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circuit designs

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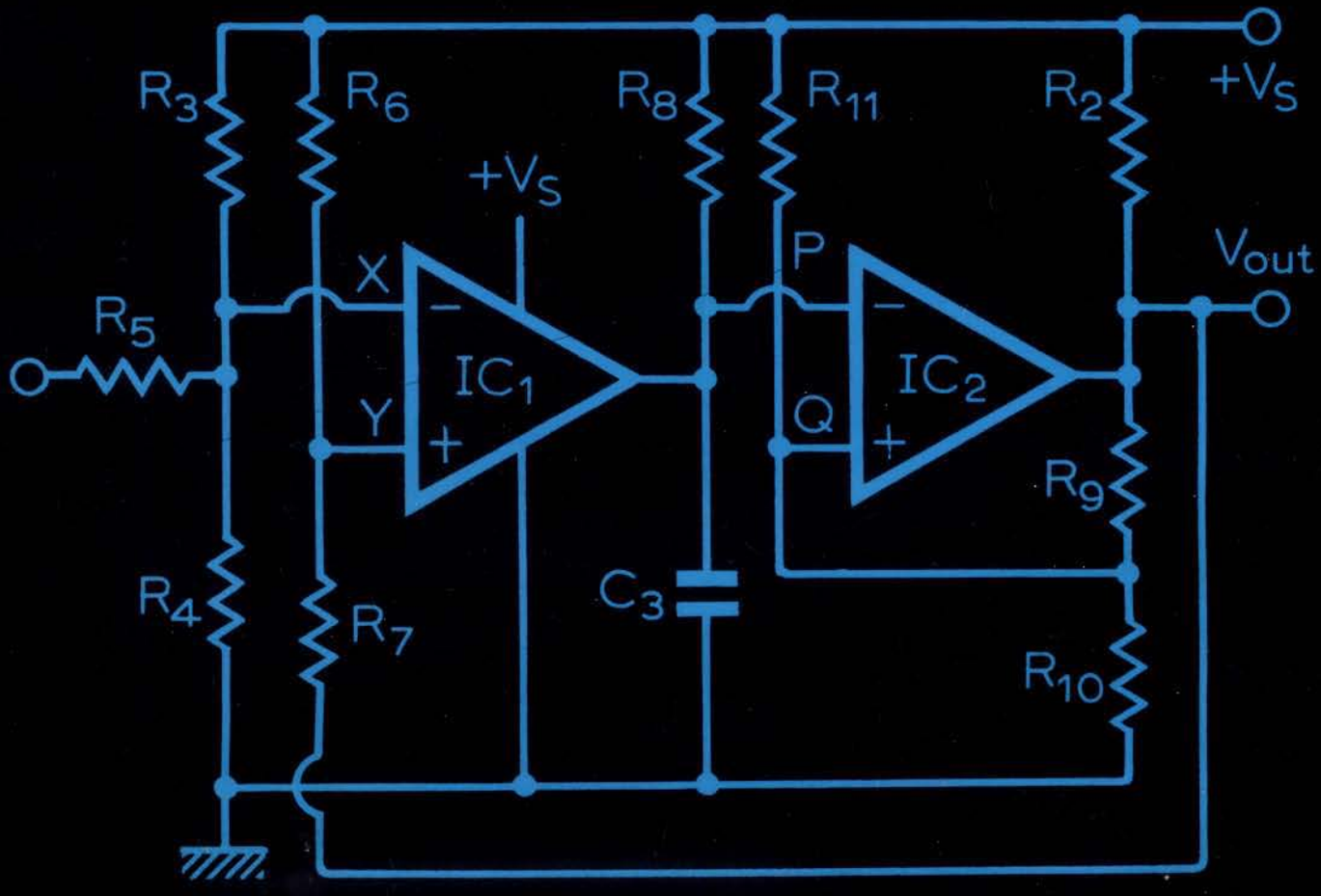
Collected Circards

P Williams / J Carruthers / J H Evans / J Kinsler



A WIRELESS WORLD PUBLICATION

In October 1972 *Wireless World* launched a circuit information system called CIRCARDS. The system was based on issued sets of 8″ × 5″ cards to complement personal filing systems. Published in conjunction with introductory articles in *Wireless World*, selected and *tested* circuits. CIRCARDS gave the subscriber descriptions of circuit operation, component values and ranges, circuit limitations, modifications, performance data and graphs.

This book is for those who design, use or understand electronic circuits. It contains information previously included on sets 11 to 20 of CIRCARDS,* corrected where necessary and supplemented with 10 pages of additional circuits. Introductory articles originally published in *Wireless World* complement each section.

The CIRCARD system won an IPC Business Press award for the best innovation of 1973.

**Sets 1 to 10 with all information was published in* CIRCUIT DESIGNS *No. 1, and is still in print.*

circuit designs

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Collected Circards

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A WIRELESS WORLD PUBLICATION
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Contents

Preface

Authors write the books they would like to read themselves. It is easy to start a book with this kind of incentive, but less easy to sustain it. Soon it becomes obvious that the author might end up as the only reader—a receptive but uncritical audience. Circards began as a response to the inordinate amount of time taken to track down a variety of solutions to each problem in the field of circuit design as it occurred. Engineers working in industry must often produce rapid solutions to problems, and rely on the knowledge and skills acquired in related areas. It is valuable to reconsider alternative approaches, since producing solutions in a hurry can so easily become a reflex action with all the possibilities of error that this implies. The question then was how to find a variety of approaches without this time delay. A first possibility was simply to make use of one of the excellent data retrieval systems (INSPEC, ISI, etc.). This would have given a list of articles on the topic together with an abstract of each—but not the circuit diagram. The time taken for the individual to track down each of the references was going to be too long, particularly as he would still have to digest them all sufficiently well to compare their merits and demerits for his particular application.

In our own work we were involved in such searches on a regular basis: in the preparation of lecture notes on unfamiliar topics; as a by-product of research for higher degrees; in the answering of queries passed on to us from local industry entering some area of electronics with which they were not yet familiar. As we had to carry out these functions anyway, it seemed to us that if we performed them in a more efficient and concentrated manner the results would be useful to a wide range of colleagues in the world of electronics.

We talked to colleagues from our own and other colleges at meetings and conferences; we quizzed industrial designers when visiting students carrying out their industrial training; we looked at the needs of amateurs trying to design their own equipment, and of technicians building circuits to often vague and contradictory specifications; and we tried listening to as well as talking to our students on their difficulties in converting theory into practice. To all these we would like to pass on our thanks. Their comments and opinions convinced us that there was a need for a circuit design service of the kind provided by Circards, and on which this book is based.

This need could not be met simply by collecting together and reprinting articles on a given topic drawn from various sources. Firstly there would be no pattern to such a collection and no easy way of comparing the performances or modes of operation. Secondly the viewpoint on each circuit would be that of the original authors; though they would be the obvious source for a discussion of the merits of their circuits, an independent judgement might be lacking. Thirdly, any measured data might be applicable only to a particular configuration or to given devices or component values. To retain the advantages of a collection of alternative solutions, while attempting to avoid the above difficulties something different was needed.

Our proposal was that we would track down the data on a given class of circuits as far as we could, and then select a number of versions for further study. After carrying out experimental work (to supplement that given in the original reference, to modify the circuit to more familiar devices or to extend its operating range in respect of supply voltages, currents, etc.) these would be written up in a standard format. Particular attention would be given to the range of operation, to the possible variation in component values and to circuit modifications. In the process it was hoped that a fair sprinkling of novel circuits would be uncovered, and that unifying features would emerge to simplify the interchange of design techniques between one class of circuit and another.

The format decided on was that of a standard file card, so that once a particular circuit had been identified by the reader as being of interest, that card could be removed for bench use while leaving the rest of the information on file. For more leisurely reference and library use this data is now collected into the present book form, together with an accompanying set of articles describing the principles underlying each topic. The original data is supplemented by a selection from recently published designs in each area, and we have tried to remove those errors and ambiguities discovered on the original cards.

In making these proposals to *Wireless World* we were delighted to find that they were received sympathetically, and would like to record our appreciation of their efforts and skills in bringing this project to fruition. Our thanks must also go to the Principal, Governors and Staff of Paisley College for their continuing encouragement. To our wives and families we can only say that without their support and encouragement this task which has brought us much satisfaction might have been started but could never have been sustained.

Peter Williams, Paisley

Postscript

"Why didn't they . . .?" Inevitably this will be the reaction of readers experienced in the design of particular circuit types described in this book. The response is simple . . . "We didn't know!".

We try to blend bench investigations with as wide a study of the technical and professional journals as possible. Fortunately we have a varied background experience, and the help and advice of colleagues to fall back on. What none of this can provide is a sense of the present and ever-changing needs of readers. In choosing topics for future publication we would welcome advice from any source—we know that errors have slipped through in the past, and have corrected in this book those that we have traced. It would be easy to minimize these errors, by sticking to standard and well-tried circuits, but that is not enough in our view. For Circards to meet the original aims there has to be a balance between the classical, the industrial standards and the novel; users and designers of electronic circuits can then take this material as the starting point for their own designs.

Information and comments on such developments would help us greatly in planning and writing future "Circuit Design" books, and would make sure that the balance of the material suits the needs of the user.

wireless world circard

Set 11: Basic logic gates

The *W.W.* article introducing this subject must have been of limited value for newcomers to logic as a result of a few typographical errors that crept in. These are corrected of course, the main errors being in lines 29 & 30 of Table 1 and in Table 6. The article forms a good introduction to Boolean algebra rules, truth tables and logic symbology (but for details of the Karnaugh map technique see article on page 60). The cards detail the different realizations of logic gates, card 4 being especially useful in summarizing the different kinds of NAND gate (standard, low power, high speed and Schottky). Card 8 is arguably the most useful giving circuits for interfacing between different kinds of logic circuits. Interfacing with analogue circuitry to form shunt or series choppers, as used in multiplexers, is covered in card 11. Three cards deal with newer kinds of logic systems. Card 9 describes the nomenclature used in threshold logic—a generalized approach of which the simple gates form special cases. Optical logic gates, three-state logic and majority gates are covered on cards 10 & 12. Set 16 card 4, and set 18 card 2 give logic circuits using current differencing amplifiers.

Basic logic gates

Logical or arithmetic processes are extensively used in systems such as industrial control, computers, electronic instrumentation and automatic telephone exchanges. These processes often involve complex functions of several variables, the desired functions being realized by switching operations in a logical manner. Although much of the design of these systems now deals with the interconnection of complex functional blocks, successful results also depend on a knowledge of the basic elements that constitute the complex functional blocks.

The basic elements of such systems are logic gates, which may perform combinational operations on their inputs. These inputs will normally be in one of two allowed states that could be, for example, two different voltages, two different currents or two different resistance values such as the limiting cases of open circuit and short circuit. Whatever form the allowed states take, a logic gate is concerned with whether certain statements about its inputs, at a given instant, are true or false. If these statements are made using normal language they become unmanageable as the number of quantities involved increases, making some form of symbolic statement highly desirable.

If a certain statement is true it is assigned the value 1 and if it is false it is given the value 0. For example, if one of the inputs to a logic gate is called A and it can be either at 5 V or 0 V then the statement "input A is at 5 V" may be true or false. If it is true than A = 1 and if it is false then A = 0. If this gate has three inputs and its output, D, is only at 5 V (D = 1) when two of its inputs, A and B, are at 5 V and its other input, C, is at 0 V, then D = 1 when A = 1 AND B = 1 AND C = 0.

Now C = 0 implies that C is NOT 1 i.e. $\bar{C} = 1$, where the bar indicates NOT or negation, so the above statement could be simply written as D = A AND B AND C. Using the multiplication sign of normal algebra (× or .) to represent the AND operation this statement becomes $D = A \times B \times \bar{C}$, or $D = A.B.\bar{C}$, or even $D = AB\bar{C}$ where the "multiplication" (AND) signs are implied. This type of algebra, based on logical statements that are true or false, is called Boolean algebra and it is a very useful tool in the development of logical thinking and in the design of digital circuits and systems.

As well as the AND and NOT operations it is necessary to postulate the OR operation which is represented by the (+) symbol of normal algebra. For example, if a logic gate has two inputs A and B, and its output D is in the logic 1 state when either A or B is in the logic 1 state this statement can be written as D = A OR B which is represented by D = A + B.

A logic gate is an example of a basic logical circuit, called a combinational circuit, the output of which at a given instant is determined by the state of its inputs. Irrespective of its complexity, certain relationships, laws and simplification rules of Boolean algebra can be used to represent or investigate the behaviour of a combinational circuit. Using up to three variables, Table 1 shows some of the properties of this algebra some of which are the same as ordinary algebra. In Boolean algebra division and subtraction have no meaning and the variables can only have the values 0 or 1. Table 2 shows the Boolean algebra theorems relating the values 0 and 1 in terms of relay contacts that are either open (logic 0) or closed (logic 1). Table 3 illustrates the Boolean algebra theorems in one variable A in similar terms, where A can have either of the states 0 (A-contact open) or 1(A-contact closed). In Table 1 relations 26 & 27 together are known as De Morgan's theorem and 29 & 30 are identical with 26 & 27 except that the variables have been negated (or inverted or complemented).

Combinational logic circuits may take many different forms, one of which employs relay contacts which is useful for illustrating some of the simple Boolean relations. For example, in Figs 1 & 2, A, B and C are contacts operated by relay

TABLE 1. Properties of Boolean algebra.

1	0+0	=0	11	$\bar{A}.A$	=0
2	0.0	=0	12	$\bar{A}+A$	=1
3	1+1	=1	13	0+A	=A
4	1.1	=1	14	0.A	=0
5	0.1	=0	15	1+A	=1
6	0+1	=1	16	1.A	=A
7	$\bar{0}$	=1	17	A+B	=B+A
8	$\bar{1}$	=0	18	A.B	=B.A
9	A+A	=A	19	(A+B)+C	=A+(B+C)
10	A.A	=A	20	(A.B).C	=A.(B.C)
21	A. (B+C)	=A.B+A.C			
22	A+A.B	=A			
23	A+$\bar{A}$.B	=A+B			
24	A.(A+B)	=A			
25	(A+B).(A+C)	=A+B.C			
26	$\overline{A+B}$	=$\bar{A}.\bar{B}$			
27	$\overline{A.B}$	=$\bar{A}+\bar{B}$			
28	$\bar{\bar{A}}$	=A			
29	$\bar{A}+\bar{B}$	=A.B			
30	$\bar{A}.\bar{B}$	=A+B			

Table 2. Boolean theorems in terms of relay contacts.

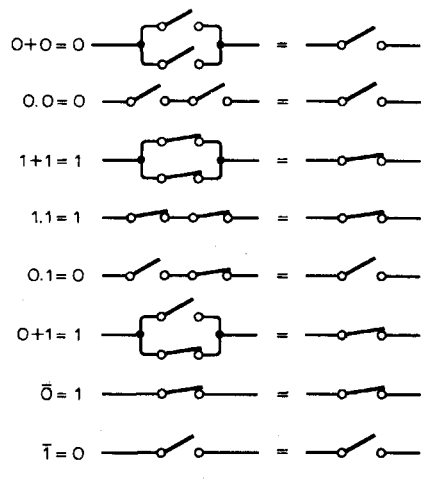
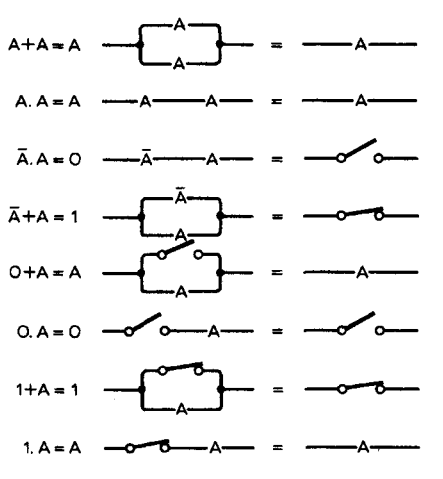


Table 3. Boolean theorems in one variable.



*All with Paisley College of Technology.

coils (not shown) to complete a path between input and output. Thus, we are concerned with the statement "the connection between input and output is complete".

When this statement is true D = 1 and when it is false D = 0. In Fig 1, D = 1 only when contacts A AND B AND C are closed simultaneously so the Boolean representation is D = A.B.C. Hence, series-connected contacts of the same type provide the AND operation. In Fig. 2, D = 1 when contacts A OR B or C are closed so the situation may be represented by D = A + B + C. If more than one contact is closed the above statement is still true, i.e. D = 1. Thus, parallel-connected contacts of the same type provide the OR (or "inclusive" OR) operation and the order in which they are wired or considered does not affect the truth of the statement.

The validity of a Boolean statement representing the behaviours of a combinational logic gate can be checked by means of a truth table. which is a tabular listing of all possible logic combinations of the variables and the resulting output logic. Tables 4 & 5 are the truth tables for Figs 1 & 2 respectively and they show that a complete truth table requires 2^n rows to represent a gate having n variables. Table 6 is a listing of the truth tables for the commonly-used combinational logic operations and shows the names given to the logic gates used to realize these operations. The NOR (NOT OR) gate performs the complement of the OR function and the NAND (NOT AND) gate the complement of the AND function.

TABLE 4. Truth table for Fig. 1

A	B	C	D
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

TABLE 5. Truth table for Fig. 2

A	B	C	D
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	1

Unlike the OR gate, the "exclusive" OR gate only makes D = 1 when either A = 1 OR B = 1 but not when A = B = 1. The exclusive OR operation is used so frequently that it is given the symbol +. Thus, $D = A\bar{B} + \bar{A}B = A \oplus B$.

Examples have been given of basic logical operations realized by means of relay contacts but this technique can become unwieldly. A more general diagrammatic representation of logic gates is desirable as the logic diagram should be independent of the circuit techniques employed in their realization. Unfortunately, there is no universally accepted symbol* to represent a particular logic gate, some of the different types of symbols that have been used being shown in Fig. 3.

While the operation indicated by a logic gate symbol is independent of the circuitry used, it should be realized that as there are two allowed states the user must decide which state is to represent the logical 1 condition. For example, if the two states are represented by voltage levels, one may be positive and the other 0 V, one may be negative and the other 0 V, one may be positive and the other negative, both may be positive or both negative. Irrespective of the values of these voltage levels, the system is said to use positive logic if the logical 1 state is represented by the more positive level and is said to use negative logic if the logical 1 state is represented by the more negative voltage level.

Although all the combinational logic gates appearing in Table 6 are available in various forms of hardware, it is possible to build complete logic systems with either only NOR gates or only NAND gates. Fig. 4 shows how the AND, OR, NOR and exclusive-OR operations may be realized using only NAND gates and Fig. 5 shows the sole use of NOR gates to

*Following a majority decision of the I.E.C., the B.S.I. have opted for the rectangular logic gate symbols (not shown in Fig. 3). BS3939 section 21 is currently being amended. — Ed.

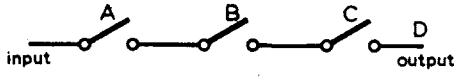


Fig. 1: D = 1 when contacts A AND B AND C are closed, represented by D = A.B.C.

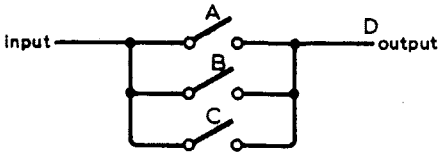


Fig. 2. D = 1 when A OR B OR C are closed, represented by D = A + B + C.

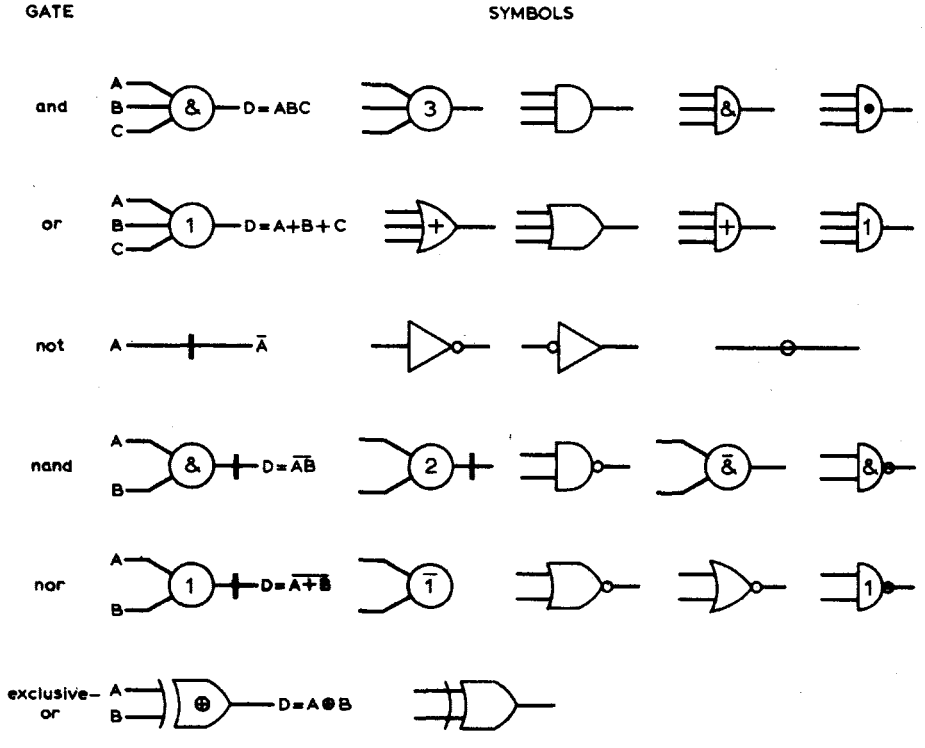


Fig. 3. Some of the symbols used for logic gates.

TABLE 6. Truth tables for common combinational logic operations.

INPUTS		OUTPUT D =				
A	B	A.B	A+B	$\overline{A+B}$	$\overline{A.B}$	$A \oplus B$
0	0	0	0	1	1	0
1	0	0	1	0	1	1
0	1	0	1	0	1	1
1	1	1	1	0	0	0
NAME OF GATE		AND	OR	NOR	NAND	EXCLUSIVE — OR

realize the AND, OR, NAND and exclusive-OR operations. These illustrations also show the application of some of the relations given in Table 1. Figs 4(a) & 4(b) use relations 28 & 30 respectively on the output function and relation 30 is also used on the output from the three-input NAND gate in Fig. 4(c). In Fig. 4(d), relations 27, 21 & 11 are used in turn on both inputs to the final gate and relation 30 used on its output function. Figs 5(a) & 5(b) use relations 29 & 28 respectively on the output function, relation 29 also being used on the output of the three-input NOR gate in Fig. 5(c). In Fig. 5(d) relation 29 is used on the input to the final gate and relations 27, 26, 21 & 11 used in turn on its output function.

These examples show that more gates of a given type are required to realize any other particular simple logic function. Although this point has been illustrated by simple Boolean expressions, in the design of more complicated systems the algebra may be cumbersome and other techniques such as Karnaugh mapping would be used to obtain a minimal solution. To synthesize a complex system it may be advisable to use gates of one type because of their availability and cost.

Many different types of solid-state electronic logic-gate realizations are available such as resistor-transistor logic (r.t.l.), diode-transistor logic (d.t.l.), direct-coupled transistor logic (d.c.t.l.), transistor-transistor logic (t.t.l.), emitter-coupled logic (e.c.l.) and complementary metal oxide transistor logic (c.m.o.s.). These families of gates have different characteristics and one family may prove to be more suitable than another in a particular application. For example, the prime consideration may be highest possible speed of operation or lowest power consumption or greatest immunity to external noise or the simplicity of interfacing the gates with other circuitry. The successful design of a digital system therefore requires a working knowledge of the capabilities of the various types of electronic gates available.

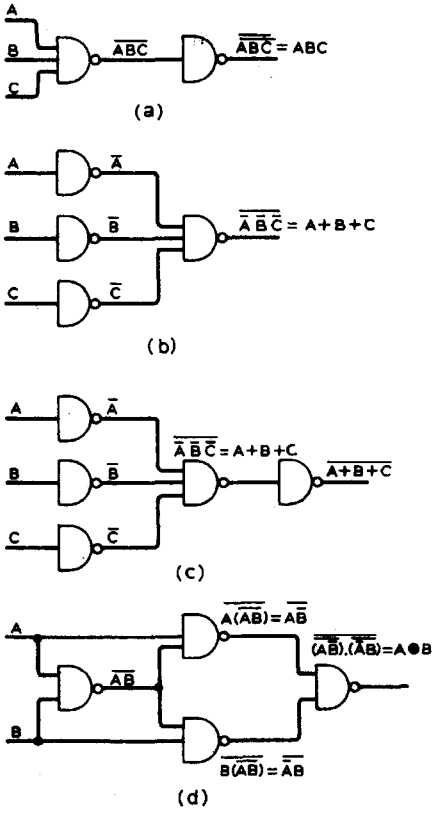


Fig. 4. Logic operations of AND (a), OR (b), NOR (c) and exclusive OR (d), can be realized using only NAND gates.

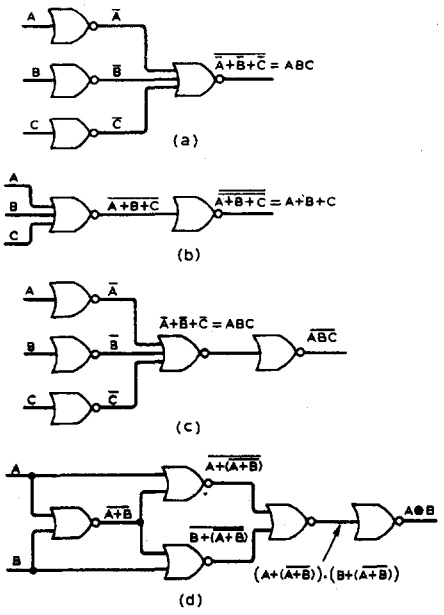


Fig. 5. NOR gates can realize the logic operations of AND (a), OR (b), NAND (c) and exclusive OR (d).

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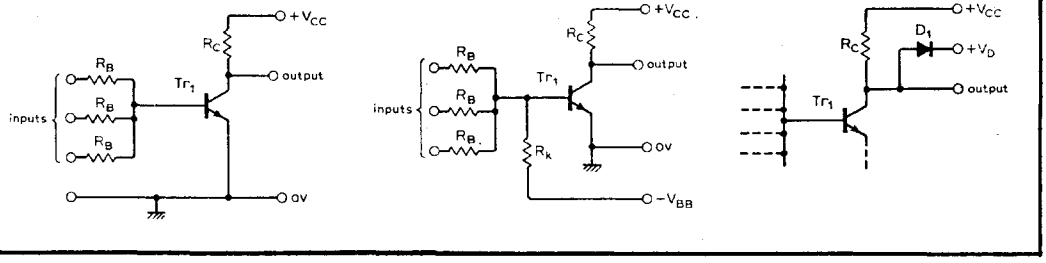
Resistor-transistor and direct-coupled gates



Typical r.t.l. parameters
$+V_{CCmin}$ 20V
$+V_{CCmax}$ 28V (4mA)
$-V_{BB}$ 0V (with silicon transistors)
R_B 82kΩ, R_K 30kΩ, R_C 7.5kΩ
logical 0 level 300mV max
logical 1 level 14V min
Fan-in 4
Fan-out 6
Maximum frequency 10kHz

Simple r.t.l.
The simplest resistor-transistor logic (r.t.l.) gate, which performs the positive logic NOR function, is shown left. A positive voltage applied to any input turns Tr_1 on, causing V_{out} to fall from V_{cc} to a value that depends on the base drive. If sufficient base drive is applied, Tr_1 saturates making $V_{out}=V_{CEsat}$, representing the logical 0 state. Positive voltages applied to the other inputs increases the degree of saturation and only change V_{out} by a small amount. If logical 0 voltages (V_{CEsat}) are supplied to all inputs the base-emitter juction of Tr_1 will be only slightly forward biased ($V_{CEsat} \approx 0.1$ to 0.4V) and $V_{out} \approx +V_{CC}$. For useful logic functions the gate must feed some load, causing an additional current I_L to flow in R_C and hence reducing the logical 1 value of V_{out} below V_{CC}. The gate is also a negative-logic NAND gate.

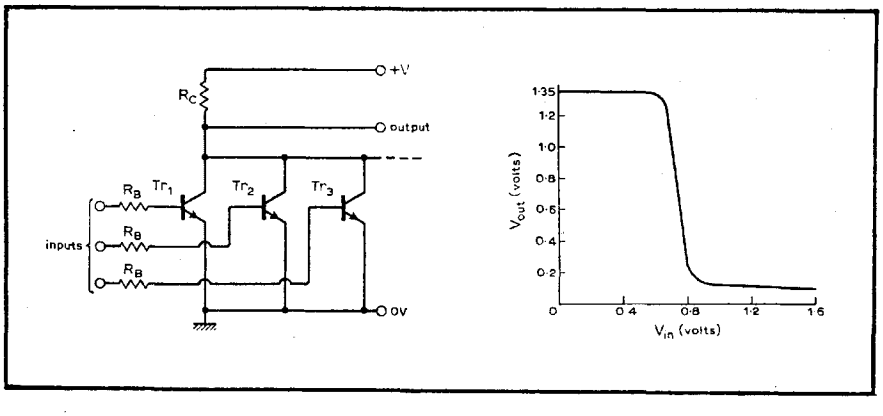
Improved r.t.l.
Inclusion of a base bias resistor, R_K in the middle circuit, returned to a negative supply ensures that Tr_1 is definitely turned off when all inputs are below the input logical 1 threshold and reduces the transistors turn-off time. Speed-up capacitors can be placed in parallel with each input R_B to produce resistor-capacitor-transistor logic. However, if all inputs are at logical 1 voltages and one of them rapidly switches to the 0-state, its speed-up capacitor couples the negative-going transition to the base-emitter junction of Tr_1 which can cause the transistor to temporarily switch off. For this reason r.t.l. gates are normally only used at fairly low switching speeds.
A clamping diode D_1, shown right, can be connected to a supply $+V_D < +V_{CC}$ to make the logical 1 output voltage less dependent on the load current, provided that the drop across R_C does not cause D_1 to become reverse-biased.

Direct-coupled logic
Direct-coupled-transistor logic is also referred to as direct-coupled logic and collector-coupled-transistor logic, but it is strictly incorrect to refer to it as resistor-transistor logic as is done by some manufacturers since the input resistors have no logic function. The base resistors bottom serve only to divide the current between transistors when their inputs are paralleled. The gate is a positive-logic NOR gate which uses the transistorsas summing elements. The transistors also provide input- output isolation and restoration of the logic levels in each gate in a cascade. A positive voltage at any input turns on its associated transistor causing V_{out} to fall to V_{CEsat}, the logical 0 level. With all inputs at logical 0 the transistors are virtually cut off causing V_{out} to rise towards $+V$ until the transistors in the following gates turn on.
For correct operation R_C and R_B values must be chosen to ensure that driven transistors turn on when the driving gate transistors turn off. Also, when the driving gate is on the driven transistors must be off, hence the threshold value of V_{BE} must exceed V_{CEsat}. The difference between these two values influences the gate's noise immunity. Discrete-circuit versions allow individual trimming of the base resistors to compensate for unequal V_{BE} values. Integrated circuit versions have closely-matched V_{BE} and V_{CEsat} values due to simultaneous manufacture on the same substrate.
Fan-in capability is limited by collector leakage currents which, for several transistors off simultaneously, could cause V_{out} to fall below the level required to ensure that the following transistors are turned on. This is particularly so in low-power versions of the gate. A typical transfer characteristic is shown below.

Further reading
Dokter, F., & Steinhauer, J. Digital Electronics, chapters 4 & 5, Macmillan, 1973.
Harris, J. N. *et al* Digital Transistor Circuits, chapters 6 & 7, Wiley, 1966.

Typical d.c.t.l. parameters

Parameter	normal	low-power
+V	3.6V	3.6V
R_C	640Ω	3600Ω
R_B	450Ω	1500Ω
Fan-out	5	5
Gate dissipation	12mW	2.5mW
Propagation delay	24ns	45ns
logical 1 level	1.2V	1.2V
logical 0 level	200mV	200mV
Noise margin, min ("1")	400mV	400mV
Noise margin, min ("0")	350mV	350mV



Diode-transistor gates

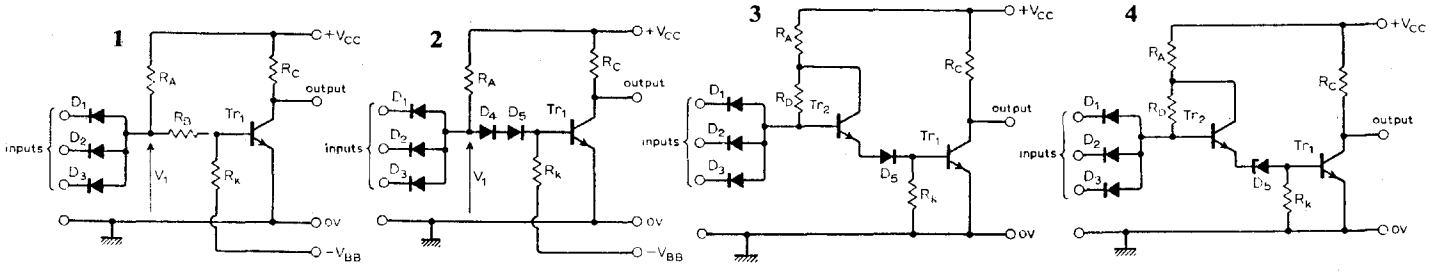


Fig. 1 shows a diode-transistor logic (d.t.l.) NAND gate, using discrete components, which is effectively a diode-logic AND gate followed by an inverting transistor. Resistors R_A, R_B and R_C act as a level-shifting potential divider designed to provide enough base drive to allow Tr_1 to saturate, making $V_{out} = V_{CEsat}$ (logical 0), when all input diodes conduct due to logical 1 levels being present at all inputs. If any input is at logical 0 V_{CEsat}, its associated diode conducts, causing V_1 to fall to the forward voltage of the diode. The transistor is then held in the cut-off state by the reverse bias obtained by potential division of V_{BB} between R_K and R_B and the output goes to the 1-level as its collector rises towards $+V_{CC}$. The turn-off of Tr_1 is assisted by the negative base voltage and the turn-on time may be reduced by shunting R_B with a speed-up capacitor. The fan-in is that of a diode logic gate and the fan-out depends on the current-sinking ability of Tr_1. Preservation of logic levels may be improved by including a collector clamp diode—see card 1.

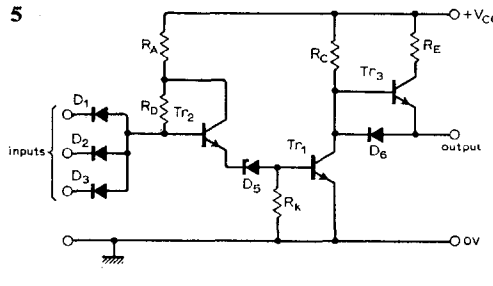
Another version of the d.t.l. NAND gate, sometimes called low-level logic, is shown in Fig. 2 where R_B and its speed-up capacitor are replaced by the input-offset diodes D_4 and D_5, which are more suitable for monolithic integrated fabrication techniques. Only a relatively small voltage swing is required at the base of Tr_1 to switch it on or off, but in Fig. 1 a relatively large swing in V_1 is required to achieve this due to the large part of V_1 lost across R_B. The use of D_4 and D_5 in Fig. 2 leads to a much smaller required swing in V_1 to achieve the desired base voltage swing. Hence the signal levels may be lowered to reduce gate dissipation which also falls due to the removal of R_B.

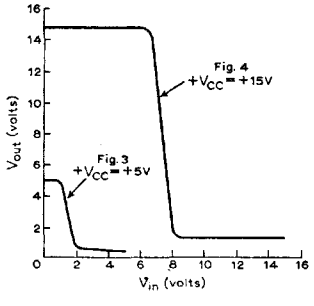
Other diodes may be placed in series with D_4 and D_5 to improve noise immunity. While the input diodes should have a very short reverse recovery time, the level-shifting diodes D_4 and D_5 should be slow recovery types to ensure that they do not return to their high-impedance, reverse-biased state until Tr_1 has cut off. Elimination of the V_{BB} supply can simplify circuitry in many instances, a popular modified form of the d.t.l. NAND gate using a single supply being shown in Fig. 3. In comparison with Fig. 2, the offset diode D_4 is replaced by Tr_2 and R_D. This transistor provides amplification that allows a higher level of base drive to be fed to Tr_1, achieving a higher fan-out capability, and also permits a reduction in the value of R_K compared with Fig. 2.

Gates used in industrial logic systems often require high noise immunity, rather than high speed and low power dissipation, as large transients can be produced in supply lines or picked up at inputs due to switching of relays, etc. Fig. 4 shows a modified form of Fig. 3 that exhibits higher noise margins largely due to D_5 being changed from a forward-biased diode to a reverse-biased diode exhibiting a zener-type characteristic when the p.d. across it reaches about 6.7V. Thus the input threshold voltage is increased by an amount equivalent to the p.d. that would occur across a further four forward-biased diodes connected in series with D_5 in Fig. 3, but is achieved by using only one such diode operating on its reverse characteristic. A higher supply voltage is required in Fig. 4 but to prevent large increases in currents, and hence gate dissipation, all resistor values are also increased. Fig. 6 shows typical transfer characteristics for the circuits of Figs. 3 & 4. Fig. 5 shows the high noise-immunity gate of Fig. 4 with an active pull-up transistor Tr_3. When Tr_1 is off R_C supplies base drive to Tr_3 which supplies load current via R_E. With the output in the 0-state Tr_3 is off and Tr_1 sinks load current through D_6 which causes the low logic level to exceed V_{CEsat} of Tr_1. The table shows a comparison of some typical parameters for integrated circuit versions of Figs. 2 to 5.

Typical d.t.l. parameters

Parameter	Fig. 2	Fig. 3	Fig. 4	Fig. 5
$+V_{CC}$	4V	5V	15V	15V
$-V_{BB}$	2V	—	—	—
R_A	2kΩ	1.6kΩ	3kΩ	3kΩ
R_C	2kΩ	6kΩ	15kΩ	15kΩ
R_D	—	2.15kΩ	12kΩ	12kΩ
R_E	—	—	—	1.5kΩ
R_K	20kΩ	5kΩ	5kΩ	5kΩ
Fan-out	5	8	10	10
Gate dissipation	10mW	10mW	28mW	28mW
Propagation delay	30ns	30ns	125ns	110ns
Noise margin ("1")	0.4V min	0.4V min	5V	5V
Noise margin ("0")	0.35V min	0.35V min	5V	5V





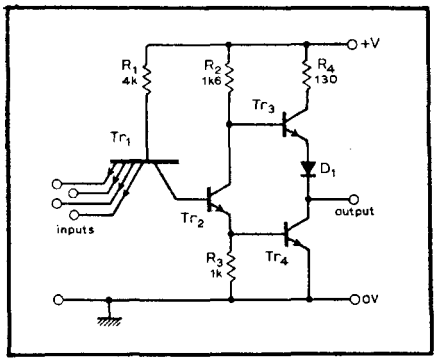
Further reading

Dokter, F. & Steinhauer, J. Digital Electronics, chapters 4, 5 and 6, Macmillan, 1973.

Meindl, J. D. Micropower Circuits, chapter 11, Wiley, 1969.

wireless world circard

Basic t.t.l. gate



Typical parameters
Temperature range: 0 to 70°C
+V min 4.5V, +V max 5.5V
"0" supply current 22mA max
"1" supply current 8mA max
Fan out 10 t.t.l. loads
Inputs:
"0" level 800mV max
"1" level 2V min
"0" level 1.6mA max at +V max
"1" level 40μA max with V_{IN}=2.4V

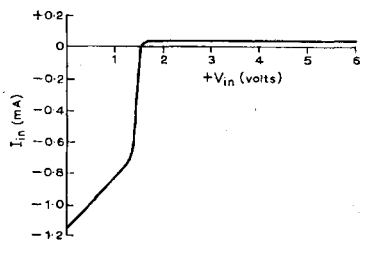
Outputs:
"0" level 400mV max at +V min
"1" level 2.4V min at +V min
"0" level 16mA
Short-circuit output current: 18 to 55mA at +V max
Propagation delay* from "1" to "0" 15ns max
Propagation delay* from "0" to "1" 22ns max
"1" noise margin 400mV min
"0" noise margin 350mV min
Gate dissipation 10mW
*With output loaded by 400Ω//15pF.

Circuit description
Circuit shows the form of the basic transistor-transistor logic gate which performs the positive logic NAND function and which may normally have up to eight inputs. If all the inputs are at a high level (logical 1), base drive is provided to Tr_2 through R_1 and the base-collector junction of Tr_1. If any one or more input is at a low level (logical 0), the current in R_1 flows through the base-emitter junction of Tr_1 to ground. The base will then be only V_{BE1} above V_{IN} and Tr_2 cut off due to lack of base drive. Transistor Tr_1 thus performs the AND function as its collector is only high if all its inputs are high. Transistor Tr_2 acts as a phase splitter that saturates with only a moderate current gain—note the small ratio of R_1/R_2 with $R_2 \approx R_3$. When Tr_2 is cut off its collector and emitter are approximately at +V and 0V respectively. When Tr_1 drives Tr_2 on, its emitter rises to V_{BE4} and its collector falls to ($V_{BE4}+V_{CE2sat}$). In this state Tr_4 will be saturated so that the output will be at V_{CE4sat} (logical 0) when all inputs are in the high state. In this condition the gate can sink current through Tr_4 from a number of loads, normally a maximum of 10, in the 0-state, without causing V_{CE4sat} to rise above the acceptable 0-threshold.
If any of the gate inputs is in the low state, Tr_4 will be off as Tr_2 is cut off. Transistor Tr_3 will be on to an extent determined by the emitter current demanded at the output. This current will be small when the gate feeds a number of similar t.t.l. gates and its base current will be smaller still. Hence the p.d. across R_2 due to Tr_3 base drive will be negligible and the output will be in the high state with V_{out} at approximately $+V-(V_{D1}+V_{BE3})$.

Switching action
When switching the output from the 0- to the 1-state, all inputs are initially high (logical 1). As the potential of one or more input falls, nothing happens until it reaches about 1.4V, when the source current via Tr_1 base-emitter junction prevents base current flowing to Tr_2 via the base-collector junction of Tr_1, which rapidly removes the stored charge from Tr_2 base and switches it off. The collector potential of Tr_2 starts to rise as this transistor turns off, but stops rising as Tr_3 begins to conduct heavily. This conduction occurs because Tr_4 has not yet switched off, as the charge stored in its base decays only relatively slowly through R_3. Therefore, a large current spike of short duration and limited in amplitude by R_4 occurs in the supply line during the switch-off action due to Tr_3 and Tr_4 being simultaneously on. This conduction in Tr_4 removes some of the stored base charge, allowing the output voltage and Tr_2 collector potential to rise. The rise continues until Tr_3 becomes cut off and the output settles to the 1-level. Typical input, output and transfer characteristics are shown in Figs. 2, 3 & 4 respectively. Width and amplitude of the current spike are virtually unaffected by the rate at which the gate is switched on and off. Hence a side effect of the current spike is an increase in power consumption as the switching frequency increases.

Unused inputs
Inputs that are unused in a particular application should be connected in parallel with used inputs for fastest switching speed. Unused inputs can be left open circuit, but excessive pick-up noise may result unless the open circuit is made at the integrated circuit package connection. If unused inputs are connected to the positive supply rail, it is advisable to do so via a resistor of around 1kΩ to prevent the gate being damaged by a supply line transient that exceeds the maximum rating.

Further reading
Scarlett, J. A. Transistor-Transistor Logic and its Interconnections, chapters 1 to 6, Van Nostrand, 1972.

2


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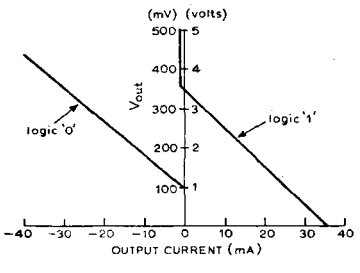

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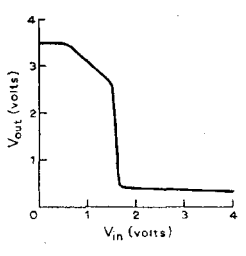
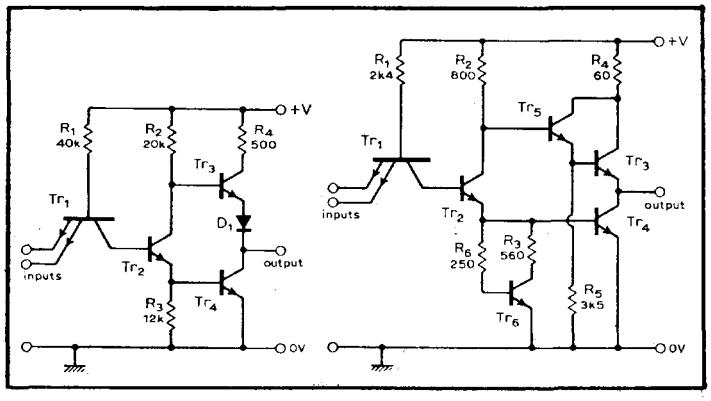


NAND gate variations in t.t.l.



In the basic, or standard t.t.l. NAND gate (card 3), the resistance values affect performance. Resistor R_1 influences the rate of rise of voltage at Tr_2 base and turn-on time. Gate dissipation, when the output is in the 0-state is affected by the value of R_2. Stored base charge in Tr_4 is removed via R_3 when the output state changes from logical 0 to 1. Turn-off time of the gate when feeding a capacitive load is influenced by the value of R_4 which provides short-circuit protection.

Low-power t.t.l.
For low-power operation the resistor values must be increased to reduce the charging-discharging currents. But larger resistors imply slower switching speeds unless transistor size is reduced to lower their capacitances. This can be done due to the lower current levels and by reducing the degree of gold doping the transistors achieve higher current gains to better-utilize the smaller currents. The resulting gate, top left, has a power dissipation only one-tenth of that in a standard gate with a speed reduction penalty of only three times.

High-speed t.t.l.
To obtain higher switching speeds than are obtainable with standard t.t.l., the charge-discharge rates of the integrated and external capacitances must be increased. This implies larger transistor currents and hence lower resistor values. The higher currents require larger transistors having increased capacitances that tend to offset the speed increase due to higher currents. A distinct speed improvement is obtainable, the high-speed NAND gate shown above having about double the speed and slightly more than twice the dissipation of the standard gate.
The Darlington-connected pull-up transistors Tr_5 and Tr_3 provide higher active-region gain which reduces the output resistance and increases the ability to drive capacitive loads. Resistor R_5 is sometimes returned to the output point, rather than to the 0-V rail, to reduce the gate dissipation. Sometimes a by-pass transistor, Tr_6, is added to the pull-down transistor, Tr_4, as shown right. Resistance of the discharge path for stored base charge in Tr_4 is reduced, improving the turn-off time. Transistor Tr_2 cannot conduct through R_3 until its emitter voltage exceeds the turn-on V_{BE} of Tr_6 which is approximately the same as that of Tr_4. Hence, the output remains in the 1 state until V_{IN} rises to a level sufficient to turn on Tr_4, which removes the low-slope region from the transfer characteristic improving noise immunity.

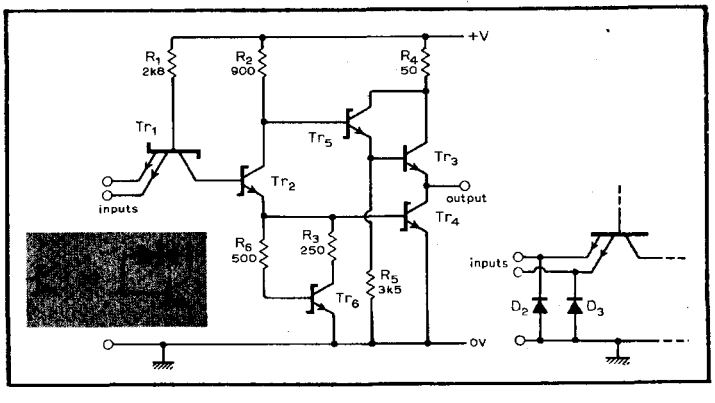
Schottky-clamped t.t.l.
Excess base drive is shunted through the diode, which clamps the collector-base junction with a p.d. of 400mV which is insufficient to produce any significant forward conduction. The elimination of gold-doping provides higher-gain, physically-smaller transistors with very little charge storage and hence much higher switching speeds without the penalty of further increased power dissipation. Use of Schottky-clamped transistors increases the output 1-level improving its noise immunity. Transistor Tr_4 below has very little stored base charge, improving the turn-off time and reducing the supply current spike. As this transistor's V_{CEon} determines the output 0-level, the level will be raised by about 100mV compared with the standard gate but its value will be far less temperature dependent. The table shows a comparison of some typical parameters of different t.t.l. NAND gates.

Input clamping diodes
Most t.t.l. gates have input clamping diodes to ground, as shown on right to reduce the negative excursions of input signals due to ringing caused by reflection of pulses along the interconnection transmission lines.

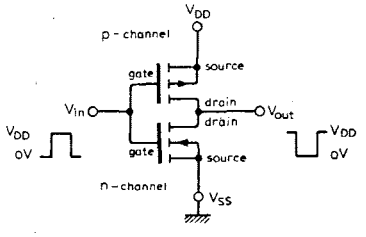
Further reading
Priel, U. Take a look inside the t.t.l. i.c. *Electron*, pp. 24, 26 & 30, 19 April 1973.
Murphy, R. H. Performance and reliability aspects of current trends in t.t.l., *New Electronics*, pp. 30, 33 & 34, 20 April 1971.
Clifford, C. Guide to low-power t.t.l., *New Electronics*, pp. 24, 27 & 28, 4 May 1971.
Scarlett, J. A. Transistor-Transistor Logic and its Interconnections, chapters 3, 4 & 9, Van Nostrand, 1972.

Cross references
Set 11, card 3; set 10, card 11.

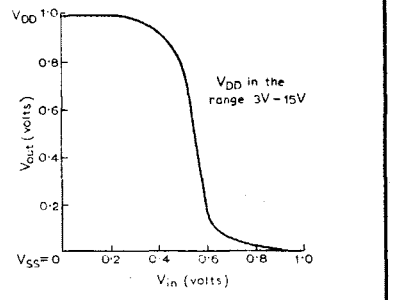
Parameter	standard	low-power	high-speed	schottky
+V	5V	5V	5V	5V
"0" current	5.5mA	0.46mA	10mA	9mA
"1" current	1.3mA	0.18mA	4.2mA	4.25mA
Fan out	10	10	10	10
Gate dissipation	10mW	1mW	22mW	20mW
Output delay "1" to "0"	8ns	30ns	6ns	3ns
Output delay "0" to "1"	12ns	30ns	6ns	3ns
Noise margin "1"	400mV	400mV	400mV	700mV
Noise margin "0"	400mV	400mV	400mV	300mV
V_{INmax} "0"	800mV	700mV	800mV	800mV
V_{INmin} "1"	2V	2V	2V	2V
V_{OUT} "0"	400mV	300mV	400mV	500mV
V_{OUTmin} "1"	2.4V	2.4V	2.4V	2.7V
I_{IN} "0"	1.6mA	0.18mA	2.0mA	2.0mA
I_{IN} "1"	40μA	10μA	50μA	100μA
I_{OUT} "0"	16mA	2mA	20mA	20mA



Complementary m.o.s. gates—1



Typical data
IC $\frac{1}{3}$ (CD4007AE)
Working voltage range (V_{DD} $-V_{SS}$) 3 to 15V
Temperature range -40 to $+85°C$
Input capacitance 5pF
Input resistance $> 10^9\Omega$
Output voltage (high) 9.99V
($V_{DD} = 10V$, $V_{SS} = 0V$)
Output voltage (low) 0.01V
($V_{DD} = 10V$, $V_{SS} = 0V$)
Fan-out d.c. > 1000
a.c. typically 20

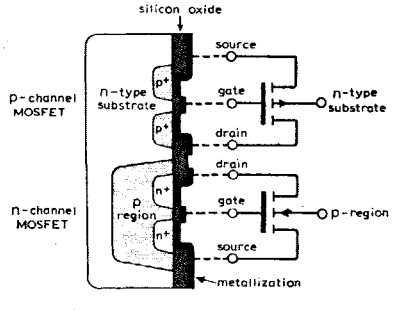


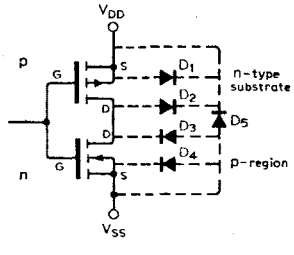
Description
The circuit shows the basic complementary-symmetry isolated-gate inverter stage, which uses both an n-channel and a p-channel enhancement-mode m.o.s.f.e.t. in a series-pair configuration. Such circuits can be directly coupled as either transistor will be in its non-conducting or off-state if its gate-source voltage is zero. Individual gates are tied together to form a single signal input gate, and the drains are commoned at the output. Assume that the input signal excursion is from $+V_{DD}$ to ground potential i.e. $V_{SS} = 0V$. When the input is $+V_{DD}$, the n-channel f.e.t. is biased to a high conducting state because V_{GS} is a high positive value. Simultaneously, the effective gate-source voltage of the p-channel f.e.t. is zero, and hence this transistor will be off, and the output will be at ground potential. When the input goes to zero volts (the low or 0-state for positive logic), the n-channel f.e.t. is biased off, but the p-channel transistor has now a large negative voltage between gate and source and is therefore biased into conduction, and the level then approaches $+V_{DD}$ (the high or 1-state). In either logic state, one transistor is conducting and the other is cut-off. It follows that the quiescent power dissipation is exceedingly low—the transistor that is off will only conduct leakage current, typically 1nA.

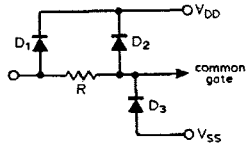
More significant power dissipation occurs during the switching from one level to the other, due to both a current spike which occurs when the inverter is in its linear region and to the charging and discharging of load capacitance. This depends on the frequency, the value of the capacitance and the square of the supply voltage.
If the p-channel source is connected to ground, the n-channel source should be connected to $-V_{DD}$ and the drive signal excursion should be from $-V_{DD}$ to 0V.

Construction
A cross-section depicting the formation of n-channel and p-channel transistors on the same chip is shown below, with associated symbols. The p-channel one is formed directly on an n-type substrate, but the n-channel device is formed in a p-region diffused into the substrate. This process creates parasitic diodes, and their relationship to the inverter terminals is shown centre. As V_{DD} is normally more positive than V_{SS}, these diodes are in a reverse-biased state, and their leakage current contributes to quiescent power dissipation. It should be noted that if the voltage level at the output terminal is subjected to any transient condition, it is unable to go more positive than V_{DD} or more negative than V_{SS}, by more than the forward conducting voltage of these parasitic diodes.

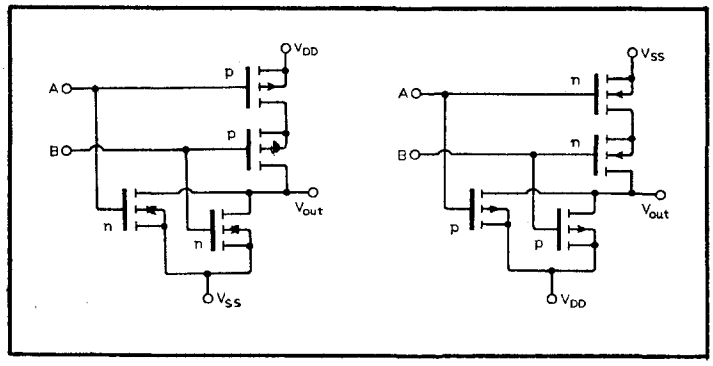
Input protection
Because the input resistance of the device is so high, static charges may be sufficient to charge the input capacitance of the gate oxide to a high enough voltage to cause breakdown ($\sim 100V$). The diode protection network, below right is one type designed into some gates. If the gate terminal voltage is greater than V_{DD}, diodes D_1 and D_2 can conduct, and if less than V_{SS}, D_3 may conduct—the current magnitude should be limited to around 10mA (R may be around $2k\Omega$). For conditions where the diodes are either forward or reverse biased, the voltage across the oxide layer is limited to approximately 1 or 25V respectively.







Complementary m.o.s. gates—2



Typical data
$V_{DD} = +10V$, $V_{SS} = 0V$, T_{amb} 25°C.

Gate	drive p(source) (mA)	V_{out} (V)	drive n(sink) (mA)	V_{out} (V)	quiescent power (μW)	delay (ns)
Nor	1.0	9.5	2.5	0.5	0.05	25
Nand	1.2	9.5	0.6	0.5	0.05	25
Inverter-pair	2.5	9.5	2.5	0.5	0.05	20
Buffer	2.5	9.5	16.0	0.5	0.5	10 to 25

Basic gate structure
NOR and NAND functions are formed by series and parallel combinations of p and n pairs. For the NOR gate, the n-type f.e.ts are in parallel and the p-type in series as shown left. The circuit configuration of the NAND is similar but the p-types are in parallel, the n-types are in series, and the supply connections are changed over, see diagram right. The NOR logic action is described assuming V_{DD} is a positive voltage and Vss is at 0V. Input excursions at A and B will be within the range 0V to V_{DD}. If either A or B is positive, then one of the p-types will be off and one of the n-types on, thus connecting V_{out} to 0V via the on-resistance of the conducting transistor. If both A and B are positive, again the output will be at 0V. If A and B are at 0V, then both p-types will be biased on, due to the negative voltage at their gates, and both n-types will be off, and hence V_{out} will be at $+V_{DD}$.

General notes
Noise immunity. Typically the input may change by up to $0.45V_{DD}$ before the output begins to alter. Over the full range of $V_{DD} - V_{SS}$ (3 to 15V), a noise immunity of $0.3V_{DD}$ is guaranteed.

Unused inputs. NOR gates: Connect input terminals together or to the lower voltage terminal Vss. NAND gates: Connect input terminals together or to the voltage terminal V_{DD}.

Parallel gates. Gate outputs may be connected in parallel allowing greater output currents at the expense of increased power dissipation—current hogging need not be considered.

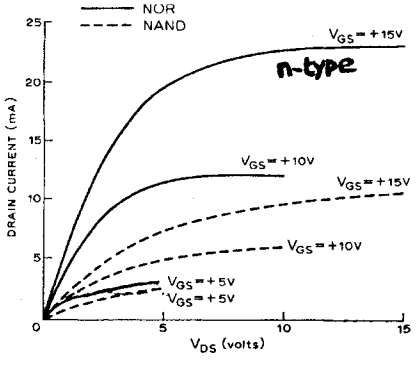
Pulse drive. Rise and fall times should be less than 5μs typically to prevent the device spending too long in the linear region during switching and thus increasing power dissipation.

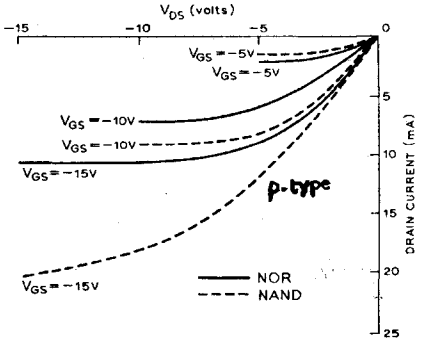
Output characteristics
The two graphs shown left illustrate typical n-device and p-device drain current characteristics for the NAND and NOR gate. Drain currents for the n-type in the NOR gate are much higher than those available in the NAND gate for the same gate-source voltage.

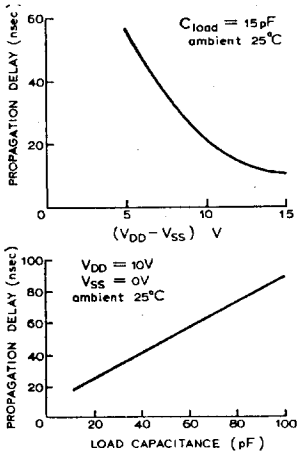
Propagation delay
Delay periods are usually defined between 50% points on the input and output level transitions, and this will depend to a great extent on the capacitive loading at the output, as this itself affects the transition time. Third graphs show that typical propagation delays depend on supply voltage, though in the 10 to 15V region the delay spread is of the order of 10ns.
As the capacitive loading is increased (each c.m.o.s. gate is an effective 5pF load), it is fairly easy to slow down.the circuits with external capacitance (right). The propagation delay is also temperature-dependent, increasing as the temperature increases due to fall-off in the g_m of the transistors.

Development
Devices have been produced which operate with V_{DD} values (V_{SS}=0V) in the range 1.1 to 1.6V, and recently 0.7V. Another technology known as dielectric isolation, applicable to both types of c.m.o.s., promises devices with propagation delays as low as 10ns.

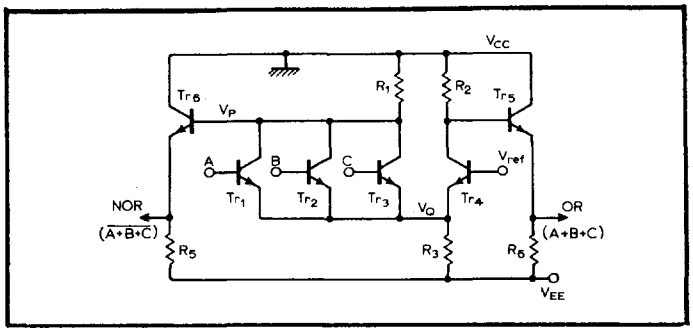
Further reading
Harrison, L., CMOS—Tolerant logic, *Electron*, 3 May 1973.
Ankrum, P. D., Semiconductor Electronics, Prentice-Hall.
Bishop, R. A. Complementary m.o.s. offers many advantages to the digital-systems designer, *Electronic Engineering*, Nov. 1972, pp. 67–70.
Funk, R. E. & Bishop, A. C.o.s.m.o.s. simplifies equipment design, *New Electronics*, 1 May 1973, pp. 24–8.







Emitter-coupled logic



Circuit description

"Emitter-coupled logic" (e.c.l.) describes integrated logic circuits in which the switching transistors do not saturate as in other forms of bipolar transistor logic. Delays due to charge-storage effects in the saturated mode are avoided, leading to faster switching.

The above diagram is one form of a three-input basic e.c.l. gate, whose outputs provide an OR and the complementary NOR logic functions. The reference voltage must be well regulated, and of a level midway between the logic swings. For nominal logic high and low output of -0.75V and -1.55V respectively, this indicates $V_{ref} = -1.15$V. The following evaluation is for guidance only. If inputs A,B,C, are at the low logic level, Tr_1, Tr_2 and Tr_3 are cut off, Tr_4 is conducting and hence the potential at Q with respect to ground, assuming 0.75V drop across all emitter-base junctions, will be -1.9V, and the voltage across R_3 is $V_{EE} - V_Q$. Assume V_{EE} is -5V, then $I = 2.6$mA. This means that the drop across R_2 is 0.78V and therefore the OR output will be -1.53V. As there is no current through R_1, V_P is 0V, and the NOR output is thus -0.75V due to the base-emitter junction drop.

When a logical 1 (-0.75V) is applied to, say, terminal A transistor Tr_1 will conduct harder than Tr_4, and the current in R_3 is then supplied via R_1, i.e. the current has been diverted from Tr_4 because the input voltage to Tr_1 is half a logic level more than that of V_{ref}, and the resultant reduction of the base-emitter drops of Tr_4 is sufficient to decrease its emitter's current to almost zero. Hence the base of Tr_5 is now at 0V and the OR output will be logical 1 at -0.75V. The related NOR is determined from the new V_Q value of -1.5V, and hence the p.d. across R_3 is -3.5V and thus $I = 2.9$mA. Therefore the p.d. across R_1 will be -0.78V and hence the NOR output is -1.53V.

● A temperature-compensated regulator package of the form shown left is available as the reference voltage, also frequently on the same chip as the gate structure. This minimizes variation of noise margin with temperature.

Faster circuits

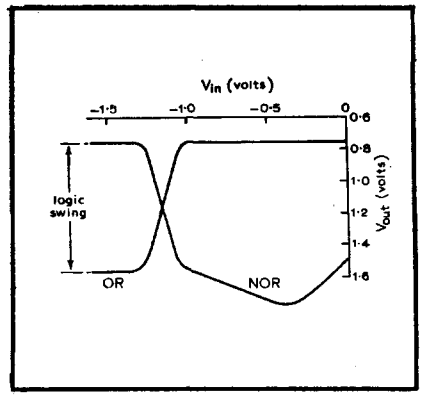
● Centre circuit shows a type of e.c.l. gate where the reference is at ground potential. With the supplies shown, logic levels nominally -400mV for logical 0 and $+400$mV for logical 1. Suitable for driving into 50Ω loads, and up to 25mA d.c. when terminated in 50- and 270-Ω pull-down resistor to -3.2V.

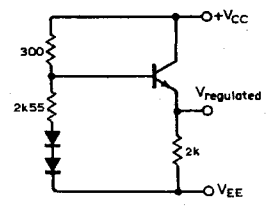
Fan-out: 12 (a.c.)
Propagation delay 2 to 3ns
Input level (high) 0.15 to 0.72V
Input level (low) -1.5 to -0.15V
Unused inputs: connect to -1V ± 50%.
Noise margin: ±200mV.

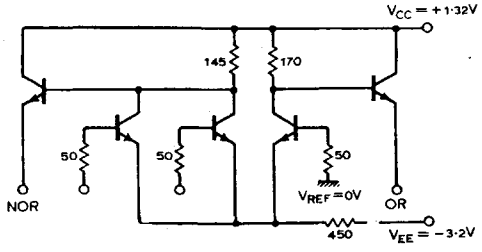
● Other e.c.l. gates with a basic configuration similar to the first provide multi-input, multi-emitter follower OR/NOR outputs, with optional pull-down resistors.

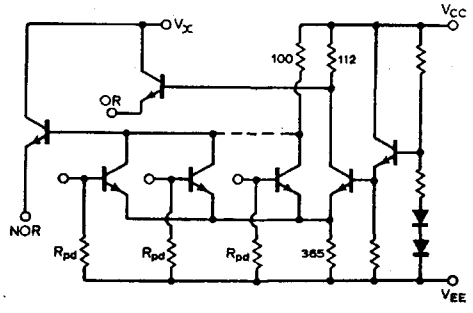
$V_{CC} = 0$V, $V_{EE} = -5.2$V ± 20%
Output (source) current: up to 2.5mA.
Operating temperature range -55 to 125°C
Propagations delay (rising) 3.5 to 5ns
Fall-time propagation delays up to 15ns due to emitter-follower output resistance and capacitance loading.
Three outputs tied together (wired OR) gives output impedance of about 2.5Ω.
Suitable for driving 50-Ω loads (two pull-down resistors only for faster fall times).
Noise margin 175mV
To maintain high speed, limit interconnection length to <25cm
Fan-in: 20; fan-out: 15 (a.c.)

● Basic form of ECL circuit capable of propagation delay <1ns is shown right. A separate supply terminal V_x is used for the output emitter-followers. V_{EE}: -5.2V. Pull-down resistors of 50 or 2kΩ provide a path for leakage currents (unused inputs can be open-circuit) and act as loads for driving gates. Power dissipation ≈55mW.
Fan-out = 70 for $R_{pd} = 50$kΩ.
Fan-out = 7 for $R_{pd} = 2$kΩ.
Propagation delay:
0.9ns for 510-Ω load.
1.1ns for 50-Ω load.
Interconnections should be 50-Ω microstrip transmission lines and termination connected to -2V supply.
Temperature range 0 to 75°C.
Logic swing typically -0.9V ("1") to -1.75V ("0").









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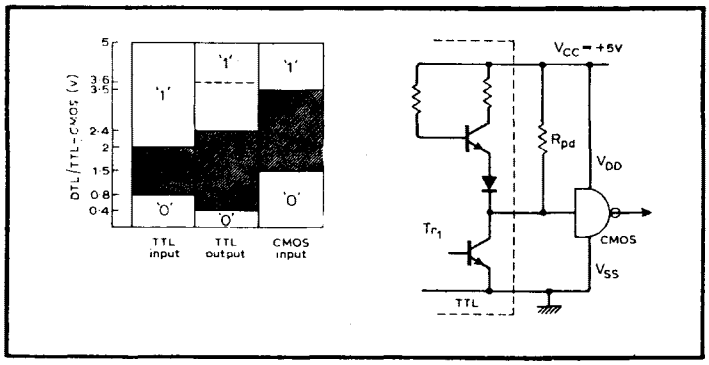
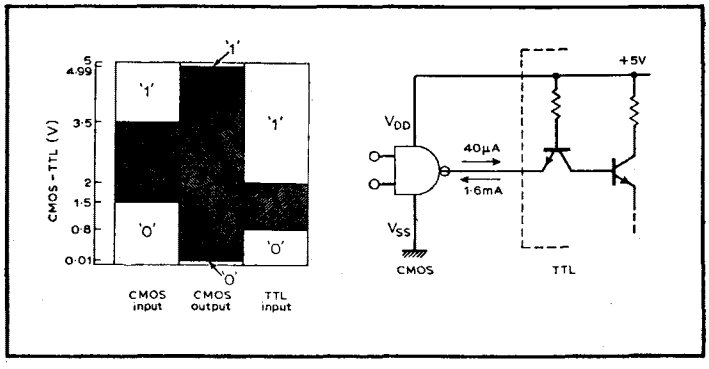
Interfacing



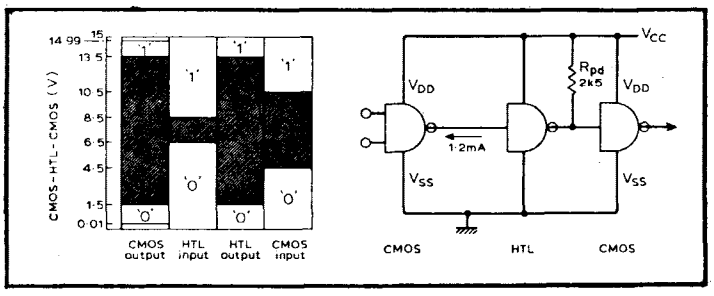
d.t.l./t.t.l.-c.m.o.s.
The minimum t.t.l. 2.4V 1-level output is normally for a load current of 400μA, but as the c.m.o.s. gate input current is approximately 10pA, the more likely 1-output is 3.6V. This is an inadequate noise margin (0.1V) and an active pull-up resistor typically 1 to 10kΩ depending on whether high speed or low power is required) is connected from the t.t.l. output to the positive supply rail of +5V.

Hence when Tr_1 is off the c.m.o.s. input will be at +5V giving a 1.4V noise margin. The threshold values of switching for the c.m.o.s. gate is typically 30% and 70% of the supply voltage, i.e. 1.5V and 3.5V respectively.
Note. Unshaded areas represent the 1- and 0-regions, the borders being the minimum 1-level and the maximum 0-level for minimum and maximum t.t.l. supply voltages.

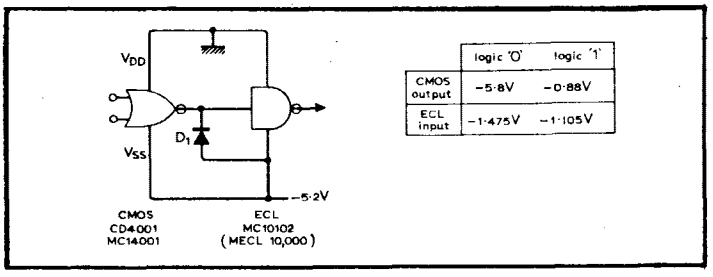


c.m.o.s.-t.t.l.
The c.m.o.s. gate must sink 1.6mA and source 40μA for the 0- and 1-state of the bipolar input respectively. Not all c.m.o.s. devices can cope with one t.t.l. load (1.6mA) but gates on the same package may be paralleled to increase their current sinking capability, or preferably buffers such as CD4009, CD4041, CD4049 should be used. These devices can sink two t.t.l. load currents and still have an output of 0.4V, thus retaining a 0.4V noise margin.

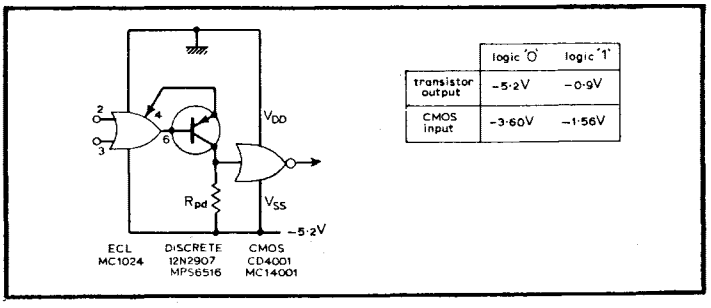
Low-power t.t.l.-c.m.o.s.
Most c.m.o.s. devices can drive low-power t.t.l. directly as the logic zero-level sink-current is 0.18mA. Again for driving c.m.o.s., the t.t.l. output should have a pull-up resistor for adequate noise margin.



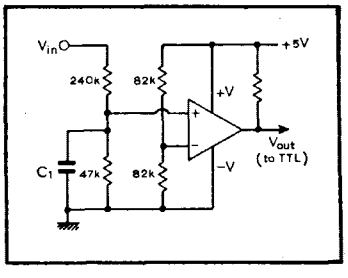
c.m.o.s.-h.t.l.-c.m.o.s.
Most high-threshold logic gates operate from a V_{CC} supply of 15 $\pm$1V. Hence direct connection with c.m.o.s. gates is possible. Noise immunity is high, of the order of 3V for high and low h.t.l. outputs, though this may be improved using a pull-up resistor as shown (in some i.cs this may be internal) which also improves the output rise-time. Rise and fall times of around 1μs should be the aim for the h.t.l.-c.m.o.s. interface.



c.m.o.s.-e.c.l.
Both may be operated from −5V $\pm$20%, but speed is restricted to 1MHz. Speed is increased if Vss is taken to a separate supply between −5 and −15V. The clamp diode D_1 keeps e.c.l. drive to a minimum of about −5.8V. Above typical figures indicate a high level noise margin of 225mV, and a low level of 4.3V.

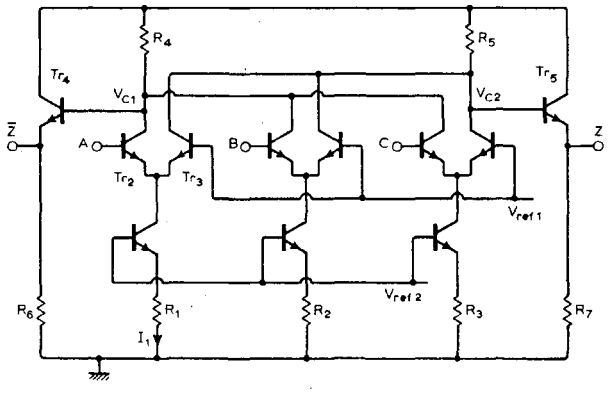


e.c.l.-c.m.o.s.
Output swing of e.c.l. (typically −1.55 to −0.75V) is inadequate to drive c.m.o.s. directly, i.e. switching levels are 30% and 70% of −5.2V. One technique is to use a two-input expandable gate driving a p-n-p transistor, with a pull-down resistor ($\approx$3kΩ) to the negative supply. This provides noise margins amplitudes of 1.56 and 0.66V.



h.t.l.-t.t.l.
Circuit shows a technique for interfacing high level logic to t.t.l. This uses a linear voltage comparator LM311, the component values used allowing an input level range of 0 to 30V. Capacitor C_1 may be added to decrease the effects of fast noise spikes.

Threshold logic



Circuit data

Supply 6V. R_1, R_2, R_3 1.5kΩ. R_4, R_5 560Ω. R_6, R_7 3.3kΩ. V_{ref_1} 4.9V, A=B=C=V_{ref_1}+100mV. V_{ref_2} 1.8V. Sequentially applying A, B & C, Z changes in 0.4V steps from 3.9 to 5.1V. "1"=5.1V (V_{ref_1}+200mV), "0"=4.7V or less (V_{ref_1}−200mV).

V_{ref_1} can be reduced towards V_{ref_2} but cannot be increased much beyond 4.90V. R_4 and R_5 can be varied but are generally tied to the values for R_1, R_2 and R_3 (ref. 1) and to the voltage swing required.

Circuit description

Threshold logic gates are much more powerful and flexible than are the normal AND, OR gates. Majority, minority, AND, and OR gates are simply particular cases of threshold logic. A threshold gate has inputs A, B, C ... with weights a, b, c ... associated with the respective inputs. The output Z from such a gate is then:

$Z=1$ if $<aA+bB+cC+\ldots>\geqslant$ some value T_1, the upper threshold, and $Z=0$ if $<aA+bB+cC+\ldots>\leqslant$ some value T_2, the lower threshold. $T_1>T_2$ and normal arithmetic addition is involved in the above brackets. The output is more precisely written as:

$Z=<aA+bB+cC+\ldots>_{T1:T2}$

T_1-T_2 is the threshold gap and is that inadmissible sum which will give an ambiguous output. Generally A, B, C, ... are binary (1 or 0); a, b, c ... need not be, but generally are, integers in which case the weighed sum can only take on integral values. The threshold performance is then quoted by those to integers between which switching takes place. We then obtain:

$Z=<aA+bB+cC+\ldots>_{t1:t2}$

where t_1 and t_2 are integers, $t_1-t_2=1$, and $t_1-t_2>T_1-T_2$.

The symbol used is shown (left).

Circuit shows a three-input threshold gate with identical weighting on each input. Basically it comprises three long-tailed pairs with a constant-current source (e.g., Tr_1 and R_1) in each tail. When A exceeds V_{ref_1} by 100mV or more the tail current flows through Tr_2 and R_4 and when A is less than V_{ref}, by more than 100mV the current flows through Tr_3 and R_5. Resistors R_4 and R_5 act as summing resistors, summing the currents from the long-tailed pairs. Transistors Tr_4 and Tr_5 act as emitter-follower output stages for V_{C_1} and V_{C_2} so that $Z=V_{C_2}-V_{be}$ and $\bar{Z}=V_{C_1}-V_{be}$. When Z is in the high state it must exceed V_{ref_1} by 100mV or more so that a succeeding stage will recognize it as logical 1. Likewise in the low state Z must be less than V_{ref} by 100mV or more.

The following formulae apply to the circuit.

● $I_1=\dfrac{V_{ref_2}-V_{BE}}{R_1}$; I_2 and I_3 are obtainable similarly.

● When I_1 is switched from R_5 to R_4 on application of logical 1 at A, then the change in $V_{C_2}=I_1R_5$. This change should be around 200mV or more to obtain decisive switching.

● Max $Z=V_{CC}-V_{BE}$ and occurs when no current flows in R_5.

● Min $Z=V_{CC}-V_{BE}-3I_1R_5$. This assumes that all the tail currents are identical and flowing in R_5.

As shown, all three inputs must be applied before Z goes to logical 1. Hence:

$Z=<A+B+C>_{3:3}\equiv Z=$ A.B.C(Boolean). Clearly if any of the inputs is permanently tied to logical 1 we obtain a two-input AND gate. Moreover, if V_{ref_1} is dropped to 4.5V only two of the inputs are required to be high for Z to be 1 and hence:

$Z=<A+B+C>_{2:1}\equiv$simple majority gate.

If now C (say) is permanently tied to logical 0 we require the two remaining inputs to be high and we have obtained a two-input AND gate. On the other hand, if C is permanently tied to logical 1 only, one of the remaining inputs requires to be logical 1 for Z to be logical 1 and hence we have obtained a two-input OR gate.

Alteration of R_4 and R_5 is more generally used to alter the threshold[1].

If R_4 and R_5 are different then the outputs from Tr_4 and Tr_5 will not be the logic complement of one another. Any other threshold logic function that one wants can be obtained within the restriction that the weightings will remain the same. Furthermore if, say, R_5 is comprised of a string of series resistors then one can obtain a large number of different functions as well as the basic one[2].

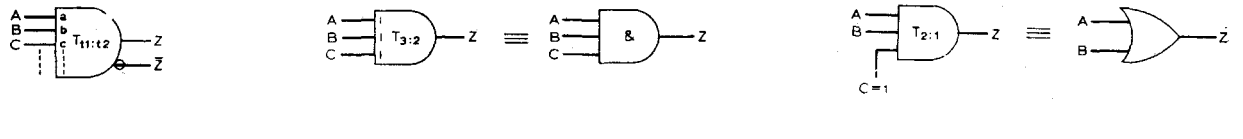
Reference 3 shows how one can improve the tolerance of the circuit to large input voltages which otherwise can cause saturation and incorrect current summation.

Further reading

Hurst, S. L. Introduction to threshold logic, *Radio and Electronic Engineer*, 1969, pp. 339–51.

1. Hampel, D. & Winder, R. O. Threshold logic, *IEEE Spectrum*, May 1971, pp. 32–9.
2. Hampel, D. Multifunction threshold gates, *IEEE Trans. on Computers*, vol. C-22, Feb. 1973, pp. 197–203.
3. Hurst, S. L. Improvements in circuit realisation of threshold logic gates, *Electronic Letters*, vol. 9, 1973, p. 123.

See also card 12.



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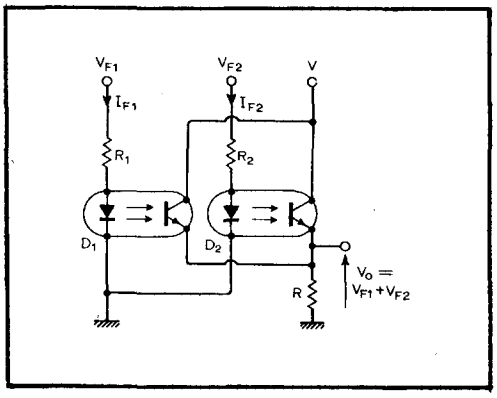
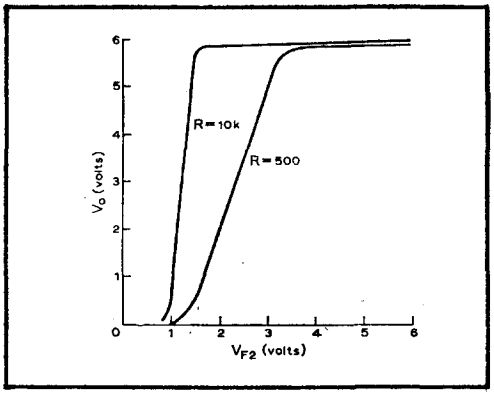
Optical logic



Performance data
R_1, R_2 100Ω
R 10kΩ and 500Ω
V 6V
V_{F_1}=0 and
V_{F_2}=0→6V giving
I_{F_1}=0 and
I_{F_2}=0→50mA
optocouplers TIL112
These figures resulted in graph (right)



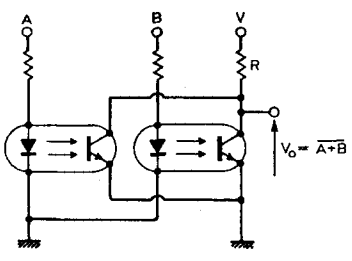
Circuit description
All the simple logic functions can be performed using optical couplers. Fan-out or speed difficulties preclude the use of these gates in complete logic system but in systems where simple logic is required and/or the input is in optical form, they can be very useful and show the usual advantages of optical coupling (cross ref. 1). Circuit shows an OR gate using optical couplers. If V_{F_1} is large enough (>1.2V) to make D_1 conduct then Tr_1 conducts and V is applied to R. Similarly V is applied to R if V_{F_2} is high and if both V_{F_1} and V_{F_2} are high. Hence, in Boolean terms, $V_o = V_{F_1} + V_{F_2}$. The transfer characteristic shown right for two different values of R indicates the static performance and shows noise immunities superior to that of t.t.l. For these two values of R with the given V the photo-transistors are being operated in their saturated mode (cross ref. 1) which permits a maximum current through each transistor of approximately 15mA. The normal parallel type of fan-out is, therefore, only one since the required I_F of succeeding stages is in the range 10 to 50mA. However, serial connection of succeeding stages could yield a fan-out of two or three if the appropriate resistance were chosen. This fan out could be increased if V were increased or, if speed was not essential, by using opto-couplers with Darlington output stages. The fan-in can easily be increased. Note that basically the drive signal is the diode current rather than the applied voltage so that current driving can easily be employed. Moreover V_{F_1} and V_{F_2} need not be the same, nor indeed do the two diode currents. All that is necessary is that each transistor be driven into saturation. With the quoted data pulse repetition frequencies of 40kHz can be handled. Higher frequencies but with lower current handling capacity can be obtained using photo-diodes and lower frequencies with greater current handling capacity with photo-darlingtons (cross ref. 2).

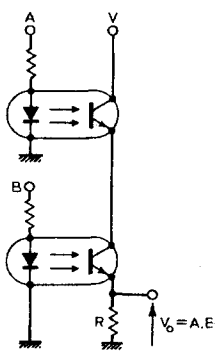
Component changes
V can be increased to 30V.
V_{F_1} and R_1 can be varied so long as I_{F_1} is in the range 10–50mA. Similarly for V_{F_2} and R_2
Optocouplers: ISO-LIT12, MCT26.

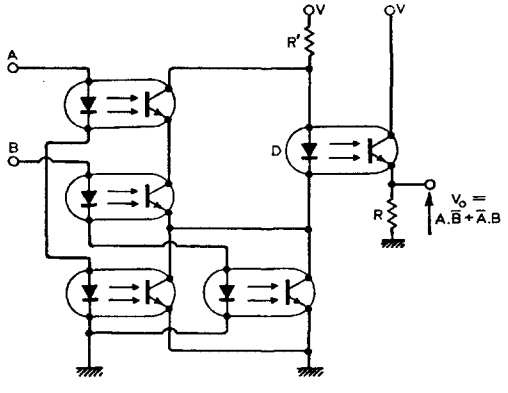
Modifications
- A NOR gate can be constructed as shown left, in which the load R is placed in the positive supply rail.
- An AND gate can be constructed as shown centre. In this case V_o when in the 1-state will be the supply volts minus the sum of the two saturated collector-emitter voltages.
- A NAND gate can be constructed by placing the load R in positive supply line.
- An exclusive-OR gate can be constructed as shown right. Current flows through D and hence in R only when A or B, but not both, are "1". R′ serves to limit the current drawn from the supply when both A and B are "1".
- Negative supply voltages can be used if p-n-p opto-transistors are used.

Cross references
Set 9, cards 8 & 9.

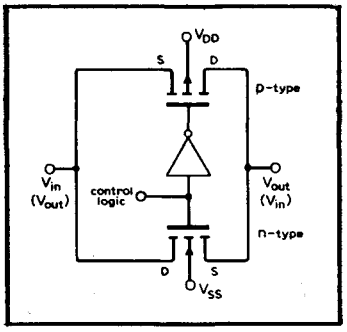
Circuit modifications



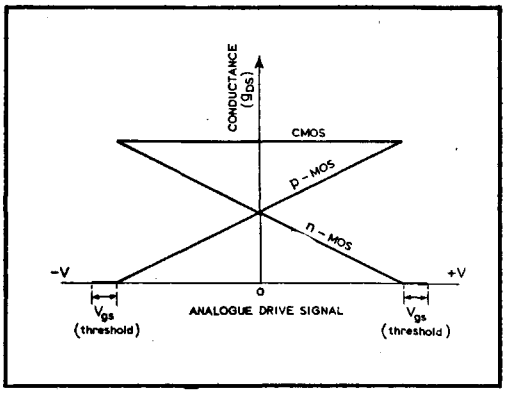




Analogue gates



Typical data
IC: ¼(CD4016AE), ¼(MC14016CL)
Supplies (max): $V_{DD}=+7.5V$, $V_{SS}=-7.5V$
or $V_{DD}=+15V$, $V_{SS}=0$
Input analogue signal range: ±7.5V or 15V peak
'on' resistance: 300 to 1kΩ (typical)
'off' resistance: 1000MΩ (typical)
Feedthrough capacitance: 0.2pF
Transfer function linearity: <0.5% distortion into 10kΩ load and ($V_{DD}-V_{SS}$)> 10V
Frequency range: up to 10MHz

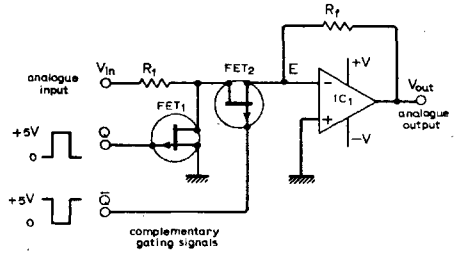


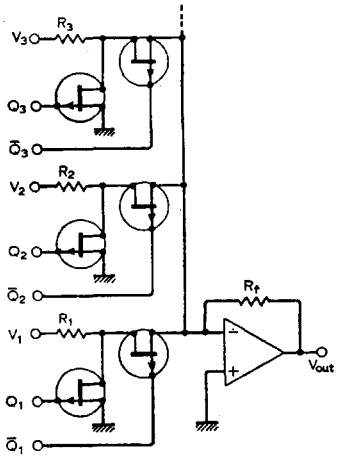
Circuit description
An analogue gate may be considered as an electronic switch which serially connects an analogue signal to a specific input point on the occurrence of a logic or control signal. This is the basis of many multi-channel multiplexers.
One gate that is particularly useful is the c.m.o.s.transmission gate. This comprises a series-pair inverter and two complementary transistors connected in parallel as shown, which allow bi-directional current flow when a control or logic signal is applied to the inverter. High and low signals are applied to the separate gates, and hence both transistors are either on or off simultaneously. The sources and drains of the parallel transistors are tied together, and either terminal may be driven by analogue or digital signals, and the excursion must be within the range of the supply, V_{SS} to V_{DD}.
If the control level is lowered to the V_{SS} rail both transistors are off. This is because the gate-source voltage of the p-type transistor will be zero or positive, and the n-type transistor gate-source voltage either zero or negative for a drive-signal swing limited to $V_{DD}-V_{SS}$. When the control signal is at V_{DD}, both transistors tend to be in the on-state. When the drive signal rises towards V_{DD}, the p-type f.e.t. will conduct harder because its gate-source voltage will increase negatively. At the same time the n-type f.e.t. conductance will begin to fall, as its positive gate-source voltage is decreasing. The resultant effect is for the parallel arrangement to exhibit a fairly constant conductance and hence constant resistance. The graph is an idealized characteristic and assumes first-order linearity of n-m.o.s. and p-m.o.s. device conductance g_{DS} against input voltage, to give a constant g_{DS} for the parallel connection. The actual characteristics exhibit some non-linearity, but the effect on the output-input voltage transfer function is most evident only at low supply voltages (e.g., $V_{DD}=V_{SS}=-2.5V$).

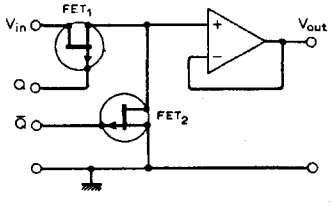
Circuit modifications
● Circuit left is a shunt-series chopper circuit using p-channel junction f.e.ts to gate the analogue signal. The f.e.ts must be fed in antiphase and can be driven from t.t.l. logic provided the f.e.t. pinch-off voltage is less than 4V. When Q is high ($\bar{Q}$ low), Tr_2 is conducting and Tr_1 is off. As Tr_2 is connected to a virtual earth point E, then the signal level at this f.e.t. input is minimum and hence the gate voltage exceeds the sum of the signal voltage and the f.e.t. pinch-off value, a necessary condition for switching. When $\bar{Q}$ is high, Tr_2 is off, and the signal is grounded via the on resistance of Tr_1. The analogue swing is limited by the maximum signal swing of the i.c. amplifier, and the speed of switching will depend on the slew rate of the amplifier.
Tr_1 & Tr_2 2N5461, IC 741 or LM301A, $R_1=R_f=10$ to 33kΩ
The junction f.e.ts may be replaced by p-m.o.s. depletion types with similar pinch-off.
● Further, similar, chopper circuits may be connected to the virtual earth point to provide a signal multiplexer (middle). Signals V_1, V_2 and V_3 can be gated in turn by applying complementary control signals to the $\bar{Q}$, Q terminals in sequence, say from a ring-counter.
● The arrangement right, a series-shunt chopper, is best suited to voltage sources as neither the op-amp or Tr_2 draws significant current when Tr_1 is on, or when Tr_1 is off. The current from the source is negligible. Hence the input signal is gated to the op-amp with almost zero attenuation.

Further reading
CD4016A Data Sheet, RCA Solid State Databook Series SSD 203A.
Johnson, P. A. Complementary m.o.s. integrated circuits, *Wireless World*, vol. 79, August 1973, pp. 395–400.
Givens, S. FETs as analog switches, *Electronic Components*, 26 January, 1973.
Honey, F. J. DTL/TTL controls large signals in commutator, *Electronics*, March 1970, p. 90.
Jenkins, J. O. M. Interface circuits drive high-level switches from low-level inputs, *Electronic Engineering*, May 1971.

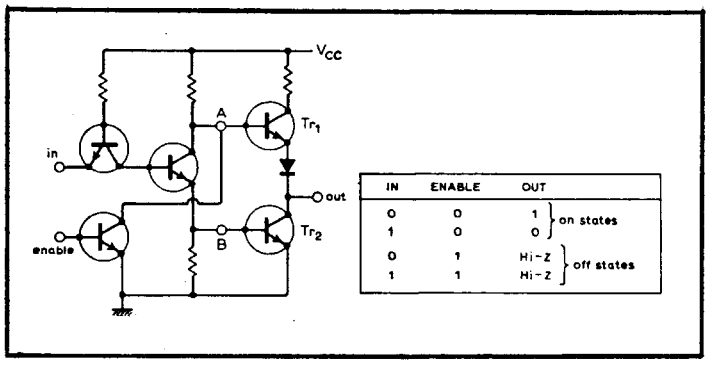
Circuit modifications







Three-state and majority logic



Three-state gates

Three-state logic (t.s.l.) is now available from at least three companies: National Semiconductor, Texas Instruments and Signetics. Flip-flops, multiplexers, demultiplexers, line drivers, counters and r.o.ms are among the devices available in this form. The three states are normal 1 and 0 levels plus an off state which represents a high impedance condition in which the gate can neither sink nor source current—effectively an open circuit. Referring to the diagram, if the enable signal is logical 0 then normal logic inversion of the input signal is performed. However, if the enable signal is logical 1, then the input signals are overridden and the device goes into its hi-Z or off state as point A and with it point B are grounded. Hence, both Tr_1 and Tr_2 are switched off and present a high impedance to the load. This means, for example, that a large number of gates can be connected by means of a bus to a single load, only one gate at a time being connected to the load, all others being in the hi-Z state. If the number of gates connected to the bus is high then the leakage current (typically 40μA) of the off devices must be taken into account as the single on-device is supplying the load plus the leakage of all the off-devices. For this reason t.s.l. gates normally have a Darlington-connected upper output stage and this increases the source current capability by an order of magnitude over that for normal t.t.l. This in itself is an advantage of t.s.l. which in addition has the usual advantages of t.t.l. with respect to other logic families. The increased source current capability also carries with it a much reduced one-level output impedance which gives a one-level noise immunity an order of magnitude better than that for t.t.l.

To ensure in a bus-organized system that no two devices are ever on at the same time, all t.s.l. devices are arranged such that the time delay from on to off is less than that from off to on. Nevertheless, overlaps can occur and although no damage is done to the devices transients resulting from this or any other source can be longer than in a t.t.l. system, principally because more gates will probably be connected to the output of a t.s.l. device and this gives rise to increased load capacitance. Note that all t.s.l. devices are fully t.t.l. compatible and that three-state buffer gates are available to convert any d.t.l. or t.t.l. device into a t.s.l. element.

Further reading

Calebotta, S. *Electronic Design*, vol. 20, no. 14, 6 July 1972, pp. 70–2.

National Semiconductor, Digital Integrated Circuits Data Book.

Majority logic gates

A majority logic gate is a form of threshold logic gate where the numerical "weight" assigned to each of its inputs is unity. Majority logic uses combinational gates that provide an output in the 1-state (true) only when more than half of the inputs are in the 1-state. To realize this requirement when the number of inputs in the 1-state exceeds the number of inputs in the 0-state by only one (an input majority of one), majority gates normally have an odd number of inputs.

It has only recently become possible to design systems based on standard integrated-circuit packages employing majority logic. These packages are of the 16-pin dual-in-line type and contain two identical majority logic gates, each having five inputs and using c.m.o.s. technology. Such majority logic gates allow the design of certain functions, such as those required for communication in the presence of noise and correlation methods, that are difficult to implement with other types of gate.

The flexibility of the majority gate can be seen by comparison with the normal AND, OR, NAND and NOR gates which select one input combination from a possible 2^n combinations of n inputs, whereas the majority gate can select 2^{n-1} of the 2^n inputs. A majority gate with only three inputs is possible, as shown left, having an output function $K=AB+AC+BC$ and, on inversion, this can produce the NOR majority function $K=\overline{AB+AC+BC}$.

The output function of the 5-input majority gate, shown centre, is more complex and is:

$K=ABC+ABD+ABE+ACD+ACE+ADE+BCD+BCE+BDE+CDE.$

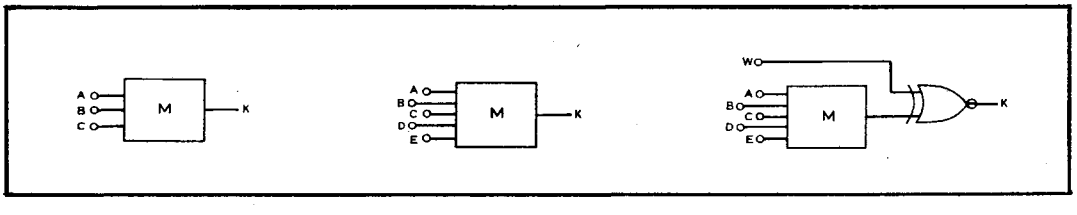
By feeding this function to an exclusive-NOR gate together with another function, that may be at logical 0 or logical 1, further flexibility is introduced. When the W-input is at logical 1 (right) K provides the above 5-input majority logic function, $K=M5$ (say), and when $W=0$ inversion occurs making $K=\overline{M5}$. With $D=1$ and $E=0$, K provides the majority of the three inputs A, B and C when $W=1$ ($K=M3$) and the NOT majority function $K=M3$ when $W=0$. With $D=E=1$, K provides the three-input OR function when $W=1$ and the three-input NOR function when $W=0$. With $D=E=0$, the three-input AND function is realized when $W=1$ and this becomes the three-input NAND function when $W=0$.

Further reading

Garrett, L., C-MOS may help majority logic with designers' vote. *Electronics*, vol. 46, no. 15, 19 July 1973, pp. 107–12.

Cross references

Set 11, cards 5, 6 & 9.



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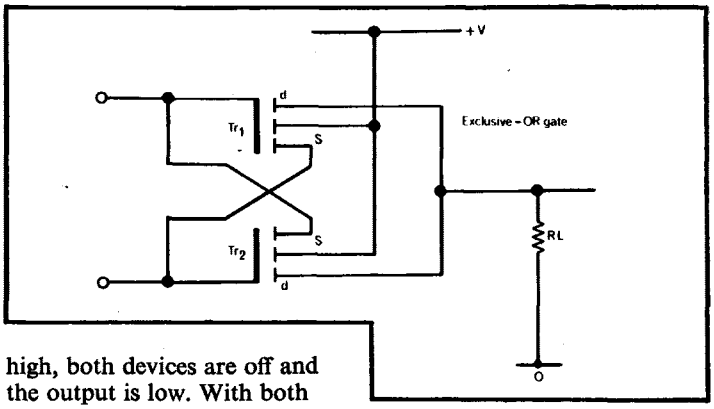
Set 11: Basic Logic Gates Up-date

1. A novel form of logic gate has been proposed recently that allows relatively complex logic functions to be constructed using a small number of components. They are compatible with existing i.c. processes and can be implemented using devices from standard i.cs. No power gain is available as the active devices are used as series switches, i.e. cascaded gates suffer from loss of signal level as with earlier diode gating systems. In the example shown, two p.m.o.s. enhancement-mode transistors are used. With both inputs



high, both devices are off and the output is low. With both inputs low, the devices are off because again each device has $V_{gs}=0$. Only if one input is high and the other low is one device put into a conducting state is the output taken high. The symmetrical nature of the circuit shows that it does not matter which is taken high, e.g. if A is high and B low, then Tr_2 conducts raising the output close to A (the difference depending on the on-resistance of Tr_2 compared with R_L). The circuit thus implements the exclusive-OR function, and the reference describes other arrangements both m.o.s. and bipolar for producing logic functions with fewer-than-normal components.

Reference

Edwards, C. R. Some novel exclusive-or/NOR circuits, *Electronics Letters*, 1975, 11, pp. 3/4.

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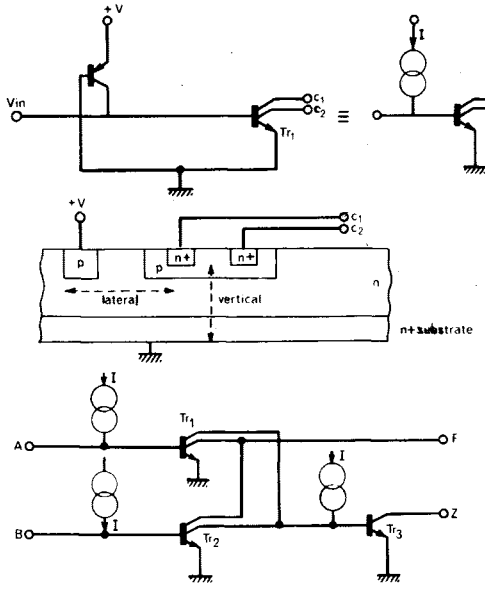
2. Integrated injection logic I^2L has the lowest speed-power product of presently available gates (1975), and a much higher packing density. The structure is such that the n-p-n transistor Tr_1 is vertical and the lateral p-n-p transistor serves as both a current source and as an active load. Tr_1 has multiple collectors c_1 and c_2. With the input of the I^2L gate high (or floating, corresponding to the previous gates being off), then Tr_1 is biased on by the p-n-p current source. Then its outputs are capable of sinking the currents from the current sources at the inputs of the gates to which they are connected.



If V_{in} < 700mV, the injected current will be diverted through the low output of the driving gate; hence no base current to p-n-p transistor and the collectors will depend on potential to which they are connected. The OR/NOR gate shown provides $F=\overline{(A+B)}$ and $Z=(A+B)$. If either input A or B is high, Tr_1 or Tr_2 conducts and F is low. Also, as then the wired-OR connection to the base of Tr_3 is low, Tr_3 is off, and Z tends to be high. Note that I^2L input/output connections are not connected directly to the package pins, but via appropriate buffer networks.

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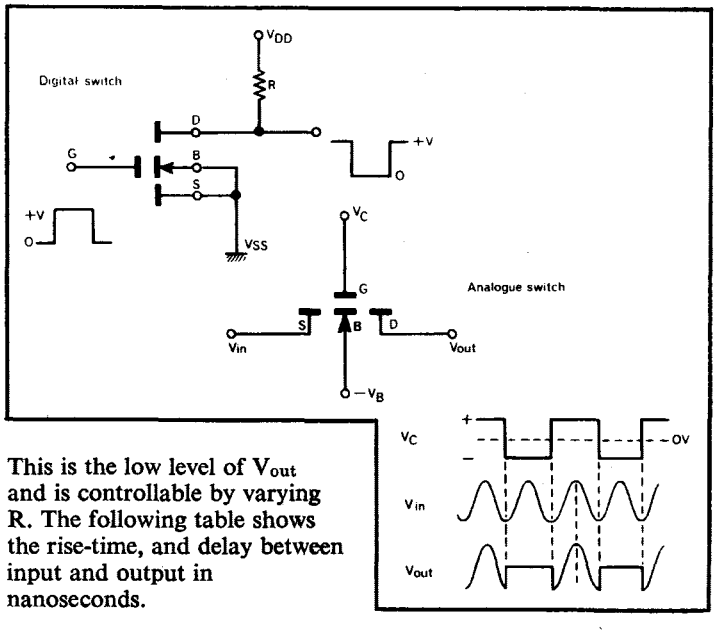
3. D.m.o.s. transistors are double-diffused metal-oxide devices, in which the channel length L of this n-type enhancement type can be controlled very accurately during production. Since R_{on} on-resistance, and input capacitance are proportional to L, while g_m and cut-off frequency are proportional to $1/L$ and $1/L^2$ respectively, then these devices provide better performance than conventional n-type f.e.ts. Digital and analogue switch configuration are shown.

For the digital switch, $(V_{DD} - V_{SS})$ can go up to +30V. With an input signal at V_{in},

$$V_{out}=\left(\frac{R_{on}}{R+R_{on}}\right)V_{DD}$$



This is the low level of V_{out} and is controllable by varying R. The following table shows the rise-time, and delay between input and output in nanoseconds.

V_{DD}	$R(k\Omega)$	t_r	t_d
5	0.68	0.7	0.6
10	0.68	0.8	0.7
15	1.0	1.0	0.9

The threshold voltage at which the transistor turns on is dependent on V_B when source and substrate are not connected as in the analogue switch application, and may have to be accounted for to avoid shift in operating point. The input signal is transmitted through the analogue switch when V_C > (most positive peak of V_{in}) and is disconnected when V_C < (most negative peak of V_{in}).

Reference

Theory and applications of DMOS, *Electronic Industry*, December 1975.

notes

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Set 12: Wideband amplifiers

After considering the suitability of various transistor equivalent circuits, the accompanying article describes the many ways to get extended h.f. performance from transistor circuits. As with valve circuits, there is the well-known limitation to the number of stages that can be cascaded for optimum gain-bandwidth product. To improve on it shunt and series peaking with inductors is the first line of attack, which soon runs into problems of instability and interaction when stages are cascaded. Incidentally, card 2 recalls the dodge, widely used in pulse circuits, of making a parallel RC input network equal in time constant to $R_{in}C_{in}$. A popular method of reducing the effect of Miller (or should we say Blumlein) multiplication of input capacitance is the cascode arrangement (cards 5 & 7), considered as a common-emitter, common-base cascade.

There are other arrangements of two transistors (see also set 20) that can provide good bandwidth; card 12 shows a common-base, common-collector arrangement, related to the d.c. feedback pair of card 9. (For readers who are unclear of the various feedback arrangements around transistor pairs, see Fig. 8, the table and the text on pages 28 and 29.)

Integrated circuits offer good solutions in many situations, useful types being variants of the standard 741, 301 devices, and compensation points to modify h.f. characteristics are provided on i.cs such as the LM318 (card 11). A dodge not to be forgotten is to use digital i.cs in a linearly-biased mode; cards 6 & 8 show how, the e.c.l. circuits offering bandwidths up to a few hundred megahertz.

Wideband amplifiers

Wideband amplifiers are extensively used in instrumentation and communication systems where the signals to be handled may be of an analogue or a digital nature. Such amplifiers are required to provide fairly equal amplification of a large range of frequencies with a lower frequency limit of zero or nearly zero. The high-frequency behaviour of the active devices must be considered in conjunction with the passive network elements to design an amplifier with required characteristics.

Many different circuit models are available for such devices, but not all are necessarily useful. Consider, for example, the bipolar junction transistor models shown in Fig. 1. The three versions of the intrinsic low-frequency equivalent circuit shown in (a), (b) and (c) are highly-idealized models that focus attention on the basic active properties of the device. The low-frequency T and h-parameter models shown in (d) and (e) are more useful, but are unsatisfactory for predicting amplifier performance in the region of its upper cut-off frequency.

Models that are useful for high-frequency design must provide a more realistic representation of the transistor as a network element. The high-frequency model one chooses is often determined by availability of data, personal preferences and experience or whether the parameters of interest are readily determined by measurement. Fig. 2(a) shows the hybrid equivalent circuit which is a reasonable compromise between accuracy and complexity and which may be reduced to simpler forms for low-frequency and high-frequency calculations.

In high-frequency transistors, r_{ce} and $r_{b'c}$ are often sufficiently large to be neglected, the former being much larger than the load impedance and the latter much greater than the reactance of $C_{b'c}$ at high frequencies. The simplified form of Fig. 2(b) is often sufficiently accurate for assessing high-frequency performance and this may be reduced to that shown in Fig. 2(c), where C_{in} consists of $C_{b'e}$ in parallel with the Miller effect equivalent of $C_{b'c}$. The base spreading resistance $r_{bb'}$ and the product $g_m r_{b'e}$ may normally be assumed to be independent of the operating point, g_m increasing and $r_{b'e}$ decreasing as I_E increases. The value of $C_{b'e}$ increases with I_E and the depletion-layer capacitance $C_{b'e}$ varies as $1/(V_{CB})^{\frac{1}{2}}$ to $1/(V_{CB})^{\frac{1}{3}}$.

To obtain a wide bandwidth with the simple cascade of common-emitter stages shown in Fig. 3, the collector coupling re-

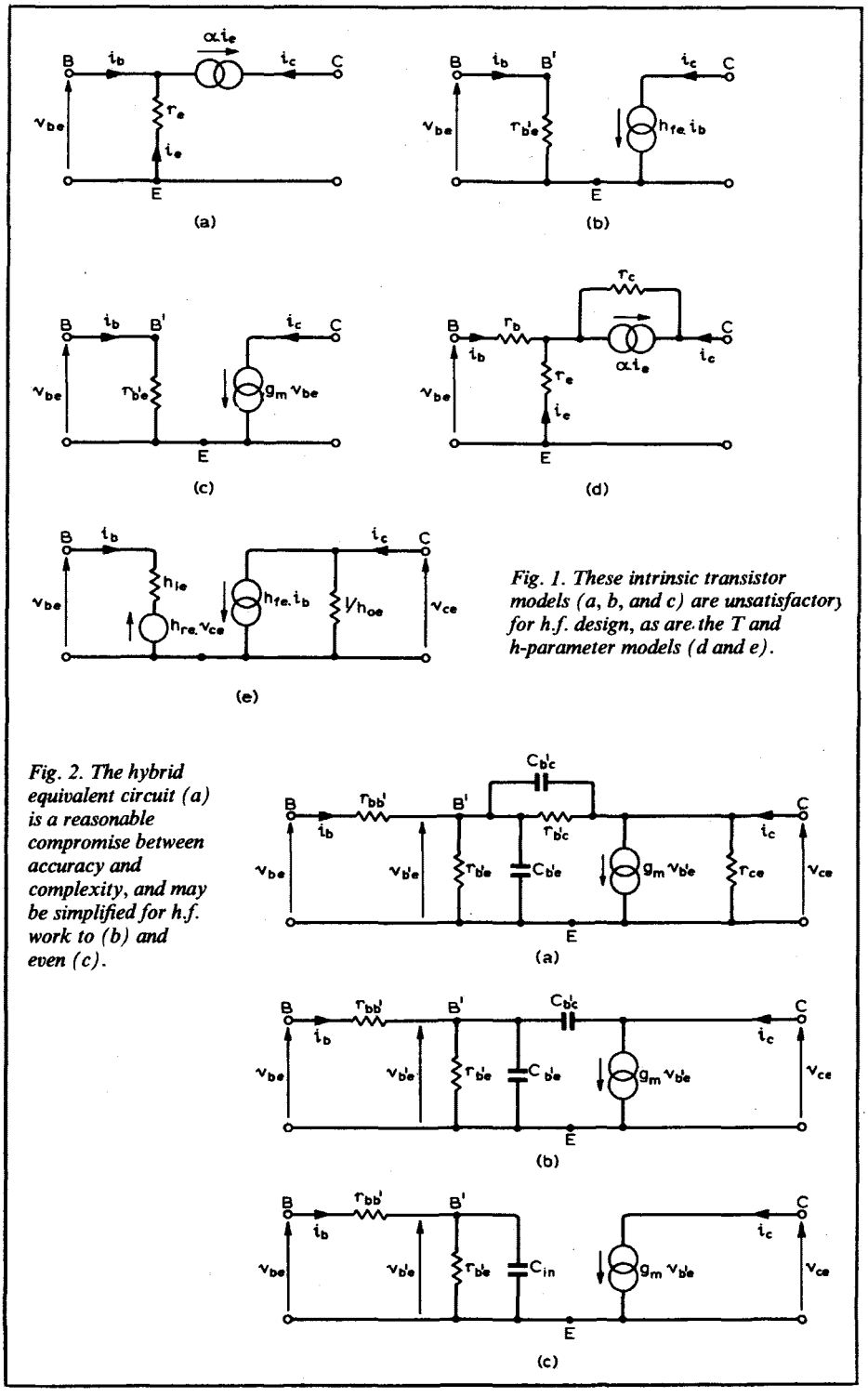


Fig. 1. These intrinsic transistor models (a, b, and c) are unsatisfactory for h.f. design, as are the T and h-parameter models (d and e).

Fig. 2. The hybrid equivalent circuit (a) is a reasonable compromise between accuracy and complexity, and may be simplified for h.f. work to (b) and even (c).

sistors must be made small compared with the input impedance of the following stage, the capacitive component of which causes the gain to fall at high frequencies. Further reduction of R_C to exchange gain for bandwidth is limited by the presence of $R_{bb'}$. Also, if the gain per stage is reduced, more stages must be cascaded to achieve a desired amplifier gain and it becomes increasingly difficult to maintain the overall bandwidth which shrinks as the number of cascaded stages increases. The gain-bandwidth product of the transistors (f_T) attains a maximum value at a particular value of emitter current, which is often small. Adjusting the emitter current of each stage to its optimum value may result in a small signal-handling capability if significant distortion is to be avoided.

Several techniques are available for improving the achievable stage gain-bandwidth product, the simplest of which is the inclusion of an inductor to compensate for the falling response due to transistor input capacitance. The stages in Figs. 4(a) and 4(b) are said to be shunt-peaked and series-peaked respectively, the latter being far less effective in improving gain-bandwidth product. The effect of the shunt-peaking inductor is illustrated in Fig. 5 and by correct design the stage bandwidth, for a given gain, can be improved by a factor of about two without lifting the high-frequency gain above its low-frequency value. Too large a value of L results in overcompensation which produces overshoot and ringing in the transient response. Amplifiers using a number of these stages in cascade may suffer from instability and prove difficult to align.

This problem may be alleviated by making the effective load on each transistor resistive. Referring to Fig. 6, this can be achieved by considering L and R_C to be in parallel with the series equivalent of the CR input network, making R_C equal to the equivalent series input resistance and designing L to produce the same short-circuit time constant for each of the parallel branches. A disadvantage of this constant-resistance cascade is that it is no longer possible to vary a network element to adjust amplifier gain or bandwidth, which must be attempted by variation of the transistor parameters, e.g. by adjusting the individual collector currents. The foregoing techniques have the disadvantage that all the cascaded stages interact, any change in the design of one stage normally requiring changes in the others.

As the input capacitance, including that due to Miller effect, plays an important part in limiting the achievable bandwidth, a design approach that attempts to eliminate the effects of internal feedback is useful. The cascode amplifier shown in Fig. 7 employs this technique and it may be considered as a common-emitter common-base cascade. The common-base stage has a very low input impedance, so the common-emitter stage has a current gain approaching h_{fe} and a very small voltage swing at its collector, resulting in a large reduction of the internal feedback between collector and base. The bandwidth of the common-emitter stage approaches f_β and as that of the common-base stage is much larger, the cascode pro-

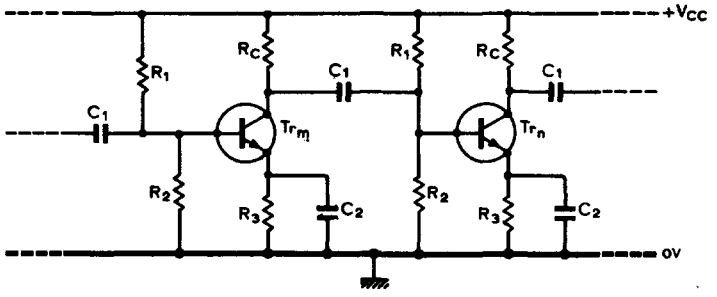


Fig. 3. Reducing R_c and increasing the number of stages can reduce overall bandwidth and give poor signal handling.

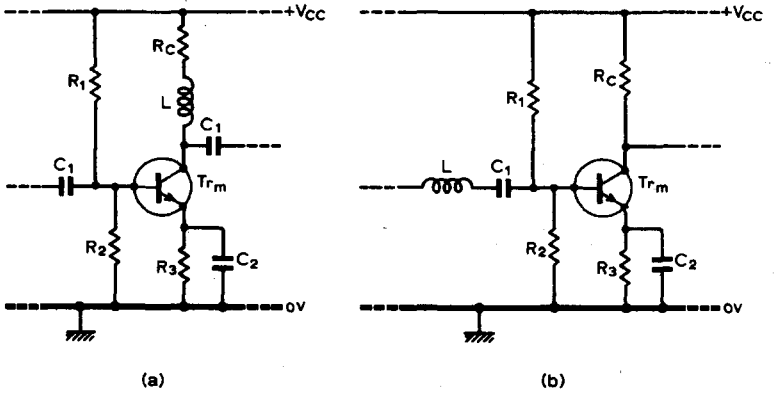


Fig. 4. Simplest way of improving bandwidth is to add shunt (a) or series (b) compensation. Effect of shunt peaking—the most effective—is shown in Fig. 5.

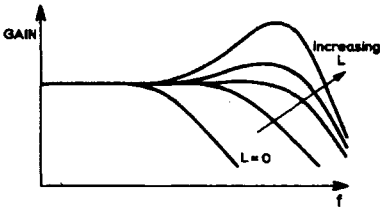


Fig. 5. Too large a value of L in Fig. 4(a) results in overshoot and ringing.

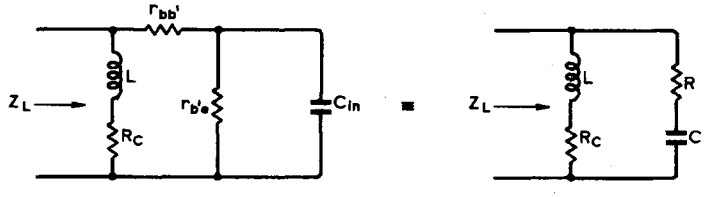


Fig. 6. To avoid instability in cascaded circuits of Fig. 4(a), the transistor load can be made resistive.

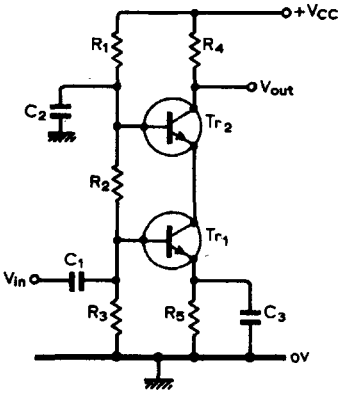


Fig. 7. Cascode circuit minimizes effect of internal feedback.

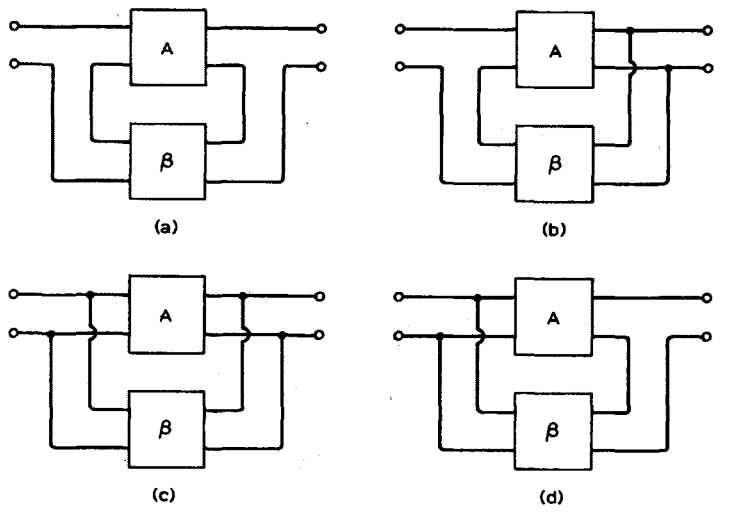


Fig. 8. Four basic ways of increasing bandwidth using negative feedback.

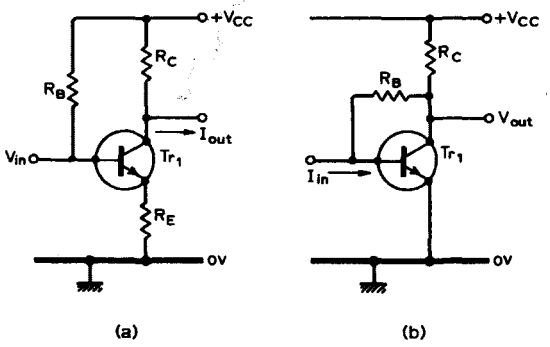


Fig. 9. Series and shunt feedback applied to a single stage.

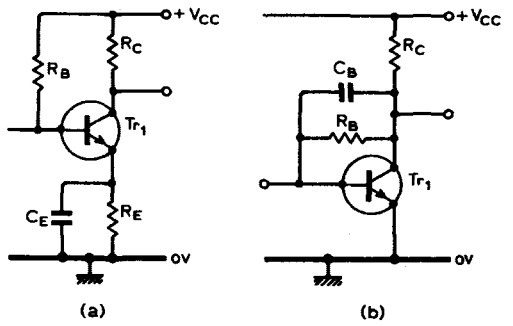


Fig. 10. Peaking capacitors improve h.f. response of Fig. 9.

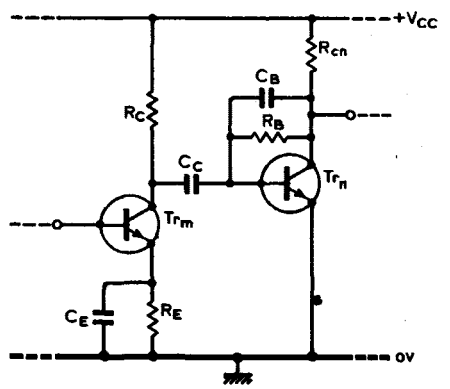


Fig. 11. Deliberate mismatching of impedances can improve stability.

vides the voltage gain and current gain of a common-emitter stage with a wider bandwidth than that obtainable with a simple common-emitter amplifier.

Satisfactory design of wideband amplifiers usually requires the interaction between individual stages or elementary building blocks to be negligible, or definable, the mid-band gain to be stable and input and output impedances to be adjustable to desired values. Use of feedback in the design allows these criteria to be approached without undue concern for the variations in transistor parameters and permits bandwidth to be extended at the expense of gain in a controllable manner. While the reduction in gain is a disadvantage it is not an expensive price to pay, bearing in mind the benefits obtained and the relatively low cost of adding extra feedback stages to meet the overall gain requirement.

Another disadvantage of feedback is the increased possibility of oscillation, which may be avoidable at the design stage by using a sufficiently accurate circuit model. In a multi-stage amplifier designed for the highest possible bandwidth before the application of feedback, the cut-off frequencies of all stages will normally be similar. Hence there is a near certainty that the combined phase shift can reach 180° while the magnitude of the gain is well in excess of unity. To remove this possibility, by deliberately setting one of the cut-off frequencies much lower than the others, negates the original requirement for maximum pre-feedback bandwidth. General-purpose operational amplifiers, such as the 741-type, have internal stages with high cut-off frequencies, but a dominant lag at about 10Hz has to be introduced to cope with the possibility of 100% feedback.

Four basic feedback configurations may be used to create elementary building blocks. Fig. 8 shows these configurations which may be described in terms of the method in which the feedback is derived and applied. Thus, (a) is series-derived series-applied, (b) is shunt-derived series-applied, (c) is shunt-derived shunt-applied and (d) is series-derived shunt-applied. Alternative descriptions of these configurations are in common usage e.g. (a) transimpedance feedback, series-series or simply series, (b) voltage-ratio feedback or series-shunt, (c) transadmittance feedback, shunt-shunt or simply shunt, and (d) current-ratio feedback or shunt-series. Other descriptions include the use of the terms current feedback or voltage feedback. In the former case the signal fed back is proportional to the output current but may itself be a current or a voltage. With voltage feedback the fed-back signal is proportional to the output voltage. All four arrangements have the property of increased bandwidth and reduced gain compared with the open-loop values. The input and output impedances become modified as shown in the table, shunt derivation (application) reducing the output (input) impedance and series derivation (application) increasing the output (input) impedance.

The two types of single-stage feedback, series and shunt, are shown in Fig. 9. In Fig. 9(a) the load impedance should be low and the input supplied from a voltage source

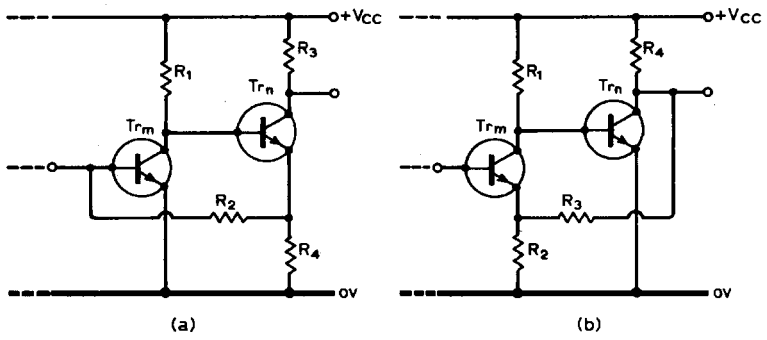


Fig. 12. Widely differing input and output impedances make two-stage feedback circuits useful for cascading.

whereas in Fig. 9(b) the load impedance should be high and the amplifier input should be from a current source. The high-frequency response of these elementary blocks may be improved by the addition of peaking capacitors as shown in Fig. 10.

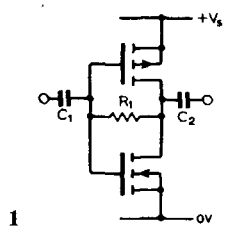
Source and load impedance requirements for stable gain with single-stage feedback can be met by purposely creating a large mismatch between cascaded stages, i.e. by alternating series and shunt feedback stages as shown in Fig. 11. With this arrangement gain-bandwidth product is high, low-frequency gain may be determined with reasonable accuracy by multiplication of individual stage gains, and there is little interaction between stages. Feedback applied to two stages can offer similar merits, Figs. 12(a) and 12(b) showing series-derived shunt-applied and shunt-derived series-applied configurations respectively. Both networks have widely differing input and output impedances and are therefore attractive as basic building blocks for cascaded stages.

Although discrete devices may be used in a multistage realization, the availability of integrated-circuit transistor arrays, containing about five transistors with parameters inherently reasonably matched, are very attractive for many designs. Integrated circuits are available in the form of a long-tailed pair which can be operated as single-ended or differential-input wideband amplifiers by the addition of external passive components that allow a high degree of flexibility in the selection of gain, bandwidth and signal-handling capability.

Other integrated circuit versions provide emitter-follower input and output transistors to make the input and output impedances high and low respectively. Integrated wideband power amplifiers can be obtained providing bandwidths up to about 8MHz and outputs of about 14V pk-pk. Integrated circuits containing pairs of cascode amplifiers and some with gating facilities are also very useful as wideband amplifiers. Modern integrated-circuit logic gates designed for high-speed switching applications may also be usefully employed as low-cost wideband amplifiers by setting the quiescent conditions in a linear part of the transfer characteristic and employing feedback to define the gain.

Feedback type	Z_{out}	Z_{in}
Fig. 8(a)	increases	increases
Fig. 8(b)	decreases	increases
Fig. 8(c)	decreases	decreases
Fig. 8(d)	increases	decreases

High input impedance c.m.o.s. amplifier



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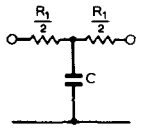

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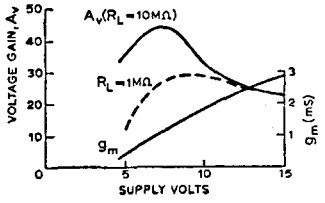

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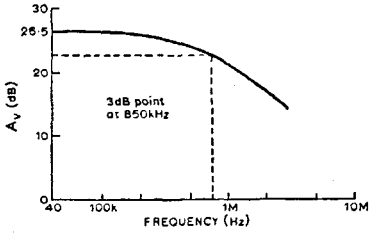


4

Circuit description

C.m.o.s. circuits have been designed for digital systems. Basic building block is the inverter consisting of a complementary pair of enhancement-mode m.o.s. devices with threshold voltages in the region of 1.7V and peak current capabilities of a few tens of milliamperes at maximum forward bias. Input resistance is extremely large with the leakage currents of the protection diodes as the limiting action. The individual device g_m is around 1 to 2mS for forward gate-source voltages in excess of 5V. Biased in the linear mode, the devices each have $|V_{gs}| \approx V_s/2$, so maximum forward bias is $\approx$7.5V for the rated supply voltage of 15V. This restricts the upper value of g_m that can be attained. In the absence of an external load resistance the voltage gain is limited by the finite slope resistance. An unusual property of this circuit is that the voltage gain falls with increasing supply voltage, as the relatively small rise in g_m is more than offset by the fall in output slope resistance at the higher resulting currents.

The disadvantage of operating at low supply voltages (and hence currents) is that the voltage gain is more load-dependent and the upper cut-off frequency falls sharply. To maximize the input resistance while using d.c. negative feedback to stabilize the operating point, the feedback resistor is decoupled (see Fig. 2). Gate current is negligible and the input and output quiescent voltages are equal.

Other c.m.o.s. devices using different fabrications, e.g. silicon gate, ion implantation, offer greater bandwidths and/or lower threshold voltages. Complementary m.o.s. circuits designed for the linear market have been recently announced.

Component changes

IC_1: Any c.m.o.s. inverter including CD4001 NOR gate, CD4009/CD4049 inverting buffers, MC1407, MC14009 and other equivalents.

R_1: 220k to 22MΩ.

C: Sets the lower frequency at which the negative feedback becomes operative, reducing the input impedances. 0.1 to 10μF (time constant $R_1C/2$).

C_2: Depends on load which, with this circuit, cannot be very low unless transconductance properties alone required with little voltage gain. 0.1 to 100μF.

V_s: 3 to 15V. At voltages below 5V the quiescent current becomes very small and output impedance is very high.

Circuit modifications

● Negative feedback may be applied over any odd number of inverting stages, e.g. over three as in the circuit shown left. Multiple phase shifts within the amplifier, together with the high voltage gain available, make the method difficult to apply without precautions. Open-loop gains of 80dB and greater may occur. Even decoupling the feedback still allows oscillation at low frequencies via the coupling/decoupling/supply time-constants.

● A better method of controlling gain than simply attenuating it is to cascade stages with shunt and series negative feedback as shown centre where inserting a resistor in the source of each device in stage 1 reduces and defines the transconductance. Shunt feedback across stage 2 defines its transresistance and the combination has a lower but well-defined voltage gain.

● Because the above amplifier is non-inverting, d.c. feedback may be applied via the third stage used purely as a d.c. coupling element linking A-A′, B-B′, with the overall a.c. feedback decoupled.

Further reading

RCA, COS/MOS Digital Integrated Circuits, 1973, pp. 24–30, pp. 37–42, p. 346, p. 355.

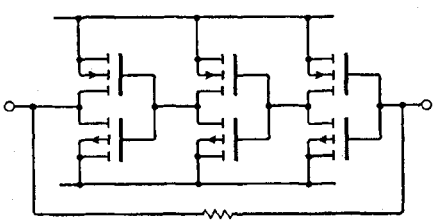
Wujek, J. H. Field-effect transistor circuits, in Electronic Circuits Manual by J. Markus, McGraw-Hill 1971, p. 22.

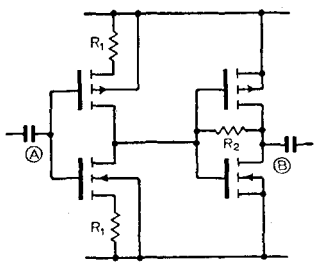
Ferranti Ltd., FET Source Follower and Bootstrapped FET Source Follower, FETs and Applications, no. 22, 1965.

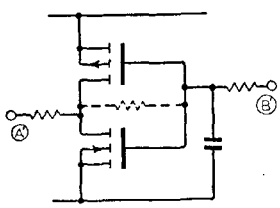
Cross references

Set 12, cards 4 & 7.
Set 11, cards 5 & 6.

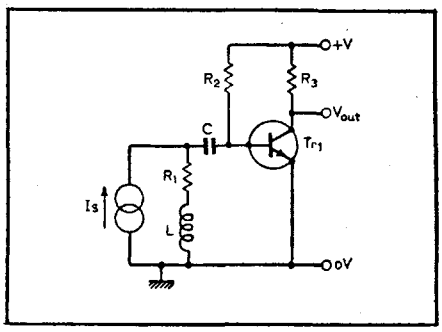
Circuit modifications



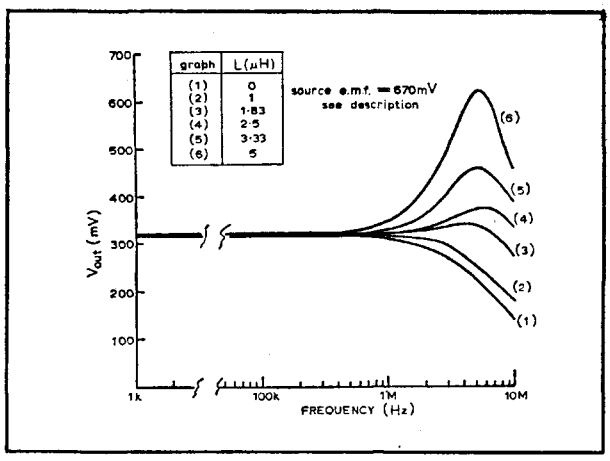




Shunt-peaked wideband amplifier



Circuit data/
Supply: +6V, 4.5mA
Tr_1: 1/5×CA3046
C: 10μF tantalum
R_1: 68Ω; R_2: 100kΩ
R_3: 680Ω
L: 1.83μH (38 turns 28 swg, close wound on 0.2in dia.)



Circuit description
Bandwidth of a common-emitter amplifier may be extended by including an inductor in shunt with its input producing a shunt-peaked amplifier. The circuit is fed from a current source, or alternatively in a cascaded amplifier R_1 and L may be used as the collector coupling network of each stage which is loaded by the input impedance of the following transistor.
Because the gain-bandwidth product of a transistor varies with its collector current, R_2 was chosen to maximize the gain-bandwidth product for the device used. Resistor R_3 was chosen to make $V_{CE} \approx +V/2$ and R_1 to provide the desired low-frequency current gain. Source resistance was 100Ω, so a current source was simulated by a chain of ten 1-kΩ resistors in series to reduce the effect of the shunt capacitance of a single 10-kΩ resistor on the measured high-frequency response.
With $L=0$, amplifier input voltage falls with increasing frequency due to transistor input (and Miller effect) capacitance. With L in circuit, low-frequency response is the same but a low-Q resonance occurs between L and C_{in} of the transistor, causing the response to peak as the frequency is raised towards its original cut-off value.
By designing L on the basis of available transistor parameter data and the required current gain, it is possible to produce a maximally-flat gain response while maximizing stage gain-bandwidth product.
Alternatively, a good starting point is to use the measured low frequency input resistance and upper cut-off frequency with $L=0$ to estimate C_{in} and then design L to resonate with this value in the region of the desired cut-off frequency with the peaked response. (See curve 3 above.)

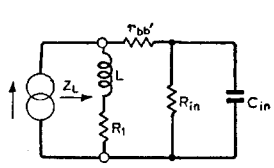
Component changes
Useful range of supply +3 to +30V. Values of R_2 and R_3 should be adjusted to produce f_T max. for transistor if maximum stage gain-bandwidth product is to be achieved. Select R_1 to give desired low-frequency gain, and C to give desired lower cut-off frequency. High-frequency response may be tailored to suit requirements by choice of L value. (See curves 2, 4, 5 & 6.)

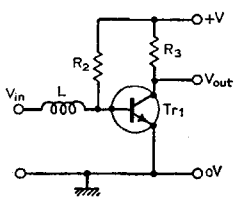
Circuit modifications
● Up to five cascaded stages may be obtained with the same integrated circuit package but it may prove easier to obtain the desired response experimentally than by calculated design. Problems of alignment and possible instability due to inter-action between cascaded shunt-peaked stages can be alleviated if each transistor feeds a resistive load. The load on each device consists of L and R_1 in parallel with the input impedance of the following stage, as shown left. Load impedance may be made purely resistive by adjusting the values of R_1 and L to be $r_{bb'}(r_{bb'}+R_{in})/R_{in}$ and $C_{in}r_{bb'}$ respectively, where $r_{bb'}$ the transistor base spreading resistance. In such a constant-resistance cascade, L and R_1 cannot be used to adjust the gain and bandwidth of the amplifier which must be trimmed by adjusting the collector currents of the transistors.
● A series-peaking inductor may be connected between a low-impedance source and the base, as shown centre, to extend the bandwidth. Stage gain-bandwidth product is less than for the shunt-peaked arrangement and its maximum value cannot be achieved with a maximally flat response.
● Another high-frequency compensation network, widely used in pulse applications, is shown right. Bandwidth may be extended by making $R_1C_1 = R_{in}C_{in}$ but the stage gain-bandwidth product, while constant, does not approach that of the shunt-peaked stage. However the constancy of the gain-bandwidth product does allow exchange of gain for bandwidth by adjusting R_1.

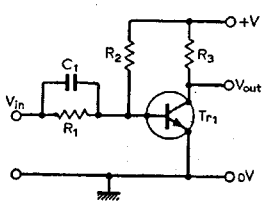
Further reading
Ghausi, M. S. Electronic Circuits, Van Nostrand, 1971, chapter 4.
Shea, R. F. (Ed.), Amplifier Handbook, McGraw-Hill 1966, section 25.4.2.
Joyce, M. V. & Clarke, K. K. Transistor Circuit Analysis, Addison-Wesley, 1963, chapter 8.
Markus, J. Electronic Circuits Manual, McGraw-Hill, 1971, p. 913.

Cross references
Set 12, cards 5, 9 & 12.
Set 7, card 9

Circuit modifications







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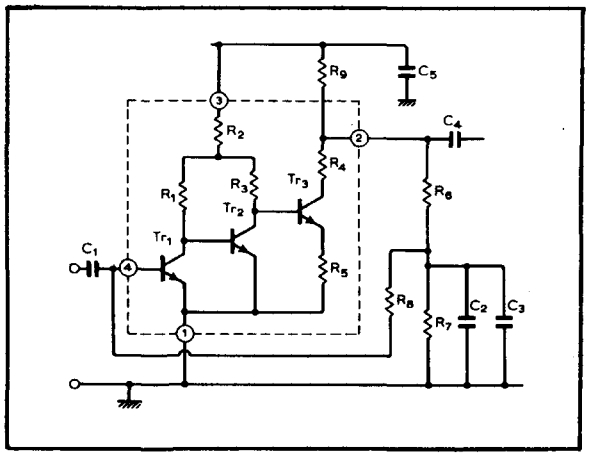
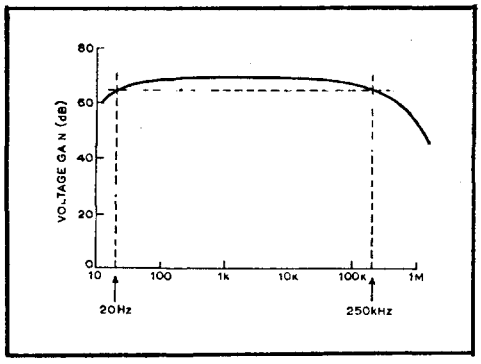
High-gain wideband amplifier



Typical performance

R_6	33kΩ	R_7	15kΩ
R_8	2.2kΩ	R_9	10kΩ
C_1	20μF	C_3	10nF
C_3	64μF	C_4	10μF
C_5	100nF		

IC MFC4010A
V_S +6V
f 100Hz to 50kHz
Voltage gain > 3000 (70dB)
Cut-off 250kHz
Input resistance 700Ω
Output resistance 8.5kΩ



Circuit description

This amplifier uses an integrated circuit developed for consumer applications. It is simple in design, consisting of three common-emitter transistors directly coupled so that the collector potentials of Tr_1, Tr_2 are defined by the base potentials of Tr_2, Tr_3 respectively, i.e. they are at ≈0.6V. Resistor R_5 has a low value with only a marginal effect on these potentials.

Output potential is forced by the feedback effect via R_6, R_7, R_8 to be some defined multiple of the base potential of Tr_1. If $R_8 < R_6$, R_7 then the output p.d. to ground is $\approx(R_6/R_7+1)$ V_{be1} and would typically be set near the supply mid-value.

Current in each stage increases with increasing supply voltage, and as a result both open-loop gain and bandwidth increase. Increased current also reduces the input impedance. Resistor R_9 determines quiescent output current provided output voltage has been fixed by feedback as outlined above. As there are three stages all contributing phase shift, the total phase shift is in excess of 180° before the magnitude of the gain falls towards unity. Hence it is difficult to apply heavy negative feedback to extend the bandwidth at the expense of gain as can be done with amplifiers using common-emitter stages. (For audio frequency applications it is possible to control the feedback to produce defined characteristics as for tape recording/playback amplifiers.) As the high gain extends to high frequencies, $A_v \approx 100$ at $f=4$MHz, proper grounding, decoupling and use of short leads, screened where appropriate are all important.

Component changes

IC: No direct replacements but groups of three transistors from CA3046 and similar multi-transistor packages may be used.

R_6, R_7: Ratio fixes output quiescent voltage $\approx(R_6/R_7+1)$ 0.6V. Resistors may be increased to minimize loading on output, but base current of Tr_1 becomes significant factor in determining quiescent conditions. Typical range 5k to 50kΩ.

R_8: Also limited by base current effects, but may be increased up to 10kΩ to maximize input resistance of circuit if required.

R_9: Determines output stage quiescent current and hence maximum load current. No advantage to making too high since current in preceding stages fixed by internal resistors. 2.2k to 22kΩ.

$+V_S$: 2 to 18V. At low voltages, gain falls sharply Choose R_6, R_7 in conjunction with V_S to bias output near mid-point of supply for maximum output swing.

C_1, C_3, C_4: Determine low frequency cut off. Maintain ratio increasing values for pro rata fall in cut-off. C_4 may be reduced greatly if feeding high impedance load.

Circuit modifications

● Any group of three transistors may be used in similar configurations. Simple arrangement (left) for low-voltage applications where output quiescent voltage of 0.6V would be adequate. Again decoupling of feedback essential since gain/phase properties too complex for application of heavy negative feedback. Resistors R_1 to R_5 may be comparable value resistors (1k to 10kΩ) though R_4, R_5 may be higher if somewhat higher output direct voltage desired.

● By using complementary transistors, each transistor has current defined by V_{be} of succeeding stage. This makes current and gain/bandwidth less dependent on supply voltage (middle). Complementary versions of each form are equally possible, reversing the supply voltage.

● The good high frequency gain allows its use in 10.7MHz i.f. applications (right) with the d.c. feedback applied via the input tuned circuit and the output taken to a ceramic filter. Similar principles apply at 470kHz but the high voltage gain makes careful design obligatory. In all r.f. applications drive from a 50Ω source is normal, but the output impedance of the circuit is relatively high.

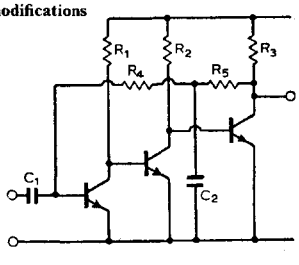
Further reading

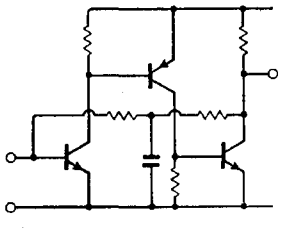
Motorola Linear Integrated Circuits Data Book, 2nd edition 1972, pp. 7–561 to 7–564.
CA3095E Wideband Amplifier, RCA Databook SSD-201A, 1973, p. 249.

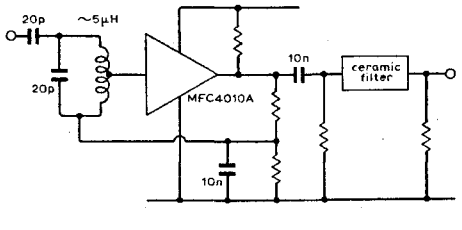
Cross references

Set 12, cards 5, 10 & 11.

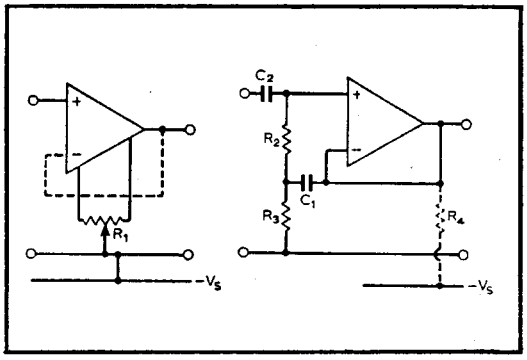
Circuit modifications







Wideband voltage followers



Circuit data
IC: LM310
R_1: 1kΩ
R_2, R_3: 100kΩ
R_4: 3.3kΩ
C_1: 2.2μF
C_2: 0.01μF
Supply: ±15V

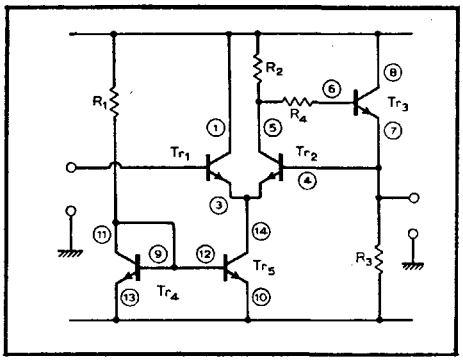
Circuit description
A specially-designed monolithic voltage-follower, the 310 has a combination of highly desirable parameters: high input impedance, low output impedance, and wide frequency range. The negative feedback is connected internally but some modifications to performance that can be made externally include offset zero by means of R_1, increased output current capability by preloading with R_4 at the expense of increased dissipation, and a.c. coupling to source, bootstrapping the bias resistors R_2, R_3 to minimize loading effects.
Slew-rate limitations imposed by the maximum charging rate of an internal compensation capacitor, mean that the large signal bandwidth is much less than small signal bandwidth—true of amplifiers having heavy negative feedback in general.

Performance
Upper cut-off frequency for small signals.
15MHz for zero source resistance, 2MHz for 10kΩ. At 1MHz, output impedance is 25Ω, output voltage swing is ±3V, and input impedance is 3pF plus strays.

Component changes
IC: Direct replacements from many manufacturers. Any op-amp compensated for 100% negative feedback may be used. In general it will not be possible to achieve the same spread of parameters, i.e., high input impedance may preclude wide bandwidth.
R_2, R_3: Increase for higher Z_{in} at expense of increased offset.
C_2, C_1: Determine lower cut-off frequency (with R_1, R_3). Combination gives inductive term to input impedance at low frequencies. 0.1 to 10μF.
R_4: Increases negative current capability at expense of dissipation.
V: ±5 to ±15V (down to ±3V in extreme cases).

Further reading
LM110—An Improved IC Voltage Follower, National Semi-conductor Linear Applications Handbook, 1972, p. LB11-1 and 2.
Campbell, T. C. Application note ICAN-5213, in RCA Databook SSD-202, 1972, pp. 203–4.
Markus, J. Electronic Circuits Manual, McGraw-Hill, p. 13.

Cross references
Set 12, cards 1 & 11.
Set 7, card 3.



Circuit data
Tr_{1-5}: CA3046
R_2: 3.9kΩ
R_1: 4.7kΩ
R_3: 1kΩ
R_4: 1kΩ
Supply: ±2.5V

Circuit description
Using the five transistors in an i.c. package (CA3046), this is a simple wide-band voltage follower. A similar circuit could be used with discrete transistors replacing current mirror Tr_4, Tr_5 by a similar current source or by a single resistor particularly if the supply voltages were higher. Transistors Tr_1, Tr_2 are the differential pair comparing input with output, the use of a monolithtic pair giving good temperature drift. Transistor Tr_3 is an emitter follower within the feedback loop. Resistor R_4 may be required to suppress very high frequency oscillations (dependent on circuit layout). Not shown, but generally important, is the decoupling of the supply voltages as close to the i.c. as possible—typically 0.01 to 1μF.

Performance
Upper cut-off frequency ≈4.5MHz.
Output impedance ≈10Ω.
Input impedance: ≈100kΩ.
Output voltage swing ≈2.5V pk-pk at 100kHz.

Circuit modifications
- Replace Tr_4, Tr_5 by any other constant current source (or even resistor, with reduced stability against supply changes).
- Increase open-loop gain output capability, by replacing R_2, R_3 with constant current sources.
- Replace Tr_3 by common emitter p-n-p transistor taking signal from Tr_1 collector instead. Higher open-loop gain, greater output swing capability, greater likelihood of oscillations requiring compensating capacitor, e.g., collector-base of Tr_3.

Component changes
IC: CA3046, CA3045, CA3086.
R_1: 1kΩ to 100kΩ. Lower values increase bandwidth and dissipation.
R_2: Set to carry half current in R_1 (assuming unity ratio for current mirror). Typically $R_1 \approx R_2$.
R_3: Low values maximize output swing and dissipation 330Ω to 33kΩ.
V: ±2 to ±7½V. Higher voltages possible if discrete transistors used.

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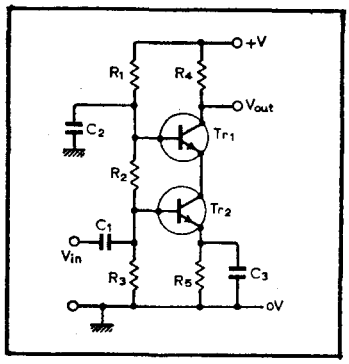
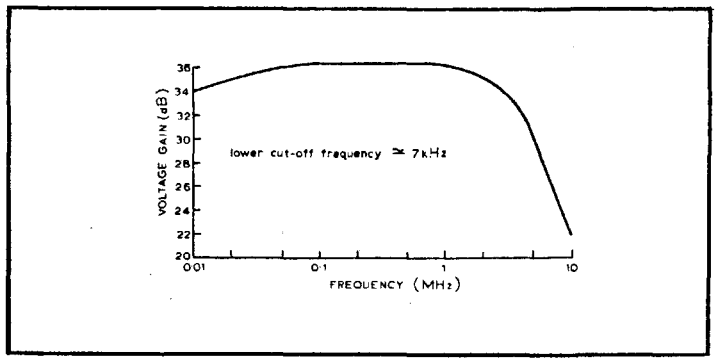
Series 12: Wideband amplifiers—5

Bipolar cascode wideband amplifier



Circuit data
Supply: +6V, 1.2mA
Tr_1, Tr_2: 1/5×CA3046
R_1: 39kΩ; R_2: 3.3kΩ
R_3: 33kΩ; R_4: 2.2kΩ
R_5: 1kΩ
C_1, C_2, C_3: 1μF
V_{in}: 10mV r.m.s.



Circuit description
The bipolar transistor cascode amplifier offers very good isolation between its input and output ports, so that the possibility of instability is virtually non-existent for all types of load. Input transistor Tr_2 acts as a common-emitter stage which is loaded by the upper transistor connected in the common-base configuration and having a very low input impedance. Thus the common-emitter stage has a current gain approaching h_{fe} and the voltage swing at its collector is very small, producing a significant reduction of the internal feedback between collector and base. Bandwidth of the common-emitter stage approaches f_β and as that of the common-base stage is much larger, the complete circuit behaves like a common-emitter amplifier as far as voltage gain and current gain are concerned, but has a wider bandwidth than is achievable with a simple common-emitter stage providing the same high voltage gain.
A reasonable estimate of the 3-dB bandwidth obtainable with the cascode amplifier may be made using available data and the relationship: gain-bandwidth product $(f_T) \approx h_{fe} \cdot f_\beta$ if it is assumed that h_{fe} and f_β are the approximate current gain and bandwidth values for the whole circuit. Each of the transistors in the integrated circuit array has typical h_{fe} and f_T values of 110 and 450MHz respectively, with $I_C \approx 1.2$mA giving $f_\beta \approx$ 4.1MHz. (Measured upper 3dB cut-off frequency was approximately 3.7MHz for the circuit.)

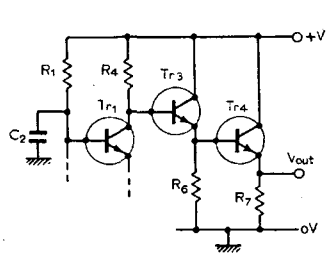
Component changes
Useful range of supply +2 to +30V.
V_{in}(max) ≈ 40mV(pk-pk).
Midband gain falls by 3dB when output is loaded with approximately 6.8kΩ (capacitively coupled).
Upper cut-off frequency largely determined by R_4 for given transistors.
Lower cut-off frequency adjustable by changing C_1, C_2 and C_3. Tr_1 and Tr_2 may each be replaced by ¼×CA3018 or equivalent discrete devices e.g. 2N706-type.

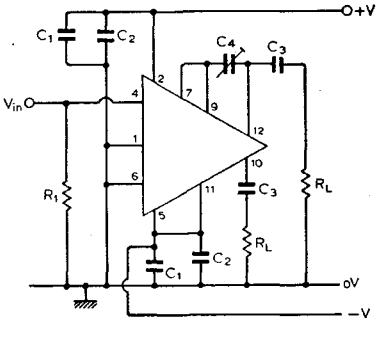
Circuit modifications
●One of the differentially-connected pair of transistors in the CA3046 package may be connected as an output emitter-follower stage to provide a low output impedance cascode amplifier. If a CA3018 package is used, all four transistors may be used by following the cascode with a pair of cascaded emitter followers as shown left. In this form, with R_6=3.3kΩ and R_7=2.7kΩ a voltage gain of about 36dB is obtainable with an upper cut-off frequency of approximately 11MHz.
●A pair of cascode stages with a common tail resistor may be used as a differential cascode amplifier. This arrangement is the basis of the CA3040 integrated circuit wideband amplifier, which employs high-input-impedance emitter-follower buffer stages between the input terminals and the common-emitter sections of the cascodes. Outputs from the cascode common-base stages are fed to the output terminals via emitter followers to produce a reasonably low output impedance.
●Centre circuit shows the CA3040 connected to a pair of equal load resistors (R_L) which receive antiphase outputs. With the amplifier connected to a 50-Ω source and R_L=50Ω the voltage gain to each output is about 22dB with a bandwidth of approximately 30MHz. The values increase to about 32dB and 50MHz respectively when R_L is raised to 1kΩ and the bandwidth may be increased to about 90MHz by including the input series peaking circuit shown right. Supplies must be decoupled with capacitors C_1 and C_2 at the integrated-circuit package pins and ferrite beads on the supply leads and careful printed circuit layout are necessary. Supply ±6V, R_1 50Ω, C_1, C_3 100nF, C_2 1nF, C_4 is a small trimmer to adjust high-frequency gain and phase balance.

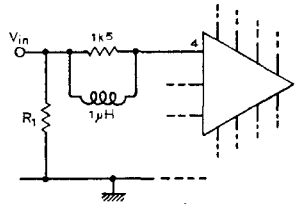
Further reading
Theriault, G. E. et al. Application of the RCA-CA3018 Integrated-Circuit Transistor Array, RCA Databook SSD-202 1972, pp. 68–70.
Austin, W. M. Principal Features and Applications of the RCA-CA3040 Intregrated-Circuit Wideband Amplifier, RCA Databook SSD-202, 1972, pp. 171–81.

Cross references
Set 12, cards 2, 3, 7 & 12.
Set 7, card 5.

Circuit modifications

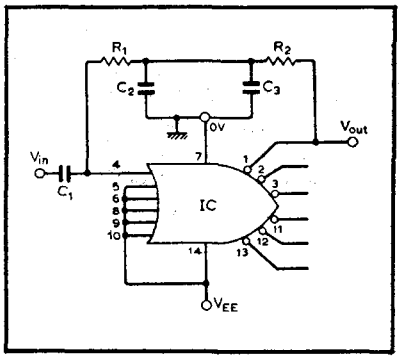






wireless world circard

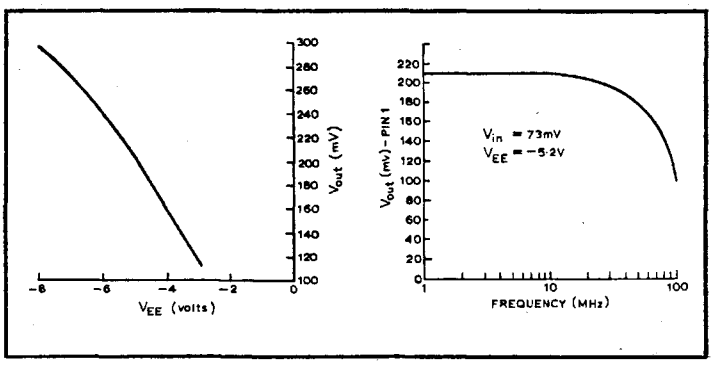
Wideband amplifier using e.c.l.



Typical performance

V_{EE}	−5.2V, 20mA
R_1, R_2	390Ω
C_1	100nF, C_2 100pF
C_3	1μF tantalum
IC	MC1001

Voltage gain (l.f.) 2.89
V_{in} 73mV r.m.s.



Circuit description

The integrated circuit is an emitter-coupled logic gate designed for high-speed digital applications. This type of gate has an input stage consisting of a long-tailed pair with multiple inputs to one half of the pair via separate transistors having their collector-emitter paths in parallel. Each half of this differential stage feeds an emitter follower output stage, a number of which may be paralleled within the package. Thus, at least one inverted and at least one non-inverted output is available and the logic gate may be used as a linear, wide-band amplifier provided it is correctly biased, for example by means of R_1 and R_2 as shown above. This simple arrangement of connecting one of the logical NOR outputs back to the input provides self-biasing of the gate that ensures that the d.c. input and output voltages are the same except for the small drop across R_1 and R_2. This is only possible if the gate is operating in the middle of its transfer characteristic, the arrangement automatically compensating for changes in bias and offset voltages.

Only the d.c. component of the output signal is fed back to the input, C_2 and C_3 decoupling the a.c. component. Capacitor C_1 prevents any d.c. component of the input signal from disturbing the self-biasing conditions. The a.c. signal voltage available at the NOR output used to derive the feedback, is typically 3 to 4% lower than that obtainable from other NOR outputs, and is approximately 9 to 10% higher than at the unloaded NOR outputs.

Careful printed circuit layout is required if a smooth, high-frequency roll-off is to be obtained in the frequency response.

Component changes

Useful range of $V_{EE} \approx -3$ to -8V (see graph).

Minimum load resistance for 10% fall in mid-band gain ≈ 270Ω (a.c. coupled via 100nF capacitor).

Distortion is less than 1% for V_{in} in the range approximately 1 to 20mV and useful V_{in} (max) without significant distortion is approximately 200mV pk-pk.

For bandwidths in excess of 300MHz use MC1660.

Circuit modifications

- More than one input of the gate may be used to increase gain by connecting others in parallel, but the offset voltage between output and input rises as the number of paralleled inputs increases. This may not be a severe disadvantage in certain applications.
- The simple self-biasing arrangement may be applied over several e.c.l.-gate amplifying stages, as shown left.
- A given total bias network resistance (R_1+R_2) may be decoupled asymmetrically. For example, if it is required that the bias-network loading of the output be reduced without changing (R_1+R_2), values such as those shown centre may be used. This will cause the input impedance of the amplifier to fall from about 390Ω to about 220Ω.
- The biasing arrangement may be changed to allow an increase in both the input and output impedances without changing the d.c. input and output voltages. One such arrangement is shown right, where the junction of R_1 and R_2 may be returned to the 0-volt rail through a suitable-value, additional bias resistor R_3. For example, with R_1, R_2 2.2kΩ, a suitable value for R_3 would be around 47kΩ. This arrangement slightly increases voltage gain.

Further reading

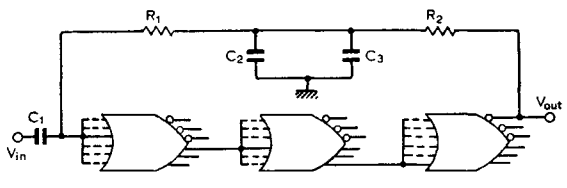
Using e.c.l. gates as wideband amplifiers, *Electronic Engineering*, June 1973.

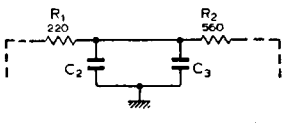
MECL Integrated Circuits Data Book, Motorola, 2nd edition, 1972, pp. 5–3 to 5–6 and pp. 4–17 to 4–20.

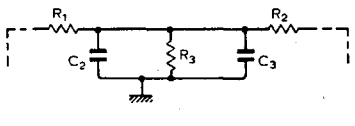
Cross references

Set 11, card 7.
Set 12, cards 8 & 10.

Circuit modifications







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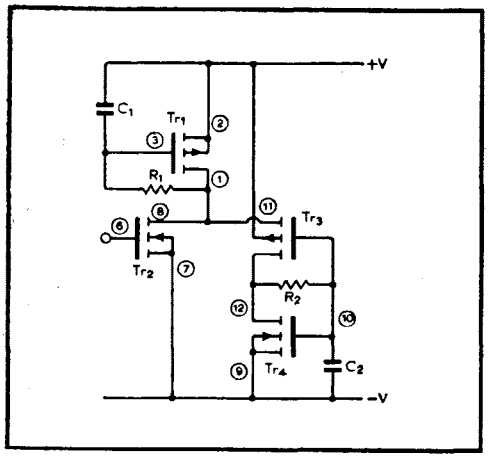
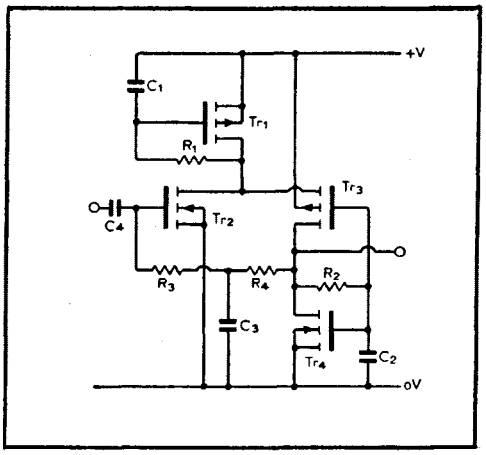
FET cascode amplifiers



Circuit data
Supply: ±7.5V
IC: CD4007AE
R_1, R_2: 1MΩ
C_1: 0.1μF; C_2: 0.33μF
Voltage gain: ≈26(R_L 33kΩ)
Cut-off frequency: 320kHz
Alternative bias for single supply: R_3, R_4: 1MΩ
C_3: 1μF; C_4: 0.01μF



Circuit description
The basic principle of a cascode stage is that of a common-emitter or common-source amplifier feeding directly into a common-base or common-gate stage, so that the first stage feeds into a near short-circuit. This allows it to develop its maximum current gain or transconductance, but more important the voltage swing at the collector or drain is small. Large voltage swings produce relatively large currents in the inevitable feedback capacitance, with a corresponding heavy shunting effect at high frequencies. This reduction in feedback (commonly called the Miller effect though first discussed by Blumlein) is of particular importance in wideband and r.f. amplifiers. In particular, the better the isolation between input and output the higher the gain that can be achieved consistent with stability. The devices need not be in series for d.c. purposes though this is more common.
In the circuit shown, based on a low-cost c.m.o.s. i.c., Tr_2 is a common-source stage whose output signal current is diverted into Tr_3 provided that Tr_1 has a high dynamic impedance at a.c. (see circuit modifications). The voltage gain of the cascode pair is equal to or greater than the highest voltage gain obtainable from a single stage, while coupling between output and input is minimized.
An alternative version is shown in which a decoupled d.c. feedback path via R_3, R_4 gives self-biasing (with a.c.-coupled source). The high input resistance of the m.o.s. devices together with the possibility of operation at $V_{dg}=0$ allows for simple biasing networks and offsets the disadvantage of the wider tolerance on m.o.s. devices as against bipolar transistors.

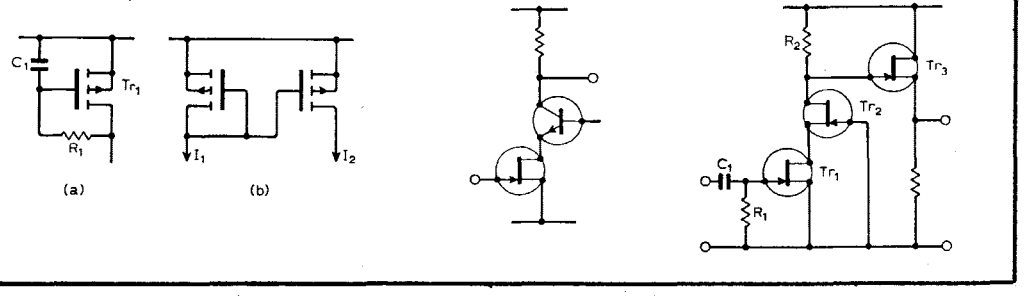
Component changes
IC: Equivalents of CD4007AE including MC14007, etc.
Other combinations of enhancement-mode m.o.s.f.e.ts may function but simpler circuits can be devised for these. This circuit was intended to make best use of this low-cost i.c.
Supply voltage: Positive voltage may need to be increased with some devices; negative rail is then reduced accordingly to stay within rating.
R_1, R_2, R_3, R_4: Not critical. 100kΩ to 22MΩ. With low resistances, low-frequency time constants are raised unless large capacitances used, while input impedance falls for second version. Very high resistances bring noise/hum/leakage problems.
C_1, C_2, C_3, C_4: High values to improve low-frequency response if required.

Circuit modifications
● The high impedance of the circuit is possible because the p-channel enhancement-mode m.o.s.f.e.t. can still have the drain well beyond the knee of its characteristics if biased with drain and gate at equal quiescent potentials. Provided the a.c. applied to the drain is adequately decoupled by R_1C_1, the dynamic impedance approaches that of the drain-source (R_1 may be very large and still achieve correct bias). The current mirror approach retains the high dynamic resistance down to d.c. at the expense of a second m.o.s.f.e.t., Fig. (b).
● Cascode circuits may have the devices in series, sharing the same d.c. current (rather than in parallel as with the complementary stage above). If the input device is a junction f.e.t., the simplest circuits demand only a bipolar transistor with base potential set to a value in excess of the pinch-voltage of the f.e.t. to achieve good cascode performances. The f.e.t. determines the input performance including very high input impedance at low frequencies, while the cascode configuration extends the high impedance to higher frequencies while allowing higher overall gain.
● All f.e.t. circuits are equally possible provided Tr_2 has a higher V_p than Tr_1. Transistor Tr_3 is a source follower to isolate the load R_2 from stray and load capacitances, i.e., increasing bandwidth of output circuit.

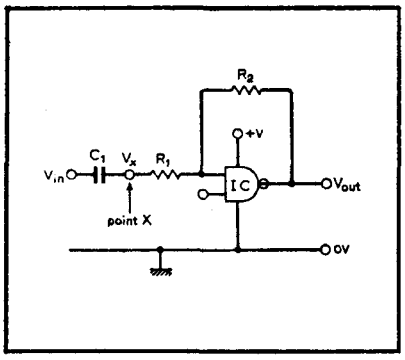
Further reading
FET Circuit Applications, National Semiconductor Linear Applications Handbook, 1972, p. AN32-2.
Schade, O. H. Jr. Application note ICAN-6080, in RCA Data Book SSD-203A, 1973, pp. 299–300.

Cross references
Set 12, cards 1 & 5.
Set 11, cards 5 & 6.
Set 7, card 5.

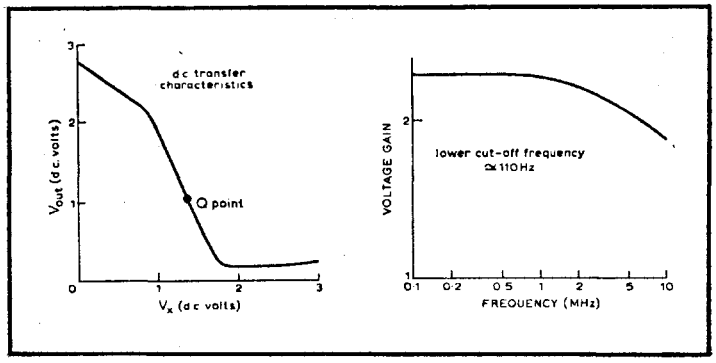
Circuit modifications



Wideband amplifiers with t.t.l., r.t.l., d.t.l.



Circuit data
Supply: 5V, 19mA
IC: 1/4×SN7400
C_1: 10μF tantalum
R_1: 220Ω; R_2: 560Ω
V_{in}: 50mV r.m.s.

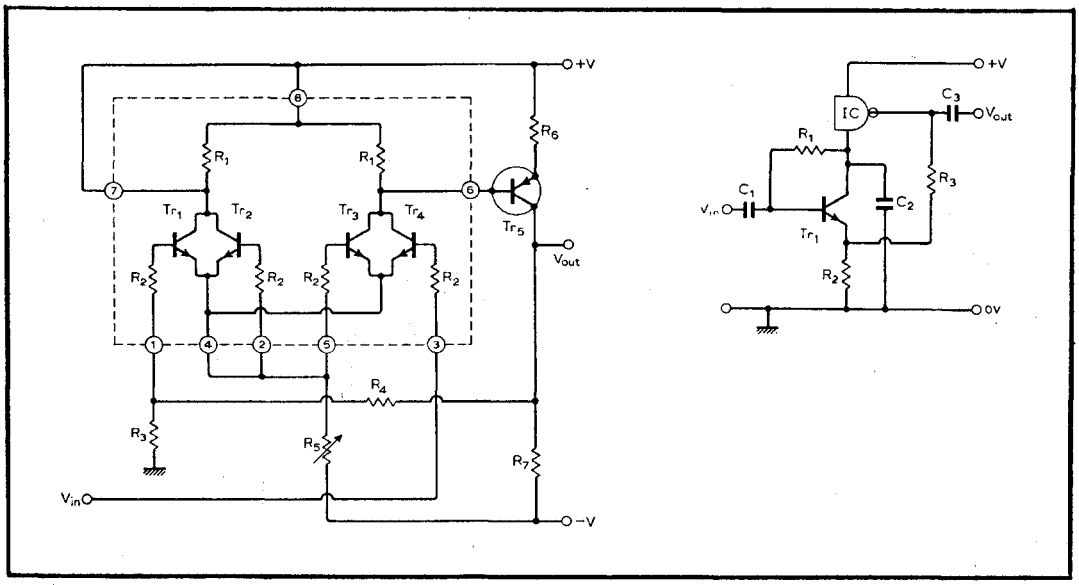


T.t.l. gate description
Without the use of negative feedback, the normal transfer characteristic of the t.t.l. gate is designed to provide well-defined logic levels with a high-gain transition region between them causing the gate to rest in either the on or off condition. Compared with the static on or off state, the supply current drain increases sharply as the gate is switched through the narrow transition region. Although designed for medium-speed digital switching applications a t.t.l. NAND gate can be converted into a linear wideband amplifier. By addition of R_1 and R_2, as shown, the shunt-derived shunt-applied negative feedback has the effect of linearizing the overall d.c. transfer characteristic, eliminating the well-defined logic states, widening the transition region, reducing the gain, and increasing the standing supply current.
Thus, a suitable operating point may be established, with a quiescent supply current of about 19mA, which will allow linear amplification of input signals having levels up to about 800mV pk-pk in the frequency range of approximately 100Hz to 12MHz. Unused gate inputs may be paralleled with the used input rather than being left open-circuit. Alternatively, a logic signal may be applied to the unused input to provide a gating facility on the used input's signal.

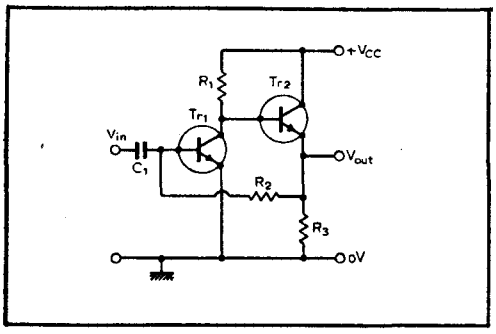
Component changes
Useful range of supply +3 to +5.5V.
Changing R_2 varies gain, shape of the transfer characteristic, and signal-handling capability.
In principle, all four gates in the package may be used simultaneously for linear amplification but the package dissipation is then far in excess of that when used for logic operation.

R.t.l. and d.t.l. gate descriptions.
A dual NAND/NOR r.t.l. gate, contained in a single 914 package (shown dotted), has Tr_1, Tr_2 and Tr_3, Tr_4 connected as a long-tailed pair with R_5 returned to the −V rail and serving as an approximation to a constant-current Source below. Transistor Tr_5 is used as an inverting output stage having a gain of two, with the output at its collector fed back to Tr_1 via R_4 and R_3. Thus, a non-inverted output is available for signals applied to Tr_4 base. The d.c. output voltage can be set to zero with the input grounded, by adjusting R_5. A gain of 10 with bandwidth greater than 10MHz is obtainable with a supply of ±6V, Tr_5 2N3702, R_1 640Ω, R_2 450Ω (internal to 914), R_3, R_5, R_6, 1kΩ, R_4 10kΩ, R_7 2.2kΩ.
● Circuit below right Shows a d.t.l. buffer gate connected in the collector circuit of Tr_1 using the former's +V and extender pins. The gate is operated at its logic switching threshold where it provides high gain. Negative feedback is provided by R_2 and R_3 which determine the overall gain. By decoupling a section of R_2, the gain may be increased without affecting the d.c. operating conditions. A gain of 10, a bandwidth in excess of 500kHz and a load-driving capability of 1 volt into 300Ω is achievable with a supply of +5V, IC ½×932, Tr_1 2N2222, R_1 120kΩ, R_2 120Ω, R_3 1.1kΩ, C_1 10nF, C_2 100pF, and C_3 10μF.

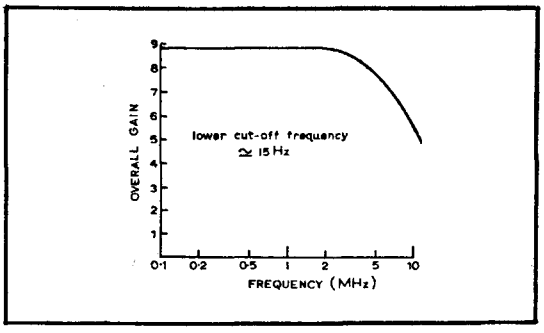
Further reading
Kolataj, J. H. Linearize your t.t.l. gates—then build useful circuits with them, in 400 Ideas for Design, Hayden 1971, pp. 2–3.
Klipstein, D. L. Build an operational amplifier from a dual NAND/NOR gate, in 400 Ideas for Design, Hayden 1971, p. 21.
Jones, D. Wideband amplifier uses a single d.t.l. gate, in 400 Ideas for Design, Hayden 1971, p. 23.



Amplifiers using d.c. feedback pair

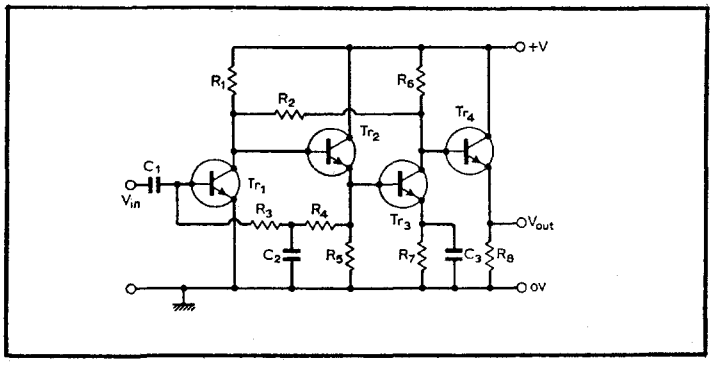


Circuit data
Supply: +5V, 6mA
Tr_1, Tr_2: 1/5×CA3046
C_1: 10μF tantalum
R_1: 3.9kΩ; R_2: 10kΩ
R_3: 150Ω
V_{C_1}: 1.5V; V_{B_1}: 0.67V
V_{E_2}: 0.77V
Source e.m.f.: 50mV r.m.s.



Circuit description
Transistor Tr_1 is connected in the common-emitter configuration and feeds the emitter follower Tr_2 with overall shunt-derived shunt-applied feedback via R_2, which allows the overall gain and input impedance to be adjusted. If the circuit is supplied from an ideal voltage source the gain will be high and the bandwidth relatively small. Such a source could be heavily loaded when connected directly to the circuit shown above. This is due to the equivalent load on the source of h_{ie} of Tr_1 in parallel with $R_2/(1+|A_v|)$, where $|A_v| \approx g_m R_{L_1}$; R_{L_1} being the equivalent load resistance seen by Tr_1. The signal generator available had an output resistance of 100Ω which approximately matched the input resistance of the amplifier. This can be seen to be reasonable assuming h_{ie} of Tr_1 to be approximately 2.5kΩ and $|A_v| \approx 80$ with $R_{L_1} \approx 3k\Omega$.
To define the overall gain and input impedance and to provide a wider bandwidth a resistor may be included in series with C_1. Response shown applies with a 900-Ω resistance included and the overall gain = V_{out}/source e.m.f. If it is desired to match the amplifier input resistance to a defined source resistance, this can be achieved using the circuit as shown above and adjusting the value of R_2.
The integrated-circuit package used contains a five-transistor array, two connected as a long-tailed pair. One of the single transistors has its emitter connected to the integrated circuit substrate which must be connected to the most negative supply rail, hence this transistor can be conveniently used as Tr_1 and any other as Tr_2. A discrete component version of the circuit is also viable.

Component changes
Useful range of $V_{cc} \approx +3$ to +15V.
Maximum source e.m.f. 72mV r.m.s. with $V_{cc} = +5$V.
R_2 adjustable to provide desired overall gain, bandwidth of input impedance, e.g. with R_2=47kΩ and circuit as shown above: overall gain ≈22 and bandwidth ≈3.4MHz.
Resistance values may be scaled by a given factor, e.g. increasing values by factor of 10: overall gain ≈28 and bandwidth ≈1MHz.

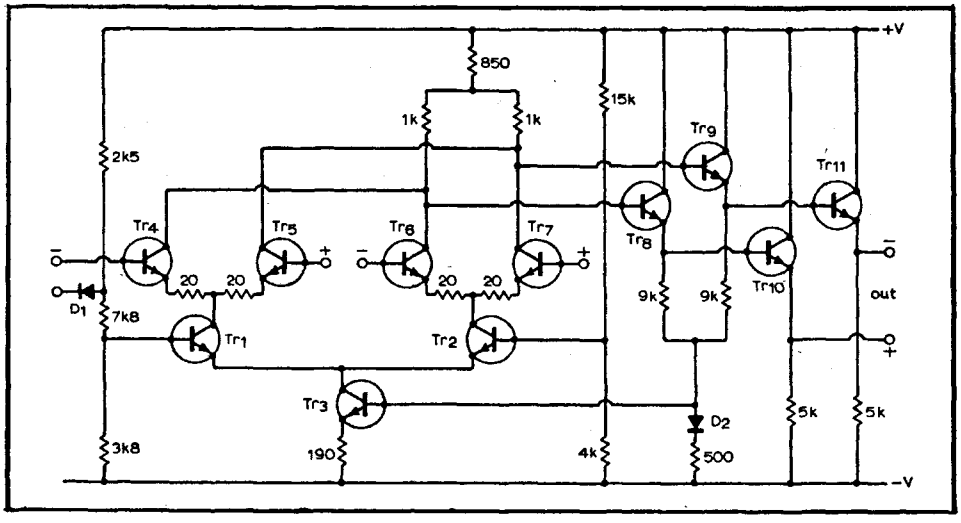


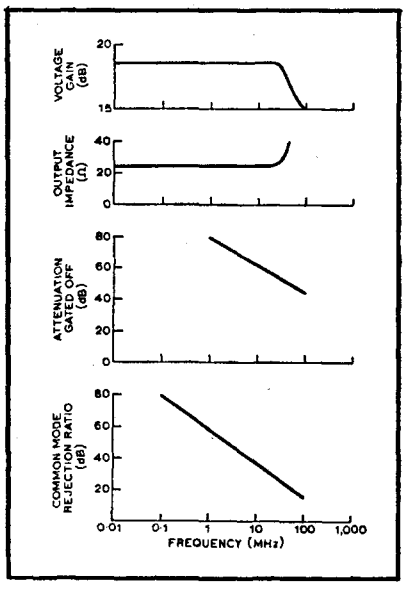
Circuit description
Another amplifier based on the configuration shown top, and also using an integrated-circuit transistor array is shown above. Transistors are contained in a single CA3018 package with Tr_3 emitter and Tr_3 base internally connected. The circuit arrangement of Tr_1, Tr_2 serving as a common-emitter common-collector pair followed by Tr_3, Tr_4 in the same configuration is designed to reduce internal capacitive feedback. The Tr_2-emitter follower acts as a low output impedance source to drive the Tr_3 common-emitter stage and also provides a low-capacitance high-impedance loading on the Tr_1 common-emitter stage.
All stages are d.c. coupled with two negative feedback paths. Feedback from Tr_2 emitter to Tr_1 base is effective at d.c. and low frequencies while that from Tr_3 collector to Tr_1 collector functions at all frequencies. Feedback provides stability of d.c. operating conditions and allows a gain-bandwidth tradeoff to be made. When supplied from a 50-Ω source, a voltage gain of 49dB with a bandwidth of approximately 32MHz is obtainable with a supply of +6V, C_1, C_2 1μF, C_3 470nF, R_1 3.5kΩ, R_2 8.2kΩ, R_3 22kΩ, R_4 18kΩ, R_5 1.8kΩ, R_6 2.5kΩ, R_7 1kΩ, R_8 2.7kΩ, using input signals in the range 7μV to 4mV (r.m.s.). Lower cut-off frequency largely depends on the capacitors used and is about 800Hz with the above values.

Further reading
RCA Application note ICAN 5296, in Databook SSD-202, 1972, pp. 68/9.
Cherry, E. M. and Hooper, D. E. Design of wide-band transistor feedback amplifiers, *Proc.I.E.E.*, vol. 110, 1963, pp. 375–87.
Tuil, J. Transistor-equipped aerial amplifiers—wideband amplifiers, *Electronic Applications*, vol. 28, 1968, pp. 75–8.

Cross references
Set 12, cards 2, 8 & 12.
Set 7, card 9.
Set 4, card 4.

Gated video amplifier





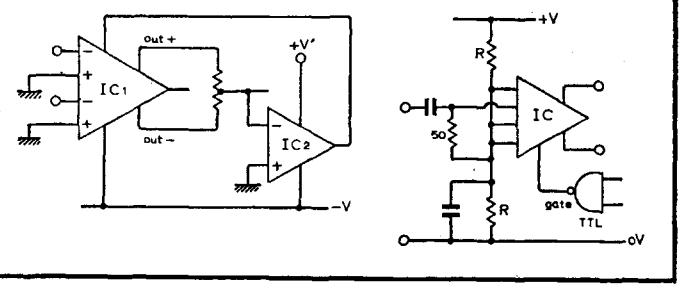
Circuit data
Supply: ±5V, 8mA
IC: MC1445L
Voltage gain: 19dB
Bandwidth: 60MHz
Output attenuation: 60dB with input gated off
Input impedance: ≈8kΩ
Output impedance: ≈22Ω
Input common-mode range: ±2.5V
Quiescent output voltage: ≈0.18V
Gate voltage range: 0.35 to 2.0V

Circuit description
The long-tailed pair is the key to the operation of this circuit, as of so many linear i.cs. The V_{be}/I_C characteristic of a bipolar transistor is given by $I_C = I_S \exp(qV_{be}/kT)$. Transconductance is obtained by differentiating I_C with respect to V_{be}, and is found to be proportional to I_C. Thus controlling I_C gives proportional control of the voltage gain of an amplifier provided that the collector load is low enough to allow the full transconductance to be developed. Used with a single transistor an output signal may be gated on and off by such a means, but the shift in d.c. level carries the gate signal through into the output circuit. With long-tailed pairs as shown, Tr_3 sustains a constant total current using common-mode feedback via the emitters of Tr_8, Tr_9. If Tr_3 conduction increases the collector potentials of Tr_4, Tr_6 must fall regardless of which the current is channelled through. This fall in potential at each collector is coupled via the emitter followers Tr_8, Tr_9 to close the d.c. feedback loop and stabilize operating conditions. The base of Tr_2 is fixed while that of Tr_1 is normally more positive, ensuring that Tr_4, Tr_5 are the conducting transistors, i.e. having sufficient g_m to give an overall voltage gain of 18 to 20dB. Transistor Tr_2 has negligible current and Tr_6, Tr_7 contribute nothing to the output. If the potential at the base of Tr_1 is lowered, either by placing a low direct voltage at the gate input (D_1), or by taking the input to the negative supply rail through a resistor, then the currents in Tr_6, Tr_7 increase at the expense of Tr_4, Tr_5. Hence the signals applied to these differential inputs are gated by a d.c. input. This input may be changed rapidly to allow gating for very short durations or may have intermediate values that allow the inputs to be summed in varying proportions.

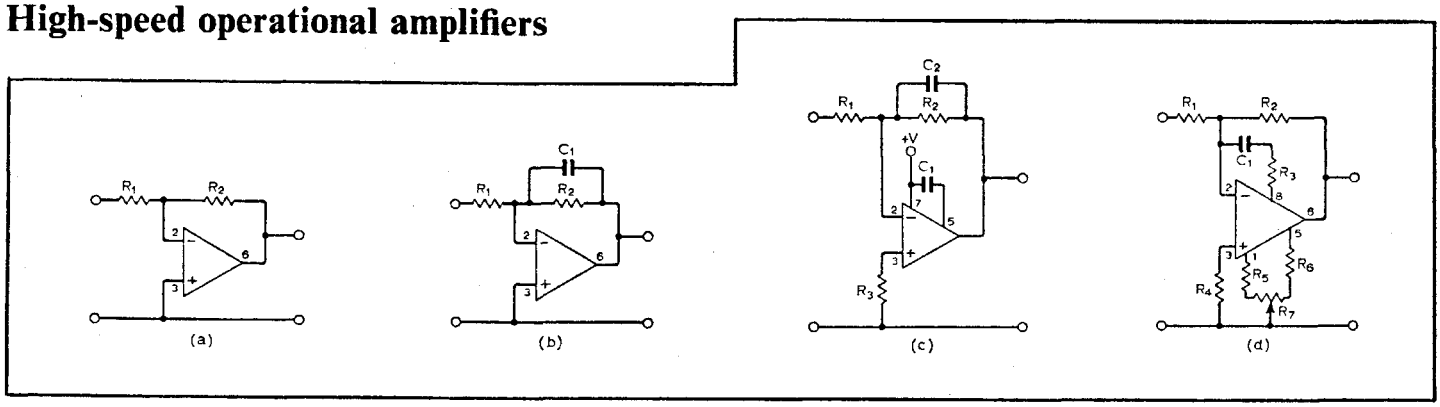
Component changes
IC: MC1445, 1545; similar i.cs with different bias arrangements include Silicon General SG1402/2402/3402. "Discrete" versions based on transistor arrays are also possible but no particular advantages would be expected except possibility of operating at unusual supply voltage/current levels. Balanced modulators/demodulators (MC1496) have similar input stages with free collectors suitable for coupling into tuned circuits.
If the frequency range is more limited, it is possible to adapt analogue multipliers with one input switched between zero and some finite value. This also allows reversal of phase of the output if the control input polarity is reversed.
V_S: ±3.5 to ±12V.
R_L: At low supply voltages the output quiescent current may be increased by placing external resistors in parallel with the 5.0kΩ internal resistors. This increases the signal current that may be capacitively coupled into a load, while lowering the output impedance. 10k to 1kΩ at ±5V supply. Observe maximum dissipation limits of device (dependent on package, ambient temperature, but up to 400mW at <50°C).

Circuit modifications
● By applying the mean value of the output to a standard op-amp, the output can be made to provide a sensitive error signal for departures of the mean i.c. output potential from ground. If the op-amp is operated from a higher positive voltage than that required by the wide-band i.c., then d.c. feedback ensures that the positive voltage applied to the i.c. forces the mean output close to zero (depending on the op-amp offset of a few millivolts). This allows d.c. coupling of signal from input to output of wide-band amplifier with negligible offset.
● For single-ended supplies the unused inputs are taken to a decoupled potential divider, with the option of a 50Ω resistance added to define the input impedance of any signal input, e.g. capacitively coupled as shown. The gate terminal then becomes compatible with a t.t.l., c.m.o.s. logic gate sharing a common ground line.

Circuit modifications



High-speed operational amplifiers



R_1, R_2: 10kΩ
Slew rate: 80V/μs
Small-signal bandwidth 14MHz

R_1: 5kΩ, R_2: 10kΩ
C_1: 5pF
Voltage gain: −2
Comparable figures to (a)

R_1, R_2: 10kΩ, R_3: 5kΩ
C_1: 0.1μF, C_2: 5pF
Shortens settling time to 1μs for 0.1% accuracy after 10V step

R_1, R_2: 4.7kΩ
R_3: 3.3kΩ, R_4: 1kΩ
R_5, R_6: 27kΩ, R_7: 2.5kΩ
Slew rate: 150V/μs

Circuit description

The bandwidth available from operational amplifiers has been extended by many manufacturers to the level where they can be applied to problems previously requiring specially-designed wideband amplifiers. The circuits (a)–(d) use a monolithic i.c. the LM318, showing how manufacturers are able to provide compensation points to modify the high-frequency characteristics—trading in stability margins for increased slew rates, minimum settling times, etc. The internal structure of any particular i.c. at this level of performance is immensely complex and most users will have to treat them as black boxes.

Using hybrid techniques as well as discrete circuitry, amplifiers are available with slew rates in excess of 1000V/μs and bandwidths greater than 100MHz. Methods of construction are more costly than monolithic circuits and they are relevant to specialized applications. In general to achieve such very high bandwidths, the open-loop voltage gain has to be restricted to the range 1 to 5000, while the monolithic amplifier above is optimized for best bandwidth consistent with voltage gains > 100,000.

Further circuits

● As a standard operational amplifier, circuits commonly used with 741, 301 and similar devices may be adapted to high frequency units such as the LM318. Layout and decoupling are important, but high frequency amplifiers, oscillators, filters and the like follow similar configurations, generally with comparable resistance values and reduced capacitances. To combine the wide frequency range with high input resistance the technique shown may be adopted. At very low frequencies the high input impedance amplifier—LM312 or similar—develops its full gain applying its inverted output to the non-inverting input of the high-frequency amplifier. The overall characteristic is inverting and the feedback is negative, while the minimal input current of the high-impedance unit permits R_1 and R_2 to have megohm values. At high-frequencies the integrator configuration of the LM312 leaves the non-inverting input of the LM318 virtually grounded. The signal appears on the inverting input via the CR network and the feedback remains negative. The two time constants define the cross-over regions the overall gain being sustained to 1MHz.

● Non-linear circuits may be extended to higher frequencies, and for example precision half- and full-wave rectifiers operate to an order of magnitude higher in frequency than with 741, etc. At these higher frequencies, Schottky diodes with their smaller forward voltage drop and absence of charge storage are worthwhile alternatives to even high-speed conventional diodes.

● Component values for the voltage follower mode are similar to those for the unity-gain inverter. Not all amplifiers are compensated for 100% feedback, but may be optimized for higher gains instead.

Further reading

LM318 data sheet, National Semiconductor Linear Integrated Circuits Databook, 1972, pp. 185–9.

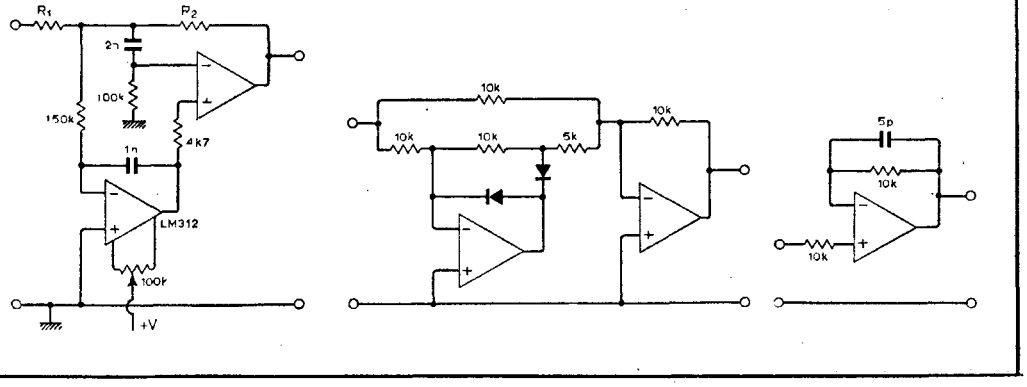
Young, R. L. Lift i.c. op-amp performance, *Electronic Design*, vol. 4, no. 21, 15 Feb, 1973, pp. 66–9.

Motorola application note—AN276, 14MHz wideband amplifier using the MC1530 op-amp.

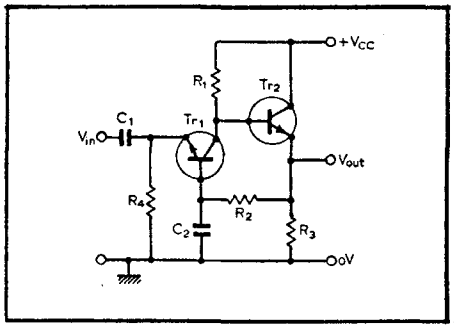
Cross references

Set 12, cards 3 & 4.

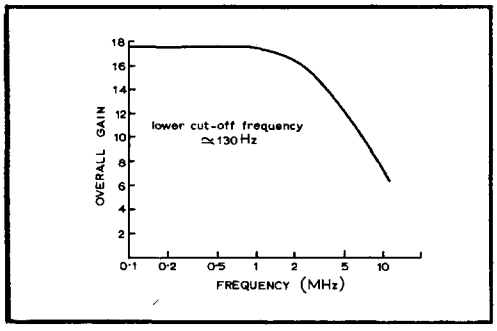
Further circuits



Common-base wideband amplifier



Circuit data
Supply: +5V, 8mA
Tr_1, Tr_2: 1/5 × CA3046
C_1, C_2: 10μF tantalum
R_1: 3.9kΩ; R_2: 10kΩ
R_3: 150Ω; R_4: 470Ω
Source e.m.f.:
30mV r.m.s.
Source res.: 100Ω



Circuit description
The input stage consists of Tr_1 in the common-base configuration with this transistor feeding Tr_2 acting as an emitter follower with overall shunt-derived shunt-applied feedback through R_2. This arrangement is similar to the circuit shown on card 9, except that the source feeds the emitter instead of the base of Tr_1, indicating that the d.c. feedback pair is a convenient method of biasing a common-base stage.
Capacitor C_1 prevents any d.c. component present in the input signal from affecting the biasing, or it may be thought of as necessary if the source cannot sink current from Tr_1. cannot sink current from Tr_1 emitter. Capacitor C_2 grounds the base of Tr_1 to a.c. signals.
The input impedence of the circuit is low and may be adjusted or matched to a source, by means of R_1 which controls the collector current and hence the emitter current of Tr_1. This type of circuit is useful for applications where the common-base configuration offers advantages such as small non-linearity of its transfer characteristic and relatively constant gain with frequency, while providing moderate gain due to the impedance transformation between input and output.
The integrated circuit used is the same as that for card 9 where one transistor has its emitter connected to the substrate which must be connected to the most negative supply rail (0V in this case). Because neither Tr_1 nor Tr_2 has its emitter grounded in the above circuit the substrate-connected transistor cannot be used but its emitter must still be grounded.

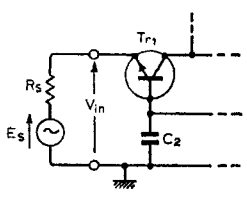
Component changes
Useful range of V_{cc}: +3 to +15V.
Maximum source e.m.f. ≈37mV r.m.s. (with V_{cc} = +5V).
With other resistors in the same ratios R_1 may be:
(a) raised as high as 100kΩ if low quiescent power is a major factor and maximum bandwidth less important.
(b) chosen to provide maximum gain-bandwidth product in Tr_1.
(c) reduced to about 100Ω if maximum output current is required.
R_3 may be reduced towards R_1/h_{FE} and R_2 increased towards $h_{FE}.R_1$.

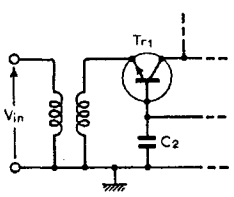
Circuit modifications
● If the signal source can sink direct emitter current of Tr_1, C_1 and R_4 may be omitted and the source connected directly to Tr_1 emitter as shown left, the rest of the circuit remaining the same.
● Where d.c. isolation of the source and Tr_1 emitter is required, an alternative input arrangement to the original circuit using a transformer may be adopted as shown centre, again the remaining circuitry being unchanged. This input transformer may be used to match the source to the input impedance of Tr_1 if desired.
● If it is required to use a common-base stage that provides an output current which is as nearly identical to the input current as possible, a compound transistor may be used as shown right. The base current of Tr_1 is a very good measure of the extent by which its collector current falls short of its emitter current. By feeding back the base current of Tr_1 to the common-base transistor Tr_3 and adding its collector current to the input current, the output current more nearly approaches I_{in}. This technique also raises the output impedance from Z_{out_1} to approximately $Z_{out_1}.h_{fb_1}/(1-h_{fb_3})$ and reduces the distortion from D_1% to approximately $D_1(1-h_{fb_3})$ % compared with Tr_1 alone.

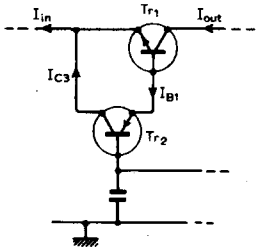
Further reading
Miller, J. R., Solid-State Communications, McGraw-Hill, 1966, chapter 15.
Boxall, F. S. Base current feedback and feedback compound transistor, *Semiconductor Products*, vol. 1, no. 5, 1958, pp. 17–24.

Cross references
Set 12, cards 2, 5 & 9.
Set 7, card 9.

Circuit modifications



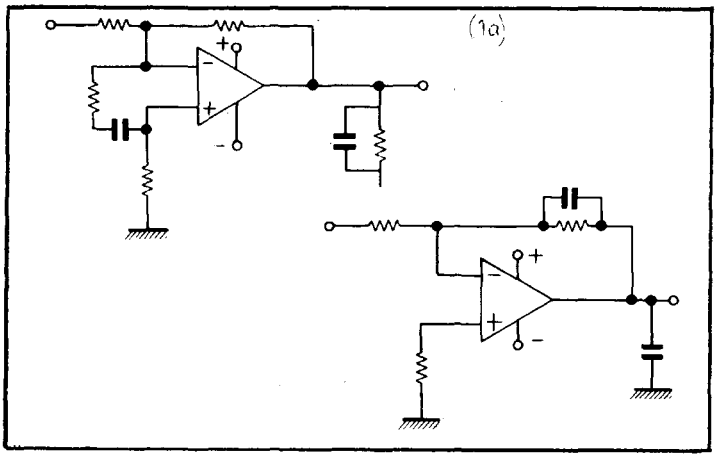




wireless world circard

Set 12: Wideband amplifiers Up-date

1. Both input and output compensation of an operational-amplifier (with 100mA capability) to provide high slew-rates are considered. Fig. 1 (a) shows input compensation, where $R_C = 47\Omega$ and $C_C = 0.01\mu F$, for unity gain. Table 1 indicates variations required to these components at higher gains. For gains greater than 5, a single capacitor across the output is adequate for stability with a sacrifice in bandwidth Fig. 1(b). The slew-rates possible are quoted in the lower part of the table and little change occurs for capacitive loads up to 50nF.

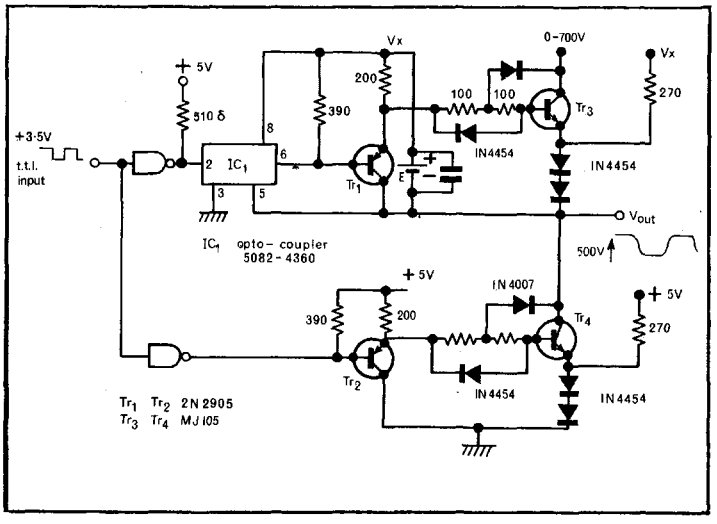


Gain	*C_C nF*	*R_C Ω*	*Slew rate V/μs*	*Bandwidth kHz*
1	10	47	50	600
10	4.7	100	30	600
100	—		100	600
5	200	—	0.75	12
10	100	—	1.5	24
50	20	—	7.5	120
100	10	—	15	240

Reference

Wyland, J. Ideas for Design, *Electronic Design* 10, May 10, 1975.

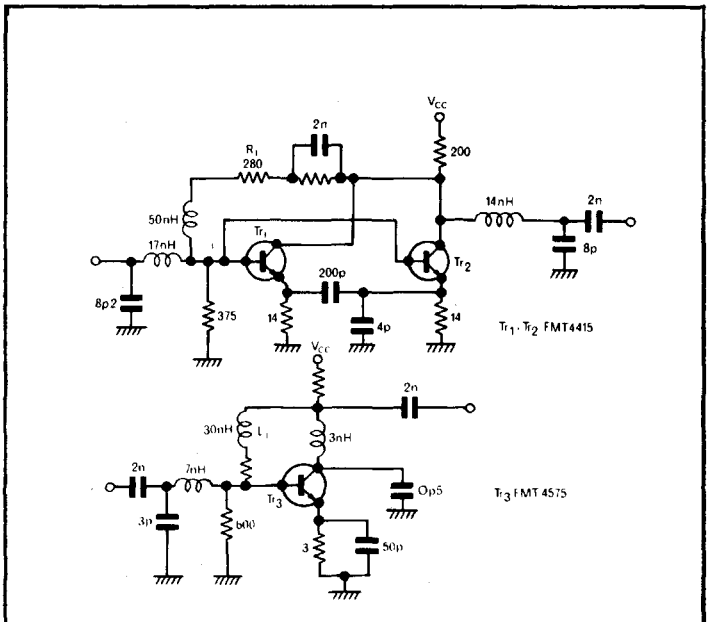
2. This circuit provides a pulse amplifier with a high voltage capability. The circuit is driven from t.t.l. levels, and can operate at frequencies up to 100kHz. High-voltage transistors Tr_3 and Tr_4 are alternately switched on and off via transistors Tr_1 and Tr_2. The bias supply for transistors Tr_1 and Tr_3 is obtained from a 4.5V battery and an optical coupler allows Tr_1 to be switched by the t.t.l. gate. No isolation is required for the lower transistor network which can be driven by t.t.l. directly. When the input is high, Tr_2 is hard on, removing the bias from Tr_4 which is convincingly off because its base-emitter junction will be reverse-biased by about −1.5V. Tr_3 will be biased on giving a high output voltage depending on power supply level.



Reference

Limuti, D. Ideas for Design, *Electronic Design* 20, Sept. 27, 1975.

3. Figs. 3 (a) and 3 (b) are circuits for wideband amplifiers using computer aided design techniques. The first provides an 11dB gain over the range 100–500MHz, and the last provides 14dB gain over the range 100MHz to 1GHz. When two transistors are placed in parallel for medium power (10 to 100mW), equal emitter resistors are included for d.c. balance, and also provide series feedback for the stage. The emitter capacitor C_E provides a gain compensation. Resistor R_1 is the shunt feedback resistor, with an inductor in series to reduce the feedback at the high frequency end of the response, and thus maintain flat gain. The reactive elements being selected at input and output for matching purposes. The single transistor amplifier is designed for discrete components, but for microstrip and thin-film hybrid amplifiers, it is suggested that a transmission line approach is better, for the necessary inductance values. It is suggested that the design in Fig. 3 (b) can be packaged in a standard TO-8 can.



Reference

Steivin, P. Use c.a.d. to optimize broadband amp design, *Electronic Design* 10, May 10, 1974.

wireless world circard

Set 13: Alarm circuits

Rather than dwelling on circuit techniques, the background article brings the concept of data domains to the fore. This interesting approach is an adaptation of that by Malmstadt and Enke, referenced in the article. Card 9, on signal domain conversion, loosely connects with the theme in presenting voltage-to-current and voltage-to-frequency converters and their converse.

Transducer circuits included in this set measure pressure and temperature on card 10, displacement, velocity and acceleration on card 12, and light on card 1. Another important group of circuits, for sensing variations in conductance, is applied to flame, smoke and gas detection on card 1, and as a water-level or moisture-sensitive alarm on cards 10 & 11. Most resistance sensors are bridge circuits, of course, & card 2 shows some useful variants, including a bridge/amplifier combination with both input and output referred to earth. The security alarm of card 11 is one application of the bridge. Cards 4 & 5 are of simple hysterectic level sensors.

Information on driving filament lamps and relays is provided on card 8, while card 4 gives various output stage configurations. Further load-driving circuits can make direct use of the 555—see cards 3 & 5, which also detail other uses of the i.c.

Alarm circuits

In this topic the viewpoint changes. Previously in Circards, circuits have been described as separate entities, with the articles laying a foundation, and the cards showing the practical alternatives. The dilemma is that the title used here, though commonly applied to the topic, can be misleading. This is because so many "alarm circuits" have several identifiable subsections each of which can be readily classified under headings such as those of previous series e.g. Schmitt trigger and astable circuits. Even heading this article "Alarm systems" might confuse since it could convey the idea of a conglomeration of alarms.

A typical alarm arrangment is shown in block diagram form in Fig. 1. An alarm signal is required from some output transducer when the signal from an input transducer indicates a particular fault condition. The intervening blocks are required to process the signal representing the fault condition, to detect a particular voltage/current level which is an analogue of the input parameter, and to deliver power to the output transducer. Before considering each of these sub-sections individually, there is a general principle which can be very helpful in considering such systems—the concept of data domains.

Data domains

Information on physical systems is obtainable in the form of physical quantities such as force, distance, energy. The required information may often have to be obtained by monitoring some more complex property involving a function of the more common parameters. In few cases is the information in such a form that it can be conveyed and displayed directly. It has to be transmitted through some medium or series of media first. To the practising engineer the medium is not the message but rather the barrier that hinders the appearance of that message.

In passing through these media the information takes on new forms or dimensions. For each new set of dimensions we may postulate a domain in which the data exists. Within that domain there may take place further conversions without going outside the domain. Thus the first main division is between inter-domain and intra-domain conversions. The division is arbitrary since the selection of domain interfaces is arbitary. One possible division is discussed below but readers may have their own ideas on this.*

For the purpose of this article, the domains are determined by the following considerations: is the data (a) continuous or discontinuous and (b) instantaneous or not. These conditions applied to electrical phenomena provide us with four domains. In addition there is the much larger physical domain (P) containing all non-electrical data. For other disciplines it is this domain that would be sub-divided into more convenient packages, as for example the heat/light/sound divisions of physics. The electrical domains are thus

	Instantaneous	Non-instantaneous
Continuous	A	t
Discontinuous	D_p	D_s

An A or amplitude function e.g. voltage/current/resistance, is an electrical signal precisely and continuously related to some other function which may or may not be within the A domain itself. It has an instantaneous value which is a measure of some property of the unknown. An example is the electrical resistance thermometer where the resistance (A domain) is a continuously variable function of the instantaneous temperature (P domain) i.e. a P-A domain conversion occurs.

A t function is also continuously variable, but to represent the data a finite time must elapse i.e. it is not instantaneous. This property should not be confused with the finite delays imposed by the physical limitations of systems, which prevent the instantaneous change in an A function. A t function will have corresponding delays in responding to changes in the data, but even with a fixed input requires a finite time to complete the conversion. An example is an oscillator whose frequency is proportional to a voltage. To determine that frequency at least one period must elapse (often many) and the data conversion is non-instantaneous. Such a voltage-controlled oscillator is performing an A-t conversion, the amplitude of the output waveform being irrelevant as all the data resides in the time-function.

Conversions may take place through more than one domain, and the shortest route in a system is not necessarily the best. If we wish, for example, to convert from temperature to frequency (a P-t conversion) we can do so by constructing an oscillator whose frequency is temperature dependent†, or we can use a thermocouple to generate a direct voltage that, amplified, controls a v.c.o. The latter can be considered as a P-A-A-t conversion with the voltage amplifier being an A-A converter i.e. input and output both existing in the amplitude or A domain. Better linearity of frequency against temperature could be achieved in this second approach.

Where the data is required in digital i.e. discontinuous form, a similar distinction can be made as to whether the data appears simultaneously at input and output (within the delay constraints mentioned above) or whether a finite time is required for the data conversion. The two categories resulting are the parallel and series modes respectively (D_p and D_s). They may also be thought of as a spatial and temporal ordering of the data—a pulse train representing the data in serial form conveys that information correctly regardless of the frequency if the order pattern is correct. In a digital voltmeter the data might be converted into serial form following an initial voltage-to-frequency/time conversion, while it would be stored and displayed in parallel form. The data domain conversion pattern would then be A-t-D_s-D_p.

Within each domain, there may be a great variety of possible forms for the data, and multiple conversions can and do take place. Even a "simple" amplifier may have individual stages best viewed as V-I and I-V converters, while a voltage amplifier can be regarded as a V-V converter.

Transducers

These are the interfaces between the physical (P) and electrical domains (A, t, D_p, D_s). The range and variety is too large to cover in such an article as this, but some obvious

*This approach was prompted by the excellent book "Digital Electronics for Scientists" by Malmstadt & Enke (Benjamin) which proposed a slightly different division.

†This can also be considered as a hidden form of P-A-t conversion since the temperature affects some A parameter such as R, C etc.

Fig. 1. Typical alarm circuit with input and output transducers.

examples are worth discussing. If an electrical conductor is subject to temperature variations its conductivity will vary. For metallic conductors the temperature coefficient of resistance is normally positive and the characteristic is sufficiently well-defined to allow precision thermometers to be based on it (platinum resistance thermometers). For semiconductors the coefficient may be negative or positive and of much greater magnitude though generally less well defined. This makes devices such as thermistors, which depend on this property, particularly useful in alarm circuits as a relatively sharp transition takes place in the resistance value and switching of a load is simplified.

If such a resistance which depends on a physical parameter is incorporated in a bridge circuit (Fig. 2) then by suitable selection of the other resistors the critical resistance value of the transducers may be made to correspond to the bridge balance point. Any high gain differential input amplifier may be used to detect this change of polarity about the balance point, providing a large output swing. Addition of positive feedback provides hysteresis, minimizing the output switching that would occur from noise or other stray input signals, when close-to-balance comparators or general-purpose operational amplifiers may be satisfactory in such applications.

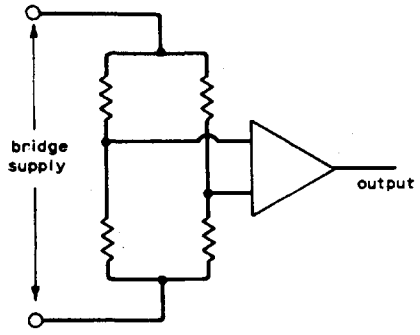


Fig. 2. Bridge circuit for including a sensing resistor.

Other physical parameters may affect the resistance of particular conductors and semiconductors. For example a polycrystalline film of cadmium sulphide in darkness has a very high resistance ($>1M\Omega$), while exposure to sunlight may drop that resistance to a few hundred ohms. Where the changes are as extreme as this, the variable resistance could simply be placed in series with a supply voltage and the load to provide a direct if somewhat imprecise alarm.

Other semiconductors when exposed to particular gaseous impurities show similar large variations in resistance and are now used in gas and smoke detectors, though they require a separate power source to raise their operating temperature. Even the basic resistance thermometer mentioned above can be adapted to detect other physical parameters; for example the flow of air or other fluid across a heated filament removes the heat more rapidly causing the resistance to fall. Thus detection of fluid velocity is a possibility.

Other transducers give a voltage or current that is a function of a physical parameter; the e.m.f. of a thermocouple and the current flow in a reverse-biased photodiode are examples. Yet others may involve the variation of electrical parameters such as capacitance or inductance, coupling between coils, etc. In such cases a common alternative to the bridge technique, still viable with the substitution of a.c. drive to the bridge, is to make the frequency of an oscillator depend on the variation of the reactance used, and follow the oscillator by some form of frequency-sensitive switch.

Following the input transducer the signal may need to be amplified, filtered or modified (domain conversion of some form) in some signal-processing stage prior to being fed to a level-sensing stage. In some cases the two functions can be combined, as operational amplifiers having very high gain can suffice. If the output of the level-sensing device is insufficient in magnitude to drive the required load then a further power stage may have to be substituted (Fig. 1).

Additionally it may be required to cause this output signal to be an audible tone or an interrupted voltage for flashing a lamp. Either case could require an astable oscillator or similar form of generator (Fig. 3). A monostable circuit may be interposed to delay the onset of the alarm output for some period after the appearance of the fault signal and logic gating would be added in more complex systems to generate alarm outputs that depend on a particular combination of input parameters.

Thus most alarm systems can be broken down into simpler blocks and the block diagram of a burglar alarm could be identical with that for a circuit intended to sense icy conditions on a road. By appreciating and making use of this principle, it is often possible to make very economical designs of alarm circuits by adapting the best individual blocks from previously published alarm circuits. The major design problem is then that of making the blocks compatible in respect of supply voltage load requirements and the like.

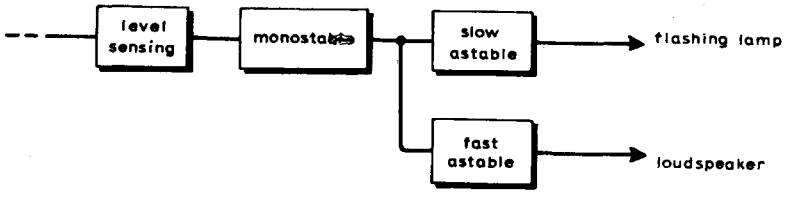
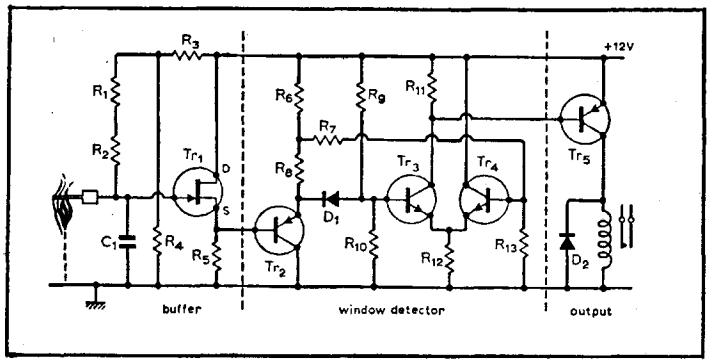
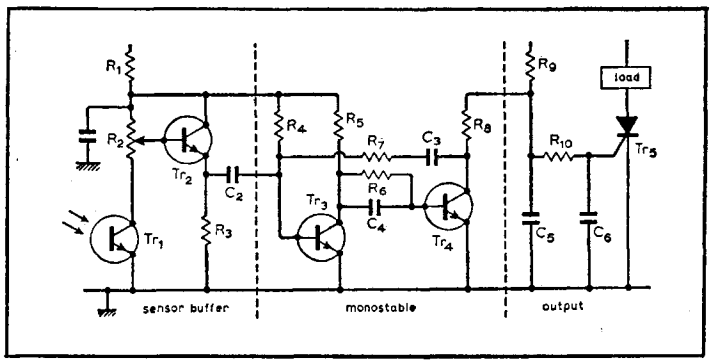


Fig. 3. Arrangement for operating a lamp and/or loudspeaker.

Flame, smoke and gas detectors





Component values

Tr_1: TIS34
Tr_2: BC126
Tr_3: BC125
Tr_4: BC125
Tr_5: BC126
D_1: 1N914
D_2: 1N4002
C_1: 1nF
R_1, R_2: 15MΩ
R_3: 2.2kΩ
R_4: 12kΩ
R_5: 6.8kΩ
R_6: 1.5kΩ
R_7, R_9: 12kΩ
R_8: 820Ω
R_{10}: 15kΩ
R_{11}: 2.7kΩ
R_{12}: 4.7kΩ
R_{13}: 22kΩ
Semiconductors not critical but TIS34 may need selection because of parameter spread.

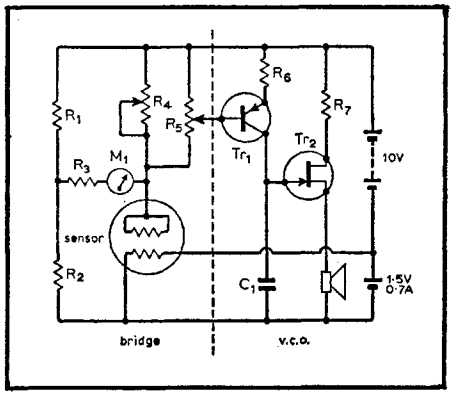
Tr_1: LS400
Tr_{2-4}: 2N712
Tr_5: C106F
R_1: 1kΩ
R_2, R_9: 100kΩ
R_3: 15kΩ
R_4: 470kΩ
R_{5-7}, R_{10}: 10kΩ
R_8: 3.9kΩ
C_1: 16μF
C_2, C_4: 22nF
C_3: 0.1μF
C_5: 50μF
C_6: 4.7nF
Transistor types not critical.

Flame detector

A flame offers a low conductance path to ground. In series with R_1, R_2, that conductance defines a range of potentials on the gate of Tr_1, that leaves the emitter of Tr_2 at a high enough potential to keep D_1 out of conduction, but not so high as to bring Tr_4 into conduction via R_7. Hence Tr_3, Tr_5 conduct holding on the relay—interlocked with the supply for fail-safe operation. If the flame is extinguished Tr_1 gate goes high, driving Tr_4 on via Tr_2, R_7. This removes the drive from Tr_3, Tr_5 and the relay. A short circuit to ground at the input reduces the base potential of Tr_2 bringing D_1 into conduction and cutting off Tr_3 and hence the output. The mid-section of the circuit offers a window action with the relay being held on for a restricted range of flame resistances, higher and lower values giving drop-out. The resistance is high requiring a high input resistance buffer; the output is conventional.

Smoke detector

When detecting the interruption of light by smoke, to avoid the effects of ambient illumination, etc., the light beam may be chopped at source and the resulting a.c. from Tr_1 above used via buffer Tr_2 to trigger the monostable circuit around Tr_3, Tr_4. This prevents the potential applied to R_{10} from rising sufficiently to fire the thyristor. If the load is a horn having an interrupter switch in series with its coil, the thyristor can cease conduction on removal of the gate drive (alternatively a.c. drive to the load would be required).

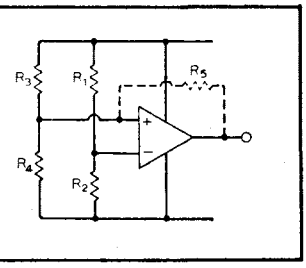


Tr_1: BC126
Tr_2: TIS43
C_1: 0.22μF
LS: 8 to 80Ω
R_1: 470Ω
R_2: 3.3kΩ
R_3, R_4: 10kΩ
R_5: 100kΩ
R_6, R_7: 1kΩ

Gas detector

A particular gas-sensor (TGS from Figaro Engineering, Shannon, Ireland) has two fine wires embedded in a semiconductor. One is used to heat the material, with the resistance between it and the second being reduced on the absorption of deoxidizing gas or smoke. The sensor is sensitive to concentrations of <0.1%, with resistance falling from many tens of kilohms to as low as 1kΩ at high gas concentrations. Response is non-linear and with a recovery time in excess of one minute. Bridge unbalance is detected on M_1 and though repeatable has to be interpreted qualitatively unless special calibration procedures are available. When the unbalance brings Tr_1 into conduction, C_1 charges until the unijunction Tr_2 fires and the cycle recommences. The audible note in the loudspeaker rises from a succession of clicks to a continuous tone as the gas concentration increases. A Schmitt trigger would allow relay drive, while the audible alarm could be transferred to the flame-detector circuit, for example.

Bridge circuits



Components
ICs: 741, V_s ±15V
R_1 to R_4: 10kΩ, R_5: 1MΩ
Bridge voltage: 1.5V (Fig. 2)

Circuit description
Three bridge configurations are shown. In each case the bridge is composed of four resistors, R_1 to R_4, and the circuits are basically Wheatstone bridges with balance occurring for $R_1/R_2 = R_3/R_4$. Substitution of impedances Z_1 to Z_4 would leave the balance requirements unchanged, and other variants such as the Wien bridge can be produced. For resistive elements it may be possible to supply the bridge and amplifier from a common d.c. supply and a high-gain op-amp detects departure from balance. A small amount of positive feedback via R_5 helps reduce jitter in the output when close to balance, but gives hysteresis to the balance sensing.

● If a separate supply is required for the bridge, one bridge balance point may be grounded, removing the need for high common-mode rejection for the amplifier (Fig .2) The errors in all these circuits include voltage offset of the amplifier, 1 to 5mV for untrimmed general-purpose op-amps, and input currents/offset, 10nA to 1μA for conditions as before. For balance detection to within 0.1% this implies bridge voltages in excess of 1V and currents of up to 1mA.

● By opening the bridge and embedding the amplifier in the network as shown, balance is achieved for the same relationship between the resistances, but with input and output both with respect to ground. Fig. 3 has an output that is a linear function of the departure of R_2 from the balance condition (R_1, R_3, R_4 assumed constant as reference resistors). For d.c. applications the input may be one or other of the supply voltages. In all cases best sensitivity is achieved for $R_1/R_2 \rightarrow 1$. If the resistor whose value is being sensed has to have a low resistance, power wastage is avoided by keeping the other pairs of resistances high.

● Another method of achieving input and output as ground-referred signals, is to use an amplifier with push-pull outputs and single-ended input. A simple case is the single transistor, Fig. 4, where the power supply, if properly by-passed, closes the bridge when used for a.c. measurement/sensing. The example shown would pass all frequencies except the notch frequency by $1/2\pi RC$, though with appreciable attenuation near the notch.

● For many purposes, the availability of a centre-tapped supply provides a "phantom-bridge" action. If the ratio of positive to negative supplies remains constant then taking one input of the sense amplifier to the centre-tap leaves only a half-bridge externally. Used for example with photodiodes, the output voltage is proportional to the unbalance currents in the diodes, i.e., to the degree of unbalance in the illumination of the diodes. Because the diodes act as constant-current devices the circuit Fig. 5, is much more tolerant of drift in the centre-tap than for purely resistive elements. The negative feedback gives a linear output-unbalance characteristic. Reversal of the amplifier input terminals would give positive feedback, introducing a switching action and hysteresis as in the first diagram.

● Some i.cs have internal potential dividers which can effectively form part of a bridge. The 555 timer, for example, has its two comparators tapped at ⅓ and ⅔ of the supply voltage via a resistor chain with very good stability to the ratio of their values; the absolute values are not important for such an application (Fig. 6). The lower-threshold detector ("trigger") when held high prevents any output change (input 1 is assumed high) regardless of the status of the reset terminal. The reset terminal regains control only when the trigger input falls below the level accurately defined by the potential divider. With the trigger taken from an external potential divider containing the required sensing element the bridge—balance sensing can be obtained.

Further reading
Markus, J. (ed.), Bridge circuits, in Electronics Circuits Manual, McGraw-Hill, 1971, pp. 84-9.
Graeme, Tobey & Huelsman, Operational Amplifiers, McGraw-Hill, 1971.

Cross references
Set 1, cards 9 & 10.
Set 9, cardr 1 & 11.
Set 13, cards 1 & 3.

Fig. 2

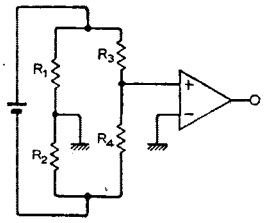


Fig. 3

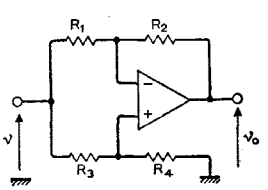


Fig. 4

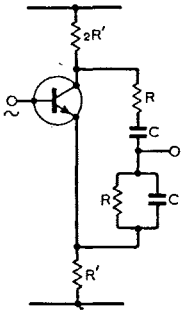


Fig. 5

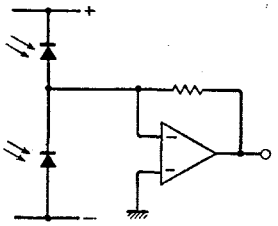
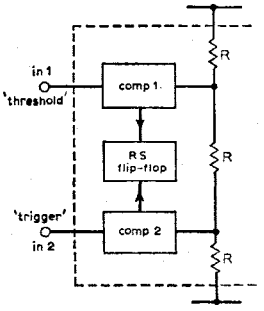


Fig. 6



Time delay and generator circuits

Fig. 1

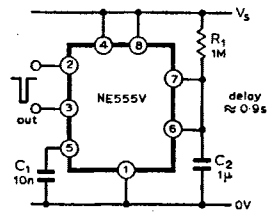


Fig. 2

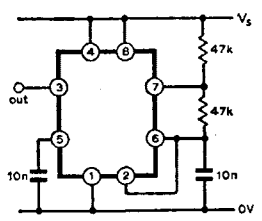


Fig. 3

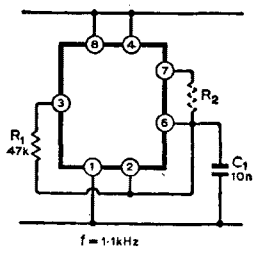
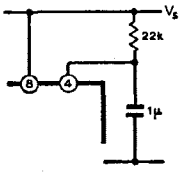


Fig. 4



Circuit description

An i.c. such as the 555, with internal comparators driving a set-reset flip-flop offers great flexibility in the design of alarm systems. With pin 2 high, the capacitor is held low via pin 7. A negative-going edge on 2 allows R_1 to charge C_2 until the potential on 6 passes $2V_S/3$, when the original state is restored.

● Linking the inputs of the two comparators (2 and 6) to the discharge path (7) causes the potential at the common point to cycle between $V_S/3$ and $2V_S/3$, set by an internal Potential-divider (Fig. 2). For both circuits the output has switching characteristics comparable to a t.t.l. gate because of a similar totem-pole output stage. An audible alarm is available by connecting a loudspeaker (3–25Ω) between V_S and pin 3. If V_S is +5V, the on/off condition of the alarm may be controlled by driving pin 4 from the output of a t.t.l. gate.

● An astable can also be constructed by feedback from the output to the paralleled comparator inputs. When the output is high, C_1 is charged (Fig. 3) through R_7 until the upper threshold is passed; the output switches low and C_1 is discharged until the trigger value set by pin 2 is passed. Timing is set by the less well-defined output amplitude, and the frequency is less stable than the basic circuit. Addition of R_2 varies mark-space ratio.

● If the reset terminal 4 is coupled to an RC network (Fig. 4), then a time-delay can be introduced at switch-on, before which firing of the circuit as a monostable cannot be achieved.

● A monostable using c.m.o.s. inverters can use very high-value resistors, giving time delays of > 1s with capacitors of < 1μF. In Fig. 5, a short-duration excursion of the input from + to ground sets the output to zero for the monostable period (about 3s) because the output of the first inverter is high, as is the input of the second until R_2 can pull the gate down by charging C_1. The high impedance makes such monostables useful as touch-operated circuits.

● A related astable circuit Fig. 6 shows an additional resistor R_1 which isolates C_1 from the rapid charge/discharge imposed by the gate protection diodes in both these circuits. The resistor improves the timing stability.

● The output stage of an astable/monostable circuit is important where high voltage/current/power is required. For the 555 timer, the output stage is similar to the typical t.t.l. output (Fig. 7). but with a Darlington-connected top section. The positive output is thus at least 1V below supply while the low output can be to within 0.1V of ground at low currents. Above 50mA the voltage drops may reach 2V and 1V respectively.

● For some applications the open-collector output of t.t.l. devices such as SN7401 gives convenient driving of loads, while other devices such as SN7406 will withstand collector-emitter voltages of up to 30V. (Fig. 8).

Further reading

Three articles, by Robbins, Orrel and De Kold, in *Electronics*, 21 June, 1973, pp. 128-32.

Application note for XR-2556 timing circuit, Exar, 1973.

Cross references

Set 3, card 9.
Set 13, card 5.

Fig. 5

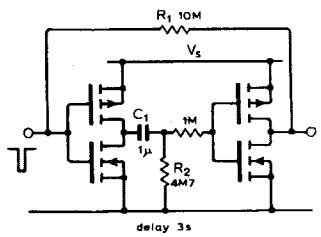


Fig. 6

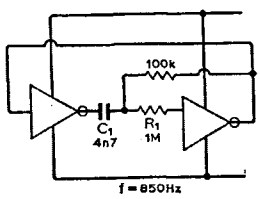


Fig. 7

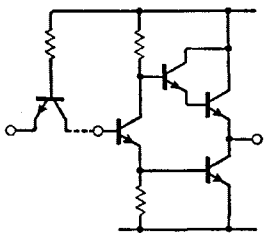
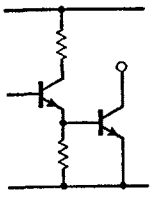


Fig. 8



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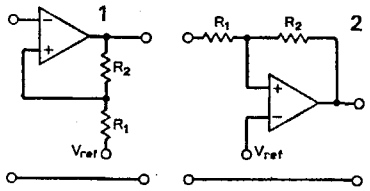
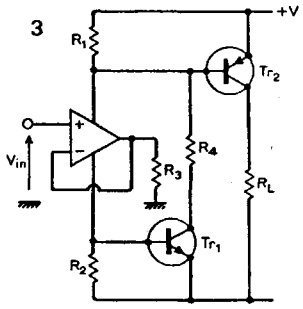
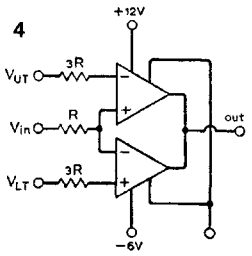
Level sensing and load driving



R_1: 1kΩ
R_2: 100kΩ
ICs: 741
V_S ±15V





R: 1kΩ.
IC: 711.

Tr_1: BFR41, Tr_2: BFR81
V_S ±6V, R_L: 200Ω IC: 741.
R_1 to R_3: 100Ω, R_4: 1.2kΩ.

Circuit description

The basic level-sensing circuits shown may be used with or without positive feedback, to obtain an output change as the input passes a defined level or levels. For $R_2 \to \infty$, $R_1 \to 0$, amplifier gain determines the range of input voltages for which the output is not switched hard to one or other extreme. (Typically 1 to 20mV for comparators, required to operate at high speeds; 0.1 to 5mV for op-amps where accuracy of level-sensing makes their slower operation an acceptable penalty.) Hysteresis introduced by positive feedback allows the circuit to latch into a final state after the first excursion through a given level, provided the input cannot reverse its sense sufficiently to pass back through the other switching level. These circuits can thus perform the combined functions of level-sensing and set-reset action required in many alarms if for example the signal is a positive-going voltage initiating the set action, while the reset action is a negative-going pulse over-riding the former, e.g., a resistor taken from the non-inverting input to the negative rail.

● An adaptation of the output stage shown in Fig. 5 gives an output when the p.d. across either R_1 or R_2 exceeds about 0.6V. In the former case this corresponds to a positive input voltage defining sufficient positive supply current via R_3, i.e., $V_{in}R_1/R_3 \approx 0.6$V. Similarly a negative input voltage switches the output via Tr_1. The switching action is not particularly sharp as it uses only the gains of the transistors.

● A standard window comparator gives sharper switching but requires two amplifiers/comparators and still requires an additional transistor if an output swing comparable to supply voltage is required, e.g. for efficient switching of lamps relays, etc. particularly at higher currents.

● A previously-described output stage (set 2) gives push-pull drive using one op-amp as driver. Resistors R_1, R_2 are selected to keep Tr_1, Tr_2 out of conduction in quiescent state. The op-amp is used in any of the sensing/oscillating modes that result in p.ds across R_3 sufficient to drive Tr_1, T_2 into conduction. Either may be used alone for driving lamps, relays, or the circuit as shown may be capacitively coupled to a loudspeaker for a.c. power drive.

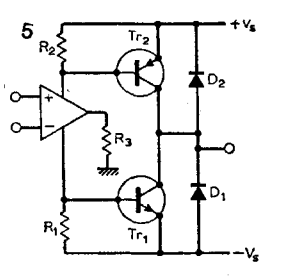
● An output stage using a bridge configuration requires antiphase switching at the inputs, but gives a load voltage whose peak-peak value is twice the supply voltage. This is equally applicable to audio alarms or to driving of servo systems for which it was designed.

● Complementary m.o.s. buffers may be used to drive complementary output transistors as shown and with the aid of an additional inverter a similar stage provides a bridge output. The transistor base current is limited to a few milli-amperes but in all these output stages, short-duration current spikes may occur during the output transitions. Diode protection against inductive voltage spikes as in Fig. 5 should be used for loudspeaker, relay and solenoid loads.

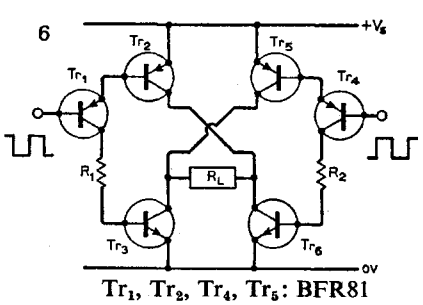
● Any of the output transistors may in principle be replaced by the compound transistor pairs if higher peak currents are needed. To reduce the above requirements it is worth considering the use of f.e.t. devices as the input transistor of the pair.

Further reading

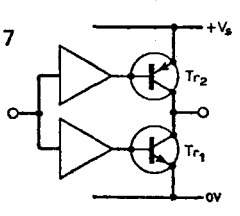
Electronic Circuits Manual (Markus, McGraw-Hill, 1971): Main circuits—pp. 1-6; lamp control circuits—pp. 344-9; trigger circuits—pp. 889-907.
Linear Integrated Circuits Handbook, Marconi-Elliot, pp. 165-170.
Industrial Circuits Handbook, SGS-Fairchild, pp. 6-13.



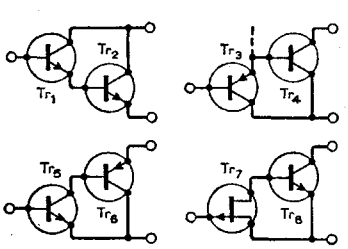
Tr_1: BFR41, Tr_2 BFR81
D_1, D_2: 1N4001, IC: 741
R_1, R_2: 180Ω, R_3: 680Ω
V_S ±6V



Tr_1, Tr_2, Tr_4, Tr_5: BFR81
Tr_3, Tr_6: BFR41
R_1, R_2: 100Ω
V_S +6V
I_L up to 300mA

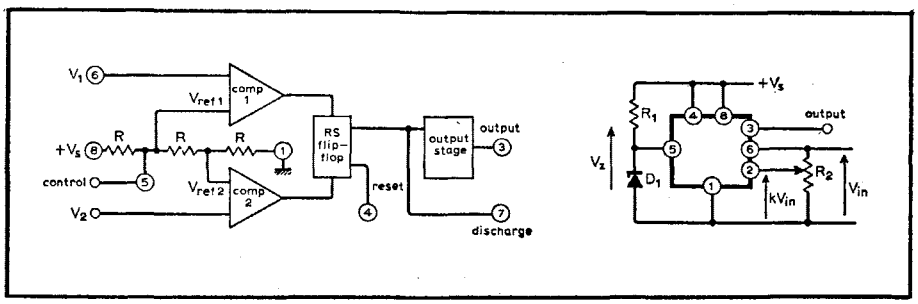


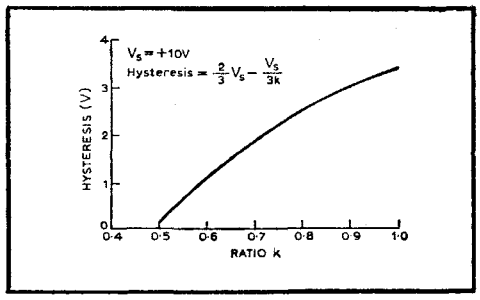
IC: ¼ CD4049
or CD4050
Tr_1: BFR41
Tr_2: BFR81



Tr_1, Tr_5: BFR41
Tr_2, Tr_4: 2N3055
Tr_6: MJE371
Tr_7: 2N3819

Applications of 555 timer





Typical performance
IC: NE555V (Signetics), V_S +10V.
R_1: 2.2kΩ, R_2: 10kΩ.
k=0.6, D_1: 5.6-V Zener diode.
Upper set point: 5.7 (V_z).
Lower set point: 4.75V ($V_z/2k$).
Output swing: 9V for $R_L \geqslant 250\Omega$.
If R_1, D_2 omitted, $V_{ref1}=2V$, $V_{ref2}=V$ and set points become $2V$ and V/k.

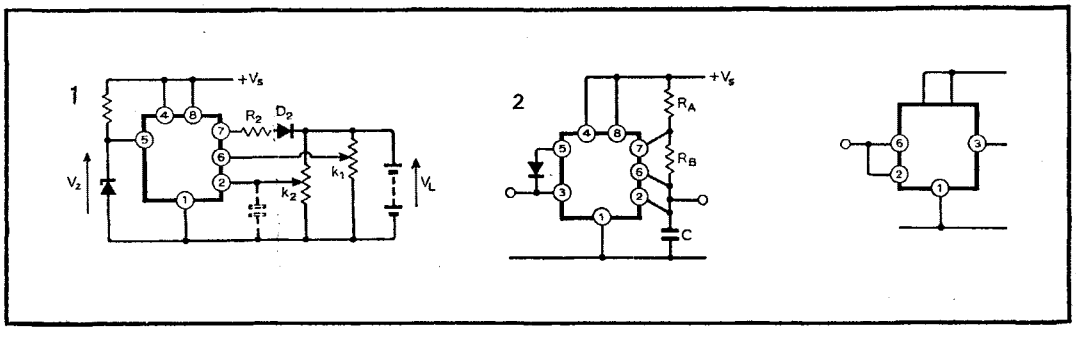
Circuit description
The 555, designed as a timing circuit with either monostable or astable operation, has internal circuit functions that allow it to be used for many other purposes. In alarm systems, the power output stage that permits currents of either polarity of up to 200mA (though 50mA minimizes voltage losses) means that lamps and relays can be driven quite readily. When used as an astable circuit the output square wave can be applied to a loudspeaker to give an audible alarm, while a voltage fed to the control terminal modulates the frequency for warble or two-tone effects. As a monostable circuit it can be used to provide delays from microseconds to minutes, allowing, for example, a warning alarm to be held for a defined period of time after the appearance of the condition being detected. In such cases the condition (closure of a switch in a burgular alarm for example) is converted into a negative-going pulse, applied to the trigger input. A further application for the device involves the controlled hysteresis provided by the two comparators biased from an internal potential divider. With $V_1 > V_{ref1}$ the output is driven negative via the flip-flop which ignores any further excursions of V_1 about V_{ref1} in either sense. When V_2 falls below V_{ref2} the flip-flop is reset, the output going positive. In the astable circuit $V_1=V_2$, $V_{ref1}=2V_S/3$, $V_{ref2}=V_S/3$ and the capacitor is charged and discharged between $V_S/3$ and $2V_S/3$.

Component changes
IC: Motorola MC1455.
Separate comparators could be used with independent reference voltages or a single comparator with hysteresis defined by feedback—see Series 2.
V_S: 4.5 to 18V. At low voltages the saturation voltages at the output may not allow adequate drive to electromechanical/filament lamp loads.
R_1, D_1: Any network to provide constant voltage at control input. Voltage may be to within 1V of common line or positive supply, but for optimum performance should be close to $2V_S/3$.
R_2: 1k to 1MΩ. At low values, excessive loading of source; at high values inaccuracies due to threshold current of up to 0.25μA.

Circuit modifications
● Use as battery charger illustrates method well (Fig. 1). Upper threshold when $k_1V_L=V_z$; lower threshold when $k_2V_L=V_z/2$. When upper threshold is exceeded output at pin 3 reverse-biases diode D_2 and battery discharges into load when present. As voltage V_L falls below lower threshold, voltage at pin 3 rises and charges battery through limiting resistor R_2. Hysteresis may be reduced towards zero for $V_z/k_1 \rightarrow V_z/2k_2$.
● To increase hysteresis, the potential at pin 5 may be reduced following a transition through the upper threshold. This may be done as in Fig. 2 by using output pin 3 via a diode—both thresholds are varied if the diode is replaced by a resistor.
● The increased swing simplifies the triggering of a following 555 used as a Schmitt trigger, as the capacitor voltage in Fig. 2 can approach zero.

Complete alarm systems can be based on such circuits combining level sensing, time delays and waveform generation, as well as audible alarms.

Further reading
Four articles, by De Kold, McGowan, Harvey & Pate, in *Electronics*, 21 June 1973, pp. 128–32.



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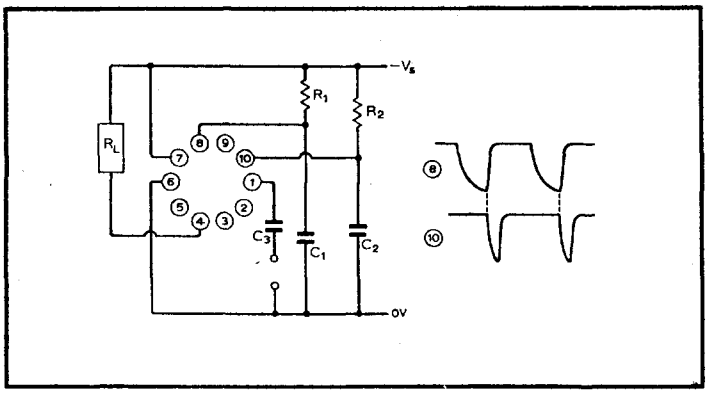
Frequency sensing alarm



Typical performance
IC: FX101 (Consumer Microcircuits) −12V supply, −3mA+load current.
V_{in}: 250mV pk-pk to pin 1.
R_1, R_2: 470kΩ.
C_1: 22nF, C_2: 10nF, C_3: 0.1μF.
Ground pins: 2, 3, 9.
Output on for: $f > 150$Hz ($f \approx 1/0.6C_1R_1$).
Pin 1 signal input.
2 grounded, holds switch state during signal loss.
open, switch off.
ground via 'C', switch off after signal break of 200ms/μF for 'C'.
3 ground, circuit automatically resets on change off.
open, switch latches when turned off.
5 link to 8, switch latches when turned on. Ground 3.
link to 8 via 'C', hysteresis in datum point of 'C'/C_1 × 100%.
9 ground, datum mode, switches on for $f > f_1$.
open, band mode, on for $f_1 > f > f_2$.
link to pin 5, output toggles at $f/20$ when in band.

Circuit description
The circuit is a monolithic m.o.s. i.c. which uses external RC elements to fix the frequencies at which the circuit provides a switching action. It does so via two separate switching times defined by C_1R_1 and C_2R_2, as from a pair of monostable circuits with the second time interval being initiated at the end of the first. The input may be a repetitive signal of arbitrary waveform, provided the amplitude is in excess of 100mV pk-pk (though it should not exceed 20V pk-pk). Internally this is presumably squared by a Schmitt type of circuit to trigger the monostables. Three distinct conditions may exist; if the period of the received signal is $t = 1/f$ and the two delays are $t_1 = k/C_1R_1$ $t_2 = k/C_2R_2$, then $t < t_1$, $t_1 < t < t_1 + t_2$, $t > t_1 + t_2$. These conditions are distinguished by additional internal circuitry that allows sensing of frequencies above a given datum or within a given band with a switched output that can be made to latch on or off, toggle at a lower frequency ($f/20$), and hold on during signal failure or for temporary interruptions of the signal. The upper frequency in the band mode or the datum in the datum mode is set by t_1 and the lower band-frequency by $t_1 + t_2$. The circuit provides frequency-sensing function similar to comparators Schmitt-triggers and window-comparators.

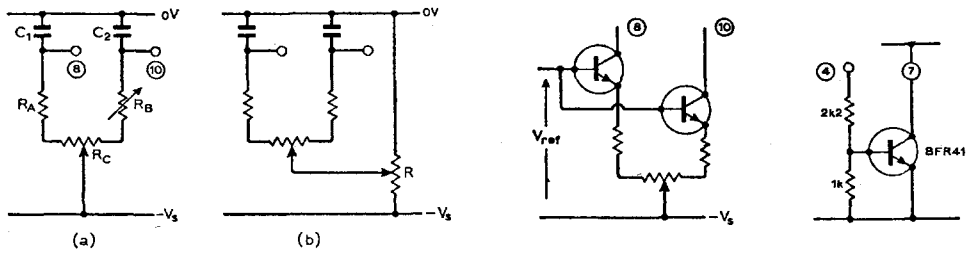
Component changes
Vs: −12 to −22V some samples operate with reduced accuracy down to −8V.
V_{in}: 0.1 to 20V pk-pk.
freq. set points: 0.01Hz to 50kHz.
response time: within 5 to 10 cycles of receipt of correct frequency.
R_1, R_2: 100k to 1MΩ.
C_1, C_2: 250pF to 1μF.
C_3: 10nF to 1μF (not critical).

Circuit modifications
● As the lower frequency in the band mode is affected by time constant C_2R_2 in the original circuit while the upper frequency is not, variation of R_2 increases the band by variation of its lower bound only. For $C_1 = C_2 = C$, variation in the tapping point of R_C in (a) at left leaves the sum of the time constants unchanged at $(R_A + R_B + R_C)C$, i.e., it is the lower frequency that remains constant while the upper frequency is changed.
● Variation in both frequencies while retaining a reasonably constant ratio of f_2:f_1 (the equivalent of a constant Q), can be achieved by varying the common bias applied to the resistors. If strong dependence on supply voltage is to be avoided the bias voltage should be supply-proportional as in (b).
● Constant-current sources allow linear control of period against a separate reference voltage, which may be supply-proportional (centre).
● Filament lamps may be driven via an additional transistor, currents up to 100mA or so being provided by circuit on right. Direct drive of reed relays, l.e.ds is possible though current is marginal.

Further reading
Volk, A. M. Two i.c. digital filter varies passband easily, *Electronics*, 15 Feb. 1973, p. 106.
McKinley, R. J., Versatile digital circuit filters highs, lows or bands. *Electronics*, 21 June 1971, p. 66.
FX101: Consumer Micro-circuits data sheet D/026.

Cross references
Set 1, cards 6 & 7.

Circuit modifications



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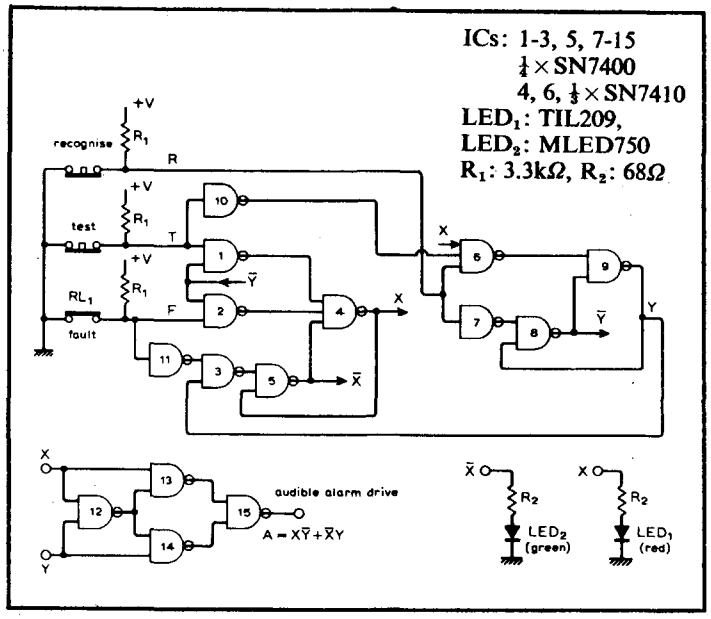
Digital alarm annunciators



Circuit function
It is assumed that a fault condition is the opening of relay contact RL_1, though any other sensor that maintains the NAND-gate input terminal at a low ('0') level is adequate. A fault will turn off a "safe" green light and illuminate a "danger" red light, and operate an audible alarm. When the "recognize" push-button is depressed, the red light stays on, but the alarm is silenced. When the fault clears, the alarm is restarted, the green light comes on and the red light goes off. The "recognize" button is again pushed to reset circuit to its normal state.

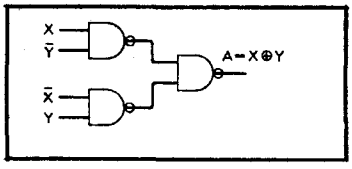
Circuit operation
Consider the circuit in its normal state where inputs R, T and F are at zero volts (or binary zero), i.e. $R=T=F=0$ and $X=0$ ($\bar{X}=1$), $Y=0$ ($\bar{Y}=1$) and hence LED_1 is energized (green) and LED_2 (red) is off.

If a fault occurs, RL_1 opens, F goes high (or binary one), i.e. $F=1$, causing $X=1$ ($\bar{X}=0$), but the state of Y (and $\bar{Y}$) remains as before. Hence $A=1$, and triggers audible alarm. Pushing the recognize button causes $R=1$, and as $F=1$, $T=0$, then $Y=1$ ($\bar{Y}=0$), but X does not change. LED_1 remains on, but $A=0$, and alarm stops. This state will be maintained until the fault is cleared.

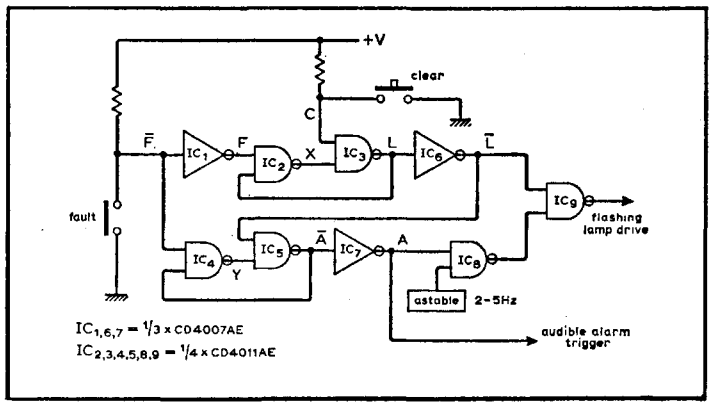
When the fault is cleared, $R=F=T=0$, Y does not change, but $X=0$ ($Y=\bar{X}=1$, $X=\bar{Y}=0$). Hence LED_2 is illuminated, $A=1$, and the alarm operates.

Final recognition of the fault clearance is obtained from $R=1$, which will return circuit to its normal state, i.e. for $R=1$, $F=T=0$, $Y=0$ and $X=0$. Depression of the test button will check LED_1 and the alarm, when started from normal state with LED_2 on.

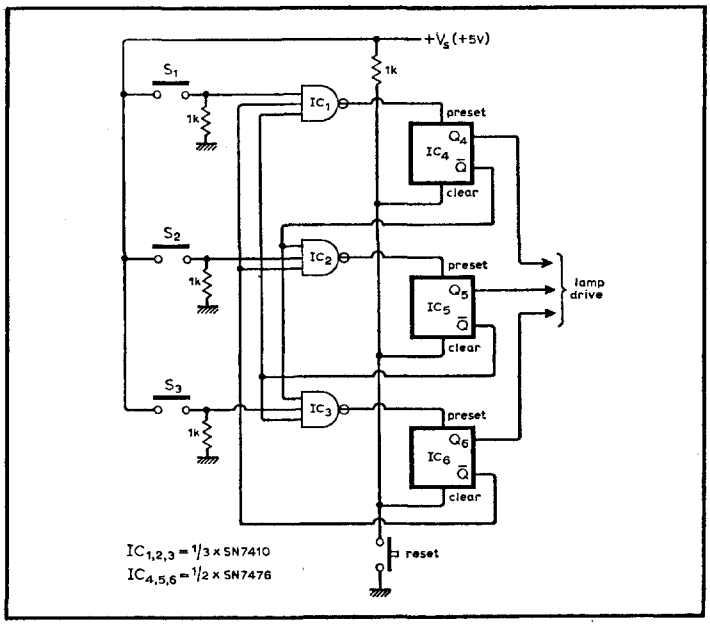
Circuit modification
As X, $\bar{X}$, Y, $\bar{Y}$ are available, the exclusive-OR function of A can be obtained as shown.



Further reading
Zissos, D., Logic Design Algorithms, Oxford 1972.



Circuit description
Complementary-m.o.s. devices may be used in the circuit above to minimize stand-by power consumption.
Normal safe condition obtains with $L=A=0$, $\bar{F}=1$. When the fault-switch closes, $F\rightarrow1$ and since L is already low, $X\rightarrow0$. Memory circuit IC_2, IC_3 does not change. Also since $\bar{F}=0$, $Y\rightarrow1$, and hence $\bar{A}$ is forced to zero, therefore $A=1$. This transition may be used to switch an audible alarm.
Simultaneously the oscillator gate is opened which will cause lamp flashing at a rate determined by the astable frequency.
If the fault is rectified, the alarm condition is maintained until the clear button is pressed causing C to below. Hence $L\rightarrow1$, and will latch in this condition via memory circuit IC_2 and IC_3. Also $\bar{L}=0$, thus $A=0$, this condition being maintained via IC_4 and IC_5, and the alarm is silenced.



Circuit description
Arrangement right allows detection of first-fault occurrence from three sensors S_1, S_2, S_3, this number being restricted by the number of inputs available per NAND-gate. Outputs Q_4, Q_5, Q_6 are set to zero when the reset button is depressed. The $\bar{Q}$ output of each flip-flop is applied to the other two NAND gates, but not to the one associated with itself. Hence two of the three inputs of each gate are high. If S_2 closes, for example, IC_2 output goes low, and this negative-going edge being applied to IC_5 preset terminal sets $Q_5=1$ (and hence $\bar{Q}=0$). Therefore IC_1 and IC_3 are now inhibited and cannot respond to a fault condition.

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Filament lamps and relays

Fig. 1

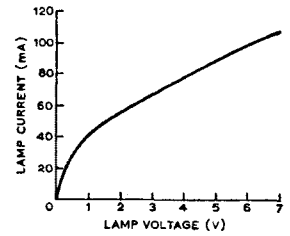


Fig. 2

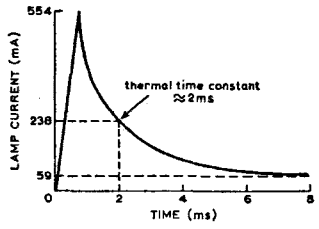
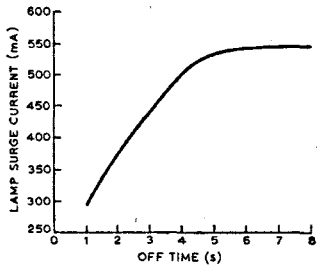


Fig. 3



Filament lamps are widely used as visual alarm indicators and often connected in the collector-emitter circuit of a bipolar transistor that is switched on and saturated under alarm conditions. These lamps have a positive temperature coefficient of resistance with a large difference of resistance between the cold and hot states—see graph 1 which is typical for a 6V, 100mA panel lamp. When switched on across a voltage source, a large current surge flows in the lamp, and switching transistor, which then decays exponentially to its normal or rated value in the hot state. This surge may be ten times the rated current, or even higher, shortens the life of the lamp, may destroy the switching transistor or blow the power supply fuse. graph 2 shows the typical initial surge current characteristic of a 6V, 60mA panel lamp having a thermal time constant of about 2ms.

When lamps are used as flashing alarms, the initial surge current is as shown in graph 2 but the surge current on successive pulses depends on the thermal time constant and the time between flashes. Graph 3 shows the typical variation in surge current when a 6V, 60mA panel lamp is switched on for 5 s then off for t_{off} seconds.

If the p.d. applied to the lamp is gradually increased the current rises in a controlled manner to its normal operating value, prolonging the life of the lamp and reducing the probability of transistor damage. A simple arrangement is shown Fig. 4, where Tr_2 is normally held on and saturated with a low value of $V_{CE(sat)}$ holding Tr_1 and the lamp off. Under alarm conditions, the base drive to Tr_2 is removed and the capacitor charges through R_B. The base voltage of Tr_1 rises exponentially so that the lamp surge current is avoided.

To prevent damage to Tr_1 should the lamp become short-circuited, a resistor R_C could be included in Tr_1's free collector, but this would reduce the lamp voltage in normal operation. Circuit Fig. 5 shows a modification that allows an almost normal lamp voltage and also limits the short-circuit current to the desired value by using only a small R_C value and a saturating transistor Tr_3.

Relays are used to actuate alarm devices that need to be isolated from their control circuitry for various reasons such as their current, voltage or power requirements being incompatible with the electronic circuitry. Circuit Fig. 6, of a commonly-used relay drive circuit which takes into account both the resistive and inductive properties of the relay coil. When actuated, the steady-state coil current is fixed by the coil resistance and supply voltage, but when Tr_1 is turned off the inductance of the coil causes the collector voltage to rise towards a level greatly exceeding V_{CC} if the protective diode D_1 were omitted. Diode D_1 allows V_{CE} to rise only slightly above V_{CC} before the diode conducts to dissipate the energy stored in the relay coil. When Tr_1 turns on D_1 is reverse-biased and does not affect the operation. The diode must be able to withstand a reverse voltage slightly greater than V_{CC} and be able to conduct the relay-coil discharge current for a brief time. Transistor Tr_1 must have a V_{CE} rating exceeding V_{CC} and be capable of carrying the relay operating current.

If a relay is required to operate when an input level exceeds a certain predetermined value, it may be included in a Schmitt trigger circuit; e.g., the relay coil and protective diode could replace R_4 in the basic circuit of series 2, card 2.

If the alarm indication uses a l.e.d. or alpha-numeric array of l.e.ds consult series 9, cards 2, 5 & 6.

Further reading

Shea, R. F. (Ed.), Amplifier Handbook, section 31–6, McGraw-Hill, 1966.
Egan, F. (Ed.), 400 ideas for design, vol. 2, pp. 18/9, Hayden, 1971.
Cleary, J. F. (Ed.), Transistor Manual, pp. 202, General Electric Co. of New York, 1964.
Industrial Circuit Handbook, section 2, SGS-Fairchild, 1967.

Cross references

Series 2, card 2.
Series 9, cards 2, 5 & 6.
Series 13, cards 4 & 7.

Fig. 4

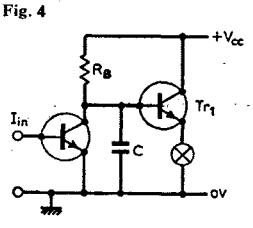


Fig. 5

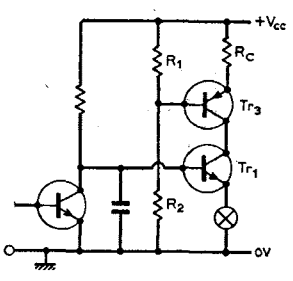
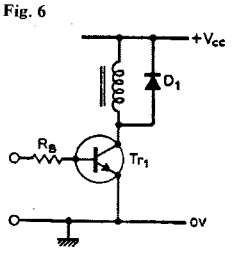


Fig. 6



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Set 13: Alarm Circuits—9

Signal domain conversion

Fig. 1

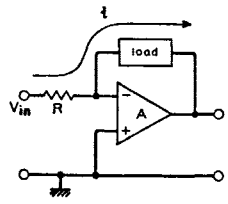


Fig. 2

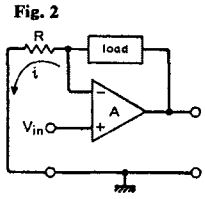


Fig. 3

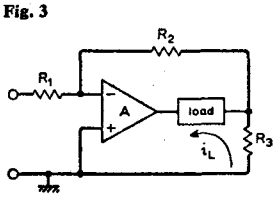


Fig. 4

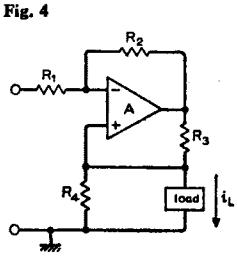
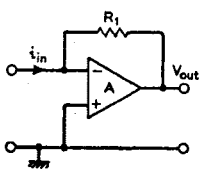


Fig. 5



Voltage-to-current conversion
It is often required to supply signals to relatively long transmission lines in which case the signal is more convenient in current form rather than as a voltage. Thus, voltage-to-current converters are useful and may be realized using operational amplifiers especially if the load is floating. Figs. 1 & 2 show the more common forms the former being an inverting type and the latter non-inverting. In both Figs, $i = V_{in}/R$ and is independent of the load impedance, but the source and operational amplifier must be able to supply this load current in Fig. 1, whereas little source current is needed in Fig. 2 due to the high input impedance of the amplifier. Fig. 3 shows another floating-load V-to-I converter which requires little source current if R_1 is large and allows i_L to be scaled with R_3, the operational amplifier supplying the whole of the load current; $i_L = V_{in}(1/R_1 + R_2/R_1R_3)$. The circuit of Fig. 4 is suitable for V-to-I conversion when the load is grounded. When $R_1R_3 = R_2R_4$ the load current is $i_L = -V_{in}/R_4$ and the current source impedance seen by the load very high.

Current-to-voltage conversion
If a device is best operated when fed from a voltage source but the available signal is in the form of a current, a current-to-voltage converter will be required, one example being shown in Fig. 5. Current is fed to the summing junction of the operational amplifier which is a virtual earth so that current source sees an almost-zero load. Input current flows through R_1 producing an output voltage of $V_{out} = -R_1$ volts/amp. The only conversion error is due to the bias current of the operational amplifier which is algebraically summed with i_{in}. The output impedance is very low due to the use of almost 100% feedback.

Voltage-to-frequency conversion
Many voltage-to-frequency converters exist, the circuit complexity often being a guide to the degree of linearity and maximum operating frequency. Fig. 6 shows one form of V-to-f converter (a v.c.o.) suitable for use at frequencies below about 10kHz, each amplifier being of the current-differencing LM3900 type. Amplifier A_1 is connected as an integrator with A_2 acting as a Schmitt trigger which senses the output from A_1 and controls the state of Tr_1 which either shunts the input current through R_2 to ground, making V_{out1} run down linearly, or allows it to enter A_1 causing V_{out1} to rise linearly with $R_1 = 2R_2$. So V_{out1} is a triangular wave and V_{out2} a square wave having a frequency that is linearly dependent of R_1, C_1 and the threshold levels selected for the Schmitt trigger.

Frequency-to-voltage conversion
Diode-pump, transistor-pump and op-amp pump circuits are widely used for low-cost frequency to voltage conversion. Another circuit, using a single LM3900 quad current-differencing amplifier package, is the phase-locked loop shown in Fig. 7 which uses the v.c.o. of Fig. 6. Amplifier A_3 is in the LM3900 package used as a phase comparator having a pulse-width modulated output depending on the phase difference between V_{in} and V_{out2} of the v.c.o. Resistor R_8 and C_2 form a simple low-pass filter which makes the d.c. output vary in the range +V to +V/2 as the phase difference changes from 180° to 0°. This direct voltage controls the frequency of the v.c.o. and its lock range may be increased by using the fourth amplifier in the package as a d.c. amplifier between the filter and the integrator. Centre-frequency of the p.l.l. is about 3kHz with: R_1, R_3 1MΩ; R_2 510kΩ; R_4, R_8, R_9, 30kΩ; R_5, R_6 1.2MΩ; R_7 62kΩ; C_1 1nF; C_2 100nF; V = +4 to +36V.

Further reading
Graeme, J. G. & Tobey, G. E. Operational Amplifiers, chapter 6, McGraw-Hill, 1971.
Linear Applications—application notes AN20 and AN72, National Semiconductor, 1973.

Cross references
Set 3, cards 3, 5 & 10.
Ser 13, cards 1 & 6.

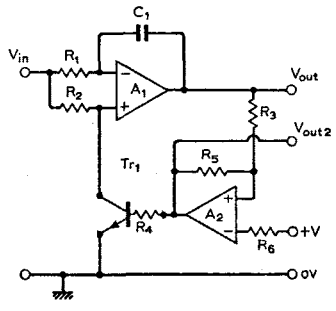


Fig. 6

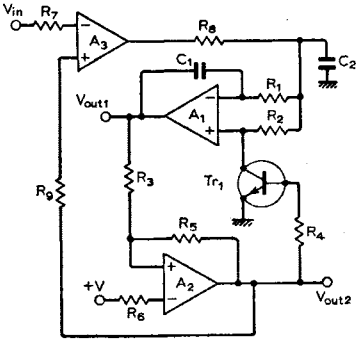


Fig. 7

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Pressure, temperature and moisture-sensitive alarms

Fig. 1

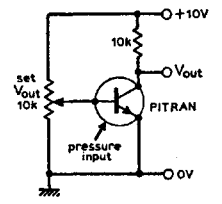
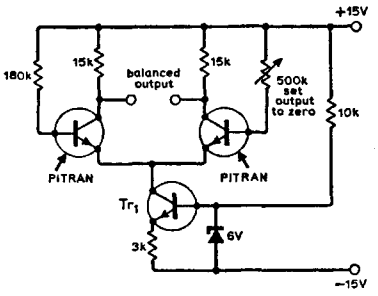


Fig. 2



Pressure-sensitive alarm

A pressure-sensitive alarm may be made using a specially-modified transistor known as the Pitran. It is a planar n-p-n transistor having a diaphragm mounted in the top of its metal can which is mechanically coupled to its base-emitter junction. When a pressure is applied to the diaphragm a reversible charge is produced in the transistor characteristics. The mechanical pressure input can be used to directly modulate the electrical output of the transistor which may be fed to the alarm circuitry, e.g., via a comparator or Schmitt trigger which switches state when the input pressure to the Pitran either exceeds or falls below some critical level. The Pitran may be connected as a single-ended-input single-ended-output Stage, as shown in Fig. 1 or as a differential-input balanced-output stage, Fig. 2

Conventional transistor circuit design techniques may be used for the Pitran stages. Linear output voltages of up to one-fifth of the total supply voltage are obtainable.

Temperature-sensitive alarm

Circuit Fig. 3, shows the input circuitry of an alarm which may be operated by the output signal from the operational amplifier when the temperature monitored by the probe transistor exceeds a pre-determined value. The temperature-sensing transistor is a low-cost n-p-n type that can produce a resolution of less than 1 deg C in a temperature range of 100 deg C. If the operating current of the probe transistor is made proportional to temperature, the non-linearity of its base-emitter voltage may be minimized, being less than 2mV in the temperature range −55 to +125°C. Zener diodes set the input voltage to 1.2V and this is applied through R_2 to fix the operating current of the probe transistor. Resistor R_4 may be adjusted to make amplifier's output zero at 0°C and R_5 is used to calibrate the output voltage to 100mV/deg C, or any other scaling factor, independently of the $V_{out}=0$ condition. R_1, R_3 12kΩ; R_2 3kΩ; R_4 5kΩ; R_5, R_6 100kΩ; D_1, D_2 LM113; Tr_1 2N2222; A_1 LM112; V±15V.

Moisture-sensitive alarm

A low-cost audible alarm which operates when the electrodes of the input sensor become damp due to increase in humidity, direct contact with water, rain or snow is shown in Fig. 4. The sensor is conveniently made from parallel-strip printed circuit board or commercial equivalent, so that increase in moisture at the strips produces a very small current to Tr_1 base via R_1 which forms a high-gain compound pair with Tr_2 which switches hard on. Transistors Tr_3 and Tr_4 form the audible alarm multivibrator, that acts as a load on the compound pair, having a repetition rate determined by the C_1R_3 time constant. A piercing note at about 2.5kHz is produced with R_1, R_2 100kΩ; R_3 1kΩ; C_1 10nF; Tr_1, Tr_2, Tr_4 ZTX300; Tr_3 OC71; LS 8-Ω loudspeaker; V+9V.

A flashing display with a rate of about 2Hz may be obtained by replacing the loudspeaker with a 6V, 60mA panel lamp and changing the values of R_2 to 470kΩ and C_1 to 2.2μF.

Further reading

Tingay, E. The Pitran—a new concept in pressure measurement, *International Marketing News*, p. 8, 1970.

Linear Applications—application notes AN31, AN56 and AN72, National Semiconductor, 1973.

Brown, F. Rain warning alarm, *Everyday Electronics*, pp. 208-11, 1972.

Fig. 3

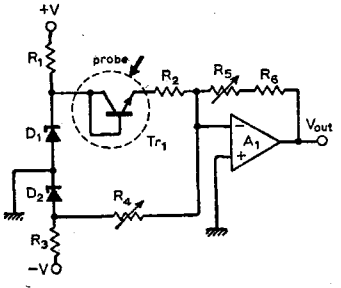
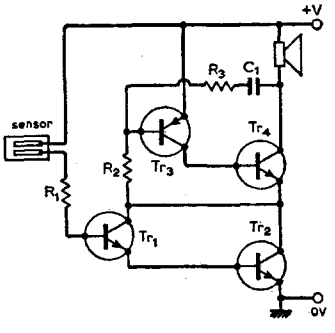
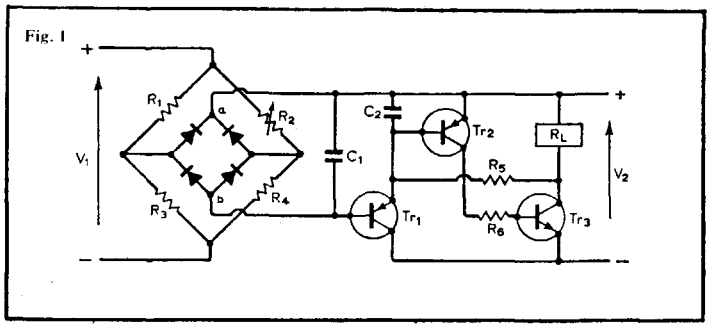


Fig. 4



Security, water level and automobile alarms

Fig. 1



Component values
R_1, R_4: 150kΩ
R_3: 200kΩ
R_2: 250kΩ variable
R_5: 27kΩ
R_6: 470Ω
C_1, C_2: 0.33μF
Tr_1, Tr_2: BC126
Tr_3: BFR41 or BFY52
Diodes 0A81
V_1: 18V
V_2: 9V

Circuit description
Component R_3 is the resistance in the search loop which if obtained using two 100kΩ resistors allows one to include switches either in series with the loop or in parallel with either resistor, or both. In the latter case changing a switch condition from open to closed in the parallel case and from closed to open in the series case can give rise to either a positive voltage or a negative voltage being applied to the diode bridge; the bridge is, of course, balanced initially. The diode bridge being a full wave rectifier will apply a negative V_{ba} to the following circuit in either case. The bridge resistors are large valued to minimize current drain from the battery but require that the following circuit have a large input resistance. Hence the buffer Tr_1 is employed.
When V_{ba} goes negative, Tr_1 and with it Tr_2, conducts. Transistor Tr_2 then drives Tr_3 which is a higher power device capable of drawing a relay coil to produce the warning signal. At the same time when Tr_3 conducts, the collector of Tr_3 goes negative and hence via positive feedback through R_5 the base of Tr_2 remains negative, even if V_{ba} is set back to zero. Hence, a latching action is obtained, which keeps the warning signal on. The warning signal will only be removed if the power supply is removed.
Capacitors C_1 and C_2 are required to prevent spurious pulses from triggering the alarm, in the case of C_1, and to prevent switching transients from triggering the alarm when the alarm is being reset, in the case of C_2.

Brake light monitor (Fig. 2.)
Both of the identical counter-wound coils are wound round the reed relay. Hence the relay switch will only close, giving a dashboard warning, if either of the brake lights fails either with an open circuit or short circuit.

Water level alarm
Fig. 3 circuit is designed to produce a note from the loudspeaker when the sensor input terminals are shorted. As such it can be used for many applications apart from suggested water level/rain alarm. When the input terminals are shorted base drive to Tr_1 via R_1 is obtained, and the supply voltage is switched to the unijunction relaxation oscillator comprising Tr_2, R_2, R_3 and C (card 4, series 3). A train of pulses of period mainly determined by the product R_2C is then presented to the base of Tr_3, thereby producing pulses of current through the loudspeaker. The loudspeaker alarm note can be altered by altering the product R_2C. Considerable effective output can be obtained by selecting the note to correspond to the resonant frequency of speaker.
In practice the alarm will sound for any resistance between zero and five megohms.
The quiescent current of the unit is of the order of nanoamps so that battery life is many months even if the unit is switched off. Provision to test the battery condition is made by switch position 2 which should cause Tr_1 to switch on the oscillator provided the battery is in good condition.
For water level sensing two conducting rods spaced an inch, or less, apart and positioned at the required level is all that is required.
For a rain alarm two rods separated by some blotting paper will suffice. When the blotting paper becomes wet contact between the rods is made, the alarm sounds and the washing is saved once more (provided the missus isn't away shopping).

Component changes
Resistor R_1 may be any value up to 5MΩ provided a true shorting of the sensor input terminals is obtainable.
The R_2C product is dictated by the pitch of the note required.
Resistor R_3 should be much less than R_2, e.g., $R_2/10$.

Further reading
Andrews, J. Security Alarm, *Practical Electronics*, 1973, p. 338.
Moorshead, H. Rain & Water Level Alarm, *Practical Electronics*, 1971, p. 820.
Morum, S. W. F., Brake Light Monitor, *Practical Electronics*, 1973, p. 588.

Component values
R_1: 100kΩ
R_2: 3.3kΩ
R_3: 270Ω
C: 0.5μF
Tr_1, Tr_3: 2N2926 (G)
Tr_2: 2N2646
LS: 8-Ω loudspeaker
Supply voltage: 9V

Fig. 2

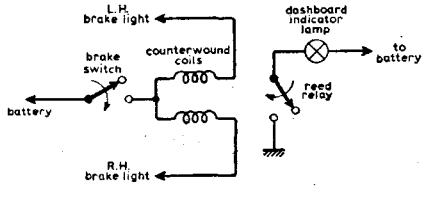
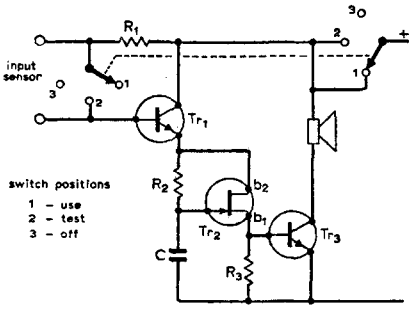
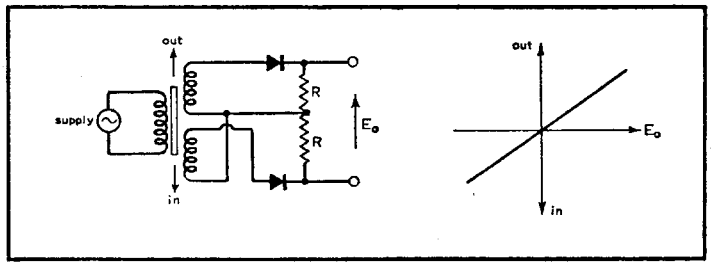


Fig. 3



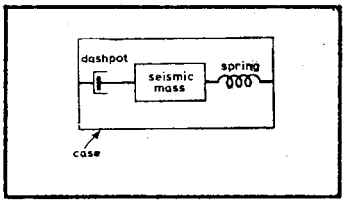
Electromechanical alarms

Electromechanical transducers are obtainable in a wide variety of types: they may be d.c. or a.c., resistive, reluctive or capacitive, contacting or non-contacting, analogue or digital, linear or angular, etc. Insofar as most alarm systems use a comparator (cross ref. 1) to compare the signal with a reference and as d.c. signals are easily compared we shall assume here that any a.c. systems are followed by signal conditioning equipment which includes a rectifier (cross ref. 2) of some sort so that the effective output is d.c.



Displacement Alarms
Circuit shows a reluctive displacement transducer, of the differential transformer type, followed by a demodulator to provide the d.c. output shown in graph. The core, which is shown in its zero output position, is attached to the member whose displacement is required. The core is generally made from high permeability ferromagnetic material so that flux linkages with and hence the e.m.fs of the secondary coils are highly dependent on the position of the core relative to the coils. Reluctive transducers generally have a displacement span of between 0.01 and 120in, in rectilinear form, and between 0.05 and 90° in angular form. As the induced e.m.fs are proportional to frequency, very sensitive systems can be made at high frequencies.
Capacitive transducers are used in situations where very small displacements have to be measured and/or non-contacting measurement has to be performed. Photoelectric/digital measurements (again non-contacting) are used when high accuracy is required, although fairly low cost versions can be constructed if accuracy is not essential.

Acceleration alarm
Acceleration transducers all have one feature in common, viz. the seismic mass, M. The basic acceleration transducer is shown below. The case of the system is attached to the body whose acceleration is required. Due to a constant acceleration the seismic mass exerts a force $M\alpha$ which in the steady state will stretch or compress the spring by an amount x where $M\alpha = Kx$, K being the spring constant. The dashpot simply provides damping whilst the mass is moving. If we know M and K then a measure of x gives a signal proportional to the acceleration. This can be done by any displacement transducer of suitable dimensions and sensitivity. Frequently, however, the spring arrangement is a leaf spring arrangement with strain gauges attached. The spring deflection gives rise to changes in resistance in the strain gauges which if connected in a Wheatstone bridge circuit gives a voltage proportional to the deflection and, hence, to the acceleration. As the Wheatstone bridge can be supplied from a d.c. source there is no need for rectifiers before feeding to a comparator. Strain gauge bridges usable up to 750Hz have been built.
For higher frequencies piezo-electric crystals replace the spring. The crystal produces a

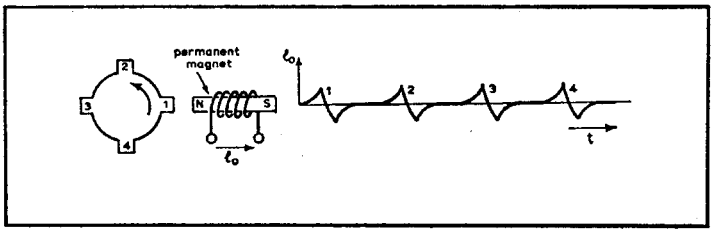


charge or voltage across its terminals when subjected to the stress of the seismic mass under acceleration. However, the output impedance of the crystal is large and amplifiers with an input impedance in excess of 500MΩ typically have to be used. Furthermore, the cable between the crystal and the amplifier requires to have low capacitance and to be free from friction induced noise. On the other hand very large accelerations (>100g) can be measured and they can be used over a large temperature range (570°C for a lead metaniobate crystal).

Further reading
H. N. Norton, Handbook of Transducers for Electronic Measuring Systems, Prentice-Hall.
Considine, Encyclopedia of Instrumentation and Control, McGraw-Hill.

Cross references
Set 2, Comparators and Schmitts.
Set 4, A.C. Measurements.
Set 13, card 4.

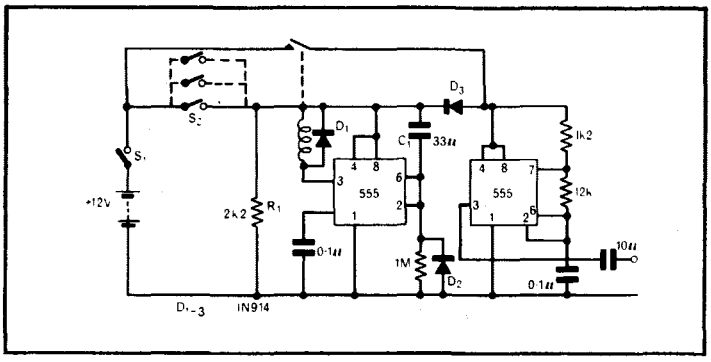
Velocity alarm
Linear velocity transducers are most commonly used in the vibrations field where the displacement of the member whose velocity is required is small. Essentially, they consist of a coil moving in a permanent magnetic field, the coil e.m.f. being proportional to the speed. As a large proportion of the speed producing systems are driven by motors one can generally obtain information on linear speed from a knowledge of angular speed. This can be obtained by various types of a.c. or d.c. tachometers, but with the increasing use of digital instrumentation, toothed rotor, photoelectric and similar systems are becoming increasingly common. Diagram shows basis of operation of the toothed rotor tachometer and the corresponding output when the rotor is rotated by the shaft of a motor. The output waveform is obtained because of the changing flux pattern caused by the changing magnetic circuit. If the output signal is fed to a zero crossing comparator (cross refs. 1, 3) or to a Schmitt trigger (cross ref. 1) one will then obtain a train of pulses, each pulse representing the passage of a rotor tooth past the permanent magnet. Obviously the pulse frequency is proportional to the shaft speed. If the train of pulses is then fed to a frequency-to-voltage converter a direct voltage proportional to shaft speed is obtained and this can be fed to a comparator to give an alarm if it exceeds a pre-determined level. Because the number of teeth on the toothed rotor can easily be varied, the range of speeds measurable by this technique is extremely large. Further, the rotor can easily be constructed in any workshop, no great precision being required for many applications. Bolt heads on a coupling between two shafts often suffice as the toothed rotor.



wireless world circard

Set 13: Alarm Circuits Up-date

1. The ability of the 555 timer to act as a monostable or astable and to deliver sufficient power to drive a loudspeaker directly is put to use in this burglar alarm. Switch S_1 is closed arming the circuit, with S_2 consisting of a number of normally-closed switches each detecting an entry point. If any of these switches is allowed to close by an opened window, etc. the relay is activated and power is applied to both monostable and astable. The audio output can be accompanied by a visual output via a second relay contact. The circuit



remains latched by the relay throughout the monostable delay, further variation in S_2 having no effect. The alarm ceases at the end of the selected delay (~12s is given in the source article) regardless of S_2, but is re-triggerable once S_2 has been opened and the stored charge in C_1 has been dissipated through D_2, R_1, i.e. the alarm operates for only one cycle. No standby current flows as the contacts of S_2 are normally open. Frequency of oscillation of the astable section is around 1kHz and transformer coupling to a low resistance loudspeaker is suggested in the article.

Reference

Long, J. D. Burglar alarm is effective, yet simple and inexpensive, *EDN*, 1974, Dec. 20, pp. 50/1.

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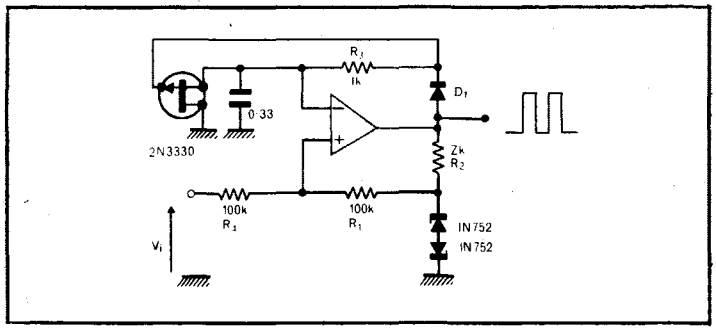
2. Positive feedback around an operational amplifier may be used to provide either astable or Schmitt characteristics. This novel circuit combines both while needing only one operational amplifier. When the op-amp output is low D_1 is reverse biased and R_3 provides the f.e.t. with a zero gate-source voltage. Hence the f.e.t. shorts out the capacitor grounding the inverting input. As the input voltage increases, it overcomes the effect of the negative voltage across the zeners, raising the non-inverting input above



zero. The op-amp output swings positive, reverse-biasing the f.e.t. gate source and allowing the capacitor to charge positively. This continues until the inverting input rises to equal the now positive potential on the non inverting input. At this point the op-amp output switches back to its negative state and the capacitor discharges, with the cycle recommencing. The reference article gives equations representing the circuit performance and indicates that 0.1% stability of trip-point is achievable, though the frequency of oscillation is determined only to within about 30%.

Reference

Graeme, J. Voltage comparator circuit gives audio alarm when tripped, *Electronic Design*, 1975, May 10, p. 148.

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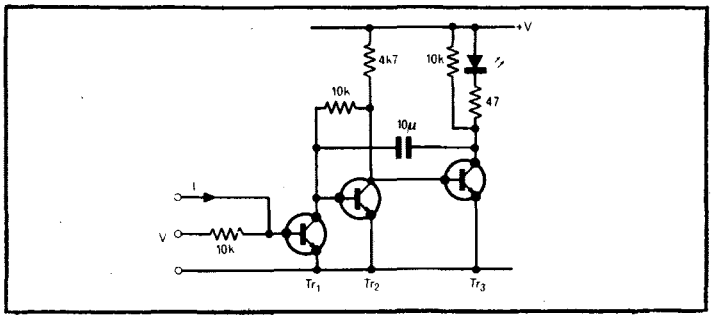
3. The circuit is an astable gated by a single transistor that can be driven from a small positive current or from a low voltage (>0.6V), including the output of t.t.l., c.m.o.s. etc. Alternatively Tr_1 can be replaced by an open-collector t.t.l. gate. The novel property of this astable that it drives an l.e.d. from a low voltage supply with the l.e.d. permanently on for input level high and flashing at, say, 1–10Hz depending on choice of



C for input level low. This allows a single l.e.d. to act as the on-off indicator for a battery instrument as a supply voltage of 2V is sufficient to initiate conduction; the same l.e.d. acts as the visual indicator of a fault condition if that fault is converted into a low voltage/current to drive Tr_1. In the quiescent state the l.e.d. current may be typically 20mA. The three transistors may be any general purpose silicon devices including those from such multi-transistor packages as CA3046, CA3086, etc. The other two transistors in such a case are usable as part of a Schmitt trigger or amplifier stage.

wireless world circard

Set 14: Digital counters

This set was the first in the revised format for Circards. But for this book, we re-set the first three cards so that they would conform to the rest. The four-column presentation allows greater flexibility of layout and we hope you agree that the "unjustified" type-setting makes for greater readability, with its equal word-spacing and jagged right-hand edge. We took this opportunity to up-date the title area and to rename "series" with the more logical "set".
Another excellent summary of the subject precedes this set of circuits. It covers all the essential points about the use of bistable circuits as counters, starting by setting out the different kinds (JK, RS, D and T, discussed in more detail on glossary card 12), defining ripple and parallel counters, design using Karnaugh maps, and concluding with sequence generators. In digital parlance notice that bistable circuits are referred to as flip-flops, whereas originally this term referred to monostable circuits, the words flip and flop indicating an unstable state and a stable state. (Anyone for flip-flip for astables and flop-flop for bistables?)
Content of the cards calls for little comment. Card 12 is useful for newcomers, listing various binary codes against decimal number, and in describing the different kinds of "flip-flops". It also shows connections for RS and JK types to give D and T functions.

An introduction to digital counters

A digital counter comprises an interconnection of bistable or two-state memory circuits or, colloquially, flip-flops. The counter embraces those circuits which accumulate pulses according to a specific code as they appear at the input, frequency dividers, sequence generators and pulse waveform generators. The application requirement will generally determine how the collection of flip-flops is identified, but in this article the generic name of counter will be used.

The basic flip-flop has one or two control inputs, and two outputs termed Q and $\bar{Q}$ (not -Q), where $\bar{Q}$ represents the opposite state of Q. The logic state of these outputs may be termed set or reset, high or low, 1 or 0, and the change of state may occur on 0 to 1 or 1 to 0 transitions at the input, depending on the type used. The varieties of flip-flops used in counters are normally described by the control inputs and are termed D-type, T-type, RS and JK. The triggering input, called the clock-pulse input, ensures that a change of state will only take place on the occurrence of a pulse at the clock-input. Other facilities that may be available are preset and clear inputs which allow a flip-flop to be set (Q = 1) or reset (Q = 0), independently of the control inputs. Typical symbols for these flip-flops are shown in Fig. 1. Other variations include operation by positive or negative logic, triggering on positive or negative pulse edges or a combination of these as in master-slave flip-flops.

A basic RS flip-flop using NAND gates is shown in Fig. 2. To represent the dependence of the Q output on the control inputs when a clock pulse occurs, a truth-table is used to demonstrate the state of Q at the nth clock pulse (Q_n), and after the next clock pulse (Q_{n+1})—Fig. 3. For example, if S and R are both at logic zero when a clock pulse occurs, the output Q will not change state, but remain as it was before the clock pulse. However, if S = 1, R = 0, then Q becomes logic 1, i.e. if it was previously logic 0 a change of state occurs, and if it was logic 1, it remains so.

The indeterminate state of Q for the condition that R = S = 1 exists because of a race condition between gates and is one disadvantage of this flip-flop—such a condition must be avoided. The JK flip-flop, however, does not have this disadvantage—all output conditions are predictable, as shown in Fig. 4. The last combination of J = K = 1 permits a useful toggle action in which the output changes state on the occurrence of every clock pulse.

Counters are generally classified as asynchronous or synchronous. The basic asynchronous circuit is implemented with cascaded toggle flip-flops, where the output of a previous flip-flop is the clock-input for the next in sequence. Alternatively, the drive inputs may come from Boolean combinations of other outputs. In either case, a disadvantage is that each flip-flop changes state at a different time in a sequence. For each flip-flop a propagation delay exists between the occurrence of a trigger pulse and the next state of the output, and this delay "ripples-through" the counter. This restricts the maximum operational speed of the counter, since the maximum ripple-through delay must be less than the time between input pulses.

In integrated circuit technology, these counters have the advantage that each flip-flop operates at half the frequency of the preceding one. This allows a trade-off in high-speed (high-power dissipation) circuits to be used in the first stage, with lower speed (low-power) configurations being used in later stages. The maximum count (including zero) of a counter containing n flip-flops is 2^n, feedforward or feedback techniques allowing counts less than this to be achieved. The number of distinguishable states through which the counter cycles is known as the modulus of the counter, and this may be fixed when implemented with individual flip-flops, but some m.s.i. packages are available that permit variation of the modulus by a simple connection change or simple gating. If the outputs of ripple-counters are to be

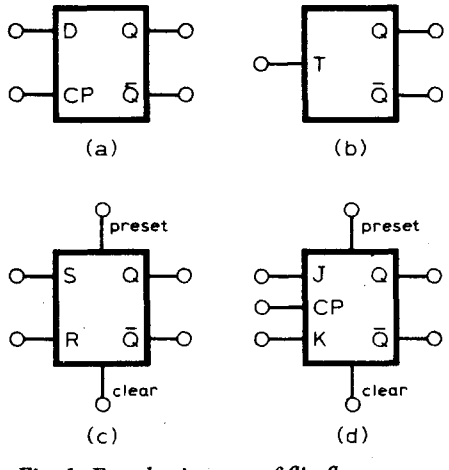


Fig. 1. Four basic types of flip-flop.

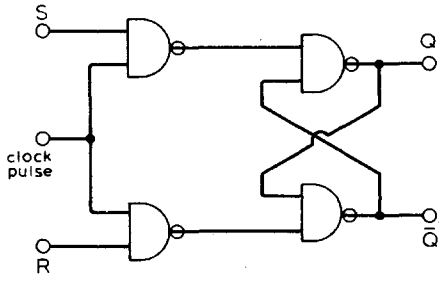


Fig. 2. Nand-gate RS flip-flop.

S	R	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	undefined

Fig. 3. Truth table for Fig. 2.

J	K	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	$\bar{Q}_n$

Fig. 4. Truth table for JK flip-flop.

decoded, care must be taken to ensure that the decoder network is enabled only when it is certain that all intermediate state changes have occurred.

The disadvantage of the asynchronous counter is avoided by the synchronous or parallel counter, in which all flip-flops change state in synchronism with a common clock-pulse. The speed of operation is limited by one flip-flop delay and that of any gating necessary, and these will depend on the type of hardware being used, e.g. c.m.o.s., t.t.l., e.c.l. Recent Schottky synchronous counter packages have internal circuitry which eliminates all external gating, and counting speeds up to 70MHz are claimed, and e.c.l. packages are available for speeds up to 110MHz.

Any sequence may be generated using individual JK flip-flops and associated gating. The design is more complicated than the asynchronous types, but one technique simplifies the design problem using Karnaugh maps.[1]

The map is a two-dimensional representation of all possible combinations of a number of variables, where each square is one unique combination and adjacent squares are identical except for one variable. The rows and columns are arranged in accordance with the Gray code representation of decimal numbers, in which only one bit changes as we progress through adjacent numbers (Fig. 5). A Karnaugh map for four variables, A, B, C and D, is shown in Fig. 6, where a 1 in a square means the existence of logical "ANDed" variables, identified by the row and column common to that square.

The 1 squares are connected by the logical OR function, and the Boolean expression represented by Fig. 6 is $F = \bar{A}.B.\bar{C}.D + A.B.\bar{C}.D + \bar{A}.B.C.D + A.B.C.D$. A 0 in a square indicates that this particular combination does not exist. The advantage of the map is that minimization of the Boolean expression is simplified by being able to group adjacent squares in pairs, fours, etc. Two squares can be combined to eliminate one variable, and these two squares can be combined with another two adjacent squares to eliminate one more variable. The four squares may be looped as shown, because of their adjacency, thus A and C become redundant as both states of each are included in these squares reducing the function to $F = B.D$. This can be confirmed by a Boolean minimization. Note that adjacency of squares exists at the extreme ends of horizontal rows, and at the extreme ends of vertical columns.

A design of a modulo-6 Johnson counter is considered as an example of the technique. The maximum modulus of an m-stage Johnson counter is $2m$, hence a minimum of three flip-flops is required. It is assumed that the outputs are taken from the Q output of the flip-flops designated A, B and C, and the map is used to minimize the gating necessary to obtain the prescribed sequence Fig. 8. As all possible combinations of the variables are not used, the "can't happen" or redundant states are denoted by a combination of one and zero (ⓘ) in the state table (Fig. 9) because the states are not specified and may be made 1 or 0 at will. In this case they will be considered as 1s. The state table shows the desired outputs at A, B and C on the occurrence of the numbered clock pulse, where 0 and 6 are equivalent, i.e. the 6th pulse resets the counter to zero. It will be assumed that the counter commences from the zero state.

The design technique requires the preparation of a Karnaugh map for the J and K input of each flip-flop to determine the control levels required at each input for every step of the sequence, by deriving a minimal Boolean expression for each map, though as these are derived independently the circuit may not necessarily be minimal. This then determines the internal gating required.

An excitation table for the JK flip-flop is derived from the JK truth-table shown earlier. This table (Fig. 7) shows the necessary J and K inputs to either hold the flip-flop in a 1 condition or a 0 con-

DECIMAL	GRAY-CODE			
	A	B	C	D
0	0	0	0	0
1	0	0	0	1
2	0	0	1	1
3	0	0	1	0
4	0	1	1	0
5	0	1	1	1
6	0	1	0	1
7	0	1	0	0

Fig. 5. Gray code for decimal numbers.

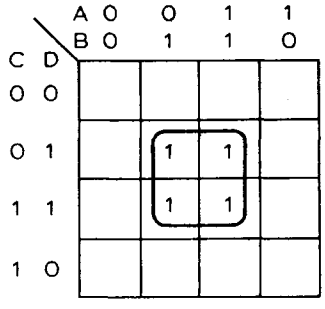


Fig. 6. Karnaugh map for four variables.

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Fig. 7. Excitation table for JK flip-flop.

C	B	A	input pulse no.1
0	0	0	0
0	0	1	1
0	1	1	2
1	1	1	3
1	1	0	4
1	0	0	5
0	0	0	6

Fig. 8. Johnson counter sequence.

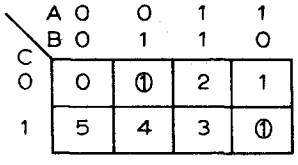
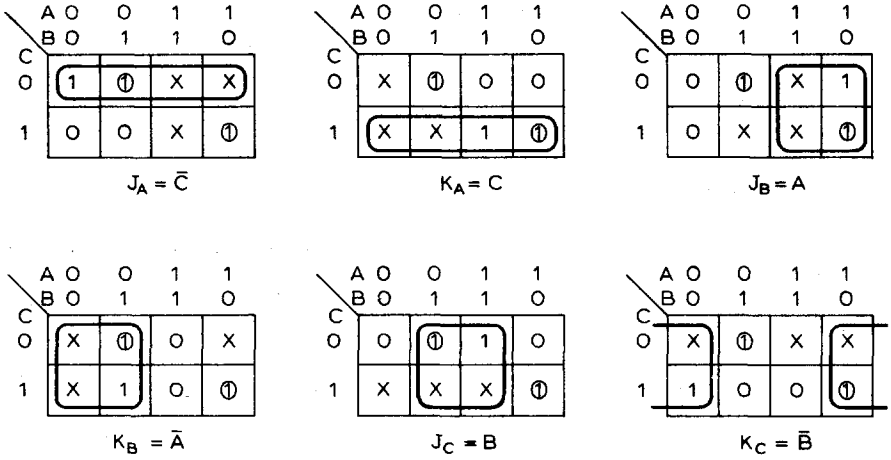


Fig. 9. State table for Fig. 8.



dition, or to cause a 1 to 0 or 0 to 1 transition, all on the occurrence of an input clock-pulse. The X indicates that it does not matter what that particular J or K state is, provided the other control input is in the correct state.

For example, if it is assumed that Q = 1, and a transition to logic 0 is required on the occurrence of a clock-pulse, then from the truth-table either J = 0, K = 1, or J = 1, K = 1 will cause this change, i.e. provided K = 1, J may be either 0 or 1. As each input pulse occurs, the flip-flops should change in accordance with the truth-table of Fig. 8. The steps involved in filling the JK maps are as follows.

The can't-happen conditions of the state-table are transferred to equivalent squares on the separate J and K maps. Consider the J_A and K_A maps. On the occurrence of the first pulse, Q_A should hold at logic 1, hence an X is put in the J_A map square representing pulse no. 1, and a 0 in the K_A map square. This is repeated for pulse no. 2. At pulse no. 3 a 1 to 0 transition is required, hence an X is put in J_A map square for pulse no. 3, and a 1 in K_A map. A 0 is maintained for pulse no. 4, hence a 0 in J_A and X in the K_A square for pulse no. 4 is necessary. This is continued until all squares for each map are filled.

As an example of the minimization, notice that symbols 0 or X may be 1, hence a loop of four adjacent squares is available in the J_A map, i.e. the minimal solution for J_A is given by $\overline{C}$. Similar loops of four are obtained for each of the other maps, the circuit being implemented in Fig. 11. No external gates are required in this circuit, because the complemented outputs are already available from each flip-flop.

Common arrangements using this technique are b.c.d. counters, decade counters, up-down counters, though some are also available in m.s.i. packages.

The implementation of Fig. 11 has been described as a modulo-6 Johnson ring counter. However, examination of Fig. 8 shows that each output Q_A, Q_B and Q_C has one pulse for every six of the input so that the device could be regarded as a divide-by-six frequency divider. Most frequency dividers, on the other hand, allow one to divide by an arbitrary number so it cannot be regarded as a very good frequency divider.

The device of Fig. 11 can also be regarded as a sequence generator, in that, given an input pulse sequence, one obtains a different output pulse sequence—admittedly not a very interesting one.

There is an infinite number of sequence generators that one could build but of particular interest are those which produce so-called maximal length binary sequences (M-sequences). Used in many areas, such as data communication system identification and correlation methods, M-sequences are generated by synthronous shift registers with feedback from various stages being used to determine the next state to be fed in. Feedback complexity is not proportional to the register length and very long sequences can be generated by very simple feedback arrangements. Feedback is performed by modulo-2 addition, i.e. via exclusive-OR gates (Fig. 12).

The properties of these sequences depend on the clock rate, f_c, and on the number of stages in the shift register, n, but all of the sequences possess to some degree properties close to those of band-limited white noise. (Hence the name pseudo-random binary sequences or p.r.b.s.) The signal bandwidth is given approximately by $f_c/3$ and the greater the value of n the more closely do the properties resemble those of random noise. The sequences are not in fact random because they are binary in nature and because they are cyclic, the cycle length being $2^n - 1$ clock periods. The binary nature of the signals is easily removed by passing them through simple first- or second-order filters so that the signal becomes continuous and has a probability density function which is close to Gaussian. The cyclic nature of the signal is in fact one of the advantages of M-sequence and is one of the non-random features one would wish to retain. This is because experiments can be repeated for checking purposes over a cycle length without the statistical difficulties of genuine random noise. From this point of view it is therefore desirable to limit n.

Design is greatly facilitated by tables which indicate what feedback paths are necessary to produce an M-sequence of given length.[2] The problem comes down to one of choice of f_c and of n for the particular application in mind.

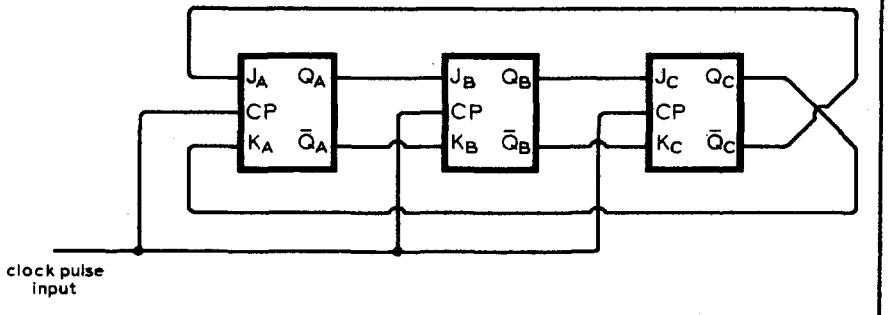


Fig. 11. Implementation of modulo-6 Johnson ring counter.

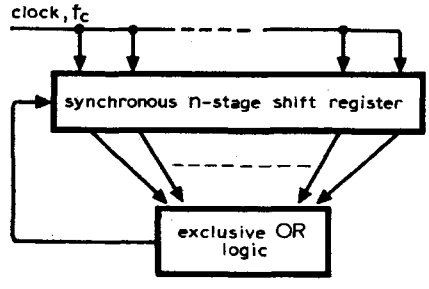


Fig. 12. M-sequence generator using exclusive-OR gates.

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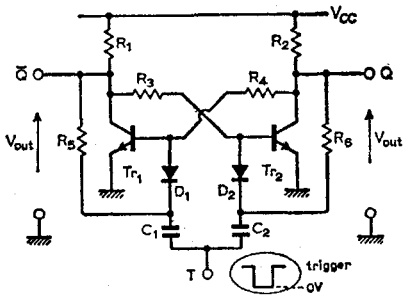
Basic binary counters



Circuit operation

The bistable circuit is a T-type "flip-flop" in which the output changes state for a negative-going transition at the trigger-input. If the base-drive current is arranged so that Tr_2 is in saturation, its collector voltage will be about 0.2V. This is too low to forward-bias the base-emitter junction of Tr_1, about 0.7V, and hence Tr_1 will be off. This means its collector-emitter voltage is high, depending on R_1 and R_3, and the base-drive current for Tr_2 flows through R_1 and R_3. Hence the terminals identified (arbitrarily) as Q and $\bar{Q}$ are low and high respectively (0 and 1 for binary coding).

When the trigger input is high, the circuit is in a stable state. When the trigger input is driven near ground the negative-going pulse-edge is steered to Tr_2 base as D_2 is forward-biased. The anode of D_1 is approximately at $V_{CE(sat)}$ and because its cathode is connected to a high potential via R_5 it is reverse-biased. Therefore Tr_2 collector current is reduced, causing a rise in its collector voltage, increasing base-drive current to Tr_1. This causes Tr_1 collector voltage to drop and Tr_2 base current decreases causing a further increase in Tr_2 collector voltage. The process continues until the other stable state, Tr_1 conducting and Tr_2 off, is sustained. The next negative-going trigger pulse resets the circuit to its previous state. It produces one output pulse for every two trigger pulses.

The interconnection of these bistable circuits to give a binary ripple counter demands that the Q output of a previous flip-flop is connected to the trigger (or T−) input of the next flip-flop. This gives a natural count of 2^n where n is the number of stages, and 2^n is the number of states through which the counter progresses.

Circuit modification

Range of R_5, R_6: 4.7k to 47kΩ
Frequency variation: 150 to 30kHz
Range of C_1, C_2: 330 to 3300pF
Frequency variation: 140 to 90kHz
Increase turn-on speed with capacitors across resistors R_3 and R_4 typically 5 to 20% of C_1, C_2.
Increased frequency of operation possible with additional diodes connected across R_5, R_6 (anode to collector).
High-speed transistors BSX19, BSX20 permit counting speeds up to 10MHz.

IC binary counter

The ripple binary counter is commonly implemented with integrated circuits using J-K flip-flops e.g. the SN7493 is a 4-bit binary counter within one package allowing a typical count rate up to 18MHz for d.c. supply +5V, and a typical load of 400Ω and 15pF.

Synchronous binary counters using dual J-K master-slave flip-flops are shown above. In all cases decouple the power supply—typically 0.01μF per package.

In Fig M1, since $J_A=K_A=1$ (high), the first flip-flop acts as a toggle. The second flip-flop is triggered by alternate clock pulses the third flip-flop is gated by the Q_A and Q_B outputs and only changes when $Q_A=Q_B=1$. Similarly, the last flip-flop only changes state when $Q_A=Q_B=Q_C=1$. This counter has the disadvantage of long counter chains requiring AND gates with a large fan-in.

The situation is avoided with the counter of Fig. M2 where the fan-in is limited to two per gate. However this is a slower counter because the gated-pulses must propagate down the AND gates before the next clock-pulse arrives. For both these counters, use the SN7473 dual J-K flip-flop package.

Another example (Fig. M3) employs the SN7472 which has effectively 3-input AND gates for each J and K input, within the package, which eliminate the need for external gates.

Typical data

Single bistable
Vcc: +12V
Tr_1, Tr_2: BC108
R_1, R_2: 3.3kΩ ±10%
R_3, R_4: 8.2kΩ ±10%
R_5, R_6: 6.8kΩ ±10%
C_1, C_2: 800pF
D_1, D_2: PS101
Frequency 100kHz typically
Trigger input ≈ 4V
Trigger input width > 1μs

Further reading

Electronic Counting, Mullard, 1967.
Designing with TTL Integrated Circuits (Texas), McGraw-Hill 1971.
Counter delay slashed in half with interconnection scheme, *Electronic Design* 13, 1972.

Cross references

Series 14, cards 4, 6 & 12.

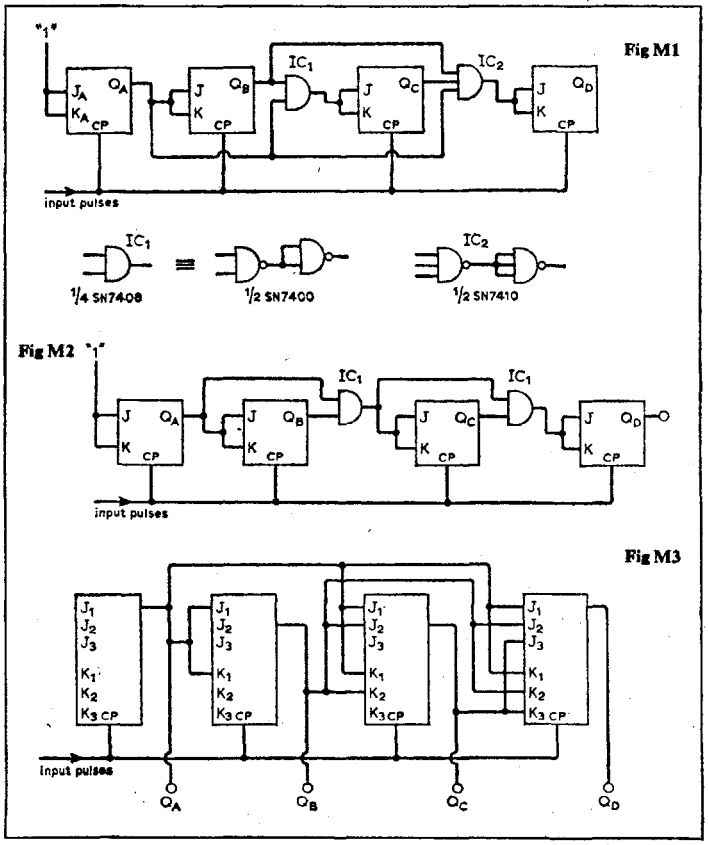
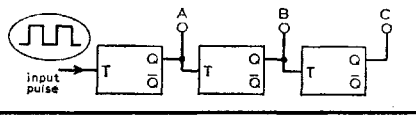


Fig M1

Fig M2

Fig M3



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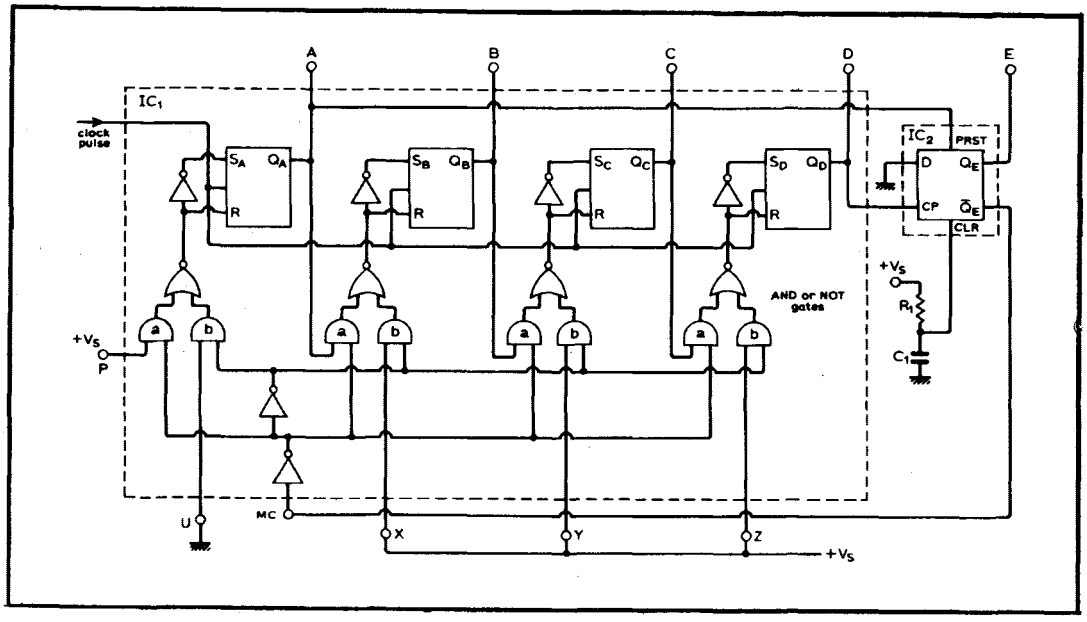
One out of n ring counter



Typical data
IC_1: SN7495
IC_2: ½SN7474
V_S: +5V
R_1: 1kΩ
C_1: 47pF

Circuit description

Component IC_1 is a 4-bit shift left or right register, comprising master-slave R-S flip-flops, with a parallel-loading capability via the AND-OR-NOT gates at terminals U, X, Y and Z. This is conditioned by mode-centre terminal MC equal to binary one. When MC=0, information transfers serially through the register, the clock-pulses being applied to the commoned right-shift and left-shift inputs (not shown). When used in conjunction with a positive-edge triggered flip-flop, IC_2, this arrangement provides a self-starting, self-priming ring-counter for circulating a zero.

Clock pulse No.	Q_A	Q_B	Q_C	Q_D	Q_E
1	0	1	1	1	1
2	1	0	1	1	1
3	1	1	0	1	1
4	1	1	1	0	1
5	1	1	1	1	0
6	0	1	1	1	1

When the supply V_s is switched on, the clear-input of IC_1 is pulled down to ground by CR network, setting Q_E= 0, and $\bar{Q}_E$ = 1. Hence MC = 1, and the counter is in the parallel mode. The left-hand AND gates are inhibited, and the voltage levels at inputs U, X, Y and Z are transferred to the set inputs, S_A to S_D, of IC_1. In master-slave flip-flops, the binary level at the set terminal is transferred to the Q terminal on the occurrence of the negative-going edge of the clock-pulse.

After the first clock-pulse, Q_A= 0, Q_B to Q_D= 1. Also, Q_A is connected to the preset input of IC_1, and hence Q_E is set to binary one. Hence $\bar{Q}_E$= 0, and the counter is switched to a serial-mode. The right-hand AND gates are now inhibited. Therefore S_A= 1, the low level of Q_A is gated to S_B, Q_B to S_C, and Q_C to S_D. After the second clock-pulse, the Q outputs are as shown in the truth table, the sequence continuing with each clock-pulse shifting the zero through the register. At the 5th pulse, Q_D changes from 0 to 1, and this positive-edge triggers IC_2. Q_E resets to zero, $\bar{Q}_E$= 1, and the parallel-mode is again entered. The 6th clock-pulse reloads the levels at U, X, Y and Z terminals and the cycle repeats.

Circuit modifications

- The number of bits can be extended by cascading IC_1 packages as in Fig. M1.
- Circulate a 1 by inverting the counter outputs with t.t.l. NAND gates (SN7400) or c.m.o.s. hex buffers (CD4049).
- A 4-bit self-starting and correcting counter (Fig. M2) for circulating 1 uses J-K flip-flops and feedback via an AND gate. The flip-flops are connected as a shift register, where the state of Q_A is passed to Q_B, and Q_B to Q_C, etc. with each clock pulse. In general, for self-correcting, and when using J-K flip-flops, J_A should be the Boolean product of the complements of all but the first and last stages.

Further reading

Self-correcting ring counter requires no external gates, *Electronic Design* 9, 1973, p.138.
Malmstadt and Enke, Digital Electronics for Scientists, Benjamin, 1969.
Texas Instruments application report CA102, Electronic Counting, Mullard, 1967.

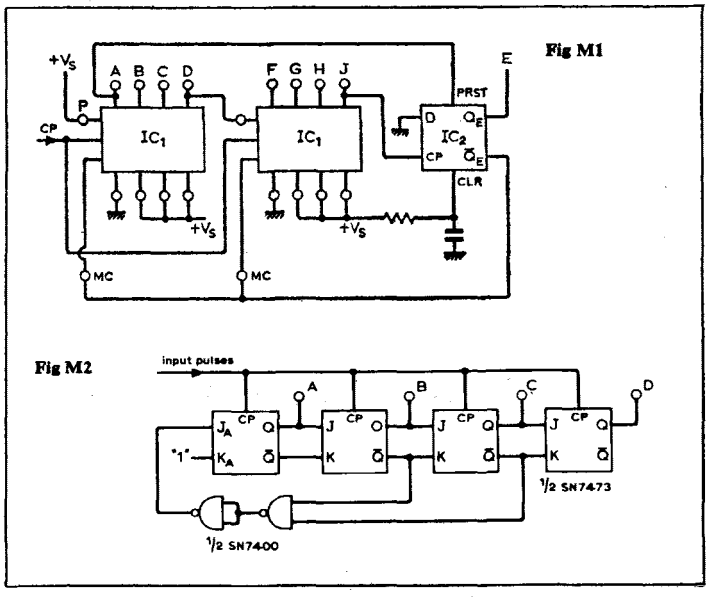
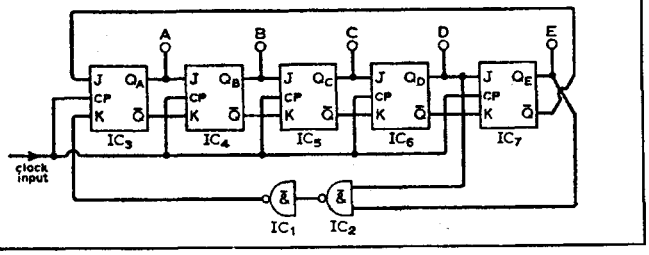


Fig M1

Fig M2

Johnson counters



Typical data
Supply: 4.75 to 5.25V
IC_1, IC_2: ½ SN7400
IC_3, IC_4: ½ SN7473
Min. clock width: 20ns
(between 50% levels)
Typical pulse height: 3.5 to 4.5V

Circuit description

This counter, also called a switch-tail ring counter, allows $2n$ counts where n is the number of cascaded flip-flops. It is a synchronous counter in that changes at the Q outputs only take place on the occurrence of a clock-pulse. If $J = \overline{K}$, the J input condition is transferred to the related Q output on the negative edge of the clock pulse, when the flip-flops are master-slave types. The above circuit has ten different states, the feedback via the AND gate causing self-correction after a few steps, should illegitimate states occur.

Consider all Q outputs to be in the 0 state. Hence $J_A = 1$ because $\overline{Q}_E = 1$. On the occurrence of the first clock pulse, the counter will load according to the truth-table. At each subsequent pulse, "1"s will be fed through the counter from the left until $Q_D = Q_E = 1$. It follows then that since $J_A = 0$, $K_A = 1$, that Q_A becomes 0 at the 6th clock-pulse. Zeros are subsequently transferred through the register according to the truth-table, until $Q_D = Q_E = 0$, then $J_A = 1$, $K_A = 0$, and the cycle repeats.

In general, when there are n stages in the counter, feedback via an AND gate from the last x stages, where x is the next larger integer to $n/3$ provides self-correction for n up to 25.

Decoding of each state is obtained using AND gates, as a unique pair exists for each state. These output pairs are indicated in the truth-table, and are applied to the gate inputs (these can be ½×SN7400 in series).

Circuit modifications

The same output sequence is obtained from dual D-type flip-flops (SN7474) as Fig. M1. In general, assuming up to eight JK flip-flops are employed, A, B, C, D, E, F, G, H, then the

clock pulse	A	B	C	D	E	decoding outputs
	0	0	0	0	0	
1	1	0	0	0	0	$A\overline{B}$
2	1	1	0	0	0	$B\overline{C}$
3	1	1	1	0	0	$C\overline{D}$
4	1	1	1	1	0	$D\overline{E}$
5	1	1	1	1	1	AE
6	0	1	1	1	1	$\overline{A}B$
7	0	0	1	1	1	$\overline{B}C$
8	0	0	0	1	1	$\overline{C}D$
9	0	0	0	0	1	$\overline{D}E$
10	0	0	0	0	0	$\overline{A}\overline{E}$

feedback functions for an even cyclic pattern are

$J_A = \overline{C}$, $K_A = B.C$	(6)
$J_A = \overline{D}$, $K_A = C.D$	(8)
$J_A = \overline{E}$, $K_A = D.E$	(10)
$J_A = \overline{F}$, $K_A = E.F$	(12)
$J_A = \overline{G}$, $K_A = E.F.G$	(14)
$J_A = \overline{H}$, $K_A = F.G.H$	(16)

An odd sequence $(2N\text{-}1)$ counter can be implemented by bypassing the all "1"s state of the normal Johnson sequence i.e. the last two bits of the 111 . . . 10 state is detected, and the gating arranged to the first flip-flop so that the next state is 011 . . . 11. (Texas ref.).

Other odd sequence counters can be implemented by J-K flip-flops without extra gating and are shown in Figs. M2 & 3. Fig. M2 uses feedforward gating and Fig. M3, feedback. In general, any $2n$ counter can be made $2n\text{-}1$ by obtaining the K input of the first-flop from the second last Q output (cf. Fig. M3).

Further reading

Davies, A. C., Design of feedback shift registers and other synchronous counters, *Radio and Electronic Engineer*, April 1969.

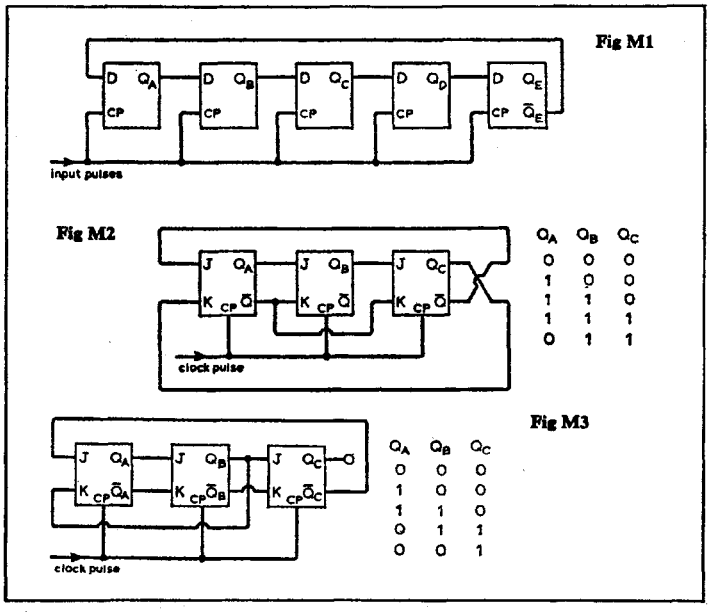
Texas Instruments application report CA102.

Kohonen, T. Digital circuits and devices, Prentice-Hall, 1972.

Malvino, A. P. & Leach, D. P., Digital principles and applications, McGraw-Hill, 1969.

Cross references

Series 14, cards 9 & 12.



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Reversible counters—1

Circuit description

Up-down or reversible counters alter their mode of counting under electrical control. The circuits shown are binary up-down counters in which the count direction is controlled by steering logic and either the flip-flop Q outputs are used for toggling subsequent flip-flops (UP) or the $\bar{Q}$ outputs are used when the Q outputs are inhibited. Fig. 1 is an asynchronous type and Fig. 2, a synchronous counter.

The equation for the output of the selector gate is, for example, $AX + \bar{A}\bar{X}$, the gating usually being implemented by the NAND gate interconnection of Fig. 3. When a logic 1 is applied to the up-down control line, the gates connected to $\bar{Q}$ are inhibited, and the flip-flops change state when their clock inputs undergo a 1 to 0 transition i.e. the Q outputs will change according to the normal binary sequence. If the control line becomes 0, the Q outputs will reverse sequence. To avoid a false triggering condition, the count/inhibit line must be 0 when the controlling function is altered from up to down or vice-versa.

In the synchronous counter of Fig. 2 such a condition is avoided. Each flip-flop will change state only if previous Q outputs are in the 1 state (when X = 1) i.e. counting up, and for a down count ($\bar{X}$ = 1), all the less significant Q outputs must be at 0 for a flip-flop to change on a 1 to 0 transition.

IC_5 (CD4029A) is a presettable synchronous up/down counter providing either a binary or b-c.d. decade sequence with appropriate mode control, i.e.
binary: B/D = 1
Decade: B/D = 0
Up: U/D = 1
Down: U/D = 0
Preset: PE = 1
J1 to J4 = 1 or 0
Parallel clocking allows cascading (Fig. 4)
Where separate "clock up" and "clock down" clock pulses are available the circuit of Fig. 5 provides a simple interface to the up/down "clock" inputs.

Fig 1

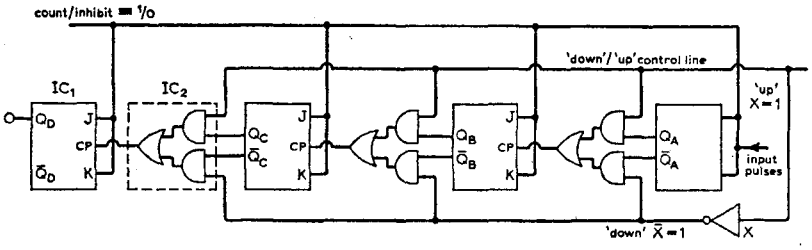


Fig 2

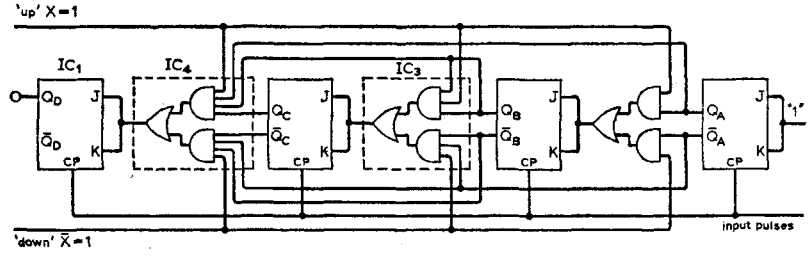
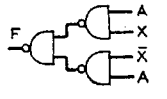


Fig 3



Integrated circuits
IC_1: SN7473
IC_2: ¾ × SN7400
IC_3: SN7410
IC_4: SN7420 and ¼ × SN7400
IC_5: CD4029A
Supply: 4.75 to 5.25V

Synchronous up-down b.c.d. and binary counters are available in packages SN74190 and SN74191 respectively.

Cross references
Series 14, cards 5 & 12.

Fig 4

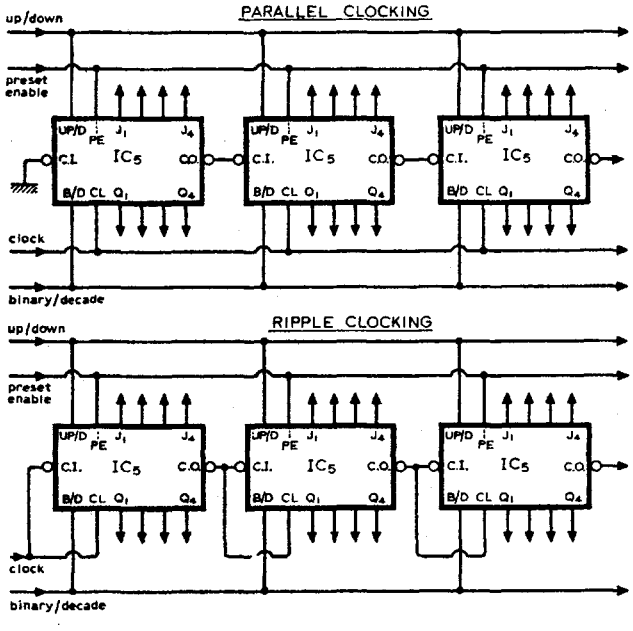
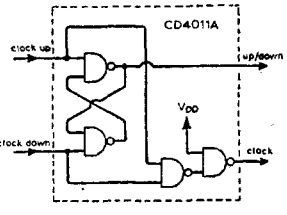


Fig 5



Reversible counters—2

The AND-OR-NOT gates provide gating control for the up/down mode. The Boolean expression for the P output is $\overline{(UP)\bar{Q}_D + (DWN)Q_B}$. If the control line = 0, then $P = Q_D = 0$. Hence $J_A = 1$, $K_A = 0$, and on the occurrence of the first clock pulse $Q_A = 1$. The counter would subsequently count up in Johnson code. However, if for example, the counter state is 1110 and control = 1, only the S output causes a change to make $Q_C = 0$ on the next pulse, and thus count down.

Circuit of Fig. 2 uses a 4-bit parallel adder and four D-type flip-flops. Consider the sum outputs $\Sigma_4 - \Sigma_1$ show 7_{10} i.e. 0111_2, where Σ_1 is the least significant bit, and that the next pulse should cause a decrement, hence control = 1. Each sum variable (Σ) is transferred to the Q output on the occurrence of the clock pulse via each D-type flip-flop. Inputs (B_1A_1), (B_2A_2) etc. are added and each produce 0 carry 1 except for (B_4A_4) which makes $\Sigma_4 = 1$. When the "carry's" ripple through, the result is 0110 with $C_{out} = 1$, which can be ignored. (This is 2's complement arithmetic, where negative-one, represented by 1111_2, is added to achieve subtraction).

IC_1: SN7483 (full adders)
IC_2: SN7495 (or 2×SN7474)
Typical operating frequency ≈ 10MHz

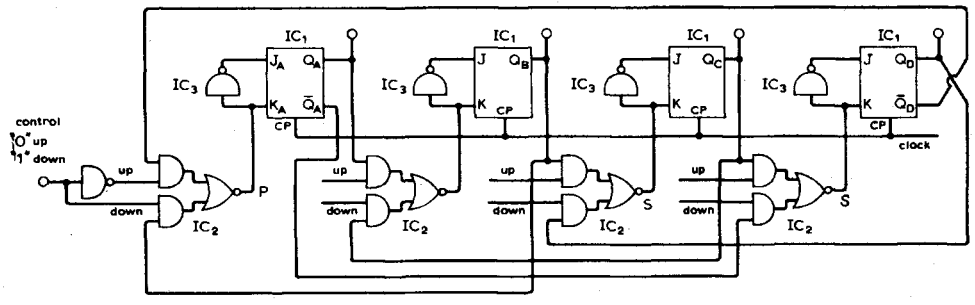
An eight-bit shift register is used to provide a variable modulus counter in which maximum and minimum counts may be detected is shown in Fig. 3

Shorting any one pair of external terminals decides the maximum counter loading at which the counter may then be considered to reverse.

Assume a counter cleared and a link at Q_C. Then, via gates X, Y, Z, $S_A = 1$, $R_A = 0$. The sequence of Q_A, Q_B, Q_C for the first three clock pulses is 100, 110, 111 and then $S_A = 0$, $R_A = 1$ and "detect max" goes high. For the next three pulses, the sequence is 011, 001, 000, when "detect min" goes high.

IC_1: SN74164 (DM8570)
IC_2: SN7400

Fig. 1



Further reading

Malmstadt & Enke, Electronics for Scientists, Benjamin, 1969.
High-speed synchronous reversible binary and BCD counters. Texas Instruments application report B40.
Baccolini, G., Benetazzo, L., & Clements, G., Variable dead-zone counter as a maximum value follower, *IEEE Trans.* vol. ECI-20, Aug. 1973.

Cross references

Series 14, cards 4 & 12.

Integrated circuits

IC_1: ½SN7473
IC_2: ½SN7451
IC_3: ¼SN7400

Fig. 2

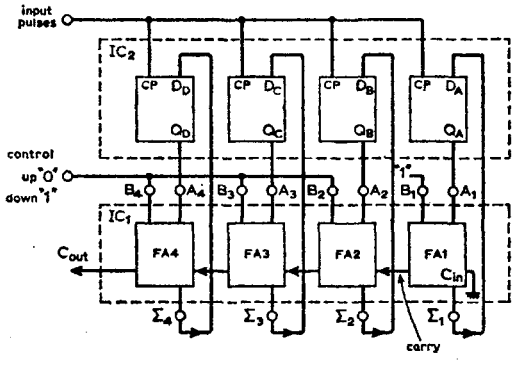
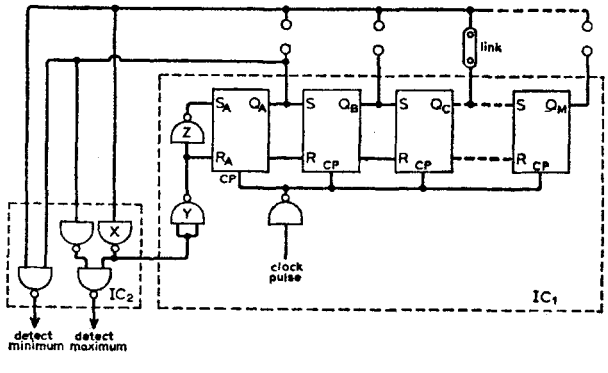


Fig. 3



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Divide by n counters

Counters with N states (modulus N) may comprise a sequence of counters with different moduli, integers n_1, n_2, n_3 etc. and $N = n_1 \times n_2 \times n_3$ . . Even numbers are achieved by cascading as in Fig. 2 (modulus 2^m, where m is the number of flip-flops). Synchronous circuits for smaller odd numbers are shown below. Q_A is the least significant bit, the natural binary sequence is followed and positive logic assumed.

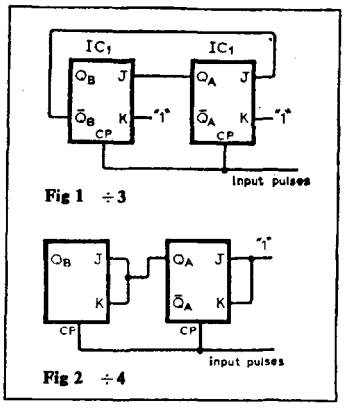


Fig 1 ÷3

Fig 2 ÷4

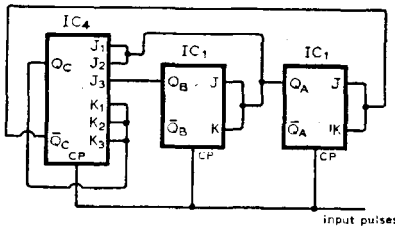
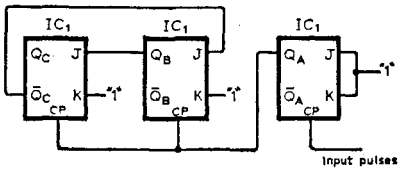


Fig 3 ÷5

Fig 4 ÷6



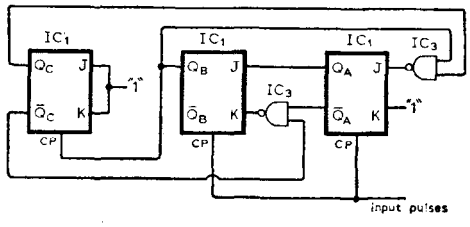


Fig 5 ÷7

SN7493 connection

Divisor N	*Feedback*	*Extra gate*
9	A D	—
10	B D	—
11	A B D	2 I/P AND
12	C D	—
13	A C D	2 I/P AND
14	B C D	2 I/P AND
15	A B C D	3 I/P AND

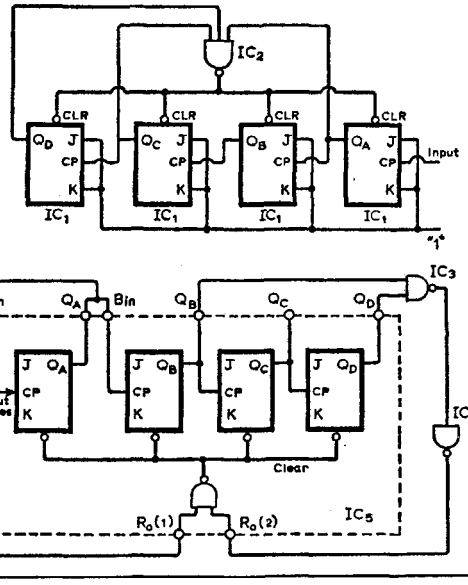
Components (typical)
IC_1: ½SN7473. IC_2: ⅓SN7410.
IC_3: ¼SN7400. IC_4: SN7472 (or ½SN7473 plus 3 input gates).
IC_5: SN7493. IC_6: ¼SN7408 (or ½SN7400). IC_7: ⅔SN7410.

Description
For the small prime numbers, it is sufficient to consider Fig. 3 as an example. Q_A flip-flop acts as a toggle and will change state on every input pulse while $\bar{Q}_C = 1$ ($Q_C = 0$). Q_B changes state whenever Q_A goes from 1 to 0. Q_C will only be set to 1 when both Q_A and Q_B are logic one i.e. on the 4th clock-pulse, because $J_1 = J_2 = J_3 = 1$ and the K inputs are 0. Hence on the 5th pulse, since $\bar{Q}_C$ is now 0, Q_A will remain at 0 hence Q_B is logic zero, and Q_C will be reset to 0, because J_1 to $J_3 = 0$ and K_1 to $K_3 = 1$. The sequence then repeats.

Fig. 6 demonstrates an alternative technique. The counter is reset to zero when a negative-going edge is simultaneously applied to the CLEAR inputs. This is obtained from the NAND gate, when the predetermined binary number, 1101 (13), is detected. The minimum duration between input pulses depends on propagation delays of flip-flops, the gate delay, and the reset delay. If the output is to be read, the lines should be gated to avoid transmitting spikes that will appear on some lines depending on the divisor N.

MSI integrated circuit packages e.g. SN7493 4-bit ripple counter contains a NAND gate for clearing, but additional gating is necessary for certain counts (see Table 1). Fig. 7 is the connection for $N = 11_{10}$, the feedback being applied via reset terminals $R_{0(1)}$ and $R_{0(2)}$. A useful arrangement for division by large numbers is shown in Fig. 8, where N_1 and N_2 must be prime numbers with respect to each other. The arrangement ($N_1 = 3$, $N_2 = 7$) provides $N = 21$; input pulses are applied simultaneously to each counter, and each cycles through its own modulus until all outputs are 1's together, thus enabling AND gates, and resetting to zero via reset terminals.

Fig 6



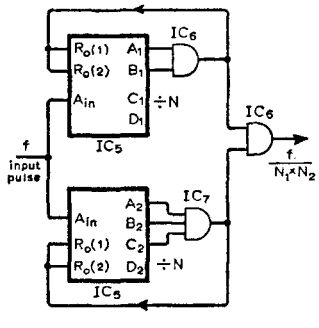


Fig 8

Fig 7

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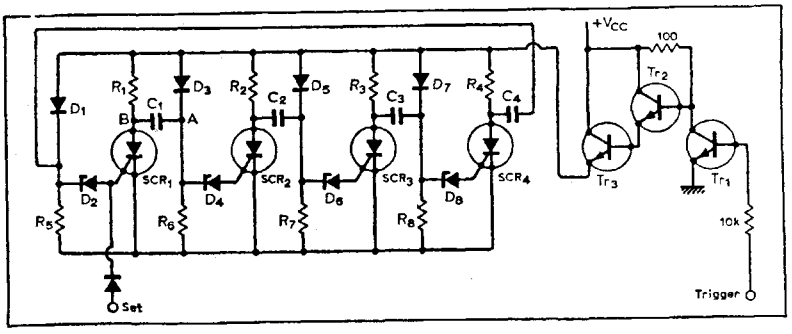
High-power counters



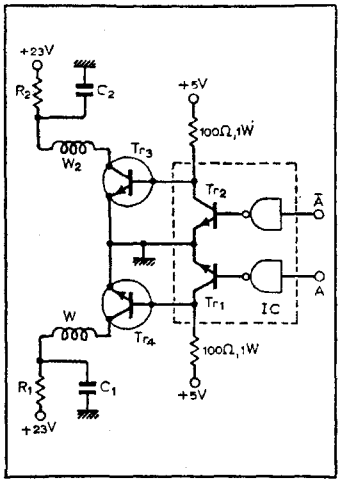
Component values
R_1, R_2, R_3, R_4: 5 to 10Ω
R_5, R_6, R_7, R_8: 100kΩ
C_1, C_2, C_3, C_4: 0.47μF
D_2, D_4, D_6, D_8: 1N757
D_1, D_3, D_5, D_7: 1N914
SCRs: 2N1595
Tr_1, Tr_2: 2N1420
Tr_3: 2N657A

Performance
Vcc: 9V
Trigger amplitude −6 to 9V
width >200μs
Set pulse: 3V max
Maximum frequency: 1kHz
Minimum frequency: depends on capacitor losses, s.c.r. leakage current, and diode leakage current

Circuit description-1
Circuit shows a four-stage dynamic ring counter with power capabilities per stage of 20W at between 2 and 5A. Consider first the situation where all the s.c.rs are non-conducting. A set pulse applied at the gate of SCR_1 causes it to conduct freely via the load resistor R_1 and this continues in the absence of a set voltage until the supply is removed, which occurs when a trigger pulse is applied as base drive to Tr_2 is then shunted to ground, removing base drive to Tr_3. While the supply is applied to the counter and SCR_1 is conducting, point B is at ground voltage and C_1 charges via D_3, so that $V_{AB} = V_{CC}$. When the supply is removed, C_1 retains this charge as there is no discharge path (apart from leakage). When the supply is reapplied, SCR_1 remains non-conducting and point B rises to the supply. Consequently, point A will rise to $2V_{CC}$. If D_4 is chosen so that its breakdown voltage lies between V_{CC} and $2V_{CC}$, breakdown occurs and SCR_2 conducts so that current flows in the second load, R_2. Further trigger pulses will cause each succeeding stage to conduct. Resistor R_6 allows C_1 to continue discharging below the zener voltage of D_4. Diode D_3 arrests this discharge so that the final condition is zero charge on C_1—which is the initial condition of C_1 prior to SCR_1 conducting. Continual rotation of a single logic 1 is what has been described so far. Two adjacent logic 1's cannot reliably be rotated by this scheme but there is no reason why any pattern cannot be rotated provided no two logic 1's are adjacent. Should more than one logic 1 be rotated then the supply section comprising Tr_1, Tr_2 and Tr_3 will require re-design as the current drawn is n + (current for one stage), n being the number of on stages.

To prevent noise falsely triggering any s.c.r., resistors between gate and ground should be provided.

Further reading
Strangio, High power counter drives 20W loads, *Electronics*, March 1, 1973



Component values
R_1, R_2: 33Ω, 16W
C_1, C_2: 100μF, 40V
W_1, W_2: 9Ω stator coils
Tr_3, Tr_4: BSW 66
IC: SN75451P

Performance
Controlled by the torque characteristics of the motor. The coil current was 550mA and the maximum speed was 6000 steps per second, corresponding to a counter clock frequency of 6000 pulses per sec. A and Ā were normal t.t.l. voltage levels (5V and 0V).

Circuit description-2
A stepper motor drive is required to rotate a magnetic field pattern in either direction and at variable speed. This can be achieved by supplying the stator coils from an up-down counter with a variable pulse rate (see Card 4). Circuit shows ¼ of the drive circuitry for an 8-phase stepper motor with power consumption of 11W which is dissipated in only 4 of the phases at any one time. Two of these phases are shown in the diagram in the form of the 9Ω coils, W_1 and W_2. The motor operation requires that current flows in one of these coils at a time and this is achieved as shown. A and Ā are obtained from one stage of a 4-stage Johnson, up-down counter. If A is "high" then T_1 will not conduct and base drive is presented to T_4 and consequently current from the 23V supply will flow through W_1. Likewise no current flows through W_2 in this condition. However, if Ā is high the position is reversed. Tr_4 and Tr_3 are high current transistors capable of feeding inductive loads. R_1, C_1 and R_2, C_2 serve to reduce the circuit time constant so that higher speeds may be achieved.

Further reading
Shakaiba, M. A. Digital control system for an 8-phase stepper motor, Project Report, Electrical Engineering Dept, Paisley College of Technology.
King, D. S. Stepper motor for digital control systems, *Control and Instrumentation*, June 1971.

Cross reference
Series 14, card 5.

High-speed counters

Circuit description

In most counting arrangements the decoding of the end of the sequence and the resulting resetting of the counter occur in the same clock period. This can be avoided by using the philosophy of the circuit of Fig. 1 and thereby obtain increased counting speeds, irrespective of the logic family used. Circuit shows a frequency divider in which the second last number to appear on the output of the counters is decoded. This is done by the AND gates A_1 and A_2 and occurs on the falling edge of the clock pulse when A_0 goes to logic 1, corresponding to the number 97. Inputs J′ and K′ are then in the logic 1 state and the next clock pulse triggers the flip-flop and also the strobe pulse. The counter remains in this state until the clock pulse at the end of the 99th state toggles the flip-flop back again. The counter is then ready to start up-counting again from the initial state, which is, of course, dictated by the b.c.d. data inputs.

This arrangement allows the reset pulse to be a full clock period wide and unaffected by the counter states. Further, the decoding time and the reset time occur in different clock periods, rather than in the same period as in other methods.

Hence the time taken for N to be fed in can be almost a full clock period and as a result higher clock frequencies can be handled.

With the devices quoted counting speeds of over 40MHz have been achieved. The second stage of the counter need not be such a high speed device (and, consequently, high power consuming device) as clock frequency to it is 1/10th of that to the first stage.

Higher frequencies are achievable if one uses faster logic families. Fig. 2 shows an e.c.l. device being used in a fashion similar to that of Fig. 1. In this case the device is a down counter, counting down from the preset state N and giving an output frequency $f_{CL/N}$. Clock frequencies in excess of 110MHz can be handled. Again the second last number in the sequence is decoded, in this case 0100, and this causes the flip-flop to change state on the next clock pulse, thereby resetting the counter to N.

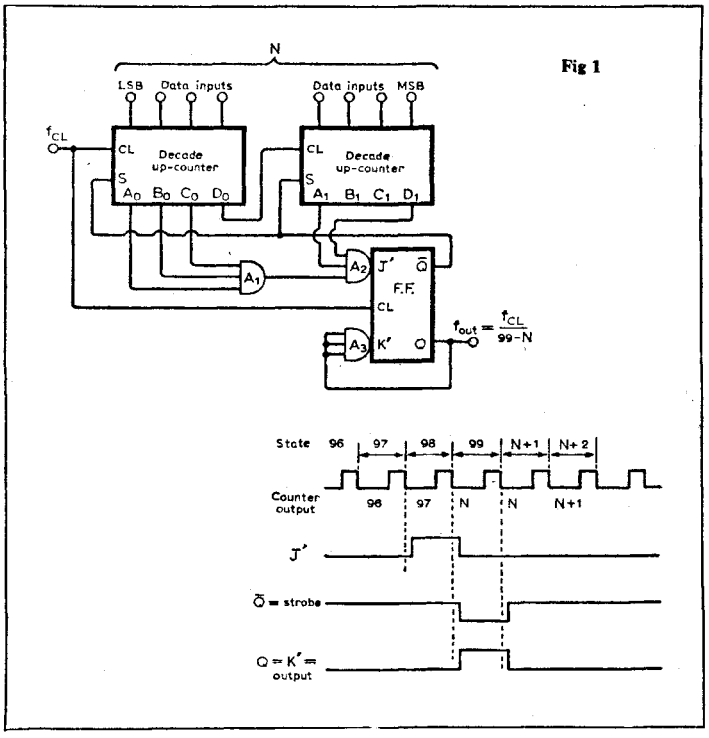


Fig 1

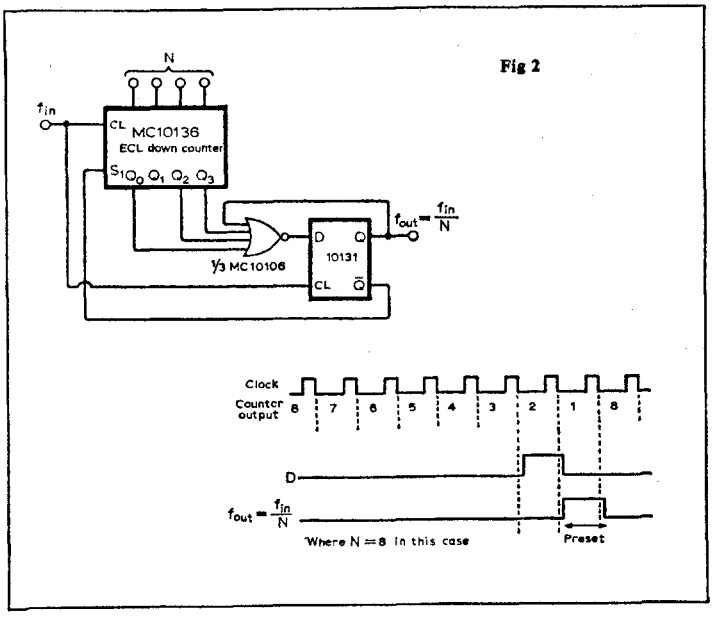


Fig 2

Components

Counters: 8290, decade up-counter for which the input data is on output when S is logic 0.
Flip-flop: 74H102 (high speed)
A_1, A_2, A_3: ⅓ MC3006

Further reading

Clifford, D. Reset dividers faster with a single flip-flop, *Electronic Design*, Aug. 5, 1971.
Balph & Granden, Boost counting speeds to 110MHz, *Electronic Design*, April 1, 1973.
Tan, Z. C. New tunnel diode ring counter, *Proc. IEEE*, April 1973.

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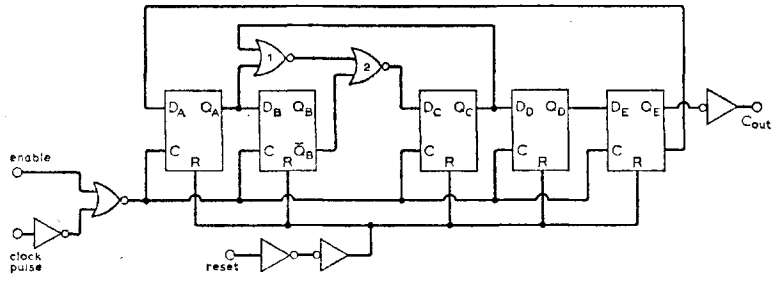
Low-power counters

Fig 1



Package CD 4017AE
Temperature: −40 to +85°C
Typical speeds:
5MHz at 10V d.c.
1MHz at 3.5V
100kHz at 3.5V
Approximate power dissipation for the above values are 30mW, 1mW and 100μW respectively, for 15pF loading.
Minimum pulse width 100 nanoseconds at 10V.

Circuit description
The counter of Fig. 1 uses a Johnson configuration and obtains speeds in the region of 5 to 7MHz, each flip-flop operating at only one tenth of the input frequency. The counter is disabled if enable is high, reset to zero being achieved by applying a logic 1 level to reset. The counter sequences on the leading edge of each clock pulse, the Johnson code being maintained by ensuring that the D_C input is only high, when either Q_A and Q_B or Q_C and Q_B are high, via NOR gates 1 and 2. Additional gating (not shown) provides ten decoded outputs, which sequentially are high for one full clock period.
For count <ten, use quad-NOR i.c. CD4001. In Fig. 2 the cross-coupled pair is a reset latch, to ensure reset when flip-flops have different reset propagation delays. The decimal zero output is low except when counter is cleared, hence when the N output goes high, point X→0, and a reset pulse is generated while the clock is high. When counter resets, zero terminal goes high. This can drive another counter.

Programmable counter
$N = 1$ to 10 IC: CD4018
This is a 5-stage Johnson counter but with the Q outputs buffered with inverters to provide a Johnson BCD output. Counts less than ten achieved by feedback to the DATA input terminal, see Fig. 3. The odd count is obtaining by ANDing the two $\bar{Q}$ outputs (table) with ½ CD4011. This ensures that the all '1's state of the counter is avoided. The counter may be preset to any combination fed to the J inputs, by pulsing the preset-enable input. Voltage levels and speeds are similar to CD4017AE. As a preset counter, counter will advance from preset state to 11110, where the right-most bit is $\bar{Q}_5$. The presence of $\bar{Q}_4$ and $\bar{Q}_5$ should be detected as shown in Fig. 4 to reset the counter.

Ripple counters
CD 4020AE
14 stages but outputs available from stage 1 and stages 4 to 14 inclusive.
Typical speed: 7MHz at 10V
2.5MHz at 5V
Power dissipation:
typical 1mW at 1MHz at 5V
10mW at 1MHz at 15V
CD 4040AE
12 stages
All 12 buffered outputs available
Typical speed: 8MHz at 10V.

Up-Down counter CD 4029AE
4 stage: Either BCD decade or binary by input control
Typical speed: 5MHz at 10V
Dissipation: 30mW
Load: 15pF
Typical speed: 100kHz at 3.5V
Dissipation: 1mW
Load: 15pF

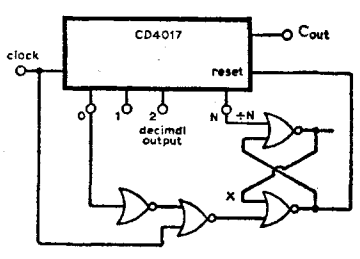
Even count	*DATA*	*N*
	$\bar{Q}_1$	2
	$\bar{Q}_2$	4
	$\bar{Q}_3$	6
	$\bar{Q}_4$	8
	$\bar{Q}_5$	10

Odd count	*DATA*	*N*
	$\bar{Q}_1\ \bar{Q}_3$	3
	$\bar{Q}_2\ \bar{Q}_3$	5
	$\bar{Q}_3\ \bar{Q}_4$	7
	$\bar{Q}_4\ \bar{Q}_5$	9

Further reading
RCA Solid State Databook Series SSD-203A 1973

Cross references
Series 14, cards 4 and 10.
Series 11, card 6.

Fig 2



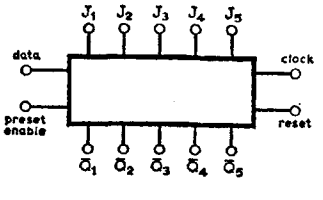


Fig 3

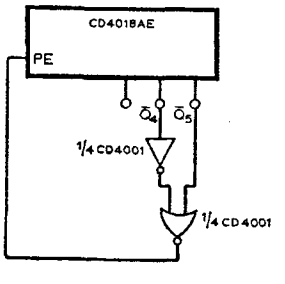


Fig 4

Decade counters

Fig 1

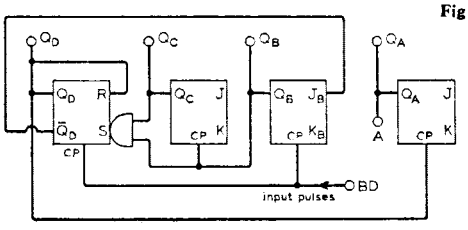


Fig 2

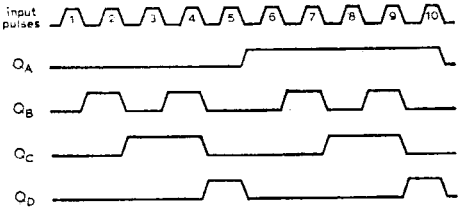
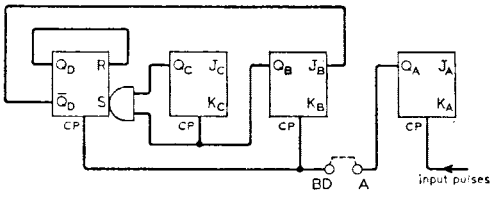


Fig 3



Circuit description

The four master-slave flip-flops of Figs. 1 and 3 are contained within one i.c. package, SN7490, and provides separate ÷5 and ÷2 facilities. A symmetrical decade counter where the period of the output pulse at Q_A is ten times the input pulse period with equal mark-to-space ratio is shown in Fig. 1, with the associated waveforms of Fig. 2. The J-K terminals with no inputs are internally connected to be logic 1. Flip-flop C toggles for all 1 to 0 transitions of Q_B, and Q_D is set on the 4th pulse, but reset on the 5th pulse ($S = 0$, $R = 1$), thus setting Q_A. Q_B cannot change because $J_B = 0$, $K_B = 1$. For the next five pulses, the sequence of flip-flops B, C and D is similar, when Q_A is reset on the tenth pulse.

The connections of Fig. 3 allow the counter to sequence in an 8 4 2 1 b.c.d. code, where flip-flop D has the maximum weighting: gated direct reset lines (not shown) are provided to inhibit count inputs and return outputs to zero. Typical frequency and power dissipation is up to 18MHz, and around 160mW.

Another asynchronous 8 4 2 1 b.c.d. counter uses J-K flip-flops in a toggle mode (Fig. 4), has no logical hazards, and may be implemented with two SN7473 and one SN7400.

Fig. 5 is an 8421 b.c.d. synchronous counter, which requires 3-input AND gates or triple input J-K flip-flops. Q_A changes state for every clock-pulse (unused J-K inputs may be connected to logic '1'). Q_B changes on the 2nd, 4th, 6th, 8th clock pulses, but is inhibited from a 0 to 1 transition on the 10th pulse, since $\bar{Q}_D = 0$. Flip-flop C is toggled whenever $Q_A = Q_B = 1$, and Q_D undergoes a 0 to 1 transition when $Q_A = Q_B = Q_C = 1$, on the occurrence of the 8th pulse. Q_D resets to zero on the 10th pulse, because $J_1 = 0$ and the K inputs are high.

Implemented with either two SN7473 and three SN7410, or four off SN7472.

Figs. 6 & 7 are two other forms of b.c.d. synchronous counters. Fig. 6 counts in 8421 code, Fig. 7 in excess-3 code. In each case the least significant bit is flip-flop A.

Further reading

T.T.L. Integrated Circuits, Counters and Shift Registers, application report CA102. Texas Instruments.

Malmstadt and Enke, Digital Electronics for Scientists, Benjamin, 1969.

Kohonen, T. Digital Circuits and Devices, Prentice-Hall, 1972.

Cross references

Series 14, cards 3 & 9.

Fig 4

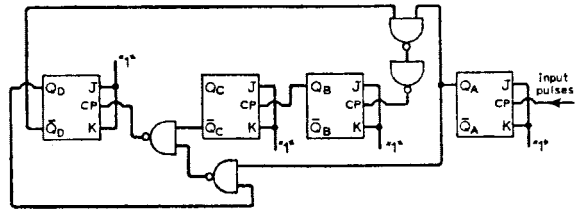


Fig 5

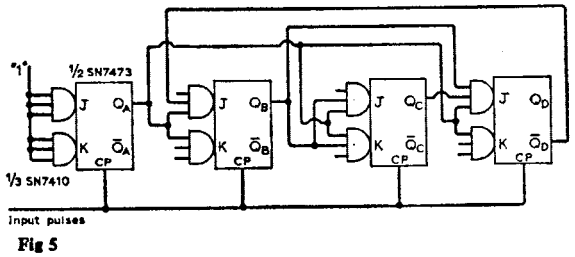


Fig 6

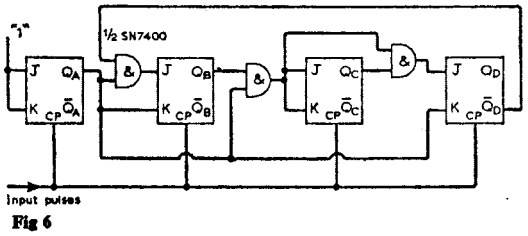
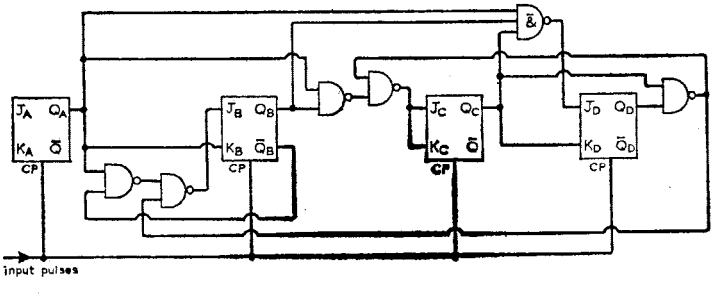
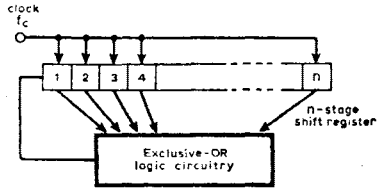


Fig 7



M-sequence generators

Fig 1



Description

Maximum length sequences (M-sequences) have many uses in data communications system identification and correlation methods. Some of them have properties very similar to that of band limited white noise, particularly if passed through simple first or second order R-C filters—hence the name pseudo-random-binary sequence (p.r.b.s.). They are produced by a simple synchronous shift register or counter with feedback from various stages determining the state of the first stage on receipt of each clock pulse. The feedback is basically by means of exclusive-OR gates (modulo-two gates). The basic diagram is as shown in Fig. 1, the output being taken from any stage. The sequence produced is cyclic and repeats itself after 2^n-1 pulses, the all-zero state being avoided. The maximum number of states for an n-stage register is 2^n but to prevent the all-zero state becoming a permanent state requires considerable extra logic and, hence, this state is avoided and the length 2^n-1 is described as maximal.

Long sequences can be generated by simple feedback arrangements. The Table indicates the simplest feedback arrangements for all those registers up to length 18, and all those beyond 18 and up to 33 which require only one exclusive-OR gate. Fig. 2 shows how the characteristic polynomials of the Table are interpreted in terms of hardware for the particular case of $n = 8$. If JK flip-flops are used as the register stages some simplification is possible if the polynomial contains D to the power one. Column 3 or the table indicates the logic necessary for the J input and column 4 indicates the K input.

If the output of stage 1 is regarded as the output, versions of this sequence delayed by $L\Delta T$, where ΔT is the clock period and $L = 0$ to $n-1$, are clearly available from the remaining stages. Delays of up to $N\Delta T$, where $N = 2^n-1$ can also be generated by modulo-two addition of several of the output stages (ref. 1).

When the sequence is being used as a noise source the output is arranged so that logic $1 = +a$ volts and logic $0 = -a$ volts. The r.m.s. value of the waveform is than a^2 and the mean value is a/N (this would be zero if $N = 2^n$ rather than 2^n-1). The power spectrum, which is discrete, is where $G(k)$ is the power in (volt)^2 of the kth harmonic. $G(k)$ is shown in Fig. 3. The small d.c. term is often ignored.

Spacing between the lines of Fig. 3 is $1/N\Delta T$ and hence the power density spectrum (power per unit bandwidth) is $G(k)N\Delta T$. The 3-dB point for the power density spectrum occurs at approximately $1/3\Delta T$ so that for systems with bandwidth less than $1/3\Delta T$ the signal appears as white noise. Further, the autocorrelation function for the signal is very similar to that for white noise (ref. 1). The probability distribution of the signal is not at all Gaussian because it consists of two lines at $\pm a$ respectively. However, when passed through a suitable R-C filter with a break point less than $1/3\Delta T$ the distribution does become close to Gaussian i.e. that for band-limited white noise (ref. 2).

$$G(k) = \frac{a^2}{N^2} + \sum 2a^2 \frac{(N+1)}{N^2}\left(\frac{\sin\frac{\pi k}{N}}{\frac{\pi k}{N}}\right)^2$$

References

1. Davies, W. D. T., Generation and properties of M-sequences, *Control*, June, July and August 1966.
2. Roberts, P. D. & Davis, R. H., Some statistical properties of smoothed M-sequences, *Proc. I.E.E.* 1966 vol. 113, p.190.

Further reading

Davies, A. C., Design of feedback shift registers and other synchronous counters, *Radio and Electronic Engineer*, April 1969.
Peterson, W. W., Error Correcting Codes, MIT Technical Press 1961.
Golomb, S. W., Shift Register Sequences, Holden Day 1967.

n	Characteristic Polynomial	J input	K input
2	$1 \oplus D \oplus D^2$	2	J
3	$1 \oplus D \oplus D^3$	3	J
4	$1 \oplus D \oplus D^4$	4	J
5	$1 \oplus D^3 \oplus D^5$	2 ⊕ 5	J
6	$1 \oplus D \oplus D^6$	6	J
7	$1 \oplus D \oplus D^7$	7	J
8	$1 \oplus D \oplus D^3 \oplus D^5 \oplus D^8$	3 ⊕ 5 ⊕ 8	J
9	$1 \oplus D^4 \oplus D^9$	4 ⊕ 9	J
10	$1 \oplus D^3 \oplus D^{10}$	3 ⊕ 10	J
11	$1 \oplus D^2 \oplus D^{11}$	2 ⊕ 11	J
12	$1 \oplus D \oplus D^4 \oplus D^6 \oplus D^{12}$	4 ⊕ 6 ⊕ 12	J
13	$1 \oplus D \oplus D^3 \oplus D^4 \oplus D^{13}$	3 ⊕ 4 ⊕ 13	J
14	$1 \oplus D \oplus D^5 \oplus D^{10} \oplus D^{14}$	6 ⊕ 10 ⊕ 14	J
15	$1 \oplus D \oplus D^{15}$	15	J
16	$1 \oplus D \oplus D^3 \oplus D^{12} \oplus D^{16}$	3 ⊕ 12 ⊕ 16	J
17	$1 \oplus D^3 \oplus D^{17}$	3 ⊕ 17	J
18	$1 \oplus D^7 \oplus D^{18}$	7 ⊕ 18	J
20	$1 \oplus D^3 \oplus D^{20}$	3 ⊕ 20	J
21	$1 \oplus D^2 \oplus D^{21}$	2 ⊕ 21	J
22	$1 \oplus D \oplus D^{22}$	22	J
23	$1 \oplus D^5 \oplus D^{23}$	5 ⊕ 23	J
25	$1 \oplus D^3 \oplus D^{25}$	3 ⊕ 25	J
28	$1 \oplus D^3 \oplus D^{28}$	3 ⊕ 28	J
31	$1 \oplus D^3 \oplus D^{31}$	3 ⊕ 31	J
33	$1 \oplus D^{13} \oplus D^{33}$	13 ⊕ 33	J

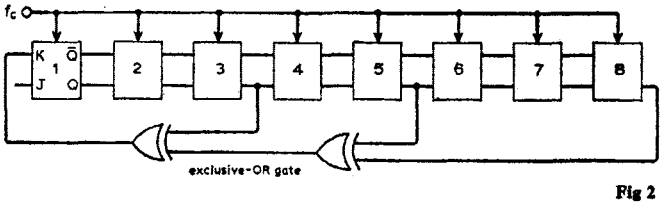
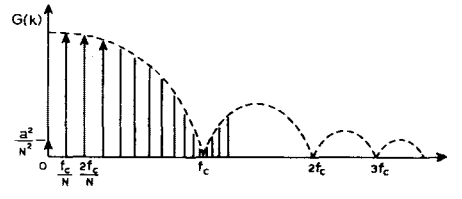


Fig 2

Fig 3



Glossary: flip-flops and b.c.d. codes

Integrated circuit flip-flops are usually clocked i.e. the change of state is initiated by a timing pulse called the clock pulse. The outputs are commonly termed Q and $\bar{Q}$. If Q = 1, $\bar{Q}$ = 0 (and vice versa). These states are dependent on the logical states of the flip-flop (or bistable) inputs and this dependence is shown in each associated TRUTH table, where Q_n is the state of the Q output after the nth pulse, and Q_{n+1} is the new state after the next pulse.

When Q is made to be logical '1', the flip-flop is said to have been SET, and when Q is made '0', the flip-flop has been RESET or CLEARED.

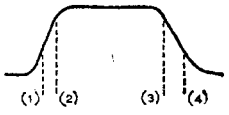
Edge-triggered and master-slave types are available. The time for which data must be present before the clock pulse threshold (set-up time) and the time for which data must be maintained after the clock edge (hold time) are normally specified. The transfer of information in the master-slave flip-flop is according to the numbers marked on the pulse shown, and it may be considered that the master and slave flip-flops are distinct, but isolated or connected by gates.

(1) slave isolated from master

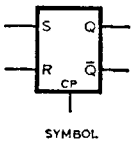
(2) data entered into master

(3) master is isolated from input terminals

(4) data is transferred from master-to-slave



R-S flip-flop



SYMBOL

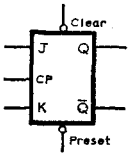
S	R	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	x

x = indeterminate

TRUTH TABLE

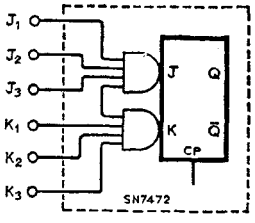
R = S = 1 must be avoided because the logical value of the Q output is uncertain.

J-K flip-flop

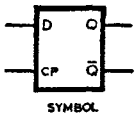


J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

This has two data inputs termed J and K (and may be considered to be similar to S and R of the R-S flip-flop), but no indeterminate state exists for any combination of the inputs. Multi-input J and K terminals are achieved on some i.cs with internal gating, where the J and K inputs are for example the ANDED inputs J_1 J_2 J_3 and K_1 K_2 K_3. CP is the clock-pulse terminal, Preset and Clear terminals may also be available. These inputs are maintained normally at logical '1'. A negative edge applied to PRESET, sets Q = 1, and if applied to CLEAR, makes $\bar{Q}$ = 1. The negative edge triggering can be indicated by the small circle at the terminal as in diagram.



D-type flip-flop



SYMBOL

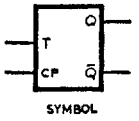
D	Q_{n+1}
0	0
1	1

TRUTH TABLE

This has one data input, and may also have both outputs available. In the table, D is the input before clocking and Q_{n+1} is the Q output after clocking.

Note—CMOS flip-flops are cleared by a positive-going edge at the clear input.

T-type flip-flop



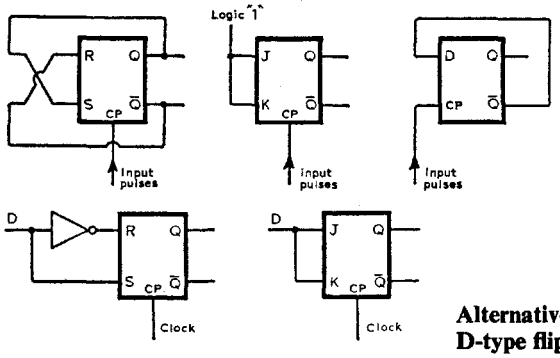
SYMBOL

T	Q_{n+1}
0	Q_n
1	$\bar{Q}_n$

TRUTH TABLE

This may be considered as the basic binary or toggle flip-flop. When T = 0, the Q output will not change state on the occurrence of a clock pulse. If T = 1, Q takes up the opposite state when the flip-flop is clocked.

Alternative toggle flip-flops



Alternative D-type flip-flops

Further reading

Walters, D. J. Integrated Circuit Systems, Iliffe Books, 1971.

Malmstadt & Elke, Digital Electronics for Scientists, W. A. Benjamin, 1969.

Texas Instruments Inc. Designing with TTL Integrated Circuits.

Cross references

Series 14, card 5.
Series 14, card 3.

Decimal codes

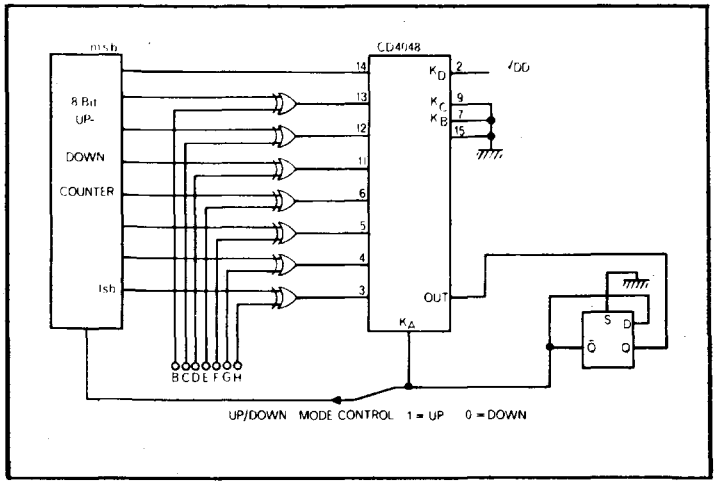
These are listed with the least significant bit (LSB) rightmost for the weighted codes, i.e. those in which a decimal numerical weighting is assigned to each bit position.

JOHNSON	NATURAL BCD 8-4-2-1	4-2-2-1	GRAY	EXCESS-3	DECIMAL NUMBER
00000	0000	0000	0000	0011	0
00001	0001	0001	0001	0100	1
00011	0010	0010	0011	0101	2
00111	0011	0011	0010	0110	3
01111	0100	1000	0110	0111	4
11111	0101	0111	0111	1000	5
11110	0110	1100	0101	1001	6
11100	0111	1101	0100	1010	7
11000	1000	1110	1100	1011	8
10000	1001	1111	1101	1100	9

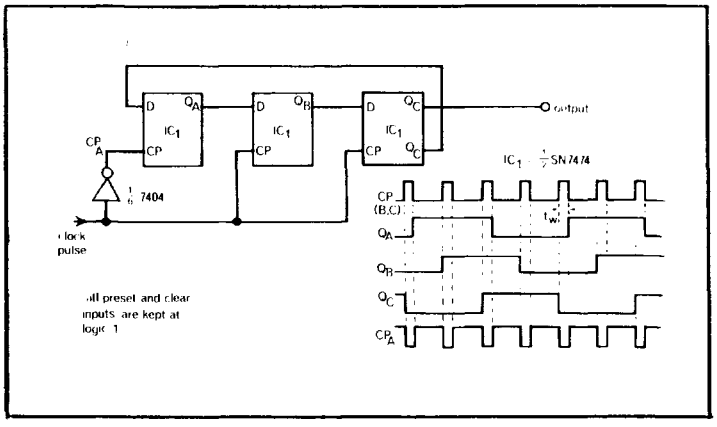
wireless world circard

Set 14: Digital counters Up-date

1. Control primarily depends on the logic simulation of the CD4048 gate where, if $K_B=K_C=0$, $K_A=1$, the gate acts like an eight-input AND gate i.e. output is 1 if all inputs are high. Also if $K_A=0$, the gate acts like an eight-input NOR gate, and the output is 1 if all inputs are logic 0. Using exclusive-OR gates between the counter and the CD4048, the counter can then be arranged to cycle between any two symmetrical binary states by programming inputs B to H inclusive, e.g. if BCDEFGH is programmed to be 0001111, then when the counter reaches 11110000, the CD4048 will see all logic 1s at the inputs and provide an output which can be used to clock the D-type flip-flop, i.e. the maximum output is 240_{10}. When the counter then starts to count down, an output is again obtained when the counter reaches 00001111, where the exclusive-OR gates will provide all 0s to the gate-inputs and as K_A is then 0. The effective NOR gate senses the 0s to provide a changeover signal.



2. The odd synchronous counter provides symmetrical high and low output levels although driven from an unsymmetrical clock pulse source. Flip-flop A is driven from an inverted waveform and hence will change state, depending on the D input, at a clock pulse rising edge, one clock pulse width earlier than any changes that occur in flip-flops B and C. Observe at clock pulse marked t_w, flip-flop C changes at the leading edge of the clock pulse and flip-flop edge changes at the trailing, since it is driven via the inverter. The minimum clock pulse allowable depends on the propagation delay of flip-flop C and the data set up time of flip-flop 1. Figures quoted are 45 and 20ns respectively giving a minimum pulse width of 65ns.

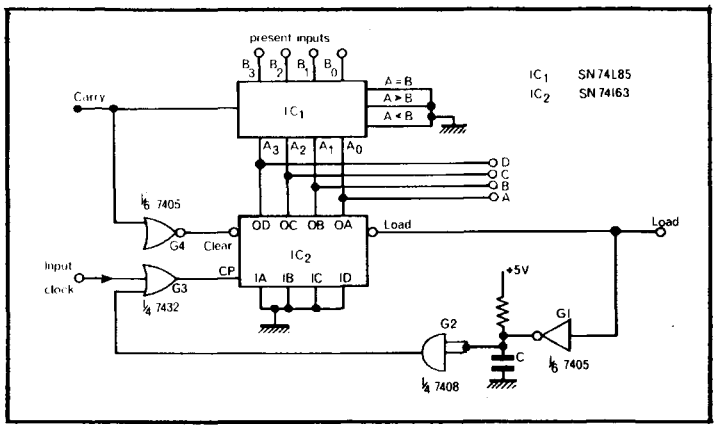


Reference

Greenberg, M. Ideas for Design, *Electronic Design 20*, Sept. 27, 1974.

3. This arrangement of a 4-bit comparator and a 4-bit synchronous counter provides a programmable variable modulus counter in the range decimal 2 to 15.

A binary number N is set up at the preset inputs B_0 to B_3 (where B_0 is the least significant bit), i.e. over the range 0001 to 0111. The clock input causes the counter to reach the number $(N+1)$, where the counter outputs compared with the programmed comparator value will show equality by generating an output pulse at the carry terminal. This is used to reset the counter to zero, and the sequence repeats. For initialising the counter, gate G_2 ensures that the exponential rise of voltage that will occur across C when the load terminal is driven low at commencement, will provide a fast logic level change at gate G_3 when the capacitance voltage reaches the threshold level of G_2. Cascade connexions of comparators allow an extension of the modulus to 256 for two stages, the carry from the first counter being ANDed with the driving clock pulse.



Reference

Panzitta, J. Ideas for Design, *Electronic Design 11*, May 24, 1974.

notes

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Set 15: Pulse modulators

The following article is intended to introduce techniques of conveying analogue information using pulse-train modulation. It describes all the important methods of coding pulse trains and discusses their properties. If you have no previous experience of pulse modulation, we recommend reading this concise summary.

Various ways of producing amplitude and duration-modulated trains are given on cards 1–4, 6, 7 & 10, including two cards whose circuits use the 555 timers. Card 8 is not really a modulator—it gives d.c. motor control schemes using pulse modulated trains. The results are especially interesting in that the motor is operated well outside its normal operating conditions. Card 11 shows how position modulated pulses are derived. Two techniques, relying on a monostable to convert p.d.m. to p.p.m., are described in the article (Figs. 7 & 8), the card giving appropriate waveforms and a circuit.

In pulse-code modulation, card 12, p.a.m. is first produced and quantized, linearly or otherwise, and then coded in a binary way. The attraction of the scheme is improved signal-to-noise ratio over the other methods (the noise hierarchy goes from p.a.m. to p.d.m. to p.p.m. to p.c.m.). Card 9 gives two modulator circuits that produce a train of binary pulses relating to the rate of change of modulating signal between sampling instants, as opposed to instantaneous values, for differential p.c.m. or delta modulation.

Two signals can be modulated onto a single pulse train in the variable slope modulator of card 5, by modifying the slope of both leading and trailing edges. A modification shows that by restricting the dynamic range of the two signals, a third may be modulated as amplitude.

Pulse modulators

Systems using amplitude modulation, frequency modulation and phase modulation use a sinusoidal carrier which has one of its characteristics—amplitude, frequency or phase—varied under the control of an analogue signal of message $x(t)$. In pulse modulation systems the carrier may be considered to be a periodic, rectangular pulse train $c(t)$ as shown in Fig. 1. The pulse train has an amplitude A_c, a pulse width τ_c and a fundamental frequency $f_c = 1/T_c$.

Amplitude, width or position (in time) of the carrier pulses may be varied as a function of the lower-frequency analogue signal waveform to produce pulse modulation, p.a.m., pulse width (duration) modulation, p.d.m., or pulse position modulation, p.p.m. For all practical applications of pulse modulation, the analogue modulating signal should be band-limited with a suitable filter so that it contains a reasonably well-defined upper frequency component f_m which is the highest significant frequency in the modulating waveform.

Each pulse in a modulated carrier pulse train $y(t)$ contains one sample of information regarding the "instantaneous" value of the modulating signal $x(t)$. The sampling theorem states that all the information in $x(t)$ will be preserved if the samples are evenly spaced and occur at a rate that is not less than $2f_m$. In practice the sampling rate normally exceeds this minimum value by a factor of at least about 1.2.

Pulse amplitude modulation may be considered to be the process of changing the amplitude of a periodic rectangular carrier pulse train in synchronism with, and in proportion to, the instantaneous variations of the modulating analogue signal. Using a sinewave as an example of the modulating signal the p.a.m. waveform shown in Fig. 2 is obtained. The basic form of a pulse amplitude modulator is shown in Fig. 3.

The unmodulated carrier pulse train shown in Fig. 1 has a Fourier series representation

$$c(t)=\frac{A_c\tau_c}{T_c}\left[1+2\sum_{n=1}^{\infty}\left\{\frac{\sin(\omega_n\tau_c/2)}{\omega_n\tau_c/2}\right\}\cos\omega_n t\right]$$

where $\omega_n = 2n/\tau_c$ and $n = 1, 2, 3 \ldots \infty$.

With a sinusoidal modulating signal of $A \sin \omega t$, the amplitude of the pulses become $A_c(1 + m_A . \sin \omega t)$ where m_A is the modulation index A/A_c which must be < 1 to avoid overmodulation of the pulse train.

The p.a.m. wave shown in Fig. 2 may be considered either as a sinewave amplitude modulating the pulse train, or as the unmodulated carrier sampling the amplitude function $A_c(1 + m_A \sin \omega t)$ over an interval of τ, at a rate equal to the p.r.f. of the pulse train, f_c. The frequency spectrum of the p.a.m. signal may be seen conceptually by considering initially that of the unmodulated carrier which will contain a d.c. component and a theoretically infinite series of sinusoids at f_c, $2f_c$, $3f_c$, etc, which have diminishing amplitude with increasing frequency.

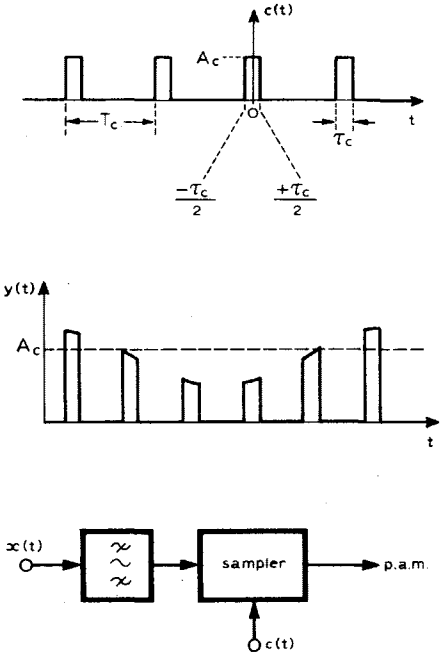


Fig. 1. Carrier pulse nomenclature.

Fig. 2. A p.a.m. waveform—a modulated pulse or a sampled input signal.

Fig. 3. The basic pulse-amplitude modulator.

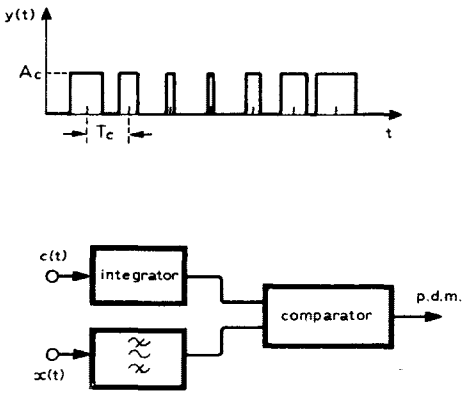


Fig. 4 (top). In this example of p.d.m., both edges are shifted, modulating the pulse symmetrically.

Fig. 5. The input signal x(t) *varies the threshold of a triangular pulse from the integrator to produce p.d.m.*

The amplitude modulation will produce a lower sideband and an upper sideband to each of the carrier components f_c, $2f_c$, etc and a component at the original modulating frequency or band of frequencies. This latter component will have an amplitude of $A_c m_A \tau/T_c$ and may be recovered by passing the p.a.m. wave through a low-pass filter, which also passes the d.c. component. P.a.m. signals are required to preserve the *shape* of the modulated pulses and therefore suffer from the same signal-to-noise ratio restrictions as a.m. but with a transmission bandwidth requirement of approximately $3/\tau_c$ Hz. Consequently p.a.m. is more commonly used as a part of the signal processing in other systems than as a system in its own right.

Pulse duration modulation may be considered as the process of changing the width of the pulses in a periodic, rectangular carrier pulse train in synchronism with, and in proportion to, the instantaneous variations of the modulating analogue signal. In p.d.m., either the leading edges or the trailing edges or both edges of the carrier pulse train may be shifted in time due to the modulation. Fig. 4 shows an example of a p.d.m. wave where both edges have been shifted and

the time interval between the centres of successive pulses remains fixed at T_c. With a sinusoidal modulating signal the unmodulated pulse width τ_c becomes $\tau_c(1+m_w\sin\omega t)$ where m_w is the modulation index τ_m/τ_c which must be $\leqslant 1$ as the pulses cannot have a negative width, τ_m being the maximum deviation of the pulse width from its unmodulated value τ_c.

The p.d.m. wave contains a d.c. component, the original modulating frequencies and the harmonic series of carrier frequencies each of which has an infinite number of sideband pairs associated with it. In practice, not more than about three of these sideband pairs has significant amplitude so the original analogue signal may be recovered by passing the p.d.m. wave through a low-pass filter provided the carrier pulse train has a sufficiently high p.r.f. compared with f_m. The signal-to-noise ratio obtainable with p.d.m. is greater than that obtainable with p.a.m. due to the use of a wider transmission bandwidth, the improvement being similar to that of phase modulation compared with amplitude modulation. One form of pulse duration modulator is shown in Fig. 5.

Pulse position modulation may be considered to be the process of varying the position in time of the pulses in a periodic, rectangular, carrier pulse train in synchronism with, and in proportion to, the instantaneous variations of the modulating analogue signal. These modulated pulses cannot be advanced in time so that they may be considered as being displaced continuously in time with respect to the positions in time where the unmodulated

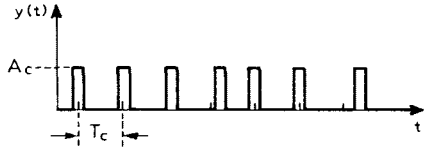


Fig. 6. Pulse-position modulation.

pulses would have occurred as indicated in Fig. 6. Pulse position modulation can be produced by generating a p.d.m. signal and feeding it into a monostable multivibrator. Figs 7 & 8 show two methods of generating a p.p.m. signal by using a pulse train $p(t)$ having a normal leading or trailing edge with a negative-or-positive slope ramp. The method of Fig. 8 avoids the need to generate a p.a.m. signal as part of the process.

With a sinusoidal modulating signal the "instantaneous" position of the pulses in time may be represented by $z(t) = f_c t + m_p \sin\omega t$ where m_p is the modulation index T_m/T_c, T_m being the peak deviation of pulses from their unmodulated position. The p.p.m. signal may be converted back to p.d.m. or p.a.m. to recover the modulating signal by means of a low-pass filter. Because noise has less effect on the position of pulses compared with its effect on the amplitude or edges of pulses, p.p.m. can provide a better

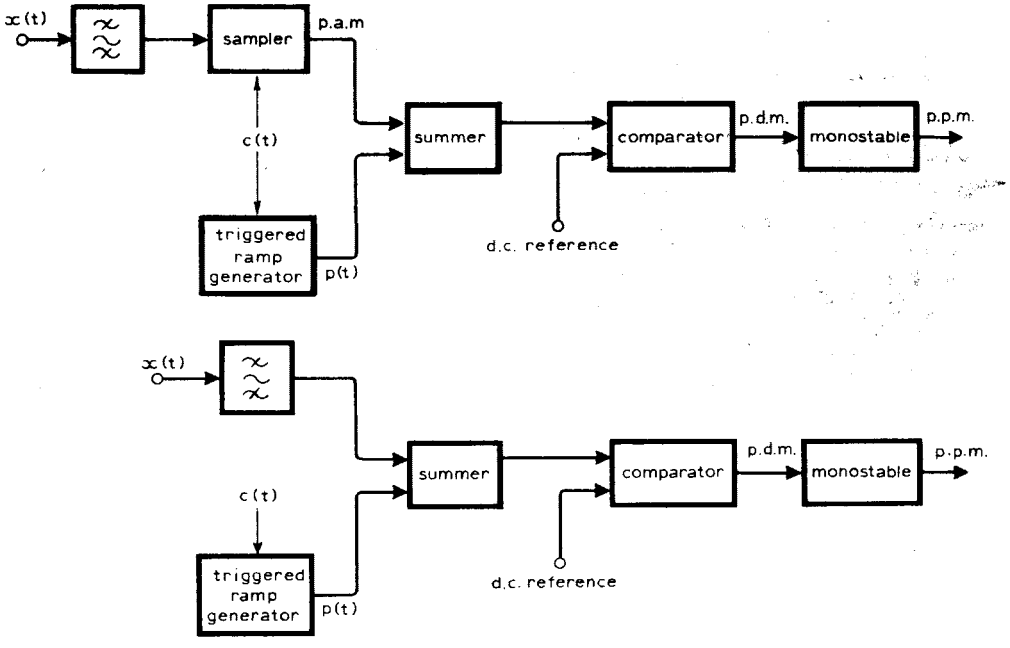


Fig. 7 (top). A pulse-position modulator.
Fig. 8. The p.a.m. is dispensed with in this system.

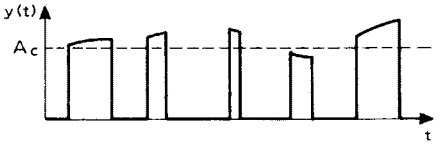


Fig. 9. Combined amplitude and width modulation for two information channels.

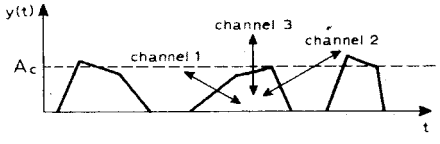


Fig. 10. Three-channel operation.

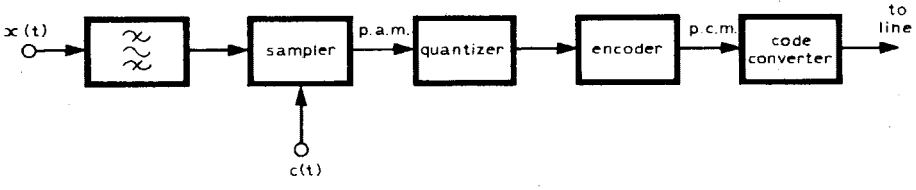


Fig. 11. A pulse-code modulator.

signal-to-noise ratio than either p.a.m. or p.d.m.

Sometimes it is useful to convey two modulating signals on the same pulse train without resorting to more complex time-division multiplexing techniques. For example, it is possible to first pulse-width modulate a pulse train with one signal and then pulse-amplitude modulate the p.d.m. wave with a second signal, the resulting p.d.m.-p.a.m. wave appearing like that shown in Fig. 9. Three signals may be made to modulate the same pulse train by using one source to vary the slope of the leading edge, one source to modulate the slope of the trailing edge and a third source to modulate the amplitude of the resulting pulses, as indicated in Fig. 10.

In pulse code modulation the analogue signal to be encoded is band-limited and passed to a sampling gate to produce p.a.m. The p.a.m. signal can have any instantaneous value within its allowed dynamic range and these variations are converted to a finite number of allowed levels by a quantizer. This process introduces an error into the signal, producing quantization noise which places a fundamental limit on the achievable signal-to-noise ratio. Each quantized p.a.m. sample is then encoded into a group of binary pulses to produce the p.c.m. signal. The number of pulses in each code group is determined by the number of allowed levels in the quantization scheme. For example, speech that has been band-limited to 0.3 to 3.4kHz and sampled at a rate of 8kHz is commonly represented by a 128-level quantization scheme so that a 7-bit code group is required since $128 = 2^7$.

To avoid transmission of the d.c. component in the binary coded pulses the p.c.m. signal is often converted to a bipolar form. Because only the presence or absence of a pulse, rather than its shape, needs to be determined at the decoder a transmission bandwidth of only

about $1/\tau_c$ is sufficient, where τ_c is the width of a pulse within a code group. The binary signals can be identically regenerated during transmission, so the overall signal-to-noise ratio obtainable with p.c.m. is much greater than that with the modulation methods already discussed.

With speech signals a further improvement is obtained by compressing its dynamic range at the encoder and expanding it at the decoder, a process known as companding. The basic processing in a p.c.m. transmitter is shown in Fig. 11 and that for a time-division multiplexed p.c.m. transmitter in Fig. 12.

Delta modulation (Δm), or differential p.c.m., does not transmit pulses related to the instantaneous value of the modulating signal at a sampling instant, but uses a one-bit code to convey information about the rate of change of the modulating signal between successive samples. The greater the rate of change of the analogue modulating signal the greater is the repetition rate of the output pulses.

The basic form of a delta modulator is shown in Fig. 13, where the pulse modulator transmits pulses from the pulse source to the integrator with one polarity if the comparator output is negative and with opposite polarity if the comparator output is positive. Thus the output from the integrator is a stepped waveform that "oscillates" about the continuous input signal waveform $x(t)$, and always attempts to keep this difference at a small value.

As a delta modulator transmits information about the rate of change of the analogue signal, an overload condition can be reached if the analogue signal changes too rapidly for the successive pulses, of fixed amplitude, to follow the change. The modulating signal can be recovered by feeding the delta modulated signal into an integrator followed by a low-pass filter. Although only a 1-bit code is used in delta modulation, the sampling or pulse rate has a minimum value that is higher than that required by the sampling theorem for p.c.m. For similar performance delta modulation generally needs a wider bandwidth than p.c.m. and the signal-to-noise ratio decreases with increasing frequency. However, the circuitry required in the encoder and the decoder is much simpler than for p.c.m.

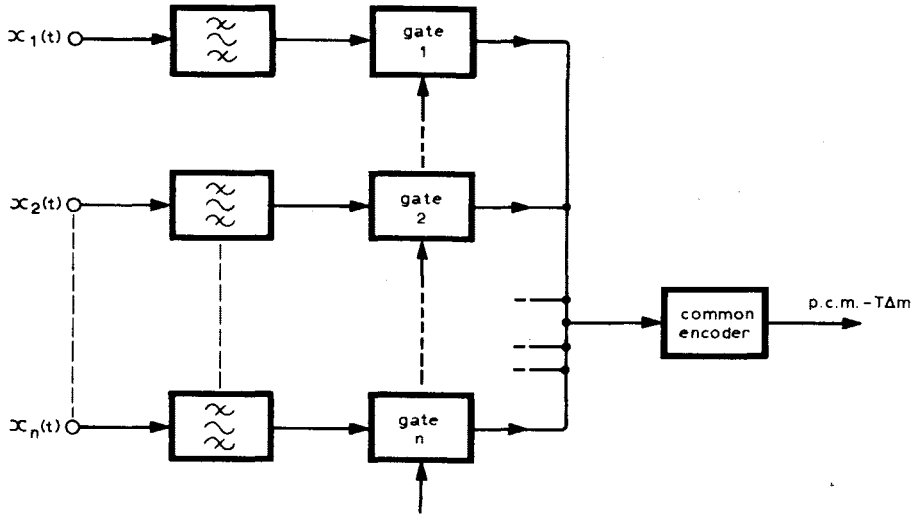


Fig. 12. Multi-channel operation in p.c.m. using time-division multiplex.

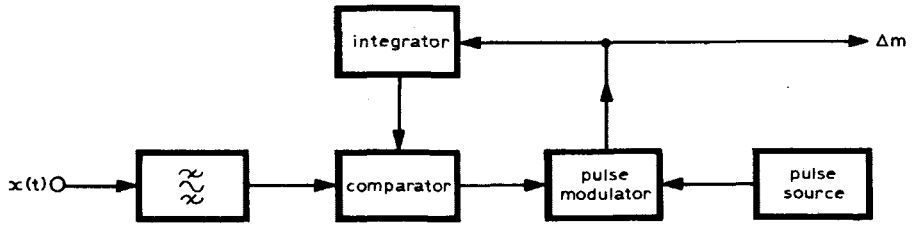
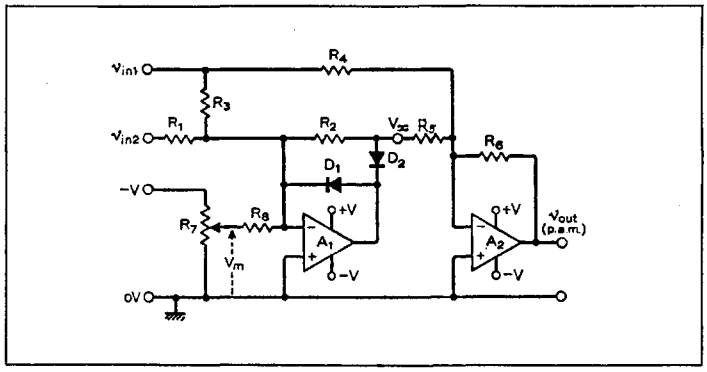
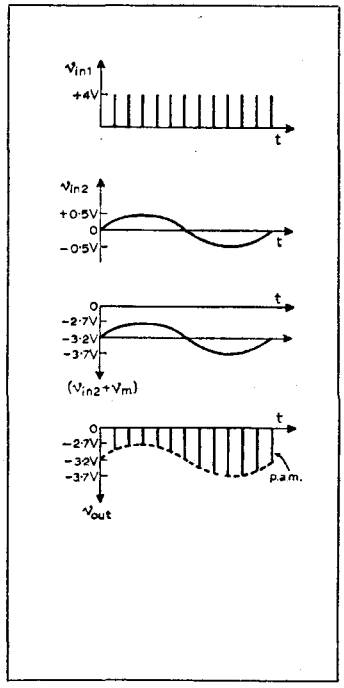


Fig. 13. The basic delta modulator.

Pulse amplitude modulator with precision limiter



Typical performance
Supply: ±15V, +3.4mA, −17mA
A_1, A_2: 741
R_1 to R_6, R_8: 10kΩ; R_7: 1kΩ linear
D_1, D_2: PS101
V_{in1}: 4-V positive pulse train, p.r.f. 10kHz, m-s ratio 1:10
V_{in2}: 1-V pk-pk sinewave, f = 1kHz
V_m: −3.2V
V_{out}: p.a.m. output—see diagrams

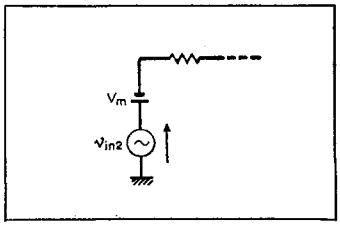


Circuit description
In most pulse amplitude modulator realizations the unmodulated carrier is in the form of a low duty-cycle, unidirectional pulse train. So with a symmetrical modulating signal the amplitude of the carrier pulses may be varied over the maximum range of zero to twice their unmodulated value with 100% modulation. The narrower the carrier pulses the greater the conservation of power but this is achieved at the expense of a wider transmission bandwidth for defined performance, as the shape of the pulse tops must be preserved.

A common method of producing p.a.m. is by the use of a diode bridge that allows and prevents transmission of the modulating signal under the control of a carrier switching pulse train. For many applications this technique is acceptable although its accuracy is determined by the characteristics of the diodes. When more precise p.a.m. is required the effects of the diodes can be greatly reduced by using a precision full-wave rectifier, as shown above which effectively reduces the forward diode p.d. by the open loop gain of the operational amplifier A_1.
When V_{in1} is a unidirectional positive pulse train, V_{in2} is a symmetrical modulating signal and V_m is negative, the output (V_x) from A_1 is zero when $(V_{in2}+V_m)$ is less than V_{in1} and is $-(V_{in1}+V_{in2}+V_m)$ when $(V_{in2}+V_m)$ exceeds V_{in1}. The p.a.m. output from the summing amplifier A_2 is $-V_{in1}$ when $V_x = 0$ and is $(V_{in2}+V_m)$ when V_x is less than zero.

Component changes
Useful range of supply about ±4 to ±18V with suitable adjustment of V_{in1}, V_{in2} and V_M levels.
V_{in1} (max): 7.5-V pulses
V_{in1} (min): 3.5-Vpulses
$|V_M$ (max)$|$: 3.6V
$|V_M$ (min)$|$: 2.8V
Max. p.r.f. of V_{in1}: 70kHz (mark-space ratio of approximately unity required to retain output p.a.m. waveshape).

Circuit modifications
To produce a wholly positive pulse amplitude modulated output waveform instead of a purely negative output, the following changes should be made: V_{in1} is changed to a unidirectional negative pulse train, diodes D_1 and D_2 are connected with reverse polarity and R_7 is connected to the positive supply rail.
With a negative p.a.m. output signal the alternative biasing arrangement shown above may be used, i.e. a d.c. bias source can be connected in series with the modulation source, V_{in2}, and R_7 and R_8 removed. To produce a purely positive p.a.m. output waveform with this arrangement, the polarity of the V_m bias source and of D_1 and D_2 is reversed as well as that of the carrier pulse train V_{in1}.

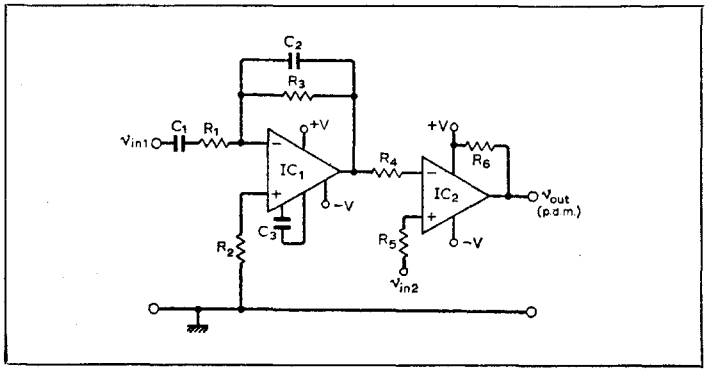


Further reading
Graeme, J. G., Tobey, G. E. and Huelsman, L. P. Operational Amplifiers—Design and Applications, McGraw-Hill, 1971, pp.400/1.
Applications Manual for Operational Amplifiers, Philbrick/Nexus, 1965.
Cattermole, K. W., Transistor Circuits, 2nd edition, Heywood 1964.

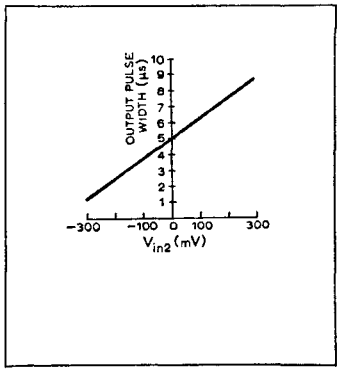
Cross references
Series 15, cards 3 & 7.
Series 4, card 3.

wireless world circard

IC pulse duration modulator



Typical performance
Supply: ±15V, ±12mA
IC_1: 748, IC_2: 311
R_1, R_2, R_4, R_5: 1kΩ
R_3: 100kΩ, R_6: 2.2kΩ
C_1: 33nF, C_2: 1nF, C_3: 30pF
V_{in1}: 400mV pk-pk square wave at 100kHz
V_{out}: 28V pk-pk



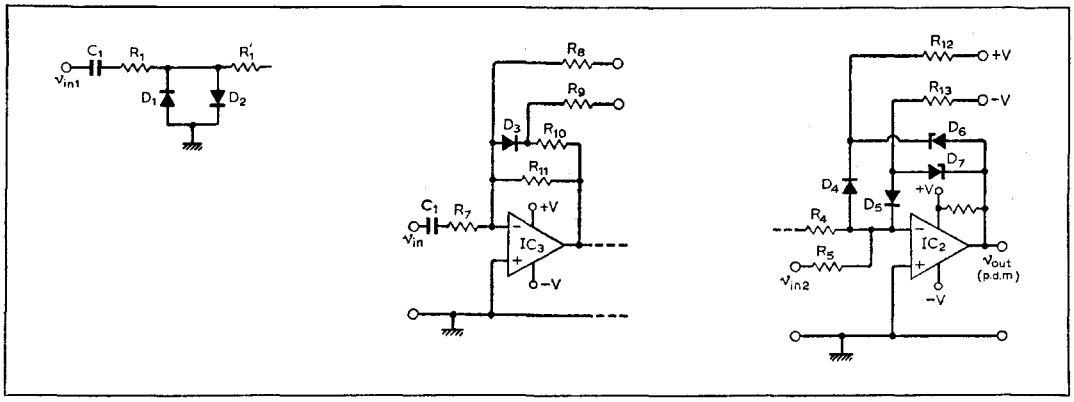
Circuit description
In pulse width modulation, the unmodulated pulse train is often in the form of a square wave having a constant pulse repetition rate. The duty cycle of this square wave is then varied under the control of a d.c. or low-frequency modulating signal. The source waveform of the carrier signal may take various forms, e.g. a sinewave which is converted to a square wave for application to an integrator and comparator. The integrator converts the square wave to a triangular wave which is applied to one input of the comparator. In the absence of modulation, which is applied to the other input of the comparator, the output is a periodic pulse-train or square wave having a fixed duty cycle.
With a modulating signal applied to the second comparator input, the duty cycle of the output pulse train varies in sympathy with changes in the modulating waveform's instantaneous value, as the comparator's output state changes when the modulation input level exceeds or falls below that of the square wave applied to its other input.
The above diagram shows an integrated circuit version using a voltage comparator and a general-purpose, externally-compensated operational amplifier for the integrator. Capacitor C_1 removes any d.c. component from the input square wave and R_3 provides d.c. negative feedback to define the mean output voltage of the triangular wave. The overall linearity obtainable is a function of the linearity of the triangular waveform applied to the comparator.

Component changes
Supply variation: ±2.2 to ±18V
$f_{max} \approx$ 200kHz with components shown. Change integrator time constant for different carrier p.r.fs. Unidirectional pulse width modulation can be produced by feeding the integrator with a train of narrow pulses and hence a sawtooth is applied to the comparator.
The comparator may be fed directly from a triangular or sawtooth wave source.

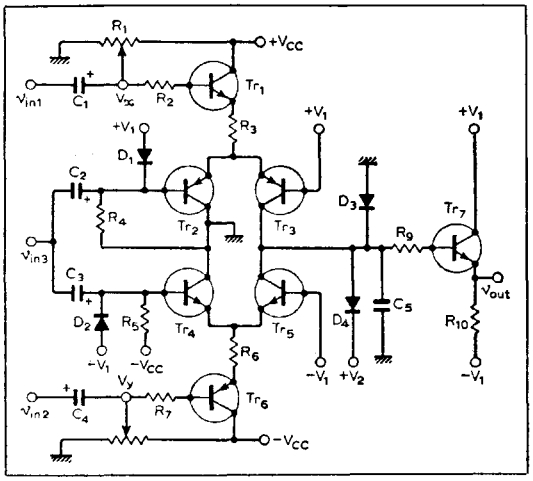
Circuit modifications
If source voltage is large, the input to the integrator may be clamped using a pair of back-to-back diodes (PS101, 1N914, etc.) as shown left.
When the available carrier source waveform is in the form of a sine wave it may be converted to a suitable form for application to the integrator by the circuit shown centre which amplifies and clips the output signal applied to the integrator. The input coupling capacitor of the original integrator can be dispensed with. Suitable components could be IC_3: 741; D_3: small silicon diode; R_7: 100kΩ; R_8, R_9: 1.5kΩ; R_{10}, R_{11}: 1kΩ. Resistors R_8 and R_9 can be trimmed to provide a symmetrical triangular wave at the output of the integrator.
Instead of allowing the comparator's output to swing between approximately ±V its excursions may be limited by including a pair of back-to-back zener diodes as shown right.

Further reading
Eimbinder, J. (Ed.), Linear IC's: Theory and Applications, Wiley, 1968, pp.15-7.
Graeme, J. D. and Tobey, G. E., Operational Amplifiers. McGraw-Hill, 1971, pp.412/3.

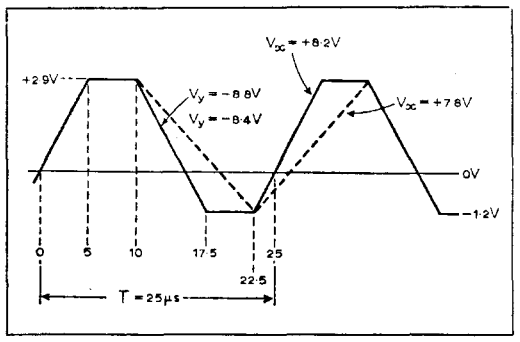
Cross references
Series 15, cards 4, 6, 7, 8, 10 & 11.
Series 2, card 1.
Series 3, card 1.



Variable slope modulator



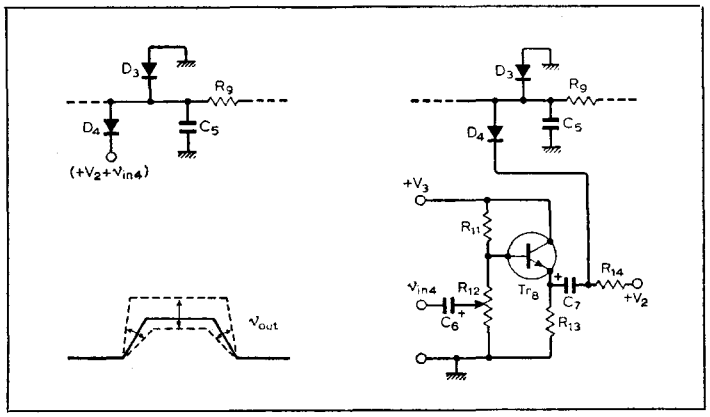
Typical performance
Supplies: ±25V, +2mA, −5mA
±V_1, ±6V, +14mA, −13mA
+V_2= +3V, 14mA
Tr_1, Tr_4, Tr_5, Tr_7: BC125
Tr_2, Tr_3, Tr_6: BC126
Diodes: PS101; R_1, R_4, R_8, 10kΩ
R_2, R_7: 2.7kΩ; R_3, R_6: 1.5kΩ
R_5: 27kΩ
R_9: 100Ω; R_{10}: 820Ω
C_1 to C_4: 50μF
C_5: 1nF; V_x +8.2V
V_y −8.8V
v_{in3} 1V pk-pk square wave, p.r.f.: 40kHz
See v_{out} waveform opposite for v_{in1} and v_{in2} available range



Circuit description
When a capacitor is charged or discharged with a constant current, the p.d. across it changes linearly with time.
In the circuit shown the unmodulated output pulse train is in the form of a trapezoidal wave having the same p.r.f. as the input square wave (V_{in3}) and having leading and trailing edge slopes determined by V_x and V_y respectively.
When V_{in3} goes positive, Tr_3 is switched on and passes the constant current from Tr_1 to charge C_5. The magnitude of this current, and hence the rate of rise of V_{C5}, is set by R_1 and is linearly related to V_x.
When V_{in3} goes negative, Tr_5 discharges C_5 with a constant current through Tr_6. The magnitude of this current is set by R_8 and is linearly related to V_y.
Thus the slopes of the leading and trailing edges of the pulse-train output waveform from the emitter follower Tr_7 are controlled by V_x and V_y respectively, which can be made to vary independently by sources of modulation V_{in1} and V_{in2}. The p.r.f. of the carrier pulse train V_{in3} is much greater than the modulating frequencies, so the square-wave half-cycles may be considered to be alternately sampling the signals V_{in1} and V_{in2}. During the sampling intervals, the instantaneous values of these signals therefore vary the slopes of the output waveform about their mean positions set by R_1 and R_8. Positive peaks of V_{out} are clamped by D_4 and +V_2.

Component changes
v_{in1} (max) = v_{in2} (max) ≈ 760mV (1kHz)
Minimum frequency of v_{in1} and v_{in2} < 10Hz
v_{in3} (min) ≈ 700mV pk-pk
Max. p.r.f. of v_{in3} ≈ 200kHz with C_5= 47pF
Min. duty cycle of v_{in3} 30%
Min. load resistance ≈ 220Ω
Vary +V_2 to set v_{out} positive peak in range 0 to +3.5V
Vary v_{out} leading edge slope with +V_1 in range +3 to +6.6V
Vary V_{out} trailing edge slope with −V_1 in range −6 to −7.5V
Reduce R_3 to reduce rise time of v_{out}
Reduce R_6 to reduce fall time of v_{out}

Circuit modifications
If the dynamic range of the modulating signals is restricted, the variations in the slopes of the leading and trailing edges of the output waveform will never be sufficient to cause the latter to assume a "triangular" pulse shape. With this restriction, V_{out} is a constant-amplitude trapezoidal pulse train with its positive peaks clamped by D_4 at +V_2. Hence, a third signal (V_{in4}) may be superposed on the +V_2 supply to provide trapezoidal-pulse amplitude modulation as shown left with V_{out} assuming the variations indicated below the circuit. One method of modulating the clamp voltage is shown right which uses an emitter-follower. All channels are no longer independent of each other since the maximum value of V_{C5} is determined by the charging current to C_5 which in turn depends on V_{in1}. Transistor Tr_8 may be a general-purpose type, typical component values being: V_3 +9; R_{11} 100kΩ; R_{12} 47kΩ; R_{13}, R_{14} 470kΩ; C_6, C_7 50μF.

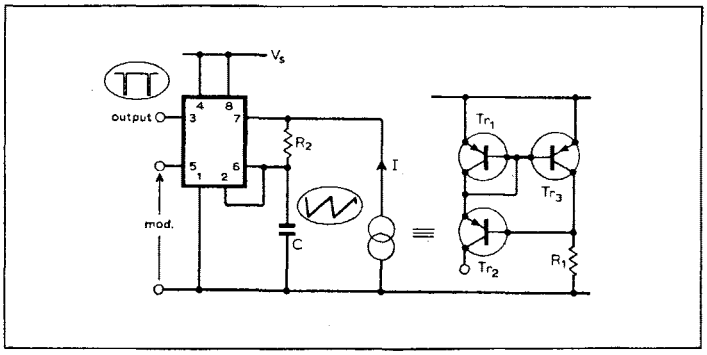


Further reading
Lee, D. N. Rise-time adjustment independent of fall time, *Electronics*, vol. 38, 1965, p.76.
Kruse, E. K. and Dobbs, D. Triple-channel modulation of a single pulse train. *Electronic Engineering*, April 1971, pp.36/7.

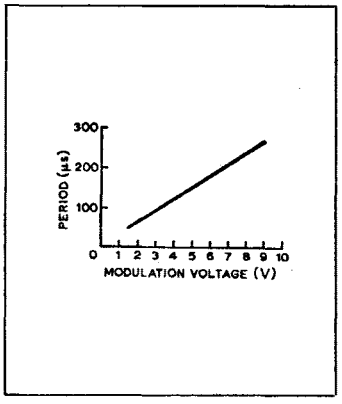
Cross reference
Series 15, card 7.

wireless world circard

Pulse modulation using 555 timer



Typical performance
IC: NE555V
Supply: +12V
C: 4.7nF
R_2: 1kΩ, I=100μA*
v_{mod}: 5V
Period: 150μs
Output: Duration of low-state 6μs,
for load resistance 1kΩ
*Current may be provided by any constant-current circuit; that shown is one example for which Tr_1 to Tr_3 are elements of IC type CA3084; R_1=47kΩ.



Circuit description
Modulation of pulse period or repetition-rate may be carried out independently by control of the threshold voltages or the charging rate of the timing capacitor in astable circuits.
In the 555 timer a constant-current charging C gives a linear ramp. Upper threshold is equal to the potential at pin 5, v_{mod}, and the lower threshold to $v_{mod}/2$ by virtue of the internal potential divider. The capacitor is thus charged through $v_{mod}/2$ at a constant rate, giving a period that is a linear function of the modulation potential provided that the discharge time is very short. This indicates a low value for R_2, which may be reduced to zero (except where large values of C would result in the 200mA current limit of the discharge transistor being exceeded for long periods).
The constant current is critical to the linearity, since for the usual astable with a resistor from pin 7 to V_S, the charging rate varies throughout the cycle. For example, as v_{mod} approaches V_S the fractional increase in period is greater than that of the modulation voltage. One possible constant-current circuit is the enhanced current mirror. This requires a low terminal p.d. for the constant-current transistor Tr_2, i.e. the constant-current stage does not impose a limit on the upper threshold/modulation voltage that can be used. Since the charging current is proportional to the supply voltage (ignoring V_{be} effects) the frequency stability is supply-dependent, in contrast with the basic mode where increased threshold voltages and charging currents neutralize each others' effects on frequency.

Component changes
V_S: +4.5 to +18V
C: 100p to 100μF. Taken in conjunction with suitable charging currents, the frequency range extends from ≪ 1Hz to > 100kHz..
I: May be as low as 1μA for very long periods, but should exceed 10μA for reasonable stability of period. Up to 10mA permissible for high frequency generation.
R_2: Should limit discharge current at pin 7 to 200mA. May be reduced to zero for low values of C in most cases, though peak currents exceed this rating for very short times. This reduces duration of low-state of output towards zero.
V_{mod}: For V_S of 12V, v_{mod} may range from 1.5 to 9V. The minimum value is of the same order at other supply voltages, while the upper is about 70% of V_S or greater for V_S > 10V. At low supply voltages internal V_{be} drops restrict the range further.

Circuit modifications
In circuits based on capacitor charging to define the period of the waveform, then constant current charging linearizes the waveform and, for defined switching points, the period will be inverse to the current, i.e. the frequency will be a linear function of the current. A simple adaptation is to apply the modulation to the current generator—a simpler current mirror is shown as an example with the diode p.d. introducing an offset to the v_{mod}/frequency graph together with some drift. Again, $R_2 \rightarrow 0$ minimizes flyback-time errors.
If a clock generator is applied to the monostable in Fig. 2 then the output is at the clock frequency but with a pulse width controlled by the modulation voltage, i.e. p.d.m. Again, for linear modulation the waveform at C has to be linearized by the addition of a constant-current stage.
The clock interconnection from a previous 555 may be as shown. The circuit may be conveniently implemented with a dual 555, but any other astable giving a negative-going edge approaching supply-voltage magnitude may be used.

Cross references
Series 15, cards 2, 4, 7, 8, 10 & 11.
Series 3, card 9.

Fig. 1

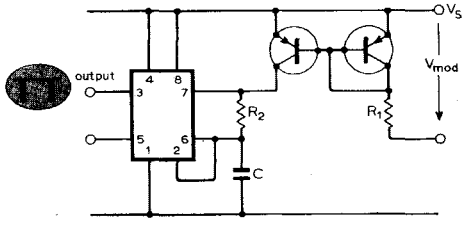


Fig. 2

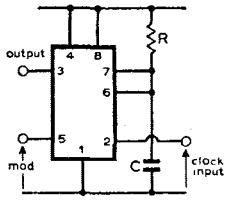
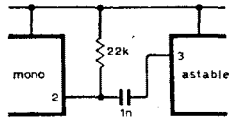
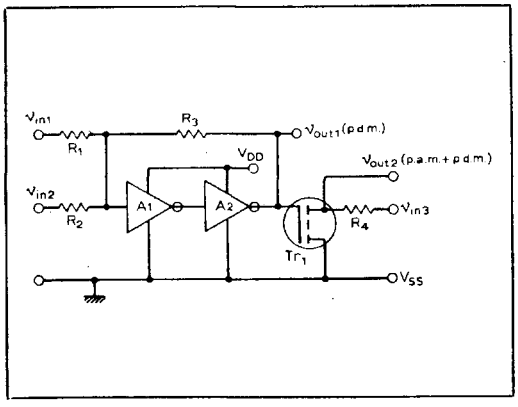


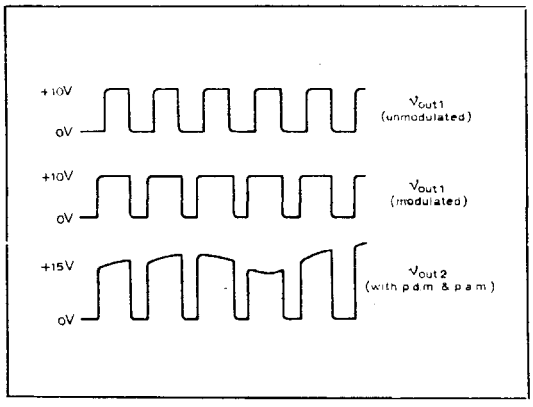
Fig. 3



CMOS pulse amplitude/duration modulator



Typical performance
V_{DD}: +10V, 830μA; V_{SS}: 0V
A_1, A_2: $\frac{1}{6}\times$CD4007
Tr_1: 1/6×CD4007; R_1, R_2: 1MΩ
R_3: 10MΩ; R_4: 10kΩ
v_{in_1}: 11V pk-pk 50kHz triangular wave superposed on +2.1V d.c. bias to make v_{out_1} a square wave
v_{in_2}: Pulse-width modulation source is 500mV pk-pk at 1kHz
v_{in_3}: Pulse-amplitude modulation source 2V pk-pk at 2kHz superposed on a d.c. bias of +5V

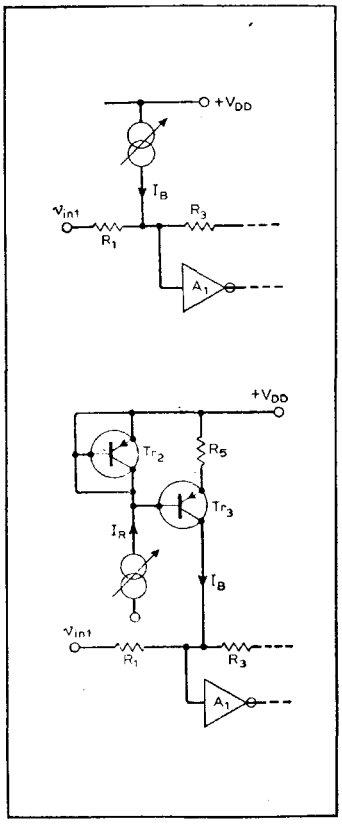


Circuit description
In the circuit shown a c.m.o.s. Schmitt-trigger circuit is formed by using A_1 and A_2 as a cascaded pair of inverters with positive feedback. In the absence of modulation, (V_{in_2}= 0) the Schmitt switching action is determined by the ratio R_3/R_1 and V_{in_1}. Provided R_3/R_1 is less than the forward gain in the linear region of the inverters, the switching action of the Schmitt follows the threshold crossings of the triangular wave input, V_{in_1}. With a 10-V supply the Schmitt switches to $+V_{DD}$ when V_{in_1} exceeds about +2.4V and switches back to V_{SS} (0V) when V_{in_1} falls below about +1.85V.
For the purposes of pulse-width modulation it may be required to produce an un-modulated square-wave output (V_{out_1}) and this may be obtained by superposing V_{in_1} on a suitable d.c. bias (+2.1V) to produce unity mark-to-space ratio. This ratio may then be varied by causing the switching times of the Schmitt to be controlled by the p.d.m. signal (V_{in_2}) which is conveniently fed to the A_1 input through R_2. The p.d.m. signal is fed to Tr_1 which provides a similar output waveform but with its positive peak amplitude determined by the voltage to which R_4 is returned. Hence by returning R_4 to a second source of modulation (V_{in_3}) a waveform (V_{out_2}) results which is simultaneously modulated in both amplitude and duration.

Component changes
Useful range of V_{DD} +3 to +15V
Maximum useful v_{in_1} frequency 150kHz
Maximum pulse width modulation is achieved with $v_{in_2}\approx$ 900mV pk-pk
Maximum pulse amplitude modulation is obtained with $V_{in_3}\approx$ 12V pk-pk superposed on a d.c. bias of +9V

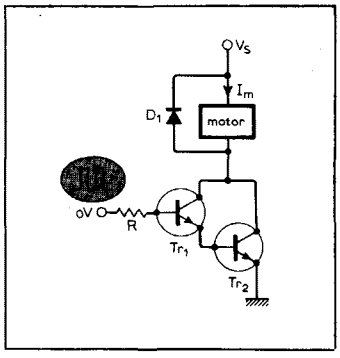
Circuit modifications
The d.c. bias on which V_{in_1} is superposed to provide a square-wave output may be dispensed with if a unity mark-to-space ratio is not required. If a low-duty-cycle pulse train output is required, the d.c. bias may be removed and the amplitude of the triangular wave (V_{in_1}) reduced so that it is only slightly in excess of the upper threshold level of the Schmitt but sufficient to allow modulation.
An approximately square-wave output can be obtained without a d.c. bias if the input triangular wave has a much larger amplitude.
When a d.c. bias is used to control the unmodulated mark-to-space ratio of V_{out}, a constant-current source may be used for this purpose as shown above. One method is to use an integrated circuit current mirror to provide the constant-current bias to set the unmodulated duty cycle as Shown right. Negative feedback obtained by the inclusion of the emitter resistor R_5 raises the output impedance of the current mirror above that of a common-emitter stage.
Pulse duration modulation may be obtained by controlling I_R with the modulation signal.

Further reading
Schmidt, B. Schmitt trigger design uses CMOS logic, *Electronic Design*, vol. 20, April 1972, p.72.
Hart, B. L. Current generators, *Wireless World*, vol. 76, 1970, pp.511-4.

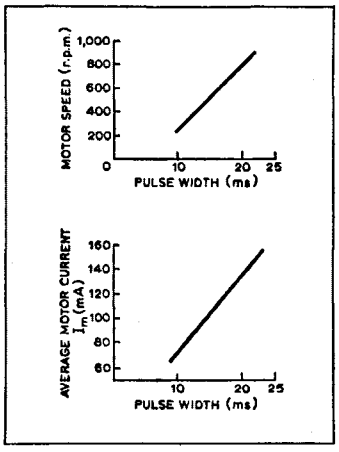


Cross references
Series 15, cards 1 to 6, 8 & 10.
Series 2, card 3.
Series 6, card 4.

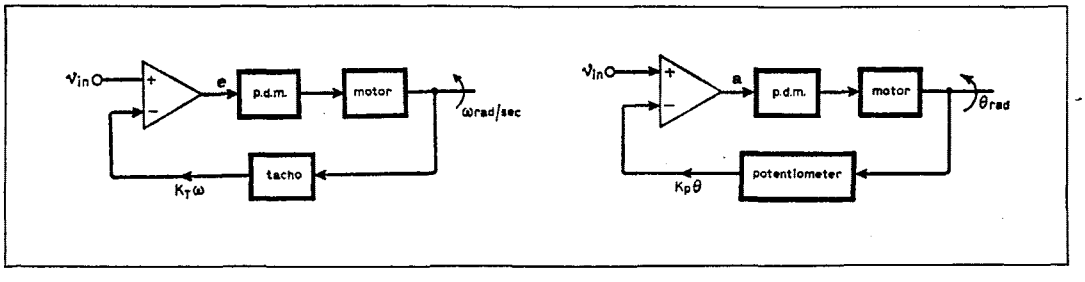
DC motor control using p.d.m.



Performance data
Supply: +40V
D_1: 1N4004
Tr_1: BFR41
Tr_2: TIP3055
R: 1kΩ
V_p: 6V
Pulse frequency: 40 per sec
Motor: 240V, 0.1-h.p.
6500 rev/min universal motor



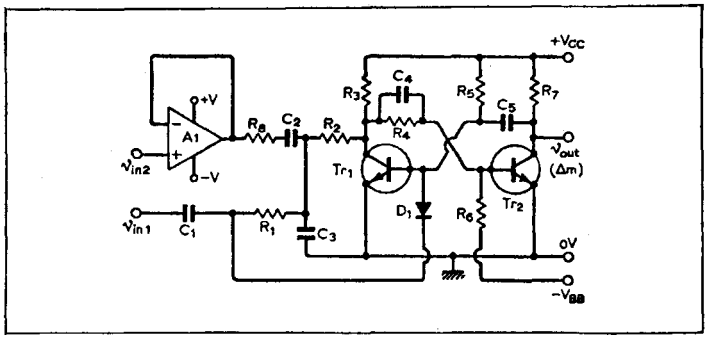
Circuit description
Circuit shows a pulse driven high-current switch Tr_1 and Tr_2 controlling the voltage applied to a motor. Basic principle involved is identical to that for thyristor driven motors viz that the average applied voltage controls the motor speed. During the pulse mark time Tr_2 conducts and the supply is able to supply current to the motor and during the pulse space time Tr_2 does not conduct and the supply is unable to deliver current. Clearly the greater the mark to space ratio of the pulse train the greater is the average applied voltage and with it the average motor current, I_m. Graphs show the results obtained. The linearity of these results, despite the fact that the motor was being used well outside its specifications, indicates the potential usefulness of the scheme.
Values of V_p and R are not critical so long as they provide sufficient base drive to Tr_1 to effect satisfactory switching and at the same time do not destroy Tr_1. In this case since we are switching currents less than 200mA and the current gain of Tr_1 and Tr_2 is greater than 1000 then the base drive to Tr_1 should be of the order of 0.2mA. Considerably less may suffice. The pulse frequency is not critical either. Maintaining a constant mark-space ratio, i.e. maintaining a constant average voltage, the motor ran at the same speed when the frequency was varied from 40Hz up to at least 4kHz. At higher frequencies lack of switching speed in the transistor caused the motor speed to change.
Diode D_1 is the diode normally necessary with motors to prevent damage due to *Ldi/dt* effects.
Motor speed control by means of a voltage can be obtained by using the p.d.m. section of the p.p.m. shown in card 4; alternatively, the discrete p.d.m. shown in card 10 can be used with alterations to allow for the use of n-p-n rather than p-n-p transistors.
A possible closed-loop speed control scheme is shown left. This will, of course, reduce the effects of nonlinearities, disturbances, etc. If the motor and p.d.m. are known in advance the maximum value of e is fixed and this effectively dictates v_{in}, k_T and the differencing amplifier.
Diagram right shows a position control system; the output transducer need not, of course, be a potentiometer. This scheme has a considerable advantage in performance terms over conventional continuous control systems, because the steady state error in response to a step input in the presence of coulomb friction is eliminated. This is important in small motors in which brush friction is frequently a large effect when compared with the maximum torque developed by the motor. In continuous systems the torque produced is proportional to the actuating signal 'a' and when this torque is less than the coulomb friction torque the motor shaft stops. Hence, 'a' can be non zero. However, if 'a' is feeding a p.d.m. as shown right, the motor develops maximum torque so long as 'a' is non zero, albeit for shorter and shorter intervals as 'a' reduces. Since the maximum torque is greater than the coulomb friction torque the motor can only come to rest when 'a' is zero.



Further reading
Ghonaimy, M. A. R. and Aly, G. M. Phase-plane method for analysis of pulse-width modulated control systems. *International Journal of Control*, vol. 16, no. 4, 1972, pp.737-50.
Pulse-width modulation for d.c. motor speed control, *Semiconductors* (Motorola) vol. 2, no. 2, 1971, pp.36-8.

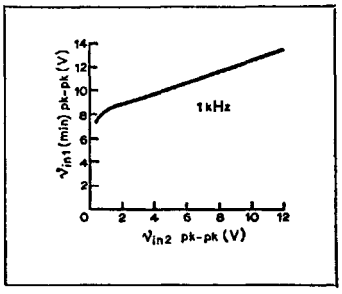
Cross references
Series 15, cards 2, 4, 6, 7 & 10.

Delta modulators



Typical performance
Supply (±V): ±12V, +22mA, −2.2mA; $+V_{CC}$: +12V
$-V_{BB}$: −5V at 200nA
A_1: 741; Tr_1, Tr_2: BC125
D_1: PS101
R_1: 10kΩ; R_2, R_3: 1kΩ
R_4: 4.7kΩ
R_5: 10kΩ; R_6: 22kΩ; R_7: 330Ω
R_8: 100Ω
C_1: 50pF; C_2: 1μF; C_3: 47nF
C_4: 220pF; C_5: 1nF
v_{in_1}: 10V pk-pk pulses, p.r.f. 50kHz, duty cycle 10%
v_{in_2}: 2V pk-pk sinewave at 1kHz
v_{out} (unmodulated) 0 to +12V pulses, p.r.f. 50kHz, m-s ratio 1:3
See overload characteristic

Circuit description
A delta modulator encodes an analogue signal into a train of binary pulses that represent the difference between the levels of the input signal at successive sampling times. The encoded pulse train has a repetition rate governed by the rate of change of the analogue signal; the greater this gradient the higher the density of the output pulses produced.
The delta modulator shown above employs a monostable multivibrator with C_5 controlling the monostable period and C_4 acting as a "speed-up" capacitor. The voltage follower A_1 is used as a low-output-impedance buffer between the modulation source and the junction of C_2 and R_2, R_8 being included to reduce ringing on the pulses at this junction.
In the stable state Tr_1 is on and Tr_2 is off so that a complementary V_{out} waveform is fed to C_3 via R_2. This signal is added to the modulating signal at the junction of R_2 and C_2. This composite voltage is compared with a threshold voltage to determine whether the monostable will be triggered to its quasi-stable state. If the composite voltage across C_3 is less than the threshold, the differential clock pulses successfully trigger the monostable via D_1 until the voltage across C_3 is raised sufficiently to exceed the threshold. When this occurs the clock pulses fail to trigger the monostable circuit and C_3 discharges until the modulating signal input exceeds the voltage on C_3.



Component changes
$+V_{CC}$ (min): +7.4V
$-V_{BB}$ is non-critical: ensures Tr_2 off-state
Max. p.r.f. with above components: 130kHz
v_{in_1} (min): 8.8V pk-pk with 1μs pulse width and v_{in_2} 2V pk-pk
Min. pulse width of $v_{in_1} \approx$ 900ns, with 10V pk-pk amplitude and v_{in_2} 2V pk-pk
Adjust C_5 for required v_{out} period

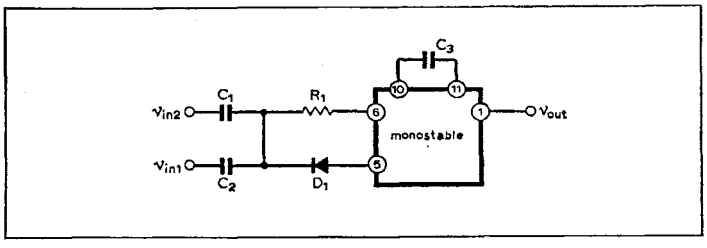
Circuit modification
Another monostable form of delta modulator using an integrated circuit is shown above where the width of the output binary pulses is controlled by C_3. The analogue signal to be encoded (V_{in_2}) and the clock pulses (V_{in_1}) are fed to the junction of R_1 and D_1 via capacitors C_1 and C_2 respectively.

As V_{in_2} would normally be a low-output-impedance source the complementary output voltage waveform (pin 6) is integrated by R_1 and C_1. Clock pulses are fed to the monostable via D_1 after being differentiated by C_2 and R_1.

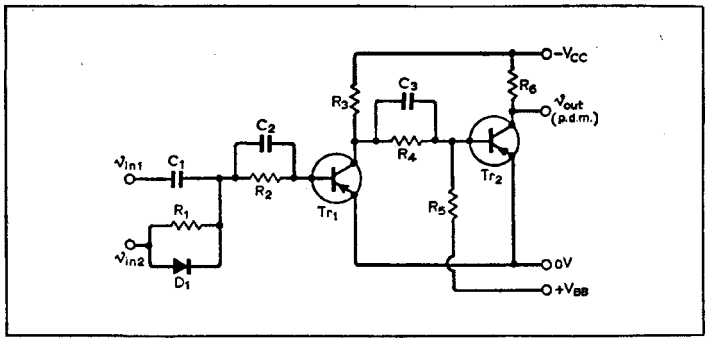
If the junction of C_1 and R_1 is at a voltage below the threshold set by the amplitude of the clock pulses, their differentiated edges will trigger the monostable, producing a positive pulse into R_1. If this junction voltage is above the threshold the clock pulses are prevented from triggering the monostable. Junction threshold voltage is correctly adjusted by varying the amplitude of the clock pulses to cause the output pulse rate to be half the clock pulse rate. Typical components are: monostable—DTμL9951; R_1 10kΩ; C_1 50nF; C_2 50pF.

Further reading
Steele, R. and Thomas, M. W. S. Two-transistor delta modulator, *Electronic Engineering*, Sept. 1968, pp.513-6.

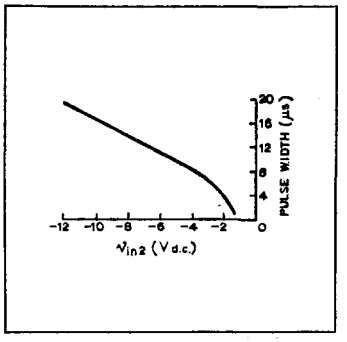
Cross reference
Series 15, card 11.



DC amplifier/pulse duration modulator



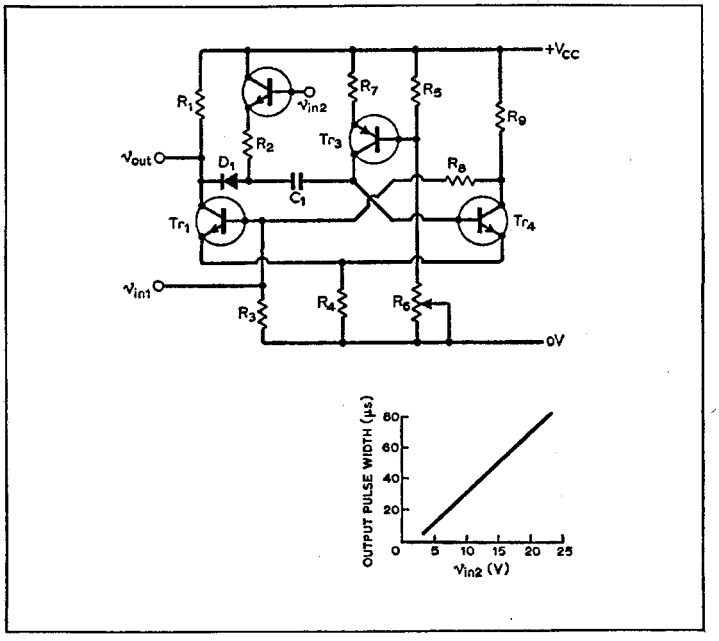
Typical performance
Supplies: $-V_{CC}$: −12V 9.7mA
$+V_{BB}$: +12V 1.8mA
Tr_1, Tr_2: BC126
D_1: PS101; R_1: 100kΩ
R_2: 22kΩ; R_3: 2.7kΩ
R_4: 470Ω; R_5: 6.8kΩ; R_6: 1kΩ
C_1: 100nF; C_2: 100pF
C_3: 470pF
V_{in1}: 3V pk-pk sawtooth at 50kHz



Circuit description
In the above circuit C_1, R_1 and D_1 act as a d.c. restorer where the peaks of the sawtooth wave (V_{in1}) are clamped to a level determined by V_{in2}. In the usual application of such a circuit, V_{in2} is a fixed d.c. level and provided that the time constant C_1R_1 is very much greater than the periodic time of V_{in1} the latter will be clamped to the desired level.
If a modulating signal, which varies much more slowly than V_{in1}, is used in place of a fixed value of V_{in2} the level to which the peaks of the sawtooth wave is clamped will be controlled by the variations in V_{in2}. Thus, the voltage appearing at the junction of C_1 and R_1 is effectively due to the addition of V_{in1} and V_{in2}.
This combined signal is applied to the input of a two-stage, high-gain, d.c. amplifier containing Tr_1 and Tr_2 which has the same form as a Schmitt trigger but with the hysteresis removed. When the input to this amplifier is large enough to change the state of Tr_1 an output pulse is obtained at Tr_2 collector having an amplitude almost equal to that of the $-V_{CC}$ supply. As the switching threshold is controlled by the level of the modulating signal the duration of the V_{out} pulses is linearly related to V_{in2} over a wide range of the latter—superposed on a suitable negative d.c. bias. Hence, V_{out} is a pulse duration modulated pulse train.

Component changes
With a restricted range of pulse width variation $-V_{CC}$ and $+V_{BB}$ have useful minimum values of about −2 and +2V respectively.

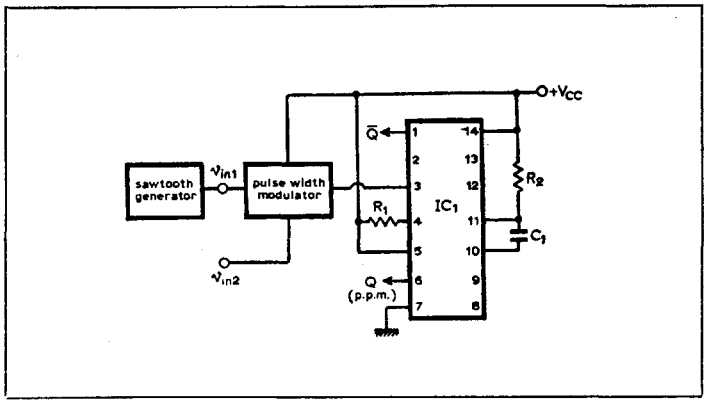
Circuit modifications
If required, the modulating signal V_{in2} may be superposed on a positive d.c. bias if the polarity of D_1 is reversed.
If n-p-n transistors are used in the d.c. amplifier, polarity of the supplies and that of D_1 should be reversed.
A different approach to linear pulse-duration modulation is shown here. This circuit uses a monostable multivibrator to set the width of the unmodulated output pulses which have a repetition rate determined by that of the input positive pulse train, V_{in1}. Output pulse width is a linear function of the modulating signal (V_{in2}) applied to the base of Tr_2 which serves as a constant-current generator. With Tr_1 off and Tr_4 on and saturated D_1 is reverse-biased, if $V_{in2} < V_{CC}$, and C_1 charges. When Tr_1 is switched on by a V_{in1} pulse the charge on C_1 changes at a rate determined by the constant-current transistor Tr_2 until the base-emitter voltage of Tr_4 rises sufficiently to switch Tr_4 on and hence Tr_1 off. Capacitor C_1 is now isolated from Tr_1 collector which therefore switches off rapidly. Typical performance is indicated left, with $+V_{CC}$: +24V; R_1, R_9: 750Ω; R_2: 7.2kΩ; R_3: 1kΩ; R_4: 30Ω; R_5, R_7: 9.1kΩ; R_6: 100kΩ; R_8: 3kΩ; C_1: 1nF.



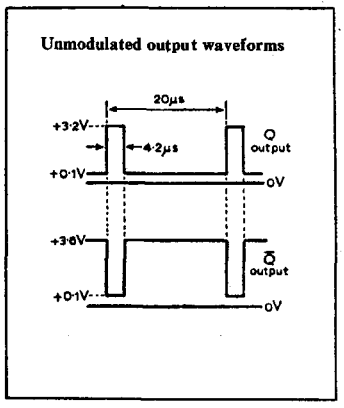
Further reading
Hart, E., Generator permits infinite pulse-width variation, in "100 Ideas for Design", no. 5, Hayden, 1965, p.5.
Hemingway, T. K., Electronic Designer's Handbook, Business Publications, 1967, pp.17/9.
Hughes, R. S. Pulse width vs. control voltage made linear by generator in "100 Ideas for Design", no. 5, Hayden, 1965, p.76.

Cross references
Series 15, cards 2, 4, 6, 7, 8 & 11.

Pulse position modulator



Typical performance
Supply: +5V, +23.5mA
IC_1: SN74121N
R_1, R_2: 1kΩ; C_1: 6.8nF
Pulse duration modulator: see card 10 with Tr_1, Tr_2 BC125 (n-p-n) transistors, +Vcc: +5V; −V_{BB}: −5V and D_1 polarity reversed.
V_{in1}: 3V pk-pk sawtooth at 50kHz
V_{in2}: Sinewave modulation superposed on a direct bias of +3.75V to give square wave output from modulator

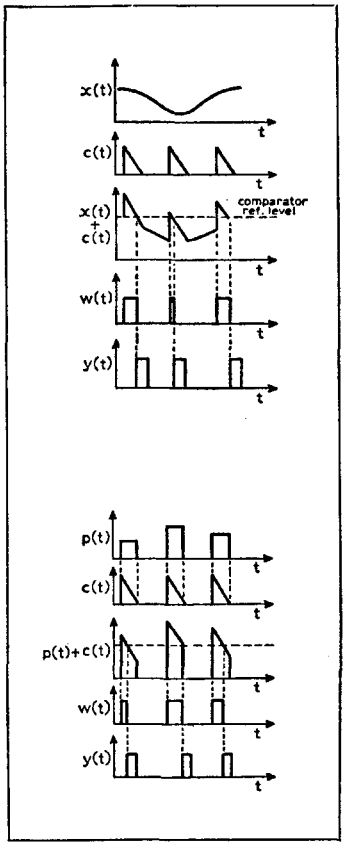


Circuit description
The pulse-position modulator employs a pulse-duration modulator feeding a t.t.l. integrated-circuit monostable package. Many different pulse-duration modulators could be used to drive the monostable provided that the output pulses are t.t.l.-compatible. The one used was the d.c. amplifier type described in card 10. To provide the required t.t.l. compatibility, the circuit shown in card 10 was modified to use BC125 (n-p-n) transistors with supplies of +Vcc +5V and −V_{BB} −5V the polarity of D_1 also being reversed. See card 10 for circuit description.
The t.t.l. monostable package provides complementary output pulses which can be initiated in several ways. With the connections shown, input B (pin 5) is held high and input A_2 (pin 4) which is unused is taken to +Vcc through a 1-kΩ resistor. In this form the package acts as a monostable circuit providing an output pulse of defined width whenever input A_1 (pin 3) receives a logic-level negative-going trigger pulse. Width of the output pulses is determined by the value of C_1 with R_2 ensuring that this width is obtained accurately and repeatedly. Larger R_2 values for a given C_1 will widen the output pulses.
As the negative-going edges fed to the monostable circuit are produced from a pulse duration modulator, times of occurrence will vary in sympathy with the instantaneous values of V_{in2}. Hence the shift in time of the monostable output pulses is determined by V_{in2} giving pulse-position modulation.

Component changes
Useful range of supply ≈ +3.5 to +5.25V (minimum value not guaranteed)
Max. range of V_{in2} ≈ 7V pk-pk superposed on a bias of +3.75V gives pulse shift of ≈ 14μs at p.p.m. output
Change R_2 and C_1 for different output pulse widths

Circuit modifications
Pulse-position modulated signals may be produced by a variety of electronic circuits which normally perform the signal processing indicated left. In the upper diagram the modulating signal x(t) is added in a summing amplifier to a pulse train c(t) having a negative-slope ramp. The composite signal x(t) +c(t) is fed to a comparator having a fixed reference level which produces a p.d.m. output w(t) having the modulation on its trailing edge only. Applying w(t) to a monostable gives time-shifted constant-width pulses (p.p.m.) at its output, y(t).
In the lower diagram the modulating signal x(t) has been sampled at regular intervals to produce the flat-topped p.a.m. wave p(t). The same sampling pulses are used to trigger a generator producing a synchronous train of pulses c(t) having a negative-slope ramp. The c(t) and p(t) signals are added as before and fed to a comparator producing a p.d.m. output w(t) which in turn feeds a monostable to produce the p.p.m. output y(t). Reversing the slope of the ramp in c(t) produces leading-edge p.d.m. to feed to the monostable.

Further reading
TTL data book for design engineers, Texas, 1973, pp.82 & 134-7.



Cross references
Series 15, cards 2, 4, 6, 9, 10 & 12.
Series 3, cards 2, 4, 6.

Pulse code modulator

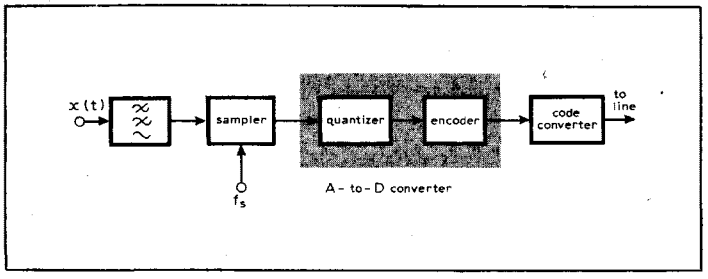
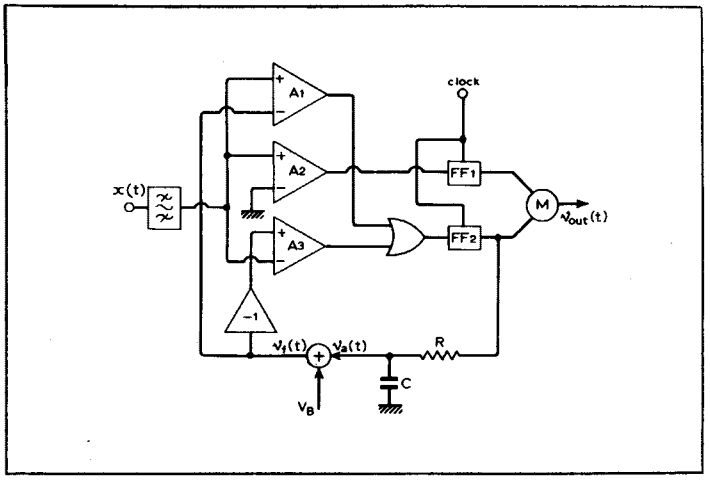


Diagram shows in block form the basic processes used in a single-channel pulse-code modulator. The analogue signal to be encoded, x(t), is passed to a sampling gate via a low-pass filter which defines the bandwidth of the modulation. The sample pulses are of low duty cycle and have a constant p.r.f. (f_s) that is at least twice that of the highest modulating signal component (f_m). In practice $f_s > 2f_m$, e.g. for speech that has been bandlimited to 0.3 to 3.4kHz, f_s= 8kHz. The output of the sampler is a p.a.m. signal which has an infinite possible number of amplitudes that are quantized, uniformly or non-uniformly, into a finite number of allowed levels. Although each sample is converted to the nearest allowed level, quantization inherently introduces errors or quantization noise. Non-uniform quantization of speech produces an improvement in the signal-to-quantization noise ratio.

Each quantized sample of the p.a.m. wave is then encoded into a group of pulses according to a binary code, the number of pulses in each code group being determined by the number of allowed levels in the quantization scheme. For speech transmission 128 levels are normally used, hence a 7-bit code is used (2^7= 128). For transmission, the coded signal is normally converted to a bipolar form to avoid wasting transmitter power by sending a d.c. component containing no information. One such code is alternate-mark-inversion (a.m.i.) which is a pseudo-ternary code with binary significance. See the works, and their bibliographies, listed under in further reading for detailed system and circuitry techniques. Diagram over shows an adaptive pulse code modulator for encoding speech. In this technique the coding signals change to track the changes in the "envelope" of the speech input x(t) after it has been bandlimited by the filter to 0.25 to 2.4kHz. The output is fed simultaneously to the voltage comparators A_1, A_2 and A_3; A_1 and A_3 together provide updated amplitude information by comparing x(t) with a feedback voltage $V_f(t)$ and its inverse respectively. Comparator A_1 produces an output logic 1 when $x(t) > +V_f(t)$ and A_3 produces a logic 1 output when x(t) is more negative than $-V_f(t)$. The A_1 and A_3 outputs are fed to bistable circuit FF2 via an OR gate, the output of which is sampled at 4.8kHz. Thus, each amplitude information bit at the FF2 output is a logic 0 when the x(t) sample is in the range $-V_f(t) < x(t) < +V_f(t)$ and is a logic 1 when x(t) is outside this range. The A_2 comparator provides x(t)-polarity information, producing a logic 1 at its output when x(t) is positive and a logic 0 when x(t) is negative. The A_2 output feeds bistable circuit FF1 which is sampled at 4.8kHz to produce polarity bits that are combined with the amplitude information bits in the multiplexer (M), which simply transmits its 2-channel inputs alternately at 9.6kbit/s. $V_f(t)$ is obtained by feeding the FF2 output to a 10ms RC integrator giving a positive output $V_a(t)$ to which is added a small d.c. bias (V_B) to ensure that $V_f(t)$ never falls to zero.



Further reading

Cattermole, K. W., Principles of Pulse Code Modulation, Iliffe 1969.

Sheingold, D. H., Analog-Digital Conversion Handbook, Analog Devices, 1972.

Renschler, E., Analog-to-Digital Conversion Techniques, Motorola application note AN-471, 1969.

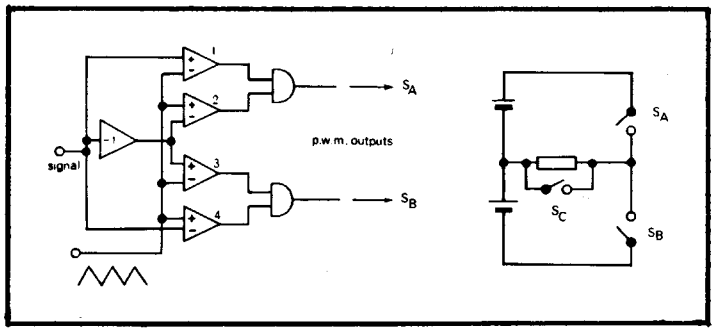
Wilkinson, R. M., Adaptive Pulse Code Modulator for Speech Signals, SRDE report no. 72001, January 1972.

Cross reference

Series 15, card 11.

Set 15: Pulse modulators Up-date

1. Pulse modulation is not restricted in its application to communication systems and data processing. Amongst the other areas of application is that of switching power amplifiers or class D systems. Recently, sub-divisions of class D have been identified which simplify the filtering of the output (class BD) and a reduction in the switching losses in the power elements (class ABD). In the former version, a set of comparators are fed with a triangular reference waveform and the signal, with a unity gain inverter giving anti-phase drive to one pair of



comparator inputs. A pair of power output stages drives the load such that on large positive inputs comparator 1 output is high except at the positive peaks of the triangular reference wave; comparator 2 goes low at the negative triangular wave peaks. Hence S_A would be gated on except for small time intervals. Throughout the positive half-cycle of the input signal S_B would be held off. The mean load voltage is thus proportional to the fraction of the time for which S_A conducts during positive inputs. Non-linearity of the triangular wave leads to distortion; push-pull operation reduces even harmonics. For inductive loads S_C must be closed when both S_A and S_B are off.

References

Martin, J. D. Class BD Amplifier Circuit, *Electronics Letters*, 1970, vol. 6, pp. 839–41. See also Daniels, A. R. and Slattery, D. Class ABD Amplifier, *Electronics Letters*, 1974, vol. 10, p. 364.

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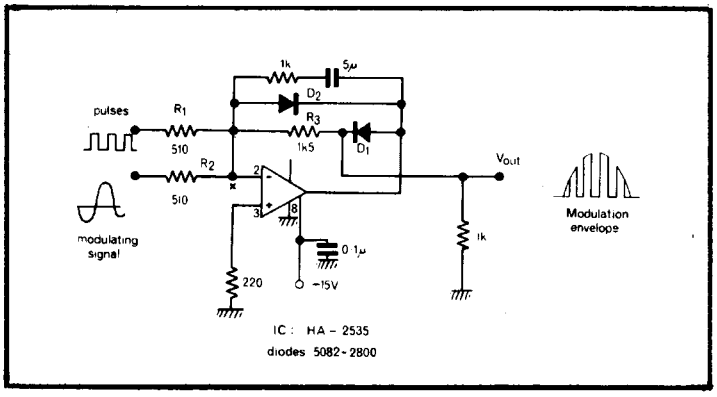
2. This circuit is aimed at producing positive half-sinusoidal envelopes with respect to zero voltage reference, with modulation at 100%.
For absolute rectification, the diodes are included in the feedback loop of the inverting operational amplifier. The gain constraint on the input pulses is then limited by the power supply levels of the op-amp. During the negative part of the modulating signal, the amplifier output swings positively by an amount depending on the ratio of



R_3/R_2 plus the drop across D_1. The input pulses are therefore forced to swing within this limit, but note that the pulse amplitude must be sufficiently great relative to the modulation amplitude to obtain 100% modulation. Overdriving the pulse level by 20% more than required is suggested. Full sine wave modulation can be obtained by adding another resistor to the summing input X, and applying an appropriate negative bias level.

Reference

Quick, D. Improve amplitude modulation of fast digital signals, *EDN*, Sept. 20, 1975.

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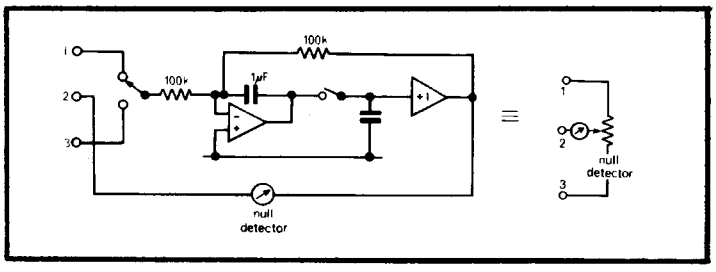
3. D.c. potentiometers normally depend on the precise ratio of a pair of resistances; that ratio has to be variable over a wide range to give the high resolution needed. This circuit replaces the precise ratio of resistances by the ratio of time intervals. These intervals are controlled by a digital clock, and the clock frequency is not critical as it is only the ratio of the times for which the input switch is connected to inputs 1 and 3 respectively. As with conventional chopper-circuits the switch should combine minimal input offset with maximum switching speed. The original paper uses a mechanical switch at the input, with a series-shunt switch at a later stage (not shown) to inhibit response to the switching transient. The final switch activates a sample-and-hold circuit that stores the integrator output. The final output thus has minimal ripple except during an input step to which it responds rapidly (99.9% within two sample periods is claimed). Additional applications noted include current comparison and cascaded voltage division from values as high as 1kV. The overall accuracy is claimed to be ±(0.1 p.p.m. + 5μV).



Reference

Sugiyama, T. & Yamaguchi, K. Pulsewidth modulation d.c. potentiometer, *IEEE Trans. Instrum. and Meas.*, 1970, pp. 286–90.

notes

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Set 16: c.d.as — signal processing

Current differencing amplifiers, or Norton amplifiers, are an ingenious solution to the need for single-supply op-amps. As there is superficial similarity in c.d.a. circuits to normal op-amp circuits, the following article warns against the transposing op-amp circuits into c.d.a. form, drawing a parallel with the days when the transistor was first introduced. Those new to circuits of the LM3900 kind should therefore make a point of reading the articles preceding sets 16 and 17, which introduce the ideas behind c.d.as in a gradual and easily assimilable way.

The first article provides a simple look at the c.d.a. circuit, the amplifier being considered as a d.c. feedback pair, fed by a current mirror. It is the current mirror that is responsible for the amplifier's name, in that it is used in such a way that the input to the feedback pair is the difference between two input *currents*. It is, in effect, the current dual to the voltage-differencing action of the long-tailed pair used in op-amps. For the next stage of circuit elaboration see card 1, which shows incorporation of an improved emitter follower output stage and an additional transistor which only operates when the input is over-driven. A third stage of elaboration is described in the article preceding set 17.

Some circuits can nevertheless be "borrowed" from conventional op-amp practice, for example, the bandpass and band stop filters shown on cards 7 & 8. But notice that the Sallen & Key filters cannot, because it isn't possible to use series applied feedback (but see the final circuit modification on card 9).

Card 10 of set 5 also gives c.d.a. circuits.

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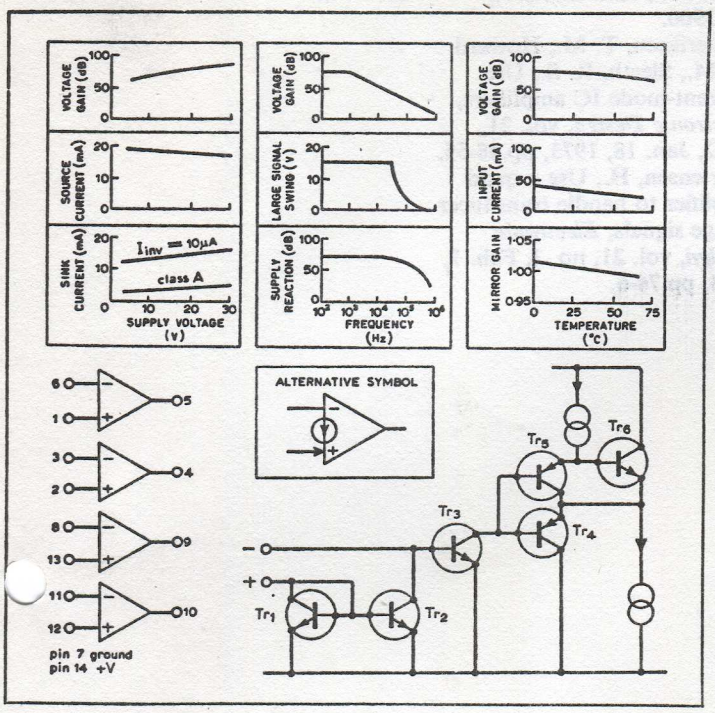
Set 16: c.d.as—signal processing—1

Current differencing amplifiers



Three sets of cards deal with current differencing amplifiers of the LM3900 kind. This set covers signal processing applications, set 17 covers signal generation and a third set deals with various other circuits including test, measurement, detection, logic and driving circuits.

Typical performance
Supply: 15V
R_L: 5kΩ
Voltage gain: 2,800 (69dB)
Output swing: 0.1 to 14.2V
Output current: source 10mA, sink 1.3mA
(overdriving inverting input increases sink current up to >30mA)
Input current: 30nA
Unity-gain bandwidth: 2.5MHz
Slew rate: +0.5V/μs, −20V/μs

N.B. Data is for National Semiconductor LM3900. A similar amplifier is available from Motorola and other manufacturers are expected to "second-source" such devices. Refer to manufacturers data sheets particularly for maximum ratings. While other current-differencing amplifiers may be expected to have similar performance in the circuits to be described it is important that the ratings of particular devices are not exceeded.

Circuit description
Transistors Tr_1, Tr_2 are a current mirror with the collector current of Tr_2, approximately equal to non-

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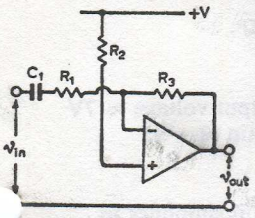
Set 16: c.d.as—signal processing—2

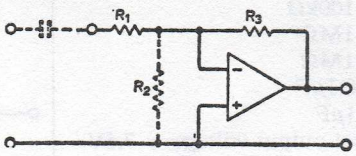
Basic amplifiers—1



Typical performance
Supply: +15V
R_1: 100kΩ
R_2: 2.2MΩ
R_3: 1MΩ
C_1: 0.1μF
Direct output voltage ≈ 7V
Voltage gain ≈ −10

Circuit description—1
No direct current flows in R_1 and hence R_2, R_3 determine the d.c. operating conditions. For perfect balance between the input circuit transistors they will carry equal current and for $V_{be} \ll +V$, the direct output voltage is given by $R_3/R_2 \times (+V)$, i.e. $R_2 = 2R_3$ is the usual condition for maximum available voltage swing with the output biased at supply mid point. As there is no significant alternating current in R_3, it is the alternating currents in R_3 and R_1 that are equal in magnitude while the virtual earth at the inverting input (though ≈0.6V d.c.) gives a voltage gain of $-R_3/R_1$. The addition of reactive components modify the gain, so that a high-frequency roll-off is readily achieved by placing a capacitor across R_3 (corner frequency $1/2\pi R_3 C$).

Capacitive coupling may be required to the load, while the reactance of $C_1 \ll R_1$ at lowest frequency. Maximum resistance values of up to 10M may be used, but roll-off due to stray capacitances is likely.



Typical performance
Supply: +15V
R_1: 470kΩ
R_3: 4.7MΩ
R_2: 470kΩ
Direct output voltage ≈ 6V
Voltage gain ≈ −10

Circuit description—2
The base-emitter voltage of the input transistor is ≈0.55V at room temperature, falling by ≈2.5mV for every 1% rise in temperature and by less than this (typically 0.5 to 1mV) for each 1-V increase in the supply voltage. This voltage is thus sufficiently stable to be used as the reference voltage for setting the d.c. output conditions, and the technique may be called the "nV_{be}" biasing method. It is identical in principle to that used in the d.c. feedback pair and the "amplified-diode". If the source has an internal resistance to ground $< R_1$ then direct coupling may be used with R_1 chosen to provide the required input resistance for the circuit and R_3 determining both the voltage gain and the direct output voltage. Resistor R_2 is omitted in this mode as is the input coupling capacitor. Direct output voltage $\approx (R_3/R_1 + 1)V_{be}$. Voltage gain $\approx -R_3/R_1$. The method requires modification both for high and low gains as the direct output voltage may not be convenient. By capacitive coupling to R_1 the d.c. and gain conditions can be made independent, with direct output voltage $\approx (R_3/R_2 + 1)V_{be}$ and voltage gain $\approx -R_3/R_1$.

inverting input current, subtracting from inverting input current at base of Tr_3. The net input current to Tr_3 is (I−) − (I+) and this is amplified by Tr_3 with Tr_5, Tr_6 forming an improved emitter follower output stage. Constant-current generators define the operating conditions while Tr_4 comes into action on over-driving the input to maximize the sink-current. Output depends on the difference between two positive input currents with negative feedback taken to the inverting input when the gain is to be defined. The non-inverting input is outside the feedback loop, and behaves as a forward-biased p-n junction. With resistive negative feedback applied between output and inverting input, the direct currents in the two inputs will be equalized to within the accuracy of the current mirror. If the non-inverting input current is defined by a resistor to +V, the direct output voltage is then a fixed fraction of +V. Transistor Tr_3 base current is ≈30nA, allowing very low bias/signal currents, and like the voltage gain and output current capabilities is controlled over wide temperature and supply variations. An internal regulator (not shown) ensures this by providing the constant currents while also biasing a set of transistors that clamp each input to ≈ −0.3V on negative input swings.

Further reading

Frederiksen, T. M., Howard, W. M., Sleeth, R. S., The LM3900—A New Current-Differencing Quad of ±Input Amplifiers, National Semiconductor application note AN72.

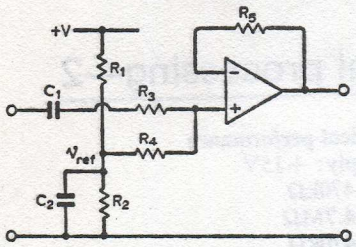
Frederiksen, T. M., Norton quad amplifier subtracts from costs, adds to design options, *Electronics*, Dec. 6, 1973, pp.116-20.

Motorola Linear Integrated Circuit Data Book, pp.7-446, 7-453, 7-456 and 7-463; data sheets on MC3301P and MC3401P amplifiers.

National Semiconductor, Linear Integrated Circuits, pp.226-33, data sheets on LM3900.

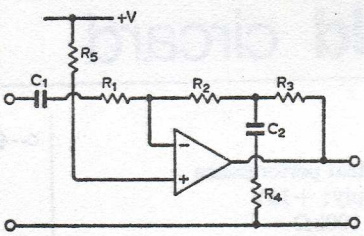
Frederiksen, T. M., Howard, W. M., Sleeth, R. S., Use Current-mode IC amplifiers, *Electronic Design*, vol. 21, no. 2, Jan. 18, 1973, pp.48-55.

Mortensen, H., Use a quad amplifier to handle transducer bridge signals, *Electronic Design*, vol. 21, no. 3, Feb. 1, 1973, pp.74-6.



Typical performance
Supply: +15V
R_1: 47kΩ
R_2: 47kΩ
R_3: 100kΩ
R_4: 1MΩ
R_5: 1MΩ
C_1: 0.1μF
C_2: 1μF
Direct output voltage ≈ 7.5V
Voltage gain ≈ +9.5

Circuit description—3
A third variation on the biasing methods available, is to take the bias resistor R_L to a separate reference voltage V_{ref} which can be decoupled to make the output voltage much less dependent on supply ripple. A single reference voltage (here equal to $+V/2$) may be used for a number of separate amplifiers separate control of the quiescent output conditions is by variation of R_4 for each amplifier while adjustment of R_1, R_2 varies all of them simultaneously. The amplifier is shown with the signal applied to the non-inverting input. No feedback is available at this input and so the impedance of the input transistor affects the input current. At room temperatures, $r_i \approx 0.026/I_{R_4}$, giving a value >3kΩ for the values shown. This reduces the gain to about 3% below the simple theoretical relationship R_5/R_3. This biasing method is equally applicable to the inverting amplifiers.

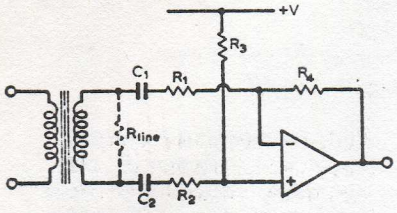


Typical performance
Supply: +15V
R_1: 1MΩ
R_2: 1MΩ
R_3: 1MΩ
R_4: 10kΩ
R_5: 2.2MΩ
C_1: 0.1μF
C_2: 4.7μF
Direct output voltage ≈ 7V
Voltage gain ≈ −95

Circuit description—4
The value of the feedback resistor is limited to a few megohms for several reasons (bias instability, effect of stray capacitance, noise and hum). If it is required to have a high input resistance and high voltage gain than the a.c. and d.c. feedback must be different. As shown, R_4 and R_3 constitute a potential divider for the output signal while only R_3 is involved in the d.c. feedback. Output voltage has a quiescent value of $+V(R_2+R_3)/R_5$. Voltage gain is $\approx(-R_2/R_1)$ (R_3/R_4+1). Where $R_2=R_1$, a convenient condition, the voltage gain simplifies to $-(R_3/R_4+1)$. However when the ratio R_3/R_4 is large the feedback theory demands that the limited open-loop gain be taken into account. In practice, a ratio that should set the gain to −20 will do so to within about 1%, while a nominal gain of −100 would be nearer to −95.

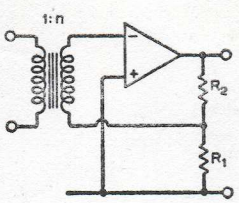
Cross references
Set 5, cards 5, 8, 9, 10.
Set 7, cards 4, 10.
Set 10, cards 1, 9.
Set 16, cards 2, 5, 6, 10.

Basic amplifiers—2



Typical performance
Supply: +15V
R_1, R_2: 10kΩ
R_3: 220kΩ
R_4: 100kΩ
C_1: 1μF
C_2: 1μF
Direct output voltage ≈ 7V
Voltage gain ≈ −10
(transformer secondary output)

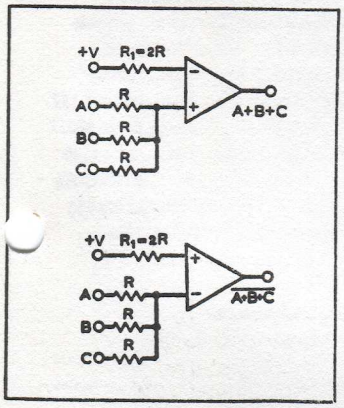
Circuit description—1
Common-mode signals are a problem when transmission over lines has to take place in a noisy environment. By coupling the signals through a transformer such common mode signals are minimized, while the anti-phase inputs of the current differencing amplifier offer a further improvement. Any common-mode voltage at the transformer secondary produces equal currents at the two inputs largely cancelling each other because the gain at the two inputs is equal and opposite. R_{line} is inserted to achieve the correct loading on the source with R_1, R_L sufficiently larger not to affect that loading. Quiescent output voltage ≈ $V(R_3/R_4)$; voltage gain ≈ $-R_4/R_1$.



Typical performance
Supply: +15V
R_1: 10kΩ
R_2: 100kΩ
Direct output voltage ≈ 6V
Voltage gain ≈ 11
(transformer secondary to output)

Circuit description—2
Where the source is inductive or is to be transformer-coupled, a variant of the "nV_{be}" biasing method provides a simple solution. Again there is the restriction that the direct output voltage and the gain of the amplifier itself are controlled by the same resistor ratio but decoupling part of R_1 to ground can make the ratio for signal frequencies ≫ the ratio at d.c. if required. In the extreme case, R_1 can be completely decoupled giving the full open-loop gain of the amplifier. This coupled with the step-up turns ratio of the transformer gives a very high overall gain. As shown, the overall voltage gain is ≈ $n(R_2/R_1+1)$ and the quiescent output voltage is ≈ $(R_2/R_1+1)V_{be}$.
Because the input current required by the amplifier is very small (≪ 1μA) the effective input impedance remains high regardless of the gain, and high step-up ratios are possible. This yields a very sensitive microphone amplifier though the noise performance is unlikely to allow use in audio applications.

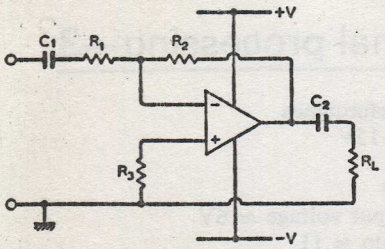
Logic gates



Typical performance
Supply: +20V
IC: ¼ LM3900
R_1: 150kΩ
R: 82kΩ
Output logic 0: 150mV
Output logic 1: 19.2V
For inputs commoned, output changes state for input voltage ≈ 20% of +V.

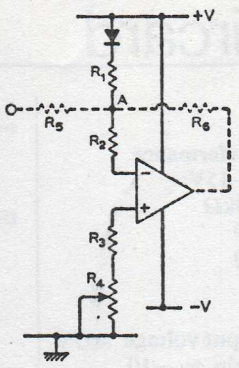
Circuit description
Availability of two current inputs simplifies the design of basic logic gates with these amplifiers. For example, a low current at one input can hold the output in one desired state while the other input receives the sum of the currents from two or more inputs. This sum can be set to overcome the bias when only one input is high or only if all are simultaneously high, leading to OR and AND-type circuits respectively. (The amplifier is working as a high-gain comparator and can also provide a majority-gate in which any two out of three inputs are enough to provide the required output. By extension some of the simpler forms of threshold logic are possible by scaling the values of resistors to assign a different weight to their importance in decision making.) In the first configuration, if any input is high the current driven into the non-inverting input exceeds the inverting input current and the output is driven high, i.e. an OR gate. The remaining input resistors connected to logic 0 bypass a small portion of that current (<$0.5V/R$ for each resistor) but unless the number of inputs is large and/or the supply voltage is low, this is not a problem. Speed of response is limited to ≈0.5V/μs for positive swings and up to 20V/μs for negative swings though the fall in voltage is slower as logic 0 is approached. By interchanging the inverting and non-inverting inputs with no change in component values, a NOR gate is produced. This flexibility of being able to produce different logic functions from the same package is very attractive. In addition, one or more of the amplifiers can be used to provide astable, Schmitt trigger functions, etc. for obtaining the appropriate waveforms with which to drive the gates.

Component changes
+V Normal voltage range is +4 to +36V, but some devices will operate to <3V without difficulty.
R_1, R Ratio of these resistances is chosen to ensure that with the lowest expected value of logic 1 to any one input that, the resulting current flow into the non-inverting input is sufficient to overcome



Typical performance
Supply: ±15V
R_1: 100kΩ
R_2, R_3: 1MΩ
R_L: 10kΩ
C_1: 0.1μF
C_2: 1μF
Direct output voltage ≈ 0V
Voltage gain ≈ −10

Circuit description—3
The biasing techniques described above are easily adapted for dual supply operation, making the amplifier compatible with standard op.amp. ±15V systems. One method is to bias the non-inverting input from the centre rail, leaving the same p.d. across R_2 and R_3 if $R_2 = R_3$, i.e. the output is substantially at 0V if the amplifier has well-matched inputs. This remains true for all values of positive and negative supply voltages including those cases where they are markedly unequal in value. R_1 plays no part in the d.c. conditions and is chosen for the desired gain/input resistance. Voltage gain $\approx -(R_2/R_1)$. Non-inverting gain is obtained as before simply by transferring R_1 to the non-inverting input. The gain is less well-defined but the bandwidth is increased, because there is then no resistor to attenuate the negative feedback, i.e. the bandwidth can approach that of the amplifier with 100% feedback while the gain can approach the value defined by (R_2/R_1).



Typical performance
Supply: ±15V
R_1, R_2: 1MΩ
R_3: 820kΩ
R_4: 500kΩ
R_5: 220kΩ
R_6: 2.2MΩ
Direct output voltage ≈ 0V
Voltage gain ≈ −10

Circuit description—4
The present form of current-differencing amplifier is not suited to low-level d.c. amplification and cannot replace standard operational amplifiers directly. The adaptation shown has a reasonable performance for d.c. signals of >100mV provided the offset adjustment is made and subsequent changes in temperature and supply are restricted. Effective input of the amplifier is point A and for $R_1 = R_2$ its potential is a 0V in the absence of feedback (the diode compensates for the input V_{be}). Adjusting R_4 sets the output voltage to 0V prior to the application of feedback with $(R_3 + R_4) \approx (R_1 + R_2)/2$. The resistors R_5, R_6 then set the input resistance and gain as for previous amplifiers. Point A is no longer such a good equivalent to a virtual earth from the signal standpoint since the presence of R_2 lowers the amplifier gain, while $R_2//R_1$ is the equivalent resistance to ground at this point.

Cross references
Set 5, cards 5, 8, 9, 10.
Set 7, cards 4, 10.
Set 10, cards 1, 9.
Set 16, cards 1, 5, 6, 10.

Fig. M1

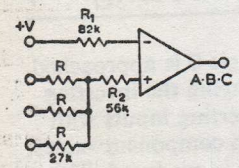


Fig. M2

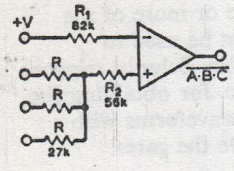
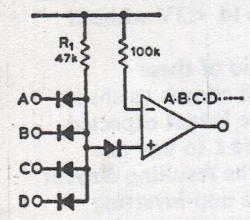


Fig. M3

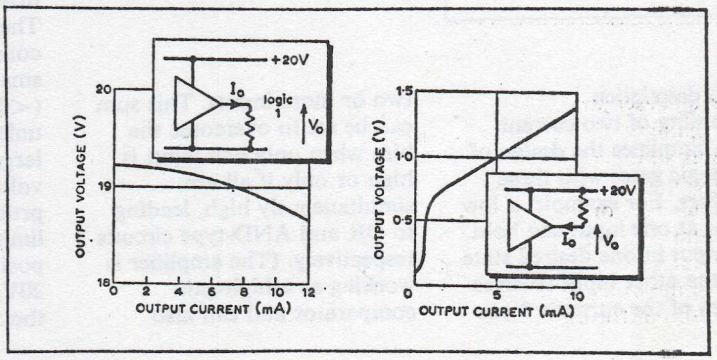


the fixed current in the positive input. (Allow for $0.5V/R$ lost in each logic 0 input.) Typically $R = R_1/2$ is a suitable starting point and R may vary from 10k to 10MΩ.

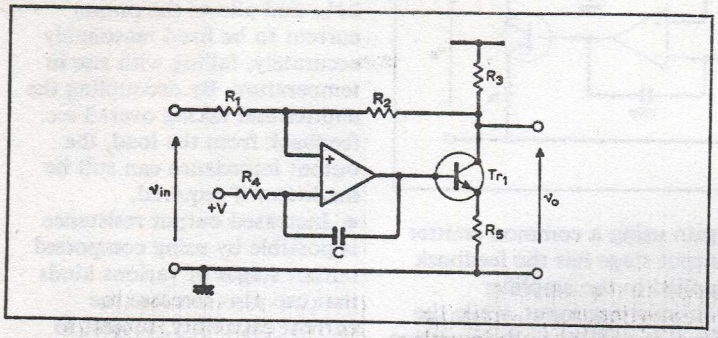
Fan-out To maximize this R, R_1 should be large but there is no great advantage to raising them above 1MΩ.

Circuit modifications
- The AND/NAND functions are slightly more difficult to construct for multiple inputs. This is because for an *n*-input gate the sum of the currents produced by (*n*-1) inputs at logic 1 differs little from that produced by *n* inputs if *n* is large. Up to three inputs can be used with a reasonable margin of safety as in Fig. M1, where the resistor R_2 reduces the current flow when two inputs are on. For a two-input AND gate R_2 may be omitted and the values of the input resistors adjusted. For example, with R_1 82kΩ, R 100 or 120kΩ.
- Again interchanging the inverting and non-inverting inputs gives a NAND gate. By scaling the resistors in some of these and/or feeding signals to both inputs circuits which are intermediate between true analogue and true circuits become possible. (Fig. M2)
- If it is required to have multiple inputs to an AND gate, simple diode gating may be used, Fig. M3, with the amplifier serving a similar function to the transistors in d.t.l., but with the advantage that the ratio of output to input current, which determines the fan-in fan-out capability, is of the order 10^6 (25nA—25mA). If any input is at logic 0 the current in R_1 flows through that diode. All inputs have to be at logic 1 for the current to be diverted into the amplifier non-inverting input to give a logic 1 out. The threshold voltage and hence the noise margin is low in this circuit. If all inputs but one are at logic 1 then that input need only rise to ≈ 0.5V to be recognized as logic 1. A NAND function is obtained by reversing the amplifier inputs.

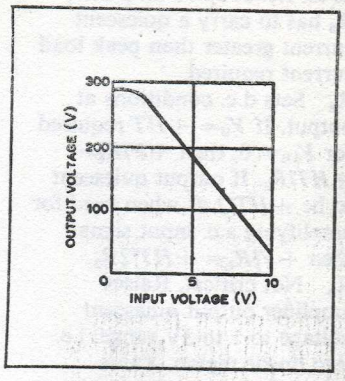
Cross references
Set 11, cards 1, 2, 11.



High voltage amplifiers



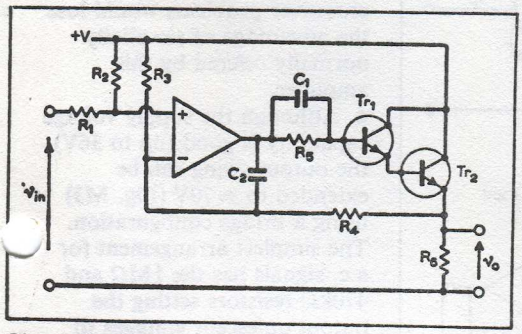
Typical performance
Supply: +15V, +300V (HT)
R_1: 330kΩ
R_2: 10MΩ
R_3, R_4: 470kΩ
R_5: 1kΩ
C_1: 100pF
Voltage gain: −31.2 (d.c. to 1kHz)
Cut-off frequency: 3kHz
Output impedance: <10kΩ (d.c. to 1kHz)
Input impedance: 330kΩ (d.c. to 1kHz)



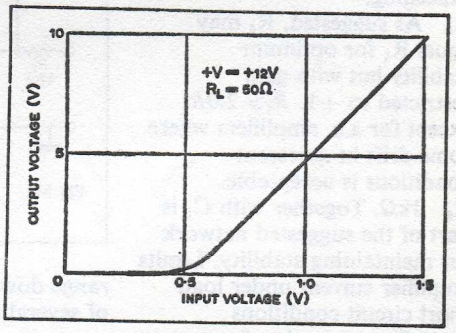
Circuit description
Where a high output voltage swing is required the amplifier must be fed from a separate low-voltage supply, and a suitable high-voltage transistor employed to withstand the main supply voltage. The configuration depends on whether it is the output voltage or current that is to be defined. If the former, then the feedback is taken from in shunt with the load. For an inverting-gain amplifier and the transistor in the common-emitter mode, the inverting gain of the transistor necessitates that the feedback be applied to what is normally considered as the non-inverting input. For an input of 0V d.c., the current flow in R_1 is small and that in R_2 is forced by the feedback to equal that in R_4. If in this condition the output is desired to be $+HT$ then $+HT/R_3 = +V/R_4$ gives the required value of R_4. Overall voltage gain is given by $(-R_2/R_1)$ as the circuit is effectively a "see-saw" amplifier while the input resistance is approximately R_1. Resistance R_5 introduces a small amount of negative feedback into the output stage and raises the amplifier quiescent voltage well into its linear region. Capacitor C_1 modifies the gain/frequency characteristic to maintain stability at the higher loop gain. Output voltage swing can be up to 95% of the supply voltage if lightly loaded and the negative feedback keeps the output impedance reasonably low.

Component changes
R_1, R_2 These set the input resistance and the voltage gain $R_2 \gg R_3$ to minimize loading on

Power amplifiers



Typical performance
Supply: +10V
R_1: 100kΩ
R_2, R_3, R_4: 1MΩ
R_5: 1kΩ
R_6: 50Ω
C_1: 1nF
C_2: 10pF
Tr_1: BFR41
Tr_2: TIP3055
V_i: 1.03V
V_o: 5.0V
Voltage gain: 9.7
Change in V for
I_L of 0-1A 0.05%
V_s of 10-14V 0.5%



Circuit description
Addition of a Darlington-connected pair of transistors increases the output current capability from 10mA to 1-5A depending on the ratings of the transistors used. One restriction is that the V_{be}'s of the transistors limit the output voltage to around 2.5V below the supply level allowing for the amplifier internal saturation. The additional phase shifts that may occur even in an emitter follower make external compensation desirable. For supply, input and output to be all positive, the configuration shown is adequate, where with $R_2 = R_3$, V_o varies linearly with V_i provided V_i is above the amplifier internal V_{be}. The relationship is then $V_o \approx V_{be} + (R_4/R_1)(V_i - V_{be})$ as the currents in R_1 and R_4 have to be equal. This means that as a d.c. amplifier it is of relatively low accuracy but is quite suitable for supplying small d.c. motors under the control of a phase-locked loop. A combination of the techniques for increasing the current ratings and voltage could allow the production of high-power amplifiers. Replacing the emitter follower stages by common emitter amplifier increases the available positive output swing to within a hundred millivolts of the positive supply.

Component changes
R_1 This sets the voltage gain in conjunction with R_4. Because of the V_{be} offset, the output voltage becomes temperature dependent particularly for V_i comparable to V_{be}, i.e. high gains are not compatible with good stability in this configuration. R_1 100k to 10MΩ.
R_2, R_3 These provide forward bias for each of the inputs allowing the output to be

the output. R_2 1M to 22MΩ.
R_3 Load resistance, dictated by user requirements. For use as an r.c.-coupled amplifier, R_3 has to carry a quiescent current greater than peak load current required.
R_4 Sets d.c. conditions at output. If $V_o = +HT$ required for $V_{in} = 0$, then $+V/R_4 = +HT/R_2$. If output quiescent to be $+HT/2$ as when used for amplifying a.c. input signal, then $+V/R_4 = +HT/2R_2$.
R_5 Not critical. Raises amplifier output quiescent voltage to 1 to 3V range, i.e. into linear region. Value dependent on output quiescent current but might be 50Ω to 5kΩ.
+V Chosen to suit amplifier, and available supplies (+4 to +36V).
+HT Dictated by load requirements.
Tr_1 Must have voltage rating in excess of +HT particularly if inductive loading possible.

Circuit modifications

● A non-inverting amplifier

Fig. 1

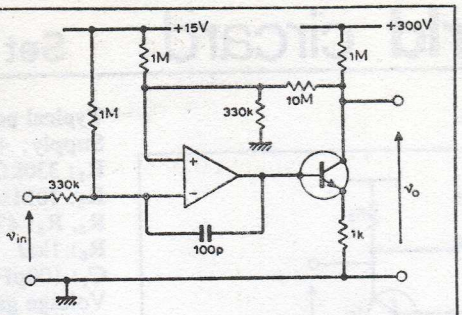


Fig. 2

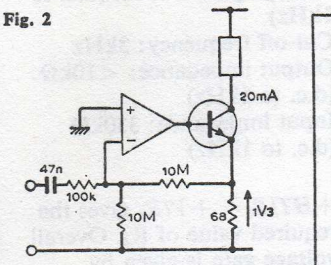
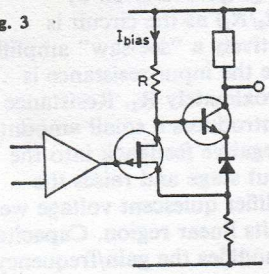


Fig. 3



again using a common emitter output stage has the feedback applied to the amplifier non-inverting input, while the signal is applied to the inverting input (the inversion in the transistor ensuring the correct overall sign for the gain). For a transfer function that passes through the origin a pre-biasing network is required. Again the gain is set by the ratio of the feedback to the input resistor.
● For a high output-impedance, the feedback is taken from the transistor emitter. The method can be employed where the load is to be transformer coupled and the direct voltage drop across the primary is too small to allow of the d.c. feedback. The two 10-MΩ resistors define the potential at the transistor emitter as about $2V_{be}$ and allows the output current to be fixed reasonably accurately, falling with rise in temperature. By decoupling the emitter and taking overall a.c. feedback from the load, the output impedance can still be made low if required.
● Increased output resistance is possible by using compound output stages of various kinds that can also increase the current capability, subject to device power limitations. An f.e.t. draws no current from the amplifier ensuring that the load and emitter resistor currents change together if the current I_{bias} is made constant, either because of the high supply voltage and correspondingly high resistance R, or by a separate low-voltage constant-current stage.

Cross references
Set 7, cards 5, 7.
Set 16, cards 1, 2, 6.

controlled for inputs down to zero. This is best achieved for $R_1 = R_4$ when $V_o = V_1$ is the first-order approximation, the V_{be} effects at the two inputs cancelling.
R_4 As suggested, R_4 may equal R_1 for optimum stability but with gain restricted to +1. $R_4 \geq 2.0R_1$ except for a.c. amplifiers where some drift in quiescent conditions is acceptable.
R_5 1kΩ. Together with C_1 is part of the suggested network for maintaining stability. Limits amplifier current under load short circuit conditions providing protection for amplifier and output stage. Not adequate unless proper heat-sinking used since limit of output current depends on transistors' current-gains and is ill defined.
C_1, C_2 Control high frequency performance. C_1: 330p to 2.2nF, C_2: 5.6 to 22pF. Choose lowest values giving stability under operating conditions.
R_6 Load resistance. This may

Fig M1

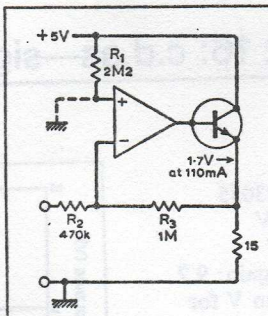


Fig. M2

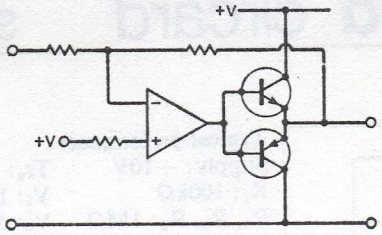
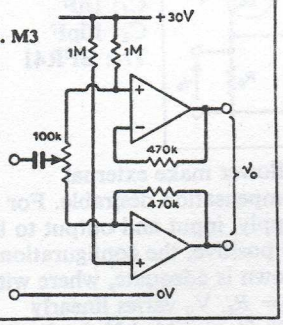


Fig. M3



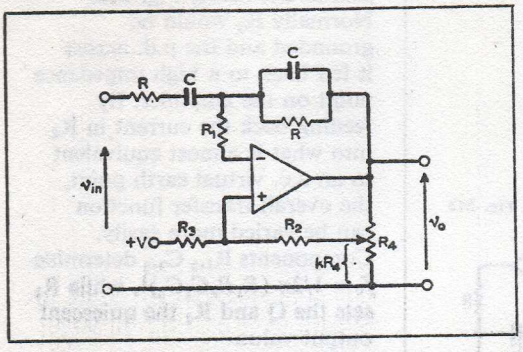
range down to 10Ω as currents of several amps are possible.

Circuit modifications

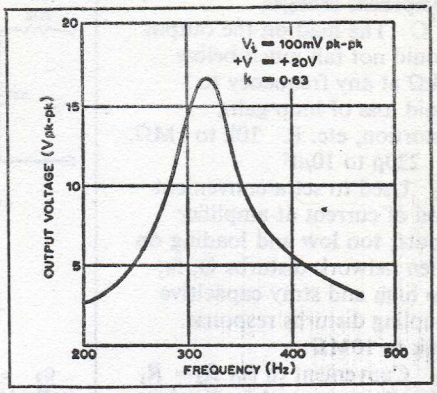
● A simpler circuit based on the same principles is Fig. M1. The limiting and compensation components have been eliminated together with the high-power transistor. The bias network shown is suitable for a source with resistive path to ground ≪470kΩ, with the non-inverting input grounding. The bias method is then basically the "nV_{be}" method as in the "amplified diode". Alternatively a capacitively coupled source may be used with no direct current in R_2 and $R_1 \approx 2R_3$ to set $V_o \approx +V/2$.
● For higher efficiency the usual Class B technique can be applied with a complementary-symmetry output (Fig. M2). Not recommended for low-distortion applications, since additional bias networks to overcome crossover problems would lose the advantage of simplicity normally offered by this amplifier.
● Although the supply voltage capability is good (up to 36V) the output swing can be extended to ≈70V (Fig. M3) using a bridge configuration. The simplest arrangement for a.c. signals has the 1MΩ and 470kΩ resistors setting the output quiescent voltages to $+V/2$ for maximum undistorted voltage swing. Replacing the two input resistors by a potentiometer and applying the signal via the pot to opposite-phase inputs gives anti-phase outputs that can be set for equal magnitude with an overall voltage gain of about 18.

Cross references
Set 7, cards 2, 4, 7, 8, 10, 11.
Set 16, card 5.

Bandpass filters

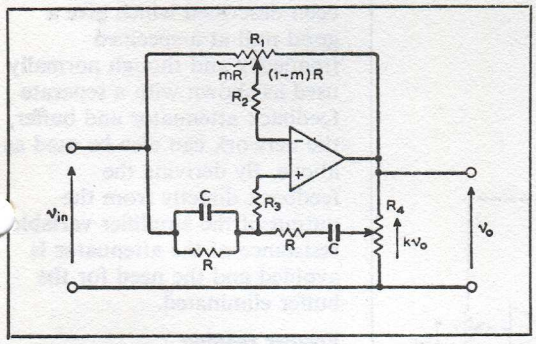


Typical performance
R: 47kΩ
C: 10nF
R_1, R_2: 1MΩ
R_3: 6.8MΩ
R_4: 100kΩ
Supply: +15V
f_o: 320Hz
For $Q = 15$
$k = 0.640$
N.B. Onset of oscillation at $k = 0.648$ compared with theoretical value of 0.66.

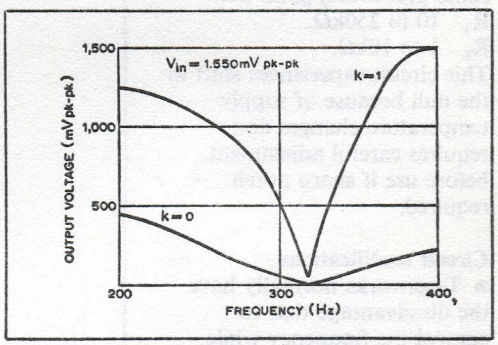


Circuit description
Active filter techniques based on operational amplifiers are applicable to current-differencing circuits. That shown is a direct adaptation of Circard 1, Set 1. A Wien network is placed between source and output with the potential at its junction monitored by the amplifier input terminal. Resistor R_1 is a high-value resistance to minimize loading on the network. Resistor R_2 provides a variable amount of positive feedback to increase the Q of the circuit with minimal effect on the centre-frequency while R_3 sets the quiescent output voltage to allow for maximum signal swing. Because $R_2 > R_1$ would be required for stability, with R_2 taken directly to the output, and variable high-value resistors are inconvenient, the alternative is to tap R_3 onto a variable portion of the output voltage. The result is a band-pass filter with centre frequency given by $f = 1/2\pi CR$ and with Q controlled by R_4. The limited gain and bandwidth capabilities of the amplifier does not allow the circuit to provide large stable Qs nor to operate successfully at frequencies ⩾10kHz. The input impedance falls as the Q is increased because of the increased output swing (gain ∝ Q to a first order). It is also true that the sensitivity of such circuits to variations in component values is proportional to the Q, i.e. for $Q = 10$ a 1% change in a critical resistor might

Notch filters



Typical performance
Supply: +20V
R_1: 100kΩ
R_2, R_3: 1M
R_4: 1kΩ
R: 47kΩ
C: 10nF
Notch frequency: 319Hz
Achieved for $m \approx 0.35$
for $k = 0$ and $k = 1$



Circuit description
The circuit is again derived from a Wien Bridge to demonstrate the principles by which known circuits can be adapted to current-differencing amplifiers. It provides a notch or null in the response at a frequency set by the RC values ($f = 1/2\pi RC$) with R_1 providing a trimming action to get as true a null as possible. If R_4 is a low resistance potentiometer, then the depth of the null is unaffected as the tapping point is varied, since both ends of the potentiometer are at zero for this condition. However, the positive feedback introduced has the effect off-null of sharpening up the response so that the gain remains close to unity for frequencies close to the null. This makes the circuit useful for nulling out the fundamental (or particular harmonic) of a complex waveform with minimal effect on the other harmonics. A weakness of this particular circuit is that it relies on the matching of the inverting and non inverting input sensitivities making it prone to variation with supply/ temperature changes, etc.

Component changes
R, C The difficulty with this particular circuit is that these should have a low impedance compared with R_3 so that the latter does not load them, while not in turn being disturbed by the varying source resistance of R_4 as k is varied. Typically R 10 to 100kΩ

produce >10% variation in the Q itself.

Component changes

R, C The load on the output should not fall much below 10kΩ at any frequency to avoid loss of loop gain, distortion, etc. R 10k to 1MΩ, C 220p to 10μF

R_1 Used to set a convenient level of current at amplifier inputs; too low and loading on Wien network disturbs Q, f_0; too high and stray capacitive coupling disturbs response. 220k to 10MΩ.

R_2 Convenient to set $R_2 = R_1$ using R_4 to control feedback. Alternatively for fixed Q particularly if low, eliminate R_4 taking R_2 directly to output. Then $R_2 > 1.5R_1$.

R_4 Not critical, but ≫10kΩ and <R_2.

R_3 Sets quiescent output voltage for maximum swing. Should be chosen after other components have been selected for desired response. Typically 2 to 10 × R_1, but for a given value, small variations in k and hence Q can be accommodated without serious bias changes.

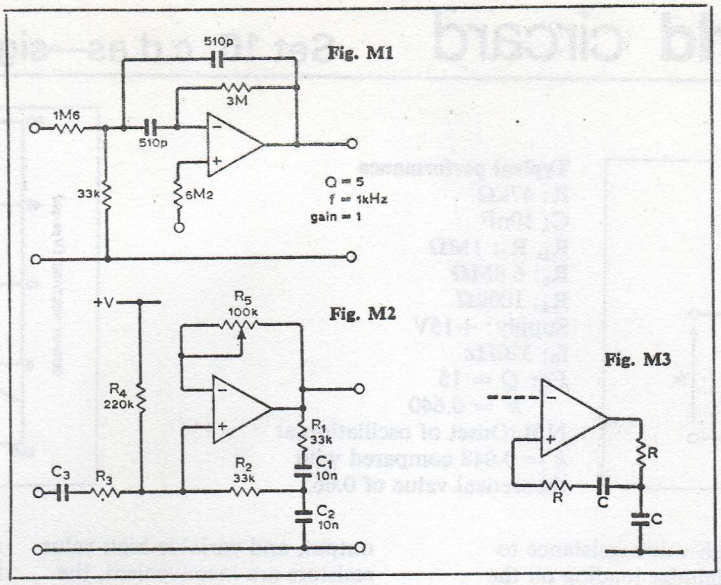


Fig. M1

Fig. M2

Fig. M3

Circuit modifications

● Multiple feedback circuits (Fig. M1) are the equivalent of the virtual earth circuits used with conventional operational amplifiers. With correct scaling of resistors, capacitors $Q > 1$ is achieved simultaneously with centre-frequency gain of unity. Again both are strongly dependent on component stability at high-Q values.

● A better approach to filter design with current-differencing amplifiers is to select passive networks whose transfer-function gives a defined output current. It is possible to adapt the Wien and similar networks, Fig. M2. Normally R_2 would be grounded and the p.d. across it fed back to a high impedance point on the amplifier. By feeding back the current in R_2 into what is almost equivalent to an a.c. virtual earth point, the overall transfer function can be varied more easily. Components $R_{1,2}$ $C_{1,2}$ determine $f_0 = 1/2\pi\,(R_1R_2C_1C_2)^{\frac{1}{2}}$, while R_5 sets the Q and R_4 the quiescent output value.

● Any of the other RC networks used in bandpass filter designs are applicable and Fig. M3 gives almost identical performance for $R_1 = R_2 = R$, $C_1 = C_2 = C$.

Cross references

Set 1, cards 1, 3, 6, 7, 8, 12.
Set 5, cards 6, 10.
Set 10, card 8.
Set 16, cards 8, 9.

with C to give frequency as $f = 1/2\pi RC$ C, 220p to 10μF.

R_2, R_3 1 to 10MΩ. At higher frequencies stray capacitance effects bring phase shifts preventing good null.

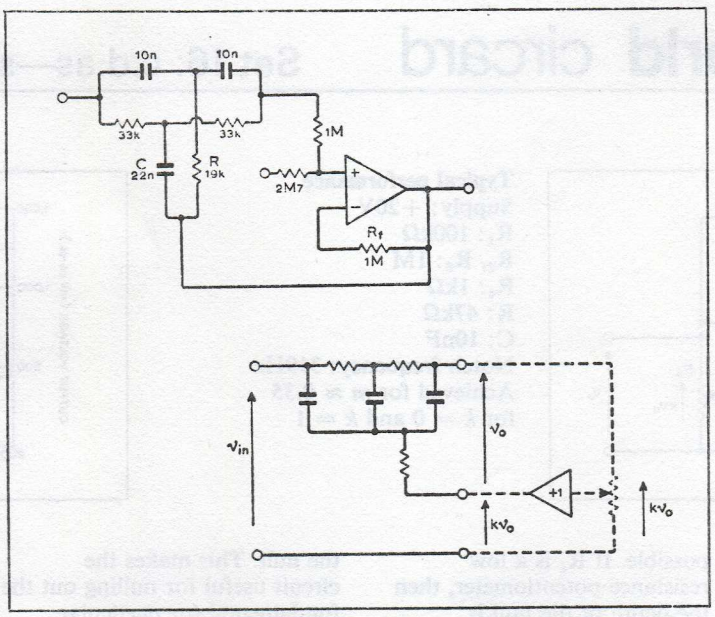
R_1 10 to 250kΩ.

R_4 1 to 10kΩ.

This circuit experiences shift in the null because of supply temperature changes and requires careful adjustment before use if sharp notch required.

Circuit modifications

● T-networks normally have the disadvantage that to control the frequency while retaining a sharp notch requires adjustment of a number of interacting components. Interconnected with an amplifier (top circuit), using positive feedback to steepen the sides of the notch (equivalent to varying the Q but not the centre frequency), it has the advantage that variations in the amplifier gain only affect the steepness leaving the depth unaffected. A further advantage accrues using the current-differencing amplifier in that the gain can be adjusted, while retaining a fixed input impedance, by varying R_f. This also affects the gain at frequencies well away from the notch, but the approach is often used where the gain is just less than unity the sides of the notch very steep and unity gain can be assumed off resonance. Independent adjustment of C and R are required to obtain a complete null and the system is easier to use if fine frequency control is possible at the oscillator, as may be possible when used as part of a distortion measuring system.



● Other passive networks have been described which give a good null at a specified frequency and though normally used as shown with a separate feedback attenuator and buffer, the network can also be used as above. By deriving the feedback directly from the output of the amplifier variable resistance of the attenuator is avoided and the need for the buffer eliminated.

Further reading

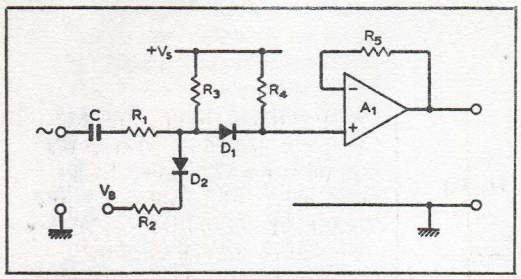
Rowe, N. B. Designing a low frequency active notch filter, *Electronic Engineering*, April 1972.

Dance, J. L. & Edwards, K. H. Simple null filter with variable notch frequency, *Electronic Engineering*. vol. 36 1964, pp.478/9.

Cross references

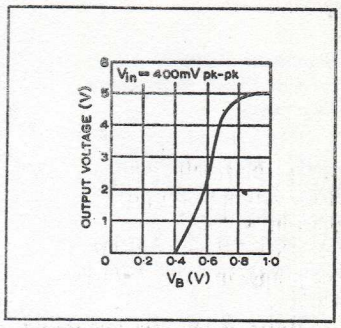
Set 1, cards 9, 10.
Set 16, cards 7, 9.

Gain-controlled amplifiers



Typical performance

Supply	+15V
A_1	¼LM3900
R_1	2.2kΩ
R_2	100Ω
R_3,R_4	100kΩ
R_5	33kΩ
C_1	10μF
v_{in}	400mV pk–pk 10kHz
for V_B	0.9V
v_o	5V pk–pk

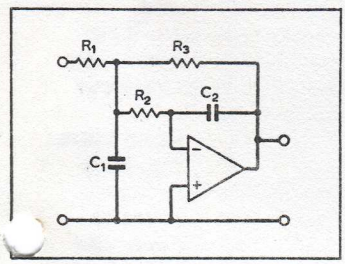


Circuit description

The non-inverting input has a diode-connected transistor as part of a current-mirror. For a given feedback resistor to the inverting input, the current flowing in the non-inverting input gives a proportional output voltage. The non-linearity of the input impedance leads to output waveform distortion if any low-resistance parallel path is used to attenuate the signal. If the path consists of a suitably-biased silicon diode then its non-linearity is comparable with that of the input stage and the input signal division between the two paths has little variation with signal amplitude, i.e. little distortion results. This remains true while the signal current is well below the bias level.

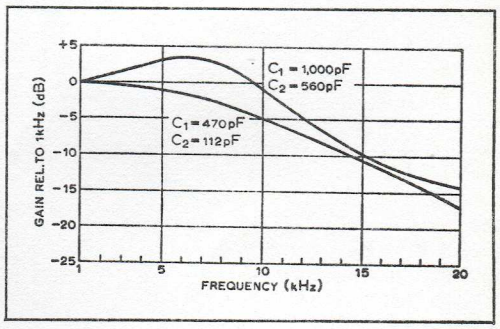
As the direct current in the diode is increased, the corresponding fall in slope-resistance by-passes more signal current reducing the gain. Resistor R_4 provides sufficient bias current to set the output potential to a minimum of $V_s/3$. This applies when the bias voltage is low with the direct current in R_3 as well as the a.c. signal current via R_1 are both shunted away through R_2, D_2. The gain is virtually zero in this condition. As V_B approaches one diode voltage, the direct currents in D_1, D_2 and the amplifier input become comparable. The slope resistances are also comparable and the input current divides equally between the amplifier and D_2. For any further increase in V_B the signal current flows on through D_1 to the amplifier with negligible attenuation by D_2. At this extreme the direct current in R_3 contributes to the amplifier bias and the output d.c. level rises to $2V_s/3$.

Low pass/high pass filters



Typical performance

Supply: 5V
R_1, R_3: 150kΩ
R_2: 47kΩ
C_1: 470pF
C_2: 120pF
−3dB point ≈ 8kHz (low frequency gain about −1)
Max. input/output swing ≈ 1V pk-pk.



Circuit description

The most convenient configuration for most feedback circuits with these amplifiers is the virtual earth configuration; it is not possible to use series applied feedback as with standard Sallen & Key type filters. The network is not easy to analyse component-by-component because of the interactions between them but the overall transfer function is well defined particularly if the gain in the pass-band is low, e.g. unity. Then it is sufficient if the amplifier voltage gain is >100 to have a transfer function that is very close to the theoretical value. A second-order low-pass filter results where the cut-off frequency may range from 1Hz to >100kHz. A convenient means of adjustment of the filter properties is via C_1, C_2. It is their product that fixed the cut-off frequency (for R_1, R_2, R_3 fixed) while their ratio determines the shape of the transfer function (i.e. Butterworth, etc.). The output impedance is low and the input impedance may be up to 1MΩ if required allowing such filters to be cascaded with negligible loading.

As shown the output voltage is defined as $(R_3/R_1 + 1)V_{be}$ provided the input has a quiescent value of zero, as would be achieved by capacitive coupling from the previous stage. Since $R_1 = R_3$ is a convenient value for design of the filter characteristics this restricts the output to a quiescent value of about 1.2V regardless of the supply. This may be inconvenient where larger voltage swings are desired and alternative biasing schemes may be needed (see Circuit modifications).

The bias range from 0 to 1V may be raised to any higher level by adding a potential divider.

Component changes

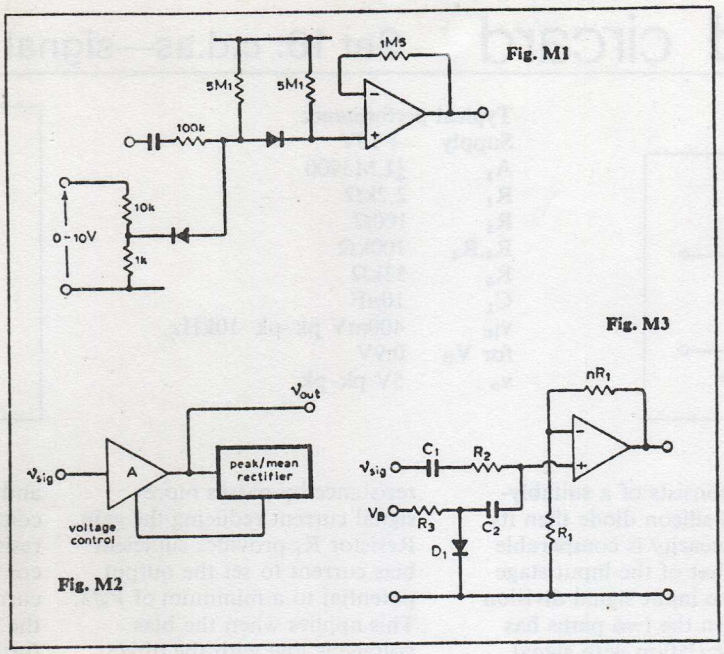
R_1 Sets input impedance 1k to 1MΩ.
R_2 Not critical but $\ll R_1$.
R_3, R_4 Normally equal, setting limits to output quiescent voltage.
$R_3 = R_4 = 3R_5$ for output levels ranging from $V_s/3$ to $2V_s/3$.
R_5 Ratio R_5/R_1 sets maximum value of voltage gain.
C_1 Not critical, but reactance $\ll R_1$ at lowest signal frequency.
D_1, D_2 Small signal silicon diodes.
V_s Whole voltage range of amplifier, 4 to 36V.
V_B Centre of gain-control region occurs for 0.6V but this is temperature dependent.

Circuit variations

● In some applications it may be more convenient to make the control voltage compatible with the normal output of other amplifiers. The potential divider raises the range of bias voltages to 0 to 10V. The component values, Fig. M1, give comparable gain figures at much higher impedance levels (taken from manufacturers application notes).

● Automatic control of output voltage against input signal variations (a.g.c.) is possible by detecting the output amplitude and feeding a smoothed control signal back to the amplifier bias input. For best control the rectified output can be compared against a direct reference voltage with the amplified difference being fed back, Fig. M2.

● A simpler circuit, Fig. M3, uses a.c. coupling between the diode being controlled by R_3 and the amplifier non-inverting input. An alternative d.c. biasing technique sets the output voltage to $(n+1)V_{be}$ provided the value of R_1 is sufficiently low that the current in it ($\approx 0.6V/R_1$) is $\gg 30nA$, the typical input current of the amplifier. Increasing the bias voltage lowers the slope resistance of D_1, diverting signal current from the amplifier input and reducing the gain (maximum gain $\approx nR_1/R_3$). The gain cannot be reduced to zero with this circuit.



Cross references

Set 16, cards 2, 3.

Component changes

Transfer function (voltage gain) is

$$\frac{\frac{1}{R_1R_2C_2C_1}}{s^2+\left(\frac{1}{R_2}+\frac{2}{R_1}\right)\frac{1}{C_1}s+\frac{1}{R_1R_2C_1C_2}}$$

where $s = j\omega$
provided $R_1 = R_3$.
This is the basic form of a second-order low-pass filter giving $\omega_n = 1/\sqrt{R_1R_2C_1C_2}$ and equivalent $Q = 1/2\xi$ where ξ is the damping factor given by

$$Q = \frac{\sqrt{R_1R_2}}{R_1+R_2}\cdot\sqrt{\frac{C_1}{C_2}}$$

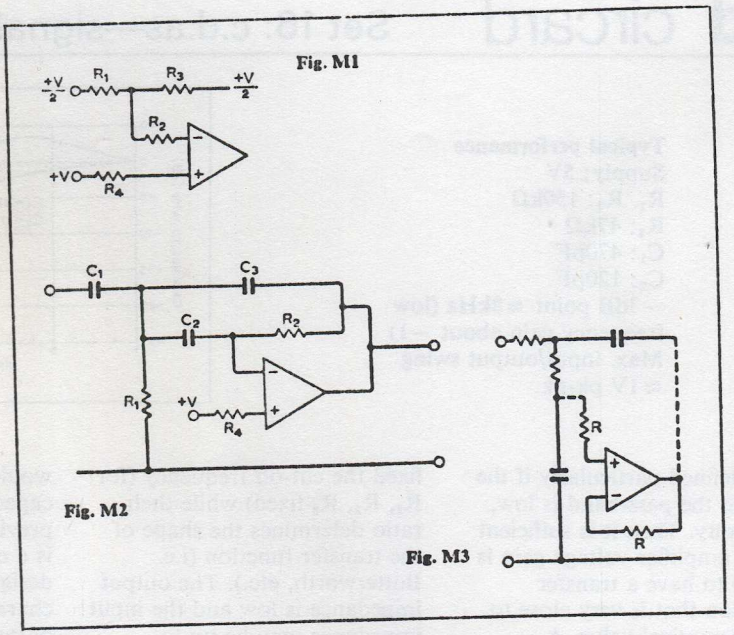
Setting R_1, R_2 to determine input impedance, C_1 and C_2 may be varied to control cut-off frequency and shape of response. Note that the equations proposed in National Semiconductor applications note AN72 pp.14-15 show a circuit as having $Q = 1$, for which the above equations suggest $Q \approx 0.4$. Measurements support the equations quoted above.
R_1, R_2 10k to 1MΩ.
C_1, C_2 47p to 10μF.

Circuit modifications

● If the filter is part of the system where it is convenient to bias input and output to $+V/2$ then the addition of resistor R_4 to the positive supply rail as shown permits this for $R_2 + (R_1 + R_3/2) = R_4$. The resistors R_1, R_2, R_3 are first selected to set the transfer function and the nearest preferred value for R_4 chosen using the given equation (Fig. M1.)

● The corresponding high-pass filter has the locations of the capacitors and resistors interchanged. Resistor R_2 is the only one contributing bias current to the inverting input leaving $R_4 = 2R_2$ as the condition for a quiescent output voltage of $+V/2$. (Fig. M2.)

● A current differencing amplifier can be adapted to behave as a voltage amplifier of defined gain—unity gain in the example, Fig. M3. R can be high in value and the loading effect on a separate passive network is light enough that filters similar to the Sallen & Key filters using voltage followers are possible.



Cross references

Set 1, cards 4, 5, 6, 7, 11
Set 5, cards 2, 3, 7, 10.
Set 16, cards 7, 8.

Current-differencing amplifiers

signal processing circuits

In the process of improving on previous designs a stage is reached where further advances are won only with great difficulty. At that point the problem has to be changed if it is to be solved. Conventional operational amplifiers have reached a very high level of performance but the demands from industry were for still lower cost and for more functions in a given space. This could be met by packing four amplifiers into a standard 14-pin dual in-line package, using two pins for the power supplies and two inputs/one output for each amplifier. Unfortunately the chip size then increases to a level where yields fall off and the cost-saving in the packaging is partially neutralized.

When this conclusion was set alongside the continuing demand for amplifiers capable of operating from a single supply such as car batteries, a discontinuity appeared in the design process—an integrated-circuit amplifier was designed that depended on the difference between two input currents for its performance rather than the voltage differencing action of the conventional operational amplifier with its input long-tailed pair. The resulting design is brilliant, simple in concept but very subtly implemented.

To take advantage of its novel characteristic the user must re-think his philosophy. Most functions that can be carried out with operational amplifiers can be carried out with current-differencing amplifiers; the configurations may look similar; the component values may be comparable. This surface conformity can obscure the underlying differences, and the user should be chary of attempting a direct transposition of familiar circuits. The problems are similar to those faced by valve designers when transistors first appeared—transistors could be forced to operate in the known valve circuits but alternative arrangements were soon found to exploit the unique properties of these cold and fragile new devices that lacked the warming glow of the familiar friends.

It is to be assumed that what we are now seeing is but the first generation of current-differencing amplifiers, devices that seek to capture the largest possible market by accepting compromises in many areas. Before this article is published there may be high frequency/low noise/high power current-differencing amplifiers on sale, but the basic design techniques should be applicable to these just as users of the 709 can transfer their skills to the super-β, infinite bandwidth, zero drift op-amps that every self-respecting manufacturer now seems able to offer. In this article two sub-circuits are discussed which when combined give the prototypical form of the current-differencing amplifier now available as a quad amplifier in 14-pin dual in-line form.

One of these sub-circuits is a very old friend. Fig. 1 shows a common-emitter amplifier driving a common-collector or emitter follower stage. The current in the input stage is low enough, while a high current gain minimizes the output impedance. If overall feedback is applied as in Fig. 2, the transimpedance of the circuit is reasonably well-defined by R_3, i.e., for an input current i, the output voltage swing is close to $-iR_3$. This is assuming high enough gains that the input behaves as a virtual earth to signals. The quiescent V_{be} of ≈ 0.6V prevents accurate low-level d.c. amplification, and this is a limitation shared by the monolithic i.c. based on this concept.

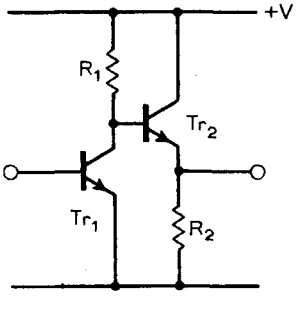


Fig. 1

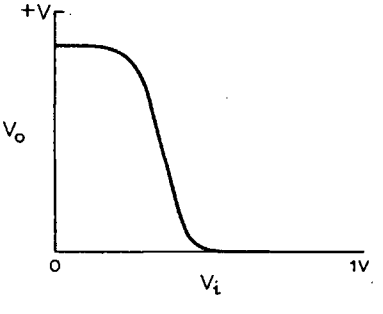


Fig. 3

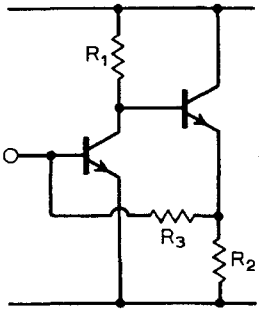


Fig. 2

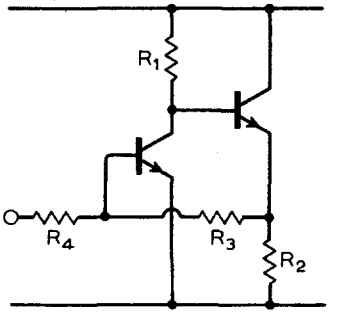


Fig. 4

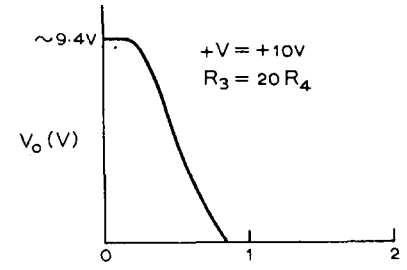


Fig. 5

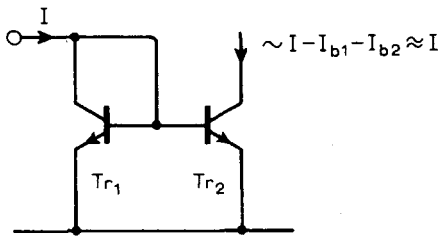


Fig. 7

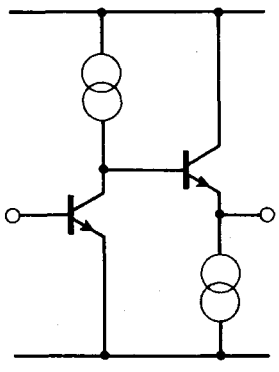


Fig. 6

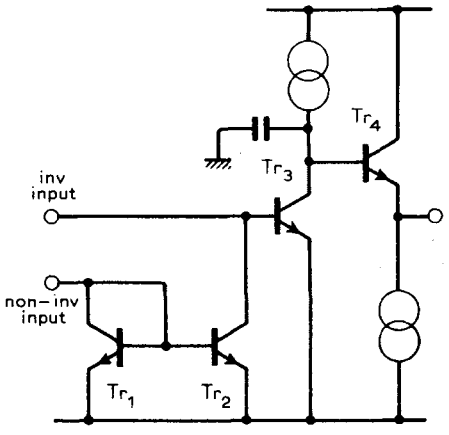


Fig. 8

Voltage transfer function, Fig. 3, is non-linear with a steep slope corresponding to a fairly high voltage gain, from a few tens to a few hundreds depending on supply voltage, resistance values, etc. An input resistor can be added to produce an elementary see-saw amplifier, Fig. 4; the resulting voltage transfer function as shown in Fig. 5 is linearized by the negative feedback. Use of a voltage source short-circuits the negative feedback in the circuit of Fig. 2 which is intended as a current in/voltage out or transimpedance stage.

The circuit is the d.c. feedback pair and is already one of the most versatile problem-solvers for the hard-pressed designer. In monolithic i.c. form the ready availability of constant-current sources allows them to replace R_1 and R_2, as in Fig. 6. Two benefits accrue. First, the increased dynamic resistance boosts the gain, and secondly the transistor currents can be tightly controlled against wide variations in supply voltage and temperature. This latter effect ensures that the voltage gain is stabilized as well as being increased.

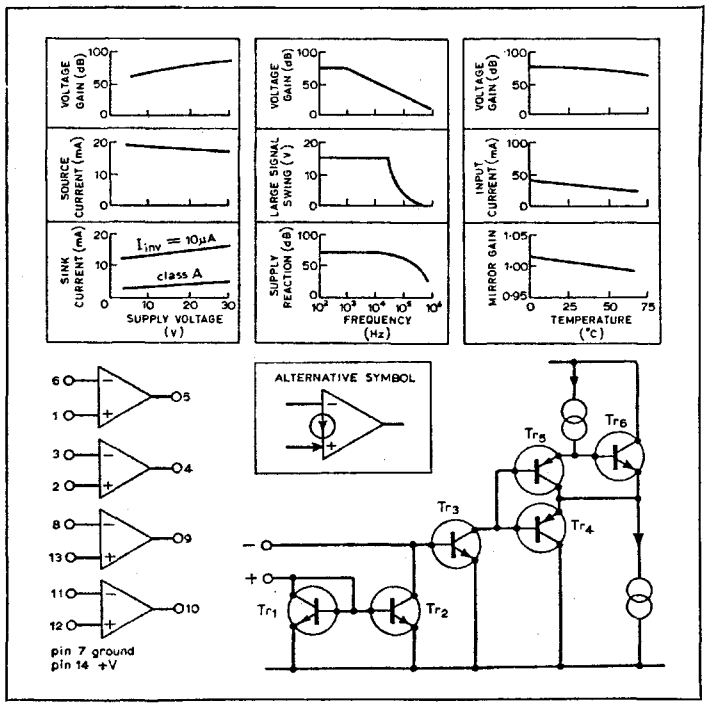
A second sub-circuit which is also well known is now added. Fig. 7 shows the current-mirror which plays the dual role in these amplifiers, to that played by the long-tailed pair in operational amplifiers. For well-matched transistors operated at equal V_{be}, the collector currents are comparable. The differences arise partly from inevitable imbalance in the transistors, partly because as shown the base currents contribute an error and partly because the collector-emitter voltages may differ. When a current-mirror is added to the d.c. feedback pair from Fig. 6 then a complete, albeit limited performance, current-differencing amplifier results (Fig. 8).

With negative feedback added the third source of error listed above is removed, because the collector potential of Tr_2 is constrained to equal that of Tr_3 base, i.e., Tr_1 and Tr_2 have comparable V_{ce} values as well as identical V_{be} values. With resistive feedback the output voltage is controlled by the difference between the two input currents. That at the inverting input would normally flow on through the feedback path (provided Tr_3 base current is small) while that at the non-inverting input is mirrored in the current drawn by Tr_2 collector, reducing the net input. Both currents are normally positive. Transistors Tr_1, Tr_2 are inoperative for negative currents while that in the inverting input may have either polarity. As a main advantage of the amplifier is that it can perform complex functions while requiring only a single-polarity supply, negative currents are not normally present except for some a.c./pulse circuits. Additional networks are provided in the practical amplifiers to clamp the inputs on negative voltage swings.

A more detailed description of the practical circuit will be given in a following article. This set of Circards (no. 16) is concerned with signal amplifying and processing, which will be followed by a series on the generation of signals and waveforms. In each of these areas novel solutions can be found, and we can only hope as users to match the ingenuity of the designers of these new amplifiers.

Current differencing amplifiers

Three sets of cards deal with current differencing amplifiers of the LM3900 kind. This set covers signal processing applications, set 17 covers signal generation and a third set deals with various other circuits including test, measurement, detection, logic and driving circuits.



Typical performance
Supply: 15V
R_L: 5kΩ
Voltage gain: 2,800 (69dB)
Output swing: 0.1 to 14.2V
Output current: source 10mA, sink 1.3mA
(overdriving inverting input increases sink current up to >30mA)
Input current: 30nA
Unity-gain bandwidth: 2.5MHz
Slew rate: +0.5V/μs, −20V/μs

N.B. Data is for National Semiconductor LM3900. A similar amplifier is available from Motorola and other manufacturers are expected to "second-source" such devices. Refer to manufacturers data sheets particularly for maximum ratings. While other current-differencing amplifiers may be expected to have similar performance in the circuits to be described it is important that the ratings of particular devices are not exceeded.

Circuit description
Transistors Tr_1, Tr_2 are a current mirror with the collector current of Tr_2, approximately equal to non-inverting input current, subtracting from inverting input current at base of Tr_3. The net input current to Tr_3 is (I−) − (I+) and this is amplified by Tr_3 with Tr_5, Tr_6 forming an improved emitter follower output stage. Constant-current generators define the operating conditions while Tr_4 comes into action on over-driving the input to maximize the sink-current. Output depends on the difference between two positive input currents with negative feedback taken to the inverting input when the gain is to be defined. The non-inverting input is outside the feedback loop, and behaves as a forward-biased p-n junction. With resistive negative feedback applied between output and inverting input, the direct currents in the two inputs will be equalized to within the accuracy of the current mirror. If the non-inverting input current is defined by a resistor to +V, the direct output voltage is then a fixed fraction of +V. Transistor Tr_3 base current is ≈30nA, allowing very low bias/signal currents, and like the voltage gain and output current capabilities is controlled over wide temperature and supply variations. An internal regulator (not shown) ensures this by providing the constant currents while also biasing a set of transistors that clamp each input to ≈ −0.3V on negative input swings.

Further reading
Frederiksen, T. M., Howard, W. M., Sleeth, R. S., The LM3900—A New Current-Differencing Quad of ±Input Amplifiers, National Semiconductor application note AN72.
Frederiksen, T. M., Norton quad amplifier subtracts from costs, adds to design options, *Electronics*, Dec. 6, 1973, pp.116-20.
Motorola Linear Integrated Circuit Data Book, pp.7-446, 7-453, 7-456 and 7-463; data sheets on MC3301P and MC3401P amplifiers.
National Semiconductor, Linear Integrated Circuits, pp.226-33, data sheets on LM3900.
Frederiksen, T. M., Howard, W. M., Sleeth, R. S., Use Current-mode IC amplifiers, *Electronic Design*, vol. 21, no. 2, Jan. 18, 1973, pp.48-55.
Mortensen, H., Use a quad amplifier to handle transducer bridge signals, *Electronic Design*, vol. 21, no. 3, Feb. 1, 1973, pp.74-6.

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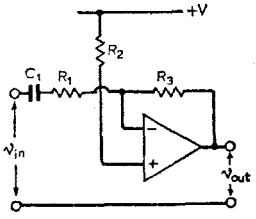
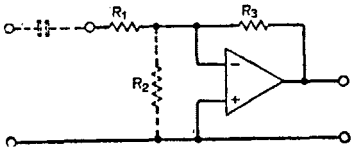
Basic amplifiers—1



Typical performance
Supply: +15V
R_1: 100kΩ
R_2: 2.2MΩ
R_3: 1MΩ
C_1: 0.1μF
Direct output voltage ≈ 7V
Voltage gain ≈ −10

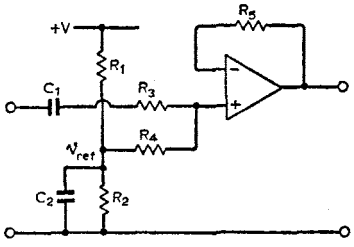
Circuit description—1
No direct current flows in R_1 and hence R_2, R_3 determine the d.c. operating conditions. For perfect balance between the input circuit transistors they will carry equal current and for $V_{be} \ll +V$, the direct output voltage is given by $R_3/R_2 \times (+V)$, i.e. $R_2 = 2R_3$ is the usual condition for maximum available voltage swing with the output biased at supply mid point. As there is no significant alternating current in R_2, it is the alternating currents in R_2 and R_1 that are equal in magnitude while the virtual earth at the inverting input (though ≈0.6V d.c.) gives a voltage gain of $-R_3/R_1$. The addition of reactive components modify the gain, so that a high-frequency roll-off is readily achieved by placing a capacitor across R_3 (corner frequency $1/2\pi R_3 C$).

Capacitive coupling may be required to the load, while the reactance of $C_1 \ll R_1$ at lowest frequency. Maximum resistance values of up to 10M may be used, but roll-off due to stray capacitances is likely.



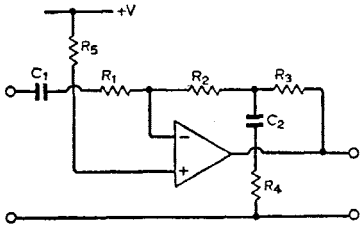
Typical performance
Supply: +15V
R_1: 470kΩ
R_3: 4.7MΩ
R_2: 470kΩ
Direct output voltage ≈ 6V
Voltage gain ≈ −10

Circuit description—2
The base-emitter voltage of the input transistor is ≈0.55V at room temperature, falling by ≈2.5mV for every 1 deg C rise in temperature and by less than this (typically 0.5 to 1mV) for each 1-V increase in the supply voltage. This voltage is thus sufficiently stable to be used as the reference voltage for setting the d.c. output conditions, and the technique may be called the "nV_{be}" biasing method. It is identical in principle to that used in the d.c. feedback pair and the "amplified-diode". If the source has an internal resistance to ground $< R_1$ then direct coupling may be used with R_1 chosen to provide the required input resistance for the circuit and R_3 determining both the voltage gain and the direct output voltage. Resistor R_2 is omitted in this mode as is the input coupling capacitor. Direct output voltage $\approx (R_3/R_1 + 1)V_{be}$. Voltage gain $\approx -R_3/R_1$. The method requires modification both for high and low gains as the direct output voltage may not be convenient. By capacitive coupling to R_1 the d.c. and gain conditions can be made independent, with direct output voltage $\approx (R_3/R_2 + 1)V_{be}$ and voltage gain $\approx -R_3/R_1$.



Typical performance
Supply: +15V
R_1: 47kΩ
R_2: 47kΩ
R_3: 100kΩ
R_4: 1MΩ
R_5: 1MΩ
C_1: 0.1μF
C_2: 1μF
Direct output voltage ≈ 7.5V
Voltage gain ≈ +9.5

Circuit description—3
A third variation on the biasing methods available, is to take the bias resistor R_4 to a separate reference voltage V_{ref} which can be decoupled to make the output voltage much less dependent on supply ripple. A single reference voltage (here equal to $+V/2$) may be used for a number of separate amplifiers. Separate control of the quiescent output conditions is by variation of R_4 for each amplifier while adjustment of R_1, R_2 varies all of them simultaneously.
The amplifier is shown with the signal applied to the non-inverting input. No feedback is available at this input and so the impedance of the input transistor affects the input current. At room temperatures, $r_i \approx 0.026/I_{R_4}$, giving a value >3kΩ for the values shown. This reduces the gain to about 3% below the simple theoretical relationship R_5/R_3. This biasing method is equally applicable to the inverting amplifiers.



Typical performance
Supply: +15V
R_1: 1MΩ
R_2: 1MΩ
R_3: 1MΩ
R_4: 10kΩ
R_5: 2.2MΩ
C_1: 0.1μF
C_2: 4.7μF
Direct output voltage ≈ 7V
Voltage gain ≈ −95

Circuit description—4
The value of the feedback resistor is limited to a few megohms for several reasons (bias instability, effect of stray capacitance, noise and hum). If it is required to have a high input resistance and high voltage gain than the a.c. and d.c. feedback must be different. As shown, R_4 and R_3 constitute a potential divider for the output signal while only R_3 is involved in the d.c. feedback. Output voltage has a quiescent value of $+V(R_2 + R_3)/R_5$. Voltage gain is $\approx (-R_2/R_1)(R_3/R_4 + 1)$. Where $R_2 = R_1$, a convenient condition, the voltage gain simplifies to $-(R_3/R_4 + 1)$. However when the ratio R_3/R_4 is large the feedback theory demands that the limited open-loop gain be taken into account. In practice, a ratio that should set the gain to −20 will do so to within about 1%, while a nominal gain of −100 would be nearer to −95.

Cross references
Set 5, cards 5, 8, 9, 10.
Set 7, cards 4, 10.
Set 10, cards 1, 9.
Set 16, cards 2, 5, 6, 10.

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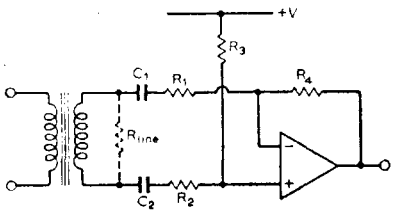
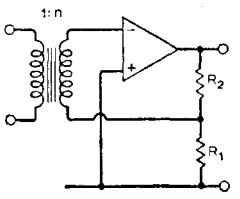
Set 16: c.d.as—signal processing—3

Basic amplifiers—2



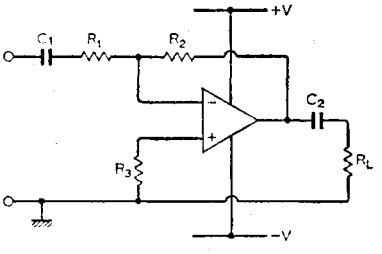
Typical performance
Supply: +15V
R_1, R_2: 10kΩ
R_3: 220kΩ
R_4: 100kΩ
C_1: 1μF
C_2: 1μF
Direct output voltage ≈ 7V
Voltage gain ≈ −10
(transformer secondary to output)

Circuit description—1
Common-mode signals are a problem when transmission over lines has to take place in a noisy environment. By coupling the signals through a transformer such common mode signals are minimized, while the anti-phase inputs of the current differencing amplifier offer a further improvement. Any common-mode voltage at the transformer secondary produces equal currents at the two inputs largely cancelling each other because the gain at the two inputs is equal and opposite. R_{line} is inserted to achieve the correct loading on the source with R_1, R_2 sufficiently larger not to affect that loading. Quiescent output voltage ≈ $V(R_4/R_3)$; voltage gain ≈ $-R_4/R_1$.



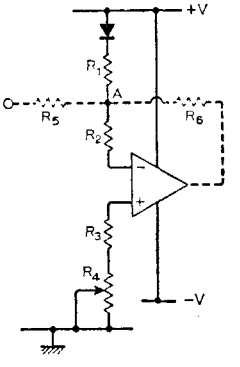
Typical performance
Supply: +15V
R_1: 10kΩ
R_2: 100kΩ
Direct output voltage ≈ 6V
Voltage gain ≈ 11
(transformer secondary to output)

Circuit description—2
Where the source is inductive or is to be transformer-coupled, a variant of the "nV_{be}" biasing method provides a simple solution. Again there is the restriction that the direct output voltage and the gain of the amplifier itself are controlled by the same resistor ratio but decoupling part of R_1 to ground can make the ratio for signal frequencies ≫ the ratio at d.c. if required. In the extreme case, R_1 can be completely decoupled giving the full open-loop gain of the amplifier. This coupled with the step-up turns ratio of the transformer gives a very high overall gain. As shown, the overall voltage gain is ≈ $n(R_2/R_1+1)$ and the quiescent output voltage is ≈ $(R_2/R_1+1)V_{be}$. Because the input current required by the amplifier is very small (≪ 1μA) the effective input impedance remains high regardless of the gain, and high step-up ratios are possible. This yields a very sensitive microphone amplifier though the noise performance is unlikely to allow use in audio applications.



Typical performance
Supply: ±15V
R_1: 100kΩ
R_2, R_3: 1MΩ
R_L: 10kΩ
C_1: 0.1μF
C_2: 1μF
Direct output voltage ≈ 0V
Voltage gain ≈ −10

Circuit description—3
The biasing techniques described above are easily adapted for dual supply operation, making the amplifier compatible with standard op.amp. ±15V systems. One method is to bias the non-inverting input from the centre rail, leaving the same p.d. across R_2 and R_3 if $R_2 = R_3$, i.e. the output is substantially at 0V if the amplifier has well-matched inputs. This remains true for all values of positive and negative supply voltages including those cases where they are markedly unequal in value. R_1 plays no part in the d.c. conditions and is chosen for the desired gain/input resistance. Voltage gain ≈ $-(R_2/R_1)$. Non-inverting gain is obtained as before simply by transferring R_1 to the non-inverting input. The gain is less well-defined but the bandwidth is increased, because there is then no resistor to attenuate the negative feedback, i.e. the bandwidth can approach that of the amplifier with 100% feedback while the gain can approach the value defined by (R_2/R_1).



Typical performance
Supply: ±15V
R_1, R_2: 1MΩ
R_3: 820kΩ
R_4: 500kΩ
R_5: 220kΩ
R_6: 2.2MΩ
Direct output voltage ≈ 0V
Voltage gain ≈ −10

Circuit description—4
The present form of current-differencing amplifier is not suited to low-level d.c. amplification and cannot replace standard operational amplifiers directly. The adaptation shown has a reasonable performance for d.c. signals of >100mV provided the offset adjustment is made and subsequent changes in temperature and supply are restricted. Effective input of the amplifier is point A and for $R_1 = R_2$ its potential is a 0V in the absence of feedback (the diode compensates for the input V_{be}). Adjusting R_4 sets the output voltage to 0V prior to the application of feedback with $(R_3 + R_4) \approx (R_1 + R_2)/2$. The resistors R_5, R_6 then set the input resistance and gain as for previous amplifiers. Point A is no longer such a good equivalent to a virtual earth from the signal standpoint since the presence of R_2 lowers the amplifier gain, while $R_2//R_1$ is the equivalent resistance to ground at this point.

Cross references
Set 5, cards 5, 8, 9, 10.
Set 7, cards 4, 10.
Set 10, cards 1, 9.
Set 16, cards 1, 5, 6, 10.

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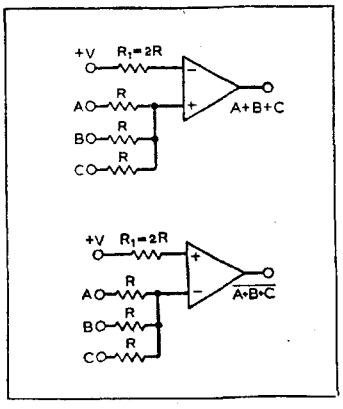
Logic gates



Typical performance
Supply: +20V
IC: ¼ LM3900
R_1: 150kΩ
R: 82kΩ
Output logic 0: 150mV
Output logic 1: 19.2V
For inputs commoned, output changes state for input voltage ≈ 20% of +V.

Circuit description
Availability of two current inputs simplifies the design of basic logic gates with these amplifiers. For example, a low current at one input can hold the output in one desired state while the other input receives the sum of the currents from two or more inputs. This sum can be set to overcome the bias when only one input is high or only if all are simultaneously high, leading to OR and AND-type circuits respectively. (The amplifier is working as a high-gain comparator and can also provide a majority-gate in which any two out of three inputs are enough to provide the required output. By extension some of the simpler forms of threshold logic are possible by scaling the values of resistors to assign a different weight to their importance in decision making.) In the first configuration, if any input is high the current driven into the non-inverting input exceeds the inverting input current and the output is driven high, i.e. an OR gate. The remaining input resistors connected to logic 0 bypass a small portion of that current ($<0.5V/R$ for each resistor) but unless the number of inputs is large and/or the supply voltage is low, this is not a problem. Speed of response is limited to ≈0.5V/μs for positive swings and up to 20V/μs for negative swings though the fall in voltage is slower as logic 0 is approached. By interchanging the inverting and non-inverting inputs with no change in component values, a NOR gate is produced. This flexibility of being able to produce different logic functions from the same package is very attractive. In addition, one or more of the amplifiers can be used to provide astable, Schmitt trigger functions, etc. for obtaining the appropriate waveforms with which to drive the gates.

Component changes
+V Normal voltage range is +4 to +36V, but some devices will operate to <3V without difficulty.
R_1, R Ratio of these resistances is chosen to ensure that with the lowest expected value of logic 1 to any one input that, the resulting current flow into the non-inverting input is sufficient to overcome the fixed current in the positive input. (Allow for $0.5V/R$ lost in each logic 0 input.) Typically $R = R_1/2$ is a suitable starting point and R may vary from 10k to 10MΩ.
Fan-out To maximize this R, R_1 should be large but there is no great advantage to raising them above 1MΩ.

Circuit modifications
- The AND/NAND functions are slightly more difficult to construct for multiple inputs. This is because for an *n*-input gate the sum of the currents produced by (*n*-1) inputs at logic 1 differs little from that produced by *n* inputs if *n* is large. Up to three inputs can be used with a reasonable margin of safety as in Fig. M1, where the resistor R_2 reduces the current flow when two inputs are on. For a two-input AND gate R_2 may be omitted and the values of the input resistors adjusted. For example, with R_1 82kΩ, R 100 or 120kΩ.
- Again interchanging the inverting and non-inverting inputs gives a NAND gate. By scaling the resistors in some of these and/or feeding signals to both inputs, circuits which are intermediate between true analogue and true digital circuits become possible. (Fig. M2)
- If it is required to have multiple inputs to an AND gate, simple diode gating may be used, Fig. M3, with the amplifier serving a similar function to the transistors in d.t.l., but with the advantage that the ratio of output to input current, which determines the fan-in fan-out capability, is of the order 10^6 (25nA—25mA). If any input is at logic 0 the current in R_1 flows through that diode. All inputs have to be at logic 1 for the current to be diverted into the amplifier non-inverting input to give a logic 1 out. The threshold voltage and hence the noise margin is low in this circuit. If all inputs but one are at logic 1 then that input need only rise to ≈ 0.5V to be recognized as logic 1. A NAND function is obtained by reversing the amplifier inputs.

Fig. M1

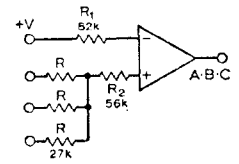


Fig. M2

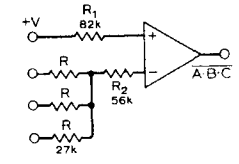
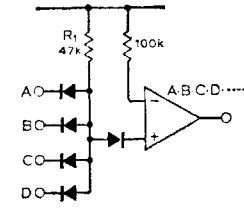
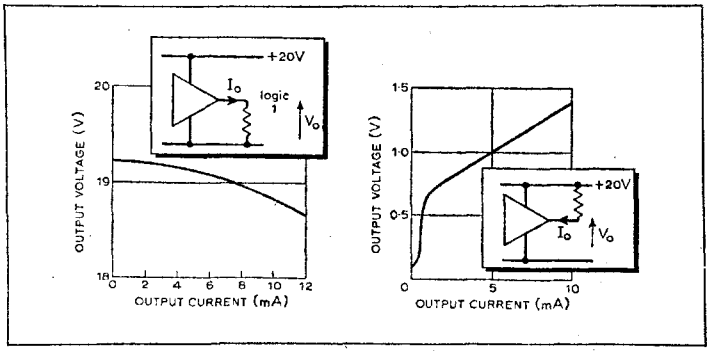


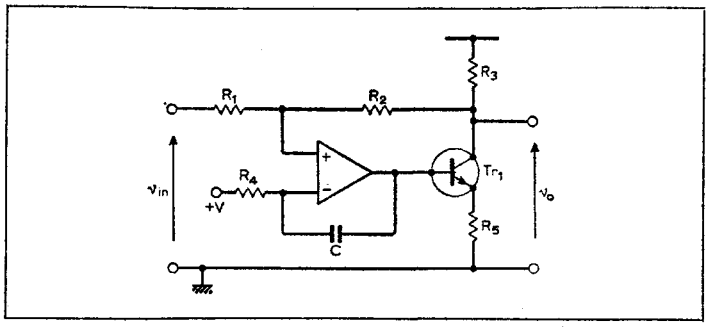
Fig. M3



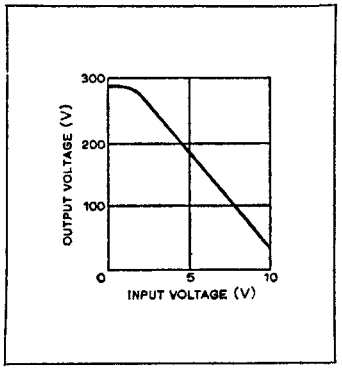
Cross references
Set 11, cards 1, 2, 11.



High voltage amplifiers



Typical performance
Supply: +15V, +300V (HT)
R_1: 330kΩ
R_2: 10MΩ
R_3, R_4: 470kΩ
R_5: 1kΩ
C_1: 100pF
Voltage gain: −31.2 (d.c. to 1kHz)
Cut-off frequency: 3kHz
Output impedance: <10kΩ (d.c. to 1kHz)
Input impedance: 330kΩ (d.c. to 1kHz)



Circuit description
Where a high output voltage swing is required the amplifier must be fed from a separate low-voltage supply, and a suitable high-voltage transistor employed to withstand the main supply voltage. The configuration depends on whether it is the output voltage or current that is to be defined. If the former, then the feedback is taken from in shunt with the load. For an inverting-gain amplifier and the transistor in the common-emitter mode, the inverting gain of the transistor necessitates that the feedback be applied to what is normally considered as the non-inverting input. For an input of 0V d.c., the current flow in R_1 is small and that in R_2 is forced by the feedback to equal that in R_4. If in this condition the output is desired to be $+HT$ then $+HT/R_2 = +V/R_4$ gives the required value of R_4. Overall voltage gain is given by $(-R_2/R_1)$ as the circuit is effectively a "see-saw" amplifier while the input resistance is approximately R_1. Resistance R_5 introduces a small amount of negative feedback into the output stage and raises the amplifier quiescent voltage well into its linear region. Capacitor C_1 modifies the gain/frequency characteristic to maintain stability at the higher loop gain. Output voltage swing can be up to 95% of the supply voltage if lightly loaded and the negative feedback keeps the output impedance reasonably low.

Component changes
R_1, R_2 These set the input resistance and the voltage gain $R_2 \gg R_3$ to minimize loading on the output. R_2 1M to 22MΩ.
R_3 Load resistance, dictated by user requirements. For use as an r.c.-coupled amplifier, R_3 has to carry a quiescent current greater than peak load current required.
R_4 Sets d.c. conditions at output. If $V_o = +HT$ required for $V_{in} = 0$, then $+V/R_4 = +HT/R_2$. If output quiescent to be $+HT/2$ as when used for amplifying a.c. input signal, then $+V/R_4 = +HT/2R_2$.
R_5 Not critical. Raises amplifier output quiescent voltage to 1 to 3V range, i.e. into linear region. Value dependent on output quiescent current but might be 50Ω to 5kΩ.
+V Chosen to suit amplifier, and available supplies (+4 to +36V).
+HT Dictated by load requirements.
Tr_1 Must have voltage rating in excess of +HT particularly if inductive loading possible.

Circuit modifications
- A non-inverting amplifier again using a common emitter output stage has the feedback applied to the amplifier non-inverting input, while the signal is applied to the inverting input (the inversion in the transistor ensuring the correct overall sign for the gain). For a transfer function that passes through the origin a pre-biasing network is required. Again the gain is set by the ratio of the feedback to the input resistor.
- For a high output-impedance, the feedback is taken from the transistor emitter. The method can be employed where the load is to be transformer coupled and the direct voltage drop across the primary is too small to allow of the d.c. feedback. The two 10-MΩ resistors define the potential at the transistor emitter as about $2V_{be}$ and allows the output current to be fixed reasonably accurately, falling with rise in temperature. By decoupling the emitter and taking overall a.c. feedback from the load, the output impedance can still be made low if required.
- Increased output resistance is possible by using compound output stages of various kinds that can also increase the current capability, subject to device power limitations. An f.e.t. draws no current from the amplifier ensuring that the load and emitter resistor currents change together if the current I_{bias} is made constant, either because of the high supply voltage and correspondingly high resistance R, or by a separate low-voltage constant-current stage.

Cross references
Set 7, cards 5, 7.
Set 16, cards 1, 2, 6.

Fig. 1

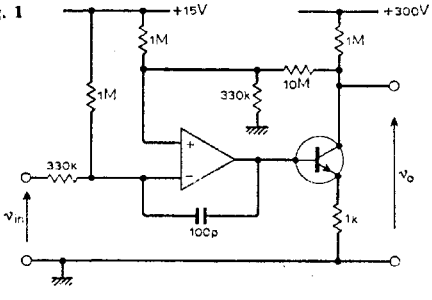


Fig. 2

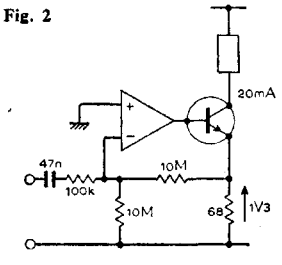
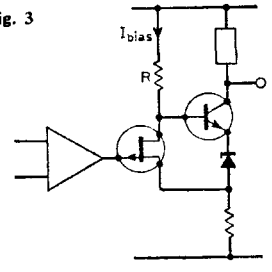


Fig. 3



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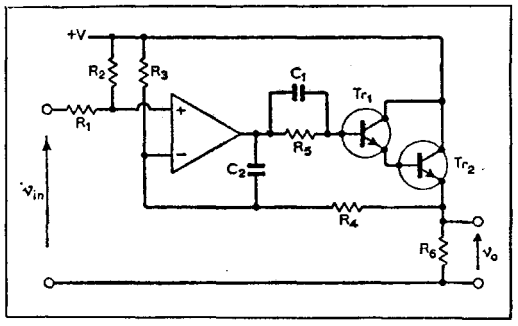
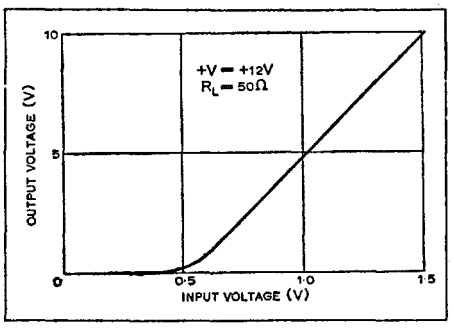
Power amplifiers



Typical performance

Supply: +10V
R_1: 100kΩ
R_2, R_3, R_4: 1MΩ
R_5: 1kΩ
R_6: 50Ω
C_1: 1nF
C_2: 10pF
Tr_1: BFR41
Tr_2: TIP3055
V_1: 1.03V
V_o: 5.0V
Voltage gain: 9.7
Change in V for
I_L of 0-1A 0.05%
V_s of 10-14V 0.5%



Circuit description

Addition of a Darlington-connected pair of transistors increases the output current capability from 10mA to 1-5A depending on the ratings of the transistors used. One restriction is that the V_{be}'s of the transistors limit the output voltage to around 2.5V below the supply level allowing for the amplifier internal saturation. The additional phase shifts that may occur even in an emitter follower make external compensation desirable. For supply, input and output to be all positive, the configuration shown is adequate, where with $R_2 = R_3$, V_o varies linearly with V_i provided V_i is above the amplifier internal V_{be}. The relationship is then $V_o \approx V_{be} + (R_4/R_1)(V_i - V_{be})$ as the currents in R_1 and R_4 have to be equal. This means that as a d.c. amplifier it is of relatively low accuracy but is quite suitable for supplying small d.c. motors under the control of a phase-locked loop. A combination of the techniques for increasing the current ratings and voltage could allow the production of high-power amplifiers. Replacing the emitter follower stages by common emitter amplifier increases the available positive output swing to within a hundred millivolts of the positive supply.

Component changes

R_1 This sets the voltage gain in conjunction with R_4. Because of the V_{be} offset, the output voltage becomes temperature dependent particularly for V_i comparable to V_{be}, i.e. high gains are not compatible with good stability in this configuration. R_1 100k to 10MΩ.

R_2, R_3 These provide forward bias for each of the inputs allowing the output to be controlled for inputs down to zero. This is best achieved for $R_1 = R_4$ when $V_o = V_i$ is the first-order approximation, the V_{be} effects at the two inputs cancelling.

R_4 As suggested, R_4 may equal R_1 for optimum stability but with gain restricted to +1. $R_4 \geq 2.0R_1$ except for a.c. amplifiers where some drift in quiescent conditions is acceptable.

R_5 1kΩ. Together with C_1 is part of the suggested network for maintaining stability. Limits amplifier current under load short circuit conditions providing protection for amplifier and output stage. Not adequate unless proper heat-sinking used since limit of output current depends on transistors' current-gains and is ill defined.

C_1, C_2 Control high frequency performance. C_1: 330p to 2.2nF, C_2: 5.6 to 22pF. Choose lowest values giving stability under operating conditions.

R_6 Load resistance. This may range down to 10Ω as currents of several amps are possible.

Circuit modifications

- A simpler circuit based on the same principles is Fig. M1. The limiting and compensation components have been eliminated together with the high-power transistor. The bias network shown is suitable for a source with resistive path to ground ≪470kΩ, with the non-inverting input grounding. The bias method is then basically the "nV_{be}" method as in the "amplified diode". Alternatively a capacitively coupled source may be used with no direct current in R_2 and $R_1 \approx 2R_3$ to set $V_o \approx +V/2$.
- For higher efficiency the usual Class B technique can be applied with a complementary-symmetry output (Fig. M2). Not recommended for low-distortion applications, since additional bias networks to overcome crossover problems would lose the advantage of simplicity normally offered by this amplifier.
- Although the supply voltage capability is good (up to 36V) the output swing can be extended to ≈70V (Fig. M3) using a bridge configuration. The simplest arrangement for a.c. signals has the 1MΩ and 470kΩ resistors setting the output quiescent voltages to $+V/2$ for maximum undistorted voltage swing. Replacing the two input resistors by a potentiometer and applying the signal via the pot to opposite-phase inputs gives anti-phase outputs that can be set for equal magnitude with an overall voltage gain of about 18.

Cross references

Set 7, cards 2, 4, 7, 8, 10, 11.
Set 16, card 5.

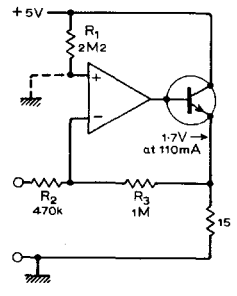


Fig M1

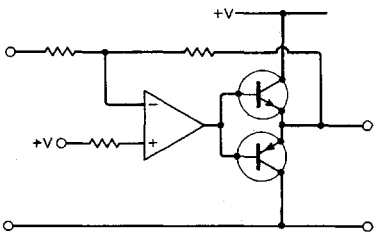


Fig. M2

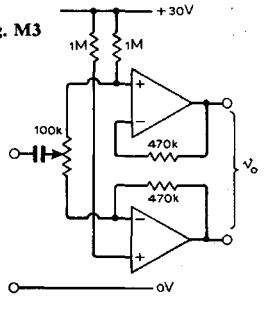


Fig. M3

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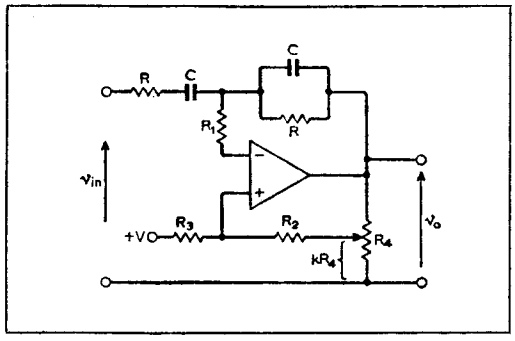
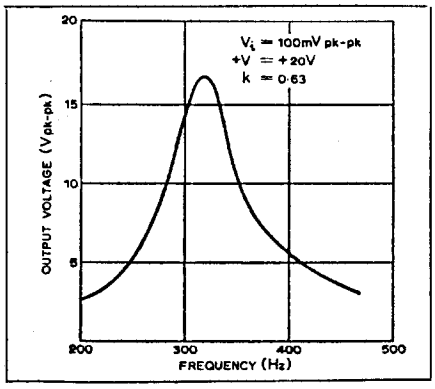
Bandpass filters



Typical performance
R: 47kΩ
C: 10nF
R_1, R_2: 1MΩ
R_3: 6.8MΩ
R_4: 100kΩ
Supply: +15V
f_o: 320Hz
For $Q = 15$
$k = 0.640$
N.B. Onset of oscillation at $k = 0.648$ compared with theoretical value of 0.66.



Circuit description
Active filter techniques based on operational amplifiers are applicable to current-differencing circuits. That shown is a direct adaptation of Circard 1, Set 1. A Wien network is placed between source and output with the potential at its junction monitored by the amplifier input terminal. Resistor R_1 is a high-value resistance to minimize loading on the network. Resistor R_2 provides a variable amount of positive feedback to increase the Q of the circuit with minimal effect on the centre-frequency while R_3 sets the quiescent output voltage to allow for maximum signal swing. Because $R_2 > R_1$ would be required for stability, with R_3 taken directly to the output, and variable high-value resistors are inconvenient, the alternative is to tap R_3 onto a variable portion of the output voltage. The result is a band-pass filter with centre frequency given by $f = 1/2\pi CR$ and with Q controlled by R_4. The limited gain and bandwidth capabilities of the amplifier does not allow the circuit to provide large stable Qs nor to operate successfully at frequencies ⩾10kHz. The input impedance falls as the Q is increased because of the increased output swing (gain ∝ Q to a first order). It is also true that the sensitivity of such circuits to variations in component values is proportional to the Q, i.e. for $Q = 10$ a 1% change in a critical resistor might produce >10% variation in the Q itself.

Component changes
R, C The load on the output should not fall much below 10kΩ at any frequency to avoid loss of loop gain, distortion, etc. R 10k to 1MΩ, C 220p to 10μF
R_1 Used to set a convenient level of current at amplifier inputs; too low and loading on Wien network disturbs Q, f_o; too high and stray capacitive coupling disturbs response. 220k to 10MΩ.
R_2 Convenient to set $R_2 = R_1$ using R_4 to control feedback. Alternatively for fixed Q particularly if low, eliminate R_4 taking R_2 directly to output. Then $R_2 > 1.5R_1$.
R_4 Not critical, but ⩾10kΩ and <R_2.
R_3 Sets quiescent output voltage for maximum swing. Should be chosen after other components have been selected for desired response. Typically 2 to 10 × R_1, but for a given value, small variations in k and hence Q can be accommodated without serious bias changes.

Circuit modifications
- Multiple feedback circuits (Fig. M1) are the equivalent of the virtual earth circuits used with conventional operational amplifiers. With correct scaling of resistors, capacitors $Q > 1$ is achieved simultaneously with centre-frequency gain of unity. Again both are strongly dependent on component stability at high-Q values.
- A better approach to filter design with current-differencing amplifiers is to select passive networks whose transfer-function gives a defined output current. It is possible to adapt the Wien and similar networks, Fig. M2. Normally R_2 would be grounded and the p.d. across it fed back to a high impedance point on the amplifier. By feeding back the current in R_2 into what is almost equivalent to an a.c. virtual earth point, the overall transfer function can be varied more easily. Components $R_{1,2}$ $C_{1,2}$ determine $f_o = 1/2\pi\,(R_1R_2C_1C_2)^{\frac{1}{2}}$, while R_5 sets the Q and R_4 the quiescent output value.
- Any of the other RC networks used in bandpass filter designs are applicable and Fig. M3 gives almost identical performance for $R_1 = R_2 = R$, $C_1 = C_2 = C$.

Cross references
Set 1, cards 1, 3, 6, 7, 8, 12.
Set 5, cards 6, 10.
Set 10, card 8.
Set 16, cards 8, 9.

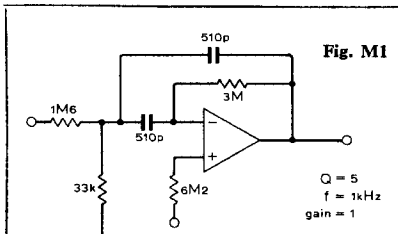


Fig. M1

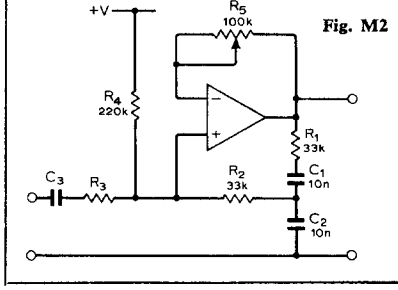


Fig. M2

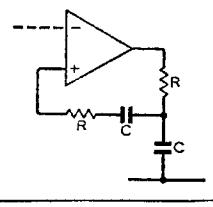
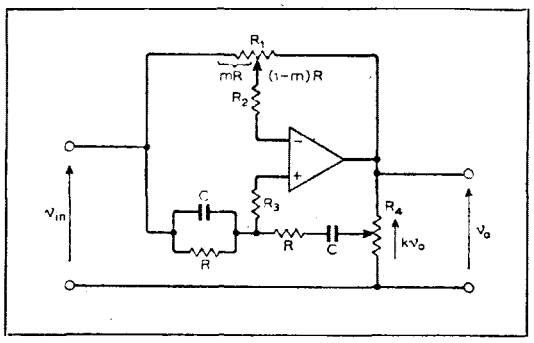
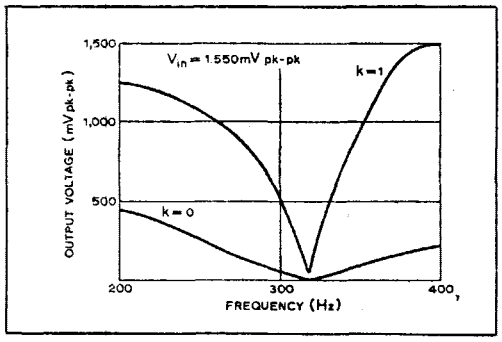


Fig. M3

Notch filters



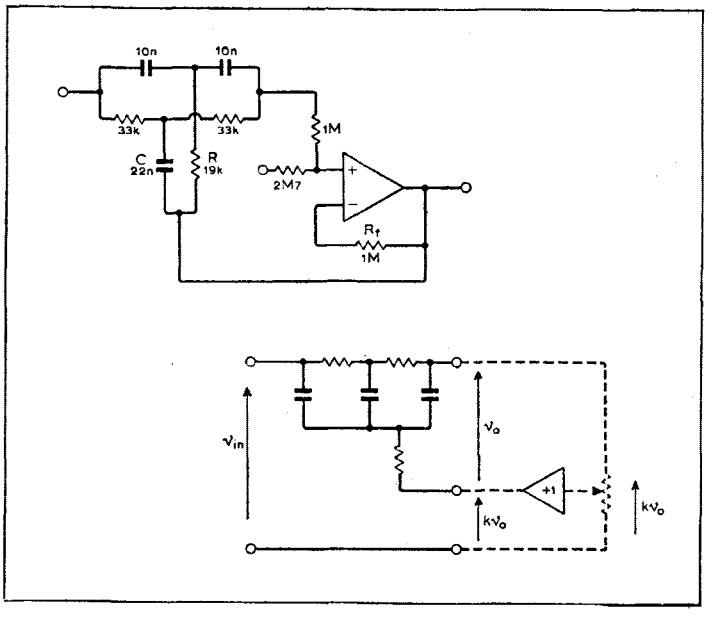
Typical performance
Supply: +20V
R_1: 100kΩ
R_2, R_3: 1M
R_4: 1kΩ
R: 47kΩ
C: 10nF
Notch frequency: 319Hz
Achieved for $m \approx 0.35$
for $k = 0$ and $k = 1$



Circuit description
The circuit is again derived from a Wien Bridge to demonstrate the principles by which known circuits can be adapted to current-differencing amplifiers. It provides a notch or null in the response at a frequency set by the RC values ($f = 1/2\pi RC$) with R_1 providing a trimming action to get as true a null as possible. If R_4 is a low resistance potentiometer, then the depth of the null is unaffected as the tapping point is varied, since both ends of the potentiometer are at zero for this condition. However, the positive feedback introduced has the effect off-null of sharpening up the response so that the gain remains close to unity for frequencies close to the null. This makes the circuit useful for nulling out the fundamental (or particular harmonic) of a complex waveform with minimal effect on the other harmonics. A weakness of this particular circuit is that it relies on the matching of the inverting and non inverting input sensitivities making it prone to variation with supply/ temperature changes, etc.

Component changes
R, C The difficulty with this particular circuit is that these should have a low impedance compared with R_3 so that the latter does not load them, while not in turn being disturbed by the varying source resistance of R_4 as k is varied. Typically R 10 to 100kΩ with C to give frequency as $f = 1/2\pi RC$ C, 220p to 10μF.
R_2, R_3 1 to 10MΩ. At higher frequencies stray capacitance effects bring phase shifts preventing good null.
R_1 10 to 250kΩ.
R_4 1 to 10kΩ.
This circuit experiences shift in the null because of supply temperature changes and requires careful adjustment before use if sharp notch required.

Circuit modifications
- T-networks normally have the disadvantage that to control the frequency while retaining a sharp notch requires adjustment of a number of interacting components. Interconnected with an amplifier (top circuit), using positive feedback to steepen the sides of the notch (equivalent to varying the Q but not the centre frequency), it has the advantage that variations in the amplifier gain only affect the steepness leaving the depth unaffected. A further advantage accrues using the current-differencing amplifier in that the gain can be adjusted, while retaining a fixed input impedance, by varying R_f. This also affects the gain at frequencies well away from the notch, but the approach is often used where the gain is just less than unity the sides of the notch very steep and unity gain can be assumed off resonance. Independent adjustment of C and R are required to obtain a complete null and the system is easier to use if fine frequency control is possible at the oscillator, as may be possible when used as part of a distortion measuring system.



- Other passive networks have been described which give a good null at a specified frequency and though normally used as shown with a separate feedback attenuator and buffer, the network can also be used as above. By deriving the feedback directly from the output of the amplifier variable resistance of the attenuator is avoided and the need for the buffer eliminated.

Further reading
Rowe, N. B. Designing a low frequency active notch filter, *Electronic Engineering*, April 1972.
Dance, J. L. & Edwards, K. H. Simple null filter with variable notch frequency, *Electronic Engineering*. vol. 36 1964, pp.478/9.

Cross references
Set 1, cards 9, 10.
Set 16, cards 7, 9.

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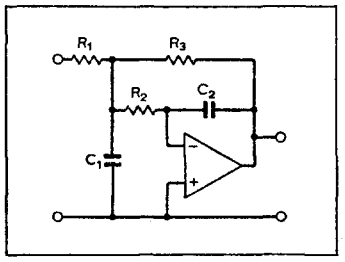
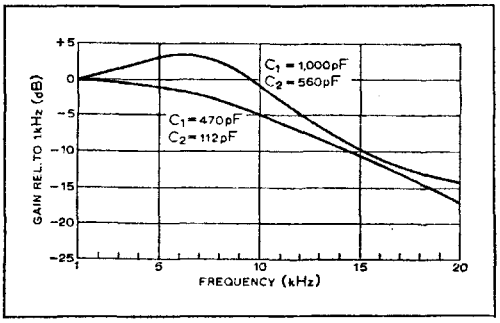
Low pass/high pass filters



Typical performance
Supply: 5V
R_1, R_3: 150kΩ
R_2: 47kΩ
C_1: 470pF
C_2: 120pF
−3dB point ≈8kHz (low frequency gain about −1)
Max. input/output swing ≈1V pk-pk.



Circuit description
The most convenient configuration for most feedback circuits with these amplifiers is the virtual earth configuration; it is not possible to use series applied feedback as with standard Sallen & Key type filters.
The network is not easy to analyse component-by-component because of the interactions between them but the overall transfer function is well defined particularly if the gain in the pass-band is low, e.g. unity. Then it is sufficient if the amplifier voltage gain is >100 to have a transfer function that is very close to the theoretical value. A second-order low-pass filter results where the cut-off frequency may range from 1Hz to >100kHz. A convenient means of adjustment of the filter properties is via C_1, C_2. It is their product that fixes the cut-off frequency (for R_1, R_2, R_3 fixed) while their ratio determines the shape of the transfer function (i.e. Butterworth, etc.). The output impedance is low and the input impedance may be up to 1MΩ if required allowing such filters to be cascaded with negligible loading.
As shown the output voltage is defined as $(R_3/R_1+1)V_{be}$ provided the input has a quiescent value of zero, as would be achieved by capacitive coupling from the previous stage. Since $R_1 = R_3$ is a convenient value for design of the filter characteristics this restricts the output to a quiescent value of about 1.2V regardless of the supply. This may be inconvenient where larger voltage swings are desired and alternative biasing schemes may be needed (see Circuit modifications).

Component changes
Transfer function (voltage gain) is

$$\frac{\dfrac{1}{R_1R_2C_2C_1}}{s^2+\left(\dfrac{1}{R_2}+\dfrac{2}{R_1}\right)\dfrac{1}{C_1}s+\dfrac{1}{R_1R_2C_1C_2}}$$

where $s = j\omega$
provided $R_1 = R_3$.
This is the basic form of a second-order low-pass filter giving $\omega_n = 1/\sqrt{R_1R_2C_1C_2}$ and equivalent $Q = 1/2\xi$ where ξ is the damping factor given by

$$Q = \frac{\sqrt{R_1R_2}}{R_1+R_2}\cdot\sqrt{\frac{C_1}{C_2}}$$

Setting R_1, R_2 to determine input impedance, C_1 and C_2 may be varied to control cut-off frequency and shape of response. Note that the equations proposed in National Semiconductor applications note AN72 pp.14-15 show a circuit as having $Q = 1$, for which the above equations suggest $Q \approx 0.4$. Measurements support the equations quoted above.
R_1, R_2 10k to 1MΩ.
C_1, C_2 47p to 10μF.

Circuit modifications
● If the filter is part of the system where it is convenient to bias input and output to $+V/2$ then the addition of resistor R_4 to the positive supply rail as shown permits this for $R_2+(R_1+R_3/2) = R_4$. The resistors R_1, R_2, R_3 are first selected to set the transfer function and the nearest preferred value for R_4 chosen using the given equation (Fig. M1.)
● The corresponding high-pass filter has the locations of the capacitors and resistors interchanged. Resistor R_2 is the only one contributing bias current to the inverting input leaving $R_4 = 2R_2$ as the condition for a quiescent output voltage of $+V/2$. (Fig. M2.)
● A current differencing amplifier can be adapted to behave as a voltage amplifier of defined gain—unity gain in the example, Fig. M3. R can be high in value and the loading effect on a separate passive network is light enough that filters similar to the Sallen & Key filters using voltage followers are possible.

Cross references
Set 1, cards 4, 5, 6, 7, 11
Set 5, cards 2, 3, 7, 10.
Set 16, cards 7, 8.

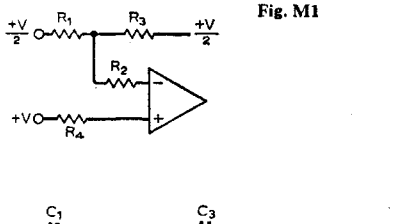


Fig. M1

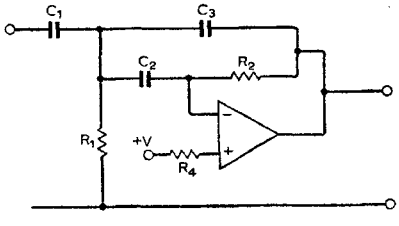


Fig. M2

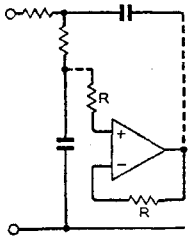
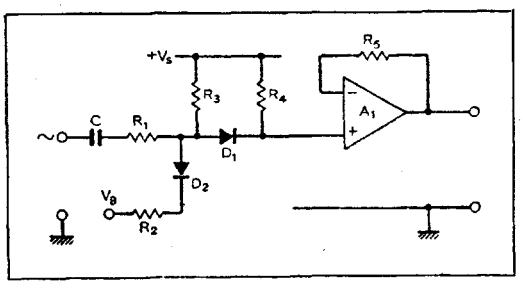


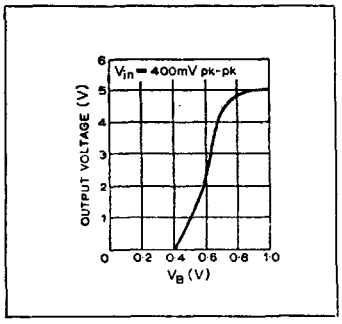
Fig. M3

Gain-controlled amplifiers



Typical performance

Supply	+15V
A_1	¼LM3900
R_1	2.2kΩ
R_2	100Ω
R_3,R_4	100kΩ
R_5	33kΩ
C_1	10μF
v_{in}	400mV pk-pk 10kHz
for V_B	0.9V
v_o	5V pk-pk



Circuit description

The non-inverting input has a diode-connected transistor as part of a current-mirror. For a given feedback resistor to the inverting input, the current flowing in the non-inverting input gives a proportional output voltage. The non-linearity of the input impedance leads to output waveform distortion if any low-resistance parallel path is used to attenuate the signal. If the path consists of a suitably-biased silicon diode then its non-linearity is comparable with that of the input stage and the input signal division between the two paths has little variation with signal amplitude, i.e. little distortion results. This remains true while the signal current is well below the bias level.

As the direct current in the diode is increased, the corresponding fall in slope-resistance by-passes more signal current reducing the gain. Resistor R_4 provides sufficient bias current to set the output potential to a minimum of $V_s/3$. This applies when the bias voltage is low with the direct current in R_3 as well as the a.c. signal current via R_1 are both shunted away through R_2, D_2. The gain is virtually zero in this condition. As V_B approaches one diode voltage, the direct currents in D_1, D_2 and the amplifier input become comparable. The slope resistances are also comparable and the input current divides equally between the amplifier and D_2. For any further increase in V_B the signal current flows on through D_1 to the amplifier with negligible attenuation by D_2. At this extreme the direct current in R_3 contributes to the amplifier bias and the output d.c. level rises to $2V_s/3$. The bias range from 0 to 1V may be raised to any higher level by adding a potential divider.

Component changes

R_1 Sets input impedance 1k to 1MΩ.

R_2 Not critical but $\ll R_1$.

R_3, R_4 Normally equal, setting limits to output quiescent voltage. $R_3 = R_4 = 3R_5$ for output levels ranging from $V_s/3$ to $2V_s/3$.

R_5 Ratio R_5/R_1 sets maximum value of voltage gain.

C_1 Not critical, but reactance $\ll R_1$ at lowest signal frequency.

D_1, D_2 Small signal silicon diodes.

V_S Whole voltage range of amplifier, 4 to 36V.

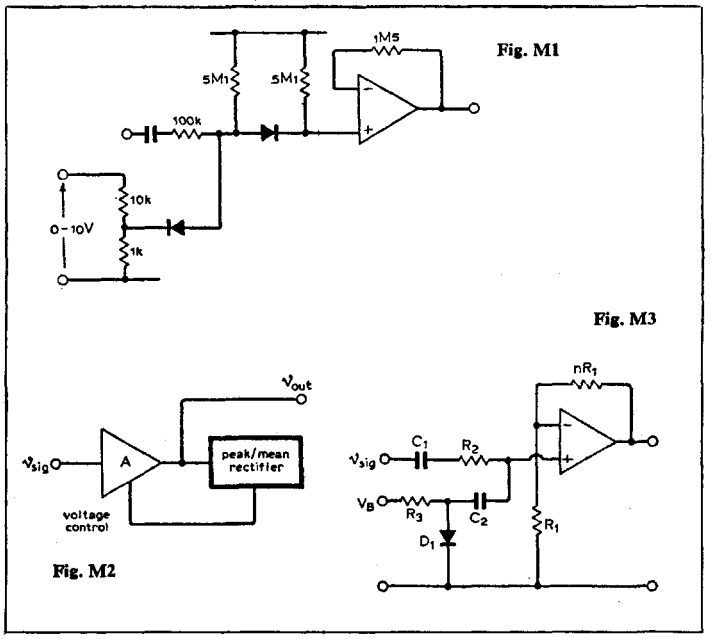
V_B Centre of gain-control region occurs for 0.6V but this is temperature dependent.

Circuit variations

- In some applications it may be more convenient to make the control voltage compatible with the normal output of other amplifiers. The potential divider raises the range of bias voltages to 0 to 10V. The component values, Fig. M1, give comparable gain figures at much higher impedance levels (taken from manufacturers application notes).
- Automatic control of output voltage against input signal variations (a.g.c.) is possible by detecting the output amplitude and feeding a smoothed control signal back to the amplifier bias input. For best control the rectified output can be compared against a direct reference voltage with the amplified difference being fed back, Fig. M2.
- A simpler circuit, Fig. M3, uses a.c. coupling between the diode being controlled by R_3 and the amplifier non-inverting input. An alternative d.c. biasing technique sets the output voltage to $(n + 1)V_{be}$ provided the value of R_1 is sufficiently low that the current in it ($\approx 0.6V/R_1$) is $\gg$30nA, the typical input current of the amplifier. Increasing the bias voltage lowers the slope resistance of D_1, diverting signal current from the amplifier input and reducing the gain (maximum gain $\approx nR_1/R_2$). The gain cannot be reduced to zero with this circuit.

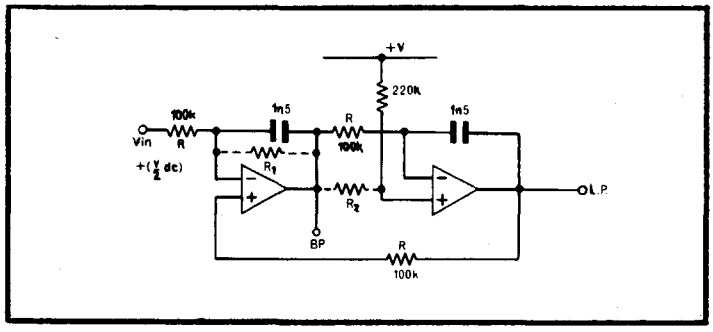
Cross references

Set 16, cards 2, 3.



wireless world circard Set 16: c.d.as—signal processing Up-dat

1. Of the standard op-amp active filters, the two-integrator loop is one of the best known—though under a variety of names including "bi-quad" and "state-space". The overall loop gain at d.c. has to be inverting to prevent d.c. latchup. This is usually achieved by inserting a unity-gain inverting stage in the loop. An alternative is to apply the feedback to the non-inverting input of one of the amplifiers while leaving the integrating capacitor at the inverting input. Using op-lamps, a high Q is only attainable using a wide



spread of component values (see ref. 2). With a c.d.a. or Norton amplifier such as the LM3900 or MC3401, the natural Q of the system shown is in excess of 200. Lower, controlled values can be obtained by adding the damping resistor R_1, when the Q will be given by R_1/R to a reasonable approximation for Q in the range of 2 to 20. The Q can be increased by removing R_1 and adding R_2, even with high values of R_2 sinusoidal oscillations may occur. Both bandpass and low-pass outputs are obtained from the filter (quadrature outputs when oscillating).

References

1. Croskey, C. State variable filter uses only two op-amps, *Electronics*, 1974, Mar. 21, pp. 98/9.
2. Attikiouzel, J. Low-cost active low-pass and band-pass network, *Circuit Theory and Applications*, 1974, vol. 1.

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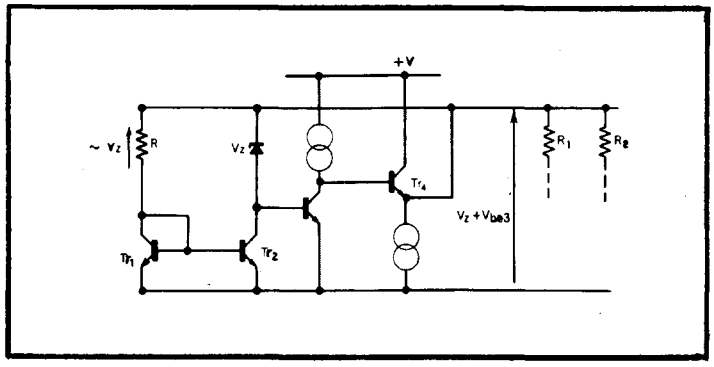
2. The technique shown provides (i) a zener diode with an operating current stabilized by the zener voltage (ii) an output voltage controlled by the zener but having a temperature drift corresponding to a single V_{be} if the zener is a low-drift type.
The p.d. across the resistor R must be V_z to a good accuracy if the V_{be}s of Tr_1, Tr_3 are well matched. The lower the current in R the more accurately this holds but in any case the current variation is very small (corresponding to a few tens



of millivolts in perhaps 5 to 10V). Thus V_z is well stabilized and the output voltage is $V_z + V_{be3}$. If this voltage is to be used to define the currents at other points in the system, for example the inputs of other comparators, then it has a drift which is small and of the right magnitude and sense to stabilize those currents against variations in the V_{be}s of the inputs. For the output voltage to be temperature-independent, the zener would need a temperature coefficient of voltage of around +2.5mV/deg C.

Reference

Fergus, R. W. Use current-mode op-amps in reference circuits, *EDN*, 1974, June 20, pp. 80/1.

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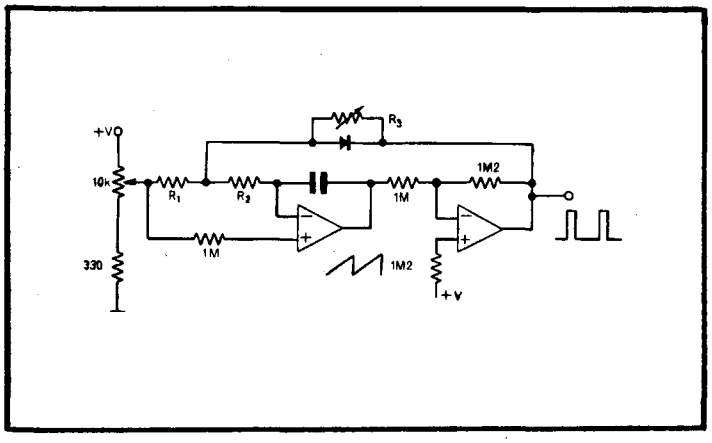
3. This modification to the v.c.o. described in set 17, number 3 was proposed a reader*, and converts the circuit into a sawtooth generator, accompanied by a pulse train with narrow pulse widths. The input potentiometer varies the frequency with the values of R_1, R_2 and R_3 controlling the waveform. If $R_1 + R_2$ are replaced by a 470kΩ potentiometer with R_1 set to 340kΩ and R_3 to 7kΩ then the pulse width is lms and



the frequency range is 0 to 140Hz. Pulse width can be increased to 4ms with a frequency range of 6 to 86Hz with R_1 22kΩ, R_3 4kΩ. In each case the supply voltage was about 16.5V, but in common with most versions of this circuit the voltage is not critical.

Reference

*Saunders, L. R. Voltage-controlled pulse generator, Private communication, Auckland, N.Z., Sept. 6, 1975.

wireless world circard

Set 17: c.d.as — signal generation

The following article discusses differences between c.d.as and op-amps as far as cut-off frequency and slew rate are concerned. It also gives a circuit that simulates a c.d.a. using a five-transistor i.c., such as the CA3046, so that the effects of different operating currents and compensation can be investigated.
That it is the current into c.d.as that is of prime concern is reinforced in the article and best results with c.d.as obtain from networks requiring a low impedance load—the inverting input—with shunt feedback. An example is given on card 2 which shows an RC oscillator followed by a level sensing circuit to give a distortion of 0.1%.
The circuits on the cards show that some functions are achieved much more simply with c.d.as than previously: rectangular and triangular-wave generators are shown on cards 1, 3 & 10. The Schmitt trigger circuit (card 6) is also very simple, provided precise switching levels are not required. Constant-voltage circuits are easily produced by using a Zener diode or planar transistor in a negative feedback loop (card 4), while constant-current circuits require balancing of positive and negative feedback to give very high output impedance (card 5).

Current-differencing amplifiers

signal generation

The simple model of the current-differencing amplifier discussed in the previous article (August issue) is sufficient to explain the principles—but not enough to satisfy the customer placing his pennies on the counter. A fuller circuit is shown in Fig. 1 representing the relevant sections of one of these amplifiers, in this case the LM3900, though other manufacturers produce similar circuits. Transistors $Tr_{9,\ 10}$ constitute the input current mirror coupling a current into the external feedback network that is the difference between the two input currents. Transistor Tr_8 is the only stage contributing voltage gain and its collector is the highest impedance point in the system—the most convenient point to place the compensation capacitor C since a small capacitance is sufficient to bring the cut-off frequency down to the required level. The single stage of voltage gain is buffered by $Tr_{4,\ 3}$ to give a reasonably low output impedance with a current source capability of tens of milliamps.

The open-loop voltage gain is very much less than is available from standard op-amps, but at 60 to 70dB (1,000 to 3,000) is ample for most applications. The reduced gain allows the open-loop cut-off frequency to be increased to about 1kHz (c.f. the value of around 10Hz for 741 op-amp) without instability occurring at high frequencies when 100% negative feedback is applied (Fig. 2). As a result the open-loop gain is 10dB greater for these current-differencing amplifiers from 1kHz to 1MHz.

This is a fair statement for small-signal applications, but the slewing characteristics of the amplifiers are quite different. In the 741 and similar amplifiers the maximum current available for the capacitor is comparable for both positive and negative swings, bringing a slew-rate of about 0.5V/μs in both directions. In the current differencing amplifier described here, the capacitor C (Fig. 1) can be discharged rapidly by Tr_8 if the latter is over-driven, and the negative slew-rate is about 20V/μs. The charging path for the capacitor is via Tr_4 base and the slew rate is limited by the low base current to about 0.5V/μs, giving asymmetry to the rise and fall times of a pulsed output (Fig. 3). The resulting large-signal response when used as an amplifier is limited to around 10kHz by this positive slew-rate.

This is but the first generation of current-differencing amplifiers, designed for simplicity and economy. It is to be expected that circuits will gradually appear offering improvements in this and other directions. With the example of operational amplifiers as a guide, we can hope to see multi-megahertz current-differencing amplifiers before long. This could be achieved by removing or reducing the compensation capacitance, provided the circuit was not then used with heavy feedback.

It is possible to experiment with a similar circuit to see the general effects of operating at different currents and with different degrees of compensation. The circuit is shown in Fig. 4 and is based on one of the low-cost five-transistor packages such as CA3086, CA3046 etc. These have gain-bandwidths in excess of 500MHz demanding care in construction if good results are to be obtained. Transistors Tr_1, Tr_2 comprise the current mirror, Tr_3 is the voltage amplifier and Tr_4 the emitter follower. Transistor Tr_5 acts as a constant-current load to the emitter follower though the slope resistance is less than that achieved by current mirrors. Bootstrapping the collector

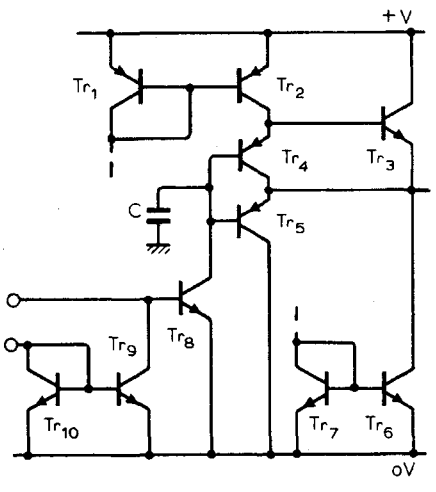


Fig. 1. Part of the LM 3900 current-differencing amplifier, to which the current mirror Tr_9, Tr_{10} couples a current into an external feedback circuit, via emitter followers, that is the difference between the two input currents.

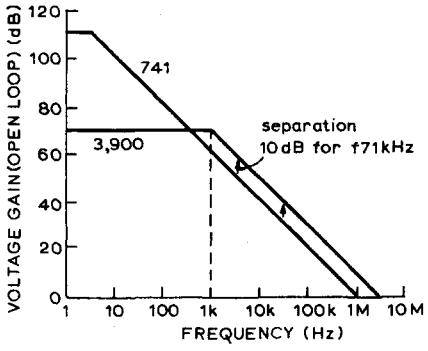


Fig. 2. Reduced gain of c.d.a. relative to 741 op-amp allows increased open-loop cut-off frequency. Open-loop gain is about 10dB greater from 1k to 1MHz.

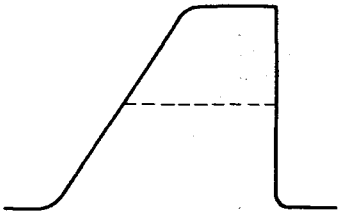


Fig. 3. Positive slew-rate is limited by the low base current in Tr_4 (Fig. 1) to about 0.5V/μs, giving asymmetry to the rise and fall time of a pulsed output.

load of Tr_3 increases the voltage gain giving some of the effects provided by the constant-current stage in the commercial amplifier. This circuit is in no sense a competitor for the complete i.c. but may help in understanding the techniques and limitations. (Possible values are R_1, R_2 47kΩ, R_3 470kΩ, C 10μF, with a supply of +10V.)

The control of direct voltages and currents is readily achieved with amplifiers of this class, with the simplest circuits requiring only the addition of a zener diode. Care has to be exercised if high stability is required since, as shown in Fig. 5, the output voltage depends on the direct voltage between the inverting input and ground. This is approximately 0.55V, changing with temperature by about −2.2mV/degC. As drawn, the zener current would be restricted to the amplifier input current of 30nA and an additional resistor between inverting input and ground would be needed to bring the current up to the level appropriate to the zener.

Sine-wave generation is by passive resonant or phase-shift networks, with the one change; that it is the current into the amplifier that is of concern. While conventional passive networks such as the phase-shift network of Fig. 6 can be adapted by using a suitably large resistance R' to force a current into the amplifier without loading the network, better results follow from designing alternative networks requiring a low-impedance load (i.e. the virtual-earth of the amplifier inverting input when used with shunt feedback).

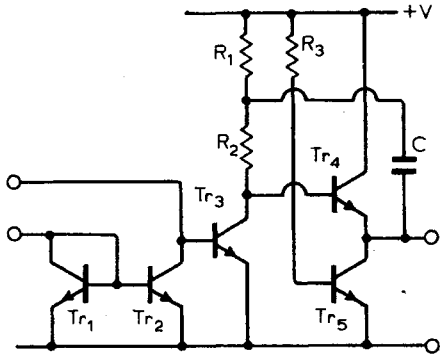


Fig. 4. By making a c.d.a. from a five-transistor i.c. the effect of altering the compensation capacitor can be investigated, gain-bandwidth products of 500MHz or more being possible.

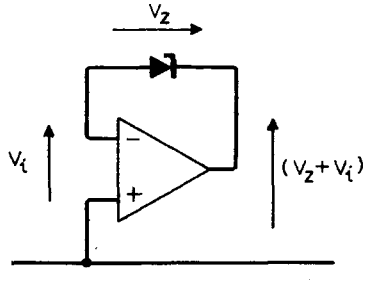


Fig. 5. Stability of voltage level in c.d.as can be improved by simple addition of a zener diode.

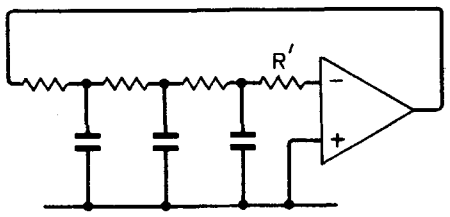


Fig. 6. Phase-shift network can be adapted for use with a c.d.a. by using a large resistance R' to force a current into the amplifier.

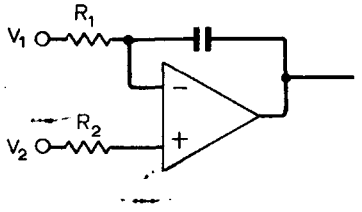


Fig. 7. Waveforms can be generated by subjecting a capacitor to alternate positive and negative current flows. Square/triangle generators can be simplified by fixing V_1 or V_2 and switching the other by a circuit that monitors integrator output.

A wide variety of waveforms can be generated by using the voltage across a capacitor subjected to alternate positive and negative current flows. Where the net charging current depends on the current-difference at the two inputs, novel circuits result. In particular, simplification of square-triangle generators is achieved by keeping V_1 or V_2 (Fig. 7) constant while switching the other from some positive value to zero under the control of a level-sensing circuit that monitors the output of the integrator.

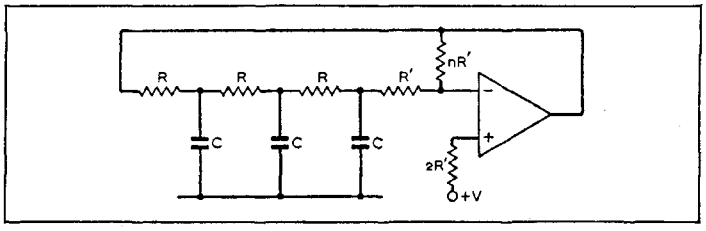
With suitable scaling of the voltages and resistors the polarity of the net current is reversed using only a single diode/transistor/f.e.t., while the magnitude of that current is determined by an external control voltage. The resulting voltage-controlled oscillator is markedly simpler than is normally possible. If one or more of the voltages is replaced by a pulsed source, then staircase/ramp waveforms are produced depending on the magnitude, polarity and timing of the pulses. In each of these circuits, the use of a second amplifier can cancel the input current of the integrator amplifier to a first order, reducing the drift to a very small level.

There is no one-to-one correspondence between the circuits designed around operational and current-differencing amplifiers. It will take considerable time and effort to make sure that the advantages of the latter are exploited. The effort will not be wasted.

Generators

Circuit description—1

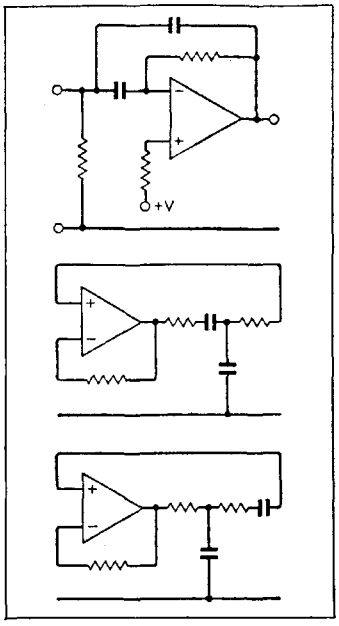
Four types of generator are considered here. They can be summarized as sine, relaxation, square/triangle and d.c. The last of these, the group of circuits normally called voltage/current regulators, can be considered as generators of direct voltage or current. Alternatively, they can be dealt with as d.c. amplifiers with input signals provided by constant voltage/current reference elements, e.g. Zener diodes (see set 16). For cisoidal oscillators the basic requirement is a passive network giving a phase-shift of 0 or π at a single frequency. This may or may not be accompanied by a maximum in the magnitude of the transfer

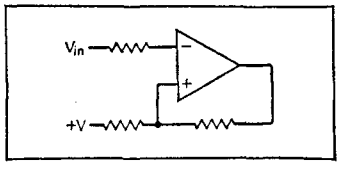


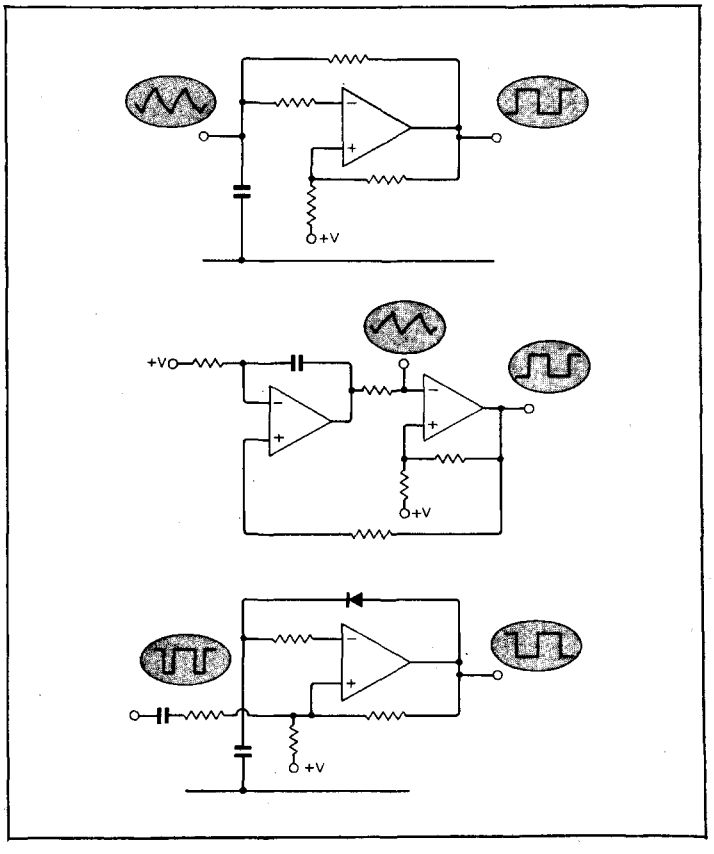
function, but in either case it dictates to which input the feedback should be returned. The circuit oscillates at the frequency for which the loop has zero phase-shift and amplifier phase-shifts cause errors at high frequencies. The classic phase-shift oscillator can be used as above, with the amplifier providing more than enough gain. Negative feedback from output to inverting input sets the amplifier gain to overcome the losses in the passive network. Largest signal at amplifier output, least distortion across last capacitor. Make $R' \gg R$ to minimize loading of network. Any band-pass filter may be inserted into the feedback loop of a system, allowing the overall loop gain to reach the critical condition only at the filter centre frequency. To adapt the more usual Wien networks to current differencing amplifiers, it is sufficient to take any such network whose output has a grounded resistor, and use the current in the resistor as a feedback—the amplifier having a low enough input resistance to act as a virtual earth. No mechanism is shown for amplitude control, but the precisely defined input non-linearities allow for simple solutions as shown later.

Circuit description—2

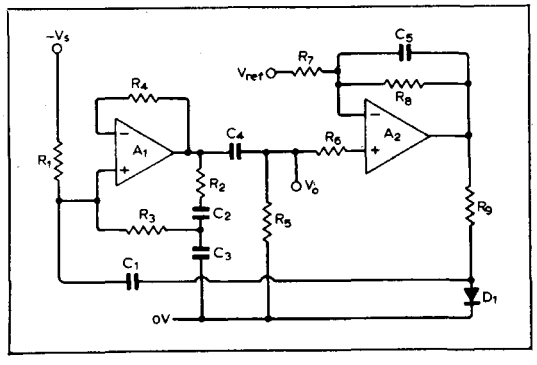
The common element to many non-sinusoidal waveform generators is a Schmitt trigger, implemented by an amplifier with positive feedback as shown below. In this amplifier the output changes state rapidly as the input passes through a given voltage level, reverting to its original state when the input returns to a different level. The difference between the switching levels is the hysteresis, and by using the circuit to monitor the voltage across a capacitor the charging current can have its direction reversed at each transition of the voltage through a switching level. The simplest arrangement is at top right where a single amplifier acts both as Schmitt trigger and as source of charging/discharging current. The current varies during the cycle according to the usual RC relationships since the output voltage has a constant value for each switched state. If the capacitor forms part of an integrator then the charging current has one of two fixed values, because the virtual earth action prevents the charging voltage across the capacitor from modifying the current. A further modification of this circuit uses an additional diode or transistor to reverse the net current flow to the amplifier by interrupting the current to either the inverting or non-inverting input. Selection of suitable resistors gives a net-charging current that reverses its direction while remaining of equal magnitude and being controlled by an external direct voltage i.e. a voltage controlled oscillator results. If the first circuit is adapted to have one stable state then it can be triggered by an external pulse into the unstable state where it remains until the capacitor has completed its charge (or discharge) sequence. The resulting monostable circuit may be edge- or level-triggered.







RC oscillators

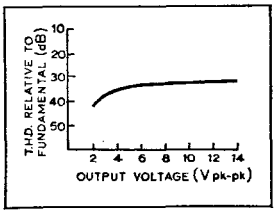


Typical performance
A_1, A_2: ½ LM3900
Supply: +20V
R_1: 220kΩ
R_2, R_3: 33kΩ
R_4: 120kΩ
R_5: 100kΩ
R_6: 1.8MΩ
R_7: 2.2MΩ
R_8: 5.6MΩ
R_9: 15kΩ
C_1: 0.68μF
C_2, C_3: 10μF
C_4: 0.1μF
C_5: 1μF

D_1: 1N914
f : 500Hz

$$f \approx \frac{1}{2\pi(R_2R_3C_2C_3)^{\frac{1}{2}}}$$

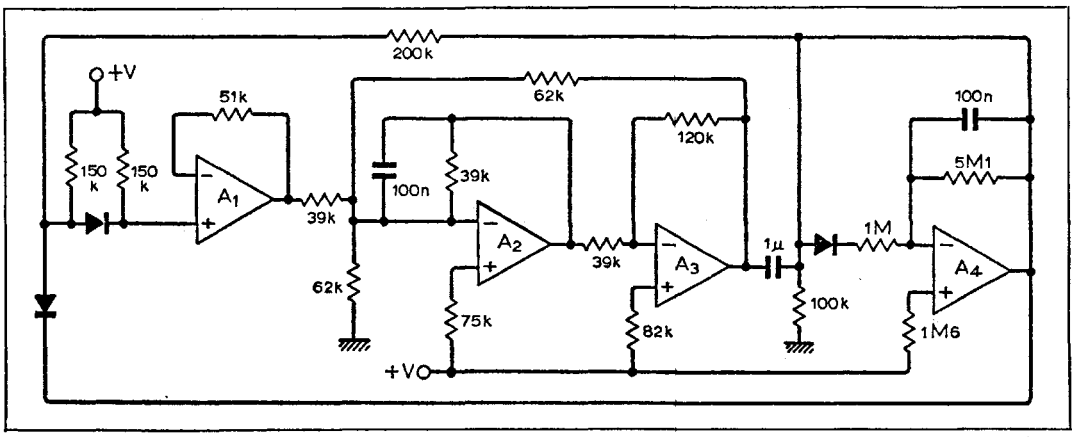
v_o: 7V pk-pk ± 0.2dB for V_s 12 to 20V.



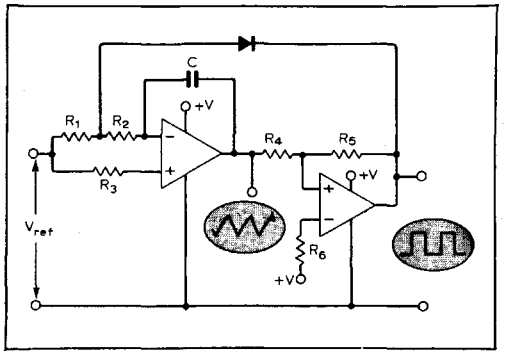
Circuit description
The circuit has two distinct sections. Amplifier A_1 together with R_1 to R_4 and C_2, C_3 constitutes a complete RC oscillator, in which the positive feedback via R_3 exceeds the negative feedback via R_4. Choosing $R_1 \approx 2R_4$, the amplifier output is biased to $\approx V_s/2$ since the d.c. feedback ensures almost equal currents in R_1, R_4. The second amplifier amplifies and filters the output of A_1 after a.c. coupling via C_4, R_5 and half-wave rectification via the non-inverting input of A_2. The addition of a reference voltage acting via R_7 causes the d.c. output of A_2 to vary the bias current in D_1 in such a way that it diverts a varying proportion of the a.c. feedback from the non-inverting input of A_1. Allowing for the time constants of the loop, the output of A_2 will vary until the half-wave rectified sine-wave output of A_2 is comparable with V_{ref}. The non-linearity of D_1 V/I characteristics does not introduce serious distortion, since it matches that of the input characteristics of A_1. Because the amplifiers are current-differencing units, the conventional Wien bridge has been rearranged, i.e. instead of grounding R_3 and using the p.d. across it as the frequency-dependent feedback, the current through it is fed back, taking the amplifier input as a virtual-earth. The output voltage of A_1 has a d.c. term of $\approx V_s/2$ and the superposed a.c. may have a peak-peak value of up to 80% of the supply voltage before the onset of clipping. The relatively low open-loop gain of the amplifier does not allow very low distortion levels but the ability to control the amplitude of oscillation by an external direct voltage, while using only two out of the four amplifiers within the i.c. is very useful.

Component changes
R_1, R_4: Ratio ≈ 2:1 to bias A_1 output $V_s/2$, R_4 is chosen to provide less negative feedback than the positive feedback via R_2, R_3, C_2, C_3 i.e. $R_4 > 3R_2$.
R_2, R_3: $R_2 = R_3$. Together with C_2, C_3 defines the frequency of oscillation. R_2 10k to 1MΩ.
C_2, C_3: $C_2 = C_3$. 1000pF to 10μF. Large R values can be used with small C values for economy, but layout/screening need to be watched to avoid hum.
C_4: Not critical. 0.01μ to 100μF. Higher values only required for lower load resistances. Circuit output current should not exceed 1mA for lowest distortion.
C_1: Must have low reactance at signal frequencies—at least 0.5μF for 1kHz.
R_6, R_7, R_8, R_9: Control mean current in and hence slope resistance of D_1. High values to minimize required value of C_5. Time constant period of waveform.
V_{ref}: 0 to 4V. Controls output voltage; R_4 can be varied to increase or decrease the control effect required via D_1.
V_s: Oscillations sustained at lower supply voltages but amplitude control difficult.

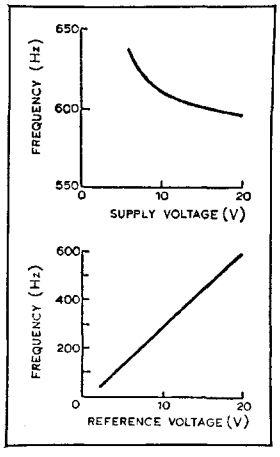
Circuit variations
● The principle of the circuit is that of an RC oscillator using A_1 and a modified Wien-network, followed by a signal level sensing circuit (A_2) that modifies the loop-gain of the oscillator feedback loop. Any other RC oscillator can be substituted for A_1 circuit, but amplitude control via a biased diode is optimum, as the diode and amplifier input non-linearities cancel.
A peak-sensing circuit is an alternative, and a diode peak detector can replace A_2 with power control of amplitude.
● A recently described oscillator uses all four amplifiers and achieves the very low distortion of 0.1%. Amplifier A_2 is a band-pass filter with A_3 setting the Q. Feedback via the 100-kΩ resistance sustains oscillations at the filter centre-frequency. Amplifier A_4 senses the mean-rectified output and controls the amount of feedback via the attenuation due to the diodes so as to keep the output as a well-defined function of the reference voltage. Resistor values are optimized to stabilize the output against temperature variation.



Voltage-controlled oscillators



Typical performance
IC: ½ LM3900
Supply: 10V
R_1: 220kΩ
R_2: 270kΩ
R_3, R_4: 1MΩ
R_5, R_6: 1.2MΩ
C_1: 1nF
Square-wave output: 9V pk-pk
Triangular wave: 7.5V pk-pk
Frequency: 610Hz

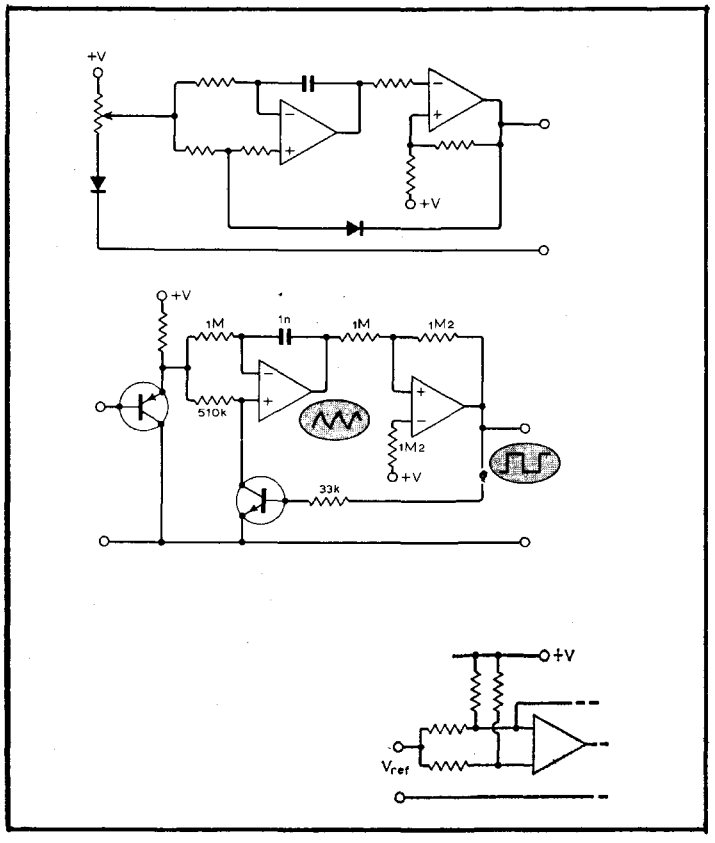


Circuit description
A basic method of generating square/triangle waves is to interconnect an integrator and a Schmitt trigger circuit. With correct phasing the integrator output changes linearly with time between the threshold voltages of the Schmitt, causing the output to reverse and with it the direction of the integrator output slope. To bring the frequency under the control of an external voltage the switched output is used to reverse the net current into the integrator, but leaving the magnitude defined by the control voltage. A current differencing amplifier is particularly suited to this technique, since the net charging current is the difference between the two input currents. If these are set in the ratio 2:1 and the larger current is switched off, the net current changes sign, remaining of equal magnitude i.e. a triangular wave results at the integrator output with peak-to-peak voltage equal to the hysteresis of the Schmitt trigger circuit.
Consider the Schmitt output positive; the diode is reverse-biased and with $R_1 + R_2 = R_3/2$, the net integrator input current is negative. Integrator output ramps negatively until the lower threshold voltage of the Schmitt is reached. Output of the Schmitt falls almost to zero and the diode conducts by passing the current in R_1 to ground through the output of the Schmitt circuit. (A residual current flows in R_2 since the output of the Schmitt is typically a 100mV but the current is small compared with the normal charging current.) The net charging current is now positive and the integrator output ramps positively until the cycle is completed on chargeover at the upper threshold level. The rate of charging is proportional to V_{ref} which may be derived from a potentiometer across the supply or from an external source with $f \propto V_{ref}$ to a good approximation.

Component changes
R_1, R_2, R_3: For equal positive and negative slopes to the triangular wave (and hence unity mark-space ratio for the square wave). $R_1 + R_2 = R_3/2$. To minimize loading on source these resistors may range from 100k to 10MΩ. $R_1 \approx R_2$ but may be different to use preferred values while meeting above conditions.
C: sets frequency of oscillation and $f \propto 1/C$ except at high frequencies where finite rise and fall times limit the response. Typically C is 1n to 10μF.
R_4, R_5, R_6: control upper and lower threshold voltages and have peak-peak value of triangular wave. For $R_5 = R_6$ and $R_4 = kR_5$, the hysteresis is $\approx k$ (square-wave output). Reducing the hysteresis increases the frequency of oscillation, other components being equal. Amplifier slew-rate of 0.5V/μs makes it difficult to obtain outputs above 10kHz.
D: Not critical. Any general-purpose silicon diode.
V_s: +4 to +30V.
V_{ref}: 0 to 30V (higher if R_1 to R_3 increased).

Circuit variations
● Using an inverting Schmitt, but with the feedback shunting the current from the non-inverting input of the integrator leaves the phasing correct for sustained oscillations. Diode compensation can be added to this and the previous circuit such that $f \to 0$ as the input pot. is set to zero.

● Improved performance at high frequencies is possible using a transistor rather than a diode to direct the integrator input current; inversion provided by the transistor requires inversion of one or other of the other circuits. Because the transistor conducts for a rise in the Schmitt output of little more than one V_{be}, the rise time of the Schmitt no longer presents such a serious limitation to the frequency at which oscillation can be sustained.
● Adding bias resistors to +V sets a minimum value to the frequency of oscillation for $V_{ref} = 0$ i.e. the frequency can be controlled over any prescribed range. (Bottom)



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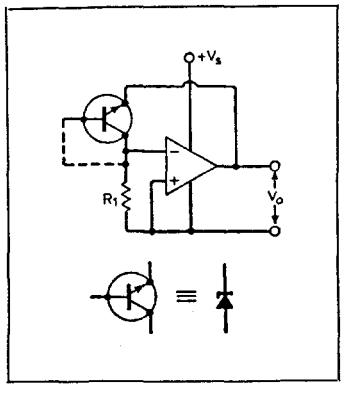
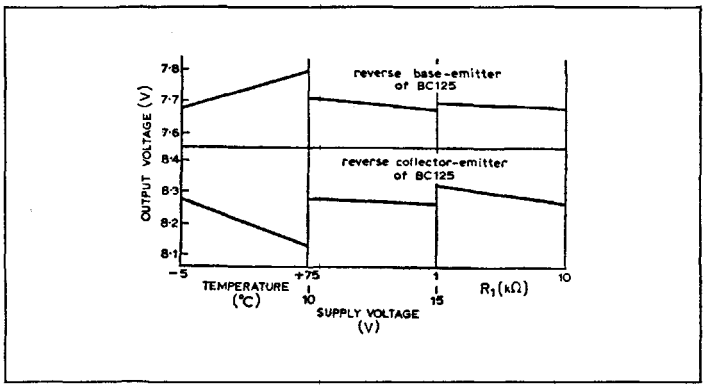
Voltage regulators



Typical performance
Supply: +15V
IC: ¼ LM3900
Tr1: BC125*
R_1: 10kΩ
V_o: 7.7V
R_1: 2kΩ
ΔV_o: +15mV
(for ΔV_s = —5V)
+25mV (for ΔT= +25 deg C)
*Use of reverse base-emitter junction gives good low-current breakdown. Using reverse collector-emitter raises voltage by 0.6V, changes drift by about −2mV/deg C.



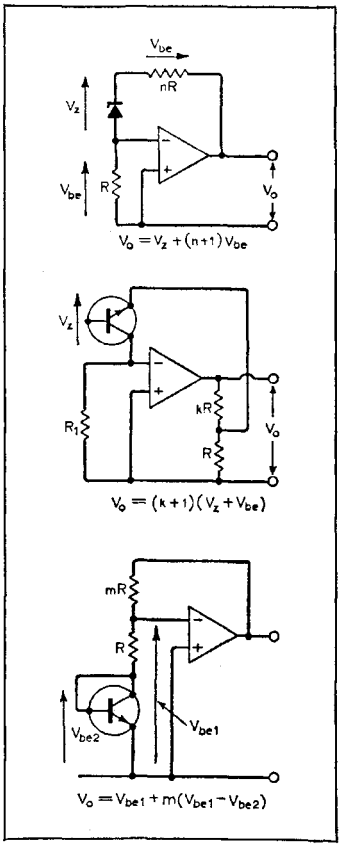
Circuit description
When negative feedback is applied around a current-differencing amplifier such as the LM3900, the inverting input terminal remains at 0.6V at 0 °C falling to nearly 0.4V at 75 °C. In the voltage regulator shown the voltage across R_1 is defined by these values, fixing the current in Tr_1 which acts as a Zener diode. Amplifier input current is very small (≈ 30nA) allowing currents between 1μA and 1mA to be adequately defined. Output voltage is the sum of the input V_{be} and the Zener voltage. Two sources of variation exist:
—direct variation in input voltage (V_{be}) as above of about −2.5mV/deg C together with a fall of 2 to 3mV for each 1V increase in the supply.
—corresponding variation in Zener voltage caused by the resulting current variation together with its own temperature coefficient.
If a Zener diode is available with a positive temperature drift cancellation between that drift and the input drift is possible, though complicated by the current variations. The use of a small-signal planar transistor with V_{eb} breakdown of about 7V gives partial cancellation while using the V_{ec} breakdown adds about 0.6V because of the forward biased base-collector diode. The additional negative drift over-compensates, for the particular device tested, but the method allows good cancellation. Conventional Zener diodes would be preferred where a quick range of voltages is required or close tolerance (but see circuit modifications).

Component changes
Tr_1: Any Zener diode may be used in principle since the output current is limited low-current operation is an advantage, and any planar transistor may be used as reverse base-emitter breakdown typically lies between 6 and 12V, being well-defined for a particular transistor type.
R_1: defines diode current as V_{be}/R_1 where V_{be} is that of the i.c. input transistor (≈ 550mV at room temperature, −2.5mV/deg C). Select for Zener current of say 100μA to 2mA depending on type, down to 1μA for planar diode/transistor.
V_s: 4 to 36V (down to 3V in some cases).
V_o: up to 36V. Limited by available diodes but see circuit modifications.
I_o: 0 to 10mA. May be boosted by adding emitter follower at output of amplifier (*inside* feedback loop).

Circuit modifications
● Additional temperature compensation is introduced by adding resistance in series with the Zener diode. Currents in the diode and resistors are almost equal since the amplifier input is small (≈ 30nA). Hence $V_o = V_z + V_{be} + nV_{be}$. Each equivalent V_{be} increases the output by ≈ 0.55V, adding a temperature drift term of −2.5mV/deg C. (Top circuit.)

● To increase the output voltage Zener/transistor (e.g. selected for its temperature dependence) the diode is tapped onto a portion of the output voltage. The potential divider should not be significantly loaded, nor should it constitute a significant load on the output so a low current breakdown device is preferred. With a chain current of 1mA the diode current should not exceed 10μA for good accuracy. (Middle circuit.)

● Relying on the V_{be} alone to define output voltage gives too large a drift with temperature for most applications. Adding a germanium transistor as shown gives first-order temperature compensation particularly for m large and the difference in the V_{be} values is in the range 400 to 450mV. (Bottom circuit.) The three techniques suggested may be used in various combination as well as separately.

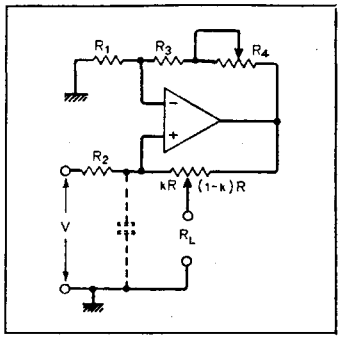


Cross references
Set 6, cards 1, 2, 7 & 10.

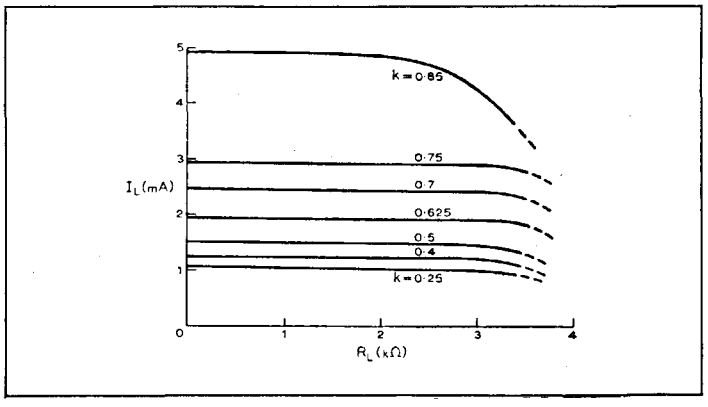
wireless world circard

Set 17: c.d.as—signal generation—

Constant-current circuits



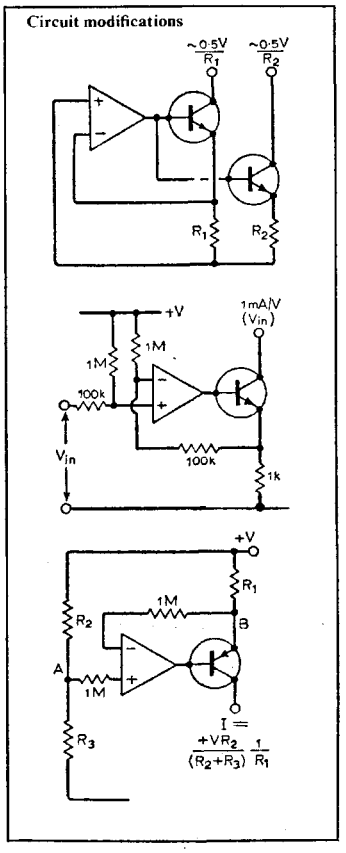
Typical performance
IC: ¼ LM3900
Supply: +15V
R_1, R_2: 10kΩ
R_3: 8.2kΩ
R_4: 2.2kΩ for particular circuit
R: 10kΩ
k: 0.5
V: 7.7V for I_L 1.5mA



Circuit description
Many circuits used with conventional operational amplifiers are adaptable for use with current differencing amplifiers. To provide a constant-current drive to a grounded load is difficult in both cases since each amplifier has its output referred to ground so that feedback can only be taken in shunt with the load, i.e. lowering the output impedance. If the load can float then the feedback may be taken across a grounded resistor in series with the load. An alternative technique combines negative and positive feedback in such a way that at some point in the network the output impedance tends to infinity. By injecting voltages/currents at other points in the system, a load connected between that particular point and ground will carry a current independent of the load resistance. As shown, R_4 is used to adjust the negative feedback such that for very high load resistances, the negative and positive feedback are almost in balance. In the ideal case, this is achieved for $(R_3 + R_4)/R_1 = R/R_2$.
Current in the load may then be varied in one of three ways, each of which has minimal effect on the output resistance: variation of the input voltage V; insertion of an alternative/additional voltage in series with R_1; variation in the tapping point of the resistor R. The last method can be used to obtain a 5:1 spread in sensitivity while retaining a high output resistance. Using a single polarity supply restricts the output to one polarity (+) but dual-polarity supplies would permit bipolar outputs for handling d.c. signals without the need for blocking capacitors.

Component changes
Vs: +4 to +36V. Because of losses in feedback-defining resistors load voltage swing is always less than amplifier capability.
R_1, R_2: 10kΩ is near lower end of working range, with amplifier normally operating with input resistor of 100kΩ upwards. However, values required where current of several mA required in load.
R_3, R_4: If high impedance is sufficient and it is not required to trim for output impedance $\rightarrow \infty$, replace by fixed resistance ($R_3 + R_4 = R$ for $R_1 = R_2$.
Negative output resistance if feedback resistance to inverting input is too large.
k: Can be varied from 0.2 to 0.9. At high values, relatively large currents obtainable but with some loss of accuracy.
V: Variable over range 2 to 10V. For input voltages too low, V_{be} errors at input prevent linearity of I_L against V.

Circuit modifications
● By adding transistors, the feedback may be taken from across one emitter resistor as would be the case for a voltage amplifier (top circuit.) The output is taken from the transistor collectors each or which carries a collector current almost equal to its emitter current if the transistors have high current gains.
In the simplest arrangement the current is defined by the amplifier internal V_{be} with a consequent temperature dependence to the currents (which may be set to any required ratios by varying R_1, R_2, etc.). Any of the techniques used in voltage regulators may be used to achieve better control over the voltage across R_1.
● A voltage-controlled current sink as shown forces the voltage across the 1kΩ resistor to match the input voltage giving an overall transconductance of 1mA/V. Bias provided by the 1MΩ resistors linearizes the characteristic at low V_{in}/I_L.

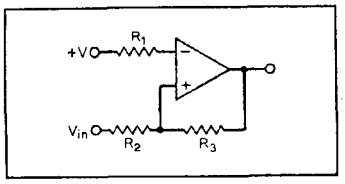


● A current source using this principle is possible but has some disadvantages. It is the voltage across R_1 that needs to be defined, but approximate equality of the p.ds across the 1MΩ resistors that is achieved. Where the voltage across R_1 is to be low (say 1V) to maximize load voltage, small unbalance in the input current sensitivities produce small voltage differences at A & B. These small errors then represent a large error in the small voltage across R_1 and hence in the load current. (Bottom circuit.)

Cross references
Set 6, cards 4 & 12.

wireless world circard

Schmitts & comparators



Typical performance
IC: ¼ LM3900
Supply: + 15V
R_1: 1MΩ
R_2: 2.2MΩ
R_3: 10MΩ

$$V_u = +V\left(\frac{R_1}{R_2}+\frac{R_1}{R_3}\right) + V_{be}\left(1-\frac{R_1}{R_2}-\frac{R_1}{R_3}\right)$$

$$V_l = +V\left(\frac{R_1}{R_2}\right) + V_{be}\left(1-\frac{R_1}{R_2}-\frac{R_1}{R_3}\right)$$

V_{be}: of input transistors assumed equal and ≈ 0.5V.
Hysteresis, $V_u - V_l = +V R_1/R_3$
Measured hysteresis: 1.51V.
Output rise-time: 30μs (corresponding to 0.5V/μs slew rate limitation for positive-going output)
Output full-time: 2μs

Circuit description
The input section of current-differencing amplifiers rely on the accuracy of matching of transistors in a current mirror to define the operating levels. It is not possible to obtain the precision of switching levels by such a method as can be achieved using a long-tailed pair and more conventional circuitry. Where a moderately wide hysteresis, say, 1V or greater, is acceptable and neither upper or lower thresholds need be defined to within a small percentage, Schmitt circuits can be simply constructed offering the other advantages of positive and rapid switching. The limited slew-rate of the amplifier makes it comparable in performance in this respect to op-amps such as the 741, but the internal compensation cannot be removed to allow speeds comparable to the uncompensated op-amps (301, 748, etc) let alone high-speed comparators. The main uses are likely to be as part of signal processing systems, alarm circuits, waveform generators, etc.

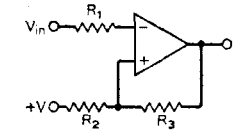
Switching takes place, assuming ideal current mirror action, when the current in R_1 equals the sum of the currents in R_2, R_3. In each case the amplifier internal V_{be} of about 0.5V has to be taken into account, effectively raising both upper and lower thresholds by somewhat less than 0.5V. To a first order approximation, hysteresis depends only on the resistor values, while the input resistance may be made >1MΩ.

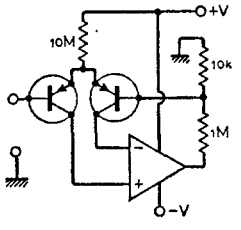
This is because the inverting stage input current of ≈ 30nA allows reasonable accuracy of switching levels even though the currents in the resistors are only a few microamperes. Increasing R_3 reduces the upper threshold without changing the lower one. Increasing R_2 reduces both thresholds by the same amount leaving the hysteresis unchanged. Increasing R_1 raises both threshold voltages proportionately, leaving the hysteresis in the same ratio to each as prior to the increase.

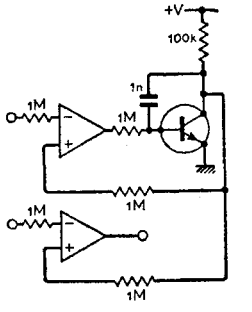
Component changes
Supply V: +4 to 36V. Usual range for given i.c.
R_1: 100k to 10MΩ. The lower value is particularly useful if voltage comparator action is required for voltages <1V. Each input is pre-biased to +V through 1M to 5MΩ resistors.
R_3: As above. If used as a comparator R_3 is absent, and comparison is possible between unequal voltages i.e. the output can be made to swing between its limits as V_{in} passes V_+/n if $R_2 = R_1/n$. Comparison of negative voltages are also possible provided bias network accommodates common mode currents. Since currents are being compared, the use of suitably large resistors allows comparison of very large positive or negative voltages, but with the limited accuracy implied by the current-mirror input.
R_2: 1M to 22MΩ. Sets hysteresis and would be absent for comparator action. Can generally be added to any comparator arrangement to introduce, for example, small amounts of hysteresis to prevent output jitter due to noise.

Circuit modifications
- The position of the input and reference voltages (+V was used in the circuit overleaf) may be interchanged to give a non-inverting Schmitt. The availability of inverting and non-inverting Schmitts is of importance in the design of such circuits as wave-form generators. The thresholds and hysteresis are approximately: $V_u = +V R_2/R_1$, $V_l = +V\left(\frac{R_2}{R_1}-\frac{R_2}{R_3}\right)$ ∴ hysteresis $= +V R_2/R_3$.
- If a p-n-p long-tailed pair is added at the input the resulting amplifier may be used as a comparator or as a Schmitt (as shown). The input impedance is extremely high if high-gain low current transistors are available, and any degree of matching for the input transistors, may be chosen for high precision. It is necessary to clip the output voltage swing more precisely (with a resistor-Zener combination for example) if the hysteresis is to be equally precise.
- If two amplifiers are used then the matching is that between corresponding inputs which can be better than between + and — inputs of a single amplifier. One amplifier plus the output transistor has overall negative feedback (transistor is an inverter) and the equal current forced into the two non-inverting inputs forces the transition point in the second amplifier output to occur for equal currents at the two inverting inputs. Again comparison can be made between unequal voltages but more account has to be taken of the effects of the small input bias currents.

Circuit modifications

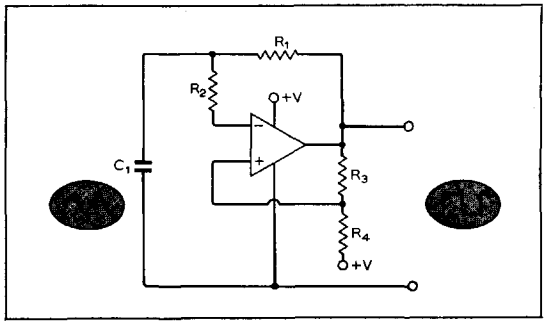




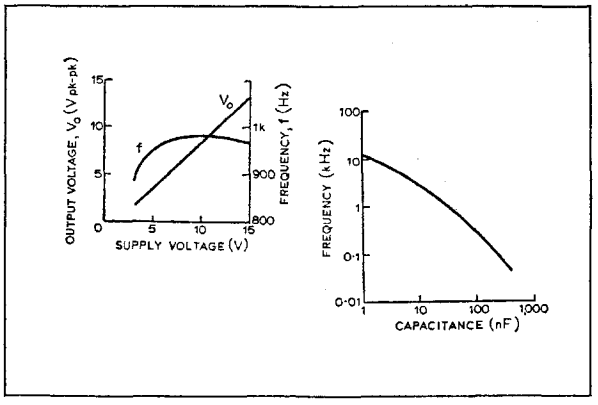


Cross references
Set 2, all cards.
Set 17, cards 3, 7, 8 & 9.

Astable multivibrators



Typical performance
IC: ¼ LM3900
Supply: +10V
R_1: 15kΩ
R_2: 1.8MΩ
R_3, R_4: 5.6MΩ
C: 47μF
f: 975Hz
v_o: 9V pk-pk
Rise time ≈ 20μs
Fall time ≈ 10μs

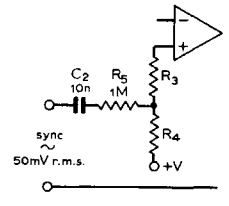


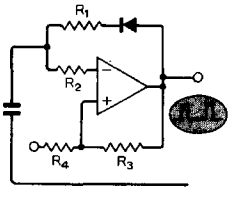
Circuit description
The amplifier together with resistors R_2, R_3, R_4 constitutes a Schmitt trigger. The output switches between the two extremes (≈ +100mV and ≈0.8V below V+). When the output is low C_1 is discharged through R_1 until the lower threshold of the Schmitt is reached. The output switches rapidly to its most positive value and the capacitor is charged positively. When the upper threshold is reached the Schmitt output is reversed and the cycle restarts. If R_2, R_3, R_4 are chosen to make the threshold voltages $V_+/3$ and $2V_+/3$ respectively then the voltage across the capacitor swings between these limits, while the output approximates to a square wave with almost unity mark-space ratio. For the highest accuracy a number of conditions must apply: The current in R_2 must be very low compared with the charging current through R_1; the output voltage swing should be as nearly as possible equal to the supply voltage; and the accuracy of the current-differencing action should be high (this places a restriction on the minimum currents in R_2, R_3, R_4). If these constraints are met then both the frequency and the mark-space ratio remain substantially constant over a wide range of supply voltages. Any increase in supply voltage produces proportional and hence self-cancelling increases in the magnitude and rate-of-change of voltage across the capacitor. The potential difference across the capacitor is uni-directional permitting the use of electrolytic capacitors for low frequency generation.

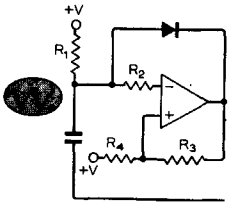
Component changes
R_2,R_3,R_4: These must be chosen jointly such that the firing points of the Schmitt trigger they constitute are $V_+/3$ and $2V_+/3$ (see circuit description). $R_3 = R_4 = 3R_2$ gives this condition. Make resistors as high as possible to avoid loading R_1, C_1 charging circuit i.e. $R_2 > 100R_1$. Typically R_2 1M to 10MΩ.
R_1: This sets oscillator frequency together with C. Too low a value loads the output. too low is loaded by R_2. Typically 4.7k to 100kΩ.
C: Max frequency of oscillation ≈ 20kHz corresponding to $C = 470$pF with $R_1 = 15$kΩ. Capacitor voltage always positive allowing use of electrolytic to give low frequencies.
R_L: Maximum output current ≈ 10mA giving minimum $R_L = 1$kΩ at $V_s = 10$V. Generally keep $R_L > 2.2$kΩ to allow output to swing close to supply.

Circuit modifications
● As with other astable multivibrators, this oscillator can be synchronized to an external waveform. Because the Schmitt action is achieved using high value resistors, the synchronizing input may also have a high input impedance, while locking can be achieved with 100mV. Locking to a sub-harmonic of an incoming signal is also possible, though for frequency division ratios in excess of 5:1 carry the risk of locking to the wrong sub-harmonic. (Top circuit.)
● Where relatively narrow pulses are required, the charge and discharge time constants should be as widely different as possible. The charging action is via R_1, a low resistance with a small current diverted into R_2. When the output is low the diode is non-conducting, and the small current in R_2 gives a long discharge time, i.e. a long space. (Middle circuit.)

Circuit modifications



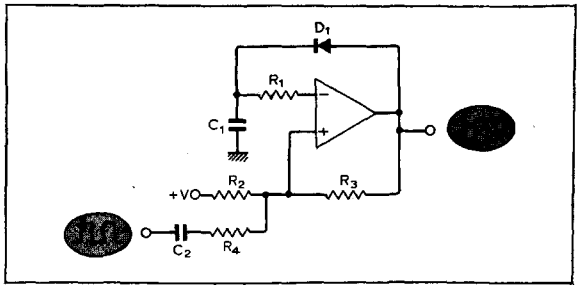




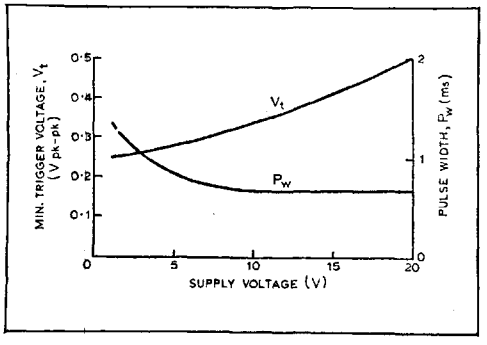
● Other forms of multivibrator may require more than one amplifier but the bottom circuit has some similarity of behaviour to the programmable uni-junction. The capacitor charges through R_1 until the upper threshold is reached. The output swings towards zero rapidly discharging the capacitor. The long mark has its duration controlled by the direct voltage applied to R_1 (+V may be replaced by an external control voltage giving a voltage controlled oscillator). The space is of short duration because of the relatively large discharge current.

Cross references
Set 3, cards 2, 4, 6 & 8.
Set 8, all cards.
Set 10, card 2.
Set 17, cards 3, 8 & 10.

Monostable multivibrators



Typical performance
Supply: +10V
R_1, R_3: 1MΩ
R_2: 10MΩ
R_4: 100kΩ
C_1: 220pF
C_2: 100pF
D_1: 1N4148
f: 100Hz
v_{in}: 0.5V pk-pk square-wave
Pulse-width: 0.66ms

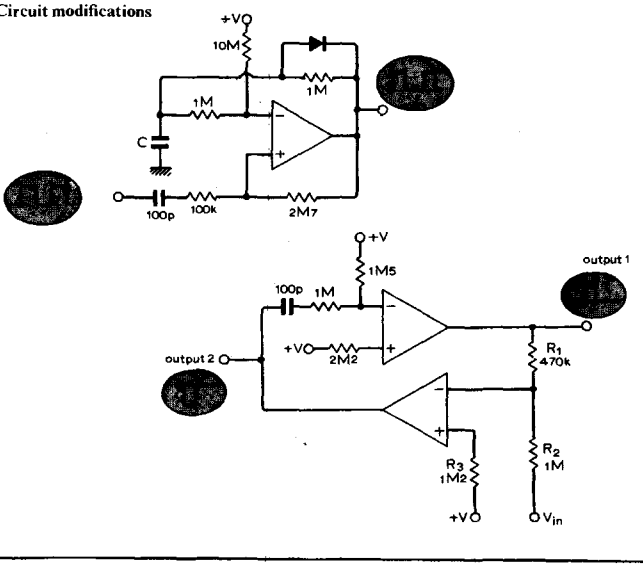


Circuit description
The circuit is closely related to the pulse generator modification of the astable circuit, and to the unijunction equivalent (card 7). The feedback network is designed so that the circuit normally latches into one particular state, with the output high. This is because in the low stage the diode inhibits current flow into the inverting input. Current in R_2 drives the output high initially and with the sum of the currents in R_2 and R_3 exceeding that in R_1. The first negative-going pulse drives the output temporarily low, the diode becoming reverse-biased. The capacitor discharges through R_1 with only R_2 contributing any current to the non-inverting input. Discharging continues until the voltage across the capacitor is down to a fraction of the supply given by R_1/R_2. At this point, the inverting input current comes into balance with that at the non-inverting input, the output begins to rise and the positive feedback causes the cycle to complete itself rapidly. The diode conducts, rapidly changing the capacitor to a volt or so below the positive supply voltage and the circuit is ready for the following trigger pulse. The positive-going slew-rate limit of 0.5V/μs limits the minimum pulse-width that can be defined with any accuracy. For a 20-V supply and a pulse of nominal length 100μs this slew rate would add up to 45% to its effective length.

Component changes
+V: +4 to +36V. Monostable action with increasing pulse-width and lowered output is possible to below 2V with some samples though outside specification.
C_1: Large values may be used (provided leakage resistance is 1MΩ) and with R_1 at 1MΩ time-delays of minutes are possible.
C_2: Used to differentiate input signal to provide short-duration positive transients. 47p to 220pF for first input pulses; increase for slower input rise times.
R_1: Ratio R_1/R_2 sets fraction of supply voltage across C_1 at which the pulse period is completed. Typically R_1/R_2 = 0.1 to 0.3. If ratio is too low the period lengthens considerably but is ill-defined.
R_2: Current in R_2 should not fall below 1μA if timing is to be controlled by RC values.
R_3: With $R_3 = R_1$ the smaller current in R_3 is sufficient to keep the output high in the quiescent state.
D_1: Any general-purpose silicon diode.

Circuit modifications
● Positive-going output pulses can be obtained with a similar circuit if the permanent bias is applied to the inverting input, the direction of the diode reversed and a changing path provided in parallel with the diode. The quiescent condition has the output low with the diode conducting and significant current only in the 10MΩ resistor. A positive-going input transition drives the input high, which state is held until the capacitor charges sufficiently to allow the current in the inverting input to exceed that in the non-inverting input. A major advantage of an amplifier having both inputs accessible is that the signal pulses can be transferred to the other input. In this version, the output pulses would then be triggered by negative rather than positive transitions, while in the previous case which required negative transitions the response would then be to positive edges.
● Two-amplifier monostable circuits can have two opposite polarity outputs and allows separation of the triggering timing and output sections more readily. The circuit shown is equivalent to a Schmitt trigger followed by a monostable although the functions are combined in a single circuit. Out_1 is normally low contributing no current to the inverting input of the lower amplifier. Hence Out_2 is only driven low when V_{in} reaches ≈ $0.8V_{in}$. Provided the input falls below this level prior to the end of the pulse then generated, the circuit is suitable for resetting an oscillator when its ramp output exceeds a given d.c. level.

Circuit modifications



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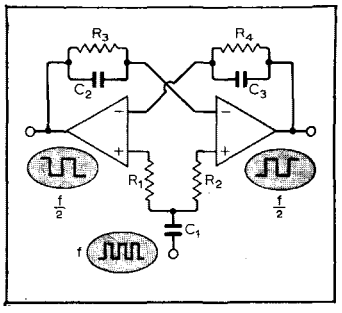
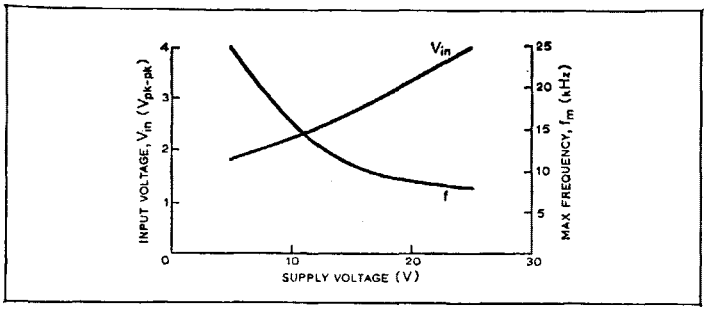
Flip-flops



Typical performance
IC: ½LM3900
Supply: +10V
R_1, R_2: 100kΩ
R_3, R_4: 1MΩ
C_1: 100pF
C_2, C_3: 56pF
v_o: 9V pk-pk
Max input frequency for satisfactory toggle action: 10kHz
Min. input amplitude: 4V pk-pk



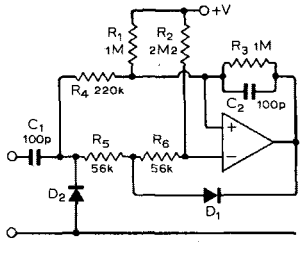
Circuit description
The circuit has strong affinities with standard two transistor flip-flop and could be triggered at either of the inverting inputs via diodes to provide a set/reset function. Non-inverting inputs provide the additional facility of triggering the flip-flop to provide a ÷2 action. Equal currents are fed into the non-inverting inputs on receipt of a positive-going edge but that amplifier whose output is already high because its inverting input receives no current will be initially unaffected. The other amplifier receives a short-duration current flow at its non-inverting input that exceeds that at its inverting input, and its output begins its positive-going transition. The speed-up capacitor couples this to the inverting input of the other amplifier and the positive feedback around the loop causes the transition to complete itself. Thus each output changes state in opposite directions on the receipt of each positive-going input transition. Two such transitions are required to complete each cycle of the output, and the output waveforms are complementary square waves at half the frequency of the input.

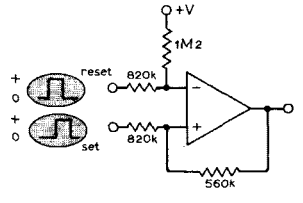
Such circuits may be readily cascaded to develop simple counters. Their low speed offers no competition to c.m.o.s., t.t.l. etc. but the ease with which they can be combined with other analogue/digital functions gives them a considerable advantage in many systems.

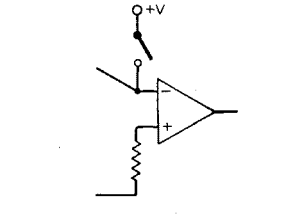
Component variations
+V: Standard supply range +4 to 36V. Samples may operate down to <2V.
R_1, R_2: Sensitivity can be controlled by varying R_1, R_2 for fixed values of R_3, R_4 and vice versa. Values are not critical and may be adjusted to suit a wide range of input pulses. 10k to 1MΩ.
R_3, R_4: These provide the current to keep the opposing amplifier saturated and are again not critical. 330k to 10MΩ could be used but as in any pulse system high resistances can be accompanied by spurious triggering. Generally the lower resistances are required at low supply voltages.
C_2, C_3: Speed-up capacitors ensure positive transitions but the maximum speed is limited by amplifier slew-rate.
C_1: Not critical. 47p to 470pF.

Circuit modifications
● Using a single amplifier, one or more diodes are used to channel the incoming pulses to the two inputs alternately, with overall positive feedback to latch the circuit. The quiescent state with the output high is sustained because both R_2 and R_3 contribute current to the non-inverting input, exceeding that in R_1. When the output goes low it remains there because now the non-inverting input receives current only via R_2, leaving the current through R, into the inverting input to dominate. In the latter state D_1 prevents any input positive-going pulse from reaching the inverting input and the circuit is triggered via R_4 into the high state. The succeeding positive pulse produces approximately twice the current through R_5, R_6 as through R_4 (D_1 is reverse biased), the output going low. C_2 is the speed-up capacitor and D_2 absorbs the negative transitions.
● Careful choice of the positive feedback in this circuit (middle) provides sufficient hysteresis to keep the output latched into a given state after an input pulse has returned to zero. Any further pulses on that input have no effect, and it requires a similar pulse on the other input to reverse the output. The input which drives the output to logic 1 is the set input, the other the reset and the circuit is an asynchronous RS flip-flop.
● To add set, reset facilities to the initial circuit, one of the amplifiers must be directly driven into its off-state by a current greater than the current pulse received from the input trigger. This overrides the trigger for that amplifier, while the other is automatically set with its output to logic 1 and the input pulses are again ineffective. A transistor may replace the switch. Shown in the bottom circuit.

Circuit modifications







Cross references
Set 2, cards 3, 8 & 9.
Set 14, card 1.
Set 17, cards 7 & 8.

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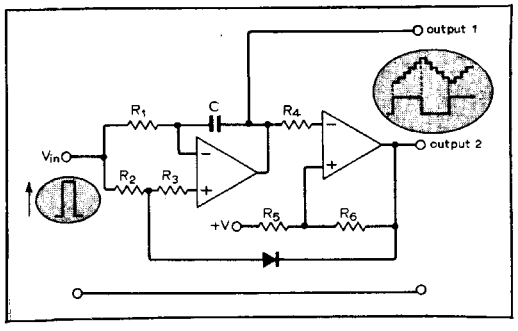
Staircase generators



Typical performance

Supply: 7.5V
R_1, R_4: 1MΩ
R_2: 120kΩ
R_3: 330kΩ
R_5: 10MΩ
R_6: 1.8MΩ
C: 1μF
D_1: 1N914

Input: pulse train +12V peak
Mark/space ratio: 2:1
Repetition rate: 30kHz
Output 1: staircase waveform 3.6V pk-pk, frequency 800Hz
Output 2: 6.8V pk-pk, frequency 800Hz

Circuit description

A staircase waveform can be generated by feeding pulses of current to a capacitor. The resulting circuits are closely related to those used in frequency meters such as the diode-pump circuit and its variants. One version as shown feeds the pulses to either the inverting or the non-inverting input of the first amplifier depending on the state of the output of the second. Consider output 2 positive. The diode is reverse biased and with $(R_2+R_3) = R_1/2$ the net positive current into amplifier 1 is positive. During each positive pulse output 1 ramps positively, remaining relatively constant between pulses. The smaller the mark-space ratio the more nearly the output waveform approaches a staircase waveform, with the rising steps occupying a small proportion of the time. At some positive voltage set by the resistors R_4, R_5, R_6 the Schmitt trigger operates, its output switching to near ground level. The diode becomes forward-biased diverting all subsequent positive pulses from the non-inverting input. The net negative input current via R_1 produces a staircase waveform in the negative direction until the lower threshold voltage of the Schmitt is reached and the cycle recommences. In essence the circuit is that of a square-triangle generator in which the direct control voltage is replaced by a succession of positive pulses giving a stepped characteristic to the triangular wave. The mean input voltage determines the mean charging current and the average slope of the ramp. If the frequency of the input signal is varied while maintaining a constant pulse height and constant mark-space ratio, then the basic repetition rate of the output remains unchanged. (It is composed of a number of steps dependent on the ratio of input frequency/output frequency.) Varying the pulse height, the mark-space ratio or Schmitt trigger points varies the output frequency.

Component changes

R_4, R_5, R_6: The magnitudes of these resistors are not critical and they may range from 10k to 10MΩ. Design procedure for the trigger levels is given on Schmitts and comparators card. Hysteresis ≈ $+VR_6/R_4$.
R_1, R_2, R_3: For comparable positive and negative slopes, $R_2+R_3 = R_1/2$. Ratio R_2:R_3 is not critical but neither should be $< R_1/10$. R_1: 10k to 1MΩ.
C: Controls the basic repetition rate of the output for given input waveform. 220p to 10μF. Output frequency can be very much less than input frequency with division ratios in excess of 100.

Circuit modifications

● When the input is at zero, current flow to ground through R_1 allows the stored voltage on C to vary. Inserting a diode prevents this at the expense of a reduced effective pulse height. Most other v.c.o. circuits can be adapted to perform this function. Replacing the diode by a transistor and controlling the pulses to the inverting input leaves the phasing correct. (Top.)

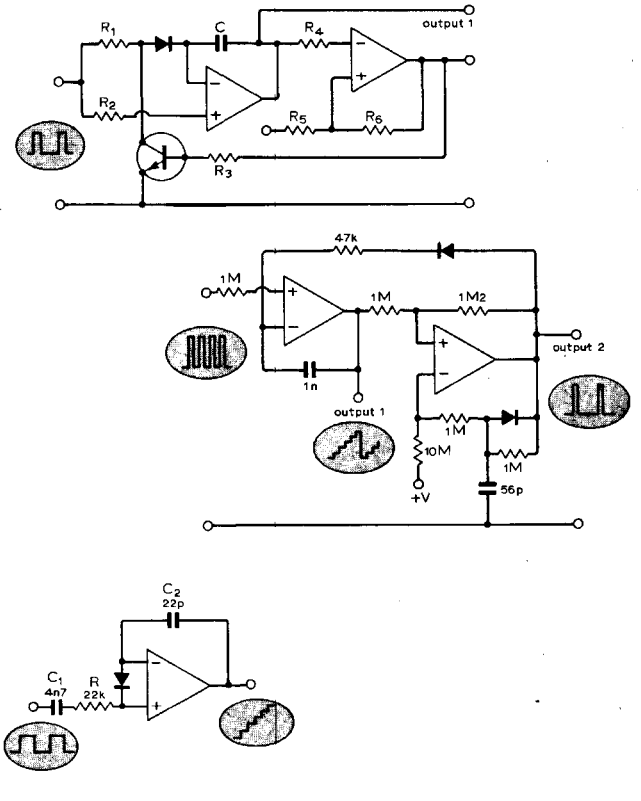
● To obtain a staircase waveform followed by a sharp transition, the Schmitt may be followed by a monostable circuit that provides a pulse of current to discharge the capacitor rapidly. Input pulses are fed to a single input as shown, and again alternative arrangements are possible by phasing input/feedback appropriately. Switching and timing actions can be combined in the single monostable shown, where the positive output pulse is initiated at a particular input amplitude, the timing remaining correct if the input voltage to the monostable falls below this firing level before the completion of the monostable output pulse. (Middle circuit.)

● Circuits designed for tachometer applications give an inherent staircase output. Further, the step height is controlled only by the input pulse height and the values of C_1, C_2, provided that the input pulse width is sufficient to allow full charge and discharge of the capacitor C_1. The version shown has a frequency doubling action with the positive input transitions being fed to the non-inverting inputs and the negative transitions to the inverting inputs.

Cross references

Set 3, cards 3 & 7.

Circuit modifications



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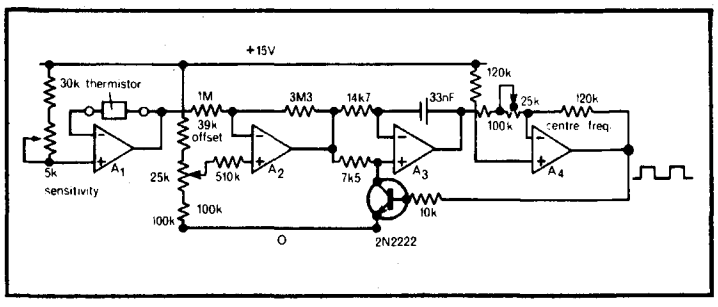
Set 17: c.d.as—signal generation Up-dat

1. A voltage-controlled oscillator is a basic tool in a number of instrumentation systems. In this example, a thermistor network having a linear variation of resistance with temperature is used as a temperature sensor. Placed in the feedback path of a current-differencing amplifier, the current through it can be controlled by the current injected into the non-inverting input. Thus the voltage output of A_1 is a linear function of temperature, and is buffered by A_2 to give a suitable offset scale—this allows the output frequency to be a



desired multiple of the temperature on the scale chosen (10 × temperature in deg F in the example given in the reference). The resistance of the thermistor falls with rising temperature causing the output of A_1 to fall, and of A_2 to rise, thus increasing the frequency. The reference gives full calibration procedures for a particular thermistor network of U.S. origin but any element or network having a linear p.d. against temperature could be substituted. Using a diode or amplified diode network, the rate-of-change of voltage with temperature would be less and the temperature range might conveniently be 0 to 100°C rather than 14-113°F in the original circuit.

Reference

Rufer, R. P. Circuit built with quad op-amp measures temperature digitally, *Electronic Design,* 1974, vol. 6, March 15, p. 160.

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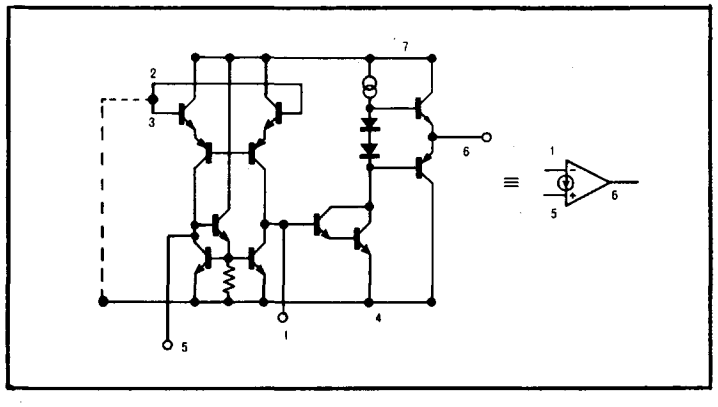
2. It is a commonplace of design that functions can be performed by particular devices/circuits, not planned for by the original manufacturer. They may be well within the device ratings, but just not mentioned on the data sheets. The circuit shown is a simplified form of basic uncompensated op-amps such as the 101/748 types and shows that both a current mirror and an output stage with inverting driver are present. These are normally driven by the input differential amplifier. The author of the reference article observed that the input stage can be



inhibited by returning both inputs to the negative supply rail. This leaves pins 1 and 5 (normally used for compensation purposes) available to act as the inputs of what is effectively a current-differencing or Norton amplifier. In principle, all the circuits in sets 16-18 can be implemented, while returning the inputs 2 and 3 to their usual voltage levels would allow one set of inputs to override the other and provide complex functions. The reference uses an audio mixer circuit as an illustrative example using both single-ended and dual supply voltages.

Reference

Jung, W. G. Op-amp in current-differencing mode becomes a non-inverting audio mixer. *Electronic Design,* 1974, vol. 6, May 10, p. 130.

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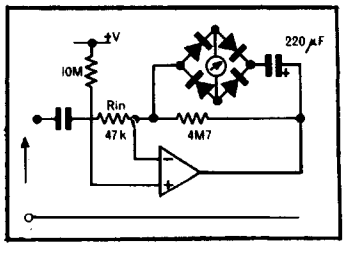
3. Some of the circuits described in sets 16-18 use diodes and/or the input current mirror to rectify the input signal: careful design allows the mean or peak output to be a linear function of the input, but the circuits still cannot respond to a.c. signals with amplitudes below p.ds. If the rectifying circuit is placed in the feedback path of the amplifier this limit is



removed. With a bridge rectifier a peak-peak output swing of at least 2.5V is required excluding voltage drops across the meter movement. This is well within the amplifier capability for supply voltages of 5V and above, provided the output is biased appropriately—to the supply mid-point for maximum swing. Two additional components are then needed in the feedback path, viz. a blocking capacitor (220μF) and a resistor (4.7MΩ) to set the quiescent output voltage in conjunction with the resistor to the non-inverting input (10MΩ). The meter reads the full-wave-rectified mean value of the input current assuming an ideal amplifier, and that current is given by v/R_{in}. The frequency response covers the audio band but it is not suited to high frequency measurements.

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Set 18: c.d.as — measurement and detection

A favourite theme of one of the Circard authors is to identify differences between and similarities of circuits of related function. Fitting circuits into a kind of family tree not only aids understanding, but can lead to development of new circuits. Peter Williams' article on Wien oscillators (*WW* Nov. 1971 pp. 541–7) is a good example of studying circuits collectively, and you will see the theme recurring in the Circard background articles from time to time. Often different realizations of similar circuits are quite unrecognizable when dressed in the clothing appropriate to the application. As the next article shows, there are strong similarities between rectifier circuits and sampling circuits, the last-mentioned using a switch to replace the rectifier diode. Similarly, when the resistive load is replaced by a capacitative one, the peak rectifier becomes a sample-and-hold circuit (cards 7 & 8).
A feature of current differencing amplifiers in sampling circuits is the relatively long hold time possible but so far they are not able to compete with standard op-amps in respect of accuracy. The feature common to most of the circuits in this set is simplicity, whether the application be providing negative resistance, interfacing with transducer, frequency measurement or defining currents for subsequent voltage measurement. For example, use of matched transducers delivering a variable current and followed by the current differencing circuit is a very simple way to sense differences in light intensity and temperature. In this set, card 1 forms an excellent summary card: read it first for a quick look at some of the possibilities.

Measurement and detection

Pattern recognition is one sign that a technology is reaching maturity. The early stages following new advances are a succession of bright ideas, half-worked-out theories and unrelated developments. This is inevitable as workers in many areas take from the original material that which meets their needs—or appeals to their prejudices.

In circuit design the same configurations appear under many guises and names, developed quite independently and for different applications. If we can recognize these similarities and construct the appropriate family tree this is worthwhile in itself.

But we can do more. If two circuits are similar in form because related in function, then by finding any other circuit designed for one of the functions there is a good chance that it can be modified to provide the other. A good designer is one who picks the best brains.*

The present topic is a particularly good illustration of this thesis. The problem is to measure some property of the amplitude of an a.c. waveform. Four circuits have their properties listed in the table and circuit diagrams representing a basic feedback form of each are shown in Figs 1 to 4. The configurations are identical, the differences lying only in whether conduction is through a diode or a switch, and whether the load is resistive or capacitive. This identity of form is far from apparent in practical versions since there are so many additional components and sub-circuits to optimize the response or effect coupling between other circuits/transducers.

The half-wave rectifier uses a diode as does the peak rectifier. It begins conduction through the diode as soon as the input goes positive remaining in conduction for the phase angle range 0 to π for sine-wave input. The mean value of the output is normally required, and a moving-coil meter is suitable as the deflection is proportional to the mean current.

*To quote Tom Lehrer:
Plagiarise Plagiarise
Remember why the good Lord made your eyes
So don't shade your eyes
But Plagiarise Plagiarise Plagiarise
—only please to call it Research

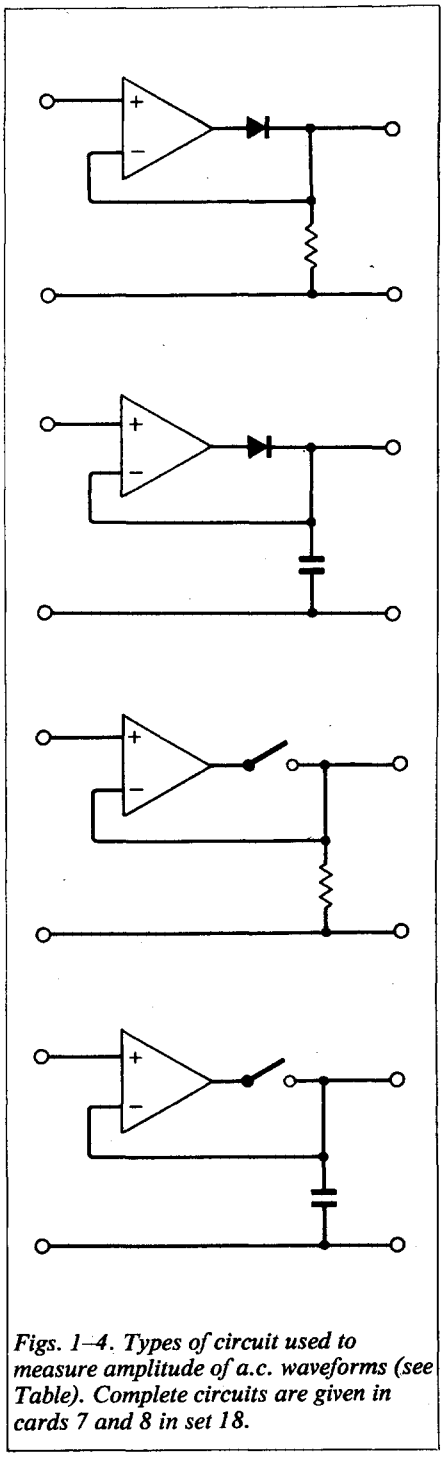
When the resistive load is replaced by a capacitor, conduction of the diode only takes place for those instants when the input voltage exceeds the voltage stored on the capacitor. For a steady-state a.c. signal this corresponds to the positive peak of the input, and assuming no discharge of the capacitor in the intervening period the conduction angle is vanishingly small and is centred on $\pi/_2$. The resulting constant voltage across the capacitor is measurable with any d.c. voltmeter whose input current requirements are so small as to avoid significant capacitor discharge.

To accommodate varying signal amplitudes some discharge must be permitted since a small amplitude would otherwise never be sensed if following a larger input. The resistive path leads to a compromise time constant between maximum holding time of the peak voltage and minimum recovery time after large peaks. Conversely, the half-wave rectifier suffers from capacitive effects at high frequency with stray capacitance leading to partial peak rectification. The resulting output/frequency characteristic often shows a rise of 1 to 3dB prior to the cut-off frequency limits of the amplifier.

The sampling circuit replaces the diode of the half-wave rectifier by a switch which closes for a brief interval at some phase angle determined by external circuits. The output is zero for all instants except the sampling instant. With capacitive loading, provided the switch closure is for a period of time greater than the time constant of the capacitance together with the amplifier output resistance, then the capacitor volt-

Four types of circuit, listed here, to measure the amplitude of an a.c. waveform—see Figs. 1 to 4.

Circuit	Load	Conduction angles, ϕ_1, ϕ_2	Conduction device	Voltmeter
Half-wave rectifier	R	$0, \pi$	diode	mean/d.c. moving coil
Peak rectifier	C	$\frac{\pi}{2}, \frac{\pi}{2}$	diode	d.c.
Sample	R	arbitrary $\Delta\phi \to 0$	switch	instantaneous
Sample and hold	C	arbitrary $\Delta\phi \to 0$	switch	d.c.



Figs. 1–4. Types of circuit used to measure amplitude of a.c. waveforms (see Table). Complete circuits are given in cards 7 and 8 in set 18.

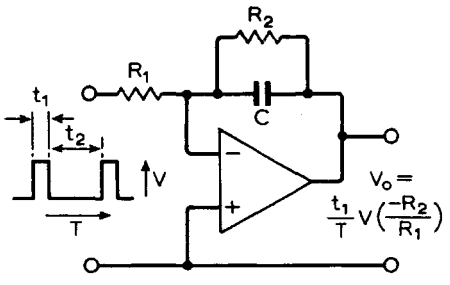


Fig. 5. LM3900 c.d.a. is well-suited to measurement of time period and frequency. An input capacitor can alternatively be charged through a diode to form a "pump" circuit (see card 10).

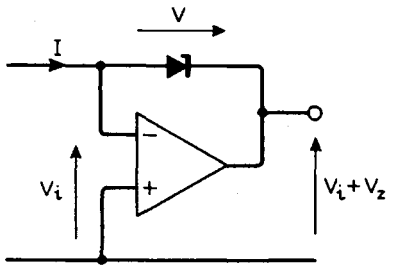


Fig. 6. Defining operating conditions for testing a zener diode with a c.d.a. (see card 5).

age becomes equal to the input voltage (again a compromise since the sampling period should not be so long as to allow a significant change in the input). If the switch is closed periodically at the same instant in successive cycles then the sampling time may be reduced, with the capacitor voltage increasing to the required level over a number of periods. With the switch open, as it is for most of the time, the capacitor stores or holds the sampled voltage, provided the measuring instrument is suitably buffered.

The sampling circuits are readily constructed with current-differencing amplifiers, and long hold times are possible. With careful adjustment the output drift can be < 5%/hour under controlled conditions which is a good performance from such a general-purpose circuit. The accuracy is less impressive since the current-mirror match is involved, and it cannot compete with standard op-amp circuits in this respect.

Measuring period and frequency

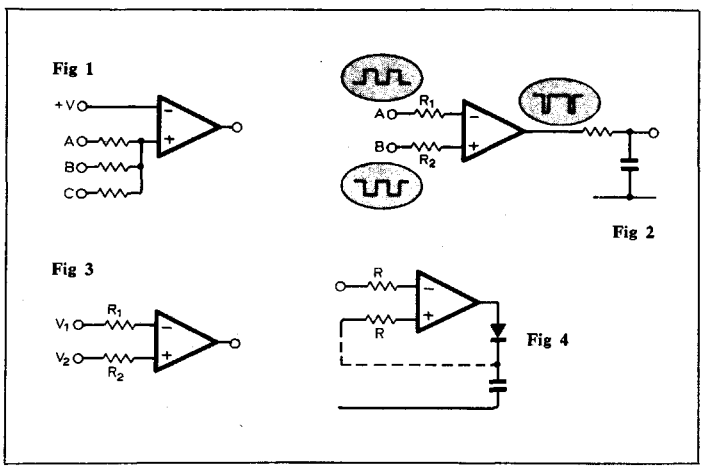
The measurement of time period and frequency is another field to which the circuit is well-suited. A pulse waveform of constant width and height but variable frequency is fed as in Fig. 5 to the amplifier with parallel RC feedback. The mean voltage across the capacitor is then directly proportional to the input frequency. Alternatively frequency and pulse height may be kept constant when the output becomes a measure of pulse width. The availability of two inputs extends this capability to the measurement of frequency difference or sum. Alternatively an input capacitor may be charged and discharged through a diode network to give the equivalent of a diode pump/transistor pump type of frequency meter (tachometer).

The d.c. characteristics of the amplifier can be used to simultaneously define the operating conditions of diodes, zeners etc, while providing a low output impedance point for ease of measurement (Fig. 6). Finally, the circuit may be used in conjunction with an external network of resistors and diodes to perform quite complex logic functions such as exclusive-OR. Though offering no competition for the usual logic families for large-scale applications, they are very convenient for providing a small number of logic functions in an existing system. The wide range of supply voltages particularly commend them for such applications.

Measurement and detection

Circuit description

These circuits operate largely in a switched or non-linear mode; one card deals with negative resistance circuits which can be considered as having controlled non-linearity.
The amplifier gain is large enough that simple logic functions are readily performed as described in set 16 (Fig. 1). By scaling the resistors the output of Fig. 2 becomes $\overline{A}+B$ and the smoothed output has a d.c. value dependent on the phase difference of the inputs if these are square waves. The phase detector combined with a v.c.o. (set 17) gives a p.p.l., see card 3. Scaled resistors can also be used to provide simple forms of threshold logic including the weighted comparator of Fig. 3, while the comparator, using equal-valued resistors if desired, forms part of the peak detector of Fig. 4. The capacitor charges through the diode until it matches the peak value of the input. Another application for the comparator is in coupling signals into and out of transducers. Positive feedback may be added to the system to provide hysteresis, or negative feedback to control the level of current/voltage in a load as when testing or measuring the properties of a device e.g. semiconductor breakdown voltages.

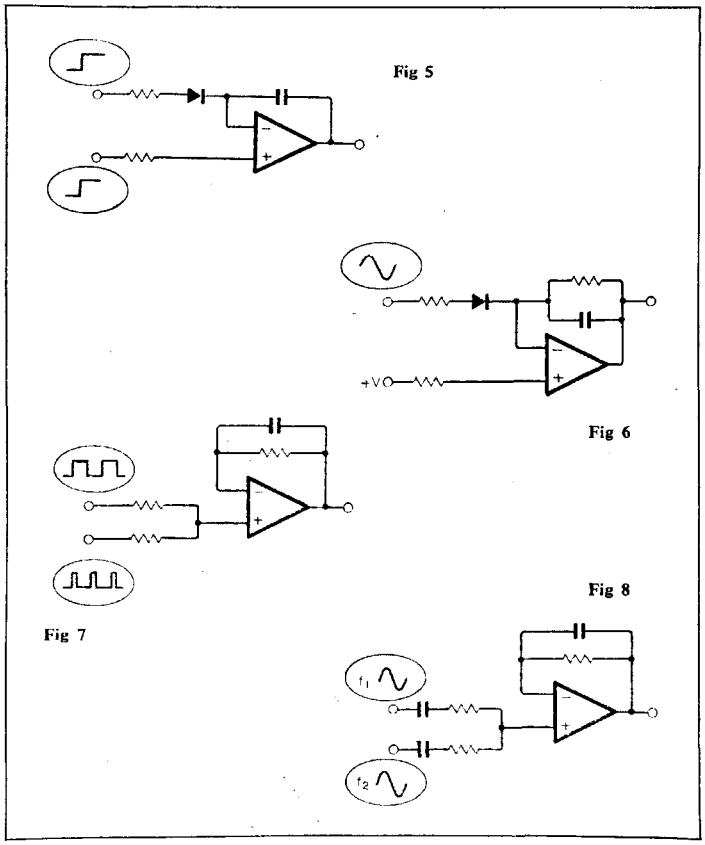


Further reading

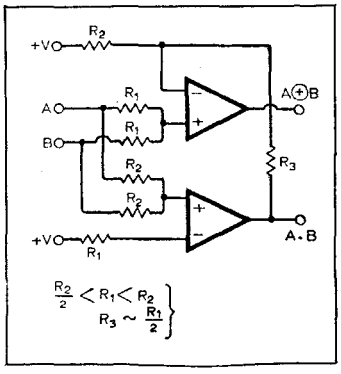
Frederiksen, T. M., Howard, W. M. Sleeth, R. S., The LM3900—A New Current-Differencing Quad of ±Input Amplifiers, National Semiconductor application note AN72.
Frederiksen, T. M., Norton quad amplifier subtracts from costs, adds to design options, *Electronics*, Dec. 6, 1973, pp.116-20.
Motorola Linear Integrated Circuit Data Book, pp.7-446, 7-453, 7-456 and 7-463; data sheets on MC3301P and MC3401P amplifiers.
National Semiconductor, Linear Integrated Circuits, pp.226-33, data sheets on LM3900.
Frederiksen, T. M., Howard, W. M., Sleeth, R. S., Use Current-mode IC amplifiers, *Electronic Design*, vol. 21, no. 2, Jan. 18, 1973, pp.48-55.
Mortensen, H., Use a quad amplifier to handle transducer bridge signals, *Electronic Design*, vol. 21, no. 3, Feb. 1, 1973, pp.74-6.

Circuit description

The integrator plays a large part in measurement circuits as in waveform generators. Sample-and-hold circuits are closely related to peak-detectors, in that a voltage is stored on a capacitor that is proportional to the input voltage at some defined instant (the sampling instant and the input peak voltage respectively). The ramp and hold circuit of Fig. 5 is an intermediate step between the two circuits. If a resistive path is placed in parallel with the capacitor then the mean voltage developed at the output is defined by the mean input. Access to both inverting and non-inverting inputs makes it possible to measure the mean value of the sum or difference of two inputs, with the capacitor minimizing the output ripple. The circuit of Fig. 6 formed part of a controlled-amplitude RC oscillator (set 17) detecting the mean value of a half-wave rectified sine-wave; that of Fig. 7 acts as a tachometer provided the inputs are of controlled amplitude and pulse width.
The non-inverting input has a non-linear v/i characteristic. Overdriven with two high-frequency signals it injects a current into the amplifier which contains sum and difference frequencies. If f_1-f_2 is a low frequency the filtering action of the RC network removes the high-frequency components while giving an output at f_1-f_2. This input stage is outside the feedback loop and is not frequency limited by the amplifier compensation. Low-level high-frequency amplification is possible using this input.



Logic circuits



Typical performance
IC: ½LM3900
+V: +20V
R_1: 82kΩ
R_2: 120kΩ
R_3: 33kΩ
Output logic 0: ≈150mV
Output logic 1: ≈19.2V
(with load current 5mA output logic 1 still within 1V of positive supply)

Circuit description
Just as t.t.l., c.m.o.s. gates may be interconnected to produce more complex functions, so the simple gate functions described on card 1 may be used in identical configurations. The standard methods for producing such functions as the exclusive-OR gate which has the output high for one and only one high input require four two-input NAND gates. This may be acceptable where it is desired to implement a system with a single device type even though multiple exclusive-OR circuits are available within a single package.
The flexibility of the current-differencing configuration allows such circuits to be designed economically while retaining the advantages of wide supply voltage range and good noise immunity—provided again that the circuit is restricted to industrial applications not requiring fast response. The lower amplifier is a standard AND gate as discussed in set 16, card 4, while the upper amplifier is an OR gate. By feeding back the AND gate output to the inverting input of the OR gate the logic 1 resulting from A=1 B=1 is inhibited by the logic 1 simultaneously appearing at the AND gate output. The resulting truth-table shows the output to be an exclusive-OR gate, but the simultaneous availability of the AND function creates a half-adder. It is obvious that such a circuit is no competitor to c.m.o.s. or t.t.l. for complex logic functions in view of the speed limitation. Where a small number of logic functions are to be introduced into an industrial system the availability of a circuit that will operate off virtually any available supply is a clear advantage. Being able to mix functions within a given package allows analogue and digital processes to be tackled efficiently.

Component changes
+V: +4 to +36V. In practice several samples of the device operated satisfactorily for supply voltages down to 2.7V at room temperatures.
R_1, R_2: Values may range from <10k to >1MΩ. There is no obvious advantage to lowering the resistances, but at high values capacitive strays may produce input current spikes significantly larger than the quiescent currents. For the AND gate, the current in R_1 must be less than current in R_2 while with both inputs high the current through the pair of R_1 must exceed that in R_2. For a logic 1 signal nearly equal to +V this gives $R_2/2 < R_1 < R_2$.
R_3: This has to provide enough current to override the OR gate action for A=1 B=1. Value is not critical and values from $R_1/2$ down to $R_2/2$ are satisfactory. Where the input is noisy, the input resistors may be centre tapped and the tapping point decoupled to ground. The high value of resistors used together with the wide noise margins possible at high supply voltages allows the circuit to accommodate high noise environments provided the supply is adequately decoupled.

Circuit modifications
● Interchanging inverting and non-inverting inputs on the OR gate converts it into a NOR gate (Fig. 1). Then the output in the absence of feedback through R_3 would be logic 1 only when both inputs are at logic 0. The feedback forces the output of the NOR gate to go to logic 1 when both inputs are at logic 1, overriding the normal NOR gate function. The net result is that the output of the NOR gate becomes logic 1 for A=B and the circuit is an equality comparator. The output can also be seen as the negation of the exclusive-OR function.

● It is not necessary to use two amplifiers to perform the exclusive-OR function. Instead, a passive AND gate using D_1, D_2 and R_1 keeps D_3 out of conduction except when A=B=1 (Fig. 2). Under these circumstances the current in R_1 is diverted through D_3 into the amplifier inverting input and overrides the OR gate action to provide a logic 0 at the amplifier output. A limitation in this circuit is the low threshold to the AND gate, with input levels rising above about 0.4V bringing D_3 into conduction i.e. 0-level noise margin is small.

● If the inputs of the original circuit are linked the result becomes a simple and readily-controlled window comparator. Replacing the paralleled resistors by single resistors the simplified form of Fig. 3 is obtained. For low input voltages both amplifier outputs are low. At some intermediate value, the lower threshold voltage V_L, output X goes high assuming $R_2/R_1 < R_3/R_4$ (Fig. 4). Output Y remains low. At the upper threshold output Y goes high driving X low. At some still higher input voltage a suitable choice of R_2, R_5 also allows X to go high again if required as the current in R_2 continues to increase while that in R_5 is restricted to $< V/R_5$.

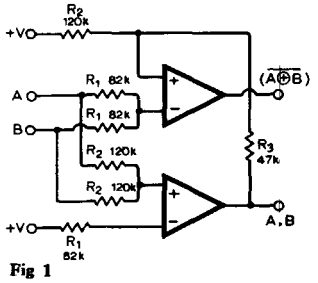


Fig 1

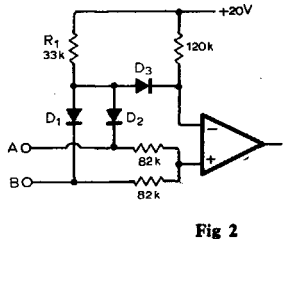


Fig 2

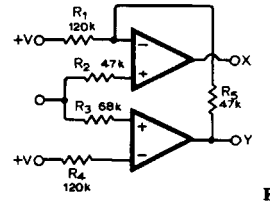
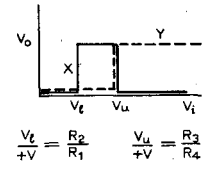


Fig 3

Fig 4



$\frac{V_L}{+V} = \frac{R_2}{R_1}$ $\frac{V_U}{+V} = \frac{R_3}{R_4}$

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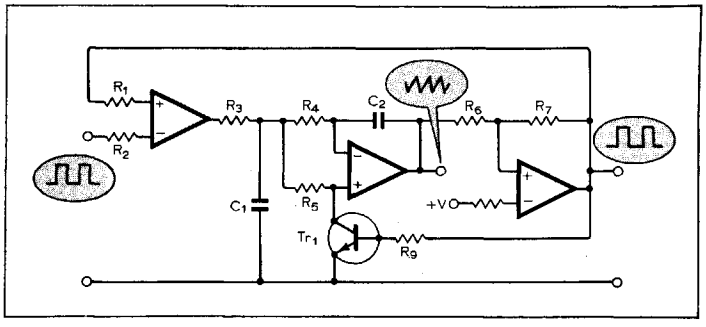
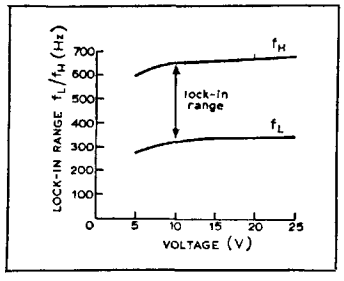
Set 18: c.d.as—measurement, detection—

Phase-locked loop



Typical performance
+V: +10V
R_1, R_3, R_9: 33kΩ
R_2: 68kΩ
R_4, R_6: 1MΩ
R_5: 470kΩ
R_7, R_8: 1.2MΩ
C_1: 0.1μF
C_2: 1nF
Tr_1: BC125
Capture range: 390 to 580Hz
Lock-in range: 320 to 660Hz
$V_{d.c.}$ over lock in range: 4.3 to 8.4V



Circuit description
There are three identifiable subsections to this phase-locked loop. The first is a phase-detector which receives one input from the signal source and one from the square-wave output of the voltage-controlled oscillator. The output of the phase detector, when the oscillator is locked to the signal source, is a negative-going pulse train of the same frequency but of mark-space ratio dependent on the phase difference between the two waveforms (see circuit modifications). Smoothed by a simple RC filter, a direct voltage results that controls the rate of charging of a capacitor in the second subsection, the integrator. When the output voltage from the integrator reaches a critical level it causes a change in level from the output of the third sub-section, a Schmitt-trigger circuit. This switches the transistor reversing the net current into the integrator and with it the direction of charging until the second trigger level is reached. This completes the cycle of the v.c.o., and if its frequency is close to that of the incoming signal, locking is achieved.
If the incoming signal changes its frequency slowly, the resulting phase difference produces a corresponding change in the direct voltage that controls the v.c.o. i.e. the frequency changes, remaining in lock, but with a new value of phase difference. If the frequency difference between the input and the v.c.o. becomes too great or if either varies too rapidly, locking can be lost. The lock-in range with this circuit is over a frequency range of about 2:1 while the capture range is somewhat smaller. In summary, frequency modulation of the signal source, if slow enough, produces pulse-duration modulation at the phase detector output. After filtering, which converts this p.d.m. into a varying direct voltage, the v.c.o. is frequency modulated causing it to track the original frequency variations of the signal.

Component changes
Schmitt: R_6, R_7, R_8. Design ranges are indicated on set 17 card 6. One change would be to design for smaller hysteresis. Increasing R_7 reduces the positive feedback to achieve this.
Integrator: To operate at low frequencies R_4, R_5 may be increased. This disturbs the frequency stability of the v.c.o. if used in a free-running mode, but closure of the feedback loop via the phase detector accommodates this at the expense of drift in the phase difference.
Filter: If the signal is expected to change frequency only slowly if at all, the filter time-constant can be increased with advantage.

Circuit modifications
● The phase-detector action is as follows: when both inputs are low the output is high. For equal amplitude inputs, and $R_1 > R_2$, then when both inputs are high the output is high since the current to the non-inverting input is greater than that to the inverting input. When only one is high the output is controlled by that input.

● Because the phase-comparator has an output with a minimum mark-space ratio of 1:1, the mean output voltage swings over the range $+V/2$ to $+V$ allowing a maximum frequency range for locking of about 2:1 assuming a linear v.c.o. By introducing an amplifier this range can be increased to any desired extent since the amplifier may be biased to give an output →0 i.e. the v.c.o. frequency may be driven to a very low value while lock is retained (Fig. 2).
● Phase difference between the received and generated signals is frequency-dependent since at any given frequency there is a specific direct voltage required by the v.c.o. and hence a specific phase difference at which the phase comparator can deliver that voltage. If the filter is replaced by an integrator with a pre-set bias, then provided the integrator has a high gain (approaches the ideal integrator), its mean output takes up a value appropriate to the incoming frequency, while the phase difference can be controlled by varying R (35k to 70kΩ to provide phase differences from 0 to π with values shown in Fig. 3). This is because the net current into the integrator →0 when the output is to remain constant.

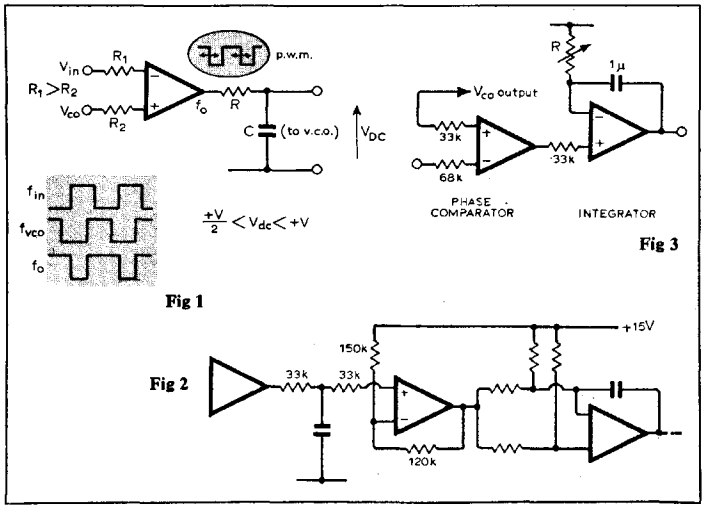
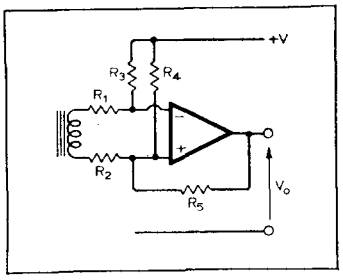


Fig 1

Fig 3

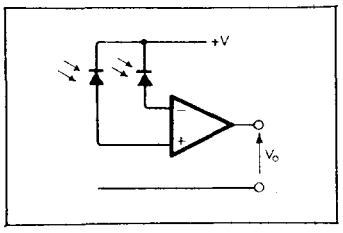
Fig 2

Transducer driving



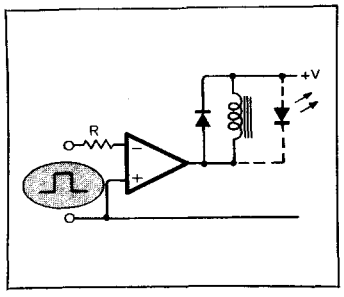
Typical performance
+V: +10V
R_1, R_2: 220kΩ
R_3, R_5: 5.6MΩ
R_4: 10MΩ
Hysteresis: 400mV

Circuit description
Where the input signal is from a transducer which has a floating and preferably low resistance output, the circuit shown gives a convenient means of setting the trip points symmetrically about the zero-voltage state of the transducer. With the output at zero and $R_1 = R_2$, $R_3 = R_5 = R_4/2$ then with the transducer output at zero, the net current into the amplifier is $V(1/R_4 - 1/R_3)$. With the output at +V the net input current is $V(1/R_4 + 1R/_5 - 1/R_3)$. With the above conditions these currents reduce to $\pm(V/R_4)$ respectively. The input sensitivity/impedance depend on R_1, R_2 increasing the former reducing the latter. Sensing of signals ≪100mV is not recommended but the circuit has reasonable rejection of high frequency noise/strays because of the relatively large input resistances used together with the effective input capacitance (said to be around 2nF by the manufacturer).



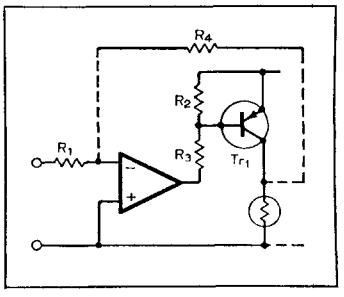
Typical performance
Inputs can be any pair of matched linear or non-linear transducers, which deliver a variable current for a fixed p.d. as the physical parameter under test varies e.g. reverse-biased silicon photodiodes giving current proportional to light intensity.

Circuit description
Current-differencing characteristics of the amplifier make it particularly suitable as a comparator of input currents from whatever source they may come. Accuracy of matching of the input stages is not such as to allow very high precision but in routine applications it can be used for rapid detection of out-of-tolerance resistors excessive leakage currents in diodes etc. One of the inputs is fed from a standard element or with a current defined by an external resistor while the device under test is connected between the other input and the positive supply line. Transducers such as photodiodes and transistors, photoconductive cells operated at low light intensities, and thermistors, can be used in matched pairs to sense the difference between physical parameters at two different locations while offering compensation against changes in any common variable (temperature effects on photoconductors etc.).



Typical performance
+V: 12V
R_L: 600Ω
R: 100kΩ
v_i: > +10V

Circuit description
The normal sink current is provided by a constant current stage of about 1.3mA. An additional internal transistor when over-driven can provide an output sink current of up to 30mA with a reasonable saturation voltage (>0.5V). This output current depends on the combined current gains of two internal transistors, allowing input currents as low as 100μA to provide sufficient drive. Output current is sufficient to drive small filament lamps and relays. As usual to protect the amplifier against reverse voltage spikes on switch-off a parallel diode is added. Driving of l.e.ds requires precautions since the device p.d. is ≪+V leaving a large amplifier dissipation at high supply voltages. Either reduce supply voltage or use resistance in series with l.e.d. to limit current.

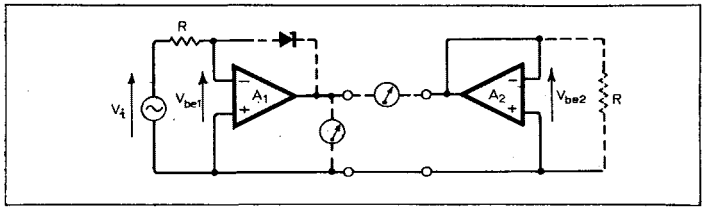


Typical performance
+V: 10V
R_1: 10kΩ
R_2, R_3: 470Ω
R_4: 100kΩ
Tr_1: BFR81
R_L: 40Ω

Circuit description
A single transistor with a current gain in saturation of >10 increases the load drive capability to >250mA. Resistor R_3 is included to minimize the p.d. across the amplifier output transistor when switched to the low state. Feedback via R_4 to the inverting input provides positive feedback for sharply defined switching (because of additional inversion by the transistor). Output swing can be to within a few hundred millivolts of the supply with a suitable power transistor and this allows for a well-defined hysteresis. The value of R_1 is reduced to allow sufficient input current to the amplifier to hold the required output state as the switching point is approached. If hysteresis is not required, R_4 is eliminated and R_1 reverts to the value used in the previous circuit i.e. that value that results in an input current of about 0.1mA at the given size of input pulse.

Cross references
Set 9, cards 1, 11.
Set 13, cards 2, 4, 8.
Set 16, cards 2, 3, 5, 6.
Set 17, card 6.

Semiconductor device testing



Circuit description

One application to which the matching characteristics of the amplifiers can be applied is the testing of semiconductor devices. To find the d.c. characteristics of a zener diode for example, the current should be defined (or measured) and the terminal p.d. measured over a wide range of currents. If the currents are low then this makes the measurement of voltage more difficult. In the circuit shown the direct current in the diode is given by V_{be}/R where V_{be} is that of the amplifier input transistor. At very low currents the diode carries the 30-nA amplifier input current as well. If the amplifier output voltage to ground is measured it gives the zener voltage after subtraction of the V_{be} term. Output impedance is low even at low zener currents, simplifying the voltage measurement. For these amplifiers the V_{be} term is little dependent on the feedback current (though somewhat more so on the output voltage). As the zener voltage is substantially constant, the V_{be} voltage can be conveniently measured when operating at a relatively high current yet will be valid for the lower currents. It is not necessary to make these two separate measurements since there are other amplifiers in the package with almost identical V_{be} values. One of these amplifiers is biased as shown and the voltage measurement taken between the two outputs. These are both low impedance points allowing a wide choice of voltmeters without significant loading. Matching between the amplifier V_{be} values is not perfect and improvement follows from operating the amplifiers at equal currents i.e. by placing equal resistance values to ground. By superposing an alternating voltage of peak-peak value $< V_{be}$ at the input, as from a generator whose internal d.c. resistance $\gg R$, an a.c. current is defined in the device under test. The alternating voltage at the output then gives a measure of the dynamic or slope resistance of the device.

Component variations

+V: Must be $>(V_z+2V)$ to allow for amplifier V_{be} plus output saturation voltage. Not critical within these limits. Rejection of supply changes improved when using compensating amplifier (to as little as 1μ V/V effect on V_{be} differentials).

R: 50Ω to 10MΩ. The range corresponds to maximum output current of about 10mA down to minimum current of 50nA. At this lower level accuracy is poor because of amplifier input current of 30nA.

If v_i, the input alternating voltage, is kept constant as R is varied, then since V_{be1} is substantially constant, the alternating current superposed on the d.c. remains a constant fraction. With zener diodes operated in their normal region the zener voltage varies little, any variation in slope resistance shows clearly in the variation of the output a.c. component.

V_i: Peak-peak voltage $< V_{be1}$. Typical values of 0.1 to 0.3 V_{be1}.

Circuit modifications

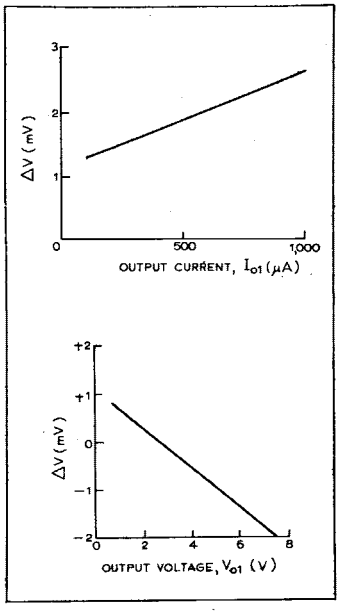
● To define the current accurately it is not enough to rely on the constancy of the input V_{be} particularly if the temperature is subject to variation. A simple alternative is to take the resistor to the negative supply rail (if available) through a diode to give compensation against the remaining small effect of V_{be} variations (Fig. 1).

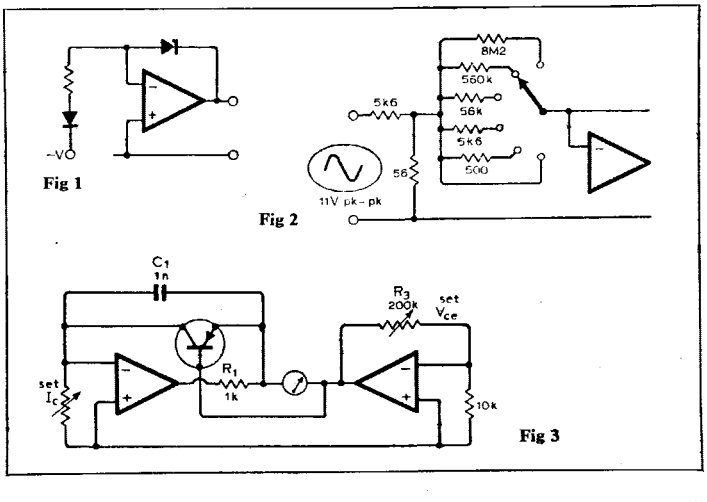
● Fig. 2 circuit varies the d.c. resistance to ground from the amplifier input terminal in 10:1 steps. The equivalent alternating voltage generated in series with this resistance is about 110mV pk-pk or about 20% of the V_{be} value. Current range as shown is 100nA to 10mA.

● A p-n-p transistor may have its V_{be}/I_e characteristic plotted using a similar arrangement. Collector current is defined with the emitter taken to the output of one amplifier, the base to the other. R_1, C_1 control the h.f. characteristics to maintain stability. By varying R_3, the V_{ce} value for the transistor can be controlled to show the small effect of V_{ce} on the I_c/V_{be} characteristics; n-p-n transistors cannot be dealt with so simply using this form of circuit.

Typical performance

IC: ½LM3900
+V: +15V
R: 5.6kΩ
Zener current: $\approx 100\mu$A
Amplifier input V_{be} unbalance, $\Delta V \approx$ 2mV for V_z of 6V
N.B. ΔV varies with both V_o and I_o but V_o in turn is approximately constant for a given zener.
Zener d.c. $\approx V_{be1}/R$
Zener a.c. $\approx v_i/R$

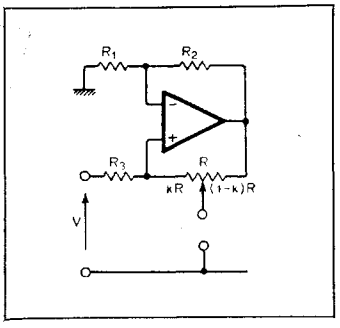




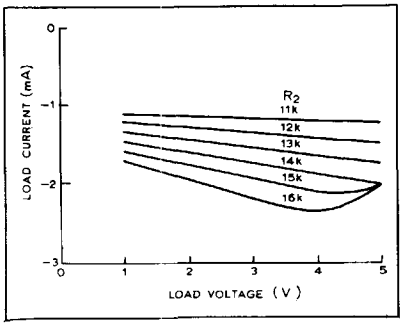
wireless world circard

Set 18 : c.d.as—measurement, detection—6

Negative resistance



Typical performance
IC: ¼LM3900
k: 0.5
R_1, R_3, R: 10kΩ
R_2: 15kΩ
Dynamic output resistance: −9.3kΩ
V_S: +15V
V: 5.3V (set for output current of 1mA with R_2 trimmed for output resistance →∞)



Circuit description
A potent tool in the design of oscillators and certain classes of active filters is the negative-resistance circuit, which may also be a particular case of a negative-impedance converter. A previously described constant-current circuit may be adapted to give a controlled negative output resistance, by allowing the overall positive feedback to exceed the negative feedback. The circuit remains stable only when the external load re-establishes the supremacy of the negative feedback. In the circuit shown, a short-circuit load eliminates the positive feedback altogether indicating that the circuit is short-circuit stable. For $R_2/R_1 > R/R_3$, the open-circuit load condition has excess positive feedback and switching of the output would occur. For intermediate values of R_L, the load current as defined by the voltage V and potentiometer setting k is observed to fall as the load-resistance is reduced. For the values shown, $R_2 = 10k\Omega$ gives the limiting case of output resistance →∞, and increasing values of R_2 produce a negative resistance of falling magnitude. Maximum current in the load is restricted to about 2mA with $k = 0.5$ but the amplifier itself restricts the current to around 10mA regardless of the resistance values chosen. In principle, emitter followers can be added at the amplifier output with all the resistor values lowered to increase the drive capability, but for most applications it is the small-signal performance that is of interest.

Component changes
R_1, R_3, R: It is often convenient to have these equal. Minimum value is dictated by loading effects on output and would not generally be much below 10kΩ. Negative slope resistance available is comparable to these values.
R_2: Controls the slope of the resistance, together with the tap on R. Range 10 to 20kΩ.
k: 0.2 to 0.8. For application suggested later, where only small negative resistance effect required $k = 0.5$ is satisfactory.
V+: +4 to +36V. Normal operating range for amplifier.
V: Used to set the output current to some range over which R_2 controls the negative slope +1V to +8V for $V_+ = 15V$.

Circuit modifications
● A typical application is to introduce a negative slope resistance into a circuit normally used as a constant-current source. This may be either to overcome some positive resistance due to leakage paths etc, or simply to modify the waveform produced in a generator. Here the circuit provides the charging current to a capacitor that is part of an astable circuit having some similarity to a unijunction oscillator (Fig. 1). Capacitor imperfections plus external resistors would result in a ramp whose dV/dt fell at higher amplitudes. By increasing the negative slope, more current is fed into the capacitor as the p.d. across it increases. This can linearize the slope or with over-compensation cause the slope of the waveform to increase at higher voltages.

● For other applications a direct equivalent of the negative-impedance converter is required. In Fig. 2 the voltage gain of the amplifier is +2. Hence the voltage appearing across the resistor R′ is equal to the input voltage in magnitude but in a sense that returns a proportional current to the source. This leads to an input resistance of $-R'$ (shunted by $+R$ where R can be up to 10MΩ is required representing a small error).
● The previous circuit is short-circuit stable in that a low source resistance ensure that the positive feedback is bypassed, leaving the negative feedback in control. With the alternative configuration in Fig. 3, the negative feedback overrides the positive feedback provided the source impedance is greater than R′. Additional bias resistors from the amplifier inputs to the positive supply line may be used to set desired output quiescent levels

Cross references
Set 3, card 8.
Set 6, card 6 (AC constant-current circuits, see note on front).
Set 17, card 5.

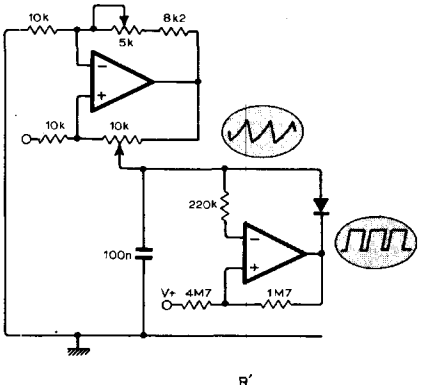


Fig 1

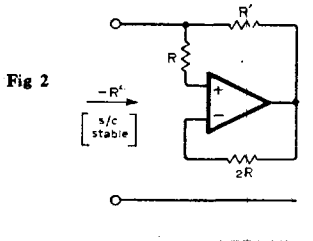


Fig 2

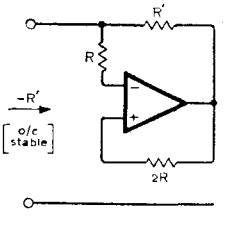
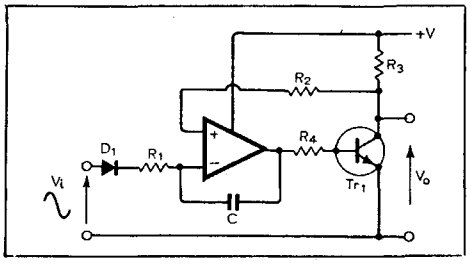


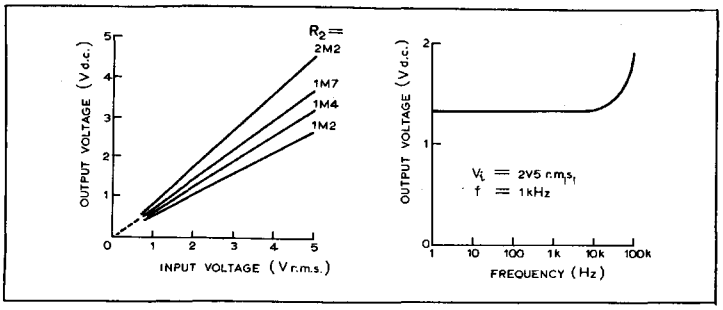
Fig 3

wireless world circard

Peak/mean rectifiers



Typical performance
+V: +15V
Tr_1: BC125
R_1: 1MΩ
R_2: 1.2MΩ
R_3: 10kΩ
R_4: 6.8kΩ
C: 10μF
D_1: 1N914
v_i: 2.5V r.m.s., 1kHz
v_o: 1.35V d.c.



Circuit description
The mean value of an alternating voltage can be obtained by rectifying the signal (half or full-wave) and applying the resulting output to a mean-sensing instrument such as a moving-coil meter. Alternatively the rectified waveform may be filtered and applied to a d.c. voltmeter (including a d.v.m.). In each case one or more diodes or transistors are required to perform the rectifying function, and they introduce two related errors into the response of the circuit. Non-linearity in the diode causes a corresponding non-linearity in the transfer function. In particular, at very low levels the signal is insufficient to bring the diode into conduction. This gives an offset to the transfer function. If other diode effects can be added, then the offset together with its temperature drift can be largely cancelled. Rectification of signals below about 0.5V r.m.s. is still impossible but above this level the error can be small.
In the circuit shown the amplifier integrates the difference between the currents caused by the rectified input signal and the mean voltage at the transistor collector. For a particular value of R_2/R_1 the diode and V_{be} drops provide partial cancellation, and the transistor collector potential becomes a linear function of the mean half-wave rectified input. (Although the slope if extended would pass through the origin, rectification of low-level signals cannot be achieved with this circuit.) The value of R_2 obtained empirically for this circuit differs somewhat from that previously proposed for the related section of the Wien bridge oscillator. The values of R_4, R_3 can be adjusted over a wide range to accommodate differing load resistors/meters etc while the capacitor can be increased to give adequate smoothing for frequencies <1Hz. At high frequencies partial peak rectification may occur in the input section because of stray capacitance while shunt capacitance across R_1 will increase the input current. A slowly rising response is observed up to 1MHz.

Component changes
+V: Not critical, provided it is $>(V_o+1V)$. For higher output currents R_3 would become too low if supply/output differential is too small.
Tr_1: Any silicon n-p-n small-signal transistor. No significant h.f. response required because of integrating action of C on rectified waveform.
R_1 sets input impedance and should be high to minimize loading on source (important because of non-linear input impedance). If too high then capacitive strays become more significant. 100k to 10MΩ.
R_2: Ratio to R_1 sets optimum slope to minimize offset effect. Empirical result suggests $R_2/R_1 \approx 1.25$, manufacturers suggest $R_2/R_1 \approx 1.6$ for similar circuit.
R_3 has to carry maximum meter current at maximum output voltage i.e. should be <10kΩ for 1mA meter movement at 5V full-scale and 15V supply.
R_4: Not critical, avoids excessive non-linear loading on amplifier output. 3.3k to 33kΩ.
C sets degree of ripple reduction at low frequencies. C>22μF is necessary for f<1Hz if needle flutter is to be reasonable. C may be <1μF for higher frequencies (self-inductance of electrolytics may cause problems at h.f.)
D_1: Small-signal silicon diode.

Circuit modifications
● A very simple alternative circuit is that used for the basic tachometer (see also set 17 card 2). In this (Fig. 1) the input transistor of the amplifier non-inverting input provides the rectifying action directly. Reverse half cycles inject current into the damping circuit which may cause disturbance to the other amplifiers in the package. A low voltage-drop diode (germanium, Schottky) may be used to absorb this reverse current but leakage effects with germanium would force the use of lower resistance values. The mean current in the two inputs will become comparable because of the negative feedback while the capacitor removes the ripple as before.
● A peak detector with gain is shown in Fig. 2, in which the capacitor is charged until the current in R_3 equals the sum of the currents in R_2 and R_1 taken at the positive peak of the input voltage. At all other points in the cycle, the diode is non-conducting and some loss of charge takes place through R_3. Resistor R_2 provides a small forward bias. Resistor R_3 cannot be increased greatly without introducing a large error term due to the amplifier input current. The diode is within the feedback loop and the error term due to the diode drop →0 at low frequencies. Amplifier slew-rate limiting prevents the circuit from approaching the frequency response of the previous circuits.

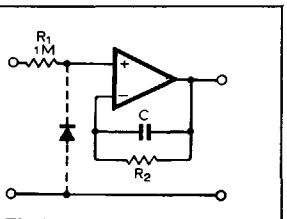
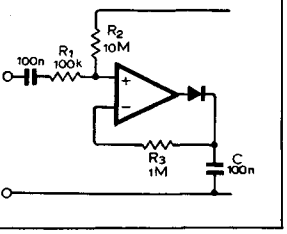
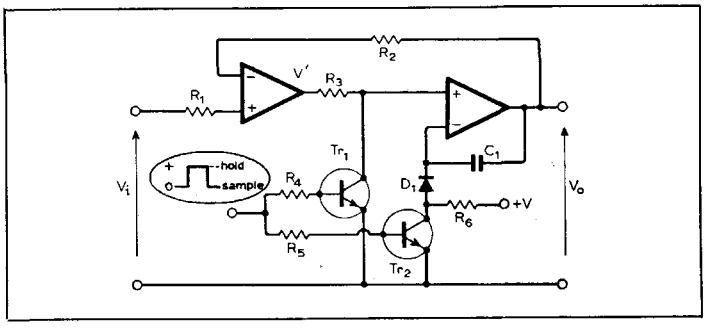


Fig 1



Cross references
Set 4, cards 2, 3, 5, 9, 10.
Set 9, card 12.
Set 17, cards 2, 3.

Sample and hold circuits



Typical performance
+V: +15V
R_1, R_2: 1MΩ
R_3: 22kΩ
R_4, R_5: 47kΩ
R_6: 33kΩ
C_1: 0.1μF
D_1: 1N4148
Tr_1, Tr_2: BC125
Input range: +1 to +14V
Output drift: +0.2V/s
in hold mode

Circuit description
If an ideal integrator is incorporated into an overall d.c. feedback loop, then the capacitor charges until it provides an output voltage equal to (or some set multiple of) the input voltage. It introduces a time delay into the loop by virtue of the maximum charging current that can be provided by the amplifiers and so the speed of response of the amplifier is limited. If the loop is interrupted at any instant such that the integrator input current is reduced to zero, the p.d. across the capacitor remains substantially constant at the value corresponding to the input just prior to that interruption i.e. the signal can be continuously or periodically sampled with the facility to hold the value of the input at any required instant. Amplifier input currents, capacitor leakage etc cause drift in this held value but with care drifts of $< 5\%$ are possible for periods of 5 to 30 minutes with simple circuitry. With the control input low (sample mode) the integrator receives current to its inputs via R_3 and R_6/D_1. It integrates the difference between those currents until the currents in R_1, R_2 are substantially equal, bringing v′ into its linear region. Any increase in v_i raises v′ and hence the current into the integrator non-inverting input until v_o tracks the charge in v_i. Allowing for an ideal current mirror at the amplifier input $v_o/v_i = R_2/R_1$ though V_{be} effects only cancel well for $R_2 \approx R_1$. In the hold mode currents in R_3, R_6 are grounded and the only currents affecting v_o are the amplifier input current plus capacitor leakage.

Component changes
R_1: Sets input resistance. If too high then amplifier input current becomes significant. 100kΩ to 10MΩ.
R_2: $R_2 = R_1$ gives best compensation against V_{be} drifts, but unequal sensitivities at two inputs can be compensated for by trimming the ratio for $v_o = v_i$ at maximum output.
R_3: Set for sufficient current at v′ maximum to override current in R_6. Typically $R_3 \approx$ 0.5 to 0.8 R_6. Maximum current should not exceed, say 5mA; too low a current restricts maximum rate of charge.
R_4, R_5: In conjunction with hold/sample pulse must be sufficient to saturate Tr_1, Tr_2.
D_1: Low reverse leakage diode for least error in hold mode.
C_1: High value increases time-constant for minimum drift in hold mode. High-leakage capacitors unsuitable, since leakage should be $\ll$ 30nA if capacitor is not to be limiting feature of circuit. Too high capacitance slows down charging rate forcing longer sample period.

Circuit modifications
● The four amplifiers in the package are closely matched, and the input current of one can be used to generate an output voltage that drives a comparable current into the other. Trimming the 2MΩ resistor (Fig. 1) compensates for input-current induced drift while over-compensation can be used to minimize the additional leakage in C_1, D_1. Compensation can be exact at only one combination of C_1 temperature output voltage etc, but with care the output can remain stable to within 1% for several minutes using low cost capacitors.
● By using only one of the switching transistors, Fig. 2, the sample mode remains unchanged, while in the hold mode only input voltages below the stored value are ignored i.e. the output voltage is updated each time the input exceeds its previous peak value, holding the new peak pending any further increase. It is a form of peak-reading voltmeter.
● Using the other switching transistor (Fig. 3), then with the pulse input low the transistor is non-conducting and the sample mode is attained. When the pulse input is high the amplifier output is driven to its zero state regardless of the input.

Cross references
Set 4, card 7.
Set 11, card 11.
Set 18, card 7.

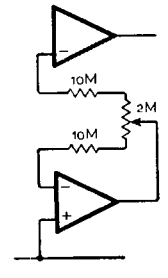


Fig 1

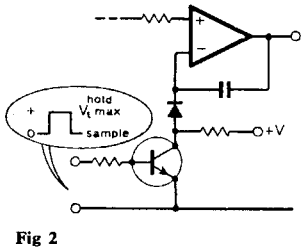


Fig 2

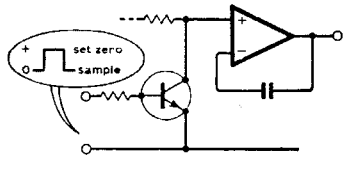
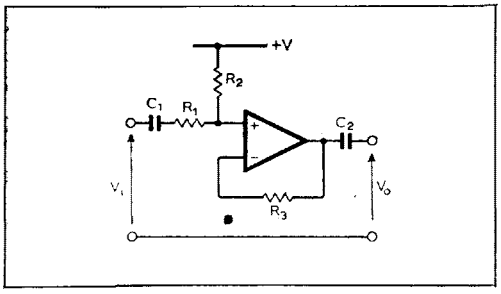


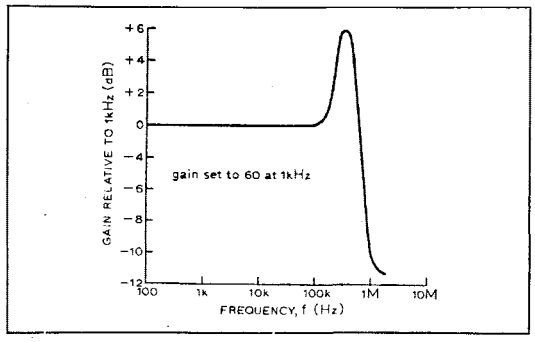
Fig 3

wireless world circard Set 18: c.d.as—measurement, detection—9

High-frequency circuits



Typical performance
+V: 10V
R_1: 1kΩ
R_2: 220kΩ
R_3: 100kΩ
C_1: 10μF
C_2: 1μF
Voltage gain: 60 @ 100kHz
Input impedance: 1.5kΩ
Output impedance: 100Ω



Circuit description
The gain-bandwidth of a feedback amplifier is a good measure of performance over a wide range of frequencies if the fall-off in gain is due to a single dominant lag as for these current-differencing amplifiers. If there is no external path to ground from the inverting input with such an amplifier while a conducting path is provided between that input and the output, there is effectively 100% feedback and the amplifier attains its maximum bandwidth. To inject a signal without reducing the effect of this feedback, the signal is fed directly into the non-inverting input. This is outside the feedback path with this amplifier but couples the signal in via a high impedance path internally (see circuit modifications). The disadvantage is that the feedback exercises no control over the input impedance at the non-inverting input i.e. the input current depends on that impedance and hence on the bias level. For most operating conditions the practical gain is 20 to 40% below that predicted on the basis of R_3/R_1 alone. Output swing available is small at high frequencies being limited by the positive slew-rate limitation of about 0.5V/μs. Hence at 500kHz, the peak-peak output cannot exceed about 500mV without distortion becoming serious. There is a variation in gain with supply voltage largely due to the effect of bias current on the input impedance at the non-inverting input but this can be held to ±10% for a 2:1 variation in supply voltage.

Component variations
+V: Normal supply range for amplifier. Higher voltages allow higher input bias current for given value of R_3. Hence input resistance at non-inverting input falls allowing gain to approach more nearly to R_3/R_1.
R_1: Sets input impedance; add on input resistance of non-inverting input $r_i \approx 25k\Omega/I_{bias}$, where I_{bias} is current in R_2 in μA. Range 1k to 10kΩ.
R_2: Sets bias as $I_{bias} = +V/R_2$ and direct output voltage as $+VR_3/R_2$. Range 100k to 1MΩ.
R_3: Sets gain in conjunction with R_1. For $R_1 \rightarrow 0$ overall voltage gain $\rightarrow 20 \times$ magnitude of supply voltage in volts.
C_1, C_2: Chosen in conjunction with R_1 and load resistance to define low-frequency cut-off. Typically 0.1 to 10μF.

Circuit modifications
● The non-inverting input is a current mirror with the input transistor behaving as an almost ideal p-n junction having transconductance g_m of 40mA/V (mS) at a current of 1mA with g_m proportional to the bias current. The exponential characteristic restricts the signal swing to a few millivolts if distortion is to be minimized. Such an input stage can be added to other amplifiers provided that the direct voltage at the amplifier input keeps Tr_2 out of saturation (Fig. 1).
● A second high frequency application takes advantage of this diode non-linearity, by injecting two high frequency signals at f_1, f_2. If the difference in frequency between these signals lies within the amplifier gain range and the amplitudes are large enough to give significant distortion products then a term at $f_1 - f_2$ appears at the amplifier output. Other terms f_1, f_2, $f_1 + f_2$ etc lie outside that range and the circuit has acted as a non-linear low-frequency mixer (Fig. 2).
● An alternative input is shown in Fig. 3 for use with signals of widely differing amplitude and is convenient for determining the frequency of an unknown signal in the low r.f. range if a large amplitude signal of comparable frequency is available; $(f_1 - f_2)$ is then measurable on audio-frequency equipment.

Cross references
Set 12, cards 1, 3, 8, 9.

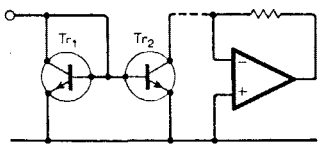


Fig 1

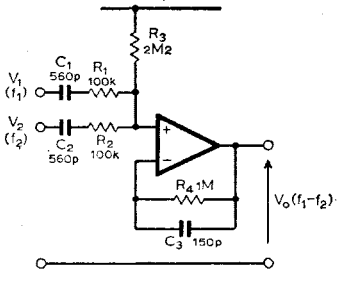


Fig 2

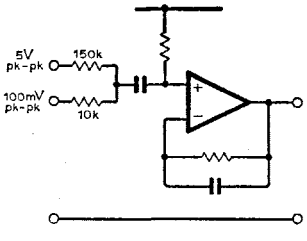
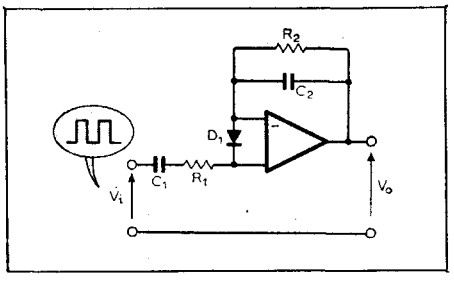


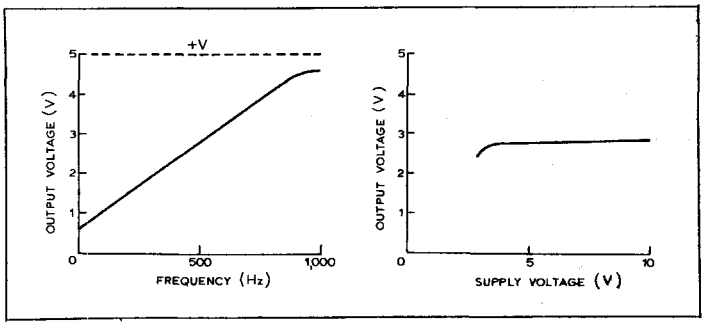
Fig 3

wireless world circard

Tachometers



Typical performance
+V: +5V
v_i: 5V pk-pk
R_1: 10kΩ
R_2: 1MΩ
C_1: 1nF
C_2: 0.1μF
for f: 500Hz,
v_o: 2.78V



Circuit description
A tachometer using both inputs of the current-differencing amplifier can reduce the ripple in the output voltage for a given frequency. It has some similarity to the diode pump circuit, in which the two diodes are D_1 and the equivalent input diode at the non-inverting input. When the input goes positive the amplifier input diode is driven into conduction and capacitor C_1 charges through R_1 until the p.d. across it is $(V_i - V_{be})$, assuming that the positive peak is held for a time appreciably greater than R_1C_1. The current mirror action at the amplifier input ensures that an equal current flows in the inverting input, causing C_2 to charge with the output going positive. When the input returns to its most negative value, D_1 comes into conduction and C_1 discharges. Current drawn through R_2/C_2 is in the same sense in both cases i.e. the effects of charging and discharging C_1 are additive at the output, doubling the effective frequency of the pulses. The mark/space ratio of the pulses is not important and need not even be constant provided only that the duration of each is sufficient to allow complete charge/discharge. Overall sensitivity is controlled by C_1 and R_2 with R_1 serving to limit the peak input current and C_2 to smooth the output d.c. In each cycle C_1 gains and loses charge of C_1v_i. This corresponds to a net current in R_2 of about $2fC_1v_i$ if f is the repetition frequency, a factor 2 coming from the fact that R_2 has to carry current corresponding to the direct discharge of C_1 via D_1 and also a current equal to the charging current because of the current mirror action as outlined above. Hence the mean output voltage is $\approx 2fC_1v_iR_2$ ignoring V_{be} effects. The time constant C_2R_2 should be $\gg$ period of waveform for low ripple.

Component changes
R_1 limits peak current to <1mA and preferably 100μA or less for high temperature operation. If too high prevents completion of charge/discharge cycles at high frequencies $C_1R_1 < 0.1f$.
C_1 sets sensitivity contributing two units of charge C_1V_1 on each cycle to the output. 100pF to 1μF.
R_1: Average current flow in R_1 is equal to the average of the charge gained and lost by C_1 as above. Because amplifier input current is low a mean current in R_2 of about 1μA is still sufficient to give moderate accuracy i.e. R_2 can be as high as 10MΩ but better accuracy for values of 1MΩ or less.
C_2: Time constant R_2C_2 determines ripple remaining on output with $R_2C_2 \gg 1/f$ for minimum ripple. C_2 must be low leakage or leakage resistance will cause loss of accuracy. 0.01 to 1μF.
D_1: Not critical. Any silicon diode.

Circuit modifications
● Transfer function of circuit is linear in v_o/f but there is an output offset of $V_{be}+(I_-)R_2$, where $I_- \approx 30$nA and $V_{be} \approx 0.55$V. By using a second amplifier with an identical feedback resistance and taking the output signal as shown, the output is substantially zero for zero input signal i.e. the transfer-function remains linear but passes through the transposed origin. The offset has good temperature compensation (Fig. 1).
● Simpler tachometer circuits are possible with some relaxation in specifications. For input pulses of defined width t_1 and current I, the mean current in the resistor R must be equal to that at the non-inverting input by current mirror action i.e. $i_R \approx fIt_1$ and the output voltage smoothed by C is $v_o \approx fIt_1R$. If the pulse width remains constant then $v_o \propto f$. No current flows in the non-inverting input when the input signal is at zero (Fig. 2).
● The output may be made to pass through zero by adding a diode at the output inside the feedback loop and with common-mode biasing. A load resistance $\ll$200kΩ should be present to ensure that the current in R_f can flow to ground while developing a very small voltage (Fig. 3).

Cross references
Set 3, card 3.
Set 13, card 6.
Set 14, cards 6, 9, 10.

Fig 1

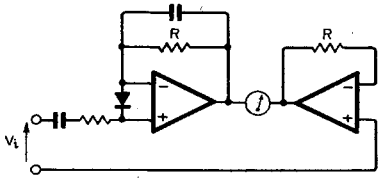


Fig 2

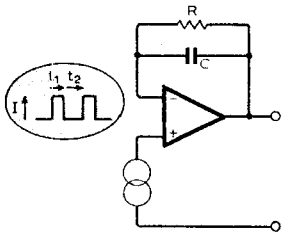
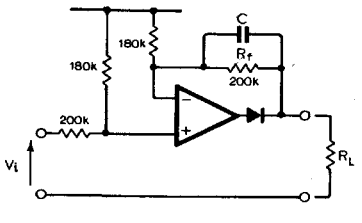
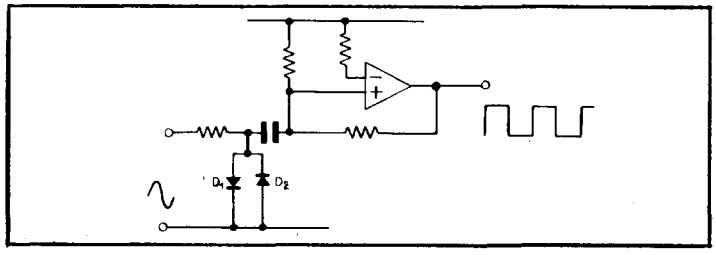


Fig 3



wireless world circard Set 18: c.d.as—measurement, detection Up-date

1. In any signal-processing circuit, the input may contain transients which might damage the amplifier or interfere with its operation by saturating it etc. The usual technique of adding a pair of back-to-back diodes across the input with a resistive limiter is equally



applicable to these amplifiers. It is shown preceding a Schmitt trigger, and clips the input to an approximate square-wave which is then applied to the Schmitt to produce a square-wave almost equal to the supply in amplitude.

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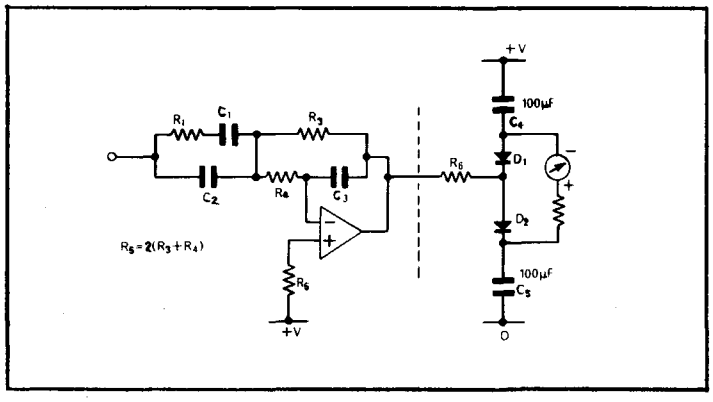
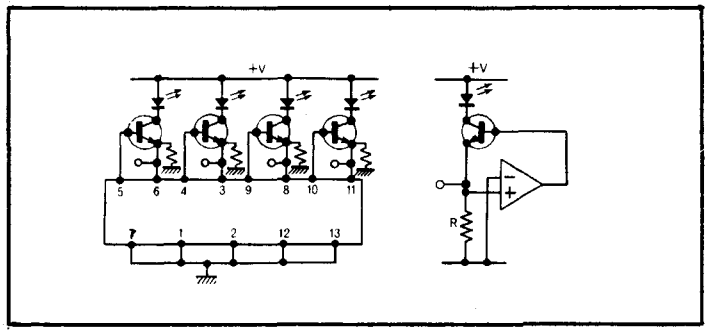
2. Two other circuits help to augment the range of functions available to users of current-differencing amplifiers. In addition to active filters as usually understood there are amplifiers with defined frequency responses, i.e. having a number of low frequency and high frequency time-constants often widely spaced. These can be realized using purely passive networks though loading of one by the other can be a problem. The circuit illustrates a combination of lead and lag networks, with C_1, C_2 reducing the gain at low frequencies and C_3 reducing it at high frequencies. Such circuits are useful in audio frequency instrumentation when a response matching various CCIR, NAB, BS or DIN curves are required. In such applications information may be needed about the peak-peak value of the signal after such processing. An example is in the measurement of wow and flutter for a tape recorder, and the meter drive circuit shown is a simple solution.



Regardless of the quiescent output, the capacitors C_4 and C_5 charge until the sum of their p.ds equals the supply voltage. When the output swings positive, D_2 conducts charging C_6 positively; for negative-going swings D_1 conducts, pulling C_4 in the negative direction. Provided the time constant of the meter circuit and the C_4, C_5 combination is long compared with the period of the lowest frequency component the ripple is small and the meter reads the peak-peak output voltage. The diodes should be low voltage-drop devices to minimize errors at low levels and can be replaced by germanium transistors with collector-base shorted.

---

3. Where many current differencing amplifiers are to be checked, the circuit shown can help. Each amplifier is connected to a l.e.d./transistor combination such that the transistor has to force a current into R (and hence the l.e.d.) sufficient to raise the inverting input to 0.5V, its normal value for linear operation. With $R = 100\Omega$ the 5mA current in the l.e.d. brings it to the level of visibility. A gross failure with either drive the output high (l.e.d. bright) or low (l.e.d. off). A more detailed check is to compare the potentials at the inverting inputs—these points have a low resistance to ground because of the 100Ω resistors, and the meter used need only have a sensitivity capable of registering a p.d. of a few millivolts but its resistance is not critical. The matching between inputs on a given chip is quoted in the reference article as typically 2mV and between different amplifiers from a production batch as 20mV.



Reference
Tenny, R. Check Norton amplifiers quickly, *EDN*, 1974, March 5, p. 72.

wireless world circard

Set 19: Monostable circuits

Monostable circuits, often referred to as multivibrators, can take various forms. The term multivibrator seems to have been used for Abraham and Blochs astable two-triode circuit of 1918, and the related bistable Eccles-Jordan circuit of 1919. Flip-flop or monostable circuits were developed a few years later, for example the 1926 transitron of van der Pol. Many of the early circuits used two timing capacitors, being derived from the a.c.-coupled multivibrator, but all of the monostables described in this set of cards use one timing capacitor. The most well-known arrangement (card 1) can be thought of as derived from the cross-coupled bistable circuit, with one resistive coupling replaced by the timing capacitor.

Recovery time is often too long with this straightforward circuit. Cards 1 & 2 show a complementary arrangement that has short recovery time (RC/β), but a possible disadvantage is that both transistors conduct in the quiescent state. Other methods are shown in the article, e.g. use of a diverting diode to prevent saturation (Fig. 3), addition of an emitter follower as shown in Fig. 4, and a circuit in which the on and off transistors are transposed, Fig. 6 (see also card 10). Emitter-coupled circuits, card 6, have the advantage of isolating the output point from the remainder of the circuit.

As with the astable circuits of set 8 this collection includes t.t.l. circuits (card 4), op-amp circuits (card 3) and circuits using c.m.o.s. devices (cards 5 & 8). Long delay circuits use the D-type flip-flop or unijunction transistors (card 8) and improved duty cycle is obtained with the circuits of card 10. A voltage-variable delay is provided by the circuits of card 7 of around 7 to 90μs and 40 to 200ms.

The monostable . . . doth give us pause

Not quite the words of Hamlet, but delay is one outstanding property of the monostable circuit. De Bono, in *The Mechanism of Mind,* could be describing another function of the circuit when he writes, "a short-term memory is just a way of extending the influence of an event beyond the real time of its occurrence along the dimension of time", e.g. a monostable will accept a transition at its input and respond with an output pulse, but for a finite time. A more formal description of the monostable (sometimes called a one-shot) is a circuit having one stable state in which it remains until triggered by an external signal into a quasi-stable state, where it remains for a time determined by circuit parameters and subsequently returns to its stable state. This basic action allows the monostable to be used for a variety of purposes such as lengthening, delaying and regenerating pulses, sequential timing and delay applications and frequency division.

The nature of the monostable circuits can be widely different because they can be designed using n-p-n and p-n-p bipolar transistors (in cross-coupled emitter-coupled and complementary modes), field-effect transistors, operational amplifiers, discrete and integrated-circuit logic gates, as well as purpose-designed monostable integrated circuits.

A very common type of monostable uses a cross-coupled configuration which can be thought of as being a modification of a symmetrical bistable where one resistive coupling is replaced by a capacitive coupling. Two possibilities are available; the timing capacitor can either be connected between the collector of a normally-off transistor to the base of a normally-on transistor, or between the collector of a normally-on transistor and the base of a normally-off transistor. Fig. 1 shows a circuit of the first type and Fig. 2 the associated current and voltage waveforms.

Transistor Tr_2 is in a stable on state, until triggered, due to the base drive supplied through R_2. Transistor Tr_1 is held in a stable off state as R_4 is connected to Tr_2 collector which is at the low saturation value of v_{ce2} and R_3 is returned to the negative V_{BB} rail. When a positive-going trigger pulse is applied to Tr_1 base via C_1 this transistor turns on causing its collector voltage to fall to almost zero.

Because the charge on C_2 cannot change instantaneously, this negative-going transition is passed to Tr_2 base which switches off. The transistors remain in these states while the charge on C_2 changes via R_2 causing v_{be2} to rise exponentially towards $+V_{CC}$. When v_{be2} passes through zero and rises positively to a value depending on the type of transistor used, which causes base current to flow in Tr_2, this transistor begins

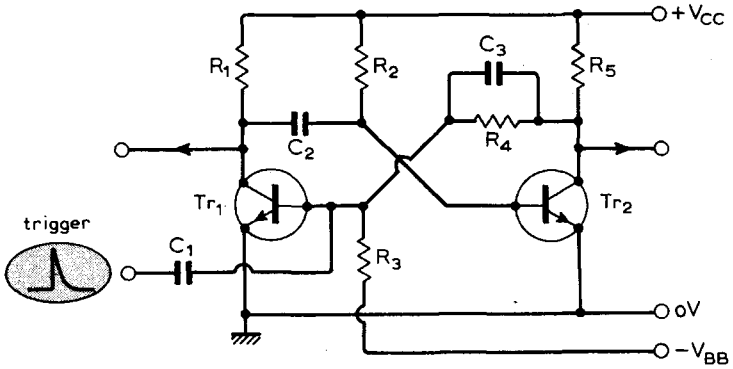


Fig. 1. A common monostable can be thought of as a bistable circuit with one resistive coupling replaced by a capacitative coupling. Two can be connected as shown.

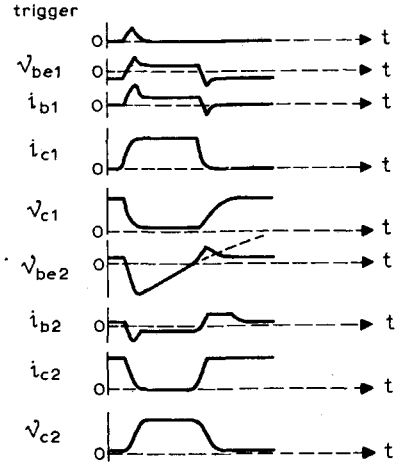
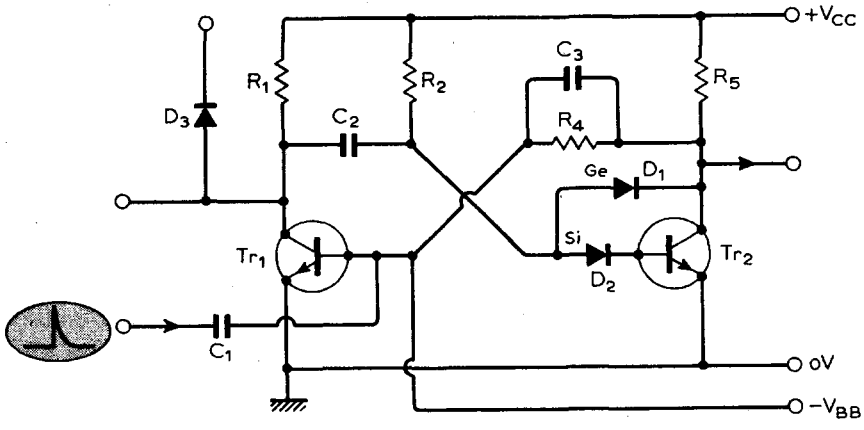


Fig. 2. Waveforms associated with circuit of Fig. 1.

Fig. 3. Switching speed of Fig. 1 circuit is improved by preventing saturation with diodes D_1 and D_2. Clamping diode D_3 reduces recovery time by connection to a supply less than V_{cc}.



to turn on. The resulting fall in v_{c2} is coupled to Tr_1 base via C_3, Tr_1 beginning to turn off; the regenerative feedback via C_2 and C_3 causes the circuit to return to its stable state of Tr_1 off and Tr_2 on, the capacitor C_2 recharging through R_1.

The switching speed of this kind of circuit can be improved by using higher speed switching transistors in a non-saturating circuit. To prevent saturation, germanium diode D_1 and silicon diode D_2 can be added as shown in Fig. 3. When Tr_2 begins to turn on, to return the circuit to its stable state, D_1 will be reverse-biased until v_{C2} falls below $(v_{be2}+v_{D2})$ causing the excessive base drive current, which would otherwise saturate Tr_2, to be diverted through D_1. Two series-connected germanium diodes can be used in place of the silicon diode D_2. The waveform at Tr_1 collector can have a slow recovery time, especially when driving capacitive loads, and this can be reduced by the addition of the clamping diode D_3 returned to a supply $V_A < V_{CC}$. The output voltage v_{C1} attempts to rise towards a higher value with D_3 present but becomes clamped at $(V_A + V_{D3})$ when D_3 conducts.

Another method of reducing the recovery time is to include an emitter follower between R_1 and C_2 of Fig. 1, as shown in Fig. 4. As C_2 is charged to almost the supply rail voltage, the emitter of Tr_3 is normally close to $+V_{CC}$. The input trigger pulse switches the circuit to its quasi-stable state and as the charge on C_2 changes, the emitter voltage of Tr_3 rises above its base voltage (v_{C1} on) cutting the transistor off. When Tr_2 again begins to conduct, the circuit returns to its stable state with C_2 being rapidly recharged by the emitter current of Tr_3.

The output from Tr_1 collector can be made to more closely approach a rectangular pulse by the inclusion of an isolation diode D_4 as shown in Fig. 5. When Tr_1 is on the collector current flows through R_1 and R_7 in parallel and a faster recovery time is achieved by making $R_7 < R_1$ so that when Tr_1 switches off D_4 is reverse biased and C_2 recharges more rapidly, through R_7, than in the circuit shown in Fig. 1. Other methods of triggering this type of monostable include negative pulses to either Tr_1 collector or Tr_2 base or positive pulses to the base of another transistor having its collector and emitter respectively connected to Tr_1 collector and emitter.

Another form of the cross-coupled monostable is shown in Fig. 6, the major difference compared with the foregoing circuits being that Tr_1 is on and Tr_2 is off in the stable state. This is achieved by correct choice of the potential-dividing chain and by D_2 being forward-biased via R_4, holding the base-emitter junction of Tr_2 reverse-biased. A negative-going input trigger pulse causes Tr_1 to switch off and hence Tr_2 to switch on and to remain in that state as C_2 charges, part of the charging current being base drive to Tr_2. Diode D_2 is reverse-biased in this quasi-stable state which ends when the base drive to Tr_2 has fallen to a level which will not maintain conduction. Transistor Tr_2 then switches off causing Tr_1 to return to the stable on state.

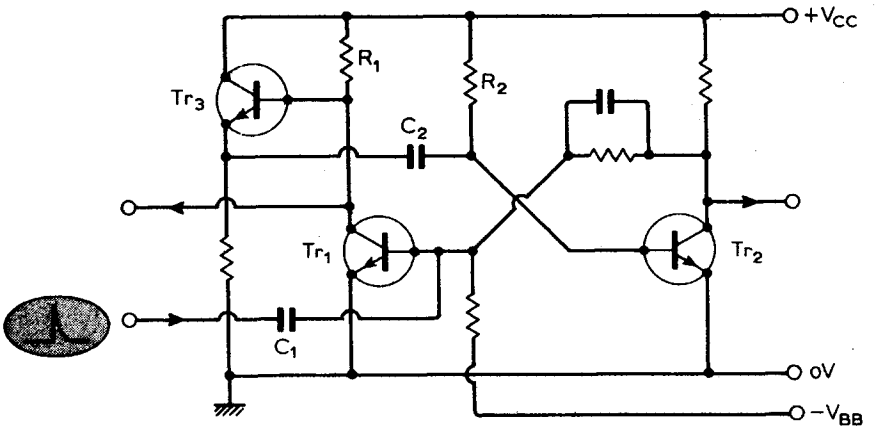


Fig. 4. Recovery time can also be reduced with an emitter follower between R_1 and C_2 of Fig. 1.

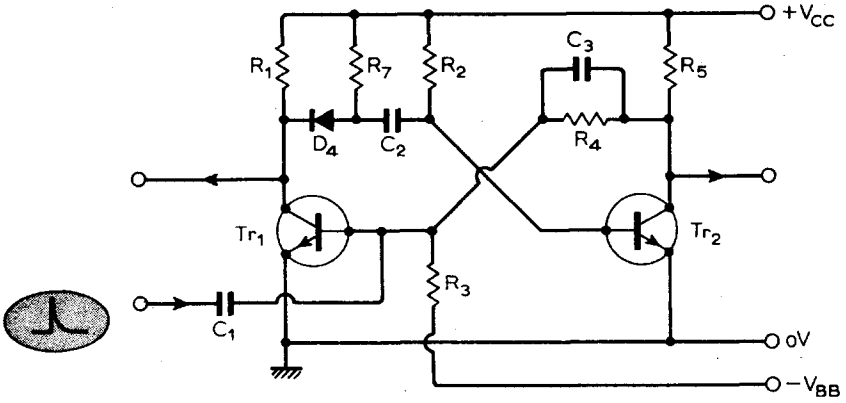


Fig. 5. Output from Tr_1 is made more rectangular by isolation diode D_4 and by making $R_7 < R_1$.

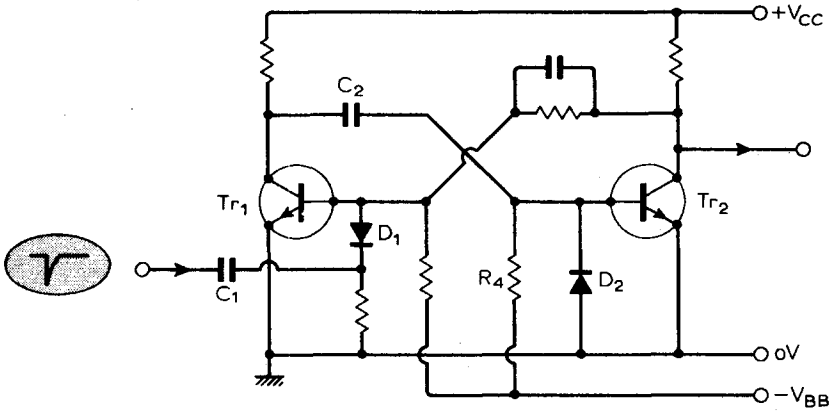


Fig. 6. In this variant of the cross-coupled monostable, Tr_1 is normally on and Tr_2 normally off. Note trigger is of opposite polarity. Circuit has much faster recovery time.

No output is taken from Tr_1 collector as a load at that point significantly changes the off time of Tr_2. This circuit has a much faster recovery time than the previous ones discussed.

A cross-coupled monostable which besides producing a time-constant-dependent output pulse may provide one due to the input pulse duration is shown in Fig. 7. In the stable state Tr_1 is on and Tr_2 is off, so when a short-duration trigger pulse is applied via D_1 the circuit remains in its quasi-stable state for a time determined largely by C_1R_3. However, when a long input pulse is applied, Tr_1 will remain off until the input is removed even if C_1 completes its discharge during that interval.

Fig. 8 shows an emitter-coupled monostable where Tr_2 is on and Tr_1 is off in the stable state. Compared with the cross-coupled circuits, this type has the advantages of only using a single supply and providing an output which is taken from a point having no internal coupling. When a negative-going trigger pulse is applied to Tr_1 collector via C_1 it is coupled to the base of Tr_2 which switches off. The emitter voltage falls allowing Tr_1 to switch on for a time determined by that required for C_2 to discharge sufficiently to allow Tr_2 to begin to conduct. The emitter voltage then rises, causing Tr_1 to begin to switch off, and the resulting rise in Tr_1 collector voltage is coupled to Tr_2 base which switches on, and Tr_1 switches off to regain the stable state. Due to the presence of R_4, the output voltage swing does not approach V_{CC} and the recovery time is not very fast, as R_3 should be greater than R_6 to ensure the correct switching action.

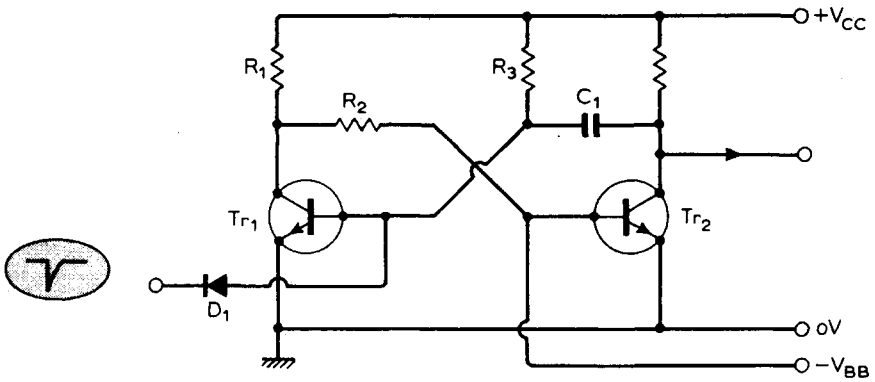


Fig. 7. This circuit produces an output pulse dependent on input pulse duration.

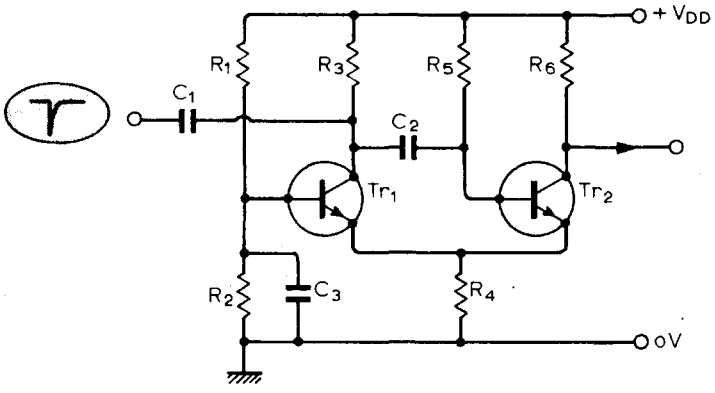
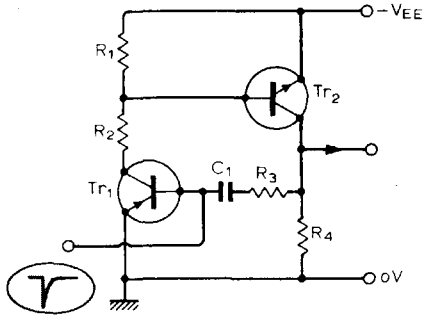
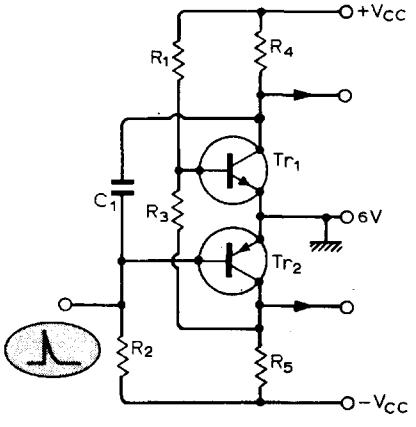


Fig. 8. Emitter-coupled circuit needs only one supply line and gives a more isolated output.



Complementary transistors enable both transistors to be normally off (Fig. 9, above) or normally on (Fig. 10, right). Opposite-polarity outputs are available from Fig. 10.



Recovery time can be improved by the addition of an emitter follower as was done in Fig. 4.

A monostable using a complementary pair of transistors, having both transistors off in the stable state, is shown in Fig. 9. A negative-going trigger pulse applied to Tr_1 base causes this p-n-p transistor to switch on, its collector current in R_1 and R_2 causing the base of Tr_2 to go positive causing this n-p-n transistor to switch on also. The resulting collector current in R_4 causes the output voltage to go negative and this change is coupled to Tr_1 base through C_1 causing Tr_1 and hence Tr_2 to be switched hard on. In this quasi-stable state C_1 charges through R_3 and Tr_2 towards $-V_{EE}$ and when the charging current is insufficient to maintain conduction in Tr_1 this transistor switches off, as does Tr_2 and the circuit returns to its stable state.

Fig. 10 shows a complementary monostable in which both transistors are on in the stable state, and which provides a pair of opposite-polarity outputs simultaneously. A positive-going trigger pulse applied to Tr_2 base turns both transistors off and after C_1 charges sufficiently, through R_2 and R_4, both transistors return to the stable on state regeneratively.

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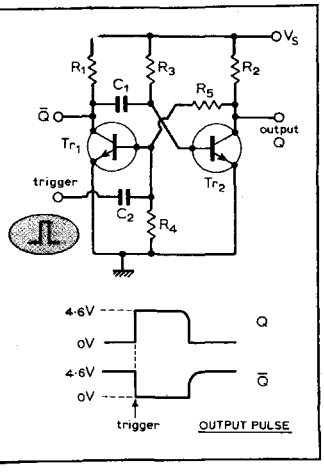
Basic discrete-component circuits



Typical performance

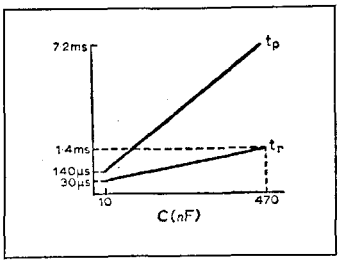
Tr_1, Tr_2: BC125
R_1, R_2: 1kΩ
R_3: 22kΩ
R_4: 4.7kΩ
R_5: 10kΩ
C_2: 100pF
V_S: 5V

Min. trigger pulse width 0.5μs
Trigger pulse height in range 1.4 to 3.6V

Output pulse width t_p depends on C_1R_3—see graph

Recovery time t_r depends on C_1R_1—see graph

Output pulse height 4.6V



Circuit description

In the quiescent state with the trigger at 0V, Tr_2 is held on due to base drive via R_3. Point Q is therefore at zero volts and hence Tr_1 is off, its base being at 0V. In receipt of the trigger pulse the base of Tr_1 is forced positive, Tr_1 conducts and its collector voltage drops. This is transmitted via C_1 to the base of Tr_2 and hence Tr_2 is forced off, raising its collector voltage. By potential division via R_5 and R_4, the base of Tr_1 is forced positive, thus forcing Tr_1 further into conduction. This positive feedback action forces a rapid change in state of both Tr_1 and Tr_2. C_1 then has one side at 0V, point $\bar{Q}$, and the other side connected via R_3 to V_S. It thus commences to charge towards V_S. This continues until the potential at the base of Tr_2 reaches a value which causes Tr_2 to start conducting. Point Q then starts to fall in potential causing the base of Tr_1 to fall. This causes $\bar{Q}$ to rise, forcing the base of Tr_2 even higher and rapidly the two transistors change back to the quiescent state. Length of the output pulse depends on C_1R_3. See graph.

The original quiescent state is not reached until C_1 has returned to its original uncharged state. The discharge path is via R_1 and the base-emitter junction of Tr_2. Discharge time is what accounts for the recovery time, t_r minus the minimum time after the output pulse trailing edge at which a further trigger pulse will give correct operation; see graph above.

Maximum trigger pulse height is fixed by the negative-going voltage applied to the base of Tr_1 on receipt of the trailing edge of the trigger pulse. If this is greater than the bias set by R_4 and R_5 then Tr_1 is switched off immediately and monostable action is prevented.

Minimum trigger pulse height depends on C_2 and on the pulse rise time.

Circuit modifications

- Both of the above restrictions on the trigger pulse height may be reduced by applying the trigger pulse as shown Fig. 1. If this arrangement is used the min. pulse height should be about 0.7V and the maximum should be the breakdown voltage of the triggering transistor.
- A general-purpose diode e.g. 1N914 should be inserted in the base line of Tr_2 as shown Fig. 2, if the supply voltage used is above 6V or so which is the base-emitter breakdown voltage of most planar transistors. If this is not done the linearity of t_p with respect to C is lost.
- If short recovery times are required between consecutive output pulses the circuit of Fig. 3 may be used. In the quiescent state both transistors are conducting, Q is low and $\bar{Q}$ is high. On receipt of the trigger pulse the p-n-p transistor (BC126) is switched off causing the base of the BC125 to fall in potential, thereby raising the voltage of Q and, via the 10kΩ resistor, the base of the BC126. The circuit thus latches into a condition where both transistors are off. Capacitor C_1 then charges via the 22k and 1kΩ resistors toward the supply and eventually turns the BC125 on and with it the BC126. Discharge of C_1 occurs more quickly in this case because the discharge path is through the collector-emitter junction of the BC126 and the base-emitter junction of the BC125. No external resistors are involved in this path as occurred previously. Hence, the circuit recovery time is considerably shorter.

Further reading

SGS Fairchild. Industrial Circuit Handbook 1967.
Hemingway, T. K., Electronic Designer's Handbook. Business Publications 1967.

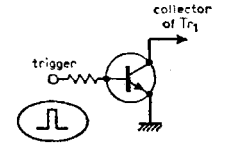


Fig. 1

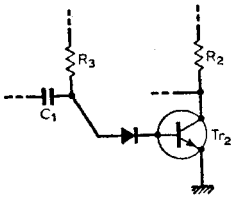
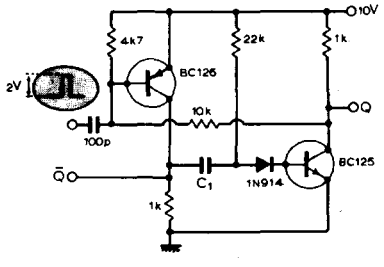


Fig. 2

Fig. 3



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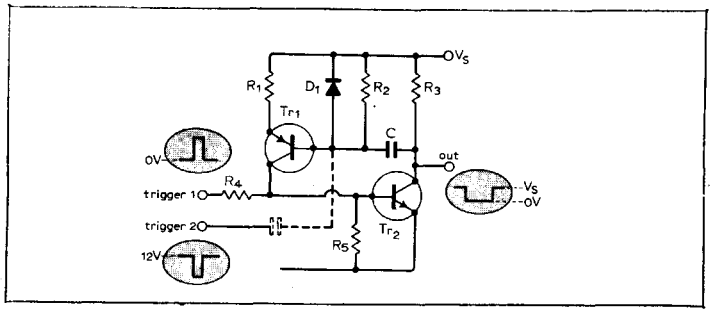
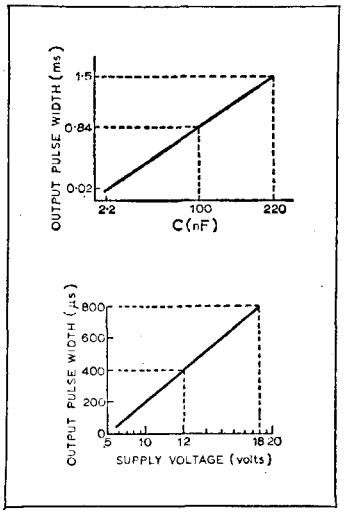
Complementary circuits



Typical performance
Tr_1: BC126, Tr_2: BC125
R_1, R_2: 33kΩ
R_3: 1.2kΩ, R_4, R_5: 10kΩ
D_1: 1N914
With V_s=12V, trigger frequency 500Hz, trigger pulse width and height 10μs and 2V respectively, graph opposite of output pulse width against C was obtained.
With C=47nF and pulse width of 10μs, minimum trigger pulse height about 1.3V.
With pulse height at 2V, minimum pulse width about 2μs.
Output pulse height about 12V; maximum mark-space ratio is 10: 1 at this frequency.



Circuit description
Monostable circuits using complementary transistors allow one to trigger either with respect to the positive supply line.
In the circuit shown both transistors are non-conducting in the quiescent state. On receipt of a positive-going pulse at trigger point 1, Tr_2 starts to conduct, dropping its collector voltage. This drop is transmitted via C to the base of Tr_1 and hence Tr_1 starts to conduct. This produces further base drive to Tr_2 and pushes it further into conduction. Very quickly both transistors are fully conducting and the output, initially at V_s drops to 0V approximately.
Capacitor C, uncharged in the quiescent state, then begins to charge towards V_s via R_2 and Tr_2. When it reaches $V_s - V_{be}$, Tr_1 is cut off, Tr_2 is cut off and the capacitor discharges via D_1 and R_3 principally. Insertion of D_1 provides a low resistance discharge path giving a fast recovery time.
When Tr_2 is cut off the output swings back to V_s so the output pulse period is determined by the charging time of the capacitor.
With the basic monostable circuit (card 1) the capacitor is, in the quiescent state, charged in one direction and this direction is reversed when triggered. Ignoring V_{be} effects, the capacitor during charging is going from $+V_s$ to $-V_s$ and the 0V or 50% point is sensed to bring the circuit back to quiescence. Because one is sensing a particular percentage of the attempted swing, the time taken is not supply voltage dependent. This is not the case here since a particular voltage is being sensed; the graph over shows the variation of pulse width with supply voltage. This could conceivably be used to produce a voltage-dependent monostable action.

Component changes
Increasing the pulse height allows a reduced pulse width (trigger pulse). Reducing R_1 to 4.7kΩ allows operation down to 6V and 0.1μs trigger pulse width. Value of R_2 is not critical; R_3 depends on Tr_2; R_4 and R_5 not critical.

Similar circuits
- The circuit of Fig. 1 will have zero stand-by power consumption but in this case has a positive-going output pulse. Again the output pulse width will depend on V_s, since in the quiescent state C is uncharged. In addition the V_{CEsat} of Tr_2 will affect the height of the pulse which should be $V_s - V_{CEsat}$. The 0V level should be well defined. In the circuit over the V_{CEsat} affects the 0V level but not the peak value (ref. 1).
- The circuit of Fig. 2 has a pulse width given by $t_p = 0.69(R_1 + R_3)C$ and a recovery time given by $t_r = R_3C/\beta$. As recharging current is supplied by Tr_1, this recovery time is short.
Pulse width is not supply dependent but since both transistors conduct in the quiescent state the standby power is large. Two outputs are available, at the collector of both transistors. They are the complement of one another (ref. 2).
- Diodes are frequently included in monostable circuits to prevent too large a reverse voltage being applied to the base-emitter junction of a non-conducting transistor (Fig. 3). A diode may be inserted in the emitter lead or in the base lead. The last-mentioned is generally preferred in that it will not affect the output pulse levels.

References
1 Electronic Circuit Design Handbook, Tab. p.174.
2 Electronic Circuit Design Handbook, Tab. p.85.

Cross references
Set 18, card 1
Set 10, card 4

Fig. 1

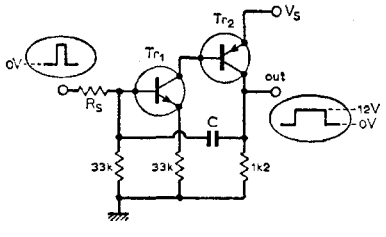


Fig. 2

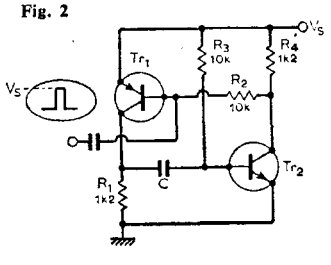
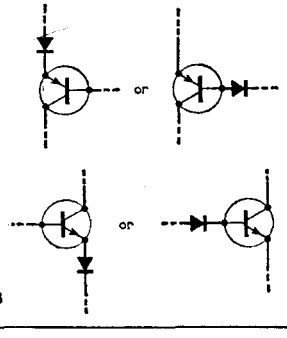
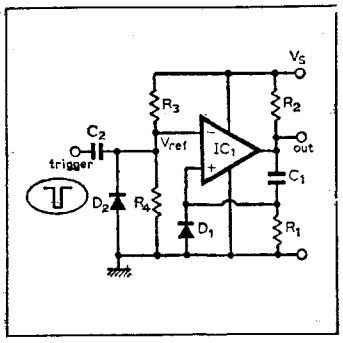


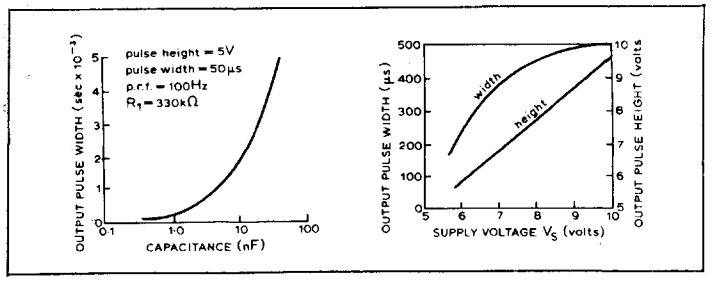
Fig. 3



Op-amp/comparator circuits



Typical performance
IC_1: ¼ LM139
V_s: +10V
C_1: 1nF
C_2: 470pF
R_1: 330kΩ
R_2: 10kΩ
R_3, R_4: 1MΩ
D_1, D_2: 1N914
Trigger pulse width: 30μs
Trigger pulse level: 6V
Output pulse width: 190μs
Output pulse level: 9V



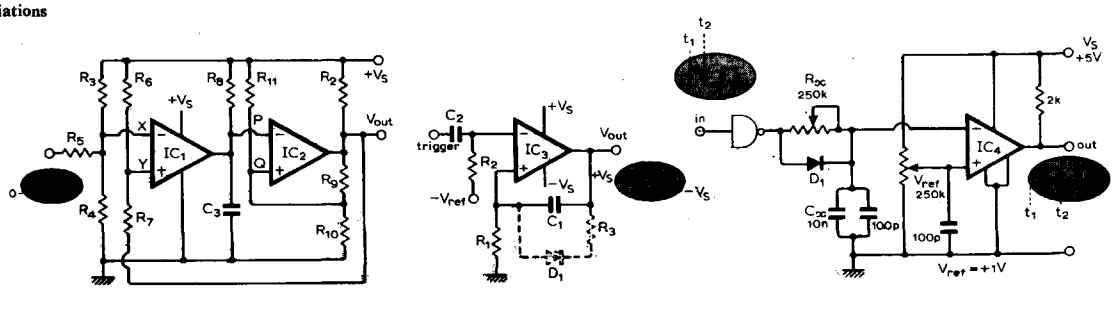
Circuit description
This comparator features an open-collector output, and may be used with pull-up resistor R_2 and a separate supply to give a wide switching range. Resistors R_3 and R_4 set the reference voltage equal to $V_s/2$, but also determine the trigger pulse level necessary for switching. Resistor R_1 should be much greater than R_2 to avoid loading the output. With $V_{ref} = V_s/2$ and the non-inverting input near 0V, the output transistor of the comparator is conducting and the output is at V_{CEsat}.
A negative trigger pulse at the input causes this transistor to switch off and hence the voltage at the output rises to almost V_s. Capacitor C_1 now charges at a rate mainly determined by R_1 and C_1, which also control the width of the output pulse. The potential of the non-inverting input now falls exponentially from V_s and the comparator switches to its original condition when the non-inverting comes below $V_s/2$. Diodes D_1 and D_2 prevent the inputs from being driven below zero volts, and D_1 also provides a low impedance discharge path for C_1.

Component changes
IC_1: ¼ × MC 3302P
Useful range of C_1: 220p to 22nF
Useful range of R_1: 47k to 470kΩ
Minimum trigger pulse width: 5μs
Minimum trigger pulse height: 5V(for $V_s = +10V$)
Range of V_s: up to 28V.
- Increasing trigger pulse height to 8V decreases pulse width by 150 to 200μs.
- Variation of pulse width with capacitance shown, for trigger pulse 5V.
- Output pulse is supply dependent, see graph above. (For C_1=1nF, R_1=330kΩ, p.w. is 50μs.)

Circuit variations
- Circuit shown left gives a pulse width that is supply independent, and is capable of a high duty cycle. Capacitor C_3 is initially charged to $+V_{cc}$ and V_{out} is at almost zero volts. Potentials at X and Y are defined by associated divider chains. A positive input trigger pulse to make $V_X > V_Y$ causes IC_1 to switch (output driven low). Capacitor C_3 rapidly discharges, and IC_2 will switch when the voltage across C_3 falls below V_Q, defined by R_{11}, R_{10}. Output voltage is now equal to V_{cc}, which is fed back bia R_7 to IC_1 which again switches to off condition. Hence C_3 now charges up via R_8. Output pulse width is defined by the time for the voltage across C_3 to just exceed that of point Q; IC_2 then reverts to its on, or low-output state. IC_1, IC_2 ¼ LM139, R_5, R_4 100kΩ, R_6 1MΩ, R_7 62kΩ, R_8, R_9 10MΩ, R_{10} 220kΩ, R_{11} 560kΩ, C_3 0.1nF.
Note that retriggering is not possible while IC_2 output is high—a useful lock-out feature.
- Circuit centre, using an op-amp, has a similar action to the comparator network. A negative reference voltage on the inverting input, with the non-inverting input tied to ground, gives a stable condition where $V_{out} = +V_s$. A positive input trigger sufficient to cause the differential input polarity to change, the output switches to $-V_s$. At this instant the potential of R_1 with respect to ground is $-2V_s$. As C_1 charges, the potential across R_1 rises towards $-V_{ref}$, when switching again occurs, and circuit resets to initial condition.
Component values: IC_3 MC1530/1531, C_2 23pF, R_2 100Ω, C_1 10nF, R_1 10kΩ, V_{ref} =2V. Pulse width typically 125μs. Diode and R_3 allow faster discharge of C_1, permitting an increase in p.r.f.
- Circuit right is a useful interface for delaying logic signals. When logic level is 1, capacitor charges quickly via diode, discharges via R_x when logic level is 0, allowing V_{out} to rise when $V_{Cx} \rightarrow +1V$. Using LM311, claimed delay is typically 0.04 to 370ms.

Cross reference
Set 17, card 8.

Circuit Variations



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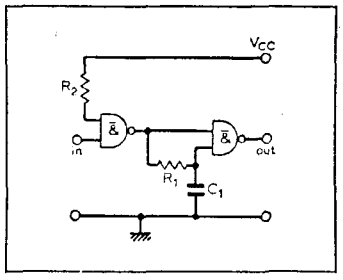
Monostable using t.t.l. gates



Typical performance
Logic gates: $\frac{1}{4} \times 7400$
Supplies: +5V; 8mA
R_1: 100Ω, R_2: 1kΩ, C_1: 1μF
Input pulses: amplitude +5V
Width: 50μs, p.r.f. about 10 kHz
Output pulse width about 74μs

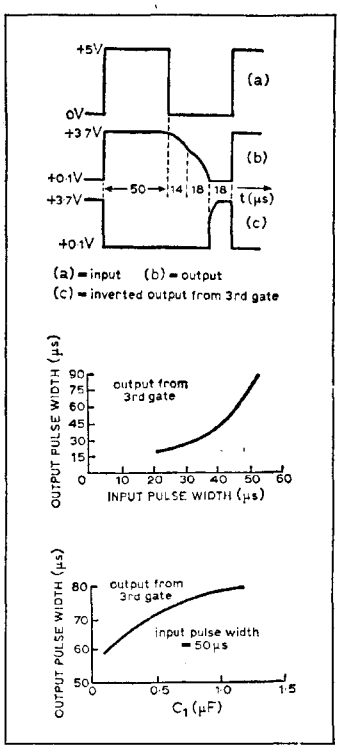
Circuit description
The circuit above uses two of the four NAND gates available in the integrated circuit package. Positive trigger pulses are applied to the first gate which is connected as an inverter, the unused input being taken to the positive supply rail (logic 1 state) via a 1-kΩ resistor to prevent the gate being damaged by a supply line transient. With the trigger input in the logic 0 state (0V), the output of the first gate is at 1, as are both the inputs to the second gate in the steady state, causing its output to be at logic 0. A positive trigger pulse causes the output of the first gate to go to its logic 0 level. One of the two inputs to the second gate immediately goes to the logic 0 level but its other input receives the voltage across C_1 which cannot change its charge instantaneously. The inputs to this gate are thus at logic 0 and 1 respectively, causing its output to switch to 1 where it remains until the trigger pulse returns to the 0-volt level. During this interval, capacitor C_1 discharges towards 0 volt through R_1 and the output impedance of the first gate and is recharged to the 1 level after the trigger pulse has returned to the 0-volt level.

Circuit changes
Useful range of V_{cc}: +4.5V to +5.5V
Maximum useful R_1: 470Ω
Maximum useful C_1: 1.5μF
Minimum trigger pulse amplitude: +3V
Minimum trigger pulse width: 40μs
Output pulse shape improved by cascading a third gate (see waveform and graphs above).

Cascading the fourth gate in the package provides a pair of complementary outputs.

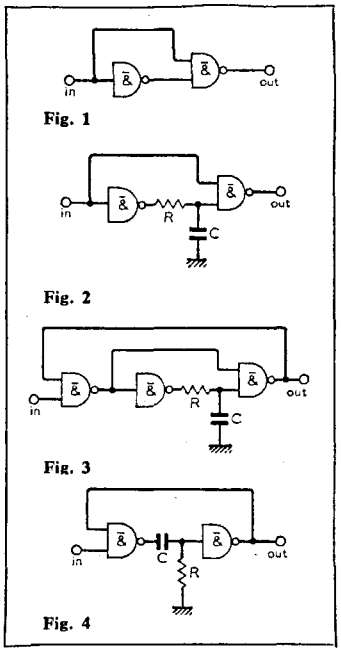
Circuit modifications
• The simple two-gate circuit shown in Fig. 1 has positive trigger pulses fed simultaneously to one input of each gate. These pulses appear at the output of the first gate inverted and delayed by the propagation time of the gate. Both of the inputs to the second gate are therefore at the 1 level for a short period, providing a narrow negative-going output pulse, delayed by the propagation time of one gate. This circuit has two defects: the output pulse is very narrow and non-adjustable and the trigger pulse must be wider than the output pulse.

• The circuit shown in Fig. 2 overcomes the first defect but still requires a trigger pulse wider than the output pulse. When the trigger input is at logic 0 the output of the first gate is at 1. Inputs to the second gate are at logic 0 and 1 since C is charged from the first gate, hence the output is at 1. When the trigger pulse goes to 1 the output of the second gate switches to the 0 state for an interval determined by the time constant, as C discharges through R, and the output impedance of the first gate. When C has discharged to a level where its voltage crosses the switching threshold of the 1 to 0 transition the output from the second gate switches back to its 1 level. Trigger pulse width must still be greater than the output pulse width, as the output of the second gate will always return to the 1 state whenever the trigger pulse returns to 0 volt.



• To overcome this problem the trigger pulses can be fed to the monstable via a third gate which has an output logic state determined by the monstable output, as shown in Fig. 3. Addition of this gate causes the monostable to be triggered when the input transition is from the 1 to the 0 state and the width of the input pulses is only that required to cause the input and output gates to change state. Since the same time constant controls the charge and discharge rates of C both circuits have relatively low maximum duty cycles, typically around 25%.

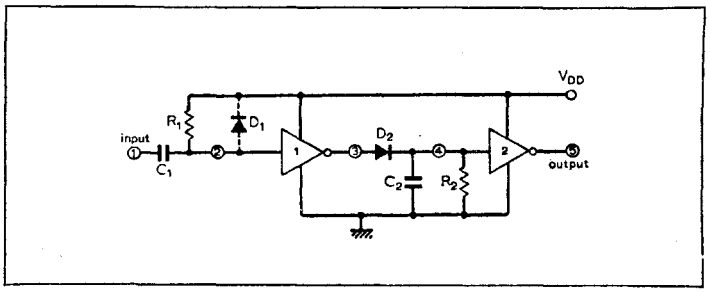
• Circuit of Fig. 4 uses only two gates but has a very similar mode of operation, the output pulses controlling the state of the input gate. This gate will normally have a 0 output since both its inputs will be at 1 until the trigger pulse goes to 0 volt. This causes the output to switch states for a time determined by that required for the CR network to cross the logic threshold.



Further reading
Malmstadt, H. V. and Enke, C. G., Digital Electronics for Scientists, Banjamin 1969, pp. 213-5.
Wilke, W., Operating a logic gate as a flip-flop, *Electronics*, 21 March 1974, pp.120/1.
Kaniel, A., Digital delay circuit for one-shot controls timing interval in programmable integer steps, *Electronic Design*, 18 Jan. 1974, p.94.

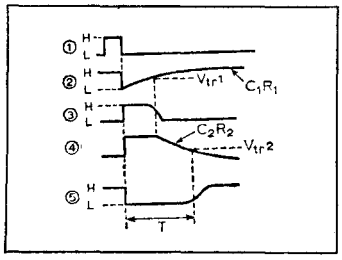
Cross reference
Set 11, card 3.

Compensated c.m.o.s. circuits



Components
D_2: general-purpose diode
Inverter 1 and 2:
$\frac{1}{3}$ × CD4007AE

Performance
$R_1C_1 = R_2C_2 = RC$
$T \approx 1.4RC$; tested in range
$10\mu s < T < 1ms$
With clock rate of 1kHz and pulse width 400μs, T remains within 4% of the nominal value over supply range 5V to 10V. With T of 330μs fall time is minimal but rise time is 120μs.



Circuit description
Complementary m.o.s. monostables using one time constant suffer from the fact that the transfer voltage (V_{tr}) of i.cs can vary by as much as ±33% so that replacement of an i.c. by another can result in a considerable change in the output pulse width. This defect can be removed by using two identical time constants with two inverters on the same chip. In this case the transfer voltage of both inverters is almost identical and the effect is cancellation of the variation in transfer voltage. This is taken advantage of in the circuit shown.
In the quiescent state with the input pulse low (ground), point 2 is high (V_{DD}), points 3, 4 and 5 are therefore low, low and high respectively. Capacitor C_1 is therefore in a charged state. On receipt of the input pulse this charge is removed rapidly via the source resistance and D_1 which is an internal protection device to prevent the input rising beyond V_{DD}. On the negative-going edge of the input pulse point 2 is taken down to ground and C_1 commences to charge towards V_{DD} via R_1. Point 3 will go high and remain in this state until C_1 passes through the transfer voltage of inverter 1. When point 3 goes low C_2 will commence to discharge via R_2, D_2 acting to prevent discharge into inverter 1. When point 4 passes through the transfer voltage of inverter 2 point 5 will go high and the operation is complete.
The graphs show that there are two possible outputs—at points 3 and 5. The output at point 5 is the only one in which there is compensation for transfer voltage variation. Due to lack of feedback in the circuit the risetime of the output is decidedly long (see performance data) but this is acceptable if the circuit is supplying further c.m.o.s. circuitry.
Despite the protection of D_1 the fact that the circuit is being fed via a capacitor makes it advisable to ensure that the input pulse height is close to V_{DD}. This can be done if the pulse is fed via further c.m.o.s. supplied from V_{DD}.
This circuit can be re-triggered, i.e. the output 5 can be maintained in its low state by feeding in a succession of pulses, provided each pulse occurs before point 2 reaches the transfer voltage of the first inverter.

Circuit modifications
- A positive-going output pulse, again triggered by the negative-going edge of the input is obtainable with the circuit shown top. In this case the output is obtained at the output of the first inverter viz point 3. This output is compensated, whereas that at 5 is not. Relevant waveforms are shown in Fig. 2. In this case re-triggering is not possible because any positive-going trigger pulse would reduce T_1 no matter the state of point 5.
- A negative-going pulse triggered on the positive-going edge of the input pulse is obtainable from the circuit shown in Fig. 3. For compensation, the output is taken from point 2 in this diagram. Relevant waveforms are as in Fig. 4. With this circuit re-triggering is also impossible because point 2 will stay low so long as point 5 is high, the trigger signal having no effect due to the normal NOR gate action.

Further reading
RCA applications note ICAN6267.
Murphy, C. Simple reconnection reduces rise time of CMOS delay circuit. *Electronic Design*, 4 Jan. 1974.

Fig. 1

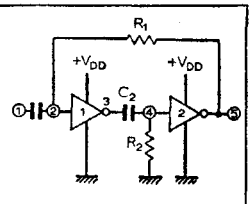


Fig. 2

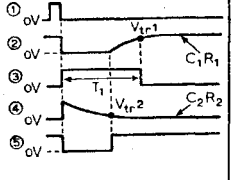


Fig. 3

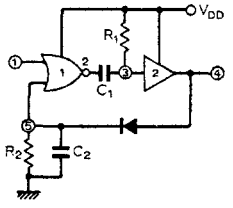
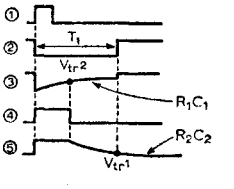
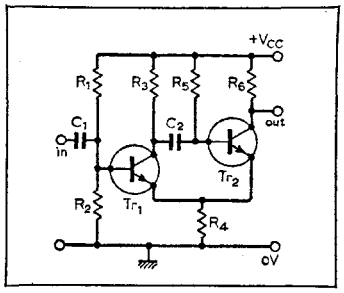


Fig. 4

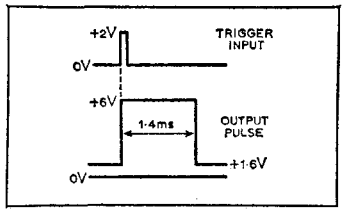


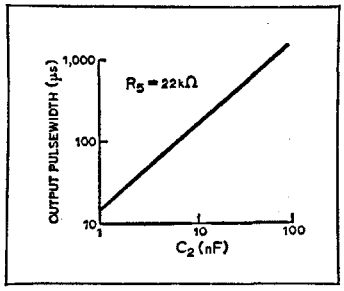
Emitter-coupled circuits



Typical performance
Supply: +6V, 4mA
Tr_1, Tr_2: BC125
R_1: 6.8kΩ
R_2: 1.8kΩ
R_3: 2.7kΩ, R_4: 330Ω
R_5: 22kΩ, R_6: 1kΩ
C_1: 100pF, C_2: 100nF
Input pulse amplitude: +2V
Input pulse width: 1μs
p.r.f.: 1kHz

Output pulse—see waveform below





Circuit description
In the stable state Tr_2 is on and saturated due to the base drive via R_5. The emitter current of Tr_2 causes the common emitter voltage to be at approximately 1.5V. Thus Tr_1 is held off by the R_1, R_2 potential divider which maintains its base at about 1.3V, slightly reverse-biasing the base-emitter junction. Output voltage at Tr_2 collector is at approximately 1.6V in this stable state. The C_1, R_1, R_2 network differentiates the input trigger pulses and, if these have a positive-going transition large enough to exceed the emitter voltage by V_{BE}, Tr_1 will switch on and saturate. The collector voltage of Tr_1 falls by about 4.5V and this negative-going transition passes to Tr_2 base through C_2 so this transistor switches off. Output voltage rises to +Vcc and Tr_2 remains in the off state while C_2 charges via R_5, Tr_1 and R_4. As C_2 charges, the base voltage of Tr_2 rises exponentially towards +Vcc but when it exceeds the emitter voltage, Tr_2 rapidly turns on and saturates. Current in R_4 increases, producing a corresponding rise in the emitter voltage which reverse-biases the base-emitter junction of Tr_1, which switches off, and the circuit returns to its stable state.

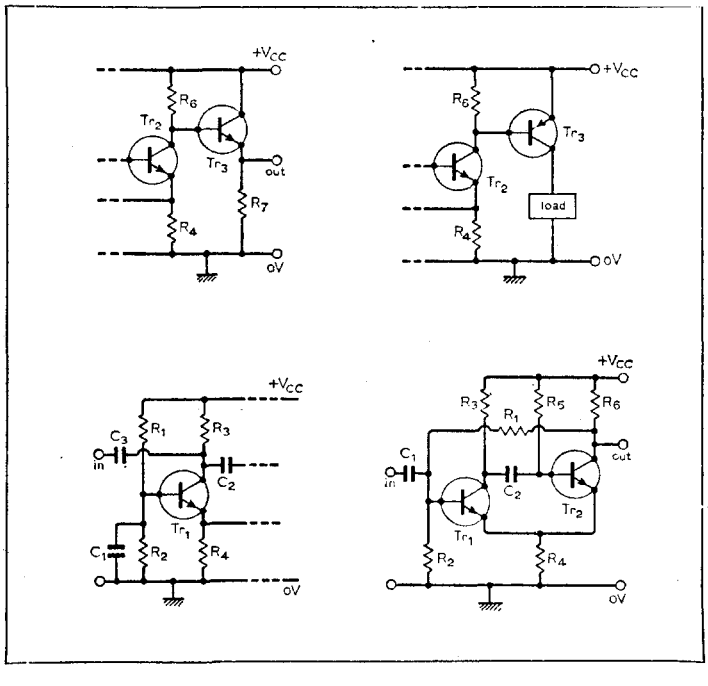
Circuit changes
Minimum trigger pulse width 0.5μs. Output pulse width could be varied by R_5 but this would also change the d.c. conditions. Larger supply voltages may be used but then a silicon diode should be included in series with Tr_2 base to prevent reverse breakdown of its base-emitter junction by the switch-off transient.

Circuit modifications
- Adding an emitter-follower to the original circuit, as shown in the top left diagram, allows the output pulses to be obtained from a low-impedance source and to be referred to ground. By adjustment of the supply voltage these pulses may be made compatible with t.t.l. logic circuitry.

- A p-n-p common-emitter stage may be added, as shown top right, to use the output pulses for driving a ground-connected load. For example, the load could be in the form of a filament lamp for alarm or monitoring purposes and as collector currents of at least 50mA may be obtained, the load could be a relay coil to provide control of some other circuitry. The inductive load provided by the relay coil should be shunted with a protective diode.

- The original circuit may be modified to be triggered by negative-going pulses as shown in the circuit shown bottom left. In this arrangement the trigger pulses are applied to the collector of Tr_1 via the small coupling capacitor C_3. The negative-going trigger pulse edge is passed to Tr_2 base through C_2 switching this transistor off. Tr_1 turns on and the remaining cycle of operations are as described previously. The circuit will function with C_1 omitted but the transition to the quasi-stable state will be more rapid when it is included in the circuit.

- In all of the circuits discussed the output point was isolated from any internal coupling. If, see bottom right, R_1 of the original circuit is taken to Tr_2 collector instead of the +Vcc rail this is no longer the case and changes in emitter voltage may be very small.
The simplest way to provide faster switching is to prevent Tr_1 and Tr_2 from saturating by increasing R_4.



Further reading
SGS-Fairchild, Industrial Circuit Handbook, 1967, pp.51/2.
Budinsky, J., Techniques of Transistor Switching Circuits, Iliffe 1968, pp.486-91.

Cross references
Set 18, cards 1 and 7.

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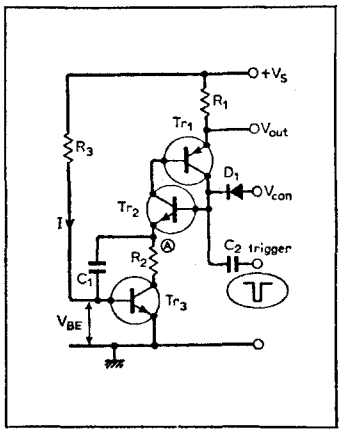
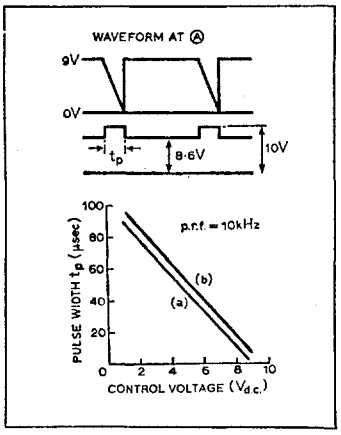
Voltage-controlled monostables



Typical performance
Tr_1: BC126
Tr_2, Tr_3: BC125
R_1: 22Ω, R_2: 1.2kΩ
R_3: 10kΩ
C_1: 1nF, C_2: 100pF
$+V_S$: +10V
D_1: 1N914
Trigger pulse magnitude: −13V
Trigger pulse width: 0.1μs
$V_{control}$: 8V
Output pulse duration: 7μs
Waveforms and timing graph shown opposite, curve (a)



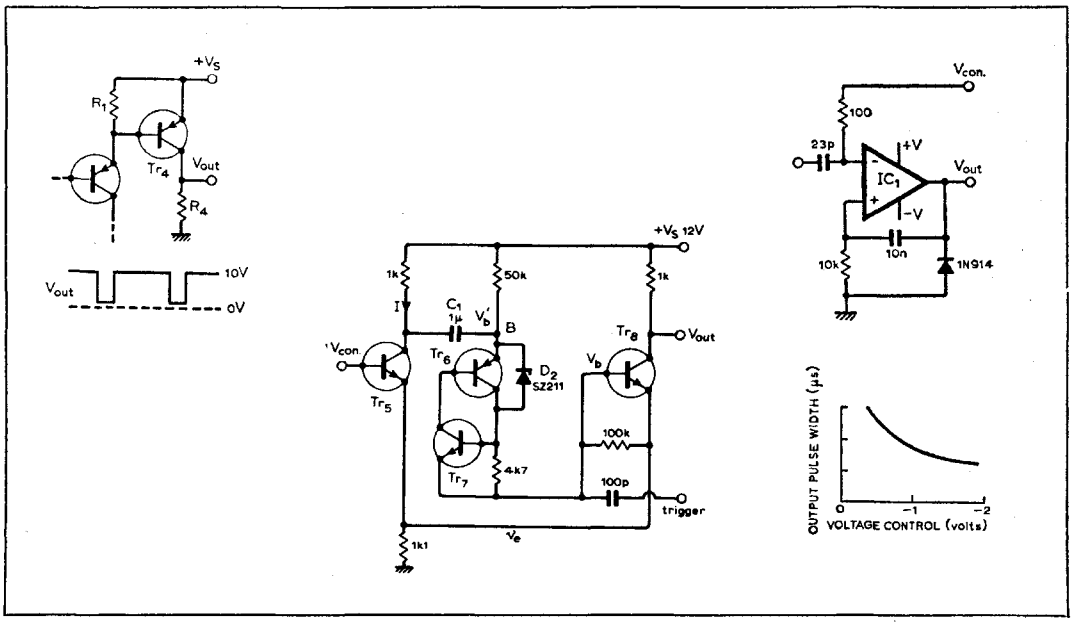
Circuit description
Transistors Tr_1, Tr_2 form a complementary-pair positive feedback switch, and are either both off or both on. In the rest state, this switch is closed, Tr_3 is on, D_1 is non-conducting, and C_1 is charged. A negative trigger pulse applied at the trigger terminal causes the regenerative switch (Tr_1, Tr_2) to open. Collector current of Tr_3 is now αI, where α is common base current gain and $I=(V_S-V_{BE})/R_3$. Hence C_1 discharges at a constant rate giving a run-down linear sweep at point A. This sweep continues until the potential of point A is less than $V_{control}-V_{D1}-V_{BE(Tr2)}$, when the complementary switch again conducts. The switch also acts as a comparator, besides providing a low impedance path for recharging capacitor C_1.
Notice that the sweep termination depends on the level of the control voltage, which therefore controls the width of the output pulse.

Component changes
Tr_2, Tr_3: BSX28, Tr_1: BSX29
Useful range of C_1: 1 to 47nF
Useful range of R_3: 10k to 100kΩ
Useful range of control voltage is in the range 10% to 90% of $+V_S$.
To minimize inductive and stray capacitive effects, this circuit was constructed on a p.c.b. to obtain above measurements.
Rise and fall times of output pulses less than 0.5μs.
Control voltage may be obtained from potential divider connected across supply.

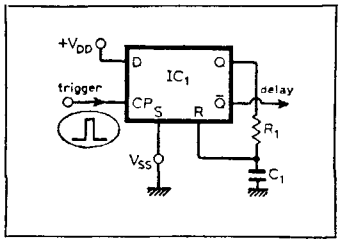
Circuit modifications
- Connect additional buffer stage Tr_4 (BC126) and R_4 (390Ω) for increased output pulse amplitude (below). Trigger pulse amplitude is 7V, when coupling capacitor C_2 increased to 1nF; provides timing graph shown above a (b).
- Circuit (centre) is basically an emitter-coupled monostable circuit. Time duration may be extended by the inclusion of a complementary pair (Tr_6, Tr_7) with breakdown fixed by zener diode D_2. This effectively increases the cut-in voltage, V_b, of Tr_8. Tr_8 is normally on. Trigger pulses cause Tr_5 to conduct (Tr_8 off), and circuit returns to its stable state when the voltage at B brings the regenerative switch into conduction. Pulse duration depends on I, which is controlled by voltage applied to base of transistor Tr_5. Output pulse duration typically in the range 40 to 200ms for a control voltage of 3 to 6V.
- Operational amplifier IC_1 (MC1530/MC1531), shown right, can provide variable delays by controlling the voltage at the inverting input. Diode clamps the negative amplitude of the output to about −0.7V. Positive output will approach +V.

Further reading
Rakovich, B. D. & Djurdjevich, B. Z., Wide-range voltage-to-time converter, *IEEE Transactions* vol. IM-22, no. 2, June 1973, p.162.
Time delay circuit for SCR control, *Electronic Eng.* June 1974, p.14.
Motorola application note AN-258.

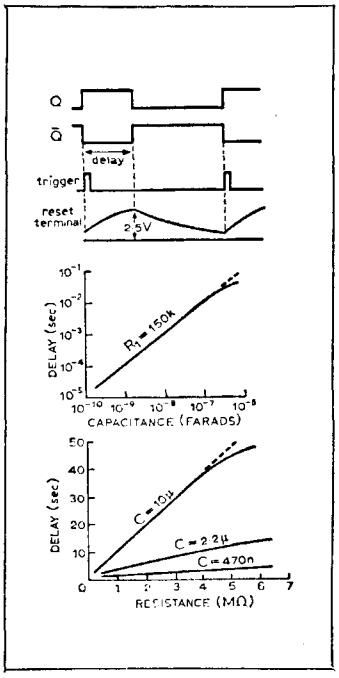
Cross references
Set 18, card 3, 6.



Long-delay circuits using c.m.o.s. and unijunction devices



Typical performance
IC_1: ½ × CD 4013AE
V_{DD}: +5V, V_{SS}: 0V
R_1: 470kΩ, C_1: 10μF
Trigger pulse width: 1μs
Trigger pulse height: 4V
Delay: 9s
Typical waveforms and delays shown opposite.



Circuit description
The high input impedance of c.m.o.s. integrated circuits offers a low leakage path for capacitor C_1, and thus allows a wide range of delays from this D-type flip-flop configuration. The D-input is permanently connected to the positive supply rail, hence Q goes high when a positive trigger pulse is applied at the clock input. A positive voltage approximately 50% ($V_{DD}-V_{SS}$) at terminal R will reset Q to its initial condition of 0V.
On the occurrence of a trigger pulse, the reset threshold will be reached in a time defined by C_1 and R_1, which in turn defines the delay available at Q̄. This circuit is fairly insensitive to supply voltage change, because the threshold level for reset will alter pro-rata. However it should be noted that this level is not well defined, and hence the accuracy of time delays will depend on specific measurement with the components used.
Unused inputs should be tied down to ground.

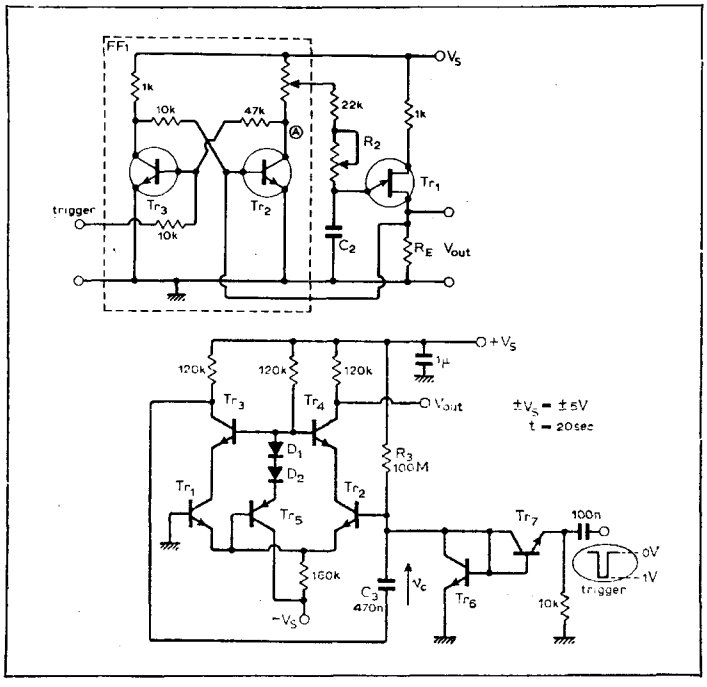
Component changes
Useful range of R_1: 100k to 10MΩ
Useful range of C_1: 47pF to 32μF
(For long time delays, low-leakage capacitors must be used)
Supply voltage range: ($V_{DD}-V_{SS}$) 3 to 15V
Minimum pulse width: 0.1μs
Minimum pulse height: 2 to 4V
Alternative IC: MM74C74

UJT transistor monostable
The circuit shown right (top). employs a discrete transistor flip-flop, with the timing controlled by the firing of the unijunction transistor Tr_1.

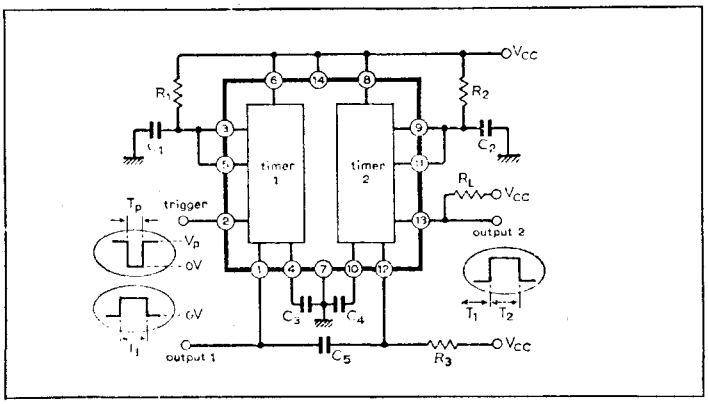
The normal rest condition of bistable FF1 is Tr_3 off and Tr_2 conducting. Hence the available voltage at point A is approximately V_{CEsat} of Tr_2. This is much less than the firing voltage V_P of the unijunction transistor which therefore is non-conducting, and the output voltage is at zero volts.
A positive pulse applied at the trigger input brings Tr_3 into conduction, and due to positive feedback Tr_2 is rapidly switched off. Hence the potential of point A rises. Voltage across C_2 now rises exponentially toward +Vs. When it reaches V_P in a time determined by R_2C_2, Tr_1 will conduct and discharge C_2 via the emitter and the resistor R_E. The output pulse developed across R_E is applied to the base of Tr_2 to turn it on again and hence reset the bistable, and turn off Tr_1. Well-defined output pulses are also available at the collectors of Tr_2 and Tr_3.
R_2 1MΩ, C_2 1μF, R_E 27Ω, Tr_1 2N4853, Tr_2/Tr_3 2N4123, Vs + 10 to +30V.
An advantage is that the initial voltage across C_2 is always the same at the start of a period no matter the pulse repetition frequency. It is claimed that with the supply voltage variation noted above, pulse duration changes are 2%.
● Circuit (bottom) uses the transistor array CA3095E. Diodes D_1, D_2 and Tr_5 act as a voltage-limiting network. Quiescent condition is with transistors Tr_1 and Tr_3 off, Tr_2 and Tr_4 on. A negative-going pulse at the trigger-input terminal is coupled to the base of Tr_2 via diode-connected transistor Tr_7. Hence Tr_2 (and Tr_4) cut off and V_{out} rises to +Vs. Because Tr_2 and Tr_1 are emitter-coupled, Tr_1 can now conduct when Tr_2 is off, therefore the voltage across C_3 i.e. V_L is near ground. Capacitor C_3 now charges via R_3. When the base potential of Tr_2 is high enough to bring it into conduction, Tr_1 again goes off and V_{out} drops to its normal value of about 1.8V.
Time duration is $t \approx 0.47R_3C_3$.

Cross references
Set 18, cards 5, 9.

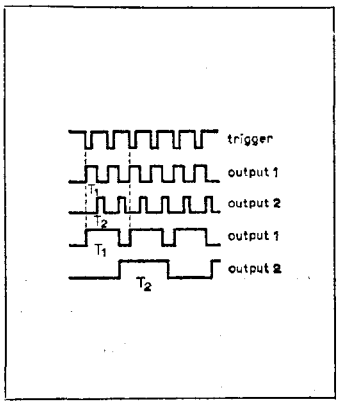
Further reading
Unijunction Transistor Timers and Oscillators. Motorola application note AN-294.



Dual monostable applications using 555 timer



Typical performance
V_{CC}: 10V (range 4.5 to 16V)
Output pulse height: 9.3 to 9.9V
C_3, C_4: 10nF
C_5: 1nF
R_L: 470Ω
R_3: 33kΩ
T_1: $1.1R_1C_1$
T_2: $1.1R_2C_2$
V_P: V_{CC}
IC: XR2556

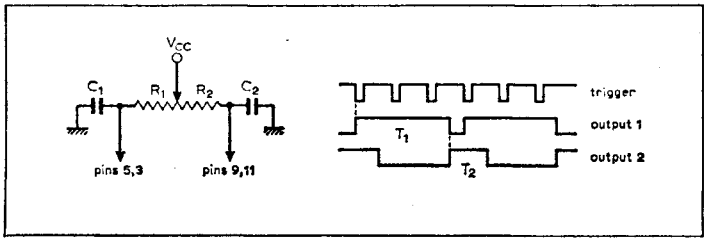


Circuit description
The i.c. shown is a dual 555-type timer (internal details of which are shown in cross references 1 and 2). In this application the output of the first timer is capacitively coupled via C_5 to the input of the second. Both timers are triggered when the input to each drops below $\frac{1}{3}V_{CC}$. In this case the trigger pulse operates timer 1 and the output of timer 1 triggers timer 2. Both timers are connected in their monostable mode. Formulae for T_1 and T_2 quoted are valid for all conditions and are fixed entirely by the external R_1, C_1 and R_1, C_2. Any succeeding trigger pulses are ignored. Both T_1 and T_2 can be anywhere in the range 10μs to 100s with two provisos: T_1 cannot be reduced below T_p, but since T_p can be less than 3μs this is not serious. Secondly low values of T_1 and T_2 should not be obtained by reducing R_1 and R_2 to a level at which current drain from the supply is serious. A minimum value of 1kΩ is recommended for both R_1 and R_2.
The only restriction on R_L is that it must not be so low as to exceed the current rating (200mA) of the i.c.
Typical waveforms are shown above. These are suitable for sequential timing circuits. Note that trigger pulses occurring during the period set by R_1, C_1 and R_2, C_2 are ignored.

Circuit modifications
- Obviously the i.c. may be used as two separate timers or monostables by omitting C_5 and R_3 and by applying the trigger pulses directly to pins 2 and 12.
- Referring to the main diagram, control over the total period (T_1+T_2) can be achieved by connecting the arm of a potentiometer to Vcc and the ends to pins 3 and 9, R_1 and R_2 being now the two segments of the potentiometer shown above. If $C_1=C_2=C$ then $(T_1+T_2)=C(R_1+R_2)$ which is constant no matter the individual T_1 and T_2.
- Each individual timer can be regarded as a frequency divider in its own right. For example, in the waveforms shown over, the lower two graphs indicate that output 1 is running at half the trigger pulse frequency and output 2 is running at half the frequency of output 1. By correct choice of T_1 one can make output 1 run at any submultiple frequency of the trigger and likewise with correct choice of T_2 output 2 can run at any submultiple frequency of output 1.
- A combined frequency divider and pulse width controller can be achieved by setting T_1 so that it is greater than the trigger period and by ensuring that $T_2 < T_1$. The value of T_1 sets the frequency division and the value of T_2 sets the pulse width, the output being output 2. Furthermore, the "phase" of the output with respect to the trigger can be controlled since, for example, frequency division by 3 allows T_1 to lie anywhere between two and three trigger periods. See waveforms above.

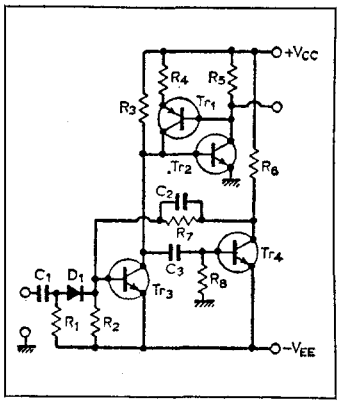
Further reading
XR-2556 Dual Timing Circuit, data sheet/application note, Exar Integrated Systems Inc.

Cross references
Set 3, card 9
Set 13, cards 3 and 5

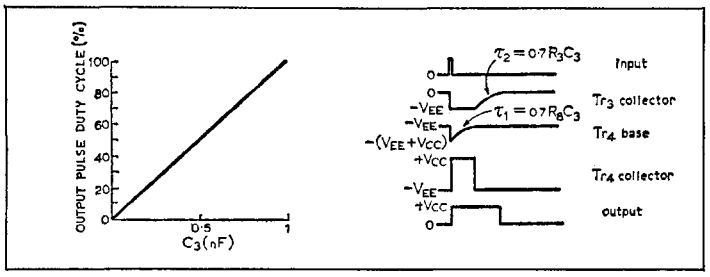


wireless world circard

High duty-cycle monostable



Typical performance
V_{CC}: +6V, 6 to 18mA*, V_{EE} −6V, 6 to 12mA*
Tr_1: BC126, Tr_2, Tr_3, Tr_4 BC125
R_1: 10kΩ, R_2, R_7: 56kΩ
R_3, R_8: 47kΩ, R_4: 1.8kΩ
R_5, R_6: 1.2kΩ, C_1, C_2: 100pF
C_3: see graph opposite; D_1 PS101
Input: 4V positive pulses, pulse width 1μs, p.r.f. about 10kHz
Output rise time: 0.5μs
Output fall time: 0.2μs
*depending on value of C_3.



Circuit description
In this circuit the timing capacitor C_3 not only determines the width of the output pulse obtained from Tr_2 collector but also delays the setting-up of the circuit in readiness for the next cycle of operations. This prevents an early trigger pulse from producing an output pulse having too short a duration. Because the circuit may be re-triggered immediately after completing its cycle, an output-pulse duty cycle approaching 100% may be obtained. The conventional "cross-coupled" monostable allows only about 95% duty cycle, even when its timing capacitor is rapidly recharged from a low-resistance source. In the stable state, Tr_3 is biased off and Tr_1, Tr_2 and Tr_4 are on. Input trigger pulses are differentiated by C_1 R_1, the positive component passing to Tr_3 base via D_1. If of sufficient amplitude, these overcome the reverse bias on Tr_3, which switches on, Tr_1, Tr_2 and Tr_4 switching off. Transistor Tr_4 remains off for approximately $0.7\tau_1$ as its base potential rises under the control of C_3. When Tr_4 turns on again, Tr_3 collector potential rises as C_3 recharges with time constant $\tau_2 = C_3 R_3$ until it exceeds approximately 0 V. Transistor Tr_2 and hence Tr_1 then switch on regeneratively and the circuit returns to its stable state and may be re-triggered immediately.

Component changes
Minimum useful supplies ±2 V
Useful range of R_1: 1k to 100kΩ
Useful range of R_2: 1k to 470kΩ
Minimum trigger pulse amplitude approximately 2.5 V
Minimum trigger pulse width less than about 0.1μs
Maximum useful p.r.f.: 200kHz.

Circuit modification
● The circuit shown top is a logical representation of a high duty-cycle monostable which may be realised with logic gates or discrete transistor circuitry. A pair of pulse-steering AND gates and a flip-flop used as a toggle cause the positive-going input trigger pulses to be alternately applied to the pair of monostables (M). The monostable outputs are combined in the OR gate to provide the output pulse and to toggle the flip-flop which changes state when the output pulse is completed. Hence, the start of the next output is only delayed by the time taken for the flip-flop to change its state, which can be a small percentage of the output pulse duration. A discrete version produced 700ms pulses every 705ms.

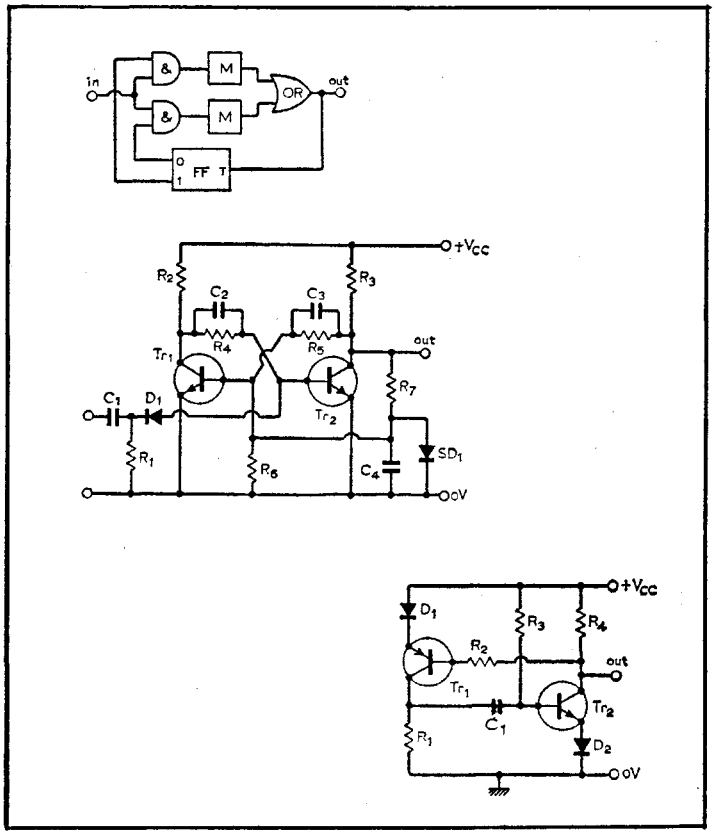
● Circuit shown next uses a flip-flop in conjunction with a Shockley diode (SD1) to achieve a high duty cycle. An input pulse causes the flip-flop to change its state producing an exponential voltage rise across C_4. When this voltage reaches a critical value the diode breaks down rapidly discharging C_4 and producing a negative pulse to reset the flip-flop via C_3 in readiness for the next input pulse. Pulses of 2μs duration may be produced after only a 250ns recovery time.

Typically, R_1, R_6 1MΩ, R_2, R_3 10kΩ, R_4, R_5 150kΩ, R_7, 2.2MΩ, C_1, C_2, C_3 20pF, C_4 500nF, D_1 1N914, SD1 4E20-8, with V_{CC} +25V.

● Circuit shown bottom can provide a recovery time of only 1% of its period and may be triggered by positive pulses at Tr_1 base or negative pulses at Tr_2 base causing both transistors to switch from their on to off states. Transistor Tr_1 can recharge C_1 with a large collector current to rapidly regain its initial voltage. Diode D_1 and D_2 may be omitted if Tr_1 and Tr_2 have a large reverse V_{BE} rating.

Further reading
Shagena, J. L. & Mall, A. Single-shot multivibrator has zero recovery time, *Electronics*, 27 Nov., 1967, p. 83.
Electronic Circuit Design Handbook, 4th edition, Tab, 1971, pp. 85, 96, 342/3.

Cross reference
Set 19, card 9.



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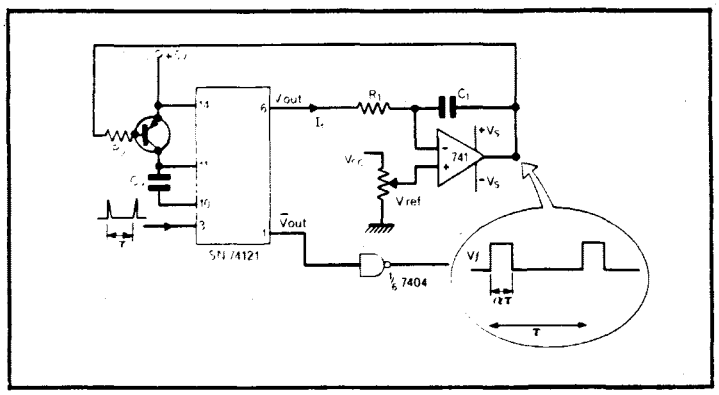
Set 19: Monostable circuits Up-date

Disadvantages of monostables in digital circuits caused by their sensitivity to noise on the output line or transients in the power supply are avoided by using integrated-circuit monostables such as the SN74121. Two applications are considered.

1. The normal timing resistor for the monostable connected between pins 14 and 11 is replaced by the impedance of a transistor. The input trigger pulses to pin 3 provide predetermined pulse width at the output of the monostable depending on C_2 and the effective resistance provided by the transistor which is changed by the feedback loop to maintain the duty cycle. The output pulse defines the time for which



current I_1 flows into C_1. For V_{out} high,

$$I_1=\frac{V_{outH}-V_{ref}}{R_1}.$$

For V_{out} low

$$I_1=\frac{V_{outL}-V_{ref}}{R_1}.$$

Average current in R_1 is

$$I_{av}=\left(\frac{V_{outH}-V_{ref}}{R_1}\right)\alpha\tau+\left(\frac{V_{outL}-V_{ref}}{R_1}\right)(1-\alpha)\tau.$$

In steady-state operation, the average current to the capacitor is zero, when α has reached the correct value. The above expression for I_{av} is then zero and

$$\alpha=\frac{V_{ref}-V_{outL}}{(V_{outH}-V_{outL})}.$$

To avoid loading the monostable output and thus possibly varying V_{outH} and V_{outL}, an alternative output is taken from pin 1 via an inverter. Variable base drive due to V_f can cause the transistor impedance to vary between 500Ω and 500kΩ, allowing a pulse repetition frequency range of the order of 1000:1.

Reference

Langon, H. P. D. *Electronics*, July 24, 1975, p. 93.

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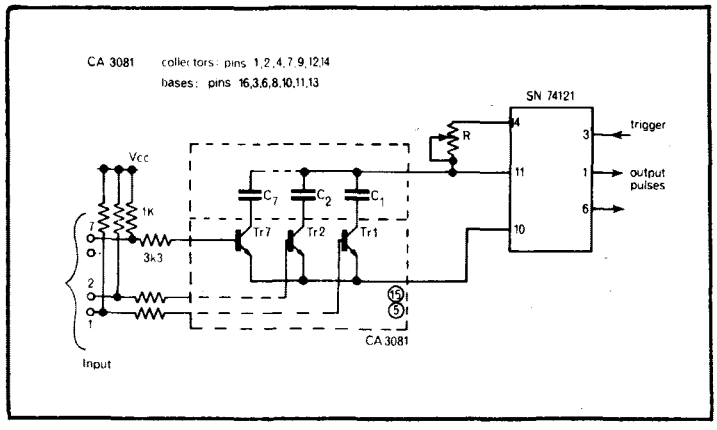
2. Integrated-circuit CA3081 contains seven n-p-n transistors with the emitters commoned. The control of pulse width from the integrated-circuit monostable is achieved by the R-C combination across pins 14, 11, 10. Hence by driving the base of one of the transistors Tr_1 to Tr_7, a different capacitor is switched across pins 10, 11. The absolute value of capacitor depends on which of the input terminals are taken high or low respectively, and this may be



controlled sequentially, as in the specific application of the reference, using a read-only memory package. It is suggested that temperature compensation for the pulse width might be achieved by including a thermistor as part of the tuning resistor network R.

Reference

Pulford, I. P. & Risk, R. J. Applied Ideas: *Electronic Engineering*, Sept. 1974.

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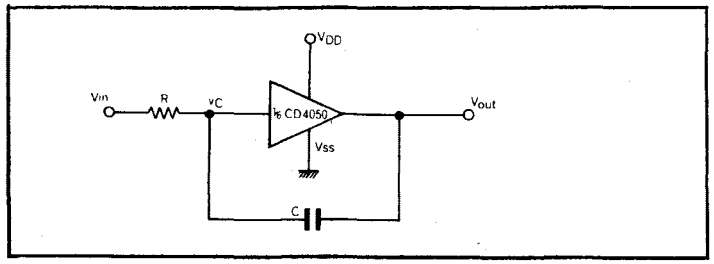
3. The input impedance of c.m.o.s. gates is very high and therefore provide a useful means of obtaining long delays with relatively small capacitance values. This circuit provides a means of eliminating the slow rise of capacitor voltage, when it is normally connected between gate-input and the V_{SS} rail. When V_C reaches the lower threshold value, then V_{out} begins to go positive. As the charge on the capacitor cannot change instantaneously, V_C follows the output at a rate determined only by the c.m.o.s. gate. A similar regenerative effect will occur on a negative transition.

Reference

Electronic Design 1, January 4, 1974.



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Set 20: Transistor pairs

Tweedledum's query seems an especially appropriate way of starting the following article on transistor pairs. Not only are the advantages of each configuration not always clear, but sometimes it's difficult to see the true operational nature of the configuration. In the cards, 20 different connections of two transistors are described, excluding c.m.o.s. circuits and triple or mixed pair arrangements. This set of circuits is an important one in that many form the basic building bricks of integrated circuits—long-tailed pairs, current mirrors, and even cascode circuits and high-gain pairs. Both the article and card 4 discuss the merits of the different long-tailed pair configurations, the card giving useful formulae for gain, common-mode rejection and temperature drift. Cards 1 & 2 contain a thorough investigation of the properties of high current gain pairs—Darlington, complementary Darlington and four-terminal pairs—the results being given in the 16 graphs, all of course derived from the compiler's measurements. Various circuits can be developed by mixing various pairs and two examples are given on card 9. One uses a long-tailed pair with constant-current tail feeding a current mirror to produce a triangular-wave generator; the other is an operational amplifier using bipolar and m.o.s. devices with a single supply.

The complementary transistor switch of card 6 is the transistor equivalent of unijunction and thyristor switches, but has the advantage of being faster than either as high-speed transistors can be used. Other cards show how the current capability of a c.m.o.s. inverter can be simply increased (card 8); how a cascode circuit is re-arranged to avoid the need for a biasing voltage (card 3); and card 5 gives performance and descriptions of m.o.s. and bipolar current mirrors—now an integral part of operational amplifiers.

Transistor pairs

"Supplementary or complementary, opposites or composites?" asked Tweedledum. "Contrariwise", said Tweedledee. It is not the intention to rewrite "Alice . . .", but it is not always clear what the advantages are in d.c.-coupled pair configurations—voltage gain plus impedance change, super current-gains, p-n-p simulation, thermal compensation or perhaps a current source as a stabilizing network.

The *pièce de resistance* might be the long-tailed pair or differential amplifier (where would the linear i.c. be without it?) which provides some satisfying amplifying properties—some possible variations for small-signal operation are shown in Fig. 1. For example, the connection shown in Fig. 1(a) converts a signal difference between two inputs to equal, but antiphase collector signals. Signals common to both inputs (e.g. superposed noise signals from the same source) are reduced without affecting the differential gain, which is that due to a single transistor.

The ability of this amplifier to prevent amplification of a common signal is called the common-mode rejection ratio, being the ratio of the differential voltage gain to the common mode gain, usually expressed in dB. The single-ended inputs of Fig. 1(b) and (e) produce an output at Tr_2 collector, equivalent to Tr_1 as an emitter-follower driving Tr_2 as a common-base amplifier. In addition, the output of Tr_1 is equal in magnitude but antiphase to that of Tr_2, on the assumption of constant total current (long-tail). Hence the differential output in Fig. 1(b) is twice the single-ended output. The voltage gains are approximately R/h_{ib} and $R/2h_{ib}$ for Fig. 1(b) and (e) respectively, where h_{ib} is the effective input resistance of the common base configuration. Fig. 1(c) and (f) are not used as amplifiers, but are useful as a means of determining the gain to common mode signals. This should be much less than unity to give good rejection.

The common-emitter, common-base, connection shown in Fig. 2(a) is the cascode amplifier, where the first stage transistor Tr_1 has current gain, and the second stage Tr_2 has voltage gain. The advantages are a large gain-bandwidth product and also, for high voltage outputs, the high breakdown value of the common base transistor Tr_2 is essential.

The common collector-common collector pair of Fig. 2(b) is the familiar Darlington connection, where the effective current would be approximately β^2, if the transistors were identical. This would be true for short-circuit outputs, but a practical value for the β of each transistor

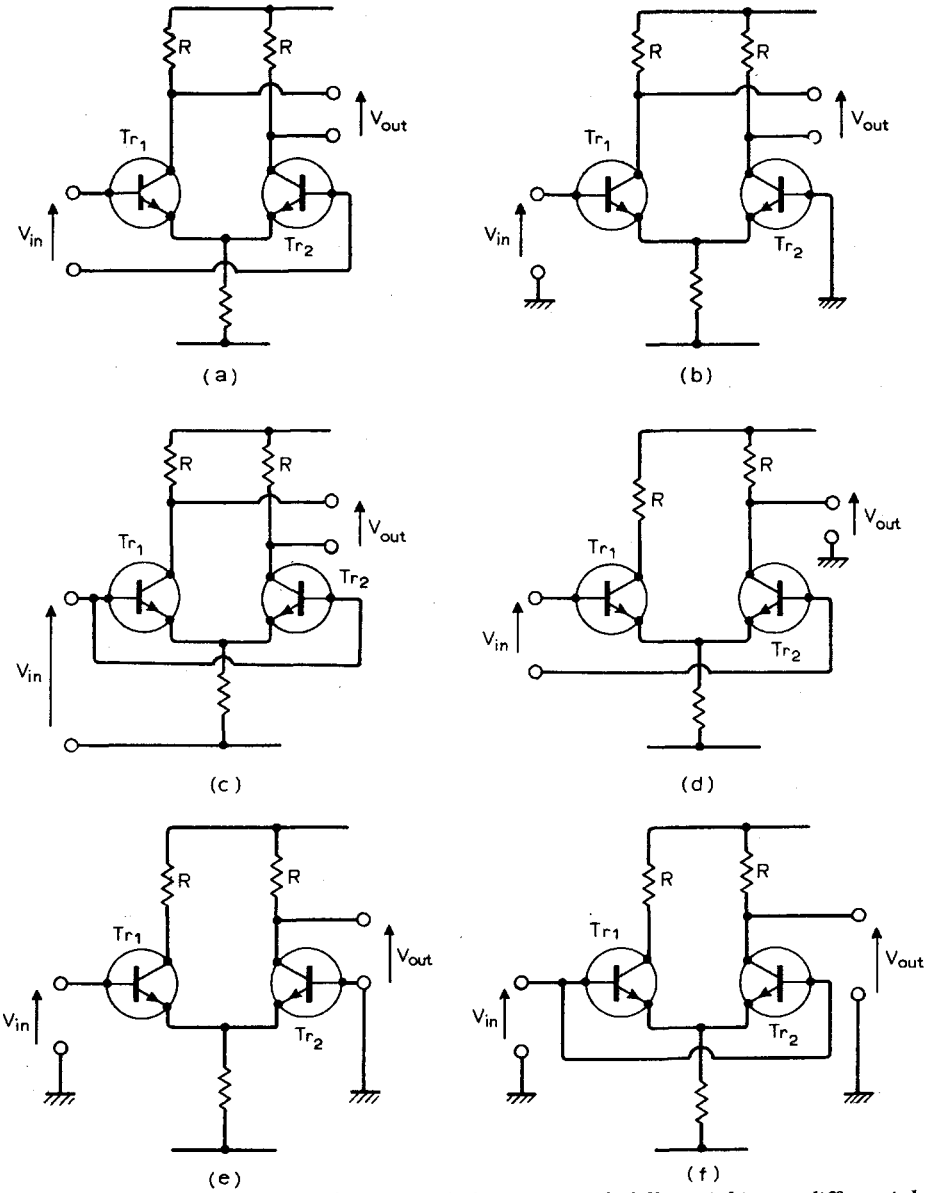


Fig. 1. Variations of the long-tailed pair include circuits with differential input, differential output (a), single-input, differential output (b) & (c), differential input, single output (d), and single input and output (e) & (f).

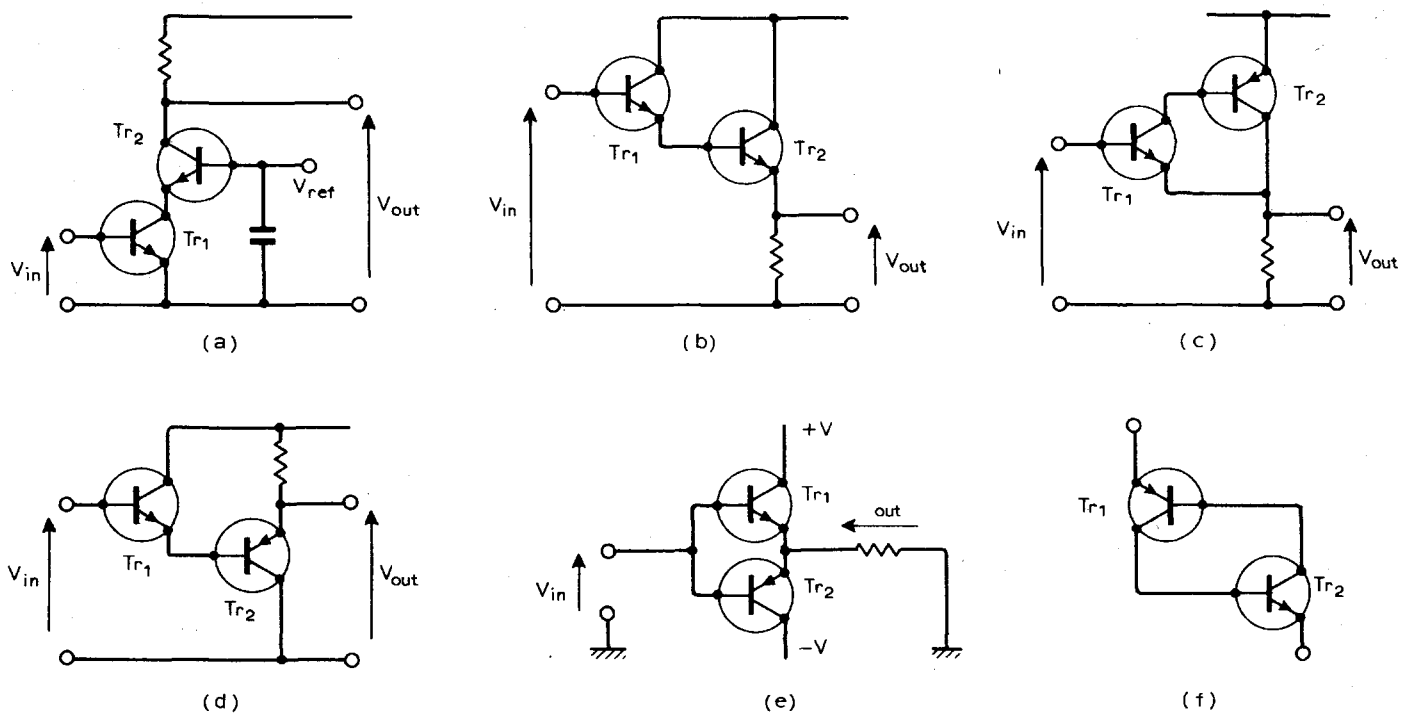


Fig. 2. Other ways of connecting two transistors are common-emitter, common-base i.e. cascode (a), common-collector pair i.e. Darlington (b), complementary pair with only one V_{be} drop (c), complementary pair with no V_{be} drop (d), symmetrical complementary pair i.e. class B amplifier (e), and the regenerative pair (f).

would be to specify the minimum value quoted by a manufacturer (assuming that discrete transistors are being discussed, because it must be remembered that super-β packages are also available with defined current gains). The complementary connection of Fig. 2(c) provides only one V_{be} drop compared with Fig. 2(b), and that of (d) cancels the V_{be} drops, but offers some second-order residual offset between input and output, and requires a separate bias path (not shown) for Tr_1 emitter current and Tr_2 base current. Complementary versions may provide an advantage, in that the transistor choice for the first stage can be that with the highest current gain at low currents.

When opposite types of transistors are connected in complementary form, such as Fig. 2(e), we have the basis of a class-B amplifier. The circuit for each half-cycle of signal is essentially identical, and the load is driven from a low-impedance source, because each transistor acts as an emitter follower. An advantage is that interstage and output transformers are not necessary when such a circuit is used at audio frequencies.

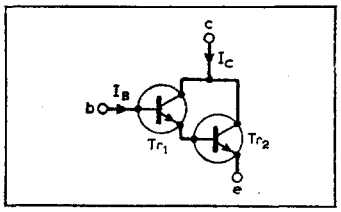
The interconnection of n-p-n and p-n-p transistors as in Fig. 2(f) provides a regenerative switching action due to the positive feedback between collectors and bases. It is similar in operation to a unijunction transistor, and there are of course similarities with the thyristor. Switching speeds can be faster than a single unijunction device because high-frequency transistors can be employed. The same arrangement is the basis for a constant-current circuit (Circards set 6, card 5), while those sources which may be classed as current controlled tend to use the current-mirror—no self-respecting operational amplifier would be without one!

The complementary-symmetry m.o.s. pair has been an excellent addition to the pair family. Besides being the basis of several logic gates, it also has application in multivibrators and as a linear amplifier.

A close study of most linear integrated-circuits will reveal the use of two or more of the pairs mentioned, to provide a composite arrangement which offers advantages that no single transistor or pair can do.

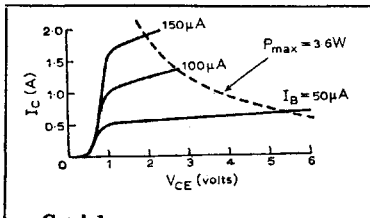
High current-gain pairs—1

Darlington pair

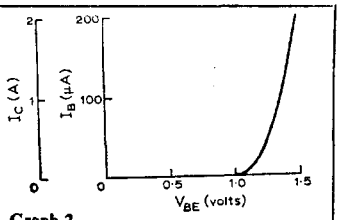


Components
Tr_1: BFR41 Tr_2: TIP3055

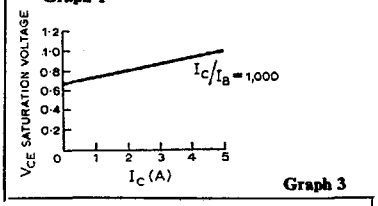
Description and characteristics
A Darlington pair as shown above is a frequently used two-transistor circuit, the purpose being to obtain high gain through cascading two transistors. Because large currents are obtained in the second transistor one frequently finds this to be a power transistor and that the arrangement is used in many switching applications.
As the circuit has only three terminals it can be regarded as a single high-gain transistor. The basic action is that I_b produces, through Tr_1, a large base drive for Tr_2. The total I_c is the sum of the two collector currents although the contribution of Tr_1 to I_c will be small if the gain of Tr_2 is large.
The characteristics obtained for the components quoted are as shown. From graph 1 we obtained an h_{oe} of about 25mS and an h_{fe} of about 11,000. Graph 2 shows an h_{fe} of around 70. These figures are in line with theory (see reference). Graph 2 also shows the dependence of I_c on I_b, the two graphs being indistinguishable because of the scales chosen.
For switching applications the value of V_{CE} is important. V_{CE}sat is defined as that V_{CE} corresponding to an arbitrarily low I_c/I_b ratio, in this case 1,000 (graph 3). With higher I_c/I_b ratios, corresponding to lower I_B values the value of V_{CE} will be lower. The corresponding graph of V_{BE}sat. is shown in graph 4.
Graph 5 shows the dependence of h_{FE} on I_c, the drop in h_{FE} at high I_c being due to saturation and that at low I_c being due to lack of base drive to Tr_1.



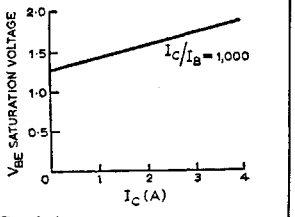
Graph 1



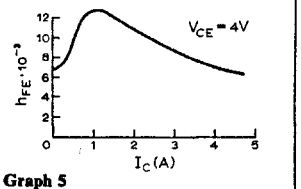
Graph 2



Graph 3

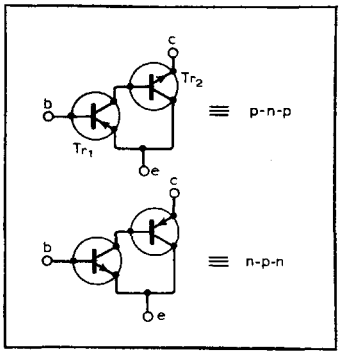


Graph 4



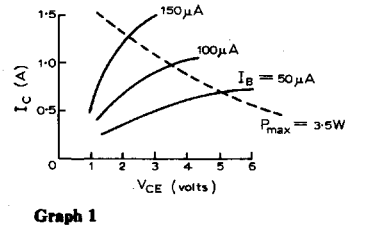
Graph 5

Complementary Darlington pair

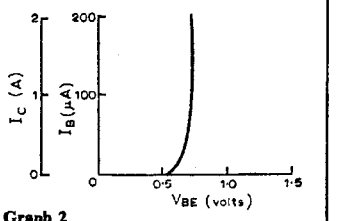


Components
Tr_1: BFR81
Tr_2: TIP3055

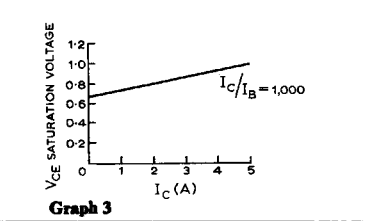
Description and characteristics
The basic action of this circuit is the same as that of the normal Darlington pair. Note that the circuit in this format is acting as a single p-n-p transistor. An n-p-n version is shown below. It is the input transistor which indicates whether the combination is p-n-p or n-p-n but one can readily check the bias voltages.
Graph 1 shows the output characteristics: not eminently suitable for a small-signal amplifier, but as the circuit tends to be used for switching applications this is not too serious. We obtained for these components an h_{fe} of 8,500 approx and an h_{oe} of greater than 0.1S.
Graph 2 shows I_B and I_c against V_{BE} and these again coincide because of the scale chosen. Note in this case that V_{BE} during conduction is about 0.7V as opposed to 1.5V for the normal Darlington; this is due to the fact that there is only one junction between b and e. This shows up again in graph 4.
By the same token, the graph of V_{CE}sat (graph 3) is much the same as that for the normal Darlington.
Graph 5 again has much the same shape as that for the normal Darlington though with a lower maximum value, which is in line with the reduced h_{FE}.



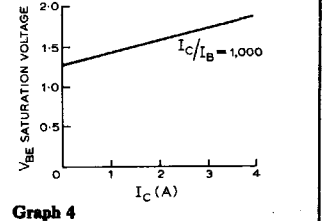
Graph 1



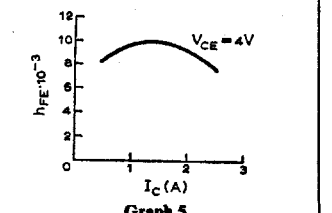
Graph 2



Graph 3



Graph 4

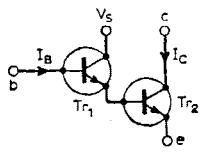


Graph 5

Further reading
Burwen, E. High-gain triple Darlington has low saturation voltage, *Electronics*, 3 Oct., 1974.

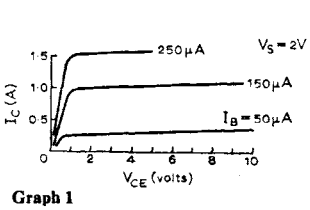
Reference
Ajdler, J. Transistor circuits, *Electronic Engineering* 1965, p.757. See also p.338 and p.112, same year.

High current-gain pairs—2

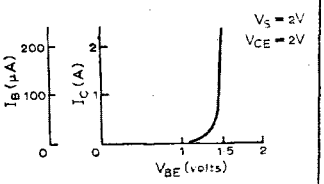


Components
Tr_1: BFR41
Tr_2: TIP3055

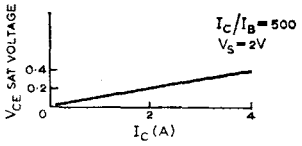
Performance and description
The Darlington circuits on card 1 are both super β circuits but have the additional charactistic that they only have three terminals and so can be regarded as a single transistor. The circuit shown above also has high gain but has four terminals, three of which can be regarded as base, emitter and collector, the fourth being connected to a voltage which gives some control over the characteristics. The principal difference in performance of this circuit is that a low saturation voltage is obtained. From graph 1 we obtained an h_{fe} of 7,000 and an h_{oe} of 25mS for V_s=2.0V. Characteristics for V_s=4.0V are virtually identical.
Graph 3 shows the low V_{ce}sat values obtained, slightly lower values being obtained for V_s=4.0V.
Graph 4 shows the expected V_{BE}sat values around 1.5V since two base-emitter junctions are between b and e. Again slightly lower values are obtained for V_s=4.0V. The graph of h_{FE} is shown in graph 5, the figures being in line with the previously obtained h_{fe}. Note that in this configuration Tr_1 will have supply voltage V_s across it and will normally require a current-limiting resistor in its collector lead.



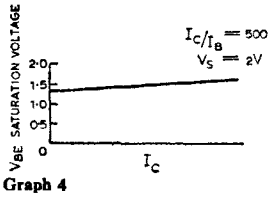
Graph 1



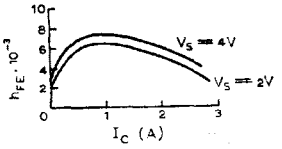
Graph 2



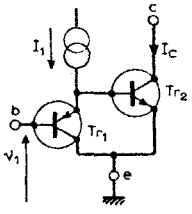
Graph 3

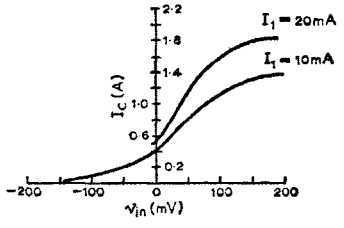


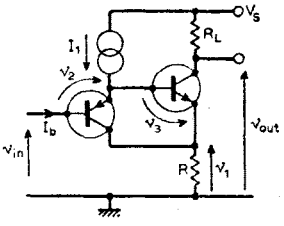
Graph 4



Graph 5







Components
Tr_1: BFR81
Tr_2: TIP3055

Circuit description
First given by Baxandall and Shallow, this circuit has a gain producing action similar to that of the Darlington's and the circuit overleaf. Base current to Tr_1 produces large base drive to Tr_2 thereby giving large gain. In this case, however, bias (I_1) must be provided for correct action. As there are more than three terminals it cannot be considered as identical to a single transistor, and it displays some characteristics that one does not obtain with single transistors. In particular, one obtains collector current I_c in the absence of any V_1, this being due to the action of I_1. The characteristics shown were obtained with a V_{CE} of 1V and exhibit an overall gm of 6A/V, obtained at V_1 of zero.
The components used were chosen for comparison with the other super β pairs but certain features would dictate other choices. For example, the circuit simulates a p-n-p transistor whilst having an n-p-n output stage. In monolithic i.cs with lateral transistors, n-p-n transistors have low gain so that Tr_1 would dictate the overall gain. As Tr_1 has a very low voltage across it, viz V_{be} of Tr_2, then Tr_1 can be made to have high gain—see MC1538R.
When used as shown above right, the circuit exhibits extremely high output resistance which, allied to the high current gain, gives large voltage gain. The reason for this is that $v_1 = v_3 + v_2 + v_{in}$ and as v_3 and v_2 cancel, both being base-emitter voltages, then $v_1 = v_{in}$ and the current in R_L is thus defined by I_1 and the current in R, no matter the value of R_L.
The circuit therefore, must have a large output resistance. Values as high as 50MΩ have been quoted.

Further reading
Baxandall, P. J. and Shallow, E. W. Constant-current source with unusually high internal resistance and good temperature stability; *Electronics Letters* vol. 2, p.351 1966.
Jarger, R. C. A high output resistance source, *IEEE Journal of Solid-State Circuits*, Aug. 1974, pp.192-4.

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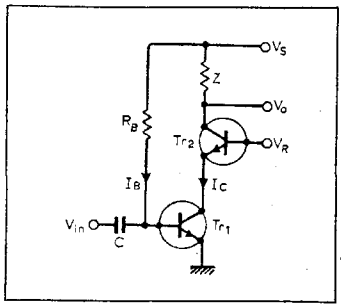
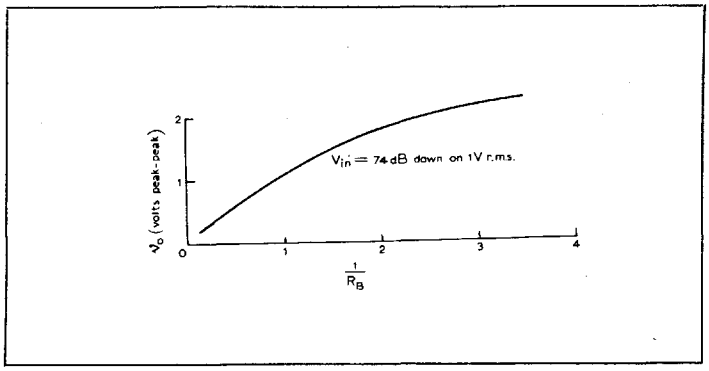
Cascode amplifier



Components
Tr_1, Tr_2: BFR41
V_S: 10V
Z: 660mH coil plus stray capacitance plus c.r.o. loading
C: coupling capacitor
R_B: see graph
V_o: see graph

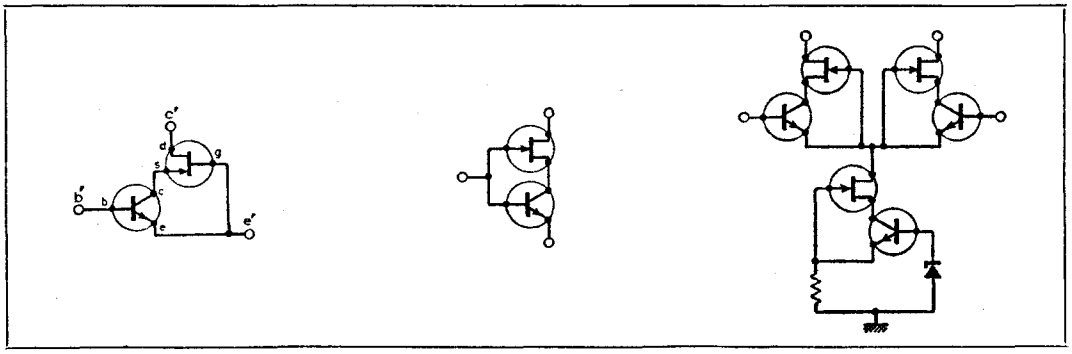


Circuit description
Tr_1 is a common-emitter amplifier which is feeding Tr_2 in common-base mode. The load on Tr_1 is therefore a near short-circuit a.c.-wise. In addition, the current gain of Tr_2 is near unity but its output impedance is high, due to the common-base mode of operation. The combination therefore shows the gain characteristics of a short-circuited c.e. stage plus the output impedance characteristics of c.b. It is therefore ideally suited for the driving of tuned resonant loads or indeed of any high impedance load.

The basic equations are
$I_c = g_m V_{in}$
$I_c \approx I_L$
$g_m = I_c/26\text{mV}$
$V_o = Z_L I_L$

The second equation assumes unity current gain through Tr_2 and the last equation assumes that h_{ob} (for Tr_2) is very low. The net result is
$V_o/V_{in} = g_m Z_L$
Since I_c is almost linearly related to I_B, particularly if V_{CE} of Tr_1 is constant which it is in this case, then g_m is controllable by R_B. The net result is the graph shown. For each result the circuit was retuned for resonance, the change in resonant frequency being around 1.5% over the complete range.
With $R_B = 1M\Omega$, the resonant frequency was 924kHz and the bandwidth 18.5kHz giving a Q of 50. V_R is not critical—it is only required to produce correct transistor action. In these results it was 3V. A 1.5-nF supply decoupling capacitor was necessary.
Note that the graph represents a range of voltage gain from 50dB to 71dB and that the range of R_B is 20:1.
The circuit above has two disadvantages viz, it is not a three-terminal device and also requires a biasing voltage. The above circuit suffers from neither of these disadvantages. The circuit is self-biasing provided only that I_c is less than I_d by an amount sufficient that the resulting V_{gs} keeps the bipolar transistor well out of saturation. Typically V_{ce} would need to be in the range 0.2 to 1.0V (though a higher value would be preferable for higher gain). This means that the operating current is restricted to the I_d of the f.e.t. with V_{gs} in the range of −0.2 to −1.0V. In practice the current is defined by some other requirement (drift, matching etc) and is often much less than I_{dss}—the f.e.t. current with $V_{gs} = 0$ (which would give no gain from the bipolar anyway). The f.e.t. will frequently be required to operate near pinch-off.
The circuit, above centre, is a less common form which loses the merit of low capacitive feedback. It does, however, have the merit of increased current capability since the f.e.t. can operate with $V_{gs} = 0$V.
The circuit right is of a form found as the input of some commercially available differential amplifiers. Each two-transistor block can be regarded as a single transistor and the circuit is then recognisable as a long-tailed pair. The tail uses the high output impedance of the pair to provide an excellent constant-current source the other two pairs being used for their high voltage gain.

Cross references
Set 20, cards 4, 10.



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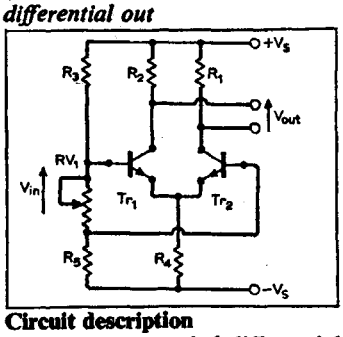
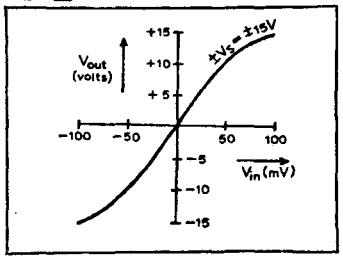
Long-tailed pair

(a) Differential in–differential out



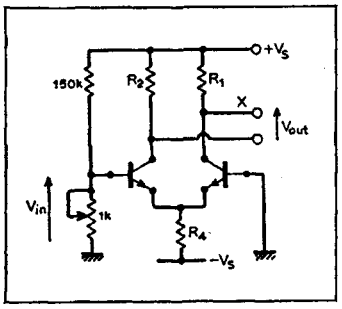
Circuit description
This emitter-coupled differential amplifier should have a large value for R_4 to provide a high common-mode rejection ratio (c.m.r.r.). This implies that the differential output voltage between collectors for a common signal at the bases, is very small and ideally zero. In general, the output signal depends on the difference between the signals at the transistor bases. Each transistor receives half the signal i.e. the gain to each output is half of that provided by a single transistor under the same conditions.

Performance data
Tr_1, Tr_2: matched pair from CA3086. R_1, R_2, R_4: 100kΩ.
R_3, R_5: 150kΩ, RV_1: 1kΩ
V_S: ±15V



Gain slope: typically 230.
Variation in gain: ±1% for several choices of CA3086.
Reducing R_1, R_2 by similar ratios will maintain slope at same order of magnitude.

(b) Single-ended in, differential out



V_{in}: 10mV d.c. (20mV)
V_{out}: 2.39V d.c. (4.79V)
i.e. gain slope similar to (a)

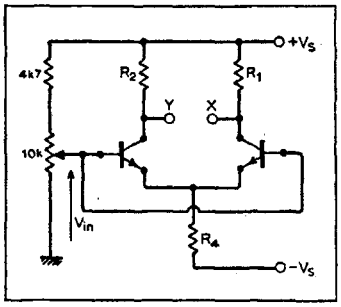
$$\frac{\Delta V_{out}}{\Delta V_{in}}=240$$

For single-ended output:
V_{out}=voltage between X and ground.

$$\frac{\Delta V_{out}}{\Delta V_{in}}=\frac{10.28V-9.06V}{20mV-10mV}=122.$$

i.e. gain is halved.

(c) Common mode input



$$\frac{\Delta V_{xy}}{\Delta V_{in}}=\frac{0.149-0.142}{2-1}=0.007$$

For single-ended output (terminal X to ground):

$$\frac{\Delta V_{out}}{\Delta V_{in}}=0.0045$$

c.m.r.r. improved by trimming R_1, R_2 for zero balance.
Figure of merit is c.m.r.r. or voltage gain for differential inputs divided by voltage gain for common-mode inputs that is 0.007/230.

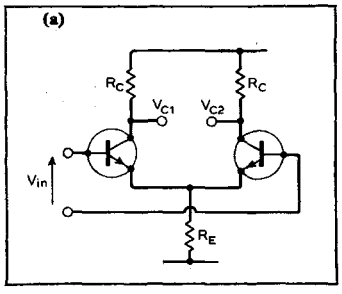
Useful relationships
Bipolar transistor collector current related to base-emitter voltage by

$$I_C \approx I_S \exp qV_{BE}/kT$$

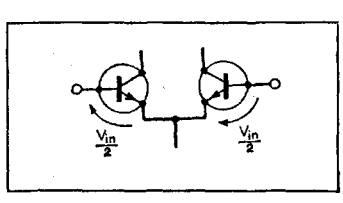
$$\frac{dI_C}{dV_{BE}}=\frac{qI_C}{kT}=g_m$$

At room temperature

$$g_m \approx \frac{I_C}{26}(\text{mA/V})$$



Differential input signal can be considered as



$$v_{C1}=-g_m\frac{v_{in}}{2}R_C$$

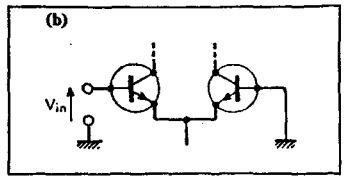
$$v_{C2}=-g_m\frac{-v_{in}}{2}R_C$$

Differential output given by

$$v_o=v_{C1}-v_{C2}$$
$$=-g_m v_{in}R_C.$$

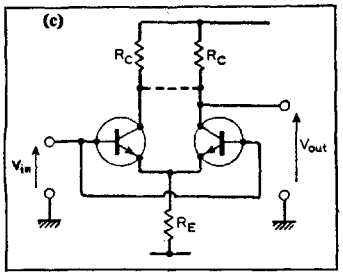
Voltage gain A_V

$$=v_o/v_{in}=-g_mR_C$$
$$=I_CR_C/26=-V_C/26.$$



This single-ended input signal can be considered as the algebraic sum of differential and common-mode signals:
i.e. $v_{in}=v_{in}/2+v_{in}/2$
and $0=\underbrace{v_{in}/2}_{\text{common mode}}-\underbrace{v_{in}/2}_{\text{differential mode}}$

If c.m.r.r. high, effect of common-mode signals negligible. Hence single-ended input equivalent to differential input.



For identical transistors the collectors are at equal potentials for common-mode signals. Hence they can be considered connected together

$$v_{out}\approx\frac{-v_{in}}{R_E}\cdot\frac{R_C}{2}$$

Note: If R_E replaced by a constant-current circuit, v_{out}(cm) can be $\ll 1$.

$$\text{c.m.r.r.}=\frac{-g_m\,.\,R_C}{R_C/2R_E}$$
$$=\frac{-g_mR_E}{2}$$

Temperature drift
For a pair of identical transistors, balanced to provide zero difference between the base-emitter voltages of each, then the temperature drift is theoretically zero—a basic advantage of the differential mode.

$$V_{BE}\approx\frac{kT}{q}\log\left(\frac{I_c}{AT^r}\right)$$

A is dependent on transistor area. Two transistors on same chip, but different areas, provides a V_{BE} variation given by

$$\Delta V_{BE}=\frac{kT}{q}\log\left(\frac{A_2}{A_1}\right)$$

Temperature drift is

$$\frac{d\Delta V_{BE}}{dt}=\frac{k}{q}\log\left(\frac{A_2}{A_1}\right)=\frac{\Delta V_{BE}}{T}$$

At room temperature (300K) drift is 3.3μV/deg C for each mV of initial offset.

Further reading
Thermal variation of the emitter-base voltage of bipolar transistors. Widlar, R. J. *Proc. IEEE* Jan. 1967.
Limits of temperature drift in non-compensated d.c. amplifiers. *IEEE Journal of Solid-State Circuits*, Feb. 1970.

Cross reference
Set 12, card 10

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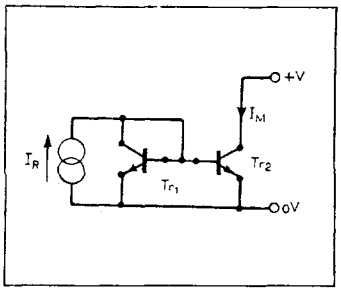
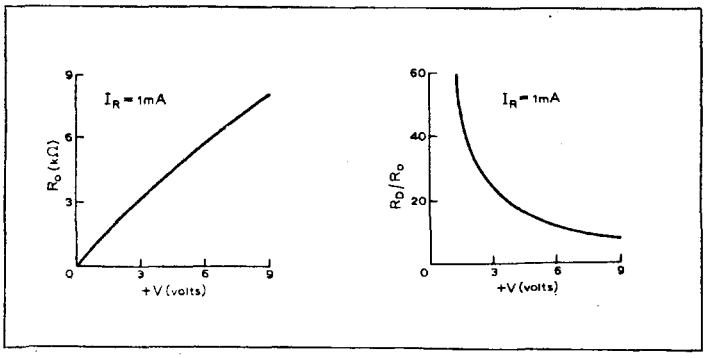
Current mirrors



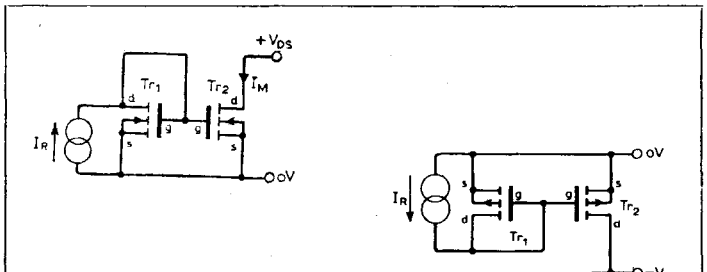
Typical data
Tr_1, Tr_2: part of CA3086
I_R: 1mA from commercial current generator, ±0.05%
I_M: measured using 4-digit multimeter.
Curves opposite show R_o and R_D as functions of +V.

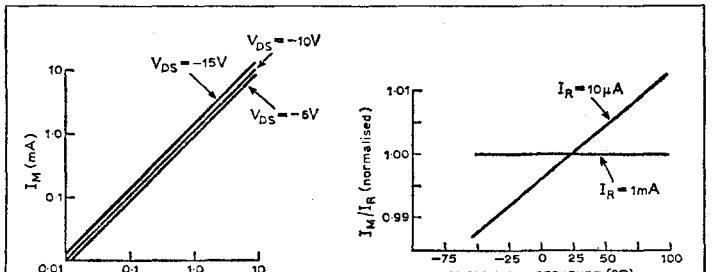


Description (bipolar)
The current mirror is an extremely useful two-transistor circuit extensively used as an integral part of monolithic operational amplifiers to define one current, the mirror current I_M, in terms of a reference current I_R. With identical transistors the base-emitter voltages are identical and if Tr_2 has a high current gain the collector currents I_R and I_M are matched, to a first order. Any matched pair of n-p-n transistors may be used but those on a single chip are preferred; the variable temperature sensitivity of discrete device reduces reliability of the circuit.
An important requirement in many applications of the current mirror is a high output resistance. The left-hand graph above shows that the static output resistance ($R_o = V/I_M$) increases with V for a given reference current value. However, the right-hand graph shows that whilst the dynamic output resistance ($R_D = \delta V/\delta I_M$) also increases with V, the far more rapid rise in R_o causes the ratio of dynamic to static output resistance to fall rapidly with increasing V. Hence, a compromise must be made between the values of R_o and R_D to be used with a given value of I_M.

For currents in the microamp range the output resistance of the current mirror can be increased by inserting a negative feedback resistor in the emitter lead of Tr_2.

For higher current requirements, transistors on the same chip can be connected in parallel to increase the junction areas.



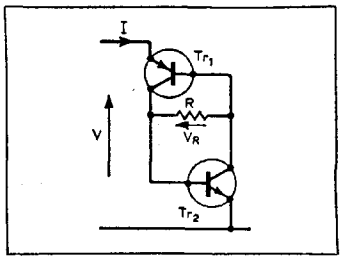


Description (m.o.s.)
Current mirror circuits can also be produced using m.o.s. transistors, the basic form using n-channel devices shown above left. Transistor Tr_1 is diode-connected performing as a transistor with 100% feedback. Thus its drain current is still controlled by its gate-source voltage V_{GS}, i.e. $I_D \approx g_{ss} V_{gs}$ where g_{ss} is the forward transconductance. Forcing a current I_R into this diode-connected transistor causes V_{GS} to rise until a state of equilibrium is attained when Tr_1 sinks the reference current. The gate-source voltage of Tr_2 is identical to that of Tr_1, due to the parallel connections. Hence if both have identical characteristics, Tr_2 is also capable of sinking an identical current, the mirror current I_M.
A reasonably good degree of matching can be obtained between the n-channel devices on a monolithic chip, the mirror current being typically within 10% of the reference current.
A current mirror using monolithic p-channel i.g.f.e.ts, shown centre left, provides better performance than the n-channel type due to the ability to provide much closer matching of the characteristics of p-channel devices. Such a circuit provides an I_M/I_R ratio which is to a first order independent of V_{DS}, as shown centre right.
The graph above right shows that the normalized ratio of I_M/I_R is within 1% of its nominal value over a wide range of ambient temperatures and I_R values.

Further reading
Jaeger, R. C. High output resistance current source, *IEEE Journal of Solid-State Circuits*, pp.192-4, August, 1974.
RCA Solid State Databook SSD-201B, pp.183-8 and 213-25, 1974.
Hart, B. L. Bidirectional *Wireless World*, vol. 76, 1970, pp.511-4.
Hart, B. L. Bidirectional current source, *Electronics Eng.* pp.39-41, July, 1974.

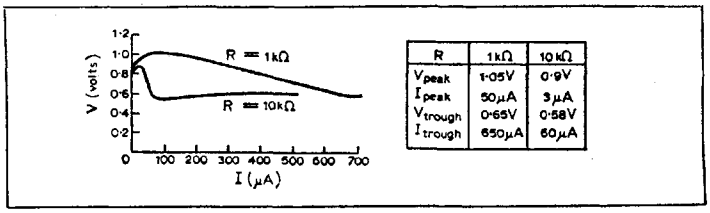
Cross references
Set 3, card 9.
Set 6, card 4.
Set 9, card 5.
Set 10, cards 1, 3, 7.
Set 12, cards 4, 7.
Set 15, card 6.
Set 16, card 1.

Complementary switching transistors



Components
Tr_1: BFR81, Tr_2: BFR41
R: 1k, 10kΩ

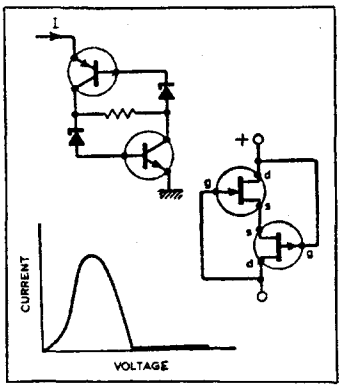
Performance
Slope in negative resistance region 0.75kΩ and 8kΩ for R=1kΩ 10kΩ respectively (see graph).

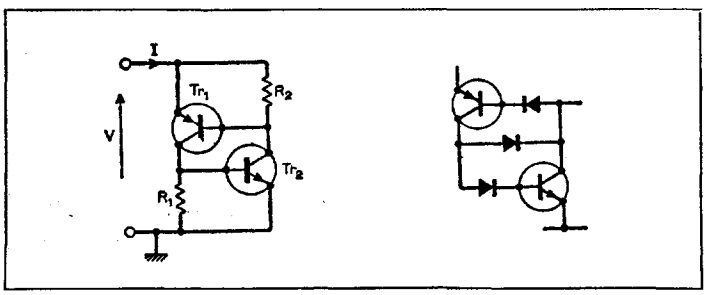


R	1kΩ	10kΩ
V_{peak}	1·05V	0·9V
I_{peak}	50μA	3μA
V_{trough}	0·65V	0·58V
I_{trough}	650μA	60μA

Circuit description
The arrangement of the complementary pair of transistors, with or without the resistor R, or connected between two other points, is a frequently used combination (see cross refs.). With the resistor R as shown, the circuit acts over a portion of its I-V characteristics as a negative resistance, of value $-R$ approximately. Graphs obtained are shown for values of 1k and 10kΩ.

Initially with low I, V may be considered as $V_{EB_1} - V_R + V_{BE_2}$. As V_R is low initially V is the sum of the two exponential emitter-base voltages. As I increases these two voltages tend to 0.6V but V_R continues to rise and because of the minus sign V starts to fall, at a value slightly less than 1.2V. The fall continues (negative resistance region) until both transistors saturate. At this point we can no longer assume that all the current is passing through both collectors and R and we are best to view V as being $V_{EC_1} + V_R + V_{CE_2}$. Since the two transistor voltages are relatively fixed, V then starts rising again. The value of the trough is given by $V_{EC_1}\text{sat} + V_{BE_2}\text{sat} \approx V_{BE_2}\text{sat}$. The voltage range of the circuit is readily increased by the modification shown opposite with Zener diodes appropriate to the application.
These circuits are described as being open-circuit stable, i.e. for any current drive there is a unique voltage. The dual of this is the voltage driven, short-circuit-stable device. An f.e.t. realization of this is shown with the corresponding characteristic (see Further reading).



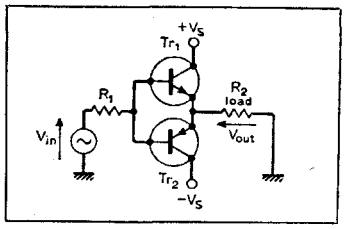


Circuit description
The circuit shown overleaf, with $R=\infty$, is the basis of simulated thyristors, silicon controlled switches and simulated unijunction transistors. The action, with $R=\infty$, can be deduced from the V-I graph shown, bearing in mind that the negative resistance slope is now $-\infty$. Alternatively, the circuit above can be considered as follows. Initially Tr_1 and Tr_2 are in the non-conducting state. A positive voltage of about 0.7V on the base of Tr_2 causes that transistor to conduct and lower its collector voltage. This causes Tr_1 to conduct and providing Tr_1 and Tr_2 produce sufficient current through R_2 and R_1 respectively to keep the transistors conducting, then the action is self-sustaining with a voltage of approximately one V_{BE} across the circuit. The circuit can thus be used as a switch, triggered by a suitable voltage at either base. With $R_1=R_2=1\text{k}\Omega$ a value of 1.3mA for I was found to be the minimum which would maintain conduction. This value is as expected as the current I will split fairly evenly between Tr_1 and R_1 and Tr_2 and R_2. Since approximately 0.65V is required at the base of each transistor to maintain conduction, it will be provided by 0.65mA in each path.
For high-speed switching it is important to prevent the transistors from saturating. Addition of the anti-saturation diodes shown prevents the collector voltages from dropping below V_{BE}. The base lead diodes are not essential.
Increasing R_1 increases the trigger voltage necessary and reduces the effect of trigger point transients.
Transients in the supply line give rise to false triggering due to rate effect. This can be reduced as R_2 is reduced although this increases the holding current necessary.

Cross references
Set 10, card 5.
Set 8, card 3.
Set 6, card 9.
Set 3, card 4.

Further reading
G.E. Transistor Manual.
Sharma, S. M. Current-controlled negative resistance circuit. *Int. J. Electronics*, 1974, vol. 37, pp.209-18.
Negative resistance shown in dual f.e.t. device, *Electronics*, April 18, 1974, p.5E.

Complementary emitter-follower



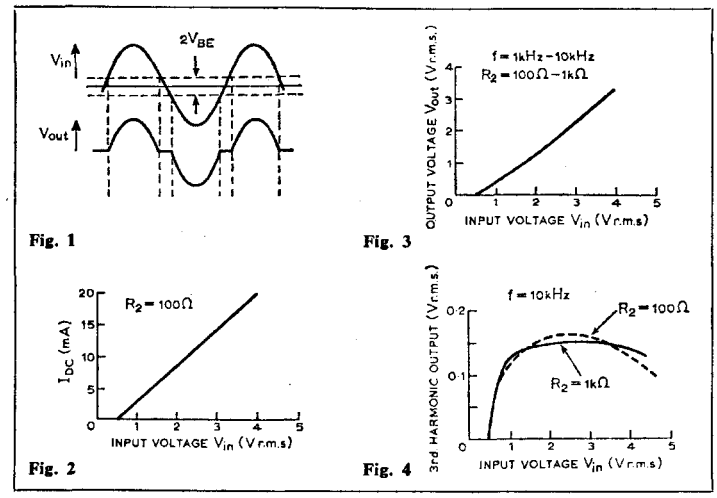
Typical data
V_S: ±6V
T_1: BFR41, T_2: BFR81
R_1: 330Ω, R_2: 1kΩ
Signal frequency: 1kHz
Fundamental/3rd harmonic output/input shown on graphs

Circuit description
The basic circuit comprises a complementary n-p-n/p-n-p pair operating under class-C bias, and is the basis for many audio power/amplifiers. When a positive-going input signal exceeds about 0.7V, transistor Tr_1 will turn on, increasing its collector current which develops a voltage across the load R_2, but with a voltage gain of less than unity. At the same time Tr_2 is biased off. Similarly, a negative-going input signal turns Tr_2 on and Tr_1 off, and the circuit thus provides bidirectional currents through the emitter load. The base-emitter diode characteristic is non-linear at low voltages, resulting in cross-over distortion (approximately $2V_{BE}$) across the load. The resulting distortion on a sine wave input is shown in Fig. 1. Without an additional bias network, the effect of this distortion can be minimized by ensuring that $V_S \gg V_{BE}$. Using both positive and negative power supplies permits operation down to zero frequency. For a single supply a capacitor is required in series with the load, to provide the base and collector currents of Tr_2 during negative-going input signals.

Component changes
R_2: Range from 100 to 1kΩ. Variation in gain minimal.
Frequency: Up to 30kHz, little difference from lower frequency operation.
Variation of mean current with input level in Fig. 2.
R_1: Chosen to suppress parasitic oscillations.
Alternative may be to keep interconnections very short to minimize series inductance.

Effect of bias (Figs. 5 & 6)
R_B varied until transistors just on the point of conduction. Graph shows 3rd harmonic distortion optimized by R_B. The above is a basic method of biasing to ensure class B or AB operation. Diodes D_1, D_2 may be chosen to achieve temperature independence of quiescent current.
Where increased current gain is needed for high power outputs, the Darlington pair of Fig. 8 (a) and compound emitter followers of (b) and (c) are useful, but may provide more difficult biasing problems.

Line driver (Fig. 7)
Driving 50-Ω cable with line capacitance slows pulse edges.



Improved using complementary pair. Typical fall time ≪ 100ns but dependent on simulated cable capacitance (R_o: 50Ω, C: 3nF, t_F: 75ns).

Further reading
Williams, P. Voltage following, *Wireless World*, Sept., 1968.
Williams, G. E. Practical transistor circuit design and analysis, McGraw-Hill 1973.
Markus, T. Electronic circuits manual, McGraw-Hill.

Cross references
Set 7, cards 1, 3.
Set 20, card 1.

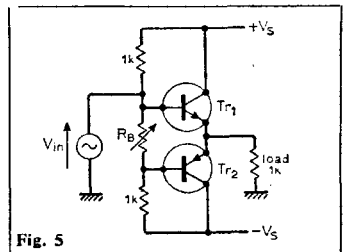


Fig. 5

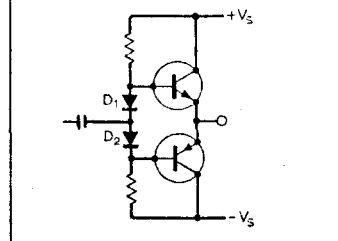


Fig. 6

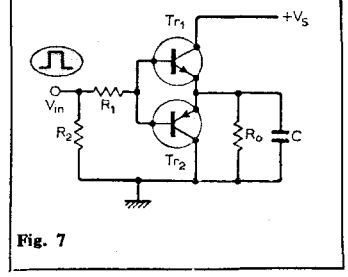
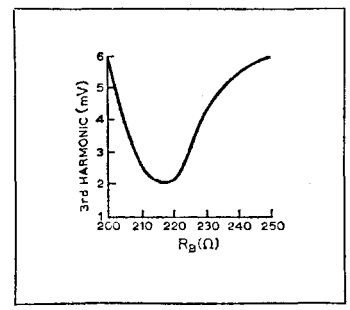
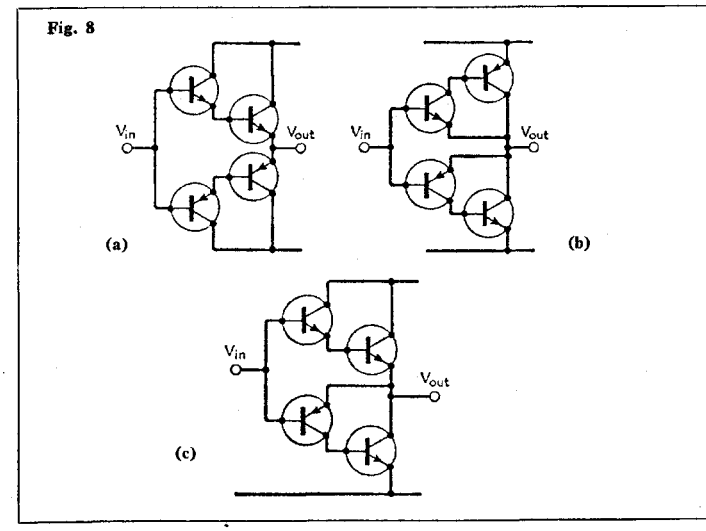
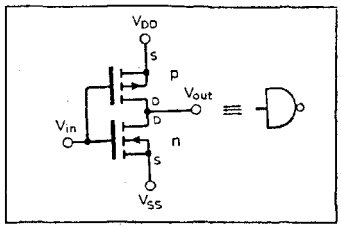


Fig. 7





CMOS circuits



Description

The c.m.o.s. inverter shown above comprises a p-type and n-type enhancement mode m.o.s. transistor on the same chip. $V_{DD}-V_{SS}$ may be in the range 3 to 15V. The pair is useful in digital circuits because of well-defined threshold that V_{in} must exceed before the device turns on.

n-type: V_{GS} positive for ON

p-type: V_{GS} negative for ON

Where the output has to sink or source current, the pair can be envisaged as the series switches. Fig. 1 is a source condition, obtained for $V_{in}=V_{SS}$ and $V_{out}=V_{DD}-I_dR_o$ where R_o is the output resistance of p-transistor in the on state. For $V_{in}=V_{DD}$, the n-type sinks current for Fig. 2; $V_{out}=I_dR_o$.

Basic i.c. package CD4007 contains one inverter and two complementary pairs with the drains unconnected. This permits a variety of interconnections: n-types are paralleled to increase sink current capability, Fig. 3. p-types are paralleled to increase source current capability, Fig. 4.

Fig. 5 is a dual bi-directional transmission gate where the two outputs and input may be interchanged for two inputs and one output. Note that the position of the transistors in the middle pair have been reversed.

The CD4049 package contains six inverters with current drive capability almost an order of magnitude greater than basic package. Parallel connection for increasing current sinking indicates typical current sharing for d.c. condition, Fig. 6.

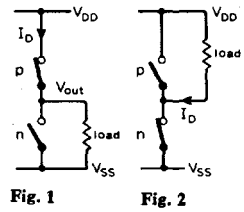


Fig. 1

Fig. 2

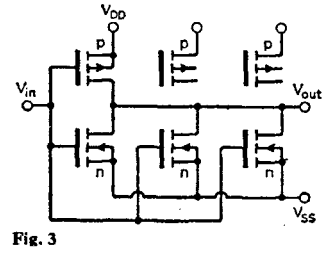


Fig. 3

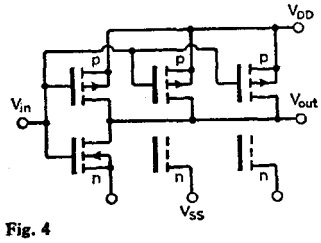


Fig. 4

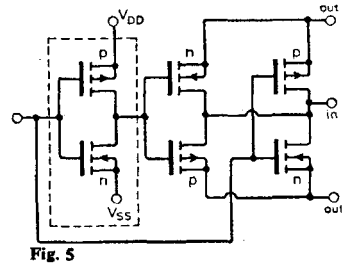


Fig. 5

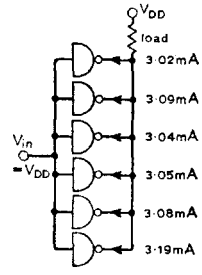


Fig. 6

CD4016 i.c. package contains four analogue switches (transmission gates). Each switch comprises an inverter and a parallel pair of n- and p-channel transistors, Fig. 7. For a threshold of approximately 2V in each channel and control voltage 10V, the gate control voltage of the p-m.o.s. is 0V. If $V_{in}>8V$, the n-channel will be open, but the gate-source voltage of the p-m.o.s. is −8V (greater than threshold) and signal is switched through.

Because the V_{GS} of each transistor never equals the threshold of the transistors, the full supply range can be switched through.

A.C. amplifier (Fig. 9)

Best linearity and voltage swing if $V_{out}=V_{DD}/2$ and this is provided by the resistive connections (Figs. 9 & 10). Supply drain ≈2mA for 10V supply.

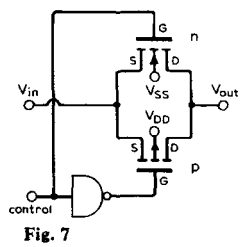


Fig. 7

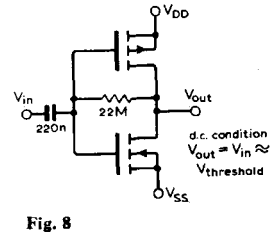


Fig. 8

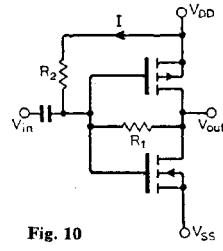


Fig. 10

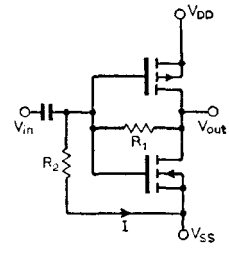


Fig. 9

Further reading

RCA Solid-State Databook Series SSD—203A 1973.

Design Ideas with COS/MOS *New Electronics*, April 30, 1974.

I.C. op-amp has CMOS output *Electronics*, Sept. 19, 1974.

Fitchen, F. C. and Ellerbruch, V. G. Linear operation of the MOSFFT complementing pair, *IEEE Journal of Solid-State Circuits*, Dec., 1971.

Cross references

Set 8, card 1.
Set 10, card 7.
Set 11, card 5.
Set 12, card 1.

Triples & mixed pairs

The principle of using transistors in pairs can often be usefully extended to the use of devices in triples, the resulting equivalent transistor having a current gain equal to the product of those of the individual transistors. In all such arrangements, two of which are shown above, the equivalent transistor has the same "polarity" as the input transistor.

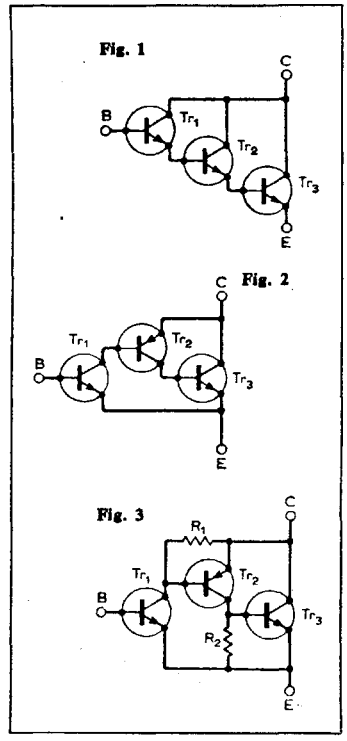
The three n-p-n transistors in Fig. 1 act as a compound emitter-follower having a current gain of approximately h_{fe}^3, for large h_{fe}, and is useful for driving currents of several amps from a driver stage delivering less than a milliamp.

The complementary transistor triple in Fig. 2 is useful in voltage regulators as a low-dissipation series element, the V_{BE} and V_{CE} values of the equivalent transistor being the lowest possible for a triple.

In this arrangement the temperature coefficient of only one transistor affects the output. The operating current in the input transistor will be very small, reducing its current gain. This effect can remove much of the benefit of using a triple instead of a pair. By using resistors as shown in Fig. 3 the operating currents in the earlier stages are increased and stabilized.

Thinking of the various pairs of devices discussed on other cards as elementary building blocks can prove a powerful method of developing more complicated circuit functions. For example, a long-tailed pair Tr_1, Tr_2 and Tr_3 may be used to drive a current mirror Tr_4 and Tr_5 as shown in Fig. 4 to produce a waveform generator which provides a symmetrical triangular output when driven by input pulses. This circuit uses the long-tailed pair to switch a defined current into two paths; which combined with a closely-matched current mirror permits the capacitor to be charged and discharged at the same rate when the charging current is varied.

Typical values. Supply ±10V, V_R 0V, R_1 5kΩ, R_2 2·2kΩ, R_3 4·7kΩ, C_1 33nF, D_1 1N914, D_2 1N5234, D_3, D_4 HP5082–2800, Tr_1, Tr_2, Tr_3 2N3546, Tr_4, Tr_5 ½×SL301–A.



This concept of mixing elementary pairs of devices can be developed to build a single-supply operational amplifier using bipolar and m.o.s. transistor pairs, as shown in Fig. 5, having a unity-gain bandwidth of about 10MHz. The operational amplifier, which requires two CA3600E and one CA3046 packages, has three stages. The differential input stage uses two p-channel m.o.s. transistors Tr_3, Tr_4, the second stage uses an n-p-n bipolar transistor Tr_7 and the output stage is a complementary m.o.s. transistor pair Tr_8, Tr_9. The zener network, using two diode-connected transistors D_1, D_2 of the CA3046, feeds a p-channel current mirror Tr_1, Tr_2 that establishes a 400μA constant current in the input stage. This differential-input amplifier is loaded by four resistors, R_1 to R_4, and a bipolar current mirror, Tr_5, Tr_6, to provide optimum balance, any voltage offset being nulled with the potentiometer R_8. The current in the second stage, determined by R_6, is adjusted to equal the 400-μA first-stage current to provide similar negative and positive slew rates. The output stage is biased as a class-A amplifier by R_5 and may be driven to within a few millivolts of the ground rail. The overall voltage gain varies inversely with the load resistance which, as with a monolithic operational amplifier, would have a value of about 2kΩ. Compensation requires inclusion of the feedback capacitor C_1, with C_2 added when using the operational amplifier as a unity-gain follower. In this configuration, R_9 and C_3 should be added to avoid the possibility of latch up and D_3 and D_4 added to the inputs to prevent negative-going input signals exceeding about 700mV which could also cause latch up. Typical values are: V+15V; R_1, R_2, R_3, R_4 200Ω±1%; R_5 20kΩ±1%; R_6 11kΩ±1%; R_7 7.5kΩ±1%; R_8 10kΩ; R_9 1kΩ; C_1 39pF; C_2 300pF; C_3 150pF; D_3, D_4 1N914.

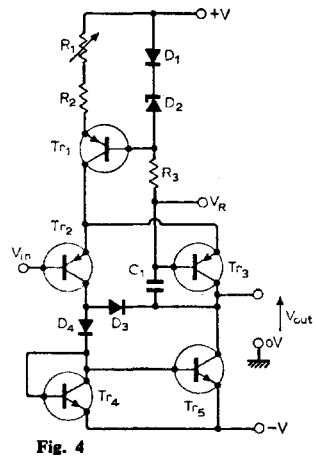


Fig. 4

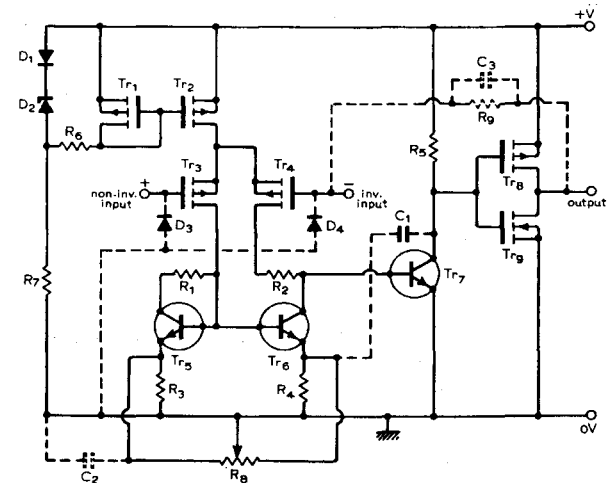


Fig. 5

Further reading

Williams, P. Voltage Following, *Wireless World*, vol. 74, 1968, pp. 295-8.

Nowicki, J. R. Compound transistor connections, *Electronic Engineering*, September, 1971, p.63.

Burwen, E. High-gain triple Darlington has low saturation voltage, *Electronics*, Oct. 3, 1974.

wireless world circard

Pot pourri

n-n-p/p-n-p simulation at high voltage

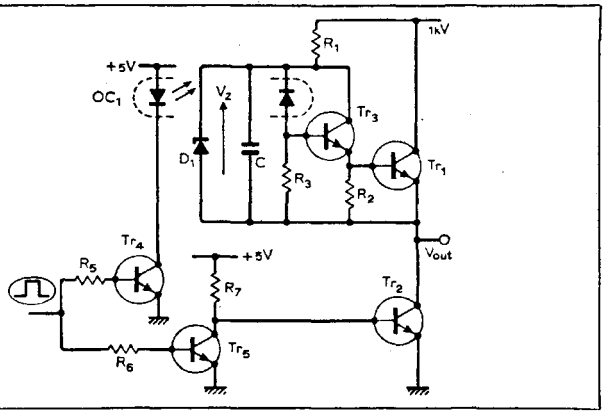
Optical couplers are used to provide fast high voltage switching with a simulated complementary pair. Transistors Tr_1 and Tr_2 are high-voltage n-p-n types: Tr_1 is on when Tr_2 is off and vice versa. With Tr_1 off, C charges to V_Z, storing charge. This is used to turn Tr_1 on fast when the optical coupler operates.

Optical coupler provides the polarity inversion when Tr_4 and Tr_5 are driven by 5V pulses.

Tr_3, Tr_4, Tr_5: 2N2222
R_1: 270kΩ (10W), R_2: 1kΩ
R_3: 100Ω, R_4: 47Ω R_5
R_6: 680Ω, C: 10nF
D_1: 6.8V zener, OC1: Monsanto MCO1

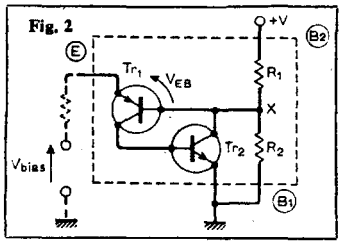
Rise and fall times of around 2μs are claimed for components used.

Fig. 1



Unijunction from bipolar pair

Fig. 2



Tr_1: 2N4126, Tr_2: 2N4124
R_1, R_2: 4.7kΩ, V: +3 to 25V

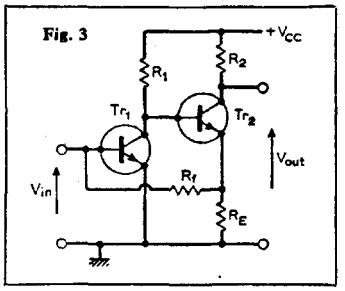
Because the collector current of Tr_1 is the base current of Tr_2 and vice versa, then any change of current provides a positive feedback action.

B_1, B_2 and E are the equivalent unijunction terminals. When E is open-circuit $V_X = R_2V/(R_1+R_2)$.

When the potential at E exceeds V_{EB} and V_X, both transistors saturate, and R_2 is short-circuited. This condition is maintained for a potential at E down to $V_{EB}+V_{CE}$sat of Tr_2. Switching speed depends on maximum frequency of of operation of the transistors. For Tr_1, Tr_2 silicon drift of $V_{EB} < 3$mV/deg C.

Shunt-series d.c. feedback pair

Fig. 3



Current fed back via R_f is proportional to Tr_2 collector current, and thus the circuit provides current-shunt negative feedback, which primarily controls the overall current-gain.

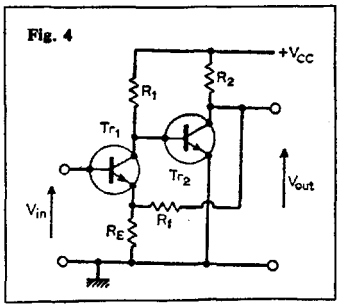
Effective current gain is $A_1/(1+\beta A_1)$ where A_1 is the current gain of the two stages, with R_f connected between Tr_1 base and ground. $\beta \approx R_E/R_f$. For $\beta < 0.1$, input resistance is $R_i/(1+\beta A_1)$ where R_i is input resistance without feedback.

Voltage gain $\approx \dfrac{R_f}{R_E} \cdot \dfrac{R_2}{R_S}$

where R_S is source resistance. Voltage gain can be increased by by-passing R_E, or by-passing the mid-point of the feedback resistor R_f.

Series-shunt d.c. feedback pair

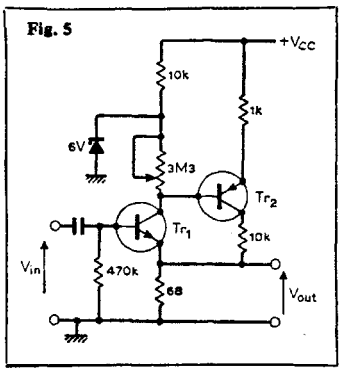
Fig. 4



In this connection, the voltage gain is now mainly affected by the feedback, and the input resistance is increased. Voltage gain is $A_v/(1+\beta A_v) \approx 1/\beta$ if A_v is large. A_v is the product of the gains of each stage, with R_F connected from Tr_2 collector to ground, and $\beta = R_E/R_F$. Input resistance is $R_i(1+\beta A_v)$, where R_i is effective input resistance of the first stage. Note: Biasing networks for those CE-CE amplifiers are not shown.

Common emitter pairs with composite transistors

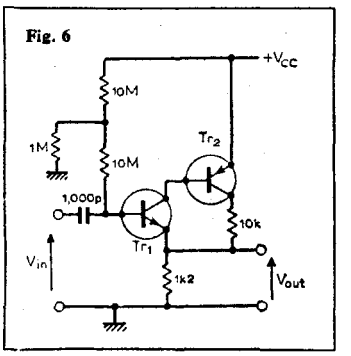
Fig. 5



Tr_1, Tr_2: 2N4355
V_{CC}: 15 to 30V
Voltage gain ≈ 100
Cut-off frequency ≈ 10kHz
Input resistance > 200kΩ

By sacrificing voltage gain, a high input impedance can be obtained with the circuit shown. below.

Fig. 6



Tr_1, Tr_2: 2N4355
V_{CC}: +10 to 30V
Voltage gain ≈ 10
Input impedance: 5MΩ

Further reading for circuits 1-6

1. Mitchell, P. & Robbins, K. Simulating an npn/pnp pair for high voltage switching. *Electronics*, Aug. 22, 1974.
2. Shyne, N. A. Bipolar pair simulates unijunction, *Electronics*, Jan. 24, 1974.
3, 5, 6. Cowles, L. G. Transistor circuit design, Prentice-Hall, 1972.
4. Millman & Halkias, Electronic Devices and Circuits, McGraw-Hill, 1967, p.502.

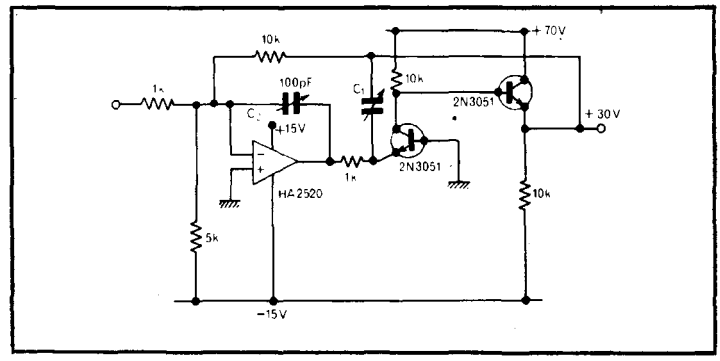
Cross references

Set 20, cards 6, 7.
Set 12, card 9.

wireless world circard

Set 20: Transistor pairs Up-date

1. The common-base and common-collector pair used in the d.c. feedback pair configuration has a low input impedance, low output impedance and wide bandwidth. Using high voltage transistors it is suitable as a pulse-amplifier to produce very fast positive edges even into capacitive loads (a complementary class B output stage would be needed to make the falling edge equally fast). It lacks d.c. stability but can be combined with a high speed op-amp as shown to give an output slew rate claimed in



the reference to be 200V/μs and full power output of 60V peak to peak at 1MHz. The overall feedback brings the output stage within the loop reducing the offset and drift to that of the op-amp. The latter provides current drive into the c.b. stage but does not need to supply a large voltage swing reducing the demands on its slew rate. The reference describes other more complex circuits capable of extending the small-signal bandwidth to 20MHz and slew-rate to 1200V/μs or even higher using special amplifiers. Precautions on layout and decoupling are given.

Reference

Bunin, H. Low-cost v.c.o. driver amplifiers really perform if designed right, *EDN*, 1974, Oct. 5, pp. 51-5.

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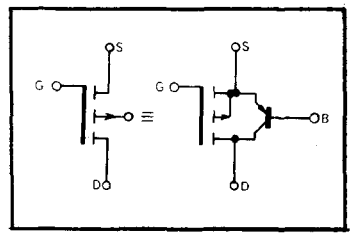
2. A recent paper has considered the complex behaviour of apparently simple m.o.s. transistors. If the substrate connection is available, then for a p-channel enhancement mode f.e.t. that substrate also acts as the base of a p-n-p transistors with source and drain representing the emitter and collector respectively. To a first-order approximation the devices are



shown to be independent when conducting with the total current being equal to the sum of the individual currents. The m.o.s. action is controlled by a square-law transconductance equation, while the bipolar transistor has a collector current proportional to the base current to a first order of magnitude (low current gain in this example). Thus the waveform in a load resistor connected to a negative supply could be varied by applying an input signal separately or jointly to the gate and substrate terminals. This parallel combination should also be amenable to other waveform processing methods by combining feedback networks with it.

Reference

Hart, B. L. and Barker, R. W. J. First-order theory of m.o.s.f.e.t. hybrid-mode operation, *Int.J. Electronics*, 1975, vol. 38, pp. 625-30.

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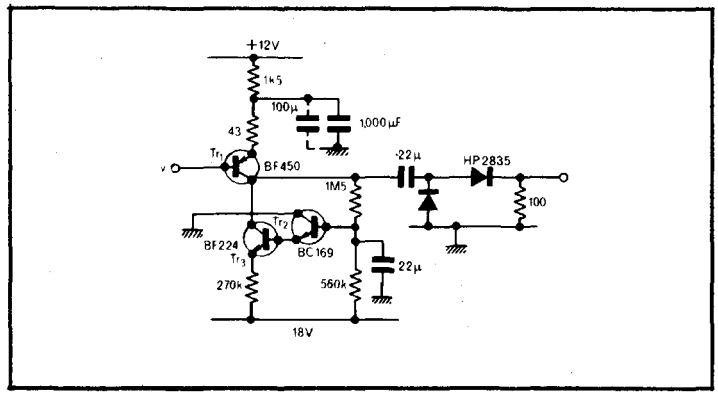
3. This circuit is not strictly a two-transistor arrangement but illustrates how a circuit can be partitioned to reveal familiar pairs. It is a wide band precision rectifier that uses a high output impedance rather than negative feedback to overcome the diode non-linearities. A Darlington pair composed of Tr_2, Tr_3 is modified to remove the collector of Tr_2 from the circuit output, by returning it to ground. This leaves Tr_3 providing a low-capacitance constant-current sink. D.c. negative feedback defines the operating points (with negligible loading because



the current gain is high allowing high-value resistors. The 43Ω resistor defines the circuit transconductance and Schottky diodes maintain the bandwidth with minimum p.d. and hence non-linearity at low levels. Where large electrolytics are needed to extend low frequency response (20Hz is quoted in reference) then parallel tantalum capacitors are added to maintain low impedance at high frequencies. The source has to be capable of carrying the base current of Tr_1. The reference indicates the upper cut-off frequency as 80MHz with good accuracy to 10MHz, and good linearity and repeatability for 200mV r.m.s. full-scale.

Reference

Knott, K. F. Sensitive wideband linear a.c.-d.c. converter, *Proc.IEE*, 1975, vol. 122, pp. 249-52.

notes

notes

circuit designs

P Williams / J Carruthers / J H Evans / J Kinsler