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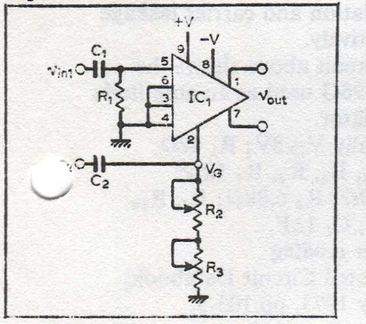
Set 22: Amplitude modulators—1

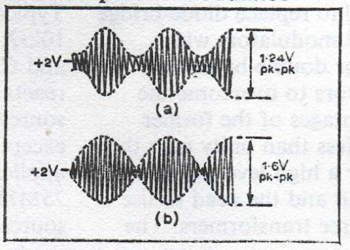
I.C. package modulators

Typical performance
Supplies: ±10V, 10mA
IC_1: MC1445L
R_1: 47Ω
R_2: 4.7kΩ; R_3: 220Ω
C_1, C_2: 100nF
Amplitude modulator
V_G 2V d.c.
v_{in1} (carrier) 130mV pk-pk
f_c=1MHz
v_{in2} (modulation) 1.3V pk-pk
f_m=10kHz, to produce maximum useful modulation depth of ≈ 78%.



v_{out} (pin 1 or 7) 800mV pk-pk unmodulated, see waveform opposite.
Balanced modulator
V_G 2.5V d.c. to balance out carrier
v_{in1} (carrier) 130mV pk-pk
f_c=1MHz
v_{in2} (modulation) 2.4V pk-pk (max)
f_m=10kHz
v_{out} (pin 1 or 7) see waveform opposite.

Circuit description
Many integrated circuit packages are available either in the form of purpose-designed modulators for producing a.m. or d.s.b. outputs or in the forms which can be readily adapted to these applications. An example of the latter type is the gate-controlled, two-channel-input wideband amplifier shown left. This integrated circuit consists of a pair of differential-input amplifiers having a constant current switched between them under the control of a gating signal which cuts off one amplifier when the other is conducting. The output from each of these amplifiers is available via low-output-impedance Darlington emitter followers. Although the gating signal would normally be at t.t.l.-compatible logic levels, the characteristics of the gate circuit allows the i.c. to be used as an amplitude modulator



when connected as shown. Although the voltage/gain/gate voltage characteristic is far from linear over the full gate voltage range, it is virtually linear over a range of a few hundreds of mV with respect to a suitable d.c. bias. This bias is obtained by connecting a coarse/fine control (R_2, R_3) between the gate (pin 2) and ground. The low-frequency modulating signal is superimposed on this bias by coupling it to the gate through C_2 and the carrier input is coupled via C_1 and R_1 to either of the input channels, pins 5 or 6 (as shown) or pins 3 and 4 (unused in circuit shown). The amplitude modulated output is available at either output, pin 1 or pin 7. With defined input signal levels, the output modulation depth may be varied using R_2 and R_3.

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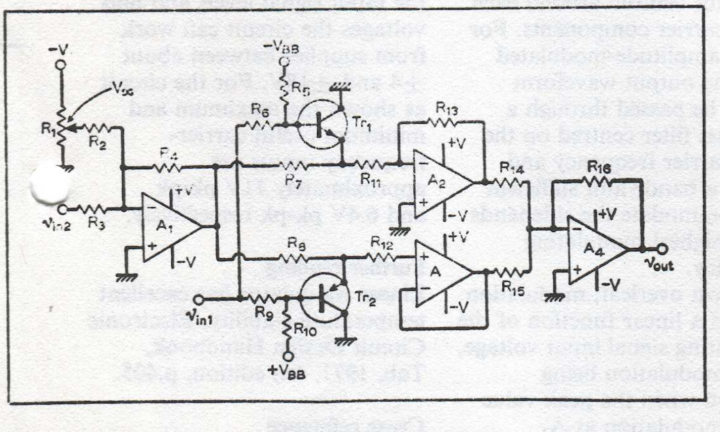
Set 22: Amplitude modulators—2

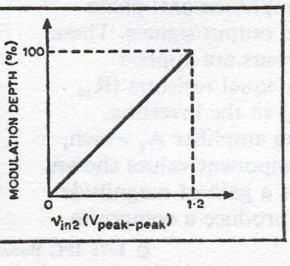
Linear amplitude modulator

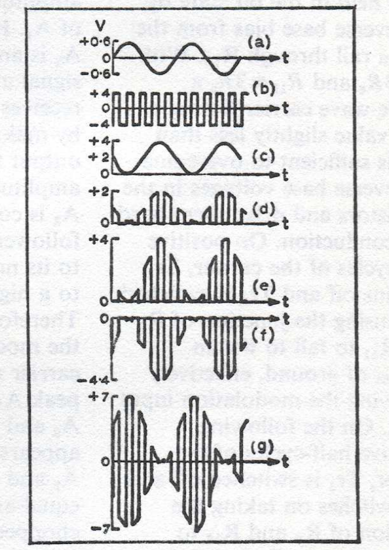


Typical performance
Supplies: V±15V+7.5mA, −9.3mA; V_{BB}±5V 0.75mA
A_1 to A_4: 741
R_1, R_3, R_7, R_8, R_{11}, R_{12}: 10kΩ
R_2: 100kΩ R_4: 33kΩ
R_5, R_{10}: 4.7kΩ R_6, R_9: 1.5kΩ
R_{13}, R_{14}, R_{15}: 22kΩ R_{16}: 39kΩ
Tr_1: BC125 Tr_2: BC126
V_x: −5.5V

v_{in1} (carrier) 8V pk-pk square wave at f_c≈10kHz.
v_{in2} (modulation) 1.2V pk-pk sinewave at f_m≈1kHz to produce a.m. output with 100% modulation (see graph right) v_{out} see waveforms opposite for 100% modulation.

Circuit description
The modulating signal (v_{in2}) is applied via R_3 to the inverting, summing operational amplifier A_1 and receives a gain of $-R_4/R_3$. Although this input is bipolar in nature the output from A_1 is not permitted to go more negative than 0V due to the presence of a d.c. bias obtained from the −V rail via R_1 (V_x) which receives an inverting "gain" of R_4/R_2. This composite, positive signal is applied over separate paths to the inverting input of A_2 (via R_7 and R_{11}) and to the non-inverting input of A_3 (via

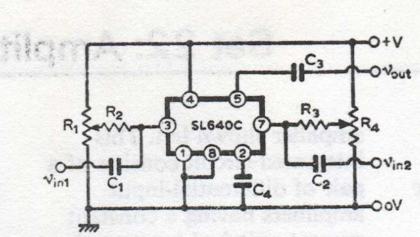


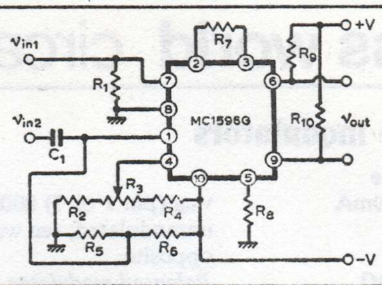


R_8 and R_{12}). The junctions of these pairs of resistors are connected to ground through Tr_1 and Tr_2 when these "chopper" transistors are switched on by the square-wave carrier (v_{in1}).

A double-sideband suppressed-carrier signal may be produced by applying the carrier simultaneously to both channels of the input differential amplifiers which then have their outputs cross-coupled. The resulting balanced modulator is as shown overleaf but with pin 5 earthed and the junction of R_1 and C_1 taken to pins 6 and 3. If the carrier has sufficient amplitude to switch these channels completely off and on, the modulating signal is switched between the channels at the carrier frequency, which is equivalent to multiplying the modulating signal by a switching function—the required condition for producing a pair of side-frequencies and suppressing the carrier. If a reduced-amplitude carrier is required, this can be produced by slightly changing the d.c. bias applied to the gate terminal by means of R_3.

Component changes
Useful range of supply: ±4 to 12V





Maximum useful carrier input ≈280mV pk-pk producing unmodulated carrier output of ≈3.3V pk-pk
f_c(max)≈75MHz
Maximum load current≈25mA.
Examples of integrated circuits purpose-designed as balanced modulators are the MC1596G and the SL640C. These packages are essentially intended to replace diode-bridge (or ring) modulators with transistor double-balanced modulators to overcome the disadvantages of the former type of less than unity gain the need for a high level signal at one input and the need to use up to three transformers. The inherently good switching of the monolithic transistors ensures that excellent carrier suppression is obtained with little need for balancing by external components when the devices are used as double-sideband suppressed-carrier generators.
An arrangement of the SL640C for this purpose is shown above. Typically, V=+6V; R_1, R_4 10kΩ; R_2, R_3 330kΩ; C_1, C_2 and C_3 should have low reactance compared with the source and output resistance, except for high frequency applications (i.e. f_c approaching 75MHz) where the modulation source resistance should be low and C_2 of comparable reactance C_4 is a base-decoupling capacitor and must have a very low reactance at all frequencies used to minimize carrier and modulation feed-through. Resistors R_1 and R_2 are adjusted to minimize modulation and carrier leakage respectively.
The circuit above shows the MC1596G used as an amplitude modulator.
Typically V±8V; R_1 47Ω; R_2, R_4, R_5, R_6, R_7 1kΩ; R_3 470Ω; R_8 6.8kΩ; R_9, R_{10} 3.9kΩ; C_1 1μF.

Further reading
Integrated Circuit Databook, Plessey 1973, pp.103-5.

In the absence of a carrier input, Tr_1 is held off by the reverse bias on its base from the $-V_{BB}$ supply via R_5 and Tr_2 is held in the off state by the reverse base bias from the $+V_{BB}$ rail through R_{10}. With $R_5 \approx 3R_6$ and $R_{10} \approx 3R_9$ a square-wave carrier having a peak value slightly less than V_{BB} is sufficient to overcome the reverse base voltages in the transistors and drive them hard into conduction. On positive half-cycles of the carrier, Tr_2 remains off and Tr_1 is switched on causing the junction of R_7 and R_{11} to fall to within V_{CEsat} of ground, effectively removing the modulation input to A_2. On the following negative half-cycles of the carrier, Tr_1 is switched off and Tr_2 switches on taking the junction of R_8 and R_{12} to within V_{CEsat} of ground, effectively removing the modulation input to A_3. Thus, the signals applied to A_2 and A_3 are in the form of the modulating signal which has been chopped at the carrier rate. As the inverting input of A_2 is a virtual earth and $R_7 = R_{11}$ the signal applied to A_2 is effectively of half the amplitude appearing the output of A_1. Hence, the output from A_2 is an inverted form of the signal at Tr_1 emitter which receives a gain of R_{13}/R_{11} and by making this gain 2 the output from A_2 has the amplitude of that at A_1 output. A_3 is connected as a unity gain follower so the signal applied to its non-inverting input is fed to a high-impedance point. Therefore, although Tr_2 chops the modulating signal at the carrier rate the full peak-to-peak A_1 output is applied to A_3 and this chopped signal appears at the follower's output. A_2 and A_3 therefore provide equal-amplitude anti-phase chopped output signals. These two outputs are applied through equal resistors (R_{14} and R_{15}) to the inverting, summing amplifier A_4 which, with component values shown, provides a gain of magnitude 1.77 to produce a composite output signal which is the linear sum of its inputs.
The output waveform will contain the original carrier frequency and its harmonics with sets of upper and lower sidebands centred around each of the carrier components. For a pure amplitude-modulated wave the output waveform should be passed through a bandpass filter centred on the input carrier frequency and having a bandwidth sufficient to accommodate the sidebands of the highest modulating frequency.
As shown overleaf, modulation depth is a linear function of the modulating signal input voltage, 100% modulation being achieved when the peak value of the modulation at A_1 output is equal to the d.c. bias at that point.
With the low-cost operational amplifiers shown the circuit can function with carrier frequencies up to about 25kHz. Higher carrier frequencies can be used if operational amplifiers having a high gain-bandwidth product than the 741 are used, and in principle, the circuit should operate with carrier up to several MHz.
With suitable adjustment of the input signal levels and bias voltages the circuit can work from supplies between about ±4 and ±18V. For the circuit as shown the maximum and minimum useful carrier-frequency inputs are approximately 11V pk-pk and 6.4V pk-pk respectively.

Further reading
Linear modulator has excellent temperature stability, Electronic Circuit Design Handbook, Tab, 1971, 4th edition, p.405.

Cross reference
Set 22, card 3.

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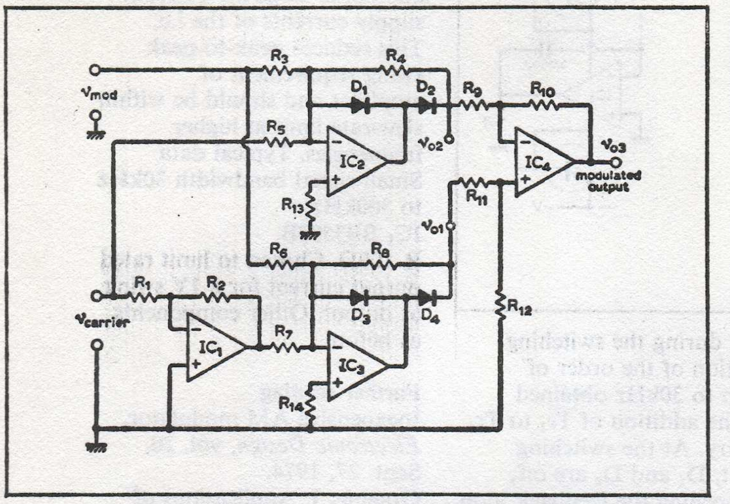
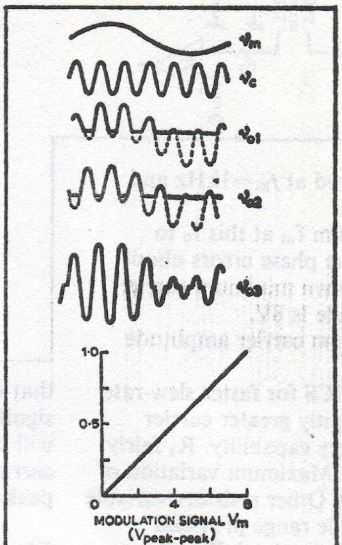
Set 22: Amplitude modulators—3

Modulator using precision rectifiers



Typical data
Supply: ±10V
IC_{1-4}: 741
R_{1-10}, R_{12}: 10kΩ
R_{11}: 4.7kΩ
R_{13}, R_{14}: 3.3kΩ
D_{1-4}: 1N914
v_{mod}: 1V pk-pk at 1500Hz
$v_{carrier}$: 2V pk-pk at 10kHz



Circuit description
IC_1 acts as inverter for the carrier signal. The lower frequency modulation signal v_m is summed with the carrier and its inversion, via the absolute half-wave rectifier circuits of IC_2 and IC_3 respectively. When the summed input is positive, the output of IC_3 tends toward a negative level due to inverter action and hence D_3 is forward biased. Therefore the negative peak outputs are clipped to a level approaching zero because D_3 is in the feedback loop. The output is characterized by V_{o1}, that at V_{o2} being similar, but of course the carrier is inverted. Non-linearity of the rectifier impedances introduces some distortion which is evident in the troughs of the modulated output and very slightly distorted at the higher levels of modulated carrier, though not the peaks of the envelope. Output filtering is unnecessary and hence drift of carrier-frequency offers no great problem.

Component changes
Maximum carrier amplitude to obtained 100% modulation 8V pk-pk ($v_m \approx$ 8V pk-pk). Maximum carrier frequency 23kHz before peaks distort

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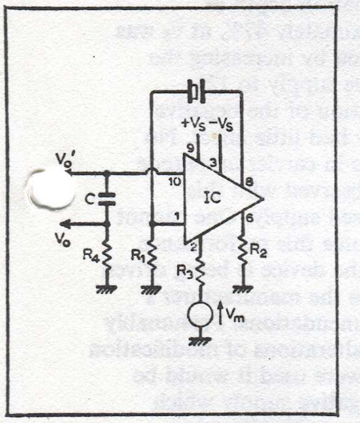
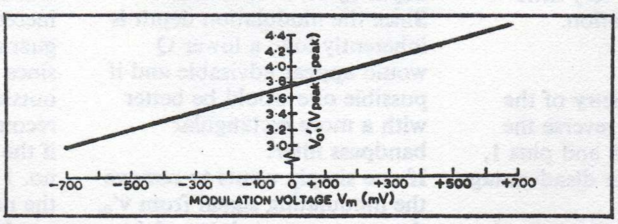
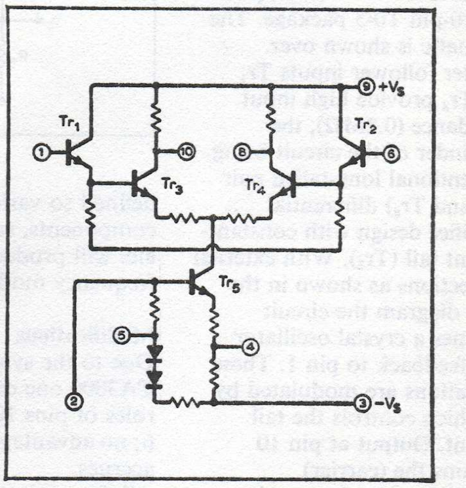
Set 22: Amplitude modulators—4

Modulated crystal oscillator

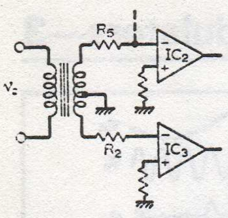


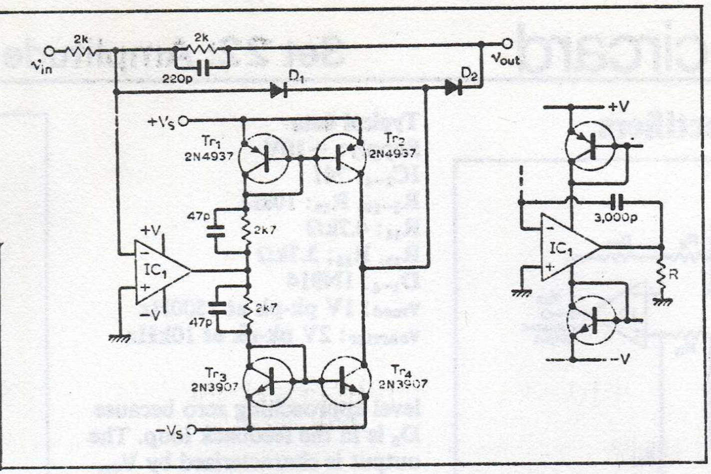
Components
Crystal: 1MHz
R_1, R_2: 1kΩ
R_3: 600Ω
R_4: 100kΩ
C: 27pF
V_s: 6V
IC: CA3000
C.r.o. probe used had impedance of 10MΩ in parallel with 10pF.





Performance
Graph shown of v'_o (not v_o) was obtained with d.c. values of v_m and indicates a modulation sensitivity of 1.07V/V and a modulation depth of approximately 25% over the range shown. Range was limited by the fact that increasing v_m beyond +700mV caused limiting on the negative peaks of v'_o. Lower limit was very much lower than that shown but there is no point in going beyond a symmetrical condition.
With the c.r.o. probe on v_o the modulation depth fell to 11% (due to the loading of the probe) and this was maintained from d.c. to approximately 2kHz without appreciable distortion. Higher frequencies caused phase distortion.
With R_1 set at 500Ω no carrier oscillations were obtained. With higher R_1, however, little effect was observed, e.g. R_1=10kΩ produced a modulation depth of 10.5% although with approximately 12% increase in carrier amplitude.
Variation of R_3 in the range 1.5Ω to 1500Ω produced very little effect; thereafter limiting





(measured at f_m=1kHz and m=1).
Maximum f_m at this f_c to minimize phase errors about 4kHz; then minimum carrier amplitude is 8V.
Maximum carrier amplitude 8.8V.
Use 741CS for faster slew-rate and slightly greater carrier frequency capability. R_1 fairly critical. Maximum variation of $\pm 200\Omega$. Other resistors variable over wide range provided ratios maintained. R_{10}, R_9 etc i.e. accurately matched resistors are suggested. Use centre-tapped transformer to provide carrier and its inverted form, as shown above.
Useful range of this modulator is in the audio band, provided that the non-linearity is not significant. Crossover distortion will be minimized for high carrier frequencies, and large peak-to-peak carrier excursions.

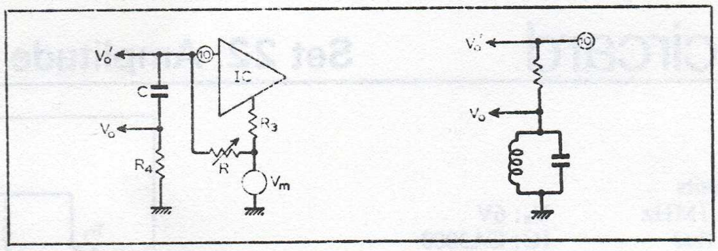
Circuit modifications
High-frequency performance is limited by slew rate and gain of the op-amp in turning off say diode D_1 and turning on diode D_2. This switching speed is increased by the circuit shown middle. Additional gain is added during the switching transition of the order of 250 up to 30kHz obtained with the addition of Tr_1 to Tr_4 circuitry. At the switching instant, D_1 and D_2 are off, thus opening the feedback loop, and do not shunt this additional network. When conduction recommences, one diode heavily conducts, shunts the high output impedance of this additional stage giving again an overall gain of near unity. Low-value resistors provide small time constants for stray capacitance.
Frequency response will be above that of op-amp when additional stage driven from supply currents of the i.c. This reduces peak-to-peak swing requirement of amplifier and should be within slew-rate limit at higher frequencies. Typical data Small-signal bandwidth 30kHz to 300kHz
IC_1 BB3500B.
R 100Ω. Chosen to limit rated output current for a 1V swing at output. Other components as before.

Further reading

Inexpensive AM modulator, *Electronic Design*, vol. 20, Sept. 27, 1974.
Graeme, J. Applications of operational amplifiers—third generation techniques, McGraw-Hill, 1973.
Graeme, J. Boost precision rectifier BW above that of op-amp used. *EDN*, July 5, 1974.

occurred.

Description
The CA3000 is a d.c. amplifier in a 10-pin T0-5 package. The schematic is shown over. Emitter follower inputs Tr_1 and Tr_2 provide high input impedance (0.2MΩ), the remainder of the circuit being conventional long-tailed pair (Tr_3 and Tr_4) differential amplifier design with constant-current tail (Tr_5). With external connections as shown in the main diagram the circuit becomes a crystal oscillator with feedback to pin 1. These oscillations are modulated by v_m which controls the tail current. Output at pin 10 contains the (carrier) oscillations plus harmonics modulated by v_m, plus v_m itself, plus d.c. The high-pass filter consisting of C and R_4 eliminates the d.c. and v_m, leaving the amplitude modulated signal.
Since the oscillator is a crystal oscillator the frequency of oscillation is extremely well



defined so variations in other components, supply voltages etc. will produce very little frequency modulation.

Modifications
Due to the symmetry of the CA3000 one can reverse the roles of pins 10, 8 and pins 1, 6; no advantage or disadvantage accrues.
All the unwanted terms in v'_o (including carrier harmonics) can be removed by use of a suitable bandpass filter.
Because the output impedance of the amplifier is high (8kΩ) a tuned L-C filter may be used as shown centre: in our case with a carrier of 1MHz and modulating signal of 2kHz a Q of 250 is permissible but would reduce the modulation depth by 0.707 at 2kHz.
Since the modulation depth is inherently low, a lower Q would appear advisable and if possible one would be better with a more rectangular bandpass filter.
If one simply wants to remove the modulating signal from v'_o, the arrangement shown right can, with suitable adjustment of R_1 simply cancel the offending term. We achieved this with a value of R of approximately 15kΩ. This has the additional effect of reducing the carrier at v_o by approximately 30% but enabled one to increase the modulation depth to approximately 43%, v_m being 6.8V pk-pk. C and R_4 were retained for direct comparison but obviously do not help to give the max. obtainable.
Modulation depth of approximately 47% at v_o was achieved by increasing the positive supply to 12V. Alteration of the negative supply had little effect. No change in carrier amplitude was observed with this increased supply. One cannot guarantee this performance since the device is being driven outside the manufacturer's recommendations. Presumably if the alterations of modification no. 1 were used it would be the negative supply which would require alteration.

References

RCA applications notes ICAN5030.
Card 8, this set.
Low-cost 2-stage circuit forms versatile a.m. oscillator. 100 Ideas for Design, Hayden, 1966

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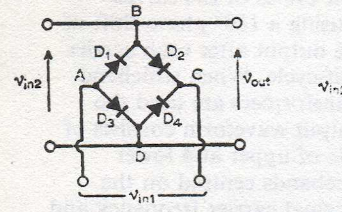
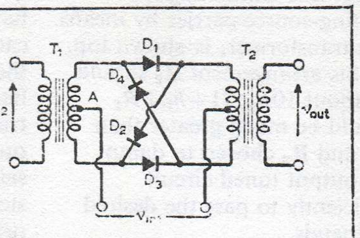
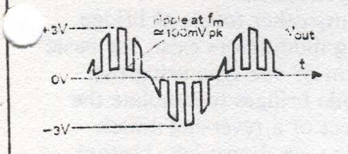
Set 22: Amplitude modulators—5

Diode bridge modulators

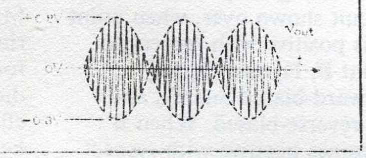




Typical performance
D_1 to D_4: PS101
V_{in1} carrier: 10V pk-pk sinewave at $f_c \approx 10$kHz, from 600-Ω source.
V_{in2} modulation: 6V pk-pk sinewave at $f_m \approx 200$Hz from 600-Ω source.
V_{out}: see waveform below.



Typical performance
D_1 to D_4: PS101; T_1, T_2: RS type T/T1, ratio 1:1
V_{in1} carrier: 1.2V pk-pk sinewave at $f_c \approx 4$kHz from 600-Ω source.
V_{in2} modulation: 2V pk-pk sinewave at f_m 200Hz from 600-Ω source.
V_{out}: see waveform below



Component changes
D_{1-4} Any general purpose, discrete or monolithic silicon, germanium or Schottky types.
A square-wave carrier source may be used in either circuit together with an output filter.
A floating source for carrier in Cowan modulator (left) can be simulated from grounded-type using a transformer.

Circuit descriptions and modifications
Both modulators are widely used at low carrier frequencies. In the Cowan arrangement diode switching in the bridge is under the control of the carrier alone provided that its amplitude is much greater than that of the modulating signal. Assuming this condition exists, then during the half-cycles of the carrier when point C is positive with respect to point A, the diodes will be reverse-biased and they present a high impedance shunted across the path between the modulation source and the output. When the carrier goes through its other alternate half-cycles, point A is positive with respect to point C, the diodes become forward-biased and the bridge provides a low-impedance shunt path across the modulation source. The higher frequency carrier voltage therefore causes the diode bridge to act as a single-pole single-throw switch which passes the modulating signal to the output during one half-cycle of the carrier and attenuates the modulation during the other half-cycle. As the magnitude of the modulating signal increases the carrier controlled switching of the diodes becomes less perfect (see waveform over) and a ripple appears on the output waveform at the modulation frequency. This

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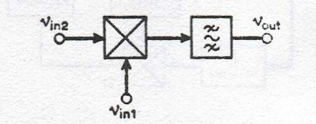
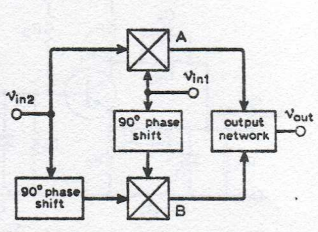
Set 22: Amplitude modulators—6

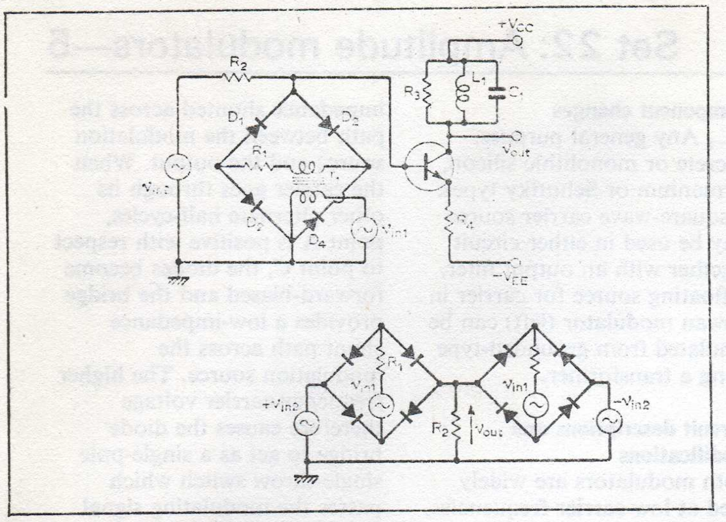
Single sideband generation

Filter method
A single-sideband signal can be produced by feeding the carrier v_{in1} and modulating signal v_{in2} to a balanced modulator to produce a double-sideband suppressed-carrier output which is then passed through a bandpass filter to select either the upper or lower sideband as required. The degree of carrier suppression depends on the design of the balanced modulator and the rate of cut—of the sideband filter, which must have a bandwidth equal to that of the baseband modulating signal. A number of different filter realizations may be used, their suitability depending on the carrier frequency at which the filtration is performed. The rise of L-C ladder filters is normally restricted to carriers in the approximate range of 20kHz to about 100kHz due to the relatively low Q-factor values obtainable with low-cost inductors. The much higher Qs obtainable with quartz crystals allow the design of bandpass filters using a lattice structure at frequencies above about 500kHz. Ladder-type mechanical filters provide much higher Qs than L-C resonant circuits, which give them excellent selectivity characteristics in a useful carrier range of about 50kHz to 1MHz. Ceramic elements using the piezo-electric effect, but having lower Q values than quartz crystals, can be used in a ladder structure over a carrier range of about 250kHz to 1MHz. Whatever the nature of the bandpass filter the same filter could be used to select either the upper





sideband or the lower sideband by shifting the carrier frequency to the appropriate edge of the filter response, assuming the filter to have a similar rate of cut at both of edges. The balanced modulator could be replaced by an amplitude modulator in certain applications, the degree of carrier suppression depending on the filter attenuation characteristic.
The unwanted sideband can be removed without the use of bandpass filters by means of phase shift techniques. The basic form of a phasing method s.s.b. generator is shown below. The carrier frequency is applied to balanced modulators A and B with a 90° phase shift introduced in one path. The modulating signal is also applied to both balanced modulators, to A directly and to B via a wideband 90° phase-shifting network. The output signals from the modulators, when combined, result in the suppression of one sideband. If the other sideband is required instead this can be achieved by reversing the phase of the carrier applied to one modulator, or by reversing the phase of the modulating signal to one modulator, or by reversing the output of one of



ripple is due to the larger-amplitude modulating signal causing some small amount of conduction on the diodes during their off state. When V_{in2} polarity makes point B positive with respect to point D a diode leakage path exists through D_2, the carrier source and D_3, and through D_1, the carrier source and D_4. When B becomes negative with respect to D. This modulator produces an output waveform containing the original modulating-frequency components and sets of upper and lower sidebands centred on the original carrier frequency and its harmonics, all of which are ideally suppressed. To remove all components except the sidebands around the original carrier frequency a band-pass filter must be incorporated at the output.

A simple method of achieving this filtration, at the same time isolating the output from the bridge and simulating the floating-source-carrier by means of a transformer, is shown top. In this arrangement R_2 should be about $10R_1$; $(1+h_{fe})\,R_4$ should be much greater than R_2, and R_3 chosen to damp the output tuned circuit sufficiently to pass the desired sidebands.

The double-balanced bridge-ring modulator obtained its name from its ability to suppress both the original modulating signal and the carrier from its output. Hence it is to be preferred to the Cowan modulator when the carrier frequency does not greatly exceed the highest modulating frequency. In the circuit shown over, when point A is positive with respect to point B, D_1 and D_3 are forward-biased and D_2 and D_4 reverse-biased. When B becomes positive with respect to A, D_2 and D_4 are forward-biased with D_1 and D_3 reverse-biased. Hence the modulating signal will pass from Tr_1 to Tr_2 over two different paths during alternate half cycles of the carrier causing a 180° phase shift of the output after each carrier half-cycle. When wideband transformers are used the output waveform consists of sets of upper and lower sidebands centred on the original carrier frequency and its harmonics, all of which are, ideally, suppressed.

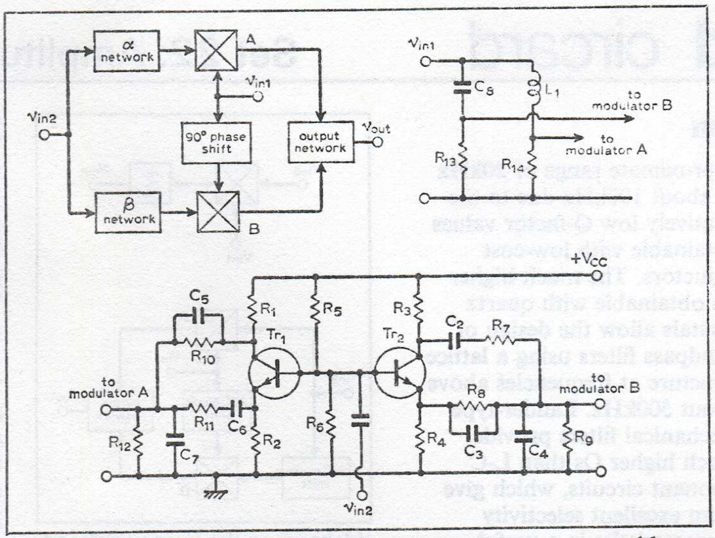
The output waveform shown over differs from the above due to the use of a.f. transformers with a 10-kHz carrier so that very little of the sidebands of harmonic carrier frequencies are present at the output due to transformer imperfections.

Many other forms of bridge ring modulators exist, the basic form of one type using two diode bridges to simulate the effect of a reversing switch being, as shown left, bottom.

the modulators. Of these methods the second is usually preferred due to the relative ease of inverting a.f. signals. In this method of s.s.b. generation, the modulating signals applied to both balanced modulators should ideally suffer by 90° over their complete frequency range whilst retaining equal magnitudes. This is virtually impossible to achieve in a single network as shown over, so practical forms use a pair of networks to more closely approach the ideal requirements as shown below.

The number of different networks that could be used to realize the α and β-networks is almost limitless, but to meet the required conditions over a range of frequencies indicates the need to combine an all-pass characteristic with a non-uniform time delay as a function of frequency over the required frequency range, which results in a type of ladder structure.

An example of such a



realization is shown above. This configuration is capable of maintaining the phase difference at the outputs to within about ±1° of the desired 90° phase difference over a frequency range of about 10:1. For the speech bandwidth of approximately 300Hz to 3kHz typical values are given below.

Supply +15V, Tr_1, Tr_2 general-purpose, reasonably well-matched silicon n-p-n transistors.

R_1, R_2, R_3, R_4 680Ω, R_5 15kΩ, R_6 6.8kΩ, R_7, R_{11} 1.775kΩ, R_8, R_{10} 10kΩ, R_9, R_{12} 4.02kΩ, C_1 100nF, C_2 45.9nF, C_3 8.2nF, C_4 21nF, C_5 32.4nF, C_6 181nF, C_7 83.1nF.

The required 90° phase shift between the carrier frequency inputs to the two balanced modulators can be achieved in a number of different ways, for example from a quadrature sinusoidal oscillator. A simple arrangement for a fixed carrier frequency using a parallel pair of L-R and C-R branches is shown right, the 90° phase shift occurring at the frequency where the inductive and capacitive reactances equal R_{14} and R_{13} respectively. For example with R_{13}, R_{14} 50Ω, C_8 8nF and L_1 20μH the carrier should be set to 397.89kHz with v_{in1} derived from a 600-Ω source.

Further reading

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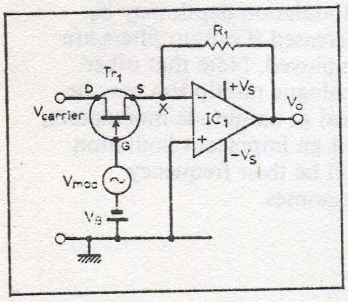
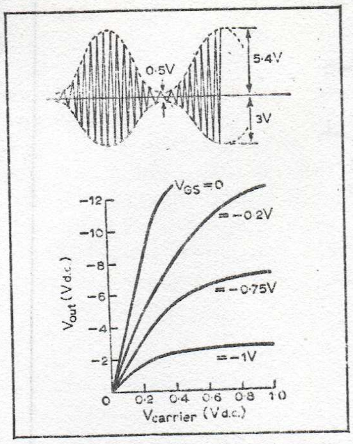
Betts, J. A. High-frequency communications, E.U.P., 1967, chapter 5.

FET modulators



Typical data
IC_1: 741, Tr_1: 2N5457
Supply: ±15V
R_1: 10kΩ
v_{mod}: 1V pk-pk $f_{mod} \approx$ 1kHz
$v_{carrier}$ 100mV pk-pk
$f_{carrier} \approx$ 10kHz
$\approx$ 0.75V
Output at v_o as shown top.
D.C. transfer function between input carrier and v_o, for varying V_{GS} of f.e.t., provides information on linear regions.

Circuit description
This circuit uses an n-channel junction f.e.t. in its voltage-controlled resistance mode, and hence the gain of the inverter-amplifier will be dependent on the slope resistance of Tr_1. The drain-source conductance g_{DS} of Tr_1 is fairly well defined by: $g_{DS} = 2I_{DSS}/-V_P + 2I_{DSS}V_m/V_P^2 = K_1 + K_2.V_m$ provided $|V_{DS}| < 100$mV. (I_{DSS} is the drain current for $V_{GS}=0$ and $V_{DS} = -V_P$). In this circuit, $V_{GS} = V_{mod} + V_B$, and if $V_B = |V_P|$, then $g_{DS} = (2I_{DSS}/V_P).(V_{mod}/V_P)$. The output from IC_1 is V_o and is $-R_1.g_{DS}.V_{carrier}$ hence $V_o = -R_1.2I_{DSS}/V_P^2.(V_{carrier})(V_{mod})$ i.e. proportional to the product of the carrier and modulation signals. Note that point x is a virtual earth point and $|V_{carrier}| = |V_{DS}|$. This restricts the carrier to a

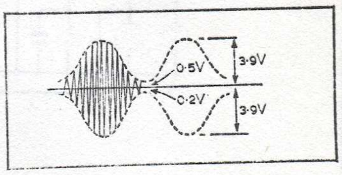


maximum of 100mV pk-pk to limit distortion. Positive values of V_{mod} much greater than $|V_P| + 0.7$V will forward-bias the gate-source junction, hence this determines the maximum allowable modulating signal.

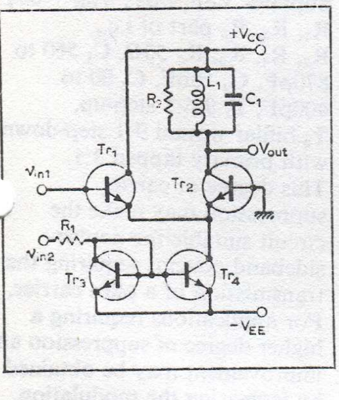
Component changes
R_1 10 to 20kΩ to provide increased output.

Carrier peaks can be equalized by biasing carrier with V_x, say. For $V_x = 29$mV, other parameters as before, output envelope is shown below.

Circuit modification
- Operational amplifier may be replaced by a single transistor in circuit over (see ref. 1). Output will contain a signal proportional to the carrier and modulating signal product which can be applied to a bandpass filter centred at f_c. C is large enough to be an a.c. short-circuit for the carrier frequency. I_E is chosen to make h_{ib} of the transistor small, given by $h_{ib} = 26/I_{E(mA)}$. This ensures that $v_{carrier} \approx v_{DS}$.

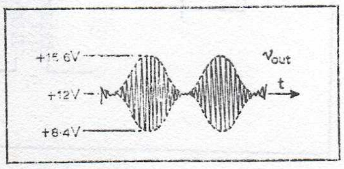


Long-tailed pair modulators



Circuit description
Circuit shown above is an example of an amplitude modulator having one input channel which is linear and the other channel highly non-linear. Although the multiplication from such a circuit is far from ideal, amplitude modulation can be obtained by applying the carrier to the non-linear input channel, applying the modulating signal to the linear input channel and taking the output across a bandpass filter centred on the carrier frequency. In this circuit the collector current of Tr_2 is a linear function of the common tail current but a highly non-linear function of the voltage between the bases of Tr_1 and Tr_2 due to the voltage drive from the carrier source to Tr_1 base. Transistors Tr_3 and Tr_4 form a current mirror that acts as a current source for the differential pair Tr_1 and Tr_2. Quiescent tail current is determined by R_1 with the single-ended (grounded) modulation source v_{in2} set to zero. This quiescent current is then varied by the modulating signal. The collector current of Tr_2 thus contains the modulating signal as well as

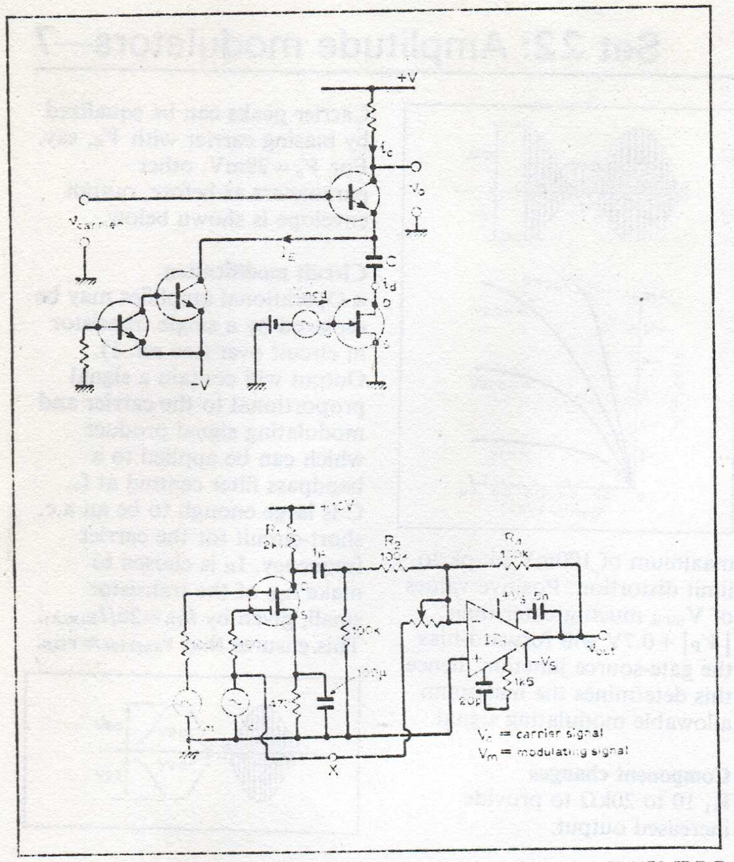
Typical performance
Supply: ±12V, ±2.7mA
Tr_1 to Tr_4: 1/5 of CA3086 (pin 13 substrate connected to $-V_{ee}$)
R_1, R_2: 4.7kΩ



the carrier and its sidebands, together with carrier harmonics and their sidebands due to the non-linear relationship between the collector current and the carrier drive voltage between Tr_1 and Tr_2 bases. To obtain an output amplitude-modulated wave the bandpass filter, in this case the parallel tuned circuit $L_1C_1R_2$, must have a sufficiently high loaded Q-factor to remove the modulation-frequency

L_1: 10μH, C_1: 1nF
v_{in1} carrier 100mV pk-pk sinewave at $f_c \approx$ 1.61MHz to produce unmodulated carrier output from tuned circuit of 3.6V pk-pk.
v_{in2} modulation 25V pk-pk (max) sinewave at $f_m \approx$ 1kHz to produce approximately 100% modulation depth output from tuned circuit.
v_{out}: see waveform left.

components and the harmonic carrier and sideband components. For the circuit shown the theoretical value of the centre-frequency for the tuned circuit is $f_0 = -1/2\pi\sqrt{L_1C_1}$ Hz = 1.592MHz which is within 1% of the value in practice. The loaded Q-factor is $Q_L = 2\pi f_0 R_2 C_1 = 47$ which provides a passband (to 3dB down points) having a width of $f_0/Q_L = 33.87$kHz which is suitable for audio



Also, since $i_d = g_{DS}.v_{mod}$ and $i_c = \alpha(I_E + i_d)$ then $v_o = V_{CC} - \alpha I_E.R_L - \alpha g_{DS}.R_L.v_{carrier}$. This provides, an a.c. product of $2\alpha R_L\, I_{DSS}/V_P^2 \times (v_{carrier})$ (v_{mod}). Similar limitations to levels apply in this circuit (α common base current gain).

● Figure (bottom) comprises a combination of a dual gate m.o.s.f.e.t. and inverting amplifier.
Tr_1 40841, IC_1 SN72709, supply ±12V.
For double-sideband suppressed-carrier operation, the carrier is fed forward through R_4.
If $v_{mod} \gg v_{carrier}$, then gain V_{DS} is given by $-(K_1 + K_2 v_{mod}).R_1 v_C$ i.e. $V_{DS} = -K_1 R_1 v_c - K_2 R_1 v_m.v_c$.
Provided $(R_4/R_3)v_c = (R_4/R_2)K_1 R_1 v_c$, then the above condition is obtained, i.e. v_{out} is proportional to the product of the two signals.
To obtain amplitude modulation the circuit is opened at X. Modulation depth must be limited to around 60%. At these levels of carrier and modulating signals where v_m is no longer much greater than v_C the g_m of the f.e.t. is a function of both signals causing unwanted harmonics.
Modulation depth may be increased if output filters are employed. Note that other analogue multipliers may be used as amplitude modulators, but an important limitation will be their frequency responses.

Further reading

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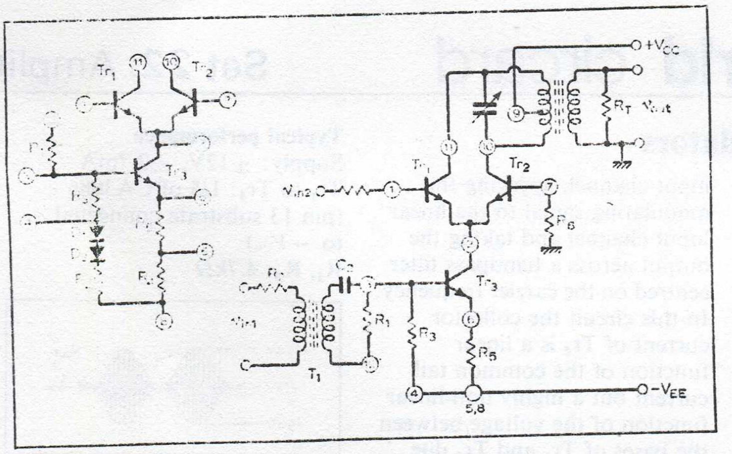
Ideas for design, *Electronic Design*, January 4, 1973, p.98.

Cross reference

Set 22, card 1.

modulation, up to 15kHz. By suitable choice of L_1 and C_1 carrier frequencies up to about 100MHz may be used, with adjustment of Q_L by means of R_2 to provide a suitable bandwidth for the highest modulating frequency.
Whereas the above circuit is formed by interconnecting the monolithic individual transistors to produce the long-tailed pair, other integrated circuits are manufactured in the long-tailed pair configuration. Examples of these are the CA3004, CA3005 and CA3006 the last type being particularly suited to use as a balanced modulator due to the small input offset voltage (typically 1mV). The internal structure of this integrated circuit is shown left. The i.c. consists of a well-balanced differential-input amplifier Tr_1 and Tr_2 fed from a constant-current source Tr_3. Due to the versatile biasing arrangements a number of different operating modes may be used but pin 8 must be connected to the most negative



direct voltage in the circuit and pin 9 to the most positive direct voltage used. Pin 12 is normally connected to ground.
A typical balanced modulator circuit using this integrated circuit is shown above.
In this application, the diodes R_2 and R_4 of the integrated biasing network are short-circuited, the modulating signal is applied between the differential pair bases v_{in2} and the carrier applied to the base of the constant-current transistor Tr_3 via transformer T_1. The differential-output double-sideband suppressed-carrier signal between Tr_1 and Tr_2 collectors is converted to a single-ended output by the tuned transformer T_2 which suppresses the unwanted output components. Attention should be paid to careful printed circuit layout and screening to obtain the best performance.
Typically the carrier suppression is around 25dB below the wanted double-sideband output when v_{in2} is adjusted to produce 16mV r.m.s. at pin 1 and v_{in1} adjusted to produce 31.5mV r.m.s. across the primary winding of T_1 at a frequency of 1.75MHz. Typical values: Supplies V_{CC} +6V, V_{EE} −6V, R_1, R_3, R_5 part of i.c., R_2, R_4, R_6, R_7 50Ω, C_1 560 to 870pF, C_2 10nF, C_3 90 to 400pF, T_1 9.6:1 step-up, T_2 bifilar wound 9:1 step-down with primary tapped 3:1.
This degree of carrier suppression may make the circuit suitable for double-sideband systems requiring the transmission of a pilot carrier.
For applications requiring a higher degree of suppression an improvement may be obtained by increasing the modulation signal input and decreasing the carrier input voltage.

Further reading

Clarke, K. K. & Hess, D. T. Communication circuits: analysis and design, Addison-Wesley, 1971, chapters 3, 4 & 8.
RCA Solid-State Databook SSD-201B, 1973, pp.183-8.

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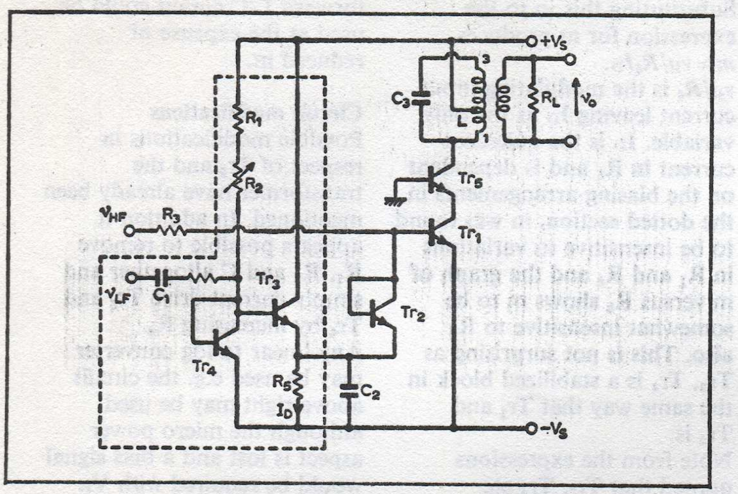
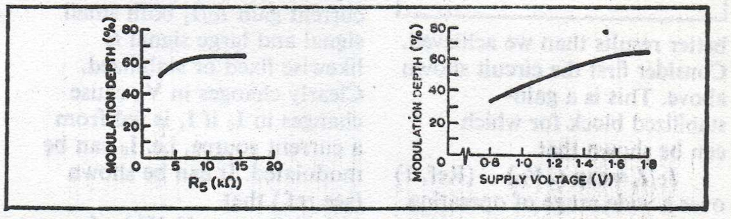
Set 22: Amplitude modulators—9

Micropower amplitude modulator



Components
R_1: 33kΩ, R_2: 5kΩ
R_3: 1MΩ, R_4: 5.6kΩ
R_5: see graph
R_6: 10kΩ load resistor

C_1: 47μF, C_2: 1.5nF
C_3: 250pF, L: 490μH (total)
C_3 and L tuned for 460kHz
Transistors from CA3086 i.c.



Performance
V_s was set to 1.5V, v_{lf} to zero and the carrier frequency adjusted to give maximum v_o; this occurred at about 460kHz. v_{lf} was then adjusted to give maximum modulation depth, m, and R_5 was varied. It was found that maximum m occurred at 1V pk-pk for v_{lf} for all R_5. The resulting graph of m versus R_5 is shown above centre. Higher values of R_5 produced non-linear modulation and lower values gave a rapidly diminishing value of m. Maximum carrier amplitude was 1.32V pk-pk with R_5=15kΩ. The modulating frequency was 400Hz and linear modulation was maintained over the frequency range 10Hz to 1kHz typical. Maintaining R_5 at 6.8kΩ, the frequency of v_{lf} at 400Hz, and altering the magnitude of v_{lf} at all points to produce maximum m produced the graph of m versus V_s, above right. The lower limit of 0.8V was chosen as being that of the end-of-life voltage of a dry cell. The corresponding range of v_{lf} was 0.48 to 1.25V pk-pk. Power consumption is less than 500μW throughout the voltage range; considerably so at the lower end.

Circuit description
This circuit is due to Venkateswavlu & Sonde (see ref.) who claim slightly

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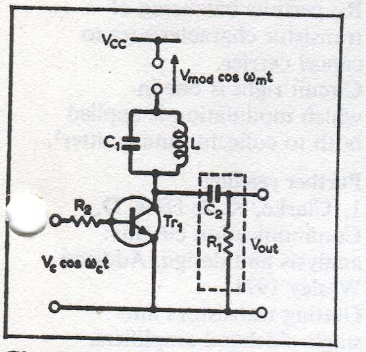
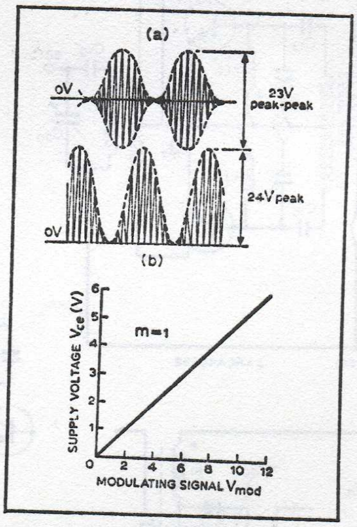
Set 22: Amplitude modulators—10

Direct tuned-circuit modulator



Circuit description
This circuit demonstrates the principle that may be used to perform the initial modulation of a carrier signal, which may then be used to drive a power amplifier. Transistor Tr_1 is driven hard into conduction once every carrier-cycle so that its base-collector junction is forward biased. The related collector current pulses excite the tank circuit LC_1 which is tuned to the carrier frequency which therefore rings between pulses at a frequency f_c. The waveform at the transistor collector or across the tuned circuit is shown opposite at (b). The envelope is approximately the superposition of $V_{CC}+v_{mod}$ and is of the form $(V_{CC}-V_{CEsat})(1+m\cos\omega_m t)$ where the modulating index $m=v_{mod}/(V_{CC}-V_{CEsat})$
To maintain approximately 100% modulation for variation of Vcc, the modulating signal is linearly related as shown in graph.

Circuit notes
- Tuned circuit Q in the range 30 to 50.
- Filter circuit (high pass) of C_2R_1 provides useful demonstration technique only. Normally output coupled out via tapped-down transformer

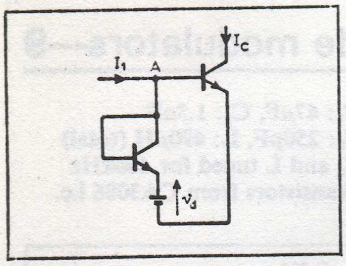


where L is the primary.
- R_1 value chosen empirically to minimize phase shift of positive and negative carrier peaks of waveform.
- Frequency range of modulating signal 1Hz to 20kHz, but some reduction in R_1 is necessary at the higher frequency to maintain symmetry of waveform.

Applications
In certain situations, a.m. is performed at low power levels, and power levels suitable for transmission are developed by power amplifiers. An example of such a circuit is shown over[3], top. To preserve a wideband performance a push-pull configuration of Tr_1, Tr_2 minimizes unwanted harmonic content. Typical performance data:

Vcc: 12.5V
Peak envelope power: 40W
Modulation: 95%
Carrier frequency: 118 to 136MHz
Carrier input power: 5mW.

A similar concept but at a low power is described in the circuit[4] shown over, bottom. Typical output 100mW depending on transistor at a



better results than we achieved. Consider first the circuit shown above. This is a gain-stabilized block for which can be shown that

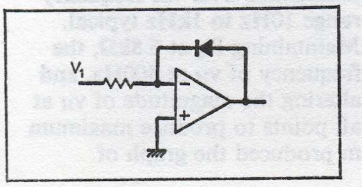
$I_C/I_1 \approx \exp(\lambda V_D)$ (Ref. 1)

over a wide range of operating conditions (λ having the usual connotation). To understand the circuit in a simplified manner assume that both base currents are negligible. Both transistors are governed by the same exponential relationship such that for a given Δv_{be} (which must be the same for both transistors) the collector currents change by the same percentage. Hence, if V_d sets different initial values of collector currents, which it will, a signal V at A will result in the same ratio of a.c. to d.c. in each transistor. As the direct current ratio is fixed by V_d (at e.g. 10:1), the ratio of a.c. is also fixed and since the collector current of the diode connected transistor is approximately equal to the input current I_1, then the current gain I_C/I_1 both small signal and large signal is likewise fixed or stabilized. Clearly changes in V_d cause changes in I_c if I_1 is fed from a current source, i.e. I_c can be modulated. It can be shown (see ref.) that

$m = \Delta i_c/i_c = \exp(\lambda \Delta V_d) - 1.$

The above block can be seen in the main diagram in the form of Tr_1 and Tr_2. V_d is produced across R_5, C_2 simply acting as a short to carrier frequency signals. The section of the main diagram enclosed by the broken line is, after a fashion, a mirror image of the gain-stabilized block and produces

$\Delta V_d \approx (1/\lambda)\ln(1 + v_{it}/R_4 I_D)$



Substituting this in to the expression for m produces

$m \approx v_{it}/R_4 I_D$.

v_{it}/R_4 is the modulating input current leaving I_D as the only variable. I_D is the quiescent current in R_5 and is dependent on the biasing arrangements in the dotted section. m was found to be insensitive to variations in R_1 and R_2 and the graph of m versus R_5 shows m to be somewhat insensitive to R_5 also. This is not surprising as Tr_3, Tr_4 is a stabilized block in the same way that Tr_1 and Tr_2 is.

Note from the expressions quoted that Tr_3, Tr_4 etc comprises a linear-log converter and Tr_1 and Tr_2 effectively take the anti-log. Tr_5 is a cascaded transistor to improve the voltage gain characteristics and may be omitted at the expense of reduced m.

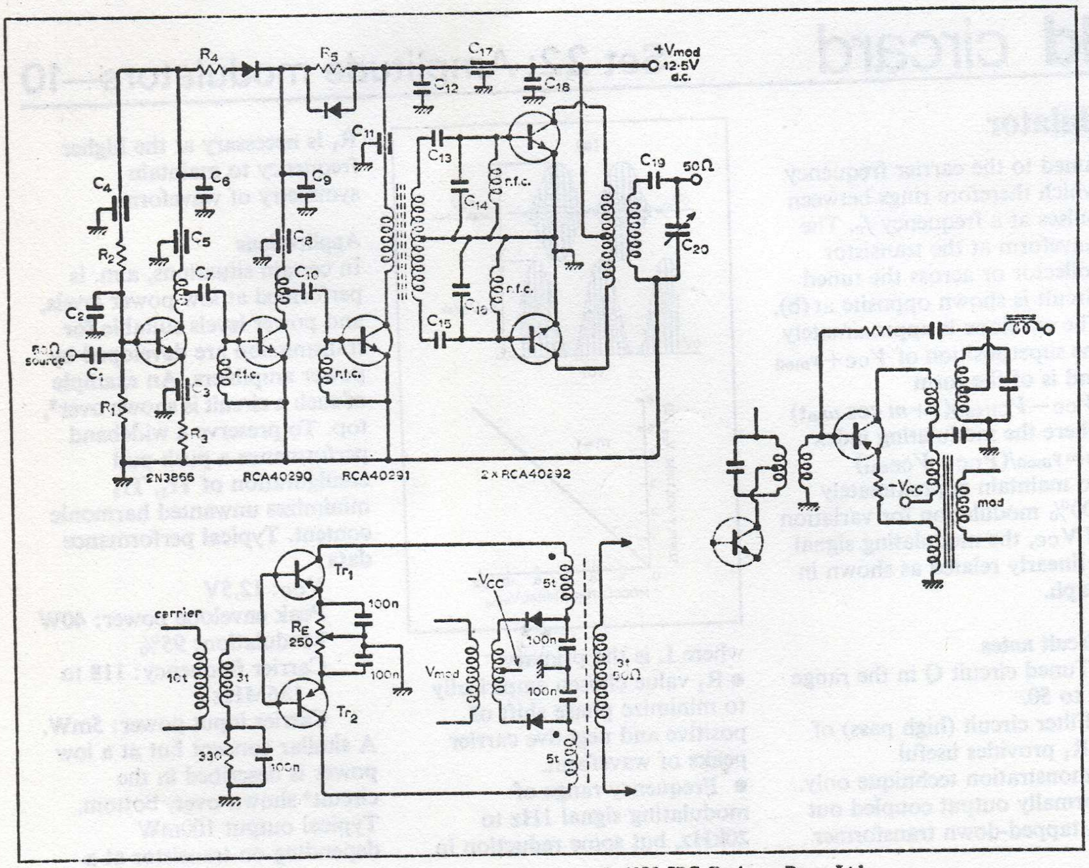
The tapped transformer is included to minimize the loading effect of R_L, again improving voltage gain characteristics. A straightforward L-C circuit could be used at the expense of reduced m.

Circuit modifications

Possible modifications in respect of Tr_5 and the transformer have already been mentioned. In addition it appears possible to remove R_1, R_2 and C altogether and simply current drive Tr_3 and Tr_4 by increasing R_4. Any linear to log converter may be used e.g. the circuit above right may be used although the micro power aspect is lost and a bias signal would be required with V_1.

Reference

Venkateswavlu, V. & Sonde, B. S. Micropower amplitude modulator, *Proc. IEEE*, July 1971, pp.1114-6.



carrier frequency of 27MHz (US citizens band). Collectors are supplied push-pull, but the bases are paralleled, as distinct from above circuit. R_E permits balancing of transistor characteristics to cancel carrier.

Circuit right is one in which modulation is applied both to collector and emitter[5].

Further reading

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Getting transistors into single-sideband amplifiers. Motorola application report AN-150.
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Cross reference

Set 7, card 6.