Unijunction voltage-to-frequency converter

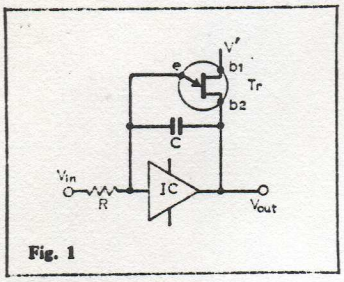


Fig. 1

Components
IC: 741, ±15V supplies
Tr: 2N2646
C: 10nF
R: 100kΩ
V′: 3.3V
V_{in}: see graph
V_o: see graph

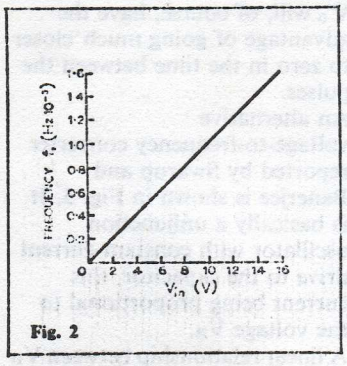


Fig. 2

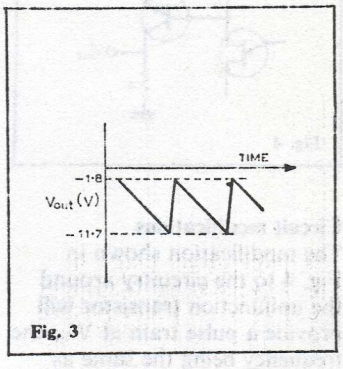


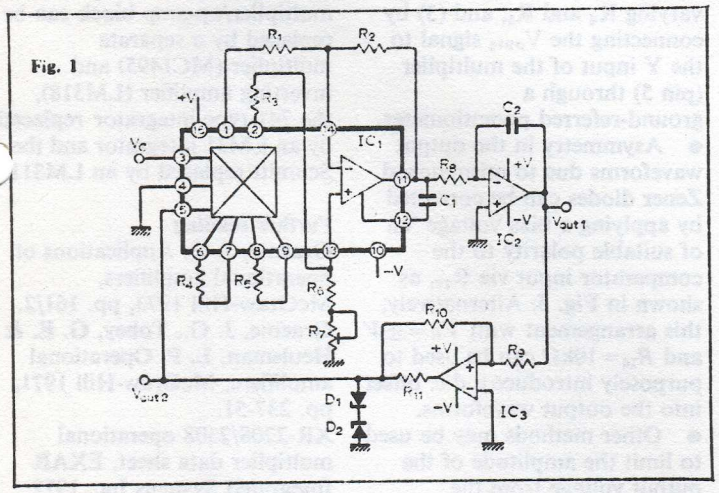
Fig. 3

Circuit description
With the removal of the unijunction transistor the circuit of Fig. 1 is simply an integrator which, with a positive V_{in}, gives a negative-going ramp V_o. If the i.c. gain is sufficiently high then V_o is $-V_{in}t/RC$. The unijunction serves to discharge the capacitor each time the voltage between e and b_1 reaches the unijunction trigger voltage. The circuit therefore goes through the cycle shown right. Lower limit of −1.8V is the voltage at which the unijunction reverts to being an open circuit. Upper limit of −11.7V is arbitrary and is the result of choosing V′, R and C so that V_{in}=10V gave a frequency of 1kHz. With ±15V supplies this obviously cannot be extended beyond 15V.
The degree of linearity in the plot of frequency against V_{in} shown in Fig. 2 is quite high e.g. 10V gave 1kHz, 5V gave 498Hz, 1V gave 96Hz and 0.15V gave 16Hz.
Rise time of the output waveform (Fig. 1 circuit gave the waveform of Fig. 3) corresponding to the time when C is discharging, was 15μs i.e. 1.5% of the period at 1kHz, so the circuit cannot be recommended for much higher frequencies.
But from the expression for the downward ramp it is clear that the same frequency range can be achieved by the use of different values of R and C, and also of V′. It will, of course, be generally desirable to keep R relatively high to give high input impedance.

▶

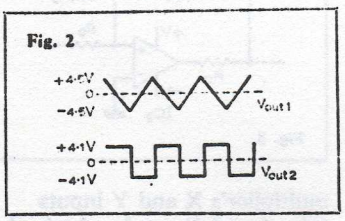
Multiplier voltage-to-frequency converter

Fig. 1



Typical performance
Supplies: ±15V, ±8.5mA
IC_1 XR2308 IC_2, IC_3 741
D_1, D_2 3.3V Zeners R_1, R_3 22kΩ
R_2, R_6 330kΩ R_4, R_5 68kΩ
R_7 100kΩ R_8, R_9, R_{10} 10kΩ
R_{11} 2.2kΩ C_1 22pF, C_2 1nF
See Fig. 3 for graph of f/V_c and Fig. 2 for waveforms.

Fig. 2



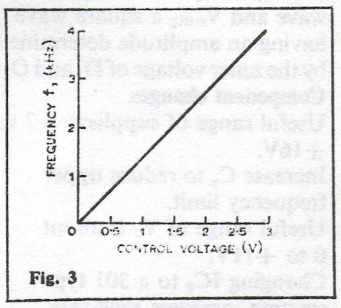


Fig. 3

Circuit description
The circuit of Fig. 1 is basically a closed-loop integrator-comparator square-triangle generator, comprising IC_2 and IC_3, with a multiplier (IC_1) inserted in the loop to provide control of frequency. The value of the output voltage from the multiplier is a scaled version of the product V_{out_2} and the control voltage V_C. Thus the amplitude of the signal to be integrated is directly proportional to a scaled value of the control voltage. A positive voltage applied to the inverting integrator charges C_2 with its output end negative relative to the input end (held close to 0V by negative feedback through C_2 and the high gain of IC_2). Thus, V_{out_1} goes negative until the current it feeds through R_9 exceeds the positive current in R_{10}, resulting in a negative current to the non-inverting input of the Schmitt comparator. V_{out_2} then rapidly switches to a negative value due to positive feedback applied to IC_3, causing the multiplier output to go negative (V_c is always positive). The output from the integrator then starts rising until it reaches a positive voltage sufficient to make the comparator change

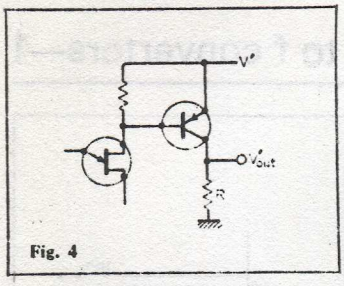


Fig. 4

Circuit modifications

The modification shown in Fig. 4 to the circuitry around the unijunction transistor will provide a pulse train at V'_o, the frequency being the same as that of the main circuit. The leading edge of this pulse train will correspond to the rising edge of V_o shown in Fig. 3. This V'_o will, of course, have the advantage of going much closer to zero in the time between the pulses.

An alternative voltage-to-frequency converter reported by Swarup and Banerjee is shown in Fig. 5. It is basically a unijunction oscillator with constant-current drive to the capacitor, this current being proportional to the voltage V_B.

A linear relationship between V_B and the output frequency is claimed in the range 0 to 500Hz. The basic action of the unijunction oscillator and modifications to reduce the discharge time of C are fully described in Circards set 3 (waveform generators) card 4.

Reference

Swarup & Banerjee, Linear voltage to frequency and voltage to pulse width converters using unijunction transistors. *Int. J. Electronics*, vol. 32, 1972, pp. 377-81.

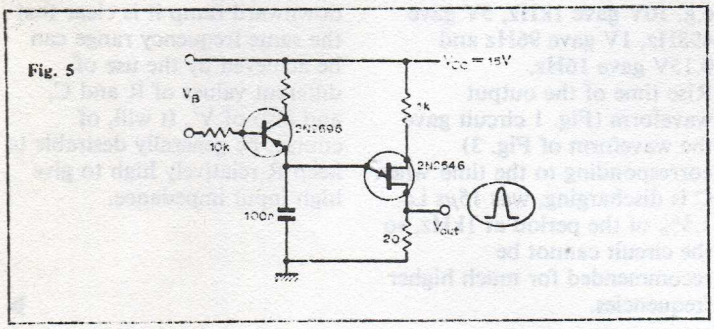


Fig. 5

its state again, returning V_{out_2} and the multiplier output to their original positive values. Hence, V_{out_1} is a triangular wave and V_{out_2} a square wave having an amplitude determined by the zener voltage of D_1 and D_2.

Component changes

Useful range of supplies: ±7 to ±16V.

Increase C_2 to reduce upper frequency limit.

Useful range of V_c is about 0 to +11V.

Changing IC_3 to a 301 type op-amp increases slew-rate capability.

R_9 can have a wide range of values the lower limit being imposed by heavy loading of IC_2 and the upper limit by the failure of IC_3 to switch before it saturates.

Circuit modifications

- Accuracy of frequency control largely depends on the nonlinearity and offset voltages in the multiplier part of the loop. Output offset adjustment is provided by R_7 and independent adjustment of the offset voltages at the multiplier's X and Y inputs (pins 3 and 5) can be obtained by the 25-kΩ potentiometers R_{12}, R_{13} shown in Fig. 4, where R_{14}, R_{15} are 100kΩ.
- For a given value of control voltage frequency depends on the scale factor of the multiplier. Adjusting this allows the output frequency to be made a simple linear function of V_c. The factor can be adjusted in three ways: (1) by adjusting the op-amp gain in the multiplier block by means of R_2, (2) by adjusting the gain of the multiplier block by varying R_4 and R_5, and (3) by connecting the V_{out_2} signal to the Y input of the multiplier (pin 5) through a ground-referred potentiometer.
- Asymmetry in the output waveforms due to mismatched Zener diodes can be corrected by applying a bias voltage V_B of suitable polarity to the comparator input via R_{16}, as shown in Fig. 5. Alternatively, this arrangement with $V_B = \pm V$ and $R_{16} = 10k\Omega$ can be used to purposely introduce a d.c. offset into the output waveforms.
- Other methods may be used to limit the amplitude of the output voltage from the comparator, e.g. by using a diode bridge limiter or by replacing IC_3 with an op-amp of the type providing access to the drive point of its output stage, such as a 748. This allows the comparator output to be clamped by zener diodes or suitably-biased transistors connected to the output stage drive point.
- For higher frequency operation the multiplier/op-amp block can be replaced by a separate multiplier (MC1495) and inverting amplifier (LM318), the 741-type integrator replaced by an LM31 integrator and the Schmitt replaced by an LM311

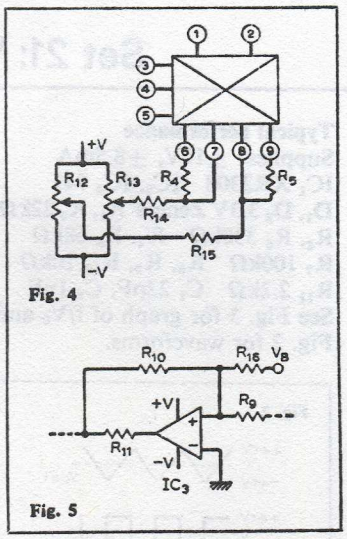


Fig. 4

Fig. 5

Further reading

Graeme, J. G. Applications of operational amplifiers, McGraw-Hill 1973, pp. 161/2.

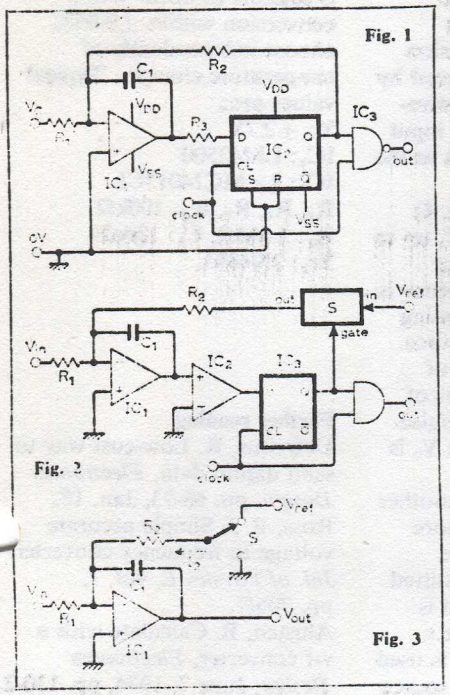
Graeme, J. G., Tobey, G. E. & Heulsman, L. P. Operational amplifiers, McGraw-Hill 1971, pp. 237-51.

XR-2208/2308 operational multiplier data sheet, EXAR Integrated Systems Inc. 1972.

Cross references

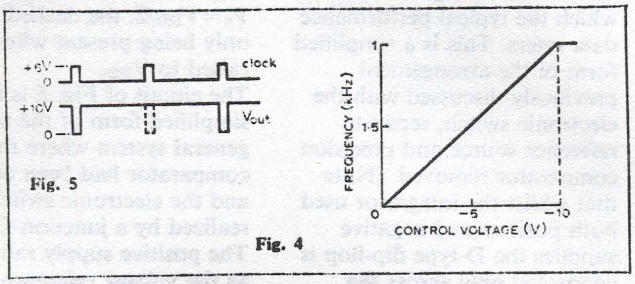
Set 2, card 1
Set 3, cards 1, 5
Set 13, card 9
Set 17, cards 3, 6
Set 21, card 4

Delta-sigma voltage-to-frequency converter



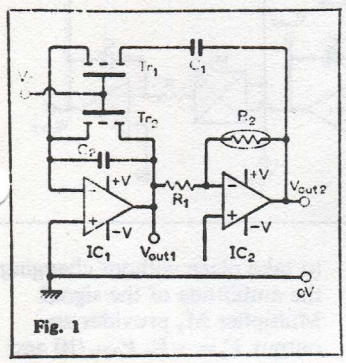
Typical performance of Fig. 1
IC_1: 741, IC_2: $\frac{1}{2}\times$CD40134E,
IC_3: $\frac{1}{4}\times$CD4011AE
Supplies: V_{DD}: +10V, V_{SS}: −10V
R_1, R_2: 100kΩ,
R_2: 1kΩ,
C_1: 100nF
Clock: 6V positive pulses,
p.r.f.: 1kHz, duty cycle: 10%
See Figs 4 and 5.

Circuit description
A class of voltage-to-frequency converter gives an output in the form of a pulse train where the repetition frequency is directly proportional to the instantaneous value of the control voltage but the pulses are generated asynchronously. The output from a delta-sigma encoder is again a pulse train but its average pulse repetition frequency is proportional to the control voltage and the pulses are generated in synchronism. with a clock pulse waveform.



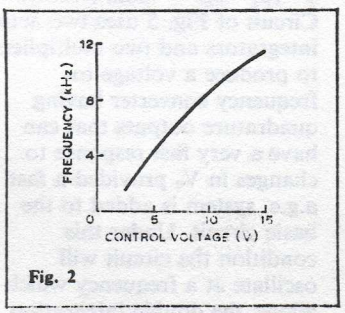
The basic form of a delta-sigma modulator is essentially a voltage-to-pulse ratio converter (Fig. 3). The circuit maintains a constant voltage across C_1 as the input voltage is varied, which requires that the charging current from the voltage reference source to be switched into C_1 at a repetition rate that attempts to keep the net change in voltage across C_1 at zero. Thus the rate at which the reference current must be switched into the capacitor must be proportional to the input voltage. If the reference current is switched under the control of a stable clock-pulse generator the output pulses will be proportional to V_{in} and synchronized with the clock pulse source. Assuming that the net voltage across C_1 is zero, that V_{in} is negative, that V_{ref} is positive and IC_1 is a high-gain op-amp then $I_1=I_2$, V_{out} (mean) $=0$ and I_{out} (mean)$=0$. As the

Sinewave voltage-to-frequency converters

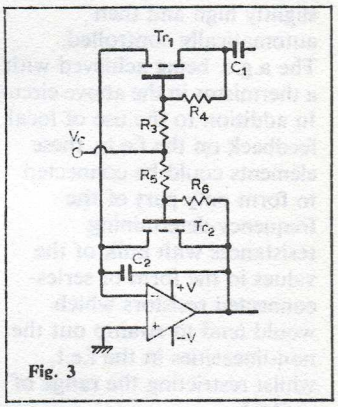


Typical performance
Supplies: ±15V
IC_1, IC_2: 741,
Tr_1, Tr_2: 1/6×CD4007AE
R_1: 150Ω,
R_2: thermistor type R13
C_1, C_2: 100nF
V_{out1}: 520mV pk-pk
V_{out2}: 1.04V pk-pk
See graph for f/V_c (Fig. 2)

Circuit description
This circuit (Fig. 1) is one of the many forms of Wien bridge oscillators with Tr_1 and C_1 forming the series-connected frequency-dependent arm with Tr_2 and C_2 forming the parallel connected arm of the bridge. For oscillation to occur the closed-loop gain must be unity, the required amount of gain being provided by the inverting



operational amplifier IC_2, the gain being determined by the ratio R_2/R_1. With this configuration the common-points of the frequency-determining resistors are connected to the virtual-earth inverting input of IC_1. This is a convenient arrangement for replacing these resistors with elements which have a resistance that can be controlled by a ground-referred voltage source. In the above circuit these elements take the form of a pair of matched c.m.o.s. transistors which have gate-source resistances that depend on the control voltage V_c. Linearity of the voltage-to-frequency conversion characteristic is not particularly good over a wide range of frequencies but may be adequate for many purposes where only a restricted frequency range is required. Resistance of the f.e.ts



depends on their drain-source signal voltages as well as on the control voltage V_c but this can be reduced, and the linearity of f.e.t. resistance-to-control voltage characteristic linearized, by using local feedback around the f.e.ts as shown in Fig. 3, where R_3, R_4, R_5 and R_6 may be of the order of 1MΩ.
If the closed-loop gain deviates from unity the amplitude of

inverting input of IC_1 is a virtual earth, $I_1 = V_{in}/R_1$ and $I_2 = kV_{ref}/R_2$ where k is pulse duty cycle required to keep $I_2 = I_1$. Equating these currents gives

$$\frac{V_{in}}{R_1} = k\frac{V_{ref}}{R_2},$$

where k is the ratio of the output pulse repetition rate (f) to the clock pulse repetition rate (f_c). Hence

$$f = \left(\frac{R_2 f_c}{R_1 V_{ref}}\right) V_{in}.$$

By making $R_2 = R_1$ and $V_{in(max)} = V_{ref}$ the maximum output p.r.f. is that of the clock source and the average output pulse rate is proportionally smaller for smaller values of V_{in}.

The arrangement of Fig. 2 uses an analogue transmission gate to realize the switch S. IC_2 is a precision comparator which determines when the reference voltage source is to be switched to R_2 by monitoring the polarity of the output from the integrator IC_1. This switching

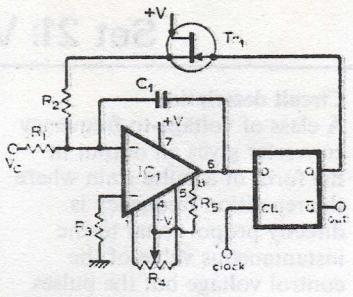


Fig. 6

action is synchronized to the clock pulses by using gating pulses derived from the output of a D-type flip-flop which receives the comparator's output at its data input.

The circuit of Fig. 1 is that to which the typical performance data refers. This is a simplified form of the arrangement previously discussed with the electronic switch, separate reference source and precision comparator removed. (Note that whilst the integrator used both positive and negative supplies the D-type flip-flop is connected only across the positive supply.) As the D-type produces output pulses equal in amplitude to the V_{DD} rail voltage only when its data input receives a positive pulse from the integrator, a separate switched reference is not essential. Also, the precision comparator can be replaced by R_3 which limits the negative-going pulses to the data input of the D-type which acts as the comparator. Average frequency/V_c graph (Fig. 4) has a linearity of $\pm 0.1\%$ up to $f = f_c$ when $V_c = V_{DD}$. No further increase in frequency is possible except by increasing the p.r.f. of the clock source.

Output pulse waveform of Fig. 5, inverted by IC_3, is of $V_c = V_{DD}/2$, the dashed pulse only being present when V_c is raised to V_{DD}.

The circuit of Fig. 6 is another simplified form of the more general system where the comparator had been omitted and the electronic switch is realized by a junction f.e.t. The positive supply rail is used as the voltage reference source and the output is taken from the $\bar{Q}$ terminal of the D-type flip-flop IC_2, which is a complementary m.o.s. version to conserve power. This circuit is capable of linear v-to-f conversion within $\pm 0.05\%$ almost independently of temperature changes. Typical values are:

V: ± 2.7V
IC_1: LM42500
IC_2: $\frac{1}{2} \times$ MC14013CL
R_1, R_2, R_3, R_4: 100kΩ
R_5: 5.6MΩ, C_1: 100nF
Tr_1: 2N4693.

Further reading

Defreitus, R. Low-cost way to send digital data, *Electronics Design*, pp. 68-73, Jan. 18.

Ross, P. J. Simple accurate voltage to frequency converter. *Jnl. of Physics E*, vol. 7, pp. 706/7.

Alusten, B. Calculate with a v-f converter, *Electronics Design*, June 7, 1974, pp. 130-2.

oscillation will vary with time, so to avoid extremely precise setting of gain it is initially set slightly high and then automatically controlled.

The a.g.c. being achieved with a thermistor in the above circuit.

In addition to the use of local feedback on the f.e.ts, these elements could be connected to form only part of the frequency-determining resistances with bulk of the values in the form of series-connected resistors which would tend to swamp out the non-linearities in the f.e.t. whilst restricting the range of control.

The f.e.ts could be replaced by matched photoconductive resistors or by bipolar transistors which are switched on and off by current pulses to the bases, the mean collector-emitter resistance being controlled by the pulse repetition frequency.

A voltage-to-frequency converter using a pair of all-pass active networks is shown in Fig. 4. These

Fig. 4

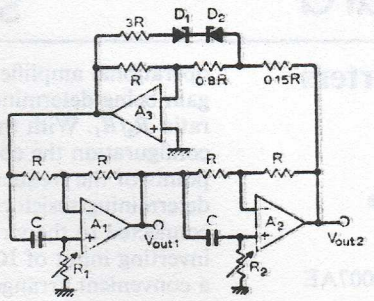
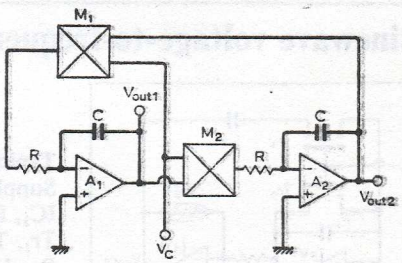


Fig. 5



networks, using A_1 and A_2, have a constant gain magnitude but a phase shift given by $\phi_1 = -2\tan^{-1}(\omega CR_1) - 180°$ and $\phi_2 = -2\tan^{-1}(\omega CR_2) - 180°$ respectively. With the 180° phase shift through the a.g.c. amplifier A_3 the current will oscillate at a frequency $1/(2\pi C\sqrt{R_1R_2})$Hz, which shows that a voltage-to-frequency conversion may be obtained by making R_1 or R_2 or both voltage-dependent resistors, e.g. f.e.ts. For a wide range of frequency variations R_1 could be a voltage-dependent resistor and R_2 a range-switching resistor. For $R = R_1 = R_2$ the outputs are generated with a controllable phase difference $\phi = (\phi_1 - \phi_2) = -2\tan^1(\omega CR)$.

Circuit of Fig. 5 uses two active integrators and two multipliers to produce a voltage-to-frequency converter having quadrature outputs that can have a very fast response to changes in V_c provided a fast a.g.c. system is added to the basic circuit. Under this condition the circuit will oscillate at a frequency which allows the double integration to take place without changing the amplitude of the signal.

Multiplier M_2 provides an output $V_2 = +V_c.V_{out1}/10$ and M_1 gives an inverted output, to maintain the loop phase shift, of $V_1 = -V_c.V_{out2}/10$. With the 1/10 scaling factor, frequency of oscillation is $V_c/20\pi RC$. Multiplier M_1 could be replaced by an inverting operational amplifier.

Further reading

Von Ow, H. P., Reducing distortion in controlled attenuators using FETS. *Proc. IEEE*, 1968, pp. 1718/9.

Multiphase voltage-to-frequency converter

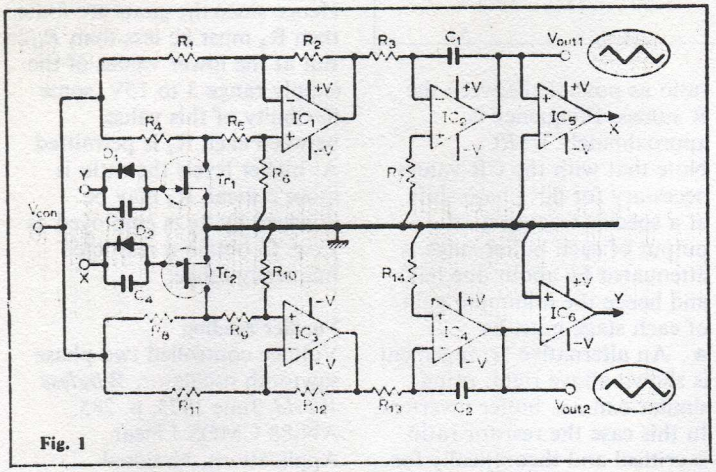


Fig. 1

Typical data
IC_1 to IC_6: 74IC
Tr_1, Tr_2: 2N5457
R_1, R_{11}: 20kΩ
R_2, R_3, R_{12}, R_{13}, R_6, R_7, R_{10}, R_{14}: 10kΩ
R_4, R_5, R_8, R_9: 2.7kΩ
C_1, C_2: 47nF
C_3, C_4: 68pF
D_1, D_2: 1N914

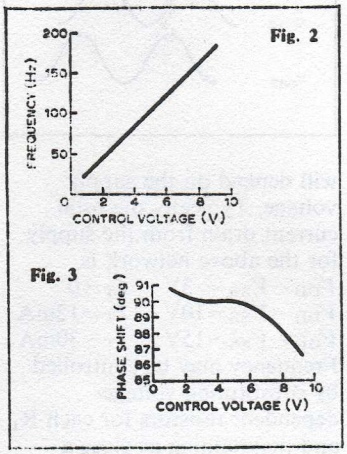


Fig. 2

Fig. 3

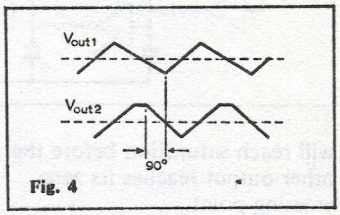
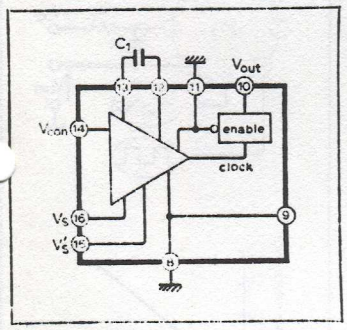


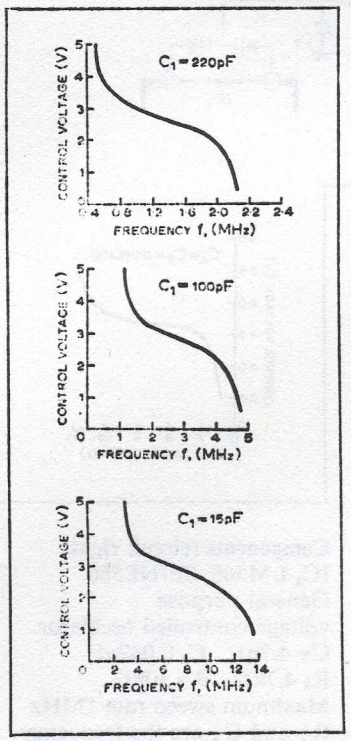
Fig. 4

Circuit description
This is a twin circuit based on R-C integration to provide the triangular waveform and level sensing to provide a square wave which operates an electronic switch controlling polarity applied to the integrator. Outputs X and Y are cross-connected giving control of electronic switches Tr_2 and Tr_1 respectively and triangular waveforms which are 90° out of phase. IC_5 and IC_6 provide high open-loop gain, and at low frequencies provide faster switching than comparators. V_{out1} is a positive-going ramp until Tr_1 changes state and this occurs at the instant of zero-crossing of V_{out2}, which then switches IC_6. V_{out1} then ramps down and changes the state of Tr_2 when a zero-crossing point is reached. The time taken to go from say a positive peak to zero level depends on the RC time constant and the value of $V_{control}$. It should be noted that as no amplitude controls for the output are imposed, one or other of the integrators

Monolithic voltage-to-frequency converters

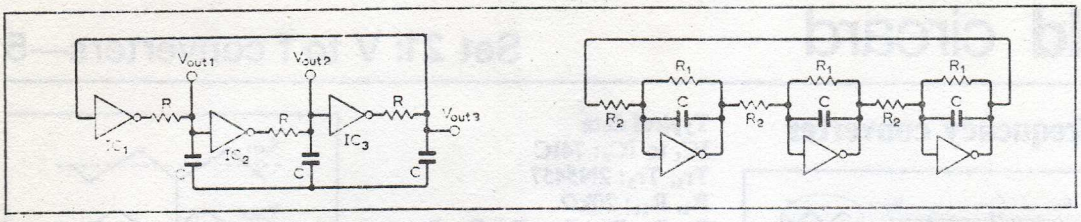


Typical data
IC ½SN74S124N
C_1 220pF
$V_s = V'_s = +5$V d.c.
Frequency range 0.7 to 1.8MHz (approx. linear)



Circuit description
An emitter-coupled astable multivibrator uses a single capacitor for timing. The circuit has high switching speed because charge storage effects are avoided by using the transistors in a non-saturated mode. This circuit is the basis of the above medium-scale integration package, where variable frequencies are obtained by charging the external capacitor at different rates via an internal voltage-controlled current source. The i.c. package contains two identical networks, but if only one is being used, it is essential that both ground connections (pins 8 & 9) are earthed to ensure earthing of the substrate and good isolation. The enable terminal (no. 11) must be grounded for continuous output at the output terminal. Output is disabled if this terminal is taken to logic high or open-circuited. Graphs opposite indicate linearity over a restricted range for each capacitor value, and waveform deteriorates at very low values of C_1, and thus at high frequencies.

Circuit modification
- Emitter-coupled astable output swings are usually restricted. An additional output stage supplied via V'_s permits the output swing to be approximately 0V up to V'_s and hence t.t.l. compatibility is easily achieved, i.e. V'_s and V_s need not be the same.
- Variable-capacitance diodes may provide a wider frequency range, depending on type (see over). Supply voltage 4.5 to 6.5V, frequency maintained constant.

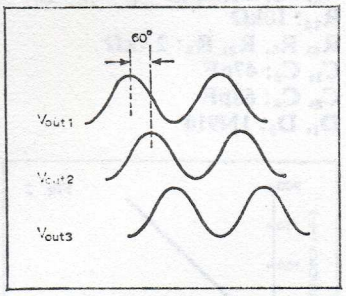


will reach saturation before the other output reaches its zero crossing point.

Circuit modifications

- Use a switched integrator rather than a switched gain amplifier. This makes IC_1, IC_3 redundant (Circard Set 3, No. 5). LM3900 quad package may be now arranged to provide the two outputs.
- Phase shift oscillator (above) provides three outputs with 60° phase relationship.

IC_1–IC_3: 1/6×CD4049,
R: 10kΩ, C: 2700pF,
frequency: 13kHz.
As the c.m.o.s. gates are being used in their linear region, both the n- and p-type transistors will be conducting and hence power consumption



will depend on the supply voltage. Typically the total current drain from the supply for the above network is

$V_{DD}-V_{SS}=3V$ $I_T=0$
$V_{DD}-V_{SS}=10V$ $I_T=12mA$
$V_{DD}-V_{SS}=15V$ $I_T=30mA$

Frequency may be controlled by substituting voltage-dependent resistors for each R_1 and maintaining as close a ratio as possible between the R values. Frequency is approximately $1/3RC$.
Note that with the CR values necessary for 60° phase shift at a specific frequency, the output of each buffer stage is attenuated by about one half and hence the minimum gain of each stage must be >2.

- An alternative arrangement is shown above right, using similar c.m.o.s. buffer inverters. In this case the resistor ratio is critical and theoretically for infinite gain amplifiers $R_2=R_1/2$ and a much better approximation to sinusoidal outputs is obtainable from each buffer, again phase shifted by 60°. Typical values R_1: 100Ω, R_2: 33 to 39kΩ, C: 2700pF, $V_{DD}-V_{SS}=6V$, frequency 1kHz.

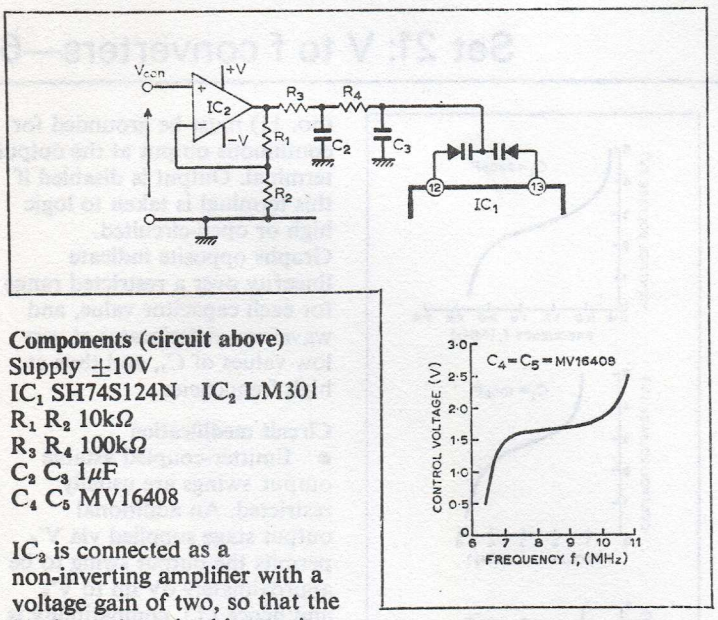
These buffers have gain-frequency responses which give higher gains for lower supply voltages. Typically 50dB at +3V up to 100Hz, and 30dB at +10V up to 100kHz. Hence since the gains are finite, then R_2 must be less than $R_1/2$. But at the lower values of the supply range 3 to 15V, some flexibility of this value between each R_2 is permitted. At higher levels the ratio is more critical, R_2 may be replaced by f.e.ts employed as v.c.r. to obtain a restricted frequency range.

Further reading

Voltage controlled two-phase sawtooth oscillator, *Wireless World*, June 1973, p. 285.
AN-88 CMOS Linear Applications, National Semiconductor, p. 170.
Frequency controllable 3-phase sinewave generator, *Electronic Engineering*, July, 1974.

Cross references

Set 11, card 6.
Set 8, card 1.



Components (circuit above)
Supply ±10V
IC_1 SH74S124N IC_2 LM301
R_1 R_2 10kΩ
R_3 R_4 100kΩ
C_2 C_3 1μF
C_4 C_5 MV16408

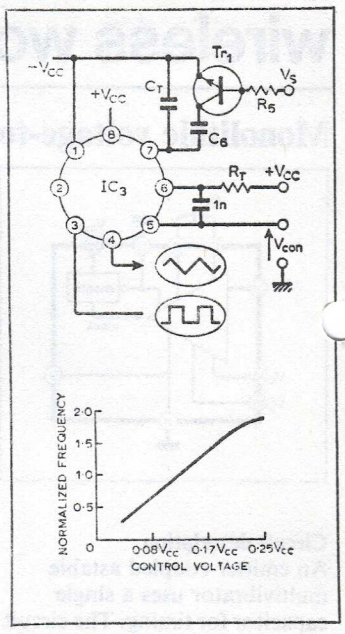
IC_2 is connected as a non-inverting amplifier with a voltage gain of two, so that the biasing voltage in this case is twice the control voltage. This gain can be altered for appropriate voltage range.
A claimed frequency range of 2 to 20MHz using varactors MV1403 and MC1456 for IC_2 is documented in the referenced literature.

Components (circuit right)
IC_3 LM566, SE/NE566
General-purpose voltage-controlled oscillator.
C_T 4.7nF C_6 0.047μF
R_S 4.7kΩ R_T 10kΩ
Maximum sweep rate 1MHz
R_T and C_T are the frequency range determining components. For a fixed value of C_T 10:1 variation in frequency is possible via a variable input at $V_{control}$ which should be within the range 3 to 5.5V for $V_{cc}=\pm 6V$.

The above values provide for a maximum free-running frequency of about 10kHz for Tr_1 off. For $V_S=-3V$, Tr_1 is saturated, hence increasing timing capacitor 10 times, free-running frequency is then approximately 1kHz.

Control voltage measured between pins 8 and 5 should be in the range 0 to $0.25V_{cc}$. (It is this voltage divided by R_T which defines capacitor charging current.) Frequency is

$$\frac{2(V_{cc}-V_{control})}{R_T C_T V_{cc}}.$$



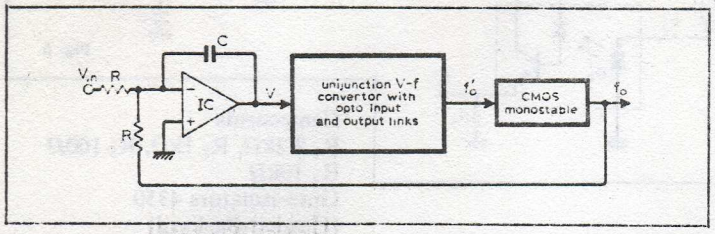
Further reading

Klein, E. Medium-scale integration for instrumentation and control, *Semiconductors* (Motorola) vol. 2 no. 1 1971, p. 20.
Signetics: SE/NE566 function generator.

Cross references

Set 17, card 3
Set 8, card 9

Linearized voltage-to-frequency converter



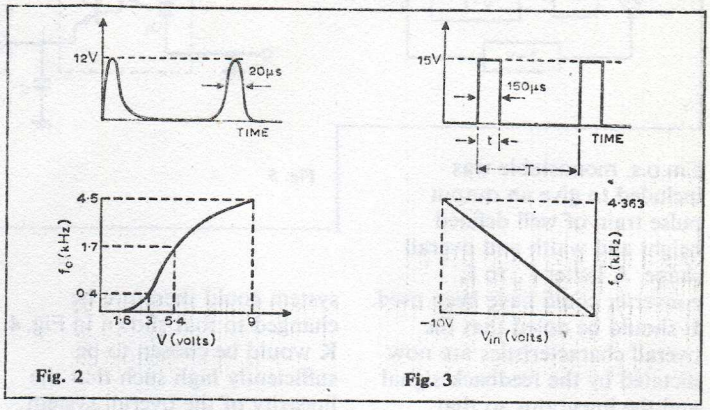
Components
R 100kΩ, C 0.22μF
IC 741
Unijunction V-f'o—see over, centre. Monostable—see over, right V_{in} 0→−10V

Performance
Graphs of f'o and fo are shown in Figs. 2 and 3. Graph V against fo, corresponding to open-loop v-f conversion, is shown in Fig. 2. with V_{in} against fo shown in Fig. 3. Linearity achieved was better than 0.5%—clearly much better than the open-loop performance.

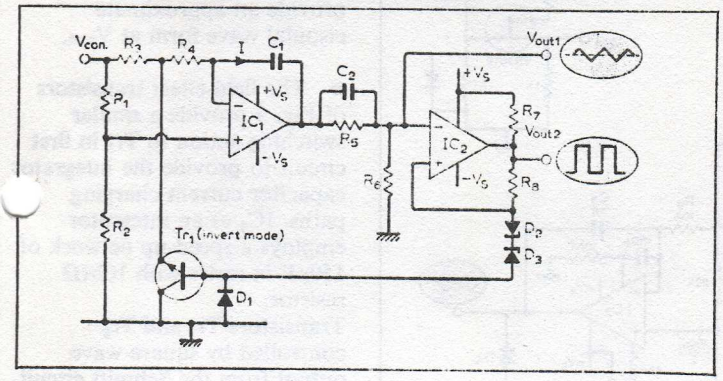
System description
If the loop gain of a closed-loop system is high then the effect of non-linearities in the forward path is much reduced. In this case we have a highly non-linear V to fo converter and an integrator/error detector is then included to provide the feedback. In d.c. terms, the integrator can be regarded as having infinite gain since for finite input voltage the output voltage after infinite time is infinite, ignoring the effect of saturation. Alternatively: $\Delta V =$

$$1/RC \int_0^T V_{in}dt + 1/RC \int_0^t 15dt$$

The steady-state condition of constant fo can only occur when V is constant and this occurs when V is zero i.e. when the integral of the input signal and the integral of the feedback signal exactly cancel. Hence exact correspondence between V_{in} and fo can be expected if the integrator and feedback signal are "perfect". Immediate improvement in the system would be effected if an i.c. with much lower input current requirements were used e.g. 308. Further improvement would be obtained by the use of a low-loss capacitor. The



Linear voltage-to-frequency converters



Circuit description
The circuit comprises an integrator whose output ramps toward positive and negative target values defined by diodes D_2 and D_3 i.e. the potential at the non-inverting input of comparator IC_2 is $V_{D_2}+V_{D_3}+V_{be}$ (or V_{D_1}) (approx ±9V). When the transistor is off (V_{o_2} negative), capacitor current is

$$I = \frac{V_{control}\left(1-\frac{R_2}{R_1+R_2}\right)}{R_3+R_4} \quad (1)$$

When Tr_1 conducts, I is

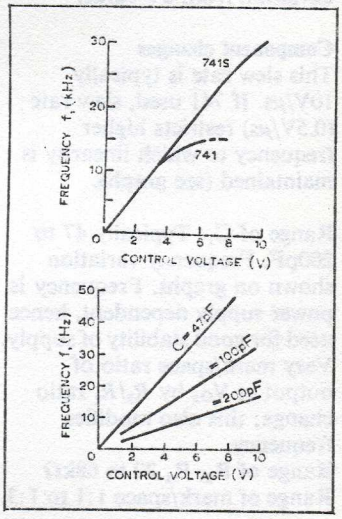
$$I = -V_{control}\left(\frac{R_2}{R_1+R_2}\right)/R_4 \quad (2)$$

For equal slopes at the triangular output, V_{o_1}, the current magnitudes are equal, provided

Typical performance data
Supply ±15V
IC_1 741S IC_2 LM311
Tr_1 ME4002
R_1 68kΩ, R_2 22kΩ, R_3 33kΩ
R_4 15kΩ R_5, R_7 3.3kΩ
R_6 12kΩ R_8 4.7kΩ all ±5%
C_1 100pF C_2 1nF
D_1 1N914
D_2, D_3 reference diodes 6.8V e.g. BZY88
$V_{control}$ range 0 to 10V
Triangular output ±8V peak
Frequency range 30Hz to 33kHz

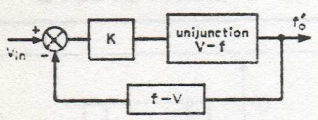
$$\frac{R_1}{R_2} = 1 + \frac{R_3}{R_4}$$

If V_{o_2} is positive, Tr_1 is on, and integrator output rises towards +9V at which level the comparator IC_2 switches over to make V_{o_2} negative, bringing Tr_2 out of conduction. C_1 changes according to the first equation, and integrator output ramps towards −9V, when comparator again changes state.



Components C_2, R_5, R_6 form a phase-advance network to compensate for the switching delays of IC_2 and Tr_1 at the higher frequencies. The invert mode of Tr_1 provides a very low collector-emitter drop (few millivolts), i.e. the effect on the second equation is neglected.

Fig. 4



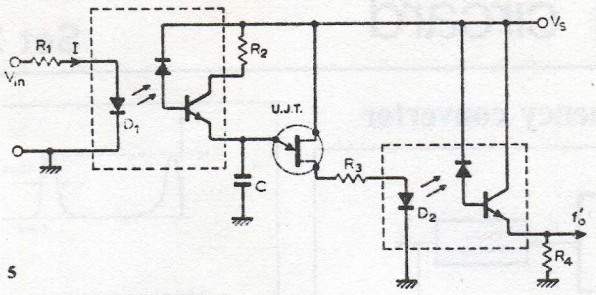


Fig. 5

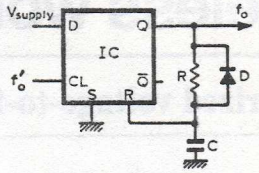


Fig. 6

c.m.o.s. monostable was included to give an output pulse train of well defined height and width and overall shape. A better f'_o to f_o converter could have been used. It should be noted that the overall characteristics are now dictated by the feedback signal and the integrator so that forward path changes, causing changes in f_o, will be completely cancelled, apart from transient effects. Changes in the shape of f_o, e.g. impulse height and width, will however have an effect on f_o, although not linearity.

System modification
Effectively, the combination of the monostable and integrator is an f'_o to v converter. The system could therefore be changed to that shown in Fig. 4. K would be chosen to be sufficiently high such that the linearity of the overall system is equivalent to that of the f to v converter. This is only satisfactory if the shape of the f'_o pulses is satisfactory.

Element description
The circuit of Fig. 5 shows the detail of the unijunction v to f converter (card 1) used. The opto-elements are included to show that their inherent isolating properties can be used not least to produce a very non-linear v to f'_o characteristic. This is because D_1 requires approximately 1.6V to conduct and is due to the fact that the charging current is not linearly related to I. Resistor R_2 is included to protect the transistor and R_4 is large to produce a sufficiently large pulse to trigger the monostable. Resistor R_1 may be reduced to allow much lower input voltages to be used. The limit is set by the opto-diode input current. Any opto-isolator may be used e.g. TIL112.

Components
R_1 2.2kΩ, R_2 1kΩ, R_3 100Ω
R_4 10kΩ
Opto-isolators 4350 (Hewlett-Packard)
U.j.t. 2N2646 V_s 15V
C 0.01μF

Circuit of Fig. 6 is the c.m.o.s. monostable used. It is identical in format to that described in set 18, card 8 but includes an extra diode to allow the capacitor to discharge closer to zero volts to improve linearity.

Components
R 100kΩ
C 2.2nF
D 1N914
IC CD4013E

Linearity is better than 0.5% over the range of control voltage, 0.1V to 8V, based on deviation from 6V value.

Component changes
This slew rate is typically 10V/μs. If 741 used, slew rate (0.5V/μs) restricts higher frequency to which linearity is maintained (see graph).

Range of C_1: Typically 47 to 200pF. Frequency variation shown on graphs. Frequency is power supply dependent, hence need for good stability of supply. Vary mark/space ratio of output at V_{o_2} by R_2/R_1 ratio change; this also modifies frequency.
Range of R_2, R_1 22 to 68kΩ
Range of mark/space 1:1 to 1:3.

Circuit modifications
● A variable output voltage is obtainable via the circuit shown in Fig. 1. Comparator hysteresis can be changed by varying the fraction fed back via a potentiometer RV_1. This will control the output

Fig. 1

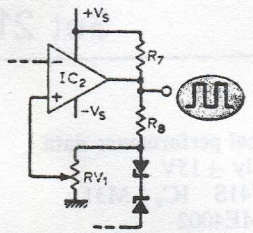
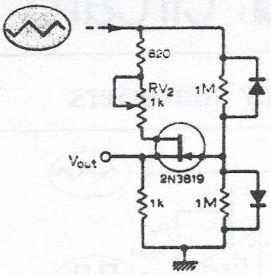
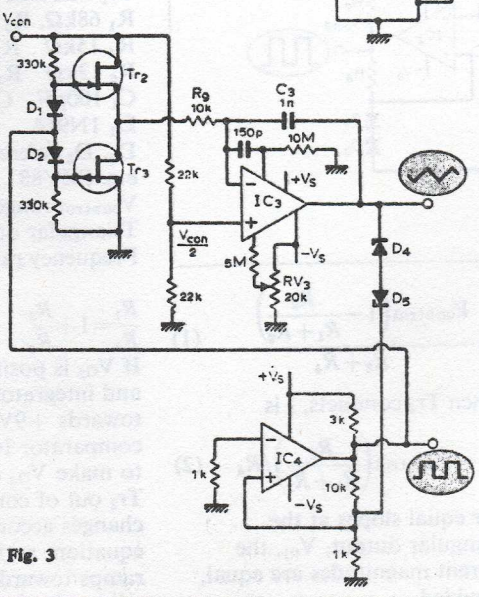


Fig. 2



Components
IC_3: LM301A
IC_4: LM311
Tr_2: 2N3972
Tr_3: 2N5019
D_1, D_2: 1N457
D_4, D_5: 1N751
V_s: ±15V

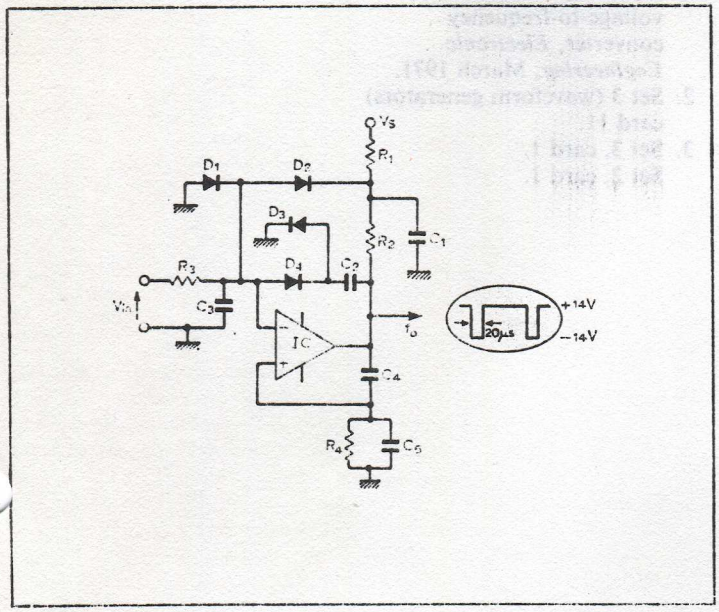
Fig. 3



amplitude. The triangular output is shaped by the circuit of Fig. 2. Potentiometer RV_2 is adjusted for a minimum even-harmonic content, to provide an approximate cisoidal wave form at V_{out}.

● The field-effect transistors of Fig. 3 provide a similar switching action to Tr_1 in first circuit to provide the integrator capacitor current charging paths. IC_3 as an integrator employs a speed-up network of 150pF in series with 10MΩ resistor.
Transistors Tr_2 and Tr_3 controlled by square-wave output from the Schmitt circuit of IC_4. When Tr_2 is on, Tr_3 is off and C_3 charges via Tr_2 and 10kΩ resistor. With Tr_2 off, and Tr_3 on, current reverses through the capacitor with magnitude defined by $V_{control}/2R_9$. RV_3 should be adjusted to provide a symmetrical square-wave output when $V_{control}$ is 5mV.
Input control voltage range: 5mV up to 5V.
Frequency range 10Hz to 10kHz.

Diode-pump voltage-to-frequency converter

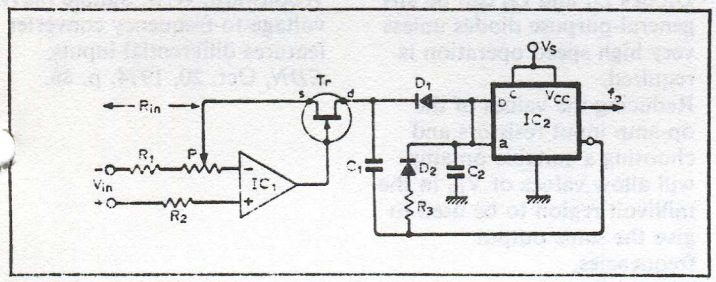


Components
Supplies: ±15V
IC: 748C
R_1: 12kΩ, R_2: 3.9kΩ
R_3: 10kΩ, R_4: 4.7kΩ
C_1: 4.7μF, C_2: 1nF
C_3: 33μF, C_4: 56pF
C_5: 500pF
D_1 to D_4: 1N914

Performance
V_{in}: 0 to +4.00V
Output pulse train: pulse width about 20μs swinging from +14V to −14V with a maximum frequency of around 14kHz, corresponding to a mark-space ratio approaching 3:1.
Linearity better than 0.3% over two decades.

Circuit description
Elements R_1, R_2, D_1, D_2 and C_1 are not basic to the action of this circuit and will be ignored initially. Suppose the i.c. output is sitting at +14V. Then C_2 will have been charged to this level via D_3. However as C_3 charges via R_3 under the influence of V_{in}, the negative terminal of the i.c. eventually reaches 0V and the amplifier output swings negative. The network comprising C_4, R_4 and C_5 provides sufficient positive feedback to make this swing very rapid—hence the use of a high speed op-amp. Capacitor C_2 then deposits its charge via D_4 into C_3 in a diode pump fashion thereby lowering the voltage across C_3. However the

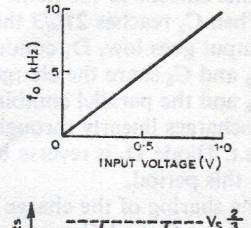
Differential input voltage-to-frequency converter



Components
Supplies: ±15V
IC_1: 741, IC_2: NE555
Tr: 2N5457
R_1: 270Ω
R_2: 1.2kΩ
R_3: 47Ω
C_1: 1nF
C_2: 22nF
D_1, D_2: 1N914

Circuit description
The above circuit is of a form published by Woodward but with what appear to us as corrections, although we have to admit to not achieving the performance claimed in his article, viz linearity better than 0.05% from 10Hz to 10kHz. The results we achieved are shown roughly in Fig. 2, measured linearity being 0.15% over the two decades, 100Hz to 10kHz.
Pin c of IC_2 is the R (reset) terminal and its action is not necessary in a brief explanation. Pins a and b are the trigger and threshold terminals of the i.c. When the C_2 capacitor voltage goes below the trigger potential, $V_s/3$, the output swings high, and when the voltage exceeds the threshold voltage, $2V_s/3$, the output swings low—see waveforms of Fig. 3.
The basic principle is that of charge dispensing in which a current proportional to a voltage is balanced by the periodic charging of a capacitor to a precise voltage. In this case, the current through the f.e.t. is fixed by the input voltage at V_{in}/R_{in}. This current flows for time T as a result of the charging of C_2 from $V_s/3$ to $2V_s/3$. Thus

Fig. 2



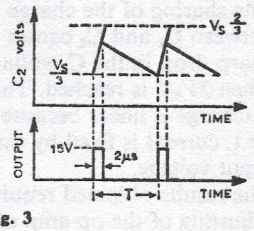


Fig. 3

$$\frac{V_{in}}{R_{in}} \cdot T = C_2 \frac{V_s}{3}$$

and $$f_o = \frac{3V_{in}}{R_{in} C_2 V_s}.$$

positive feedback network consists of elements with a short time constant and the voltage on the positive terminal quickly becomes less negative than the negative terminal voltage and so the amplifier voltage swings back to +14V. In the −14V period the circuit is acting rather like a monostable, the delay being fixed by the C_4, R_4, C_5 network and by the R_3, C_3 network. Because there is again positive feedback the rising edge will be equally sharp but the period will be difficult to define accurately, partly because of the complexity of the CR networks and partly because two voltages both going in the same direction (positive) are being compared.
This, however, is not serious since the pulse width does not affect the amount of charge on C_2, and it is this charge which is being balanced by the current in the input network.

The maximum frequency we obtained was close to the limit of the op-amp but the mark-space ratio could have been made even lower if required by reducing C_3, R_3 or lengthening the time constant of C_4, R_4, C_5. The network comprising R_1, R_2, C_1 and D_2 prevents the device from locking into a saturated condition by too large an input voltage (positive). Diode D_1 prevents the negative input terminal being overdriven by a negative input voltage.

Circuit modifications

- A high-speed comparator would be preferable to an op-amp which was used in our experiments.
- The pulse width does not theoretically affect the result but the pulse height does. A c.m.o.s. buffer amplifier could be included to give a well defined output pulse height—see reference 2.
- An alternative approach to the pulse height problem is to use internal clamping of the output level—see references 3.

References

1. Pease, R. Ultra-linear voltage-to-frequency converter, *Electronic Engineering*, March 1971.
2. Set 3 (waveform generators) card 11.
3. Set 3, card 1.
   Set 2, card 1.

This expression is valid so long as T is large compared with the pulse width.
When the output goes high C_2 charges via R_3 and D_2 from $V_s/3$ toward V_s. During this period D_1 is reverse biased and at the same time C_1 is providing some current to the f.e.t.
When C_2 reaches $2V_s/3$ the output goes low, D_1 conducts, C_1 and C_2 share the charge on C_2 and the parallel combination discharges linearly through the f.e.t. Diode D_2 is reverse biased in this period.
The sharing of the charge between C_1 and C_2 causes the sharp drop in the C_2 voltage when $2V_s/3$ is reached. The discharge is linear because the f.e.t. current is fixed by the input voltage.
The results obtained required adjusting of the op-amp offset voltage to zero. Common-mode rejection ratio is independent of input resistor match and is dictated by the op-amp used. However, common-mode voltage should not exceed ±2V.

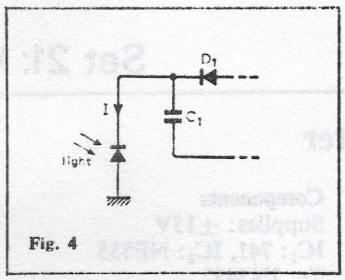


Fig. 4

Component changes
The charging time depends on C_2R_3 and should be short without R_3 being so low as to overload IC_2. This is not difficult to achieve since it is the open collector terminal which is used to charge C_2. Capacitor C_1 serves to cut off D_1 whilst C_2 is charging, so its value is not critical. Generally speaking though it should be less than C_2 to minimize the drop in C_2 voltage when D_1 starts conducting again, thereby keeping the slope of the downwards ramp as large as possible and clearly defining the time at which the voltage drops below $V_s/3$. Actually, C_1 and D_1 can be removed altogether without complete failure of the circuit, although linearity and output pulse shape are affected.
Diodes D_1 and D_2 can be any general-purpose diodes unless very high speed operation is required.
Reducing the values of the op-amp input resistors and choosing a suitable op-amp will allow values of V_{in} in the millivolt region to be used to give the same output frequencies.

Circuit modifications
Any circuit which will successfully draw constant current from the junction of C_1 and D_1 will produce the same result and such a circuit is shown in Fig. 4. The photodiode current is proportional to light intensity so an intensity-to-frequency converter would be produced by this arrangement. The differential input aspect is lost, however, unless one puts a second photodiode, connected the opposite way round, across the one shown.

Reference

Woodward, W. S. Simple 10kHz voltage-to-frequency converter features differential inputs, *EDN*, Oct. 20, 1974, p. 86.