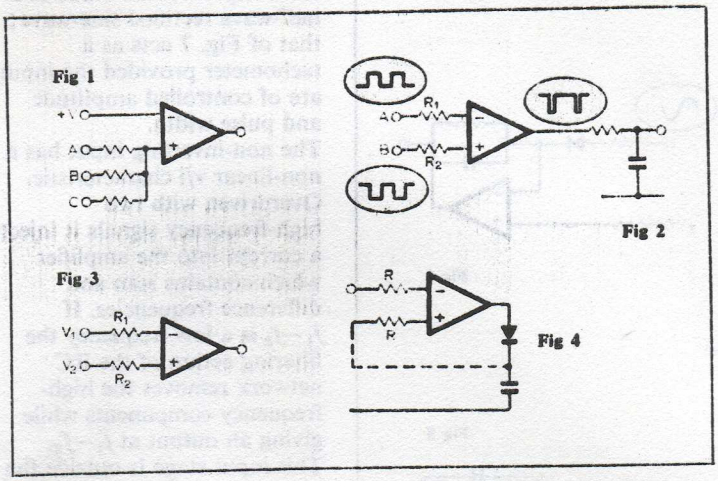
Measurement and detection

Circuit description

These circuits operate largely in a switched or non-linear mode; one card deals with negative resistance circuits which can be considered as having controlled non-linearity.

The amplifier gain is large enough that simple logic functions are readily performed as described in set 16 (Fig. 1). By scaling the resistors the output of Fig. 2 becomes $\overline{A}+B$ and the smoothed output has a d.c. value dependent on the phase difference of the inputs if these are square waves. The phase detector combined with a v.c.o. (set 17) gives a p.p.l., see card 3. Scaled resistors can also be used to provide simple forms of threshold logic including the weighted comparator of Fig. 3, while the comparator, using equal-valued resistors if desired, forms part



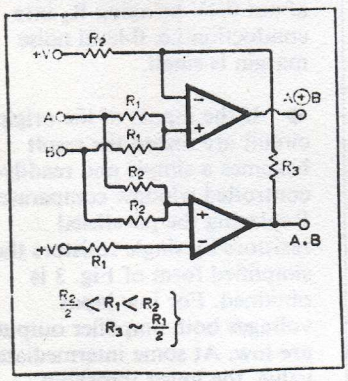
of the peak detector of Fig. 4. The capacitor charges through the diode until it matches the peak value of the input.

Another application for the comparator is in coupling signals into and out of transducers. Positive feedback may be added to the system to provide hysteresis, or negative feedback to control the level of current/voltage in a load as when testing or measuring the properties of a device e.g. semiconductor breakdown voltages.

Circuit description

The integrator plays a large part in measurement circuits as in waveform generators. Sample-and-hold circuits are closely related to peak-detectors, in that a voltage is stored on a capacitor that is proportional to the input voltage at some defined instant (the sampling instant and the input peak voltage respectively). The ramp and hold circuit of Fig. 5 is an intermediate step between the two circuits. If a resistive path is placed in parallel with the capacitor then the mean voltage developed at the output is defined by the mean output. Access to both inverting and non-inverting inputs makes it possible to measure the mean value of the sum or difference

Logic circuits



Typical performance

IC: ½LM3900
+V: +20V
R_1: 82kΩ
R_2: 120kΩ
R_3: 33kΩ
Output logic 0: ≈150mV
Output logic 1: ≈19.2V
(with load current 5mA output logic 1 still within 1V of positive supply)

Circuit description

Just as t.t.l., c.m.o.s. gates may be interconnected to produce more complex functions, so the simple gate functions described on card 1 may be used in identical configurations. The standard methods for producing such functions as the exclusive-OR gate which has the output high for one and only one high input require four two-input NAND gates. This may be acceptable where it is desired to implement a system with a single device type even though multiple exclusive-OR circuits are available within a single package.

The flexibility of the current-differencing configuration allows such circuits to be designed economically while retaining the advantages of wide supply voltage range and good noise immunity—provided again that the circuit is restricted to industrial applications not requiring fast response. The lower amplifier is a standard AND gate as discussed in set 16, card 4, while the upper amplifier is an OR gate. By feeding back the AND gate output to the inverting input of the OR gate the logic 1 resulting from A=1 B=1 is inhibited by the logic 1 simultaneously appearing at the AND gate output. The resulting truth-table shows the output to be an exclusive-OR gate, but the simultaneous availability of the AND function creates a half-adder.

It is obvious that such a circuit is no competitor to c.m.o.s. or t.t.l. for complex logic functions in view of the speed limitation. Where a small number of logic functions are to be introduced into an industrial system the availability of a circuit that will operate off virtually any available supply is a clear advantage. Being able to mix functions within a given package allows analogue and digital processes to be tackled efficiently.

Component changes

+V: +4 to +36V. In practice several samples of the device operated satisfactorily for supply voltages down to 2.7V at room temperatures.

R_1, R_2: Values may range from <10k to >1MΩ. There is no obvious advantage to lowering the resistances, but at high values capacitive strays may produce input current spikes significantly larger than the quiescent currents. For the AND gate, the current in R_1 must be less than current in R_2 while with both inputs high the

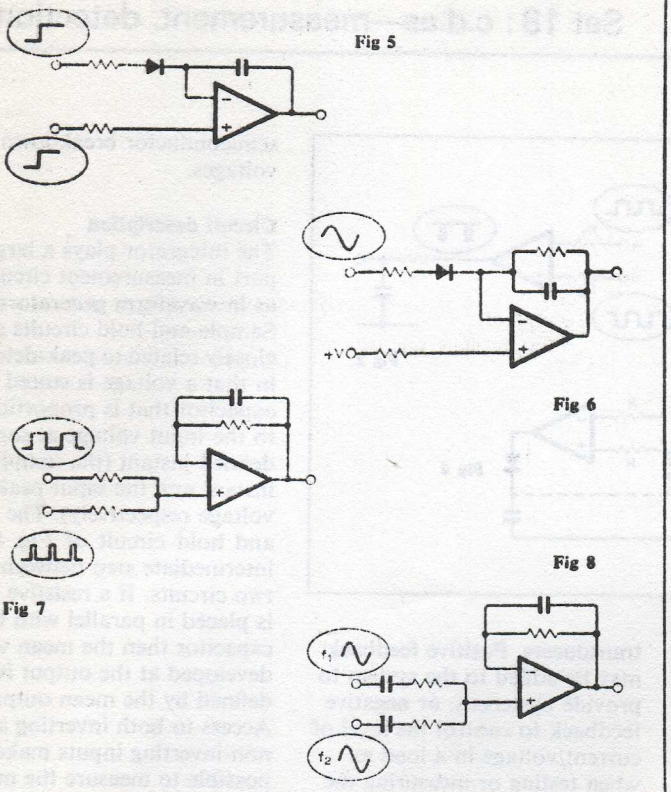


Fig 5

Fig 6

Fig 7

Fig 8

of two inputs, with the capacitor minimizing the output ripple. The circuit of Fig. 6 formed part of a controlled-amplitude RC oscillator (set 17) detecting the mean value of a half-wave rectified sine-wave; that of Fig. 7 acts as a tachometer provided the inputs are of controlled amplitude and pulse width.

The non-inverting input has a non-linear v/i characteristic. Overdriven with two high-frequency signals it injects a current into the amplifier which contains sum and difference frequencies. If $f_1 - f_2$ is a low frequency the filtering action of the RC network removes the high-frequency components while giving an output at $f_1 - f_2$. This input stage is outside the feedback loop and is not frequency limited by the amplifier compensation. Low-level high-frequency amplification is possible using this input.

Further reading

Frederiksen, T. M., Howard, W. M. Sleeth, R. S., The LM3900—A New Current-Differencing Quad of ±Input Amplifiers, National Semiconductor application note AN72.

Frederiksen, T. M., Norton quad amplifier subtracts from costs, adds to design options, *Electronics*, Dec. 6, 1973, pp.116-20.

Motorola Linear Integrated Circuit Data Book, pp.7-446, 7-453, 7-456 and 7-463; data sheets on MC3301P and MC3401P amplifiers.

National Semiconductor, Linear Integrated Circuits, pp.226-33, data sheets on LM3900.

Frederiksen, T. M., Howard, W. M., Sleeth, R. S., Use Current-mode IC amplifiers, *Electronic Design*, vol. 21, no. 2, Jan. 18, 1973, pp.48-55.

Mortensen, H., Use a quad amplifier to handle transducer bridge signals, *Electronic Design*, vol. 21, no. 3, Feb. 1, 1973, pp.74-6.

current through the pair of R_1 must exceed that in R_2. For a logic 1 signal nearly equal to +V this gives $R_2/2 < R_1 < R_2$.

R_3: This has to provide enough current to override the OR gate action for A=1 B=1. Value is not critical and values from $R_1/2$ down to $R_2/2$ are satisfactory. Where the input is noisy, the input resistors may be centre tapped and the tapping point decoupled to ground. The high value of resistors used together with the wide noise margins possible at high supply voltages allows the circuit to accommodate high noise environments provided the supply is adequately decoupled.

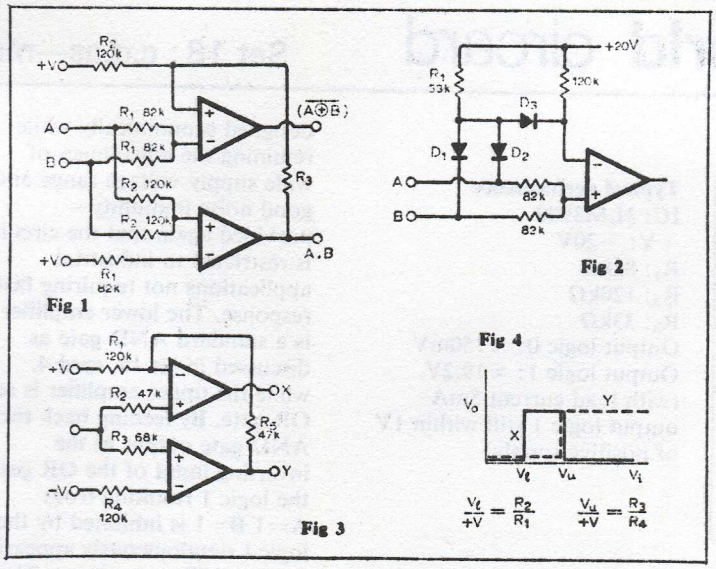


Fig 1

Fig 2

Fig 3

Fig 4

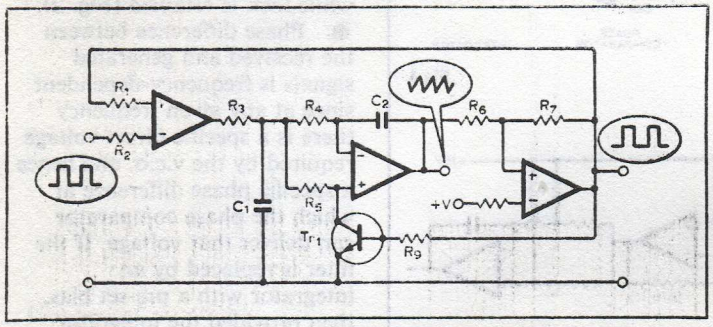
Circuit modifications

● Interchanging inverting and non-inverting inputs on the OR gate converts it into a NOR gate (Fig. 1). Then the output in the absence of feedback through R_3 would be logic 1 only when both inputs are at logic 0. The feedback forces the output of the NOR gate to go to logic 1 when both inputs are at logic 1, overriding the normal NOR gate function. The net result is that the output of the NOR gate becomes logic 1 for A=B and the circuit is an equality comparator. The output can also be seen as the negation of the exclusive-OR function.

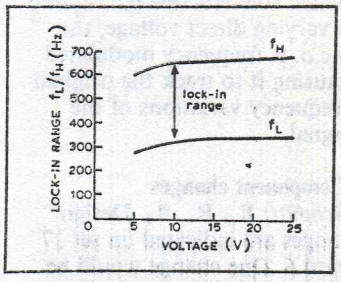
● It is not necessary to use two amplifiers to perform the exclusive-OR function. Instead, a passive AND gate using D_1, D_2 and R_1 keeps D_3 out of conduction except when A=B=1 (Fig. 2). Under these circumstances the current in R_1 is diverted through D_3 into the amplifier inverting input and overrides the OR gate action to provide a logic 0 at the amplifier output. A limitation in this circuit is the low threshold to the AND gate, with input levels rising above about 0.4V bringing R_3 into conduction i.e. 0-level noise margin is small.

● If the inputs of the original circuit are linked the result becomes a simple and readily-controlled window comparator. Replacing the paralleled resistors by single resistors the simplified form of Fig. 3 is obtained. For low input voltages both amplifier outputs are low. At some intermediate value, the lower threshold voltage V_L, output X goes high assuming $R_2/R_1 < R_3/R_4$ (Fig. 4). Output Y remains low. At the upper threshold output Y goes high driving X low. At some still higher input voltage a suitable choice of R_2, R_5 also allows X to go high again if required as the current in R_2 continues to increase while that in R_5 is restricted to $< V/R_5$.

Phase-locked loop

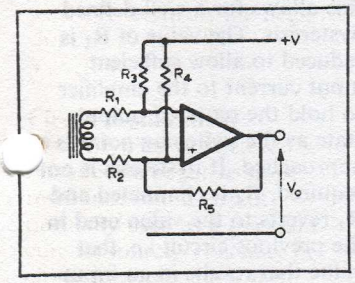


Typical performance
+V: +10V
R_1, R_3, R_6: 33kΩ
R_2: 68kΩ
R_4, R_8: 1MΩ
R_5: 470kΩ
R_7, R_8: 1.2MΩ
C_1: 0.1μF
C_2: 1nF
Tr_1: BC125
Capture range: 390 to 580Hz
Lock-in range: 320 to 660Hz
$V_{d.c.}$ over lock in range: 4.3 to 8.4V



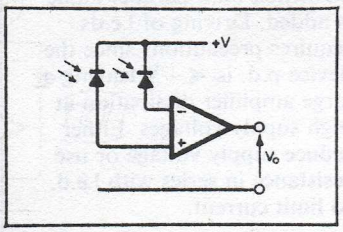
Circuit description
There are three identifiable subsections to this phase-locked loop. The first is a phase-detector which receives one input from the signal source and one from the square-wave output of the voltage-controlled oscillator. The output of the phase detector, when the oscillator is locked to the signal source, is a negative-going pulse train of the same frequency but of mark-space ratio dependent on the phase difference between the two waveforms (see circuit modifications). Smoothed by a simple RC filter, a direct voltage results that controls the rate of charging of a capacitor in the second subsection, the integrator. When the output voltage from the integrator reaches a critical level it causes a change in level from the output of the third sub-section, a Schmitt-trigger circuit. This switches the transistor reversing the net current into the integrator and with it the direction of charging until the second trigger level is reached. This completes the cycle of the v.c.o., and if its frequency is close to that of the incoming signal, locking is achieved.
If the incoming signal changes its frequency slowly, the resulting phase difference produces a corresponding change in the direct voltage that controls the v.c.o. i.e. the frequency changes, remaining in lock, but with a new value of phase difference. If the frequency difference between the input and the v.c.o. becomes too great or if either varies too rapidly, locking can be lost. The lock-in range with this circuit is over a frequency range of about 2 : 1 while the capture range is somewhat smaller. In summary, frequency modulation of the signal

Transducer driving



Typical performance
+V: +10V
R_1, R_2: 220kΩ
R_3, R_5: 5.6MΩ
R_4: 10MΩ
Hysteresis: 400mV

Circuit description
Where the input signal is from a transducer which has a floating and preferably low resistance output, the circuit shown gives a convenient means of setting the trip points symmetrically about the zero-voltage state of the transducer. With the output at zero and $R_1 = R_2$, $R_3 = R_5 = R_4/2$ then with the transducer output at zero, the net current into the amplifier is $V(1/R_4 - 1/R_3)$. With the output at +V the net input current is $V(1/R_4 + 1R/_5 - 1/R_3)$. With the above conditions these currents reduce to $\pm(V/R_4)$ respectively. The input sensitivity/impedance depend on R_1, R_2 increasing the former reducing the latter. Sensing of signals ≪100mV is not recommended but the circuit has reasonable rejection of high frequency noise/strays because of the relatively large input resistances used together with the effective input capacitance (said to be around 2nF by the manufacturer).



Typical performance
Inputs can be any pair of matched linear or non-linear transducers, which deliver a variable current for a fixed p.d. as the physical parameter under test varies e.g. reverse-biased silicon photodiodes giving current and light intensity.

Circuit description
Current-differencing characteristics of the amplifier make it particularly suitable as a comparator of input currents from whatever source they may come. Accuracy of matching of the input stages is not such as to allow very high precision but in routine applications it can be used for rapid detection of out-of-tolerance resistors excessive leakage currents in diodes etc. One of the inputs is fed from a standard element or with a current defined by an external resistor while the device under test is connected between the other input and the positive supply line.
Transducers such as photodiodes and transistors, photoconductive cells operated at low light intensities, and thermistors, can be used in matched pairs to sense the difference between physical parameters at two different locations while offering compensation against changes in any common variable (temperature effects on photoconductors etc.).

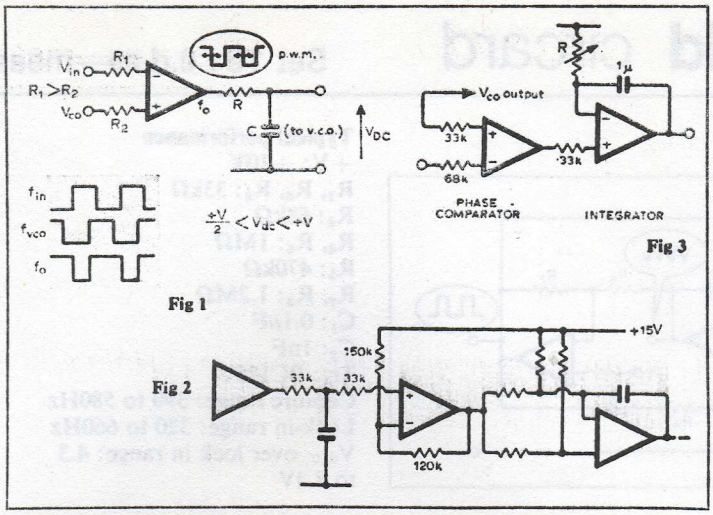
source, if slow enough, produces pulse-duration modulation at the phase detector output. After filtering, which converts this p.d.m. into a varying direct voltage, the v.c.o. is frequency modulated causing it to track the original frequency variations of the signal.

Component changes

Schmitt: R_6, R_7, R_8. Design ranges are indicated on set 17 card 6. One change would be to design for smaller hysteresis. Increasing R_7 reduces the positive feedback to achieve this.

Integrator: To operate at low frequencies R_4, R_5 may be increased. This disturbs the frequency stability of the v.c.o. if used in a free-running mode, but closure of the feedback loop via the phase detector accommodates this at the expense of drift in the phase difference.

Filter: If the signal is expected to change frequency only slowly if at all, the filter time-constant can be increased with advantage.

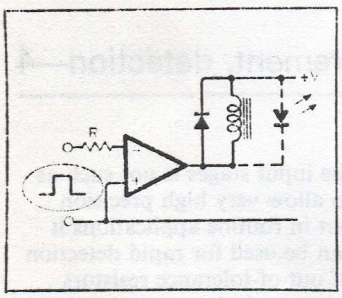


Circuit modifications

● The phase-detector action is as follows: when both inputs are low the output is high. For equal amplitude inputs, and $R_1 > R_2$, then when both inputs are high the output is high since the current to the non-inverting input is greater than that to the inverting input. When only one is high the output is controlled by that input.

● Because the phase-comparator has an output with a minimum mark-space ratio of 1 : 1, the mean output voltage swings over the range $+V/2$ to $+V$ allowing a maximum frequency range for locking of about 2 : 1 assuming a linear v.c.o. By introducing an amplifier this range can be increased to any desired extent since the amplifier may be biased to give an output →0 i.e. the v.c.o. frequency may be driven to a very low value while lock is retained (Fig. 2).

● Phase difference between the received and generated signals is frequency-dependent since at any given frequency there is a specific direct voltage required by the v.c.o. and hence a specific phase difference at which the phase comparator can deliver that voltage. If the filter is replaced by an integrator with a pre-set bias, then provided the integrator has a high gain (approaches the ideal integrator), its mean output takes up a value appropriate to the incoming frequency, while the phase difference can be controlled by varying R (35k to 70kΩ to provide phase differences from 0 to π with values shown in Fig. 3). This is because the net current into the integrator →0 when the output is to remain constant.

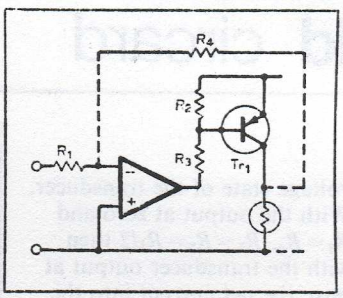


Typical performance

+V: 12V
R_L: 600Ω
R: 100kΩ
v_i: > +10V

Circuit description

The normal sink current is provided by a constant current stage of about 1.3mA. An additional internal transistor when over-driven can provide an output sink current of up to 30mA with a reasonable saturation voltage (>0.5V). This output current depends on the combined current gains of two internal transistors, allowing input currents as low as 100µA to provide sufficient drive. Output current is sufficient to drive small filament lamps and relays. As usual to protect the amplifier against reverse voltage spikes on switch-off a parallel diode is added. Driving of l.e.ds requires precautions since the device p.d. is ≪ +V leaving a large amplifier dissipation at high supply voltages. Either reduce supply voltage or use resistance in series with l.e.d. to limit current.



Typical performance

+V: 10V
R_1: 10kΩ
R_2, R_3: 470Ω
R_4: 100kΩ
Tr_1: BFR81
R_L: 40Ω

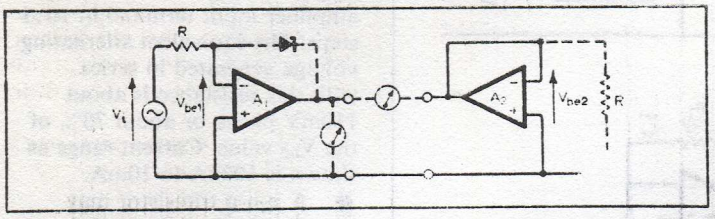
Circuit description

A single transistor with a current gain in saturation of >10 increases the load drive capability to >250mA. Resistor R_3 is included to minimize the p.d. across the amplifier output transistor when switched to the low state. Feedback via R_4 to the inverting input provides positive feedback for sharply defined switching (because of additional inversion by the transistor). Output swing can be to within a few hundred millivolts of the supply with a suitable power transistor and this allows for a well-defined hysteresis. The value of R_1 is reduced to allow sufficient input current to the amplifier to hold the required output state as the switching point is approached. If hysteresis is not required, R_4 is eliminated and R_1 reverts to the value used in the previous circuit i.e. that value that results in an input current of about 0.1mA at the given size of input pulse.

Cross references

Set 9, cards 1, 11.
Set 13, cards 2, 4, 8.
Set 16, cards 2, 3, 5, 6.
Set 17, card 6.

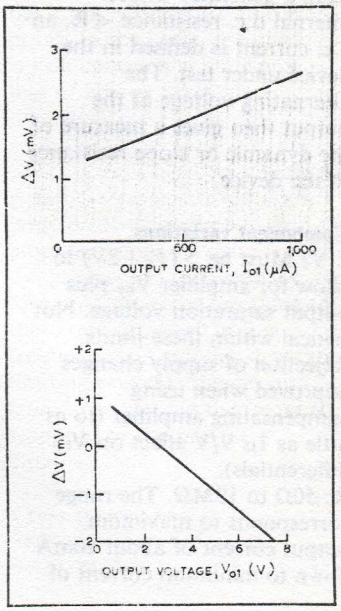
Semiconductor device testing



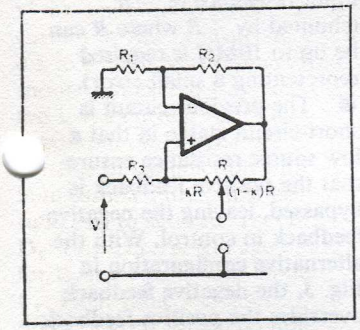
Circuit description
One application to which the matching characteristics of the amplifiers can be applied is the testing of semiconductor devices. To find the d.c. characteristics of a zener diode for example, the current should be defined (or measured) and the terminal p.d. measured over a wide range of currents. If the currents are low then this makes the measurement of voltage more difficult. In the circuit shown the direct current in the diode is given by V_{be}/R where V_{be} is that of the amplifier input transistor. At very low currents the diode carries the 30-nA amplifier input current as well. If the amplifier output voltage to ground is measured it gives the zener voltage after subtraction of the V_{be} term. Output impedance is low even at low zener currents, simplifying the voltage measurement. For these amplifiers the V_{be} term is little dependent on the feedback current (though somewhat more so on the output voltage). As the zener voltage is substantially constant, the V_{be} voltage can be conveniently measured when operating at a relatively high current yet will be valid for the lower currents. It is not necessary to make these two separate measurements since there are other amplifiers in the package with almost identical V_{be} values. One of these amplifiers is biased as shown and the voltage measurement taken between the two outputs. These are both low impedance points allowing a wide choice of voltmeters without significant loading.

Typical performance

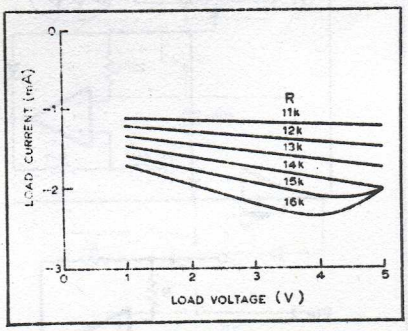
IC: ¼LM3900
+V: +15V
R: 5.6kΩ
Zener current: ≈100μA
Amplifier input V_{be} unbalance, $\Delta V \approx 2$mV for V_z of 6V
N.B. ΔV varies with both V_o and I_o but V_o in turn is approximately constant for a given zener.
Zener d.c. ≈ V_{be1}/R
Zener a.c. ≈ v_i/R



Negative resistance



Typical performance
IC: ¼LM3900
k: 0.5
R_1, R_3, R: 10kΩ
R_2: 15kΩ
Dynamic output resistance: −9.3kΩ
V_s: +15V
V: 5.3V (set for output current of 1mA with R_2 trimmed for output resistance →∞)



Circuit description
A potent tool in the design of oscillators and certain classes of active filters is the negative-resistance circuit, which may also be a particular case of a negative-impedance converter. A previously described constant-current circuit may be adapted to give a controlled negative output resistance, by allowing the overall positive feedback to exceed the negative feedback. The circuit remains stable only when the external load re-establishes the supremacy of the negative feedback. In the circuit shown, a short-circuit load eliminates the positive feedback altogether indicating that the circuit is short-circuit stable. For $R_2/R_1 > R/R_3$, the open-circuit load condition has excess positive feedback and switching of the output would occur. For intermediate values of R_L, the load current as defined by the voltage V and potentiometer setting k is observed to fall as the load-resistance is reduced. For the values shown, $R_2 = 10k\Omega$ gives the limiting case of output resistance →∞, and increasing values of R_2 produce a negative resistance of falling magnitude. Maximum current in the load is restricted to about 2mA with $k=0.5$ but the amplifier itself restricts the current to around 10mA regardless of the resistance values chosen. In principle, emitter followers can be added at the amplifier output with all the resistor values lowered to increase the drive capability, but for most applications it is the small-signal performance that is of interest.

Component changes
R_1, R_3, R: It is often convenient to have these equal. Minimum value is dictated by loading effects on output and would not generally be much below 10kΩ. Negative slope resistance available is comparable to these values.
R_2: Controls the slope of the resistance, together with the tap on R. Range 10 to 20kΩ.
k: 0.2 to 0.8. For application

Matching between the amplifier V_{be} values is not perfect and some improvement follows from the amplifiers at equal currents i.e. by placing equal resistance values to ground. By superposing an alternating voltage of peak-peak value $< V_{be}$ at the input, as from a generator whose internal d.c. resistance $\ll R$, an a.c. current is defined in the device under test. The alternating voltage at the output then gives a measure of the dynamic or slope resistance of the device.

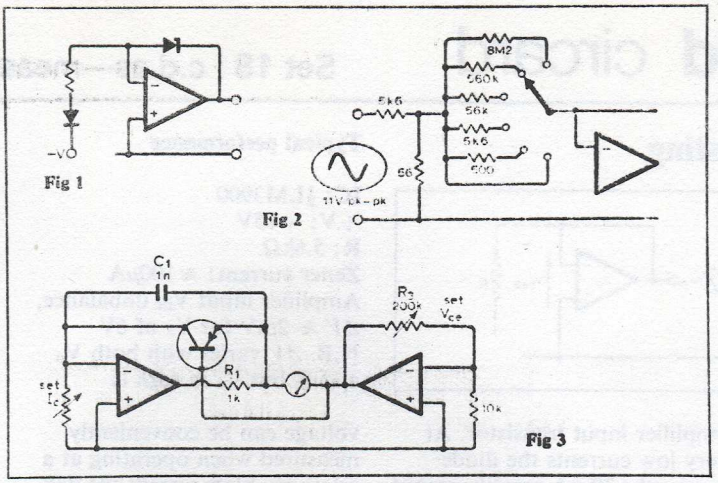


Fig 1

Fig 2

Fig 3

Component variations

$+V$: Must be $>(V_z+2V)$ to allow for amplifier V_{be} plus output saturation voltage. Not critical within these limits. Rejection of supply changes improved when using compensating amplifier (to as little as 1μ V/V effect on V_{be} differentials).

R: 50Ω to 10MΩ. The range corresponds to maximum output current of about 10mA down to minimum current of 50nA. At this lower level accuracy is poor because of amplifier input current of 30nA. If v_i, the input alternating voltage, is kept constant as R is varied, then since V_{be_1} is substantially constant, the alternating current superposed on the d.c. remains a constant fraction. With zener diodes operated in their normal region the zener voltage varies little, any variation in slope resistance shows clearly in the variation of the output a.c. component.

V_i: Peak-peak voltage $< V_{be_1}$. Typical values of 0.1 to $0.3V_{be_1}$.

Circuit modifications

● To define the current accurately it is not enough to rely on the constancy of the input V_{be} particularly if the temperature is subject to variation. A simple alternative is to take the resistor to the negative supply rail (if available) through a diode to give compensation against the remaining small effect of V_{be} variations (Fig. 1).

● Fig. 2 circuit varies the d.c. resistance to ground from the amplifier input terminal in 10:1 steps. The equivalent alternating voltage generated in series with this resistance is about 110mV pk-pk or about 70% of the V_{be} value. Current range as shown is 100nA to 10mA.

● A p-n-p transistor may have its V_{be}/I_c characteristic plotted using a similar arrangement. Collector current is defined with the emitter taken to the output of one amplifier, the base to the other. R_1, C_1 control the h.f. characteristics to maintain stability. By varying R_3, the V_{ce} value for the transistor can be controlled to show the small effect of V_{ce} on the I_c/V_{be} characteristics; n-p-n transistors cannot be dealt with so simply using this form of circuit.

suggested later, where only small negative resistance effect required $k=0.5$ is satisfactory.

$V+$: $+4$ to $+36V$. Normal operating range for amplifier.

V: Used to set the output current to some range over which R_2 controls the negative slope $+1V$ to $+8V$ for $V_+=15V$.

Circuit modifications

● A typical application is to introduce a negative slope resistance into a circuit normally used as a constant-current source. This may be either to overcome some positive resistance due to leakage paths etc, or simply to modify the waveform produced in a generator. Here the circuit provides the charging current to a capacitor that is part of an astable circuit having some similarity to a unijunction oscillator (Fig. 1). Capacitor imperfections plus external resistors would result in a ramp whose dV/dt fell at higher amplitudes. By increasing the negative slope, more current is fed into the capacitor as the p.d. across it increases. This can linearize the slope or with over-compensation cause the slope of the waveform to increase at higher voltages.

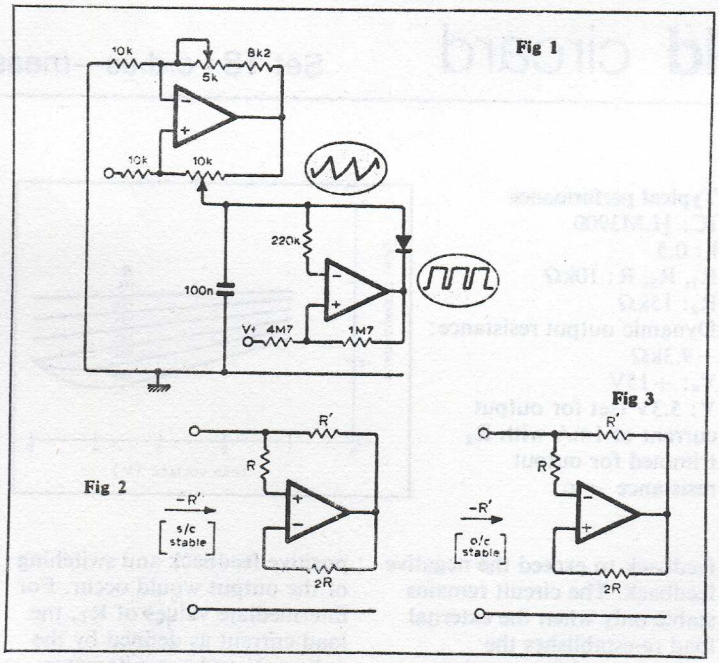


Fig 1

Fig 2

Fig 3

● For other applications a direct equivalent of the negative-impedance converter is required. In Fig. 2 the voltage gain of the amplifier is $+2$. Hence the voltage appearing across the resistor R′ is equal to the input voltage in magnitude but in a sense that returns a proportional current to the source. This leads to an input resistance of $-R'$ (shunted by $+R$ where R can be up to 10MΩ is required representing a small error).

● The previous circuit is short-circuit stable in that a low source resistance ensure that the positive feedback is bypassed, leaving the negative feedback in control. With the alternative configuration in Fig. 3, the negative feedback overrides the positive feedback provided the source impedance is greater than R′. Additional bias resistors from the amplifier inputs to the positive supply line may be used to set desired output quiescent levels.

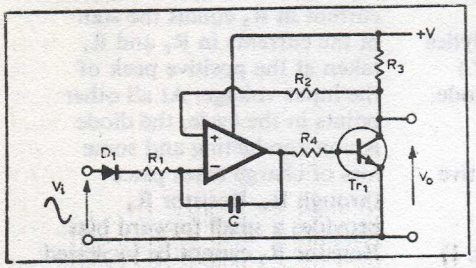
Cross references

Set 3, card 8.

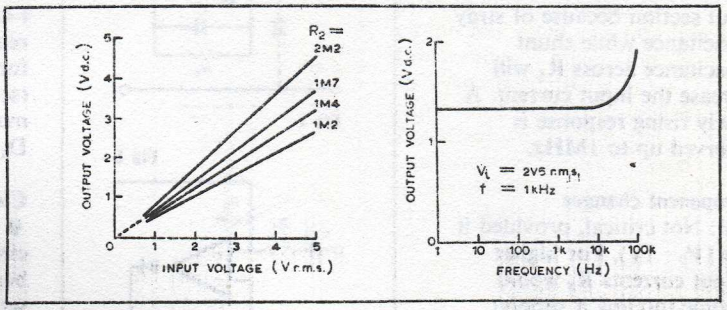
Set 6, card 6 (AC constant-current circuits, see note on front).

Set 17, card 5.

Peak/mean rectifiers

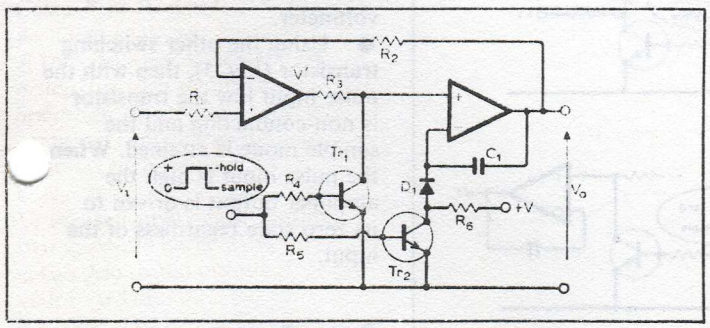


Typical performance
+V: +15V
Tr_1: BC125
R_1: 1MΩ
R_2: 1.2MΩ
R_3: 10kΩ
R_4: 6.8kΩ
C: 10μF
D_1: 1N914
v_i: 2.5V r.m.s., 1kHz
v_o: 1.35V d.c.



Circuit description
The mean value of an alternating voltage can be obtained by rectifying the signal (half or full-wave) and applying the resulting output to a mean-sensing instrument such as a moving-coil meter. Alternatively the rectified waveform may be filtered and applied to a d.c. voltmeter (including a d.v.m.). In each case one or more diodes or transistors are required to perform the rectifying function, and they introduce two related errors into the response of the circuit. Non-linearity in the diode causes a corresponding non-linearity in the transfer function. In particular, at very low levels the signal is insufficient to bring the diode into conduction. This gives an offset to the transfer function. If other diode effects can be added, then the offset together with its temperature drift can be largely cancelled. Rectification of signals below about 0.5V r.m.s. is still impossible but above this level the error can be small.
In the circuit shown the amplifier integrates the difference between the currents caused by the rectified input signal and the mean voltage at the transistor collector. For a particular value of R_2/R_1 the diode and V_{be} drops provide partial cancellation, and the transistor collector potential becomes a linear function of the mean half-wave rectified input. (Although the slope if extended would pass through the origin, rectification of low-level signals cannot be achieved with this circuit.) The value of R_2 obtained empirically for this circuit differs somewhat from that previously proposed for the related section of the Wien bridge oscillator. The values of R_4, R_3 can be adjusted over a wide range to accommodate differing load resistors/meters etc while the capacitor can be increased to

Sample and hold circuits



Typical performance
+V: +15V
R_1, R_2: 1MΩ
R_3: 22kΩ
R_4, R_5: 47kΩ
R_6: 33kΩ
C_1: 0.1μF
D_1: 1N4148
Tr_1, Tr_2: BC125
Input range: +1 to +14V
Output drift: +0.2V/s in hold mode

Circuit description
If an ideal integrator is incorporated into an overall d.c. feedback loop, then the capacitor charges until it provides an output voltage equal to (or some set multiple of) the input voltage. It introduces a time delay into the loop by virtue of the maximum charging current that can be provided by the amplifiers and so the speed of response of the amplifier is limited. If the loop is interrupted at any instant such that the integrator input current is reduced to zero, the p.d. across the capacitor remains substantially constant at the value corresponding to the input just prior to that interruption i.e. the signal can be continuously or periodically sampled with the facility to hold the value of the input at any required instant. Amplifier input currents, capacitor leakage etc cause drift in this held value but with care drifts of <5% are possible for periods of 5 to 30 minutes with simple circuitry. With the control input low (sample mode) the integrator receives current to its inputs via R_3 and R_6/D_1. It integrates the difference between those currents until the currents in R_1, R_2 are substantially equal, bringing v′ into its linear region. Any increase in v_i raises v′ and hence the current into the integrator non-inverting input until v_o tracks the charge in v_i. Allowing for an ideal current mirror at the amplifier input $v_o/v_i = R_2/R_1$ though V_{be} effects only cancel well for $R_2 \approx R_1$. In the hold mode currents in R_3, R_6 are grounded and the only currents affecting v_o are the amplifier input current plus capacitor leakage.

Component changes
R_1: Sets input resistance. If too high then amplifier input current becomes significant. 100kΩ to 10MΩ.
R_2: $R_2 = R_1$ gives best compensation against V_{be}

give adequate smoothing for frequencies < 1Hz. At high frequencies partial peak rectification may occur in the input section because of stray capacitance while shunt capacitance across R_1 will increase the input current. A slowly rising response is observed up to 1MHz.

Component changes

$+V$: Not critical, provided it is $>(V_o+1V)$. For higher output currents R_3 would become too low if supply/output differential is too small.
Tr_1: Any silicon n-p-n small-signal transistor. No significant h.f. response required because of integrating action of C on rectified waveform.
R_1 sets input impedance and should be high to minimize loading on source (important because of non-linear input impedance). If too high then capacitive strays become more significant. 100k to 10MΩ.
R_2: Ratio to R_1 sets optimum slope to minimize offset effect. Empirical result suggests

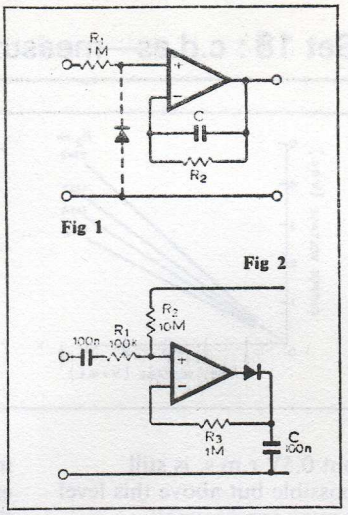


Fig 1

Fig 2

$R_2/R_1 \approx 1.25$, manufacturers suggest $R_2/R_1 \approx 1.6$ for similar circuit.
R_3 has to carry maximum meter current at maximum output voltage i.e. should be < 10kΩ for 1mA meter movement at 5V full-scale and 15V supply.
R_4: Not critical, avoids excessive non-linear loading on amplifier output. 3.3k to 33kΩ.
C sets degree of ripple reduction at low frequencies. $C > 22\mu F$ is necessary for f < 1Hz if needle flutter is to be reasonable. C may be $< 1\mu F$ for higher frequencies (self-inductance of electrolytics may cause problems at h.f.)
D_1: Small-signal silicon diode.

Circuit modifications

● A very simple alternative circuit is that used for the basic tachometer (see also set 17 card 2). In this (Fig. 1) the input transistor of the amplifier non-inverting input provides the rectifying action directly. Reverse half cycles inject current into the damping circuit which may cause disturbance to the other amplifiers in the package. A low voltage-drop diode (germanium, Schottky) may be used to absorb this reverse current but leakage effects with germanium would force the use of lower resistance values. The mean current in the two inputs will become comparable because of the negative feedback while the capacitor removes the ripple as before.

● A peak detector with gain is shown in Fig. 2, in which the capacitor is charged until the current in R_3 equals the sum of the currents in R_2 and R_1 taken at the positive peak of the input voltage. At all other points in the cycle, the diode is non-conducting and some loss of charge takes place through R_3. Resistor R_2 provides a small forward bias. Resistor R_3 cannot be increased greatly without introducing a large error term due to the amplifier input current. The diode is within the feedback loop and the error term due to the diode drop →0 at low frequencies. Amplifier slew-rate limiting prevents the circuit from approaching the frequency response of the previous circuits.

Cross references

Set 4, cards 2, 3, 5, 9, 10.
Set 9, card 12.
Set 17, cards 2, 3.

drifts, but unequal sensitivities at two inputs can be compensated for by trimming the ratio for $v_o = v_i$ at maximum output.
R_3: Set for sufficient current at v' maximum to override current in R_6. Typically $R_3 \approx$ 0.5 to 0.8 R_6. Maximum current should not exceed, say 5mA; too low a current restricts maximum rate of charge.
R_4, R_5: In conjunction with hold/sample pulse must be sufficient to saturate Tr_1, Tr_2.
D_1: Low reverse leakage diode for least error in hold mode.
C_1: High value increases time-constant for minimum drift in hold mode. High-leakage capacitors unsuitable, since leakage should be ≪ 30nA if capacitor is not to be limiting feature of circuit. Too high capacitance slows down charging rate forcing longer sample period.

Circuit modifications

● The four amplifiers in the package are closely matched, and the input current of one

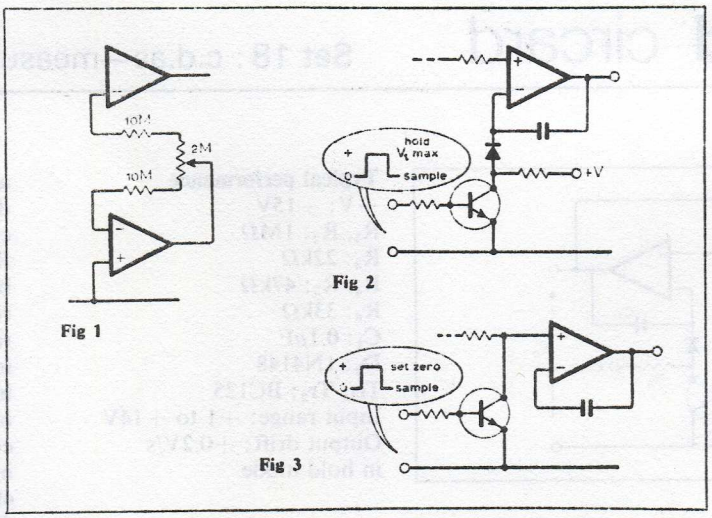


Fig 1

Fig 2

Fig 3

can be used to generate an output voltage that drives a comparable current into the other. Trimming the 2MΩ resistor (Fig. 1) compensates for input-current induced drift while over-compensation can be used to minimize the additional leakage in C_1, D_1. Compensation can be exact at only one combination of C_1 temperature output voltage etc, but with care the output can remain stable to within 1% for several minutes using low cost capacitors.

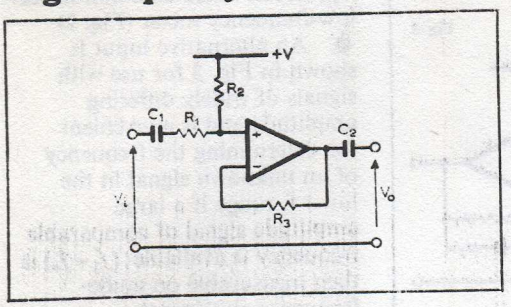
● By using only one of the switching transistors, Fig. 2, the sample mode remains unchanged, while in the hold mode only input voltages below the stored value are ignored i.e. the output voltage is updated each time the input exceeds its previous peak value, holding the new peak pending any further increase. It is a form of peak-reading voltmeter.

● Using the other switching transistor (Fig. 3), then with the pulse input low the transistor is non-conducting and the sample mode is attained. When the pulse input is high the amplifier output is driven to its zero state regardless of the input.

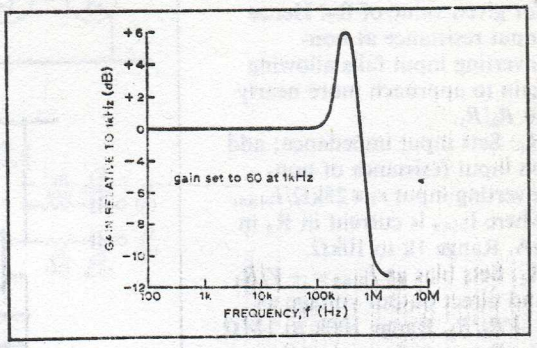
Cross references

Set 4, card 7.
Set 11, card 11.
Set 18, card 7.

High-frequency circuits

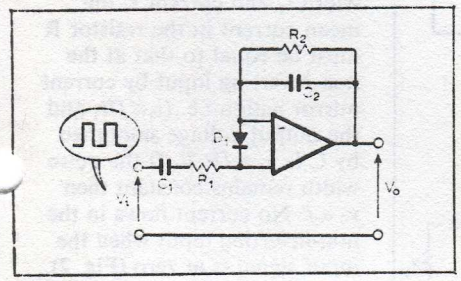


Typical performance
+V: 10V
R_1: 1kΩ
R_2: 220kΩ
R_3: 100kΩ
C_1: 10μF
C_2: 1μF
Voltage gain: 60 @ 100kHz
Input impedance: 1.5kΩ
Output impedance: 100Ω

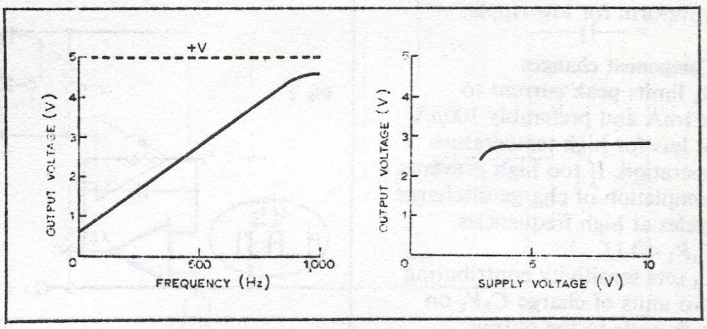


Circuit description
The gain-bandwidth of a feedback amplifier is a good measure of performance over a wide range of frequencies if the fall-off in gain is due to a single dominant lag as for these current-differencing amplifiers. If there is no external path to ground from the inverting input with such an amplifier while a conducting path is provided between that input and the output, there is effectively 100% feedback and the amplifier attains its maximum bandwidth. To inject a signal without reducing the effect of this feedback, the signal is fed directly into the non-inverting input. This is outside the feedback path with this amplifier but couples the signal in via a high impedance path internally (see circuit modifications). The disadvantage is that the feedback exercises no control over the input impedance at the non-inverting input i.e. the input current depends on that impedance and hence on the bias level. For most operating conditions the practical gain is 20 to 40% below that predicted on the basis of R_3/R_1 alone. Output swing available is small at high frequencies being limited by the positive slew-rate limitation of about 0.5V/μs. Hence at 500kHz, the peak-peak output cannot exceed about 500mV without distortion becoming serious. There is a variation in gain with supply voltage largely due to the effect of bias current on the input impedance at the non-inverting input but this can be held to ±10% for a 2:1 variation in supply voltage.

Tachometers



Typical performance
+V: +5V
v_1: 5V pk-pk
R_1: 10kΩ
R_2: 1MΩ
C_1: 1nF
C_2: 0.1μF
for f: 500Hz,
v_o: 2.78V



Circuit description
A tachometer using both inputs of the current-differencing amplifier can reduce the ripple in the output voltage for a given frequency. It has some similarity to the diode pump circuit, in which the two diodes are D_1 and the equivalent input diode at the non-inverting input. When the input goes positive the amplifier input diode is driven into conduction and capacitor C_1 charges through R_1 until the p.d. across it is $(V_1 - V_{be})$, assuming that the positive peak is held for a time appreciably greater than R_1C_1. The current mirror action at the amplifier input ensures that an equal current flows in the inverting input, causing C_2 to charge with the output going positive. When the input returns to its most negative value, D_1 comes into conduction and C_1 discharges. Current drawn through R_2/C_2 is in the same sense in both cases i.e. the effects of charging and discharging C_1 are additive at the output, doubling the effective frequency of the pulses. The mark/space ratio of the pulses is not important and need not even be constant provided only that the duration of each is sufficient to allow complete charge/discharge. Overall sensitivity is controlled by C_1 and R_2 with R_1 serving to limit the peak input current and C_2 to smooth the output d.c. In each cycle C_1 gains and loses charge of C_1v_1. This corresponds to a net current in R_2 of about $2fC_1v_1$ if f is the repetition frequency, a factor 2 coming from the fact that R_2 has to carry current corresponding to the direct discharge of C_1 via D_1 and also a current equal to the charging current because of the current mirror action as outlined above.

Component variations

+V: Normal supply range for amplifier. Higher voltages allow higher input bias current for given value of R_3. Hence input resistance at non-inverting input falls allowing gain to approach more nearly to R_3/R_1.

R_1: Sets input impedance; add on input resistance of non-inverting input $r_i \approx 25k\Omega/I_{bias}$, where I_{bias} is current in R_2 in μA. Range 1k to 10kΩ.

R_2: Sets bias as $I_{bias} = +V/R_2$ and direct output voltage as $+VR_3/R_2$. Range 100k to 1MΩ.

R_3: Sets gain in conjunction with R_1. For $R_1 \rightarrow 0$ overall voltage gain $\rightarrow 20 \times$ magnitude of supply voltage in volts.

C_1, C_2: Chosen in conjunction with R_1 and load resistance to define low-frequency cut-off. Typically 0.1 to 10μF.

Circuit modifications

● The non-inverting input is a current mirror with the input transistor behaving as an almost ideal p-n junction having transconductance g_m of 40mA/V (mS) at a current of 1mA with g_m inverse to the bias current. The exponential characteristic restricts the signal swing to a few millivolts if distortion is to be minimized. Such an input stage can be added to other amplifiers provided that the direct voltage at the amplifier input keeps Tr_2 out of saturation (Fig. 1).

● A second high frequency application takes advantage of this diode non-linearity, by injecting two high frequency signals at f_1, f_2. If the difference in frequency between these signals lies within the amplifier gain range and the amplitudes are large enough to give significant distortion products then a term at $f_1 - f_2$ appears at the amplifier output. Other terms f_1, f_2, $f_1 + f_2$ etc lie outside that range and the circuit has acted as a non-linear low-frequency mixer (Fig. 2).

● An alternative input is shown in Fig. 3 for use with signals of widely differing amplitude and is convenient for determining the frequency of an unknown signal in the low r.f. range if a large amplitude signal of comparable frequency is available; $(f_1 - f_2)$ is then measurable on audio-frequency equipment.

Fig 1

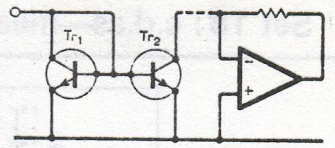


Fig 2

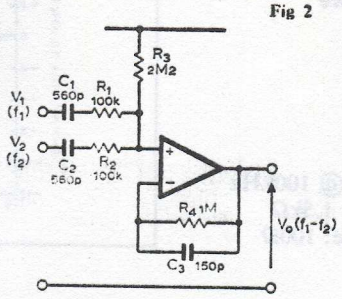
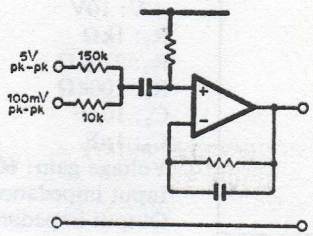


Fig 3



Cross references

Set 12, cards 1, 3, 8, 9.

Hence the mean output voltage is $\approx 2fC_1v_iR_2$ ignoring V_{be} effects. The time constant C_2R_2 should be $\ll$ period of waveform for low ripple.

Component changes

R_1 limits peak current to < 1mA and preferably 100μA or less for high temperature operation. If too high prevents completion of charge/discharge cycles at high frequencies $C_1R_1 < 0.1/f$.

C_1 sets sensitivity contributing two units of charge C_1V_1 on each cycle to the output. 100pF to 1μF.

R_1: Average current flow in R_1 is equal to the average of the charge gained and lost by C_1 as above. Because amplifier input current is low a mean current in R_2 of about 1μA is still sufficient to give moderate accuracy i.e. R_2 can be as high as 10MΩ but better accuracy for values of 1MΩ or less.

C_2: Time constant R_2C_2 determines ripple remaining on output with $R_2C_2 \ll 1/f$ for minimum ripple. C_2 must be low leakage or leakage resistance will cause loss of accuracy. 0.01 to 1μF.

D_1: Not critical. Any silicon diode.

Circuit modifications

● Transfer function of circuit is linear in v_o/f but there is an output offset of $V_{be} + (I_-)R_2$, where $I_- \approx 30$nA and $V_{be} \approx 0.55$V. By using a second amplifier with an identical feedback resistance and taking the output signal as shown, the output is substantially zero for zero input signal i.e. the transfer-function remains linear but passes through the transposed origin. The offset has good temperature compensation (Fig. 1).

● Simpler tachometer circuits are possible with some relaxation in specifications. For input pulses of defined width t_1 and current I, the mean current in the resistor R must be equal to that at the non-inverting input by current mirror action i.e. $i_R \approx fIt_1$ and the output voltage smoothed by C is $v_o \approx fIt_1R$. If the pulse width remains constant then $v_o \propto f$. No current flows in the non-inverting input when the input signal is at zero (Fig. 2).

● The output may be made to pass through zero by adding a diode at the output inside the feedback loop and with common-mode biasing. A load resistance $\ll$200kΩ should be present to ensure that the current in R_f can flow to ground while developing a very small voltage (Fig. 3).

Fig 1

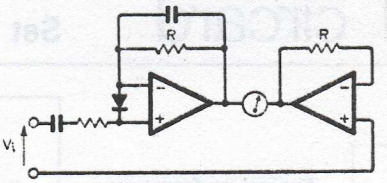


Fig 2

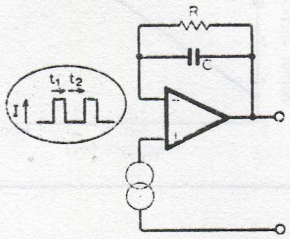
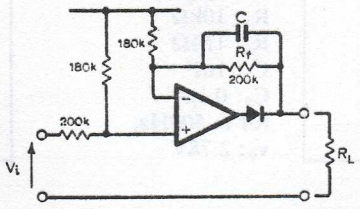


Fig 3



Cross references

Set 3, card 3.
Set 13, card 6.
Set 14, cards 6, 9, 10.