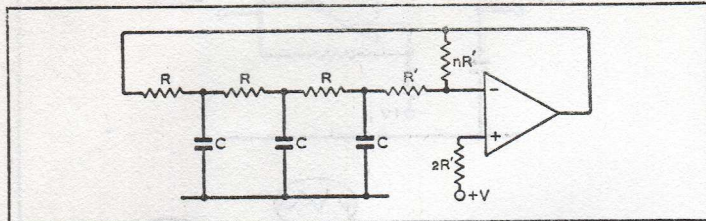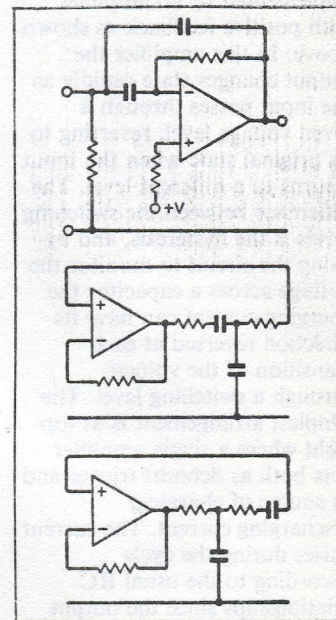## Generators

Circuit description—1

Four types of generator are considered here. They can be summarized as sine, relaxation, square/triangle and d.c. The last of these, the group of circuits normally called voltage/current regulators, can be considered as generators of direct voltage or current. Alternatively, they can be dealt with as d.c. amplifiers with input signals provided by constant voltage/current reference elements, e.g. Zener diodes (see set 16). For cisoidal oscillators the basic requirement is a passive network giving a phase-shift of 0 or π at a single frequency. This may or may not be accompanied by a maximum in the magnitude of the transfer function, but in either case it dictates to which input the feedback should be returned. The circuit oscillates at the frequency for which the loop has zero phase-shift and amplifier phase-shifts cause errors at high frequencies. The classic phase-shift oscillator can be used as above, with the amplifier providing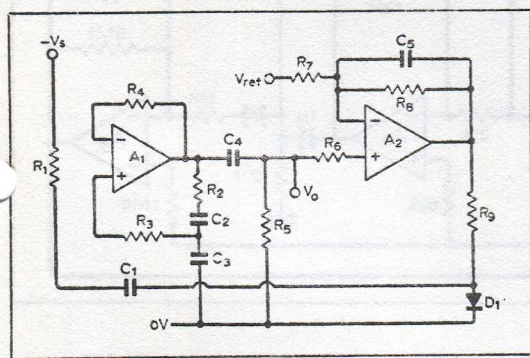 more than enough gain. Negative feedback from output to inverting input sets the amplifier gain to overcome the losses in the passive network. Largest signal at amplifier output, least distortion across last capacitor. Make $R' \gg R$ to minimize loading of network. Any band-pass filter may be inserted into the feedback loop of a system, allowing the overall loop gain to reach the critical condition only at the filter centre frequency. To adapt the more usual Wien networks to current differencing amplifiers, it is sufficient to take any such network whose output has a grounded resistor, and use the current in the resistor as a feedback—the amplifier having a low enough input resistance to act as a virtual earth. No mechanism is shown for amplitude control, but the precisely defined input non-linearities allow for simple solutions as shown later.

Circuit description—2

The common element to many non-sinusoidal waveform generators is a Schmitt trigger,
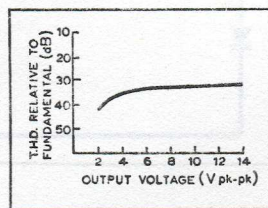
RC oscillators

Typical performance
A_1, A_2: $\frac{1}{2}$ LM3900
Supply: +20V
R_1: 220kΩ
R_2, R_3: 33kΩ
R_4: 120kΩ
R_5: 100kΩ
R_6: 1.8MΩ
R_7: 2.2MΩ
R_8: 5.6MΩ
R_9: 15kΩ
C_1: 0.68μF
C_2, C_3: 10μF
C_4: 0.1μF
C_5: 1μF

D_1: 1N914
f : 500Hz

$$f \approx \frac{1}{2\pi(R_2 R_3 C_2 C_3)^{\frac{1}{2}}}$$

v_o: 7V pk-pk $\pm$ 0.2dB for V_s 12 to 20V.

Circuit description

The circuit has two distinct sections. Amplifier A_1 together with R_1 to R_4 and C_2, C_3 constitutes a complete RC oscillator, in which the positive feedback via R_3 exceeds the negative feedback via R_4. Choosing $R_1 \approx 2R_4$, the amplifier output is biased to $\approx V_s/2$ since the d.c. feedback ensures almost equal currents in R_1, R_4. The second amplifier amplifies and filters the output of A, after a.c. coupling via C_4, R_5 and half-wave rectification via the non-inverting input of A_2. The addition of a reference voltage acting via R_7 causes the d.c. output of A_2 to vary the bias current in D_1 in such a way that it diverts a varying proportion of the a.c. feedback from the non-inverting input of A_1. Allowing for the time constants of the loop, the output of A_2 will vary until the half-wave rectified sine-wave output of A_2 is comparable with V_{ref}. The non-linearity of D_1 V/I characteristics does not introduce serious distortion, since it matches that of the input characteristics of A_1. Because the amplifiers are current-differencing units, the conventional Wien bridge has been rearranged, i.e. instead of grounding R_1 and using the p.d. across it as the frequency-dependent feedback, the current through it is fed back, taking the amplifier input as a virtual-earth. The output voltage of A_1 has a d.c. term of $\approx V_s/2$ and the superposed a.c. may have a peak-peak value of up to 80% of the supply voltage before the onset of clipping. The relatively low open-loop gain of the amplifier does not allow very low distortion levels but the ability to control the amplitude of oscillation by an external direct voltage, while using only two out of the four amplifiers within the i.c.
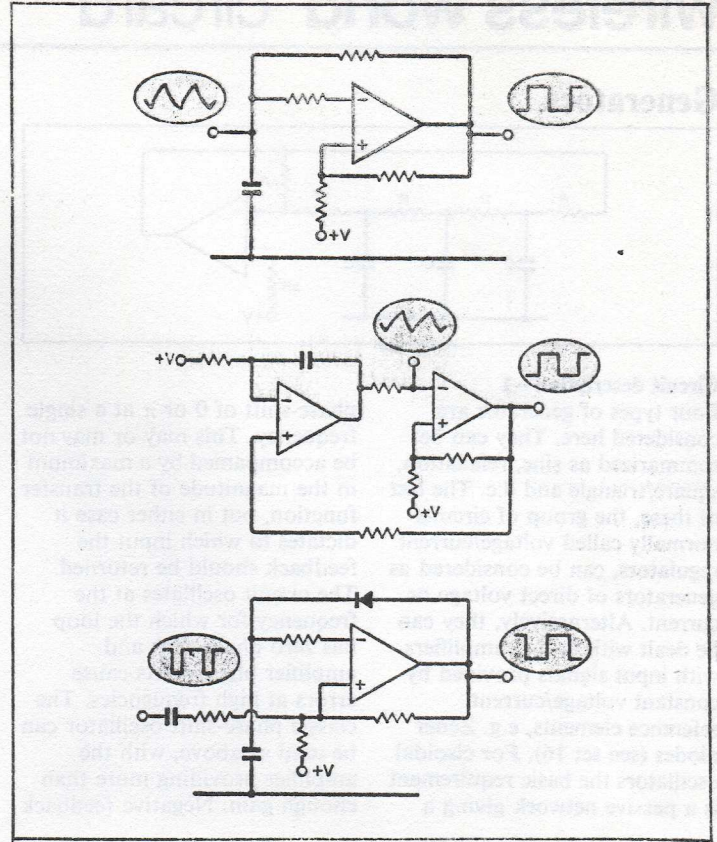
Component changes

R_1, R_4: Ratio $\approx$ 2:1 to bias A_1
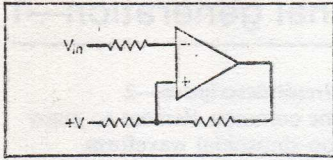
implemented by an amplifier with positive feedback as shown above. In this amplifier the output changes state rapidly as the input passes through a given voltage level, reverting to its original state when the input returns to a different level. The difference between the switching levels is the hysteresis, and by using the circuit to monitor the voltage across a capacitor the charging current can have its direction reversed at each transition of the voltage through a switching level. The simplest arrangement is at top right where a single amplifier acts both as Schmitt trigger and as source of charging/discharging current. The current varies during the cycle according to the usual RC relationships since the output voltage has a constant value for each switched state. If the capacitor forms part of an integrator then the charging current has one of two fixed values, because the virtual earth action prevents the charging voltage across the capacitor from modifying the current. A further modification of this circuit uses an additional diode or transistor to reverse the net current flow to the amplifier by interrupting the current to either the inverting or non-inverting input. Selection of suitable resistors gives a net-charging current that reverses its direction while remaining of equal magnitude and being controlled by an external direct voltage i.e. a voltage controlled oscillator results. If the first circuit is adapted to have one stable state then it can be triggered by an external pulse into the unstable state where it remains until the capacitor has completed its charge (or discharge) sequence. The resulting monostable circuit may be edge- or level-triggered.

output $V_s/2$, R_4 is chosen to provide less negative feedback than the positive feedback via R_2, R_3, C_2, C_3 i.e. $R_4 > 3R_2$.
R_2, R_3: $R_2 = R_3$. Together with C_2, C_3 defines the frequency of oscillation. R_2 10k to 1MΩ.
C_2, C_3: $C_2 = C_3$. 1000pF to 10μF. Large R values can be used with small C values for economy, but layout/screening need to be watched to avoid hum.
C_4: Not critical. 0.01μ to 100μF. Higher values only required for lower load resistances. Circuit output current should not exceed 1mA for lowest distortion.
C_1: Must have low reactance at signal frequencies—at least 0.5μF for 1kHz.
R_6, R_7, R_8, R_9: Control mean current in and hence slope resistance of D_1. High values to minimize required value of C_5. Time constant period of waveform.
V_{ref}: 0 to 4V. Controls output voltage R_4 can be varied to increase or decrease the control effect required via D_1.
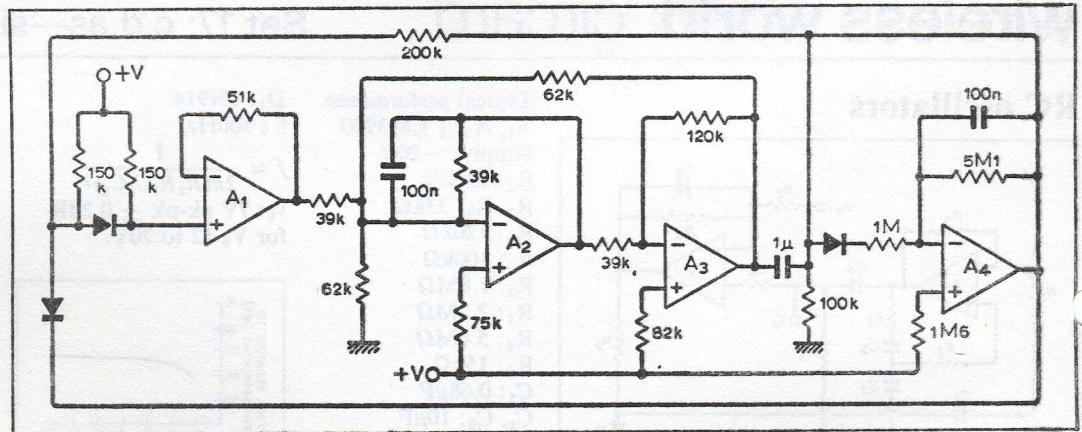
V_s: Oscillations sustained at lower supply voltages but amplitude control difficult.

Circuit variations
● The principle of the circuit is that of an RC oscillator using A_1 and a modified Wien-network, followed by a signal level sensing circuit (A_2) that modifies the loop-gain of the oscillator feedback loop. Any other RC oscillator can be substituted for A_1 circuit, but amplitude control via a biased diode is optimum, as the diode and amplifier input non-linearities cancel.
A peak-sensing circuit is an alternative, and a diode peak detector can replace A_2 with power control of amplitude.
● A recently described oscillator uses all four amplifiers and achieves the very low distortion of 0.1%. Amplifier A_2 is a band-pass filter with A_3 setting the Q.

Feedback via the 100-kΩ resistance sustains oscillations at the filter centre-frequency. Amplifier A_4 senses the mean-rectified output and controls the amount of feedback via the attenuation due to the diodes so as to keep the output as a well-defined function of the reference voltage. Resistor values are optimized to stabilize the output against temperature variation.
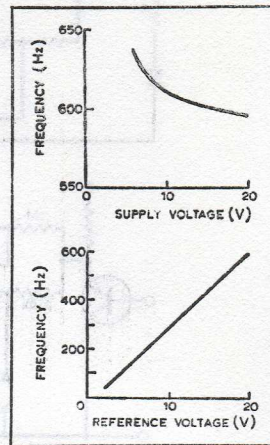
Voltage-controlled oscillators
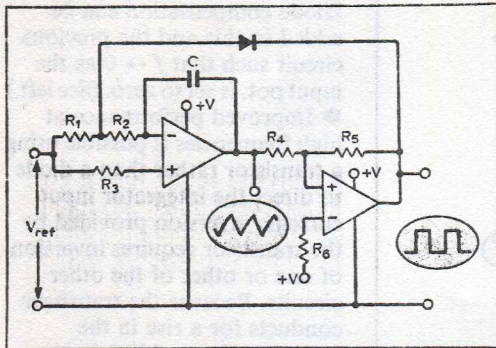
Typical performance
IC: $\frac{1}{2}$ LM3900
Supply: 10V
R_1: 220kΩ
R_2: 270kΩ
R_3, R_4: 1MΩ
R_5, R_6: 1.2MΩ
C_1: 1nF
Square-wave output: 9V pk-pk
Triangular wave: 7.5V pk-pk
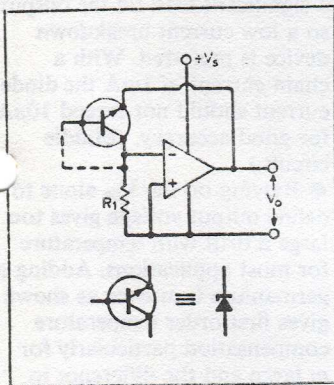Frequency: 610Hz

Circuit description

A basic method of generating square/triangle waves is to interconnect an integrator and a Schmitt trigger circuit. With correct phasing the integrator output changes linearly with time between the threshold voltages of the Schmitt, causing the output to reverse and with

it the direction of the integrator output slope. To bring the frequency under the control of an external voltage the switched output is used to reverse the net current into the integrator, but leaving the magnitude defined by the control voltage. A current differencing amplifier is particularly suited to this

technique, since the net charging current is the difference between the two input currents. If these are set in the ratio 2:1 and the larger current is switched off, the net current changes sign, remaining of equal magnitude i.e. a triangular wave results at the integrator output with

peak-to-peak voltage equal to the hysteresis of the Schmitt trigger circuit.

Consider the Schmitt output positive; the diode is reverse-biased and with $R_1 + R_2 = R_3/2$, the net integrator input current is negative. Integrator output ramps negatively until the lower threshold voltage of the Schmitt is reached. Output of the Schmitt falls almost to zero and the diode conducts by passing the current in R_1 to ground through the output of the Schmitt circuit. (A residual current flows in R_2 since the output of the Schmitt is typically a 100mV but the current is small compared with the normal charging current.) The net charging current is now positive and the integrator output ramps positively until the cycle is completed on chargeover at the upper threshold level. The rate of

Voltage regulators

Typical performance
Supply: +15V
IC: $\frac{1}{4}$ LM3900
Tr1: BC125*
R_1: 10kΩ
V_o: 7.7V
R_1: 2kΩ
ΔV_o: +15mV
(for $\Delta V_s = -5$V)
+25mV (for $\Delta T = +25$ deg C)
*Use of reverse base-emitter junction gives good low-current breakdown. Using reverse collector-emitter raises voltage by 0.6V, changes drift by about −2mV/deg C.

Circuit description

When negative feedback is applied around a current-differencing amplifier such as the LM3900, the inverting input terminal remains at 0.6V at 0 °C falling to nearly 0.4V at 75 °C. In the voltage regulator shown the

voltage across R_1 is defined by these values, fixing the current in Tr_1 which acts as a Zener diode. Amplifier input current is very small ($\approx$ 30nA) allowing currents between 1μA and 1mA to be adequately defined. Output voltage is the sum of the input V_{be} and the
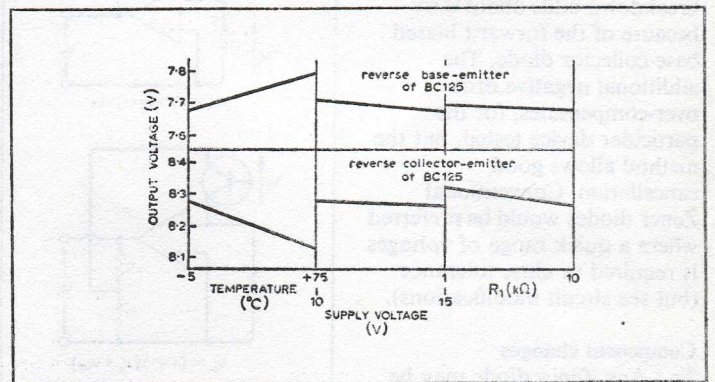
Zener voltage. Two sources of variation exist:
—direct variation in input voltage (V_{be}) as above of about −2.5mV/deg C together with a fall of 2 to 3mV for each 1V increase in the supply.
—corresponding variation in

Zener voltage caused by the resulting current variation together with its own temperature coefficient.

If a Zener diode is available with a positive temperature drift cancellation between that drift and the input drift is possible, though complicated by

charging is proportional to V_{ref} which may be derived from a potentiometer across the supply or from an external source with $f \propto V_{ref}$ to a good approximation.

Component changes
R_1, R_2, R_3: For equal positive and negative slopes to the triangular wave (and hence unity mark-space ratio for the square wave). $R_1 + R_2 = R_3/2$. To minimize loading on source these resistors may range from 100k to 10MΩ. $R_1 \approx R_2$ but may be different to use preferred values while meeting above conditions.
C: sets frequency of oscillation and $f \propto 1/C$ except at high frequencies where finite rise and fall times limit the response. Typically C is 1n to 10μF.
R_4, R_5, R_6: control upper and lower threshold voltages and have peak-peak value of triangular wave. For $R_5 = R_6$ and $R_4 = kR_5$, the hysteresis is $\approx k$ (square-wave output). Reducing the hysteresis increases the frequency of
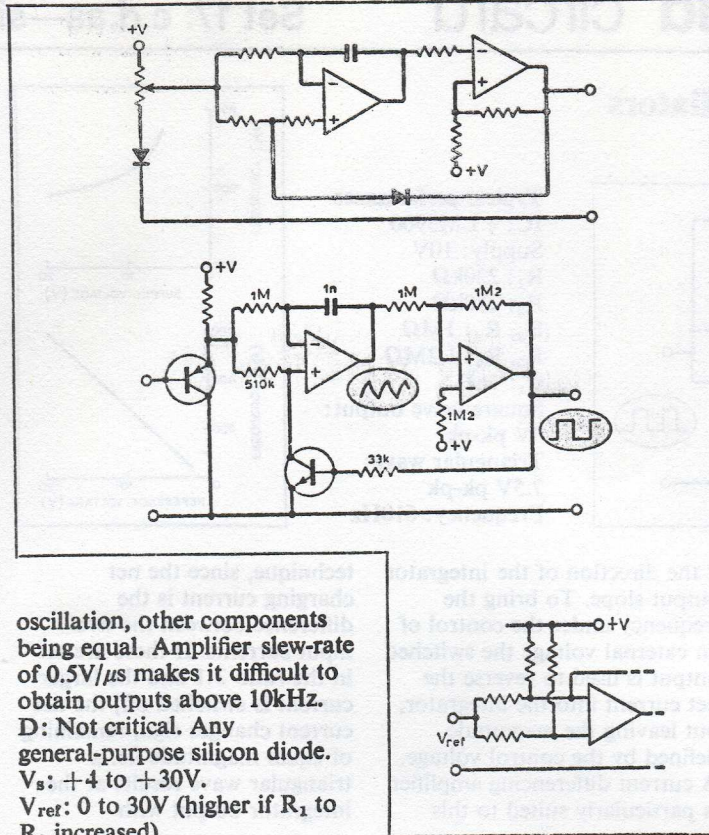
oscillation, other components being equal. Amplifier slew-rate of 0.5V/μs makes it difficult to obtain outputs above 10kHz.
D: Not critical. Any general-purpose silicon diode.
V_s: +4 to +30V.
V_{ref}: 0 to 30V (higher if R_1 to R_3 increased).

Circuit variations
● Using an inverting Schmitt, but with the feedback shunting the current from the non-inverting input of the integrator leaves the phasing correct for sustained oscillations. Diode compensation can be added to this and the previous circuit such that $f \to 0$ as the input pot. is set to zero. (See left.)
● Improved performance at high frequencies is possible using a transistor rather than a diode to direct the integrator input current; inversion provided by the transistor requires inversion of one or other of the other circuits. Because the transistor conducts for a rise in the Schmitt output of little more than one V_{be}, the rise time of the Schmitt no longer presents such a serious limitation to the frequency at which oscillation can be sustained.
● Adding bias resistors to +V sets a minimum value to the frequency of oscillation for $V_{ref} = 0$ i.e. the frequency can be controlled over any prescribed range. (Bottom)

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the current variations. The use of a small-signal planar transistor with V_{eb} breakdown of about 7V gives partial cancellation while using the V_{ec} breakdown adds about 0.6V because of the forward biased base-collector diode. The additional negative drift over-compensates, for the particular device tested, but the method allows good cancellation. Conventional Zener diodes would be preferred where a quick range of voltages is required or close tolerance (but see circuit modifications).

Component changes
Tr_1: Any Zener diode may be used in principle since the output current is limited low-current operation is an advantage, and any planar transistor may be used as reverse base-emitter breakdown typically lies between 6 and 12V, being well-defined for a particular transistor type.
R_1: defines diode current as V_{be}/R_1 where V_{be} is that of the i.c. input transistor ($\approx$ 550mV
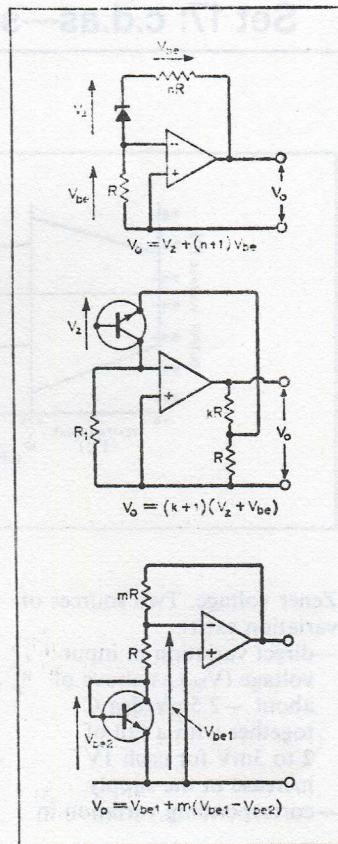
at room temperature, −2.5mV/deg C). Select for Zener current of say 100μA to 2mA depending on type, down to 1μA for planar diode/transistor.
V_s: 4 to 36V (down to 3V in some cases).
V_o: up to 36V. Limited by available diodes but see circuit modifications.
I_o: 0 to 10mA. May be boosted by adding emitter follower at output of amplifier (*inside* feedback loop).

Circuit modifications
● Additional temperature compensation is introduced by adding resistance in series with the Zener diode. Currents in the diode and resistors are almost equal since the amplifier input is small ($\approx$ 30nA). Hence $V_o = V_z + V_{be} + nV_{be}$. Each equivalent V_{be} increases the output by $\approx$ 0.55V, adding a temperature drift term of −2.5mV/deg C. (Top circuit.)
● To increase the output voltage Zener/transistor (e.g. selected for its temperature

dependence) the diode is tapped onto a portion of the output voltage. The potential divider should not be significantly loaded, nor should it constitute a significant load on the output so a low current breakdown device is preferred. With a chain current of 1mA the diode current should not exceed 10μA for good accuracy. (Middle circuit.)
● Relying on the V_{be} alone to define output voltage gives too large a drift with temperature for most applications. Adding a germanium transistor as shown gives first-order temperature compensation particularly for m large and the difference in the V_{be} values is in the range 400 to 450mV. (Bottom circuit.) The three techniques suggested may be used in various combination as well as separately.
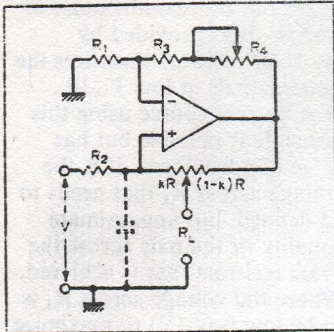
Cross references
Set 6, cards 1, 2, 7 & 10.

$V_o = V_z + (n+1)V_{be}$

$V_o = (k+1)(V_z + V_{be})$

$V_o = V_{be1} + m(V_{be1} - V_{be2})$

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Constant-current circuits

Typical performance
IC: ¼ LM3900
Supply: +15V
R_1, R_2: 10kΩ
R_3: 8.2kΩ
R_4: 2.2kΩ for particular circuit
R: 10kΩ
k: 0.5
V: 7.7V for I_L 1.5mA

Circuit description
Many circuits used with conventional operational amplifiers are adaptable for use with current differencing amplifiers. To provide a constant-current drive to a grounded load is difficult in both cases since each amplifier has its output referred to ground so that feedback can only be taken in shunt with the load, i.e. lowering the output impedance. If the load can float then the feedback may be taken across a grounded resistor in series with the load. An alternative technique combines negative and positive feedback in such a way that at some point in 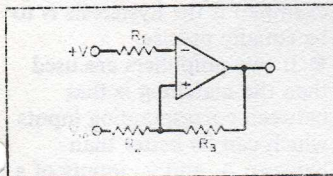the network the output impedance tends to infinity. By injecting voltages/currents at other points in the system, a load connected between that particular point and ground will carry a current independent of the load resistance. As shown, R_4 is used to adjust the negative feedback such that for very high load resistances, the negative and positive feedback are almost in balance. In the ideal case, this is achieved for $(R_3 + R_4)/R_1 = R/R_2$. Current in the load may then be varied in one of three ways, each of which has minimal effect on the output resistance: variation of the input voltage V; insertion of an alternative/additional voltage in series with R_1; variation in the tapping point of the
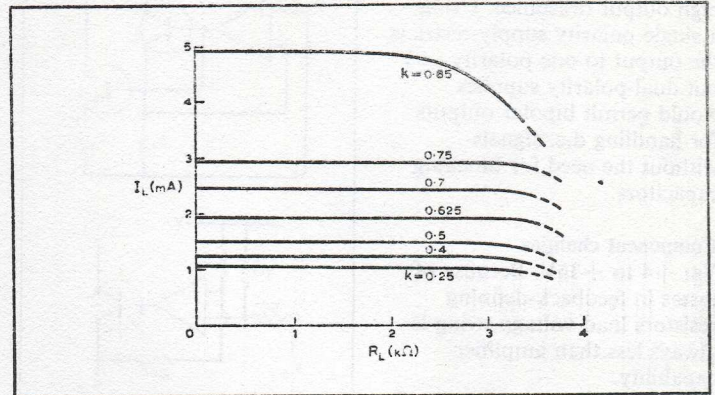
Schmitts & comparators

Typical performance
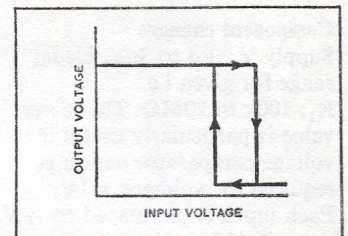IC: ¼ LM3900
Supply: + 15V
R_1: 1MΩ
R_2: 2.2MΩ
R_3: 10MΩ

$$V_u = +V\left(\frac{R_1}{R_2} + \frac{R_1}{R_3}\right)$$
$$+ V_{be}\left(1 - \frac{R_1}{R_2} - \frac{R_1}{R_3}\right)$$
$$V_1 = +V\left(\frac{R_1}{R_2}\right)$$
$$+ V_{be}\left(1 - \frac{R_1}{R_2} - \frac{R_1}{R_3}\right)$$

V_{be}: of input transistors assumed equal and ≈ 0.5V.
Hysteresis, $V_u - V_1 = +VR_1/R_3$
Measured hysteresis: 1.51V.
Output rise-time: 30µs (corresponding to 0.5V/µs slew rate limitation for positive-going output)
Output full-time: 2µs

Circuit description
The input section of current-differencing amplifiers rely on the accuracy of matching of transistors in a current mirror to define the operating levels. It is not possible to obtain the precision of switching levels by such a method as can be achieved using a long-tailed pair and more conventional circuitry. Where a moderately wide hysteresis, say, 1V or greater, is acceptable and neither upper or lower thresholds need be defined to within a small percentage, Schmitt circuits can be simply constructed offering the other advantages of positive and rapid switching. The limited slew-rate of the amplifier makes it comparable in performance in this respect to op-amps such as the 741, but the internal compensation cannot be removed to allow speeds comparable to the uncompensated op-amps (301, 748, etc) let alone high-speed comparators. The main uses are likely to be as part of signal processing systems, alarm circuits, waveform generators, etc.
Switching takes place, assuming ideal current mirror action, when the current in R_1 equals the sum of the currents in R_2, R_3. In each case the amplifier internal V_{be} of about 0.5V has to be taken into account, effectively raising both upper and lower thresholds by somewhat less than 0.5V. To a first order approximation, hysteresis depends only on the resistor values, while the input resistance may be made >1MΩ. This is because the inverting stage input current of ≈ 30nA allows reasonable accuracy of switching levels even though the currents in the resistors are only a few microamperes. Increasing R_3 reduces the upper threshold without changing the lower one. Increasing R_2 reduces both thresholds by the same amount leaving the hysteresis unchanged. Increasing R_1 raises both threshold voltages proportionately,

resistor R. The last method can be used to obtain a 5:1 spread in sensitivity while retaining a high output resistance. Using a single polarity supply restricts the output to one polarity (+) but dual-polarity supplies would permit bipolar outputs for handling d.c. signals without the need for blocking capacitors.

Component changes
Vs: +4 to +36V. Because of losses in feedback-defining resistors load voltage swing is always less than amplifier capability.
R_1, R_2: 10kΩ is near lower end of working range, with amplifier normally operating with input resistor of 100kΩ upwards. However, values required where current of several mA required in load.
R_3, R_4: If high impedance is sufficient and it is not required to trim for output impedance → ∞, replace by fixed resistance (== R for R_1 == R_2). Negative output resistance attained if feedback resistance to inverting
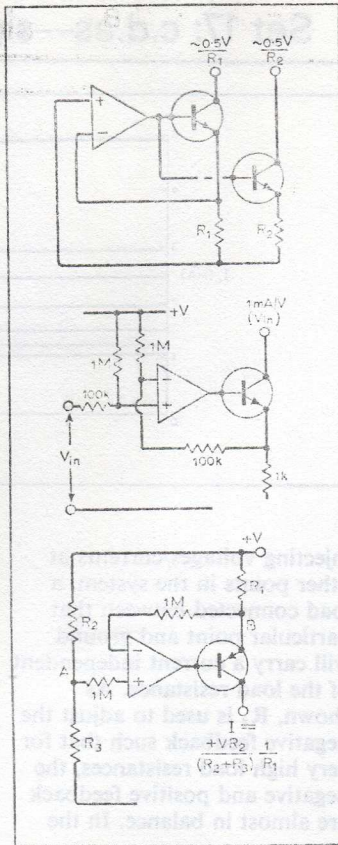
input is too large.
k: Can be varied from 0.2 to 0.9. At high values, relatively large currents obtainable but with some loss of accuracy.
V: Variable over range 2 to 10V. For input voltages too low, V_{be} errors at input prevent linearity of I_L against V.

Circuit modifications
● By adding transistors, the feedback may be taken from across one emitter resistor as would be the case for a voltage amplifier (top circuit.) The output is taken from the transistor collectors each or which carries a collector current almost equal to its emitter current if the transistors have high current gains. In the simplest arrangement the current is defined by the amplifier internal V_{be} with a consequent temperature dependence to the currents (which may be set to any required ratios by varying R_1, R_2, etc.). Any of the techniques used in voltage regulators may be used to achieve better

control over the voltage across R_1.
● A voltage-controlled current sink as shown forces the voltage across the 1kΩ resistor to match the input voltage giving an overall transconductance of 1mA/V. Bias provided by the 1MΩ resistors linearizes the characteristic at low V_{in}/I_L.
● A current source using this principle is possible but has some disadvantages. It is the voltage across R_1 that needs to be defined, but approximate equality of the p.ds across the 1MΩ resistors that is achieved. Where the voltage across R_1 is to be low (say 1V) to maximize load voltage, small unbalance in the input current sensitivities produce small voltage differences at A & B. These small errors then represent a large error in the small voltage across R_1 and hence in the load current. (Bottom circuit.)

Cross references
Set 6, cards 4 & 12.

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leaving the hysteresis in the same ratio to each as prior to the increase.

Component changes
Supply V: +4 to 36V. Usual range for given i.c.
R_1: 100k to 10MΩ. The lower value is particularly useful if voltage comparator action is required for voltages <1V. Each input is pre-biased to +V through 1M to 5MΩ resistors.
R_2: As above. If used as a comparator R_3 is absent, and comparison is possible between unequal voltages i.e. the output can be made to swing between its limits as V_{in} passes V_+/n if $R_2 = R_1/n$. Comparison of negative voltages are also possible provided bias network accommodates common mode currents. Since currents are being compared, the use of suitably large resistors allows comparison of very large positive or negative voltages, but with the limited accuracy implied by the current-mirror input.
R_3: 1M to 22MΩ. Sets
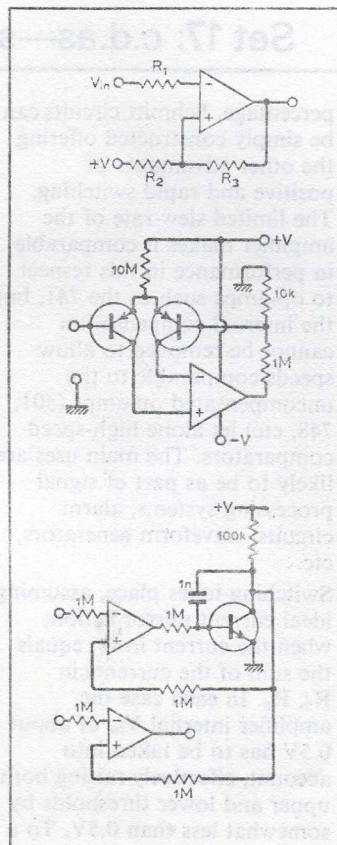
hysteresis and would be absent for comparator action. Can generally be added to any comparator arrangement to introduce, for example, small amounts of hysteresis to prevent output jitter due to noise.

Circuit modifications
● The position of the input and reference voltages (+V was used in the circuit overleaf) may be interchanged to give a non-inverting Schmitt. The availability of inverting and non-inverting Schmitts is of importance in the design of such circuits as wave-form generators. The thresholds and hysteresis are approximately:
$$V_u = +V R_2/R_1,$$
$$V_1 = +V\left(\frac{R_2}{R_1} - \frac{R_2}{R_3}\right)$$
∴ hysteresis == $+V R_2/R_3$.
● If a p-n-p long-tailed pair is added at the input the resulting amplifier may be used as a comparator or as a Schmitt (as shown). The input impedance is extremely high if high-gain low current transistors are available, and any degree of

matching for the input transistors, may be chosen for high precision. It is necessary to clip the output voltage swing more precisely (with a resistor-Zener combination for example) if the hysteresis is to be equally precise.
● If two amplifiers are used then the matching is that between corresponding inputs which can be better than between + and — inputs of a single amplifier. One amplifier plus the output transistor has overall negative feedback (transistor is an inverter) and the equal current forced into the two non-inverting inputs forces the transition point in the second amplifier output to occur for equal currents at the two inverting inputs. Again comparison can be made between unequal voltages but more account has to be taken of the effects.
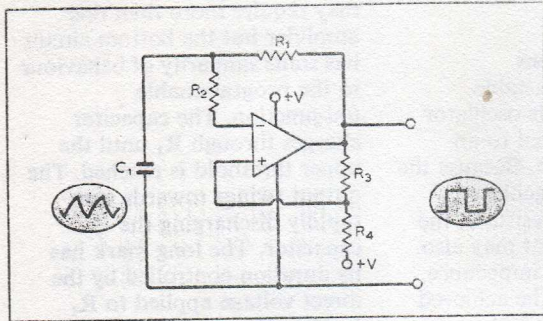
Cross references
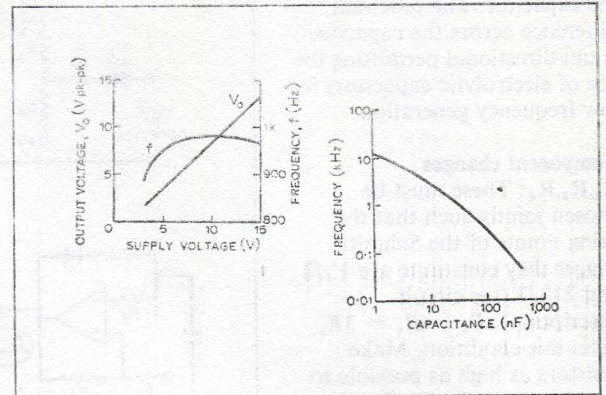Set 2, all cards.
Set 17, cards 3, 7, 8 & 9.

Astable multivibrators

Typical performance
IC: $\frac{1}{4}$ LM3900
Supply: $+10$V
R_1: 15kΩ
R_2: 1.8MΩ
R_3, R_4: 5.6MΩ
C: 47µF
f: 975Hz
v_0: 9V pk-pk
Rise time ≈ 20µs
Fall time ≈ 10µs

Circuit description
The amplifier together with resistors R_2, R_3, R_4 constitutes a Schmitt trigger. The output switches between the two extremes (≈ +100mV and ≈ 0.8V below V+). When the output is low C_1 is discharged through R_1 until the lower threshold of the Schmitt is reached. The output switches rapidly to its most positive value and the capacitor is charged positively. When the upper threshold is reached the Schmitt output is reversed and the cycle restarts. If R_2, R_3, R_4 are chosen to make the threshold voltages $V_+/3$ and $2V_+/3$ respectively then the voltage across the capacitor swings between these limits, while the output approximates to a square wave with almost unity mark-space ratio. For the highest accuracy a number of conditions must apply: The current in R_2 must be very low compared with the charging current through R_1; the output voltage swing should be as nearly as possible equal to the supply voltage; and the accuracy of the current-differencing action should be high (this places a restriction on the minimum currents in R_2, R_3, R_4). If these constraints are met then both the frequency and the mark-space ratio remain substantially constant over a wide range of supply voltages. Any increase in supply voltage produces proportional and

Monostable multivibrators
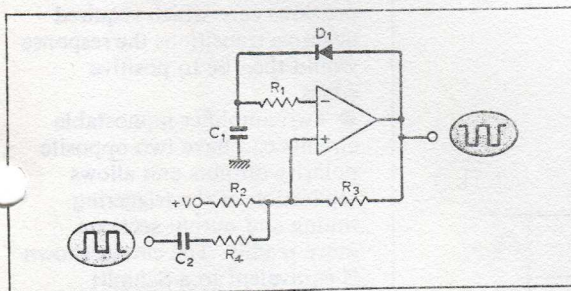
Typical performance
Supply: $+10$V
R_1, R_3: 1MΩ
R_2: 10MΩ
R_4: 100kΩ
C_1: 220pF
C_2: 100pF
D_1: 1N4148
f: 100Hz
v_{in}: 0.5V pk-pk square-wave
Pulse-width: 0.66ms
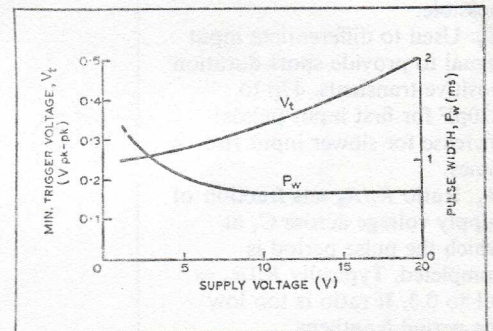
Circuit description
The circuit is closely related to the pulse generator modification of the astable circuit, and to the unijunction equivalent (card 7). The feedback network is designed so that the circuit normally latches into one particular state, with the output high. This is because in the low stage the diode inhibits current flow into the inverting input. Current in R_2 drives the output high initially and with the sum of the currents in R_2 and R_3 exceeding that in R_1. The first negative-going pulse drives the output temporarily low, the diode becoming reverse-biased. The capacitor discharges through R_1 with only R_2 contributing any current to the non-inverting input. Discharging continues until the voltage across the capacitor is down to a fraction of the supply given by R_1/R_2. At this point, the inverting input current comes into balance with that at the non-inverting input, the output begins to rise and the positive feedback causes the cycle to complete itself rapidly. The diode conducts, rapidly changing the capacitor to a volt or so below the positive supply voltage and the circuit is ready for the following trigger pulse. The positive-going slew-rate limit of 0.5V/µs limits the minimum pulse-width that can be defined with any accuracy for a 20-V supply and a pulse of nominal length 100µs this slew rate should add up to 45% to its effective length.

Component changes
+V: +4 to +36V. Monostable action with increasing pulse-width and lowered output is possible to below 2V with some samples though outside specification.
C_1: Large values may be used

hence self-cancelling increases in the magnitude and rate-of-change of voltage across the capacitor. The potential difference across the capacitor is uni-directional permitting the use of electrolytic capacitors for low frequency generation.

Component changes

R_2, R_3, R_4: These must be chosen jointly such that the firing points of the Schmitt trigger they constitute are $V_+/3$ and $2V_+/3$ (see circuit description). $R_3 = R_4 = 3R_2$ gives this condition. Make resistors as high as possible to avoid loading R_1, C_1 charging circuit i.e. $R_2 > 100R_1$. Typically R_2 1M to 10MΩ.
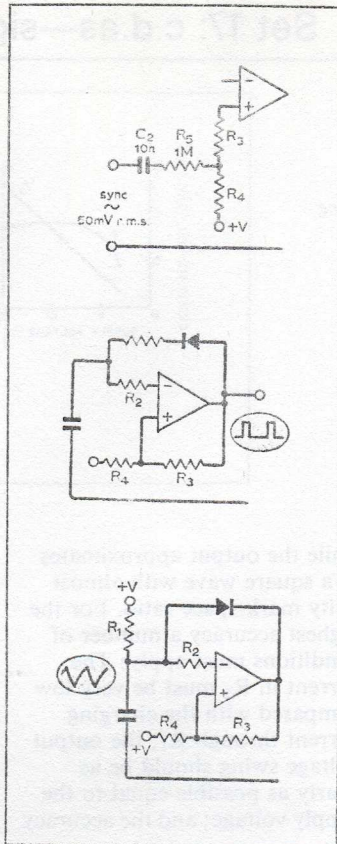
R_1: This sets oscillator frequency together with C. Too low a value loads the output. too low is loaded by R_2. Typically 4.7k to 100kΩ.

C: Max frequency of oscillation $\approx$ 20kHz corresponding to $C = 470pF$ with $R_1 = 15k\Omega$. Capacitor voltage always positive allowing use of electrolytic to give low

frequencies.

R_L: Maximum output current $\approx$ 10mA giving minimum $R_L = 1k\Omega$ at $V_s = 10V$. Generally keep $R_L > 2.2k\Omega$ to allow output to swing close to supply.

Circuit modifications

● As with other astable multivibrators, this oscillator can be synchronized to an external waveform. Because the Schmitt action is achieved using high value resistors, the synchronizing input may also have a high input impedance, while locking can be achieved with 100mV. Locking to a sub-harmonic of an incoming signal is also possible, though for frequency division ratios in excess of 5:1 carry the risk of locking to the wrong sub-harmonic. (Top circuit.)

● Where relatively narrow pulses are required, the charge and discharge time constants should be as widely different as possible. The charging action is via R_1, a low resistance with a small current diverted into

R_2. When the output is low the diode is non-conducting, and the small current in R_2 gives a long discharge time, i.e. a long space. (Middle circuit.)

● Other forms of multivibrator may require more than one amplifier but the bottom circuit has some similarity of behaviour to the programmable uni-junction. The capacitor charges through R_1 until the upper threshold is reached. The output swings towards zero rapidly discharging the capacitor. The long mark has its duration controlled by the direct voltage applied to R_1 (+V may be replaced by an external control voltage giving a voltage controlled oscillator). The space is of short duration because of the relatively large discharge current.

Cross references
Set 3, cards 2, 4, 6 & 8.
Set 8, all cards.
Set 10, card 2.
Set 17, cards 3, 8 & 10.

(provided leakage resistance is 1MΩ) and with R_1 at 1MΩ time-delays of minutes are possible.

C_2: Used to differentiate input signal to provide short-duration positive transients. 47p to 220pF for first input pulses; increase for slower input rise times.

R_1: Ratio R_1/R_2 sets fraction of supply voltage across C_1 at which the pulse period is completed. Typically $R_1/R_2 = 0.1$ to 0.3. If ratio is too low the period lengthens considerably but is ill-defined.

R_2: Current in R_2 should not fall below $1\mu A$ if timing is to be controlled by RC values.

R_3: With $R_3 = R_1$ the smaller current in R_2 is sufficient to keep the output high in the quiescent state.

D_1: Any general-purpose silicon diode.

Circuit modifications

● Positive-going output pulses can be obtained with a similar circuit if the permanent bias is applied to the inverting input,
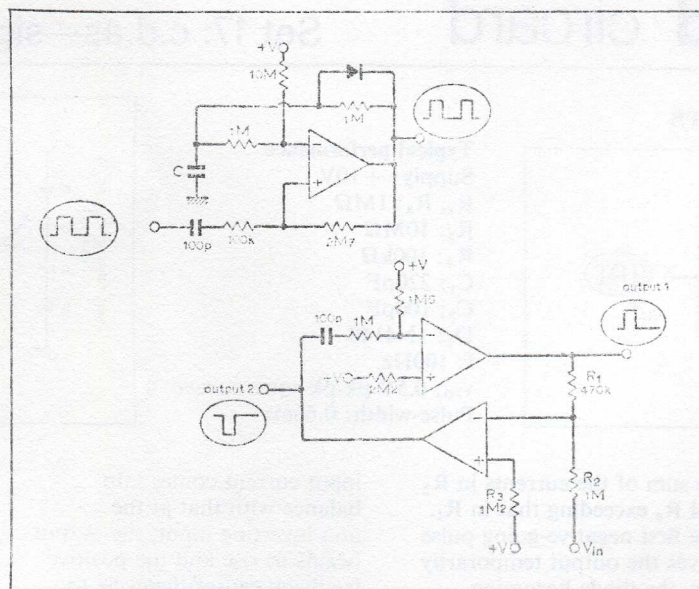
the direction of the diode reversed and a changing path provided in parallel with the diode. The quiescent condition has the output low with the diode conducting and significant current only in the 10MΩ resistor. A positive-going input transition

drives the input high, which state is held until the capacitor charges sufficiently to allow the current in the inverting input to exceed that in the non-inverting input. A major advantage of an amplifier having both inputs accessible is that the signal pulses can be

transferred to the other input. In this version, the output pulses would then be triggered by negative rather than positive transitions, while in the previous case which required negative transitions the response would then be to positive edges.

● Two-amplifier monostable circuits can have two opposite polarity outputs and allows separation of the triggering timing and output sections more readily. The circuit shown is equivalent to a Schmitt trigger followed by a monostable although the functions are combined in a single circuit. Out$_1$ is normally low contributing no current to the inverting input of the lower amplifier. Hence Out$_2$ is only driven low when V_{in} reaches $\approx 0.8V_{in}$. Provided the input falls below this level prior to the end of the pulse then generated, the circuit is suitable for resetting an oscillator when its ramp output exceeds a given d.c. level.

Flip-flops
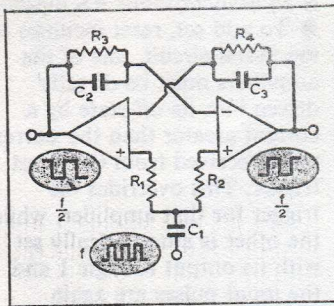
Typical performance
IC: $\frac{1}{2}$LM3900
Supply: +10V
R_1, R_2: 100kΩ
R_3, R_4: 1MΩ
C_1: 100pF
C_2, C_3: 56pF
v_o: 9V pk-pk
Max input frequency for
satisfactory toggle action: 10kHz
Min. input amplitude: 4V pk-pk

Circuit description

The circuit has strong affinities with standard two transistor flip-flop and could be triggered at either of the inverting inputs via diodes to provide a set/reset function. Non-inverting inputs provide the additional facility of triggering the flip-flop to provide a ÷2 action. Equal currents are fed into the non-inverting inputs on receipt

of a positive-going edge but that amplifier whose output is already high because its inverting input receives no current will be initially unaffected. The other amplifier receives a short-duration current flow at its non-inverting input that exceeds that at its inverting input, and its output begins its positive-going transition. The speed-up

capacitor couples this to the inverting input of the other amplifier and the positive feedback around the loop causes the transition to complete itself. Thus each output changes state in opposite directions on the receipt of each positive-going input transition. Two such transitions are required to complete each cycle of the output, and the

output waveforms are complementary square waves at half the frequency of the input.

Such circuits may be readily cascaded to produce lower frequency to develop simple counters. Their low speed offers no competition to c.m.o.s., t.t.l. etc. but the ease with which they can be combined with other analogue/digital functions
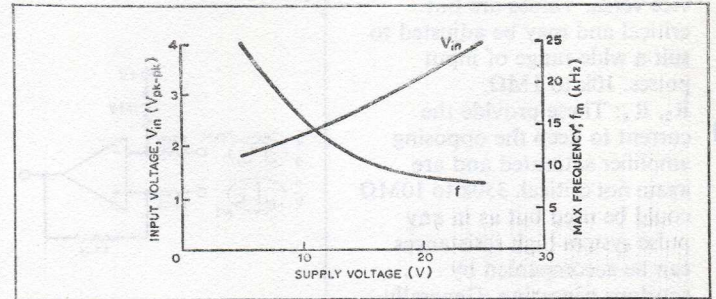
Staircase generators
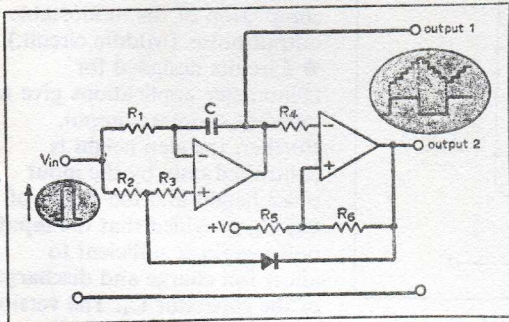
Typical performance
Supply: 7.5V
R_1, R_4: 1MΩ
R_2: 120kΩ
R_3: 330kΩ
R_5: 10MΩ
R_6: 1.8MΩ
C: 1μF
D_1: 1N914

Input: pulse train +12V peak
Mark/space ratio: 2:1
Repetition rate: 30kHz
Output 1: staircase waveform
  3.6V pk-pk, frequency 800Hz
Output 2: 6.8V pk-pk, frequency
  800Hz

Circuit description

A staircase waveform can be generated by feeding pulses of current to a capacitor between pulses. The resulting circuits are closely related to those used in frequency meters such as the diode-pump circuit and its variants. One version as shown feeds the pulses to either the inverting or the non-inverting input of the first amplifier depending on the state of the

output of the second. Consider output 2 positive. The diode is reverse biased and with $(R_2 + R_3) = R_1/2$ the net positive current into amplifier 1 is positive. During each positive pulse output 1 ramps positively, remaining relatively constant between pulses. The smaller the mark-space ratio the more nearly the output waveform approaches a staircase waveform, with the rising steps

occupying a small proportion of the time. At some positive voltage set by the resistors R_4, R_5, R_6 the Schmitt trigger operates, its output switching to near ground level. The diode becomes forward-biased diverting all subsequent positive pulses from the non-inverting input. The net negative input current via R_1 produces a staircase waveform in the negative direction until the

lower threshold voltage of the Schmitt is reached and the cycle recommences. In essence the circuit is that of a square-triangle generator in which the direct control voltage is replaced by a succession of positive pulses giving a stepped characteristic to the triangular wave. The mean input voltage determines the mean charging current and the average slope of the ramp. If the frequency of the input signal is varied while maintaining a constant pulse height and constant mark-space ratio, then the basic repetition rate of the output remains unchanged. (It is composed of a number of steps dependent on the ratio of input frequency/output frequency.) Varying the pulse height, the mark-space ratio or Schmitt trigger points varies the output frequency.

Component changes
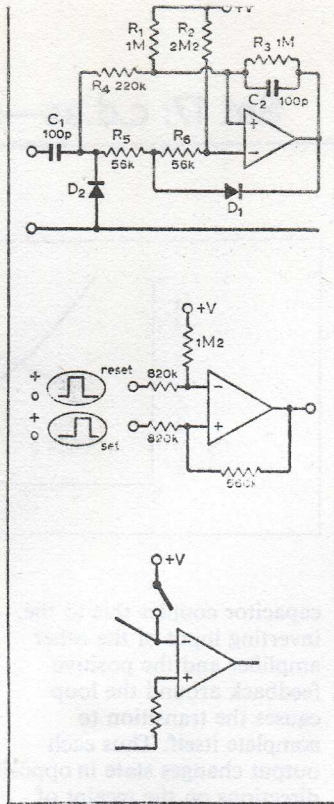R_4, R_5, R_6: The magnitudes of

Component variations

+V: Standard supply range +4 to 36V. Samples may operate down to <2V.

R_1, R_2: Sensitivity can be controlled by varying R_1, R_2 for fixed values of R_3, R_4 and vice versa. Values are not critical and may be adjusted to suit a wide range of input pulses. 10k to 1MΩ.

R_3, R_4: These provide the current to keep the opposing amplifier saturated and are again not critical. 330k to 10MΩ could be used but as in any pulse system high resistances can be accompanied by spurious triggering. Generally the lower resistances are required at low supply voltages.

C_2, C_3: Speed-up capacitors ensure positive transitions but the maximum speed is limited by amplifier slew-rate.

C_1: Not critical. 47p to 470pF.

Circuit modifications

● Using a single amplifier, one

these resistors are not critical and they may range from 10k to 10MΩ. Design procedure for the trigger levels is given on Schmitts and comparators card. Hysteresis $\approx +VR_6/R_4$.

R_1, R_2, R_3: For comparable positive and negative slopes, $R_2 + R_3 = R_1/2$. Ratio $R_2:R_3$ is not critical but neither should be < $R_1/10$. R_1: 10k to 1MΩ.

C: Controls the basic repetition rate of the output for given input waveform. 220p to 10μF. Output frequency can be very much less than input frequency with division ratios in excess of 100.

Circuit modifications

⊙ When the input is at zero, current flow to ground through R_1 allows the stored voltage on C to vary. Inserting a diode prevents this at the expense of a reduced effective pulse height. Most other v.c.o. circuits can be adapted to perform this function. Replacing the diode by a transistor and controlling the pulses to the inverting input leaves the phasing correct. (Top.)

channel the incoming pulses to the two inputs alternately, with overall positive feedback to latch the circuit. The quiescent state with the output high is sustained because both R_2 and R_3 contribute current to the non-inverting input, exceeding that in R_1. When the output goes low it remains there because now the non-inverting input receives current only via R_2, leaving the current through R_3 into the inverting input to dominate. In the latter state D_1 prevents any input positive-going pulse from reaching the inverting input and the circuit is triggered via R_4 into the high state. The succeeding positive pulse produces approximately twice the current through R_5, R_6 as through R_4 (D_1 is reverse biased), the output going low. C_2 is the speed-up capacitor and D_2 absorbs the negative transitions.

● Careful choice of the positive feedback in this circuit (middle) provides sufficient hysteresis to

● To obtain a staircase waveform followed by a sharp transition, the Schmitt may be followed by a monostable circuit that provides a pulse of current to discharge the capacitor rapidly. Input pulses are fed to a single input as shown, and again alternative

given state after an input pulse has returned to zero. Any further pulses on that input have no effect, and it requires a similar pulse on the other input to reverse the output. The input which drives the output to logic 1 is the set input, the other the reset and the circuit is an asynchronous RS flip-flop.

● To add set, reset facilities to the initial circuit, one of the amplifiers must be directly driven into its off-state by a current greater than the current pulse received from the input trigger. This overrides the trigger for that amplifier, while the other is automatically set with its output to logic 1 and the input pulses are again ineffective. A transistor may replace the switch. Shown in the bottom circuit.
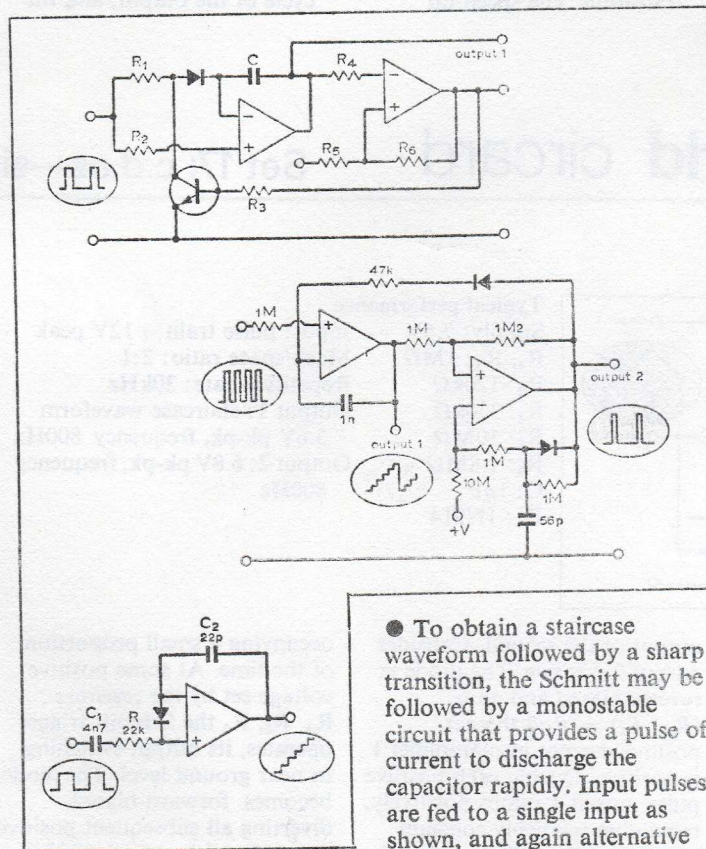
Cross references
Set 2, cards 3, 8 & 9.
Set 14, card 1.
Set 17, cards 7 & 8.

arrangements are possible by phasing input/feedback appropriately. Switching and timing actions can be combined in the single monostable shown, where the positive output pulse is initiated at a particular input amplitude, the timing remaining correct if the input voltage to the monostable falls below this firing level before the completion of the monostable output pulse. (Middle circuit.)

● Circuits designed for tachometer applications give an inherent staircase output. Further, the step height is controlled only by the input pulse height and the values of C_1, C_2, provided that the input pulse width is sufficient to allow full charge and discharge of the capacitor C_1. The version shown has a frequency doubling action with the positive input transitions being fed to the non-inverting inputs and the negative transitions to the inverting inputs.

Cross references
Set 3, cards 3 & 7.