ELECTRONICS & WIRELESS WORLD

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Optical broadcast telecomms

Working with DSP

Frequency counter design

Slow rams – cache them if you can

Mass storage developments

Block encryption techniques

Economics of equipment hire

Paradoxical gyroscope

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Big changes, little changes

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REED BUSINESS PUBLISHING

The electronics industry has reached its highest ever rate of change. Not just in the limited sense of a higher technology but across a much broader front where the very activity of the industry at large is changing dramatically.

Consider ASICs. Once the preserve of Hewlett-Packard, IBM and companies of similar economic muscle, designer chips can find a place in your product, or your competitor's, for under £1000. These are true custom metallised gate array products, not just a programmable standard logic array.

Consider also the engineer who designed it. He (and, regrettably, it would almost certainly have been a "he") would have used a PC type desktop computer to run design and logic translation software, the same £1000 machine which could also be used for secretarial and accountancy work. A couple of years ago the glue logic which this sort of chip replaces would have been designed using pencil and paper, a soldering iron and a stack of 74LS.

These differences are also reflected in system engineering. Designers hardly have to consider bus timing, compatibility in logic levels and component level problems in general. One simply thumbs through the catalogue for the board level product which performs the desired function. Minimal knowledge of electronics needed here. Much more useful to possess a working knowledge of the software sitting on that PC or VME board controller. Not electronics. Not wrong. But different.

If it causes confusion to those working in the industry, it also creates an identity crisis for magazines wanting to write about electronics. Should a magazine cover the software aspects of design at the expense of the hardware, attempt to divorce them or simply acknowledge that they are two sides of the same coin?

Obviously the last option makes sense and this is the way that we at EWW intend to deal with this new-born dichotomy. We intend to reflect the change from component level to system level design.

Some things won't change. The perennial interest in and perennial need for analogue design. No matter how many board level products in a given system, there will always be some part of it which makes contact with the real world. And there you will find an analogue engineer. The same thing goes for the wonderful art of RF design. EWW has always understood this area and I, as the new editor, don't intend to let it go.

I would also like to retain our role as a forum for abstract concepts but, having studied recent exchanges in our pages, now feel that the debate must be moved on. We started in the December issue reporting events apparently occurring beyond the speed of light. We continue this month with a note on the strange behaviour of gyros.

And me? I'm aged 39 but remember Lisle St as an Aladdin's cave of ex government wonder. I built my first television using a green phosphor VCR97 ex WW2 indicator tube. I have worked in the electronics industry on the design side and, rather later, looking in from outside as the components editor of Electronics Weekly. I still own a soldering iron but lately have learned to speak several computer languages.

In common with most of the people who will be reading this, I too have always been an EWW reader. I revere its traditions but appreciate the importance of looking to the future. I do hope that you will join me.

Frank Ogden, Editor

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High-resolution frequency counter

Using a microprocessor enables the designer to provide better resolution at low frequencies and to add such useful features as sum, difference and ratio measurement.

STEPHEN THEOBALD

The circuit presented here was designed to overcome some of the limitations of conventional instruments using decimal dividing chains. Such instruments are generally characterized by poor resolution at low frequencies unless very long measuring periods are resorted to, and are rather inflexible.

Several specialized and, in most cases, highly-priced integrated circuits are available, offering nearly all the hardware necessary for building a complete counter, but these suffer from the same disadvantages. The basic design has for a long time now needed a little freshening up.

In line with modern practice, a powerful eight-bit microprocessor is at the heart of the circuit, resulting in fairly simple supporting hardware composed of a small number of inexpensive and readily-available 74-series devices. The computational abilities of the microprocessor make it possible to produce a very versatile instrument, capable of much more than just frequency measurement, but the extra facilities add almost nothing to the cost. The fact that the instrument is under program control also means that it can, if necessary, be tailored to particular applications.

The most important extras that the design offers are the sum, difference and ratio functions. The first two of these allow intermediate frequencies to be taken into account in radio receivers, regardless of whether the signal picked up lies above or below that of the local oscillator. It is only necessary to store the intermediate frequency in the memory, and the frequency to which the receiver is tuned can be read out directly by measuring the local oscillator frequency and applying the appropriate function. Again, the difference mode makes it an easy matter to determine drift in an oscillator. Simply make a measurement of the frequency, store the value and then switch over to the difference mode. Deviation will be displayed automatically. The last of these functions, the ratio of the input to some previously stored frequency, proves useful when working on frequency synthesis.

SPECIFICATION

Overall frequency range: 25μHz to 1GHz in three ranges, autoranging within each range.

Range function			Min.resolution	Accuracy
VLF[1]	freq.	25μHz–3Hz	1 part in 10^4	± 1 digit
	period	40ks–330ms	1 part in 10^5	± 1 digit
MF	freq	0.9Hz–>30MHz	1 part in 10^4	± 1 digit
	period	1.1s–<33ns	1 part in 10^4	± 1 digit
HF	freq.	<25MHz–1GHz	4 parts in 10^6	± 1 digit
	period	>40ns–1ns	1 part in 10^5	± 1 digit
Pulse		200ns–1s	200ns	+400ns, −0
		1s–50ks	1 part in 10^6	± 1 digit
Event[2]		0–9 999 999	–	–
Clock		0–9999.999s	1ms	±1ms
Freq. ratio[3]		10^{-9}–10^{+9}	1 part in 10^4	± 1 digit

Note 1. This range extends to 31Hz (period to 31ms), with lower resolution.
Note 2. The maximum pulse repetition rate should not exceed 10kHz.
Note 3. Ratio, sum and difference modes are not available on vlf ranges.

Input	Freq.range	Sensitivity	Input resistance	Max. input
VLF/MF amp.	0–40MHz	30mV pk-pk	1MΩ//25 pF	50V pk-pk
HF prescaler	25MHz–1GHz	10mV rms	50Ω approx.	3V pk-pk

MEASURING LOW FREQUENCIES

Let us first consider how to measure low frequencies very accurately, while keeping short the time required to do so. For frequencies not less than about 1Hz, we can use the hardware arrangement shown in **Fig.1**. The controller, which is the cpu and an input port, can enable, read, and reset the counter, and must also be able to measure elapsed time in short units of time, dt seconds.

Initially the counter is reset and then enabled (**Fig.2**). The controller synchronizes the start of the measuring period with a positive edge at the clock input, which it detects by sensing that the lsb of the counter changes from 0 to 1. Incoming pulses are now counted for a fixed length of time, Xdt. At this point the controller again notes the state of the lsb and continues to measure time for some variable period, xdt, until the next positive edge at the clock input causes the lsb to change state once more. Detecting this condition, the controller now disables the counter via the And gate and reads the count, which we shall denote as N+1. (Remember that the counter goes to 1 just before the measuring cycle starts.) N complete cycles of the input have now been received in a period of (X+x)dt seconds, and the frequency of the input is simply calculated as $f=N/(X+x)dt$ Hz.

The degree of resolution obtainable depends on X, while the minimum duration of the measuring period to achieve a given resolution rests on the values of both X and dt. Worst case resolution occurs when the variable x assumes its minimum value of 1; that is, when $f = N/(X+1)dt$. The slightly lower frequency, f′, for which x becomes 2, is obviously $f' = N/(X+2)dt$ Hz. The difference between the two frequencies is the smallest change that the system can detect, and is given by

$$df=f-f'=N/(X+1)dt-N/(X+2)dt$$
$$=f/(X+2)\rightarrow f/X, X\gg 2$$

Resolution, which we define as df/f, is thus 1/X; and the shortest period necessary to achieve this value is Xdt. The design being presented here has values of X and dt of 10^5 and 10^{-5} respectively, permitting a frequency of 9.9998Hz to be distinguished from 9.9999Hz.

At any frequency, the maximum time which can elapse before a result can be calculated is given by Xdt+2/f seconds, i.e. 3 seconds at 1Hz, while the minimum time is Xdt+1/f seconds. The exact time depends on how long the system must wait for synchronization to occur. Although not shown here, a similar analysis for f″, the slightly higher frequency which can just be distinguished from f, yields the same results.

Synchronization is necessary up to at least 10kHz to ensure a minimum of five significant digits in the result. Above this point the system can revert to the more normal technique of just counting the input pulses, not bothering to synchronize to the input, provided that counting is performed for at least one second. This design continues to synchronize up to 25kHz because it was slightly easier to arrange it that way in the program.

The vlf range differs from the mf range in that the counter is not used. Instead, the controller reads the input directly and measures over just a single cycle of the input. This has the advantage that the start of the measuring period may be synchronized with either the positive or negative edge of the input, whichever occurs first, thus saving time and wear-and-tear on the operator when the input is very low in frequency. By maintaining dt at 10μs it is possible to attain five-figure precision up to $\sqrt{10}$Hz. Since it was desired that this range should extend to a somewhat higher frequency, a switch from five-figure to four-figure readout occurs as f exceeds the 3Hz mark. A similar reduction to three-figure accuracy would be called for at frequencies greater than about 31Hz, so this figure was chosen as the upper limit of the vlf range. Aliasing occurs beyond this point, giving a readout of f/(INT(f/31.35)+1)Hz.

CIRCUIT ARRANGEMENT

Hardware (**Fig. 3**) is fairly straightforward except that the three highest address bus lines are used for control purposes. The range and function switches allow the cpu to determine which programs to call for a particular function as well as which input amplifier connection to select. The chosen input is applied to the input port either directly, for vlf measurements, or via the 12-bit binary counter. The pulse processing circuit, if selected, gates the clock oscillator with the input signal and sends trains of 5MHz pulses to the counter.

At the end of each measuring period, the processor disables the input and reads the input port. It then selects the 5MHz clock as the input to the counter and enables its own interrupt input, which then receives short pulses from the monostable each time Q_{11}, the counter's msb, changes from 0 to 1. These interrupts drive the multiplexing of the display while the cpu calculates the results. Thus the display is multiplexed at a rate in excess of 1.2kHz. Once the final result becomes available, the required display is stored in ram and the interrupt is disabled. The next measurement cycle is now undertaken while the cpu times the display drive internally, sending out the digits stored in memory to the output ports.

It is obvious that a 12-bit binary counter is inadequate for measuring signals higher than about 4kHz on its own, so the microprocessor detects overflow on Q_{11} by sampling this line via the port sufficiently often to ensure that the count is accurate, even at frequencies as high as 50MHz. In this way the counting chain is extended within the cpu.

In the main digital circuitry (**Fig 4, 5**), note that the 74150, which is a 16-line multiplexer used as an input port, is neither tri-state nor open-collector at its output. It is therefore connected to the data bus through a diode and pull-up resistor instead. The ram chosen for the design was the 2K 6116-LP3 since this is cheap and uses little power.

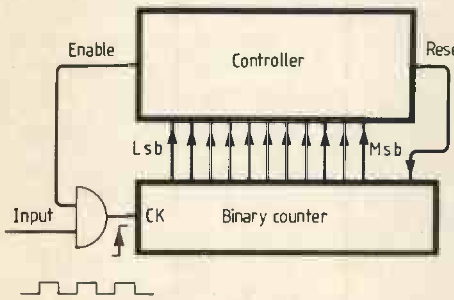


Fig.1. Basic hardware arrangement for measuring low frequencies.

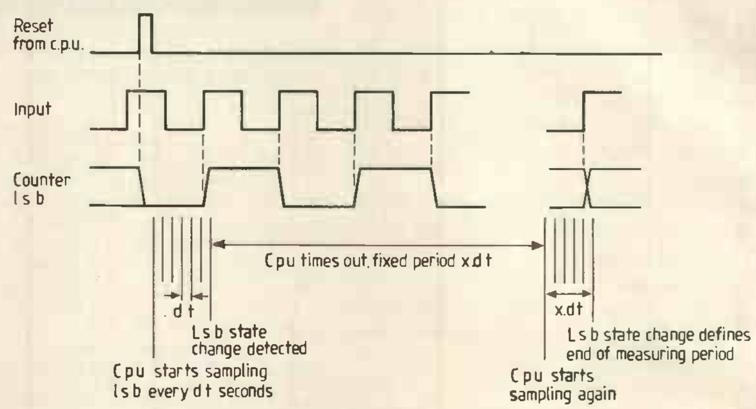


Fig.2. Sequence of events for measuring low frequencies.

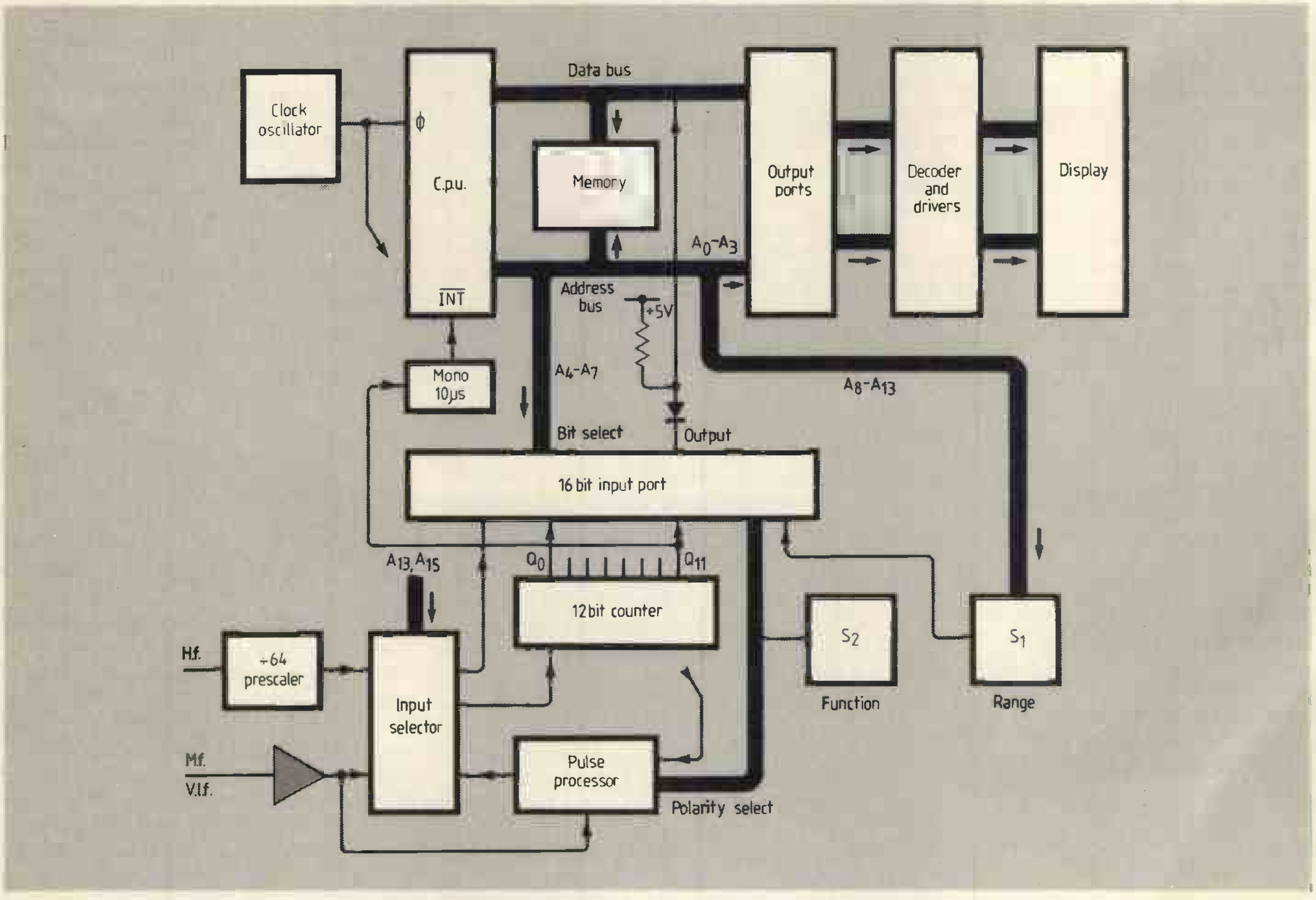


Fig.3. Block diagram of the high-resolution counter. The processor is a Z80.

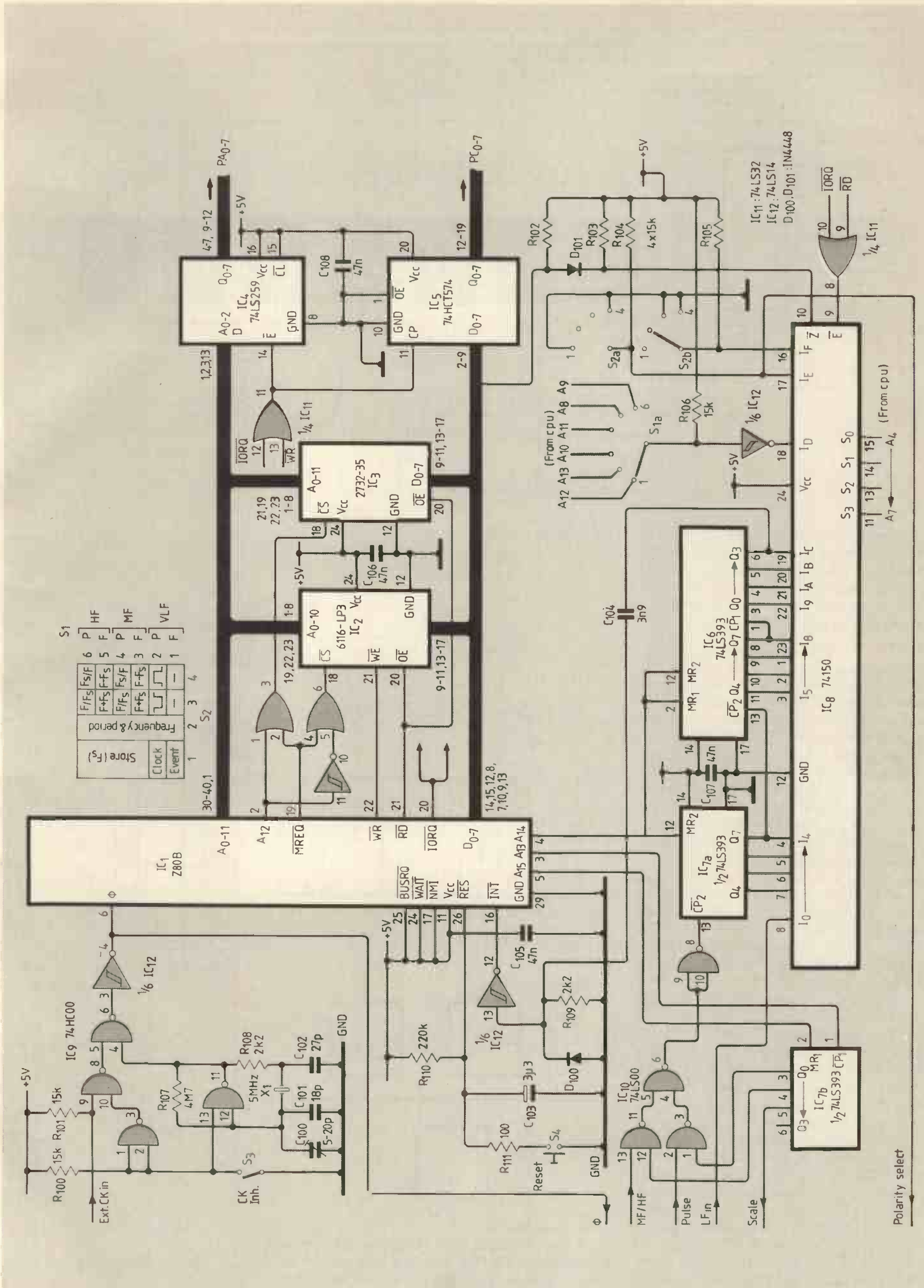


Fig.4. Digital section of the counter. A programmed eprom is available from the author – details at the end of this article.

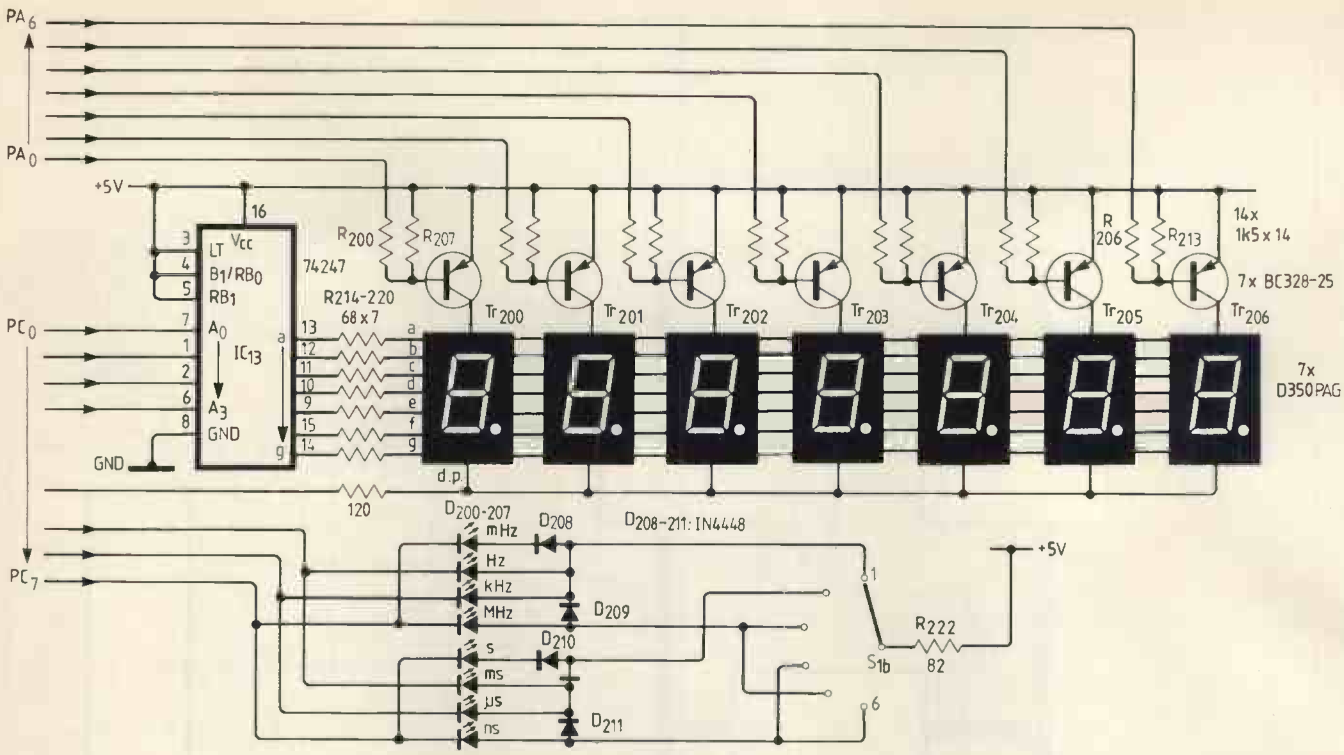


Fig.5. Display section.

However, the program requires no more than 128 bytes of ram and other, smaller memories may be used provided that cpu address lines A_0-A_5 plus A_8 are connected. Line A_8 became necessary as a result of a programming short-cut.

VLF/MF INPUT

Input amplifiers, selection network and pulse processor are all shown in **Fig. 6.** The vlf/mf amplifier has a frequency response extending from 0Hz to about 40MHz. The capacitor-resistor network feeding Tr_1 provides a high-impedance input for signals less than about 1V pk-pk of 1MΩ//20pF. Larger inputs are clipped by diodes D_1 and D_2, whereupon the input looks like a 1k resistor in series with 10pF. Relay Rl_a is used to select either ac or dc coupling. Potentiometer P_1 and the associated switched resistor chain allow an offset voltage to be applied to the gate of Tr_1 to balance out any direct voltage applied to the input when this is dc coupled. This arrangement also serves as a simple trigger control with capacitively coupled signals. The average value of low-level, narrow duty-cycle inputs may be such as to prevent reliable counting unless a small offset is superimposed. Signals are taken from the potential divider at the source of Tr_1 at about ground level and applied to one input of the 733 wideband video amplifier. The other input is connected to a similar tapping on the source of Tr_2. This transistor is only used to compensate for drift in the working point of Tr_1 with temperature variations. The 733 must not be overloaded too severely at high frequencies since its recovery time is then so great that it canot follow the input. Relay Rl_b is used to switch extra feedback into the circuit if necessary, to overcome this problem. The output of the 733 is differential and at ttl levels, so one of these outputs is fed to a Schmitt trigger to square up the signal before going further to the and routing network.

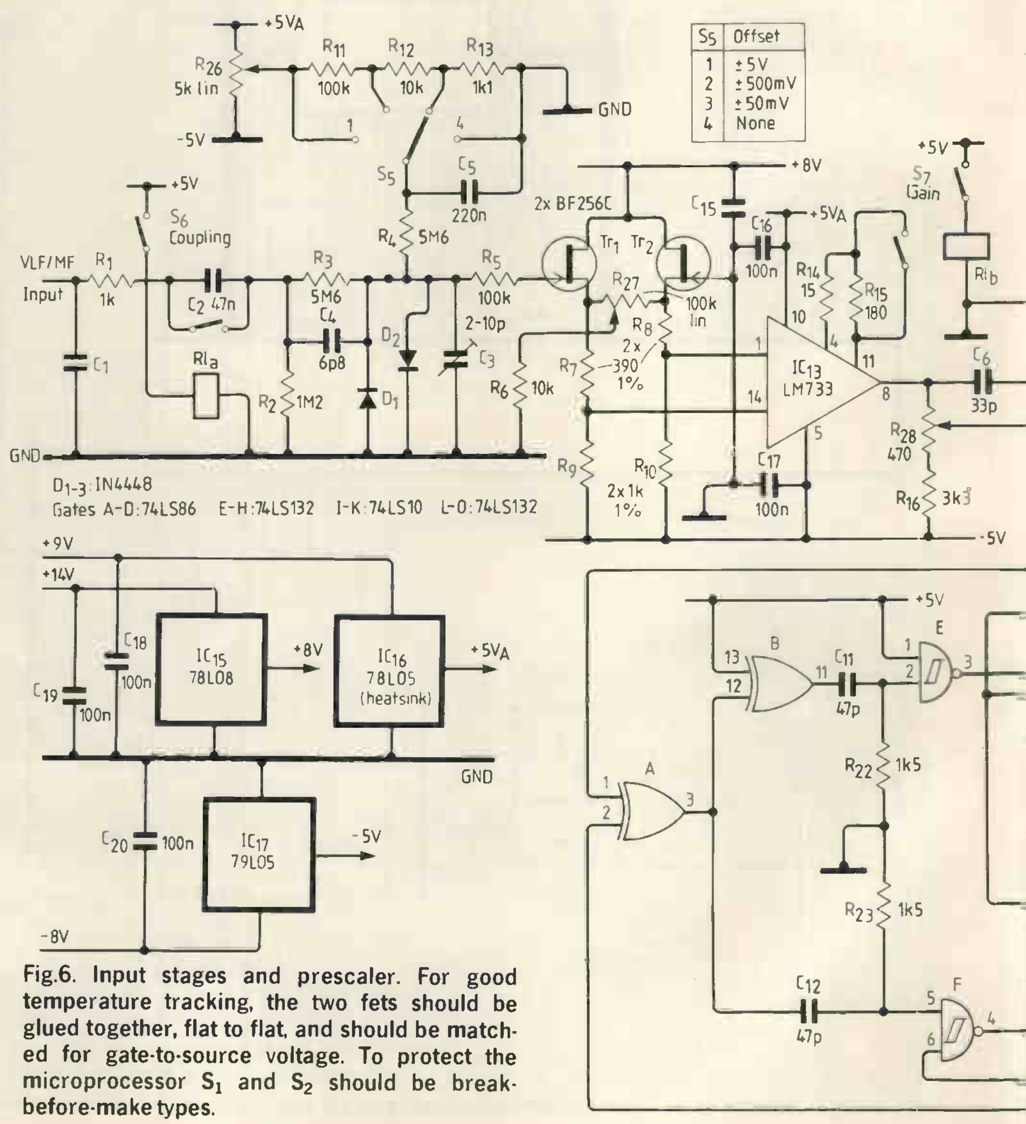
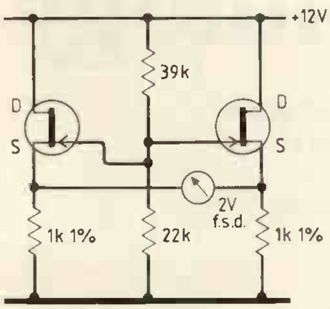
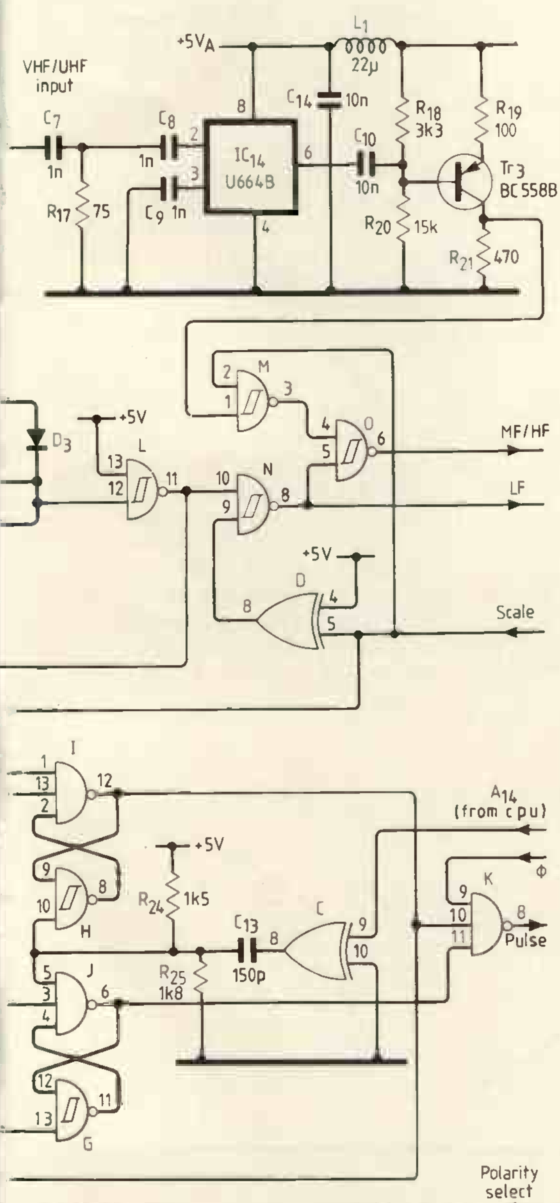


Fig.6. Input stages and prescaler. For good temperature tracking, the two fets should be glued together, flat to flat, and should be matched for gate-to-source voltage. To protect the microprocessor S_1 and S_2 should be break-before-make types.



Fets for the input amplifier should have well-matched gate-to-source voltages at a drain current of 5mA. Of eight devices tested by the author using the circuit above, two pairs were found to have gate-to-source voltages within 20mV of one another.

The input amplifier is best built in one long run down the printed circuit board to ensure good isolation between output and input.



The pulse processor receives this signal as its input and operates as follows. The cpu selects the pulse function by making $\mathrm{IC}_{7b}\ \mathrm{Q}_0$ and Q_2 high. It resets the two bistables formed from gates G, H, I, and J by pulsing A_{14} high for a moment, the falling edge providing the reset. The output of gate I is then low, while that of J is high. Output I blocks gates F and K, thereby hindering the clock from triggering the counter. Let us now assume that that the polarity select line to gate A is high. Gates A and B then work as two inverters and when the positive edge of an input pulse occurs at gate A it is passed unchanged to gate E, which generates a short pulse to alter the state of the H-I bistable, enabling K and allowing the clock oscillator through to the counter. This condition is maintained until the negative edge of the input pulse arrives, is inverted by A, and with the help of F, which was enabled when the H-I bistable flipped over, changes the state of the G-J latch so that the gate K is once more disabled, cutting off the 5MHz pulse train to the counter. The cpu senses this behaviour and calculates the pulse duration by multiplying the count by 200ns. Inputs of the opposite polarity are measured if the polarity select line to gate A is low, since this will then be non-inverting.

HF INPUT

The hf input is applied straight to the input of the U664B prescaler. This is a moderately-priced Telefunken device which has excellent sensitivity all the way up through the vhf and uhf bands to 1GHz. Take care not to confuse this with its stable-mate the U664BS, which is designed for self-oscillation in the absence of an input signal. The outputs of these devices are at ecl levels and so Tr_3 is used to translate them to ttl levels.

The cpu selects the source for the counter via the nand routing network, this being steered by Q_0, Q_1, and Q_2 of IC_{7b}, which is itself controlled by address lines A_{13} and A_{15}. The amplifiers are supplied from their own voltage regulators to prevent noise feed-through from the main digital circuitry causing problems.

THE PROGRAM

The program is very nearly 4K in length. In view of the very wide range of high-precision numbers that the arithmetical routines must handle, floating-point format was decided upon for internal representation. These have a 24-bit mantissa and an eight-bit exponent with no offset. Because of the small number of operations to be performed to calculate any result, this format allows working to an accuracy of seven significant digits, which is just about adequate. All calculations are properly rounded up or down to maintain precision.

For the sum and difference modes, the program slips into bcd arithmetic. This not only demands much less programming effort, it also safeguards against showing these results with spurious accuracy. Suppose that the signal being measured is 10MHz and that the stored frequency is 9.99998MHz. It is no good showing the difference between them as 20.000Hz to five not-very-significant-figures. Unlike floating-point arithmetic, bcd arithmetic works with a fixed decimal point, its position being determined by whichever of the two frequencies is the larger, and the zeroes which would then appear in the above example are displayed in the readout, which becomes 0.00002MHz.

To prevent the program getting stuck while trying to synchronize to an input which is suddenly removed half-way through a measuring cycle, a time-out limit has been included to abort the measurement after about one second.

DISPLAY

Great care has been taken to ensure smooth multiplexing of the display. The microprocessor is responsible for doing this whilst attending to a great many other chores in each cycle. Even quite small fluctuations in the rate of multiplexing cause surprisingly large amounts of flicker in the display, but the present version of the program has overcome this problem entirely.

Display format has been made as logical as possible within the limitations imposed by the 74247 decoder. When switched to a non-existent function, the program produces a display with only the decimal points lit. This is also the case with vlf and pulse functions until the first edge to which the program triggers occurs, whereupon zeroes are displayed in the frequency and pulse modes, and zeroes with decimal points in the period mode. This remains until the first meaningful result is obtained. Much the same system is used when overflow occurs in the ratio mode, which results if the divisor is zero. Ratios are shown as five-figure numbers followed by an exponent, the exponent being expressed in the multiple-of-three convention. An annoying shortcoming of the 74247 is its inability to show a minus sign and so, for want of better, the last decimal point of the readout has been pressed into service. A reading of 12.345 6. is therefore to be interpreted as meaning 12.345×10^{-6}. Use has been made of the same device in the frequency difference mode when the stored value is greater than the input frequency.

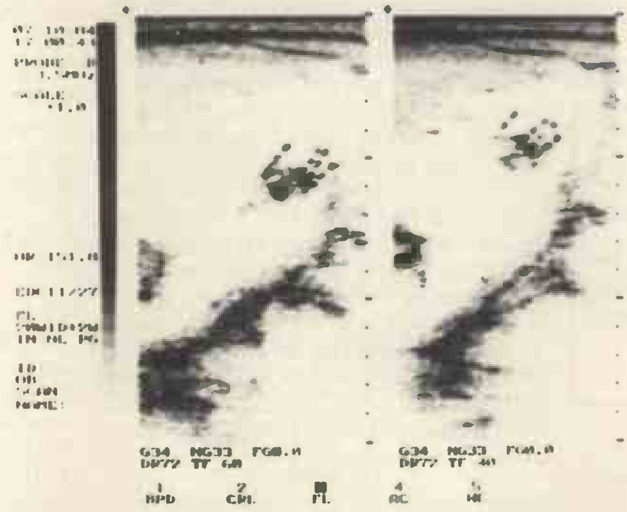
One point to note is that the clock function only measures time while the gate of Tr_1 is held higher than that of Tr_2 (use R_{26} to apply a bias if wished), and that the clock works cumulatively. It may be zeroed by resetting the instrument or choosing another function.

● A further article describing a method of interfacing the instrument with PCs is in preparation.

Software in eprom for this design is available from the author; readers should ask their bank to raise a cheque for 150 Danish kroner (about £13). If there is sufficient interest, he will also offer a set of three printed circuit boards. Enquiries can be forwarded to him via the editorial office: mark your covering envelope "Frequency counter".

Radial array technology

Development of medical ultrasonic scanning has been rapid but, according to General Electric, it has actually been slowed down by a more agressive market. This article charts technological progress in ultrasonic scanning and explains why GE considers that radial scanning is the way forward.



With image processing and better mechanical systems, interpreting an ultrasound image no longer needs a trained eye.

For the past two decades, clinical applications of ultrasound have expanded as a result of technological improvements in the instrumentation. Technological development activity has always been directed towards improving image quality and reliability. Because of competitiveness in the ultrasound market, and falling profits, development activities among the established market leaders have diminished.

Each company, in an effort to protect its own investment, has promoted its own product with minor modifications to achieve near-term improvements and product acceptance. In recent years, no company has introduced a technology that not only satisfies present clinical needs but will withstand the test of early obsolescence.

Over the past twenty years, each new ultrasound scanning technique has been accepted as the clinical standard for a period of time, but has gradually disappeared and been replaced by a new technique, **Fig. 1**.

Articulated-arm scanners produced the first two-dimensional clinical images on a large scale. For many years the articulated arm was considered the only clinically acceptable instrument. Its acceptance peaked in about 1979. But during the era of the static scanner two important developments occurred.

In 1973, the analogue-scan converter was introduced, replacing bistable images with grey scale. A more reliable device – the digital-scan converter – replaced the analogue scan converter in 1977. Solid-state computer technology then introduced the microprocessor into ultrasound systems. The microprocessor permitted more complex systems with more complex controls and functions; and significant decreases in the cost of memory, particularly dynamic ram, encouraged a variety of development efforts in the imaging field. The first commercial real-time linear array was introduced in 1974.

Compared to the articulated-arm scanner, this new technology was relatively inexpensive and for the first time in clinical ultrasound, dynamic evaluation was possible with clinically acceptable images.

Real-time imaging rapidly expanded its clinical use during the late 1970s with the development of sector scanning, using either the mechanical sector scanner or the phased array.

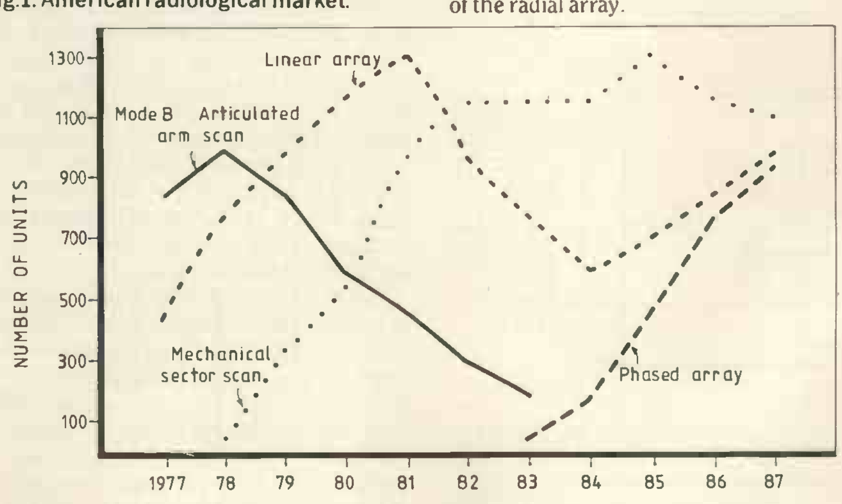
Radiologists preferred the image quality of mechanical sector scanners to that achievable with the early phased arrays, since the mechanical sector scanner – although limited in many respects including lack of dynamic focus – offered the contrast resolution and dynamic range needed to detect subtle changes in parenchymal (glands as opposed to flesh, etc.) structure. On the other hand, cardiologists were less concerned with contrast resolution but more interested in the high frame rate achievable with the phased array and its ability to produce cardiac images intercostally (between the ribs) with a small transducer footprint.

Linear arrays remained important as the standard low-cost imaging device for obstetrical use. Very few experts would have expected the linear array to re-emerge as the technological leader in image quality (the second peak on the linear array curve of Fig. 1). However, it should have been abundantly clear that the linear array with good image processing and adherence to fundamental engineering principles could achieve a leadership position in image quality and contrast resolution that would eventually change the radiologist's view of the choice instrument.

Computed sonography was introduced in 1983 using a linear-array transducer. The technique demonstrated to the radiologist the image improvements that were possible using a large-aperture system. The linear array had initially not been accepted by the radiologist because its footprint seriously limited its clinical applications.

Despite its inconveniences and limitations, the high quality linear array was eventually accepted as the standard of image quality by the radiologist. But the radiologist still needed other instruments to perform clinical examinations where a small footprint was necessary. Computed sonography demonstrated what could be accomplished with the large aperture, but there was a void that could only be filled by the development of the radial array.

Fig.1. American radiological market.



WHY THE RADIAL ARRAY?

The radial array, as its name implies, is composed of an array of transducer elements serially arranged along a predefined arc with a specific radius of curvature. Thus, it can incorporate the attractive features of the linear array without sacrificing access or beam steering. The highly curved radial array has the same geometry as the mechanical-sector scanner, but has no moving parts or liquid path.

For large field-of-view imaging, such as that required to look at unborn babies, the moderately curved array is the optimal choice. Different radii of curvature in combination with transducer arrays of different frequencies permit a full range of clinical applications. The radial array requires special transducer technology that has been developed recently using fully-integrated manufacturing techniques.

Therefore, individual electrical connections are not "hand-wired" but manufactured using the techniques employed in manufacturing integrated circuitry. This technique reduces cost relative to performance and increases the reliability of the transducer. It permits performance improvements in inter-element matching sensitivity that in the past would have been prohibitive in cost. The radial array also uses advanced materials composed of low grain, highly sensitive special ceramic transducer material. These are among the many properties of the radial array that are important and form the foundation for this technology, **Fig. 2**.

GEOMETRIC STEERING

Direction of the acoustic pulse generated from the transmit aperture of the radial array is determined by the construction of the particular transducer and its corresponding radius of curvature. Sector images are produced by the group of elements forming the aperture and the direction of the shoot (emission from transmitter) is geometrically determined. It is important to compare this method of beam steering to those of the phased array and the mechanical sector scanner, **Fig. 3**.

COMPARISON TO THE PHASED ARRAY

Absence of long delay Lines. Radial arrays achieve steering of the beam geometrically, and hence do not require long delay lines to direct the beam as do phased arrays. This is an important difference, since long delay lines result in image degradation due to refraction errors brought by the inhomogeneous tissue paths through which the sound wave travels.

Delay lines used in the radial array are shorter and are used only to achieve dynamic focussing. Since image quality is related to refraction error effects as well as the electronic accuracy of the delay lines, it is essential to reduce the electronic delays to a minimum to achieve optimal image resolution. Short electronic delay lines are also essential to avoid the phase distortion of the signal induced by long delay lines. This is extremely important if Doppler fluid-flow sensing is to be integrated in an array, since Doppler detection involves the detection of undistorted phase differences.

GRATING LOBES

All array systems in which the transmitting aperture is composed of multiple piezoceramic elements are subject to grating lobes. **Figure 4** shows the direction of the grating lobe generated in relationship to the main lobe. Direction of the main lobe is in the direction of the acoustic shoot. In the case of the radial array it corresponds to the geometric centre of the group of elements used to create the transmitted acoustic beam.

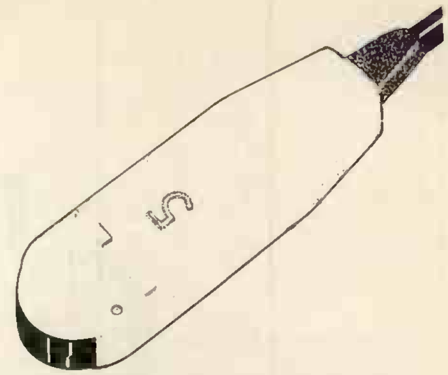


Fig.2. This radial-array ultrasound head has integral Doppler sensing for detecting and analysing blood flow.

The typical pitch, or inter-element spacing is 0.6 lambda (where lambda is the wavelength of the centre frequency of the soundwave) and results in a grating lobe that is approximately 80 degrees from the main lobe. In the case of the radial array this relationship never changes as a function of the beam direction, since a differently oriented set of elements is used to create such a shoot.

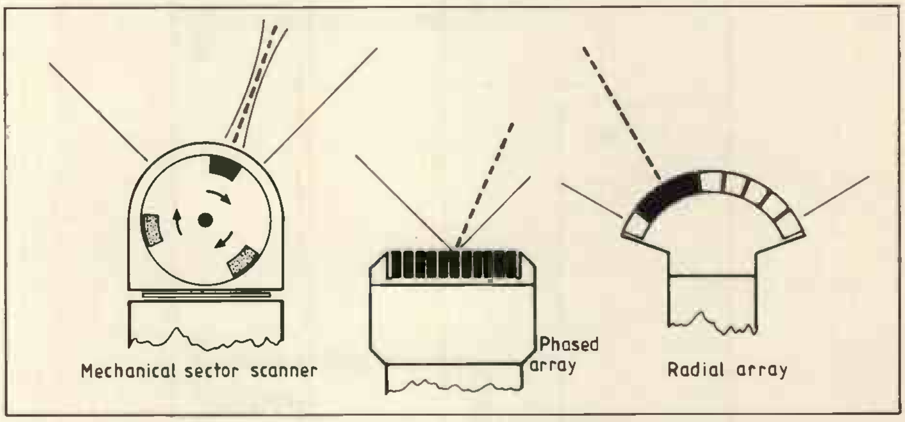


Fig.3. Each method of ultrasound scanning has its advantages and disadvantages.

In contrast, the phased array uses the same elements for every shoot but with different delays. Since the grating lobe angle is fixed, the direction of the main lobe moves closer in angle when the beam is steered at an angle to the face of the array. It is evident that the grating lobes are markedly diminished in the radial array resulting in better system performance.

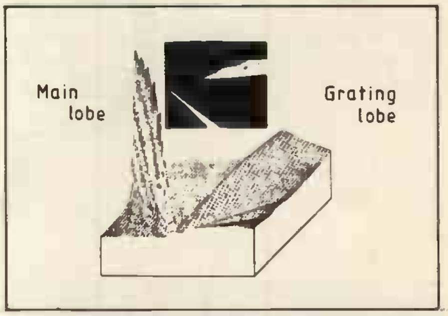


Fig.4. Direction of the grating lobe generated in relationhip to the main lobe.

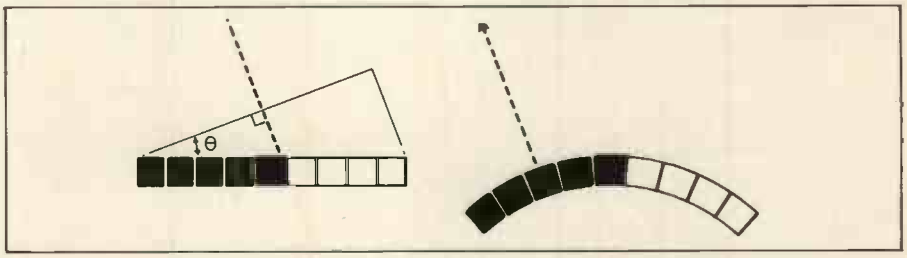


Fig.5. Effective aperture of the phased array decreases with increasing scan angle.

Effective aperture. As shown in **Fig. 5** the effective aperture of the phased array decreases with increasing scan angle. The resultant effective aperture of the phased array decreases to approximately 70% at 45 degrees of steering. Figure 5 also shows that this decrease in aperture does not occur with the radial array since the face of the radial array slowly changes direction and also "faces" the direction of the acoustic beam.

Comparison to mechanical sector scan. Geometric steering can also be contrasted with mechanical steering. The most obvious advantage of the radial array is the ability to achieve dynamic focussing which is not possible with the mechanical scanner. Reliability of the radial array is achieved with the elimination of any moving parts and the fluid chamber that are integral to the mechanical array system whether it be the single-focus transducer or the annular phased array.

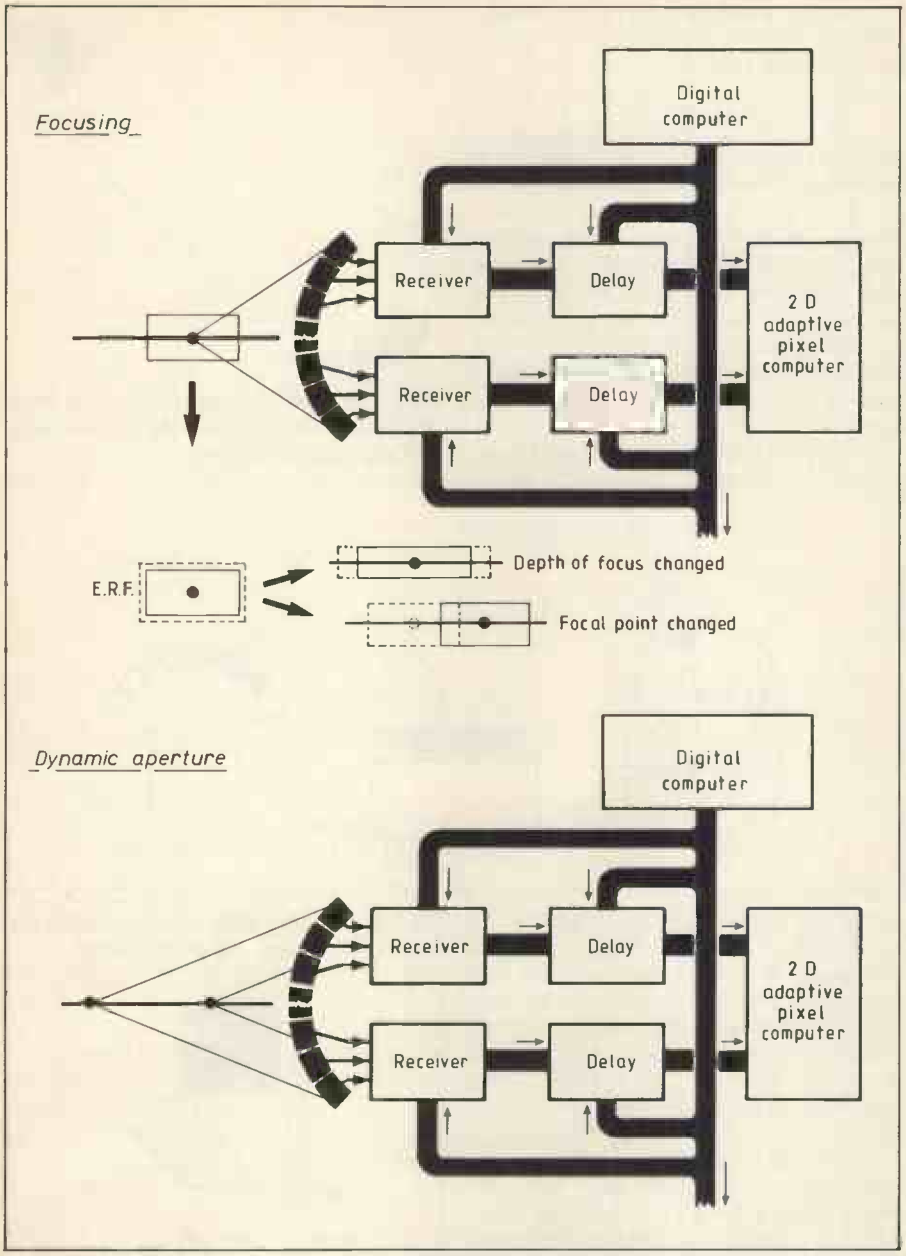


Fig.6. Electronic radial focus provides control similar to a standard camera, where both the portion of maximum forms and the depth of focus are independently controlled throughout the field of view.

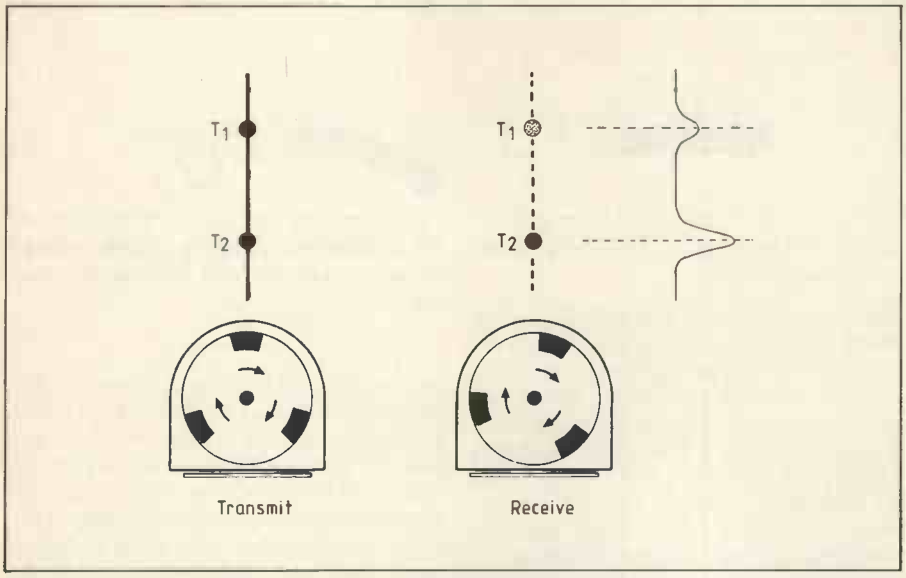


Fig.7. Echoes far from the transducer, although they return to the scanner housing, may not be received if the transducer is no longer oriented to them.

Dynamic focus. Conventional mechanical scanners using a single axially-symmetric transducer are limited in size since they are a compromise between lateral resolution and depth of field. Increasing the diameter of the transducer (increasing aperture) improves lateral resolution but only over a small depth of field.

Further increases of diameter are unacceptable, since loss of lateral resolution outside this depth of field results in an unsatisfactory image. With a single focus the question of the 'best' choice of focal zone is always a compromise. Thus the aperture of the mechanical scanner is decreased to avoid the large degradation in lateral resolution. This compromise results in a relatively uniform but diminished lateral resolution throughout the depth of field.

Although the mechanical phased annular array permits multiple focusing, it still suffers from degraded resolution outside the focal zones. Electronic radial focus, e.r.f., provides the controls similar to a standard camera, where the portion of maximum focus (A) as well as the depth of focus (B) are independently controlled throughout the field of view, **Fig. 6**.

NEAR FIELD NOISE AND REVERBERATION

The mechanical scanner is steered electromechanically, rotating at either a 'constant velocity' or oscillating with some sinusoidal velocity. In either case the transducer moves in a fluid medium and is covered by a membrane or plastic housing. The plastic housing around the moving transducer is the surface that contacts the patient. The acoustic properties of such a scanning head are responsible for artifacts from multiple echoes and diffraction of the central beam. Both of these effects result in near field 'noise', that has always plagued mechanical scanners.

AZIMUTHAL AMBIGUITY

Another defect inherent in mechanical scanners should be recognized: azimuthal ambiguity. A single line of acoustic data is obtained from the echoes returning from a single transmitted acoustic pulse in a single direction.

A mechanical scanner moves continuously and therefore during the receive period after acoustic transmission, the transducer is no longer pointing in exactly the same direction. It is clear that echoes far from the transducer, although they return to the scanner housing, may not be received if the transducer is no longer oriented to them, **Fig. 7**. Moreover, this phenomenon varies in magnitude over the depth of field, degrading image quality and distorting relative grey scale values of different tissue.

ACTIVE ACOUSTIC APERTURE

Quality of the image improves dramatically with improvements of lateral resolution and contrast resolution. Although independent parameters, they are both dependent on the acoustic beam that is transmitted into the media. These two parameters are affected by the size of the aperture and the quality of the beam that is transmitted from the face of the transducer.

In simple terms, detailed resolution is the ability to distinguish two objects that lie close to each other. Contrast resolution allows the viewer to distinguish the fine low-level echoes from the brighter high level echoes without ambiguity.

APERTURE SIZE

The first feature to be discussed is the size of the transmit aperture. It is well known that lateral resolution improves with increasing aperture size. However, it is also known from experimental data that this relationship is limited by other factors, including the shape of the transmitted acoustic pulse.

Electrical excitation of the transducer should produce an acoustic pulse of short duration. The resultant waveform, as seen on an oscilloscope, can be analysed by a spectrum analyser and displayed as a spectrum. Such a signal is composed of many individual frequencies having different strengths relative to the centre frequency of the transducer. On either side of the centre frequency the typical spectrum decreases in amplitude.

Width of the spectrum expressed in frequency units (the width is measured at some arbitrary amplitude down from the peak) is called the bandwidth. Short-lived time pulses have wider bandwidths. The typical pulse has negligible spectral strength at frequencies greater than three times and less than one fourth of the centre frequency, as seen in **Fig. 8**.

It is also well known from antenna theory and practical designs that in order to focus a particular frequency the antenna size should be at least 20 wavelengths long, i.e., 20 lambda. Since we are interested in focussing all of the frequencies that make up the pulse we must be able to handle the lowest significant frequency in the typical excitation. Since the lowest frequency is one fourth the centre frequency, (thus four times the wavelength) the aperture must be 80 wavelengths in size (twenty times four times the wavelength).

Apertures beyond this size are ineffective since negligible energy exists at longer wavelengths. Thus, the optimal aperture for acoustic imaging systems is about 80 lambda. This should be compared to mechanical systems that typically use apertures between 25 and 36 lambda. The mechanical system cannot use the optimal aperture since this larger value would compromise even further their ability to image in the near and far field. Even phased-array sector scanners do not use the large optimal aperture.

CONVOLUTION OF APERTURES

Generation of an acoustic image is a two-way phenomenon determined by the size of the aperture in both transmit and receive. The effective aperture size and the resultant image quality are expressed as the convolution of the transmit and receive apertures, **Fig. 9**.

Increasing the aperture results in a corresponding decrease in width of the main lobe of the transmitted acoustic beam. However the relative strength of the side lobe to the main lobe remains unchanged. The suppression of the side lobes of the beam increases as the 'square' of the aperture function because of the convolution effect. Thus a square transmit and receive aperture when convolved result in an aperture function that is triangular.

As shown in Figure 9, the side lobes are diminished accordingly. Side lobe reduction is important since it is directly related to improvement in contrast resolution. Apodization of the acoustic aperture changes the aperture function from a 'square' to a 'Gaussian' function. The convolution of the Gaussian aperture in transmit and receive results in a Gaussian function.

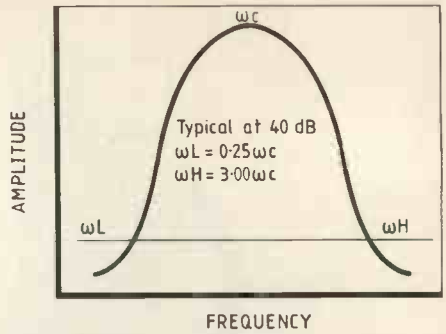


Fig.8. The typical pulse has negligible spectral strength at frequencies greater than three times and less than a quarter of the centre frequency.

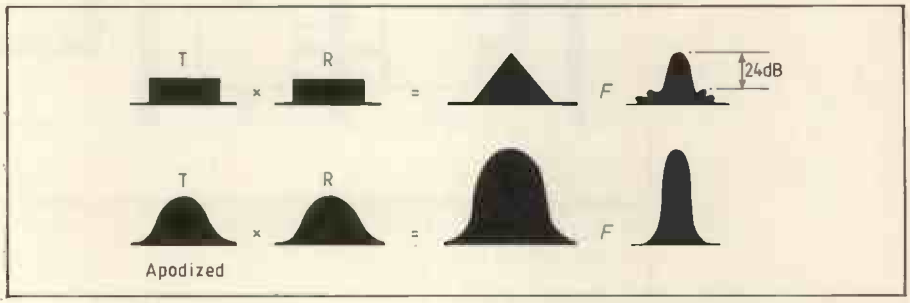


Fig.9. Effective aperture size and resultant image quality are expressed as the convolution of the transmit and receive apertures.

The Fourier transform of such a function is also Gaussian so there are no significant sidelobes. Decrease in the sidelobes is at the expense of a slight increase in the beam width. However, with an optimally chosen acoustic aperture this effect is minimal. Improved image quality and ability to detect subtle parenchymal changes accompany improved contrast resolution that is the result of the Gaussian beam spread.

ADAPTIVE PIXEL COMPUTER

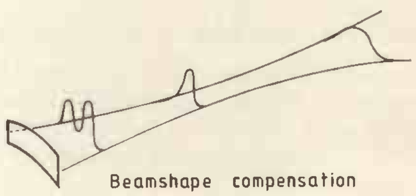
Each transmission or shoot from the elements forming the transmit aperture results in a direction of propagation of the acoustic wave determined by the entroid of the acoustic elements. The two-dimensional adaptive pixel function is complex but its objectives are clearly specified.

Reception of an undistorted representation of energy. Energy received from a particular direction as a result of a particular shoot is continuously computed as a function of depth from the returning echo. The process of converting received echo to energy is called detection.

Detected signals therefore form the image. The detection process can introduce significant errors that degrade range resolution and contrast resolution. However, the two-dimensional adaptive pixel computer uses a detection system that is extremely accurate and therefore preserves the integrity of the signal. The net result is an undistorted representation of the received energy.

Proper representation of received energy in the pixel. In any imaging system, only a finite number of memory locations represent the image pixels, and these locations are thought of as uniform 'boxes' that are placed on the image plane and located in space by their x and y coordinates. Location of these pixels does not necessarily correspond to the actual location of the energy representation of the received echoes.

Fig.10. The acoustic pulse does not have a constant set of characteristics over the full depth of the image.



In the two-dimensional adaptive-pixel computer the task is to take the properly detected echoes and allocate their energy to the pixels without distorting the image. This cannot be accomplished with simple interpolation algorithms. Furthermore, the process is two dimensional and the distribution function is unique for each pixel and is dependent on depth, angle and scan format. The net result is an adaptive process in which accurate representations of the received energies are properly computed and correctly placed in each image pixel.

IMPROVEMENT OF NEAR FIELD

The two-dimensional adaptive pixel computer is also used to perform computations in the near field of the image. It is well known that the acoustic pulse does not have a constant set of characteristics over the full depth of the image, **Fig. 10**.

Images are maximally distorted in the near field and this results in image ambiguities. The variation of acoustic beam shape as a function of depth can be compensated for with this processor so as to improve the image in the extremely complex near field.

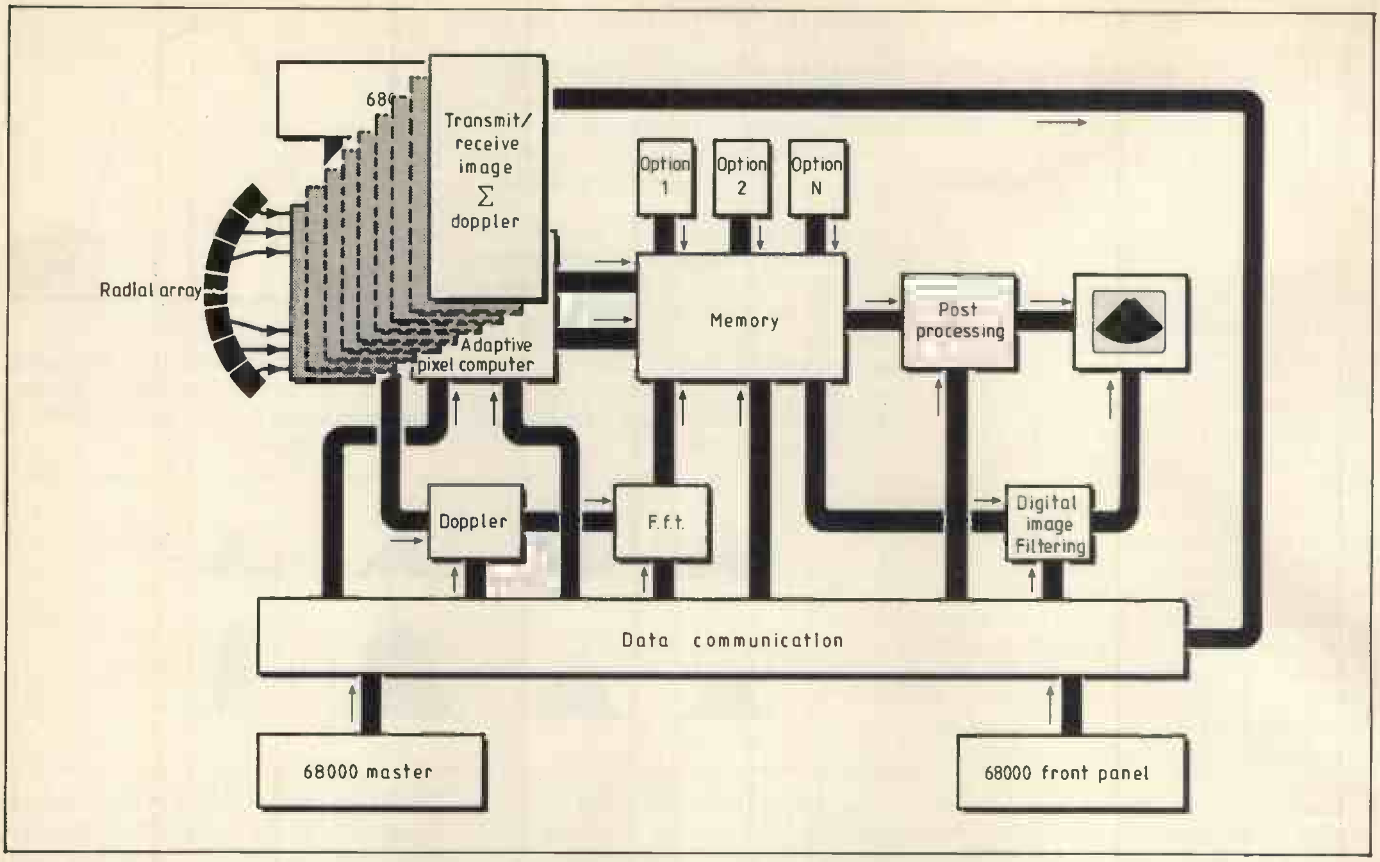


Fig.11. Radial array system employing an optimized dual-function transmitter in the transmit/receive circuit.

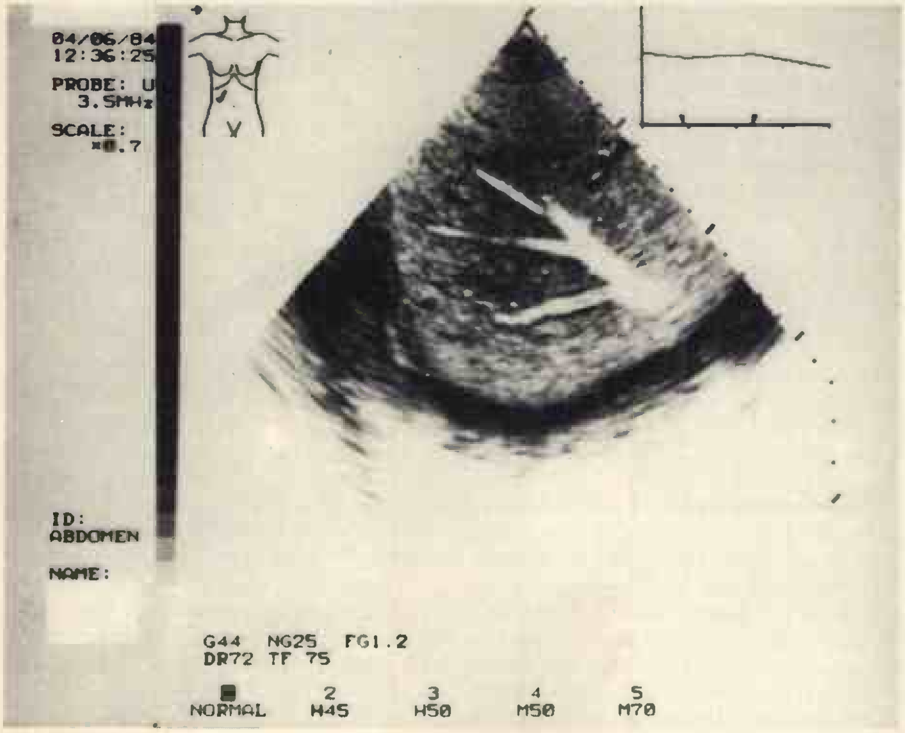
The net result is an overall resolution improvement, particularly in the near field.

INTEGRAL SIMULTANEOUS DOPPLER

The radial array system shown in **Fig. 11** employs an optimized dual-function transmitter in the transmit and receive circuitry. Design of the radial-array system took into account the fact that Doppler processing from the array is an indispensible clinical requirement.

Furthermore, optimization of the Doppler transmission from the array had to be achieved, along with optimization of the image pulse. Doppler transmission requires optimization excitation and optimized delay-line technology. All of these engineering features are provided for in the initial system as well as modularity that permits upgrades to colour-flow imaging. Colour-flow imaging requires sensitive and coherent Doppler detection as well as a fully integrated system. The radial array with integral Doppler is the prerequisite for colour flow.

Radial scanning produces good resolution and contrast over the full image field.



SUMMARY

Radial array is the technological choice for superior clinical performance. The flexible architecture of the electronic design combined with the reconfigurable software offers the user insurance against obsolescence. Improvements over the full image field in both contrast and detail resolution are a key feature of the technology.

The focus system permits the user to vary the focal point and the depth of the focal zone independently. And image processing produces contrast resolution that is clearly superior to conventional systems, assuring the clinician the ability to differentiate subtle tissue changes.

Technological features of radial scanning include high reliability and suppression of side lobes through the use of the large acoustic aperture and apodization. The two-dimensional adaptive pixel computer uses sophisticated signal processing to compensate for acoustic ambiguities in the near field and relative undersampling in the far field.

Radial-array technology described in this paper is the next generation of ultrasound systems that provides the physician with high reliability, high-quality imaging, integral Doppler and modular architecture.

Dry-cell charger

When powered by a 9V-direct source this dry-cell charger recharges a dry cell in about 12 hours. Components shown are for an AA type cell; R_x should be lowered to 68Ω for C and D types. Recharging cells in series should be avoided since it can cause cell damage.

While cell voltage remains below 1.6V, the comparator gates output from the c-mos squarewave oscillator through to the charging transistor. As cell voltage approaches 1.6V, the comparator periodically turns charging off, causing the led to flicker. This regulation prevents over-charging.

To increase charge retention, the shunt transistor provides a small amount of reverse current. For charging to be successful, discharging of the cells must have been recent, and it must have been to no less than 1V off-load.

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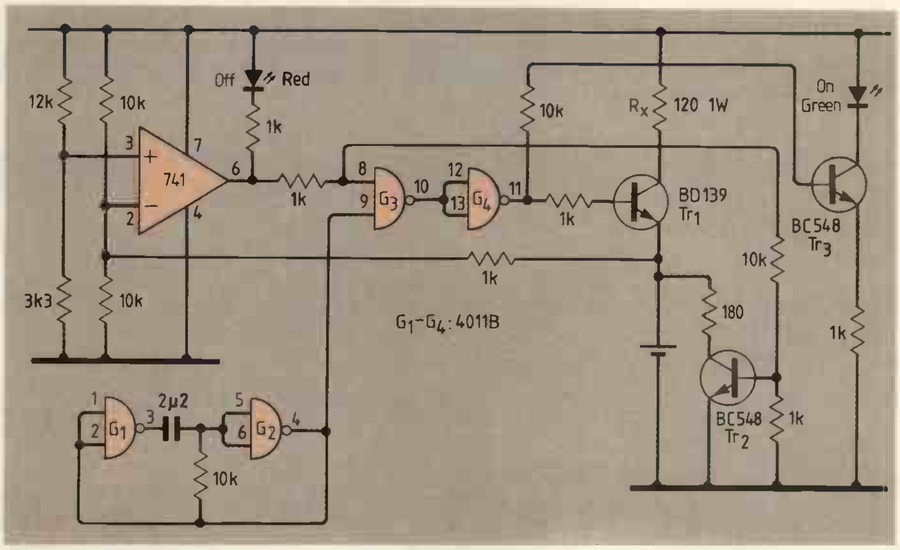

Dry-cell recharging can work, but is 'prohibited' by manufacturers because it can cause cell explosion and/or leakage. Readers without a sound knowledge of the mechanisms and consequences of these dangers should not attempt to recharge dry cells – Ed.

Automatic one-to-three data splitter for PC1512

While using an Amstrad PC1512 with internal modem as a general communications data receiver, I needed to route the serial output to three separate systems. Here is how I did it.

The Amstrad receive program was written to recognize the data source which would determine a particular subroutine selected by the program.

Since text was being received, only seven data bits were in use. Consequently, it was a simple task to modify the program to output a byte above 127_{10} as the first character and another as the last character. These codes would be detected to determine data routing.

In order to detect codes above 127_{10} the data is received by an ICL232 and converted from serial to parallel by a 6402 u.a.r.t. Next, the three most-significant bits are decoded by IC_6 and latched by IC_7. Outputs from IC_7 are used to gate the data through IC_8 to its appropriate line driver. In this case one RS422 and two RS232 i.cs.

The final code received from the Amstrad is used to reset IC_7 and await the next code above 127_{10} to be detected. In this case the codes chosen are 128_{10} for channel 3, 160_{10} for channel 2, and 192_{10} for channel 3; 224_{10} is used as the reset code.

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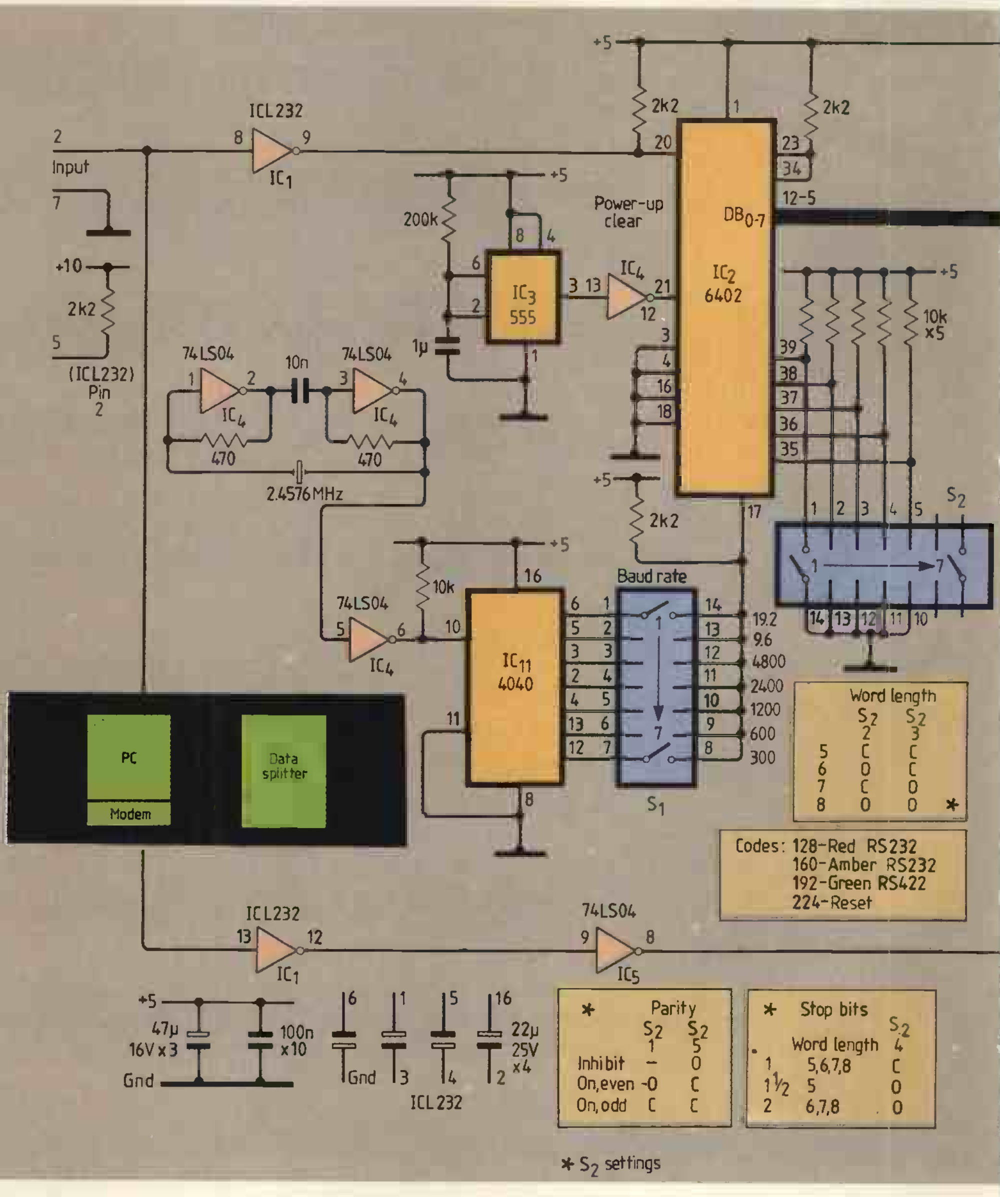


Voltage-to-current converter allows grounded load

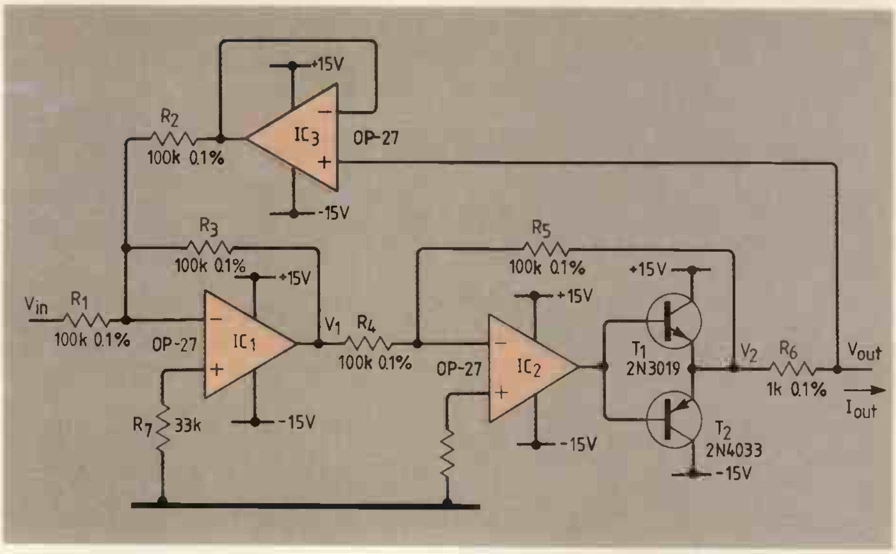
Excellent d.c. and a.c. characteristics are exhibited by this voltage-to-current converter. It contains only three common op-amps, two medium-power transistors and a few passive components.

Besides allowing grounded loads, this circuit features easy control of I_{out}/V_{in} ratio, wide output range from around 1μA to the current ratings of the output transistors, high output resistance of 50MΩ, high precision, linearity and stability and low noise.

Op-amp IC_1 inverts added input and output voltages,

$$V_1 = -(V_{in}+V_{out}).$$

The second op-amp, IC_2, and the transistors invert this voltage to give,



$$V_2 = -V_1 = -(-(V_{in}+V_{out})) = V_{in}+V_{out}.$$

Calculation of output current,

$$I_{out} = \frac{V_2-V_{out}}{R_6} = \frac{V_{in}+V_{out}-V_{out}}{R_6} = \frac{V_{in}}{R_6}$$

shows that I_{out} depends only on V_{in} and R_6.

Voltage follower IC_3 reduces any effect that sensing current might have on output current.

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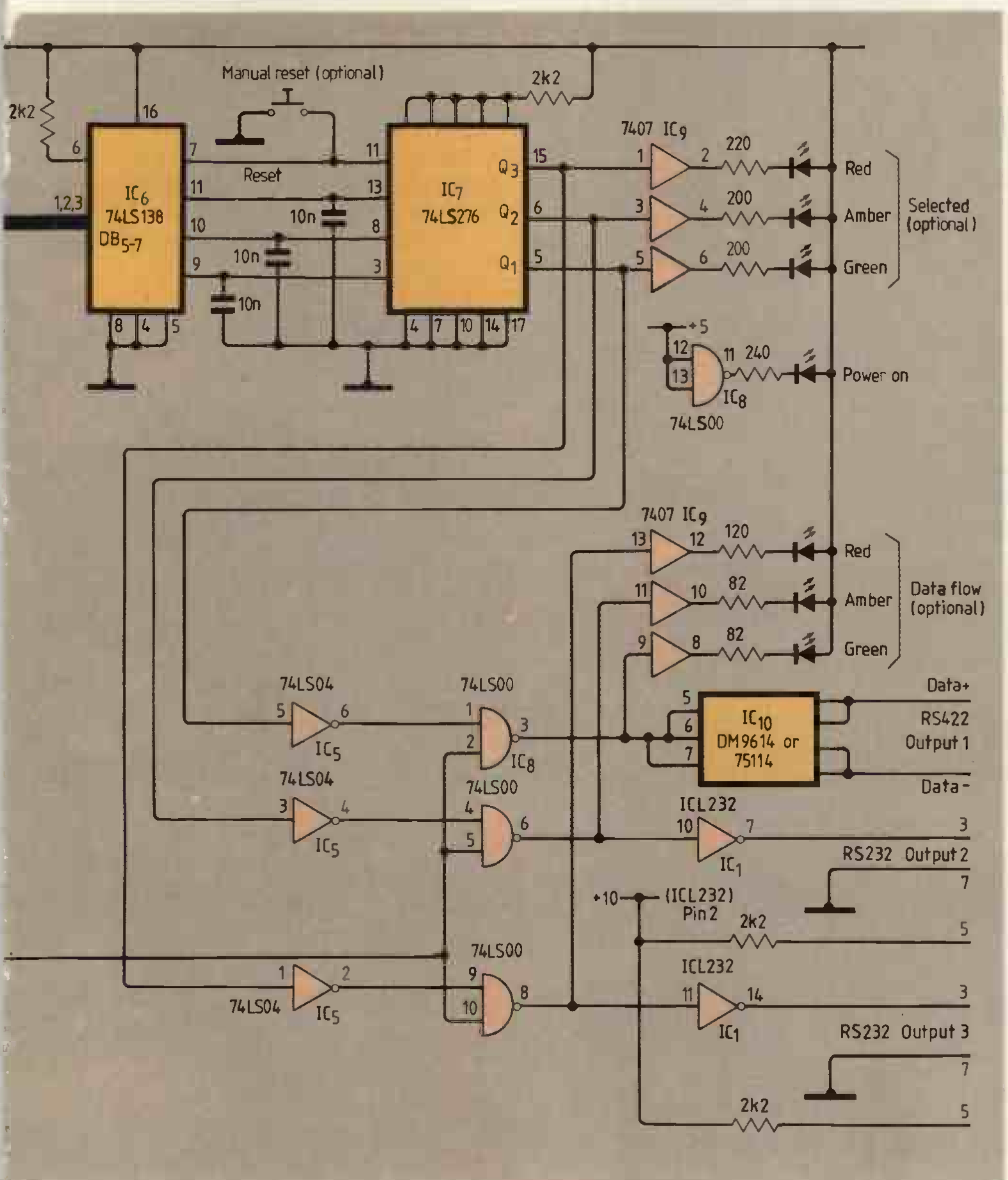
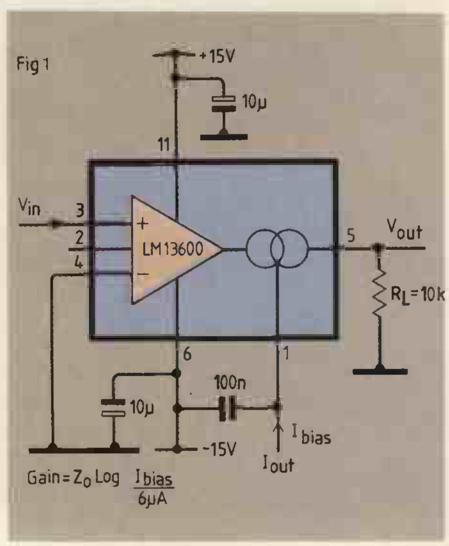


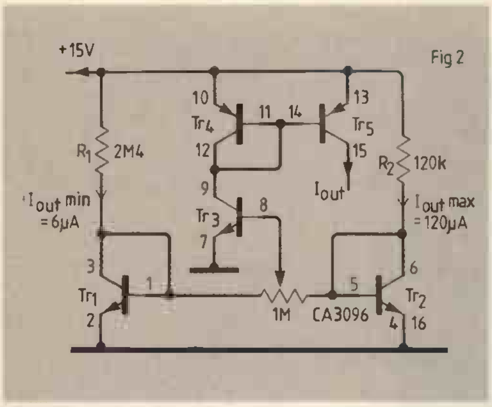
Decibel gain control

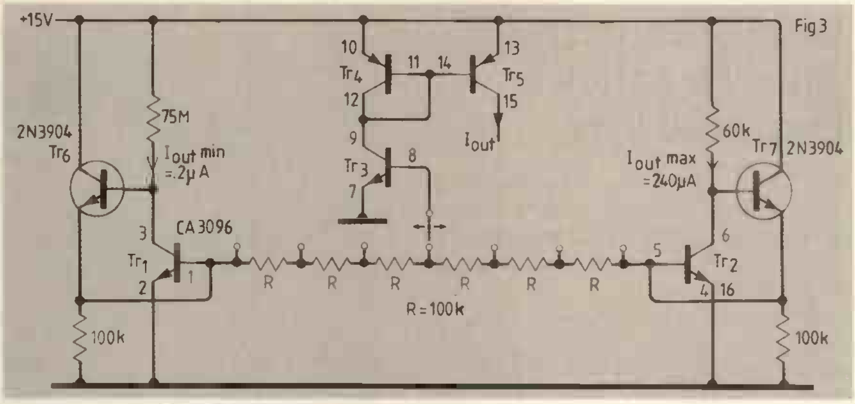
Normally a logarithmic-law potentiometer controls gain of an audio amplifier. While this practice is adequate for volume control, it is inadequate for precision audio research applications.

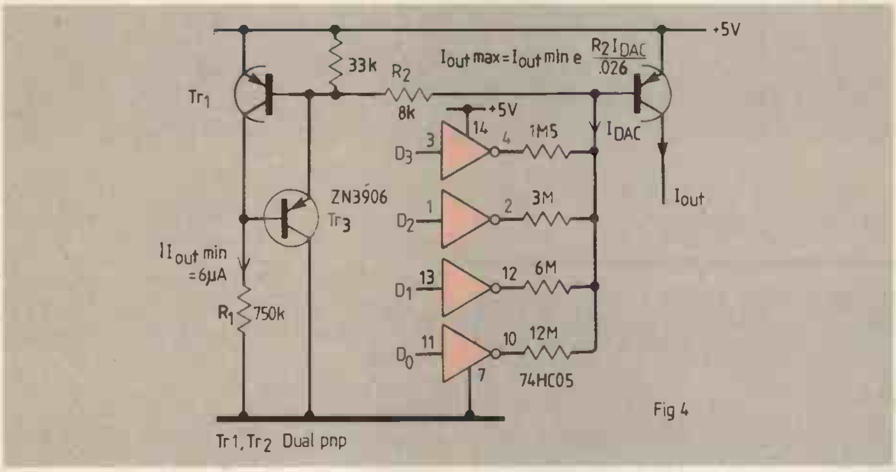
In Fig. 2, the linear potentiometer controls current, I_{out}, that sets the gain of operational transconductance amplifier Fig. 1. Current I_{out} is varied logarithically between I_{out}max (set by R_1) and I_{out}min (set by R_z) by the linear potentiometer. Position of the potentiometer wiper is directly proportional to the o.t.a. gain of Fig.1. For



CIRCUIT IDEAS







example, if I_{out}min is set to produce 0dB gain and I_{out}max is set to produce 24dB gain, then the ¾ position on the wiper will produce 18dB the gain.

For discrete gain step control, the linear potentiometer can be replaced with a single-pole rotary or slide switch, Fig. 3, with any number of taps; equal value resistors assure equal decibel increments.

Figure 3 also shows current-boosting emitter followers $Tr_{6,7}$ that supply load current to the resistor string. This allows wider I_{out}min and I_{out}max settings without loss of accuracy. Value of the resistor string is lower than the linear potentiometer to reduce the effects of Tr_3 base current.

If digital control of the o.t.a. gain of Fig. 1 is desired, the circuit of Fig. 3 can be used. The 74HC05 open-drain inverters vary the voltage linearly at the Tr_3 base to produce equal logarithmic increments in I_{out} for corresponding decibel increments in the o.t.a. Resistor R_1 sets I_{out}min directly and I_{out}max is;

$$I_{out}(max) = I_{out}(min).e^{\frac{R_2 I_{out}}{0.026V}}$$

All three gain control circuits provide output current that is essentially temperature independent. It may therefore be used for any current-controlled device that needs logarithmic scaling, e.g. programmable low-pass filter, current-controlled oscillator, power amplifier, photographic timing etc.

You might find the LM13600 data sheet from National Semiconductor useful.

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NEXT MONTH

Decoding RDS. Electronics & Wireless World presents the first ever practical decoder design for the Radio Data System, now making its appearance throughout Europe. Simon Parnall, senior design engineer at the BBC, explains the decoding process together with the hardware and software requirements.

Confused pictures from space. The consumer electronics industry has a history standards battles in all new developments. DBS is set to break new records with at least four separate standards scheduled for orbit. Will total industry confusion protect us earthlings from a galactic tide of soap? Barry Fox narrates a script that you just won't believe.

Compressing digital data. Fax type image and document data compression is finding new applications for mass document archive. IBM recently built a system for a US insurance company which cut the retrieval time from an average of three days to just 20 seconds. AMD has produced a chipset which implements the compression algorithm.

Transputers on the spot. The Inmos alternative computer architecture is gaining a favourable reputation for realtime control applications. A pocket sized satellite navigation positioning receiver uses a transputer to perform the signal conditioning and calculations. Phillip Mathos explains the system, the problem and the solution.

Fets, feedback and amplifiers. Negative feedback in audio amplifiers has been in and out of fashion like a woofer cone fed with direct cut discs. Most of the time it has been in. Lately it was out. The fact is... it's in again but will it stay in?

Designing an EPLD programmer. The usual approach of software configurable pin drivers allowing all variations of programming voltage, current and slew rate is complete overkill for most applications. If your production line is restricted to the 16L and 16R series of devices, it becomes possible to build a full function programmer for a fraction of the normal cost.

Block encryption

Following his explanation of stream encryption in August 1987, Brian McArdle examines another category of encryption and decryption of binary-coded data

BRIAN P. McARDLE

Most engineers and technicians know of the Data Encryption Standard[1] which is used to encrypt binary-coded data. It has been in existence since 1977 and has been implemented on integrated circuits which can be interfaced to 8-bit microprocessors. To be precise, this method of encryption is known as *block encryption* and the purpose of this article is to give an explanation of the various operations – the other categories are *stream encryption* and *public key encryption*. The statements and conclusions refer to any block system and not specifically to the DES.

Figure 1 shows the usual representation of a block system, which can be described mathematically by the equation

$$\hat{E}_K[P_1,P_2,P_3,\ldots,P_n]=[C_1,C_2,C_3,\ldots,C_n] \quad (1)$$

where both blocks consist of bits. The importance of the operation lies in the fact that each C_j (for j=1 to n) depends on every bit in the plaintext block. This point is developed further later. The parameter K is called the key and usually is also a block of bits; its purpose is to vary the encryption process, because the other operations within E are fixed. To use a block system, a party must choose a key from a set of possible keys, {K}, and encrypt the various plaintext blocks, which are recoverable by another party from the ciphertext blocks by using the decryption operation, provided that the appropriate key is known.

The following are the main secrecy requirements:

- {K} must be sufficiently large to prevent recovery of the plaintext blocks by trying every key in turn.
- The block size, n, should be large.
- The various steps within $\hat{E}$ must be sufficiently complicated such that individual bits in the plaintext and ciphertext blocks cannot be paired together.

In the remainder of the article, the reasons for these requirements will become clear.

PERMUTATION

This type of operation re-arranges the order of the bits that make up a block and can be easily explained by a simple example. Consider the permutation

P:	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
C:	16	8	11	9	17	22	6	19	4	18	1	3	7	20	10	13	24	5	21	2	23	12	14	15

on a block of 24 bits. This means that the bit in position 1 of the plaintext block moves to position 16 of the ciphertext block and so on. In electronic terms this is just wire crossing. Another permutation would be the equivalent of a different key in equation (1) and obviously there is a total of 24! possible permutations. If the block is formed from 3 ASCII characters (8 bits per character), then the encryption operation would result in the form shown above.

Block	1	2	3	4
plaintext	C R Y	P T O	G R A	P H Y
ciphertext	109 066 098	041 150 082	045 066 100	075 130 066

The ciphertext is written in numeric form as numbers from 0 to 255, because the permutation produces numbers which do not represent characters in the ASCII alphabet. There is no doubt that the process is a block operation, but it would have to satisfy the secrecy conditions before it could be used. The next step shows that the level of secrecy is totally inadequate.

If the plaintext-ciphertext block pairs in the example happen to be known (which would not be unusual for a system in wide-spread use), then the following arrangement, where the data is re-written in binary form, gives the most important information.

010000110101001001011001
010100000101010001001111
010001110101001001000001
010100000100100001011001
plaintext
011011010100001001100010   1
001010011001011001010010   2
001011010100001001100100   3
010010111000001001000010   4
ciphertext **block**

From a brief inspection of the two matrices, the following relationships between the columns and therefore the bits within a block can be easily identified.

C:	2	3	7	9	22	23
P:	20	12	13	4	6	21

The full permutation could probably be deduced from a few plaintext ciphertext block pairs: a block system could not, therefore, depend solely on permutations.

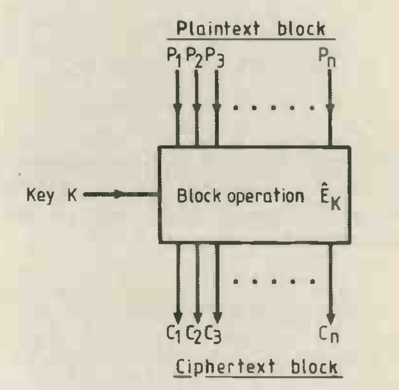

Fig.1. Basic block encryption system

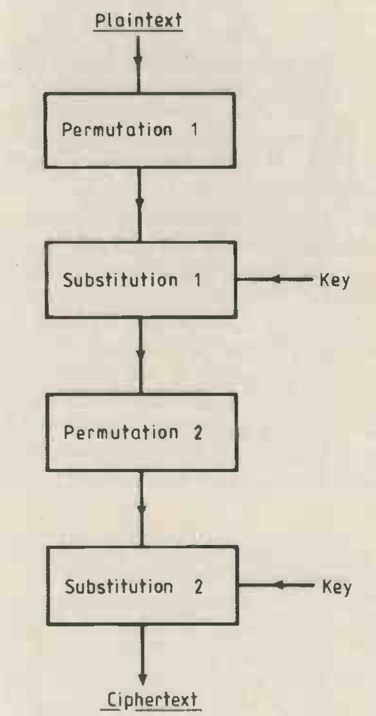

Fig.2. Permutation and substitution in combination can produce a very secure system

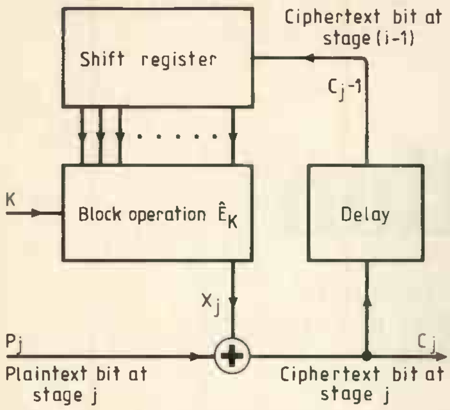

Fig.3. Cipherfeedback, for use in telecommunications. The receiver must carry out a similar block operation

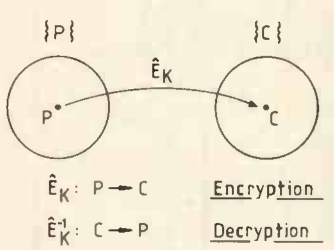

Fig.4. If elements in P or C were isomorphic, it would be possible to deduce plaintext-ciphertext pairs from a few known pairs

SUBSTITUTION

This can also be adequately explained by a simple example. A block of 3 bits has $2^3=8$ possible combinations. Thus a typical substitution would be

plaintext 000 001 010 011 100 101 110 111
ciphertext 101 110 001 100 111 000 011 010

where 000 becomes 101 and so on. In electronic terms, each substitution can be implemented using logic gates and there is a total of $2^3!$ different substitutions. It has an obvious advantage over a permutation, in that it can be more difficult to establish a connection between specific bits of the plaintext and ciphertext blocks. However, it would also be vulnerable to a known plaintext analysis[2]. Consequently, it does not satisfy the secrecy requirements even with a larger block size, such as 64 or 128 bits.

The reader should note that the above example is trivial and it does not have a key block. In practice, keyed substitutions are used within block systems where the function of the key is to vary the substitutions. A detailed explanation can be found in reference 3.

PERMUTATION-SUBSTITUTION

While substitution and permutation operations on their own are insecure, a system formed from a number of these operations in cascade can be very secure. The idea is illustrated in Fig. 2, and the reader is referred to reference 4 for a detailed explanation which is not required in this article. This principle is the basis of the DES[1] where there are 16 stages in the algorithm, the final result being that each bit in the ciphertext block depends on every bit in the plaintext and key blocks. The essential requirement is that the key in use can only be deduced by an exhaustive search where every key is tried in turn.

In the specific case of the DES, the main controversy concerns the size of the key at 56 bits which means 2^{56} different keys: a computer which can make an exhaustive search will probably be available in the 1990s. The algorithm based on permutation-substitution operations in cascade appears to be very satisfactory.

CIPHERFEEDBACK

This is not part of a block encryption process, but is used for telecommunications applications, which data is transmitted between a sender and receiver. The arrangement is illustrated in Fig.3, where the shift-register, whose purpose is to vary the input block, is provided with a seed by the user. The block operation is used to generate a sequence, $\{X_j\}$, which is, in turn, used to encrypt the sequence of plaintext bits, $\{P_j\}$, with an exclusive-or operation

$$C_j = (P_j + X_j) \bmod 2 \qquad (2)$$

to produce the sequence of ciphertext bits, $\{C_j\}$. The receiver must be able to generate the same sequence $\{X_j\}$. The block operation is not used to encrypt the data, but as a pseudo-random number generation. The arrangement is really stream encryption[2] because a plaintext bit is encrypted, transmitted and the full procedure followed again for the next bit. However, the level of secrecy is completely dependent on the block operation. The main disadvantage is the effect of transmission errors on an entire message; if a single bit is corrupted during transmission, then the input block at the receiver stage is incorrect until the erroneous bit is shifted out of the register. Hence the channel between sender and receiver must be reasonably free of noise.

MATHEMATICAL ANALYSIS

This section attempts to give a mathematical flavour to the idea of block operation. It assumes that a reader is familiar with the basic ideas in Set and Group Theory. If this is not the case, the background information can be obtained in most text books, as the ideas are elementary. Modern algebra is not just theory for mathematicians. It does have some applications to engineering.

Consider Fig.4. The set of possible plaintext blocks, $\{P\}$, and the set of possible ciphertext blocks, $\{C\}$, each have 2^n elements. Both sets are groups under the Boolean logic operations And, Or and exclusive-Or. The encryption operation, $\hat{E}_K$, for any K in $\{K\}$ establishes a one-to-one relationship between $\{P\}$ and $\{C\}$. The decryption operation represented by $\hat{E}_K^{-1}$ is the inverse operation. These statements could be considered unnecessary because they appear to repeat information that is already explained. However, a student of modern algebra will notice the possibility of an additional relationship which turns out to be significant. To ensure secrecy, $\{P\}$ and $\{C\}$ should not be isomorphic. This means that $\hat{E}_K[PoP']$ should not equal $\hat{E}_K[P]o\hat{E}_K[P']$ where P and P′ are two arbitrary blocks in $\{P\}$ and o denotes a Boolean logic operation. For example, if the logic operation is an exclusive-or, then an exclusive-Or between two plaintext blocks before the encryption operation should not produce the same ciphertext block as an exclusive-Or between the two ciphertext blocks which result from the encryption of the two plaintext blocks. Otherwise, a cryptanalyst could deduce a number of plaintext-ciphertext block pairs from just a few known pairs. This result is not immediately noticeable from the conclusions in the other sections. Further mathematical analysis depends on the particular system.

The exclusive-Or in Figs.3 and 4 does not compromise the overall arrangements because it does not alter $\hat{E}_K$, which should not be an isomorphism in the first place. A rigorous mathematical treatment of encryption can be found in reference 5.

Appendix

(1) The decryption operation for the cipherfeedback arrangement is given by the equation

$$P_j = (C_j + X_j) \bmod 2 \qquad (3)$$

and can be shown by the following example.

P_j	X_j	P_j+X_j	C_j	C_j+X_j	$(C_j+X_j) \bmod 2$
0	0	0	0	0	0
0	1	1	1	2	0
1	0	1	1	1	1
1	1	2	0	1	1

In electronic terms both equations are implemented by an exclusive-or operation.

(2) Usually the sender and receiver use the encryption and decryption algorithms respectively. In the particular case of the cipherfeedback arrangement both the sender and receiver must use the encryption algorithm *or* both must use the decryption algorithm. Both must generate the same sequence $\{X_j\}$.

(3) The term *digital signature* is an identifier which a sender includes a message. It can be used in electronic mail, etc. but is not the equivalent in law of a personal signature on paper. The full procedure does not just allow a receiver to identify a sender but also to validate a message. It is an important area of encryption and the reader is referred to references 2 and 6 for a complete explanation.

References

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Optical disc storage

Improved technology and falling prices have brought optical storage out of the laboratory and are enabling it to take root.

RICHARD LAMBLEY

After three-and-a-half decades of bringing musical enjoyment to the public – about the same lifespan as Mozart's or Gershwin's – the vinyl long-playing record is preparing itself for the attentions of the obituary writers. Displacing it from the record collector's shelves is the Compact Disc, which despite its much higher price is already outselling the black disc in some

Instead of thumbing through dusty legal tomes, Italian lawyers can now refer to this CD-rom: within the 52 000 pages of text stored upon it are all the country's working laws.

sections of the market. One major record label – Deutsche Grammophon, part of the Polygram group – has announced that its latest recordings will now appear on compact cassette and CD only; while another company in the classical music field, Nimbus Records, gave up making vinyl discs as long ago as April 1986.

Around the world, 50 plants are producing CD-audio discs, 23 of them in Europe. In addition, 15 countries, the Soviet Union among them, are building or planning to build CD factories. Some 400 million audio CDs were made during 1988, each earning its inventor Philips a two-cent royalty.

The optical revolution is propagating rapidly through the world of the computer too. This year, 1989, could see the emergence of optical discs from the obscurity of specialized high-volume data storage applications into the mainstream, with optical drives becoming almost as familiar a PC peripheral as the common magnetic variety.

Every company of more than modest size

Recordable optical discs such as the one shown here come in two varieties: write-once and erasable.

is a potential user of optical storage. Most large computer companies are now offering optical storage products – IBM, HP, DEC, Data General, Honeywell, Kodak, Bell & Howell, NEC and 3M among them. Only a small fraction of the total mass storage market (which amounted in 1987 to some £20 000M), less than 3%, is now optical; but, just as with CD music, falling hardware prices will bring about a big expansion, possibly to as much as a quarter of the total data storage requirement. And that requirement itself is growing at a rate of 40% per year. However, in the medium term – say, the next five years – magnetic discs are likely to remain the preferred first level of storage.

LASER VISION

Although optical discs still have a long way to go before their full potential can be realised, they have already been in circulation for more than a decade. The very first was the Philips Laservision disc, which appeared as a consumer product in 1978. Despite a lack of competition (Laservision pre-dated the domestic video cassette recorder) it never became a popular success in the UK and has been confined mainly to industrial and educational uses. There, the random-access character of the disc makes it more suitable than tape for interactive use. For example, Lloyd's Bank uses videodiscs for training staff at its 1500 branches in clerical techniques and the handling of customers; and in Germany and Austria, the large Bauhaus chain of do-it-yourself stores uses them to teach customers how to use power tools. Yet in Japan, the picture is very different: video discs continue to outsell pre-recorded video cassettes there.

However, the recent launch of an updated version called CD-Video (see panel), with products by Philips, Sony and others, is likely to give the medium a shot in the arm: Polygram predicts a worldwide demand for five-inch CDV discs of 350M in 1992.

CD-ROM

In the US especially, a derivative of the CD audio disc now enjoys wide acceptance as a distribution medium for large databases, a substitute for microfilm. Some 400 CD-rom titles were published worldwide in 1987 and the output is growing rapidly. Each five-inch disc can store 650Mbyte of data, or about 250 000 typewritten A4 pages – the equivalent of two sets of Encyclopedia Britannica. An alternative file format, with less error-correction, can give still higher capacities.

CD-rom drives are available as an add-on for the IBM PC and compatibles, and for the Apple II and Apple Macintosh computers, at prices in the UK from less than £700. Support for CD-rom is available as an extention to the MS-DOS operating system, enabling users to read any CD-rom disc and to recover both data and sound from it. A basic work-station that will allow you to use CD-rom need cost no more than £2000.

Among the CD-roms already available in the engineering field are a McGraw-Hill encyclopaedia of science and technology, containing 7300 signed articles, together with a technical dictionary with 98 500 terms and 115 500 definitions; Termdok, a

Optical discs manufactured by PDO, the Philips and Du Pont Optical joint company: clockwise from bottom left, a five-inch audio Compact Disc produced at Hanover (this one carries recordings by the Academy of Ancient Music); a 12-inch Worm (write once, read many times) disc made at Blackburn; a 14-inch Worm disc made by PDO at Wilmington, Delaware (this type has been in production for several years for specialized US Government applications); a five-inch CD-rom made at Hanover (this one contains the complete text of all Du Pont's 60 000 textile fibre patents at the US Patent Office); and a five-inch erasable optical disc made at Eindhoven. Write-once and erasable discs are available with or without ISO standard protective plastics cartridges.

Compact Disc Video was launched by Philips in October. The first batch of CDV releases from Polygram (Philips, Decca and Deutsche Grammophon) included 160 titles ranging from pop videos to opera. Three sizes of discs are offered, all of which can be played on the Philips CDV475 combination player seen in the photograph: five-inch, costing about £5 and giving six minutes of sound and vision (plus a further 20 minutes of sound alone, which can also be played on a conventional CD player); eight-inch, a double-sided disc with up to 44 minutes of sound and vision; and 12-inch, also double-sided, costing from about £20 and giving up to two hours – sufficient for full-length feature films or opera and ballet productions. Unlike the earlier Laservision discs, CDVs have digital sound, though the picture is still analogue. CDV discs are distinguished from audio CDs by their gold colour.

multilingual technical dictionary compiled by the Swedish Centre for Technical Terminology; the US National Technical Information Service database, covering abstracts and citations from US government and foreign r&d sources, to which over 70 000 citations are added each year; and a mass of other academic and medical databases.

Elsewhere, Boeing and British Airways have adopted CD-rom for distributing servicing information and parts catalogues for the 757 airliner. Other CD-roms in the UK include the Royal Mail's database of UK post-codes, containing details of all UK postal addresses (a boon for marketing folk preparing mailshots); an expert system to help the fight against Aids, the first in a series of health databases developed by AAH Meditel in collaboration with Nimbus Records; and, for libraries and bookshops, Whitaker's Bookbank disc, which carries details of nearly 500 000 book titles and 12 000 publishers, and is updated monthly with some 6000 new titles and 100 000 price changes.

In Germany, the University of Bielefeld has used a pair of discs to catalogue its library of 1.4M books; and in Italy, the Instituto Geografico de Agostini has compressed 52 000 pages of legal information, 60 volumes containing all the country's working laws, on to a single disc for lawyers and government officials.

Committing data to CD-rom is no longer a big undertaking for a publisher. Nimbus and PDO both offer a service, and preparation houses exist which will accept data on a floppy disc, structure it appropriately and output it on a tape suitable for mastering. At Nimbus, mastering a CD costs about £1500; production cost of the discs themselves ranges from £18 for very short runs down to £2.25 each for 5000. PDO's mastering charge is £2500, and the total cost for 1000 discs about £5000. For rapid turn-round, there is an overnight messenger service to the Hanover factory.

Compared with the cost of the stored information, the value of the disc itself is negligible; publishers can therefore afford to send out monthly update discs if necessary. Urgent updates could be transmitted to users by techniques such as the BBC's Datacast, a cousin of teletext.

A development which may make an impact in the consumer field is an interactive version of CD-rom, suitable for mixed-media presentations such as educational simulations. Perhaps the best-known interactive disc is the BBC's Domesday disc (see *E&WW* February 1987, page 189) and its successors. Interactive CD-rom (CD-I) allows the designer to create impressive animation effects using a high-resolution colour image as a background and adding foreground movement sequences. This method makes it possible to keep the data update rate within the 150kbyte/s output of the disc.

Pioneering a number of CD-rom and CD-I applications in the UK is Nimbus, which has developed systems both for evaluation and sale. Its mixed-mode CD-rom contains the company's catalogue of music recordings, with detailed contents listings, critical reviews, digitized images of the cover artwork and even a half-minute audio excerpt from each one. A finished version of this was ready to be installed in December at the Tower Records super-store in London, where record buyers would be able to browse through it using a simple touch-screen user interface.

Another novel application being developed by Nimbus, this time with the help of lexicographers at Birmingham University, is a "type and talk" speech device for the vocally handicapped. Words typed at the keyboard are recognized by software and used to retrieve spoken recordings of them from a CD. Some subtlety is included: the

Optical mass storage for ICL mainframes

New data storage technologies have a habit of being expensive; but a high-capacity optical disc system developed by a Southampton company, Kenda Electronic Systems, is, according to the company, significantly cheaper than the magnetic tape systems it replaces.

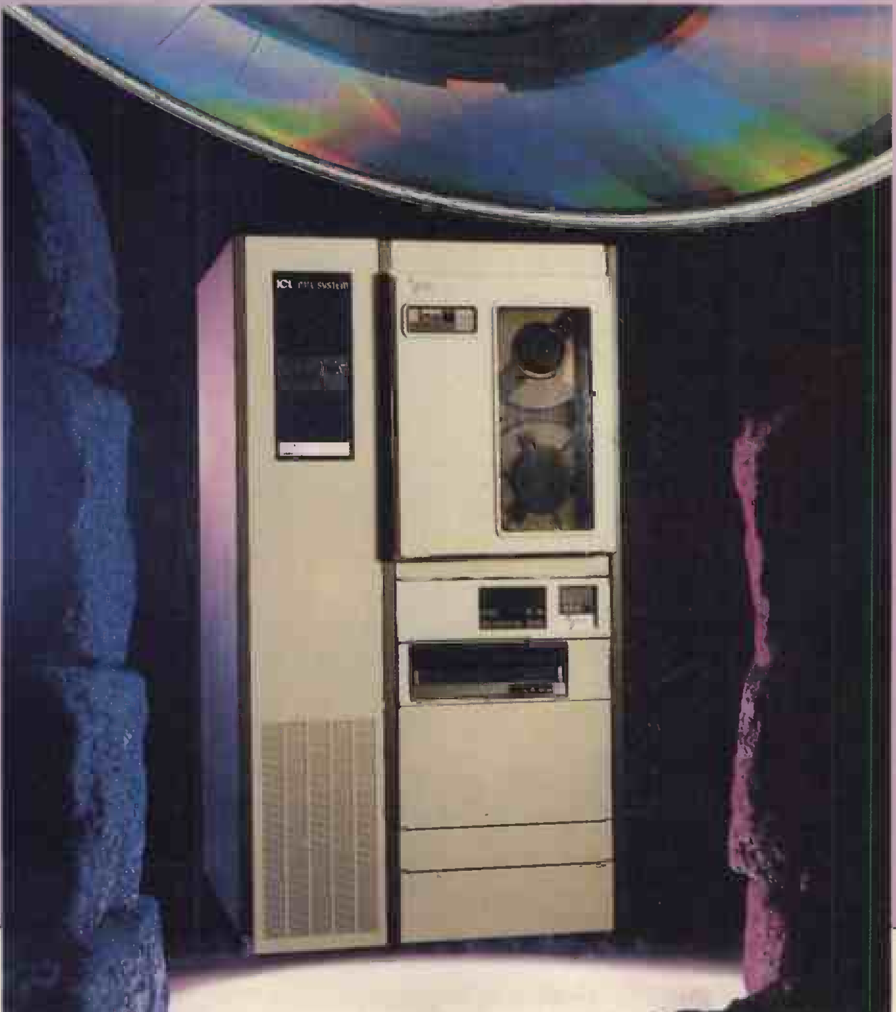
Storage medium for the data is a write-once, read many times (Worm) 30cm glass disc, capable of holding 1Gbyte per side. This is the equivalent of some 30-60 spools of tape. Taking into account the need to re-write tapes every 12-18 months to avoid loss of data, the annual cost of ownership works out at between £12 and £70, according to Kenda. Annual running cost of a library of 10 000 tapes could be as much as £150 000. But an optical disc costs just £330 at the one-off price, and integrity of the stored data is guaranteed for 30 years.

Kenda developed the system in collaboration with ICL, as an adjunct to ICL's Series 39 mainframe computers; it simply emulates a magnetic drive and so requires no additional software to run it. Some of the first drives will be installed in Government computer systems, but they could be used much more widely, especially for archiving. For very large storage requirements, a juke-box mechanism can provide on-line access to up to 95 double-sided discs. It takes only 10 seconds to load a new disc into the drive.

Under an agreement with the PDO disc factory in Blackburn, the discs will continue to be available for at least 10 years.

Data is written by a laser, which opens a hole in a heat-sensitive layer. Immediately after each bit is written, the laser's power is stepped down for a read operation to verify that the bit has indeed been written. Even if it hasn't, error concealment techniques applied during a normal read operation should ensure that subsequent accesses to that file are successful. But just to make absolutely certain, if an error is detected the sector will be recorded a second time on another, reserved part of the disc. Then, if a subsequent read fails, the sector in the reserved area will be substituted automatically.

Price of a basic system is less than £60 000.



system speaks "12" as "twelve" rather than as "one two". Up to 16 000 words can be stored on the disc, far more than the average Briton's vocabulary; but by switching to four-bit coding it should be possible to expand it further into trade jargon and other specialized language. The system also has the potential for accepting input in one language and speaking it in another.

Nimbus is also developing toolbox software which will enable users to examine and index CD material. And its US offshoot is working on interactive games using CD-I.

WORM DISCS

CD-rom's one big drawback is its inability to record user data – though of course the impossibility of cloning CDs is to the piracy-conscious publisher a positive advantage. But even this weakness, such as it is, is now being overcome by the emergence of writable and indeed rewritable (erasable) discs.

Worm discs (*write once, read many* times) began to appear at the start of the 1980s, though at the time there was no established hardware base for optical discs. But with the arrival of the desktop personal computer the outlook began to change (see also the panel opposite).

By the end of 1989, nearly 1000M write-once optical discs will be in users' hands, finding applications in such fields as document storage and archiving. In the US, the Patent Office keeps patent data on them; the American Express company uses them to store images of sales vouchers, so that it can send out laser-printed facsimiles when the time comes to dispatch the monthly bills. And an insurance company is using them for document storage, so that its remote offices can retrieve paperwork instantly without incurring delays or line charges.

Write-once discs can provide attractive cost savings by virtue of their high capacity and easy indexing and retrieval. Although the write-once feature sounds like a severe handicap, at least to anyone familiar with magnetic discs, it need not be a real one. Some stored information is safer if it cannot be changed: for example, UK companies have to keep business invoices for at least seven years and here the permanence of Worm is an important advantage.

Capacity of a 12-inch or 14-inch Worm disc is so huge that rewriting an entire file to update it need not be wasteful, even though the original version must remain on the disc (and it can even be useful to retain earlier versions). But since any write operation entails updating the disc's directory, catalogue information must be placed on an associated magnetic disc.

ERASABLE DISCS

Inevitably, pressure for an erasable disc has proved impossible to resist, and discs and drives are available or on the way from a variety of manufacturers. Philips has a five-inch magneto-optical disc (see panel) with a capacity of 325Mbyte per side, and Maxtor (a US company specializing in winchester discs and optical drives) has a type of its own with 500Mbytes per side. Sony has a 5¼-inch erasable drive, though it is not yet on sale; Olympus, Canon and other companies (mostly in Japan), have been active too.

Optical discs are an attractive choice for designers of high-capacity workstations which rely heavily on image storage, since the frictionless disc is not subject to the risk of head crashes – and the user can remove it at will.

As a high-capacity substitute for winchester discs, the magneto-optical medium will find ready uses in television and other broadcast applications. A deficiency of editing systems which rely on magnetic hard discs is that the store may not be big enough to hold the whole programme, especially where several takes of the same section are to be combined. The Japanese company Asaca now offers a video disc recorder capable of storing ten minutes of digitized moving pictures in composite PAL or 4:2:2 component-coded format, with 16 bit p.c.m. sound. This machine could be employed by facilities houses for animation and image manipulation, as in commercial production, or more simply for recording and replaying programme inserts. The disc may be erased and re-recorded repeatedly. Another machine from the same maker acts as a digital store for still pictures or sound recordings, or both.

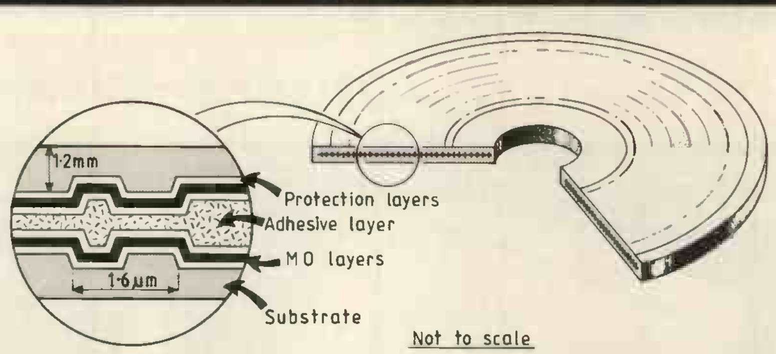
None of the present optical disc drives can rival magnetic drives for access time and data transfer rate. CDs achieve their high capacity not through a high packing density within each track (it is no better than that of magnetic drives), but through their ultra-fine track spacing: more than 10 000 tracks can be fitted per inch on an optical disc, compared with 50 on today's standard magnetic discs. With CD-rom, the data flow is restricted by the output rate for CD audio to about 150kbyte/s. Access times are of the order of half a second.

Magnetic discs could be increased in density and transfer rate by up to about four times, but would then be up against physical limitations. But optical discs could also improve, possibly by ten times. The real limitation at present is the spot size, which is governed by the laser frequency: this could be reduced to half a square micron, quadrupling capacity, but expensive new laser devices will be needed. Philips and Matsushita are working in this field.

In the CD-rom field, Nimbus has developed experimental discs in which the spacing is reduced so that the capacity is doubled to 1.44Gbyte, and even doubled again.

Another major limiting factor is the mass of the optical head, which restricts access time. One way out here is to spin the disc faster: present ISO standard discs spin at 1800rev/min and the fastest optical drives now made run at 300rev/min. A further increase to 4500rev/min might be possible, but the resulting heat might make it difficult to fit such a drive into the standard 5½-inch drive housing.

ERASABLE OPTICAL DISCS – HOW THEY WORK



Erasable optical discs in commercial use at the present time are based on *optically-assisted magnetic recording*. To execute a write operation, a magnetic field of appropriate polarity is applied to the area; and the precise spot where the bit is to be written is defined by heating it locally with a laser.

The medium itself consists of a vacuum-deposited thin film of a mixture of one or more rare-earth elements (for example, terbium or gadolinium) and transition metals (such as iron or cobalt). Coercivity is typically more than 1000 oersted. Magnetization takes place at right-angles to the plane of the film.

Reading of the disc is accomplished by a light beam, whose polarization is rotated on transmission through or reflection from the medium (the Kerr and Faraday effects). The amount of rotation is small (only a few degrees) but sufficient for good results with practical lasers and optical paths.

Technologies under development for the future include a dye-polymer medium, which changes colour on being written to, and a medium whose light-scattering properties can be altered by switching it between crystalline and amorphous states. Storage capacities of up to 1Gbyte per side could be possible in the next three years; optical discs would then be competitive for mainframe storage.

Addresses

Ambar Systems Ltd (Worm and erasable optical drives made by Maxtor): Rabans Close, Aylesbury, Buckinghamshire HP19 3RS, tel. 0296-89949.

Apple Computer UK Ltd (AppleCD SC drive), Eastman Way, Hemel Hempstead, Hertfordshire HP2 7HQ, tel. 0442 60244.

Asaca Shibasoku Europe Ltd (video, hdtv and audio storage), 284 Aberdeen Avenue, Slough, Berkshire SL1 4HG, tel. 0753-820228.

Hitachi Europe Ltd (12-inch write-once and 5¼-inch CD-rom drives): Trafalgar House, Hammersmith International Centre, 2 Chalkhill Road, London W6 8DW, tel. 01-748 2001.

Kenda Electronic Systems Ltd, Nutsey Lane, Totton, Southampton SO4 3NB, tel: 0703-869922.

Microinfo Ltd (CD-rom databases and hardware): P.O. Box 3, Omega Park, Alton, Hampshire GU34 2PG, tel. 0420-86848.

Nimbus Records, CD-rom division, Wyastone Leys, Monmouth, Gwent NP5 3SR, tel. 0600-890682.

Philips and Du Pont Optical Company (PDO), Greyhound House, 23-24 George Street, Richmond, Surrey TW9 1JY, tel. 01-948 5771. Technical Indexes Ltd (CD-rom database), Willoughby Road, Bracknell, Berkshire RG12 4DW, tel 0344-426311.

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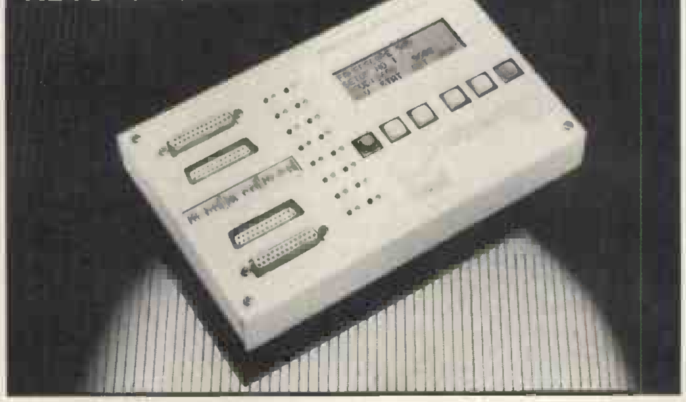

Easily operated by soft keys, with user prompts displayed on an 80 character LCD, the Fakerscope includes an RS 232 breakout box, plus a data monitor and message generator. The message generator can output both canned and pre-programmed data, while output flow control can be Xon/Xoff or level control. Each Fakerscope 500 includes 8kbyte of capture RAM. Data can be reviewed on the LCD or a separate terminal and is displayed in ASC11, HEX or baudot. The Fakerscope 500 costs only **£495.00.**

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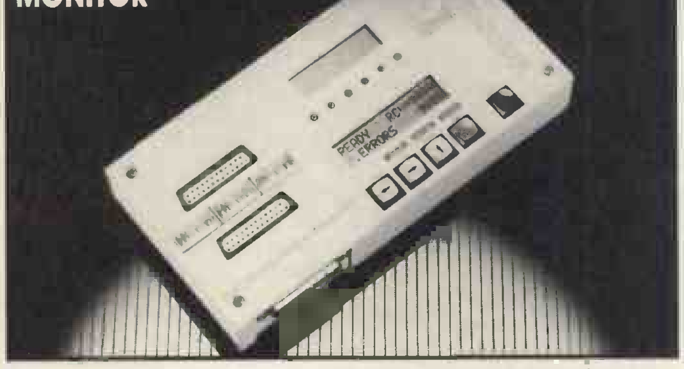

Menu driven and easy to operate, the Miniscope includes 8 kbyte of capture RAM and a 32 character LCD for data display. Data on Tx and Rx is shown in its correct relationship and the control characters displayed as symbols. The Miniscope is powered by re-chargeable batteries, includes a mains adaptor and costs only **£295.00**

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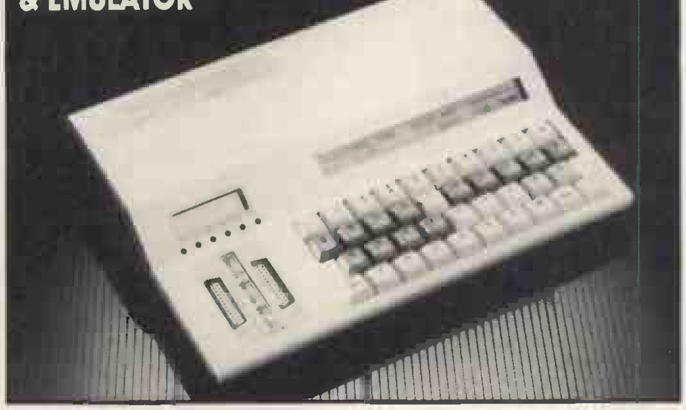

The Fakerscope 2500 has asynchronous and bisynchronous message generator and capture facilities of up to 72kbps. It is compatible with HDLC and SDLC formats, is fitted with a qwerty keyboard and will decode at levels 2 and 3, for both X.25 and SNA. In addition, it includes 8kbyte of non-volatile capture RAM, a buffer search and trigger facility and a bit error rate tester. It costs only **£987.00.**

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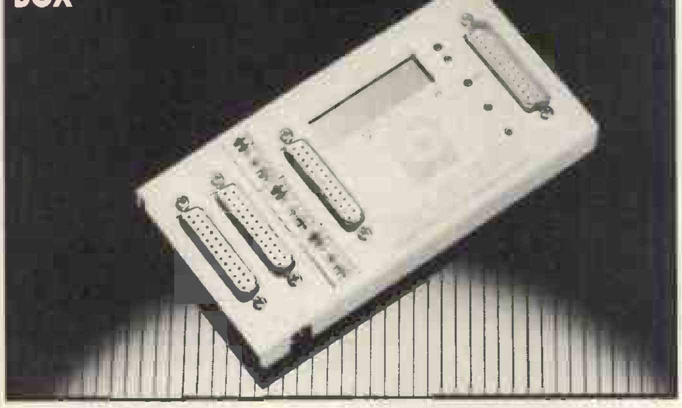

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Anti-gravity electronics

Reinterpretation of Newton's Third Law of Motion suggests that it depends upon an electronic action. Electronic interaction therefore explains the paradoxical anti-gravity properties of the force-precessed gyroscope.

H. ASPDEN

Anti-gravitational behaviour of force-precessed gyroscopes poses perplexing problems for scientists who are well versed in the principles of Newtonian mechanics. These machines demonstrate a lift force that has no counterpart, as required by Newton's Third Law of Motion, unless one imagines that a balancing force is exerted on the ether.

Traditionally we have come to accept that action must be balanced by an equal and opposite reaction. It is true that material bodies are caused to move by out-of-balance forces, but they then accelerate and there really is a balance force represented by inertial reaction. What has now emerged on the technological scene is a machine that can produce that out-of-balance force without accelerating. This means that it can, wholly or partially, offset the force of gravitation and so defy the acceleration effects of gravitation.

Some interest in this subject has been shown in the Feedback columns of *Electronics and Wireless World* (for example, see January 1987, March 1987 and August 1988 issues). For this reason and the further reason that the phenomenon has an explanation in terms of electronic effects, the following account has been written for *E&WW* readers.

THE LAW OF ELECTRODYNAMICS

The Lorentz version of the electrodynamic force law for the force caused by a unit electromagnetic charge moving at velocity v acting on a unit electromagnetic charge moving at velocity v', separated by a unit vector distance r, can be written as [v'.[v.r]] in vector product notation. When this same expression is formulated in scalar product terms it becomes,

$$(\mathbf{v}'.\mathbf{r})\mathbf{v}-(\mathbf{v}.\mathbf{v}')\mathbf{r}$$

This force is not balanced with reaction because it does not lie along r owing to the first term and because it changes magnitude if v and v' are interchanged.

Clerk Maxwell knew that a term (v.r)v' could be added without this affecting the empirical data. Such a term imparts a symmetry which assures balance of linear action and reaction, but allows an out-of-balance couple.

The alternative, which can be shown to account for induction effects with energy conservation, is to subtract such a term.

$$(\mathbf{v}'.\mathbf{r})\mathbf{v}-(\mathbf{v}.\mathbf{r})\mathbf{v}'-(\mathbf{v}.\mathbf{v}')\mathbf{r}$$

Then the formula assures no out-of-balance couple and so conservation of angular momentum for electronic interaction. It gives an out-of-balance linear force, but it can satisfy the form of gravitational interaction. This is easily seen for the situation in which the gravitational effect is set up by fundamental charges of the same polarity, same mass and same velocity (v = v'). Then the first two terms cancel to leave a mutual force of attraction acting directly between the charges and fully satisfying the action-reaction law of Newton.

NEWTON'S RULE

Students of physics, when confronted with Newton's laws of motion, are led to accept that when matter interacts by collision or otherwise (e.g. via electric or gravitational forces) there is separate conservation of linear momentum and angular momentum.

Action and reaction are balanced and this has come to mean that no self-acting machine can develop a propulsive force without shedding mass in some form. Similarly, we have always believed that no machine having a rotor and a stator can develop its own interaction to rotate the rotor at constant speed without applying a balancing torque on the stator.

Textbooks then argue from this action-reaction law and the law of energy conservation that when two perfectly elastic bodies collide so as to suffer no energy loss by heat or radiation they must comply with what is known as Newton's rule.

This rule, you will remember, says that the relative velocity of the bodies after impact is $-\epsilon$ times the relative velocity of the bodies before impact. Here ϵ is what is known as 'the coefficient of restitution', which has a value of unity for perfectly elastic loss-free collisions.

What is never explained in textbooks is the chicken-and-egg type of question, namely: 'Which comes first, Newton's Third Law or Newton's rule?' Why do we take the action-reaction law as fundamental and not Newton's rule? If Nature actually determines that Newton's rule is the more fundamental of the two, then, given that energy is conserved, we can deduce that action balances reaction.

Now, of course, it is immaterial to bother about Nature's priorities if both the action-reaction law and the rule are unquestionably valid in any physical situation. However, having discovered that the action-reaction law can be breached, there is purpose in wondering whether Newton's rule is an expression of a more basic fundamental truth.

Then it becomes possible to say that, provided energy associated with the linear, translational motion of the interacting bodies is conserved, there will be conservation of linear momentum and so balance of action and reaction. However, this argument permits us to imagine that some of that energy can be drawn from the rotary motion of one of the bodies. In this case, we will not find perfect balance of action and reaction or conservation of linear momentum. We will, in this special situation, be able to understand how a flywheel can slow down whilst using its energy to move the system linearly against the force of gravitation.

THE UNDERLYING ELECTRONICS

The implication from this is that Newton's rule is the more fundamental characteristic of interactions between colliding or interacting bodies. How can electronics be involved? Well, let us not restrict the meaning of electronics to the flow of electron currents in circuits. Electronic action can be that of the atomic electrons brought into collision with the bodies.

Consider two equal charges of the same polarity and imagine that they move along a common line so as to come into collision. Their relative velocity is a measure of the mutual electromagnetic field in the near vicinity of the collision. The energy in the field at the moment of collision is proportional to that relative velocity squared. Energy is conserved in the collision. Therefore, immediately after the collision the square of the relative velocity is unchanged from the value it had immediately before the collision. Yet initially the charges were coming together and later they were separating. Therefore, the relative velocity before collision is different from that after collision, but the square is the same. It follows that, for reasons connected with electromagnetic energy conservation, the relative velocity after impact is minus one times the relative velocity before impact. This is Newton's rule for a loss-free collision.

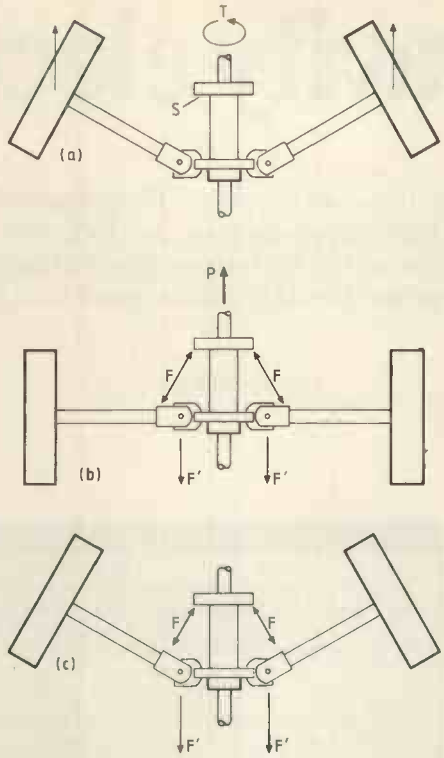
If the charges have different polarity we do not get the same result, but this merely means that the collisions satisfying Newton's rule are confined to the electrons which act as the outer guards screening the positive atomic nuclei from any involvement.

The proposition, therefore, is that, when matter interacts or collides, the action is really a summation of actions between fundamental electron-sized charges. For electromagnetic reasons the action must comply with Newton's rule and this makes that rule the fundamental condition. Thus the derivation of the law of action and reaction is consequential upon the requirement that no energy can transfer from rotary motion to the linear motion involved in the collision.

It will be seen from this that we have not had occasion to refer to forces on the ether. We do not need to countenance such forces, because we are not obliged to adhere to the action-reaction law. However, it is necessary to find a way in which to force energy from the rotary motion of a flywheel, for example, to allow this to be combined with the linear kinetic energy. This is the exceptional role of the force-precessed gyroscope.

THE FORCE-PRECESSED GYROSCOPE

It is important to realize that there is no obvious counterpart to Newton's rule when we consider rotation. Conservation of angular momentum for motion confined to a common plane is a direct consequence of energy conservation of a body moving under the action of a central force. When two bodies in rotation collide, the collisions between their individual elementary charged particle constituents will be those discussed in the linear case. However, there is some fundamental mechanism which conserves angular momentum and so assures a balance of action and reaction in that sense. No doubt this is connected with that elusive ether or the inertial frame of reference, which somehow constitute a universal non-rotating frame of reference.



Mechanism of force-precessed gyroscope, Middle diagram shows net lift force resulting from forces F and F'. Lower diagram (the toy gyroscope) shows no anomalous out-of-balance force.

Thus we do find that the gyroscope relies on the principle of conservation of angular momentum. Imagine that a flywheel spinning about a shaft is subjected to a couple which acts on the shaft to tend to turn it about an axis at right angles to the shaft axis. The plane of the flywheel will tend to be deflected by that couple. This means that the angular momentum can only be conserved about a given axis if the whole flywheel and its shaft are caused to move about a third axis orthogonal to the two axes already mentioned.

This motion is that of the precession. In a normal tower-mounted toy gyroscope the gravity forces on the flywheel develop the couple causing the precession. The centre of the flywheel precesses in a steady horizontal plane around the tower. There is no defiance of any laws of mechanics because the energy of the flywheel is unaffected by the precessional motion.

However, imagine now that the couple is not just that set up by the weight of the flywheel, but is also that of a torque applied forcibly about the vertical support axis. The flywheel will then tend to precess in a vertical plane and the key question is whether the energy needed to match the change of gravitational potential will involve exchange with that of the flywheel rotation or will be drawn from the source powering the forced precession. The answer to this, based on observation, is that it is the flywheel spin energy that is involved in the gravity balance.

The conclusion, therefore, is that the anti-gravitational properties of the force-precessed gyroscope are explicable in terms of the breach of Newton's law of action and reaction, as applied to linear momentum properties. This has been justified in terms of electronic interaction between matter.

THE FUNDAMENTAL IMPLICATION

It is curious that it has taken a discovery concerning the mechanical properties of the gyroscope to cause us to realize the true electronic basis of the laws of mechanics. The evident fact that action need not balance reaction in the linear sense can help to resolve one of the great mysteries in cosmology. Why is it that stars so far removed from one another can have both linear momentum and angular momentum?

If there can be an exchange of energy from the spin state to set up linear motion, then that need no longer be a problem. The angular momentum of a star can still be balanced against that which it possesses owing to its motion around the centre of the galaxy and the energy exchange can be local to the star.

Of more direct relevance to electronics, however, there is the classical question of the electrodynamic interaction between two electrons. Anyone who has thought about this will know that the Lorentz force law as used to work out the mutual forces between two electrons in motion gives an out-of-balance linear force and an out-of-balance linear couple. Physicists excuse this by saying that all charge motion is circuital and arguing that the out-of-balance effects then cancel out. However, they are wrong in this and cannot escape the perpetual controversy kept alive by those who do believe in the search for the real truths.

Ampere is famous for trying to avoid the issue by insisting on a complete balance of action and reaction. Maxwell, in his treatise, drew attention to an empirical law which insisted on there being no linear out-of-balance but was tolerant of an out-of-balance couple. I, however, have insisted for thirty years that the real truth rests in accepting that there has to be no out-of-balance couple, but there could be an out-of-balance linear action. This is exactly what has emerged from the gyroscope experiments.

Why is this important? Well, it comes back to that problem which Einstein could never

THE FORCE-PRECESSED GYROSCOPE

In the top diagram (above), owing to torque T applied to bearing assembly S about the vertical axis, the contra-rotating offset flywheels on pivotally-supported shafts rise, as they precess in a vertical plane. There are no vertical reaction forces on the central support, even though the masses of the flywheels are rising. (Gravity forces are disregarded).

In the middle diagram in order to force the flywheels back to a lower position, forces F are exerted between the flywheel shafts and the bearing assembly. This results in complementary forces on the bearing assembly F' acting through the pivots. However, the vertical components of the F' forces, are less than the vertical components of the F forces, because the effect of these forces and their reaction is to apply couples to the flywheel shafts which tend to lift the bearing assembly relative to the flywheels. This means that there is an upward thrust P acting on that assembly as it moves in relation to the flywheels from the position shown in the top diagram to that shown in the middle diagram. (Again, gravity forces are disregarded).

In the lower diagram, the effect of relatively weak forces F is depicted, with the precession of the flywheels needed to balance the angular momentum now being about the vertical axis. Here there is no out-of-balance force. (This disregards gravity forces, but note that such forces due to the weights of the flywheels are analogous in effect to the forces F in this case.)

Whereas the lower diagram is representative of the non-anomalous behaviour of the toy gyroscope, a combination of the actions of the top two diagrams can result in a machine with an anomalous net lift force. Such a machine was recently demonstrated by Scott Strachan, an Edinburgh research scientist. His machine incorporates a cam profile in the bearing surfaces of the bearing assembly. This allows the action to alternate between a progressive rise of the flywheel shaft and a lift-developing reset by downward thrust imposed via the cam surface. The fact that the machine develops a sustained lift force in defiance of Newton's Third Law is indisputable, owing to the placement of the demonstration machine on a balance with a knife edge support and the use of counter-weights.

solve. How can the law of electrodynamics and the law of gravitation be made compatible? Remember that Einstein was locked into electrodynamics that could be deduced from the Lorentz transformations. The Lorentz force law could hardly fit with gravity, which does require a force to act directly between the interacting particles. Ampere's old law bore no resemblance to gravitation, because it gave different forces at the same distance for different relative orientations of the particles and their motion.

Equally, the law mentioned by Maxwell was not of much use, because it involved a turning couple as part of the interaction. This leaves my law and this works for gravity, because the imbalance of linear force vanishes in the special case of mutually parallel charge motion and the law then fits the form of the gravity force. However, more than this, the law is merely based on adding a term to the Lorentz force to account for Faraday's inductive action.

CONCLUSIONS

Thanks to the development of force-precessed offset gyroscopic machines it is now established that Newton's law of action and reaction balance stands disproved. This makes it essential to regard Newton's rule as more fundamental than his Third Law of Motion. Newton's rule can be deduced from electromagnetic energy conservation as matter, which is electronic in content, interacts or collides. Starting with Newton's rule and allowing energy conservation to draw on the spin energy of a flywheel there is physical basis for understanding why an out-of-balance linear force can be produced.

In its turn, as applied, to the electrodynamic charge interaction, this condition allows the unique law of electrodynamics to be determined empirically. This law happens to be of the form required to comply with gravitation, hence advancing us towards that ultimate goal of field unification. An incidental result of this is that the difference between the Lorentz force law and that deduced in this way is precisely that needed in electronic interaction to account for the effects of magnetic induction.

In writing this article no specific reference has been made to those who deserve praise for their efforts to get the world to wake up to the practical significance of the precessing gyroscope's anomalous-force producing properties.

Supporters of Einstein's theory acclaim Einstein for having shown that Newton's law of gravitation was inadequate, but are all too ready to assume that error is involved and so scorn those who demonstrate precessing gyroscopes operating in a way which defies Newton's laws.

Who then are the pioneers that attract this attention? Are they just those who have received media publicity? So far as the writer is aware, the primary credit of long standing goes to Alex Jones, Sandy Kidd and Eric Laithwaite, but names such as Scott Strachan and Frederick Scovell are also likely to feature in the technological race that lies ahead. The patent literature extends beyond UK and already adds other names of inventors contributing to this field. This is revealed by a study commissioned by L.F. Holihan, Director of the Advanced Energy Research Institute in London.

We are on the verge of a transition concerning the viability of Newton's Third Law but, since the history of science and invention cannot be written as it happens, we must await events. In this regard, however, and concerning the author's interpretation of the phenomena discussed above, it is appropriate to note that, in accepting this article, the Consulting Editor has stated that he is mindful of similar views expressed to him over many years by Alex Jones. This article therefore serves essentially to reinforce the prior work of others and, hopefully, will further their cause.

Readers who do not remember the photograph showing Professor Laithwaite supporting a heavy precessing gyroscopic flywheel with his little finger and his arm partially extended should refer to Alex Jones' contribution on p. 64 of the January 1987 issue of *E&WW*. Surely Isaac Newton would have burned out many a candle revising his laws had he been aware of this phenomenon.

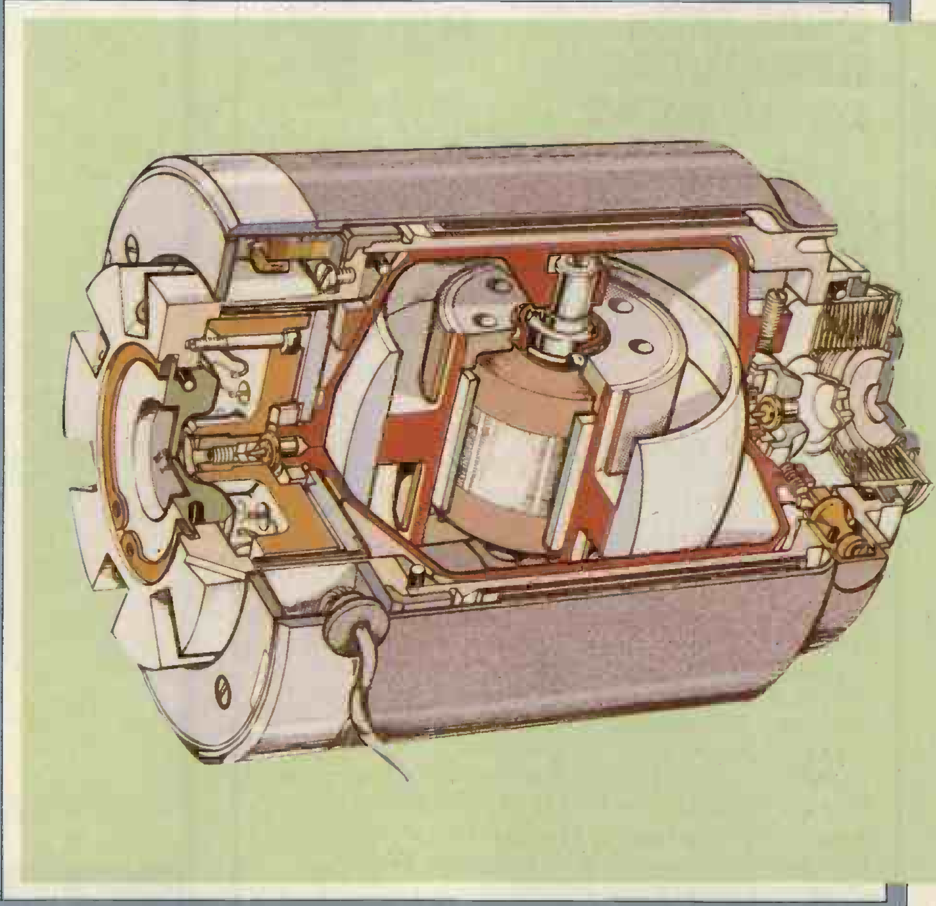
Dr. Aspden is in the Department of Electrical Engineering at the University of Southampton.

Gyroscope life test exceeds 12 years

After running almost continuously for 12 years, twelve gyroscopes based on this design have outlived their running equipment. Originally, their life test was intended to run for two years using Ministry of Defence funding: the contract was extended to five years and then continued with funding from the European Space Technology Centre and British Aerospace in support of the European Space Agency's Olympus communications satellite.

The practicability of expensive communications satellites depends on the long-term reliability of gyroscope-based attitude control and pointing systems. This particular gyroscope – the 125 – is produced by Ferranti for Iras, Exosat and the European Spacelab Instrument Pointing System. It is also used in the inertial guidance and flight-control system for the Ariane Launcher.

Apart from stops for routine tests, the twelve gyroscopes have only occasionally had extended breaks during their twelve year marathon. In the late 1970's industrial action by power workers resulted in low mains voltages which tripped out the running gear and the three month firemen's strike reduced the running time to forty hours a week for safety reasons. The gyroscopes have now achieved over ten years continuous running since the start of the tests and there are plans to run them for at least another three.



Alvey's final fling

In the final phase of the Alvey Programme, Rob Morland, director of the vlsi programme looks back on what has been achieved and also to the future with a new programme and organisation.

The past year has been eventful for all involved in Alvey, but particularly so for those in the vlsi community. GEC withdrew from a number of vlsi technology projects and in November 1987 Plessey announced that it was to acquire the semiconductor interests of Ferranti. Although welcomed as a major step toward strengthening the UK semiconductor industry, this change inevitably caused difficulties in a number of projects during the subsequent period of reorganisation and policy formulation. These problems are now largely resolved and those involved are working toward the final research goals.

Within the Alvey Directorate, major changes have taken place during the past year. The new Information Engineering Directorate in the DTI was formed in January 1988 followed by reorganisation of component-related research into the new technical area of Devices. This brings together not only the Alvey activities but also those of the old Electronics Applications (LA) Division of the DTI to form a single new organisation with responsibility not only for silicon work but also activities in compound semiconductors and a variety of electronic materials technologies.

Organisational changes during the year have not been confined to industry and the DTI. Within the Ministry of Defence, the Directorate of Components, Valves and Devices has, after many years of valuable service to defence component procurement, been the subject of reorganisation. Responsibility for development work in the components area now rests with the new Electronic Components Group under the management of RSRE at Malvern.

In Europe, the year was marked by the efforts involved in connection with the first Esprit II call for proposals. Many UK firms and academic establishments spent considerable time on aeroplanes and in meetings during the crucial run-up to the final submission date in May.

The technology strategy remains unchanged in its central thrust towards 1μ feature-size silicon circuits, with no work on III-V semiconductors, optoelectronics or microwave devices. A range of cmos and bipolar technologies is included within the programme and effort is directed both at the 1-micron primary goals an the maintenance of the long-term research base in semiconductor technology within the UK.

The extension programme strategy called for support for work within most vlsi topic areas, and 14 layer-processing projects were extended to meet this requirement. In many cases this work is primarily targeted to support the whole-process projects, but a number of areas of strategic, longer-term research were also provided with additional funding.

Extension of the industrial components of whole-process projects are targeted at the achievement in full of the Alvey vlsi goals of 1μ feature-size cmos sos and bulk cmos technologies in pilot production by 1989.

ACHIEVEMENTS IN LAYER PROCESSING

Over 40 projects have been undertaken which are concerned with the various elements of process fabrication used to produce a silicon whole-process technology. These include ion implantation, etching, layer disposition, lithography and diffusion. The research topics covered range from activities aimed at supporting directly Alvey whole-process projects to those which seek to improve understanding of the fundamental aspects of device behaviour for longer-term application within the industry. Other areas actively pursued include materials and fabrication processes for packaging of vlsi circuits, techniques for circuit inspection and failure analysis, and research on aspects of advanced manufacturing technology.

Excellent progress has been achieved in the area of plasma oxidation for mos gate dielectrics and performances equivalent to high temperature furnace oxides have been produced. Exploitation of the technology developed by Liverpool University within Project 004 is undertaken by Rytrak Semiconductor Ltd. The role of GEC in the electrical characterization of dielectric layers has been transferred to STL, Plessey and Liverpool University.

Work has also progressed well to establish low-temperature plasma-controlled deposition technologies for thin and ultrathin active and passive dielectrics. This has led to the design by Mullard and Electrotech of a new advanced dielectric deposition reactor, the prototype of which has recently been constructed by Electrotech.

For the effective development of improved performance vlsi processes, it is essential that measurement techniques with increased sensitivity and resolution are produced. A major equipment development has been the production of a high performance magnetic sector secondary ion mass spectrometer instrument by VG Ionex. Following delays in construction, the equipment was installed at Warwick University in May 1988 and is being applied to the analysis of special Alvey technology structures. In spite of the delays prospects for this instrument are such that Vacuum Generators established in July 1988 a new company, VG Microtrace, to manufacture and market the system.

There has been good progress in the epitaxial growth of silicon at reduced temperatures and pressures to support one-micron geometry cmos and bipolar whole-processes. Additionally, the prototype of a new advanced expitaxial reactor has been constructed by Philips Components Ltd (formerly Mullard Southampton) and installed at Strathclyde University for expitaxial growth studies at low pressures.

Accurate computer modelling of semiconductor process steps and resultant device characteristics is essential to the cost-effective development of new technologies. An improved model for dopant diffusion in polycrystalline silicon layers used for advanced bipolar emitters has been produced and collaborative research has enabled accurate measurement of the depth dependence of lateral spreading in ion implantations to be achieved. The first issue of the integrated process and device software package included a command language, graphics and the ability to model ion implantation, diffusion and oxidation in two space dimensions together with an off-state device simulator. The next software release included significant enhancements in the capabilities of all the component parts of the package. In addition, the Equips two-dimensional interactive process model developed by

ALVEY VLSI PROCESS SUMMARY UPDATED FROM NOVEMBER 1987 ISSUE

Technology	Bipolar CDI		UHS	Complementary m o.s. Digital		Digital		Analogue	SOS*	
Participants	Plessey Semiconductors		Plessey Soton, Oxford Univs	British Aerospace Racal STC		Plessey Research GEC Research		MEDL Plessey Research	GEC Research RSRE MEDL	
Minimum feature size (micron)	1.2	0.8	1.0	1.25	1.0	1.5	1.0	1.5	1.5	1.0
Maximum toggle frequency (MHz)	650	1200	11000	165	210	450	900	375	410	600
Effective circuit (logic gates/cm^2)	5×10^4	2.2×10^5	3.6×10^4	8×10^4	1×10^5	1.6×10^5	6.2×10^5	1.8×10^5	2.25×10^5	6.25×10^5
Figure of merit (gate Hz/cm^2)	3.2×10^{13}	2.6×10^{14}	4×10^{14}	1.3×10^{14}	2.1×10^{13}	7.2×10^{13}	5.6×10^{14}	6.7×10^{13}	9.2×10^{13}	3.8×10^{14}
prototype silicon	July 1987	July 1988	June 1987	Mar 1987	Dec 1989	Feb 1987	June 1988	Dec 1987	June 1988	Oct 1989
production	April 1988	Dec 1989	Oct 1987	July 1987	June 1990	Oct 1987	April 1989	Sept 1988	Mar 1989	Mar 1991

*Radiation sensitivity: transient upset = 10^2rad/s

Queen's University Belfast and Edinburgh University has been released to industrial and academic groups and the resultant exprience gained with the programme is being used to improve the capabilities of the code. In the device modelling projects, the Minimos-2 programme has been used to successfully simulate a 1.25μm cmos process and detailed modelling of bipolar devices is underway.

To meet the pattern transfer requirements of one micron silicon processes, research has been undertaken in the areas of lithography and etching. Included within this work is the production of high quality masks and reticles for use in optical steppers, production of electron beam resists, improved understanding of plasma processes, the development of plasma and reactive ion etchers and the application of dry etching to particular layer processing requirements such as contact hole formation.

In lithography, research work on single-level, positive resist has been exploited with the Plessey mos, bipolar and cdi one micron whole-process developments. The technology required to fabricate masks and reticles with a critical dimension control of ±0.1μm has been completed successfully. Work in this project has led to the development by Vindon Scientific of a novel image reversal system for use in mask making which is being marketed through Lamda Photometric, and to the production of a mask cleaning system by Balzers which has already been installed at Plessey Semiconductors (Swindon). The Rutherford Appleton Laboratory and Compugraphics.

A single wafer cassette-to-cassette dry etching machine produced by Nordiko incorporating a multipolar magnetic electrode is being installed at Southampton University where it will be used for reactive ion etch process development. Plasma Technology has developed a single wafer etcher based on electron cyclotron resonance. A prototype is also at Southampton University and the equipment is now available commercially; several units have been sold to customers in Europe, the USA and Japan.

A comprehensive on-chip multilevel interconnect technology based on multiple layers of aluminium alloys and silicides has been investigated. During 1987, a 4-5μm pitch process was successfully transferred into production by Plessey Semiconductors in Oldham and STC Technology have transferred a similar semi-planarized process to STC Semiconductors.

Studies of electrical overstresses in vlsi circuits included the development of test methodologies and equipments together with stress tests on cmos and bipolar test chips with geometries down to one micron. The work has led to design recommendations for circuit protection against electrical overstress which are directly applicable to Alvey vlsi circuits.

Work on silicon-on-insulator for cmos applications has continued on the improved silicon-on-sapphire, electron beam recrystallization, porous silicon and oxygen implantation routes to s-o-i. An outstanding achievement in the current year has been the production of cmos devices in porous silicon substrates which have near-optimum behaviour including high mobilities, high drive currents, low leakage currents and subthreshold characteristics steeper than bulk silicon equivalents. This was only possible due to collaborative effort with the required expitaxial layers grown at Plessey, anodizations performed at RSRE and cmos devices processed and analysed at BTRL.

Progress on the oxygen implantation approach has been affected by the curtailment of the VG OXIS oxygen implanter equipment development. However, wafers purchased from Spire Corporation (USA) are currently being processed by BTRL. In addition, research on improved s-o-s techniques has illustrated that carrier mobiles similar to bulk silicon devices can be achieved without affecting significantly the leakage performance s-o-s technologies. It is hoped that future research in s-o-i will be undertaken within a European collaborative project involving a local source of oxygen implanted material.

For the efficient fabrication of asics, it is essential to be able to schedule wafer batches through the processing facility in a manner which takes account of such variables as job priority, unforeseen job arrivals and machine breakdowns. The development of a reactive, knowledge-based scheduler, which is able to process the large quantity of data collected by a work-in-progress tracking system, is expected to be completed this month. This prototype system will then be installed on the process line at Plessey Caswell. Commercial exploitation of the techniques developed in the project is intended to be achieved through a new start-up business venture.

WHOLE PROCESS ACHIEVEMENTS

The core of the vlsi technology is the six whole-process projects that build on the layer processing technologies developed with the restof the programme. Significant advances have been made in all the whole-process projects and in general, the phase-1 goals have been achieved with the 1.5μm variants of the process being available for prototyping. Progress has also been maintained toward achieving the full 1μm goals within the coming year. Overall, internationally competitive technologies are being established in the UK in spite of, in international terms, very modest resources. Additional pull-through of many of the processes is occurring through characterization, optimization, and demonstrator programmes funded by MoD.

The first process to achieve all its goals has been the 1.25μm p-well bulk cmos process at STC Technology. British Aerospace and Racal. This project made use of extensive process and device modelling to maintain its aggressive timescales, and innovative technologies such as rapid thermal annealing and silicided junctions have been introduced for improved performance. The full 1.25μm process develoment, with double layer metallization, is now complete. Gate propagation delays of 0.5ns and a figure of merit of 1.6×10^{13} gate-Hz/cm^2 have been achieved. The process has been installed both at STC Semiconductors and at British Aerospace at Stevenage. Full design information is available as is commercial product, notably a very fast (<15ns) 16K sram with very low static power consumption into a "menu" to form the basis of an Integrated Technology Concept leading with other process steps, to a variety of process flows including bicmos. This is now also available for prototyping in a number of minimum feature-size variants.

The other bulk digital cmos process in the Alvey programme is being developed under Project 059. An intermediate 1.5μm variant has been transferred to the Plessey Semiconductors facility at Roborough, and is in production there on the 6in fabrication line. A linear shrink of this process to 1.2μm and beyond is currently being implemented at Roborough. Futher development of the process towards the 1μm goals is being continued within an extension programme at Plessey Caswell, following the withdrawal of GEC HRC from the project. All the advanced features of the process, such as trench isolation, shallow silicided source/drains, and multilevel metallizations on a 3μm pitch, have now been developed and the overall process schedule defined and successfully operated. Ring oscillator gate delays of 120ps have been measured and shift registers have achieved clock speeds of 180MHz. Current work is now concentrating on final process optimization and the fabrication and evaluation of a 300K transistor demonstrater circuit, which includes a 38K sram, prior to transfer to pilot production this autumn.

Project 060 involves the development of an analogue variant of the above cmos process at 1.5μm minimum feature size. Following withdrawal of GEC HRC from the silicon technology development, GEC MEDL has joined the project and is involved in completion of the development work on polysilicon resistors and the low voltage coefficient double polysilicon capacitors.

Process development at Plessey Caswell has included evaluation of pnp bipolar transistors with transition frequencies of over 1GHz and gains of 80. An 8-bit a/d video converter demonstrator is now ready for fabrication and evaluation prior to completion of the project this year. The process is currently being established at the Plessey Semiconductors production facility at Roborough as a major tool for enabling new telecommunications products.

Development at MEDL of a commercially viable one-micron radiaton-tolerant cmos s-o-s process (known as S 1) is being addressed within the 058 extension programme. The intermediate goal of a 1.5μm minimum feature size process (S 1.5) in pilot production has been achieved. Fully functional 64K srams have been made in the S 1.5 process and have given access times of less than 55ns over the temperature range −55 to +125°C, and initial radiation testing has validated required levels of radiation tolerance for space and military applications.

A MoD-funded 35,000 gate sea-of-gate chip in the same process technology is close to hardware evaluation and further characterization and optimization of the process for military requirements is also being supported by MoD. A provisional 1μm process flow has been defined and the areas of silicides, materials and double layer metallization step coverage have been identified for further optimization. Evaluation of a variety of s-o-i substrates is included in the work plan and is scheduled for the coming year. Work at RSRE has demonstrated the viability of cmos s-o-s processing below the 1μm level.

A 1μm collector diffusion isolation bipolar process combines the attributes of good digital performance and flexible analogue capability in a simple, low mask-count process. The project is continuing following the takeover of Ferranti Electronics by Plessey Semiconductors. The intermediate 1.2μm minimum feature size, 4.5μm grid pitch technology (FAB4) is in pilot production and starting to satisfy requirements for commercial products this year. Current MoD developments include a 8-bit 200MHz adc and a 20ns 16bit multiplier. Three components (amplifier, oscillator and divider) for the input stages of the digital cellular radio communicators part of Project LD002 have all been fabricated in the FAB 4 technology and have operated at speeds of between 1 and 2GHz. Development of the 1μm feature size, 3.6μm grid pitch process (FAB5) continues. Viable alternative technology options have been identified and are being fully assessed and optmized, including rapid thermal annealing, polysilicon emitters and silicited contacts. Further optimization is occurring under MoD support. Establishment of the process and verification of the design rules are due to be completed in the coming year.

A ultra high speed 1μ bipolar process for digital and analogue applications is being developed at Plessey Caswell, in collaboration with Southampton and Oxford Universities. Very significant advances have been made during the past year and the performance being achieved now is equal to the current state of the art. Process improvements have led to an increase in transition frequency to 22GHz and gate delays down to 40ps. A divide-by-eight circuit has operated at 10.7GHz, a world best silicon result, and similar to the best in any other technology. Similar comparisons worldwide on a gate delay/power per gate basis are equally favourable. This process, which includes trench isolation, polysilicon emitters and three-layer metallization with a via pitch of 3.6μm (known as HE2) is near the end of the

SILICON TOWARDS 2000

Last year's report "A Suggested VSLI/CAD Science and Technology Programme for the UK" which recommended a sharply focused national and European effort in the areas of vlsi science, technology, architectures and cad, designed specifically to meet user needs towards the year 2000.

Following publication of this first document, the strategy group undertook a programme of consultation with government, industry and the academic community which led to a number of enhancements being made to the proposed programme. Then in January the DTI was reorganised under the government's Enterprise Initiative and the new Information Engineering Directorate established to oversee collaborative research work across the whole IT field. Government policy in this area was covered into White Paper which confirmed UK support for the Esprit II programme and announced a new national IT research effort to follow Alvey.

Further work undertaken within the vlsi and cad community in early 1988 revised Silicon Towards 2000 strategy both to take account of new government policy for research support and to add details to the outline workplans, particularly in the cad and vlsi Architectures areas. Specific steps were taken to develop and promote cross-boundary topics which linked devices work more closely with research in the other two IED programme areas of systems engineering and systems architecture. A new version of the document was published in March 1988 and, following consultation, the final workplan was competed for distribution in June.

The technical content of the Silicon Towards 2000 programme is designed not only to meet specific supplier and user needs but also to complement the expected UK involvement in the Esprit II microelectronics programme. In the area of whole semiconductor processes, it is expected that the magnitude of research required can only be supported on a European scale. However, the underlying science, much of which requires strong collaboration between industry and academia, forms a vital topic for the national effort. A new concept of Semiconductor Science Consortia has been developed to address this need.

Interconnection and packaging technology features for the first time as a major area for collaborative research, and i.c. manufacturing technology is also included within the strategy, although research in this area is not expected to start until later in the programme.

A change in balance away from support for whole processes is evident in the emphasis being given to cad work within the new programme. Building on the successes of Alvey, a substantial cad research effort is planned, with targets set to meet the needs of leading edge users into the 1990s and beyond.

In vlsi architectures too it is intended to establish a number of forward looking projects which will probe into the opportunities for design innovation provided by current and planned generations of vlsi technology.

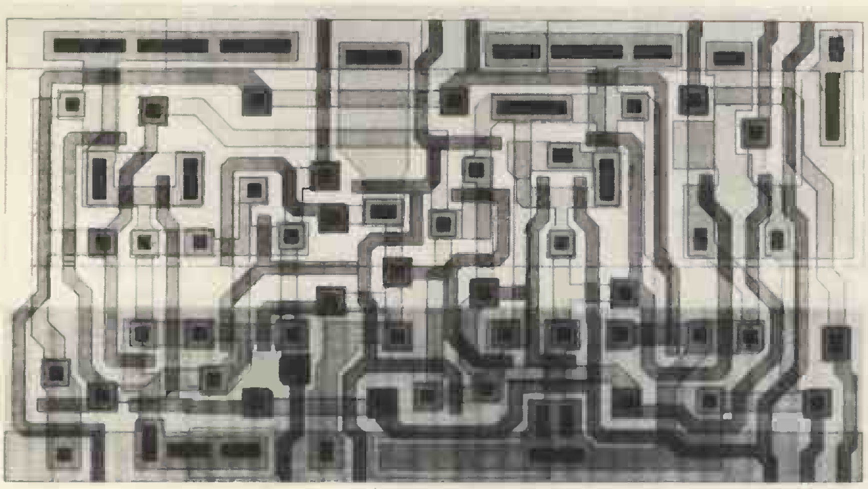
In parallel with detailed preparations for the new national programme, many research groups within the UK microelectrics community spent the first part of 1988 actively engaged in preparing proposals for the Esprit II programme, aiming for the closure date for submissions in May.

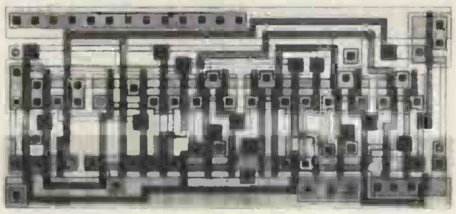
With tales of light aircraft delivering proposals to Brussels on the final day, it was clear that UK organisations were taking this opportunity for enhanced European collaboration seriously.

In the event, 112 proposals were received by the European Commission in the microelectronics area and there was UK involvement in 81 of these. Of course, the programme was heavily oversubscribed and the complex process of technical evaluation was made more difficult by the need to maintain a balance between the various topics to be covered, and between large and small projects. About 26 projects have now been approved, although several take the form of competitive definition phases. There is UK involvement in 19 of these, representing a substantial research effort in national terms.

As might be expected, many projects have been obliged to cut their funding to fit the available resources for the Espite II programme, even though the overall Community funding for this call has been increased from 600 to 780 million ecu. Those involved in approved projects have been working on revised plans to take account of this, whilst at the same time considering their role in the new UK national programme and the important links to be made between their national and European research activities.

In establishing the new joint national IT programme, the opportunity was taken to rationalize the existing complex structure of committees that advised the DTI, SERC and Alvey Directorate. In the devices area, a new Devices Committee advises both DTI and SERC on all programmes related to semiconductor technology, devices, design and cad. Supported by four sub-committees, thew new structure will cover silicon and compound semiconductor technology, certain electronic materials work, cad vlsi architecture research and optoelectronics. In addition, it will be closely associated with molecular electronics and high temperature superconductivity.





Alvey support has resulted in cmos and bipolar processes with feature sizes down to 1μm. Typical logic cell using 3μm design rules, top, with an actual size of 200μm reduces to 125μm with the 1¼μm Alvey process (STC semiconductors).

the development phase having met all its target specifications. It is now being transferred into pilot production at Plessey Semiconductors, Swindon. An earlier version of the process (HE1) involving a 5μm pitch technology is now entering full production at Swindon. Circuits already developed on this process include an MoD-funded 8bit universal shift register operating at 1.5GHz, a 240-gate differential CML array with toggle rates up to 3.6GHz, a wideband limiting amplifier with a gain of 40dB and bandwidth of 2GHz, and an 8bit dac with a 1.2ns settling time. Plessey Semiconductors have recently signed an agreement with AMCC in the USA to jointly develop and market a family of ecl gate arrays to be fabricated on the HE process with complexities of up to 14,000 gates. Initial manufacture will be at Swindon but the agreement also covers the fabrication of the arrays by AMCC.

The chart on page 34 is a revised summary of Alvey process technologies and includes the current schedule of availability dates for design rules, prototype silicon and first production.

VLSI ARCHITECTURES AND ACHIEVEMENTS

The main objectives in the vlsi area were to investigate novel silicon architectures with applications in information, signal and data processing and to stimulate the full and timely exploitation of the process technologies. Included are various parallel processing techniques, including systolic and distributed arrays. Methods of improving testability and achieving a high level of fault-tolerance are also being investigated, as is the application of architectural concepts to the achievement of viable approaches to wafer scale integration.

The development work of a dynamically reconfigurable processor array at Southampton University has been completed. The manufacture of a test chip in 3μm cmos, and simulation of an array of 1024 processing elements, has demonstrated the potential of the technology. Enhancement of the design, particularly in the area of data routing, has been completed and the work is now headed for commercial exploitation.

The hardware-oriented work is complemented by a software programme the objective of which is to develop a virtual system architecture language for SIMD machines. This will prove highly beneficial in enabling wider access to new parallel processing systems through standard parallel languages such as Fortran 8X.

The development of a design methodology and fault-tolerant design techniques for wafer-scale integrated circuits is the objective of Project Arch 073. The work covers all aspects of design through to manufacture and includes economic modelling. Four demonstrators have been selected, three in silicon and the other a hybrid, each with a viable but fundamentally different defect tolerant architecture. All designs are well developed and will be realised in hardware within the next few months. Economic modelling has been undertaken by Brunel University. An example application in the image processing field indicates an order of magnitude improvement in weight, power consumption and performance of a wsi solution compared to the conventional approach, with a net cost saving of 50%.

The suitability of regular array architectures to a range of commonly occuring problems is being investigated in Project Arch 013. Two differing applications have been selected for detailed study, these being a video picture motion estimator (ME) and a Cordic arithmetic function generator. The ME design involves a 15×15 array, operates at the word level and permits estimation of the whole picture without interruption. Commitment to silicon is expected shortly. The Cordic processor operates at bit level and involves an 8-bit input and output architecture for simultaneous generation of sine and cosine functions. Performance in excess of 80 Mwords per second and 40MHz clock is anticipated from the 3500 gate-equivalent design which has already been committed to silicon using Plessey's Alvey supported 1μm, three-level metal cmos technology.

Work is progressing well within the Prism project to develop an advanced processor for use in real-time computer graphics applications. The prime requirement is to produce a family of devices to support high performance computer generated imagery. The family comprises processors for geometry, display and database control. A single chip cmos design solution for the geometry process has been completed and commitment to silicon is anticipated in the near future.

Warwick University is developing vlsi architectures for single-chip, high-speed arithmetic functions for use in a variety of applications requiring high system throughput. The emphasis is on a modular approach for the system so as to minimize design time. Work has concentrated on unified transmission techniques such as Cordic and redundant number systems. A 16-bit processor executing Cordic algorithms has been designed and fabricated in 3μm cmos technology. The design of a pipelined version of this processor, to operate at 10MHz, is nearing completion and commitment to silicon is anticipated by the end of 1988. The design will enable operation both in array configuration and as a dedicated coprocessor. Performance improvement anticipated over the non-pipelined version results from the elimination of the area-consuming barrel shifter and use of redundant number formulations. To evaluate this technique, a redundant number adder circuit has been designed.

The objectives of project Arch 020 are to develop the logic design of a function library for serial architectures and to produce and demonstrate a new-generation silicon compiler for technology independent specification of signal processors based on this library. The work is intended to relax the technological and functional limitations of the existing process dependent compilers. To date, a new cmos process-independent compiler has been demonstrated and work to develop a behavioural-to-structural translator is well advanced. A high performance radix-4, 1024-point, complex Fast Fourier Transform system with a 512μs cell library, and commitment to silicon is anticipated in the near future.

VHPIC APPLICATION DEMONSTRATORS

The Alvey strategy called for a number of advanced demonstrators to assist in pulling through the new technologies into marketable opportunities. Unfortunately, insufficient funding was available to support the substantial commercial demonstrators although very useful work was included in the Alvey Large Demonstrator project on mobile information systems. This aimed to utilise Ferranti/Plessey cdi technology in advanced cellular radio system applications.

However, the MoD has in place a demonstrator programme designed to help meet its long-term procurement needs, and sufficient progress has been made on a number of projects within this initiative to justify reporting.

The VHPIC Application Demonstrator Programme jointly funded by MoD and Industry the principal objective of encouraging the timely exploitation in Defence equipment of the advanced cad and vlsi capability developed under the Alvey programme. The chosen route has been to support the design and fabrication of a number of signal processor asics with a functional throughput rate in excess of 10^{12} gate – Hz/watt and to demonstrate the performance benefits that this offers in a realistic system application.
realistic system application.

The chips under development will be fabricated in the Plessey or STC 1.2/1.25μm cmos processes, but it is now intended to also include in the programme some circuits fabricated on the MEDL 1.5μm cmos/sos process and on a Plessey 1μm process. Each of the chips currently under development has made extensive use of Ella in the design and simulation stage, which has involved the specification and validation of designs typically at complexity levels of 20,000 to 80,000 gates.

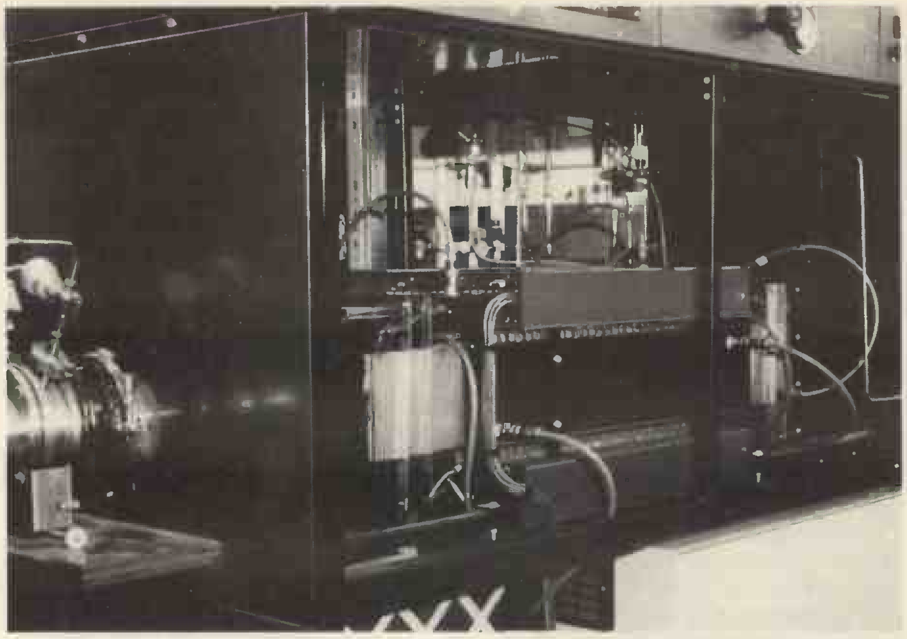
The systolic node array demonstrator is being developed by STC Technology, supported by STC Defence Systems, and is based on a reduced instruction set signal processor with a versatile i/o and internal routing capability. It has been optimized for use in a wide variety of dedicated array configurations so that processing throughput can be directly traded for physical size and power consumption. An adaptive beamformer systolic array module incorporating 10 node chips can, for example, provide a sustained throughput in excess of 340 Mflops with a dissipation, of 50 watts for a complete hardware system with all necessary i/o interface and control circuitry.

Each individual node chip consists of a digital circuit incorporating over 180,000 transistors at an internal clock speed in excess of 15MHz. The design features multiple floating point arithmetic blocks for very fast numerical computation and six parallel 24-bit wide data ports with fifo buffering for rapid transfer of data between chips.

The design route has taken a top-level Pascal specification to a detailed hardware description in Ella and converted this into an Isis-HDL based design at the silicon level. This route has revealed and solved a number of problems in the cad software and has generally identified a need for faster, more effective simulation facilities. The chips will be fabricated by STC Semiconductors at Footscray using their 1.25μm cmos process.

Modules to be built using the node chip design should find a wide range of applications, particularly for beam forming, Doppler filtering and adaptive signal processing.

The digital radio demonstrator is also being developed jointly by STC Technology and STC Defence Systems. The original aim was to produce a number of zero-i.f. combat net radios in manpack form and demonstrate the possibility of complete software control of the mode of operation. This required a 20-bit adc and high performance low-power digital signal processor. The work has demonstrated the technical viability of the original concept but commercial pressures and production timescales have meant that the actual demonstrator to be built will now be a high performance receiver.



To study advanced expitaxial silicon growth at low temperatures, this radiantly heated epitaxial reactor has been built in-house at Philips Components Southampton (VLSI project 022).

The key vhpic component is a programmable digital filter chip which, in combination with a high performance bipolar pdm, produces the essential front-end analogue-to-digital conversion with better than 19-bit accuracy. The programmable digital filter chip contains approximately 98,000 transistors, with parts of the chip operating at a 96MHz internal clock rate. The design route followed has been similar to that described for the systolic node chip, and it has been necessary to carry out much of the lower level simulation on a Zycad hardware accelerator to bring the simulation times down to manageable level. It is intended to fabricate the chips using the 1.25μm cmos process at STC Footscray.

THE INTELLIGENT WINDOW ADDRESSABLE MEMORY

Demonstrator is being developed by Racal Defence Electronics with support from Racal Research. The objective is to show that the use of vhpic technology makes it possible to adopt a new and more effective sysem architecture approach to signal processing in esm systems. The concept was first verified by the successful design of a window addressable memory chip using umbrella 2-3μm cmos design rules. The 108,000 transistor chip functioned correctly and was fabricated with sufficient yield to demonstrate that very impressive system performance could be achieved. The design is now being shrunk to provide increased reliability and yield by fabricating it on the Plessey 1.2μm cmos process.

Although primarily aimed at specific esm applications this chip should be widely applicable to other systems using an associative memory approach. Design is now proceeding to produce a much more complex chip about 340,000 transistors, which will incorporate several of the wam blocks together with the control circuits and data processing functions required for particular esm applications. This demonstrator has also used the Ella/Isis design route and the final chips will be fabricated on the Plessey 1.2μm cmos process.

The aim of the **sonar dsp** demonstrator, which is being developed by Plessey Naval Systems with support from Plessey Research, is to design an asic which provides a programmable arthimetic unit optimized for signal processing tasks in sonar applications. The chip should be suitable both for lower power use in sonobouys as well as offering a high throughput multichip solution for the case of large towed array sonars.

The original design was based on the anticipated availability of an aggressive 1μm cmos technology but has now been modified to use the 1.2μm Plessey Alvey process which is available in the required timescale. The design route used has been based on Ella together with the Plessey Classic system. The chip contains about 230,000 transistors and executes 24bit-block floating-point arithmetic with a typical 35ns clock cycle time. It has dual bidirectional 24-bit ports for i/o communications. These processors can be linked together in a data-flow architecture to provide a wide range of trade-offs between processing throughput, board area and power dissipation. It is hoped that some of the ideas explored in this project can be applied to the design of a new asic based on 1μm Alvey technology to provide a further increase in computational throughput.

Adapted from the 1988 report of the Alvey Programme, available from IEE Publication Sales, Station House, Nightingale Road, Hitchin, Herts, price £15.

FEEDBACK

Whose is the cavity magnetron?

In Ken Smith's November article discussing some of Hertz's brilliant pioneering experiments with electromagnetic waves he implies rather too direct a link between Hertz's devices and the cavity magnetron invented during the second world war. When working as a postgraduate student at Birmingham University I was told that Boot and Randall originally envisaged the cavity magnetron as a form of reflex klystron, in which a beam of electrons, which had been velocity modulated by sending them past the gap of a resonant cavity, were induced to pass the gap again by bending them round in a magnetic field instead of reflecting them back from a suitably biased electrode. With this development background the capabilities of the magnetron as a source of high power pulses appeared as something of a gift from the gods (Wotan perhaps?).

Detailed computer calculations of electron orbits within a magnetron published after the war showed that, while those of the electrons emitted from the cathode which absorbed energy from the oscillating fields in the cavities quickly returned to it, those that did reach the anode did so by way of long and complicated paths which, when their phases of emission relative to the oscillating fields were taken into account, allowed the electrons to delivery a substantial fraction of the electrostatic energy they acquired in moving from cathode to anode up to the cavity oscillations. These favourable trajectories were found to group into current carrying 'spokes', which rotated round the magnetron axis at an appropriate subharmonic of the oscillation frequency – a finding in qualitative agreement with the inventors' original expectations of its mode of operation, though they could hardly have anticipated the extent of the azimuthal velocity modulation which would be induced.

Thus the cavity magnetron involves the technology of ion optics in a high vacuum. Although today this is very much taken for granted, the first significant steps towards it came appreciably later than Hertz's experiments with electromagnetic waves.

C.F. Coleman
Grove
Oxon

Students fit for work

In reply to 'Comment' in the November issue of *EWW*, I agree when the author states that there are many people who say it is no longer worthwhile to spend one's spare time building their own equipment.

It is a sign of the times that many young engineers fresh from the campus are experts when it comes to filling in reams of paper full of formulae explaining the intricacies of a particular device in a circuit, but ask them to stoke up the iron and do a hands-on job and you could be met with a look of contempt; it would seem to some that it is below their station to have any physical contact with the hardware that they have been theorizing about.

I, like many others will no doubt remember the halcyon days of the 50s and 60s when the weekend would mean a trip to London to visit the Mecca in Lisle Street. There, with a few pounds in your pocket you could purchase more bits and pieces than you could carry home, and the stillness of winter nights was broken by the he-hawing of metal being formed in the gentle art of *chassis bashing.* But what joy when you fired up your latest masterpiece, to be confronted by a pair of 807s and its associated circuitry in all its glory giving you sound, light and heat!

Don't get me wrong; I am not saying that the clock of technology should be held back, but I agree with the author that it is made too easy today for students of the industry. As a past employer of the so called *high-flyers* fresh from the halls of learning and clutching their degrees, experience has shown me that while these chaps are great theorists, hands-on trouble shooting and some iron work is beyond their comprehension.

Of course I am not advocating the *'suck-it-and-see'* approach; with today's hardware that could be costly to an employer, but there should be a more balanced attitude of young engineers, a good grounding in theory together with *hands-on* experience, most of all a love of the job and all it entails.

E. Pearson
Gatehouse of Fleet
Kirkcudbrightshire

FFT and non-repetitive sampling windows

The articles on FFT by Sewards in August and Hutchings in October contain some very useful material, but unfortunately both emphasize applications in which the sampled signal changes little from one windowed interval or 'snapshot' to another, whereas the extra speed of the FFT really comes into its own in permitting real time analyses of successive snapshots from fluctuating signals, such as the waveforms of continuous speech.

Hutchings' statement that 'since the digital computer only processes samples... of the signal... we modify the continuous transform into the discrete transform DT...' is misleading. Instead, as Sewards states in his second paragraph, this modification introduces '...the implicit assumption that the signal outside the block repeats what is in the block from past to future infinity'. Nevertheless FFTs can be and are applied to obtain approximations to the Fourier transforms of pulses with lengths of up to say half of the window width.

The window width determines the smallest frequency interval over which sensible results can be expected, while the digital sampling interval determines the highest frequencies which are properly registered. For continuous signals the allegedly superior resolution provided by a rectangular window applies only if one already knows something about the waveform outside the window. With speech one doesn't. It can be shown that if a series of overlapping windows are used to generate FFTs from a speech waveform, and the phase information is retained, the stored information allows the original waveform to be reconstituted. The book 'Numerical recipes in C' (W.H. Press *et al.*, Cambridge University Press) contains an excellent section on FFTs.

A final point is appropriate to some of Allan Sewards's figures. Digitization is *not* a linear process. Thus digitizing a signal, Fourier-transforming it, and then applying the averaging process which corresponds in the frequency domain to the use of a Hann window produces a different result from applying the Hann window to the time signal, digitizing it, and then carrying out the Fourier transformation. The difference is small if the number of bits is large, but will become more and more evident as the number of bits is made smaller.

C.F. Coleman
Grove
Oxon

Car theft

I have just read the article by Jeremy Stevens on page 1108 of the November issue about an anti-theft device for a car. I have owned American cars (Cadillacs) for some forty years and for the last twenty-five years or more anti-theft devices were an option on most General Motors cars but standard on Cadillac. They made use of the fact that any door which opened operates a light switch and as there are also lights under the bonnet and under the boot lid, that information is passed into a control unit which comes into operation when the central-locking system has been activated by key.

Any attempt to open a door, bonnet or boot immediately sets an alarm off which, in my opinion, is the obvious type of alarm in that alternately the horns sounds, followed by all four headlights flashing. This goes on for twenty minutes, ceasing just before the batteries run down.

It is interesting that if anybody hears a car horn being used they turn round to see what it is, whereas there are so many alarm noises now made by sirens etc. that nobody takes any notice of them.

I have all the circuit diagrams available of the General Motors system and in my view it would be quite easy for a person with reasonable intelligence to make use of all these door switches as described by Mr Stevens.

Joshua Sieger
Poole
Dorset

No integers for $a^n+b^n=c^n$

There seems to be no magazine in Australia which invites letters of the range dealt with by the incomparable Wireless World. I am sure that this will interest other readers.

The following, in which all variables are integers greater than zero, is offered as a proof that where $n>2$; there can be no integers for $a^n+b^n=c^n$.

Where $n>1$, x^n-y^n can always be divided into two factors, one of which will be $x-y$. When such exercises have been carried out a few times it becomes apparent that the process could be continued indefinitely and that the number of elements, all positive, within the second set of brackets equals the value of n. For example,

$$x^{11}-y^{11}=(x-y)(x^{10}+y^{10}+xy^9+x^9y+x^2y^8+x^8y^2+x^3y^7+x^7y^3+x^4y^6+x^6y^4+x^5y^5)$$

Of course, $x^2-y^2=(x-y)(x+y)$

and $x^3-y^3=(x-y)(x^2+y^2+xy)$

$$x^4-y^4=(x-y)(x^3+y^3+xy^2+x^2y)$$

$$x^5-y^5=(x-y)(x^4+y^4+x^3y+xy^3+x^2y^2)$$

ad infinitum.

So, regarding the equation $a^2+b^2=c^2$ and the supposition $a^n+b^n=c^n$, $c-a$ must always be a factor of b^n (or of c^n-a^n) and $c-b$ must always be a factor of a^n (or of c^n-b^n).

Regarding the supposition, a^n and b^n can be factorized in accordance with these rules only when a, b and c values match sets of integers applicable to the equation; for, if a^n and b^n are respectively divisible by $c-b$ and $c-a$ then so must be a^2 and b^2.

Name and address supplied
Western Australia

Mine not Wien's

Many thanks for publishing my articles on "Remotely controlled RC oscillator" in October and November of 1988. I would like however to make the following comment.

The original title of the article was "Another look at RC oscillators", this was changed by your staff to include the wording "Remotely controlled Wien oscillators". Although the Wien-bridge circuit was referred to in the article the various forms of the oscillator described were of my own design and not based on the Wien bridge circuit.

Austyn J.P. Williams
Raglan
Gwent

Anti-gravity electronics

My article on "Electronic Action and Reaction" in this issue (p.29) was written before the news that the lift forces in the Kidd machine were confirmed. Readers may have seen the front page story in the *Sunday Express* of 23 October and the following BBC reports. The device has moved from the realm of being a scientific curiosity and is headed towards commercial technological application. There are tremendous prospects ahead in the space and aviation fields.

From the layman's point of view this is not perpetual motion, but a means of 'swinging' through space, like a Tarzan who can hook the end of a rope to any chosen point in the sky.

Physicists need something more by way of scientific justification and, with this in mind, I feel I should comment further on the electronic explanation in my article. The 'relative velocity' proposition from which Newton's rule is derived is really better formalized in Clerk Maxwell's treatise by what is termed 'electrokinetic energy'. To derive the more familiar forms of electrodynamic law, Maxwell used Fechner's hypothesis. This says that an electronic current is really attributable to a counterflow of charges of opposite polarity. In modern scientific parlance this implies electron-positron pair creation and annihilation in a way that corresponds to current flow. I emphasize this because I well appreciate the problem of defining proper frames of reference for electron collisions, especially where electrons collide when moving in the same direction.

The following references to my prior published work on this theme will help readers interested in this subject.

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1 "The Maxwell-Fechner hypothesis as an alternative to Einstein's Theory", *Spec. Sc. Tech.*, vol.8, 283 (1985).
2 "New perspective on the law of electrodynamics", *Physics Letters*, vol.111A, 23 (1985).

Smps waveform distortion

I am afraid that Dr Pedder in his article 'How to combat waveform distortion by switch-mode supplies' on page 1016 of the October 1988 issue, has got it all wrong. I went through the same calculations and found that the input currents are much smaller.

During recharging of the capacitor mean current is,

$$i=C\frac{dV}{dt}$$

where dV=20V and

$$dt=\frac{10\times20}{180}=\frac{10}{9}\text{ms},$$

which gives

$$i=450\frac{20\times9}{10}=8.1\text{A}.$$

Mean current over one period is therefore,

$$\frac{8.1\times20}{180}=0.9\text{A}$$

With the 1A switching converter current, it gives a mean input current of 1.9A (not 9A).

Also, the rms value of the current pulse of trapezoidal form is,

$$i_{rms}=\left(3+\left(\frac{12\times10}{20}\right)^{1/2}\right)\times\frac{20}{180}$$

$$=(3+2.45)\frac{1}{9}=0.605\text{A}$$

and not 3.2A as Dr Pedder stated.

A. Bouhadjera
Basingstoke
Hampshire.

• Dr Pedder comments: Dr Bouhadjera has misunderstood the article. Firstly, 9A is mean current level *during* the recharging pulse, not the whole cycle. The recharging current is shown, when idealized, in Fig.3: 15A peak, 9A mean during the pulse and 1A mean over the whole cycle. Secondly, the rms input current is 3.2A as stated. Dr Bouhadjera has somehow calculated an rms level below his mean level – a form factor of less than unity – which would be very useful.

Hand-held satnav receiver

A pocket-sized satellite navigation receiver that can be carried about by a person on foot to enable him to find his position is being developed by Inmos. It uses the GPS (Global Positioning System) satellite navigation scheme (April 1987 issue, p. 377) and an Inmos transputer (microprocessor) to perform digital signal processing and computation for position finding. The receiver is battery-powered and small enough to be held in the hand. Its size is largely determined by the area of the flat, planar type L-band antenna with its slightly larger ground plane – about 130mm×80mm. The antenna folds down over the keyboard and display.

An important feature of the design is that its extensive use of software reduces the time needed to acquire four GPS satellites to only a few seconds. Conventional receivers can take several minutes for this task.

The design approach adopted was described by Philip Mattos of Inmos, Bristol, at the recent IEE conference on mobile satellite systems (see also item below). Hardware is used for the rf circuits and for interfacing to the transputer, while dsp software running on the transputer performs four-channel frequency tracking, code tracking and filtering/detection, as well as the necessary calculations for position finding. The bulk of the cpu's work is taken up by the signal processing rather than by the position calculations.

After the 1542.42MHz below-noise satellite signal is picked up by the flat antenna, which is printed on a ceramic substrate, it is fed through an rf amplifier, downconverted by an integrated diode ring mixer to 70MHz and passed to an if amplifier. A second, similar mixer then downconverts the signal further to 5MHz. The cycles of signal are hard limited to form digit pulses, which are clocked serially into an eight-bit shift register. From this, eight-bit bytes are transferred through a link adaptor to the processor.

Basically the receiver's task is to acquire the satellite's pseudo-random noise (prn) signals, which are transmitted by spread spectrum technique over a 2-MHz band, decode them by correlation with a locally generated prn code, detect the 50bit/s modulation on the carrier and finally calculate the position fixes by solving simultaneous equations for x, y, z and time. In the dsp function of the transputer the digitized received signal is first multiplied by the locally generated prn code, using the exclusive-or logical process, and then mathematically downconverted to a very low frequency (0-15kHz).

A fast Fourier transform is then performed on the resulting signal to detect the presence of a satellite by determining the frequency and amplitude of its signal. The transputer's link dma facilities are used to input one batch of data while another batch is being processed. Mr Mattos said that the method adopted was so fast that it could be used for both acquisition and tracking on the same processor. Finally the data phase-shift-keyed on the carrier at 50bit/s is extracted and transferred to the satellite and receiver position-finding calculation processes.

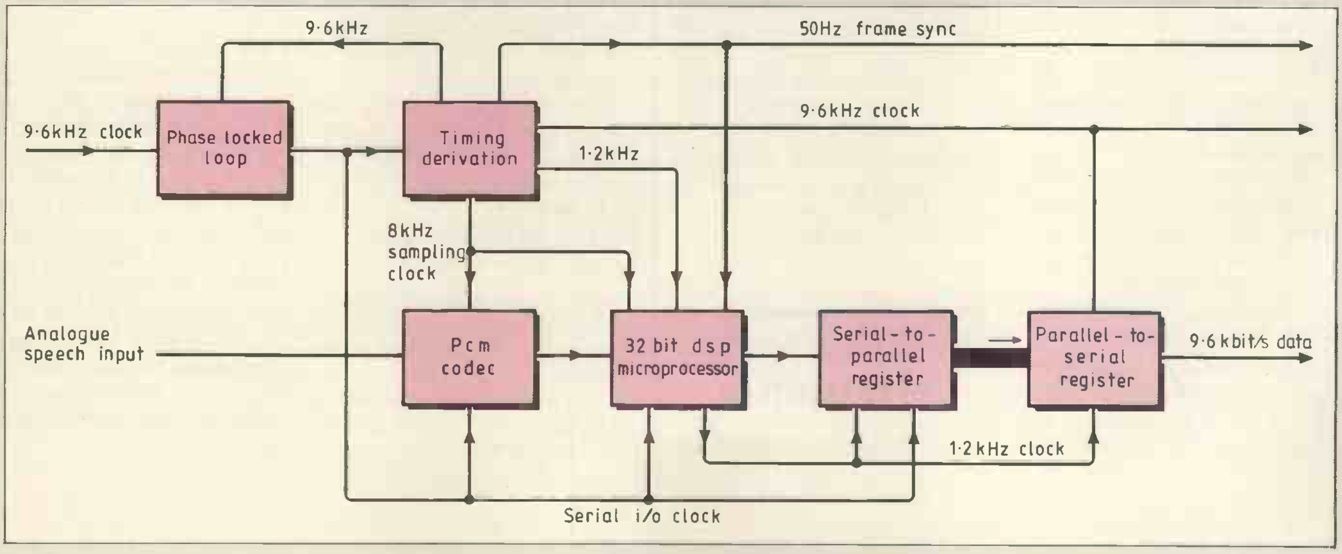
Skyphone speech encoding

Passengers on certain British Airways transatlantic flights are now able to make direct-dialled telephone calls to anywhere in the world. British Telecom International is running a trial service with its Skyphone aeronautical satellite system which provides public telecommunications for airline travellers. This follows from Inmarsat's 1985 decision to offer aeronautical mobile satcom services through its space segment generally (see July 1987 issue, p. 737). In this case the BTI trial service is using the Marecs B2 geostationary comsat over the Atlantic Ocean and an Earth terminal in the UK, at BTI's Goonhilly station, Cornwall, which links with the international public telephone network.

Two British Airways Boeing 747 airliners have been fitted with the necessary mobile equipment. Each aircraft can provide two simultaneous telephone conversations through international direct dialling. As reported earlier, the voice signals are digitally encoded to give a data rate of 9.6kbit/s. At a recent IEE conference, Satellite Systems for Mobile Communications and Navigation, three speakers from BT's research laboratories, I. Boyd, C.B. Southcott and D.P. Crowe, described the codec they have developed for this low bit-rate – low because of the limited satellite power available. This codec design is one of several, originating from different parts of the world, that are now being considered by airlines for eventual permanent services.

To achieve the required spectral efficiency with the low bit-rate the developers chose a linear predictive coding algorithm for the codec. The encoding process

Speech encoding hardware used by BTI for the codec in its Skyphone system, providing public telecommunications from airliners.



involves splitting the incoming speech into frames of 10ms-20ms duration to derive short-term and long-term prediction parameters, and also an 'analysis-by-synthesis' process to obtain the pulse positions and amplitudes. A short-term predictor models short-term correlations in the speech signal, while a long-term predictor takes advantage of long-term correlations in speech arising primarily from pitch relationships. Non-linear equations have to be solved, so the process is very complicated.

For this algorithm the required digital signal processing is done on a 32-bit dsp microprocessor, the WE DSP32. This has four 40-bit accumulators, on-chip rom and ram, off-chip memory expansion to 56kbytes and an instruction cycle of 160ns. The diagram shows how the microprocessor is used in the encoder hardware. A pcm codec samples the analogue speech waveform at a rate of 8kHz and generates an eight-bit encoded sample every 125µs. These samples are clocked out serially to the microprocessor at a rate of 1536kHz. A 50Hz clock signal is used for frame synchronization.

At the output are two eight-bit registers, serial-to-parallel and parallel-to-serial. These are controlled by a 1.2kHz clock (one eighth of the 9.6kHz bit rate) in such a way that each burst of eight data bits at 1536kHz is converted into a continuous data stream at 9.6 kbit/s.

Subsequently this digitized voice signal is multiplexed with the dialling data – a dual-tone multi-frequency signal – to produce a data stream at 10.368kbit/s. This data stream then passes through forward error correction and a process called interleaving to combat multi-path fading. A result of the error correction is to double the data rate and the final output is a 21kbit/s digital signal. This modulates the rf carrier by a form of quadrature phase-shift keying known as 'aviation qpsk'.

Eventually the Atlantic service will be supplemented to give world-wide coverage, using two more Inmarsat comsats, over the Indian and Pacific oceans, and two more Earth stations, in Norway and Singapore.

Gso allotment plan

Equitable access to the geostationary orbit was the guiding principle of the ITU space conference WARC ORB-88 recently held in Geneva. This principle for satellite communications was actually laid down in what amounted to the first session of the conference, ORB-85, held three years ago (see report by David Withers in December 1985 issue, pp. 65-66).

The main task of ORB-88 was to translate this general principle into specific allotments in the Fixed Satellite Service (FSS) for all member countries of the ITU. It did not, however, deal with the whole of the FSS allocations but only with those additional bits of spectrum made available at the general frequency allocation conference WARC 1979. These extension bands, as they are known, amount to a total 800MHz of spectrum space. Of this, 300MHz is in the C band (6.725-7.025GHz for uplinks; 4.5-4.8GHz for downlinks) and 500MHz in the Ku band (12.75-13.25GHz for uplinks; 10.7-10.95GHz and 11.2-11.45GHz for downlinks).

A report on how the FSS allotments were worked out, and a few other space decisions made at Geneva, was given at an IEE meeting by Dr Keith Shotton, director of radio technology at the DTI's Radiocommunication Division. It emerged that equitable access does not in fact mean equal amounts for everyone. As in George Orwell's *Animal Farm*, some are more equal than others. This is currently justified by the argument that some countries – notably the rich, industrialized ones – have a greater requirement for satellite communications than others such as the relatively poor Third World countries. And indeed this inequality is already a fact of life in the geostationary orbit. In the early days after the 1971 space WARC the principle of FSS allotment was simply first-come first-served, and naturally the advanced industrialized nations tended to get in first.

This legacy of earlier methods is apparent in even the WARC 1979 extension bands, which already contain about 26 C-band satcom systems and 28 Ku-band systems (including the Astra direct broadcasting satellite). Dr Shotton explained that ORB-88 dealt with this situation by accepting that the existing satcom systems would have to stay – they were given another 20 years' tenancy – and then planning compatible allotments in the remaining orbital and frequency space.

What 'equitable access' really comes down to is that every member of the ITU – virtually every country in the world – is guaranteed at least one orbital slot, with access to the whole 800MHz in the C and Ku bands and a protection ratio against interference from other users (carrier power/aggregate interference power) of 26dB.

To allow flexibility in planning, each slot is treated as a nominal 'pre-determined orbital arc' with a possible range of ±10° at the system pre-design stage, ±5° at the design stage and zero degrees at the operation stage. Technical parameters used in the planning included carrier-to-noise ratios of 23dB for uplinks, 17dB for downlinks and 16dB overall in rain faded conditions. Minimum beam sizes are 1.6° for C band and 0.8° for Ku band, while the satellite antenna beam pointing accuracy must be ±0.1°.

As an example, the small African country of Chad now has a nominal orbital location of 10.5°W, with the frequency and protection guarantees mentioned above. Chad is interesting as being one of several tens of countries which did not even put in requests for allotments at the conference. Here, in the absence of applications, the allotments were made by the International Frequency Regulation Board. The British delegation came away with three orbital slots, and Dr Shotton said that his outcome was very satisfactory for the UK.

It was also decided that groups of countries should be able to club together to set up sub-regional rather than national satcom systems. Here the national allotments will be suspended for the lifetime of the sub-regional scheme but still protected for later eventualities.

As for direct broadcasting from the gso, Dr Shotton said that the main task of the ORB-88 conference was to establish a feeder link plan for the BSS in ITU Regions 1 and 3. This was mainly in the 17.3-18.1GHz band. It differed from the corresponding Region 2 dbs feeder plan in that the rf power in these uplinks – which has to be increased to compensate for rain fading – was now controlled to be kept below certain limits. The maximum permitted power increase – as necessary in very heavy rain – was set at 10dB. Digital sound broadcasting was referred to a future conference, and there was no progress in trying to find a world-wide allocation for wideband high-definition television systems (see September 1988 issue, pp. 846-847).

• Frequency allocations to the mobile satellite service have been modified to provide spectrum specifically for the new land mobile applications just beginning to appear (November 1988 issue, p. 1095). Mike Goddard, a colleague of Dr Shotton at the DTI, gave details at an IEE conference on mobile comsat systems (see item elsewhere). He said that primary L-band allocations had been made for these land mobile systems at a WARC in 1987. Two 3MHz bands, uplink and downlink, were now shared with the corresponding maritime mobile satellite service bands, while the 4MHz bands, uplink and downlink, were exclusive, having been taken from spectrum previously allocated to the aeronautical mobile satellite service. These changes would come into force in October 1989.

Satellite Systems was written by Tom Ivall.

Handling matrices

In spite of the jargon, they can make life much simpler

JOULES WATT

Some time ago, I had a word or two with you about transistor parameters[1] and their use in calculating the properties of linear amplifiers. The form of the equations we developed there gave rise to a convenient notation for the coefficients of the terms. You might remember that I quite nonchalantly introduced a *matrix*, or tabular array for them.

These matrices, or two-dimensional arrays of numbers form a common part of elementary mathematics teaching in circles where people talk about "modern maths". But I still meet older engineers, some of them senior ones, who say, in connection with matrices, "between you and me, I never *really* grasped their use. I muddle through of course, but you can imagine the difficulties with youngsters coming to ask me how to use them."

THE "BLACK BOX" AGAIN

Recapping on the earlier work, the two linear equations describing the two-port in **Fig. 1** leads us straight into matrix notation, which I suppose is the way people in electronics gain a nodding aquaintance with it. We call the **Y** array

$$\begin{bmatrix} y_i & y_r \\ y_f & y_o \end{bmatrix}$$

a 2 × 2 square matrix. The **I** matrix on the left-hand side of the equation and the **V** matrix on the right yield examples of *column matrices*, in this case of order 2 × 1. Some authors write

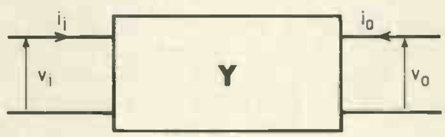
$$[i]=[y][v]$$

as a shorthand for such matrix equations. Others use bold capitals such as

$$\mathbf{I=YV}$$

as I do here. Both contractions suppress the order number of the matrices, which you have to state separately. The above example shows the scheme in which everyone has agreed to write down the order number; that is, if you see m rows and n columns, then the matrix is of order "m × n" or is an "m by n" array.

The first matrix operation arises by interpreting the right-hand side as a *product*. The "rule" for this appears to be 'move across ... dive down'. In other words, take each element along the top row of the first matrix and multiply by the corresponding one going down the first column of the second and add up all the products. You then repeat this pattern for all the other combinations. What happens, you may ask, if you run out of elements in a row or column? The answer is this cannot happen, since the numbers must



$$\begin{bmatrix} i_i \\ i_o \end{bmatrix} = \begin{bmatrix} y_i & y_r \\ y_f & y_o \end{bmatrix} \begin{bmatrix} v_i \\ v_o \end{bmatrix}$$

$$\mathbf{I} \quad = \quad \mathbf{Y} \quad \mathbf{V}$$

Fig.1. This standard two-port shows the relation between the y parameters and the input and output currents and voltages.

match every time to be valid. When they match, we call the matrices *conformable*.

On this argument, swapping (or, put politely, "commuting") the two matrices in the "I" equation above, yields

$$\begin{bmatrix} v_1 \\ v_o \end{bmatrix} \begin{bmatrix} y_i & y_r \\ y_f & y_o \end{bmatrix}$$

which has no meaning, because written in this order the matrices do not conform, which makes us immediately suspicious of glibly commuting matrix factors in any way at all. Are they commutable, even when conformable?

Try these to see:

$$\underset{\mathrm{A}}{\begin{bmatrix} 1 & 2 \\ -1 & 3 \end{bmatrix}} \underset{\mathrm{B}}{\begin{bmatrix} 3 & 5 \\ 1 & 3 \end{bmatrix}} \underset{=}{=} \underset{\mathrm{C}}{\begin{bmatrix} 2 & 11 \\ 0 & 4 \end{bmatrix}}$$

$$\underset{\mathrm{B}}{\begin{bmatrix} 3 & 5 \\ 1 & 3 \end{bmatrix}} \underset{\mathrm{A}}{\begin{bmatrix} 1 & 2 \\ -1 & 3 \end{bmatrix}} \underset{=}{=} \underset{\mathrm{D}}{\begin{bmatrix} -2 & 21 \\ -2 & 11 \end{bmatrix}}$$

D is an entirely different matrix to **C**, therefore **AB** is not equal to **BA**. So matrix algebra appears non-commutative, but you came across the same kind of result with vector algebra[2]. On the other hand, matrices do sum easily.

$$\begin{bmatrix} 6 & 1 \\ 4 & 3 \end{bmatrix} + \begin{bmatrix} 8 & 4 \\ 2 & 3 \end{bmatrix} = \begin{bmatrix} 14 & 5 \\ 6 & 6 \end{bmatrix}$$

Corresponding elements add. The matrices must have the same order in a sum.

These rules for the sums and products show why we chose various parameters for shunt, series or cascade connections of two-port networks: choosing the appropriate circuit parameters simplifies the matrix operations in the analysis. You will find that square matrices commonly turn up in applications, particularly in circuit analysis but, as we have seen, non-square m by n matrices do exist. Conformability means that an m by n array requires an n by p to follow in the product, the result being an m by p matrix. We say the first matrix *premultiplies* the second. Alternatively you could say the second *postmultiplies* the first.

DETERMINANTS AND MATRICES

That other array, the *determinant*, really has an independent existence. For example, a determinant must be square, i.e. have equal numbers of columns and rows. A whole set of rules and operations for determinants exist, which you might profitably look up[3]. Unlike a matrix, a determinant can be multiplied out. For example,

$$\begin{vmatrix} 6 & 1 \\ 4 & 3 \end{vmatrix} = 6\times3-4\times1=14$$

You can multiply out determinants of higher order by developing the result via *cofactors*, as they are called. The cofactor of an element is the lower order array remaining when you cross out the row and column intersecting at the element in question.

SQUARE MATRICES

I already mentioned that square matrices turn up more often in circuit applications than other types.

In spite of authors warning readers that "matrices and determinants are different: a determinant has a value, a matrix does not", some of them proceed to talk about "the determinant of the square matrix A ..." Therefore, although they *are* different, you can associate a determinant with a matrix. Of course, determinants, being square, cannot exist at all for an m by n matrix, where m ≠ n. For square types, the determinant yields various pieces of information about patterns in the elements of the matrix.

Other symmetries and patterns exist for square matrices, but not for general m by n types. For example, a *diagonal matrix* has finite elements in the top left, down the diagonal to bottom right positions, but zero everywhere else. Generally speaking, this line of elements forms the *principal* or *leading* diagonal of any square matrix. You probably know that all "algebras" have a *null* element, corresponding to zero in ordinary numbers, and a *unity* element, corresponding to 1. The unit matrix **I** has all ones in the leading diagonal, i.e.

$$\mathbf{I}=\begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}$$

There must be any number of 'unit matrices', according to the order, but they are all square. Some people write I_n with n indicating the order. The null, or zero matrix (again of various orders) has all elements equal to zero. We write it as **0**. These two matrices are the only ones to commute in multiplication with suitably conformable general matrices.

We can go on to all sorts of special definitions. For example, returning to the general m × n matrix for a moment, the *transpose* of A, written as A^t, is the n × m matrix formed by interchanging its rows and columns. Of course, square matrices have transposes too. In some of these, you may come across matrices equal to their transposes. For this, the elements a_{ij} in an n^{th} order square matrix must relate according to $a_{ij} = a_{ji}$. The i and j correspond to the row and column position numbers, both running from 1 to n of course. Such matrices have the property of being *symmetrical*.

You only require a glance at the kind of quantities that arise in most of our work to see that complex numbers figure prominently. Now, a complex number $z = r + jx$ has a *conjugate* $z^* = r - jx$. Extended to complex elements in a matrix array, if you take all the conjugates, you get the conjugate of the whole matrix. **Z** has the conjugate $\mathbf{Z}^*$. This definition yields a way to see whether a matrix is real or imaginary: if $\mathbf{Z} = \mathbf{Z}^*$ then the elements are wholly real, but if $\mathbf{Z} = -\mathbf{Z}^*$, the elements are purely imaginary. The transpose of a conjugate matrix is called the *associate* of the matrix.

Finally, in my selection of properties, if a matrix equals its associate, that i, if $A = A^{*t}$, then we say the matrix is *hermitian* (after Charles Hermite, 1822 to 1905). The *skew-hermitian* matrix is the negative of the transpose of the conjugate, i.e. $A = -A^{*t}$.

OPERATIONS WITH MATRICES

The need for conformability in matrix multiplication, a non-commutative operation in any case as we have seen, would appear to make the algebra restrictive. Adding the fact that matrices only sum when of the same order might confirm this suspicion, but conformable matrices do obey the *associative law*.

$$\mathbf{A(BC) = (AB)C}$$

Again, with suitable conformability, multiplication *distributes* over addition, that is

$$\mathbf{A(B + C) = AB + AC}$$

Dare I say it, "I leave the proofs to the reader!"

However, other restrictions, like limiting the discussion to square matrices, expand the operational possibilities again. Square matrices of the same order, although not necessarily commutative, do exhibit conformability both ways and they sum easily. And a square matrix obviously shows conformability with itself. It also commutes with itself, so that you can define a squaring or raising to a power operation,

$$\mathbf{AA} = \mathbf{A}^2$$

and in general

$$\mathbf{A} \ldots \mathbf{A} = \mathbf{A}^r$$

You will find another rather surprising departure from the norm we know so well in "ordinary" algebra. We know that if two numbers multiply to zero, then either one or the other must itself be zero. But in matrix algebra,

$$\begin{bmatrix} 6 & 4 & 2 \\ 9 & 6 & 3 \\ -3 & -2 & -1 \end{bmatrix} \begin{bmatrix} 0 & 1 & -2 \\ -1 & 0 & 3 \\ 2 & -3 & 0 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

which means that in general $\mathbf{AB} = \mathbf{0}$ does not imply that either $\mathbf{A} = \mathbf{0}$ or $\mathbf{B} = \mathbf{0}$.

Here is a typically interesting matrix "theorem", in which I have insufficient space to prove, but you might like to try.

> 'the transpose of the product of two conformable matrices is equal to the product of their transposes, taken in reverse order'.

$$\mathbf{(AB)^t = B^tA^t}$$

By extension, this applies to a whole string of producted matrices.

If you have managed a tea break at this point, I might get away with suggesting a little more to come! We ought, at least, to mention the meanings of the *adjoint* and the *inverse*, as applied to the ubiquitous square matrices.

Everyone becomes familiar with ordinary reciprocals, defined as

$$x^{-1} = \frac{1}{x}$$

when x is not zero. This has the property $xx^{-1} = x^{-1}x = 1$. Also, division is done away with after learning about inverses or reciprocals. Notice that only multiplication survives. You saw how multiplication of matrices arose but, as yet, I have made no attempt at defining division. Does a (square) matrix have an *inverse* (or reciprocal)? If it does, then the redundant division, no longer required as such, can be done by multiplication.

First look at determinants again. If the determinant of a square matrix differs from zero, we can divide by it. If $|a_{aj}|$ does equal zero, then the matrix **A** is *singular*. The *adjoint* of a square matrix has the following definition. The square matrix **A** has a determinant $|a_{ij}|$. If A_{ij} is the cofactor of the element a_{ij} in this determinant, then the matrix

$$A_{ji} = A_{ij}^{\ t}$$

which is the transpose of A_{ij}, has the grand title, *adjoint* of A, often written as adjA. You probably had to read that a couple of times, so an example might help. Suppose we have the matrix

$$A = \begin{bmatrix} 1 & 2 & 4 \\ -1 & 0 & 3 \\ 3 & 1 & -2 \end{bmatrix}$$

Then $$|a_{ij}| = \begin{vmatrix} 1 & 2 & 4 \\ -1 & 0 & 3 \\ 3 & 1 & -2 \end{vmatrix} = 7$$

From the definition of adjoint, going across the first row the cofactor of the 1 is

$$\begin{vmatrix} 0 & 3 \\ 1 & -2 \end{vmatrix}$$

that of the 2 is

$$-\begin{vmatrix} -1 & 3 \\ 3 & -2 \end{vmatrix}$$

and so on. This means that the adjoint of A is the transpose of

$$\begin{bmatrix} \begin{vmatrix} 0 & 3 \\ 1 & -2 \end{vmatrix} & -\begin{vmatrix} -1 & 3 \\ 3 & -2 \end{vmatrix} & \begin{vmatrix} -1 & 0 \\ 3 & 1 \end{vmatrix} \\ -\begin{vmatrix} 2 & 4 \\ 1 & -2 \end{vmatrix} & \begin{vmatrix} 4 & 4 \\ 3 & -2 \end{vmatrix} & -\begin{vmatrix} 1 & 2 \\ 3 & 1 \end{vmatrix} \\ \begin{vmatrix} 2 & 4 \\ 0 & 3 \end{vmatrix} & -\begin{vmatrix} 1 & 4 \\ -1 & 3 \end{vmatrix} & \begin{vmatrix} 1 & 2 \\ -1 & 0 \end{vmatrix} \end{bmatrix}$$

(Notice the alternating negative signs).

Some cryptologists have sent secret messages by encoding matrix elements with the sensitive information, then employing adjoints and so on to make it hard to decode. ("I'm not surprised", did I hear you say?)

We have yet to look at the *inverse*. Fortunately that causes no further problems, since

$$A^{-1} = \frac{\text{adj}A}{|a_{ij}|}$$

Although all square matrices possess adjoints, only non-singular matrices have reciprocals, because the determinant in the denominator must not go to zero.

USES

Now that we have the inverse, or reciprocal, we can do useful work at last. Non-singular matrices and their inverses multiply, so that

$$\mathbf{AA^{-1} = A^{-1}A = 1}$$

and it follows that, for any square matrix,

$$\mathbf{adjAA = AadjA = |a_{ij}|1}.$$

From our example above,

$$A^{-1} = 1/7 \begin{bmatrix} -3 & 8 & 6 \\ 7 & -14 & -7 \\ -1 & 5 & 2 \end{bmatrix}$$

so that

$$A^{-1}A = 1/7 \begin{bmatrix} -3 & 8 & 6 \\ 7 & -14 & -7 \\ -1 & 5 & 2 \end{bmatrix} \begin{bmatrix} 1 & 2 & 4 \\ -1 & 0 & 3 \\ 3 & 1 & -2 \end{bmatrix}$$

$$= 1/7 \begin{bmatrix} 7 & 0 & 0 \\ 0 & 7 & 0 \\ 0 & 0 & 7 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

From all this, we find that in the matrix equations

$$\mathbf{Ax = I \text{ or } xA = 1}$$

x will equal $\mathbf{A}^{-1}$ and this is the solution.

Stronger than this, but following from it, we have the set of solutions in which the n × n matrix A, the n × m matrix **B**, the m × n matrix **C** and the matrix **x** relate according to,

$$\mathbf{Ax = B}, \text{ whence the solution is } \mathbf{x = A^{-1}}$$

or

$$\mathbf{xA = C}, \text{ again the solution is } \mathbf{x = CA^{-1}}$$

If you make **B** the column matrix

$$y = \begin{bmatrix} y_1 \\ y_2 \\ \vdots \\ y_n \end{bmatrix}$$

then $\mathbf{Ax = y}$ whose solution is $\mathbf{x = A^{-1}y}$ (**A** non-singular), relates the variables in a set of n linear equations in x and y. You can solve the set of linear equations this way, by reading off the elements in the column matrix for x on the right. Considering the patterns in the matrices, before even attempting the problem, tells you whether a solution exists at all – or whether a very poor result might be obtained (the so-called "ill-conditioned" result). This discussion shows the usefulness of matrices when discussing *linear transformations*. In fact, matrices turned up in the work of the English mathematician Arthur Cayley (1821 to 1895) during his work on linear transformations.

The use of computers in handling matrix operations has the edge because of the amount of "number crunching" required. Pascal has many built-in, structured, matrix functions, as does early ('mainframe') Basic. But unfortunately most of the people writing microcomputer versions saw fit to drop the MAT functions. Recently I had a brief search for a cheap version of Basic suitable for popular machines, but BBC Basic, Sinclair Basic and GWBasic Basica for IBM all fail to turn up such functions. If any readers know of a version with MAT, I would appreciate a note.

But even with computing power at your disposal, surprises turn up if you have to deal with a large number of equations and unknowns. For example, if your computer can handle 10 000 multiplications per second, then for developing a 5th order inversion (determining the determinant) would take 5! computations (0.01 seconds). A 10th order computation (10 unknowns) requires 10! computations (5 minutes). A 12th order requires 10 hours; the 14th order, 3 months and the 16th order would take 60 years ... Therefore a direct frontal attack rapidly becomes hopeless, and short cuts greatly reduce the time. One such you will find goes under the title *Gauss' elimination method*[4].

BACK TO CIRCUITS

I have already pointed out[1] that by choosing the appropriate set of parameters (z, y, h and so on) for networks, interconnection of the two-port boxes became easy. The elements of the square 2 × 2 matrices either added, or in a couple of cases, they multiplied according to the rules. In practice, the most common of these multiplication cases arises from using the A B parameters, or as some people call them, the *chain parameters*.

THE INDEFINITE ADMITTANCE MATRIX

Before looking at the chain parameters and matrices, a glance at an actual circuit shows how a more generalized matrix can help in understanding its properties. In the case of a transistor, the various configurations, such as the CE, CB or CC, depend on which terminal you choose as the common one. Alternatively, if you drive all terminals at once, the transistor looks like a three-port network. You can imagine this network possessing an external reference terminal r; see **Fig 2**.

Notice that the ys in the 3 × 3 matrix depend on one another, in the sense that if you know the conditions at two of the ports, then you know those at the third also. This

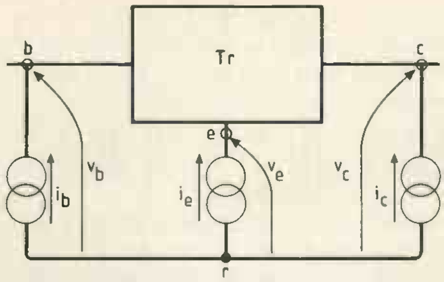


Fig.2. If all three terminals of a transistor receive current inputs, then the 3 × 3 matrix relating all the currents and voltages is known as the *generalized admittance matrix*.

property makes the *indefinite admittance matrix* we are talking about useful as an even more concise way of arranging all the y parameters corresponding to the various configurations. More than that, if you know the four parameters of one configuration, then you effectively know all the others, because the dependence means that the sum of the elements of any row or any column in the matrix equate to zero.

You can easily see this from Kirchhoff's Law,

$$i_b + i_e + i_c = 0$$

Since the matrix equation is valid for any small voltage signals, let v_b be finite but $v_e = v_c = 0$,

then $\quad i_b = y_{11}v_b,\ i_e = y_{21}v_b,\ i_c = y_{31}v_b$

by multiplying out.
Substitute in the above equation for the sum of currents,

$$\therefore \qquad (y_{11}+y_{21}+y_{31})v_b=0$$

But we assumed v_b had a finite value, so it is the factor

$$y_{11} + y_{21} + y_{31} = 0$$

You can write down the sum of the other columns in the same way. For the rows, set all the voltages equal. This means that no p.d. exists and therefore no currents can flow, so that

$$i_b = i_e = i_c = 0$$

Take the first row of the matrix equation and multiply it out,

$$\therefore \qquad i_b=y_{11}v_b+y_{12}v_e+y_{13}v_c.$$

But we have $i_b=0$ and $v_b=v_e=v_c=v_o$, say,

$$\therefore \qquad 0=(y_{11}+y_{12}+y_{13})v_o.$$

We did not set v_o equal to zero, so again the factor

$$y_{11} + y_{12} + y_{13} = 0.$$

Similarly you can write down results for the other rows. These results indicate that if you know any four parameters, with not more than two in any one row or column, then you can find the other five.

For example, if you know that the common-emitter parameters are

$$y_{ie} = (2.5 + 1.5j)10^{-3}$$
$$y_{re} = -(1 + j25)10^{-6}$$
$$y_{fe} = (30 - j4)10^{-3}$$
$$y_{oe} = (25 + j75)10^{-6}$$

then you might be asked what the CB and the CC y parameters are.

Write down the generalized admittance matrix, with the "emitter" row and column blank, (because in the CE stage 0 appears on the emitter as common reference). Place the four known parameters into the correct positions in the matrix – at the four corners in the present example. Sum the rows and columns to zero thus yielding the other parameters. **Figure 3** sums it all up.

THE COLPITTS OSCILLATOR AGAIN

In discussing "equivalent circuits" a while ago[5], I derived the conditions for maintenance of oscillation and the frequency in a Colpitts circuit. You should find the chain matrix approach to solving this problem just as interesting. It further illustrates the value of matrices, and you can compare the methods as I have applied them to the Colpitts. You can also apply a similar chain matrix approach to other oscillator configurations.
Consider,

$$v_1 = Av_2 - Bi_2$$
$$i_1 = Cv_2 - Di_2$$

You can also rewrite these (rather trivially!) as,

$$v_1 = Av_2 + B(-i_2)$$
$$i_1 = Cv_2 + D(-i_2)$$

so that in matrix form,

$$\begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} v_2 \\ -i_2 \end{bmatrix}$$

Some people find that unexpected negative sign on i_2 awkward. But we have all agreed to

$$\begin{array}{cccc} & \begin{array}{ccc} b & e & c \end{array} & & \\ \begin{bmatrix} i_b \\ i_e \\ i_c \end{bmatrix} = & \begin{bmatrix} y_{ie} & y_{rc} & y_{re} \\ y_{fc} & y_{ib} & y_{rb} \\ y_{fe} & y_{fb} & y_{oe} \end{bmatrix} & \begin{bmatrix} v_b \\ v_e \\ v_c \end{bmatrix} & \begin{array}{c} \text{— b} \\ \text{— e} \\ \text{— c} \end{array} \end{array}$$

$$\therefore \mathbf{Y} = \left[\begin{array}{c|c} (2{\cdot}5 + j1{\cdot}5)\times10^{-3} & -(1+j25)\times10^{-6} \\ \hline (30 - j4)\times10^{-3} & (25+j75)\times10^{-6} \end{array}\right]$$

Fill in the missing values :-

$$\mathbf{Y} = \begin{bmatrix} (2{\cdot}5+j1{\cdot}5)\times10^{-3} & -(2{\cdot}5+j1{\cdot}48)\times10^{-3} & -(1+j25)\times10^{-6} \\ -(32{\cdot}5-j2{\cdot}5)\times10^{-3} & (32{\cdot}52-j2{\cdot}49)\times10^{-3} & (24+j50)\times10^{-6} \\ (30-j4)\times10^{-3} & -(30{\cdot}03-j3{\cdot}93)\times10^{-3} & (25+j75)\times10^{-6} \end{bmatrix}$$

Fig.3. The procedure illustrated here shows that, given four parameters out of the nine in the generalized admittance matrix, the other five turn up quite naturally by adding rows and columns and equating to zero.

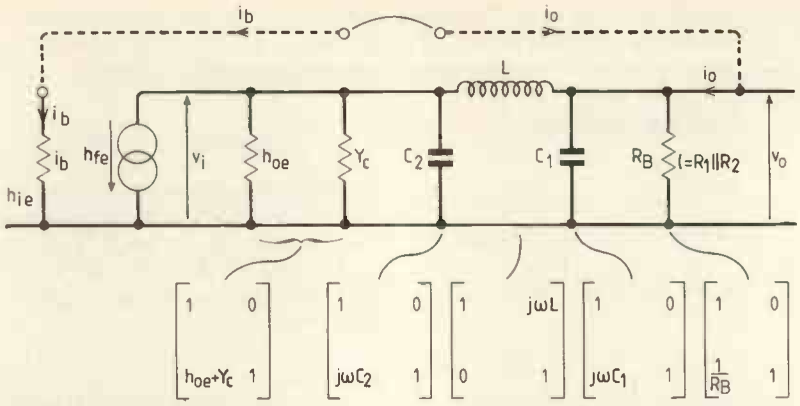
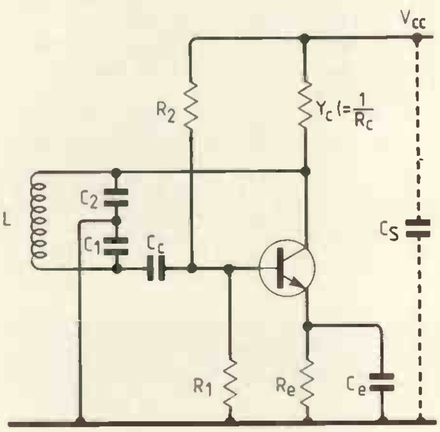


Fig.4. This standard Colpitts oscillator circuit, exactly the same as that in ref. 5, lends itself well to ABCD matrix parameter analysis.



use it so that the "inward" current convention on all our two port network boxes doesn't get violated. Yet because the output current of a leading network in the chain becomes the input current of a trailing one, you will find the change in current directions conveniently taken up in this one sign change – however long the chain is.

Now for the Colpitts. Take a look at **Fig 4**, which I have chosen to be the same as that in **Fig. 3** of ref. 5. Draw the equivalent circuit, ending up with the network of **Fig. 5**. Because each output current equals the input current to the next stage, the chain of matrices multiplying together in order,

$$\begin{bmatrix} v_i \\ -h_{fe}i_b \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ h_{oe}+Y_c & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C_1 & 1 \end{bmatrix} \begin{bmatrix} 1 & j\omega L \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C_2 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{R_B} & 1 \end{bmatrix} \begin{bmatrix} v_o \\ -i_o \end{bmatrix}$$

You might remember that the Barkhausen condition says the loop gain (current gain in this case) must equal 1 for oscillations (just) to be maintained. Therefore the gain

$$|A_i| = \frac{i_o}{i_b} = 1;\ \text{also}\ -i_o = i_b\ \text{and}\ v_o = i_o h_{ie}$$

Now multiply out the chain matrices,

$$\begin{bmatrix} v_i \\ -i_b h_{fe} \end{bmatrix} \begin{bmatrix} 1-\omega^2 LC_1 + \frac{j\omega L}{R_B} & j\omega L \\ (h_{oe}+Y_c)(1-\omega^2 LC_1) + j\omega C_2 + j\omega C_1(1-\omega^2 LC_2) \times \frac{j\omega L}{R_B}(h_{oe}+Y_c) + \frac{1-\omega^2 LC_2}{R_B} & j\omega L(h_{oe}+Y_c) + 1 - \omega^2 LC_2 \end{bmatrix} \begin{bmatrix} -i_b h_{fe} \\ i_b \end{bmatrix}$$

Choose the equation for $-i_b h_{fe}$

$$-i_b h_{fe} = \left\{ (h_{oe}+Y_c)(1-\omega^2 LC_1) + j\omega C_2 + j\omega C_1(1-\omega^2 LC_2) + \frac{j\omega L}{R_B}(h_{oe}+Y_c) + \frac{1-\omega^2 LC_2}{R_B} \right\} i_b h_{ie} + \{ j\omega L(h_{oe}+Y_c) + 1 - \omega^2 LC_2 \} i_b$$

Fig.5. The Colpitts equivalent circuit especially suited to ABCD matrix interpretation. Each component has its chain matrix representation as shown. The overall matrix is simply the product of these.

Cancel through the base current. Equate the imaginary terms to zero. By doing this you obtain the frequency condition,

$$C_2 h_{ie} + C_1 h_{ie} - \omega^2 LC_1C_2 h_{ie} + \frac{h_{ie}L}{R_B}(h_{oe}+Y_c) + L(h_{oe}+Y_c) = 0$$

Assume now $1/R_B$ and h_{oe} so small that you can neglect the terms they are in;

$$\therefore \quad \omega^2 = \frac{C_1+C_2}{LC_1C_2} + \frac{Y_c}{C_1C_2h_{ie}}$$

Often we can neglect the second term, especially as Y_c, often replaced with a radio frequency choke, means $B_{choke} \rightarrow 0$. You should make the C/L in the tuned circuit large, the circuit then becoming a "high-C Colpitts". Gouriet and Clapp modified the circuit further so that the effective C/L ratio was greater still.

The next step equates the reals, to give the Maintenance Condition. You can eliminate the ω^2 using the simplified expression for frequency just obtained,

$$\therefore \quad h_{fe} \geq \frac{C_2}{C_1}\left(1+\frac{h_{ie}}{R_B}\right) + \frac{C_1}{C_2}(h_{oe}+Y_c)h_{ie}$$

With approximations of the same order as before, you get the final result that $h_{fe} \geq C_2/C_1$ for oscillations to start and continue. If your inductor has a resistive component r, you can account for it as another matrix in the chain. Compare the final equations with those in the earlier article.[5]

Forms

When you continue studies of matrix methods to some depth, *forms* arise for consideration. This does not mean matrices are more bureaucratic than other mathematical techniques, but that two or three-number structures turn up with a particular *shape*.

For example, you might come across *quadratic forms* or *hermitian forms*[6]. I only have space for a quick illustration of the hermitian form as an example of "form use" in our subject. Remember the properties of Hermite's complex matrix and you will follow how such matrices arise in dealing with tests on a network concerning its passivity or activity.

In a *passive* network, the sum of all the small-signal power entering it ports is either zero (in the lossless case) or positive (the lossy case). If the sum results in a negative number, then more power is leaving the network than entering – we have an amplifier, or *active* network. The hermitian form gives us a convenient way of looking at this problem via the matrices.

Working with the y parameters yields the following result for a two-port; **Fig. 1**. The total average power P going into the two-port is,

$$\begin{aligned} P &= |v_1|\,|i_1|\cos\theta_1 + |v_2|\,|i_2|\cos\theta_2 \\ &= \mathrm{Re}\,v_1 i_1^* + \mathrm{Re}\,v_2 i_2^* \\ \text{or,} \quad &= \mathrm{Re}\,v_1^* i_1 + \mathrm{Re}\,v_2^* i_2. \end{aligned}$$

Therefore by a little imaginative re-writing,

$$P = \tfrac{1}{2}(v_1^* i_1 + v_1 i_1^*) + \tfrac{1}{2}(v_2^* i_2 + v_2 i_2^*).$$

A further slight re-arrangement gives,

$$P = -(v_1^* i_1 + v_2^* i_2) + -(i_1^* v_1 + i_2^* v_2).$$

Now you can write this in matrix form if you remember that

$$\mathbf{I} = \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}$$

and the transpose of $\mathbf{V}^*$ is $\mathbf{V}^{*t} = [v_1^*\ \ v_2^*]$,

so that

$$P = \tfrac{1}{2}\mathbf{V}^{*t}\mathbf{I} + \tfrac{1}{2}\mathbf{I}^{*t}\mathbf{V}.$$

Now bring in the fact we discussed earlier that if

$$\mathbf{I} = \mathbf{Y}\mathbf{V},\ \text{then}\ \mathbf{I}^{*t} = \mathbf{V}^{*t}\mathbf{Y}^{*t},$$

which means you can write the expression for P as

$$P = \tfrac{1}{2}\mathbf{V}^{*t}\mathbf{Y}\mathbf{V} + \tfrac{1}{2}\mathbf{V}^{*t}\mathbf{Y}^{*t}\mathbf{V}.$$

Take out the pre-factor matrix and the post-factor matrix, to get

$$P = \mathbf{V}^{*t}[\tfrac{1}{2}(\mathbf{Y}+\mathbf{Y}^{*t})]\mathbf{V} = \mathbf{V}^{*t}\mathbf{Y}_h\mathbf{V},$$

where $\mathbf{Y}_h$ is the hermitian matrix $\tfrac{1}{2}(\mathbf{Y}+\mathbf{Y}^{*t})$, possessing all the properties of the earlier discussion. We call this final result for P a *hermitian form*. You now have the conditions limiting the y parameters to either lossless or lossy passive networks, or else to active networks.

For example, if the y parameters have real and imaginary parts,

$$Y=\begin{bmatrix} g_i+jb_i & g_r+jb_r \\ g_f+jb_f & g_o+jb_o \end{bmatrix}$$

Then the conjugate is

$$Y^*=\begin{bmatrix} g_i-jb_i & g_r-jb_r \\ g_f-jb_f & g_o-jb_o \end{bmatrix}$$

Now transpose this

$$Y^{*t}=\begin{bmatrix} g_i-jb_i & g_f-jb_f \\ g_r-jb_r & g_o-jb_o \end{bmatrix}$$

By adding, we get the hermitian result,

$$Y_h=\tfrac{1}{2}(Y+Y^{*t})=\begin{bmatrix} g_i & \dfrac{y_r+y_f^*}{2} \\ \dfrac{y_f+y_r^*}{2} & g_o \end{bmatrix}$$

For the network to be passive, $P\geqslant 0$ for all V not equal to 0 and the mathematicians call this condition on the hermitian form, *positive-semidefinite*[7]. For this, Y_h must have a positive or zero determinant, together with non-negative principal minors.

This means that $g_i\geqslant 0$ and that

$$g_ig_o-\frac{y_r+y_f^*}{2}\cdot\frac{y_f+y_r^*}{2}\geqslant 0.$$

You can write the last equation either as,

$$g_ig_o+b_rb_f-\frac{|y_f+y_r|^2}{4}\geqslant 0.$$

or

$$g_ig_o-g_rg_f-\frac{|y_f-y_r|^2}{4}\geqslant 0.$$

(Try it, you will need your skills in handling complex conjugates . . .) Starting again, this time looking at the two-port the other way round gives $g_o\geqslant 0$.

If you find any one of these conditions violated, then the network is *active*. The above equations re-arranged look like this (at least the second one in the last pair does),

$$1-\frac{|y_f-y_r|^2}{4(g_ig_o-g_rg_f)}\geqslant 0$$

or $1-A\geqslant 0$ where A is the second term.

This if you find $g_i\geqslant 0$, $g_o\geqslant 0$ and $0\leqslant A\leqslant 1$, the network is passive. If $A>1$ the network is active. A measures the "amount" activity, as it were.

ECONOMY OF WRITING

The last section shows you a rather abstract piece of work, which could be done with everything written out in full. But the matrix symbol economy does say it all in a lot less space, although you do have to get familiar with the new terms.

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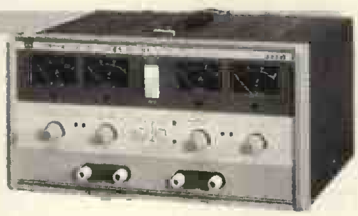

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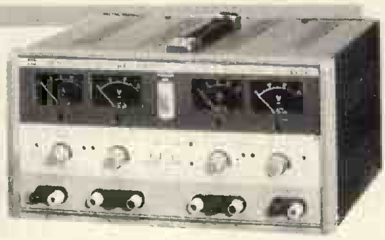

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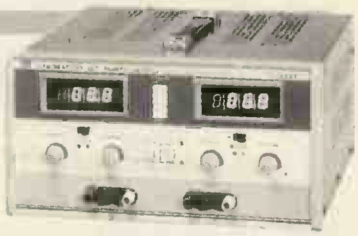

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Shannon, coding and spread spectrum

In the first article of this short series, the author outlines the basic properties of communications channels and examines the virtues of techniques such as frequency-hopping as a defence against jamming and interference.

L.C. WALTERS

In the late 1940s, Claude Shannon of Bell Telephone Laboratories published his now famous expression for the capacity of a communication channel, references 1 and 2 being perhaps the most widely known expositions.

In these classic papers he showed that it is theoretically possible to communicate up to a particular data rate (the channel capacity C) with an arbitrarily low error rate but that any attempt to exceed that data rate results in a total breakdown of communication.

This was a somewhat surprising result since it had previously been commonly believed that

- the presence of noise must always result in the possibility of errors, however rare;
- the error rate would merely increase continuously with decreasing signal-to-noise ratio.

Shannon also showed that in order to approach the limit C, coding of the information is required and that the time involved in coding and decoding increases asymptotically towards infinity as the data rate approaches C.

At first sight this may appear to be unhelpful from a practical viewpoint; but fortunately the essential time delays increase rapidly only when one gets quite close to the limit. Rates of C/3 to C/2 need involve delays which for most purposes are trivial, figures of milliseconds or less being quite feasible for many practical modern systems.

Shannon derived a precise mathematical expression for the capacity C, and since his derivation makes no assumptions about the nature of the system (e.g. its linearity or type of modulation or coding etc.), it is a truly fundamental limit which provides an invaluable yardstick against which to assess the performance of real systems.

His expression defined C in terms of the system bandwidth, the signal-to-noise ratio at the receiver, and a noise characteristic which he termed its entropy, since it is related to the degree of randomness of the noise. He also showed that the worst case occurs when the noise is gaussian and white (see boxes) over the receiver bandwidth, and that in this case the expression for C takes the simple form

$$C = W\log_2(1+S/N) \qquad (1)$$

Compressing speech or video bandwidths will always result in higher sensitivity to noise ...

where W is the bandwidth (hertz), S is the signal power at the receiver, N is the effective white gaussian noise power at the receiver and C is the capacity in bits per second.

It is important to realise that C is a limit on the *baud* rate, i.e. the information bit rate, and is not necessarily readily related to the transmission rate, though in many practical systems there is a simple fixed numerical relation between these.

Although in theory the capacity is slightly greater if the noise is not gaussian or not white, equation 1 is almost always used in practice for the following reasons:

(i) the gaussian noise case is easier to analyse!

(ii) in many instances the noise, at least at the input, *is* substantially white and gaussian.

(iii) if the noise is not white (i.e. is "coloured"), then it can usually be made white by suitable filtering, after which equation 1 will apply.

(iv) if the noise is not gaussian, the necessary information regarding its statistics if often neither available nor readily estimated and so cannot be exploited.

(v) if the noise is not gaussian and its statistics are known it is often quite difficult to take advantage of this knowledge.

(vi) if the noise is not gaussian and if its statistics are known and *have* been exploited, the resulting improvement in system performance is often very small.*

*Note that there are some significant exceptions which occur internally *within* systems, due for example to non-linear processing; but usually the *input* noise is substantially white and gaussian and processing converts this to calculable non-gaussian and/or non-white noise. However, equation 1 still applies to such cases if W, S and N are the values at the input.

Moreover, by restricting ourselves to the gaussian worst-case situation we avoid the problems otherwise involved in dealing with specific examples taken from a virtually infinite "library" of possible statistics. Henceforth, therefore, we shall ignore much of the subtlety of Shannon's work and assume that the capacity is always given by equation 1 (or that if preprocessing has been performed, as a result of which equation 1 applies, then the values of W, S and N employed are those subsequent to such processing).

From now on we shall assume that within the constraints of any given transmission system which attains an "error free" rate of kC baud, the factor k (<1) depends only on the type of system and that the dependence on bandwidth W and signal-to-noise ratio S/N remains precisely as given by equation 1, so that we may use this expression to assess the effect of changing these parameters. (If this were not so, then clearly, in changing W and/or S/N, one or other system has not been optimized).

... this does not mean that such techniques are not worth developing ...

Real systems are rarely wholly error-free but one may select, more or less arbitrarily, an acceptable error performance and use the corresponding values of W, S and N.

We therefore have the concept of a reference system which communicates with acceptable performance at a baud rate $R_0 = k_0C_0$ within a bandwidth W_0 at a signal-to-noise ratio $r_0 = S_0/N_0$, where, from equation (1), $C_0 = W_0\log_2(1+r_0)$. Thus,

$$R_0 = k_0W_0\log_2(1+r_0) \qquad (2)$$

and Shannon's expression implies that one can exchange signal/noise ratio for baud rate or bandwidth on a logarithmic basis. It is this logarithmic exchange potential which is exploited by all error-correction coding, and before considering this in a little more detail it is worth evaluating the maximum performance attainable on the basis of Shannon's theory.

THEORETICAL CODING GAIN

Suppose we have a reference system with parameters R_0, W_0 and r_0 related by equation 2. If we wish to change one or more of these parameters we can assess the effect by using this equation. One particularly interesting case is that in which we increase the bandwidth by a factor n, to give a new bandwidth W, say (i.e. $W_1=nW_0$), keeping the "performance" parameter R_0 unchanged. Then since we also assume k_0 to remain unchanged, this performance will be achieved at a different signal/noise ratio, r_1, say.

Thus $R_0=k_0nW_0\log_2(1+r_1)$, and since $n\log x = \log x^n$ this is equivalent to

$$R_0=k_0W_0\log_2(1+r_1)n \qquad (3)$$

From equations 2 and 3, $(1+r_1)^n=1+r_0$. Hence

$$r_1=(1+r_0)^{1/n}-1 \qquad (4)$$

Consequently, by expanding the bandwidth by a factor n one could achieve the same performance at a lower signal-to-noise ratio, an effect which may be viewed as giving a performance gain G_s, equal to the factor by which the threshold signal-to-noise ratio has been decreased. Thus,

$$G_s=r_0/r_1=r_0/[(1+r_0)^{1/n}-1] \qquad (5)$$

or in dB,

$$G_s(\mathrm{dB})=10[\log_{10}r_0-\log_{10}\{(1+r_0)^{1/n}-1\}] \qquad (6)$$

We shall show later that with good design a system whose bandwidth is expanded by a factor n should always permit a performance gain of n. Consequently the ratio of G_s to n gives the theoretical additional gain attainable by clever coding. We shall call this the theoretically attainable "coding gain", G_c. Hence,

$$G_c=G_s/n=r_0/n[(1+r_0)^{1/n}-1] \qquad (7)$$

$$\text{or } G_c(\mathrm{dB})=G_s(\mathrm{dB})-101\log_{10}n \qquad (8)$$

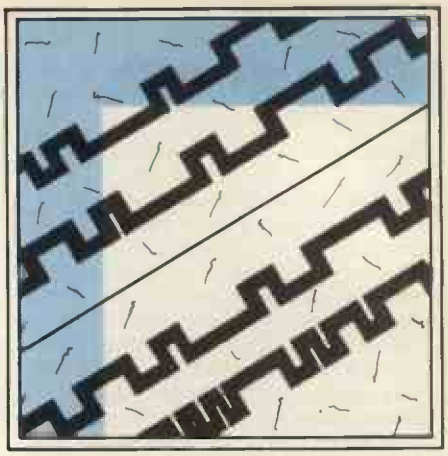
Note that G_c depends on the "initial" signal-to-noise ratio r_0 and on the bandwidth expansion factor n.

BANDWIDTH COMPRESSION

The case of bandwidth compression can be dealt with by letting n assume a value less than unity. Then we may put $1/n=m$ where m is greater than unity. By expanding $(1+r_0)^{1/n}=(1+r_0)^m$ in equation 5, it is easily seen that in this case G_s is less than unity or G_s(dB) is negative.

Hence bandwidth compression schemes essentially involve loss of performance for a given signal-to-noise ratio or, equivalently, demand higher signal/noise ratio for the same performance. Of course, it may be that the reduction in bandwidth results in a reduction in noise and so to greater signal-to-noise ratio. But this is already taken into account in the expression for G_s and does not affect the conclusion.

Thus techniques for compressing speech or video bandwidths will always result in higher sensitivity to noise and demand en-



One of the earliest attempts to counter interference by expanding bandwidth was the introduction of fm ...

GAUSSIAN NOISE

If we measure, over a fairly long period, the fraction of the time which a voltage waveform spends within a small voltage interval, it will usually be found that this fraction depends on where (as a voltage) the interval is set. Furthermore, if the interval is small enough this time will be proportional to its size. Thus the fractional time that a voltage waveform spends in the interval dv between values v and v+dv may be expressed as P(v)dv. P(v) is then called the amplitude distribution density function.

For example, for a triangular waveform confined within $-V_0$ and $+V_0$ an equal amount of time is spent within each voltage interval dv. Consequently its density function is constant between its voltage limits. Moreover, since the sum of all the time fractions must add up to unity, this constant must be such that the integral over all values is unity. Thus

$$P(v)=1/2V_0 \text{ for } -V_0<v<+V_0 \text{ and } =0 \text{ elsewhere.}$$

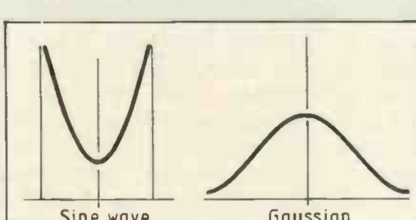
This in fact is a rare example for which P(v) appears not to vary with v; but the above shows that although the dependence is simple, it is still present because P(v) changes its value when v moves outside the range $-V_0$ to $+V_0$. If the waveform is a random waveform such as noise, or sometimes even if it is not, P(v) is called its probability density function or pdf. Strictly speaking it should be called its first-order probability density function since there is an infinity of higher-order density functions relating probabilities of lying within different small intervals at different times. We shall not consider these here.

In general P(v) is also a function of time; but, for a very important class of noise processes known as stationary processes, this is not so. Normal thermal noise generation in receivers is such a stationary process. (The noise output of a normal amplifier is stationary but if there is an operator who keeps varying its gain then the output is non-stationary. In simple terms stationarity means that the *statistics* do not change with time).

There is a powerful mathematical theorem called the central limit theorem which states that when a very large number of variables are added together, whatever their density functions and whether or not these are all the same, provided only that the variables are not precisely related, the density function of their sum tends to a gaussian function; that is, a function of the form

$$P(v)=(2\pi\sigma)^{-1/2}\exp[-(v-v_0)^2/2\sigma^2]$$

where v_0 is the mean or dc value (usually zero in the case of noise) and σ is the rms



Amplitude density distribution functions

value. The graph of this function is the familiar bell-shaped curve (see below) and the power of the central limit theorem lies in the fact that it converges very rapidly. That is to say, the sum of even a dozen or so independent variables of roughly comparable magnitude has a pdf which already bears a strong resemblance to a gaussian function even when the pdfs of the components are nothing like gaussian. As an example, the pdf of a sine wave is a highly non-gaussian (in fact a secant) function as shown below. Yet the sum of only a dozen sine waves of roughly the same amplitude and of different, unrelated frequencies has a pdf which very closely resembles the gaussian function right down to levels at which the ordinate is only 1% of its maximum value at the centre of the "bell". (For a truly gaussian pdf all the higher order density functions are also defined, but this need not concern us here.)

Electrical noise such as receiver noise is the sum of signals generated by billions of electrons and/or other charged particles in motion, so it is not surprising that it is closely gaussian.

By integrating P(v) from v to infinity we can determine the cumulative probability function i.e. the probability that an instantaneous sample of the waveform will exceed v. (Note that while this is a true probability, P(v) is *not* a probability but a probability *density*.) Values of the integral, often known as the probability integral, are included in many collections of mathematical tables. Non-linear processes such as rectification can change probability functions of all types but we shall not consider this here.

WHITE NOISE

According to Fourier, any repetitive waveform is equivalent to the sum of harmonically-related sine waves, the fundamental frequency of the series being the reciprocal of the repetition period. This collection of sine waves is called the spectrum of the waveform, and if one were to plot the amplitude of the sine waves vertically against frequency on the horizontal scale the result would be a series of vertical lines separated by the fundamental frequency. For this reason it is called a line spectrum.

As the repetition period becomes longer and longer, the fundamental frequency becomes lower and lower and the separation between successive frequency components becomes smaller and smaller. In the limit, as the repetition period becomes infinite, (i.e. the waveform becomes non-repetitive) the frequency separations become zero and the spectrum ceases to be a line spectrum and becomes continuous with all frequencies present. This is the case for random noise.

Now, Newton showed that white light consisted of all the colours (i.e. frequencies) of the rainbow, and by analogy, noise is described as "white" if its spectrum is flat, i.e. if the noise power within a given small bandwidth is the same, whatever the frequency on which that bandwidth is centred.

Truly white noise up to infinite frequency cannot exist in nature because its total energy would be infinite. However, many sources of noise arising in radio and other electronic systems have spectra which are flat over the frequency range of interest (and often far beyond). So far as such systems are concerned, the effect is the same as if the noise were truly white and consequently we call such noise white.

Also by analogy, noise which does not have a flat spectrum over the range of interest is sometimes called coloured noise and the analogy is even sometimes extended to describe the "non-flatness". Thus noise in which the higher frequency components have larger amplitude than those at lower frequencies is sometimes called blue or violet noise (since violet and blue are at the higher frequency end of the visible spectrum). Correspondingly the more common case in which the lower frequencies are more evident is called red noise. As a final twist, noise whose spectrum level is greater at lower than at higher frequencies but not very markedly so, is often called pink noise.

The spectrum of a waveform must not be confused with its probability density function and, at least in the case of random noise, they are quite independent.

In particular, if white gaussian noise is passed through a linear filter its spectrum will become modified according to the frequency response of the filter but it will nevertheless remain gaussian.

hanced signal/noise ratios for acceptable quality. This does not mean they are not worth developing since in some applications the benefits they provide may make an increase in power requirements a small price to pay. Nevertheless, it is a price which is unavoidably associated with bandwidth compression.

JAMMING

We now temporarily revert to equation 2 and convert the logarithms to the more familiar "natural" base e. Thus,

$$R_0 = k_0 k_1 W_0 \log_e(1+r_0) \qquad (9)$$

where $k_1 = \log_2 e = 1/\log_e 2 = 1.4427$

Now for r_0 less than unity we can expand the logarithmic term in equation 9 to give

$$R_0 = k_0 k_1 W_0 [r_0 - r_0/2 + r_0/3 - \ldots] \qquad (10)$$

and if r_0 is "sufficiently small" we may ignore terms in the second and higher powers of r_0.

What is "sufficiently small" is to some extent a personal choice. The author usually chooses a "threshold" value of ¼ or −6dB. For r_0 less than this, the "error" resulting from the approximation is less than 12 percent or 0.5dB.

Whatever value of "threshold" is chosen, we may assume that for r_0 less than this value,

$$R_0 \simeq k_0 k_1 W_0 r_0 \qquad (11)$$

We now wish to consider the sources of noise at the receiver. Firstly there will be the "receiver noise" power, $N_r = FkTW_0$ where F is the effective receiver noise factor, k is Boltzmann's constant, T the effective receiver temperature in kelvin and W_0, as before, the receiver bandwidth. Secondly there may be some external source of white noise of power density N_e giving rise to a noise power of W_0N_e. Finally, there may be an external interfering source or jammer which introduces a noise power N_j into the receiver. (It is important to consider N_j separately since it is not necessarily dependent on bandwidth, because a jammer has the option of concentrating all his power within the bandwidth W_0, regardless of what value of W_0 is chosen).

Thus the total noise power N is given by $W_0(N_e+FkT)+N_j$.

Since N_e and FkT are both multiplied by W_0 they can be treated as a single source of white noise of power density $N_d = N_e + FkT$.

Hence, from equation 11, when the signal/noise ratio is less than about −6dB,

$$R_0 = k_0 k_1 W_0/(W_0 N_d + N_j) \qquad (12)$$

We now note that in the absence of jamming ($N_j = 0$), this expression reduces to

$$R_0 = k_0 k_1 / N_d \qquad (13)$$

This implies that at low signal-to-noise ratios (and assuming suitable coding) the information rate attainable is independent of bandwidth! In these circumstances, expansion of bandwidth, by spread spectrum techniques for example, theoretically wins nothing – but also loses nothing – in terms of overall performance. On the other hand, it may spread the signal energy over so large a bandwidth that its power density at an intercept receiver is very low, perhaps even less than the thermal noise power density in that receiver. In such cases, while a perfectly viable communication channel may exist, an interceptor may well fail to recognize even that a transmission is occurring. This is the so-called low-detectability or low-probability-of-intercept (LPI) mode of operation.

In contrast to the non-jamming case, however, if the interference or jamming power is the dominant factor so that N_j is much greater than W_0N_d, then from equation 12,

$$R_0 = k_0 k_1 W_0 / N_j \qquad (14)$$

This expression shows that for low signal-to-noise ratios, increasing the system bandwidth W_0 permits a directly proportional performance improvement. In other words, every doubling of bandwidth requires an extra 3dB of jamming power to maintain the same jamming effectiveness. Similarly, such bandwidth expansion can be used to nullify the effect of unintentional interference.

This is the linear improvement "by the factor n" mentioned earlier as being always potentially available. Note that it represents a limit as the signal-to-noise ratio tends to zero.

Spread spectrum systems exploit this *linear* exchange of bandwidth for signal-to-noise ratio either to achieve low detectability or to counter deliberate or accidental interference. In either case, the potential improvement or "processing gain" is, to a good approximation, the ratio of the transmission bandwidth to the information bandwidth.

One other point which may be made here is that a number of such systems may coexist within the same bandwidth since any "interfering" signal may be treated as a jammer signal. There are certain requirements to be met in the design of such a "multiplexed" system and some of the more important of these will be discussed later.

From the foregoing discussion we have derived the following conclusions:

- By the use of suitable coding we may exchange signal-to-noise ratio for bandwidth (or data rate) on a logarithmic basis.
- When the signal-to-noise ratio is less than about −6dB there is very little difference between a logarithmic and a linear exchange and the latter may be more convenient to implement.

It is perhaps worth noting that one of the earliest attempts to counter interference by expanding bandwidth was the introduction of frequency modulation. However, this type of "coding" does not, in its most usual implementation, using limiters and discriminators, normally permit operation at very low signal-to-noise ratios, though its value in countering impulsive interference and, within limits, fading is well known.

SPREAD-SPECTRUM

We have so far mentioned expansion of bandwidth by spread-spectrum without defining what we mean by this term. Indeed, at one level the above sentence could be viewed as a tautology, since the words "spread-spectrum" could be taken legitimately as synonymous with bandwidth expansion. However, although many methods of bandwidth expansion are possible (fm has already been mentioned) the term "spread-spectrum" is usually reserved for at most two basic techniques.

The first of these, which has received

much publicity in the 1980s, is "frequency-hopping" – in which, usually, a more or less conventionally modulated carrier is intermittently shifted in frequency over a bandwidth much wider than the information bandwidth. Although the design of frequency-hopping systems can pose considerable engineering problems the basic principle is easily understood. In many cases, it may be viewed merely as a conventional system where from time to time the operating frequency is changed; though as the rate at which these changes occur is increased more complicated considerations are involved.

We shall not here discuss frequency-hopping in any detail except to say that it is obvious that if interference or jamming is concentrated in narrow regions of the frequency spectrum, then such systems are likely to spend much of their time operating at frequencies free from such interference and thus offer an anti-jamming capability. The case in which the jamming is spread uniformly over the total bandwidth employed nullifies this particular aspect but requires the jammer to distribute his energy over the wider band and thus reduces his effectiveness wherever the instantaneous operating frequency may be. Thus the anti-jamming property is fairly obvious and in fact frequency-hopping systems were devised and implemented well over a quarter of a century ago as anti-jamming schemes for radar.

Finally, it may be noted that there have been claims that frequency-hopping transmissions are very difficult to detect. This is not true and the misconception arises from an invalid extrapolation of conventional (and valid) communications "lore". It is true that conventional communications intercept systems would have difficulty in detecting (and/or locating the source of) many frequency-hopped emissions, but that is merely a statement that such conventional means are inappropriate to deal with systems having very different parameters from those for which they were designed. In fact, with properly designed intercept equipment, frequency-hopping transmitters are usually easier to detect and locate than many conventional systems. Frequency-hopping schemes do offer a further advantage in that they make it more difficult for an interceptor to determine message content; but where this is important, cryptographic encipherment is normally employed in all systems and so the advantage is perhaps relatively minor.

The term "spread-spectrum" is also applied (and in the minds of many, exclusively applied) to what is more properly termed direct sequence spread-spectrum or DSSS. This will be further discussed in a future article.

For the present we shall conclude with a simple and plausible model to demonstrate the basic feasibility of operation at very low signal-to-noise ratios, since one sometimes meets incredulity on this point.

OPERATING WITH LOW S:N

Consider a conventional communication link occupying a bandwidth b and let the receiver noise power density by M_0 and the received signal power be P_r. Then the effective signal-to-noise ratio is

$$R_1 = P_r/bM_0 \tag{15}$$

Now suppose the transmitter is modified to transmit the same signal simultaneously on m different frequencies, thus occupying a total bandwidth

$$B = mb \tag{16}$$

(We assume for the present that the receiving system now comprises m of the "old" receivers, each one tuned to a different one of the m channels).

We must not cheat by assuming also an increase in total transmitter power; so the received power in each channel of bandwidth b will now be only P_r/m.

The signal output *voltage* V_s from each channel will be proportional to the square root of the power. Thus $V_s = \propto (P_r/m)^{1/2}$ say.

If we can be sufficiently clever in our modulation system we can arrange that all the V_s will be identical and in phase; and since there are m of them, we may add them all together *coherently* to obtain a system output signal voltage of

$$mV_s = m\propto(P_r/m)^{1/2} = \propto(mP_r)^{1/2} \tag{17}$$

This corresponds to an effective signal power of mP_r. Noise components in each channel will be independent and uncorrelated (see the next article) and so they will add only power-wise. Thus the system output noise power will be mbM_0, giving an effective output signal-to-noise power ratio of

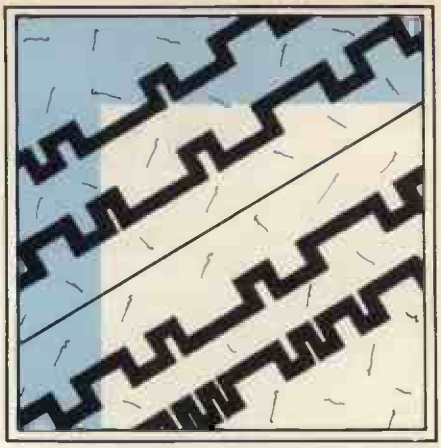
$$r_2 = mP_r/mbM_0 = P_r/bM_0 \tag{18}$$

It will be seen that this is precisely the same as for the original case (equation 15) and hence should give the same performance despite the fact that the signal-to-noise power ratio in the transmission bandwidth is only P_r/mbM_0 or 1/m times that in the conventional system. This example is closely analogous to the use of spread spectrum for low detectability purposes. Indeed it represents a conceptually feasible means of implementing a spread spectrum system, though not one the author would normally recommend!

Similarly it can be used as a conceptual explanation of the use of spread spectrum to counter jamming, for if the jammer can inject a noise power N_j into the conventional system (where we assume $N_j \gg bM_0$) then that system will experience a signal-to-noise ratio of P_r/N_j.

In the modified system, the jammer may choose to inject N_j into just one channel giving m−1 channels of fairly good signal-to-noise ratio and one of appalling s:n. However, the summed output will have a very good signal-to-noise ratio. Alternatively, the jammer may elect to spread his power over all m channels, but in that case only N_j/m will be injected into each channel and the output signal-to-noise ratio will be $mP_r/m.(N_j/m) = mP_r/N_j$, or m times that of the conventional system. The reader might care to calculate the output signal-to-noise ratio if the jammer adopts other strategies such as sharing N_j amongst a sub-set of say q channels.

The above assumes that the jammer components are uncorrelated: in other words, that while the signal components in each channel are identical and in phase, noise or jamming components are not, and so add power-wise rather than voltage-wise. However, if the communicator can arrange for the former to be true, the jammer can do likewise, so that an intelligent and well informed jammer designer can nullify the advantage postulated. This is only one of several reasons why this particular form of spread spectrum is not used in practice. Nevertheless, it provides a readily understood and simple model to explain the underlying principles and the plausibility of operation at very low signal-to-noise ratios. As a practical example, in the very early 1960s the author had a two-way digital vhf data link operating over about 30 miles and employing direct sequence spread spectrum (DSSS). It operated satisfactorily with an output data bit error-rate of less than 10^{-3} at an input signal-to-noise ratio of about −27dB.



There have been claims that frequency-hopping transmissions are very difficult to detect. This is not true ...

In subsequent articles the author will outline aspects of DSSS systems (which provide a linear exchange of bandwidth for signal-to-noise ratio) and of error-corrrection systems (which attempt to provide a logarithmic exchange). He will also discuss coding gains and the distinction between and applicability of hard and soft decision coding.

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Working with DSP

The routes to Fast Fourier Transform have multiplied with the arrival of specialist DSP chips. The article presents a practical look.

JULIAN NOLAN

The Fast Fourier Transform (FFT) is one of the most frequent applications of DSP. A number of efficient algorithms have been written to implement this. Naturally the FFT is not restricted to DSPs and because of this I have outlined alternative systems together with their relative speeds.

When designing an FFT system or investigating alternatives the following criteria should be taken into account:

Accuracy; execution speed; programming effort; hardware design effort; system cost; system flexibility, and integration required.

These considerations should not be compared with regard to their absolute value as individual relevance largely depends on the level of problem solving.

Alternatives to the single-chip DSP solution are those based on general-purpose computers, which include those programmed at high level, micro-programmed or with a dedicated arithmetic processor; the microprocessor-based systems implemented in a microcomputer, with or without arithmetic coprocessor; and systems based on signal-processing units, which may be single or multi-chip types – bit and word-slice systems, for example.

The relative speeds of these various systems, together with their very approximate costs are shown in **Figs. 1a, 1b and 1c**.

Not surprisingly, DSP systems provide a cost effective solution for applications which require relatively high-speed number crunching capabilities.

This is also supported by **Table 1** which gives very approximate figures for the various alternatives in the categories outlined above.

There have been many recent advances in DSP design with the launching of many new DSP devices over the last few months. The first compact entrant was the Intel 2920. This device suffered from major shortcomings such as analog I/O with limited resolution (9-bit ADC) and the absence of a dedicated multiplier. In all devices introduced since then the most important building block has been the hardware multiplier which obviously greatly decreases an FFT's execution time, thus making DSP devices ideal for this task.

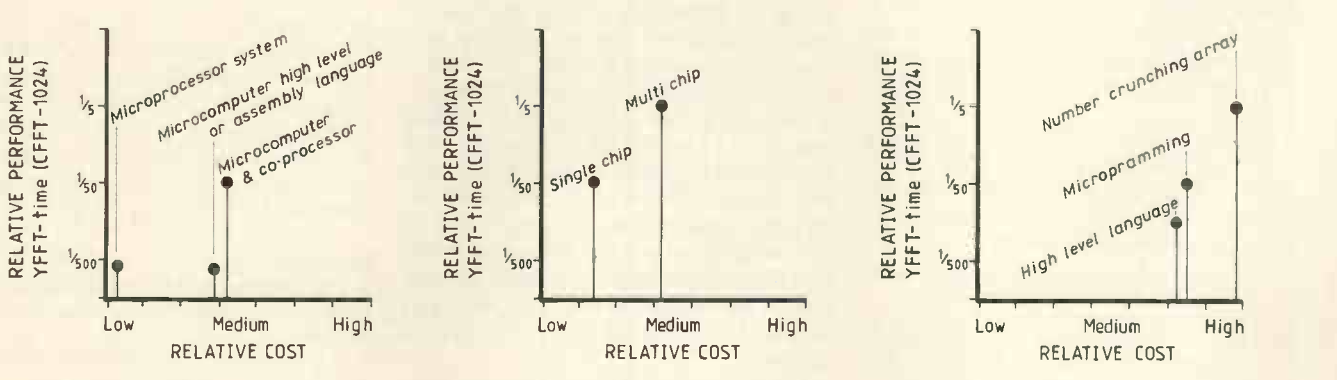
Alternatives	Execution speed (ms)	Programming effort	Hardware design effort	System Cost Relative	Average £	System flexibility
GP high level lan.	240	Low	None	Above average	10,000	High
GP microprogramming	50	High	None	Above average	10,000	Above average
GP + number cruncher	5	High	None	High	25,000	Above average
Microcomputer	1000	Below average	None	Medium	2,000	High
Microcomputer+coproc.	50	Below average	None	Medium	3,000	Above average
Microprocessor sys.	1000	Average	Medium	Low	75	Average
Single chip SP	50	Above average	Medium	Above average	200	Average
Multi-chip SP	5	High	High	Medium	1,000	Low

GP – general purpose computer
SP – signal processor

Established popular devices include the NEC 7720, AMI 2811 and TMS32010. Both the AMI and NEC processors have limited on chip memory and no external addressing capability, which limit the dimension of a FFT. On these chips an FFT can be calculated directly to 32 points, while proper sequencing operations and block data transfers from external memory under supervision of a controlling microprocessor are required to extend the size of the transformation. If this is implemented execution speed suffers. Favourable 32 point CFFT execution times can often be increased considerably with higher transform lengths due to the data transfer overhead.

The TMS 32010 can handle CFTTs up to 64 points (0.535ms) because of its greater on-chip memory. External memory addressing, however, can take place up to 4K, thus allowing a direct CFFT of up to 1024 points (execution time 69ms for looped program [optimized]). The execution speeds can be significantly improved by paralleling devices, each executing a smaller subtransform.

Fig.1. Cost/performance comparisons of DSP systems



The TMS32010 has now been around several years and because of this a wealth of development and applications information is available for this device. Support tools, and also low cost development kits are available. In terms of cycle time (200ns) and on-chip memory the TMS32010 is now beginning to show its age, although it and other older processors still remain a viable option for low-cost DSP systems.

New devices include the Fujitsu 8764, the Hitachi 61810, the AT&T DSP32C, the Motorola 56000, the NEC 7281 and the Philips PCB5010. Texas Instruments has also released two new DSP components continuing the TMS320 series: the TMS320C25 and TMS320C30 both offer advanced architectures. The high growth rate of the DSP sector has left behind a number of niches in the market, which as always are being filled by the latest crop of highly enterprising American semiconductor houses.

The Zoran Corporation has produced the ZR34161 VSP (vector signal processor), the instruction set of which incorporates such commands as FFT. Other contenders include the high-speed data-conversion company Datel.

For real-time signal processing up to the

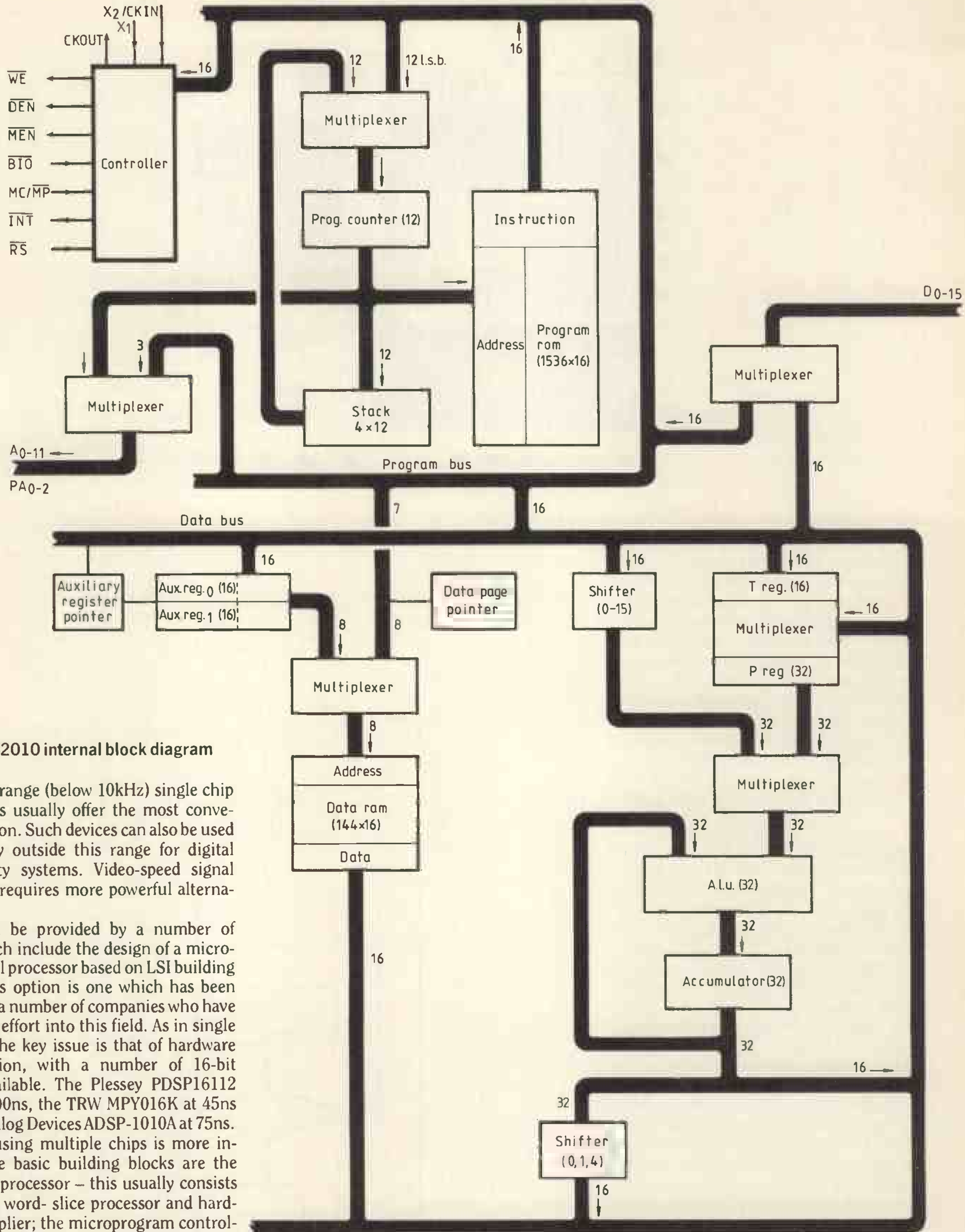


Fig.2. TMS32010 internal block diagram

voice-band range (below 10kHz) single chip DSP devices usually offer the most convenient solution. Such devices can also be used increasingly outside this range for digital high fidelity systems. Video-speed signal processing requires more powerful alternatives.

This can be provided by a number of means which include the design of a microcoded signal processor based on LSI building blocks. This option is one which has been adopted by a number of companies who have put a lot of effort into this field. As in single chip DSP the key issue is that of hardware multiplication, with a number of 16-bit devices available. The Plessey PDSP16112 cycles at 100ns, the TRW MPY016K at 45ns and the Analog Devices ADSP-1010A at 75ns.

Design using multiple chips is more involved. The basic building blocks are the arithmetic processor – this usually consists of a bit- or word- slice processor and hardware multiplier; the microprogram controller which includes an instruction sequencer and a data and coefficient address generator; and the data and program memory along with tempory registers (can be pipelined).

A system comprising industry standard components could include a 2901 4-bit slice processor, a hardware multiplier/accumulator, store, and two 2911 microcontrollers. Using this kind of implementation a 1024 point CFFT can be executed in about 10ms.

Reportedly using a system based around two Plessey PDSP16316A complex accumulators and a PDSP16112A hardware multiplier, a new complex Butterfly algorithm can be generated every 50ns allowing a 1024 point CFFT to be executed in 256µs.

Increasingly the trend in some systems is to move towards floating rather than fixed point processing and TRW, Analog Devices and AT&T offer chip sets in this field. Established devices return 1024 point CFFT execution times of less than 4ms, while latest Analogs' devices yield throughputs in excess of 40 Mflops.

Single chip digital signal processing ICs have now reached the price and performance required for widespread use. Software support is plentiful for the more popular devices, while hardware design effort is in most cases limited. These factors have been significant in the acceptance of DSP by manufacturers such as H-P who use the TMS32010 in the HP-3561/2 spectrum analyser.

In the multi-chip DSP sector the recent move from bit-slice to word- and floating-point-slice architectures has enabled de-

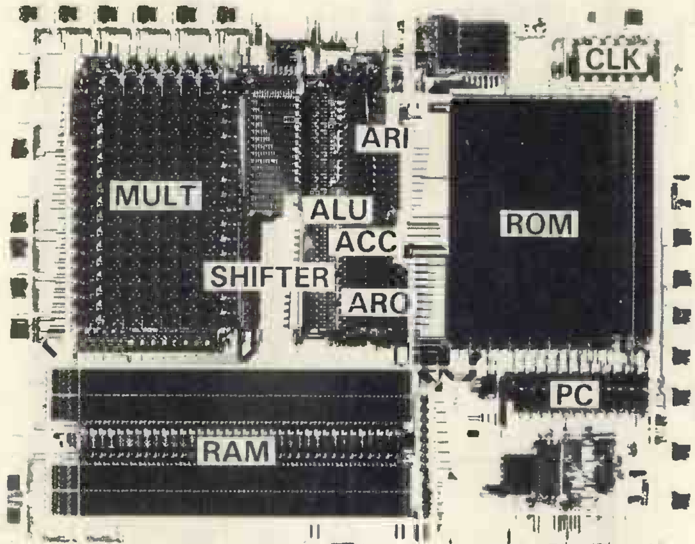


Fig.3. Texas Instruments TMS32010

velopment of signal processors with array-processor-speed performance at a fraction of the previous cost. Microsequencer support and decreased hardware multiplication times have also been a major factor. Generally this type of implementation requires a hardware and software design effort which should not be underestimated on custom systems. New devices have tended to reduce this through the use of data flow and systolic array signal processing architectures.

APPLICATIONS AND TECHNIQUES/ TMS32010

Typical applications for DSP's in signal processing include digital filtering, correlation, Hilbert transforms, FFT's, adaptive filtering, radar and sonar processing, seismic processing, speech processing and waveform generation. In the instrumentation sector applications takes in spectrum analysis (usually based around FFT system), digital filtering, phase-locked loops, transient analysis, arbitrary waveform generation and averaging.

Fig. 2 shows the block diagram of the TMS32010 from which it can be seen that the device is based on a modified Harvard architecture – the discrepancy being that the device allows transfers between program and data spaces. In a Harvard architecture the program and data memory lie in two different spaces, permitting full overlap of the instruction fetch and execute. Through this modification coefficients stored in program memory can be read into the RAM, eliminating the need for a separate coefficient ROM.

As in most other DSP processors a hardware multiplier and barrel shifter are incorporated.

A wide range of DSP applications require correlation and digital filtering to be carried out as part of an overall calculation, or in their own right.

The main steps of implementing a Finite Impulse Response (FIR) filter are shown in **Fig. 4**. The coefficients, h(k), which are stored in ROM must be initially read into RAM using the TBLR (table read) instructions. Following this the current input, x(n), is read into the data RAM, and the multiply, accumulate, and data shift operations are performed. The data shift operation enables the x(n) values to be realigned, thus enabling the next value y(n) to be computed (ie Z^{-1}

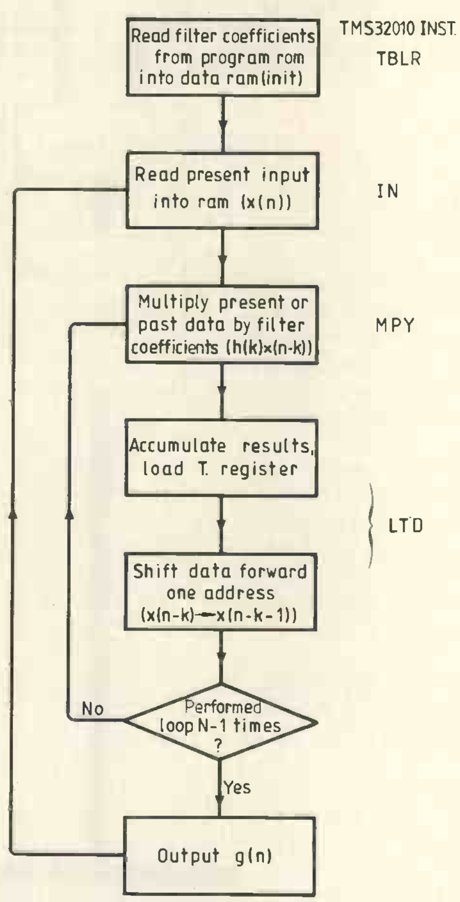


Fig.4. Flow diagram showing implementation of FIR filter

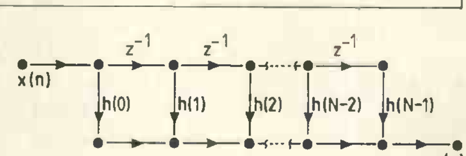


Fig.5. Direct-form FIR filter

operation).

Digital filters are normally based on the following relationship between the filter input sequence, x(n), and the filter output sequence, y(n):

y(n) = sum(ak ★ y(n−k)) + sum(bk ★ x(n−k)) . . . . (1)

This equation is referred to as a linear-coefficient difference equation, the FIR filter being one of the two filters representable by linear-coefficient difference equations (the other being IIR).

To implement a FIR filter using a TMS32010 DSP the following concepts need to be considered:

A) the relationship between the filter structure and unit sample response of a FIR filter;

B) the use of LTD and MPY (Load 'T' register, accumulate product, and move data in memory forward one address (LTD) and multiply with T register, store product in P register (MPY);

C) the ordering of the input samples in the data memory of the TMS32010.

For FIR filters all of the ak in (1) is zero, thus reducing to:

y(n) = sum(bk ★ x(n−k)) (2)

To.

$$y(n)=\sum_{h=1}^{M} a_k y(n-k)+\sum_{k=0}^{M} b(k)x(n-k) \qquad (2)$$

$$y(n)\sum_{k=0}^{M} b_k x(n-k) \qquad (2)$$

$$y(n)\sum_{k=0}^{M} h(k)x(n-k) \qquad (3)$$

$$H(z)=\frac{Y(z)}{X(z)}=\sum_{h=0}^{M} b_k z^{-1}=\sum_{k=0}^{M} h(k)z^{-k} \qquad (4)$$

$$Y(n)=cx(n)+\sum_{i=1}^{[(N-1)/2]} P_i(n) \qquad (5A)$$

For this reason, the output of a FIR filter is simply a finite-length weighted sum of the present and previous inputs to the filter. The unit sample is referred to as a discrete time impulse, or just an impulse. If the sample response of the filter is denoted as h(n), then from (2) it can be seen that h(n) = b(n), allowing (2) to be written as

y(n) = sum(hk ★ x(n−k)) (3)

From this it can be seen that a FIR filter has a finite length response to a unit sample, as the name implies. If the z transforms of x(n), y(n) and h(n) are represented as X(z), Y(z) and H(z) respectively then

H(z) = Y(z)/X(z) = sum(bk ★ z) = sum(hk ★ z) (4)

Both equations (3) and (4) may be represented in networks structure shown in **Fig. 5**. Since the filter coefficients can be identi-

```
* THIS SECTION OF CODE IMPLEMENTS THE FOLLOWING EQUATION:                *
* x(n-4)h(4) + x(n-3)h(3) + x(n-2)h(2) + x(n-1)h(1) + x(n)h(0) = y(n) *
*
NXTPT     IN    XN,PAQ          * GET THE NEW INPUT VALUE XN FROM PORT PAQ *
*
          ZAC                   * ZERO THE ACCUMULATOR *
*
          LT    XNM4            * x(n-4)h(4) *
          MPY   H4
*
          LTD   XNM3            * x(n-4)h(4) + x(n-3)h(3) *
          MPY   H3
*
          LTD   XNM2            * SIMILAR TO THE PREVIOUS STEPS *
          MPY   H2
*
          LTD   XNM1
          MPY H1
*
          LTD   XN
          MPY   H0
*
          APAC                  * ADD THE RESULT OF THE LAST MULTIPLY TO *
                                * THE ACCUMULATOR                        *
*
          SACH YN,1             * STORE THE RESULT IN YN *
*
          OUT   YN,PA1          * OUTPUT THE RESULT TO PORT PA1 *
*
          B     NXTPT           * GO GET THE NEXT POINT *
```

Fig.6. Code to implement a length-5 FIR filter

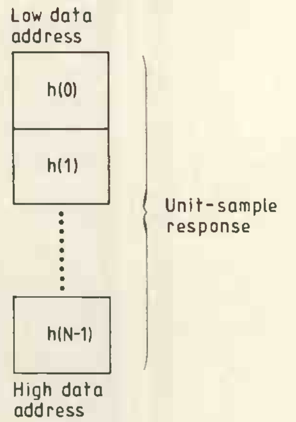


Fig.7. Filter resulting from code in Fig.6

fied directly from the difference equation (3) this structure is referred to as a direct-form realization of a FIR filter. The branches labelled with z in Fig. 5 correspond to the analogous delays in (3) and the multiplications by z^{-1} in (4). The portion of code to implement a length-5 FIR filter (for TMS32010) is shown in **Fig. 6**, while the length-5 FIR filter is illustrated in **Fig. 7**. As usual XN corresponds to x(n) and XNM1 corresponds to x(n−1) etc.

The input sequence x(n) is stored as shown in Fig. 4. Generally each of the multiplies and shifts of x(n) in (3) are implemented with an instruction pair in the form

LTD XNM1

MPY H1

The instruction LTD XNM1 loads the T register with the contents of address XNM1, adds the result of the previous multiply to the accumulator, and also shifts the data at the address. XNM1 to the next higher address in the data memory.

References.

H. Van der Auweraer and R. Snoeys, FT Implementation Alternatives in Advanced Measurement Systems. IEEE February 1987.

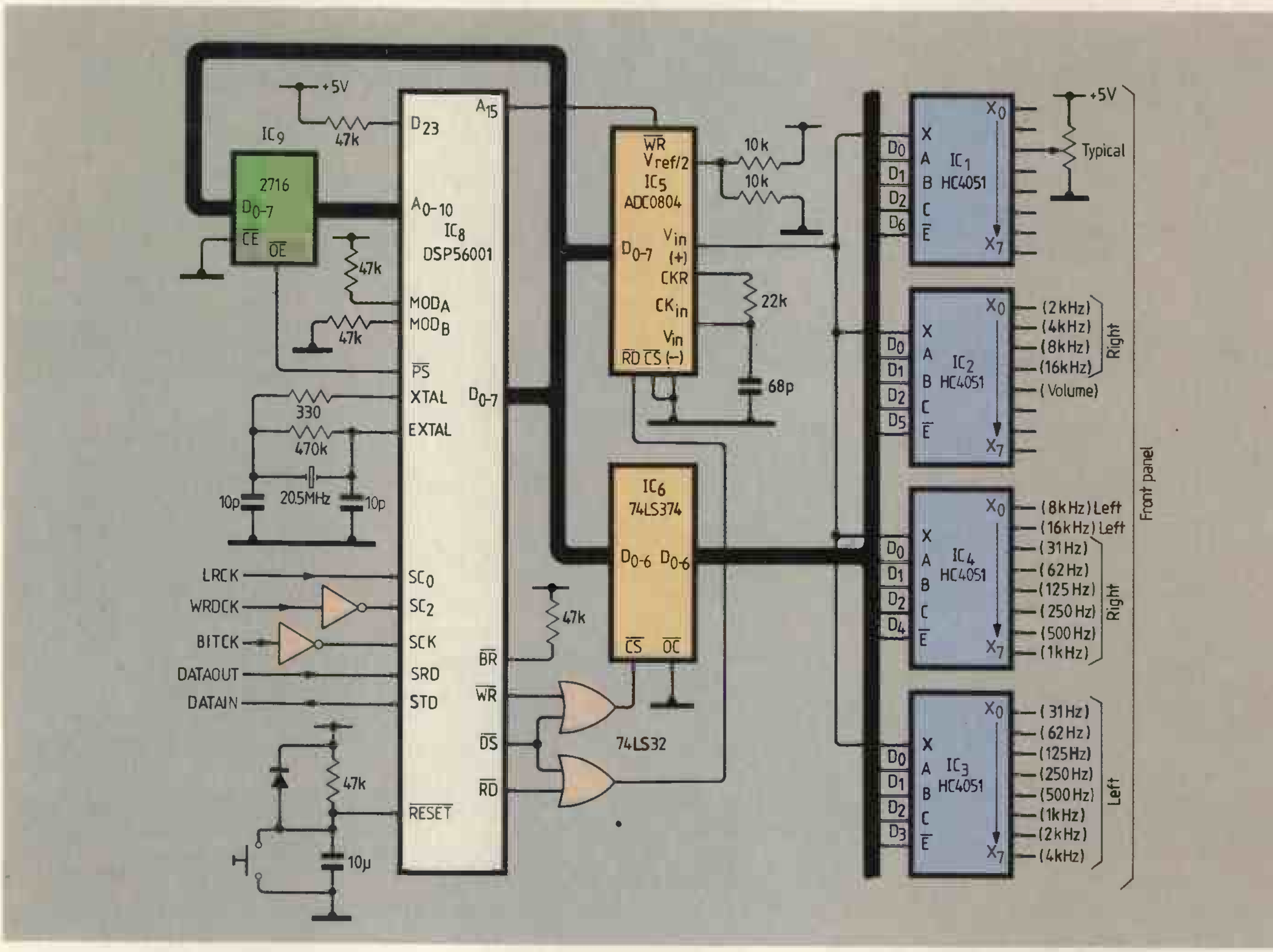
C.S. Burrows and T.W. Parks. "DFT/FFT and Convolution Algorithms – theory and implementation". Pub. John Wiley & Sons.

A.V. Oppenheim and W.W. Schafer, "Digital Signal processing" Prentice Hall Inc., Englewood Cliffs, NJ), 1975

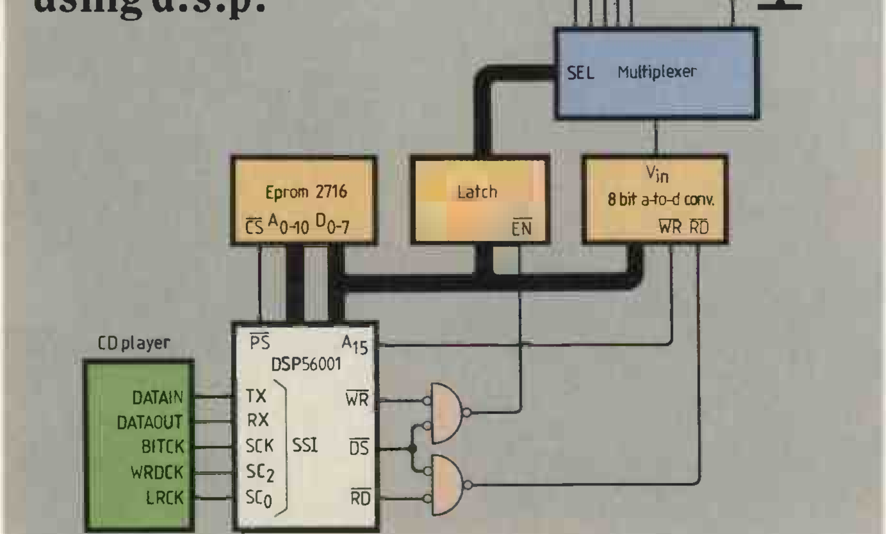
Implementation of FIR/IIR filters with the TMS32010 Texas Instruments 1984.

Zoran, Plessey, Analog Devices, T.I., AT&T, AMI, DSP data books/information packs, 1987/88.

APPLICATIONS SUMMARY



Graphic equalization using d.s.p.



Full details of a stereo ten-band equalizer based on the 56001 signal processor are given in publication APR2/D from Motorola. Interfacing to the equalizer is fully digital; the authors designed the unit specifically for the serial data interface on a Sony 650ESD which is not available in the UK, but engineers at East Kilbride can help out European o.e.ms wanting to adapt the design.

Included in the 33-page note are details for designing and implementing band-pass filters, interface circuits and software.

Motorola, Macro-Marketing Ltd, Burnham Lane, Slough, Berkshire SL1 6LN. 06286 4422.

'World-chip' modem now autodials

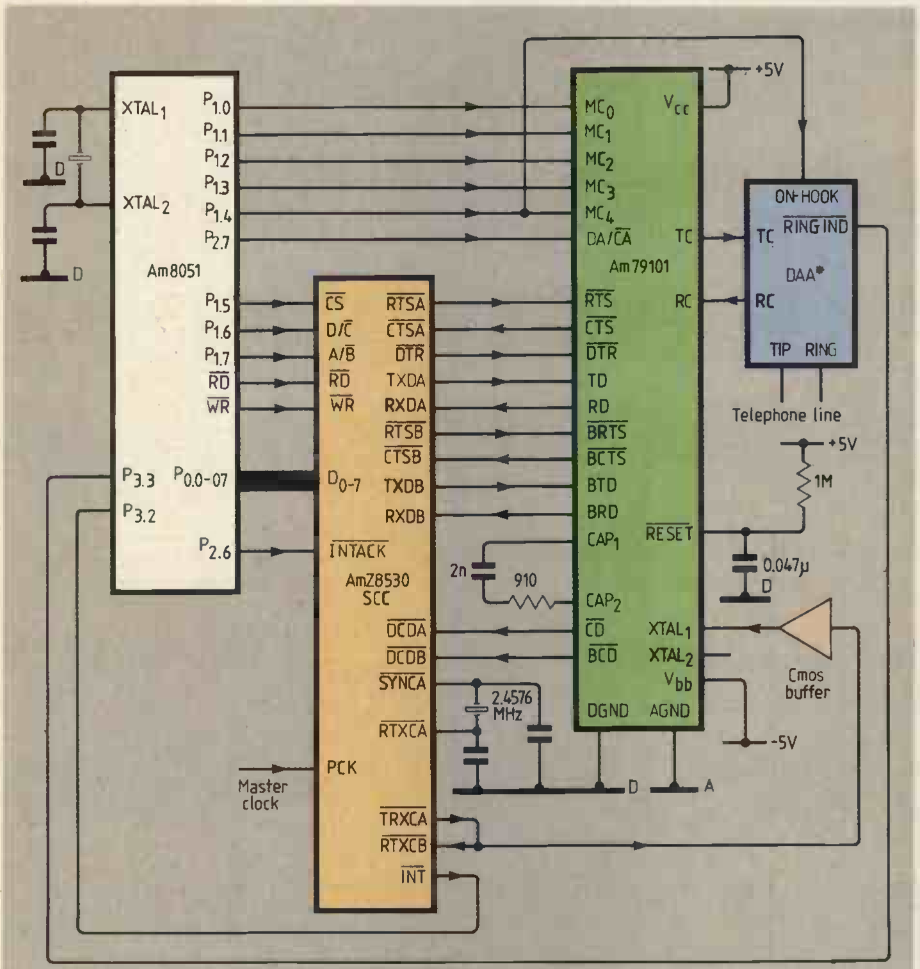
An advanced version of the Am7910 f.s.k. modem has been produced that includes not only the 7911's extended mode set but also d.t.m.f. autodial support, answer-call-progress tone detection and an on-chip 4-to-2-wire duplexer.

Application details of the device – the Am79101 – are given in a comprehensive technical manual that covers all three modem chips. It gives background information on modems followed by more specific details of the three devices and how they interface to serial controllers, processors and the telephone line.

This circuit, for a 1200bit/s half-duplex modem with 75/150bit/s back channel, is shown here to illustrate how few components are needed to interface the device; it is not from the technical manual but from the device data sheet. For a 300bit/s full-duplex modem, the circuit is further simplified since the 8051 internal serial controller replaces the 8530 serial communications controller.

Mode-control signal MC_4 controls the on-hook relay in the data-access arrangement, d.a.a. When low, MC_4 takes the circuit

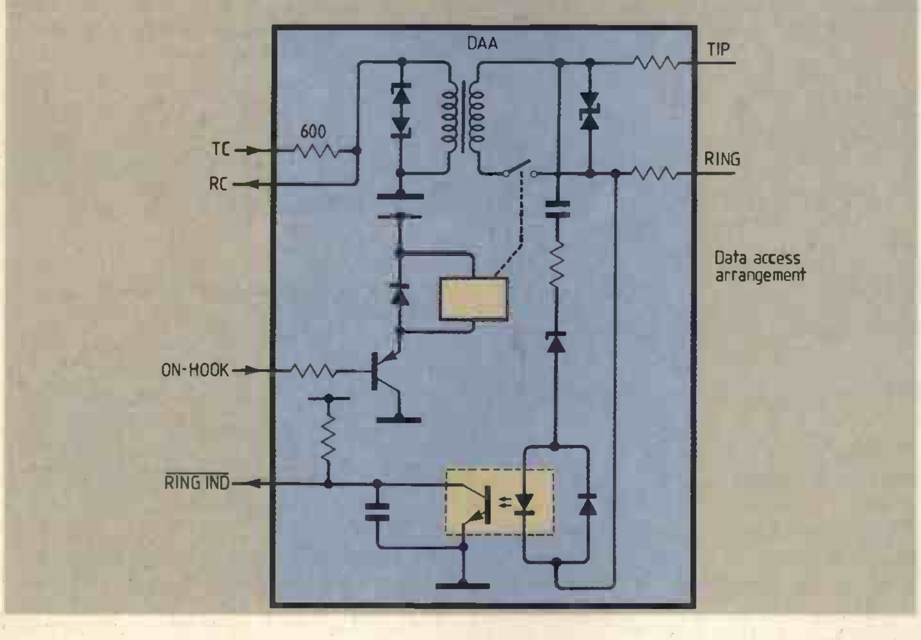
APPLICATIONS SUMMARY



off-hook and when high it keeps the circuit on-hook for analogue loopback testing. If d.t.m.f. is not available, the relay can be pulsed.

During automatic answering, incoming calls interrupt the processor via the ring indicator and an interrupt-service routine is entered. This routine places the relay off hook and sets the modem chip in call mode so that the answer tone can be produced. Once the call is established or answered, the 8051 has complete control and can start data transfer.

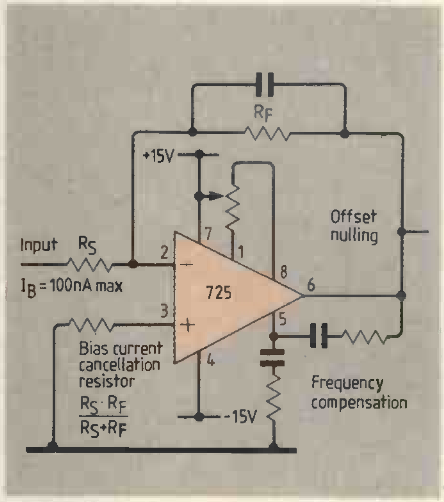
AMD, AMD House, Goldsworth Road, Woking, Surrey GU21 1JT. 04862 22121

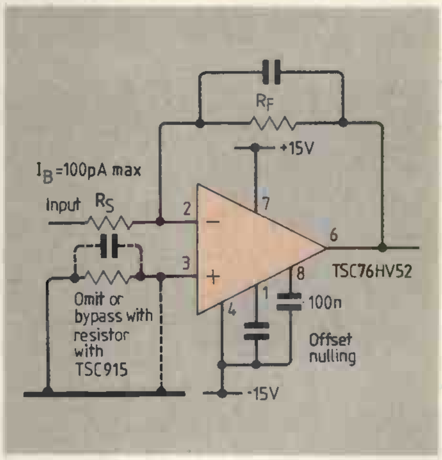


Data access arrangement

Using chopper-stabilized op-amps

Replacing an ordinary op-amp with a chopper-stabilized device can lower offset drift, lower offset voltage and lower power consumption. One thing to bear in mind though when replacing a high-input bias-current device like the 725 with a chopper stabilized operational-amplifier like the c-mos TSC76HV52 is that the bias current





compensation resistor becomes a nuisance.

Conventional design practice is to cancel bias current by matching input impedances as shown. Since the HV52 has a maximum input bias current of only 100pA, the resistor is unnecessary. In fact including it will make the charge-injection current passing through the impedance balancing resistor appear as a noise source.

Teledyne's latest op-amp data book contains quite a lot of design information, although the number of applications circuits is a little small.

Teledyne, SSI, 128-130 Carshalton Road, Sutton, Surrey SM1 4RS. 01 643 1126/9

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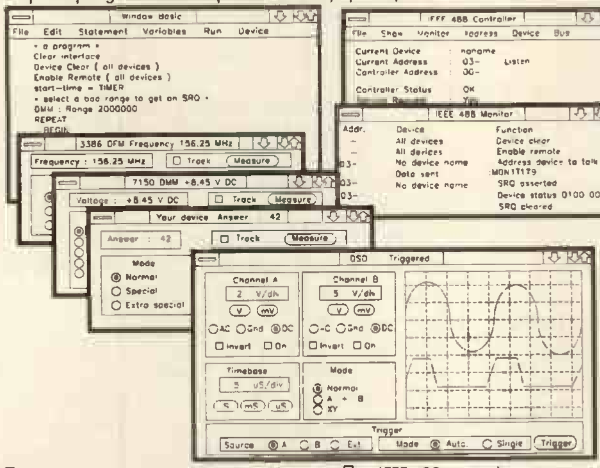

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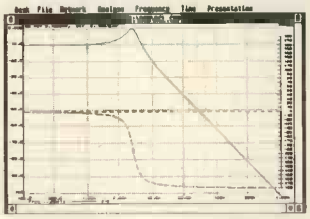

Frequency response of a low pass filter circuit

1 Frequency response
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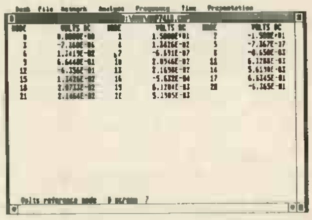
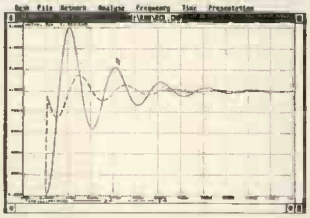
2 DC Quiescent analysis
SPICE•AGE analyses DC voltages in any network and is useful, for example, for setting transistor bias. Non-linear components such as transistors and diodes are catered for. (The disk library of network models contains many commonly-used components – see below). This type of analysis is ideal for confirming bias conditions and establishing clipping margin prior to performing a transient analysis. Tabular results are given for each node; the reference node is user-selectable.



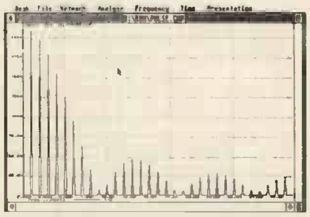
DC conditions within model of 741 circuit



Impulse response of low pass filter (transient analysis)

3 Transient analysis
The transient response arising from a wide range of inputs can be examined. 7 types of of excitation are offered (impulse, sine wave, step, triangle, ramp, square, and pulse train); the parameters of each are user-definable. Reactive components may be pre-charged to steady-state condition. Up to 13 voltage generators and current generators may be connected. Sweep time is adjustable. Up to 4 probe nodes are allowed, and simultaneous plots permit easy comparison of results.

4 Fourier analyses
SPICE•AGE performs Fourier transforms on transient analysis data. This allows users to examine transient analysis waveforms for the most prevalent frequency components (amplitude is plotted against frequency). Functions as a simple spectrum analyser for snapshot of transients. Automatically interpolates from transient analysis data and handles up to 512 data values. Allows examination of waveform through different windows. Powerful analytical function is extremely easy to use.



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Video distribution using op-amps

Design precautions and performance characteristics of a video distribution amplifier built from monolithic operational amplifiers.

DR. C.O. ANAZIA

Broadband video-distribution amplifiers made from hybrid amplifiers are readily available but expensive. Such amplifiers often incorporate switched-mode supply techniques and are normally used in community-antenna television systems or tv transmitters and translators. However, by taking advantage of relatively low cost operational amplifiers, a video or tv camera signal distribution amplifier can be built for considerably less cost but with all the features of commercial models.

The need for such low-cost video distribution amplifiers is acute in developing countries where import restrictions make it almost impossible to purchase commercially available video-distribution amplifiers. This amplifier, using a buffered high slew-rate op-amp with feedback, drives 1V pk-pk video signals into 75Ω coaxial cable.

The first op-amp can be any high slew rate type with high input impedance and wide bandwidth; an example is the National Semiconductor LH0032 with 500V/μs slew rate and 10^{12}Ω input impedance at 70MHz bandwidth. Requirements of the buffer op-amp are low output impedance, high slewrate, low harmonic distortion and high power efficiency. You could use National Semiconductor's LH0002 which has 200V/μs slew rate, 6Ω output impedance at 0 to 50MHz bandwidth and harmonic distortion typically in the region of 0.1%. To increase current output the input and output buffers are integrated inside the feedback loop.

Input capacitance of most operational amplifiers with high slew rate is typically very small, at around 5pF. This small input capacitance can form a significant time constant with resistance in the feedback loop, R_f. Thus for the optimum performance of the input buffer, input capacitance to the inverting input is compensated by a small variable capacitor across the feedback resistor. The value of such capacitor is fairly dependent on closed-loop gain.

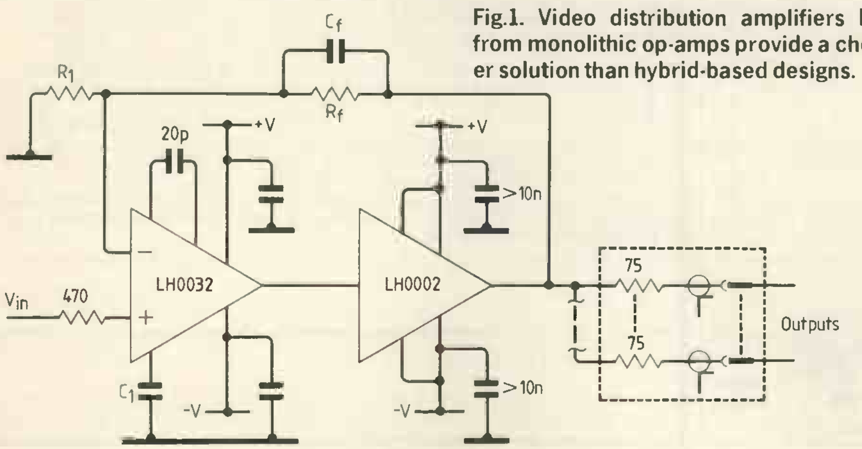

Fig.1. Video distribution amplifiers built from monolithic op-amps provide a cheaper solution than hybrid-based designs.

CIRCUIT GAIN CHARACTERISTICS

No phase reversal between output and input voltage is present in the circuit and the feedback voltage across R_1 is in series with but subtracts from input voltage V_{in}. Hence V_{in} sees the very high input impedance of the non-inverting input of the input buffer. Since the non-inverting input of the input buffer draws negligible current, it will not load the signal source.

Closed-loop voltage gain can be given as,

$$A_f=\frac{A}{1+\beta A} \qquad (1)$$

where A is the voltage gain without feedback. Voltage gain for a compensated feedback loop is A_{fc}, thus,

$$A_{fc}(\omega)=\frac{A_f(\omega)}{1+\beta_c A_f(\omega)} \qquad (2)$$

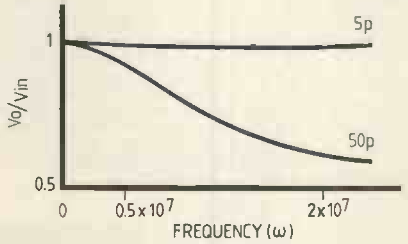

Fig.2. With a low value feedback capacitor, frequency response is essentially flat up to 4MHz, but it deteriorates quickly with larger values.

You can then deduce from eq.(1) that,

$$|\beta_c|=\frac{\beta}{(1+\omega^2 R_f^2 C_f^2 \beta^2)^{1/2}}$$

where β is the uncompensated feedback factor and can be given as;

$$\beta=1/(1+R_f/R_1) \qquad (3)$$

Factor β is normally complex at high frequencies. Alternatively, eq. (3) can be expressed as,

$$|\beta_c|=1/[A_f^2+\omega^2 C_f^2 R_f^2]^{1/2} \qquad (5)$$

Consequently, the output signal gain can be approximated as;

$$\left|\frac{V_{out}}{V_{in}}\right|=\frac{1}{\beta}(1+\omega^2 C_f^2 R_f^2)^{-1/2} \qquad (6)$$

From eq.(5), you can see that voltage feedback factor β_c is frequency dependent. Hence C_f, the frequency response compensation capacitor, can be adjusted to provide output amplitude of high integrity within the operating frequency range.

Equation (6) can be used in determining the range of the compensating capacitor.

PERFORMANCE

Output impedance of LH0002 is typically 6Ω and in conjuction with a voltage bandwidth of approximately 50MHz, it can be considered to approach a zero-impedance voltage source so that loads connected to the output resistor have no effect on one another. The purposes of the 75Ω output resistors are,

- to provide the proper drive source impedance for coaxial cables,
- to increase isolation between the loads,
- to give short-circuit protection to the LH0002 buffer

Usually in order to provide information concerning the frequency and phase of the missing colour subcarrier signal, a colour burst is sent along with the video signal. The amplitude of the colour burst may be greater than that of a standard PAL composite video signal. With proper frequency compensation, the effect of the colour burst on the output of the circuit can be minimized.

Normalised frequency response of the circuit is shown for the two values of frequency compensating capacitor. You can see that the circuit is flat up to approximately 4MHz for the lower value of frequency compensating capacitor; response is poor however for a relatively high compensating capacitor.

Further reading

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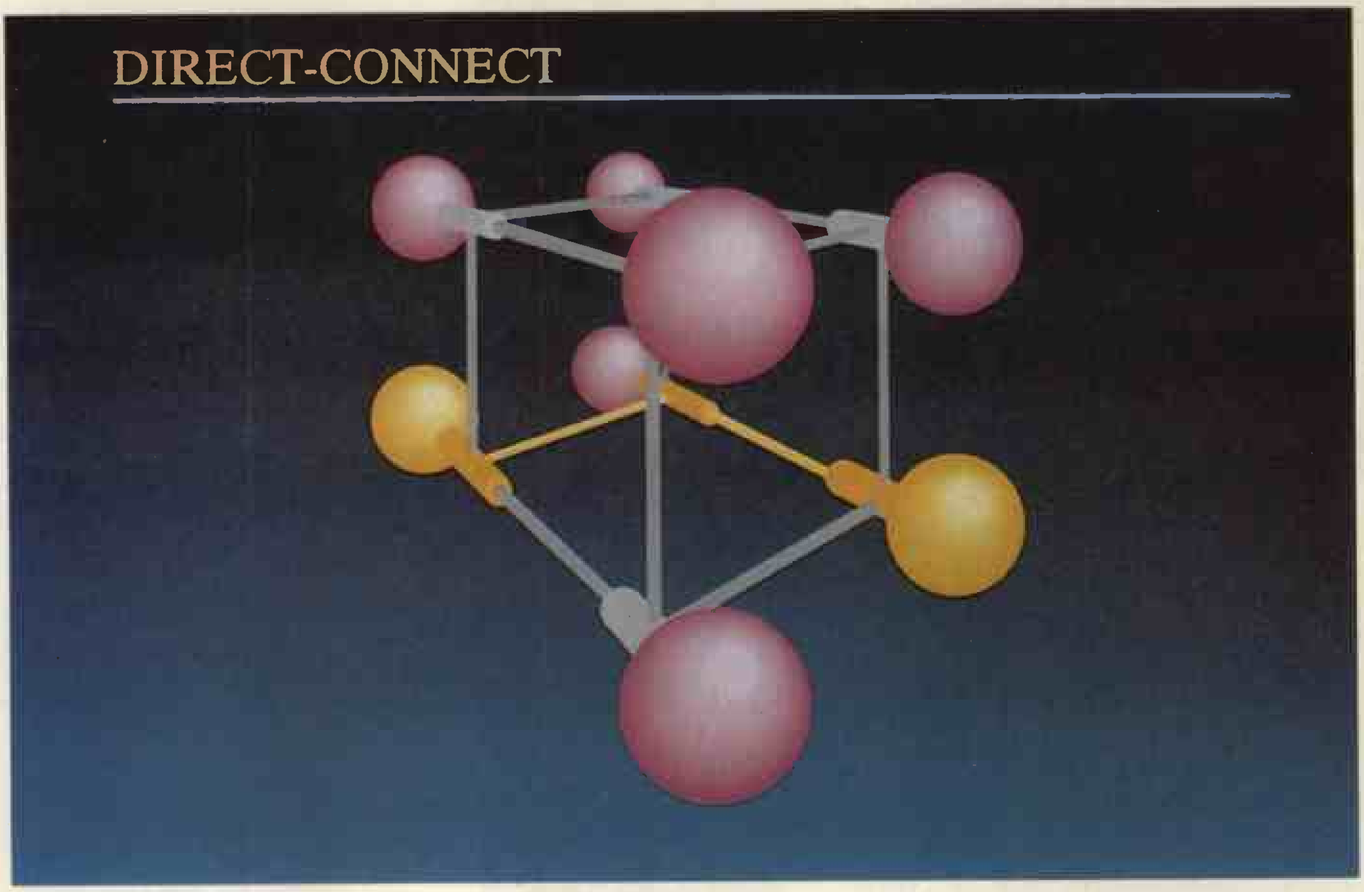


With direct connect, each node of the hypercube can talk directly to any other.

I/O nodes for iPSC/2

Dedicated i/o nodes and concurrent file system speed up concurrent supercomputer

MARTIN ECCLES

In a parallel processing cube, the speed of the system is tempered by the speed of its slowest node. Given a supercomputer capable of 1200Mflop peaks, this limitation might seem trivial but software has a tendency to expand to suit the limits of the machine. As you know, this phenomenon is universal but it particularly applies to scientific and engineering computing applications, where large amounts of data need to be processed simultaneously.

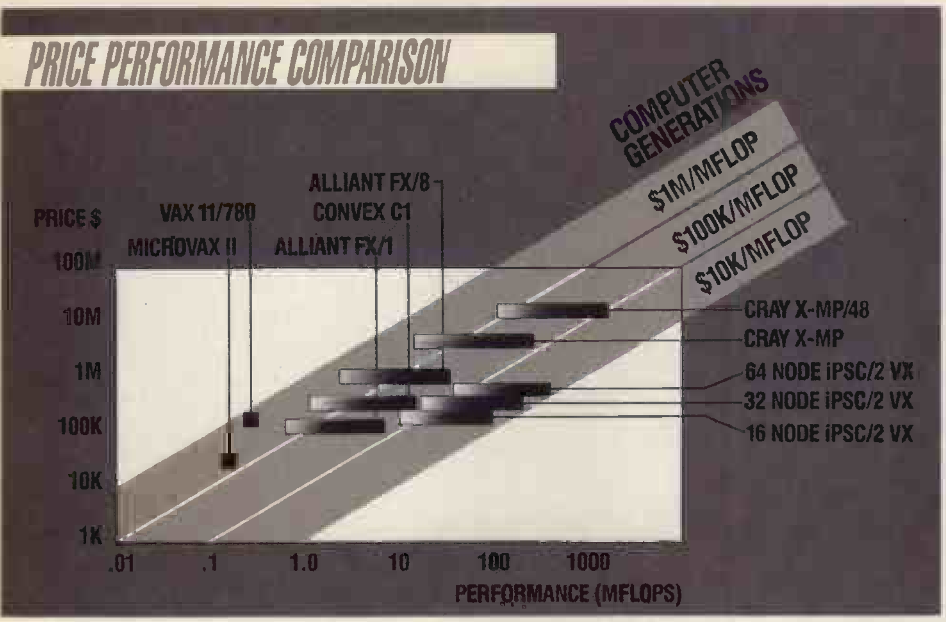
Each node in Intel's iPSC/2 concurrent supercomputer consists of an 80386 32bit processor with up to 16Mbyte of memory, and an 80387 floating-point co-processor; scalar and vector processing accelerators can be added so you can see that each node is quite a powerful computer in itself. As illustrated by Alan Clements' recent series on multiprocessor systems though, high performance within each node is only a small part of the parallel-processing problem. Most of the problem concerns providing an efficient communication path between all nodes in the system.

To get a message efficiently from one node to its neighbour is relatively easy but when a message has to travel through nodes, processing time and storage capacity are wasted because intermediate nodes have to collect the message and send it on – so-called store-and-forward communication. Within each node of the iPSC/2 however a 'Direct-Connect' interface effectively provides hardware bypass switching for every node in the system. As a result messages pass equally quickly between adjacent nodes and nodes at opposite corners of the parallel processing network, whatever its size.

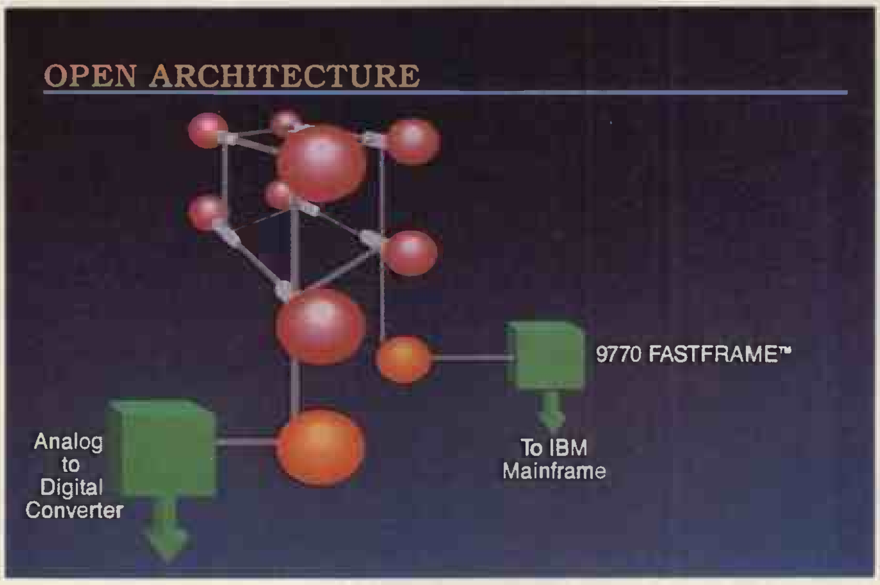
Bypass switching at the nodes takes a few microseconds but after that messages travel at 2.8Mbyte/s regardless of their destination in the network. Since each node's Direct-Connect module can handle up to eight simultaneous messages at that rate without requiring any intervention from intermediate nodes, communication between any two nodes is very fast.

Fast computing at the nodes and efficient inter-node communications result in a high-speed computer that is good at computing, but there remains a further factor – getting data in and out of the system. Processing nodes of the iPSC/2 are good at computing but they are not optimized for i/o. Directory management, request queuing, buffer handling and device control all reduce the amount of processing power available for computing.

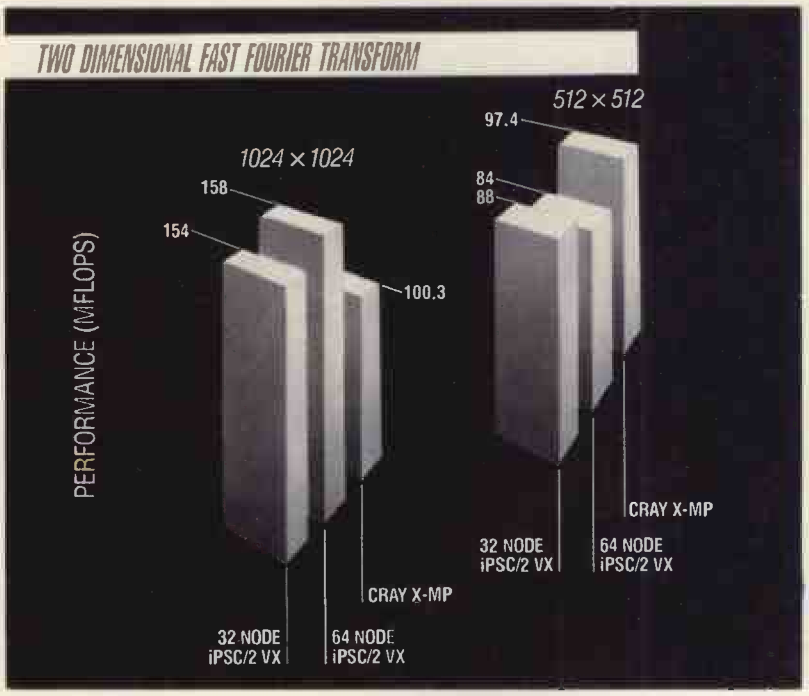
For this reason, Intel Scientific Computers has introduced hardware and software specifically for concurrent i/o handling on iPSC/2. The hardware consists of 80386/87-based modules with 4-16Mbyte of memory, a 16Kbyte cache, SCSI interfacing and parallel



This price/performance graph of vector computers indicates ranges from minimum to peak performance.



I/o nodes interface to anything from a simple data converter to an IBM mainframe.



i/o ports. These modules form nodes working on the same principles as the computing nodes, i.e. with a Direct-Connect interface, but they are optimized for i/o.

For the most i/o intensive application – data storage and retrieval – each i/o node has a 4Mbyte/s SCSI bus that takes up to seven peripherals. On the biggest iPSC/2 system, fitted with 128 i/o nodes, these SCSI interfaces provide up to 500Gbyte of disc storage. Other i/o, for anything down to a humble switch-sense input, is carried out via VME or Multibus II at up to 13Mbyte/s.

With the i/o-node hardware providing an efficient path for getting large amounts of data in and out of the computer, there still remains the problem of filing data. There's Unix of course which has the great advantage of being familiar to many engineers and scientists, but as founder and Technology Director of Intel Scientific Computers Justin Rattner points out, "Unix is not famous for its i/o capabilities."

So Intel Scientific has started afresh with a completely new implementation called Concurrent File System, CFS. Rattner says that CFS is far more comprehensive than the disc striping technique used by Cray and even improves on Sun's distributed Network File System, NFS. "With NFS", says Rattner, "you create separate files on every disc and try to make them part of one global filing directory, but the user must still partition data into all those little files."

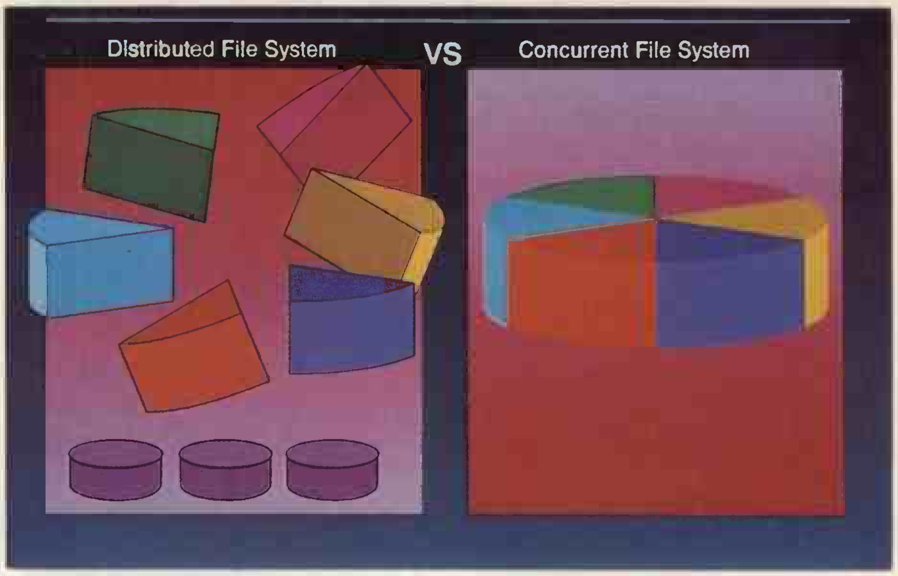
Despite the fact that the Unix V compatible CFS both supports 'studio' standard i/o library calls and has Unix-style hierarchical directory and file structures, it is different. Effectively, the user sees one disc drive, no matter how large the system. "With CFS", says Rattner, "the user creates one file and the system automatically distributes it among all available discs and channels. To the user it makes highly parallel mass storage as easy to use as any conventional single-disc filing system but it is far more powerful."

To give you an idea of where efficient i/o is important, oil searchers facing an ever increasingly difficult task are now using 3D techniques to process seismic-survey data that can total hundreds of gigabytes. Even at large seismic data-computing centres, this processing can take weeks. Fortunately, seismic data is such that it can be processed in chunks but even so the chunks still total between four and sixteen gigabytes.

Typical supercomputer centres for seismic processing require disc capacity of between 20 and 40Gbyte so that working data sets can be stored along with other data sets from tape drives. On a 128-node iPSC/2 with concurrent i/o providing 32 parallel channels for 90Mbyte/s peak i/o bandwidth to 64 760Mbyte drives, the 3D migration might take a couple of hours. A supercompu-

Two dimensional fast Fourier transform computations illustrate efficiency of the iPSC/2 communication paths. In addition to the computation at each node, the data needs to be passed between all nodes.

No matter how many disc drives are connected to the system, Concurrent File System makes them appear as one.

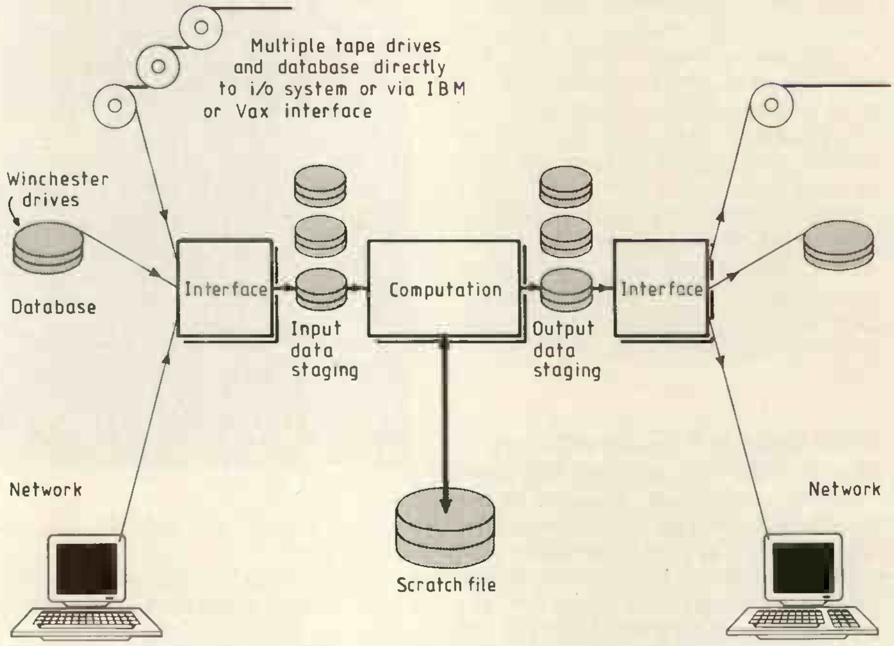


ter would take about the same amount of time but it would be accessing far more expensive disc drives.

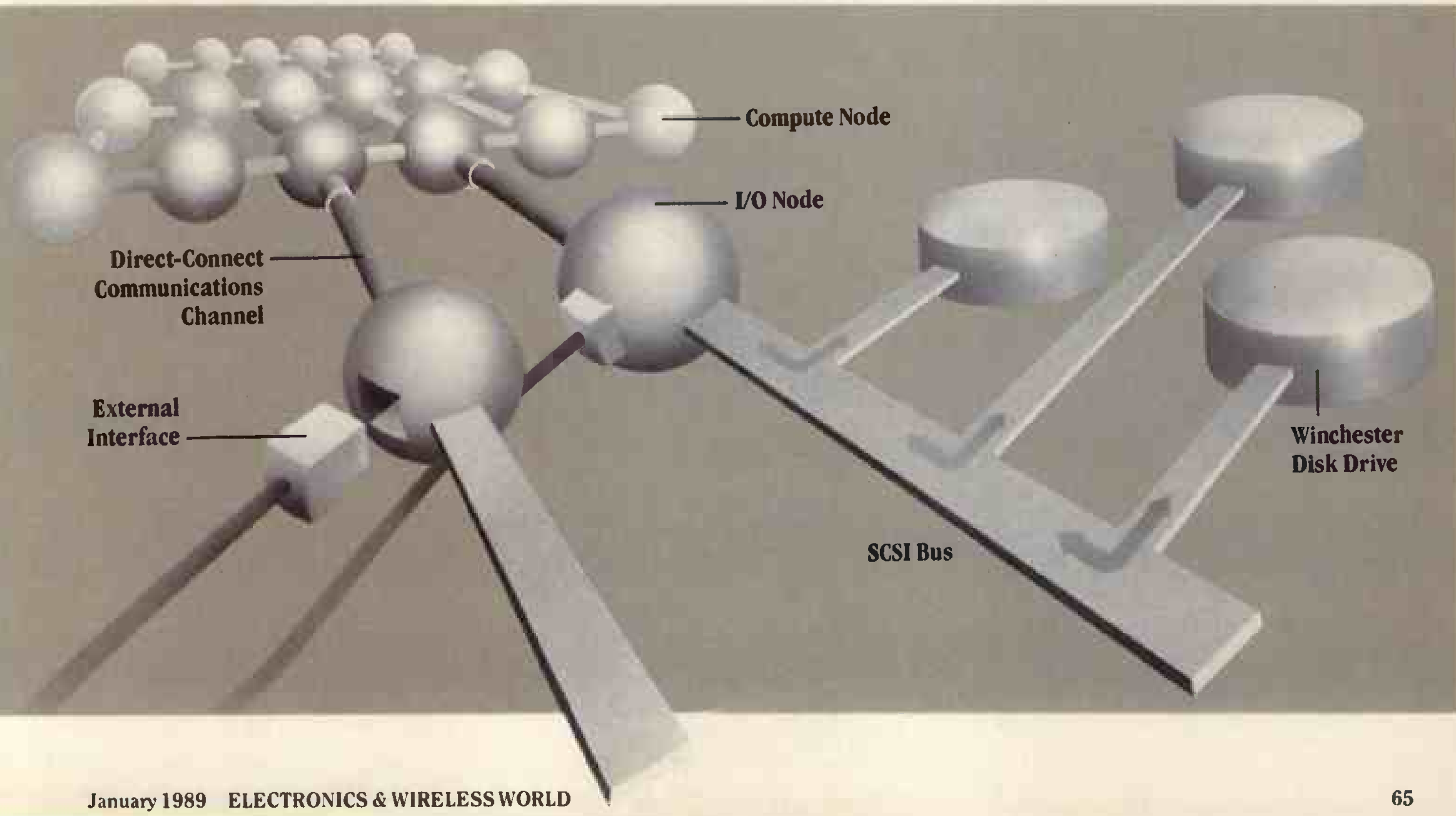
Passing data between the computer and tape drives is also a big job. More than four nine-track tape drives might be connected to the iPSC/2 SCSI buses at once. Alternatively, tape handling and much of the data processing can be done on a main frame such as the IBM 3090 via a link to the iPSC/2 via Intel's Fastpath 9770.

Seismic data processing is just one scientific application of the iPSC/2 with concurrent i/o. There are numerous other such applications where the computer is already used including fluid-flow and molecular modeling, and there are obvious applications in defence, particularly in areas requiring both numeric and symbolic processing where input data has to be processed then analysed using artificial intelligence.

But fast and efficient data processing combined with the massive amounts of fast-access storage made possible by concurrent i/o open the path for more diverse applications of the scientific computer. Suggesting new areas like financial modeling, transaction processing, data-base systems and e-cad, Intel expects the Japanese market to open up next – one interested party is a Japanese trading company.

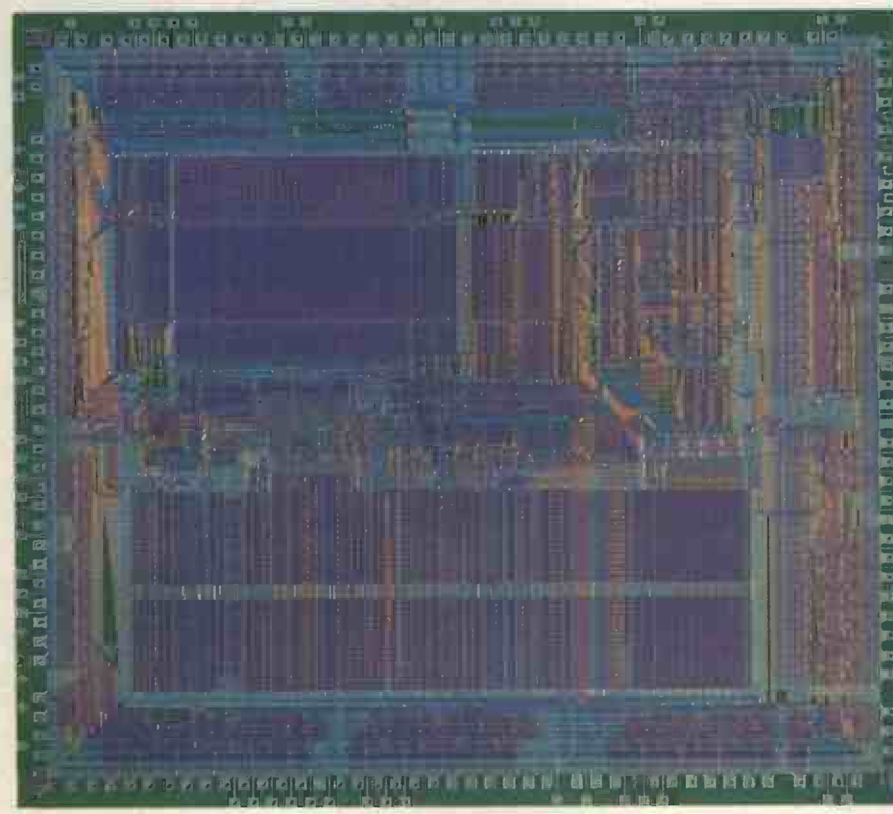


To handle the gigabytes of data involved in processing seismic data for oil exploration, efficient data i/o is needed. In this typical system, tape drives connected directly to the iPSC/2 can hold the bulk of the data or alternatively the data can be passed to and from a main frame.



Input/output nodes connect directly to any node in the system.

The risc business at Electronica



The MIPS R3000 chip as manufactured by LSI Logic.

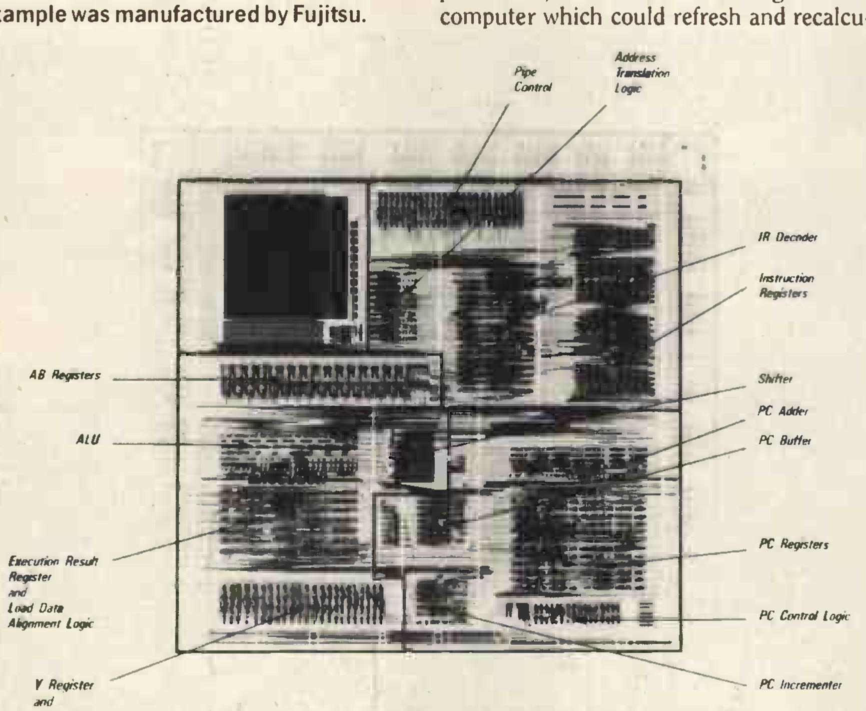
The RISC theme was very much to the fore among the semiconductor companies, if only because Intel – who wasn't at any of the 25 exhibition halls which make up Electronica – has yet to grant second source rights on the 80386 processor used throughout the IBM PC world. There was talk of RISC machines emulating the instruction set at the same rate as a genuine Intel device running at 16MHz. This would allow the 6 trillion bytes of DOS software – the dBases, Lotuses, Wordperfects and other applications for the PC – to run at a respectable speed while leaving the way clear for software which can take advantage of the blinding performance available in the new architectures.

And the performance is staggering. Ironics, a customer of AMD's 29000 series RISC processors, demonstrated a single board computer which could refresh and recalculate to a new view, a high definition 3D pixel mapped computer image in around one second without recourse to a separate floating point processor. Try that on a 386 and see how long it takes.

The Inmos parallel processor architecture represents a slightly different approach to the data bottleneck, the excessive fetching and carrying which consumes substantial amount of processing power just to keep a standard system running. It wanted to show that software wasn't a problem when using a lattice of transputers. The company wrote a complete flight simulator program in its Occam design language, a realtime application processing all associated data at 25 times per second displaying the result as the pilot's eye view. The remarkable thing about the exercise is that it took just two man weeks to write, claims the company. The demonstration was running on a total of 11 transputers with individual tasks broken down and assigned to individual groups of processors. It speaks volumes for the accessibility of Inmos technology.

LSI Logic has introduced a gate array system which holds 200 000 gates on a chip. This is the highest complexity of any array offering. It uses 0.7μm channel length to achieve this packing density. There are enough gates provided on the chip to imple-

SPARC (Scalable Processor ARChitecture) represents the other principal RISC based computer architecture. Designed by Sun Microsystems for high performance UNIX workstations, it isn't tied to particular semiconductor companies or even chip pin out. Several companies support the architecture including TI and Cypress. This example was manufactured by Fujitsu.



Fujitsu Microelectronics, Inc., Advanced Products Division's MB86901 (S-25) RISC processor provides 15 MIPS sustained performance operating at 25 MHz ment a full reduced instruction microprocessor (RISC) yet still have around 30K gates left over for housekeeping and interface. This last function normally requires a handful of chips on its own account.

The technology is also fast as one would expect from such a short channel structure. The basic two input NAND gate has a typical delay of 450ps, some 20 per cent faster than other cell based products says the company. Internal toggle rates, a good measure of circuit operating speed, can exceed 450MHz taking the technology up to the threshold of ECL performance.

HEADING FOR 40 MIPS

ASIC of this complexity is all about really high speed computing either directly for applications such as real time signal processing, or indirectly as an accelerator for the rather archaic desktop PC architecture. Director of LSI Logic's microprocessor group Brian Halla claimed that the LCB7000 would "allow the customer to combine a 32-bit megacell with 30 000 gates of random logic and more than 32K bits of RAM and 512K of ROM within a single ASIC.

"Coupling this device to a floating point accelerator chip and write buffers, he can put together a system with the performance of Cray in a laptop box."

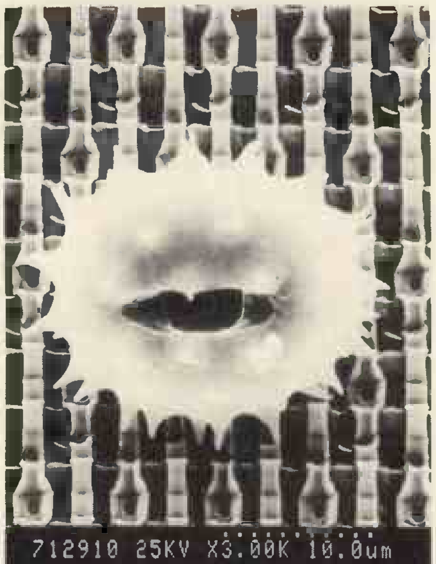
But the chip won't be cheap to work with. Halla quoted a typical non recurring engineering cost of around $250k to $350k. It takes a long time to design the linking for 200 000 gates, even using a specially enhanced version of LSI's Modular Design Environment software.

MIPS Computers, the Californian venture RISC computer company probably leads the performance field in the new architecture. Its $110 000 M/2000 machine using an LSI Logic/Integrated Device Technology R3000 RISC processor with associated floating point R3010 chip claims a performance improvement of 17 times over that of a DEC MicroVAX II. According to IDT the 32-bit chip set performs a sustained rate of 20 millions of instructions per second at 25MHz clock rate. An Intel 80386 performs in the region of 4MIPs for the same clock speed. IDT and partners are already working on an R4000 version combining the CPU and floating point unit on a single chip. It hopes to see performance between 35 to 40MIPs for the part.

The R3000 includes on chip CPU, memory management, cache controller, 512K of instruction and data caches and other housekeeping. The chip measures almost half an inch on a side.

Siemens production of 1MB DRAM chips is now running at around 1 million chips per month. To increase the efficiency of its production process it has reduced the chip size from 54 to 45mm. In common with other semi component companies, Siemens is using DRAM development as the driving force technology in other areas. It expects to see chip sizes as large as 500mm^2 by the mid 1990s used for ISDN and digital television chips. 4MB generation memory chips are already in sampling using 0.8μm design rules on a total chip area of 91mm square.

Motor control isn't glamorous but an extremely important semiconductor application never the less. Think of the applications requiring precision motor control: disk drives, video recorders, printers, auto-



The picture shows the 1μm structures on Siemens' latest 1MB DRAM chip compared to a pollen grain.

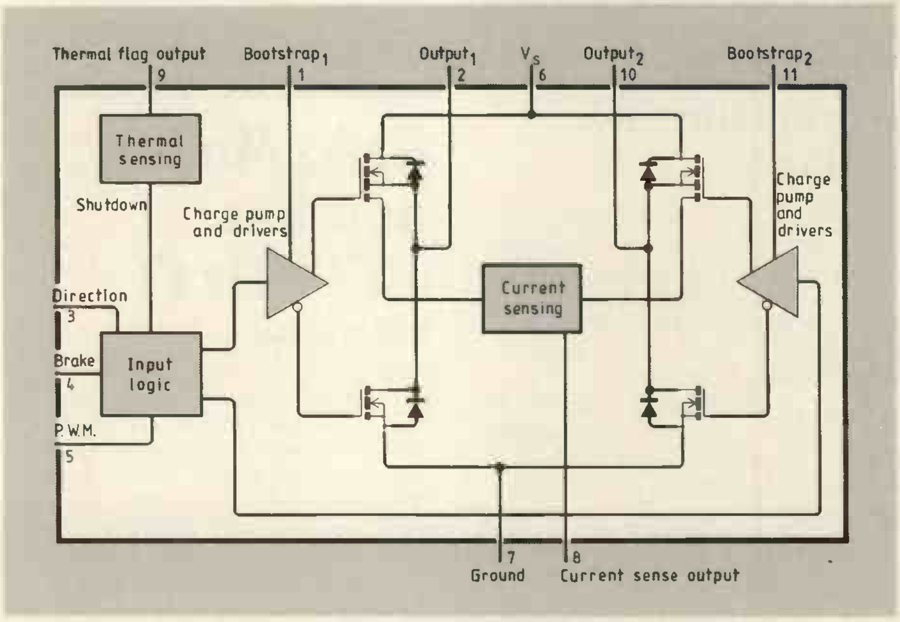
WHAT IS RISC?

It stands for reduced instruction set computer. It actually refers to a microprocessor type structure with a much higher program execution speed than standard microprocessors, for instance the entire Intel family of general purpose processors or Motorola's 68 series.

Conventional micros (CISC or complex instruction set computers) require every instruction involved in a particular task to be spelt out for them in a series of micro instructions. Each move of data between registers requires an individual instruction which in turn requires a full clock cycle in which to execute. This results in simple tasks such as register to register transfer taking up a considerable number of clock cycles.

The RISC approach is to use the transistor packing density available in modern CMOS semiconductor processing to create parallel data paths through the chip and register duplication where data bottlenecks would normally occur. The net result is that most tasks can be executed within a single clock cycle, speeding up the overall program execution time.

Because things happen faster in RISC, between five and ten times faster, the architecture places great demands on memory speed and organisation. RISC system builders make extensive use of fast static RAM cache holding both data and instructions in a bid to keep up with the processor.



Block diagram of the "bullet proof" NS/IR 8200 H bridge motor control chip.

motive, etc. National Semiconductor and International Rectifier have got together to produce an H bridge motor control circuit which is "overload protected, over current protected, thermally protected, overvoltage protected and bullet proof" both parties claim.

The switching elements are four 0.3Ω power mosfets integrated onto the same chip as the logic control circuit. Each switch transistor has an associated power diode to take up the back EMF of the switching process. Neither does it require any snubbing network. Unusual for cmos the device uses avalanche breakdown to absorb spikes greater than its nominal maximum rail voltage of 55V. It claims to be latch-up free.

It comes in a standard multilegged plastic power package.

Electrically reprogrammable gating

Think of the system design options which would occur if a standard architecture microprocessor could talk to its program and user memory, peripherals and the outside world through a gate array which could be reconfigured at will, under program or external interrupt control.

Smart peripherals could load their own data directly into memory without tying up the CPU. The CPU could automatically reconfigure the gate matrix into an I/O device with changing characteristics according to the task under execution. Instructions held centrally in ROM could be channelled through temporary data paths to other processors within the system for parallel processing applications. A reconfigurable gate array could change itself into the digital part of a modem.

All this and more is on offer with the Electrically Programmable Array, a Plessey manufactured product designed by a firm of independent consultants. The ERA comprises an array of NAND gate cells and programmable interconnect repeated across the chip. The input and output connections of every gate are controlled by programming data inputs to the gates on the chip by an overlay static RAM, the individual cell outputs of which either enable or disable the associated gate. Writing to the overlay RAM has the effect of programming the gate array function. The configuration can thus be stored in system ROM or derived interactively from data produced elsewhere in the system. Because the configuration is based on RAM it can be changed as fast and as often as the system requires.

This chameleon like ability allows the ERA to perform hardware protocol conversion. Adaptive recursive filters and encryption applications can exploit the facility by self learning. Adapting part of the array can be done without affecting the function of the rest. The same design thinking could be used to make a fault tolerant system.

The first devices will have a gate complexity around the 10k mark using a 1.4μm three layer CMOS process. Typically around 40 per cent of these would be usable at any one time. Future geometry reductions will allow 20k gates/chip.

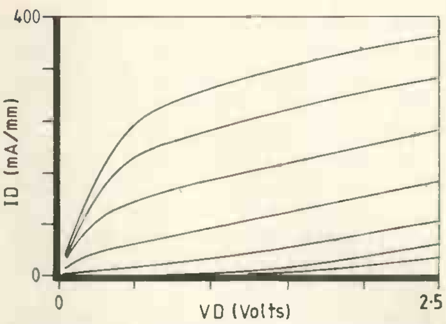
The use of ERA type devices holds out interesting advantages. It supports hierarchical methods and shares the flexibility of gate arrays. It isn't necessary for the ERA designer to learn different design methods from those acquired with ordinary gate arrays. It also gives a non destructive learning tool. Parts using the technology will be available early next year.

GaAs Modfet now has 123 GHz fT

Martin Eccles

Recently, researchers at Siemens and Cornell University, have independently improved on their 113GHz Modfet, which they had developed jointly, taking its f_T to 123GHz and 122GHz respectively. These devices have not only the highest f_T of any GaAs fet, but are also capable of producing the highest maximum frequency of oscillation; according to Dr. Erhard Kohn, one of the scientists involved in the project, technological optimization for highest f_T and highest maximum frequency of oscillation, however, do not necessarily go hand in hand.

Electron-microscope scan of a recessed and lifted-off gate cross section. The process achieves a minimal ungated recess region.



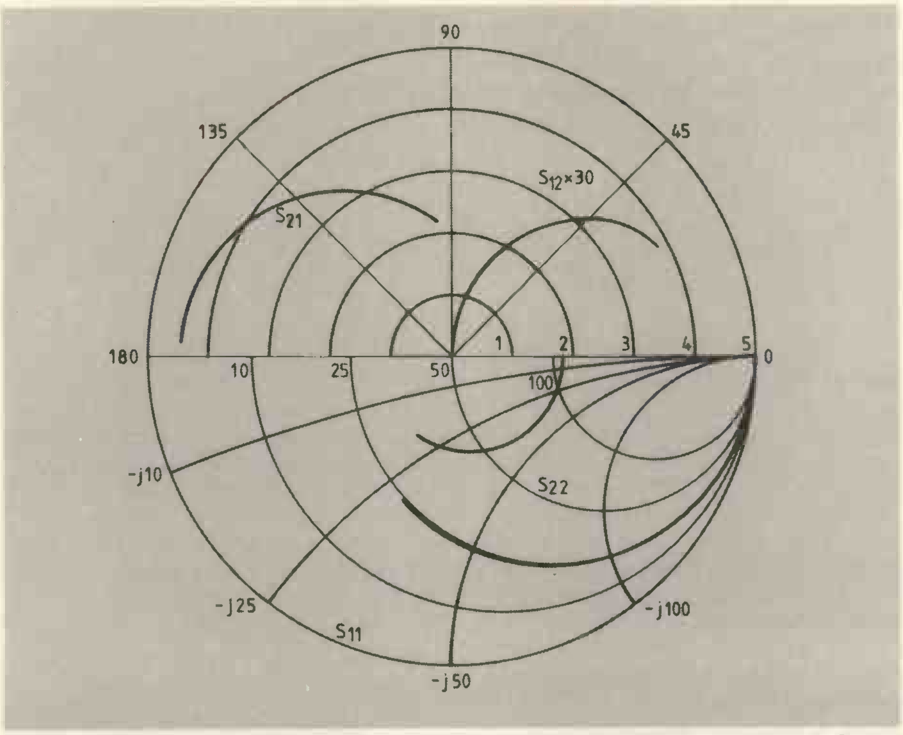
Typical current/voltage characteristics with d.c. drain for a 100 hm by 150 μm T-gate Modfet.

Fast Modfets find applications in millimetre-wave radar, satellite communications and astronomy, where the devices are cooled to obtain extremely low noise, and there has recently been interest in using them in millimetre wave power amplification. When asked when the devices might be manufactured on a large scale, Dr. Kohn said that this type of device is already in pilot production. Professional applications for which the devices are best suitable are still few – presently, one 3in wafer will probably supply the millimetre-wave radar and satellite communication needs for a year.

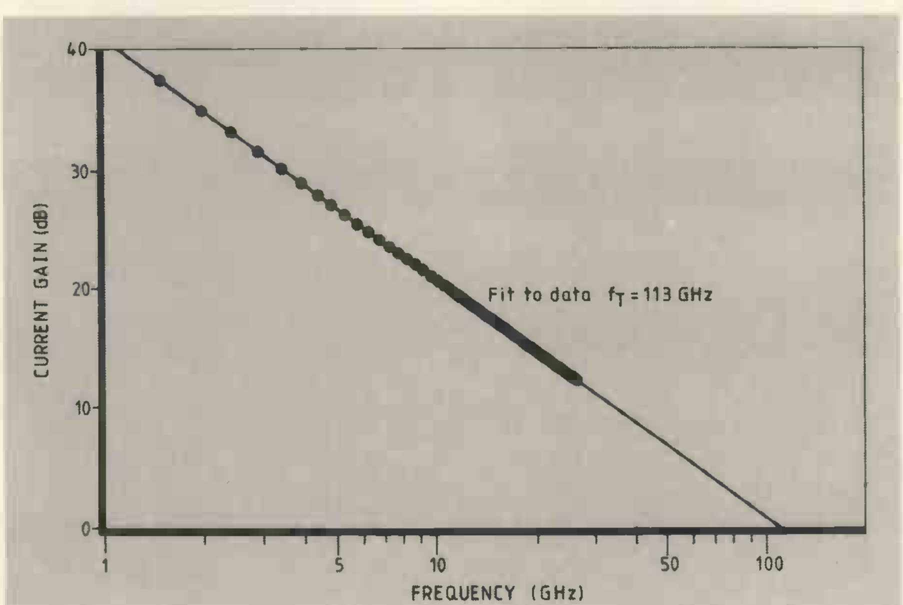
Dr. Kohn added that this type of Modfet is very interesting for 12GHz satellite broadcat receivers, but these need not to have the extremely small gate length of 0.1 to 0.2μm as the devices mentioned above. Millimetre-wave radars will become more widely used first in military systems and one could foresee mass production of the devices and microwave monolithic circuits with these devices in the near future. The breakthrough in speed is significant for the future; up to now only diodes have been available for frequencies around and above 100GHz.

Demonstrating improved microwave performance over the GaAs Mesfet, now these Modfets have the advantage of higher electron mobility and higher saturation velocity. Their cut-off frequencies, say the reearchers, are over 50% higher than any previous AlGaAs/GaAs Modfet and higher than any other type of GaAs fet.

To achieve the 113GHz unity current-gain cut-off frequency in late 1987, AlGaAs/GaAs 'modulation doped field-effect transistors', or Modfets were made using a T-section gate of 100nm length – the equivalent of about



Measured S-parameters from 0.05 to 26.5GHz for the 113GHz T-gate Modfet. Drain-source voltage is 1V, gate-source voltage is −0.3V and drain-source current is 29mA.



300 atom layers of gate metal. Introducing quantum wells (wells of the size of that of an electron wave) of strained (i.e. lattice-stressed) indium-gallium-arsenide into the material has stepped up the frequency to 123GHz even when using a 30% longer gate. Dr. Kohn calls these faster devices "Pseudomorphic Modfets".

Fabrication of the 'spike-doped' devices is essentially done by molecular beam epitaxy and the extremely short gate length is accompanied by a very thin active material structure which is tailor "grown" by molecular beam epitaxy; nanometres thin extremely highly doped layers (so called spike doping) allow a gate-to-channel separation of only about 25 nm, which avoids 3D effects even at the shortest gate length.

Earlier 100nm-gate Modfets made using single-level resist techniques had given state-of-the-art performance, but they had not shown the f_T improvements expected in relation to the previous 250nm gate-length Modfets. The T section gate was the clue to the increased performance.

When used to reduce gate length to 250nm or smaller, conventional single-level electron beam resist techniques reduce capacitance and increase transconductance but they compromise microwave performance since the smaller gate cross section causes excessive parasitic gate resistance. Forming a T-section gate improves performance by maintaining a small gate footprint without causing a high gate resistance. In making the gate, a multi-layer electron beam resist system was used to form resist profiles suitable for lifting-off 100nm-footprint gates with more than 250nm wide tops.

Resulting devices have a peak intrinsic transconductance (gm) of 810mS/mm at almost 200mA/mm current, and a threshold voltage of −1V. The new pseudomorphic HEMTs have larger current drive capability and the peak g_m is maintained up to over 300mA/mm.

Life above 30GHz

Views are sought by the Department of Trade and Industry on the use of the radio spectrum above 30GHz. As occupancy of the lower frequencies becomes ever more intensive, future expansion of radio services will increasingly depend on the exploitation of the relatively under-used millimetre waves. In a 40-page consultative document, the DTI's Radiocommunications Division sets out its present understanding of the potential of millimetre waves and their associated technology and poses some of the options for their exploitation by the industry.

Examples of services which could be established in this region are short-range television (including systems such as the television distribution service described this in month's Television Broadcast column); very fast data transmission; cordless PABXs (see also page 1198); electronic funds transfer at point of sale (cashless shopping with "intelligent cards"); line-of-sight communication between neighborouring buildings; and mobile services such as portable telephones and route guidance for vehicles.

With 1992 in mind, the DTI needs to harmonize its plans with those of Britain's European partners; and one of the purposes of the consultative document is to enable the UK administration to construct its case to the European forum.

Copies of the document are available from the Radiocommunications Division of the DTI, telephone 01-215 2072.

Expanded or extended memory?

Eight years after the introduction of the PC by IBM there is still an ocean of confusion on the difference between expanded and extended memory. This is the definitive statement.

ROGER PHEBEY

IBM initially designed its first PC around the Intel 8088 microprocessor, and while this device had the capability to address directly 1MB of memory, IBM decided that it would reserve 384K of this memory area for special purposes, such as BIOS, video-adaptors, hard-disc controllers and terminal emulation adaptors. This left 640K (1MB-384K) of memory which could be used by DOS, application programs and user data. This 640K of memory is known as Conventional Memory. **Fig. 1** illustrates the memory configuration of an IBM PC.

The 640K limit of usable memory is often referred to as the 'DOS Barrier'. But strictly speaking it represents a hardware limitation imposed by the designer of the PC and the 8088 processor. Users of application programs such as Lotus *1-2-3* began to discover that limiting working memory to 640K prevented the creation of enlarged data files.

In 1985 Intel and Lotus created an Expanded Memory Specification (EMS) which enabled PCs to access an additional 8MB of memory. Later that year Microsoft joined Intel and Lotus and the Expanded Memory Specification was amended to be compatible with all future versions of DOS. The standard was then set at version 3.2.

Expanded memory is accessed using a bank-switching technique. When the Expanded memory card is installed, a 64K non-initialized block is allocated within the memory area above 640K, ie, that reserved for BIOS and adaptor cards. This 64K block is then used as an address window, through which a much larger memory arranged as pages can be accessed. **Fig. 2** illustrates how Expanded memory is accessed. The analogy is a small computer screen view of a much larger spread-sheet.

Lotus released versions of *1-2-3* and *Symphony* to make use of Expanded memory, while Intel developed a family of Expanded memory cards known as the *Above-Board* range.

Expanded memory is often referred to as LIM (Lotus/Intel/Microsoft) memory, or EMS (Expanded Memory Specification) memory. It can only be accessed by the application of programs designed specifically to make use of Expanded memory. Currently most of the professional business packages support Expanded memory and it has become a *de facto* industry standard. Some of the more popular programs which can benefit include:

1-2-3, Framework, Excel, Paradox, SuperCalc 4, Symphony, Windows 2, Smart and AutoCAD.

In 1983 IBM announced the PC/AT which made use of the Intel 80286 processor. This microprocessor is capable of running in two modes. Firstly, Real Mode, which is the mode utilised by DOS, permitting direct access to 1MB of memory (the same as for the Intel 8088 microprocessor). The other mode is Protected Mode, which enables direct access to 16MB of memory. This aspect will be dealt with later.

The same memory limitations imposed by

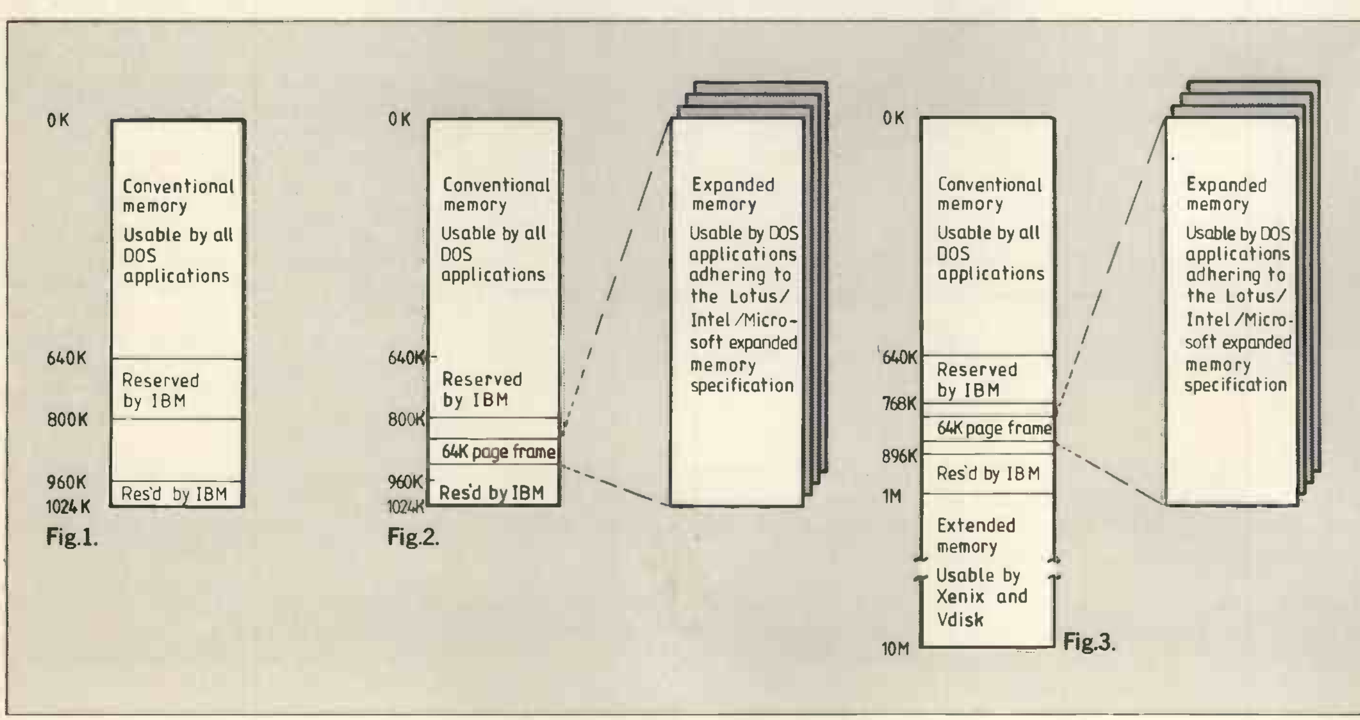


Fig.1. Fig.2. Fig.3.

the hardware constraint found in the original PC, exist within the PC/AT and likewise the new 80386 PCs. Hence, the only way to break through the 640K DOS barrier is by using Expanded memory cards.

Shortly after Intel, Lotus and Microsft announced the EMS specification, AST together with a few other manufacturers released another memory expansion specification known as Enhanced Expanded Memory Specification (EEMS). The EEMS was a superset of the LIM-EMS supporting all the features of EMS, but with several extra options. Most EMS programs run exactly the same on both EMS and EEMS memory expansion cards. However, a few, including Quarterdeck's *Desqview* and Digital Research's *Concurrent DOS* made use of the extra features offered by EEMS.

In August 1987, LIM announced a new version of the EMS, Version 4.0. This version is a vast improvement over the original Version 3.2 in two main areas. Firstly, it enables up to 32MB of Expanded memory, instead of the 8MB available with the earlier version.

Secondly, Version 3.2 allowed only data to 'reside' in Expanded memory, whereas Version 4.0 allows both data and programs to 'run' in Expanded memory. Version 4.0 allows programs written for Version 3.2 to operate normally. However, new programs such as Microsoft *Excel* and Lotus *1-2-3* release 3, will only make use of Version 4.0.

Many manufacturers supply the new Expanded Memory Manager Drivers free of charge to existing users of Expanded memory cards, enabling them to make use of EMS Version 4.0. AST and other supporters of EEMS immediately confirmed their support for the new LIM-EMS Version 4.0 in preference to the EEMS, so now the entire PC industry is unified. Future software and hardware developments will now support the industry standard, EMS Version 4.0.

The Intel 80286 can be run in Protected Mode which enables it to directly address up to 16MB of memory.

Several operating systems run 80286 and 80386 microprocessors in Protected Mode, thereby benefitting from the extra memory they can address. The most frequently used operating systems are OS/2, UNIX and Novell's Advanced NetWare 286. The extra 15MB (that memory above the standard 1MB) is known as Extended memory. In fact, these three operating systems can only use Extended memory and can't run Expanded memory. **Fig.3** represents a memory map of an 80286 or 80386 system, showing where the Extended memory resides.

It is important to remember, that if a user is currently specifying DOS, with the probable requirement in the future for Expanded memory, then memory-cards which provide for Expanded and Extended memory should be considered. This criterion is equally relevant should the user decide at a later date to change to another operating system, such as OS/2.

Roger Phebey works for Micro Marketing (Electronics) Ltd

After fibre optics, optical broadcasting?

With coherent optics, routing in a fibre-optical telecommunication network could be achieved passively simply by tuning at terminals

GEOFFREY SHORTER

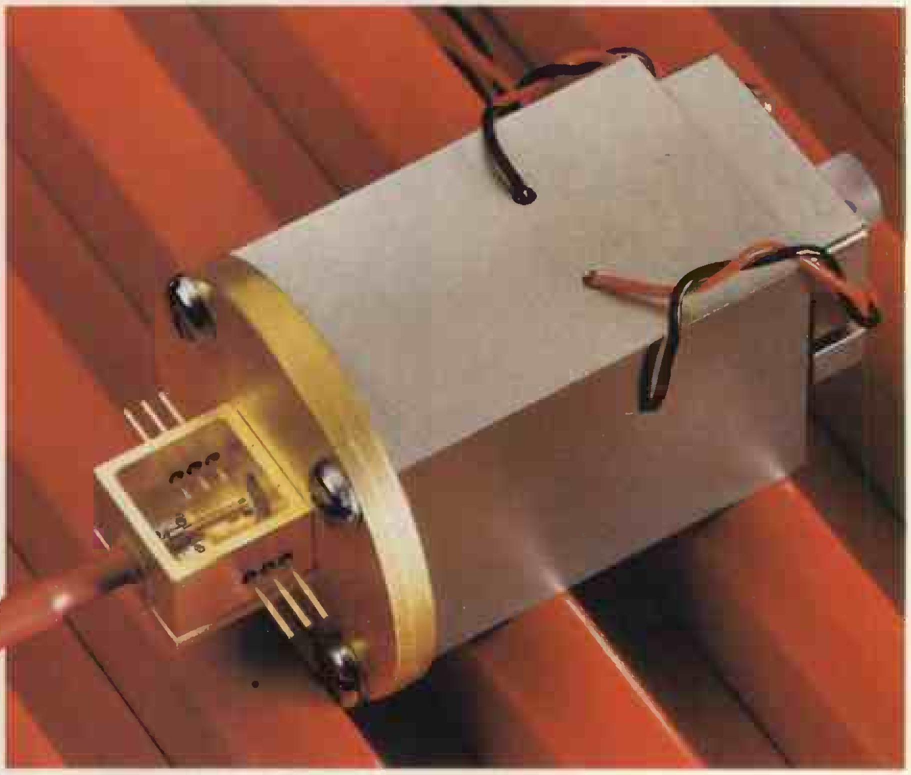
To complement the reductions in transmission cost that optical fibre systems have brought about in the last decade future networks could well operate without the relatively expensive electronic switches presently used for routing traffic. They would be replaced by passive optical nodes, and routing would be achieved by wavelength selectivity, much as used in radio systems communication.

The idea is that all signals would be broadcast to all terminals in a network; a channel is established by wave length regardless of geographic location of the terminals. Obviously such a scheme would require tunable devices working in a coherent environment and, in addition, some kind of optical amplifier to avoid the noise and cost penalties of electronic regenerators.

Research establishments around the world are presently perfecting components for coherent systems, and the originators of this particular idea of a broadcast telephone network, at British Telecom Research Labs forecast that for both local area use and long-haul applications such networks will probably be demonstrated within the next five years.

But before that, the existence of over 400,000km of laid single-mode fibre will mean that wavelength-multiplexed coherent systems can be installed very simply, leading to at least a ten-fold increase in transmission capacity.

BTRL themselves have made significant strides at both device and system level, and recently demonstrated their achievements with a 565Mbit/s coherent system in operation over 176km of fibre – believed to be the first yet for a coherent system in an operational environment – and over 230km in the laboratory (see panel).



Packaged long external cavity laser developed by BTRL for coherent systems.

WAVELENGTH MULTIPLEXING

The idea of wavelength division multiplexing in fibre systems has been around for over a decade, but it has not been widely adopted because of the dependence on electronic signal regeneration, which must be provided separately for each wavelength channel. And since the loss through the optical multiplexers must come out of the optical power budget, the result is little if any net saving in cost.

This situation could be transformed by the advent of low-noise optical amplifiers, which could amplify many wavelength channels simultaneously in a single photonic device and hence remove the electronic bottleneck from the transmission path. These could immediately provide bit-rate transparency in conventional intensity-modulated systems, but extension to multi-wavelength transmission could result in crosstalk between channels at high power levels, where the modulation of the optical power level on each channel would modulate the amplifier gain for all other channels. Coherent transmission techniques based on angle modulation do not involve power fluctuations, so they may provide the key to using optical amplifiers to the best advantage and allow more amplifiers to be cascaded.

COHERENT SYSTEMS

In the conventional or direct detection method of handling received signals from an optical fibre, receivers respond to the amount of optical *power* in each transmitted pulse, and suffer three kinds of limitation. Span is limited by thermal noise in the receiver, spacing of separate-wavelength channels is limited by the resolution of optical filters, and the ability to amplify several wavelength channels simultaneously limited by crosstalk.

In contrast, the operation of a coherent system is based on the use of an optical sinewave whose phase, frequency, or amplitude is modulated to carry the transmission.

At the receiver, the message is recovered by reference to an unmodulated optical local oscillator with nominally the same carrier frequency. The received signal and local laser fields are combined in an optical coupler, and the photodetector responds to the square of the vector sum of the combined electric fields. This squaring process mixes the two signals, yielding a photocurrent with a component centred at the difference frequency between the two carriers, and whose amplitude depends on both the received signal level and that of the local laser. Close channel spacing is possible since the receiver responds only to optical signals which mix down within the electrical passband of the receiver. Improved signal to noise ratio follows from local oscillator gain: the electrical signal increases with local laser power, and this gain can be used to offset the thermal noise of the receiver.

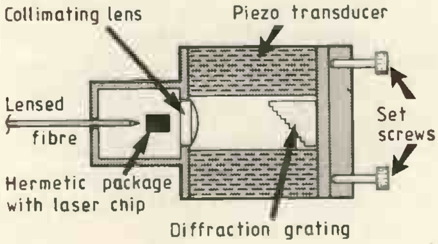
Also, since angle modulated waves are not affected by the crosstalk mechanism that applies to amplitude or intensity modulated signals (non-linearity in optical amplifiers at high power levels) it should be possible to transmit more channels through a larger number of amplifiers using coherent techniques than for direct detection, with the promise of very high capacity transmission over many hundreds of kilometres.

BTRL's experimental work during the early 1980s showed that near-quantum-limited performance could be achieved for a variety of modulation formats in a series of experiments at 140Mbit/s and below using HeNe and long external cavity lasers and commercial low-noise pinfet receivers. AT&T Bell Labs report results for dpsk systems at higher bit-rates using external cavity lasers and wider bandwidth receivers, and setting records in distance bit-rate product. In Japan, similar record breaking results were reported using lasers based on the dfb structure for fsk systems. At BTRL the effort has been concentrated on solving the problems associated with field operation, and in particular, the demonstration of automated endless polarization control in a 565Mbit/s system, and a new lithium niobate transducer.

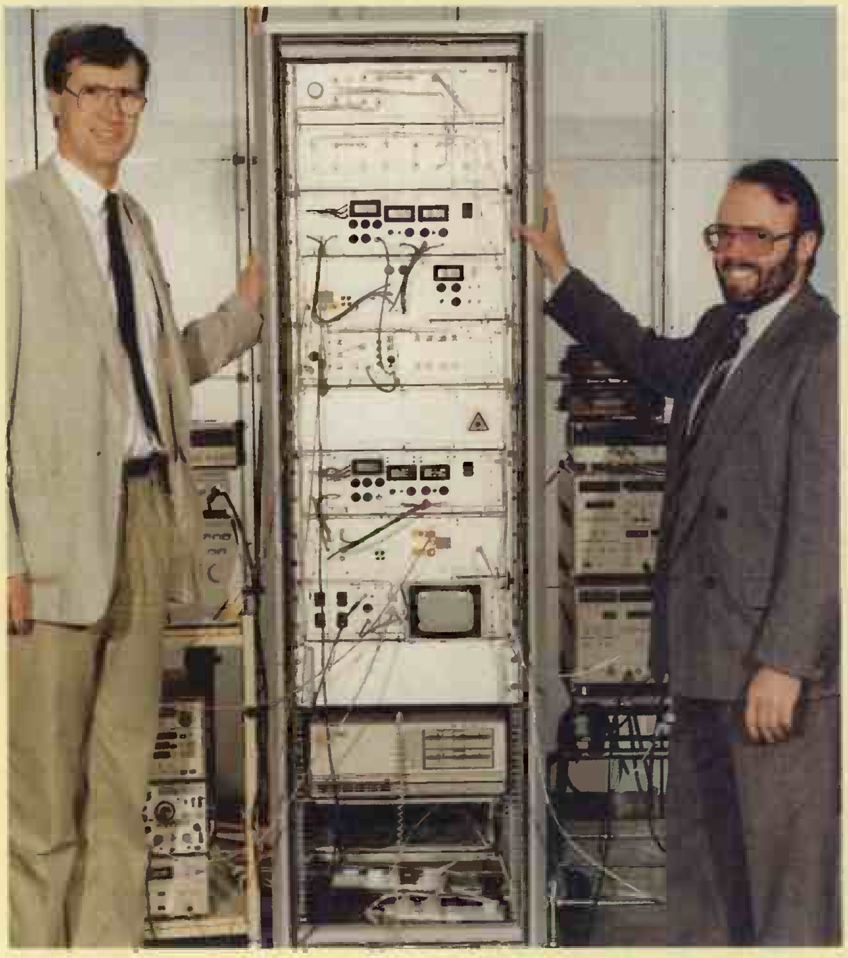
So, in a telecommunications network, coherent detection offers longer spans between terminals in the short term, more wavelength channels on the same fibre in the medium term (using optical amplifiers as multi-wavelength repeaters), and the possibility of passive routing through the network in the longer term. This suggests less equipment and greater reliability in the network, fewer electronic bottlenecks in the optical path, and greater transparency for the user.

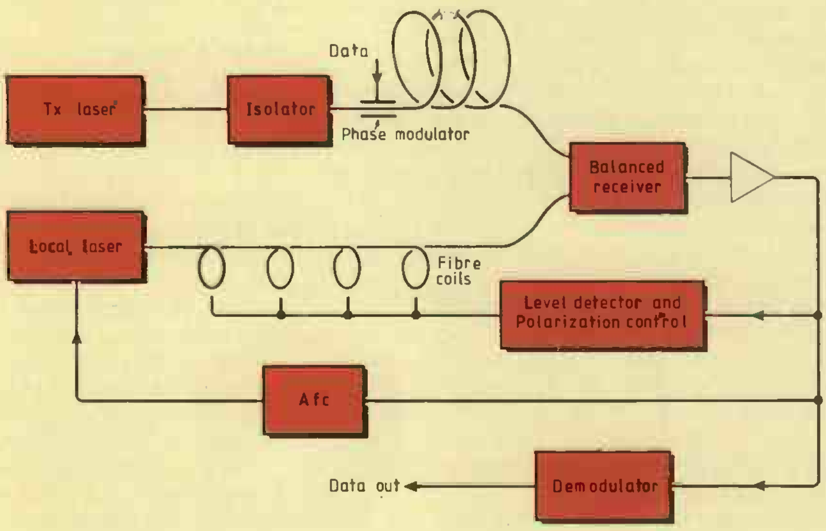
LASER SOURCES

The prime requirement in coherent systems is for a single-mode laser source with narrow linewidth and continuous wavelength tuning, for use at both the transmitter and as local oscillator in the receiver. A type widely used is the long external cavity laser – using a relatively simple laser chip with one facet anti-reflection coated, coupled via a collimating lens to a diffraction grating, shown below. The chief difficulty has been in getting reflections suppressed over a sufficiently wide range of wavelengths. Such assemblies tend to be sensitive to vibration, but Mike Brain and his team at BTRL have successfully miniaturized and ruggedized the assembly to make it suitable for use outside the laboratory. Its wavelength is adjustable over 40nm, continuously over 0.4 nm (50 GHz) with spectral linewidth of less



BT's demonstration installed at the trunk exchange in Cambridge operated at 565Mbit/s using differential phase shift key modulation and heterodyne detection. The transmitter comprised a miniaturized long external cavity laser developed at BTRL, followed by a single 30dB optical isolator. Differential phase shift key modulation was applied to the optical carrier by a lithium niobate phase modulator, and the optical signal power boosted by a semiconductor laser amplifier to a level of +1dBm in the single-mode fibre before transmission through 176km of conventional single-mode fibre contained in an 18-fibre cable installed between Cambridge and Bedford. The receiver, also located at Cambridge, comprised an lec laser as the local oscillator source, an automated endless polarization controller also developed by BTRL, a fused tapered fibre coupler to combine the signal and local waves, and a wideband receiver with an optically-balanced input. Loss of the 176km of fibre was almost 0.3dB/km: lower incremental losses in cabling and installation could allow repeaterless link lengths approaching 250km – as achieved in the lab – whilst further development of devices and components could extend this to 300km, or alternatively provide margin for error-free operation. Spans of this order indicate a capability to link cities without repeaters.





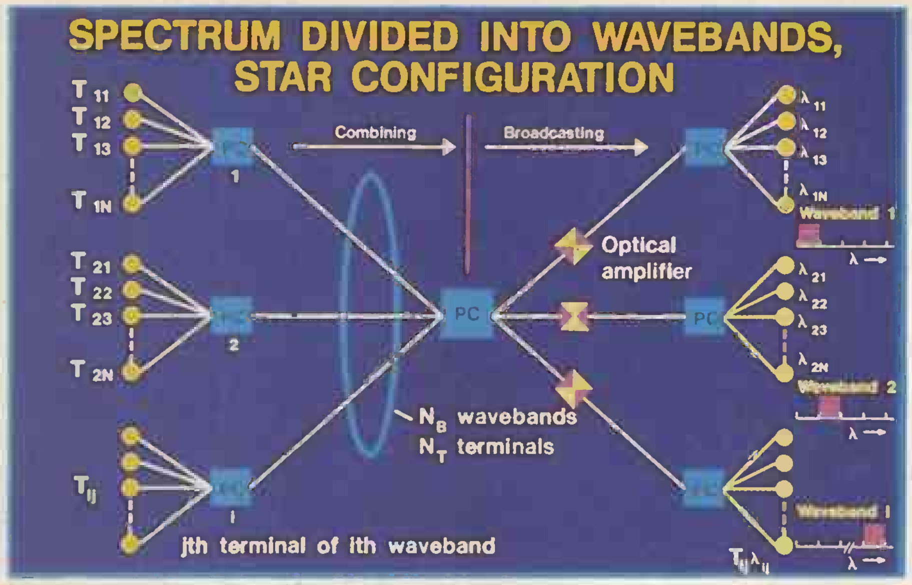
than 100 kHz, and an output power of 0dBm. It requires less than 30 dB of optical isolation, which can be provided outside the package, but BT say further work is needed to examine its mode stability over the long term, "Initial tests using temperature stabilization are very encouraging", says Mike Brain.

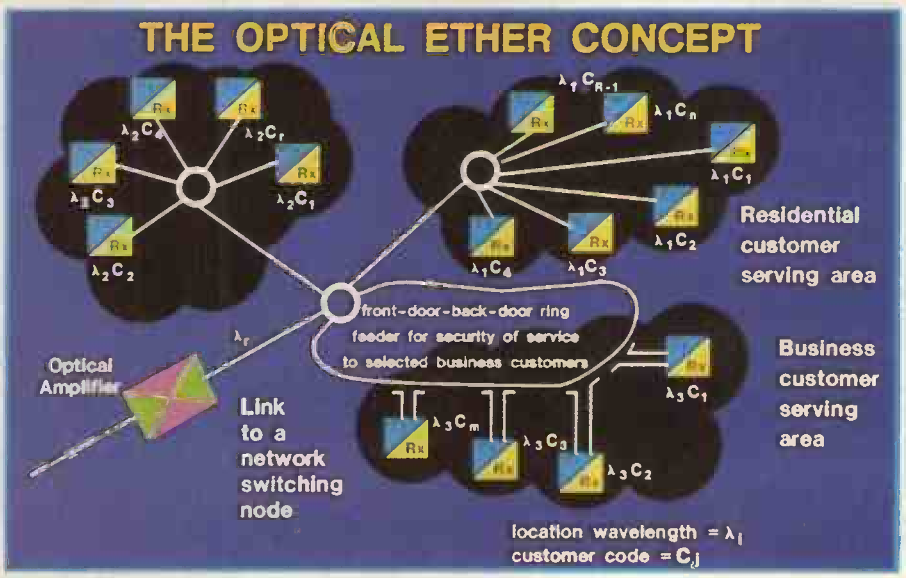
An alternative approach is the distributed feedback laser which has a grating incorporated alongside its active region to provide both optical feedback and frequency selection, and so does not suffer from this potential problem of modal instability. It is far more sensitive to optical reflections which spoil the spectral purity (coherence) of the optical carrier, and needs at least 60 dB of optical isolation close to the output facet, which represents a complex packaging problem. It also requires a more complex chip structure than the external cavity laser to remove phase nonlinearities. And as the wavelength is defined by the material composition, matched pairs for the transmitter and local oscillator are difficult to provide at present.

There are also phase non-linearities associated with frequency modulation applied via the drive current.

There are other approaches under investigation, but BT's development of the lec laser has provided the first laser source suitable for coherent transmission in the operational network environment.

A further innovation in the BT field demonstration was the inclusion of an optical power amplifier as the output stage of the transmitter to overcome the losses in the isolator and modulator and to boost the power launched into the fibre. This allowed the distance between the repeaters to be increased, with no significant penalty to the sensitivity of the receiver.





POLARIZATION MATCHING

The second requirement is for a means of ensuring that the states of polarization of the received signal and the local oscillator are matched. BT wishes to use the conventional single-mode fibre that is already installed throughout the network, but changes in stress or temperature can alter the polarization state of the transmitted signal.

One approach is to provide a polarization-diversity receiver that responds to the transmitted signal regardless of how it is polarized. Such receivers require optical components which are only just becoming available – polarization beam-splitting fibre couplers and polarization-maintaining fibre couplers, for example – and may also involve optical loss and sensitivity penalties.

As an alternative, BTRL have provided a means of adjusting the polarization of the local oscillator to track that of the received signal with unlimited tracking range, using two types of transducer. The field demonstration used one based on polarization-maintaining fibre wound on piezoelectric cylinders, which requires a mechanical strain of only 10^{-4} to produce the required change in state of polarization.

Routing traffic through this 'optical ether' offers great flexibility, as wavelengths are associated with particular terminals rather than geographic locations. Also, unlike the radio ether, the optical ether is enclosed by a guiding medium, so additional capacity can be added through further ethers, without mutual interference. Longhaul transmission is catered for by providing optical amplifiers as simple multiwavelength repeaters. The question is, how many channels can be provided, and over what distance?

POWER BUDGET

Assuming 565Mbit/s channels, spaced at 10GHz (0.08nm) intervals, suggests 500 wavelengths in an optical amplifier passband of 40mm.

Next consider power budget. The maximum output power level for the optical amplifiers is divided between the alloted wavelengths to yield the power/channel. Each fibre section incurs a transmission loss which is equalled by the gain of each optical amplifier, and each amplifier contributes to the quantum noise on the signal, and adds an amount of excess noise. The maximum number of amplifiers in cascade is determined when the noise floor has been raised by succeeding amplification stages to yield an snr which is only just acceptable. The total gain in the system is then equated to the transmission losses to yield a maximum separation between terminals.

From preliminary calculations, it emerges that low fibre loss, low amplifier noise, and high amplifier output power contribute to network capacity and range, but so does low amplifier gain. Nevertheless, for a network of 250 terminals operating at 565Mbit/s, a separation between terminals of up to 1000km could be expected, using fibre with a loss of 0.2dB/km, and amplifiers with 15dB gain, 1mW output power, and an excess noise factor of 2. Greater capacity (or margin) could be accommodated by lower amplifier gain (though 10dB would still yield 50km repeater spacings) or higher output power.

Further work is needed, BT say, to provide reference wavelengths and distribute them throughout the network. Multi-access protocols will also be needed. The example may not represent the performance of the ultimate network, but the technique has the potential to simplify routing both for long-haul communications and, if coherent technology can be made less expensive, in computer and local loop network applications.

Thanks to Mike Brain, head of coherent optical systems at BT Research Labs, for help in the preparation of this article.

Cacheing in the chips

Ian Wilson of Intel describes how cache memory allows low-cost dynamic rams to be used in high performance systems.

Since its introduction in October 1985, the 80386 microprocessor has become one of the industry's most widely used 32bit microprocessors. The 80386, fabricated using Intel's 1μm CHMOS IV process, can be clocked at up to 25MHz, with a 33MHz version becoming available in 1989. It can perform a bus transfer every two processor clock periods – every 80ns at 25MHz – providing a raw bus bandwidth of 50Mbyte/s.

The challenge that high speed processors such as the 80386 present to designers is how to design a memory system that does not introduce an excessive number of wait states such that most of the 80386 performance is lost.

For designers to get the maximum 80386 performance from their systems it is necessary to turn to the design techniques used in supermini design. One technique that needs to be adopted is the use of a cache memory system. High performance 80386 systems, especially those using the 25MHz and future 33MHz 80386, will need to use a cache memory system to be cost effective. Intel's 82385 cache controller is a vlsi companion device to the 80386 that implements cache control functions and a cache directory on a single device.

The idea behind a cache memory system is to provide a memory system that has the performance of fast static rams but at the cost of slower dynamic rams. A cache is a small amount of very fast memory that sits between the cpu and main memory. The size of the cache is typically 16Kbyte to 64Kbyte and the cache holds a copy of frequently used code and data.

The cpu can access the cache memory with a zero wait states access. It is pointless to use a high performance cpu like the 80386 with a slow memory system that causes the cpu to execute a lot of wait states.

CACHE EFFECTIVENESS

The effectiveness of a cache memory system depends on the so-called "principle of locality". This is based on the observation that once a memory location is accessed it is highly likely to be accessed again in the near future. This means that once data for a given memory location is in the cache subsequent accesses to the same memory location only need go to the cache. Obvious common examples of this are program loops and access to local variables and parameters within procedures.

Each time that the cpu makes a memory access the cache memory controller looks at the address put out by the cpu. It compares

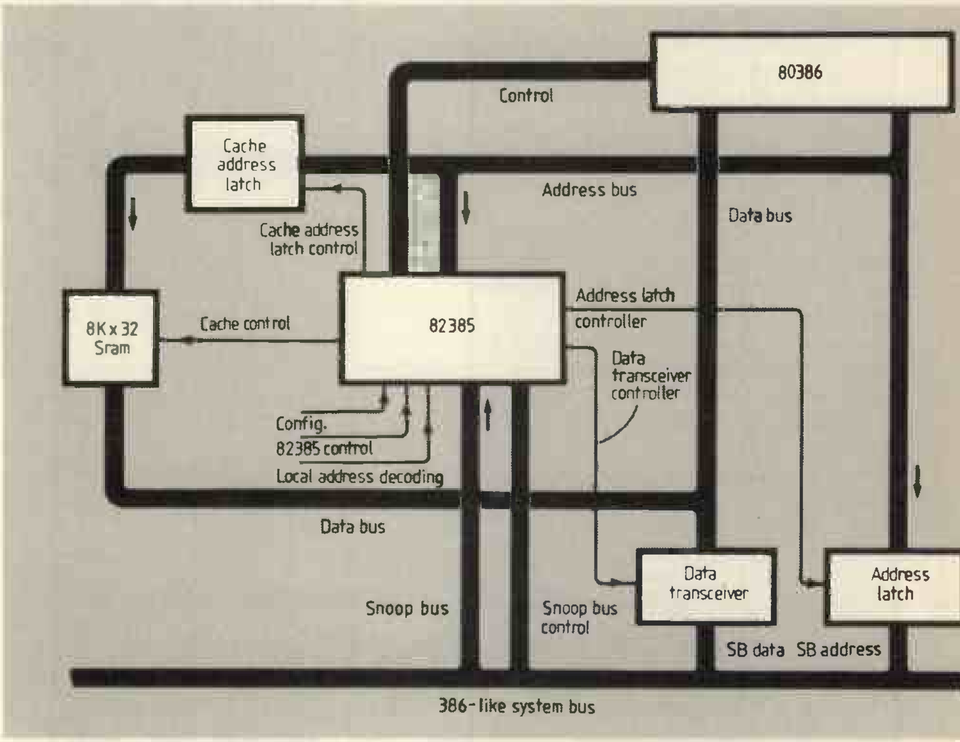
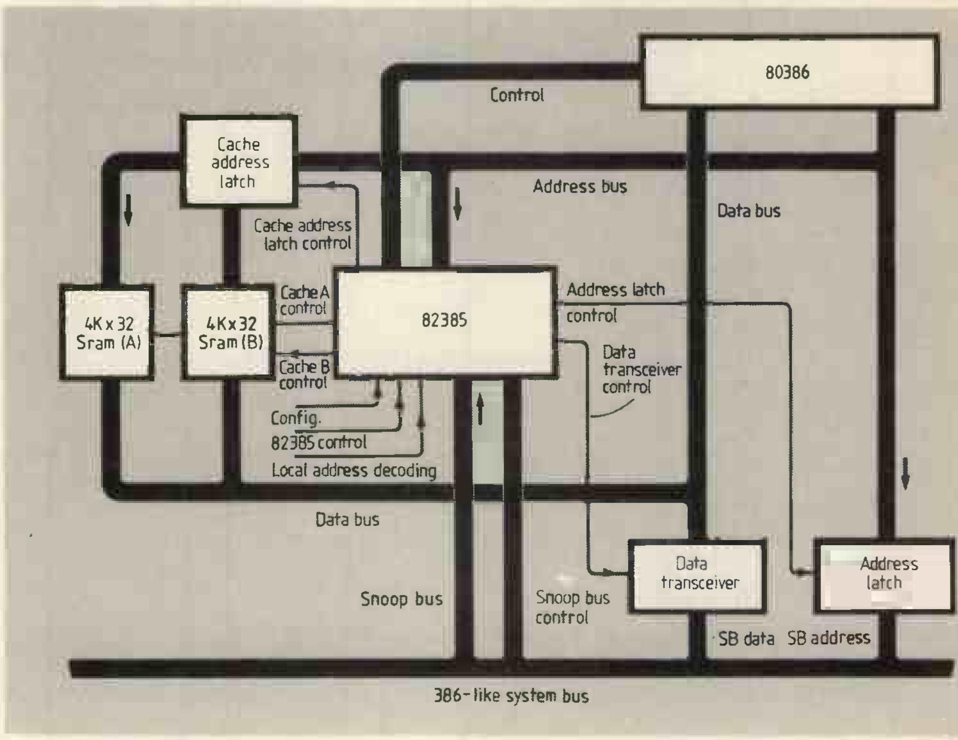


Fig.1. In direct-mapped cacheing – the simplest method – data for a given address can only occupy one particular entry in the cache.

Fig.2. A fully associative cache allows any memory address to use any cache entry, but the logic required to do this is complex. A good compromise is the two-way set-associative cache shown here.



this address with a list of addresses, or "tags", that identify memory addresses that have copies of data in the cache. If it finds a match, a cache "hit", then it directly reads or writes the data in the cache and the bus cycle finishes without any wait states. On the other hand if the current address does not match any tag, a cache "miss", a slow memory access must be made to main memory.

Normally on a miss the cache is updated so that the new address is added to the tags, and the new data is entered as the data corresponding to that tag. This means that the next access to the same address will only need to go to the cache.

Using a cache, a designer can implement a 25MHz 80386 system with say 8Mbyte of memory using commodity dynamic rams, say with 100ns access time, but still provide very close to zero wait-state performance. To implement the same system without a cache and to get the same performance would require 8Mbyte of very fast and very expensive static ram. With a 25MHz 80386 cpu this would require fast static rams with access times of less than 35ns.

Given the cost of fast static rams this would only be a practical solution for systems requiring a small amount of memory, typically less than 1Mbyte. Many systems that use 32bit microprocessors require several megabytes of ram.

Using a cache, a designer can implement a 25MHz 80386 system with say 8Mbyte of memory using commodity dynamic rams, say with 100ns access time, but still provide very close to zero wait-state performance.

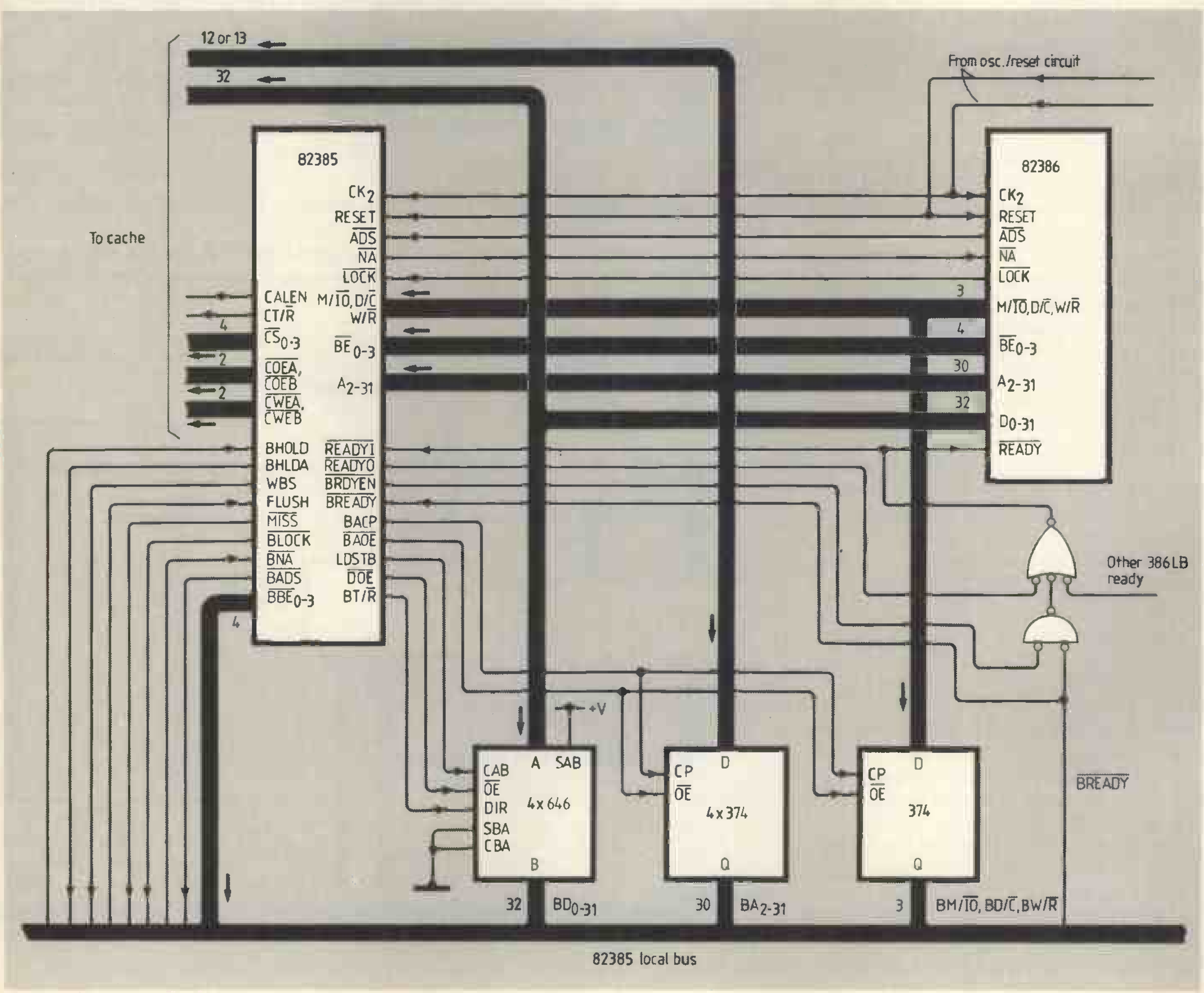
An ideal cache would give the same system performance as a zero wait-state memory system, but a real cache will obviously give somewhat lower performance. The performance of a cache memory system depends on the cache hit rate and the cache management policies. The cache hit rate is simply the ratio of cache hits to the total number of cpu bus cycles. The ideal situation is a hit rate of 100% where all bus cycles only need go to the cache, but this is obviously impossible. Practical cache implementations give hit rates in the range of 80%-95%. Cache management policies determine how write cycles and cache coherency are handled and can influence the system level performance of a particular cache implementation with a given hit rate.

A number of factors influence the hit rate. Firstly the size of the cache; the bigger the cache the higher the hit rate, but also the cost of the cache increases. A cache the same size as the main memory, say 8Mbyte, would obviously give a 100% hit rate but would defeat the object of having a cache! Caches are normally larger than 8Kbyte and rarely larger than 256K byte.

Secondly the transfer block size can have an important effect. The transfer block size is the unit of transfer between main memory and the cache when a cache miss occurs and typical values would be 16, 32 or 64bit. For a 32bit processor such as the 80386 the normal value is 32bit.

The third factor that can influence the hit rate is the organization of the cache. According to way in which the cache memory is organized, different methods are used to map the address put out by the cpu to the corresponding cache entry which holds the

Fig.3. Interfacing between the 80386 and 82385.



data for that address. There are two ways of organizing a cache. The very simplest is known as "direct mapped". Here the data for a given address can only occupy one particular entry in the cache. If the size of the cache is say 32Kbyte, then locations in main memory separated by multiples of 32Kbyte all use the same cache entry. This can cause what is known as "thrashing" where there is contention for the same cache entry.

FULLY ASSOCIATIVE CACHE

At the other extreme there is a fully-associative cache where a memory address can use any cache entry, but the logic required is very complex. Effectively a comparator is needed for each cache entry and typically there are 16K to 32K entries. A compromise is an n-way-set-associative cache where n is typically two or four. In this case a given memory address can use n possible cache entries so the chances of thrashing are reduced. The logic required is much simpler; only n comparators are needed, n being the number of ways.

Cache management policies can have a dramatic effect on the system performance of a cache. A cache controller must maintain "cache coherency"; that is, the copy data in the cache must be in step with the corresponding data in the main memory.

Write cycles present a particular problem. Suppose that the cpu does a write cycle to an address in main memory and the data at that address has been cached. If the write cycle just updates the cache the cpu write cycle can complete in zero wait states, but the cache coherency problem would have now arisen. The copy of the data in the cache would now differ from the data in main memory. If the entry in the cache were reused to hold the data for another main memory location, the new data for the old memory location would never have been written into main memory.

There is a number of solutions to this problem. The simplest approach is to have a write-through cache where on every write cycle that is a cache hit both main memory and the cache are updated. The problem with this approach is that every write cycle is penalized by the number of wait states incurred in going to main memory. In measuring the performance of the cache it leaves a residual number of effective wait states that cache size cannot decrease.

A better solution to this problem is to adopt a "posted write through" policy which ensures that main memory is updated on every write cycle but without a decrease in performance. In this case the cache is always updated on a cache hit write cycle, and main memory is updated on every write. But the write into main memory takes place asynchronously with the cpu's activity. So the write into the cache can take place with zero wait states and the cpu can start another bus cycle. Meanwhile the slower write into main memory can still be taking place. The cpu will only see wait states if two write cycles occur back to back, or if a read miss follows a write cycle. This technique removes most of the performance degradation caused by write cycles.

In cases where main memory is shared with other bus masters another policy decision has to be made. What should be done when another bus master, for example a dma controller transferring data from a disc into ram, updates a main memory location that has been cached? To do nothing would lead to the cache coherency problem.

Flushing the entire cache each time another bus master writes into main memory would ensure cache coherency, but would have a severe impact on performance. An effective policy is to adopt "bus watching" where the system address bus is monitored by the cache controller and if another bus master writes into a main memory location that is cached, the corresponding cache data is marked as invalid, thus ensuring cache coherency. Next time the cpu wants data from that address there will be a cache miss and it will go to main memory to get the new data and update the cache with the new data for that address.

APPLYING THE CACHE CONTROLLER

Implementing a cache memory system can be costly both in terms of logic and components. Intel's 82385 cache controller aims to maximize system performance by reducing cpu wait states and system bus accesses, but also to reduce costs by minimizing the amount of external logic and components required. It integrates into one device all the cache control logic and cache tags. All that needs to be added to the 82385 are the cache data rams and a small number of buffers and latches.

The 82385 is closely coupled to the 80386; it runs synchronously with the cpu and resides on the cpu's local bus. The 82385 supports 32Kbyte of cache memory with either a direct-mapped or two-way set-associative organization. The full 4Gbyte physical address space of the 80386 can be cached.

Figs.1 and **2** show a block diagram of a 386/385 system for direct mapped and two-way set-associative configurations. The 80386, 82385 and cache memory can be regarded as a "super-cpu" core. To the rest of the system this store looks just like an 80386 with the same signals on the 82385 local bus as on the 80386 local bus.

The discussion above highlighted the problems of cache coherency. The 82385 supports a posted write through policy and bus snooping to maintain coherency. The latches for the address and control signals and the latching transceivers for data between the 80386 local bus and the 82385 local bus are controlled by the 82385 and support the posted write feature (see **Fig.3**). While the 80386 has started another bus cycle to the cache, the control, address, and data signals are held on the 82385 local bus until the cycle to main memory has completed.

In order to implement the cache memory for a 25MHz 80386 system 25ns or 30ns static rams are required. The choice of rams depends on whether a direct mapped or two-way set-associative organization is being used, and also depends on the timing parameters of the chose static rams. All cache hit bus cycles run by the 80386 are non-pipelined zero-wait-state bus cycles. These are the fastest possible 80386 bus cycles. Supposing that 100ns dynamic rams are used for the main memory in a 25MHz 80386/82385 systems, and that the cache hit rate is 90%, then the effective number of wait states for this system will be about 0.2. This compares to two wait states if the cache was not present, and represents only about a 4% reduction on full zero wait state 80386 performance. Actual applications using the 82385 should show hit rates in the range 85-95%.

Intel's 32 bit computing-platform components enable designers to implement full 32bit 80386 systems that fully exploit the power of the 80386. The first generation of 80386 products did not deliver the full performance of the 80386 at the system level. The second generation of 80386 products now emerging are using devices such as the 80387 and 82385 cache controller to provide a substantial performance increase over the first generation products.

REED NATIONAL MANAGEMENT GAME

Reed Business Publishing, publisher of *Electronics and Wireless World*, and Nicklin Advertising are to sponsor the ICL/Cranfield Management Game.

Retitled The Reed National Management Game, it provides competing teams with the opportunity to run a computer simulated manufacturing company pitting their skills against other teams in a fiercely competitive marketplace.

A large ICL mainframe computer holds the model, one for each participating team, allowing individual management decisions to be fed into the model. The computer sets up the changing market environment and feeds back the effect of management decisions to the teams. The team with the most profitable model at the end of the game wins. The teams, which normally comprise between three to six people face decisions on capital deployment, interest rates, variations in product demand, R&D spending, exchange rate fluctuations and the like.

The first round of the game is conducted on a regional basis with winners qualifying for the grand final taking place in September, 1989.

The game has been in existence for some years and the 1988 game attracted more than 400 entries from all sectors of British industry and outside. Last year's winners were a team of teachers working in London's East End. The new sponsors hope to attract at least 2000 teams with a total of 10,000 managers involved. Entry to the game costs £250 per team but there are no other bars.

Teams wishing to enter should write to ICL-Cranfield Business Games Ltd, Cranfield School of Management, Cranfield, Bedford MK43 0AL before December 24.

Hewlett-Packard 4951 protocol analyser for 19.2 kb/s data communications.

Test gear – rent or buy?

Pride of possession might conceivably seem out of place in an electronics laboratory, but it appears to be one of the main objections to renting instrumentation. What are the others and how soundly based are they?

In company with estate agents, dental surgeons and undertakers, companies offering test gear for hire seem to have found an infallible method of surviving reasonably well regardless of the current state of the economy. Clearly, to do that they must be satisfying a need in the industry at least as well as those who sell equipment. Hiring must be attractive even to the larger users. Why?

Electronic test equipment can occupy, in companies of almost any size, a disproportionate amount of "dead" capital. Test gear used in manufacture and calibration, admittedly, earns its keep by contributing to production and revenue, but the equipment that spends its life in spasmodic employment in a research or development laboratory is often under-used, out-dated, space-consuming and quite possibly not in a fit state for instant use when the need arises – an expensive piece of shelf-furniture. Company accountants loathe and despise test gear.

A recent estimate put the amount of test equipment currently in the possession of UK industry at around £M250-£M350. It is almost impossible to estimate how much of that is being used in anger, as opposed to the stock of instruments mouldering away, waiting for a call to action. Some equipment will be the earthly remains of a long-forgotten development project, while the rest has been made obsolete by rapid change in the design of instrumentation; the life of t and m gear is currently around five years and is decreasing all the time.

THE ATTRACTIONS

The imperatives which direct a user towards the renting of equipment are, in general, to do with cost and performance, while the objections are more concerned with attitudes.

Finance. At around 10-12% of the purchase price per month for short periods or 6% per month for a year, rental cost compares favourably with outright purchase which, taking into account interest, depreciation, maintenance and time out of action, can amount to over 50% per year.

Utilization. If one makes a decision to acquire a piece of equipment, the decision is obviously made in response to an immediate requirement; but needs change, and often rapidly. At the end of the requirement, the instrument might not be needed again and can be returned if it is rented. Further, if a piece of equipment is going to be used for only a small percentage of the time, rental is probably economic sense, assuming that the rental companies can guarantee to deliver it promptly when it is needed.

Tektronix 2445 (cost new £2999)	1	4	12	13	24	26	52
Microlease	82.65	82.65	78.3	65.25		56.66	39.15
Technirent	85	85	66	66	66	59	43
Hamilton	81	73	61		53		
First Rental	87			69.6		60.9	
Instrument Rentals	84	80	63		55		42
Livingston	87		65		61		

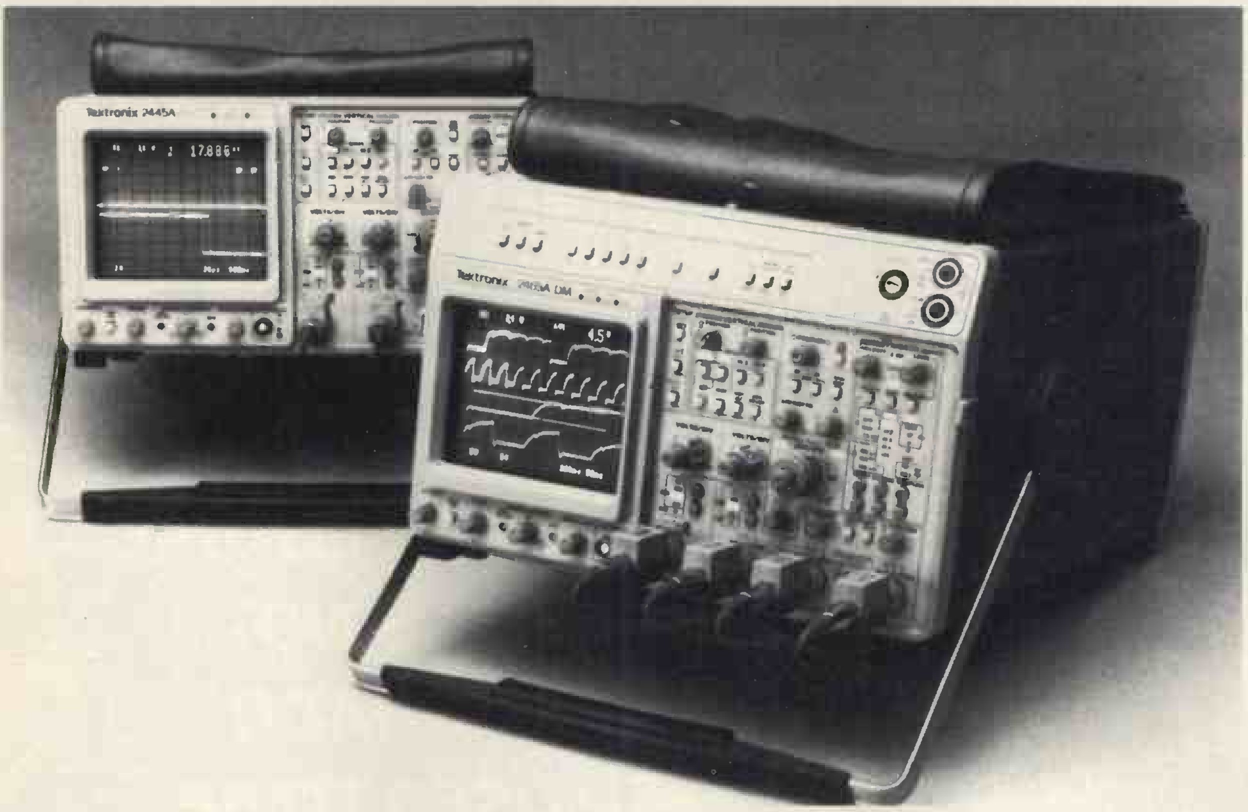
Hewlett-Packard 4951B (cost new £3752)	1	4	12	13	24	26	52
Microlease	119	118.75	112.5	90		81	56.25
Technirent	105	105	82	82	82	74	53
Hamilton	94	84	70		61		
First Rental	124			99.2		86.6	
Instrument Rentals	99	94	88		76		49.5
Livingston	117		88		82		

Evaluation. Where several instruments with similar specifications are available, there is not alway a clear-cut choice between them; short-term hire will provide the evidence to make the final decision on expensive equipment, leading either to long-term rental or purchase.

Peak demand. When every engineer in the department inexplicably discovers an overwhelming need to use the only logic analyser in the building, outright purchase of another three is unlikely to be the most economical method of satisfying the demand. Indeed, by the time the orders have been raised and passed through channels and the manufacturer's delivery time elapsed, the engineers have probably either borrowed analysers or found a way round the problem.

Quality. If company policy is against the renting of test gear, a small company must deny itself the use of higher-priced equipment and larger companies may find the price of the more exotic instruments difficult to justify. Renting removes much of the difficulty, particularly for short periods. Capital outlay is avoided. One advantage of renting, therefore, is that small users have access to expensive equipment that would otherwise be completely out of the question.

Maintenance. In a large organization, whole departments can be devoted to the maintenance and repair of test equipment; two or three salaries, the overheads of any department and material cost must be supported. On the other hand, rental companies routinely provide a free repair service, the only "cost of ownership" being the rental fees of the equipment. In extreme cases, the instrument is replaced, quickly.



Tektronix 2445 4-channel, 100MHz oscilloscope, left.

Obsolescence. Assuming a five-year write-off period, it is likely that an instrument would have reached the stage of obsolescence long before its value was written down to zero on the books. Clearly, the problem is avoided if the instrument is rented: it is simply returned in exchange for a later one. If it is the property of the user, he is effectively either stuck with the obsolescent instrument or is saddled with yet another purchase.

Costing. Knowing the cost of equipment in advance eases the problem of costing projects.

Shorter periods. It is clearly uneconomic to buy expensive gear for one job and then allow it to gather dust.

THE OBJECTIONS

In the main, the most frequently heard opposition is that the test equipment ceases to be a company asset. This is a point of view that may have some validity, but since the asset is a depreciating one it is not a strong argument. There is also some truth in the assertion that there is security in possession; to have available all the equipment to be used in the foreseeable future does remove some of the possibility of running out of time in a contract because the test gear is on a long delivery time or has broken down. To counter this argument, the rental companies can point to their record in high-speed delivery.

It is also pointed by one company that, in the case of the 4951 protocol analyser, non-standard protocols could be a problem that only the manufacturer would wish to cope with. If the instrument were to be rented, delays might therefore ensue.

The decision on whether to rent or buy rests on costs; all the above considerations contain a core of financial reasoning. In the tables, costs of renting from six companies are shown; they are all of the same order, but vary slightly, depending on the equipment and on the number of months rental period. The picture is confused a little by the fact that the companies quote different price breaks at different periods, but all are ready to give prices for other periods.

Leasing, as an option, is often mentioned. This is effectively a longer-term hire than the ordinary rental agreement, at lower rates, but the rental companies are strangely reluctant to discuss it. Leasing rates are fiendishly complicated to work out and the impression gained is that it is not often used. A variant of leasing is the "sale and lease back" process offered by Hamilton, in which a user can turn some of the capital tied up in test equipment into cash by selling the gear to Hamilton and leasing it back for use. No figures for this are provided in the catalogue.

Microlease, First Rental, Hamilton and Instrument Rentals all offer the "purchase option" agreement, whereby an instrument is rented for long enough for the user to decide that he does actually need it, after which he can decide to buy it outright. Between 25 and 30% of the rent paid is credited against the purchase.

THE COMPANIES

Livingston Hire is one of the oldest companies in this field, being formed from an older company 21 years ago. It claims to have more than 9 000 users in the UK and more than 16 000 individual items of test equipment in its inventory. Livingston Hire Limited, 2-6 Queen's Road, Teddington, Middlesex TW11 0LB. 01-977 8866.

ATS TechniRent Limited is a seven-year-old company, covering the whole of the UK with deliveries. ATS TechniRent, Park House, The Pavilions, Downmill Road, Bracknell RG12 1QS. 0344 411011.

First Rental Limited have recently acquired the rental division of Electroplan Limited and have moved to new premises. First Rental Limited, PO Box 19, Newark Close, York Way, Royston, Hertfordshire. 0763 47251.

Instrument Rentals (UK) Limited is a wholly owned subsidiary of the American US Instrument Rentals, 1988 being the 21st anniversary of the company's appearance in the UK. IR recently took over the assets of Electronic Brokers, which was well known for its new and used equipment sales. Instrumex, which is part of IR, now handles equipment sales. Instrument Rentals Limited, Dorcan House, Meadfield Road, Langley, Slough, Berkshire SL3 8AL. 0753 44878.

Hamilton Rentech is a division of Hamilton Rentals, which is a subsidiary of the British company Atlantic Computers plc. Hamilton Rentech Limited, Hamilton House, North Circular Road, London NW10 7UB. 01-965 2772.

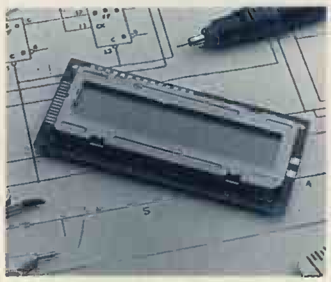
Microlease plc, in spite of the name, is a rental company. "It's either in stock or we can get it for you" is the claim. Microlease plc, Forbes House, Whitefriars Estate, Tudor Road, Harrow, Middlesex HA3 5SS. 01-427 8822.

NEW PRODUCTS

Wide viewing angle l.c.d.

A viewing angle of 80° is offered by Toshiba's 16-character one line l.c.d. unit.

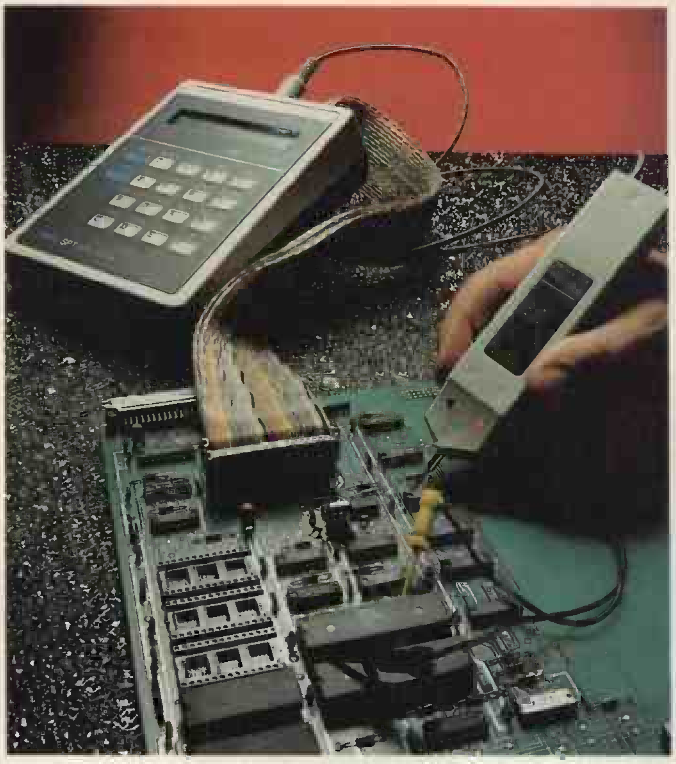
The module is complete with a built-in controller/driver, display ram and character generator rom, it interfaces directly with 4 or 8 bit data from a c.p.u. and operates from a 5V d.c. supply. The increase in viewing angle is achieved by changing the optical thickness of the display which consists of characters formed by a 5 × 7 dot matrix measuring 3.1 × 5.76mm. The TLC-671S is accommodated on a p.c.b. ready for mounting. Toshiba Electron Tube and Device Division, Electronic Component Group, Toshiba (UK) Ltd, Riverside Way, Camberley, Surrey GU15 3AY. Tel: 0276 694600.



Solar powered digital multimeter

A pocket-size digital multimeter available from Universal Instruments has an internal solar power cell to give continuous use without the need for a battery.

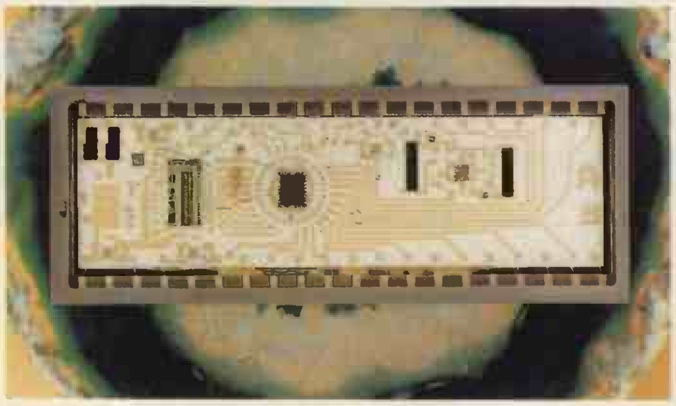
The model 3242 is an autoranging instrument with a single rotary switch and a 3½ digit l.c.d. showing the units and symbols of measurement and polarity. Direct voltage is measured from 0.1mV to 500V in five ranges with a basic accuracy of less than 1%. Alternating voltage is from 1mV to 500V in four ranges. The hand-held meter measures 120 × 65 × 18mm including a fully enclosed test lead storage compartment. Universal Instrument Services Ltd, Unit 62, GEC Site, Cambridge Road, Whetstone, Leicester LE8 3LH. Tel: 0533 750123.



Micro-board troubleshooter

Fault finding on microprocessor boards down to component level is simplified when using the SPT micro-board troubleshooter.

The SPT runs pre-defined test sequences and each version simulates one type of processor; versions are available to simulate most popular microprocessors and microcontrollers. It is suitable for users at all skill levels in field service, base repair, manufacturing test and proto-type debugging and is available from Antron Electronics. It tests the processor's address, data and control lines for short circuits and monitors and displays the status of control inputs and performance tests of ram and rom, including pattern sensitivity, and calculates checksums and address de-coding. Antron Electronics Ltd, Guildford Road Industrial Estate, Farnham, Surrey GU9 9PZ. Tel: 0252 737191.



Analogue to digital converter

A two-chip hybrid analogue to digital converter available from Microelectronics converts to 16 bit resolution in 4μs.

The device is complete, including an on-board bandgap reference, clock, and tri-stage output buffer. The t.t.l. compatible output is offered to the microprocessor bus as either 16 bit parallel or two 8 bit words. Serial output is also available. The speed of conversion is controllable via an external voltage; alternatively an external clock can over-ride the internal oscillator where synchronized conversion is necessary. Based around the HADC52160, the converter is the successive approximation type, and requires ±15V. Microelectronics Technology Ltd, Unit 2, Great Haseley Trading Estate, Great Haseley, Oxon OX9 7PF. Tel: 08446 8781.

Pre-print labels

Custom pre-print labels offering print protection to high temperatures and to solutions such as Freon, solvents and de-ionized water are available from OK Industries. P.c.bs, i.cs, cables and other electronic, electrical and mechanical parts can be identified with the labels which are protected by a special laminate. OK Industries UK Ltd, Barton Farm Industrial Estate, Chickenhall Lane, Eastleigh, Hants SO5 5RR. Tel: 0703 619841.

Ceramic chip capacitors

A nickel barrier layer in the end metallization of the Kemet Solderguard II series of multilayer ceramic chip capacitors prevents silver leaching or scavenging, which could result in open circuits during assembly.

The chips are offered in COG, X7R and Z5U dielectrics in 100 and 50V ratings – with the 0805 and 1206 sizes available on 8mm aluminium blister tape and the 1812 size on 12mm tape. The devices feature a capacitance range of 1pF to 0.22μF. The Capacitor Group, STC Electronic Services, Edinburgh Way, Harlow, Essex CM20 2DF. Tel: 0279 626777.

Thin axial fan

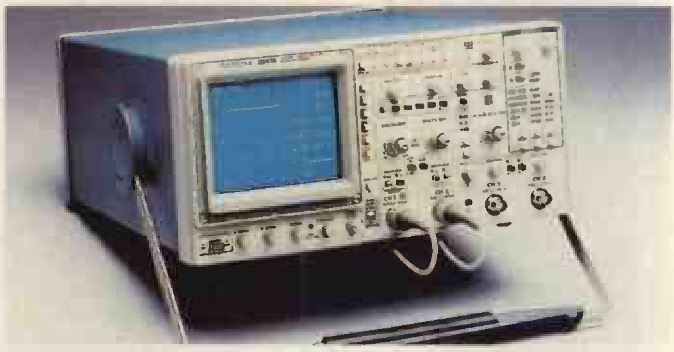
A 20mm thick, brushless, d.c. axial fan has been introduced by Highland Electronics to meet the demand for smaller fans.

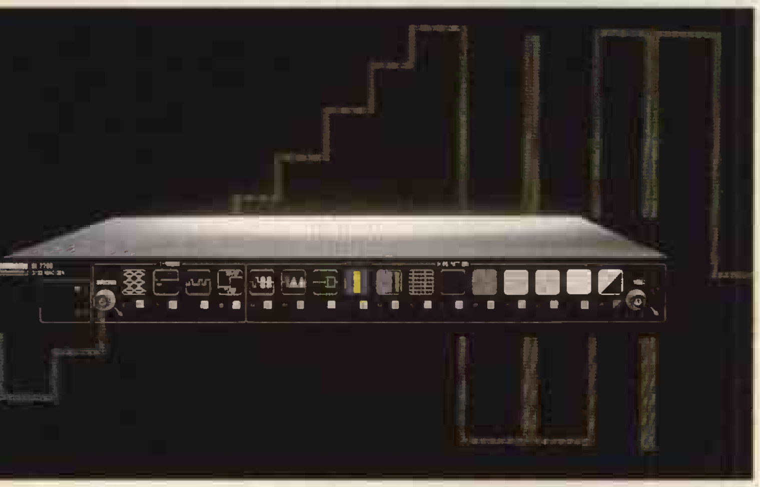
It is available in 12 or 24V versions with a choice of speed giving either high flow rates or quieter running depending on the requirements. The fans are supplied with a moulded case and flying leads. A special version with an alarm circuit can warn of stall trouble. Highland Electronics Ltd, Albert Drive, Burgess Hill, West Sussex RH15 9TN. Tel: 04446 45021.

NEW PRODUCTS

Measuring oscilloscope

Tektronix announce the 2247A portable oscilloscope, which features a counter/timer, automatic rise/fall time measurements, and extended measurement capabilities. The 2247A is a 100 MHz, 4-channel oscilloscope, providing auto setup, on-screen cursors and up to 20 preprogrammed measurements. The 2247A is intended for the digital design and field service markets. Tel: 06284 6000.





Signal generation for D-MAC and D2-MAC

Schlumberger Instruments announces a D-MAC and D2-MAC packet test signal generator designed to provide test patterns and signals to EBU specifications. The generator simply replaces the program for testing a transmission channel, receiver or code converter. Synthesis is performed on 10 bits at the D2-MAC clock frequency. The 7765 generates a colour pattern incorporating standard international signals, duo-binary synchronization patterns, and external equipment synchronization. Tel: 0252 544433.

Digital storage oscilloscope

The Hameg MH205-2 can operate as a digital storage or real-time oscilloscope. In analogue mode, it provides two channels with frequency range to 20MHz and a timebase ranging between 0.2s and 20ns per cm. As a digital storage oscilloscope, 1042 × 8 bit memory is available per channel and maximum sampling rate is 5MHz per channel. Feedback Test and Measurement. Tel: 0892 653322.

Function generator

The AFG from Rohde and Schwarz can function as a pulse generator with single pulses, or pulse trains which are either internally or externally triggered with adjustable rise and fall times. In sweep mode, the unit provides linear or logarithmic sweep with phase continuous steps and am, fm, vco, pulse modulation and frequency-shift keying.

Five operating modes are featured, notably continuous, burst, half-cycle burst, gate and sweep. In all five modes sine, triangle and square waveforms are adjustable over the range 10MHz to 20MHz. Feedback Test and Measurement. Tel: 0892 653322.

D connectors with integral suppression

From Murata is the CUBL range of D-type connectors which feature integral rfi suppression capacitors connected between the metal casing and user-selected pins. Since they are connected directly to the exit points of signals from circuit boards, the capacitors provide more effective emi suppression. The shielded metal screen further improves the rfi screening.

The CUBL range comprises nine, 15, 25 and 50 way versions. Tel: 0252 522111.

High-stability pressure transducer

The EPNM series from Entran are miniature pressure transducers with a threaded body, designed for high-stability performance. Metallic-foil strain gauges bonded to a APX-4 stainless steel diaphragm provide an output of typically 9mV fs for 5V excitation, an optional internal amplifier giving a high output of 5 volts fs. Pressure range is from 0-150 psi up to 0-7500 psi. Tel: 0344 778848.

256k eproms with 70ns access

Toshiba announces the TC57H256D family of 256kbit UV-erasable eproms. With a 32768 × 8bit architecture, these devices offer access times for read operations as low as 70ns, 30mA maximum active current at 14.2MHz and a standby current as low as 100uA. Tel: 0276 694600.

NEW PRODUCTS

Portable telemetry terminal

Duty engineers can monitor, record and display information from any current Dynamic Logic outstation using the company's fully menu driven portable telemetry terminal.

The D1126 terminal is based on the Toshiba T-1000 lap top computer with data being gathered from the outstation via the public switched telephone network using an acoustic coupler. Received site storage data may be manipulated for display in tabulated or graphical form, printed as hard copy, and saved on disc. The lap top computer, a thermal printer, acoustic coupler and battery charger are all contained in a brief case. Dynamic Logic Ltd, The Western Road, Bracknell, Berkshire RG12 1RW. Tel: 0344 51915.

Generation of circuit diagrams

New software available as an option for the Pro 1990 hybrid board test system from DCA Technology generates a schematic diagram of the circuit under test even when access to original drawing is not possible.

The system learns the device interconnections of the board under test by using a combination of probes and test clips. The software package can be run on the Pro 1990 or the interconnection information can be downloaded onto a PC and the schematic generated remotely from the tester. The system directs the operator through each step of the testing procedure. A graphical representation of the board under test is displayed on the screen together with detailed instructions as to where to place each test clip. DCA Technology Ltd, 5 Grove Park, Mill Lane, Alton, Hants GU34 2QG. Tel: 0420 84088.

Low-cost surface mount assembly

A low-cost surface mount assembly system capable of handling board sizes up to 175 × 120mm consists of five compact bench top units.

A stencil printer for solder paste, hand assembly table, vacuum component pick-up tool, rotary carousel component store, and an infra red reflow oven make up the manual surface mount assembly and reflow sequence. Ongoing support is offered by S.M.T. via a telephone and fax helpline. For companies needing extra help a consultancy and a complete turnkey package through to set up and training is provided. S.M.T., Unit 2A, J. Samuel White's Estate, Medina Road, Cowes, Isle of Wight. Tel: 0983 290333.

Glue gun gives instant bonding

The trigger action on Power Adhesives' MR900 12mm stick-fed hot-melt glue gun allows fast and accurate bonding.

It can be operated at temperatures from 160 to 215°C so it can be used on temperature sensitive substrates such as expanded foams or with high temperature polyamide adhesives. The electronic temperature control delivers 2.4kg of hot-metal adhesive per hour. Power Adhesives Ltd, 103 Wnatz Road, Dagenham, Essex RM10 8PS. Tel: 01-592 1216.

Surface mount device rework

Where only occasional or low volume soldering rework is required the Ungar 6966 heat gun used in conjunction with a hand soldering unit is a low cost solution.

Although the heat gun has many applications from heat shrinking to encapsulation, the heat and airflow characteristics, combined with a close tolerance nozzle, allow effective removal of surface mounted components. Once the component is removed the new one can be hand soldered in place. Ungar Division, Unit 1, Clifton Road, Shefford, Beds SG17 5AB. Tel: 0462 814914.

Reprogrammable gal

An electrically erasable programmable c-mos logic array manufactured by SGS offers a number of advantages over convertional programmable logic devices.

Devices programmed in error or needing to be updated to accommodate system changes can be erased and re-used up to 100 times. Data retention is specified at 20 years. The GAL16V8 from Impulse features propagation delays down to 15ns and maximum asynchronous frequency of operation can be in excess of 66MHz. It has eight logic microcells for the output stages allowing the device to emulate any other 20 pin pal device, and provide full compatability in terms of function, fuse-map and parametric performance. Impulse Electronics, Hammond House, Caterham, Surrey CR3 6XG. Tel: 0883 46433.

Interface for IBM PS/2

The GPIB-3000 interface card available from Roalan turns the IBM PS/2 PC into an IEEE controller.

The card plugs into any micro-channel architecture slot and comes complete with the necessary drivers and diagnostics for Basic. If the card is used through an installable MS-DOS driver a GPIB file is created and then any language can be used with the installed driver package. Users can build into their own software the commands for the GPIB-3000 as the source code is not protected. The board uses the Texas TMS9914 IEEE controller chip and free access to the low level commands of the 9914 is available. Roalan International, Gleneagles House, 31 Riverside Road, West Moors, Wimbourne, Dorset BH22 0LG. Tel 0202 861512.

Portable or rack mounted keyboard

A 64-key Qwerty Plus low-profile keyboard from Access Keyboards is suitable for portable equipment or for rack mounting.

It is available with either ASCII or positional up/down coding and provides a basic qwerty layout with several function and cursor keys. An optional row of 15 additional function keys can be incorporated if required. Switch life is rated at 50 million operations. Auto repeat is included as standard on all keys, at a rate of 10 characters/s. The keyboard uses a 1200Baud asynchronous interface and is supplied complete with a 1.8m coiled cable. Access Keyboards Ltd, Unit 18, Suttons Industrial Park, Earley, Reading, Berks RG6 1AZ. Tel: 0734 663333.

Telex terminal with text manipulation

A series of telex terminals from Siemens called T1200, is available either screen-based or incorporating an 80-character line-display.

Text on the screen-based model is displayed on a 12in, high-resolution, non-reflecting screen with a black-on-white display. An autonomous hard-copy dot-matrix printer is provided which offers bi-directional printing and a maximum speed of 60 characters/s. Wordprocessor-style text-manipulation features and the ability to create up to ten text modules enable frequently used passages to be inserted at the press of a key. The screen-based terminal memory is capable of holding up to 115 pages of text and is protected from power failure by a trickle-charge battery. Siemens Ltd, Windmill Road, Sunbury-on-Thames, Middlesex TW16 7HS. Tel: 0932 785691.

NEW PRODUCTS

Scanner lets PCs read books

A hand-held scanner which enables personal computers to read and store information from books and similar sources has been developed by Skyworld Technology to speed up the input of data into computers.

The device, known as Skyscan, is compatible with IBM-XT, PC-AT and PS/2 can capture photographs, artwork, logos, maps, handwriting or the surfaces of three dimensional objects. It can accommodate images up to 10.6 × 30.5cm. After scanning the image is displayed on a computer screen where it can be edited, enlarged or reduced prior to being stored, printed out, or transmitted to linked computers. Conversion of image files to ASCII files compatible with Wordstar, WordPerfect and other text editors can be delegated to the ReadRight character recognition software. Graphics captured in image files by Skyscan, can be merged with text files using desktop publishing software packages. Sky Technology Ltd, 11/F Hang Lung Bank Building, 8 Hysan Avenue, Hong Kong. Tel: 5 777848.

Monochrome video monitors

Resolution has been improved to 800 lines in Norbain Imaging's uprated range of 9 and 12in monochrome video monitors.

The models reproduce stable pictures in bright areas where viewing can be difficult using other monitors. They are designed to operate in combination with cctv cameras and time-lapsed or event alarm v.c.rs. Power consumption is only 27W. Parallel connection of two or more units is via video input/output terminals to allow repeater monitoring in separate locations. Norbain Imaging, Norbain House, Boulton Road, Reading, Berks RG2 0LT. Tel: 0734 864411.

Serial/parallel buffer switch

The SPS-Plus serial-parallel buffer switch provides up to six computers with access to two user-selectable output devices.

The unit is suitable for applications in which the two output devices operate at widely different speeds, a laser printer and a plotter. The computer is released with the minimum delay regardless of which peripheral is being used. The SPS-Plus is an upgraded version of Nighthawk's SPS serial-parallel buffer switch. Data can be sent into the buffer simultaneously, while both printers are in operation and buffer memory is allocated to each user on an as-needed basis. Two buttons allow each output to be halted if an error occurs. The interface supports xon/xoff and control-line flow-control, and operates all common Baud rates from 50 to 19,200 Baud. Nighthawk Electronics Ltd, PO Box 44, Saffron Walden, Essex CB11 3ND.

Resistance test-set cuts r.f.i.

The Dytecna bond resistance test set measures the low bond resistances between mating surfaces and equipments to ground which are essential for high rf immunity.

It operates at less than 100μV and is sensitive enough to detect the small build up resistance which indicates the eventual failure of the bond, enabling corrective action to be taken. Dielec anticipates an increase in the amount of on-site testing of equipment to reach the standards required by pending EEC legislation. Dielec Ltd, Ivor House, 39 Bath Road, Swindon SN1 4AS.

Secure digital communications

All standard communications channels can be protected using the KV3000 strategic level secure speech system for telephone and radio.

Incorporating an LPC10 vocoder and a 2.5Kbit modem, the device gives practically undegraded speech quality, while two slow speed modems take care of the synchronisation, which generally takes less than 7s. The KV 3000, available from Cairntech, can operate in an asynchronous mode to ensure that secure communications can be made in line conditions where a digital system may not be suitable or workable. The whole system is fully duplex with the ability to operate in the simplex mode for poor quality links, MF SSB or INMARSAT. Once programmed the whole system can be controlled from the KV's own telephone or by a small remote control panel. Cairntech Ltd, 67 Marionville Road, Edinburgh EH7 6AJ. Tel: 031 652 1108.

Multiplexer turns PC into data logger

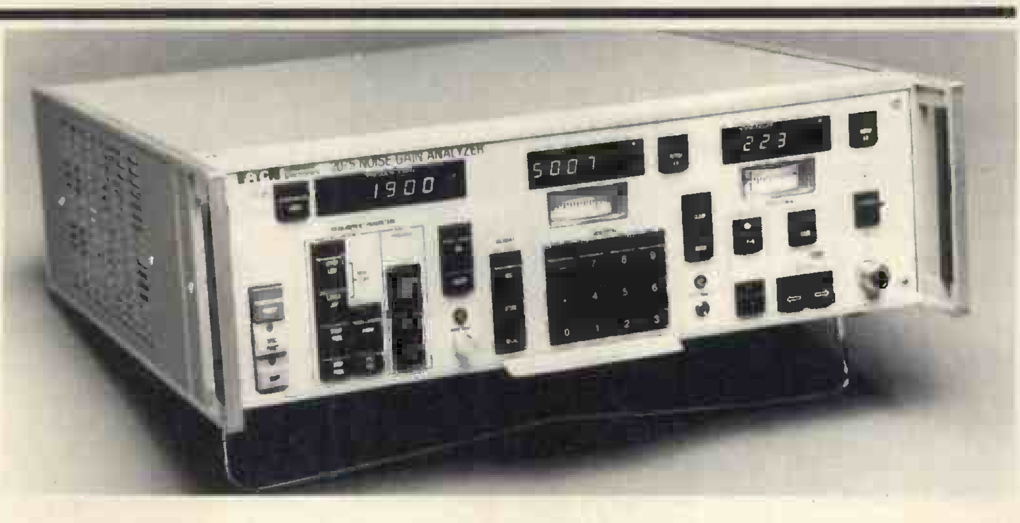
Any personal computer can be extended to a data logger using First Source's 128 channel multiplexer.

Timing and voltage measurement facilities have been added, so that the ADM128 can interface temperature, pressure, humidity and other inputs via sensors generating voltages up to ±40V to a computer. Voltages from any one or more of the 128 channels can be scanned or displayed at predetermined time intervals, and/or compared with pre-set upper and lower limits. An on-board clock function is available which can be interpolated with the readings, and hard-copy output can be obtained via the parallel printer port. All functions are controlled by a set of 16 control commands and nine two-character escape sequences. First Source, The Business Centre, Colne Way, Watford, Herts WD2 4ND.

Noise figure/gain analyzer

Direct broadcast tv receiver testing requirements are met by Eaton's re-engineered noise figure/gain analyzer, the 2075B.

By driving a digital plotter directly the analyser produces charts which can be submitted as part of a test report. An enlarged memory has allowed an increase in calibration points, the addition of loss compensation tables and better use of noise source storage tables. Eaton EID, Eaton House, Molly Millar's Lane, Wokingham, Berks RG11 2QS. Tel: 0734 794717.

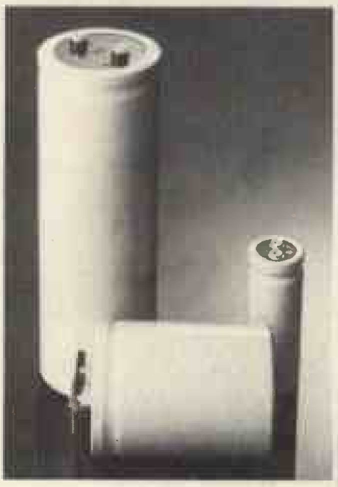


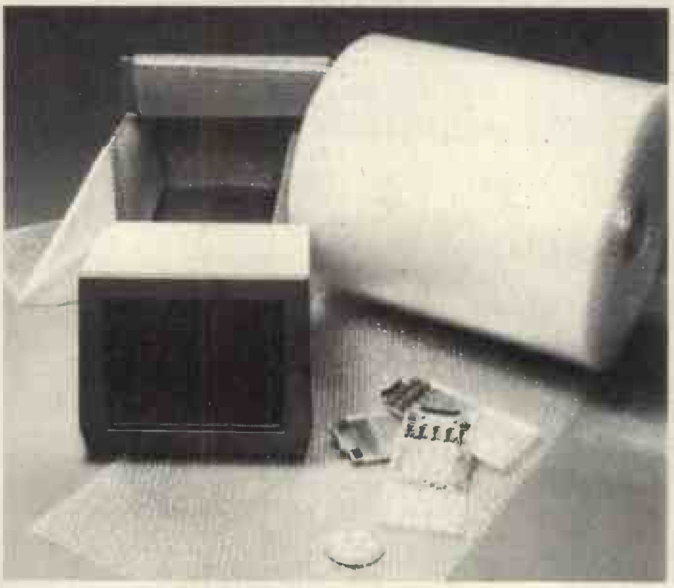
NEW PRODUCTS

Electrolytic capacitors

Large computer-grade aluminium electrolytic capacitors including several types optimised for low equivalent series resistance are available from AVX.

Most specialized of these is the SFC series, which has large welded connection flanges to reduce contact resistance and features special stacked-foil internal construction to improve esr figures at mains frequency. An esr of 2mΩ is claimed for the 0.1F, 6V type, with smaller capacitances and higher voltage ratings increasing the figure to a maximum of 15mΩ for the 6800μF, 50V capacitor. AVX Ltd, AVX House, Manor Park, Aldershot, Hants GU12 4RG. Tel: 0252 312131.





Packaging prevents stress fractures

To prevent electronic equipment and components from developing stress fractures through a chemical reaction with packaging during storage, Sealed Air has upgraded its range of Anti-static and Tri-stat Aircap bubble cushioning products.

The company has removed highly reactive amines which sometimes reacted with the polycarbonate plastics equipment enclosures producing surface stress cracks and marring. Anti-static AirCap does not produce electrostatic charge during handling and dissipates any charge on its surfaces preventing electrostatic discharges onto the device being packaged. Tri-Stat features a three layer construction consisting of a conductive core between two layers of anti-static polyethylene. This provides both rapid charge dissipation and Faraday Cage shielding against electrostatic fields. Sealed Air Ltd, Telford Way, Kettering, Northants NN16 8UN. Tel: 0536 522347.

Thyristor modules

The SKKT105 range of dual thyristor modules can be used in place of two lower-power devices to reduce the component count of equipment.

To simplify their connection in bridge circuits, the modules from Semikron contain two series-connected thyristors with their centre points brought out to terminals. Bridge circuits rectifying most common industrial single-phase and three-phase supplies can be constructed using the modules, since the series comprises four devices with peak repetitive voltage ratings between 800 and 1600V. The high thermal conductivity ceramic insulators provide junction to case thermal resistances as low as 0.28°C/W, enabling the modules to carry average currents up to 115A. The modules are suitable for use in industrial applications such as motor drives and temperature controllers, as well as professional lighting equipment. Semikron Ltd, 4 Marshgate Drive, Hertford SG13 7BQ. Tel: 0992 584677.

Wideband microwave transistors

Two pulsed power microwave transistors offer an alternative to vacuum tubes, such as travelling wave tubes or magnetrons, in S-band (2.7 ro 3.5GHz) radar applications.

The RX2713B90W and RX3034B70W produce 100 and 80W respectively in long pulse mode, defined as 10μs at a 100% duty factor. Philips claim that no other microwave transistor on the market can match this performance in the S-band. The devices are designed for the class C broadband amplifier power stage of the radar output. They are constructed with an interdigitated structure which makes for a high emitter efficiency. Diffused emitter ballasting resistors give good current sharing. Multicell geometry ensures a balance of power dissipation and low thermal resistance. The transistors are housed in an FO-125A metal ceramic flanged package. Philips Components Division, PO Box 218, 5600 MD Eindhoven, The Netherlands. Tel: 31 40 756181.

Protective coating

A surface hardening treatment from Chequers toughens surfaces on injection moulded components that may be subject to excessive wear. The treatment is applied as a thin sprayed coating which cures at normal room temperatures and combines with the molecular structure of the material surface to achieve a uv fast, colourless and transparent finish. Chequers (UK) Ltd, 1-4 Christina Street, London EC2A 4PA. Tel: 01-739 6964.

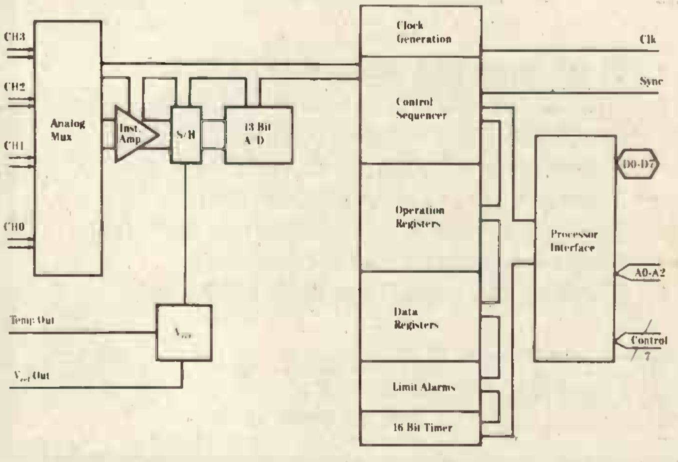
Smart power ics for brushless d.c. motors

A family of sip-packaged, smart power drivers for brushless d.c. motors is available from Sprague. With pulse-width-modulated current control, commutation logic, and well protected power outputs on a single chip, the UDN-2936W and UDN-2937W provide three 45V push-pull outputs, each rated at 3A continuous (4A at startup) and protected by ground-clamp, flyback power diodes and thermal shutdown. Tel: 0932 253355.

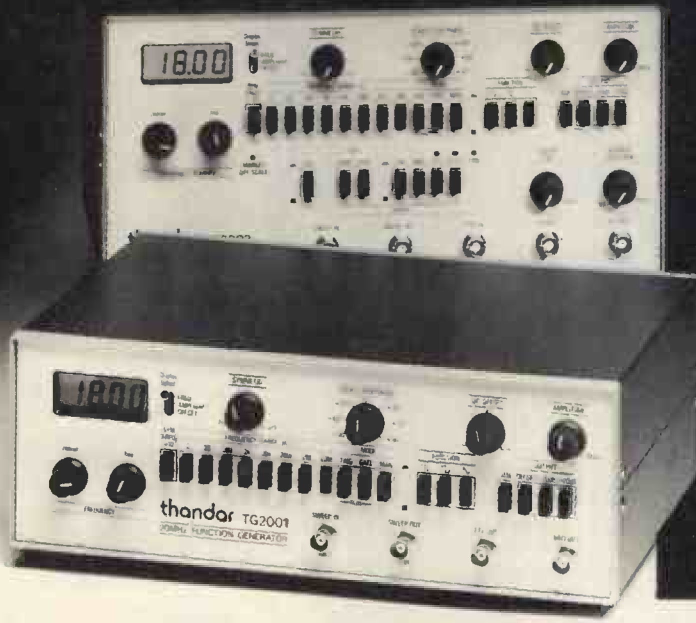
Single-chip data acquisition peripheral

The Micro Linear ML2200 data acquisition peripheral combines a self-calibrating 13-bit analogue to digital converter with a programmable control sequencer and micro-processor interface on a single 40-pin cmos chip.

A four-channel differential or eight-channel single ended input multiplexer, a combination sample-and-hold/instrumentation amplifier, the 13-bit a/d converter, and a 2.5V band gap reference make up the analogue section of the chip. The digital side consists of a control sequencer, operation and data registers, limit alarms, a 16-bit timer, and a microprocessor interface. The company has designed an exerciser for the ML2200 that helps the system engineer become familiar with the device, assists in applications development and shortens development time. Ambar Cascom Ltd, Rabans Close, Aylesbury, Bucks HP19 3RS. Tel: 0296 434141.



20 MHZ Function Generator



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Pioneers

25. Hidetsugu Yagi (1886-1976) and the Yagi-Uda antenna

W.A. ATHERTON

I did my best to beat the Americans. I did my best for my country. So answered Hidetsugu Yagi when questioned by the War Commission about the scientific work he had done in Japan during the Second World War. On hearing this one American went to shake his hand. Yagi was the first Japanese he had heard who spoke proudly of his work instead of denying all.

But like so many others, Yagi too had suffered. In April 1945 his home was destroyed in a fire-bomb attack and much of the data he had collected in the previous thirty or so years went up in flames.

Hidetsugu Yagi was born in Osaka on 28 January, 1886, shortly before Heinrich Hertz made his fundamental discoveries in radio wave generation, propagation and detection. He died in 1976, a few days before his 90th birthday, with more honours than there are directors on a television aerial. It is only our ignorance that leads us to think of the common television aerial, rather than the man, when we hear his name.

He was the second son of an Osaka family which had for many generations served as a retainer to a Japanese shogun. They made payments in rice to other members of the shogun household. Though it was a position of some responsibility, it was by no means the highest. When the eldest son brought disgrace on himself and split the family (by dealing in stocks and shares which was then considered little better than gambling) Hidetsugu assumed the role of the "eldest" son.

Yagi was an idealist and a socialist. Later in the life he was elected to the upper legislative house, roughly equivalent to our House of Lords, though he withdrew without being very active because his political ideas differed from those of the party.

His ideals were also later revealed in his deep interest in labour relations and patterns of working life. He wrote articles on the subject. In fact he was a prolific writer in several spheres, not just engineering and science. He wrote for popular magazines and newspapers as well as scientific journals and covered a range of subjects including education, society, and relationships between science and society as well as electrical communications.

Early in his education Yagi preferred the arts to science, but gradually his enthusiasm for natural phenomena grew. When a teacher tried to steer him back towards a career in the arts or law Yagi's forthright reply was, "Man-made laws change with the country and the years; I wish to study natural laws given by God which do not change." He respected a power greater than

mere mortals and he recognised the limits of human knowledge: "Some people say science controls nature but a real scientist would never feel that way." Science, he insisted, should be used for world peace.

YAGI'S GRAND TOUR

Yagi graduated from the Tokyo Imperial University (now Tokyo University) at the age of 24 and began teaching at the Sendai Engineering High School. Sendai is a large city some 200 miles north of Tokyo with a population of around a million. After four years the Ministry of Education sent him abroad to further his studies, a fairly common practice, and it was to Germany he went to study resonance phenomena under Heinrich Barkhausen at the University of Dresden. It was a few years later, in 1919, that Barkhausen discovered the magnetic domain effect now named after him. Yagi's work under Barkhausen was mostly concerned with the generation of continuous electromagnetic waves using oscillations produced by electric arcs, a technique dating back to the turn of the century.

When war broke out in 1914 Yagi was on a study tour of Austria, Switzerland and Italy. Instead of returning to Germany, he abandoned his experimental data there and headed for London where he approached J.A. Fleming, the famous inventor of the vacuum diode and professor of electrical engineering at University College, London. Fleming was 65 years old and short of students because of the war. He agreed that the Japanese graduate should continue under him his study of the generation of continuous electromagnetic waves. It is said that one day Fleming was so excited at seeing Yagi's success with continuous wave oscillations that he danced round the laboratory shouting "Bravo! Bravo!"

The next stage of Yagi's three-year grand tour took him to the United States and a brief stay at Harvard University. Then in 1916 it was back to Japan to resume his teaching career at Sendai. Soon the Engineering High School was merged into the Tohoku Imperial University as the new Faculty of Engineering and Yagi received his doctorate two years later in 1921. The Electrical Engineering Department regards Professor Yagi not only as one of its founders but as one of those who helped establish its reputation for education based on original and creative research.

We have seen that by the time Yagi had settled into the routine of university life at Tohoku he was well versed in the ways of producing continuous radio waves by using electric arcs. However in the early 1920s he learned of the invention of another, potentially better, method of generating short wavelength radiation. A Japanese naval officer, returning from a visit to the USA, told him of the invention of the magnetron tube by Albert Hull at the research laboratories of the General Electric Company (New York). It was not long before Yagi and his research students had incorporated the magnetron into their own work. In 1927 Yagi's student Kinjiro Okabe was able to produce wavelengths of a few tens of centimetres and

SHINTARO UDA (1896-1976)

Shintaro Uda attended Tohoku University as a student when Yagi was there as a teacher, and gained his bachelor's degree in 1924 and his doctorate in 1931. He worked as Yagi's student and co-researcher in the 1920s and performed the experiments on the aerial which Yagi described in America in 1928. Yagi, in his classic paper, pointed out that Uda had already published nine papers on the beam system in Japan and they had written others jointly. In 1932 Uda received a prize from the Imperial Academy of Japan for his studies on microwaves and four years later was appointed Professor of Electrical Communication Engineering at Tohoku University. He retired in 1960, becoming Professor Emeritus, but was soon appointed as a professor at another university in Yokohama. From 1955 to 1958 he worked as a Unesco expert at the National Physical Laboratory of India in New Delhi.

went on to obtain greater output intensities by splitting the anode into segments – the invention of the split-anode magnetron.

It was another of Yagi's students and co-researchers, Shintaro Uda (see box), who performed the experiments which established the aerial we now know as the Yagi or Yagi-Uda aerial and which can give a directional radio beam. It was the combination of the split-anode magnetron and the directional aerial to form an ultra-high frequency beam communication system which brought Yagi to the attention of western engineers in 1928.

Evidently Yagi was skilled at selecting and training his research students. Shintaro Uda became a professor at Tohoku University and Kinjiro Okabe a professor at Osaka University – to which both he and Yagi moved in the early 1930s. Okabe is credited with inventing the first Japanese radar for detecting aircraft at Osaka in 1936.

During World War Two the Japanese used two general types of radar system. In one a continuous wave was transmitted as a beam between two stations and aircraft passing through the beam were detected by doppler effects. The second method used the conventional pulse techniques. It was the first type that Okabe and Yagi worked on in 1936 and Yagi has stated that it was based on an idea which occurred to him during his trip to Germany before the First World War. The longest beam radar used by the Japanese during the war reached over 650km from Taiwan to Shanghai.[2]

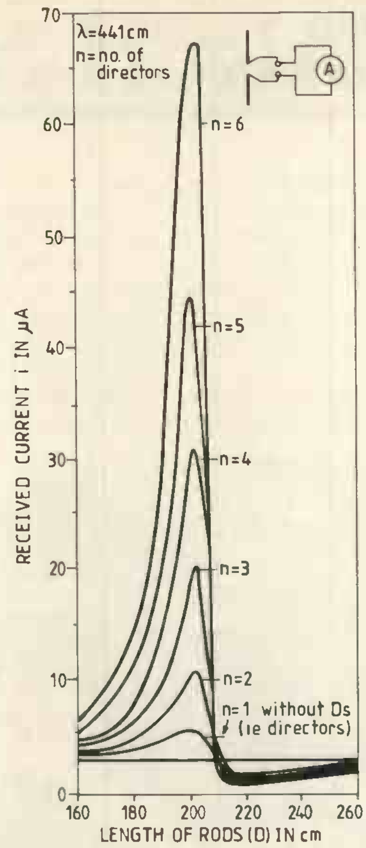
Yagi was nominally in charge of civilian fundamental research and severely criticized the Japanese High Command's piecemeal approach to electronics research. Radar was viewed as a defensive equipment and therefore of low importance in a war in which Japan expected to be always on the offensive. Work was undertaken entirely separately by the army and the navy.

A CLASSIC PAPER

It was in 1928 that the success of Yagi's team became known in the West. During a tour of the United States he described the work carried out by himself and his research students and co-researchers Uda and Okabe. He lectured to at least three meetings of the Institute of Radio Engineers (IRE, a forerunner of the present IEEE) and to staff at General Electric where the original magnetron was invented. A paper was published in the *Proceedings of the IRE* in June 1928 and was reprinted in 1894[1].

The discussion which took place at one of the IRE meetings is also printed in the *Proceedings*. J.H. Dellinger, chief of the radio division of the Bureau of Standards in Washington DC, ended his own remarks with the comment: "In conclusion, I would like to say that I have never listened to a paper that I felt so sure was destined to be a classic." Dellinger's remark was no mere polite comment.

The paper, "Beam transmission of ultra short waves," was in two parts. Part 1 dealt with the Yagi-Uda aerial system using wavelengths of approximately 4.4m and 2.6m. Part 2 covered the generation of centimetre waves from split-anode magnet-



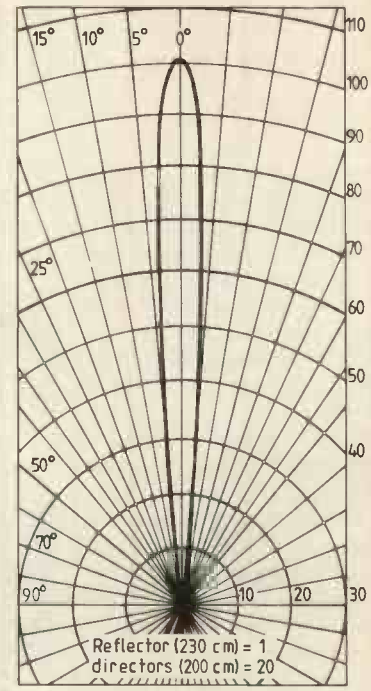


Fig.1. Two figures from Yagi's paper, now a classic of radio engineering: above, "the effect of varying number and length of directors in the wave canals on received current"; right, the beam radiation from a "radiator utilizing a wave canal".

rons, mostly at wavelengths of around 40cm but with some at 19cm, 12cm and even 8cm. Yagi was careful to give credit to the ingenuity of Shintaro Uda for the experiments on the aerial and to Kinjaro Okabe for those on the magnetrons. Theoretical explanations had already been given in publications in Japan and more were to follow, and Yagi assured his listeners that the coming publication would be in English.

Uda's experiments on the aerials included studies of the effects of aerial height, the use of reflectors, the number, length and spacing of the directors (a row of which Yagi called a "wave canal"), polarization, etc. The results were expressed in 22 figures, two of which are reproduced here. Another 16 figures were used in Part 2 of the paper.

The basic description of the aerial system began with the effect that the natural frequency of a metal rod of finite length has in determining its action as a "wave reflector" or "wave director". "By utilizing this wave directing quality, a sharp beam may be produced," wrote Yagi, introducing the main feature of what has become the most common directional aerial today. A triangle of three or five antennas, he explained, could be arranged behind the main radiating antenna to become a "trigonal reflector". A number of directors could be placed in front. "By properly adjusting the distance between the wave-directors, and their natural frequencies, it is possible to transmit a larger part of the energy in the wave along the row of directors."

HONOURS

Like many pioneers, Yagi held numerous awards and special appointments. After retiring he was an Emeritus Professor of both Tohoku and Osaka Universities. He was a member of the Japan Academy and special adviser to the Yagi Antenna Company (which he had founded in 1952), the Japan television broadcasting network, the Tokyo Express Electric Railway, and to various scientific councils and government agencies. More unusually for an electronics pioneer he was a special correspondent for a large daily newspaper and had been chairman of a number of assocations including the Tokyo Efficiency Association and the Home Electrics Culture Association. Amongst the numerous prizes he received perhaps the most notable was the Cultural Order of Merit which he received from Emperor Hirohito in 1976, the year in which he died.

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2. R.I. Wilkinson, "Short survey of Japanese radar", *Electrical Engineering*, Aug./Sept. 1946, 370-377, and Oct.1946 455-463.

Next in this series of pioneers of electrical communication: Harold Black, inventor of the negative feedback amplifier.

Dr Tony Atherton is on the staff of the Independent Broadcasting Authority's Harman Engineering Training College at Seaton in Devon.

He would like to thank Professor S. Adachi of Tohoku University for information on which this articled is based and Mr and Mrs J. Loftus for their essential help with translations.

RESEARCH NOTES

Ten times hotter than the Sun

Thermonuclear plasmas nearly ten times hotter than the centre of the Sun have been achieved in JET (Joint European Torus), the experimental nuclear fusion project at Culham near Oxford. JET now routinely produces plasmas with temperatures well over 100 million degrees for several seconds.

JET, the flagship of Europe's co-ordinated fusion research programme set up ten years ago, is the world's largest experiment aimed at establishing the feasibility of using nuclear fusion for power generation. Fusion is the source of energy of the Sun and stars in which reactions take place at a temperature of about 15 million degrees. To make a fusion power source on Earth requires more stringent conditions such as temperatures greater than 100 million degrees. At these temperatures the fuel is a plasma which can be held together by magnetic fields.

The principal advantages of fusion are that it would use fuels such as deuterium and tritium which are plentiful and widely distributed and which do not have the drawbacks associated with the burning of fossil fuels. A fusion reactor would be a very safe system since there would only be sufficient fuel in the reactor for a few seconds of operation. There would be no radioactive waste from reaction products although the reactor structure itself would become radioactive.

Earlier this year the European Council of Ministers approved the extension of the JET programme up to the end of 1992 with an annual budget of £75M. The staff and funds for the project come from Euratom and fourteen European countries (the 12 member countries of the EEC together with Sweden and Switzerland).

At the halfway stage of the scheduled experimental programme JET has not only reached plasma temperatures greater than 100 million degrees but has also achieved the required plasma density and the necessary confinement time for a reactor, though not all at the same time. JET is the only machine to have achieved a confinement time greater than one second. The record plasma heating current of 7×10^6 amperes is more than twice that of any other fusion experiment.

As for generating real power, that must await the next generation of machines. JET has however defined the parameters of such a commercial reactor, which will be about two-and-a-half times larger still. Plasma currents will be about 3×10^8 amperes and will be maintained for up to an hour at a time.

Several teams are working on designs for the next step. These include NET (Next European Torus) and ITER (International Thermonuclear Experimental Reactor), involving teams from the USA, USSR, Japan and Europe.

Such teams confidently predict the emergence of fusion power as a viable alternative to nuclear fission.

How stress kills high performance chips

Ever since integrated circuits first made their appearance in the mid-1960s, the biggest problems for manufacturers have been defects and impurities. Some chip diseases such as the once-dreaded 'purple plague' almost did for the chip industry what myxomatosis did for rabbits. But with modern manufacturing plant cleaner even than an operating theatre, high standards of reliability were taken for granted by the late '70s.

It therefore came as something of a shock about five years ago when certain US manufacturers discovered high-speed chips literally cracking up on the shelf. An insidious new plague was killing i.cs as they sat in storage – long before they had ever been built into equipment. Sometimes it took a few hundred hours, sometimes a year or two.

Now a team from Cornell University has published (*Applied Physics Letters*, 4 July) the first thorough analysis of the causes of these unexpected failures. The silent killer, it turns out, is unrelieved stress built up during the heating and cooling of the manufacturing process. Chips are manufactured and processed at temperatures up to 400°C, after which they obviously have to cool down to room temperature. Needless to say all the different constituents – silicon, aluminium, gold, ceramics, plastics etc. – have different coefficients of expansion. So when a chip cools to room temperature it builds up internal stresses to quite a significant degree.

Why then has the problem only come to light recently? The answer is that today's powerful new chips are much tinier and more delicate than their predecessors. Line patterns may be no thicker than 10^{-6}m. So even the tiniest stress fractures, however microscopic, have a much more disastrous effect than they would on thicker and heavier structures.

The first sign of mechanical stress is the formation of tiny voids in the lattice structure of atoms within the metal. As the structure relieves its stress, layers of atoms separate off and redeposit themselves elsewhere. In the case of metal conductors 10^{-6}m in width, these voids eventually grow into cracks big enough to disrupt the flow of current entirely.

As chips continue to become increasingly powerful, and hence smaller and more intricate, this problem is bound to become more serious. The Cornell researchers calculate that a tenfold reduction in chip dimensions will lead to a thousand-fold reduction in thermal stress reliability. They've also, for the first time, come up with a good mathematical analysis of the phenomenon which may, they say, enable manufacturers to do more than just tinker with their production processes. The team is also working on ways of getting around chip stress entirely by means of new materials. They hope, for example, to develop metal alloys with flexible inter-atomic bonds as a way of absorbing the inter-atomic forces.

But if history is anything to go by, this problem will be overcome just in time to witness the first of a new genre – the high-flying super-intelligent chip having a nervous breakdown.

RESEARCH NOTES

Health hazards

A report from the National Radiological Protection Board (NRPB – R222) examines the health issues that may arise in the siting of a low frequency transmission mast. It is based on evidence presented by the Board at a recent public inquiry into the proposed installation of a 500kW RTE transmitter in Co. Meath, Republic of Ireland; and although it has direct significance only to the frequency range 100kHz to 1MHz, the author points out that it has implications for other frequency ranges also.

The health issues under consideration are those due to bulk body heating, rf burns from ungrounded objects and potential hazards such as cancer which may arise from non-thermal processes.

Of the thermal effects, this report investigates the levels of radiation likely to be encountered in practice at an lf transmitter site. These, it considers, are at least 10 000 times less than those at which harmful effects might be expected.

As for rf burns, these could possibly occur when a person touches a conducting object like a car or a wire fence that is insulated from the ground. The NRPB report points out however that above frequencies of about 50kHz, muscle contraction does not occur, nor does the rf current affect the heart. Nevertheless if current density exceeds about 300mAcm^{-2} a burn will be experienced at the point of contact. Earlier work by the International Radiation Protection Association, however, suggests that there is a threshold current of about 50mA below which no burns can occur, no matter how small the area of contact.

The NRPB report suggests that it is extremely unlikely that such currents would occur except in very close proximity to a low-frequency transmitter. The only problem the Board does concede is the danger to farmers operating long electric fences within 1km of the transmitter. Pre-cooked cows?

Finally the contentious question of non-thermal effects. Here the NRPB admits that it is impossible to be very scientific. It says that attempts to demonstrate harmful effects of low-level rf on animals and other biological organisms have yielded confusing and often conflicting results. The report also goes to some lengths to distinguish between ionizing radiation (X-rays and gamma-rays) which *do* have measurable non-thermal effects on the body, and non-ionizing radiation (such as rf) for which the evidence is scant. Overall it concludes that there are no significant thermal effects of relevance to human health in the range 100kHz to 1MHz.

So it does seem that, with low radio frequencies, if you can't feel them then they won't harm you.

Ultimate clock from frozen atoms

Scientists at the US National Bureau of Standards (NBS) in Maryland and the Ecole Normale Supérieure in Paris have succeeded in different ways in cooling atoms to within a few microdegrees of absolute zero. This cooling, which reduces the movement – and hence the Doppler shift – of the atoms removes the main limitation to the accuracy of atomic frequency standards and clocks.

At normal temperatures, gas atoms bounce around in their containers to such an extent that any measurements on them are subject to considerable variability. So if, for example, a gas atom emits a photon of light (as it would do when excited in a discharge tube), the frequency of emission has a degree of uncertainty determined by its motion relative to the measuring equipment. The hotter the gas, the faster is the movement of the atoms and hence the greater the degree of any inaccuracy of measurement. For that reason, today's best frequency standards are only accurate to two parts in 10^{14}.

Such a fundamental limit can obviously be overcome only by cooling the gas to a point at which the atomic motion is for all practical purposes negligible. But it is not just a job for the domestic freezer. Absolute zero, like absolute silence, becomes increasingly hard to attain the

The most recently published work (*Science* vol. 241, p.1041) indicates that the National Bureau of Standards team has breached what was once considered an almost impenetrable barrier at around 0.25mK. Using six laser beams they have succeeded in slowing down atoms of sodium vapour and trapping them with streams of photons.

The way this is done is extremely ingenious; it's not just a game of snooker on the atomic scale. Each laser is tuned to a frequency some 5-20MHz below the spectral emission of the sodium atoms. So if a sodium atom attempts to move towards a particular laser, Doppler shift will cause the atom to 'see' the laser as being close to its own resonant frequency. At resonance the atom absorbs more photons, loses energy and retreats from the laser.

With six lasers, this 'potential feedback' creates a region in which the sodium atoms are held nearly motionless, that is almost without temperature. But they key word is 'almost' because there's yet another barrier – the so-called 3μK photon recoil limit. This is the temperature equivalent to the energy transferred when an atom absorbs a single photon.

Even this barrier has now been sidestepped by the French group, who have used two lasers facing each other to slow down the movement of helium atoms preferentially in one particular direction. The resulting 'low' of 2μK is an intriguing example of the bizarre concept of one-dimensional temperature!

Fascinating though all this is for theorists, the really valuable practical consequence is likely to be an improvement by several orders of magnitude in the accuracy of atomic frequency standards. NBS researchers are optimistically predicting one part in 10^{18} – that's an error of about one second since the Big Bang . . .

Bright future for solar cells

A gallium arsenide solar cell with an efficiency of 28.1% has been developed in the laboratories of Varian Associates of Palo Alto, California. It comprises a single junction and measures 5mm × 5mm.

This record efficiency, although only about two percentage points higher than the previous best is extremely significant in terms of what it could make possible in space applications. The odd percent improvement means, for example, a few more communications channels on satellites which, in most cases today are limited by their power budgets.

Gallium arsenide cells have an additional advantage over their silicon counterparts in such hostile environments, being less affected by temperature variations and bombardment by cosmic radiation.

Varian has now established a pilot production facility and hopes to produce the cells commercially early next year.

Crash program

In the days when office workers could hardly hear themselves think because of the pounding of manual typewriters, everyone dreamed of silent word-processors. Today, it seems, we're all suffering from withdrawal symptoms. With no more than the odd bleep's worth of auditory feedback to listen to, many people crave for the days when you could actually hear what the machinery was doing.

Bill Gaver of the University of California at San Diego has filled this long-felt need with a program called Sonic Finder. When run on a Macintosh machine it brings most of the normal functions to ear-splitting life.

Erasing a file sounds like dropping an object in the dustbin; the arrival of e-mail sounds like a letter dropping on the mat; copying a file sounds like a bottle gradually filling with water.

Gaver says the program is primarily designed to relieve the need constantly to watch the screen. This is likely, he thinks, to reduce fatigue. The other potential benefit, in conjunction with the screen, would be to enable the user to monitor two operations simultaneously.

Research Notes is written by John Wilson of the BBC World Service science unit.

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7448	1.00
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7451	0.35
7453	0.36
7454	0.38
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7472	0.45
7473	0.45
7474	0.50
7475	0.60
7476	0.45
7480	0.65
7481	1.80
7483A	1.05
7484A	1.25
7485	1.10
7486	0.42
7489	2.10
7490A	0.55
7491	0.60
7492A	0.70
7493A	0.55
7494	1.10
7495A	0.60
7496	0.80
7497	2.90
74100	1.90
74107	0.50
74109	0.75
74110	0.75
74111	0.55
74116	1.70
74118	1.10
74119	1.70
74120	1.00
74121	0.55
74122	0.70
74123	0.80
74125	0.65
74126	0.55
74128	0.55
74132	0.75
74136	0.70
74141	0.90
74142	2.50
74143	1.30
74144	2.70
74145	1.10
74147	1.70
74148	1.40
74150	1.75
74151A	0.70
74153	0.80
74154	1.00
74155	0.80
74156	0.90
74159	2.25
74160	1.10
74161	0.80
74162	1.10
74163	1.10
74164	1.20
74165	1.10
74166	1.40
74167	4.00
74170	2.00
74172	4.20
74173	1.40
74174	1.10
74175	1.05
74176	1.00
74178	1.50
74179	1.50
74180	1.00
74181	3.40
74182	1.40
74184	1.80
74185A	1.80
74190	1.30
74191	1.30
74192	1.10
74193	1.15
74194	1.10
74195	0.80
74196	1.30
74197	1.10
74198	2.20
74199	2.20
74221	1.10
74251	1.00
74259	1.50
74265	0.80
74273	2.00
74276	1.40
74278	1.70
74279	0.90
74283	1.05
74742	3.20
74290	0.90
74293	0.90
74298	1.80
74351	2.00
74365A	0.80
74366A	0.80
74367A	0.80
74376	1.80
74390	1.10
74393	1.20
74490	1.40

74LS SERIES

74LS00	0.24
74LS01	0.24
74LS02	0.24
74LS03	0.24
74LS04	0.24
74LS05	0.24
74LS08	0.24
74LS09	0.24
74LS10	0.24
74LS11	0.24
74LS13	0.34
74LS14	0.50
74LS15	0.24
74LS20	0.24
74LS21	0.24
74LS22	0.24
74LS24	0.50
74LS26	0.24
74LS27	0.24
74LS28	0.24
74LS30	0.24
74LS32	0.24
74LS33	0.24
74LS37	0.24
74LS38	0.24
74LS40	0.24
74LS42	0.50
74LS43	1.50
74LS48	0.90
74LS49	1.00
74LS51	0.24
74LS54	0.24
74LS55	0.24
74LS73A	0.36
74LS74A	0.35
74LS75	0.45
74LS76A	0.36
74LS78	0.42
74LS83A	0.70
74LS85	0.75
74LS86	0.35
74LS90	0.48
74LS92	0.35
74LS93	0.54
74LS95B	0.75
74LS96	0.90
74LS107	0.40
74LS109	0.40
74LS112	0.45
74LS113	0.45
74LS114	0.45
74LS122	0.70
74LS123	0.80
74LS125	0.50
74LS126	0.50
74LS132	0.65
74LS133	0.55
74LS136	0.45
74LS138	0.55
74LS139	0.55
74LS145	0.95
74LS147	1.75
74LS148	1.40
74LS151	0.55
74LS152	2.00
74LS153	0.65
74LS154	1.60
74LS155	0.65
74LS156	0.65
74LS157	0.50
74LS158	0.50
74LS160A	0.65
74LS161A	0.75
74LS162A	0.75
74LS163A	0.75
74LS164	0.75
74LS165A	1.10
74LS166A	1.50
74LS168	1.30
74LS169	1.00
74LS170	1.60
74LS173A	1.00
74LS174	0.75
74LS175	0.75
74LS181	2.00
74LS183	1.90
74LS190	0.75
74LS191	0.75
74LS192	0.75
74LS194A	0.75
74LS195A	0.75
74LS196	0.80
74LS197	0.80
74LS221	0.90
74LS240	0.90
74LS241	0.90
74LS242	0.90
74LS243	0.90
74LS244	0.70
74LS245	0.90
74LS247	1.10
74LS248	1.10
74LS249	1.10
74LS251	0.75
74LS253	0.75
74LS256	0.90
74LS257A	0.70
74LS258A	0.70
74LS259	1.20
74LS260	0.75
74LS266	0.60
74LS273	1.25
74LS279	0.70
74LS280	1.90
74LS283	0.80
74LS290	0.80
74LS292	14.00
74LS293	0.80
74LS295	1.40
74LS297	14.00
74LS298	1.00
74LS299	2.20
74LS321	3.70
74LS322A	3.90
74LS323	3.00
74LS324	3.20
74LS348	2.00
74LS352	1.20
74LS353	1.20
74LS356	2.10
74LS363	1.00
74LS364	1.80
74LS365	0.50
74LS366	0.50
74LS367	0.52
74LS368	0.50
74LS373	0.70
74LS374	0.70
74LS375	0.75
74LS377	1.30
74LS378	0.95
74LS379	1.30
74LS381	4.50
74LS385	3.25
74LS390	0.80
74LS393	1.00
74LS395A	1.00
74LS399	1.40
74LS445	1.80
74LS465	1.20
74LS467	1.20
74LS490	1.50
74LS540	1.00
74LS541	1.00
74LS608	7.00
74LS610	25.00
74LS612	25.00
74LS624	3.50
74LS626	2.25
74LS628	2.25
74LS629	1.25
74LS640	2.00
74LS640-1	3.00
74LS641	1.50
74LS642	2.50
74LS642-1	3.00
74LS643	2.50
74LS643-1	3.00
74LS644	3.50
74LS645	2.00
74LS645-1	4.00
74LS668	0.90
74LS669	0.90
74LS670	1.70
74LS682	2.50
74LS683	3.00
74LS684	3.50
74LS687	3.50
74LS688	3.50
74LS783	16.00

74S SERIES

74S00	0.50
74S02	0.50
74S04	0.50
74S05	0.50
74S08	0.50
74S10	0.50
74S11	0.75
74S20	0.50
74S22	0.50
74S30	0.50
74S32	0.60
74S37	0.80
74S38	0.80
74S40	0.50
74S51	0.80
74S64	0.45
74S74	0.70
74S85	5.50
74S86	1.00
74S112	0.90
74S113	1.20
74S114	1.20
74S124	3.00
74S132	1.00
74S133	0.60
74S138	1.00
74S139	1.00
74S140	1.00
74S151	1.00
74S153	1.50
74S157	2.00
74S158	2.00
74S163	5.00
74S169	5.50
74S174	3.00
74S175	3.20
74S188	1.80
74S189	1.80
74S194	3.00
74S195	3.00
74S196	3.50
74S200	4.50
74S201	3.20
74S225	5.20
74S240	4.00
74S241	4.00
74S244	4.00
74S251	2.50
74S257	2.50
74S258	2.50
74S260	1.00
74S261	3.00
74S283	2.70
74S287	2.25
74S288	2.00
74S289	2.25
74S299	4.50
74S373	4.00
74S374	4.00
74S387	2.25

Special offer to E&WW readers only – 10% off on all TTLS and CMOS

74ALS SERIES

74ALS00	0.45
74ALS02	0.45
74ALS04	0.50
74ALS08	0.50
74ALS10	0.45
74ALS20	0.48
74ALS32	0.45
74ALS74	0.70
74ALS138	1.50
74ALS139	1.50
74ALS244	4.00
74ALS245	4.75
74ALS573	2.60
74ALS574	4.50
74ALS580	2.60

4000 SERIES

4000	0.20
4001	0.24
4002	0.25
4006	0.70
4007	0.25
4008	0.80
4009	0.45
4010	0.60
4011	0.24
4012	0.25
4013	0.36
4014	0.60
4015	0.70
4016	0.36
4017	0.55
4018	0.60
4019	0.60
4020	0.80
4021	0.60
4022	0.70
4023	0.30
4024	0.48
4025	0.24
4026	0.90
4027	0.40
4028	0.60
4029	0.75
4030	0.35
4031	1.25
4032	1.00
4033	1.25
4034	2.50
4035	0.70
4036	2.50
4037	1.10
4038	1.00
4040	0.60
4041	0.55
4042	0.50
4043	0.60
4044	0.60
4045	1.00
4046	0.60
4047	0.60
4048	0.55
4049	0.36
4050	0.35
4051	0.65
4052	0.60
4053	0.60
4054	0.80
4055	0.80
4056	0.85
4060	0.70
4063	0.85
4066	0.40
4067	2.30
4068	0.25
4069	0.24
4070	0.24
4071	0.24
4072	0.24
4073	0.24
4075	0.24
4076	0.65
4077	0.25
4078	0.25
4081	0.24
4082	0.25
4085	0.60
4086	0.75
4089	1.20
4093	0.35
4094	0.90
4095	0.95
4096	0.90
4097	2.70
4098	0.75
4099	0.99
4501	0.36
4502	0.55
4503	0.38
4504	0.95
4505	3.60
4506	0.90
4507	0.35
4508	1.20
4510	0.55
4511	0.55
4512	0.55
4513	1.50
4514	1.10
4515	1.10
4516	0.55
4517	2.20
4518	0.48
4519	0.32
4520	0.60
4521	1.15
4522	0.80
4526	0.70
4527	0.80
4528	0.65
4529	1.00
4531	0.75
4532	0.65
4534	3.80
4536	2.50
4538	0.75
4539	0.75
4541	0.90
4543	0.70
4551	1.00
4553	2.40
4555	0.36
4556	0.50
4557	2.40
4560	1.40
4566	1.40
4568	2.40
4569	1.70
4572	0.45
4583	0.90
4584	0.48
4585	0.60
4724	1.50
14411	7.50
14412	7.50
14416	3.00
14419	2.60
14490	4.20
14495	4.50
145000	6.50
14599	2.00
22100	3.50
22101	7.00
22102	7.00
40014	0.48
40085	1.20
40097	0.36
40098	0.40
40100	1.50
40101	1.25
40102	1.30
40103	2.00
40104	1.20
40105	1.50
40106	0.48
40107	0.55
40108	3.20
40109	0.80
40110	2.25
40114	2.25
40107	2.80
40163	1.00
40173	1.20
40174	1.00
40175	1.00
40192	1.00
40193	1.00
40194	1.00
40244	1.50
40245	1.50
40257	1.80
40373	1.80
40374	1.80
80C95	0.75
80C97	0.75
80C98	0.75

LINEAR ICs

ADC0808	11.90	LM710	0.48	TBA231	1.20
AM7910DC	25.00	LM711	1.00	TBA800	0.80
AN103	2.00	LM723	0.60	TBA810	0.90
AN-1-5050	1.00	LM725CN	3.00	TBA20	0.80
AY-3-1350	5.00	LM733	0.65	TBA820M	0.75
AY-3-8910	4.90	LM741	0.22	TBA920	2.00
AY-3-8912	8.00	LM7747	0.70	TBA950	2.25
CA3019A	1.00	LM748	0.30	TC9109	5.00
CA3020	3.50	LM1011	4.80	TCA270	3.50
CA3028A	1.10	LM1014	1.50	TCA940	1.75
CA3046	0.70	LM1801	3.00	TDA1010	2.25
CA3059	3.25	LM1830	2.50	TDA1022	4.50
CA3060	3.50	LM1871	3.00	TDA1024	1.10
CA3080E	0.70	LM1872	3.00	TDA1170S	3.00
CA3085	1.50	LM1886	6.00	TDA2002	3.25
CA3086	0.60	LM1889	4.50	TDA2003	1.90
CA3089E	2.50	LM2917	3.00	TDA2004	2.40
CA3090AQ	3.75	LM3302	0.90	TDA2006	3.20
CA3130E	0.90	LM3900	0.80	TDA2030	2.50
CA3130T	1.30	LM3909	1.40	TDA2593	5.00
CA3140E	0.45	LM3911	1.80	TDA2653	7.00
CA3140T	1.00	LM3914	3.50	TDA3560	7.50
CA3146	2.25	LM3915	3.40	TDA3810	7.50
CA3160E	1.50	LM3916	3.40	TDA7000	3.50
CA3161E	2.00	LM13600	1.50	TEA1002	7.00
CA3162E	6.00	M51513L	2.30	TL061CP	0.40
CA3189E	2.70	M51516L	4.50	TL062	0.60
CA3240E	1.50	MB3712	2.00	TL064	0.90
CA3280G	3.00	MC1310P	1.50	TL071	0.40
D7002	6.00	1413	0.75	TL072	0.70
DAC1408 8	3.00	MC1458	0.45	TL074	1.10
DAC0800	3.00	MC1495	3.00	TL081	0.35
DAC0808	3.00	MC1496	0.70	TL082	0.55
DG308	3.00	MC3340P	2.00	TL083	0.75
HA1366	1.90	MC3401	0.70	TL084	1.00
ICL7106	6.75	MC3404	0.65	TL094	2.00
ICL7611	0.95	MF10CN	4.10	TL430C	1.20
ICL8038	4.00	MK50240	9.00	UA759	3.20
ICM7555	0.90	ML902	5.00	UA2240	1.20
ICM7556	1.40	ML922	4.00	UCN5801A	5.00
LC7120	3.00	MM6221A	3.00	ULN2001A	0.75
LC7130	3.00	NE529	2.20	ULN2002A	0.75
LC7131	3.50	NE531	1.20	ULN2003A	0.75
LC7137	3.50	NE544	1.90	ULN2004A	0.75
LF347	1.20	NE555	0.22	ULN2068	2.90
LF351	0.60	NE556	0.60	ULN2802	1.90
LF353	0.90	NE564	4.00	ULN2803	1.80
LF355	0.90	NE565	1.20	ULN2804	1.90
LF356N	1.10	NE566	1.50	UPC575	2.75
LF357	1.00	NE567	1.25	UPC592H	2.00
LF398	4.00	NE570	4.00	UPC1156H	3.00
LM10CLH	4.50	NE571	3.00	UPC1185H	5.00
LM301A	0.30	NE592	0.90	XR210	4.00
LM307	0.45	NE5532P	1.50	XR2206	4.50
LM308CN	0.75	NE5533P	1.80	XR2207	3.75
LM310	2.25	NE5534P	1.20	XR2211	5.75
LM311	0.60	NE5534AP	1.50	XR2216	6.75
LM318	1.50	OP-07EP	3.50	XR2249	1.20
LM319	1.80	PLL02A	5.00	ZN404	1.00
LM324	0.45	RC4136	0.55	ZN414	0.80
LM334Z	1.15	RC4151	2.00	ZN419P	1.75
LM335Z	1.30	RC4195	1.50	ZN423E	1.30
LM336	1.60	RC4558	0.55	ZN424E	1.30
LM339	0.40	S50240	9.00	ZN425E8	3.50
LM348	0.60	SFF96364	8.00	ZN426E8	3.00
LM358P	0.50	SL490	3.00	ZN427E8	6.00
LM377	3.00	SN76013N	5.00	ZN428E8	4.50
LM380N 8	1.50	SN76033N	5.00	ZN429E8	2.25
LM380N	1.50	SN76115N	2.15	ZN447E	9.00
LM383	3.25	SN76489	4.00	ZN448I	7.50
LM384	2.20	SN76495	4.00	ZN449E	3.00
LM386N-1	1.00	SN76660	1.20	ZN450E	7.50
LM387	2.70	SPO256AL2	7.00	ZN459CP	3.00
LM391	1.80	SP8515	7.50	ZN1034E	2.00
LM392N	1.10	TA7120	1.20	ZNA1040	6.60
LM393	0.85	TA7130	1.40	ZNA134H	23.00
LM394CH	4.00	TA7204	1.50	ZNA234E	9.50
LM709	0.35	TA7205	0.80		
		TA7222	1.50		
		TA7310	1.50		

VOLTAGE REGULATORS

1A FIXED VOLTAGE PLASTIC TP220

+ VE		− VE	
5V 7805	0.45	7905	0.50
6V 7806	0.50	7906	0.50
8V 7808	0.50	7908	0.50
12V 7812	0.45	7912	0.50
15V 7815	0.50	7915	0.50
18V 7818	0.50	7918	0.50
24V 7824	0.50	7924	0.50

1A FIXED VOLTAGE PLASTIC TO92

5V 78L05	0.30	5V 79L05	0.45
6V 78L06	0.30	12V 79L12	0.50
8V 78L08	0.30	15V 79L15	0.50
12V 78L12	0.30		
15V 78L15	0.30		

OTHER REGULATORS

FIXED REGULATORS

LM309K	1A 5V	1.40
LM323K	3A 5V	3.50
L78H05KC	5A 5V	7.50

VARIABLE REGULATORS

LM305AH		2.50
LM317T	TO-220	1.20
LM317K	TO3	2.40
LM337T		2.25
LM350T		4.00
LM723N		0.50

SWITCHING REGULATORS

ICL7660	2.50
SG3524	3.00
TL494	3.00
TL497	2.25
78S40	2.50
RC4195	1.50

COMPUTER COMPONENTS

CPUs

1802CE	6.50
2650A	10.50
6502	4.50
65C02-2MHz	12.00
6502A	6.50
6502B	6.00
6800	3.50
6802	3.50
6809	6.50
6809E	10.00
68B09	10.00
68B09E	12.00
68000-L8	36.00
8035	3.50
80C35	6.00
8039	4.20
80C39	7.00
8080A	9.50
8085A	3.00
80C85A	7.50
8086	22.00
8087-5	£120
8087-8	£160
8088	17.50
8741	15.00
8748	10.00
TMS1601	12.00
TMS9980	14.50
TMS9995	16.00
V20-8	12.00
V30-8	12.00
Z80	2.50
Z80A	2.90
Z80B	5.50
Z80H	7.50
TMS4500	14.00
TMS9901	5.00
TMS9902	6.00
TMS9914	14.00
Z80PIO	2.50
Z80APIO	2.75
Z80CTC	2.50
Z80ACTC	2.75
Z80DART	6.50
Z80ADART	7.00
Z80DMA	7.00
Z80ADMA	7.50
Z80ASIO/0/2/9	7.00
Z80BPIO	5.00
Z80BPIO	9.00
Z80BCTC	5.00
Z80BDART	9.00

SUPPORT DEVICES

2651	12.00
3242	6.00
3245	4.50
6520	3.00
6522	3.50
6522A	5.50
6532	4.80
6551A	6.00
6821	1.60
68B21	2.50
68040	3.75
68B40	6.00
6850	1.80
68B50	2.50
6852	2.50
6854	4.50
68B54	6.00
8154	6.50
8155	3.80
8156	3.80
8205	2.25
8212	2.00
8216	1.60
8224	POA
8226	4.25
8228	5.50
8237	6.50
8243	2.60
8250	12.00
8251A	3.25
8253C-5	3.50
8255AC-5	3.20
8256	16.00
8257C-5	54.00
8259C-5	4.00
8275	29.00
8279C-5	4.80
8282	4.00
8284	4.60
8287	3.80
8288D	6.50
8755A	18.00

MEMORIES

2114-3	1.00
4116-20	1.50
4164-12	3.20
4164-15	2.75
5101	5.00
6116-3	6.50
6810	2.50
41256-12	7.50
41256-15	7.50
41464-12	9.50
41464 15	9.50
62256-12	12.00

PROMS

28L22	4.00
74S188	1.80
74S287	2.25
74S288	1.80
74S387	2.25
82S23	1.50
82S123	1.50
82S129	1.75

IBM AMSTRAD UPGRADES

8075-5	£90
8087-8	£160
80287-5	£160
80287-8	£220
80287-10	£260

EPROMs

2716 +5V	4.50
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Revolution or evolution?

Broadcast engineers and technical operators seldom venture into the minefield of administrative and political matters, yet currently are facing an unprecedented and orchestrated attack upon the systems they have helped to evolve.

For several years European broadcasters and industry have been developing new technology including MAC and HD-MAC. Active participants have included IBA and BBC engineers, with the encouragement and latterly the financial support of the British Government. The theme has been "evolution not revolution", reflecting the view that the introduction of new technology must take into account investment by viewers in receivers and video recorders and the historical evidence that new channels (such as Channel 4 in 1982) are introduced more smoothly when no radical change is involved – as was the case with the BBC-2 launch in 1964, with the switch to uhf and 625 lines.

IBA engineers have always stressed that since dbs must necessarily involve the change to frequency-modulated vision, it gave a unique opportunity to introduce MAC in a more-or-less compatible manner without significantly adding to the cost for the viewer. Nevertheless, in advertising the franchise won by BSB, the IBA emphasized the high risk of financial disaster in such projects.

Now the Government has thrown caution and history to the winds in its White Paper "Broadcasting in the 90s: competition, choice and quality". It opts firmly for "revolution not evolution" in seeking to destroy the IBA, to downgrade and fragment the ITV network, auctioning it off as Channel 3 on a once-and-for-all payment to the highest bidders, who will then be subjected to a virtually unrestrained company take-over jungle. It expresses the aim but not the method of fragmenting both the BBC and IBA transmission systems into the private sector as competitive regional operations and limits the engineering commitment of the new Independent Television Commission to frequency and coverage planning.

No mention whatever is made of the engineering research and development departments which, within the BBC, IBA and ITVA, have repeatedly been prepared to tackle long-term projects, including digital video and satellite transmission systems, initially beyond the resources of the hard-pressed UK broadcast equipment industry. How Japanese firms must welcome the White Paper!

Despite the skilful window-dressing in this Home Office "glossy", it bears more than one set of fingerprints and could be summed up as "Maggie's revenge: never mind the quality, feel the choice and let who dares gamble on the wheel-of-fortune."

While superficially the BBC may appear to have escaped lightly, other than in the possible selling off of its transmitters, it will apparently remain under the fatal threat of its licence revenue being phased out in favour of "subscription" which, with the competition of "free" commercial channels, would make it a tiny minority "public service" element.

Deregulation and delicensing may "sell" the proposals to the public and enable the Government to force through the necessary legislation. No matter that they will turn both programme-making and engineering topsy-turvy in gambling on the concept that market forces will give the viewers what they want; no matter how cheaply the programmes have to be made or, with no quota, almost entirely bought-in. Industry may reap short-term benefits in catering for new satellite and microwave channels and an enforced 25 percent of independent production. The Treasury clearly expects to benefit from companies buying channels and from a levy based on gross advertising revenues.

Several European countries entrust broadcast transmission to PTTs but the UK terrestrial system has been as successful as any and better than most. As the Americans say, "If it ain't broke, don't fix it". If coverage had depended on market forces alone, many rural areas in the UK, where coverage is 99.4 percent, would have no hope of receiving good television signals.

Perhaps, as one who worked at the IBA under Sir Robert Fraser, chief architect of ITV, and Sir Brian Young, chief architect of Channel 4 I am prejudiced. I still believe that the IBA's Television (programme) Division and Advertising Control, as well as the Engineering Division, contributed, for all their occasional lapses, to the establishment of a unique form of commercially-funded public service broadcasting, that has served the viewer well. It seems incredible that such a system should now be subject to revolution rather than evolution.

Outlook uncertain

Robert Harris in *The Observer* ("Maggie's Ministry of Fear", 30 October, 1988) noted many parallels between the Prime Minister's style of government and the teaching of Niccolò Machiavelli in "The Prince" – for example, "It is far better to be feared than loved". Certainly within broadcasting she has inspired more fear than love. But in attempting to take British television away from its traditional Reithian concept of public service broadcasting, she might perhaps be wise to remember that Machiavelli also wrote: "There is nothing more difficult to take in hand; more perilous to conduct, or more uncertain in its success than the introduction of a new order of things, because the innovator has for enemies all those who have done well under the old conditions, and lukewarm defenders in those who may do well under the new."

It is not only those of us who have been involved with the system (and who could be accused of prejudice) who view Government proposals with surprise and alarm. An American journalist, William Piaff, writing in the *International Herald Tribune* "Thatcher's grudge against the world's best TV system" comments: "It will come as a surprise to many that Britain is about to destroy the best television system in the world. Rightly or wrongly, that is what most foreigners think of the BBC-ITV system. To destroy it might seem crazy, but that is what Prime Minister Margaret Thatcher seems determined to do. Her motives are ideological and political. Mrs Thatcher is committed to private, not public, enterprise – to an absolute minimum of state involvement in national life. She thinks the existing commercial system in Britain is elitist, exercising an advertising monopoly, and guilty of inefficient commercial practice. She wants to substitute a programme production system driven entirely by market forces. Her political motivation is that she believes both BBC and ITV are biased against her and her government. She has always lived by the political rule of 'is he one of us, or is he one of them?'"

Will we soon, despite technological progress, soon be identifying and looking back on "the past golden age of British television"?

TV in brief

In his IEE talk, "The outcome of the ITU **Space WARC 1988**" (ORB-88), Dr Keith Shotton (DTI) reported that choice of a frequency allocation for wide-band high-definition television, possibly in the range 12.7 to 23GHz, was referred to a future conference; similarly it was left to a future conference to decide on a frequency allocation for satellite (digital) sound broadcasting, the decision to be based on a detailed examination of the frequency range 0.5 to 3GHz following further CCIR studies. In answer to my question, whether ORB-88 had considered the problems posed by the proposed use (by Astra) of fixed satellite service (FSS) frequencies for direct reception in the home (a breach of the intentions if not the letter of the ITU Radio Regulations although legalized in the UK by DTI), Dr Shotton pointed out that this matter was not raised at ORB-88, although a number of countries indicated that they intend to use the 11GHz FSS band primarily for television distribution to cable networks etc. A broadcast satellite service feeder-link plan was adopted for Regions 1 and 3 largely in the 17.3 to 18.1 GHz band, including the use of power control to take account of rain fade margins (in Europe the power control range is limited to a dB or so).

Television Topics is written by Pat Hawker.

UK geophysical broadcasts soon?

The Propagation Studies Committee of the Radio Society of Great Britain is hoping soon to provide a nationwide service of geophysical data broadcasts, including information on current sunspot count, solar flux and magnetic index. These are intended to replace the French low-frequency broadcasts from Ste Assise of data obtained at the Meudon Observatory, which have now been discontinued.

Encouragement for the scheme is coming from the amateur radio member-societies of the IARU, from DTI, RAL etc. and from industry. The Marconi Company has offered to donate a 1kW hf transmitter and there is a possibility that this could be sited at a University of Sheffield test site at Buxton, Derbyshire.

Transmissions would consist of "Ursigram"-type messages, using morse and/or radioteleprinter, at hourly or half-hourly intervals, on a frequency of the order of 3500-40000kHz, preferably outside the UK amateur band (3500 to 3800kHz) if DTI approval can be obtained. Alan Taylor, G3DME, who organizes existing RSGB "beacon" transmissions, is hoping that the scheme will attract further approval and support from organizations involved with radio physics, both in the UK and western Europe.

At present one of the most useful guides to real-time ionospheric propagation conditions remains the unique series of beacon stations which transmit continuously on 14 100kHz and which it is hoped to extend to a 15-station network on three different amateur bands over the next five years. This system, organized by the Northern California DX Foundation, comprises a co-ordinated system of automatic beacon transmissions with each beacon operating in sequence for one minute at ten-minute intervals from: New York (4U1UN, time 00); California (W6WX, 01); Hawaii (K6HO, 02); Japan (JA2IGY, 03); Israel (4X4TU, 04); Finland (OH2B, 05); Azores (CT3B, 06); South Africa (ZS6DN, 07); and Argentina (LU4AA, 08). Each transmission comprises the general call "QST" followed by the callsign and a series of long dashes with descending power output.

Some recent problems have included the theft of the unattended beacon transmitter W6WX from Stanford University, California and increasing interference on 14 100kHz from amateur "packet" data transmissions. Nevertheless during much of the time, three, four or more of the beacons are usually receivable in the UK, providing an excellent means of assessing current propagation conditions.

Cycle 22 puzzles

Radio Broadcast (*E&WW*, August 1988, p832) noted the forecast by Dr Geoffrey Brown (University College of Wales) that the current solar cycle 22 may have one of the highest sunspot maxima on record, a prediction he based on the use of precursors such as the number of geomagnetic abnormal quiet days during the declining period of the preceding cycle. This led him to predict a maximum sunspot number of 174 ± 35 with the maximum in 1990±1.

However, Robert M. Wilson of the NASA Marshall Space Flight Center in *Nature* (27 October, 1988, p773) has questioned the validity of this and other recent predictions by R.P. Kane, K.H. Shatten, G. Gonsalez and R.J. Sargent of a very high maximum based on a variety of linear fits. In contrast he believes that bivarite fits have proved highly correlative with much smaller standard errors and so are inherently more reliable as a basis for predictions. He considers the most reliable for predicting R_{max} uses the minimum annual averages of sunspot number R_{min} and the Ap index, Ap_{min}, which he suggests has a correlation coefficient of 0.997 and a standard error of only 3.9. For cycle 22, R_{min} in 1986 was 13.4 and Ap_{min} in 1987 had a value of 11.0. This implies that R_{max} should be about 144.6 ±7.8 (the low end of Dr Brown's range), less than both cycles 21 (164.5) and 18 (151.8) and roughly similar to cycle 11 (140.5), making it only the fourth or fifth largest recorded cycle.

Robert Wilson concludes: "Cycle 22 probably will not be an exceptionally large, record-setting cycle, although it will be above average in size." The next couple of years will put all these predictions to the test.

Defeating hackers

The revelation that over several years, 23-year-old hacker Edward Singh was able to gain access to information stored in over 200 military, space, nuclear, commercial and academic computer data banks on both sides of the Atlantic has once again underlined the shortcomings of password-handshake security techniques in systems designed to be accessed from remote terminals. His use of Joint Academic Network terminals at Surrey University has led to renewed calls to criminalize hacking in the UK, as it is already in the USA, Canada, Sweden and France. While such a measure might or might not deter the "amateur" hacker it would not deter those whose motivation is fraud (usually an insider activity) or industrial or military espionage since these are already "crimes". In Texas, a computer programmer, Donald Burleson, recently became the first person to be convicted of computer sabotage in breach of a State law prohibiting "harmful access to a computer". He received a suspended sentence of seven years and was ordered to pay $11 800 compensation.

At present in the UK it is not, as a recent inquiry noted, a criminal offence to use a piece of machinery belonging to somebody else provided that the machine is returned undamaged to its owner. Nor is it a crime to gain unauthorized access to confidential information unless this is used to commit a specific criminal offence such as fraud, although the position in regard to Government secrets could be affected if the Official Secrets Act is changed in the manner proposed. It is planned to convert sensitive Government and defence computer networks to incorporate a computationally-secure, multi-level cryptosystem that would limit the access of terminals to specific files, that is currently under development at the Royal Signals of Radar Establishment as SCP2. However, the security of any cryptosystem depends on its being used correctly within a set of rules or procedures, known as the protocol. The increasing amount of computer power that can be used to attack high-grade ciphers has also to be taken into account.

This has been made clear by the success of an international group of computer scientists in factoring a 100-digit number into two large prime numbers, without incurring any costs in paid-for computer time. By using the down-time of some 400 computers in the USA, Australia and Holland, they solved a problem that had been estimated previously as requiring six months' on a Cray supercomputer.

According to a report in *Nature*, the success of this project – organized jointly by Arjen Lenstra of the University of Chicago and Mark Monasse of the DEC Research Centre – depended on the work of Robert Silverman (Mitre Corporation) who in 1985 devised a means of breaking up the factorization algorithm to enable it to be run in parallel on a large number of computers.

Clearly this development represents a potential threat to the security of the RSA public-key (two key) cryptosystem which is generally regarded as computationally-secure. RSA cryptosystems have in practice been entirely secure because of the enormous computer power required to factorize two large prime numbers multiplied together. Hundred-digit numbers have previously been regarded as secure but, following the DEC project, it is now being recommended that at least 150 digits should be used (this would require 100 000 times more computer-power to factorize than a 100-digit number). Mark Manasse believes it may be possible to factorize numbers greater than 100 digits by using 5000 to 20 000 computers and is planning such an attempt. With a public-key system, once the secret number is recovered the information can be read without undue difficulty. The RSA system can thus not be regarded as entirely secure without the use of very large prime numbers.

Radio Broadcast is written by Pat Hawker.

RADIO BROADCAST

POWER-side am broadcasting

Leonard R. Kahn, for many years the leading advocate of compatible single-sideband (cssb) and independent-sideband (isb) stereo-am techniques, has now proposed what, in effect, is a combination of these techniques as a means of significantly improving the reception of am monophonic broadcasts. He claims (*IEEE Trans. on Broadcasting*, September 1988, pp407-420) that the system, for which he has registered the name POWER-side, would allow listeners to "sideband tune" with new types of mono receivers in order to reduce co- and adjacent-channel interference; and that it would improve the effective fidelity of an a.m receiver as well as making its tuning *less* critical. Additionally, his system with special audio processing and unequal low-frequency sideband components would reduce selective fading and distortion due to antenna nulls and re-radiation problems on both "sideband-tuned" and digitally-tuned isb stereo and mono receivers tuned to the carrier frequency.

Kahn also stresses that "most importantly this type of wave substantially reduces co-channel beating effects that have, since the earliest days of broadcasting, plagued am signal reception." In effect, POWER-side transmissions can be implemented by using one of a pair of Kahn-Hazeltine isb-stereo exciters (FCC-approved models STR77/84) plus a special audio processor. One set of sidebands is reduced by 10dB, the other raised by 3.5 to 4.7dB compared with conventional dsb.

He reports that on-air tests by WMCA, New York (raising the upper sideband) and WSYR, Syracuse (raising the lower sideband), both on assigned channel 570kHz, achieved significant reduction of mutual interference. At night, he claims, a listener only seven miles from WSYR and 250 miles from WMCA is able to receive an intelligible signal from WMCA when using an isb-type am stereo receiver.

In the 1960s, European broadcasters investigated and then rejected several systems of cssb broadcast techniques, claiming that with envelope detection there was excessive quadrature distortion unless pre-correction audio processing was applied, which in itself represented a form of distortion on existing receivers. However, since then many UK and European broadcasters have adopted audio processing; and synchronous demodulation, free of quadrature distortion, can now be implemented at costs within the range of consumer electronics. Kahn points out that cssb is used successfully for air-to-ground communications.

Work on early forms of broadcast cssb was carried out in the 1930s in the UK and Holland but was considered to result in excessive distortion. Leonard Kahn proposed a system offering much reduced distortion which he described in *Proc. IRE*, October 1961. A simplified form of Kahn's system was used on the long-wave Voice of America station at Munich in the 1960s that made use of the Radio Moscow channel. Philips developed an alternative system described in *EBU Review*, Part A, February 1962.

Woes of am-stereo

Writing from South Africa, Joh Hansen comments on the way that commercial rather than technical problems have contributed to the woes of am-stereo (see *Radio Broadcast*, August 1988) in that country. Directed at listeners around Johannesburg, C-QUAM am-stereo was introduced on commercial broadcasting from the Bophuthatswana 702 (702 kHz) transmitter located in the so-called black homeland, some 100km from Johannesburg. This was in 1984 when 702 was losing listeners to the state-controlled non-commercial fm transmissions within South Africa.

Much publicity, including distribution for a number of Sony am-stereo receivers, attended the launch. For a time some of the night-time presenters were persuaded to make the 200km return trip to the transmitter to play out stereo recordings instead of using the 702 studio in Johannesburg which is connected to the transmitter by a landline suitable only for mono. But the peak-time, daylight programmes continued to be originated in Johannesburg and remained in mono, although the 25kHz stereo pilot-tone was left on.

Neither listeners nor local industry was told that most daytime programmes were mono-only. Joh Hansen's firm developed a retrofit am-stereo module based on the Motorola MC13020 decoder chip (about £8 each) but this proved an expensive way of merely switching on a light-emitting diode since it was usually impossible to demonstrate stereo to potential customers during business hours. For a time the 702 management would not confirm the real reason why transmissions remained in mono despite the stereo pilot indicator. Then it decided that since so few people were equipped with stereo receivers it could not justify the cost of installing a stereo-capable link from the Johannesburg studio to the transmitter in Bophuthatswana.

The result is that the station, proclaimed on letterheads and publicity posters as a "stereo" station, now transmits in stereo infrequently because few people have stereo sets, while nobody is buying stereo sets because they can't hear stereo demonstrated.

Commenting technically on C-QUAM stereo received over a relatively long distance with African 9kHz channelling, Joh Hansen believes there are two inevitable compromises:

Noise: Although Motorola claims there is only an insignificant increase in noise when the set is switched to the stereo mode, this appears to be true only with strong, local signals. Synchronous detection of the lower-amplitude Q-component introduces both atmospheric and receiver noise. While this may be corrected by coupling a loop antenna into the tuning circuit of the tuner, unless this is done carefully it tends to have a detrimental effect on the bandwidth of the rf/if stages and overall audio response. By contrast, local fm stereo requires a relatively simple antenna.

Bandwidth: Experiments with the IEEE "wideband" a.m tuner using weakly coupled rf stages achieved an audio response to 8kHz, making am mono sound remarkably similar to fm-mono. However on switching to the stereo mode, there tended to be excessive adjacent channel breakthrough, especially of the higher audio frequencies. In South Africa, the am stations, operating outside the Republic, tend to be bunched together at the lower-frequency end of the broadcast band in order to maximize daylight range. In practice, with nominal (Region 1) 9kHz channels, the maximum usable audio bandwidth appears to be about 5kHz, perfectly acceptable for portable or car-radio reception but at a disadvantage to fm with full-range equipment.

Can am stay alive?

The BBC-organized Radio Show at Earl's Court, which attracted some 100 000 visitors, placed much emphasis on the benefits of fm reception and the potential value of RDS (Radio Data System), though it was by no means clear whether this was entirely on the grounds of better reception or was motivated by BBC Radio's current fear of losing much of its audience when it is forced to give up some medium-wave frequencies. There is also the problem that if the bulk of listeners adopt fm this might block the possible introduction of multiplexed digital audio channels for which microwave frequencies are being sought and for which the BBC appears to be pressing for a new 20-bit digital production standard.

There was a distinctly frosty BBC reply to Norman McLeod's letter to *The Independent* newspaper, in which he suggested that "RDS is an incredibly complicated and expensive system, suited mainly to up-market digital radios. . . if you are bright enough to be able to turn a knob to the right station, there is very little else RDS has to offer." Instead he proposed a "save am radio campaign" pointing out that he still would not swop the tone of his 1957 wireless set for a Compact Disc player worth fifty times as much, adding: "Progress? What progress?"

Radio Broadcast is written by Pat Hawker.