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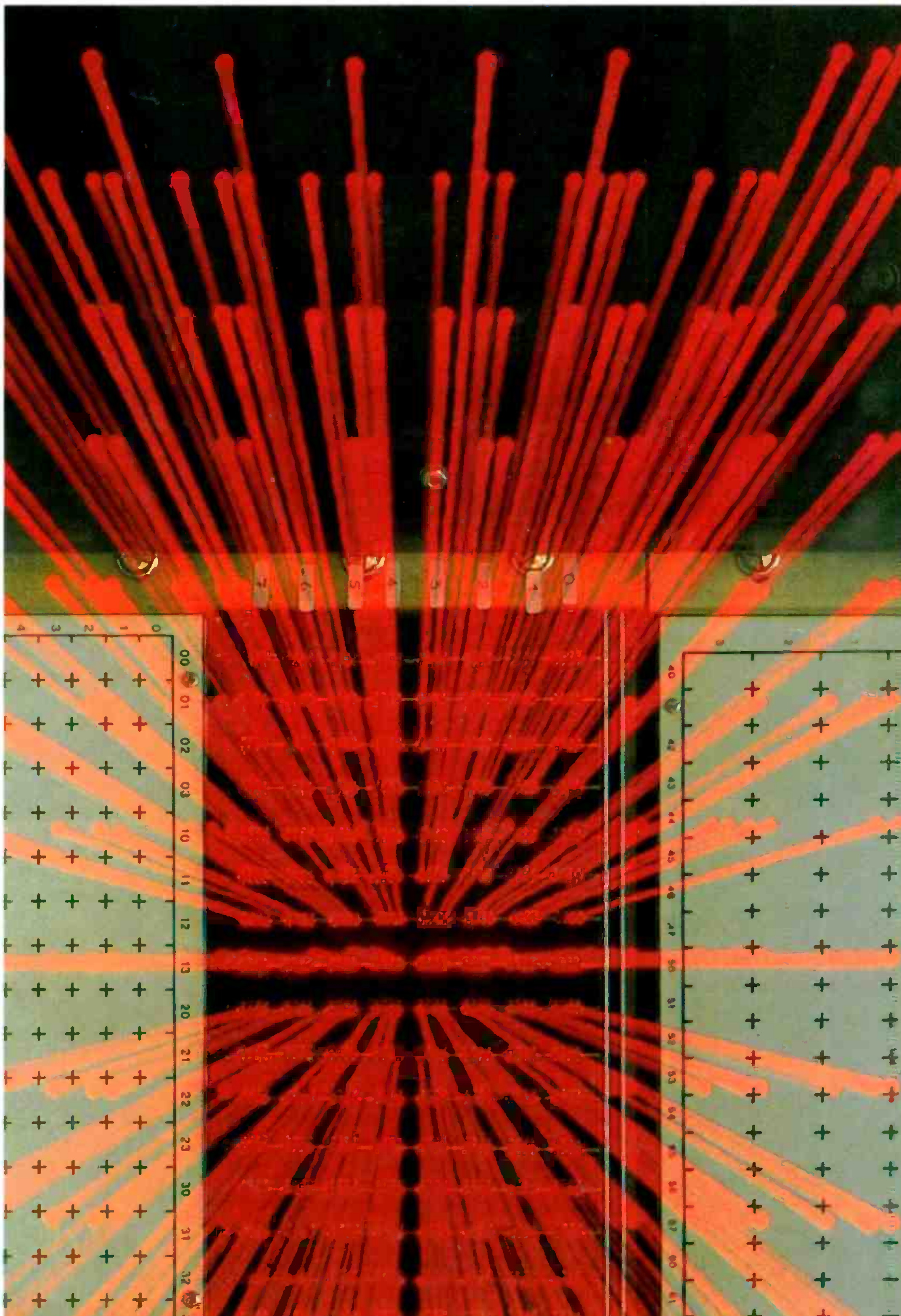

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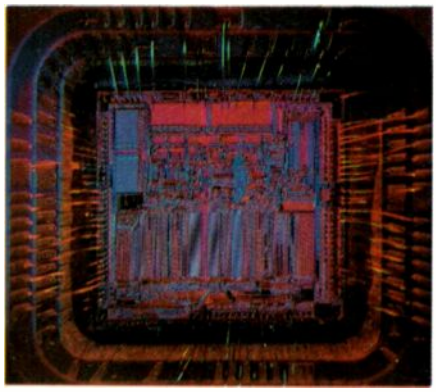

Motorola's 68020 chip. See the article on page 209.

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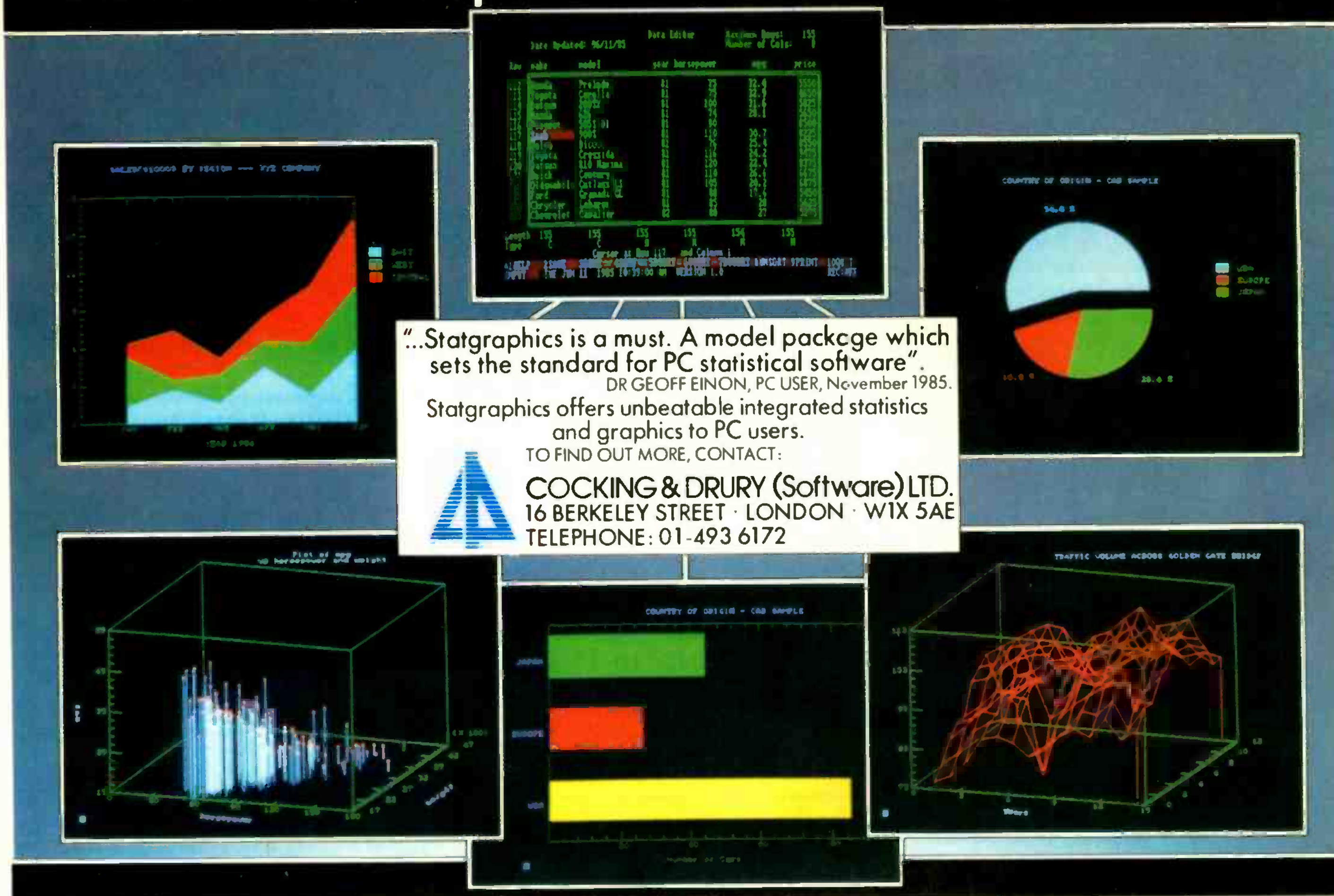

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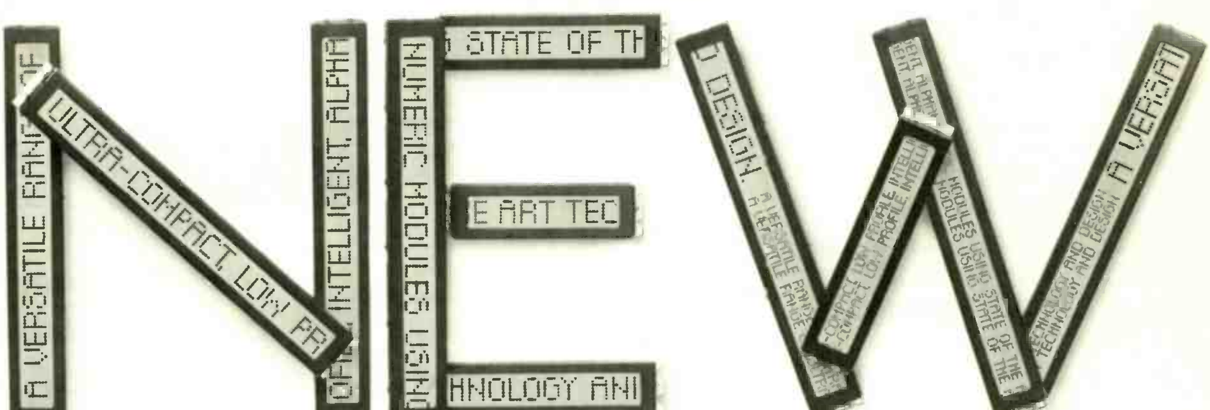

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COMMENT

Political semiconductors

Industrial societies are now permeated by electronic technology to such an extent that they can fairly be said to be commercially dependent on their ability to design and manufacture electronic equipment. It is clearly not, therefore, in their best interests to allow foreign manufacturers to monopolize the base of this essential activity, which is the production of semiconductor devices. If this footing is removed from its direct control, the majority of a country's industry loses much of its independence and, with this loss, the ability to innovate.

In the teeth of North American and Far Eastern domination of semiconductor technology, Europe is in an extremely difficult position – and it cannot be long delayed before the Americans find themselves similarly placed. Japanese manufacturers have already virtually enclosed the market for memories, are well on the way to the same performance with microprocessors and peripheral i.cs and, with that accomplished, will be able largely to dictate the development of hardware anywhere in the world.

In the absence of some kind of EEC financial assistance, the only way a relatively small (compared with Japanese or American) semiconductor industry can survive is to concentrate on the type of device not seen as spectacularly profitable by the large companies – usually quite advanced and therefore expensive to develop and produce. By doing this a small industry can survive, but on the wider EEC scene these small-scale specialized operations are of no help at all in retaining control of Continental industrial development.

It is essential that a full range of semiconductors should be produced by an industrial community which is determined to preserve industrial – and therefore political – autonomy. To bring this about would entail some difficult decisions including, possibly, the erection of trade barriers and certainly massive Community help with finance. Co-operation between universities and companies and between individual companies would assuredly meet strong resistance but, equally certainly, is one of the keys to the re-building of a sound industry.

Trade barriers are an uncivilized impediment to world trade, and it must be pointed out that even the Japanese now express their willingness to trade in the more conventional, bidirectional manner. But this gradual lowering of Japanese barriers is recent: their semiconductor industry was built up behind the protection of an impenetrable wall of inscrutability, with a high level of government assistance and low costs of borrowing.

If is is agreed that a comprehensive European semiconductor industry is essential and that the hugely successful Japanese industry can be taken as a model, then it may be that their methods, however unpalatable to Western society, may offer a way forward.

Electronics & Wireless World is published monthly USPS 687-540 Current issue price £1.95, back issues (if available) £2.10 at Retail and Trade Counter, Units 1&2, Bankside Industrial Centre, Hopton Street, London SE1 Telephone: 01-928 3567. By post, current issue £2.25, back issues (if available) £2.50. Order and payments to 301 *Electronics and Wireless World*, Quadrant House, The Quadrant, Sutton, Surrey SM2 5AS. Cheques should be payable to Business Press International Ltd. **Editorial & Advertising offices:** *EWW* Quadrant House, The Quadrant, Sutton, Surrey SM2 5AS. **Telephones:** Editorial 01-661 3614. Advertising 01-661 3130 01-661 8469 **Telex:** 892084 BISPRS G (EEP) **Facsimile:** 01-661 2071 (Groups II & III) **Beeline:** 01-661 8978 or 01-661 8986. 300 baud, 7 data bits, even parity, one stop-bit. Send ctrl-Q, then EWW to start; NNNN to sign off. **Subscription rates:** 1 year £18 UK and £23 outside UK. **Student rates:** 1 year £11.50 UK and £14.50 outside UK. **Distribution:** Quadrant House, The Quadrant, Sutton, Surrey SM2 5AS. Telephone 01-661 3248. **Subscriptions:** Oakfield House, Perrymount Road, Haywards Heath, Sussex RH16 3DH. Telephone 04444 59188. Please notify a change of address. **USA:** $49.40 surface mail, $102.60 airmail. Business Press International (USA). Subscriptions Office, 205 E. 42nd Street, NY 10117. **Overseas advertising agents: France and Belgium:** Pierre Mussard, 18-20 Place de la Madeleine, Paris 75008. **United States of America:** Jay Feinman, Business Press International Ltd, 205 East 42nd Street, New York, NY 10017. Telephone (212) 867-2080 Telex 23827. **USA mailing agents:** Mercury Airfreight International Ltd, Inc., 10(b) Englehard Ave, Avenel N.J. 07001. 2nd class postage paid. Postmaster – send address to the above. ISBN 0043 6062

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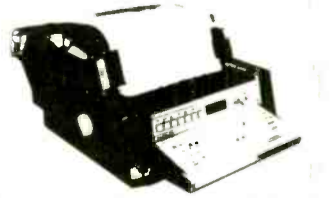

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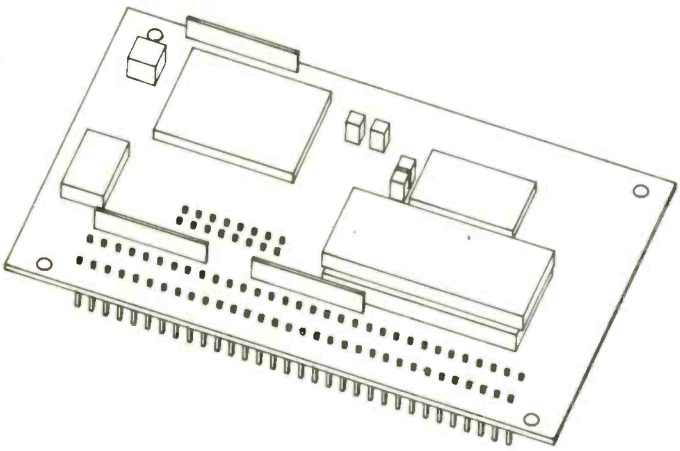

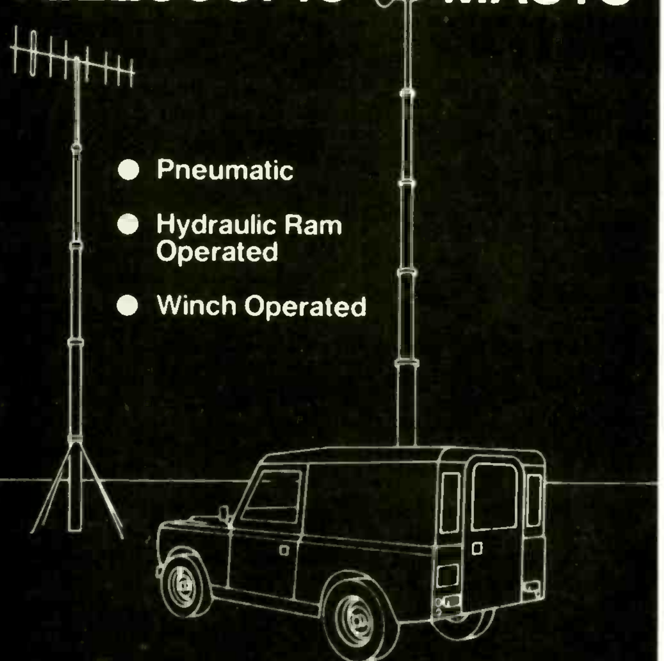

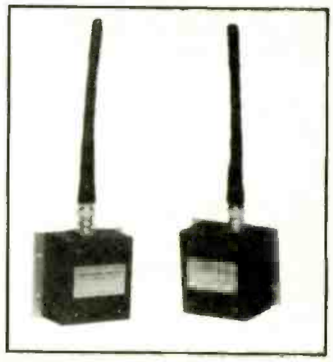

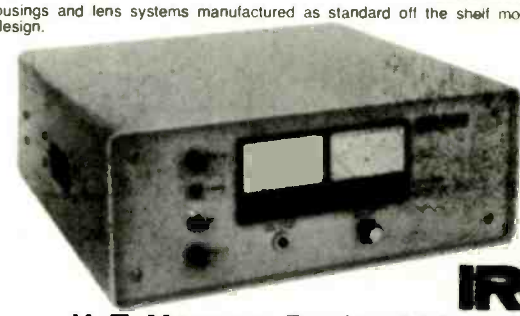

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Displays for instruments

The range of electronic displays available for instrumentation applications has broadened enormously over the last decade: designers are now faced with a bewildering choice of different technologies, each with their own strengths and weaknesses.

BRIAN ROSE

At present, the range of technologies available for use as instrumentation displays breaks down into six different types: light emitting diodes (l.e.ds), liquid crystal displays (l.c.ds), vacuum fluorescent displays (v.f.ds), plasma gas discharge displays (p.g.ds), electroluminescent displays (e.l.ds) and cathode ray tubes (c.r.ts).

Some display technologies are well-established, whereas others have emerged in the last few years as viable displays. Selecting the correct display for a particular application is crucial, particularly as a number of devices may, on initial study, appear to be adequate for a particular requirement. However, unless the characteristics and limitations of a display are understood, it is all too easy to design-in one part, only to find in the course of further development that some aspect of the display imposes unacceptable constraints on the design of the complete instrument or system for which it is intended. The following review summarizes the characteristics, limitations and advantages of the different display technologies and also describes recent developments that have been made, both in the basic technology and in application.

LIGHT EMITTING DIODES

The l.e.d. is one of the most venerable and well established display technologies available. L.e.ds are semiconductor devices that emit light in response to an applied voltage. Typically, the material used for the junction from which light is emitted is gallium phosphide (GaP) doped with elements such as nitrogen and arsenic. By doping a GaP junction with appropriate quantities of a particular dopant, an energy gap can be created between the electronic valence and conduction bands of the gallium phosphide. By the application of a voltage, electrons are promoted from the valence to the conductor band, this promotion being continuous once the voltage is applied, as is the return of electrons from the conductor to the valence band. In dropping from the conductor to the valence band a quantum of light is emitted, the frequency of this quantum being proportional to the energy gap. Thus, by tuning the gap by the use the particular dopants, colours from red, through orange, yellow and green to blue can be produced. For the emission of visible light the energy gap has to be larger than 1.8 electron volts, since the spectral range extends from 1.8 to 3.10 eV, corresponding to an optical wavelength range of 700 to 400nm.

Red and green have always been straightforward colours to produce, although until recently it has been difficult to produce yellow l.e.ds with a tight colour spread and acceptable brightness variation within the batch. For some time, colour and brightness have been selected by batch, but increased control of production has largely eliminated this.

The blue l.e.d. has only been available for a few years and the light output and price still leave a lot to be desired. Consequently, application, for blue l.e.ds have been limited, being mostly restricted to spectroscopy applications.

The basic l.e.d. chips can be packaged in many ways: as individual lamps, as seven-segment and alphanumeric displays, as bargraphs, backlights and dot-matrix displays. As a single indicator the l.e.d. has no competition and when configured as a single seven-segment display, it provides a very cost-effective solution. However, l.e.ds are somewhat power hungry. A single l.e.d. lamp running at 5V and 20mA does not improve much of a power requirement on any system, but when multiple, seven-segment displays are used, the power requirement tends to add up and can be prohibitive.

Being solid-state, l.e.ds are intrinsically robust and can operate over wide temperature ranges (−25 to + 80°C). Reliability is excellent with a 500,000 hour m.t.b.f. a conservative figure these days.

In summary, l.e.ds provide a simple, cheap and reliable display for single indicator, single or dual-digit applications, but where a greater amount of information needs to be displayed cost and power consumption can be prohibitive.

LIQUID CRYSTAL DISPLAYS

After the abortive initial launch of l.c. displays using the dynamic scattering type fluid (unreliable with poor environmental integrity and poor contrast) l.c.ds have now come of age with the use of twisted nematic fluids.

The l.c.d. is an interesting technology as it emits no light. Information is conveyed by modification of incident light, in most cases.

L.c.ds consist of two glass panels sealed together, containing liquid-crystal material. On the inside surfaces of the two glass panels are electrode patterns etched in conductive, transparent indium tin oxide. The inner surfaces of the glass are prepared in such a way as to anchor Liquid-crystal molecules in a fixed position top and bottom and to impose a 90 degree twist in the molecules between the two plates, liquid-crystal material have no effect on normal light but do have the ability to rotate the plane of polarized light. In l.c.ds polarized light is produced by the use of front and rear polarizing filters attached to the outer surfaces of the glass panels. These filters are usually applied with their polarizing axes orthogonal to each other. Thus, with the liquid-crystal molecules in their normal state (twisted and able to rotate the plane of polarized light) any light passing through the l.c.d. and polarizers and reflected back is substantially unaltered. However, when a voltage is applied across the electrodes, the liquid-crystal molecules straighten out, thus losing the ability to rotate the plane of polarization light: hence, any area over which this occurs appears opaque to the viewer.

An enormous range of standard l.c.ds is available from companies such as Hitachi, Sharp, Epson, Varitronix and Toshiba. Displays from a single, half-inch tall, seven-segment digit through 4, 6, and 16 digit units up to large single digits, many inches tall are available.

Many options are available with l.c.ds: there is a choice of viewing mode, connection type, viewing angle and operating temperature range.

Viewing modes can be chosen as restrictive, transmissive and transflective. Reflective displays can only be seen in ambient light, not in darkness. Transmissive displays are designed to be permanently lit from behind (good in the dark, but poor in strong ambient light unless strong backlighting is used.) Transflective displays combine the features of transmissive and reflective units. They can be seen in good ambient light but, since they will permit light to be shone through from behind, a backlight can be switched on in low light levels.

A number of connector types can be used with l.c.ds including push-on pins, bonded pins, elastomeric connectors and heat-bonded connector films. In some cases, due to the number of contacts that have to be brought out in a limited space a high-density elastomeric connector may may to be used. Bonded-pin displays are easy to use and can be inserted in p.c.bs like an i.c.

Due to production constraints, a preferred viewing direction must be selected at the time of manufacture. This is normally 6 o'clock, i.e. viewed from below, but 12 o'clock viewing is available for top viewing as are special angles (such as 3 o'clock for a car-radio application). Standard temperature range for l.c.ds is now 0 to +50°C but some types are available spanning −40 to +85°C. Simple l.c.ds such as 4-digit, half-inch tall digit types are used in great numbers in measuring instruments such as multimeters.

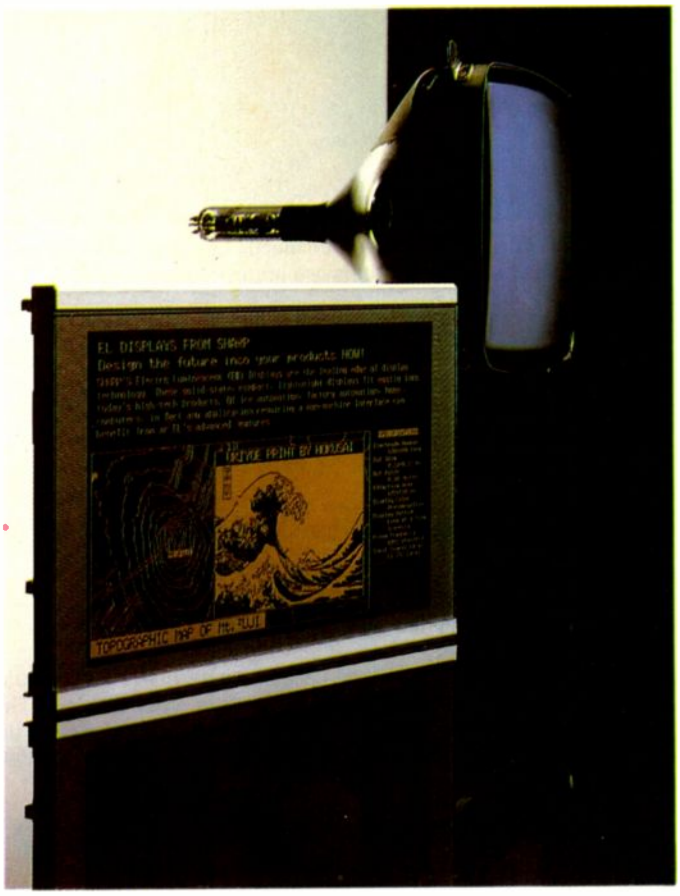
The scope of the l.c.d. has been greatly increased by the availability of custom-designed facilities. Almost all l.c.d. companies now offer a custom service where an l.c.d. can be designed and manufactured to a customer's specifications. This particular area of the market has been tainted in recent years by the activities of certain 'cowboy' companies. Reputable companies include Sharp, Hitachi, Epson, Varitronix and Lucid.

With a custom l.c.d. design, bargraphs, legends and even company logos can be incorporated into one display.

When a larger amount of information needs to be displayed such as several lines of alphanumeric characters then a complete module rather than just an l.c.d. is generally preferred. Modules comprise l.c.d, connectors, elastomers and driver i.cs.

An area of considerable growth in the past few years has been graphic l.c.d. modules. Unfortunately, it is in these products that the shortcomings of l.c.ds become apparent. With large displays (650 by 200 dots for example), each dot needs to be separately addressable.

However, it is impossible to dedicate one contact for each dot: it is necessary to use a multiplex drive system. Many dots share a common electrode and hence unique addressability can only be achieved by a complicated sub-division of drive-voltage levels and reduced address time per drive cycle. The result of a high-duty cycle multiplex drive (100:1 or more) is to give reduced contrast and viewing angle compared with simple l.c.ds: early graphics l.c.ds of 640 by 200 dot size were virtually illegible. Continuing development over the past few years has produced a useful improvement, but the



600 by 400 element electroluminescent display from Sharp.

This vacuum fluorescent display dashboard was designed for the Aston Martin Lagonda, by Kemitron. Road and engine speed r.p.m. are shown on bar-graph gauges, all the usual standard warning symbols are incorporated, and a separate dot-matric display is linked to a speech synthesizer to give system messages.

release this year of new units using the new super-twisted birefringent l.c.d. material has finally produced usable large graphics displays; leaders in this field are Sharp, Hitachi and Epson. Sharp have super-twist units available now with Hitachi and Epson due to follow very soon.

L.c.ds are small and light, if somewhat fragile, due to their thin glass construction. The great advantage is their very low power consumption, in the order of a few milliwatts even for the largest display. However, since they are passive displays and emit no light they are unsatisfactory in low light conditions. Backlighting can of course be used, but this detracts from the low power consumption advantage of the l.c.d. Another major advantage of l.c.ds is their low cost. For a display of four digits and above, there is no cheaper option and this coupled with the availability of a wide range of c-mos driver helps to explain their popularity.

VACUUM FLUORESCENT

The vacuum fluorescent display has been around for many years and although it has been very popular with Japanese equipment manufactures it remains relatively unpopular in the UK.

V.f.ds operate in a similar manner to valves. Electrons from a cathode are accelerated by a potential difference through a grid to impinge (fluoresce) upon a phosphor layer. V.f.ds are identifiable by their attractive bright blue-green colour which is filterable to other colours. Their familiarity in the UK comes from their use in almost every video-cassette recorder: however, they are rarely seen in instrumentation. V.f.ds are bright with good viewing angles, but the vacuum envelope is intrinsically fragile, particularly the "neck" where they are sealed after evacuation. Although attractive, v.f.ds are not a particularly cheap technology, especially when driver costs are borne in mind. There are only three major manufactures – Itron, NEC and Futaba – all Japanese.

PLASMA GAS DISCHARGE DISPLAYS

Plasma displays take the form of a gas-filled space between two electrodes. When a high voltage is applied across the space, the gas molecules ionize and emit light at the electrode surfaces. Neon is the gas most normally used: this requires a discharge of 180V+ and gives a bright orange display. Small displays are not practical with p.g.ds and available units range from 4 digit units to 640 by 400-dot flat panels. Very high brightness (up to 300 foot-lamberts) can be obtained from p.g.ds and this partially explains their popularity as bargraphs in pro-

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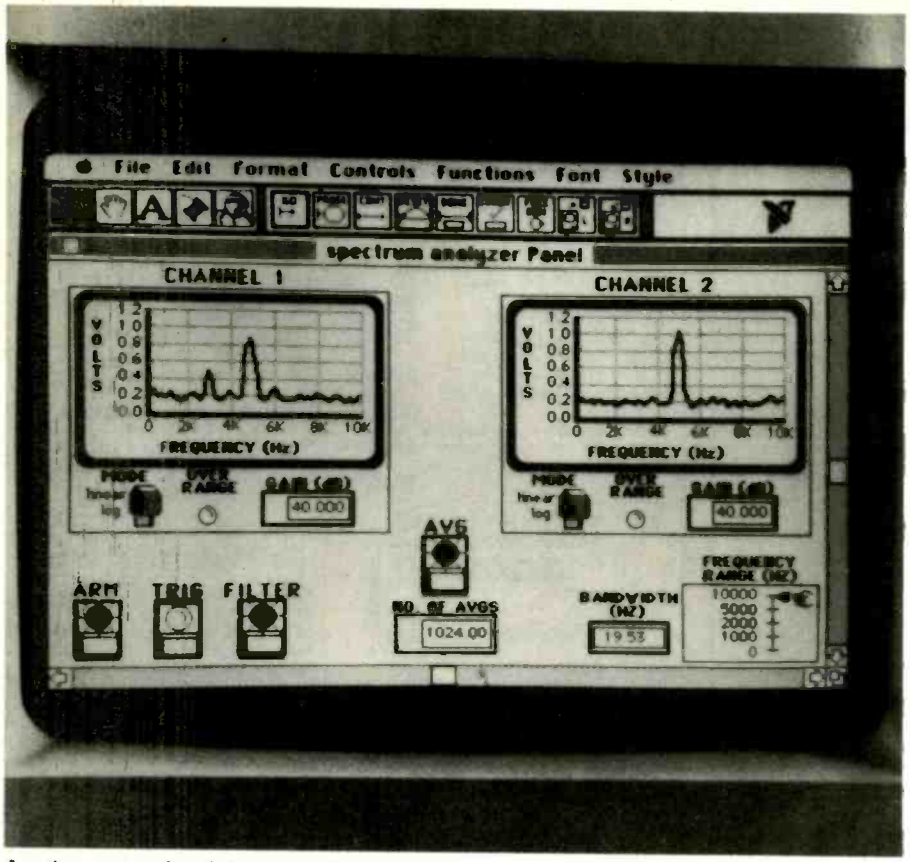
Cathode ray tubes, as well as being instrument display devices in their own right on oscilloscopes etc, can also simulate other displays. This high-resolution c.r.t. from AEG combines the function of several mechanical meters into one display for use in aircraft, all superimposed on a radar map to give all the essential information in a single display.



Another example of the versatility of c.r.ts is provided in the Labview software for the Apple Macintosh computer, available from Amplicon in Brighton. It can display the "front panel" of an instrument connected to the computer through a GPIB interface.

cess control instrumentation.

P.g.ds are most popular in the United States where many years ago Burroughs were the world leader in this technology. Unfortunately, the demise, resurgence and demise again of Burroughs and other spin-off p.g.d. manufacturers led for many years to erratic supply. Japanese companies such as NEC now also manufacture p.g.ds and supply has stabilized somewhat. P.g.ds have been unlucky in attracting a bad press over the last few years. Their flicker has attracted criticism and at one time there was talk of banning p.g.ds for computer terminal applications.

There has also been a (surely) aprocyphal story about the British defence instrumentation manufacturer whose marine p.g.d. displays failed to operate in the darkness of the Arctic circle. Apparently, some ionization of the neon gas needs to be present before an initial discharge can be struck, this ionization being normally provided by light photons which, if absent, prevent strike-up. One method of avoiding this problem is to incorporate minute quantities of radio-active tritium to ionize the neon.

Although popular in the US, p.g.ds have never really taken off in the UK although many large p.g.d. graphics panels now look attractive. Many p.g.d. manufacturers still have not solved the display/driver integration problem and it is not unusual to see p.c.bs stacked four deep on the back of a p.g.d.

ELECTROLUMINESCENT DISPLAYS

Like l.c.ds, e.l. displays had a bad start. There are four types, thin film, thick film, a.c. drive and d.c. drive. Thick film a.c. drive panels have been renowned for their short half-life and this has unfortunately rubbed off on the other variety. The dominant technology is thin-film a.c. drive e.l. panels. These have been pioneered by Sharp in Japan.

E.l. panels consist of two sheets of glass with electrodes etched in indium tin oxide on the internal surfaces. One set of electrodes is orthogonal to the other – when assembled an x-y grid is produced. Sandwiched between the two plates of glass is a thin layer of zinc manganese sulphite. When a potential difference is applied across the phosphor it emits a pleasing yellow-glow. Hence, the panel is completely solid-state with no fragile envelope containing a gas or a vacuum. Integration of display and drivers has been taken to an advanced level with surface-mounted drivers sitting on flexible printed-circuit boards which are attached to the four sides of the display. These boards fold tidely behind the display, resulting in a compact package.

Current Sharp units offer viewing angles of more than 120 degrees in all axes, brightness greater than 20 foot lamberts (68cd/m^2), and high contrast, all in a package less than 35mm thick.

E.l. displays have only been in production for the last five years, but even so, they show signs of becoming the flat-panel display of the future. Unfortunately, e.l. displays are not viable as small units. The smallest display in production is 320 by 240 dots, but the largest is 640 by 400 dots, and is most suitable where a large amount of information needs to be displayed. An interface very similar to that of a c.r.t. has enhanced acceptance and has given e.l. displays an advantage over v.f.ds and p.g.ds.

Outstanding features of e.l. displays are robustness, compactness, brightness, wide angle, stable image and good system integration.

CATHODE RAY TUBES

The cathode ray tube is the oldest of the electronic displays currently in use. In terms of value, more c.r.ts have been sold than all other display types combined. The crude units used for television before the second world war have developed into today's high-resolution monochrome and colour displays. The basic technology of c.r.ts is well known – electrons from a heated cathode are accelerated in a vacuum towards a grid and guided by external magnetic or static forces to impinge on a phosphor coated screen.

Except for esoteric units, no major changes have been made in the basic technology used in the vast majority of c.r.ts supplied today. Instead, detailed improvements in the performance and variety of phosphors, the resolution of screen etching and better yoke design have taken place. The huge volumes of c.r.ts in productions mean that costs are very competitive.

The design of a c.r.t. display package involves trade-offs. Increased resolution is achievable only at the expense of brightness, for example. Tube depth can be reduced by using tubes with large deflection angles, but these angles may jeopardize display quality, due to loss of linearity and poor edge resolution.

Higher scanning rates (up to 64kHz for colour) are now possible, which gives higher resolution and this, together with the achievement of dot pitches down to 0.26mm, has produced c.r.ts more suited to the demands of computer terminals and c.a.d./c.a.m. units. It is, however, in the field of monitors (the integration of c.r.t. into a display system) that most advances have been made.

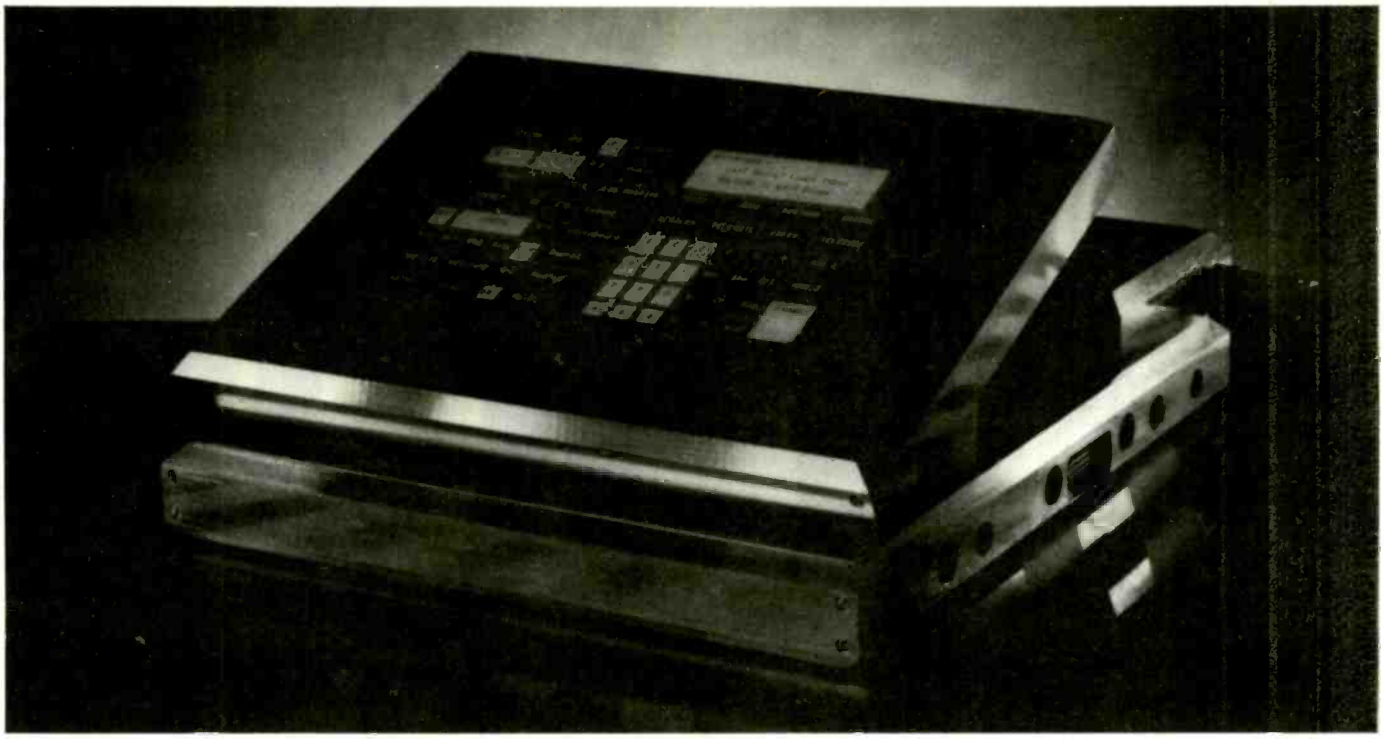
In general, a monitor is engineered to display data at a single fixed frequency. However, new advances have produced a single monitor that can accommodate a variety of scanning (data) rates, which means that the circuit can operate from mulitple sources showing varying resolution. The NEC Multisync is an example of this new type of monitor accommodating frequencies of 15kHz to 35kHz.

QUICK GUIDE

No one display technology will suit every application. The criteria that should influence selection of a display include size, power consumption, legibility, robustness and interfacing.

It is possible to get a more meaningful view of the way in which these factors influence selection by grouping types of displays together by the amount of information they can display.

Low information-content displays Here l.e.ds reign supreme. They are small, robust, with good viewability and are comparatively cheap, so long as the number of l.e.ds used is



Touch-sensitive pads are incorporated into the face of this British electro-luminescent display to provide an interactive system for control and display. The display offers 640 by 256 pixels and has the advantage of a wide viewing angle, suitable for both text and graphics. The 8 by 16 capacitive switches can be programmed to match the corresponding areas of the display by high-level language so that, e.g., a read-out from a required function can be obtained by touching that spot on the screen. By Phosphor Products of Poole.

restricted. Power consumption is acceptable even in portable equipment. Towards the higher end of this category (say four digits and above) l.c.ds start to become more attractive so long as they are to operate in normal lighting conditions. Their low power consumption is a great advantage and as long as l.c.ds are carefully mounted, their robustness is quite good.

Medium information-content displays If we define this category to commence with, say, a single line of sixteen alphanumeric characters, then the choice is between l.c.d. modules and v.f.ds. L.c.d. modules usually have a price advantage and are to be preferred unless the pleasing blue/green characters of a v.f.d. are considered aesthetically more important than the unimpressive black character of the l.c.d. Even with a backlight, an l.c.d. module still consumes less power than a v.f.d, especially if the backlight need only be used intermittently in low-light conditions.

Although plasma displays can also be attractive, their integration with driver and their expense tend to militate against them in this category.

High information-content displays If this category is considered to begin at 4 lines of 40 characters, then the choice here is bewildering. All the displays mentioned qualify.

For smaller units, l.c.d. modules are probably the best choice, up to about eight lines of characters. V.f.d. and p.g.d. units are also available at this size and integration of display and drivers rivals that of the l.c.d. module, albeit at higher cost and greater power consumption. Here if the power consumption and cost penalties are acceptable, the decision to be made is one of aesthetics. Both v.f.d. and p.g.d. are better-looking displays than l.c.ds.

At the top end of this category where an entire screen of information needs to be shown, then the choice is between l.c.d., p.g.d., e.l. and c.r.t types.

The c.r.t. is still the cheapest way to display a large amount of information, so long as the weight and size is acceptable. The neck of a c.r.t. always makes the depth of a unit problematical. Several companies, including Sinclair, Sony and Philips have produced c.r.ts with reduced depth, but costs are high and they show no sign as yet of taking a significant share of the total market.

If a c.r.t. is unacceptable then the choice is between l.c.d. modules, p.g.d. and e.l. L.c.d. modules offer the lowest power consumption, but even the new super-twist units offer an unexceptional display compared with p.g.d. and electroluminescent displays.

For a flat-panel display with good viewability, the choice is between p.g.d. and e.l. P.g.ds have a slight edge on brightness, but are usually larger and heavier than an equivalent e.l. display (this may be important for portable equipment). Interfacing to an e.l. display is usually easier – in many cases c.r.t. controllers may be used.

Unlike the majority of electronic components, the way a display looks has a great influence upons its selection. It is not unknown for the selection of a display to be conditioned by its match to a company's colour scheme. Designers are spoilt for choice as far as displays are concerned – even though some hard work may be necessary to select the correct display for a particular application.

Brian Rose is the product manager of Impectron Ltd of Horsham.

Intended for use in portable computers but also suitable for laboratory instrument applications, this electroluminescent display comes from Finland (Lohja corporation). It has all the electronics necessary to be compatible with the output of an MS-DOS computer.

This flourescent indicator from NEC includes all the support and control electronics to allow the unit to be connected directly to the data and control signals.

Novix — a radical approach to microprocessor design

Currently, programming languages are adapted to suit a given processor, but what happens when the processor is designed to implement the language?

WILLIAM WATSON AND CHRIS STEPHENS

Look at the information accompanying the introduction of a new microprocessor and you will usually find that it describes perhaps a 20% increase in clock speed, faster internal microcode, an extra level of pipelining, or some new addressing mode.

Now consider reading about a processor which outperforms most traditional designs by at least a factor of ten, directly executes a high-level language, and which uses only a modest clock speed. You then read on to find that it is not even a custom-silicon device but put together on a gate array with fewer than 4000 gates and was designed by just two engineers in under a year.

Clearly some kind of explanation is in order. How could such a feat be possible when each new generation of conventional processors normally requires a commitment of millions of dollars and all the resources of a custom-silicon design department? But there is such a device – the Novix NC4000 Forth processor.

Before describing it in detail, we'll discuss recent developments in processor design to let you see why Novix architecture is such a radical departure from the norm, and how its design offers some new concepts to the rest of the microprocessor industry.

CURRENT TRENDS

A decade seems a short time and yet, in the context of the electronics industry, it has seen the development of several generations of microprocessors. Most existing designs originate from two or three major American corporations and more often than not each new processor generation has had a link to the previous one, for example 8080, 8085, 8086, 80286, 80386, and so on. Others show signs of 'creeping featurism' – a d.m.a. controller here, a timer there, some extra i/o somewhere else, all added on to the c.p.u. but not providing an increase in computational performance.

As each new design has evolved, the resulting chip has become increasingly complicated. One way of trying to rationalize this complication while retaining compatibility with existing designs has been to use microcode. Manufacturers started designing a fast processor whose microcode then emulated the required assembler function.

Unfortunately, as design complexity has increased so has the number of microcode cycles needed to implement those complex instructions, so that now a 16MHz clock will yield perhaps two million instructions per second, each instruction requiring eight clock cycles to be loaded, decoded and executed.

As the number of bits of processors has moved up and up from 8 to 16 to 32, the complexity of this microcode has also spiralled. In an attempt to give the user more processing power, designers have been forced to use more and more gates and higher and higher clock frequencies, so that devices with over 100 000 gates and clock speeds greater than 16MHz no longer surprise us.

A recent development has been risc philosophy, where the chip's microcode has been stripped to a minimum. The goal here is to execute a reduced instruction set very quickly, at one instruction per clock cycle if possible. The theory is that the risc processor can execute several small instructions more quickly than one (more complex) instruction on a conventional processor. This technique gains speed but at the expense of requiring more software. It does wonders for a processor's Mips rating (million instruction per second) and shows how misleading such figures can be, as the risc machine is having to execute many more instructions to achieve a given function than its cics (complex instruction set computer) counterpart.

Another method of increasing performance has been to incorporate a pipeline – a facility which prefetches the first instruction while the second is being executed within the processor and the results of the third are being stored. In practice there can be many more than three levels – one recent offering has six.

Like risc, the aim of pipelining is to minimize the processor's time away from memory. But it also presents a problem: in the case of a jump, loop or subroutine call the processor cannot know what the next instruction is until it has executed the current one. In this situation, the processor has to abandon all its pre-fetched instructions and no increase in speed is gained. Some processors manage to juggle the instruction sequence so that at least some useful work is done during otherwise wasted internal clock cycles, but at a penalty of greater processor-design complexity.

Despite these developments, all processors from the slowest to the fastest still present programmers with the same tradeoff: whether to program in assembly language or in a high level language (h.l.l). Assembly language gives maximum performance but at the expense of long development times; employing a high-level language such as C, Pascal, Basic or Forth eases the programming load but at the expense of execution speed, which now depends on the complexity or quality of someone else's compiler. Nor have any of these methods of improving processor performance provided a complete implementation of a high-level language on a processor, for all these languages require assembler code to create the 'virtual machine' for that language on the processor.

THE FORTH VIRTUAL MACHINE

What happens if you turn the problem round the other way? What would be gained by implementing a high-level language like Forth in hardware?

Besides the obvious advantage of simplicity, there are other benefits to such a scheme. Instead of yet another assembler that programmers have to learn and understand, there would be a well documented and popular language that already has an established programmer base. In other words, there would be engineers who already knew how to program such a processor even before it was designed. Furthermore, Forth is a language which is fast in execution – it is widely used in real-time applications – so a specific Forth processor should be very fast indeed. In the longer term, a number of other high-level languages could also be used to program the device because versions of Pascal, C, Basic and Prolog have already been written in Forth.

FORTH IN SILICON

What is needed to produce a Forth processor in hardware? As already mentioned, a Forth implementation is really a Forth virtual machine, Fig.1, synthesized from the architectural and instructions of a given microprocessor. Some of the hardware requirements for the language are:

– A data stack for passing parameters from

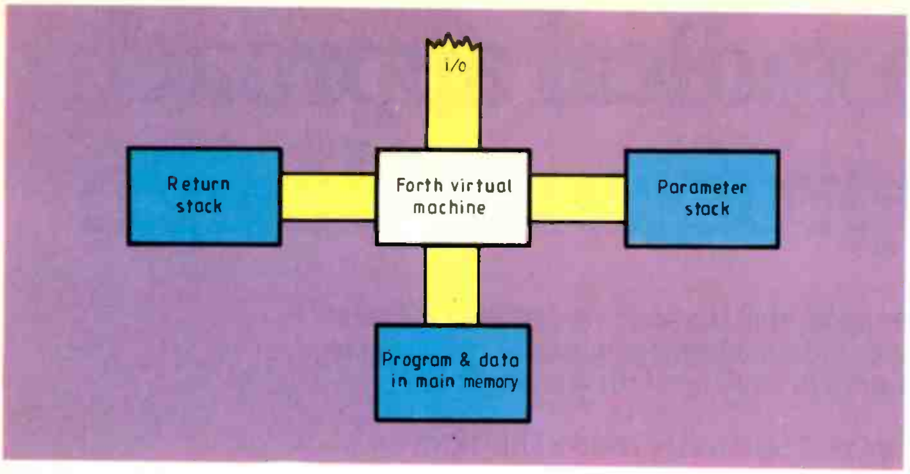
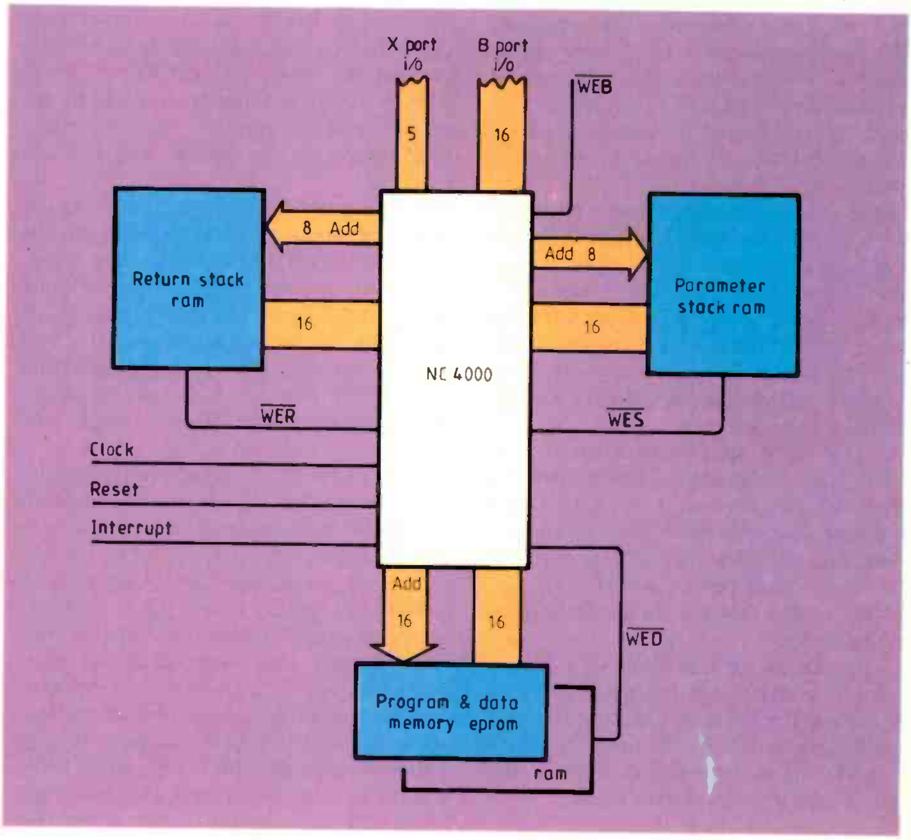


Fig.1 Three principle data storage areas are required by the Forth virtual machine – parameter or data stack, return stack and program/data space in main memory. Forth has specific instructions for fetching and storing data in each of these areas. A further 'bus' in the form of i/o has been added. It's not an essential part of Forth, but is almost always there as part of an application.

Fig.2 NC4000 has four sets of buses, used to implement the three data storage areas of the Forth virtual machine and i/o. Each data bus has data and address lines and a write-enable strobe.



one function to the next. This is quicker and less wasteful of memory than using variables.

- A return stack to give a very fast subroutine return mechanism.
- Memory mapped or bus-based i/o to accommodate Forth's extensive use in i/o intensive applications.

In conventional Forth systems, the stacks are found in main memory. If the i/o is not memory mapped, then an i/o bus usually just means an extra line on the processor indicating i/o data on the memory bus. Thus all the key features of Forth are bottlenecked by the memory bus, and an obvious first step to take in designing a Forth processor is to map these four logical buses (main memory, two stacks and i/o) onto physical ones.

Such an arrangement is shown in Fig.2, which illustrates the various blocks of an NC4000 system. The top two items on the data stack are actually two on-chip registers, T and N, so that a word like SWAP, which swaps over the top two items on the stack, needn't involve any bus activity at all.

In fact the processor could pick up a subroutine return address from the return stack and the next instruction from memory in parallel. With careful design, all four buses can be active in any one clock cycle.

Here is an example of how it could work. The processor reads a 16-bit instruction from memory. This instruction could be to pull data from the 16-bit port into the top register, T; the old value of T is pushed into the next register N, and N is pushed out onto the external parameter stack. At the same time, the processor can execute a subroutine return by popping the contents of the return stack and putting it onto the main address port. This causes the processor to perform the equivalent of a return from subroutine. Each bus has played its part in single machine cycle, moving a piece of data from an i/o port onto the stack and returning from a subroutine call.

What emerges is a processor capable of at least one high-level operation in one clock cycle. The majority of the NC4000 instructions follow this pattern, although some long jump and memory reference instructions (where the code is followed by the address) require two clock cycles.

There are over 40 basic Novix instructions, shown in Table 1. There isn't room here for a full description of Forth, and in any case you can find out about the language from Leo Brodie's excellent book Starting Forth and articles that have already appeared in *Wireless World*. However, the list of Novix basic instructions covers most of the Forth nucleus (subroutine library) which on a conventional system would consist of assembly language code.

I have already described how all four buses can be active in one clock cycle. Combining this with the data paths within the processor, Fig.3, means that many of these Forth primitives can be combined into one 16-bit instruction, and some examples are shown in Table 2.

Microcode is not necessary to achieve all this because the Forth virtual machine is sufficiently simple to allow a direct implementation in logic. This logic is controlled by a number of bit fields within a 16-bit machine instruction, each field representing different operations according to the class of instruction (stack , a.l.u. i/o, memory access, etc).

This scheme requires a layer of instruction-decoding logic but certainly no microcode. In fact, the NC4000 can execute Forth primitive in less time than many architectures execute a single microcode cycle. At the 4000's maximum clock speed of 8MHz each Forth instruction takes 125ns – on the VAX 780 each microcode cycle takes 200ns.

Pipelining is not used in the 4000 for several reasons. The design objective was to produce a simple processor (simplicity equals speed) and implementing a pipeline is complicated. If the processor uses no microcode, there is no need for a pipeline; the processor is going to be accessing memory of each clock cycle anyway.

But a pipeline does not help a highly modular language like Forth. The way in which Forth executes a program means that much of the processor's time is taken up calling functions and returning from them.

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Fig.3 Internal data pathways in the NC4000.Data operations such as arithmetic (+, −,etc), logical (And, OR, Note etc.), or tests (if, zero, >. etc). take place on the top two items of the stack, T and N. Data paths around P, A and I ensure a one cycle subroutine call and a return in parallel with T and N operations if possible. Note how the Forth last-in-first-out stacks are handled automatically by the two stack ports and the J/K stack pointers, requiring no software overhead.

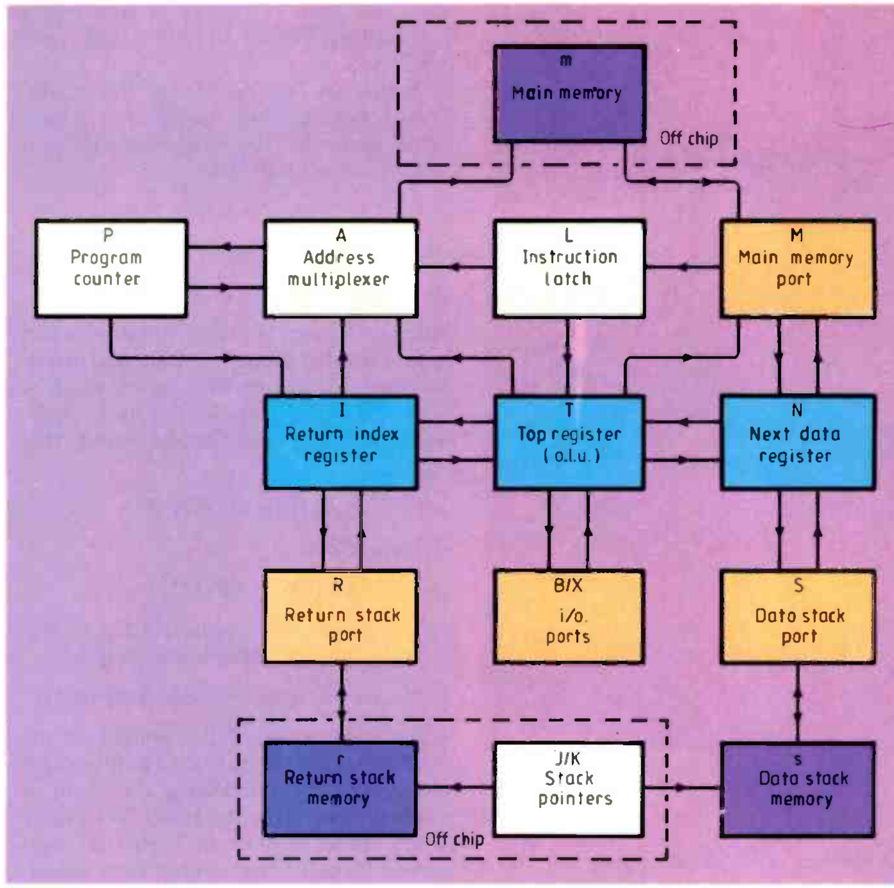


TABLE 2 Instructions corresponding to multiple Forth words

Stack manipulation

SWAP DROP	DROP DUP
SWAP −	SWAP −c
OVER +	OVER +c
OVER −	OVER −c
OVER SWAP −	OVER SWAP −c
OVER OR	OVER XOR
OVER AND	

Shift operations

All stack manipulation operations above followed by 2*, 2/ or 0<.

Return stack

R> DROP

Full literal fetch

n +	n +c
n −	n +c
n SWAP −	n SWAP −c
n OR	n XOR
n AND	

Short literal fetch

nn +	nn +c
nn −	nn −c
nn SWAP −	nn SWAP −c
nn OR	nn XOR
nn AND	

Data fetch (WORD)

@ +	@+c
@ −	@ −c
@ SWAP −	@SWAP −c
@ OR	@XOR
@ AND	

DUP @ SWAP nn + (incrementing fetch)
DUP @ SWAP nn − (decrementing fetch)

Data store (WORD)

DUP !
SWAP OVER ! nn + (incrementing fetch)
SWAP OVER ! nn − (decrementing fetch)

Local data fetch

nn @ +	nn @ +c
nn @ −	nn @ −c
nn @ SWAP −	nn @ SWAP −c
nn @ OR	nn @ XOR
nn @ AND	

Local data store

DUP nn !	DUP nn ! +
DUP nn !	DUP nn ! SWAP −
DUP nn ! OR	DUP nn ! XOR
DUP nn ! AND	

Internal data fetch

nn I@ +	nn I@ −
nn I@ SWAP −	nn I@ SWAP OR
nn I@ XOR	nn I@ AND
DUP nn I@ +	DUP nn I@ −
DUP nn I@ SWAP −	DUP nn I@ OR
DUP nn I@ XOR	DUP nn I@ AND

Internal data store

DUP nn I!	DUP nn I! +
DUP nn I! −	DUP nn I! SWAP −
DUP nn I! OR	DUP nn I! XOR
DUP nn I! AND	nn I!

TABLE 1 Instructions corresponding to single Forth words.

Stack manipulation		
DUP	(n − n n)	Push copy of top stack onto stack
Drop	(n −)	Discard top stack element
OVER	(a b − a b a)	Push copy of second (next) stack element
SWAP	(a b − b a)	Reverse order of top two stack elements
Arithmetic/logic		
+	(a b − sum)	Add top two elements as 16-bit twos complement integers
+c	(a b − sum)	Add with carry
−	(a b − a − b)	Subtract top element from second element as 16-bit twos complement integers
−c	(a b − a − b)	Subtract with carry
OR	(a b − or)	Bit-wise logical Or
AND	(a b − and)	Bit-wise logical And
XOR	(a b − oxr)	Bit-wise logical Xor
2/	(n − n/2)	Arithmetic shift T right one bit
2*	(n − n*2)	Arithmetic shift T left one bit
0<	(n − ?)	Return "true" flag (FFF_{16}) if n is negative, otherwise "false" (zero)
D2/	(d − d/2)	Double-length arithmetic shift right
D2*	(d − d*2)	Double-length arithmetic shift left
*'	(d − d)	Multiply step
*−	(d − d)	Signed multiply step
/'	(d − d)	Divide step
/''.	(d − d)	Last divide step
S'	(d − d)	Square root step
Return-stack control		
R>	(− n)	Pop top of return stack onto data stack
R@	(− n)	Copy top of return stack onto data stack
I	(− n)	Copy loop index onto data stack
>R	(n −)	Push top of data stack onto return stack
Structure control		
if		Jump if T contains zero
else		Jump unconditionally
next		Jump and decrement loop counter if it is non-zero
times	(n −)	Sets repeat-instruction counter
call		Jump to subroutine
EXIT		Return
Memory and i/o access		
@	(adr − n)	Fetch value at memory address (2 cycle)
!	(n adr −)	Store value into memory address (2 cycle)
@	(adr − n)	Fetch value at local memory address (2 cycle)
!	(n adr −)	Store value into local memory address (2 cycle)
I@	(adr − n)	Fetch value from internal register
I!	(n adr −)	Store value into internal register
n (no name)	(− n)	16-bit literal fetch (2 cycle)
n (no name)	(− n)	5-bit literal fetch

This involves either a lot of jumps or subroutine calls and returns, which render the pipeline useless.

Despite this, Forth still performs very well on pipeline micros – it is just that pipelining does not help. In the words of Charles Moore, inventor of Forth and co-designer of the Novix NC4000, "Until recently, Forth competed with other languages on their turf – on computers optimized for them. After waiting 10 years for someone else to, I designed a microprocessor optimized for Forth."

The device itself is implemented on a Mostek 4000D gate array comprising some 16 000 transistors (1/10 that of some of its rivals). This array is a c-mos device mounted on a 121-pin grid array. Benefits of using this technology are low investment (and risk) compared with custom silicon, and second sourcing from other silicon foundries.

In hardware terms, the 4000 is a 16-bit processor with 16-bit addressing in main memory (though the data space can be expanded if needed) and two buses of eight-bit address, 16 bit data for each of the stacks. As Fig.2 shows, each bus is equipped with its own write-enable line.

ONE-BIT OPCODE

So far, I have outlined how Forth primitives work on the NC4000. But in Forth, most of an application consists of one high-level definition (word) calling other, previously defined words. This is the function most likely to be called since one Forth word invokes the high-level definitions from which it is made up, and it needs to be as efficient as possible.

Most conventional Forths use a system of pointers called 'indirect threaded code'. A definition contains a series of addresses which point to either a sequence of assembler instructions (as would be found in a Forth primitive) or to other high level definitions.

Here is an example of how this works. Three actions make up the function GO: FIRST, SECOND, and THIRD. The Forth compiler converts the source statement,

: GO FIRST SECOND THIRD :

into the following memory entries,

(:) (FIRST) (SECOND) (THIRD) (:)

where each term between parentheses is a pointer to other progams. Now a new definition needs to be created to take the result of GO, which has been left on the stack, duplicate it, and then shift it left by one bit. This code is,

: ACTION GO DUP 2* :

which produces

(:) (GO) (DUP) (2*) (:).

Each machine-code routine (e.g. DUP, 2* or ;) could be defined in assembly language as,

(next word) opcode opcode jump next

Where (next word) is the pointer to the machine code. Code produced in this way is very compact but following the chain of pointers costs execution time. To increase speed, some versions of Forth use subroutine threaded code, rather than addresses, to call each high-level definition. The disadvantage is that each call to a high-level function occupies three bytes as against two required by indirect threaded code. Here is the example in subroutine threaded code,

GO becomes
jsr (FIRST)
jsr (SECOND) jsr(THIRD)

rts ACTION becomes
jsr (GO)
jsr (DUP)
jsr (2*)

rts DUP becomes
op code
op code
rts

The 4000's designers took the best of both these principles and produced a subroutine structure with the lowest possible overhead: a subroutine call of one clock cycle, occupying one cell (two bytes) of memory.

The 4000 achieves this by using a single bit instruction – bit 15 reset to zero. When the processor encounters this as code to be executed, it uses the remaining 15 bits as the subroutine address. The chip's instruction sequence places this 15 bit data onto the address bus in time for the next instruction. Although the NC4000 is not a risc machine, this single bit takes the risc philosophy, of making the most used instructions the shortest one, to its ultimate conclusion – a single bit instruction. If bit 15 is one, then the remaining bits are a machine-code instruction.

Here is how the example might look for the NC4000, with the boxed numbers indicating the top bit.

GO becomes
$\boxed{0}$ (FIRST)
$\boxed{0}$ (SECOND)
$\boxed{0}$ (THIRD)
$\boxed{1}$ EXIT

ACTION is
$\boxed{0}$ (GO)
$\boxed{0}$ (DUP)
$\boxed{0}$ (2*)
$\boxed{1}$ EXIT

DUP, a machine primitive, is
$\boxed{1}$ DUP
$\boxed{1}$ EXIT

A secondary advantage of subroutine threaded code is that in-line machine code can be included between high-level definitions. Words DUP and 2* happen to be Novix code primitives so the code for ACTION becomes,

$\boxed{0}$ (GO)
$\boxed{1}$ DUP
$\boxed{1}$ 2*
$\boxed{1}$ EXIT

Execution time is the time for GO plus one for each word. Remembering that the mutliple buses of the Novix allow the stack (DUP) the a.l.u. (2*) and the return stack (EXIT) to operate in parallel. The last three instructions can be combined by an optimizing compiler to give,

$\boxed{0}$ (GO)
$\boxed{1}$ (DUP and 2* and EXIT)

TABLE 3. Benchmark give some comparisons with other processors.

1,000,000 empty loops			
Intel 802826	(10MHz 0 w.s.)	'C'	5.0s
8088 (IBM-PC)		Assembler	3.8s
68000	(8MHz 1 w.s.)	Assembler (DBRA)	2.3s
NC4000P	(6MHz)	NovixForth FOR...NEXT	0.17s
Eratosthenes sieve (10 iterations)			
Intel 802826/310	(10MHz 0 w.s.)	'C'	6.6s
68000	(8MHz)	Assembler	4.9s
VAX 780		'C'	1.4s
NC4000P	(6MHz)	NovixForth	0.85s
NC4000P	(6MHz)	NovixForth (optimized)	0.45s
IBM 3033		PL/1	0.36s

Execution time is now the time for co plus one cycle. This illustrates how the call overhead is usually only one clock cycle, and is certainly never more than two.

By way of comparison, Intel's 80186 requires 19 clock cycles to make a subroutine call, and a further eight for the return for a total of 27. At 8MHz this is 3.375μs, so that the fastest that you can execute an empty subroutine is 300kHz – a far cry from 4MHz achieved by the 4000, for the same clock frequency.

The obvious tradeoff for this single-bit subroutine scheme is that program address space is limited to 15 bits, or 32K words (64K bytes). However, given the inherent compactness and power of the instruction set and the possible parallelism of compiled code, this restriction is not as limiting as it might first appear, and 64K-byte can contain much more code than an equivalent traditional system.

PERFORMANCE

Executing a high-level language at an average of 1.2 instructions per clock cycle gives rise to some surprising performance figures when actually running a program. Table 3 shows some benchmark timings.

A good rule of thumb for the NC4000 is that it is consistently 12 times faster than the 68000 programmed in assembly language for the same clock speed. From the software engineer's point of view, there is now the luxury of being able to program in a high-level environment with all the advantages of Forth's interactiveness, and still produce code which is an order of magnitude faster than programs in assembly language.

As can be seen from Table 1, some of the arithmetic on the NC4000 works in one clock cycle. For multiply and divide, the device has step primitives. At 8MHz, a 16-by-16 multiplication takes 3.5μs, and a 16-by-16 division between 4 and 6μs. Charles Moore saw potential applications for the NC4000 as a graphics processor, and included a square root function; the NC4000 calculates the square root of a 31-bit number in just over 3μs.

With no on-chip multiplication hardware, the NC4000 does not match digital signal processing chips when executing multiplication-intensive software such as a butterfly algorithm as part of an FFT. However, for general purpose number crunching it comes out very well; for floating point arithmetic it has roughly the same throughput as Intel's 8087 floating point co-processor.

Having i/o directly coupled to the NC4000 gives it the potential of handling high i/o bandwidth. For example, the device can read data in from the B port onto the parameter stack at 16 bits per clock cycle, or 16M-byte/s at 8MHz. If port B was connected to a 16-bit serial-to-parallel shift register, the bit stream input frequency could be 128MHz.

Obviously there is a limit to how much data can be dumped onto the stack. For large quantities of data a high-level loop is required to read a value in from the port and store it incrementally in memory. Such a loop looks something like

Charles Moore, Forth and Novix

It is a singular achievement to invent a new language and design a processor to execute it. Charles Moore's work in providing software for controlling astronomical telescopes, and his goal of an interactive interface with the hardware he was controlling led him first to develop an interpreter (1958), then a compiler for threaded code (1968) and finally an interactive compiler.

The result was Forth, but the language remained confined to the astronomy world until 1973 when Moore and some colleagues left Kitt Peak Observatory and set up Forth Inc to explore Forth's commercial potential. Forth became more generally known from 1978 onwards with the formation of the Forth Interest Group (FIG).

For a while Moore was content to exploit the language commercially, hoping others would incorporate aspects of the Forth architecture into a processor. But although Forth had established a sizable following in the microcomputer user comminity, processor manufacturers did not accept Forth as the basis of an architecture for hardware design and implementation, even though some went as far as putting Forth 'on chip' in the form of a rom (for example Rockwell's 65F11). Some sporadic efforts were made to design a Forth processor, in bit-slice technology and in random logic, but of no lasting consequence.

Around 1980 Charles Moore started to work on his ideas for a design, putting together e.c.l. prototypes to see what logic was needed, resulting in a Forth engine simulator in March 1983. In 1984 the Novix consortium put the necessary funding in place for implementing a real device and just one year later the first working chip was delivered. It was a gate array made for Novix by Mostek, and ran at 8MHz. The design team had a Forth-like simplicity: Charles Moore and Bob Murphy, an expert in gate arrays. There was a delay due to Thompson CSF's takeover of Mostek in December 1985, but the NC4000 became generally available around May 1986.

... FOR Bport 1@ SWAP 1!+ NEXT ...
Execution time =
1 cycle + 1 cycle + 1 cycle

FOUR BUSES AND 121 PINS

At first sight, hardware aspects of the NC4000 seem rather daunting. Here is a chip with formidable performance and rather a lot of pins. However, all that has happened is that it has four times as many buses as a conventional processor, and that each bus is actually very simple to understand. In fact, the NC4000 cannot afford to have a complex bus structure, for such complexity imposes time on any given clock cycle, time that can be ill afforded if the ultimate design goal is speed.

That pursuit of speed has also influenced the Novix design team to choose a gate array with on-chip high-speed c-mos drivers, so that external address and data buffers are not usually needed. Ironically, bus drivers are used on Novix's own development system, the Beta Board, but only in a sacrificial capacity. It is a lot easier (and cheaper) to replace some 74HC245s than a Novix chip if something disastrous happens on your prototype hardware. Most existing Novix system designers have used standard high-speed c-mos for decoding parts. These are fast enough and are compatible with the NC4000's c-mos input and output voltage levels.

The x port was originally conceived for use in memory expansion but it can be used in a variety of other ways to reduce the hardware count, and keep decode timing delays to a minimum. Using 'off-the-shelf' parts, it is possible to put together a 5 Mips board with a component count barely in double figures.

Apart from its high pin count, the NC4000, has some other unusual hardware aspects. The chip is entirely static, and its internal operations are triggered by the rising edge of the clock. The processor takes about 65ns for all its internal operations to complete, and new address and data signals are presented at the chip pins as they get generated internally; they are not synchronized with the falling edge of the input clock.

FUTURE DEVELOPMENTS

The 4000 has been available in a prototype version for about eight months, and a number of products have already emerged which take advantage of its speed. An early success was the Calay automatic p.c.b. layout routing accelerator.

This product illustrates the commercial advantages of Novix architecture. The project started as a bit-slice design, involving a sizeable team not only designing the hardware but also having to grapple with horizontal microcode. However two engineers found that the 4000 would give them higher performance than the bit-slice original, and with a shorter development cycle.

Most of the first products to appear are general purpose single-board computers, including products for the IBM PC bus and VME. As one might expect from a processor with this kind of performance, it has been taken up for research in areas such as artificial intelligence, signal processing, and robotics. Some designers have homed in on its i/o capabilities and are using the device as a super fast i/o controller.

Novix has moved onto the next version of the device, the NC6000, which has more functions and higher clock speeds (10MHz). Two versions are planned, one an NC4000P pin-compatible version and the other a new 144-pin device with expanded i/o facilities, including the ability to construct multiprocessor systems. A 32-bit version is also a possibility.

Given the parallel nature of the existing device, it is likely that such a processor could achieve some very impressive code compression, and one might expect 20 Mip performance as well as the usual benefits of higher-accuracy arithmetic and unrestricted memory addressing.

Novix technology is in its infancy, and yet it already outperforms most conventional processors. The possibilities offered both by higher bus widths and by moving the design onto custom silicon must excite even the most conservative engineer.

William Watson and Chris Stephens are with Computer Solutions of Byfleet.

Parameters

The black-box approach to network analysis

JOULES WATT

"Do you still design a lot of transistor circuits?" enquired the young man. He was a new trainee in the workshop and he went on to say that he thought there was an i.c. to do everything these days.

After some consideration, everyone realised that a large amount of discrete-component circuit design still takes place. "Beside," we asked, "who designs the circuits on the chips of the i.cs?"

"Are you saying it is still necessary to know about those transistor constants that I've come across – the 'h' something or another?" "Ah, you mean the parameters. Of course it is, not only the h parameters, but the z, the y, the A, B, C, D, the g, – and those called scattering parameters. *Wireless World* has had articles discussing some of these in the past[1,2].

One fact that quickly arises when discussions start about this subject, is that the h, z or any of the others are not constants, but are true parameters. *Para-meter,* literally "beside-measure", is usually taken to mean 'constant for this example, but variable in general'. This shows that it is an error to ask, "what is *the* h_{fe} of a BC109?" Not only are there wide manufacturers' spreads in such devices, but of more fundamental importance, the designer can often choose parameter values by positioning the Q, or operating point, which is done by designing the bias arrangements to sit the transistor at the chosen values. The parameters are also strong functions of the frequency – their phases and amplitudes vary over the band. Therefore, if measured or known only at one frequency, they cannot be used to calculate performance over a wide bandwidth.

Wide application. Another small fallacy is to assume that the parameters apply only to transistors. The h parameters are so common in makers' literature because of the relative ease of measurement and the standardization that has become implicit. A glance at i.c. makers' data shows similar use of parameters to characterize some linear devices. For example, Plessey's SL series of i.c. amplifiers are offered complete with g parameters, as in Fig.1.

The use of parameters is not limited only to active devices, either. Filters, transmission networks, and whole systems are characterized by them because of the generality of the approach. Power engineers employed the A, B, C, D chain parameters for cascaded networks in solving problems, at least back to the 1920s. Guillemin offered a discussion which became the standard for subsequent work. He included the use of matrices. But this was in 1935![3,4]

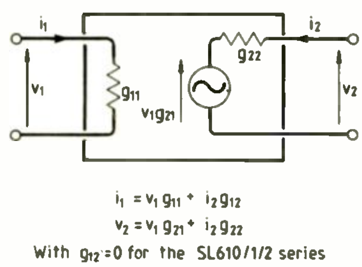
THE BLACK BOX

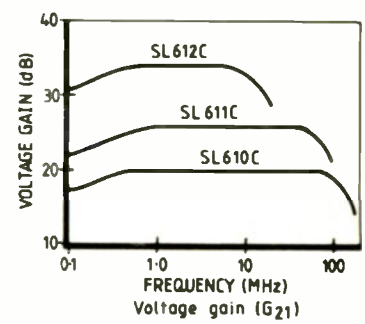
When introducing studies on this subject, lecturers usually say, "We come now to the 'black box' equivalent circuit. You don't need to know anything about what is in the box..." and they mean that a two-port, or four-terminal block is about to be discussed.

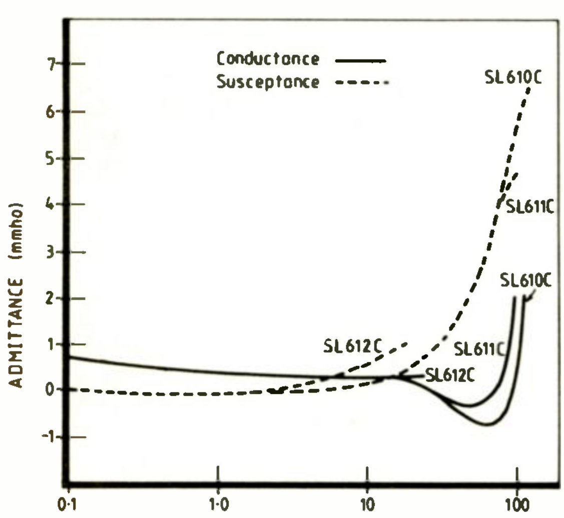
Such a circuit block or stage is a transmission network, in the sense that it has a pair of input terminals or – another way of saying it – an input port; together with an output port, as shown in Fig.2. The only accessible quantities are the input voltage and current, V_1, I_1 and the output voltage and current, V_2, I_2. These four quantities are written in capitals to indicate that they represent d.c. or r.m.s. values. Any two of them can be varied and the other two measured to see the effect. The functional relationship linking the variables to give the effect is set by the form of the contents of the 'black box'.

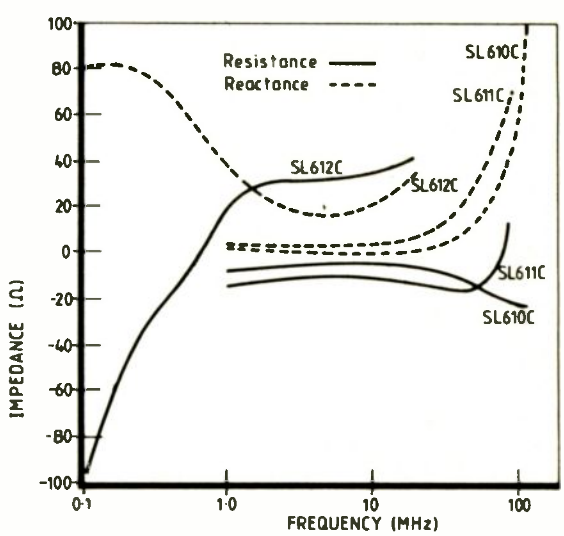
The particular two from V_1, I_1, V_2, I_2 we choose to vary first become the independent

Fig.1. The g parameters are useful for modelling a *voltage amplifier,* where $Z_L >> g_{22}$ and $Z_s << g_{11}$. g_{21} is the *voltage gain* under these conditions. The g parameters vary with frequency and possess real and imaginary components. For the SL610 series, the makers publish data on a log-log plot showing how these real and imaginary parts vary with the frequency. (Acknowledgements to Plessey.)









variables: the other two automatically become the dependent variables. Ringing the changes on these four yield all the various parameters possible – except the special case of 's', the scattering parameters, which do not directly employ V_1, I_1 etc. but the intensities of waves on transmission lines.

Taking two things from four gives six possibilities. The first question arising is how to decide which pair to choose. As an example, choose I_1 and I_2 as the independent variables, according to,

$$\begin{aligned} V_1 &= f_1(I_1, I_2) \\ V_2 &= f_2(I_1, I_2) \end{aligned} \qquad (1)$$

Simply writing this has not answered the question fully. Before doing so, let us ask another.

The second question arising is to do with *linearity*. All the 'black-box' approaches assume a linear circuit, i.e. no distortion. This means that the various signals and variations can be simply added with no interactions*. Such an assumption is a tall order for real active devices such as transistors, but is approximately true for small signals. The approach is sometimes called the small-signal analysis.

The next step, therefore, is to vary the steady quantities in equations (1) by a sufficiently small amount to maintain linearity. This is equivalent to expanding equations (1) using Taylor's Theorem – and retaining only the linear terms. What amounts to the same thing is to proceed directly by adding the partial contributions made by both independent variables. Because of the linearity, there is no interaction and the result is simply the sum.

$$\delta v_1 = \frac{\partial V_1}{\partial I_1}\delta i_1 + \frac{\partial V_1}{\partial I_2}\delta i_2$$

and

$$\delta v_2 = \frac{\partial V_2}{\partial I_1}\delta i_1 + \frac{\partial V_2}{\partial I_2}\delta i_2 \qquad (2a)$$

These are read as, "the total change in V_1 is how fast V_1 changes with I_1, times the actual small change in I_1; plus how fast V_1 changes with I_2, times the actual small change in I_2". Similar reasoning is used for all the others. Writing V_1 etc., is ugly and lower case letters have become standard for changing quantities.

Therefore,

$$\begin{aligned} v_1 &= \frac{\partial V_1}{\partial I_1} i_1 + \frac{\partial V_1}{\partial I_2} i_2 \\ v_2 &= \frac{\partial V_2}{\partial I_1} i_1 + \frac{\partial V_2}{\partial I_2} i_2 \end{aligned} \qquad (2b)$$

The parameters are simply the partial differential coefficients and you can see there are four of them. In this example, the coefficients are voltages divided by currents in every instance and, by Ohm's Law, this means their dimensions are ohms. By this choice, we have derived the impedance, or 'z' parameters. Equations (2b) can be written,

$$\begin{aligned} V_1 &= z_{11} i_1 + z_{12} i_2 \\ V_2 &= z_{21} i_1 + z_{22} i_2 \end{aligned} \qquad (2c)$$

Or if you want to give an air of authority, you can call them the 'matrix parameters' and write the 'Z matrix' by putting (2c) into matrix form,

*This is known as the 'Law of Superposition'.

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \qquad (2d)$$

This would at least show you have studied a little 'modern maths' (but note Guillemin[3]).

THE FAMILIAR 'h'

Deriving any other set from the six possibilities is just as simple and any text book will show them all[5,6]. I will simply quote the h parameter set as the most important bipolar transistor characterization,

$$\begin{aligned} v_1 &= h_{11} i_1 + h_{12} v_2 \\ i_2 &= h_{21} i_1 + h_{22} v_2 \end{aligned} \qquad (3)$$

One point arising is that you might look at equations (2c) and (3) and think z_{11} is equal to h_{11}, thus calling them 'the input impedance' at port 1. They are input impedances at port 1, but are far from *the* input impedance. There are many input impedances, according to how you define them. z_{11} is the rate v_1/i_1 only if $i_2=0$ (as seen from the first of equations (2c), that is, only if the output terminals are open circuited. h_{11} is v_1/i_1 only if $v_2=0$. In other words, only if a short circuit is applied across the output terminals. So z_{11} and h_{11} are measured under entirely different conditions. The only time h_{11} becomes equal to z_{11} is if $h_{12}=z_{12}=0$, in other words, if the network in the box is 100% unilateral – nothing going on at the output can feed back to affect the input. Things are not always quite so simple. If you look closely at y_{11} in the admittance parameter set, then it does look as though this is equal to $1/h_{11}$ in the hybrid set. Therefore the parameters are not all independent.

There are a vast number of parameters, because other than the six basic possibilities, a transistor can be connected into the common emitter, common base or common collector arrangement. In each two-port example there are four parameters, so altogether there are $6\times3\times4=72$ possibilities for individual parameters. Obviously, the skill in using them comes into choosing the appropriate set for your job in hand. The parameters are not all independent of course, and academics like to give their students long exercises or large tables showing all the conversions of "h into z, y_{fe} into y_{fb}" and so on.

WHAT DO THEY MEASURE; WHAT DO THEY MEAN?

It is interesting to look at the physical meaning of, for example, equations (3). Because the values have emerged only by measurements at the terminals, the situation is similar to Thévenin's or Norton's Theorems as applied to two-terminal networks. The first equation in (3) shows that v_1 is the sum of two internal voltages in the box. The second equation shows i_2 is the sum of two currents. The internal equivalent circuit for the input and output ports of the box can now be drawn, as shown in Fig.3. This shows why the parameters are called 'hybrid' or h for this example. The input is a Thévenin equivalent, while the output circuit is a Norton equivalent. Also h_{11} is an impedance, but h_{22} is an admittance.

What might be a new idea to some people is highlighted by this black-box model – the idea of a controlled generator. The current generator at the output is controlled by i_1, which is a current in a separate circuit. h_{12} is the 'strength' of the generator, as it were. The voltage generator at the input is controlled by v_2 in a similar transfer across. It could be said to have a 'strength' h_{21}. h_{12} and h_{21} are transfer quantities, linking the input and output. h_{11} and h_{22} are terminal quantities (sometimes called 'driving point' quantities).

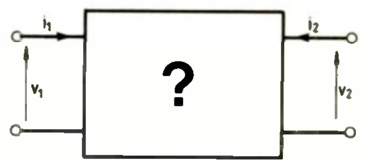


Fig.2. The "black box" already appeared in Fig.1. (with appropriate contents...). In general, what is in the box is a mystery. As the terminal voltages and currents are the only ones we can measure, all the various ways in which these quantities can be related give rise to a different interpretation of what is inside.

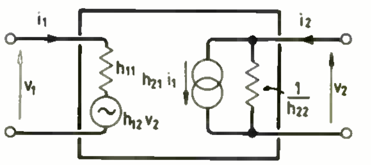


Fig.3. Shown here is what has become the most general parameter description of a bipolar transistor. h_{22} is often very small in relation to circuit values and is then neglected. The same applies to h_{21}, because in modern transistors, the internal feedback (which this parameter describes) is extremely small.

As a historical fact, the idea of controlled generators is not new. For decades, thermionic valves were modelled as voltage-controlled voltage generators (for triodes) or as voltage-controlled current generators (pentodes) in their equivalent circuits.

For circuit engineering purposes, the parameter subscript notation is changed a little. This makes it more 'user-friendly', to use some modern jargon. In the case of a common-emitter transistor amplifier circuit, h_{11} is an input terminal parameter (an input impedance) and is written h_{ie}, i for 'input' and e for 'emitter common'. Similarly h_{12} is written h_{fe} because it is a forward transfer parameter (current gain), h_{21} is h_{re}, a reverse transfer parameter (the feedback voltage ratio), and h_{22} is written h_{oe} as it is an output terminal parameter (an output admittance). The various parameters are real quantities at low frequencies, but you must be prepared to work with complex numbers at h.f.

They are all useful at times One may question the need to keep so many of the possible parameters, when say, the h parameters might work for all eventualities. The various systems of parameters do have individual advantages, which you can see when the matrix representation is written down.

continued on page 224

STE bus as an i/o bus in VME systems

Recent trends in standard bus specifications provide the means to quickly integrate multiple bus systems using off-the-shelf board-level hardware. Here's how to couple VME and STE buses together, the ensuing system architecture and the role that each bus plays.

TIM ELLSMORE

As system architectures built around VME bus become the increasingly popular choice for speedy integration of high performance microcomputer systems, the problems faced by the system integrator shift in emphasis. This is largely because many fundamental design features of a system become automatically established when the decision to use VME bus is made, and previously less significant problems move forward into the limelight.

How to include a variety of system interface options without significantly increasing system cost, how to avoid becoming bound, and how to optimise cost and performance using standard products, are just three problems. Many integrators of VME bus systems, dismayed by the cost of pure VME solutions, are beginning to turn to multiple bus architectures to help solve these problems. STE bus is emerging as the most logical contender for a secondary i/o bus.

TRADITION vs ELEGANCE

The traditional industrial microcomputer is a single bus system in which a single microprocessor performs all of the processing tasks. It utilizes the system bus as an execution bus as well as a data transfer bus for transfer of input and output data to and from interface boards. The system bus effectively serves as an extension of the microprocessor local bus.

The majority of VME bus boards assume this type of architecture, which tends to force the system integrator toward a system more closed than may be desirable. An unwary designer can all too soon be locked into a system architecture dictated by the chosen board vendor. Many vendors of

COUPLING VME TO STE

STE bus provides system-level enhancements in cost, performance and versatility when used as an independent i/o bus in VME bus systems. It can be coupled with VME systems by a pure hardware protocol conversion, by intelligent hardware with an associated software protocol, or by use of a local area network. The cost-to-performance ratio of a system achieveable by use of this technique is system-dependent, but generally exceeds that achieved by alternate methods. This short system development time – and therefore time to market – associated with standard buses is further improved due to the ease with which custom STE bus boards can be developed.

The concept of STE bus as an i/o bus is not limited to VME bus and is likely to become a logical contender for providing i/o in Multibus II systems as it has a more convenient form factor than iSBx modules. It is also likely to be used in systems built around Futurebus; the IEEE Microprocessor Standards Committee view all three buses as an hierarchically compatible family.

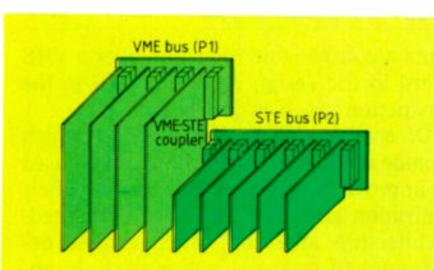


Fig. 1. There are a number of methods that a system integrator can apply to add an STE sub-system into a VME system. The method deemed most appropriate for any given system will depend upon the application. Figure 1 demonstrates a method for combining the two buses within the same sub-rack. Most VME boards are double height (233.35mm), standard depth (160mm) Eurocard size and most STE bus boards are single height (100mm), standard depth (160mm).

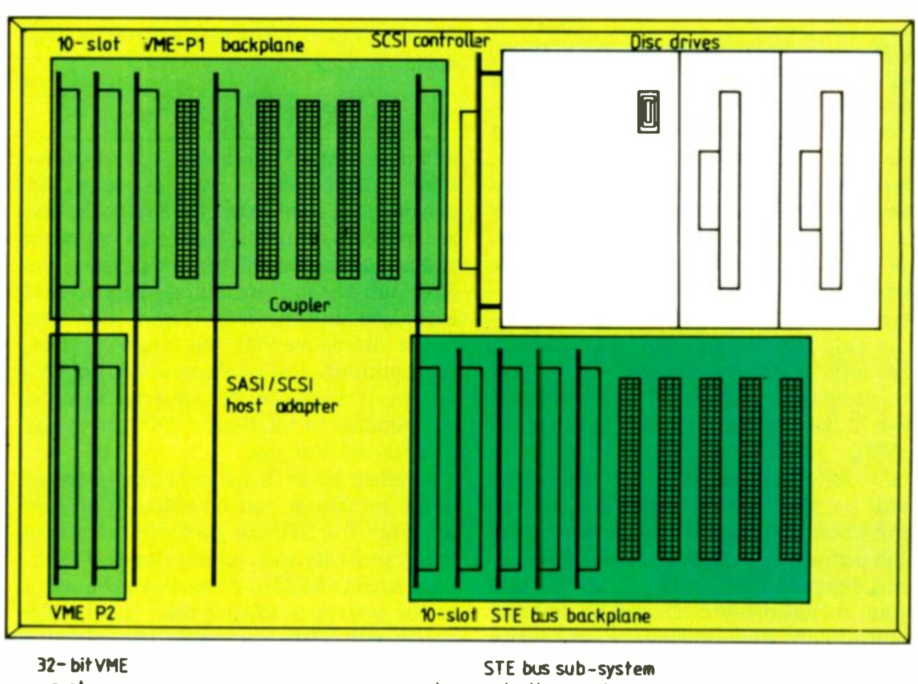


Fig.2. High performance industrial microcomputer using sub systems: the system controller is a 32-bit VME c.p.u. board (e.g. 68020) closely coupled to an expansion memory board via the VME bus P1 and P2 connectors (P2 carries the VME 32-bit extension signals). The disc sub-system comprises an intelligent VME-compatible small computer system interface adaptor coupled to a 5.25in footprint-compatible disc controller board mounted on the hard-disc drive. Communication with terminals and other peripheral interfaces such as GPIB is via an independent STE sub-system.

board-level VME bus products have followed the lead of the pioneering VME manufacturers in providing products that support only traditional industrial system architecture.

Novel, unique and elegant system architecture is often difficult and expensive to devise when using traditional standard VME-compatible products. It is disturbing that these products tend to lock the user to a particular performance level far below the real potential of VME bus systems.

WHY A BYTE-WIDE SECONDARY BUS?

Due largely to a number of established standards, most notably ascii data interchanged between systems and peripherals is almost universally byte organised. Most interfaces implemented to industrial computer systems are byte organized: Shugart Associates System Interface, Small Computer Systems Interface, IEEE488 General Purpose Interface Bus and asynchronous RS232C communication. Data is almost exclusively transferred to and from storage media in byte format.

This being so, data moving between the CPUs and the various i/o devices is necessarily transferred a byte at a time. This is wasteful of a wider-path bus bandwidth (number of bytes that can be transferred per second). In a 32-bit VME system, for example, 75% of the bus bandwidth is wasted each time an i/o byte is transferred over the bus. In an i/o-intensive system such as a multi-user microcomputer this could translate into a significant performance overhead.

Another advantage of byte-wide buses is that there is no need to consider the anomaly of byte justification that causes processor compatibility problems with wider-path buses. There is therefore no requirement for byte swapping logic which can represent a cost penalty. There is also, of course, a reduction in the number of data transceiver components and, therefore, control elements, required in the bus interface – another cost-saving feature.

WHY STE BUS?

In December 1982, when the IEEE P1000 working group first began to piece together the requirements and objectives of STE bus, it became clear that it could be an ideal intelligent i/o channel for VME bus systems. The main reason for this was a high degree of compatibility between the non-performance requirements of both buses. For example, the IEC mechanical specification and the associated DIN 41612 connector were considered essential for STE bus, and asynchronous data transfer protocol was chosen as the only effective means to achieve processor-type and speed independence. Both of these features are also fundamental to VME.

Carefully implemented, the hooks provided for compatibility with VME bus systems would not compromise the potential of high performance eight-bit stand-alone systems designed around STE. So the working group included more features to improve compatibility, such as using the same power supply voltages and power-fail signalling as VME bus, identical system utilities (system clock and system reset) and defining only the outer two rows of the connector leaving the centre row free for VME bus 32-bit expansion signals.

An unstated objective of the working group was to provide both physical and conceptual upward migration paths from STE to VME bus, to allow system designers to easily maintain their investment in STE bus when developing more powerful, next-generation systems. By use of some mechanism to couple one or more STE sub-systems into a VME bus system, existing STE-compatible boards can be used and, if the coupling mechanism includes intelligence, all existing software for the STE bus boards can be utilized. The implication is that a large portion of an existing system can be literally grafted into a next generation product.

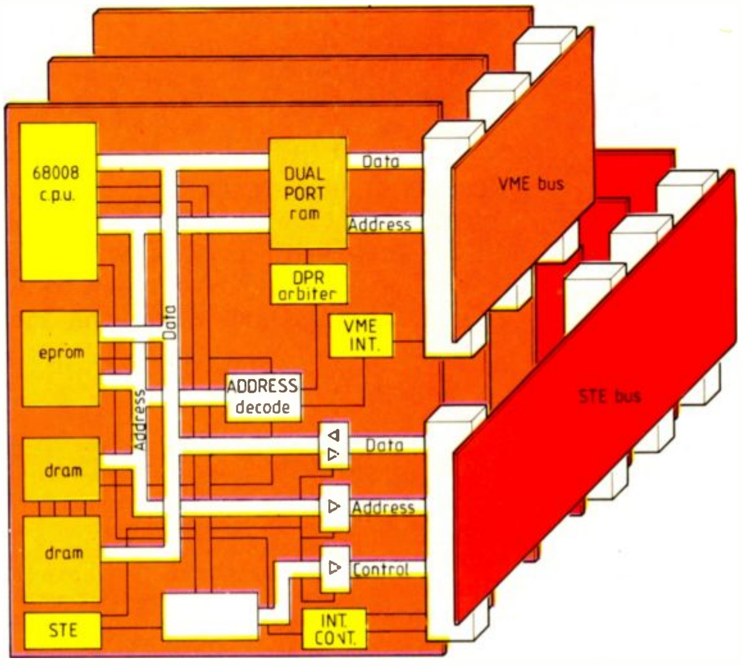


Fig.3. In this intelligent bus coupler, the c.p.u. is a 68008 which is code-compatible with other 68000-family c.p.us, the on-board ram is 512K bytes and provision for firmware is up to 64K bytes. Communication between the VME masters and the on-board c.p.u. is via a 64K byte dual-port ram window. This is separate from the 512K byte ram area in order to provide a high degree of protection for data buffers being assembled and formatted in the main ram area. Indivisible read-modify-write mechanisms can be employed through the dual-port ram to pass semaphores between the VME system and the STE sub-system, allowing further protection as buffers or programs are transferred to the dual-port ram.

COST ADVANTAGE

Adding a coupler into a VME system represents a cost penalty in itself, of course, but generally the coupler and the STE backplane are low-cost elements. Before an optimum system can be established, the cost of the STE sub-system, including coupler and backplane, must be weighed against the cost of the alternative VME bus boards. In fact, the optimum cost/performance ratio of a system is likely to be achieved using a combination of intelligent VME slaves and STE bus sub-systems.

Another factor that should be considered is the minimum cost of adding a new i/o function. The STE bus card size is small so the granularity with which standard functions such as RS232C channels can be added to the system is smaller than is generally found with VME bus cards. The STE bus interface is simple to implement and requires only a few components. This represents a considerable reduction over a VME board in the design cycle time and in the production cost of custom boards.

Of course VME i/o boards exist which include intelligence, and these can be used to improve system performance, but their utilization embodies an essentially closed-architecture approach which can be detrimental to product development. In applications where there is a high degree of confidence that the planned hardware environment will not evolve further, these intelligent slave boards may be a fairly cost-effective approach. But many of these applications can be much more effectively catered for with a single board solution.

DISTRIBUTED ARCHITECTURE

Despite the lack of support from traditional VME board manufacturers, a new wave of more open and flexible system architectures is becoming evident in industrial systems. The ever-declining cost of microprocessors and memory devices has prompted a number of VME system integrators to devise architectures which make use of a loosely coupled distribution of intelligence. In this type of architecture each discrete i/o or data processing task is performed by a dedicated microprocessor. A single processor is designated as the system master and operates at the highest virtual level, overseeing and controlling the dedicated processors by use of a command-level protocol transmitted over the VME bus.

The system integrator's choice of VME as the main system bus is possibly the most significant factor that makes these elegant architectures cost-effective. VME bus was designed to allow modular construction of medium-to-high performance industrial computer systems. The versatility and underlying open-architecture characteristics of the bus theoretically permit VME-based microprocessor systems to be employed for nearly every conceivable type of industrial application and to yield cost-effective, modular, systematic and structured architectures.

Another aid to the integrator in targeting a distributed intelligence system is the introduction of self-contained intelligent VME bus sub-systems for controlling disc and terminal i/o. But the most significant contribution to maintaining an efficient and low-cost open architecture is the implementation of open sub-systems using a high performance byte-organised i/o bus such as STE.

MULTIPLE MASTERS vs INTELLIGENT SLAVES

VME bus provides arbitration facilities which allow a number of execution units (c.p.u. boards) to share the system bus. This allows dynamic distribution of processing tasks among multiple processors which collectively provide a quasi-parallel processing environment. However, the addition of each new processor in this type of architecture yields only a percentage performance increase. The throughput improvement diminishes with the number of processors as the system bus becomes the overriding bottleneck in the system.

This implies that the number of bus masters in a VME system should be limited and that all intelligent elements should minimize or eradicate the need to transfer data over the bus. Some new high performance c.p.u. boards are becoming available that incorporate a wide private memory bus to optimize program execution speed. Some make use of the VMX memory expansion bus, but the more popular approach is to define a proprietary execution bus.

In fact the optimum performance of a system in any given application may be realized by employing a combination of distributed intelligence and multiple masters – Fig.2.

SECONDARY BUS FUNCTIONS

There are two reasons why a system integrator may choose to use a secondary bus for i/o within a VME system. First, to provide a significant performance advantage at an optimum cost, and second to make use of a wide range of interface functions.

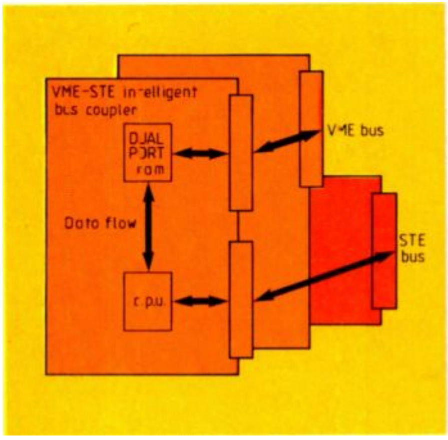


Fig.4. VME masters communicate with the dual-port ram in 16-bit transfers and, as an additional feature, the coupler has the capability of signaling interrupts on the VME bus and responding to an interrupt acknowledge with either a byte or a word-with vector. It includes an STE bus interrupt controller capable of both explicit (vectored) and implicit (non-vectored) response to interrupts from STE slaves.

The performance advantage stems from the partitioning and distribution of processing responsibility within a system – the burden of processing i/o can be off-loaded from the main system processor. Data flow between a system and external device is often slow and usually incurs a significant interrupt servicing overhead; an intelligent sub-system running a realtime executive, separate from the rest of the system, can more efficiently organize data input to the system into pages of packets before interrupting the flow of the main processor. Similarly, large packets of data can be handed to the i/o sub-system from the main processor for orderly output.

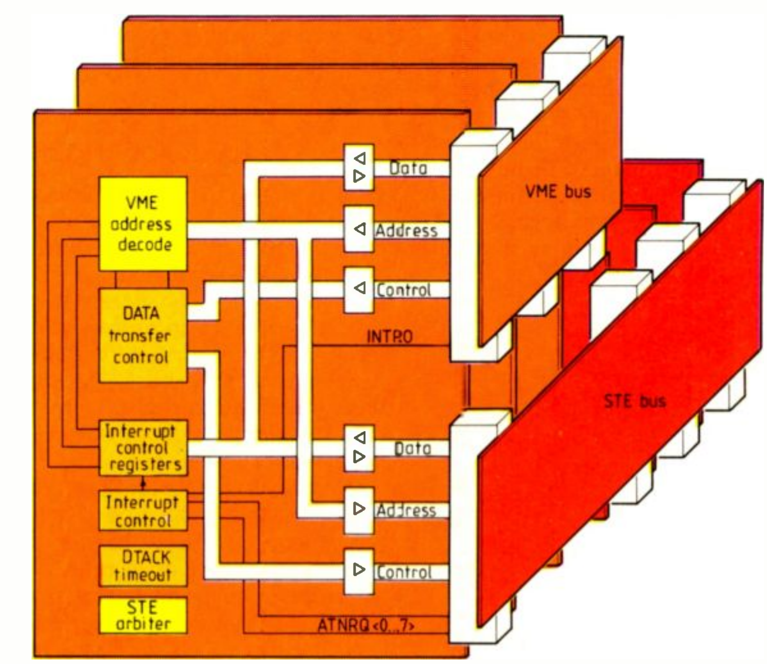
Simple examples of this type of i/o handling are printer queuing and spooling, disc file management, communications front-end processing, network management etc.

Two intelligent STE bus sub-systems can be incorporated for example one dedicated to communications and the other to a complete disc control sub-system which effectively replaces the SCSI host adapter and disc controller in Fig.2. It also provides some spare slots for the addition of other STE compatible peripheral interfaces.

Partitioning i/o handling in this way can dramatically improve system throughput and, as an additional bonus, the STE bus sub-system can be developed independently, and tested remotely, from the main system.

Many functions are available as STE-compatible products that are not directly available as VME compatible products. This may be because they are only provided as part of an ensemble of other functions on a VME-compatible single-board computer of a multi-function board, or because the market requirement for a given function is simply too low to warrant the development investment required for a VME product. In many of these cases a VME-to-STE coupler can be used merely to allow connection of an

Fig.5. This protocol converter differs significantly from the intelligent coupler in that it provides a transparent medium through which the VME masters can access STE slaves. At first sight this appears more efficient than using the intelligent coupler, but data transfers are confined to a byte at a time.



STE-compatible function in to a VME system regardless of any performance requirements.

INTELLIGENT VME-STE COUPLER

In an i/o intensive environment, where the performance of the main system processors is degraded by i/o handling overhead, it is necessary for the STE bus sub-system to include some intelligence. In these cases the bus coupler itself should include a c.p.u., firmware, and a reasonable amount of ram for data buffering. Such an architecture is embodied in the VME-STE intelligent Bus Coupler from Performance Interconnect, Inc., Figs 3,4.

The software used to control the STE compatible i/o boards can either be entirely resident in firmware or can be passed from the VME system to the onboard c.p.u. via the dual-port ram. This allows either the STE sub-system or the main VME system to be responsible for configuration and start-up after reset. A simple monitor loop can be devised to pass high level commands through the dual-port ram, and although the high-level command set is bound to be highly application-dependent, PI Inc is attempting to establish a general purpose protocol layer to facilitate developments of i/o control software.

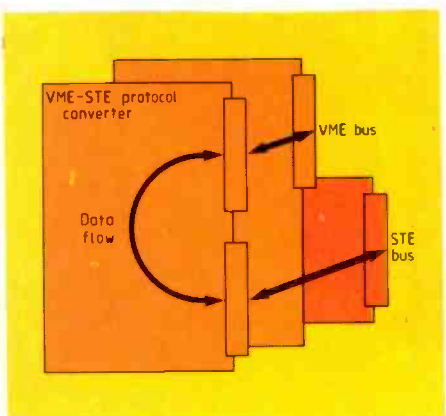
VME-TO-STE PROTOCOL CONVERTER

In the case where there is a requirement for including unusual or elementary i/o in a VME-bus system but no requirement for boosting system performance, significant development and production cost excesses can be avoided by use of a protocol converter card to simply map STE boards into the VME bus address map. The simplicity of the bus interface makes STE a natural choice for custom application design, and the small size of the single Eurocard enables close tailoring of additional hardware to minimize redundant functions.

Performance Interconnect's VME-to-STE Converter board, Figs 5 and 6 provide all of the protocol conversion logic necessary to simply map STE cards into the VME address map. It also contains a programmable interrupt controller to combine all eight STE bus attention-request levels into a single VME bus interrupt. By making use of the protocol converter with STE bus i/o cards, the development and production costs of VMEbus systems can be significantly reduced.

Support for multiple STE bus masters is provided allowing both d.m.a. and additional intelligence to be utilized on the STE bus. An STE bus arbiter is provided and the board maintains the indivisible of read-modify-write sequences through the protocol conversion so that semaphores can be passed between VME masters and STE masters. This allows safe sharing of resources between tasks running independently on each bus – an essential feature of multi-processor systems.

Fig.6. Protocol conversion is one way only: that is, STE masters cannot access the VME bus via the converter. Apart from a terminated backplane, the converter board is all that is needed to connect STE bus cards into a VME bus system. Conversion is transparent to VME masters accessing STE slaves and the board acts as a default master in the STE system.



MECHANICAL OPTIONS

Vendors around the world today make available a plethora of Eurocard-compatible products that have ensured these DIN standards an untouchable reputation in the history of standardization. This success story highlights the value of standards and justifies the many long hours that spirited individuals have donated to the cause. The adoption of the Eurocard standard was probably the most significant feature causing the exploding success of the VME bus market.

Over the years, since the Eurocard mechanical standards began to become popular throughout Europe, a large number of manufacturers have developed an impressive range of compatible racks, sub-racks, modules, desk top cases, portable cases, cabinets, front panels and accessories, all of which can be used to quickly construct novel housings for VME bus and STE bus systems. Since the more recent adoption of the Eurocard by US engineers, even more packaging options have become available from US manufacturers and the number of ways in which a system can be constructed seems endless. Fig.7 shows just one example.

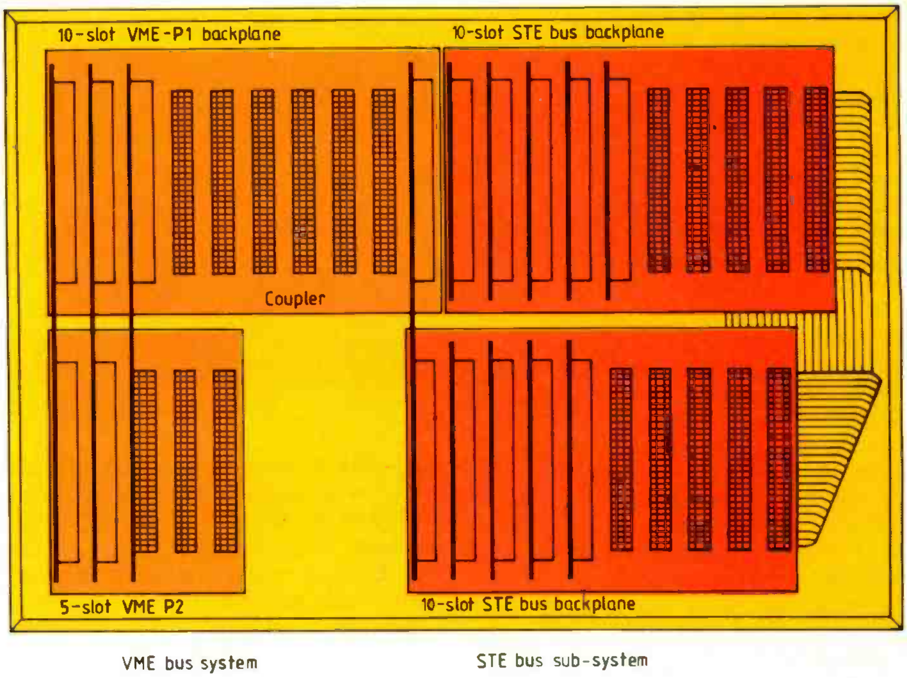


Fig.7. One method of combining a VME system with a maximum STE system in a standard double-height sub-rack takes advantage of STE tolerance to a short extension via ribbon cable. Although not mentioned in the IEEE P1000 specification, STE bus was designed to accommodate short ribbon cable connection as long as each backplane connected is separately provided with power supplies. This capability is provided in the routing of signal protection ground lines and in the settling time tolerance. Absence of daisy-chained signals and the restriction of the signal set to the a and c rows of the connector are also fundamental. Each STE backplane must be terminated only at the end away from the ribbon cable interconnect.

Tim Ellsmore is technical director of Performance Interconnect Inc of San Diego, a subsidiary of Advanced Digital Systems Inc.

NETWORKING

Another method of coupling VME bus and STE bus systems is by local area network. A number of STE systems, each containing their own c.p.u., can act as nodes in a distributed network together with one or more VME systems. Typically, the VME system would be a file server and would incorporate and control common resources such as console management and disc and tape storage. This type of distributed architecture is typical of large-plant process control such as factory automation, and can be achieved using an STE-compatible network interface such as Commendec's (UK) STE compatible token-passing network controller card. The same card can be used to form the VME node, interfacing to the VME masters via a VME-STE bus coupler – this precludes the necessity to develop a VME compatible network interface.

Impact of VME in the UK

If you intend to produce a system for a market while the market window is open, don't spend time and valuable resources reinventing the wheel, says Bob Squirrell. And look to the home market.

Electronics and computer companies in the UK are innovative. The pages of trade and technical journals progressively reveal hundreds of new products being brought to market. The Department of Trade and Industry offers financial assistance for the incorporation of microprocessors into manufacturing processes, for the increased usage of computers in industry, and for the design of new products for the market. And there appears to be no shortage of applicants.

As a supplier of board-level products to many UK manufacturing companies and systems houses, I am particularly aware of the increased use of standard boards based on the VME bus. The increase is not simply due to conversion from one old standard to something more up-to-date, but rather, the market for standard boards in itself is on the increase – and not just in the UK. Certainly, there is a migration from the older standards such as Multibus and STD, but the underlying trend is that of increased usage of ready-designed and manufactured boards from third-party suppliers. However, this is set against a gloomy background in which UK industry is hardly growing at all. The usual indicators such as the semiconductor book/bill ratio show that the electronics industry has not escaped, although recently cautious optimism has reappeared amongst distributors.

The board-level market is predicted to be a major growth area, centred around VME. The reason is not hard to see. VME has become an international standard based on the proven Eurocard mechanical standard (now fully adopted in the USA). It is supported by many major manufacturing companies, including several semiconductor manufacturers, and a great many smaller manufacturers, some of whom are successful start-ups built specifically around VME. It is a public domain standard, supported by its own trade association, VITA. It has the support of the IEEE in the form of the draft standard IEEEP1014, and has been widely publicised by some 200 manufacturing companies worldwide. Its emergence as a vehicle for the 68000 family was timely and, based on the Eurocard, it succeeded in Europe where Versabus failed. Whatever its technical merits (and it has plenty of critics on this point), it has become a bandwagon for manufacturers and users alike.

And so innovators find themselves with a useful standard vehicle for their ideas. Use of ready-made boards, conforming to a widely supported standard, not only cuts down on design cycle times and capital investment, but also on in-house resources in the form of circuit designers, p.c.b. draughters, assembly equipment and operatives, and test facilities. In a situation where the intention is to produce a system for a market whilst the market window is open, why spend time and valuable resources reinventing the wheel? Use ready-made boards from the many on offer and concentrate on system design, software, packaging marketing, and after-sales support.

That a system is based on VME is in itself a sales feature – customers know that the system is expandable and that the boards used are not tied to a single source. Even the power of the system can be enhanced – starting with the 68000 and upgrading to the 68020 version is one obvious route. Field-servicing is easier since most problems can be diagnosed down to board level, and the faulty board swapped on-site. All these points are reasons for the success of VME.

But consider for a moment the extension of this success: UK industry is not growing at the same rate as the VME market. Where is the increased business coming from? It is a result of substitution – ready-made boards in replacement for boards that would otherwise have had to be produced in-house, or sub-contracted.

There is evidence of a change in the way that systems are built, with the design phase starting from selection of a standard bus, then the boards to plug into it, the 'mix' and the application software becoming the key to the specific personality of the system. Whereas previously problems of p.c.b. design and manufacture would have been a major element in a project, the project now starts at a higher level. So what happened to the resource that was previously used in the design and manufacture of the boards? The answer is simple: this is the responsibility of the board-level manufacturer, a third-party company specialising in the production of standard bus boards. The benefits to the user are clear. But how does this fit into the overall pattern of the electronics industry?

Use of ready-made boards conforming to a widely supported standard not only cuts down on design cycle times and capital investment, but also on in-house resources in the form of circuit designers, p.c.b. draughters, assembly equipment and operatives, and test facilities.

The de-emphasis on in-house board design and manufacture, clears the way for specialist companies to supply the market. VME has become the ideal product for a board level manufacturer – high price-ticket items sold on the basis of an internationally accepted standard to customers who already recognise their advantages. VME has become the ideal distributor item, providing a challenge to commodity semiconductors as a potential leader in marketable merchandise for the same reasons.

But consider again: who are these specialist board-level manufacturers? Are they in the local phone book or on the same industrial estate as the p.c.b. house you used to use? They may be if you live in Northants, Co. Durham or a few other locations in the UK. It is more likely you'll find them in the USA, Germany or Japan. My research indicates that over 80% of VME boards sold in this country are from overseas.

If you are designing equipment on the VME-bus for use in the design, manufacture and test of component boards, hope that your overseas marketing is already set up. If the VME trend continues, with the majority of boards for UK consumption being made overseas, there will soon be an identifiable UK reduction in the design, manufacture and assembly of boards, with correspondingly less market for this equipment. Will the trend continue to the point of showing up the UK's semiconductor book-to-bill ratio? What other industries will feel the pinch?

Of course, there are some UK manufacturers of VME boards as there are for other popular buses, most notable being IEEEP1000 (STE) where 29 of the known 32 manufacturers are based in the UK. There is also the opportunity for UK manufacturers to lead the world with manufacture of futurebus (IEEEP896) boards. But for the meantime, the volume market is VME and I state my case in the context of VME.

I make only one request: consider a British VME board first. If you can't find what you're looking for in VITA's guide, call a British manufacturer or a distributor of British-made products. If unable to help, at least they will have gained some market input. And that can be valuable. They might even be on the point of releasing a new product for your application. Just give them the chance. First.

Bob Squirrell is sales director of Dean Microsystems, a distributor of VME boards from predominantly British manufacturers including Plessey, Europel, IMP, Racal, and of most STE products.

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CA1352E	1.75	MC145106P7	7.95	TA7108P	1.50	TBA810AS	1.65	TDA2600	6.50
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HA1366W	3.50	ML231B	1.75	TA7176AP	2.95	TBA820Q	1.45	TDA2640	3.50
HA1377	3.50	MSM5807	6.75	TA7203	2.95	TBA890	2.50	TDA2680A	2.75
HA1156W	1.50	PLL02A	5.75	TA7204P	2.15	TBA920	1.65	TDA2690	2.45
HA1339A	2.95	SAA500A	3.50	TA7205AP	1.15	TBA950/2X	2.35	TDA3310	2.95
HA1398	2.75	SAA1025	7.25	TA7222AP	1.80	TBA990	1.49	TDA3560	5.50
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LA4461	3.95	SN76033N	3.95	TAA350A	3.50	TDA1035	2.50	UPC1182H	2.95
LC7120	3.25	SN76110N	0.89	TAA570	1.95	TDA1037	1.95	UPC1185H	3.95
LC7130	3.50	SN76115N	1.25	TAA661B	1.95	TDA1074A	1.95	UPC1191V	1.50
LC7131	5.50	SN76131N	1.30	TBA700	1.70	TDA1170	1.95	UPC1350C	2.95
LM324N	0.45	SN76226DN	2.95	TBA120AS/B/C/ SA/SB/T/U	1.00	TDA1190	2.15	UPC1353C	2.45
LM380N8	1.50	SN76226N	1.05	TBA395	1.50	TDA1270Q	5.50	UPC1365C	3.95
LM380N14	1.75	SN76533N	1.65	TBA396	0.75	TDA1327	1.70	UPC2002H	1.95
LM383T	2.95	SN76544	2.65	TBA440N	2.55	TDA2002	1.95	555	0.36
LM3900N	3.50	SN76650N	1.15	TBA480Q	1.25	TDA2003	1.95	556	0.60
M51513L	2.30	SN76660N	0.80	TBA510	2.50	TDA2004	2.95	723	0.50
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				TBA530	1.10	TDA2030	2.80	7805	0.65
				TBA530Q	1.10	TDA2522	1.95	7808	0.60
				TBA540	1.25	TDA2523	2.95	7815	0.65
						TDA2524	1.95		

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AC125	0.20	BC182LB	0.10	BD233	0.35	BFT42	0.35	SKE5F	1.45
AC126	0.45	BC183	0.10	BD234	0.35	BFT43	0.35	TIP29	0.40
AC127	0.20	BC183L	0.09	BD236	0.49	BFW92	0.85	TIP29C	0.42
AC128	0.28	BC184LB	0.09	BD237	0.40	BFX29	0.30	TIP30C	0.43
AC128K	0.32	BC204	0.10	BD238	0.40	BFX84	0.26	TIP31C	0.55
AC141	0.28	BC207B	0.13	BD242	0.65	BFX85	0.32	TIP32C	0.42
AC142K	0.45	BC208B	0.13	BD246	0.75	BFX86	0.30	TIP33C	0.95
AC176	0.22	BC212	0.09	BD376	0.32	BFX88	0.25	TIP34B	0.95
AC176K	0.31	BC212L	0.09	BD410	0.65	BFY50	0.21	TIP41A	0.45
AC187	0.25	BC212LA	0.09	BD434	0.65	BFY51	0.21	TIP41C	0.45
AC187K	0.28	BC213	0.09	BD437	0.75	BFY52	0.25	TIP42C	0.47
AC188	0.25	BC213L	0.09	BD438	0.75	BFY90	0.77	TIP47	0.65
AC188K	0.37	BC214	0.09	BD520	0.65	BLY48	1.75	TIP120	0.60
ACY17	1.15	BC214C	0.09	BD538	0.65	BRY39	0.45	TIP125	0.65
AD142	0.79	BC214L	0.09	BD597	0.95	BR100	0.26	TIP142	1.75
AD143	0.79	BC237B	0.09	BD589	0.45	BR101	0.49	TIP161	2.95
AD149	0.70	BC238	0.09	BD701	1.25	BR103	0.55	TIP2955	0.85
AD161	0.39	BC239	0.12	BD702	1.25	BRC4443	1.15	TIP3055	0.55
AD162	0.39	BC251A	0.12	BD707	0.90	BT100A/0	20.85	TIS91	0.20
AD161/2	0.90	BC252A	0.15	BDX32	1.50	BT106	1.49	TV106/2	1.50
AF106	0.50	BC258	0.25	BF115	0.35	BT116	1.20	2N1308	1.35
AF114	1.95	BC258A	0.39	BF119	0.35	BT119	3.15	2N2219	0.28
AF115	2.95	BC2284	0.30	BF119	0.65	BT120	1.65	2N2222	0.29
AF116	2.95	BC300	0.30	BF127	0.39	BU105	1.95	2N2905	0.40
AF117	2.95	BC301	0.30	BF154	0.20	BU108	1.69	2N3053	0.40
AF121	0.60	BC303	0.26	BF158	0.22	BU124	1.25	2N3054	0.59
AF124	0.65	BC307B	0.09	BF160	0.27	BU125	1.25	2N3055	0.52
AF125	0.35	BC327	0.10	BF167	0.27	BU126	1.60	2N3702	0.12
AF126	0.32	BC328	0.10	BF173	0.22	BU204	1.55	2N3703	0.12
AF127	0.65	BC337	0.10	BF177	0.38	BU205	1.30	2N3704	0.12
AF139	0.40	BC338	0.09	BF178	0.26	BU208	1.39	2N3705	0.20
AF150	0.60	BC347A	0.13	BF179	0.34	BU208A	1.52	2N3706	0.12
AF178	1.95	BC461	0.35	BF180	0.29	BU208D	1.85	2N3708	0.12
AF239	0.42	BC478	0.20	BF181	0.29	BU3276	1.20	2N3733	9.50
AFZ12	3.75	BC527	0.20	BF182	0.29	BU407	1.24	2N3773	2.75
ASY27	0.85	BC547	0.10	BF183	0.29	BU500	2.25	2N3792	1.35
AU106	4.50	BC548	0.10	BF184	0.28	BU508A	1.95	2N4427	1.95
AU107	3.50	BC549A	0.10	BF185	0.28	BU526	1.90	2N4444	1.15
AU110	3.50	BC550	0.14	BF194	0.11	BU80Y	2.25	2N5294	0.42
AU113	4.50	BC557	0.08	BF195	0.11	BUY69B	1.70	2N5296	0.48
BC107A	0.11	BC557B	0.08	BF196	0.11	MJ3000	1.98	2N5298	0.60
BC107B	0.11	BC558	0.10	BF197	0.11	MJE340	0.40	2N5485	0.45
BC108	0.10	BCY33A	1.60	BF198	0.16	MJE520	0.48	2N5496	0.95
BC108A	0.11	BD115	0.30	BF199	0.14	MPSA13	0.29	2SA715	0.60
BC108B	0.12	BD124P	0.59	BF200	0.40	MPSA92	0.30	2SC495	0.80
BC109	0.10	BD131	0.42	BF241	0.15	MRF237	4.95	2SC496	0.80
BC109B	0.12	BD132	0.42	BF245	0.30	MRF450A	13.95	2SC1096	0.80
BC109C	0.12	BD133	0.40	BF257	0.28	MRF453	17.50	2SC1106	2.50
BC114	0.11	BD135	0.30	BF258	0.28	MRF494	26.50	2SC1172Y	2.20
BC116A	0.15	BD136	0.30	BF259	0.28	MRF455	17.50	2SC1173	1.15
BC117	0.19	BD137	0.32	BF271	0.26	MRF475	2.95	2SC1306	1.40
BC119	0.24	BD138	0.30	BF273	0.18	MRF477	13.50	2SC1307	2.95
BC125	0.25	BD139	0.32	BF336	0.34	MRF838	13.95	2SC1364	0.50
BC139	0.20	BD140	0.30	BF337	0.29	OC16W	2.50	2SC1449	0.80
BC140	0.31	BD144	1.10	BF338	0.32	OC23	1.50	2SC1678	1.25
BC141	0.25	BD150C	0.29	BF355	0.37	OC28	1.50	2SC1909	1.25
BC142	0.21	BD159	0.65	BF362	0.38	OC29	2.25	2SC1945	3.75
BC143	0.24	BD160	1.50	BF363	0.65	OC32	2.25	2SC1954	0.95
BC147A	0.12	BD166	0.95	BF371	0.25	OC42	0.75	2SC1957	0.80
BC147B	0.12	BD179	0.72	BF394	0.19	OC44	0.75	2SC1969	1.95
BC148A	0.09	BD181	0.45	BF422	0.32	OC45	0.55	2SC2028	1.15
BC148B	0.09	BD182	0.70	BF457	0.32	OC70	0.45	2SC2029	1.95
BC149	0.09	BD183	0.70	BF458	0.36	OC71	0.55	2SC2078	1.45
BC157	0.12	BD201	0.83	BF459	0.36	OC72	0.85	2SC2091	0.85
BC158	0.09	BD202	0.65	BF467	0.68	OC75	0.95	2SC2098	2.95
BC159	0.09	BD203	0.78	BF494	0.45	OC81	0.50	2SC2166	1.95
BC1174	0.09	BD204	0.70	BF495	0.45	OC171	3.50	2SC2314	0.80
BC174A	0.09	BD222	0.46	BF595	0.23	R2008B	1.45	2SC2371	0.36
BC177	0.15	BD223	0.59	BF597	0.25	R2010B	1.45	2SD234	0.50
BC178	0.15	BD225	0.48	BFR39	0.23	R2322	0.58	3N211	2.95
				BFR81	0.25	R2323	0.66	3SK88	0.95
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AA119	0.80	BY208-800	0.33	IN4001	0.04
BA115	0.13	BY210-800	0.33	IN4003	0.04
BA145	0.16	BY223	0.90	IN4004	0.05
BA148	0.17	BY298-400	0.22	IN4005	0.05
BA154	0.06	BY299-800	0.22	IN4007	0.06
BA156	0.15	BYX10	0.20	IN4148	0.02
BA157	0.30	BYX36-150R	0.20	IN4448	0.10
BAX13	0.04	BYX38-600R	0.60	IN5401	0.12
BAX16	0.12	BYX55-600	0.30	IN5402	0.14
BB105B	0.30	BYX71-600	1.75	IN5403	0.12
BT151	0.79	BZY95C30	0.35	IN5406	0.13
BY126	0.10	CS4B	4.50	IN5407	0.16
BY127	0.11	CS10B	8.45	IN5408	0.16
BY133	0.15	OA47	0.09	ITT44	0.04
BY164	0.45	OA90	0.05	ITT923	0.15
BY176	1.20	OA91	0.10	ITT2002	0.20
BY179	0.63	OA95	0.06		
BT182	0.55	OA202	0.10		
BY184	0.35	IN21DR	5.00		
BT199	0.40	IN23B	5.00		
BY206	0.14	IN23C	5.00		
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BZY88 Series	0.10

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CME1428GH	45.00	DP7.5	35.00	M38-120WA	65.00
CME1428W	39.00	DP7.6	35.00	M38-121GHR	65.00
CME1523W	39.00	DN13.78	35.00	M38-121LA	65.00
CME1431GH	39.00	F16-101GM	75.00	M38-122GW	65.00
CME1431W	39.00	F16-101LD	75.00	M38-140LA	65.00
CME202GH	45.00	F21-130GR	75.00	M38-142LA	65.00
CME2024W	45.00	F21-130LC	75.00	M38-341P31	65.00
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D13-51GM/26	85.00	M23-112GM	55.00	V7031GH	59.00
D13-45GH/01	55.00	M23-112GV	55.00	V7031/67A	59.00
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D16-100GH/67	65.00				
D16-100GH/79	69.00				
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4-527V-51000	5150	Capston Motor	29.95
143-0-4904-00900	FVHP615	Gear Idler Assy.	5.95
143-2-457T-05900	VTC9455	Stopper Reel Base	0.55
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ECF86	1.70
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ECF801	0.85
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ECF806	10.25
ECH3	2.50
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ECH35	3.50
ECH42	1.50
ECH81	1.00
ECH83	1.00
ECH84	1.00
ECH2000	1.50
ECL80	0.60
ECL82	0.79
ECL83	2.50
ECL84	0.74
ECL85	0.69
ECL86	0.95
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EF37A	2.50
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EF41	3.50
EF42	3.50
EF50	2.50
EF55	4.95
EF70	1.20
EF71	1.50
EF72	1.20
EF73	1.00
EF80	0.55
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EF94	0.95
EF95	1.95
EF97	0.90
EF98	0.90
EF183	0.65
EF184	0.65
EF730	1.80
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EL86	1.25
EL90	1.75
EL91	6.00
EL95	1.75

EL153	12.15
EL183E	3.50
EL18P	3.50
EL360	6.75
EL500	1.40
EL504	1.40
EL509	5.25
EL519	6.95
EL802	3.65
EL821	8.50
EL822	12.95
EM1	9.00
EM4	9.00
EM80	0.70
EM81	0.70
EM84	1.65
EM85	3.95
EM87	2.50
EN32	15.00
EN91	1.95
EN92	4.50
EX35	235.00
EY51	0.80
EY81	2.35
EY83	1.50
EY84	5.95
EY86/87	0.50
EY88	0.55
EY91	5.50
EY802	0.70
EZ40	2.75
EZ41	2.75
EZ80	0.75
EZ81	0.75
EZ90	1.50
F606	2.95
FWA/800	2.95
G55/1K	9.00
G180/2M	6.95
G240/2D	9.00
GC10B	17.50
GC10D	17.50
GC10/4B	17.50
GC10/4E	17.50
GC12/4B	17.50
GD86W	6.00
GDT120M	5.00
GN4	6.00
GN10	15.00
GR10G	4.00
GS10C	16.50
GS10H	12.00
GS12D	12.00
GT1C	14.00
GT1CS/S	13.00
GTN175M	8.00
GTR150W	1.00
GU20	35.00
GU50	17.50
GXU1	13.50
GXU3	24.00
GXU50SS	14.50
GY501	1.50
GY802	1.50
GZ30	1.50
GZ31	1.50
GZ32	1.50
GZ33	4.50
GZ34	2.15
GZ37	4.50
HAA91	1.00
HABC80	0.90
HBC90	0.75
HBC91	0.80
HF93	0.75
HF94	1.50
HK90	1.05
HL2K	4.95
HL23DD	4.00
HL41	3.50
HL42DD	3.50
HL90	0.70
HL92	1.50
HL13DD	3.50
HT2	4.00
HY90	1.00
HVR2	3.00
K3118	85.00
KR6/3	45.00
KT8C	7.00
KT33C	3.50
KT36	2.00
KT44	4.00
KT45	4.00
KT61	5.00
KT63	2.00
KT66 USA	9.95
KT66 GEC	17.50
KT66 Sp. Yellow Spot	19.50
KT67	9.00
KT77 Gold Lion	10.95
KT81	7.00
KT88 USA	10.95
KT88 G Lion	18.95
KTW61	2.50
KTW62	2.50
KTW63	2.00
KTZ63	2.50
L102/2K	6.95
L102/2K	12.00
LB7-20	95.00
LS9B	6.95
M502A	60.00
M537A	60.00
M5143	155.00
M8079	6.00
M8082	7.50
M8083	3.25
M8091	7.50
M8096	3.00
M8098	5.50
M8099	5.00
M8100	5.50
M8136	7.00
M8137	7.95
M8161	6.50
M8162	5.50
M8163	5.50
M8190	4.50

M8195	6.50
M8196	5.50
M8204	5.50
M8223	4.50
M8224	2.00
M8225	3.95
ME1401	29.50
ME1402	29.50
ME1501	14.00
MH4	3.50
MHL6	4.00
ML4	4.50
MP25	195.00
MS4B	5.50
MU14	3.50
MZ1-100	125.00
N37	12.50
N78	9.85
OA2	0.85
OA2WA	2.50
OA3	2.50
OB2	0.85
OB2WA	2.50
OC2	2.50
OC3	1.50
OD3	1.70
OM4	1.00
OM5B	3.00
OM6	1.75
ORP43	2.50
QRP50	3.95
P61	2.50
P41	2.50
PABC80	0.75
PC86	0.75
PC88	0.75
PC92	3.50
PC97	1.10
PC800	1.10
PC900	1.25
PCC84	0.40
PCC85	0.55
PCC88	0.70
PCC89	0.70
PCC189	0.70
PCC805	0.70
PCC806	0.80
PCE82	0.80
PCF80	0.65
PCF82	0.60
PCF84	0.65
PCF86	1.20
PCF87	0.40
PCF200	1.80
PCF201	1.80
PCF800	0.40
PCF801	1.35
PCF802	0.60
PCF805	1.25
PCF806	1.00
PCF808	1.25
PCH200	1.50
PCL82	0.85
PCL83	2.50
PCL84	0.75
PCL85	0.80
PCL86	0.85
PCL800	0.80
PCL805	0.90
PE1-100	69.00
PEN25	2.00
PEN40DD	2.50
PEN45	3.00
PEN45DD	3.00
PNE46	2.00
PE06-40N	42.00
PFL200	0.95
PL21	2.50
PL36	1.75
PL38	1.50
PL81	0.72
PL81A	0.72
PL82	0.60
PL83	0.52
PL84	0.78
PL88	1.00
PL95	1.75
PL302	1.00
PL345	12.50
PL500	1.10
PL504	1.15
PL508	1.75
PL509	4.85
PL519	4.95
PL802T	3.50
PL820	2.95
PL5557	29.50
PY32	0.60
PY33	0.50
PY81	0.70
PY82	0.70
PY83	0.70
PY88	0.65
PY500A	1.95
PY800	0.79
PY801	0.79
QB3-300	54.95
QB3-1750	139.60
QB5-3500	495.00
QE03-10	4.95
QE08-200	145.00
QF40	65.00
QP25	1.00
QQE02-5	19.50
QQE03-12	7.95
QQE03-20	35.00
QQE06-40	45.00
QQV02-6	19.50
QQV03-10	5.50
QQV03-10 Mullard	15.00
QQV03-20	25.00
QQV06-40A	27.50
QQV06-40A Mullard	45.00
QQV07-50	63.50
QQZ03-20	42.50
QS75/20	1.50
QS75/40	3.00
QS92/10	5.00
QS95/10	4.85
QS108/45	4.00
QS150/15	6.95
QS150/30	1.15
QS150/45	7.00
QS1200	3.95
QS1202	3.95

QS1203	4.15
QS1205	3.95
QS1206	1.05
QS1207	0.90
QS1208	0.90
QS1209	3.15
QS1210	1.50
QS1211	1.50
QS1212	3.20
QS1213	5.00
QS1215	2.10
QS1218	5.00
QU37	9.50
QV03-12	5.75
QV05-25	1.75
QV06-20	29.50
QV08-100	145.00
QV2-2500	45.00
QY3-125	65.00
QY4-250	70.00
QY4-400	76.00
R10	4.00
R16	12.00
R17	1.50
R18	2.50
R19	2.50
R20	1.20
R1169	55.00
RG1-125	4.95
RG1-240A	14.50
RG3-250A	3.50
RG3-1250A	35.00
RK2K25	62.50
RK-208	12.00
RL16	1.50
RPL16	12.00
RPY13	2.50
RPY43	2.50
RPY82	2.50
RR3-250	15.00
RR3-1250	35.00
RS613	45.00
RS685	54.95
RS5688	52.15
S6F17	5.95
S6F33	28.95
S11E12	38.00
A30/2K	12.00
S104/1K	10.00
S109/1K	15.00
S130	5.59
S130P	5.95
SC1/800	5.00
SC1/1100	6.00
SC1/1200	5.00
SC1/1300	6.00
SC1/200	9.00
SP41	5.00
SU42	4.95
TB2.5/300	65.00
TB2-300	45.00
TB3-2000	395.00
TD1-100A	25.00
TD03-10F	35.00
TD3-12	4.00
TDD4	5.50
TP25	19.50
TSP4	7.00
TT11	1.50
TT21	45.00
TT22	45.00
TT100	57.00
TTR-31MR	65.00
TY2-125A	85.00
TY4-400	85.00
TY8-600W	365.00
TYS2/250	375.00
U18-20	2.75
U19	11.95
U24	2.00
U25	0.90
U26	0.90
U37	9.00
U41	6.95
U50	2.00
U82	3.00
U191	0.70
U192	1.00
U193	0.65
U251	1.00
U801	0.75
UABC80	0.65
UAF42	1.00
UBF80	0.60
UBC41	2.25
UBC81	1.50
UBF89	1.00
UBL21	1.75
UC92	1.20
UCC84	0.70
UCC85	0.60
UCF80	1.00
UCH21	1.20
UCH42	2.50
UCH81	1.00
UCL82	1.75
UCL83	2.50
UF41	1.15
UF42	1.15
UF80	1.15
UF85	1.20
UF89	1.00
UL41	5.50
UL44	3.50
UL84	1.50
UL85	0.85
UU5	3.50
UU7	8.00
UU8	9.00
UY41	3.50
UY85	0.70
V235A/1K	250.00
V238A/1K	295.00
V246A/2K	315.00
V2406/1K	225.00
V241C/1K	195.00
V339	3.50
V453	12.00
VLS631	10.95
VP4B	4.50
VP133	2.00
VR75-30	3.00
VR101	2.00
V105/30	1.50
VR150/30	1.15
VT52	2.50

VU29	4.50
VU39	1.50
W21	4.50
W77	5.00
W729	1.00
W739	1.50
X24	4.50
X66/X65	4.95
X76M	1.95
XC24	1.50
XC25	0.50
XFW47	1.50
XFW50	1.50
XG1-2500	75.00
XG5-500	22.50
XL628FT	7.50
XNP12	2.50
XR1-1600A	49.50
XR1-3200A	79.50
XR1-6400A	115.00
Y502	25.00
Y65	6.95
YD1100	75.00
YJ1060	265.00
YL1020	42.50
YL1060	195.00
YL1070	195.00
YL1071	195.00
YL1290	65.00
Z77	1.20
Z302C	12.00
Z359	9.00
Z505S	15.00
Z520M	4.00
Z521M	8.00
Z700U	3.00
Z749	0.60
Z759	19.85
Z803U	18.95
ZA1000	12.50
ZA1001	1.50
ZM1005	8.00
ZM1020	6.00
ZM1021	8.00
ZM1023	7.95
ZM1041	14.00
ZM1082	9.00
ZM1084	10.00
ZM1177	9.00
ZM1202	55.00
ZM1263	4.00
1B22	10.00
1B27	55.00
1B35A	45.00
1B63A	75.00
1C1	2.50
1C5GT	2.50
1FD1	2.50
1G3GT	2.50
1J3GT	2.50
1K3	2.50
1N2	4.50
1N5GT	2.50
1P28	25.00
1P39	19.50
1R5	0.90
1T4	1.00
1U4	1.75
1U5	1.00
1X2B	1.40
1Z2	8.95
2AS15A	11.50
2B7	1.50
2B22	69.50
2C39A	32.50
2C39BA	39.50
2C40	37.00
2C42	29.50
2C43	60.00
2C51	0.75
2C53	45.00
2CY5	1.50
2D21	1.95
2D21W	2.50
2E22	49.00
2E26	7.95
2J42	93.00
2J55	245.00
2K25	35.00
2K25 Raytheon	75.00
2K26	95.00
2K29	250.00
2K48	140.00
2K56	250.00
2X2A	5.00
3A/107B	12.00
3A/108A	9.00
3A/109B	11.00
3A/110B	12.00
3A/141K	11.50
3A/147J	7.50
3A/167M	10.00
3A/2	3.95
3A3A	3.95
3A4	1.10
3A5	4.50
31L5	0.95
3AT2	3.35
3B2	3.00
3B4	4.95
3B7	4.50
3B24	10.00
3B26	24.00
3B28	15.00
3BZ6	1.50
3C4	1.00
3C23	19.00
3C45	24.00
3CB6	1.50
3CN38A	2.50
3CS6	0.95
3CX3	2.50
3CY5	1.50
3D6	4.50
3D21A	29.50
3E22	49.50
3EH7	1.95
3EJ7	1.95
3V4	1.75
3W4GT	2.50
4B5518	115.00
4-65A	59.00
4-250A	79.50
4-400A	87.50
4-1000A	425.00

4B32	35.00
4BQ7A	1.75
4BZ6	1.95
4C27	25.00
4C28	25.00
4C35	145.00
4CX1000A	425.00
4CX4000A	1100.00
4CX250B	49.00
4CX250B EIMAC	59.50
4D32	125.00
4CX250BN	75.00
4CX250K EIMAC	95.00
4CX125C EIMAC	125.00
4CX350A	95.00
4CX350F	79.50
4XC1500B	398.50
4E27	195.00
4GS7	2.25
4J52	75.00
4JC6A	2.95
4KT6	1.50
4X150A	35.00
5A/102D	9.50
5A152M	9.00
5A163K	10.00
5A170K	6.25
5A-180M	9.00
5A-206K	10.00
5AM8	2.15
5AN8	1.20
5AR4	2.00
5AU4	1.50
5B.110M	10.00
5B-254M	14.50
5B-255M	19.50
5B-256M	15.00
5B-257M	15.00
5B-258M	14.50
5C22	125.00
5CL8A	2.50
5J180E	2950.00
5R4GB	5.50
5R4GY	4.95
5T4	5.95
5U4G	2.95
5U4GB	4.50
5V4G	1.50
5Y3GT	1.95
5Z4GT	1.50
6/30L2	0.70
6A/203K	9.00
6A7	4.95
6A8G	1.50
6AC7	2.00
6AG5	1.50
6AG7	1.95
6AH6	2.50
6AJ4	2.00
6AJ7	2.00
6AK5	1.95
6AK6	2.50
6AL5	0.60
6AM4	3.25
6AM5	6.00
6AM6	1.95
6AN5	4.50
6AN8A	3.50
6AQ5	1.75
6AQ8	0.85
6AR5	5.95
6AR8	3.95
6AS5	1.50
6AS6	2.50
6AS7G	4.50
6AT6	0.75
6AT8	1.75
6AU4	2.00
6AU5GT	4.50
6AU6	0.95
6AV6	0.75
6AW8A	2.50
6AX4GT	1.95
6AY3B	1.95
6AZ8	4.50
6B7	2.80
6B8G	1.50
6B10	1.95
6BA6	0.95
6BA7	4.50
6BA8A	3.50
6BE6	0.95
6BG6G	3.00
6BH6	1.95
6BH8	1.50
6BJ6	1.50
6BK4	4.00
6BK7A	1.95
6BL6	85.00
6BL8	1.15
6BM6	115.00
6BM8	0.58
6BN4	1.65
6BN6	1.65
6BN7	4.50
6BN8	3.95
6BQ5	0.75
6BQ7A	0.72
6BL7GTA	3.95
6BR5	0.70
6BR7	4.95
6BR8	2.15
6BR8A	2.15
6BS7	5.50
6BW4	1.50
6BW6	5.35
6BW7	1.50
6BW8	4.00
6BX6	0.48
6BX7GT	3.50
6BZ6	2.50
6BZ7	2.95
6C4	1.25
6C5	1.95
6C6	2.50
6C8G	1.50
6C11	2.50
6C18	2.50
6CA4	4.95
6CA7	3.50
6CB5	3.95
6CB6	1.95

6CD6GA	4.50
6CF6	1.50
6CG7	2.25
6CH6	6.95
6CL3	3.95
6CL6	3.25
6CL8A	1.50
6CN5	1.60
6CM7	2.95
6CS6	0.75
6CS7	0.95
6CW4	6.50
6D6	2.50
6DC6	2.35
6DJ8	0.95
6DK6	1.50
6DQ5	5.95
6DQ6B	2.50
6DT6A	1.50
6DW4	2.15
6E5	3.95
6EA4	4.95
6EA7	2.50
6EA8	2.50
6EB8	1.75
6EM5	2.50
6EM7	2.50
6EU7	1.95
6EU8	1.75
6EV7	2.95
6EW6	2.95
6EW7	4.50
6F1	2.00
6F5	4.95
6F6	2.50
6F6G	2.00
6F7	5.50
6F12	1.50
6F13	3.00
6F14	1.00
6F17	2.75
6F21	2.50
6F23	0.60
6F24	1.25
6F25	1.25
6F28	1.25
6F32	1.25
6F33	17.00
6FG5	1.95
6FQ7	2.95
6G6G	5.50
6GE5	3.95
6GH8A	0.80
6GK5	1.50
6GK6	1.95
6GM6	2.65
6GS7	2.15
6GV7	2.50
6GW6	2.50
6GW8	2.50
6GY5	3.95
6H1	9.50
6H3N	2.50
6H6	1.95
6H6GT	1.95
6HF5	5.50
6HF8	2.50
6HS6	4.95
6J4	2.15
6J4WA	3.15
6J5	2.50
6J6	2.00
6J7	4.15
6JB6A	4.50
6JE6C	6.50
6JU8	2.50
6JS6C	6.50
6J7G	4.15
6K7G	2.00
6K8G	3.00
6KD6	6.50
6KM8	2.50
6KT8	2.95
6L1	2.50
6L15	3.15
6L19	3.95
6L6GC	2.95
6L6GC(GE)	4.95
6L6GT	1.95
6LD20	1.15
6LF6	7.50
6LJ8	2.50
6LQ6	6.50
6N7	2.50
6N7GT	2.50
6P15	1.50
6P25	4.00
6P26	4.00
6P28	2.00
6Q7	1.75
6Q7GT	1.20
6R7G	3.15
6S4A	1.50
6SA7GT	1.35
6SC7	1.50
6SG7	2.50
6SH7	1.35
6SJ7GT	1.20
6SK7	1.35
6SK7GT	1.35
6SL7GT	0.85
6SN7GT	1.35
6SQ7	1.35

6SS7	1.95
6U4GT	1.75
6U6WA	3.50
6U8	1.15
6U8A	1.50
6V6G	1.25
6V6GT	1.50
6VGG	1.00
6Y6G	3.95
6X2N	1.00
6×4	1.50
6×5GT	1.00
6×5GTY	1.00
6×8B	2.25
7A6	4.50
7A7	2.00
7AD7	1.75
7AU7	1.50
7B6	3.50
7B7	2.50
7C5	3.50
7C6	2.50
7E7	2.50
7H7	3.50
7J7	5.50
7Y4	2.50
8B8	2.50
8B10	2.50
8BQ5	1.95
8FQ7	1.95
10D2	1.25
10DE7	2.50
10EW7	2.95
10F1	0.75
10GK6	1.95
10P14	2.50
10P18	0.78
10LD12	0.65
11E2R	85.00
11E3	55.00
11R3	5.50
12A6	3.95
12AD6	1.50
12AH7GT	4.95
12AL5	1.00
12AT6	1.25
12AT7	1.15
12AT7WA	2.50
12AU6	1.50
12AU7	0.85
12AV6	1.95
12AV7	2.50
12AX7GT	1.00
12AX7	0.65
12AX7WA	2.50
12AY7	3.95
12AZ7A	1.95
12B4A	4.50
12BA6	1.50
12BE6	1.95
12BH7A	2.50
12BL6	1.75
12BY7A	2.75
12C8	2.50
12CA5	1.95
12CX6	1.20
12DQ6B	3.50
12DW4A	3.50
12E1	19.50
12E14	38.00
12GN7	3.95
12HG7	4.50
12HG7A	4.50
12J5GT	3.95
12J7GT	3.50
12JZ8	2.95
12K5	1.95
12K7GT	1.50
12K8	1.95
12SA7GT	1.95
12SG7	4.75
12SH7	1.95
12SK7	1.95
12SJ7	1.50
12SQ7GT	1.95
12SN7GT	1.85
12X4	1.95
12SY7	4.50
13D3	3.20
13D7	3.20
13D9	3.20
13DE7	2.50
13DR7	2.95
13E1	145.00
13EM7	3.50
14S7	1.95
16GY5	2.95
17BE3	2.50
17DW4A	2.95
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5692	3.50
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5718	6.15
5725	2.50
5726	2.50
5727	2.50
5749	2.50
5750	1.85
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5899	4.50
5963	1.75
5065	2.25
6005	1.85
6012	16.00
6021	3.65
6057	3.75
6058	3.95
6059	3.75
6060	2.25
6062	4.50
6063	2.00
6064	3.25
6067	7.00
6072	4.20
6080	8.50
6080WA	9.50
6132	10.50
6136	2.50
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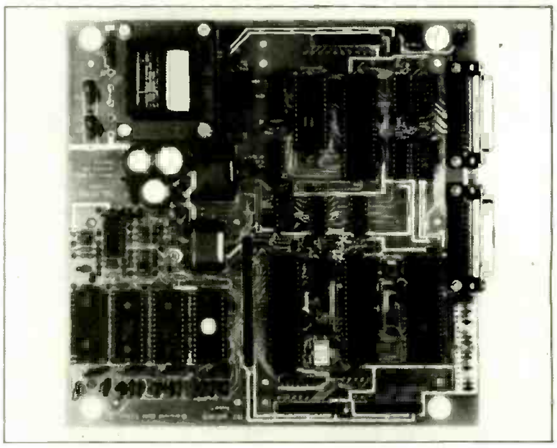

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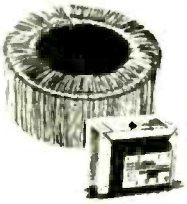

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VME subsystem bus standardized

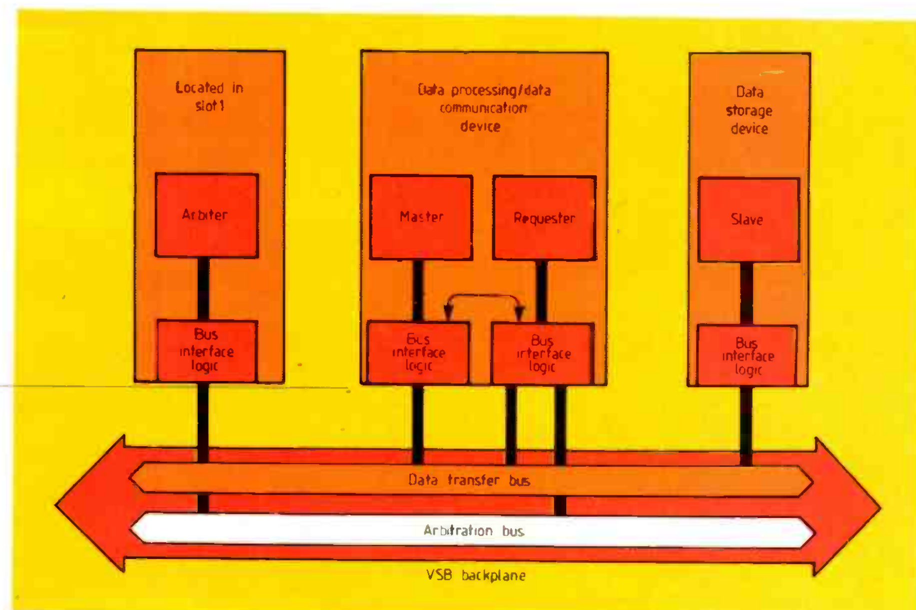
Last year the battle between VMX bus and VMX32 bus ended with acceptance of VSB as the standard local VME bus extension.

ZOLTAN HUNOR

Last year the first revision of the VME subsystem bus reached the market. Initial reaction was astonishment at the complexity of the specification, and at the consequent complexity of the silicon design to be integrated onto boards. An 'idle' state followed, everybody waiting to see what the others were going to do. Motorola's announcement of support for the subsystem bus with custom-designed silicon was the vitalising factor. Suddenly, acceptance of this new development increased and more companies evaluated the idea of introducing the new standard to their production. Henceforth, we hope to see the end of all the customer i/o buses that characterize the chaos around the J2 connector. The dice are thrown. We have VSB.

VSB is a local subsystem extension bus that allows processors to remove traffic from the VME bus to local resources. Increasing demands of multiprocessing systems led to this development, with the aim of improving total throughput through the design of local subsystems.

Functionally VSB consists of two sub-buses, the data transfer bus and the arbitration bus, Fig.1.



PIN	ROW A	ROW B	ROW C
1	AD_{00}	+5V	AD_{01}
2	AD_{02}	OV	AD_{03}
3	AD_{04}	User Defined	AD_{05}
4	AD_{06}	User Defined	AD_{07}
5	AD_{08}	User Defined	AD_{09}
6	AD_{10}	User Defined	AD_{11}
7	AD_{12}	User Defined	AD_{13}
8	AD_{14}	User Defined	AD_{15}
9	AD_{16}	User Defined	AD_{17}
10	AD_{18}	User Defined	AD_{19}
11	AD_{20}	User Defined	AD_{21}
12	AD_{22}	OV	AD_{23}
13	AD_{24}	+5V	AD_{25}
14	AD_{26}	User Defined	AD_{27}
15	AD_{28}	User Defined	AD_{29}
16	AD_{30}	User Defined	AD_{31}
17	OV	User Defined	OV
18	$\overline{IRQ}$	User Defined	OV
19	$\overline{DS}$	User Defined	OV
20	$\overline{WR}$	User Defined	OV
21	SPACE0	User Defined	$\overline{SIZE0}$
22	SPACE1	OV	$\overline{PAS}$
23	$\overline{LOCK}$	User Defined	SIZE1
24	$\overline{ERR}$	User Defined	GND
25	GND	User Defined	$\overline{ACK}$
26	GND	User Defined	AC
27	GND	User Defined	$\overline{ASACK_1}$
28	$\overline{GA0}$	User Defined	$\overline{ASACK_0}$
29	$\overline{GA1}$	User Defined	$\overline{CACHE}$
30	$\overline{GA2}$	User Defined	$\overline{WAIT}$
31	$\overline{BGIN}$	OV	$\overline{BUSY}$
32	$\overline{BREQ}$	+5V	$\overline{BGOUT}$

Fig.1.. The constraints of the P2 connector obliged designers to choose a multiplexed solution for the VSBbus.

VSB DATA TRANSFER BUS

The d.t.b. includes 32 high-speed asynchronous multiplexed address/data lines and associated control signals necessary to execute cycles on the VSB.

Masters use the d.t.b. to select byte locations provided by slaves and to transfer data to or from these locations. Asynchronous transfer protocols allow a slave to take as long as it needs to fulfil its response. Protocols of the VSB define two types of cycles to transfer data: single transfer and block transfer cycles.

A single transfer cycle, either read or write, consists of an address broadcast followed by one data transfer. A block-transfer cycle, also read or write, is akin to a string of single transfers. It allows the masters to provide a single address on the bus followed by a sequence of data without providing additional addreses.

An important feature of VSB is its support of dynamic bus sizing – the ability of a board to automatically adjust the size of data transfer and the number of cycles to the basic data transfer capabilities of the responding board. This allows programmers to store information without regard for the memory organisation on which the software runs. The system hardware adjusts the size of the transfer, transparently to the software.

Many modern processors can perform indivisible sequences of memory accesses that have to proceed one after the other, without allowing another processor or master to interfere and access any of the same locations before the sequence is completed. These processors signal such an access to the outside world in a different way from a normal access. This is one of the integrated features in the VSB through a dedicated line called LOCK. There are two classes of indivisible sequences: the intradomain indivisible sequence, in which access to all the byte locations involved in the sequence is controlled by the same arbitration mechanism, and the interdomain indivisible sequence in

Fig.2. What VMEbus hasn't got the VSB has. Geographical addressing they call it, but in fact it is nothing else than providing each backplane slot with its own ID to implement the interrupt mechanism.

which access to the byte locations is controlled by two or more arbitration mechanisms. An example of such a sequence is one that involves access to a byte location on the VSB and also a byte location on the VME bus.

VSB defines a protocol that allows slaves to request interrupt service from a master. The interrupt protocol of VSB defines how the slave transfers status/ID information to the master to invoke an interrupt service routine. If a slave requests an interrupt from a master and receives an acknowledge signal it must drive an interrupt ID on $AD_{24}-AD_{30}$ lines. This interrupt ID must contain the geographical addressing bits to ensure that each board has a unique code. These bits are slot dependent and are defined as follows:

SLOT	GA_2	GA_1	GA_0
1	low	low	low
2	low	low	high
3	low	high	low
4	low	high	high
5	high	low	low
6	high	low	high

The interrupt ID that a slave drives may contain user defined and supplied bits on $AD_{27}-AD_{30}$.

ARBITRATION BUS

The most fundamental resource of any system is the data transfer bus, and any multiprocessing system needs an efficient allocation method. The VSB offers this through the arbitration bus, Fig.3.

VSB has two arbitration methods, a serial arbitration where a requester module requests the bus and waits for acknowledgement and for the bus to be granted by the arbiter, and a parallel arbitration method where a requester initiates an arbitration cycle. All the requesters that have a request pending participate in the cycle. During the arbitration cycle, the requesters determine which master will be granted the use of the d.t.b. The arbitration method is dynamically selected during the power-up sequence of the subsystem.

There are two basic arbitration modules – the arbiter that co-ordinates the transfer of control of the d.t.b. for the serial arbitration. For parallel arbitration there is no arbiter required (Fig.4) and the requester asks for exclusive use of the d.t.b. on behalf of its associated master.

MECHANICAL REQUIREMENTS

A VSB subsystem consists of a backplane and from two to six VSB boards which are electrically and mechanically connected together via the VSB backplane or a VME bus J2 backplane and associated subrack. The outside two rows of the VME bus J2 connectors are designated as user-defined and on the VSB those roms are defined with the pin assignment shown on page 151.

The full VSB specification is available from VITA-Europe, PO box 192, 5300 AD Zaltbommel, Netherlands for $25.

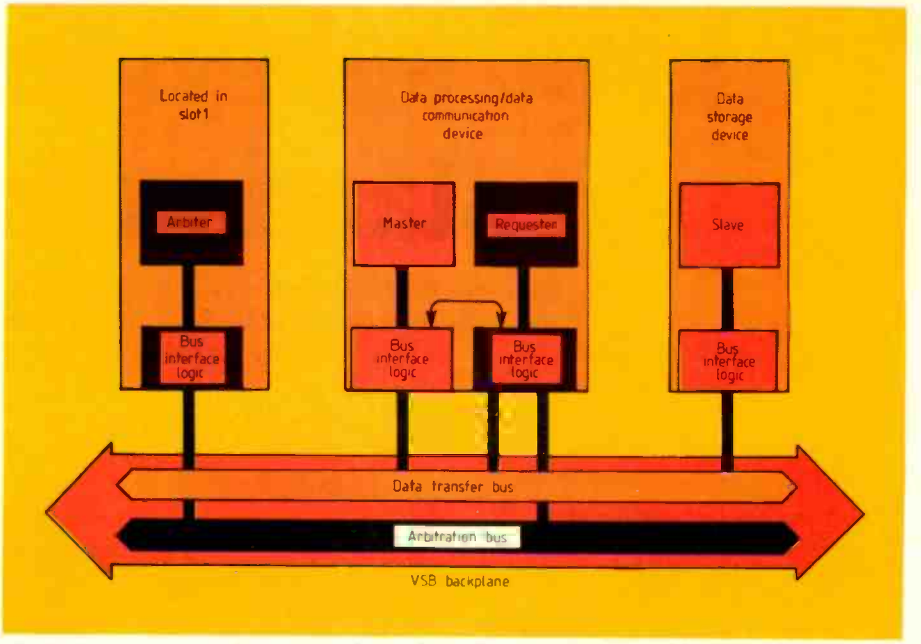


Fig.3. Even a secondary bus of good quality needs bus arbitration; facilities for multiprocessing were also essential.

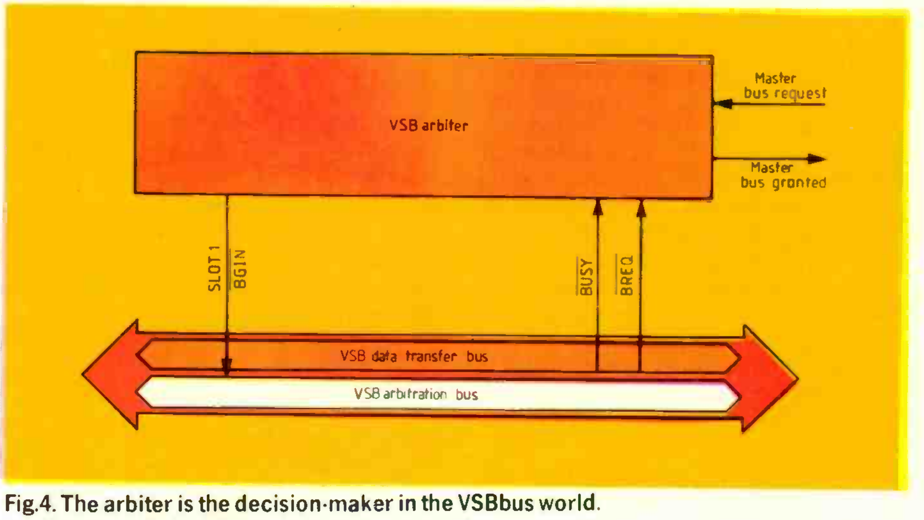


Fig.4. The arbiter is the decision-maker in the VSBbus world.

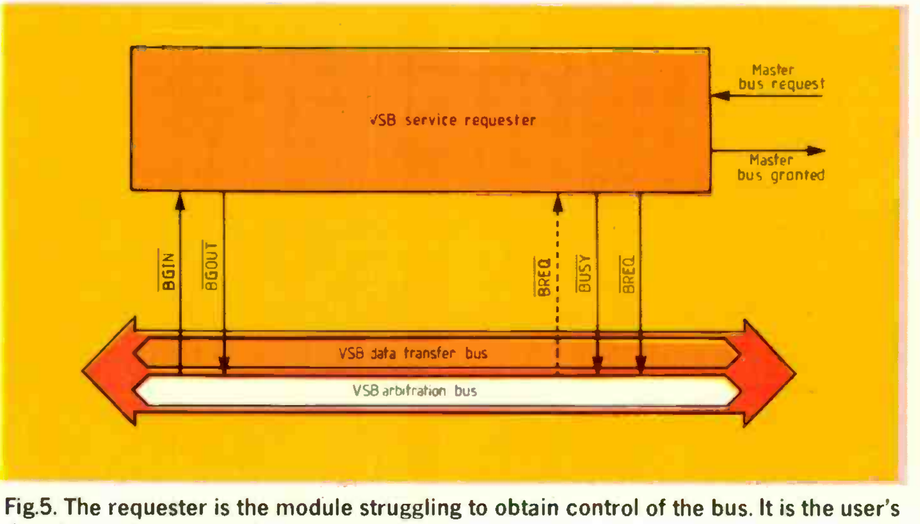


Fig.5. The requester is the module struggling to obtain control of the bus. It is the user's decision to give it a fair chance.

Zoltan Hunor, BSEE, is director of VME International Trade Association-Europe. Born in Romania, he studied electronic engineering at the Polytechnic Institute of Cluj-Napoca and obtained his BSEE degree at the Technical University of Utrecht. He became director of VITA-Europe in July of last year.

TELECOMMS TOPICS

ADRIAN MORANT

£20 million B T directory update

The capacity of the world's largest directory enquiry service will be almost doubled by a £20 million-plus extension ordered from STC by British Telecom. The equipment used is an advanced version of the system developed by Computer Consoles Incorporated (CCI) of Rochester N.Y., USA. STC has subcontracted the installation and maintenance work to Computer Field Maintenance Ltd (CPM) of Hitchin and this represents the largest network installed and maintained by any third-party maintenance company and also the biggest single civil maintenance contract.

Shortly, the British Telecom Directory Assistance System (DAS) will have the processing power for 250,000 calls an hour instead of the current 180,000, giving British Telecom the ability to handle the total customer demand.

Representing an investment in hardware alone of £55m, BT's current DAS service handled around 500 million customer enquiries last year. Some 200 directory enquiry bureaux, and a similar number of management locations using 4,500 terminals, plus communications interfacing equipment and control systems are needed to handle this enormous amount of traffic. The problem is further complicated by the fact that there are a total of about 23 million directory entries, and approximately 35,000 changes a day are processed automatically and distributed nationwide.

DAS has already provided improvements for telephone users with its up-to-date computerized directory, the reduction of the average time for dealing with an enquiry from 52 to less than 40 seconds and greatly increased British Telecom operator efficiency.

CCI has developed what is claimed to be the most advanced emergency telephone system. Scheduled to go on-line in the City of Pennsylvania in March, this enhanced "911" service, to be known as the CCI LIFE-911, will utilize a database of telephone listing names and address together with local emergency information to facilitate rapid response to emergency situations. Additional information that will be presented to the despatcher at the Public Safety Answering Point can include particular information about the address, a nearby intersection or landmark and the particular emergency agencies serving that address.

First all-optical regenerator

What is believed to be the world's first all-optical light regenerator for use in optical communications systems has been demonstrated by British Telecom Research Laboratories, Martlesham Heath. The regenerator, still in the experimental stage, both amplifies and re-times light pulses without converting them from light to electricity as done by conventional regenerators.

Developed by two BT research engineers, Rod Webb and John Devlin, the device is based on the principle that a Fabry-Perot semiconductor laser has nonlinear input/output power characteristics because its effective refractive index varies with optical power level. At some wavelengths, this nonlinearity leads to bistability. In operation, an optical clock signal is fed to the laser to hold the switch state just in the "off" condition. Then, when a pulse of light from the incoming fibre arrives at the laser it has sufficient optical energy to switch on the laser but only when the optical clock signal is also present. This triggers the laser to generate a more powerful burst of light, in synchronism with the clock, which is then injected into the outgoing fibre.

The all-optical regenerator differs from previously demonstrated optical amplifiers in two important respects: bistable operation leads to a signal output level which is relatively constant over a range of input levels: and the signal is retimed by the optical clock.

The regenerator has been operated at 140Mbit/s and its inventors are now working to improve performance. Ultimately, the device will be produced commercially by BT & D Technologies, the optoelectronic components company jointly owned by BT and Du Pont.

A-I-S cable inaugurated down-under

The 4,600km submarine cable link, code-named A-I-S, between Perth, Australia; Jakarta, Indonesia; and Singapore has entered service. Despite Australia's being well advanced in international communications facilities, this is the first submarine telecommunications system to land on its west coast, supplied at a cost of £104million ($150m) by Britain's STC Submarine Systems to the Overseas Telecommunications Commission (Australia), the PT Indonesia Satellite Corporation of Indonesia, the Telecommunications Authority of Singapore, and Cable and Wireless (Hong Kong) Ltd, representing the 12 co-owners.

The 1380 circuit system is designed for a 25-year working life and has more than 8-times the capacity of the Seacom system it replaces. Capable of carrying speech, telex, data and other forms of traffic it links with other recently completed cable systems to Asia, the Middle East and Western Europe.

The magnitude of the tasks involved in the project can be seen from the distance between Perth and Jakarta. This distance of around 3600km is so great that even the CS Cable Venture, which has the largest cable carrying capacity of any cableship afloat, could not complete the link in one lay. She therefore had to buoy-off the laid cable 1927km from Perth and return to Singapore for reloading, prior to completing the lay.

Oftel orders open tender

Prof. Bryan Carsberg, Oftel's Director General, has made his determination listing the descriptions of telecommunications equipment in relation to which BT is for the time being a monopoly purchaser in the UK. In future, BT will have to go out to open tender for these products, even though they are manufactured by BT. Products covered include radio paging equipment, switching systems and payphones.

When announcing his determination he said that: "This determination marks a positive step forward in the development of a healthy competitive environment for the UK Telecommunications Industry. It should give a measure of reassurance to those who have expressed concern about the possibility that BT would favour its own manufacturing subsidiary in order to extend its dominance of the market in products where it already has a dominant supply position..."

The ruling by Oftel formalizes the informal procedure that BT had adopted since the middle of last year to comply with a condition of its licence. This required it to transfer its manufacturing businesses to separate subsidiaries not later than 1 July 1986.

Value-added network services on Vodafone

Istel and Racal-Vodata have combined to make value-added network services (vans) available over the Vodafone cellular radio network. As a result of the commissioning of a direct link Istel's nationwide data network, Infotrac, Comet electronic mail and Viewshare videotex services can now be accessed while away from one's desk via cellular phones.

The system uses Racal-Vodatel developed special protocol, called cellular data link control (c.d.l.c.), which is aimed at overcoming the problems associated with transmitting data through the hostile environment of a cellular radio path. C.d.l.c. has been designed to be transparent to all user applications. A 2400bit/s modem giving a 1200 bit/s net user rate is available which incorporates this protocol and is compatible with the vast majority of lapheld and portable terminals.

Because a c.d.l.c. modem has been incorporated at the point where the Vodafone and Istel networks are interconnected, users wishing to access Infotrac services via Vodafone need only invest in a single modem rather than the two, one at each of a path, which are needed in addition to an appropriate terminal.

First System Y local exchange enter service

The first AXE local digital exchange to be delivered to British Telecom has entered service. It has been supplied by Thorn Ericsson Telecommunications Ltd under a £100million ($150m) contract awarded in 1985 for the supply of 26 exchanges. The AXE switching system was selected by BT to provide an alternative switching system to System X – hence "System Y".

Installed at Sevenoaks in Kent it will initially serve 1500 subscribers locally and a further 2000 in nearby Tonbridge and West Malling via remote concentrators. Ultimately, it will serve 40,000 subscribers before the end of the century.

Delivery of these AXE exchanges will continue for the next 18 months while installation work for them is already in progress at 15 sites.

As well as providing normal telephone service, the Sevenoaks switch will offer what BT refers to as "Star Services". These include abbreviated dialling, repeat last call, three-way conference, call diversion, call waiting and call barring, automatic 'wake-up' call and charging.

Private trans-atlantic cable contract won by STC

The contract for the first private transatlantic telephone cable, to be jointly owned by Cable & Wireless and Tel Optik, has been won by STC Submarine Systems in a deal worth $350million. Known as PTAT1, it is scheduled to enter service mid-1989. C&W is already looking for traffic orders for it in, ideally, minimum, parcels at DS-3 (45Mbit/s). As the company already owns or controls 6,000 miles of digital transmission networks across the USA it fits into the C&W strategy for a global digital highway.

The cable will contain three fibre pairs each of capacity 280Mbit/s. Transmission will be at 1300nm with 50km average repeater spacing. PTAT1 will be followed by PTAT2 as soon as traffic warrants. There will then be an alternative path available in the event of loss of service on one cable.

The cable will come ashore in the UK at Weston-super-Mare, near Bristol at the mouth of the river Severn in south west England. The western end of the 4,300 mile cable will be at Long Island, New York and there is, in addition, a spur to Bermuda. Nynex, the New York/New England Telephone Company, is at present seeking legal permission to buy the Tel Optik stake. In view of the high proportion of transatlantic traffic terminating in the Nynex area, that can be expected to increase market competition.

Mercury places opto orders

Mercury Communications Ltd has placed orders for 565Mbit/s optical-fibre transmission equipment to the value of £1.5million with Plessey Network and Office Systems Ltd. Each 565Mbit/s system can carry 7680 simultaneous telephone calls, or an equivalent amount of data.

One order calls for the supply, installation, testing and commissioning of systems for the Mercury East Coast network. This will link London and Edinburgh via Peterborough, York, Leeds and Newcastle. The other order calls for the supply of 30 terminals and 5 intermediate station equipments to be put into operation by Mercury as and when needed.

BT update

According to Michael Bett, BT's managing director, Inland Communications, by the end of 1987 about 60 per cent of BT's business customers will have access to modern local telephone exchanges. He said this when speaking at a recent conference on BT network strategy. Under its network modernization programme, BT is installing new digital and enhanced electronic local exchanges at the top 500 business exchange sites around the country.

At the same conference, John Tippler, Director Networks, BT Inland Communications, outlined the way that the trunk network is changing. Instead of nearly 400 trunk switching units, the new structure would only have 55 digital trunk exchanges; and all but one of these are already in service. By March 1987, nearly 40 per cent of all trunk traffic will be carried on the network in a digital form. Then, within a further two years, all trunk traffic would have been loaded onto the digital network.

He stressed that the development of the new network would have to take account of economic factors involved in serving residential communities, especially where the rate of telephone usage was low. Tippler went on to say that fibre will quickly find an application in the denser parts of the local loop distribution. This has implication for the size of the areas served by an exchange. While current research and development is also exploring a variety of new ways of delivering the communications services in the low usage environment, Tippler indicated that, looking further to the future, very high capacity optical fibre systems – possibly with one million fibre circuits per fibre by the year 1995 – were already being considered in BT's network strategy.

TIA formed out of TDA ashes

A new organization, entitled Telecommunications Industry Association, has been formed. It has grown out of the Telecom Dealers' Association and claims to be the voice of the whole UK telecommunications industry. It says that "it takes up issues on behalf of its members, provides a range of benefits, negotiates preferential rates for services to its members and acts as a focal point for the industry. The TIA is here to assist and support every sector of the industry from manufacturers to retailers, from distributors to consultants and from wholesalers to installers."

It also gives its objects, which were not stressed by the TDA, "as being to promote high standards of trading, ensure that membership is seen as a sign of integrity, reliability and expertise, and to campaign in the highest circles on behalf of the industry."

The chief executive of the TIA is Richard Woollam. The Association is based at 364-366 Fulham Road, London, SW10 9UH (tel: 01-351 7115).

Double-notch filter simplifies distortion analysis

To support last month's theory that a 'canyon' filter simplifies t.h.d. analysis, Jerry Sokol now describes how such a filter is realized and applied.

B.J. SOKOL

In t.h.d. measuring equipment, using a band-reject filter with a canyon-shaped characteristic instead of the usual notch filter, has advantages – as last month's theory showed. The canyon filter is easier to tune and therefore gives more reliable results. This article discusses converting the theoretical canyon-filter into hardware and shows how the filter is applied in a complete t.h.d. analyser.

Two second-order notch filters form the canyon filter. For use in a distortion analyser, these filters must be easy to tune and have a resonant frequency difference of 3%. Switched-capacitor filters with digitally-related clock frequencies might appear to be an easy way of realizing such a filter, but I found digital noise and beating between the two slightly differing clock frequencies troublesome.

Using a four op-amp active-filter for each notch, however, did prove successful. Sensitivity to component variation is low, the configuration is easily tuned with a variable resistor, and there are other advantages as you will see.

In general, the transfer function for the second-order biquad filter is,

$$H(s)=\frac{s^2+cs+d}{s^2+as+b}$$

where d is the square of the zero frequency ω_z and b is the square of pole frequency ω_p. To achieve the desired second-order notch function, c needs to be zero for zeros on the $j\omega$ axis and d needs to be b for $\omega_z=\omega_p$. Then the general relationship of Q and the middle term of the quadratic gives $a=\omega_p/Q$.

Figure 1 shows how the general biquad function can be realized. The coefficients are related to the passive components (see ref.) by,

$$a=\frac{1}{R_1C_1} \qquad b=\frac{1}{R_2R_3C_1C_2}$$

$$c=a-\frac{R_9}{R_7}.\frac{1}{R_4C_1} \qquad d=b-\frac{\ }{R_8}.\frac{1}{R_2R_4C_1C_2}.$$

This configuration has one great advantage in that the last of these relationships enables an exact match of pole and zero frequencies (e.g. d=b) simply by making R_8 infinite – that is, simply by leaving it out. However then, at the resonant frequency $\omega=\sqrt{b}$ the transfer function reduces to cs/as which has amplitude c/a. Depth of the notch therefore

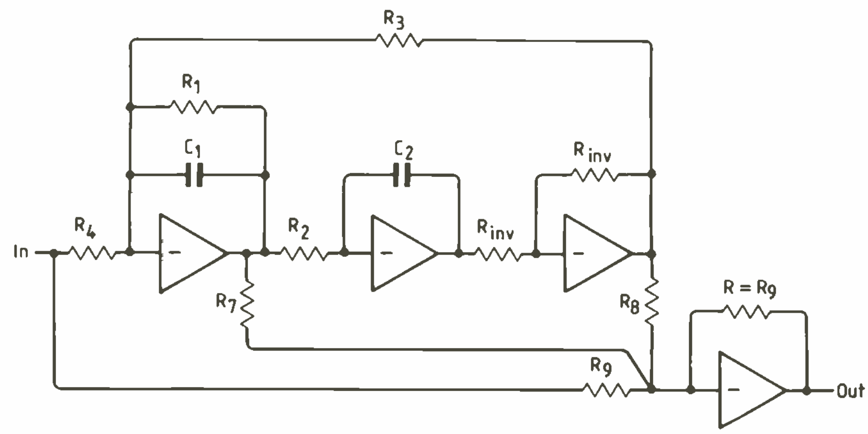


Fig.1. Realization of the general biquad function. This configuration's great advantage is that it enables an exact match of pole and zero frequencies simply by making R_8 infinite.

depends on the degree of cancellation of coefficient c.

This cancellation depends on matching of four resistors because

$$c/a=1-\frac{R_1R_9}{R_7R_4}.$$

For 60dB suppression resistor tolerances of 0.1%, or trimming of at least one of these resistors, would be required.

That difficulty led to a search for another configuration. A successful alternative was suggested by reconsideration of the above biquad arrangement with R_8 omitted. Another way of seeing the same circuit is as a three op-amp inverting bandpass filter with its output summed with the unfiltered input. The unfiltered input can be seen as the result of a transfer function equalling one, which is the same as the function

$$\frac{s^2+as+b}{s^2+as+b}$$

while the inverting bandpass filter has transfer function

$$\frac{-as}{s^2+as+b}$$

The weighted sum of these two transfer functions is clearly the second order notch function only if the weights of the two terms (and thus the opposed s terms in the two numerators) are exactly equal. This requires close component matching.

Looking at the biquad realization of the notch filter in this way not only explains the problem, but also suggests another similar approach which solves it. This time consider the summing of two other filters, a second-order high-pass and a second-order low-pass function. That gives the desired notch response without any s term in the numerator; band-reject filter equals high-pass filter plus low-pass filter, because of the mathematical identity,

$$\frac{s^2+\omega^2}{\text{denominator}}=\frac{s^2}{\text{denominator}}+\frac{\omega^2}{\text{demoninator}}$$

This always-true formula expresses the case exactly if all the denominators are the same quadratic $s^2+A\omega s+\omega^2$.

High and low-pass functions with identical denominators are both available at different points in a single (old fashioned analogue-computer style) Kerwin, Huelsman, Newcomb three op-amp filter. This configuration is illustrated in Fig.2 with the simplification that all resistors around the first op-amp are taken to be equal (unequal values allow high Q's, not necessary for t.h.d. canyon filters). In this case the circuit analysis follows readily from,

$$V_{in}+V_2=V_1+V_3$$
$$V_2sC_1+(V_1/R_4)=0$$
$$V_3sC_2+(V_2/R_5)=0$$

Solving these equations for V_x/V_{in} shows that transfer functions at the three op-amp outputs are standard high-pass, band pass, and low-pass functions respectively.

One more op-amp summing high and low-pass outputs $V_{1,3}$ produces a second-order notch filter, Fig.3. The three equations above show that the denominator of all the filter functions is the same.

$$s^2+(1/C_1R_4)s+(1/C_1C_2R_4R_5).$$

Resonant radian frequency is the square root of the last term, and can thus be tuned by either capacitor or either resistor, or any combination.

All the components need only have 1% tolerance. If 1% capacitors are difficult to obtain, standard tolerance types can be used with proportional compensation applied in either R_4 or R_5. One of these resistors can also be used to produce the 3% frequency offset between the two notches. Since the frequency of each notch depends on a square root relationship, the R_5 resistors of the two notch filters might differ by 6% (because $\sqrt{1.06}\approx 1.03$).

There is one remaining problem, which is that Q of the notches will vary with frequency if the tuning is done by one resistor only. Mathematically this is implied by the easily derived relationship.

$$Q=R_4C_1\omega=\sqrt{(R_4C_1)/(R_5C_2)}.$$

This is a problem we must live with, for four section variable resistors or capacitors are difficult to obtain. The solution is to switch in new fixed components for each frequency range, and to make these ranges fairly narrow. Thus the Qs will vary relatively little. Also the frequency-tuning resistors of the two notch filters only need to be adjustable over a narrow range, which eases the problem of variable-resistor tracking.

There is a further refinement possible which eliminates the summing op-amp at the output of the first notch filter. Input of the second filter is through the non-inverting terminal of its first op-amp. It is thus not a summing node, but due to the high impedance at the non-inverting input, it can serve to average voltages fed to it by equal resistors.

If one of these resistors comes from the high pass and one from the low-pass output of the first Kerwin, Huelsman, Newcomb filter, the effect is the same as using the sum of these output except that there is a gain factor of 1/2 and the (unneeded) inversion due to the summing stage is lost. Each of the (effectively parallel) input resistors must be twice the value of the feedback resistor in the second filter to maintain the same relationship of input and feedback as before. The gain of 1/2 can be cancelled in the final summing op-amp by doubling its feedback resistor to make its gain two. Thus an overall filter with the same responses as the eight op-amp filter, with a gain of one in the passband, is produced with one fewer op-amp, two fewer resistors and less op-amp noise. Figure four shows the complete filter.

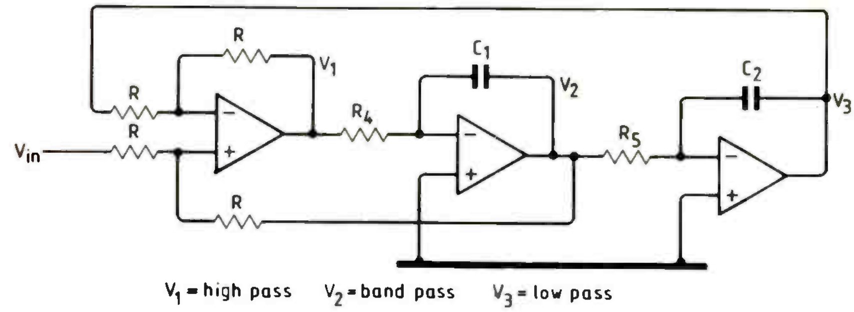


Fig.2. Normally resistors around the first amplifier in this type of three op-amp state-variable filter are unequal in order to gain a high Q factor. Filters for t.h.d. analysis do not require high Q so the circuit can be simplified by making these resistors equal.

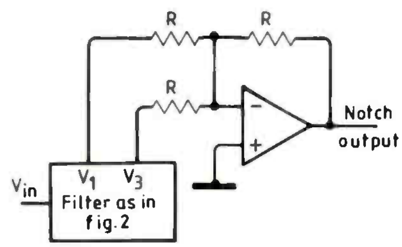


Fig.3. Adding an op-amp to Fig.3 to sum high and low-pass outputs V_1 and V_3 turns the circuit into a second-order notch filter.

PRACTICAL T.H.D. ANALYSER

This section describes remaining circuits required for implementing a double-notch distortion analyser. These are a power supply block, a switching block, an audio-frequency r.m.s. voltmeter block, and filter-adjusting components.

Functions of the blocks can be realized in a variety of ways; these proposals have the advantages of requiring few parts and of being easy to construct through use of specialized i.cs.

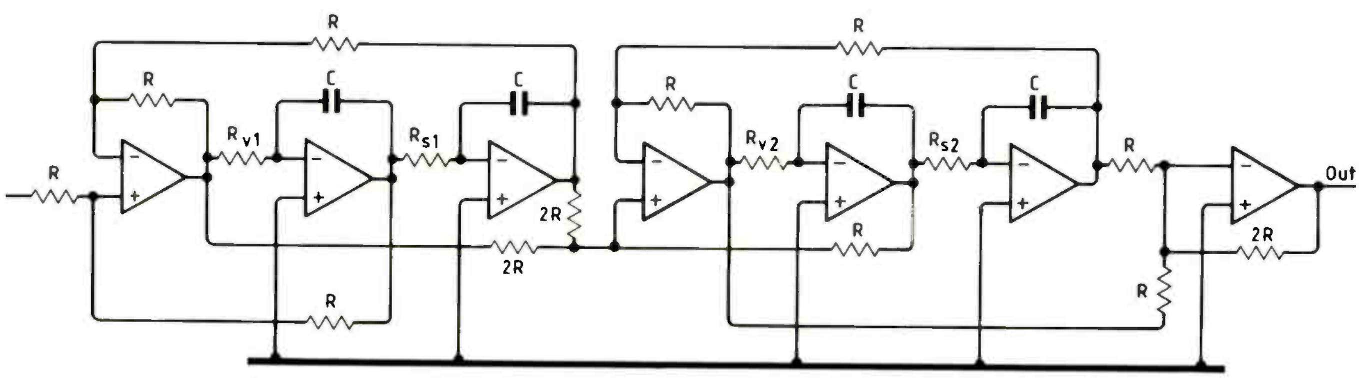
The power supply may be designed around a cheap 6-0-6V type transformer and voltage doubler. Bypass all the analogue chips supply lines and use separate returns to the a single point for earth (as far as possible). To further minimize crosstalk, a printed circuit ground plane is not a bad idea – although I did not find one necessary. To maximise the voltmeter range and to accommodate signals with a high crest factor, + and − 15V supplies are included in the suggested circuits although operation from + and − 9V (two batteries) is a practical alternative.

The switching block simply performs the function shown in Fig.5, to measure input level and then t.h.d. Position the switch well away from sources of interference since it carries very low level signals when in the t.h.d. position.

The r.m.s. voltmeter block needed for t.h.d. measurements is potentially useful on its own, especially if the extra components required for decibel readings are fitted, Fig.6. It uses an AD563A laser-trimmed r.m.s.-to-direct-voltage converter which is suited to logarithmic and linear measurements of true r.m.s. voltage. It is factory trimmed and calibrated for unity r.m.s. alternating-to-direct-voltage conversion and accurate to about 1% of full scale up to 40kHz.

Accuracy of the r.m.s. voltmeter is improved by using the two-pole post filter rather than a single-pole averaging capacitor following the logarithmic-coversion and multiplier stages with the AD563A. These

Fig.4. Complete canyon filter. Using some refinements, a seven op-amp canyon filter with the same response as an eight op-amp version is possible. These refinements reduce not only components but also noise. Gain in the pass band is one.



All op-amps ¼TL074 and R is 22k
Note. For centre of 1kHz C=4n7, R_{s1}=33k, R_{s2}=35k, R_{v1} and R_{v2} are each 28k in series with one half of a 15k dual pot. (adjusts from 900Hz to 1100Hz)

stages output a current source signal on pin 8.

The two-pole low-pass filter is realized using the op-amp stage built into the AD562A which has its non-inverting input on pin 6 and its output on pin 7. This post filter reduces ripple at the d.c. output, which increases accuracy, and allows minimum converter-settling time. Fast settling time permits accurate readings at low input frequencies (the settling time achieved contributes only 0.1% error at 20Hz). This feature is not needed for t.h.d. measurements, but it makes the instrument useful for other audio-frequency voltage measurements.

A preamplifier for the r.m.s. voltmeter is essential for t.h.d. measurement. Gain of this amplifier is switchable to 10 or 100, the latter of course making the percentage of distortion easy to determine.

When making a t.h.d. measurement, the first step is to adjust the input audio-signal level for full-scale reading on the ×1 voltmeter sensitivity range (range A) with the function switch in its signal position. The function switch is now set to t.h.d. to place the double-notch filter in the measurement path. Next, adjust the filter frequency control for minimum output reading, using progressively more sensitive ranges of the voltmeter. Finally, using the ×100 sensitivity settling of the voltmeter range switch (range C), read the t.h.d. directly where the range-C full scale represents 1% t.h.d.

The decibel measuring section of the voltmeter circuit is not essential for t.h.d. measurements because t.h.d. is defined as the linear percentage of distortion (r.m.s.) in an original sinusoidal signal. However adding the components shown within the dotted lines in Fig.5 is easy. These components scale the (normally inverted) decibel output of the converter to make it +100mV/dB.

The decibel measurement section is easily calibrated by means of the adjustment shown in Fig.6. A sinusoidal signal source is applied and adjusted to 1.0V r.m.s. using the linear r.m.s. voltmeter (which is laser calibrated). Then the selector is changed from linear to log and the range switch changed to position B. The Programmable 334Z current source (N.S) is then adjusted so that the meter reads just full scale.

When the logarithmic option is chosen the full-scale swing of each range is 20dB. The ranges are spaced also at 20dB so that a reading of +5 plus a change of one range up (to the less sensitive) for example means +25dB relative to zero of the first range. Thanks to the inverting and scaling op-amp circuit, decibels are displayed linearly across the meter scale starting from zero at the

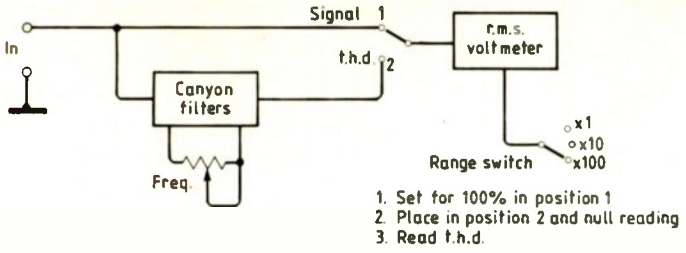


Fig.5. Input level then t.h.d. is measured by the switching block. In the t.h.d. position, the switch carries very low level signals so it should be kept well away from interference sources.

meter's zero. On the least sensitive range (range C) full scale or +20dB corresponds to 10V r.m.s.; on range B this corresponds to 1V r.m.s., and on range A this corresponds to 0.1V r.m.s.

A diode protects the meter from reverse inputs produced by the decibel circuit when inputs below 0dB are measured (e.g. voltages less than 1, 0.1, or 0.01V r.m.s. on ranges C, B, or A respectively). No input signal at all, or 0V, corresponds to infinitely negative dB, which of course will pin the meter needle on the lefthand stop; the diode makes this action safe. When using the log option, it is necessary to see movement to the left of zero on the meter scale for this indicates that a more sensitive range-switch setting is needed to obtain an accurate reading.

When the voltmeter is used with the t.h.d. analyser, the linear r.m.s. scales are read, but you can use the compression effects of the log scales in the first stage of nulling. I applied the t.h.d. analyser to a trusty twenty year old (light-bulb stabilized) Wien bridge oscillator and easily nulled the fundamental to show a t.h.d. of 0.1% at 1kHz. An oscillator monitoring canyon-filter output showed that this distortion consists mainly of spikes produced at zero crossing, presumably by the totem pole output stage of the op-amp in the oscillator.

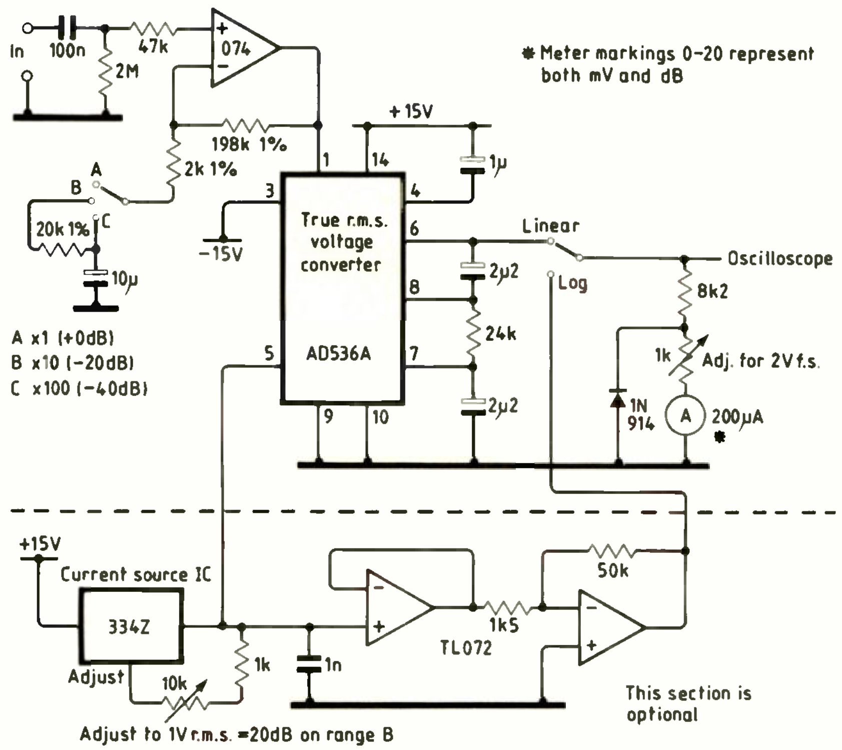
Another experiment was very instructive. I disconnected one of the two notch filters in the t.h.d. analyser to make a conventional t.h.d. measuring set. Then I tried testing the Wien bridge oscillator again. It was extremely difficult to tune the oscillator to the exact frequency to produce a decent null; and once there, it wouldn't stay there. Within seconds it drifted off the null frequency, and a large percentage of fundamental was seen on the oscilloscope. This was presumably due to temperature effects. It was almost impossible to get a good reading of t.h.d. with this set-up, while that was blissfully easy using the full canyon filter.

These circuit realizations or their equivalents provide an easy to use and reasonably sensitive means of measuring t.h.d. in a sinusoidal audio waveform. The double-notch analyser will not replace expensive fully-automatic t.h.d. meters in all applications. And the finite depth of its double-notch canyon filter will not allow it to measure very low t.h.d. levels so it will not replace the fiddly technique of using doubly adjusted bridges for extremely precise measurements. But for everyday purposes, as for example setting tape-recorder bias, or checking a cartridge or preamplifier, it does the job well, cheaply, and easily.

Reference

Formulae from G. Daryanani, Principles of active network synthesis and design, Wiley N.Y., 1976.

Fig.6. This r.m.s. audio-voltmeter block is well suited to t.h.d. measurement. The Analog Devices r.m.s. alternating-to-direct-voltage converter allows both linear and logarithmic true r.m.s. measurements to be made.



SATELLITE SYSTEMS

TOM IVALL

INTELSAT still growing

With the recent addition of Mauritius and Rwanda, the International Telecommunications Satellite Organization (INTELSAT) has grown to 112 member countries. Of these, 27 countries use the organization – a non profit making co-operative – to provide domestic communications.

Currently INTELSAT has 16 geostationary comsats in service, 9 over the Atlantic Ocean, 4 over the Indian Ocean and 3 over the Pacific Ocean. These are a mixture of the INTELSAT IV and IV-A cylindrical types made by Hughes and the later V and V-A box-shaped spacecraft with solar paddles made by Ford Aerospace. The latest V-A comsats, which are really expanded versions of the type V, have a total bandwidth of 2.25 GHz and will carry 15,000 voice circuits.

There is increasing use of digital modulation systems, especially time-division multiple access (t.d.m.a.) in which earth stations use the satellite in sequence by transmitting timed bursts of digits. Recent trials have concentrated on 32-Kbit/s adaptive differential pulse code modulation and other low bit-rate systems.

Tercentenary of Newton's Principia

Newtonian mechanics, although modified by Einstein's relativity, is still accurate enough to be the basis of the astrodynamics by which we launch satellites into desired orbits and keep them properly oriented and on station. The science is enshrined principally in Newton's three laws of motion and his related law of universal gravitation, as found in all general physics textbooks.

Isaac Newton, a professor of mathematics but not yet knighted, worked towards these theories from about 1665 – when the famous incident of the falling apple was said to have occurred. It was not until 1685, however, when he had available Jean Picard's improved value for the radius of the Earth that he was able to complete his science of moving bodies. At about this time he discussed the work with Edmund Halley (whose comet visited us last year) and Halley was so impressed that he encouraged Newton to get it published by the Royal Society.

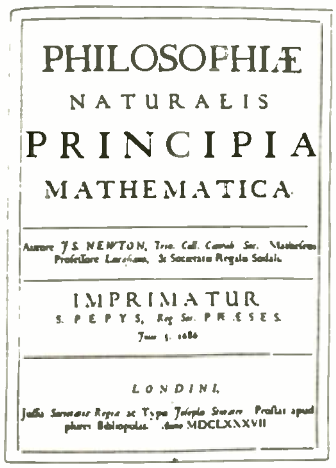
But the Royal Society couldn't afford the expense and in the end Halley paid for a book to be printed himself. This book, actually divided into three volumes, was duly published for the Society just three hundred years ago in 1687 under the title *Philosophiae Naturalis Principia Mathematica* (The Mathematical Principles of Natural Philosophy: the work had been written in Latin as was customary among scholars at that time). Incidentally, the title page bore the imprimatur of Samuel Pepys, of *Diary* fame, who was then president of the Royal Society.

The *Principia* was a scientific masterpiece. It was a brilliant work of synthesis, bringing physics and astronomy together, completing what the late mediaeval physicists had begun and finally solving a problem that had occupied astronomers for thousands of years – the movements of the planets in space. Here, Newton owed debts to Copernicus, Descartes, Galileo (who died the year Newton was born 1642), Huygens and Kepler. If these and others forged individual nails for the coffin of Greek astronomy, it was Newton who hammered them in.

For example, Galileo's famous 'acceleration' experiment, of rolling metal balls down grooves in a board and timing the distances covered, was virtually a prior experimental proof of Newton's second law of motion. It was Kepler, of course, a pupil of Tycho Brahe, who, by immensely painstaking observations and calculations, discovered that the planets moved at varying speeds round the sun in elliptical orbits. He formulated three laws of planetary motion but did not explain the physical reasons for them.

Newton, however, lived at a time when the notion of the inverse square law was in the air. Christopher Wren and Edmund Halley, for example, both thought that gravitational attraction might operate on this principal. But in the *Principia* we see Newton proving, by a breathtakingly complete mathematical analysis, that an inverse square law of attraction would result in Kepler's elliptical orbits. (In other conditions, circular, parabolic or hyperbolic paths.)

And it was Newton who postulated that the attractive force acting from the sun on the planets was the same kind of force which acted from the Earth on the Moon and on every body on the Earth itself. This was a completely new idea – the concept of universal gravitation. Challenged later to explain the precise nature of this attractive force, Newton was unable to reply. He was content to say that it simply acted in the manner he had described and accounted for the motions of all celestial bodies. If artificial satellites had been invented at that time no doubt he would have included them.



PHILOSOPHIÆ
NATURALIS
PRINCIPIA
MATHEMATICA

IMPRIMATUR
S. PEPYS, Reg. Soc. PRÆSES.

LONDINI,

Anno MDCLXXXVII

Title page of first edition of Newton's *Principia*.

This ability to describe natural phenomena precisely but not necessarily explain them is of, course, characteristic of physics. It emerges, too, in Newton's concept of force as expressed in his second law of motion.

Force, as Bertrand Russell has pointed out, is "a mathematical fiction, not a physical entity." Newton made the ghost more visible at least, and certainly very useful to engineering, by clothing it in a definition: force is that which, applied to a body, is proportional to the rate of change of linear momentum (his 2nd law). This now gives us a way of measuring force, whatever it may be, in terms of the acceleration it produces ($F=ma$). And the SI unit of force, deservedly called the newton, is that which applied to a mass of 1kg gives it an acceleration of $1m/s^2$ The *Principia* also made explicit for the first time the basic concepts of mass and momentum.

Coming back to satellites, Newton's third law of motion, on the equivalence of action and reaction, is of course the principle of reaction propulsion as seen in rocket launchers and spacecraft control thrusters.

A simple example of how the mechanics of the *Principia* come into the practical engineering of satellite astronautics is in calculating satellite altitude from orbital period or vice versa. As every schoolboy knows, artificial satellites, like the Moon, are continually falling towards the Earth by the force of gravity but the centrifugal force resulting from their orbital motion offsets this. Provided the orbital velocity is sufficient, the centripetal and centrifugal forces balance and the satellite remains aloft.

By equating the gravitational force F_G exerted by the Earth on the satellite (given by Newton's law of universal gravitation) to the centrifugal force of the satellite F_C (given by Newton's second law of motion), we can arrive at a formula relating the satellite's orbital period to its altidude. Thus $F_G=G.m_E m_S/r^2$ is equated to $F_C=m_S r\omega^2$, where m_E is the mass of the Earth, m_S the mass of the satellite, G the gravitational constant, r the distance between the Earth and satellite centres of mass, and ω is the angular velocity of the satellite in its orbit, $r\omega^2$ being acceleration. Simple algebraic manipulation yields the expression:

$$T^2=4\pi^2 r^3/Gm_E$$

where T is the orbital period. If this is evaluated for, say, the Spot satellite mentioned last month, its altitude of 822km (part of r) corresponds to an orbital period (T) of 101 minutes.

Microterminals for data

Alan Smith walked into the IEE lecture theatre, opened a briefcase and took out what looked like a folding umbrella, a small electronic unit about the size of a book and a hand-held keyboard. He opened the 'umbrella' to reveal that it was in fact a crossed-dipole antenna with an octagonal wire type reflector. He connected it to the electronic unit and, hey presto! we had a complete, portable, battery-powered u.h.f. satellite communications earth terminal assembled before our very eyes.

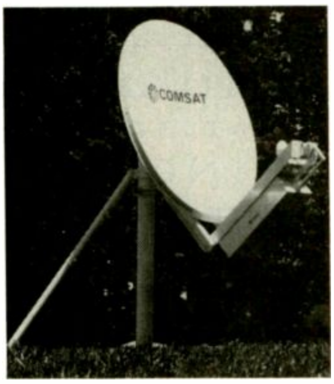
The occasion was an IEE colloquium in London on small-terminal satellite communication systems. Alan Smith was from the satellite communications centre of the Royal Signals & Radar Establishment, Defford, Worcestershire. He and his colleagues have been developing extremely small portable terminals, now becoming known as microterminals, for use by the military. His u.h.f. prototype operates in the 240 – 322 MHz band through satellites such as the military Skynet 4 or the civil Marisat. Two such terminals can work with each other.

The secret of its small size and portability is a deliberately restricted performance. It will only work in simplex mode and will only transmit and receive data, and that at the very low bit rate of 50 bit/s – typewriter speed. Thus the signalling bandwidth is very small and the power can be quite low to achieve an adequate signal/noise ratio. In fact the r.f. power output is 20W. Working through a Marisat transponder to a large earth station at the other end, the s/n ratio referred to unit bandwidth is 43 dBHz, which is 15dB above the threshold for 50-bit/s data.

Data is entered on an ASCII alphanumeric hand-held keyboard. A synthesizer controls the transmit and receive frequencies in 10kHz steps over the full satcom band and is set by a selector. Modulation is d.p.s.k. at 50 bit/s. The circuitry uses conventional bipolar transistors with some thick-film hybrid construction. The receiver front-end has a 3dB noise figure. Including the rechargeable batteries, the weight is about 2kg.

Although Mr Smith is working in the military field he said this kind of hand-held equipment also opens up possibilities in civil satcoms for quick-reaction emergency and disaster applications in situations where conventional communications are not within reach. But the restricted u.h.f. spectrum space available for satcom use would put a limit on the growth of a such a device. However, there would clearly be scope for receive-only terminals of this kind, and the number of these that could be used would not be limited by the bandwidth constraints on the transmit/receive version. The technology for civil equipment would be similar to that used in the RSRE prototype.

The whole IEE colloqium was, in fact, very much biased towards the growing use of microterminals for data communication. Several contributions referred to the "Ku-band explosion" that has occurred in the USA. This has resulted partly from the technological and commercial possibilities opened up by the short Ku-band wavelengths and partly from the deregulation of public telecommunications in the USA.



Antenna and r.f. unit of Comsat's microterminal for their data networking system. The r.f. section mounted on the offset feed arm houses a low-noise down-converter, an up-converter/synthesizer and a 2.2W solid state r.f. power amplifier using fets and thin-film microstrip. The pole support can be mounted on a transportable metal baseplate for quick deployment.

Private satcom terminals with dish sizes of 1.2m – 1.8m for medium speed data communications (56 kbit/s to 1.544 Mbit/s) have been springing up at business premises all over that country. These have become known as 'very small aperture terminals' (v.s.a.ts). Their purpose is to establish multi-point networks with up to about a hundred remote sites.

These v.s.a.ts typically have an offset-fed parabolic reflector, and one being supplied by Comsat (Communications Satellie Corporation) for its Starcom interactive data networking system is shown in the photograph. As described by Jonathan Collins of Comsat (UK) Ltd, this system is arranged like spokes going into the hub of a wheel. The 'hub' is the central network control point. Connected to the hub are several mainframe host computers belonging to the user. Connected to the remote v.s.a.ts are other computers of the user's data network. Data is transmitted from the hub to the v.s.a.ts by t.d.m. and from these remote terminals back to the hub by random access t.d.m.a.

The system allows any of the user's host computers to 'talk' to any of his remote v.s.a.ts. This can be done either individually or to all terminals simultaneously. Network control also permits other hosts to communicate with particular user v.s.a.ts and for any v.s.a.t. to communicate with any host.

Host computers are linked to the hub through terrestrial circuits with user's interfaces working at 9.6, 19.2 or 56 kbit/s. In a terrestrial circuit the user's host 'talks' to the hub by using a normal polled protocol. At the hub the system separates the data from the normal protocol and puts it into a special Comsat error-correcting protocol. It then goes into a buffer where it is formed into packets, and these packets from the various interfaces are multiplexed by t.d.m. into a signal which is transmitted to all the remote terminals.

In the return direction of communication, the network control system arranges for the v.s.a.ts to transmit to the hub in random access t.d.m.a. by a system of indentifiable packet frames with timing and synchronization.

Such private satcom data systems are not taking on in Europe, for several reasons. First of all the regulatory laws do not allow it. Anybody can install a receive-only terminal to pick up television programmes, but private individuals or organizations are not permitted to transmit directly to satellites. You can only communicate via satellite systems through the terrestrial networks and earth stations of the official national organizations, such as British Telecom and Mercury in the UK. Naturally the telecoms authorities, whether privatized or not, don't want to lose terrestrial communications revenues as a result of satellite 'by-passing' as it is called in the USA.

In Europe there is also less demand for multi-point data services over long distances, and various restrictions on the transmission of data across national frontiers. However, there might be a possibility for European telecoms organizations to offer a type of service based on a shared hub system. One big earth station would provide facilities for a large number of users in different networks.

This approach is currently being investigated through trials in the UK, France and Germany. In the UK, Mercury Communications has just started such a data trial service. It has been developed by them with Comsat Technology Products and utilizes the INTELSAT space segment (see first item). Co-operating in the trial, which covers technical, operational and commercial aspects, are IBM United Kingdom, the London Stock Exchange and Electronic Data Systems.

The trial data service operates over a star-shaped 'intelligent' digital network. A single or a small number of central hosts are linked to a large number of remote terminals. Traffic can be broadcast from host to terminal only, or it can be interactive. Communication may be to a single terminal, selective to a group of terminals, or to all the terminals. Data from the host is converted from the host equipment protocol to the network protocol and transmitted in packet form over the satellite link at 256 kbit/s. Data from the remote terminals is similarly transmitted in packets over the satellite link network at 56 kbit/s.

At the remote terminal there is a 1.2m antenna for transmission and reception. Its outdoor equipment is connected to an intelligent indoor unit which provides the interface to the user's terminal equipment. In addition to handling data, the indoor unit also provides speed and protocol conversion and error correction. The whole technology is based on software so that new protocols can be developed fairly easily to handle options that may emerge or specific markets or applications.

RESEARCH NOTES

JOHN WILSON

Thin layers-faster circuits

The Cavendish Laboratory of Cambridge University has become the third British research centre to join a major programme of investigation into low dimensional structures, sponsored by the Science and Engineerng Research Council (SERC). A total of £24 million is expected to be spent over the next four years. So far industry itself has contributed over £2 million in direct support.

Low dimensional structures are formed by the deposition of semiconductors layers only a few atoms thick and etched by ion beam techniques. In these structures electrons cease to behave in the same way as they do in bulk solids, thus opening up the possibility of smaller and faster circuit elements. The variety of possible low dimensional structures far exceeds those that can be fabricated from bulk solids.

At present, the bulk of the research is concentrating on techniques to produce the necessary semiconductor samples. Oxford and Nottingham Universities are working on vapour deposition and molecular beam epitaxy respectively, whilst the Cambridge group will also be using m.b.e. techniques, together with ultra-fine lithography. With additional funding from BT and GEC this work will specialize in structures built from gallium arsenide and gallium aluminium arsenide.

Decisions, decisions

Senior executives, at least if tv advertising is anything to go by, don't make much use of personal computers. One suspects there's even a degree of technofear in the boardroom!

Things may be changing, however, to judge from a study of 113 senior managers of US corporations, conducted by the Stanford University Graduate Study of Business. This study shows that senior and chief executives use their machines on average seven hours per week.

What is equally interesting is the use to which different levels of management put their p.cs. Conventional wisdom suggests that top management would use computers for decision making, whilst middle management would use them primarily for information processing. What the Stanford Study reveals in fact is the exact opposite. Top managers, it appears, use their machines to keep an eye on how the company is doing, whilst the middle managers are using them for decision making, analysis and planning.

Polymer-electrolyte batteries

Research at Leeds University, in conjunction with Venture Technology, is leading to promising new solid electrolytes for batteries. These are mostly polymers in which inorganic salts such as lithium perchlorate can dissolve and ionize. In this respect they behave no differently from liquid electrolytes, though their conductivity is usually much less.

Whilst this may be overcome to some extent by the use of a very thin film of polymer, there are still problems in trying to make a battery with low internal impedance for high current applications. To achieve a performance high enough for automotive applications, a battery with a polyethylene oxide electrolyte would have to operate at inconveniently high temperatures (above 100°C). The Leeds team are therefore concentrating their efforts on applications where a modest internal impedance is no handicap, for example in microelectronic devices such as memories. They are also working on new chemical structures for polymers that will function more effectively at room temperature.

The most promising of these are known as 'comb' polymers; that is, they have a backbone structure with sub-units of polythene oxide sticking out like the teeth of a comb. By cross linking the molecules, it is possible, to some extent, to tailor the polymer to suit a specific application.

Obviously, the compatibility of the polymer with particular electrodes is important to the success of any practical battery. To this end, Venture Technology are evaluating a number of promising materials. If successful, this work will lead to batteries which are leakproof, relatively non-toxic and capable of working at temperatures beyond which a liquid electrolyte would either freeze or boil.

Dancing dopants

Although diffusion of dopant atoms into silicon lattices is fundamental to virtually every semiconductor manufacturing process, surprisingly little is known about what goes on at the atomic level. The usual assumption is that the dopant atoms – usually of a group III or IV element – find their way into the silicon lattice through defects such as missing or supernumary atoms.

That simple view has now been challenged by K.C. Pandey of IBM's Thomas J. Watson Research Center in New York. Pandey has developed a theory that will work even with a perfect silicon lattice. According to this theory, the dopant atoms link themselves to the silicon atoms by re-configuring the chemical bonds. The atoms can then change places in the lattice by slowly rotating and breaking only a minimum of bonds. So, in effect, the dopant is passed through the lattice in a sort of 'atomic folk dance'.

This theory not only explains how diffusion can be accomplished with relatively low energies, but also how some dopants such as phosphorus and aluminium can move through a silicon lattice faster than atoms of silicon itself.

Computer graphics i.c. design

Realistic computer-generated moving pictures for such applications as flight simulators and car design will be the goal of new research for which two University of Sussex electronic engineers have just received a £339,000 grant. The research into integrated circuit design for high-performance computer graphics systems will be carried out jointly with GEC's Hirst Research Centre at Wembley and Singer Link Miles at Lancing.

The techniques to be developed will result in better and cheaper systems for application in flight-training simulators for pilots, industrial graphic design and television animation.

The award to Dick Grimsdale, Professor of Electronic Engineering, and Dr Paul Lister, Lecturer in electronics, has been made by the Science and Engineering Research Council under the Alvey Programme. The work will involve the development of new forms of computer architectures to support the extremely high processing rates required for high-performance graphics display systems.

The development of these architectures will involve v.l.s.i. technology which will eventually, it's hoped, lead to high-performance graphics systems that are better and significantly cheaper than current systems.

Underwater optics

The first under-sea trial of a submarine optic-fibre system using 1.55μm technology has been successfully conducted in the Pacific, near the Amani Islands. The low loss at this wavelength enabled satisfactory operation at 446Mbits/s. over a 120km line.

Existing commercial systems use a 1.3μm technology, which is simpler and cheaper, but requires a repeater spacing of 40-50km for a data rate of 280Mbits/s. Such technology will continue to form the basis of commercial systems until the end of the decade. Nevertheless the demand for wider repeater spacing and a greater data rate, especially for undersea cables, will necessitate a move to 1.55μm for the next generation of systems. This is the wavelength at which fibre loss becomes minimal.

The researchers, from the Nippon Telegraph and Telephone Corporation, used in their tests a newly developed zero-dispersion fibre, specially designed for minimum bending loss. Its best loss figure is actually about 0.205 dB/km. The cable used in the test was looped back and forth over a 7km path and contained 12 splices, each causing an additional 0.121dB loss.

Also tested in the same undersea environment were the regenerators designed to work with the cable. Each comprised four bipolar i.cs, one InGaAs avalanche photodiode and a distributed feedback laser diode.

Results showed a fibre loss change during laying of no more than 0.007dB/km. Also no change of chromatic dispersion was noted, even at the maximum cable tension. In fact, error free operation at 446Mbit/s was maintained throughout the whole operation.

These figures are, of course, nowhere near the limits of 1.55μm technology under ideal terrestrial conditions. Using similar optoelectronic systems in the laboratory, AT&T Laboratories in the USA have successfully operated an 80km link with splices every 2km at a bit rate of 1.6 Gbit/s.

Microwave modulation goes digital

British Telecom is to start engineering trials this year of advanced modulation equipment which could increase the capacity of its digital microwave radio network by up to a third. Four contracts worth a total of £1.5 million have been awarded to GEC Telecommunications, STC Telecommunications, the Italian firm Telettra and to NEC of Japan.

The equipment operates in the lower 6GHz frequency band and uses a technique known as 64 q.a.m. – quadrature amplitude modulation. It will be installed on three radio links and is due to start operating this summer. British Telecom will then evaluate the performance of the equipment for general use in the network. The 64 q.a.m. equipment will allow eight channels, equivalent to 16,000 calls, to be fitted into one band, increasing its capacity by 33 per cent.

64 q.a.m. is the latest evolution in the development of digital modulation techniques aimed at making more efficient use of the radio spectrum. Early digital systems used by British Telecom employed four-phase modulation called quadrature phase shift keying (q.p.s.k.) and this is used on the 11GHz equipment. To improve efficient use of the spectrum the 4GHz band will use a q.p.s.k. technique where the band width is deliberately restricted to less than the theoretical requirement (reduced bandwidth q.p.s.k.). This requires elegant techniques to compensate for the inevitable distortions due to the reduced bandwidth.

An alternative is to modulate the carrier not only in phase but also in amplitude – generally termed quadrature modulation (q.a.m.). In 16 q.a.m. the carrier can take any one of 16 discrete states and this reduces the symbol rate (which determines the amount of radio spectrum bandwidth required for transmission) to one quarter of the bit rate to be transmitted. 16 q.a.m. will be used in the upper 6GHz frequency band.

The 64 q.a.m. technique again utilizes amplitude and phase modulation to produce 64 discrete carrier states, thereby reducing the transmission symbol rate to one sixth of the channel bit rate and hence reducing the required transmission bandwidth to about 23MHz. This enables the existing, internationally recommended frequency channel plan to be re-used and produces a band utilization somewhat better than the 1800 channel and analogue systems currently used in the band.

64 q.a.m. systems are more demanding than the earlier systems in terms of sensitivity to transmission impairments, such as noise, symbol distortion and interface, and powerful countermeasures against multipath fading effects are therefore necessary.

British Telecom has carried out theoretical studies, and field trials have shown that overall there is no technical penalty involved in adopting 64 q.a.m. for the lower 6GHz band.

500V power mos

Until now it hasn't been possible to integrate low power logic circuits with high voltage power mosfets on a single chip. Isolation problems have limited power chips to about 100V, well below the maximum for discrete mosfets.

Ixys Corporation in San José, California, have now developed an experimental chip that successfully combines low power c-mos control circuitry with a mosfet operating at 500V and 25A. They claim that with power mosfets being the fastest growing area of the semiconductor market, there is likely to be a huge market for fully integrated control systems for process control, switched-mode power supplies and automotive applications. Having already successfully integrated a small amount of logic with a power mosfet, Ixys hope by the end of the year to develop analogue and digital p.w.m. circuits.

Making these products work is no easy task because the currents through the power mosfets create noise that can cause the c-mos devices to latch-up. Also the high temperatures (150°C) tend to increase parasitic currents which further increase the likelihood of latch-up.

The answer to these problems, according to Ixys, is to change the traditional layout of cells in the low-power c-mos section of the devices. By means of a process similar to that used for the company's existing high-performance double-density (hdmos) power fet, they intend to fabricate the low and high-power devices simultaneously, side by side on the same chip. They also expect before long to uprate the devices to run at 1000V.

Materials analysis service

ERA Technology has installed thermal analysis equipment to increase its capability in the fundamental study of materials.

The equipment, a differential scanning calorimeter, is being employed to monitor changes in the enthalpy (heat content) of a material as a function of temperature or time. The small changes which most chemical and physical transformations produce can be examined quantitatively to provide data for materials characterization and comparison.

ERA is already using the equipment in a project, sponsored by the Electric Cable Manufacturers' Confederation and the Department of Trade and Industry, to investigate the performance of crosslinked, polyethylene, high-voltage cable insulation. Other applications for which the facility will be used include the study of the curing reactions of epoxy and polyester resins, crosslinked polyethylene, varnishes and adhesives, thermal degradation and oxidation. The differential scanning calorimeter can also be used for cost-effective quality control and fault investigation.

Magnetic materials

A new develop in materials technology is responsible for further improvements to the range of rare-earth, high-energy permanent magnets available from Mullard Ltd. Known as RES 270, it contains iron, boron and neodymium and can achieve magnetic energy levels of 27 megagauss oersted. For the time being, samples are available only in simple experimental shapes.

Rare-earth magnets are capable of providing more magnetic energy than magnets made from any other material. This high energy, combined with high coercivity, enables designers to reduce the volume of magnetic material required for any particular application. Another advantage is that the iron/boron/neodymium mixture is much cheaper than the traditional cobalt/samarium compound used for high-energy applications.

At the moment, RES 270 is confined to maximum operating temperatures of 130°C, though Mullard researchers are looking at modified mixtures which, they hope, will retain their magnetic properties at higher temperatures.

Researching the researchers

'Research Notes' can't yet afford a correspondent in every town. If your company, university, etc. has a story that's worth telling, please send any suitable papers, abstracts, scribbled notes, photographs to 'Research Notes' 25, Quarrendon Road, Amersham, Bucks. HP7 9EF.

APPLICATIONS SUMMARY

USING VOLTAGE-TO- FREQUENCY CONVERTERS FOR ANALOGUE CONVERSION

Serial output of a voltage-to-frequency converter is turned into a parallel digital representation of input voltage simply by feeding the serial-output stream into a time-gated counter. Analogue-to-digital converters made using such a building block are slower than successive approximation types, but they can be very accurate.

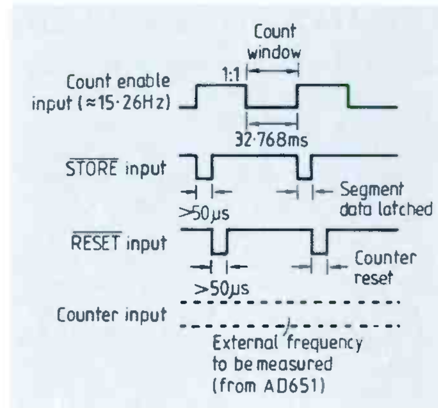
There are three main advantages of using voltage-to-frequency devices for a-to-d conversion. Unlike converters based on binary-weighted networks, converters using v-to-f devices are inherently monotonic under all supply and temperature conditions. Secondly, the analogue input signal is converted to an easily transmitted serial bit stream. As a result the analogue section, consisting of any signal conditioning circuits and the v-to-f converter, can be located close to the signal source and the digital circuits comprising counters, the timing gate and display (or digital processor) can be remote.

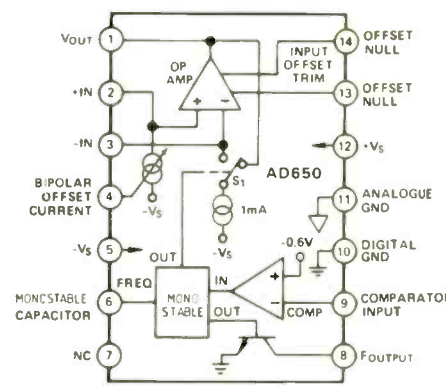
Finally, since the digital representation is accumulated over a large number of cycles, integration and therefore reduction of unwanted signals is inherent.

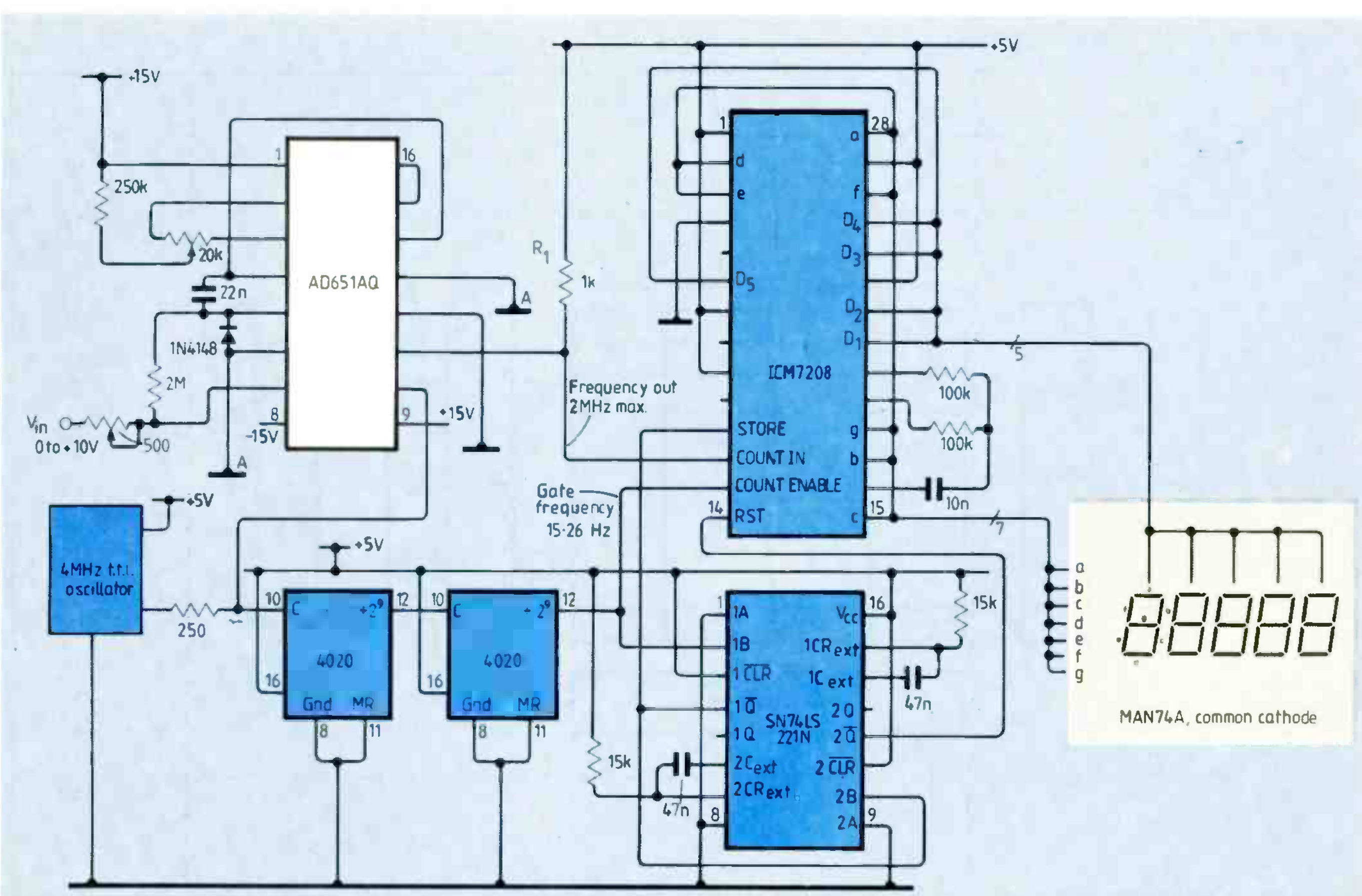
With pulse counting, though, the counter gating window is wide and remains constant for all input voltages. An alternative to pulse counting is pulse timing, in which an output pulse from the v-to-f converter gates a counter clocked by a higher frequency. This provides a much smaller window which varies depending on input voltage.

Analog Devices application note 'Analogue-to-digital conversion using voltage-to-frequency converters' describes how both period-counting and period-timing a-to-d converters are implemented. Besides this circuit for a complete 16-bit resolution converter with display, the note also presents a microprocessor-interfaced converter, and a discussion of gating-out interference signals. Examples of 8051 software for pulse counting and timing are given.

EWW 302 on reply card







VIDEO PALETTE FOR HIGH-RESOLUTION COLOUR GRAPHICS

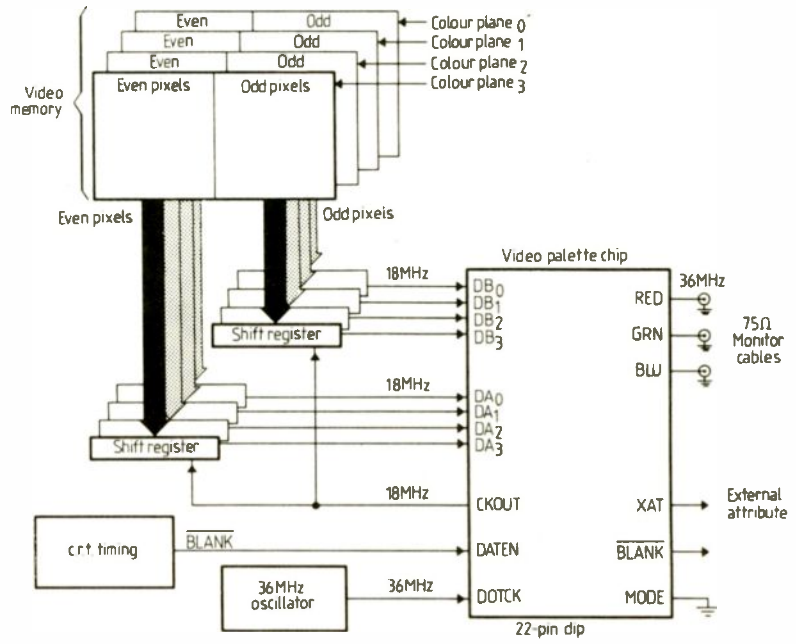
Separate analogue red, green and blue signals are produced from digital data by video palette i.cs. Using three 4-bit digital-to-analogue converters alone would allow one of 4096 colours to be produced for each pixel, but 12 data bits would be required for each dot.

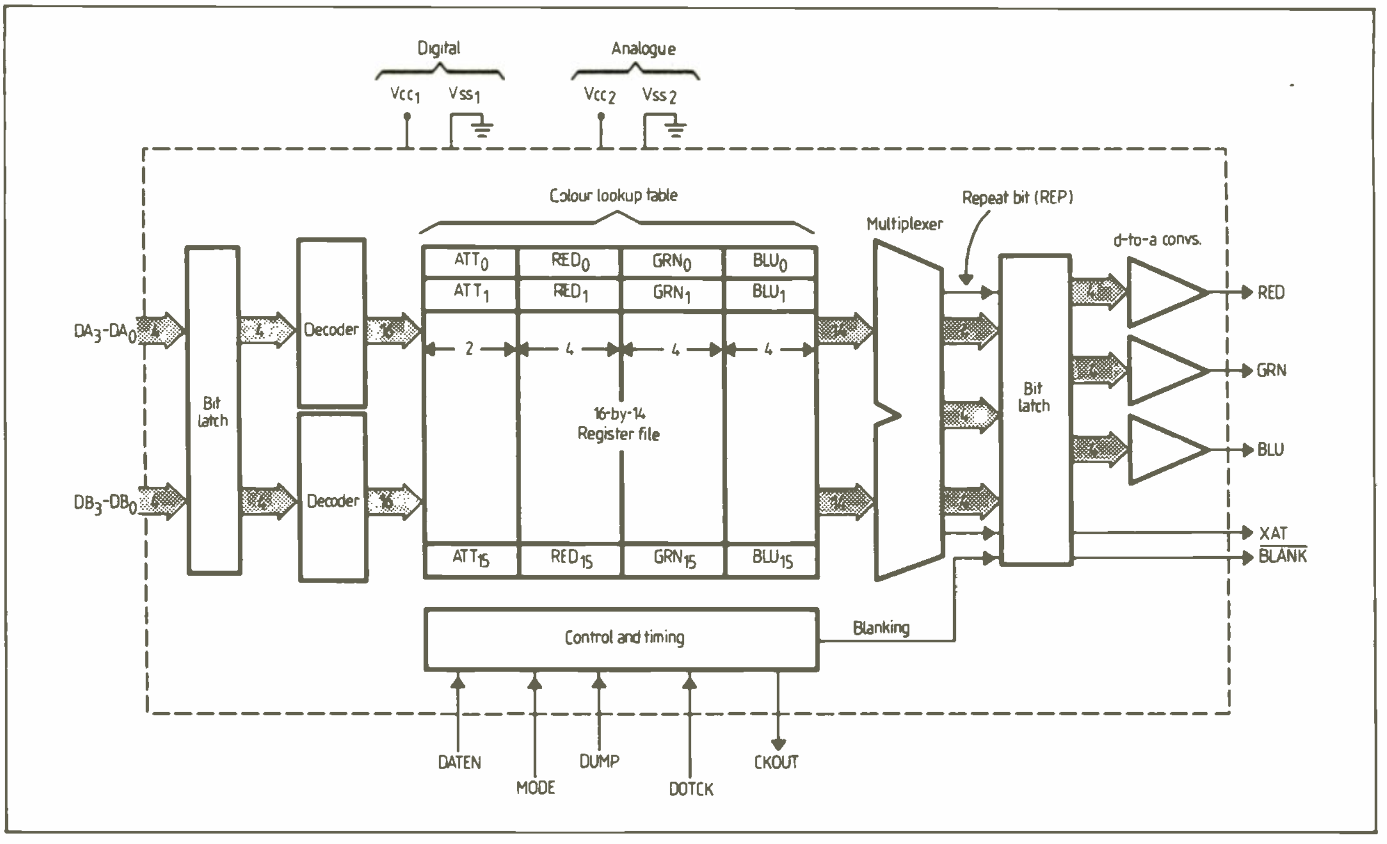
Video palette i.cs have three d-to-a converters, but they also include a colour look up table to reduce the number of colours, and hence memory requirement, to a reasonable level. In addition they incorporate control and timing circuits, as these diagrams from the Texas TMS34070 user guide show.

With the 34070 video palette, the colour look-up memory can be loaded with a new set of 16 colours from video memory at the start of each scan line or at the frame beginning. Loading can be done automatically which saves processing time. Look-up information is held within the palette i.c. in a 16-by-14 bit register file. The 16 rows represent the 16 possible colours and the 14 columns hold four reference bits for each of the three converters and two bits of attribute control. Four-bit pixel data presented to the chip selects one of the 16 rows.

Video memory for the palette is divided into up to four colour planes, which each present one of the four bits for each pixel. Dot frequency of the 34070 is up to 36MHz, which corresponds to a display resolution of about 800-by-600 pixels. To reduce memory speed requirements, the palette loads two four-bit segments at once from the even and odd pixel memories.

301 on reply card.





Computers, language and logic

We find it hard to convey in words the complex ideas an engineering drawing can express. Why then should we suppose language is the right medium for programming computers?

A. MEDES

Over the past four decades there has been considerable development in computing machinery. During this period it has come to be accepted that language and logic form the heart and soul of a computer's operations. We can converse with the computer in a proliferation of languages and courses entitled "digitable logic" are taught to electronic and computer science students.

Today there is even a computer language called Prolog (*Pro*gramming with *log*ic), which is touted as the most powerful computer language ever conceived, the language of the 21st century.

This is most unfortunate since the subjects of language and logic are quite literally trivial. They are by no means fundamental to a computer's operations and are in fact only superficial aspects of computing.

How dare I say this, you ask? Well, if we look to the roots of the word 'trivial' we find that it stems directly from the trivium. The trivium, in mediaeval (Graeco-Roman) learning, was the lower division of the seven liberal arts, consisting of grammar, rhetoric and logic (literally three-ways).

Scholars who wished to strut around convincing their fellows of things not necessarily true would have to study the trivium, which taught the formal rules of language and logic. The ground rules being laid down, scholars could then entertain themselves no end with their learned discourses.

But is this a sound basis upon which to build machines? That is, can we build truly effective machines if we restrict ourselves to a foundation of dubious wordplay? I think not.

Where, then, is there a better way? In the *quadrivium*, of course! The quadrivium was the higher division of the liberal arts and consisted of arithmetic, geometry, astronomy and music. The quadrivium was much stricter stuff than the trivium and involved learning about the workings of nature. It had to be studied in order to build useful machines.

LANGUAGE...

Why is it that the subjects of the quadrivium are more relevant to computing machines than those of the trivium? I shall try to explain by mentioning just a few of the many examples.

Let us consider language as a means of communicating information. It is often said that a picture is worth a thousand words. This is reasonable since language is essentially one-dimensional (in time) whereas a picture is two-dimensional (in space).

In engineering, where information must be conveyed in a complete, concise and efficient manner, the medium is the engineering drawing. That is, a two-dimensional picture, geometric in appearance. Several hundred years of practical experience have shown this to be the best method.

Before drawings were extensively used, and occasionally today, communication was via scale models. The models were three-dimensional (in space) and thus were even more effective than two-dimensional drawings. But 3-D models have the disadvantage that they cannot be folded flat and posted through the mail.

Incidentally, machines – including computers – exist in at least four dimensions. That is, three of space and one of time: they are solid and they move.

That drawings are a better medium of communication than language is easily proved. Just try to get an engineering subcontractor to fabricate a part of only moderate complexity by describing it solely with language, perhaps over the telephone. Small chance of getting it right first time!

If language were an adequate means of conveying detailed information, then the producers of this publication could save themselves a considerable sum of money by replacing circuit diagrams on these pages with linear parts lists and node lists. Although circuit diagrams may be no more accurate than the parts and node lists, they are certainly a lot easier to understand.

Instructors of computer programming say that the first step in programming a problem is to draw a flow-chart. This is because a two-dimensional and non-lingual flow-chart is easier to comprehend and modify than a linear linguistic description of a program. Only after the problem is solved in flow-chart form are we to encode it as a linear sequence of verbal instructions.

In arithmetic, and more generally in algebra, we find that communication is again, essentially two-dimensional. Consider the following simple algebraic form:

$$\frac{A+B}{C}+D$$

Translating into 'natural' language might give "A plus B all divided by C plus D". Retranslating might give

$$\frac{A+B}{C+D}$$

which is not the same!

This ambiguity in the linear verbal form has to be resolved in computer languages by giving arbitrary priorities to the various operators (which the programmer must remember) or by using lots of brackets to mark the extent of the operators.

"We can save ourselves frustration by realising that 'natural language' operating systems are no more than a gimmick."

The point is that although we can always describe something with a sufficiently long linear linguistic form, we can make life a lot easier for ourselves by using at least the extra dimension that is available on a sheet of paper. And there is no reason why computers can not interpret such a two-dimensional description.

...AND NO LANGUAGE

As a further example of how we might efficiently communicate our desires to a machine, imagine the following scene.

You climb into your latest model IBM p.c. (personal car). In front of the ergonomically-designed seat you find a high-resolution v.d.u. and slimline 96-key Selectric-style keyboard. There is no windscreen since all the information you will require will be instantly available at the v.d.u.

You decide to go for a test drive. (Your input is shown lower case, the computer output upper case).

```
>motor mode=on
MOTOR=ON:RPM=852:OILPRESS=NORM:TEMP=LOW
>engage gear=1:indicate=r:disengage brake/park
RPM=736:SPEED=2.37MPH:STEER=R3.8DEG
>accelerate=.12g:steer=r5deg
RPM=1528:SPEED=14.33MPH:OBSTACLE AT 18.4FT/BEARING=L9.1DEG
>decelerate=.4g:steer=r..............
```

"Damn, the system's crashed...", you say; "...oh well, think of the time I'm saving using this marvellous new technology called the automobile."

In reality we communicate our desires to the automobile by pulling and pushing on a few levers. Not only is this positioning of levers in space a precise, reliable and rapid means of communication, but it is also quite effortless. We can talk, listen to the radio, and think about the weekend whilst simultaneously changing gears, negotiating a bend and avoiding pedestrians.

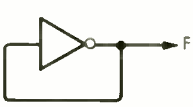
Fortunately non-linguistic means of communicating with computers are slowly emerging: namely, the mouse/icon-driven operating systems of some p.cs, and to a lesser extent Xerox's Smalltalk programming environment. Languages such as Prolog, however, are a retrograde step, especially for the study of something as non-trivial as artificial intelligence.

LOGIC

Now for logic – today called Boolean logic or the predicate calculus. Just as language is inadequate for detailed communication then so too is logic an incomplete calculus. As an illustration of why logic still resides in the trivium and not the quadrivium I offer the following.

Some twenty five centuries ago Epimenides, who was a Cretan, said "all Cretans are liars". Ever since then, logicians and philosophers have had a marvellous time arguing whether self-referential paradoxes of this type are true, false or meaningless. Whitehead and Russell's Principia Mathematica is a classic example of how to spend eighty or so pages arguing the point in order to develop a theory that is simply not necessary.

Restating Epimenides' words slightly more explicitly we can say "the truth value of this statement is falsehood". Just as other more sensible logical assertions and premisses can be formed from logical elements, in silicon if required, so too can the above statement. It is simply



The logical gate is an inverter (i.e. not) and the basic circuit as a whole, which is quite common in electronics, is a ring oscillator. The condition of the output function F cannot rightly be said to be true, false or meaningless (1, 0 or X) as in fact it oscillates. Just as Epimenides' statement appears to do.

Now if a logical state that oscillates between true and false appears to be nonsense then consider that there is a remarkable analogy between the oscillating logical state and the arithmetical value *i* or the square root of minus one (for further reading on this analogy, and much more, I recommended "Laws of Form" by G. Spencer-Brown).

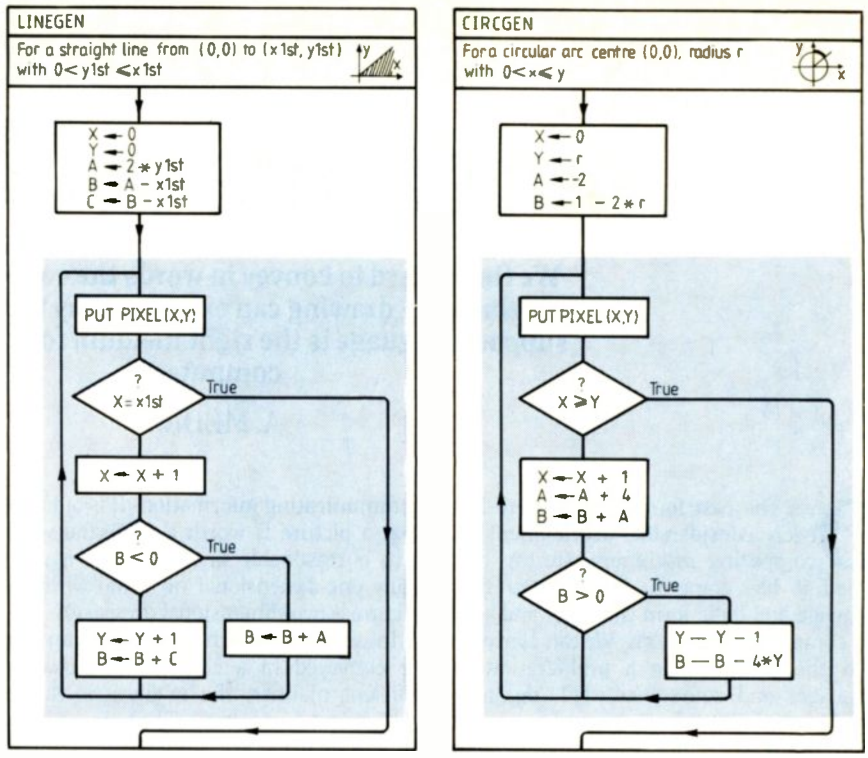
The analogy goes like this:

In the trivium

1. We consider statements that can be true (T), false (F) or meaningless.
2. We consider the statement "This statement is false."
3. Rearrange (letting s = the word "statement", and S = everything between the quotation marks)

   S = not(s)
4. The statement is asserting something and so is not meaningless.
5. Try s = T → S = not(T) = F (which is wrong since s refers to and is supposed to be the same as S).

   Try s = F → S = not(F) = T (which is also wrong).
6. We invent a rule disallowing us to consider statements of the above type.
7. We stop.



Computer programming in two dimensions: flow-charts explain the routines more efficiently than a one-dimensional flow of language could.

In the quadrivium

1. We consider numbers that can be positive, negative or zero.
2. We consider the equation $x^2 + 1 = 0$
3. Rearrange: $x = -1/x$
4. For the equation to balance x must be a form of unity.
5. Try $x = +1 \rightarrow +1 = -1/+1 = -1$ (wrong)

   Try $x = -1 \rightarrow -1 = -1/-1 = +1$ (wrong)
6. We consider a form of unity (call it *i*) that equals the square root of minus one and so satisfies our equation.
7. We develop various tools to manipulate this new number and go on to build bigger bridges, power stations, television, etc.

FLIP-FLOPS AND PARADOXES

The situation today is similar to the situation two hundred years ago when engineers were manipulating the square roots of negative numbers even though those numbers were not formally acknowledged by the mathematical community. Today's engineers are quite happy to design and use D-type flip-flops even though these and other edge-triggered devices are built on exactly the logical paradox illustrated above. Likewise, devices such as UK flip-flops and memory elements that use feedback paths are beyond the comprehension of logic.

So, although the calculus of logic can be used to describe some simple circuits, namely those of the first degree (with no feedback), it is totally inadequate if we require a rigorous mathematical description of other types of computer circuit – namely those of degree higher than the first.

The acceptance and use of complex numbers (those that include $\sqrt{-1}$) allows us to design reliably much of the machinery that surrounds us today. Without complex numbers the design process is either severely restricted, through rules which disallow us certain options, or expensive since the only way foward is via trial and error.

I believe that if we develop the mathematical tools with which we can manipulate higher-degree forms of circuitry, then we will gain a better understanding of how different configurations of computers might be made to work. This understanding will in turn enable us to build more powerful computing machines, confident that the machines will work as intended.

We can also save ourselves further frustration in programming these new machines by realizing that 'natural language' operating systems are no more than a clever but superficial gimmick.

At best, natural language systems will allow the office manager to use the office computer (which admittedly will be good for sales). But they will never be capable of effectively communicating the detailed in-

Continued on page 224.

Laser-diode power supply

This low-noise, spike-free laboratory supply stabilizes either laser current or optical output power. Amplitude modulation can be applied.

J. VANDEWEGE, H. PEREMANS AND J. SCHOTTE

Until recently the only low-cost semiconductor laser diodes were single heterostructure gallium arsenide or GaAs/GaA1As diodes. These are rather simple components with so high a threshold current (the current at which laser action starts) that at room temperature, only low duty-cycle pulsed excitation is possible (e.g. RCA SG2000 series, Laser Diode LD60 series, ITT LA series.) Their main application is in time-domain range finding, an optical equivalent of pulse radar.

Continuous-wave semiconductor laser diodes are much more advanced devices in which the electromagnetic field created by the drive current and by the light it excites is confined to a very narrow region of the semiconductor crystal. This makes the laser action start at a much lower drive current level, so that continuous operation is possible without excessive dissipation.

Owing to their complexity and the advanced fabrication technology required, c.w. laser diodes were once confined to applications such as broadband optical fibre networks, where an individual diode is cheap by comparison with the surrounding network. But today, laser diodes for use in compact disc players sell at a very reasonable price – either alone or, for about £50, as replacement CD head units complete with collimating optics and tracking photodiodes.

But c.w. semiconductor laser diodes require a very reliable power supply. They operate at extremely high internal field strengths, where a picosecond spike of current can damage the delicate semiconductor by generating crystal defects or by multiplying existing imperfections. A number of such spikes, or a power supply switching transient, can turn a laser diode into a side-emitting led, if any light emission is left at all. But with a properly-designed supply and with device-handling precautions adopted from c-mos practice, you can have a c.w. laser system up and running for several hundreds of hours without any noticeable laser degradation.

LASER BASICS

Figure 1 shows a laser diode chip in its package. The chip has been cleaved to a small block and two opposite cleaving facets act as laser mirrors, reflecting most of the light back into the laser chip. Inside the package, a silicon photodiode is placed so as to collect the light emitted by the laser's rear facet. Photocurrent from this diode can be used to stabilize the operating point.

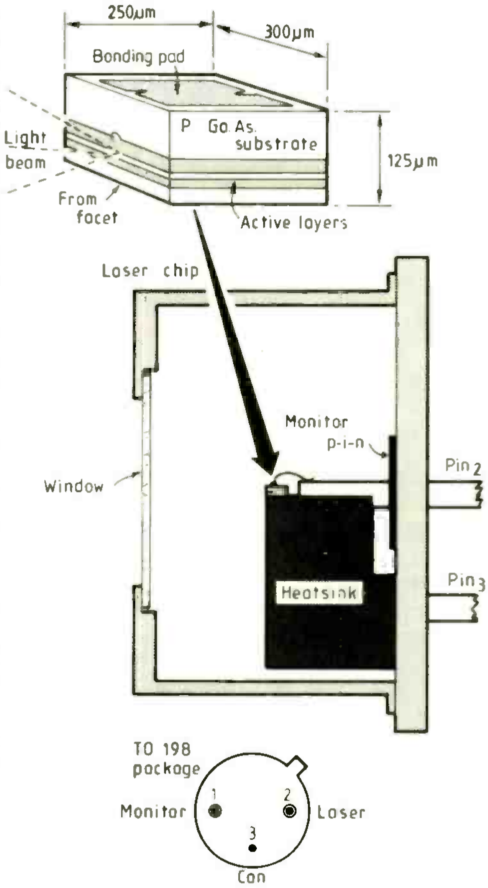


Fig.1. Cross section of a TO-148 solid-state laser package with monitor p-i-n diode. Detail: A Sharp LT022MC laser chip is mounted on the package heatsink with its active layers down for efficient heat transfer.

For the Sharp LT022MC found in most compact disc players (Fig.2), the cathodes of both laser and photodiode are connected to the metal package. Other laser diodes can be used as long as these cathodes are connected in common. No modifications of the supply circuit is needed to allow for optical power stabilization.

Abridged specification of the LT022MC are given in Table 1. The absolute maximum ratings impose limits on reverse voltage, temperature (and so dissipation) and optical output power.

The optical specifications include the 50% beam divergence angles for two reference planes. A laser diode does not produce the highly collimated, high coherent beam given by a typical gas laser. Like a cheap torch, it radiates light across the wide angle; the coherence length is of the order of a millimetre. For most applications which require a collimated beam, the optics of a commercial CD laser head are adequate.

Table 1. Electrical and optical specifications of the Sharp LT022MC (from the manufacturer's Laser Diode User's Manual, reference number HT482D).

Absolute maximum ratings:
Optical output power (P_o): 5mW
Reverse voltage (V_r) – laser: 2V
– p-i-n diode: 30V
Operating temperature (T_{opr}): –10 to +60°C

Operating characteristics
Threshold current (I_{th}): 50mA typ., 80mA max.
Operating current at P_o=3mW:
at room temperature, I_{op}=65mA typ., 100mA max.
at 60°C, I_{op}=110 mA max.
Wavelength at P_o=3mW, single transversal mode: 770nm min., 780nm typ., 790nm max.
Monitor current at P_o=3mW: 0.3mA min., 0.9mA typ., 1.6mA max.
Angles of 50% radiation intensity at P_o=3mW:
parallel to the junction, 8.5° min., 11° typ., 16° max.
perpendicular to the junction, 20° min, 33° typ., 45° max.
Differential efficiency at P_o=2mW:
0.1mW/mA min., 0.25mW/mA typ., 0.6mW/mA max.
Heat resistance:
20°C/W min., 35°C/W typ., 70°C/W max.

Figure 3 shows a Sharp LT022MC assembled into a Philips CD100 replacement laser head. This unit produces a well-collimated infra-red beam of up to 0.5mW and about 5mm diameter. It also contains a beam-splitting prism which directs light reflected from the disc towards a dual-slit silicon detector array located in the dil packages. Details were given in J.R. Walkinson's article, *Wireless World* April 1985, pages 44-46.

The current-to-light transfer characteristics of the laser is given in Fig.5 for three different temperatures. Below the threshold current I_{th}, the internal field strength is too low to start the lasing action and the diode acts as a led. A dim red spot can be observed on the front facet. The exact value of I_{th} varies with chip temperature and time, but is typically 50 and at most 80mA.

The only way to discover the operating point of the laser electrically is by observing the monitor diode's photocurrent. When the drive current exceeds I_{th}, lasing starts and optical output power increases sharply. The differential efficiency is defined as the ratio of increase in optical power to the corresponding increase in drive current. It is typically 0.25mW/mA and is fairly constant for a given laser at various drive current levels, which indicates good modulation linearity.

OPERATION

The instrument (Fig.6) has two operating modes: constant laser drive current or constant optical power. The first can be used to check the laser characteristic or to drive a laser which has no monitor diode. It works basically as a very clean variable current source with a large and accurate setting range – 100μA to 250mA, set by a 10-turn precision potentiometer. In the second mode, the monitor photocurrent is used to stabilize the optical output of the laser by feedback. In either mode a current limit can be set to protect the laser.

The large setting range is obtained by feeding a constant reference current (current mode), or the monitor p-i-n photocurrent through a variable-gain current mirror A before sending it to the laser current source B.

A three-digit display indicates laser current or optical power. For the latter a calibration resistance is needed in the laser plug to cope with variation from one diode to another.

The instrument is doubly isolated. It provides active protection against mains failure and on/off switching transients, and against mishandling such as pulling out the laser plug when the laser is on.

CIRCUIT DESIGN

Many of the time-constants of the circuit are critical and so no attempt should be made to modify it unless its transient behaviour can be thoroughly tested with high speed signal-storage equipment.

The analogue regulator section is shown in Fig.7. The op-amp is part of a dual open-collector op-amp i.c. TAE2453. Earlier designs using both op-amps did not meet the transient suppression requirements and so the second is not used. The op-amp and Tr_4 form a current source feeding the laser. Resistor R_6 limits the maximum current this can supply to 250mA. The variable current limit (determined by R_7) can be raised somewhat above laser threshold; but in normal operation the laser current is lower by a value proportional to the collector current of Tr_3.

Resistor network R_{10}-R_{10}' is a precision 0.1Ω network. The voltage drop it causes can be measured with a 0-999mV panel meter, which monitors the laser current in two ranges chosen by S_2 (Fig.7). The choke (10 turns on a Siemens ring core B64290-K37-X830) and capacitors C_3 (a tantalum electrolytic), C_4 (ceramic) form a low-pass filter to protect against transients.

The meter can also indicate the photocurrent voltage drop across R_{cal} (S_3) which is a measure of the rear-facet optical output power. This resistor has been located in the five-pin DIN laser connector. When a calibrated optical photometer is available, R_{cal} can be adjusted so as to give a direct front-facet power reading in microwatts, for a given laser diode or for a complete laser head. This calibration should be done near the normal point of the laser (e.g. 1-3 mW), as the optical front/rear facet power ratio depends on drive level.

SAFETY PRECAUTIONS

The compact disc laser diode used is a GaAlAs type emitting at 780nm wavelength. At this near infra-red wavelength the human retina is very insensitive; but the eye lens remains transparent and so laser light could reach the retina and damage it without one's being aware of it. When this laser is without lenses, it can be observed safely from some 10cm away or more because of divergence of the beam. However, when collimating optics of a microscope are used, take care not to concentrate the full laser power into the eye. A safe method of working, which also permits observation of the near infra-red radiation, is to use a vidicon camera. Most silicon vidicons and ordinary camera lenses are suitable; a macro zoom objective is fine for close observations.

Fig.2. A Sharp LT022MC GaAlAs laser diode package. This relatively low-cost device is found in many compact disc players.

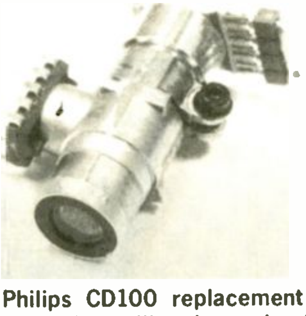


Fig.3. Philips CD100 replacement laser head, containing collimating optics, beam-splitting prism and dual-shift reflected light silicon photodetector.

Fig.4. Philips laser head dismantled to show the beam-splitting prism.

Transistors Tr_1-Tr_3 form a variable-gain current mirror to change the polarity and level of the current from the reversed-biased monitor photo diode. Its current transfer ratio is set by the 10-turn potentiometer. In optical feedback mode, it is fed with the monitor photocurrent through S_1. In constant-current mode, R_8 supplies it with a fixed current.

Several elements have been added to protect the laser. A relay controlled by the logic circuit of Fig.8 shunts the laser connections in dangerous circumstances – such as at switch-on, when mains power is off or interrupted, when no laser is plugged in, or when no 'laser free' command has been given by toggling S_4.

The fet is a BSS89 (Siemens) with a very low on-resistance; it controls the current source. Overall timing is critical for obtaining correct switching. The sequences (Fig.9) are as follows:

Switch-on: after mains-on and setting of the laser drive level –

T_0: output free instruction given

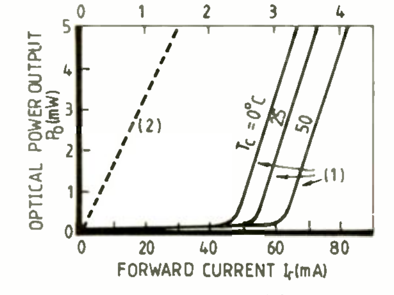


Fig.5. Optical power output (1) and monitor current (2) of an LT022MC laser diode plotted against forward current.

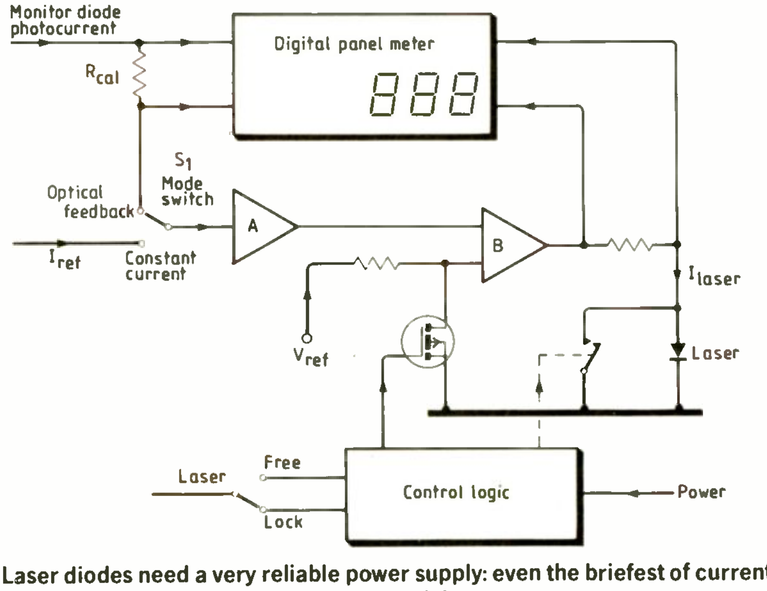


Fig.6. Laser diodes need a very reliable power supply: even the briefest of current spikes may damage the delicate semiconductor material.

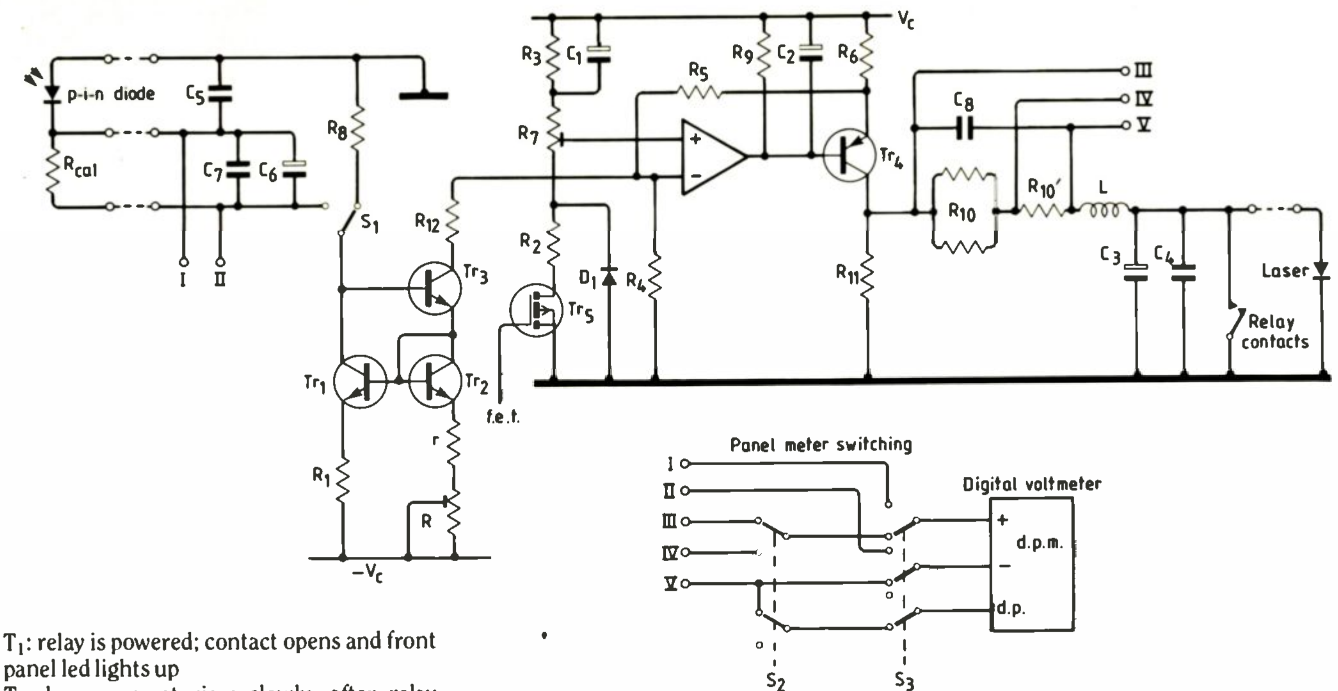


Fig.7. Analogue current regulator, showing the variable-gain current mirror Tr_1-Tr_3, the laser current source (op-amp and Tr_4) and switching for the digital panel meter.

T_1: relay is powered; contact opens and front panel led lights up

T_2: laser current rises slowly, after relay contact bounce has died out (50ms), powering the laser gently after about 250ms.

Switch off: T_3: output lock instruction given; laser current falls to zero within 5ms in a well-controlled manner

T_4: relay contact closes.

The time constant R_{13}/C_9 controls the relay's switching delay. The slow rise of laser current is timed by R_3/C_1. When the 'output lock' command is given, Tr_5 is blocked and the op-amp saturates immediately so that R_3/C_1 has no effect. The falling laser current is controlled by R_9/C_2.

TESTING

If no tv camera or infra-red power meter is available, a large-area silicon photodiode or a solar cell can be used for checking the laser output. Most silicon detectors produce a short-circuit current of about 0.55A per watt of optical power at 780nm wavelength. If possible, set the laser power at a modest 0.5mW (or around 0.2mW for a CD laser head) for long life.

For critical applications the modulation linearity can be checked with a high speed avalanche photodetector connected to a spectrum analyser. Keep the light level on the a.p.d. low to avoid generating harmonics at the detector. Very high quality amplitude modulation of the laser output is possible, with low sideband levels and with very little noise added by the modulation process.

Dr Jan Vandewege is a research leader at Ghent University's electromagnetism and acoustics laboratory, with interests in s.a.w. design, general r.f. instrumentation and optoelectronics. H. Peremans and J. Schotte developed the instrument presented here as part of their final year B.Sc. project.

A component list, p.c.b. layout and constructional information are available from the *Electronics & Wireless World* editorial office at Quadrant House in return for an A4-size, stamped addressed envelope. Mark your covering envelope 'Laser supply'.

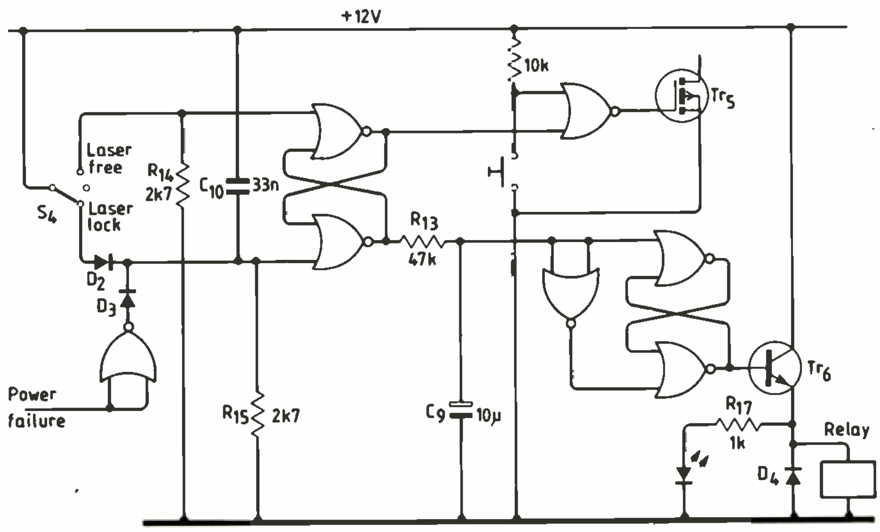


Fig.8. Control logic. This ensures the correct switch-on/switch-off sequences required for safe operation of the laser.

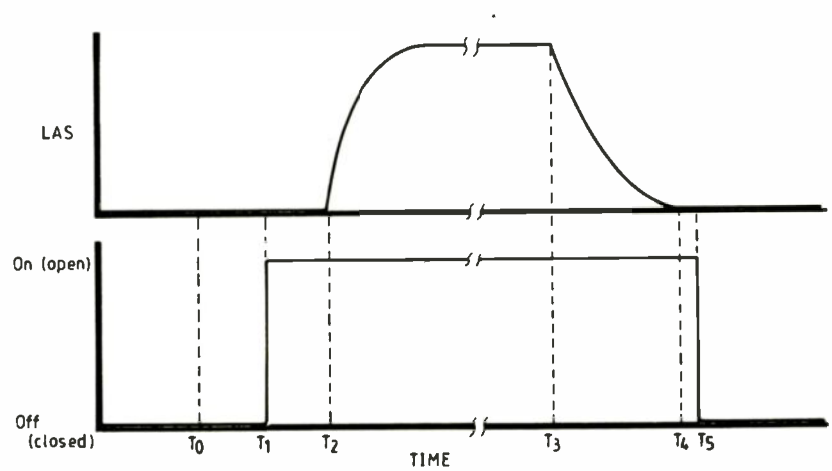


Fig.9. Switch-on/switch-off sequences. Scale of the sequence: T_0-T_2 scale is compressed (slow); T_3-T_5 is expanded (fast).

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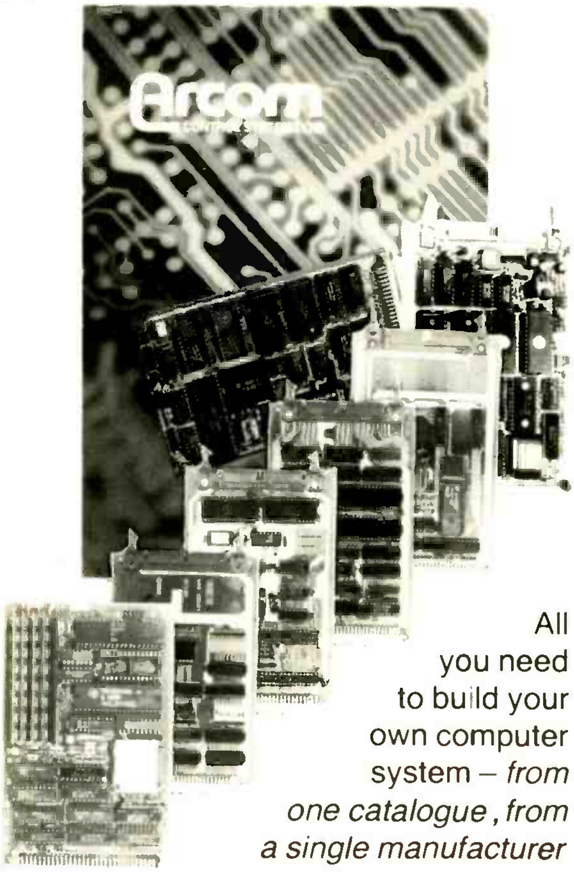

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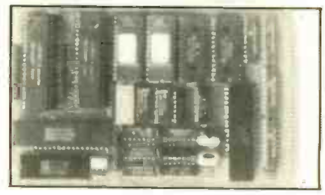

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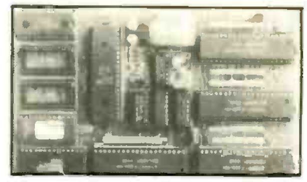

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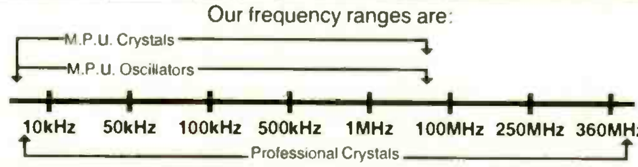

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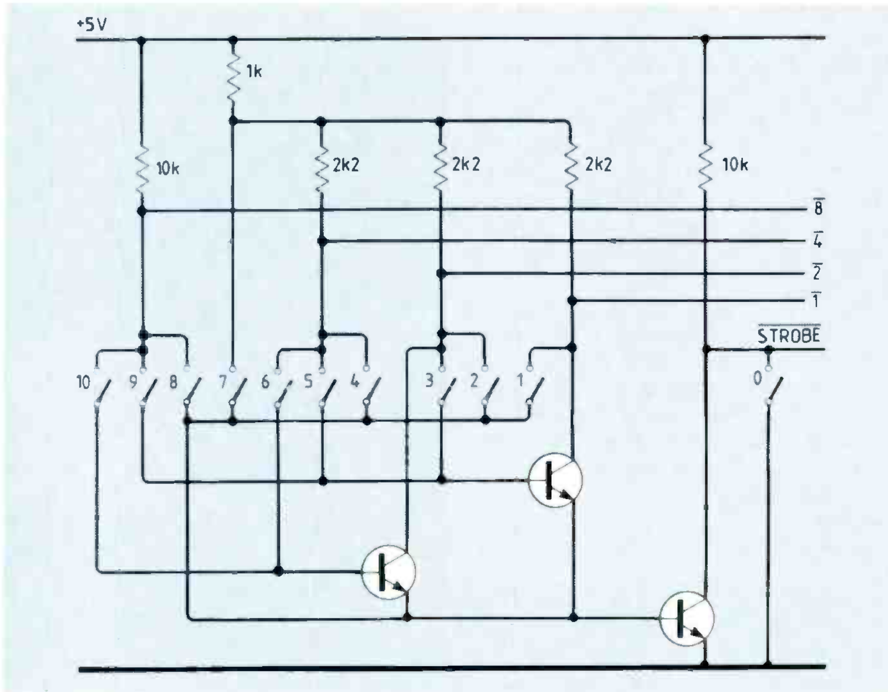


Phase angle-averager

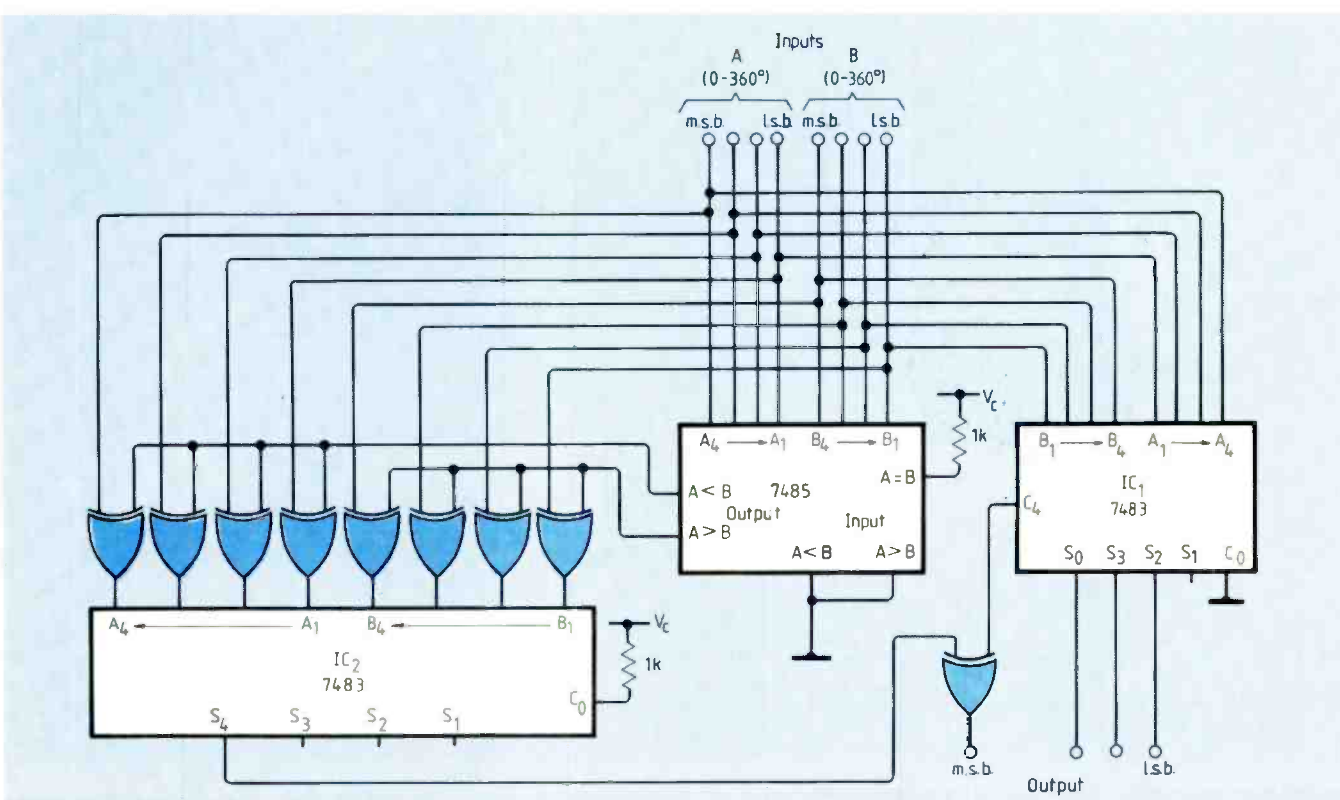
Phase averaging is different from arithmetic averaging in that the phase average of 350° and 10° is 0° for example and the arithmetic average is 180°. However in the case of angles 170° and 190°, both phase and arithmetic averages are 180°.

It is possible to find the phase average from the arithmetic average by working out the arithmetic average of the phase angles, then the absolute value of phase difference between them. If the difference is equal to or greater than 180°, 180° is added to the arithmetic average to obtain the phase average. When the difference is less than 180° the arithmetic average is the phase average.

In the circuit, the adder calculates the arithmetic average (A+B)/2. Values A and B are compared and to obtain the absolute phase difference |A-B|, the larger angle is added to the two's complemented value of the smaller angle.

A logic one in the m.s.b. of |A-B| indicates that phase difference is greater than 180° so this bit is used for complementing the m.s.b. of the arithmetic average, which is the same as adding 180° to it. In this way, the phase average is obtained.

A. Dhurkadas
Indian Institute of Technology
New Delhi
India



Synthesized oscillator

No preset adjustments are required for this synthesized oscillator covering 100Hz to 19.9kHz. Amplitude remains within ±0.1dB and t.h.d. at 1kHz is 0.2%.

The audio signal is produced by a crystal-derived pure sinewave of 102.4kHz. This sinewave modulates the p.l.l. generated signal, the reference signal of which is derived from the same crystal as the 102.4kHz signal. Component IC_1 is a fifth-order elliptic filter.

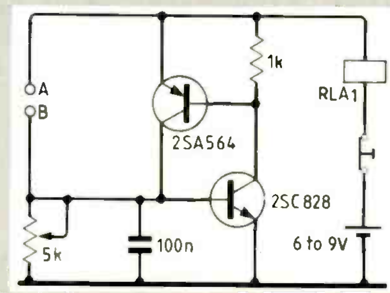
Since linear input on pin 1 of the 1596 modulator/demodulator is the fixed-frequency sinewave, output voltage is constant for all frequencies and the critical filtering can be done at one frequency, IC_1. Component IC_3 is a third-order elliptic filter which removes unwanted frequency products above 20kHz.

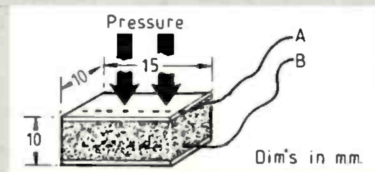
J.R. Page,
London W3

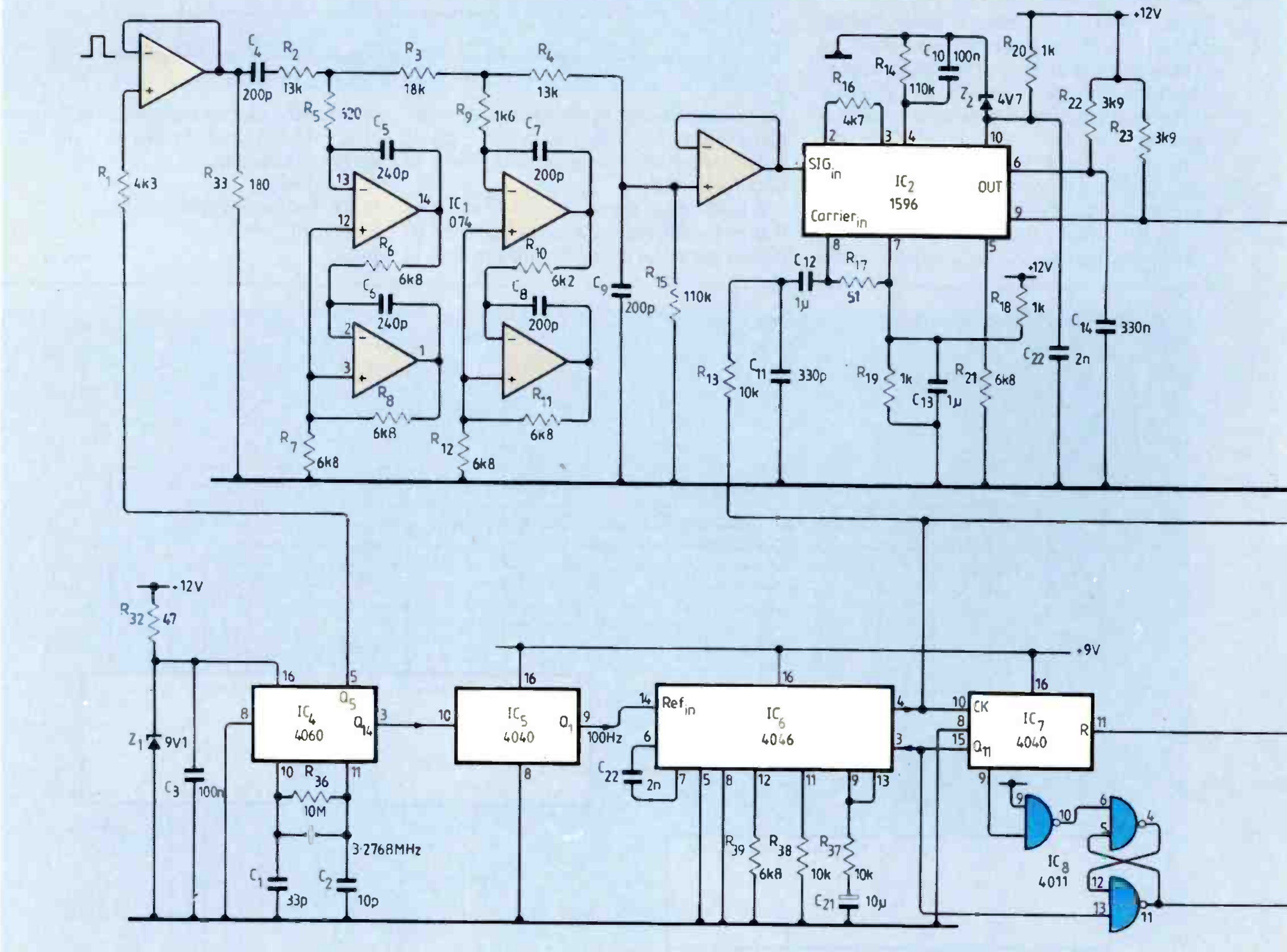
Conductive foam senses pressure

Conductive foam used to protect mos i.cs from electrostatic discharge can also be used as a pressure sensor. The circuit, part of a burglar alarm, latches when the sensor is pressed.

Amir Ali Khan
Lahore
Pakistan







CIRCUIT IDEAS

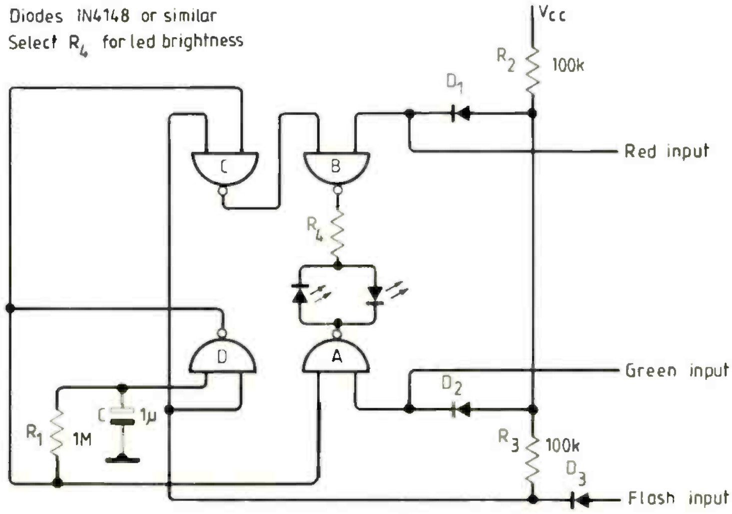
Simple multistate indicator

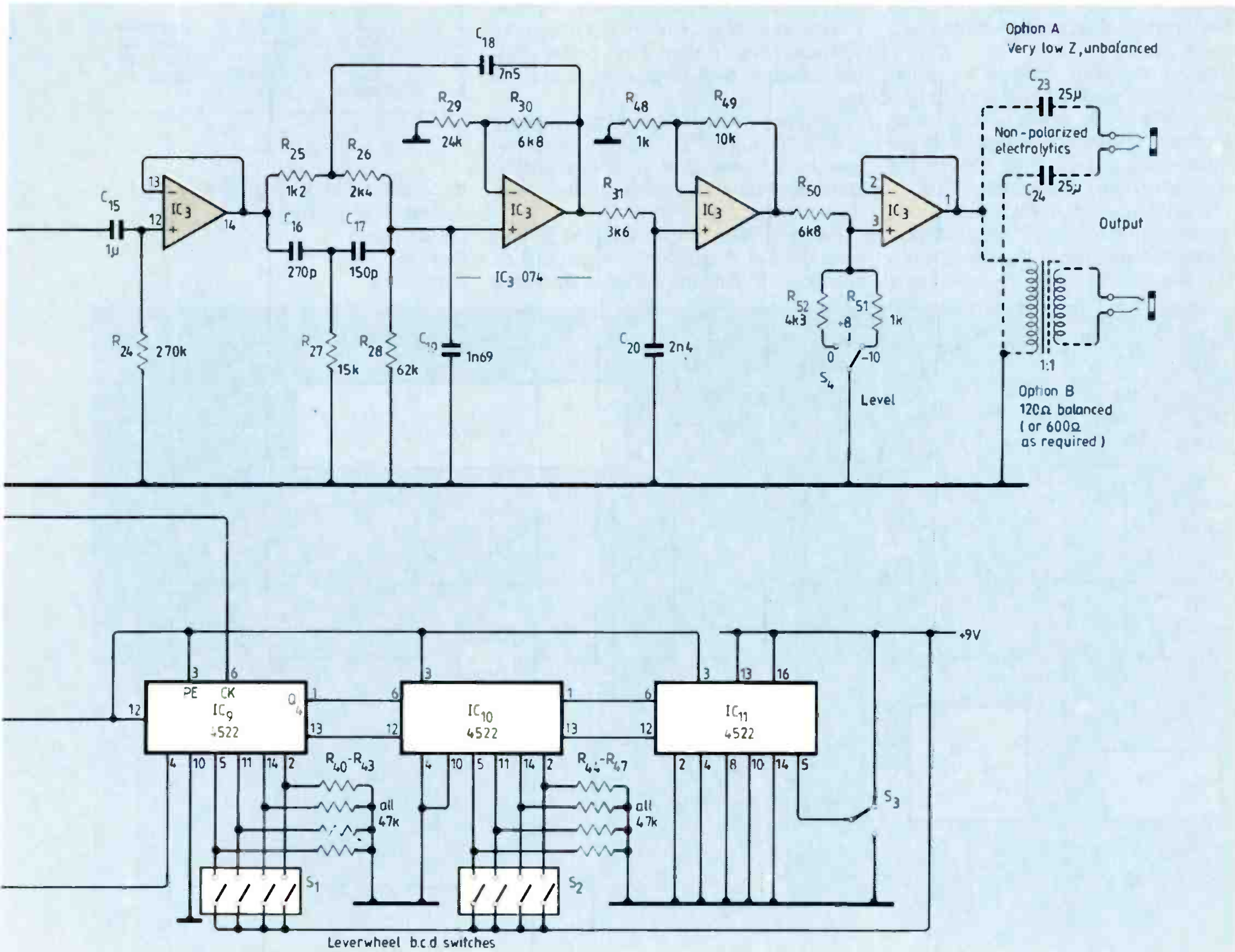
A convenient four-state indicator may be made from a two-colour led and a simple c-mos logic chip. When both inputs are low the led is off, if one is high the led is red, if the other is high the led is green, and if both are high the led flashes red and green.

This operation applies when R_3 and D_3 are left out or the flash input is low. When R_3 and the diodes are excluded or the flash input is high, flashing occurs in all three led-on states. When R_3 is not used, direct connection is required from R_2 and $D_{1,2}$ to gates C and D; resistor R_3 is short-circuited, not open.

With low supply voltages, a 74HC132 will be more suitable but note that the pin-out is different and that R_4 is essential to limit current.

James M. Bryant
Cheltenham, Gloucestershire.





CIRCUIT IDEAS

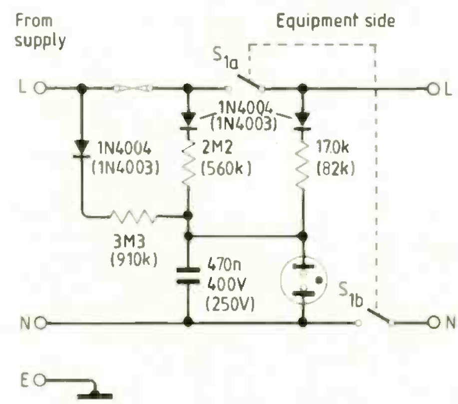
SINEWAVES WITH FAST AMPLITUDE STABILIZATION

A 6.2V reference voltage is required for this circuit on page 36 of the November issue. The author suggests using a 1N821 temperature-compensated diode.

Fuse monitor indicates three states

Under normal conditions with the switch closed, the neon lamp in this fuse-condition indicator glows constantly. When the switch is opened, the lamp flashes rapidly warning that mains voltage is still connected. Warning of a blown fuse is given by the lamp flashing slowly. In this case, the capacitor is only charged through the left-hand resistor.

R.B. Hughes
Powys
Wales



Musical instrument tuner

During performances, aural instrument tuning can be impossible. Using a meter and electronic frequency division, this small battery-operated device makes tuning simple and accurate.

Although originally designed for guitar tuning, the unit can also be used to tune bass guitars, since it also works with notes an octave lower, and other instruments. Input is an electrical signal either directly from the instrument or from a microphone.

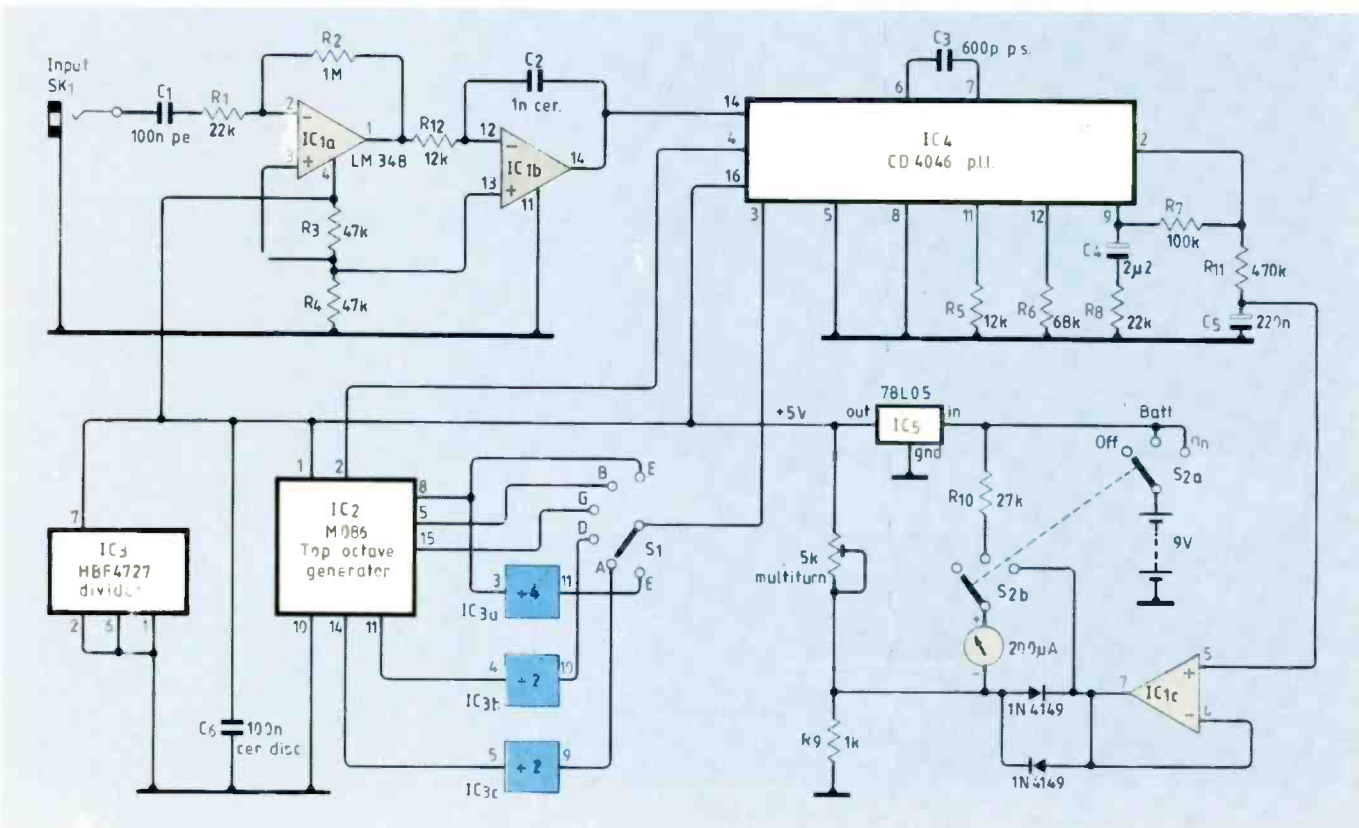
It is best to select the most mellow sound for tuning. With a guitar, this is normally produced by switching to the most central pickup and picking the string towards its centre. The meter should adopt some steady value for most of the note duration, indicating pitch accuracy. Flat notes are indicated when the needle is on the left and sharp ones when the needle is right. From centre scale, full deflection is about plus and minus one tone.

Temperature tests showed a frequency drift of 200 p.p.m./°C from room temperature to 75°, but drift is determined by component stability. I noticed no long-term frequency drift.

For calibration, I used a tuning fork to tune the top E string of my guitar then connected the guitar to the tuner. By setting the switch and plucking the string gently, the meter can be zeroed.

David Greaves
Romsey
Hampshire.

Note	Division ratio	Frequency (Hz)	Error relative to top E
E	239	329.5	0
B	319	246.9	0.000 084
G	402	196.0	0.000 128
D	536	147.0	0.001 002
A	716	110.00	0.000 266
E	956	82.375	0



Microprocessors: design for test

Today's v.l.s.i. devices are so complex that testability needs to be built in right from the start. Mike Catherwood of Motorola explains his company's approach.

M.I. CATHERWOOD

As more functionality is squeezed on to today's v.l.s.i. devices, ever more efficient test strategies are needed by semiconductor manufacturers as they battle to keep test times within commercially viable limits. The traditional approaches, often referred to as functional testing, in which the device under test contributes little or nothing to its own testability, are often inadequate for volume testing of v.l.s.i. components.

However, many limitations of functional testing can be minimized or removed altogether through the addition of on-chip test features such as device partitioning and built-in self-test.

A significant drawback of incorporating structured testability techniques in a design is that they invariably require part of the device to be dedicated to test purposes only. Although a good scheme will take full advantage of any inherent modularity and existing design structures in the device (e.g. bus orientation, registers etc.), it will take additional time to develop, design and simulate and will almost invariably demand silicon area. On the other hand, moving some of the burden away from the tester and placing it within the device under test will simplify the resulting test program and can substantially reduce the engineering effort required to develop it. The test program will be smaller and more modular, which should also make it easier to manage.

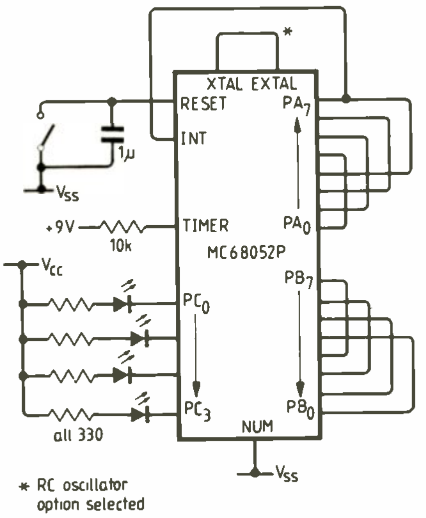
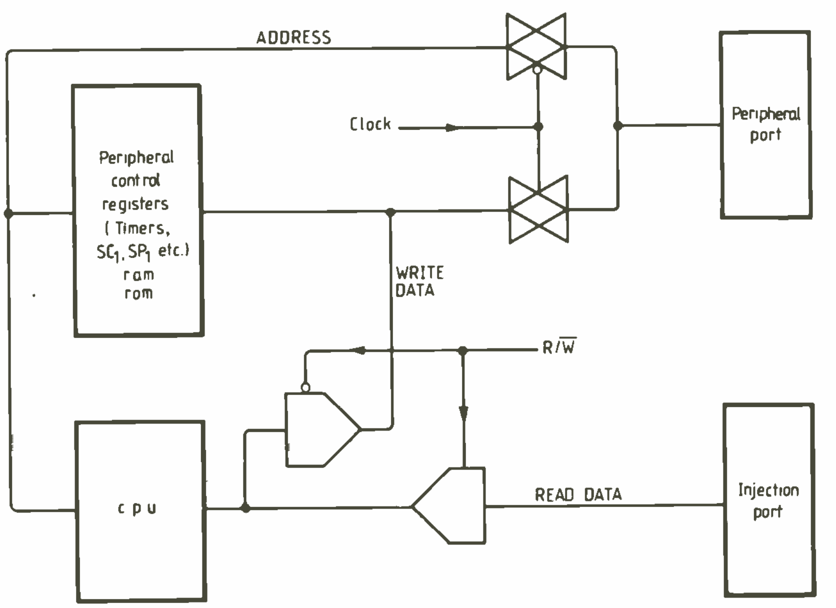


Fig.2. Self-test arrangement for one of Motorola's rom-based microcontrollers. Test mode forces the device to use alternative reset and interrupt vectors.

Some of the techniques applied in a structured testing scheme may also produce a known fault coverage. This can form a useful contribution towards the reduction of test grading expenditure.

Fig. 1. Typical non-user mode test configuration.



Improved testability and better fault coverage are benefits of structured testing that can be difficult to assess accurately in financial terms. For example, by offering the opportunity to *create* – not just pay lip service to – an overall test philosophy early in the design process, the structured approach can make for a highly testable device with built-in quality. It is unfortunate that the advantages of built-in testability are harder to quantify than the obvious savings in silicon area if you don't bother!

We now examine four concepts associated with structured testability and discuss the benefits afforded by each: partitioning, signature analysis, test microcode and built-in test software. This list is by no means exhaustive; however, these techniques have been successfully applied in the practical examples which follow.

PARTITIONING

Partitioning is one of the most fundamental aspects of device architecture design in creating a structured test environment.

When in test mode, the device is split into separate functional blocks by on-chip logic (e.g. data selectors and multiplexers). Internal bus structures (it is assumed that the device is modular in design) are used whenever possible – for example, to route internal signals to and from the external pins. The tester can thereby gain independent access to areas of the device which would otherwise have been impossible to see directly. This technique can substantially improve the controllability of individual modules within a device.

An alternative approach is to partition through the judicious placement of on-chip test pattern generators and/or signature analysis registers, which bring us to our next concept.

SIGNATURE ANALYSIS

Signature analysis uses data compression to accumulate large amounts of test result data and to create a unique – but very much smaller – 'signature'. Data compression using linear feedback shift registers (l.f.s.r.) configured to implement the CCITT cyclic redundancy check polynomial, is well known[1] and extensively used for error-detection in data communication systems.

L.f.s.rs are used predominantly in serial data transfer applications. However, it is possible to configure them as multiple-input signature registers for the accumulation of parallel data. In the examples discussed later, on-chip c.r.c. code generators based on 16-bit l.f.s.rs, are incorporated into the partitioning scheme to compress the test result data generated by a particular block. The 16-bit signature register is subsequently read by the tester and compared with the (known) signature that would be generated by a fault-free block.

The addition of an on-chip test pattern generator forms a test structure often referred to as a built-in logic block observer or Bilbo. A pseudo-random binary sequence generator using another l.f.s.r or some form of built-in test software are both examples.

It has been shown[2] that a signature register of length n bits, with appropriate feedback paths, can have a probability of successfully catching more than $100(1-1/(2^{n-1}))\%$ of all detectable errors that can occur during compression of, for example, a test result sequence less than (2^n-1) entries long. This is equivalent to 99.9969% for a 16-bit signature register.

Signature analysis often produces elegant solutions to difficult test configuration problems. For example, architectural limitations may make some nodes in a device difficult to reach. A carefully-positioned signature register may remove this problem. A further difficulty might be that testing at full speed is impracticable, perhaps through tester or pin-out restrictions. An on-chip self-test scheme incorporating signature analysis could provide the answer. This solution may be developed to allow other test activity to be performed at the same time as the on-chip test thereby improving the efficiency of the test program.

TEST MICROCODE

Incorporating test microcode into a (microcoded) microprocessor design can form the basis of an elegant approach to test management. For example, it may be used to activate partitioning logic in a device under test or reveal hidden registers and so on to the tester. Additional test microcode might then comprise test sequences which would be executed, in the partitioned device, concurrently with other tester activity. The test microcode may also be configured to use data passed to it from the tester.

Essentially, test microcode forms a logical bridge between the structured design concepts inherent in a microcoded machine, and structured testing. Its usefulness is limited only by the machine's architecture and the designer's ingenuity.

BUILT-IN TEST SOFTWARE

On-chip test software is possible only in single-chip microcontroller units (m.c.us) which, of course, have the on-board program rom to contain it. In such a scheme, an area of rom is reserved for a short test program which will be executed when the device is forced into a special test mode. In the examples discussed later, this involves placing the device in a simple independent test jig.

Test code is written using the machine's normal instruction set and it attempts to test as much of the device as possible (e.g. ram, timers, ports etc), though many other sections are exercised by the simple fact that the m.c.u. is running (e.g. the c.p.u.).

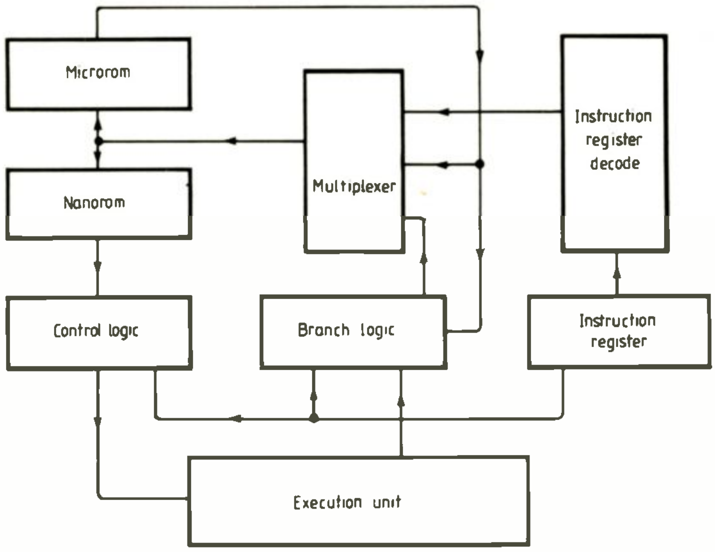


Fig.3. Simplified diagram of the MC68000 micromachine. All M68000 devices are microcoded.

The tests are cyclic, repeating so long as the device remains in the self-check test mode and none of the tests fails. Leds are connected to a port which increments every time a test is passed. Should a test fail, the test program wil hang and the frozen leds can be decoded to indicate the identity of the first failed test. The simplicity of the test jig allows effective go/no-go tests to be performed in the field without the use of a v.l.s.i. tester.

Combining self-test software with a signature analysis scheme provides a structured test solution for an m.c.u. device almost totally independent of the tester (though not quite, see later).

We shall now review four examples of the practical application of structured testing in commercially-available v.l.s.i. devices which are in volume production. The complexity of the devices to be discussed ranges from a very simple m.c.u. family (M6804), to the most powerful microprocessor Motorola currently produces (MC68020). Unfortunately, a detailed description of the features of these devices is beyond the scope of this article. Dates in brackets refer to the year when the device – or the first family member – went into production.

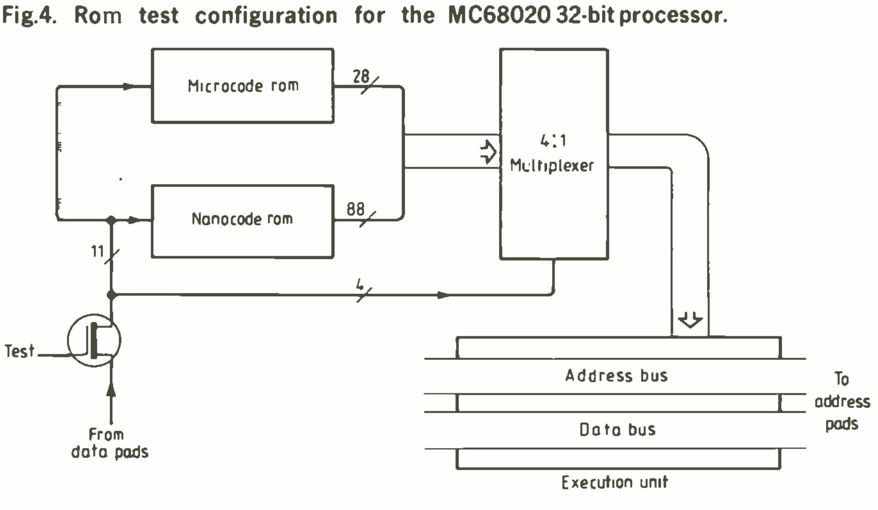
M6805 (1978)

This is Motorola's largest and most popular family of eight-bit m.c.us; it currently has 30 members and is still being expanded. All members have on-chip rom or eprom (with two exceptions), ram, timers and i/o ports. Some also contain on-board peripheral functions such as serial interfaces, a-to-d converters, p.l.ls and eerom arrays. All the rom-based devices feature two test modes:

1. **Non-User Mode.** The M6805 family was not intended to be expandable (i.e. internal address, data and control buses are not user-accessible). This presented a test problem which was overcome through the addition of a test mode that partitions the device and routes the internal buses to the device ports (Fig.1).

Note that the resulting bus configuration is somewhat unusual – the partitioning is arranged to isolate the c.p.u. data read (injection) bus from the data write (peripheral) bus. This effectively allows the c.p.u. to use program/data information from a source other than the internal address space. However, all c.p.u. 'writes' are active

Fig.4. Rom test configuration for the MC68020 32-bit processor.



internally, though they may also be externally duplicated.

Restrictions in pin-out make it necessary to multiplex the peripheral data bus with some of the address lines. Using for operations ports which are also used to interface to on-board peripherals is avoided. A synchronizing clock and some control signals are also provided. Timing is such that even with the multiplexed buses, full speed operation is possible. Non-user mode is entered through a hardware configuration present when the device is reset, the details of which vary from device to device. This test mode is also used in the design of in-circuit emulators.

2. **Selfcheck.** All rom-based devices feature a stand-alone, self-testing mode of operation called 'selfcheck'. Test mode configurations are different for many M6805 family members; however, a typical self-check circuit is shown in Fig.2. The selfcheck test mode forces the c.p.u. to use an alternative set of reset and interrupt vectors by modifying one of the rom array address lines. Consequently, after a reset, the device will execute self-test instead of user code.

The on-chip software is capable of testing about three-quarters of the device. It consists of a series of subroutines which test each module individually. The effectiveness of each is traded off against rom space used, so many of the tests are very simple. However, as many of the tests may be called from user code as subroutines, the programmer can effect a limited in-circuit chip functionality test – during initialization, for example – with a minimum software overhead.

M68000 (1979)

This family of high performance 16/32bit microprocessors features a 32-bit internal architecture. The full 32-bit device, MC68020, incorporates many improvements to the original M68000 test configuration, and is therefore discussed separately.

All M68000 family members are microcoded: a simplified diagram of the M68000 micromachine is shown in Fig.3.

The macro (user) instruction is loaded into the instruction register. The instruction register decoder consists of entry and residual p.l.as. Entry p.l.as provide the starting address of the appropriate microcode routine in the microrom and the address of the first word to be used from the nanorom. In the nanorom are field-encoded control words which, after further manipulation by the control logic, directly manipulate the execution unit. The microrom generally provides the next address for both itself and the nanorom. Residual p.l.as decode fields extracted from the instruction word which are not involved in instruction sequencing (e.g. execution register allocation). Outputs of these arrays are directly interfaced to the execution unit.

MC68000 (1979): in test mode, the device is partitioned to separate the nanorom outputs from the execution unit and route them to the address bus. As the nanorom is very wide, it must be multiplexed on to the bus.

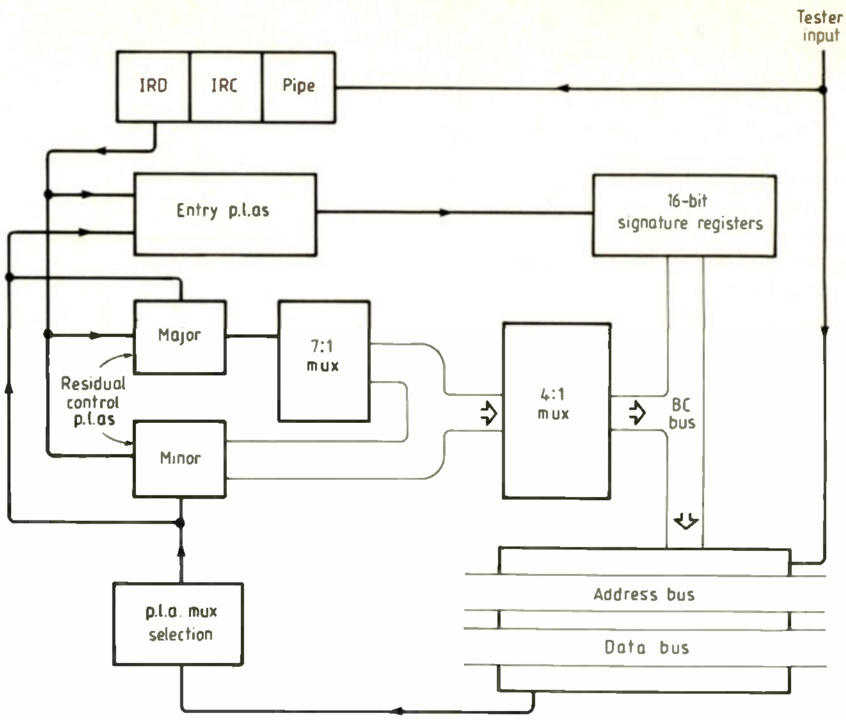


Fig.5. Testing the programmable logic arrays in an MC68020: test microcode is used to partition the instruction decodes p.l.as from the rest of the device.

The test pattern is injected into the instruction register and designed to exercise decoder p.l.as, microrom and nanorom. In this configuration, the execution unit is disabled. However, although this scheme did allow access to the internal roms, it suffered from many drawbacks. Observability was poor: when a failure appeared, it was difficult to determine the source of the problem owing to the degree of interdependence between the internal structures under test. The test program was lengthy, tough to implement and was microcode-dependent. Nevertheless, it was a move in the right direction, and one which was to be improved upon for the considerably more complex MC68020.

MC68020 (1985): this device included many new features, such as on-chip instruction cache, instruction pipelining, co-processor support and many new addressing modes. To improve observability of the micro and nanoroms, the partitioning scheme was modified[3] to isolate the instruction register's decoder p.l.as from the micro and nanorom, and route the rom address lines to the data bus (Fig.4).

The rom outputs are multiplexed on to the address bus much as before using the upper data lines to control the multiplexer. Inputs to the roms are no longer restricted to what the p.l.as can generate and the rom address space is small (2K) and so exhaustive testing is therefore feasible.

Test microcode is used to partition the instruction decoder p.l.as from the rest of the device (Fig.5). The entry arrays (A1, A2, A5, A6) are tested independently with test microcode. One form of this uses deterministic data originating from the tester, the other is built-in selftest. The array outputs are only

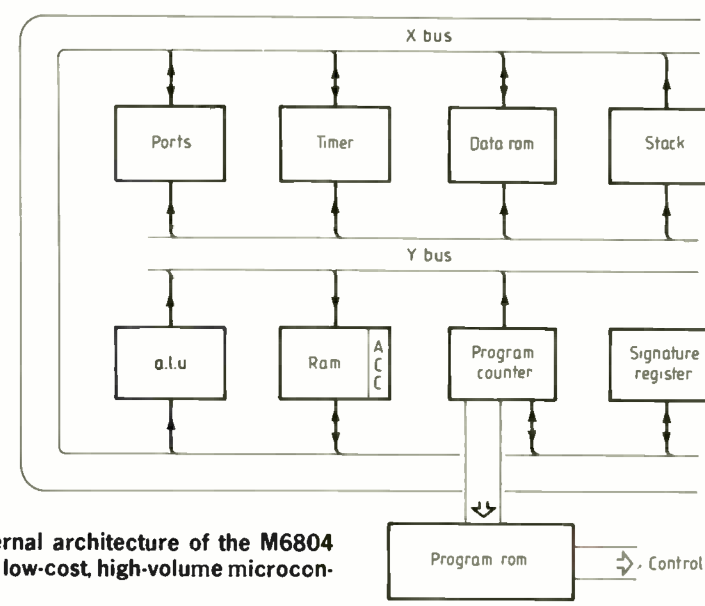
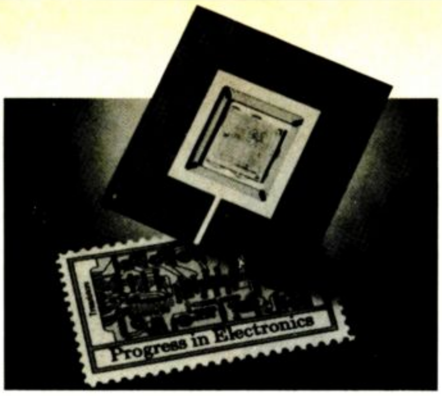


Fig.6. Internal architecture of the M6804 family – a low-cost, high-volume microcontroller.



M68000 device in p.g.a. package.

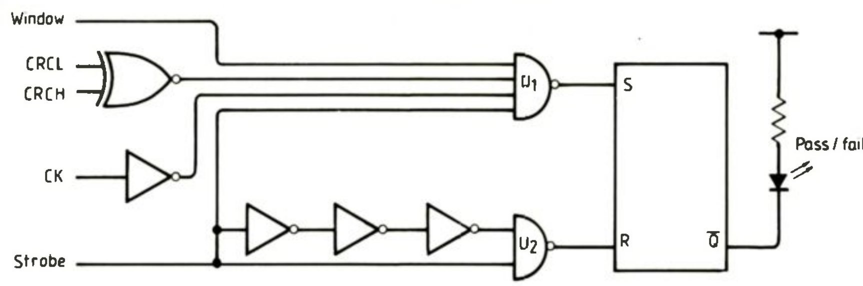


Fig.8. External hardware needed for rom-verify testing of M6804 devices.

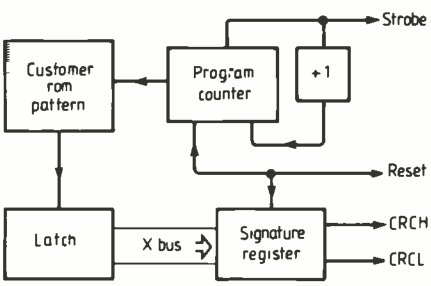
11 bits wide and are therefore suitable for data compression using a 16-bit l.f.s.r. (signature register). The resulting signature is bused off chip via the address bus after each entry array is tested. The residual p.l.as are too wide to test through signature analysis and so their outputs are multiplexed and then bused off the chip. The test pattern is injected through one of the instruction registers.

In an attempt to simplify the development of concise test patterns for complex arrays like these, Motorola has developed automatic test-pattern generation software.

M6804 (1983)

The M6804 family of eight-bit m.c.us is intended for use in low-cost, high-volume controller applications. Versions in both h-mos (high density n-mos) and c-mos are available (including one reduced pin-out version in a 0.3 inch wide, 20-pin package).

Fig.7. Rom verify mode: the 6804 is partitioned to bring its signature register bytes off-chip.



To reduce die size, a serial architecture was used (Harvard, Fig.6), though the m.c.u. appears to the programmer as an eight-bit device. However, the serial nature of the machine forced the use of some degree of on-chip self-test, since to test it conventionally would have required an extremely large number of test vectors. For such a low-cost m.c.u. test costs had to be minimized and so on-chip signature was adopted as a solution to the problem[4]. Three test modes are available.

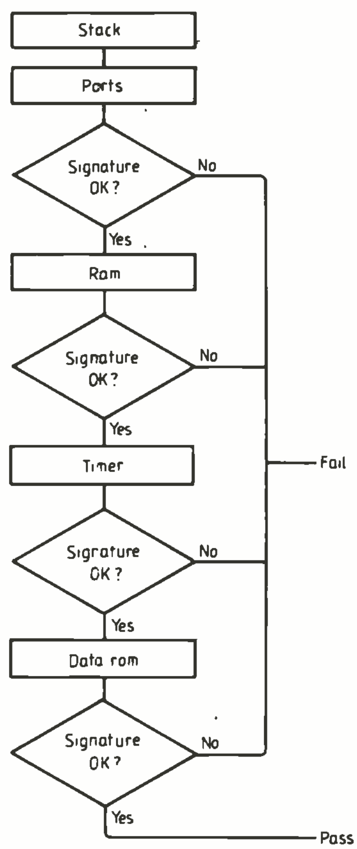
1. **Rom verify:** to keep the test program small the rom is verified on-chip. To do this, the device is partitioned to route the high and low-order bytes of the 16 bit c.r.c. (signature) register off-chip, together with some control signals (Fig.7). External hardware required for stand-alone operation is shown in Fig.8.

After leaving the reset state, the c.r.c. register is loaded with a seed word. The program counter then increments through the entire memory map, feeding all program rom data through the register. When the counter overflows, a strobe signal opens gate U_1 and allows the final register content to be clocked out. The window signal indicates when valid data is being clocked out.

The seed word is calculated (by Motorola) to ensure that the final high and low-order c.r.c. contents are always the inverse of each other ($AA and $55). As the seed is predetermined and is placed into data space rom, any external supervising pattern will therefore become customer-independent.

2. **Selfcheck:** operation of this test mode is very similar to the M6805 family's selfcheck except that use is made of the c.r.c. register. From Fig.6, all activity on the X bus is directed into the register. By using the register within the self-test software (Fig.9), the M6804 self-test monitors device functionality during the execution of every instruction cycle. The M6805 self-test, however, can only indicate the end result of a specific test. Consequently the M6804 self-test achieves 96% fault coverage through just 288 bytes of program rom. Functions such as reset, mode select logic and non-user mode operation cannot be completely tested through self-check.

Fig.9. Self-test flow-chart for 6804: 96% fault coverage is achieved through just 288 bytes of program rom.



3. **Non-user mode:** since some areas of the device cannot be checked by self-test, an additional test mode which can gain access to the internal buses becomes mandatory. Also, as the test pattern is customer-independent, the rom pattern number allocated to the customer (stored in data space rom) must be read by the tester to confirm that the correct part is being tested. However. as with the M6805 family, a significant application for non-user mode operation is within in-circuit emulators.

THE FUTURE

Although the concepts behind structured testability have been discussed for many years, few commercial v.l.s.i. designs have made much use of them. The silicon area necessary to implement what is essentially superfluous test logic, is a sticking point. But as device complexity increases, designers are finding that structured techniques are essential if their devices are to be testable. Nowhere is this more apparent than in the field of semi-custom v.l.s.i. devices.

The M6804 test philosophy is very close to 100% Bist. Yet for the 1K rom h-mos version (MC6804P2) the test logic silicon is only about 5% of the total die size. Although in many cases a fully structured test approach like this may not be practical, possible or even desirable, such ideas may offer food for thought to anybody currently about to embark on a new v.l.s.i. design.

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2. Hans Christian Oersted (1777-1851): discoverer of electromagnetism

Picture: Institution of Electrical Engineers.

Pioneers

W.A. ATHERTON

Major scientific discoveries are rarely made before an audience: still less, perhaps, before an audience which is unimpressed. But such was the case when H.C. Oersted discovered electromagnetism in 1820 and so unified the two previously separate sciences of electricity and magnetism.

Oersted's name is now enshrined within our system of units of measurement, whereas those of his unappreciative audience are lost in the sands of time.

Hans Christian Oersted was the elder son of a Danish apothecary (pharmacist). In his early childhood he and his younger brother, Anders Sandoe, were looked after by neighbours while his parents attended to the business of earning a living.

The neighbours, a German wig maker and his Danish wife, taught the boys German, religion and arithmetic. A friend instructed them in multiplication and a parson in division. Latin and Greek were learned from an engraver and drawing from the local baker.

This rather unusual education gave the boys a thirst for knowledge and a self-reliance in getting it. It also bound them together very closely in their learning, a habit which was to last into their university years.

After serving apprenticeships in their father's pharmacy – a training in basic chemistry which served Hans Christian well in his future scientific career – both went to Copenhagen University where Oersted graduated with a degree in pharmacy and his brother with one in law. Their ways then separated. Anders Sandoe became not merely a judge but eventually prime minister!

At university Oersted acquired a passionate devotion to the philosphy of Immanuel Kant (German philosopher, 1724-1804). So much so that he became a member of the editorial staff of a magazine specializing in defending and promoting Kant's philosophy, and his Ph.D. thesis was about the importance of that philosophy to science. It was also to become the rock on which his own philosophy and his future scientific career were founded. By it he was led to a conviction that forces could be converted from one form to another and eventually to the discovery that electricity could be converted into magnetism.

During a short spell as a manager of the Lion Apothecary, a well-established pharmacy in Copenhagen, and whilst an unpaid lecturer at the university, Oersted was awarded a three-year travel scholarship. By now he was a talented philosopher but still had much to learn about being a scientist. He used the travel to further his scientific interests.

In 1800 Alessandro Volta in Italy had announced the invention of the primary battery and caused a scientific sensation. Like many others Oersted built his own battery and began his Grand Tour of Germany and France in 1801 while the fervour was still fresh.

On the tour he became acquainted with some of the leading figures of the day, and not always entirely to his benefit. By at least one he was led into accepting philosophical supposition as fact – only to be shredded by the eminent scientists of Paris, then one of the leading scientific centres of the world. Thus labelled as an uncritical scientist, on returning to Copenhagen Oersted found it impossible to gain the professorial position he sought.

His extremely popular public lectures, however, helped restore his reputation and he later became a great popularizer of science. Securing a post as 'extraordinary professor' he began a series of careful scientific experiments, which were well received. His climb up the ladder of scientific respectability had begun.

Oersted's philosophy was always to seek unity in nature. "It is my firm conviction", he wrote in 1810, "that a great fundamental unity permeates all nature."

Further, with the backing of a strong Christian faith, he believed that the universe had been designed by God and in such a way as to use the minimum resources. Working before the enunciation of the principle of the conservation of energy, Oersted saw the seemingly diverse phenomena and forces of nature as all intimately linked: "all phenomena are produced by the same original power" was the basis of his ideas. As such, electricity, magnetism, light, heat, and chemistry were probably different forms or manifestations of the same two powers, "which probably might be only two different forms of one primordial power."

Since 1800 the new science of electrochemistry had demonstrated that there really was an intimate link between electricity and chemistry.

In Oersted's view, an electric current was the manifestation of two forces of electricity (positive and negative) in conflict with each other. The consequences of this conflict, he believed, would travel wave-fashion through space. If constrained by a fine wire the wire became warm or even hot, showing that heat was also probably a manifestation of this conflict of two basic forces. A very thin wire could be heated to incandescence. Therefore it seemed that light and electricity were both results of the same forces.

In 1812-1813 Oersted expressed these ideas in a great book. He predicted the close association of electricity and magnetism years before Faraday or Maxwell and eight years before his own discovery of electromagnetism.

This was quite out of keeping with the scientific thinking of the times. The similarities between electricity and magnetism had long been known: both exhibited powers of attraction and repulsion, both had two forms (positive and negative electricity, north and south magnetic poles), steel needles were known to have become magnetized after a lightning strike and Franklin had shown that lightning was electrical in its nature. In 1774 the Royal Bavarian Academy had posed a prize essay question to try to show whether the two were related, but no-one had been able to give a conclusive answer.

Then in the 1780s the great French scientist Charles Coulomb proved conclusively (or so it was believed) that electricity and magnetism were two quite separate and distinct sciences, even if somewhat similar.

For most of the scientific community that had settled the matter.

To Oersted, however, with his deep convictions based on his understanding of Kant, coupled and supported by a strong belief in God as supreme designer, the existence of a link seemed inevitable. All that was needed was to discover the right conditions for the conversion of one to the other to take place.

In the winter of 1819-1820 Oersted gave a series of lectures to a small group of advanced students. One experiment he wished to try was the effect of a closed electrical circuit on a magnetic needle. Open-circuit conditions had been tried exhaustively by others to no avail.

Not having had time to rehearse the experiment before the lecture he decided to postpone it. But during the lecture he changed his mind and gave it a try. In accordance with his beliefs the wire was thin and so had a high resistance; in fact he thought the wire might have to glow with heat before any effect would occur. A feeble current flowed, a magnetic field was produced around the wire, and the needle moved.

The effect was not very dramatic and even Oersted was not certain. Further experiments were postponed for three months to July 1820 until time and a more powerful battery (and in the end, thicker wire) were available.

Later even Oersted himself could hardly credit the delay in pursuing the discovery which gave him fame in the history of science. The results were now conclusive: an electrical current produces magnetism.

Having discovered a new continent in the world of science Oersted himself carried out the first exploration. A direct current flowing through a wire affected a magnetic compass needle placed below it. He moved the needle around the wire and discovered that the magnetic field (in modern parlance) was circular around the wire and that the kind of metal used was not critical, though it did affect the magnitude. This latter observation, to be explained later by Ohm's Law (1826-27), was the first demonstration of the principle of the ammeter.

Michael Faraday on H.C. Oersted: "No experimental proofs of the peculiar opinions he entertained were known; but his constance in the pursuit of his subject, both by reasoning and experiment, was well rewarded... by the discovery of a fact of which not a single person besides himself had the slightest suspicion."


EXPERIMENTA

CIRCA EFFECTUM

CONFLICTUS ELECTRICI IN ACUM MAGNETICAM.

Prima experimenta circa rem, quam illustrare aggredior, in scholis de Electricitate, Galvanismo et Magnetismo proxime-superiori hieme a me habitis instituta sunt. His experimentis monstrari videbatur, acum magneticam ope apparatus galvanici e situ moveri; idque circulo galvanico cluso, non aperto, ut frustra tentaverunt aliquot abhinc annis physici quidam celeberrimi. Cum autem haec experimenta apparatu minus efficaci instituta essent, ideoque phaenomena edita pro rei gravitate non satis luculenta viderentur, socium adscivi amicum Esmarch, regi a consiliis justitiae, ut experimenta cum magno apparatu galvanico, a nobis conjunctim instructo, repeterentur et augerentur. Etiam vir egregius Wleugel, eques auratus ord. Dan. et apud nos praefectus rei gubernatoriae, experimentis interfuit, nobis socius et testis. Praeterea testes fuerunt horum experimentorum vir excellentissimus et a rege summis honoribus decoratus *Hauch*, cujus in rebus naturalibus scientia jam diu inclaruit, vir acutissimus Reinhardt, Historiae naturalis Professor, vir in experimentis instituendis sagacissimus Jacobsen, Medicinae Professor, et Chemicus experientissimus Zeise, Philosophiae Doctor. Saepius equidem solus experimenta circa materiam propositam institui, quae autem ita mihi contigit detegere phaenomena, in conventu horum virorum doctissimorum repetivi.

In experimentis recensendis omnia praeteribo, quae ad rationem rei inveniendam quidem conduxerunt, hac autem inventa rem amplius illustrare nequeunt; in eis igitur, quae rei rationem perspicue demonstrant, acquiescamus.

Apparatus galvanicus, quo usi sumus, constat viginti receptaculis cupreis rectangularibus, quorum et longitudo et altitudo duodecim aequaliter est pollicum, latitudo autem duos pollices et dimidium vix excedit. Quodvis receptaculum duabus laminis cupreis instructum est ita inclinatis, ut baculum cupreum, qui laminam zinceam in aqua receptaculi proximi sustentat, portare possint. Aqua receptaculorum $\frac{1}{60}$ sui ponderis acidi sulphurici et pariter $\frac{1}{60}$ acidi nitrici continet. Pars cujusque laminae Zinceae in aqua submersa Quadratum est, cujus latus circiter longitudinem 10 pollicum habet. Etiam apparatus minores adhiberi possunt, si modo filum metallicum candefacere valeant.

First page of Oersted's 1820 pamphlet "Experiments on the effect of electric current on a magnetic needle". It created a frenzy of scientific excitement.

The magnetic field was found to pass through various media, but a needle made from 'non-magnetic' material did not work.

Oersted was certain that the effects he saw were not electrostatic. On 21st July, 1820 he published a brief account of his work in Latin and sent copies of it to the leading scientific centres in Europe. Its importance was recognized immediately and a frenzy of scientific excitement followed.

The ramifications of Oersted's discovery were enormous. In science, for example, it led to the enunciation of the laws of electrodynamics, the production of electromagnetic rotation, the search for and discovery of electromagnetism, the discovery of thermoelectricity, and of course the study of *the* physical science of the 19th century: electromagnetism itself. In engineering the practical results were rapid: the electromagnet, the galvanometer and the electromagnetic telegraph to begin with; and later, electric motors and generators, the telephone and radio.

Oersted's later scientific work included extensive studies of the compressibility of gases, and diamagnetism; but before his death in 1851 he turned again to his first love – philosophy.

Within Danish society he rose to become the country's leading scientist. In 1820 he obtained funds to build a chemistry laboratory for student use at Copenhagen University, something then almost unheard of – students in those days merely saw experiments demonstrated to them, they did not perform experiments themselves.

He helped found the Society for the Promotion of Natural Science, a magnetic observatory, and the Technical University of Denmark, of which he became the first director. He also helped to lead public discussion about the need for general education to include science and he continued his own public lectures, which he approached with all the dedication of an actor going out to give a great performance.

Socially, Oersted met most if not all the great scientists of the day: Ampère, Biot, Arago, Fresnel, Fourier, Gauss, Seebeck, Herschel, Davy, Faraday, and Wheatstone to name just a few. In fact it was Oersted who encouraged Wheatstone to write his first scientific paper.

Today Oersted's name is used for the unit of magnetic field strength (in the c.g.s. system) and he is celebrated for making what is arguably the most important discovery in the history of electricity.

Next in this series of pioneers of electrical communication will be André Marie Ampère, father of electrodynamics.

Tony Atherton works at the Independent Broadcasting Authority's Engineering Training College in Devon. He is the author of the book "From Compass to Computer, A History of Electrical and Electronics Engineering" (Macmillan, 1984).

FEEDBACK

Planck and the fine structure

Two well-known constants in atomic physics are the Planck's constant, h, with a numerical value equal to 6.626176(36)E-34 Ws^2 and the atomic fine structure constant, α, represented by a dimensionless number of 1/137.03604(11). It is less well known that there exists a relation between these two fundamental physical constants,

$$h=2\pi m_e r_e c(a-1)$$

where m_e= electron rest mass 9.109534(47) E−31 kg; r_e= classical electron rest radius 2.8179380(70) fermi; c= propagation velocity of light in vacuum 2.99792458E8; (a−1)= reciprocal value of the atomic fine structure constant 137.03604(11)

For the sceptical, it is easy to check the validity of this relation by using a calculator, inserting these figures in the given relation. The relationship discloses a deep relation between fundamental constants in physics.

Ove Tedenstig
Märsta
Sweden

Baseband signal generator

M. Charnley's "cost-effective" signal generator (*EWW*, December 1986. pp.55-57) reminds me of a very much simpler method of generating arbitrary periodic waveforms which was used in an Admiralty laboratory more than 30 years ago.

Inside the light-tight hood of an oscilloscope of the type adapted for photographing waveforms a photodetector was placed which was connected to the Y amplifier of the oscilloscope. The shape of the waveform required was cut out of a piece of brown paper with a pair of scissors, and this was put against the face of the display.

When the gain and polarity of the oscilloscope amplifiers were set up correctly, the light spot ran along the edge of this paper mask and the desired waveform appeared on the outputs of the Y amplifiers. The signal repetition frequency could be adjusted by setting the timebase controls over a very wide range, seemingly limited only by the frequency response of the photodetector.

John C. Rudge
Harlington
Middlesex

Airmac

This letter was passed to us by the CBI. Does anyone know the receiver Mr Bar mentions?

May I be allowed to express my congratulations and thanks to the producer of the Airmac radio-receiver which I bought in 1946 in London when leaving for Poland as a demobilized officer of the Polish Air Force in Great Britain.

The radio has been serving usefully for 40 years.

Ludwik Bar
Warsaw

White-collar engineers

I read with great interest the article in the December issue entitled 'White-collar engineers'. I am a final year undergraduate in electronic and communications engineering and the tone of the article appeared to be in complete sympathy with my own views. Having now been an engineering student for some seven years, (the long road from CGLI) I have found more and more of my fellow students have taken an almost obsessional view of the ever-increasing computing content of the syllabus.

I have always viewed this as undesirable trend and have myself tended to bias my efforts towards the more academic parts of the syllabus. I feel now that button pressed and black-box shufflers are all that can be turned out from my polytechnic with the recent introduction of the SPICE system. An incredible amount of time has to be spent on the SPICE system in order to keep up with course work.

I commented to a lecturer that engineers are designing themselves out of profession, since there appears to be less and less emphasis on fundamental engineering principles, and the ubiquitous "it can be shown that" crops up more in my lecture notes than even before. Surely circuit analysis must be taught and understood manually before discarding it for powerful development tools like SPICE.

After my graduation I intend to make a complete educational shift, as I feel I don't understand enough of the analytic techniques used by the circuit designers of old to this end I'm now applying for engineering mathematics-based courses.

B.G. Newdick
Brookhill Road
Barnet

Electronic exchanges

In your June issue you published a letter in which T.J. Robinson complained about British Telecom's attitude towards its electronic exchanges, so a letter from BT recently received by subscribers on the 061-440 exchange may be of interest.

Inter alia, this stated "...modernization programme...faster, clearer, more cost-efficient...wide range of extra facilities... if you have any communication equipment that is neither supplied by BT nor maintained by our engineers you should contact your supplier to check its compatibility with the new digital network".

This makes it look as though BT has changed its mind.

D.J. Wattson
Cheadle Hulme
Cheshire

Intentional logic symbols

One remark by John C. Rudge (July 1986 Feedback) must not pass without comment.

The staff of the British Standards Institution (not Institute) are not civil servants, nor are they responsible for deciding the technical content of British Standards. That is done by committees on which are represented all the various interested parties; all, that is, that bother to participate. Moreover, before a standard is published a draft is circulated for public comment.

If bad standards are published, it is because few people have taken an interest at the drafting stage.

Another remark needing comment is J.L. Linsley Hood's (July 1986, p.24) about young staff leaving for higher salaries and more secure prospects. I can almost sympathise with him, because one bright young graduate recently left my section for 50% better pay in another organisation. Only his move was *from* government emploment *to* industry.

Richard G. Mellish
North Harrow
Middlesex

Admixture

I would like to make a plea for a return to sanity in the layout of Wireless World (I refuse to recognise the tautological *Electronics* and...). My complaint is not with the presentation of articles, but rather with the scattering of advertisement pages in an abandoned manner throughout the magazine.

Advertisements are clearly necessary and even useful, but they should have their place at front and back, leaving the meat of the magazine free. A quick flip through *WW* on a bookstall leaves the impression that it is one of those give-away magazines containing only advertisements and ad-related text: hardly the way to attract new readers, I should have thought. Regular readers know that this is not the case, but they are addicted anyway.

I did mention this on the recent questionnaire, but felt that the point might be emphasized in this way.

H. Morgan
Tonbridge
Kent

Mr Morgan echoes a view put forward by many readers, but we do have to take note of the requirements of advertisers, who demand 'facing matter' positions. If they did not advertise, the cover price would be impossibly high. Nevertheless, I would welcome comment on this point – from advertisers as well as readers – Ed.

Fourier and filters

In the November Letters both B.J. Pollard and I wrote about the use of Fourier transforms to calculate the effect of near-ideal low-pass filters. However, since my letter dealt with the problem in the frequency domain, and his in the time domain, it wasn't immediately obvious that we were in agreement. In the time domain, the input waveform is *convolved* with the impulse response of the filter to obtain the output waveform. In the frequency domain, the amplitude of each element of the spectrum of the input waveform is *multiplied* by the amplitude of the corresponding element of the 'transfer function' for the filter (i.e. the Fourier transform of its impulse response) to obtain the spectrum of the output waveform. Thus my comments about permissible phase responses of physically realisable filters and the Hilbert transform correspond with Mr Pollard's comment that carrying out the convolution in the time domain involves integrating the impulse response of the filter into future times.

I sympathise with D. Gibson's remark in the September letters that the use of unnecessarily elaborate mathematical tools should be avoided. However, music must be described in terms of both time and pitch. After making the apparently straightforward change from the brain's pitch to the physicist's frequency, one can easily be tempted into the fantasyland of 'the frequency at an instant'. A very modest acquaintance with Fourier transforms and their application to some simple physical systems will make it possible to grasp the significance of the 'acoustic uncertainty principle', which states that, if you want to define the frequency of a waveform to better than $\triangle f$, you cannot restrict the time interval over which it is sampled, Δt, to less than $1/\triangle f$ seconds. Thus a filter cutting off over a frequency range Δf will have a settling time for step functions in excess of $1/\triangle f$ seconds. Anyone whose armoury for investigating the frequency domain is limited to Fourier series is in effect shutting his eyes to uncertainty phenomena by assuming that Δt is infinite, even though he may believe that he is dealing with waveforms of finite duration. An ideal low-pass filter is, by its very name, defined in the frequency domain, so perhaps the folklore about determining its behaviour using Fourier transforms is not too surprising.

C.F. Coleman
Grove
Oxfordshire

Energy transfer

To reply to the supposition in the letter from Gibson, May 1986, the problem for which transmission lines are split into multiple cables arises from voltage, not current. In a.c. transmission, excessive corona loss appears on small wires above about 30,000V. Answer: make the wires larger in diameter to reduce the surface electric field intensity in the air. By splitting the conductor into a "bundle" of small wires, the effective conductor diameter is increased to that of the bounding circle. Therefore, less corona loss.

J.D. Ryder
Ocala
Florida
USA

Relativity

I was stunned in the middle of W.A. Scott Murray's relativity article (December issue p.28) to find him pondering the design of the earth as an oblate spheroid and stating that the necessity for this was demonstrated by its satisfying the condition that the plumb-line is always at right angles to (any line in the horizontal derived from) the spirit level. This would be so even on a planet shaped as an irregular tetrahedron, or in deep space, since the two devices equally define the *vertical*, the spirit level by giving us a line or plane at right angles to it.

In the relativistic context I want to shatter the picture of a person upset by living on a perfectly spherical rotating planet and finding his plumb line is pulled away from pointing to the centre of gravity by the centrifugal force caused when the planet rotates – the picture that has to be ditched to explain our own planet – by rudely saying of its rotation "it does, does it?" I propose a modest experiment whereby we remove every object but the earth from the universe (an EEC grant should do the trick) and find out whether the *actual* bucking, and change of direction, of gravitational force, still occurs. The rotation itself would be impossible to measure under these conditions, so in what sense would its exist? Is centrifugal force, then, due to the rotation or to the presence of the rest of the universe?

(Obviously the actual *slanting* of gravity-plus-centrifugal force only occurs away from the poles and the equator, where the centrifugal force at right angles with our axis of rotation forms an angle with the gravity vector. But this is the situation for most of us.)

Bernard Jones
London W1

I well appreciate Michael Snoswell's anxieties. The hypothesis that energy has inertial mass is not entirely straightforward but it does seem to me to be a far more reasonable starting point than the usual one about light. My own view is that nature is intrinsically simple and I offer for debate the proposition that there are no laws of nature; only self-evident propositions. A suitable definition of the concept of energy as potential for imposing change would immediately imply inertia; this may be one such self-evident proposition supporting the mass/energy hypothesis.

If you accept it, the mass/energy hypothesis does provide an easily understood and quantitatively correct alternative explanation of the otherwise seemingly weird phenomena associated with clocks and rods in motion according to relativity theory. Not only that, it provides an underlying explanation of light (and other radiations at velocity c) complete with its properties of absolute velocity, which are generally not easily accepted. Perhaps even more significantly, we also see possible explanations for gravitational attraction and quantum phenomena via the resultant principle of the "spatially distributed single event" explained in my paper. I am convinced that when a unified theory is put forward the mathematics to understand it will not be as difficult as Michael Snoswell fears.

I was delighted to see more from my friend James McHarg. He was not to know that I too am a Leo. We agree on far more than he volunteers. In his previous letter he very profoundly pointed out that mass (or rather its quality, inertia) prevents instantaneous change. If energy exchanges cannot be instantaneous from one place to another we can reasonably look for an associated mass that has to be accelerated.

The "wriggling device" which James McHarg mentions is, of course, a principal remaining item necessary in the unified theory. If we can show that stationary or slowly moving packets of energy can only exist in discrete sizes, I suspect that they will have masses corresponding to electrons and the other well known particles. I further suspect that these eigen packages will have a uniquely defined angular momentum $h/2\pi$ and a practical explanation of quantum theory phenomena will follow with gravitation close behind. The known fact that an electron-positron pair can turn into a γ-particle and vice-versa is strong evidence in support of this notion. It may be that Einstein saw all this in an LSM, as suggested by James McHarg.

C.F. Coleman objects to my use of accelerated systems. Einstein himself states in his book, The Meaning of Relativity, that time and space relationships depend only on velocity, not on acceleration. General Relativity kinematics is constructed in the literature using inertial frames of reference momentarily coincident with the accelerating frames (of course the classical effects of acceleration on an imperfectly balanced balance wheel and stress in materials are discounted). This simplification still leaves matters complicated; for example, the progressive contraction of an observed accelerating frame means that fixed points in the frame have different accelerations. However, the subject is manageable and in The Theory of Relativity by Moller, published by Oxford University Press, we find a complete explanation of the Clock Paradox in which both parties agree on the performance of each other's clocks, i.e. it is no longer a paradox.

The word 'simultaneous' needs clarification. We agree that the concept of a universal time has to be abandoned and any general notion of simultaneity that goes with it. So, how do we define the length of a moving rod? The two sequences of events traced out by the two ends must be used. We have no option but to set up some prac-

FEEDBACK

tical time measurements in our laboratory and define length as the separation between two clocks which give the same reading as the ends pass. This I do in my paper in the most obvious way using standard clocks and reflected signals to synchronise them and we get the famous $(1-v^2/c^2)^{1/2}$ factor.

C.F. Coleman takes the view that electromagnetic effects are "determined" by the geometrical structure of the space-time continuum and describes it as Einstein's major achievement. I am not sure what this means: writing down a mathematical proposition cannot "determine" physical events and I am sure Einstein only saw it as descriptive, just as his theory of gravitation was descriptive rather than explaining the phenomena.

H.Aspden is not commenting on my paper, but I find his thesis interesting. It is, of course, possible to construe a set of mathematical rules of behaviour to "explain" all the observed phenomena. The question is, what makes them do it? H. Aspden is proposing an ether with extraordinarily complex behaviour, by what mechanism? Whatever it is, this mechanism that makes things happen has zero mass and offers no resistance to motion! I submit that it is not necessary to go to such complexity. As I see it, space permits geometrical shape and movement, while time permits (or is a recognition of) change. Without either of them we could not be talking and our existence would have no meaning. Accepting that we do exist and can discourse, space and time must therefore exist. We do not need to fill space with a complex mechanism (the ether) when all that is required is energetic interaction between particles by direct contact as explained in my article. Nature is essentially simple, and that should be a basic premise. Einstein once asked "When God created the universe did he have any choice?"

In his article "If you want to know the time..." (December, 1986) Dr Scott-Murray talks about the failure of relativity theory to match results from an experiment in 1971 with clocks in aeroplanes. However it does not appear that any clocks would have registered the effects.

Caesium clocks are separately quoted in 1970 as being accurate to 1s in 1000 years and 'a few parts in 10^{10}'. The CRC Handbook of Chemistry and Physics (affectionately known as the Rubber Bible) in 1976 states an accuracy of 5s in 300 years, which is equivalent to one part in 2×10^9. Taking the best of these as one part in 4×10^{10} it is well short of the required relativistic correction factor of 1.2×10^{-12} (or one part in 8×10^{11}). If, instead of equatorial velocity, we consider aircraft (whose velocity will be half or less) we get a relativistic correction of one part in 3×10^{12}. Currently (1986) caesium clock accuracies of one part in 10^{13} are mentioned: perhaps another test should be mounted.

It is, of course, important to test scientific theories. As Karl Popper would have it, they cannot be proved, only disproved or falsified. On the other hand I would press for a more positive attitude. There is a long list of directly observable phenomena which require to be explained. It is not helpful to look for every opportunity to knock the theory that provides an explanation without any vestige of something to replace it. Dr Scott-Murray clearly does not understand the theory from the statement ending his first paragraph. Relativity theory does not suggest that the clock on the equator is reciprocal with that at the pole, as he states!

Prof. R.A. Waldron (Letters, December 1986) claims to answer Alan Watson's request for experimental evidence contradicting Einstein's postulates, with two examples. For the first of these, Prof. Waldron claims that since a flash of light cannot have zero duration, the wave front seen by two observers cannot be a valid basis for deriving the Lorentz Transformation! How this conclusion follows is not explained; nor, as far as I can discern, is it experimental evidence. The second 'piece of observational evidence' is stated by Prof. Waldron to be less conclusive than the first, and I entirely agree. This concerns de Sitter's argument on spectroscopic binary stars. As Prof. Waldron explains, on one point support is given to relativity theory, on another the violation cannot be seen and on a third point some explanation is simply needed for a spectroscopic line splitting.

L. Essen, in the same issue, claims to have changed the theory of relativity or its basis of presentation. My recollection from seeing his article in *Wireless World* is, as he states, to have argued that Einstein's theory is 'demolished by its own internal errors and contradictions'. This hardly constitutes a change in the theory or its form of presentation. L. Essen also argues that the theory 'contravenes the foundations of science' by duplicating units of measurement. This is simply not so, the theory is constructed on a clear, consistent and practically defined system of measurement. As explained in my *WW* article last June, it leads to a behaviour of clocks and measuring rods described in the Lorentz Transformation.

This system of measurement requires clocks to be distributed at rest in each frame of reference and synchronized to the clock at the origin. The time of an event anywhere in the frame is defined as the reading of the clock at that position. When Observers A and B (in relative motion) time each other's clocks, they look at different series of events. Observer A notes the readings of the clock at B as it goes past clocks stationary in A's frame but not at A. Conversely, B notes the readings of the clock at A as it goes past clocks in B's frame but not at B. There is no error or contradiction over A being observed slower than B and B slower than A. Unless this is clearly understood, no progress can be made.

If, following L.Essen, one states that thought experiments are a 'travesty of science', then one disallows any theorectical mechanics. This surely cannot be.

M.H. Butterfield
Wimborne
Dorset.

Novel Q meter

My congratulations to J.M. Woodgate (Letters, December 1986) for correctly untangling the multiple schematic errors in my Q meter (October, 1986) piece and my thanks for the name of Thomas Roddam as the originator of this oscillator. I differ with Mr Woodgate on two minor but related points. On the matter of d.c. levels, the first circuit actually will work when redrawn as he correctly describes it, and indeed was the first breadboard circuit, but has limited frequency range because of the low collector voltages. The grounded-base stage in the final schematic was added as a straightforward way around this problem and could be regarded simply as a level shifter added to the basic version to get around the d.c. level problem without using a coupling capacitor.

As to Frank Henry's comments, first of all the "conventional Q meter" circuit I gave, although in principle workable, was simply a mistake on my part which resulted from an incorrect reading of a diagram in the manual for the Hewlett-Packard 4342A, which actually uses a still different arrangement. The circuit given by Stanley Kelly is the one I should have used.

Calibration of the new Q meter was in fact checked against the H-P and held within a few per cent to about 10MHz, deteriorating somewhat above that. It is true, as he implies, that at high Q values, circuit loading degrades the accuracy, but the same comment can be made regarding the conventional circuit in which the voltmeter input impedance must be high compared with the shunt loss being measured.

On Mr Kelly's comments, yes it is an inelegant beast. By today's rules an elegant instrument must include:

1. five-digit, direct-reading display
2. key-pad
3. microprocessor
4. stepper motor

so the Q meter won't qualify.

I think I detect a shred of controlled outrage here. Reflect, sir, if I did not like the instrument I would not have built one.

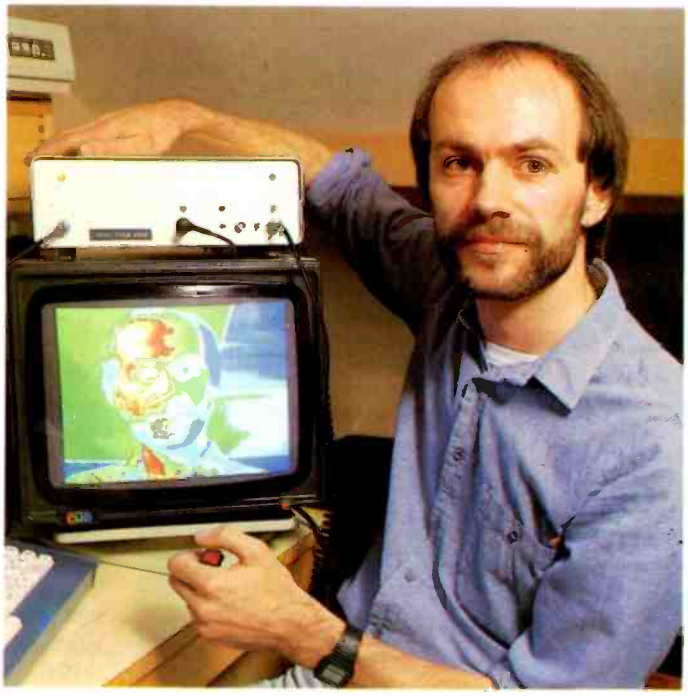
The main difference I think between G.W. Short's Q meter and mine is that he chose to use a coupling capacitor C_2 where I used a level-shifting stage. There are potential problems with this, since the capacitor must have negligible reactance over the entire working frequency range, but there are also questions about the level-shifter, so no debate. His comments on calibration and the use of an inverse log rheostat are of interest and I think entirely sound.

McKenny W. Egerton, jr.
Owings Mills
Maryland
USA

Video frame store

Operation of the memory board and setting-up procedure for the basic frame store.

D.E.A. CLARKE



Timing for memory write is shown in Fig.23. The master clock is shown for reference. Alternate samples from the flash converter on the analogue board are designated A(n) and B(n) to indicate which memory block (A or B) the data is destined for. Latching/steering waveforms are derived from IC_{104} pins 8 and 9 and consist of the clock divided by two.

Sample A(n) is latched in IC_{202}; and on the next clock cycle sample B(n) is latched in IC_{210}. Two consecutive samples are now ready to be written simultaneously to memory. Since the latch output enables are low during write mode, the data is present at the ram data pins. The write pulse from IC_{111}(3) on the control board completes the write cycle.

WRITE PULSE TIMING

The write pulse is active for a whole clock cycle and ends prior to the next address transition. The width of the write pulse is the most critical factor governing the choice of ram speed in this application. For 150ns static rams, write must be active for at least 90ns, which means a maximum clock frequency of 11.1MHz. In practice, the devices will often be faster than specified, especially if chip-enable is held active: the prototype worked without errors at sampling rates in excess of 15MHz.

With typical 150ns devices, the time for which the address must be held after a write is typically specified as 10ns, but it may vary between manufacturers. Link 3 on the control board enables this delay to be adjusted if necessary (in practice, no extra delay should be necessary).

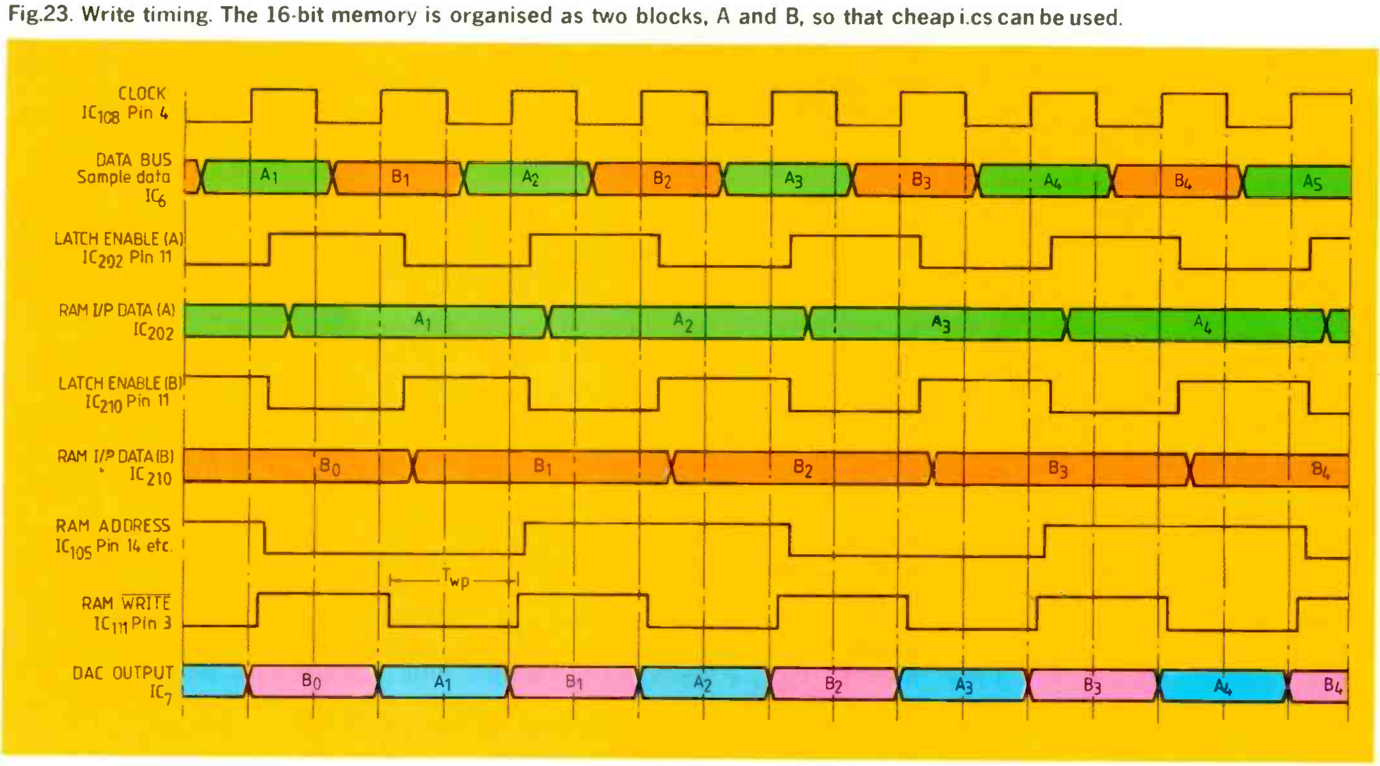
MEMORY READ MODE

Timing for memory read is shown in Fig.24. The memory ouputs are permanently enabled (OE low) during read mode, and the input data latches IC_{202}, IC_{210} are disabled. Stored data is then available at the ram outputs after an address transition.

Two pixels are available simultaneously from memory; these are designated A(n) or B(n) depending on the source memory block (A or B).

Referring to the timing diagram, data from memory B is latched in IC_{209}; notice

Fig.23. Write timing. The 16-bit memory is organised as two blocks, A and B, so that cheap i.cs can be used.



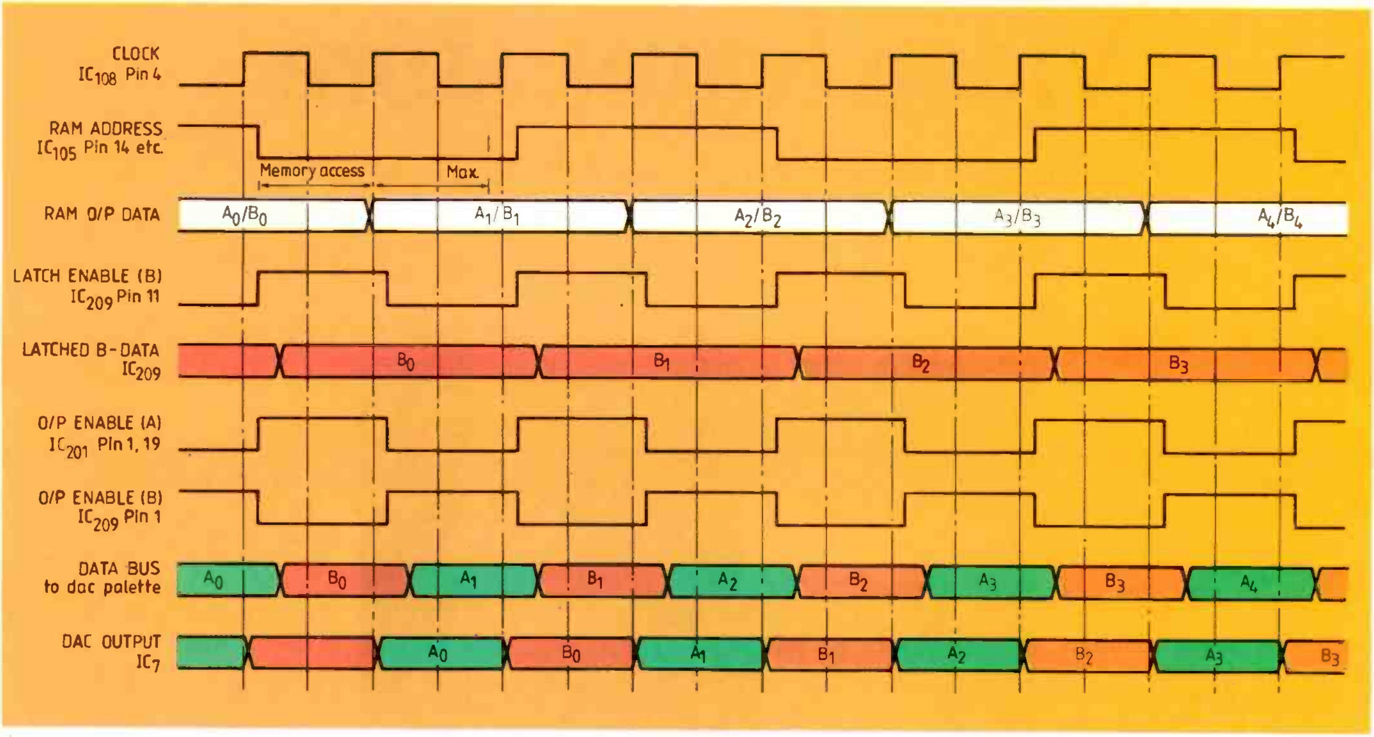


Fig.24. Memory read timing. Two pixels are available simultaneously, A(n) or B(n).

that this is in fact data from the previous address cycle. The data is held and enabled on to the bus simultaneously for picking up by the d.a.c. or colour palette half-way through the next address cycle. Data from latch B is then disabled and data from memory A enabled on to the bus in the second half of the current cycle. It is picked up by the d.a.c. or palette at the end of the current address cycle; companion data from B is latched and the sequence repeated.

It can be seen that nearly two clock cycles are available for memory access and that this results in a minimum throughput of 13.3MHz for 150ns rams. In practice, performance is likely to be considerably better.

During read, data on the bus is latched in the d.a.c. (or colour palette) and displayed as a frozen image.

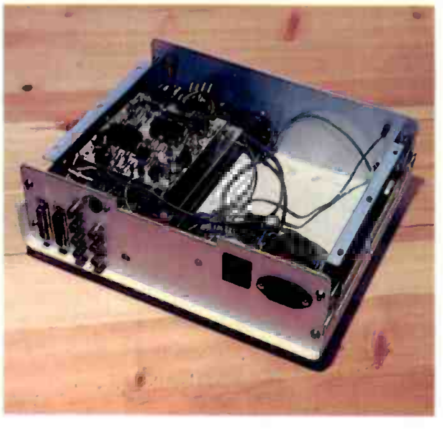
POWER SUPPLY

Power requirements for the frame store are modest: +5V at 600mA and +10V at 150mA (with colour palette and 256K ram). But an extra margin is desirable to accommodate future enhancements.

The provision of a negative rail (Fig.25) is a small overhead which increases the range of applications for the power supply p.c.b. The +5V rail can supply up to 1.25A (with 12 – 0 – 1230VA transformer). The 10V rail is adjustable over the range 9V to 13V with current-limiting set at about 250mA. The −5V rail could be used as a cheaper alternative to the on-board voltage converter on the signal processing board; otherwise, components around IC_3 can be omitted.

SETTING UP

The unit was designed for modular assembly with the major functional blocks on separate boards. Interconnections should be short with good inter-board grounding. Board layout is generally uncritical although the usual precautions such as separate



Printed circuit boards for this design will be available by the end of January from Ipswich Electronics Ltd, Hadleigh Road Industrial Estate, Ipswich IP2 0HB, tel. 0473-216056.

analogue/digital grounding and h.f. design rules should be applied to the converter circuitry. The first prototype worked well on breadboard.

Provision of front panel controls and indicators will depend on your application but I found the following quite useful:

- switchable video input impedance (R_1) for video busing
- separate sync (replace Link 4 on the converter board with a front panel switch.)
- internal video source selection switch
- field selector switch in 512×512 mode (fit a two-way centre-off switch S_{102} as indicated in the control diagram)
- freeze switch (S_{101}) and/or jack socket
- field sync selection (replace Link 1 on the control board with a two-way front panel switch)
- led for flagging external c.p.u. activity (see control diagram)

The converter circuitry is initially set-up in isolation by grounding the blanking input and latch enable $IC_6(1)$ from the control board. A t.t.l. clock of about 6MHz should be applied to CK_1. Connect the internal video source at R_1 and a monitor at R_{35}. With all pots initially centred, adjust the sync slicing level with P_1 until a synchronized white square appears in the centre of the screen. Video input levels for the a.d.c. $IC_5(1)$ are then set by P_2 and P_3.

The objective is to set the signal black-level (P_2) equal to or slightly above the low reference voltage V_{refL} and the peak-white amplitude equal to, or slightly below the high reference voltage V_{refH} (P_3). These levels can be approximated by observing the displayed picture and adjusting P_3 for no peak-white clipping and P_2 for minimum black-level pedestal; it is an iterative procedure. Optimum settings can be obtained later by software observation of the frame memory with a source giving calibrated areas of peak-white and black (such as a crosshatch generator).

The control circuitry is now set up in conjunction with the converter board. Links on the control board should be configured as given in Table 1 and the c.p.u. control inputs left floating. In 256×256 and 512×512 modes, a blanked border surrounds the displayed image.

The aspect ratio is set by adjustment of the clock frequency with C_{105} and the display horizontally centred with P_{101}. Fine tuning of the vertical display position is achievable by connecting $IC_{111}(10)$ to another output of IC_{115} (or +5V) to add or subtract lines from the vertical blanking period.

Odd/even field selection (with standard sync) should be set up with S_{102} in the ALT position (interlacing) and P_{102} adjusted for a 25Hz clock at $IC_{114}(5)$. Then P_{102} should be set to the centre of the range over which 25Hz toggling occurs. Switch S_{102} can now be used to select odd field (IC_{114} pin 5 low) or even field (high).

Details of link options 1 to 9 on the control board were set out last month in Table 1. Link 10 allows the host c.p.u. the possibility of field-synchronized access to the frame store. This feature could be used for dynamic switching of the colour palette look-up table during the field blanking interval, or for identifying odd and even fields when capturing images.

Finally, when the links on the memory board have been set in the appropriate positions, the basic system is complete.

Activating the freeze switch momentarily will make the display alternate between live (digitized) and frozen images.

COMPUTER INTERFACING

Two ports are necessary for computer interfacing: a port with seven latched t.t.l.-level drivers with an optional input or interrupt for field waveform detection and a bidirectional eight-bit data transfer port. Both ports can be derived from a standard peripheral interface device. It should be remembered that the frame store is accessed in two distinct modes – read and write (read is the default mode when inputs are floating).

Six control inputs are used to access the frame memory. These are analogous to the corresponding internal signals.

- $\overline{\text{CK}}$ generates the memory controls and increments the horizontal address counter.
- $\overline{\text{LS}}$ starts the horizontal counter and increments the vertical delay and address counters.
- $\overline{\text{FS}}$ resets the vertical counters and enables the vertical delay counter.
- $\overline{\text{BLNK}}$ disconnects the internal signals and enables c.p.u. access; the display is blanked.
- $\overline{\text{WR}}$ sets write (memory update) mode.
- $\overline{\text{FSEL}}$ in 512×512 mode selects image field to access.
- $\overline{\text{SYNC}}$ is an optional status signal for synchronizing field capture or palette updating.

Timing constraints on these inputs are not critical. The limiting resistors with c-mos buffer IC_{107} provide excellent noise and crosstalk immunity. Switch S_1 should obviously be open for c.p.u. access and a video source must be connected.

SOFTWARE DRIVERS

I suggest that you create the following driver routines –

Unblank: called after memory access to unblank the display in freeze mode, preserving memory contents. If the colour palette board is fitted it should be re-initialized because the pixel clock is stopped during c.p.u. access.

Freeze: to freeze the display, the $\overline{\text{WR}}$ input should be de-asserted and a delay of 25ms initiated for the signal to be clocked on the next field sync transition.

Display: to display live video and continuously update frame store memory, $\overline{\text{WR}}$ is asserted and 25ms delay initiated.

The following routines set the frame store for c.p.u. access, blanking the display.

Setrd: to read image data, $\overline{\text{BLNK}}$ is asserted, $\overline{\text{WR}}$ is de-asserted and the c.p.u. p.i.o. is initialised for data input. A 25ms delay should be initiated for signal clocking on next field sync.

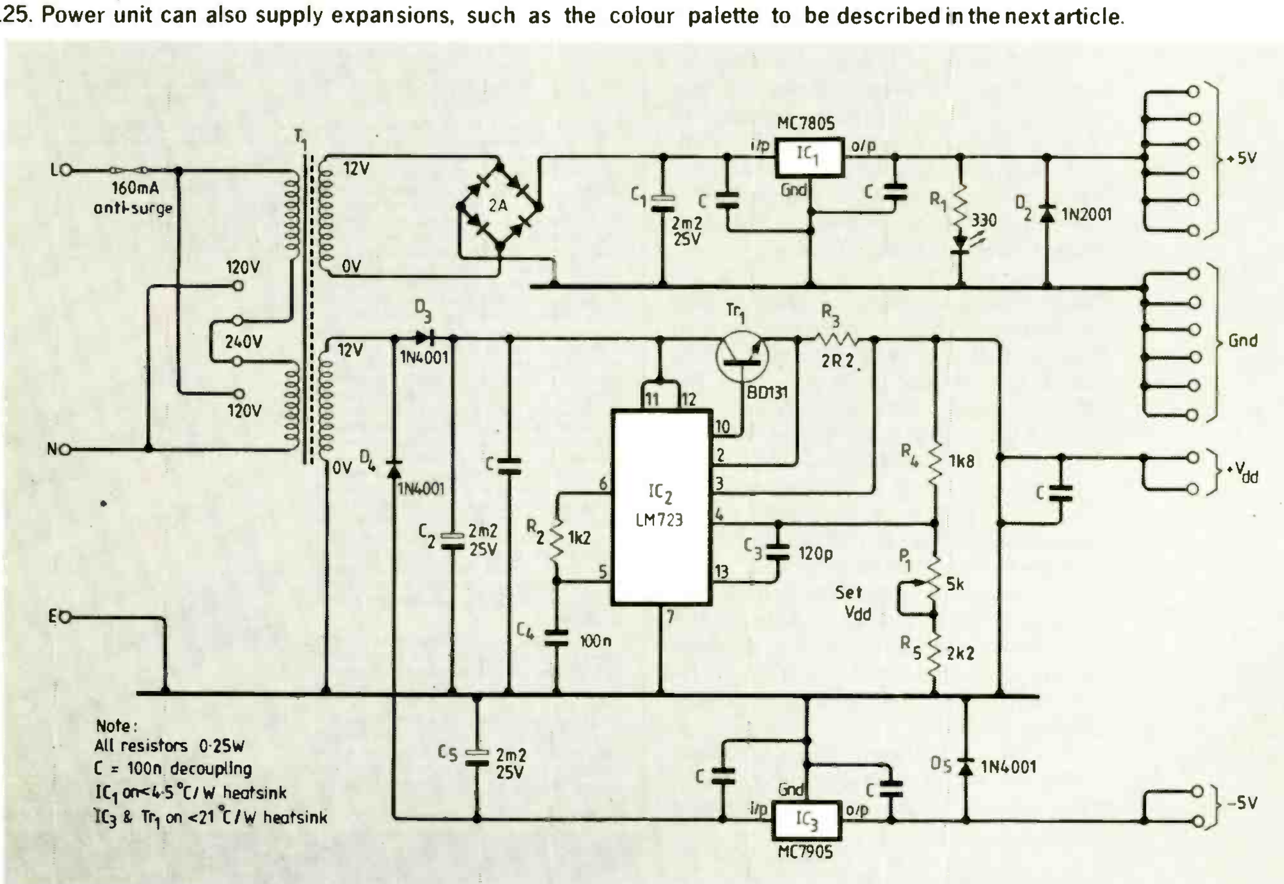
Setwr: to write image data, $\overline{\text{BLNK}}$ and $\overline{\text{WR}}$ are asserted and the c.p.u. p.i.o. is initialized for data output with a 25ms delay for field sync clocking.

For the following routines it is assumed that the appropriate frame store mode is selected as described above. The $\overline{\text{BLNK}}$ and $\overline{\text{WR}}$ inputs should remain in their allotted states throughout the access sequence. How to achieve this in software depends on the c.p.u. Some processors and p.i.os allow bit-mode output which simplifies this type of control, but otherwise you will have to keep track of port bit-status with a memory or register variable. A variable called Mode, to keep track of access mode (i.e. read or write), will be useful for simplifying and speeding up the code.

Line: this routine resets the horizontal address counter and advances the vertical delay counter. The $\overline{\text{LS}}$ line is pulsed low then high and a delay of about 30 microseconds initiated to allow time for the horizontal delay monostable to time out.

Clock: this routine causes memory to be written or read depending on the access mode; the horizontal address counter is advanced every alternate cycle. The $\overline{\text{CK}}$ input is pulsed low then high. Data should be output in write mode prior to this operation;

Fig.25. Power unit can also supply expansions, such as the colour palette to be described in the next article.



```
PROCEDURE TESTPATTERN

CONSTANT
 DISPLAYFORMAT = 256;  (256x256 mode)

BEGIN
    SETWR;          (initialize port and set WRITE mode)
    RESET;          (reset all address counters)

    FOR Y := 0 TO DISPLAYFORMAT - 1 DO
     BEGIN
       FOR X := 0 TO DISPLAYFORMAT/2 - 1 DO
         BEGIN
          OUTPUT (DATAPORT) = 0;  (pixel=black)
          CLOCK;               (clock memory)
          OUTPUT (DATAPORT) = 255; (pixel=white)
          CLOCK;               (clock memory & address)
         END;
       LINE;
     END;
    UNBLANK;         (disable c.p.u., leave image frozen)
END.
```

```
PROCEDURE DUMPIMAGE

CONSTANT
 DISPLAYFORMAT = 256;  (256x256 mode)

BEGIN
    SETRD;          (initialize port and set READ mode)
    RESET;          (reset all address counters)

    FOR Y := 0 TO DISPLAYFORMAT - 1 DO
     BEGIN
       FOR X := 0 TO DISPLAYFORMAT - 1 DO
         BEGIN
          PIXEL := DISPLAYINPUT (DATAPORT);
          ANYDEVICE( PIXEL );
          CLOCK;     (clock memory/address)
         END;
       LINE;
     END;
    UNBLANK;         (disable c.p.u., leave image frozen)
END.
```

in read mode data is available *before* clocking.

The efficiency of this operation significantly affects the overall display memory dump time. It is therefore desirable to optimize the code to perform this function. In the absence of a convenient hardware pulse, two port writes will be required and it is worth making the operation an assembler macro rather than a subroutine.

Reset: clears and primes the address counters for memory access: $\overline{FS}$ is pulsed low then high to reset the vertical counters and to enable the vertical delay counter. The routine Line is then called N times to advance the vertical delay counter, where N depends on the outputs of IC_{115} decoded by $IC_{111}(8)$; e.g. for $CI_{111}(10)$ connected to $CI_{115}(5)$, $N=(4+32)=36$. If you get it wrong, accessed data will be vertically displaced.

The generalized programs above illustrate the use of these routines. The first fills the frame store memory with alternating vertical black/white lines, useful for checking operation/performance. Below it is a procedure which dumps the frame memory to an arbitrary device.

Once the basic driver routines have been tested with simple programs such as these, you are ready to proceed with your own applications software.

to be continued

EARLY TV

British Television: the formative years by R.W. Burns. IEE History of Technology series 7, Peter Peregrinus in association with the Science Museum, London; 488 pages, hard cover, £38.40. Detailed academic history of the medium from Baird's early experiments to the establishment of the Marconi-EMI electronic system and to the suspension of the service at the outbreak of war in 1939, with many photographs and drawings. Absorbing reading for Baird-watchers, since inevitably much of the content deals with the Scottish inventor's endless squabbles with the General Post Office and the BBC; Professor Burns has much more patience with him than others have shown. No doubt it was clear to many that the man was caught in an evolutionary blind alley and that his spinning discs offered no possibility of a service with real entertainment value; but it was hardly dignified of P.P. Eckersley, the BBC's chief engineer to prejudice his Board against the system before they had seen it working. Inevitably, the reader is left filled with admiration for Shoenberg, Blumlein and the rest of the EMI team, who conjured up what is essentially the television standard we have today in the space of a few months.

Baird, incidentally, showed great animosity towards his rivals, which he saw as an American-inspired (EMI had access to RCA patents) campaign to undermine his all-British invention. A parable for our time?

Was this the article that set Baird thinking? It appeared in *Wireless World* in 1922 whilst he was in Hastings recuperating from illness and some exhausting ventures in the grocery trade. Two months later, his first television experiments were reported in the local paper.

NOVEMBER 11, 1922 THE WIRELESS WORLD AND RADIO REVIEW 197

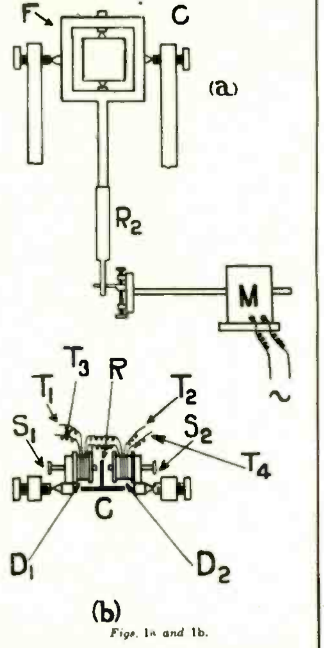
A Development in the Problem of Television.

By NICOLAS LANGER.

The following article, contributed from Hungary, describes experimental work in connection with the problem of Television. Whilst the actual process described does not include transmission by wireless, yet this being a logical development from line transmission, the subject as presented should be of great interest to wireless experimenters.

THE purpose of the following article is to describe a development in methods for enabling objects at a distance to be seen by the eye by means of electrical circuits or by wireless, in much the same manner as the ear is enabled by means of these methods to hear sounds at a distance. The problem of television has been already partly solved by the methods adopted by Professor Korn. Professor Korn's apparatus, however, relates only to the transmission of photographs, and the process takes from six to fifteen minutes, and the method is not a direct one, but one which necessitates taking a photograph in the ordinary way and afterwards reproducing it by means of the Korn apparatus. The following article will describe apparatus by means of which distant objects can be made visible without the necessity of the use of the intermediary of the camera, and it is even possible to represent at the receiving end pictures in motion in a similar manner to the cinematograph. It is claimed that in this system it is possible to transmit a picture at a speed exceeding that of the Korn transmitter by 10,000 to 20,000 times. The very interesting nature of the problem attracted my attention many years ago. The results of my investigations are no doubt of interest, and I will therefore give here a short *résumé* of this work in order to introduce the subject intelligibly.

Every picture (if we disregard the colours) may be regarded as consisting of a combination of black and white spots, and for the sake of simplicity, throughout this article, we shall term these spots "picture elements." It is easily understood that these picture elements vary in brightness from black down through gradations of tone to white. In order to set about transmitting a picture, we must first analyse the picture into elements, and the area of each element or spot must be sufficiently small so that no difference in tone would



Figs. 1a and 1b.

Domesday discs

Just nine centuries after William the Conqueror's men completed the original Domesday Book, the BBC launched its Domesday laser-disc system in November following two years of energetic information-gathering and technical development.

Contained in the two 30cm silver discs is a snapshot of Britain in the 1980s in words and pictures, an immense work of reference which the BBC hopes will prove as valuable to present-day researchers as it undoubtedly will to future historians. It's estimated that to look through all 108 000 pictures and 648M-bytes of data would take seven years.

For reading the discs, the BBC and its partners Philips, Logica and Acorn Computers have developed an interactive system based on a laser disc drive and a BBC Master series microcomputer. A version for the RML Nimbus computer is available and a universal IBM p.c. equivalent is on the way.

A feature of the system is that it is designed for people who have no knowledge of computers. Using the tracker-ball and on-screen pointer for control, even unskilled users can quickly move about the database and locate or manipulate information. They can search the discs through menus, by keywords, cross-references or just by browsing at random. At each stage, a menu bar appears on the screen showing possible options. Use of the keyboard is kept to a minimum.

On the first disc, the National Disc, is information about the British economy, culture, society and environment – much of it taken from official information stored in Essex University's archive of machine-readable data.

Works of art from the national collections and examples of British wild life are included in the 22 000 or so still photographs on the disc. Certain sets of pictures can be used interactively to simulate a visit to some typical British environments – such as a farm, a nature reserve, or even a stockbroker's house. The user can explore each one in detail by moving from one scene to another with the tracker-ball.

Over 6000 sets of statistical data are stored in the form of arrays. They can be processed under the user's control and plotted in a variety of forms – such as bar-charts, pie-charts and overlays on maps.

On the other side of the disc is an hour of moving pictures and sound, including memorable news events such as the ending of the Iranian embassy siege in 1980.

The second disc, described as a people's database, includes information contributed from all over the United Kingdom by schools and community groups and compiled under the direction of an independent editorial board. Providing a framework for it are thousands of detailed Ordnance Survey maps.

With an astronaut's view of the entire country as a starting point, it's possible to zoom down through successive levels of maps to arrive at one-inch scale or, in the case of 70 cities, to large-scale maps covering areas only 800 metres across. At each level the user can break off to see high-quality colour photographs, to study specially-commissioned articles written by authorities on each area or topic, or to read contributions from countless ordinary people about their locality or way of life.

Alternatively, you can type in a place-name and the system will find it for you in the text or on a map – supplemented once again with pictures and articles. Armchair travellers can 'map-walk' where they wish, and can even measure distances and areas with an on-screen cursor.

Retrieval software was written in BCPL by Logica. The discs carry some 200K of code, or about 67 000 lines, read in as overlays.

The control computer is a BBC Master AIV, which includes an s.c.s.i. interface and the Acorn 65SC102 co-processor; virtually every byte in its memory is needed. Output from the RGB socket is merged with video from the laser-disc player (which has its own s.c.s.i.) for connection to the monitor.

To handle the player, the BBC computer has a videodisc filing system (in a 16K rom) which enables it to read the data as files rather like those of the Acorn ADFS.

It's possible to break out of Logica's user-friendly software environment to examine the files at system level: on the National disc, it turns out that there are 41 (including a boot file) and that they occupy 226 277 376 bytes. More than 100 megabytes remain free, which should allow plenty of room for the updates the BBC is thinking of providing System calls are provided to allow programmers to access pictures and data directly so that they can write their own retrieval software.

The Domesday system is the first interactive database of its kind on public sale and the BBC now hopes to establish it as a standard for others to adopt. Early in 1987 it plans to issue a further disc, an educational study in ecology. Other information publishers have already shown interest in the new medium.

A complete Domesday system including colour monitor costs £3990 plus v.a.t., though schools can take advantage of Government grants and subsidies worth about £1000. An upgrade kit for existing BBC Master computers costs £3555; the discs alone are £230. The very first system has been presented to the Public Record Office in London, where the original Domesday Book is kept.

Details from BBC Enterprises Ltd, Woodlands, 80 Wood Lane, London W12 0TT; tel: 01-743 5588.

Deciding h.f. radio's future

With international broadcasting still expanding unabated, this month's WARC promises to be the hardest-fought yet – and maybe the most political.

D.P. LEGGATT

Under construction: a new BBC relay station at Hong Kong.

World Administrative Radio Conferences (WARCs) take place fairly frequently under the auspices of the International Telecommunications Union (ITU). An individual WARC is usually concerned with one sector of the radio spectrum – l.f./m.f., h.f., v.h.f., u.h.f. etc. – or with a particular application of radio communications such as land mobile use.

With one significant exception, the ITU plans the use of all radio frequency bands, from 9kHz to 400GHz at present, allocating segments for specific purposes and allotting particular channels to individual countries. ITU membership has international treaty status and nearly all countries of the world are signatories. A number of territories, mostly small, are not ITU members; but they include Taiwan, which is among the ten largest shortwave broadcasters.

The h.f. (short wave) broadcasting bands are the only frequency segments which are not planned by the ITU. Efforts have been made to do so since 1947, but all have foundered on the very significant excess of requirements over available capacity in the bands. Countries have not, on the whole, been able to agree significant reductions in their requirements.

The existing approach to international control of h.f. broadcasting is embodied in Article 17 of the ITU Radio Regulations. This amounts to little more than a requirement for countries to state their broadcasting intentions (frequencies, powers, target areas, programme times) for the coming seasons. These individual intentions are collated by the International Frequency Registration Board (IFRB) into a 'Tentative High Frequency Broadcasting Schedule' from which all countries can at least deduce what interference they may expect to receive from others. No specific action is called for and Article 17 is largely a vehicle for registration and exchange of information.

Article 17 was first formulated in 1959, originally as Article 10. During nearly 30 years of its operation there have been major and continuing increases in the global amount of h.f. broadcasting, in the number of countries participating and in the powers of h.f. transmitters. Consequently the amount and severity of interference has steadily risen, much of it apparently deliberate; and there has been increasing incidence of out-of-band broadcasting.

WARC-HFBC

A further attempt is now being made to bring more effective international control into this area. The first session of a WARC on h.f. broadcasting took place in 1984, with the second to be held in Geneva for five weeks during February and March 1987.

The first session agreed the following statement of planning principles:

> "In accordance with the International Telecommunications Convention and with the Radio Regulations annexed thereto, the planning of the high frequency bands allocated to the broadcasting service shall be based on the principle of equal rights of all countries, large or small, to equitable access to these bands."

Other agreements at the first session set out technical criteria for broadcast services, such as minimum field strengths and interference protection ratios in reception and, in cases where a frequency channel of adequate quality has been assigned, discouragement of further frequency channels carrying the same programme to a given target area.

With these principles and criteria as a basis, the conference outlined a planning method whereby countries would list their requirements with all necessary details, including any equipment constraints such as ability to operate only in a particular frequency band or on particular fixed frequencies.

The requirements of all countries would then be collated into a single schedule and the appropriate frequency band selected for each requirement. Requirements would then be examined for incompatibilities and remedial measures applied to relieve any apparent congestion. These measures were to include progressive reduction in the protection from interference, followed if necessary by reductions in the number and durations of individual countries' services during congested periods.

A significant general requirement of the planning method was that the system must be optimized to ensure the maximum possible use of all available channels.

The first session of the conference requested the IFRB to develop computer programs for applying the planning method, test the results and prepare a report in time for the second session in 1987.

THE IFRB PLANNING SYSTEM

The IFRB has now produced its computer-based system, necessarily filling in details where the outline planning method was not specific.

The system first examines each frequency band hour by hour to determine whether congestion exists. If there is none, broadcasters' requirements can be met on the basis of high-quality service with co-channel protection ratios of 27dB or better and adequate margins to allow for fading and multiple interference.

If the number of required channels exceeds the number of channels available in any band-hour, then there is congestion and measures to resolve it are applied. Interference and fading allowances are progressively reduced, down to a co-channel protection ratio of 27dB at this stage.

If this reduction of technical standards fails to resolve the congestion then a series of 'suspension rules' is brought into play. The first three rules, N1 to N3, suspend frequency requirements in a given band which appear to duplicate a country's service to a given target area. Simultaneous services from one country to any given target area are regarded as duplications, even though they may be in different languages.

Rule N5 suspends requirements to transmit simultaneously from one country to a given target area in more than one frequency band. The requirement in the most congested band is suspended, even though the other band or bands may not be the best on propagation grounds.

Rule N4 does not suspend any of the requirements but further reduces the co-channel interference protection ratio, down to a value of 17dB if necessary. To put these measures into perspective, it can be said that a signal-to-interference ratio of 27dB represents good quality reception; a ratio of 17dB might provide just-acceptable service in the context of shortwave broadcasting where interference-free reception cannot often be enjoyed.

If congestion still remains after the application of rules N1 to N5, then rule N6 is applied. This reduces transmission time down to a minimum of 30 minutes in each congested hour. Thus, for example, a two-hour requirement may be cut down to two non-consecutive periods of 30 minutes each.

If congestion persists despite all these suspension procedures, interference protection ratios are further reduced, without limit, until congestion is resolved.

FREQUENCY ASSIGNMENT

With congestion resolved, the next step is to assign frequencies. Attempts are made to preserve frequency continuity for the duration of a requirement and between consecutive requirements, recognizing also any requests for preferred frequencies and any frequency constraints due to equipment limitations.

If it proves impossible to assign frequencies to all requirements, frequency continuity and preferred frequencies are disregarded.

As a final step, requirements which have been suspended are re-inserted into the system to see whether they can be fitted in with no interference protection and without adverse effect on requirements already included.

IMPLICATIONS OF THE PLANNING SYSTEM

One of the most significant implications of the proposed system is that governments would lose their existing sovereign right to decide what services should be broadcast in the h.f. bands, to whom and when. Requirements of all countries would be taken fully into account by the system, but the final determination of what could be broadcast would rest with the IFRB planning system.

During the past year the system has been tested with a set of requirements submitted by ITU members. Taking a very global view, covering all frequency bands and all hours of the day, this first plan manages to assign frequencies to about 73% of requirement-hours; and of these requirements with assigned frequencies, 60% have signal-to-interference ratios equal to or better than 17dB.

These overall figures conceal some very different patterns when particular bands and hours are considered.

For a worst case we can look at the 6MHz band in the most congested hour, 23.00 GMT. To satisfy all requirements with good technical quality, a total of 293 frequency

BBC Far Eastern relay station at Kranji, Singapore.

channels would be needed, whereas only 25 are available. Only 40% of requirement hours can be assigned a frequency and of these only 5% have signal/interference ratios better than 17dB; 49% have negative ratios, indicating interference greater than the wanted signal.

Another disturbing feature of the plan is that many requirements, although given frequency assignments, do not enjoy time or frequency continuity. Transmission periods may be fragmented into discontinuous 30-minute blocks and one or more frequency changes may be entailed.

An unfortunate example is that of one small country which wishes to broadcast continuously for 18 hours per day. The plan does indeed satisfy the requirement with frequency assignments covering the whole period – but with a change of frequency every hour throughout the 18 hours.

IS THE PLAN WORKABLE?

The disagreeable consequences of the plan stem mainly of course from the inescapable fact that many more people want to do shortwave broadcasting than there is room for in the available bands.

Nevertheless, it may be argued that a major shortcoming of the plan is that it is too much influenced by the conference's exhortion to ensure maximum possible use of all available channels; it is this that leads to a preponderance of time and frequency discontinuities. The system seems more geared to the requirements of a point-to-point communications network where professional receivers and operators are available to cope with frequency changes, rather than to broadcasting where the listener will have difficulty in quickly re-locating a programme on a new frequency.

Some smaller countries may have high hopes that a new planning system will offer them readier access to clear channels in the h.f. bands. But no broadcaster, large or small, will find it easy to accept the loss of audiences which time breaks and frequency changes would entail. Indeed, the rapid frequency changes would be difficult for the broadcaster to implement without a standby transmitter which many might not have available.

ADDITIONAL CAPACITY

A few developments are possible which could increase the capacity available for international broadcasting.

- At some future date it might be agreed that additional h.f. spectrum be allocated to broadcasting, particularly in the form of extensions to the heavily congested 6MHz and 7MHz bands. Welcome though this might be, it cannot be expected that extensions could be great enough to do more than slightly ease existing congestion.
- Single-sideband working could offer a useful increase in channel availability. But the provision of cheap and stable s.s.b. receivers poses formidable problems and it would be very many years before the existing world stock of d.s.b. receivers could be considered to have reached the end of their useful lives.
- There is the possibility of direct radio broadcast from satellites. This could provide a useful although limited increase in available channels; but again the question of receiver cost rears its head. If, on the other hand, low-power communication satellites are envisaged, it must be remembered that reception and local distribution would be possible only with the co-operation of the authorities in the receiving area.

These developments seem likely to offer useful extras, but not to solve basic problems.

A different kind of effective increase in spectrum capacity would be afforded by the cessation of jamming. Countries which suffer jamming tend to respond by transmitting their programmes on several frequencies simultaneously, which are all jammed in due course; so the channel losses due to jamming are cumulative. But this of course is a political matter which an IFRB plan cannot take into account.

PROSPECTS FOR 1987

It is clear that the 1987 second session will hinge as much on political considerations as on technical aspects and it might well be concluded that the proposed planning system will not do as it stands. The outcome cannot easily be foreseen.

Pat Leggatt is the BBC's chief engineer, external relations.

Japanese displays reflect UK shortfall

"The UK had a two to three-year lead in this technology but this lead has been totally dissipated by indecision about potential commercial exploitation"

The findings of a DTI-sponsored fact-finding visit to Japan offers some sobering thoughts to the British industry. "Japanese companies are mounting greater efforts in research especially on active-matrix l.c.ds, and at the same time have enhanced their ability to develop very rapidly products based on ideas from anywhere in the world." So says John Raines of the electronic application division of the DTI, during last December's seminar, reporting on the visit. The British delegates attended the Japan Display Conference, the Japan All-Electronics show and visited several flat-panel display manufacturers. Members of the delegation reported on some aspect of the visit relevant to their specialization.

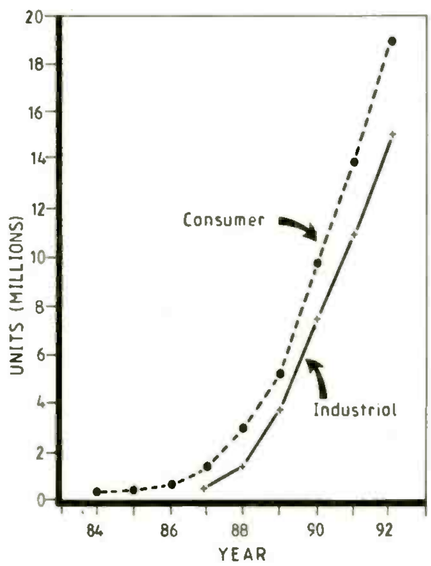
SUPERTWIST

Two impressive and significant flat-panel developments are the colour active-matrix l.c.d. tv and the A4-size supertwist graphics display. Long-pitch cholesteric liquid crystal cells incorporating pleochroic dyes were the first type of supertwist displays to be reported and patented in 1983 by researchers at RSRE Malvern. Subsequent work by Brown Boveri in Switzerland led to the discovery in 1985 of another type of supertwist device based on the supertwisted birefringence effect (s.b.e.). The s.b.e. is a solution to the task of electrically driving l.c.ds at high multiplexing levels (64).

A number of Japanese l.c.d. companies have been quick off the mark to develop the supertwist effect, and are now marketing – within a space of 18 months – large, (A4) l.c.d. graphic panels with 400 by 640 formats, working at duty cycles between 1:100 and 1:200. Supertwist panels are proving to be the answer to the portable computer industry's – and other's – prayers for a c.r.t. replacement, and are expected to become a major seller in the future.

Like a number of other good ideas, the supertwist effect is one of the latest pieces of l.c.d. research to be successfully exploited by the Japanese. In contrast, efforts by UK l.c.d. companies have been sluggish in comparison and hampered by the usual low levels of investment or through failure to appreciate the significance of the s.b.e., caused to some extent by being component and not producted.

Because of inherent restrictions of colour and speed, many Japanese companies regard supertwists as a stop-gap solution, to be



Projected world demand for active matrix displays

superceded by either the ferroelectric or a cost-effective active-matrix l.c.d.

Supertwist displays use at least twice the molecular twist of standard twisted-nematic devices and be classified into the s.b.e. display with 270°C of twist; and the supertwisted nematic (s.t.n.) display which can be configured between 180 and 260° depending on the required multiplexing level.

In addition to these developments, much effort has been directed toward providing flat fluorescent back lighting. Combined with the appropriate filters they can be used to more nearly reproduce a printed page by overcoming the yellow or blue appearance of these displays.

Research programmes are concerned with developing saleable products, where a detailed understanding of the fundamental physics is seen as a means to an end. Once a research programme has been agreed, manpower and funding are allocated which in general are both greater than those available to a British company. A pilot line producing pre-production devices for demonstration is usually larger than the biggest UK l.c.d. production line.

ACTIVE MATRIX-ADDRESSED DISPLAYS

All of the major Japanese display manufacturers have research and development programmes on active matrix l.c.ds addressed by thin-film transistors (t.f.ts). These are chiefly intended for use in portable/pocket tvs: 2 to 3in diagonal pocket tvs are already available at about £250 from Seiko-Epson and Matsushita. All but one of the t.f.t. l.c.ds used amorphous silicon as the semiconductor. The exception was Seiko-Epsom who use polycrystalline silicon which has the additional advantage of possibly being used to integrate peripheral drivers. All the devices were based on the twisted nematic effect, they all contained RGB filters and were illuminated by a specially developed backlight.

The general belief in Japan was that these displays would be limited to eight to ten-inch diagonals because of production costs and yields. However Seiko-Epson has already demonstrated a projection system which produces a display with a one-metre diagonal. A demonstration display which contained many defects but still represented a "remarkable achievement" was a 14in display by Seiko Instruments.

Drs Migliorato and Moseley of GEC Hirst agree that "The Japanese are committed to the large-scale production of active matrix displays but the traditional step-by-step approach to research and development adopted by Japanese companies may prove to be unsuccessful and innovations by companies in Europe may be needed for their successful large-scale production. The advantages to the UK in this case should not be lost because of lack of investment."

FERROELECTRIC DISPLAYS

Japanese research into ferroelectric l.c.ds is limited by the available liquid crystal materials. The technology has proved more difficult than twisted nematic devices, but high-resolution demonstration cells are now being made. Some problems still need to be solved before manufacture can start. The displays are fast bistable devices with virtually unlimited resolution. Techniques used with other two-level displays can be used to produce a greyscale.

One of the drawbacks of these devices is that there is limited theoretical knowledge of how they work. Another is that very high-speed materials are needed, faster than those available commercially. Ferroelectric l.c.ds require different surface treatment from other displays. The devices respond to d.c. rather than a.c., so new drive schemes have to be developed.

Under the UK's JOERS/Alvey programme

small-area test displays using ferroelectric materials have been demonstrated. They have achieved much faster change rates than Japanese versions and video rates appear to be feasible. It is aimed to develop the technology and demonstrate high-resolution panels by 1988.

DISPLAY MARKETS

Most of the market in terms of volume will be in tv and consumer applications, having a major impact on portable entertainment electronics, and this will be served primarily by colour active-matrix l.c.ds in sizes up to 8 or 10in diagonal. The current enthusiasm for twisted nematic and supertwist displays is likely to be short lived and be replaced by the active-matrix types, or by emissive displays such as electroluminescent or plasma. For the larger displays (up to 35in diagonal) these emissive types are likely to offer advantages over l.c.ds because of the power and size of the backlighting required for l.c.ds. For even bigger displays the l.c.d. again has the advantage when used in a projection system. Many companies are looking into liquid crystal light valves as a way forward.

JAPAN DISPLAY '86

The delegation attended the Japan Display '86 conference where liquid crystal displays had the largest proportion of contributions, with over a third of the papers. They covered all aspects of the field from colour filters and materials, through impressive active-matrix demonstrations to the more fundamental research being undertaken on ferroelectric smectic devices.

Nearly half of the liquid crystal papers were concerned with active-matrix displays. The first session on this topic followed the keynote address of Mr Sasaki of Sharp who had highlighted the role of 4 to 6in full-colour displays in the future generation of portable tvs and pocket information terminals. It isn't surprising therefore that this topic was supported well by Japanese contributions. It was clear from the type of contribution that the technology is maturing rapidly toward production with many papers concentrating on the product oriented research of increasing display size, improving thin-film transistor (t.f.t.) yield with redundancy and repair systems and achieving good greyscale performance. From GEC and LETI, in Europe, came some novel electrode geometries for displays driven from polycrystalline and amorphous silicon (αSi) t.f.ts respectively. The aim of these structures was to decrease the complexity of manufacture and potentially improve yield. The largest device demonstrated was a 14in αSi device, while the Hosiden 5in colour tv demonstration gave the best picture quality, colour and grey scale.

The papers on ferroelectric smectic C devices were at a much earlier stage than active matrix in the research and development cycle. All but two of the papers were from Japan; the other two being from RSRE (Malvern), reporting work from the Joint Optoelectronic Research Scheme/Alvey collaboration in the UK. Alignment of samples and their subsequent characterization were the major research tasks described and it was clear that the Japanese were building their own database of experimental observations.

In contrast to some of their previous displays work, they are intent on building some level of theory to explain their observations and not waiting for input from elsewhere. This is exemplified by a paper from Hitachi which has achieved true bistable switching of a thick cell based on its previous theoretical studies of the role of elastic constants of ferroelectric smectic materials on bistability.

Supertwisted birefrigence effect (s.b.e.) displays were already coming on to the market, and were considered as an existing technology; so papers concerning this were on enhancing the success – the fine tuning – of such devices. Two areas of effort were in improving the response time, and the alignment process that will allow larger twist angles and hence a higher level of multiplexing.

Hitachi reported further work on its laser-scanned smectic A device. It is developing a multi-colour system to give a 2000 by 2000 matrix and eight colours.

The overall impression of the conference, according to Dr Frances Saunders of RSRE, was that the Japanese companies are moving rapidly from research and development to production, particularly with active matrix and supertwist displays. Although no working demonstrations of ferro-electric smectic displays were on show, visits to several Japanese companies showed that this was an area of significant active development. The pace of l.c.d. technology in Japan is unabated and is outstripping both the UK and USA.

One area where the UK still had a lead was in liquid crystal materials research. Both material and display device research of such places as the University of Hull, RSRE, BDH, and STL would be considered very large even by Japanese standards. But the UK has fallen behind in manufacture and "if we are to compete with the Japanese in large-area display devices, we must vastly improve our capability to manufacture them, whilst maintaining our excellent material and device research", said Dr David Lacey of Hull. "Otherwise we have to export our materials, and once again we will have become victims of the great British disease; good at inventiveness but poor on application."

CURRENT STATE OF ACTIVE MATRIX L.C.C DEVELOPMENT IN JAPAN

COMPANY	SIZE mm^2	PICTURE ELEMENTS	COLOUR QUALITY	VIDEO DEMONSTRATED	DEFECTS	ACTIVE MATERIAL	APPLICATION	STATUS
Asahi Glass	100 x 100	250 x 250	Poor commercial filters	No	~25 point defects 4 line defects	αSi	T.V Car Dashboard	Pre-pilot
Fujitsu	120 x 90	(320x3) x 240	Poor commercial filters	Yes 16 grey scales	~50	αSi	TV	Pre-pilot
Hitachi	138 x 96	(200x3) x 640	Very good	No	None	αSi	TV & coloured VDU	Pre-pilot line
NEC	66 x 88	480 x 378 (240 x 252) RGB Trio)	Very good	No	?	αSi	TV & coloured VDU	Laboratory prototype
Seiko Epson	88 x 96	440 x (160x3)	Very good	No	None	Poly Si	TV	40 x 30 mm^2 TV on sale
Seiko Instruments	210 x 300	640 x (400x3)	Poor on this display. But good colour technology	Yes	~50 point defects ~10 line defects	αSi	TV & coloured VDU	Laboratory prototype
Sharp	65 x 48	360 x 240	Very good	Yes	~20 point defects	αSi	TV & coloured VDU	Have set up a production line
Toshiba	192 x 144	640 x 480	Very good	No	1 cm line defect	αSi	TV	Pilot line
Matsushita	254 x 192	640 x 480	?	Yes	?	αSi	TV	3 inch TV on sale
Hosiden	77 x 101 130 x 130	240 x 480 650 x 650	Very good Very good	TV No	None Part of line	αSi αSi	TV	On sale in 1 year
Mitsubishi	135 x 211	408 x 640	Very good	No	possibly 1 or 2	αSi	TV, VDU telephone	?

LESSONS FOR THE UK

From Japan, the UK is viewed as a valuable source of novel ideas, most of which are published openly as scientific papers. Overall benefit will only accrue to the UK if these ideas are rapidly exploited, in a full commercial sense. Patent protection is not very effective in this respect; companies will only stay ahead of the competition by moving quickly into production. This requires an enormous uplift in the UK's production capability and flexibility. Most Japanese research and development schemes have access to pilot and/or production lines. The pilot alone offers a capability greater than UK production lines.

- **To get back into the world market it is necessary to commit a minimum of £5m to £10m, with further investment required to build up to the projected Japanese level of production.**
- **One viable route for UK companies might be through joint ventures with Japanese companies. The UK can still offer significant contributions from its current research base. The Japanese can offer their development and production expertise.**
- **There needs to be more 'vertical integration' – the matching of components to the appliances which will use them. Many of the Japanese research efforts are run by the consumer product manufacturers. And the Japanese with large manufacturing bases are quick to incorporate new ideas into their products. UK manufacturers should do so too.**
- **The massive UK research into flat-panel displays would be wasted if the technology were not exploited. This requires the commitment of UK manufacturing companies.**

Packets all around the country

The Department of Trade and Industry has cleared the establishment of ten experimental amateur radio packet relay stations. These new relay stations extend the distances over which Britain's 57,000 radio amateurs can exchange short duration 'packets' of information. The new packet relay stations use high-technology hardware and software to enable a number of UK radio amateurs to operate on one radio channel. As a result, this type of transmission extends the use of computer technology in r.f. experimentation and leads to increased frequency usage.

Another first which comes with the introduction of the repeaters is the ability to pass communications from relay to relay around the UK. The Radio Society of Great Britain, who have planned a 14 month experiment with the DTI, believes that packet communication will eventually be possible throughout the UK with links via h.f. and satellites to similar national networks in other countries. Within the UK plans are in hand to provide microwave linked packet switching relay stations as a means of handling a greater number of messages. The satellite team at Surrey University plan to use their amateur radio and educational satellite (UOSAT II) to retransmit packets to overseas stations.

The packet system provides the opportunity for UK industry to develop and manufacture digital hardware and software and v.h.f. and microwave hardware. A new type of antenna has already been developed in the UK for packet radio. The availability of relatively cheap and powerful micro-computers can be combined with experimental radio technology thereby encouraging radio amateurs to develop their expertise in the most up-to-date methods of communications.

The Radio Society of Great Britain's packet relay station located at their headquarters in Potters Bar, Herts, was officially switched on by the DTI's Head of Radio Amateur Licensing Section, Barry Maxwell.

The little box on top of the radar monitor is a speech recogniser, Macrospeak from Marconi, and is claimed to have overcome the drawbacks of such systems. The unit can recognise 650 words and transmit them through an RS232 line to any v.d.u.-based computer system. This offers hands-free control of computer commands. The system has undergone successful trials as part of an aircraft control unit responding to commands from the aircrew.

Asic design agreement

ES2, the European consortium set up to produce application specific i.cs using a direct write on silicon technique, has signed an agreement with Sun Microsystems to amalgamate the ES2 Solo 2000 custom v.l.s.i. design system with the Sun-3 workstation.

Both parties are very pleased with the deal. Rod Attwooll managing director of the British branch of ES2 said: "Both ES2 and Sun are committed to the open systems concept and using standards such as Unix and Ethernet. Solo 2000 software in combination with the Sun workstation offers a flexibility, which in terms of power and cost effectiveness will prove unrivalled in the market place."

Bill Passmore of Sun Microsystems UK added: "It is very important to us to forge partnerships with companies offering advanced technology in order to continue to provide customers with the products that they need. We are very pleased that ES2 has chosen Sun to provide a platform on which to offer their products.

Solo 2000 is an integrated design system structured around a unified data base, built around the SDA v.l.s.i. toolset. It is designed to cope with the most complex circuits built from macrocells and yet has the ability to incorporate individually designed cells for special functions as well. The system is available in modules which can be added as required, and build up to a complete design, layout and test system for custom i.cs as well as semi-custom designs in both analogue and digital circuits. Sun produce Unix-based technical workstations which are sold to other manufacturers who add software and hardware to produce systems for cad, cam, artificial intelligence, software engineering, electronic publishing and automatic test equipment.

More electronics in York

The annual intake of students into electronic engineering courses at the University of York is to be increased from 45 to 70 as from October 1987.

This increase is made possible by a special allocation of funding announced by the University Grants Committee (UGC), which will enable the University to increase the staff and facilities of its department of electronics. The extra accommodation needed will be provided by a new building which will be erected close to the present Physics and Electronics Building. This new building will also house the York Electronics Centre, which is part of the department, enabling it to extend the design and consultancy services it provides to industry. The department of electronics took its first students in 1979. Since 1984 the annual intake of undergraduates has been 45, most of whom are sponsored by industrial firms, including 20 by British Telecom.

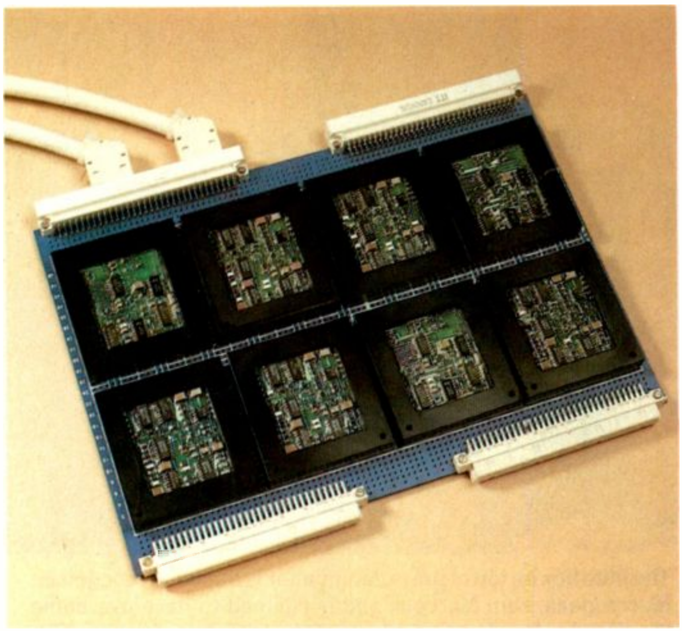
The continued growth of the department will also enable it to strengthen its research groups in communications (including electromagnetic compatibility), control (including flight control systems), microelectronic devices, and image and speech processing. The extra income has also made possible the introduction of a new course in avionics. In the recent review of all university departments in Britain by the University Grants Committee, the research work of this department was classified as outstanding.

Holographic airbourne display

Yet another form of head-up display (h.u.d.) for pilots is one developed by GEC Avionics. This uses diffractive optics (holograms) to provide the pilot with a wide field of view suitable for both day and night operations. Computer-generated symbols are projected into the pilot's forward view, making it unneccessary to look down at instruments.

This display is the latest in a series of GEC Avionics h.u.d. designs capable of presenting a raster (TV-like) display, as well as stroke-written (vector) symbols. The raster display depicts the night scene, as produced by a forward-looking infra-red (f.l.i.r.) image, superimposed exactly in scale and in the correct location, so that the pilot literally sees in the dark. In conjunction with the vector graphics symbols, this arrangement allows pilots to use, at night, the visual clues they normally use by day.

GEC Avionics first announced flight tests of night vision displays in 1971, with a system which has since seen long service with the United States Navy. This h.u.d., however, has a conventional field of view (the angles subtended at the eye by the boundaries of the display). The use of holograms, or diffractive optics, is to make the pilot's field of view much larger than is currently possible with conventional optical techniques, thus giving greater safety and effectiveness in low altitude manoeuvering by day and night. Apart from the large instantaneous field of view, (30°azimuth by 17°vertical), other important gains are provided by the new design. One of these is the ability to apply a computer-programmed correction to the displayed information, in order to optimise windscreen canopy corrections, augmenting techniques used in the optical system to ensure high accuracy over the total field of view.



This eurocard has incorporated a number of 'daughter' sub-circuits which are individually plugged into zif sockets. This aids testing and repair and is an example of hierarchical interconnect technology, mentioned in our feature last month as "the basis of the next generation of p.c.b. interconnect.

Communications standards centre

Work has started on setting up the first British information centre for communications standards. It will be located at the Production and Engineering Research Assocation (PERA), Melton Mowbray, which has been awarded a £1M contract by the DTI. Known as the ComCentre, it will provide information services and demonstration facilities to help manufacturing and process industry wishing to introduce Computer Integrated Manufacturing (CIM). MAP (Manufacturing Automation Protocol) and TOP (Technical Office Protocol) communication standards will top the list of priorities for the establishment of standards. As part of its information services, the centre will collect published materials from all over the world on communications standards and establish an on-line database accessible to all its members. It will also organise awareness seminars and conferences, training programmes and visits to company demonstrations, and will link with organizations involved in communications standards.

The ComCentre will be operated by PERA, the Institution of Mechanical Engineers and the Institution of Production Engineers.

Communications security and standards

There is a fierce battle by companies cooperating with the International Standards Organization to implement Open Systems Interconnect principles first and so become the standard implementation. The network systems business has vast potential to realize the OSI concept and the first product in the market stands to gain overwhelming precedence.

In this highly competitive arena, however, there stands the national standards organisations, writes Steve Cameron. Although the British Standards Institute (BSI) has published its own efforts in the field of information technology it has decided to support and adopt the ISO work on data security. The OSI philosophy, which points the way to how systems should be designed to communicate, disseminated seven layers, all of which may be compromised with respect of security, clearly indicating the problems of data security and integrity.

The Data Encryption Standard was approved for US government use nine years ago, being reviewed and re-certified after five years. It is now understood that it will not be re-certified when it comes up for review in 1988, and consequently government applications in commercially secure areas will be implemented using unpublished algorithms. This decision, although opening a larger market for secret algorithms, will prevent public awareness and scrutiny to point out possibilities of abuse.

The compromise of DES will no doubt come. The dependence that financial institutions have placed on such an algorithm must be reviewed.

The sturdy alternative and key-management-flexible RSA algorithm (after Rivest, Shamir and Adleman) following years of under-utilization in the shadow of DES, may now make its break-through as ISO adopt it as an international standard algorithm along with DES.

Credit-card data bank

A credit card sized "memory bank" which can hold up to 800 pages of text, eight photographs or a combination of both is to be supplied by British Telcom. A licence to sell the tamperproof cards, known as LaserCards, has been purchased from the Drexler Technology Corporation of California, which holds the patents.

The LaserCard makes available in a low-cost credit card format up to 2Mbytes of data. The data can be imprinted by photographic techniques at the time of manufacture or subsequently by low-cost lasers. The cards are intrinsically secure and difficult to corrupt either accidentally or deliberately. They are also cheaper and faster to produce than other data storage media such as floppy discs.

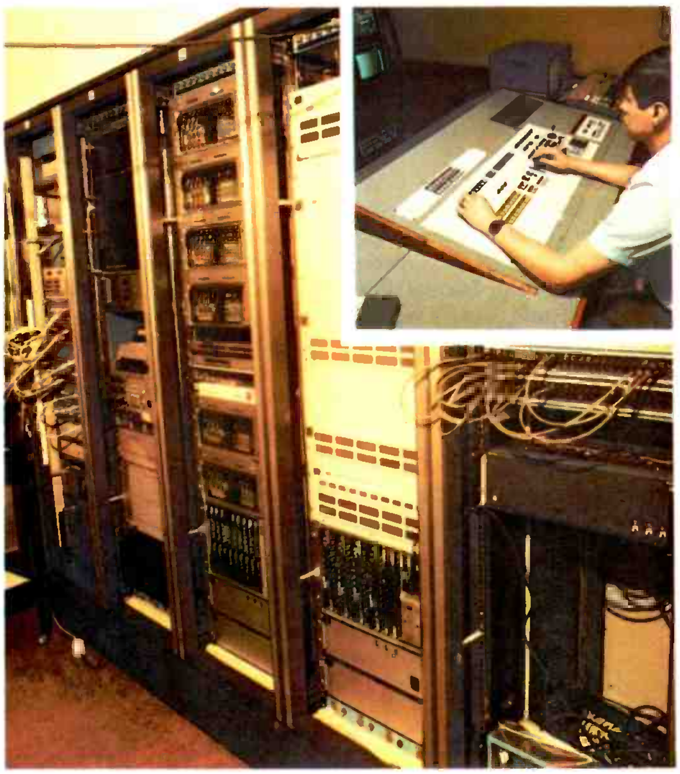
British Telecom is negotiating with a major London hospital which is considering the use of LaserCards for holding maternity records. Photographs of X-rays, sonic scans, and medical notes can all be held on the same card. Other fields where the cards have found application in the USA, Europe and Japan include financial payments and records, data collection, distribution and security. British Telecom anticipates that the combination of secure personal data record with the facilities of communications networks will lead to even more effective solutions to many of the requirements of information technology users.

British Telecom will also supply the equipment for recording and reading data on the cards. Currently these cards and the recording equipment are made in the United States and Japan, but there is a possibility of local manufacture, should demand in Britain merit it.

Digital tv studio

The Independent Television Companies Association (ITCA) has developed in its laboratories the first digital component video studio working entirely on the 'world standard' for studios and video recorders. The system has now been temporarily installed at Thames Television's studios at Teddington, where it is being assessed under operational conditions whilst further development is undertaken. The ITCA Technical Development Board has been developing the component parts of a complete digital video studio for over seven years. Funded by the ITV companies, the £1million project has reached a significant stage where it is now possible to record and edit a television programme using digital component techniques in place of PAL encoding and distribution.

The digital equipment operates on the parameters established by CCIR Recommendation 601 which are now more commonly referred to as the 4:2:2 system. The interconnection standard is the bit-parallel format specified in EBU technical document 3246.



Sources and codecs

Red, green and blue analogue output signals from three cameras and one telecine from Thames Television studios are converted to 4:2:2 (Y:U:V) digital components in ITCA-designed coders. Each coder contains a triple a-to-d converter and multiplexer; the corresponding decoder contains a demultiplexer and triple d-to-a converter. The RGB output of a slide scanner is similarly converted to 4:2:2 via a coder. An ITCA-designed PAL comb-filter decoder operating entirely digitally, has a 4:2:2 output. This provides a means of accepting PAL composite signals as sources where three are no alternatives (for example from archive recordings). Further sources include: an Aston-4 character generator which is 4:2:2 compatible, an Abekas Gemini field store which can be used as a synchroniser and as a transcoder between PAL or RGB sources and 4:2:2 and two Sony DVR1000 digital video tape recorders which have 4:2:2 output. A Tektronix component signal generator provides an alternative input to any one of the codecs for test purposes.

Routing switches

The system employs two routing switchers which have been developed by Pro-bel under an ITCA contract. Each switcher accepts eight inputs and provides four outputs. One switcher is dedicated to the digital mixer while the other one provides preview facilities, monitoring and input selection for the d.v.t.rs. Following the successful production of these 8 by 4 switchers, larger matrices are now under development. All cable runs in the installation are less than 1000 metres and the bit-parallel format was chosen for interconnection rather than the high frequency serial format. The parallel format also offered a more economic solution even allowing for the higher installation cost of the special twisted pair cables.

Mixer

The mixer, which is an experimental prototype, is the result of a long term development contract between ITCA and Abekas Cox (originally Michael Cox Electronics). The mixer architecture is based on the Cox T16 mixer system. However, in this case due to the limitations of the input matrix, there are only eight inputs supplying the preset and foreground/effects buses. In addition to a full range of wipes and mixes, the effects bus can operate in a number of modes including split screen, chroma-key, internal key and external linear or instantaneous key. Colour fill and border control is available with selectable hue saturation and softness.

All internal signal processing in the mixer is in 4:4:4 format. This uses a novel arithmetical process with pre and post-filtering to interface with the 4:2:2 buses. By using 4:4:4 within the unit the same precision of control of each component signal is achieved and this gives better processing than 4:2:2. Signals from each 4:2:2 bus pass through an ITCA-designed timing corrector to ensure precise synchronization of the input signals for processing. This is an important factor where signals are taken from various sources (as in this instance) and eliminates the need for precise source timing.

Field store and digital video effects

The Gemini field store was specifically modified by Abekas for 4:2:2 inputs and ouput. Its prime function is to produce a limited range of digital video effects for the mixer. The Gemini provides picture position manipulation, horizontal and vertical reverses, mosaic, quantization and freeze frame with adjustable rate. The field store may also be selected by the mixer for re-entrant multiple effects. All control connections for both the mixer and the video effects are via simple RS 422 serial interfaces. More complex video effects can be easily be added to the system.

Synchronisation

The normal sync reference distribution to the inputs of digital codecs (a-to-d and d-to-a converters); and source equipment are mixed sync pulses supplied from an Acron pulse generator locked to the Thames studio reference. Synchronisation of equipment at digital level is either through the sync pulse generator (s.p.g.), developed by Acron under an ITCA contract. This s.p.g. is capable of genlocking to a 4:2:2 signal and produces both digital and standard reference signals for monitoring purposes and for recoding the output signal to PAL if required.

Monitoring
Production monitoring use two colour monitors (one for preview and one for programme output) and eight monochrome monitors for sources. All colour monitoring is at RGB level, decoded from 4:2:2, whereas source monitoring is of luminance only, derived from the codecs or the source equipment. A separate RGB decoder is used for an engineering colour monitor, the input of which can be switched to monitor most of the other input and output signals.

Engineering tests
By a suitable choice of either RGB or digitally-derived test signals, conventional waveform monitors and oscilloscopes have been found adequate for testing and fault finding on the experimental system. However, a programme of development has been started to incorporate auto-testing and monitoring facilities within the system.

Sound
Currently, analogue sound signals are used in the studio but in the future digital audio will be incorporated, based on current development work in this area at another ITCA laboratory.

First d.b.s. licence

Last December the first 15-year British d.b.s. licence was issued by the IBA to BSB, a consortium founded by Granada, Anglia, the Virgin group, Amstrad and Pearson. This consortium was coordinated by Andrew Quinn of Granada who said that they hoped to begin a four-programme service on three satellite channels in 1990: Now, Screen, Zig-zag and Galaxy.

The consortium is now looking for a satellite. They are being advised by Telesat of Canada and talking to British Aerospace, Hughes, RCA and Eurosatellite about a five-transponder vehicle with output powers of 100 to 120W/channel with a standby spare vehicle in orbit. Adapters to receive the signals would cost about £200 and the dish antennae could be as small as 450mm or even 300mm in some areas. To overcome the problems of insuring the launch, they hope to buy (or hire) a vehicle in orbit.

BSB expects to have 400 000 viewing homes by the end of the the first year of operation; not including those who may get the programmes via cable. The five companies have committed £80M to the project with £120M being underwritten. Further investment is sought and the total cost is likely to be £500 to 600M before it starts receiving any profit.

'Screen' is a film channel to be offered to subscribers at about £2.50 a week. The three other services will be free advertisment-supported channels: 'Now' for news and current affairs, 'Zig-zag' for children and 'family' programmes, and 'Galaxy' for 'entertainment'. The usual IBA requirements on impartiality, balance, decency etc will apply but there is no requirement for d.b.s. channels to provide a mix of information, education and entertainment. It is not clear how the four services will time-share the three transponder channels.

In brief

Acorn Computers have won a major order to supply 1500 Master Compact and 200 Master 128 computers to a Polish mining cooperative. The deal is worth about £1M.

With their recent move to Milton Keynes, NEC Electronics have established a new design centre for semi-custom application specific integrated circuits (asics). In addition to increasing their investment in hardware and software their design team, led by design centre manager Bob Laird, has been increased to 14 engineers. NEC believe that they are able to offer more and better facilities for semi-custom asics than any major semiconductor manufacturer in Europe.

The combination of hardware, software and the design engineering team makes it possible for equipment designers with almost any level of experience in design and customised asics to use the new service. Various levels of design are provided, from NEC producing an i.c. from a customer's circuit diagram and test pattern to providing remote terminal access to NEC's computer, and within the constraints.

NEXT MONTH

Soldering technology. We examine the techniques used in mounting components on printed-circuit boards, from basic hand tools to industrial flow-soldering equipment.

Digital image processing. Two-dimensional, digital signal-processing techniques are used in data compression, enhancement and restoration. This article provides an overview of the technology.

Digital audio broadcast. Adaptive delta modulation is an efficient and practical method of broadcasting audio and stereo television sound via d.b.s., cable and terrestrial transmitters.

High-resolution c.r.t. drivers. The design of high-voltage, high-speed amplifiers for driving high-resolution colour tubes. The amplifiers possess wide small-signal bandwidth and excellent large-amplitude slew rates.

Mains control system. Following a recent piece on mains communications, we present an article on the remote control of equipment via mains circuits by means of a carrier current transceiver and microprocessor.

R.f. millivoltmeter. The design of an instrument to measure voltages down to 0.2mV in the frequency range 1kHz to 1GHz.

NEW PRODUCTS

COMPONENTS

Single array with 50000 gates

A series of 1.5µm c-mos gates has been produced by VLSI. The VGT100 series uses VLSI's Continuous Gate Technology which allows use of around 75% of the total gates on an array compared to only 40 to 50% for similar competitive products. The gates are constructed from continuous rows of P and N transistor pairs. The largest of the series, the VGT100 – 67000 array, has 66550 raw gates which produces 50000 usable gates.

The main advantages of the VGT100 series include high performance with a typical gate delay for a 2 input Nand gate of 0.7ns, i/o cells offering programmable output drive (2 to 12mA), flexible configurations for all pads, powerful design tools and an extensive library of more than 280 macros functionally equivalent to VLSI's standard cells. A key factor in VLSI's ability to achieve high transistor densities is the use of gate isolation. This does away with the 'traditional' thick field oxide to isolate cell structures. With VGT100 arrays, gate isolation is used which turns off P and N transistor pairs to isolate the diffusion nodes. This releases much of the 20% of silicon that was used for isolation in the past. Macros available for the VGT100 series include buffers, gates, decoders/multiplexers, adder/subtractors, multiplexed flip flops, synchronous counters, and toggle flip flops. Gate densities allow the VTG100 series to range from 9000 to 50000 usable gates. VLSI Technology Limited, Tel: 0908 667595.
222 on reply card.

New concept in asics

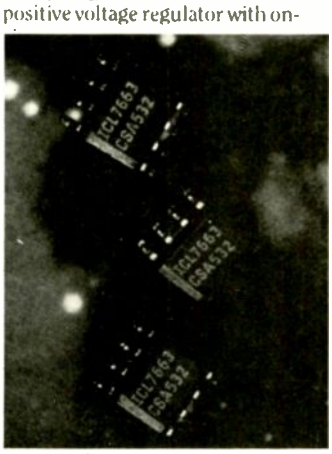
A new idea in application-specific i.cs has been announced by LSI Logic; the custom structured array. Called the LCSA15, the system uses compact 1.5µm geometry. The system allows the user to design a metal-programmable masterslice which can use a variety of memory and logic cells from a structured cell library and place them into a masterslice containing LCA10000 series Compacted Array gates. This allows a user, who may have several designs which contain the same basic building block elements, to gain quick turnaround time and low option cost on each new design.

Rick Rasmussen, manager of new product development at LSI Logic cited the following example: "Let's say a contractor had a basic design to sell to three different customers, but all three had their own specific bus interface. The contractor could put the design core into memory and megacells and build up a masterslice with a reasonable amount of blank LCA10000 Compacted Array gates. These can be incorporated into a single masterslice which contains his core function. The logic array section could be altered in three different ways, providing a final product which would meet the specifications of all three customers." LSI Logic Ltd, Tel: 0334 426544.
225 on reply card.

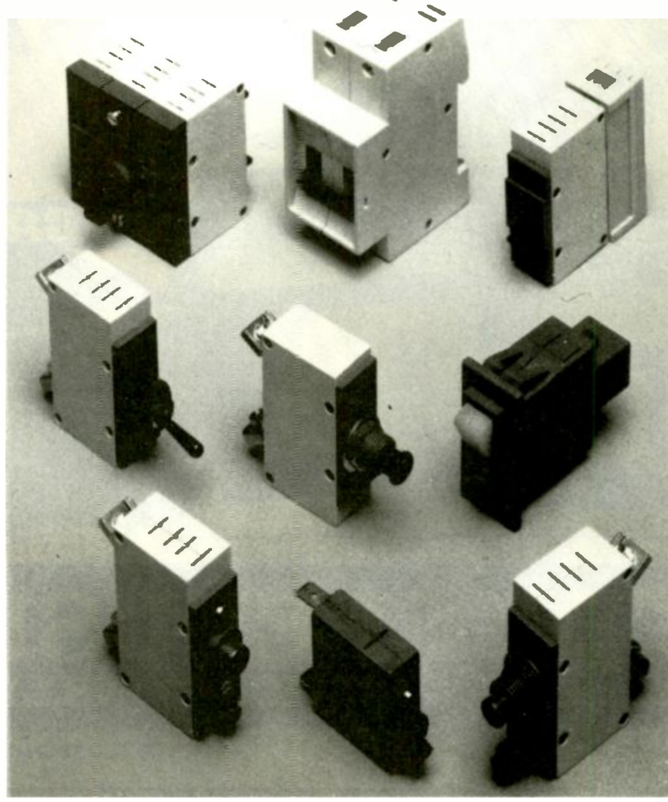
Programmable voltage regulators

Adjustment-free programmable voltage regulators – the ICL7663A and ICL7664A – are made by Maxim. They have a 1% reference voltage accuracy. This eliminates the need for potentiometers and calibration in most applications, which reduces board space and component cost. The new c-mos voltage regulators can be programmed from 1.3V to 5V using two external resistors which, if rated at 1% tolerance, will produce a 5V supply at 2.7% accuracy guaranteed over the full 0 to 70°C temperature range. The ICL7663/4 A and B all have guaranteed line and load regulation as well as input/output saturation resistance over the full temperature range. All are fully compatible with Intersil's originals.

Three new c-mos programmable/fixed regulators for batteries have also been introduced. They have quiescent currents of only 12µA maximum. MAX663 is a positive voltage regulator; MAX666, a positive voltage regulator with on-



chip low-battery detection; MAX664, a negative voltage regulator. All three devices have Maxim's "Dual Mode" feature, fixed 5V output or programmable 1.3 to 15V output with guaranteed accuracy of 5%. Output current capability is 40mA. The MAX666 has the additional feature of low battery detection, especially useful in hand-held instruments. All the devices have internal current limiting and shut-down facilities. Available from Dialogue Distribution, Tel: 0276 682001.
224 on reply card.



Miniature circuit- breakers

Superceding the Stopcircuit Z series is the Galaxie range of miniature circuit breakers. The range includes m.c.bs with current ratings from 0.1 to 32A in thermal-magnetic or thermal only configurations and with up to four poles. Optional extras include auxilliary signal contacts, temperature compensation and tropicalization. The devices offer an improved electrical specification and a smaller size than their predecessors and have a number of fitting options, suitable for most applications. Rilton Electronics Ltd, Tel: (08926) 4489.
218 on reply card.

Hard-disc controller

Capable of controlling any combination of four floppy or hard disc drives, Advanced Micro Devices AM9580A v.l.s.i. disc-controller i.c., available from Quarndon Electronics, contains on-chip error checking, dual-sector buffers and direct memory access (d.m.a.). The chip provides three error-checking schemes: cyclical redundancy check (for detection only) and single and double-burst Reed-Solomon error detection and correction.

AMD claims the error detection and correction provided by the Reed-Solomon schemes is three to four times more reliable than that provided by traditional file codes. In addition to having better single or double-burst capabilities, the Reed-Solomon codes have a smaller probability of miscorrection. The two sector buffers in the AM9580 provide high throughput rates. While one buffer is communicating with the disc, the other can communicate with the host.

This facility allows the i.c. to accommodate zero-sector interleave, and it reduces file-access time by reducing the number of disc revolutions needed to access data from physically contiguous sectors. The data buffers accommodate programmable sector sizes.

The software controls for the device are built-in disc primitives, i/o parameter blocks which reside in memory and specify the commands the controller is to perform. Parameter blocks can be linked together to allow the execution of a sequence of commands without any host intervention. The linked command list provides overlapping operations by searching ahead in the list to find active or inactive files. An on-chip direct memory access controller fetches commands, data, write-status information, and write data from the discs. Quarndon Electronics Ltd, Tel: Derby 32651.
217 on reply card.

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A high-performance, dual-channel, low-pass programmable filter has been designed for low-noise amplifier applications such as vibration analysis and audio signal analysis involving low-level signals. Known as the model 552, the new filter combines exceptional pre-filter gain with superior performance in the pass band and stop band. Overall frequency range is from 10Hz to 50kHz, and cut off frequencies can be programmed with 2-digit resolution. Full-scale sensitivity is selectable in 5dB steps from −60dBV (1mV) r.m.s. to +20dBV (10V) r.m.s. Inputs may be d.c. or a.c. coupled, with a nominal impedance of 1MΩ and 20pF. Output on a standard 50Ω line is 1V r.m.s. into 5kΩ with +10dB output gain. Noise, harmonic content and intermodulation products are all very low.

Filter and gain settings for each of the two channels are displayed on l.c.ds. Matching between the two channels is good. Model 552 can be set up from the integral keypad, or from a remote controller using either the RS232 or IEEE488 interfaces fitted as standard. This professional filter unit is specified for operation over the temperature range 0 to +40°C and is supplied for bench top operation.
209 on reply card.

Oscilloscope calibrator

An instrument to provide all the signals necessary for checking performance and recalibrating oscilloscopes up to 150MHz bandwidth comes from Waugh Instruments.

A calibrated-amplitude square wave generator checks to correct adjustment and accuracy of input attenuators. A wide range of timing signals from an internal crystal-controlled oscillator provides pulses with periods from 10ns to 5s. Vertical amplifier risetime can be checked with a clean, fast-rise < 1ns square pulse. Two sine wave outputs of 1kHz and mains supply frequency can be used for checking correct level, selecting of trigger circuits and locking the sweep circuits to the mains supply when checking vertical amplifiers and e.h.t. supplies for mains hum. Oscilloscope sync separators used for television measurements can be checked using the fully interlaced composite video output: both positive and negative going video provided.
221 on reply card.

Optical reflectometer has three lids

OFR10 – STC's latest optical time domain relectometer – gives almost instantaneous display of fault location and loss, joint loss, and attenuation in fibre of up to 87km in length, as well as loss for fibre connectors and splices. As with previous reflectometers, the unit consists of a mainframe housing c.r.t., printer and electronics, and an interchangeable lid containing opto-interface and control panel. Three lids are available with NTT-type connectors, covering 1300nm multimode, 1300nm single and multimode, and 1550nm singlemode operation. It claims exceptional s.w.d.r.* of 24dB and evaluates fibres up to 87km in length. Adaptations include special fibre-length menus, alternative connector types, and foreign-language on-screen help pages. STC Defence Systems, Tel: 0532 577261.
226 on reply card.

* Single-way dynamic range

Automatic cellular radio testing

A radio test set designed to automate cellular radio testing is a combination of Solartron's new 4922 radio code analyzer and the established Stabilock test set. Large input and output level ranges of the 4922 enable it to be linked to any audio test set but for cellular radios the test set requires full duplex capability, given by the Stabilock duplex f.m. demodulator option.

The Stabilock 4040 (the similar but lower cost 4039 is pictured below with it) is controlled from the 4922 by the GPIB with frequencies, level and modulation set by its test program. Programmable rom contains 98 tests that help to pinpoint the location of malfunctions. Test codes for all types of bleepers and message pagers, d.t.m.f. phones and sequential cellular radios can be generated. Radio data messages can be structured and analysed down to bit level. Solartron Instruments tel: 0252 544433.
228 on reply card.

Combined analogue and digital multimeter

A new multimeter, the MX573 from ITT Instruments is a combined analogue and digital instrument which offers true r.m.s. a.c. measurements combined with very high sensitivity and measurement bandwidth. The instrument incorporates two totally different measurement technologies within the same package: a precision analogue moving-coil multimeter and a 3.5-digit l.c.d. digital multimeter. As a result, users can observe the precise instanteous value of a signal on the digital display, while at the same time see any trends in rapidly changing signals without being confused by rapidly changing digits.

The 2000-count digital multimeter provides an accuracy of 0.1%. Analogue indication is based on a taut-band galvanometer, which avoids the mechanical friction inherent in pivot-type movements, and permits reliable, sensitive, hysteresis-free measurements. The MX573 provides eight measuring functions and a total of 35 ranges from 20mV to 1kV d.c. or 750V (r.m.s.) a.c., 200μA to 10A (a.c. and d.c.), and 200Ω to 20mΩ. The instrument can be used for direct readings in decibels, and continuity and diode test functions are incorporated. A single linear scale scale is used for all ranges (except 1000V) and functions, including resistance.

For d.c. voltage measurements, the MX573 provides a 10MΩ impedance. Auto-polarity switching is included, and the a.c. voltage bandwidth is 25kHz. The MK573 is designed to be rugged and reliable in field or laboratory use. Security connectors on the test leads protect the user against accidental contact with dangerous voltages, and the ammeter function is fully protected. The ohmmeter function will withstand of 380V without damage. ITT Instruments, Tel: 0753 824131.
215 on reply card.

• DATABANK •

KENT MODULAR ELECTRONICS LTD

The new KME range of high resolution colour monitors is fully described and illustrated in the information pack just released by Kent Modular Electronics Ltd. Cased monitors are currently available in 10in, 12in and 14in, sizes. Chassis display modules for installation in OEM enclosures can be supplied for 10in, 12in, 14in and 20in, screen sizes. KME also supply board and tube kits and CRT drive board systems.

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This edition includes many new items and important additions to existing popular product ranges.

ENTER 7 ON REPLY CARD

DEAN MICROSYSTEMS

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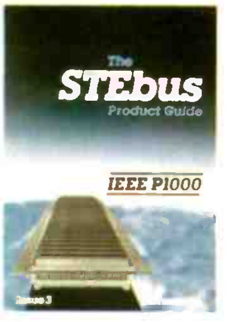

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NEW PRODUCTS

COMPUTING

Single-chip multi-register computer

New from Zilog is the Super 8 family of 20MHz single-chip microcomputers. Features of the devices include 325 byte registers comprising 272 general-purpose registers and 53 mode and control registers; addressing of up to 128K bytes of memory; and an improved instruction set which includes multiply, divide, Boolean, and b.c.d. operations. Additional instructions support threaded-code languages such as Forth.

Super 8 also has two register pointers to allow use of short and fast instructions to access register groups within 1μs; a direct memory access (d.m.a.) controller; two 16-bit counter/timers; a full duplex serial uart with an on-chip baud rate generator; and an on-chip oscillator. Up to 32 bit-programmable and 8 byte-programmable input/output lines, with handshake channels are provided and the interrupt structure supports 27 interrupt sources, 16 interrupt vectors, and 8 interrupt levels. Super 8 microcomputers can be used as input/output or memory-intensive computers, or can be configured to address external memory while still supporting many input/output lines. It is available as a rom-less microcomputer with four byte-wide input/output ports plus a byte-wide address/data bus. Additional address bits can be configured up to a total of 16. The Super 8 is supplied in a 48-pin dil plastic package. Available through Hi-Tek Electronics. Tel: (0233) 213333.
206 on reply card.

Optical disc hold 2Gbytes

Designated the LaserDrive 1200 and manufactured by Optical Storage International (OSI), a joint venture company of Control Data and Philips, the new random-access, Worm (write once, read many) disc drive provides a storage capacity of 1Gbyte on each side of a 12in diameter removable disc.

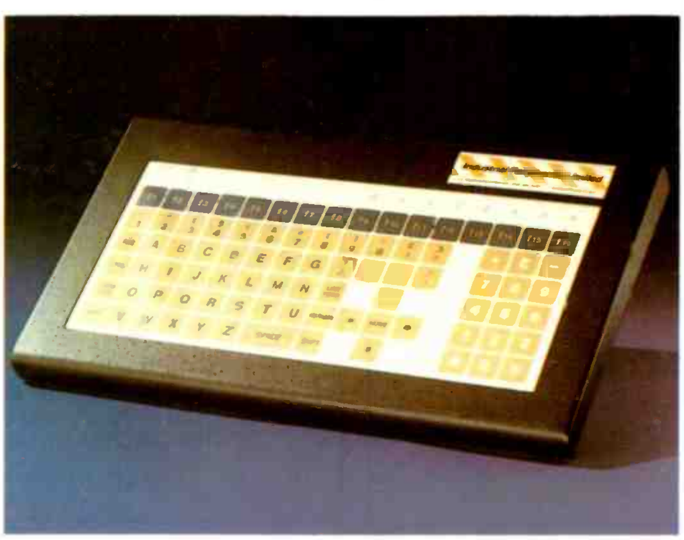
Incorporating built-in control electronics with an ISI or SCSI, the LaserDrive 1200 unit includes data buffering, a direct read-during-write facility, error correction and error recovery capabilities for improved system throughput and data integrity, providing an error rate of less than one in 10^{12}, and mean time between failures of 12,000 hours. It features a burst transfer rate of up to 2Mbytes/s and a sustained data rate of 250 Kbytes/s. Available through Sintrom Electronics Ltd. Tel: 0734 875464.
223 on reply card.

STE/IEEE 488 interface

GMT Electronic systems, who make a range of System 1000 STE bus products and development systems, have announced a new interface card for the bus which greatly improves currently available connection systems for IEEE 488 measurement and control equipment. The 1070 board is based around the 7210 intelligent controller and gives easy STE bus access to the wide range of printers, plotters and other data gathering systems which use the IEEE 488 standard. The card also provides an interface to other computers. GMT's new board meets all the necessary 488 requirements for talker, listener and controller and can be jumpered to provide interrupts on attention request and d.m.a. request lines. It occupies 10 i/o locations and is software configurable. Tel: 03727 42333.
212 on reply card.

PC keyboard for harsh environments

A sealed-sheet keyboard, the CKS-168, is designed for use in wet or dirty environments. It has serial or parallel interfaces and an IBM-PC compatible version is available. Intended to overcome the 'dead' feeling of membrane keyboards, the CKS-168 uses a matrix of sealed switch elements covered by a flexible polyester sheet. The keyboard will interface with most computer systems, programmable logic controllers and data loggers and provides a rugged replacement for most standard keyboards. The PC version mimics the positions and function of the PC keyboard as closely as possible. Industrial Peripherals Ltd. Tel: (0244) 532718.
205 on reply card



OS-9 on a 68020 computer

Cambridge Micro Computers has introduced the OS-9 operating system as an alternative to Unix on its recently introduced Vitesse Tower 16/32-bit microcomputer. OS-9 has recently been reconfigured for use with the 68000 and 68020 processors used in the Vitesse machine and offers a number of benefits for certain applications. Like Unix, it is a multi-tasking, multi-user operating system, but it is considerably more compact than Unix. Because a fully configured OS-9 system occupies only about 24Kbyte, compared with over 200Kbyte for Unix, it becomes feasible to load it into rom – hence creating a discless computer system which is highly cost-effective and which is more suitable for applications such as process control and embedded systems. The Vitesse supports both Unix and OS-9 on the 68020 processor. OS-9 is written in assembler language and runs at high speed. It also supports the C language and provides many of the standard features expected from Unix systems. Cambridge Micro Computers Ltd. Tel: 0223 314666
213 on reply card.

A-to-d for STE-bus

A fast high-resolution a-to-d converter for the STE-bus is provided by the ADC12/16 board which uses the AD574A to provide 12-bit conversion in 25μs using the successive-approximation method. Careful shielding limits input noise to typically less than 80μV. A software-selectable, on-board programmable-gain amplifier extends the resolution over three decades to ×100, corresponding to resolutions of 2.44mV over ±5V, 244μV over ±500mV and 24.4μV over ±50mV. The combination of conversion speed, resolution and accuracy extends the utility of the STE bus into many new digitization applications. As well as an interface to STE, the board contains a header-connector interface to Arcom's standard range of signal conditioning modules. A software-controlled analogue multiplexer selects any one of 16 differential inputs from this interface, allowing connection of modules such as thermocouple amplifiers, current sensors and prototyping boards. Channels can be switched in 6μs. The board also offers a faster conversion time of 17 microseconds with 8-bit resolution. This feature is software-selectable. Arcom Control Systems Ltd, Tel: Cambridge (0223) 242224.
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74LS30	20p	74LS241	65p
74LS32	20p	74LS244	65p
74LS51	20p	74LS245	80p
74LS74	20p	74LS257	50p
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17508

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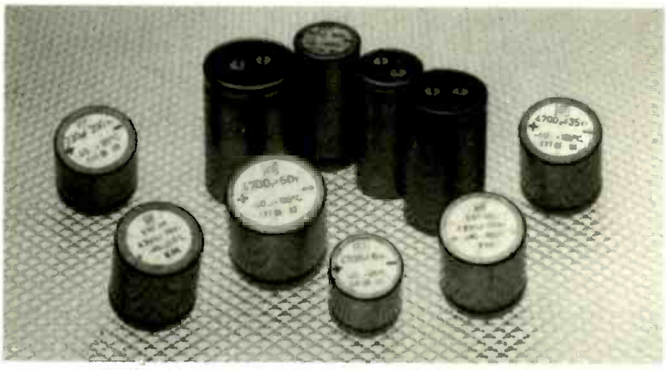
A family of standard and custom thin-film resistor networks and hybrid circuits are manufactured by HyComp Inc. They are packaged in 20 and 28 pin JEDEC type case styles. These surface mount devices are available with pin-outs compatible with JEDEC standards. L.c.c. packaged circuits for critical applications are also available, these being pinned out for minimal internal conductor lengths and/or parasitic reactances where higher accuracy and thermal stability are required.

The LCC/J series capability includes design, fabrication, packaging and 100% testing to commercial and military requirements. Standard resistor products include: quad divider feedback networks, 7,8 or 12 equal independent resistor networks, binary weighted dividers and general-purpose R-2R ladders. Custom products include hybrid active multi-pole analogue filters, temperature-stable precision voltage references, data converters with resolution to 14 bits, op-amps and gain-programmable instrumentation amplifiers. Resistor elements are manufactured using proprietary thin-film Nichrome techniques and resistance range is 1Ω to 1MΩ. Absolute tolerance is available from 10% down to 0.01% whilst ratio tolerance is from 1.0% to 0.005%. The J series circuits are suitable for use in production lines where reflow solder techniques are used. Information from: GCA Electronics Ltd., Tel: 08446 8861.
208 on reply card.

Ultra-high sensitivity relays

Featuring ultra-high sensitivity, the Takamisawa RA4 relay will operate at only 0.045W. The RA4 has a form C (4PDT) bifurcated contact arrangement and contacts are gold overlay, silver palladium alloy. The relay is offered in three types: single winding, non latching; single winding latching; and double winding latching. Other features include a maximum resistance of 100MΩ, maximum current of 2A, and ratings of 120V a.c., 0.5A, 24V d.c. 1A resistive. The minimum insulation resistance is 1000MΩ at 500V d.c. and the dielectric strength between open contacts is 1000V a.c. The RA4 is supplied in a 10mm high 14-pin dual-in-line package. The device is compatible with the SDS DS4 relay. ITT MULTIcomponents, Tel: 0753 824131.
207 on reply card.



High-voltage electrolytics

A range of low-profile electrolytic capacitors has been added to Steatite Roederstein's EYF series. Designated EYF06, the new capacitors are designed for use in high-reliability switch-mode power supplies and similar applications where headroom is at a premium. Values cover 47μF at 385V to 680μF at 200V, d.c. working. Capacitance tolerance is −10 to +30% and the working temperature range is −40 to +105°C. Mounting is direct into 0.1in (2.54mm) p.c.b. matrix by means of snap-in radial leads. Steatite Roederstein, Tel: (021) 454 6961.
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Five-user PC expansion

Plus4 is an expansion system for the IBM PC or compatibles to create inexpensive, high performance, clusters for five users. It is designed to meet the needs of small businesses and corporate departments requiring multi-user capability without investment in complex and costly local area networks (lans). A complete five-user system built using Plus4 requires only one host PC equipped with a hard disc and four inexpensive terminals. Performance is up to eight times the speed of networked PCs at a typical cost saving of 30%. Plus4 includes Alloy's NTNX Novell-compatible multi-user system software, tape backup, and four Alloy PC-SLAVE/16 boards that provide each user with an individual NEC V20 processor and 1Mbyte of memory. With Plus4 up to five users can share PC peripherals, data, and applications software developed to run under MC-DOS or Novell's lan operating system software, NetWare. Each user is added by simply plugging a terminal into Plus4. Each terminal is, in essence, a fully configured PC. Because Plus4 attaches directly to the bus of the host PC, performance is many times faster than a lan. It incorporates Alloy's APT-40 internal tape drive, which provides a file-orientated backup capacity of 40Mbytes per cartridge at a transfer rate of 500Kb/s. Alloy Computer Products Ltd, Tel: (0285) 69571.
219 on reply card.

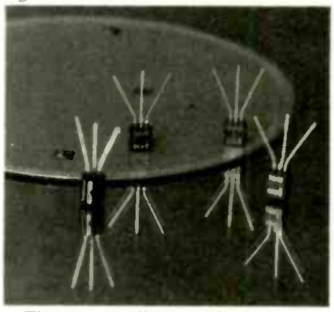
Clock-and-memory chip

The MK48T02 is a timekeeper ram chip made by Thomson Semiconducteurs. It combines a 2K by 8 full c-mos s-ram, a bytewide accessible real time clock, a crystal and a long-life lithium cell in one 24-pin plastic dip. The 48T02 is a non-volatile pin and function equivalent to any JEDEC standard 2K × 8 s-ram such as the 6116 or 5517. It also fits into many eprom and eeprom sockets providing the non-volatility of the proms without special write timing or write performance limitations. Data retention is effected simply. With V_{cc} applied, the 48T02 operates as a conventional bytewide static ram. However V_{cc} is constantly monitored. Should it decay or fail completely the ram will automatically shut down and protect its contents.

Access to the clock is simple because the ram and clock are combined on the same die. The timekeeper registers are located in the upper eight locations of the ram. The registers contain: year, month, date, day, hour, minute and seconds data in 24-hour, b.c.d. format. Leap year correction is included. The registers are constructed from biport memory cells which allows unhindered access to the rest of the ram. Access and cycle times are equal and four versions are available: 120ns, 150ns, 200ns and 250ns. Hawke Components has stocks of all versions as well as comprehensive data. Tel: 01-979 7799.
214 on reply card.

Conductive depletion mode transistors

Siemens has added to its 'Sipmos' range of small signal transistors two depletion-type devices (n-channel) which begin conducting even at slightly negative gate voltages – normally such transistors conduct only when the gate voltage is positive (enhancement type). Transistors of the type are suitable for all applications which require a monolithic normally-closed contact, e.g., telephone equipment. The new Sipmos components, designated BSS129/229, are housed in T092 packages and are suitable for up to 230/250V_{DS} (drain-source) and 150/100mA drain current, with a rated power dissipation of up to 1/0.63W and a maximum on-state resistance R_D of 20/60ohms.



The new small-signal depletion-type transistors, in addition to being particularly suitable for applications involving negative gate voltages, also help to simplify a number of circuits of the type required in telephone terminals. A current limiter and switch are formed by means of two resistors and a diode; a constant current source by a resistor and a potentiometer and a complete voltage regulator can be made using conductive depletion-mode transistors operating in conjunction with a capacitor, a resistor and a Zener diode. A constant-current source implemented by means of the BSS 229 can be operated across the full voltage range from 1 up to 250V_{DS} and supplies continuous drain current of up to 10mA. The gate threshold voltage $V_{GS(th)}$ remains below −0.7V. This circuit is also suitable for use as an auxiliary power supply. The voltage regulator employing a BSS 129 or 229 is suitable for feeding c-mos components. The particular advantage of this configuration is that the available current just meets the requirement of the c-mos components; and, independent of the load (the c-mos component's switching status), it incurs practically no current loss. The desired output voltage is defined by means of the Zener diode. Siemens Ltd, Tel: (09327) 85691.
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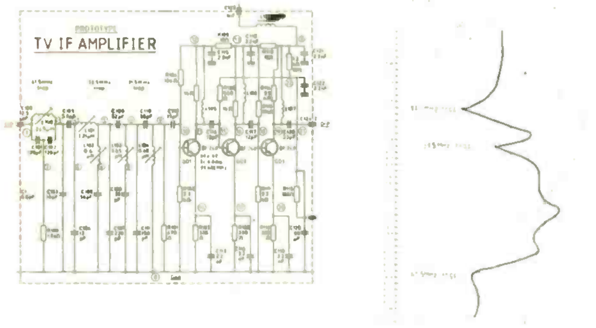

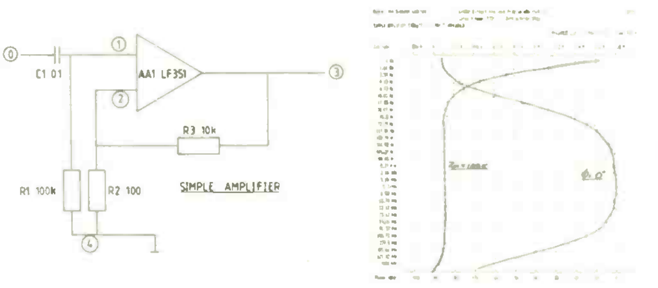

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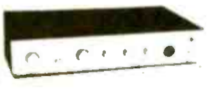

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Low-cost Tek

Tektronix has celebrated its 40th year by announcing more new products than in any previous year, the latest to emerge being the 2225 50MHz portable oscilloscope. At £750, it is the lowest cost instrument in its class yet made by Tek, and it was designed, engineered and made at the Hoddesdon plant. Its salient characteristics include alternate magnification, in which the single timebase is magnified up by to 50 times on alternate sweeps to give a roughly similar effect to a delayed timebase; 500 microvolt/div. sensitivity; high and low-pass trigger-coupling for increased stability; and the usual range of trigger modes, including tv line and field and single sweep. Minimum sweep time is 5ns/division. The 2225 is said by Tek to be one of the simplest to use high-speed oscilloscopes available, which will find many applications in education, servicing and production.
229 on reply card.

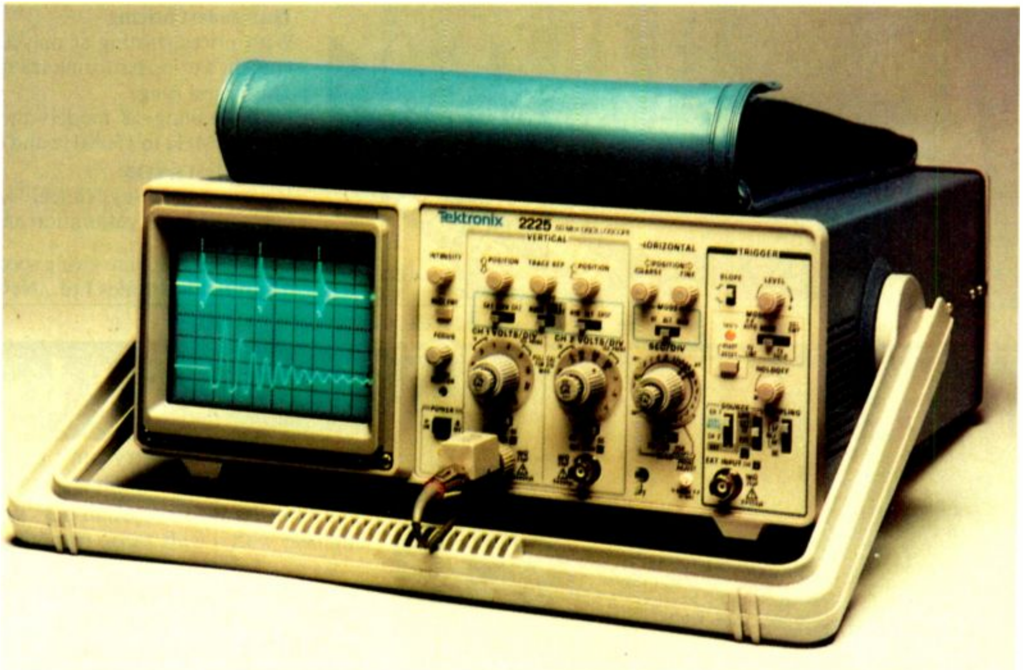
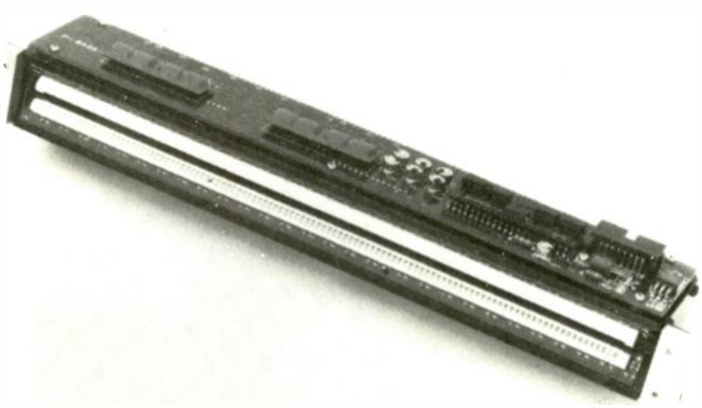


Image sensors for contact reading

Contact image sensors from Toshiba have linearly arranged elements covering the full document width. This arrangement provides exact 1:1 correspondence when the sensor is brought close to the document. As a result, the overall size of image inputting equipment can be substantially reduced. The integrated sensor modules use either c.c.d. (charge coupled device) or a-Si (amorphous silicon) to read the image.

The c.c.d. type is an integrated module comprising the newly developed Toshiba long c.c.d. array (up to 4,864 picture elements), a precision rod lens array and a high-brightness led array. Drive circuitry, pre-amplifier and control circuitry are all incorporated in hybrid i.c. packages assembled on the contact image sensors' integral printed circuit board. The c.c.d. image sensors have a resolution of 16 elements per mm for optimum scanning performance. Modules are available for paper sizes from B8 to A3. The modular construction enables easy installation without the need for critical adjustments. Toshiba's a-Si image sensors comprise a single-line photo detector array and analogue scanning circuits on an alumina substrate. Readable document width ranges from A4 to various special pattern recognition sizes, with resolution ranging from 1 to 8 elements per mm. The a-Si sensors are also easy to instal due to the limited number of control lines. Both types of contact image sensor from Toshiba offer high operational speed and sensitivity and are designed to serve a wide range of applications.
227 on reply card.



IBM into semi-custom workstation

A semi-custom simulation package, Lesim, turns an IBM-XT or AT Personal Computer (with FutureNet added) into a low cost work-station for the design and simulation of Mullard c-mos gate arrays and standard cell arrays. The package is designed to help engineers whose initial throughput will not justify investment in the more complex engineering work-stations used by design centres or large-scale users. Accredited customes will not be charged for the software. After schematic capture, the Mullard Lesim software enables the designer to carry out simulation (both functional and timing) for the circuit. The Mullard Design Centre will carry out placement and routing, followed by post layout simulation, from the designer's results. Support material includes a comprehensive user manual, Lesim software, plus component libraries for 00 and 06-series gate arrays and a standard cell library all supplied on five diskettes.
219 on reply card.

Antennae aligned by laser

A portable system for the quick, accurate and inexpensive alignment of antennae is available from Tony Chapman Electronics. It enables rapid alignment between line-of-sight transmit and receive antennae and can be used in a test chamber or in an open environment for ranges of up to one mile (1.6km). Possibly the greatest benefit is the elimination of the need for traditional surveying instruments which is both time-consuming and difficult to use.

Before antennae can be tested in an anechoic chamber, the source antenna and the antenna under test must be aligned, or boresighted, perfectly. The new centrehead boresight laser made by Hulbert Engineering is designed to greatly ease this task without sacrificing accuracy by using a coherent light source. The laser is first used to align the antenna under test by replacing the source antenna and directing a 1mW visible light beam down-range to the test antenna (see figure). Azimuth adjustments are then made to this antenna's polarization positioner until the laser beam intersects the geographical centre of the antenna to leave the positioners aligned in one plane. The laser is then mounted on the test antenna's positioner and the process is repeated until both antenna positioners are boresighted in two planes.

The whole process requires about 30 minutes. The boresight laser has been designed for use with all standard 8in (200mm) diameter mounting flanges. Its weight (about 2.4kg) has been kept to a minimum by the use of hard anodized aluminium.

The laser tube has a typical lifetime of greater than 15,000 hours, and has been built to operate from 10 to 60°C at humidity levels as high as 95%. Since the laser's current requirements are low, 4-5mA, it can be battery powered for field use.
220 on reply card.

Within the 68020

To make best use of the 68020's upgrading to 32 bits, the 68000-family instruction set has been expanded.

DAVID BURNS AND DAVID JONES

Widening the address and data buses of the 68020 to 32 bits meant that new instructions were needed to make best use of the extra width. For example with an addressing range of up to 4G-byte it became necessary to have branch instructions with 32-bit displacement to reach any address.

Other instructions, like the register-boundary check and signed/unsigned multiply instructions CHK. MULS and MULU, have been extended to operate on 32 bits operands. In addition, the divide instruction DIV now operates on 32 and 64 bits of data and DIVS can be used to perform a 64-by-32-bit division. A new instruction, DIVSL, has been added specifically for 32-by-32-bit long-word division.

Arithmetic capability of the 68020 is improved. To speed up operation of shift and rotate instructions, a 32-bit barrel shift register has been designed into the processor. This allows from 1 to 32 shifts or rotations to be made within a register in only one clock cycle.

Two other instructions for sign extension and linking lists of local data, EXT and LINK, have been modified. Sign extension of a byte to a word or long word is now possible using the modified EXT instruction EXTB, and LINK can accommodate a 32-bit displacement.

Lengths of some instructions executed on the 68020 may differ from the same instructions executed on the 68000. This is because the new addressing modes require an additional 32-bit instruction-extension word which is decoded by the processor.

INSTRUCTION ENHANCEMENTS

New instructions have been added to give additional flexibility for the programmer. One of these is CHK2 which performs an upper and lower boundary check on a register's content, instead of just on the upper boundary as with other 68000 processors.

With the 68000, the TRAPV instruction causes a system trap which routes to the operating system via a supervisor access if the condition-code register overflow bit is set. This instruction modified to TRAP_{cc} now responds to all the bits in the condition-code register.

In addition to the coprocessor general function instructions for passing command words to coprocessors such as the MC68881 floating-point device, there are six instructions for testing or controlling active coprocessors within a 68020 system. Their mnemonics are cpSAVE, cpRESTORE, cpB_{cc}, cpDB_{cc}, cpS_{cc} and cpTRAP_{cc}.

The last four of these instructions operate in the same way as 68020 instructions B_{cc}, DB_{cc}, S_{cc} and TRAP_{cc} except that they operate on the coprocessor condition-code register. During assembly, these instructions are given an identifcation field (ID) corresponding to one of eight possible coprocessors. Using these test and control instructions, the programmer can make judgements based upon the results of a coprocessor operation.

Instructions cpSAVE and cpRESTORE perform a context switch on a processor. Each time a context switch occurs (the operating system switches to a new user or runs a new task) all internal information that the coprocessor requires to perform instructions is placed on the supervisor stack. After the context switch the new user or task has full use of the coprocessor internal programming registers. To restore the coprocessor to its original condition, i.e. its state before the cpSAVE instruction was issued, cpRESTORE is used.

SUPERVISOR INSTRUCTIONS

Improvements have been made to the 68020 supervisor mode. A number of specific instructions belong to this group. To accommodate programming of the 68020's additional control register the MOVEC instruction now covers cache control and address registers.

For example a MOVEC.L D0,CACR operation loads the value contained in D0 into the cache control register. The value represented by D0 can indicate a cache enable, a cache clear, a cache freeze or a clear entry operation.

To perform the debugging task of inserting breakpoints into a code sequence the 68000 processor needs to execute a predefined illegal instruction. On receiving such an illegal instruction the processor jumps to the illegal instruction's exception-handling routine and executes the required breakpoint task. In a monitor program for example it may well halt the program and display the internal register contents on a terminal.

Using this method, the processor has to store an entry for the displaced code in some form of breakpoint table in memory. A large amount of software is required to manage this table, for example to replace the original opcode after the breakpoint has been finished with by the programmer.

A dedicated breakpoint instruction, BKPT, is included in the 68020 and used in the form BKPT#<data>. Since the immediate data value represented by #<data> can be from 0 to 7, up to eight hardware breakpoints are possible. In Motorola assembly language, the # sign designates an immediate value.

On executing a breakpoint instruction the 68020 reads a word from the c.p.u.-space address corresponding to the breakpoint number, Fig.1. If the DSACK_x signals terminate the cycle then the data at this address is latched into the processor. This data is the 16-bit opcode that was displaced to make room in memory for the breakpoint instruction. If this breakpoint acknowledge cycle is terminated by the BERR control signal then the processor performs exception processing for an illegal instruction – as with the 68000.

This hardware process is much faster than the 68000 equivalent since the breakpoint table is managed by the processor and not the system software. The sequence of events illustrated in Fig.2 shows that when a breakpoint instruction is placed in a code sequence (by a monitor program, say) it places the displaced opcode into its corresponding c.p.u.-space register or memory location.

The remaining 16-bits of this register can be used to implement a breakpoint count. This count is loaded with the number of times the program should execute the displaced instruction before the breakpoint is actually taken. For example if BKPT is executed and the count is non-zero then the external hardware will need to generate

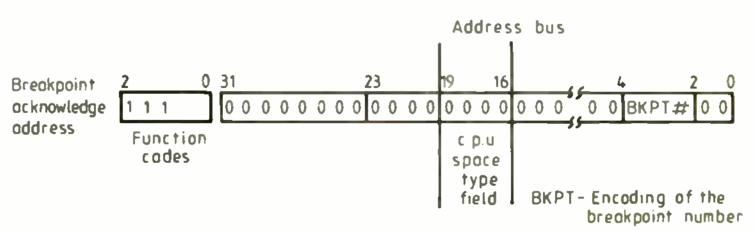


Fig.1. During a breakpoint-acknowledge cycle the 68020 addresses this memory location in c.p.u. space (function codes all ones) to fetch the displaced opcode. If the breakpoint is to be taken then the memory access should terminate in a BERR, otherwise DSACK_x, are asserted.

Two previous articles presented in our December and January issues introduced the 68000 family and discussed 68020 architecture.

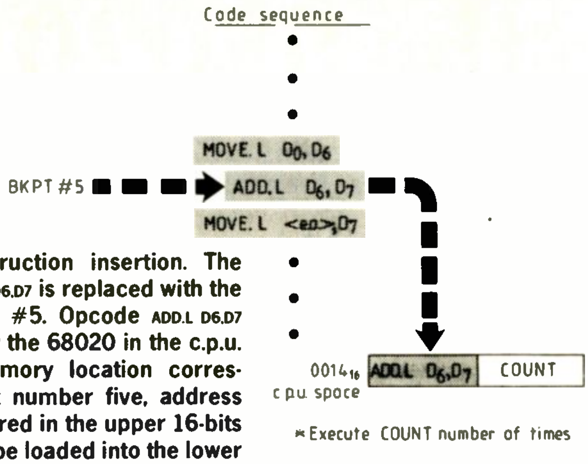


Fig.2. Breakpoint instruction insertion. The 16-bit opcode for ADD.L D6.D7 is replaced with the 16-bit opcode for BKPT #5. Opcode ADD.L D6.D7 must then be stored by the 68020 in the c.p.u. long-word (32-bit) memory location corresponding to breakpoint number five, address 14_{16}. The opcode is stored in the upper 16-bits and a count value can be loaded into the lower 16-bits.

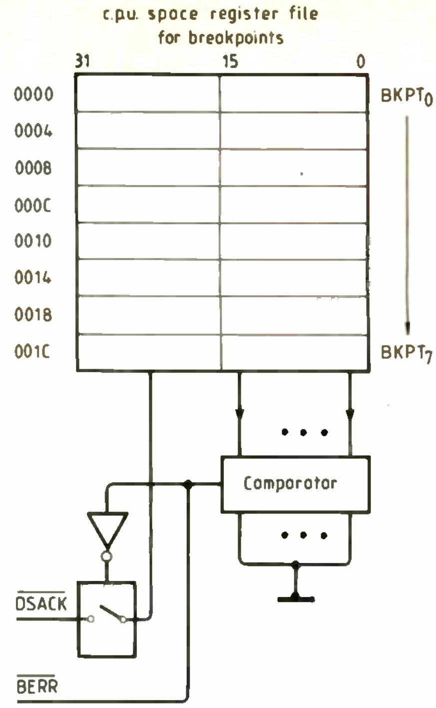


Fig.3. External breakpoint hardware. Eight long-word memory locations from $0\text{-}1F_{16}$ in c.p.u. space are used to temporarily store the opcode replaced by a BKPT instruction. Each time BKPT is executed the 68020 accesses one of the locations depending on which breakpoint is being executed ($BKPT_0 - BKPT_1$) If the count value (bits 0-15) is not zero the replaced opcode is placed on the data bus (bits 16-31) and the $\overline{DSACK}_x$ lines are asserted. If the count is zero then $\overline{BERR}$ is asserted to initiate a breakpoint acknowledged cycle in the 68020.

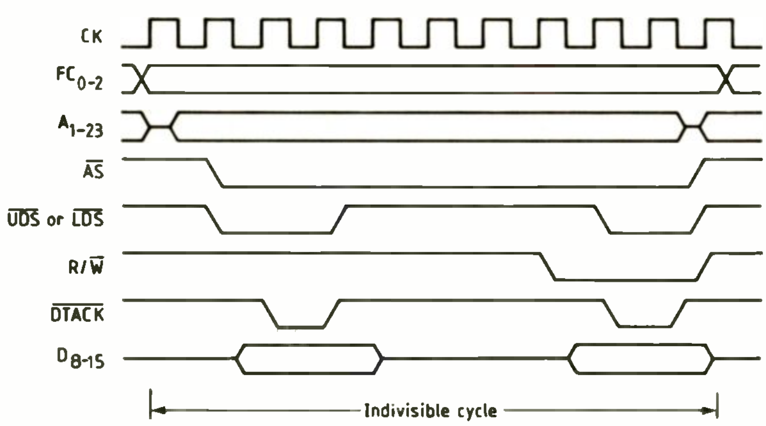


Fig.4. When executing the TAS instruction (test and set an operand) the cycle is made indivisible, i.e. uninterruptible, by continued assertion of address strobe $\overline{AS}$ through the read and write operations.

$\overline{DSACK}_x$ in order to execute the displaced code. When the count reaches zero the hardware should generate $\overline{BERR}$ and exception processing will begin for the breakpoint service routine. For simplicity, design of this hardware can be incorporated into a memory-management unit as is the case with the MC68851 paged-memory-management unit.

Hardware is shown in Fig.3.

MULTIPROCESSING AND MULTITASKING

The MC68020 has several facilities for multiprocessing. It has special instructions like TAS, CAS and CAS2 for interprocessor or intertask communications and a hardware line ($\overline{RMC}$) for bus locking. An instruction-continuation facility allows easy transfer from one processor to another.

Execution of the special instructions forces assertion of the $\overline{RMC}$ signal (read-modify-write cycle) and thus causes the bus to lock. Any alternative bus masters in the system must wait until the negation of the $\overline{RMC}$ signal before they can take control of the bus.

Instruction TAS (test and set an operand) is the same as that on the 68000 processor and allows implementation of flag variables for globally-shared memory blocks. This instruction allows the testing and setting of a variable to be performed in an indivisible cycle.

With the 68000 this indivisible cycle is achieved by keeping the address-strobe signal ($\overline{AS}$) asserted throughout the read-modify-write operation. You can see this in Fig.4 where the processor reads a memory location, tests the data item and may modify it and then write it back out to memory. This cycle is carried out without negation of the address strobe. With the 68020, execution of this type of cycle is further indicated by assertion of the $\overline{RMC}$ signal.

Flags are very important elements in the implementation of any multitasking/multiprocessor system. In these types of application flags are used to control access to globally-shared memory blocks. If a task or processor needs to gain access to one of these memory blocks it must test the associated flag to determine whether the block is presently being used. If the flag is clear then the task (processor) will claim control of that memory block by setting that flag. It should then be guaranteed sole access to that particular block.

If your system is configured such that reading and testing of the flag is implemented through one instruction and setting of the flag is implemented through another instruction then it is possible that a number of tasks (processors) may gain access to the memory block at one time.

This situation can arise if task A for example reads the flag and, finding it clear, decides to set it and thus claim access to the block. Task B may then interrupt task A (in a multitasking environment there may well be a preemptive-timer interrupt) and it too may read the flag associated with the memory block and also find it clear because task A did not finish writing the data. Task B claims the memory block by setting the flag.

The preemptive interrupt may occur again and reconstitute task A. Execution of task A continues from where it detected the flag as being 'clear and continue' by setting the flag to claim the memory block.

In this way, two tasks concurrently execute the same memory block and as a result there is a risk of data corruption. To remove this possibility, testing and setting of the flag must be performed in an indivisible cycle, i.e. with no interrupts or bus arbitration, which is done using the TAS instruction.

This read-modify-write class of instruction is further expanded by CAS and CAS2. Compare-and-swap-with-operand, CAS, is an extension of the TAS instruction and allowing data items (byte, word or long word) to be compared and swapped. This instruction could for example be used in the manipulation of linked lists when a new item is required to be inserted for example.

A copy of the old starting pointer must first be put at the base of the new item block and then the pointer to the new item block must be updated into the starting pointer area. To perform this reliably, updating of the new starting pointer must be executed using an indivisible cycle.

The first operation is to place a copy of the old starting pointer at the base of the new linked items block. This new item is starting address must now also become the starting address of the linked list. If after placing the old starting pointer at the base of the new item the present process, task A, was interrupted then task B could intervene, placing its own new item in the linked list.

The pointer at the base of task A's item is no longer the next item in the linked list – it doesn't know of the existence of task B's item. To remedy this problem it is necessary to retest the start pointer before you update it.

This can simply be done by using the instruction CAS DC, DU, START. To give an example, the existing starting pointer is copied into data register DC and then by using the CAS instruction the value in this register (old starting pointer) is compared with the present starting pointer (START). If these two are the same then the starting pointer is updated with the value in the other data register, D_u, (the new starting pointer). If the values in data register, D_c, and START don't compare (i.e. the START pointer has subsequently been changed) then the update is not performed and integrity of the linked list is preserved. This function is again performed as an indivisible operation and its bus activity is shown in Fig.5.

Instruction CAS2 is identical to CAS except that it can be used to compare and update two operands within the same indivisible cycle. This is of use in maintaining doubly-linked lists i.e. items with both a next-item pointer and a last-item pointer.

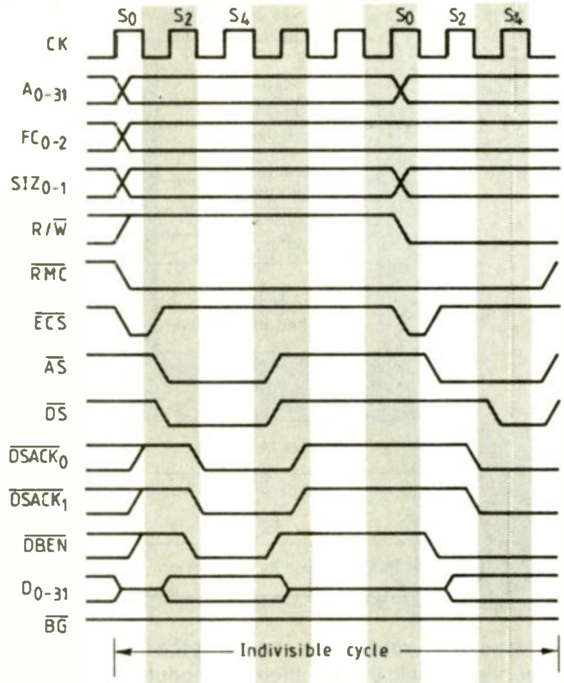


Fig.5. Execution of the CAS instruction (compare and swap with operand) requires a change of address and so continuous assertion of address strobe AS cannot be used. The RMC (read-modify-write cycle) signal indicates indivisible cycles.

MODULE SUPPORT

In comparison with the 68000, the 68020 has more levels of access control than just the supervisor/user split as on previous M68000 processors. Two instructions CALLM and RTM (call module and return from module) can be thought of as advanced subroutines used to gain access to other levels of security.

This feature enhances the computer operating system by allowing a number of layers or shells to be created around the computer kernel. With this type of system the 68020 can monitor attempts by the user to gain access to higher levels of security than permitted. In this case an access level exception will be taken by the processor and an error condition will be flagged. Figure 6 shows what such a system could look like in an operating system application.

In modern computing there are many areas where this mechanism could be used to give more security to an operating system. For example, consider an applications programmer who would like to access a large database to obtain personal details about an employee. For this example the programmer would need to have access permission to obtain this information. In addition the programmer needs to be prevented from updating that information, this being a function of the database manager or system administrator. Another area of use could be in the Unix operating system to set up different shells. Typically Unix runs with a Bourne shell, however other layers or shells are available for Unix; in addition user generated shells can be created.

The 68020 can be used to achieve these features by a combination of software and external hardware. The execution of the CALLM instruction is

CALLM #<data>,<e.a.>

This instruction is very similar to JSR (jump to subroutine), except that the immediate data value is the number of bytes of argument to be passed via the stack to the called module. Effective address <e.a.> is the actual address of the module descriptor in memory.

The module descriptor can be thought of as a gateway through which the calling program must gain access. The module being called can be thought of as a subroutine that is to act upon the data arguments passed to it. This module can be the same priority level or different to that of the caller. Figure 7 illustrates the procedure that the MC68020 goes through during execution of the CALLM instruction.

The CALLM instruction acts as follows. The effective address (<e.a.>) in the instruction points to the address of the module descriptor or gate to find control information. At the same time, the MC68020 creates a module-stack frame similar to an interrupt. The module descriptor contains the following information.

- How arguments are to be passed to the called module (option field). They can be passed either under the module stack or through an indirect pointer in the stack of the calling module.
- Descriptor type (type field). Two types are used; one in which there is no change in access rights (where the module stack is

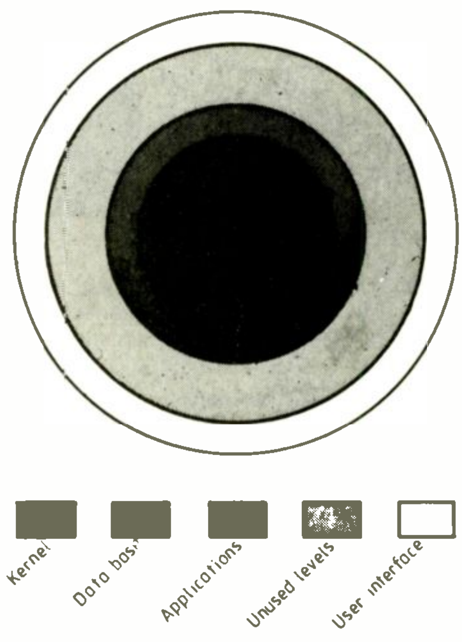


Fig.6. A typical computer can be thought of as layers of protected software programs. At the heart of the computer is the kernel. This is code written such that it will interface directly to the computer hardware. This will typically be the highest priority code and, as such, runs in supervisor mode. Other layers that need protecting from the user programs include database and applications software, these being accessible only to users with high access-permission privileges, e.g. system administrators.

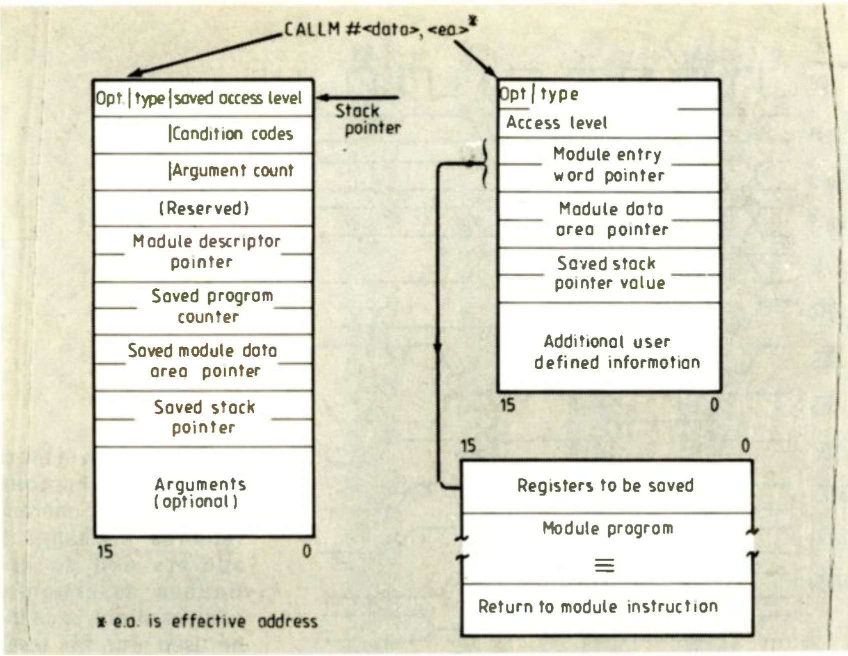


Fig.7. CALLM can be thought of as an advanced subroutine. On executing the instruction the 68020 places information on the supervisor stack; this is called the module stack frame. The effective address given in the instruction (<e.a.>) points to the address in memory of a module descriptor containing specific information about the module being called. Within the module descriptor is the actual address of the program to be executed.

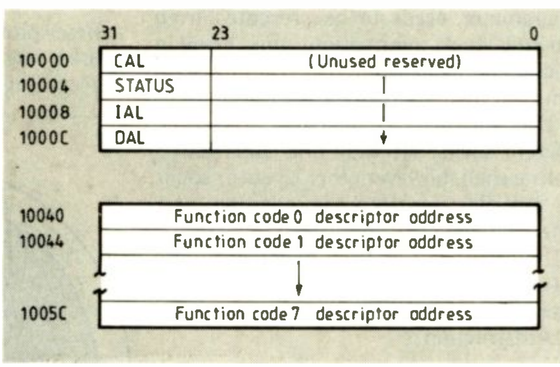


Fig.8. Implementing access-level support requires external hardware at these addresses in c.p.u. memory. Four long words are used to control access privilege and eight long words are used to contain addresses of up to eight module descriptors.

created on the calling module) and the other where there is a change in access levels (a change of stack pointer may be needed).

- Called module access level.
- Stack address of the called module. Note that the first word of the module program indicates the registers used in the program; this is interpreted by the 68020 in such a way that the processor knows which registers to place on the stack.
- If the access change requires a change of stack pointer, the old value is saved in the module and all the arguments are copied to the new stack.
- User-defined information, for example a count of the number of times the module has been accessed within a certain task.

The module stack frame contains information needed by the processor to continue program execution from the instruction following the CALLM. Arguments passed to and from the module are placed on the stack before execution of the call module instruction. If there is a change in the stack pointer requested from the module descriptor, this is requested and the arguments are copied onto the new stack, typically for access-level changes.

This does not offer a great deal of protection for this system, since the user can obtain access to a higher-privilege level simply by reading the module address in the descriptor. For this reason, the protection mechanism is designed into the 68020 as one of the special c.p.u. functions. Any request for change of access level causes the processor to execute a c.p.u.-space cycle. While processing a type #01 (a module call for which there is a change in stack pointers) descriptor the CALLM and RTM instructions communicate with external access-control hardware in c.p.u. address space at the address shown in Fig.8. These registers would typically be designed into a memory-management unit as an aid to the protection mechanism (as with the 68851 paged memory management unit). As the communication to these registers is performed by the c.p.u. microcode, the user is unaware of these operational checks. The current access-level register (CAL) contains the access level of the currently executing module. The increase access-level register (IAL) is the register through which the calling module requests increased access rights and the decrease access-level register (DAL) is the register through which the processor requests decreased access right. These registers are updated from the module descriptor stack frame.

The access-status register allows the processor to determine from the external hardware whether an intended access-level transition is valid. During the CALLM instruction, the processor uses the descriptor register to communicate the address of the type #01 or descriptor.

The RTM instruction is executed as the last instruction of the called module and is used to restore the original information to the processor and to the next instruction to be executed. After the RTM instruction has executed, resultant arguments will be resident on the stack for the program to use.

Support for up to eight levels of access can now be supported, as opposed to the previous user/supervisor mode on other M68000-family processors.

David Burns and David Jones are with Motorola in East Kilbride.

Futurebus group starts up

In response to the growing number of requests for product and information on Futurebus, the IEEE's 32-bit bus standard, a number of UK companies have established the Futurebus Manufacturers and Users Group. It is the intention of the group to give the UK an early start and a competitive edge in Futurebus products, an opportunity that has been sadly missed with other buses, notably VME.

Twenty invited representatives of 12 UK companies attended the inaugural meeting held last autumn, hosted by National Semiconductor at Swindon. Nat Semi said they were the only manufacturer with Futurebus devices in production, offering a range of transceivers, drivers and receivers which conform to the P896 specification.

Also present and with product available was BICC-Vero who have backpanels, termination networks, extender cards and prototyping boards in current production. A number of other companies are known to have Futurebus products under development including an advanced multiprocessor system based on multiple 32332's, graphics engines and systems for high-speed parallel processing, but most of these products are firmly 'under wraps', with the intending suppliers playing their cards close to their chests. Apart from National Semiconductor, at least four other manufacturers are known to have l.s.i. products for Futurebus currently under development.

The potential market for Futurebus is said to be vast, with very little competition in the 32-bit stakes. It is claimed that it has all the answers to the 'bus driving problem', cache coherency, bus arbitration and bandwidth whilst also being manufacturer and technology independant. (news, Jan 1984, page 45).

Represented at the inaugural meeting National Semiconductor, BICC-Vero, Dean Microsystems, Plessey, British Telecom, Ferranti, Array Consultants, Fraser Williams Industrial Systems, Spectra-Tek and the DTI.

RADIO BROADCAST

PAT HAWKER

H.f. spectrum management

A recent IEE colloquium on h.f. Frequency Management brought home the complex operational problems of frequency planning for h.f. broadcasting and communications due to the diurnal, seasonal and 11-year sunspot cycle variations and the difficulty of selecting suitable channels many months in advance in the case of broadcasting and, for communications, the use of computer-prediction programs and real-time channel evaluation (t.r.c.e.) techniques.

G.S. Spells (BBC External Services) gave an overview of the current procedures under Article 17 of the ITV Radio Regulations by which the many seasonal changes in the frequency schedules are selected and registered with the IFRB. The planning starts at least nine months before the start of the three-month period concerned. This involves the use of desk-top microcomputers and other aids to interpreting the long-term ionospheric predictions. BBC frequencies are co-ordinated before submission to the IFRB (International Frequency Registration Board) with those for Voice of America, Radio Free Europe/Radio Liberty (American-funded transmissions from West Germany into the Eastern Bloc), FCC, Radio Canada, Radio Netherlands and Deutsche Welle.

The BBC alone uses some 80 high-power trannmitters of up to 500kW output and is seeking, by increasing use of overseas relay bases, to provide single-hop coverage of most of the world. Programmes to overseas bases are now all distributed by satellite and this can give rise to curious "pre-echo" problems in areas where a UK transmitter may be received on the same frequency to that of the nearest relay base due to the satellite delay time. Three or four frequency changes are required in each 24-hour period and because of the difficulty of predicting propagation conditions accurately many months ahead, it is now common for programmes to be targeted to the same area on three or four h.f. bands simultaneously despite the ITU recommendation that not more than two bands should be used. For Bush House, the choice of languages and transmission time periods is controlled by the Foreign & Commonwealth Office and at present amount to English and 36 other languages.

N.St C. Gerdes (School of Signals, Blandford) described the growing use of prediction techniques based on programs suitable for microcomputers derived from the 1978 "Minimuf" algorithm by Levine, Rose and Martin and the German "MiniFTZ2" program based on a reduced CCIR map. He has translated and modified MiniFTZ2 to run on a fast co-processor 8-bit 64-Kbyte microcomputer and is convinced that MiniFTZ2 will largely replace Minimuf for smaller microcomputers. He also foresees increased use of "electronic mail" to obtain current information on the state of the ionosphere.

N.G. Riley (Marconi Research) is endeavouring to produce a "model" for h.f. interference taking into account the likelihood of any 1 kHz of h.f. spectrum being free at any given time, based on the occupancy data collected by Dr G.F. Gott of UMIST. The speaker admitted that if many users all attempted to base their frequency management on the same model it would be a non-productive exercise.

Paul Cannon (RAE) described the problems encountered at high latitudes including the severe polar cap absorption conditions that can completely disrupt h.f. signals for periods of from two to ten days. The less severe auroral absorption of communications circuits can usually be overcome by the use of a "dog-leg" relay station to the south of an affected radio path.

Radio! Radio!

Several years ago I acquired a copy of the American publication "A flick of the switch 1930 – 1950" by Morgan McMahor – an excellent 312-page paperback compilation on the development of radio and television receivers as marketed in the USA. This includes many photographs and original advertisements for hundreds of receivers, including amateur-radio communications receivers and some American military communications equipment of WW2.

Now Jonathan Hill, one of the founder members of the British Vintage Wireless Society, has produced an impressive British counterpart covering radio sets from the earliest pre-1992 receivers up to the 1960s. The result is a large (A4 format) 244-page book that includes considerably more explanatory text on the history of broadcasting than the American book, although it is evident that the author, a professional photographer and designer, remains more fascinated by the enormous variety of cabinets and enclosures than with the internal circuitry.

His book, in fact, provides a vivid reminder of all our yesterdays and there will be few readers born before 1960 who will not find illustrated reminders of the radio sets they grew up listening to. For the growing band of collectors of "valve" radios the book is clearly a must. My own regret is that, unlike "A flick of the switch" there are no illustrations of the communications or military receivers of the 1930s and '40s. Jonathan Hill sticks firmly to broadcast receivers – but of these he provides many hundreds of brief details and illustrations. There is also, for instance, some 40 photographs of British valve types from the 1922 "R" valve up to the B8A-based valves from 1953 onwards, though I doubt if the 1934 "acorn" valves were ever used in broadcast receivers.

Also included is an illustration of the 1935 miniature Hivac valves, probably the miniatures made in the UK. Some of these miniature valves, incidentally, were adopted by the German Abwehr (military intelligence) Geheim Funkmeldedienst radio unit at Berlin-Stannsdorf for use in several of their early clandestine radio equipment, production of which began in 1936-7. The Abwehr went to considerably pains in the first year of WW2 to continue to obtain these miniature valves by importing them through neutral countries (probably Portugal) despite all the British efforts to prevent such exports under the "trading with the enemy" regulations. Presumably Hivac had no idea where some of their products were going or what they were being used for!

Radio! Radio! is available direct from Sunrise Press, 2-4 Brook Street, Bampton, Devon EX16 9LY (telephone 0398 31310), price £18 plus £2 P&P for the deluxe signed and numbered hardback edition, or £12.95 plus £2 P&P for the softback edition.

Sporadic E on m.f.

Interest in extended-range radio propagation by means of Sporadic E ionization has usually been confined to frequencies between about 20 MHz and 150 MHz. It was in the late 1930s that the first amateur contact between the UK and Italy on the 56 MHz band was reported, though at the time little was known about the mechanism that brought this about. Sporadic E propagation really came into prominence with the spread of v.h.f. television. It was seen not as a bonus but as presenting, if only randomly, a serious interference problem on Band I (41 to 68 MHz).

Sporadic E brings in many European amateur signals on 21 and 28 MHz during the "summer season" of Sporadic E throughout the sunspot cycle. But relatively few engineers appreciate that Sporadic E can also affect medium-wave transmissions in the hours of dusk and darkness when m.f. signals are not absorbed in the lower D layer.

This is confirmed by an interesting university study carried out in Japan in 1981-83 and reported by Masayoshi Mambo et al "Comparison of measured and predicted field strengths of m.f. sky waves over short distances in Japan", *IEEE Trans* AP-34, No 10, October 1986, pages 1214-22. This report shows that in Japan, where sporadic E conditions are much more frequent than in the UK, measured median field strengths over paths of about 250 km from broadcast transmitters on 1222 kHz and 828 kHz during periods shortly after sunset can be over 7 dB stronger than predicted from CCIR techniques based on the "international reference ionosphere". When sporadic E is present, the skywave appears rapidly after sunset at enhanced strength, finally approximating to the CCIR predictions about four hours later and tending to fall below the CCIR curves some six hours after sunset.

TELEVISION BROADCAST

PAT HAWKER

TV in Europe

The Royal Television Society's "Golden Box" presentation at the Commonwealth Institute on the Philips Vidiwall and large screen Eidophor, marking the 50th anniversary of the start of the BBC service from Alexandra Palace (November 2, 1936), proved an interesting and attractive compilation. But I was not the only person to raise my eyebrows slightly at its ending with some rash claims about how Britain created it all – to the musical accompaniment of "Land of Hope and Glory".

TV-50 in general did seem to pay too little acknowledgement to the part played not only in the USA but also in Germany and France etc.

The IEE conference partly made amends with several contributions from the USA and one from Germany by Dip.Ing. Joachim Kniestedt of the German Ministry of Posts & Telecommunications at Bonn. The Germans celebrated their TV-50 in 1985 in connection with their 180-line service from the Berlin Radio Tower, received in public viewing rooms scattered throughout Berlin.

This service reached a high point with the televising of the 1936 Olympic Games (August 1 to 14), with Dr Walter Bruch of PAL-fame operating an electronic camera, reportedly seen by 150,000 viewers in 28 public viewing rooms. The 180-line v.h.f. transmitter was destroyed by fire at the Berlin Radio Exhibition of 1938. It was replaced by a 441-line transmitter (14kW, later 40kW) at Berlin – Charlottenburg and this service continued with interruptions until destroyed by RAF bombing in November 1943. A 441-line system was also set up by the Germans in Paris (the French had a pre-war service using 180 lines and later 455 lines). This continued until August 16, only ten days before the liberation of Paris.

Less well-known is that, during the occupation, French engineers continued work under hazardous conditions on 800 and 1200-line systems.

Radiodiffusion Nationale also began training engineers in television broadcasting techniques. One result was that on October 1, 1944, 441-line broadcasts were resumed on a restricted basis pending the introduction of the French 819-line system on November 20, 1948. Although I was in Paris in October, 1944 – and this was still seven months before the end of the war in Europe – few of us were aware of the French television operations based in the Rue Cognacq Jay and Eiffel Tower. But I do recall that it was about this time that the very first V2 missile landed in Paris early one morning.

Germany also occupies a unique place in European tv history in that experimental transmissions were made not only on m.f. (30 line 12.5 frames) and v.h.f. (90-line 25 frames in 1932, 180-line from 1933) but also even on long waves (Deutschlandsender 183-.5 kHz, 30 lines, May 1930) and h.f. (January 1931, 48 lines 25 frames on 2100 kHz etc).

The British EMI, Marconi, Cossor teams certainly played a prominent part in establishing electronic television, but we should not forget there were many others actively working in this field. Herr Kniestedt, in 1985, wrote a detailed account of German tv in the 57-page booklet "Die historische Entwicklung des Fernsehens". An account of 50 years of French television is included in the special issue of the *EBU Review*, December 1986.

Teletext struggle

Although there are now approaching 10-million teletext-equipped receivers, with around 3.5 million in the UK alone, the attempts to establish teletext and two-way videotex on the American cable systems have been littered with abandoned projects including those of Time Inc, CBS, NBC, Field Enterprises and Knight-Rider. Only the "WTBS Superstation" of Ted Turner based on Atlanta, Georgia continues to carry a limited 50-page magazine using two lines in the vertical blanking interval. This stems from an 85-page four-line service called "Electra" broadcast on WKRC-TV, Cincinnati and run by MS Hillary Goodall, formerly of BBC Ceefax, with a six person staff.

This service uses the British "World Teletext" standard, but it is recognized that at present there are only a few thousand teletext sets in use in the USA. The cheapest model appears to be a large 270inch receiver retailing at around $1000, with a printer available for an additional $100. One small Californian firm has begun marketing an external teletext adaptor based on British components from one of the abandoned projects.

The WTBS superstation satellite-distributed signals go into the vast majority of American cable homes but it seems to be proving an extremely uphill task convincing American viewers that teletext is a worthwhile addition in a multi-channel environment.

In the UK, with a penetration of around 15 per cent of television homes, the main limitation to growth is that the control units are not considered by many people, particularly those past their youth, as "user-friendly". With average access time down to about seven seconds, the main frustration is either when you need to go through various index pages to reach what you want or when you arrive at the wrong moment on a multipage sequence. The basic problem of remembering wanted page numbers I suppose will eventually give way ot voice-recognition systems whereby the user would simply ask for what he or she wants. Technically feasible, but at a cost that would put teletext well above its "perceived value".

The growth of the British teletext services is impressive. For example, the Oracle sub-titling service for the hard of hearing now has a staff of 22 based in its own premises and using 14 of the "Newfor" subtitle preparation units developed jointly by Oracle Teletext and Southampton University. It produces some 24 hours of teletext subtitles per week and is likely soon to use a dedicated field blanking line (335). The main computer system has also been expanded in recent months with the installation of another six minicomputers connected by an Ethernet local area network. The system currently uses 48 editing terminals, 26 of them located remotely from the main Oracle centre, and with the recently introduced conditional-access service (Subscriber User Groups) offered in conjunction with Air Call Teletext Ltd.

Unlike television, it is fair to claim teletext as a British development – although I am not sure whether any broadcaster would hail it with "Land of Hope & Glory" as it is not easy to make the system pay – except in terms of public-service broadcasting.

Wind turbines

For some years broadcast engineers have found it difficult to ensure good reception in areas adjacent to busy docks, particularly those handling container vessels. This is due primarily to the constantly changing pattern of multi-path (ghosting) due to the reflection and scattering of u.h.f. or v.h.f. signals from tall moving cranes. At Southampton and Ipswich, additional relay stations have had to be provided at carefully selected sites to serve the affected areas to avoid reflections.

Similar problems are already arising from the reflection and scattering of signals by the revolving blades of large electric-power generating wind turbines (p.g.w.ts) that may eventually be erected on many hilltops under the "alternative energy" project. A small prototype p.g.w.t with a blade area of 20 m^2 at Burgar Hill, Orkney has led to the provision since August 1986 of a small relay station serving the few hundred viewers in the locality.

Since much larger wind turbines with blade areas of about 200 m^2 are under construction, theoretical and experimental model studies have been carried out in the UK by service area planning engineers of the IBA. At IBC86, Dr John Causebrook and Dr Henry Palmer of the IBA reported on model experiments carried out at 10.7 GHz. These have confirmed earlier (1979) studies in the USA by Sangupta and Senior. The theory has been extended by the development of methods using diffraction theory to calculate the strength of the scattered signals in the shadow areas behind a p.g.w.t. They suggest that such work should enable broadcast engineers to work with those responsible for building p.g.w.ts to plan locations which would reduce the potential interference to an acceptable level.

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BC108	0.13
BC109	0.14
BC113	0.12
BC114	0.12
BC115	0.12
BC116	0.19
BC117	0.24
BC118	0.30
BC125	0.25
BC126	0.25
BC135	0.18
BC136	0.18
BC137	0.22
BC147	0.12
BC148	0.12
BC149	0.12
BC157	0.12
BC158	0.13
BC159	0.12
BC167	0.10
BC170	0.09
BC171	0.11
BC172	0.09
BC173	0.09
BC177	0.15
BC178	0.28
BC179	0.15

BC182	0.11
BC183	0.09
BC184	0.11
BC212	0.11
BC213	0.11
BC214	0.11
BC237	0.09
BC238	0.09
BC301	0.36
BC303	0.36
BC307	0.09
BC308	0.09
BC327	0.09
BC328	0.09
BC337	0.09
BC338	0.09
BCY30	3.75
BCY31	7.50
BCY32	3.75
BCY33	2.50
BCY34	2.50
BCY39	3.60
BCY40	3.00
BCY42	0.32
BCY43	0.45
BCY58	0.25
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BCY71	0.21
BCY72	0.21
BCZ11	3.50
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BD132	0.42
BD135	0.27
BD136	0.27
BD137	0.30
BD138	0.30
BD139	0.30
BD140	0.30
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BD238	0.35
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BF153	0.19
BF154	0.17
BF159	0.20
BF160	0.20
BF166	0.35
BF167	0.30
BF173	0.45
BF177	0.30
BF178	0.30
BF179	0.30
BF180	0.30
BF181	0.25
BF182	0.30
BF183	0.30
BF184	0.30
BF185	0.30
BF194	0.15
BF195	0.15
BF196	0.15
BF197	0.15
BF200	0.33
BF224	0.15
BF241	0.12
BF244	0.15
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BF258	0.30
BF259	0.30
BF336	0.30
BF337	0.30
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BFS61	0.30

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BFW10	1.04
BFW11	1.01
BFX84	0.28
BFX85	0.28
BFX87	0.28
BFX88	0.28
BFY50	0.28
BFY51	0.28
BFY52	0.28
BFY64	0.36
BFY90	0.65
BSX19	0.27
BSX20	0.27
BSX21	0.27
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OC23	10.00
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OC25	0.79

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OC29	4.40
OC35	4.00
OC36	4.00
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OC42	1.50
OC43	1.50
OC44	1.25
OC45	0.85
OC71	0.65
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OC73	1.45
OC74	1.40
OC75	1.40
OC76	1.60
OC77	2.75
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TIP110	0.10
TIP117	0.45
TIP125	0.35
TIP130	0.45
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TIP132	0.48
TIP135	0.45
TIP137	0.48
TIP140	0.85
TIP141	0.85
TIP142	0.85
TIP2955	0.60
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ZS140	0.25
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ZTX109	0.13
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ZTX303	0.14
ZTX304	0.14
ZTX311	0.13
ZTX314	0.25
ZTX500	0.14
ZTX501	0.14
ZTX502	0.14

ZTX503	0.14
ZTX504	0.20
ZTX531	0.20
ZTX550	0.25
1N914	0.03
1N916	0.03
1N4001	0.04
1N4002	0.04
1N4003	0.04
1N4004	0.04
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1N4006	0.04
1N4007	0.05
1N4009	0.06
1N4148	0.03
1N5400	0.10
1N5401	0.11
1S44	0.04
1S290	0.10
1S921	0.12
2G301	1.00
2G302	1.20
2G306	1.50
2N404	1.50
2N696	0.30
2N697	0.36
2N698	0.38
2N705	2.50
2N706	0.20
2N708	0.22
2N930	0.25
2N1131	0.35
2N1132	0.35
2N1302	1.80
2N1303	0.90
2N1304	3.00
2N1305	1.00
2N1306	3.00
2N1307	1.20
2N1308	4.00
2N1309	1.50
2N1613	0.30
2N1671	5.00

2N1893	0.30
2N2147	8.00
2N2148	2.75
2N2218	0.32
2N2219	0.32
2N2220	0.22
2N2221	0.22
2N2222	0.20
2N2223	7.50
2N2368	0.23
2N2369	0.23
2N2384	0.24
2N2646	0.75
2N2904	0.30
2N2904	0.30
2N2905	0.30
2N2906	0.22
2N2907	0.22
2N2924	0.12
2N2925	0.22
2N2926	0.12
2N3053	0.30
2N3054	0.55
2N3055	0.70
2N3440	0.60
2N3441	0.75
2N3442	1.00
2N3641	0.11
2N3702	0.11
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2N3711	0.10
2N3771	1.20
2N3772	1.20
2N3773	1.60
2N3819	0.50
2N3820	0.60

2N3823	0.80
2N3866	1.00
2N3904	0.10
2N3905	0.10
2N3906	0.10
2N405X	0.12
2N4059	0.20
2N4060	0.12
2N4061	0.12
2N4062	0.15
2N4124	0.13
2N4126	0.13
2N4248	0.25
2N4288	0.15
2N4289	0.12
2N4400	0.12
2N4401	0.12
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E83CC	8.40
E86C	8.25
E88C	8.25
E88C	10.33
E90CC	9.47
E90F	9.90
E91H	6.25
E92CC	8.75
E99F	9.10
E130L	18.50

E180CC	10.50
E180F	12.05
E182CC	13.25
E186F	11.50
E188CC	8.91
E280F	22.51
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E288CC	17.50
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EABC80	1.25
EAC91	3.50
EAF42	2.50
EAF801	2.00
EB41	4.00
EB91	1.50
EBC33	2.50
EBC41	2.50
EBC81	1.50
EBC90	1.25
EBF80	1.50
EBF83	1.75
EBF89	1.50
EBL31	10.00
EC90	1.25
EC91	8.00
EC92	1.75
EC175	462.00
ECC33	4.50
ECC35	4.50
ECC40	5.50
ECC81	1.75
ECC82	1.75
ECC83	1.75
ECC84	1.75
ECC85	1.75
ECC86	2.50
ECC88	3.50
ECC89	2.00
ECC91	8.93
ECC189	2.10
ECC807	1.75
ECC808	3.00
ECF80	1.50
ECF82	1.50
ECF86	2.50
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ECL84	1.50
ECL85	1.50
ECL86	1.75
EF37A	5.00
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EF80	1.75
EF83	4.00

EF85	1.75
EF86	3.50
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EF91	2.95
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EL83	6.00
EL84	2.25
EL86	2.75
EL90	3.25
EL91	7.39
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EL822	13.97
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EM81	2.50
EM84	2.00
EM85	2.75
EM87	2.50
EN32	25.00
EN91	6.50
EN92	6.96
EY51	2.75
EY81	2.50
EY83	2.50
EY84	9.24
EY86	1.75
EY88	1.75
EY500A	3.00
EY802	1.75
EZ35	1.75
EZ40	2.50
EZ41	2.50
EZ80	1.50
EZ81	1.50
EZ90	3.00
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KTW63	2.50
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M8080	8.25
M8081	9.82
M8082	9.69
M8083	10.25
M8091	10.43
M8096	6.80
M8097	8.10
M8098	8.15
M8099	8.00
M8100	10.30
M8136	11.75
M8137	12.25
M8140	6.00
M8141	6.50
M8142	8.75
M9144	7.50
M8149	6.50
M8161	9.35
M8162	11.75
M8163	8.25
M8190	5.00
M8195	10.85
M8196	7.50
M8204	7.05
M8212	11.37
M8223	6.00
M8224	6.30
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MD2901	115.00
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OC2	4.55
OC3	2.50
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OZ4	3.50
PC86	2.50
PC88	2.50
PC95	1.75
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PCC85	1.50
PCC88	2.00
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PCC189	2.50
PCC805	1.60
PCC806	1.60
PCE82	2.00
PCF80	2.00
PCF82	1.50
PCF86	2.50
PCF87	2.00
PCF200	3.25
PCF201	3.25
PCF801	2.50
PCF802	2.50
PCF805	1.70
PCF806	1.70
PCF808	1.70
PCL82	2.00
PCL83	3.00
PCL84	2.00
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PCL86	2.50
PCL805/85	2.50
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PL83	2.50
PL84	2.00
PL504 5	2.50
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PL509	6.00
PL519	6.00
PL801	1.50
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PY83	1.25
PY88	2.00
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ZM1020	9.00
ZM1022	9.00
ZM1023	9.00
ZM1040	19.36
ZM1041	16.66
ZM1042	17.77
1B3GT	3.00
1B24	25.00
1B35A	48.00
1B63	64.00
1R5	1.75
1S5	1.75
1T4	1.75
2AS15	11.50
2C39A	60.00
2C43	70.00
2D21	3.25
2E26	8.25
2J4Z	98.00
2J55	245.00
2J70A	383.00
2J70B	336.00
2K25	125.00
3400Z	115.00
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3A5	3.00
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3B240M	17.50
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6AG7	3.00
6AH6	5.00
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6AK6	2.50
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6AQ5	3.25
6AS6	8.66
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6F23	1.60
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6F33	33.50
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6H3N	2.75
6H6	3.00
6J4	5.50
6J6	8.93
6J7	4.75
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6K4N	2.50
6K6GT	2.75
6K7	3.00
6K8	3.00
6KD6	8.00
6L6G	5.00
6L6GA	3.50
6L6GC	5.75
6L6GT	3.00
6L7	2.50
6N2P	2.50
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6N7	3.00
6P225	4.00
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6SQ7	3.40
6SR7	4.00
6SS7	2.75
6U5G	3.50
6U8A	2.25
6V6GT	4.25
6X4	3.00
6X5GT	1.75
7B7	2.50
7C5	4.00
7C6	2.50
7H7	4.00
7R7	4.25
7S7	3.50
7Y4	2.25
7Z4	2.00
12AH8	5.00
12AT6	1.50
12AT7	1.75
12AU6	2.50
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12AV6	2.50
12AW7	3.50
12AX7	1.75
12AY7A	4.00
12B4A	3.50
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12BY7	3.00
12E11 PT	28.00
12E14	65.00
12E1	20.00
13E1	170.00
19H5	47.50
24B9	67.25
30C15	2.00
30C17	2.00
30C18	2.00
30F5	1.60
30FL1 2	1.38
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30FL14	2.00
30L1	1.50
30L15	2.00
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5651	4.45
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5675	28.00
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5726	11.37
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5749	2.50
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5879	5.00
5886	17.50
5963	2.50
5965	3.50
6005	2.25
6021	4.50
6057	12.25
6058	12.34
6059	6.00
6061	6.00
6063	3.75
6064	10.25
6067	11.75
6072	6.00
6080	14.00
6097A	235.00
6097B	200.00
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6146B	12.00
6159B	19.00
6189	9.50
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6550	8.00
6883B	12.50
6973	7.50
7025	3.00
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7400	0.35
7401	0.36
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7403	0.36
7404	0.42
7405	0.42
7406	0.48
7407	0.55
7408	0.36
7409	0.36
7410	0.36
7411	0.40
7312	0.42
7413	0.36

7416	0.48
7417	0.48
7420	0.48
7422	0.36
7423	0.36
7424	0.36
7427	0.36
7428	0.36
7430	0.36
7432	0.36
7433	0.55
7437	0.36
7438	0.36
7439	0.36
7440	0.36

7441	0.48
7442	1.25
7450	0.30
7451	0.30
7453	0.30
7454	0.30
7460	0.30
7470	0.48
7472	0.30
7473	0.48
7474	0.36
7475	0.65
7476	0.48
7480	0.32
7483	0.48

7484	0.72
7486	0.54
7490	0.72
7491	0.36
7492	0.54
7493	0.54
7494	0.78
7495	0.65
7496	0.60
7497	3.90
74100	0.84
74107	0.36
74109	0.54
74110	0.48
74111	0.51
74116	1.50
74118	1.20
74119	1.50

74120	0.75
74121	0.54
74122	0.70
74123	0.60
74125	0.60
74126	0.54
74128	0.55
74136	0.70
74141	0.46
74143	1.30
74145	0.72
74147	1.50
74148	1.40
74150	1.60
74151	0.36
74154	1.40
74155	0.60
74156	0.48

74159	1.75
74170	1.20
74172	4.00
74173	0.72
74174	0.60
74175	1.00
74176	1.00
74180	1.48
74190	1.20
74191	1.20
74192	1.10
74193	0.60
74194	1.10
74195	0.72
74196	1.00
74197	1.00
74198	2.20
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RADIO COMMUNICATIONS

PAT HAWKER

Mobile packets

The growing interest in packet-based switching systems for digital telecommunications networks is extending to the potential use of such techniques in large civilian cellular mobile-radio networks and also for secure tactical military communications systems.

AT&T Bell Laboratories have investigated the transmitting of packetized voice and data on cellular mobile networks operating between 800 and 900 MHz (see M.R. Karim, *AT&T Technical Journal*, May/June 1986, pages 12 to 20).

The major problem with mobile data transmission has always been that the signal undergoes pronounced multipath fading because of the scattering and reflections from buildings and other obstructions. The amplitude of the incoming signal at any point over distances of a few hundred wavelengths varies randomly about a mean level with a Rayleigh distribution, while its phase is uniformly distributed between 0 and 2π. M.R. Karim points out that with conventional f.m., analogue speech reception is frequently interrupted by short noise bursts that appear in the form of pops and clicks. Fades on data transmission cause error bursts. To overcome these it is usual practice to use error-correcting codes and repeated transmission, leading to significantly reduced throughput in order to achieve some degree of robustness.

However, when digital signals are transmitted in the very short bursts of packet radio most of the packets will be accepted by the receiver on its first transmission, since most will occur between fades. In only a limited number of cases will automatic retransmission be required.

The Bell study is based on high level data link control (h.d.l.c.) procedures as defined by the International Standards Organization, although this protocol has not been designed specifically for use on fading channels. In h.d.d.c. a 16-bit frame-check sequence is used to detect transmission errors. Unlike more conventional data transmission systems, as long as the system is in connected mode, there is virtual assurance that a packet receiver will not accept for display a packet that has acquired errors during transmission: "If you get it, you get it perfectly." Because of the short bursts of specifically "addressed" packets, it is possible for many stations to share a single-frequency channel.

The Bell Laboratories study shows that a good throughput can be achieved at u.h.f. at vehicle speeds up to about 70 m.p.h. with the average "delay" a function of packet size. While the average delay increases significantly with increasing packet length, the choice of a very small packet increases the percentage of "overheads" and housekeeping signals and thus tends to reduce the effective throughput.

It is clear that, at least theoretically, there is a useful range of values of packet size over which the delay is small and efficiency high. This opens up the possibility of transmitting packetized speech and data on mobile radio channels with high spectrum utilization efficiency.

Already increasing use of packet techniques is being made on the 144 MHz amateur band both in Europe and the USA. In the UK many of the planned national network are now in operation.

In the USA, portable "two camera-case" packet stations have been developed for emergency and public-service communication while for general amateur use some 20,000 packet systems have now been bought or assembled. Transmission speeds on 144 MHz are of the order of 1200 w.p.m.

Expanding world of e.m.c.

Although electromagnetic compatibility problems have been with us for at least as long as broadcasting, it remained a little-regarded and rather esoteric aspect of professional radio engineering for many years. But a number of factors have emerged in recent years that now combine to turn e.m.c. into a major problem area in almost all branches of electronics. There was, for instance, the need to pack a number of receivers and transmitters in close proximity in a single, small, space satellite or on board a naval vessel; there was the susceptibility of c-mos and other semiconductors to r.f., including lightning and nuclear electromagnetic pulses; the problem of high-speed digital pulses escaping from computers (and thus making them vulnerable to convert reading of their contents or enciphering mechanisms); the spurous r.f. radiation from thyristors, switched-mode power supplies and the like; the widespread use of plastic rather than metal cabinets and enclosures; the vulnerability of semiconductor devices to voltage transients; the use of vulnerable devices in vehicles and industry that can prove hazardous due to r.f.i.; the growing problems of spectrum abuse and the increased sensitivity of u.h.f. and microwave receivers... etc, etc.

Today there are an increasing number of university courses, conferences and symposia concerned with e.m.c. There is also increased recognition that many design engineers working in the field of domestic and automotive consumer-electronics remain almost totally unaware of the extent of e.m.c. problems. The world of "electronic smog" is made more difficult by the lack of foresight in the "sunrise" industries! Sometimes accidental, sometimes, one suspects, due to shutting of eyes for economic motives.

However the current flurry of professional interest in e.m.c. is yielding ideas and information of interest to us all. I have been dipping into IERE Conference Publication No 71, which gives the 45 or so papers presented at the 5th International Conference on Electromagnetic Compatibility held at the University of York, October 1 to 3, 1986.

For example, a portable test set for r.f. interference from applicances, designed to measure radiation on 160kHz (considered the most vulnerable section of the spectrum to appliance r.f.i.) was taken to two stores, one a well run, city-centre showroom for retail centres; the other a busy, reputable, tool-hire firm. In the first, a quick test of 11 appliances ranging from a liquidizer to vacuum cleaners showed all to be within BS800 limits at the test frequency. But in the tool-hire business, ten hand tools were tested, including grinders, drills, sanders and saw. Five of the 11 were outside the by-no-means demanding limits of BS800.

A University of Kent project aimed at measuring electrical noise on ships and its potential effect on radio communications shows that locally-generated electrical noise is the most significant component of the background noise. Tests carried out on four cross-Channel ferries and a container ship indicate that man-made noise can be of a level to significantly degrade the performance of communications systems.

The German broadcast research organization (IRT, Munich) has, like a team at Bradford University, been investigating hazards in the vicinity of powerful radio transmitters from the influence of electromagnetic fields on electro-explosive devices. IRT has developed "worst case" estimates based on an impedance concept in which the real power absorbed in detonators is calculated, but showing that probability of this situation is many orders of magnitude smaller, of the order of 10^{-5} (i.e. only one second per day). In itself this reduction of probability compared with worst-case hazards is not significant, since transmitters may be operating 24 hours per day and it takes less than a second to detonate an explosive! However the Germans do agree with Dr Peter Excell ("Feedback", *E&WW*, December 1986 that "worst case" calculations greatly overestimate the real risk. Nevertheless I would defend my earlier misgivings in respect of BSI departure, under Government pressure, from this basis in radio-frequency hazards generally. Murphy's Law is not to be disregarded lightly. The suggestion that we might still be carrying red flags in front of motor vehicles only serves to remind us that, in the UK alone, we now have some 5000 fatalities yearly from traffic accidents. "Worst-case" scenarios are not popular with the nuclear industry but few of us would wish to disregard such possibilities after Chernobyl! The idea that radio amateurs should not draw attention to such risks seems an odd comment on journalistic responsibilities!

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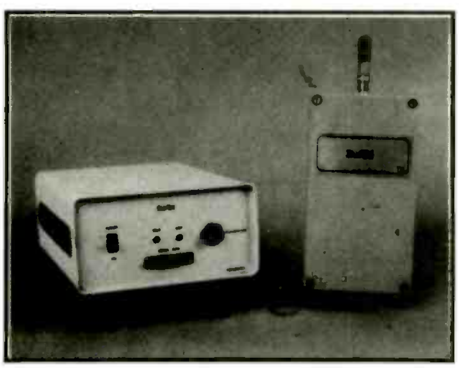

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APRIL 1987 **Spectrum analysers.** Advances in the application of microprocessors to these instruments have opened up a wider area of use. Those on the UK market are listed and new techniques examined.

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Single-ended conductance

New features and circuit functions emerge from this analysis of what is effectively a new circuit element.

GORDON SHAW

Resistors, capacitors and inductors – the only linear passive components that we know – can be connected in an infinite number of ways, but what they can achieve alone is quite limited. It would be exciting to discover a new linear network element.

Additionally of course there are amplifiers, and although they are active devices we can pretend they are linear for most of the time. Together with Rs, Cs and Ls they extend our freedom to create a wide variety of analogue networks.

Standard methods analyse the behaviour of a circuit once we know its topology and composition. Ignoring non-linearities – both the hard ones produced by diodes, magnetic materials, large-signal amplifiers etc, and the more subtle ones associated with all devices – analysis can begin by producing an equivalent circuit consisting of an interconnection of component models. A few straight lines and circles on paper, the concept of impedance or admittance (Ohm's law), and an agreement about dependent generators and the circuit can be completely modelled. Follow this with some mathematical manipulation, apply a Kirchhoff Law or two and we can achieve the prime objective of analysis, which is to predict the performance of the circuit in terms of functions such as voltage gain and input impedance.

Such analysis may well reveal that the requirements of the circuit have not been achieved. The solution may be to modify the circuits, but there are obviously constraints produced by having only a few device types to work with. If we had another type with different laws governing its behaviour it may well be possible to achieve otherwise unattainable functions – or at least similar functions – with fewer components.

This article introduces the single-ended conductance, which, because of the laws governing its behaviour can achieve the benefits of a new type of device.

The idea originated while devising ways of electronically varying the parameters of a filter, as distinct from manual knob control. Starting from the electronic simulation of a variable resistance it became evident that a simplification (which produced the seg) could lead to other advantages, especially cheaper implementation, modified and improved filter performance, including greater Q-factor and a new mode of control for the topology. The last factor suggests it can be viewed as a new type, which the nodal admittance matrix confirms. All these points are discussed in what follows and a practical example is analysed to illustrate the principles.

Those of a sensitive mathematical disposition are warned that this article contains descriptive passages which may offend the pedantic. You are left to judge whether the seg is an artefact of practical value, like the gyrator for example, or whether, like the negative impedance converter, it should remain as a theoretical idea, not worth spending time on[1].

NODAL ADMITTANCE MATRIX AND PIVOTAL CONDENSATION

The technique of pivotal condensation on the nodal admittance matrix leads to a systematic procedure for determining transfer and immittance functions for a linear circuit. The detail of the procedure is included in the panel on page 222, but if you require a more comprehensive refresh consult one of the many texts, such as reference 2.

Consider the indefinite admittance matrix for a transmission network having n nodes connected by linear passive admittances and dependent generators. The indefinite matrix will have n×n elements and the value of each passive component will appear in four of these elements; an external reference node is implicit and the matrix contains redundant information. The redundancy is removed by making one of the internal nodes the reference: there is usually a ground or earth common to input and output which an be conveniently chosen. The resultant matrix is obtained by removing the row and column associated with the internal reference node.

The new matrix is usually called the definite admittance matrix and will be of size

Gordon Shaw introduces the concept of the seg or single-ended conductance and suggests how it can be implemented in RC networks. Argueing from a basis of a standard network analysis he demonstrates that it can be regarded as a new linear device with desirable changes in circuit performance when embedded in a well-known active filter section.

The seg can be substituted for a conductance in any linear network without altering the transfer function, provided that the non-conducting end of the seg is tied to a constant-voltage point. Used in place of a floating conductance, the maximum pole Q-factor is significantly enhanced, and as a variable element the seg not only enables adaptive control but also adds a desirable alternative mode, as well as reducing the component spread needed for a given pole Q-factor.

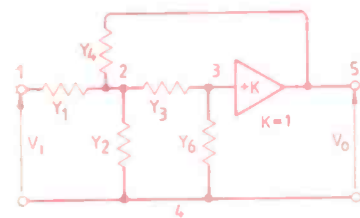

Fig.1. Example of a general second-order active filter section with nodes numbered in preparation for analysis. The gain-defining feedback circuit which makes K=1 is omitted.

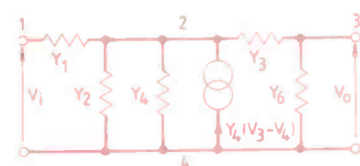

Fig.2. Simplified circuit model of Fig.1 where node 5 has been removed. This allows the indefinite admittance matrix to be written by inspection prior to its reduction by pivotal condensation.

$(r-1)\times(n-1)$. Further reduction is obtained by pivotal condensation about each inner node in turn until only a 2×2 matrix remains, dimensioned in terms of the input and output nodes, i and o say. Then the condensed matrix [Y] can be represented in general form:

$$[Y]=\begin{bmatrix} y_{ii} & y_{io} \\ y_{oi} & y_{oo} \end{bmatrix} \qquad (1)$$

from which the voltage gain may be deduced because:

$$A_v=-y_{oi}/y_{oo}$$

To illustrate this technique, consider an active filter network as shown in Fig.1, recognised as a Sallen and Key type. K is the defined gain of an operational amplifier with resistive feedback, for this illustration assumed to be unity implying that the operational amplifier is simply connected as a voltage follower. While this simplifies the following arguments it does not trivialise the circuit; the unity-gain Sallen and Key filter is useful, provided that the required Q-factor is fairly low (say about three or less).

The nodes of Fig.1 are numbered in preparation to write the indefinite matrix but first, a little simplification. Because K=1 the voltage at node 3 is the same as at node 5:

$$v_o=v_5-v_4=v_3-v_4.$$

The amplifier can be removed if replaced by a suitable equivalent. This is conveniently done, assuming normal amplifier idealities, by considering the output voltage v_5-v_4 to be connected in series with an impedance of $1/Y_4$ and performing a Norton transformation on the combination. These manipulations effectively remove node 5 and the variable v_5. The result is shown in the circuit model of Fig.2.

As the voltages at the nodes 3 and 5 are equal, for the purpose of determining the voltage gain, the output voltage is that between nodes 3 and 4. Thus the indefinite matrix can be written directly by (careful) inspection of the network of Fig.2, to give equation 3:

$$[Y]_I=\begin{array}{c c} & \begin{array}{cccc} 1 & 2 & 3 & 4 \end{array} \\ \begin{array}{c} 1 \\ 2 \\ 3 \\ 4 \end{array} & \begin{bmatrix} Y_1 & -Y_1 & 0 & 0 \\ -Y_1 & \Sigma Y & -Y_3Y_4 & -Y_2 \\ 0 & -Y_3 & Y_3+Y_6 & -Y_6 \\ 0 & -Y_2-Y_4 & Y_4-Y_6 & Y_2+Y_6 \end{bmatrix} \end{array} \qquad (3)$$

where $\Sigma Y=Y_1+Y_2+Y_3+Y_4$. Then a definite matrix can be produced by choosing node 4 as the logical reference node:

$$[Y]_D=\begin{array}{c c} & \begin{array}{ccc} 1 & 2 & 3 \end{array} \\ \begin{array}{c} 1 \\ 2 \\ 3 \end{array} & \begin{bmatrix} Y_1 & -Y_1 & 0 \\ -Y_1 & \Sigma Y & -Y_3-Y_4 \\ 0 & -Y_3 & Y_3+Y_6 \end{bmatrix} \end{array} \qquad (4)$$

Condense about node 2:

$$[Y]=\begin{array}{c c} & \begin{array}{cc} 1 & 3 \end{array} \\ \begin{array}{c} 1 \\ 3 \end{array} & \begin{bmatrix} Y_1-\dfrac{Y_1^2}{\Sigma Y} & \dfrac{-Y_1(Y_3+Y_4)}{\Sigma Y} \\ \dfrac{-Y_1Y_3}{\Sigma Y} & Y_3+Y_6-\dfrac{Y_3(Y_3+Y_4)}{\Sigma Y} \end{bmatrix} \end{array} \qquad (5)$$

Hence from equation 2:

$$A_v=\frac{Y_1Y_3}{(Y_3+Y_6)\Sigma Y-Y_3(Y_3+Y_4)}\ \text{i.e.}$$

$$A_v=\frac{v_o}{v_i}=\frac{Y_1Y_3}{Y_6(Y_1+Y_2+Y_3+Y_4)+Y_3(Y_1+Y_2)}. \qquad (6)$$

Equation 3 reveals that each of the admittance values representing a passive component appears four times. More specifically, the individual admittance terms appear twice in two rows and twice in two columns, thus the four appearances lie at the corners of an imaginary rectangle.

The appearance of an admittance term (Y_x, say) in a diagonal element occurs because it has been assumed that a positive current flows through that admittance *away* from the node in question when a contrived voltage is applied to that node (of the same number as the row and column). Y_x appears again elsewhere in that row, (with a negative sign) because an imagined voltage applied to the other end of Y_x at an adjacent node (of the same number as the column) would cause an equal positive curent to flow *toward* the original node. (It may be convenient to visualize the end of the admittance connected to the original node acting as a current sink, giving rise to the term in the diagonal element, and then separately as a current source, giving rise to the negative component of the other element in the same row.) A similar argument applied to the node at the other end of Y_x explains why the admittance term reappears, yet again, twice in another row.

These descriptive arguments can sometimes be more confusing than helpful. I suppose it depends on one's background knowledge and method of reasoning. However the intention here was to justify the following statement.

Statement 1: When a passive admittance having a value of Y_x is connected between two nodes j and k, Y_x will appear twice in the jth row because the admittance is capable of both sourcing and sinking current from the jth node. Similarly Y_x will also appear twice in the kth row because it has the same capability with respect to the kth node. The occurrences of Y_x will appear in the jth and kth columns.

The quadrate property is fundamental to the individual passive admittance terms in the indefinite matrix and can be checked in this particular topology by adding an extra component between any existing nodes and reconstructing the matrix. The point is that you cannot add a single passive component to a circuit without it reflecting a corresponding Y value into four of the elements of the matrix according to the rules as outlined. For example, it would not be possible to add an extra admittance to the network of Fig.2 in such a way as to modify the elements of the matrix in equation 3, subscripted 22 and 23 alone. For that change to be physically realisable then elements 32 and 33 would also be similarly modified. This rigid structural property is peculiar to the indefinite matrix, complete with its redundancy.

Once the matrix is reduced to its definite form the integrity of this pattern is destroyed. By definition, the elements of the indefinite matrix associated with the reference node are removed. Using the previous type of argument, those passive admittances connected to the reference node do not appear to act as either current sources or sinks at the end connected to the grounded node – not because they are any different from the others, but because there cannot be any signal voltage applied to them at that node. (The argument is not complete but I do not pursue it further.)

The only admittances which retain their original quadrate pattern of the particular example chosen are Y_1 and Y_3. However there is a further observation. The process of pivotal condensation and equation 2 show that the elements of the row associated with the input node do not enter into the expression for A_v. This could be attributed to the fact that the presence of Y_1 (in our example) will not cause any change in the source voltage v_i no matter what current is caused to flow to, or away from the source. The ground has now been prepared for statement 2.

Statement 2: The elements of the rows of the i.a.m. associated with the reference node and the input node play no part in determining the transfer function A_v.

Before developing the ideas further consider the underlying theory of a specific circuit which can then be used as a particular example to illustrate the seg's applications.

LOW-PASS FILTER SECTION

An RC active filter is generally made up of a series of second-order sections to maintain reasonable passive component sensitivities (a first-order section would be added if the overall order is odd). The general form of the transfer function of a second-order section is

$$T(s)=\frac{P(s)}{s^2+B_ps+\omega_n^2} \qquad (7)$$

where P(s) is a quadratic in s (or simpler), ω_n is the undamped natural angular frequency, $B_p=\omega_n/Q_p=2\xi\omega_n$ is the angular pole bandwidth, Q_p is the pole Q-factor, ξ is the damping factor.

Q_p and ω_n are familiar parameters which allow the function to be specified in practical terms. The denominator quadratic specifies the poles of the system and P(s) specifies the zeros. Fig.1. enables the synthesis of sections with a variety of P(s) forms and hence a variety of well-known responses such as low, high, and bandpass are practical. In the case of the low-pass function, used here as an example, it is usual to position the zeros of transmission, thus the numerator polynominal becomes diminutive and equal to the constant ($\omega_n^2\times$ gain).

To decide which of the admittances in Fig. 1 are to be of the form G (pure conductance) and which are to be of the form sC (pure susceptance), refer to equation 6. The numerator is a constant (i.e. no s or s^2 terms) hence $Y_1=G_1$ and $Y_3=G_3$. The denominator requires more thought: the expression $Y_6(G_1+Y_2+G_3+Y_4)$ + $G_3(Y_1+Y_2)$ must contain an s^2 term, an s term and a constant. Once it is realised that Y_2 is surplus to requirements we can set $Y_2=0$, then there is an explicit solution: $Y_4=sC_4$ and $Y_6=sC_6$. Fig. 3 shows the resulting circuit for which the transfer function may be written from equation 6 as T(s)=

$$\frac{v_i(s)}{v_o(s)}=\frac{G_1G_3/C_4C_6}{s^2+s(G_1+G_3)/C_4+G_3G_1/C_4C_6}. \qquad (8)$$

Identifying the coefficients of the denominators of equations 7 and 8

$$\omega_n=\sqrt{\frac{G_1G_3}{C_4C_6}} \qquad (9)$$

$$B_p=\frac{G_1+G_3}{C_4} \qquad (10)$$

$$Q_p=\frac{\sqrt{G_1G_3}}{G_1+G_3}\sqrt{\frac{C_4}{C_6}}. \qquad (11)$$

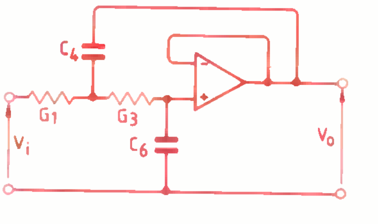

Fig.3. Explicit diagram of a low-pass version of Fig.1. It is a unity-gain Sallen and Key circuit and may suffer from high sensitivity to the f_T of the amplifier and may call for a high component value spread if the required Q-factor is not low.

It is worth noting that Q_p is maximum when $G_1 = G_3$

$$\text{i.e. } Q_p\text{max} = \tfrac{1}{2}\sqrt{\frac{C_4}{C_6}}. \qquad (11a)$$

SENSITIVITY AND VARIABLE CONTROL

Parameters ω_n, B_p and Q_p have been chosen because they have particular meaning to the designer: nowhere is this more evident than in the case of the second-order band-pass filter where centre frequency, 3dB bandwidth and Q-factor have obvious significance with respect to the amplitude response. In other cases the identification is not so transparent, ω_n is not necessarily the cut-off frequency nor B_p the 3dB bandwidth (that is why it is referred to as the pole bandwidth, and not simply bandwidth). However, these parameters do have a presence in the mathematics of all the second-order sections and a physical significance which can be, more often than not, fairly easily recognised. Figure 4 illustrates some of these relationships. Observe that the three parameters are not independent; because $B_p = \omega_n/Q_p$, if any two are specified the third is defined. It is the sensitivity of these parameters to the passive component values – especially ω_n and Q_p – that dominated the literature on active filters for many years.

Let P represent one of the parameters and x the value of a component, then the sensitivity of P with respect to x is

$$S_x^P = \frac{\partial P/P}{\partial x/x}. \qquad (12)$$

It is a straightforward though tedious task to calculate S_x^P for ω_n and Q_p to all of the individual components in a network. Equation 9 reveals, as examples:

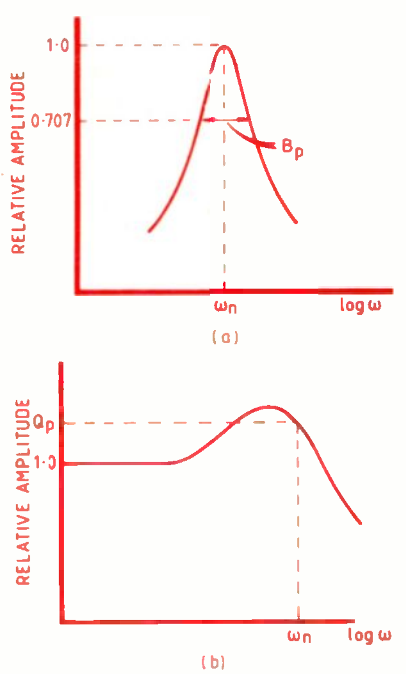

Fig.4. Simple illustrations of the physical significance of the parameters ω_n, B_p and Q_p with reference to the amplitude responses of bandpass filter (a) and low-pass filter (b).

$$S_{C1}^{\omega_n} = \tfrac{1}{2},\ S_{C6}^{\omega_n} = -\tfrac{1}{2},\ S_{R1}^{\omega_n} = -\tfrac{1}{2} \qquad (13)$$

where $R_1 = 1/G_1$.

One way of interpreting the concept of sensitivity is to consider it as a measure of the perturbation of the parameter with relation to the error in a component value (inevitably caused because that value cannot be precisely correct nor will it remain absolutely constant). Interpreted loosely this would mean that if R_1 were 1% high there would be a corresponding ½% fall in ω_n. This sensitivity figure of ½ (plus or minus) is generally considered to be an ideal because it is what would be expected from a passive filter. The general conclusion therefore seems to be that low sensitivity is good.

Nevertheless it is not the whole story, and this becomes apparent where we intend to introduce variable control. Consider for the moment that we have a suitable variable capacitor and that we require to vary ω_n at constant pole-bandwidth. Equations 9, 10 and 11 show that this would be possible if C_6 were variable: the controlling law would be a reciprocal square-root law.

This is implicit in the sensitivity results of equation 13 (because $S_{C6}^{\omega_n} = 4$, where the negative sign indicates the reciprocal and the ½ indicates the square root). In general, the evaluation of sensitivities with respect to resistance and capacitance for a wide variety of networks indicates that the reciprocal and square-root relationships are a regular occurrence and that is not attractive.

I have argued that linear control of the parameters is desirable[3] and this means that the law of the manipulation device should ideally be complementary to the associated sensitivity. This means that C_6 should vary according to an inverse square law as the input control is varied linearly and it is unlikely that we shall ever be lucky enough to find a device with an accurately prescribed law when that law is so complicated.

Perhaps it is unfair to consider capacitance as the controlling element because active filters are at their best at low frequencies and the required capacitance values much too large for available devices. Variable resistors are a much better proposition but they would also be expected to operate with the same contorted law as the capacitor. This begs the question as to what alternative variable components there are.

Calculating sensitivities and searching for variable devices having complementary controlling laws is an open-ended task. Suitable variable devices are not thick on the ground; for manual control the list begins with variable resistors. What is really needed of course, heeding previous observations, is a variable conductance, which is different.

When it comes to electronic control we are in the world of invention. One of the favourites is the switched capacitor (q.v.); there are also the fet, the linear current-controlled conductance[3], the transconductance amplifier, and more. Generally such devices are likely to produce distortion and add significant complexity to the original filter, though these penalties do not necessarily exclude their use.

In summary I would like to see a gadget with a conductance linearly related to the input variable; in this context I will discuss the transconductance amplifier.

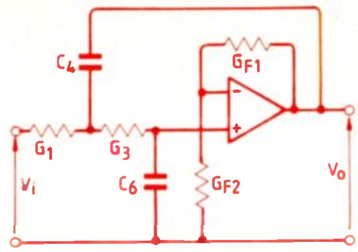

Fig.5. Alternative low-pass circuit to that of Fig.3. – sometimes referred to as the 'gain-of-three' Sallen and Key section – may suffer from high sensitivity to component values.

ACHIEVEMENT OF HIGH Q

Before proceeding on that line, consider the ability of networks to allow the achievement of high Q-factors, because, as a later example will show, this is pertinent to one of the advantages of the seg. Frankly, we rarely need high Q but a circuit which has this ability is at least of academic interest and might occasionally offer some tangible benefits. There are going to be some sweeping statements in this section but so long as they are not misleading generalisations can be valuable.

Active filters may suffer from one or more of three main weaknesses compared with passive filters. First, there is a possible limitation if the passive component sensitivity, S_x^P, is high. Although not a major problem in the circuit of Fig.1, it may be in others, for example the Sallen and Key so-called gain-of-three section illustrated in Fig.5. If a high Q is required this flaw will be exaggerated and there is little that can be done to alleviate it.

Second, there is a sensitivity to the non-idealities of active components. In practice this usually means that the limited gain-bandwidth product (f_T) of the operational amplifiers may upset the response. The concept of active component sensitivity is slightly more difficult to come to terms with than S_x^P reference 4 put these two sensitivities into perspective and is recommended for further reading. There is a family of filters which suffers mainly from high active sensitivity while having a low passive sensitivity. Examples are the circuit of Fig.3 and the state-variable three-amplifier filter section shown in Fig.6 (ref 5). However it has been shown that amplifier sensitivity can be alleviated; see ref.5 for the improvement of the three-amplifier sections and 7 for single-amplifier networks. Reference 3 shows that the Q-factor of the state-variable network can with certain simplifications, that is $R_9C_2 = R_8C_1$, $R = R_3$ and $R_2 >> R_1$, be reduced to

$$Q_p \approx \tfrac{1}{2}\frac{R_2}{R_1}$$

and provided the compensation technique described in ref.5 is used it is practical to achieve a respectably high Q-factor. These state-variable realisations are accepted as being amongst the best of the RC feedback inductorless sections, but the price that has

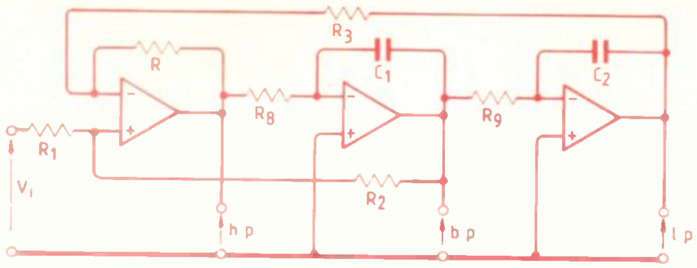

Fig.6. The Kerwin, Heulsman and Newcomb state-variable network can give high-pass, band-pass and low-pass functions without modification. Classed as one the best types, it nevertheless may be sensitive to the finite gain-bandwidth product of the op-amps. The need for three amplifiers has obvious disadvantages.

to be paid is the use of all those amplifiers. By comparison the single amplifier network has its obvious advantages, but it is not possible to achieve a high Q-factor with it, even when partially corrected for the limited f_T.

Part of the reason is the need for large component value spreads and this is a third weakness which may afflict active filter networks. To illustrate, imagine that the circuit of Fig.3 is required to produce a pole Q-factor of 50. Equation 11a reveals that a component spread (C_4:C_6) of 10,000 would be needed. There is a practical upper limit to the larger capacitance we can choose due to economic and reliability constraints and there is a lower limit because a very small capacitance may become comparable with unknown strays. In practice the component spread must be kept very much lower than 10,000 and therefore the achievable Q-factors with the unity-gain section cannot be high.

I do not pretend that the extensive subject of optimising sensitivities has been explained and summarised adequately here. The object however is to draw attention to the intrinsic limitation imposed by an expression typified by equation 11(a), characterised by the square-root of a simple ratio which is bound to require a wide component spread if a large Q_p is needed. On the other hand the more complex circuit which leads to equation 14 is much more acceptable because the Q-factor is approximately directly proportional to the ratio of the component values, not to their square root.

SIMULATION OF A VARIABLE CONDUCTANCE

In the search of an equivalent variable conductance or resistance with electronic control, consider the equations which define the relationship between current and voltage, both for the conductance itself and for an operational transconductance amplifier. The RCA 3080 is an available o.t.a. (ref.8) and with reference to Fig.7(a), the mutual conductance G_m is

$$G_m = i_o/(e_x - e_y).$$

G_m can be set over a wide range (about four decades) by programming the d.c. current I_B.

Fig.7(b) shows a simple conductance connected between two nodes x and y, and clearly:

$$G = i_y/(v_x - v_y).$$

By observation, the o.t.a. can simulate the current flowing toward node Y(i_y) if $G_m = G$, $e_x = v_x$ and $e_y = v_y$. This is achieved by setting I_B correctly (for the 3080, $G_m = 19.2\ I_B$) and connecting as shown in Fig.8.

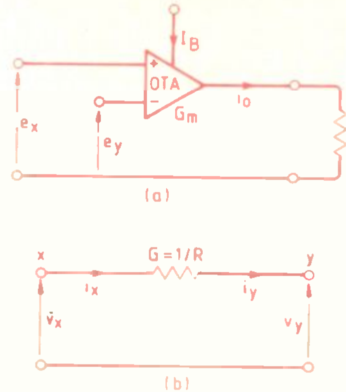

Fig.7. Comparing the terminal voltages and currents of an operational transconductance amplifier (a) and a simple conductance (b).

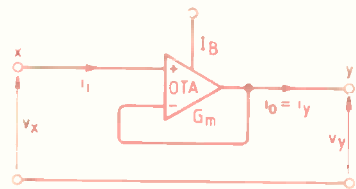

Fig.8. How a single operational transconductance amplifier may be connected to make $i_o = i_y$ (of Fig.7. when the terminal voltages are indentical. *This arrangement is in fact the seg.*

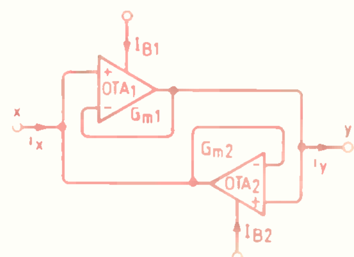

Fig.9. Use of the two transconductance amplifiers enables complete simulation of conductance when $I_{B1} = I_{B2}$. Then G=G $\approx 19.2 I_B$.

This arrangement is not a complete simulation of the conductance since idealiy i_i will be zero and therefore there is no current equivalent to i_x flowing from node x. Obviously i_x should be the same as i_y, therefore two amplifiers can be connected as Fig.9 to complete the simulation, provided that the two bias currents are nominally equal.

You could be forgiven for thinking that the circuit of Fig.9 is an expensive substitute for a variable resistance. But there are two features which distinguish it from the common potentiometer. It allows electronic control by varying the current I_B and therefore could be useful in an adaptive mode of operation. And second, the relationship between the input variable (I_B) and the output variable (G_m) is a linear one. The fact that it is linear and that we are controlling conductance rather than resistance are likely to be to our advantage.

Without yet suggesting that there is any practical value in doing so, G_1 and G_3 in

HOW TO FORM AN INDEFINITE ADMITTANCE MATRIX

This method allows the i.a.m. to be written by inspection for a net-work containing linear passive components and voltage-controlled current generators.

For a network containing n nodes, an nxn matrix [Y] will be produced of the general form:

$$[Y] = \begin{bmatrix} y_{11}\, y_{12} \cdots\cdots y_{1n} \\ y_{21}\, y_{22} \cdots\cdots y_{2n} \\ \vdots \\ y_{n1}\, y_{n2} \cdots\cdots y_{nn} \end{bmatrix}$$

Define each forward diagonal element in general by y_{kk}. Then y_{kk} is the admittance operator, equal to the total current which would flow away from the kth node if a unit voltage was applied to that node and the voltages at all other nodes were reduced to zero.

Define each of the other elements of matrix in general by y_{kj}. Then y_{kj} is the admittance operator, equal to the total current which would flow away from the kth node if a unit voltage was applied to the jth node and the voltages at all other nodes were reduced to zero.

If these definite statements are not familiar, it may be because of the way in which they have evolved to cope with dependent generators. The specific wording has been developed to more clearly support the context of the current topic. In electronic circuits it is common to find both current and voltage generators, when it is then convenient to transform voltage generators to current generators by a Norton transformation.

Mechanism of pivotal condensation

An m×m matrix may be reduced to an (m−1)×(m−1) matrix by the simultaneous removal of row numbered x and column numbered x if all the remaining elements are suitably modified. If each element in question is represented typically by y_{kj} (and in this case k may be equal to j but neither k nor j may be equal to x) then the modified element becomes y'_{kj}, where the appropriate transformation is

$$y'_{kj} = y_{kj} - \frac{Y_{kx} Y_{xj}}{y_{xx}}.$$

Fig.3 could each be replaced by the conductance of Fig.9. However, G_1 is different from G_3 and a simpler arrangement would suffice. Because of statement 2 and the argument preceding it, o.t.a. is not needed for the simulation of G_1: the implementation of Fig.8 would do just as well. So when a simulated conductance is connected either to the input node or to ground, only one of the o.t.as is necessary for complete emulation. The circuit of Fig.8 (or its mirror image) is the single-ended conductance.

ANALYSIS OF SINGLE-ENDED CONDUCTANCE

The immediate advantage of being able to use the seg instead of the full circuit of Fig.9 is one of economy, because in the example just cited three o.t.as were used instead of four. In principle, the circuit would function quite conventionally either way, but the saving is not an impressive one.

We have established that a floating conductance such as G_3 requires two o.t.as for complete simulation while a conductance tied to ground or to a constant-voltage source such as G_1 is only needs one. What would happen if a floating conductance were to be replaced by the seg? Circuit behaviour would be changed – forget about economy – and the functional differences might be quite interesting.

Take the same example (Fig.3), replace G_1 and G_3 by the seg and company the analysis of this new circuit Fig.10 with that of the original. The new symbol represents the seg; the lower case g identifies changes that may occur in the mathematics. The pointed end of the symbol indicates the output end of the seg and although it looks like an arrow head, it should not be confused with a directional indicator; it is there to locate the end where current flows. This current can flow either way, as appropriate to a source or a sink, but no current flows at the opposite end of the seg.

The original analysis started from the circuit model of Fig.2 and is described in equations 2 to 11a. In order to draw an accurate comparison then, we can start from the same model except that Y_1 and Y_3 must be treated as special components. Y_1 will not source or sink current at node 1 and Y_3 will not source or sink current at node 2. The i.a.m. can then be written by inspection:

$$[Y]_I = \begin{array}{c} \\ 1 \\ 2 \\ 3 \\ 4 \end{array} \begin{array}{c} \begin{array}{cccc} 1 & 2 & 3 & 4 \end{array} \\ \begin{bmatrix} 0 & 0 & 0 & 0 \\ -Y_1 & Y_1+Y_2+Y_4 & -Y_4 & -Y_2 \\ 0 & -Y_3 & Y_3+Y_6 & -Y_6 \\ 0 & -Y_2-Y_4 & Y_4-Y_6 & Y_2+Y_6 \end{bmatrix} \end{array} \quad (17)$$

Y_1 no longer appears in row 1 (compared with equation 3) nor does Y_3 appear in row 2. Thus the quadrate property has disappeared for the seg and in this respect it behaves as if it were a new type of circuit element.

Choosing node 4 as the reference, the d.a.m. is:

$$[Y]_D = \begin{array}{c} \\ 1 \\ 2 \\ 3 \end{array} \begin{array}{c} \begin{array}{ccc} 1 & 2 & 3 \end{array} \\ \begin{bmatrix} 0 & 0 & 0 \\ -Y_1 & Y_1+Y_2+Y_4 & -Y_4 \\ 0 & -Y_3 & Y_3+Y_6 \end{bmatrix} \end{array} \quad (18)$$

Condense about node 2:

$$[Y] = \begin{array}{c} \\ 1 \\ 3 \end{array} \begin{array}{c} \begin{array}{cc} 1 & 3 \end{array} \\ \left[\begin{array}{c|c} 0 & 0 \\ \hline \dfrac{Y_1Y_3}{Y_1+Y_2+Y_4} & Y_3+Y_6-\dfrac{Y_3Y_3}{Y_1+Y_2+Y_4} \end{array}\right] \end{array} \quad (19)$$

Hence from equation 2:

$$A_v = \frac{v_0}{v_i} = \frac{Y_1Y_3}{Y_6(Y_1+Y_2+Y_4)+Y_3(Y_1+Y_2)} \quad (20)$$

Compared with equation 6. The disappearance of Y_1 from row 1 in equation 18 has made no difference to A_v, but the disappearances of Y_3 from elements subscripted 22 and 23 have indeed changed the expression.

Proceeding as before, and with reference to Fig.10 making the specific substitutions, the transfer function is

$$T_{(2)} = \frac{V_{i(s)}}{V_{0(s)}} = \frac{g_1g_3/C_4C_6}{s^2+sg_1/C_4+g_1g_3/C_4C_6} \quad (21)$$

Then
$$\omega_n = \sqrt{\frac{g_1g_3}{C_4C_6}} \quad (22)$$

$$B_p = \frac{g_1}{C_4} \quad (23)$$

$$Q_p = \sqrt{\frac{g_3}{g_1}}\sqrt{\frac{C_4}{C_6}}. \quad (24)$$

AN ILLUSTRATION

To keep things simple, stay with the same circuit so that the results in equations 9 to 11a can be compared with those in equations 22 to 24.

As the seg lends itself to variable control it is appropriate at first to discuss the two versions of the filter section in this context. Begin by referring to the orginal circuit (Fig.3) and assume that C_4 and C_6 cannot be variable, but G_1 and G_3 represent the conductances of two resistors (R_1 and R_3 say) which could be variable. To be practical, suppose that either R_1 or R_3 is variable, and if both are, that $R_1 = R_3$.

There are three parameters, ω_n, B_p and Q_p and it is desirable to vary two of these while the third remains fixed (ref.3): this gives three possible modes to look for. Equations 9 and 11 show that ω_n can be varied at constant Q-factor, provided that R_1 and R_3 are ganged then the law will be simply a reciprocal one. (For readers who like to visualise the root locus, the poles move along radial lines passing through the origin of the s-plane.) The graphical representation of the amplitude response variation is shown in Fig.11(a).

More careful scrutiny of equations 9, 10 and 11 reveals that neither of the other two desirable modes of control are practical if we are constrained to having only R_1 (G_1) or R_3 (G_3) as the variable elements.

Turning to the seg version of the network (equations 22, 23 and 24), direct comparison shows that this network also allows variable control of ω_n at constant Q_p if g_1 and g_3 are varied together and are equal. This is similar to the previous result as we might expect; there are, however, two advantages. First, the controlling law is now linear, and second the maximum value of Q is doubled (eqns. 24 and 11a). Put another way, for a given

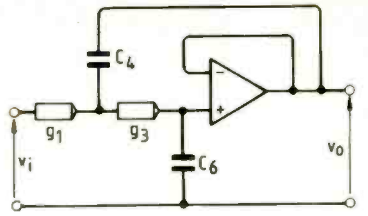

Fig.10. The circuit of Fig. 3 with a G_1 and G_3 replaced by segs g_1 and g_3. Current follows at the pointed ends of the segs, but not at the opposite ends.

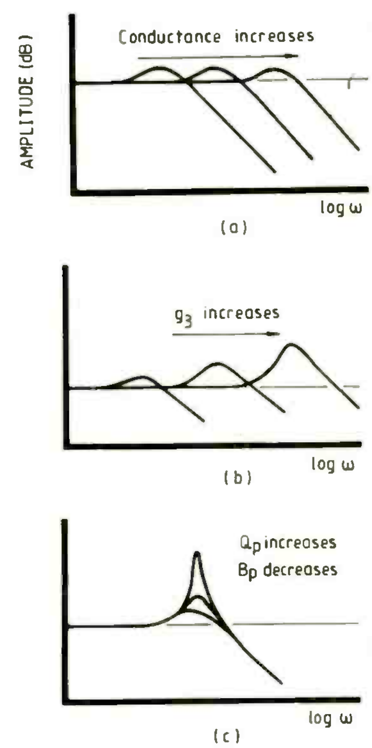

Fig.11. Graphical representations of the amplitude variations for the three desirable modes of control where two of the three parameters (ω_n, Q_p and B_p) vary and the third remains constant.

Q-factor the component value spreads (C_4:C_6 in this case) are four times less.

There is another desirable mode of control: ω_n can be varied at constant B_p. This can be achieved if g_3 alone is varied (and this implies that g_1 may be implemented by a fixed resistor, so only one o.t.a. is required). The law will be a square-root one – not ideal, but better than no control at all. The root locus is a vertical line parallel to the jω-axis on the s-plane, and the amplitude response variation is sketched in Fig.11(b).

The third desirable mode of control (B_p and Q_p vary at fixed ω_n) is not reasonably practical for either version of this particular network. For the record, the root locus would be circular, centred at the origin and the amplitude responses for this mode are shown in Fig.11(c).

There is yet another advantage of the seg implementation of the network if it is to be used in the fixed mode. The maximum value of Q-factor of the original version is limited by the squaring effect on component spreads (eqn 11a). But equation 24 indicates that, in principle at least, the component spreads need only be equal to the Q-factor. Using the earlier figures for illustration, a Q_p of 50 demanded a theoretical ratio (C_4:C_6) of 10,000 whereas in the seg version the same Q-factor requires a ratio of only 50 (for both C_4:C_6 and g_3:g_1). This is a very significant improvement and could be implemented using only one o.t.a. for seg g_3.

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Computers language and logic

formation required to reconfigure (program) a powerful machine.

To conclude with a positive example I include two routines that may be useful for graphics programmers. The routines calculate the pixels (x,y) that lie closest to a given straight line or circle.

The basic method is as follows: each time through the loop, increment x and conditionally increment y (for LINEGEN – y for CIRCGEN) thus moving 45° diagonally; or leave y unchanged, thus moving horizontally. The routines only apply in the octants indicated; other octants are catered for by the various symmetries.

The routines can be made very fast since they do not require any multiplication, division or floating point operations. Note that multiplication by two can be done with one left-shift or addition and by four can be done with two left-shifts or additions; left-shifts and additions are typically much faster than multiplications.

Notice how the descriptions are two-dimensional in nature and include very few words (no GOTO, FOR, WHILE, UNTIL etc.). In fact the only words are the names of the two routines, some comments and the name of another routine PUT. PIXEL (X,Y) which puts a dot at the appropriate location on a display.

I think Lao-Tzu put it best when he wrote in the Tao Teh Ching, "the myriad things are made without the slightest word."

Parameters

continued from page 141

For example, the z parameters are particularly useful when two networks are connected in series at their inputs and outputs, as shown in Fig.4.

Now,

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \text{and} \begin{bmatrix} v_1' \\ v_2' \end{bmatrix} = \begin{bmatrix} z_{11}' & z_{12}' \\ z_{21}' & z_{22}' \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \quad (4a)$$

Alternatively,

$$\begin{aligned} v_1 &= z_{11}i_1 + z_{12}i_2 \qquad & v_1' &= z_{11}'i_1 + z_{12}'i_2 \\ & & \text{and} & \qquad\qquad (4b) \\ v_2 &= z_{21}i_1 + z_{22}i_2 & v_2' &= z_{21}'i_1 + z_{22}'i_2 \end{aligned}$$

for the two respective black box networks. But $v_{in} = v_1 + v_1'$ and $v_{out} = v_2 + v_2'$, so adding the appropriate pairs of equations in (4b) gives,

$$\begin{aligned} v_{in} &= (z_{11}+z_{11}')i_1 + (z_{12}+z_{12}')i_2 \\ v_{out} &= (z_{21}+z_{21}')i_1 + (z_{22}+z_{22}')i_2 \end{aligned} \quad (5)$$

This shows that the overall z parameters of the series/series connected system are given by the sum of the separate z matrices,

$$\begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} + \begin{bmatrix} z_{11}' & z_{12}' \\ z_{21}' & z_{22}' \end{bmatrix} \quad (6)$$

There is a warning about series compound-connected networks. The current coming out of the bottom terminals of the upper network and going into the appropriate top terminals of the lower network, must be equal to the input current as shown in Fig.4. If this is not so, equations (5) or (6) do not apply.

The other parameters are more suitable for other types of interconnection. For example the h parameters are most convenient for a series – shunt-connected, two-port pair. The A, B, C, D parameters, given by,

$$\begin{aligned} v_1 &= Av_2 - Bi_2 \\ i_1 &= Cv_2 - Di_2 \end{aligned} \text{ or } \begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} i_1 \\ -i_2 \end{bmatrix} \quad (7)$$

are the best for cascaded stages, where the individual matrices are multiplied in order, hence the name 'chain parameters'.

The historical evolution of the chain parameters from transmission-line theory had the output current flowing in the opposite direction to the modern convention shown in Fig.2. This accounts for the minus sign on i_2. It is interesting to note that from the way A,B,C,D are defined, both dependent variables are input quantities and no equivalent circuits can be found to fit into the box in the way possible for the example shown in Fig.3.

Good textbooks give full details on deriving and using the parameters in their chapters on linear network analysis. Perhaps these will not look so forbidding to you from now on.

On the other hand, scattering parameters require some ability with transmission-line theory and a knowledge of reflection coefficients. s_{11}, s_{12}, s_{21} and s_{22} turn up in discussions about networks in the microwave part of the spectrum. But that is another story.

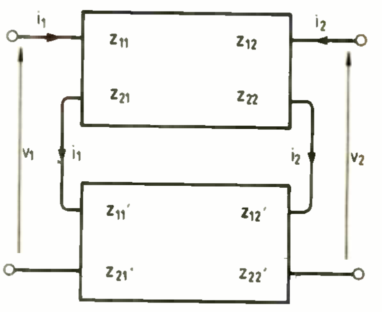

Fig.4. The convenience of z parameters becomes obvious when a series-series connected pair of networks is considered for overall performance. The "z" network could be an amplifier and the "z′" network a feedback circuit. All the other possibilities are handled by using the appropriate series or shunt parameters.

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Thyristor current pulser for high magnetic fields

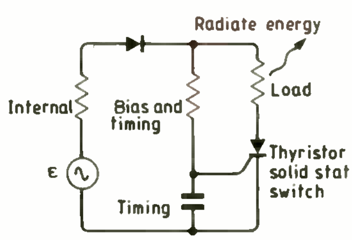
Transient magnetic fields of high flux density, produced by large current pulses from a low-current source, can exhibit some interesting phenomena – as well as problems of causality in interactions.

P.J. RATCLIFFE

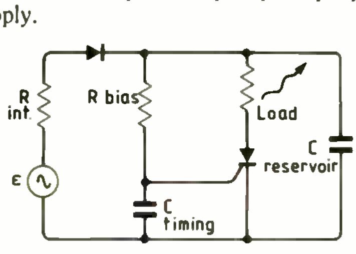
Large current pulses have use in producing intense magnetic fields for experimental use. I required a large current from a low-current source to produce a transient magnetic field of very high flux density.

An inductive load connected directly to a reservoir capacitor with a switch produces splendid visual and acoustic effects of the sparking fireworks as the switch contacts close (for strong coupling). This wastes a lot of energy in the switching element that could be passed through the load.

A thyristor used as a solid-state switch is much faster closing, ensuring more energy is useful dissipated in the load. For example, a thyristor could be used as a relaxation oscillator to drive the load from an intermittent or half-wave supply to ensure periodic quenching and resetting of the switch:



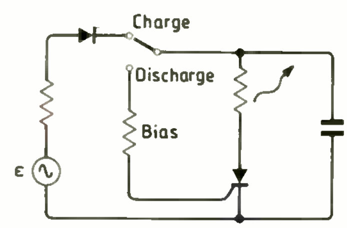
The maximum available loading current is limited by the internal resistance of the supply. (In the prototype this current limit was determined by the coupling efficiency of a mains isolating transformer composed of two bell transformers back-to-back as a step down and a step up transformer respectively). Current amplification can be obtained by using discontinuous or intermittent loading of a reservoir capacitor, 'pumped up' by the supply.



This simple circuit works but has the disadvantage that if the thyristor fires when the e.m.f. is on a positive cycle, or remains switched on discharging the reservoir whilst the e.m.f. goes through a positive cycle again, then the thyristor also shorts the supply through the heavy duty load. For a high internal resistance supply this is of no consequence if the heating effects are negligible or minimally non-destructive to the windings of the isolator transformer.

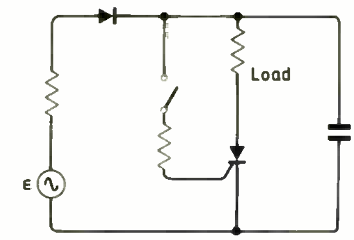
The effective internal resistance was so high in the prototype that the presence of the bias resistor caused too much drain through the gate input without the thyristor reaching its triggering threshold so that the voltage across the reservoir never rose high enough for spontaneous triggering.

The bias resistor can be removed (or loosely coupled) for manual triggering by using a mechanical switch (for strong coupling), and also a change-over to disconnect the circuit from the supply whilst the thyristor is firing.



Alternatively it is better to obtain the bias from the upper electrode (anode) of the thyristor so that when it fires and draws and draws current through the load the non-useful current through the bias resistor is removed.

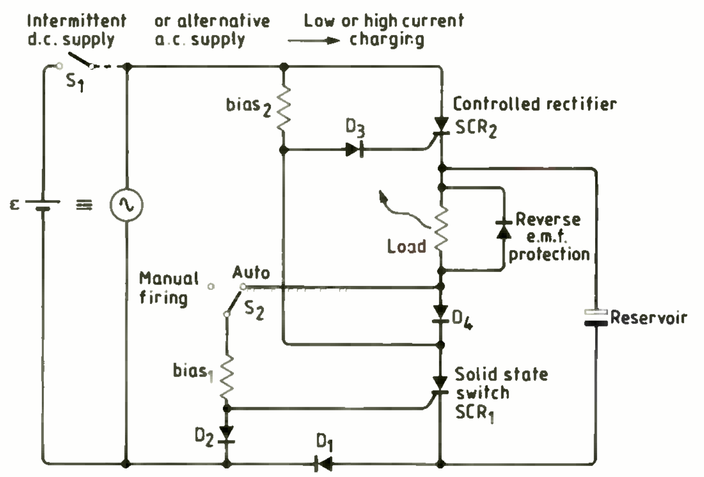
However this leaves the thyristor permanently connected across the supply if sequential mechanical switching is not used in the supply and bias lines. This is no good if we require to transfer this circuit to a low impedance supply, causing excessive heating of the load and thyristor if such heavy virtual short-circuit currents are main-

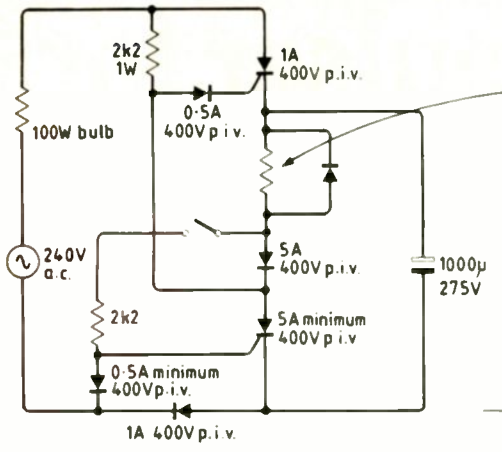


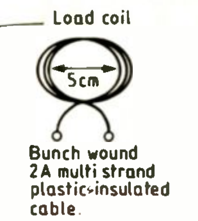
tained for longer than a transient pulse; too frequent re-cycling causes overheating as well.

A more extravagant but safe method of ensuring that the thyristor is never shorted across the supply when it discharges the reservoir is to use a second thyristor as a controlled rectifier that is switched off when the loading thyristor fires. The idea is to ensure that the loading thyristor itself cannot fire until the controlled rectifier has quenched on a negative-going cycle of the input, see circuit below.

The power rectifier in the mains supply has been translated around the circuit through the e.m.f., from the previous diagrams, to appear in the lower supply line as D_1. The gate bias for SCR_1 is shunted to 0V by D_2 when the e.m.f. is on its positive cycle along the top supply rail. So initially SCR_1 fires by its own bias current, charging the reservoir. The time for charging depends on the internal resistances of the source (use a 100W bulb as a current limiter, say) and the magnitude of the reservoir capacitance. It may be fully charged over one or more cycles of the e.m.f. – that is if an alternating e.m.f. is used to periodically quench SCR_2 instead of a d.c. supply and a manual switch S_1. When the reservoir is charged there is







enough e.m.f. to provide a trigger current for SCR_1. It used, the manual switch S_2 can be closed. Bias current will be diverted to 0V if the e.m.f. is on its positive half-cycle causing the small current rectifier D_2 to be forward biased.

When the e.m.f. goes negative the voltage-polarity switch D_2 goes open-circuit and bias current from the energy stored in the reservoir triggers the thyristor. Also, when SCR_1 fires it holds the bias to SCR_2 low so that as long as SCR_1 is on then the power rectifier SCR_2 cannot switch on when the e.m.f. goes on its positive half-cycles.

Diode D_3 provides reverse bias protection against breakdown for the cathode-gate of SCR_2. Diode D_4 in the loading circuit ensures that bias current to SCR_2 is not diverted to the reservoir when the supply is first connected. For then SCR_2 would not be able to fire and the rate of charging would depend on the trickle of current through this bias resistor. The diode causes some wastage of useful energy that could better be redirected or concentrated into the load but it is essential for this protective circuit, using a controlled rectifier to prevent the full loading current passing through SCR_2 over the long duration of the supply cycle.

With an inductive load, D_5 protects both s.c.rs from the high reverse e.m.f. induced in the coil when the current and flux fails after the peak of the pulse. Essential to the extent that Lenz's law of induction is valid for such short duration pulses in very low inductances.

As an abstract control system, fields can be induced in remote matter and the reaction back takes a finite time. By a suitable choice of time delay and field reversal we can induce negative feedback instability analogous to that in feedback amplifers, which becomes apparent when discrete-time element analysis is used. This could push matter apart and bring Newtonian mechanics into doubt. The consequences of this possibility are discussed later.

PRACTICAL CIRCUIT

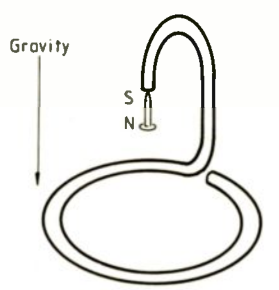
High current-handling components were used for SCR_1 and D_4 but since only short-duration high-current pulses are used, devices with a lower current handling capability could be used (sacrified), though you must be careful not to let the current pulses become too regular such that they overheat significantly.

USES OF HIGH-FLUX PULSED MAGNETIC FIELDS

The circuit was originally designed for experiment only. It was used to induce stresses in large metallic structures without any physical connection e.g. a metallic wall frame gave a loud 'clunk' when the field was pulsed near it, causing bending at the molecular or atomic scale.

The high field can also be used to magnetize all sorts of objects placed in the coil, for example small tinplate, heavy steel tools, and becaue it is a d.c. pulsed field the induced field can be successively cancelled by reversing the coil and firing pulses as the object is gradually moved away after each iteration. The quantitative description of such a sequential process uses the mathematics of discrete-element analysis, and we want the conditions that the net field accumulated or frozen into the test object converges to zero rapidly enough, to within an acceptable 'noise' level (or error from zero) in a reasonably finite time t. (That is, after a small number of iterations n of the magnetic field which need not be spaced at regular time intervals at all: n is more important than t as a descriptive variable of the interaction.)

A simple magnetic field detector can be made using a magnetized needle suspended at its point, using its own internal magnetizations coupling to a wire framework (made out of a wire coathanger).



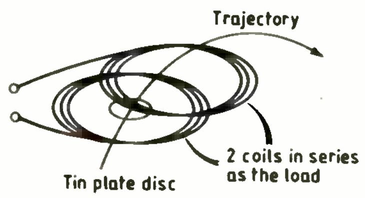
When a magnetized object is brought near the lower end of the magnetized pin, the pin deflects in a direction indicating the polarity, giving a measure of the strength of the applied magnetic field.

Another use of the pulsed magnetic field is as a moving ornament. Using a sheet metal punch, I cut about 50 small circular discs (3mm diameter) from a piece of tin plate and place them in a small covered glass jar standing in the coil. The shiny surfaces produce tinted kaleidoscopic patterns. When the field is pulsed the elements jump like a fountain to a height depending on the strength of the field, from a gentle tremor to an uprushing stream of projectiles, simulating magnetohydrostatic phenomena.

When the discs fall they settle into new patterns. Each pattern is uniquely different, and which could be projected onto a screen by reflecting light off the mirrored discs.

At high field strengths the discs fly up like projectiles spraying in a showr or fountain pattern. They could be trapped by an inverted glass fishbowl so that when they hit the sides they funnel back down into the coil for the next cycle, to make an ornamental fountain, of slow periodicity like the geyser 'old faithful'.

Another novelty is a magnetic game. A piece of tin plate inserted in the coil jumps about 60cm vertically into the air when the field is pulsed or fired: useful as a magnetic dice-shaker. By using two coils in series standing on top of one another, with slightly eccentric centres, the shape of the resultant field is distorted and the trajectory bent sideways. This is like ludo – trying to predict the trajectory of the tin plate disc or 'token'.



NEWTONIAN DOUBT

There is a more fundamental purpose in pulsed magnetic fields. The pulsed field brings into doubt the principle of Newtonian mechanics that action and reaction should be equal and opposite at every instant of an interaction. The magnetic field is produced by a pulsed current in the coil of very short duration. The information that this field exists takes a finite time to propagate, to produce magnetic effects on an object, and reciprocally for the information on that interaction to propagate back and react with the source, loading it. This is just the same problem as remote loading of a generator along a transmission line coupling. What matters is the interaction, not the material density of the intervening coupling medium.

The idea and physical demonstrability of pulsed phenomena means that Newtonian mechanics needs to be replaced by a more fundamental system of a truly casual mechanics, from which the Newtonian scheme can be derived as an asymptotic limit of interactions to-and-fro. That's if it does tend to a constant limit and that it doesn't suggest other phenomena that the Newtonian limit implicity precludes. For example, the legendary 'space drive' of science fiction fame. In a true system of causal mechanics interactions are mediated by field particles. With a suitable generator (in about 300 years time at the present rate of progress) we can induce resonances, not necessarily magnetic in character, to push matter around in space. If nobody dreams there will be no advance, and worse than that, we will never know whether it is truly possible or not.

High-precision composite op-amps

New technique using cascaded op-amps gives low vector error using simple feedback networks without component matching.

JOHN D YEWEN

Several recent articles have discussed amplifier configurations with reduced vector error for a given overall bandwidth (see references). The transfer functions of these systems have the first N terms of the numerator and denominator equal for an Nth-order system, for example a third-order system would be of the form

$$\frac{2s^2+2s+1}{s^3+2s^2+2s+1}$$

and in servo terms would have zero position, velocity and acceleration error, giving a finite error only when the input function has a non-zero third derivative.

It can also be seen from the form of the transfer function that for low frequencies, the error term varies as the cube of the frequency and can thus be made very small for operating frequencies relatively near the cut-off frequency where $s \approx 1$.

Previous articles have described non-inverting configurations and rely on matching resitor networks and, for the most part, matching amplifier gains.

The circuits described here are inverting circuits where the gain is set by only two components, which may be resistive or reactive, so that filters and integrators may be made. In addition there is a true virtual earth, so that signals may be summed if required.

The matching of the transfer function numerator and denominator terms is inherent in the circuit topology, and is independent of the precise values of either the resistors or the amplifier cut-off frequencies.

The generalised circuit schematic is shown in Fig.1 For an Nth order system there will be N separate forward paths between the amplifier virtual earth input and the output.

The ω terms are cut-off frequencies of the op-amps in rad/s, and the passive interstage attenuators are used to shape the closed-loop transfer function into a stable and useful form, as shown in the worked third-order example following.

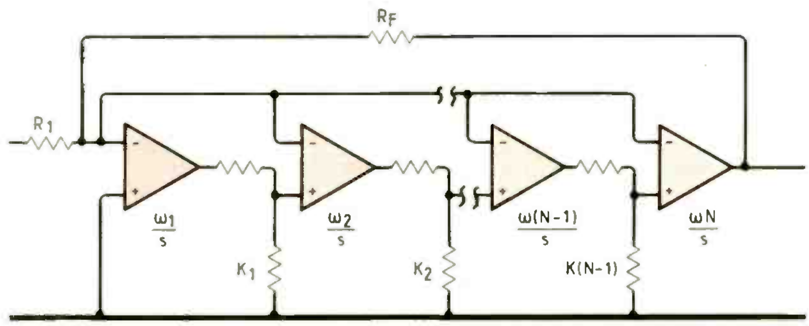


Fig.1. Nth-order circuit schematic.

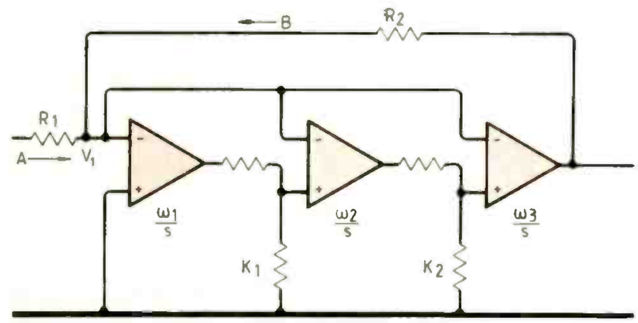


Fig.2. Third-order system.

SUMMARY

The use of cascaded op-amps in a new circuit configuration enables precision inverting amplifier circuits to be constructed using standard feedback networks. The completed circuits have a very low phase and amplitude vector error, and, unlike previously published circuits, do not require elaborate matched feedback networks to maintain high accuracy, are easy to use, and have lower output impedance. In addition, they are also suitable for use in summing, integrating and filtering applications.

TRANSFER FUNCTION

Referring to Fig.2 the open-loop transfer function is

$$\frac{V_{out}}{V_{in}}=\frac{\omega_3}{s}+\frac{K_2\omega_2\omega_3}{s^2}+\frac{K_1K_2\omega_1\omega_2\omega_3}{s^3}$$

$$=\frac{s^2\omega_3+sK_2\omega_2\omega_3+K_1K_2\omega_1\omega_2\omega_3}{s^3}$$

So putting in the input and feedback path gains A and B, multiplying top and bottom by s^3, and using the standard servo closed-loop formula

$$\frac{G(s)}{1+H(s)G(s)}$$

we get $V_{out}/V_{in}=$

$$\frac{A}{B}\cdot\frac{s^2\omega^3+sK_2\omega_2\omega_3+K_1K_2\omega_1\omega_2\omega_3}{s^3/B+s^2\omega^3+sK_2\omega_2\omega_3+K_1K_2\omega_1\omega_2\omega_3}. \quad (1)$$

The last three terms match identically in the numerator and denominator as a direct consequence of the term G(s) in the numerator and denominator of the servo closed-loop formula above, and the matching is totally independent of the actual values K, ω, A and B.

To produce a stable system, the transfer function denominator polynomial must meet the Routh-Hurwitz stability criterion, and in practice must exceed this by a safe margin.

Suitable normalized coefficients could be the binomial series 1,1; 1,2,1; 1,3,3,1; etc. giving coincident negative real poles. A somewhat better approach would be to use the standard Butterworth filter denominator coefficients, which would give better frequency domain performance, at the expense of poorer settling time and transient response.

WORKED EXAMPLE

Taking the third-order close-loop transfer function (eqn 1). Choose a unity-gain inverter as an example, giving B = ½. Chose third-order Butterworth denominator coefficients 1,2,2,1). Assume that individual amplifier frequency responses are the same – this is not essential but simplifies the example – so $\omega_1 = \omega_2 = \omega_3 = \omega$.

Because we want a normalized form, multiply through by B giving unity for our first denominator term:

Now re-normalize to $\omega_0 = \omega/4$ giving $\omega = 4\omega_0$ which gives the second term equal to 2, as required:

$$s^3 + 2\omega_0 s^2 + 8K_2\omega_0^2 s + 32K_1K_2\omega_0^3,$$

from which k_2 = ¼ and k_1 = ⅛ to give the other two terms equal to 2 and 1 respectively.

Replacing these values in the original closed-loop transfer function (1) and putting B = ½. A = ½ gives

$$s^3+\tfrac{1}{2}\omega s^2 + \tfrac{1}{2}K_2\omega^2 s + \tfrac{1}{2}K_1K_2\omega^3.$$

$$\frac{s^2\omega+\frac{1}{4}s\omega^2+\frac{1}{32}\omega^3}{2s^3+s^2\omega+\frac{1}{4}s\omega^2+\frac{1}{32}\omega^3}.$$

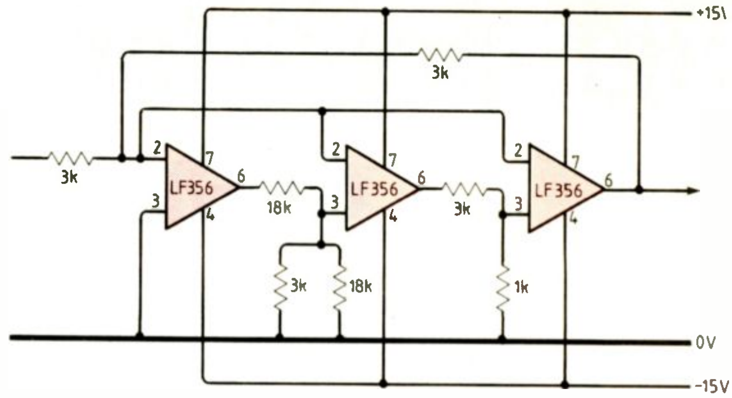


Fig.3. Completed circuit for worked example.

At low frequencies the s^2 and s terms are negligible compared with the constant term, and the error is represented by the s^3 term, where the denominator differs from the numerator. So the low frequency error is approximately.

$$2s^3/(\tfrac{1}{32})\omega^3=(4s/\omega)^3.$$

So using LF356 amplifiers ($\omega \approx$ 4MHz) for example at a frequency of 100kHz in the circuit we get

$$(4\times 100\text{kHz}/4\text{MHz})^3=1/1000$$

i.e. one part per thousand error.

The circuits can be adapted to work at any closed-loop gain; use a variety of amplifiers, not necessarily all identical; have their transfer functions tailored to suit specific applications; and be made of any required order to meet a given specification.

In addition, as large amounts of negative feedback are being applied they have lower closed-loop output impedances than would otherwise be the case.

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Reducing amplifier distortion, A.M. Sandman *Wireless World* October 1974 p.367.

Analgoue Applications Seminar Notes, Precision Monolithics Inc. September 1986.

Active op-amp compensation, A.M. Soliman, *Electronics & Wireless World* November 1986, p.49,50.

John Yewen is an analogue design engineer with Automatic Systems Laboratories of Milton Keynes. He has been involved with the design of standards-quality resistance bridges for the last 12 years. He is a keen amateur astronomer and a fellow of the Royal Astronomical Society.

BOOKS

Newnes Electronics Pocket Book, 5th edition, edited by E.A. Parr. Heinemann, 315 pages 95×196mm, hard cover, £8.95. Useful and very portable reference book covering all aspects of the subject from fundamental physics to fault-finding. This edition includes numerous revisions, including new material on op-amp applications and design of digital circuits. Emphasis is on communications and computing, with an entire new chapter on the latter. Not to be confused with the same publisher's Radio and Electronic Engineer's Pocket Book (E&WW, July 1986, p.21), which duplicates very little of the same territory.

BBC Annual Report and Handbook 1987. BBC Publications, 291 pages, soft cover, £8. Review of the BBC's activities in 1986 with many colour photographs of the year's radio and television programme highlights. Also included is a great deal of reference material – such as, for example, where to apply for a job. The editors devote 37 pages to the accounts and only about half that to engineering matters, which no doubt shows the way things are these days.

British Television: the formative years by R.W. Burns. IEE History of Technology series 7, Peter Peregrinus in association with the Science Museum, London; 488 pages, hard cover, £38.40. Detailed academic history of the medium from Baird's early experiments to the establishment of the Marconi-EMI electronic system and to the suspension of the service at the outbreak of war in 1939, with many photographs and drawings. Absorbing reading for Baird-watchers, since inevitably much of the content deals with the Scottish inventor's endless squabbles with the General Post Office and the BBC; Professor Burns has much more patience with him than others have shown. No doubt it was clear to many that the man was caught in an evolutionary blind alley and that his spinning discs offered no possibility of a service with real entertainment value; but it was hardly dignified of P.P. Eckersley, the BBC's chief engineer to prejudice his Board against the system before they had seen it working. Inevitably, the reader is left filled with admiration for Shoenberg, Blumlein and the rest of the EMI team, who conjured up what is essentially the television standard we have today in the space of a few months.

Baird, incidentally, showed great animosity towards his rivals, which he saw as an American-inspired (EMI had access to RCA patents) campaign to undermine his all-British invention. A parable for our time?

DOUBLE-NOTCH FILTERING

An unfortunate error in the January part of this article made nonsense of Mr Sokol's argument. The affected part was the first equation on page 47 and the correct version is

$$H(s)=\frac{s^2-\omega^2}{s^2+(\omega/Q)s+\omega^2}$$

Our apologies to readers and to Mr Sokol.

EARTHQUAKE

Laboratories monitoring earthquake tremors, as well as radio enthusiasts within a few hundred miles of regions prone to earthquakes, may find a radio technique backs up ether theory.

H. ASPDEN

Electromagnetic waves propagate relative to a frame of reference which, according to the Theory of Relativity, is set by each and every individual observer. Yet classical theory and, indeed intuition suggest that this frame is physically determined by something in our local environment providing a shared and common local frame of reference. Today there is an increasing willingness to recognize that the vacuum itself is not a void, but rather has a structured property[1]. It may be seen an elusive fluid having a disposition to crystallize, adopting the general motion of coextensive matter, so far as its crystalline content is concerned, but dissolving at boundaries.

An ether of this form, activated by a common sychronous motion of the lattice, can explain how energy propagation must occur in quanta proportional to frequency. It is even possible to deduce the dimensionless constant incorporating the Planck constant, obtaining a value correct to well within one part per million. This is provided one can undo, as it were, the good work of the Reverend Samuel Earnshaw, who a century and a half ago proved mathematically that the ether could not be a stable electric stucture[2].

If then we are open to think of the Earth itself setting our local electromagnetic frame of reference and having an influence extending through our atmosphere, we can expect geophysical adjustments of body Earth to affect the em frame. Earthquakes might cause ripples in this frame of reference. Also, since electric fields are stored in the vacuum by physical displacement of something electrical (the structure mentioned above) from its natural equilibrium position, the sudden release of strains in rocks can signify the setting up of oscillations which spread through our em reference frame.

It follows that radio reception is likely to be affected during, and even prior to, earthquake events. It is not profitable to speculate about the true nature of the ether, bearing in mind that the mainstream physics community prefers to assume that the ether has no real role to play. But it is profitable to note that, should the ether really exist, it is very likely that radio waves will suffer distortion at time when earthquakes are prevalent. It seems obvious that if the em reference frame is set in oscillation then the effect will be that of the speed of propagation varying about its usual value in the affected regions. As wave energy in transit is conserved, this means that the amplitude of a signal will flutter and, perhaps more to the point, v.h.f. f.m. reception will be affected because the frequency will also be modulated by the ether disturbance.

This proposition that there is an ether willing to reveal itself when earthquakes occur can be tested by monitoring the noise properties of radio waves, and in particular by comparing the noise content of f.m. and a.m. signal propagation over the same test distance. The task is one of searching for a correlation between earthquake tremors and enhancement of the f.m. noise a.m. noise ratio.

This is not wild speculation. Ten years ago there was a serious earthquake in north east Italy. A radio enthusiast in Switzerland[3] reported that ten minutes before the tremor reached his house he happened to be listening to a BBC a.m. broadcast using his own small v.h.f. f.m. relay or repeater. He describes how he suddenly became aware of a high pitched, rustling noise in the speaker sounding like scrubbing a fine emery paper on glass. Checks indicated that the scratching noises were on the whole v.h.f. range, but that the a.m. broadcast kept completely clear and was immune from the disturbance. Then the tremor struck and two or three minutes later the whole system reverted to normal.

Here then is at least a clue to a possible means of predicting earthquakes, based on the sensitive detection of minor tremors by apparatus operating in a.m. and f.m. modes so as to distinguish, by their collective action, between background noise and earthquake-related noise.

However, the belief in the Theory of Relativity is so strong that few will wish to accept the underlying explanation for the anomalous reception just discussed. The ether is not so easily brought back to life, even if its revival might be a by-product of useful research aimed at predicting earthquakes, based on an accidental discovery in Switzerland ten years ago.

Interested readers should have little difficulty devising an apparatus which could continuously monitor a.m. and f.m. transmission and reception and record unusual peaks in the f.m. noise ratio. If these data checked with data on earth tremors then that would surely speak in favour of a real ether.

A BOOST TO ETHER THEORY?

Readers may recall Dr Aspden's earlier article "The ether – an assessment" in *Wireless World*, October 1982, if not his book Modern Aether Science. Though adherence to ether belief may seem futile, Dr Aspden says he can now point to its predictive power.

There is currently no accepted explanation for the proton-electron mass ratio, but amongst Aspden's many scientific papers is "Calculation of the proton mass in a lattice model of the ether". By a major technological advance, the proton-electron mass ratio was recently measured to within a precision of 41 parts per billion, a severe test for the value given by ether theory. The authors of the experiment have acknowledged in their report that the value given by Dr Aspden's theory was "remarkably close to the experimentally measured value (i.e. within two standard deviations)". They also said that this was "even more curious" taking into account that the theory was published several years before direct precision measurement of this ratio had begun.

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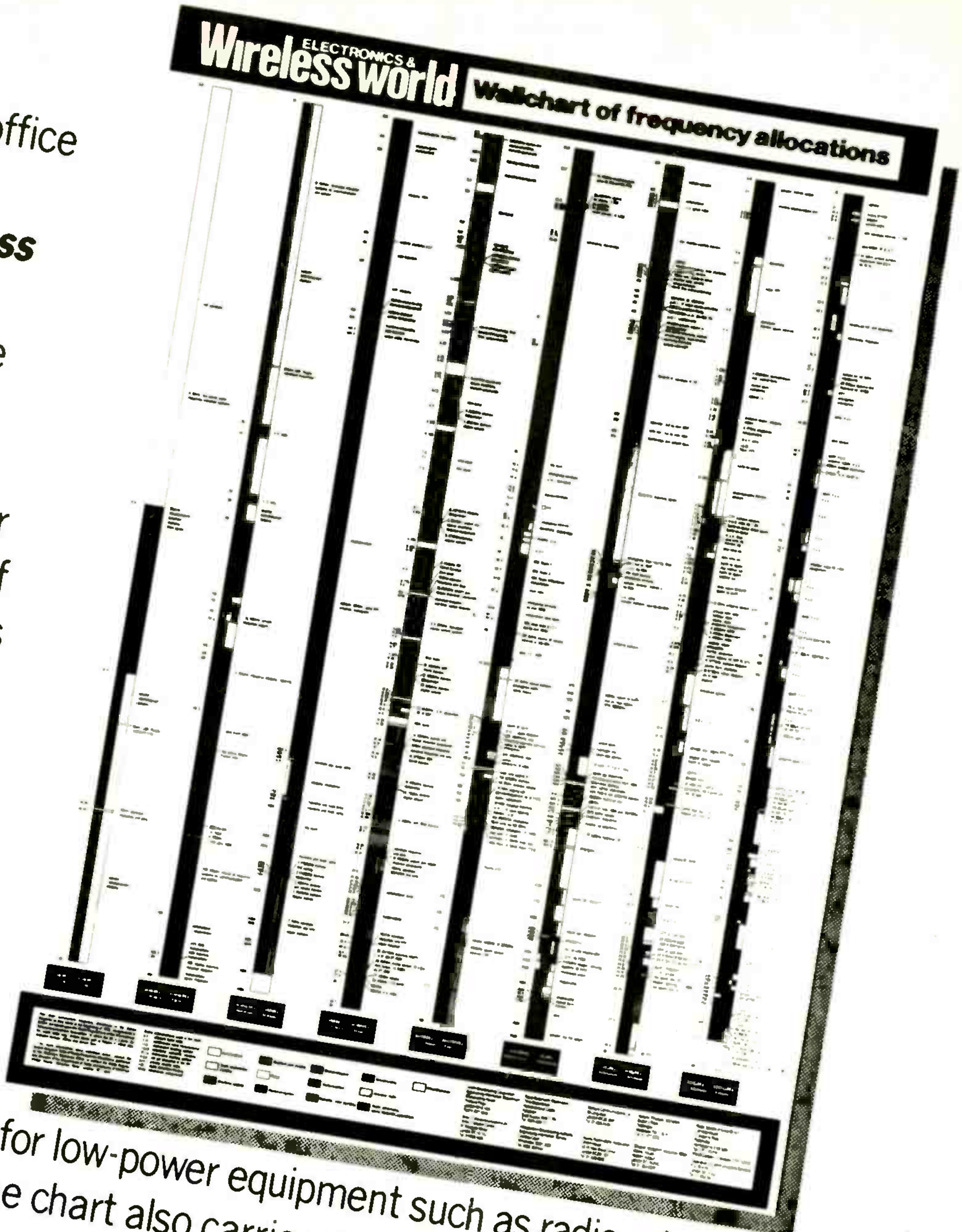
V.F. Weisskopf, *Physics Today*, vol. 34-12, 1981 p.69.
2. H. Aspden, *Nature*, vol. 319 1986 p.8.
3. M. Markert, *New Scientist*, vol. 70 1976 p.488.

Harold Aspden, B.Sc., Ph.D., F.I.E.E., F.I.Mech.E, M.Inst.P, is a visiting senior research fellow at Southampton University. Most of his working career has been spent on patents work, mainly with IBM as European Director of Patents, from which he took early retirement to further his scientific interests.

Brighten up your office or lab with a copy of ***Electronics and Wireless World's*** wallchart of frequency allocations. The chart covers frequencies from 3kHz to 300GHz in eight sections, with colour codes to show the uses of each band. Detailed notes mark areas of special interest to the scientist and engineer — such as standard frequency and time signals, radio-astronomy bands, mobile radio, public radiophones and pagers, and assignments for low-power equipment such as radio-microphones and anti-theft devices. The chart also carries a useful list of addresses.



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WORKFILE

STEPHEN HORN

The British Broadcasting Corporation is finding it so hard to recruit suitably qualified engineering graduates that it is running conversion courses for those who took the wrong course the first time around.

When it comes to radio-frequency (r.f.) design engineers it certainly begins to look like a seller's market. John Prodger from Executive Recruitment Services said that, during his 13 years in the engineering recruitment business, he's never known demand to fall off. "I've been banging my head against a brick wall not knowing where my next r.f. design engineer is coming from," he said.

Marconi Personnel Office Les Thompson would agree. "Every major employer who is looking for r.f. engineers has a problem because there simply aren't enough on the market," he said. BBC Engineering Recruitment Officer Bob Neal agrees: "good people are hard to come by." However Neal said the secret was in a good recruitment programme. The BBC actively recruits young people with both 'A' levels and degrees and has, according to Neal, some success. "We obviously get them – we're still in business," said Neal.

Salary levels offered reflect the seniority of the job and the experience of the candidate but can, according to Prodger, be equated with those offered to other engineering disciplines. A graduate fresh out of university can expect around £8,000 while an engineer with about five years experience will be looking for a project leader's job, and a pay package of some £19,000. Prodger said that r.f. engineer salaries can now be roughly equated with those enjoyed by computer software engineers.

Most employers are looking for engineering graduates. Thompson said Marconi sponsors a number of graduates through university and is therefore particularly keen to monitor their progress. However, with today's labour market as it is, this is not a hard and fast rule. Thompson said Marconi may start with the HND level and indeed the BBC will take on engineers with good 'A' levels.

Under their graduate conversion scheme, the BBC has recently received some 3,000 applications for 30 course placements. People from all disciplines have applied for the course, even sociology graduates. Neal said the BBC were happy with the scheme and are repeating it again this year. So far, according to Neal, they have provided some 2,000 places for this year's course.

After completing the conversion course, engineers then follow the normal BBC engineering course for school leavers with 'A' levels, according to Neal. These people then go into operations. On the question of experience, the BBC seldom hires people after they have left university. The corporation has a policy of promoting from within and so could only offer an experienced graduate a trainee's wage. With the labour market as it is, Neal said he would be surprised if engineers turned down a higher salary for a trainee's pay packet.

Prodger said an M.Sc. – especially in a specialization such as microwaves – is valuable to an employer. Indeed, some universities are now running M.Sc. courses aimed at supplying the demand for r.f. engineers. Among those institutions are Portsmouth, University College London, Bradford, and Leeds Universities. Prodger went on to say that those engineers who go on to take a Ph.D. qualification soon become highly specialized and more often than not would opt for a research environment rather than a commercial operation.

Indeed, a new scheme has just been launched to combat the dearth of engineers and technicians experienced in radio-frequency engineering. The Mobile Radio User's Association (MRUA) have joined with the Association of Marine Electronics and Radio College (AMERC) to offer courses relevant to the land-mobile radio industry. AMERC currently runs a three year course for 'O' level standard candidates leading to a

National Diploma and HNC qualifications in electronic and communications engineering.

The new courses – on offer from September 1987 – are concerned with the land-mobile radio industry and will fit into existing modular schemes which contain fundamental core information, such as electrical and electronic principles, mathematics and radiocommunications.

The course run by AMERC will seek to give students an understanding of the principle characteristics and requirements of electronic circuits operating at both v.h.f. and u.h.f. They will also seek to help the student develop skills in the use of commercial test equipment, and to enable the student to acquire practical experience of systems and techniques at these frequencies.

The new modules will include the following topics considered by many to be essential knowledge for engineers seeking employment within the mobile radio industry:

- communication principles relating to land-mobile radio;
- v.h.f. and u.h.f. receiver and transmitter design considerations;
- spectrum efficiency and management;
- principles of site management;
- implementation of cellular and trunked radio systems;
- other specialized communication topics such as battery design.

AMERC core courses have been running for a number of years and are accredited by the Business and Technician Education Council. AMERC chairman Bill Cotton said he hoped B/TEC would accredit the new modules by Easter.

The amount of experience required by employers clearly varies with the seniority of the post. Simon Hall from RNW Recruitment said his company was looking for graduates in their mid-20's with four to five years experience. Two to three years experience tends to be the norm but, given the tightness of the market, employers have to be flexible. "Even a good graduate with a final year university project can command a series of interviews," Prodger explained.

An engineering graduate with a few years post-graduate experience should certainly be able to keep busy. The question asked by many is whether or not to gain a professional qualification, such as membership of the Institute of Electrical Engineers. To become a MIEE a prospective candidate can follow two paths. He could take an accredited university degree and then follow a carefully monitored programme of training. This will include training at a recognized place of work as well as filling in a detailed log-book. Those who don't, according to IEE training Officer William Baker, need to submit a curriculum vitae of some 1,000 words.

However, Baker maintains professional membership is an investment in the future. For example, the IEE is a member of the Federation of European Engineering Institutions. Many overseas contacts will only be awarded to companies, Baker said, whose primary employees are institute members.

While there seems to be universal demand for r.f. engineers, it is Ministry of Defence contractors who seem to be recruiting the hardest, according to Hall. Hall said these contractors have both money and the lure of large projects to entice graduate engineers, although the large amount of paper work can put off some engineers. There is increasing demand from commercial communication organizations and radio paging systems for r.f. engineers.

Hall said that most career engineers, on leaving university, begin to gain specialized experience through working on a large project. These people will work as design and prototype engineers and will gain valuable r.f. experience. Their career path depends entirely on the individual, he explained, with many achieving project leadership after five years experience gained in a broad spectrum of specialities. Not surprisingly, Hall bemoaned the fact that there are not enough of this calibre engineer on the market.

Stephen Horn is Employment Editor, *Electronics Weekly*

APPOINTMENTS

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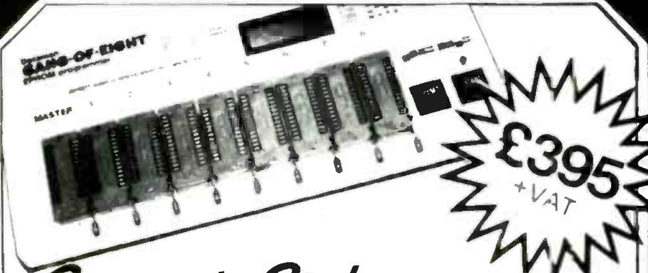

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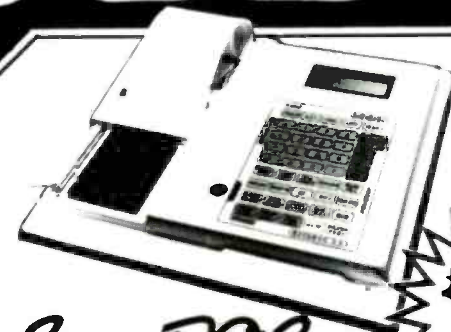

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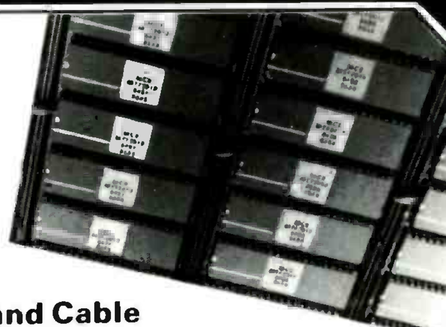

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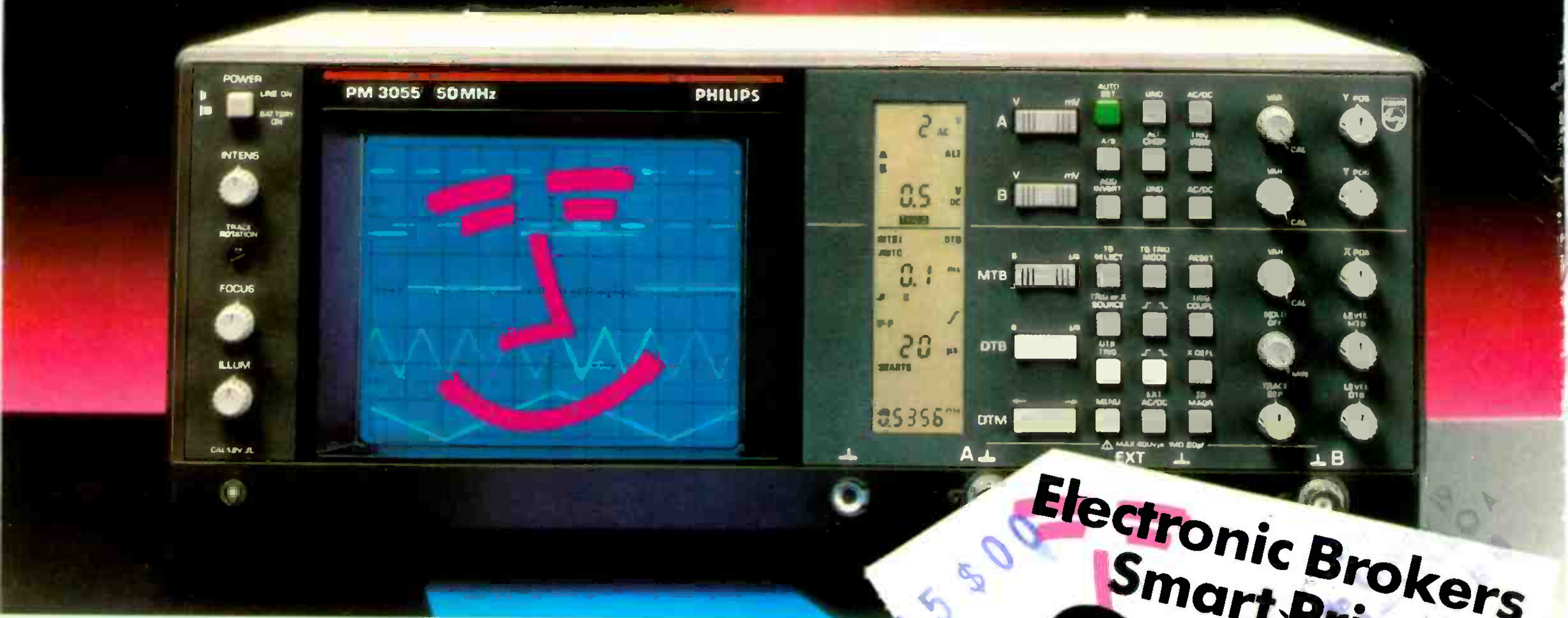

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