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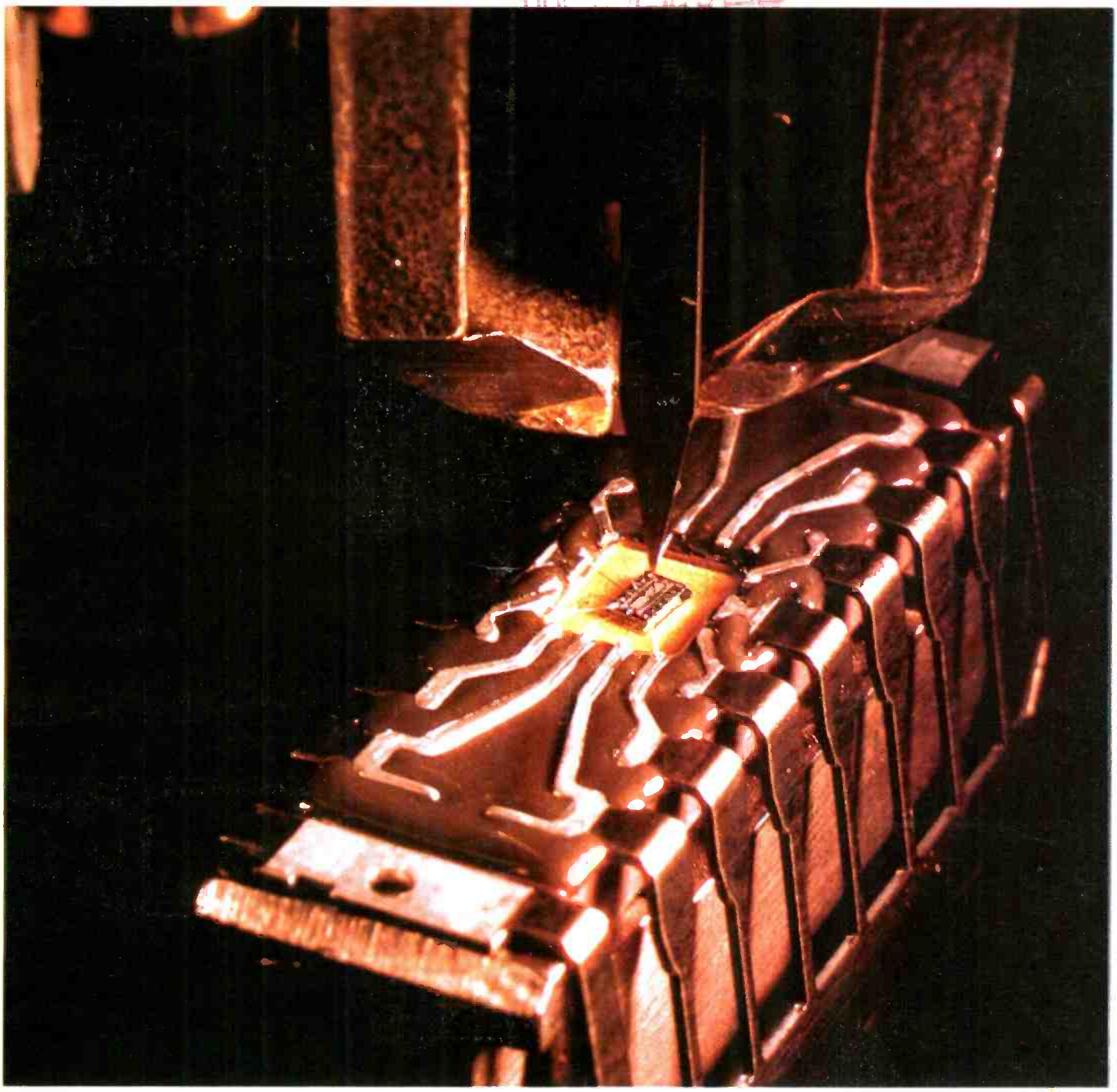

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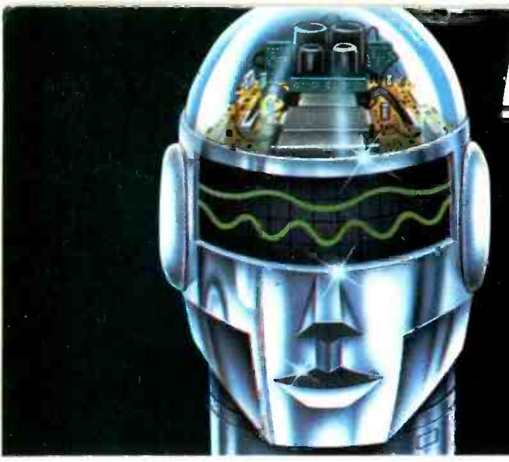

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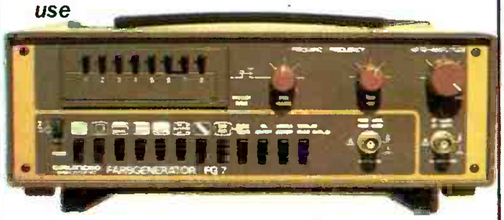

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August 1986
Volume 92
Number 1606

FEATURES

REGULARS

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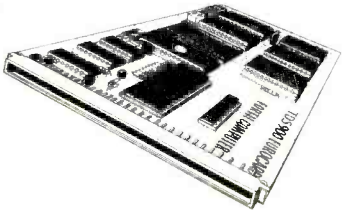

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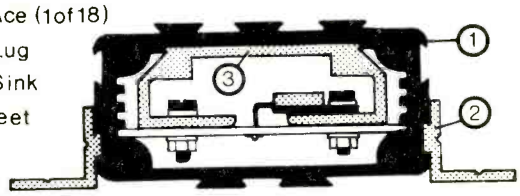

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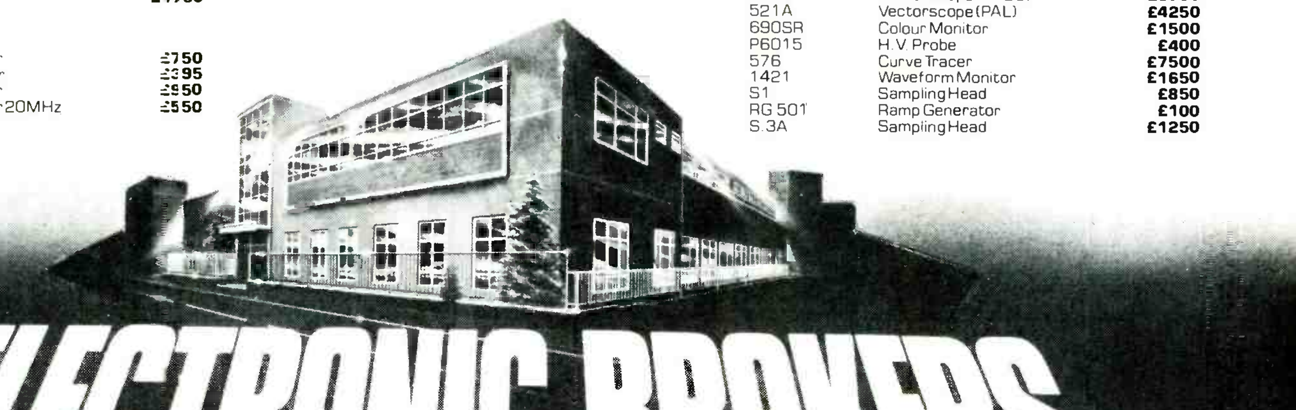

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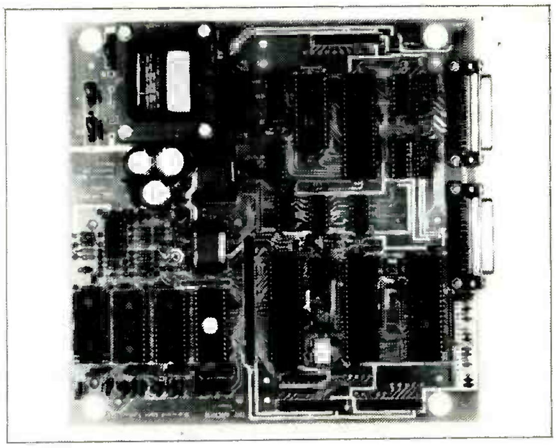

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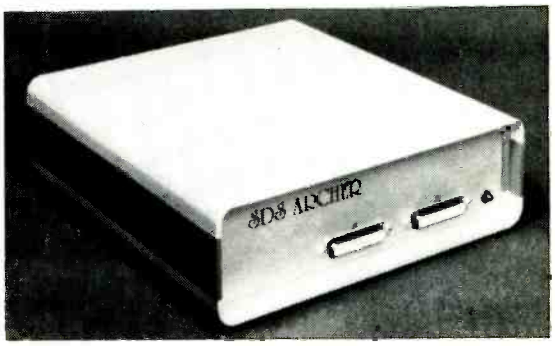

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- BC137 0.22
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- BC157 0.12
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- BC159 0.12
- BC167 0.10
- BC170 0.09
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- BC172 0.09
- BC173 0.09
- BC177 0.15
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- BC179 0.15
- BC182 0.11
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- BC184 0.11
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- BC213 0.11
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- BC238 0.09
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- M8081 9.82
- M8082 9.69
- M8083 10.25
- M8091 10.43
- M8096 6.80
- M8097 8.10
- M8098 8.15
- M8099 8.00
- M8100 10.30
- M8136 11.75
- M8137 12.25
- M8140 6.00
- M8141 6.50
- M8142 8.75
- M8144 7.50
- M8149 6.50
- M8161 9.35
- M8162 11.75
- M8163 8.25
- M8190 5.00
- M8195 10.85
- M8196 7.50
- M8204 7.05
- M8212 11.37
- M8223 6.00
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- PCF86 2.50
- PCF87 2.00
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- PCF201 3.25
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- PCF805 1.70
- PCF806 1.70
- PCF808 1.70
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- PCL84 2.00
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- PL509 6.00
- PL519 6.00
- PL801 1.50
- PL802 6.00
- PY33 2.50
- PY81 1.50
- PY82 1.50
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- PY88 2.00
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- ZM1041 16.66
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- 2J55 245.00
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- 2J70B 336.00
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- 3A5 3.00
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- 3CX100A 47.00
- 3E29 45.00
- 3S4 2.00
- 3V4 1.75
- 4-65A 60.00
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- 6BW7 1.50
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- 6CL6 3.75
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- 6F23 1.60
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- 6H3N 2.75
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- 6J6 8.93
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- 6JE6 7.50
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- 6SQ7 3.40
- 6SR7 4.00
- 6SS7 2.75
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- 6U8A 2.25
- 6V6GT 4.25
- 6X4 3.00
- 6X5GT 1.75
- 7B7 2.50
- 7C5 4.00
- 7C6 2.50
- 7H7 4.00
- 7R7 4.25
- 7S7 3.50
- 7Y4 2.25
- 7Z4 2.00
- 12AH8 5.00
- 12A16 1.50
- 12AT7 1.50
- 12AU6 2.50
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- 12AV6 2.50
- 12AW7 3.50
- 12AX7 1.75
- 12AY7A 4.00
- 12B4A 3.50
- 12BA6 2.50
- 12BE6 2.50
- 12BH7 2.75
- 12BY7 3.00
- 13E1 170.00
- 12E1 28.00
- 12E13 65.00
- 12E1 20.00
- 13E1 170.00
- 19H5 47.50
- 24B9 67.25
- 30C15 2.00
- 30C17 2.00
- 30C18 2.00
- 30F5 1.38
- 30FL1/2 1.38
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- 30L1 1.50
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- 6058 12.34
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- 6064 10.25
- 6067 11.75
- 6072 6.00
- 6080 14.00
- 6097A 235.00
- 6097B 200.00
- 6146A 12.00
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- 6159B 19.00
- 6189 9.50
- 6201 11.40
- 6442 20.00
- 6550 5.00
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- 7027A 8.00
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- 7609 56.00
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- 7895 12.00
- 8068 16.50
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- 8417 6.00
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- 18045 10.49
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- I octal 0.55
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- DG7-31 58.07
- DG7-32 58.07
- DG7-36 65.00
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- DH7-11 113.12
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- 7401 0.36
- 7402 0.36
- 7403 0.36
- 7404 0.42
- 7405 0.42
- 7406 0.48
- 7407 0.55
- 7408 0.36
- 7409 0.36
- 7410 0.36
- 7411 0.40
- 7412 0.42
- 7413 0.36
- 7416 0.48
- 7417 0.48
- 7420 0.48
- 7422 0.36
- 7423 0.36
- 7425 0.36
- 7427 0.36
- 7428 0.36
- 7430 0.35
- 7432 0.36
- 7433 0.55
- 7437 0.36
- 7438 0.36
- 7439 0.36
- 7440 0.36
- 7441 0.48
- 7442 1.25
- 7450 0.30
- 7451 0.30
- 7453 0.30
- 7454 0.30
- 7460 0.30
- 7470 0.48
- 7472 0.30
- 7473 0.48
- 7474 0.36
- 7475 0.65
- 7476 0.48
- 7480 0.32
- 7483 0.48
- 7484 0.72
- 7486 0.54
- 7490 0.72
- 7491 0.36
- 7492 0.54
- 7493 0.54
- 7494 0.78
- 7495 0.65
- 7496 0.60
- 7497 3.84
- 74100 0.84
- 74107 0.36
- 74109 0.54
- 74110 0.48
- 74111 0.51
- 74116 1.50
- 74118 1.20
- 74119 1.50
- 74120 0.75
- 74121 0.54
- 74122 0.70
- 74123 0.60
- 74125 0.60
- 74126 0.54
- 74128 0.55
- 74136 0.70
- 74141 0.36
- 74143 1.30
- 74145 0.72
- 74147 1.50
- 74148 1.40
- 74150 1.60
- 74151 0.36
- 74154 1.40
- 74155 0.60
- 74156 0.48
- 74159 1.75
- 74170 1.20
- 74172 4.00
- 74173 0.72
- 74174 0.60
- 74175 1.00
- 74176 1.00
- 74180 1.48
- 74190 1.20
- 74191 1.20
- 74192 1.10
- 74193 0.60
- 74194 1.10
- 74195 0.72
- 74196 1.00
- 74197 1.00
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Opto-pioneers rewarded

Eleven scientists who have made 'outstanding contributions to the science of opto-electronics' have been awarded cash prizes by the Rank Prize Funds.

Optical discs

Three of them; Dr Pieter Kramer, Gijs Bouwhuis, and Dr Klaas Compaan, were given the prize for their work on optical-digital discs at Philips Research which led to LaserVision and the Compact Disc. They devised the complete opto-electronic system and electronic techniques to enable the recording of images and/or sound to be played without contact using laser light.

The prototype for LaserVision was first demonstrated as early as 1972, and, after considerable research and product development was launched in the USA in 1978. The rise of the video cassette recorder limited the appeal of the optical disc, which is now being revived by its use in interactive video systems, such as the Domesday project. The compact disc, launched three years ago, has had no such restraints and has taken off dramatically. Interactive use of these discs is also under development and they have found uses in data storage for computers. The Philips team are researching ways of producing an optical disc that can be recorded on as well as played back by the user. They are studying materials for eraseable discs that can be reused.

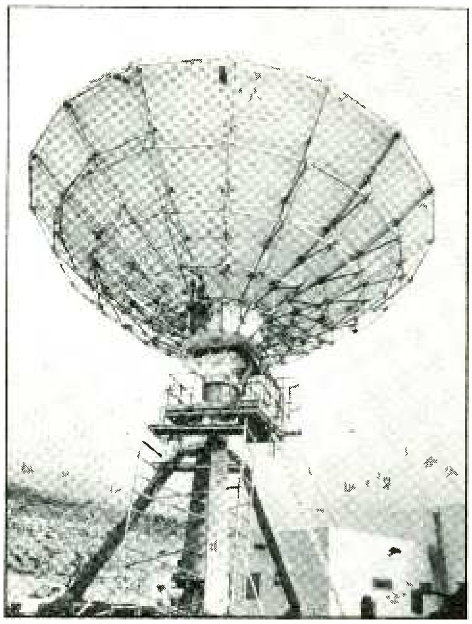
Liquid-crystal light valve

Four scientists from the Hughes Corporation in the US; Dr Jan Grinberg, Dr Williams Bleha, Dr Alex Jacobson and Terry Beard, were involved in the development of a low-cost, large-area projection displays of tv. At the heart of the system is the liquid-crystal light valve (l.c.l.v.) which is an optical-to-optical image transducer capable of accepting a low-intensity light image and converting it into a bright output image with light from another source. The device works by reflecting the light source, so the input and output light beams are completely separate and non-interfering. When used for large screen displays, the light valve accepts an image from a c.r.t. and transmits it by modulating the beam of a xenon-arc lamp. Thus the light-valve projector acts as a 'real-time slide projector' to give a very bright and greatly enlarged reproduction of the tube image. The system has been used in sports fields and at pop concerts, for conferences and in flight simulators.

Hot spotters

Two researchers from the Royal Signals and Radar Establishment; Dr Ernest Putley and Rex Watton, and two others; William Wreathall and Dr Alan Goss, from the English Electric Valve Co. received their prize for their work on thermal-imaging cameras. Infrared tv camera tubes can "see" through smoke and locate hidden obstacles, such as a burning stairs which present danger. They are now widely used in fire-fighting equipment. They have also found use in the location of people and were used in Mexico City to search out those trapped in collapsed buildings after the earthquake. In medicine, similar cameras can locate disease in the body at an early stage by detecting and locating 'hot spots', often the first sign of the disease.

The Rank Prize Funds were established by the late Lord (J. Arthur) Rank, shortly before his death in 1972. He selected two areas which he believed to be of special benefit to mankind: opto-electronics and animal nutrition. In addition to the prizes (these opto-electronics awards totalled some £115 000) the Funds sponsor research projects, international symposia and other meetings particularly for young scientists in these two areas.



One of two 13m C-band antennae being installed by Marconi at Whiehill, Oxon as part of an Inmarsat earth station for Mercury Communications.

European passport for engineers

A new title: "European Engineer" is to be introduced by FEANI (International Federation of National Engineers Associations). It will be open to Europe's one million professional engineers, including the 200 000 Chartered Engineers in the UK. An agreement, reached after several years of negotiations at FEANI, offers Europe-wide professional standards by providing for mutual recognition of qualifications. The British National Committee took an initiative by embodying training and experience along with academic qualifications as part of the formula now accepted by the 20 countries represented at FEANI.

The new title will be granted to engineers who have successfully completed an approved degree, training and experience of not less than seven years in total. UK chartered engineers will generally be recognized as possessing qualifications satisfying the requirements of the new title. These minimum requirements will act as an incentive to individual improvement and as a lever for raising standards; a crucial objective if the European industrial base is to compete with the USA and Japan, according to FEANI.

The title should become a passport for working at professional engineer level throughout Europe. A similar scheme is planned for technician engineers.

Don't cut us off – aged and infirm

BT has few procedures for checking that a telephone user is elderly or disabled before disconnecting them if they do not pay their bills. The Advisory Council on Telecommunications for Disabled and Elderly People (DIEL) called on BT to make a concerted effort to ensure that this did not happen. DIEL is aware of concern that some people may be cut off during illness or hospitalization. The risk of disconnection could be avoided if BT's billing and follow-up system were more flexible.

BT have said that improvements can be expected once fully computerized systems come into operation, but DIEL demands more immediate action to adjust the procedures where the old and infirm are concerned.

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Technology training in Sheffield

A joint venture between Sheffield City Polytechnic and the Manpower Services Commission Sheffield Skillcentre has resulted in the launching of an Centre for Advanced Manufacturing Technology in the city.

It offers a complete training package for all levels of company personnel from shop-floor to boardroom, and includes a consultancy and advisory service. The centre is provided with a mainframe computer but also has a data link to the Polytechnic's computer, effectively doubling its capacity. The facilities were demonstrated at the opening ceremony by designing a component on the computer, obtaining the manufacturing instructions and then actually making the part on a c.n.c. machine tool. The Prime Computer with eight workstations has a comprehensive range of software including Cad/cam, manufacturing systems simulation, and production control. The Centre's facilities include a number of c.n.c. machine tools, materials handling equipment and robot systems. "The computer and robot are no longer 'new technology' said Bryan Nicholson, chair of the Manpower Services Commission at the opening ceremony; "They are tools to be used in the same way we use conventional tools."

The centre can also offer impartial advice on the selection of equipment, free from the pressure of sales reps.

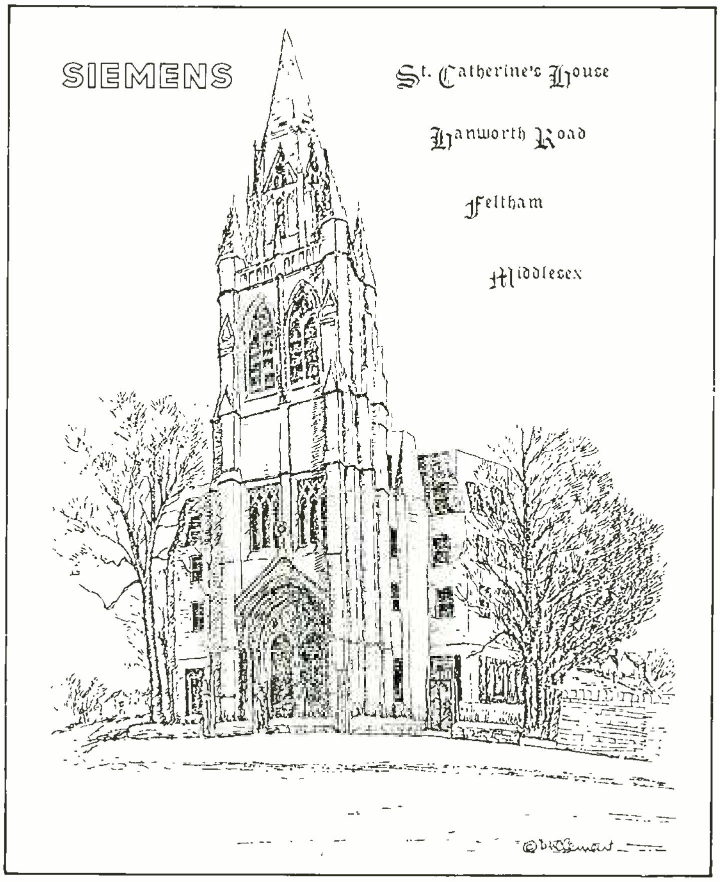
IT still puzzles managers

Despite recognizing that it is important, many managers are not using information technology as well as they might. So says John Butcher, Undersecretary for Industry. He pointed out that a DTI survey showed that very few companies had achieved more that 80% of the potential usage of IT; the average is about 55% and a third of the companies surveyed were below 40%. He put the blame on management training: "It is widely agreed that our managers are on average less well trained for their jobs than the managers of our international competitors.

"Fewer than 10% of the 2.5M managers hava a degree. A further seven percent have membership of a professional body as their highest qualification. Only two percent can boast of any kind of business degree or management qualification. Worse still, 70% of the managers get no training at all for their management role at any time during their careers. But with the introduction of new technology, the need for continuing training can only increase.

"Of course the picture is not all gloom. Many of Britain's best run companies operate highly developed management and staff training programmes. We need to see this best practice being adopted by many more companies."

Mr Butcher warned that organizations which chose not to take advantage of the simple cost saving that IT made possible should bear in mind that competitors at home and abroad certainly will.

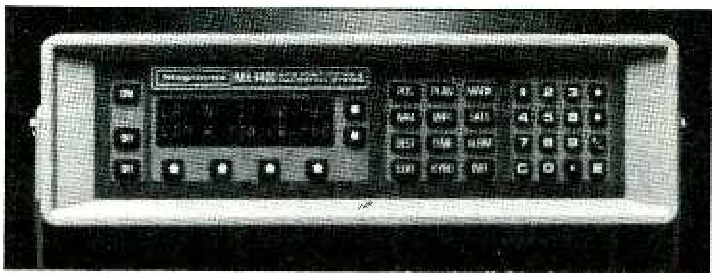


This unfrocked church at Feltham, Middlesex is now in secular hands as a temple of information technology. Siemens Ltd have remodelled it extensively as a training and consultancy centre, a base for expanding the company's activities in the UK telecommunications and computer markets. Picture was produced on one of Siemens' new laser printers, which can churn out 100 pages/min.

Optical cable across the Atlantic

Telecommunications authorities in the UK, USA, Canada, France and Spain have agreed on the construction of an optical-fibre cable that will be ready for service in 1991 and will have land terminals in each of the five countries. Other countries are to be invited to become joint owners of the \$400M cable which will be known as TAT9.

Already planned is a shift from the more usual transmission wave-length of 1.3μm to 1.55μm which is more efficient and would require fewer amplifiers. The transmission rate of 565Mbit/s will double that planned for earlier cables. The main transatlantic section and the UK and USA branches will have two operational fibre pairs. A submerged multiplex branching unit is planned to provide flexible routing for signals between the countries with landing points. All the landing points are to linked to the local networks and so the French and Spanish branches, for instance, could link a major part of Europe to the cable.



This Magnavox satellite receiver can tell exactly where it is to within a few metres, using the signals from the US Navstar satellites. The US Defence department are likely to scramble the P-codes used to obtain the more accurate positioning and will only licence those who are friendly to the US. However if an MX4400 is used in a fixed, known position it can unscramble the codes and transmit a correction signal to another mobile unit which can then fix its position more accurately than if it had access to the codes. The Navstar program has been delayed by the Challenger tragedy.

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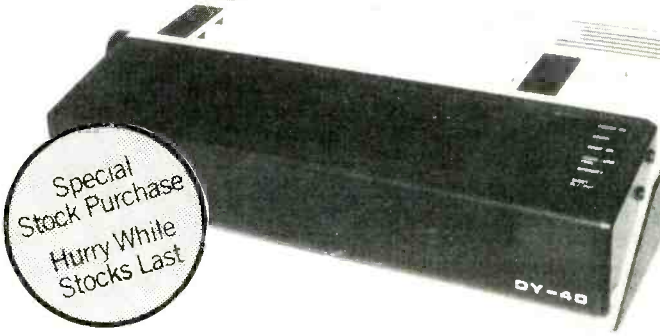
There must be something wrong!

This? for This?



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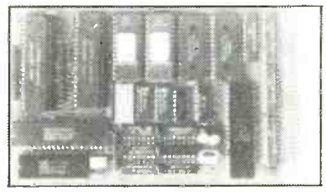

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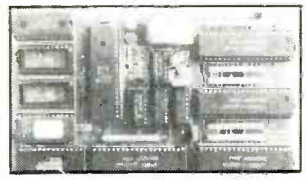

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7446A	1.00
7447A	1.00
7448	1.00
7450	0.36
7451	0.35
7453	0.38
7454	0.38
7460	0.55
7470	0.50
7472	0.45
7473	0.45
7474	0.50
7475	0.60
7476	0.45
7480	0.65
7481	1.80
7483A	1.05
7484A	1.25
7485	1.10
7486	0.42
7489	2.10
7490A	0.55
7491	0.70
7492A	0.70
7493A	0.55
7494	1.10
7495A	0.60
7496	0.80
7497	2.10
74100	1.90
74107	0.50
74109	0.75
74110	0.75
74111	0.55
74116	1.70
74118	1.10
74119	1.70
74120	1.00
74121	0.55
74122	0.70
74123	0.80
74125	0.65
74126	0.55
74128	0.55
74132	0.75
74136	0.70
74141	0.90
74142	2.50
74143	1.30
74144	2.70
74145	1.10
74147	1.70
74148	1.40
74150	1.75
74151A	0.70
74153	0.80
74154	1.40
74155	0.80
74156	0.90
74157	0.80
74159	1.75
74160	1.10
74161	0.80
74162	1.10
74163	1.10
74164	1.20
74165	1.10
74166	1.40
74167	4.00
74170	2.00
74172	4.20
74173	1.40
74174	1.10
74175	1.05
74176	1.00
74178	1.50
74179	1.50
74180	1.00
74181	3.40
74182	1.40
74184	1.80
74185A	1.80
74190	1.30
74191	1.30
74192	1.10
74193	1.15
74194	1.10
74195	0.80
74196	1.30
74197	1.10
74198	2.20
74199	2.20
74221	1.10
74251	1.00
74259	1.50
74265	0.80
74273	2.00
74276	1.40
74278	1.70
74279	0.90
74283	1.05
74742	3.20
74290	0.90
74293	0.90
74298	1.80
74351	2.00
74365A	0.80
74366A	0.80
74367A	0.80
74376	1.60
74390	1.10
74393	1.20
74490	1.40

74LS SERIES

74LS00	0.24
74LS01	0.24
74LS02	0.24
74LS03	0.24
74LS04	0.24
74LS05	0.24
74LS08	0.24
74LS09	0.24
74LS10	0.24
74LS11	0.24
74LS13	0.34
74LS14	0.50
74LS15	0.24
74LS20	0.24
74LS21	0.24
74LS22	0.24
74LS24	0.50
74LS26	0.26
74LS27	0.24
74LS28	0.24
74LS30	0.24
74LS32	0.24
74LS32	0.24
74LS33	0.24
74LS37	0.24
74LS38	0.24
74LS40	0.24
74LS42	0.50
74LS43	1.50
74LS48	0.90
74LS49	1.00
74LS51	0.24
74LS54	0.24
74LS55	0.24
74LS73A	0.30
74LS74A	0.35
74LS75	0.45
74LS76A	0.36
74LS78	0.42
74LS83A	0.70
74LS85	0.75
74LS86	0.35
74LS90	0.48
74LS91	0.90
74LS92	0.35
74LS93	0.54
74LS95B	0.75
74LS96	0.90
74LS107	0.40
74LS109	0.40
74LS112	0.45
74LS113	0.45
74LS114	0.45
74LS122	0.70
74LS123	0.80
74LS125	0.50
74LS126	0.50
74LS132	0.65
74LS133	0.55
74LS136	0.45
74LS138	0.55
74LS139	0.55
74LS145	0.95
74LS147	1.75
74LS148	1.40
74LS151	0.65
74LS152	2.00
74LS153	0.65
74LS154	1.60
74LS155	0.65
74LS156	0.65
74LS157	0.50
74LS158	0.65
74LS160A	0.65
74LS161A	0.75
74LS162A	0.75
74LS163A	0.75
74LS164	0.75
74LS165A	1.10
74LS166A	1.50
74LS168	1.30
74LS169	1.00
74LS170	1.40
74LS173A	1.00
74LS174	0.75
74LS175	0.75
74LS181	2.00
74LS183	1.90
74LS190	0.75
74LS191	0.75
74LS192	0.80
74LS194A	0.75
74LS195A	0.75
74LS196	0.80
74LS197	0.80
74LS221	0.90
74LS240	0.80
74LS241	0.80
74LS242	0.90
74LS243	0.90
74LS244	0.80
74LS245	1.10
74LS247	1.10
74LS248	1.10
74LS249	1.10
74LS251	0.75
74LS253	0.75
74LS256	0.90
74LS2457A	0.70
74LS258A	0.70
74LS259	1.20
74LS260	0.75
74LS266	0.60
74LS273	1.25
74LS279	0.70
74LS280	1.90
74LS283	0.80
74LS290	0.80
74LS292	9.00
74LS293	0.80
74LS295	1.40
74LS297	9.00
74LS298	1.00
74LS299	2.20
74LS321	3.70
74LS322A	3.90
74LS323	3.00
74LS324	3.20
74LS348	2.00
74LS352	1.20
74LS353	1.20
74LS356	2.10
74LS363	1.80
74LS364	1.80
74LS365	0.50
74LS366	0.50
74LS367	0.52
74LS368	0.50
74LS373	0.90
74LS374	0.90
74LS375	0.75
74LS377	1.30
74LS378	0.95
74LS379	1.30
74LS381	4.50
74LS385	3.25
74LS390	0.60
74LS393	1.00
74LS395A	1.00
74LS399	1.40
74LS445	1.80
74LS465	1.20
74LS467	1.20
74LS490	1.50
74LS540	1.00
74LS541	1.00
74LS608	7.00
74LS610	19.00
74LS612	19.00
74LS624	3.50
74LS626	2.25
74LS628	2.25
74LS629	1.25
74LS640	2.00
74LS640-1	3.00
74LS641	1.50
74LS642	2.50
74LS642-1	3.00
74LS643	2.50
74LS643-1	3.00
74LS644	3.50
74LS645	2.00
74LS645-1	4.00
74LS668	0.90
74LS669	0.90
74LS670	1.70
74LS682	2.50
74LS683	3.00
74LS684	3.50
74LS687	3.50
74LS688	3.50
74LS783	21.00

74S SERIES

74S00	0.50
74S02	0.50
74S04	0.50
74S05	0.50
74S08	0.50
74S10	0.50
74S11	0.75
74S20	0.50
74S22	0.50
74S30	0.50
74S32	0.60
74S37	0.60
74S38	0.60
74S40	0.50
74S51	0.60
74S64	0.45
74S74	0.70
74S85	3.00
74S86	1.00
74S112	1.50
74S113	1.20
74S114	1.20
74S124	3.00
74S132	1.00
74S133	0.60
74S138	1.80
74S139	1.80
74S140	1.00
74S151	1.50
74S153	1.50
74S157	2.00
74S158	2.00
74S163	3.00
74S169	5.50
74S174	3.00
74S175	3.20
74S188	1.80
74S189	1.80
74S194	3.00
74S195	3.00
74S196	3.50
74S200	4.50
74S201	3.20
74S225	5.20
74S240	4.00
74S241	4.00
74S244	4.50
74S251	2.50
74S257	2.50
74S258	2.50
74S260	1.00
74S261	3.00
74S283	2.70
74S287	2.25
74S288	2.00
74S289	2.25
74S299	4.50
74S373	4.00
74S374	4.00
74S387	2.25

74C SERIES

74C00	0.70
74C04	0.50
74C08	0.70
74C10	0.70
74C14	0.50
74C20	0.70
74C32	1.00
74C42	1.50
74C48	1.50
74C73	1.00
74C74	1.00
74C76	1.00
74C83	2.00
74C85	2.25
74C86	0.50
74C90	1.90
74C93	1.50
74C95	1.60
74C107	1.00
74C150	5.00
74C151	2.00
74C157	2.50
74C160	1.80
74C161	1.80
74C162	1.80
74C163	1.80
74C173	1.00
74C174	1.50
74C175	1.50
74C193	1.50
74C194	1.50
74C195	1.50
74C221	2.50
74C244	2.00
74C245	2.25
74C373	2.25
74C374	2.25
74C902	1.20
74C911	9.00
74C912	4.50
74C922	6.00
74C923	6.50
74C925	6.50
74C926	7.50

74ALS SERIES

74ALS00	0.45
74ALS02	0.45
74ALS04	0.50
74ALS08	0.50
74ALS10	0.45
74ALS20	0.45
74ALS32	0.45
74ALS74	0.70
74ALS138	1.50
74ALS139	1.50
74ALS244	4.00
74ALS245	4.75
74ALS573	2.60
74ALS574	4.50
74ALS580	2.60

[illegible]

4000	0.20
4001	0.24
4002	0.25
4006	0.70
4007	0.25
4008	0.60
4009	0.45
4010	0.60
4011	0.24
4012	0.25
4013	0.36
4014	0.60
4015	0.70
4016	0.36
4017	0.55
4018	0.60
4019	0.60
4020	0.80
4021	0.60
4022	0.70
4023	0.30
4024	0.48
4025	0.24
4026	0.90
4027	0.40
4028	0.60
4029	0.75
4030	0.35
4031	1.25
4032	1.00
4033	1.25
4034	2.50
4035	0.70
4036	2.50
4037	1.10
4038	1.00
4040	0.60
4041	0.55
4042	0.50
4043	0.60
4044	0.60
4045	1.00
4046	0.60
4047	0.60
4048	0.55
4049	0.36
4050	0.35
4051	0.65
4052	0.60
4053	0.60
4054	0.80
4055	0.80
4056	0.85
4060	0.70
4063	0.85
4066	0.40
4067	2.30
4068	0.25
4069	0.24
4070	0.24
4071	0.24
4072	0.24
4073	0.24
4075	0.24
4076	0.65
4077	0.25
4078	0.25
4081	0.24
4082	0.25
4085	0.60
4086	0.75
4089	1.20
4093	0.35
4094	0.90
4095	0.95
4096	0.90
4097	2.70
4098	0.75
4099	0.99
4501	0.36
4502	0.55
4503	0.36
4504	0.95
4505	3.60
4506	0.90
4507	0.35
4508	1.20
4510	0.55
4511	0.55
4512	0.55
4513	1.50
4514	1.10
4515	1.10
4516	0.55
4517	2.20
4518	0.48
4519	0.32
4520	0.60
4521	1.15
4522	0.80
4526	0.70
4527	0.80
4528	0.65
4529	1.00
4531	0.75
4532	0.65
4534	3.80
4536	2.50
4538	0.75
4539	0.75
4541	0.90
4543	0.70
4551	1.00
4553	2.40
4555	0.36
4556	0.50
4557	2.40
4560	1.40
4566	1.40
4568	2.40
4569	1.70
4572	0.45
4583	0.90
4584	0.48
4585	0.60
4724	1.50
14411	7.50
14412	7.50
14416	3.00
14419	2.60
14490	4.20
14495	4.50
145000	6.50
14599	2.00
22100	3.50
22101	7.00
22102	7.00
40014	0.48
40085	1.20
40097	0.36
40098	0.40
40100	1.50
40101	1.25
40102	1.30
40103	2.00
40104	1.20
40105	1.50
40106	0.48
40107	0.55
40108	3.20
40109	0.80
40110	2.25
40114	2.25
40147	2.80
40163	1.00
40173	1.20
40174	1.00
40175	1.00
40192	1.00
40193	1.00
40194	1.00
40244	1.50
40245	1.50
40257	1.80
40373	1.80
40374	1.80
80C95	0.75
80C97	0.75
80C98	0.75

LINEAR ICs

AD7581	12.00
ADC0808	11.90
AM7910DC	25.00
AN-1-5C50	1.00
AY-3-1350	3.50
AY-3-8910	4.90
AY-3-8912	5.00
CA3019A	1.00
CA3020	3.50
CA3028A	1.10
CA3046	0.70
CA3059	3.25
CA3060	3.50
CA3080E	0.70
CA3085	1.50
CA3086	0.60
CA3089E	2.50
CA3090AQ	3.75
CA3130E	0.90
CA3130T	1.30
CA3140E	0.45
CA3140T	1.00
CA3146	2.25
CA3160E	1.50
CA3161E	2.00
CA3162E	6.00
CA3189E	2.70
CA3240E	1.50
CA3280G	3.00
D7002	6.00
DAC1408-8	3.00
DAC0800	3.00
DAC0808	3.00
DG308	3.00
HA1366	1.90
ICL7106	6.75
ICL7611	0.95
ICL7650	4.00
ICL7660	2.50
ICL8038	4.00
ICM7216B	22.00
ICM7217	7.50
ICM7555	0.90
ICM7556	1.40
LC7120	3.00
LC7130	3.00
LC7131	3.50
LC7137	3.50
LF347	1.20
LF351	0.60
LF353	0.90
LF355	0.90
LF356N	1.10
LF357	1.00
LF398	4.00
LM10CLH	4.50
LM301A	0.30
LM307	0.45
LM308CN	0.75
LM310	2.25
LM311	0.60
LM318	1.50
LM319	1.80
LM324	0.45
LM334Z	1.15
LM335Z	1.30
LM336	1.60
LM339	0.40
LM348	0.60
LM358P	0.50
LM377	3.00
LM380N-8	1.50
LM380N	1.50
LM381AN	1.70
LM383	3.25
LM384	2.20
LM386N-1	1.00
LM387	2.70
LM389	1.89
LM391	1.80
LM392N	1.10
LM393	0.85
LM394CH	4.00
LM709	0.35
LM710	0.48
LM711	1.00
LM723	0.60
LM725CN	3.00
LM733	0.65
LM741	0.22
LM7747	0.70
LM748	0.30
LM1011	4.80
LM1014	1.50
LM1801	3.00
LM1830	2.50
LM1871	3.00
LM1872	3.00
LM1886	6.00
LM1889	4.50
LM2917	3.00
LM3302	0.90
LM3900	0.80
LM3909	1.00
LM3911	1.80
LM3914	3.50
LM3915	3.40
LM3916	3.40
LM13600	1.50
M51513L	2.30
M51516L	4.50
MB3712	2.00
MC1310P	1.50
1413	0.75
MC1458	0.45
MC1495	3.00
MC1496	0.70
MC3340P	2.00
MC3401	0.70
MC3403	0.65
MF10CN	4.10
MK50240	9.00
MK50398	11.00
ML902	5.00
ML922	4.00
MM6221A	3.00
NE529	2.20
NE531	1.20
NE544	1.90
NE555	0.22
NE556	0.60
NE564	4.00
NE565	1.20
NE566	1.50
NE567	1.25
NE570	4.00
NE571	3.00
NE592	0.90
NE5532P	1.60
NE5533P	1.60
NE5534P	1.20
NE5534AP	1.50
OP-07EP	3.50
PLL02A	5.00
RC4136	0.55
RC4151	2.00
RC4195	1.50
RC4558	0.55
S566B	2.20
S50240	9.00
SAA1900	16.00
SFF96364	8.00
SL490	3.00
SN76013N	3.00
SN76023N	3.00
SN76033N	3.00
SN76115N	2.15
SN76489	4.00
SN76495	4.00
SN76660	1.20
SPO256AL2	7.00
SP8515	7.50
TA7120	1.20
TA7130	1.40
TA7204	1.50
TA7205	0.90
TA7222	1.50
TA7310	1.50
TBA641BX1	4.00
TBA231	1.20
TBA800	0.80
TBA810	0.90
TBA20	0.80
TBA820M	0.75
TBA920	2.00
TBA950	2.25
TC9109	5.00
TCA210	3.50
TCA220	3.50
TCA270	3.50
TCA940	1.75
TDA1004A	5.00
TDA1010	2.25
TDA1022	4.50
TDA1024	1.10
TDA1170S	3.00
TDA2002	3.25
TDA2003	1.90
TDA2004	2.40
TDA2006	3.20
TDA2020	3.20
TDA2030	2.50
TDA2593	5.00
TDA2653	7.00
TDA3560	7.50
TDA3810	7.50
TDA7000	3.50
TEA1002	7.00
TL061CP	0.40
TL062	0.60
TL064	0.90
TL071	0.40
TL072	0.70
TL074	1.10
TL081	0.35
TL082	0.55
TL083	0.75
TL084	1.00
TL094	2.00
TL170	0.50
TL430C	1.20
UAA1003-3	9.35
UA759	3.00
UA2240	1.20
UAA170	1.70
UCN4801A	4.00
ULN2001A	0.75
ULN2002A	0.75
ULN2003A	0.75
ULN2004A	0.75
ULN2068	2.90
ULN2802	1.90
ULN2803	1.80
ULN2804	1.90
UPC575	2.75
UPC592H	2.00
UPC1156H	3.00
UPC1185H	5.00
XR210	4.00
XR2206	4.50
XR2207	3.75
XR2211	5.75
XR2216	6.75
XR2240	1.20
ZN404	1.00
ZN414	0.80
ZN419P	1.75
ZN423E	1.30
ZN424E	1.30
ZN425E8	3.50
ZN426E8	3.00
ZN427E8	6.00
ZN428E8	4.50
ZN429E8	2.25
ZN447E	9.00
ZN449E	3.00
ZN450E	7.50
ZN459CP	3.00
ZN1034E	2.00
ZNA1040	6.60
ZNA134J	23.00
ZNA234E	9.50

VOLTAGE REGULATORS

1A FIXED VOLTAGE PLASTIC TO220

+VE			−VE	
5V	7805	0.45	7905	0.50
6V	7806	0.50	7906	0.50
8V	7808	0.50	7908	0.50
12V	7812	0.45	7912	0.50
15V	7815	0.50	7915	0.15
18V	7818	0.50	7918	0.50
24V	7824	0.50	7924	0.50

1A FIXED VOLTAGE PLASTIC TO92

5V 78L05	0.30	5V 79L05 0.45
6V 78L06	0.30	12V 79L12 0.50
8V 78L08	0.30	15V 79L15 0.50
12V 78L12	0.30	
15V 78L15	0.30	

OTHER REGULATORS

FIXED REGULATORS

LM309K	1A 5V	1.40
LM323K	3A 5V	3.50
78H05KC	5A 5V	5.40
78H12	5A 12V	6.40
78P05	10A 5V	9.00

VARIABLE REGULATORS

LM305AH		2.50
LM317T	TO-220	1.50
LM317K	TO3	2.40
LM337T		2.25
LM350T	10A+VAR	4.00
LM396K	10A+VAR	15.00
LM723N		0.50
78HHO5KC	5A 5V	5.75
78HGKC	5A+VAR	6.50
78GUIC	1A+VAR	2.25
79HGKC	5A−VAR	6.75
79GUIC	1A−VAR	2.50

SWITCHING REGULATIONS

ICL7660	2.50
SG3524	3.00
TL494	3.00
TL497	3.00
78S40	2.50
RC4195	1.50

COMPUTER COMPONENTS

CPU

1802CE	6.50
2650A	10.50
6502	4.50
65C02-2MHz	12.00
6502A	6.50
6502B	8.00
6800	2.50
6802	3.00
6803-2	12.00
6809	6.50
6809E	10.00
68B09	10.00
68B09E	12.00
68000-L8	36.00
8035	3.50
80C35	6.00
8039	4.20
80C39	7.00
8080A	4.20
8085A	3.00
80C85A	7.50
8086	22.00
8088	17.50
8741	15.00
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75122	1.40
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75154	1.20
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6.00MHz	1.40
6.144MHz	1.40
7.00MHz	1.50
7.16MHz	1.75
8.00MHz	1.50
8.867MHz	1.75
10.00MHz	1.75
10.50MHz	2.50
10.70MHz	1.50
11.00MHz	3.00
12.00MHz	1.50
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MAN4640	200p
MAN6610	200p
MAN8910	120p
NSB5881	570p
SFH305	100p
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TIL32	75p
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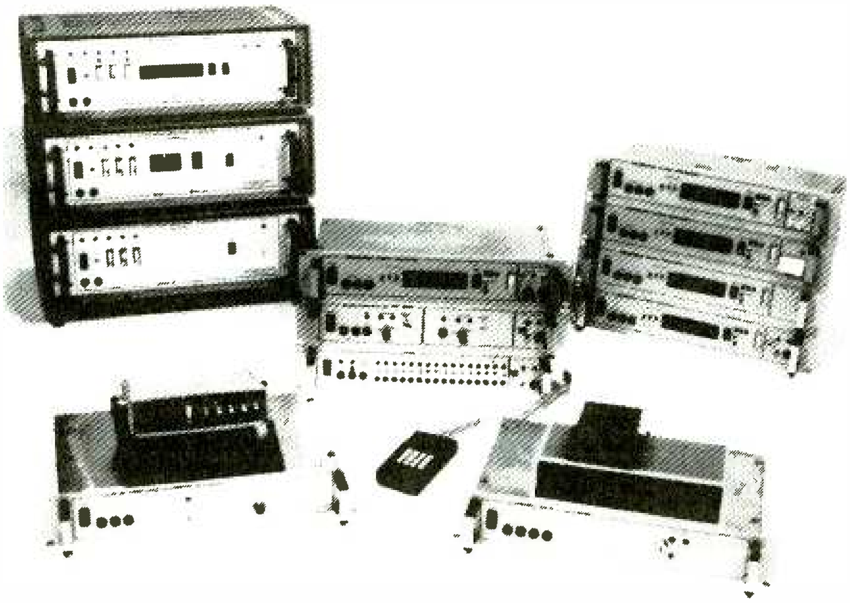

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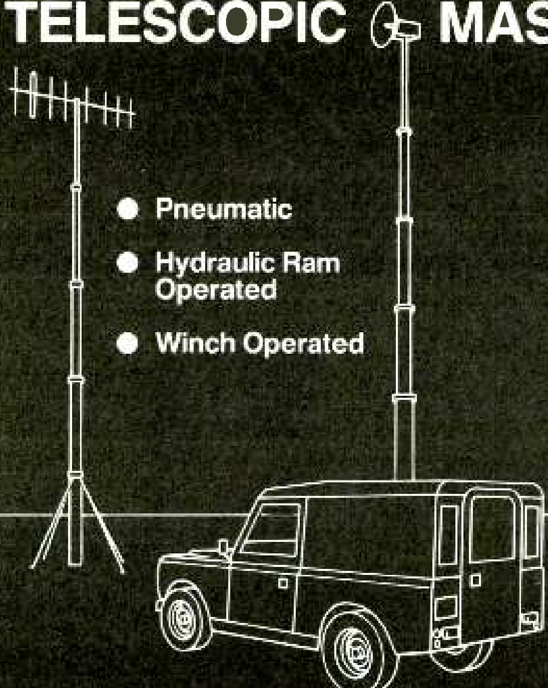

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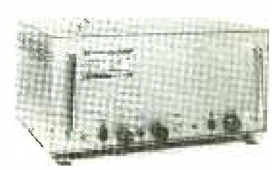

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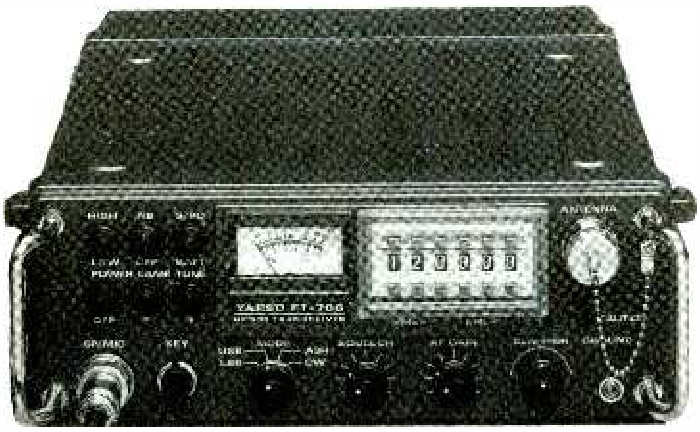

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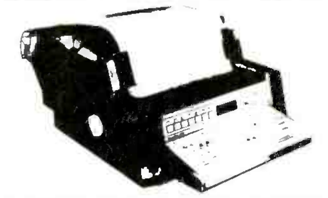

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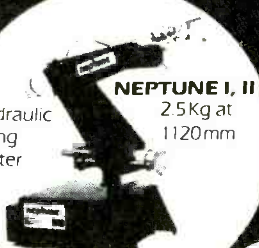

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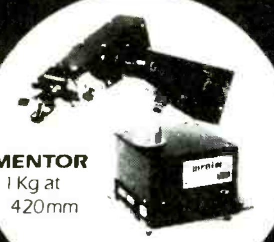

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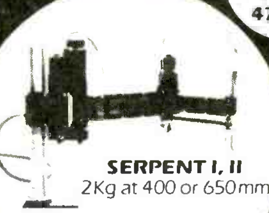

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Designing with dynamic memory

How dynamic memory works and how to interface it with 68000 systems.

by Alan Clements
Teesside Polytechnic

Alan Clements is senior lecturer in computer science at Teesside Polytechnic. He became interested in microprocessors while working for his doctorate on an iterative approach to adaptive detection of orthogonal groups, which involved the design of high speed digitial equalizers. This article is based on a forthcoming book – his third – on the 68000.

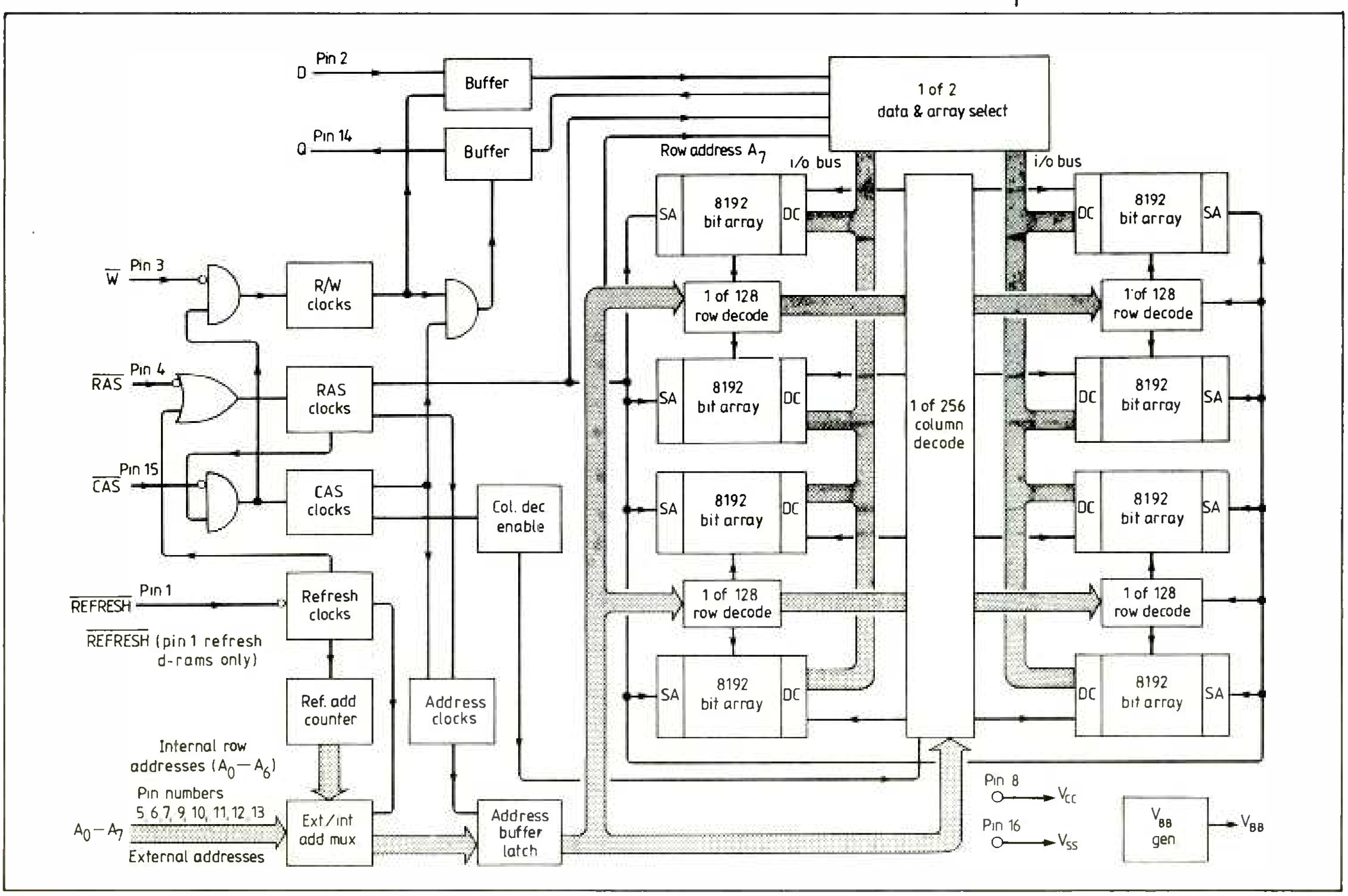
Dynamic memory is a form of low-cost, random access memory usually associated with memory arrays larger than about 64Kbytes; smaller arrays are frequently implemented as static ram. Like its static counterpart, dynamic read/write ram (d-ram for short) is available in a number of different formats. At the moment the preferred dynamic memory is organized as 256K by 1 bits. The older 16K part is still being sold to support existing systems, and the 1M × 1 part is finding its way into some applications of microprocessors, but this article is about the 64K device because of its low-cost and popularity.

Dynamic memory stores information as charge on a capacitor forming the inter-electrode capacitance of a metal oxide field-effect transistor. The capacitor is leaky, and its charge gradually lost, so some mechanism is needed to periodically restore it. This refreshing is performed at least once every 2 ms.

Manufacturers argue, quite rightly, that it is irrational to put very high density memory chips in physically large packages; this defeats the object of producing compact memory modules. A dynamic ram of 64K × 1 might be expected to have 16 address pins, two for power, one each for chip select, R/W and data pin, at least 21 pins in all, which would require a 24-pin package, taking up a nominal $1.2 \times 0.6 = 0.72$ in^2 of board space.

The majority of dynamic memories have multiplexed address buses, so that for a 64K chip a 16-bit address is fed in as two separate 8-bit values. This reduces the address bus requirement to eight pins, but needs two strobes to latch the address. The $\overline{\text{RAS}}$ (row address strobe) latches the 8-bit row address, and then the $\overline{\text{CAS}}$ (column address strobe) latches the 8-bit column address. The address multiplexing and the control of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ strobes

Fig. 1. Internal arrangement of a typical 64K dynamic ram.



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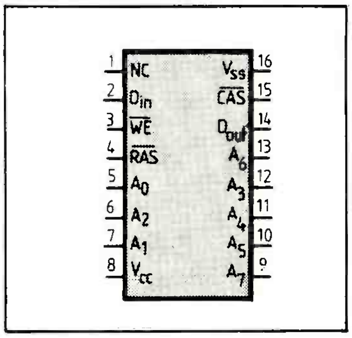

Fig. 2. Pinout of HM4864-2 64K dynamic ram.

are done off-chip with logic supplied by the user. Consequently a 64K dynamic ram can now fit into a 16-pin dual in-line package, taking up a board space of $0.8 \times 0.3 = 0.24$ in^2.

Figure 1 gives the internal arrangement of a typical 64K dynamic memory and Fig. 2 its pinout. Data are stored in one of eight arrays, each of 8192 bits. There is not enough space here to delve into the internal operation of the dynamic memory, as its circuitry is so complex. Early dynamic rams required three power supplies, at +12V, + 5V and −5V, the +12V to provide clock pulses of adequate amplitude within the chip and the −5V the substrate bias. Fortunately for the system designer, current 16K and larger chips operate from the system +5V V_{cc} supply alone. Dynamic memories still need a negative V_{bb} supply, but it is now derived on-chip from an internal generator.

A difficulty associated with dynamic memory is the alpha-particle problem. As the capacitance on which each bit of data is stored is exceedingly tiny an alpha particle, i.e. a helium ion, passing through a memory cell can cause sufficient ionization to corrupt the stored data, creating a 'soft error' (so called as the cell has not been permanently damaged, but has lost its stored data). The alpha-particle contamination comes largely from the encapsulating material, and through manufacturers attempt to minimize the problem by careful quality control of the encapsuation material it is impossible to reduce the soft-error rate to zero.

An approach to soft error control is to build special memory arrays that can detect, or even detect and correct, soft-errors. As long as soft errors are relatively infrequent, this approach yields a very large mean time between undetected soft errors. Error detection and correction is not yet done inside the memory components: it must be provided by the memory systems designer.

There are few things in the known universe more terrifying than the timing diagrams of a dynamic ram. Not only do they look hopelessly complex, there are 35 or more parameters associated with them. The best way of approaching the dynamic ram timing diagram is to strip it of all but its basic features, and add the fine detail when the simplified model has been digested.

Figure 3 gives an outline of the basic dynamic memory timing diagram during a read cycle. To put this diagram into context, look at the arrangement of a 64K word by 16-bit memory based on the 64K × 1 chip, Fig. 4. Each memory component has its eight address inputs (labelled A_0 to A_7) connected to the eight ouputs of the address multiplexer, MPLX. The inputs to the address multiplexer are A_{01} to A_{08} (the row address) and A_{09} to A_{16} (the column address) from the 68000. Assume that when MPLX is low the row address is selected, and when high the column address is selected. Note that the 23 address lines from the 68000, A_{01} – A_{23}, select one of 2^{23} word (i.e. 16-

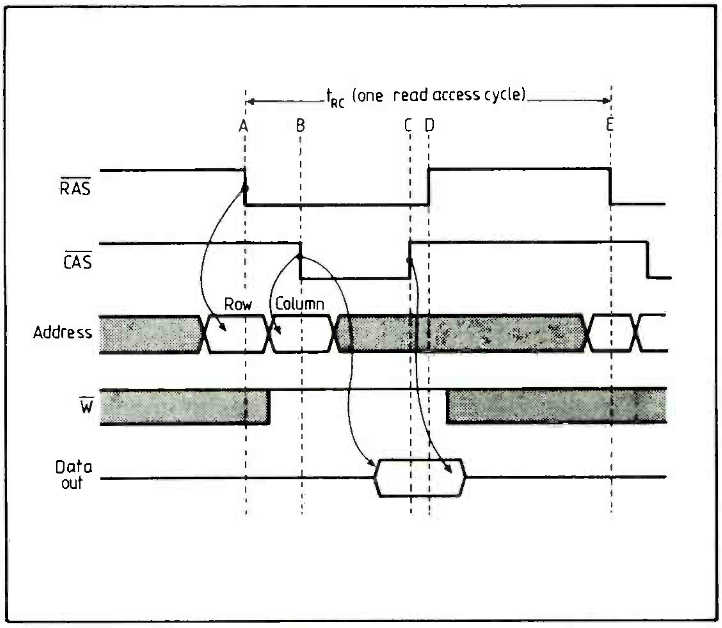

Fig. 3. Basic read cycle timing diagram of a dynamic ram in which the falling edge of the row address strobe latches the row address into the d-ram. Falling edge of the column address strobe latches the column address to complete the caputre of a 16-bit address. Read cycle is terminated when the first of $\overline{\text{CAS}}$ or $\overline{\text{RAS}}$ goes high.

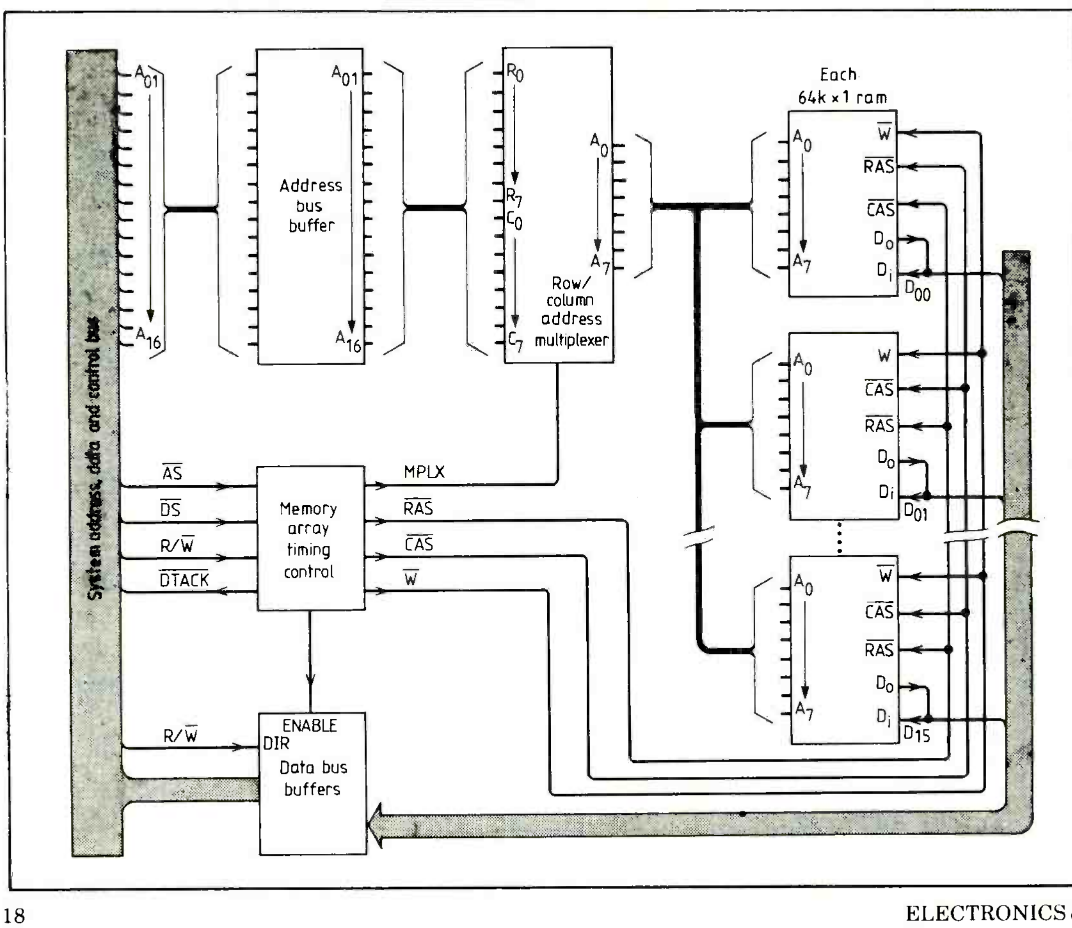

Fig. 4. A minimal d-ram module contains three elements: array itself, address multiplexer and timing control circuit which controls the multiplexer and generates $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ from the processor's own timing signals.

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bit) addresses. The two data strobes, $\overline{LDS}$ and $\overline{UDS}$, select the lower or upper or both bytes of the word addressed by $A_{01} - A_{23}$.

The data-in and out pins of each memory component in Fig. 4 are strapped together in this application, and are connected to the system data bus after suitable buffering. Four signals, MPLX, $\overline{RAS}$, $\overline{CAS}$, and $\overline{W}$, control the operation of the memory system. The timing control module must furnish these signals from the available system control signals. In other words, the design of the timing control module will vary from one microprocessor system to another, as each processor has its own unique timing signals. Note that Fig.4 is simplified in two ways. We have not provided the byte/word control required by the 68000, and no facilities for refreshing the dynamic memory are yet available. A read cycle in Fig. 3 lasts from A to E, and has a minimum duration of t_{RC}, the read cycle time. For convenience, this section illustrates the dynamic memory timing diagram with the HM4864-2, a 150ns component. The minimum value for t_{RC} is given as 270ns. Note that dynamic memory has a cycle time much greater (270 ns) than its access time (150 ns), unlike static memory which has equal access and cycle times. The designer of a dynamic memory system cannot, therefore, begin the next access as soon as the current one has been completed. This is because the dynamic memory performs an internal operation, known as pre-charging between accesses.

The first step in a read cycle is to provide the chip with the lower-order bits of the address on its eight address inputs, A_0 to A_7. Then, at point A, the row address strobe, $\overline{RAS}$, is brought active-low to strobe the row address into the chip's internal latches.

Once this has been done, the low-order address is redundant and is not needed for the rest of the cycle. Contrast this with the static ram, where the address must be stable for the entire read or write cycle.

The eight higher-order address bits are then applied to the address inputs of the memory, and the column address strobe ($\overline{CAS}$) brought active-low at point B to latch the column address. Now the entire 16-bit address has been acquired by the memory and the contents of the system address bus can change.

Once $\overline{CAS}$ has gone low, the addressed memory cell responds by placing data on its data-output terminal, allowing the processor to read it. At the end of the read cycle, $\overline{CAS}$ returns inactive-high and the data bus drivers are turned off, floating the data bus. $\overline{RAS}$ and $\overline{CAS}$ may both go high together, or in any order. It does not matter as long as all other timing requirements are satisfied.

To make explanation of the dram more tractable, we break it up into its component parts, beginning with a discussion of the role of the address pins.

Address timing

Details of the address timing requirements shown in Fig. 5, an enlargement of the address bus timing in Fig. 3, are effectively the same as those of a typical latch. The row address must be stable for a minimum of t_{ASR} seconds before the falling edge of the $\overline{RAS}$ strobe. As the minimum value of t_{ASR} is quoted as zero, the address has a zero setup time and does not have to be valid prior to the falling edge of $\overline{RAS}$. In the worst case, it must be valid coincident with the falling edge of $\overline{RAS}$. Once $\overline{RAS}$ is low, the row address must be stable for t_{RAH}, the row address hold time, before it can change. The hold time is 20ns minimum, which restricts the time before which the column address may be multiplexed onto the chip's address pins.

Once the row address hold time has been satisfied and the column address multiplexed onto the memory's address pins, $\overline{CAS}$ may go low. The column address setup time, t_{ASC}, is quoted as −10 ns minimum, so that $\overline{CAS}$ may go low up to 10ns *before* the column address has stabilized. After CAS has gone low, the column address must be stable for a further t_{CAH} seconds, the column address hold time, before it may change. Once t_{CAH} (45ns minimum) has been satisfied, the address bus plays no further role in the current access.

An important parameter in

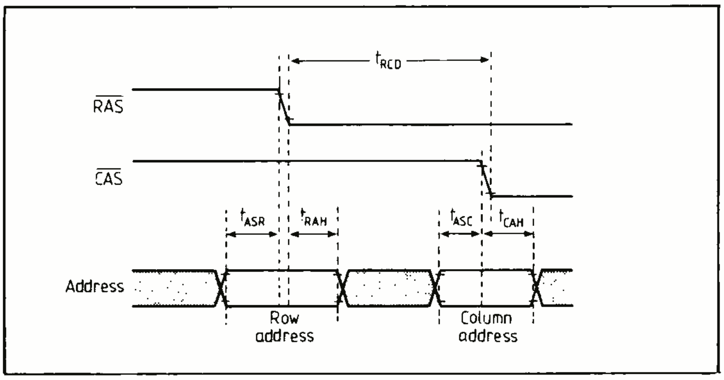


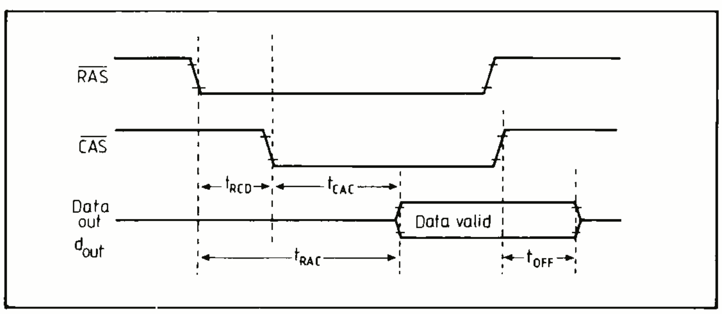
Fig. 5. In the address timing of a d-ram, the row address must be valid from t_{ASR} seconds before the falling edge of the row address strobe and t_{RAH} seconds after it. Column address must be valid t_{ASC} seconds before, and t_{CAH} seconds after, the falling edge of the column address strobe.

Fig. 5 is t_{RCD}, the row to column strobe lead time. For the HM4864-2 the *minimum* value of t_{RCD} is quoted as 20ns, and the *maximum* value as 50ns. These limiting values are not fundamental parameters of the memory – they are derived from other parameters. The minimum value is determined by the row address hold time plus the time taken for the address from the multiplexer to settle. The maximum value is a pseudo-maximum. It is not a maximum determined by the device, but a maximum which, if exceeded operationally, extends the access time of the memory (see later).

My favourite apocryphal comment on dynamic memory is "What's the difference between static ram and dynamic ram? Static ram works and dynamic ram doesn't" (L. T. Hauck, Byte, July 1978), though perhaps the answer should have been "Static memory works on its own – dynamic memory has to be made to work for you".

Timing parameters vary between nominally equivalent devices from different manufacturers. This variation is sometimes larger than that in the parameters of static memory components. Table 1 provides some indication of the variations. A consequence is that dynamic memory components of equal size and nominally equivalent access times are not necessarily inter-

Fig. 6. In a read cycle, data becomes valid not more than t_{CAC} seconds after the falling edge of $\overline{CAS}$ and not more than t_{RAC} seconds after the falling edge of $\overline{RAS}$. At the end of the cycle, the data bus buffer is turned off no later than t_{OFF} seconds after the rising edge of the first of $\overline{RAS}$ or $\overline{CAS}$.



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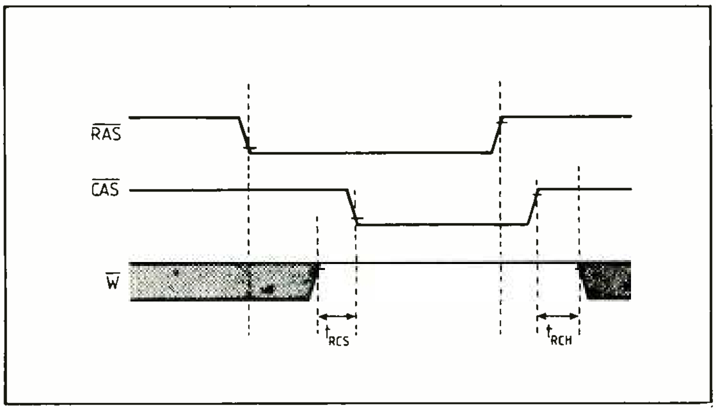


Fig. 7. In a read cycle, there are no complex restrictions on the $\overline{W}$ (write enable) input. It must be high at least t_{RCS} seconds before the falling edge of $\overline{CAS}$ and remain high until after the rising edge of $\overline{CAS}$.

Typical time values (ns)

t_{ASC}	col address hold	20-50
t_{ASR}	row address setup	0
t_{CAC}	access time from $\overline{CAS}$	100
t_{CAH}	col address hold	45
t_{CAS}	col address strobe pulse width	100-10µs
t_{CRP}	col-to-row strobe precharge time	20
t_{CSH}	$\overline{CAS}$ hold time	150
t_{OFF}	output buffer turn-off time	0-40
t_{RAC}	access time from $\overline{RAS}$	150
t_{RAH}	row address hold	20
t_{RAS}	row address strobe pulse width	150-10µ
t_{RC}	random access cycle	270
t_{RCD}	row-to-col strobe lead time	20-50
t_{RCS}	read command setup	0
t_{RCH}	read command hold	0
t_{RP}	row address strobe precharge time	100
t_{RSH}	$\overline{RAS}$ hold time	100

changeable in any particular memory system.

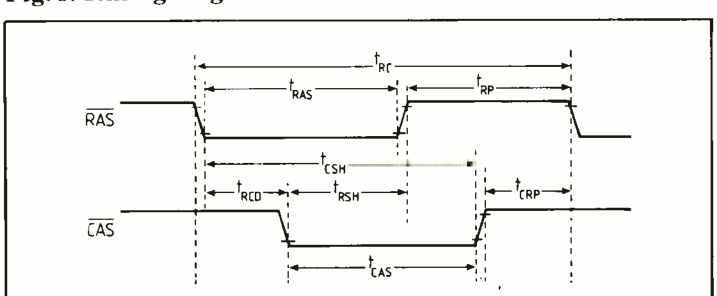
Data timing

Having latched an address in the chip, data appears at the data-out pin as depicted in Fig. 6, in which only $\overline{RAS}$, $\overline{CAS}$ and the data-out signals have been included for clarity. It is assumed that the address set up and hold times, and all other relevant parameters have been satisfied.

Data at D-out is valid no later than t_{RAC}, the access time from row address strobe, following the falling edge of $\overline{RAS}$. This is, of course, the quoted access time of the chip and is 150ns for a HM4864-2. However, in the world of the dynamic ram, all is not so simple. The row access time is achieved only if other conditions are met, as we shall see.

The column address strobe has two functions: it latches the column address which interrogates the appropriate column of the memory array, and turns on the data output buffers. For these reasons, data is not available for at least t_{CAC}, the access time from $\overline{CAS}$ low, after the falling edge of $\overline{CAS}$. The maximum value of t_{CAC} is 100ns. In other words, reading

Fig. 8. Timing diagram of $\overline{RAS}$ and $\overline{CAS}$ strobes.



data is a two-part process: accessing the memory cell and placing the data on the chip's D-out pin. The following two examples should make this distinction clear.

Suppose $\overline{CAS}$ goes low at the minimum time after the falling edge of $\overline{RAS}$ (ie t_{RCD} = 20ns), data will appear at the data-out pin no later than $t_{RCD} + t_{CAC}$ = 20ns + 100ns = 120ns later. At this time, the data is not guaranteed to be valid, as the minimum value of t_{RAC} (ie 150ns) has not been met. However, once t_{RAC} has been satisfied, the data will be valid.

Now suppose the falling edge of $\overline{CAS}$ is delayed beyond the maximum quoted value of t_{RCD}. Say that $\overline{CAS}$ is asserted 100ns after $\overline{RAS}$. The data will not be valid until $t_{RCD} + t_{CAC}$ = 100 + 200ns =200ns later, which value exceeds t_{RAC} by 50ns.

Now you can see why the maximum value of t_{RCD} given in the data sheets of dynamic rams is pseudomaximum. It is not a maximum determined by the memory, but a limit which if it is exceeded operationally throws away access time. There is little point in buying and expensive 150ns chip and then limiting its access time to 250ns by a careless design which exceeds $t_{RCD(max)}$. The relationship between $t_{RCD(max)}$, t_{RAC} and t_{CAC} is:

$$t_{RCD(max)} = t_{RAC} - t_{CAC}.$$

At the end of a read cycle when $\overline{CAS}$ goes high, the data bus drivers are turned off and the bus floats t_{OFF} (output buffer turn-off delay) seconds later. The maximum value of t_{OFF} is 40ns. Note that $\overline{RAS}$ does not play any part in the ending of a read (or write) cycle. $\overline{RAS}$ may be negated before or after $\overline{CAS}$, as long as its timing requirements are met.

$\overline{W}$ timing. The Diagram of the $\overline{W}$ input to the dynamic memory, Fig. 7, is very simple and shows that $\overline{W}$ must be high at least t_{RCS} seconds before the falling edge of $\overline{CAS}$ and remain high until at least t_{RCH} seconds after the rising edge of $\overline{CAS}$. Both t_{RCS} and t_{RCH} are quoted as zero minimum, which means that $\overline{W}$ must be high for a read cycle the entire time that $\overline{CAS}$ is low.

$\overline{RAS}$ and $\overline{CAS}$ timing. The final part of the read cycle timing diagram, given in Fig. 8, concerns the timing requirements of the row and column address strobes. The $\overline{RAS}$ and $\overline{CAS}$ clocks are responsible for controlling several internal operations within the chip, as well as the more mundane tasks of latching addresses and controlling tri-state buffers. Although Fig. 8 looks relatively complex with its eight timing parameters, it is entirely straightforward, and there are no critical parameters leading to engineering difficulties, as in the case of the $\overline{RAS}$, $\overline{CAS}$ and address multiplex timing in Fig. 5. Basically, Fig. 8 illustrates the maximum and minimum times for which $\overline{RAS}$ and $\overline{CAS}$ must be high and low, and the relationship between them.

A fundamental parameter of Fig. 8 is the read cycle time, the minimum time which must elapse between successive memory cycles. This is quoted as 270ns for the HM4864-2, which has a 150ns read access time. The corollary of these figures is that the cycle time must be taken into account when designing memory systems. For example, if a microprocessor had a 250ns cycle time, this dynamic ram could not be relied upon, even if its 150ns read access time were more than adequate. Interestingly, the value of 270ns for t_{RC} is the minimum value necessary for reliable operation over the device's full temperature range of 0°C to 70°C. If the ambient temperatures were guaranteed to be always lower than 70°C, the value of t_{RC} would be improved as the device slows with increasing temperature.

The $\overline{RAS}$ clock must be asserted for at least t_{RAS} seconds (the row address strobe pulse width) during each read access. This has a minimum value of 150ns and a maximum value of 10µs. The maximum value is related to the need to refresh the device and creates no problems, as it is many times longer than a processor read cycle. The only danger in a 68000 system would arise if $\overline{DTACK}$ were not asserted in a read cycle, and the processor hung-up with $\overline{RAS}$ held low. This situation is normally avoided by asserting $\overline{BERR}$ after a suitable time-out.

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TABLE 1. Address timing parameters of three 150ns 64K × 1 drams

Parameter	MCM6665A-15		TMS4164-15		MB 8264-15	
Row address setup time	t_{ASR}	0ns min	tsu(RA)	0	t_{ASR}	0ns min
Row address hold time	t_{RAH}	20ns min	th(RA)	20	t_{RAH}	15ns min
Column address setup time	t_{ASC}	0ns min	tsu(CA)	−5	t_{ASC}	0ns min
Column address hold time	t_{CAH}	35ns min	th(CLCA)	45	t_{CAH}	45ns min
$\overline{RAS}$ to $\overline{CAS}$ delay	t_{RCD}	30-75ns	t_{RLCL}	20-50	t_{RCD}	25-50ns

After $\overline{RAS}$ has been negated, it must remain high for at least t_{RP} seconds, the row address strobe precharge time. The precharge time is a characteristic of dynamic memories and relates to an operation internal to the chip. The minimum value of t_{RP} is 100ns and no maximum value is specified, subject to the constraint that the memory needs periodically refreshing. The final constraint on the timing of $\overline{RAS}$ is its hold time with respect to $\overline{CAS}$, t_{RSH}. $\overline{RAS}$ must remain low for at least t_{RSH} seconds after $\overline{CAS}$ has been asserted. The $\overline{RAS}$ hold time is quoted as a minimum of 100ns.

The column address strobe timing requirements are analagous to those of the row address strobe. $\overline{CAS}$ must be asserted for no less than t_{CAS} seconds (100ns), it must be negated for at least t_{CRP} seconds (−20ns) before the falling edge of the next $\overline{RAS}$ clock, and it must be asserted for at least t_{CSH} seconds (150ns) measured from the falling edge of the current $\overline{RAS}$ clock. (−20ns for t_{CRP} indicates that $\overline{CAS}$ may rise up to 20ns after $\overline{RAS}$ has fallen in the next cycle).

The full timing diagram of a HM4864-2 dynamic memory is given in Fig. 9 so that all the points discussed so far may be related to each other.

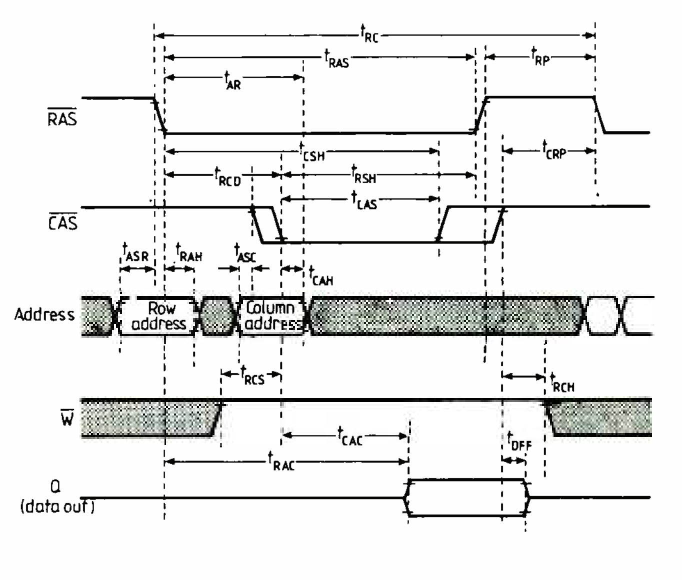
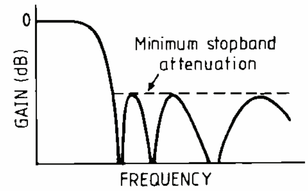


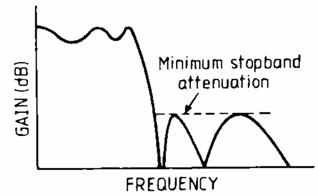
Fig. 9. Full timing diagram of a dymanic rame in a read cycle.

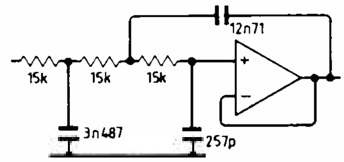
To be continued

Low-pass filters

In Tom Scharf's June article, three drawings became detached from page 22, Figs 9, 10 and 13:







On page 21, in the formula for attenuation, the frequency term should be raised to the power 2n.

Relativity simplified

We greatly regret the transposition of text that occured in M.H. Butterfield's article in June's issue, page 41. The section starting with equation 2 through equation 6 to the paragraph ending "It is not the case that clocks are going both faster and slower" should appear prior to the third paragraph in column 2, following "According to Newton, force is rate of change of momentum, so . . ." (Incidentally, equations 3 are referred to as 3a and 3b in the text.) Readers are welcome to a photocopy of a correctly laid out version.

Books

Spread Spectrum in Communication by R. Skaug and J. F. Hjelmstad. Peter Peregrinus Ltd on behalf of the Institution of Electrical Engineers; £28 in the UK, £32 elsewhere, 201 pages, hard covers. Frequency-hopping radio techniques: how they work, their pros and cons, and how to put together a system. Emphasis is largely on military systems, reflecting the background of the Norwegian authors.

Introducing C by Boris Allan. Collins, 184 pages, soft covers, £9.95. C is the most widely-used language for writing systems software. Using many practical examples, the author looks at both programming technique and the workings of the language itself. Appendices deal with BCPL (the precursor of C) and the Unix operating system.

A First Class Job by Joan Long. Published by the author, 210 pages, soft covers, ISBN 0 9511208 0 8: available by mail at £5.95 plus 50p inland postage from Greenleas, 5c Weybourne Road, Sheringham, Norfolk NR26 8HF. Biography by his daughter of Frank Murphy – radio pioneer, industrialist and self-taught philosopher, who after a dramatic rise to fame between the wars was to die in obscurity abroad. This unusual man's story has plenty to interest the vintage radio enthusiast (the book reproduces many of Murphy's famous advertisements), but there is much else for art and social historians. It's probably risky to draw parallels, but the man comes over as very much the Clive Sinclair of his day.

Choosing and Using CMOS edited by M.J. Walsh. Collins, hard covers, 304 pages, £25. Contributions from a variety of authors (mostly British) examine c-mos technology from both the manufacturer's and the user's point of view. Chapters cover s.s.i. design, gate arrays, analogue techniques, microprocessors and future prospects for c-mos. Two practical case studies, a gate array and a custom i.c., are included.

Videotex Europa – Basel 85, Proceedings of last September's internal conference; from Alphaville AG, Basel, Switzerland. Nearly 70 papers and other contributions, mainly in German, on all aspects of viewdata and teletext technology.

Oscilloscopes: how to use them, how they work (second edition) by Ian Hickman. Newnes Technical Books, 124 pages, soft covers, £5.50. Up-to-date guide for the student, hobbyist or technician. Very readable. Text and pictures cover the latest and cleverest 'scopes as well as basic types. An appendix lists sources of models on the UK market.

Industrial Control Handbook, volume 1 (of 3) – Transducers, by E.A. Parr. Collins, 286 pages, hard covers, £20. Textbook with a practical slant, for the student or working engineer. Author has aimed to keep the maths to a minimum in the interests of readability, with attractive results. The first volume deals with measurement of quantities and examines some of the commercial devices available.

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Digital signal processing

A further endorsement of the attractions of using general-purpose, consumer-type, signal-processing integrated circuits in high-grade h.f. communications receivers can be found in a report by A.P. Cheer of Plessey. Using a current PRS2280 receiver with digital interface, channel filtering and demodulation boards, using Texas Instruments TMS 32010 d.s.p. devices, the work has shown that two boards of digital electronics with a component cost (one off, quantity price) of £250, can replace £400 of analogue components (including crystal filters) yet providing essentially the same performance.

Although Rockwell-Collins began production of an h.f. receiver using d.s.p. last year (Model HF 2050) there have been no previous reports of UK companies in a position to put a digital radio into the production cycle, although it is clear that a lot of R & D is going on in this area.

A.P. Cheer claims that Plessey is "already in a position to develop a cost-effective standard i.f. transceiver i.c. module which could have wide application in a variety of fields. But the real competitive edge will be achieved in the future with the realisation of a full custom chipset which would give an ultimately lower unit price and increase the performance to a level where the complete all-digital transceiver system would become a reality."

The experimental model digitizes the signal at an i.f. of 1.4 MHz with data reduction to 40 Kw/s. With 12-bit d-a converters the dynamic range of the processors is limited to about 72dB. To cater for the various modes, the demodulator and filters act under software control.

Ultra fast data

The failure of the first launch of the new Ariane 2 rocket carrying Intelsat V, F-14, due apparently to a failure of the liquid hydrogen/liquid oxygen third stage motor, follows hard on the Shuttle disaster and the failures of Titan and Delta launches. While the technical problems may be solved in a matter of weeks or months the effects on launch and payload insurance could prove of longer term consequence. It is already impossible to obtain full cover for a launch and payload, and premiums for partial coverage can be as high as 20 to 30 per cent compared to around 10 per cent before the 1984 crop of mishaps. It will add to the interest in the trans-atlantic optical-fibre "cables" TAT8 (1.3 μm) due in mid-1988 and the proposed TAT9 (1.5 μm) for 1991. Satellites, despite their time-delay problems for two-way telephones, are operationally much more flexible in providing many possible routes via a single satellite. But optical fibres could emerge as the most reliable and cost-effective broadband system for linking main traffic centres, though the long-term reliability of submerged laser repeaters remains something of an unknown quantity.

The fantastic capacity of optical fibres is underlined by the recent successful experiment by AT&T Bell Laboratories in demonstrating for the first time digital transmission at a rate of no less than 8 Gbit/s through a single-mode optical fibre over a distance of 30 km, using a directly modulated 1.31 μm multi-longitudinal-mode laser. This is over a thousand times faster than the data rate of broadcast teletext.

C.F. Jenkins and early television

A detailed account of the early work of film and mechanical television pioneer Charles Francis Jenkins has been published in the *SMPTE Journal* (February 1986) by Albert Abramson, who has previously published a number of books on the development of electronic television. Abramson believes that Jenkins, who founded the Society of Motion Picture Engineers 70 years ago in July 1916, was responsible for many advances in the early days of television for which he is seldom given credit. In the early 1920s he was the only person seriously working on tv development in the USA. Although his early work provided little more than crude silhouettes there can be little doubt that his experimental apparatus was constructed to a standard far superior to that of J.L. Baird who appears, in effect, to have been following in the footsteps of Jenkins' "radiovision". While Abramson is careful to avoid entering into the controversy surrounding Baird's claims and demonstrations, there can be little doubt that as early as June 14, 1925 Jenkins publicly demonstrated his ability to transmit his low-definition images over a distance of five miles by radio transmission. Although Baird tried to convey the impression that he used a radio link, even between adjacent rooms, and later used his experimental licences 2TV and 2TW, all the evidence suggests that the first time Baird's signals were actually transmitted by radio was about July 1927 when he persuaded H.L. Kirke of the BBC to let him use, unofficially, a BBC medium-wave transmitter. This was soon stopped, following Post Office intervention. It was not until about February 1928 that Baird's signals were radiated on about 7 MHz from Ben Clapp's amateur-experimental station 2KZ at Coulsdon, leading to the much-publicized transatlantic tests.

Abramson lists some 90 US (patents for tv developments filed by Jenkins between March 1922 and March 1928 including US Patent No. 1,544,156 "Transmitting pictures by wireless", filed March 13, 1922 and issued June 30, 1925, which was based on scanning using two rotating prismatic rings. As Abramson puts it: "His contribution to the infant art of television is on the record. He was the first American television pioneer. He not only dreamed up a workable system, he designed, built and operated it. This the true test of a genius".

But Jenkins suffered from the fact that pioneering seldom pays. His company ran into financial difficulties in the American depression of 1929. He also stubbornly believed too long in the value of silhouettes when others had followed Baird into half-tone images. Jenkins Television, like De Forest Radio, went bankrupt. Many of Jenkin's pending patents were acquired in 1930 by RCA, who had by then embarked on an ambitious programme to develop electronic tv under Dr V.K. Zworykin. That Jenkins was much more than just a crude experimenter is amply illustrated in the SMPTE paper, showing early apparatus beautifully constructed.

Creativity

A study carried out in the USA by Teresa Amabile and the Center for Creative Leadership, based on more than 100 interviews with engineers and middle managers (reported in *IEEE Spectrum*) suggests that in a working environment there are five major stimulants to technical creativity, in descending order:

(1) freedom in deciding how to conduct one's work.
(2) good project management, including the setting of clear project goals, matching talents and interests to the task, protecting employees from unnecessary distractions and time-wasting activities, and maintaining clear channels of formal and informal communication within and among work groups.
(3) sufficient resources including funding and equipment.
(4) management enthusiasm for, and commitment to, a research idea and the encouragement of risk taking.
(5) A supportive organization.

Teresa Amabile similarly lists obstacles to successful creativity. Most important: "restriction of freedom and lack of autonomy, choice and self-direction". Other disincentives include excessive red tape, poor internal communication, lack of organizational commitment to innovation, lack of resources, undue pressure due to extremely tight deadlines involving too much work in too short a time.

The problem, she suggests,

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is to persuade managers to let people work on things they are enthusiastic about, and challenged by, rather than just letting people drift, and then to allow them freedom in deciding how to tackle the project.

One wonders just how well UK electronic firms and organizations would score in such a survey.

Polarization diversity

Experiments at Bell Communications Research Laboratories in New Jersey have shown that short-distance communications links at frequencies around 800 MHz can be usefully protected against multipath reflection and handset orientation by the use of polarization diversity. The work included paths within, or partly within buildings, and also mobile operation.

To measure the correlation coefficient of two orthogonally polarized signals, the two ouputs from a dual-polarized microstrip patch antenna were fed to two spectrum analyzers used as tunable recivers. It was found that under non-line-of-sight conditions, where deep fading occurs with a portable communications, signal impairments can be usefully mitigated by polarization diversity. This avoids the use of multiple frequencies for frequency diversity and the separation distance of space diversity. The cross-polarization antennas can be positioned directly on top of one another.

Loop applicator

The June *C.C.* described the use of the inductively-fed h.f. transmitting antennas based on the "miniloop" system originally patented by J.H. Dunlay.

A basically similar system has been developed by R.H. Johnson of the Wolfson R.F. Engineering Centre, Royal Military College of Science, as a diathermy applicator ("New type of compact electromagnetic applicator for hyperthermia in the treatment of cancer", *Electronic Letters*, Vol.22, No. 11, 22 May 1986, pp. 591-3). In effect, a tunable resonant loop, with variable tuning capacitor, inductively fed from a smaller loop, is formed from flat plates, the entire assembly being contained in screening box having one side, placed on the patient, covered with a low-loss dielectric. This form of applicator (patent applied for) can be used at 22, 27, 200, 400 and 900 MHz, with a physical dimension for 22 MHz being reduced by filling the unit with liquid having a relative permittivity of 2.3. It is claimed that this form of lightweight low-cost applicator has dimensions which can be made virtually independent of frequency, enabling the heated area of tissue to coincide with the treatment site. Field penetration is comparable with conventional, heavier applications of the same aperture dimensions.

The major problems for hyperthermia treatment appears to lie in concentrating power on deep-seated tumours without overheating tissue near the skin. R.H. Johnson claims that his design should also be effective in multiple arrays and could be useful in physiotherapy.

Amateur cryptology

The UK amateur transmitting licence makes it clear that all messages must be in plain language and refer to matters of a personal nature, in which the licensee or the person with whom he or she is in contact has been directly concerned and use signals (i.e. procedure signals) not in secret code or cipher. Anything resembling private codes and ciphers is expressly forbidden.

Nevertheless an increasing number of amateur and personal computer enthusiasts have become interested in the subject of cryptography and cryptanalysis. While initially much of the interest has been concentrated on devising software programs for enciphering and deciphering relatively simple systems, some enthusiasts, particularly in North America, seem prepared to tackle anything less than "computationally secure" ciphers.

Mike Barlow, ex-G3CVO, a founder member of the British Amateur Television Club but for many years resident in Canada as a tv engineer with CBC, has recently launched a "Computer Supplement" newsletter is association with *The Cryptogram* bulletin of the American Cryptogram Association with the first issue including his "TRS80 programs for grille encipherment and decipherment" and with an extensive bibliography on the use of computers in cryptography. The supplement is sent to all members of ACA. (Annual subscription $15 – ACA, 12317 Dalewood Drive, Wheaton, MD 20902, USA)

Mike Barlow mentions that several British amateurs are known to be actively interested in computer cryptography and have shown their ability to solve problems set in issues of *The Crytopgram*. He acts as the computer specialist for the ACA, most members of which still tackle ciphers with pencil and paper rather than with computers. His address is 5052 Chestnut Avenue, Pierrefonds, Quebec, H8Z 2A8, Canada.

The professionals in this field still seem to be locked in debate about the security of such systems as the Americans DES and British B-Crypt. In the USA the National Security Agency (counterpart of British GCHQ) has begun taking a more active role in developing improved systems for commercial users as well as for the Armed Services, partly to offset the many recorded "successes" of the "hackers" equipped with microcomputers. NAS no longer approve the use of DES with its ten-year old IBM-developed 64-bit "key" but instead licences approved companies to manufacture and market chips for NSA's own "Comsec" systems. While manufacturing companies can supply information on chips and modules, to obtain applications information and sample chips needs NSA prior approval. A problem is that the market for specialized encryption chips is relatively small, with some 80,000 DES i.cs sold in 1984. The cost of providing good communications security to a personal computer can amount to $1000.

Although some forms of "public key" cryptosystems (which remove many of the problems of key managment) have been shown to be vulnerable, the RSA (Rivest, Shamir and Adelman) system of the late 1970s still appears to be entirely secure against any imaginable computer attack. Its use however has been limited by the relatively slow speed of encipherment and decipherment, ruling out its use for speech. A new quadratic form of public key cryptosystem, much faster than RSA, but which similarly derives its security from the inability of computers of factorize rapidly, has been proposed by T. Okamoto of NTT, Japan. (*Electronics Letters*, 22 May 1986). Public-key cryptosystems offer the added advantage of providing "authentication" (electronic "signature") to messages. But although encipherment can protect data and messages during transmission, it provides no protection against "humint" (human intelligence) – and it is often cheaper to suborn those who handle messages in "plaintext" than to attack enciphered traffic with large mainframe computers.

In brief

In some remote areas, illegal "high-power" cordless telephones are being increasingly used over distances of several miles.

A detailed synopsis, data sheet for Si8901 ring demodulator/balanced mixer and an application note for Ed Oxner's new commutation double-balanced mosfet mixer of high dynamic range (using resonant-gate drive) is available as a 16-page publication "Designing a super-high dynamic range double-balanced mixer" from Siliconix Ltd, Publicity Department, Morriston, Swansea SA6 6NE.

PAT HAWKER, G3VA

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by P.E.K. Donaldson

Frequency – hopping in r.f. energy-transfer links

The effect of coupling coefficient on frequency in self-oscillating transmitters

P.E.K. Donaldson was born in 1927 and educated at the Royal Naval College, Dartmouth and Cambridge University. He served in the Royal Navy from 1941 to 1952 and was Technical Officer at the Physiological Laboratory, Cambridge University between 1953 and 1967. He has been on the engineering staff of the Medical Research Council Neurological Prostheses Unit since 1968, and has contributed occasionally to *Wireless World* since 1963.

Radio frequency links, in which a receiver coil operates in the near magnetic field of an opposed transmitting coil, provide a useful technique for 'throwing' energy across a physical gap. In our Unit their application is in powering microelectronic implants from a transmitter attached to the surface of a patient's body[1,2,3]. More familiar uses include d.c.-d.c. transformers for voltage-changing, d.c.-d.c. transformers for level shifting, and couplers of radio transmitters to their resonant aerials.

Starting from the simple circuit of Fig. 1, for which the equation is just $E_2=\omega MI_1$, we see at once the value of using radio frequency: by making ω large enough, we can obtain a useful output E_2 with small M; and since $M=k\ (L_1L_2)^{0.5}$, this means we can have both small coupling coefficient k (large 'throw') and robust windings of a few thick turns for L_1 and L_2.

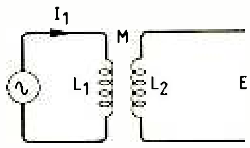

Fig. 1. Radio-frequency link in the form of a loosely coupled transformer

Because the coupling is loose, most of L_1 and L_2 will be leakage inductance, rather than coupled. The arrangement is more realistically portrayed in Fig.2. We might as well place capacitors in series with L_1 and L_2 to tune out most or all of that useless leakage inductance. Adding a load, we arrive at Fig. 3; and transforming the series-resonant circuits to their shunt equivalents, adding some rectification and filtering in the secondary circuit, and putting in a Hartley set-up for the generator, we come to the familiar arrangement of Fig. 4, in which a self-oscillating transmitter is used rather than the more complicated master oscillator/power amplifier.

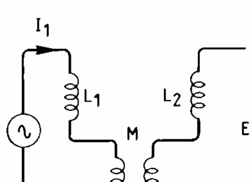

Fig. 2. Much of the inductance in Fig. 1 is leakage-uncoupled-inductance.

Anyone who has ever experimented with this arrangement, or its valve equivalent, knows that it behaves quite sensibly so long as k remains small. Beyond a certain degree of coupling, however, strange things begin to happen. V_0 may change discontinuously to a new value with varying k, or with varying V_1, or with the passage of time. If the reserve loop gain of the oscillator is insufficient, oscillation may cease altogether. Since the efficiency of energy transfer rises as the coupling is made tighter, it is important to understand what sets an upper limit to k. The subject was of great interest 50 or 60 years ago, when amateurs had to get the maximum power into the aerials of one-valve transmitters. More recently, little or nothing seems to have been written about it. A morning spent browsing in the IEE library turned up one terse mathematical treatment[4] dating from 1972. It seemed to me, therefore, that the subject could stand reiteration.

Stable oscillation

Consider first a series-resonant self-oscillating circuit, represented in essentials in Fig. 5. Above resonance, the tuned circuit looks inductive and so the current lags the voltage. At resonance the tuned circuit will look like a small resistance; current will be in phase with the voltage. Below resonance it will look capacitative and the current will lead the voltage. If the circuit is oscillating and the frequency were for some reason to try to rise, the phase of the feedback signal, which is the phase of the current, would become lagging, lowering the frequency of oscillation again. And vice-versa. We see that the condition for stable oscillation in a series oscillator is that the tuned circuit reactance becomes increasingly inductive with rising frequency; or, taking inductive reactance as positive, $dX/d\omega$ is positive when $X=0$.

Consider now the shunt-resonant self-oscillating circuit (Fig. 6). Above resonance, the tuned circuit looks capacitative, and the voltage therefore lags the current. At resonance, the tuned circuit looks like a high resistance and the voltage will be in phase with the current. Below resonance, it will look inductive and the voltage will lead the current. If the circuit is oscillating and the frequency were for some reason to try to rise, the phase of the feedback, which is the phase of the voltage, would become lagging, lowering the frequency of oscillation again. And vice-versa. We see that the condition for stable oscillation in a shunt oscillator is that the tuned circuit reactance becomes increasingly negative with rising frequency; or, that $Dx/d\omega$ is negative when $X=0$.

Introduction of secondary circuit: series oscillator.

Suppose now a secondary circuit, tuned to the same frequency as the primary, is brought up to the series oscilla-

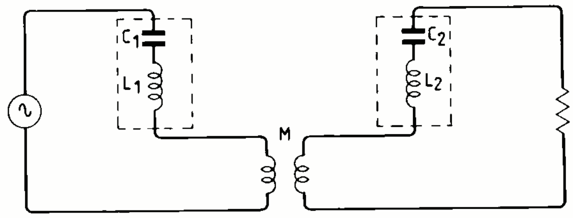

Fig. 3. Fig. 2, with capacitors to tune out the leakage inductance, and a resistive load.

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tor (Fig. 7). To the primary impedance

$$Z=R_1+jX=R+j(X_{L1}-X_{C1})$$

must be added the coupled impedance

$$\frac{\omega^2M^2}{j(X_{L2}-X_{C2})+R_2}$$

To simplify things a bit, let $L_1=L_2=L$, $C_1=C_2=C$. Then

$$\omega^2M^2=k^2\times X_L^{\,2}$$

and

$$X=(X_L-X_C)-\frac{k^2X_L^{\,2}(X_L-X_C)}{R_2^{\,2}+(X_L-X_C)^2}\quad(1)$$

$dX/d\omega$ is obviously positive for small k. To find where, if anywhere, it ceases to be positive, differentiate (1) with respect to ω and equate to zero. At the frequency ω_0 where $X_L=X_C$,

$$\left(L+\frac{1}{C\omega^2}\right)\left(1-\frac{k^2X_L^{\,2}}{R_2^{\,2}}\right)=0$$

and writing Q_2 for X_L/R_2, $k.Q_2=1$, an important result. Figure 8 sketches the way X varies with ω for three values of k. When k=0, $dX/d\omega$ is everywhere positive and the oscillator runs stably. When k reaches $1/Q_2$, $dX/d\omega=0$ when X=0 and the stability is neutral. When $k>1/Q_2$, oscillation at ω_0 is in unstable equilibrium. The slightest perturbation in ω will lead, not to restoration to ω_0, but to movement away from ω_0. The frequency will 'hop' to one of two new stable values ω_1,ω_2.

Introduction of secondary circuit: shunt oscillator.

We assume again that $L_1=L_2=L$ and $C_1=C_2=C$. In the absence of the secondary circuit, the primary reactance is

$$X=-\frac{L}{C}\left\{\frac{R_1^{\,2}/X_L+(X_L-X_C)}{R_1^{\,2}+(X_L-X_C)^2}\right\}\quad(2)$$

On bringing up the secondary circuit (Fig. 9), equation (2) has to be modified by subtracting from X_L, in two of the three places where it occurs, the coupled reactance term. That is, replace X_L by

$$X_L-\frac{k^2X_L^{\,2}(X_L-X_C)}{(X_L/Q_2)^2+(X_L-X_C)^2}\quad(3)$$

There is little point in battling to substitute (3) into (2). X is easily evaluated, for a few interesting cases, on a microcomputer, and varies as is sketched in Fig. 10. At k=0, $dX/d\omega$ is negative in the region of ω_0 and oscillation is stable. As in the series case, $dX/d\omega$ becomes zero at ω_0 when $k=1/Q_2$ but in theory, oscillation is still stable because there is still one frequency only, ω_3, where X=0, and at ω_3, $dX/d\omega$ is still negative. Marginal stability is reached at $k=k_2$, and at $k=k_3$ frequency hops become possible, between ω_1 and ω_2.

In practice, the phase shift in the rest of the oscillator may not be exactly π;, oscillation will still occur, but at some frequency at which X is not equal to zero, so that some of the total 2π loop phase shift of the oscillator has to come from the tuned circuit. So, although it is strictly possible to have stable shunt oscillation when $k>1/Q_2$, it is probably unwise to try to achieve it. It is safer to keep $k<1/Q_2$ as a criterion for the avoidance of frequency-hopping in both shunt and series configurations.

Implications for link design

When r.f. links are used to 'throw' energy to a surgically-implanted device, there is often some uncertainty about the working distance between transmitting and receiving coil. The former may not be attached to the skin in quite the right place. Even if it is, there may be a good deal of relative movement between the external and the implanted device with the patient's body movements. It is helpful if the

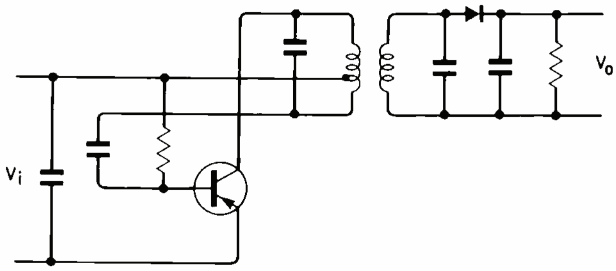

Fig. 4. Fig. 3 developed into a self-oscillating transmitter/receiver with a direct-current output.

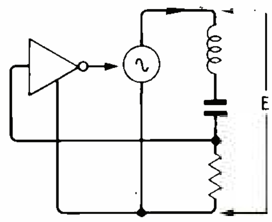

Fig. 5. Skeleton series-resonant self-oscillator in one possible form. The resistor would be a very low-value component, just enough to develop a useful feedback signal in phase with the current.

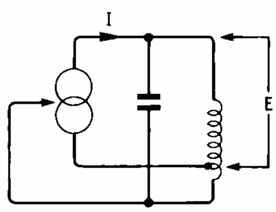

Fig. 6. Skeleton shunt-resonant self-oscillator in Hartley form.

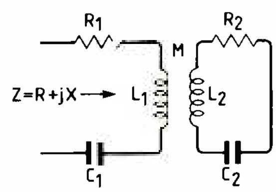

Fig. 7. Coupled circuits, series-resonant primary. R_1 and R_2 are the r.f. resistance of L_1 and L_2 respectively.

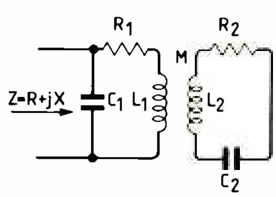

Fig. 9. Coupled circuits, Shunt-resonant primary. R_1 and R_2 are the r.f. resistance of L_1 and L_2 respectively.

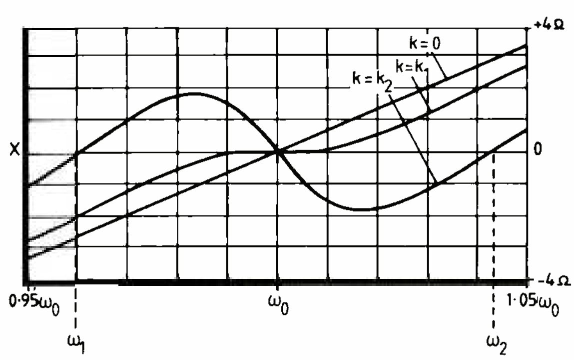

Fig. 8. Reactive part of the impedance seen looking in at the terminals in Fig. 7. In this example, $L=1\,\mu H$; $C=1\,nF$. $Q_1=10$; $Q_2=20$; $k_1=0.05$; $k_2=0.1$

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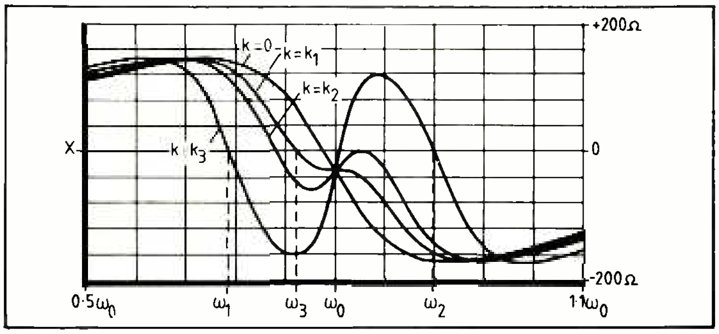

Fig. 10. Reactive part of the impedance seen looking in at the terminals in Fig. 9. Ls, Cs and Qs as for Fig. 8. k_1=0.05; K_2=0.065; k_3=0.1.

gain of the link can be made insensitive to changes in coupling coefficient, and a good way to achieve this is to seek to work at critical coupling [5]. At critical coupling the gain of the link is at a maximum, so that the rate of change of gain with coupling is zero.

A straightforward way to build a vice-free and rational r.f. link is to use a mopa transmitter, as described in reference 5. Vis-a-vis a simple Hartley or Colpitts, a mopa is more complicated, so more fault-prone and more expensive; it has two, possibly three, tuning adjustments to set up; power must be provided for the m.o. and, where present, buffer stages; it is probably bulkier and therefore, if worn continuously under clothes, harder to conceal and less comfortable to wear. There is therefore good reason to use simple self-oscillating transmitters if frequency-hopping can be avoided.

Hop-free working

As we increase k from zero, we want to reach k_{crit}, where the link behaves well, before we reach $k_{closest}$ = $1/Q_2$, at which the link begins to behave badly. From the well-known expression $k^2_{crit}Q_1.Q_2 = 1$,

$$\frac{1}{\sqrt{Q_1Q_2}}<\frac{1}{Q_2}$$

where Q_1 is the unloaded circuit Q of the transmitter tuned circuit. Hence $Q_1>Q_2$.

If frequency-selectivity is unimportant, this inequality is easily met by damping the receiver tuned circuit, but the link gain and the 'throw' will be poor. Where selectivity is important, or where a good 'throw' (e.g. one coil diameter) is essential, there is no option but to make Q_2 about 30, and to make Q_1 even greater. These are circuit Q's, not device Q's; an interesting challenge for circuit designers.

References

1. Anon: "Artificial vision": *Wireless World*, May 1971: 214-217.
2. T.E. Ivall: "Artificial vision progresses": *Wireless World*, April 1975: 156-158.
3. T.E. Ivall: "Radio-activated implant for bladder control": *Electronics and Wireless World*, January 1984: 61-64.
4. J.H. Reyner and P.J. Reyner: Radio Communication. Chapter 2: 3rd edition, Pitman, London. 1972.
5. N. de N. Donaldson and T.E. Perkins:" Analysis of resonant coupled coils in the design of radio frequency links": *Med. Biol. Eng. & Compt.* 21 612-617 (1983).

BOOKS

1985 Satellite Directory, 7th annual edition. Phillips Publishing Inc., 7811 Montrose Road, Potomac, Maryland 20854, USA: 936 A4 pages, soft covers. Price to UK readers is $197 plus $25 for carriage; orders must be prepaid. Business guide to satellite communications, with the emphasis on the US domestic market. Extensive directory sections list (among others) system operators, equipment suppliers, trade associations, launch services, transponder brokers, research groups and educational institutions, technical and financial services and even communications lawyers. Tables show orbital positions of existing and planned US and Canadian satellites and summarize their technical characteristics.

Making Computers Talk by Ian H. Witten. Prentice-Hall, 150 pages, soft covers, £17.95. Introduction to speech synthesis, pitched at the technically-minded lay reader. Chapters explain how speech works and examine the various methods of producing it artificially, with their problems and pitfalls. An especially interesting section covers some commercial applications of speech synthesizers, among them the Kurzweil reading machine for the blind and a telephone enquiry service which responds to tones from a keypad. Clearly written and free of unecessary jargon.

Solar-Terrestrial Disturbances of June-September 1982: special issue of *Journal of the Radio Research Laboratory*. Ministry of Posts and Telecommunications, Nukui-Kitamachi, 4-chome, Koganei-shi, Tokyo 184, Japan; 315 pages. Fourteen papers covering aspects of this period, in which some remarkable solar events occurred during the descending phase of the cycle. Topics include geomagnetic disturbances, magnetospheric v.l.f. emissions, transequatorial ion whistlers, h.f. propagation disturbances, ionospheric scintillations of geostationary satellite waves, 50MHz auroral observations and more.

The Complete Wordwise Plus Handbook by Paul Beverley. Norwich Computer Services, 420 A5 pages, ring-bound. Available by post at £17.50 from NCS, Freepost, 31 Cattle Market Street, Norwich NR1 3BR. Wordwise Plus, the word-processor for the BBC microcomputer, is unusual in that it comes with a built-in Basic-like language for manipulating text. This book, based on material from the author's earlier publications but with much new information (and now with the imprimatur of Computer Concepts, producers of Wordwise Plus), offers a detailed guide to the possibilities of this powerful language. Among the many program listings are indexers, document formatters, sorters, a mail-merge program and a logger for recording scientific data. Other chapters provide solutions to a variety of common word-processing problems. Major programs are offered on disc at £7.50 extra.

Linear ICs (Thomson Semiconductors data book). From Hawke Electronics Distribution, 45 Hanworth Road, Sunbury-on-Thames, Middlesex TW16 5DA: 1006 A5 pages, soft covers, £12. Data sheets on most of Thomson's industrial and consumer i.cs, including second-sourced types. There are some useful cross-reference tables.

Microprocessor Sourcebook by George Loveday. Pitman Publishing, 247 large-format pages, soft covers, £9.95. Attractive handbook of microprocessor lore, presented in easy-to-scan A-Z format. Especially useful for the newcomer. Entries cover applications of microprocessors as well as their anatomy and physiology and include many useful tables and diagrams. Under M, the author lists principal families of microprocessors with their instruction sets and supplies an informative rundown on each.

Wallchart of frequency allocations

Corrections to the wallchart first issued in June 1986

* In column 1, 14-14.35MHz is an amateur allocation and should have been coloured pink.

* In column 8, 81-84MHz should have included a red band. These frequencies are not yet allocated in the UK but are earmarked by the ITU for the fixed, mobile, fixed-satellite and mobile-satellite services.

* The 1632-1792 assignment for cordless telephones is paired with 47.44-47.55MHz.

* Cross-hatched sections of the chart represent Government allocations.

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FEEDBACK

FREQUENCY ALLOCATIONS

I was rather alarmed to note from the wallchart of frequency allocations provided with your June edition that it is proposed to move the 200 kHz BBC Droitwich Service to 198 on 1st February, 1988.

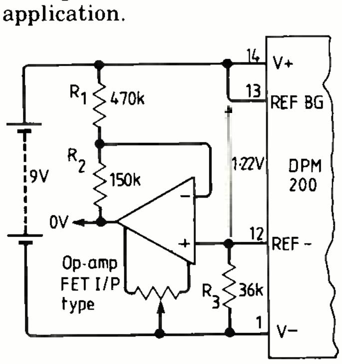
Many people like myself use off-air frequency standards based on the 200 kHz transmission, and these devices will become useless in 1988. I really wonder if the decision to move from 200 kHz has taken the widespread use of the transmission as a frequency standard into account.

H.D. Ford,
Richmond,
Surrey.

ALTIMETER

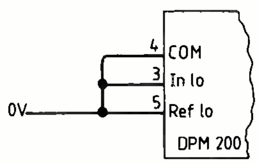
I read with interest Mr F. Ogden's altimeter article (June, 1986) in which he uses one of our DPM 200 panel meters. I would like to make some comments which may be of interest.

The temperature-stable supply can be improved by using the redundant band-gap reference diode on the meter. This device has a temperature coefficient of typically 50ppm/°C. Fig. 1 shows such an application.



The voltage between Ref BG and Ref− is 1.22V nominal. Resistors R_1 and R_2 should be low-drift types. The advantage of this circuit is that it avoids the temperature coefficient of D_5 and the V_{be} and H_{fe} coefficient of the BC212 transistor.

My second comment refers to the analogue inputs of the meter. The ground of the analogue section is COM (Pin 4). This is held by the meter at approximately 2.7 volts below V+. The common-mode rejection ratio of the inputs is 86dB (or 50μV per volt of common-mode voltage.) With In Lo at 5V below V+ there will exist 2.3V of common mode. This can cause 100μV or one count offset. To remove this, simply connect COM to 0V as in Fig. 2.



Although COM will sink a large amount of current to maintain its level below V+, it cannot source more than 10-20μA and can easily be pulled down to the lower potential.

My final comment concerns the use of silicone grease. Avoid grease coming into contact with the l.c.d., especially the conductive rubber connectors inside, as this may cause open circuits and thus missing segments.

Simon Wyre,
Technical Manager,
Lascar Electronics.

The author replies:

Mr Wyre's comments are most helpful. I fully endorse the circuit changes he suggests but would add that the slight improvement in temperature stability they produce is less than the inherent errors of silicon pressure transducers: hysteresis, scaling error, etc. This means that if you've built the original, there is little point in changing anything.

The point about silicone grease hadn't occurred to me. I used the heavy heatsink type which doesn't migrate. Silicone sprays might well give trouble.

BBC CUTBACKS

The silly season in the BBC seems to have started earlier than usual. In recent weeks there have been advertisements in the trade and national press for technical operators in the BBC's Engineering Department: recruitment is being done by an independent consultancy. At the same time this union is negotiating with the BBC on the Corporation's "priorities for the future" proposals. Those proposals, as originally tabled, included the decimation of the BBC's engineering specialists departments, the abolition of consultancy and cut backs in its central appointments and publicity departments. Substantial opposition to these proposals by this union means that the BBC have been forced to rethink their cuts strategy and as yet there have been no compulsory redundancies in the engineering specialists. However the future for at least 60 staff is still not secure. It is nonsensical that an organisation seeking to make cuts on the grounds of so-called efficiency should be negotiating post closures and voluntary redundancies at the same time as it seeks to recruit new staff.

Laura Vincent,
Asst. General Secretary,
Broadcasting and Entertainment Trades Alliance

XY PLOTTER

J. Jardine in his letter in May 1986 gives a line generation program for the XY plotter previously featured in this magazine.

If the motor control circuitry were to allow simultaneous movements in both X and Y directions, then we would have four possible diagonal movements as well as the four axial ones. Thus a combination of axial and diagonal steps would give a closer approximation to the true line.

I reproduce below another method of generating the next best step when plotting a straight line on a device capable of diagonal motion. It has the advantage of being more efficient than the previous method (a factor of 3 in Basic) and is very amenable to conversion to machine code. The program shown works in the first octant and outputs an 'A' when the next step is axial and 'D' when it is diagonal.

```
10 INPUT "INPUT X"; A
20 INPUT "INPUT Y"; B
30 S = −A
40 BMA2 = B−A+B−A : B2 = B+B
50 FOR I = 1 TO A
60 IF S < 0 THEN INC = B2 :
PRINT "A"; ELSE INC = BMA2
: PRINT "D";
70 S = S+INC
80 NEXT
```

I claim no credit for the method used; it is actually based on the Bresenham line generation algorithm[1] which has been around since 1965 and has been used by many commercially produced plotting devices. It is of course well suited to raster devices as well as incremental plotters.

Reference.

1. *IBM Systems Journal*, Vol. 4, No 1, 1965.

M. Eggleston,
University of Leeds

RELATIVITY

Professor Butterfield's analogy explaining time dilation (June issue) neglects the force accelerating the clock balance wheel round. If this were to decrease as $f = f \times (1-v^2/c^2)^{1/2}$ the clock would mark the table along which it travels at intervals predicted by $t = t/(1-v^2/c^2)^{1/2}$. An observer of these marks assumes that time dilates for an accelerated observer, when in fact clock rotation had slowed down for all observers, accelerated or not. Of course, Professor Butterfield will argue that table recoil due to its acceleration of the clock indicates an increase of mass; therefore a variable force with velocity cannot be true. In reality, as opposed to analogy, the table is an electron accelerator 1 mile long and rather massive regarding a relativistic recoil of 40 000 electron rest mass. It hardly moves at all, while electrons accelerate to velocity: thus ambiguous equations describe experimental effects. The best example of a velocity-dependent force is the precession of the DI Herculis orbits. Multiply the predicted result by a reciprocal of the "discrepancy" and you get the observed result (*New Scientist* 29 August 1985 "Double-star system defies relativity"). These stars have nearly equal mass, therefore transfer detectable relativistic mass, if any, one to the other. Apparently there is none by an

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exact amount namely $(2.34° + 1.93°) \times 0.15 = 0.64°$.
Michael Dobson,
Hampton,
Middlesex.

Professor Butterfield has set himself an impossible task. Relativity cannot be simplified; one of its basic postulates is wrong!

This wrong postulate (that the speed of light is the same to all Toms, Dicks and Harrys) leads to a famous but wrong conclusion that mass is energy.

Why, then, does Professor Butterfield *begin* his article with this crazy conclusion? By working backwards, you merely end up with Einstein's wrong postulate!

Physicists have had their minds boggled for decades by Einstein's nonsense; it's high time for de-boggling! It's bad enough having the old, old story of Einstein's nonsense dished out to us, forward-wise. Please don't give us the old, old story backwards.
A.H. Winterflood,
Muswell Hill,
London, N10.

Ezekiel had a vision of wheels arguing circularly around an axle of *presumption*, and so do I. Inertia is a quality of mass which prevents instantaneous change and causes it to happen through time.

Is it then a reasonable proposition to combine trad Newton with a new law that energy has inertia mass, and then to derive a spatially distributed single event which must be inertial mass?

Sorry, Prof.: back to the drawing board and invent the LSM, but please remember that you were not the first because it inhabits the space which Albert could not conceive to be empty.

While you are busy, accept the fact that we do not see what happens, but rather see a distorted vision of what happens which our dirty great egos *presume* to be the truth. When things move extremely quickly, the quickness of the hand deceives the eye and any other massive sensor.

Nor, Mr Burniston Brown, do I like Sachs' belief that Albert changed his mind: further evolution of the thing changed *him*. That is why I like Albert: he demonstrated an active intelligence.
James A. MacHarg,
Wooler,
Northumberland.

ELECTROLYTICS

I would like to answer both Mr Self and Mr Hall in order to remove any confusion about the capacitor test referred to in my previous letter. First, Mr. Hall is correct in asserting that the test is primarily measuring linear distortion. I have found the magnitude of the linear distortion in an electrolytic capacitor to be typically 500 times larger than the harmonic distortion measured under similar conditions. Should we just ignore the linear component, or should we at least consider it as a potential aberration that deserves closer scrutiny?

Mr Self's allegation that what is primarily measured in the capacitor differential test is due to film breakdown is inaccurate, as he is referring to non-linear distortion. It can also be shown that d.c. biasing a polar aluminium capacitor will not improve its measurement in this test.

Dielectric absorption (d.a.) in a capacitor can be simulated by adding parallel branches of series RC components[3]. This extended capacitor model can be shown to closely approximate the actual dielectric absorption. Therefore, one can add the appropriate RC branches to a nearly ideal capacitor and obtain an almost complete null when paired against a typical electrolytic capacitor in the differential capacitor test. Alternatively, in a computer simulation of the different capacitor test, one can model a non-ideal capacitor (with d.a.), paired against an ideal capacitor, and note the similarity of the output waveform to what is typically measured with the differential capacitor tester.

In conclusion, I again invite those who are interested, to try the test themselves. There is much more to be learnt about capacitor differences than has been published thus far. I still recommend the AD524 or equivalent IN-AMP for serious measurements in order to head off any potential criticism of measurement accuracy.
John Curl,
Lineage Corporation,
New York,
USA.

References

1. J.J. Curl, *WW*, "Letters", Nov., 1985
2. W. Jung and J. Curl, "If the Cap Fits", *Hi-Fi NEWS & Record Review*, April, 1986
3. R.A. Pease, National Semiconductor Corp., "Understand capacitor soakage to optimize analog systems", *EDN* Oct., 13, 1982.

I am sorry to have to disagree with Ben Duncan in public as I usually find his writings most entertaining. However, I found his views on The Great Capacitor Crisis more than a little obscure, and I fail to see how any of his points clarify the vexed question of whether or not a capacitor in normal audio use can cause audible problems.

It is obviously true that music signals are made up of harmonics, but these are in themselves sinusoidal, because that is how Fourier transforms work. Fourier transforms work that way because they are a mathematical expression of the behaviour of things in the real world. How Mr Duncan takes the next step in his reasoning, which is to say that musical waveforms are therefore accompanied by a varying d.c. component, I do not understand. No one denies that real waveforms are often markedly assymmetrical, but this is an assymmetry of the peak value of the signal, which is why professional peak – reading level meters invariably use full-wave rectification. The positive and negative peaks can vary by 8dB or more, particularly on speech. However, this has *nothing whatsoever* to do with the mean level of the signal, which almost by definition is centred on zero volts. This is always the case, unless a d.c. error exists in the circuitry, or some sort of really gross slew limiting, clipping, or suchlike is taking place.

A moment's thought will show that this must be true, because the bandwidth of the audio chain does not reach down to d.c. I submit that the barometic pressure in the recording studio is not a parameter that needs to be reproduced for the best subjective effect. In reality any acoustic signal will lose its d.c. level on encountering either the microphone, the guitar pickup, the tape machine, or the phono cartridge, all of which are quite incapable of passing on d.c. levels. As for the ill-fated bass driver, I suggest that simply excessive level or an amplifier d.c. fault accounts for its demise. Occam's razor is still as sharp as it ever was.

I resignedly repeat I accept that some capacitors, such as electrolytics, object strongly to having voltage changes impressed on them. In fact I demonstrated it myself in a previous letter,[1] though I pointed out at the time that the effect would never intrude on a properly designed circuit. I much appreciate Mr Duncan's invitation to 'offer my skills to the work' but I thought I already had, even if the results were not convenient for everyone; I do wish that someone else would join in on the problem from the measurement side. In fact, I suggest it is up to Mr. Duncan to show us exactly how his mysterious d.c. waverings are generated, specifying circuitry that does it and showing us diagrams of the relevant waveforms.

As for Mr Curl's capacitor tester, once again there seems to be a logical step missing. Nobody would deny that all capacitors possess series resistance and leakage to some degree, but the question is, how does this affect signals passing through it? The subjective effect has often been described, though sadly the reports contradict each other. Sometimes it is called 'compression', sometimes a 'a delayed echo of the original signal'. In no case can anyone provide a model of how such effects could be induced by any amount of e.s.r. or other defect. I can only hope that someone will produce an objectively testable hypothesis, so that the matter can be laid to a well-earned rest one way or the other.

Finally, back to the furtive practice of gold flashing. If I interpret Mr Duncan's position on this one correctly, it is that non-noble contacts suffer a sort of continuous high-speed unreliability of connection, rather like drop-outs on poor quality tape. This one can surely be simply checked with a storage oscilloscope; I could find no trace of such an effect with the grottiest connectors I could lay my hands on. For readers having a distortion analyser handy, it is instructive to try all sorts of duff contacts in an attempt to induce even tiny levels of distortion into the signal. It is quite surprisingly difficult. Am I really the only one that actually tries this sort of thing, as opposed to theorising about it?
D.R.G. Self,
Bow,
London E3.

Reference

1. Self, D. 'Feedback', *Wireless World*, February 1986, p43.

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Waveform recorder interface

by P.B. Unstead
and A. Blunden
North East London
Polytechnic

This analogue interface, suitable for the Apple II and other 6502 machines, can also act as a waveform generator.

This interface allows measurements to be made with rapidly varying input signals whose bandwidth requirements are in excess of the ranges available with the data logger described in the July issue.

The hardware features control logic which allows samples to be aquired and converted in approximately 15μs. The d-to-a converter also provides a programmable trigger level when the a.d.c. is used for recording transients.

Via a block of ram, the interface can output or input up to 2816 values at intervals from 15μs to 1290μs. The output may be retriggered to generate continuous waveforms at a selected frequency; inputs are displayed on a high-resolution screen simulating anioscilloscope with a sweep time of 4ms to 3.6s.

Circuit and software details are for the Apple II but it should be a simple matter to adapt the interface to other 6502-based machines.

Hardware

The hardware makes use of the Ferranti chips ZN447 and ZN428 for a-to-d and d-to-a conversion. The 447 is an eight bit, successive-approximation device with a conversion time of less than nine clock cycles. With a 100pF capacitor connected between pin 3 and ground, the internal clock operates at about 1MHz. Resolution is 1 part in 256, giving a dynamic range of 48dB.

The input range, 0 to V_{ref}, is essentially 0 to 2.5V but the input network extends it to ±5V.

The analogue input circuitry also includes four cascaded unity gain double-pole filter stages preceded by an input buffer and a non-inverting amplifier with a gain variable up to 90. For the filter stages the overall cut-off frequency is about 10kHz and the gain roll off 48dB per octave.

The input buffer can be switched to a.c. or d.c. coupling. When the signal is direct-coupled, the input resistance is about 4MΩ; when it is a.c.-coupled, the cut-off frequency is less than 1Hz. Input and output amplifiers are dual fet operational amplifiers TL082. The digital to analogue converter includes an input data latch and has a settling time of 800ns.

The output is buffered and level shifted with gain to cover the range ±5V, allowing the complete system to be operational with the same gain on input and output. The output of the buffer is filtered through a four-pole, unity-gain filter with a cut-off frequency equal to twice that of the input filter, that it about 20kHz.

In constructing the circuit, take care to use a good quality hold capacitor between pin 11 of the sample-and-hold chip and ground. The three most suitable types in order of preference are polystyrene (below + 85°C), Teflon and Parlene. Drift in the hold mode can be minimized by surrounding pin 11 with a guard ring of track which links pins 7,10 and 12. The offset potentiometer between pins 3 and 4 produces a change in the output of the order of two l.s.bs.

A-to-d and d-to-a operations are controlled through the signals $\overline{\text{SC}}$ (start conversion), $\overline{\text{RAD}}$ (read a to d) and $\overline{\text{WDA}}$ (write to d to a). A further signal $\overline{\text{WAD}}$ (write to a to d) is required to initiate an interrupt-driven data acquisition sequence. The address of the chips in the memory map of the Apple II is determined by the strobe signals $\overline{\text{DEV SEL}}$ and $\overline{\text{I/O}}$ available in the Apple slots.

The interface is designed to operate in slot 1 for which $\overline{\text{DEV SEL}}$ goes low in the ϕ_2 part of the clock cycle of the processor, when the address is in the range $C090_{16}$ to C09F. In the second half of the clock cycle $\overline{\text{I/O}}$ goes low when the bus holds an address in the range C800 to C8FF. Both signals therefore have a duration of approximately 400ns and could, if required for other machines, be produced by address bus decoding as described in the third article. The address bus decoded signal could then be logically anded with ϕ_2 to produce a pulse of the required duration.

In the interface $\overline{\text{I/O}}$ is combined with R/$\overline{\text{W}}$ to produce the required active low write strobe to the d-to-a whilst $\overline{\text{DEV SEL}}$ is combined with R/$\overline{\text{W}}$ to produce the required $\overline{\text{SC}}$ and $\overline{\text{RAD}}$ signals for a to d.

The relative timings required, shown in diagram 2, are achieved using two dual monostables, 74LS123, which are triggered by the falling edge of a START signal which can be produced in one of two ways.

As can be seen from page 30 the output of the Schmitt nand, gate 1, will go high when either $\overline{\text{RAD}}$, a read of the a.d.c. or $\overline{\text{IRQ}}$, an interrupt request, is taken low. When either strobe returns high START will go low producing the negative-going trigger input to the two monostables.

Assuming that $\overline{\text{RAD}}$ initiates the sequence, the timing is as follows. The $\overline{\text{RAD}}$ strobe takes about 400ns and coincides almost exactly with START. One half of monostable 1 is triggered by START's falling edge to produce a time, delay of approximately 0.5μs(Fig. 2).

Previous articles in this series of intelligent interfaces for the Apple II and other 6502 machines have included:

- **real-time clock board (April)**
- **eprom programmer (May)**
- **data logger (July)**

An assembly language listing of the software for this design is available from the editorial office. Please enclose a stamped addressed envelope and mark your covering envelope 'Apple waveform recorder'.

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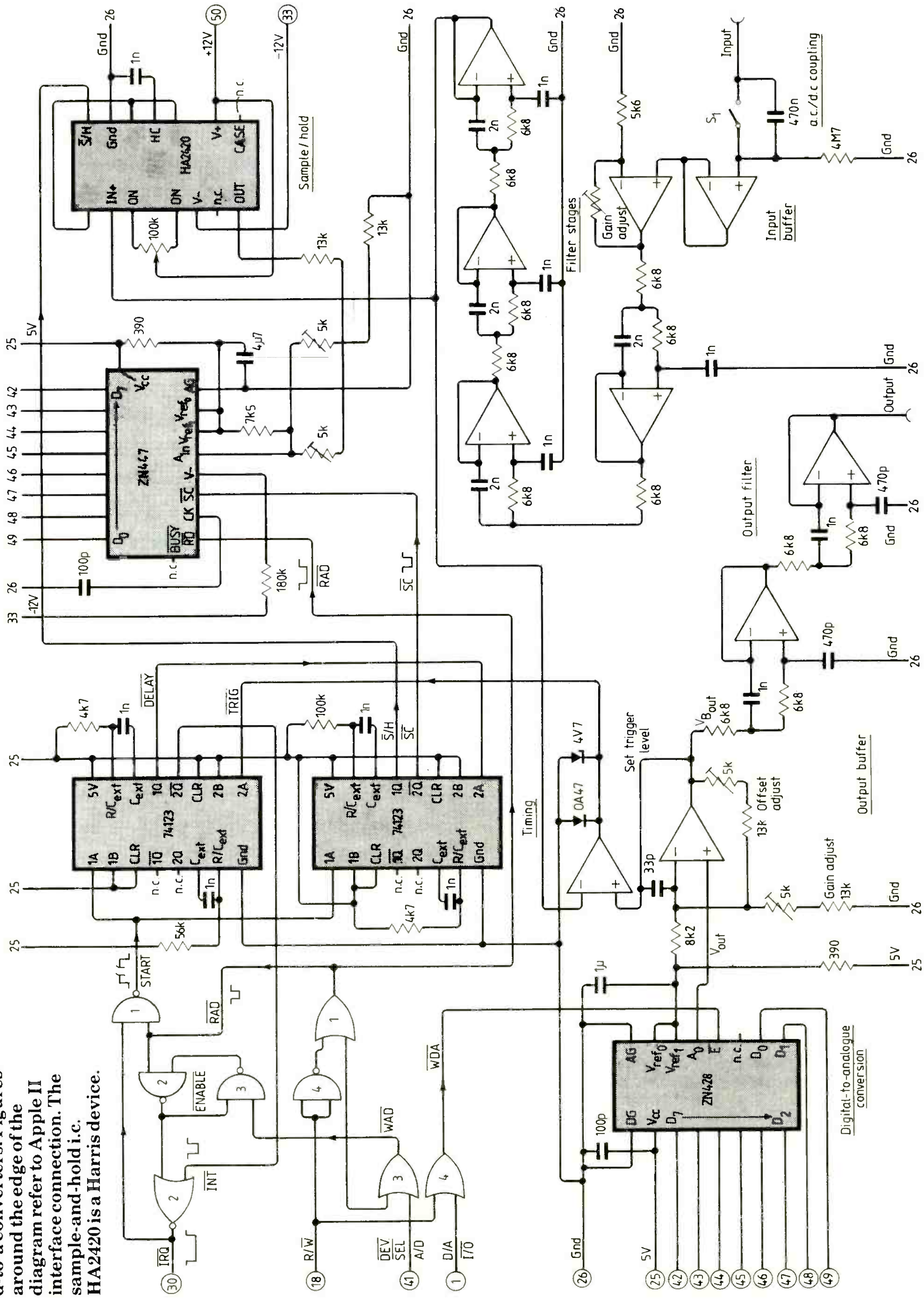

Fig. 1. The interface contains both a-to-d and d-to-a converters. Figures around the edge of the diagram refer to Apple II interface connection. The sample-and-hold i.c. HA2420 is a Harris device.

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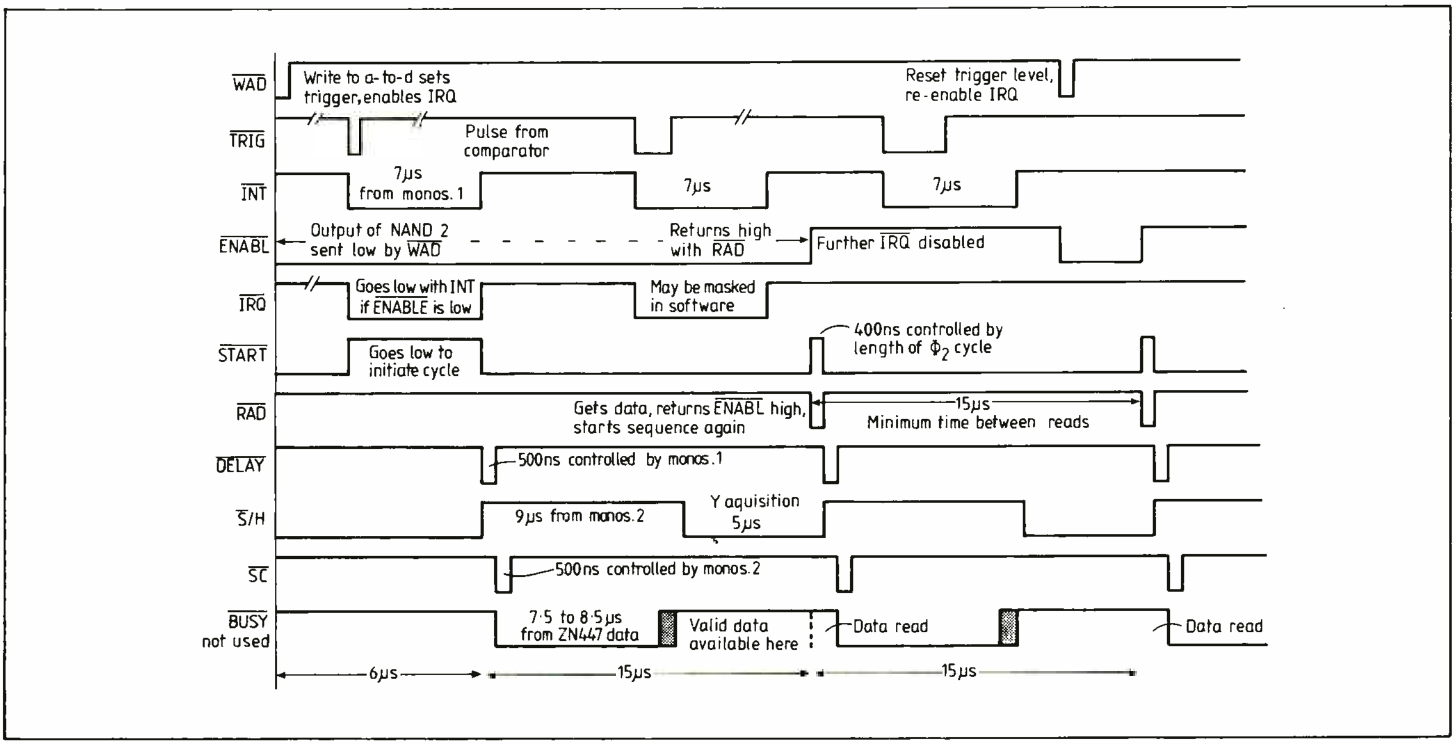

The rear edge of $\overline{\text{DELAY}}$ is used to produce $\overline{\text{SC}}$ which is also about 0.5µs long (100ns is all that is required).

One half of monostable 2 is also triggered by START's falling edge and produces a 9µs long hold signal at pin 14 of the sample and hold circuit. Conversion takes place during this hold period; at the end of the conversion, about 8.5µs after $\overline{\text{SC}}$ goes high, data is available for reading.

The sample-and-hold circuit acquires the next sample in the 5µs which elapses before the data is read thus taking $\overline{\text{RAD}}$ low again to repeat the sequence. This sequence is used when the a-to-d interface is operated without a trigger level.

Writing to the d.a.c. can be used to set (or reset) the trigger level at the input of one TL082 connected as a comparator. A write to the a.d.c. produces the strobe $\overline{\text{WAD}}$ which causes the output of the Schmitt nand, gate 2 ($\overline{\text{ENABL}}$), to go low.

If the output $\overline{\text{INT}}$ from the remaining half of monostable 1 is also low then an interrupt request, $\overline{\text{IRQ}}$, will be generated at the output of gate 2 of the quad or gate. If at this time the processor is engaged in servicing a previous interrupt the request will be masked out in software since the I bit will be set in the service routine. It is the level change at the output of the comparator which triggers monostable 1 to produce $\overline{\text{IRQ}}$ pulse of about 7µs when $\overline{\text{ENABL}}$ is low.

Whilst the output of or gate 2 is low the output of nand gate 1 is high. But when the output of the or gate returns high, both inputs to the nand gate are high and the output goes low. This produces the trailing edge of START which is required to initiate the sequence. Since the $\overline{\text{IRQ}}$ input to the processor is level-sensitive the line must be held low for sufficient time for the processor to finish execution of its current instruction, about 7µs.

The $\overline{\text{ENABL}}$ output of the R-S flip flop, made from nand gates 2 and 3, must be set high if further interrupts are to be hardware-disabled. This is achieved by the first read of the data from the conversion. When $\overline{\text{RAD}}$ goes low further interrupts can only be enabled by rewriting to the a.d.c. to produce a further $\overline{\text{WAD}}$ strobe.

Both START possibilities are illustrated in the timing diagram Fig. 2 which also illustrates how the interrupts may be controlled.

The interval between successive reads of the a.d.c. can be about 15µs; the actual time will depend largely upon the choice of timing components for the monostables. The corresponding sampling rate of about 66kHz allows signals with a bandwidth of 10kHz to be sampled and displayed.

Each write to the d.a.c. produces the strobe $\overline{\text{WAD}}$ and can be used to set or reset the trigger level to the a.d.c.; each output l.s.b. represents 10mV. After passing through the buffer with gain the trigger increments are ±40mV.

Waveforms can be output through the d.a.c. by writing data successively to the port. The data may have been acquired from the analogue input or may have been stored previously, after calculations, in a reserved block of memory. A measure of synchronization can be achieved in this application by using the trigger on the a.d.c. input. This technique is described later.

Software

A hex code listing of the software is given in the Table. For a-to-d operation, CALL 51456; and for d-to-a operation CALL 51460. The first part of the firmware writes a program in ram at 9600_{16} to input or output a chosen number of values at selected intervals. The number of values is selected by keying in a hex number between 1 and B to give 100_{16} to $B00_{16}$ bytes.

The interval is selected by keying in a hex number between 0 and FF; its length in microseconds is equal to five times this value plus 15. All interrupts are disabled and the $\overline{\text{IRQ}}$ vector is set to 9600_{16}; a

Fig. 2. Timing diagram for the interface. Samples can be acquired and processed in just 15µs.

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Hex listing in 6502 machine code.

```
C8A0  00 00 28 68 68 A0 00 40   ..(hh .@
C8A8  AD 90 C0 99 00 01 A6 FA   -.@...&z
C8B0  CA D0 FD C8 D0 02 60 00   JP}HP.'.
C8B8  B9 00 01 8D 00 C1 A6 FA   9....A&z
C8C0  CA D0 FD C8 D0 02 60 FF   JP}HP.'.
C8C8  51 92 9C A8 8A A4 AC 82   Q..(.$,.
C8D0  98 5A 62 6A 52 5E 6A 9A   .ZbjR^j.
C8D8  92 86 A4 9E A6 8A 86 74   ..$.&..t
C8E0  48 9D 9E 5E A0 82 8E 8A   H..^ ...
C8E8  A6 74 48 A9 A4 92 8E 8E   &tH)$...
C8F0  8A A4 74 48 FF FF FF FF   .$tH....
C8F8  FF FF FF FF FF FF FF FF   ........
C900  A9 A8 D0 02 A9 B8 85 1E   )(P.)8..
C908  A9 C8 85 1F AD 90 C0 A9   )H.. .@)
C910  00 8D FE 03 A9 96 8D FF   ..~.)...
C918  03 20 E4 CB A2 E1 A0 19   . dK"a .
C920  20 4B CD A2 00 20 0B CD    KM". .M
C928  A6 F9 E8 86 FA A2 EB A0   &yh.z"k
C930  26 20 4B CD A2 02 20 0B   & KM". .
C9C8  CD C9 0C B0 F0 69 7F 85   MI.0pi..
C940  FB A9 FF 85 73 A9 7F 85   {)..s)..
C948  74 85 FD EA A2 00 BD A2   t.}j".="
C950  68 9D 00 96 E8 E0 05 D0   h...h'.P
C958  F5 A2 00 A0 00 E6 FD A5   u". .f}%
C960  FD C5 FB 08 B1 1E C9 01   }E{.1.I.
C968  D0 02 A5 FD 28 D0 06 C0   P.%}(P.@
C970  07 D0 02 A9 F9 9D 05 96   .P.)y...
C978  C8 E8 C0 0B 90 E1 A5 FD   Hh@..a%}
C980  C5 FB 90 D7 A5 F9 D0 0C   E{.W%yP.
C988  CA CA CA CA CA A9 EA 9D   JJJJJ)j.
C990  05 96 0A E8 B1 1E C0 0D   ..jh1.@.
C998  D0 03 8A 49 FF 9D 05 96   P..I....
C9A0  C8 E8 C0 0F 90 EE B1 1E   Hh@..nl.
C9A8  F0 0A 58 8D 90 C0 20 03   p.X..@ .
C9B0  96 F0 FB 60 85 FC 85 FD   .p{'. .}
C9B8  A9 20 85 E6 A9 40 85 E3   ) .f)@.c
C9C0  AD 54 C0 AD 53 C0 AD 57   -T@-S@-W
C9C8  C0 A2 F4 A0 99 20 4B CD   @"t . KM
C9D0  A2 06 20 0B CD A5 FF F0   ". .M%.p
C9D8  03 8D 00 C1 A9 C9 48 A9   ...A)IH)
C9E0  FF 48 58 8D 90 C0 AD 00   .HX..@-.
C9E8  C0 10 FB 78 8D 10 C0 AA   @.{x..@*
C9F0  68 68 E0 8D D0 34 AD 90   hh'.P4-.
C9F8  C0 AD 54 C0 AD 51 C0 60   @-T@-Q@'
CA00  AD 52 C0 AD 50 C0 A5 E6   -R@-P@%f
CA08  49 60 85 E6 A5 E3 49 20   I'.f%cI
CA10  85 E3 A5 FC 49 01 85 FC   .c% I..
CA18  20 45 CA 20 30 CA A4 FC    EJ 0J$
CA20  B9 54 C0 A5 FF D0 B5 20   9T@%.P5
CA28  E6 C9 78 A0 0F 4C A6 C9   fIx .L&I
CA30  A2 00 8A 48 A0 00 BD 00   "..H .=.
CAC8  80 49 FF 4A 20 57 F4 68   .I.J Wth
CA40  AA E8 D0 EE 60 A9 00 A8   *hPn').(
CA48  A6 E6 86 FE 91 FD C8 D0   &f.~.}HP
CA50  FB E8 E4 E3 D0 F4 60      {hdcPt'
```

data buffer is reserved at 8000_{16}.

For d-to-a operation the firmware clears interrupts and then repeatedly calls the subroutine at 9603_{16} (the first three bytes, clearing the stack, are omitted). CALL 51627, after resetting the machine, provides continuous playback of the data.

Since the period of repetition may not exactly equal the playback time some form of synchronization is required. This can be achieved by providing an interrupt on input of an a.c. signal or a trigger level through the a-to-d interface. The firmware causes the playback to restart, from the beginning of the data buffer, at each interrupt event. A variable-frequency square-wave provides a suitable synchronizing signal.

For a-to-d operation, the firmware allows the trigger level to be input via the keyboard. The start address of a graph-plotting routine using the rom subroutine at $F457_{16}$ is pushed on to the stack. The interrupt service routine at 9600_{16} clears the stack of re-entry data pushed on by the interrupt sequence so that when data acquisition is complete, the processor returns to the graph plot. The secondary screen page is wiped and the graph plotted on this page. The other page is then selected using the software switch provided in the Apple system, causing the digital trace to appear. Vectors are then altered so that the next trigger causes the graph to be plotted on the other page, and so forth, giving a continuous display.

Whilst the processor is waiting for an interrupt it continuously polls the keyboard. If a key is pressed, execution jumps to the trigger input phase so that the trigger level may be re-set. If a trigger level of zero is input, the trigger level is not re-set and the interrupt is not cleared after data acquisition so that one-shot oscilloscope operation rather than a continuous mode is achieved.

If the return key is pressed, execution returns to the operating system, with all interrupts disabled. The digital oscilloscope displays only 256 data points, equally spaced over the whole acquisition period, and has only half the full 8-bit vertical resolution.

Calibration

The gain can be adjusted up to about 90 using the 500k potentiometer. The optimum gain is that which gives an input signal in the range ±5V. The d.a.c. may be calibrated by writing 3_{16} to the chip and adjusting the offset potentiometer in the output buffer until the output signal is −5V. Writing FD_{16} to the d.a.c. and adjusting the gain potentiometer until the output is ±5V completes the calibration with one l.s.b. equivalent to ±40mV.

To calibrate the a-to-d interface the two potentiometers connected to its input should be adjusted as follows. Input an a.c. signal near to the full range value. CALL the a-to-d program and set the trigger to 0. Reset the trigger continually until the trigger operates and a trace appears on the screen. Press return and inspect the memory buffer; the smallest stored value should be that of the trigger level. Adjust the offset potentiometer and repeat until successful.

Now set the trigger level to FF_{16} and continually reset the trigger to a lower value until a trace appears. The largest value stored in the buffer should be that of the trigger level. Adjust the gain potentiometer until this is so. ■

IN OUR NEXT ISSUE

What makes a good oscillator?
K. Lewis discusses the parameters to consider when defining the performance of an oscillator and attempts to remove some of the confusion which can prevent a better understanding of the subject.

Ringing the changes on bels
Jules Watt begins a series on subjects which all engineers consider basic, but which often contain elements of misunderstanding, leading to error. This article is on decibels, which have been used to indicate ratios of almost anything from salaries to horsepower.

Thames television logo player
The opening sequence of Thames programmes, the view of St Paul's and Tower Bridge, is not obtained from a film, but solid-state memory. I.G. Brown describes its production and the equipment used.

8085 development on the BBC computer
J.L. Gordon describes hardware, firmware and software which enable a Beeb owner to develop applications from the 8080 series of microprocessors. The system consists of a single 8085 controller board.

Applying a single-chip microcomputer
Mike Catherwood demonstrates the capabilities of Motorola's 'S2' 28-pin single-chip microcomputer with a-to-d converter, using a pulse-burst generator and frequency meter as application examples.

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Heat transfer in electronic equipment

by K.L.Smith, Ph.D.*

*University of Kent at Canterbury

The generation of heat in active devices is a frequent cause of failure. Dr Smith shows that removal of the heat is not quite as straightforward as one might suppose.

Active devices in electronic systems handle energy flows at various rates. In these processes, the efficiencies of power conversion into the wanted form never reach 100% and the "losses" appear as low-grade heat energy. Efficiency can be defined in these systems as the fraction of the power input appearing in the wanted form at the output.

This was well illustrated in an application I discussed recently[1,2]. In those articles, I pointed out how engineers attempt to raise the efficiency by using switching methods in power supplies, instead of dissipative control in the linear versions.

Whichever design techniques are employed, either those used to increase the efficiency, as in switchers, Class B or Class C amplifiers and so on; or whether dissipation is deliberately tolerated, as in series-pass designs, Class A amplifiers and similar, getting rid of the thermal energy produced is important. If heat is not removed quickly, the associated temperature rise could soon destroy the devices. In any event, increases in the operating temperature, or even high storage temperatures, will reduce the reliability of components, although they are below the burn-out point. A typical reliability curve as a function of temperature is shown in Fig. 1. In high power systems, the rate of heat production is considerable.

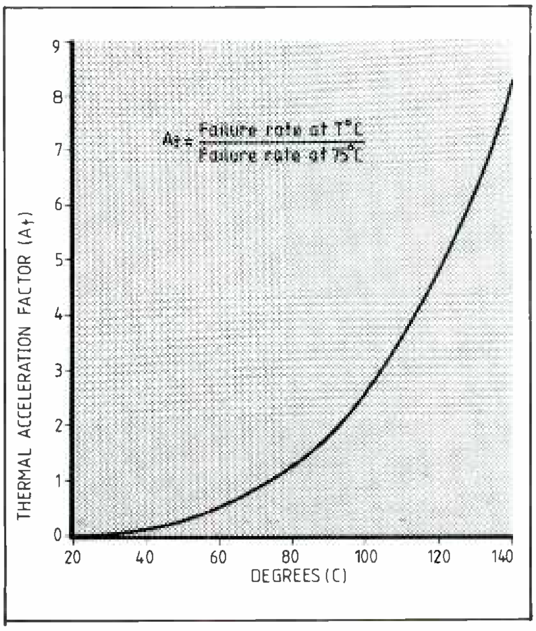

Fig. 1. There is a rapid rise in the failure rate of electronic components as the temperature goes up. This is the same as saying that the reliability worsens. Even at temperatures considerably lower than the absolute maximum allowed, the lifetimes may be much reduced.

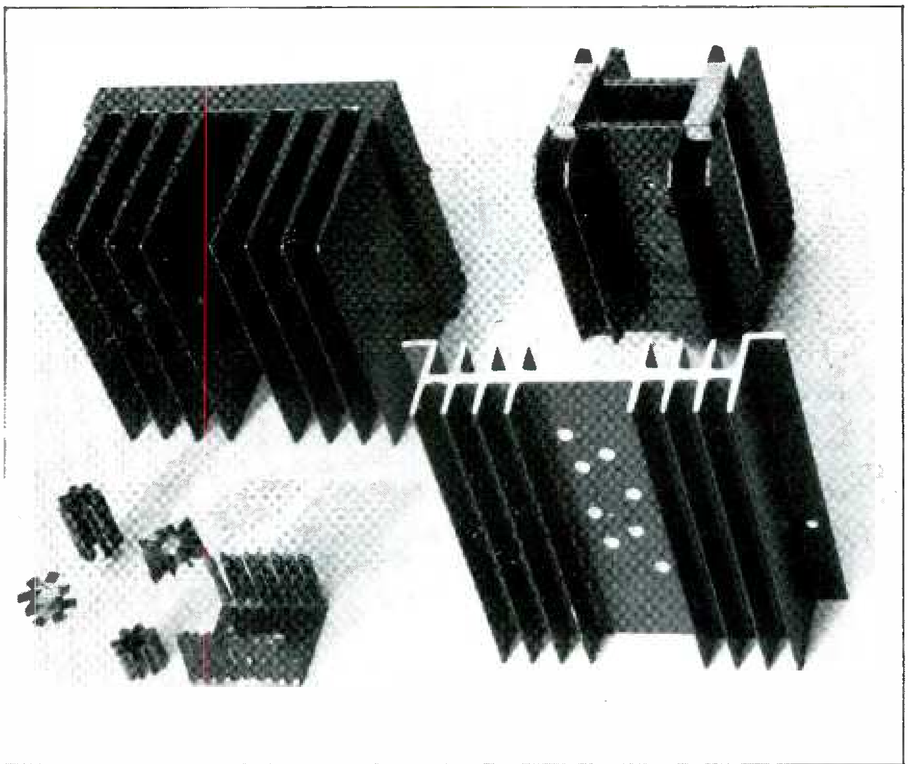

Fig. 2. These typical finned heatsinks and coolers found in electronic equipment show the diversity of design shapes and sizes, according to the duty expected of them.

Heat sinks

There are only three ways available to remove heat energy. You can conduct it away through a substantial block of material (usually metallic). A fluid can be passed by or through, the hot region, warmed and thus bear away the surplus heat. This is cooling by convection which can be classified into two 'regimes'. One is cooling by natural convection; the other by forced fluid flow. Either is notoriously difficult to analyse. Finally, energy radiates away from the hot region at the speed of light. The ease with which it radiates depends on the physical nature of the hot surface.

The important rule from thermodynamics which cannot be avoided is that heat energy will not flow by any of the mechanisms just mentioned unless there is a temperature difference. It is absolutely no good spending a lot of money on a heat dissipating system if you want to keep your transistor at 75°C in surroundings also at 75°C.

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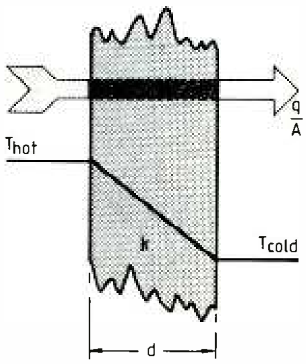

Fig. 3. The assumption that a linear temperature gradient occurs under steady state heat flow normal to the surface of conducting wall is illustrated. The slope of the gradient is directly related to the thermal conductivity of the wall.

The heat will only pass from hot to colder regions and the answer to the old joke question about how long will it take to boil a kettle on a block of ice is, 'a very long time indeed'*. Therefore in cooling requirements of any kind you must have a cool heat sink or low-temperature reservoir. Strictly speaking, the metal plate, or block with fins on it, is not the heat sink proper. The ultimate sink is the fluid – usually air – into which the heat finally passes, there to be borne away. But it has become universal with electronic design people to call the block upon which the active devices are mounted, a *heat sink*. If the dissipator block is so small that it is mounted onto the device instead, it is often called a *cooler*. Some of the sinks and coolers in current use are illustrated in Fig. 2.

Thermal conduction

The quickest and easiest method to remove heat energy from a concentrated point is to conduct it away in all directions. To do this, a good conducting solid material must be in intimate contact all round the source. This is not always convenient in the case of electronic components and the heat transport approximates to flow across an area normal to one direction into the heat sink.

After switching on the power and beginning to dissipate heat, the thermal energy spreads out in the larger volume of the sink, raising its temperatures according to its *thermal capacity*. This is the transient phase. When the steady state is reached, the temperatures become stable, only altering if the dissipation and/or the temperature of the surroundings changes.

Fourier[3] proposed that the rate at which heat flows through a solid is proportional to the area A, normal to the flow and to the temperature gradient dT/dx,

$$q = -kA\frac{dT}{dx} \text{ watts}$$

The minus sign tells us that the heat is going from the high to the low temperature along the x direction. The proportionality constant k (watts per metre per °C), is the *thermal conductivity*. In many instances, the temperature gradient is uniform. An example might be the insulating washer under a transistor on a heat sink, as in Fig. 3. Therefore q across an area A, through thickness d, is,

$$q = \frac{kA}{d}(T_1 - T_2) \text{ watts} \qquad (1)$$

The thermal conductivity is not often used directly in electronic cooling problems, but transposing equation (1) gives,

$$\frac{T_1 - T_2}{q} = \frac{d}{kA} = R_{th}\ {}^{\circ}\mathrm{CW}^{-1}$$

where R_{th} is the *thermal resistance*.

As the heat flows from the hot spot to the surroundings, it passes across various interfaces, goes through various materials and otherwise models closely a series electrical circuit. The temperature corresponds to the potential difference, with the heat flow analogous to the current. The electrical resistance corresponds to the thermal resistance and thermal capacity corresponds to electrical capacitors in shunt. This is summarised in Table 1 and Fig. 4. The major job in heat sink design is to determine the thermal resistance and use a thermal version of Ohm's Law to solve the design problem.

*Although according to statistical thermodynamics, it is not absolutely impossible!

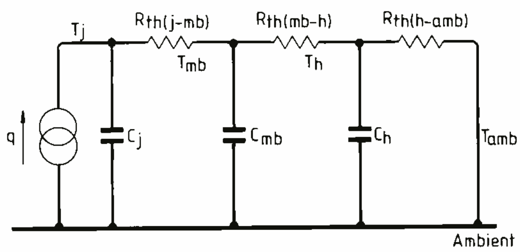

Fig. 4. The electrical analogue of thermal flow problem is a typical low-pass filter. Steady-state conditions corresponds to the d.c. case in the electrical circuit. If the thermal capacitances are large, a considerable time may elapse before steady conditions are reached. Designers sometimes exploit this on the assumption of intermittent loads, (in an amateur transmitter, say).

Convection

The end stage dissipation from the heat sink to the surroundings is a surface phenomenon, as already mentioned. By attaching fins to the surface, a large increase in area is obtained which assists this convection process. Radiation is not helped much by fins, as their surfaces 'look at' each other.

Natural convection appears to rely on a stationary boundary layer of the fluid 'stuck' to the surface, as it were. The heat has to flow through this layer by conduction. The layers further out receive the heat, expand, and the resulting lower density increases the buoyancy of these layers and the fluid rises, thus drawing in more cool fluid from the bottom.

A few points arise concerning this mechanism. The fins must be vertical, or little smooth flow can be established. Restrictions in the path of the fluid flow should be avoided and finning is of little use if the fin spacing is less than the sum of the two boundary layer thicknesses. Of course, in weightless conditions, there is no natural convection.

On the other hand, forced convection with a fan or blower tends to break up the boundary layer, or at least make it much thinner, as well as removing the fluid much more quickly. The forced process is obviously much more efficient at removing the heat. The fins, or channels can follow any geometry, as gravity is no longer relevant.

The ideas just expressed are reminiscent of some elementary physics most engineers must have met in their schooldays. Forced convection has some connection with Newton's Law of Cooling. It was Sir Isaac [4] who gave us the empirical expression for this,

$$q = h_c A (T_s - T_f) \qquad (2)$$

where q, the heat loss rate is proportional to the surface area A, (which explains the finning) and to the difference between the surface temperatures T_s, and fluid temperature T_f. The proportionality 'constant' h_c is called the *heat transfer coefficient*, in this case, for convection. Equation (2) is very similar to equation (1). Over the years equations of this type have become generalized expressions describing any heat flow process. The difficulty in using equa-

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TABLE 1	
electrical	Thermal
current generator	heat generator
resistance R, $\frac{\text{ohms}}{\text{ampere}}$	thermal resistance R_{th}, $\left(\frac{C}{W}\right)$
capacitance C, $\frac{\text{amp sec}}{\text{volt}}$	thermal capacity C_{th}, $\frac{\text{watt sec}}{C}$
potential diff. $(V_1 - V_2)$, volts	temperature diff. $(T_1 - T_2)$ C
current (charge flow), amps	heat flow, watts

TABLE 2	
Device Package	$R_{th(j-mb)}$
TO5/TO39	15°CW^{-1}
TO3	1.5 to 2.5°CW^{-1}
TO220	4°CW^{-1}
TO202	12°CW^{-1}

tion (2) in convection calculations is connected with finding h_c. This coefficient is anything but a constant and the equation is hardly a physical 'law'. Using equation (2) amounts to an empirical approach, considering the guesses that must be made to determine h_c. The heat transfer coefficient depends on shape and geometry of the surfaces and the properties of the fluid. It even depends on the temperature difference, so calling it a proportionality constant is certainly a misnomer.

If you had gone on to study a little more physics of convection, a bewildering array of 'numbers' would have arisen. A student soon finds that dimensionless quantities called Nusselt numbers, Grashof numbers, the Prandtl number and so on, all arise. There is no space to go into this rather involved area here[5] but the approach boils down to writing,

$$N_u = C(G_r)^{\alpha}(P_r)^{\beta}$$

where N_u $\left(=\frac{haL}{k}\right)$ is the Nusselt number, G_r

$$\left(=\frac{g\gamma p^2 L^3 (T_h - T_c)}{\mu^2}\right)$$

is the Grashof number and P_r $(=C_p\mu/k)$ the Prandtl number.

In these expressions, the quantities involve viscosity, density, thermal conductivity and thermal cubic expansion of the fluid. The gravitational acceleration g comes into the picture and the temperature difference, together with a 'characteristic length' L describing the geometry of the cooling object. The problem is to determine the indices and . This is done experimentally. Once the Nusselt number and L are found, so is h_c.

Saunders[6] found that and were 0.25 for smooth natural fluid flow and 0.33 for turbulent flow. On a large heatsink there is the likelihood of laminar and turbulent flow occurring over different parts at the same time. A flat plate fin might develop a flow pattern as shown in Fig. 5.

The outcome of these investigations is a working value of h_c which, for simple vertical plates cooling in normal air, is given by,

$$h_c = 1.37\left(\frac{T_S + T_A}{L}\right)^{0.25} Wm^{-2\circ}C^{-1} \qquad (3)$$

where T_S is the plate temperature and T_A is that of the ambient or surrounding air. This shows that h_c is itself a function of the temperature difference. L is the vertical height of the plate in metres.

Another complication arises in that the metal of the plate or fin has a finite conductivity. Therefore temperature differences to the ambient vary over the surface of the fin, being greatest near the dissipating device. This means that the cooling performance of practical plates is a little less than what at first sight might have been expected. This lowering from the ideal is taken into account by using *fin effectiveness factor* . Fin effectiveness (for a given amount of heatsink material) is improved if the cross section of the fin is triangular instead of rectangular. Putting it another way, the same heat dissipation requires only about 70% of the heatsink material[7] if a triangular cross section is used for the fins.

The fin cross sectional area, and hence fin volume, increases as the cube of the heat flow. So if you want to double the heat dissipation for the same temperature difference, a fin eight times as large would be required. On the other hand, a second fin, identical to the first, would do the job. Therefore in heatsink design the use of many stubby fins is much better than one or two large ones. But there is a limit to how close fins can be, as I mentioned above regarding fluid boundary layer thickness.

Radiant heat loss

At first sight, because thermal radiation is such a strong function of the temperature, one might think that calculations would be even more intractable than for convection. Fortunately this is not so, as the Stefan – Boltzmann Law is quite rigorous. The only slightly vague factor is the *emissivity* of a surface, which varies with its colour, texture and so on.

According to Stefan – Boltzmann, for a body at absolute temperature T_S °K, with surface area A and emissivity E, the rate of heat loss is,

eq

where σ is *Stefan's Constant* = 5.67×10^{-8} $Wm^{-2}K^{-4}$

If the body is immersed in surroundings at temperature T_A, it receives heat at a rate of,

$$q^A = EA\sigma T_A^4$$

$$\therefore \; q = q_S - q_A = EA\sigma(T_S^4 - T_A^4) \text{ watts} \qquad (4)$$

Now if the hot body's temperature (T_S) is not too great, we can write the average temperature as $(T_S + T_A)/2$. Half the difference between the temperatures, $(T_S + T_A)/2$, represents how far T_S is above, and T_A is below the average temperature. Substituting these in equation (4) and simplifying by neglecting small quantities, we have,

$$q_S = EA\sigma T_S^4 \; (T \; \underline{T_A} + 273)^3 (T_S - T_A)$$

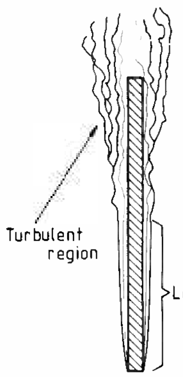

Fig. 5. The flow along a vertical plate or fin is often complex. There is a region of laminar flow – and the building up to this at the bottom. Further up the fin, if it is long enough, the flow breaks up into turbulent region. The removal of heat per unit area of fin differs in the two regions.

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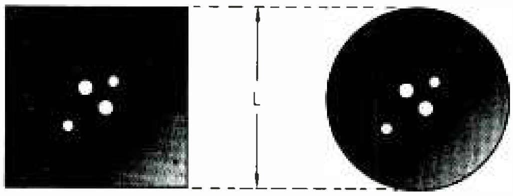

Fig. 6. Simple flat plates, either rectangular or circular, are sometimes used for light-duty heat removal. They should nevertheless be designed or estimated by using similar theory to that discussed here.

where T_S and T_A are now in °C.

Comparing this result with the 'rate' equation (2), a value for the heat transfer coefficient for radiation h_r, can be picked out as the factor multiplying the temperature difference,

$$h_r=4E\sigma\left(\frac{T_S+T_A}{2}+273\right)^3 \qquad (5)$$

Some emissivities are given in Table 1.

Overall heat transfer coefficient

The discussion appears reasonably satisfying in spite of the difficulties regarding convection. Heat transfer coefficients have been found for the three modes of heat transport.

h_c – convection
h_r – radiation
h_k – $(=\frac{k}{d})$ for conduction

The first two are appropriate for heat-sink design, as they are 'final surface' quantities. Thermal conductivity is an 'internal' quantity determining the flows to arrive at the final surfaces.

If a square or circular heat-sink plate is operated vertically, as shown in Fig. 6, the thermal resistance to the ambient is found from the overall heat transfer coefficient by,

$$R_{th(h-amb)}=\frac{1}{2L^2\eta(h_c-h_r)}\ °CW^{-1} \qquad (6)$$

where η is the fin effectiveness factor mentioned earlier. The evaluation of η is not easy, but I have used an average value of about 85% (0.85) without introducing significant errors for simple heat sinks. Nomographs have been published that yield more precise values of η[8,9].

As an example, consider that you have been asked to design a square, black, anodized-aluminium heat dissipator, 1.6 mm thick, where T_S=90°C and T_A=60°C. If it is to have a thermal resistance of $4°CW^{-1}$, we could proceed as follows, assuming to be 0.85 as the plate is reasonably thick.

$$\therefore h_c=1.37\left(\frac{90-60}{L}\right)^{0.25}$$

from equation (3),

$$\text{and } h_r=2.27\times10^{-7}\left(\frac{90+60}{2}+273\right)^3\times0.9$$

from equation (5).

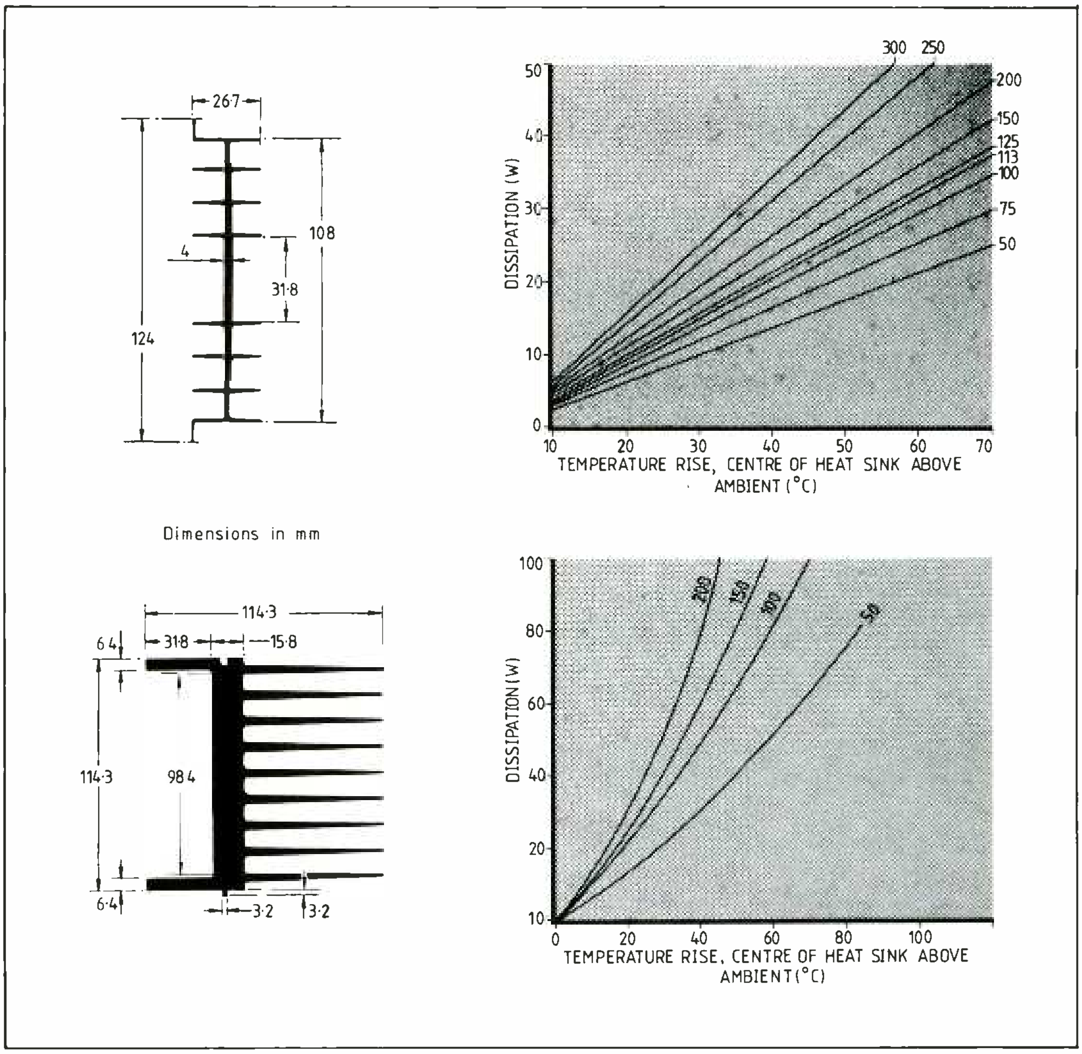

Fig. 7. These profiles are typical of commercially available extrusions for duty as finned heat sinks. The curves are used as design aids to select an appropriate sink and length. The dissipation in watts is given as a function of temperature rise above ambient, with the length as a running parameter on the curves. (With acknowledgements and thanks to Messrs. Marston Ltd., Wolverhampton.)

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Substituting into (6),

$$4=\frac{1}{2L^2\times0.85\left[1.37\left(\frac{90\text{-}60}{L}\right)^{0.25}+1.45\times10^{-10}\left(\frac{90+60}{2}+273\right)^3\right]}$$

The only unknown is L, which we want. But how is this equation solved, containing as it does L^2 and $L^{0.25}$, without a high-powered computer program?

The usual procedure is to guess an initial value for L 'from experience', substitute and see what result is obtained.

Guess a value L=10cm

$$\therefore h_c=1.37\left(\frac{90+60}{0.1}\right)^{0.25}=5.7\ \text{Wm}^{-2}{}^{\circ}\text{C}^{-1}$$

$$\text{and } h_r=0.9\times2.27\times10^{-7}\left(\frac{90+60}{2}+273\right)^3=8.6\ \text{Wm}^{-2}{}^{\circ}\text{C}^{-1}$$

$$\therefore R_{th(amb)}=\frac{1}{2\times0.10\times0.85\times14.3}=4.1\ {}^{\circ}\text{CW}^{-1}$$

This result is reasonably satisfactory; the plate could be made just a little larger. If an unsatisfactory value had been obtained, try a new size – larger or smaller as required.

What is worth noting here is the large contribution by radiation. Also worth noting is that the area A, for insertion into the formulae to calculate h_c and h_r, would differ for more complex (finned) geometries.

Commercial heat sinks

All the basic work has been done by the manufacturer who publishes $R_{th(h-amb)}$, or curves describing the performance of various lengths of the standard extrusions. Some of the heat sinks available are illustrated in the photograph. Fig. 7, together with the performance graphs, shows typical heat sink profiles that are available. Of course, the final thermal resistance is only one in a series chain back to the device junction. If the device is poorly mounted, then it could very well burn out – even on an infinite heat sink.

The thermal resistance from junction to mounting base $R_{th(j-mb)}$, is set by the manufacturer. Table 2 gives an indication of $R_{th(j-mb)}$ for a few common packages.

The mounting base is usually bolted directly to the heat sink, but often an insulating washer is required to electrically isolate the device from the often-grounded heat-sink mass. This tends to isolate the mounting base thermally as well, because electrical insulators are usually thermal insulators also. Table 3 gives typical thermal resistances for various mounting washers and the thermal compounds often met in practice. The bolting down pressure can have a large effect on $R_{th(mb-h)}$.

The 'thermal drop' $(T_j - T_{amb})$ is easily found by passing the heat flow through $R_{th(j-mb)}$, $R_{th(mb-h)}$ and $R_{th(h-amb)}$ in series so that,

$$T_j-T_{amb}=\frac{R_{th(j-mb)}+R_{th(mb-h)}+R_{th(h-amb)}}{q} \quad (7)$$

TABLE 3

All mountings have thermal compound on both sides of the washer, or on the mounting base, except the last case.

Washer Material	Thickness		$R_{th(mb-s)}$	
mica	0.002 in.		0.4	
anodized aluminium	0.016 in.		0.35	
beryllia	0.063 in.		0.25	
		hole diameter in heat sink	at bolt torque of: 2 lb in.	5 lb in.
mica	0.004 in.	0.25 in.	2.2	2.05
mica	0.004 in.	0.113 in.	2.1	1.9
mica	0.002 in.	0.25 in.	1.6	1.5
mica	0.002 in.	0.113 in.	1.45	1.4
bare	–	0.14 in.	0.3	0.2
bare (no compounds)	–	0.14 in.	1.4	1.0

where q is now the thermal power dissipated in service by the junction of the device. T_j is the junction temperature laid down by the device manufacturer which must not be exceeded. T_{amb} strongly depends on your environment and is an awkward parameter to determine. The thermal resistances are all now well understood, so given the awkward T_{amb}, the final design is in principle, easy.

Whether you make a custom heat dissipator or buy a standard extrusion after doing the calculations, the final size of the heat sink is determined your by ambient temperature. But enough has been said to show that it is little use tucking away your heat sink in a corner of a closed cabinet, or letting anyone drape their coat over the equipment in a disco – or even backing your hi-fi system onto the central heating radiator. It is salutory to realise from equation (7) that every degree rise in T_{amb} is reflected through to just about a degree rise in T_j. So, whatever the heat sinking arrangements, your devices will eventually close down in increasingly hot environments. ■

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Nigel Cawthorne

64th NAB – Dallas

NAB, the world's largest broadcast engineering show, was held in Dallas. Some 40,000 visitors from all over the world came in search of the latest developments in broadcasting.

Although there are many stories to be told from this year's NAB, this report will concentrate on just four of them: the HDTV debate, the Voice of America massive short-wave re-equipment programme, Radio Data Service (RDS) and the introduction of klystrodes into u.h.f. tv transmitters.

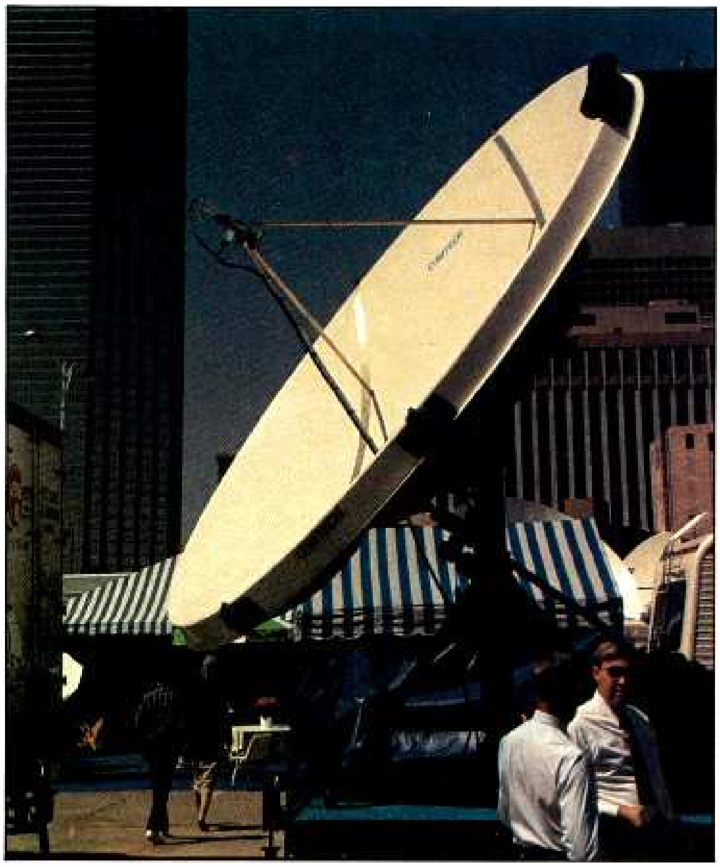
HDTV debate hots up

Less than a month before the opening of the CCIR Plenary in Dubrovnik, that will debate the controversial h.d.t.v. issue, a powerful European team used the occasion of this year's NAB to remind the 60Hz world that there is a view on the h.d.t.v. studio production standard question other than the proposed NHK 1125 line 60Hz system.

A paper introduced by France stated bluntly, "there is no question of setting definitive values for h.d.t.v. parameters (at the current CCIR Plenary) as a good deal of research and experimental are still required."

A report produced by a European team concluded that the work accomplished by the CCIR during the 1982-86 research period now provides a good understanding of the requirements that a compatible world h.d.t.v. production standard will have to satisfy. The Europeans proposed that additional h.d.t.v. research should be done during the next four-year CCIR period ending in 1990, with the objective of agreeing a world standard at the next series of CCIR Final Meetings.

A special h.d.t.v. demonstration area at NAB included equipment from 24 manufacturers, including cameras from Sony and Bosch, a telecine from Rank, a production switcher from Grass Valley, a Paintbox from Quantel, test equipment and monitors from Sony and a prototype component waveform monitor from Tektronix.



Mr E. William Henry, chairman of the US Advanced Television Systems Committee (ATSC) said, in direct contrast to the European's "let's wait and see" attitude, that "the time to establish a single worldwide h.d.t.v. studio standard is now".

HDTV: terrestial transmission tests

Plans for the experimental terrestial transmission of h.d.t.v. in the Washington area were described in one of the over sixty papers presented at NAB. The first objective of the US experiment is to demonstrate advanced tv systems to broadcasters through on-air transmissions rather than as laboratory curiosities.

The choice of location, the Washington area, is connected with the second reason for the experiment, which is to inform government decision makers in the US about advanced television systems.

U.h.f. tv channels in the US (unlike in Europe) are continually under threat from the land mobile radio industry, and US broadcasters hope through these experiments in the Washington area to convince Congress and the FCC not to preclude, through changes in the u.h.f. spectrum allocations, the broadcast delivery of advanced television.

For broadcasters in the US this is an urgent question, because the FCC is currently considering a proposal to allow land mobile services to share parts of the u.h.f. television spectrum with broadcasters.

The site for the experimental h.d.t.v. transmissions is being chosen so that signals could be received directly in both the US Capitol (Senate and Congress offices) and the headquartes of the FCC.

The first system demonstrated will be the MUSE (Multiple Sub-Nyquist Sampling Encoding) system, which was originally developed by the Japanese NHK for satellite distribution of the proposed h.d.t.v. standard. The compression techniques in MUSE allow the reconstruction of an h.d.t.v. picture from a signal about 8MHz wide.

MUSE has been demonstrated as a working system in Japan using f.m. However, the US experiments will use a.m. to save channel width. The test site will also be used for the experimental transmission (on terrestial u.h.f. tv channels) of MAC systems which are being advocated by the Europeans.

The US paper concluded that it is important that the programming be attractive and interesting for these local experimental h.d.t.v. transmissions, because, as the paper puts it: "Many of the people (congressmen and senators) whose present actions will influence the future of terrestial broadcasting in the US and advanced television development, are non-technical and cannot be expected to spend much time looking at colour bars, resolutions charts or ducks floating on a lake!"

European view

Representing a European view on h.d.t.v., George Walters, technical director of the EBU,

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said at NAB that "the problems facing broadcasters in relation to h.d.t.v. must be separated into those relating to production and those relating to transmission".

Waters reminded his audience that the combined Broadcasting Unions' February meeting in Prague had passed a resolution calling for the allocation of spectrum in the 22GHz band for h.d.t.v. broadcasting in Region 1. Regions 2 and 3 already have this allocation.

Getting a worldwide allocation for h.d.t.v. would present some difficulties and would require careful negotiation. For example, in the UK these frequencies are already allocated to Mercury for their fixed links. However, Waters concluded that a single, worldwide broadcast band would be the best solution for h.d.t.v.

VOA s.w. project

The VOA's massive modernization and expansion programme, which could involve the purchase of over one hundred 500kW short-wave transmitters, was a major discussion point among transmitter manufacturers at NAB.

Although not selected as one of the four suppliers (Continental, Brown Boveri, Marconi and Telefunken) of single 500kW transmitters for the VOA's evaluation trials in Greenville, Thomson-CSF from France had on display the control panel from their latest generation of high-power s.w. transmitters. Thomson were reminding visitors that their new second-generation 500kW short-wave transmitter in Abidjan had recently come on air.

Telefunken, also with an eye on the VOA \$1 billion project, had a 1/72 scale model of the 500kW short-wave transmitter. Telefunken's Juergen Graaff told *E&WW* that acceptance tests on Telefunken's recently installed 500kW transmitter were due to start at Greenville the week following NAB. The VOA were expecting acceptance trials to run for about a month.

The VOA then plan to operate the four 500kW transmitters, each from a different manufacturer, alongside each other for a comparative evaluation period of about four months. The VOA expect to be issuing the first main transmitter purchase tenders later this year.

The VOA's short-wave re-equipment project has been described as the biggest single transmitter project ever. The project involves re-equipping (or building) up to fourteen high-power transmitter sites around the globe.

CCIR/RDS – a US view

One paper at NAB explained for a US audience the effects recent CCIR decisions will have on broadcasting in North America. One area of possible disagreement was the Radio Data System (r.d.s.) proposed by the EBU. Concerns have been raised in the US regarding the compatibility of r.d.s. with other subcarrier services now in use or being tested.

F.m. subcarrier operations are now fully deregulated in the US and it is therefore unclear what regulatory weight, if any, can be given in the US to a CCIR recommendation concerning r.d.s. It is no also unclear exactly what status any CCIR-adopted recommendation enjoys in the US.

In conclusion, the paper showed a thread of hope in what otherwise could be a confused situation, by suggesting that with the current FCC philosophy of not developing or adopting technical standards, but preferring to leave this function to the "market place", a CCIR recommendation itself may be an "alternative avenue" to the pursuit of technical standards in the US.

Klystrodes

Nat Ostroff, head of the US tv transmitter manufacturer Comark, described the introduction of a klystrode into a high-power u.h.f. tv transmitter as the most significant development in u.h.f. tv transmitter design in the past 35 years.

The traditional battle between the klystron and the tetrode as the amplifying device in u.h.f. tv transmitters has now been joined by the Eimac Varian klystrode, which is a re-incarnation of a pre-war invention referred to then as the IOT (Induction Output Tube).

Today's klystrode has magnetically focussed electron beam, an input cavity and a collector. The electron beam is bunched by an r.f cavity-driven grid and operates as a Class B amplifier with a gain of between 18 and 23dB.

In this NAB paper Ostroff made a cost-of-ownership comparison between a klystron and a klystrode transmitter, concluding that the klystrode, with its higher efficiency, should provide a five-year cost-of-ownership advantage of \$100,000 at the 60kW level. The first operational use of a klystrode in a u.h.f. tv transmitter will be followed with interest by broadcast transmitter engineers around the world.

Klystrons

Not to be outdone in the klystron/klystrode debate, Dr Roy Heppinstall of EEV presented a paper entitled "Klystron operating efficiencies: Is 100% realistic?". Heppinstall warned that care must be taken when comparing the operating efficiency figures quoted for gridded klystrons, klystrodes and multi-staged depressed collector klystrons.

Defending the klystron, Heppinstall said that he expected that the figure of merit for a gridded klystron operating at optimum efficiency in a full-time modulated mode would be comparable with that of a klystrode or multi-staged depressed collector klystron.

New-comer

The NAB is held annually in the US. The two major European broadcast exhibitions (IBC in Brighton and the International TV Symposium in Montreux) are both held bi-annually on alternate years. This arrangement results in there being one major broadcast show on each side of the Atlantic every year.

This year there is a new-comer to the broadcast exhibition circuit; a new show, "Broadcast '86" is being launched in Frankfurt in late June.

However many broadcast shows there are in Europe, none of them will match NAB: the world's biggest broadcast show. ■

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AF127	0.65
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BC461	0.35
BC478	0.20
BC527	0.20
BC547	0.10
BC548	0.10
BC549A	0.10
BC550	0.14
BC557	0.08
BC557B	0.80
BC558	0.10
BCY33A	1.60
BD115	0.30
BD124P	0.59
BD131	0.42
BD132	0.42
BD133	0.40
BD135	0.30
BD136	0.30
BD137	0.32
BD138	0.30
BD139	0.32
BD140	0.30
BD144	1.10
BD150C	0.29
BD159	0.65
BD160	1.50
BD166	0.55
BD179	0.72
BD181	0.45
BD182	0.70
BD183	0.70
BD201	0.83
BD202	0.65
BD203	0.78
BD204	0.70
BD222	0.46
BD223	0.59
BD225	0.48

BD232	0.35
BD233	0.35
BD234	0.35
BD236	0.49
BD237	0.40
BD238	0.40
BD242	0.65
BD246	0.75
BD376	0.32
BD410	0.65
BD434	0.65
BD437	0.75
BD438	0.75
BD520	0.65
BD538	0.65
BD597	0.95
BD589	0.45
BD701	1.25
BD702	1.25
BD707	0.90
BDX32	1.50
BF115	0.35
BF119	0.35
BF119	0.35
BF127	0.39
BF154	0.20
BF158	0.22
BF160	0.27
BF167	0.27
BF173	0.22
BF177	0.38
BF178	0.26
BF179	0.34
BF180	0.29
BF181	0.29
BF182	0.29
BF183	0.29
BF184	0.28
BF185	0.28
BF194	0.11
BF195	0.11
BF196	0.11
BF197	0.11
BF198	0.16
BF199	0.14
BF200	0.40
BF241	0.15
BF245	0.30
BF257	0.28
BF258	0.28
BF259	0.28
BF271	0.26
BF273	0.18
BF336	0.34
BF337	0.29
BF338	0.32
BF355	0.37
BF362	0.38
BF363	0.65
BF371	0.25
BF394	0.19
BF422	0.32
BF457	0.32
BF458	0.36
BF459	0.36
BF467	0.68
BF494	0.45
BF495	0.45
BF595	0.23
BF597	0.25
BFR39	0.23
BFR81	0.25
BFR88	0.30
BFR90	1.50

BFR91	1.75
BFT42	0.35
BFT43	0.35
BFW92	0.85
BFX29	0.30
BFX84	0.26
BFX85	0.32
BFX86	0.30
BFX88	0.25
BFY50	0.21
BFY51	0.21
BFY52	0.25
BFY90	0.77
BLY48	1.75
BRY39	0.45
BR100	0.26
BR110	0.49
BR103	0.55
BRC4443	1.15
BT100A/0	20.85
BT106	1.49
BT116	1.20
BT119	3.15
BT120	1.65
BU105	1.95
BU108	1.69
BU124	1.25
BU125	1.25
BU126	1.60
BU204	1.55
BU205	1.30
BU208	1.39
BU208A	1.52
BU208D	1.85
BU3276	1.20
BU407	1.24
BU500	2.25
BU508A	1.95
BU526	1.90
BU80Y	2.25
BUY69B	1.70
MJ3000	1.98
MJE340	0.40
MJE520	0.48
MPSA13	0.29
MPSA92	0.30
MRF237	4.95
MRF450A	13.95
MRF453	17.50
MRF454	26.50
MRF455	17.50
MRF475	2.95
MRF477	10.00
MRF838	13.95
OC16W	2.50
OC23	1.50
OC28	1.50
OC29	2.25
OC32	2.25
OC42	0.75
OC44	0.75
OC45	0.55
OC70	0.45
OC71	0.55
OC72	0.85
OC75	0.95
OC81	0.50
OC171	3.50
R2008B	1.45
R2010B	1.45
R2322	0.58
R2323	0.66
R2540	2.48
HCA16334	0.90

RCA16335	0.80
SKE5F	1.45
TIP29	0.40
TIP29C	0.42
TIP30C	0.43
TIP31C	0.55
TIP32C	0.42
TIP33C	0.95
TIP34B	0.95
TIP41A	0.45
TIP41C	0.45
TIP42C	0.47
TIP47	0.65
TIP120	0.60
TIP125	0.65
TIP142	1.75
TIP161	2.95
TIP2955	0.85
TIP3055	0.55
TIS91	0.20
TV106/2	1.50
1N1308	1.35
2N2219	0.28
2N2222	0.29
2N2905	0.40
2N3053	0.40
2N3054	0.59
2N3055	0.52
2N3702	0.12
2N3703	0.12
2N3704	0.12
2N3705	0.20
2N3706	0.12
2N3708	0.12
2N3733	9.50
2N3733	2.75
2N3792	1.35
2N4427	1.95
2N4444	1.15
2N5294	0.42
2N5296	0.48
2N5298	0.60
2N5485	0.45
2N5496	0.95
2SA715	0.60
2SC495	0.80
2SC496	0.80
2SC1096	0.80
2SC1106	2.50
2SC1172Y	2.20
2SC1173	1.15
2SC1306	1.40
2SC1307	1.75
2SC1364	0.50
2SC1449	0.80
2SC1678	1.25
2SC1909	1.25
2SC1945	2.65
2SC1954	0.95
2SC1957	0.80
2SC1969	1.95
2SC2028	1.15
2SC2029	1.95
2SC2078	1.45
2SC2091	0.85
2SC2098	2.95
2SC2166	1.95
2SC2314	0.80
2SC2371	0.36
2SD234	0.50
3N211	2.95
3SK88	0.95

DIODES

AA119	0.80
BA115	0.13
BA145	0.16
BA148	0.17
BA154	0.06
BA156	0.15
BA157	0.30
BAX13	0.04
BAX16	0.06
BB105B	0.30
BT151	0.79
BY126	0.10
BY127	0.11
BY133	0.15
BY164	0.45
BY176	1.20
BY179	0.63
BY182	0.55
BY184	0.35
BY199	0.40
BY206	0.14

BY208-800	0.33
BY210-800	0.33
BY223	0.90
BY298-400	0.22
BY299-800	0.22
BYX10	0.20
BYX36-150R	0.20
BYX38-600R	0.60
BYX55-600	0.30
BYX71-600	1.10
BZY95C30	0.35
CS4B	4.50
CS10B	8.45
OA47	0.09
OA90	0.05
OA91	0.06
OA95	0.06
OA202	0.10
IN21DR	5.00
IN23B	5.00
IN23C	5.00
IN23ER	5.00
IN23WE	5.00

IN4001	0.04
IN4003	0.04
IN4004	0.05
IN4005	0.05
IN4007	0.06
IN4148	0.02
IN4448	0.10
IN5401	0.12
IN5402	0.14
IN5403	0.12
IN5406	0.13
IN5407	0.16
IN5408	0.16
ITT44	0.04
ITT923	0.15
ITT2002	0.10

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BZX61 Series	0.15
BZY88 Series	0.10

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ITT CVC30	8.25
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PHILIPS G11	13.99
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TELEFUNKEN 711A	11.15
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THORN 8000	23.50
THORN 9000	9.95
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Sanyo VTC 5500	3.75
Sanyo VTC 9300	3.75
Sanyo VTC 9300P	3.90
Sharp VC 6300	3.75
Sharp VC 7300	3.75
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Sharp VC 9300	3.75
Sony SL 3000B	3.75
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Sony SL C7/J7	4.00
Toshiba V5470	4.50

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SANYO ORIGINAL PART NUMBER	MODEL	DESCRIPTION	
4-529-10800B	VTC5150	Reel Motor 3.6W	9.95
4-527T-23501	VARIOUS	Motor Assy	9.75
4-527V-51000	5150	Capston Motor	29.95
143-0-4904-00900	FVHP615	Gear Idler Assy	5.95
143-2-457T-05900	VTC9455	Stopper Reel Base	0.55
143-0-545T-01701	VARIOUS	Pinch Roller Assy	8.95
143-0-545T-01700	VARIOUS	Pinch Roller Assy	1.95
143-0-551T-VTC9300		Idler Assy	0.95
143-0-661T-03800	VARIOUS	Loading Roller	0.95
143-0-662T-01201	VTC5150	Reel Drive Pulley	8.50
143-0-9974-00100	FVHP615	Mod Kit IC BA6304A	1.95

Video Head Cleaning Tape (VHS Automatic wet/dry)	6.50
Video Head Aerosol Cleaner	0.85
Video Copying Lead and Connector Kit Z/V	7.95

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S-3P Stairsteps 30 min.	49.50

EHT MULTIPLIERS

ITT CVC20	6.35
ITT CVC30	6.35
PHILIPS G8 550	6.96
RANK T20A	6.91
THORN 3000/3500	7.57
THORN 8500	8.00
THORN 9000	8.00
UNIVERSAL TRIPLER	5.45

VARICAP TUNERS

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ELC1043/06 MULLARD	8.65
U321	8.25
U322	8.25
U324	11.00

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PHILIPS G8 (550) 6-WAY	14.49

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200MA – 5 AMP	5p each

THERMISTORS

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VA1056S	0.23
VA1104	0.70
VA8650	0.45
VA1097	0.25

20MM ANTI SURGE FUSES

100MA-800MA	15p each
1A-5AMP	12p each

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HEAT SINK COMPOUND	1.00
FREEZE IT	0.95
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PUSH PULL MAINS SWITCH (DECCA, GFC, RANK, THORN ETC.)	1.02
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DET18	28.50
DET22	35.00
DET23	35.00
DET24	39.00
DET25	22.00
DET29	32.00
DF91	1.00
DF92	0.60
DF96	0.65
DF97	1.00
DH63	1.20
DH77	0.90
DH79	0.56
DH149	2.00
DK91	0.90
DK92	1.20
DL35	2.50
DL63	1.00
DL70	2.50
DL73	1.50
DL92	0.95
DL93	1.10
DL94	2.50
DL96	2.50
DLS10	13.50
DLS16	10.00
DM70	1.95
DM160	2.75
DY51	1.50
DY86/87	0.65
DY802	0.72
E80L	29.50
E81L	12.00
E82CC	3.50
E83CC	3.50
E83F	5.50
E86C	9.50
E88C	7.95
E88CC	3.50
E88CC Siemens Special	5.95
E19CC	7.95
E90F	7.95
E91H	4.50
E92CC	3.95
E99F	6.99
E130L	18.50
E182CC	9.00
E180F	6.50
E186F	8.50
E188CC	7.50
E1T	15.00
E280F	19.50
E283CC	10.00
E288CC	13.50
E810F	25.00
E1148	1.00
E1524	6.95
EA50	1.00
EA76	1.95
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EABC80	0.70
EAC91	2.50
EAF42	1.20
EAF801	2.00
EB34	1.50
EB41	3.95
EB91	0.85
EBC33	2.50

EBC41	1.95
EBC81	1.50
EBC90	0.90
EBC91	0.90
EBF80	0.95
EBF83	0.95
EBF85	0.95
EBF89	0.70
EBF93	0.95
EBL1	2.50
EBL21	2.00
EC52	0.75
EC70	1.75
EC80	9.50
EC81	7.95
EC86	1.00
EC88	1.00
EC90	1.10
EC91	5.50
EC92	1.95
EC93	1.50
EC95	7.00
EC97	1.10
EC157	475.00
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ECC32	3.50
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ECC81 Special Quality	0.65
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ECC83 Philips	1.95
ECC83 Siemens	2.50
ECC83 Tungsram	1.50
ECC84	0.50
ECC85	0.75
ECC86	2.75
ECC88	0.95
ECC91	2.00
ECC180	0.95
ECC189	1.95
ECC801S	3.50
ECC803S	4.95
ECC804	0.60
ECC2000	12.00
ECF80	1.15
ECF82	1.15
ECF86	1.70
ECF200	1.85
ECF202	1.85
ECF801	0.85
ECF805	2.50
ECF806	10.25
ECH3	2.50
ECH4	3.00
ECH35	3.50
ECH42	1.50
ECH81	1.00
ECH83	1.00
ECH84	1.00
ECH2000	1.50
ECL80	0.60
ECL82	0.79
ECL83	2.50
ECL84	0.74
ECL85	0.69
ECL86	0.95
ECL805	0.69
EF37A	2.50
EF39	1.50
EF40	4.50
EF41	3.50
EF42	3.50
EF50	2.50
EF55	4.95
EF70	1.20
EF71	1.50
EF72	1.20
EF73	1.00
EF80	0.55
EF83	3.95
EF85	0.50
EF86	2.25
EF86 Mullard	4.50
EF89	1.50
EF91	1.95
EF92	2.15
EF93	0.95
EF94	0.95
EF95	1.95
EF97	0.90
EF98	0.90
EF183	0.65
EF184	0.65
EF730	1.80
EF731	3.50
EF732	3.50
EF800	11.00
EF804S	19.50
EF805S	13.50
EF806S	14.50
EF812	0.65
EFL200	1.50
EH90	0.72
EK90	0.95
EL32	0.95
EL33	5.00
EL34	2.25
EL34 Mullard/Philips	4.50
EL36	1.95
EL37	9.00
EL38	4.75
EL41	3.50
EL42	2.00
EL81	6.95
EL83	5.95
EL84 Brimar	0.95
EL84 Mullard	2.95

EL85	4.50
EL86	1.25
EL90	1.75
EL91	6.00
EL95	1.75
EL153	12.15
EL183E	3.50
EL18P	3.50
EL360	6.75
EL500	1.40
EL504	1.40
EL509	5.25
EL519	6.95
EL802	3.65
EL821	8.50
EL822	12.95
EM1	9.00
EM4	9.00
EM80	0.70
EM81	0.70
EM84	1.65
EM85	3.95
EM87	2.50
EN32	15.00
EN91	1.95
EN92	4.50
EY51	0.80
EY81	2.35
EY83	1.50
EY84	5.95
EY86/87	0.50
EY88	0.55
EY91	5.50
EY802	0.70
EX35	0.75
EZ40	2.75
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EZ80	0.75
EZ81	0.75
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GZ33	4.50
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KT44	4.00
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KT61	5.00
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KT66 USA	9.95
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KT88 G Lion	18.95
KTW61	2.50
KTW62	2.50
KTW63	2.00
KTZ63	2.50
L102/2K	6.95
L102/2K	12.00
LB7-20	95.00
LS9B	6.95
M502A	60.00
M537A	60.00
M5143	155.00
M8079	6.00
M8082	7.50
M8083	3.25
M8091	7.50
M8096	3.00
M8098	5.50
M8099	5.00
M8100	5.50

M8136	7.00
M8137	7.95
M8161	6.50
M8162	5.50
M8163	5.50
M8190	4.50
M8195	6.50
M8196	5.50
M8204	5.50
M8223	4.50
M8224	2.00
M8225	3.95
ME1401	29.50
ME1402	29.50
ME1501	14.00
MH4	3.50
MHL6	4.00
ML4	4.50
MS4B	5.50
MU14	3.50
MZ1-100	125.00
N37	12.50
N78	9.85
OA2	0.85
OA2WA	2.50
OA3	2.50
OB2	0.85
OB2WA	2.50
OC2	2.50
OC3	1.50
OD3	1.70
OM4	1.00
QM5B	3.00
OM6	1.75
ORP43	2.50
ORP50	3.95
P61	2.50
P41	2.50
PABC80	0.50
PC86	0.75
PC88	0.75
PC92	3.50
PC97	1.10
PC800	1.10
PC900	1.25
PCC84	0.40
PCC85	0.55
PCC88	0.70
PCC89	0.70
PCC189	0.70
PCC805	0.70
PCC806	0.80
PCE82	0.80
PCF80	0.65
PCF82	0.60
PCF84	0.65
PCF86	1.20
PCF87	0.40
PCF200	1.80
PCF201	1.80
PCF800	0.40
PCF801	1.35
PCF802	0.60
PCF805	1.25
PCF806	1.00
PCF808	1.25
PCH200	1.50
PCL82	0.85
PCL83	2.50
PCL84	0.75
PCL85	0.80
PCL86	0.85
PCL800	0.80
PCL805	0.90
PE1-100	69.00
PEN25	2.00
PEN40DD	2.50
PEN45	3.00
PEN45DD	3.00
PNE46	2.00
PE06-40N	42.00
PFL200	0.95
PL21	2.50
PL36	0.95
PL38	1.50
PL81	0.72
PL81A	0.72
PL82	0.60
PL83	0.52
PL84	0.78
PL88	1.00
PL95	1.75
PL302	1.00
PL345	12.50
PL500	1.10
PL504	1.15
PL508	1.75
PL509	4.85
PL519	4.95
PL802T	3.50
PL820	2.95
PL5557	29.50
PY32	0.60
PY33	0.50
PY81	0.70
PY82	0.70
PY83	0.70
PY88	0.65
PY500A	1.95
PY800	0.79
PY801	0.79
QB3-300	54.95
QB3-1750	139.50
QB5-3500	495.00
QE03-10	4.95
QE08-200	145.00
QF40	65.00
QP25	1.00
QQE02-5	19.50
QQE03-12	7.95
QQE03-20	35.00
QQE06-40	45.00
QQV02-6	19.50
QQV03-10	5.50
QQV03-10 Mullard	15.00
QQV03-20	25.00
QQV03-20B	32.00
QQV06-40A	27.50
QQV06-40A Mullard	45.00
QQV07-50	63.50
QQZ03-20	42.50
QS75/20	1.50
QS75/40	3.00
QS92/10	5.00

QS95/10	4.85
QS108/45	4.00
QS150/15	6.95
QS150/30	1.15
QS150/45	7.00
QS1200	3.95
QS1202	3.95
QS1203	4.15
QS1205	3.95
QS1206	1.05
QS1207	0.90
QS1208	0.90
QS1209	3.15
QS1210	1.50
QS1211	1.50
QS1212	3.20
QS1213	5.00
QS1215	2.10
QS1218	5.00
QU37	9.50
QV03-12	5.75
QV05-25	1.75
QV06-20	29.50
QV08-100	145.00
QV2-2500	45.00
QY3-125	65.00
QY4-250	70.00
QY4-400	76.00
R10	4.00
R16	12.00
R17	1.50
R18	2.50
R19	2.50
R20	1.20
R1169	55.00
RG1-125	4.95
RG1-240A	14.50
RG3-250A	3.50
RG3-1250A	35.00
RK2K25	62.50
RK-208	12.00
RL16	1.50
RPL16	12.00
RPY13	2.50
RPY43	2.50
RPY82	2.50
RR3-250	15.00
RR3-1250	35.00
RS613	45.00
RS685	54.95
RSS688	52.15
S6F17	5.95
S6F33	28.95
S11E12	38.00
A30/2K	12.00
S104/1K	10.00
S109/1K	15.00
S130	5.59
S130P	5.95
SC1/800	5.00
SC1/1100	6.00
SC1/1200	5.00
SC1/1300	6.00
SC1/200	9.00
SP41	5.00
SP42	3.00
SP4B	4.95
SS501	35.00
ST11	1.50
STV280/40	11.95
STV280/80	19.95
SU42	4.95
TB2 5/300	85.00
TB2-300	45.00
TB3-2000	395.00
TD1-100A	25.00
TD03-10F	35.00
TD3-12	4.00
TDD4	5.50
TP25	1.50
TSP4	7.00
TT11	1.50
TT21	45.00
TT22	45.00
TT100	57.00
TTR-31MR	65.00
TY2-125A	85.00
TY4 400	85.00
TY8-600W	365.00
TYS2/250	375.00
U18-20	2.75
U19	11.95
U24	2.00
U25	0.90
U26	0.90
U37	9.00
U41	6.95
U50	2.00
U82	3.00
U191	0.70
U192	1.00
U193	0.65
U251	1.00
U801	0.75
UABC80	0.65
UAF42	1.00
UBF80	0.60
UBC41	2.25
UBC81	1.50
UBF89	1.00
UBL21	1.75
UC92	1.00
UCC84	0.70
UCC85	0.60
UCF80	1.00
UCH21	1.20
UCH42	2.50
UCH81	1.00
UCL82	1.75
UCL83	2.50
UF41	1.15
UF42	1.15
UF80	1.75
UF85	1.20
UF89	2.00
UL44	3.50
UL84	1.50
UL85	0.85
UU5	3.50
UU7	8.00
UU8	9.00
UY41	3.50
UY85	0.70
V235A/1K	250.00
V238A/1K	295.00
V246A/2K	315.00

V2406/1K	225.00
V241C/1K	195.00
V339	3.50
V453	12.00
VLS631	10.95
VP4B	4.50
VP133	2.00
VR75-30	3.00
VR101	2.00
V105/30	1.50
VR150/30	1.15
VT52	2.50
VU29	4.50
VU39	1.50
W21	4.50
W77	5.00
W729	1.00
W739	1.50
X24	4.50
X66/X65	4.95
X76M	1.95
XC24	1.50
XC25	0.50
XFW47	1.50
XFW50	1.50
XG1-2500	50.00
XG2-6400	135.00
XG5-500	22.50
XI1-5V	1.50
XL628FT	7.50
XNP12	2.50
XR1-1600A	49.50
XR1-3200A	79.50
XR1-6400A	115.00
Y502	25.00
Y65	6.95
YD1100	75.00
YJ1060	265.00
YL1020	29.00
YL1070	195.00
YL1071	195.00
YL1290	65.00
Z77	1.20
Z302C	12.00
Z359	9.00
Z505S	15.00
Z520M	4.00
Z521M	8.00
Z700U	3.00
Z749	0.60
Z759	19.85
Z800U	3.00
Z803U	18.95
ZA1000	12.50
ZA1001	1.50
ZA1002	1.50
ZM1005	8.00
ZM1020	6.00
ZM1021	8.00
ZM1023	7.95
ZM1041	14.00
ZM1082	9.00
ZM1084	10.00
ZM1177	9.00
ZM1202	55.00
ZM1263	4.00
ZM1612	3.00
1A3	4.50
1AC6	1.20
1AE	43.50
1B3GT	1.95
1B22	10.00
1B27	55.00
1B35A	45.00
1B63A	75.00
1C1	2.50
1C5GT	2.50
1FD1	2.50
1G3GT	2.50
1J3GT	2.50
1N2	4.50
1N5GT	2.50
1P28	25.00
1P39	19.50
1R5	0.90
1T4	1.00
1U4	1.75
1U5	1.00
1X2B	1.40
1Z2	8.95
2AS15A	11.50
2B7	1.50
2B22	69.50
2C39A	32.50
2C39BA	39.50
2C40	37.00
2C42	29.50
2C43	60.00
2C51	0.75
2CY5	1.50
2D21	1.95
2D21W	2.50
2E22	49.00
2E26	7.95
2J42	93.00
2J55	350.00
2K25	35.00
2K25 Raytheon	75.00
2K26	95.00
2K29	250.00
2K48	140.00
2K56	250.00
3A5	4.50
3A/107B	12.00
3A/108A	9.00
3A/109B	11.00
3A/110B	12.00
3A/141K	11.50
3A/147J	7.50
3A/167M	10.00
3A/2	3.95
3A3A	3.95
3A4	1.00
3AL5	0.95
3AT2	3.95
3B2	3.00
3B4	4.95
3B7	4.50
3B24	10.00
3B26	24.00
3B28	15.00
3BZ6	1.50
3C4	1.00
3C23	19.00
3C45	24.00

3CB6	1.50
3CN38A	2.50
3CS6	0.95
3CX3	2.50
3CY5	1.50
3D6	4.50
3D21A	29.50
3E22	49.50
3EH7	1.95
3EJ7	1.95
3V4	1.75
3W4GT	2.50
4B5518	115.00
4-65A	59.00
4687A	9.50
4-125A	72.50
4-250A	79.50
4-400A	87.50
4-1000A	425.00
4B32	35.00
4BQ7A	1.75
4BZ6	1.95
4C27	25.00
4C28	25.00
4C35	145.00
4C86	1.95
4CX1000A	425.00
4CX4000A	1100.00
4CX250B	49.00
4CX250B EIMAC	59.50
4D32	125.00
4CX250BN	75.00
4CX250K EIMAC	95.00
4CX125C EIMAC	125.00
4CX350A	95.00
4CX350F	79.50
4XC1500B	398.50
4E27	195.00
4GS7	2.25
4J52	75.00
4JC6A	2.95
4X150A	35.00
5A/102D	9.50
5A152M	9.00
5A163K	10.00
5A170K	6.25
5A-180M	9.00
5A-206K	10.00
5AMB	2.15
5ANB	1.20
5AR4	2.00
5AU4	1.50
5B 110M	10.00
5B-254M	14.50
5B-255M	19.50
5B-256M	15.00
5B-257M	15.00
5B-258M	14.50
5C22	125.00
5J180E	2500.00
5R4GB	3.50
5R4GY	3.50
5T4	5.95
5U4G	2.95
5U4GB	4.50
5V4G	1.50
5Y3GT	1.95
5Z4GT	1.50
6/30L2	0.70
6A/203K	9.00
6A7	4.95
6A8G	1.50
6AC7	2.00
6AG5	1.50
6AG7	1.95
6AH6	2.50
6AJ4	2.00
6AJ7	2.00
6AK5	1.95
6AK6	2.50
6AL5	0.60
6AM4	3.25
6AM5	6.00
6AM6	1.95
6AN5	4.50
6AN8A	3.50
6AQ5	1.75
6AQ8	0.85
6AR5	5.95
6AR8	3.95
6AS5	1.50
6AS6	2.50
6AS7G	4.50
6AT6	0.75
6AT8	1.75
6AU4	2.00
6AU5GT	4.50
6AU6	0.95
6AV6	0.75
6AW8A	2.50
6AX4GT	1.95
6AY3B	1.95
6AZ8	4.50
6B7	2.80
6B8G	1.50
6B10	1.95
6BA6	0.95
6BA7	4.50
6BA8A	3.50
6BE6	0.95
6BG6G	3.00
6BH6	1.95
6BH8	1.50
6BJ6	1.50
6BK4	4.00
6BK7A	1.95
6BL6	85.00
6BL8	1.15
6BM6	115.00
6BM8	0.58
6BN4	1.65
6BN6	1.65
6BN7	4.50
6BN8	3.95
6BQ5	0.75
6BQ7A	0.72
6BL7GTA	3.95
6BR5	0.70
6BR7	4.95
6BR8	2.15
6BR8A	2.15
6BS7	5.50

6BW4	1.50
6BW6	5.35
6BW7	1.50
6BW8	4.00
6BX6	0.48
6BX7GT	3.50
6BZ6	2.50
6BZ7	2.95
6C4	1.25
6C5	1.95
6C6	2.50
6C8G	1.50
6C11	2.50
6C18	2.50
6CA4	4.95
6CA7	3.50
6CB5	3.95
6CB6	1.95
6CD6GA	4.50
6CF6	1.50
6CG7	2.25
6CH6	6.95
6CL3	3.95
6CL6	3.25
6CL8A	1.50
6CN5	1.60
6CM7	2.95
6CS6	0.75
6CW4	6.50
6D6	2.50
6DC6	2.35
6DJ8	0.95
6DK6	1.50
6DQ5	5.95
6DQ6B	2.50
6DT6A	1.50
6DW4	2.15
6E5	3.95
6EA4	4.95
6EA7	2.50
6EA8	2.50
6EAB8	1.75
6EM5	2.50
6EM7	2.50
6EU7	1.95
6EU8	1.75
6EV7	2.95
6EW6	2.95
6EW7	4.50
6F1	2.00
6F5	4.95
6F6	2.50
6F6G	2.00
6F7	5.50
6F12	1.50
6F13	3.00
6F14	1.00
6F17	2.75
6F21	2.50
6F23	0.60
6F24	1.25
6F25	1.25
6F28	1.25
6F32	1.25
6F33	17.00
6FG5	1.95
6FQ7	2.95
6G6G	5.50
6GE5	3.95
6GH8A	0.80
6GK5	1.50
6GK6	1.95
6GS7	2.15
6GV7	2.50
6GW6	2.50
6GY5	3.95
6H1	9.50
6H3N	2.50
6H6	1.95
6H6GT	1.95
6HF5	5.50
6HF8	2.50
6HS6	4.95
6J4	2.15
6J4WA	3.15
6J5	2.50
6J6	2.00
6J7	4.15
6JB6A	4.50
6JE6C	5.50
6JU8	2.50
6JS6C	4.95
6J7G	4.15
6K7G	2.00
6K8G	3.00
6KD6	5.50
6KM8	2.50
6KT8	2.95
6L1	2.50
6L15	3.15
6L19	3.95
6L6GC	2.95
6L6GC(GE)	4.50
6L6GT	1.95
6LD20	1.15
6LF6	7.50
6LJ8	2.50
6LQ6	5.50
6N7	2.50
6N7GT	2.50
6P15	1.50
6P25	4.00
6P26	4.00

6P28	2.00
6Q7	1.75
6Q7GT	1.20
6R7G	3.15
6S4A	1.50
6SA7GT	1.35
6SC7	1.50
6SG7	2.50
6SH7	1.35
6SJ7GT	1.20
6SK7	1.35
6SK7GT	1.35
6SL7GT	0.85
6SN7GT	1.35
6SQ7	1.35
6SS7	1.95
6U4GT	1.75
6U6WA	3.50
6U8	1.15
6U8A	1.50
6V6G	1.25
6V6GT	1.50
6VGG	1.00
6X2N	1.00
6×4	1.50
6×5GT	1.00
6×5GTY	1.00
6×8B	2.25
7A6	4.50
7A7	2.00
7AD7	1.75
7AU7	1.50
7B6	3.50
7B7	2.50
7C5	2.50
7C6	2.50
7E7	2.50
7H7	3.50
7J7	5.50
7Y4	2.50
8B8	2.50
8B10	2.50
8BQ5	1.95
8FQ7	1.95
10D2	1.25
10DE7	2.50
10EW7	2.95
10F1	0.75
10GK6	1.95
10P14	2.50
10P18	0.78
10LD12	0.65
11E2R	45.00
11E3	55.00
11R3	5.50
12A6	3.95
12AD6	1.50
12AL5	1.50
12AT6	1.25
12AT7	1.15
12AT7WA	2.50
12AU6	1.50
12A17	0.65
12AV6	1.95
12AV7	2.50
12AX7GT	1.00
12AX7	0.65
12AX7WA	2.50
12AY7	3.95
12AZ7A	1.95
12B4A	4.50
12BA6	1.50
12BE6	1.95
12BH7A	2.50
12BL6	1.75
12BY7A	2.75
12C8	2.50
12CA5	1.95
12CX6	1.20
12DQ6B	3.50
12DW4A	3.50
12E1	17.95
12E14	38.00
12GN7	3.95
12HG7	4.50
12HG7A	4.50
12J5GT	3.95
12J7GT	3.50
12J28	2.95
12K5	1.95
12K7GT	1.50
12K8	1.95
12SA7GT	1.95
12SG7	4.75
12SH7	1.95
12SK7	1.95
12SJ7	1.95
12SQ7GT	1.95
12SN7GT	1.85
12SR7	2.50
12X4	1.95
13D3	3.20
13D7	3.20
13D9	3.20
13DE7	2.50
13DR7	2.95
13E1	145.00
13EM7	3.50
14S7	1.95
16GY5	2.95
17BE3	2.50
17DW4A	2.95
17EW8	0.95

17JZ8	4.50
18D3	6.00
18GB5	3.50
19AQ5	3.50
19AU4GT	2.50
19G6	9.00
19G3	17.00
19H4	35.00
19H4R	25.00
19H5	33.50
19Q6	9.00
20A2	10.50
20D1	0.70
20LF6	7.95
20L1	0.95
20P1	0.55
20P3	0.60
20P4	1.95
20P5	1.15
21LU8	2.50
24E1	39.50
25DQ6B	2.95
25L6GT	1.75
25EQ6	1.75
29C1	19.50
29KQ6	6.50
30C17	0.40
30C18	1.48
3F5	0.95
30FL1	1.00
30FL2	1.35
30FL12	0.95
30FL13	1.10
30FL14	1.25
30L1	0.45
30L15	0.60
30L17	0.60
30P4MR	1.00
30P12	1.00
30P18	0.60
30P19	1.00
30PL1	2.50
30PL13	0.60
30PL14	1.75
31JS6C	5.50
33A/158M	19.50
35A5	4.50
35LEGT	2.00
35Z3	1.85
38HE7	4.50
40KD6	5.50
42	6.95
47	6.00
50A5	1.50
50C5	0.95
50CD6G	1.15
50EH5	1.50
50JY6	2.95
52KL	2.00
53CG	15.00
61SPT	4.50
75B1	3.50
75C1	2.50
80	4.50
83	8.50
84	3.00
85A1	6.50
85A2	1.95
90AV	15.00
90C1	3.50
90CG	13.50
90CV	12.50
91AG	9.00
92AG	19.50
92AV	15.00
95A1	6.50
100E1	10.00
108C1	1.50
150B2	6.50
150C2	2.50
150C4	2.15
155UG	25.00
185BT	1.50
211	33.50
274A	15.00
307	5.00
328A	15.00
388A	17.50
425A5	8.00
431U	4.50
572B	55.00
705A	8.00
708A	8.00
715C	45.00
724A	275.00
726A	75.00
803	14.95
805	39.00
807	1.95
810	85.00
811A	15.00
812A	35.00
813	23.50
829B	14.50
833A	95.00
866A	6.50
872A	20.00
873	60.00
884	5.50
930	9.95
931A	13.95
954	1.00
955	1.00

958A	1.00
1299A	0.60
1619	2.50
1625	3.00
1626	3.00
2050W	6.95
2050	5.50
2051	5.50
3534	4.00
404A	10.95
927	15.00
1927	25.00
4212E	250.00
4313C	4.00
4328D	9.00
5636	5.50
5642	9.50
5651	2.50
5654	1.95
5663	1.95
5670	3.25
5672	4.50
5675	28.00
5678	7.50
5687	4.50
5692	3.50
5696	3.50
5704	3.50
5718	6.15
5725	2.50
5726	2.50
5727	2.50
5749	2.50
5750	1.85
5751	2.95
5763	5.75
5814A	3.25
5823	9.50
5829WA	6.50
5840	3.50
5842	11.00
5847	10.95
5879	5.00
5886	13.95
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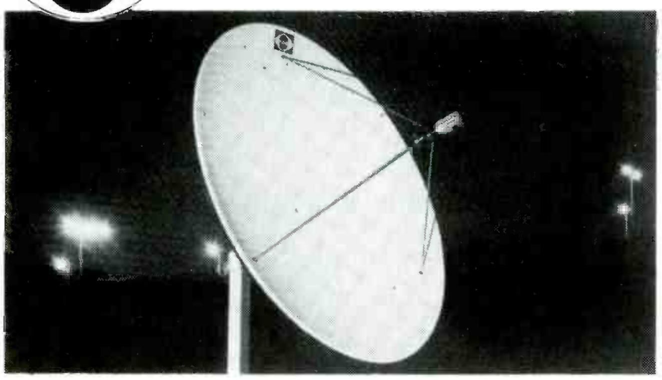

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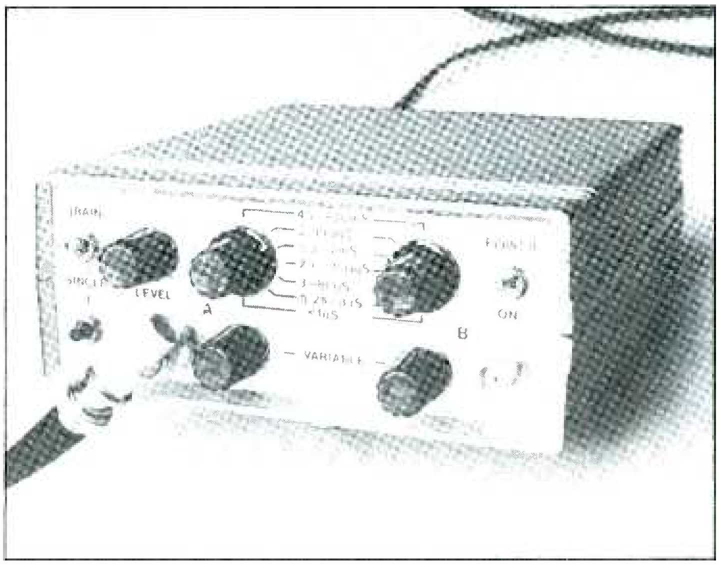
Simple pulse generator

by B.J. Frost, B.Sc., M.I.E.E.

Requiring only two i.cs and four power mosfets, this design provides up to 15V pulses at 1A, with rise times of less than 10ns.

Brian Frost graduated from Bangor University in 1974 with a degree in electronic engineering. He recently left Standard Telephones and Cables, where he was in charge of the design of automatic-test and manufacturing equipment and is now with Deltest Systems working on advanced, analogue-specific automatic-test equipment. He is a licensed radio amateur (G6UTN) and has completed a number of constructional projects, including a microprocessor-controlled 2m synthezised transceiver.

Other interests include an involvement with REMAP, a UK-wide network of engineers working voluntarily to make special aids for the disabled. In this field he is working on radio communication aids for the deaf.



A pulse generator should be capable of driving a wide variety of loads. This will always require more drive capability than is provided by the pulse generation logic and, as Fig 1 shows, divides the design of a pulse generator into two major sections: the pulse generation circuitry and the output stage(s). Within these two functional blocks there are several techniques that can be used.

Pulse generation. It is within this section that there exists probably the greatest number of possible options. Most designers can list at least six ways of generating logic pulses and this number is increased again when one considers the number of logic families available from which to choose actual devices. From this wide choice of circuitry it is necessary to choose a design that provides the pulse generation with the minimum number of components, yet provides the nearest approach to the list of ideals.

Having decided to generate a simple mark/space pulse system with no multiple-pulse or formal delay functions, one can employ any astable circuit that allows independent control of the mark and space time constants. Nevertheless the intended maximum/minimum pulse widths must be obtained with realistic components and the output from such circuitry should be interfaced easily to the output stage.

The 555 timer is worthy of first consideration but was ruled out for two reasons. Firstly, the timing capacitor is shared by the charge and discharge time constants, making wide independence between mark and space rather difficult, and secondly because the maximum speed of operation is not much in excess of 1MHz. This is understandable because of the use of internal analogue comparators for the threshold detections rather than logic components.

Commerical generators often go down to 10ns, but this is only achievable by using logic families based on 5V and, as I shall show when considering the output stage, this introduces extra difficulties. If a lower pulse width limit of 50-100ns is acceptable, the c-mos family offers some worthwhile simplification. It can accept a wide range of power-supply voltages (including 9V for portable use), and since the upper logic level of +15V always exceeds that of other families, the design of the output stage is very much easier when no there is no voltage step-up to be performed. In this way, the output stage becomes only a buffer and can be kept much simpler than otherwise.

A common device possessing the majority of the required features is the dual-monostable 4528. This comprises two independent monostables that are able to generate pulse widths from around 50ns to several seconds and, if they are coupled in tandem, form an adjustable mark/space system that can provide any combination of pulse timings.

Features

An output always obtained, irrespective of control settings.
Most pulse generators provide a delay function and set a pulse period with a width adjustment within this period. This does tend to cause users to set most generators with the aid of an oscilloscope, since it is very easy to get no, or double, outputs. A guaranteed output would be desirable.

Pulse range from <1μs to >1s

A generator that exceeds 1s in period is useful in allowing simple switching of relays or very low-speed devices.

Fully adjustable output voltage from 0V to 15V p-p

The generator is capable of enough output voltage and current swing to operate such items as relays, power mosfets (at full 15V gate drive), as well as correct operation of c-mos logic at full voltage.

Power output stage capable of 0.5A sink, >100mA source

It is desirable to have an output that would drive all the logic families, be fast, and also capable of driving small relays and power loads.

Switching times of 20ns

The ability of a generator to switch fast into capacitive loads allows it to be used with the increasing number of power mosfet devices that operate most efficiently at switching speeds of <100ns, but appear as a load often up to several thousand picofarads.

Two complementary, identical outputs.

The provision of two outputs is incidental from the simplicity of the design. In use however, the two outputs have proved to be useful for such things as push-pull drive, floating load drive of 30V p-p, and pre-trigger functions.

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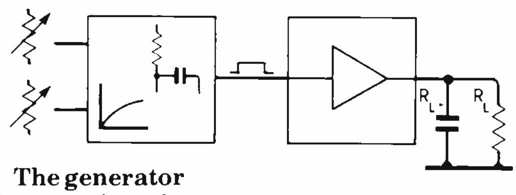


Fig. 1. The generator comprises two functions, generation and power output.

Fig. 2. Power mosfet is one example of a demoding load.

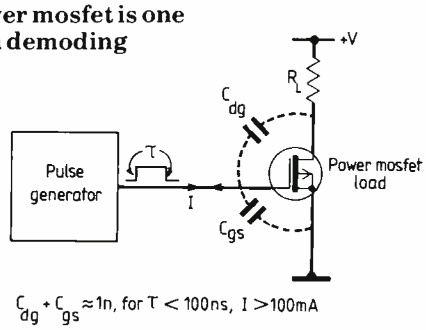


Fig. 3. Simplest output stage, with the effect of output capacitance on waveform.

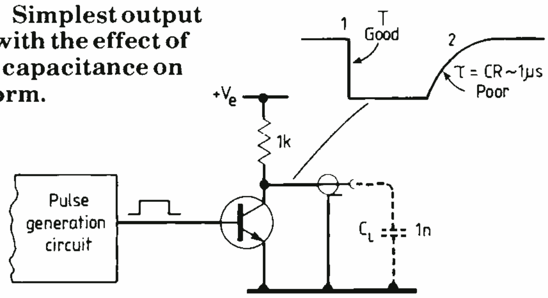


Fig. 4. Totem-Pole output offers an improvement, but speed still limited.

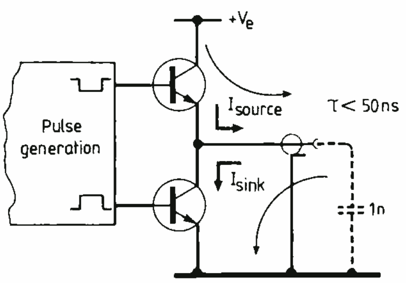
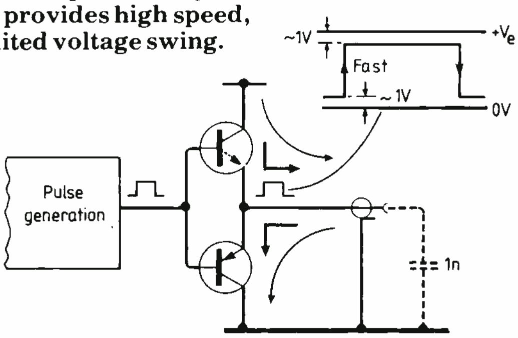


Fig. 5. Complementary output provides high speed, but limited voltage swing.



Using two monostables for the pulse generation results in front-panel controls that differ slightly from conventional generators. The usual period and width controls are replaced by two separate, A and B, pulse-width controls. This does not seem to present any problem; indeed it can be a definite advantage, in that it is not possible to set the pulse width greater than the period, as happens on some commercial generators, resulting in no, or double, pulse outputs. With this 'mark/space' technique, there will always be an output, however dissimilar the settings of mark and space.

There is an increased complexity caused by the need to ensure that the tandem connection of monostables always starts up, since it is possible that both monostable can be at rest and so not trigger one another. As will be seen, this can be accommodated within the circuitry that also provides a single-pulse facility. Were it not for this extra logic only the 4528 need be used; during testing, the tandem connection of monostables very rarely failed to start on power-up, but it is prudent to include protection for this eventuality.

Output stage. A good pulse generator should be capable of driving a wide variety of loads. Of these loads, the logic families themselves probably represent the easiest to drive, the most difficult being switching power devices and other reactive loads. Increased use of power-mosfet devices in switch-mode circuitry as in Fig 2 provides a load for which a good pulse-generator is required. The generator has to be capable of both sourcing and sinking currents that can drive the 1-3 nF of input capacitance with 10V logic signals at transition times well below 100ns. Simple calculation shows that this requires at least 100mA.

The problems of designing a good output stage for this generator are the same as those faced by the designers of all the logic families. A decision has to be made as to the relative tradeoffs between output switching speed, output voltage swing and load capacitance capability and ultimately the power consumed by the output stage that results.

Figure 3 shows the simplest output stage, based on one transistor. A pulse drives the base of the transistor, so turning it on and off. It is clear to see that when the transistor turns on, current can be 'pulled' out of the charged capacitive load through the transistor at a high level, certainly high enough to achieve a fast negative-going output transition (1). However, when the transistor is turned off, the positive transition (2) is entirely limited in speed by the load capacitance ($\approx$ 1000 pF) and the value of the pullup resistor (1kΩ), resulting in a sluggish rise with a time constant (CR) of 1μs. Obviously, this will make nonsense of pulse widths less than this. The situation can be improved by lowering the pullup resistor value but clearly this results in hot resistors and more current through the transistor and cannot improve matters by more than about one order of magnitude.

The circuit can be improved as shown in Fig. 4 by the use of an active load. This is the technique widely used in bipolar logic families and often called the Totem-Pole output stage. It operates by providing a complementary drive to the two output devices, one to sink current from the load during negative transitions and the other to source current to the load during positive transitions. This allows the load to demand almost as much current as it requires, but more importantly it allows the output stage itself to draw very little quiescent current when not actually switching, since both devices are never on at the same time.

Unfortunately this configuration is rather unattractive for our purposes. In using bipolar transistors in this way there are secondary charge storage effects limiting switching speeds, which makes the construction of such an output stage best left 'on-chip' to the logic i.c. designer. To obtain good switching times these transistors need attention to the amount of base drive, to the prevention of saturation and operation from a restricted supply rail such as 5V.

Another solution to output design is shown in Fig. 5 where two complementary transistors can be used in power-

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buffer stage without paying these switching penalties. In this connection, both transistors are connected as emitter-followers, with current taken through either the p-n-p during sink, or the n-p-n during source. This circuit owes its speed to the fact that neither transistor ever saturates, and this circuit is widely used for driving high-capacitance loads at fast switching speeds. Unfortunately for this application, the circuit is restricted in that the output cannot get to within nearer than 0.6V of either rail, and this limited lower voltage prevents it from interfacing to t.t.l.-type inputs.

C-mos logic uses another, similar, type of 'totem-pole' output stage, shown in Fig. 6. In this case the two devices are complementary mosfets. The drive pulse causes one device to switch off whilst the other switches on. Mosfets have no charge-storage time, thus inherent switching times are fast and assisted by the switching of the other device. As they switch from one to the other there is a short time when momentarily both devices are on, resulting in a current which flows from the supply to ground: the on resistance of the devices limits this current to millamps and it is of very short duration. The devices allow the output voltage to reach the supply rails.

In Fig. 7, discrete mosfet devices are used to build an output stage which has the benefits taken from several of the previous configurations. A complementary drive pulse is used to drive two n-channel power mosfet devices (VN10), so avoiding complementary devices. These are connected in the same totem-pole format as the transistors in Fig. 4. Use of the VN10 instead of bipolar transistors removes the speed limitations of saturation and storage time, and their 15V drive capability offers easy drive from existing c-mos circuits. The VN10 is a device with a 5 ohm on resistance, which makes it a device that combines medium input capacitance, easily driven by c-mos logic, yet which has a low enough on resistance to handle currents of up to 1A. With the output stage connected as shown, the output voltage is taken down close to ground and up to within 2-3V of the positive rail. Switching times of the VN10 are fast; measurements show transition times of around 5ns. An added advantage is that the 4528 monostable can directly provide the required complementary drive waveforms.

One major advantage of using mosfets is that adjustment of the output voltage is very simple. Because the gate voltage may range from −15V to +15V irrespective of the drain voltage, it is possible to drive the output stage from the 4528 whilst varying the upper mosfet drain voltage and so varying the output. The switching speed and on resistance remain the same.

This output stage is used for each of the two outputs from the generator with only a few modifications to permit reasonable matching into 50 ohm lines and protection against limited inductive spikes.

Complete generator

Figure 8 shows the complete circuit diagram. IC_2 is a single 4528 dual-monostable which generates the required mark/space waveform and directly supplies the output stage. In principle, the falling edge of one monostable pulse triggers the other monostable, thus a square-wave is generated where the 'mark' and 'space' are independently adjusted by the timing settings of each monostable.

The complementary outputs from each monostable are used to drive the output stages, each of which consist of two VN10 mosfets. Supply voltage to the output stages is made variable by the output level adjustment R_{20}. Protection against reasonable inductive overshoot is provided by D_3 and D_4, and R_{16} and R_{17} allow both outputs to reach +15V to fully drive 15V c-mos logic with reduced pull-up. Resistors R_9, R_{15}, R_{12} and R_{14} provide output current limiting and a reasonable match into 50 ohm co-ax. by subjective evaluation on test. (Sorry, trial and error!) Increased output current to more than 1A can be obtained if these resistors are omitted, but there is increased risk to the mosfets from unlimited load currents.

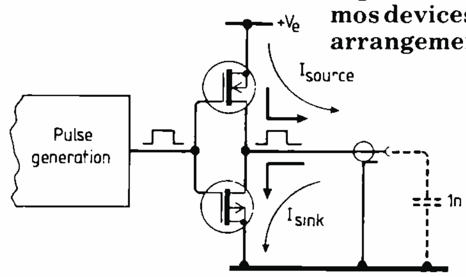

Fig. 6. Complementary mos devices in totem-pole arrangement.

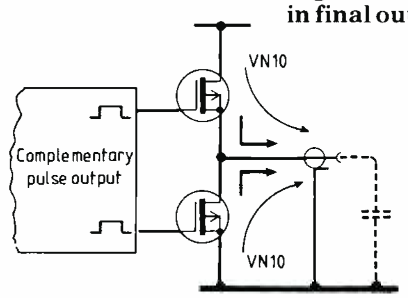

Fig. 7. N-channel mosfets in final output stage design.

Extra logic is provided by IC_1 to provide the 'single pulse' facility and to guard against the monostable outputs starting-up with no pulse from either output. Should this occur, IC_{1a} gates an oscillator (IC_{1b}) which injects an external trigger to the monostable if neither output is producing a pulse. IC_{1c} and IC_{1d} allow S_2 to trigger both monostables if a 'single' pulse is required. Closing switch S_1 disables the oscillator IC_{1b} via D_5 and biases the A input of the monostable into a high, untriggered state. Each press of the push button S_1 causes a negative-going edge to be coupled via C_{10} into the A monostable. This generates a composite output of an A pulse followed by a B pulse, allowing A to be used as a pre-trigger for B as the main output, if required.

Performance

Figure 9(a) shows the performance of the generator unloaded. A 100kHz 50.50 waveform shows rise and fall times of around 100ns. Figure 9(b) shows the effect of loading this same waveform with a 0.1μF capacitor. The output amplitute is reduced to 9Vp-p, showing an equivalent ouput impedance of around 50 ohms. This figure is largely due to the 15Ω resistors present in the output stages used to match into co-ax. lines and to provide some current limiting. If these resistors are removed, the 0.1μF is now discharged from 9V in less than 1us, showing the potential current sink capability of just under 1A (Fig. 9(c)).

The minimum pulse widths are <200ns, resulting in a square wave >2MHz. This pulse width can be further reduced to 50-80ns if an extra position is provided on the range switch where there is no timing capacitor. At this level though, the calibration is poor.

The generator will operate satisfactorily from any supply voltage from around 5V to 15V as shown in Fig. 10. As a mains unit it can be supplied from 15V, allowing the output voltage to be set from zero to this value. At 15V, the worst-case supply current is around 35mA, excluding any current that may be sourced to a load. Alternatively, the unit can be operated from a 9V battery, when the current falls by a factor of two and is around 5 mA for a 100kHz, 50:50 output. The supply current follows an unusual law and does not change as the pulse width changes unless the duty cycle differs significantly from 50:50, when the current can fall towards half the 50:50 value. In principle though, the low level of supply current does allow battery operation to an extent difficult to obtain with conventional pulse generators.

Figure 11 shows the variation of pulse width with supply

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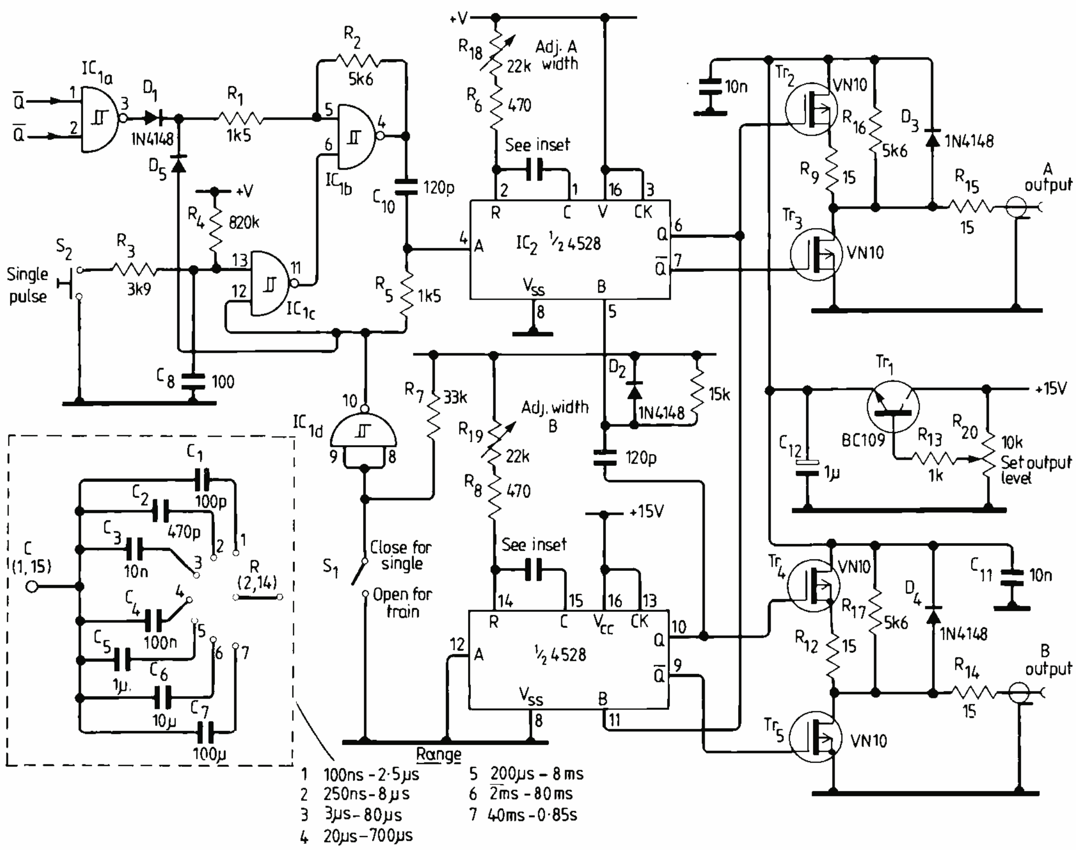

Fig. 8. Complete circuit diagram.

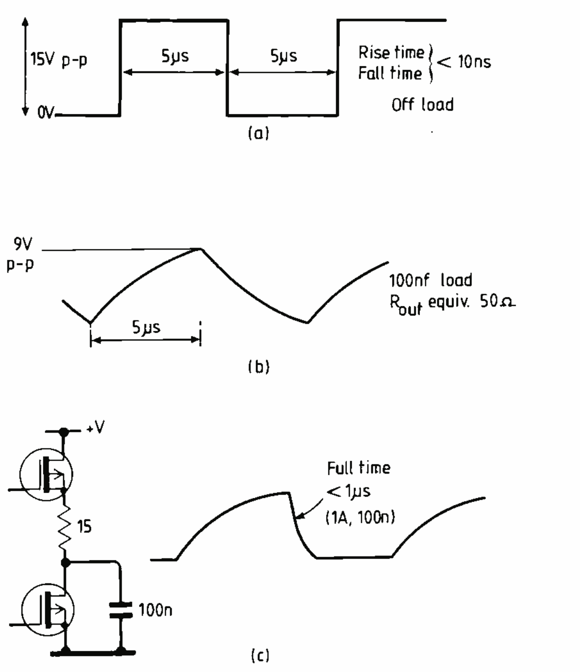

Fig. 9. At (a) is a 100kHz output waveform unloaded, while at (b) is seen the effect of a 1nF capacitor. Removing 15Ω matching resistors gives waveform at (c), the 9V, 1µs fall time indicating a current sink capability of almost 1A.

voltage. The generator is not a precision device and for operation between 15V and 9V a change in pulse width of around 15% can be expected. Take the supply to 5V and the width has increased by 20%. Note, too, that the output stage drive capability will be significantly lower for supplies below 7-8V, due to the falling gate voltage on the VN10s.

Construction and testing

There should be no particular construction difficulties due to the simplicity of the unit, but there are a few techniques during testing that can avoid possible damage to the output stages.

During construction, leave the VN10s in their packet and do not fit them into the circuit; more about the reasons for this later.

The timing capacitors can most conveniently be mounted on the switch itself. This reduces the wiring between switch and p.c.b. to only two wires per switch. Avoid runs of more than 150cm (6in) from either the timing switch or potentiometer, since this introduces extra stray capacitance, which will limit the minimum pulse width obtainable.

Do not omit the decoupling capacitors. Ensure that a 10n-100n capacitor is wired across the 4528 and that the same is wired across each of the output stages. Place a 10-100µF capacitor anywhere across the supply rails. When the pulse generator output changes state, currents of up to 1A will flow for times as short as 10ns. These current pulses must be met from the supply rails without the supply voltage falling or the operation of the unit can easily be unpredictable. At 10ns pulse widths a piece of wire more than a few centimetres long has enough self-inductance to cause a fall in voltage for more than a few mA of current. The only way of supplying these current pulses is to provide strategically placed 'reservoirs' of charge. It is from these decoupling capacitors – particularly the output stage decoupling – that the short-term pulse output capability of the generator will be met.

Any 15V or 9V battery supply will do, depending on the

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intended use of the unit: its current consumption is only some 20-30 mA at 15V.

Testing

The most annoying damage that can befall the unit is to have the output stage(s) fail. This occurs because one or more VN10s is faulty or is not driven in a complementary manner to its twin. In this situation it is typical for both VN10s in any one output stage and the level adjusting transistor Tr_1 all to fail. A post mortem is both unpleasant and avoidable by the following test procedure.

The VN10s should still be in their packet. Do not insert the 4093 and temporarily link IC_2 pin 4 to ground. This connects the monostable to oscillate by itself (assuming it starts) and allows the timing components to be checked without worry about the output stages or the restart circuitry.

Switch the circuit on and check for oscillation at pins 6,7,9 or 10. There may be occasions when it does not start, so switch off and then on again. Check that each switch range works, together with its variable control from end to end. A total generator range from around 1s to under 0.5μs should be obtained. If there are problems on the longer time ranges, check that the electrolytics are connected with positive to pins 2 and 14 respectively, and be aware that the accuracy of such electrolytics is poor and so may require substitution in some cases.

Remove the link on pin 4. Insert the 4093 and check the operation of the 'single/train' logic. Select pulse widths longer than about 100ms and switch from 'train', where the unit should happily self-oscillate, to 'single', when it should stop. Press the 'pulse' button, there should be one output pulse, immediately at pin 6 and delayed at pin 10.

If all is well, insert the first two VN10s. Experience shows that these are more static sensitive than c-mos and if only one is damaged, its twin will almost certainly go with it at switch-on. Immediately on removal from the anti-static packaging, wind some fine copper wire in a figure-of-eight between the leads just under the body. In this way the devices can be handled at will, soldered in, and the wire removed only at the last minute.

Fit the VN10s, Tr_3 and Tr_5 with their anti-static wires intact. When in place, remove these wires and apply power. Check that an output is obtained that varies smoothly with the level control from zero to 15V p-p. Note that faster waveforms will show a slow risetime because the positive edge is being obtained by the pullup resistors R_{16} and R_{17} instead of the upper VN10 devices. Verify that neither VN10 has suffered gate damage by checking that the gate drive voltage from pins 7 and 9 is a full 15V p-p. Damaged fets can still operate whilst loading the driving stage.

When this is done, fit the remaining VN10s, remove their anti-static wiring and apply power. An output should be obtained from both A and B sides of the generator that can be varied from zero to 15V p-p and is little changed at 1MHz by a 100pF capacitor placed on the output.

Calibration

Calibrating a unit such as this can present a problem. Defining a pulse width on any monostable by an RC time constant is always difficult when accuracies greater than 10% are required. Due to the nature of the 4528, the wide range of capacitors and the variable potentiometer, an accuracy of around 20% will be quite good. Various attempts have been made to devise a reliable means of calibrating but, to achieve good calibration, work will be necessary to adjust the values of each of the capacitors on the range switches against some known standard until satisfactory. One method of calibration is to find a common scale where several ranges can easily be made to agree within the required amount and then to scale the potentiometer accordingly. It then remains only to adjust the capacitors of the other ranges. All of this work is unpleasant and difficult so perhaps like myself, you may consider that if the unit will be used with an already calibrated oscilloscope, then it is only necessary to ensure that all ranges overlap. This arrangement results in a greatly simplified front-panel and is much less critical on the values of timing capacitors.

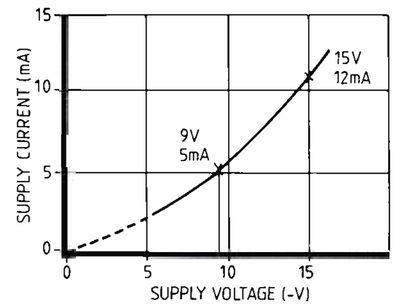

Fig. 10. Power supply current against voltage at 100kHz.

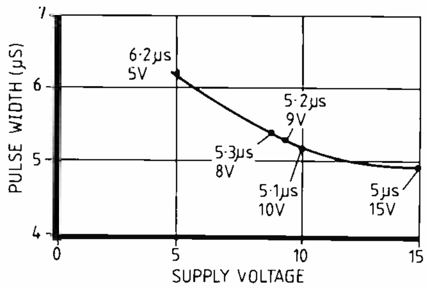

Fig. 11. Pulse width against supply voltage.

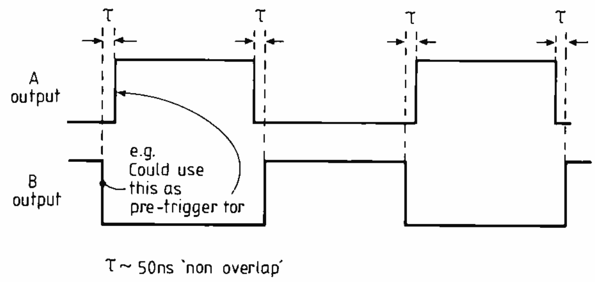

Fig. 12. Timing diagram of the two outputs.

Use

For simple, variable mark/space waveforms, either the A to B output provides a variable-level, adjustable-width pulse train when the single/train switch is set to 'train'.

Sometimes, due to their timing relationship, both outputs can be useful. See the timing diagram of Fig. 12, which shows that the two outputs can be considered as anti-phase or complementary at widths >1μs but that they are also non-overlapping. There is a fixed delay of around 50ns between every edge of A to every edge of B, irrespective of the pulse width set. This allows output A to be used as a pre-trigger for the main output taken from B. Triggering the oscilloscope from A will allow the complete positive edge of the output from B to be seen on a slower instrument. This is a useful function and saves having to provide a formal pre-trigger output.

With the single/train switch set to single, each press of the button provides one pulse from A followed by one pulse from B. Again, the main output can be taken from B using A simply to delay the output pulse or to provide the previously mentioned pre-trigger facility. Any combination of mark/space settings may be used; for example to generate a 1μs output pulse (from B) following a 1s delay from A. ■

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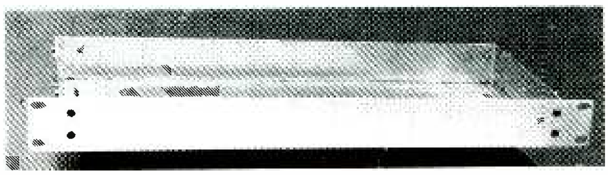

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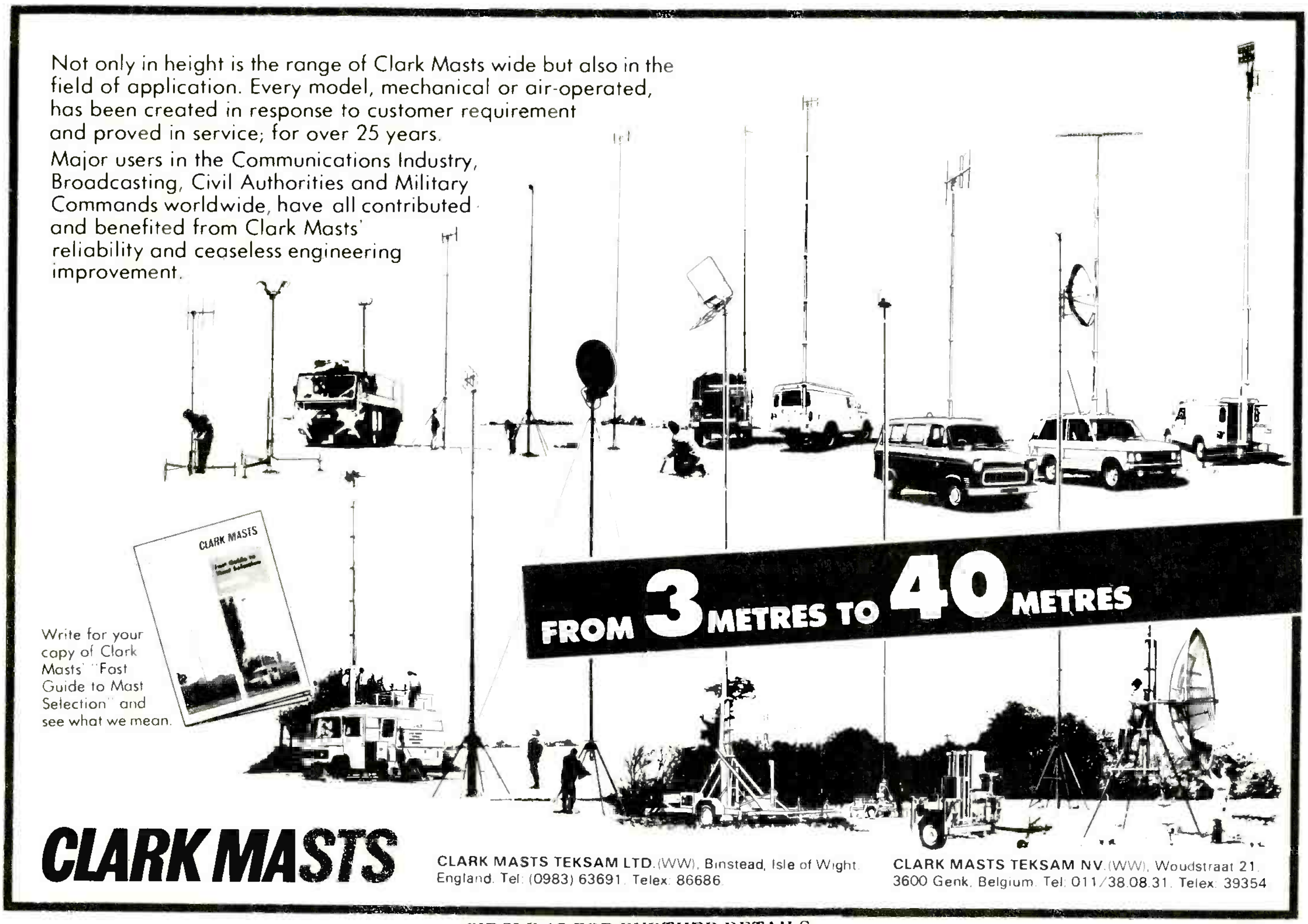

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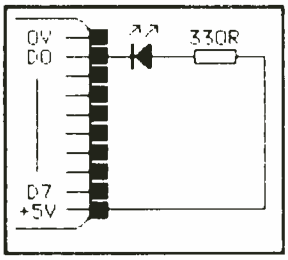
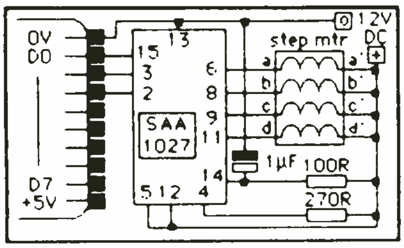
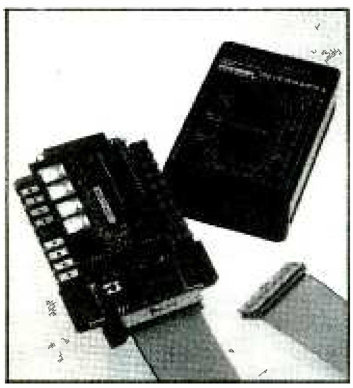




Applications simple (above) and more complex (below) for the output port of Interpack 1. Examples are from the instruction manual.



Interpack 1 includes an eight-channel a-to-d converter.

To order these units at the special prices arranged for readers of *Electronics and Wireless World*, turn to the coupon on page 74

Microcomputers make excellent data gatherers and controllers for automatic equipment. And many are so cheap now that it is no extravagance to dedicate them full-time even to relatively trivial tasks.

But linking a micro to external equipment is not always straightforward, especially if its i/o facilities are limited. So DCP Microdevelopments' range of interface units, the subject of our special offer this month, looks as if it could fill a widespread need.

Two main interface units are on offer. For simple control applications there is the **Interpack 2**, which adds to your computer six independent relay outputs for switching small motors or lamps, eight switch inputs and an auxiliary power output of about 4.5V (for leds, or for biasing opto-couplers). The relays have single-pole changeover contacts capable of handling 1A at 24V and their driver circuits are latched.

For more complex applications, the **Interpack 1** has eight analogue inputs for voltage measurement, eight t.t.l. input/output lines, four single-pole relay outputs and four switch inputs: a varied mixture which will satisfy almost every common requirement short of direct mains switching – though of course you could easily add secondary relays to do that. The a-to-d has a 10ms conversion time and gets its reference from a precision voltage source i.c.

Both Interpacks are fitted with an expansion port for connecting other input or output accessories or even a further Interpack.

A special feature of these interfaces is that the same units can be used with a variety of different computers, including Amstrad, Apple, BBC, Commodore and Sinclair Spectrum (IBM PC to be added to the list soon). Only a small personality board, which DCP call an **Intercard**, needs to be changed to match.

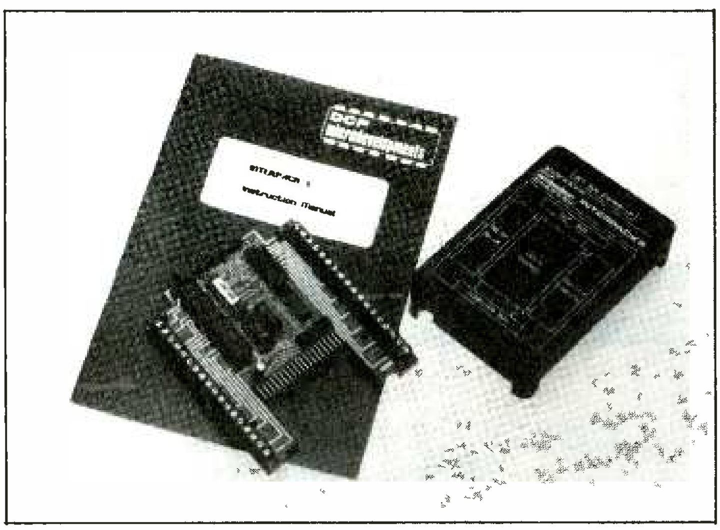
This card plugs into a recess in the main interface board and its flying lead connects to the host computer. As the instructions point out, such an arrangement is unlikely to withstand rough or very frequent handling; but it does mean that another Intercard can be substituted quickly and cheaply if the equipment needs to be transferred to a different computer.

All the p.c. boards are of glass-fibre and are compact and well made. A black plastics box supplied with each Interpack houses both it and the associated Intercard and carries a sticker identifying the terminals.

The instruction manuals go into plenty of detail and provide some interesting application ideas. For example, they show how to connect a stepper motor, and how you can sense light: for that, all you need is a light-dependent resistor across the input terminals.

No complete circuit diagram is given with either interface, but there are many smaller illustrations showing the internal connections of each port and typical configurations. Program examples are generalized, since the actual commands used will vary according to the computer: information about these is given in the sheet which accompanies each Intercard and there is space in the main manuals to note them down.

Both modules are priced very reasonably at a level which should find them a place in many laboratories and classrooms, and should encourage ZX81s and other workhorses to emerge from retirement for useful activity once again. Interpack 1 costs just under £40 and Interpack 2 just under £50.



Interpack 2 gives six change-over relays and eight switch inputs.

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S5/8 – the technical details

by Andrew Hardie

This universal serial interface offers a simple solution to computer interconnection problems.

The S5/8 standard specifies nine signals (eight poles plus screen), as follows:

DINP	data input
DOUT	data output
HINP	handshake input
HOUT	handshake output
SINP	subsidiary input
SOUT	subsidiary output
V+	power supply
GROUND	signal ground (common)
EARTH	earth

The data input and output carry the serial data stream. The handshake signals perform simple hardware flow control and V+, ground and earth are self-explanatory. (The subsidiary input and output are not to be used; they may be the basis of a future enhancement.)

Note that the S5/8 interface is defined at the mating face of the eight-pole socket on the D-device, with the input and output referring to the signal flow at that point, i.e. into and out of the D-device.

There is a defined relationship between DOUT and HINP, with HINP controlling the flow of data transmitted on DOUT. A logic 1 enables and a logic 0 disables transmission. A similar, but mutually independent, relationship exists betwen DINP and HOUT. The HOUT signal reflects the state of readiness of the device to receive data on DINP, logic 1 indicating ready and logic 0 indicating not ready.

Such hardware flow control is intended for simple applications and as a backup system. It is intended that more sophisticated configurations will use a software flow control protocol, i.e. using the data channels alone. However, the S5/8 specification insists that the handshake lines must still be present and functional.

Electrical aspects

The electrical characteristics of S5/8 are listed in the accompanying table. They can be satisfied by very simple circuits based upon a single high-speed c-mos logic device, such as an HC14 when operated from a single-rail power supply of +5V ±10%. Power consumption of this arrangement is about 1mA, considerably less than that required to power an RS-232C interface, especially where the bipolar voltages required have to obtained from a battery using a d.c.-d.c. converter.

High-speed c-mos devices have a symmetrical output impedance which makes them good at driving capacitive loads. Leading and trailing edges are slowed to the same degree so that, when the waveform is recovered at the receiver, it emerges almost identical to the original; it is merely delayed by the time constant of the load capacity and output impedance. Examples of receive and transmit circuits are shown in Figs 3 & 4.

Note that the data input is fitted with a pulldown resistor but the handshake input is fitted with a pullup instead, giving the ON condition.

The V+ power supply is an output on a D-device, able to supply up to 20mA at +5V ±10%, and an input to an S-device.

The signal ground is connected to the 0V (common) of both devices and is distinct from the earth which is used for screening and safety purposes.

Mechanical aspects

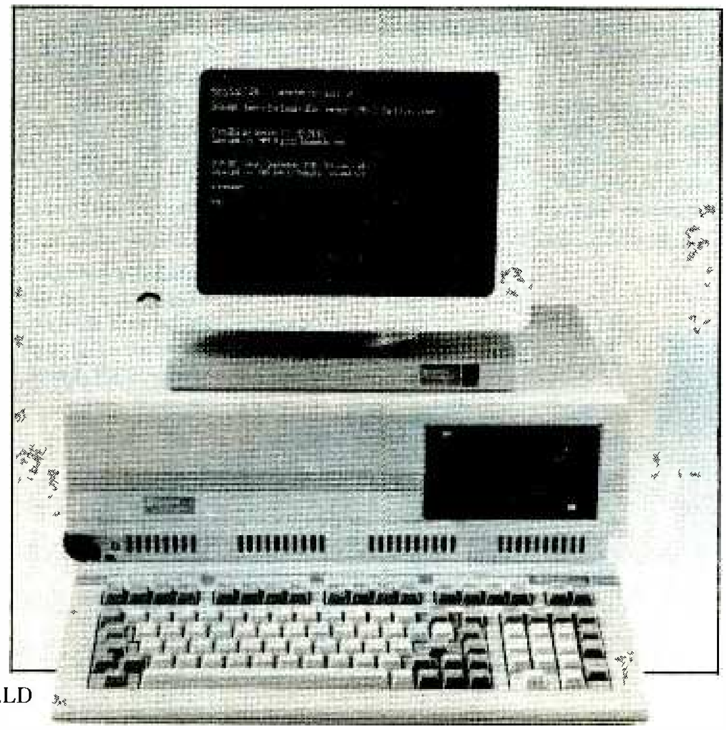
The connector specified for S5/8 is an eight-pole DIN connector, to the DIN specification 45326 (IEC 20 and IEC 21). The mating face of the socket is shown in Fig. 5. (Note that there is another type of eight-pole DIN connector, very similar to, but not inter-mateable with, the 45326 type. It is not

Andrew Hardie is research director of Oval Automation Limited and is a member of a number of standards committees and user bodies, including the BSI committees IST/18/1 (text and office systems) and IST/6/7 (interconnection of equipment), a user group on Integrated Services Digital Networks (ISDN) and a manufacturers' group, the British Office Technology Manufacturers' Alliance.

In his role as technical consultants to the Public Services Working Party he advises on floppy disc standards and was responsible for devising the S5/8 interface.

In last month's article Andrew Hardie outlined the drawbacks of the serial and parallel interfaces commonly used for digital data transfer between computers and peripherals, and proposed S5/8 as a replacement.

In an era when uarts are cheap and multi-pin connectors expensive, he explained, S5/8 with its low-cost eight-pole DIN connectors makes better economic sense. Its data transfer rate, fixed at 9600 bit/s, is fast enough for almost all applications other than printer buffers. And its simple, universal design puts an end to the need for reversing cables and breakout boxes: a single type of cable should meet all interconnection requirements.



An early recruit to the S5/8 camp is Gemini's Challenger computer. This 12MHz 68000-based machine has two S5/8 ports as standard.

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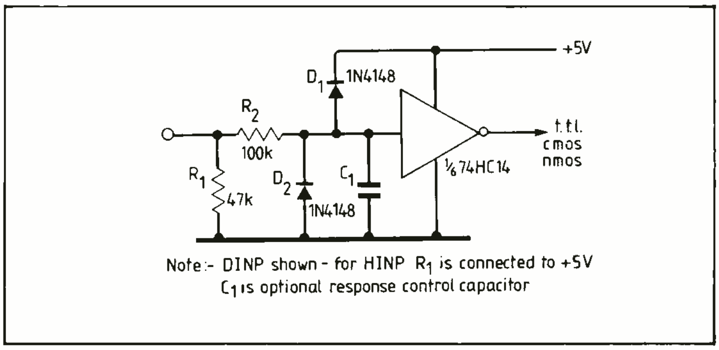

Fig. 3 Line receiver circuit. S5/8's low power requirement makes it especially appropriate for battery portable equipment.

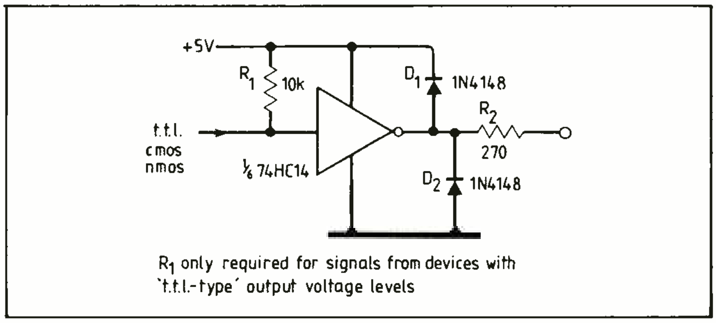

Fig. 4. Line driver circuit.

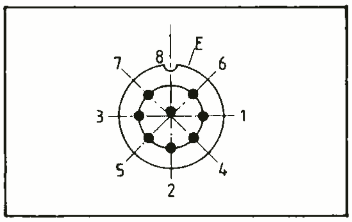

Fig. 5. Socket pin numbering (mating face view). S5/8 is based on an eight-pole DIN connector, but leads fitted with five-pin plugs will suit most purposes.

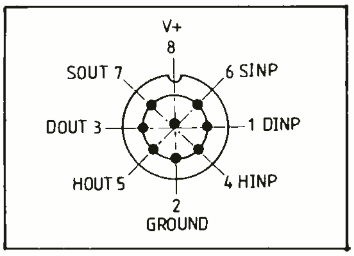

Fig. 6. Socket contact assignment. Poles 6 and 7 are reserved for future use.

widespread, but is used on some audio-visual equipment of Far Eastern origin.)

These connectors are now readily available from sources such as RS Components and Verospeed, and will accept either eight-pin plugs or five-pin, 180° plugs. They are cheap, compact, lightweight, widely available in a variety of styles and qualities to suit the application. And they are available screened, a factor of increasing significance.

The assignment of poles is shown in Fig. 6. Input and output signals are paired on opposite sides of the connector, as in audio practice, with the common on pin 2. A five-pin plug connects only to the DINP, DOUT, HINP, HOUT, and GROUND signals.

The peculiar numbering on the DIN connector is historical. It started life with three pins in, out and common. Then someone invented stereo and an extra input and output had to be added, and the eight-pin just logically follows on from that.

When inter-connecting D-devices, the SINP and SOUT are not used and the V+ signals must not be connected together as any voltage difference between the regulators at each end will cause a large current to flow. The solution to this is to use five-pin plugs for the D-device to D-device interconnection cable. This cable is illustrated in Fig. 7. It is a plug-to-plug reversing cable, very similar to a mirror audio cable but with a separate screen.

This cable is thus the only type the user needs. Compared with cables using 25-way D-types or 36-way Amphenols and multicore cable, it is cheap, lightweight and compact, of particular importance for portable equipment.

The S-device captive cable is similar, but with the use of the eight-pin plug and the incorporation of the V+ line. It is shown in Fig. 8.

A length of 1.5 metres is suggested for the D-device to D-device free cable and the captive S-device cable, but any convenient length can be used, subject only to the maximum load capacity specification. Since no length is ever right for every application, extension cables are also specified, as shown in Fig.9. They are non-reversing, six-circuit plug to socket cables. Any number can thus be used between D-devices and S-devices or other D-devices.

The V+ connection is preserved in connections from D-device to S-device, but is broken by the five-pin plug-to-plug cable that must be used to complete the connection between two D-devices. All three cables can use the same type of 6-core screened cable.

Data structure

The data structure is the familiar start-stop (asynchronous) mode serial frame, as used by all uarts, and in the same sense as RS-232C: the line rests low and goes high for the start bit and the transmitted data bits are inverted. However, in contrast to RS-232C, the data structure is standardized as one start bit, eight data bits, no parity bit and one stop bit, giving a 10-bit frame (Fig. 10). Error detection is more efficiently performed using block methods, such as checksum or c.r.c. The addition of a parity bit slows the effective data transfer rate by 10%.

Signalling rate

The data signalling rate, or bit rate (often referred to incorrectly as the baud rate), yet another variable in the RS-232C equation, is specified at 9600 bit/s. This is the fastest widely-used bit rate and is a *de facto* standard with many suppliers, such as DEC and Intel.

Flow control

Only the simple hardware flow control provided by HINP and HOUT is specified in the S5/8 standard. No specification has been produced yet for software line flow-control protocols. These may be the subject of a future related standard.

The question of protocols for asynchronous lines has recently been attracting interest and an ad-hoc group has been formed to examine the requirement for such a system, particularly in the context of providing an Open Systems Interconnection (OSI) network service. Readers with strong views on the subject are invited to contact the author, via

Behind the Gemini Challenger: a serial expansion board (fourth from right) gives a further four S5/8 ports.

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the editor. You could have the opportunity to provide a user view on the requirement.

Data coding

Similarly, the S5/8 standard makes no specification about the meaning of the data transferred across the interface. It merely provides transfer of binary octets (bytes) without loss or change of information.

This is perfectly satisfactory for non-imaging devices and applications, but otherwise an agreed meaning for the data must exist. Just specifying Ascii is almost meaningless. Character coding is now much more complex, with considerations such as national variants, graphic characters and control codes for imaging devices all to be taken into account. A major international standard is emerging to encompass all this, and more. It is ISO-6937, it exists in three parts at the moment, with several more parts in the pipeline.

Retro-working

Although it is intended that S5/8 should become a widely used standard on desktop p.cs, portable computers and peripheral devices, perhaps assisted into the market by user pressure for a simple interface scheme, interworking with existing equipment will be required in the transition period.

For interworking with Centronics-type equipment, serial-to-parallel converters (and, occasionally, the reverse) will be required. These can be constructed as s-devices. Two types have already been manufactured, one a simple uart-based device and the other using a c-mos single-chip micro to provide data buffering and flow control conversion.

For interworking with RS-232C it can be seen from the electrical characteristics that an S5/8 output constructed using a 5V high-speed c-mos gate is *not* guaranteed to drive an RS-232C input, which has specified thresholds of ±3V. Accordingly, the S5/8 specification has been written to allow bipolar outputs (up to ±7V, but ±5V preferred), without actually specifying them. With mains powered equipment, the provision of such bipolar supplies is less of a problem than in battery portable equipment.

An S5/8 input, on the other hand, will safely and correctly receive RS-232C signal levels. Accordingly, manufacturers of existing RS-232C equipment can simply change the connector to an eight-way DIN socket (cheaper, smaller and easier to mount), retain the bipolar output voltages (able to drive both RS-232C and S5/8) and change the input receiver to an HC Schmitt gate (able to receive S5/8 and RS-232C).

True S5/8 devices, particularly battery operated equipment, will then interwork with such hybrid devices and, of course, with each other, but are not guaranteed to interwork with current RS-232C devices. This approach will allow S5/8 to migrate into widespread use. The hybrid bipolar output arrangement will then no longer be required and can be discarded.

Obviously, retro-working with existing RS-232C devices may require support for lower bit-rates than the specified 9600, but the intention is eventually to have intelligence in all devices with flow control to regulate the data transfer and rate adaptation where necessary, for example, in modems.

Who is using S5/8?

S5/8 arose out of a Government study into the required specifications, including interconnecting, for a portable micro-computer for the Public Service. The machine that emerged as the result of that study, the Thorn-EMI Liberator has two S5/8 interfaces, allowing full benefit to be obtained from the space and power saving offered by S5/8.

Transam Microsystems chose S5/8 for the serial interface on their unique M1 intelligent modem for cellular radio.

Gemini computers have adopted the hybrid (bipolar output) approach, also using the space-saving features of S5/8 to provide four serial interfaces on a single card for their Challenger computer.

The latest recruit to the S5/8 interface is British Telecom, whose advanced QWERTY-phone loudspeaking feature telephone and terminal incorporates two S5/8 interfaces for connection to printer and desk top computer.

Within my own company, Oval Automation, S5/8 has been incorporated into a number of computer peripheral and add-on products, including c.r.t. display adaptors for portable computers, protocol converters, line adaptor units, intelligent interface converters and serial-interface disc drive units. ■

S5/8's electrical characteristics

Inputs:
Input resistance: 47KΩ
Input low threshold: +0.9V maximum
Input high threshold: +3.85V minimum
Input protection: ±25V minimum

Outputs:
Output low voltage: +0.15V maximum
Output high voltage: +4.35V minimum
Capacitive load drive capability: 2500pF minimum
Short-circuit protection:
to any other signal on the interface

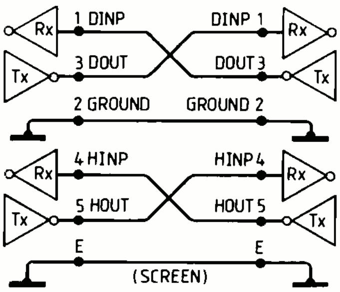

Fig. 7 (left). Standard S5/8 interconnecting cable. This one type will satisfy nearly every requirement.

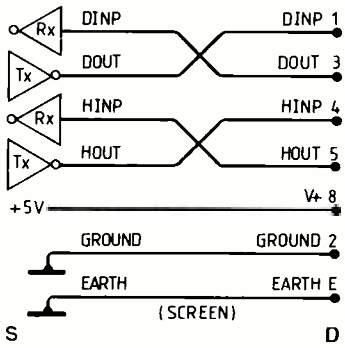

Fig. 8 (above). S5/8 captive lead for s-devices, which are those with no built-in power supply.

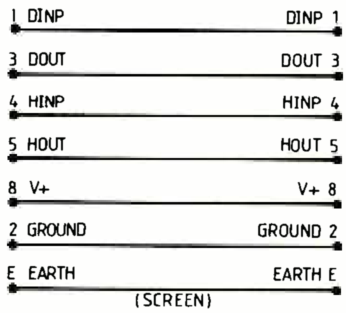

Fig. 9. Extension cable, suitable for insertion at the points labelled X in Figs 1 & 2 last month.

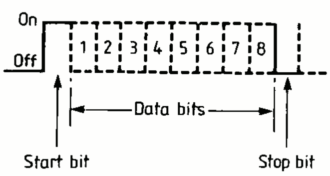

Fig. 10. Frame composition of S5/8 data. No parity bit is included because error-correction is intended to be done block-by-block. Sending rate is normally fixed at 9600 bit/s.

S5/8 devices

The relationship between devices transferring data over an S5/8 link is equal. There is no master and no slave, nor is there any polarization with one device regarded as the sender and the other as the receiver. But the S5/8 specification divides devices into two categories according to their power supply provision.

An s-device has no supply of its own, but may draw up to 20mA over the interface through its captive lead. Typical s-devices are mice and joysticks.

Nearly all computers and other peripherals are powered by mains or battery and are classified as p-devices.

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APPLICATIONS SUMMARY

Most manufacturers in the electronics industry spend large amounts of time and money on developing and describing applications for their products. To keep you informed, we will be publishing extracts from these notes from time to time. Readers wanting more information about particular notes need only circle the appropriate Reader Enquiry Service number.

Communications terminal unit

The 65-series of microprocessors includes a device especially for telephone-line signalling and data-transmission, produced by GTE. Note 3009-04-02 describes using this microprocessor, the G65SC150 communications terminal unit, as the heart of a Bell 103, 300 baud modem.

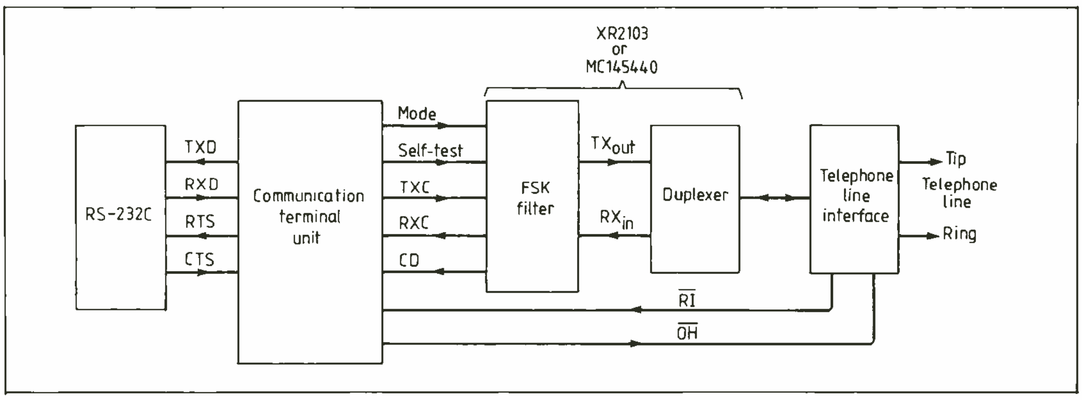
General-purpose as well as modem-specific software includes page-zero data assignment, clock-updating, uart parallel/serial data conversion and modem-initialization routines.

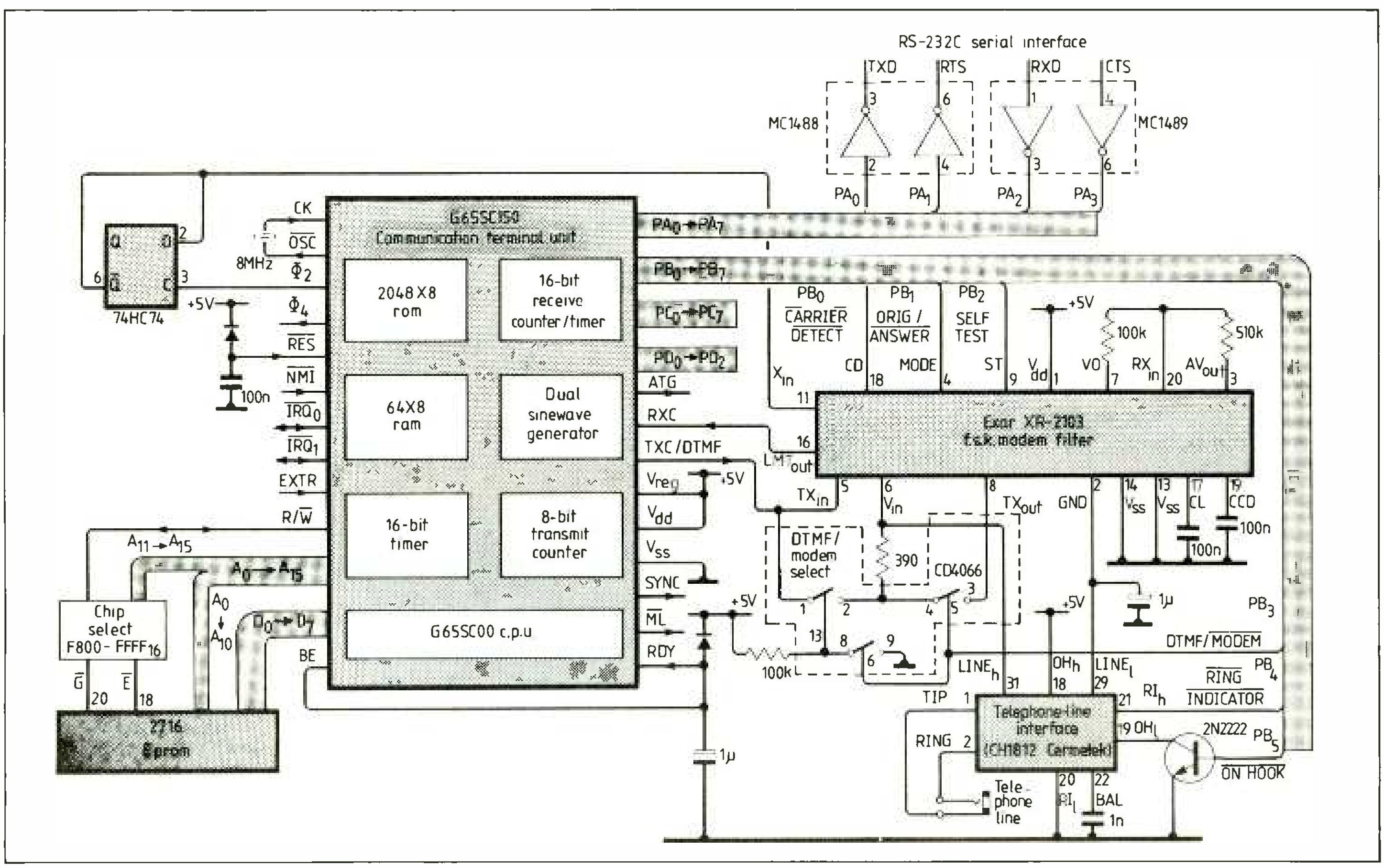
Unless you intend communicating with US databases, the Bell standard is not much use in the UK but the software is in assembly-language form with comments, so it should be a relatively simple matter to convert the design for European use. The processor can be used to control either d.t.m.f. or pulse dialling and is suitable for rates of up to 600 baud.

There is no equivalent modem filter for V21 from Exar — the company decided that the European market was too small — but there are pin-incompatible filters that do the same job, such as the RM5361AP from E.G. and G. Reticon.

Exar devices are available from Microcall, via Midwich in small quantities, and Cermetek products are distributed by Dialogue.

EWW300





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32-bit computer design

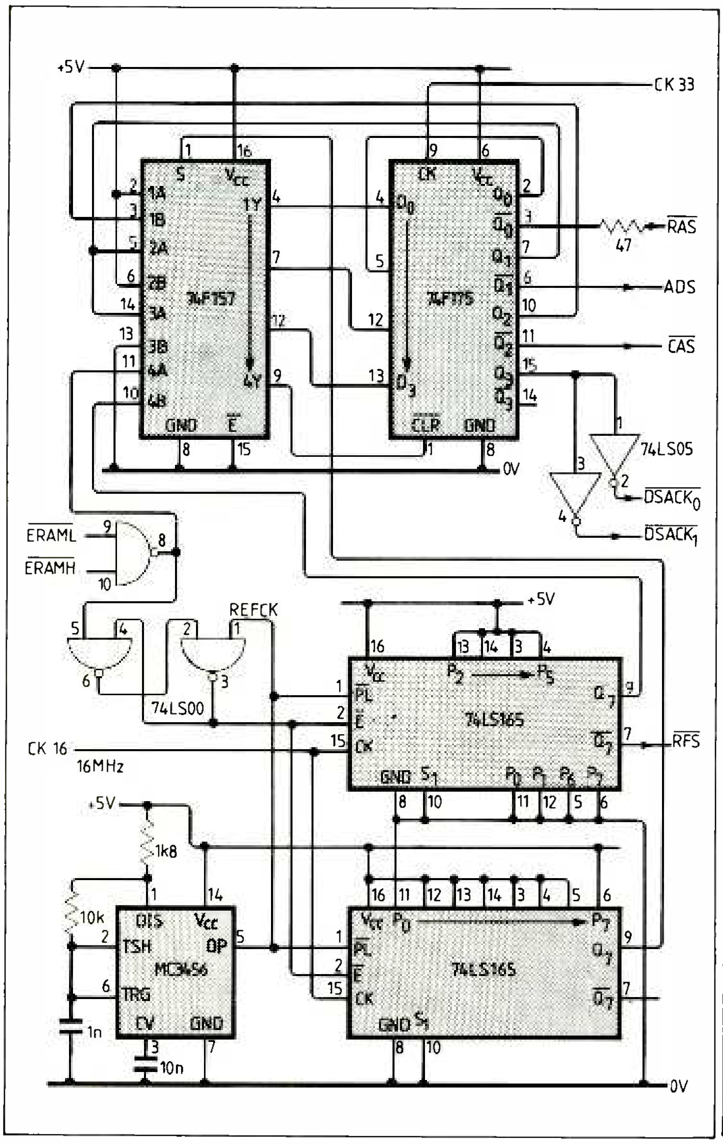
Hardware for a small 68020 computer with a 68881 floating-point coprocessor and 68851 paged memory-management unit is described in Motorola application note ANE001/D.

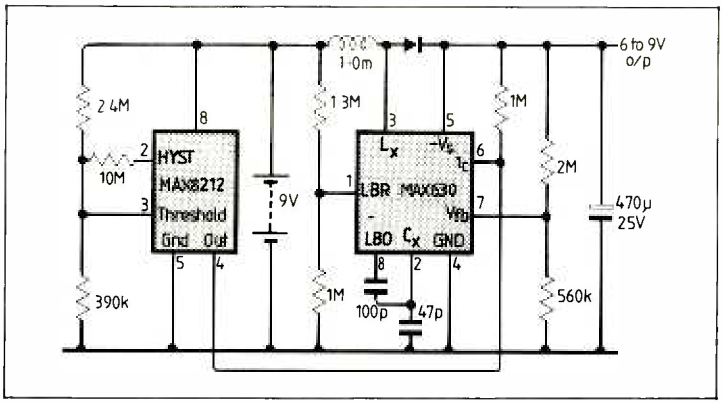
Peripheral devices in the design include a 68681 dual uart, providing two RS232 serial ports, and a 68230 parallel interface/timer for printer control and timing. A random-logic controller interfacing 32, 256Kbit dynamic rams is used, and there is decoding for 64Kbyte of firmware eprom.

This circuit (bottom) is the dynamic-ram refresh controller for producing row-to-column changeover signal ADS, row and column address strobes $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ and d-ram data-transfer acknowledge/port signals $\overline{\text{DSACK}}_{0,1}$.

Whenever the c.p.u. accesses memory, a $\overline{\text{RAS}}$-before-$\overline{\text{CAS}}$ sequence is used: in this mode, $\overline{\text{ERAML}}$ or $\overline{\text{ERAMH}}$ allows a zero logic level to propagate through successive Q_n outputs of a 74F175 quad D-type bistable device, asserting d-ram control signals on successive postitive-going clock edges.

Refreshing occurs every 15µs under control of REFCK. Negative-going edges of this clock signal initiate a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ sequence and the order in which the d-ram control signals are generated changes.
EWW301





Longer battery life

An efficient switching regulator can be used to increase useful battery life by making supply voltage largely independent of battery voltage.

This circuit, part of the Maxim application/date sheet for MAX630 c-mos d.c.-to-d.c. regulators, continues to supply a minimum of 7V until the 9V battery level falls to 2V.

When battery voltage is above 7V, the 630 is disabled and draws only 10nA. Switch current of the 630 is 150mA and the device can operate from supplies of up to 16.5V.

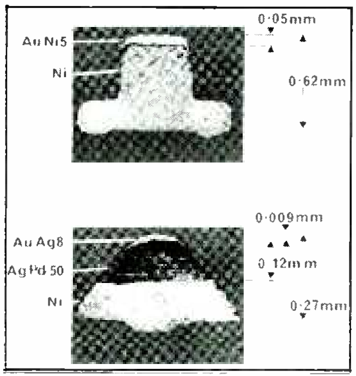
Other applications in the note include voltage converters, an uninterruptible 5V supply and two-rail regulators.
EWW302

Using discrete contact surfaces

In low and medium-power contacts for high-volume production, contact points can be a separate piece of metal called a 'microprofile' which is welded to the main contact element.

Accurate positioning of the contact point is possible using this approach, so money can be saved on precious-metal coatings. According to a note called "The application of microprofiles for electrical contacts" from Inovan, additional production costs through using microprofiles are nearly always outweighed by savings in precious metal. And profiles can be accurately formed, which allows a further reduction in coating area.

The four-page note briefly discusses contact requirements, savings in precious metal, production/quality and contact design. A list of contact materials and their characteristics is included.
EWW303



Cross sections of two contact profiles, one 1mm wide and the other 0.66mm wide. Close control of metal-layer thickness and contact profile minimizes precious metal use.

Addresses

GTE Microcircuits
Montenstrasse 11
8000 Munich 19
West Germany

Inovan
Technical Elements
136 Lawford Lane
Rugby
Warwickshire
CV22 7JT

Supertex
Dialogue Distribution
Wieat House
403 London Road
Camberley
Surrey GU15 3HL

Motorola Ltd
European Literature Centre
88 Tanners Drive
Blakelands
Milton Keynes
MK14 5BP

Samsung (UK) Ltd
6th floor
Victoria House
Southampton Row
London WC1

EG & G Reticon
34 Market Place
Wokingham
Berkshire RG11 2PP

Microcall Ltd
Thame Park Road
Thame
Oxfordshire OX9 3XD

Thame Midwich Ltd
Gilray Road
Diss
Norfolk IP22 3EU

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CIRCUIT IDEAS

Fast, balanced Schmitt trigger

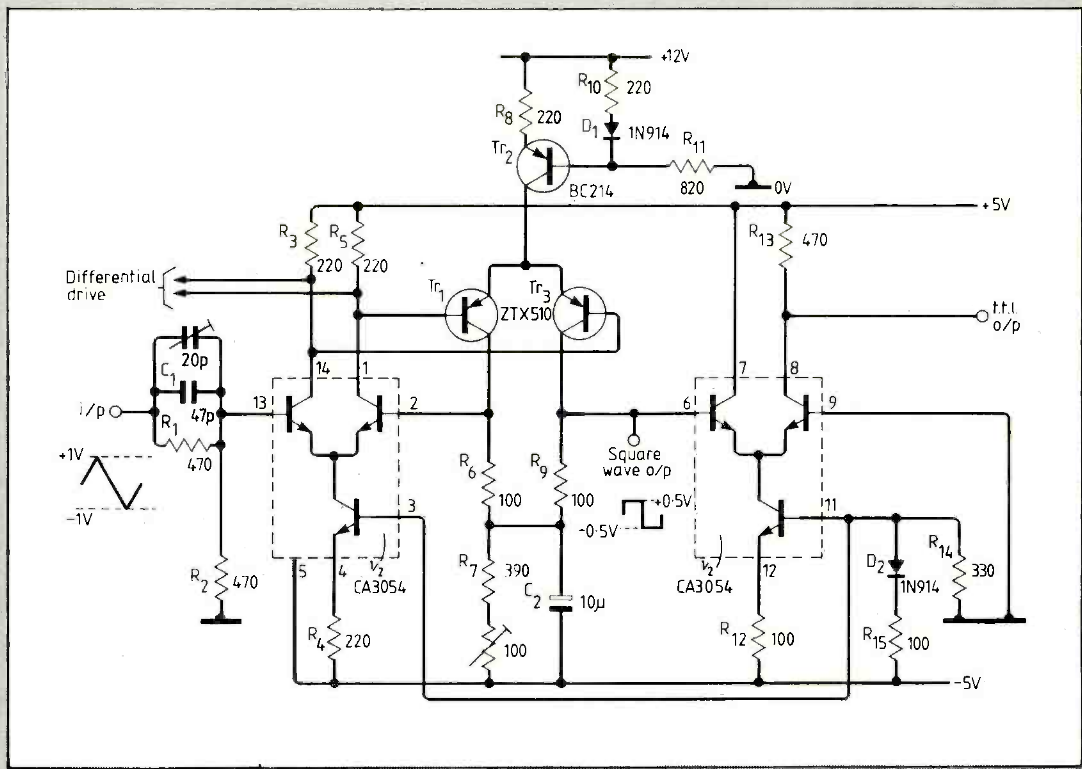
This trigger was developed for use in a voltage-controlled oscillator where the requirements of fast response and stable, well-defined switching levels could not be met by standard i.cs.

Hysteresis is determined by current source Tr_2 and R_6; with values shown, current through the source is 10mA and hysteresis is 1V. The potentiometer is adjusted to centre the hysteresis range about 0V so that switching levels at the circuit input are ±5V.

In the v.c.o. circuit, a second differential pair is driven in parallel with $Tr_{1,3}$ to generate a triangle wave, and a symmetrical squarewave is taken from the collector of Tr_3.

Series input capacitance provides frequency compensation to over 5MHz; response time is about 10ns. The second half of the CA3054 provides a t.t.l.-compatible squarewave.

D.J. Faulkner
Institute of Opthalmology
London



Electronic telephone-patch circuit

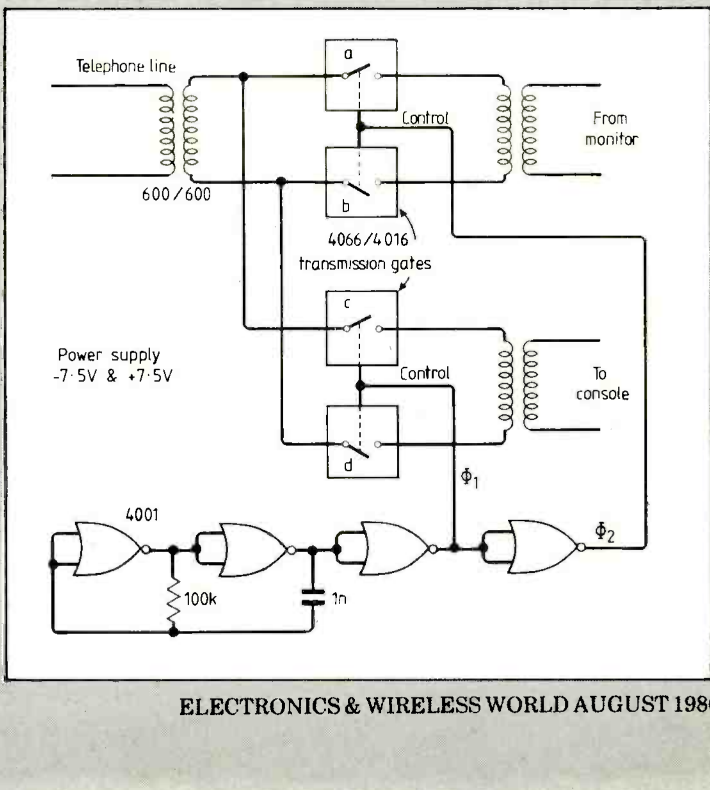
A simple, economical alternative to the transformer hybrid circuit for coupling a telephone line to a transceiver is this time-division-multiplexing telephone bridge circuit.

This is a slightly different approach to the familiar circuit used in the past to provide dual-trace displays on single-beam oscilloscopes. Instead of multiplexing two signals into one output, the circuit is used to ensure that output of the transceiver is never connected to the input.

Resistance of the transmission gates in their off state is several megaohms. Each transmission-gate pair, connected as a double-pole single-throw switch, is switched alternately by two clock signals — one true and one inverted. These two symmetrical clock signals are provided by the 4001.

The transformers are optional. Note that the telephone line is terminated correctly but the transceiver input and output are not.

Marshall P. Brown
Dhahran
Saudi Arabia



Telephone circuits

Please remember that in the UK, all equipment for connection to the public-switched network must have BABT approval. BABT does not consider circuit diagrams for approval, only complete apparatus, and the approval process is expensive and time consuming.

The approval system is intended to ensure that signals passed down the telephone line are within certain limits so that they do not cause interference on other lines, and to ensure that lethal voltages can never appear on the telephone line.

British standards relating to connection of apparatus are given in the December 1985 issue, page 77.

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256K memory for QL

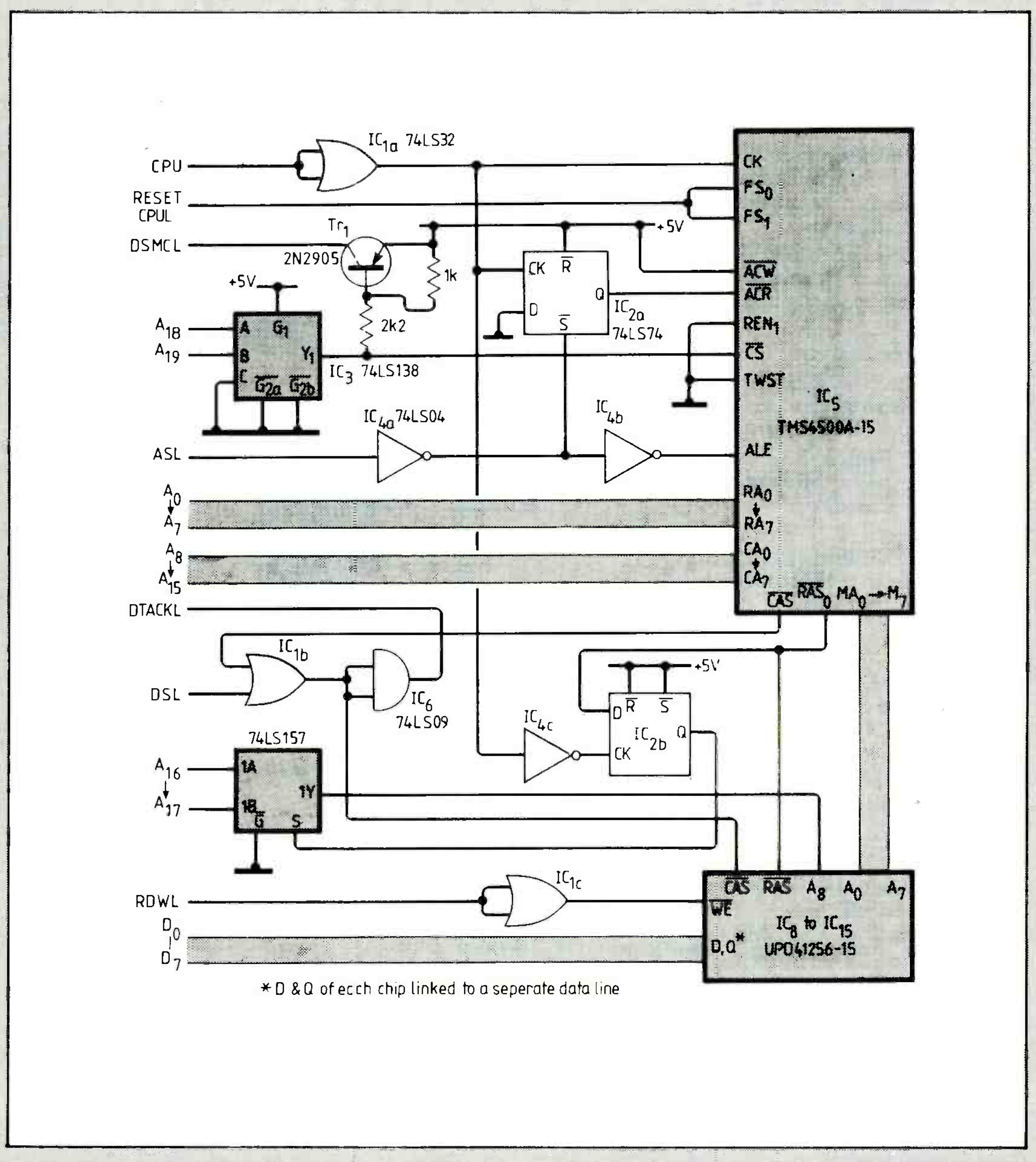
This design adapts the readily available TMS4500 dynamic-ram controller for interfacing 256Kbit ram i.cs to the 68008 processor in the QL computer. This controller is intended to drive i.cs of up to 64Kbit so an extra multiplexed address line must be provided for 256K devices.

The UPD41256 ram requires a refresh address on only eight of the nine address inputs so an external multiplexer selecting between two address lines is suitable for driving MA_8. Multiplexing for this line is controlled from the $\overline{\text{RAS}}$ signal delayed by a D-type bistable i.c. which is clocked by negative edges of the system clock; this ensures that address set-up and hold times relative to $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are met.

As well as enabling the controller at addresses 40000 to 7FFFF, the 74LS138 disables the internal rom and ram images normally present by pulling up the DSMCL line. Note that the DTACKL line is driven from an open-collector gate.

The unit plugs into the peripheral expansion socket and requires an on-board 5V regulator and good power-supply decoupling, especially around the ram i.cs

J. Williams
Watford
Hertfordshire

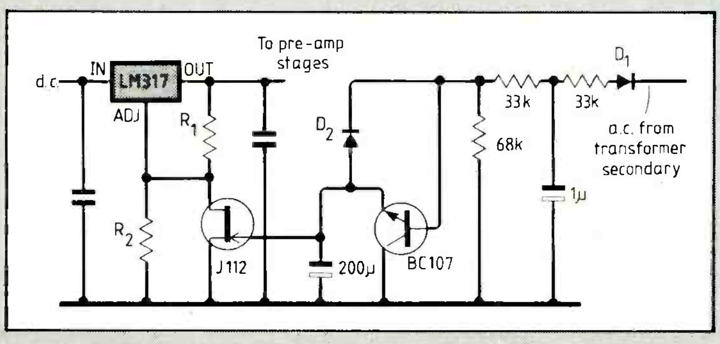


Preamplifier switch-on transient eliminator

Good design and balanced circuitry reduce switch-on transients to insignificant levels in power amplifiers but the switch-on problem in low-level audio circuits is not so easily solved.

Besides stopping 'thump' at switch on, an eliminator must not be fooled by repeated on/off switching at short intervals and it must not affect normal operation of the audio circuit. This circuit satisfies these requirements.

When gate/source voltage is zero, the fet acts as a resistor of typically under 100Ω and keeps regulator output at around 2V. As V_{gs} becomes more negative, the fet starts to turn off and regulator voltage rises. At a V_{gs} of greater than −5V, the fet is turned fully off and regulator output voltage is determined by $R_{1,2}$ alone.



Slow turn on is achieved by charging the 200μF capacitor through two 33kΩ resistors. At turn off, this capacitor is discharged quickly through the BC107 transistor. The 1μF capacitor makes sure that the 200μF capacitor is not discharged because of ripple or mains fluctuation and D_2 protects the transistor against excessive negative V_{be}.

Turn on/off times may need changing to suit your needs.

Graham Nalty
Derby

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Cassette mechanism control logic using a keyboard encoder

Solenoid-operated cassette mechanisms such as the one supplied by Hart Electronics use three solenoids, one for fast forward, one for rewind and one for cue/review. Both fast-wind solenoids operate together for play or record. A Hall-effect sensor gives one pulse for each revolution of the take-up spool.

Logic control of these solenoids is easy using a 74C922 16-key encoder i.c. which encodes a matrix of up to four-by-four momentary push switches into a four-bit binary number and provides debouncing.

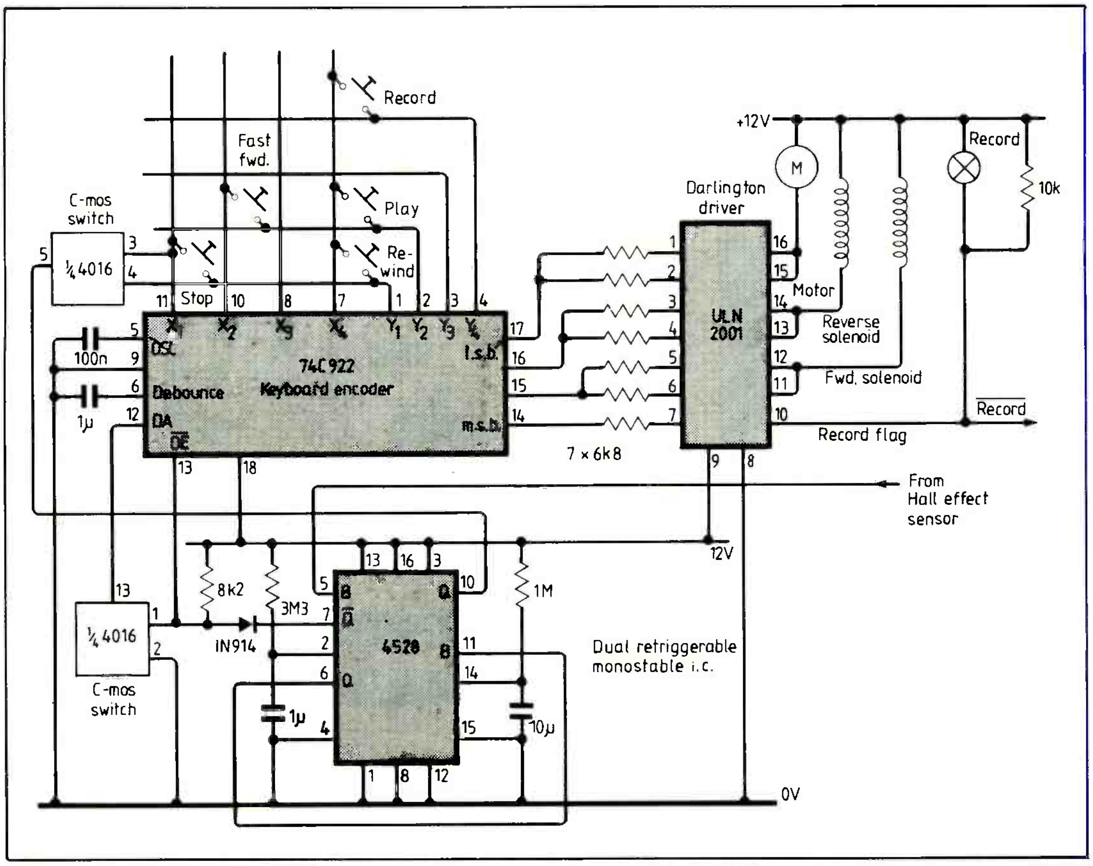
Two bits of the binary output are used to drive the fast-wind solenoids and one forms a record-flag line. For battery-operation, the fourth output bit switches the drive motor; in other applications this may not be necessary.

By choosing five appropriate matrix positions for play, record, fast-forward, rewind and stop, the binary outputs can be made to switch the solenoids, motor and record flag in the desired combinations. The solenoids are driven satisfactorily from a 12V supply using a Darlington-transistor array.

One half of a dual retriggerable monostable i.c. stretches pulses from the Hall-effect motion sensor and the other half sends a stop pulse to a c-mos switch wired in parallel with the stop button. A further c-mos switch used as an inverter drives the keyboard-encoder output-enable low; subsequently, this line is held low by the pulse stretching monostable i.c. through a diode.

Discrete transistors could be used to save space. The cue/review facility is not implemented here but spare switches could be used to operate it when either of the fast-wind buttons is held down. Remote or automatic control is possible by connecting additional c-mos switches across appropriate push buttons.

Keith Wootten
Reading
Berkshire



Fast switching opto-coupler

Transition time of this logic-signal isolating circuit is 320ns using a 4N26 opto-coupler. Fast switching is obtained by using the photo-transistor as a small-signal amplifier and keeping it active.

Negative feedback makes sure that the transistor stays in small-signal mode. The first inverter is a linear amplifier and R_f provides feedback and bias.

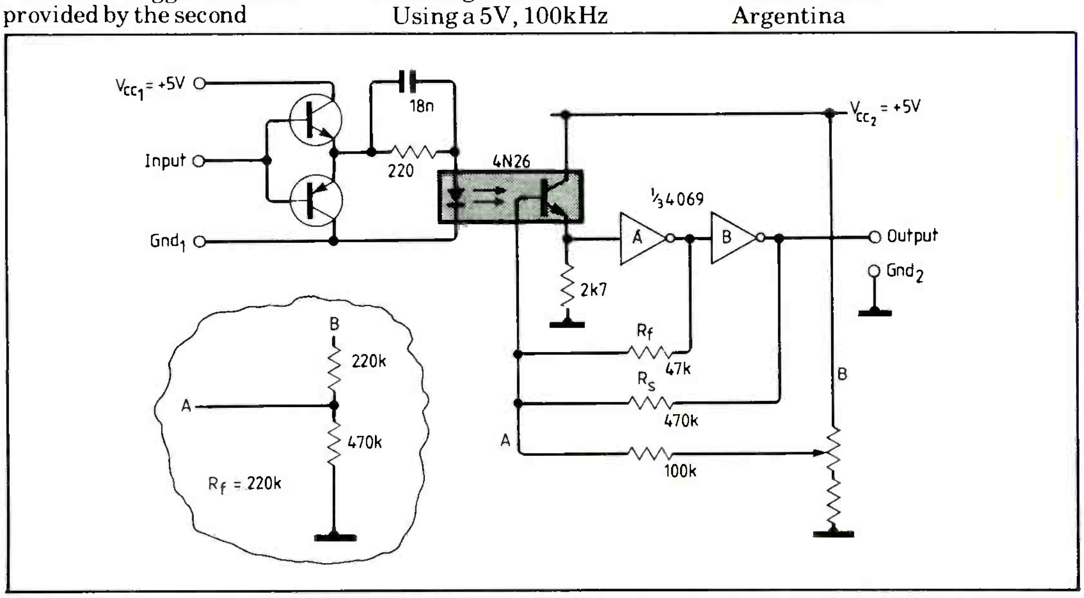
Schmitt-trigger action is provided by the second inverter, output of which gives positive feedback through R_s. The hysteresis loop prevents typical switching oscillation in the output and provides some noise immunity.

To allow the phototransistor to be biased for maximum inverter amplification, a potentiometer is included. Calibration is done by applying a 5V squarewave input and setting the potentiometer to give the best switching times.

Using a 5V, 100kHz squarewave with 40ns rise and fall times, output rise delay is 200ns, rise time is 120ns, fall delay is 120ns and fall time is 200ns. This gives a transition time of 320ns.

An input signal of 2MHz transferred well, but phase delay was approximately 180°. Replacing the potentiometer with fixed resistors makes the circuit simpler but switching time is reduced.

Hernán Tacca
Buenos Aires
Argentina



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64180 computer board

by J.H. Adams, M.Sc.

So many peripheral functions are included in the 64180 microprocessor that this c.p.u. board for SC84 can be used on its own. Operation is discussed this month.

This Eurocard-size 64180 microcomputer board is designed to replace the SC84 microcomputer c.p.u. card. It performs so many peripheral functions though that it is suitable for use as a complete microcomputer or as the basis of other multi-board systems. This second and final article describes operation of the board.

In this design, the timer-output function is unused and a current-limiting resistor is provided for the $\mathrm{CKA_0}$ clock-output line.

Timing problems concerning $\overline{\mathrm{ME}}$ and $\overline{\mathrm{LIR}}$ are easily solved by latching circuits on the peripheral boards if necessary. More serious is the effect of the processor on Z80 peripherals other than the MK3801. In defence of the HD64180 though, you could argue that the external peripheral functions are unnecessary as they are all included in the processor.

Besides the processor, the computer-board circuit consists of bus buffering, serial i/o buffering, memory, memory decoding and reset circuits.

A long pulse at power-up of approximately 50ms and a shorter pulse on operation of the reset switch are provided by the reset circuit. Length of the power-on reset pulse is determined by the time taken to charge C_3 through R_2.

When power is applied there is no charge in C_3 and hence no potential difference across it. This means that pin three of IC_6 is initially high and the $\overline{\mathrm{RESET}}$ line low but as the capacitor charges, voltage at pin three falls. Eventually the gate switches to change the state of the $\overline{\mathrm{RESET}}$ line. Capacitor C_3 continues to charge until pin three is at ground potential.

When the reset button is pressed, C_1 is discharged, causing a low-to-high transition at pin six which is differentiated by C_2/R_2 to give a short positive pulse at pin three. Diode D_2 prevents the differentiation from being swamped by the relative size of C_3.

During pressing or releasing of the button, the time constant of the circuit prevents bounce in the switch from triggering several reset pulses. Diode D_1 ensures that C_3 discharges rapidly when power is removed so that if the power is turned off then on quickly, the reset circuit operates correctly.

In normal use, the processor will be used with the internal 256Kbyte dynamic memory occupying all physical addresses up to 3FFFF. When resetting of the system occurs, either on application of power or as a result of pressing the reset switch, the system memory is rearranged so that the system eprom appears at all read locations and the dynamic ram appears at all write locations.

Devices that can be used for the system eprom are 2764, 27128 or 27256. Link one is made for the first two devices and link two for the 27256. Whichever device is used, the eprom image is repeated throughout the 512Kbyte address range.

Contents of the eprom should be the operating system, a routine for copying the operating system to its position in d-ram and any once-only code for initializing areas of the computer.

Two options are provided for the operation which disables the eprom and leaves the system completely ram based. Link four selects any i/o operation as the remapping pulse while link five selects an external signal as the pulse.

In practice, the eprom should contain code to produce the remapping process at an address that overlaps and leads directly to a jump to the operating system in the d-ram. In the standard eprom, the code

```
XOR  A
OUT  (SILTRK),A
JP   MCOS
```

is located at the top of the eprom and at the top of MCOS. A jump to this code in eprom results in the first two instructions being fetched and executed from eprom but the third and subsequent instructions come from d-ram, the eprom then having been switched out of use.

The advantage of this technique is that the computer memory, once remapped, is completely read/write memory so a new operating system can be loaded into what would normally be unalterable rom.

A potential disadvantage is that a rogue program can corrupt the operating system, but the 64180 traps illegal op-codes and so reinstatement of the system after such a corruption requires only a press of the reset button.

The normal sequence of a dynamic memory access is as follows. Half of the access address is applied to the address pins for the memory and this address is latched by a negative-going edge on the $\overline{\mathrm{RAS}}$ (row-address strobe) input. The second half of the access

64180-board features

Up to 32Kbyte eprom on-board.
256Kbyte zero wait-state ram.
Decoding for further four 64Kbyte memory blocks.
6.144MHz clock.
Two high-speed d.m.a. channels.
Two asynchronous serial channels.
One synchronous serial channel.
Two programmable timers.
Eurocard format.

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address is then applied to the same address pins and this is latched into the memory by the negative going edge of $\overline{\text{CAS}}$ (column-address strobe).

After the necessary period the selected location is accessed and while $\overline{\text{CAS}}$ remains low, the contents of the location appear at the device's Q output pin. During this $\overline{\text{CAS}}$-low period the write line $\overline{\text{W}}$ may be driven low in which case data on the device's D input pin is written into the location on the falling edge of $\overline{\text{W}}$ and consequently appears at the Q output.

That is a basic description of d-ram access, which has not changed since the earliest days of multiplexed devices. Nowadays d-ram manufacturers have added several extra modes of operation in order to make the devices more versatile. Increasing the number of pins on an i.c. increases the price and since d-rams are probably the most price-sensitive components made, these additional features all depend on relative timings of $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{W}}$ to minimize the number of pins.

Signal $\overline{\text{RAS}}$ not only has the effect of latching half the access address but also of accessing all locations of which that address forms part. Accessing a location also refreshes it and so $\overline{\text{RAS}}$ only cycles can be used for refresh purposes.

This mode of operation is used by the HD64180 to effect transparent d-ram refresh. The HD64180 puts out an 8 bit address during each refreshing cycle that it inserts into the execution sequence. This address is incremented after each refresh and so the entire memory content is kept intact.

Address strobe $\overline{\text{CAS}}$ is only recognized as a memory accessing signal when $\overline{\text{RAS}}$ is low, the normal mode of memory use being $\overline{\text{RAS}}$ before $\overline{\text{CAS}}$. As well as latching the second half of the address, the falling edge of $\overline{\text{CAS}}$ latches the state of the $\overline{\text{W}}$ line.

If $\overline{\text{W}}$ is inactive (high) at this point then the cycle continues as a read cycle which could turn into a write cycle as described earlier. If $\overline{\text{W}}$ is active (low) when latched then the cycle is taken to be a write one but, more significantly, the Q output remains inactive. This means that, provided that the $\overline{\text{W}}$ signal is active at an early point in the write cycle, the d-rams may be used in the "common i/o" mode as is standard with static and bus-oriented devices.

Most microprocessors, the HD64180 included, do not produce an "early write" signal as the write signal itself is intended as a writing strobe rather than as an indicator that a write will occur in the current cycle.

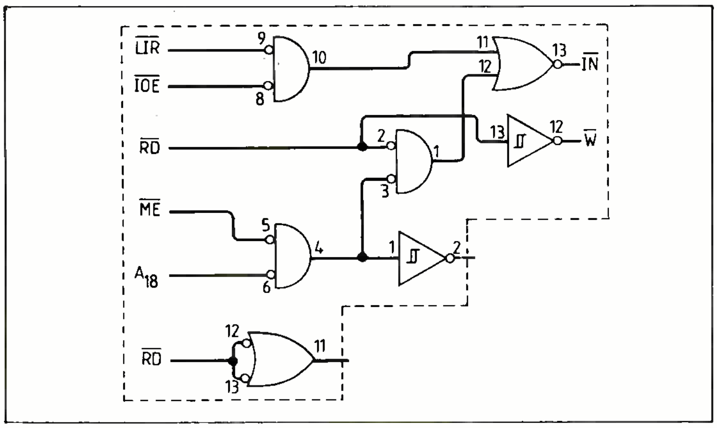
The system read signal is however an early-read signal and so the state of this line at the falling edge of $\overline{\text{CAS}}$ reflects whether the cycle it to be a read or not-read one.

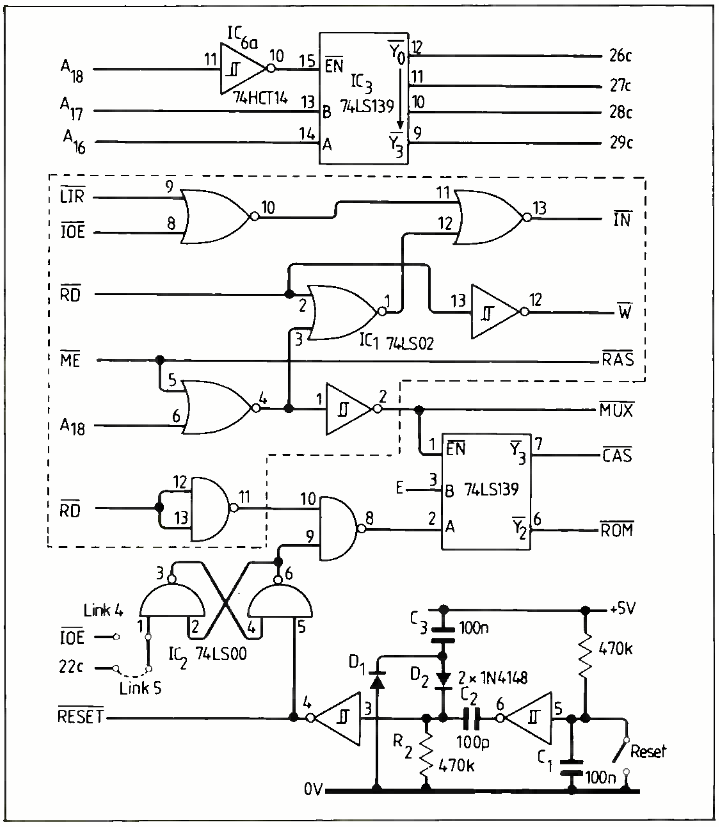
There are types of cycle which are neither read nor write. Possible contention is avoided since no $\overline{\text{CAS}}$ signal is produced in this type of cycle. The fact that this system produces a potential early-write cycle every time that there is not a processor $\overline{\text{RD}}$ cycle does not cause any spurious writes to the d-ram as $\overline{\text{CAS}}$ is fully decoded and is only active during memory accesses to the lower half of memory. In this way the d-ram will not even notice i/o cycles, interrupt acknowledge signals or accesses to external memory.

Timing diagrams for the memory control were shown last month. There are several types of memory cycle that the HD64180 can execute. As all read/write operations (op-code fetches, processor read/writes and d.m.a. read/writes) have the same cycle length (unless extended by the insertion of WAIT states) the lower diagram is a composite diagram illustrating the reading or writing of data from/to memory.

The difference between a fetch of an op-code and the fetch of data from memory is that during the op-code fetch LIR is active and data is expected to be stable one half clock cycle earlier. The upper diagram shows a refresh cycle without WAIT states.

The data bus buffer is turned inward during interrupt ack-





Control logic for the 64180 computer board. Signals MUX, RAS and CAS are for the d-rams and ROM selects the eprom for reading at switch on or after reset. Link 4 determines whether the rom is switched out of the memory map following an i/o operation or following occurrence of an external signal through connector pin 22c. Part of the gating is shown in intentional logic (top).

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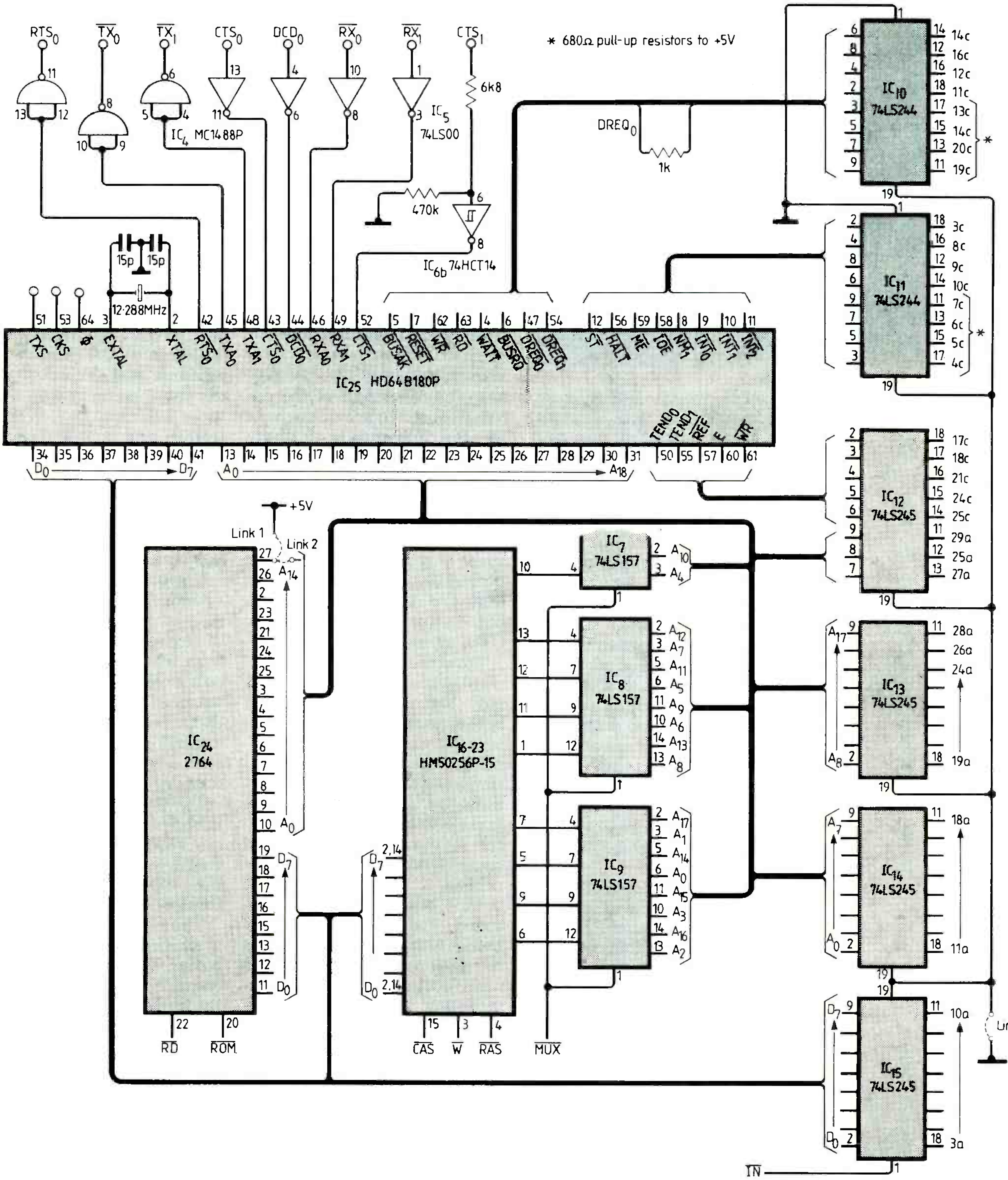
64180 computer board main circuit. Because the microprocessor has integrated peripheral functions, a computer with memory management unit, two d.m.a. channels, three serial channels with programmable bit-rate generator, two-channel counter/timer, interrupt controller, 256Kbyte ram and an eprom can be built on one Eurocard board. To simplify the diagram, control logic is shown separately.



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Kits and boards

Three kits will be available from John Adams. First is a processor kit containing a 6MHz 64B180 microprocessor, turned-pin socket, 12.288MHz crystal and manual. This kit is £23.75 to UK readers and £25.25 to those in Europe. Secondly, there is a memory kit including eight d-rams and a preprogrammed 2764 at £29 in the UK and £29.50 in Europe. Finally, a kit of passive parts with resistors, capacitors and connectors but excluding crystal is available for £9.50 in the UK and £10 in Europe.

All prices include postage and packing but exclude v.a.t. For further details and kit prices for countries outside Europe, send a s.a.e. to John at 5 The Close, Radlett, Hertfordshire WD7 8HA.

A Eurocard p.t.h. board for this microcomputer will be available toward the end of July at £19 inclusive from Combe Martin Electronics, King Street, Combe Martin, North Devon EX34 0AD.

nowledge cycles and read cycles other than those made to the lower half of the physical memory. The gates used in control circuit are drawn in their logical and positive logic sense. Most signals in the system are active low and hence negative logic is implemented.

The algorithm for the bus-direction signal is that the direction is $\overline{\text{IN}}$ when $\overline{\text{LIR}}$ And $\overline{\text{IOE}}$ are active Or when $\overline{\text{RD}}$ And Not ($\overline{\text{ME}}$ And Not A_{18}) are active. Signal $\overline{\text{ME}}$, the Z80 $\overline{\text{MREQ}}$ signal, is used directly as $\overline{\text{RAS}}$ and, gated with A_{18} and delayed by two gates and the switching time of multiplexer IC_3, as the address multiplexer switch. This tight timing is possible as the address hold requirement after the $\overline{\text{RAS}}$ strobe is only 15ns maximum.

Gating with A_{18} is not strictly necessary for the $\overline{\text{MUX}}$ signal but it provides a useful component for deriving $\overline{\text{CAS}}$, which is produced by gating the new E signal with $\overline{\text{MUX}}$. This produces a signal indicating a memory operation in the lower half of physical memory which is directed by the rom mapping circuitry to either enable the rom or to act as $\overline{\text{CAS}}$.

Generation of a $\overline{\text{CAS}}/\overline{\text{ROM}}$ signal at an early stage in the processor cycle allows the use of cheap dynamic rams without the need for any WAIT states, giving highest-speed operation.

There is not enough time for access of a standard 250ns eprom without WAIT states being added but the HD64180 leaves its reset procedure with three WAIT states programmed into each cycle and a high refresh request rate and so the system automatically runs at low speed while the operating system is copied into the d-ram. Once control is passed to the d-ram-based code the WAIT states can be removed and the refresh-request rate reduced to provide maximum execution speed.

After reset READ is passed through two inverting gates to IC_3 where it acts as the select input to what is effectively a one-to-two-line demultiplexer producing either a $\overline{\text{ROM}}$ or a $\overline{\text{CAS}}$ signal for each memory access. When the mapping bistable device is pulsed, the path for READ is closed and the demultiplexer set to permanently supply the $\overline{\text{CAS}}$ signal. The other half of the decoder is used to provide selects for the upper four 64Kbyte memory segments.

The asynchronous ports require five input and three output RS232 level-shifting buffers. Owing to restricted p.c.b. space only four standard input buffers are available and so an ordinary inverter with an input limiter is provided for the CTS_1 input.

Construction is straightforward. Points to note are that only the microprocessor and eprom should be mounted in sockets and that the decoupling capacitors are critical components. These capacitors must be good-quality multilayer ceramic types. The crystal is mounted upright and supported by a fillet of silicone rubber.

Full bus buffering is provided, the 64-way bus now being fully used. Some lines have been redefined since the specification for SC84 was devised but these are restricted to lines which have not yet been used. The current v.d.u. and i/o boards can be used with minimal modification.

On the v.d.u. board the connection to pin 20c should be broken and made to pin 26c. The 2N2369 transistor should be removed and the v.d.u. select switches starting from the 64-way connector set to on, off, on, off.

For the i/o board a wire should be connected from pin 22c to IC_{204}, pin 7 and, if fitted, the wire from pin 21c to IC_{205}, pin 5 should be removed.

To modify the i/o board for d.m.a. control of the floppy-disc system connect wires from IC_{211}, pin 38 to IC_{219}, pin 11 and from IC_{219}, pin 10 to pin 19c.

On the silicon-disc board the 2N2369 transistor should be removed, the connection to 21c should be broken and made to 29a instead and the switches should be set so that all except the one nearest the edge of the board are on.

Connection 25c should be broken and rerouted to 22c.

There are several advantages to changing to the new processor board. The extra serial i/o largely obviates the need for a separate i/o board, the extra instructions are quite useful, the extra speed is welcome and the extra memory and memory-based features such as the d.m.a. controllers and memory management unit make program development much more interesting. To complement the design of this board new versions of MCOS and SciDOS have been developed.

The machine-code operating system MCOS has been increased in size by 512 bytes, the extra memory being taken from what was the disc-sector buffer. The new system does not need this buffer and so the extra features built into the expanded MCOS are not included at the expense of system memory.

The printer routine has been modified to work through serial channel one on the c.p.u. board, leaving the more versatile serial port on the i/o board free for other applications.

The routine also implements a 48Kbyte internal printer buffer. This buffer is located in one of the extra pages of ram on the processor board. Operation of the printer buffer goes largely unnoticed, the serial port working on interrupts.

While the long term printing rate is, of course, controlled by the printer, the use of such a buffer frees the computer for regular use while printing continues as a background

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activity.

As an example this complete article, which is just over 42 000 characters long, takes as little as 18 seconds to dump to the printer buffer, after which the computer is free for other uses. Without the buffer it would take approximately ten minutes of computer time when printed on a matrix printer or over half an hour on a daisy-wheel printer.

During the balance of time anything may be done with the computer other than immediately using the printer, or switching the computer off. Tests have shown negligible slowing in the computer's rate of working while printing takes place.

All disc handling is performed using d.m.a. control and an extra disc function has been introduced. The three original functions are still provided for the sake of continuity but I recommend that the new single function be used in future software development.

The new function DODSK is called at address location MCOS+036_{16} and, like the original functions, is entered with the IX register pointing to a disc data block. The difference is in the length of this block which now comprises the one-byte drive code, one-byte track number, one-byte sector number, one-word d.m.a. address, one-byte d.m.a. bank, and finally the count of bytes to be transferred which also takes one word.

When the DODSK function is called the A register must contain the command code for the operation to be executed. This command code is in two four-bit sections. The upper half of the byte is the command type, value eight meaning read sectors, A meaning write sectors, E meaning read track and F meaning write track.

The lower four bits are function descriptors and have the following significance. Bit zero set implies that the command is to repeat until the number of bytes specified in the count have been processed. Bit one set implies that the operation is to be verified and bit two is set when the operation will involve a data transfer to or from the disc. Bit three is set when the transfer will be a write to the disc.

Examples of commands are 084_{16} for reading a single sector and 085_{16} for reading sequential sectors until the number of sectors on the track is exceeded or until the number of bytes specified in the count value has been reached.

Version 2.2 of SciDOS takes advantage of this new disc function. All disc operations through SciDOS are handled on a multi sector basis, accesses to the magnetic discs being made via a track-sized buffer in one of the HD64180's extra memory pages.

This dramatically speeds up operation of the disc interface, accesses to the disc only being made whenever the system wishes to change track. The SC84 was already a fast computer but these changes make it even faster, a 16Kbyte file taking as little as three seconds to save.

All accesses to the silicon disc are made directly rather than via this buffer. This has an important advantage over the current system. When using programs such as Wordstar from the silicon disc, users have noticed that drive A: regularly starts up. This wastes a small amount of time but, more to the point, it is distracting and means that eight-inch disc users have to keep their mains-powered drives on.

The cause of this in Wordstar, and other packages, is the regular use of logging functions within the DOS which relog the system to drive A: and to the current one, i.e. they put all other drives off-line. Logging involves scanning the directory of a drive and as the entire directory of drive A: can reside in the track buffer while access to the silicon disc is taking place, there is one access to drive A: at the start of the session – and then all is quiet.

One problem with buffered disc systems is that the user has to remember not to strand data in the buffer at the end of a session. The SC84 has always been a buffered system although up to now this has been just for the physical sector being used; avoiding lost data has primarily meant leaving a program in an orderly manner rather then just breaking off by switching off.

With the newer, bigger buffer the need to exit correctly is even more critical and so the system collapses the buffering system whenever data is being written to the track containing the directory. As the directory is the last area accessed when closing a file or leaving a program, this ensures that the disc is always up-to-date at the end of an application. ■

LITERATURE RECEIVED

An **Integrated circuit data-book** from Exar contains a large nuber of "application-specific" i.cs. Telecommunications circuits include line interface, repeaters, speakerphone and telephone i.cs. There is a section on single-chip modems and filters. Computer interface circuits consists of various read and/or write amplifiers for floppy and hard discs. There is a wide range of operational amplifiers, timer and voltage regulator circuits for industrial applications. Under the heading "instrumentation" there are oscillators and waveform generators, multiplexers, p.l.ls and tone decoders. There are display drivers and printer hammer drivers and a number of special function circuits. There are also details of the company's semi-custom chips and a very useful section of application notes. Exar Corporation, Moorbridge Road, Maidenhead, Berks SL6 8PL. **EWW 250 on the reply card**.

Renting test equipment often makes sense for development of products. TechniRent offer a range of processor development systems and emulators, logic analysers, computers and computer-aided design and test equipment. They also have a list of second-user equipment for sale. TechniRent Ltd, Unit 4, Kings Ride Park, Ascot, Berks SL5 8BP. There is another branch in Warrington, Cheshire. **EWW 251 on the reply card**.

Connectors, cable, wiring accessories and tools are included in the **Catalogue** of Argosy Components Ltd, PO Box 137, Beaconsfield, Bucks HP9 1RJ. **EWW 252 on the reply card**.

AMI make gate arrays and include in their catalogue chapters on the use of cad/cae tools in their development. Following these sections on custom and semi-custom i.cs, AMI's **mos products catalogue** lists its standard products, including communications products such as station and p.c.m. products, codecs, modems, filters and diallers. Roms range from 16K to 256K in n-mos and 256K in c-mos. Consumer products include driver circuits. There are the S6800 and S7720 signal processor AMI Microsystems Ltd, Prosect Place, Swindon, Wilts SN1 3JZ. **EWW 253 on the reply card**.

The Midwest **PTC current protector** is made from a special polymeric compound that has a sensitive temperature range and if it gets too hot automatically becomes a very high resistance. Versions are available to respond to current overload or to ambient temperature limits, and they may be used in the protection of d.c. motors, p.c.bs, delicate components, transformer secondary windings, heaters and batteries (against overcharging). Detailed in a data sheet from Elyon Electronics Ltd, Unit J, Charlwoods Business Centre, Charlwoods Road, East Grinstead, W. Sussex RH19 2HH. **EWW 254 on the reply card**.

Instruments for the measurement, analysis and recording of data relating to sound, noise, vibration, illumination, thermal environment and medical diagnostics are described in a short-form catalogue from Brüel and Kjaer (UK) Ltd, 92 Uxbridge Road, Harrow, Middlesex HA3 6BZ. **EWW 255 on the reply card**.

The development and advantages of plastic leaded chip carriers, used in surface-mounted i.cs are detailed in a brochure from MM which also lists the product available in p.l.c.c. packages. Monolithic Memories Ltd, 1 Queens road, Farnborough, Hants GU14 6DJ. **EWW 256 on the reply card**.

Frequency control in all its aspects; quartz crystals, oscillators and filters are detailed in a 150-page catalogue from IQD Ltd, North Street, Crewkerne, Somerset TA18 7AR. **EWW 257 on the reply card**.

Jaybeam make a wide range of antennae, and associated masts and mounting equipment together with splitters, duplexers and filters. These are all detailed in the **product information guide** of the Antenna and Electronics Division, Jaybeam Ltd, Kettering Road North, Northampton NN3 1EZ. **EWW 258 on the reply card**.

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NEW PRODUCTS

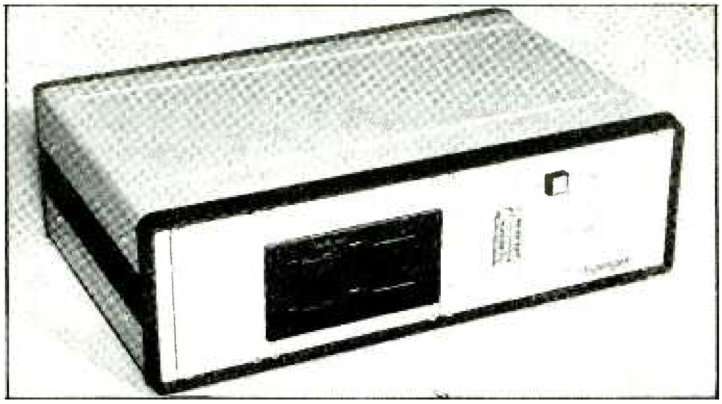
Optically isolated logic

A first is claimed for the General Instrument family of optically coupled logic interface gates. Functionally the gates are the same as a t.t.l. or c-mos buffer or inverter, and versions are available to be compatible with t.t.l. and c-mos logic or to interchange between the two. The gates come on three silicon chips in a single package; the first is an input amplifier and led driver the second is the led itself and the third, a photodetector and output amplifier.

The Optologic devices feature a typical propogation delay of 60ns; isolation from voltages up to 2500V r.m.s. (1 minute) for a working voltage of 440V; common mode transient immunity of 5000V/μs, with a typical common mode of 15000V/μs. Applications are many but the devices are especially useful in communications equipment and for interfacing between different logic families. General Instrument (UK) Ltd, Optoelectronics Division, Times House, Station Approach, Ruislip, Middlesex HA4 8JG.
EWW 216 on the reply card.

Development system for 6301X

Application development of the Hitachi HD6301X has been slow and expensive as no simulation device has been available. However Beamen Ltd has produced the Microtrac Simulator which provides in-circuit emulation for both mask and electrically programmable models. It bridges the gap between 'zero turnaround' devices and full emulation systems. It is powered by the target circuit, is compact and "ideal for laboratory and on-site work." Another simulator, for the HD11, is to be available soon. Beamen Ltd, Centaur House, Fairview Road, Cheltenham, Glos GL5 2EX.
EWW 213 on the reply card.

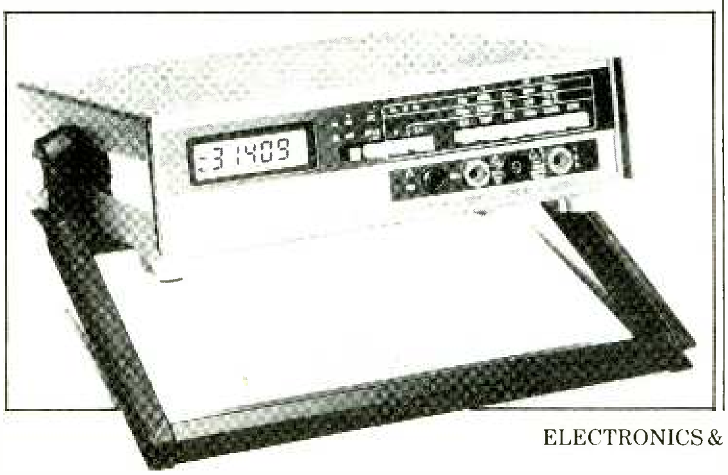


Development system for 6800

R.S.C. Microsystems have produced the LCDS which is a software development system for the R6500, R65C00, RM65 and related devices. It incorporates an R65C02 processor and can be used to develop and run code for all processors within the range. A rom-based editor/assembler and de-bug monitor make the system much faster than a comparable disc-based system. Hardware target systems can also be developed in conjunction with the Rockwell low cost emulator which provides real-time in-circuit emulation at speeds up to 4MHz. The LCDS can be used with high-level languages for software development of target hardware based on the RM65. RCS Microsystems Ltd, 141 Uxbridge Road, Hampton Hill, Middlesex TW12 1BL.
EWW 222 on the reply card.

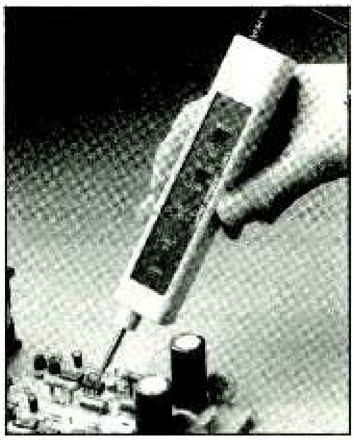
Multimeter with r.m.s. and high resolution

A basic accuracy of 0.05% is guaranteed for one year for the 1504 d.m.m. from Thurlby. The 4.75-digit display gives a full-scale count of 32000 which provides a 60% greater resolution than 4.5-digit units. Direct voltages up to 1200V can be measured with alternating voltages up to 750V with true r.m.s. measurement. Direct and alternating current measurements up to 10A and resistance up to 32M Ω. The sensitivities for the appropriate ranges are 10μV, 1nA, and 0.01Ω. The resistance ranges provide high accuracy diode test measurements and in-circuit measurements across semiconductors are possible without losing accuracy. Frequency measurement up to 3.9999MHz is possible with an accuracy of 0.005% and a resolution of 100Hz. Complete with test leads and manual for £199. Thurlby Electronics Ltd, New Road, St. Ives, Huntingdon. Cambs PE17 4BG.
EWW 221 on the reply card.



Updated logic probe

The latest version of the LP1 probe is now suitable for e.c.l. logic as well as t.t.l. and c-mos. It detects, memorizes and displays logic levels, pulses and voltage transients. The instrument, when set to 'pulse' can capture pulses as short as 50ns. The memory function can store single-shot or slow pulse train events indefinately. High frequency signals, up to 10MHz, cause the indicator to flash at 3Hz while The high and low indicators show the duty cycle of the pulse train. The probe is protected against overvoltage and reverse polarity supplies. The 100k Ω input impedance ensures low loading of the circuit. Global Specialities Corporation (UK) Ltd, Shire Hill Industrial Estate, Saffron Walden, Essex CB11 3AQ.
EWW 212 on the reply card.



Electrolytics for audio

The introduction of an additional conductive layer within the paper separator in the BG capacitors has made them particularly low in leakage losses. This resolves the problems of power loss and e.s.r. normally associated with electrolytics and makes them highly suitable for audio applications. The series have a temperature range of −40 to +85°C, voltage ratings from 6.3 to 100V and capacitance range of 0.47 to 4700μF. KCP Electronics Ltd, Unit 7/9 Redburn Industrial Estate, Woodhall Road, Ponders End, Enfield, Middlesex EN3 4NB.
EWW 217 on the reply card.

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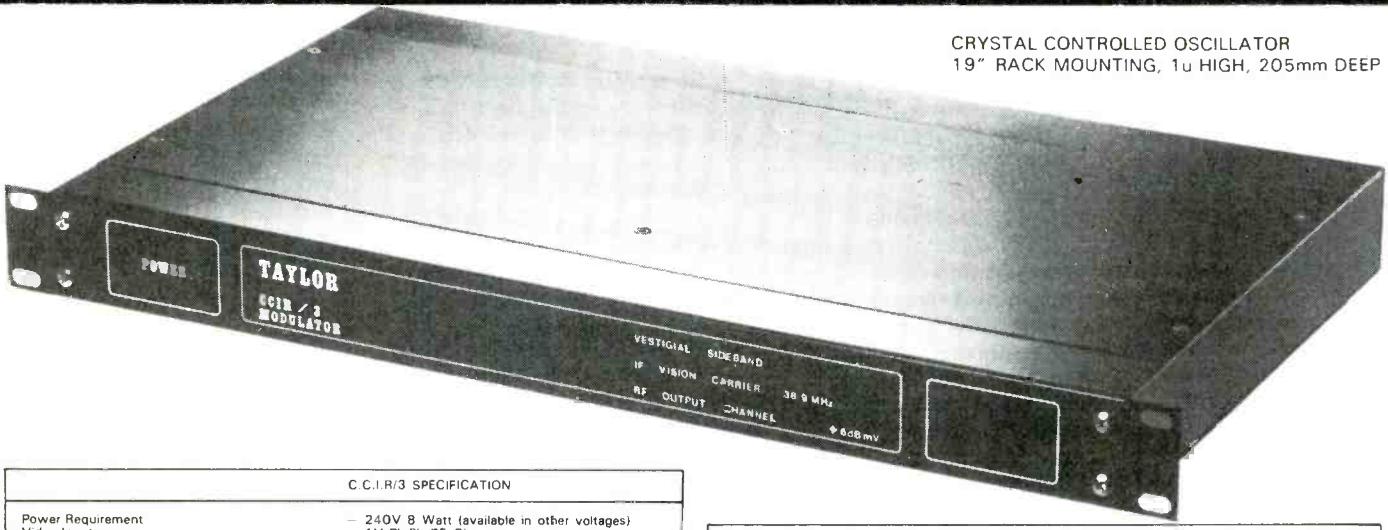
TAYLOR

VESTIGIAL SIDEBAND TELEVISION MODULATOR C.C.I.R/3



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Racal Solid State Communication Receivers – RA1217 – Mechanical digit readout 1 – 30MC/S – £300. **Racal RA17L Communication Receivers** 500KC/S to 30MC/S in 30 bands 1MC/S Wide – £175 – All receivers are air tested and calibrated in our workshop – supplied with dust cover – operation instructions – circuit – in fair used condition. **Racal Synthesisers** (Decade frequency generators) **MA250** – 1.6MC/S to 31.6 MC/S – £100. **MA1350** for use with RA17 receiver – £100. **MA259G** – precision frequency standard 5MC/S – 1MC/S – 100KHZ – £100 to £150. **RA137 and RA37** – LF convertors 10 to 980KC/S – £40 to £75. **RA98** SSB-ISB convertor – £50. **RA121** SSB-ISB convertor – £75. **Plessey PR155G** Solid State receivers – 60KC/S – 30MC/S – £300. **Transtel Matrix Printers** AF11R – 5 level baudot code – up to 300 bauds – for print out on plain teleprinter paper – £50. **Army field telephone sets** type F L and J – large quanitity in stock – £6 to £15 depending on type and quantity. P.O.R. **Don 10 Telephone Cable** – half mile canvas containers – £20. **Night Viewing infra – red periscopes** – twin eyepiece – 24 volt DC supply – £100 EA. Original cost to Government over £11,000 EA. **Static invertors** – 12 or 24 volt input – 240 volt AC sinewave output – various wattages. P.O.R. **XY Plotters and pen recorders** – various – P.O.R. **Signal Generators** various – P.O.R. **TF 893A** – Power meter – £50. **Racal frequency counter** type 836 – £50. **Tektronix plug-ins** – 1A1 £50. 1A2 £40. 1A4 £100. M £50. All items are bought direct from H.M. Government being surplus equipment: price is ex works. S.A.E. for enquiries. Phone for appointment for demonstration of any items: also availability or price change. V.A.T. and carriage extra.

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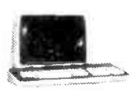

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A2900	13.75	EF89	1.60	PD500/510	4.30	1L4	0.80	6CW4	8.50	12AT6	0.75
AR8	0.75	EF91	1.60	PFL200	1.10	1R5	0.80	6CX8	4.60	12AT7	0.95
ARP3	0.70	EF92	2.15	PFL200*	2.80	1S4	0.65	6CY5	1.50	12AU7	0.95
ATP4	0.60	EF95	0.95	PL36	1.10	1S5	0.65	6D6	2.50	12AX7	0.75
B12H	3.90	EF96	0.60	PL81	0.85	1T4	0.65	6F6G	1.95	12BA6	1.25
CY31	1.40	EF183	0.80	PL82	0.70	1U4	0.80	6F6GB	1.10	12BE6	1.25
DAF96	1.25	EF184	0.80	PL83	0.60	2X2A	2.50	6F7	2.80	12BH7	3.45
DET22	28.50	EF812	0.75	PL84	0.90	3A4	0.70	6F8G	0.85	12E1	19.95
DF92	0.80	EFL200	185	PL504	1.15	3AT2	3.40	6F12	1.50	12J5GT	0.55
DF96	0.70	EH90	0.85	PL508	2.00	3B28	12.00	6F14	1.15	12K7GT	1.15
DH76	0.75	EL32	0.85	PL509	5.65	3B28*	19.50	6F15	1.30	12K8GT	1.25
DL92	1.10	EL34	2.10	PL519	5.85	3D6	0.60	6F17	3.20	12Q7GT	0.75
DY86/87	0.65	EL34*	4.55	PL802SE	3.45	3E29	19.00	6F23	0.75	12SC7	0.80
DY802	0.70	EL82	0.70	PY80	0.70	3S4	0.70	6F24	1.75	12SH7	0.65
E92CC	2.80	EL84	0.80	PY81/800	0.85	4B32	18.25	6F33	10.50	12SJ7	0.70
E180CC	11.50	EL86	0.95	PY82	0.75	5R4GY	3.35	6FH8	18.80	12SK7	1.45
E1148	0.58	EL90	1.75	PY88	0.60	5U4G	1.85	6GA8	1.95	12SQ7GT	0.85
EA76	1.60	EL91	6.50	PY500A	2.10	5V4G	0.75	6GH8A	1.95	12Y4	0.70
EABC80	0.80	EL95	1.25	QQV03/10	5.95	5Y36T	0.95	6H6	1.60	13D3	2.80
EB34	0.70	EL504	2.70	QQV03/10*	10.00	5Z3	2.80	6J4	1.95	13D6	0.90
EB91	0.60	EL509	5.85	QQV03/20A	27.50	5Z4G	1.25	6J4WA	3.10	19AQ5	1.35
EBC33	1.85	EL519	7.70	QQV06/40A	28.50	5Z4GT	1.15	6J5	2.30	19G3	11.50
EBC90	0.90	EL821	8.45	QQV06/40A*	49.50	6/30LS	0.90	6J5GT	0.90	19G6	10.35
EBC91	0.90	EL822	9.95	QV03/12	5.75	6AB7	0.70	6J6	0.85	19H5	38.00
EBF80	0.95	ELL80SE	4.50	SP61	1.80	6AC7	1.15	6J6W	2.80	20D1	0.80
EBF89	0.80	EM80	0.85	TT21	43.70	6AG5	0.60	6JE6C	5.90	20E1	1.30
EC52	0.65	EM87	2.50	TT22	48.30	6AK5	0.95	6JS6C	6.40	20P1	0.65
EC91	4.40	EY51	0.90	UABC80	0.75	6AK6	6.50	6JU6	5.85	25L6GT	1.60
EC92	1.85	EY81	0.75	UBF80	0.70	6AL5	0.60	6K7	1.45	25Z4G	0.75
ECC81	0.95	EY86/87	0.60	UBF89	0.70	6AL5W	0.85	6KD6	6.50	35W4	2.80
ECC82	0.95	EY88	0.65	UCC84	0.85	6AM5	6.50	6L6	4.60	85A2	1.40
ECC83	0.75	EZ80	0.70	UCC85	0.70	6AM6	1.50	6L6GC	4.20	85A2*	2.55
ECC84	0.60	EZ81	0.70	UCH42	2.50	6AN8A	2.50	6L6GT	1.95	807	2.20
ECC85	0.75	GM4	8.90	UCH81	0.75	6AQ5	1.75	6L18	0.70	807*	3.40
ECC88	0.80	GY501	1.30	UCL82	0.95	6AQ5W	2.30	6LD20	0.70	812A	44.80
ECC189	0.95	GZ32	1.05	UF41	1.35	6AS6	1.15	6LQ6	5.90	813	28.50
ECC804	0.90	GZ33	4.20	UF80	0.95	6AS7G	4.95	6Q7G	1.30	813*	68.50
ECF80	0.95	GZ34	1.05	UF85	0.95	6AU6	0.90	6SA7	1.80	829B	16.00
ECF82	0.95	GZ34	3.20	UL84	0.95	6AX4GT	1.30	6SG7	1.80	829B*	24.00
ECF801	0.95	GZ37	3.95	UM80	0.90	6AS5GT	1.30	6SJ7	1.80	866A	5.05
ECH42	1.20	KT66	15.50	UM84	0.70	6B4G	7.40	6SK7	1.35	866E	9.80
ECH81	0.70	KT77*	16.10	UY82	0.70	6BA6	0.85	6SL7GT	0.85	931A	13.95
ECH84	0.80	KT88	17.00	UY85	0.85	6BA6	1.50	6SN7GT	1.60	931A*	19.80
ECL80	0.70	KT88*	23.00	VR105/30	1.45	6BE6	0.65	6SQ7	0.95	954	1.20
ECL82	0.75	ML4	2.80	VR150/30	1.80	6BE6	1.20	6SR7	4.60	955	1.20
ECL85	0.75	ML6	2.80	X61M	1.70	6BG6G	1.60	6V6G	1.50	956	1.20
ECL86	0.90	MX120/01	29.50	X66	1.80	6BJ6	1.30	6V6GT	1.30	5763	5.75
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Modular test equipment

A range of modules enables an engineer to build and configure an automatic testing facility or programmable logic controller. The range is called MATE (modular automatic test equipment) and systems of almost any complexity can be built with these rack-mounted IEC-size cards. A 43-way connector is used and this enables all signals to be routed through the backplane, leaving the front free for servicing and calibration. All connections to the outside world are opto-isolated, or operated through relays to provide robustness and practicality in the sometimes harsh environment of the factory floor.

A simple bus system is used between the modules which is designed to communicate with the eight-bit ports of a 6521 or 6821 p.i.a. on a computer.

The module range includes a 16-way digital input interface; an 8-relay output; an 8-way lamp (or solenoid/relay) driver; an auto-ranging voltmeter with an 8-way input selector; programmable power supply with an 8-way distribution switch and a special adaptor to accommodate blade connectors. Peter Levesley Consultancy Ltd, 67 Birmingham Road, Aldridge, Walsall, W. Midlands WS9 0AJ. **EWW 208 on the reply card.**

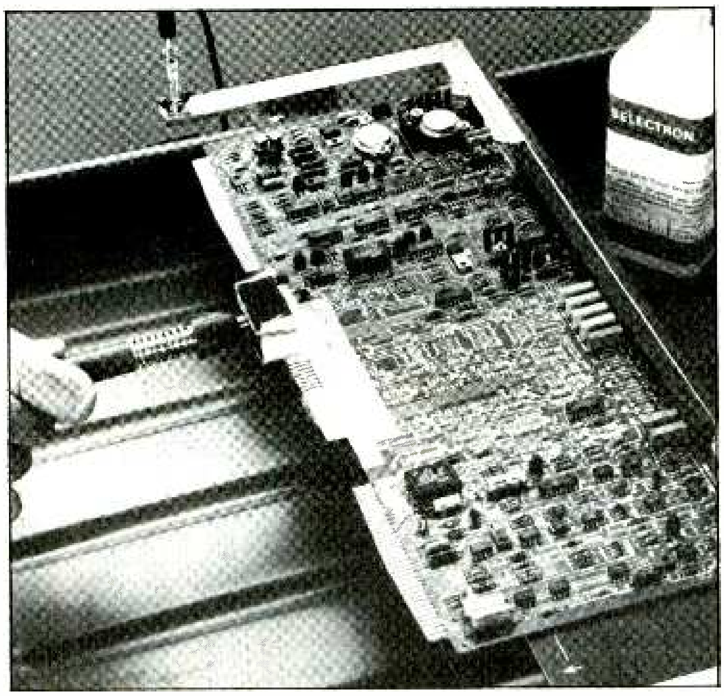
Ram-disc for G-64

A plug-in ram board has been designed to provide high-level language compilation in development systems, and to speed up handling of large data arrays in applications. The SYN-RD512 offer 512Kbytes of d-ram which can be accessed in the same manner as a disc. The memory is particularly suited to systems based around the 6809 and 68008 processors, running the OS-9 operating system. The memory slots into the G-64 valid peripheral address space and requires only four bytes of computer address space. Syntel Microsystems, Queens Mill Road, Huddersfield, HD1 3PG. **EWW 206 on the reply card.**

Circuit-board repair system

A method of plating p.c.b. tracks has been developed by Selectrons. It allows the deposition of metal onto selected areas with a minimum of masking and relatively small quantities of the plating solution. The operation is carried out by using a stylus with a suitably shaped graphite tip, (the anode) which is wrapped in absorbent material to hold the solution. This is connected to a d.c. power pack and there is an earth return. A built-in amp-hour meter monitors the thickness of the deposit.

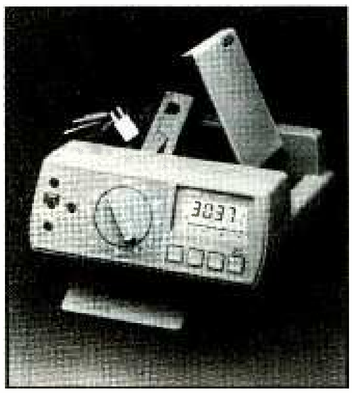
Selectrons provide the solutions as well as the equipment to plate with nickel, gold, rhodium, copper and lead. The system can cope with such areas as plated through holes. It may also be used to plate complete prototype boards. Selectrons Ltd, 38 Walkers Road, Moons Moat North, Redditch, Worcs B98 9DH.
EWW 207 on the reply card.



Bench/portable d.m.m.

Fluke's new digital multimeter includes a bargraph analogue display for simplifying the detection of peaks and nulls. It has a min/max mode which allows the retention of minimum and maximum reading over any period, e.g. overnight; and touch-hold mode so that readings can be captured and read when the probes are removed. A differential mode displays the difference from a preset value. A continuity bleep is also included.

The meter is provided with comprehensive overload protection. It is powered from a standard 9V battery which will provide about 1000h of operation. D.c. accuracy is 0.1% and there is a wide bandwidth for a.c. measurement.

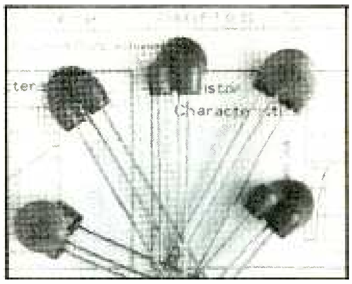


The case includes a hinged compartment for leads, probes and tools. Model 37 costs £187. Fluke (GB) Ltd, Colonial Way, Watford, Herts WD2 4TT.
EWW 215 on the reply card.

Interference supressor

A three terminal device combines the functions of a varistor and capacitor and so functions as a by-pass capacitor but also connects any high voltage surges to ground. The addition of ferrite beads to form a 'T' filter in the device means that noise suppression characteristics are better than with capacitors alone and high-frequency noise to above 60MHz is effectively removed.

The DSS710 EMI-Guard operates as a 2200pF, 12V d.c. capacitor in parallel with a 22V varistor. The ferrites increase lead inductance to 0.8μH each (at 1KHz). Rated current for the device is 7A, and the device in self heating, allowing it to cope with pulses of up to 600V. Murata Erie Electronics (UK) Ltd, 100 Albert Street, Fleet, Hants GU13 9RN.
EWW 223 on the reply card.



Miniature crystals for low frequencies

A series of quartz crystals has been produced specifically for use in series oscillators. The CX-IH products from ETA is available in a wide range of standard frequencies, together with 10KHz to 2MHz leadless versions for direct surface mounting. These are additions to the IQD catalogue of frequency control devices. IQD Ltd, North Street, Crewkerne, Somerset TA18 7AR
EWW 205 on the reply card.

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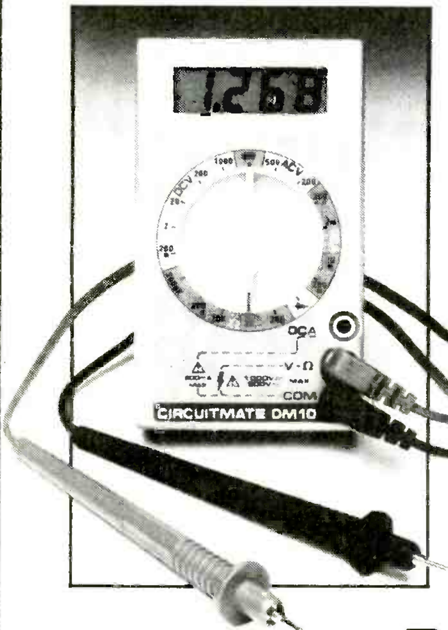

This 3½ digit multimeter has a basic DC accuracy of 0.8%, compared with 3% of full scale on most low-cost analogue instruments. For around £32.

Measuring only 4.75 x 2.75 x 0.95 in, the DM 10 is light in weight and easy to carry in a shirt pocket. It features DCV, ACV, Ohms and diode test, with fuse protection on current ranges.

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CIRCLE 32 FOR FURTHER DETAILS

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Single-chip microcontrollers

Based around a fast 16-bit c.p.u, Intel's MCS-96 family of microcontrollers include five 8-bit i/o ports, a p.w.m. analogue output and a 10-bit a-to-d converter. The devices will address up to 64Kbytes of memory and have 8Kbytes of rom/eprom plus 232bytes of ram on chip. Also provided on the chip are a full-duplex serial port and a supervisory timer.

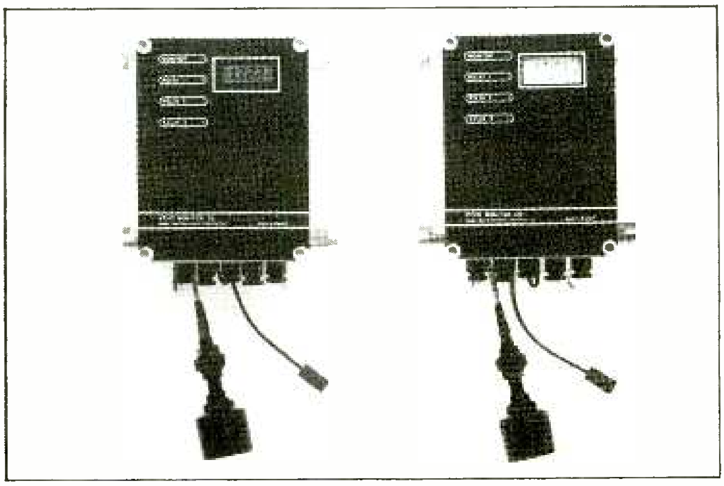
The controller chips are available in a variety of packages, with a variety of variations, to suit differing applications. Emulation and development packages are available. Rapid Silicon, Rapid House, Denmark Street, High Wycombe, Bucks HP11 2ER.
EWW 211 on the reply card.

Tenfold power for IBM PC

A plug-in processing board for the IBM PC, AT or compatibles incorporates the 68020 32-bit processor and a megabyte of ram to provide greatly improved speed and ability. An example is provided by the prime number Sieve of Eratosthenes benchmark; a PC took 108 seconds, IBM AT took 34s and the Software Engine, as it is called, 6.5s. The board is produced by Intelligent Software in the UK and they claim that a computer fitted with this board has the equivalent power of a multi-user minicomputer.

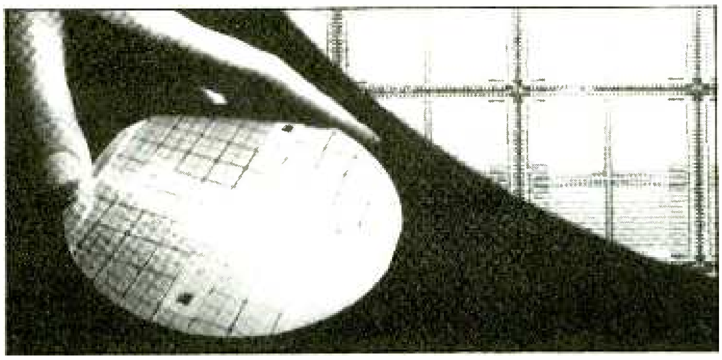
I.S. see the board being of most use in graphics simultions, computing model simulations, and for artificial intelligence research. Recent demonstrations have been running Lisp, the AI language.

The Engine runs directly under CP/M 68K software. Assembler, C, Pascal, Fortran, Lisp and Prolog are all available. PC-DOS interface assists in accessing existing PC software. The computer uses to the full the PC's own processor and the 68020 running in parallel and can transfer data at 300Kbytes/s. The PC acts as an i/o processor for the Software Engine. I.S. Concepts Ltd, 340 High Street, Chadwell Heath, Romford, Essex RM6 6AJ.
EWW 219 on the reply card.



Ultrasonic rangefinder

At £299, the Echo-Monitor is claimed to bring non-contact level monitoring within the reach of those who usually have to put up with mechanical or other contact devices, at a fraction of the cost of similar rival devices. The monitor uses a small, sealed, rugged ultrasonic transducer which communicates with a control box. A temperature sensor is provided to allow compensation for variations of the speed of sound in air. The control box has an analogue or digital meter which can supply a read-out of the distance of the transducer from the target, or a percentage of the distance between preset maximum and minimum. It is possible to preset three levels and provide relay switching when the levels are reached. The instrument offers an accuracy of 1mm over a measured distance of 2m with an alternative model with a resolution of 10mm in a 10m range. Space Age Electronics (Industrial) Ltd, Spalding Hall, Victoria Road, Hendon, London NW4 2BE.
EWW 209 on the reply card.



Racal expands gate array series

The Racal family of c-mos gate arrays has been expanded by the introduction of a 9500-gate device using a high-density layout technique. RM19500 uses a double metal process and a 'sea of gates' design system to achieve greater density. This eliminates the routing channels of conventional layouts and reduces the die size while maintaining the high gate-count. Routing channels are created over the top of unused gate areas. Full use of the die in a well-structured circuit would employ about 80% of the gates. Circuits with large amounts of random logic can still achieve 50 to 60% usage.

Extensive computer-aided design support is available for the new array. The chip has 146 i/o connections available and can be configured into a number of different packages. Racal Microelectronic Systems Ltd, Worton Grange, Worton Drive, Reading, Berks RG2 0SB.
EWW 220 on the reply card.

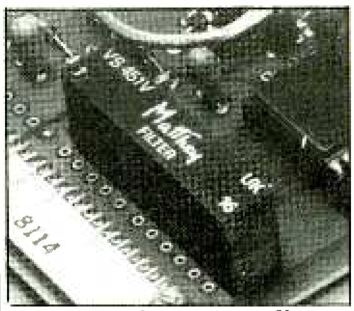
Improved transistor for tv line output

Thicker pins and mounting base make the BU208A a direct replacement for tv line output transistors. The chip is fully bonded to the base to achieve optimum heat transfer and thus reduce temperature rise. This results in lower failure rates and better performance in high-load conditions. The transistors are all fully tested. Stahnsdorf transistors are available through Edicron Ltd, 1 Wesley Avenue, London NW10 7BZ.
EWW 218 on the reply card.

Brick wall filter for video

A pass-band filter from Matthey, for the PAL "I" system allows video signal up to 5.56MHz to pass unhindered. Above 5,95MHz however they are offered a >40dB brick wall, which is how the filter gets its name. This represents a sharpness factor of 1.07. The NTSC version cuts at above 4.2MHz to reduce the audio sub-carrier at 4.5MHz by 40dB. Group delay ripple is adequately controlled.

Other new video products from Matthey include a zero loss delay line for broadcast quality video. This is fully phase equalized and offers switchable steps of 2ns in ranges up to 183ons with 1ns fine trim.



There is also a range of low-pass filters which are much smaller than their equivalents and offer considerable saving in p.c.b. space. The MHD range of filters, up to 30MHz, are specifically designed for use in high-definition tv, with <0.1dB pass band ripple and <10ns group delay ripple. Matthey Electronics, Burslem, Stoke-on-Trent ST6 3AT.
EWW 214 on the reply card.

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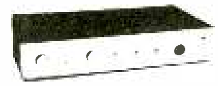

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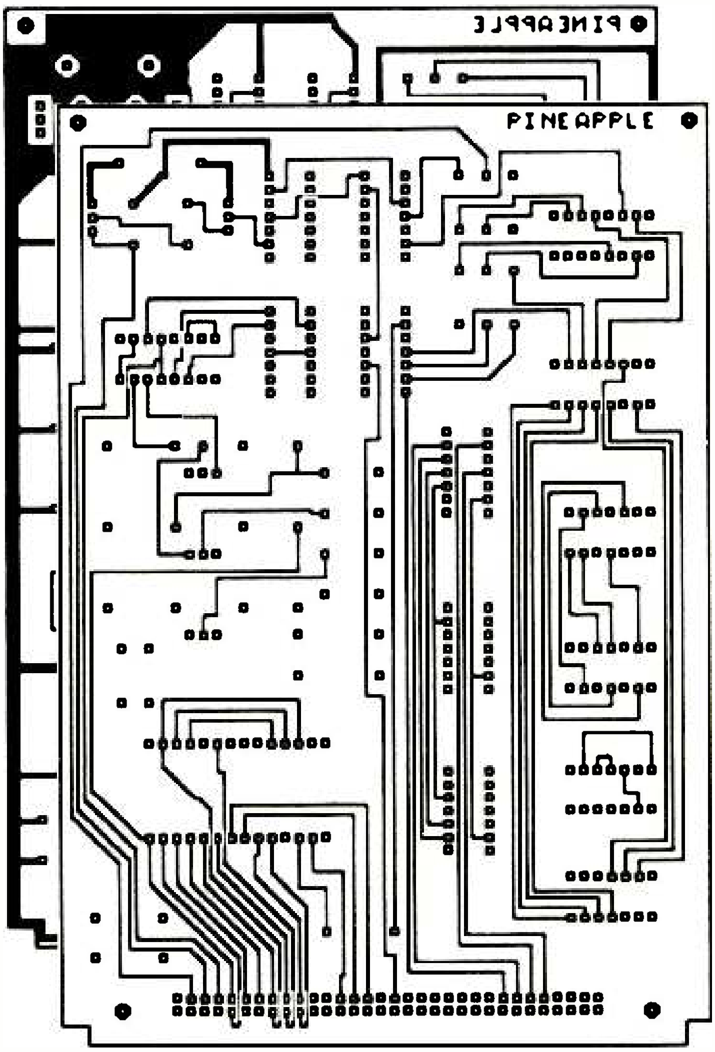
CIRCLE 10 FOR FURTHER DETAILS

www.americanradiohistory.com

PCB designer for the BBC computer



Artwork for double-sided p.c.bs can be produced by a programme that resides in a rom for the BBC computer. This leaves enough space in ram for a virtually unlimited number of tracks of any complexity for boards up to 200 by 142mm.

The printing routine significantly enhances what is presented on the screen by automatically rounding corners, straightening diagonals and adjusting the widths of tracks running between 0.1in-pitch paids. Printers with "quadruple-density" are capable of printing 1:1 overlay patterns with a resulotion high enough to allow tracks to be run between i.c. pins, as the example shows. It takes about five minutes to print one side of a Eurocard-size board.

Any size of dil i.c. package or two-pin component can be positioned using a few keystrokes. Rows of 0.1in pads can be made in one step. Configurations for other components are built by individually placing the pads, normally on a 0.1in grid. Components may be moved around the board easily before the tracks are routed. The placing of the components completes the first stage of the design, then the tracks are routed. It is possible to go back and forth between the stages but repositioning a 40-pin component after its tracks have been routed can leave quite a mess to untangle! Track routes for both sides of a board are displayed simultaneously on the screen, each side being assigned a different colour. Standard track widths are 0.25, 0.5 and 0.75in but wider tracks are possible by running track side by side. For large copper areas, a fill routine is used. Erasing tracks on one side of the board does not affect tracks on the other side. The reverse side is not printed as a mirror image.

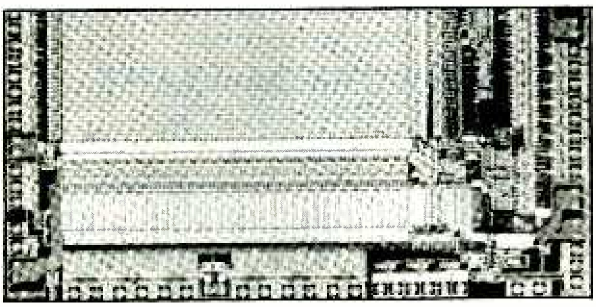
The pattern can be printed onto paper or transparent film (an old printer ribbon is recommended to avoid smudges). Paper images can be copied photographically or sprayed with oil-based liquid to make then translucent for transferring to the copper surface by u-v light.

Pineapple Software, 39 Brownlea Gradens, Seven Kings, Ilford, Essex IF3 9NL.
EWW 225 on the reply card

Digital signal processor from Inmos

By taking an analytical look at the functions of a digital signal processor, Inmos identified the multiply/accumulator as the bottleneck to high-speed signal processing. This has resulted in a radical new design, the IMS A100, which incorporates no less than 32 of the 16 by 16bit multipliers together with registers and control logic arranged to give a fully programmable digital transversal filter. It operates at rates up to 10MHz. The device is cascadeable to produce transversal filters of several thousand stages with high numerical accuracy. The processor will find use in communications, control, radar, sonar, image and speech processing. Working devices exist within Inmos, evaluation trials are progressing and the device will be available to cusotmers on October 1. Inmos Ltd, PO Box 424, Bristol BS99 7DD.

EWW 226 on the reply card.



High-output moving coil pick-up

No additional pre-amplifier is needed for the new Ortofon X-series moving coil cartridges. This has been achieved through the use of a specially shaped samarium cobalt magnet and ultra-thin (18μm) copper wire on the armature which allows many more windings with no increase in mass. The mV output matches normal phono inputs to amplifiers. Ortophon also claim a new low cost as they are able to automate the production of these cartridges with no degradation in performance. Ortophon Manufacturing A/S, 11B, Mosedalvej, DK-5000 Copenhagen-Valby, Denmark.
EWW 227 on the reply card.

High-voltage d.c. converters

Two units from K.E. Developments are pin-compatible with other similar devices and are offered as replacements. Types B5/180 and C5/180 provide 180V at 15mA from a stablised 5V supply. Operating with an efficiency of about 75% at full load, they are suitable for driving many types of gas discharge displays. Other input and output voltages are available with isolation up to 500V. K.E. Developments Ltd, The Mount, Toft, Cambridge CB3 7RL.

EWW 228 on the reply card.

www.americanradiohistory.com

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BBC MODEL B

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- ☆ Rubber Banding for drawing lines.
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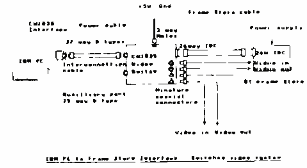
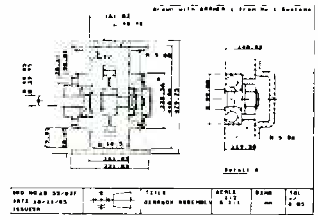
- ☆ Output to standard dot matrix printer.
- ☆ Prices from – £45 ex VAT.



MINIMUM HARDWARE REQUIRED:
- ☆ BBC Model B.
- ☆ Single or Dual 5.25" Disc Drive – 40 or 80 track.
- ☆ T.V. or monitor.
- ☆ Games Joystick, Mouse or Trackerball.
- ☆ Dot Matrix Printer (Epson 80 series or Epson compatible – BBC default mode preferable).



For further details please write or phone quoting Dept W.W.

Number One Systems Ltd 1

Crown Street, St Ives, Huntingdon, Cambs. PE17 4EB. Telephone: St Ives (0480) 61778 Telex: 32339

CIRCLE 54 FOR FURTHER DETAILS

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BOARD CODE: ☆ PLATED THROUGH HOLE ● SINGLE SIDED

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6502	3.30	2.80	74LS541	45	35	27256-250	3.90	3 70
6522	3.30	2.80	8155	1 50	1 30	6116LP-3	1 30	1 15
74LS138	.30	25	8251	1 50	1 30	6264LP-15	2.30	2.10
74LS139	30	.25	8253	1 50	1 30	4164-15	0.90	0 75
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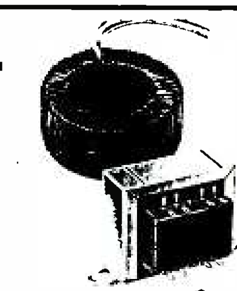
CIRCLE 36 FOR FURTHER DETAILS

Toroidal & E.I. Transformers



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MAIL Order Price List (prices inclusive of VAT & Postage)

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15VA **7.95**, 30VA **9.18**, 50VA **10.16**, 80VA **11.36**, 120VA **12.07**, 160VA **14.20**, 225VA **15.51m** 300VA **17.04**, 500VA **22.10**, 625VA **24.66**, 750VA **28.75**, 1000VA **44.82**.
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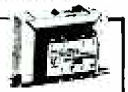
Also available 1k2, 1k5, 2k, 2k5, 3k. Prices on request.



E.I. transformers (clamp)
6VA **2.90**, 8VA **3.40**, 12VA **4.20**, 15VA **4.75**, 25VA **5.40**, 50VA **6.50**, 100VA **13.02**.
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Input 240 output 110V. rating continous/tool
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AIR LINK

Air Link Transformers.
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CIRCLE 20 FOR FURTHER DETAILS

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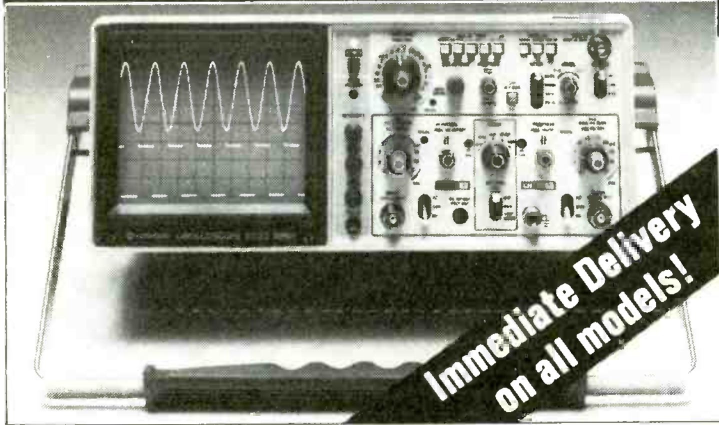
Hitachi Oscilloscopes

the highest quality the most competitive prices from **£299** +VAT



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CIRCLE 28 FOR FURTHER DETAILS

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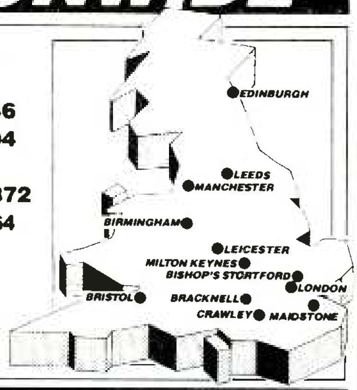

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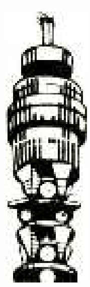

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Salary scale £8,238 – £9,327 plus £1,494 London Weighting Allowance.

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Duties include general studio work, rigging, boom operation etc., and sound recordist duties on location with both film and video recording crews.

Experience or knowledge of sound techniques is required.

This post is suitable for job share.

Application forms and further details from Personnel Services Division (PER/PS 4a), Room 366, The County Hall, London SE1 7PB.

The closing date for completed application forms is 29 August 1986.

Applicants should be aware of and committed to the Authority's Equal Opportunities Policy.

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WAVERLEY ELECTRONICS

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Appointments

Inner London Education Authority
LEARNING RESOURCES BRANCH
Television & Publishing Centre, Thackeray Road, SW8 3TB.

Assistant Vision Engineer
(Lighting) (ST1/2)

Salary Range £6,222 – £9,327
Plus £1,494 London Weighting Allowance.

An Assistant Vision Engineer (Lighting) is required to work, as part of a team taking responsibility for the quality of television pictures recorded. The assistant vision engineer will be particularly concerned with the rigging, adjustment and maintenance of lamps and operation of telecine.

Candidates should have suitable technical background and qualifications and a good working knowledge of appropriate equipment.

This job is suitable for job-sharing.

Application forms and further details are available from Personnel Services Division, (PER/PS4A), Room 366, The County Hall, London SE1 7PB.

Closing date is 29th August 1986.

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Computing Technician Grade 4

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Closing date: 1 August 1986.

Salary scale: £6,429 to £7,395 plus £1,365 London Weighting

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Applicants should have relevant HNC, HND, Advanced City & Guilds, BTEC/TEC Higher Certificate or equivalent qualifications in appropriate subjects plus a minimum of 8 years relevant experience (including training period).

Closing date: 22 August 1986

Salary scale: £6,930 to £8,091 plus £1,365 London Weighting

Application forms and further details are available from the college. Completed application forms should be returned to PER/PS5b Room 336a, County Hall London SE1 7PB

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Inner London Education Authority
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Applicants must demonstrate a thorough understanding of and commitment to the Authority's policies on equality of opportunity.

Application form and full job description from Personnel Services Department, PS4a, The County Hall, Room 366, London SE1 7PB. Please enclose SAE.

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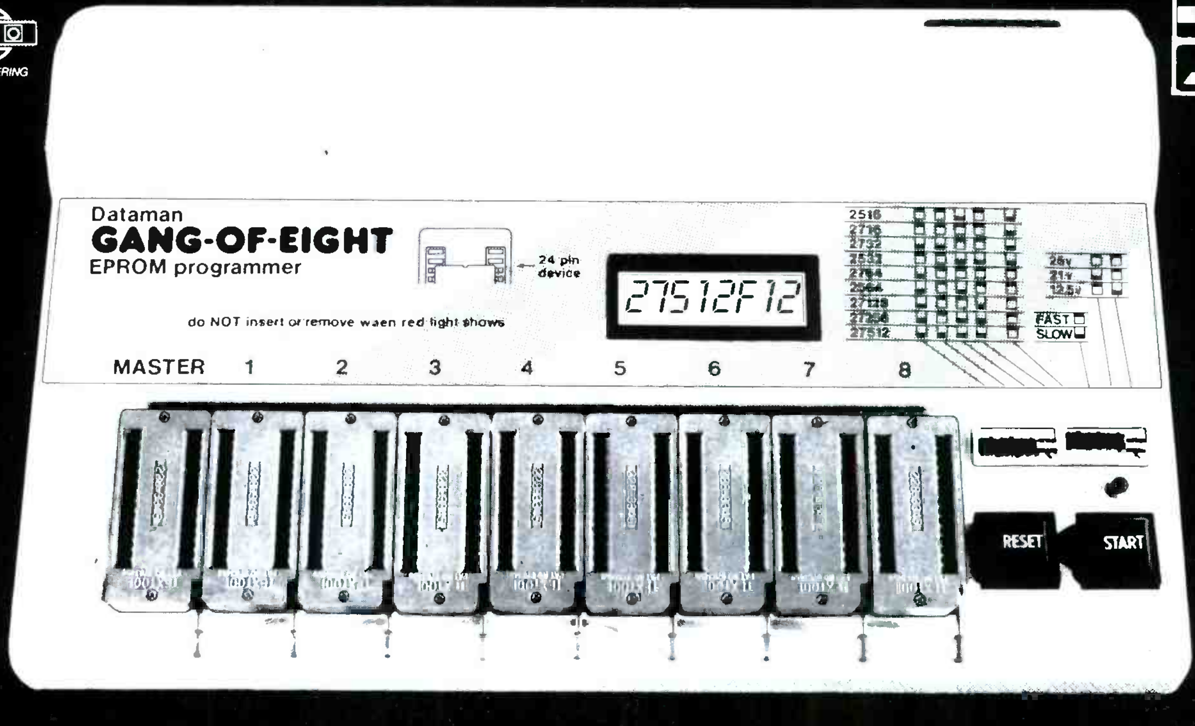

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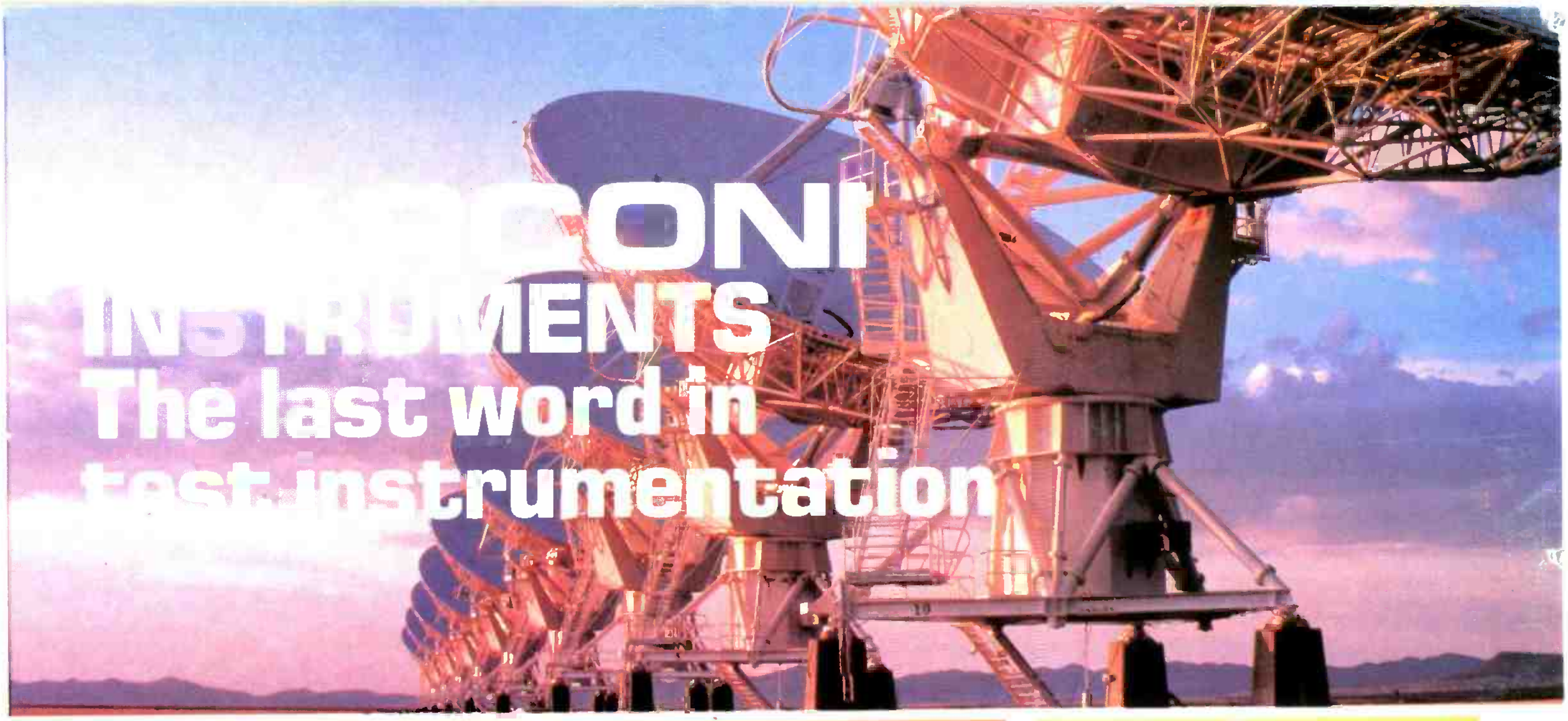

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