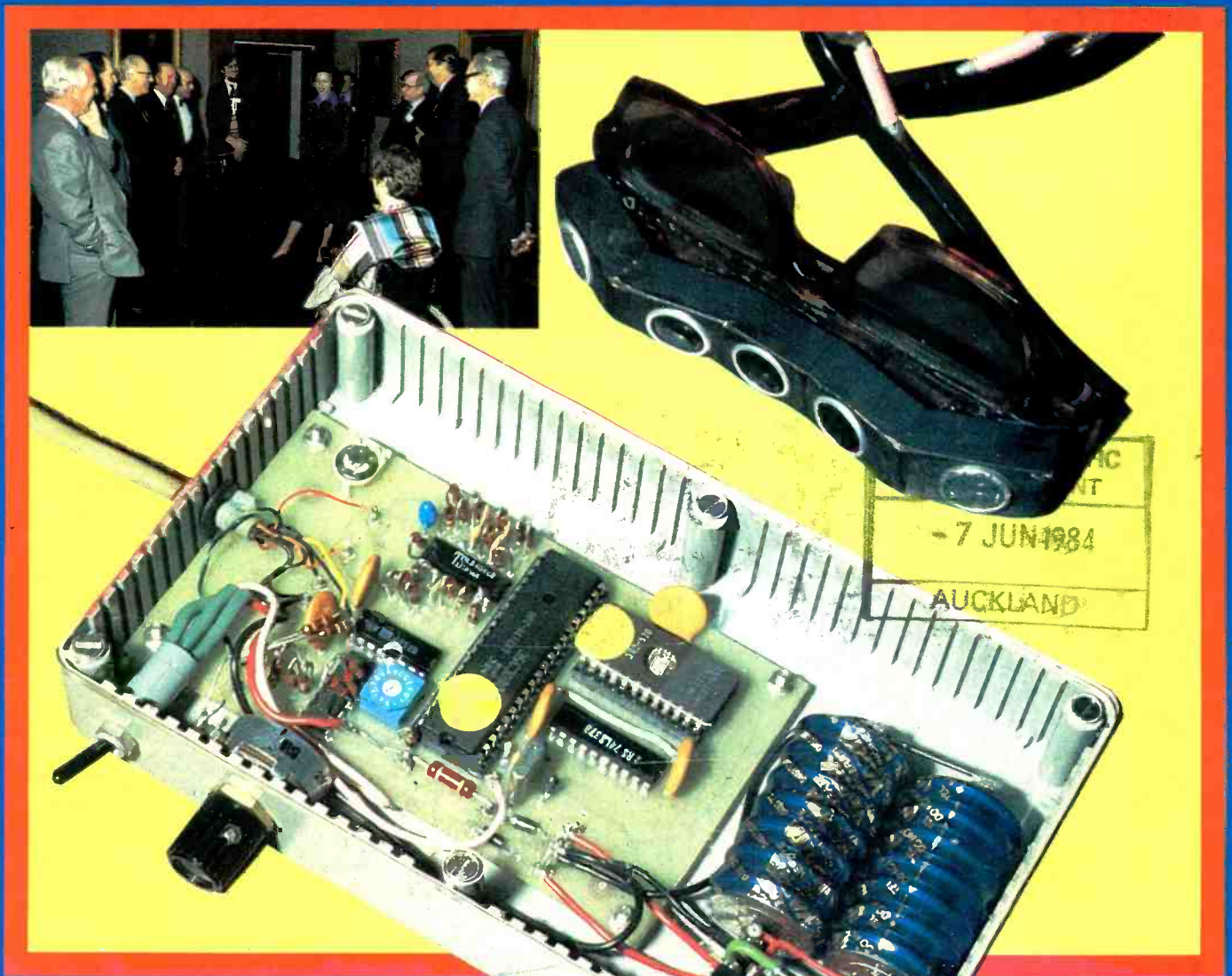


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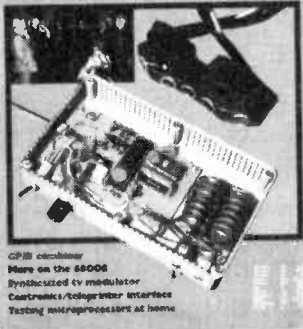
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**Competition award**



Microprocessor-based ultrasonic pulse-echo-system depicted on cover is described elsewhere in this issue by Tony Heyes.

**NEXT MONTH**

**Pausaid**, a training aid for sufferers from certain motor speech disorders. This device won second prize in *Wireless World's* recent design competition.

**Variable-speed video playback** begins a series on combining servo head tracking with digital timebase correction that allows playback to broadcast standard over a wide range of speeds.

**Dr Murray** chose to avoid criticising Relativity Theory in his recent *Heretic's Guide*. He makes good the omission by drawing attention to one of Einstein's rare but crucial mistakes.

**Designer of WW Scientific Computer, John Adams**, describes another computer design, this time a disc-based CP/M-compatible system.

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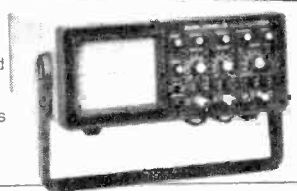
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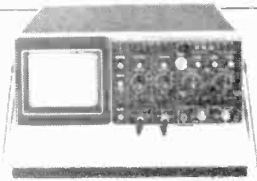
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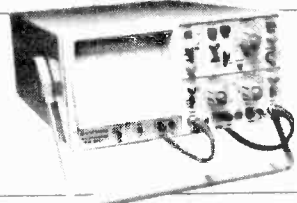
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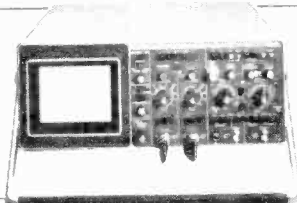


**Philips PM3217 50MHz Oscilloscope £850**  
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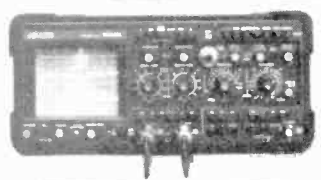
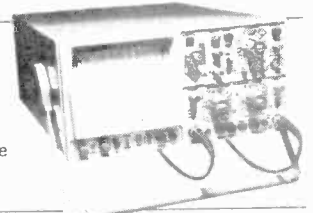


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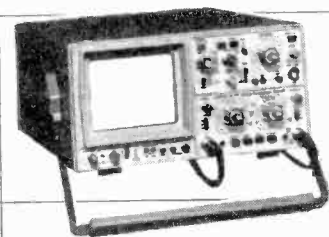
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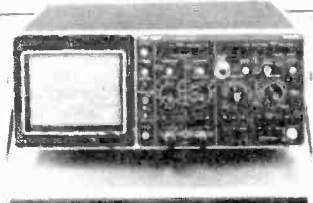


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Tough, light-weight ruggedised unit, with shoulder strap, that can be used in harsh service environments. Fast trigger circuits to over 100MHz. TTL triggering is standard. Trigger view third channel and full X-Y display. Dual trace with 2mV sensitivity and delayed time base.  
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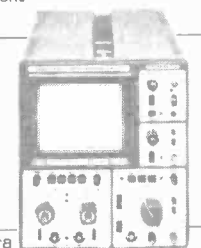


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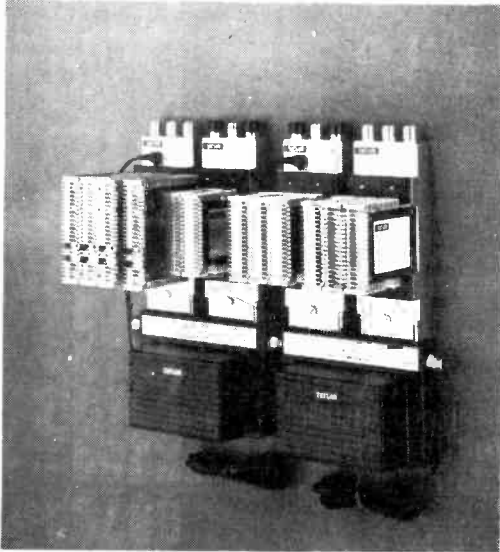


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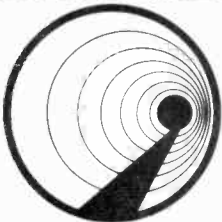
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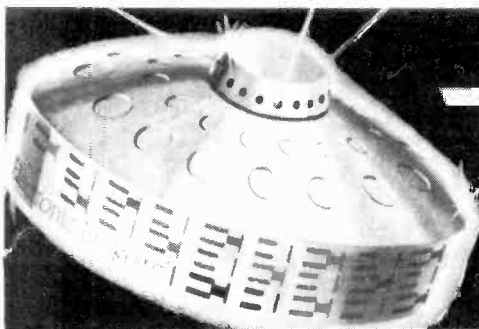
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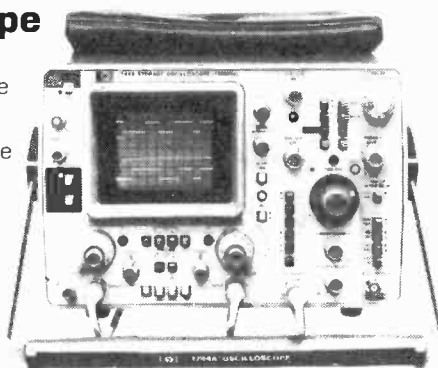
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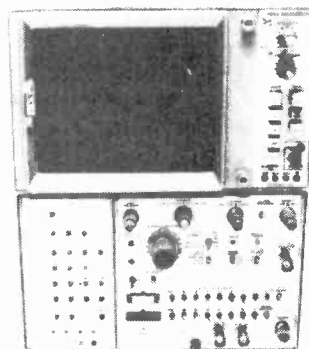
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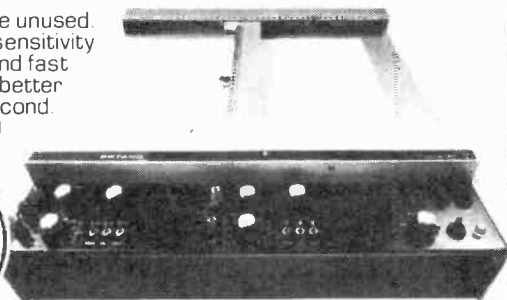


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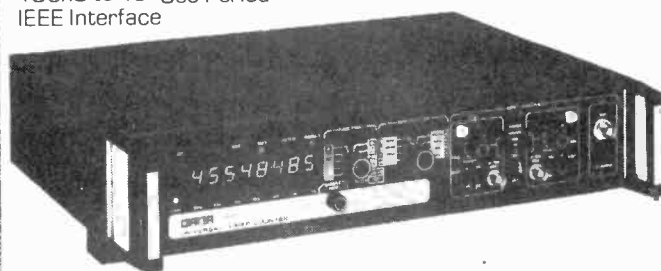
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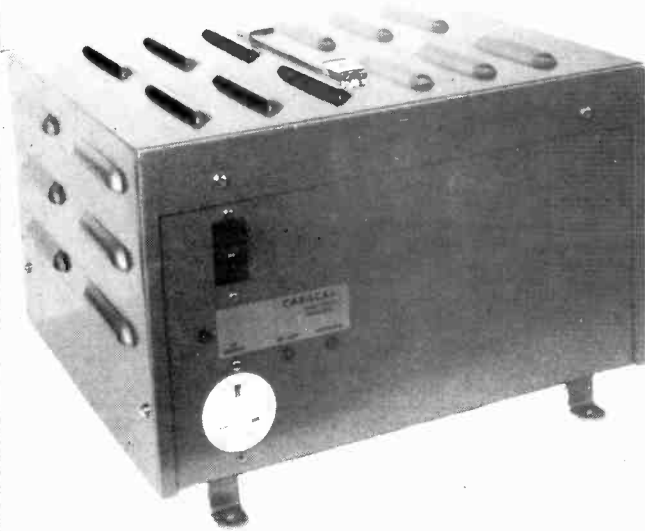
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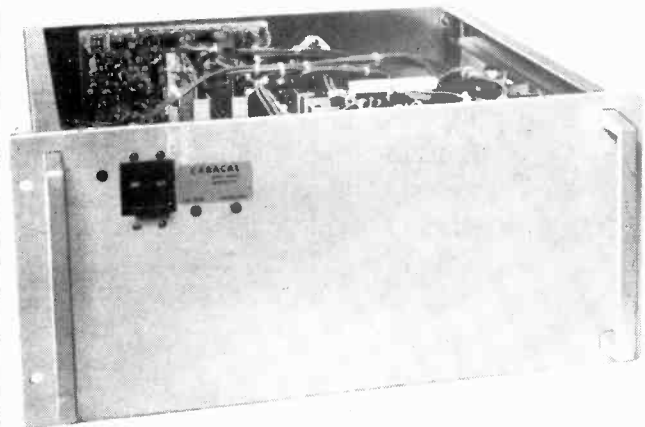
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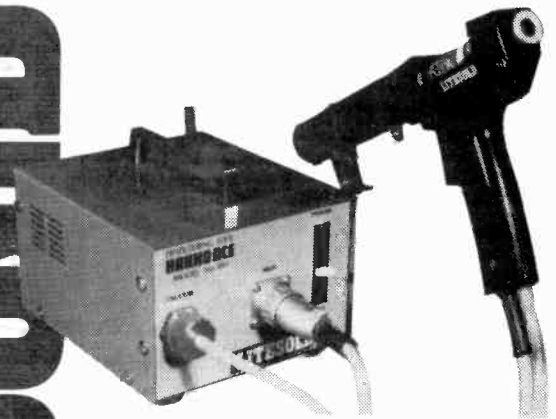
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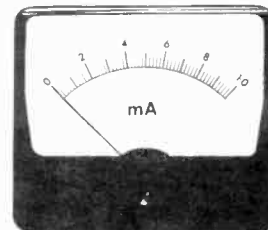
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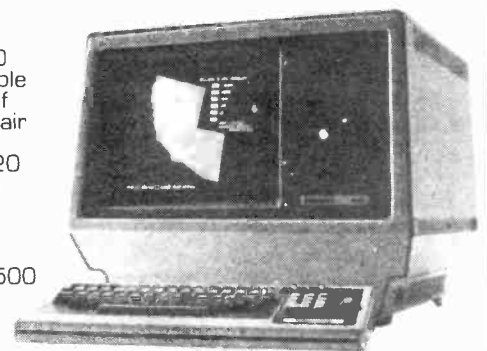
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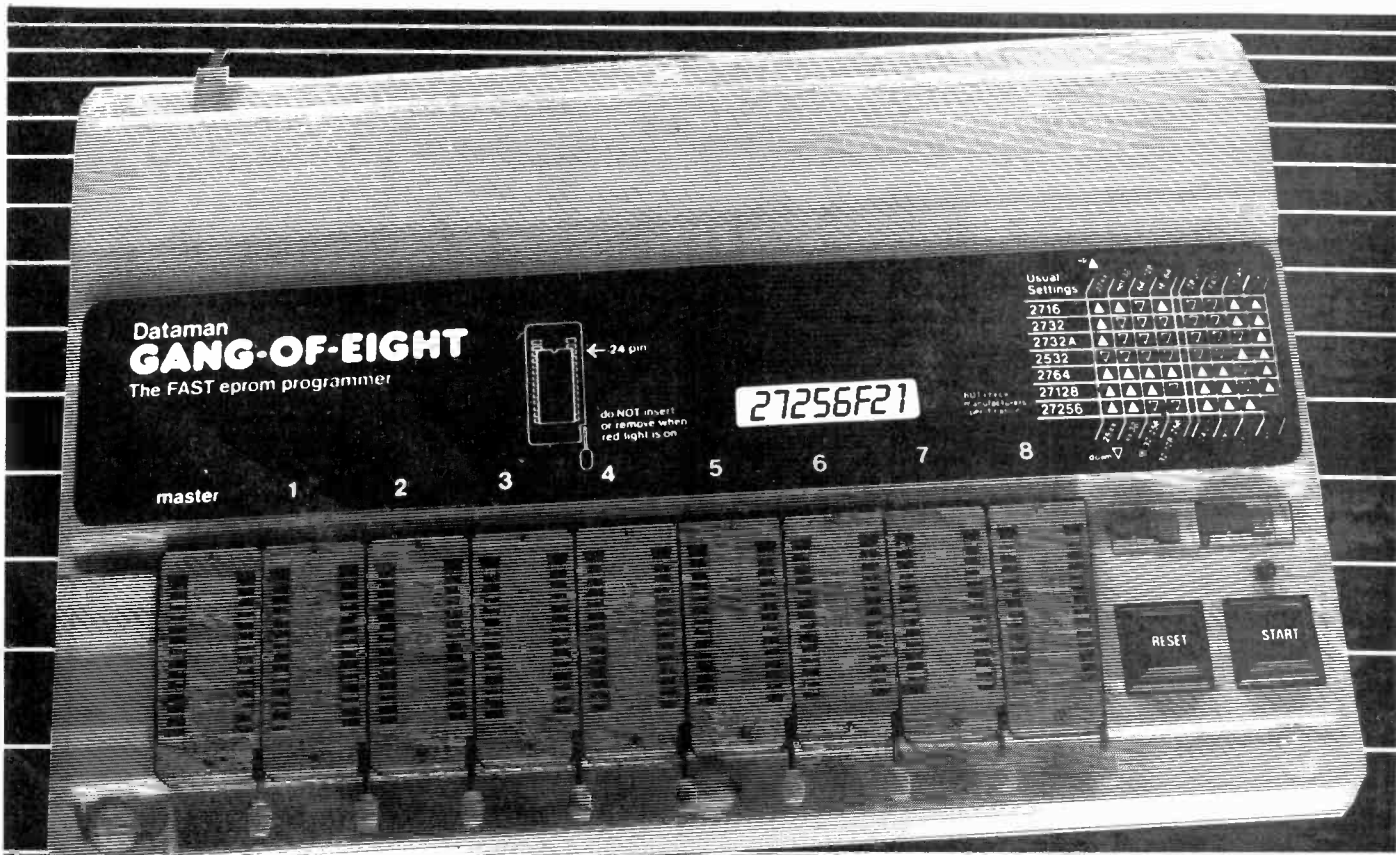
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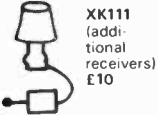
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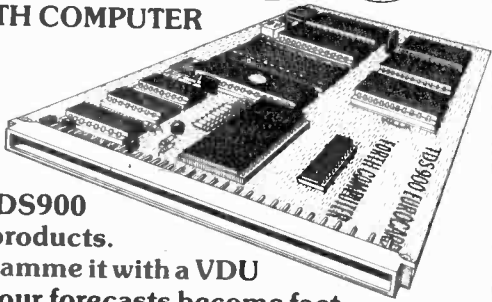
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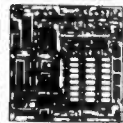
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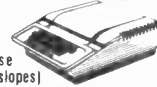
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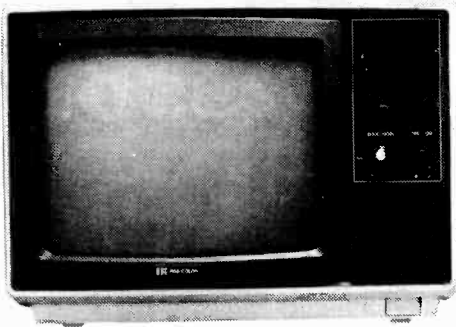
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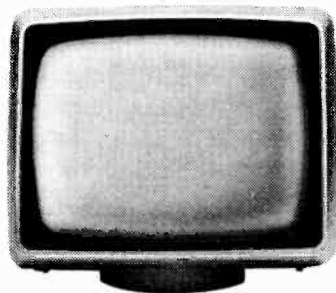


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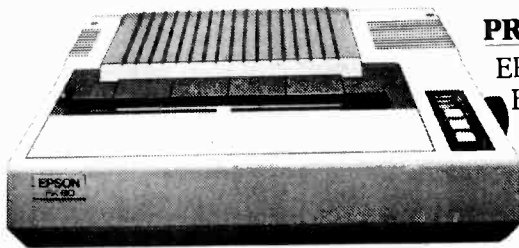
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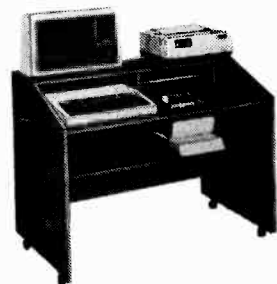
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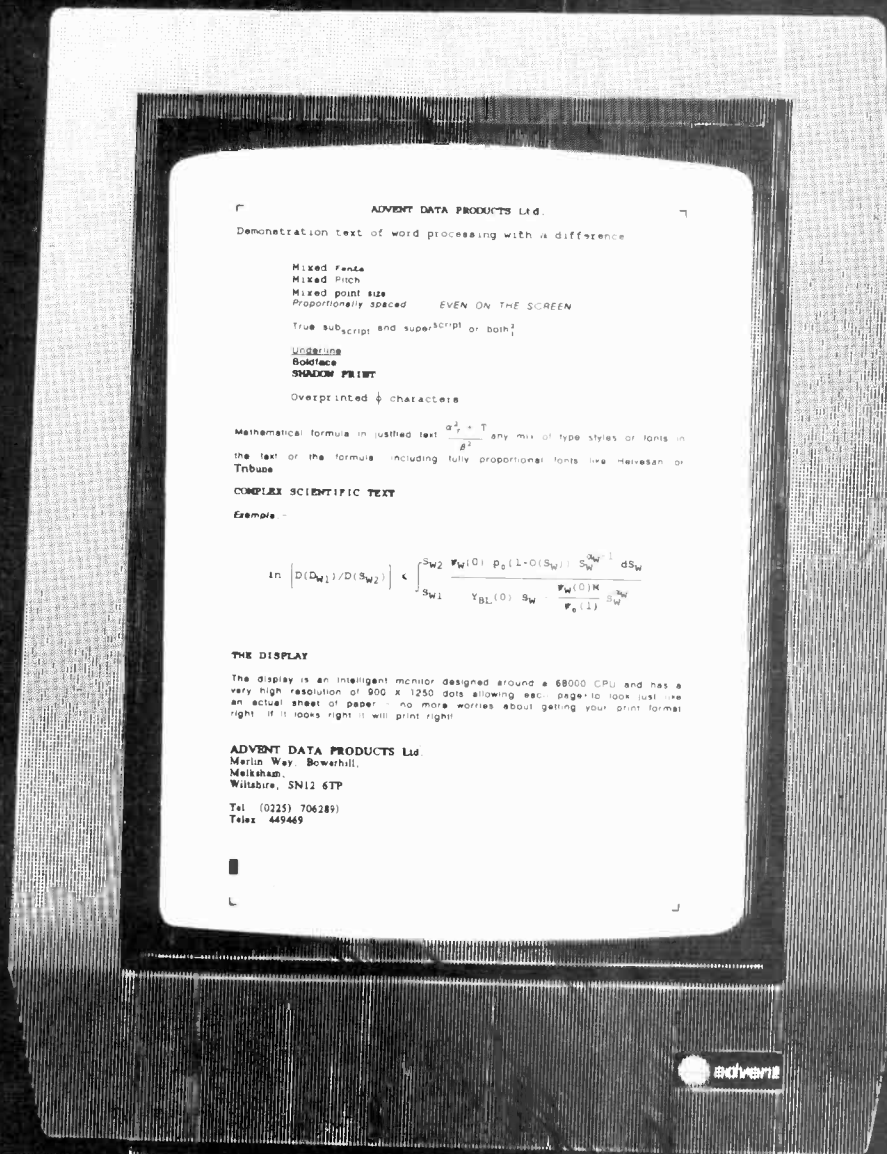
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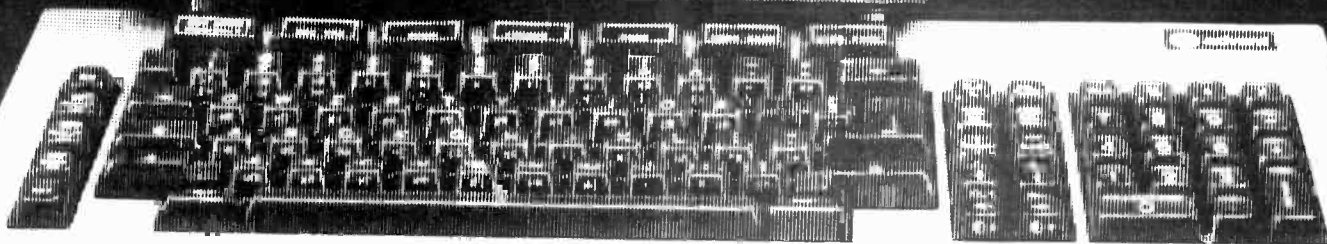


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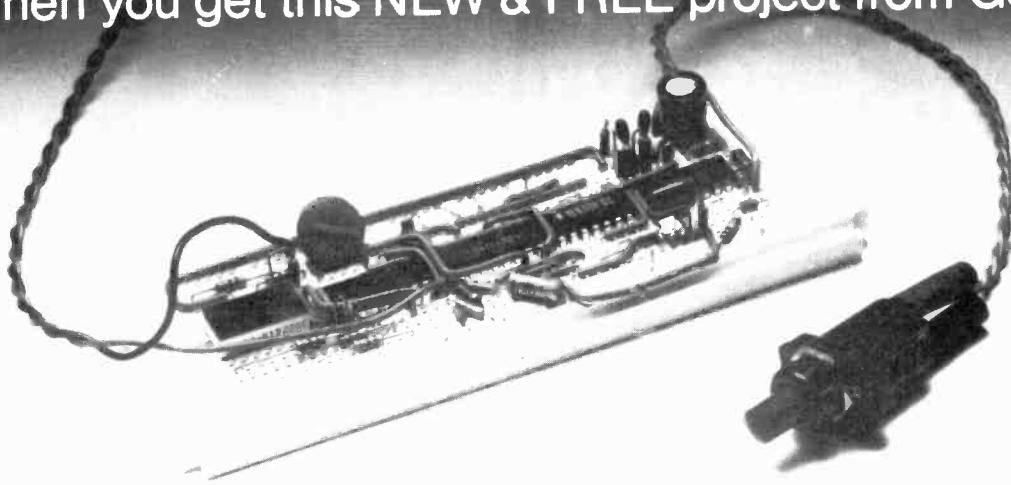
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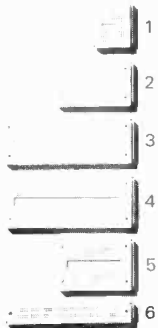
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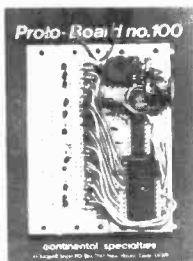


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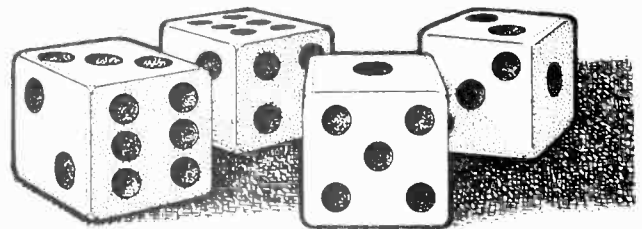
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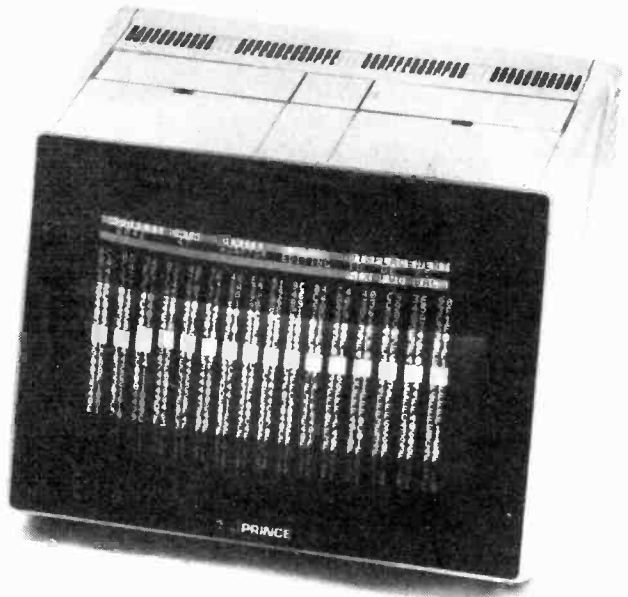
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## The mind-forg'd manacles

The affair at Government Communications Headquarters earlier this year goes much deeper than the question of banning union membership. Certainly the ban and its implications for civil liberties may well be a serious matter to some of our readers who work at GCHQ as engineers or technicians. But this dispute is only one immediately obvious sign of a more general and widespread process: the technicization of society — a process that threatens not only liberty but the very existence of democracy in what we call the free world.

If "technicization" only meant gadgets and machines to make life and work easier it would be welcome. But here we mean not just the hardware/software itself but the characteristic mode of thinking and feeling that determines the way the machines and systems are designed, the way they are used and, more recently, the way that people and machines have to interact in complex systems of command and control.

This mode of thinking and feeling is an iron in the soul of technocrats everywhere, East and West: the iron of technical necessity. Given an apparent "problem" in which certain constraints, factors and other data are fixed, there are certain options which can be clearly defined. Rational judgment shows one solution to be measurably superior to the others. It is objectively inescapable and therefore necessary. It has nothing to do with morality, wisdom, compassion or any other such human foibles. It is the "right" solution within its own terms of reference.

Sir Geoffrey Howe said that GCHQ "must provide a service which can be relied on with confidence at all times." Given the political and military premises from which this intelligence gathering system has arisen, Sir Geoffrey's "must" is a technical necessity. And the equally inescapable conclusion is that any people involved in this system must be prevented from interfering with the service it provides, regardless of their motives.

From this, a perfectly rational expedient could emerge: reduce the dependence of

the system on human beings. Systems like GCHQ could probably be made less vulnerable by increasing the ratio of machine intelligence to human intelligence. With modern information technology, and expert systems and "fifth generation" computers not far off, this outcome is more than likely.

Responsibility would be centred in the smaller group of people left in charge. They, necessarily, would be absolutely loyal to, and identified with, the system. Like "company men", they would feel a threat to the organization as a threat to themselves.

This kind of process is already happening within the organizations of modern industrial states. It is clearly dangerous. The small number of technocrats in real control of these organizations always have better, more specialized knowledge of what is happening than have the legislators and representatives of the people who are supposedly making the rules that determine our lives. As specialists they are only expected to offer guidance, but this guidance increasingly takes the form of the already-prepared decision, the logical outcome of technical necessity, which the lay legislators cannot reasonably refuse to endorse.

Representative democracy is being undermined by the information-power of technocrats who are not answerable for anything beyond the technical effectiveness of their systems.

Britain, like other industrialized nations, is no longer instinctively understood as a human, geographic and historic entity. In the minds of many it is an economic machine designed to produce a yield, the more efficiently the better. The beginnings of this mental transformation were discerned two centuries ago by William Blake. In his poem *London*, after speaking of the "charter'd" streets and Thames — places reduced to legal definitions — he exclaims: "In every voice, in every ban, The mind-forg'd manacles I hear."

# COMMUNICATIONS

## Narrow-channel tv

Ever since the early experiments in providing video telephone services in Germany in the mid-1930s, including the use of 90-line mechanical scanning, the cost of providing the necessary bandwidth has been daunting. Even when a "permanent" Berlin-to-Leipzig tv-telephone service opened in May 1936, public interest was less than expected. With two tv-telephone offices in Berlin and one in Leipzig the cost for a three-minute call was 3.50 Reichmarks, but one suspects the service was heavily subsidized.

When Bell introduced their public Picturephone service a decade or so ago it proved a commercial disaster and led most telecommunications authorities to limit their interest to teleconferences for business purposes rather than video telephones. Broadcast-quality television signals need as much bandwidth as about 960 telephone circuits, though a video telephone showing talking heads can make do with about 1.5MHz bandwidth as an analogue signal. British Telecom has been developing a 313-line colour system that uses digital transmission at 2.048Mbits/s, including speech, as part of the European COST 211 project. Analogue transmission of 1MHz analogue 313-line pictures is possible over audio-pairs of telephone lines up to distances of about 1.5km without intermediate repeaters.

A new American system of narrow-band tv has been developed by Widcom Inc. of California. This makes use of extremely sophisticated bandwidth compression to squeeze the video signal into a data stream of 56kilobits/second (i.e. bandwidth about 28kHz) which is slow enough to be transmitted over the standard digital telephone circuits proposed in the USA or with BT's System X. The aim is to provide a system that has video transmission charges no greater than for speech transmission.

Developed under American defence funding, the system provides colour pictures of talking heads, graphs and engineering drawings to a quality standard comparable with that of many consumer video cassette recorders, although quality degrades sharply if the picture is panned, since the system will not cope with fast motion.

The codec can provide bit reduction ratios as high as 1440:1 on video digitized initially at 80Mbit/s. Compression to 1.5 Mbit/s is achieved by removing spectral and spatial redundancy from the bit stream. Further compression uses temporal redundancy by frame skipping, interpolation and conditional replenishment. Compression thus makes use of five processes: filtering and subsampling of chrominance components gives 2.5:1 reduction; a 2:1 sub-sampling in each direction yields 4:1; 2d cosine transform coding for pixel-to-pixel decorrelation yields 6:1; frame skipping and interpolation 3:1; and

conditional replenishment 8:1. The current design is based on special Schottky t.t.l. and low-power Schottky t.t.l. devices, since arithmetic and logic operations up to 14-million/sec are required. The 56kbit/s systems are claimed to be already in production for Government and commercial applications. A smaller, lower-cost model is reported under development. Whether the cost of complex processing, together with picture origination and display equipment, could be reduced to the level needed for public video telephone applications remains to be seen.

## Home video pay-tv

The first pay-tv system based on the use of video-recording during the down-time of broadcast transmitters has been launched in Chicago by ABC's "TeleFirst". The idea is to provide overnight transmission of films in scrambled (encrypted) form for play-out by the subscribers at convenient times. The service aims to provide viewers each month with four major new films, some months before these are released to cable operators, plus 16 to 20 "early release" films at roughly the same time as they are available on film cable channels. Monthly subscription fee is \$25.95, but subscribers can claim a \$2 credit for any early-release film they do not wish to record.

Home video nets of this type have been advocated as alternatives to cable and DBS by Sony who are supplying the addressable decoders for the Chicago service (\$40 per home or \$75 installed). Chicago at present has about 17 per cent of homes with video recorders. TeleFirst are selling VHS and Betamax recorders from about \$400 with credit facilities.

Meanwhile cable tv continues to grow in the USA. Home Box Office is the major pay-tv film channel offered on some 5200 cable and MDS (microwave distribution system) networks with 13,500,000 subscribers by the end of 1983, a 59% increase since May 1982. Showtime had 4.75 million subscribers on 2900 systems (up 58% in 18 months) with Cinemax on 2000 systems and 2.7-million (up 87%) subscribers.

Of the "basic" cable programmes, Ted Turner's WTBS-Atlanta channel can reach 27.65-million homes on 5717 systems but has been overtaken by the entertainment and sports ESPN channel on 7074 systems having 28.5 million subscribers. Cable operators have been gaining about 400,000 subscribers a month to reach a total of over 34-million or 40.5% of all US television homes.

## Twin-oscillator amplifier

M. Nakahma and J. Ikenoue of Kyoto University have proposed a system of linear amplification using a coupled system of two synchronized oscillators with a hybrid element. Experimental verification has been achieved using two 9GHz Gunn

oscillators, but the Japanese engineers believe the technique could be applied at optical frequencies using two laser diodes. In the absence of an external signal, the two oscillators are mutually synchronized in antiphase state and output is cancelled at one port. When external signal power is fed from the port, the oscillators change towards an inphase state so that combined power appears at the port in accordance with the input power.

## Satellites and insurance

Disastrous successive failures of the booster engines on the two communications satellites launched from the Challenger space shuttle in early February seem bound to have significant knock-on effects on the costs of systems based on geostationary satellites. Insurance pay-out, including loss of revenue elements, has been estimated at well over £150-million.

In the 1960s, during the planning of the Intelsat system, a rule-of-thumb estimate was one failure in five, and this figure continued to be reflected up to about 1980 when, for DBS planning, insurance premiums to cover two launches and in-orbit for two satellites for five years were estimated at about £20-million for a £100-million project.

Insurers, however, are by nature a cautious community and it seems doubtful if today it would be possible to obtain cover on either Space Shuttle or Ariane operations at such a rate. Potential operators and insurers for DBS must also be concerned at the sparsity of in-flight life-data for high-power travelling-wave-tubes, and the relatively small number of vulnerable transponders.

Military and experimental satellites normally do not carry insurance and it is difficult to ascertain what percentage of satellites, particularly in higher orbits, successfully fulfil their missions. But it is claimed that for 12 commercial launches in 1983 no insurance claims were made.

## OECD before ITU?

The American administration is seeking to involve the Organization of Economic Co-operation (OECD) in the planning of international telecommunications policy and regulation of the radio-frequency spectrum. The aim appears to be primarily to counter the increasing politicalization of the International Telecommunications Union by providing a planning forum at American, Japanese and Western European countries could discuss radio regulatory planning and policy in advance of the ITU meetings. However this ignores the major differences between telecommunications administration in Europe and the USA and involves the risk of a further polarization of the attitudes of Third World and Eastern European bloc countries.

The FCC is currently preparing the way for the extension of the American medium-wave broadcasting band between 1605 and

# COMMENTARY

1705kHz. American radio amateurs will use 1900 to 2000kHz, with those communication services currently using 1605 to 1705kHz moving up in frequency. A problem for listeners is that many existing broadcast receivers do not extend up to 1705kHz.

FCC as part of its "deregulation" policy is withdrawing from any disputes over the allocation of call-letters to broadcast stations and will no longer insist that the call signs should be in "good taste".

Of the 5000 comments filed with FCC during 1983 on the proposal to issue "no-code" v.h.f. amateur radio licences, only about one in 20 was in favour. The proposal has now been dropped.

## AMATEUR RADIO

### Sweepers and creepers

In 1959, two Americans, N. C. Gerson and W. H. Gossard at Palo Alto, California reported the discovery of a new form of "atmospherics" that they have termed "sweepers". They described these as sounding like "clicks, tweeks, hisses and swishes" sweeping through parts of the h.f. band. Their paper (*J. Atmos. Terr. Phys.*, vol. 17, 1959, pp.82-4) speculated that these were in some way connected with Type I or Type III solar bursts. In 1977 two Indian engineers reported (*J. Inst. Electron & Telecommun. Eng (India)* vol. 23, no. 1, 1977, pp.19-21) detailed observation of sweepers between 20 and 25MHz, again ascribing the signals to a natural phenomenon. In 1978 I drew the attention of radio amateurs to these sweepers (*Radio Communication* January 1978). One result was a series of careful observations, including tape recordings, made by Ted Cook, ZS6BT in Johannesburg.

Subsequently a careful analysis was made on professional equipment in the UK of the South African recordings. These proved conclusively that the 25MHz sweepers were not natural phenomena but resulted from long-distance propagation of signals from unstable industrial r.f. heating equipment, nominally operating in the industrial, scientific and medical (ISM) frequency bands.

I see that Norman Fitch, G3FPK has recently reported similar interference in the 14MHz amateur band. There is little doubt that this originates from 13.5MHz industrial equipment, again proving that powerful r.f. generators such as welding equipment can cause interference many miles distant without being converted to an aerial. One of the clues that led to iden-

tification was Ted Cook's observation that few sweepers were heard in South Africa during the European lunch-hour!

Current industrial equipment includes 12 and 25kW r.f. generators nominally on 13.56MHz and used for such industrial processes as rapid curing of synthetic resin adhesives in the wood industry, etc. It seems surprising that more care is not taken to ensure better frequency stability and/or absence of parasitics with such high-power "transmitters".

### Grenada aided military

As further details emerge of the activities of 22-year-old Mark Barellella, KA20RK, at the Grenada medical school last October it has been admitted that his transmissions "inadvertently aided US troop movements". His transmissions were widely monitored by the media and did much to reassure the parents of the American students. The first American amateur he contacted during the invasion reminded him that the USA had no third-party amateur-radio traffic agreement with Grenada. This was waived by FCC but broadcasters were not permitted to conduct over-the-air interviews with him on the grounds that amateur radio rules strictly prohibit the use of the band for business communication. The all-news station, WTOP in Washington D.C., claimed a two-hour "scoop" in reporting that the evacuation of the medical students was about to take place, based on monitoring the transmissions from KA20RK. FCC has subsequently endorsed these activities with James McKinney, chief of the Mass Media Bureau, claiming: "I have not heard an ounce of criticism from anyone about the way the amateurs conducted those operations. Grenada constituted one more shining hour of Amateur Radio public service for the benefit of all Americans."

### Is "amateur" derogatory?

Last year I reported the feeling of some radio amateurs that the University of Surrey's Uosat project had been directed primarily towards scientific rather than amateur-radio experimentation, and had taken advantage of the facilities of the international amateur satellite service while at the same time had shown surprisingly reluctance to be associated with 'amateur radio'. The reason, it later appeared, was that the university disliked the ambiguity of the term, pointing to the dictionary definition of "amateurish" as inexpert, lacking professional skill. The RSGB which has existed to serve "amateur radio" for so many years, now appears to agree with the views of the university to the extent where it is suggested that it may run a competition to find a better name! Since the Society already frowns on the long-established term "ham" and dislikes being confused with Citizen's Band activities,

and since the term "community radio" is already spoken for, the search may be a difficult one.

Meanwhile the University of Surrey is pressing forward with construction of Uosat-B for an early launch. Again its objectives are largely scientific, and not telecommunications. It would be welcomed more enthusiastically by British amateurs if the university were less inhibited in admitting that the satellite will operate as part of the "amateur" service.

### GaAs on 144MHz?

The superior low-noise performance of gallium-arsenide devices compared with silicon devices is well-established at microwave frequencies. But in recent years the reduced cost of some dual-gate GaAs fet devices has led a number of amateurs into using these at the relatively low frequency of 144MHz, claiming exceptionally good strong-signal performance. This claim is disputed by Chris Bartram, G4GDU, of MuTek, who has found that, on measurement, the GaAs devices have third-order intercept points of the order of OdBm, roughly the same as for good silicon devices. They also have a "bath tub" noise characteristic that results in noise figures at 144MHz slightly higher than at 430MHz. He believes that the idea that GaAs devices provide exceptionally good dynamic range is largely a myth, although one that is already influencing a number of enthusiasts.

### In brief

During the flight of the Columbia space shuttle Dr Owen Garriott, W5LFL, recorded identifiable calls from 290 stations including about six in the UK. The number of real-time two-way contacts however was Vt is hoped that amateur radio operations will be repeated in some future flights. . . . Problems arising from leakage of cable television signals on frequencies within the 144MHz band have been reported from the British Telecom installation at Milton Keynes. . . . The death occurred last December of Eric ("Bill") Yeomanson, G3IIR, former president RSGB, who did much to establish the Raynet emergency network and to popularise the use of amateur r.t.t.y. . . . The DTI has confirmed that the installation of transceivers by short-wave listeners is legal provided that they do not use the transmitting facilities. . . . Mobile rallies at the University of Leeds on April 1, and at Pavilion Gardens, Buxton and Patti Pavilion, Swansea on April 8. . . . RSGB National Convention 1984 at NEC, Birmingham on 28-29 April will include technical sessions and an h.f. convention. . . . A new edition of "The AMSAT UK Guide to amateur satellite operation" is available to non-members of AMSAT for £1.25 including postage (AMSAT-UK, 94 Heron-gate Road, Wanstead Park, London E12 5EQ). PAT HAWKER, G3VA

WW Design Competition  
First prize winner

# Sonic Pathfinder

*A programmable guidance aid for the blind*

The Sonic Pathfinder is designed to give the independent blind traveller information relating to objects in and to the side of his path. It presents only that information relevant to safety and efficiency, and displays the information in an easy to understand format. The device does not aim to provide a surrogate for vision, rather to provide a limited amount of supplementary information over and above that obtained from the user's other senses. In common with all previous electronic travel aids for the blind the aid is not able to provide protection against holes in the ground; consequently, this is a 'secondary aid' to be used in conjunction with a cane or a dog.

## General description

During the last fifteen years many electronic guidance aids have been developed by engineers and physicists and introduced to the blind. They have met with almost total failure. In response to the problem so created – namely, that devices which clearly are capable of providing the blind user with much of the information denied him because of his handicap are, nevertheless, found to be unacceptable – the Medical Research Council and the Department of Health and Social Service jointly created the Blind Mobility Research Unit and placed it in the Department of Psychology at the University of Nottingham. Over the years this unit has developed evaluative procedures capable of giving objective measures of a user's performance with any aid, thus enabling us to highlight the shortcomings of existing aids and to achieve an understanding of the informational requirements of the independent blind traveller. The Sonic Pathfinder is an attempt to embody, within a practical device, the many insights gained during the work at Nottingham.

The aid is an ultrasonic, pulse-echo device, mounted on a spectacle frame, and with an auditory display: Fig. 1 shows the aid being modelled by the author. The prime function of the aid is to detect and indicate the distance of any obstacle which lies directly in the blind pedestrian's path. In the absence of any obstruction ahead, it reverts to its secondary function of indicating the presence and range of obstacles to the left and right of the travel path. Like the simpler hand-held Nottingham Obstacle Detector<sup>1</sup>, the aid represents the distance of the nearest object in terms of the notes of the musical scale – one note being assigned to each of the one-foot-range zones. Again, like its predecessor,

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by **Tony Heyes**  
B.Sc., Ph.D, M.Inst.P.

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the aid is a digital device, no attempt being made to provide an analogue signal to give textural information. This is done to avoid information overload. Moreover, if a blind user really wants to distinguish between a tree and a lamppost he can reach out and discover this by touch.

The user listens to the display through two small earpieces, one mounted on each side of the spectacle frame in close proximity to, though not actually in contact with, the ear. Time division multiplexing is employed between the three receivers and the two earpieces so that the distance of any object which lies, within range, to the left of the main travel path is signalled only in the left earpiece whilst an object to the right is signalled only in the right earpiece. An object which lies directly ahead produces a signal at both earpieces and, in this way, creates a central sound image. In the absence of any obstacle within the area viewed by the aid the display is totally silent.

With the aid in use, the pedestrian is able to walk parallel to the inner shore line – the hedge or wall – by keeping the repeating note at the 'inner' ear at a constant pitch. He is at the same time able to tell when he passes a tree or lamppost on the outer shore line by the interposition of the occasional note in the other ear; such objects are vital landmarks for the blind. If he encounters an object lying directly ahead, the side information is no longer provided and information relating to the central hazard is presented to both ears. As an additional 'attention grabber' the central display is arranged to have a repetition rate four times that for the side information – some 16 times a second. Only when the hazard is circumnavigated does the aid revert to giving side information.

Early prototypes of the aid were made using c.m.o.s. integrated circuits. A number of these prototypes have been evaluated using blind volunteers<sup>2</sup> and the results have been most encouraging. However, some shortcomings were identified during the evaluation. For example, although users were advised to switch the aid from long range to short range – from 8 ft. down to 4 ft. – when trying to negotiate narrow openings, they tended not to do so. By changing to a microprocessor-

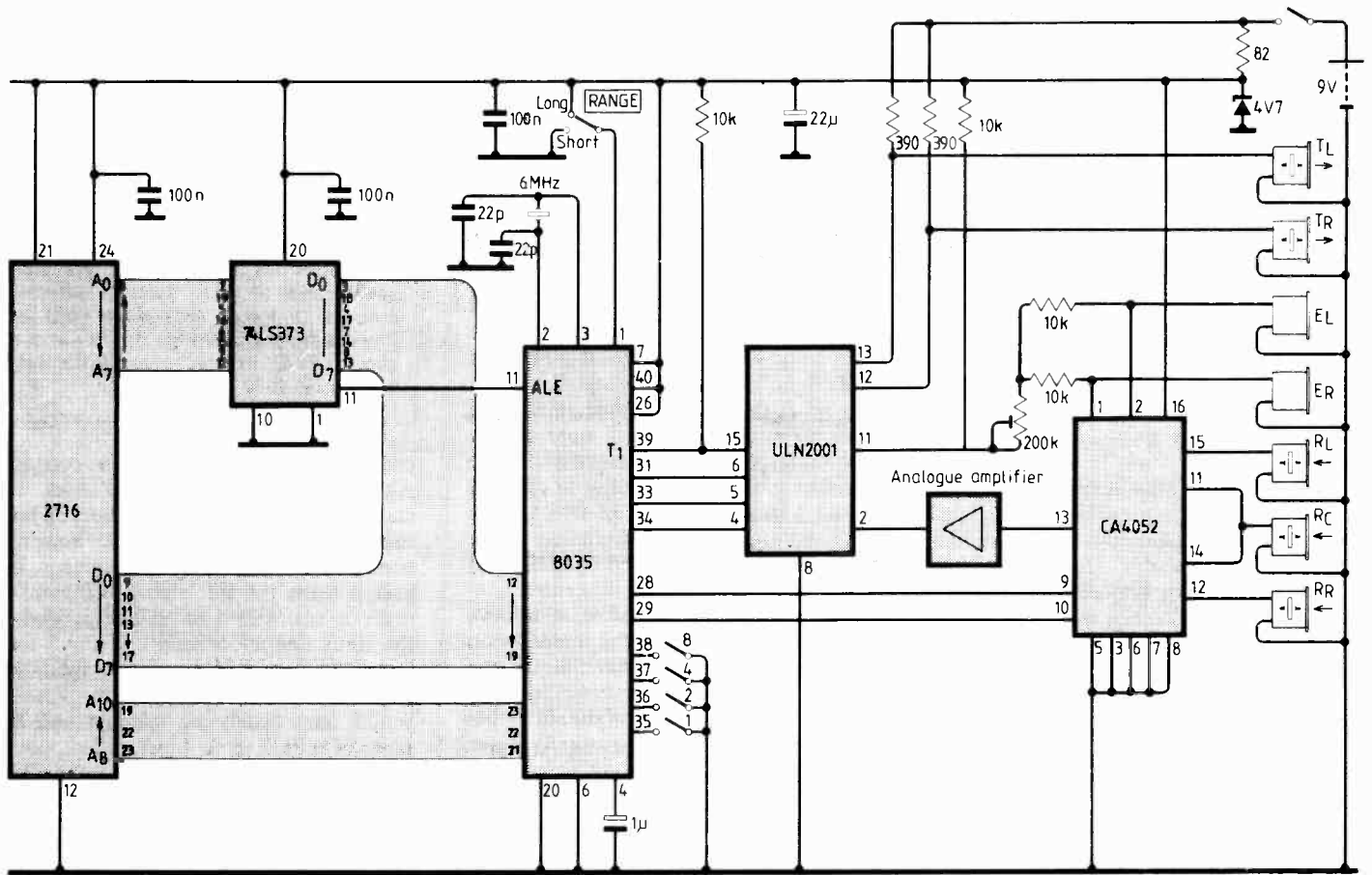


Fig. 1. Dr Heyes wearing a prototype of the Sonic Pathfinder.

based system it has been possible to develop software information processing algorithms and thereby achieve an automatic adjustment of the range. These techniques are discussed later.

## Circuit description

Use has been made of the Intel 8048 family of microprocessors<sup>3</sup>. Referring to the circuit diagram shown in Fig. 2, it is seen that, for convenience of programming, the prototype devices use the 8035 version of the microprocessor in conjunction with an external memory, the 2716, and associated latch, the 74LS373. When the software has been finalized, the program will be masked into the internal memory of the low-power, c.m.o.s., version of the 8048. All outputs are taken from port 1. Those for the two transmitters,  $T_L$  and  $T_R$ , and that for the display output, are buffered via a Darlington driver. Outputs P11 and P12 are used as control lines for the c.m.o.s.



**Fig. 2.** Main circuit diagram of the guidance aid.

two-pole analogue switch, the 4052. One pole of this switch is used to select the current receiver transducer and the other to short out one of the earpieces when the side receiver transducers are in use, or neither earpiece when the centre receiver transducer is in use. The analogue receiver in Fig. 3, is based on the LS404 quad amplifier and is designed to have a peak response at 40kHz. I am indebted to Allan Greaves of B.T. Research for suggesting the design of this stage. The output of the amplifier is inverted using one of the Darlington drivers before being fed to input T<sub>1</sub> of the microprocessor. Other inputs to the microprocessor are T<sub>0</sub>, the short/long range switch, and the higher half of port P2 which usually sits high but may be connected to earth via a hex. switch, which is used to select various software options. All timing is derived from the microprocessor's internal clock, controlled by a 6MHz crystal. Self starting on switch-on is achieved by shorting pin 4 to earth via a 1μF capacitor.

The whole action of the aid is determined by the program, all the necessary delays and frequencies being derived from software timing loops. Many novel features are included, as will be seen from the following description.

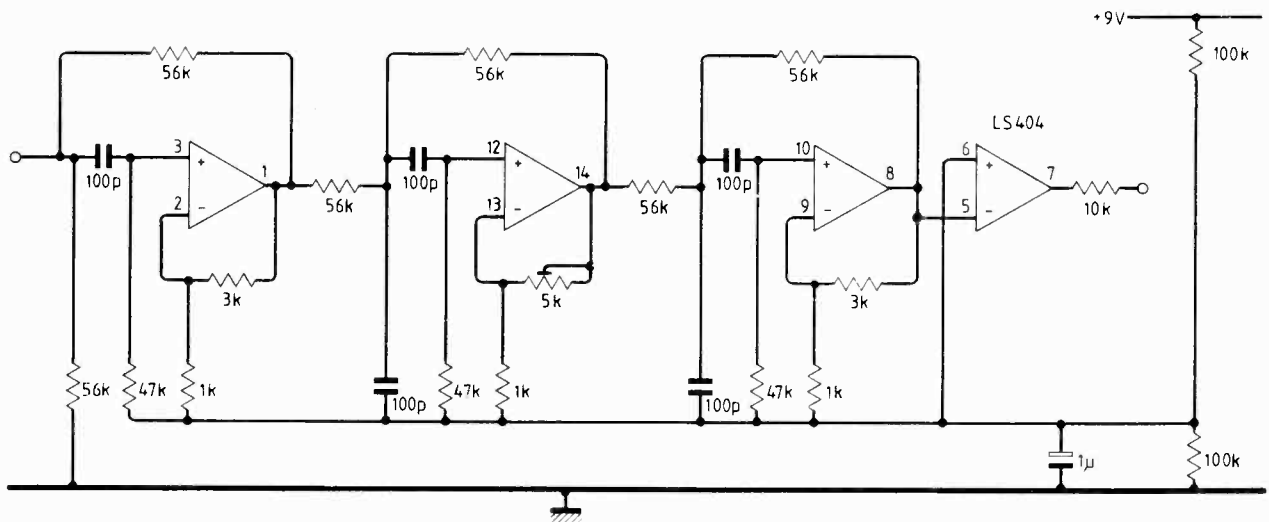
**Program**

The design involves the use of cheap, readily available transducers. In order to provide a suitably wide beam, two splayed

transmitters are used, convergently rather than divergently splayed to avoid the 'hole in the middle'. Unfortunately, using two transmitters at the same frequency produces a diffraction pattern resulting in the aid having 'corridors of insensitivity'. This is overcome by reversing the phase of one of the transmitters at appropriate intervals. The multiplexing and transmitter phasing is controlled by a single register, named MULTI, such that:

- 0 0 0 0 0 0 0 look left, out-of-phase
- 0 0 0 0 0 0 1 look centre, out-of-phase
- 0 0 0 0 0 1 0 look right, out-of-phase
- 0 0 0 0 0 1 1 look centre, out-of-phase
- 0 0 0 0 1 0 0 look left, in-phase
- 0 0 0 0 1 0 1 look centre, in-phase
- 0 0 0 0 1 1 0 look right, in-phase
- 0 0 0 0 1 1 1 look centre, in-phase
- 0 0 0 1 0 0 0 RESET TO
- 0 0 0 0 0 0 0 look left, out-of-phase

**Fig. 3.** 40kHz analogue amplifier. Amplifier i.c. is LS404.



For each step of MULTI the transmitters are activated for a 0.5 ms burst of 40kHz. Precise frequencies, both in-phase and out-of-phase, are obtained from software loops controlling the appropriate bits of the output port.

During the transmitter pulse and for a short time afterwards the receiver must remain off. This, the 'dead time' is necessary to prevent the receiver from triggering due to cross-talk. For short range pulse-echo systems it is necessary to set this time to a minimum value. However, this minimum is critically dependent upon component and wiring layout and is therefore difficult to pre-set. Using the microprocessor it has been possible to write a software routine which uses the first twenty four transmission pulses after switch-on to 'dynamically' determine and set the minimum usable 'dead time'.

The elapsed time between the transmitter pulse and the receipt of the first echo determines the musical note displayed to the user. The notes are obtained from a software timing loop, the parameters of which are obtained from a 'look-up' table.

Interference from other ultrasonic sources has been largely eliminated by the inclusion of a software-controlled digital filter: the processor has a cycle time of 2.5µs. The output of the analogue receiver amplifier is sampled every 4 cycles until a change is detected, confirmatory samples then being taken every 5 cycles, provided each one is the inverse of its predecessor; if not, after a 3-cycle delay, the 4-cycle sampling is resumed. This mixture of 3, 4 and 5-cycle sampling ensures that any 40 kHz waveform is detected, no matter what its phase relationship to the internal clock of the processor. By requiring nine successful samples before an echo signal is regarded as genuine, the digital filter has an effective bandwidth of 6kHz cycles. This is more than adequate to cater for the Doppler shift introduced in the frequency when the user is approaching the object from which the echo is received. For example, at a walking speed of 5 mile/h the received frequency is 40.5kHz.

Priority is given to objects in the centre of the user's path - Centre Echo Priority - by failing to increment MULTI when a central echo is detected. And, if after a period of repeated central echo an echo is not detected, bit 2 of MULTI is complemented and one last 'look' is taken in the centre, this time with the opposite transmitter phase inter-relation, before the aid reverts to its left/right scanning mode.

### Information-processing algorithms

The difficulties encountered during the evaluation by users trying to negotiate narrow gaps may be illustrated with reference to Fig. 4. The figure depicts a plan view of a subject standing still and facing an open doorway leading onto a corridor. Very small rotations of the head produce three different musical notes: a note of low pitch corresponding to the distance to the nearest doorpost  $d_1$ , a note of higher pitch corresponding to the distance to the corri-

dor wall  $w$ , and a note of intermediate pitch corresponding to the distance to the far doorpost  $d_2$ . The centre-echo-priority algorithm ensures that these notes are presented to both ears, giving no obvious impression of the existence of a gap. Furthermore, very small head movements produce a jangling sound which is very difficult to interpret. (The user will only realize he is facing a gap when he notices that one of the notes has a higher pitch than the other two!) How much better the information display would be if the aid had a maximum range greater than  $d_2$  but less than  $w$ ! If this were the case small head rotations would produce a note of low pitch corresponding to distance  $d_1$ , a note of higher pitch corresponding to distance  $d_2$  and a middle position in which these two notes are presented alternately to the left and right ears, giving an unambiguous indication of an opening in the centre.

It has been found possible to achieve this desirable display by the introduction of an algorithm which I have named the Ratchet. Essentially the action of the Ratchet is to reduce the range of the aid to that of the nearest object in the central region and to maintain this limited range for a certain time, the Ratchet hold time. In order to avoid numerous undesirable side-effects certain constraints must be placed on the Ratchet algorithm. For instance, referring to Fig. 4, a crude Ratchet with a hold time greater than, say, 2 seconds would result in the near doorpost - the note corresponding to the distance  $d_1$  - alone being displayed. This seems inappropriate, since the far doorpost - distance  $d_2$  - is sufficiently close that it could be encountered within the 2 second hold time, even if, as in this case, the subject is moving from a standing start. Consideration of walking speed, acceleration and reaction times have led to the action of the Ratchet being restricted to the four outer zones of the aid. Thus the Ratchet never reduces the range of the aid to less than 4 feet.

A careful choice of Ratchet hold time is crucial if other undesirable side-effects are to be avoided. In the above example a Ratchet hold time of 2 seconds was chosen, a duration long compared to the time taken for the user to make head rotations but short compared to the time required to negotiate the doorway and move into the

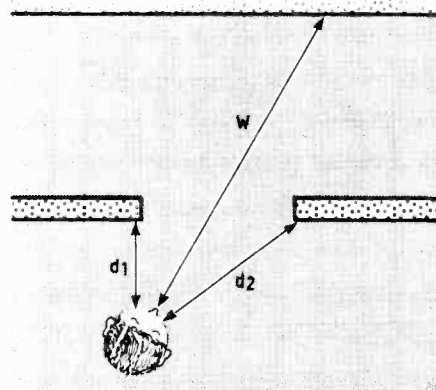


Fig. 4. Plan view of user approaching open doorway.

### The author

Tony Heyes is a Senior Research Fellow with the Blind Mobility Research Unit, Department of Psychology, University of Nottingham. Trained as a physicist, Dr Heyes went blind while researching into crack propagation at the Cavendish Laboratory, Cambridge. After eight operations the sight of one eye was saved and a new research interest created. Dr Heyes received a Ph.D. in Physics from Cambridge in 1967 and a second Ph.D. in Psychology from Nottingham in 1979.

comparative open space of the corridor. Although in these circumstances the choice of 2 seconds for the Ratchet hold time is appropriate it does, however, produce one unfortunate consequence. If a user is using the side signal of the aid in order to maintain a travel line parallel to the shore line at a distance of say 3 feet, and if he were momentarily to rotate his head towards the shore line, the Ratchet would immediately be invoked and the range of the aid set to 4 feet. (4 feet, not 3, because of the restriction described above.) Thus from that moment, for the duration of the Ratchet hold time the user has only the protection of an aid with a range of 4 feet. In these circumstances this is serious because he is not moving from a standing start and may be travelling at 4 mile/h! The solution is to use a Ratchet hold time proportional to the time the invoking object remained in 'view'. Thus a quick 'glance' towards a near object would produce a hold time considerably shorter than would a prolonged 'stare'. It does, however, remain necessary to limit the Ratchet hold time to some maximum value - 2 seconds seems to be appropriate.

Having made the Ratchet hold time dynamically determined one has, in effect, produced an aid, the range of which is governed by the walking speed of the user. That is to say, instead of an aid with a range of 8 feet, we have an aid with a range of 2 seconds! Rather an odd concept. However, given the information-processing demands inherent in independent blind travel<sup>4</sup> and the moment-to-moment problem solving nature of blind travel<sup>5</sup> it would seem highly desirable to have an aid which was limited to providing informa-

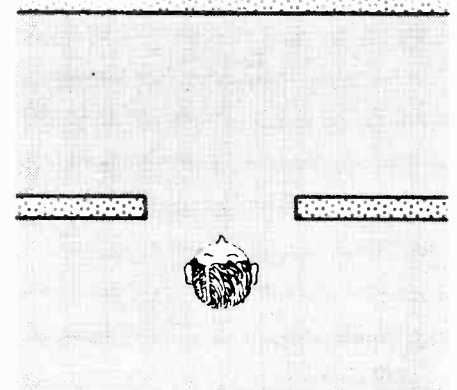


Fig. 5. User about to pass through open doorway.

tion solely about those objects which would be encountered during the next 2 seconds of travel.

Figure 5 illustrates what may happen when our blind subject takes a pace forward. Large head rotations are now required to bring the door posts into the central region of the aid and there is a high probability that the Ratchet will be released before the doorway is negotiated. When this happens the aid returns to having an 8 foot range and the Centre Echo Priority algorithm ensures that the musical note corresponding to the corridor wall is

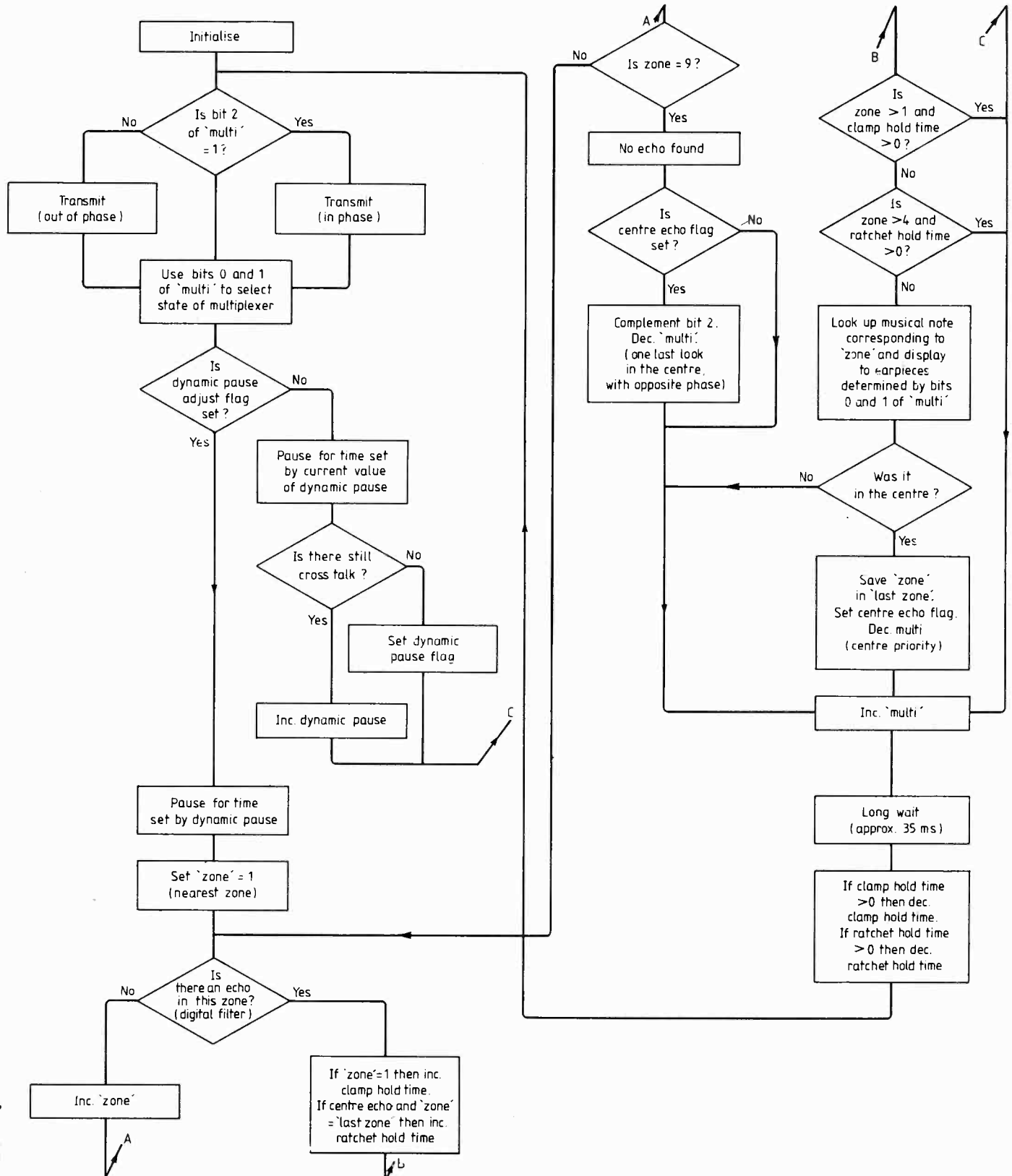
displayed rather than the side information about the door posts. The undesirable effect may be eliminated by yet another information processing algorithm – the Clamp.

The Ratchet can only be invoked and sustained by signals received in the central, forward facing receiver. The Clamp, on the other hand, may be invoked and sustained by any signal received in the nearest zone of the aid (zone 1) whether

left, right or centre. The Clamp operates for a fixed duration (1.2 seconds) and has the effect of reducing the aid to a single-zone device. By increasing the length of near zone to two feet and reducing the ranges of the other zones so that the overall range of the aid remains equal to 8 feet the Clamp provides an effective solution to the problem described with reference to Fig. 5. The presence of one or the other door post in the side regions of the near zone prevents the far corridor wall from being perceived no matter how slowly the

*continued on page 62*

**Fig. 6.** Flow chart showing information processing in Sonic Pathfinder.



# Designing with the 68008 microprocessor

*A member of the 68000 8/16/32 bit processor family, the 68008 has an internal 32-bit architecture and an eight-bit external data bus. This second article shows how it is used with other microcomputer components – rom, ram and peripheral devices.*

Interfacing the 68008 to memory, peripherals and other microcomputer devices is straightforward. The examples shown here are practical circuits using the popular 74LS z.t.l. family. When the separate examples are brought together to form a complete system numerous circuit rationalizations can be made. In the case of very high volume designs f.t.l. tends to be replaced by custom circuits.

## 68000 with rom

A practical minimum 68008-based system could employ one 8kbyte rom to contain program code and reset vectors. Fig. 3 shows the 68008 interfaced to an 8kbyte rom, MCM68764. The eight-bit data bus and the low-order address lines of the MPU are connected to the rom on a one-

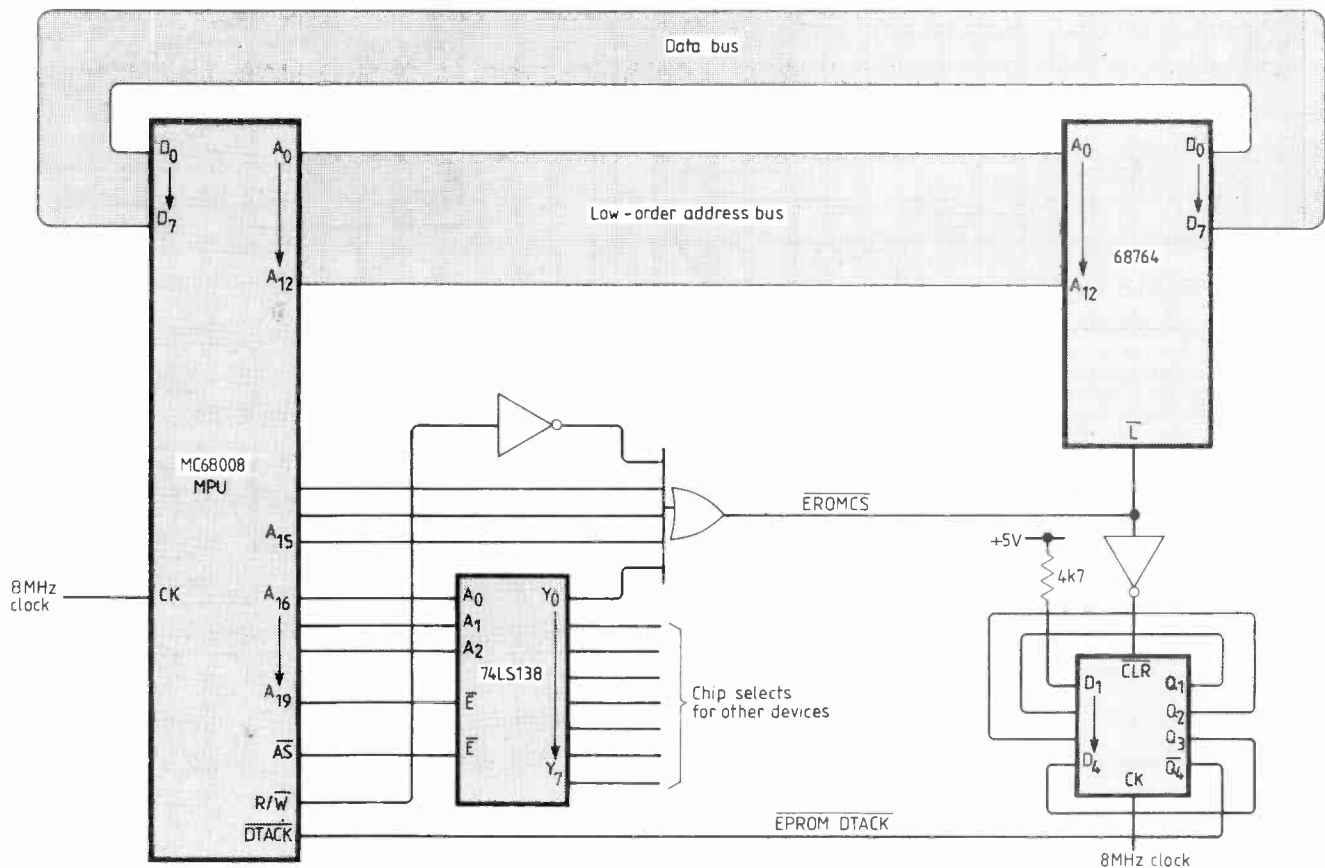
by A. J. Barth

to-one basis. The high-order address lines are used to allocate different portions of the one megabyte address space to various memory and peripheral devices in the system. A 74LS138 1-of-8 demultiplexer is driven by these lines to generate a chip-

**Fig. 3.** 68008 interfaced to rom. Asynchronous data bus enables the bus cycle time to be ne-tuned to the speed of the currently accessed memory or peripheral.

select signal for each device. The demultiplexer is enabled by the 68008 address strobe signal (AS) which indicates when a valid address is on the address bus.

During a read operation on the rom the m.f.u. sets up the read/write signal (R/W) and places the appropriate address on the address bus. Signal AS is activated by the processor enabling the demultiplexer to chip-select the rom. As part of the asynchronous bus cycle, hardware must activate data-transfer-acknowledge (DTACK), to indicate to the processor that data from the rom will shortly be valid on the data bus. A 74LS175 quad D-type flip-flop acts as the DTACK generator for the rom. The rom chip-select signal EROM/CS releases the flip-flops from their cleared state which allows a logic zero to propagate from one Q





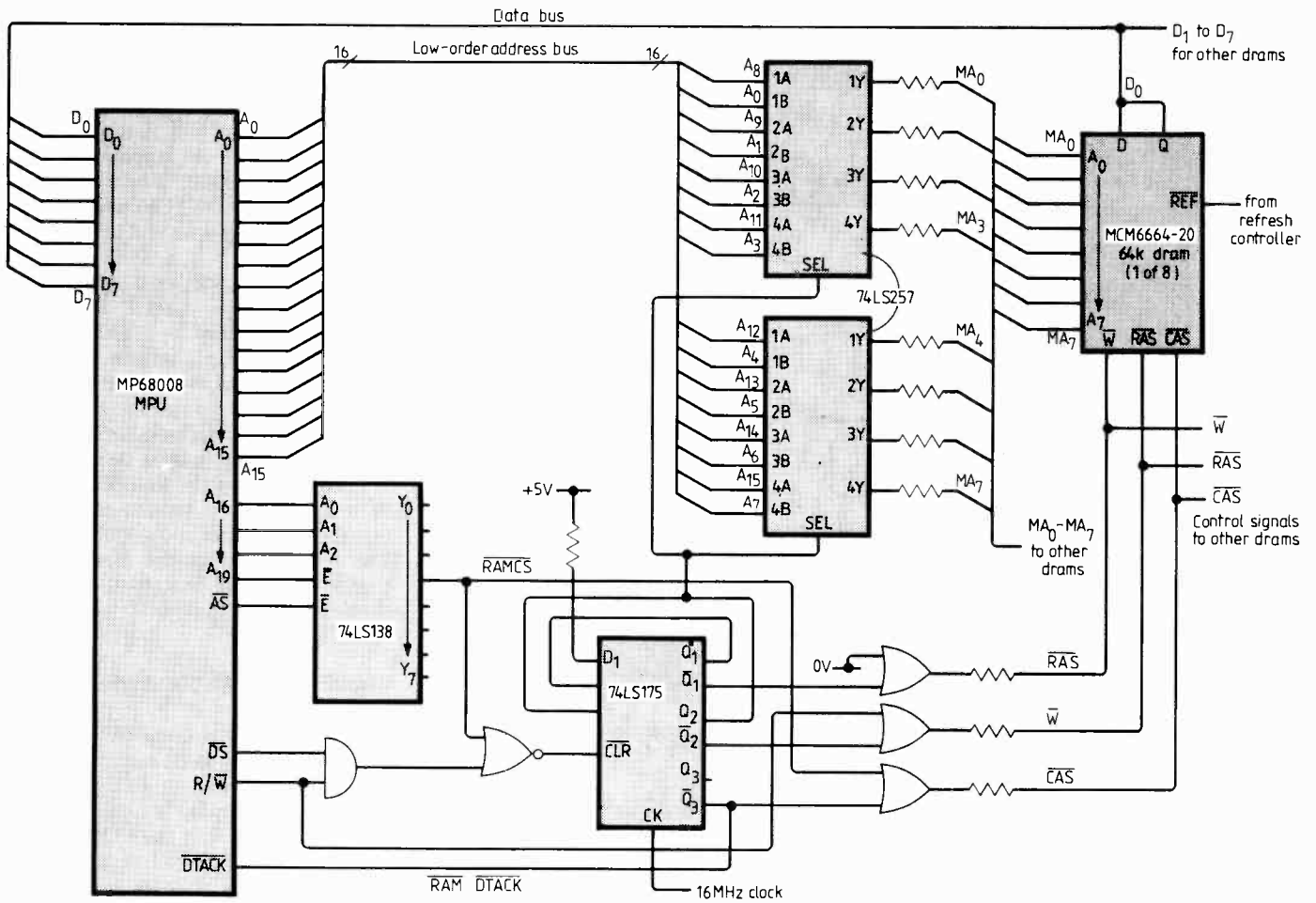


Fig. 4. 68008 interfaced to ram. High-density rams require the m.p.u. address to be multiplexed into a column and row address

an asynchronous bus are lost since the processor executes an unnecessarily long bus cycle for the faster devices. However, in a very price-conscious design where minimum device count is paramount, this may be an acceptable engineering compromise. As well as generating the ram DTACK the 74LS175 also provides the dram control signals, row address strobe (RAS), column address strobe (CAS), write (W), and the switching signal SEL for the multiplexers. AS, R/W and data

output to the next on successive rising edges of the 8MHz clock. The fourth Q output generates the active low DTACK which signals the 68008 to read the data on the data bus and to terminate the bus cycle. The DTACK delay time is governed by the number of flip-flops and the frequency of the clock, and is chosen to suit the rom access time (approximately 450ns in this case).

In this example the R/W signal and all of the high-order address lines have been included in the rom chip-select logic. This enables the detection of illegal operations such as writes-to-rom and access to some unused memory space. In a price-sensitive product this may be considered a luxury and the inverter and the five-input or-gate could be omitted.

### 68008 with ram

Interfacing the 68008 to static ram is similar to the rom case except that the read/write signal connects directly to the ram or rams and is not included in the chip-select logic. Dynamic ram interfacing is more complex because they require refreshing and address multiplexing logic. Fig. 6 shows the 68008 connected to eight MCM6664 64kbit dynamic rams providing 64kbytes of read/write memory. The D input and Q output of each dram are connected to a different 68008 data line — only one dram is shown in Fig. 4 for clarity. The 16 low-order address lines are multiplexed together using two 74LS257 quad two-input multiplexers to form the row address and column address needed by the rams.

Like the rom circuit a 74LS175 quad D-

type flip-flop is used as DTACK generator. Where the ram and rom, or any other device used, have the same data access time a single generator may be used for these devices. If a single generator is shared among several devices having different access times much of the benefits of

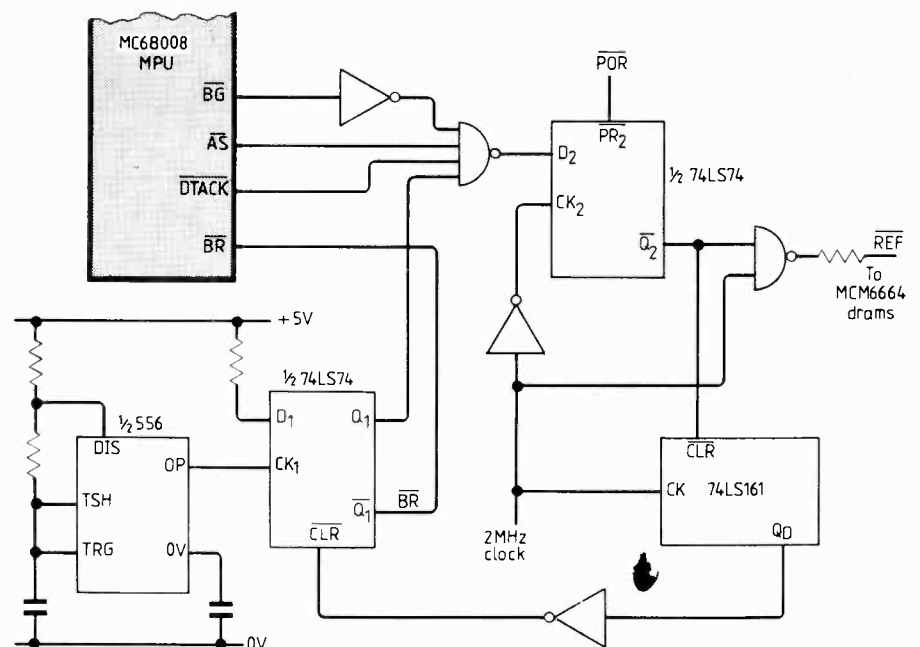


Fig. 5. 68008 dynamic ram refresh controller. The MCM6664 64K drams use a simple pin-1 refresh technique. Here the m.p.u. operation is temporarily suspended while a block of eight internal memory rows are refreshed.

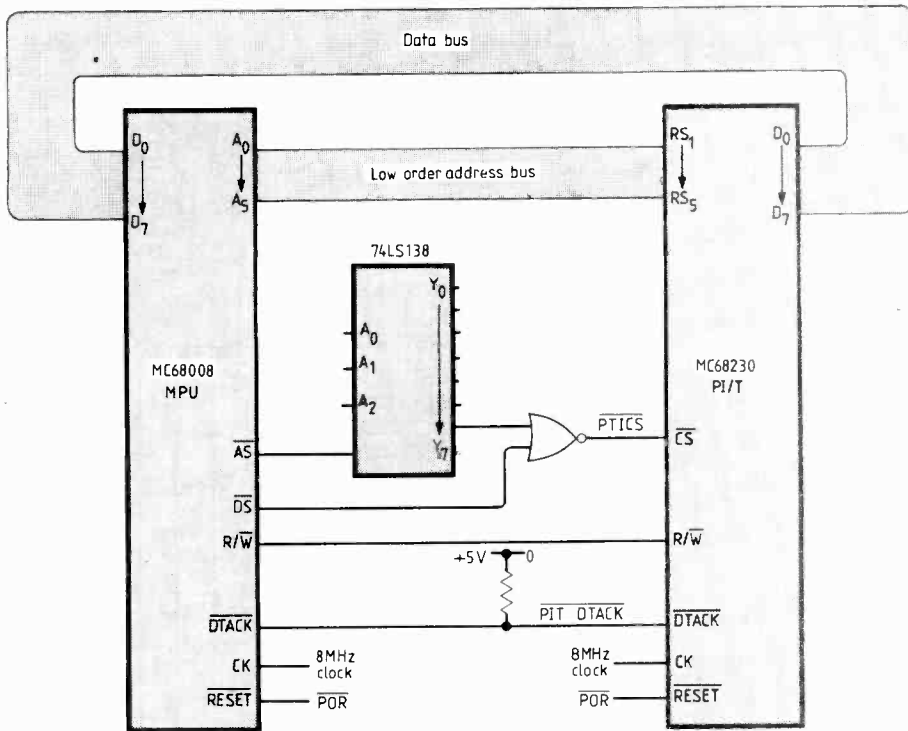


Fig. 6. 68008 with M68000 type peripherals have on-chip DTACK generators which provide the return handshake signal for the asynchronous data bus.

strobe (DS) are used to ensure the DTACK waveform is generated correctly for the three types of 68008 bus cycles — read, write and read-modify-write.

Refresh requirements for the MCM6664 drams are modest, which makes them ideal for a low-cost 68008-based system. The refresh row address counter is on-chip and refresh may be performed by providing a pulse on pin 1 (REF) to refresh the next row of memory elements. A dynamic ram refresh controller is shown in Fig. 5. The technique used is to temporarily suspend processing by requesting the 68008 bus. Eight successive rows within the drams are refreshed before allowing the 68008 to continue. Block refreshing in this way affects the longest possible interrupt la-

tency time, the time between an interrupt occurring and the mpu entering its interrupt handler. A block refresh of eight rows is acceptable for most applications.

The 68008 bus arbitration, controlled by bus request (BR) and grant (BG), is used to suspend processing. When BR is activated by external logic the 68008 makes BG active as soon as possible, usually directly after internal synchronization. Once BR is removed BG is deactivated and the 68008

Fig. 7. 68008 with non-M68000 type peripherals. Special m.p.u. control lines allow straight forward interfacing to these peripherals with minimal hardware. The m.p.u. performs a synchronous bus cycle when accessing such devices.

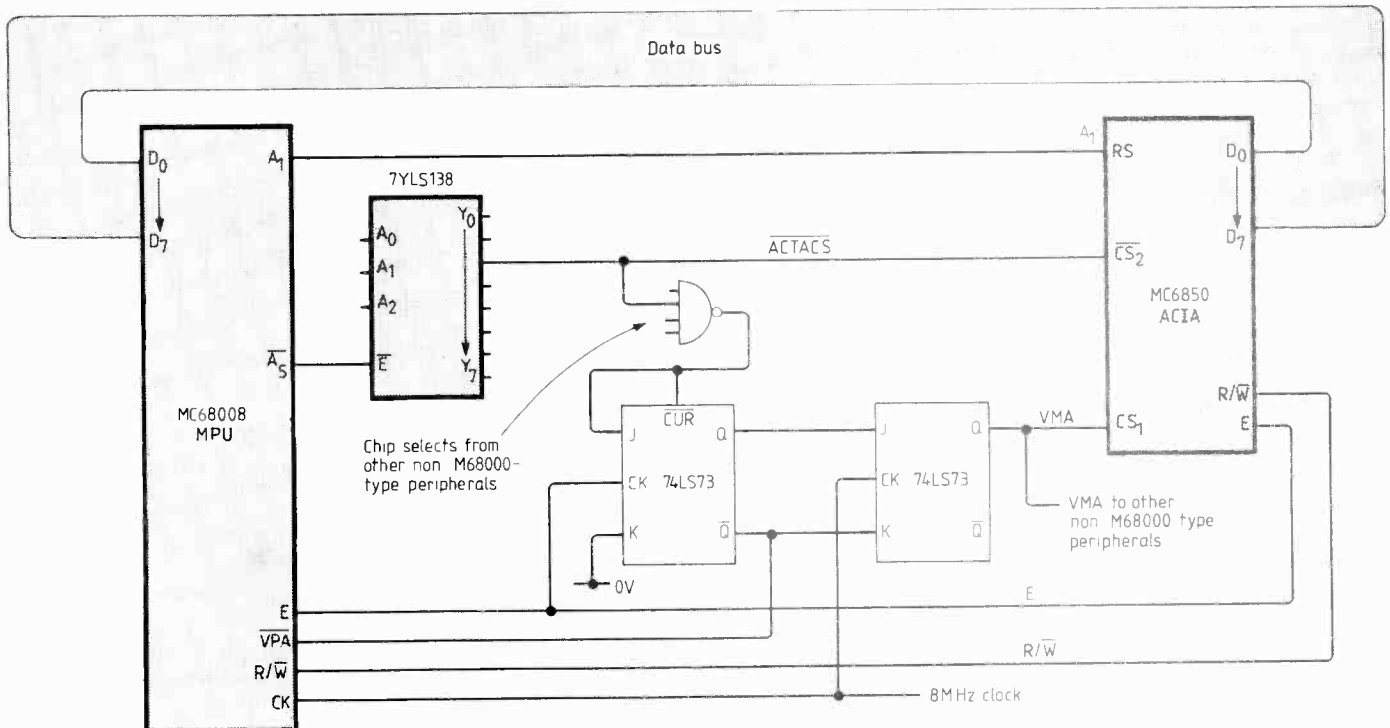
resumes processing. In Fig. 5 the multivibrator (1/2 MC3456) produces a clock REFCLK at the required refresh rate (about 9kHz). The rising edge of signal REFCLK triggers the first D-type flip-flop (1/2 74LS74) which generates the bus request to the 68008. When bus grant is received AS and DTACK must be monitored to determine the end of the current bus cycle.

This condition, detected by the four-input nand-gate, is clocked through the second D-type flip-flop. The Q<sub>2</sub> output goes high enabling a stream of negative-going pulses to appear on the REF inputs of the drams. And simultaneously, the 74LS161 counter is allowed to count. After eight refresh pulses have been generated the counter clears the first flip-flop. This in turn removes the bus request, and disables the REF pulses and stops the counter. The 68008 removes the bus grant and continues normal processing. This state continues until the next rising edge of REFCLK.

### 68008 with M68000-type peripheral

Many M68000 peripheral devices have 8-bit data buses and some may be configured for eight or 16-bit buses. In these cases the data bus lines D<sub>0</sub>-D<sub>7</sub> are connected on a one-to-one basis with the 68008 data bus. For the few peripherals with only 16-bit buses, a 16-bit interface can be constructed using two octal transceivers and a couple of gates.

Fig. 6 shows a typical interconnection between the 68008 and the 68230 parallel interface/timer (PI/T). The PI/T register select inputs (RS<sub>n</sub>) are controlled by the low-order address lines A<sub>1</sub>-A<sub>5</sub>. Note that address line A<sub>0</sub> is not used in this example. While it is quite acceptable to use A<sub>0</sub>, making it a "don't care" places the byte-sized internal registers of the PI/T on 16- rather than eight-bit boundaries in the memory map. This preserves complete software compatibility with programs



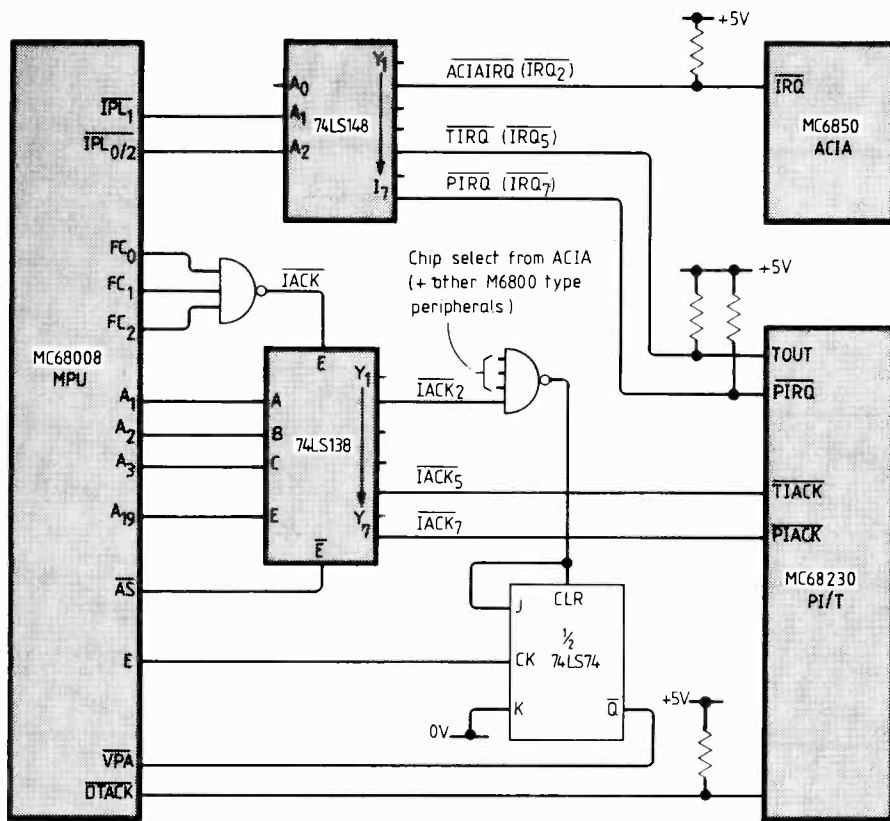


Fig. 8. 68008 interrupt interface logic. M68000-type peripheral (68230) uses the vectored interrupt scheme where it provides the vector number (0-255) on the data bus. Non-68000 type peripheral 6850 uses the auto-vector scheme.

written for the 68000 m.p.u. (which does not have an external  $A_0$  signal).

M68000-type peripherals have an on-chip DTACK generator so the DTACK pin is connected directly to the 68008 DTACK, and may be or-wired with the DTACK signal from other peripherals.

The interfacing of interrupt signals is described later.

### 68008 with non-M68000-type peripheral

Non-M68000-type peripherals do not have on-chip DTACK generators and are usually accessed synchronously using the M6800-peripheral signals enable (E) and valid peripheral address (VPA). Fig. 7 shows the interconnection of the 68008 with a 6850 a.c.i.a. Each time such a device is accessed during a m.p.u. bus cycle, the 68008 VPA input is used for the returning handshake instead of DTACK. VPA signals the 68008 to perform the current bus cycle synchronously. Data transfer is made on the falling edge of the E clock which the 68008 provides for the peripheral. A J-K flip-flop (1/2 74LS73) generates VPA whenever any M6800-type peripheral in the system, such as the a.c.i.a. is chip-selected. A second flip-flop provides a valid memory address (VMA) used by many of these devices.

### 68008 interrupt logic

Fig. 8 shows the interrupt connections for a typical small system. A M68000-type peripheral (68230 PI/T) uses interrupt priority level 7 for its parallel interface and level 5 for its timer. A M6800-type peripheral (6850 ACIA) uses level 2. The three

interrupt request signals (PIRQ, TIRQ and ACIAIRQ) are priority encoded by the 74LS148 priority encoder which generates a three-bit binary number corresponding to the interrupt level. Two bits of the three-bit number are presented to the 68008 via its interrupt priority level inputs IPL0/2pin to both the IPL0 and IPL2 inputs internally the 68008 encodes values of 0, 2, 5 and 7. Level zero is used to indicate that there is no interrupt depending and level seven is a non-maskable edge-triggered interrupt. Except for level seven, the requesting level must be greater than the level contained in the processor status register before the 68008 will acknowledge the request.

Interrupt acknowledgement (IACK) is indicated by the processor function code outputs  $FC_0$ ,  $FC_1$  and  $FC_2$  all logic high. The address lines  $A_1$ ,  $A_2$  and  $A_3$  contain a three-bit binary number corresponding to the interrupt priority level being acknowledged. In Fig. 8 a 74LS138 1-of-8 demultiplexer decodes the individual IACK for each peripheral device (IACK<sub>n</sub>). For M68000-type peripherals IACK<sub>n</sub> is connected to an input pin on the peripheral for this purpose (e.g. PIACK or TIACK on the 68230 PI/T). When this input is activated the peripheral places the vector number (binary 0-255) on the data bus and then it activates the DTACK signal. The 68008 reads the vector number and uses it to find the start address of the required

interrupt handler from its interrupt vector table. Non-M68000 peripherals, not capable of this vectored interrupt method, need hardware to provide the v.p.a. signal. Asserting VPA during IACK signals the m.p.u. to use one of the autovectors to find the appropriate interrupt handler. The NAND-gate J-K flip-flop used as VPA generator here is the same as that in Fig. 1

### Other circuit elements

No special multi-phase clocks are required by the 68008. An 8MHz t.t.l. clock generated from a crystal and several inverters is sufficient. A double-frequency master clock is useful for producing certain timings such as those for controlling dynamic memories. A watch-dog timer should be used in asynchronous microprocessor systems to detect attempts by software to access non-existent memory. It may be constructed in similar fashion to the DTACK generators shown but connected to the 68008 bus error input (BERR). Its time-out period should be longer than the slowest memory or peripheral device in the system. Power-on reset logic could comprise a 555 timer and several inverters.

### Microcomputers as 68008 peripherals

Low-cost single-chip microcomputers, like the MC6805 family, may readily be cus-

*continued on page 41*

### Motorola peripheral devices

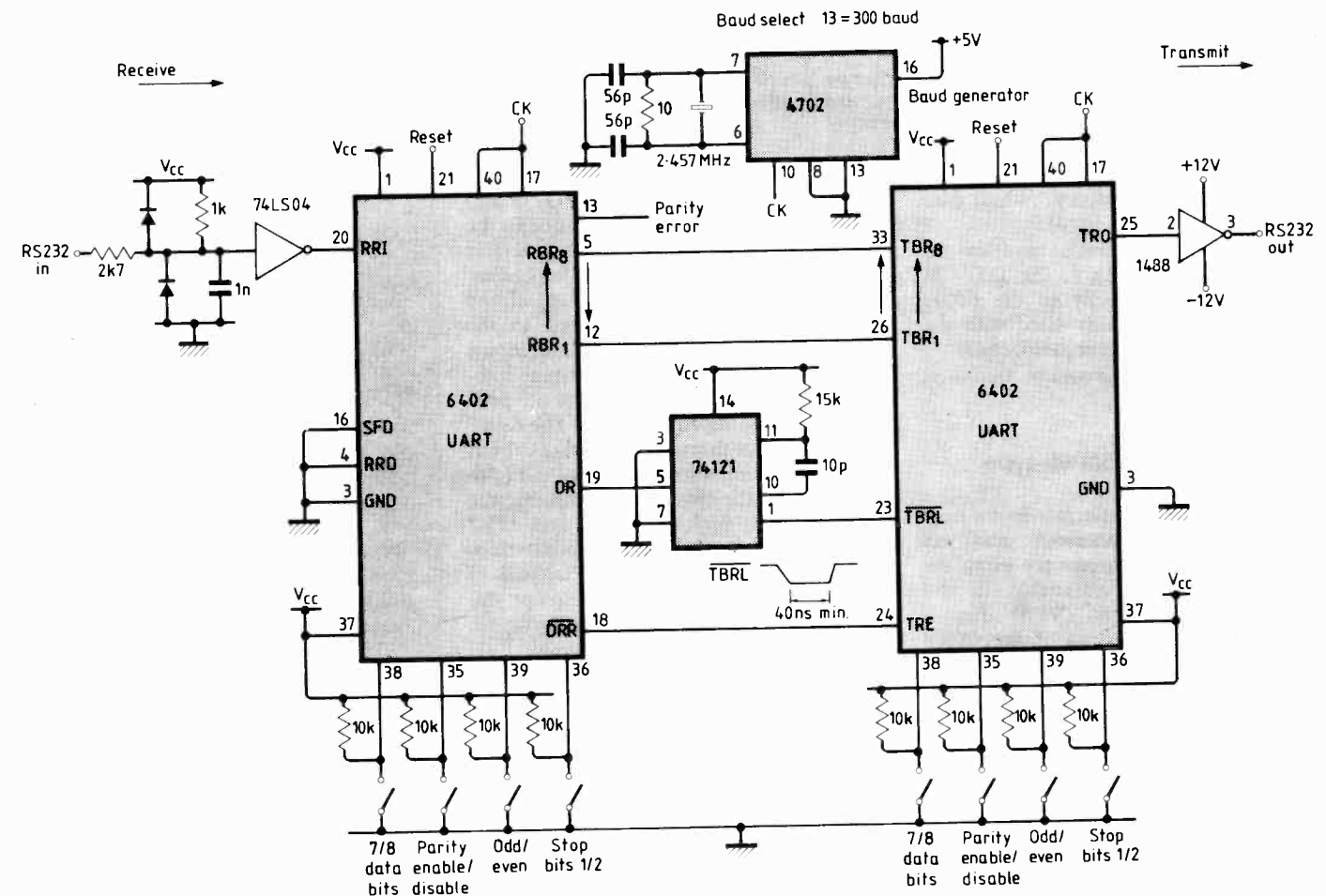
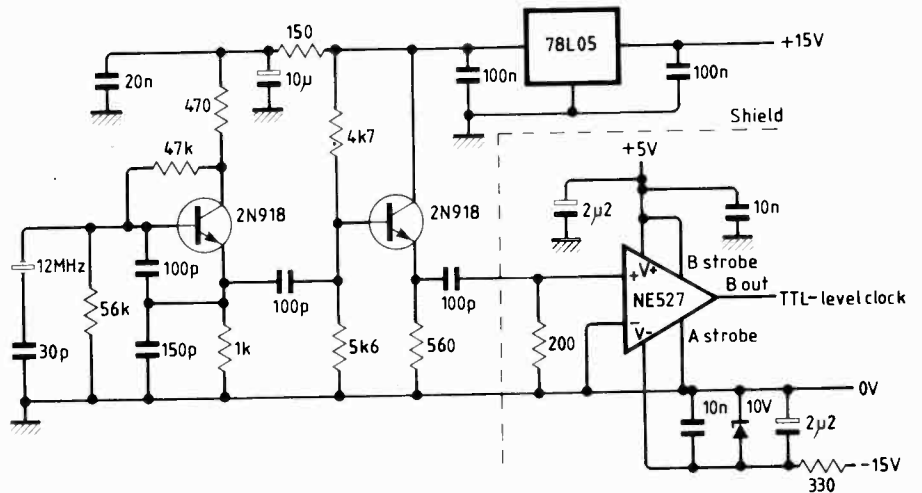
6821	PIA	Peripheral interface adapter
6822	IIA	Industrial interface adapter
6829	MMU	Memory management unit
6835	CRTC	Mask programmed c.r.t. controller
6840	PTM	Programmable timer module
6844	DMAC	Direct memory access controller
6845	CRTC	CRT controller
6847	VDG	Video display generator
6850	ACIA	Asynchronous communications interface adapter
6852	SSDA	Synchronous serial data adapter
6854	ADLC	Advanced data link controller
68120	IPC	Intelligent peripheral controller
68153	BIM	Bus interrupter module
68230	PIT	Parallel interface and timer
68440	DDMA	Dual direct memory access controller
68450	DMAC	Direct memory access controller
68451	MMU	Memory management unit
68452	BAM	Bus arbitration module
68454	IMDC	Intelligent multiple disc controller
68459	DPLL	Disc phase-locked loop
68488	GPIA	General-purpose interface adapter
68561	M P C	Multi-protocol communications controller II
68562	DUSC	Dual universal serial communications controller
68564	SIO	Serial input output
68590	LANCE	Local area network controller for Ethernet
68652	MPCC	Multi-protocol communications controller
68653	PGC	Polynomial generator and checker
68661	EPCI	Enhanced programmable communications interface
68681	DUART	Dual universal asynchronous receiver transmitter
68802	LNAT	Local area network controller
68901	MFP	Multi-function peripheral
14442	A to D	Microprocessor compatible a-to-d converter
146818	RTCC	Real time clock + ram

# CIRCUIT IDEAS

## Low-jitter crystal oscillator

While constructing digital audio equipment, a need arose for a very low noise 12MHz crystal oscillator with t.t.l. output. Designs using logic gates have too much jitter so I developed this circuit comprising a conventional crystal oscillator, buffer and t.t.l. comparator. The oscillator must be well shielded and its separately-stabilized power supply introduced via feed-through filters.

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Department of Music  
University of York



## Serial data-frame converter

My requirement was for converting eight-bit serial RS232 data into seven-bit data serial data. Input to the first uart is converted to t.t.l. level by a 7400 i.c. instead of the usual 1489 receiver to save money. I wanted a fixed data rate of 300 baud but simple switching on the 4702 generator inputs allows other data rates to be selected.

Serial data enters the uart on the left at input RRI; this uart is set for eight-bit serial data words. Parallel data passes from this uart to the second one under handshake control between the data-received output, DR, and transmitter-buffer register load input, TBRL, and between the data-received reset input, DRR, and transmitter-register empty output TRE. A 74121 monostable i.c. is included to com-

ply with timing requirements. The second uart is set for seven-bit serial data words and transmits through a 1488 driver at output TRO. Inclusion of switches allows data frames to be set to any combination and the circuit is easily modified for two-way communications.

Stephen Evans  
Cradley Heath  
West Midlands

## Reducing op-amp crossover distortion

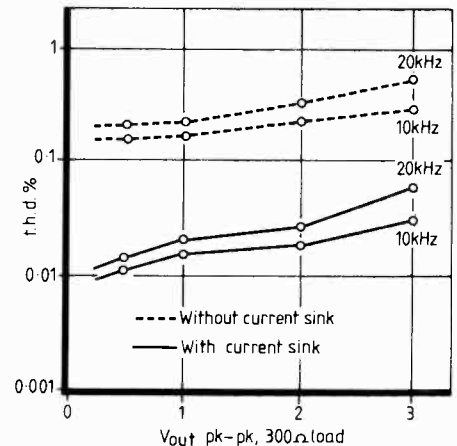
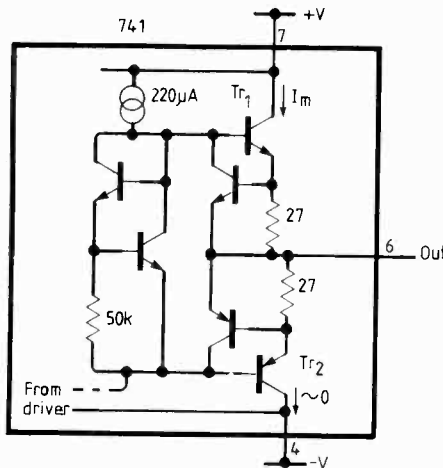
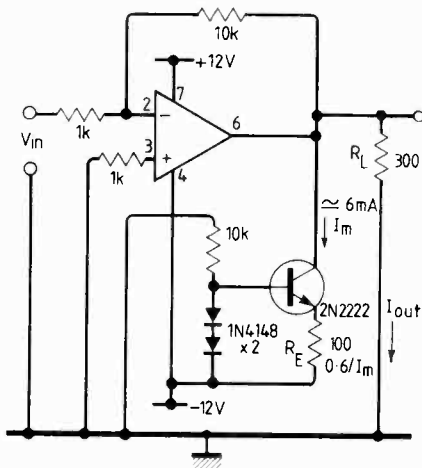
Crossover distortion in op-amp push-pull outputs operating in class AB mode worsens when driving low impedance loads at high frequencies. But fortunately the output can usually be forced to work in class A mode, as shown here where an op-amp connected as an inverter has an external current sink. Operating mode of the op-

amp is changed considerably. The n-p-n output transistor  $Tr_1$  is forced to carry a quiescent current equal to  $I_m$  while p-n-p transistor  $Tr_2$  is switched off as long as  $I_{out} \geq -I_m$ .

Bearing in mind that 741 output current is limited at about 16mA,  $Tr_1$  continuous current should be set so that maximum undistorted output swing  $I_m$  is less than 8mA. Advantages are absence of crossover distortion, reduction of other forms of

distortion due to higher operating current of  $Tr_1$  and increased phase margin of the whole amplifier since slow lateral p-n-p output transistor  $Tr_2$  is removed from the signal path. Disadvantages are an increase in quiescent current and reduced output swing. Distortion reduction using this technique ranges from 20 to 40dB.

Giovanni Stocchino  
Rome  
Italy



## Alternative biasing for valve amplifiers

In this configuration, i.e. voltage regulators allow accurate setting of quiescent current and maintain the setting for the life of the valve. Another important feature is the absence of d.c. in the transformer primary winding which minimizes core distortion. Regulator input current is

$$I_{in} = I_{out} + I_q = V_{out}/R_L + I_q$$

Quiescent current drawn by the regulator,

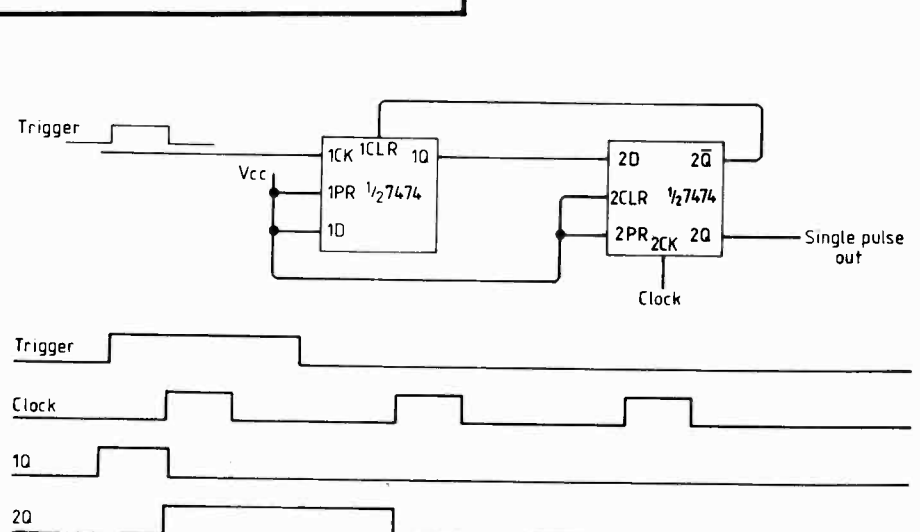
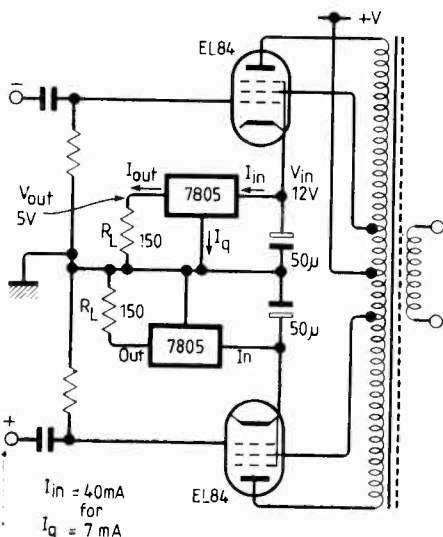
$I_q$ , is typically around 7mA for a 7805 regulator and varies by only between 1 and 1.5mA for a 20V input change. Cathode current is the same as the regulator input current and is solely determined by output voltage and load resistance, both of which are constant. Values shown are those used to convert my Leak Stereo 20 amplifier.

J. S. Spicer  
Melbourne  
Australia

## Precise single pulses

Referring to D. A. Haines' circuit in the November 1983 issue, precise single pulses equal in width to the clock period can be obtained using only two D-type bistable i.cs.

A. Dhurkadas  
Cochin  
India



# Assembly language programming

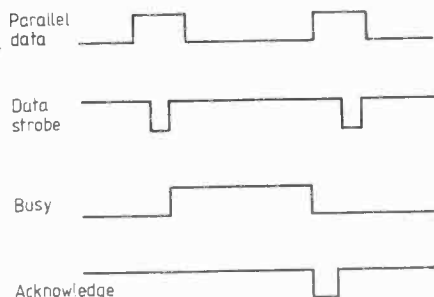
## Centronics-to-teletypewriter interface

*In this final assembly-language application, Picotutor's processor is turned into a low-cost interface for driving a teleprinter from a microcomputer. But you don't need to know anything about assembly-language to use this simple circuit.*

Bringing concepts introduced in previous articles together, this final application example is a larger project for driving a Creed teletypewriter from a Centronics parallel interface such as found on most microcomputers. Software for the interface was developed on the Picotutor assembly-language trainer. If you have a later version of this kit, software for the interface is already programmed in; those of you with earlier versions can have your processor reprogrammed for a small charge. For readers just interested in the interface hardware the preprogrammed processor may be obtained separately.

Teletypewriters — used by British Telecom for the Telex service — have been around for many years and have remained almost unchanged in design. Many find their way on to the amateur-radio surplus market and are widely used by amateurs for 'radio teletype,' often known as r.t.t.y. Being readily obtainable and cheap they represent an ideal low-cost printer for a home computer. A Creed 7E teletypewriter was used to design the prototype but other models should be just as easy to adapt. Printing is on 216mm-wide plain paper in roll form.

There are two main design problems when interfacing a teletypewriter to a microcomputer. For compatibility with



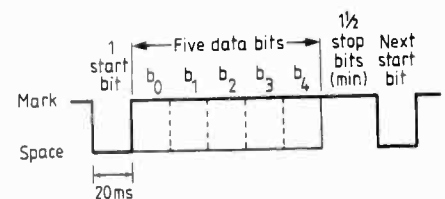
**Fig. 1.** Centronics interface timing diagram. Eight parallel data lines carry ASCII-coded signals from the computer under control of these signals. Data strobe, when low, tells the printer that there's a character on the data lines. Busy and acknowledging signals are sent to the computer by the printer to give 'handshaking'.

by R. F. Coates

signals transmitted over telephone lines, teletypewriters are designed for use with high-voltage drive signals. Secondly, serially-transmitted data used to control teletypewriters, called Baudot, is quite different from ASCII code sent in parallel form (i.e. more than one bit at once, in this case eight) through the Centronics interface. The first problem is a hardware one and easily solved by replacing the original drive circuit in the teletypewriter; both RS232 and t.t.l. levels are accepted by the circuit presented. The second problem is taken care of by the MC68705P3 single-chip microcomputer used in Picotutor.

### Printer interface

The Dragon Computer printer interface on which the prototype was based is a Centronics type, devised by printer manufacturer Centronics Data Computer Corp. It sends characters to the printer one at a time under control of 'handshake' signals. Timing for the data transfer is shown in Fig. 1. The computer first places the ASCII code for the character to be sent on the eight data lines. Only seven lines are required to select one of the 128 ASCII codes so the adaptor software ignores data-bit seven. The printer then receives a negative-going data strobe pulse from the computer to tell it that there is a character waiting for it on the data lines. Upon receiving this pulse the printer reads the character on the data lines and sends an 'acknowledge' pulse to the computer to indicate that the character has been read and that another character may be set up on the data lines. A 'busy' signal is also sent to the computer to stop it sending further characters while those already received are being printed; characters are normally printed a line at a time. When printing is finished, the 'busy' signal ceases and the computer is allowed to send



**Fig. 2.** Teletypewriter serial data is similar in form to that usually sent down RS232 links, and travels at 50 baud.

the next 'data-strobe' pulse if there is another character to be printed.

### Baudot code

Character code used by the teleprinter is in five-bit serial Baudot form. Only five bits means that there are only 32 possible combinations yet we need to send more than this. Letters of the alphabet and numbers 0-9 alone add up to 36 characters. Baudot code solves this by having two modes, letters (LTRS) and figures (FIGS). LTRS and FIGS are two unique codes which set the receiving teleprinter to the appropriate mode. With the exception of 'space,' 'carriage return' and 'line feed,' all other codes will print one of two different characters depending on the mode set, i.e., either a letter or a number/punctuation mark (see 'Nanocomp teleprinter interface,' P. C. Barton, October 1983 issue).

For instance, letter Q and figure 1 both have the same five-bit code — which one is printed depends on which 'mode' character was sent last. Data is sent serially down a single pair of lines and the format, shown in Fig. 2 is similar to the RS232 serial code. When no transmission is taking place, the signal line remains in the 'mark' state, which in the case of this modified teleprinter interface is zero volts. A character to be sent is preceded by a start bit, which puts the signal line into the 'space' state (+5V) for one data-bit period. Length of the data-bit period is determined by the data rate, which for a teleprinter is normally fixed at 50 baud (50 data-bits per second so one data-bit period is 20ms). The five data-bits are then sent and finally a stop signal which is the 'mark' state for at least one and a half bit periods.

## Converter

The adaptor is divided into two sections — the ASCII to Baudot parallel-to-serial converter and the teletypewriter t.t.l. driver interface. The converter consists of the Motorola MC68705P3, suitably programmed, and a few passive components. This section performs most of the work. Its job is to read ASCII characters from the computer, convert them to equivalent Baudot code, send out a LTRS or FIGS-mode code if necessary and send the character out serially at 50baud to the teleprinter; the hard work is all done in software.

## Converter software

Software flow is shown in Fig. 3 and the relevant part of the Picotutor-monitor in assembled form, see over. This program list was produced by the development system used to write the software for Picotutor. Such a list is produced when the source code is assembled by an assembler

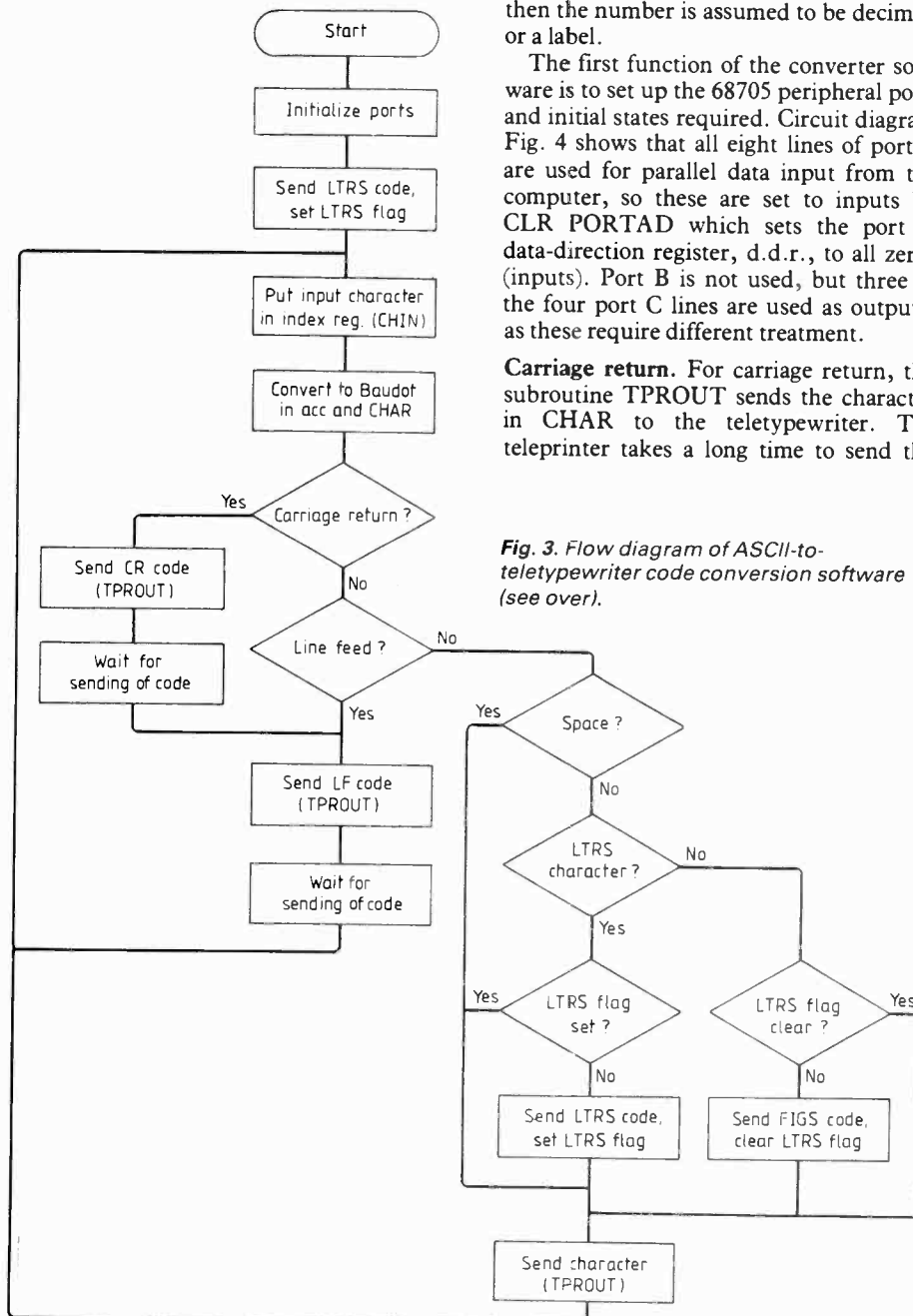


Fig. 3. Flow diagram of ASCII-to-teletypewriter code conversion software (see over).

program, to provide the object code for programming into the 68705 eeprom. The assembly-language source program, i.e. what is written by the programmer and typed into the development system, is below and to the right of the source-line page heading. Everything to the left of this is produced by the assembler. Column headings are

**LOC** — the hexadecimal address (location).

**OBJECT** — object code, the result of assembling.

**M** — not used with this type of program.

**STAT** — the statement number of each line. Comment lines begin with \* and are not allocated a statement number.

**E** — column holds an error code if there is an error in the line.

**LINE** — line number.

Note that hexadecimal numbers are preceded by an H and enclosed by single quotation marks in assembly language used with this development system. Similarly, binary numbers are preceded by a B; if there is no prefix or quotation marks then the number is assumed to be decimal, or a label.

The first function of the converter software is to set up the 68705 peripheral ports and initial states required. Circuit diagram Fig. 4 shows that all eight lines of port A are used for parallel data input from the computer, so these are set to inputs by CLR PORTAD which sets the port A data-direction register, d.d.r., to all zeros (inputs). Port B is not used, but three of the four port C lines are used as outputs. as these require different treatment.

**Carriage return.** For carriage return, the subroutine TPROUT sends the character in CHAR to the teletypewriter. The teletypewriter takes a long time to send the

heavy carriage from one end to the other, so a delay loop is introduced before going on to the next character. Also, when the Dragon sends a carriage return signal, it really means carriage return *and* line feed (or new-line) so after carriage return line feed is sent in a similar way. Note that with the BBC micro, whether carriage return with line feed or just carriage return is sent is determined by software. It should be configured to send just carriage return, which is the default setting.

**Line feed.** This is sent to the teleprinter as before but a further shorter delay is inserted. The program then branches back to get the next input character.

**Space.** This code is sent out and the program branches back to get the next input character.

If the code isn't one of these three then it's one which requires the teleprinter to be in the appropriate mode. Testing bit seven of the code indicates the mode required, and testing the LFLG, BITSTR bit flag indicates which mode the printer is in.

Bit manipulation instructions need the bit number within the byte and the byte address. Flag LFLG is equated earlier in the source file (not shown) to give the bit number, and similarly BITSTR is equated to a ram byte address. If the teleprinter is not in the correct mode, then the appropriate subroutine, LTRSET or FIGSET, is called to send the mode code and alter LFLG, BITSTR. The character code is then sent and the program then loops back to CHIN where the BUSY line is cleared, acknowledgement of receipt of the last character is sent, and the next character waited for.

Characters or mode codes are sent to the teletypewriter by calling subroutine TPROUT. This first sends the start bit by setting PC<sub>0</sub> high (serial-data out) for one data-bit period (20ms) by calling subroutine WAI50B which loads the accumulator with value eight and passes to subroutine WAIT which executes a 2.5ms-delay loop for the number of times indicated in the accumulator, and then returns from the subroutine. On return, the five data-bits are sent one at a time, bit zero first, by a loop which sets PC<sub>0</sub> according to the state of each bit of the data code in turn and Port C d.d.r. is set up by writing FF (all ones or outputs) to it. These three outputs also have to have an initial value; C-port line PC<sub>2</sub> is set to (+5) to indicate busy, PC<sub>1</sub> is set to one, the normal state for the acknowledge line and PC<sub>0</sub>, the serial data output, is set to zero. To ensure that the teletypewriter is in the LTRS mode, an LTRS code is sent and an LTRS flag in ram is set. Both of these functions are performed by the LTRSET subroutine.

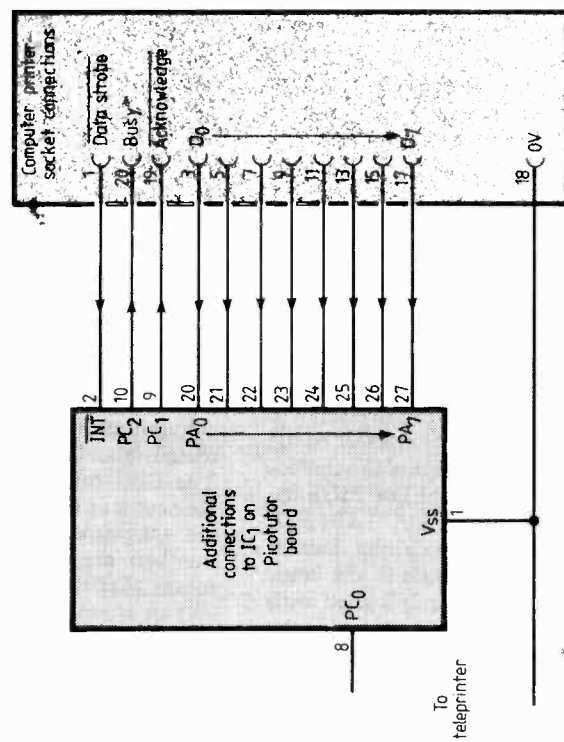
The main loop of the program is now entered, the BUSY signal is released and a pulse is sent to acknowledge receipt of the last character — if there was one. Next the program waits for a character to be sent by repeatedly testing the data-strobe line for a negative pulse. The data-strobe line from the computer is connected to the 68705 interrupt input, but the line is not used as an interrupt in this application. At power-

Software for the interface in assembly - language form

LOC	OBJECT	M	STAT	E LINE	SOURCE LINE
1127 *	DRAGON	-	TAKES STANDARD CENTRONICS TYPE ASCII INPUT AND CONVERTS TO BAUDOT CODE AND TRANSMITS AT 50 BAUD TO TELEPRINTER		
1128 *					
1129 *					
1130 *					
1131 *					
1132	OLY508	EQU	8	50 BAUD BIT PERIOD DELAY	
1133	OLYCR	EQU	100	CARRIAGE RETURN DELAY	
1134	OLYLF	EQU	20	LINE FEED DELAY	
1135 *					
1136	LTRS	EQU	0	BAUDOT LETTERS MODE CODE	
1137	F16S	EQU	4	BAUDOT FIGURES MODE CODE	
1138 *					
1139	ACK	EQU	1	ACKNOWLEDGE LINE (PC1)	
1140	BUSY	EQU	2	BUSY LINE (PC2)	
1141	OUT	EQU	0	OUTPUT LINE (PCD)	
1142 *					
1143	LFLAG	EQU	2	BIT FLAG IN BITSTR TO INDICATE MODE	
1144 *					
1145 *					
634	JF04	CLR		PORTAD	
635	A6FF	LDA	#H'FF'	SET UP PORTS	
636	B706	STA	PORTCD		
637	A606	LDA	#B'00000110'	INIT PORTC; BUSY, NOT ACK, MARK	
638	B702	STA	PORTC		
639	A07E	BSR	LTRSET	SET TELEPRINTER IN LTRS MODE	
640	A641	LDA	#65	SET CHARACTER COUNTER FOR FULL LINE	
641	B724	STA	COUNT		
642	2FFE	BH	CHIN1	WAIT FOR DATA STROBE LOW	
643	1502	BCLR	CHIN	BUSY, PORTC SET NOT BUSY	
644	1302	BCLR	ACK, PORTC	ACK, PORTC SEND ACKNOWLEDGE PULSE	
645	1202	BSET	ACK, PORTC	ACK, PORTC	
646	8E00	BH	CHIN1	WAIT FOR DATA STROBE LOW	
647	1402	LDX	PORTA	READ CHARACTER IN	
648	D6062D	BSET	BUSY, PORTC	SET BUSY	
649	8722	LDA	TABLE,X	GET BAUDOT EQUIVALENT OF ASCII CODE INTO A	
650	A117	STA	CHAR	AND SAVE FOR LATER	
651	2616	CMP	#H'17'	IS IT CR CODE?	
652	A037	BNE	TRYLEF	BRANCH IF NOT	
653	A684	BSR	TPROUT	CARRIAGE RETURN, SO SEND IT OUT	
654	A04E	LDA	OLYCR	BUT WAIT A WHILE TO ALLOW IT TO DO IT	
		BSR	WAIT		
1180 *					
655	000580	A641	LDA	#65	SET LINE COUNTER FOR FULL LINE
656	00058F	B724	STA	COUNT	
1183 *					
1184 *					
1185 *					
1186	0005C1	A610	LDA	#H'10'	NOW SEND A LF AS WELL
1187	0005C3	B722	STA	CHAR	
1188	0005C5	A029	BSR	TPROUT	SEND LINE FEED
1189	0005C7	A614	LDA	OLYLF	AND WAIT ALSO
1190	0005C9	A040	BSR	WAIT	
1191	0005CB	20D5	BRA	CHIN	AND GET NEXT CHARACTER
1192 *					
1193 *					
1194 *					
1195	0005CD	A110	CMP	#H'10'	BRANCH IF LINE FEED
1196	0005CF	27F4	BEG	LF	
1197 *					
1198 *					
1199 *					
1200	000501	A11B	CMP	#H'1B'	BRANCH IF SO AND SEND IT
1201	000503	2708	BEG	SEND	
1202 *					
1203 *					
1204 *					
1205 *					
667	000505	40	TSTA		TEST BIT 7 TO SEE WHICH MODE REQUIRED
668	000506	2A11	BPL	FIG50P	BRANCH IF BIT 7 NOT SET, FIGS MODE
669	000508	041002	BRSET	LFLAG,BITSTR,SEND	CHECK IF TELEPRINTER ALREADY IN LTRS MODE
670	000508	A03F	BSR	LTRSET	BRANCH IF SO, OTHERWISE SET IT IN LTRS MODE
671	000500	A011	BSR	TPROUT	SEND OUT THE CHARACTER IN 'CHAR'
672	00050F	3A24	DEC	COUNT	DECREMENT CHARACTER COUNT
673	0005E1	268F	BNE	CHIN	AND DO NEXT CHARACTER IF NOT FINISHED A LINE
674	0005E3	A617	LDA	#H'17'	FINISHED A LINE SO SEND CR/LF BEFORE CONTINUING
675	0005E5	B722	STA	CHAR	
676	0005E7	20CE	BRA	CR	
1219 *					
1220 *					
1221 *					
677	0005E9	0510F1	LFLAG,BITSTR,SEND	BRANCH & SEND IF ALREADY IN FIGS MODE	
678	0005EC	A028	BSR	FIGSET	IF NOT, SET MODE FIRST
679	0005EE	20ED	BRA	SEND	
1225 *					
1226 *					
1227 *					
1228 *					
1229 *					
680	0005F0	1002	TPROUT	BSET	OUT, PORTC SEND START PULSE
681	0005F2	A015	BSR	MAI508	
1232 *					
1233	0005F4	AED5	LDX	#5	SET COUNTER FOR NUMBER OF DATA BITS
1234 *					
683	0005F6	3422	LDR	CHAR	GET NEXT CODE BIT INTO CARRY
684	0005F8	1102	BCLR	OUT, PORTC	SET OUTPUT LOW
685	0005FA	2402	BCC	TPR2	
686	0005FC	1002	BSET	OUT, PORTC	ON THE OTHER HAND, SET HIGH IF THIS BIT IS
1237 *					



0005FE A009	687	1240	TPR2	BSR	WAI50B	WAIT FOR ONE 50 BAUD PERIOD	000645	1818181B
000600 5A	688	1241		DECC		DECREMENT COUNTER	1818181B	1818181B
000601 26F3	689	1242		BNE	TPR1	AND DO NEXT BIT UNLESS FINISHED ALL 5	00064D	18181A08
LOC OBJECT	M	STAT E	LINE	SOURCE	LINE		1812181A	1812181A
	1243	*					000655	1000820E
000603 1102	690	1244		BCLR	OUT,PORTC	FINISHED CHARACTER, SO SET O/P LOW FOR STOP	131C0302	131C0302
000605 A60C	691	1245		LDA	#DLV50B*3/2	PULSE WHICH IS 1.5 DATA BITS LONG	00065D	0908001E
000607 2002	692	1246		BRA	WAIT	BRANCH AND RTS	150FDA18	150FDA18
	1247	*					000665	19071111
	1248	*					18011806	18011806
000609 A608	693	1249		*WAI50B	- WAIT FOR 1 BIT PERIOD, 50 BAUD (20MS)		00066D	059C8691
	1250	*					969E9285	969E9285
	1251			WAI50B	LDA	#DLV50B	000675	88999490
	1252	*					80839387	80839387
	1253	*					00067D	8988959A
	1254	*					8F98818C	8F98818C
	1255	*					000685	828A8E1B
00060E 8723	694	1256		STA	DELAY	STORE DELAY MULTIPLE	1818181B	1818181B
000600 4F	695	1257		CLRA			00068D	189C8691
00060E 4A	696	1258		DECA			969E9285	969E9285
00060F 26F0	697	1259		BNE	WAIT1		000695	88999490
	1260	*					80839387	80839387
000611 JA23	698	1261		DEC	DELAY		00069D	8988959A
000613 26F9	699	1262		BNE	WAIT1		8F98818C	8F98818C
	1263	*					0006A5	828A8E1B
000615 81	700	1264		RTS			1818181B	1818181B
	1265	*						
	1266	*						
	1267	*						
	1268	*						
000616 151D	701	1269		FIGSET	BCLR	LFLAG,BITSTR		
000618 A604	702	1270		LDA	#FIGS			
00061A 2004	703	1271		BRA	LTRS1			
	1272	*						
	1273	*						
	1274	*						
	1275	*						
00061C 141D	704	1276		LTRSET	BSET	LFLAG,BITSTR		
00061E A600	705	1277		LDA	#LTRS			
	1278	*						
000620 BE22	706	1279		LTRS1	LDX	CHAR	SAVE ORIGINAL CHARACTER	
000622 BF1F	707	1280		STX	TEMPX			
000624 B722	708	1281		STA	CHAR	STORE LTRS/FIGS CODE		
000626 A0C8	709	1282		BSR	TPROUT	AND SEND IT		
000628 BE1F	710	1283		LDX	TEMPX	RECOVER ORIGINAL		
00062A BF22	711	1284		STX	CHAR			
00062C 81	712	1285		RTS				
	1286	*						
	1287	*						
1288	*							
1289	*							
1290	*							
1291	*							
00062D 1818181B	713	1288		TABLE	- ASCII TO BAUDOT CONVERSION TABLE			
18181814	714	1289			WHERE NO BAUDOT EQUIVALENT EXISTS, 'SPACE' IS SUBSTITUTED			
000635 18181018	715	1290		TABLE	DATA	'H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18'		
18171818	716	1291		TABLE	DATA	'H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18'		
00063D 1818181B	717	1292		TABLE	DATA	'H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18'		
18181818	718	1293		TABLE	DATA	'H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18','H'18'		



\* For BBC computer, PC<sub>2</sub> output (pin 10) is not connected

Fig. 4. Pictotutor can be connected to act as a Centronics-to-teletypewriter interface as shown, but an alternative is to use just the microprocessor as in Fig. 5.

up the interrupt mask bit (I) in the condition-code register is set and interrupts are ignored until this bit is cleared, which it isn't in this program. The state of the interrupt pin tested by using branch-if interrupt-low/high instructions. Instruction BIH CHIN1 branches back to itself until the data strobe goes low. On the low strobe, the program proceeds by reading the data character into the index register from port A and setting the BUSY line.

### ASCII-to-Baudot conversion

Converting ASCII to Baudot code is simple. The ASCII character set consists of 128 characters, represented by hexadecimal values of 00 to 7F. There is a 128-byte table in the program (TABLE) which contains a byte with the Baudot equivalent for each ASCII code. Five bits of each byte in the table represent the character (b<sub>0</sub>-b<sub>4</sub>) and bit seven indicates whether the character requires LTRS (b<sub>7</sub> high) or FIGS (b<sub>7</sub> low) mode. Instruction LDA TABLE,X loads the accumulator with the Baudot equivalent of the ASCII code in the index register. The accumulator is loaded with the contents of a memory location in the table. This address is an offset equal to the ASCII value in the index register added to the starting address of the table. For example, ASCII code for letter A is 41. This value is added to the address of TABLE, 62D, to give the address in the table of 66E which contains Baudot code for A, 9C. Bit 7, being high, indicates that LTRS mode is required. The Baudot code is also stored in ram register CHAR for later use. Tests are made on the code to see if it is a space, carriage return or line feed waits for one data-bit period. Finally a stop bit is sent which is a logical zero for one and a half bit periods, calculated by the assembler at LDA £DLY50B\*3/2. Label DLY50B is the one-bit period delay value required by subroutine WAIT and is determined early in the list by assembler directive DLY50B EQU 8. The rest of the operand field tells the assembler to multiply that value by three and divide by two.

### Converter construction

The teletypewriter software must be in the 68705 eprom. Recently distributed versions of Picotutor include this software but earlier versions will need reprogramming (note to follow). To find out which software release you have, examine memory location D9; if it holds 00 you don't have the teletypewriter software, if it contains 12 then you do.

The converter can either be constructed as a stand-alone unit or Picotutor can be used. Connection details for adapting a Picotutor are shown in Fig. 4, and those for a stand-alone unit in Fig. 5. Note that with both of these circuits, additional driver gates are not used on the 68705 outputs, but strictly speaking they should be. Inputs on a Centronics interface normally have 1kΩ pull-up resistors to +5V. This means that the driver must be capable of sinking at least 6mA, which is outside the specification for PC<sub>1</sub> and PC<sub>2</sub> outputs of the 68705. However, the BBC micro

uses 4.7kΩ pull-up resistors and the Dragon 10kΩ which it will drive satisfactorily. If you have a computer that requires drivers, Fig. 5(a) may be used. This simple circuit is easily constructed on Veroboard. Power to drive the 68705 can be taken from the Dragon through the interface cable. With other computers it may be necessary to provide a separate +5V supply.

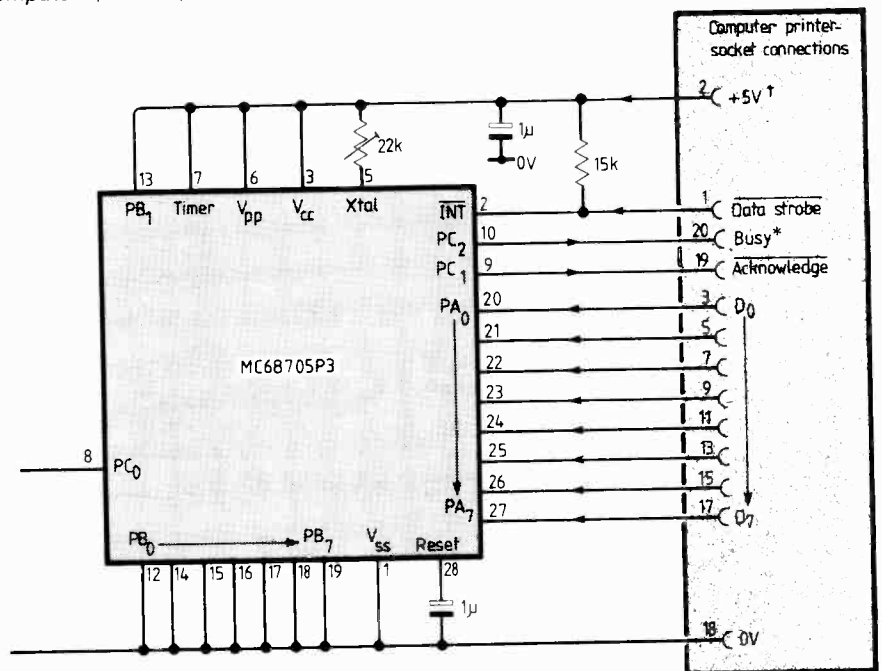
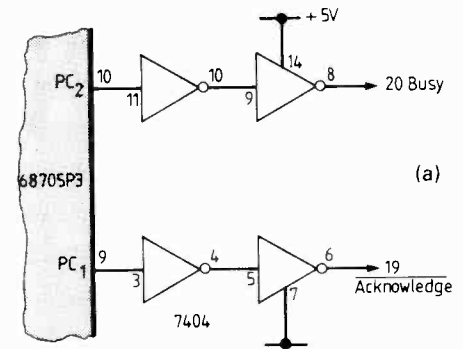
The printer interface connector used on the Dragon is not a standard Centronics one, presumably for reasons of cost, but is a 20-way ribbon cable insulation-displacement socket. Looking into the Dragon connector on the side pin 1 is at top right and numbers on the circuit diagram refer to the conductor number of the assembled socket and cable, counting conductors from pin 1. If the adaptor is to be used with another type of computer, the connections may need to be altered to suit (details should be given in the manual). The BBC microcomputer uses the same connector as the Dragon and pin numbers are the same except that all even pin numbers are connected to ground. This means that the BUSY signal is not used and an alternative 5V source of +5V will have come from inside the computer. Conductors at the other end of the ribbon cable are taken to the appropriate pin of the 68705 and unused conductors cut off. Insulate these well. The ribbon cable should be shorter than 30cm if buffers are not used. Output from the adaptor to the teletypewriter can be any twin flex; length here is not too critical.

Fig. 5. Excluding a small circuit for raising the signal driving the teletypewriter, this microprocessor used in Picotutor is the complete Centronics-to-teletypewriter interface. Buffers, shown separately, may be needed to feed the inputs of some computers (see text).

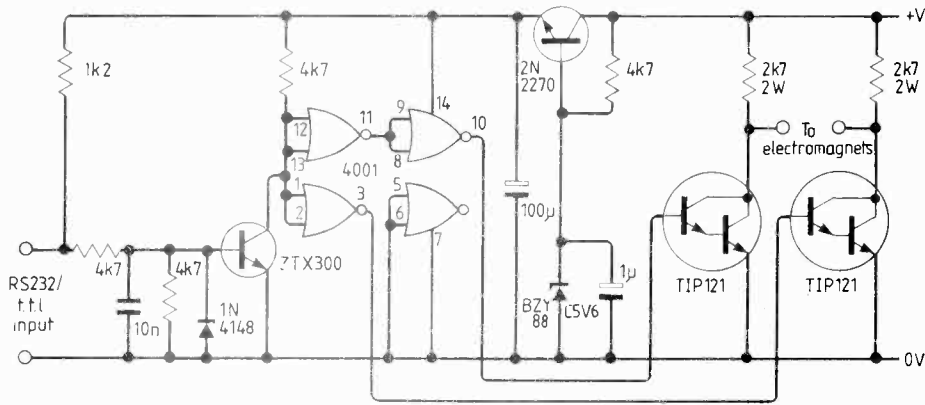
### Teletypewriter interface

To enable the teletypewriter to accept t.t.l. level signals sent by the converter, some minor modification is required. If your teletypewriter has a separate terminal unit and interconnecting cable, these are not required and can be discarded. The motor is driven from 240V a.c. mains. This input is taken to the input of the mains filter on the far left of the teletypewriter, underneath. The electromagnets are to be driven by the input from the adaptor and they move an actuating arm one way or the other depending on the state of the input signal. This movement is passed on through the mechanical print mechanism to decode the character and print it.

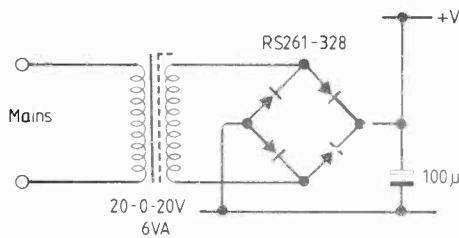
All original connections to the electromagnets should be removed and the circuit shown in Fig. 6 constructed and connected to them. The electromagnets are on the right-hand side of the unit, on top, but, the connecting block for them is underneath, directly below. It consists of four connectors as shown in Fig. 7. Original connections should be removed and the middle two connected together and the outer two taken to the interface circuit board. This board can be constructed on Veroboard from the circuit in Fig. 6 and can either be mounted in space underneath the teletypewriter or in a separate box. Which way round the electromagnet



\* For BBC computer, PC<sub>2</sub> output (pin 10) is not connected  
 † For Dragon computer only. For other computers, see text



**Fig. 6.** Teletypewriters weren't designed with computers in mind so this circuit is needed to raise the low-level signal for driving electromagnets.



connections are made is important, but is best found by trial and error as described later.

The circuit of Fig. 7 was designed to accept either RS232 or t.t.l. levels and so the first section converts the input to 0 and +5-volt levels. This then drives three logic gates which give complementary signals to drive the two Darlington transistors. One or other is on according to the input state thus sinking current through one of the 2.7kΩ resistors and coils, giving a reversal of current through the coils for a change of input state.

**Setting up**

The adaptor can now be connected to the computer and the teletypewriter interface.

**Centronics-to-teletypewriter interface**

Programmed microprocessors and kits of parts including p.c.b. and mains transformer are available from Magenta Electronics Ltd, 135 Hunter Street, Burton-on-Trent, Staffordshire DE14 2ST for £24.98 and £12.97 respectively, including vat. Case and hardware cost a further £3, and postage is 50p for each order.

For those who already have the Picotutor or any 68705s of their own and require the latest software release or wish to use a crystal instead of resistor oscillator, the 68705 can be re-programmed by the author for an inclusive cost of £2 by sending it to 57 Dalebrook Road, Burton-on-Trent, Staffs DE15 0AB. State whether a crystal or resistor clock is to be used.

The program for the teleprinter interface is included in the latest version of the Picotutor monitor (version 1.2) which also has some minor modifications to the monitor and the software for the teletypewriter interface and mini-organ (November 1983 issue). The mini-organ runs from address '0A4' or alternatively will run automatically at switch-on if PB<sub>1</sub> is tied to ground and PB<sub>0</sub> to +5V. This turns Picotutor into a stand-alone organ.

First check that the electromagnets have been connected up correctly. With everything connected up, switch on the computer and teletypewriter. If you are using Picotutor key in go 0A1 to run the program. The stand-alone version automatically runs the program at power-up. If the electromagnet connections are correct, the teletypewriter motor should run and nothing else happen, but if it clatters away seemingly trying to print something, but not actually doing so, then the two connections from the interface board to the electromagnets should be reversed.

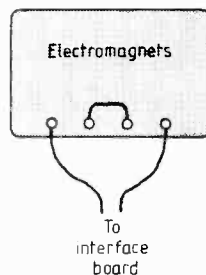
The printer is now ready for trying out, but the variable resistor on the adaptor may need adjusting before intelligible results can be obtained. This resistor sets the clock speed of the 68705. Data rate timing depends on this resistor. Using Picotutor, R<sub>17</sub> will need either to be replaced by a 22kΩ variable (or a selected fixed resistor). If you are using a crystal for timing (the eeprom has to be reprogrammed for this, see December 1983 issue) a crystal of 3.2768MHz should be used, which will give the correct data rate without adjustment.

Enter a line or two of text into the computer and then send this to the teletypewriter, using the LLIST command in the case of the Dragon. The teletypewriter should now attempt to print something. Adjust the variable resistor until the printing becomes intelligible; the setting is not critical.

**Conclusions**

One difficulty with this arrangement is that not all ASCII characters are available in Baudot. In most cases, a space is printed where there is no Baudot equivalent, with

**Fig. 7.** Electromagnet connections on the teleprinter. These may need to be changed in some cases (see text).



these exceptions.

By altering the table, any character can be made to print as you wish, so it is possible to alter this to suit your needs. I mentioned earlier that if you are using Picotutor you need to key in the program start address, but a stand-alone unit will run the printer adaptor at switch-on using PB<sub>0</sub>. When the 68705 is powered up, all peripheral pins are programmed as inputs. On Picotutor, all port B lines are pulled up to +5V by the 270Ω resistor network (see circuit diagram, December 1982 issue) but in Fig. 5 (stand-alone circuit) PB<sub>0</sub> is tied to ground. At switch-on, or when reset is pressed, the monitor program tests the PB<sub>0</sub> input. If it is one, it runs the monitor program, if it is zero, it jumps to the computer/teletypewriter adaptor program and runs that.

For those following the 'Assembly language programming' series, I hope that this description of a real application of the 6805 and the software listing will help to show some of the techniques of programming. When learning to program it is extremely useful to look at programs other people have written to get ideas and for this reason the complete source listing for the Picotutor monitor is available if required and is advised if full use of the facilities on the Picotutor is to be made. Unfortunately, because of its size (about 25 pages) it is not possible to publish it but copies may be purchased through Magenta Electronics (see box).



**Articles in this series**

- Picotutor**  
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January 1983, pp. 70-72
- Assembly language programming**  
March 1983, pp. 33-35  
April 1983, pp. 63-66  
May 1983, pp. 51-52  
June 1983, pp. 59-61  
August 1983, pp. 68-69  
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**Designing with 68008**

*continued from page 33*

tomized as intelligent peripherals having a 68008-type interface; the interface being emulated by m.c.u. software. Some of the m.c.u. i/o ports are used to provide the peripheral data bus D<sub>0</sub>-D<sub>7</sub>, chip-select (CS), read/write (R/W), DTACK, IACK, and register select (RS<sub>n</sub>) lines. Port lines programmed as inputs (CS, R/W and RS<sub>n</sub>) are monitored by the on-chip software to determine 68008 accesses. And with the port lines used for D<sub>0</sub>-D<sub>7</sub>, DIACK and IACK, the m.c.u. may be programmed by the 68008, and provide vectors during interrupt acknowledgement cycles. To the 68008 the m.c.u. behaves just like any other M68000 family peripheral.

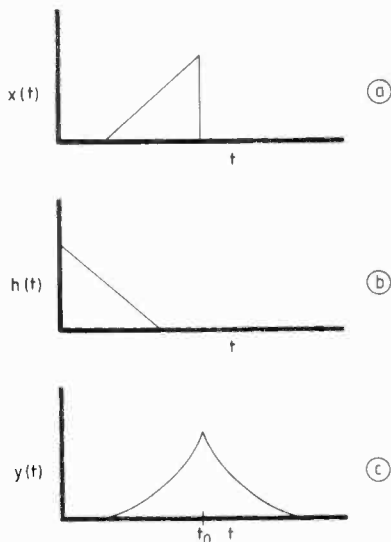


# Matched filters for radar and satellites

Surface wave, charge transfer and digital v.l.s.i. devices enable complex and powerful matched filters to be made. Geoffrey Robinson describes some examples that illustrate their different forms and uses.

A fundamental building block of radar and communication systems, the matched filter is used in radar receivers as the main signal processing circuit to detect weak echoes returned from a target, and in synchronization and detection circuits of digital communication systems. Matched filters have nothing to do with the concept of impedance matching between filters for maximum power transfer. They are, in fact, filters that are matched to a particular signal. They can be either entirely passive or active and range from the simplest two component capacitor-resistor low-pass filter to complete sub-systems of thousands of amplifiers, logic gates and associated circuits.

A filter is said to be matched to a signal if its impulse response is the time-reversed replica of that signal. The filter matched to the signal  $x(t)$  shown in Fig. 1(a) would therefore have an impulse response  $h(t)$  as shown in Fig. 1(b). Mathematically the



relationship between the two waveforms, which defines a matched filter, is

$$h(t) = kx(t_0 - t) \quad (1)$$

where  $k$  is an arbitrary constant and  $t_0$  is a fixed time delay. The transfer function  $H(\omega)$  of the matched filter is the Fourier transform of  $h(t)$

$$H(\omega) = kX^*(\omega)\exp(-j\omega t_0) \quad (2)$$

where  $X^*(\omega)$  is the complex conjugate of  $X(\omega)$ , the Fourier transform of  $x(t)$ . The frequency response  $|H(\omega)|$  of the

by G. N. Robinson B.Sc.



Since graduating from Salford University in 1975, Geoff Robinson has worked for Marconi Avionics on the AEW Nimrod project, and for Marconi Communication Systems where he is currently a principal engineer in the space and microwave division. During this time he has also spent three years at Leeds University working on an experimental spread spectrum system which will form the basis for a Ph.D thesis.

matched filter is therefore the same as the amplitude spectrum  $|X(\omega)|$  of the signal to which it is matched. The output of the filter,  $y(t)$ , is found by convolving  $x(t)$  with  $h(t)$

$$y(t) = \int_{-\infty}^{\infty} x(\tau)h(t-\tau)d\tau \quad (3)$$

From Fig. 1(c) the matched filter has caused considerable distortion of the input signal  $x(t)$ . This distortion is typical of all matched filters which in general produce a 'peaked' symmetrical output, similar to  $y(t)$ , when their matched signal is the input. Substituting equation 1 in equation 3 gives

$$y(t) = \int_{-\infty}^{\infty} x(\tau) \cdot kx(t_0 - t + \tau)d\tau \quad (4)$$

or

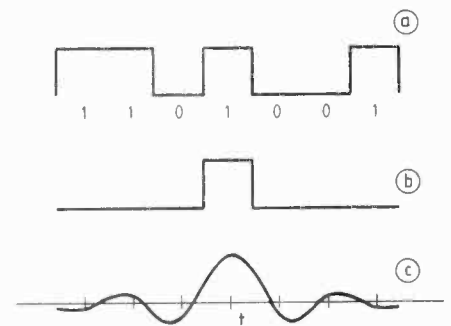
$$y(t) = R(t - t_0) \quad (5)$$

The output therefore is the autocorrelation function  $R(\tau)$  of the matched signal. This often serves as an alternative definition of a matched filter: i.e. one whose output sig-

nal is the autocorrelation function of its input signal.

The 'peaked' output obtained from a matched filter is exactly the type of response needed to detect the presence of a signal buried in noise. The matched filter is, in fact, the optimum device for detecting weak signals and it is therefore no surprise to learn that it forms the basis of many radar and digital communication receivers. In digital communications, matched filter considerations generally only arise when transmitter power is limited, such as in the case of satellite communication.

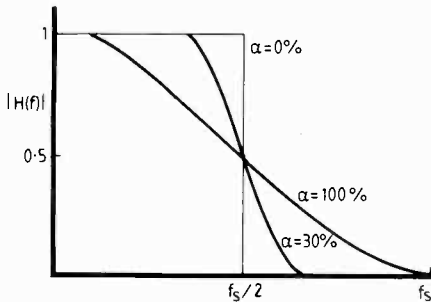
Before discussing the use of matched filters in satellite earth stations it is necessary to review some of the fundamentals of digital transmission. Digital information, whether computer generated or from some other source such as p.c.m.-encoded voice, is usually available prior to transmission in the form of an n.r.z. rectangular waveform, as shown in Fig. 2(a). To transmit



such a waveform without distortion would require an infinite bandwidth in theory. The waveform can be considered to be made up of the sum of individual pulses as in (b) which are confined to a time interval  $t$  seconds. If the n.r.z. waveform is filtered to limit the bandwidth, the effect on the individual pulses is to stretch them so that they are no longer entirely contained in their original time slot.

The effect of one particular low-pass filter is shown in Fig. 2(c). If the filtered n.r.z. signal is sampled at the points shown the tails of the individual pulses will affect the sample values in the nearby time slots. This effect, known as intersymbol interference (i.s.i.) can be avoided if the filtering is performed in accordance with Nyquist's vestigial symmetry theorem. This theorem, put forward by Nyquist as long ago as

1928, states that the zero crossings of the waveform in (c) occur at the sampling instants (giving no intersymbol interference) if the filter is either an ideal 'brick-wall' low-pass filter or an ideal 'brick-wall' low-pass filter with a transition band modified to give odd symmetry about the cut-off frequency. The theorem also requires the original n.r.z. waveform to be converted into a sequence of impulses so that the spectrum at the input of the filter is flat over the filter bandwidth. A class of widely used filters which satisfy this theorem are the raised-cosine filters. The amplitude response of the raised-cosine filter with various values of excess bandwidth or roll-off factor  $\alpha$  are shown below. A linear

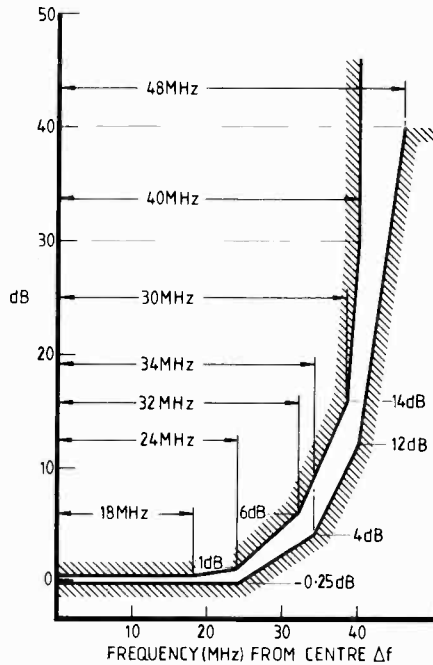


phase characteristic up to the zero transmission frequency is also required. In any bandwidth-efficient data transmission system with no intersymbol interference, overall channel filtering should therefore be as shown or equivalent to it for an r.f. modulation system.

### Satellite data transmission

Although the overall channel response for interference-free data transmission has been specified, the apportioning of this response between the various transmitter and receiver filters is a complicated problem. It is true, however, that if the transmission medium is linear between the transmitter and the receiver then the optimum split of the overall response is an equal division of the filtering between the transmitter and the receiver. The frequency response of the identical transmitter and receiver filters is therefore the square root of the response shown. This filter, known as a root cosine roll-off filter, is therefore only 3dB down at half the signalling frequency as opposed to 6dB in the diagram.

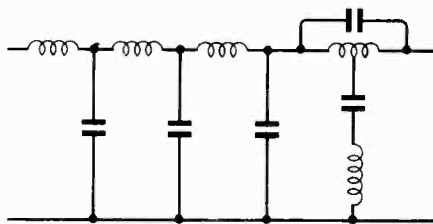
The equal division of the overall Nyquist response results in a matched filter at the receiver. This then simultaneously combats both intersymbol interference and the effects of noise. Although most satellite channels are non-linear due to the operation of transmitter high power amplifiers at or near saturation, the matched filter concept is still used in many earth station designs. A number of major satellite operators have specified this type of system including Intelsat who have made root 40% cosine roll-off filtering mandatory for their 120Mbit/s t.d.m.a. traffic service through the Intelsat V satellites. The earth station receiver filter mask specified by Intelsat is illustrated next, being nominally a root 40% cosine roll-off filter.



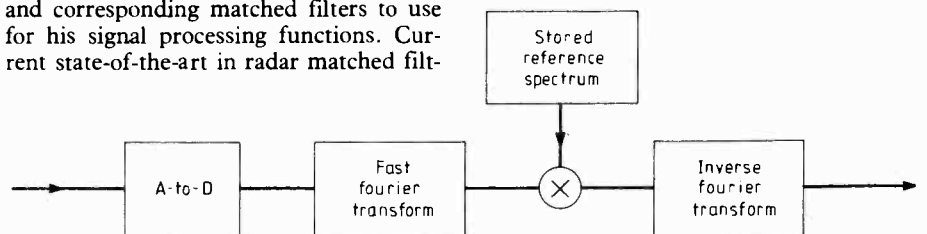
The actual filters used to realise these responses are generally based on standard filters such as Butterworth, Chebyshev or elliptical filters. The filter shown below consisting of a sixth-order Butterworth filter followed by a stage of delay equalization realises a root 100% cosine roll-off low-pass filter.

### Radar

Most radar receivers use matched filtering, although prior to about 1960 this was relatively trivial and merely involved the optimizing of conventional i.f. bandwidths. The usefulness of a matched filter, from a radar designer's viewpoint, is directly proportional to the time-bandwidth product of the filter, obtained by multiplying signal duration by filter bandwidth. Unfortunately the complexity of a matched filter is also proportional to its time-bandwidth product. The type of matched filters previously discussed in relation to digital communication generally have time-bandwidth products of the order of unity and are consequently not considered to be complex. In radar, however, the designer



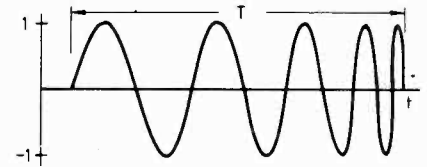
is not restricted by considerations of intersymbol interference and as a result has virtually an infinite variety of waveforms and corresponding matched filters to use for his signal processing functions. Current state-of-the-art in radar matched filter



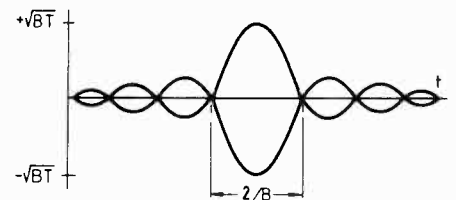
ers provides a time-bandwidth product in the range 10,000 to 100,000.

The main motivation behind the early matched filter development which led to the invention of the pulse compression radar was the need to obtain good range resolution with limited peak powers. Long range detection requires a large pulse energy which with a conventional power-limited radar means increasing the pulse duration. This causes a direct reduction in range resolution and accuracy. If instead of increasing the pulse duration the pulse bandwidth is increased, an improvement in range resolution in proportion to the time-bandwidth product is obtained.

The most well-known pulse compression technique uses the frequency chirp waveform shown next together with its dispersive delay-line matched filter. The



matched filter output, which is the compressed pulse, is shown below. The sin x/x-shaped pulse has a peak which is  $\sqrt{BT}$  times larger than the original chirp signal amplitude. Dispersive delay lines, that is



delay lines with a delay proportional to frequency, are today generally fabricated using acoustic surface wave technology and a wide variety are currently available 'off the shelf'.

The more complex matched-filter receivers which have also to satisfy the additional requirement of being able to process many different waveforms often resort to digital techniques. Bottom diag. is a flexible arrangement which performs matched filtering by multiplication in the frequency domain, rather than by convolution in the time domain, as in the previous filters discussed. In this method the signal is first sampled at a very fast rate, anything up to 200MHz, and then passed through an a-to-d converter. Blocks of digitized samples are then converted into corresponding blocks of frequency samples by a fast Fourier transform circuit. Then next these samples are multiplied by stored coefficients which represent the conjugate spectrum of the signal. Finally the transform circuit is re-configured to perform an inverse transform on the samples. WW

# Testing microprocessor-based systems at home

Though the design of microprocessor systems is not particularly difficult, testing is not so simple for the first-time builder without access to logic analysers or emulators. Here are some simple procedures that highlight hardware and software problems.

The design of simple microprocessor systems is not a particularly difficult task. Provided that one adheres to the correct loading rules for both current and capacitance, the design can be as easy as putting toy building bricks together. However, testing that the system — hardware or software — works is not so simple for the amateur or first-time builder who does not have access to logic analysers or plug-in microprocessor emulators. This article identifies some simple procedures to highlight both hardware and simple software problems. The discussion is based around the 8085 microprocessor but applies to virtually any microprocessor having a ready input.

Developed in the mid-seventies by Intel, the 8085 is an update for the 8080 chip set. Because the device has only 40 pins, Intel multiplexed the lower eight address bits with the eight data bits on lines designated AD<sub>0-7</sub>, Fig. 1. Figure 2 shows typical timing for the 8085 during a memory read and illustrates how AD<sub>0-7</sub> are multiplexed. The 8085 produces a clock output that is half the frequency of the source at X<sub>1</sub> and X<sub>2</sub>; the timings of all the other signals

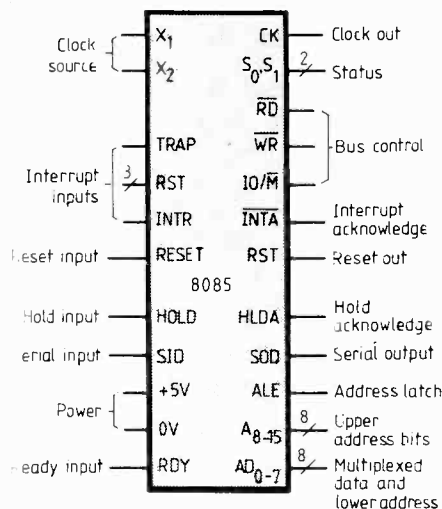


Fig. 1. Pin-out of the 8085 indicates the difficulty in using only 40 pins.

by Colin Carson

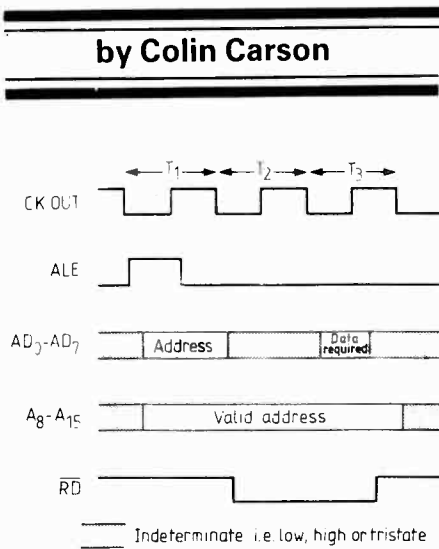


Fig. 2. Bus AD<sub>0-7</sub> is multiplexed between address and data by ALE.

produced by the microprocessor are related to its edges.

Shortly after the start of T<sub>1</sub>, the lower eight bits of the memory address appear on lines AD<sub>0-7</sub> and are guaranteed to be stable before the negative edge of ALE, generally used to latch the address into an eight-bit buffer such as a 74LS373 (see Fig. 3). As

this is a transparent buffer, the address will be passed through the buffer whenever ALE is high, and latched on the negative edge. The address is stable some time before the latching and the use of a transparent latch ensures that the address is available early in the read cycle, so that it can be used by other circuitry such as chip select logic. This is a great advantage when using fast microprocessors.

Around the start of T<sub>2</sub>, the memory address bits are removed and AD<sub>0-7</sub> goes tristate, waiting for data to be read in during T<sub>3</sub>.

Figure 3 shows how this might be achieved in hardware terms. Some designers add an additional latch on the upper eight address lines, which can glitch when certain instructions are executed.

During a write cycle the multiplexing of AD<sub>0-7</sub> follows in a similar fashion, address being valid before the trailing edge of ALE and valid data long before the rising edge of WR.

## Ready

The 8085 has a ready pin which can be used to extend the length of read or write cycles to compensate for slow peripheral chips or to handle devices not always available such as dual-ported memory. Figure 4 shows how the ready pin is sampled by the

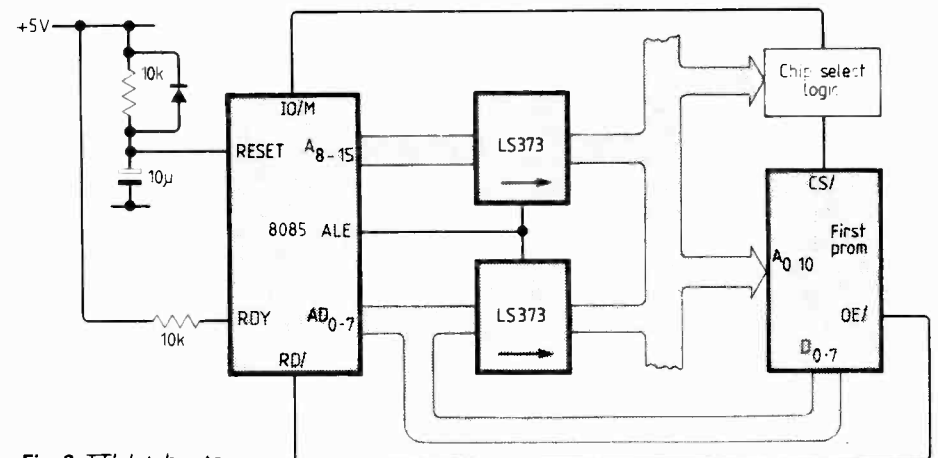


Fig. 3. TTL latches to demultiplex the address from the bus.

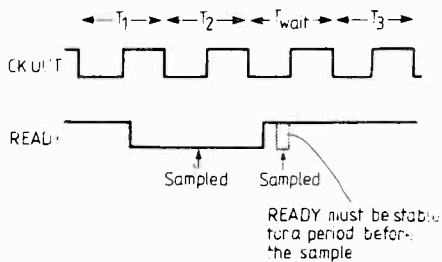


Fig. 4. READY is sampled during T<sub>2</sub> and any successive wait states.

8085 in the middle of T<sub>2</sub>, although it must be stable for a period before the sampling, the set-up time. If ready is low when sampled then on completing the T<sub>2</sub> cycle, the 8085 produces another T<sub>2</sub> cycle rather than going on to T<sub>3</sub>. This will repeat until the ready pin is sampled high.

The test procedures mentioned here make use of the ready pin, and the fact that signals such as  $\overline{RD}$ ,  $\overline{WR}$  and AD<sub>0-7</sub> remain unchanged during the not ready period.

### Reset

After the 8085 is reset, it reads the contents of the memory location whose address is 0000. It then continues to read from consecutive locations, decoding and executing them until instructed to jump to a different address. However if the ready pin is forced low before the 8085 is reset the microprocessor sits doing repetitive T<sub>2</sub> cycles with the address 0000 at the outputs of the latches,  $\overline{RD}$  low and waiting for valid data. This valid data should be the contents of the first location in prom and will invariably be the first byte of the three byte instruction LXI SP which sets-up the internal stack pointer.

### First test procedure

1. Check that the Hold input is not being driven high. Hold will force many of the 8085 outputs tristate.
2. Pull the ready input low, taking care not to damage any chips driving this pin. If necessary remove the 8085 from its socket and bend the ready pin so that it does not make contact on re-insertion. Then using a crocodile clip and lead ground the ready pin.
3. Reset the 8085.
4. Using a logic probe or oscilloscope, check the address lines are all low.

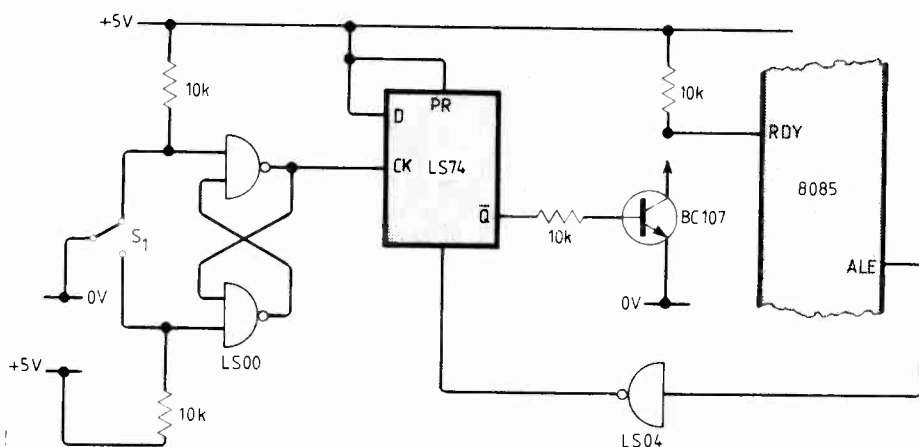


Fig. 5. The 8085 can easily be single-stepped by using t.t.l.

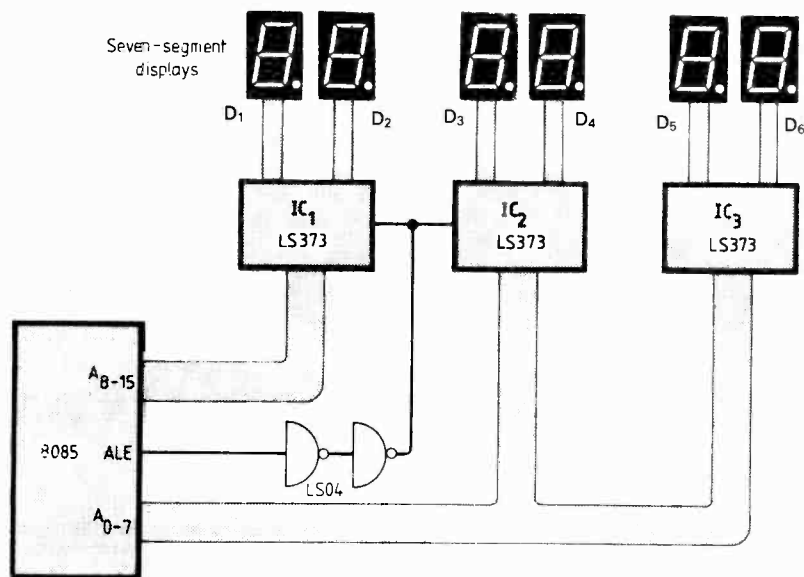


Fig. 6. Provided there is adequate bus during capability, seven-segment displays can be used to follow address and data.

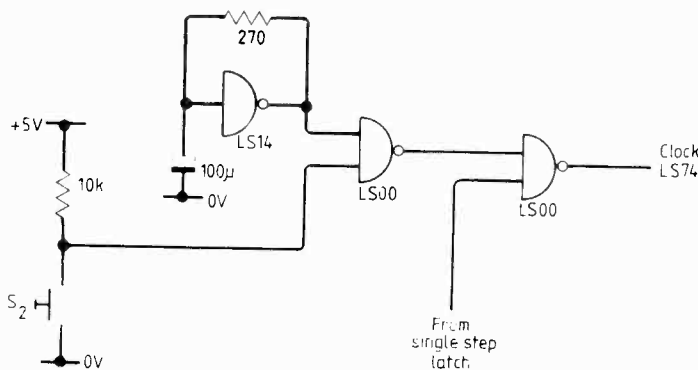


Fig. 7. Multiple step function can easily be incorporated, as shown.

5. Check the address pins on the prom are all low.
6. Check the chip select logic is driving the chip select pin on the prom low.
7. Check that  $\overline{RD}$  is driving the output enable on the prom low.
8. Check the correct eight bit data for location 0000 is present on AD<sub>0-7</sub>.

By following this step-by-step procedure simple hardware faults can be highlighted but because all the address lines are low, this will not show up shorts between them. To further exercise the hardware and trace simple software faults a single step facility is required, such as that in Fig. 5.

### Single step

The next stage is to step the microprocessor through instructions, monitoring the data and address buses until something unexpected happens. When the circuit is on, the flip flop and hence ready can be either low or high. After the power-on reset, the 8085 produces an ALE to latch the lower address byte 00. Signal ALE is inverted by G<sub>3</sub> clearing the flip flop and ready goes low. This condition will continue until the push switch S<sub>1</sub> is depressed, which after debouncing by G<sub>1</sub> and G<sub>2</sub>, clocks a high through the flip flop. Ready goes high and the 8085 completes reading the first instruction and issues the address for the next byte. Once again the flip flop is cleared and the microprocessor waits for S<sub>1</sub>. In this fashion S<sub>1</sub> can be used to single step the 8085 through each byte of each instruction. Take care to ensure that G<sub>3</sub> does not overload the ALE line, which can drive a maximum of five normal LS t.t.l. loads.

Using this circuit the microprocessor can be stepped through its program in prom until something goes wrong. Often it will only take a few instructions to highlight shorted address or data lines, although the tester will obviously need to be able to spot certain 8085 op-codes such as jumps, calls, interrupts and returns. The beginner to the 8085 should learn a lot

continued on page 49

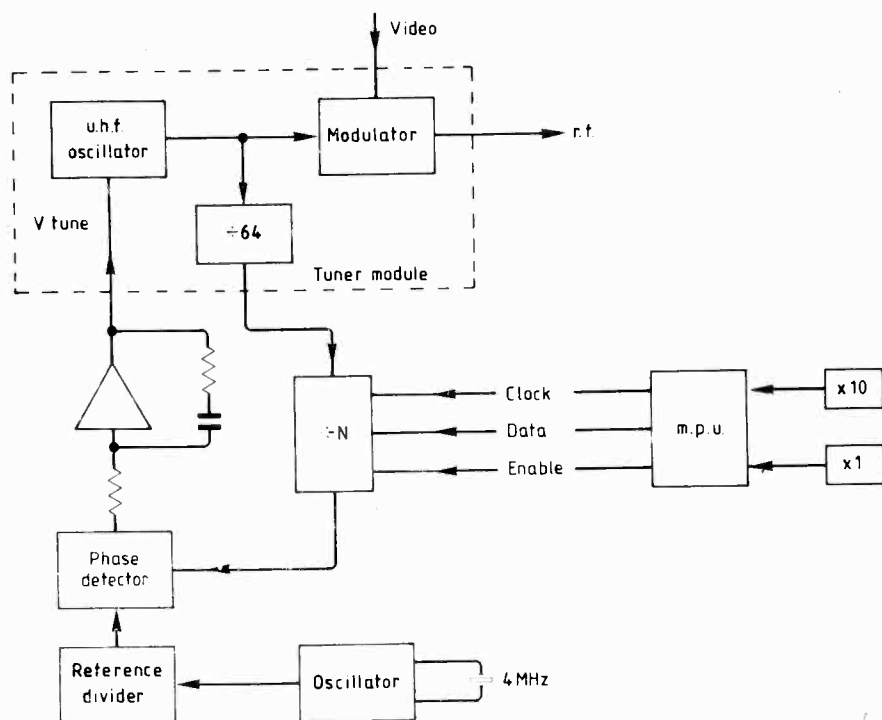
# Synthesized television modulator

As well as providing 5.5 and 6MHz sound, this modulator can be accurately switched to any desired u.h.f. channel

There are a variety of television modulators currently available for inclusion into video games, pattern generators etc. Such modulators have a tuning characteristic with a very wide tolerance, and a long-term and thermal frequency stability that leaves a lot to be desired. These problems are being highlighted by the introduction of frequency synthesis to domestic television receivers. These precision tuning systems still require provision for fine tuning and a.f.c. It seemed obvious to us that frequency synthesis should also be applied to the television modulator, and this article describes such a design.

The objective then was to provide a television signal at r.f. whose frequency could be adjusted with confidence to any one of the recognized u.h.f. television channels. Frequency synthesis would be used, the channel being loaded by thumbwheel switches, and the whole system being under the control of a microprocessor. The diagram of Fig. 1

Fig. 1. Block diagram of complete tv synthesizer.



by R. Wilkins & L. Cergel

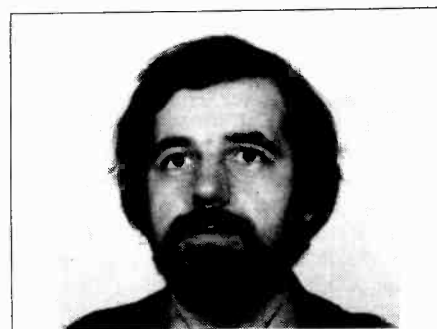
shows a basic phase-locked loop whose programmable divider ratio is supplied from the microprocessor.

## Microprocessor

The MC6805-P2 m.p.u. is an eight-bit microprocessor with a built-in software capacity of 1Kbyte of rom, 64 bytes of ram, and twenty t.t.l./c.mos-compatible bidirectional input/output lines. Eight of the lines are l.e.d.-compatible. The microprocessor is designed for low-cost high-volume applications; normally the makers of the device would produce a rom pattern from the customers software, and manufacture at least several thousand parts. For the one-off however, there is an eprom version that can be loaded with software and if necessary erased and loaded again many times over and the MC68705-P3 version was chosen for this application. Its task is to take in the channel number from the two b.c.d.

thumbwheel switches, do the necessary calculations and send the division ratio to the programmable divider. However, as the information sent to the programmable divider is latched into the divider the microprocessor unit need only send the information when it needs changing. This has the advantage of keeping radiation from the microprocessor to a minimum, which is essential in r.f. applications.

As the microprocessor is only checking the thumbwheel switches most of the time, it can be given additional work to do. Firstly, if the requested channel is less than 21, the microprocessor presumes that the user has made a mistake, lights a lamp and sends the data for channel 21 to the programmable divider. Similarly, if a channel greater than 68 is requested, the light comes on again and channel 68 is sent. Secondly, as sound may well be required as well as vision, the micro-



Roger Wilkins' schoolboy interest in radio was complemented by an HND from Kingston Polytechnic and led him into a career in consumer electronics. For the last 15 years he's been involved in the design of colour television receivers in London, Bradford, Geneva and now Gosport. His previous job was as an applications engineer with Motorola in Geneva, which is where this project was completed. Working now for Thorn EMI Ferguson on chroma and video circuits, his original interest in radio is still alive, with emphasis on receivers and amateur radio.

Lubomir Cergel, born and educated in Czechoslovakia, now lives in Geneva. Well qualified academically, his early career was in pure research, firstly at the Czechoslovak Academy of Science and later as a visiting scientist at CERN. He then worked for Motorola in Geneva on c-mos and e.c.l., and now specializes in eight-bit c-mos microprocessors.



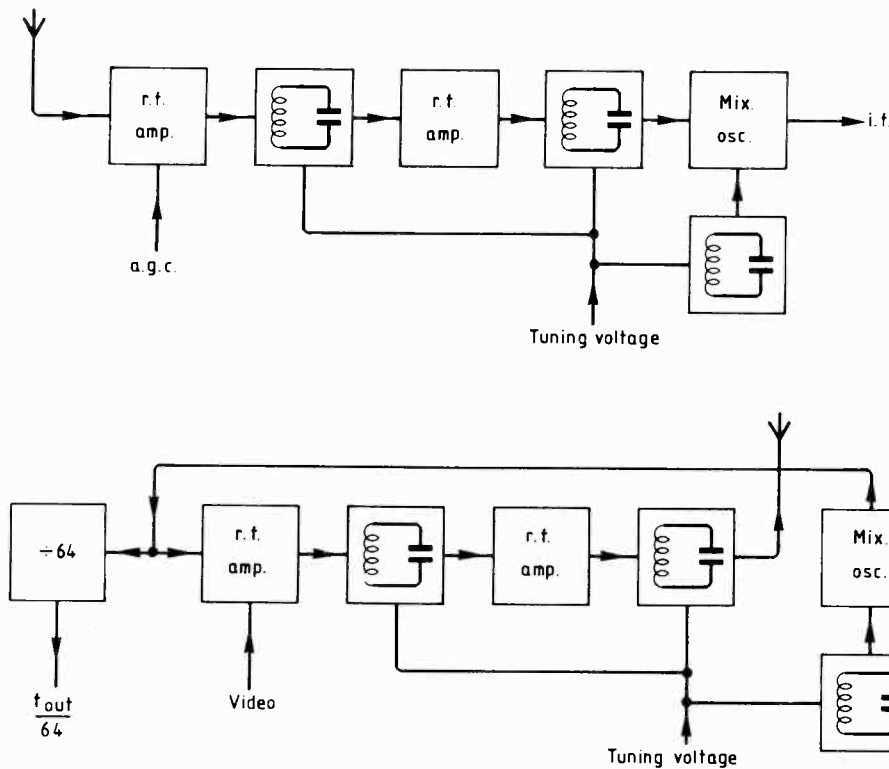


Fig. 2. Restructuring of the ELC1043 tuner to turn it into a modulator.

processor can control a second phase-locked loop, synthesizing either a 5.5MHz or a 6.0MHz sound carrier.

### Modulator

In Fig. 1 the circuit blocks that are enclosed by the broken line were the result of heavily modifying a Mullard ELC1043 television tuner. But as the purpose of this article is to describe the application of frequency synthesis, only an outline of the necessary modifications to the tuner are given. The changes, shown in block form in Fig. 2, follow an original article by Trundle (*Practical Television*, April 1975).

Three further changes were necessary beyond the circuit described by Trundle. Firstly, the length of the oscillator tuning line was increased so that the whole u.h.f. band could be covered by the oscillator. Secondly, a  $\div 64$  prescaler was fitted inside the tuner box and coupled up to the oscillator output. Thirdly, the original black-level stabilizing circuitry was improved. The result of the modifications was a tuner box that required and produced the signals shown in Fig. 3.

### Phase-locked loops

Fig. 4 shows the contents of a UAA2000 which is the device chosen for both phase-locked loops in this application. The crystal frequency chosen was 4MHz, and is used as a clock for the microprocessor as well as the second UAA2000. In both phase-locked loop circuits, the output from the reference divider is 976.5625Hz, the frequency that the u.h.f. oscillator must be divided down to. For example, channel 44 is 655.25MHz, and this must be divided by 670975 to make it equal the reference frequency. Part of the division ratio is fixed at 64 by the tuner pre-scaler and there is an additional fixed  $\div 2$  in the UAA2000. The programmable divider

must therefore divide by 5242 to obtain the correct result. Calculation of the ratio provided by the programmable divider is done by the microprocessor.

The UAA2000 accepts data in serial form made up of 18 bits. Data are transferred into the shift register on positive-going edges of the clock, and latched into the programmable divider after the enable signal goes high. The required waveforms and their timings are depicted in Fig. 5, together with the format of the serial data word. The first four bits are used in v.h.f./u.h.f. operation and are all zero in this application. The last 14 bits are the binary equivalent of the division ratio, with the first bit, bit five, being the most significant. Fig. 6 shows the data, clock and enable waveforms for channel 44. This requires a programmable division ratio of 5242 which has a binary equivalent of 0001010001111010. The order of the binary number is reversed however to satisfy the requirements of the UAA2000 shift register.

For the sound channel modulation, the microprocessor sends the binary equivalent of 2816 for 5.5MHz or 3072 for 6.0MHz.

### Circuit description

The complete circuit diagram is shown in Fig. 7. The incoming video has its sync. tips clamped to a voltage adjusted to match ELC1043 a.g.c. characteristic.

A sound carrier is generated using a Hartley oscillator tuned by an MV2112 diode. Its output frequency can be either 5.5MHz or 6.0MHz depending on the data fed into the phase-locked loop divider. The sound carrier output, as well as being fed back to the UAA2000 to complete the loop, is added to the video via an 18pF capacitor. A locally generated 700Hz tone

frequency modulates the sound carrier, though an external modulation may be connected. The correct 50 $\mu$ s pre-emphasis is provided by the 2.2nF capacitor connecting the audio to the Hartley oscillator. An ever-increasing frequency response is prevented by the 10k $\Omega$  resistor limiting the maximum amplitude at about 15kHz.

The two phase-locked loops have the same circuit but different filter time constants. Values used for the calculation of the loop filters are

$$K_{\phi} = 0.8 \text{ volt/rad}$$

$$K_o = 84.5 \times 10 \text{ rad/s/volt for vision}$$

$$\text{and } K_o = 571 \times 10 \text{ rad/s/volt for sound}$$

Both UAA2000s share the same data and clock, but have different enable signals for obvious reasons.

### Software description

Because there is no hardware or timer interrupt used in the system, the software is organized as depicted in Fig. 8.

**Initialization.** After power is applied or the reset activated, the microprocessor starts with the initialization subroutine. The following operations are performed. Input/output relations are established on ports A and B. Port A is configured as eight input lines, on port B only the line PB<sub>2</sub> is configured as input; all remaining lines are outputs. The UAA2000 circuits are set into the starting conditions, in that the input VDR, DATA, CLOCK are set into logic state 1. The starting address of the program – which is the initialization – is stored under the reset interrupt priority. The MC6805P2 or MC68705 can be reset three ways: by initial 'power-up', by the external reset input (RESET), and by an optional low-voltage detect circuit.

**Input data for vision.** In this subroutine the switches are read and debounced. The value is read in b.c.d. and compared to the value previously read. If there is no difference, no further action is required

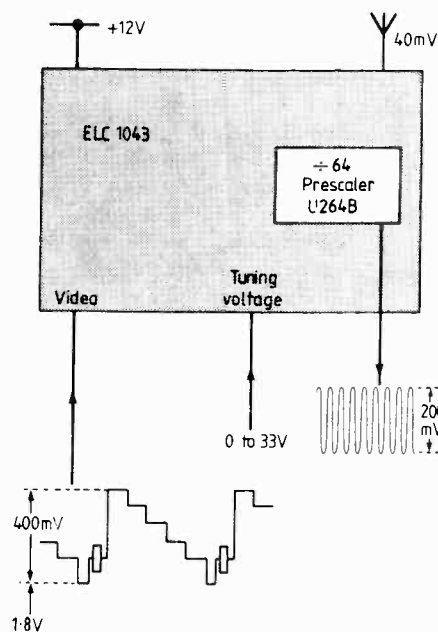


Fig. 3. Signal levels to be found around the modified ELC1043 tuner.

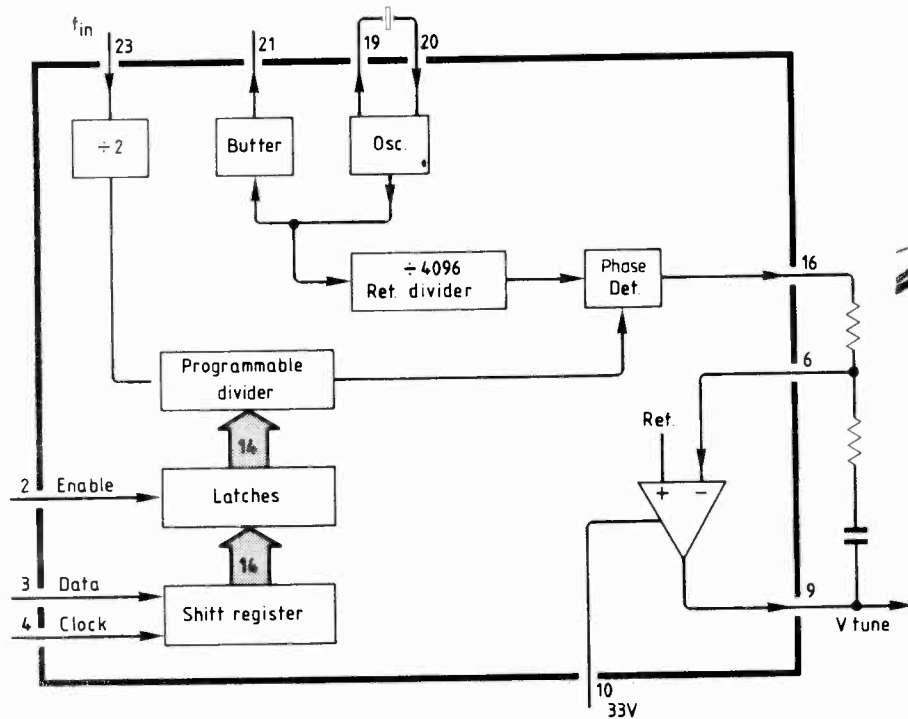


Fig. 4. Simplified block diagram UAA2000 showing the parts necessary in this application taken from Motorola data.

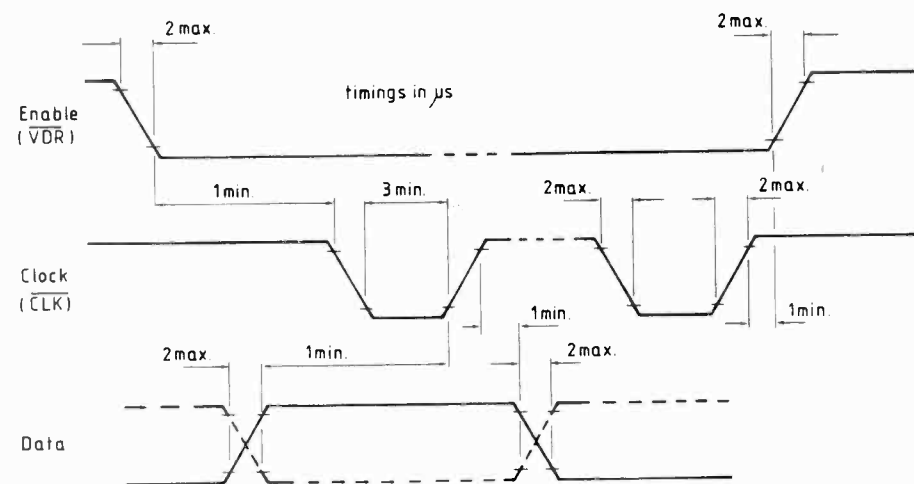
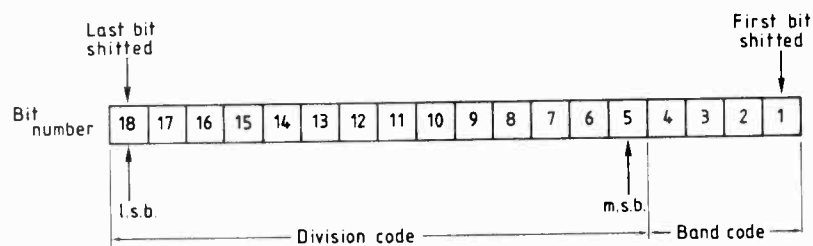
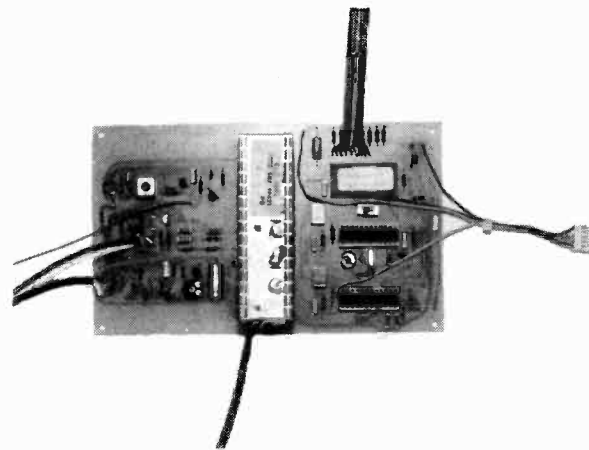


Fig. 5. Motorola UAA2000 data format and timing diagram.

and the program execution is diverted to the next subroutine. If there is a difference, the b.c.d. is transformed into the n.c.b. value. The result of the transformation is compared to the value for channels 21 and 68. If the new value is lower than that for channel 21, the value for channel 21 is considered correct. On the other side of the scale, if the new value read is greater than 68, the value for channel 68 is considered correct. In both cases the lamp is switched on, signalling an


incorrect value read from the switches.

In the next step, the division ratio for the UAA2000 circuit is calculated. The result is 14 bits long and stored in two registers. Input data format for the UAA2000 is 18 bits long and consists of the band code, which is four bits long and the input frequency division code, which is 14 bits long. High-to-low transition on the v.d.r. allows an access to the new data. The new data starts with the band code first, followed by the input frequency



Copies of the software listing and printed circuit board and component layouts are available from the editorial office at Quadrant House, The Quadrant, Sutton, Surrey SM2 5AS, in return for a stamped and addressed envelope.

division ratio code, most significant bit first. During this operation the timing must be guaranteed, as required by the data sheets for the UAA2000.

**Data input sound.** Information about the sound frequency is on the pin PB<sub>2</sub>. The input frequency division code for the sound is altered only if there was a change with the previous reading. The values that are to be sent to the UAA2000 for sound are stored in the same registers as the vision values, and the same routine for code generation is used as for the vision code. At this stage the program is returned to the reading of the possible new data for vision and the process continues. 

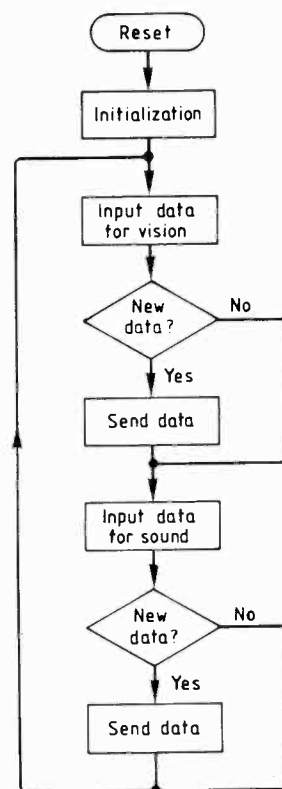


Fig. 8. Software flowchart for both sound and vision loops.

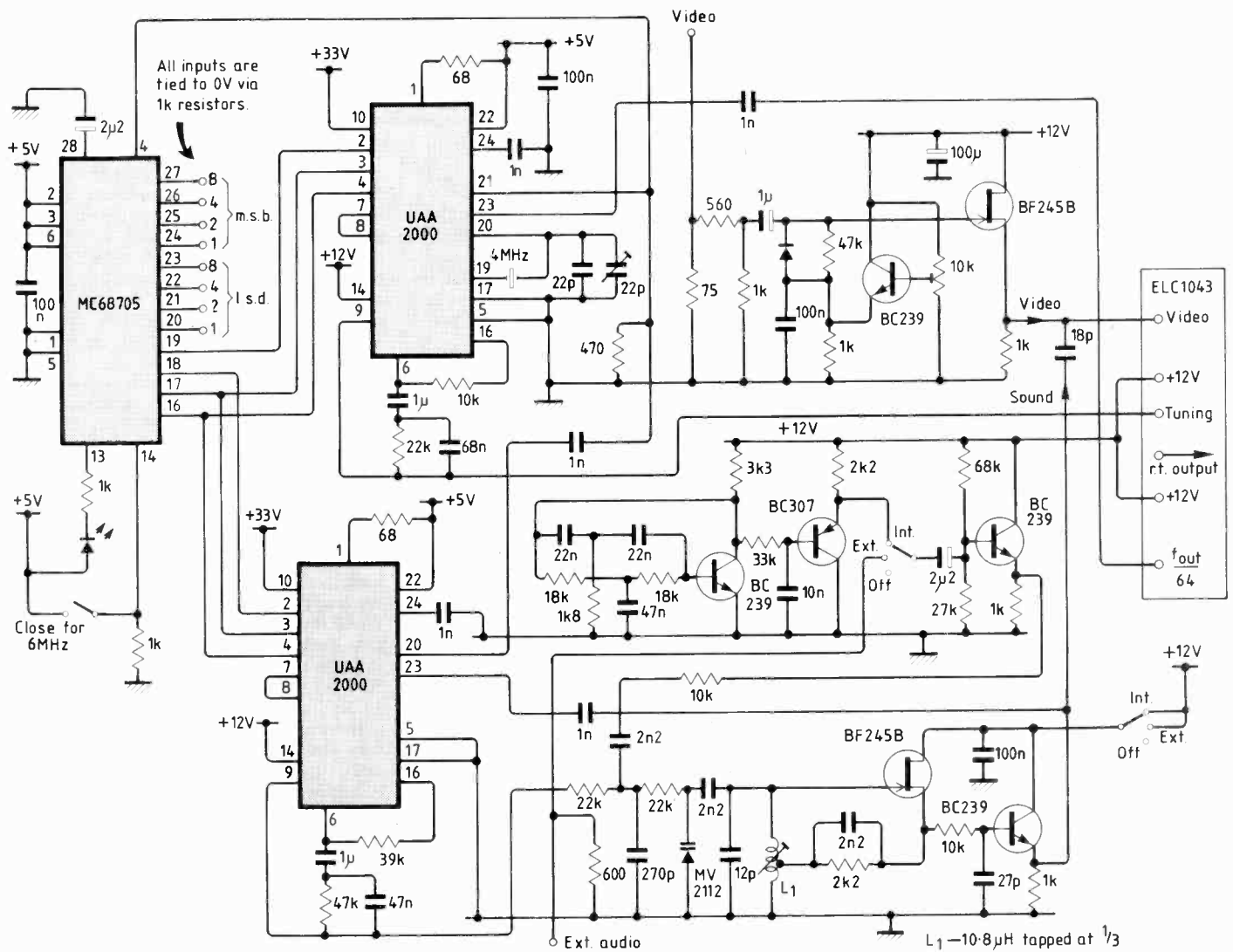


Fig. 7. Full circuit diagram of synthesized television modulator.

**Performance**

Vision carrier power +87dB $\mu$ V  
 Sound carrier power +50dB $\mu$ V  
 Residual f.m. on vision carrier  $\pm$ 3kHz  
 Vision/sound intermodulation -50dB  
 Vision bandwidth -4dB at 5MHz  
 -8dB at 10MHz  
 In settling from channel 40 to channel 41, the software processing time is 43ms, followed by a p.i.l. settling time of 11ms.

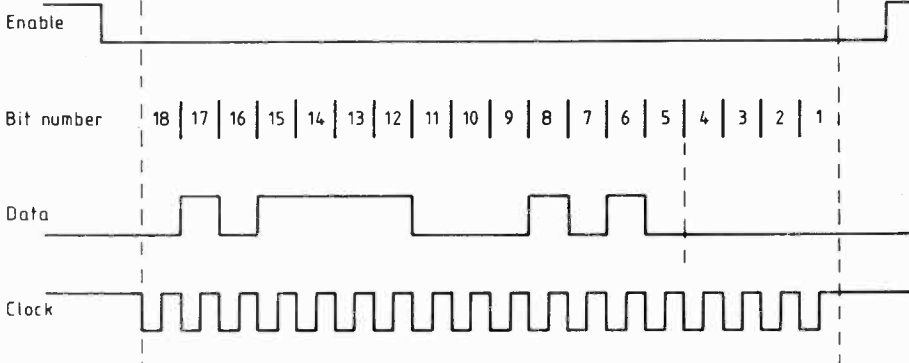


Fig. 6. Serial input waveforms for channel 44 as sent to Motorola UAA2000 controlling the modified tuner frequency.

## Testing microprocessor-based systems

about its operation by making practical use of this circuit.

### Displays

Examining the address and data buses with a logic probe or oscilloscope for a dozen or so instructions starts to prove rather tedious and if serious use is intended then it is worthwhile adding some displays and a high-speed multiple step.

Data and address can be displayed on individual i.e.s or more expensively on seven-segment displays. Either way, the addition of displays must load the 8085 as little as possible and certainly via buffers.

One approach is to wire the buffers etc to a 40 pin i.c. clip that fits over the 8085.

Figure 6 shows an array of seven-segment displays D<sub>1</sub> to D<sub>6</sub>. Displays D<sub>1</sub> and D<sub>2</sub> register the upper address byte and are driven from a 74LS373 latched on a buffered version of ALE so that it only presents one LS load. Each display is a TIL311 which includes the relevant decoder. Other displays can be used although not all can display the hex codes A to F satisfactorily, or alternatively single i.e.s could be driven from each bit. Consideration must also be made of the extra power consumption this type of circuit requires. Displays D<sub>3</sub> and D<sub>4</sub> show the lower

continued from page 45

address byte and D<sub>5</sub>, D<sub>6</sub> the data. And IC<sub>3</sub> can be either a straight buffer such as an 81LS95, or a latch clocked by RD or WR so that either can be monitored. Note that this circuit loads AD<sub>0-7</sub> with two buffers.

### Multiple step

A multiple-step facility can easily be incorporated, as shown in Fig. 7. The capacitor value can be varied to suit personal choice.

There are many other enhancements that can easily be made, however the circuits and notes described here have to be found quite adequate for simple hardware and software debugging.

# LETTERS

## TEM-WAVE PHYSICS

Let the fierceness of Mr Catt's response to Mr Dalton (February 1984 issue) obscure what he said, could I diplomatically support all that was contained in his letter while at the same time describe a situation where E and H are 90 out of phase. This should please Mr Dalton.

But first let me remind Mr Dalton that the opposite of "static" is "dynamic" and not "oscillatory". The last is just one of many modes of motion which need not even be periodic. This is particularly important because the example I propose to give for E and H being 90° out of phase is static. This should please Mr Catt.

Starting from Maxwell's equations it is easy to derive equations of wave propagation for E and H, the solutions of which are

$$E=f(x-ct)$$

$$\text{and } H = \frac{1}{c\mu} f(x-ct)$$

where f can be any function, not just sinusoidal or even periodic e.g. a digital (level) change, a single pulse - square or any other shape.

The variation (f) of H matches precisely the variation of E (also f) whatever whatever f happens to be. There is no delay between E and H or, in the case of f being sinusoidal, no phase difference. As Mr Catt states there is no causality between E and H. However, and this may be part of the origin of Mr Dalton's error, there is a rotation of 90° from E and H which is right handed about (not along) the direction of propagation. Thus if f is sinusoidal E and H are in phase but at right angles to each other in space, not time.

If the equations above are divided one into the other then

$$\frac{E}{H} = \frac{1}{c\mu} = \sqrt{\frac{\mu}{\epsilon}} = Z_0$$

where  $Z_0$  is the wave impedance of free space (about 375 ohms) which is independent of f.

If E and H were sinusoidal and 90° out of phase as Mr Dalton suggests, then  $Z_0$  would be the tangent i.e. from minus infinity to plus infinity. This would make it difficult for a wave to propagate. At the very least it would imply causality if one knew which occurred first and at worst would mean changing the title of your illustrious magazine.

This brings me to the example of E and H being out of phase and possibly the other half of Mr Dalton's confusion.

Suppose that a sinusoidal wave described by

$$E_1 = E_0 \sin \left\{ \frac{2\pi}{\lambda} (x-ct) \right\}$$

has superimposed on it an equal wave but travelling in the opposite direction, say by reflection, described by

$$E_2 = E_0 \sin \left\{ \frac{2\pi}{\lambda} (x+ct) \right\}$$

Some trigonometry reduces the sum of these to

$$E_1 + E_2 = 2E_0 \sin \frac{2\pi x}{\lambda} \cos \frac{2\pi ct}{\lambda}$$

$$\text{or } 2E_0 \sin \frac{2\pi x}{\lambda} \cos \omega t$$

$$\text{Similarly } H_1 + H_2 = -2H_0 \cos \frac{2\pi x}{\lambda} \sin \omega t$$

This results in the well-known standing wave where the nodes of H correspond with the peaks of E and vice versa i.e. 90° out of phase. When E is a maximum, H is zero everywhere. Then H

grows and E decreases until it is a maximum and E is zero, and so on cyclically. Thus the standing wave has all the appearance of transforming itself from an entirely electric form to an entirely magnetic one and vice versa. But it is just an illusion, for as Mr Catt states, there is no causality between E and H for a single wave, still less is there any between two in which we only observe their interference pattern.

This, I hope, explains the source of Mr Dalton's confusion.

Finally I would like to disagree with Mr Catt (only in a very minor way) concerning his references. Carter in his book "The Electromagnetic Field in its Engineering Aspects" pages 266 to 276 is quite specific about there being a delay (or phase difference in the sinusoidal case) between E and H, both in his diagrams and text, and of which the above is, I trust, an accurate paraphrase. They correspond, though in different words, with the views expressed by Mr Catt.

E. O. Richards  
Hitchin  
Herts

PS: For those who share Mr Catt's disgust with sin and cos I commend a closer look at Walsh functions, an introduction to which appeared in these pages in January 1982. An excellent book on the subject is "Walsh Functions and the Engineering Applications".

## OPERATING FORTH

The articles by Brian Woodroffe and Roy Easson on the description and applications of the Forth language have been admirable and must have done much to popularise this elegant little computer language. In particular Mr Easson's introductory paragraphs are as concise an explanation of Forth as I have seen anywhere.

Of all the features of Forth the one which seems to be over-emphasized is the manner in which it is extensible, i.e. that new words, defined by the user, can be added to the dictionary thereby extending the language. This mechanism is not unique to Forth. Most languages especially the so-called block-structured ones have similar features. In Algol, Pascal and Coral 66 the section of code which carries out one small well-defined task can be isolated, called a procedure and then given a unique name. Thereafter, whenever that particular little job needs to be done, the controlling program merely calls that procedure by name. Similarly the procedure can be incorporated into bigger procedures and so on. Most large operating systems with a job control language have a similar arrangement. Sequences of commands are put into a named file (a macro) that can then be considered as an extension to the j.c.l. since invoking it causes the machine to obey the command sequence it contains. That macro may also be incorporated in further macros. Where Forth scores is surely the simplicity with which its new words are defined.

It is this simplicity and conciseness which are its real advantages. Forth is not just another language. It is also a complete miniature operating system. In size, it requires much less memory than most compilers would require as their workspace.

In implementation it means that Forth can be installed on most machines quickly and economically, especially if the FIG-Forth model is used. In operation, it means that a new user can

sit down at any keyboard and use Forth without needing a week or more to learn how to drive the host computer first (the problem that ADA is striving to beat). Time on development is saved and, due to the structures of Forth, so is time and effort in testing. Any project manager on a tight budget will tell you how valuable these savings can be.

I don't wish to eulogise Forth, for it is not the perfect language by any means. But its more unusual virtues are very real and deserve recognition. It comes much closer than any other so far to my personal ideal of a Universal Assembler Language that I can afford.

L. J. Smith  
Barnet  
Herts.

## 'CURRENT DUMPING'

Readers may be interested in the basis on which 'current dumping' is founded. In the *Wireless World* for January 1973 and October 1974 I published two contributions on 'error take-off', as I now call it, which preceded P. J. Walker's AES lecture on current dumping in March 1975.

However, Vanderkooy and Lipshitz have very clearly shown in the *JAES* (Jan./Feb. 1980, Fig.6) the connection, reproduced below. It may well help others who wish to develop error take-off circuits, of which current dumping is a successful example.

A. Sandman  
London NW3

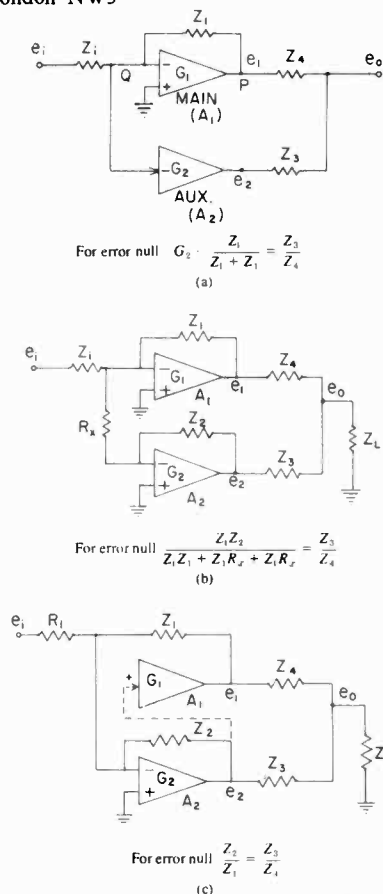


Fig. 6. (a) Sandman's 'error take-off' principle, in which any errors (including gain errors as well as nonlinear distortions) caused by  $A_1$  appear at its virtual ground summing point  $Q$  and are thus available for amplification by the auxiliary amplifier  $A_2$  and subsequent subtraction from the output signal. (b) The circuit rearranged to make use of an operational amplifier for  $A_2$ . (c) Showing how 'current dumping' is derived from (b). The resistor  $R_1$  has been removed, and  $A_1$  can derive its input signal from the output of  $A_2$ . If  $A_2$  has a large gain then there will be no distortion in  $e_o$  if  $Z_2 = Z_3 Z_4$ .

## FORTH COMPUTER

Although James Kidd and I agree about what makes the 6809 so suitable for FORTH, I disagree with his rankings: 1 data stack access 2 NEXT 3 control stack access. As NEXT is executed every time any code fragment finishes it is executed as often as all other fragments put together. Hence it is the most critical piece of code in any FORTH implementation. It is the execution frequency and not the static frequency of occurrence that matters (i.e. those things at the centre of loops matter more than those outside). Conversely the execution time of 80% (or is it 66%?) of the code has minimal effect on the overall performance. Hence the fast execution of infrequently encountered instructions (e.g. divide, string search versus add, move etc) is almost irrelevant and hence the RISC argument. It is a mistake to make a virtue out of anything that extends NEXT not only because NEXT is time critical but also because error correction and program testing in a high level interactive environment should be done with the tools of that environment and not with the aid of single step debugging.

The FORTH primitives DOCOL and SEMIS are the most commonly executed. Implementers of FORTH on processors which do not support two stacks should investigate the potential of making the control stack the processor "normal" stack and maintaining the data stack via a user pointer. This should benefit the 8088 for the common control stack operators (DOCOL, SEMIS) only push and pop values. This would leave BP free to access the data stack using indexing modes as noted by J. O'Connor. The 8088 BP register is used for the control stack in the FIG model.

The 9900 series memory to memory architecture appears to be peculiarly unsuited to computation and FORTH for most operations involve the time penalty of three data accesses to memory whereas more normal architectures (e.g. 6800/8080 etc) seldom require more than one. Texas have dropped their 99/4A home computer (9995 based) and their latest personal computers incorporate more mainstream products. However, the 9995 by virtue of its own on-chip memory that could be programmer maintained as an instruction cache could be an interesting prospect for FORTH. Caching is a method of keeping frequently accessed data (or instructions) in fast on-chip memory which makes the whole memory system look faster. It is similar in concept to paged virtual memory between disc and main memory which FORTH has. I leave it to the interested reader to follow this up. (The Z800 with genuine on-chip cache looks especially interesting in this respect.)

Mr Bacon goes on to castigate me for trying to make some allowance for the processor's required memory speed. In any design with a half decent size of memory the cost of that memory will be more than that of the processor (in my case 4:1 approximately), hence it is reasonable to make some allowance for higher cost of faster memories. Hence my crude attempt to rationalize processor speed with memory access time. As James Kidd points out access time does not linearly scale with clock rate (especially if wait states are used). However, some allowance must be made. Also as James Kidd points out my design should use 350ns eproms, although I still use 450ns parts with a standard 6809 running at

We assure Mr Woodroffe and his readers that the reprinting of his correspondence was entirely inadvertent! - Ed.

1.5MHz. As the read/write control signals (MR, WE etc) are conditioned by the processor clocks there is no problem if the chip selects glitch upon an address change.

The on-chip memory used as a program cache is the main reason why Texas were able to show the 9995 running the Intel benchmarks faster than the 8088. One would expect the 9995's performance to be less good if the program could not fit the cache. So there are problems about the suitability of the benchmark as a performance indicator for the target application. Similar reservations should be borne in mind when looking at the Sieve of Eratosthenes results. If your application is scientific (floating point operations dominate) then the Sieve results will not be a good indicator. You should think in terms of a processor that supports a numeric co-processor (i.e. a newer 16-bit or a mini), but if you want to run FORTH then in most any environment the 6809 takes a lot of beating.

It is not true that 'in most high level languages most time is spent pushing garbage'. Today's compiler technology is such that an optimizing compiler will produce more efficient code than a human can. Not only will it be done correctly every time but also the computer is much better at taking a global picture. Hence reasons why neither Inmos (Occam for the transputer) nor Xerox (for the Mesa system) issue details of the machine instruction set, for the compiler will produce optimum code. Today most operating system kernels are written in compiled code (e.g. Unix in C). High-level languages are accepted as the means to get programs to work more quickly and thus save programmers' time. No matter how fast a program runs, unless it runs correctly, it is wasting programmers' time.

Dr Croker of Woking has written to me pointing out that the FIG model for the 8088 is coded sub-optimally. NEXT can be shortened to the four byte macro 'LODSW; MOV BX, AX; JMP [BX]' improving NEXT's speed by about 40%. It is not true that as originally coded there have to be multiple copies of NEXT for the JMP NEXT is coded as a short jump (+-32k bytes) and not a near jump (+-127 bytes) as Martin Bacon supposes. Second, by keeping the top of data stack in a register (e.g. DI), many data primitives can be improved (e.g. @ becomes MOV DI, [DI] etc). This technique can be applied to any simulation of a zero address machine. I looked into this when I coded my 6809 (top of stack in D) but I felt the disadvantages to the branch primitives (OBRANCH, LOOP) etc would outweigh the benefits to the data primitives (@, + etc).

Mr Carter of Nottingham has also written to me showing that my method for producing a 11µs data transfer routine can be improved. He points out that as the transfer loop does not affect the carry flag then it can be cleared upon loop entry. This is then tested for upon possible loop exit and in the normal case it will loop back. However when the sector transfer is complete the NMI interrupt occurs to set the carry flag in the saved context hence letting the processor exit the loop. As the interrupt does not cause the loop exit but only flags for it there is no need to have differing interrupt vectors. He also points out that if the WD1793 exhibits an interrupt latency near its maximum rather than typical value my data transfer loop could fail, requiring a re-try ( $t_{irr}$  500ns typ, 3000ns max).

Further failings in my proof readings have been detected by constructors. The full list of

errors appears to be:

- pins 39/40 of the 6821p.i.a. are shown reversed June page 56.
- power supply op-amp is MC3405 July page 61.
- power supply op-amp pins 5/6 shown reversed July page 61.
- 6809 interrupt pins are irq 3, firq 4, nmi 5 May page 56.
- LS122 for pin 9 read 11, for pin 11 read 13 May page 56.
- dot clock oscillator 51pF connects to IC<sub>74</sub> pin 9 not 8 June page 56.
  - Some constructors' computers hang upon producing the log on message. I have been unable to reproduce this. It is apparently cured by pulsing an interrupt low.
- LS139 see corrections in June issue, page 58.
- LS138 pin 15 label 'v' not 'u' June page 56.

A source listing is also available.

Brian Woodroffe  
Edinburgh

## PRECISION PREAMP

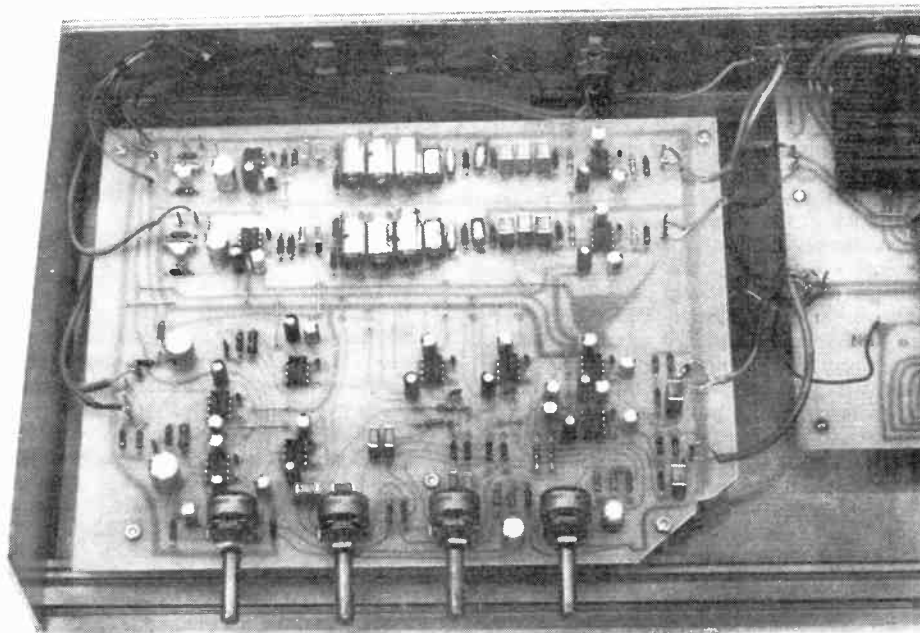
I should like to thank Mr Armstrong (Letters, January) for the interest he has taken in my latest preamplifier design. Unfortunately I am in the position of having to contradict virtually everything he says. At the end of my article I expressed the pious hope that anyone wishing to dispute points of the kind raised by Mr Armstrong would arm themselves with objective evidence (i.e. actual measurements). Sadly, he has not done this.

I was not surprised that I failed to convince everyone that tone controls could actually be useful; although it is less than ten years since a preamp without them would have been unthinkable, since then fashion and dogma have been invading a field in which the technical challenges have largely been overcome. Omitting the tone controls will not save a lot of components, as you must retain not only the high-impedance buffer, but also the tone-control op-amp, in order that the balance control can be retained. This also keeps all ins and outs in phase. I should like to emphasize that with the controls set centrally the signal undergoes no spurious phase shift or detectable degradation. Nonetheless, here are the details for a no tone-control version.

(a) Delete R<sub>21</sub>, and C<sub>19</sub> to C<sub>21</sub>, and also the treble control.

(b) Replace R<sub>20</sub> and the bass control with short circuits, and change R<sub>18, 19</sub> to 1.7k. This should be satisfactory, though I must emphasize that I have not tested it exhaustively.

I do not believe that I have neglected any of the important parameters of electrolytic capacitors. They are quite adequately reliable when operated with no polarizing voltage; only the application of a reverse bias greater than 1V is likely to cause breakdown of the dielectric film. This of course cannot happen when an electrolytic is being used as an audio coupling capacitor, because the voltage across it does not change significantly during any cycle of normal audio frequency: if it did then it would act as a low-cut "filter". Of course, no-one in their right mind



This printed circuit board, accommodating a stereo version of D. Self's precision preamplifier (*Wireless World*, October 1983) is available from its designer, P. A. Joiner, at Glensuie, Lybster, Caithness TW3 6BS, for £13 inclusive of postage.

The preamplifier uses the recently introduced NE5534 op-amp circuit. Measurements on Mr Self's prototypes gave a signal-to-noise ratio on the moving-magnet disc input of 81dB (referred to a 5mV r.m.s. input at 1kHz). Distortion on the line inputs for a 100mV signal was 0.005% (1-20kHz).

would attempt to define a critical time constant using a wide-tolerance electrolytic, though I do wonder quite how well Mr Armstrong understands this point.

It should also be unnecessary for me to point out in a journal of *WW*'s calibre that the reason op-amps do not saturate themselves with their own offset voltages is because they have d.c. negative feedback, not despite it.

Mr Armstrong's next point surprises me; if any preamps have been built using nothing but non-polar electrolytics, then I should think they were very expensive and bulky. All a waste of money too, because this fabled "electrolytic capacitor cross-over distortion", which is, I assume, what he means, simply has no existence in reality. Any old electrolytic will pass an audio signal with less than 0.001% harmonic distortion (the limit of my Sound Technology testgear) and no questions asked. I fully understand that many people will consider sinewave testing hopelessly unhip, and will claim that this alleged audio degradation mechanism, like so many others, is only audible on critical listening to music of a specified genre. However, like many engineers, I find it hard to believe in a degradation mechanism that is intelligent enough to tell the difference between music and sinewaves, and only mangle the former. I can imagine that a complicated circuit could be devised with this property - a "pathological amplifier", but I do not see how such an inevitably complex mechanism could lurk inside a humble capacitor.

Similar objections apply to the mysterious failings in non-gold connectors. While it is in

theory possible for a rectifying contact to be set up, in practice it just doesn't happen; if it did it would be instantly audible as gross distortion. It is instructive to set up the above-mentioned testgear, with the oscillator output returned to the analyser input via the connector under test, and to attempt to generate distortion (even 0.001% would do) by loosening or maltreating it. Having failed to produce a convincing rectifier from a series of ancient connectors, and various scraps of oxidized wire, I was eventually driven to using a rusty iron nail as one contact. This was capable of generating some second-harmonic distortion, but while it may be relevant to crystal sets it has nothing to do with hi-fi.

There is no point in worrying about electrolytics or connectors in the signal path. Not only are they normally harmless, but any signal your hi-fi system is likely to encounter will have already passed through hundreds of both in the recording process. The complexity of modern mixing desks and multi-track recorders is such that only real, rather than mythical, engineering considerations are given house-room.

Mr Armstrong, like all too many hi-fi enthusiasts, has come on strong with assertions but without a single shred of objective evidence.  
D. R. G. Self  
London E3

## XY PLOTTER

I was most interested in the article on constructing a cheap X-Y plotter in the January issue of *Wireless World* and in the follow-up letter on drawing straight lines in the subsequent issue. You may be interested that a complete straight line drawing program is to be found in the Sinclair ZX81 BASIC Programming manual on page 121. This is the first edition dated 1980 - I have not checked that it is still in there in any subsequent reprints. I have implemented this program in machine code on the *Wireless World* Nanocomp, two of the 7-segment displays being used to indicate the rotation of the stepper motors.

I understand that this is an implementation of a Digital Differential Analyser algorithm (it integrates a constant). It would only need a second routine with an inverter to draw circles or parts

of circles, this being a digital equivalent of a sine/cosine generator using two integrators and an inverter (I am an analogue computer enthusiast myself). Maybe there is someone out there who may like to investigate!

M. D. J. Foreman  
Department of Computer Studies  
Bristol Polytechnic

## FUEL LEVEL SAFETY

I am concerned about the safety of the "Fuel-level indicator" Circuit Ideas, (January 1984). When used with liquids like petrol, precautions to prevent a static discharge from the tank to the "outer copper tube" should be taken. The connections to the copper tubes comprising the sensing capacitor should be in a vapour-free region, lest a mechanical failure occurs while the circuit is live.

C. D. H. Williams  
Durham University

## PREFERRED HISTORY

I'm afraid that both Watson (November 1983) and Scott (January 1984) impute too formal a construction of the preferred value series. It has, by the way been variously called the stepped incremental series, logarithmic and exponential series. Many laws could no doubt be fitted closely to the values but that is not how the system was designed.

At the outbreak of the 1939-45 War, the standard series for resistors was 10, 15, 20, 25, 30, 35, 40, 45, 50, 60, 75, 100. From these 35, 45 were frequently omitted by manufacturers. These omissions were of academic interest only, since designs called for almost any value required viz. 140 or 2300 or 37500, which values were generally found by selection.

However the rapid build up of sophisticated electronics in 1940 to '45, saw industry being slowly choked by demands for large quantities of outlandish valued resistors. The process of selection had been passed back from the user to the manufacturer, and action had to be taken to relieve the situation. The same of course was happening in other components, particularly valves.

In October 1941, the MAP, MOS, and Admiralty set up the Inter-Services Component Committee. With representatives in the design establishments, it was intended to control the supply of components, and to prevent wastage of manufacturing effort. One of its aims was also to standardize on components, to simplify stockholding by the Services supply branches, and to simplify servicing. One of its early tasks, through its technical committee ISCTech.C was to try to devise a value series, and at the same time reduce the number of values in the basic (20%) series.

A number of draft proposals were made in a memorandum sent to the Design Establishments, TRE, ADRE, RAE and ASEE, as well as equipment manufacturers. There were many uncomplimentary remarks thrown around concerning what many considered to be interference, until it was realised that (a) the ISCS meant business and (b) ultimately standardization would be in the interest of designers as well as the War effort in general.

The initial series hinged around the R x 1.5 sequence. When expanded this gives a reasonable series at the lower end of the scale: 10, 15, 22.5 (rounded to 22) 33, but from here, the scale widens 49.5 (rounded to 49), 73.5 (rounded to

73) and 109.5. Clearly the range should fit into the decade better.

Possibly a disproportionate amount of effort was put into the problem, remembering that we were in a crucial stage of the War, and that if any real benefit was to come out, the solution had to be found quickly, as otherwise it would be too late to affect production within the foreseeable future. In the meantime vast numbers of new equipments were being designed using the decimal series.

One event however concentrated the minds wonderfully. A ship carrying a bulk consignment of resistors from the USA was sunk. Many equipments were intended to be totally provisioned by this consignment, but one of them was the GL3 (AA No 3 Mk2) which required over a million resistors mainly for the Presentation (display) Unit. Immediately, The Gramophone Co. (EMI), who were responsible for the PU and already resistor manufacturers on a relatively small scale, set up a vast crash programme to produce not only those components they themselves required, but also to satisfy other manufacturers. They used the spiralled carbon process and I enclose some samples of the resistors made at that time, including also some wirewound ones (on glass).

In expanding production the company produced preferred series of their own for use by their own designers, arguing that any decimal value could be satisfied *within its tolerance* by the nearest preferred value. Their series was 10, 15, 23, 32, 47, 68, 100 in which the values 23 and 32 could equally have been 22 and 33: they were simply the nearest whole numbers to 20, 25 and 30-35 respectively. Similarly 47 is the near equivalent of 45 and 50, and 68 that of 65 and 70. The important thing however is the recognition that it is possible to build a series built on tolerances.

In the meantime other thoughts had also turned to the use of tolerances to delimit the series, using the tolerance limits to touch or just slightly overlap. Thus any value resistor as manufactured could be assigned a unique value, *within its tolerance*. If we consider the 20% series the following are the possible figures:

```

10 15 22 33 49 73 100
    49 72
    48 71
    48 70
    47 69
    47 68
  
```

In most cases however, the +20% tolerance of the higher choices (69-73) exceeds 80 (=100-20%) by substantial amounts. If the tolerance band overlaps are minimized and equalized, the most likely series becomes 10, 15, 22, 33, 47, 68, 100. Similar methods can be used to fix the 10 and 5% series.

The preferred value list was promulgated in late 1942 or early 1943 and was published in *WW* and other periodicals in March 1943 (*WW* vol. 49 no. 3 page 71). The scales were not so much mathematical, but were good old compromises born of the necessity to simplify manufacture. They were, even so, too late to have a significant effect during the War. They became however lastingly effective for resistors, but although capacitor lists have quoted the standard values since the 1950's, it is only in the last few years that they have become almost universal. Though there were still continued murmurings about different scales (see for instance Bowen, *WW* vol. 50 no. 8 August 1944 page 253).

The arguments about the basic structure of the E series have flared from its early days, but one of the most effective explanations came

from 'Cathode Ray' in *WW* in 1952 'Why 47' (vol. 59 no. 2, page 77).

Donald H. Tomlin  
Malvern  
Worcs

## GPIB/IEEE488 INTERFACE

It was with great interest that we read the article by A. G. Ray in your February issue, entitled "An IEEE488 Interface for the BBC Micro," and we totally agree that the BBC machine with an IEEE488 interface is a powerful combination for automated testing and measurement. However, we were most surprised to learn that this was the first IEEE 488 interface available for the BBC Micro, since we have been manufacturing and marketing such an interface for more than six months!\* Our interface, the CST Procyon, has been extensively featured in the electronics press, and *Wireless World* itself has carried advertisements for it. So it was some shock to learn that Mr Ray was unaware of its existence.

From the information give in his article, it would appear that Acorn's design philosophy has been different from our own in that we have tried to make our interface easy to use. To appreciate the difference between the interfaces, it is only necessary to compare the article's example program with an equivalent one for our own interface.

```

10 *DISC
20 result%=OPENOUT("RESULTS")
30 *IEEE
90 siggen%=7
100 dvm%=3
110 FOR frequency%1000 to 10000 STEP 100
130 PRINT#siggen%,"0.1V,"=STR$
    (frequency%)+ "Hz"
160 INPUT#dvm%,reading$
180 response=20*LOG(VAL
    (reading$)/(0.1*0.7071))
190 *DISC
200 PRINT#result%,frequency%,
    response
210 *IEEE
220 NEXT frequency%
250 *DISC
260 CLOSE#result
  
```

There are three principal areas in this example where the CST Procyon Interface is simpler to use than the Acorn.

1. When the interface is initialized, the Procyon makes sensible default assumptions - these make it unnecessary to include lines 60 to 80 of the Acorn program.
2. The organisation of channel and file handling is different: the Procyon handles all device addressing automatically, so, when a string is sent to a device, the interface unaddresses any previous listeners and then addresses the target device to listen. This removes the need for a separate command channel and lines 40, 50, 120, 140, 150 and 170 in the Acorn program are unnecessary.
3. The Procyon provides simplified file handles for use with devices with single primary addresses. These are automatically opened when the interface is initialised and may be used without further use of the OPEN command

\*We understand from Mr Ray that prototypes of the Intelligent Interfaces design, complete and with software in rom, reached Acorn as long ago as November 1982. No changes were made for the production units, the first of which were delivered to Acorn in November 1983. - Ed.

though it is perfectly valid to do so. This simplification allows us to eliminate the OPEN and CLOSE commands in lines 90 and 100, 230 and 240.

These simplifications will make programs considerably shorter and much easier for the uninitiated to understand.

Polling is another area in which the Procyon is far simpler than the Acorn: serial and parallel polls are both easily and quickly done using the BGET# command on special channels allocated by OPEN.

For a serial poll: (of device 7)

```

serial poll = OPENIN("SA7")
response = BGET# serial poll
and for parallel poll: (of all devices)
parallel poll = OPENIN("P")
response = BGET# parallel poll
  
```

The Procyon interface also allows all bus commands to be sent individually. Here, we use a different operating system interface - the "Commands" or command line interpreter OSCLI. We also use the mnemonics recommended by the IEEE488 standard, rather than the cumbersome Acorn command strings:

```

Acorn - PRINT #cmd%, "LOCAL
LOCKOUT"
CST Procyon - *LLO
  
```

Many powerful operating system features of the Procyon can be used because of its similarity to other filing systems. The commands "LOAD" and "SAVE" may be used to move blocks of binary data, with a maximum rate of over 50 kilobytes per second; the "SPOOL" and "EXEC" commands and the DFS utilities "DUMP", "TYPE" etc. may be used in the same way as other filing systems.

Users who wish to use the interface as a simple talker/listener are given full software support rather than being left with the vague advice to PEEK/POKE into hardware registers.

The Procyon uses secondary addresses to select between the various functions which are implemented. One selects the filing system on the device and this can be used for transferring programs and data between BBC machines and other computers. It is both faster and more standardised than the RS432 interface.

Another secondary address sends incoming characters to the v.d.u. driver routines, allowing the device machine to be used as an inexpensive graphics display screen for another machine. Software support is also provided for passing control of the bus from one controller to another.

Assembler programmers have a choice of using the standard filing system calls in the "usual" way, which is sufficiently straightforward to be worthwhile in the Procyon system, or they can use a low level interface corresponding to the mnemonic star commands, but accessed through calls to Osbyte 139 (\*OPT).

The Procyon interface is available in a special version optimized for use with CBM discs as an alternative to the disc filing systems and allows for use of CBM hard disc units. Support is also provided for the widely used Torch Z80 second processor within the standard interface. A bus analyser rom will also be released shortly.

The many features of the Procyon Interface are fully explained and documented in a 130 page manual, which includes a tutorial section to help the novice user through the first steps of setting up an IEEE488 system.

Guy Jennings  
Procyon Research Ltd  
Martin Baines  
Cambridge Systems Technology.

# GPIB combiner

Up to six standard g.p.i.b. controllers can be simultaneously connected to a set of standard peripherals. A typical application is the sharing of one disc unit and one printer between several CBM Pet computers.

The GPIB, HPIB, IEEE-488 or IEC625 bus is well known and widely used because of the ease with which it may be used to interconnect many peripheral devices. GPIB-compatible devices are made by many manufacturers and range from printers and disc units to industrial power controllers, network analysers and digital multimeters. A dozen or so of these devices are simply attached to one computer or controller using the specially designed connectors which can be plugged into each other. The 24 wires which make up the bus simply run in parallel from one device to the next. The main disadvantage of the bus is that only one controller may be connected to the string of peripherals at one time. However, with the GPIB combiner described in this article, up to six controllers can be linked via separate 24-core cables. A single 24-core cable leads from the combiner to the peripherals which are "daisy-chained" in the usual manner.

The prototypes for this design have been in use for over three years where a varying number of CBM Pet computers have needed to be connected to a varying number of printers and disc units. They have been very successful and the users are rarely aware of the existence of the combiners. However, the Pet does not use all of the functions which are provided for in the IEEE definition of the bus (in particular the serial and parallel poll sequences) and I cannot guarantee that the combiner will work with controllers built by other manufacturers.

Table 1 shows the designations of the 24 lines which make up the bus. The 16 signal lines all use negative logic, i.e. zero volts is logic one. At each device on the bus, each line is driven by an open-collector buffer and at each buffer there is a two resistor arrangement to pull up the line to about +3V when the transistor is off (Fig. 1). In this way all lines of the bus are nodes of a wired-or gate. That is, any device can pull a particular line low, but it is only when all devices are not pulling a line to zero that it floats high. The high state is also the idle state for all lines.

The operation of most of the lines of the bus is not altered by the functioning of the combiner and so a full description of the bus is not presented here. An accurate and readable description of the working of the bus is given in the references.

The bus functions by entering various modes in which different devices have control over different lines. For most com-

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by David J. Greaves

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munications, only four states are used. These are:

● **Idle mode:** this is the quiescent state which must exist before any communications can occur. All lines are high except possibly for remote enable (DEN) which is hardwired low in some systems. In particular both NDAK and NRFD are high, a state which can always be used to detect the idle mode.

● **Device talker mode:** in this mode the controller is receiving a string of bytes from a device connected to the bus. The bytes are transferred along the bus on the eight data lines DA<sub>0</sub>-DA<sub>7</sub>. Handshaking is performed using the three wires NDAK, NRFD and DAV. The talking device drives DAV while the controller drives NDAK and NRFD. When the talker comes to send the last byte in the string, it also pulls EOI (end of identify) low. EOI is normally high. The controller recognizes this signal and will then prepare to terminate the data transfer and return to idle mode.

Table 1. GPIB line designations

Pin name	Type	Mnemonic	Name
1	Data	DA <sub>0</sub>	Data 0 (least significant)
2	Data	DA <sub>1</sub>	Data 1
3	Data	DA <sub>2</sub>	Data 2
4	Data	DA <sub>3</sub>	Data 3
5	Control	EOI	End of identity
6	Handshake	DAV	Data valid
7	Handshake	NRFD	Not ready for data
8	Handshake	NDAK	Negative data acknowledge
9	Control	IFC	Interface clear
10	Control	SRQ	Service request
11	Control	ATN	Attention
12	Control	REN	Remote enable
13 or A	Data	DA <sub>4</sub>	Data 4
14 or B	Data	DA <sub>5</sub>	Data 5
15 or C	Data	DA <sub>6</sub>	Data 6
16 or D	Data	DA <sub>7</sub>	Data 7 (most significant)
17 or E		GND	Ground
18 or F		GND	Ground
19 or H		GND	Ground
20 or J		GND	Ground
21 or K		GND	Ground
22 or L		GND	Ground
23 or M		GND	Ground
24 or N		GND	Ground

● **Device listener mode:** this is similar to the talker mode except the controller and device swap control of the lines NRFD, NDAK, DAV, DA<sub>0</sub>-DA<sub>7</sub> and EOI. Hence bytes are transferred from the controller to the device. (Many devices such as printers are listen-only devices.)

● **Command mode:** it is likely that more than one device will be connected to the bus, and so before communications can take place the controller must transmit information to select one (or possibly more) of the devices present. Also, many physical devices have several logical registers within them and these too must be distinguished. The solution is to give each physical device a distinct device address (or device number). The different registers within a device are also given a number – the secondary address. Both halves of the total address are integers in the range 0 to 30. It is this information that is sent in command mode. Command mode can always be identified by ATN (attention) being low.

## A typical transaction

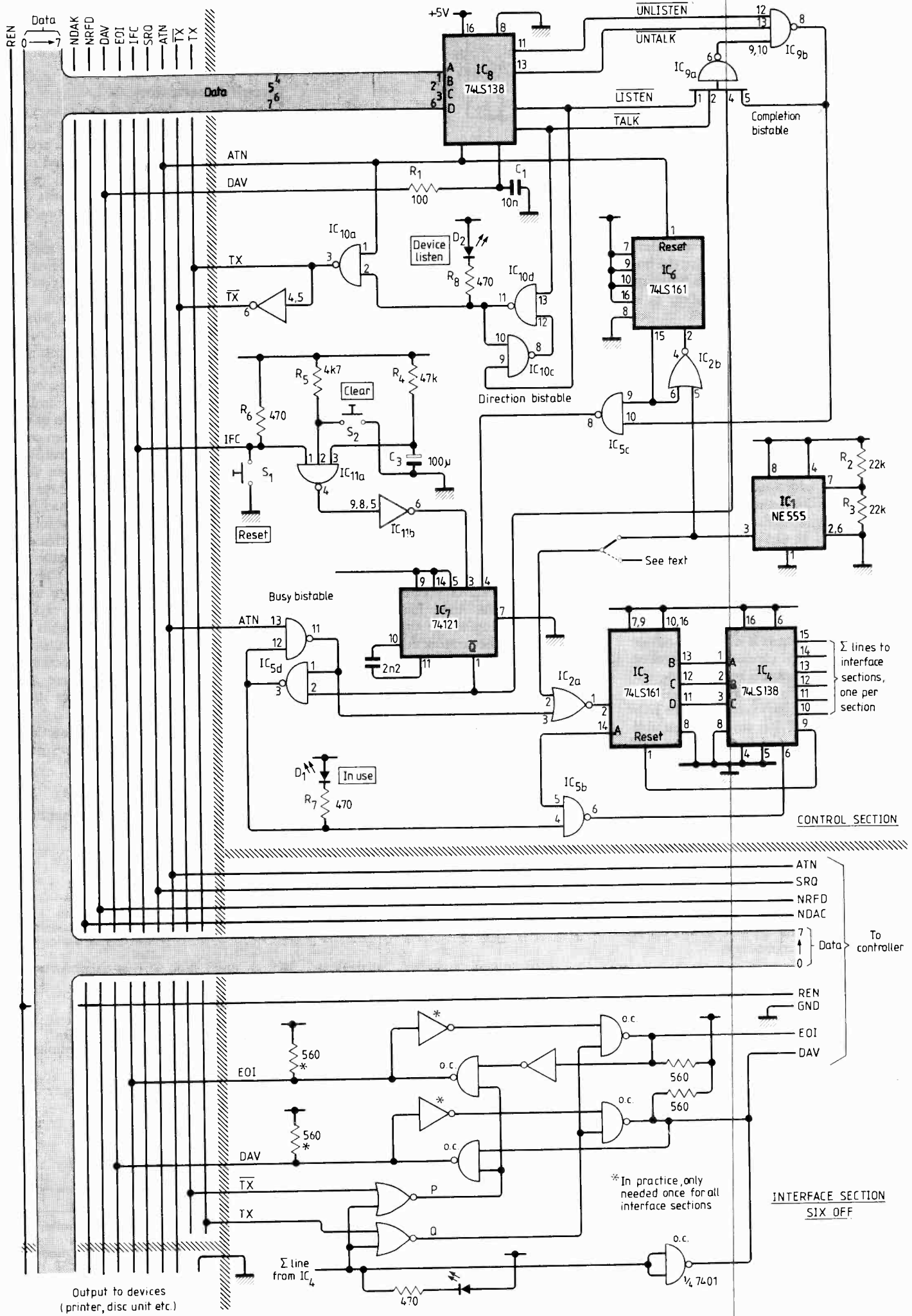
A transaction is the complete sequence of events from leaving to returning to idle mode. Table 2 shows the steps of a typical sequence – the reading of one line from an open disc file or a paper tape reader. Ten separate events have been identified starting in the idle mode at event one. For each event shown, the lines DAV, NRFD and NDAK complete one handshake cycle and the byte shown on DA<sub>0</sub>-DA<sub>7</sub> is transferred from one device to another. The byte on DA<sub>0</sub>-DA<sub>7</sub> is true when DAV (data valid) is low. All transactions start when ATN goes low as in event two.

*Event 2:* the controller puts ATN low to wake up all devices and command mode is deemed to have been entered. All devices have to respond at this point since they do not yet know which of them is to be addressed in the coming transaction. Each device temporarily enters device listener mode (although this is more properly called acceptor handshake).

The controller now sends out a command byte selected from Table 3. In this example the transaction will be data coming from a device to the controller, so the

*Fig. 1. In full circuit of the combiner only one control section is needed but a separate interface section is needed for each user.*





**CONTROL SECTION**

ATN  
SRQ  
NRFD  
NDAC  
Data  
To controller

**INTERFACE SECTION  
SIX OFF**

\* In practice, only needed once for all interface sections

Output to devices  
(printer, disc unit etc.)

upper three bits of the command byte are 010. Since the device number that data is being read from is eight, the other five bits are 01000. This byte is communicated to all devices on the bus using a standard DAV, NRFD and NDAK handshake.

**Event 3:** this event occurs only when a secondary address is needed. Again a command byte is selected from table three, but this time the top three bits are 011. This tells the device that the low-order five bits are the secondary address to be used for the forthcoming data transfer. Only the device which recognized its device number during event two will need the secondary address, but all devices handshake the bus while ATN is still low – they are watching out for their own device number. It is because more than one device can be handshaking the bus at one time that the open collector, wired-or structure is used.

At the end of event three the controller puts ATN high and the remainder of the devices which were not selected return to idle mode.

**Event 4:** since this is an example of a device talking to the controller, the controller is now waiting for the first data byte from the addressed device. It sets up NRFD and NDAK and waits for DAV to go low signifying that the byte is present on DA<sub>0</sub>-DA<sub>7</sub>. If DAV does not go low within a reasonable length of time then the controller can only assume that device eight is broken, switched off or non-existent.

**Events 5-8.** The controller goes on reading bytes for as long as it likes. The device sourcing the data cannot stop sending bytes even if it has run out of data – it must pad with nulls. However it can indicate that it would like to stop with the EOI line. On the CBM Pet the Basic variable ST is set to 64 when an EOI is detected. If the program then continues fetching further data with, say, an INPUT# or GET# statement then ST is set to 2.

**Event 9:** when the controller has had enough data it again puts ATN low to re-enter the command mode. All devices set up NRFD and NDAK in order to receive a command byte. The controller sends 5FH which is the untalk command.

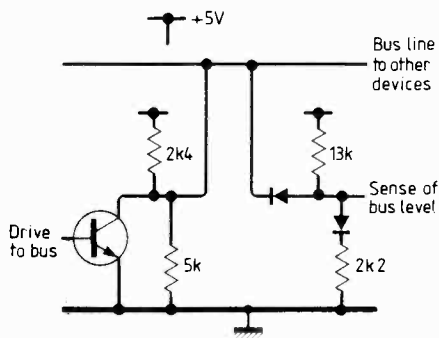
**Event 10:** finally, the controller puts ATN high. All lines are now in idle mode ready for the next transaction.

### Logically connected transactions

Consider the case where a program has been written on the controller to transfer a file from one device to another, one byte or line at a time. This might be the case when listing a disk file on a printer. In the original IEEE488 standard there is provision for such a process to be set up by the controller and run as a single transaction. However, the average user will not bother to consult lengthy texts to find out how to do this. Instead he will write a simple program such as

```
40 INPUT#1,A$
50 PRINT#2,A$
60 GOTO 40
```

This uses two separate transactions for each line of the file and although this is not



**Fig. 2.** Electrical connection used at each device on each line to sense and influence the status of the line.

particularly undesirable, it does cause the bus to pass through idle mode many times during the execution of the program.

From the point of view of the combiner the only way that it can detect that a user has finished with the bus is the presence of the idle mode. However, in this example, the user has not finished and will be immediately submitting another transaction. It is undesirable that another user should interrupt and gain control of the printer (say) during an idle period half-way through the first user's job.

The combiner overcomes this problem by providing a special re-admit period. This is an interval of about 1.5 seconds after a particular user has finished a transaction during which that user alone can submit further transactions. If he has no further work to do then the next controller that is queued is allowed to proceed; or if there is none, the bus becomes free.

There is a disadvantage of the re-admit period: when two users are quite separa-

tely using two peripherals it works out that one of them is continually waiting for a 1.5s gap in the other's transaction stream. Only then can they swap roles.

### Circuit description

The combiner consists of eight sections: six interface sections, one control section and a power supply. The sections are interconnected by an internal bus and most of this bus also leads directly off to the peripheral devices. Figure 1 shows one interface section, the control section and the internal bus.

The interface sections are very simple as all except two of the signal lines from the controller lead directly through it to the internal bus. DAV and EOI are only connected through to the internal bus when a particular interface section is enabled by the control section. EOI must normally be isolated because of a limitation on the early Pet computers. To prevent excessive flicker on the Pet screen when scrolling was taking place, a programmable output pin was connected so that the screen could be blanked, under software control, during scrolling. Unfortunately, when all of the outputs from the computer's three versatile interface adaptors (v.i.as) had been assigned, there was none left to use for this blanking signal. Instead, the pin that controls EOI on the g.p.i.b. connector was used for this purpose as well. The two consequences are that the screen sometimes blanks when using the bus and that the computer produces an extraneous EOI pulse every time the screen scrolls. The EOI half of the interface section is therefore provided to stop these spare pulses from interrupting other users' transactions.

The DAV half of the interface section is provided so that the combiner can pull a

**Table 2.** Typical sequence of bus events making reading up a bus transaction: reading the line BLUE <CR> from device 8, register 4, in this example.

Event	Mode	Control of		Data on DA <sub>0</sub> DA <sub>7</sub>	ATN	EOI	Comments
		DAV, EOI DA <sub>0</sub> DA <sub>7</sub>	NRFD NDAK				
1	idle	—	—	00-all high	high	high	Quiescent state
2	command	controller	all devices	48H	low	high	Controller requests that device 8 should talk
3	command	controller	all devices	64H	low	high	'Secondary address 4'
4	talker	device 8	controller	42H	high	high	Data B
5	talker	device 8	controller	4CH	high	high	transfer L
6	talker	device 8	controller	55H	high	high	U
7	talker	device 8	controller	45H	high	high	E
8	talker	device 8	controller	0DH	high	*	return
9	command	controller	all devices	5FH	low	high	Controller commands UNTALK
10	idle	—	—	00	high	high	

\*If this were the last byte in a file, EOI would be low.

**Table 3.** Command byte meaning

DA <sub>7</sub>	DA <sub>6</sub>	DA <sub>5</sub>	DA <sub>4</sub>	DA <sub>3</sub>	DA <sub>2</sub>	DA <sub>1</sub>	DA <sub>0</sub>	Interpretation
0	1	0	n	n	n	n	n	Cause device nnnnn to go into talk mode
0	1	0	1	1	1	1	1	Untalk command
0	0	1	n	n	n	n	n	Cause device nnnnn to go into listen mode
0	0	1	1	1	1	1	1	Unlisten command
0	1	1	n	n	n	n	n	Use secondary address nnnnn

Note:- 'nnnnn' is a five-bit binary number in the range 0 to 30. Device number 31 is illegal.

**Table 4. Integrated circuit list**

IC	Type	+5V	GND	Usage
1	NE555	8	1	Clock
2	74LS02	14	7	
3	74LS161	16	8	'Which controller?' counter
4	74LS138	16	8	'Which controller?' counter
5	74LS00	14	7	
6	74LS161	16	8	'Re-admit' timer
7	74121	14	7	'End of transaction' monostable
8	74LS138	16	8	Bus command detector
9	74LS20	14	7	Completion bistable
10	74LS00	14	7	Direction bistable et al.
11	74LS10	14	7	

controller's DAV line low without pulling the DAV line of the internal bus low. The interface section holds this low unless it is enabled, in which case it connects it to the internal bus. When a controller wants to use the bus, the first thing it does is to test its DAV line to see if it is high. If the controller finds it low, it sits in a software loop until it does go high. This loop or "hang" is the basis of the combiner's queueing system. Because the interface sections are not normally enabled, when a controller wants to start a transaction it normally finds DAV low and goes into a hang.

Circuit IC<sub>1</sub> in control section is the master clock and runs at a few hertz. Assuming the busy bistable (IC<sub>5a</sub> and IC<sub>5d</sub>) is clear, clock pulses are transmitted through IC<sub>2a</sub> into IC<sub>3</sub>. IC<sub>3</sub> is a four bit counter and is decoded by IC<sub>4</sub> so that the interface sections are each enabled in a "round-robin" fashion. If a particular controller has a transaction ready it will see DAV go high as its interface section is enabled and put ATN low (event 1). ATN is connected to IC<sub>5d</sub> and this sets the busy bistable, stopping IC<sub>3</sub> at its present count.

Some Pet users have effected the facilities provided by this combiner purely by modifying the g.p.i.b. handling software

within their computers. However, this approach has a number of drawbacks, among which is the problem IC<sub>5b</sub> is designed to solve. What can happen is that the software checks that the bus is in idle mode (i.e. not being used) and then starts its transaction with the assertion of ATN. Meanwhile, on another user's machine the same software can be running just a few microseconds further on. Because time must elapse between the execution of the idle mode check and the execution of the instructions which assert ATN, both controllers get the impression that the bus is free and both assert ATN at once. On the combiner described here, there is a safety period of one clock cycle after an interface section has been enabled and then disabled during which the controller can still assert ATN and gain control of the bus.

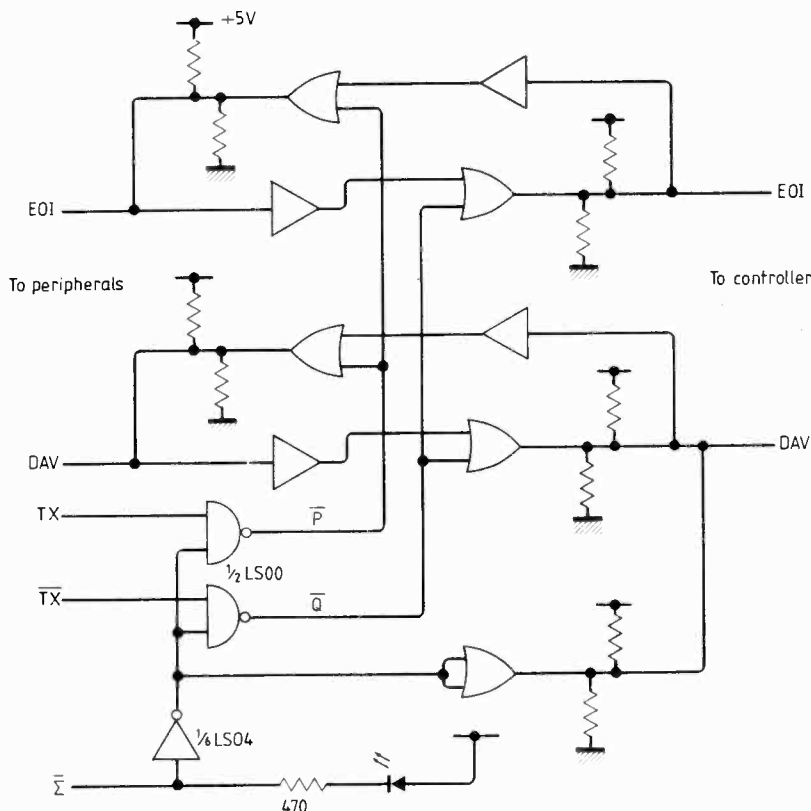
The buffers in the interface sections are bidirectional and need to know whether it is a controller or a peripheral device which is driving DAV and EOI. This information is sent along the TX lines which are controlled by IC<sub>10a</sub> in the control section of the combiner. If ATN is low then it is command mode and the controllers drive DAV and EOI. IC<sub>8</sub> is a 3-to-8 line demultiplexer and provides a simple way of re-

*David Greaves is an engineering student at St John's College, Cambridge. He has designed and built many projects including a digital spectrum analyser and a powerful microcomputer system using three microprocessors. He is currently working on a polyphonic keyboard synthesiser. He is a three times winner of the Design Technology competition sponsored by Esso, a holder of an IEE Jubilee Scholarship and was once a contestant on BBC TV's 'Young Scientists of the Year' programme. An enthusiast for most types of music, he plays the guitar. Other interests include archery, sailing, canoeing and badminton.*

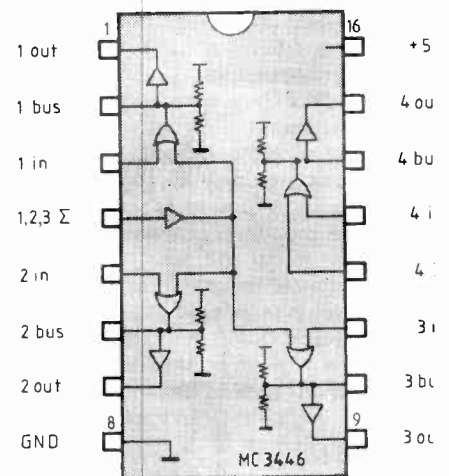
cognizing the command bytes that the controllers send. In fact it is a bit too simple since it does not work with device numbers in the range 16-30! A more complex detector must be used instead of IC<sub>8</sub> if it is desired to use these device numbers. The direction bistable (IC<sub>10c</sub> and IC<sub>10d</sub>) is set depending on whether a talk or listen command byte is detected and when ATN again goes high at the end of the command mode (event 3 in the example) the TX lines take up the information from this bistable.

All the circuitry in the combiner remains passive until the command mode is again entered at the end of the transaction. When either the unlisten or untalk command byte is sent, IC<sub>8</sub> detects it and sets the completion bistable (IC<sub>9a</sub> and IC<sub>9b</sub>). IC<sub>6</sub>, another four bit counter, and IC<sub>2b</sub> together form a retriggerable monostable capable of high duty cycles. Whenever ATN goes low, IC<sub>6</sub> is reset, and when it goes high, clock pulses from IC<sub>1</sub> feed through IC<sub>2b</sub> causing it to count up until it reaches 15. This takes about 1.5 seconds and provides the re-admit period after ATN has gone high and the bus finally returned to the idle mode. If no new transactions are started by the enabled controller during this period, then the completion bistable will still be set and the busy bistable will be cleared. The circuitry which does this is IC<sub>5c</sub> and IC<sub>7</sub>. However,

*continued on page 62*



**Fig. 3.** (a) Alternative circuit for the interface sections using the MC3446 integrated circuit (b) which is specifically designed for use with the g.p.i.b.



## Plymouth satellite tv system bounces back

Despite the setback of being rejected by the Part report, the direct broadcasting by satellite system developed at Plymouth Polytechnic has just been successfully demonstrated. The development team from the Polytechnic's communications engineering department is led by Dr Martin Tomlinson. At the time of the Part report, Dr Tomlinson said "Given the funds, I have no doubt that we could meet the deadline [1986] and offer the UK a system that could put us ahead of the world in satellite tv broadcasting long into the future. Most of the technology required for our system already exists." He has kept his word; funds have been obtained from an undisclosed US source, and the successful test was carried out using a NATO satellite. This makes a nonsense of the Part rejection of the system which found it "elegant and ingenious" but claimed that there was not enough time to meet the deadline. There are two years left for 'fine tuning'.

Part selected the IBA's Multiplexed Analogue Component (Mac) system. A licence to operate two channels of d.b.s. was granted to the BBC, but they have been unable to reach an agreement on standards with other European broadcasters and have virtually abandoned the project.

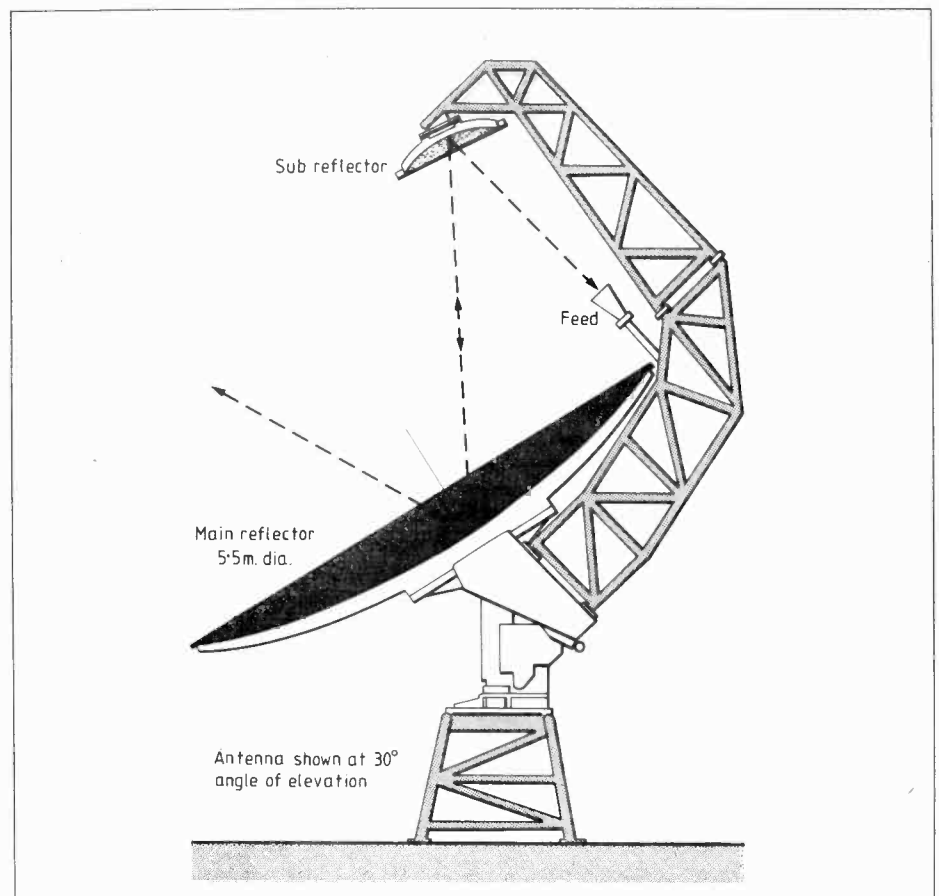
Details of the system were described by Dr. Tomlinson in our issue of January 1983. In essence it separates chrominance and luminance signals and transmits both. Each signal is quantized into sixteen amplitude levels and coded into a digital signal. At the same time an error signal from the quantization process is generated. Sound channels are transmitted separately as a 2Mbit/s stream digital signal and there is an additional 2Mbit/s data stream provided. The luminance, chrominance, sound and any data signals are time-division multiplexed into a composite 60Mbit/s digital stream. The analogue quantization error signals are

also time-division multiplexed and are then phase modulated onto the carrier at a low level along with the digital bit-stream so that analogue and digital components are all transmitted together, using the same carrier. As the analogue modulation is at a low level, no error is caused in the digital information. At the receiver fairly simple demodulating and demultiplexing circuits recover the signals and they are converted back to analogue form with the quantization error signal, used for correction, reimposed on the signals. The system offers, it is claimed, very high bandwidth and signal/noise ratio on both luminance and chrominance with no crosstalk between them. Encryption for subscription tv services may be easily provided. Dr Tomlinson is now confident that this is by far the best system yet devised and has high hopes that it will be accepted internationally.

## Dish antenna allows denser satellite spacing

A smaller dish aerial with an improved performance will enable more countries to use more communications satellites, according to British Telecom, who designed it. The 5.5m-diameter dish is based on the geometry of an optical telescope invented by James Gregory, a 17th century Scottish mathematician, and the design is known as Offset Gregorian. The traditional design of earth terminal aerials has been based on Cassegrain geometry, with a parabolic dish, a convex subreflector and a feed usually placed symmetrically in the centre of the dish. This works well for large, 8m or more, diameter reflectors but the performance falls off as the diameter is reduced. The Gregorian design uses a shallower paraboloid dish, an offset concave subreflector and an offset feed to give a performance at least as good as that of larger diameter Cassegrain aerials.

Placing the subreflector and its supporting structure to one side eliminates the block to power caused by the subreflector. It is possible to achieve a narrower beam with reduced sidelobes. This will become important if plans by Intelsat are put into operation. At present there is a limit to the number of satellites which can be placed in equatorial geosynchronous orbit. A slot is provided every 3° allowing a maximum of



120 positions. The proposal is that the angle be reduced to 2°, creating an extra 60 locations. This would reduce the distance between satellites from 2 200 to less than 1 500km and would require earth station antennae to produce narrower beams to avoid interference between satellites. The new design meets these requirements.

The 14GHz up-link has a 5dB beam width of 0.27°, which means that when it reaches the satellite the beam is only 336km wide. Radiation at angles greater

than 1° from the beam axis is at least 10dB less than from a conventional antenna. The offset design also gives a lower angle of elevation for a given beam angle. In the illustration, the beam angle of elevation is 30° while the dish elevation is only 20°. This helps to reduce wind loadings and makes it less obtrusive. Erected on the roof of a BT building in Ealing, London, the first use of the antenna will be on a transatlantic digital transmission service, Sat-Stream.

## Is European electronics beaten?

"Common Market countries will have to regard each other as friendly partners, rather than foreign threats, if they are to have any hope in catching up with their non-European competitors in the electronics industry," says Ian Mackintosh, head of the market research organization that bears his name. Each nation," he said at a recent conference in Milan, "must create a national strategic plan for electronics, which is fully in tune with the overall interests of the European Community. Only then can the European companies have any hope of fighting back to a position of parity with such competitors.

"Over the last 20 years or so, the electronics industry in Europe has in-

creasingly fallen behind the rapid pace set by companies in the US, Japan and some parts of SE Asia, so that today, with only a few honourable exceptions, Europe's electronics companies are no longer leaders in terms of either market share or innovation."

Dr Mackintosh pointed out that although there were potentially formidable resources of finance and talent, these had been dissipated by management failure and financial caution, compounded by governmental indifference. Looking at a ten-year forecast of worldwide markets and production, he predicted an electronics trade deficit in the European Community of \$16 billion by 1992.

*Operated by voice-entry terminal, microcomputer, disc drive and voice synthesizer, this voice-activated domestic appliance demonstration system cost about £3000 to build, though it is expected that production systems could be sold for under £1000. A vocabulary search is made prior to using the voice print which is built up over a period of training sessions. Initiated by Mal Hyams for the DTI travelling exhibition 'The Concerned Technology', the system was constructed in six weeks by Voice Input Ltd of St Ives, Cambridgeshire.*



## Ultrasonic eye probe

An ultrasonic data imaging and recording system for an eye scanner has been developed at Harwell for use in the Moorfields Eye Hospital. The scanner was originally developed in the mid-70s and has been used in the clinical diagnosis of eye disorders. In operation a low-energy pulsed beam of ultrasound is scanned in a raster movement across the eye; the reflected signals may then be recorded and processed to give an image of the interior of the eye.

The new system can display the images directly on to a standard tv screen and they may be recorded using a standard video recorder. The image processing equipment consists of a dual memory unit through which the captured data is transferred to a temporary store. Subsequent processing involves co-ordinate plotting and transfer of the data to a picture store for manipulation and display. The system makes extensive use of programmable circuits which allow variations of scan and of picture presentation to be made by simple changes in software. It is built around an LSI-11 computer.

A key element of the system is the development of video synchronization techniques which will ensure that the processed data emerges as a genuine video signal, compatible with any standard unmodified v.c.r. This development overcomes the main criticism of ultrasonic inspection methods, that they were very inconvenient to use. The system has applications in industrial non-destructive testing. Indeed it was the NDT Centre at Harwell that developed the system. For on-site testing the raw scanning data can be recorded on a v.c.r. for later processing and display.

## Coax centenary

Just one hundred years ago, Werner Siemens described a new method for constructing an induction-free cable. "It consists of individual conductors covered by a sheath which forms the common return conductor," he wrote to Ludwig Lüffler. The concept was patented in Germany on March 27, 1884, as a solution to the problem of "induction-free cables of lightweight design." It was not until the Berlin Olympic Games in 1936 that a coaxial cable was put to a practical use when a link was set up between Berlin and Leipzig. By using a carrier wave it was found possible to transmit 200 telephone calls and a tv signal simultaneously. Current techniques using an 18-core cable permit the transmission of 100 000 calls and 18 tv signals.

## Repeaters for amateur tv

Licences have been granted for five amateur tv repeater stations to be established in the UK. As they are all set in the 1.2 to 1.3GHz allocation, it is thought that this will lead to a much wider use of the band and preserve it for the amateur service.

Callsign	Location	Channel	Vision freq. (kHz)		Sound freq. (kHz)	
			in	out	in	out
GB3GV	Leicester Bath	RMT-1	1276.5	1311.5	1282.5	1317.5
GB3UT						
GB3TV	Luton Stoke-on-Trent Worthing	RMT-2	1249.0	1318.5	1255.0	1324.5
GB3UD						
GB3VR						

Repeaters on channel RMT-1 will receive a.m. or f.m. signals and retransmit them on a.m. only. RMT-2 channels are likely to be f.m. only. Vision transmissions are 625-line, negative-going video with positive-going synchs. F.m. signals are limited to a 6.5MHz deviation with CCIR pre-emphasis. Sound frequencies shown in the table are for a.m. systems. F.m. systems will contain a 6MHz sound subcarrier. Aerial polarization is horizontal. It is expected that GB3GV, GB3TV and GB3VR are to be operational almost immediately. Further details may be had from the British Amateur Television Club, Telephone: 0533 600108.

## Extra-long play compact disc

A new performance of Beethoven's Choral symphony, lasting 71 minutes, has been issued on one side of a compact disc. Although designed to last for up to 74 minutes, the discs have mostly been made with a playing time of less than one hour. One reason for this stems from the difficulty of achieving precision moulding in the outer areas of the disc (readers will recall that the disc is scanned from the inside outwards). Less-than-perfect mouldings can cause birefringence, a double refraction phenomenon that scatters the light from the pick-up's laser and makes signal detection virtually impossible. The discs are injection moulded from the centre which is why it is difficult to get the right degree of accuracy at the outside edge. Denon engineers at the Kawasaki plant of Nippon Columbia Co. near Tokyo, investigated varying the temperature of the mould and the plastics and also the injection speed and pressure, and adjusting the thickness of the stamper. They believe that this will not only increase the playing time of the digital discs but also increase the overall precision and quality of the recordings.

## Farewell Westinghouse?

A system by which railway train brakes are actuated electrically rather than by air is being tested by British Rail. Proving trials are being held and an electric actuator has been mounted in the bogie of a passenger coach in regular use between London and the West Midlands where it will be subject to all the normal shocks and vibration experienced by rolling stock. The actuator

is being operated against a dummy load and plays no part in the braking of the train. Brake callipers are applied through a large step-down gearbox from a small d.c. electric motor. The motor is powered from a battery which is constantly recharged through the train's power supply. The motor has been designed to withstand the actuating current when in a stalled condition with the brakes applied. As with the air system, invented by George Westinghouse in 1872, a fail-safe approach means that the brakes are automatically applied in the event of a system failure. The electronic control of the system offers a stepped degree of brake pressure, switching a current to the actuator.

The system has worked successfully on the test bench and for 12 000km on a test train so the current experiment is designed to test the longer term durability of the actuator and of the battery charging circuit. A special controller applies and releases the brakes through a series of timed cycles and the currents, voltages and the brake application force are all continuously monitored and recorded.



Despite their problems they can still join a union!

## Save telecom industry say unions

Trades unions in companies manufacturing telecom equipment are joining the British Telecom Union in pressing parliament to adopt key amendments to the Telecommunications Bill that would protect British industry. They see their jobs at companies like Plessey, GEC, and STC as being at risk. The companies themselves have certain misgivings and Lord Weinstock, chairman of GEC, is also pressing for amendments in the House of Lords. The amendments would stop overseas manufacturers selling telecom equipment in Britain while the markets in their countries are not open to British manufacturers. To open the British market to foreign competition without any reciprocal agreement would be catastrophic, according to a spokesperson for the various telecommunication workers unions.

## Videoconference on videoconferences

Appropriately enough, the International Teleconference Symposium, to be held on April 3 to 5, links participants from four continents by satellite. In the first-ever live link-up on such a scale, those taking part will be able to see and hear each other from conference centres in London, Tokyo, Philadelphia, Sydney and Toronto. The London centre will be the Royal Lancaster Hotel, which will be fitted with large projection tv screens. Also at the hotel will be an exhibition of equipment and services. The symposium will be taking full advantage of the digital compression techniques developed in the UK which only transmits changes in a picture rather than the whole frame. The symposium also heralds the transatlantic teleconferencing services which will soon provide a link to Canada and later in the year to the USA. A service within Britain will also commence this year.

# AmPAL – replacement for the NTSC system

Following the decision by the FCC to phase out the current 525/60 NTSC system, American broadcasters have been looking at PAL to see if its colour fidelity can be achieved without the drawbacks of the eight-field sequence. This report – leaked from the working party studying the competing systems – details the system most likely to be adopted.

Since the introduction of the PAL colour broadcast system, it has become clear that it does successfully overcome the major failing of the NTSC system, i.e. sensitivity to chrominance phase errors, but that a penalty is paid in the complexity of broadcast equipment designed to handle it. The major problems with PAL arise because of the quarter-cycle difference between sub-carrier and line frequencies necessary to make up the chrominance spectrum

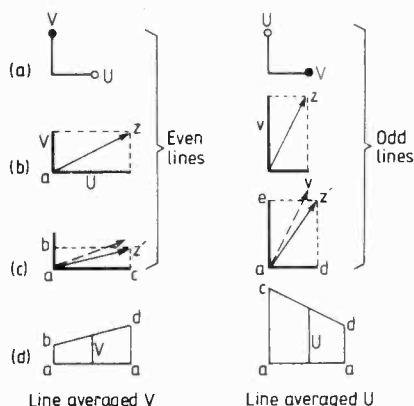


Fig. 1

spreading caused by the V-switch interleave with the luminance sidebands. This causes the PAL structure to have four-line groups of burst phase, whereby the sequence only repeats every eight fields. This causes difficulties in video editing where a four-field edit causes a 180° phase jump in the video, which timebase correctors convert into a picture shift to restore subcarrier phase to reference. A further difficulty is that the original PAL specification did not define the subcarrier H phase relationship, with the result that video tapes from different sources will not colour frame without adjustment to equipment.

The criteria by which the system has been designed are

- colour accuracy as good as or better than PAL
- four-field sequence length maximum
- use as many existing components as possible
- eliminate drop-frame time code.

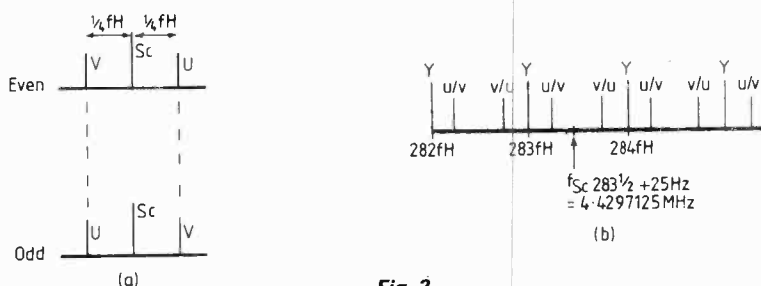
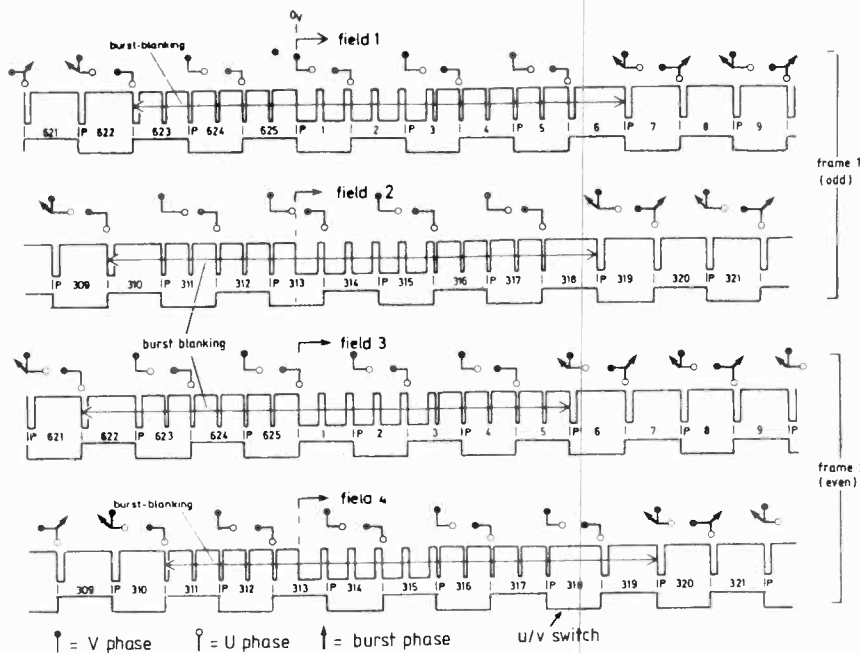


Fig. 2

It was decided that a phase-alternating system was mandatory to equal the PAL colour accuracy and eliminate the NTSC hue control. A novel approach has been used whose performance can exceed that of the PAL system. In AmPAL® the RGB camera signal is converted into the PAL U and V colour difference signals as normal, but the alternating line principle is achieved by interposing U and V on alternate lines. On even lines, U is horizontal in

the phasor diagram and V is vertical, whereas on odd lines V is horizontal and U is vertical (a). Fig. 1(b) shows the resultant phase az as broadcast on successive lines, and (c) shows the signal az' as received with a phase error. This is decoded to ab, on the even line, and V is too small because of the phase error. On the odd line, however, az' becomes ad, and V becomes too large because of the phase error. Line averaging, as in (d), gives an almost correct V signal. Similarly, the line averaging of U gives an almost correct signal. As in PAL, the phase error becomes a saturation error not a hue error.

Fig. 3. Subcarrier phases shown correspond with the AmPAL® definition of subcarrier H phase for video signals recorded on tape.



The saturation error can be calculated from the difference between odd and even line U and V signals, which determines the phase error, and from the U and V signals themselves which determines the desaturation due to the error. It is possible to compute a correction signal which largely eliminates the residual saturation error, which gives this system its superiority over PAL. A custom lsi chip has been designed which includes a digital cosine look-up table to perform the correction at low cost. In urban America with multipath problems caused by skyscrapers and frequent aircraft, the system has been tested and found to give better results from any other.

The result of the U and V interchange is to cause a pair of chrominance sidebands to appear which are at  $\pm \frac{1}{4} f_H$  from subcarrier. These sidebands are alternately

occupied by U and V energy, as shown in Fig. 2(a). Optimum interleaving of luminance and chrominance spectral energy occurs when subcarrier is an odd multiple of half line rate as in (b). The subcarrier is suppressed of course. The result is that, like PAL, there is no energy at half line intervals, but the subcarrier has a half cycle offset, rather than a quarter cycle, so the sequence simplifies to two lines, and repeats every four fields to meet the second criterion, Fig. 3. The actual subcarrier frequency chosen is  $283\frac{1}{2}f_H + 25\text{Hz}$ . The 25Hz term gives cancellation of residual subcarrier on alternate fields.

The 625 line system gives a better balance of horizontal to vertical resolution than 525 lines, and it is proposed to use 625 line transmission. As the current field rate of NTSC, 59.94Hz, is not locked to 60

cycle power, it has been decided that the advantages of 50Hz field rate, i.e. compatibility with European standards, ease of televising movie film, etc., outweigh the improved flicker performance of 60Hz. As 60 and 50Hz have a simple relationship, synchronizing to 60Hz equipment would be easier than using drop-frame time code.

As the line period is unchanged, tv receivers can be made for the new system using existing line output transformers and scan components.

In this election year, the White House anxiously conveys the message that this is a genuine move to improve television quality, since some minority groups are already implying that it will become a rich versus poor issue and are demanding subsidies for low income groups to purchase new receivers. JRW

## Sonic pathfinder continued from page 29

subject moves. Only when he steps through the doorway is the user informed of the existence of the corridor wall. Indeed, it is only then that this information becomes relevant.

After introducing the Clamp it became necessary to reduce the maximum Ratchet hold time to 1.5 seconds.

The existence of the Ratchet and the Clamp will not be perceived by the user during normal use of the Sonic Pathfinder. The various durations used in the algorithms have been chosen to correspond to those involved in human movement. Consequently the user does not, contrary to what might appear to be the case from the above description, experience objects leaping in and out of his perception. There is only one weird side-effect; all objects

disappear if the user walks backwards!

Since the aid uses only readily available components it is capable of being made relatively cheaply; current estimates suggest £50, leading to a final selling price of some £250. The final device would be powered by a 9 volt rechargeable battery and the user would have to plug in the charger for an overnight charge once a week. Training in the use of the aid would be provided by Mobility Officers of which there presently exists some 120 throughout the UK. Current experience suggests that some 15 hours of training will be necessary.

The work described in this paper was funded by the DHSS and carried out under the general supervision of Professor C. I. Howarth. Special thanks are due to the

Unit technician, Carl Espin, who has helped in the assembly of numerous prototypes.

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## GPIB combiner continued from page 28

if a new transaction does start, either a talk or listen command will occur and reset the completion bistable. Then, when the readmit period completes, nothing will happen.

Because the re-admit period and "round robin" polling of the controllers both use similar circuits, there is an average latency of half the re-admit period on all one-off transactions, even if the bus is completely free. To overcome this, on one prototype a second NE555 counter was fitted running at about 150Hz. This was connected into IC<sub>2a</sub> instead of IC<sub>1</sub> thereby increasing the response time. The colossal disadvantage of this is that the pretty display caused by the interface section i.e.d.s flashing in turn is completely lost.

The two push buttons are termed clear and reset. Pushing "reset" generates an interface clear signal (IFC) and resets all devices on the bus. If any old-style Pet disc units are connected then they will need re-initializing. Pushing "clear" is generally a good way to get rid of a "bus-hogger".

### Alternative interface sections

An alternative circuit for each of the six interface sections, Fig. 3(a) uses the

MC3446 integrated circuit of Fig. 3(b). The MC3446 contains four-line driver-receivers specifically designed for interfacing with the bus, their equivalent circuit being exactly as shown in Fig. 1. The driver transistor is guaranteed to sink 48mA and an absolute rating of 150mA is specified.

If very long lengths of cable are to be used, then buffers similar to those already on EOI and DAV can be made up for the other lines of the bus. These extra buffers must still be enabled only when the enable line from the control section is low and must buffer in the correct direction depending on the TX signal. That is, DA<sub>0</sub>-DA<sub>7</sub> always go in the same direction as EOI and DAV, NDAK and NREFD always go in the opposite direction, ATN and REN always go from the controller to the peripherals and SRQ always goes from the peripherals to the controller. IFC is best neglected.

When one user is performing a large transaction such as printing a listing on a printer, other users who are queued and awaiting access to the peripherals may change their minds and decide to do something else that does not use that peripheral. In this case some means of exiting from the queue or "unhanging" their controller is

required. In the case of the Pet computer, pressing buttons on the keyboard is to no avail, the only solution being to unplug the g.p.i.b. connector from the rear of the computer. To reduce connector wear, it may be preferable to fit four pole push-to-break buttons in series with the lines NDAK, NREFD, DAV and ATN. Operation of this switch has the same effect as removing the connector. The controller sees that DAV has gone high, asserts ATN, finds that NREFD and NDAK are both high (an error condition) and aborts its transaction.

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 IEEE bus standard, by P. R. Ellefson, *Wireless World*, June/July 1980, pages 75-78. WWW

## Improving colour television decoding

We regret that David Read's final articles describing a one-line PAL comb decoder have been postponed due to pressure on space. In the meantime you may be interested to read of the new PAL modifications proposed for North America, described on the previous page.



# Digital-storage oscilloscopes

*According to one market study digital storage is the fastest growing segment of the oscilloscope market. In 1982, digital storage represented 13% of the oscilloscope market and is expected to represent 33% by 1987.*

In recent years faster i.c.s have led to the introduction of more and more oscilloscopes using semiconductor memory to store the waveform in digital form. In terms of flexibility, digital-storage techniques offer much more than is possible using an oscilloscope with a storage tube. They also allow extremely slow waveforms to be displayed, and indefinite storage. However, high-quality storage-tube instruments allow persistence of the screen to be varied, they are faster and they generally offer higher resolution. If waveform capture is the only facility required over the functions of a normal oscilloscope, storage-tube instruments can work out cheaper than digital ones; storage tubes and their drive circuits are complex but developments over many years have brought prices down.

## Concepts of digital storage

In the digital storage oscilloscope, an analogue-to-digital converter changes the signal from the input amplifier into binary words which are stored in memory. Some manufacturers call this device a digitizer. The number of binary words produced in a given time – the sampling rate – is governed by an accurate timebase clock signal and determines horizontal resolution of the stored waveform (not necessarily the displayed waveform). This same clock drives a counter which steps through the addresses of memory locations to put each word sampled sequentially in the memory bank.

Vertical resolution of the stored wave-

form is determined by the number of bits in each binary word. Converters used in oscilloscopes are usually eight, nine or ten-bit devices giving a resolution of 256, 512 or 1024 steps respectively. Generally speaking, the more bits the converter has, the longer the conversion time, but there are ways of shortening conversion time by using two converters and sampling them alternately.

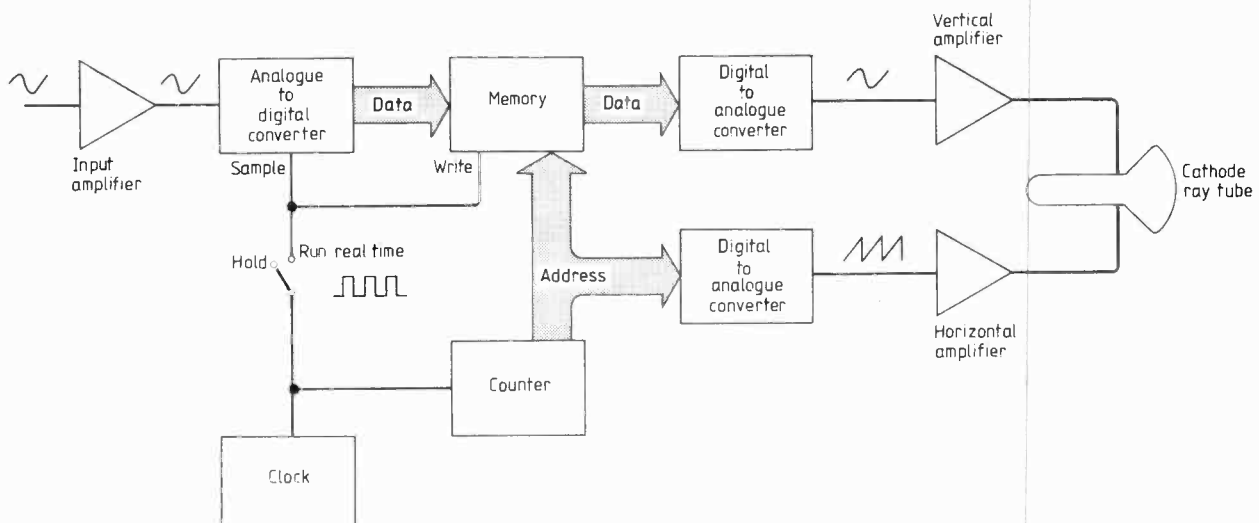
Once in memory, the stored waveform in binary form can be displayed by feeding it to a digital-to-analogue converter to drive the tube vertical amplifier. For each binary word clocked out of memory, a counter driving a further d-to-a converter is incremented. Output of this second converter forms a ramp which drives the tube horizontal amplifier. The waveform only has to be clocked out of memory fast enough to stop screen flicker so these

*Essentials of a digital storage oscilloscope. As shown, the tube drivers, d-to-a converters and c.r.t. would have to be as fast as the input circuits but in practice, the stored waveform only needs to go from memory to the tube fast enough to stop screen flicker. Most digital-storage oscilloscopes use fast tubes and circuits though so that the storage section can be bypassed and the instrument used as a conventional real-time analogue oscilloscope. Waveforms from the a-to-d converters are made up of dots and many instruments use interpolators to join the dots together. Digital-storage oscilloscopes with at least an optional interface for computer control are common.*

converters, the tube amplifiers and the tube need not be high speed unless the oscilloscope has an analogue mode.

In practice, things are usually a lot more complicated than this because processing circuits are invariably included to improve fidelity of the reproduced waveform and the digital circuits lend themselves to the inclusion of many enhancements. Using just a d-to-a converter as described above, the display consists of a number of dots but as frequency of the input signal rises, the dots become further apart. With fast periodic waveforms this can result in a confusing display through a phenomenon called perceptual aliasing, i.e. one's mind tends to join the wrong dots together. About 25 dots for every cycle of a sine wave are needed to present a recognizable display. To avoid this, interpolators are often included to join the dots. Interpolators are optimised to work best with either pulses or sinewaves, not both.

Due to the sampling method, trying to store and display signals at frequencies higher than the time-base setting permits gives strange and misleading results through aliasing. The simplest demonstration of this is to imagine a sine wave being sampled at periods exactly equal to one cycle of the sine wave. All the samples would be exactly the same and the interpolator would produce a tidy straight line. Shift one of the frequencies slightly and the results are even more confusing. To avoid this the sampling rate should always be twice as fast as the highest frequency in the signal. Anti-aliasing filters (similar to





bandwidth limiters but with a higher roll-off rate) may be used but obviously, these obscure part of the signal.

### Triggering

One of the main features of a digital-storage oscilloscope is pre-triggering — the ability to trigger after or in the middle of an event rather than before as is the case with a conventional oscilloscope. Before triggering occurs in pre-trigger mode, the memory is constantly updated with the current input signal. When triggering occurs, the memory is frozen if the pre-trigger is set to 100%, or otherwise allowed to run for a set interval after triggering so the one can see what happened both before and after the trigger point.

There are many unpredictable types of

fault that can be detected by a storage oscilloscope that can't be detected by any other means because of this feature. What happens just before a failure is usually much more important than what happens just after but the failure itself is the only trigger source. Pre-triggering also lets one see the initial section of a transient that is lost on a conventional oscilloscope because of the trigger-level setting and response time.

Digital triggering by setting the trigger level as a binary value and comparing it with the value at the a-to-d converter output is often used. This results in stable and repeatable triggering. Some oscilloscopes allow trigger hysteresis to be set and/or have a bi-trigger mode for use when one is not sure whether the transient to be captured is positive or negative.

### Time base

Being governed by a crystal oscillator, the digital storage oscilloscope's time base is far more accurate than the one found in most conventional oscilloscopes, i.e. one derived from an analogue ramp generator. Short and long-term stability and horizontal linearity are also greatly improved upon through use of a crystal-controlled time base. Some digital oscilloscopes allow the time base to be switched electronically from one setting to another during capture so that part of the waveform may be stored at a higher horizontal resolution than the rest.

### Memory

Size of an oscilloscope's memory is usually expressed in terms of words rather than bytes because many of the converters used

### Digital-storage oscilloscopes

Model	Oscilloscope/ plug-in	Channels	Max sampling rate (MHz)	Resolution (bits)	Memory (Kbyte or words)	Analogue bandwidth (Hz)	Single-shot bandwidth (Hz)	Pre-triggering	Trace expansion horiz./vert.	Stored waveforms	Interpolator	Cursors	Averaging Time/volts display	GPIB	Pen-recorder output RS232	Price £	Reply card number	
<b>Analogue</b> D6000	O	—	—	—	56K	—	—	—	64/512	Many	●	●	●	○	○	6500	Extensive waveform processing facilities, disc drive option	WW500
610	P	2	0.1	14	—	100k	—	●	—	—	—	—	—	—	—	2400	External clock	
611	P	4	0.1	14	—	100k	—	●	—	—	—	—	—	—	—	3255	External clock	
620	P	1/2	100/50	8	—	20M	20M	●	—	—	—	—	—	—	—	6200	External clock	
<b>Farnell</b> DTS12	O	1/2	0.5	8	1K	12M	100k/50k	●	5	2	●	—	—	○	○	825	Analogue mode	WW501
<b>Gould</b> OS1400	O	1	2	8	1K	20M	—	●	10/-	1	●	—	—	—	—	1095	Analogue mode	WW502
OS1420	O	2	2	8	2K	20M	—	●	10/-	2	●	—	—	○	—	1550	Analogue and continuous sampling modes	
5110	O	2	1	8	2K	100M	—	●	—	18	●	●	●	●	—	8400	Microprocessor controlled, menu selection	
OS4020	O	2	2	8	4K	10M	—	●	50/-	2	●	—	—	○	—	2575	General purpose, live and stored trace display	
OS4040	O	2	10	8	5K	25M	—	●	60/-	4	●	—	—	○	—	3980	Automatic operation, trigger window	
OS4200	O	2	0.8	10	4096	—	—	●	50/-	2	●	—	—	○	—	2490	High sensitivity, XY display	
4030	O	2	20	8	2K	20M	—	●	10/-	2	●	—	—	●	—	2290	One converter/channel, stores and expands video waveforms	
4500	O	2	100	8	2K	35M	—	●	Yes	2	●	●	●	●	●	16250	Disc option, d.m.a., one converter for each channel	
<b>Hitachi</b> V6015	O	2	1	8	2K	10M	150k	●	—	2	—	—	—	—	—	1295	Analogue mode, general purpose industrial	WW503
V6041	O	2	40	8	8K	40M	5M/10M	●	Yes	4	●	●	—	○	●	3890	Analogue mode with delay, roll mode for slow waveforms	
<b>Hewlett-Packard</b> 1980	O	2	0.05	10	500	100M	25k	—	—	2	●	●	●	—	—	10949	Extensive waveform-processing facilities, digital plotter output, 4-channel option	WW504
<b>Iwatsu</b> SS5802	O	2	1	8	4K	10M	—	●	—	—	—	—	—	—	—	2095	External clock	WW505
DMS6430	O	2	1.25	8	4K	250k	—	●	64/16	4	●	●	○	●	—	4195	Microprocessor controlled, external clock	
DMS6440	O	2	0.5	12	4096	100k	—	●	64/64	4	●	●	○	●	—	4950	Microprocessor controlled, external clock	
<b>Kikusui</b> DSS6522	O	2	2	8	4K	300k	—	●	100/-	4	—	—	○	●	—	1685	Roll mode for slow waveforms	WW506
<b>Nicolet</b> 4094	O	2/4	—	—	32K	—	—	—	—	256	32	—	—	—	—	4500	Signal processing, optional disc storage and disc maths routines	WW507
4851	P	2	0.1	15	32K	50k	10k	●	—	—	—	●	●	—	—	4950	External clock, bandwidth limiting, time/ point setting, trigger view, data move/ subtract facility, remote control	
4562	P	2	2	12	32K	650k	400k	●	—	—	—	●	●	—	—	3950	Bubble memory option, general purpose portable indust. oscilloscope	
3091	O	2	1	12	8000	300k	200k	●	60	4	—	●	●	○	●	3750	High-speed, features as 4851	
4175	P	2	50	8	32k	100M	10M	●	—	—	—	●	●	—	—	6950	High-speed, features as 4851	
<b>Philips</b> PM3310	O	2	50	8	1K	60M	—	●	2.5/5	4	●	—	—	○	●	3795	Roll mode for slow waveforms, up to 8 traces displayed, tv triggering	WW508
PM3311	O	2	125	8	1K	60M	30M	●	2.5/5	4	●	—	—	○	●	4250	As above	
PM3305P	O	4	2	8	4K	35M	250k	●	/40	4	—	—	—	○	—	2750	External clock, glitch-detection, converter output	
<b>Tektronix</b> 7854	O	2*	0.5	10	1024*	400M	50k	●*	Yes	40	—	●	●	●	—	13050	Extensive waveform processing facilities, wide range of plug-in options	WW509
7D20	P	2	40	8	6K	70M	10M	●	10/5	6	—	●	●	●	—	7661	Extensive waveform processing facilities, control setting storage	
5223	O	4*	1	10	1024*	10M	100k	●*	10/10	4	—	—	—	○	●	4296	Roll mode for slow waveforms, external clock, wide range of plug-ins	
5D10	P	2	1	8	—	100k	100k	●	—	6	—	●	●	—	—	2410	1% accuracy, waveform processing	
468	O	2	25	8	512	100M	10M	●	—	4	●	●	●	○	○	5571	Analogue mode, envelope mode for glitch, frequency drift and aliasing detection	
336	O	2	1	10	16384	50M	140k	●	10/-	16	—	●	●	○	●	3797	General-purpose portable instrument with envelope mode	

\* Depends on plug-in

— Not applicable

● Fitted as standard

○ Optional

# 20MHz + 5mV/Division

## TRIO

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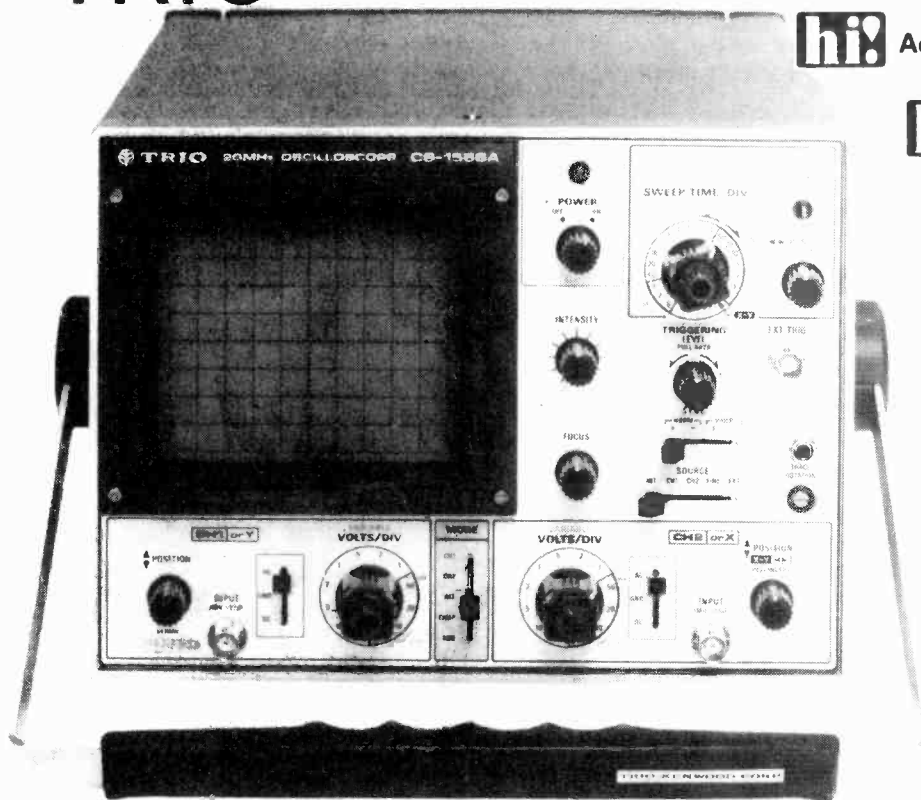
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## EDITORIAL FEATURES

### 1984

ISSUE DATE	PUBLICATION DATE	FEATURE
June 1984	May 16th	Emulators
July 1984	June 20th	2m Transceivers
Sep. 1984	Aug. 15th	Digital Multimeters
Dec. 1984	Nov. 21st	Components Buyers Guide
Jan. 1985	Dec. 19th	Single Board Computers

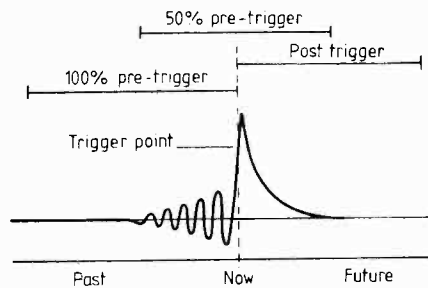
For more details regarding advertising contact **Bob Nibbs**  
01-661 3130

are either nine or ten-bit devices, rather than eight. A 4K-word memory in an oscilloscope using a ten-bit converter is larger than a 4K-word memory in an instrument using a nine-bit converter, or at least it should be.

Memory segmentation is usually possible, which means that more than one waveform can be stored at the expense of resolution (or stored at the same resolution at the expense of part of the waveform depending on how you look at it). Using 512 words of memory to store a waveform means a horizontal resolution of 512 steps which will give a good reproduction of the original waveform when the memory section is displayed in full. The reason why most digital oscilloscopes allow much more memory than this to be used for a single stored waveform is that they invariably have a zoom facility which allows one to look at a part of the waveform in detail.

### Flexibility

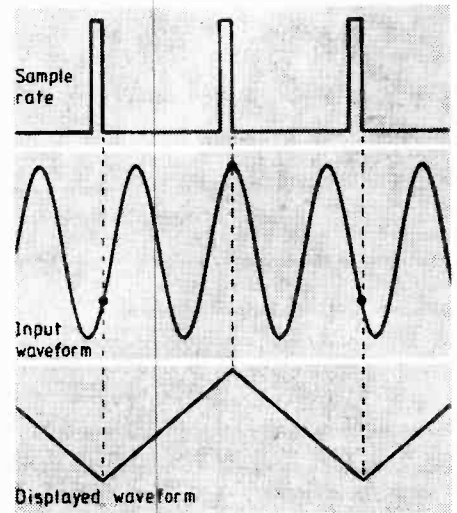
Memory output can easily be converted for viewing on the c.r.t., but it can just as easily be fed to a digital plotter or a computer or a disc drive for permanent storage, provided that the instrument has the right interface circuits and outputs. Digital circuits used for the storage process, triggering and time base also lend themselves to computer control, and hence many digital oscilloscopes have at least an optional GPIB (IEEE488) interface for this purpose



*Digital-storage allows one to see what happened before the trigger as well as after. On triggering in pre-trigger display mode, memory holds information gathered before the trigger so events leading up to say a circuit failure can be recorded using a failure-warning lamp as a trigger.*

### Resolution and accuracy

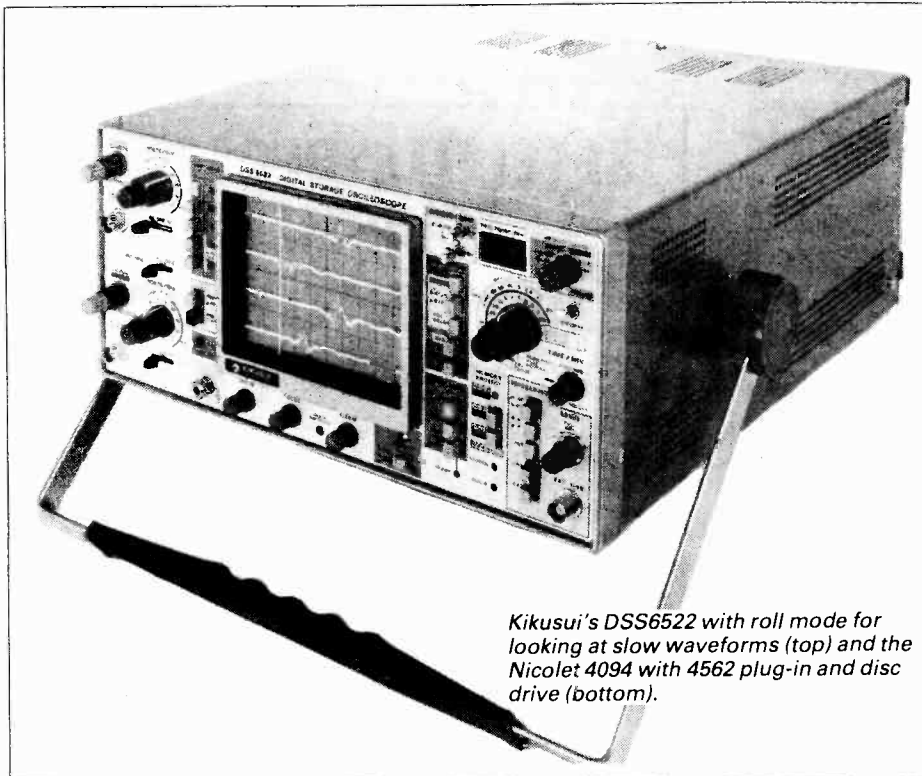
Resolution is not synonymous with accuracy. Imagine a 10V ramp signal driving a 100% accurate eight-bit a-to-d converter and driving the converter binary output word from zero to full scale (255). For each 0.039% increase in the ramp, the binary output value increments by one. If the ramp now represented as a series of binary numbers is converted back to analogue form by a digital-to-analogue converter, d-to-a, it becomes a staircase waveform with 256 steps; lower amplitude input signals give a decreasing number of steps but reso-



*When the speed limit of a digital-storage oscilloscope is approached, false readings are unlike those displayed on a conventional instrument and more difficult to spot unless special features are available. Aliasing occurs when the converter sampling rate is too low for a given frequency component. In the bottom waveform, line interpolation is used to join the dots resulting from a sampling rate which is too slow. One-off and random waveforms suffer most because in periodic waveforms, repeated samples can often be overlaid.*

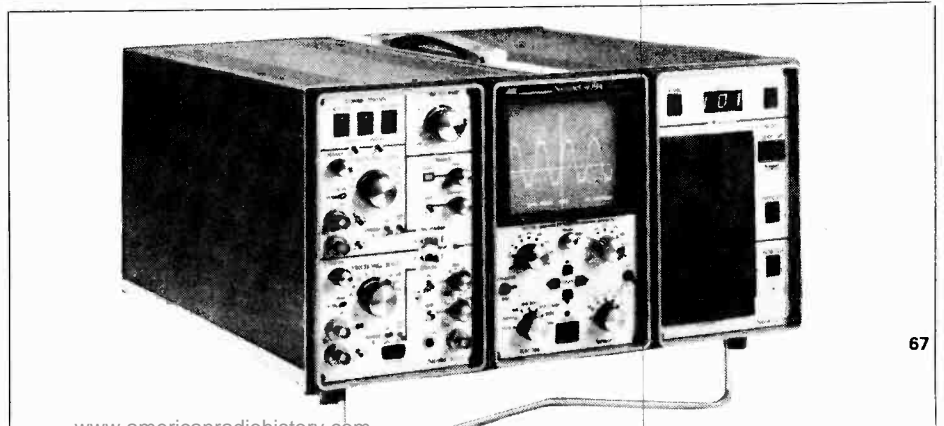
lution remains within 0.39% of full scale. Resolution therefore defines the degree of change in the converter input value that can be represented in the binary output signal.

As far as accuracy is concerned no converter is absolutely linear, even under static conditions. As the rate of change in the input signal increases, linearity worsens and a point is reached where output codes that should appear are skipped. In a digital-storage oscilloscope, the dynamic transfer function of a converter is important in determining the fidelity of reproduction of waveforms which have fast components. Non-linearities and missing codes at various frequencies are parameters well worth looking at. If accuracy was determined by resolution alone, a 10-bit converter would offer an accuracy in the region of 0.1% but in practice, digital storage oscilloscope accuracies are usually in line with similar quality conventional analogue oscilloscopes as far as amplitude measurement is concerned. Cursors used on many digital oscilloscopes though reduce human and parallax errors when making comparisons. WW



*Kikusui's DSS6522 with roll mode for looking at slow waveforms (top) and the Nicolet 4094 with 4562 plug-in and disc drive (bottom).*

— one or two even have built-in disc drives. Computing within the oscilloscope often allows things other than just a waveform to be displayed. Cursors to allow, say sections for zooming or trigger levels to be set are the most basic addition but instruments that display crucial front-panel settings, waveform timing and voltage levels are not uncommon. These readouts are particularly useful if the only means of obtaining hard copy is a camera.



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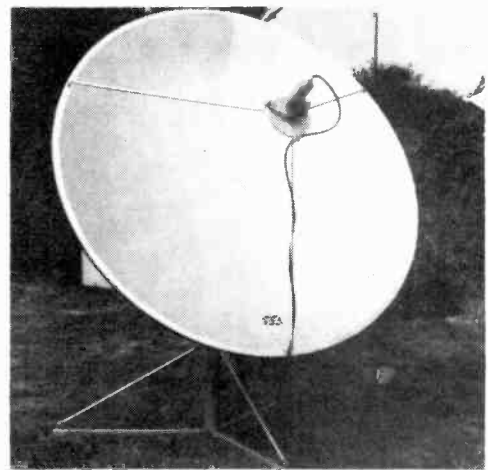
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# NEW PRODUCTS

## Double Forth

One particularly useful feature of the Microkey 4500 computer is that it can accept input from two independent keyboards and display the results on two monitors. This means that for program development or for text manipulation it acts as two computers. The ability to drive two monitors can have many uses. For example it is possible to have one screen displaying a control program while the other shows the results. The computer is based around the 6502 processor but may be alternatively fitted with a 6809 with no hardware modifications. In this configuration it can run the Flex operating systems. An add-on 68000 second processor extension is planned.

The 'native' language for the computer is an extended combination of Forth-79 and FIG-Forth with an assembler and a screen editor. Being developed is a Logo-type extension to Forth, a database system and a power systems engineering package. Through Flex a number of other languages may be used including Pascal and C.

Some clever techniques are employed to make maximum use of ram. Screen information may be written to the video display memory which occupies the same memory area as the rom which may be accessed during a read cycle; thus the video ram is 'invisible' to the user. All 128K ram and 32K rom may be accessed to allow maximum use of the memory, though the ram may also be divided into two distinct areas of 64K each for the two-user mode.

High-resolution graphics are possible with 640 by 200 elements in 16 colours. In monochrome, it is possible to produce 1280 by 200 dots. There are three bidirectional parallel ports and a full RS232 communications port as well as an expansion bus using a similar pin-



out to Apple computers. One or two Sony 3.5in disc drives may be fitted into the computer and up to two more may be added. A Winchester drive will be available.

The designers see their computer being of most use in educational, industrial, scientific and medical fields and are willing to offer a wide variety of hardware and software configurations to suit specific applications. The basic system without a monitor or disc drive (but including a disc interface and a high-quality professional keyboard) costs £650. Microkey Ltd, 98a St James Street, Brighton, Sussex, BN2 1TP.

WW301

## More than a multimeter

Claiming to offer more measuring facilities than any multimeter, the Philips PM2519 is called a 'digital measurement centre'. Apart from all the volt, ohm and amp measurements with an accuracy of 0.1%, it includes a counter to measure frequency up to 1MHz, dB may be measured on both a.c. and d.c. voltage ranges, and there are 16 reference values built in to provide relative measurements.

Included in the display is

logarithmically scaled bar graph which indicates some digitally displayed values, providing a virtual analogue display for the easy setting of null values. The bar graph may also be used in the relative reference mode, enabling rapid and simple adjustment to a specific value, held in the internal non-volatile memory.

The PM2519 has a self-test facility and in the event of a fault, the built-in signature analysis fault finding technique ensures fast detection and repair. The meter is available in two versions; with an IEEE488 interface bus to enable computer-controlled testing at £495, or without for £285. A battery back-up pack is available to make the instrument fully portable. Pye Unicam Ltd, York Street, Cambridge CB1 2PX.

WW302

## Build your own computer

A high-resolution-display computer, based on the MC6809E, is a British design from Micro Concepts of Cheltenham. The Microbox offers a minimal cost approach so that functions may be added as required. But the designer stresses that this is a 'no compromise' approach which equals or even exceeds the capabilities of the best personal computers. These include 60K of main system ram, disc controller for two 5.25" 40 or 80-track drives, two RS232 ports, a Centronics printer port and a parallel keyboard input port. An additional 128K ram is reserved for display and for 'silicon disc'. The ram-based silicon disc looks to the system like a conventional floppy disc with a capacity equal to a 40-track single-sided, single density disc; however the access time is a lot faster. The same principle is applied to the rom area; eprom cartridges, called 'discs' in this context, will accept up to four 8, 16, 32 or 64K eproms

each, up to a maximum of 256K. These slot into a port that is fully buffered and isolated so that the rom discs may be changed while the system is powered. A built-in eprom programmer is included in the design.

The display offers several alphanumeric formats including 108 columns by 24 lines and 128 columns of 72 lines. Use of the NEC 7220 graphics controller chip gives a 768 by 576 element display with high-speed drawing through the inbuilt vector generation. Such facilities as points, lines, rectangles, circles, arcs and the ability to fill an area are provided.

For disc operation, the Flex system was selected because it is hardware independent and a considerable range of software is already available. Implementation is taken care of by the auto-configuring boot program which is included in the supplied system support monitor so there is no need for any knowledge of hardware or software to get the system going. This 8K rom contains all disc, console and graphics drivers plus 27 diagnostic and utility commands.

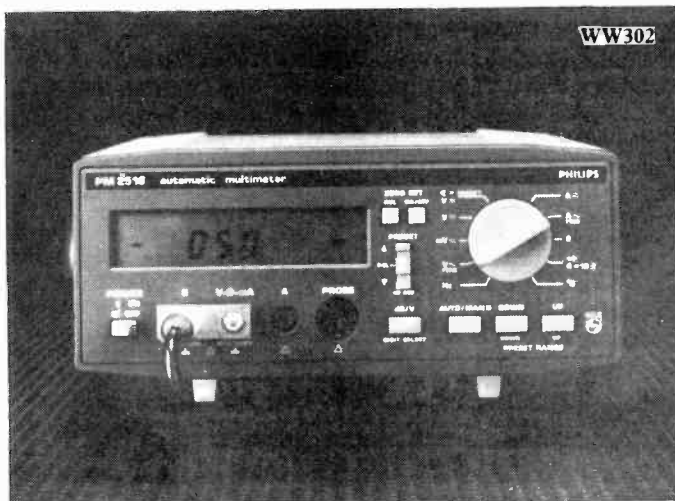
The start-up kit consists of a bare through-hole plated p.c.b. measuring 305 by 241mm, a 76 by 100mm eprom carrier board, the system support eprom, system utilities on a 5.25in disc, constructional notes, operational documentation, and a list of components and suppliers. All for £95 from Micro Concepts, 8 Skillicorne Mews, Queens Road, Cheltenham, Glos GL50 2NJ.

WW303

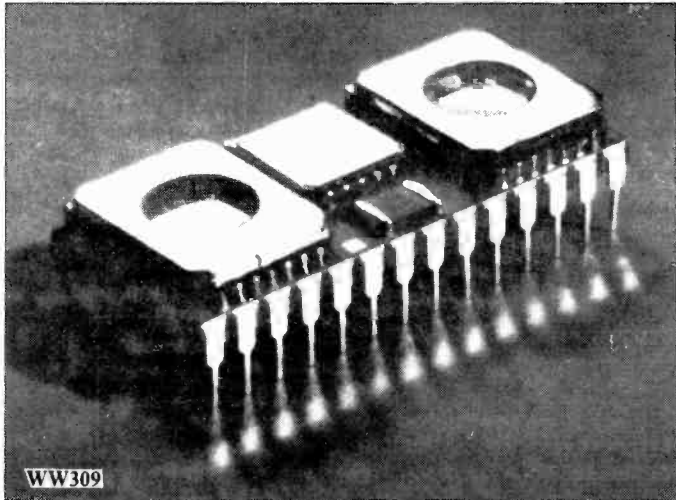
## Commodore enhancement

A plug-in rom for the Commodore 64 home computer adds nearly 100 Basic commands to its operation. Particular areas of improvement are in the high resolution display facilities, the organization of sprites, colour text displays, sound commands have been improved to give synthesizer capabilities. There are many new commands to improve the ability to program in machine code and to give the Basic more of a structured approach. Input and output control has several new commands and there are many others. One of the criticisms of the Commodore 64 has been its inadequate Basic and this toolbox addition seems to be very useful in correcting this. Known as BC Basic, the rom comes with an 82-page manual for £57.50 (inclusive) from Kuma Computers Ltd, Unit 12, Horseshoe Park, Pangbourne, Berks RG8 7JW.

WW304



# NEW PRODUCTS



WW309

## Massive Eprom

By combining a number of eprom chips onto a ceramic substrate, it is possible to get eproms with up to 256Kbits of storage into a standard d.i.l. package. Included on the substrate is decoupling capacitors and decoding to provide the configuration so that externally it behaves as a single unit with pin functions conforming to JEDEC standards. 32Kbyte versions are available in n.mos and c.mos, with a 16Kbyte version in c.mos only. A 16K by 16 version will become available soon. Electronic Design Europe Ltd, Shelley House, The Avenue, Lightwater, Surrey GU18 5RF.

WW309

## Single-chip modem

A single-chip c.mos f.s.k. modem has been produced by TI. It incorporates filters which conform to the CCITT V23 standard, having a transmit modulation at 75, 150, 600 or 1200baud and receive demodulation at 600 or 1200baud. It offers full duplex operation up to 1200baud receive and 1500baud transmit or half duplex at 1200baud both ways. It operates from a single 4 to 6V supply with a consumption of only 30mW and is ideal, according to Texas, for communications by telephone between home/personal computers, intelligent terminals, credit card readers, viewdata terminals etc. Texas Instruments Ltd, Manton Lane, Bedford MK41 7PA.

WW310

## Video filters

A range of 22 filters from Barr & Stroud has been designed to cover all known current requirements for both analogue and digital video processing applications. The range consists of nine luminance low pass filters, four chrominance low pass, three luminance/chrominance YUV filter combinations, four sub-

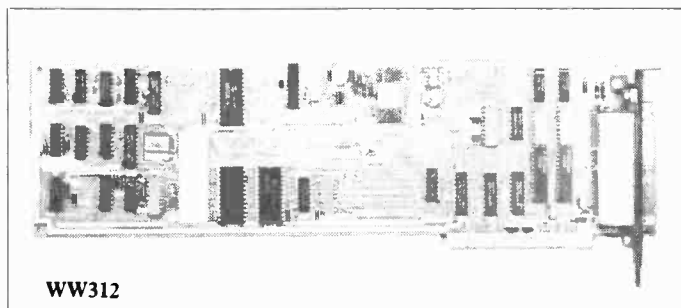
carrier band pass and two sub-carrier band stop filters. The sub-carrier filters, used to isolate the chrominance and luminance information in colour tv systems, are available in NTSC and PAL versions. In addition to the standard range, the manufacturers are willing to provide a made-to-measure service. Barr & Stroud Ltd, Melrose House, 4 Savile Row, London W1X 1AF.

WW306

## A and D i/o board for IBM PC

A single board containing both analogue and digital inputs and outputs is available for the IBM personal computer. Costing £495 (less in o.e.m. quantities), the DT2808 includes an on-board prammable clock and its own processor. It provides 16 channels of a-to-d with 10-bit resolution and two channels of d-to-a with 8-bit resolution, there are also 16 lines of digital i/o. The board is intended for use in industrial control, data logging, product testing, and quality assurance. Energy management and security systems are also among the applications.

The on-board processor acts as interface between the board and the host computer. It controls all the i/o functions on the board and includes self-test functions it may be programmed through its internal microcode, or through a special software package available from the manufacturers, Data Translation



WW312



WW306

Ltd, 430 Bath Road, Slough, Berks SL1 6BB.

WW312

## Connect 36

Strips of 0.025in square pins and receptacles, made in straight and right-angular form have beryllium copper contacts. With a standard 0.1in pitch, the makers say that they are ideal for mother/daughter module connectors. They come in standard lengths of 36 connectors and are notched to break off a desired length. Robinson Nugent Ltd, 74 London Road, Riverhead, Sevenoaks, Kent.

WW313

## Polyester decoupling

A new range of metallized polyester 5mm-lead-pitch capacitors has been designed to replace the more expensive multi-layer ceramic types used in decoupling. The small size allows high density packing on a p.c.b. and with this in mind the makers have printed the value, from 100pF to 1.0µF, on the top for easy identification. Leads are ready-cropped and are provided with mounting 'feet'. Suffix Ltd, Risca, Newport, Gwent NP1 6YD.

WW314

## Reference diode

A 2.5V reference diode offers a tolerance of 5mV or 0.2%. The LT1009 is a precision trimmed shunt regulator diode, with a temperature drift of less than

25ppm/°C. It operates over a wide current range; from 400µA to 10A, with a dynamic impedance of 0.6Ω. A third terminal is supplied to allow the reference voltage to be altered by 2% to calibrate out any system errors. Dialogue Distribution Ltd, Watchmoor Road, Camberley, Surrey GU15 3AQ.

WW315

## Spectrum interface

A printer interface for the Sinclair ZX Spectrum includes both RS232 and Centronic interfaces. It is able to implement the Copy command which allows the printing of a high resolution screen image. This is available for a number of popular printers including Epson, Star and Seikosha and will give a full colour image with the Seikosha GP700 printer. The ZX Lprint III costs £34.95 inclusive from Euroelectronics, 26 Clarence Square, Cheltenham, Glos GL50 2UJ.

WW316

## Ribbon-cable cutter

The KT80 ribbon-cable cutter is made from steel with plastics-covered handles. It has a hollow ground hardened steel blade which is provided with a toggle-lever action so that all conductors are cleanly cut at the same time. The g.r.p. anvil has a built-in guide to ensure that a cut is made at right angles. The blade and angle are replaceable and spares are included. Klippon Electricals Ltd, Terminal Works, Power Station Road, Sheerness, Kent NE12 3AB.

WW317

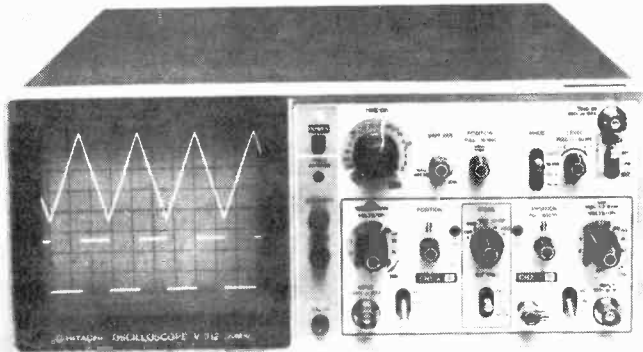
*If you would like more information on any of the items featured here, enter the appropriate WW reference number(s) on the mauve reply-paid card bound in this issue. Overseas cards require a stamp.*





# Hitachi Oscilloscopes

## performance, reliability, value and immediate delivery!



Hitachi Oscilloscopes provide the quality and performance that you'd expect from such a famous name, with a newly-extended range that represents the best value for money available anywhere.

V-212	20MHz Dual Trace	V-209	20MHz Mini-Portable
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V-203F	20MHz Sweep Delay	V-1050F	100MHz Quad Trace
V-353F	35MHz Sweep Delay	V-134	10MHz Tube Storage
V-422	40MHz Dual Trace	VC-6015	10MHz Digital
V-650F	60MHz Dual Timebase	VC-6041	40MHz Digital

Prices start at around £300 plus vat including 2 probes and 2 year warranty. We hold the range in stock for immediate delivery.

For colour brochure giving specifications and prices ring (0480) 63570  
Thurlby-Reltech, 46 High Street, Solihull, W. Midlands, B91 3TB

WW - 033 FOR FURTHER DETAILS

## Add 8 channels to your 'scope New Thurlby OM358 multiplexer £169+vat

The Thurlby OM358 gives any oscilloscope an 8 channel display. Observing many waveforms simultaneously can be essential when analysing sophisticated equipment. Application areas include microprocessor based products, data transmission systems, A to D converters, frequency synthesizers etc. The OM358 is ideal for digital equipment (it can often solve problems that would otherwise need a fast logic analyser) but, unlike dedicated logic test instruments, it is equally suited to analogue waveforms. The OM358 has a bandwidth of 35MHz and 3% calibration accuracy. Each input has an impedance of  $1M\Omega - 20pF$  and accepts signals up to  $\pm 6V$ . An 8 channel, 4 channel, or single channel display can be selected with triggering from any channel. *Colour data sheet with full specifications available.*

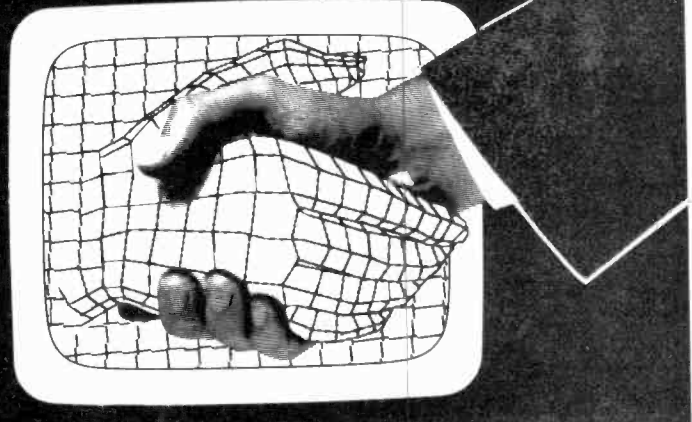


Thurlby Electronics Ltd  
New Road, St. Ives, Cambs.  
PE17 4BG Tel: (0480) 63570

OM358 with two BNC  
cables £197.80  
(inc P & P and VAT)

WW - 022 FOR FURTHER DETAILS

# Where business is making contact



For the communications industries worldwide, the United Kingdom is currently a focus of attention.

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Once again, the latest presentation of this established event has attracted hundreds of companies - from the world over - who market communications products and services.

They are there to discuss how their organisations can help your business.

Whatever aspect of communications is your concern, you can view and compare the alternatives - comfortably, cost-effectively and conveniently under one roof.

Attend the associated conference too, and add further to the value of your visit.

The time and place are right, so make a date. Communicate with the communicators at COMMUNICATIONS 84.

15-18 May 1984 National Exhibition Centre  
Birmingham, England



Communications 84 is organised by Industrial & Trade Fairs Limited, Radcliffe House, Blenheim Court, Solihull, West Midlands B91 2BG  
England ☎ 021-705 6707 Telex 337073

## Communications 84

INTERNATIONAL EXHIBITION OF TELECOMMUNICATIONS, RADIO AND INFORMATION TECHNOLOGY PRODUCTS AND SERVICES.

Please send me the **visitor information pack** for COMMUNICATIONS 84, which includes details of the conference programme, easy travel arrangements, and free registration card for the exhibition.

Name \_\_\_\_\_ Company \_\_\_\_\_

Address \_\_\_\_\_

Complete and send to Department PS1 at the address shown. WWW2

WW - 014 FOR FURTHER DETAILS

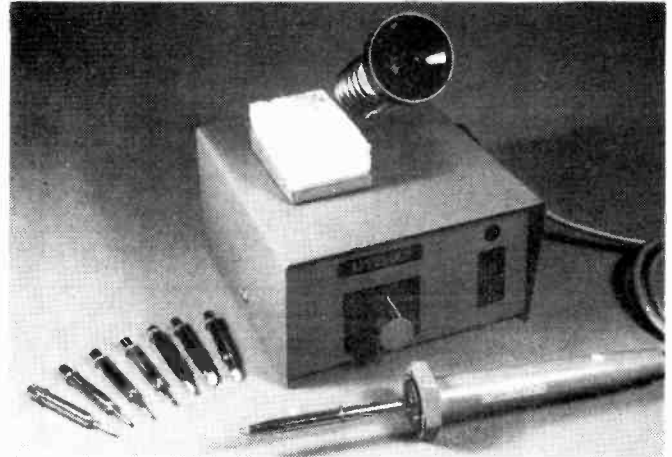
# Temperature-Controlled Soldering? LITESOLD have it-to a Degree!

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Using a special 5-transistor and op. amp. circuit, the power unit provides a controlled low-voltage dc supply to the plug-in lightweight soldering iron, in response to a thermocouple sensor located inside the bit. Spiking, RFI, hum and magnetic effects are totally avoided. The metal power unit case and the soldering iron shaft are earthed for screening and static elimination.

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Soldering irons are interchangeable without re-calibration and are simple and inexpensive to



service. Burnproof 4-wire leads are fitted and non-seize iron-plated bits are available in 16 shapes/sizes. So get your degree in temperature-controlled soldering — with LITESOLD.



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## LIGHT SOLDERING DEVELOPMENTS LTD

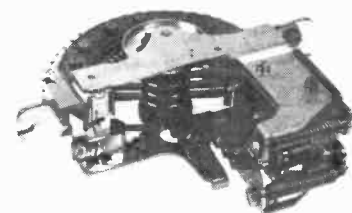
97/99 GLOUCESTER ROAD, CROYDON, SURREY CR0 2DN. TEL: 01-689 0574. TELEX: 8811945

WW - 058 FOR FURTHER DETAILS

TRANSFORMERS EX-STOCK				INVERTERS			
<b>MAINS ISOLATORS</b>				<b>12/24V DC in. 240V 13A</b>			
Pri/Sec 120V x 2				Skt. AC out. Cont. Rated			
VA	Price	P&P		100W	£57.00		
*20	5.82	1.60		250W	£157.36		
60	9.49	1.80		500W	£235.50		
100	11.08	2.00		1000W	£341.00		
200	15.69	2.25					
250	18.97	2.64					
350	23.47	2.70					
500	29.23	2.95					
750	41.28	3.70					
1000	53.00	4.00					
1500	68.37	4.70					
2000	82.27	5.10					
3000	115.35	OA					
6000	203.65	OA					
*115 or 240V sec only							
<b>400/440V ISOLATORS</b>				<b>CONSTANT VOLTAGE TRANSFORMERS</b>			
400/440 to 200/240V CT				Spoke-free stable mains			
VA	Price	P&P		120VA	£148		
60	9.50	1.80		250VA	£172		
100	11.08	2.00		500VA	£193.69		
200	15.68	2.25		1kVA	£336.40		
250	18.97	2.40		2kVA	£594.50		
350	23.47	2.70		5kVA	£1587		
500	29.23	2.95					
750	41.28	3.70					
1000	52.98	4.00					
2000	82.27	5.00					
3000	115.37	OA					
6000	228.75	OA					
<b>24/12V or 12-0-12V</b>				<b>AVOs &amp; MEGGERS</b>			
2x12V Secs. Pri. 240V				8 Mk5 (latest) £140.70			
12V	24V	Price	P&P	73 £78.90			
0.3A	15	2.41	90	MM5 Minor £52.00			
1	5	3.19	1.20	DA212 LCD £98.60			
2	1	4.25	1.20	DA116 LCD £154.50			
4	2	4.91	1.60	DA117 Autorange £157.00			
6	3	7.69	1.60	Megger Gen £116.40			
8	4	8.98	1.60	Batt Megger £85.50			
10	5	9.82	1.80	AVO 2001 £91.60			
12	6	10.89	1.90	P&P E2 VAT 15%			
16	8	12.97	2.12				
20	10	17.46	2.44				
30	15	21.69	2.64				
60	30	44.45	OA				
83	41	51.20	4.50				
<b>96/48V Pri x 120V</b>				<b>TOROIDALS</b>			
Secs 2 x 36 48V				Wound to order. Fast deliveries. Small batches 10-14 days.			
72-96	36-48V	Price	P&P				
0.5A	1	5.37	1.20				
2	4	14.69	2.20				
3	6	17.79	2.40				
5	10	32.23	3.20				
6	12	40.36	3.50				
8	16	44.03	3.75				
<b>24-0-24V or 25-0-25V</b>				<b>CASED AUTOS</b>			
2x25V Tap Secs. 5, 7, 8, 10, 13, 15, 17, 20, 25, 30, 33, 40, 20-0-20 or 25-0-25V				240V to 115V USA skts.			
50V	25V	Price	P&P	VA	Price	P&P	
0.5	1	4.13	1.40	20	7.21	1.50	
1	2	8.69	1.84	80	9.35	1.60	
2	4	10.36	1.90	150	12.10	1.90	
3	6	14.10	2.12	250	14.73	2.00	
4	8	18.01	2.20	500	22.14	2.20	
5	12	24.52	2.70	1000	33.74	2.80	
6	16	30.23	3.00	2000	55.74	2.80	
8	20	36.18	3.20	3000	60.47	4.50	
10	24	36.18	3.20	5000	108.30	OA	
<b>30/15V or 15-0-15V</b>				<b>RESISTORS</b>			
2x15V Tap Sec. Volts				ELECTROSIL TR4 5%			
3, 4, 5, 6, 8, 9, 10, 12, 15, 18, 20, 24, 30 or 15-0-15V	30V	Price	P&P	12, 20, 33, 47, 75, 390, 430, 510Ω, 560, 1k, 1k1, 1k3, 1k6, 1k8, 2k, 3k, 3k9, 5k6, 16k, 24k, 27k, 39k, 56k, 82k, 100k, 110k, 120k, 130k, 150k, 200k, 220k, 270k, 300k, P&P 20p			
0.5A	15V	1.39	1.20				
1	2	4.32	1.40				
2	4	6.99	1.60				
3	6	8.10	1.65				
4	8	9.67	1.90				
5	10	11.95	2.00				
6	12	13.52	2.00				
8	16	18.10	2.26				
10	20	20.88	2.26				
12	24	23.20	2.50				
15	30	26.60	3.00				
20	40	35.64	4.83				
<b>400/440V ISOLATORS</b>				<b>CUSTOM WINDING SERVICE</b>			
400/440 to 200/240V CT				3VA-15KVA Single & 3 phase Fast deliveries. Prototypes 7/10 days			
VA	Price	P&P					
60	9.50	1.80					
100	11.08	2.00					
200	15.68	2.25					
250	18.97	2.40					
350	23.47	2.70					
500	29.23	2.95					
750	41.28	3.70					
1000	52.98	4.00					
2000	82.27	5.00					
3000	115.37	OA					
6000	228.75	OA					
<b>24-0-24V or 30-0-30V</b>				<b>EXPORT ENQUIRIES WELCOMED</b>			
Pri 2x120V. 2x30V Tap Secs 6, 8, 10, 12, 16, 18, 20, 24, 30, 36, 40, 48, 60, 24-0-24 or 30-0-30V				<b>PLEASE ADD 15% VAT TO ALL ITEMS AFTER P&amp;P</b>			
60V	30V	Price	P&P				
0.5	1	4.70	1.50				
1	2	7.15	1.50				
2	4	9.20	1.90				
3	6	13.31	2.00				
4	8	15.15	2.20				
5	10	19.16	2.20				
6	12	21.86	2.65				
8	16	30.72	3.00				
10	20	35.76	3.30				
12	24	41.22	3.50				
<b>MINIATURES</b>				<b>BARRIE ELECTRONICS LTD</b>			
Sec V	A	Pri	P&P	<b>Unit 211, Stratford Workshops</b>			
3-0-3	2A	3.11	90	<b>Burford Road, London E15 2SP</b>			
6x2	1A x 2	3.45	1.20	<b>Tel: 01-555 0228 (3 lines)</b>			
9-0-9	1	2.59	90				
9x2	3x2	2.41	90				
8.9x2	5x2	3.36	1.20				
8.9x2	1A x 2	4.27	1.40				
15x2	2A x 2	4.27	1.40				
12-0-12	0.5	3.11	90				
20x2	3x2	3.39	1.20				
20,12,0	9	4.13	1.30				
12,20	1A x 2	5.60	1.60				
15,20-2	5x2	4.83	1.40				
15,27x2	3x2	4.83	1.40				
15,27x2	1A x 2	7.30	1.60				
<b>SPLIT BOBBIN</b>				<b>WW-6</b>			
PC or CLAMP. MTG. PRI 2x120V Twin Secs. 4.5V, 6, 7.5, 9, 12, 15V Ratings 1.5VA, 3, 6, 9, 12, 25VA							

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## UNISELECTORS TYPE 2 SERIES



Uniselectors are designed to meet the requirements for mechanisms having long life and dependability. They are approved by British Telecom and used extensively by them.

Uniselectors can be supplied with double-ended wipers giving two appearances of 25 points per revolution. 4, 6, 8, 10 and 12 level uniselectors can also be supplied with single-ended wipers, connected in adjacent pairs which give 2, 3, 4, 5 and 6 complete circuits of 50 points per revolution respectively. Wipers may be bridging or non-bridging and can be adjusted for position on bank contacts independently of mechanism adjustments.

Also in stock: Miniature Uniselectors, 3000 Type Relays, Carpenter Polarised Relays, High Speed Relays, Transformers, 2000 and 4000 Type Selector Mechanisms, etc.

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Telecommunication component factors  
Unit 3, Argyle Way, Stevenage, Hertfordshire SG1 2AD  
Telephone (0438) 352497/352326. Telex 825617

WW - 067 FOR FURTHER DETAILS

# WHAT RESOLUTION FOR ONLY £230. (EX. VAT)



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That's a bargain we guarantee you won't see from any other micro retailer.

We've managed to acquire the sole distribution rights enabling us to offer these superb monitors at this unbeatable price.

And just because you're saving on price doesn't mean you're sacrificing quality. Here's what Personal Computer News had to say about our monitors.

**"There is no doubt that the JVC range of ECM colour monitors is excellent value for money... there is no loss in quality of picture after long periods... remember as more and more resolution is available with new micros, the need for a better display will be that much greater."**

For those who only require medium resolution we also have a model (370 × 470 pixels) at £149.95 (excluding VAT) which is equally excellent value for money.

Both units have a 14" screen and are suitable for the BBC Micro, Spectrum QL, Lynx, Oric, Apple, IBM and

most other leading micros.

And naturally there's a years full guarantee.

Another one of our commitments is to make certain we deliver your monitor by courier within ten days of receiving your order.

You can order by filling in the coupon below and posting to: Opus Supplies Ltd., 158 Camberwell Road, London SE5 0EE. Or by telephoning 01-701 8668 quoting your credit card number. Or, of course, you can buy at our showroom between 9.00–6.00pm, Monday–Friday 9.00–1.30pm, Saturday.

Now available from John Menzies.

To: Opus Supplies Ltd., 158 Camberwell Road, London SE5 0EE.  
Please send me:

- \_\_\_\_\_ High Resolution Colour Monitor(s) at £229.95 each (ex. VAT).  
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\_\_\_\_\_ Connection lead(s) at £6.00 each.

I understand carriage per monitor will cost an extra £7.00. (N.B. A High Resolution Monitor including VAT, lead, and carriage costs £279.39. A Medium Resolution Monitor including VAT, lead and carriage costs £187.39).

I enclose a cheque for £\_\_\_\_\_ Or please debit my credit card account with the amount of £\_\_\_\_\_. My Access/Barclaycard (please tick) no. is \_\_\_\_\_

Please state the make of your computer \_\_\_\_\_

Name \_\_\_\_\_

Address \_\_\_\_\_

Telephone: \_\_\_\_\_

**Opus.**  
Opus Supplies Ltd.

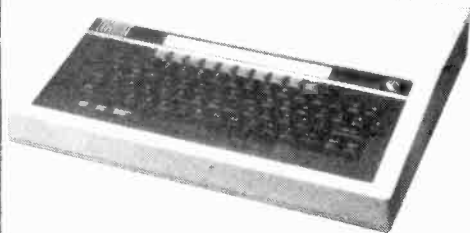
WW12

MODEL REFERENCE	1302 2 High Resolution	1302 1 Medium Resolution
RESOLUTION	580x 470 Pixels	370x 470 Pixels
C.R.T.	14"	14"
SUPPLY	220/ 240v. 50/60Hz.	220/ 240v. 50/60Hz.
E.H.T.	Minimum 19.5kv Maximum 22.5kv	Minimum 19.5kv Maximum 22.5kv
VIDEO BAND WIDTH	10MHz	6MHz
DISPLAY	80 characters by 25 lines	80 characters by 25 lines
SLOT PITCH	0.41mm	0.63mm
INPUT VIDEO	R.G.B. Analogue/ TTL Input	R.G.B. Analogue/ TTL Input
SYNC	Separate Sync on R.G.B Positive or Negative	Separate Sync on R.G.B Positive or Negative
EXTERNAL CONTROLS	On/off switch and brightness control	On/off switch and brightness control

# BBC Micro Computer System

## OFFICIAL DEALER

Please phone for availability



Software from ACORNSOFT/  
PROGRAM POWER/GEMINI in  
stock

- BBC Model B £348
- B + Econet £389
- B + DFS £409
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- WORDWISE 8k Rom £32
- Carr £1.50
- UTILITY ROMS
- BBC Ultracalc £65, Toolkit £20
- EXMON £20 Disc Doctor Rom £28
- FX Dump £15 Graphics Rom £28
- Termi Rom £29

# FLOPPY DISC INTERFACE

## £84 & £15 installation

### BBC COMPATIBLE DISC DRIVES

These drives are supplied with manual, form disc and cables.

Single Drive: 100k £150; 200k £180\*; 400k £195.

Single Drive with PSU: 100k £185; 200k £260; 400k £240.

Dual Drive with PSU: 2 x 100k £330; 2 x 200k £400\*; 2 x 400k £420

\*These drives are switchable between 40/80 tracks.

40/80 Switch Module for 1 x 400k and 2 x 400k Drive £32.

DISKETTES: In packs of 10. W = Wabash, M = 3M

40T SSSD, W: £15, M: £17.50; 40T DSDD M: £22

80T SSSD, W: £24, M: £26; 80T DSDD, W: £26, M: £30

Carriage £2/box.

FLOPPICLENE Drive Head Cleaning Kit £14.50

Phone or send for our BBC leaflet

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- SANYO DR101 Data Recorder £34 + £2.50 carriage
- BBC Tape Recorder £28.50 + £2.50 carriage
- Cassette Lead £3 + £1 carriage
- HOBBIT Floppy Tale £135 + £2.50 carriage
- HOBBIT Zero Memory Option £25 + £1 carriage
- Computer Grade C12 cassette 50p each. £4.50 for 10 £1 carriage

### MONITORS

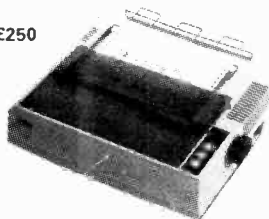
- MICROVITEC 1431 14" RGB Std Res £210
- MICROVITEC 1431P 14" RGB/PAL Std Res £249
- MICROVITEC 1451 14" RGB Med Res £320
- MICROVITEC 1441 14" RGB Hi Res £440
- MICROVITEC 2031 20" RGB Std Res £287
- KAGA VISION 12" RGB Hi Res £230
- KAGA VISION II 12" RGB Hi Res £260
- KAGA VISION III 12" RGB Super Hi Res £385
- KAGA 12" GREEN Hi Res £106
- SANYO DM8112CX 12" Green Hi Res £99
- All leads included. Carriage £7

### TORCH Z80 DISC PACK

Your BBC computer can be converted into a business machine with the addition of a TORCH Z80 disc pack. The Torch pack with twin disc drive and the Z80 processor card greatly enhances the computer's data storage and processing capability. Z80 card comes complete with 64K RAM and a CP/M compatible operating system. In addition to BBC owner's user guide and a systems disc the package is supplied with PERFECT software package comprising of DATABASE, WORD PROCESSOR & SPREADSHEET and COMANEX, an interactive business management game. Complete Package for £730 + £8 carr.

### PRINTERS & PLOTTERS

- EPSON FX80 £325. EPSON RX80 FT £250
- EPSON FX-100 £555
- NECPC80 23BE-N £310
- SEIKOSHA GP 100A £170
- SEIKOSHA GP 250X £190
- SEIKOSHA GP 700A Colour £375
- JUKI 6100 Daisy Wheel £365
- MSP 40 Col Printer/Plotter £109
- Colour Graphics Plotter A3 size £270
- GRAFPAD Graphics Tablet £125
- Carriage £7.



### ACCESSORIES

- Parallel Printer Lead £10 + £1 carriage
- Serial Printer Lead £8 + £1 carriage
- EPSON Serial Interface 2K £40 + £1 carriage
- EPSON Serial Interface £25 + £1 carriage
- NEC Serial Interface £42 + £1.50 carriage
- EPSON Paper Roll Holder £17 + £1.50 carriage
- FX80 Tractor Attachment £37 + £1.50 carriage
- Paper Fanfold 2000 sheets £13.50 + £2.50 carriage

### 'TIME-WARP'

#### BBC REAL-TIME-CLOCK/CALENDAR

A low cost unit that opens up the total range of Real-Time applications. With its full battery backup, possibilities include an Electronic Diary, automatic document dating, precise timing and control in scientific applications, recreational use in games, etc - its uses are endless and are simply limited by one's imagination. Simply plugs into the user port - no specialist installation required - No ROMS. Supplied with extensive applications software. £29.

### BBC EPROM PROGRAMMER

A fully self-contained Eprom Programmer with its own power supply, able to program 2516, 2716/32/32A/64/128 single rail Eproms.

- ★ Personality selection is simplified by a single rotary switch.
- ★ Programming voltage selector switch is provided with a safe position.
- ★ Warning indicator to show programming in progress.
- ★ Programmer can read, blank check, program and verify at any address/addresses on the EPROM.
- ★ Simple menu driven software supplied on cassette (transferable to disc).
- ★ Full editor with ASCII disassembler.

Programmer complete with cables, software and operating instructions: £89 + £2 p&p

### BOOKS (no VAT; p&p £1)

- Advanced User Guide (£2 p & p) ..... £12.95
- Assembly Lang Prog. for BBC ..... £8.95
- Assembly Lang programming on BBC Micro by Ferguson and Shaw ..... £7.95
- Basic Prog. for BBC ..... £5.95
- BBC An Expert Guide ..... £6.95
- Easy Programming on BBC ..... £5.95
- Further Programming on BBC ..... £5.95
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- Programming the BBC ..... £6.50
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- Structured Programming ..... £6.50
- The Friendly Computer Book BBC ..... £4.50
- Beyond Basic BBC ..... £7.25

### EPROM ERASERS

UV1T Eraser with a built-in timer and mains indicator. Built-in safety interlock to avoid accidental exposure to the harmful UV rays. It can handle up to 5 eproms at a time with an average erasing time of about 20 mins. £59 + £2 p&p.

UV1 as above but without the timer £47 + £2 p&p.

UV140 up to 14 Eproms £61.

UV141 as above but with timer £79.

### PRODUCTION PROGRAMMER: P8000

P8000 provides reliable gang programming of up to 8 EPROMS simultaneously with device sizes up to 16k x 8 bytes. Devices supported range from 2704 to 27128 in single and three rail versions. Simple menu driven operation ensures easy eprom selection and reliable programming in minimum programming times. £695 + £6 carriage.

Large number of other titles stocked

### ★★ ATTENTION ★★

All prices in this double page spread are subject to change without notice.

### ACORN IEEE INTERFACE

This IEEE 488 standard interface is a general purpose system for exchanging digital data between a number of devices in a local area. The interface complies with the IEC 625-1 standard and can be connected to up to 14 other devices. Interface board is supplied complete with software in ROM, interconnecting cables, IEEE cable for connection to an external device and a comprehensive manual. £282.50 + £2.50 carr.

### SMARTMOUTH

#### SPEECH SYNTHESISER FOR BBC

The 'infinite vocabulary' self-contained speech synthesiser unit. Uses only 5-10 bytes per word - no ROMs required - simply plugs into the user port. (Has Aux. Audio output sct.). Supplied with Demo/Development programs and simple software instructions, £37 + £2 p. & p.

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### CONNECTOR SYSTEMS

#### I.D. CONNECTORS

(Speedblock Type)			
No of ways	Header	Receptacle	Edge Conn.
10	90p	85p	120p
20	145p	125p	195p
26	175p	150p	240p
34	200p	160p	320p
40	220p	190p	340p
50	235p	200p	390p

#### D CONNECTORS

No. of ways			
MALE		FEMALE	
Solder	80p	105p	160p
Angled	150p	210p	250p
Solder	105p	160p	200p
Angled	165p	215p	290p
Hoods	90p	85p	90p
IDC 15-way plug	340p	Socket	400p
IDC 25-way plug	385p	Socket	450p

#### TEXT TOOL ZIF

SOCKETS	24-pin £5.75
	28-pin £8.00
	40-pin £9.75

#### DIL SWITCHES

4-way	70p	8-way	130p
6-way	100p	10-way	150p

#### JUMPER LEADS

24" Ribbon Cable with Headers				
1 end	14pin	16pin	24pin	40pin
2 ends	145p	165p	240p	350p
	210p	230p	345p	540p

#### RS 232 JUMPERS

(25-way D)	
24" Single end Male	£5.00
24" Female-Female	£5.25
24" Male-Male	£10.00
24" Male-Female	£3.50
24" Female-Female	£9.50

#### DIL HEADERS

Ribbon Cable with D. Conn.		
25-way Male	500p	Female 550p
Solder Type	40p	100p
	160p	110p
	240p	150p
	400p	225p

#### AMPHENOL CONNECTORS

Solder IDC	
36-way plug Centronics	£5.25
36-way socket Centronics	£5.50
24-way plug IEEE	£5.00
24-way socket IEEE	£4.75
PCB Mtg Sct. Ang pin	£5.00
24-way £6.00. 36-way £6.50	

#### RIBBON CABLE

(Gray/meter)	
10-way	40p
16-way	60p
20-way	85p
26-way	120p
34-way	160p
40-way	180p
50-way	200p
64-way	280p

#### EURO CONNECTORS

DIN 41617	Plug	Skt.
21-way	160p	165p
31-way	170p	170p
DIN 41612		
2x32-way St. Pin	230p	275p
2x32-way Ang. Pin	275p	320p
3x32-way St. Pin	250p	300p
3x32-way Ang. Pin	375p	400p
1 DC Sct. A + B 275p	A + C 350p	

#### TEST CLIPS

14-pin 375p	16-pin 400p
	40-pin £10.30

#### EDGE CONNECTORS

0 1"		0 156"	
2x6-way (Commodore)	—	—	300p
2x10-way (Commodore)	—	150	—
2x12-way (Vic 20)	—	—	350p
2x18-way	—	—	140p
2x22-way (ZX81)	—	—	220p
2x25-way	—	—	225p
2x28-way (Spectrum)	—	—	200p
2x36-way	—	—	250p
1x43-way	—	—	250p
2x22-way	—	—	190p
2x43-way	—	—	355p
1x77-way	—	—	400p
2x50-way (S100conn)	—	—	600p

Table listing various electronic components such as diodes, capacitors, and integrated circuits with their respective part numbers and prices.

Table titled 'LINEAR ICs' listing various integrated circuits including operational amplifiers, comparators, and logic devices.

Table titled 'COMPUTER COMPONENTS' listing CPUs, controllers, memories, support devices, ROMs, and EPROMs.

Table titled 'MODULARS' listing various modular components like relays, triacs, thyristors, and bridge rectifiers.

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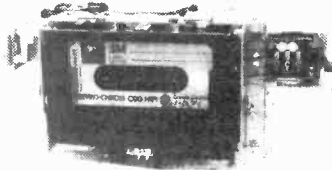


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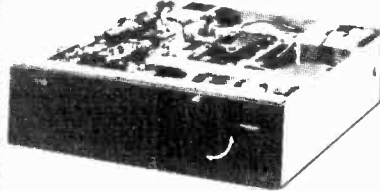
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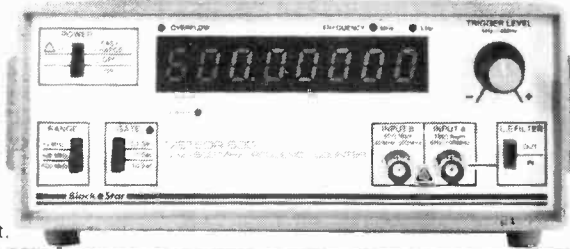
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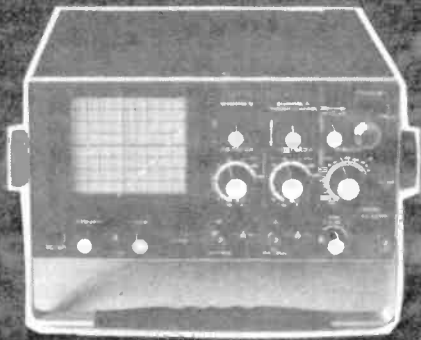
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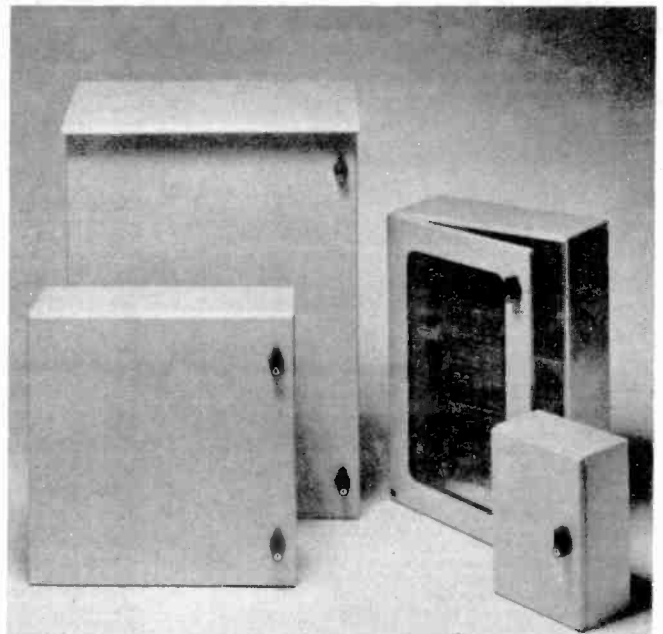
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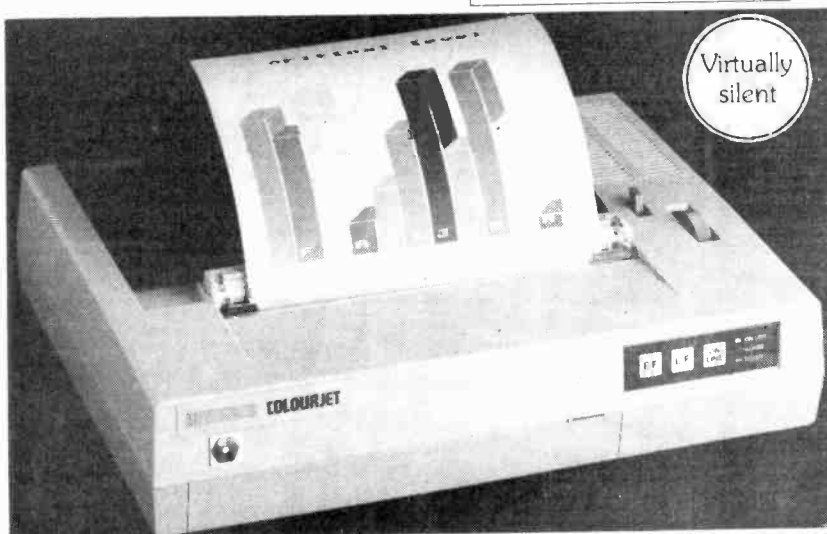


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- ★ Auto configuring 'FLEX' disc operating system boot program in monitor
- ★ 12x9.5in. through hole plated main PCB; 3x4in. eeprom board.

'FLEX', which is supported by MICROBOX, is a well-proven, industry standard, disc operating system with a wealth of available software packages. Basic, Forth, Pascal, PL9 and C high-level languages as well as assemblers, word processors and electronic spreadsheet are currently available. Clever programming techniques have permitted the inclusion in the system monitor of a boot program that automatically loads and configures the operating system to the MICROBOX hardware requirements.

The on-board ram and eeprom discs are seen by the operating system as conventional disc drives. The ram disc has the capacity of a 40-track single-density disc but with an access time 10 times that of a floppy disc. Eeprom discs are supported by way of a plug-in eeprom carrier which has provision for four 8, 16, 32 or 64K eeproms into which can be programmed the operating system and any other often used programs by way of the built-in programmer. 'FLEX' supports up to four disc drives which in MICROBOX can each be allocated as floppy, ram or eeprom types so providing, if required, a completely silicon configuration.

A startup kit for the advanced MICROBOX system is available and consists of: Bare PCBs, 8K system support monitor, 'FLEX' system support disc, constructional notes, system documentation, component supplier list.

PRICE: £95 + V.A.T.

'FLEX' disc operating system for MICROBOX, including editor and assembler: £75 + V.A.T.

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### Micro Concepts

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Above prices include Carr/postage & VAT.

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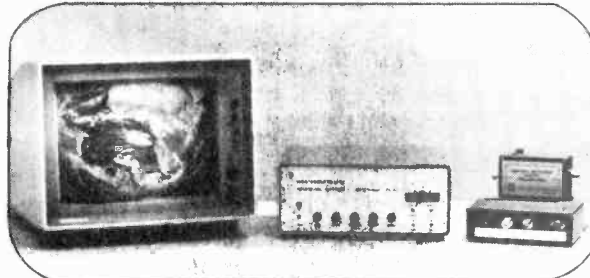
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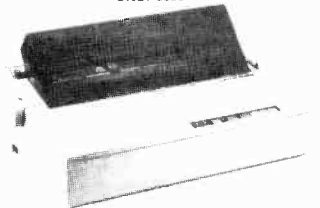
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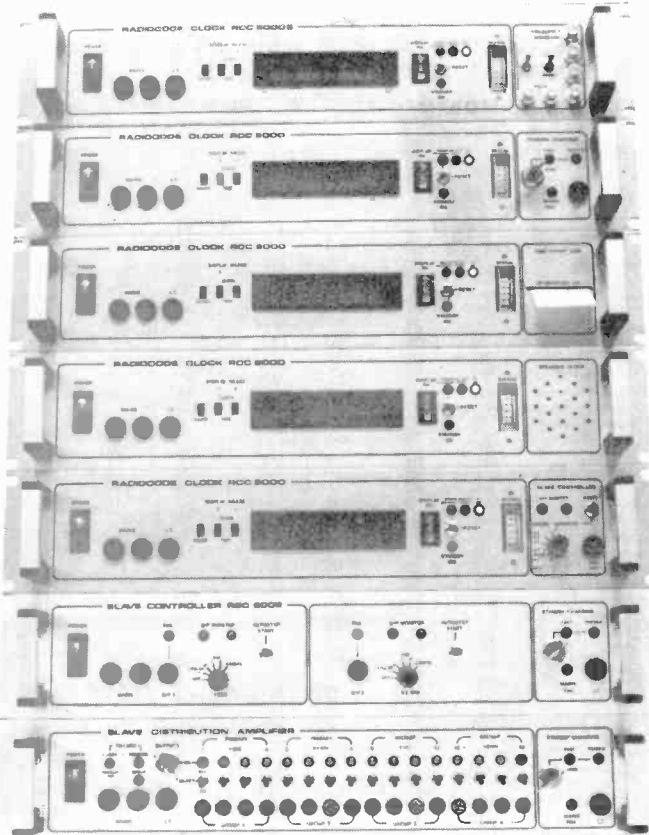
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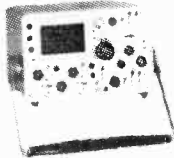
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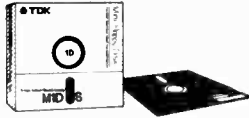
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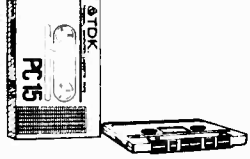
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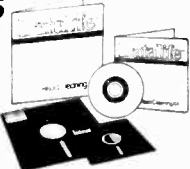
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**TDK PC15** £5.90

### DISK DRIVE HEAD CLEANING KITS



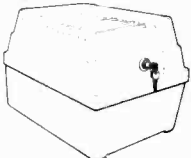
Helps to protect your valuable data, and minimise expensive downtime and repair costs. Consists of a flexible jacket, which receives a pre-saturated cleaning disk. Each disk is sealed within a foil sachet to ensure that it contains the right quantity of cleaning fluid when used. After use the disk is disposed of, and the jacket is kept for future use.

Suitable for single or dual head drives. Please specify 8" or 5 1/4" disks.

**STARTER KIT** £7.70  
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**REPLACEMENT CLEANING KITS** £14.80  
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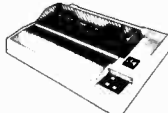
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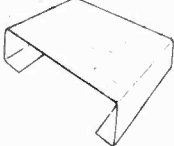
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Print sample available on request.

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**Special VIC20/VIC 64 interface** £46.00

### PRINTER STAND



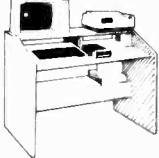
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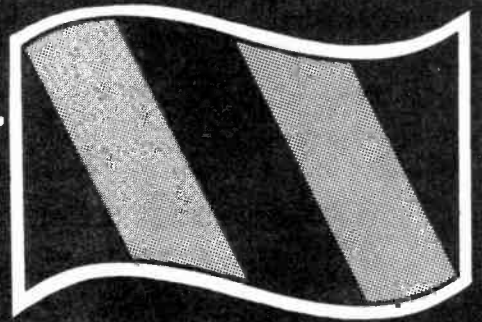
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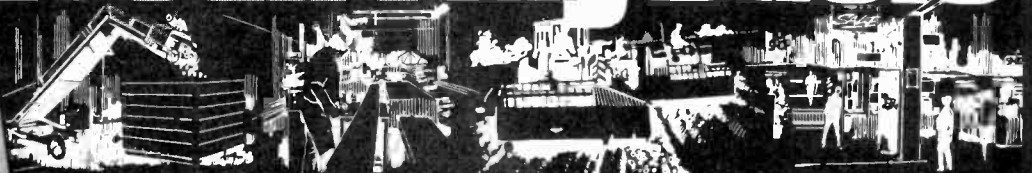
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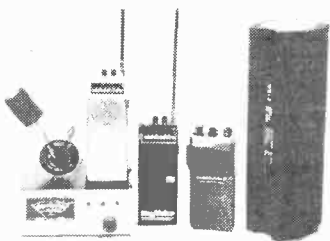


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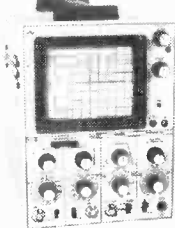
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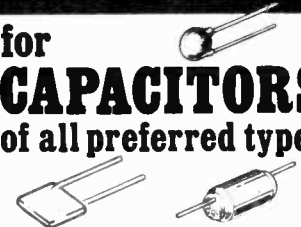
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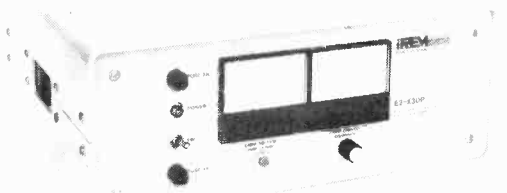
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**ELECTRONIC COMPUTER AND MANAGEMENT APPOINTMENTS LIMITED**  
 Freepost, Barkway, Royston, Herts SG8 8BR

(1926)

*Philip Drake Electronics Ltd is a growing, successful company that has established itself as a leading supplier of studio communications equipment, programme quality sound distribution modules and special "one-off" designs to the Broadcast Industry.*

*Our continuing expansion has led to a requirement for suitable people to fill the following positions which have become vacant or are being created to handle our increasing business.*

*As well as attractive salaries, the Company offers a pension scheme and BUPA membership and the new premises being constructed will provide a pleasant working environment when completed.*

### PROJECT ENGINEERS

We have vacancies in the Projects Department for both senior and junior engineers. The department deals primarily with system design of studio talkback and intercom equipment. In addition to this, the department undertakes one-off designs to customer's requirements and modifications to audio and control equipment. The work involves liaison with customer engineers, detailed system design, preparation of production and handbook documentation and technical support for sales, manufacturing and test departments.

Applicants for the senior projects engineering positions should have a recognised electronic engineering qualification and at least two years' experience of system/project engineering of professional equipment.

Junior engineers would initially assist on major projects but would be expected to tackle small systems as experience is gained. A suitable engineering qualification and some practical experience could be advantageous to enable the successful applicants to progress within the Company.

Applications in writing and including an up-to-date cv should be addressed to **The Personnel Officer, Philip Drake Electronics Ltd, 37 Broadwater Road, Welwyn Garden City, Herts AL7 3AX**, or phone **Jill Humphreys** on **Welwyn Garden City (07073) 33866** for an application form.

(2533)

### ANALOGUE/DESIGN ENGINEERS

We have vacancies for experienced engineers to join our Development Department. Candidates should have a relevant degree and will probably have worked in a design environment. The person will be responsible for all aspects of development from initial concept to production, and will therefore become involved in a variety of tasks. An ability to produce innovative but practical designs with minimum supervision is essential.

### JUNIOR DRAUGHTSMAN

A junior draughtsman is required to join our Development Department. The work involves close liaison with engineers to produce metalwork, circuit and wiring drawings for both manufacture and customer documentation. The ideal applicant will be self-motivated and capable of adding the finer details to the work passed on by the engineer.

### TEST ENGINEERS

We are looking for suitably qualified test engineers with experience in testing analogue (preferably audio) circuits, who will be involved in varied testing, from small batch produced modules to complete communication systems, and who are able and willing to adapt to digital technology as this is introduced by the Company.

## Analogue design

£8K to £14K

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**0453 883264 & 01-290 0267**

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## Electronic Test Engineers/Technicians

Racal Radar Defence Systems part of the Racal Electronics Group is undergoing a period of rapid growth. To meet our increasing production demands, we need to recruit a number of Test Technicians and Test Engineers at the following locations in Surrey - New Malden, Chessington and Hersham, and at Leicester.

The Company manufactures a wide range of products aimed principally at the Defence Industry including radar early warning and guidance systems, military displays and ECM and ESM systems.

The Test Department is responsible for the test and diagnostic functions on a wide range of complex radar equipment using high quality manual and automatic test equipment.

Applicants should be educated to HNC/HTC standard and have practical knowledge or experience of radar and/or microwave systems.

Conditions of employment are excellent including a competitive salary, five weeks holiday, and company pension and life assurance scheme.

Interested? Then phone me on: 01-397 5281 or alternatively write with brief details of qualification experience and current salary to:

Mr P N Willis,  
Senior Personnel Officer,  
Racal Radar Defence Systems Ltd.,  
Davis Road, Chessington, Surrey.

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**RACAL**

(2188)

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We have many clients interested in employing ex-Service fitters and technicians at sites throughout the U.K. Phone for details.

#### 5) £600 per week

We are paying very high rates for contract design and test engineers who have a background in RF, Microwave, Digital, Analogue or Software, at sites throughout the U.K.

Hundreds of other Electronic and Computer vacancies to £12,500  
Phone or write:

Roger Howard, C.Eng., M.I.E.E., M.I.E.R.E.

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Tel: 0344 489489 (1640)

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Box No. 2499

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The problems we are solving are difficult:  
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Although we don't necessarily expect experience in this fields, we do require a good theoretical background, combined with practical engineering ability. Whether you have just graduated or have one-two years' experience, you will need to be one of the best. Most of the problems with which we are faced have not been solved before; inventive design and a professional attitude are required.

At our Research and Development Department in rural Oxfordshire you will find a small, enthusiastic, friendly team, using computer-aided design, manufacture and test to create original high performance hardware of the highest quality.

Please write to John Wilson and enclose your cv

(2497)

# Appointments

## Electronics Engineers £9561 Communications Design in High Tech Country

At H.M. Government Communications Centre we're using the very latest ideas in electronics technology to design and develop sophisticated communications systems and installations for special Government needs at home and overseas.

With full technical support facilities on hand, it's an environment where you can see your ideas progress from initial concepts through prototype construction, tests and evaluation, to the pre-production phase, with a chance to influence every stage. Working conditions are pleasant, the surroundings are attractive, and the career prospects are excellent.

Ideally we're looking for men and women who have studied electronics to degree level or equivalent and have had some experience of design, whether obtained at work or through hobby activities. Appointments will be made as Higher Scientific Officer (£7149-£9561) or Scientific Officer (£5682-£7765) according to qualifications and experience.

For further details please write to the address given below. As our careful selection process takes some time, it would be particularly helpful if you could detail your qualifications, your personal fields of interest and practical experience, and describe the type of working environment most suited to your career plans.

The Recruitment Officer, HMGCC, Hanslope Park, Buckinghamshire MK19 7BH.

(2448)

### APPLICATIONS ENGINEERS CUSTOMER SUPPORT ENGINEERS

## Zehntel LTD

**AUTOMATIC TEST EQUIPMENT  
£ NEG MILTON KEYNES**

Due to rapid growth, ZEHNTEL are again looking for additional APPLICATIONS ENGINEERS and CUSTOMER SUPPORT ENGINEERS to be based at their Milton Keynes office.

ZEHNTEL are world leaders in in-circuit technology, and as such, require quality people to assist with further expansion plans.

The ideal candidates would be:

- ★ Aged between 20 and 40.
- ★ Qualified to Degree level or equivalent.
- ★ Background/experience in software & hardware engineering.

Above all, we are looking for self-motivated people, who want to be a part of a progressive team.

The benefits package includes an excellent salary and bonus scheme, private health insurance and genuine career prospects. Company car commensurate with position.

Please write in confidence, enclosing cv to:

**The Personnel Manager  
ZEHNTEL LTD  
Sentry House**

**500 Avebury Blvd., Saxon Gate West  
Central Milton Keynes MK9 2NJ**

(2507)

### Brompton Hospital

## Medical Physics Technician III ELECTRONICS

A vacancy exists for a technician with hospital experience to join the team of technicians in the Department of Medical Electronics. The Department provides a comprehensive maintenance and development service to two busy cardiothoracic hospitals. The technician will be based initially at the Brompton Hospital, SW3, but he/she must be willing to also work at London Chest Hospital, E2.

**For further information contact Mr P. Butler, Chief Technician, 01-980 4433, Ext 340.**

**For a job description and application form contact Miss J. A. Jenks, Group Personnel Manager, Brompton Hospital, Fulham Road, London SW3 6HP. Tel: 01-352 8121 Ext 4357.**

(2501)

## ELECTRONICS RESEARCH at the UNIVERSITY OF ESSEX

Graduates who have (or final year students who expect to obtain) a first or upper second class honours degree are invited to apply for research leading to a higher degree (M.Sc., M.Phil. or Ph.D.) in the following areas:

**Acoustic Noise and Vibration Cancellation** (adaptive microprocessor-controlled system); **Audio Engineering** (high-precision digital signal processing, system transparency, stereo); **Circuit Design Studies** (circuit theory, fault diagnosis, sensitivity effects, CAD, filter realisations); **Digital Transmission for Telecommunications** (data transmission filters, pulse shaping and channel coding techniques, local digital access); **Interactive Systems** (handwriting analysis, computer graphics, speech, personal databases); **Microcomputer Systems** (embedded microcomputer applications, micro-programming, architectures); **Microwave and Millimetre Wave Engineering** (scattering from precipitation particles, space frame radomes); **Optical Communications** (detectors, noise processes, signal design, switching); **Picture Coding and Processing** (data reduction, adaptive filtering, motion estimation, feature extraction); **Satellite Communication Systems** (business systems, protocols, data and video services); **Telecommunication Switching Systems and Software** (computer control, software production, teletex and viewdata, information system performance engineering); **Visual Displays and Television Engineering** (computer graphic input systems, stereo, colour and high-precision displays).

Further information and application form available from: Dr. G. J. Ritchie, Chairman, Department of Electrical Engineering Science (ref JAN/2), University of Essex, Wivenhoe Park, Colchester CO4 3SQ.

(2512)



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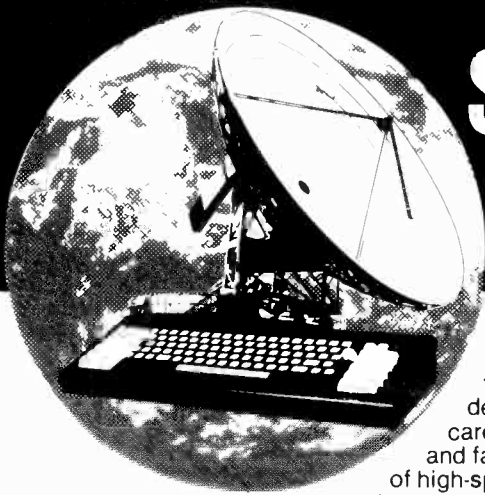
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You will have the opportunity to be fully involved in total systems, from RF to Baseband, including system configuration, advanced studies or original hardware design. You will also enjoy an up-front position in some of today's most prestigious communication projects which include advanced data networks and next-generation satellite ground stations.

To cope with the increasing demand for their expertise, this go-ahead Company seeks to recruit further high calibre professional engineers who have an engineering degree or HND and at least 2 years experience in communications or related technology for:

**Microwave/R.F., I.F. and Baseband Design;  
Antenna Design;  
Real-Time Software Design;  
System Design; Systems Definition;  
Advanced Systems Studies;  
Technical Management — Group and Section Leadership; Project Management.**

Opportunities also exist at less senior levels for candidates with HNC/H. Tech. qualifications or graduates yet to gain experience.

With an attractive salary package, the opportunity for overseas travel and full company benefits, including five weeks holiday and generous relocation package, these important positions present a major opportunity for the engineer set to really make his mark in world-wide communications.

**TO FIND OUT MORE** and to obtain an early interview, please telephone FRED JEFFRIES C.Eng. MIERE in complete confidence on HEMEL HEMPSTEAD (0442) 212655 during office hours or on (0442) 49909 evenings and weekends (not an answering machine). Alternatively write to the address below.



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#### UNIVERSITY OF OXFORD

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### ELECTRONICS ENGINEER OR PHYSICIST

This post offers an opportunity for an engineer or physicist with a definite interest in medical engineering. The appointee would be responsible for maintaining an extensive range of computing and electronic equipment, and would design and construct a wide variety of instruments for bioengineering research. Projects currently include a range of microprocessor-based patient monitoring systems. The appointment will involve working with medical and scientific staff in both the Nuffield Orthopaedic Centre and the Department of Engineering Science of the University of Oxford. Candidates should possess a degree in electronic engineering or physics. Appropriately qualified candidates would have the opportunity to undertake original research.

Appointment to this post would be for an initial period of three years, renewable subject to the contractual arrangements for the Centre.

The salary range is £6,310-£11,615, depending on age, qualifications and experience.

Further details are available from:

**J. D. Harris, Director**  
Oxford Orthopaedic Engineering Centre  
Nuffield Orthopaedic Centre  
Headington, Oxford OX3 7LD  
Tel: 0865-64811, Ext. 514/510

Applications should be submitted by 2nd April, 1984.

(2498)

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A two-year full-time course which combines an up-to-date technological education with a considerable 'hands on' experience of a wide range of modern equipment and techniques.

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For further details contact the Department of Engineering, Cambridgeshire College of Arts and Technology, Cambridge CB1 1PT.

Telephone (0223) 352973 or 352979.

(2514)

## TRAINEE RADIO OFFICERS

### First-class, secure career opportunities

A number of vacancies will be available in 1984 for suitably qualified candidates to be appointed as Trainee Radio Officers.

If your trade or training involves Radio Operating, you qualify to be considered for a Radio Officer post.

Candidates must have had at least 2 years' radio operating experience or hold a PMG, MPT or MRGC certificate, or expect to obtain this shortly.

On successful completion of 35 weeks' specialist training, promotion will occur to the Radio Officer grade. Registered disabled people may be considered.

### SALARY AND PROSPECTS:

Trainee Radio Officer: £4,579 at 19 to £5,481 at 25 and over. On promotion to Radio Officer: £6,270 at 19 to £8,182 at 25 and over. Then by 4 annual increments to £11,182 inclusive of shift working and Saturday and Sunday elements.

For full details please contact our Recruitment Office on **Cheltenham (0242) 32912/3** or write to:



Recruitment Office, Government Communications Headquarters,  
Oakley, Priors Road, Cheltenham,  
Gloucestershire, GL52 5AJ.

(2412)

## TEST EQUIPMENT DESIGN ENGINEERS

Rediffusion Consumer Manufacturing design and manufacture a full range of advanced specification colour television receivers and monitors.

We are looking for experienced Electronic Design Engineers to help us maintain our industry lead in sophisticated computer controlled test gear for production testing of our products. Future test equipment will be an interesting mix of digital and analogue circuitry aimed at increasing the automation of the production testing operation.

If you are able to conceive, design and implement production test equipment with minimal supervision, we'd like to hear from you.

These positions are based in our Chessington Engineering Centre but some visits to our factories in the North East and Lancashire will be required at infrequent intervals. Salaries are obviously dependent on qualifications and experience, but will reflect the importance of future test gear projects to the Company's long term development.

Interested? ... Then write or phone:

Harry Brearley,  
Rediffusion Consumer Manufacturing Ltd.,  
Fullers Way South,  
Chessington, Surrey. KT9 1HJ.  
Telephone: 01-397-5411.

## REDIFFUSION

(2408)

## BRITISH ANTARCTIC SURVEY

### Radio Operators/ Electronic Technicians

The Survey requires RADIO OPERATORS/ELECTRONIC TECHNICIANS who have experience in the maintenance and operation of HF and satellite communications to work single-handed at its stations in the Antarctic.

Responsibilities of the postholders include:

The efficient operation of Inmarsat satellite communications installations, VHF and HF transmitters, receivers, and peripheral gear and its routine maintenance; logging of all traffic schedules; carrying out operational communications schedules; and maintenance of scientific electronic equipment.

Because of the isolated situation of Antarctica the ability to work on their own initiative is essential; they will be solely responsible for all aspects of communications. Ability to operate MRGC standard with some knowledge of maritime procedures is also necessary. Appropriate training on specific equipment will be given if required.

The period of employment will be from 2nd July, 1984, until spring 1987 which entails working in Antarctica for two consecutive winters.

Applications are invited from single men who are physically fit and aged between 22 and 35 to work mainly overseas.

Salary: from £7,255 per annum plus annual increments.

Accommodation provided whilst overseas. Clothing, messing and canteen are provided free on base and free messing on voyage.

For further details and an application form please write to:  
The Establishment Officer, British Antarctic Survey, High Cross, Madingley Road, Cambridge CB3 0ET. Please quote ref: BAS 6. Closing date: 11th April, 1984.

**NATURAL ENVIRONMENT RESEARCH COUNCIL**

## WALES S4C CYMRU

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### SENIOR ENGINEER

S4C is consolidating its post production facilities and urgently requires a Senior Engineer, experienced in broadcast operations and qualified in electronic to H.N.C. or equivalent standard. Based in Cardiff

**Salary: £11,091**

**Further details and application form from:-**

**Vince Flanagan, Chief Engineer,  
S4C, Sophia Close, Cardiff  
(0222) 43421**

### Inner London Education Authority LEARNING RESOURCES BRANCH

### Assistant Vision Engineer (Lighting) ST1/2

An Assistant Vision Engineer (Lighting) is required to work as part of a team taking responsibility for the quality of television pictures recorded. The assistant vision engineer will be particularly concerned with the rigging, adjustment and maintenance of lamps and operation of telecine.

Candidates should have suitable technical qualifications and a good working knowledge of appropriate equipment.

The current salary range is £5,517-£8,316 plus £1,347 L.W.A.

Application forms and further details are available from: The Education Officer, EO/Estab. 1B, Room 365, The County Hall, London SE1 7PB.

The closing date for the receipt of completed application forms is 16th April 1984. This post is suitable for job sharing.

ILEA is an equal opportunities employer

(2517)

## ARTICLES FOR SALE

### WORLD RADIO TV HANDBOOK

1984 ed. £12

1984 THE RADIO AMATEUR'S H/B by A.R.R.L. Price £12.50

BEGINNER'S GUIDE TO INTEGRATED CIRCUITS by I. R. Sinclair Price £4.50

ELECTRONIC PROTOTYPE CONSTRUCTION by S. D. Kasten Price £15.95

UNDERSTANDING ELECTRONIC SECURITY SYSTEMS by M. D. Lamont Price £2.30

UNDERSTANDING DIGITAL ELECTRONICS by G. McWhorter Price £4.30

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AVO 8 SERIES. Fully refurbished and calibrated Avo 8 Mark 3, 4, 5. Price including Avo type leads, prods, crocs and VAT £70. Also digital meters from £29. Telephone for details Bela Electronic Designs, Bedford 857171. (2521)

VALVES, PROJECTOR Lamps, 6000 types, list 75p, world wide export. Cox Radio (Sussex) Ltd., The Parade, East Wittering, Sussex. Phone (024 366) 2023. (1991)

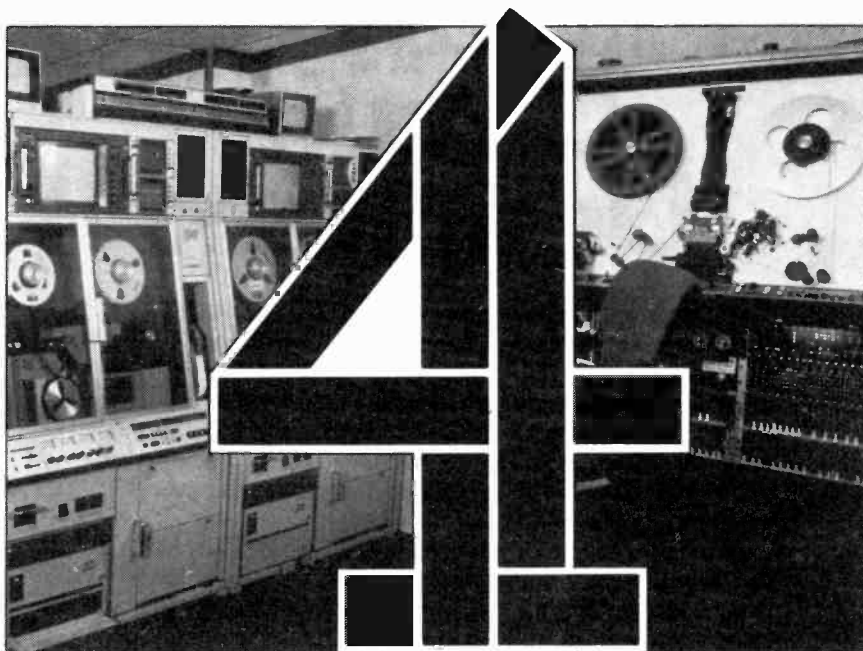
RADIO MORSE READING PROG. FOR ZX81, unexpanded memory. Prints translated Morse Code on screen with spaced scroll action, easy to read. Variable speed. £7. Spectrum version £8. Pinehurst Data Studios, 69 Pinehurst Park, W. Moors, Wimborne, Dorset BH22 0BP. (2532)

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Please apply, with full C.V. including current salary, to the Personnel Department, Channel 4 Television, 60 Charlotte Street, London W1P 2AX, quoting reference EG13.



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325 Fore Street, London N9 0PE

(1762)

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# Microwave Circuit Designers

Here at Marconi Electronic Devices, our Microwave Development team is dedicated to the achievement of excellence.

Our products and indeed the whole division is built around people, creating an environment packed with all the technical resources you'll ever need. We don't just believe in our engineers, we believe in supporting them with every means at our disposal.

We want to talk to Microwave Engineers who will be able to put these resources to good use. Your experience could be in any of a number of areas – SAW Devices, RF System Integration, FET Amplifiers, Mixers, Switches, etc.

It's a rare chance to influence the future direction of microwave technology, providing an innovative input on projects at the very forefront of component and sub-system technology.

So call **Chris McDonnell** on **0522 693389** during normal working hours or any evening between **7.00pm** and **9.00pm** on **0522 752244**. Alternatively send brief career details to him at: **Marconi Electronic Devices Ltd., Doddington Road, Lincoln LN6 3LF.**



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 TEKTRONIX Model 4601 hard copy unit for 4000 Series graphics terminals ..... £185  
 GOULD-BRYANS Model 50000 'COMPUGRAPH' A3 plotter with intelligent RS232 interface. Current new price £3500. ..... £1650  
 TEKTRONIX Model 611 graphics display. (With a 1mm wide burn at extreme bottom of screen) ..... £200  
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# Wireless World

ELECTRONICS &

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**TCSU-D**  
temperature control digital

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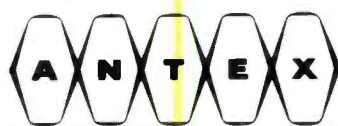
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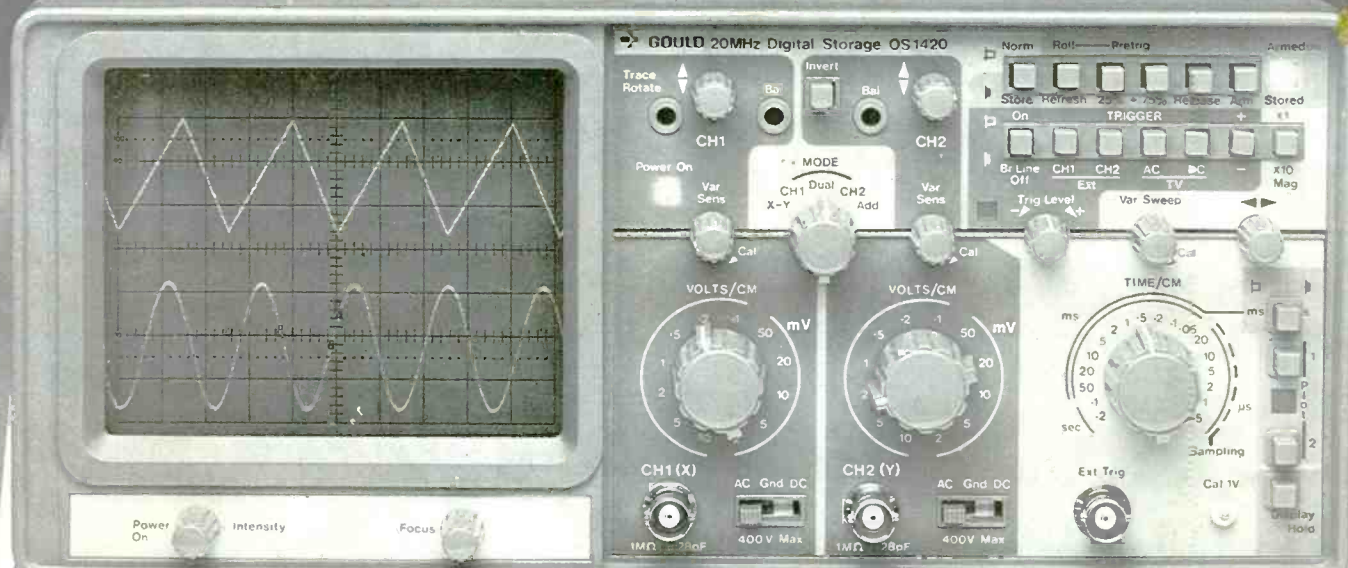
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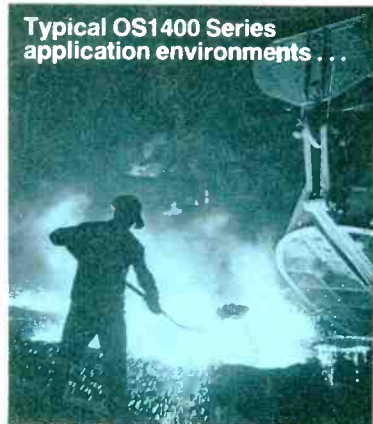
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