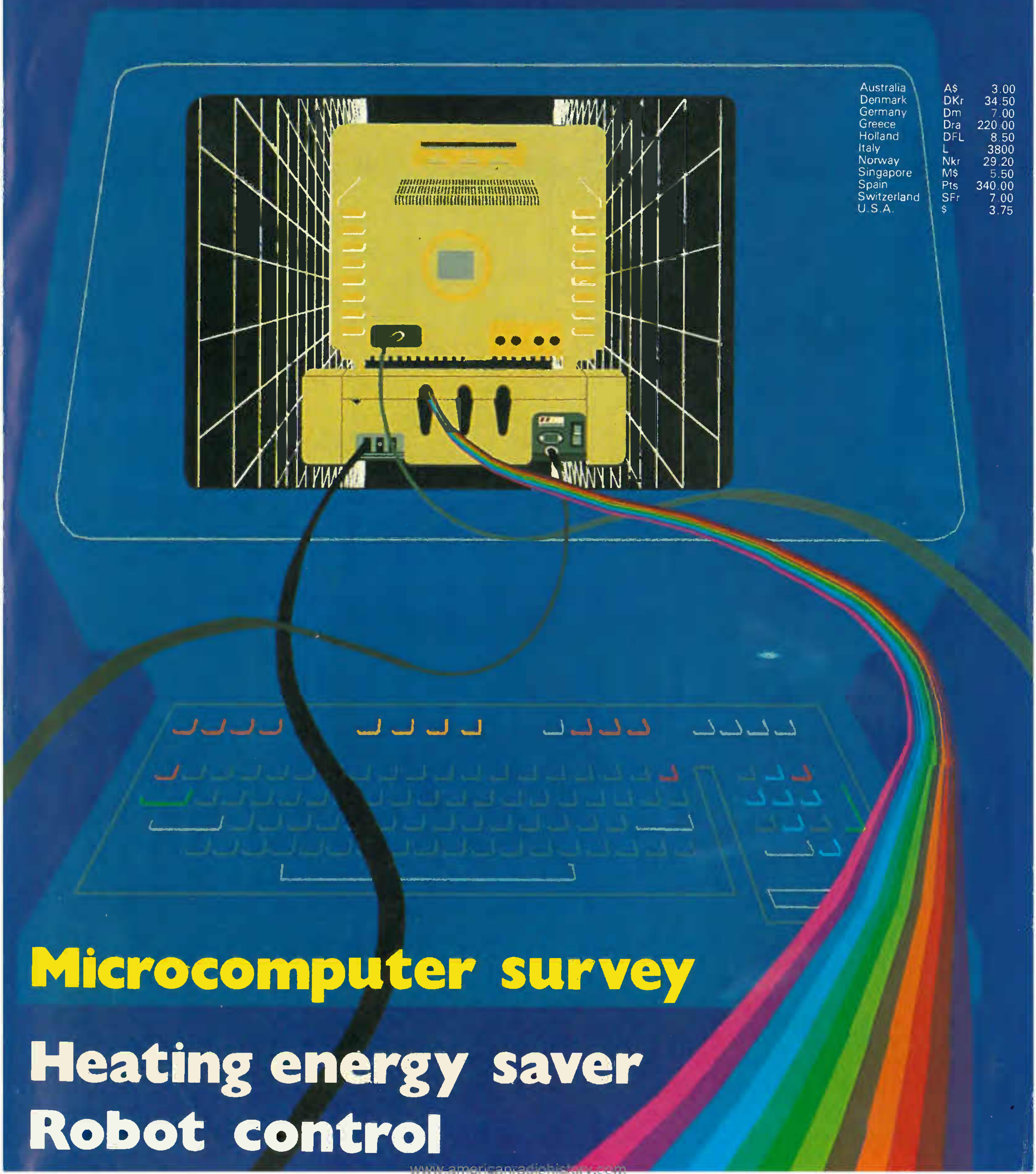
ELECTRONICS &
Wireless World

DECEMBER 1983

85p



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P8000

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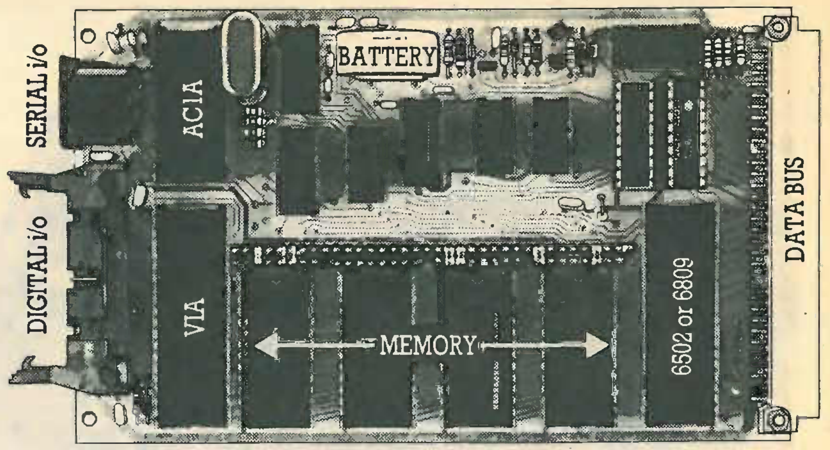

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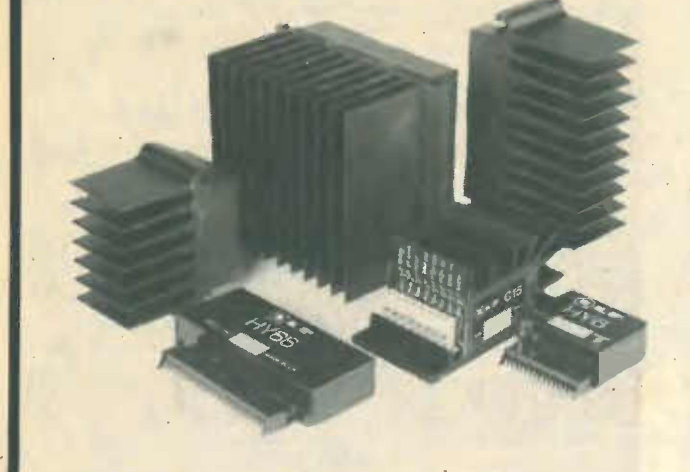

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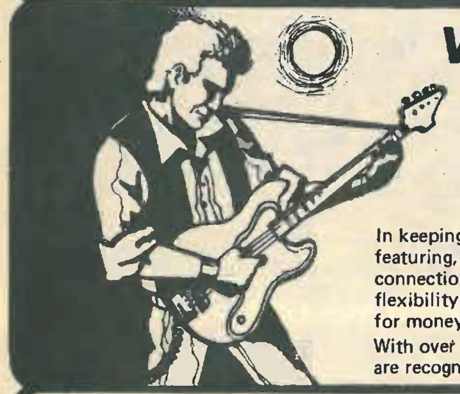

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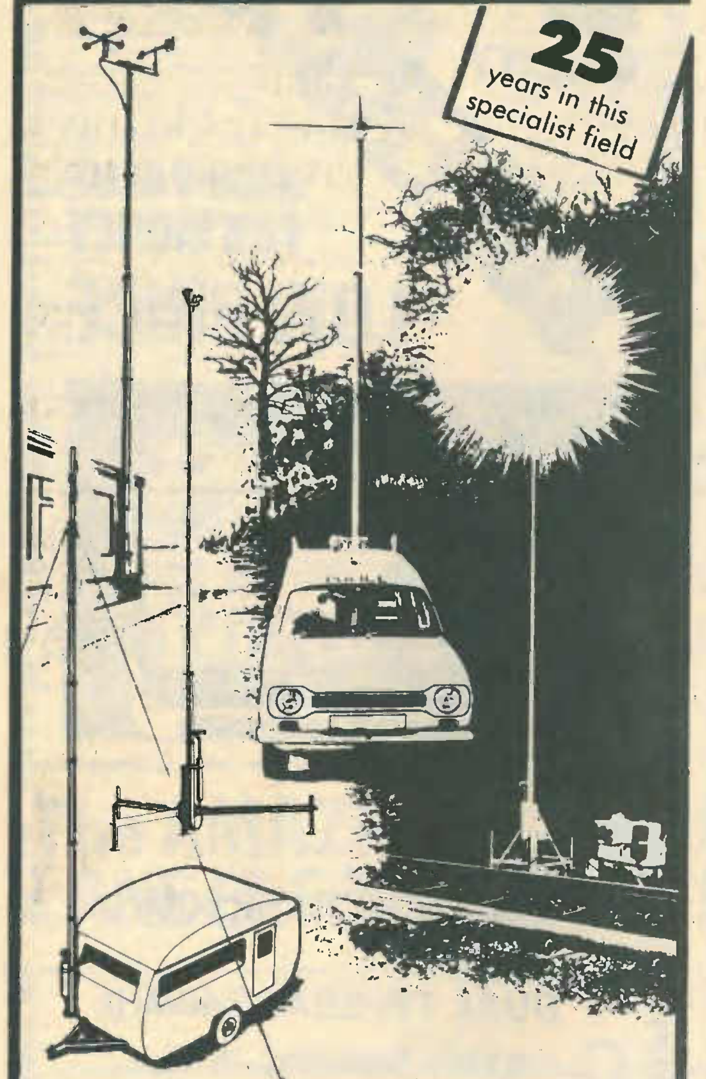

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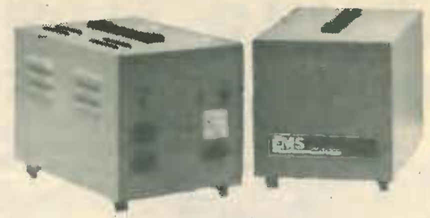

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Deputy Editor:
GEOFFREY SHORTER, B.Sc.
01-661 8639

Technical Editor:
MARTIN ECCLES
01-661 8638

Projects Editor:
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Technology assessment

An engineer's motivation is, if nothing else, to innovate. Given his head and an unlimited supply of money and facilities, a good engineer is happy to spend his time producing designs for new equipment that either demonstrate his skill in circuitry, or perform their function with a greater finesse, or both – the two not necessarily going hand in hand. The job satisfaction is present, whatever the eventual purpose of the product, in the design process.

Taking a wider view is the manager and, such is the effect of technology, the politician, whose brief is to formulate policy after taking advice from those who are expert and who will carry out the development policy.

These two fields of activity currently appear to exist almost separately: the engineer and the politician pursue their interests with no great awareness of larger problems. Advice from a committed engineer is inevitably biased – he must take a positive view of his project, or it would never reach a satisfactory conclusion, so that it is reasonable to expect that the only guidance supplied by engineers to policy makers will be favourable to continued development of any given project. Politicians are not, in the main, technically competent, and it must be only too easy for them to be seduced by technologists, with their promises of magical new developments.

Although engineering itself cannot be accused of possessing the attributes of either good or evil 'intent', events of the last few years have shown that it can produce results that are extremely difficult to forecast. There may be unexpected side-effects; a failure may cause knock-on effects that would only have been foreseen by a great deal of research; people's health might suffer; all by the application of 'innocent' technology in response to market pressure or to the excited lobbying of technologists who have discovered another solution to a demand which has yet to be created.

Recent history illustrates all this profusely: Three Mile Island, Seveso, oil spillage, nuclear waste protestations, pollution, asbestos, the aerosol fluorocarbon scare, and the most devastating of all – the possibly fatal development of nuclear weapons from an innocent enquiry into the structure of the atom.

In the US, there is The Technology Assessment Act of 1972, which is intended to provide the information needed by Congress to formulate policy. In the 11 years since it was enacted, it is not clear what effect it has had on US technology, but at least the problem is perceived. In the UK, Government still gives the impression of naively embracing all that technology has to offer, with never a second thought of unlooked-for effects on society. Its belated fascination with technology shows little sign of any concern about the possible ancillary effects of its wholesale adoption.

Ideally, there should be an international technology assessment organization, which would receive information from engineers on what is possible, and from social scientists on the probable results of applying the possible and would then reach a consensus on how to avoid disaster: technology will not be unlearned, so there will never be a way of suppressing it for ever, even if that were desirable.

COMMUNICATIONS COMMENTARY

Third method d-c

The decision by the Ministry of Defence to place a substantial order for a military version of MEL's "Callpac" h.f. manpack/vehicle transceiver brings back both third-method s.s.b. generation/demodulation and direct-conversion receiver techniques to the forefront of the communications scene. D. K. Weaver first described his ingenious "third method of generation and detection of s.s.b. signals" as long ago as December, 1956 in the famous *Proc. IRE* issue on single-sideband. In the same issue J. P. Costas drew attention to the value of direct-conversion, homodyne-type receivers for synchronous communications. But the first two s.s.b. methods – the filter and conventional phasing techniques – were more generally accepted, and in recent years the filter approach has been almost universally employed. A fourth method, based on polyphase networks and developed by M. J. Gingell of STL, has similarly never found wide use, although all four approaches have been used by radio amateurs. The popular filter method requires a fixed i.f. and cannot be used in direct-conversion or direct-generation equipment. In 1981, W. A. Painter, describing the MEL Callpac transceiver, claimed that modern technology makes possible the efficient implementation of homodyne and third-method systems in an easily manufactured, high-performance product with microprocessor control and a frequency-synthesizer using two LOC-MOS chips to cover 1.6 to 30 MHz in steps of 100 Hz, with s.s.b. as the primary mode.

Hot words

It is a long time since the hope that, with broadcasting across frontiers, nations would speak peace to nations. Our Prime Minister has made it clear that she sees need to heat up the war of radio words to combat Soviet radio "at every turn". Many commentators agree that "Voice of America" has increasingly become a service of propaganda rather than information – and President Reagan has not given up his efforts to establish Radio Marti for broadcasts on m.f. to Cuba despite solid opposition from American broadcasters. In the UK the Foreign and Commonwealth Office is attempting to overcome the local objections to its acquiring the Bearsley site for high-power h.f. transmissions to Eastern Europe.

Even that traditional friendly frontier between the USA and Canada has been witnessing a border broadcasting dispute, though this is more about money than way-of-life. In 1976 Canada introduced new tax legislation that denies tax deduction to Canadian advertisers buying time on US stations with large Canadian audiences. For some time the US Administration has been seeking a tit-for-tax measure to persuade American firms not to buy time on Canadian stations. Now there is talk of a truce, with Canada dropping its restrictions.

The commercial and technical rivalry between the four systems of a.m.-stereo being promoted in the USA by Harris, Kahn, Motorola and Magnavox took another turn in mid-August when the FCC suddenly ordered Harris to withdraw its system from the market and told 65 US stations to stop using it from September 1. FCC claimed that the stereo exciter being supplied by Harris (STX-1) was not the same as the model granted type-acceptance in August 1982, alleging that the exciter could greatly exceed, at least theoretically, FCC limits on monophonic harmonic distortion.

However, by the end of September, the FCC admitted that in practice distortion was low and granted "temporary authorization", allowing the 65 stations to resume stereo broadcasting. Harris claim to be clear leader in the a.m. stereo race, with more than 70 exciters supplied; Kahn has around 30 stations using his system; Motorola around 20; and Magnavox "a handful".

Useful or viable?

People involved in telecommunications and broadcasting have observed, with increasing unease, the enormous number of options that new technology can provide in the form of new user-services, new products, made possible largely by the development of very-large-scale integration (and soon ultra-large-scale integration), by the gradual blurring of the former distinctions between telecommunications services and broadcast services, and by the possibility of further exploiting the radio spectrum. Teletext, with 7 Mb/s data, carried piggy-back on television transmissions is a vivid but by no means unique example of what can be done.

Radiodata, already waiting in the wings, could provide a host of new services, including a nationwide low-cost personal radio paging service. Earlier this year the FCC created new opportunities for the 4500 American v.h.f./f.m. broadcast stations by relaxing its rules for SCA ("subsidiary communications authorization"). This is the long-established extra channel subcarrier system often known as "storecasting" but which over the years has been used for a wide variety of special programming. By extending the f.m. baseband from 75 to 99 kHz, American stations can now provide two separate SCA services, including non-broadcast applications such as paging, electronic mail, data and facsimile. The flexible EBU Radiodata specification, now facing another series of field-trials, differs from SCA in not incorporating speech or music transmission capability, though for example ASCII control of voice synthesizers is foreseen as a useful means of providing traffic information.

Overnight distribution of "subscription" material for use on v.c.r. machines ("Home Video Network") was approved in 1982 by FCC for use on the ABC network, following development by Sony as an alternative to cable and DBS. Selective distribution of information by radio is already reflected in the "Dow-Alert" system aimed, for instance, at business and financial subscribers who can select what information they wish to receive.

The problem is to decide which new systems will eventually prove financially viable – and how long it will take for this to happen. Engineers, not unnaturally, tend to be anxious to press forward with all technologically-feasible systems; accountants are often less sure. Politicians, social scientists, market researchers, all tend to jump on and off the new technology bandwagon. In the long run it is the consumer who decides whether a new service is worth acquiring, though Government can influence this by fiscal measures such as those by which DTI have aided teletext.

Predicting success

Richard Ducey of the United States Department of Telecommunication has recently published (*IEEE Trans on Broadcasting*, Vol. B-C, No 2, June 1983) a serious attempt to provide a simple model to predict the take up of broadcasting innovations by relating technical attributes to user needs, stressing that innovative services are often constrained to the extent which technological features of these services are able to correspond to the expectations and needs of users. Prediction models, admittedly, seem sometimes to stress the obvious: for example, "If the innovation sells well, it is considered a success; otherwise some modifications may be needed". Nevertheless as increasingly we enter an era of options, refinement of prediction techniques for new technologies become increasingly important to both industry and engineers. Market researchers still come up with dramatically opposite predictions. A few years ago *IEEE Spectrum* devoted an entire issue to major electronics projects that flopped ingloriously, such as video telephones. Currently the video disc and even digital-audio discs are struggling. Surround-sound comes and goes. Yet v.c.r. machines and portable audio have surprised many by their enormous take-up.

It has been estimated that the free-world market of consumer electronics has risen in a decade from about US)10-billion to over $50-billion, but it would be dangerous to assume that by 1992 it will be $250-billion!

Briefly noted

CBS has dropped its support for the NHK 1125-line, 60-field, 5:3 aspect-radio standard for high-definition tv in favour of a proposed compatible 525-line/1050-line, 60 Hz system fitting into two frequency channels. In effect one channel carries 525-lines with the usual 4:3 aspect ratio; the second an interlaced 525-lines with 5:3 wide screen aspect-radio. It needs a large digital memory to put the h.d.t.v. picture together (with lower resolution at the edges).

The American semiconductor industry is likely to accept two proposed new standard voltages for i.c. devices not able to withstand the electric field stress of 5V supplies: 3.3V±0.3V for devices powered by a regulated supply and 2.8V±0.8V for battery-powered devices.

FCC has allocated 44.20 MHz and 45.90 MHz for civil meteor scatter communications by private systems with 42.40 MHz and 44.10 MHz for common carrier stations in the USA. Since these frequencies are fairly close to low-band v.h.f. television, FCC has warned that the possibility exists of intermittent interference to television reception on Channel 2 (54-60 MHz), and has stressed that the stations will operate "under a developmental grant policy to insure that the expanded use of this new technology does not cause harmful interference."

Trio-Kenwood, well known Japanese supplier for the amateur radio market, has entered the commercial, two-way, mobile field with models providing up to 50 watts (v.h.f.) or 40 watts (u.h.f.) output.

AMATEUR RADIO

Two years of UOSAT

Even with the passing of the second anniversary of the launching of the University of Surrey's UOSAT on October 6, 1981 it appears to be still too early to evaluate fully the successes and failures of this first British experimental space satellite in the amateur radio service. It seems increasingly unlikely that any clear pictures of the Earth taken with the c.c.d. camera will ever materialize, although the camera is known to be working. On the other hand the "packet" data transmission experiments have worked well. Of the four h.f. beacons, only that on 21 MHz has been reported, although telemetry shows that the 7, 14 and 29 MHz beacons are working but apparently experiencing aerial problems. In general the university team has been able to carry out many of the planned experiments, although the absence of any communications transponders has inevitably restricted the amount of active participation by radio amateurs.

Oscar 10, the first successful Phase III high-altitude satellite, has now settled into its orbit with an apogee of 35,000 km, perigee 3958 km, inclination 26.2° and is providing many long-distance contacts.

Flares & Sporadic E

In *Nature* (Vol. 305, September 22, 1983) scientists at the University of New Hampshire and at Nobeyama Solar Radio Observatory in Japan describe in great detail the two intense solar flares that occurred on June 7 and 21, 1980. During these flares, virtually simultaneous acceleration of electrons and ions were noted, in direct contradiction to widely accepted concepts of solar flare particle acceleration. It seemed worthwhile checking back to see whether these unusual flares resulted in any unusual radio propagation. In practice, Sporadic E was observed on frequencies as high as 144 MHz three days later on June 10, and there was also 50 MHz SpE for several days after June 24, again three days after the flare. However as there was also 144 MHz SpE on July 10, the correlation, although interesting, is far from conclusive.

The Raynet amateur radio emergency organization has agreed to recommend to its members that they should conform with the IARU 144 MHz band-plan which allocates 144.845 to 144.875 MHz for beacon operation. For several years there has been considerable Raynet activity on 144.875 MHz and it is hoped this will cease from the end of this year. The RSGB is to seek frequencies specifically for Raynet and emergency use.

Problems have also arisen over the use of 29.3 to 29.7 MHz for f.m. operation based on modified 40-channel c.b. equipment. This is conflicting with the use of the segment 29.3 to 29.55 MHz for the amateur satellite down-link band. The RSGB is asking that this segment be kept clear of terrestrial signals at all times. At the next IARU Region 1 Conference the society will propose a 28 MHz sub-band specifically for f.m. and repeater operation. Many reports of abuse of the South London 144 MHz GB3SL repeater continue to be received, both in the form of deliberate interference and highly offensive language. It is difficult to understand why this problem has existed for so many years on this particular repeater, with relatively few serious problems on the many other repeaters now operating throughout the country.

Here and there

Early morning, November 28, 1983, is the 60th anniversary of the historic first two-way transatlantic contacts on short-waves (actually about 110 metres) between the French pioneer amateur Leon Deloy in Nice and three American amateurs John Reinartz, Ken Warner and Fred Schnell, the result of several months of preparations. Deloy later helped Jack Partridge, G2KF to get across to Ken Warner on the morning of December 8, 1923 for the first USA-UK amateur two-way contact.

Chairman W. N. Craig, G6JJ reports a highly successful 1982-83 year for the Radio Amateur Invalid and Blind Club which by means of volunteer "representatives" helps its members enjoy the hobby by assisting with equipment, installing it where necessary and keeping it serviceable. During the year there were 217 new members and 36 new representatives. Members acquired 40 more Class A and 55 more Class B licences. Enquiries or offers of help always welcome (Hon. Secretary, Mrs Frances Woolley, G3LWY, 9 Rannoch Court, Adelaide Road, Surbiton, Surrey).

The RSGB has approached the Department of Transport about the possibility of British amateurs using their callsigns as vehicle registration numbers. This has long been possible in some American states, although Canada insists that any vehicle bearing a callsign-type number plate *must* be carrying two-way radio equipment when it enters Canada, on the grounds that the police and public have come to recognise call-sign number plates and may seek emergency communications.

Guernsey Amateur Radio Society won the "Golden Jubilee" 50th RSGB National Field Day Trophy. The VHF National Field Day (open section) was won by the HADRABS and Addiscombe Contest Group. An increasing number of NFD contestants now operate from caravans, car-campers etc, rather than tents. In the south of England lightning and static-charged rain caused considerable damage to solid-state equipment.

In brief

World records for both the 10 GHz (1621 km) and 1.3 GHz (1963 km) bands were established by IoSNY/EA9, an Italian amateur visiting Ceuta, Spanish Morocco last July by two-way working to Italian stations in Sicily and the Italian mainland, further evidence of the long ducts that often form above the Mediterranean . . . Class B licences with the new G1 callsign prefix began to be issued about August and by October were well into the G1B series.

PAT HAWKER, G3VA

The Fowberry energy saver

A device to help reduce the effects of a crude on-off thermostat on the cost of running a central-heating boiler.

All boilers demonstrate inertia, and inertia means a time-lag in the feedback of information from the thermostat to the burner. By the time the burner has heated the water-jacket, and the water jacket has heated the water, and the water has heated the thermostat sensor, the burner finds out too late that it should have turned off, and burns too long by the length of the time delays. The result is what is called "over-temperature", and it occurs every time the boiler cycles on and off. Because it is essentially a time function occasioned by the thermal mass of the system, it does not matter how efficient the boiler may be, nor how little back-lash the thermostat may have, over-temperature must inherently occur unless a crafty means is used to prevent it. If a room sensor is used, extra time-delays make things worse.

Over-temperature wastes energy in precisely the same way as an over-heavy foot on the loud pedal of a motor car – it causes too much acceleration in the system: we must try to make the boiler do a constant 56 m.p.h. rather than simulate driving in town!

The Fowberry Energy Saver operates along entirely different principles to the multitude of proprietary timer-programmers which merely tend to stop the boiler working at all for certain periods of time, so tending to make *you* a slave to *them*: they also let things cool down so that the boiler has to work hard to bring temperatures back to normal. This effect will be well known to those who have used a holiday cottage or farmhouse at weekends only – the boiler goes like the clappers from Friday night to Sunday night, and the place is just beginning to get warmed through when it is time to go home!

With the device described, the effects of insulation and normal operational thrift are actually increased, and the saving available is even greater if there is a secondary form of heating such as a back-boiler to a solid fuel fire, or solar panels or whatever, because under these circumstances the boiler is literally allowed to tick-over rather than give the minimum burn length (caused by the time delays) each time it cycles.

Figure 1 demonstrates the manner in which the boiler output temperature is reduced (i.e., cutting out over-temperature) with increased setting of the control knob on the device but the thermostat setting fixed.

by J. A. MacHarg

Figure 2 demonstrates the way that the boiler cycling is reduced with an increase of temperature from a secondary source of heat fed into the system.

Principle of operation

Essentially, what the device does is pulse the burner during the on-periods of the thermostat, the rests between the pulses giving time for the heat to transfer towards the thermostat sensor, the last pulse tending to "just" turn off the thermostat rather have it kicked off by a mighty over-burn of energy.

The thermostat off-time is a fair measure of demand in the system: this is sensed by the device and the length of the first pulse is modified accordingly in order to cope with demand if it exists: if there is only low demand, perhaps from system losses, the first pulse will be short. Whatever the demand may be, subsequent pulses reduce in length so that the thermostat is "just" tripped off.

If the thermostat is not tripped off within about a quarter of an hour, an over-ride comes in to increase gradually the length of the pulses, so to cope with unexpectedly high demand.

Circuit description

The stabilized power supply lights Led_1 through R_{17} whenever the device is powered by the system thermostat: this led therefore announces "Thermostat On".

The relay, with its coil shunted by the mandatory diode D_5, pulses the burner during the thermostat "On-periods".

Whenever the device is powered by the thermostat, C_2 is charged through R_2 up to the level of D_{14}, the transistor being held off by D_3. Each time the thermostat switches the device off the transistor conducts, charging the memory capacitor C_3 through D_4. The slow draining of this capacitor through R_4, D_{11} and D_{12} effectively measures the thermostat "Off-time" and thus the demand in the boiler system.

In IC_1, a dual j-fet op-amp; the right half is a follower, following the voltage on C_3 without loading it, while the left half operates as a phase-changer cum amplifier cum level-shift, supplying the charging voltage for the twin timing capacitors C_7-C_7 as a function of the thermostat "Off-time" and thus in accordance with demand.

The left half of the 556 timer IC_2 pulses the relay in accordance with the time taken to charge the twin timing capacitors C_7-C_7, the relay reset times being set through R_{16} and the manual control R_{19} when the output of the timer is low. During the discharge of C_7-C_7, the charging voltage is cut off because IC_1 is fed with power through D_{10}.

The right half of IC_2 is a level-controlled Schmitt trigger whose input is determined by the voltage across C_6. Each time the device is turned off by the thermostat, C_6 is discharged through D_8 so that it may start to charge from scratch each time the device is turned on. This is the over-ride: if the device is not turned off within about a quarter of an hour, the Schmitt output goes high, and slowly re-charges the memory capacitor C_3 through D_6 and R_5, at the same time lighting D_{16} through R_{18} as a warning that the over-ride is in operation.

The dual switch S_1-S_2 is only used for testing purposes and serves to shorten the otherwise very long time-constants: test point TA allows testing of the follower, while test point TB allows testing of the left half of IC_1. The operation of IC_2 may be heard through the clicking of the relay. Components not discussed, such as the two Zener diodes, D_{14} and D_{17}, are merely level-setters to ensure correct operation of the circuit.

Connection and adjustment

Connection to the boiler is extremely simple: the lead supplying power to the burner from the system thermostat is broken. The lead from the thermostat is fed to the "Live-in" terminal, while the "Live-out" terminal is connected to feed the burner. Neutral and Earth may be picked up from any convenient point.

To adjust, the knob should be turned as far clockwise as possible so that D_{16} only lights under conditions of unusually high

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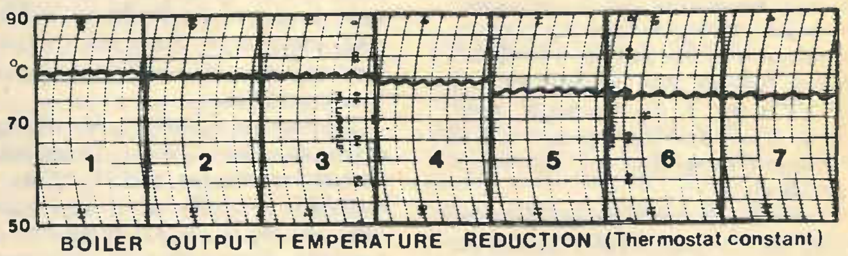
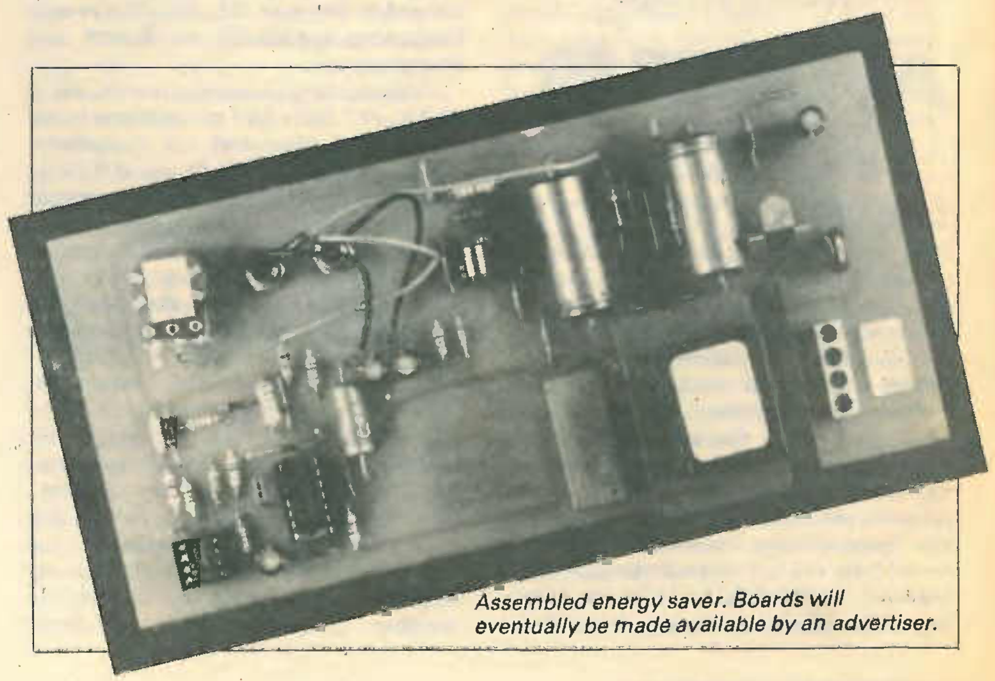


Fig. 1. With the thermostat fixed, the boiler output temperature is reduced as the energy-saver control is increased, indicating that over-temperature is decreased.



Assembled energy saver. Boards will eventually be made available by an advertiser.

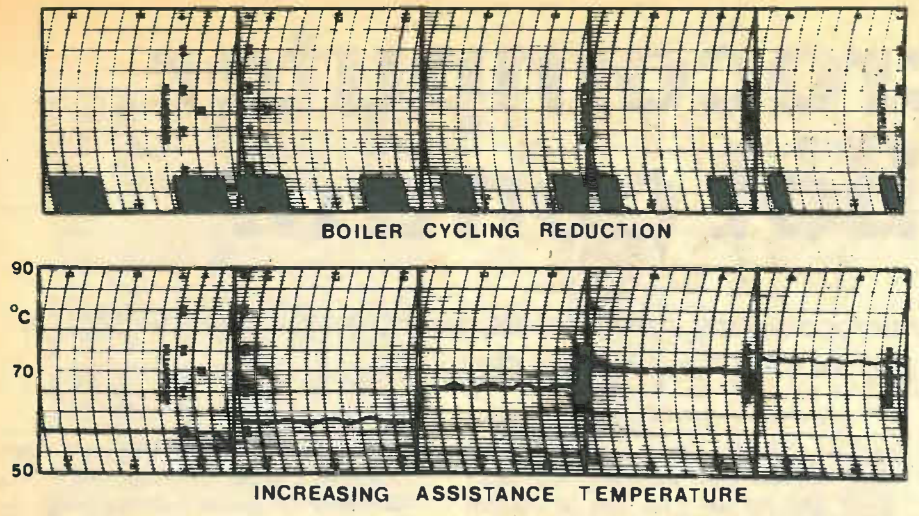


Fig. 2. As the secondary heat source is increased, the boiler 'on' time is reduced accordingly.

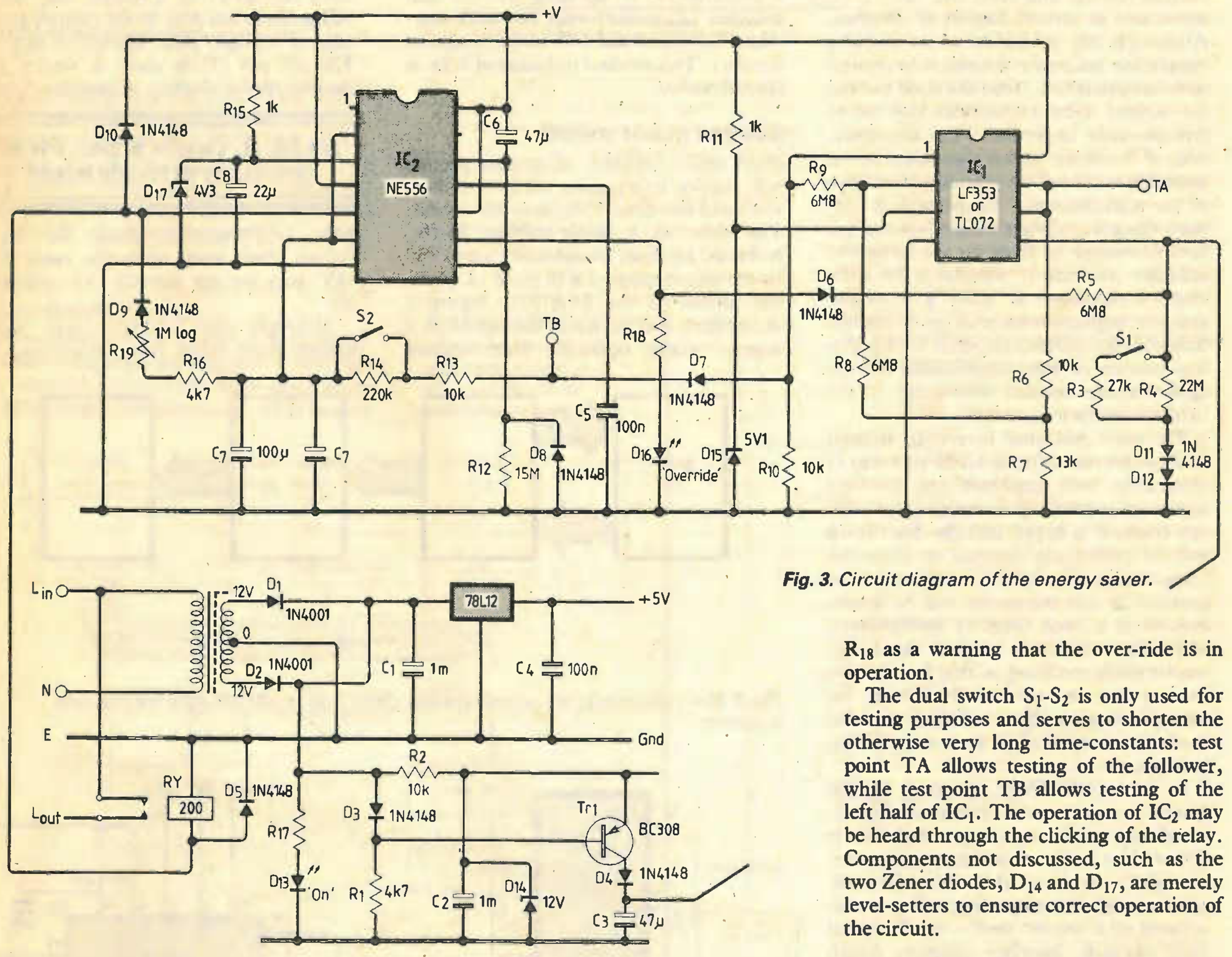


Fig. 3. Circuit diagram of the energy saver.

Microcomputer robot control

Morris Driels describes the microcomputer control of stepper motors, using a 6522 v.i.a. and SAA1027 motor-drive circuit

It is now relatively inexpensive to purchase small, non-servo-type robot manipulators for a variety of educational, research and small assembly activities. These machines are invariably activated by means of stepper motors and have the facility for movement in several degrees of freedom. Although the manufacturers usually supply the necessary interfaces to control their manipulators, there are good reasons for serious users to consider the use of custom-made controllers: the incorporation of feedback sensors to assist in an assembly task requires intimate knowledge of the manufacturers' hardware and software designs; existing controllers are not flexible enough to allow for the control of auxiliary machinery, whether it be additional manipulators or "hard" automation; and the implementation of more sophisticated robot movements such as straight-line motion or joint-interpolated motion again require detailed knowledge of the hardware/software interface.

The work described here is an attempt to illustrate one solution to the problem of integrating both hardware and software aspects of controlling a stepper-motor-driven robot. It is hoped that the describtion will be sufficiently detailed to allow the construction of a specific device, yet be general, so that the design can be implemented in a wide range of manipulators and microcomputers. Indeed, the design can be easily modified so that it will drive devices that are not strictly robots, for example numerically controlled machine tools, programmable data acquisition systems, etc.

A functional block diagram of the system components is shown in Fig. 1. Flexibility in the computer/robot link is achieved by means of an interface adaptor, essentially any device that will make available one eight-bit output port. This article is based on a specific device, the Rockwell 6522 versatile interface adaptor, which allows any 6502 based microcomputer to control the robot. Those familiar with the device will know that it can do a lot more than provide one output port, even though in this application that is all that is required of it. 6800 based systems could utilize the 6821 p.i.a., while those who prefer a Z80 system would implement the interface using the Z80 p.i.o.

Figure 2 is a diagram of the 6522, indicating the required connections to the external computer. Of the two parts provided by this device, only part of port A is used, allowing the remaining lines to be used for additonal i/o; for example, to feed back the arm joint positions. The chip-select lines on the v.i.a. can be enabled either by directly decoding the address bus using nand gates and inverters, or by using a combination of decoding devices and switches to memory-map the 6522 anywhere between 0 and 64K in the computer memory. This method is discussed fully in the reference.

Stepper motor control

Most major suppliers of stepper motors will supply information on how motors work and also circuit boards to drive them. The drive of a single stepper motor, however, has been considerably simplified by the introduction of a 16 pin d.i.l. package known as the SAA1027. Figure 3 shows how this device is connected to a stepper motor operating from around 12Vd.c., requiring only two input signals. The direction pin (3) determines in which direction the motor will step; logic high will produce a clockwise rotation while logic low produces anti-clockwise rotation. With the direction specified, the motor will perform one step on the positive going edge of a single pulse applied at pin 15. The set pin (2) is used to restore the stepper motor shaft to a known orientation.

by M. R. Driels B.Sc., Ph.D
University of Rhode Island

tion. Unfortunately, since the input voltage levels must be in the range 7.5-18V, they are not directly t.t.l. compatible.

Although the SAA1027 will drive motors much larger than those found in any educational robot, even larger motors are handled by incorporating a power amplifier stage in the four phase lines Q_1-Q_4. Figure 3 indicates that the complete motor/driver combination may be treated as a 'black box' requiring only a d.c. level and sequence of pulses to produce a movement.

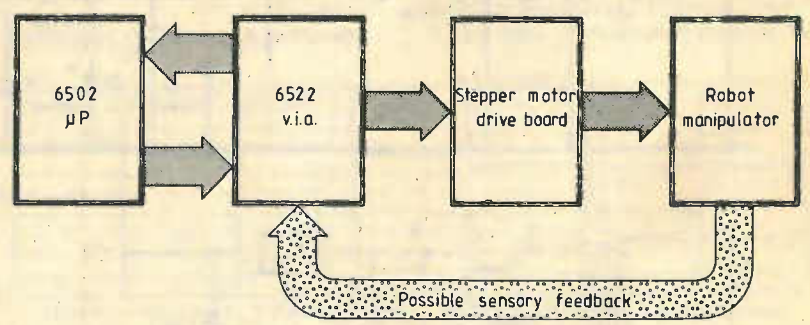


Fig. 1. Block diagram of the control system. Other micros will use different interface adaptors.

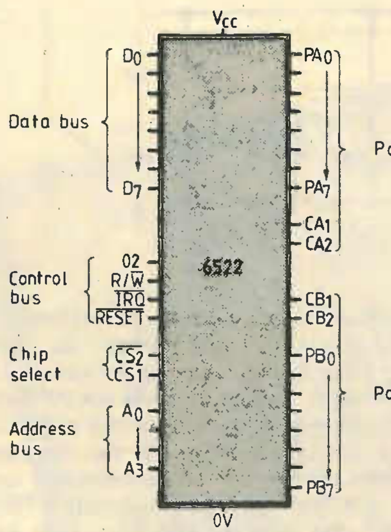


Fig. 2. Rockwell 6522 verstile interface adaptor. Only port A is used in this application.

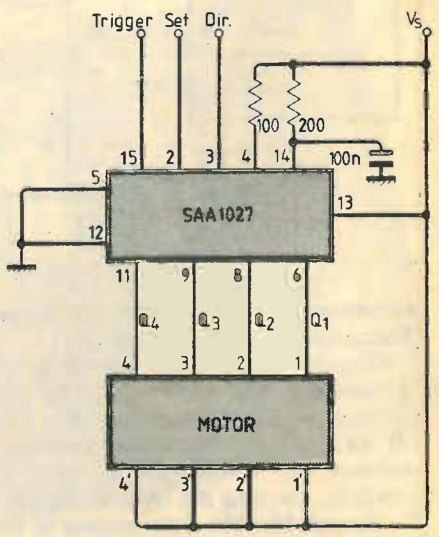


Fig. 3. Using a SAA1027 to control a stepper motor.

Motor/dir.		PA4	PA3	PA2	PA1	PA0	Decimal val.
1	for.	1	1	0	0	0	24
	rev.	0	1	0	0	0	8
2	for.						25
	rev						9
3	for.	1				0	26
	rev	0				0	10
4	for.			0			27
	rev.			0			[illegible]
5	for				0	0	28
	rev				0	0	12
6	for.	1	1	1	0	1	29
	rev.	[illegible]	1	1	0	1	13

Fig. 5. Table showing set of all numbers needed to operate joint motors.

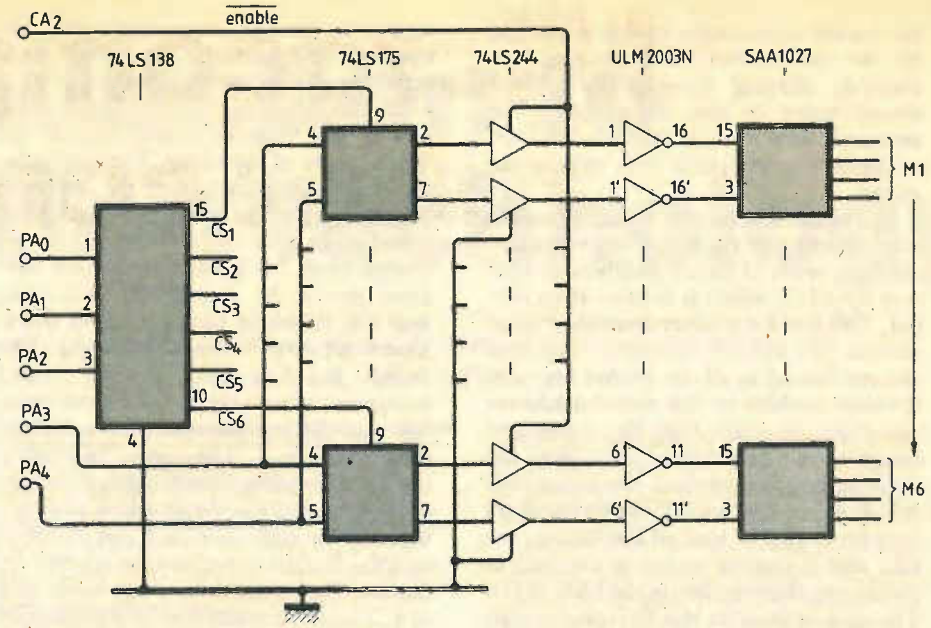


Fig. 4. Six-channel motor drive. ▶

Six-channel driver

This circuit, shown in Fig. 4, uses port A of the 6522, although only part of this port is actually used. The basic operational philosophy is that the six 74LS175 latches

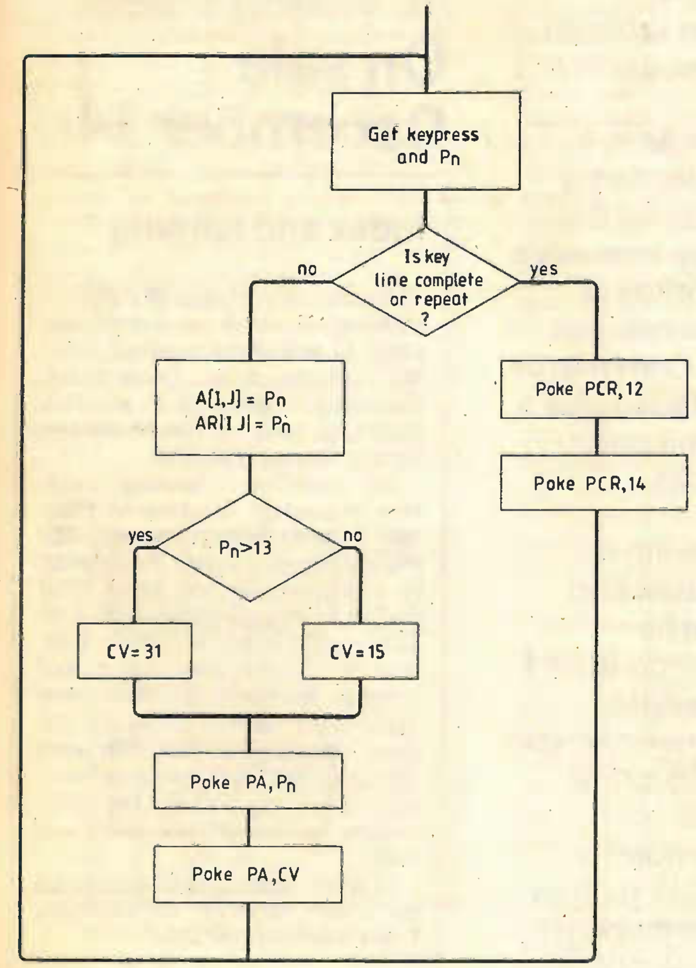


Fig. 6. Flow chart of 'teach' part of program, using keyboard to store movements in A.

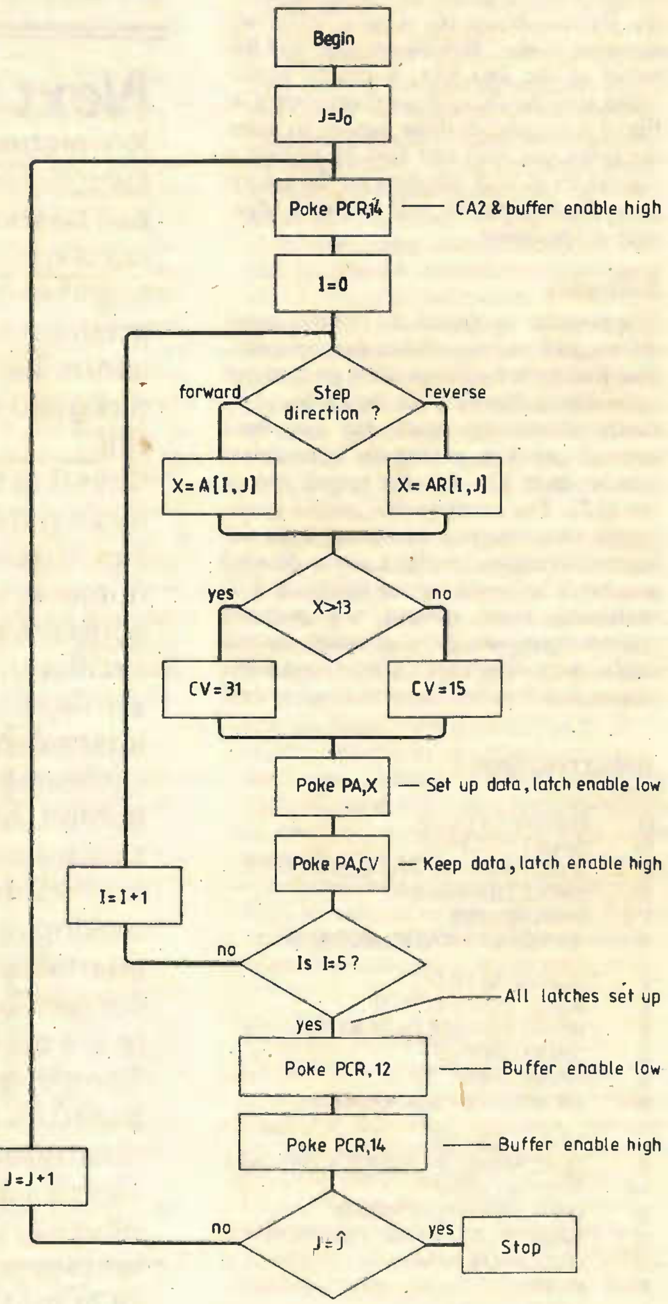


Fig. 7. Flow chart for 'run' mode, where A or AR control motors.

are loaded sequentially with data relating to the six motors. Buffers are then enabled, allowing those motors which should move to step accordingly. The process is then repeated until the required manipulation sequence has been completed.

In a more detailed look at the operation, it can be seen that the motors are moved by placing a series of binary numbers on port A of the 6522, which is defined as an output. This five-bit number consists of three address bits and two data bits. The data bits are bussed to all the latches but only the latch enabled by the decoded address bits stores the data. One bit of the data relates to the direction of step while the other determines whether the motor will step (high) or not (low). Once six numbers have been used to load all the latches, the CA2 line is toggled to enable the buffers connecting the step data to the SAA 1027s. The data relating to the direction is connected to the motor drivers through permanently enabled buffers. All buffer outputs pass through the ULM 2003N Darlington arrays to achieve the necessary voltage levels required by the motor drivers. By considering the range of addresses accepted by the 74LS138 decoder, and the values of the data bits, it can be appreciated that the decimal numbers shown in Fig. 5 represent all those needed to move the robot one step and that by placing a succession of such numbers on the output port, the manipulator will execute a sequence of operations.

Software

The program to operate the robot is menu driven, and can be considered in two parts. The first twelve options allow each motor to be driven directly from the keyboard by firstly identifying which key has been pressed and then poking the appropriate number from Fig. 5 to the output port of the 6522. For example "Q" might correspond to movement of Motor 2 in the reverse direction, resulting in the decimal number 9 being sent to the interface. The remaining eight options are program control characters, most of which are self explanatory. The 'line finished' command allows simultaneous movement of several motors by moving them sequentially and then typing F, indicating that the preceding operations are to run in parallel.

The flow diagram shown in Fig. 6 is the part of the program which controls the 'teach' mode of operating. The manipulator is driven directly from the keyboard and in doing so the motor movements are stored in an array A. At the same time a reverse array AR is computed. Each keypress moves the appropriate motor one step and allows for multiple motor movements per step as described above. The 'repeat' key may also be used for rapid movement of one motor. The reverse array AR uses the complement of the decimal value stored in A. The reason for compiling AR is that many robot applications are of the 'pick and place' type where an object is picked up from location x and placed at location y. Before performing another sequence, the manipulator must move back to x. The movement from x→y is specified by A while that from y→x is defined by AR. For example, if one of the forward steps is the clockwise rotation of the hip joint, A would use the number 29 while AR would contain 13. Once the sequence has been stored, the arrays can be inspected and edited (D), restarted (Z) or saved on tape or disc.

Executing the movements is handled by the 'run' mode of the program shown in Fig. 7. In this mode, either array A or AR is used to load the latches shown in Fig. 4 and cause rotation of the motors. Most of the program steps should be self explanatory. The only complication arises over the variable CV. It is necessary to present the correct data at the latch input while the clock (pin 9) signal performs a low to high transition. By pokeing CV to the latch after the data variable x, this is achieved and the correct data is clocked into the latch.

The program shown in the flow diagram was written in Basic and found to run fast enough in the teach mode though not in the run mode. The program was subsequently compiled and found to operate at an acceptable speed in both modes. WW

Reference

Microcomputer interfacing for 12 bit data acquisition, *Wireless World*, M. R. Driels, vol. 89, Feb. 1983, pp. 49-52.

OPERATING MENU

Q	ELBOW EXTEND
W	WRIST PITCH UP
E	WRIST ROTATE ANTICLOCKWISE
R	SHOULDER DOWN
T	HAND CLOSE
Y	HIP ROTATE ANTICLOCKWISE
1	ELBOW RETRACT
2	WRIST PITCH DOWN
3	WRIST ROTATE CLOCKWISE
4	SHOULDER UP
5	HAND OPEN
6	HIP ROTATE CLOCKWISE
F	LINE FINISHED
Z	ZERO MEMORY BLOCK & RESTART
M	DISPLAY MENU
D	DISPLAY DATA STORED
B	BACK TO STARTING POSITION
V	QUIT PROGRAM
G	RUN
L	LOOP OPERATION

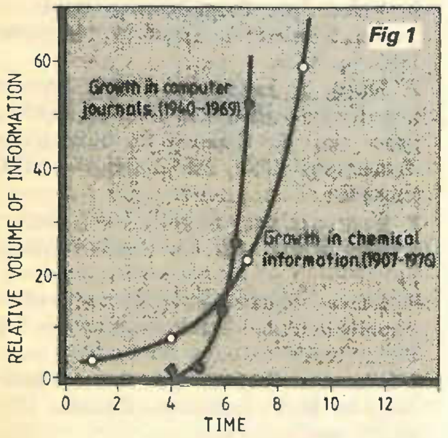
Introduction to information technology

"Much future learning must take place in the home if government expenditure on education is to be reduced in a non-harmful way."

by Philip Barker

Information is derived and generated from a multitude of different sources, but undoubtedly the largest volume of new information is generated from research activity, the object of which is to solve some of the problems that confront society. Of course it is also possible to produce new information from existing material through the application of a variety of hardware and/or software processing techniques. These simply transform information in one form to an alternative representation in another. But unfortunately, information produced in these ways is often both costly and time consuming to produce.

Because of its cost, new information has to be stored in appropriate archives and libraries for use by others. Each year the volume of stored information increases substantially. It has been estimated that the volume of recorded knowledge doubles roughly every 20 years. This effect is seen by examining the graphs shown in Fig. 1. The first curve, indicated by open circles, represents the physical volume of the collective decennial indexes to a research publication called *Chemical Abstracts*, produced by the American Chemical Society. The graph covers the period 1907 through 1976. The second curve, indicated by filled circles, shows the growth in the number of computer journals for the period 1940 to 1969. Although each curve covers a slightly different period and relates to different subject matter, both show a similar exponential shape. One of the main objectives of research and development in information technology is to provide techniques and equipment capable of helping to control this 'information explosion'. Some of the more important areas of current research interest are briefly outlined below.



Electronic journals

There is much to be said for information that is held in electronic form. In addition to being compact, it is also easy to disseminate and simple to up-date. Because of the importance of holding information in this way, much research has been devoted to investigating the use of the electronic journal and book as a means of distributing reference documents and the results of research activity.

The basic idea behind the electronic journal is fairly straightforward and depends on the availability of appropriately designed communication networks, database support software and text/image processing equipment. Essentially, contributors enter their source material via suitable computer terminal equipment. Once a document has been entered into the storage system (a distributed database), documents may be modified and updated in various ways prior to submission to the journal's editorial panel. An electronic version of the manuscript is then referred and provided it is accepted for 'publication' is then stored in the centrally accessible portion of the distributed data base. Potential users of the final report are then made aware of its existence and may gain access to it by means of interactive terminals linked to the host database with appropriate communication linkage.

Provided suitable selection mechanisms, information filters, and security procedures can be designed, the electronic journal concept is likely to offer a significant contribution toward solving some of the problems with which information technology is concerned.

Potential of the video disc

When combined with a suitably designed computer control system, optical disc equipment can make available a number of novel solutions to many of the problems of information storage and retrieval,[1] but at present there are several limitations. They are read-only; discs must be loaded by their manufacturer; they are costly to produce; no standards exist to enable disc exchange schemes to operate; they are not yet commonly available; and, they are difficult to author. Currently, there is much research being devoted to solving each of these problems and when solved the optical disc will undoubtedly provide many new opportunities for designers of information systems. The impending development of the 'intelligent video disc' is likely to offer many fresh possibilities[2] for those who are interested in the construction of novel i.t. products for use in the home, industry and within education.

Satellites and fibre optic networks

Two types of communication resource are very likely to significantly influence developments in information technology over the next decade: optical fibres and satellite systems. Recently, there has been much discussion regarding the possible 'rewiring of the UK' using optical fibres to provide high bandwidth communication channels able to support interactive tv, electronic shopping, meter reading, home security systems and other computer-based services for use in the home. Within many parts of the world the use of satellite data communication links are well established and there are now several worldwide data transmission networks in which satellites play a significant role.

Combining both of these technologies is likely to produce a completely new range of possibilities for users of information technology. Heterogeneous systems[3] constructed from local area networks based on optical fibres and global communication provided by satellites will undoubtedly provide many new approaches to work, leisure and education, particularly within the home. Indeed, to combat the rising costs of travel and office accommodation, as well as over-crowding within cities, working from home through the use of appropriately designed workstations is likely to become increasingly important in the future, as will be the development of home-based educational systems.

The role of education

Education is intimately concerned with information, its dissemination and assimilation by individuals, groups, societies, and nations. As an information technology tool, education thus has a vital part to play. Its role in relation to the production of information via research is depicted in Fig. 2, which illustrates the type of information/knowledge transfer processes that are

Dr Barker is in the department of computer science at the Teesside Polytechnic.

characteristic of most primitive educational systems. Knowledge and information are produced by subject experts such as researchers and scholars. Teachers assimilate this knowledge and pass it on to learners or students. Clever students may be capable of assimilating this knowledge for themselves – once they have achieved a particular threshold age.

Within Fig. 2 it is easy to see that two types of entity are of crucial importance to the process of educational information transfer: teachers and students. Within some Universe of Discourse, a teacher is regarded as being information-rich. In contrast, a student is one who is thought of as being information-deficient within this domain. The function of the teaching process is to transfer information from the teacher to the student. In the past, large mainframe and minicomputer systems have been used to implement computer-based teaching processes, severely limiting the potential that these techniques are able to offer. Nowadays, easy access to microcomputers, intelligent terminals and communications facilities, particularly within the home, is likely to provide many new opportunities for the use of such approaches to education. One of the most interesting of these will probably arise through the development of expert systems[4].

An expert system is a sophisticated software package that is able to support two basic types of human-computer dialogue. One of these (knowledge acquisition) is essentially an input operation while the others (information transfer) is primarily dedicated to output operations. During the input dialogue a human who is expert in a particular subject area 'converses' with the computer that hosts the software package that constitutes the expert system. This conversation enables the human expert to pass over to the computer software a subset of knowledge and decision-making expertise. The computer then constructs a knowledge base and a set of rules that together embody the information that has been acquired from the dialogue. The rules that are deduced by the system are important because they describe how to use the stored knowledge/information in different types of situation. Both the rule set and the knowledge base are adaptable – that is, they can be dynamically modified as a result of further interaction with the subject expert.

The second type of dialogue (information transfer) is essentially informatory. It enables the stored material embedded within the expert system to be used as a means of solving problems posed by its user. These problems will usually involve some form of decision making. If it is required, the software will provide an explanation as to how and why it has made particular decisions. The machine can thus be used to display its 'thought pattern'.

The potential role that expert systems could play within education is substantial. For example, they could be used to construct intelligent tutors and counselling aids; to build systems that are capable of training people in decision making; and they could form the basis of many new i.t.

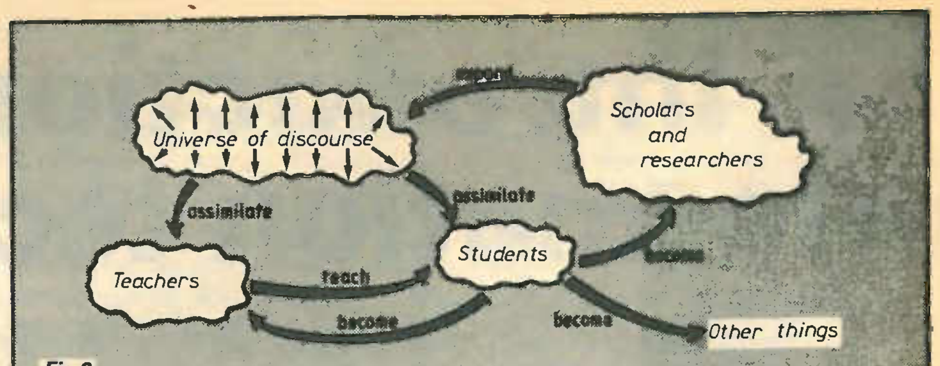


Fig 2

products for use in the domestic marketplace and in home-based education. Products might include expert systems to help people work out their tax returns, claim social benefits and provide sources of advice on problems arising in cooking, gardening, home maintenance and a host of other mundane educational problems inadequately catered for by conventional approaches to education. Indeed, combining expert system technology with that of the video disc could provide a powerful new educational medium for use in the home – an area where much future learning must take place if government expenditure on education is to be reduced in a non-harmful way.

The future

Undoubtedly, information technology as we perceive it today is going to have a significant impact in the future. Its greatest effects will be on people and the nature of the lives they lead. People spend a large proportion of their time in their homes and it is here, therefore, where many new market opportunities for i.t. products will probably arise. During the next decade the home is likely to change in many subtle ways as novel domestic i.t.-based services are made available. Four factors are likely to contribute to these changes: easy access to electronic information via computer networks; the introduction of new storage media such as optical discs; highly intelligent software that reacts to user demands made via easy-to-use human-computer interfaces.

We are already experiencing a steady increase in the number of microcomputers that are available for home use. When combined with communication networks and video disc facilities, completely new horizons in home i.t. are likely to emerge – not only home shopping, interactive tv, intelligent video for home instruction but hosts more. Perhaps one of the most frightening possibilities is that presented by 'electronic democracy' – voting (or decision making) on issues of local and natural interest by means of a keypad located in each home. If the potential offered by this is to be successfully and intelligently used then the future role of education is extremely important. If education in a democratic society has to have as its first objective the training of students "for an active role in which the individual takes responsibility for his/her own destiny", then people must be given the opportunity of becoming informed about and deciding on those issues that directly influence their lives. Through new technology we are moving closer to this. However, there are still many social and cultural problems that remain to be solved, many of which stem from ignorance and a fear of technology. Education has much to achieve.

Naturally, one of the greatest fears at present is the effect that information technology might have on employment. In the guise of automation, we cannot do other than believe that i.t. can bring substantial reductions in the workforce of those areas where it is applied. So, where will the future lie for those who are dispelled from work? Stonier believes that one of the biggest employers in the future must be the 'knowledge industry'. If research is included in this category then this must be true. For where else might the future of the UK lie? The nation must therefore further promote and exploit the excellent research done in British institutions. Without this, and the support that i.t. can provide, will there be a future for the UK?

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Instability at h.f. in feedback amplifiers

Simple mathematical analysis of the conditions for high frequency instability in a feedback amplifier or any abstract control system

by Philip Ratcliffe

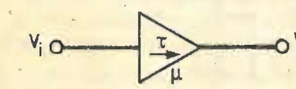
Electronic amplifying devices, valves, bipolar or field-effect transistors, rely for their operation on the drift of electronic charge in controlling mechanisms. The speed of drift of the geometrical size of the devices define the physical limitations to the high frequency response.

In bipolar transistors the high frequency limit depends on the time taken for the drift of physical electrons or energy band holes across the base region. For any useful gain at high frequencies the base region is made very thin, but this has the disadvantage that the device has a very low collector-to-emitter 'punch through' voltage.

For valves and f.e.ts the main current is composed of charges travelling through a homogeneous medium (ignoring the electrode interfaces) but is controlled by electric fields whose influence can propagate faster than any material mediator and so gives a much better h.f. response.

A simple switching analysis is used. The time taken for a control effect to propagate from input to output will be assumed to be constant, τ.

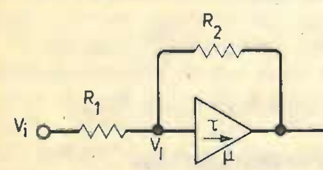
A more sophisticated analysis would consider the electronic drift currents as a diffuse bunch of charges. Suppose that the abstract amplifier has an open-loop gain in Fig. 1



where, by definition of the causal relation, assume that

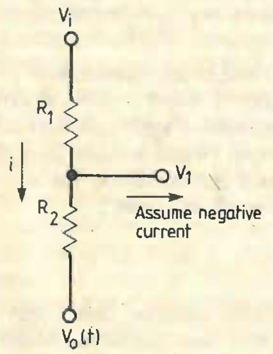
$$v_0(t)=\mu v_1(t-\tau) \qquad (1)$$

and μ can be positive or negative. Apply voltage feedback by a simple resistance network, Fig 2



The resistance chain is an instantaneous voltage dividing system, and in particular, for negative feedback (μ<0) it can be regarded as forming a 'voltage lever' pivoted at the amplifier input v_1.

In the following analysis a simple voltage or Heaviside function will be applied to see how the amplifier responds. Suppose that when the amplifier is created that v_0 has some arbitrary initial value such as zero. When a constant voltage v_i is applied at time t the system will not respond until t+τ. At t the voltages v_i and v_0 on the resistor network interact instantaneously and define the value for v_1 at the amplifier input, Fig. 3



The current in the resistive network, assuming negligible loading by the amplifier input, gives v_1

$$i=\frac{v_i-v_0}{R_1+R_2}=\frac{v_1-v_0}{R_2} \qquad (2)$$

so $$v_1(1)=\frac{R_1}{R_1+R_2}v_i+\frac{R_1}{R_1+R_2}v_0(1) \qquad (3)$$

where the arguments $v_1(1)$, $v_0(1)$ denote the values of these variable voltages during the first period from t to t+τ.

At t+τ until t+2τ the value of the output voltage depends on the value of v_1 given by equation 3 in accordance with the causal behaviour of equation 1

i.e. $$v_0(2)=\mu v_1(1)$$

or $$=\frac{\mu R_2}{R_1+R_2}v_i+\frac{\mu R_1}{R_1+R_2}v_0(1) \qquad (4)$$

This new $v_0(2)$ interacts with the (constant) voltage v_i in the resistance network to produce a new $v_1(2)$:

$$v_1(2)=\frac{R_2}{R_1+R_2}v_2+\frac{R_1}{R_1+R_2}v_0(2) \qquad (5)$$

and at period t+2τ to t+3τ the new output voltage v_0 is

$$v_0(3)=\mu v_1(2)$$
$$=\frac{\mu R_2}{R_1+R_2}v_i+\frac{\mu R_1}{R_1+R_2}v_0(2) \qquad (6)$$

and $v_0(2)$ is given by equation 4 so we can reduce $v_0(3)$ into terms of the arbitrary initial value $v_0(1)$.

The constant factors $R_s/(R_1+R_2)$ and $\mu R_s/(R_1+R_2)$ for s=1,2 occur frequently, so for mathematical simplicity replace them by labels k_s' and k_s respectively i.e. put

$$k_s'=\frac{R_s}{R_1+R_2} \text{ and } k_s=\mu k_s' \text{ for } s=1,2 \qquad (7)$$

then it will be easier to see the build up of the pattern in the voltages.

The recursive relations for the n periods are

$$v_0(n)=\mu v_1(n-1) \qquad (8a)$$
and $$v_1(n)=k_2'v_i+k_1'v_0(n) \qquad (8b)$$

then from equations 8 we obtain the recursive relation for v_0

$$v_0(n)=k_2v_i+k_1v_0(n-1) \qquad (9)$$

This is a Markovian process, familiar in the study of difference equations. It is a simple repetitive updating process, and it can easily be summed if we assume that v_i is a constant (also for certain specific functions). The pattern of the output voltages is a sequence of constant value steps $v_0(n)$ of duration from periods t+(n−1)τ to t+nτ

$$v_0(1)=\text{arbitrary}$$
$$v_0(2)=k_2v_i+k_1v_0(1)$$
$$v_0(3)=k_2v_i(1+k_1)+k_1^2v_0(1)$$
$$v_0(4)=k_2v_i(1+k_1+k_1^2)+k_1^3v_0(1)$$
$$\vdots \qquad (9')$$

In general

$$v_0(n)=k_2v_i(1+k_1+\ldots+k_1^{n-2})+k_1^{n-1}v_0(1)$$

The initial condition $v_0(1)$=arb is propagated through the equations. If $|k_1|<1$ then the amplitude coefficient k_1^{n-1} tends to zero and the initial 'transient' or arb. value $v_0(1)$ becomes insignificant in the successive propagation through the generations and so has little effect on the long-term future of the output voltage of the amplifier for a constant step input v_i. The sum is recognised as a geometric progression and so the general formula can be written

$$v_0(n)=\frac{k_2}{k_1-1}(k_1^{n-1}-1)v_i+k_1^{n-1}v_0(1) \qquad (10)$$

As a simple check, the ratio of terms k_2, k_1-1 'cancel' to give a recursive dimension of n−1 in both coefficients. This equation is the complete switching solution to the feedback amplifier for a step voltage v_i. Now examine this to find the conditions for various modes of operation.

Conditions for special cases

Firstly the feedback system is stable if and only if $|k_1|<1$. If $k_1 \rightarrow +1$ there is uncontrollable growth, which in reality leads to saturation when constrained by finite supply line voltages. If $k_1 \rightarrow -1$ this point on the circle of convergence of the mathematical sequence-generating process of equation 9 leads to switching oscillation in a mode similar to a bistable with an (ideal) frequency of $\nu = 1/2\tau$.

As $n \rightarrow \infty$ for the stable region, equations 9 or 10 give

$$v_0(\infty) = \frac{k_2}{1-k_1} v_i^{(\text{const. step})} \qquad (11)$$

where $|k_1|<1$. The stability condition is equivalent to $|\mu| < |(R_1+R_2)/R_1|$ i.e. the feedback can be very loose, up to open-loop gain. It must not be too strong otherwise it leads to strong self-interaction and instabilities, which in reality are damped and manifest themselves as distortions of the signal.

Substituting into equation 11 for the constants into terms of the parameters of the system using equation 7 we obtain the closed-loop amplification factor as

$$A = \frac{v_0(\infty)}{v_i} = \frac{\mu R_2}{(1-\mu)R_1 + R_2}. \qquad (12)$$

Consider three limiting conditions of the three variables μ, R_1, R_2. First if $R_2 \rightarrow \infty$ then $A \rightarrow \mu$, the open-loop gain as expected. Secondly if μ is very large (and negative only, because of the realy-ly impassible singularity of a pole at $k_1 = +1$) the dominant terms in equation 12 are

$$\frac{v_0(\infty)}{v_i} = \frac{-R_2}{R_1} \qquad (13)$$

where $|\mu| \gg 1$ and strictly $R_2/R_1 > |\mu| - 1$, though in practice this condition is ignored and is only realistically valid for $\mu < 0$.

We recover the usual equation for the negative-feedback 'operational' amplifier but the more general formula 12 also allows for a small positive feedback for *regeneration* as long as $|k_1| \leq 1$ as assumed in this analysis for taking the limit $n \rightarrow \infty$ to be finite gain A. Note that in 12, as $k_1 \rightarrow 1_{(-)}$ the third mode (of regenerative amplification) gives

$$\frac{v_2(\infty)}{v_i} \approx \frac{R_2}{R_1} \cdot \frac{(R_1+R_2)}{[R_1(1-\mu)+R_2]} \qquad (14)$$

for $\mu \leq 1 + R_2/R_1$. The singularity structure for regenerative amplification from 14 can be found if we denote the small linear error in μ from the limiting values as δ, and put

$$\mu = 1 + \frac{R_2}{R_1} - \delta \text{ near singularity}$$

and substitute this into 14 to obtain

$$\frac{v_0(\infty)}{v_i} \approx \frac{R_2(R_1+R_2)}{R_1^2} \cdot \frac{1}{\delta}$$

The $1/\delta$ factor shows that the singularity is a simple pole.

* * *

We can analyse what is happening at the amplifier input v_1 using equation 8b and the general solution 10 for $v_0(n)$. From 8

$$v_1(n) = k_2' v_i + k_1' v_0(n) \quad 0 \leq k_s' < 1 \quad s = 1,2 \qquad (15)$$

where the terms k_s' contain no gain μ so must both be positive, less than unity, by definition 7, for real resistances and the direction of change of $v_1(n)$ is always in the same sense as $v_0(n)$, and the general solution is

$$v_1(n) = \frac{k_2}{k_1 - 1}(k_1^n - 1)\frac{v_i}{\mu} + k_1^n \frac{v_2(1)}{\mu} = \frac{1}{\mu} v_0(n+1) \qquad (16)$$

from 10, which is curious in that it says $v_1(n)$ depends on the future value of $v_0(n+1)$, but as a repetitive causal process it is quite sensible. The limiting condition if $|k_1|<1$ as $n \rightarrow \infty$ is

$$v_1(\infty) \approx \frac{k_2}{1-k_1} \cdot \frac{v_i}{\mu} = \frac{1}{\mu} v_0(\infty) \qquad (17)$$

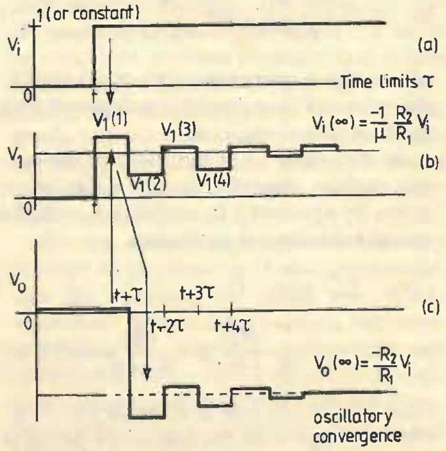
from 11 and in accordance with 1.

Further if $\mu \rightarrow \infty$, $v_1(\infty)$ tends to zero, the direction of approach depends on the sign of v_i in 16 and is a damping effect, and we obtain the condition for the so-called 'virtual earth amplifier'.

* * *

A graphical analysis makes this algebraic description meaningful in considering two special cases, for $k_1<0$ and $k_1>0$ with $|k_1|<1$ assumed throughout this analysis.

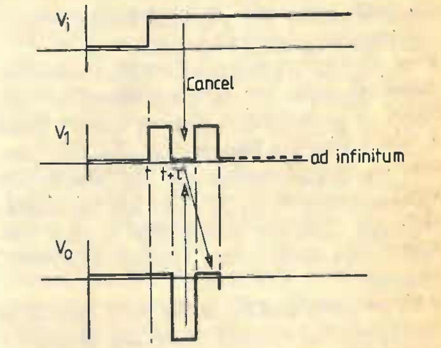
First, if v_i is zero for all time from $-\infty$ up to t we may also suppose v_0 has been zero, say. At t the input voltage jumps to a constant level for the rest of time, Fig. 4(a).



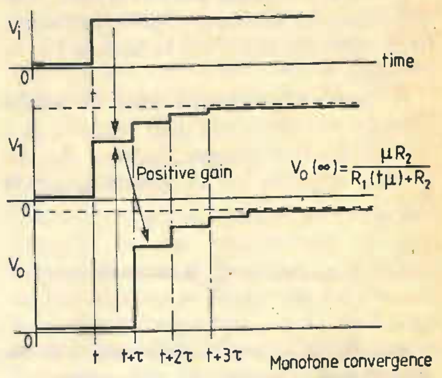
Instantaneously v_1 varies to a value the same sign as v_i. After τ we see v_2 responds overshooting and undershooting the ultimate limiting value. The finite (causal) time delay in negative feedback systems explains the 'overshoot' of the Gibbs phenomenon in Fourier's analysis. In mathematical function analysis we are looking for self-consistently matching or fitting functions using the limiting calculus (when we let $\tau \rightarrow 0$ in continuous functions) and using infinitely many degrees of freedom ($n \rightarrow \infty$) to model behaviour near discontinuities. The condition for stability in negative feedback is

$$-\left(1 + \frac{R_2}{R_1}\right) \leq \mu \leq 0.$$

The condition for switching oscillation is when $\mu = -(1 + (R_2/R_1))$ or $R_2/R_1 = |-\mu| - 1$ then the large value of v_0 exactly cancels v_i on alternate cycles in the 'voltage lever', so that the voltage at the input of the amplifier v_1 switches between values $v_1(1)$ and zero, where $v_1(1)$ is given in 3 and we see that it retains a 'memory' of the arbitrary initial value $v_o(1)$, forever echoing through the amplifier system, Fig. 5 (assuming no dispersive processes as in reality causing a loss of information on the structure of the signal into the noise).



In the second case $k_1>0$ we can obtain finite regenerative amplification under the condition $0<k_1<1$ i.e. $R_2/R_1 > \mu - 1$. The diagrams for the graphical analysis are easier to construct using equation 9:



This illustrates the second type of convergence of mathematical sequences, it can saturate to a finite value or increase indefinitely. The condition is regenerative positive feedback for stability is

$$0 \leq \mu < 1 + \frac{R_2}{R_1}$$

then the closed-loop gain is finite.

Further investigations

The behaviour of time-delayed control can be studied mathematically in computer simulations on the way the system reacts to more varying input functions than a mere step. Results show that the behaviour of the system depends on the character of the signal being processed – look at the response to square waves, sinusoids, etc. which can induce 'resonances' in the am-

continued on page 79

16-line p.a.b.x with options

Incoming and outgoing exchange calls and call transfer are functions of the flexible electronic/electromechanical p.a.b.x described in this second article.

by J. H. Kuiper

This first section completes the description of internal conversation and relies on circuit diagrams published last month.

Because O-relay coil values are only 700Ω, a common limiter resistor is included to keep current through the telephones within acceptable limits; only one O relay operates at a time so a common resistor suffices (470Ω, 1W using a 45V supply). The same applies to the G bus, where a common resistor may be included betwen the G line and contacts gh_2/gi_2 in the external control. Further relay current-limiting resistors should be chosen to suit the relays used, taking into account resistances due to long connecting lines. Using 700Ω relays throughout, typical values are 390Ω, 1W for II, EI, and R relays and 1kΩ, 1W for others using a 45V supply.

Looking at the terminatór, ii_2 like ii_1 has been following the movements of II caused by two pulse trains. With the bistable, output at logic 0 and counter 40161 and decoder/latch 4514 enabled as mentioned, operaton is as follows. Counter 40161 advances on positive going edges while the 4514 decoder/latch requires negative-going trailing edges. Pulses caused by ii_2 are advanced through the counter and then latched in the decoder. After the final pulse in the second train, b_2 closes, preventing further dial pulses from having any effect as the input bistable is locked and the 40161 counter pin 1 is pulled to V_{ss}, forcing it into a 'no-count' state.

The selected latched output of the decoder has gone to logic 1 which drives the connected T relay through its corresponding transistor enabled through b_2. As the dialled station's T relay energizes, its t_1 contact prevents the busy-signal caused by a third party from interferring, similar to the o_2 contact of the calling party explained previously. At the same time t_1 prepares a path from the called station through ri_1 to the reply relay R. Finally, b_2 closing started the ringing-tone oscillator/interrupter, RT. Ringing current is sent to the called party from ri_1 through the selected station's t_1, o_2 and g_2 contacts while the ringing tone is returned to the caller from ri_2, $2eng_2$ and the caller's o_2 and g_2 contacts. Ringing-interruptor relay RI controls the timing of current and tone.

When the called station answers, reply relay R operates by current from ground through the a-line, the called position, its b-line, g_2, o_2 and t_1 contacts and ri_1 through R to V_{ss}. Contact r_1 connects a second holding path for IR and disconnects the ringing tone relay RT which in turn stops the RT oscillator/interruptor through rt_2. The speech circuit between both sets is completed through r_2; operation of r_3 and r_4 contacts will be explained later.

After completion of the conversation both stations replace their handsets. Resetting does not start until both holding paths to IR are broken, i.e. not until both handsets are back in their cradles. Resetting is as follows. Both II and R relays, being disengaged, release IR. Contact ir_1 disconnects all relays held, viz. C, D, E & O, after which e_1 releases the K relay(s). Finally, k_1 prevents the 1-ENG relay from inadvertently operating while k_2 clears the 40161 counter and forces all 4514 outputs low, switching off the T relay. While resetting takes place r_3 helps to prevent relay RT from again starting the RT oscillator in the event of II disengaging long before R. This completes resetting and the system is now ready for accepting and processing the next call.

Both pull-up resistors and the capacitor around ii_2 prevent glitches from ii_2 upsetting the 40161 counter when dialling takes place. The ringing-tone oscillator/interruptor is an adapted version of a circuit previously published (*WW* Feb. 1981 p.63) and consequently produces a BT-type 'double tone' which provides clear distinction between internal calling and an incoming exchange call employing single-tone signalling (one interruption as opposed to the two produced by BT). If the inverse is applicable then the ringing-tone oscillator should be omitted and the 555 dial tone oscillator replaced by a 556 type, the second half of which produces single interruptions for driving the RI relay. Ringing tone to ri_2 then has to be taken through a 100nF capacitor from the new dial-tone oscillator. The change in B_2 and rt_2 contacts is shown separately.

Table 1 lists the 16 outputs of the 4514 latch/decoder and specifies numbers to be dialled to obtain the required output. As a telephone dial will only produce digits one to zero, causing pulse trains of one to ten pulses respectively, and the decoder has 16 outputs, two digits must be dialled to make all 16 outputs accessible. Swedish telephones having dials marked zero to nine will produce one pulse when dialling zero and ten pulses when dialling nine. Basically the combined number of pulses produced after dialling determines the final output of the decoder. Since two digits have to be dialled the first accessible output will be output two when dialling 11 (1+1 pulses). To access outputs zero and one the counter has to overflow, or dialling 60 and 79 respectively (6+10 and 7+9 pulses) produces output zero while dialling 70 or 89 (17 pulses) results in output one becoming logic one. Any appropriate number of pulses will switch the corresponding output. A list of two groups of consecutive numbers is given. If under ten stations will suffice, relays D and B in the internal control may be omitted. Dialling one digit only will now suffice. Note that contact a_2 has to replace b_2 in the terminator and ringing-tone oscillator/interruptor. No further circuit changes are required. Active outputs of the 4514 are now outputs one to A.

Incoming exchange calls

Each telephone connected has to be modified by fitting a ground key and a led. Details are given in a separate diagram for both UK and continental sets. Both the switch and led operate from the red a-line and a total of four wires from each station to the exchange are required, the common a-line at positive potential, the return line b, the ground-key line GK and the status-indicator led line.

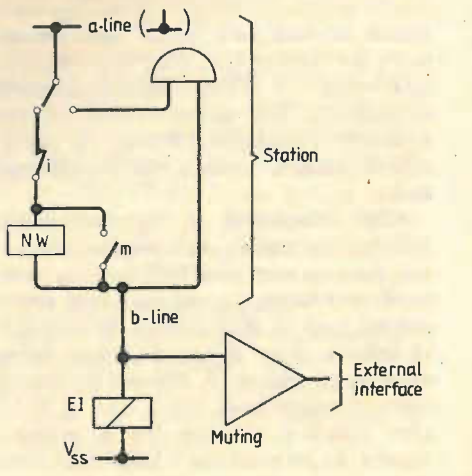
The line interface primarily consists of a remotely controlled telephone in which the cradle switches es, muting contact m and interruptor contact ei are replaced by relay contacts. The exchange line is fully isolated from the internal system. The cradle switches which would normally be operated when lifting the handset are now remotely operated by ground key GK from each of the individual stations through the Ground in and hold relay arrangement GI/GH which is a toggle switch, switching on when closing the station's ground key initially and switching off when the ground key is operated again. Ignoring the condition of 1_1 and p_1 for the moment, switching occurs when the toggle input at n.o. contact of 1_1 is connected to V+ (by operating the gound key). This energizes

G_1 through the diode while at the same time GH will not operate as it is shorted by gh_1. A holding path for GI is provided by gi_1 (through p_1 on to V+. Releasing the ground key removes V+ from the toggle switch input so GH is activated through gi_1 while the diode now prevents gh_1 from shorting the GH coil. Switching of gh_1 takes place to allow for reset. This occurs on a subsequent operation of the ground key which deenergizes and thus disconnects the previous holding path through gi_1. GH is still held from the input through the diode and won't disengage until the ground key is released.

Operating sequence when taking an incoming call is as follows. An incoming call rings the bell from the exchange a-line through a capacitor, $2cs_1$, the ringer and the EB-line which would normally be connected to the returning b-line (all in the line interface). The parallel opto-isolator also detects ringer a.c. and consequently the bell-detector relay BDT switches in tune with the audible signal. In the external control, bdt_1 switches led-switch relay LS and ls_1 connects all leds at the various stations, visually indicating an incoming call. A handset lifted will first establish a path as described earlier under the heading operation, and provided no internal call is being made at the time ringing current will produce an automatic switching pulse through bdt_2 and r_4 equal to the duration of the ringing tone plus the release time of the slow turn-off relay. If an internal conversation is in progress however, r_4 would be open as it would be undesirable to have an incoming call breaking into an existing conversation; r_4 being open prevents automatic switching. Assuming no internal conversation is taking place the following events occur (following switch order than real-time events).

First a path is established from V+ through the answering station o_3 contact and diodes to its G relay on one hand and through l_1 to the GI/GH toggle on the other. Note that all relay contacts are drawn in their off states. Relay L however is permanently powered when the system is not in use to keep a protective load on the power supply (note the states of l_1 and l_2).

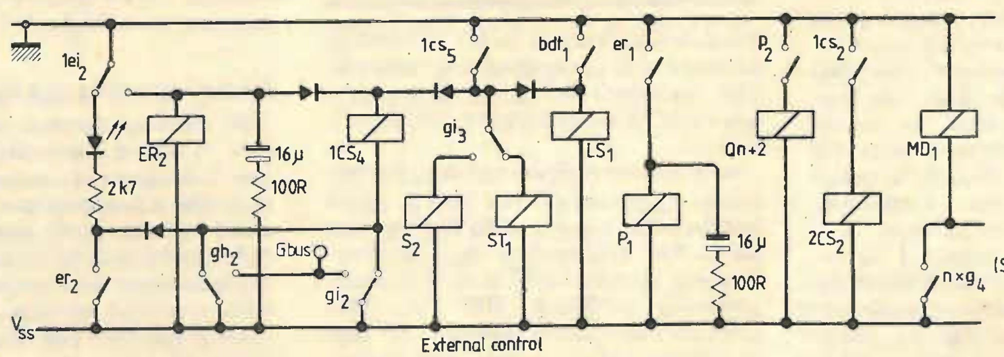
After switch on of GI at the start of the bell signal, contact g_2 in the external control completes connection of the answering station G relay. Its g_1 contact immediately holds G active through g_1, G coil and gi_2. The station's G_2 contact will break the original connection between this station and the internal control which now resets as if the handset had been replaced as outline earlier, allowing the next internal call to be made.



Basic diagram of a telephone 'off hook', with the bell disconnected and speech path established. Coil EI is active.

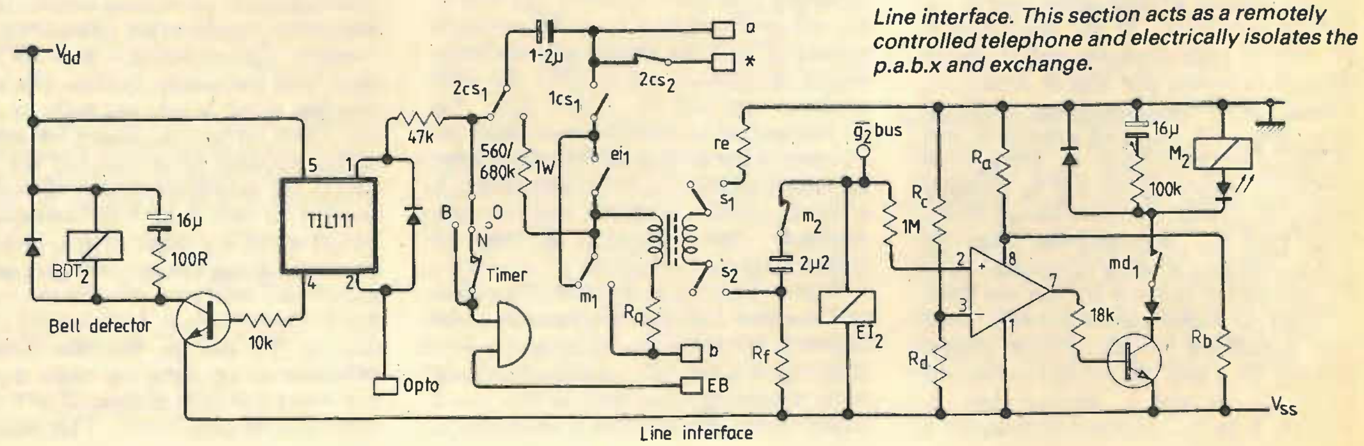
The line interface, which is essentially a remotely-operated telephone, is controlled by this, the external-control section.

Termination of the BDT pulse to the toggle now takes place either by o_3 resetting or the actual end of the bell signal which disconnects bdt_2, whichever occurs first. This allows GH to energize and gh_2 for the moment is in parallel with gi_2. Meanwhile gi_3 prepared S for switch on and gi_4 took over inhibit of the hold oscillator as lcs_4 will release before long. Contact g_2 which initialized resetting of the internal control now connects the external interruption relay EI into the line interface to the answering station. Contacts g_3 bypasses its q contact thus securing operation of GI/GH toggle from the answering station ground key. Action of g_4 is immaterial in this stage. In the line interface ei_1 doubles m_1 while in the external control, ei_2 provides power for the external reset relay ER. In co-operation with er_2, it also energizes the cradle switch relay IC. Contact lcs_2 operates 2CS so in the line interface lcs_1 connecting the primary transformer coil and $2cs_1$ disconnecting the ringer operate as a make-before-break switch. Contact lcs_3 duplicates ei_2 in providing power to CS and through gi_3 (which switched previously) operates S which in turn connects the transformer secondary by means of s_1 and s_2 thus establishing a speech path between the answering station and the exchange line through a capacitor and m_2. At the same time lcs_3 holds the led-switch relay LS on so the leds at each of the stations are continuously lit through h_1 and ls_1 in common and branching through individual limiting resistors to each of the separate stations and back through their a lines indicating 'a-line occupied' status at all positions. The hold oscillator remains inoperative since gi_4 keeps the oscillator-inhibit input pulled to V_{ss} when lcs_4 disconnects. Relay P is operated by er_1 so p_1 provides the holding path for the GI/GH toggle and p_2 operates the Q relay(s). Note that P acts well before the bell pulse terminates, allowing correct operation. The purpose of q_1 and q_2 will be discussed, but more important each station's q contacts will break. Because only one g_3 contact switched previously, only one station will now have exclusive control over the toggle.



If an internal conversation is being made (contact r_4 open) automatic switching of an incoming exchange call will not occur. Lifting the handset of a third station will produce a busy signal, as outlined through this station's g_2, o_2 and t_1 contacts all being inoperative then onwards through closed k_1 contacts operating 1ENG. As all q contacts are still closed any station, provided it is off-hook (including the two possibly having a conversation), may operate its ground key and immediately initialize the GI/GH toggle from the a-line, the station's ground key, its GK line, q contact and diode to l_1 thus establishing the speech path manually in a similat way to auto-switching as described above.

After conversation, resetting takes place when the handset is returned to its cradle. This de-energizes EI in the line interface. Contact ei_1 opening has no effect, to comply with line interfacing requirements according to which an interruptor contact may only send dial pulses and not perform a going-on-hook function. This is due to contact m_1 in parrallel. Now ei_2 disconnects tje external reset relay ER of which er_1 deenergizes P while er_2 disconnects CS which now performs an 'on hook' operation in the line interface by disconnecting the transformer coil and reconnecting the ringer. Relay LS extinguishes the leds by virtue of lcs_3 which also switches off S. Completing the reset p_1 disconnects the GI/GH toggle thus releasing G while p_2 reconnects all q contacts in readiness for the next line call.



Line interface. This section acts as a remotely controlled telephone and electrically isolates the p.a.b.x and exchange.

Making outgoing calls

Access to the exchange line is manually acquired by going off-hook and operating the ground key as detailed earlier. Upon receipt of external dialling tone from the exchange, dialling may commence. Some theory is required first though at this stage to clarify the process of dialling. As mentioned, the line interface is basically a remotely operated telephone. The relevant diagram depicts a very basic set-up in the off-hook condition i.e. with the bell disconnected and speech path established with EI engergized.

As soon as the dial is moved its m contact short ciruits the speech circuit to provide a clear path through the interruptor contact i, which in the actual telephone instrument is a normally-closed contact. Releasing the dial interrupts the i contact, causing pulses to be sent (to avoid adverse effects due to contact bounce and arcing, an RC network is connected across the i contact). Some time after the final dial pulse, the muting contact will re-open when the dial comes to a halt. The above action will now be imitated under remote control.

A voltage comparator is included which monitors the voltage between the telephone and the EI coil as indicated in the drawing. As the telephone connected represents a resistance (approx. 300Ω), voltage division occurs. Moving the dial shorts this resistance so the reference point goes fully to V+. As a consequence, muting relay M in the line interface operates and shortly after the last pulse, the telephone's m contact opens, the voltage at the reference point drops and consequently relay M disconnects. The RC network across the M relay emphazises proper delayed operation of the interface m contact. So when dialling takes placeEI follows the pulses produced by the telephone while the comparator i.c. reproduces the required muting action, the RC shunt keeping M powered. In the external control section ei_2 pulses a led for monitoring purposes and in the line interface a monitoring led is included in the M coil path. When dialling, the muting led shows up before dial pulses are sent, remains continuously lit with the dial-pulse led showing pulses dialled, and extinguishes some time after the last pulse. Pulsing of ei_2 does not effect relay ER as it is slow to release. CS is held via lcs_3.

Inhibiting out-dialling is accomplished by connecting contact g_4 of the station from which out-dialling is not desired. Any number of g_4 contacts may be connected in parallel. When such a station is connected to the exchange line its g_4 contact will operate muting disable relay MD which disconnects muting relay M. Thus on dialling ei_1 will still follow pulses produced but since m_1 does not operate nothing will happen. Replacing the handset will reset the system as described under the heading 'Incoming exchange calls'.

Call transfer

Incoming or outgoing external calls may be transferred to any other station or private consultations may be made as follows. These relays are switched on – EI, ER, CS, S, LS, GI, GH and the station's G and Q relay(s). Operating the ground key disengages the toggle through appropriate g_3 and e_1 contacts. Firstly when pressing the ground key, contact gi_2 secures a hold for CS, gi_3 disconnects S and instead energizes ST (its function to be explained) while gi_4 starts the hold oscillator which operates h_1 at approximately 2Hz. This results in all station's leds flashing at 2Hz, indicating the hold status. Secondly, when releasing the ground key gh_2 deenergizes the station's G relay and provides a second hold for CS. Contact g_2 connects the internal control and originator relays which act as described under Internal conversation. It also disconnects EI, ei_1 having no effect by virtue of m_1 and ei_2 releasing ER and by ER disengaging P, and Q reset.

The outcome of this is that in the line interface and external control sections only CS, LS and ST remain powered, the hold oscillator flashes the leds and all stations again have access to the toggle through their q contacts while CS maintains the line connection thus keeping it on hold.

After set-up of the internal control initialized by g_2 switching, internal dialling tone will be heard and the required station may be dialled. If private consultation only is required, or in the event of no reply, the calling station may return to the party on hold by operating its ground key. Alternatively the called station, when informed that there's a caller 'under the button' may take over the outside conversation by operating its own ground key. Access to the exchange line is regained by the switching action of various relays as outlined under 'Incoming exchange calls', with the difference that CS remains powered all the time, first by gh_2 not operating until the ground key is released and when it is released by energizing of ER causing er_2 to hold CS long before GS switches (explaining parallel connection of gi_2/gh_2). The hold oscillator will be stopped by gi_4 and the leds remain on continuously, again indicating a line-busy status.

In the event of no reply when trying to transfer a call, further attempts may be made in two ways. The usual procedure is to operate the ground key twice. The first operation will reconnect the exchange line and reset all internal circuits and the second push will regain access to the internal system, leaving the outside party on hold as described above.

The second procedure is to replace the handset and picking it up again while in hold mode. In a centrally supervised switchboard stations replacing the handset while having a caller on hold would automatically reroute the caller back to the switchboard, but as in this system every station is a switchboard in its own right the outside call won't be lost. Reset and set up will occur as explained under 'Internal conversation'. Finally, after completion of a transfer the initial station has two indications as to whether or not the transfer was successful – the led will stop flashing and the engaged signal will be received. This engaged signal will be given because as outlined earlier the internal circuits will not reset until both handsets are replaced so although the called station took over the conversation its t_2 contact will still be closed. As the calling station's g_1 contact will now also be on, holding relay G active, it will also operate relay 2ENG. Contact $2eng_1$ starts the engaged oscillator and $2eng_2$ provides a path for the busy signal through the initial station's held o_2 contact and its g_2 contact to this station. The initial station may now go 'on-hook' which resets all internal circuits.

Options are discussed in the next section, including connection of auxiliary equipment, paging and self-test.

There were one or two crossed lines in last month's circuit diagrams. Readers sending a large s.a.e. to Wireless World p.a.b.x., Quadrant House, The Quadrant, Sutton, Surrey SM2 5AS will receive amendments and a copy of the author's notes on construction.

Three-to-one cable applications

According to figures issued by the Department of Trade and Industry and the Home Office, there have been 37 applications to provide up to 12 cable tv pilot projects. Each application is to be evaluated by EIU Informatics, a subsidiary of the Economist Intelligence Unit. Their report will be considered by independant advisers who will submit their findings to the appropriate Secretaries of State. The pilot schemes are a limited experimental phase to be put into action before the full legislation for the proposed cable authority can be enacted. Applications had to be submitted twice; to the DTI for telecommunications licences to install and run the systems, and to the Home Office for a licence to provide programme services.

National Consumer Council

A letter sent to all the applicants for cable television licenses by the National Consumer Council, stresses the need for such services to meet the needs of ordinary consumers and suggests that to be a successful cable operator, skill must be used to interpret what the consumers want from cable, providing entertainment and services at a price that represents value for money.

Five specific points are presented that the applicants are urged to take into account. The plans and proposals should be made public so that consumers would have the opportunity to discuss the programme content; the operator may be helped in interpreting the need of the local community by forming a local consumer advisory group; a useful part in the local community could be played by allowing access to local voluntary organizations; the provision of a local database and 'notice board' should be taken into account in the medium term development of the company's strategy; interactive services, home banking and shopping for example, seem to offer advantages to the majority of consumers, and especially to the housebound and disabled, such a service should also be part of the medium-term strategy.

As a national body, the NCC cannot comment on the appropriateness of any plans to meet the needs of a specific local community, but their experience is that the consumers can do it themselves.

BT to sell tv cables

British Telecom is negotiating multi-million pound contracts with British industries to supply the advanced technology needed for cable tv. The orders are for 'switched star' systems, favoured by the Government for longer term franchises. BT expects to be able to offer the system in the second half of next year, in time for the introduction of the first new networks. Customers will be able to dial the service they require with a possible selection from up to 30 channels of broadcast and satellite tv and radio programmes; a pay-as-you-view channel; a selection of programmes available on demand from a video disc library, security locks; cable videotext; Prestel and remote banking and shopping. Future expansion could provide electronic mail, alarm services, remote meter reading, opinion polling and home computer and video games programs.

The system is being offered by BT Cable, an organisation created by BT specifically for marketing in this area. They are involved with supplying the system to ten potential operators.

● Mr Roy Fairbish, formerly a commissioner with the Canadian Radio-Television and Telecommunications Commission, is to join BT as a special adviser on cable tv. He will advise BT top management on the market potential for cable tv and related services, and on the preparation of franchise applications. Mr Fairbish has had considerable experience with cable tv companies in Canada and the US and was Managing Director of CJOH-TV, a cable tv network in Ottawa.

Stolen yacht caught in the net

When the 40ft ketch *Frizelle* was stolen from Alicante it was reported to the local amateur radio maritime network. Such reports are repeated twice a day and the news spreads world-wide through various relay stations. About two weeks later, a member of the network spotted a boat 'answering the description' of the *Frizelle* in Arrecife, Canary Islands. Registration and engineering serial numbers confirmed it to be the stolen yacht which was probably on its way to South America, where incidentally other sailing 'hams' had already been alerted.

The nets are organised for the informal exchange of position, weather and harbour information but some dramatic rescues have been assisted by floating radio amateurs. In the Round-the-World yacht race, a French competitor, Jaques de Roux, was sinking in the South Pacific. He pushed the 'panic button' on his satellite tracking transponder. The 'ham' relay station in Newport, Rhode Island alerted the UK station who passed the information to their New Zealand counterparts. The New Zealand station was in touch with Richard Broadhead, another competitor who was 300 miles away from De Roux. Richard got to Jaques when he had only four inches of freeboard left. The UK network was started in September 1969, by David Jolly, who kindly provided the information.

Industrial robots with an integrated vision system are being introduced by the Swedish company, ASEA. The one shown identifies the workpiece, visually inspects it and orients it. Its 'eye' is a c.c.d. tv camera in conjunction with grey-scale image processing, claimed to be much better than binary systems as it does not need special lighting. Programming involves a 'learning' procedure in which the object is placed in front of the camera and the image is processed. The system then collects data on the orientation of the object and checks it to show that it really 'recognises' the object. Defining the robot's grip position is included in the programming mode. ASEA are at 721 83 Vasteras, Sweden.

125 yaars ago, HMS Agamennon *went through considerable difficulties when laying the first complete transatlantic cable: in June 1858 there was one of the severest gales ever reported. The cable was inaugurated when Queen Victoria sent a 90-word telegram of congratulation to the President of the United States which took 16½ hours to transmit. The new transatlantic cable, TAT-7, was inaugurated in October, exactly 125 years after the first one. It can carry more than 4,200 simultaneous phone calls and can handle computer data and telex messages. It boosts Britain's transatlantic cable capacity by more than 50%, and restores the cable to satellite ratio to 50-50. An historic link between the two cables is that STC provided the new one and their predecessors, Glass, Elliot & Co. provided a proportion of the original. The next cable, TAT-8, already at the planning stage, is likely to offer digital transmission along glass fibres.*

Business software directory

The Department of Trade and Industry is to finance the setting up of directory of business software for microcomputers. This is intended to provide a showcase for the "thousands of software authors in this field". The directory is to be compiled by the NCC Microsystems Centre, 11 New Fetter Lane, London EC4A 1PU. When the project was announced, John Butcher MP said: "British programmers are the most talented in the world but many of them, particularly the one-man bands and home enthusiasts, have difficulty in marketing their products. I am determined to give them an opportunity to gain national exposure and take advantage of a domestic installed user base which is the highest, per head of population, in the world". He hoped that the creation of the directory would give the programmers the boost they needed so that they would become able to beat any international competitors. We hope so too and look forward to similar directories in the fields of science and industry.

New role for BTG

The principal role of the British Technology Group (the amalgamation of the National Research Development Council and the National Enterprise Board) will be to assist the translation into commercial products of new research ideas, particularly those from the public sector where the Government is the ultimate owner of the industrial property. The idea is to bring together the researcher who has made the discovery, companies who are looking for new products, and venture capital institutions who are willing to finance fresh ideas. There is often a gap between a research idea emerging and its commercial exploitation and the object of the BTG will be to act in collaboration with and in support of private initiative.

The services of the BTG will include: maintaining contact with research work, particularly in universities; helping to evaluate the 'marketability' of new ideas from both public and private sources; assistance with their development and with their protection through patents; helping industry and financiers to identify research work of potential interest to them by means of a database or through active search, particularly for the smaller companies; support for new companies to start up where other means of exploitation cannot be found, particularly those based around the researcher.

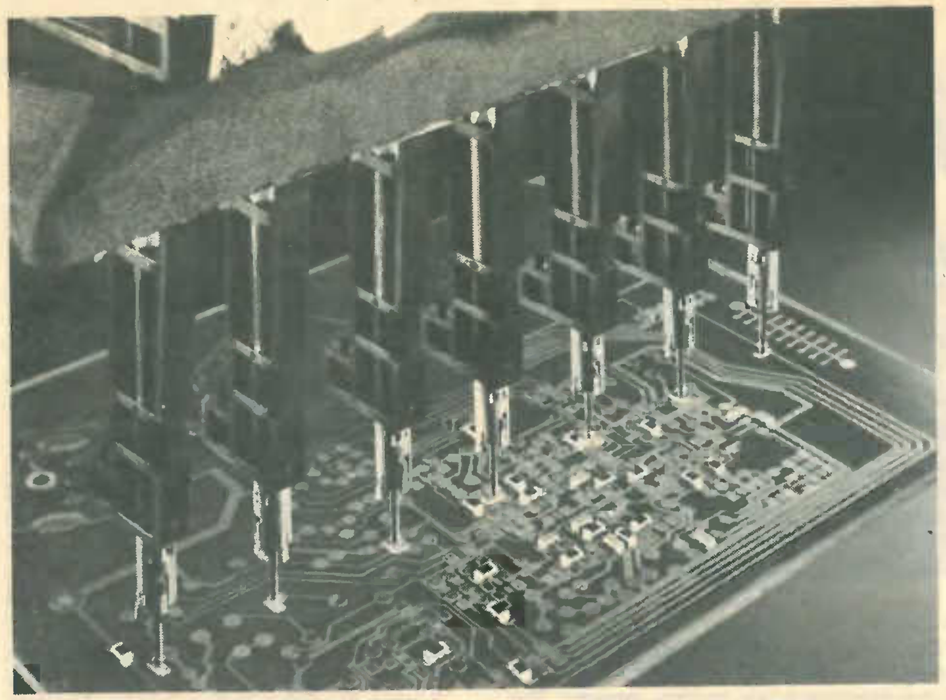
The BTG no longer has the right of first refusal to publicly funded research. New guidelines to govern future exploitation and the involvement of the BTG are being drawn up in consultation with those concerned, including the Research Councils who will use the guidelines when setting out the terms and conditions of any new research grants.

The NEB's investment programme is to be concentrated on this 'technology transfer' activity and the existing portfolio is to be disposed of. The BTG will be permitted to retain all income arising from its activities with the objective of becoming self-financing.

The present Chairman of the BTG, Sir Freddie Wood, is to retire early, as soon as the role of the Group has been fully formulated.

Martin Schimmer and Tim Lyons are the producers and presenters of Radio West's Datarama programme on microcomputers. The Bristol ILR station claims a 'first' for a programme which in addition to reviews of the latest equipment and software, and news, actually broadcasts computer programs. The signals are taken from the cassette outputs of a number of popular micros.

NEWS



Used in hydrid microcircuits for some time, surface mounted components offer considerable saving in space. Mullard have developed automatic placement machinery so that the components may be used on conventional p.c.bs. Illustrated are pick-and-place arms from an MCM III machine which can orient the components and lower them on to the p.c.b. which has been automatically prepared with spots of glue to hold the components prior to wave soldering. Each bank of arms can place 32 components in 2½ seconds and up to four banks can be used in one computer-controlled machine. Advantages claimed for the system are a 30% saving in space, and a 50% saving in assembly cost with a quality assurance of better than 50 ppm.

Zilog 32-bitter

Some details have been released of the Zilog Z80000, a 32-bit microprocessor which has on-chip cache and memory management. The instruction set, internal and external data paths and data types are all 32-bit. The c.p.u. is compatible with the 16-bit Z8000 but has greater computing power and is more versatile. The single chip supports 4Gbyte of directly addressable memory and runs at a clock speed up to 25MHz. 'Pipelining' allows more than one instruction to be executed at the same time and prototype performance tests have yielded an average of 2.2 cycles to execute all instructions, including jumps and multiplication and division. The high speed is partly due to the inclusion of a 256-byte cache memory on the same chip. This stores copies of the memory locations most recently referred to. If a memory location is accessed, the cache is checked first and the contents may be read indirectly without needing to access the main memory. The c.p.u. has two main operating modes; Normal, for user programs; and System, for internal operating systems functions. This separation protects the critical parts of the operating system from user access and takes care of all the time-critical or background tasks in multi-tasking applications.

The chip has 16 32-bit general purpose registers to hold addresses or data and there are two arithmetic and logic units, one of which is used for address calculations, the other for program execution.

The Z80000 has about 150,000 transistors on the chip and is made using Zilog's Z4 process, producing an n-mos chip with 2-micron geometry. Samples of the processor, housed in a 68-pin leadless package will be available in spring 1984 with production quantities to be available in summer.

"Mercury" in Texas

A telecommunications system similar to the UK Mercury system is to be developed along the railway lines of the Missouri-Kansas-Texas Railroad. The railroad company will be the major shareholder of the telecommunications company, partnered by Cable and Wireless who will install some 560 miles of fibre optic cable between Dallas and Houston by way of San Antonio and Austin. When the initial requirement of the railroad company's own communications are fulfilled, the rest of the 24,000 available voice channels will be leased on a wholesale basis in minimum quantitiies of 45Mbit/s, equal to 672 voice circuits. Further extensions of the system will be in response to 'market pressures'.

New frequency for Southern Sound

The 41st Independent Local Radio station opened in Brighton with the title of Southern Sound. Two new transmitters will cover an area along the southern coast from about Goring in the West to Peacehaven in the east, and inland as far as Haywards Heath. One interesting feature is that the station has been allocated the v.h.f. frequency of 103.4MHz, very near the end of the scale on most v.h.f. receivers and in an area still dominated by emergency communications services. By international agreement these frequencies are to be released for public broadcasting. So ILR now has a toe-hold in this part of the spectrum.

Dish in the docks

London's first satellite earth station is to be built in the heart of derelict dockland. Planned to be operational early in 1984, the station is to have two dishes, each of 13m diameter operating in the 11/14GHz frequency band. One will operate in conjunction with ECS the European communications satellite, the other with Intelsat V, over the Atlantic Ocean. With a quick substitution of a few components, either will be capable of assuming the role of the other. The antennae and transmission equipment is to be supplied by Marconi Communications Systems and the station built and operated by British Telecom International.

No v.h.f. tv after 1984

Following the report of the Merriman Review of the spectrum, the BBC and the IBA have issued a joint statement that the 405-line v.h.f. tv service is to be progressively shut down during 1984 with the last stations being closed during the first week of 1985. They estimate that 99% of the population already receive the 625-line u.h.f. service from BBC-1, BBC-2 and ITV and 90% also receive Channel 4. U.h.f. stations are being installed at about 60 a year to cover the remaining areas. However it has been admitted that some small remote communities will still be without u.h.f. tv by the end of 1986.

Those who are affected, and they can easily identify themselves as those at present unable to get BBC-2, which is u.h.f. only, can get more information from the Engineering Information Departments of both broadcasting authorities.

Practical subwoofer design

This add-on active filter design was designed to match a pair of LS3/5a loudspeakers but is easily modified to match other small high quality speakers.

This subwoofer system was designed to match a pair of LS3/5a speakers, but is easily modified to match many other small high quality speakers. The application called for an add-on system, requiring no modification to the existing stereo amplifiers. In addition, I decided it is necessary to have a subwoofer with an adjustable "low end" so that the system would suit a range of signal sources. Finally, I hoped to design a subwoofer which would fit into my rather small listening room and yet provide adequate output down to 20 Hz.

For my style of listening I determined that 88dB spl is an adequate sound pressure level. A single B139 l.f. unit driven by an amplifier delivering up to 30 volts r.m.s. can deliver this sound level. Of course extra sound can be bought by multiplying speakers and amplifier power, however Bach organ music sounds very authentic in my room with the volume control at partial 'wick', so I am satisfied with what I have.

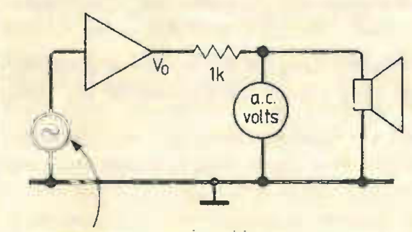
A transmission line enclosure – effectively a long pipe behind the driver – has several attractions. A seven or eight foot tapered pipe filled with long fibre wool should be easy to build, and should provide low bass with good efficiency and few complications.[1] However such theoretical advantages are compromised in transmission lines that are folded because they suffer from resonances. Sadly, an unfolded transmission line would not fit in my listening room.

The best remaining choices are reflex and closed box enclosures. The reflex enclosure is tricky to tune, and the tuning depends on parameters which I believe are not stable with regard to time, temperature, and humidity. The closed box is the smallest and therefore also most easily made rigid of the types of enclosures considered. This appealed as I am not a great craftsman in wood, and I also have little space. Hence it was chosen and its peculiar problems coped with electronically.

The problems of a closed box enclosure are that it raises speaker resonance (the transmission line actually lowers it) and that it rolls off sound output level from the resonant frequency downwards at 12dB/oct, behaving like a second-order high-pass filter.[2] Thus a flat electrical input will not produce much acoustical output below the resonance. The answer is to provide an electrical input boosted by an antiresonance equal and opposite to the speaker resonance. This is realised in a equalizer placed ahead of the subwoofer's own power amplifier. The stage must be an active filter having second-order complex zeros with identical resonance frequency and Q as the poles of the closed box. Such filters ordinarily require either four op-amps or are difficult to tune,[3] but I devised a special three op-amp filter which can be tuned easily to equalize the resonance of a subwoofer in a closed box.

by B. J. Sokol

The box can be built with only rough consideration of enclosed volume and then its parameters can be measured electrically. My box, of about 40 litres capacity, doubled the free-air resonant frequency of a B139, which is about the right amount for a properly designed closed box.[4] Once I'd mounted the unit in the box, filled it loosely with acoustic absorbant and sealed it, I measured its parameters by the method shown in Fig. 1. The measurements yielded 48Hz and Q=0.71. Using these parameters the equalizer is easily tuned.



First measure the resistance to d.c. of the speaker, R.

Next determine the frequency f_r at which the a.c. resistance (=100×V) is maximum, R_{max}.

Calculate $R_m = \sqrt{R_{dc} \cdot R_{max}}$.

Find the two frequencies f_1 and f_2 above and below f_r where the a.c. resistence measures R_m (e.g. $V = R_m/100$).

Calculate $Q = \frac{fr}{f_2 - f_1} \cdot \sqrt{\frac{R_{dc}}{R_{max}}}$.

***Fig. 1.** How to find Q and f_r of a closed box speaker (ref. 2 page 806).*

The equalizer works as follows. A convenient subsonic frequency was chosen for the filter poles (it must have two poles or its output would become infinite as input frequency approached zero). The frequency chosen was 7.2Hz, the factor of convenience being standard component values. Two non-inverting filters were built with that pole frequency, one a low-pass and one a bandpass, each with a Q of 0.5. The two filter outputs are added with adjustable weighting factors to the original signal. The result is a biquad filter with complex zeroes easily adjusted for both frequency and Q. The mathematics to prove this is simple using complex frequency (s). One need only know the forms of second-order high-pass and bandpass functions and that the quadratic expression s^2+As+B is related to resonance parameters by $B=\omega^2=(2\pi f_r)^2$ and $A\omega/Q$. Then the transfer functions are

signal passed straight through:

$$H_0 = 1 = \frac{s^2+As+B}{s^2+As+B}$$

bandpass filter:

$$H_1 = \frac{\omega s}{s^2+As+B}$$

low-pass filter:

$$H_2 = \frac{\omega^2}{s^2+As+B}$$

The sum H+kH+kH will have a numerator of the form

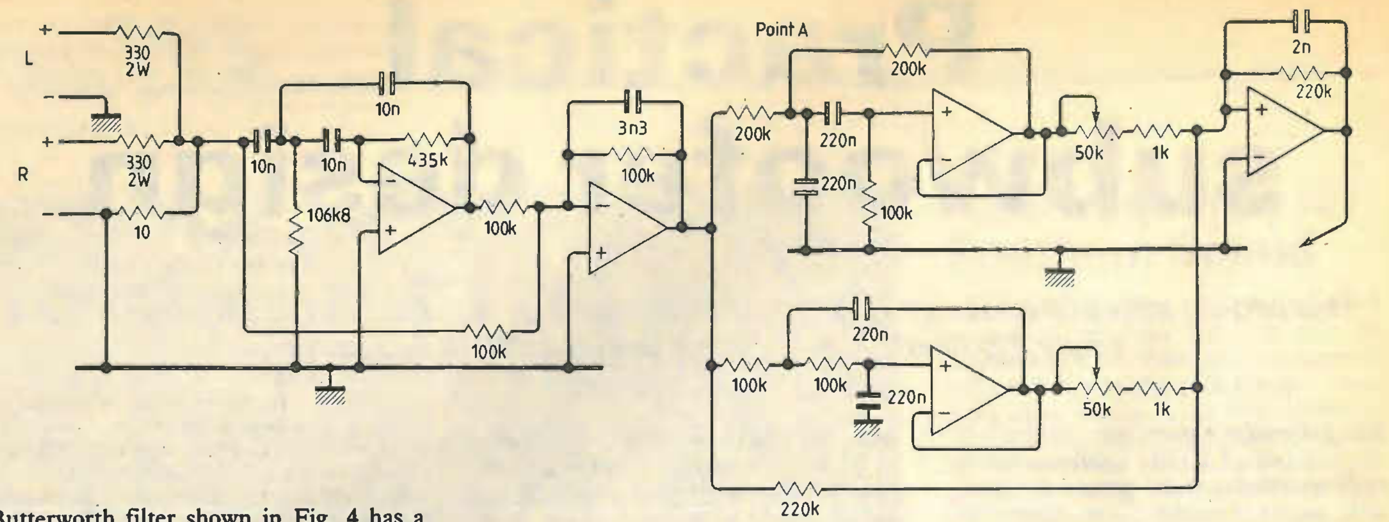
$$s^2+Cs+D,$$

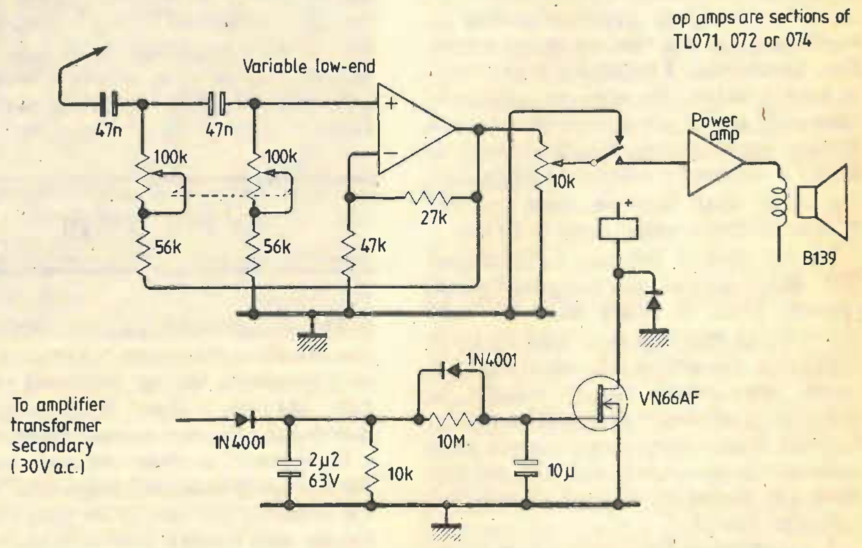
where C is tunable by k_1 and D is tunable by k_2 without interaction. Thus we have an "orthogonal" means of tuning C and D, which provides an easily adjusted pair of zeros.

Practically, the equalizing filter is adjusted as follows.

- Measure f_r and Q for the closed box woofer as in Fig. 1.
- Earth point A in Fig. 2, apply input signal set to f_r at input and adjust p_2 for *minimum* output.
- Keep same input, remove the earth and adjust p_1 so that the gain of the equalizer (measured from input to output) is exactly 1/Q. The shorting of point A is of course to maximize the Q of the zeros to get a sharp null (that is, to make C as small as possible during the second step).

The equalizer is finished. The equalized box will roll-off its output below 7.2Hz. This is too low, so the adjustable low-end filter is added in series with this stage. The





op amps are sections of TL071, 072 or 074

Butterworth filter shown in Fig. 4 has a high-pass 3dB point variable from 22 to 34Hz. Below its set frequency it flattens the equalizer output and allows the closed box output to roll off at −12dB/oct. The Butterworth filter (Q=0.707) produces no peaking, but a Bessel filter (Q=0.5) will produce less phase change at the cost of some bass output. If you want to try that simply remove the 47kΩ resistor in the filter shown. I did not hear an improvement with that change. Be sure to earth the case of the dual pot, and make its shaft available from outside the subwoofer enclosure.

Finally the crossover must be designed. Here a lively debate is in progress, with current arguments presenting the all-pass or double Butterworth crossover functions as best.[5] It is instructive to see why this is not so for subwoofer crossovers. The main advantage of the all-pass crossover is good spatial dispersion in spite of non-coincidence of the crossed-over units. This is hardly significant where the wavelengths in question are commensurate with the size of the listening space. The price of this crossover, uneven power response, could produce boominess, the anathema of bass speakers. Its one remaining advantage, rapid fall-off in output for both units, can be compensated in other ways.

So the all-pass crossover functions

$$\frac{s^4}{(s^2+\sqrt{2}s+1)^2} \text{ and } \frac{1}{(s^2+\sqrt{2}s+1)^2}$$

were rejected for my design. A good thing, as they cannot be realized in the desired add-on system because the side speakers, unmodified, do not have double Butterworth characteristics! In fact, the characteristics of my side speakers are of the second-order filter type, because they are closed boxes. Published graphs show that f_r=74 Hz and Q=0.67. (Many other small speakers are of similar type, and their parameters can be determined by the method of Fig. 1.) The delightfully simple solution to the crossover problem I chose is to subtract an analogue to the response of the side speakers from the total signal and to provide that difference signal (the missing sound) to the subwoofer. The realization of this design is shown in Fig 3 together with equations needed to modify it for other side speakers.

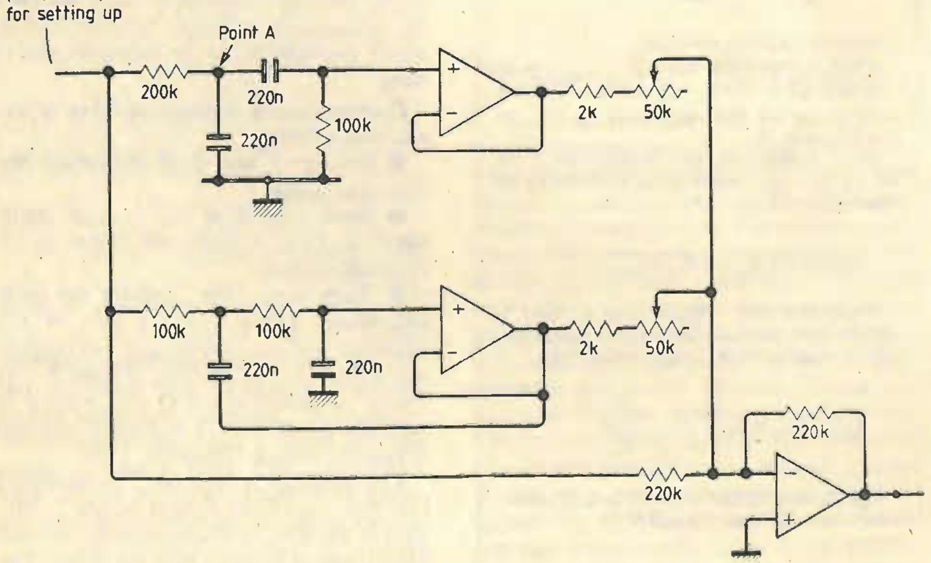
Such a crossover, the asymetrical constant-voltage type, has a well-known problem.[7] That is the difference function sent to the subwoofer has a single real zero

$$H_{+over}=1-H_{h.p.}=1-\frac{s^2}{s^2+As+B}$$

$$=-\frac{As+B}{s^2+As+B}, \text{ zero at } s=\frac{-B}{A}.$$

The consequence is that the subwoofer rolls off at only −6 dB/oct beyond this zero. The B139 can in fact reproduce higher frequencies as its cone doesn't resonate until about 800Hz, but if the third 'channel' were allowed to deliver output at

Fig. 2. In closed box equalizer stage R_2 adjusts f_r and R_1 adjusts Q.



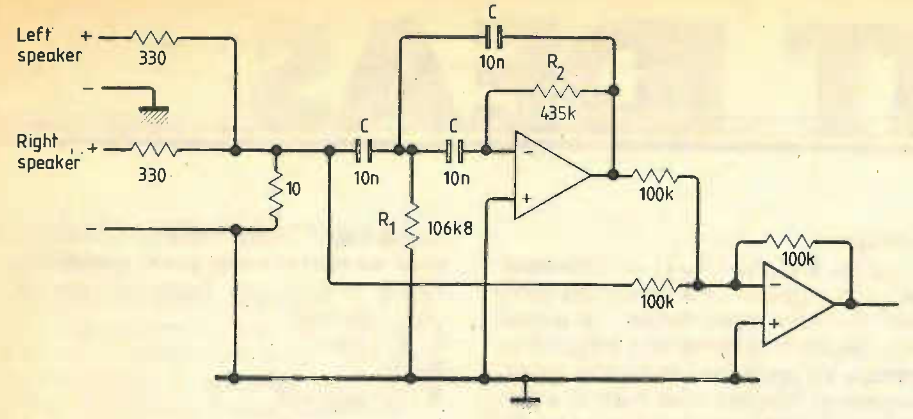


Fig. 3. Design equations for this inverting crossover filter are

$$f_r=\frac{1}{2\pi C\sqrt{R_1R_2}} \quad Q=\frac{1}{3}\sqrt{\frac{R_2}{R_1}}$$

so it can be adopted to any other small closed-box speaker once f and Q are determined. Left-hand op-amp emulates the LS5/3a response.

mid-frequencies it would muddle the stereo image. My solution was to add two additional single-order sections (one capacitor in each summing stage in Fig. 4) so that there is finally a −18 dB/oct roll-off for the subwoofer.

This solution sounds excellent. In fact the musical effect of the subwoofer is sometimes uncanny. Purcell's Funeral Music for Queen Mary was played during testing when the subwoofer was off to the side away from both side speakers, and yet the great kettle drums seemed to come right out of the tiny LS3/5a speakers. Evidently, the side speakers provided all the transient and higher harmonic information by which the ears determine sound origin.

Two practical notes complete the description of the system. The summing of the stereo channels is achieved using 330Ω resistors at the *signal* end of twisted-pair cables. As the input impedance of the subwoofer is set to 10 ohms long cables produce no hum pickup. In setting up, p_4 is used to match the subwoofer output to the efficiency of the side speakers – it need not be readjusted when the variable low-end control is used. If the stereo preamp were seperate from the amp the signal could have been taken from its (post volume control) output. Then another summing op-amp would be needed and the speaker terminals would have to be reversed to restore phase.

Finally let me explain the rather elaborate anti-thump relay shown in Fig. 4. It has two time constants to delay signal half a minute after switch-on and also turn signal off milliseconds after power down. This protects the expensive driver.

Enjoy the restored missing octaves!

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4. Small, R. H., Closed box loudspeaker systems, part 2: synthesis, *JAES* 1978, p.11. Also Zacharia, K. P., On the synthesis of closed box systems using available drivers, *JAES* 1973, p.729.
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6. Harwood, H. D., Whatton, M. E. and Mills, R. W., Design of the miniature loudspeaker type LS3/5a, Research Dept, BBC Engineering, 1976, pp. 2, 3.
7. Small, R. H., Constant-voltage crossover network design, *JAES* 1971, p.16.

WW

The author

Introduced to building crystal sets at about eight, Jim MacHarg applied for his first patent while still at school and has had several patents granted in totally unconnected fields. He conceived the Rectavox Omni loudspeaker, selected by the London Design Centre, and his analysis of the chances of winning on ERNIE was published in Stock Exchange Gazette. After developing a computer, in pre-microchip days, to determine in how many numbers "house" should be called in order to win bingo prizes, seven years of research revealed how actual gas generation in the lead-acid battery could be sensed from the terminals alone. He is at present maintaining an ancient listed Northumbrian landmark, Fowberry Tower, in which his complicated heating system burns about 80 tons of timber per winter.

continued from page 27

demand: this increases the rest periods between pulses of the burner and allows the maximum time for the heat to transfer.

Application

Being concerned purely with the manner in which the burner fires, the energy saver should be compatible with any form of timing controller. However, because of the "holiday-cottage effect", it is suggested that best operation may perhaps be achieved with least inconvenience if a two-stage thermostat is used in order to prevent unnecessary cooling down of the structure of the house or other building, because this allows the ingress of conducting damp into the walls, so speeding the dissipation of energy to the outside: this effect does not help the asset much either! Having found a little dry rot at Fowberry Tower before we moved in, the writer knows full well the importance of such matters – if not caught in time it can be positively devastating to all timbers, and cost very much more to put right than a little steady energy usage: wet rot seems to help to let the dry rot in.

The first priority must always be to keep the energy where it is meant to be by using adequate insulation and by stopping draughts especially at floor level – cold draughts do not rise and cold feet tend to make you feel cold so that you want to turn up the heat. The second priority is to use the most efficient boilers, and the third is to stop over-temperatures and so cut as much acceleration out of the system as possible. Finally, control if you wish to, but if you have attended adequately to the earlier points you must not be surprised if control fails to provide the anticipated saving.

A useful tip: if your loft or roof void is adequately ventilated (and this is important) a layer of ordinary builder's polythene stapled over the ceiling joists, on top of the insulation, serves three useful purposes. Firstly it stops convection currents dancing up carrying the heat out of the insulation, secondly it stops draughts scooping the heat from out of the insulation, and thirdly, if you do have a roof leak, it sags between the joists to form mini-lakes which evaporate at their leisure leaving a tell-tale tidemark, which is far preferable to a soggy mass of insulant. The cost is minimal.

WW

Correction

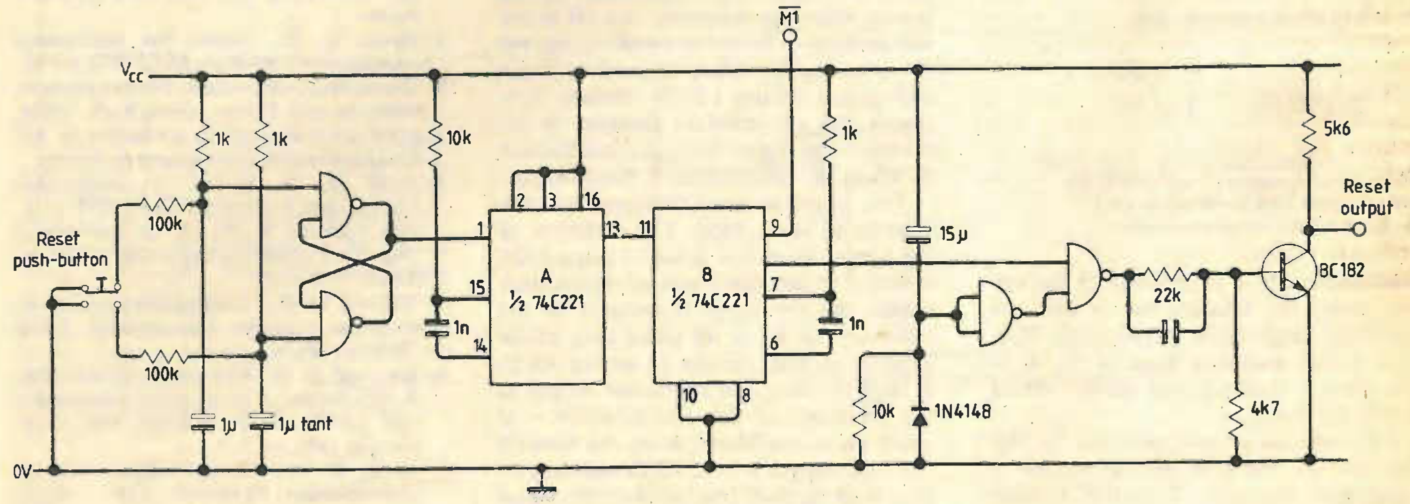
Nanocomp to teletypewriter interface. This article in the October issue referred to the 6502 Nanocomp, which does not exist. Two versions of the Nanocomp exist, one using the 6802 microprocessor and one using the 6809. Mr Barton's teletypewriter interface was designed for the 6802 version.

Z80 reset without memory loss

Generating short pulses synchronized with the processor M1 signal, this circuit overcomes the problem of loss of data in dynamic ram which is caused by resetting a Z80 microprocessor used to generate refresh signals.

Section A of the 74C221 dual monostable i.c. is triggered by a debounced signal from the reset push button for around 10μs. Monostable circuit B is triggered by negative M1 transitions during this period, ensuring at least one reset pulse at a time when the processor is executing its longest instruction. Under normal conditions when no reset is taking place, section B is held in its reset state. Spare gates provide power-on reset.

G. K. Dore
Perton
Wolverhampton

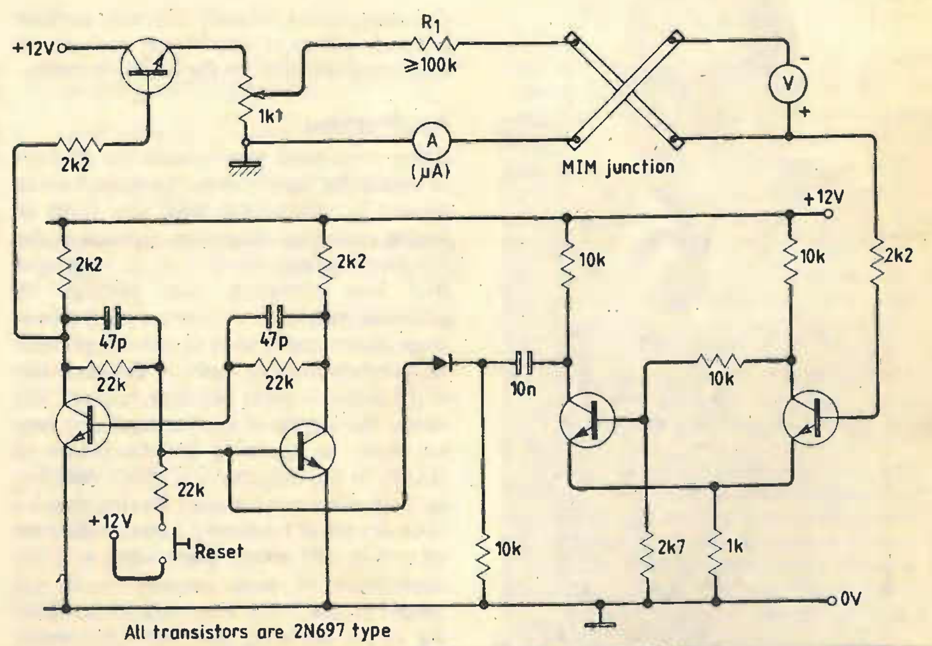


MIM tunnel junction measurements

Breakdown voltages of metal-insulator-metal junctions are measured to obtain information about their work function characteristics, but methods previously described (see page 79) have been destructive and have not allowed breakdown measurements in both directions on the same junction. This circuit switches off less than 5μs after breakdown occurs, leaving the junction intact, and allows repeated measurements to be made on the same junction.

A Schmitt trigger is coupled to a bistable multivibrator through a differentiating network which applies a negative pulse to the base of one of the multivibrator transistors to switch it off when breakdown occurs. The second multivibrator transistor switches on and the emitter voltage of the series-pass transistor falls to zero, cutting off the supply to the junction. Breakdown voltages of less than 0.4V could be measured by setting the Schmitt-trigger threshold at about 0.2V. After each breakdown reading the potentiometer wiper is grounded and the reset button pressed. Resistor R_1 should be a high value.

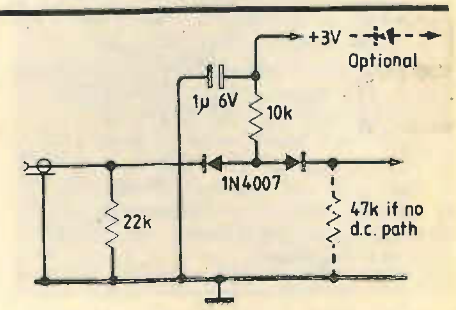
Ijaz ur Rahman
Quaid-e-Azam University
Islamabad
Pakistan



Thunder storm protection

Having lost two r.f. transistors in a recent thunderstorm I designed this simple means of protection which, in the event of a storm, will cost at worst a 1μF capacitor – short of a direct hit of course.

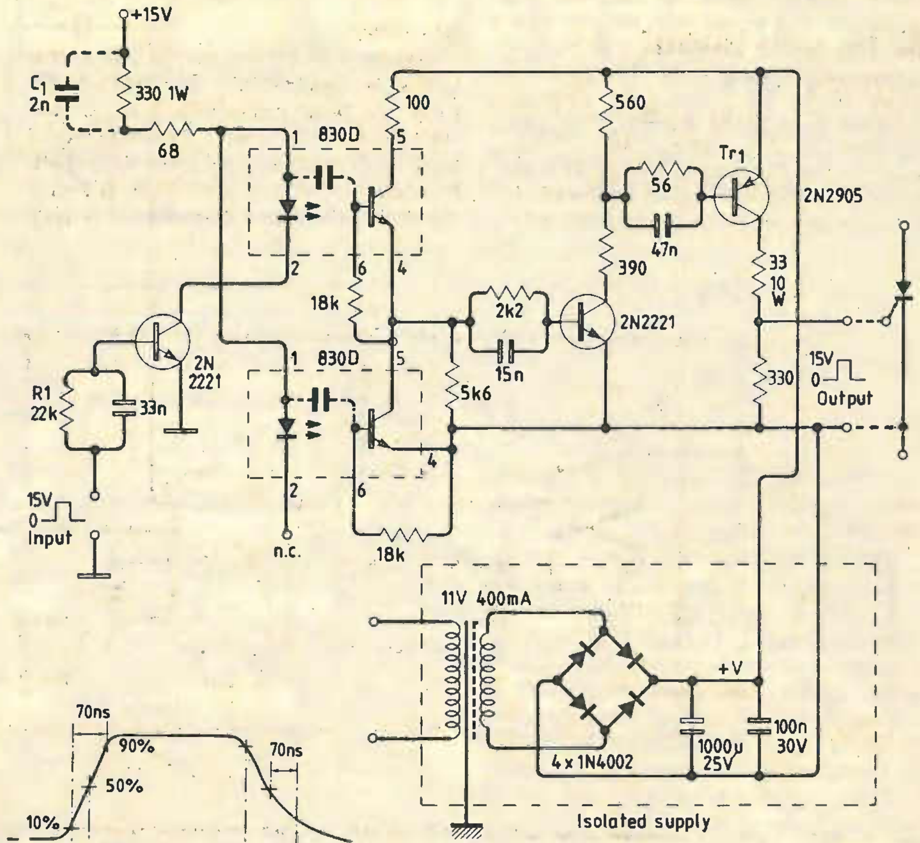
R. G. Young
Newhaven
Sussex

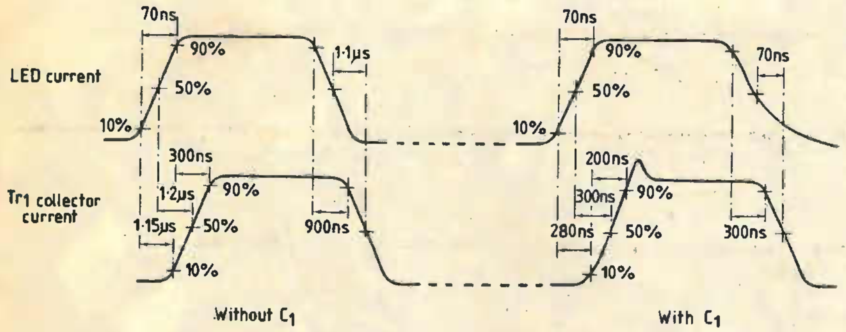


High-speed, high-c.m.r. isolator

Designed for triggering thyristors, this circuit using inexpensive Fairchild opto-isolator units exhibits low delays and fast switching times at operating frequencies greater than 10kHz. During normal operation, only one of the isolators transmits pulses, since a led connection of the second is left open. Common-mode noise would normally cause false triggering through the coupling capacitance of the isolator, but in this case the second isolator also turns on and shorts the emitter resistor of the first isolator. Both isolators are now on, but no pulse is transmitted. Waveforms shown are at 10kHz with 50% duty cycle.

S. K. Biswas
Indian Institute of Science
Bangalore



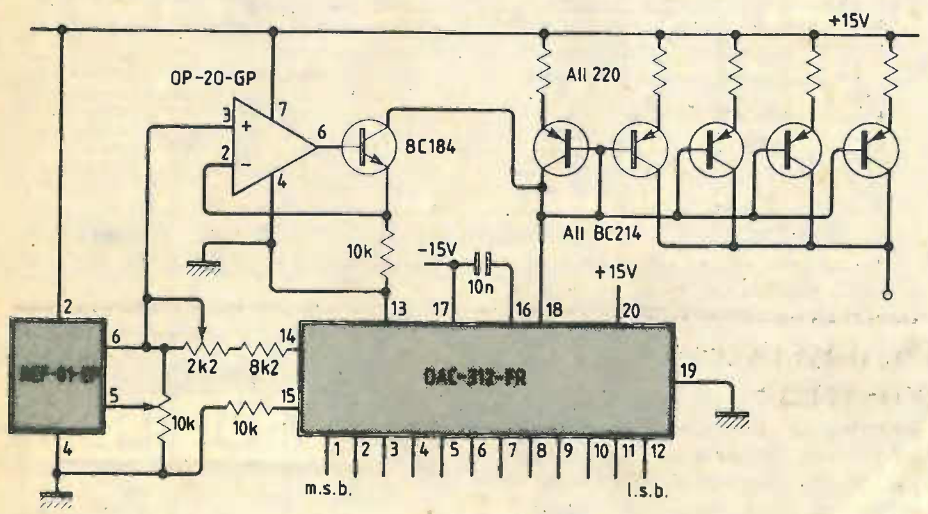


Programmable current loop

An accurate cureent loop that can be varied between 4 and 20mA is often required for control system calibration and automatic test equipment. This 12-bit digital 4-20mA loop is easily calibrated, is t.t.l. compatible and has a fast settling time. It uses a 10V reference to set the op-amp/BC184 current sink to 1mA. With all-zeros digital input, the 10kΩ potentiometer is used to set output of the multiplying mirror to 4mA. When all digital inputs are at one, the d-to-a converter sinks 4mA, so with the 1mA standing current, the multiplied output is 20mA.

Though 12-bit accuracy may not be needed – few transducers are accurate or repeatable to within 0.25% – the converter's 4mA full-scale current is useful. One or both adjustment potentiometers may be omitted if 0.5% error is acceptable, provided that accurate resistors are used. Output compliance is –25 to +14V.

G. R. Nimmo
Bourns Electronics Ltd
Hounslow
Middlesex



CIRCUIT IDEAS

Low-pass filter design

Many situations occur in electronic engineering where a second-order low-pass filter is required, having amplitude and phase-frequency responses that can be selected by careful design. The simplest way to design a second-order, low-pass filter is to arrange for two RC lag networks to have the same corner frequency with the transfer function

$$\frac{E_0}{E_i}=\frac{1}{(1+sC_1R_1)(1+sC_2R_2)}$$

where $\omega=\frac{1}{C_1R_1}=\frac{1}{C_2R_2}$.

Fig. 1.

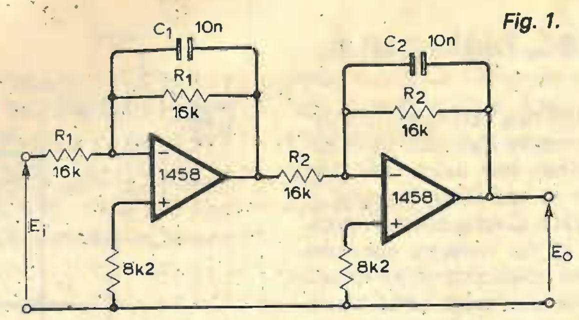
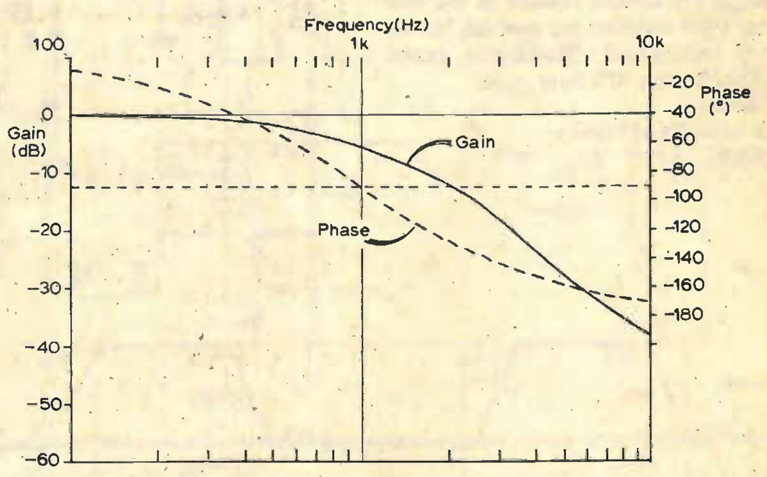


Fig. 2.

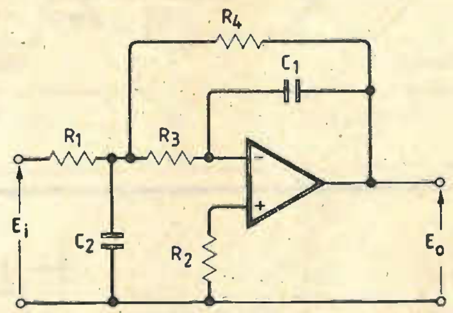


An active filter of this form is shown in Fig. 1 and the frequency response, where the corner frequency is 1kHz, in Fig. 2.

To vary the filter response by controlling the rate of change of gain and phase one needs to specify a particular value of damping factor, ζ. The damping factor can be varied over a wide range without significantly affecting the filter's bandwidth as shown in Figs. 3 and 4, these diagrams show the circuit and frequency response of a second-order filter having the same nominal bandwidth of 1kHz but with a damping factor of 0.15. The transfer function is now

$$\frac{E_0}{E_i}=\frac{1/R_1R_3}{s^2C_2C_1+sC_1(1/R_1+1/R_3+1/R_4)+1/R_3R_4}$$

Fig. 3.



Calculations can be based on the following design equations.

$$C_1=\frac{k}{2\pi f_o}$$

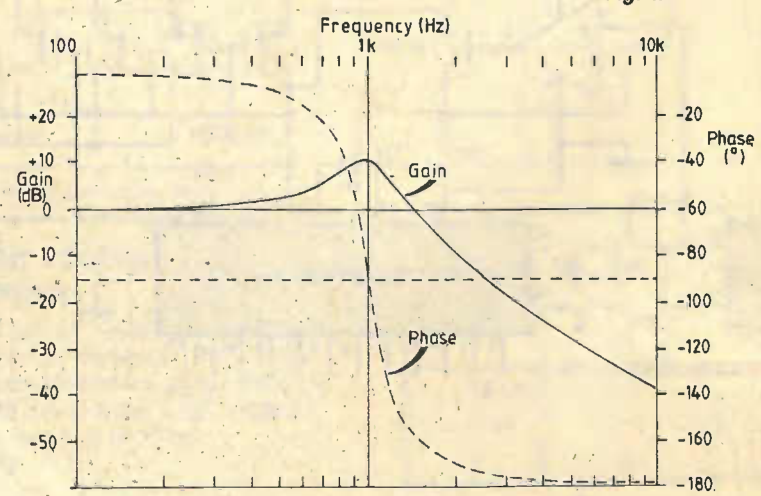
where f_o=1kHz and C_1=0.01µF, say, and

$$C_2=\frac{1}{\zeta}.(A+1)C_1$$

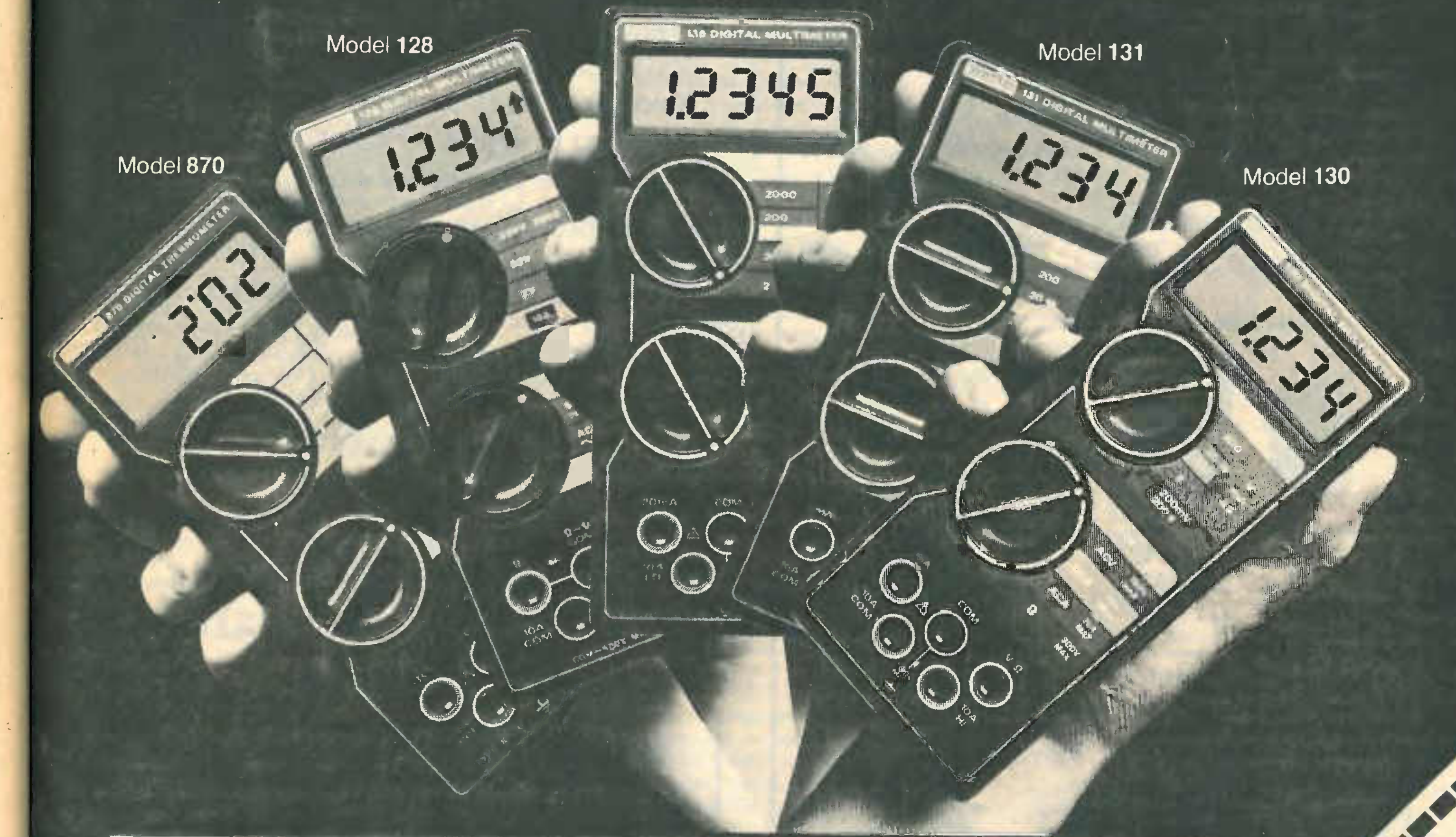
where ζ is 0.15, A is unity passband gain, R_1 is ζ/Ak, R_2 is $R_3+(R_1||R_4)$, R_4 is AR_1 and R_3 is $\zeta/(A+1)k$. By applying these design equations, the values given are obtained. Standard values have been selected.

$R_1=R_2=R_4=2.4k\Omega$
$R_3=1.2k\Omega$
$C_1=0.01\mu F$
$C_2=1.0\mu F$

Fig. 4.



D. Cutler
Thorn-EMI Datech Ltd
Somerset



LETTERS

TECHNOLOGY AND PEOPLE

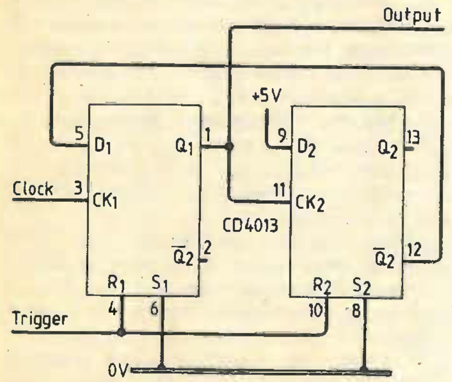
If, as J. A. MacHarg (*WW* letters, October) asserts in his advocacy of Professor Campbell's theories, "everything we do is done ultimately for stimulation of the pleasure areas which have evolved out of the "smell brain" of the fish", why then is it such a common observation of human life, that those who do what they like rarely seem to like what they do?

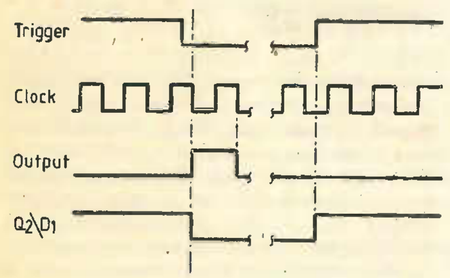
S. C. Elliston
Hemel Hempstead
Hertfordshire

PRECISE SINGLE PULSES

With reference to D. A. Haines' Circuit Idea "Precise Single Pulses" in your November 1983 issue I feel that I should draw your attention to the fact that the circuit will produce a glitch on the output when the trigger input returns to the quiescent high state. This high resets Q_1 to a low while the $\overline{Q}_1$ output resets Q_2 to a low. Thus during the propagation delay time of the second half of the CD4013, Q_1 is low and Q_2 is high, producing a spurious output.

The same function can be achieved with just the CD4013 chip if it is connected as shown in the attached circuit. With reference to the enclosed timing diagram, it is seen that the quiescent trigger level holds both of the flip-flops reset. The first clock after the trigger line goes low sets Q_1 (starting the output pulse) while the edge on Q_1 sets Q_2 high and $\overline{Q}_2$ low. Thus, the D_1 input is held low and the next clock pulse resets Q_1 to low (ending the output pulse) while the negative edge on Q_1 has no effect on the second flip-flop. The circuit is now locked-up with succeeding clocks having no effect. Only the trigger line returning high can reset the second flip-flop to unlock the circuit.





Note that in both circuits the trigger pulse must be a minimum (for worst case phasing w.r.t. the clock) of two clock periods wide.

Colin Ramsay
Stevenage
Hertfordshire

DESIGN COMPETITION

A circuit to remove background noise when a person is speaking (Letters: G. Barnes, October 1983) might consist of an amplifier whose frequency response envelope matches that of the human voice. In a more advanced design (i.e. where an amplifier is required to discriminate between an unusual kind of sound and its noisy background) a variable frequency response, preset or manual might be provided.

If the background noise is weaker than the signal, one could also arrange for loud sounds to be amplified more than soft ones. After this initial contrast expansion (by a non-linear circuit) the signal could be clipped at its lower energy level and finally restored to its original amplitude range (by an inverted non-linear circuit).

The above two distinct "selections modes" of an amplifier (frequency discrimination and amplitude discrimination) could be combined with a third selection-mode, namely, signal discrimination in which the oppositely-pointing microphones are used in anti-phase.

A. H. Winterflood
Muswell Hill
London N10

CURRENT DUMPING

Wireless World of September and October contain no less than 12 pages by Mr McLoughlin, analysing very thoroughly various contributions to current dumping that have appeared in this publication.

I will agree at once with most of McLoughlin's analysis. Yes indeed the presence of R_{12} does affect the balance condition exactly as he states. His mathematics, as one would expect, are quite precise and perfectly acceptable. Yes again, we are quite prepared to accept 5-10% error in the balance condition and still show a major advantage over a non current dumping amplifier of the same configuration and the same overall feedback.

If I may summarize Mr McLoughlin's conclusions they are, I believe, that if the balance condition is perfect all works as it should, but if there is any error in the balance condition, as there must be, then one is better off without the current dumping concept. But this ignores completely the overall loop gain and the necessity to meet the Nyquist criteria. Indeed we have twelve whole pages without a single pole in sight.

If we take the simplified model repeated as Fig. 1 for convenience and assuming A to have very high (call it infinite) gain, then indeed removing C and shorting L produces a perfect conventional amplifier – an amplifier with conventional feedback and very high (call it infinite) loop gain. But such an amplifier is impossible.

In the simplified circuits, we have used the concept of 'virtual earth' to define the gain of the class A amplifier. This seems to cause some confusion, so let us redraw it as an integrator of defined gain, filling in the other values to suit, as in Fig. 2.

The balance condition is met and the overall feedback is 48dB at 10kHz and falling with frequency – just about what is required for a good stable amplifier, and we're all agreed no 'crossover' distortion.

Next, assume an unbalance of 10% by changing any one of the constants, let's say by changing L by 10%. At once a small kink appears in the transfer characteristic. It distorts. So following McLoughlin now get rid of the current dumping by shorting L completely. The distortion is now much worse and we find we have to interfere with the integrator gain to restore the situation. But what have we done? We have in fact just added more overall feedback. How easy life would be could we but increase feedback ad infinitum.

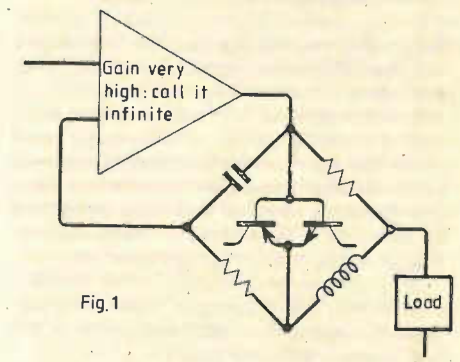


Fig. 1

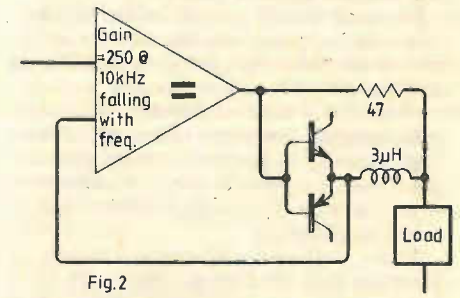


Fig. 2

Of course, we can apply bias to the dumpers or add various other refinements as one would to improve the conventional amplifier. Adding current dumping to such an amplifier will still give the same relative improvement. I am referring, of course, only to the voltage transfer distortion of the output stage and not to any other distortions which may be present.

Peter Walker
Acoustical Manufacturing Company
Huntingdon

I have read with much interest the articles by Michael McLoughlin in the September and October issues. Seeing that my name is mentioned several times in them, I would like to make the following comments.

The explanation of the basic principle of the Quad 405 amplifier given in my Letter of July 1976 is described by Mr McLoughlin as 'intuitive', and my dictionary gives the meaning of intuition as 'immediate apprehension without reasoning'. Now it seems to me that my explanation involves quite rigorous reasoning as far as it goes, and in several hundred pages of notes on the topic I have used a good deal of simple algebra. But I thought it best for the July Letter to omit the algebra and let the essential simplicity of the idea stand out unadorned.

LETTERS

In the grey-background editorial inset on page 39 of the October issue it is said "... one group insists that the amplifier works by feed-forward, another school disagrees and says it uses feedback". I do not feel to belong to either of these insistent schools, and in chapter 14 of the Newnes-Butterworths book Radio, TV and Audio Technical Reference Book I say "It is also possible to regard this amplifier as employing the principle of 'feed-forward error correction', for the class-A amplifier contributes current directly to the load only when the dumpers are unable to do so fully – in other words, the class-A amplifier provides feed-forward correction of the dumper-stage error." So I was glad to find Mr McLoughlin defending the validity of alternative views. Of course such alternative views really only affect physical reasonings, and inventive steps in evolving modified circuits. Once a circuit exists, mathematical *analysis* of its performance does not essentially require any specific categorization of the circuit.

I was, however, very surprised to find Mr McLoughlin maintaining that John Vanderkooy and Stanley Lipshitz "again insist that feedforward alone is the only correct explanation", for a careful reading of their truly excellent paper (*AES Journal*, Jan./Feb. 1980) does not reveal to me any such insistence. Indeed it was with satisfaction that I found they included my name amongst those who had "correctly understood its operation". They choose to base their approach on the error feedforward concept – and I have no quarrel with this – but nowhere suggest that my alternative "instantaneously-variable negative feedback" approach is in any way wrong. I still prefer it.

Pervading Mr McLoughlin's thorough mathematical treatment there seems to be an implied belief that fully satisfactory stability, in the Nyquist sense, can be retained when the reversions to simple traditional overall feedback, mentioned in several places, are adopted. Unfortunately, in practice, stability considerations assume a dominant role, and are far from being just little engineering details that can be sorted out afterwards.

Messrs McLoughlin, Bennett and Halliday all point out, quite correctly, that though the Quad bridge scheme can theoretically produce zero distortion (ignoring any small distortion in the A amplifier itself), it is liable in practice, when component tolerances are allowed for, to produce considerably more distortion than would be obtained, stability considerations permitting, by removing the local feedback on the A amplifier and employing just simple overall feedback. But if this is tried in practice, what is the result? Oscillation at several MHz, even on a nice simple 8-ohm resistance load. Mr McLoughlin says "no traditional amplifier would contain such a component as C_2" – but what about the capacitor frequently connected between the collector and base of the second stage in many traditional amplifiers? The purpose is the same – to attenuate the loop gain at high frequencies in such a manner as to preserve stability.

The philosophy in the Quad 405 design is to make the A amplifier circuit behave as a clean and simple Blumlein integrator, with 120pF integrating capacitor, up to frequencies of many MHz. This has been done, very elegantly in my opinion, by providing all the mutual conductance for the integrator amplifier by means of a single transistor – the top right-hand one in Mr McLoughlin's Fig. 11. The other two transistors in the integrator amplifier are emitter followers, of extremely wide bandwidth, serving merely to raise the input impedance appropriately. This integrator circuit, fed from the high output impedance of the 405's input stage, Tr_2, provides such an enormous effective forward gain at medium and low audio frequencies that there is simply no need, at such frequencies, to bother about any clever bridge techniques. The impedance of L is negligible, and for all practical purposes the amplifier just has overall feedback directly from the output terminal – indeed it virtually becomes just what Mr McLoughlin and his friends would advocate. There is about 68dB of overall feedback at 1000Hz, for high signal levels, and more still at even lower frequencies, giving extremely low distortion. At 10kHz, because of the reduced forward gain, the distortion, with L short circuited, would be nominally ten times greater than at 1000Hz, though still pretty small. With L in action, however, this increase in distortion is largely prevented from occurring.

Now in any practical class-B audio power amplifier aiming at extremely low distortion, as anyone who has carried out practical design work will know, there are always distortion mechanisms additional to those considered in the idealized theory. By the very nature of it, a class-B power amplifier inevitably has some amps of highly non-sinusoidal current flowing in the two halves of the output stage, and a certain amount of unwanted coupling between the conductors carrying these currents and the input circuit conductors is unavoidable, especially at high audio frequencies. A mere thousandth of a microhenry in the wrong place can easily provide the dominant distortion-producing mechanism at 10kHz. Because of such considerations, it becomes pointless to try to carry the distortion-nulling technique involving L beyond a certain degree of precision, and tolerances no closer than ±5% have therefore been specified for the bridge components. Also, in view of the extremely high effective forward gain of the integrator amplifier, it would be quite meaningless to adopt any of the more elaborate formulae for bridge balance mentioned by Mr McLoughlin, and the design has therefore simply been based on $L=CR_1R_3$, with a slight correction, in no way critical, to allow for the effect, explained by him, of R_{12} in the base of the input transistor. To say, as he does, "R_{12} is causing unpredictable consequences and it must go" is really just nonsense, and seems to show a lack of awareness of the spendidly uncritical nature of the design.

Indeed, uncriticalness is the dominant virtue of the 405 amplifier and is one of the reasons for its relatively low price and great commercial success. The recipe, in a nutshell, consists of zero-biassed output transistors, a 47 ohm resistor to give some transfer of signal even at very low signal levels, an enormous amount of overall negative feedback at low and medium frequencies to give extremely low distortion, plus the application of feed-forward error correction, bridge technique, or instantaneously-variable negative feedback (take your pick!) to keep the distortion low at high frequencies too.

The fact that the feed-forward error correction technique is theoretically capable of yielding *zero* distortion seems to be what academically-inclined people have concentrated upon – it is an attractive idea – but of course, if relied on too heavily and not used in combination with a large amount of overall negative feedback, everything becomes rather critical, thus providing an opportunity for plenty of mathematics! I regard the use of an integrator in the forward path of the 405 as being truly a master stroke, rendering the design as uncritical as possible while also providing proper stabilization of the overall feedback loop. The slew-rate performance is such that the amplifier can properly cope with the most exacting digitally-recorded programme material.

The real engineering virtue of the Quad 405 scheme for audio power amplifiers is not that it enables lower distortion to be obtained than is possible by other means – for the best amplifiers not using it give quite low enough distortion – but rather that it enables a crude current-dumping, unbiassed output stage to be employed, having neither adjustments nor long-term drift and thermal problems, but without producing an amount of high-frequency distortion that many people would regard as too high. (Actually I would question whether a very critical listener would be able to detect the effect of shorting out the inductor L on any normal programme material, though the effect is just audible on sine-wave tone.)

When all aspects are taken into account, it seems to me that the elegant combination of unconventional circuit design techniques embodied in the Quad 405 represents a true advance in the field. The practical exploitation of these ideas has also been carried out in an exemplary manner, and I feel it was most appropriate that this excellent British product should have been selected for a Queen's Award to Industry. I think it is to be deplored that *Wireless World* should have lent its support to the misleading conclusions reached by Mr McLoughlin in his otherwise quite impressive articles.

Peter J. Baxandall
Malvern
Worcs

PS There is one specific mathematical point I would like to bring up. I am puzzled by the statement in the second article, at the top of the middle column on page 35, that "when currents and voltages depart from the sinusoidal, the symbols Z_2 and Z_4 have no meaning", for surely the whole basis of Heaviside's "operational impedance" concept is that these impedances are $Z_2=1/pC$ and $Z_4=pL$, where p means d/dt and is equal to jω in the particular case where sine waves are involved. Thus one may certainly note the current through C and multiply by 1/pC to obtain the voltage, for 1/p is the inverse of p and means integration with respect to time. Thus $V=(1/pC)\times I$ means $V=\int(I/C)dt$. For the inductor we have $V=pL\times I$, meaning that $V=d/dt(LI)$, or $V=LdI/dt$ for fixed L, which is a very well known result.

Mr McLoughlin says "the ratio V/I wanders through most values from zero to infinity throughout the cycle" – but so it does with sine waves, for with reactive elements V and I are in quadrature.

Certainly the distortion-nulling technique involving C and L is just as theoretically sound when considered in relation to transient waveforms as it is with sine waves.

HERETICS

Dr Scott Murray's amplification in the October letters of his discussion of the experiments by Aspect *et al.* is reasonable in so far as he confines himself to what was actually measured, but completely wrong about the interpretation of the measurements. In the first place it was not assumed that when the two cascade photons are emitted from the calcium atom they are polarised identically. In fact the angular momenta of the three states of the atom are known, those of the highest and lowest energy states being zero. This knowledge allows one to deduce from quantum mechanics the polarization properties of the two photons. The calculations show that:

– If photons travelling parallel to the Z-axis are observed with an ideal detector of right-hand circularly polarised photons it will respond to just half the photons passing through it. Whenever it responds to a photon and the other photon is emitted in exactly the opposite direction it too will be found to be right-hand circularly polarized. A similar set of statements holds for left-hand circularly polarized photons from the calcium atom.

– If photons travelling parallel to the Z-axis are observed with an ideal detector of photons line-polarized parallel to the X-axis, it too will respond to just half of the photons passing through it. Whenever it responds to a photon, and the paired photon is emitted in exactly the opposite direction, it will be found to be line-polarized parallel to the X-axis, while if the second detector is set up to respond to photons line-polarized parallel to a direction normal to the Z-axis and making an angle θ with the X-axis, the coincidence rate between the two detectors will be reduced by the factor $\cos^2(\theta)$. A similar set of statements holds whatever direction normal to the Z-axis the first detector is set up to select.

So far as I know this combination of polarizations and polarization correlations cannot be realised in classical optics. One may note in passing Dr Murray's comment about 'how little it (i.e. the quantum theory) has to say even within the field it claims to cover'. The quantum theory predictions have been confirmed by experiments, in part of course by Dr Aspect's experiments.

Secondly the generalized Bell inequalities specifically do *not* involve quantum theory, but only the basic ideas of Special Relativity and the *rejection* of the notion of action-at-a-distance. They are clearly violated by the Aspect results, which give too high a relative coincidence rate between the two detectors for values of the angle θ between the settings of the two polarimeters in the neighbourhood of 22½ degrees.

Thirdly, the 'hidden variables' theories are not quantum theories, but seek to reproduce the experimental predictions of quantum theory by a deterministic theory, with random unobserved variables accounting for the fluctuating results associated with the uncertainty relationships. Though Dr Murray doesn't realise it, the people putting forward these theories are more or less on his side! The Bell inequalities still hold when one uses such theories, but do not require that one should use them. The article by Clauser and Shimony[1] provides an extensive account of these matters for anyone prepared to wade through some heavy mathematics.

C. F. Coleman
Grove, Nr Wantage
Oxfordshire

Reference

1. Clauser, J. F. and Shimony, A. Reports on Progress in Physics 41 (1978) 1881-1927.

The articles by Dr Scott Murray, together with the controversial inconsistencies outlined by I. McCausland regarding the theory of special relativity, have given rise to arguments typical of those misunderstandings, about any subject, that occur where one or more of the words used are not defined.

I consider a word as being defined only when it has one and only one stated meaning.

The following words which are fundamental to physics are not defined according to this criterion: mass, force, energy, velocity, acceleration, and time. Thus any theory using one or more of these words cannot be regarded as rigorous.

It was H. Dingle who pointed out that the word time has at least three meanings i.e. is not defined, and as a result it follows that the other words just listed, which are expressed, directly or indirectly in terms of time have themselves at least three meanings.

A recognition of the absence of definitions for these and other words, is the first and main step required of physicists if they are to extricate themselves from the morass of inconsistencies they have struggled through during the last 50 years. I can assume then that, if they were to take this step, new and comprehensible theories can be postulated which comply with all the known phenomena and more importantly add greatly to one's understanding of nature without the need for virtually incomprehensible mountains of mathematics.

David A. Chalmers B.Sc.
Finchley
London N3

I note with some relief that Dr Osinga (Letters, July) admits to the possibility of there having been oversights and omissions regarding the M-M experiment.

The reply to his problem concerns the conflict between the classical and relativistic viewpoints together with the indoctrination, given by modern teaching, which tends to force those things further apart.

In his book, mentioned by McCausland, Rudakov uses the phrase (re the M-M experiment): "The result of the experiment indicated that there was something wrong with the assumptions."

That phrase epitomizes Dr Osinga's problem because, whatever any scientist might try to have you believe, the assumptions were never tested.

Light has a velocity which is constant with respect to space, or if you are of courage the aether, and thus with respect to the experiment it is inevitable that the velocity *of the wavefront* shall vary.

Taking those things into account together with Doppler we may be sure, if we are to as a last resort cling to reason, that the experiment constituted an unequivocal disproof of the relativistic tenet that length varies with relative velocity.

We must always remember that an experiment may never prove a theory but that it most surely can disprove it, as is the case with the much misinterpreted M-M experiment.

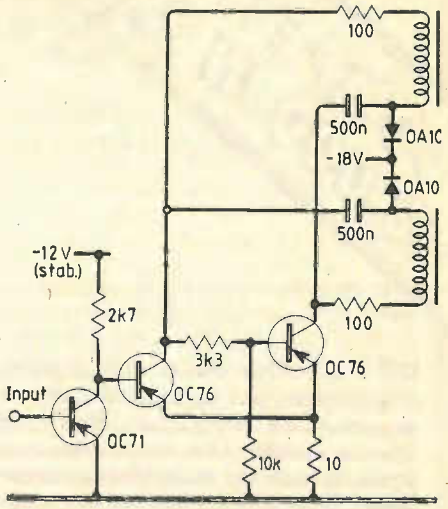
A. Jones
Alderney
C.I.

NANOCOMP/TTY INTERFACE

The problem of interfacing a teleprinter from low-voltage logic circuitry was tackled by a prototype design team some 24 years ago when transistor types like those used by P. C. Barton were not available (*Wireless World*, October 1983, p.75).

Some truly awful circuits were dreamed up and considered, including twin transistorized Cockroft-Walton ladders and an arrangement we called an oscillating totem-pole.

The latter circuit worked quite well but was



felt to be not the sort of thing that deserved the cost of a patent application; the firm therefore published it to prevent anybody else from doing so (*Electronic Engineering*, May 1961, p.278.)

It was then realised that the two coils of a type 7B teleprinter could be separated and driven in antiphase; also, with the bias spring disconnected, the selector lever could be held at "0" or "1" by a very small current and the 75 volts minimum specified by the t.t.y. manufacturers was required only at the moments of transition to get the coil currents changing fast enough to follow the code groups.

This led to the design of the circuit shown here in which the inductive surge generated as one coil is switched off is superimposed on the supply voltage applied to the other coil to get the current in that moving promptly.

This allowed such a dramatic reduction of the supply voltage required that the teleprinter could be driven as shown from the unstabilized rail in the power supply for the logic circuitry.

I have never seen this technique used since.

J. C. Rudge
Harlington
Middlesex

ETHERNET

In the News column of your October 1983 edition you include a paragraph entitled "Ethernet wins one race". In the article you imply that CSMA/CD has been adopted as the sole Media Access technique under IEEE 802. This is not the case. The IEEE forwarded three documents to the Peking meeting of ISO/TC 97/SC6: Logical Link Control (802.2), CSMA/CD (802.3) and Token Bus (802.4). The absence of the Token Ring document (802.5) from this list is only indicative of the late start this Media Access technique had. Indeed a letter was sent to the Peking meeting stating that it was intended to submit a Token Ring document at a later date.

Work is continuing in IEEE Project 802 on wideband systems which may well appear before ISO in the future. The Token Ring standard is by far the most 'active' document at present as the working group responsible for it (of which I am a member) strive to catch up with the other parts of Project 802. A Media Access Technique very similar to the IEEE 802 Token Ring has been submitted to ANSI X3 T9.5, the speed of operation of this ring is intended to be 100 Mbit/s, a speed at which not many designers would think of using Ethernet.

Ian Watson
British Telecom

COMPETITION (£8,000 IN PRIZES)

Wireless World Competition

Electronic devices for the disabled

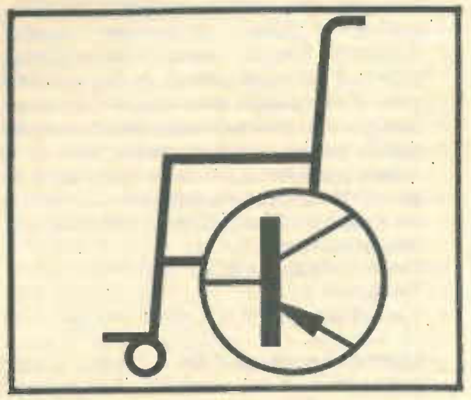
Our competition closed with numerous completed entries: an impressive response in view of the many distractions of the summer months. They range from simple domestic items up to complex computer-linked projects; and one of the judges' hardest decisions will be in finding where lies the greatest benefit to the disabled. This page shows a selection, though mention here should not be taken to imply endorsement.

Arrangements for the judging and presentation of awards have yet to be finalised, but we have fixed a date (30th January) and will announce fuller details soon. A short-list of the most promising entries will be compiled by the *Wireless World* editorial staff, to reduce the task of the judges to manageable proportions; and in the case of short-listed entries which have been submitted in paper form only, we shall then request the devices themselves for demonstration.

To select the prize-winners we have invited the following:

- Mr Bill Bond, Principal Lecturer in the Mechanical Engineering Department of the Polytechnic of the South Bank in London. Mr Bond runs Britain's only degree course in engineering product design. He is also involved in work for the handicapped.
- Miss Elizabeth Fanshawe, Director of the Disabled Living Foundation. The Foundation is a charitable trust; it operates an information service and conducts research connected with aspects of ordinary life that present problems to disabled people. Miss Fanshawe is an occupational therapist and is herself disabled.
- Mr David Gemmell, Managing Director of Possum Controls Ltd, which manufactures a range of electronic aids for the disabled.
- Professor Meredith Thring, former head of the Department of Mechanical Engineering at Queen Mary College and author of many books on engineering in theory and practice.
- Professor Heinz Wolff, head of the new Brunel Institute for Bioengineering at Brunel University, Uxbridge. Part of the Institute's work is connected with technological aids for the elderly and disabled.

One of the first parcels to arrive, and physically one of the smallest, brought us the Talking Box from Mr Ian Mitchell of Hull. Scarcely larger than a pack of cards, this contains a speech synthesiser and a tiny loudspeaker. At a touch on the keypad,



out comes your choice from a couple of dozen phrases of everyday usefulness ("please can I go to the toilet?"); for greater versatility an external keyboard can be plugged in.

The problem of communications for the handicapped seems to invite solutions in electronic form and has been a recurring theme in the competition. Another entry connected with speech difficulties was brought to Quadrant House by one of its co-designers in person. The Hector Speech Aid is a gadget to help overcome stammering: hidden on the body, it discreetly provides a stabilising 'feedback' to the ear. We hope Mr Ron Turrell won't mind if we reveal that his stammer is ordinarily quite severe, because with his device in action it seemed to vanish altogether.

An unusual entry in the medical field is a pain-inhibiting pulser from Mr Ray Lightwood, who works at the Queen Elizabeth Hospital in Birmingham. This is a small battery powered stimulator, complete with skin electrodes, and is intended to give relief to sufferers from severe intractable pain. According to many authorities, electrical stimulation can release natural opiates, the body's built-in pain relievers.

Distress alarms are a common need for the elderly or disabled, and we have received several. One of these uses a portable infra-red transmitter: this sets off the alarm via a remote pick-up point feeding signals through the mains wiring. Another, designed for multi-occupied housing, employs low-power h.f. radio links giving seven separate alarm circuits. Remote control techniques have been adopted by several other entrants to provide easy operation of household electrical items.

On the lighter side, one intriguing little entry is an aid for computer games players. Computer games, believe it or not, have a useful function in developing co-ordination; though for disabled children the average zap-the-aliens game often runs much too fast. But with the 'Slowcoach' board in the computer, they're in with a chance.

For this tetraplegic computer programmer, a computer interface designed by Dr Michael Bolton and Mr Alastair Taylor means full-time employment.

Forth language

Forth consists of words and new words must be compiled and entered into its dictionary. Following a description of the dictionary and compiler, Brian Woodroffe discusses advanced concepts in this third article.

by B. Woodroffe

Having shown how the address interpreter executes lists of addresses to execute program commands and that threaded code is compact, I will now explain how Forth builds these lists, i.e., how it compiles. Each list representing an action is rather like a verb in a natural language and in Forth is called a WORD. The collection of these words, which is Forth, is known as the dictionary. The outermost WORD in Forth breaks input text down into character strings which it then searches for in the dictionary. (Spaces are important, for instance, '−1' is treated as a negative number, whereas '− 1' is treated as the arithmetic subtraction operator followed by the positive number one.) If the string is found, it is executed, otherwise an error message is generated. The dictionary also needs a mechanism to allow the search to occur. Searching involves a traverse of all the words in the dictionary. Each entry has a pointer to the previous one (link field), which makes the dictionary a linked list. To enable matching of the source text each word also has its name in ASCII form (name field). Dictionary entries for each word, List 1, have four fields – name field, link field, code field and parameter field. The name field also contains data for use by the compiler (precedence and smudge bits) as will be explained, and it includes the length of the name to allow variable name lengths of up to 31 characters.

For language expansion it is important to be able to build dictionary entries for new words. This is done by invoking the compiler. When the compiler is invoked (Forth word ':'), the language state is switched from execution to compilation. Next, input text is scanned forward for the next text string which is used to build a newly created name field. The name is 'smudged' so that during the building of the incomplete definition, the same name cannot be found. This normally prevents recursion, but again in Forth, this rule can be overcome, List 2. Then the linked list of the dictionary is updated by copying it into the dictionary link and the address of DOCOL is copied as this new word's code field. Next, input text is scanned for character strings. As these character strings are matched with words that already exist in the dictionary, the code field of each word found is copied into the parameter field of the word being compiled. Finally, as the word to terminate compilation is encountered ';' SEMIS is copied as the last word of the definition and the Forth program is returned from the compile state to the execution state. The compiled word is now 'unsmudged' to allow it to be accessed.

The compile process can be quite long as many dictionary searches have to be made. As the dictionary is a linear list and the code routines which ultimately have to be compiled are at the bottom, it is a long search. No speed up algorithms such as hashing have been applied to standard FIG Forth though there has been experimentation[8,9,10]. As so much work is done during the compile phase the execution performance of newly defined words is nearly as quick as predefined words. Further, as the first half of the dictionary entry

List 1. Each dictionary entry has four fields called name field, link field, code field and parameter field.

```
            Dictionary entry
            7 6 5 4 3 2 1 0
NFA         1 p s < 1 e n >    p=precedence, s=smudge, len=length of name
            0 a s c i i 1
            0 a s c i i 2      ASCII characters of word
            0 . . . . . .
            1 a s c i i n      d7 set on last character of name
LFA         <             >    16 bit address of previous n.f.a.
CFA         <             >    16 bit address of code routine
PFA         <             >
            <             >    parameters, normally other c.f.as
            <             >
```

List 2. Example of recursion in Forth to calculate a factorial.

```
First define
: MYSELF
    LATEST               ( put address of word currently being defined on stack )
    PFA CFA ,            ( convert to code-field address and compile )
                         ( it in dictionary so that it may call itself )
    ; IMMEDIATE          ( as this word is to execute when in the compile state it has
                         'precedence'. )
Then use myself in the recursive definition
    : FACTORIAL ( n . . . )
      DUP 1 = IF ELSE    ( end of recursion?, yes leave 1 as 1!=1 )
      DUP 1 −            ( n, n−1 . . . )
      MYSELF             ( call myself to calculate n−1! )
      *                  ( n!;=n*[n−1!] )
      ENDIF
      ;
```

List 3. Definitions of IF, ENDIF and ELSE.

```
: IF
  COMPILE 0BRANCH      ( compile into the dictionary the c.f.a. of '0BRANCH' )
  HERE                 ( place on stack where we are )
  0,                   ( make space for jump offset )
; IMMEDIATE            ( make compiler execute this word, even if in compile state )
: ENDIF
  HERE                 ( where are we? )
  OVER −               ( calculate offset to HERE executed in IF )
  SWAP !               ( patch in offset to address left by IF )
; IMMEDIATE
: ELSE
  COMPILE BRANCH       ( compile run time address of routine to skip false statements )
  HERE 0 ,             ( make space for jump offset )
  SWAP                 ( get address of where IF was )
  [COMPILE] ENDIF      ( use ENDIF to fix address, ENDIF is immediate and to overwrite
                       that such that it is compiled )
; IMMEDIATE
```

List 4. Examples of VARIABLE and CONSTANT.

```
: VARIABLE
    <BUILDS          ( variable is a new parent word )
    ,                ( store in the p.f.a. the value that was top of stack )
    DOES>            ( start defining what offspring will do )
    ;                ( nothing – p.f.a. is storage location for an offspring of type VARIABLE )
: CONSTANT
    <BUILDS ,
    DOES> @          ( constants provide a constant value which has been )
    ;                ( stored in their p.f.a. )

0 VARIABLE ABC       ( ABC is an offspring with initial value 0 )
1000 CONSTANT K      ( K is an offspring of value 1000 )
```

(name and link fields) is only required during compilation for fixed applications where compilation is not required, these fields can be deleted. This dramatically reduces the memory requirements of the Forth system[11], and can be especially useful when the code will be placed in rom.

To enable the compiler action of Forth to do more than just that described above certain words need to execute even when the language is in the compile state. This gives the compiler the full capabilities of Forth. These words are generally involved in building control structures for the compiler (IF-ELSE-ENDIF, see List 3). These words have a precedence bit set which the compiler recognises when it matches the input text so instead of compiling its code field it executes it. In the case of IF the compiler compiles into the dictionary the c.f.a. (code-field address) of 0BRANCH and advances the dictionary pointer to allow the as yet unknown offset to be placed. It also pushes this address onto the stack so that when the compiler encounters an ELSE or ENDIF statement it can calculate the offset back to the IF statement and store the offset there. This shows the power of Forth in that the computational ability of the language is available to the compiler and to the user. Further there are times when words that would normally execute (i.e. have precedence) need to be compiled (i.e. execution action delayed until the word currently being defined executes). This is done using the word [COMPILE]. Again, it is sometimes required to delay compilation of a word until the word that contains it executes. This is done using the word COMPILE.

Advanced concepts

With an idea of how the inner interpreter (address interpreter) and the compiler (text interpreter) work we can now move on to advanced concepts including extension, vocabularies and virtual memory. Forth is either in the compile state, when it finds words and copies their code-field addresses into the dictionary to form new entries, or in the execute state, when it executes each code-field address encountered. I have shown how certain immediate words can override the state, and can even execute in the compile state. It is also possible to overrule words which are declared as immediate and compile them, as in the case of ELSE which was described earlier.

In Forth, even the compiler can be modified. Not only can new compiler control structures be introduced but also new compiler words may be defined. Normally the programmer would have to rewrite the compiler but with this feature, known as extensibility, modification is relatively simple. It involves use of the words <BUILDS and DOES> to define a new class of words. The defining word defines words of this new class. Behaviour of the new defining word is determined by the words between <BUILDS and DOES>, i.e. when a word of the new class is defined, behaviour of the new word during compilation is determined by what comes between <BUILDS and DOES>. When a word of this new class executes, it executes the words following DOES>. To allow the parent class-defining word to access its offspring (class-defining word to access its offspring (class-defined word), the parameter-field address (p.f.a.) of the latter is placed on the data stack. Two simple examples from the Forth compiler are VARIABLE and CONSTANT, List 4. These can easily be expanced to form arrays and tables. The word ':' is also a defining type. When offspring of ':' are executed they call the word DOCOL which decides how to execute their parameter field. An alternative to DOES> is used to define ':'; the assembler is invoked so that the parent-word execution field is machine code and not Forth but in other respects it is the same.

The major part of Forth is the dictionary, and to enable different problems to be solved in different areas of the dictionary each problem is given its own vocabulary. The dictionary may have many vocabularies alongside the normal basic set of FORTH, ASSEMBLER and EDITOR. Using vocabularies means that the same word may have different meanings, depending on which vocabulary is active. FIG-Forth has two active vocabularies – CURRENT and CONTEXT. The former is the one in which words are defined and the latter is the one which is searched first. All vocabularies are linked to FORTH (Forth's definition in Forth). Much debate is taking place on the subject of vocabularies concerning the subject of searching vocabularies [11 – 13].

Virtual memory

Memory is the most precious resource of a computer and although Forth makes very efficient use of it, there are still times when programmers wish it was infinite. Disc memory is much cheaper than semiconductor memory but it is also slower. By the concept of virtual memory, the memory space available to the programmer is expanded beyond the main memory to include disc storage so memory capacity as far as the programmer is concerned is only limited by the capacity of the disc. In Forth, the virtual-memory cancept is only applied for data whereas in most processor applications (e.g INS16000 series) it is also applied for program storage. Through use of the word BLOCK, the programmer can visualise the disc memory as processor memory. The Forth operating system recovers data from disc and places it in a buffer to make it accessible to the user program. Many such buffers exist in the host processor and BLOCK uses an algorithm that determines which blocks should be maintained in the store and which should be written back to the disc. With the right algorithm the number of disc accesses will be minimal and the apparent memory-access time low.

Forth words used in last month's program example

Stack operators

DUP pushes the top of the stack on to itself so the stack increases by one and the top and second stack elements are equal.

SWAP interchanges the two elements at the top of the stack.

OVER places a copy of the second element in the stack on the top. The original top element is now second and all other elements move down one.

ROT takes the third element and makes it the top element so the old top element becomes second and the old second element becomes third.

Arithmetic operators

MINUS replaces the top stack element with its two's complement.

+ takes off the top two elements, adds them and pushes back the result which becomes the new top of stack.

– takes off the top two elements and pushes back the result of second element minus the top element.

* takes off the top two elements, multiplies them and pushes back the result.

/ takes the top two elements, divides the second by the first, and pushes back the result.

n pushes the value of n on the stack.

SQRT takes the top two elements, treats them as double precision (32-bit), and pushes back the 16-bit square root.

0< if the top stack element is less than zero it is replaced by a one (true), if it is not less than zero it is replaced by a zero (false).

Control operators

IF tests and deletes the top stack element and executes the next word if the condition is true. If the condition is false, control skips to ELSE or ENDIF, whichever comes first.

ELSE marks the end of the IF-TRUE clause and the beginning of the IF-FALSE clause.

ENDIF is the end of an IF clause.

Terminal operators

CR sends a carriage return and line-feed signal to terminal.

." starts text entry into the dictionary (until""). When executed it will type out the text string.

. converts the top of the stack to an ASCII string and types it out.

Space and time

I have shown how the Forth dictionary is created (i.e. its form), how it may be extended by compiling and how any processor may readily simulate the virtual Forth machine by means of indirect threaded code. As mentioned earlier, by introducing the concept of threaded code, execution speed is traded for code space. So one can expect that Forth is not as fast as the host processor's own code although it may approach it where many subroutine calls are made. Execution of a process defined in the source language divides into two parts; one is the examination of source text to find out what action is to be taken and the second is execution of the actions by the processor. In most systems the first part is carried out by compiling source text in the machine code of the host machine. In Forth this means compiled into the thread, the machine code of the hypothetical machine. Target machine code is then run in Forth using the address interpreter. Running time can be traded for space by choosing an intermediate language of suitable complexity. Running time performance of compilation has no effect on the running time of the application program, which leads to the view that the compiler should do as much work as possible. Unfortunately, compiling to machine code using a simple processor with limited addressing capability, such as a current 8-bit microprocessor, often results in the code not fitting into the memory so an intermediate target code is chosen, with the accompanying penalty of interpreting it. Forth's address interpreter costs some tens of percent.

Other losses occur because microprocessors are not zero-address devices so the zero-address function has to be simulated. Memory-space benefits are illustrated by the amount of memory required for a Forth system, which is typically 8Kbyte (may be rom) for virtual-machine simulation, the Forth compiler, i/o drivers, etc., and 8K for stacks, virtual-memory buffers and the user dictionary.

Forth is also fast because of the explicit use of the stack. In languages using the assignment operator, data normally resides outside the stack. It is brought to the stack, operated on, and finally placed back into the store. If the next statement uses the same variable it is once again taken from the store and placed on the stack. When computing partial results this causes excess memory traffic. Unless optimization is used this redundant memory activity will cause delays. Forth avoids this because normally data only resides on the stack. No unnecessary memory space or time is taken up by temporary variables.

It is interesting to compare Forth's performance with the commonly used language for microprocessors, Basic. Systems using Basic have little compiler action, the source text being saved in memory, although the key words are converted into internal tokens. During program execution, each token is parsed and acted upon in turn so the source of Basic's execution-time interpreter is close to that of the source text whereas Forth's source for the running-time interpreter is close to the language of the host computer. As all the work in a Basic system is done while the program is running the speed penalty is high, usually at hundreds of percent. Further, since Forth compresses object code into 16-bit addresses (code-field addresses are the equivalent of tokens) it is as efficient as Basic in terms of memory space.

Processing speed is an emotive issue without benchmark tests and unbiased benchmarks are notoriously difficult to produce. Table 1 was derived using the Seive of Eratosthenes (see List 5) and seems fair[14]. Qualitatively, it confirms what one could expect – assembly-language is faster, followed by compiled languages with interpreted Basic well behind. The table also shows how well the 6809 compares with newer and more popular designs and that it compares with at least one 16-bit device, the 8086. I would attribute this to the instruction set as was shown in the analysis of Forth word NEXT. A more elaborate, special-purpose instruction set does not necessarily lead to a more effective processor. This has been shown in recent research into reduced instruction set computers.

continued on page 61

List 5. Representation of algorithm used for benchmark test, see Table 1.

```
8190 CONSTANT SIZE
0 VARIABLE FLAGS SIZE ALLOT             ( allocate 8191 bytes for an array )
: DO–PRIME
  FLAGS SIZE 1 FILL                     ( fill array with '1', <true> )
  0                                     ( counter )
  SIZE 0 DO                             ( set up a DO loop of 8190 times )
  FLAGS I + C@                          ( I is loop counter, get relevant flag )
  IF                                    ( C@, C! are byte versions of @,! )
            I DUP + 3 + DUP I +         ( stack is . . . count, prime, K )
    BEGIN                               ( begin a block )
      DUP SIZE <                        ( array index < size ? )
    WHILE                               ( test flag, to see if exit block )
    0 OVER FLAGS + C!                   ( set relevant flag false, FLAGS[K] )
    OVER +                              ( K:=k+prime )
    REPEAT                              ( end of block, loop back )
   DROP DROP 1+                         ( delete prime, K; one extra prime found )
   THEN                                 ( end of IF )
LOOP                                    ( end of DO . . . LOOP block )
. ." primes" ;                          ( print number of primes )
```

Table 1. Relative speeds of various processor and languages.

Processor/language	Time in seconds
CRAY-1 Fortran	.11
68000 assembly language (8MHz)	1.12
PDP11/70 C	1.52
VAX 11/780 (C/Fortran/Pascal)	1.5-5.0
8088 assembly language (15MHz)	4.0
6809 assembly language	5.1
PDP11/40 C language	6.1
Z80 assembly language (4MHz)	6.8
6809 IMS Pascal compiled (2MHz)	8.9
PDP11/70 Decus Forth	11.8
Z80 Microsoft Basic compiler	18.6
8088 Pascal (Softech compiler) (15MHz)	19.4
68000 Forth (8MHz)	27
6809 FIG Forth (2MHz)	45
8088 FIG Forth (15MHz)	55
8086 FIG Forth (12.5MHz)	64
6809 FIG Forth (1.5MHz)*	67
Z80 Forth (Timin) (4MHz)	75
Z80 Forth (Laboratory Microsystems) (4MHz)	78
Z80 FIG Forth (4MHz)	85
6809 IMS Pascal P-code (2MHz)	105
6809 Basic 09 (2MHz)	238
6502 FIG Forth (1MHz)	287
6809 TSC Basic (2MHz)	830
Z80 Microsoft Basic	1920
APPLE integer Basic	2320
TRS80 Microsoft Basic	2250
6809 Computerware Basic	4303

* Used in my design as described in *Wireless World*

Assembly language programming

In learning assembly language programming one must also know how to write programs to suit different microcomputer systems. In his eighth tutorial, Bob Coates looks more closely at elements of Picotutor and describes its use as a stop watch to demonstrate the hardware timer.

In this article I describe Picotutor in more detail, looking in particular at how the keypad and display operate. To demonstrate the hardware timer within the microprocessor a description of how to program Picotutor as a stop-watch is included. A disadvantage with assembly language programming is that each microprocessor has its own unique language so to demonstrate the subject one has to choose a particular processor. To complement this series I designed a small microprocessor trainer based on an eprom version of the 6805 – the 68705 – which was described in the December 1982 and January 1983 issues of *WW*. The 68705 is primarily intended for small industrial and consumer single-chip control applications, as opposed to microprocessors such as the Z80 and 6809 which are intended for use in larger computers, and can only be programmed at assembly language level.

Two main considerations when designing Picotutor were low cost and simple construction. As a result, it is not possible to enter programs directly in assembly language; they must be converted to machine code by hand. For beginners hand assembly has the advantage that it gives one a greater appreciation of the subject and for small programs it is quite adequate. All examples given in this series have been hand assembled.

Reading the keypad

Operation of the keypad and display was described in the December 1982 issue. To recapitulate, peripheral ports B and C of the 68705P3 microcomputer are used to interface the keypad and display. Reading of the keypad and driving of the display are performed by software in the monitor program and four sub-routines can be used in user programmes to provide these functions.

KEYIN scans the keypad and returns with a code in the accumulator (A) for the key currently being pressed. If no key is being pressed (or more than one key) the accumulator is cleared.

DISKEY performs a dynamic refresh of the multiplexed display with data contained in six ram registers (one for each display digit). The state of each bit in each ram register byte indicates whether its associated segment in the display should be lit or not. When the display function is complete, KEYIN is executed before the subroutine returns.

DISGET repeatedly calls DISKEY (giving continuous refresh of the display) until a new key is pressed, then returns with its code.

DISHEX calls DISGET and if the key pressed is a hexadecimal key, converts the key code to the appropriate hexadecimal code.

I will first explain what keycodes are and how they are formed. The Texas keypad used is a 6-by-4 matrix of keys, i.e. six column and four row lines, with a switch at each row/column junction (see circuit diagram). Closing a switch causes those particular column and row lines to be shorted together. So with only ten connections to the keypad, the microprocessor can determine which one of the 24 keys is being pressed. The six columns go to port B and the four rows to IC_2, but which connections go to which pins was determined soley by the easiest p.c.b. layout. When it detects a column/row short, KEYIN software produces a unique 8-bit code which may appear to be random. What code is produced doesn't matter, as long as each key-code is unique.

by R. F. Coates

See what code a key produces with the following program.

```
030     BD89   JSR   DISGET
032     83     SW1
```

This program when run will wait, refreshing the display (which will show the last data entered, the 'go' command) until a key is pressed. It will then execute the software interrupt, with the accumulator containing the key-code. The accumulator can now be examined using the reg key and it will give the key-code for the key you have just pressed. Try this program with each key of the keypad and build up a table of key-codes. Now change the subroutine call from DISGET to DISHEX (address 8C) and it should covert the hexadecimal keys to the correct hexadecimal code (00 – 0F), but leave other codes unmodified. Check also that the C bit in the condition-code register is clear if a hexadecimal key, but set otherwise. This is to inform the calling program as to whether or not a hexadecimal key was pressed.

Driving the display

The basic subroutine for driving the display is DISKEY, which also scans the keypad. Digits in a multiplexed display can only be lit one at a time so to give the impression of a multi-digit display, each digit is lit in turn for a short period and when the last has been lit, the first is lit again, and so on. In 'PICOTUTOR', the looping period is about 20ms, so a slight flicker may be noticeable in the display.

As segment data cannot be latched into the display, it has to be stored in ram, and retrieved when required. Six bytes of ram are used to store the data, one for each digit, starting at address 010 which is given the label DISBUF (display buffer). To effect a display, appropriate segment data is stored in the six bytes of DISBUF and then DISKEY is called repeatedly, in a loop. Each bit of a DISBUF byte drives a particular segment of the appropriate digit, a one bit causing the segment to be lit, a zero bit causing it to be extinguished. Bit/segment allocations are shown in Fig. 1. Allocations are not in a particularly logical or convenient sequence as once again, the easiest p.c.b. layout was the determining factor. This example illustrates how to drive the display.

```
030          BDBO   JSR   CLRDIS
032          A6BF   LDA   #%1011-
                          1111
034          B710   STA   DISBUF
036          A675   LDA   #%0111-
                          0101
038          B711   STA   DISBU-
                          F+1
03A  BD83      LOOP JSR   DISKEY
03C  20FC           BRA   LOOP
```

Subroutine CLRDIS sets all 6 bytes of DISBUF to zero, or clears the display. The first LDA instruction sets all bits to one, except bit 6, which will give the display pattern for the number six with a right-hand decimal point. This is stored in DISBUF, which is the r.a.m. byte corresponding to the leftmost display digit. The next LDA instruction sets bits 0, 2, 4, 5 and 6 to one and bits 1, 3 and 7 to zero to give the pattern for numeral three which is stored in DISBUF+1 which corresponds to the next digit to the right. The program then enters an indefinite loop which first calls DISKEY, causing each of the six digits to be lit once (although the last four have been blanked by CLRDIS). The branch-unconditional instruction causes the subroutine to be called again, and so on, giving a continuously lit display until the reset button is pressed.

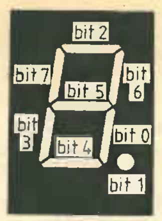


Fig. 1. Bit/segment allocations of Picotutor display.

Display software

Referring to the circuit diagram (*WW* Dec. 82 issue) and List 1 we can see how a software driver for the display is developed. List 1 is an extract from the Picotutor's monitor software showing the portion of DISKEY which drives the display. Looking first at the circuit diagram, to light a given digit the appropriate digit cathode is selected by sinking it to 0V while the others are allowed to rise to +5V. When a 4-bit binary code is written to port C it is decoded by IC_2 which selects the equivalent output, driving it to zero, while the others are at one. At this point, ignoring port B for the moment, all segments of that digit would be lit; all segment anodes are connected to +5V through one of eight 270Ω resistors which allow current to flow through each of the diodes. But if a zero is written to a particular port B pin when port B bits are all programmed as outputs, that pin will provide a short circuit to ground across the diode, diverting its current supply and extinguishing the diode. If port B output is set to one it will pull to +5V and help to light the diode, so by storing the appropriate pattern of ones and zeros in port B, a particular character shape can be produced on the display.

Look now at List 1 to see how Picotutor performs this. Note that segment data is set in port B before the cathode is selected, and afterwards the cathode is disabled before the segment data is altered to prevent a ghosting effect in the display. First, ports B and C are set as outputs, then the same pattern (FF) is stored in address label CATH (port C data register) since all ones to IC_2 disables all outputs. The index register is used as a pointer to the data and is initially set to zero.

At label DSK1, the accumulator is loaded with data from the DISBUF ram for the first digit

LDA DISBUF, X

This is stored in label SEG (port B data register). Next a value is loaded into the accumulator from the DIGSEL table (digit select) which is a table of 6-bit patterns for driving port C to select each of the six-digit cathodes in turn. This value is stored in CATH and at this point, the left-most display digit will light up. A delay loop is now entered to keep the display lit for a short period. This delay loop is a little odd because it is designed to exit with 0F in the accumulator.

List 1. Illustration of a software display driver from Picotutor's monitor.

```
*
*  DIGSEL   –                    Codes for driving 7442 to select left-most to
*                                right-most digit cathode
*
   DIGSEL   DATA   6,5,4,7,8,9
*
*
*
   DSK10    LDA    #$FF          Set up display ports as outputs to refresh disp.
            STA    SEGD
            STA    CATHD
            STA    CATH          Turn off all cathodes
*
            CLRX                 Initialize display pointer
*
*
   DSK1     LDA    DISBUF,X      Get digit segment data
            STA    SEG           Set up segment drive
            LDA    DIGSEL,X      Get cathode drive code
            STA    CATH          Switch on cathode
*
*
            LDA    #$F           Wait for light up period
   DSK2     DECA
            CMPA   #$
            BNE    DSK2
*
*
            STA    CATH          Switch off cathode
*
*
            INX                  Inc. DISBUF pointer
            CPX    #6            Finished all 6?
            BNE    DSK1          Round again if not
```

A value which determines the period of the delay is initially loaded into the accumulator and it is in fact set with the maximum delay value causing 256 iterations of the loop to DSK2. When the delay loop is left, the accumulator contains 0F which is stored in CATH (Port C), disabling the digit cathodes. The index pointer is then incremented and if all digits have not been serviced (X<6) the program loops back to DSK1. This second time round, the index register contains 01 so the two LDA indexed instructions load the second value in DISBUF and DIGSEL respectively. The main loop is executed six times, lighting each of the digits in turn for about 3ms. When refresh is complete, this subroutine scans the keypad. If scanning is not required it can be ignored, but remember that the accumulator is modified by the refresh.

6805 timer

The above display driver routine uses a software loop delay, but the 6805 has an inbuilt hardware-programmable timer which could have been used. The monitor does not use this timer at all so it may be used at will. Once the timer has been set, it causes an interrupt at a predetermined time, which allows accurate time periods to be determined, while allowing the processor to function normally in between. Clock source for the timer can be either the internal system clock or an external clock connected to the TIMER input pin. Gating of the internal clock by the external TIMER input allows pulse-width measurements to be made. A variable prescaler may also be used to extend the range of the timer, which is only eight bits, to give the equivalent of 15 bits and a maximum count of 32768.

There are two registers associated with the timer, the timer data register (t.d.r.) and timer control register (t.c.r.). Input pulses decrement the data register and when it reaches zero, an interrupt is caused; this register may be programmed with an initial value to give the required timing period. The control resister is used to set up the various operating modes and control timer interrupts. Page 00 shows two possible configurations for the control register, one to provide correct emulation of the rom versions of the 6805 and the other to allow software programming of the timer, which is the one applicable to Picotutor.

To operate the timer the mode of operation and the prescaler value is first set, the prescaler cleared, the required count stored in the data register and the timer interrupt mask cleared. Program execution may then proceed, but will be interrupted when the count in the timer data register reaches zero. The interrupt-service routine must then clear the timer interrupt-request bit before it finishes and then return control to the main program. This gives very briefly one way in which the timer may be used. I do not intend to cover all the details of the timer as these are adequately covered in the manufacturer's data

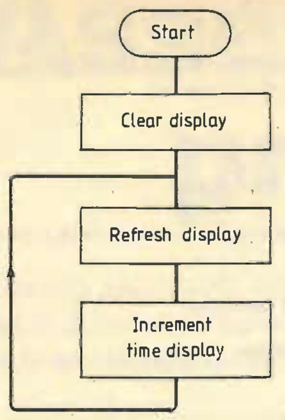


Fig. 2. Flow diagram for a software timer.

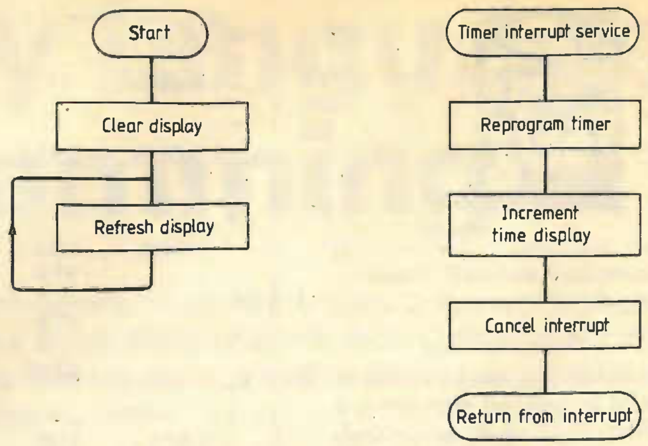


Fig. 3. More precise timing is possible using an independent hardware timer.

sheet but there follows an illustration of one use for the timer and an example.

Simple stopwatch

Implementation of a stopwatch on Picotutor requires a continuous display of elapsed time using continuous calls of the subroutine DISKEY, and some means of keeping an accurate track of time. It is possible to implement a software timer function, but there are considerable difficulties involved. Figure 2 is the flow diagram for a software timer. It is important that the loop takes an exactly known and constant amount of time to execute. If it took 100ms for instance, the time display would increment every tenth of a second. Although DISKEY takes a fixed amount of time to execute (if no key is pressed), time incrementation will vary according to whether a carry between digits is required. For instance, if the least significant digit is nine, then it must be cleared rather than incremented and the next digit incremented instead, or if that is nine, cleared and the next one incremented, and so on. If no carry function has to be performed, these operations can be skipped and operation will be much quicker. To ensure that exactly the same time is taken each time round the loop, blocks of no-operation instructions or some other form of delay must be introduced for the shorter execution paths to ensure that all possible paths are exactly the same length. This is difficult and time consuming to program correctly.

A much better solution is to use an independent hardware timer to keep track of time precisely so that time taken to perform software loops no longer matters. Figure 3 gives the flow diagram for such an operation. The main program merely has to keep refreshing the display, and every so often it is interrupted in the middle of its task by the timer, which causes an interrupt at regular intervals. When an interrupt occurs, the c.p.u. pushes the current contents of all registers including the program counter on the stack to save them. It then gets the address of the interrupt-service routine, puts that in the program counter register then carries on processing from the new program-counter

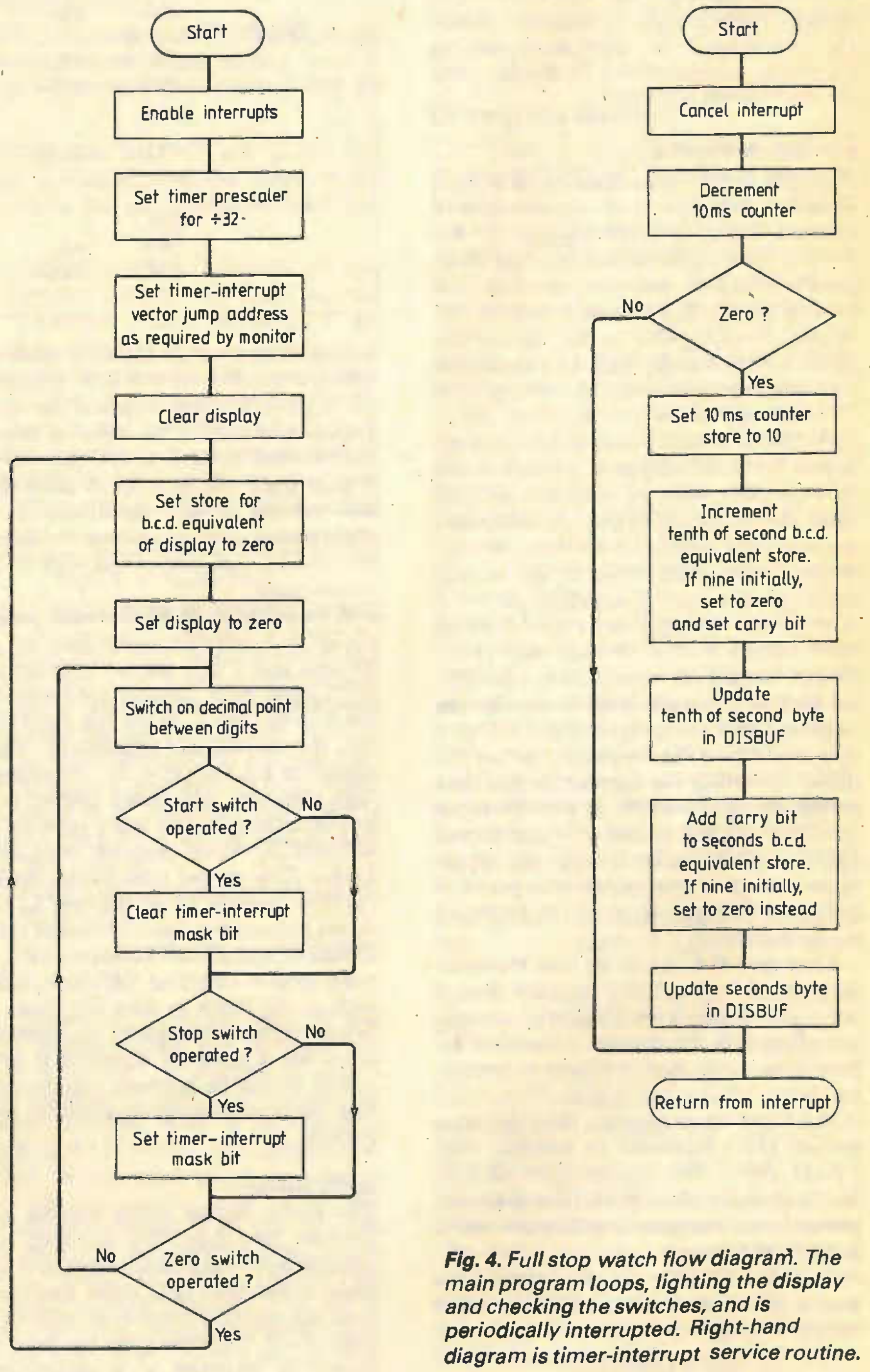


Fig. 4. Full stop watch flow diagram. The main program loops, lighting the display and checking the switches, and is periodically interrupted. Right-hand diagram is timer-interrupt service routine.

address. Incrementing of the time display is done here and if it takes a varying amount of time, it doesn't matter as the timer is re-armed first and is already counting away the time to the next interrupt. The service routine must of course take less time than the interrupt period or there will be problems!

The last instruction of the service routine will be a 'return from interrupt' (RTI). This pulls all the registers off the stack to restore them, then carries on processing the main part of the program from where it left off.

Stopwatch flowchart

Figure 4 is the full stop-watch flow diagram. This stopwatch uses three port A inputs to provide start, stop and zero functions for the two-digit stopwatch which counts in tenths of seconds. Three of the eight dual-in-line switches are used for this function. The stopwatch itself is divided into two entirely separate parts. After an initialization section, the main program goes into an infinite loop, the execution of which will occasionally be interrupted by the timer. The 'timer interrupt-service routine' is then executed and after the return-from-interrupt instruction, main program execution resumes from where it left off. An interrupt is caused by the timer when its data register is decremented to zero, providing both the interrupt (c.c.r.) and timer interrupt (t.c.r.) mask bits are clear. This can occur anywhere in the main program as the timings are not related, and when it does the c.p.u. completes the instruction in progress before servicing the interrupt. Because seven-segment codes used by the display are in no sensible way connected to the hexadecimal digit they display, a separate two-byte register giving in this case the b.c.d. equivalent value of the character in the display is used.

Main program

List 2 shows assembly language for the stopwatch program. This list was produced by a Motorola development system assembler. Before the start of the program proper, some of the labels used have to be defined as they are not defined in the program by appearing in the label field. The first three EQU instructions give the addresses of system calls used within the monitor program. Addresses within the 68705P3 memory map of port A data register and the timer control register (t.c.r.) and bit numbers within the t.c.r. of the interrupt mask and request bits are given. Remaining EQU instructions are r.a.m. registers.

The ORG statement tells the assembler the address of the program start. First the interrupt flag in the condition-code register is cleared to allow interrupts to take place. The timer prescaler is then set to divide the clock source from the internal-system clock by 32, the timer interrupt-request bit cleared, the prescaler cleared and the timer interrupt-mask bit set, all by storing 01000101 in the timer control resister.

Next the register TIMEV is set with the

List 2. Assembly language for the Picotutor stop watch program.

```
                                OPT     LLE=100
                          *
                          *----------------------------------------
                          *
                          *             S T P W A T C H
                          *
                          *       A STOPWATCH FOR THE PICOTUTOR
                          *
                          *----------------------------------------
                          *
                          * R F COATES     1 AUGUST 1983
                          *
                          * MONITOR CALLS
                          *
                0080    A CLRDIS EQU    $B0
                009E    A RSEG   EQU    $9E
                0083    A DISKEY EQU    $83
                          *
                0002    A PORTA  EQU    2          PORT A DATA REGISTER
                0009    A TCR    EQU    9          TIMER CONTROL REGISTER
                0010    A DISBUF EQU    $10        DISPLAY BUFFER RAM
                0016    A TIMEV  EQU    $16        ADDRESS REG. FOR TIMER SERVICE
                0019    A BCDEQU EQU    $19        BCD EQUIVALENT OF DISBUF
                001B    A TIC    EQU    $1B        10MS COUNTER
                          *
                          * INDIVIDUAL BIT NUMBERS IN 'TCR'
                          *
                0006    A TIM    EQU    6          TIMER INTERRUPT MASK
                0007    A TIR    EQU    7          TIMER INTERRUPT REQUEST
                          *
                          *
A 0020                          ORG     $20
                          *
A 0020 9A                 START CLI                ENABLE INTERRUPTS
A 0021 A6 45            A       LDA     #%01000101 SET TIMER FOR DIV. 32
A 0023 B7 09            A       STA     TCR        PRESCALER
A 0025 A6 49            A       LDA     #TIMINT    SET TIMER INT. JUMP
A 0027 B7 16            A       STA     TIMEV
A 0029 BD B0            A       JSR     CLRDIS     CLEAR DISPLAY
                          *
A 002B 4F                 ZERO  CLRA               SET BCDEQU TO ZERO
A 002C B7 19            A       STA     BCDEQU
A 002E B7 1A            A       STA     BCDEQU+1
A 0030 BD 9E            A       JSR     RSEG       CONVERT '0' TO 7 SEG.
A 0032 B7 10            A       STA     DISBUF     AND STORE IN DISPLAY
A 0034 B7 11            A       STA     DISBUF+1   BUFFER
                          *
A 0036 12 10            A LOOP  BSET    1,DISBUF   PUT D.P. ON IN LEFT DIGIT
A 0038 BD 83            A       JSR     DISKEY     REFRESH DISPLAY
                          *
A 003A 00 02 02 003F            BRSET   0,PORTA,TRYSTP BR IF START SWITCH OPEN
A 003D 1D 09            A       BCLR    TIM,TCR    CLEAR TIMER INT. MASK (START)
                          *
A 003F 02 02 02 0044 TRYSTP BRSET   1,PORTA,TRYZER BR IF STOP SWITCH OPEN
A 0042 1C 09            A       BSET    TIM,TCR    SET TIMER INT. MASK (STOP)
                          *
A 0044 04 02 EF 0036 TRYZER BRSET   2,PORTA,LOOP BR IF ZERO SWITCH OPEN
A 0047 20 E2    002B            BRA     ZERO       IF CLOSED, BRANCH AND ZERO
                          *
                          * TIMER INTERRUPT SERVICE ROUTINE
                          *
A 0049 1F 09            A TIMINT BCLR   TIR,TCR    CANCEL INTERRUPT
A 004B 3A 1B            A       DEC     TIC        DECREMENT 10MS COUNTER
A 004D 26 0C    005B            BNE     TIMOUT     BRANCH IF NOT DOWN TO ZERO
                          *
A 004F A6 0A            A       LDA     #10        RESET 10MS COUNTER FOR
A 0051 B7 1B            A       STA     TIC        10 COUNTS
A 0053 AE 01            A       LDX     #1
A 0055 99                       SEC                SET CARRY BIT
A 0056 AD 04    005C            BSR     ADDC       ADD C BIT TO LS DISPLAY
A 0058 5A                       DECX
A 0059 AD 01    '005C           BSR     ADDC       ADD ANY CARRY TO MS DIGIT
                          *
A 005B 80                 TIMOUT RTI
                          *
                          * ADDC - ADDS C BIT TO BCDEQU AND DISBUF
                          *
A 005C 4F                 ADDC  CLRA
A 005D E9 19            A       ADC     BCDEQU,X   ADD A (ZERO) PLUS C BIT
A 005F A1 0A            A       CMP     #$A        GONE PAST 9?
A 0061 98                       CLC
A 0062 26 02    0066            BNE     ADD1       BRANCH IF NOT
                          *
A 0064 4F                       CLRA               GONE PAST 9, SO RESET TO 0
A 0065 99                       SEC                AND PREPARE TO PASS ON CARRY
                          *
A 0066 E7 19            A ADD1  STA     BCDEQU,X   STORE RESULT BACK
A 0068 BD 9E            A       JSR     RSEG       CONVERT RESULT TO 7 SEG.
A 006A E7 10            A       STA     DISBUF,X   STORE IN DISPLAY BUFFER
A 006C 81                       RTS
                          *
                          *
                                END
TOTAL ERRORS 00000--00000
```

address of the timer interrupt-service routine, TIMINT, because when a timer interrupt occurs, the c.p.u. fetches the starting address of the service routine from the addresses 7F8/7F9. These addresses though are in eprom and cannot be changed by a user program. Instead, they are set with the address of the following small routine in the monitor, in which the first line loads the index register with the timer-interrupt vector.

```
77E   BE16  TIME LDX  TIMEV
780   FC         JMP  0.X
```

When a timer interrupt occurs this routine loads the index register with the contents of ram register TIMEV at address 016, then jumps (indexed) to that address. So to use the timer, the 8-bit direct address of the service routine is placed in TIMEV.

Next in the program, display is cleared and the b.c.d. equivalent store for the time to be displayed is set to zero. Seven-segment code to display a zero is then obtained by calling the system call RSEG which converts the right-hand (least significant) hexadecimal character in the accumulator seven-segment code. This is then stored in the two display positions used in DISBUF. Routine RSEG always turns the decimal point bit off, but in this application we need the decimal point on in the first digit. To do this, bit one in the first DISBUF byte is set and DISKEY is called, which as previously described will cause one refresh of the display from the contents of DISBUF.

Each of the three switches are checked in turn in the next section. The start switch is checked first by the instruction

```
BRSET O,PORTA,TRYSTP
```

The three operand arguments given to the BRSET instruction are 0 to indicate the bit number to be tested, PORTA which is the address of the byte in which bit 0 is to be tested and TRYSTP, the label to which execution must branch if port A bit 0 is set. If the port A bit 0 switch is open, the associated pull-up resistor causes the c.p.u. to read a one (set) and the branch will occur, but if the switch is closed the branch doesn't occur and the instruction BCLR TIM,TCR is executed. This clears the timer interrupt mask bit allowing interrupts to be serviced and the watch to start.

Stop and zero switches are then checked in the same manner. If the stop switch is closed, the timer interrupt mask bit is set again inhibiting the service of interrupts and stopping the clock. When the zero switch is open the program loops back to LOOP to refresh the display again, the loop repeating indefinitely to give the impression of a continuous display. If the zero switch is closed, the program branches back to the label ZERO which resets the time display to zero before continuing the loop.

Timer interrupt-service routine

Nothing in the main program affects the numbers in the display, except the zero function. Alterations to the data are made within the interrupt-service routine. No reference has been made so far to the timer data register, which as mentioned earlier can be programmed with a value from which it decrements to zero. In this example the t.d.r. is not programmed at all and is left to count the full 256 counts. When it reaches zero, an interrupt is generated but it also carries on decrementing to FF, then FE and so on.

It has been assumed that the clock frequency of Picotutor is 819.2kHz, but with an RC oscillator there will obviously be some tolerance to this and without a crystal oscillator the stopwatch may not be accurate. The timer has been programmed to be preceded by a divide-by-32 prescaler, which means that the t.d.r. will only be decremented every 32 clock cycles. This gives a total division of 256×32=8192. An 819.2kHz clock has a period of 1.22 microseconds, so the t.d.r. passes through zero and generates an interrupt every 1.22 ×8192μs or 10ms. As we need to increment the display every 100ms, the interrupt service routine counts up the interrupts and only increments the display every tenth interrupt.

When the timer generates an interrupt, it latches a request to the c.p.u. until such time as the c.p.u. can respond. The service routine must therefore cancel the request by clearing the timer interrupt request bit, otherwise as soon as the RTI instruction is executed, the service routine will be called again immediately. In the example this is done first and then the ram register 'tic' which counts the 10 interrupts is decremented. If this is not then zero, the service routine is terminated with no further action. If it is zero, 'tic' is reset to 10.

The display is then incremented as follows. A subroutine is used which adds the carry bit of the c.c.r. to a byte in BCDEQU and then converts this number into a seven-segment code, storing it in DISBUF. Which byte in BCDEQU and DISBUF is operated on is indicated by the offset in index register, which is first set to 01, the C bit set, and the subroutine ADDC called. To add just the C bit, the accumulator is cleared and the ADC instruction used which adds one to BCDEQU(+1). If the result is greater than nine, it is reset to zero and the C bit set, otherwise the C bit is cleared. The result is then stored in BCDEQU(+1) and after converting it into a seven-segment code, is stored in DISBUF(+1). On returning from ADDC, the index is decremented (00) and ADDC recalled. This time it adds any carry from BCDEQU(+1) to BCDEQU(+0) and DISBUF(+0); fortunately none of the intervening instructions affects the C bit. Hence the display will be incremented with the sequence 08, 09, 10, etc.

So what happens in the complete stopwatch software is that the main programme loops round, lighting up the display and checking the switches while being periodically interrupted providing the stop switch hasn't been operated for the display contents to be incremented.

Crystal operation

Clearly a stopwatch that isn't very accurate will not be particularly useful; in accurate timing applications, a crystal oscillator is required. The version of the 6805 in Picotutor gives a choice of two types of clock oscillator, RC or crystal. In non-critical applications, the RC oscillator is chosen because of the cost saving, but for an application such as a stopwatch a crystal should be used.

The two circuit configurations are shown in Fig. 5, but unfortunately more must be done than just changing the type of oscillator. The processor has to be told which type of oscillator is to be used by the programming of the mask-option register (m.o.r.). This is a byte in eprom, which in the P3-suffix version is at address 784. Six bits of the m.o.r. are used, five being for the timer prescaler to ensure compatibility with rom versions of the 6805. In Picotutor these are all zero which allows software programming of the prescaler as just described. Bit six is the clock-oscillator type bit and is bit seven of address 784.

A look at this address with the mo function on Picotutor will show that it contains 80. The one in bit seven indicates that an RC oscillator is being used, but if this is programmed as a zero, a crystal oscillator must be used. If the eprom is re-programmed a 3.2768MHz crystal could be used to give accurate timing from the stopwatch.

Picotutor may be modified as shown in Fig. 6 to accept a crystal. R_{17} should be removed from the board and replaced by a crystal, the hole spacing being correct for an HC18/U can. A 22pF capacitor is soldered to the underside of the board between pin 1 of IC_1 and the adjacent crystal pin. A wire link it taken from crystal pin to IC_1 pin 4, and the track between the crystal and R_{18} cut, as shown. For those of you without programming facilities a service will be offered later, giving a choice of oscillator type and some extra programmes in eprom as well as the monitor.

Bob Coates discusses microprocessor analogue interfacing in the next section and presents examples using Picotutor.

Timer-control register

b7	b6	b5	b4	b3	b2	b1	b0	
TIR	TIM	1	1	1	1	1	1	Timer control register 009

TCR with MOR TOPT = 1 (MC6805P2/P4 emulation)

b7	b6	b5	b4	b3	b2	b1	b0	
TIR	TIM	TIN	TIE	PSC*	PS_2	PS_1	PS_0	Timer control register 009

TCR with MOR TOPT = 0 (Software programmable timer)

* write only, reads as zero

TIN	TIE	Clock
0	0	Internal clock (Φ2)
0	1	Gated (AND) of external an internal clocks
1	0	No clock
1	1	External clock

PS_2	PS_1	PS_0	Prescaler division
0	0	0	1 (bypass prescaler)
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Configuration of the t.c.r. is determined by the logic level of bit 6 (timer option TOPT) in the mask-option register, m.o.r. Two configurations of the t.c.r. are shown, one with the timer-option bit at one and the second with it at zero. With this bit at zero, software control of the timer-control register is possible. When this bit is one, the timer-control register emulates two other versions of the 6805 known as MC6805P2 and MC6805P4. Under software control, i.e. with TOPT in the m.o.r. at zero, bits 0-2 in the t.c.r. (PS_{0-2}) set the prescaler as shown in the larger table. Bit 3 resets the prescaler when high. The external-timer pin is enabled when bit 4 is high and bit 5 selects an external clock when high or the internal clock when low. Bit 6 is the timer-interrupt mask bit which when high inhibits the timer interrupt to the processor and bit 7 indicates the timer interrupt when at logical one. Resetting does not affect bits 4 and 5. The smaller table explains operation of bits 4 and 5. Further details are given in the Motorola data sheet.
Prescaler should be cleared before changing prescaler bits 0-2 in software.

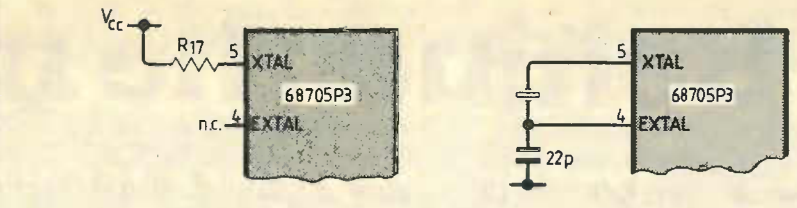


Fig. 5. Two timing elements that may be used with the 68705. Hardware modification is simple but the processor's eprom must also be altered slightly.

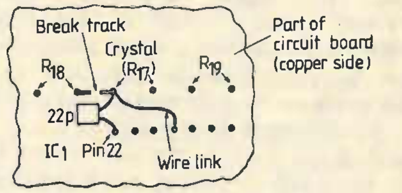


Fig. 6. Hardware modifications to Picotutor to allow more accurate timing using a crystal reference. Some reprogramming is necessary, see text.

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List 6. Array boundary checking using <BUILD . . . DOES>.

```
: ARRAY                                        ( low high . . assumes low <high )
  <BUILDS
  OVER – SWAP OVER                             ( delta low delta )
  SWAP , ,                                     ( store low is p.f.a., delta as p.f.a. +1 )
  DUP + ALLOT                                  ( that much storage, byte address machine )
  DOES>
  DUP ROT                                      ( . . p.f.a. p.f.a. index )
  SWAP @ – DUP 0<                              ( . . p.f.a. required-delta flag )
  IF ." array bound error, too low" QUIT THEN
  OVER 2+ @                                    ( . . p.f.a. reqd allowed )
  OVER <                                       ( . . p.f.a. reqd flag )
  IF ." array bound error, too high" QUIT THEN
  DUP +                                        ( word index to byte index )
  + 4 +                                        ( add index-skip parameters, leaving array
;                                                address )
```

Forth problems

So far, only advantages of Forth have been discussed but it has some disadvantages. The most obvious of these is notation. For the beginner, reverse-Polish notation and the lack of an assignment operator (:=) are considerable problems. Practice lessens the problems though program comments and stack diagrams generally remain necessary to show what is going on.

Floating-point arithmetic is not standard and all data manipulation assumes 16-bit two's-complement arithmetic, but it may be programmed in[15]. This shows Forth's origin in the control field of computing. However, many Forth programmers maintain that most problems can be reduced to scaled-integer arithmetic. This drawback makes one aware of the processing cost of floating-point arithmetic. Forth does not use 'data typing'. This means that integer operations are used when logical operations are being performed ('0=' for NOT). There are also separate operators for 32-bit arithmetic. Computer languages can usually apply different operations for the same operator by data typing.

A more serious drawback is the lack of built-in data structures – not that Forth is any worse in this respect than Basic or Fortran. What is lacking are the type of data structures available in Pascal. In common with the formerly mentioned languages, Forth lacks a method of checking for overflow and array boundary conditions in normal operation. But as shown in List 6. This can be programmed in. Naturally, this process increased execution time but when the application works a simpler version of array can be coded by missing out the check. Finally there is as yet no file management software. Access to disc information has to be done using BLOCK numbers.

Summary

I have shown that the programmer is released from the instruction set of the host computer with little time penalty by applying threaded code. Using the compiler, one may easily extend the Forth instruction set to suit one's own application. As the whole dictionary is available all of the time (ranging from virtual-machine instructions to <BUILDS . . . DOES> structures) the programmer can tackle low or high-level problems, such as i/o driving or word processing, with equal ease and efficiency. The consistent nature of the compiler and text interpreter allow easy interactive testing of code before it is compiled. Reverse-Polish notation simplifies the compilation process and allows it to be completed in one pass in a small memory. Virtual memory and vocabularies further enhance Forth by offering infinite data space and better control of the application software respectively. However, shortcomings of the language may prevent it from being applied to larger computers where its space-saving features are less useful. But it will continue to find many applications in small and interactive systems and real-time applications including hardware simulation, video games and test-equipment control.

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8. M. McNeil, A hashed dictionary search method, FORML '81 papers, FIG.
9. T. Dowling, Hash encoded Forth Fields, FORM '81 papers, FIG.
10. K. Schleisiek, Separated heads, *Forth Dimensions*, vol. 12, no 5, pp. 147-150, FIG.
11. D. Petty, Utilizing vocabularies, FORML '81 papers, FIG.
12. J. Cassady, Towards a 79-Standard Fig-Forth Romable Vocabulary and Smart FORGET, FORML '81 papers, FIG.
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14. J. Gilbreath, A. high-level Benchmark, *Byte*, Sep. 1981, pp.180-196 (for algorithm and performance data see *Byte*, Jan. 1983).
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Behind the micro

Putting the microcomputer to work: a guide to computers for laboratory or workshop

Choosing a microcomputer – rather than letting one be chosen for you – is a difficult task for those who want to experiment, write programs and interface and control their own circuits. There is information enough for people who want to buy a microcomputer for office use or to play games on. But there are many potential users between these groups who want a microcomputer which they can develop to suit needs not catered for by off the shelf hardware or software. Among these people are engineers, technicians, designers, teachers and home-computer users. Our survey concentrates on the needs of potential microcomputer users in these areas, in particular on interfacing.

For a journal such as ours there are different ways of approaching a microcomputer survey, the two extremes being to talk about four or five computers in depth or to give very brief details about as many as possible. The first method is the easy way out but it is unlikely that one will find the computer best suited to one's needs from the four or five discussed. The second approach is more helpful in that it allows one to compile a list of computers that potentially suit one's needs.

Here we present a table to allow you to compile a short-list, and give further information about the computers mentioned to supplement it. We have biased supplementary information towards that relevant to the technically-minded computer buyer.

A supplementary article appearing in next month's issue provides further information for potential microcomputer buyers and a list of addresses and telephone numbers of manufacturers mentioned here. Popular interfaces are discussed as are a few computer boards to give you an idea of what computers without cases are for, and their advantages and disadvantages.

About the computers

ABS *ORB:* series of computers offering multi-user capability. Recently introduced, intended for business and scientific applications. **WW501**

Acorn *BBC Microcomputer:* Paged rom feature permits up to 16 resident languages, utilities, applications programs. Two parallel ports, i/o port, RS423, four-channel analogue input. Second processors on the way: Z80 (for CP/M), 16032 (for UNIX) and 6502. Optional rom cartridge port, speech synthesiser, networking, Viewdata and teletext/telesoftware adaptors. Easy mixing of Basic and assembly language; other languages include Forth, Lisp, BCPL, S-Pascal. Widely used in schools and colleges. *Electron:* stripped-down version of BBC micro using the same BBC Basic. Upgrades promised. **WW502**

ACT International *Sirius 1:* for technical applications, scientific word-processing, computer-aided design and manufacturing. Interfacing to existing computers. Optional d.m.a. board for expansion port. *Apricot:* aimed mainly at the businessman, but with many features of wider interest. **WW503**

Action Instruments *PAC* personal automation controller: ten-slot expansion bus for maker's range of analogue and digital i/o boards. Extensive interfacing possibilities. **WW504**

Advance *86a:* 'compatible' with IBM personal computer. Separate keyboard stows in base unit for portability. Upgradable to *86b*, which has two disc drives. **WW505**

Alpha Micro *AM1000:* business computer with i/o expansion module option: video-recorder interface allows fast serial data transfer. Other models available. **WW506**

Apple *IIe:* numerous interface cards to fit internally. Boasts largest selection of software for any computer. CP/M option. *III:* for more complex applications: hard-disc data storage option. *Lisa:* mainly for business. 'Mouse' for easy control by the computer-illiterate. Non-standard monitor gives very high resolution graphics. Software for calculation, graphs etc. built in. **WW507**

Aston Technology *Crystal 68000* range: bigger machines are multi-user Winchester-based. R series for RS232 communications, C series for networking through high-speed coax links. PICK operating system said to be easy for first-time users. Fortran, C, Pascal, Cobol, APL. Can support CP/M indirectly. **WW508**

Atari: range is aimed largely at home games players, but there is much software for more serious purposes. Shop around for the best price. *600XL* has 256 colours, four-voice sound, cartridge slot, 16K ram expandable by 64K. Data storage is on special cassette machines (not included) or disc. Add-ons include joysticks and tracker ball. **WW509**

Bleasdale *BDC680A:* d.m.a. controller as standard, internal IEEE-796 multibus with six slots free, ten RS232 ports. Options include 10MHz processor, multi-user capability, tape back-up. Intriguingly named 'MISTRESS relational database management system'. Maker supplies interesting UNIX benchmark comparisons. **WW510**

BMC International *if 800:* versatile machine with many options. Built-in graphics printer. Three open bus slots. **WW511**

British Micro *Mimi 803:* modular design, 50-pin bus connector, internal Winchester connector. CP/M-compatible operating system. Allows conversion of Superbrain-format discs to Mimi format. High-res. graphics option. **WW512**

Bromcom *SuperStar 10:* S100 bus, CP/M (2.2 version for Z80 or 86 for 8086 processor). No keyboard provided. Options include MS-DOS, integral Winchester storage, multi-user capability (with up to 16 processors). **WW513**

Camputers *Lynx:* range also includes 96K version. Promised 128K machine will run CP/M and work as a main-frame terminal. Built-in machine code monitor. Cartridges coming for Pascal, Forth, Logo and Comal. Handbook gives detailed port connections. User magazine published by manufacturer. **WW514**

Ceedata *8200:* offers CP/M 2.2 with additional utilities. Compatible with Superbrain single-sided discs. 192K 'silicon disc' option. On-board i/o expansion facilities. Boasts 'low-maintenance' p.c.b. **WW515**

Computer Games Ltd *CGL M5:* joystick port, cartridge port, 56-way expansion bus. Character set includes Greek symbols. Also available as Sord M5. **WW516**

Comart *Communicator* range: numerous Z80, 8086 models, good choice of operating systems. Keyboard not included. Modular design, multi-processor options. **WW517**

Commodore: range includes scientific, business and home computers. Good software availability. *VIC-20:* primarily a games computer, but IEEE interface available. *64:* second processor, networking, Viewdata options, educational software. *500:* for scientific applications. Up to 86K ram. Optional CP/M, MS-DOS using second processor. **WW518**

continued on page 65

Table guide

Where a manufacturer produces a range of models we have taken a basic version. Filled blobs in the table indicate that a feature is provided, open blobs or parentheses that it is optional. A fuller description of the table will follow next month.

C/WP *Cortex:* not to be confused with Powertran's machine. Interrupt-driven RS232 interface, though essentially an office machine. Selected as standard computer by the City University. BBC Basic available. Second processor (6502) has 48K ram, 8K rom for graphics display ('treats the screen as if it were 192,000 electric light bulbs'). **WW519**

Datac *MC* system: for education and laboratory use. A special Basic interpreter handles real-time interrupts and nested scheduling. Various optional analogue and digital i/o boards (£19-£79) may be connected via an experimental unit (£125). **WW520**

Digital (DEC): large range of personal computers and word-processors. *Rainbow 100:* three expansion slots for options, runs CP/M-86,80. *Professional 325:* 'a PDP-11 on your desk'. Winchester storage. *Professional 350:* similar, but with four option slots. **WW521**

Dragon Data *Dragon 32:* cartridge and expansion ports. Extra languages include Pascal and Cobol. Some resemblance to expanded version of Tandy TRS-80 Colour Computer. *Dragon 64* at £196 has 64K ram and a built-in RS232 port. **WW522**

DVW Microelectronics *Husky:* NiCd-powered portable machine for use in flammable atmospheres. A-to-d option and parallel port for data gathering can be built in. Extended Basic, up to 144K memory. Range of communications interfaces including IBM 2870 compatibility. **WW523**

EACA *Colour Genie:* two parallel ports, light-pen port, processor signals available at cartridge port. Assembler included. **WW524**

Elan *Enterprise:* promised for April 1984. Standard features include two cassette ports, cartridge port, RS423, 256 colours, stereo sound, built-in joystick, 64-way interface connector, network interface for up to 32 computers. Memory expandable to 3.9MB. Built-in word-processor. Forth and Lisp to come. **WW525**

Epson *QX10:* 60-way bus with five expansion slots; light-pen port; memory expandable to four switchable banks of 64K, with 2K of battery-backed ram; upgradable to colour. **WW526**

Future *FX20:* 'IBM-PC compatible'. IBM bus option. On-board diagnostic software

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			Processor			Languages			O.S.		Display							Printer			Storage			Interface							
Maker	Model	Basic price (£) excluding v.a.t.	Type	Bits	Speed	Included	Rom size	Others	Type/size	Rom/disc	V.d.u (integral)	Video out	R.G.B.	R.f. modulator	Other display	Chars (max)	Pixels	Built-in	Centronics	Other interface	Ram (K)	Disc(s)	Cassette	Communications	Processor access	Serial	IEEE-488	S100	Other parallel	Analogue	Real-time clock
ABS	Orb	5950	8086-2	16					MP/M86	r/d	M					80×25			●		256	●				●					
Acorn	BBC	347	6502	8	2	B	16	○	16K	r		●	●	●		80×25	640×256		●		32	○	○	○	●	●			●	●	
	Electron	173	6502	8	2	B	32		with Basic	r			●	●		80×25	640×256		○		32	○	○	○					○	○	
ACT	Apricot	~1495	8086+8087	16	5	B		●	various	d	M				lcd	132×50	800×400		●		256	●		○		●					
	Sirius	2195	8088	16		B		●	various	d	M					132×50	800×400		●		128	●		○		●	●				
Action Instruments	PAC		Z80A	8	4	B	16	○	ABLE ≤24K	r		●				80×24	160×80		●		2		○			●	○	○	●	●	●
Advance	86a	348	8086 (+8087)	16	~5	B			40K	r		●	●	●		40×25	640×200		●		128	○	○							●	
Alpha Micro	AM1000		68000	16		(B)			CP/M etc	d		●							●		128	○				●					●
Apple	IIe	845	6502A	8		B		○	various	r/d		●	○			40×24	280×192			○	64	○	○		●	○			○		
	III	2395	6502B	8		B		○	SOS, DOS	r/d		●	●			80×24	560×192			●	256	○			●	●			○		
	Lisa	6500	68000	16		B		○	DOS	r/d	M	●				144×45	720×364			●	1M	●	○	○	●	●			●		●
Aston Technology	Crystal	4395	68000	16	10	B			various	d	C/M					132×25				●		●				●					
Atari	600XL	139	6502C	8	1.8	B	24	○	DOS III	d		●		●		40×24	320×192			●	16	○	○		●	●					
Bleasdale	BDC 680A	8509	68000	16	8				UNIX,C	d											256	●			●	●			○		
BMC International	if 800	1700	Z80A	8	4						C/M	●				80×25	640×200	●	○		64	●	○	○	●	●	○		●	○	●
British Micro	MIMI 803	1495	Z80A	8	4				CP/M-type	r/d	M	●				80×25			●		64	●			●	●					
Bromcom	Superstar 10	1750	Z80A/8086	8/16					CP/M(86)	d									●	●	64	●				●					
Camputers	Lynx Level 1	196	Z80A	8	4	B	16		with Basic	r		●	●	●		40×24	248×256		○	○	48	○	○						●	○	
	Lynx Level 3	387	Z80A	8	4	B	20		(CP/M)	r/d		●	●	●		80×24	248×512		○	○	128	○	○			●			●	○	
Caedata	8200	1735	Z80A	8	4				CP/M	d	M	●				80×24			●		64	●				●			●		
CGL	M5	165	Z80A	8	~4	B	8K		8K	r		●		●		40×24	256×192		●		20	○	○		●						
Comart	CP100A	1895	Z80A	8	4				CP/M	d											64	●				●		●			
	CP1202	2745	8086	16	6				CP/M etc	d											256	●				●		●			
Commodore	VIC-20	121	6502	8	1	B			with Basic	r				●		22×23	176×158			●	5	○	○	○		●	○		●		
	64	173	6510	8		B	20		with Basic	r		●		●		40×25	320×200				64	○	○	○		●	○		●		

Maker	Model	Basic price (£) excluding v.a.t.	Processor: Type	Processor: Bits	Processor: Speed	Languages: Included	Languages: Rom size	Languages: Others	O.S.: Type/size	O.S.: Rom/disc	Display: V.d.u (integral)	Display: video out	Display: R.G.B.	Display: R.f. modulator	Display: Other display	Display: Chars (max)	Display: Pixels	Printer: Built-in	Printer: Centronics	Printer: Other interface	Storage: Ram (K)	Storage: Disc(s)	Storage: Cassette	Interface: Communications	Interface: Processor access	Interface: Serial	Interface: IEEE-488	Interface: S100	Interface: Other parallel	Interface: Analogue	Interface: Real-time clock
	500	800	6509(8088)	8	1	B	28		28K	r		●	●	●		40×25	320×200			●	128	○	○			●	●		●		
C/WP	Cortex	1695	Z80A+6502	8	4				CP/M	r/d	M					80×25	640×308		●		64	○			●	●					
Datac	MC	439	Z80	8	2	B	8		8K(inc mon)	r		●		●		40×24					16		○		●	●			○	○	
Digital (DEC)	Rainbow 100		Z80/8088		8/16	(B)		○	CP/M,MSDOS	d	M	●				132×24	800×240			EIA	128	●				●			●		
	Professional 300		F11 (Z80)			B		○	P/OS	d	M	●				132×24	960×240			●	512	●				●			●		●
Dragon	Dragon 32	152	6809	8	1	B	16		with Basic	r		●	○	●		32×16	256×192		●		32	○	○		●					●	
DVW Microelectronics	Husky	1784	NS800	2		B	32								lcd	32×4				●	32					●					●
EACA	Colour Genie	146	Z80A	2		B	16		with Basic	r		●		●		40×24	320×192				32	○	○	○	●	●			●		
Elan	Enterprise	200	Z80A	8	4	B	32		with Basic	r		●	●	●		84×56	672×512		●		64	○	○		●	●			●		
Epson	QX-10	1735	Z80-type	8	4				CP/M	d	M					80×25	640×400		●		192	●		○	●	●					●
Future	FX20		8088	16						d	M					80×25				●	128	●				●			●		
Haywood	9000	1795	Z80A	8	4				CP/M	r/d	M					80×25					64	●				●					
Hewlett-Packard	HP-75C	762	c.m.o.s	8		B	48		with Basic	r		○		○	lcd	32×1				○	16		○			○	○		○		●
	HP-85B	2257				B	>48		with Basic	r	M					32×16	256×192	●			120		●			○	○		○		●
	HP-86B	1194				B	>56		with Basic	r		●				80×24	544×240			○	128	○				●	●				
	HP-150	2900	8088	16	8				MSDOS		M					80×27					256	○		●		●	●				
	HP-200,16	3770	68000	16	8	B		●			M		○			80×25	400×300			●	128	●	○		○	●	●		○		●
HH Microcomputers	Tiger	2795	Z80/6809	8					CP/M etc	r/d	C	○	●	○		80×24	512×512		●	●	64	●	○	●	●	●	●				
Hotel Microsystems	Minstrel	3185	Z80A	8	4				CP/M, TurboDOS	d	C										64	●				●		●	●		
Hytek	Model 20	3450	Z80B	8	6				CP/M+32K	r/d	M					80×25					192	●				●					○
IBM	PC	2678	8088	16	4.8	B	32	○	various	r/d	M	●	○			80×25	720×350	●	●	○	64	●		●	●	●	○	○	●	○	
ICL	PC15	1795	8085AH2	8	5				various	r/d	M		○								64	●				●					
Immediate Bus. Systems	Fieldwork 50		Z80L	8		B	8		with Basic	r					lcd	40×2					32K					●					●
Integrated Micro Prods.	IMP-68		68000	16	8			●	various	r/d											256	●				●		●			●
ITCS	Alfa D3	1995	Z80A	8			16		CP/M	r/d	M								●		64	●				●	●		●		
	Zita-E4	2395	Z80A	8	4				CP/M	r/d	M						160×72		●		128	●				●			●		●
Iotec	64CD	1650	Z80A	8					DOS	d		●	●			80×25					64	●	○	○	●				●		
Jarogate	MP5		Z80/8086	8					CP/NOS etc		○	○	○				754×482			○	64	●	○	○	●			●		○	
Jupiter Cantab	Ace	78	Z80	8	~3	F	8			r				●		32×24	64×48				3		○						●		
Kemitron	KS200E		Z80A	8	4				CP/M		M								●		64	●			●	●	○		●	○	○
LSI	Octopus	1530	Z80B/8088	8/16	6/8		<32		various	r/d	M	●	●	●		132×29	720×325		●	●	128	●		○	●	●			●		●
Leenshire	VCT6910		6809	8			<48				C	○				132×27	512×512			○	16			●	●	●			○	○	●
Logica VTS	Vitesse	2490	8086	16	5	B		○	various	r/d	C	●				80×24			●	○	64	○				●					
Mattel	Aquarius	44	Z80A	8	4	B	8		with Basic	r				●		40×24	320×192			○	4		○			●			●		
Memotech	MTX500	239	Z80A	8	4	B	24	○	with Basic	r		●		●		40×24	256×192		●	○	32	○	○	○	●	○			●		●
Micronix	MX400	799	Z80A	8	4				CP/M		[illegible]	●				80×24					64	●		○	●	●			●		●
Modcomp Inc.	Zorba 2000	~1400	Z80A	8	4	B			various	d	M	●				80×25			●	●	64	●		●		●	●		●		
Modus	Tensor		Z80A	8	4		<32		CP/M-type		M					80×24					64	○				●		●	●	○	●
Motorola	EXORset 100		6809	8		B			X-DOS	r/d	M								●		56	●				●					
	VME/10		68010	16					various	r/d	M		●							●	384	●			●	○	○			○	
Multitech	MPF-1 Plus	140	Z80A	8		(B)		○	8K	r			●		fluor	20×1					4		○		●				○		
NEC	APC	1875	8086(8087)	16	5				various	r/d	M					80×25	640×475		●		128	●		○		●			○		●

Maker	Model	Processor: Basic price (£) excluding v.a.t.	Type	Bits	Speed	Languages: Included	Rom size	Others	O.S.: Type/size	Rom/disc
Newbrain	Newbrain	~200	Z80	8	4	B	29		with Basic	d
Oric	ORIC-1	87	6502	8		B	16		with Basic	r
Osborne	Executive	1995	Z80A	8	4	B	8	●	various	r/d
Philips	P3500	>3000	Z80	8	4	B	8		TurboDOS	d
Phoenix	Stratos	~2000	Z80	8					CP/M	d
Plessey	PC-16		8086(+8087)	16	8	B	8	●	MS-DOS	r/d
Portico	Miracle	1795	Z80A	8			4		CP/M	
Positron	900	1095	6809			B	<128		OS-9	r
	9000	1536	6809	8		B	36	○	OS-9	r
Powertran	Cortex kit	344	TMS9995	16		B	24	○	MDEX	r
Rediffusion	Teleputer 3	3595	Z80	8		B			CP/*,CP/M	d
Research Machines	Link 480Z	685	Z80	8	4	B	32	○	CP/M	r
Rockwell	AIM 65/500	530	6502	8		(B)	12	○		r
	AIM 65/40	375	6502	8		(B)	(8)	○		r
Seed	19/64DS5	1304	6809	8	2	B			OS-9	r/d
SBC	Duet 16		8086(+8087)	16	8	B	8	○	MS-DOS	d
Semi-Tech	Pied Piper	1066	Z80A	8			4		CP/M	d
Sharp	MZ700	217	Z80					○		
	MZ80B	900	Z80	8	4	B		○	FDOS	d
Sinclair Research	ZX81	35	Z80A	8	~3	B	8	○	with Basic	r
	ZX Spectrum	87	Z80A	8	~3	B	16	○	with Basic	r
Sirton	Midas MPS		Z80A	8	4		1		CP/M-type	r/d
Sord	M223/III	2800	Z80A	8	4			○	Pips	
Stirling	Dennis kit	~430	6809	8	1				FLEX	r/d
SWTP	F/09		6809						FLEX	
	S/09		6809						UniFLEX	
Systime	S301	~3000	8086	16	5				various	d
Tandy TRS-80	MC10	87	6803	8		B				
	Model 100	434	80C85	8	2.4	B	32		with Basic	r
	Colour computer	209	6809	8	0.9	B	8	○	with Basic	r
	Model 4	1304	Z80A	8	4	B	14	○	various	d
	Model 12	2086	Z80A	8	4	B		○	various	d
	Model 16	3303	Z80A,68000	16	6	B		○	various	d
Tashki	OM8064	1080	Z80, 6502	8		B	<14		CP/M	d
Televideo	TS1603	2395	8088	16					CP/M-86,MS-DOS	d
Texas Instruments	TI99/4A	79	9900	16		B	26	○	with Basic	r
Triumph Adler	Alphatronic PC	350	Z80	8	4	B	32	○	with Basic	r
	Alphatronic P30		8085A/8088	8/16		B	4	○	various	
Transam	Tuscan	~1700	Z80	8	4		4		CP/M	r/d
Tycom	Microframe		various						various	r/d
Videcom	Apollo		2×Z80A	8					CP/M	
Wessex	Wyvern	290	6809	8	1	B	16		with Basic	r
Windrush	6809X	875	6809	8	2				FLEX	d
Zenith	ZF-100-21	2070	8085/8088	8/16					various	d

Maker	Model	Display: V.d.u (integral)	Video out	R.G.B.	R.f. modulator	Other display	Chars (max)	Pixels	Printer: Built-in	Centronics	Other interface	Storage: Ram (K)	Disc(s)	Cassette	Interface: Communications	Processor access	Serial	IEEE-488	S100	Other parallel	Analogue	Real-time clock
Newbrain	Newbrain		●		●		80×40	640×250			●	32	○	○	○		●			●		
Oric	ORIC-1			●	●		40×28	240×200		●		16	○	○	○	●						
Osborne	Executive	M	●				80×24			●	●	128	●		●		●	●		●		●
Philips	P3500	M					80×25			○	●	64	●		○	●	●					
Phoenix	Stratos	M								●	●		●									
Plessey	PC-16	M/C					80×25	640×400		●		>96	●				●					●
Portico	Miracle	M					80×25			●		128	●		○		●					
Positron	900											64	○				●	●				
	9000		●	●	●		40×24	240×240			●	64	○	○	○	●	●	●				
Powertran	Cortex kit		●	●	●		40×24	256×192				64	○	○			○				●	●
Rediffusion	Teleputer 3	C					80×24					128	●		●		●					●
Research Machines	Link 480Z		●	○	●		80×25	640×192		●		64	○	○			●	●				
Rockwell	AIM 65/500		○		○	led	20×1		●			4	○	○	○	●	●			●	○	
	AIM 65/40					fluor	40×1		●	●		16	○	●	○	●	●	○		●	○	
Seed	19/64DS5									●		56	●				●			●	○	
SBC	Duet 16	M/C					80×25	640×400		●		96	●				●	○		●		●
Semi-Tech	Pied Piper		●		○		80×24			●		64	●		○		○			●		
Sharp	MZ700		●	●	●				○			64		○						●		
	MZ80B	M					80×25	520×200			●	64	○	●			○			●		
Sinclair Research	ZX81				●		32×24	64×48			●	1		○		●				●		
	ZX Spectrum				●		32×16	256×192			●	16		○		●				●		
Sirton	Midas MPS									●		64	●				●		●	●		
Sord	M223/III	M		●	○						●	64	●		●		●	●	○	●	○	○
Stirling	Dennis kit		●	○			40×24	512×512		○	○	<64	○	○		●	●			●	○	
SWTP	F/09									●		64	●				●			●		
	S/09									●		64	●				●			●		
Systime	S301	M										256	●		○		●					●
Tandy TRS-80	MC10				●		32×16				●	4		○			●					
	Model 100					Tcd	40×8	240×64		●		8		○	●		●					●
	Colour computer				●		32×16	256×192		●		16	○	○			●				●	
	Model 4	M					80×24			●		64	●	○			●			●		
	Model 12	M					80×24			●		80	●				●			●		
	Model 16	M					80×24			●		128	●				●			●		
Tashki	OM8064	M			●		80×24			●		64	●	○								
Televideo	TS1603									●		128	●				●					
Texas Instruments	TI99/4A				●		32×24	256×192			●	16	○	○		●	○			●		
Triumph Adler	Alphatronic PC			●	●		80×24			●		64	○	○			●			●		
	Alphatronic P30											64	●									
Transam	Tuscan	M					80×24			●		64	●	○			●		●	●		
Tycom	Microframe	M/C	●	●			80×24	1024×400		●		<576	○			●	○					●
Videcom	Apollo	M					80×26				●	64	●				●					
Wessex	Wyvern		●	●	●					●		32	○	○		●	○	○		●	●	○
Windrush	6809X	M					80×24	512×480				56	●			●	●	○		●		●
Zenith	ZF-100-21		●	○			80×25			●		128	●				●		●			

for hardware monitoring. Ram parity checking. Local-area networking facility as standard. Ethernet gateway, multi-user, communications options. Range includes seven other models; upgrade kits available. **WW527**

Haywood *9000:* CP/M computer. Serial output is prom-programmable in five modes for special applications. **WW528**

Hewlett-Packard: large range of machines for a variety of purposes, widely used in research and development. High performance, high price. *HP-75C:* battery-powered portable. Accepts three 16K plug-in roms, up to 24K ram. Built-in clock, reader for 1300-byte magnetic cards. Mini-cassette interface. *HP-85B:* maximum rom 96K, total memory storage 640K (120K fitted). Non-standard tape cartridge with search feature. Optional b.c.d., serial current-loop, general purpose i/o interfaces. Five-inch c.r.t. *HP-86B:* real-time clock plus three timers (0.5ms to 1.16 days). Maximum rom 104K, total addressable memory 712K. *HP-150:* 896 display characters including special mathematical symbols, touch screen. *HP Series 200, Model 16* personal technical computer: real-time clock and timers, various built-in or add-on interfaces, Basic and Pascal. **WW529**

HH Microcomputers *Tiger:* triple processor design – second for i/o with 16K rom, 2K ram and third for graphics with 96K separate display memory. 50-pin Z80 bus expansion connector. Network data link. Prestel modem complete with jack plug built in. **WW530**

Hotel Microsystems *Minstrel:* various configurations possible from Z80A CP/M system up to 68000-based model, including 8086 range. Ten S-100 bus slots. **WW531**

Hytek *Prelude 20:* CP/M computer can be upgraded to hard disc. Network interface processor option. MS-DOS promised. Other models available. **WW532**

IBM *Personal Computer:* colour and hard-disc options available. Standard o.s. is MS-DOS but CP/M86, UCSD-p available and Unix 'being looked into'. Five expansion slots are available internally. Printer and some software included in price. **WW533**

ICL *Personal Computer:* two models with CP/M and Basic, two with MP/M and Basic. Hard disc except on Model 15. Design will accommodate 8088 16-bit processor. ICL/IBM communications, much software. Maximum memory 512K; four channel d.m.a. Four serial ports standard, eight optional. **WW534**

Immediate Business Systems *Fieldwork 50:* battery-powered portable, suitable for harsh environments. Bubble memory option. **WW535**

Integrated Micro Products *IMP-68:* multi-user operating system, C compiler, Pascal compiler, utilities to read and write CP/M, RT-11 and UNIX discs. Up to 1MB ram with parity-checking; S100 i/o and on-board i/o can be mapped to any 64K block; d.m.a. Maximum of ten serial ports. Cartridge tape back-up available. Requires keyboard. **WW536**

ITCS: range of five machines including three transportables (with c.r.t. and disc drives). *Andromeda Alfa-D3:* parity checking in memory (expandable to 128K), d.m.a. Expansion bus slots. Takes up to four RS232, four IEEE-488 and four Centronics ports. *Andromeda Zita-E4* portable: teletext character set, CP/M. Optional RS422 network interface and modem, colour graphics terminal, Winchester disc. **WW537**

Iotec *64CD:* full Z80 bus on 50-way connector plus additional select signals for use with rom/ram expansion and memory management. 64 colour shades. Supports Teletext graphics. Wide range of other machines available. **WW538**

Jarogate *MP5* multi-processor system, mixed 8/16-bit. One S100 bus per processor. Multi-user, up to 16 printers. Numerous options include interfaces, tape back-up, slave processors, hi-res. colour graphics, Ethernet, Viewdata, telex, mainframe links. Requires keyboard. **WW539**

Jupiter *Ace:* the only home microcomputer to have Forth as its standard language. Reverse polish notation. Expandable to 51K ram. Relatively little software. The manufacturer called in a receiver at the beginning of November, but machines may still be on sale. **WW540**

Kemitron *K2000E* technical microcomputer for industrial and scientific uses: many measurement and control interfaces available, including 12-bit analogues, six-channel RS232 boards. Keyboard required. *KM3000* is similar, but with 8in discs instead of mini-floppies. Two programmable RS232 ports as standard. Programmable four-channel counter-timer. **WW541**

LSI *Octopus:* business computer with wider applications. Up to 32K eprom, two RS232 ports, disc interface with d.m.a., quick-connect expansion boards. Options include 8087 maths co-processor, graphics board, four more RS232 ports, one RS422, modem board, networking, bus expansion, Winchester disc interface with d.m.a. **WW542**

Leenshire *VCT6910:* two RS232 ports, four parallel ports, up to 48K eprom. User-programmable screen formats; 64 foreground, 64 background colours. One of a range of colour terminals. **WW543**

Logica VTS *Vitesse* personal computer: CP/M-86, MS-DOS, BOS. Languages available include Pascal, Fortran and Cobol. 64K ram is expandable to 512K and shortly to 1MB. Removable Winchester cartridge back-up and colour graphics card also promised. **WW544**

Mattel *Aquarius:* cartridge port. Mainly for games. No editing facilities. 4K ram expansion and printer available. Soon to be marketed directly by its makers, Radofin. **WW545**

Memotech *MTX* series: ram expandable to 512K; up to two expansions (ram or communications) can be fitted internally; joystick and cartridge ports; separate numeric pad on keyboard; node/ring networking possible; assembler/disassembler included, Forth and Pascal available as rom extensions. Two RS232 ports on optional communications board. Floppy disc and hard disc expansions use CP/M 2.2 o.s. Also *MTX512* with 64K ram at £274. **WW546**

Micronix *MX* range: CP/M system, ram expandable to 128K. Two RS232 ports, two parallel; buffered bus. Hard-disc subsystem available. Keyboard required. Four models; single-board available separately. **WW547**

Modcomp *Zorba 2000* series: transportables with 9-inch screen. Can read and write a variety of disc formats. *Model 16* has 8- and 16-bit processors. **WW548**

Modus range of industrial computers. *Tensor:* many control and data acquisition interface boards available. Networking possible. **WW549**

Motorola *VME/10:* designed for scientific and engineering uses, software development. Various configurations possible. VME bus with additional i/o channel to serve peripherals. *EXOR*set **100:** for software development. **WW550**

Multitech *Microprofessor MPF1 Plus:* single-board microcomputer with built-in keyboard and fluorescent display. Full processor bus and 48 i/o lines. Optional Basic and Forth (8K each). Expansions include i/o board, sound and speech synthesiser boards, mini-printer. **WW551**

NEC *APC* (Advanced personal computer): colour or monochrome with high resolution graphics; 8in disc drives; second RS232 available; optional communications facilities. Range also includes some 8-bit models, including the *PC-8201*(£475), a portable similar to the Tandy 100 but with 16K ram. **WW552**

Newbrain: was almost adopted as the BBC microcomputer. Two serial ports, one parallel; two cassette interfaces; optional built-in fluorescent display. Full screen editing. Following the recent demise of Grundy Business Systems, the Dutch distributor Tradecom has taken responsibility for the Newbrain and it will now be distributed in the U.K. by Brainwave Software. **WW553**

Oric *Oric-1:* moving keys, eight-octave sound generator, teletext display mode; add-ons include colour plotter, 3in disc drives, communications modem. Forth available. Also a 48K model. Cassette interface operates at "super reliable 300 baud or reliable super fast 2400 baud"! **WW554**

Osborne *Executive:* portable with 7 inch screen, can read/write numerous other disc formats. Also Osborne 01 at £1495. U.S. parent went into bankruptcy in October, but stocks are still available from Osborne (UK). **WW555**

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Philips *P3500:* mainly for the office, but software is available for manufacturing control etc. Launched as an 8-bit multi-user, multi processor system but 16 bit upgrades are to follow. **WW556**

Phoenix *Stratos* CP/M business computer with 8in disc drives. D.m.a. **WW557**

Plessey *System 19, PC-16:* networking personal computer. User ram expandable to 512K; two RS232 ports; d.m.a.; optional colour display, hard discs. The company also offers a range of fast minicomputers for real-time control applications. **WW558**

Powertran *Cortex* kit: also available ready-built (no relation to C/WP Cortex). Powerful Basic for scientific and other applications: 48-bit floating-point arithmetic, 11-digit accuracy. Separate 16K screen memory. Machine-code monitor, assembler, disassembler all included. Buffered printer port. Supports up to 16 output devices. **WW559**

Portico *Miracle:* CP/M portable with 10in screen and two disc drives. D.m.a. Five expansion slots, two RS232 ports plus optional RS422; optional hard disc interface. **WW560**

Positron *900:* boxed single-board computer; memory expansion up to 256K. Also in single-board form. *9000* series: for science, education, engineering as well as business. Can execute multiple concurrent tasks. Fully buffered address, data and control bus. **WW561**

Rediffusion *Teleputer 3:* business machine with modem and autodialler for Viewdata etc.; PSS, networking. **WW562**

Research Machines *Link 480Z:* parallel port, two RS232, optional network interface. Also disc-based *RML 380Z*, with IEEE-488 interface at about £1900; 8in discs optional. Both machines bought by secondary schools through the Government's microelectronics education programme. Available software is mostly educational. **WW563**

Rockwell *AIM 65:* 44-pin expansion connector accepts five-slot mother-board for disc controller, extra memory etc. Applications connector for i/o, analogue, cassette interfacing. Also available unboxed. *AIM 65/40* is an advanced version with improved keyboard and graphics printer and display. Many expansion modules available for i/o, communications, distributed processing. **WW564**

SBC *Duet 16* system: choice of keyboards and monitors. Two-channel RS232. Hard discs on the way. **WW565**

Semi-Tech *Pied Piper:* portable computer with built-in 800K disc drive. STD-bus expansion port for engineering applications. Hard disc and telephone modem options. **WW566**

Seed System 19: for small businesses, education, research. Dual disc system, hard disc interface. Pascal and C available. Several add-on boards, including i/o, serial, analogue, timer, memory expansions. Also a wire-wrap board for prototyping. **WW567**

Sharp *MZ700:* optional cassette recorder and plotter-printer fit directly into housing. Joystick ports, twin cassette ports. **WW568**

Sinclair *ZX81:* the cheapest home computer. Optional 16K ram pack and small, cheap thermal printer. Many add-ons available from other manufacturers, even a rom word-processor. Powerful but awkward to use. *ZX Spectrum:* 48K version also available. Physically small. Add-ons include thermal printer, expansion modules for tape-loop microdrives, rom cartridge port, joysticks. Large amount of software on cassette, mostly for games. **WW569**

Sirton *Midas MPS:* multi-user system with distributed processing for scientific, technical applications. Storage on 8in or hard discs. Single cable 800kbit/s data link, 1000ft max. Several languages available. **WW570**

Sord *M223/III:* uses Sord's 'Pips' languages. Various versions available with a choice of disc drives. Many interface boards for measurement and control applications. Range includes several other models suitable for engineering including *M416* 16-bit machine. Unusual applications include computer video tape editing. All machines supported by 'Indomitable Energy generated by Great Reliance on "Youth" and "Passion" ' (sic). The Sord *M5* home computer is also available from Computer Games Ltd as the *CGL M5*. **WW571**

Stirling Microsystems *Dennis Microsystem:* modular rack-mounted 6809 system for control applications, scientific, industrial users, hobbyists etc. Optional hi-res. colour graphics, disc controller, ram, p.i.o. boards and some software. Basic system with c.p.u., video and ram boards plus monitor software costs £158: keyboard, p.s.u., rack etc. bring it up to £430, or you could shop around. Interesting possibilities for expansion. **WW572**

SWTP *F/09* system (made in the UK) and *S/09* (from the USA). Modular 6809 systems available in a variety of configurations. Languages include Fortran, Pascal, Pilot and Forth. **WW573**

Tandy. Many models, from which we have picked some of the most recent. *MC10* portable. Moving keys, but display is upper-case only. Ram expandable to 20K. The *Pocket Computer* at £44 has mini-printer and cassette options but no other interfacing possibilities. *TRS-80 Colour Computer:* cartridge port; ram, disc, printer expansions available. *TRS-80 model 100* portable: mainly for business uses, with word-processor and desk diary programs in rom as well as MS-Basic. Telecomms interface included, with software: requires an acoustic coupler. *TRS-80 model 4:* desk-top machine, also available without discs at £651. Keyboard not detachable. *TRS-80 model 12:* desk-top machine, upgradable to 16-bit. D.m.a. Dual disc version also available. *TRS-80 model 16:* multi-user possibilities with TRS-XENIX operating system. D.m.a. **WW574**

Tashkl *OM 8064:* CP/M system with separate 8-slot expansion module. **WW575**

TeleVideo *TS1603:* two RS232 ports, one high-speed RS422 for networking. Memory expansion and graphics options. Other versions available. **WW576**

Texas Instruments *T199/4A:* the cheapest 16 bit computer. Ports for joystick and rom cartridge. Optional eight-slot peripheral expansion for disc-drive, memory extra memory etc. Languages include Forth and UCSD-Pascal. Manufacturer has decided to cease production of this machine and to cut the price to clear stocks. Service facilities are to continue. **WW577**

Torch *700 series:* triple processor arrangement gives access to UNIX and CP/M software. A 6502 handles peripherals and disc caching. Torchnet. *Torch C:* first micro with British Telecom approval. Built-in modem, LAN and TOSCA synchronous communications, hard disc option. **WW578**

Transam *Tuscan:* twin disc drives, separate numeric key-cluster. Univos operating system can read discs in more than 30 formats. Also as a kit. **WW579**

Triumph Adler *Alphatronic PC:* for small business, 'up-market' (sic) hobbyist use, Separate numeric key cluster, rom cartridge port. Floppy disc add-on (£330) comes with CP/M 2.2. Three other models, mainly for office use. **WW580**

Tycom *Microframe:* versatile modular system using 'base-bus-connect' construction; described by maker as the first "future-proof" micro. Can use 8, 16, 32-bit processors. Expansions for text and graphics, peripherals. Supports d.m.a., interrupt-driven devices. **WW581**

Videcom *Apollo:* CP/M micro offering Basic, Cobol and Fortran. Three RS232 ports. **WW582**

Wessex *Wyvern* series of controllers: details are for *WSX1000* + *WSX1001* system, which has 16 i/o lines with handshake, four multiplexed a-to-d channels and one d-to-a. Many expansion modules available for measurement and control, even a speech synthesiser. Modules may be racked or free-standing. VME backplane available soon. Basic interpreter is compatible with software for the Dragon 32 and (via a loader) the Tandy Colour Computer. **WW583**

Windrush *6800, 6809 microcomputers:* rack-mounted systems with a wide range of optional expansion modules – including an eprom programmer, maths chip, ram backup, i/o lines, speech synthesiser. Price quoted excludes keyboard and display. Other models available. **WW584**

Zenith *Z100:* desk top computer with a five-slot expansion chassis and d.m.a. Hard-disc and colour versions available. **WW585**

Improving colour television decoding

Viewing pictures over extended periods, it is apparent that different methods of decoding are suited to different types of picture. A simple one-line comb filter decoder that can be applied to a home tv receiver is described in this series.

In the present colour television systems luminance and chrominance information shares the spectral space available within band limits set by international agreement. On receivers decoding PAL or NTSC signals and using a common notch, the picture is degraded by residual subcarrier, seen as moving dots on vertical coloured edges (cross luminance), and by spurious colours produced by luminance components being demodulated as chrominance (cross colour). These system imperfections are detailed and ways of reducing their visual effect suggested, together with a procedure for obtaining wider luminance bandwidth by removing the luminance channel notch filter.

The first part shows spectral energy distribution of the composite PAL signal, the quadrature colour subcarrier phase relationships across adjacent line, field and picture periods, and alternative methods of decoding that enhance some performance parameters to the disadvantage of others. Viewing pictures over extended periods, it is apparent that the different methods of decoding are suited to different types of pictures.

The parameters of the PAL system will establish themselves in the following text, but an understanding of the basic television waveform is assumed.

To decode using a comb filter, which relies on the spectral distribution, luminance and chrominance relationships must be established. Figure 1 illustrates the spectrum of a video signal operating on PAL standard video while Fig. 2 shows the luminance components of the scene and shows how the periodic scanning system produces frequency interleaving. The diagram explains the Nf_L structure (integers of line frequency). Fig. 3 shows the U (weighted B−Y) chrominance spectrum with a note explaining f_{sc} (colour subcarrier) derivation. In this diagram the frequency of the subcarrier used is (284−¼)×15.625kHz, and forms the centre for the new chrominance spectrum sidebands, which decay in amplitude as shown and repeat either side of the subcarrier frequency at 15.625kHz spacings – but always offset by one-quarter of line frequency lower than the line spectral luminance centres.

Fig. 3 shows that the groups of energy forming the V (weighted R−Y) spectrum would overlay the U-chrominance but for the PAL (squarewave) 7.8kHz squarewave which is added in the V-chrominance mod-

by David Read
B.Sc.(Hons), M.I.E.E.

ulator in the PAL coder. The spectrum is thus shifted by ±½ the line frequency, Fig. 4. Combining the spectral diagrams of Y, U and V with the aid of vectors, Fig. 5(a) provides a representation of V-axis switching, show in Fig. 5(b). This would represent an adjacent line in the field compared with the line in Fig. 5(a), where the V-axis has been switched to the opposite direction. To understand how these spectral diagrams are derived and to assess some of the decoding techniques it is worthwhile explaining the PAL encoder of Fig. 6.

PAL encoding

Incoming signals representing the red, green and blue primary colour components of the scene (R,G,B) containing frequencies up to 5.5MHz are first reproportioned by a resistive matrix (inverting amplifiers provide the negative contributions). The resulting signals are a luminance Y signal (black and white scene detail) and two colour difference signals B−Y and R−Y. After amplitude weighting these components become the U and V signals where U=0.493(B−Y) and V=0.877(R−Y). This re-arrangement is required to produce a transmittable PAL waveform and is not directly concerned with the process of decoding to be discussed.

The colour difference signals from the matrix are filtered, Fig. 7, and applied to separate modulators together with feeds of colour subcarrier in quadrature. In addition the V demodulator has its subcarrier switched on alternate lines at 7.8kHz (the PAL squarewave or vertical axis switch). The luminance channel is delayed to match delays in the chroma low-pass filters and modulator. Also syncs are added and an amplitude preset is provided. The three signals, Y and modulated U and V, are then summed and the final output of the encoder filtered to 5.5MHz. This low-pass filter, defining the luminance bandwidth, cuts some of the upper sideband energy from the chrominance modulators, as well as $2f_{sc}$ and $3f_{sc}$ products. The final output is shown in Fig. 8.

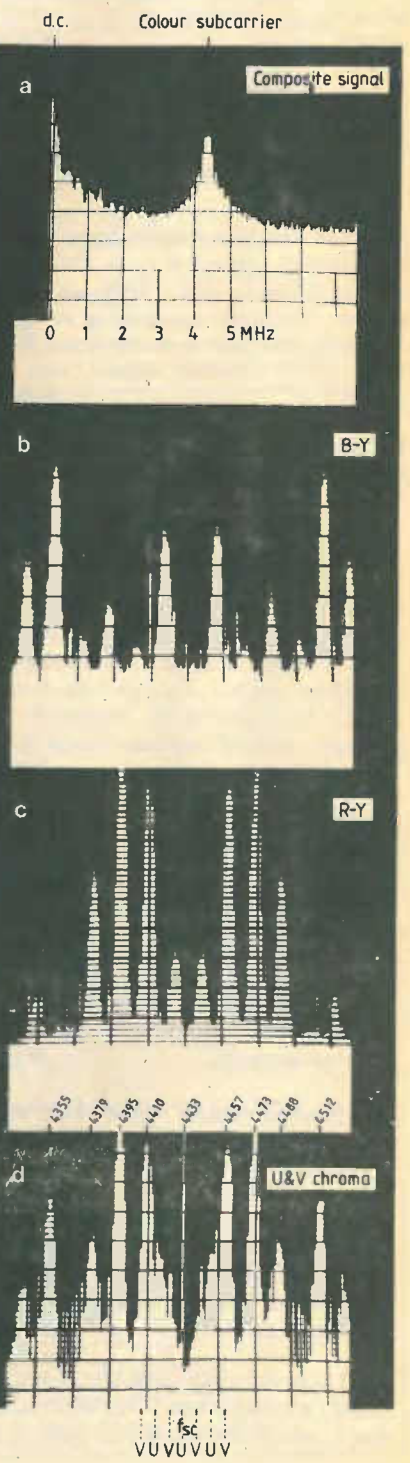


Fig. 1. This video signal (a) is from the PAL encoder with 100% colour bars. With vertical chroma bars there is no change in chroma line-by-line and the waveform provides a steady pattern of chroma sidebands. Trace of spectral energy (b) shows the PAL encoder output with U-axis modulation only. Trace (c) shows encoder output V-axis quadrature modulation. Bottom shows both U and V chroma modulation with the sidebands interleaving for 100% bars (d).

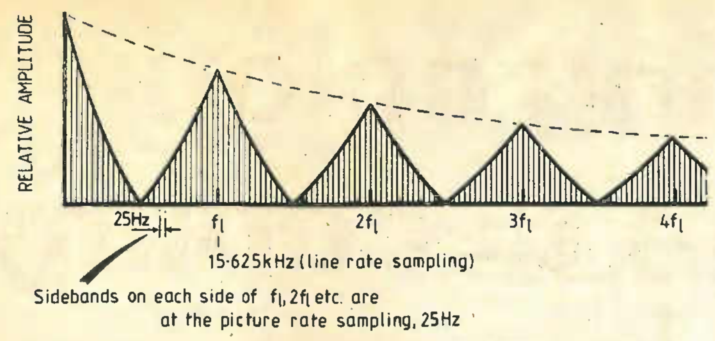


Fig. 2. Spectrum of luminance component of a television signal with 15.625kHz sequential scanning of a stationary picture. Scene is sampled at 15.625kHz for 625 lines and 25 pictures per second are constructed. The spectral energy centres are therefore at line frequency f_L and at $2f_L$, $3f_L$, etc. Spacing of sidebands about the multiples of f_L is 25Hz, which is the picture rate.

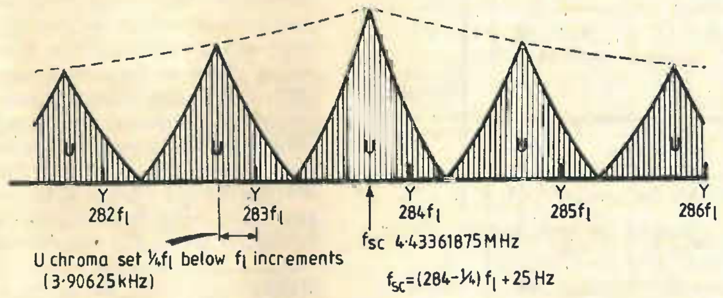


Fig. 3. U chrominance signal spectrum (also representing the V spectrum, except for the V-axis switching). The 25Hz can be ignored because only line-frequency harmonics around $284f_L$ are considered, where the phase shift is negligible. Colour subcarrier (f_{sc}) of 4.43MHz carrying the difference signal is derived as f_{sc}=(284−¼)×15.625kHz+25Hz. As 25Hz is very small compared to (284−¼)×f_L it is ignored. Note the U-spectrum is symmetrical about f_{sc}. Therefore as the modulator carrier is high ($2f_{sc}$=8.866MHz) and causes spectrum reversal, the PAL modifier has no effect on the U vectors.

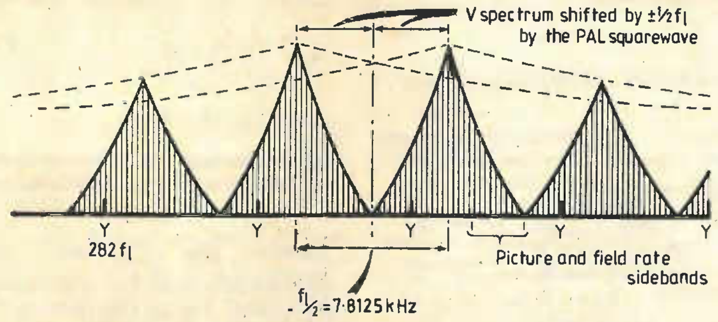


Fig. 4. V-axis spectral energy groups are alternatively reversed about the centre of subcarrier frequency at half the line frequency (7.8kHz).

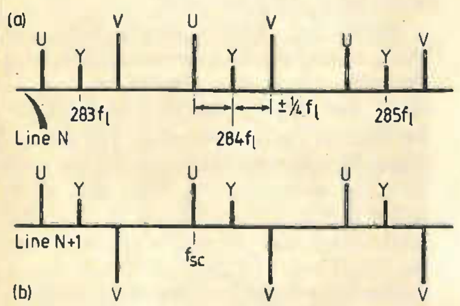


Fig. 5. Y, U and V spectra combined and simplified. Bringing these U and V spectrum diagrams together, but simplifying them by not showing the decaying picture-rate sidebands, results in (a). U has a quarter-line offset (low) with respect to the Y signal spaced at multiples of line frequency. V has a quarter-line offset above the multiples of line frequency. Note, there is no spectral peak component dominant at the half line frequencies.

Subcarrier phase relationships across lines, fields and pictures

The subcarrier phase relationships over four adjacent lines of a television field, Fig. 9, show that lines N and N+2 cancel, whereas the luminance components which are predominantly in-phase across the lines (vertically) add. Equally, taking the difference of the same two lines, the chrominance augments and the luminance components largely cancel. This is one method of decoding. The summing action incidentally results in a 3dB noise reduction.

Fig. 10 shows line N as before but the next trace down shows line N emerging from a delay line 56ns (i.e. 90° of the subcarrier) short of the 64μs one-line period. Because of this difference, line N emerges a quarter of a line early with respect to line N+1. Thus, the chrominance sinewaves from line N+1 and the signal from the delay line are antiphase, and adding them causes chroma cancellation. Operating across adjacent lines in a field is better than operating across two lines as shown in Fig. 9 because vertical resolution loss is visibly less on pictures.

As PAL encoding involves quadrature modulation of the subcarrier such that the U components cancel and the switched quadrature V components add, it is better to draw the two vectors representing the quadrature modulation in the form shown in Fig. 11(a). This diagram shows another decoding technique in which line N, N+2 and N+4 are added and subtracted using weighting factors of ¼, ½ and ¼ to enhance either the chrominance or luminance components. A circuit using this technique was built and the block diagram explaining this arrangement is the lower part of Fig. 11(b). Fig. 11(c) gives a mathematical derivation for the output of ¼-½-¼ adder, indicating the shape of the comb filter response.

This method involves decoding over five adjacent lines in each field. But this represents ten lines per picture, so the vertical resolution is much impaired, with diagonal luminance errors and horizontal colour changes producing strange effects on pictures.

The right-hand part of Fig. 11(a) shows the signal in vector form when a chrom-length delay is used. Chroma-length delay is the delay of one television line (64μs) minus the quarter-line offset (56.39ns), equivalent to 283.5 cycles of f_{sc} with this

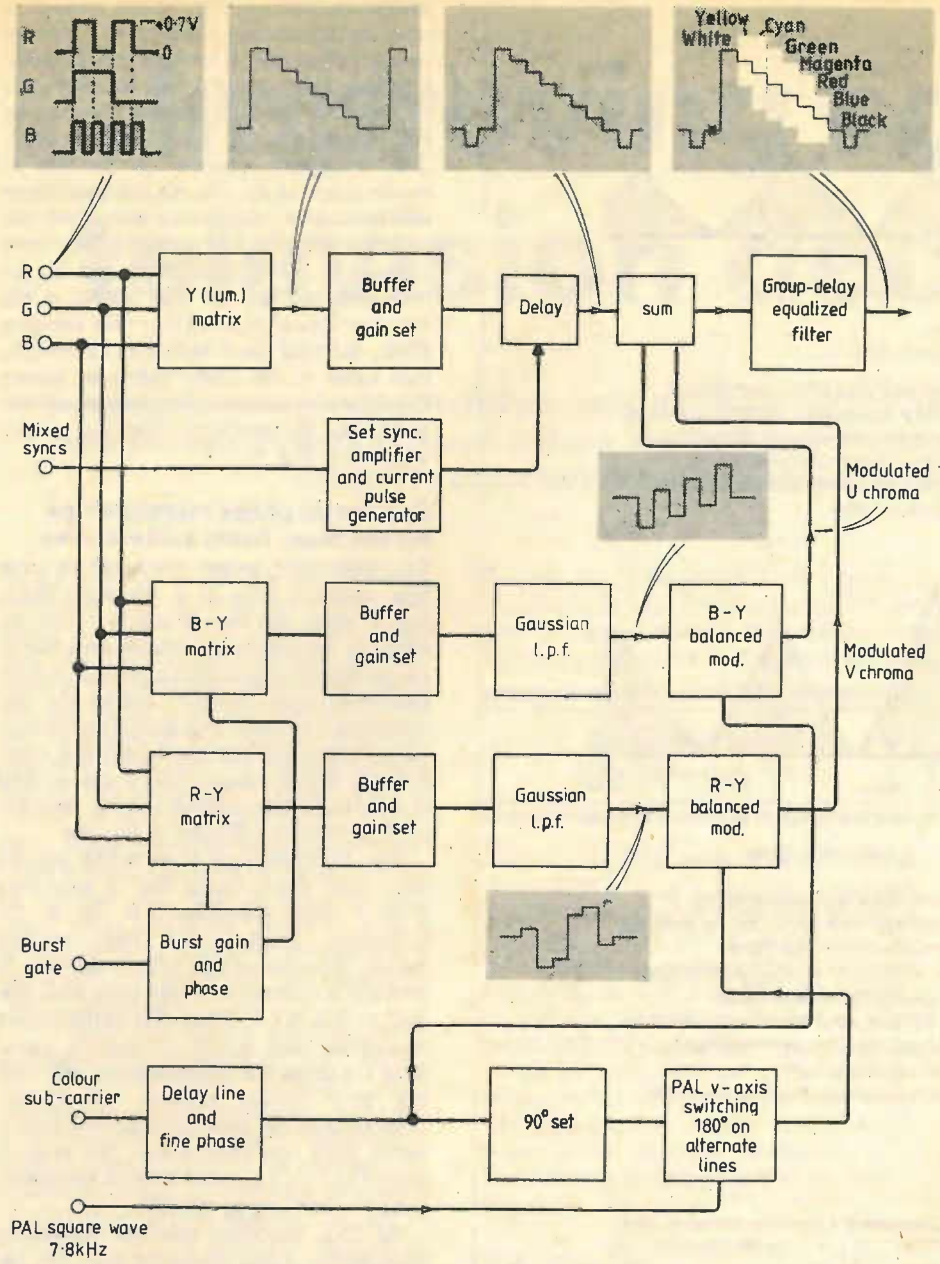


Fig. 6. Block diagragm of PAL encoder illustrates waveforms for input of 100% colour bars.

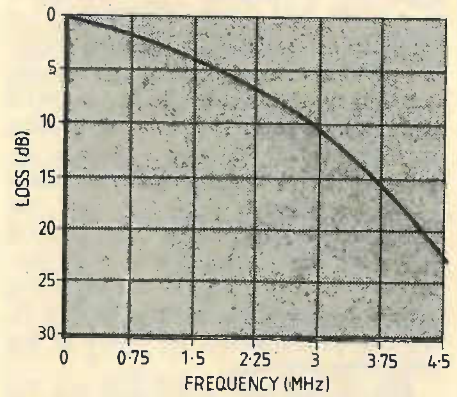


Fig. 7. Characteristics of the filters used in front of R−Y and B−Y modulators in the PAL encoder. These are linear-phase Gaussian filters with 3dB loss at 1.3MHz.

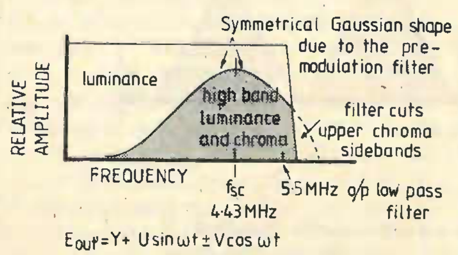


Fig 8. PAL encoder output signal showing the shaping y chrome pre-modulator filters and the output filter. Output signal is as shown, where Y is the luminance component, Usinωt is the B−Y colour component, and Vcos ωt is the R−Y colour component both modulated onto the 4.43MHz subcarrier. The cos term shows quadrature phase relationship between U and V. ± indicates the alternating V axis.

delay, the 90° rotation (56ns) does not have to be considered; the V-axis signal phase being simply reversed on alternate lines as before. Addition and subtraction of adjacent lines either enhances the V or the U signal but it does not produce cancellation of the predominant vertical luminance because the picture points are not aligned vertically, being horizontally staggered by 56ns. This technique can therefore be used in the chroma circuit (56ns is small in terms of chroma resolution) and three lines are combined in the amplitude ratio ¼:½:¼ for enhancing both U and V components. Fig. 12(a) which shows the oscilloscope display of a horizontal colour bar signal indicating reduced horizontal resolution; and (b) is a colour picture with only chroma present (see also colour print 1, to follow). The chroma comb filter reduces the amount of luminance that enters the two chroma demodulators, and so reduces the fine cross-colour i.e. luminance at 4.43MHz by a half (6dB).

When the chroma length delays are used, signals subtract across adjacent lines. Spatially, there is a vertical shift in the scene, but there is also an horizontal shift by 56ns (113ns for two lines). The result of using 64μs delays and arranging the comb filters to operate across three lines to enhance luminance are shown in Fig.12(c). This shows that chroma is removed well, but the loss of diagonal luminance is visible with some pictures. To obtain signals relating to positions on the screen that are spatially coincident, they must be taken from adjacent pictures (two fields apart). To illustrate this, Fig. 13 shows the U and V chrominance phase relationships over an eight-field period (i.e. a complete change of the subcarrier phase-to-line relationship).

Notice that Fig.13(a) shows the recommended U and V quadrature modulated in the coder and burst phase relationships to the line timing as defined by the E B U, but to simplify explanation, subsequent diagrams do not adhere strictly to this definition.

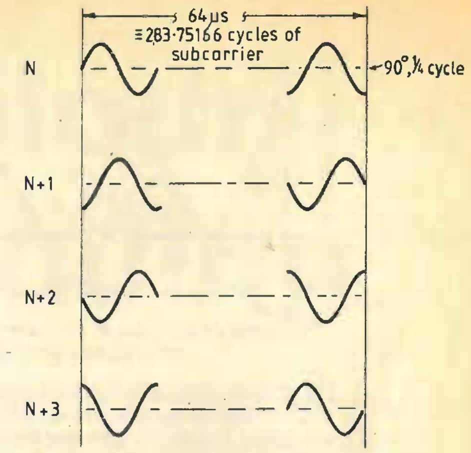


Fig. 9. To simplify explanation four adjacent lines in the field are numbered N, N+1, N+2 and N+3 and considered to contain only continuous unmodulated subcarrier. Top of diagram shows the subcarrier waveform extending from the beginning to the end of line N over the period of 6μs. In this period there are (283−¼)f_L cycles in the line period. The frequency is reduced and there is a 90° difference in subcarrier phase between the beginning and the end of the line. During the next N+1 line the subcarrier continues, again with a quarter-cycle reduction ending 90° short. The diagram shows that lines N+2 and N+3 are similarly built up. (25Hz term in the f_{sc} derivation is so small considering phase shift between adjacent lines that it has been ignored).

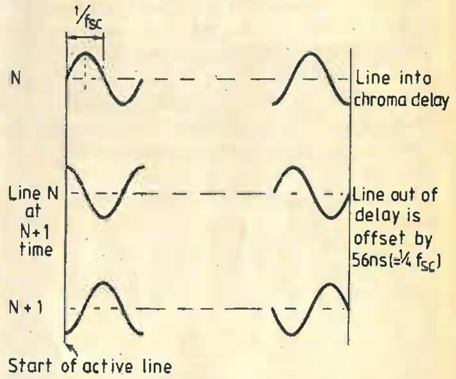


Fig. 10. Adjacent lines from one tv field with a chroma delay (64μs−54ns) used.

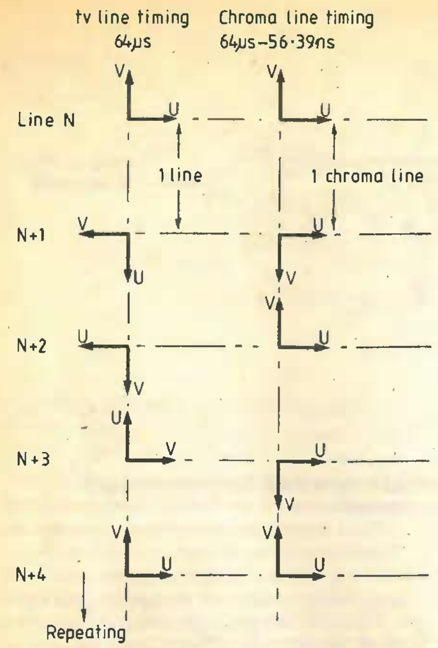


Fig. 11(a). Change in U and V vectors considering adjacent lines in one field. This diagram shows U and V phase relationships on lines N, N+1, N+2, N+3 etc. Starting arbitrarily on line N and V (representing the R−Y modulated chroma in vector form) drawn vertically and U (B−Y chroma) horizontally to the right. One tv line later on line N+1, left side of diagram, the U-signal rotates by 90° because of the quarter-cycle f_{sc} offset. U-signal is now vertically down. V-signal phase has reversed because of the PAL switch and has also rotated clockwise by 90° because of quarter-cycle offset. V-vector is now to the left. One line later, N+2, U will rotate clockwise by 90° because of quarter-cycle offset. V-phase has again reversed and rotated by 90° (quarter-cycle offset). Vectors are now as shown on the third line down. In the same way, the diagram builds up lines N+3 and N+4 phase relationships.

Luminance and chrominance enhancement across field or picture

In considering timing relationships which compare adjacent lines, the 25Hz term in the subcarrier expression has been ignored. But when shifting 625 lines between the same spatial points in adjacent pictures which rperesent 40ms time shift the 25Hz term is significant and is included in the calculation in Fig.13(b). Adding picture 1 (P_1) and picture 3 (P_3) causes the chrominance to cancel and the luminance to enhance, see the block diagram, part of Fig.13(b).

Because these picture-spaced video signals are exactly overlaid there are no unwanted effects from luminance components at frequencies in the subcarrier region, or at any angular position (i.e. diagonals), such as occur with adjacent line comb decoders. These cause discrepancies in the chrominance and luminance separation. Decoding across picture delays, luminance and chrominance signals can be separated with more of the individual sidebands combed. There will be no bandwidth limitation as would occur with a notch, and the residual subcarrier in the luminance channel will be even lower as the subcarrier sidebands are taken from

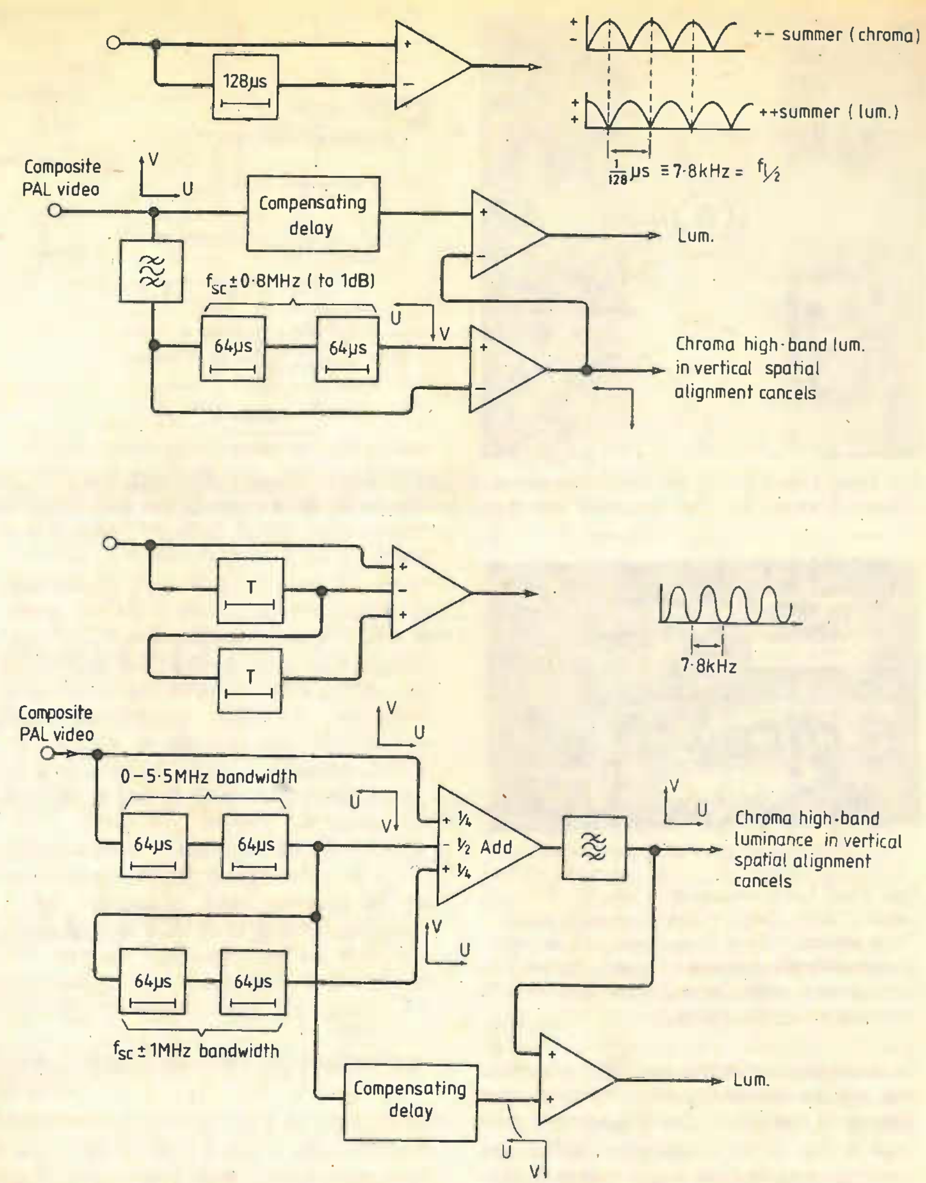


Fig. 11(b). Block diagram of a filter operating over a three-line period with ½:½ contribution from the outer lines (top) or across five lines in the ratio ¼:½:¼ i.e. lines N, N+2, N+4, (bottom).

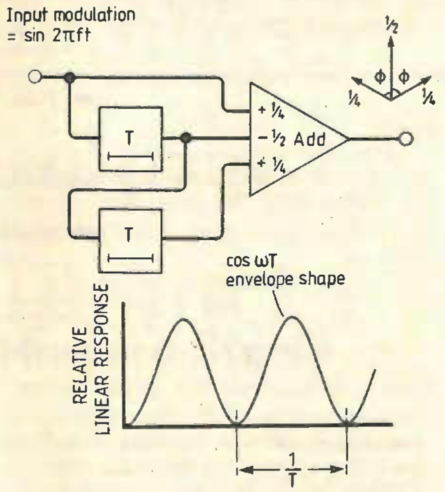


Fig. 11(c). Derivation of comb filter characteristic using algebra and vector diagram. Output is vector sum of the three contributions. Phase angle (ϕ=2π fT) swings between 0° and 180° as the modulation, representing the tv signal, swings between 0-5MHz. When ϕ=0° signal doubles, ϕ=180° signal cancels. Output signal is

$$\tfrac{1}{4}\sin\omega t-\tfrac{1}{2}\sin\omega(t+T)+\tfrac{1}{4}\sin\omega(t+2T)$$

Subtract T from each

$$\tfrac{1}{4}\sin\omega(t-T)-\tfrac{1}{2}\sin\omega t+\tfrac{1}{4}\sin\omega(t+T)$$

$$=\tfrac{1}{2}\sin\omega t+\tfrac{1}{4}(\sin\omega t\cos\omega T-\cos\omega t\sin\omega T)+\tfrac{1}{4}(\sin\omega t\cos\omega T+\cos\omega t\sin\omega T)$$

$$=\tfrac{1}{2}\sin\omega t+\tfrac{1}{2}\sin\omega t\cos\omega T$$

$$=\tfrac{1}{2}\sin\omega t(\cos\omega T-1)$$

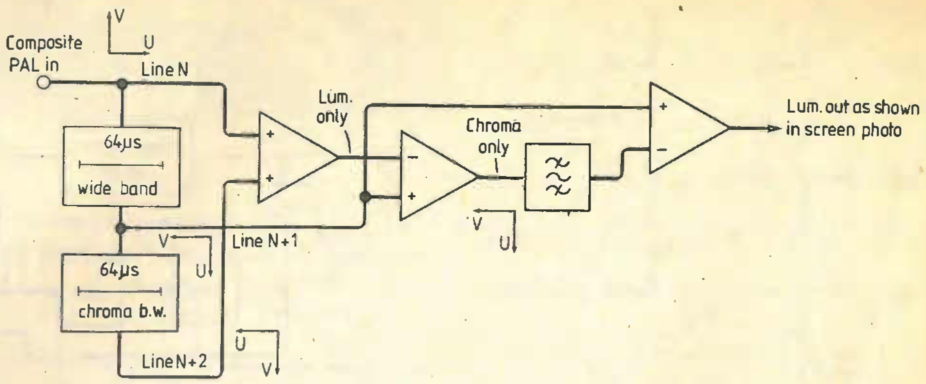


Fig. 12(c). Using a zone plate test signal the display shows luminance comb operating across three lines in one field, illustrating loss of diagonal resolution. The 'returned' resolution within the boxes is inverted, but is not significant on pictures.

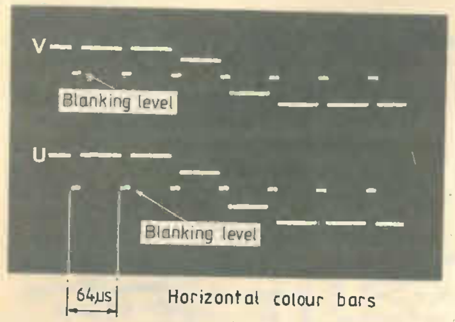


Fig. 12(a). Trace shows R–Y and B–Y outputs from chroma demodulators using three adjacent lines from a field in the ratio ¼:½:¼. Steps indicate reduced rate of change over a vertical transition from green to magneta, see (b).

the luminance channel at 25Hz intervals (for picture store decoding), which is the spacing of the comb. Comb spacing is derived in Fig. 11(b). Luminance information is therefore preserved in the region of the chrominance band and this will improve fine detail in the displayed picture. Again, the comb does not involve LC filters, as digital filtering field and picture delays are used and there are none of the problems assocated with group delay.

Under the special condition of still pictures, picture delay decoding can produce near-perfect results giving no visible cross-colour or cross-luminance. However, as the information combined is taken across two pictures and represents a time shift of 80ms, temporal components representing movement are significant. Even if the components of the scene are themselves stationary, the camera normally 'pans' so that the picture information has positional displacement and the changes result in the decoder not working perfectly. As soon as fast panning of the camera occurs the decoding method becomes unsatisfactory *therefore* and we must pursue other decoding methods or adaption between line field/picture spaced decoding, because good decoding is only available on slow movement.

The next experimental decoding method makes a compromise between the temporal and spatial factors by use of delays of 312 lines twice, representing one picture of storage. In Fig.13(a), if lines 622 (end of field 8), 309 (end of field 1) and 621 (end of field 2) were combined in the amplitude

Fig. 13(a). Full eight-field sequence over which the colour subcarrier phase sequence repeats. The pairs of rounded vectors show U/V phases across field and picture intervals. (From EBU statement D22-1979).

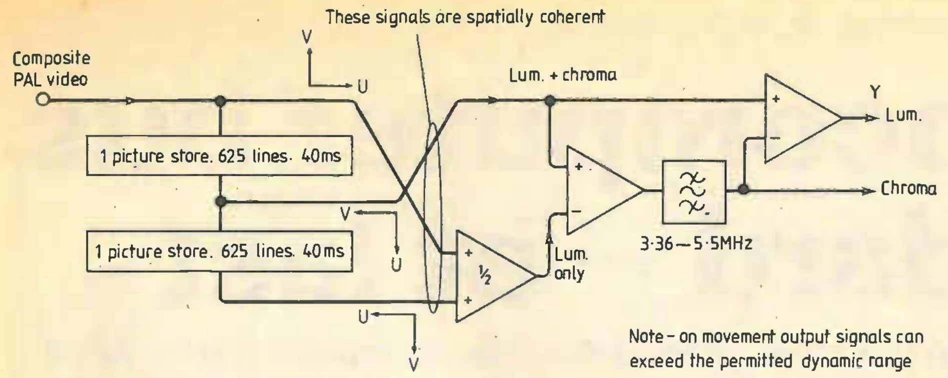


Fig. 13(b). Block diagram of circuit to decode between picture periods. Coded-colour signal components Y, U and V derived from adjacent pictures describing the same spatial point on the display can be decoded as shown. Frequency of the colour subcarrier can be calculated from the expression already shown to give 4.42261875MHz. As field rate is 50Hz and there are two interlaced fields in each picture, the picture rate is evidently 25Hz, 0or one every 40 ms. By dividing the period of the colour ($1/f_{sc}$=225.549389ns) into the picture period we obtain the number of colour subcarrier cycles occurring in one picture. Number of cycles of subcarrier is 40×10^6/225.549389=177,344.75 cycles per picture. The 0.75 (≡270°) indicates three quadrants of phase shift. Phase relationships across picture periods are thus established. Number of cycles in two picture periods (80 ms) is 354,689.5 (≡180°).

ratios of ¼:½:¼ and a sum and difference across the three lines taken, the luminance and chrominance can be combed. Temporal errors are now halved, but because three adjacent lines in each picture are used in comb filtering spatial problems arise that cause diagonal luminance components to enter the chrominance circuits and produce cross-colour. And horizontal or diagonal colour changes prevent the comb from removing colour subcarrier from the luminance, resulting in cross-luminance.

When combing between adjacent lines or adjacent pairs of lines the luminance signal is only losing its vertical resolution in the high frequency energy areas above 3.3MHz. It is therefore difficult to detect the loss of vertical resolution on luminance; in fact it shows up on diagonals, Fig.12(c). It may appear a simple matter to look across the picture delay for temporal components and subtract, look for the differences detecting movement and then switch back to adjacent line decoding to prevent temporal effects maring the decoding. But in coded PAL the coded subcarrier is a moving pattern on stationary coloured parts of the scene and the detecting methods are not straightforward.

The subcarrier only returns to its original phase after eight fields, Fig. 13(a). This moving subcarrier can be misinterpreted as picture movement and adds to the difficulty of movement detection.

Changing subcarrier frequency by 6.25Hz

If the subcarrier frequency is reduced by 6.25Hz, both the U and V chrominance signals are in antiphase over one picture period, Fig.14. Comb filtering can be carried out by addition and subtraction across these spatially coincident points. Thus picture decoding is again achieved on still pictures; where movement occurs the impairments from temporal displacement effects will be halved. The change of subcarrier frequency by 6.25Hz is unlikely to cause mis-operation of the phase-locked loops used for subcarrier regeneration in the receiver because capture ranges are typically greater than 500Hz. It would however be too big a change for broadcasters to accommodate, requiring modification of many items of equipment. Further, although the amount of storage required to obtain a good comb filter decoder is halved, it is still expensive for use in a home receiver.

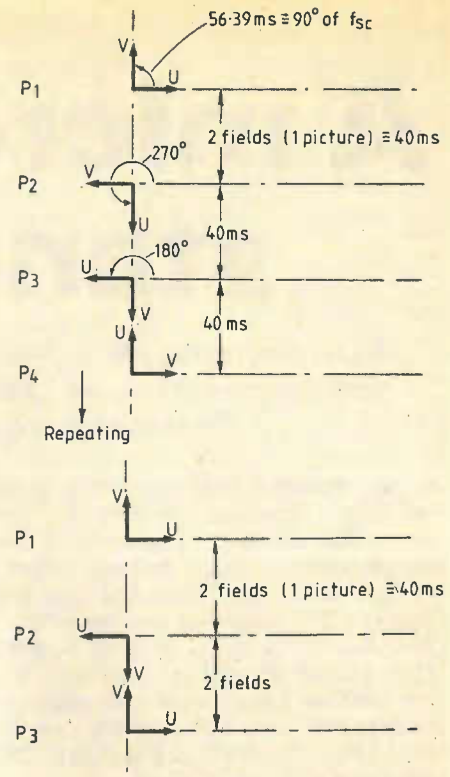


Fig. 14. By raising colour subcarrier by 6.25Hz, perfect decoding of still pictures free of cross-luminance and cross-colour can be obtained using one 625line picture store.

continued from page 34

plifier. Moreover the system has a slight memory, although a rapidly fading one, of its previous experience.

Alternatively, instead of being restricted to high frequency oscillations, much longer delays can be synthesized using charge-coupled delay lines for experimental investigations. The crudest system is the thermostatically-controlled central heating system, and the 'flying' regulator on steam engines which displays a large inertia or reluctance to change.

This analysis of time delay or Markovian systems fits into a wider scheme of knowledge including a realistic modelling of gravitational interactions, de Broglie wave behaviour of electrons in atoms and co-operative phenomena, for example ferro-magnetism, stimulated emission, and nuclear fission.

In a realistic physics the finite time delay interactions are postulated to be mediated by 'field particles', the flux of which obeys the geometrical law of intensity $1/r^{d-1}$ in arbitrary d-dimensions. This is just the beginning and a lot of work needs to be done.

Howard Steele

Howard Steele, television engineer, died on October 11th. After a meteoric rise through a graduate apprenticeship with Marconi, via Alpha Television Studios and ABC Television, he became, at 36 years old, Chief Engineer of the Independant Television Authority and supervised the preparation for the launch of ITA's 625-line colour tv service. He had earlier been involved with colour tv research at the ITA Research establishment and worked on the early development of colour system transcoders. In 1978 he was appointed Managing Director of Sony Broadcast Ltd.

In addition to his working career, Howard Steele was deeply involved with the Institution of Electrical Engineers and served on several committees and boards. He was also involved in several international institutions including the EBU and the CCIR. He was awarded a special Citation at the 1969 Montreux International television symposium for his work on tv systems and in May this year, the Gold Medal of the Royal Television Society for "outstanding services to television over more than a quarter of a century. His particular contributions included the planning and design of television studios, the introduction of the u.h.f colour service to the ITV network and his role with national and international organisations on the formulation of technical standards".

A microcomputer bus standard – at last

As an electronics engineer faced with developing a microprocessor-based system, which computer databus will you choose? Tim Roberts, managing director of High Technology Electronics, explores the story, development and scope of IEEE696.

If your answer is S100, you are in good company. Most developments in the microcomputer field – especially 16 bit multiprocessors, direct memory access, cache memory, hard discs, and even the mighty CP/M operating system itself – have become available on S100 systems first. Though not well-known in the UK, the S100 bus has achieved high respectability in the United States, having recently been adopted as an official standard by the influential IEEE, as IEEE696.

At last designers trying to put together 'intelligent' systems will be able to rely on an official S100 standard which will eventually take over from the several variations of the bus that are in widespread use.

S100 has become a *de facto* standard largely because it was the first microprocessor databus in the field. It remains both effective and flexible, giving full scope to experimenters or developers wanting some later up-grade capability, but equally to the builders of top-level high-integrity systems. It has won a large following in the USA and with the emergence of British specialist suppliers of S100 function cards it is finding greater favour with British designers.

The S100 bus came about at the birth of the microcomputer industry as a result of a publishing initiative. When in 1974 the US magazine *Radio Electronics* launched its Mark 8 home computer, *Popular Electronics* responded by commissioning the Altair 8800 from a small company, MITS. In many ways, MITS got it right; the Altair was modular and the computer's functional circuit boards plugged into a 'motherboard', interconnections being made over a group of common lines; that is a databus. The designers obtained a 'job lot' of backplane connectors that had 100 pins. Onto the lines went buffered control, address and data lines from the 8080 microprocessor which had recently been launched by Intel, then a young little-known company.

Inevitably other companies went on to improve on the Altair but they kept the same bus, which became known as the Altair bus, Altair/IMSAI bus, and by various other names. Other entrepreneurs weighed in with bus-compatible add-on expansion, peripherals and full computers. And by then the original bus was widely accepted as a standard so proprietorial names were dropped in favour of S100, standing for 'standard 100-pin bus'.

By-and-large the original pin allocations, though not always ideal, were adhered to but manufacturers lost their conformity when it came to signal timing and application of previously unused lines. When it was suggested to the IEEE that things were getting out of hand and that a formal standard was needed, the IEEE set up a working group. After much consultation with industry, the group – a sub-committee of the microprocessor standards committee – agreed on an enhanced bus which allowed for 16-bit as well as eight-bit processors and memory, and could accept most modern processors. The enhanced bus gained its final seal of approval as a real and usable standard in March this year.

by P.T.H. Roberts M.A.

Bus standards

Computers do not have to have buses; many rely on loosely-coupled processors communicating with each other on point-to-point serial links. Such computers cannot be modified or expanded without changing the wiring.

In contrast are the more tightly coupled systems in which several processors share a common bus. The bus may be global, allowing processors to share the available memory and input/output on an arbitrated priority basis. Otherwise a mixture of global and local bus is used; each processor has a local bus with its own block of programmable memory, but the processors are connected globally and organised in a hierarchical fashion.

All microcomputer buses provide a format for the connection of data, address and control lines. Some buses, such as STD, simply provide a pathway between processors and their memory and i/o lines, and have no circuitry interfacing the processor to the backplane. Other buses achieve a higher functional capability with some minimal circuitry; S100, Multibus and Versa/VME are in this class. Higher-level buses still, such as Eurobus, have special chip sets and communication protocols, while the proposed Futurebus may have a microprogrammed subsystem as processor-blackplane interface, providing a high-level fault-tolerant backplane interface, providing a high-level fault-tolerant architecture.

Efforts are being made to roll back the tide of bus anarchy. The Eurocard version of the STD bus (P961), for example, has strong support, but the handful of manufacturers who market a range of STD bus cards on the older card size and using a direct connector have so far provided an effective rearguard opposition. Like S100, STD appeals to the 'keep it simple' school. The signal set is a derivative of the 8080/Z80 class of processors but because of its simplicity it can be difficult to interface other processors such as the 6809 or 6502 to it without penalising them on timing. Most of these problems can be overcome with care.

Multibus (A796) has been plagued by differences of opinion over standards, the IEEE Multibus committee members wanting consistency in nomenclature, but each wanting that consistency to be in line with his own habitual notation. Nevertheless recent progress has been made in this area, and over changes to power supplies, the advanced acknowledge signal, 16-bit addressing techniques, and board sizes. Multibus is an 86-pin format originally developed by Intel for its SBC series of cpu, memory, i/o, communications, high-speed maths and dma control boards. The bus lends itself to multimaster operation with multiplexed processors, dma controllers and disc controllers.

Versabus, born of Motorola's need to accommodate various processors including its own eight-bit (6800), 16-bit (68000) and 32-bit devices, has 260 pins, divided between two edge connectors on large (14.5 by 9.14in) boards. A version of it dedicated to large systems is currently in the standardization procedure within the IEEE as P970. The similar VME bus is better known in Europe because of its DIN connector and Eurocard format, but is not yet in the IEEE standardization mill. Versabus was partly a response to slow progress of the proposed Futurebus in becoming standardized.

One of the best-conceived buses, Eurobus – developed by the Admiralty Surface Weapons Establishment – is little used despite its acceptance by BSI, ISO, and ESONE. Perhaps this is because it was developed for military application and because of controversy over its quick acceptance by BSI. Nevertheless its design has been well funded, its protocols formally verified, and it is the only example of a bus which has a dedicated lsi chip set available for interfacing processors to the backplane.

Futurebus (P896) is still a long way ahead. An ambitious concept, providing a communications highway between processors in fault-tolerant processor systems, it has been subject to political controversy. An early draft of it was said to be too similar to Eurobus and to share shortcomings of VME bus in the driver and back-plane-termination/network areas; P896 was also multiplexed whereas VME was not. But new drafts are now in preparation. Goals of the Futurebus committee are to provide true multiprocessor capability, processor and manufacturer independance and fault tolerance to a high level on a Eurocard/DIN format.

In being first past the post, the S100 (P696), has gone a long way in winning widespread confidence. It provides an impressive example of how an *ad hoc* collection of signals and mechanical formats which have been copied and modified by various manufacturers to a degree where they are no longer compatible, has been taken by a group of dedicated enthusiasts and transformed into a competent and usable standard.

While buses like Multibus, S100 and STD – all originally derived from the 8080 signal set – differ mechanically in the USA at least their signal connections are similar, and a degree of standardization exists. In Europe on the other hand, there is a great need for bus standardization; the DIN connector and Eurocard are standard enough, but there are over 60 microcomputer buses using them – most of them proprietary!

Thought on a microelectronics timescale the S100 is venerable, it is nevertheless one of the highest performance buses available today. It is a mid-range bus, without the inherent intelligence of a Eurobus or Futurebus, but providing the flexibility to satisfy knowledgeable users wanting quick, cost-effective solutions. It supports both eight and 16-bit processors, up to 16Mbyta of memory and 64K ports. Almost every tape of processor can be used.

Designers are only too familiar with the fact that in any new system, only a small core warrants entirely new design and that most of the functions could be built up with standard circuits if they were available. S100 meets just this need. With almost 150 o.e.ms and 1000 circuit cards to choose from – more if other standards cards embodying S100 adaptors are included – S100 frees the designer to concentrate creative attention on the new core by allowing quick assembly of the rest, Lego-style, from standard building blocks.

IEEE standard

The new standard IEEE696/S100 bus has 16-bit capability, can accept between four and 22 boards and has a practical maximum data rate of 10MHz (the standard is 6MHz). It supports up to 16 megabytes of memory (24 address lines) and has 43 control timing and status signals; 16 data lines and eight power supply and earth lines. Other lines are reserved for future use or are not defined.

IEEE696 S100 bus pin list

Pin	Signal	Active level	Description
1	+8V (B)		Average max <11V
2	+16V (B)		Average max. <21.5V
3	XRDY (S)	H	One of two ready inputs to current bus master. Bus ready when both are true (see pin 72)
4	$\overline{VI_0}$ (S)	L o.c.	Vectored interrupt lines 0 to 7
5	$\overline{VI_1}$ (S)	L o.c.	
6	$\overline{VI_2}$ (S)	L o.c.	
7	$\overline{VI_3}$ (S)	L o.c.	
8	$\overline{VI_4}$ (S)	L o.c.	
9	$\overline{VI_5}$ (S)	L o.c.	
10	$\overline{VI_6}$ (S)	L o.c.	
11	$\overline{VI_7}$ (S)	L o.c.	
12	$\overline{NMI}$ (S)	L o.c.	Non-maskable interrupt
13	$\overline{PWRFAIL}$ (B)	L	Power fail bus signal
14	$\overline{TMA_3}$ (M)	L o.c.	TM priority bit 3
15	A_{18} (M)	H	Extended address bit 18
16	A_{16} (M)	H	Extended address bit 16
17	A_{17} (M)	H	Extended address bit 17
18	$\overline{SDSB}$ (M)	L o.c.	Disable 8 status signals
19	$\overline{CDSB}$ (M)	L o.c.	Disable 5 control output
20	0V (B)		Common with pin 100
21	NDEF		Not defined (maker specifies use)
22	$\overline{ADSB}$ (M)	L o.c.	Disable address signals
23	$\overline{DODSB}$ (M)	L o.c.	Disable data output
24	Φ (B)	A	Master bus timing signal
25	pSTVAL (M)	L	Status valid strobe
26	pHLDA (M)	H	Used with HOLD to coordinate bus master transfer operations
27	RFU		Reserved for future use
28	RFU		Reserved for future use
29	A_5 (M)	H	Address bit 5
30	A_4 (M)	H	Address bit 4
31	A_3 (M)	H	Address bit 3
32	A_{15} (M)	H	Address bit 15 (most signifiant for non-extended addressing)
33	A_{12} (M)	H	Address bit 12
34	A_9 (M)	H	Address bit 9
35	DO_1 (M) ED_1 (M/S)	H	Data out bit 1 bidirectional even data bit 1
36	DO_0 (M) ED_0 (M/S)	H	Data out bit 0 even data bit 0
37	A_{10} (M)	H	Address bit 10
38	DO_4 (M) ED_4 (M/S)	H	Data out bit 4 even data bit 4
39	DO_5 (M) ED_5 (M/S)	H	Data out bit 5 even data bit 5
40	DO_6 (M) ED_6 (M/S)	H	Data out bit 6 even data bit 6
41	DI_2 (S) OD_2 (M/S)	H	Data in bit 2 odd data bit 2
42	DI_3 (S) OD_3 (M/S)	H	Data in bit 3 odd data bit 3
43	DI_7 (S) OD_7 (M/S)	H	Data in bit 7 odd data bit 7
44	sM_1 (M)	H	Indicates current cycle is op-code fetch
45	sOUT (M)	H	Identifies data transfer bus cycle to output device
46	sINP (M)	H	Identifies data transfer bus cycle from input device
47	sMEMR (M)	H	Identifies bus cycles that transfer data from memory to bus master which are not interrupt acknowledge instruction fetch cycle(s)
48	sHLTA (M)	H	Acknowledges HLT instruction executed
49	CLOCK (B)	A	2 MHz (±0.5%) 40-60% duty cycle
50	0V (B)		Common with pin 100
51	+8V (B)		Common with pin 1
52	−16V (B)		
53	0V (B)		Common with pin 100
54	$\overline{SLAVE\ CLR}$ (B)	L o.c.	Reset bus slaves. Active with $\overline{POC}$, may be generated externally
55	$\overline{TMA_0}$ (M)	L o.c.	TM priority bit 0
56	$\overline{TMA_1}$ (M)	L o.c.	TM priority bit 1
57	$\overline{TMA_2}$ (M)	L o.c.	TM priority bit 2
58	$\overline{sXTRQ}$ (M)	L	Requests 16-bit slaves to assert $\overline{SIXTN}$
59	A_{19} (M)	H	Extended address bit 19
60	$\overline{SIXTN}$ (S)	L o.c.	Generated by 16-bit slaves in response to 16-bit request signal $\overline{sXTRQ}$
61	A_{20} (M)	H	Extended address bit 20
62	A_{21} (M)	H	Extended address bit 21
63	A_{22} (M)	H	Extended address bit 22
64	A_{23} (M)	H	Extended address bit 23
65	NDEF		Not to be defined
66	NDEF		Not to be defined
67	$\overline{PHANTOM}$ (M/S)	L o.c.	Disables normal slave devices and enables phantom slaves
68	MWRT (B)	H	$\overline{pWR}$ −sOUT (logic equation) must follow $\overline{pWR}$ by ≤30ns
69	RFU		Reserved for future use
70	0V (B)		Common with pin 100
71	RFU		Reserved for future use
72	RDY (S)	H o.c.	See pin 3
73	$\overline{INT}$ (S)	L o.c	Primary interrupt request bus signal
74	$\overline{HOLD}$ (M)	L o.c.	Used with pHLDA to coordinate bus master transfer operations
75	$\overline{RESET}$ (B)	L o.c.	Reset bus master devices. Active with POC, mav be external
76	pSYNC (M)	H	Identifies BS1
77	$\overline{pWR}$ (M)	L	Valid data on DO bus or databus
78	pDBIN (M)	H	Requests data on DI bus or data bus from currently addressed S
79	A_0 (M)	H	Address bit 0 (least significant)
80	A_1 (M)	H	Address bit 1
81	A_2 (M)	H	Address bit 2
82	A_6 (M)	H	Address bit 6
83	A_7 (M)	H	Address bit 7
84	A_8 (M)	H	Address bit 8
85	A_{13} (M)	H	Address bit 13
86	A_{14} (M)	H	Address bit 14
87	A_{11} (M)	H	Address bit 11
88	DO_2 (M) ED_2 (M/S)	H	Data out bit 2, bidirectional even data bit 2
89	DO_3 (M) ED_3 (M/S)	H	Data out bit 3 even data bit 3
90	DO_7 (M) ED_7 (M/S)	H	Data out bit 7 even data bit 7
91	DI_4 (S) OD_4 (M/S)	H	Data in bit 4 odd data bit 4
92	DI_5 (S) OD_5 (M/S)	H	Data in bit 5 odd data bit 5
93	DI_6 (S) OD_6 (M/S)	H	Data in bit 6 odd data bit 6
94	DI_1 (S) OD_1 (M/S)	H	Data in bit 1 odd data bit 1
95	DI_0 (S) OD_0 (M/S)	H	Data in bit 0 (least sig) odd data bit 0
96	sINTA (M)	H	Identifies bus input cycles that may follow an accepted interrupt request presented on INT
97	$\overline{sWO}$ (M)	L	Identifies bus cycle which transfers data from bus M to S
98	$\overline{ERROR}$ (S)	L o.c.	Signifies error condition during present bus cycle
99	$\overline{POC}$ (B)	L	Power-on clear signal for all bus devices; must stay low for 10ms min
100	0V (B)		System ground

B backplane, S slave, M master, TM temporary master

Each S100 circuit board measures 10 by 5.3in overall, and plugs into a 100-pin edge connector (50 pins per row) on a motherboard. An offset ensures that boards cannot be inserted wrong way round. The bus supplies unregulated voltage to the boards which therefore carry their own power regulators. This arrangement reduces noise coupling between modules.

One change brought about by the IEEE standard is to allocate to all S100 cards the status of bus master or bus slave. A master is a device, such as a processor, that controls the bus and a slave is a peripheral or block of memory that is controlled. The bus allows for an elaboration whereby, while there is a single permanent bus master, there may also be up to 16 temporary bus masters. The temporary bus masters are given control on request according to a priority system that is arbitrated by the permanent master. This architecture gives flexible multi-user, multi-processor capability.

The temporary master is typically a device such as a disc controller or secondary processor, and obtains access to the bus under a temporary master access (TMA) system. To request, a t.m. signals its priority on one of four arbitration lines. Unless it has to defer to a higher priority user already on the line, the t.m. wins control of the bus, and may then perform any type of cycle (not just a memory cycle).

Until the IEEE revision, memory slaves used to respond only to 16 address bits, giving the system a total capacity of 64Kbyte. The address bus has, however, been extended by eight lines, increasing the memory capacity of the system to 16Mbyte. Input/output slaves used to respond to only eight address bits, giving a total of 256 i/o port locations. Now 16 address lines may be used, allowing up to 64K i/o ports.

Another IEEE change has been to give S100 the ability to operate with eight-bit, or 16-bit processors, or both. For eight-bit transfers, one bus line (the data out or DO bus) carries data from master to a slave and another (data in or DI) carries data from slave to master. A 16-bit transfer is organised by making both these buses bidirectional instead of unidirectional. Data can flow both in and out, depending on the type of cycle in progress. Two lines, '16 request' and '16 acknowledge', had to be added to allow for this.

The committee decided that a phantom line could be used to disable memory slaves for both read and write cycles, and specified the timing. TMA cycle timing has been more closely specified to ensure that arbitration and transfer take place in a 'glitch-free' manner. Another IEEE enhancement has been to allocate eight lines for an interrupt controller slave. This can arbitrate the priorities of interrupting devices.

Advantages

S100 offers major advantages. It is processor and manufacturer independent and can accept 8-bit c.p.us such as the 8080A, 8085, Z80, 2650, 6502, 6800, 6802 and 6809 plus 16-bit processors like the 8086, LST-11, 9900, 8088, Z8000 and 68000. There is a matching array of operating systems – CP/M, Turbodos, MS-dos, NS-dos, DP-cos, Unix, etc – and all the major computer languages are catered for. S100 is powerful; no other microcomputer system has direct addressing of up to 16Mbytes of memory, 64K i/o ports, up to ten vectored interrupt lines, up to 16 masters with priority and up to 23 plug-in slots.

Hardware and software developers prefer S100 because the latest technology seems to appear on it first. Every major new processor has been available on the bus before it has been ready for other systems. CP/M first appeared on S100, as did floppy discs. While it is true that S100 systems might not have the lowest hardware costs, the true economy lies in the speeding up of development and manufacture.

In one example, a contracting company had just a few months to construct and instal a prototype data handling and display system. S100 was chosen as the basis because of the immediate availability of modules required – backplane, processor, 64K memory, disc controller and drives, colour display controller and extensive i/o to host mainframe computers. Numerous assemblers for the Z80 processor were available so that software work could start at once. Using this approach with S100, the system was completed from concept to commissioning in less than six months, and is now being evaluated by the MoD as part of an air defence network. The contractor is secure in the knowledge that any system extensions ordered later can also be S100-based, giving good system integration and economy.

The number of S100 building blocks is steadily growing and the blocks themselves becoming more capable. Whereas a year or so ago a system may have had separate processor, i/o disc controller and four static ram cards, the same functions can now be realised on one or two cards. And a currently popular configuration of Z80 micro-running CP/M with a separate memory up to 64Kbytes may soon give way to a recently introduced package combining Z80A with hardware floating point processor, interrupt controller, counter timer, two serial i/o ports – typically for a v.d.u. or printer – and 128K by 9 bit parity ram, all on a single card. Other cards have 16-bit processors or eight and 16-bit dual processors for users wanting to start with eight bits and up-grade later. Standard 64K memory will eventually be complemented by 128K, 256K and even 1M cards. S100 bubble memory is available for special application and hard disc storage is a common addition to conventional 5¼ or 8 in floppy discs.

Users are not limited to American cards; British manufacturers are producing cards that rival and surpass longer established American products, increasing the choice for everyone.

S100 is, by its nature, 'futureproof' in that improvements in technology such as those outlined regularly increase the appeal and benefits of the system and will continue to do so. The new standard provides immense scope for future development and is likely to prove as much a shot in the arm to the burgeoning S100 industry as to users.

Problem solving

Finally, an example known personally to the author illustrates how S100 can be used to solve problems.

When the BBC wanted a caption generator able to produce workman-like captions for evening programme summaries on a new cable vision service, it found the bespoke generators already on the market too sophisticated and expensive. They also needed specially trained people to operate them whereas the Corporation wanted a simple-to-operate device suitable for clerical staff.

An S100 caption generator provided the answer. A Z80 processor with 32K of ram and disc drive permit synchronization to an external video signal for subtitling and caption generation. Line and field are synchronized with an on-board sync generator. The card features 75-ohm line drivers providing an RGB output and CCIR levels, and automatic interlace selection.

This S100-based system can be expanded simply whenever a requirement arises. Two logical developments would be the addition of a further ram card to permit automatic unattended cycling of captions, and a single-card modem allowing the system to download captions from other BBC departments via Prestel. An electronic time and date display could be added accurate to one second per month and allowing for leap years. A further display card and slave processor would give multi-user capability. The BBC unit as it currently exists has proved inexpensive, effective and easy to use, providing good studio, roll-free, teletext-style captions. Software to allow teletext pages to be created was written straight from keyboard, making no demands on disc storage capacity.

A similar requirement later arose with the Norwegian Broadcasting Authority. The Norwegians heard of the unit the BBC were using, recognised studio sync as the key, and came to the UK to buy the same card. In the end they bought a full S100 system, completed with peripheral drives and interfaces: eight sub-titling units cost no more than a single highly specialized dedicated device designed to do the same job. If they wished the Norwegian could now increase their storage capacity 100-fold by adding another card and substituting a hard disc drive for the present floppy. They will in any case add a fast serial and parallel communications card permitting communication with a mainframe computer for the overall control of tv programming content involving subtitles.

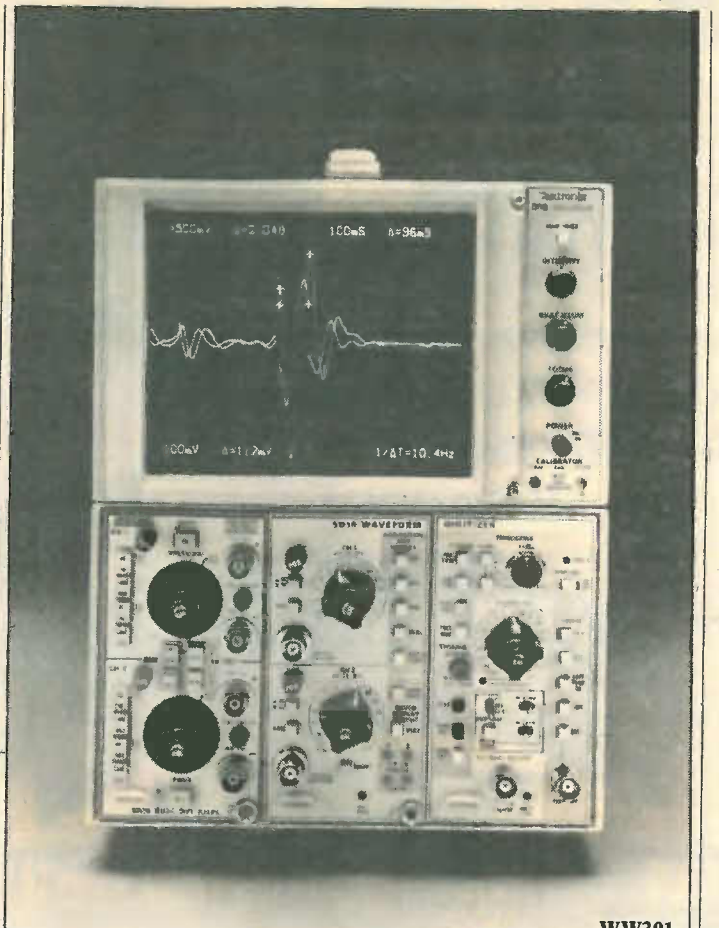
Without S100, the options would be impossible or expensive, and it is this ability of S100 to accommodate evolution without great expense which is its greatest strength. At last we have a powerful, practical and *standard* databus which is well backed and can be adopted with confidence.

WW

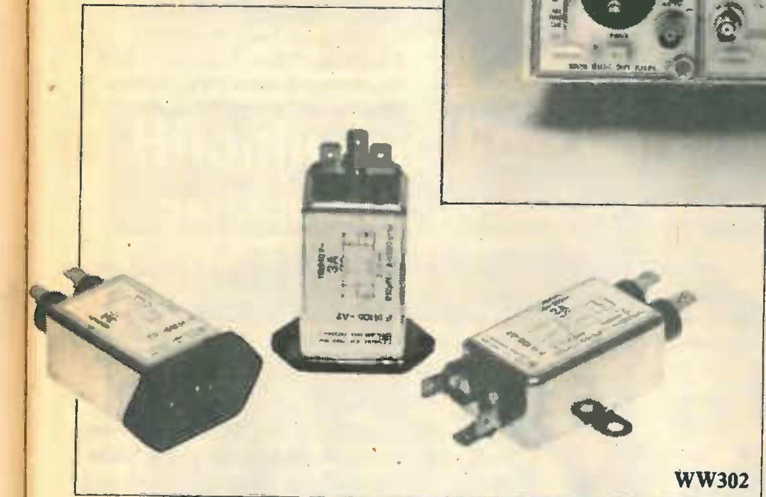
NEW PRODUCTS

Scope for colour

Addition of colour to an oscilloscope display has been made possible with the use of a liquid crystal colour shutter. The display has many inherent advantages over a shadow mask colour c.r.t.; it is much cheaper to produce, has no convergence problems, and the only limit to resolution is the spot size. But there are also limitations; only two colours, cyan and orange, are available in addition to the neutral white. They are arranged so that the upper trace is cyan, the lower trace is orange. Alphanumeric readouts use the same colours as the traces while axes and time measurements appear in neutral. The system is to be applied to the whole 5000 range of Tektronix oscilloscopes. When fitted with the 5D10 waveform digitizer they become digital storage oscilloscopes. The 5D10 provides the switching signal to the colour shutter. Tektronix UK Ltd, PO Box 69, Harpenden, Herts AL5 4UP.
WW301



WW301



WW302

Mains r.f. filters

A range of r.f. supression filters comes from Iskra. They protect mains-powered equipment from mains r.f. interference. They incorporate series inductors and parallel capacitors within the screened metal housings to give attenuation greater than 40dB over the frequency range 750kHz to over 30MHz. Three versions have differing r.f. and electrical characteristics; all are rated at 240V a.c. 50Hz, and operate over a wide range of temperatures. Iskra Ltd, Redlands, Coulsdon, Surrey CR3 2HT.
WW302

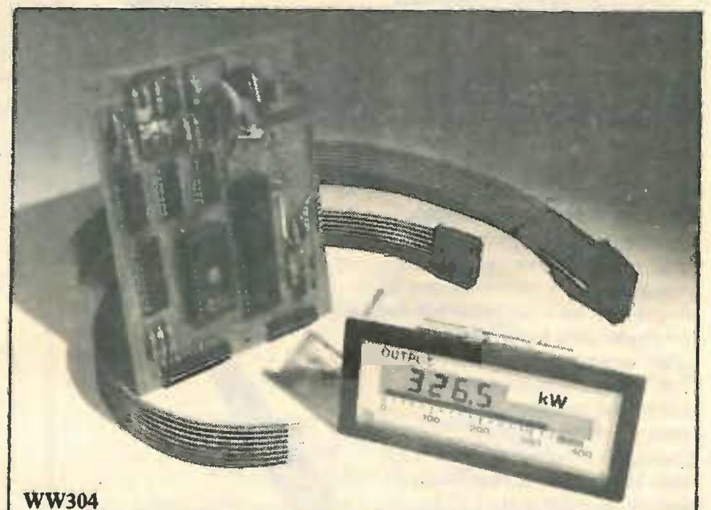
68000 on a board

A single-board computer incorporating the 16-bit 68000 processor has been produced by Apollo Software. The processor runs at 10MHz and has 17 internal 32-bit registers and a 24-bit program counter. The standard board comes with a comprehensive monitor on eprom which provides full debug facilities, single step and trace, down line loader, and a programming handler. Also on the board is 4K of ram (expandable to 16K), the 16K eprom is expandable to 32K, a 24-line parallel interface and an RS232C interface with a wide range of transmission rates. An optional plug-in eprom programmer board can program 2764 and 27128 eproms with code from the computer card, or downloaded from a host computer. Apollo also offers a cross assembler for Z80-based computers available in disc format for use with CP/M or with cassette interface for the Sharp MZ range of computers.

A complete 68000 development system consisting of a host Z80 computer, cross assembler, 68000 c.p.u. board and an eprom programmer can be bought for around £1000. Apollo Software, Bucklebury Alley, Cold Ash, Newbury, Berks RG16 9NN.
WW303

A and D on same meter

Shown at Internepcon in Brighton last month, Sifam are claiming a 'world's first' for their combined digital and analogue panel meter. Resembling a conventional l.c.d. digital meter, it also incorporates a 'trend' bar, displayed beneath the digital read-out, which expands or contracts in proportion to the reading. Incorporating a microprocessor, the meter can be programmed to serve as a multimeter covering several different measurement functions or ranges. One sector of the l.c.d. can display the function or range in use. It may also be programmed as a remote monitor to initiate control or alarm functions at pre-set low or high limits. Sifam Ltd, Woodland Road, Torquay, Devon.
WW304



WW304

Signals for CD testing

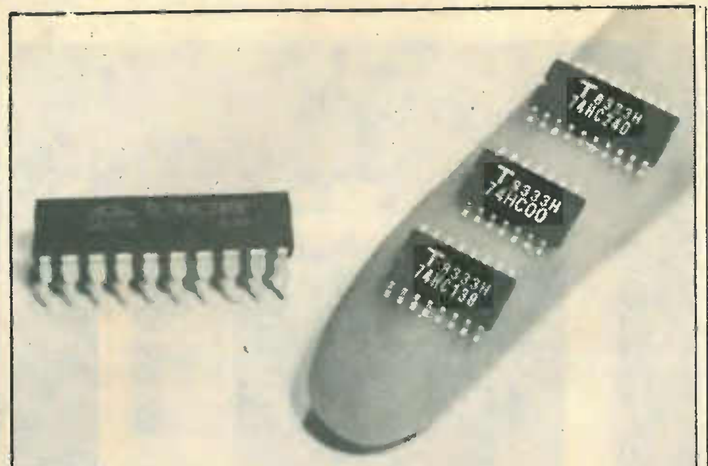
The compact disc has engendered a whole range of equipment that needs to be tested and serviced. The Kenwood Compact Disc Encoder generates a signal equivalent to that produced from

the laser pick-up of a CD player with code formats conforming to CD standards. Nine audio signals are generated internally and are used to produce five test frequencies in a variety of waveforms. Error detection can be tested by inserting externally generated tone bursts. Subcodes can be used to give any test pattern required. The p.c.m. output is provided at t.t.l. level as well as r.f. House of Instruments, Clifton Chambers, 62 High Street, Saffron Walden, Essex CB10 1EE.
WW305

NEW PRODUCTS

Cmos logic in small Packages

Thirty of the 74-series logic components have been produced in small flat packages suitable for surface mounting (see also News). The package occupies about half the space of conventional i.cs on a p.c.b. and are less than half the thickness and a fifth of the weight. The Toshiba logic packs are made in a 'New HS C^2MOS' which is claimed to be 20 to 30 times as fast as regular cmos. This, combined with the small size of the package which makes p.c.b. track lengths much shorter, can lead to both very high speed and accuracy of operation, says Toshiba. Toshiba UK Ltd, Frimley Road, Frimley, Camberley, Surrey WV5 8AQ.
WW306



WW306

TV test chart

For the instant testing of tv cameras and ancillary equipment almost anywhere, Crow of Reading have produced a double test chart with the BBC 62P colour bar chart and a nine-step log reflectance grey scale reflectance chart. They are mounted together in a folder and incorporate a black matt screen to cover the colour chart when the grey scale is in use. When folded the charts are sealed against light and dirt and fit into a nylon carrying case. The colour chart devised by the BBC research department with W. R. Royle and Sons uses specially developed pigments which give a high saturation colour image. Crow of Reading Ltd, PO Box 36, Reading, Berks RG1 2NB.
WW307

WW307

Photodiode for micron waves

A photodiode made of a compound of indium, gallium, arsenic and phosphorus is sensitive to light in the wavelength range 1 to 1.5 μm and has a maximum quantum efficiency of about 70%. Developed by Hitachi, the HR1101 is thought to be of particular use in long-distance fibre optic communications because at these wavelengths the transmission losses along an optical fibre are known to be minimum. Up to now, avalanche photodiodes have been used but the new diodes offer higher speed, higher sensitivity, one tenth of the 'dark' current and between a quarter and an eighth of the operation voltage. Hitachi Electronics Components (UK) Ltd, Hitec House, 231 Station Road, Harrow, Middlesex HA1 2XL.
WW308

WW310

Cross-compiler for software

When a program has been developed for use with a particular processor it can be difficult to translate it for use on other processors. Not so, if the software is developed on a Codata 3300 running Unix as it can be used on the 8080, 8085, 8086, Z80, 6502, 6809 and TMS7000 and other processors. The cross-compiler is based around the C-language, which provides high-level commands and structures while manipulating data normally associated with low-level languages. C enables applications software to be rapidly developed on the Codata and the cross compilers can subsequently be used to generate the native code for the processor to be used, without modification. If required a Systems interface library can give access to the commands of a variety of operating systems, such as CP/M, VAX/VMS and RSX-11. Programmers who would prefer to use Pascal can have their source code translated into C and thence into the various processor-specific codes. Translators from Fortran and Basic are being developed. Cambridge Micro Computers Ltd, Cambridge Science Park, Milton Road, Cambridge CB4 4BN.
WW309

Optical power meter

A hand-held small, lightweight power meter for light measurement could be useful for taking readings in awkward places. The Anritsu ML96A is just such a meter with autoranging and switching between Watt and dBm displays. The meter uses different sensors to cover wavelengths from 0.4 to 1.8μm with a sensitivity from −60dBm to 10dBm. It has an accuracy of 5%. The meter was designed for use in research and development, particularly in the areas of optical communications, video and audio digital discs. The unit comes complete with internal rechargeable batteries, capable of operating for 20 hours, and a battery charger unit. Anritsu Europe Ltd, Thistle Road, Windmill Trading Estate, Luton, Beds LU1 3XJ.
WW310

If you would like more information on any of the items featured here, enter the appropriate WW reference number(s) on the mauve reply-paid card bound in this issue. Overseas cards require a stamp.

HART

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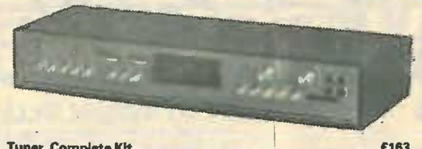

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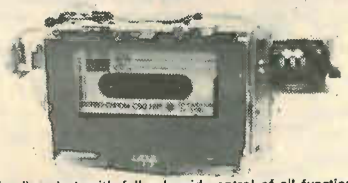

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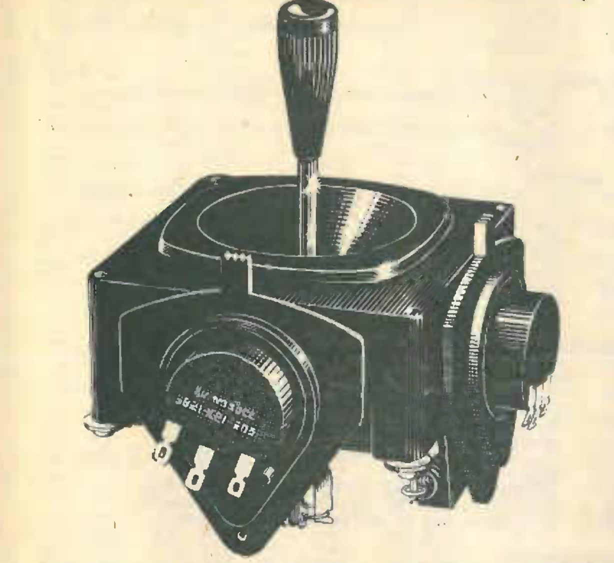

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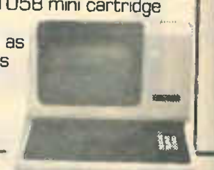

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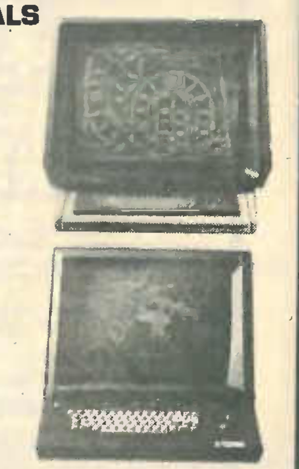

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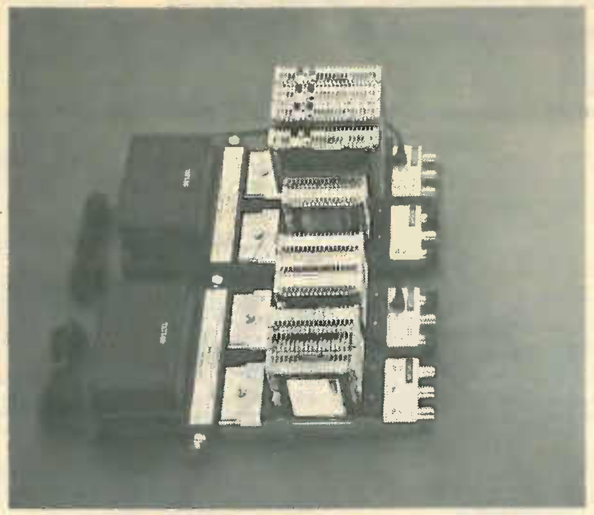

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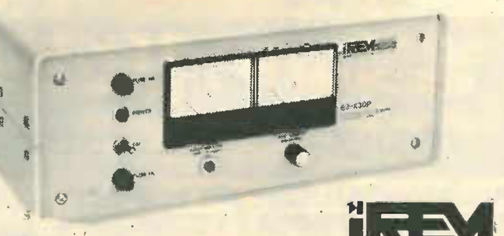

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A1065	1.40
A2293	8.60
A2900	13.75
AR8	0.75
ARP3	0.70
ATP4	0.60
B12H	3.90
CY31	1.40
DAF96	0.70
DET22	28.50
DF96	0.70
DH76	0.75
DL92	0.60
DY86/87	0.65
DY802	0.70
E92CC	2.80
E180F	7.70
E182CC	6.25
EA76	2.25
EABC80	0.80
EB91	0.60
EBC33	1.15
EBC90	0.90
EBF80	0.60
EBF83	0.60
EBF89	0.80
EC52	0.65
EC91	4.40
EC92	0.85
ECC81	0.85
ECC82	0.60
ECC83	0.85
ECC84	0.60
ECC85	0.60
ECC88	0.80
ECC189	0.95
ECC804	0.90
ECF80	0.85
ECF82	0.65
ECF801	1.05
ECH34	2.25
ECH42	1.20
ECH81	0.70
ECH84	0.80
ECL80	0.70
ECL82	0.75
ECL85	0.80
ECL86	0.90
EF37A	2.15
EF39	1.25
EF80	0.85
EF83	1.75
EF85	0.60
EF86	0.75

Valve	£
EF89	1.05
EF91	1.50
EF92	2.90
EF95	0.65
EF96	0.60
EF183	0.80
EF184	0.80
EF812	0.75
EFL200	1.85
EH90	0.85
EL32	1.10
EL34	1.80
	2.90*
EL37	5.20
EL82	0.70
EL84	0.60
EL86	0.95
EL90	1.00
EL91	4.20
EL95	0.80
EL504	1.70
EL803	5.90
EL509	3.95
EL821	8.20
EL822	3.95
ELL80(SE)	2.80
EM80	0.85
EM87	1.30
EY51	0.95
EY81	0.65
EY86/87	0.60
EY88	0.65
EZ80	0.70
EZ81	0.70
GM4	5.90
GY501	1.30
GZ32	1.05
GZ33	4.20
GZ34	2.75
GZ37	3.95
KT86	7.80
	11.20*
KT88	10.50
	13.80*
MH4	2.50
ML6	2.50
N78	9.90
OA2	0.70
OB2	0.80
PCL82	0.95
PCL84	0.90
PCL86	0.75
PCL805/85	0.95
PD500/510	4.30

Valve	£
PFL200	1.10
	2.60*
PL36	1.10
PL81	0.85
PL82	0.70
PL83	0.60
PL84	0.80
PL504	1.00
PL508	2.40
PL509	5.65
PL519	5.80
PL802(SE)	2.95
PY80	0.70
PY81/800	0.85
PY82	0.65
PY88	0.60
PY500A	2.10
QQV03/10	3.20
	7.50*
QQV03-20A	21.50
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QQV06/40A	19.50
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SP61	1.80
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UBC41	1.20
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UBF80	0.70
UBF89	0.70
UCC84	0.85
UCC85	0.70
UCF80	1.30
UCH42	1.65
UCH81	0.75
UCL82	0.95
UF41	1.35
UF80	0.95
UF85	0.95
UL84	0.95
UM80	0.90
UM84	0.70
UY82	0.70
UY85	0.85
VR105/30	1.25
VR150/30	1.35
X66	0.95
X61M	1.70
Z759	19.00
Z749	0.75

Valve	£
Z800U	3.45
Z801U	3.75
Z803U	18.00
Z900T	2.45
1A3	0.85
1L4	0.50
1R5	0.60
1S4	0.45
1S5	0.45
1T4	0.45
1U4	0.80
1X2B	1.40
2X2A	2.50
3A4	0.70
3AT2	2.40
3B28	12.00
	19.50*
3D6	0.50
3D22	23.00
3E29	19.00
3S4	0.60
4B32	18.25
5R4GY	1.80
5U4G	0.75
5V4G	0.75
5Y3GT	0.95
5Z3	1.50
5Z4G	0.75
5Z4GT	1.05
6/30L2	0.90
6AB7	0.75
6AC7	1.15
6AG5	0.60
6AH6	1.15
6AK5	0.65
6AK8	0.60
6AL5	0.60
6AL5W	0.85
6AM5	4.20
6AM6	1.50
6AN8A	2.50
6AQ4	3.40
6AQ5	1.00
6AQ5W	1.80
6AS6	1.15
6AT6	0.90
6AU6	0.60
6AV6	0.85
6AX4GT	1.30
6AX5GT	1.30
6BA6	0.55
6BE6	0.60
6BG6G	1.60
6BJ6	1.30

Valve	£
6BQ7A	0.85
6BR7	4.80
6BW6	6.20
6BW7	1.80
6C4	0.50
6C6	0.55
6CH6	8.20
6CL6	2.75
6CW4	8.50
6CX8	3.80
6CY5	1.15
6D6	0.70
6F6	1.60
6F6GB	1.10
6F7	2.80
6F8G	0.85
6F12	1.50
6F14	1.15
6F15	1.30
6F17	3.20
6F23	0.75
6F24	1.75
6F33	10.50
6FH8	12.50
6GA8	1.95
6GH8A	1.95
6H6	1.60
6JU6	5.85
6J4	1.35
6J4WA	2.00
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6J5GT	0.90
6J6	0.65
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6K7	0.80
6KD6	4.50
6L6M	2.80
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6L6GT	1.25
6L18	0.70
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6Q7G	1.30
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6SK7	0.95
6SL7GT	0.85
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6SQ7	0.95
6V6G	1.50
6V6GT	0.95
6X4	0.95
6X5GT	0.65
6Y6G	0.90

Valve	£
6Z4	0.70
9D6	2.90
11E2	19.50
12A6	0.70
12AT6	0.70
12AT7	0.85
12AU7	0.60
12AV6	0.95
12AX7	0.65
12BA6	0.90
12BE6	1.25
12BH7	1.95
12E1	18.95
12J5GT	0.55
12K7GT	0.70
12K8GT	0.80
12Q7GT	0.60
12SC7	0.65
12SH7	0.65
12SJ7	0.70
12SQ7	1.45
12SQ7GT	0.85
12Y4	0.70
13D3	2.80
13D5	0.90
19AQ5	0.85
19G3	11.50
19G6	8.50
19H5	39.55
20D1	0.80
20E1	1.30
20P1	0.85
25L6GT	0.95
25Z4G	0.75
35W4	0.80
85A2	1.40
	2.55*
807	1.90
813	19.32
	68.50*
829B	16.00
832A	8.90
866A	3.80
866E	6.25
931A	13.80
954	1.20
955	1.20
956	1.20
5763	4.80
6060	1.95
6080	5.30
6146	5.80
6146B	5.80
6360	2.85

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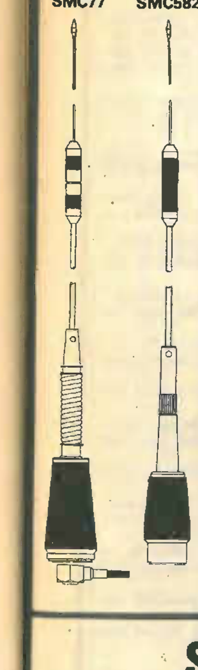

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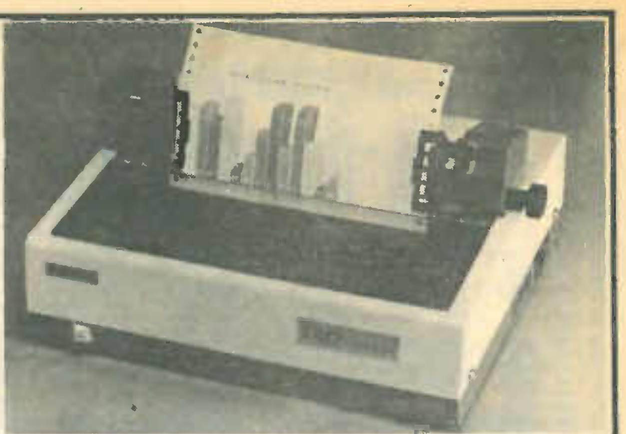

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Marconi Autotest Type OE 1483 Auto Testing Equipment for the production testing of radio telephone equipment. The equipment consists of a general-purpose controller type OA 1444a/25 and three instrumentation racks type OA 1445/28, –/29 and –/30. Units housed in the three racks are as follows:

OA 1445/28 – Modulation Meter, TF 2301, R.M.S. AC/DC Converter TF 2607, Power Meter OA 7024/4, Access Panel TK 7022/1, Power Connections Panel TK 7055, Power Supply Programmer TM 9774, DC Power Supply No. 1 TM9780/4, Attenuator Bird model 8322, LF Generator Wavetek 155.

OA 1445/29 – Frequency Selection Unit TK 7047, Peripheral Logic Unit TM 9765/5, Random Access Switch TM 9770, UHF Attenuator TF 2168, DVM TM 9767 (modified Solartron 1420.2), Synthesizer Rohde & Schwarz ND 100 M, Modulator Rohde & Schwarz MAF, Synthesizer Rohde & Schwarz SMDV.

OA 1445/30 – DVM. Interface Unit TM 9764, Limits Comparator TF 2412/2, Printer TM 9768/1, Power Supply Programmer No. 2 TM 9774, DC Power Supply TM 9780/16, DC Power Supply Hewlett Packard HP 6268A.

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Pye Olympic M201 AM High Band, complete but less mike, speaker and cradle. With circuit diagrams. **£40 plus VAT.**

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Computer Grade Electrolytic Capacitors, screw terminals, 25000 mfd., 33 volt, brand new, **£1 each plus 50p. p.p. plus VAT.**

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1W E24	6p
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1nF to 6nF	7p
8nF to 47nF	8p
56nF to 150nF	10p

100V

100nF to 150nF	11p
180nF to 270nF	14p
330nF to 390nF	20p
470nF to 560nF	26p

uFd	V	
2.2	100	11p
2.2	350	30p
3.3	25	10p
3.3	40	11p
3.3	63	12p
4.7	16	8p
4.7	25	9p
4.7	40	11p
4.7	63	12p
4.7	100	14p
10	25	8p
10	40	12p
10	63	14p
10	100	16p
10	350	55p
22	25	11p
22	40	14p
22	63	16p
22	100	21p
47	25	14p
47	40	17p
47	63	28p
47	100	28p
100	16	14p
100	25	16p
100	40	22p
100	63	25p
100	100	30p
220	10	16p
220	16	17p
220	25	22p
220	40	25p
220	63	30p
220	100	40p
470	16	22p
470	25	28p
470	40	33p
470	63	43p
470	100	60p
1000	16	30p
1000	25	38p
1000	40	46p
1000	63	65p
2000	16	40p
2200	25	63p
2200	40	70p
2200	63	134p
4700	16	75p
4700	25	89p

RADIALS (PCB wires one end). Matsushita only.

uFd	V	
10	16	6p
22	10	6p
22	16	7p
47	10	7p
47	16	8p
100	10	9p
100	16	10p
220	10	11p
220	16	12p
470	10	17p
470	16	18p
1000	10	20p
1000	16	24p
2200	10	34p
2200	16	44p
3300	10	50p
3300	16	65p
4700	10	65p
4700	16	95p

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All 240V Primary 6.0 6V, 9.0 9V, 12.0 12V, 15.0 15V

100mA	95p
1A	2.65
20.0 20V 1.25A	2.65
12.0 12V 50VA	5.26
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100 × 160	2.10
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203 × 114	2.40
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100 × 160	2.20
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2N2907	25p	40871	1.00	BC548B	14p
2N2907A	28p	40872	1.00	BC548C	15p
2N2920	8.50	AC125	49p	BC549	13p
2N2923	25p	AC126	32p	BC549B	14p
2N2924	15p	AC127	32p	BC549C	15p
2N2925	15p	AC128	35p	BC550	15p
2N2926	10p	AC132	68p	BC550C	25p
2N3053	27p	AC141K	28p	BC557	15p
2N3054	56p	AC142K	28p	BC557A	16p
2N3055	60p	AC151	51p	BC557B	16p
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2N3250	36p	AC153	55p	BC558A	15p
2N3251	36p	AC153K	64p	BC558B	16p
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2N3440	80p	AC176K	37p	BC559	15p
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2N3442	1.35	AC187K	28p	BC559C	17p
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2N3468	1.00	BC107	10p	BCY70	16p
2N3512	1.06	BC107A	12p	BCY71	16p
2N3653	2.65	BC107B	12p	BCY72	19p
2N3638	66p	BC108	10p	BD131	44p
2N3638A	70p	BC108A	12p	BD132	44p
2N3702	10p	BC108B	12p	BD135	35p
2N3703	10p	BC108C	14p	BD136	35p
2N3704	10p	BC109	10p	BD137	37p
2N3705	10p	BC109B	12p	BD138	37p
2N3706	10p	BC109C	12p	BD139	38p
2N3707	10p	BC140	29p	BD140	38p
2N3708	10p	BC141	37p	BD237	98p
2N3709	10p	BC142	29p	BD238	98p
2N3710	10p	BC143	30p	BD239A	57p
2N3711	10p	BC147	10p	BD239C	64p
2N3712	2.00	BC147A	10p	BD240A	59p
2N3713	1.38	BC147B	10p	BD240C	73p
2N3714	2.98	BC147C	20p	BD241A	61p
2N3715	3.31	BC148	10p	BD241C	67p
2N3716	3.60	BC148A	12p	BD242A	65p
2N3773	1.99	BC148B	13p	BD242C	70p
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2N3820	38p	BC149	10p	BD143C	85p
2N3821	1.84	BC149B	12p	BD244A	82p
2N3822	90p	BC149C	13p	BC244C	1.00
2N3823	45p	BC152	35p	BD245A	1.14
2N3824	1.70	BC153	23p	BD245C	1.30
2N3866	90p	BC154	27p	BD246A	1.20
2N3903	13p	BC157	11p	BD246C	1.50
2N3904	13p	BC157A	12p	BC249A	2.00
2N3905	13p	BC157B	13p	BD249C	2.31
2N3906	13p	BC158	10p	BD250A	2.11
2N4030	75p	BC158A	12p	BD250C	2.46
2N4031	65p	BC158B	13p	BD419	1.29
2N4032	69p	BC159	11p	BD420	1.37
2N4036	63p	BC159A	12p	BD437	88p
2N4037	49p	BC159B	13p	BD438	88p
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2N4347	2.26	BC160	42p	BD440	91p
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2N4401	27p	BC167	10p	BD442	93p
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2N4403	30p	BC167B	13p	BD530	1.30
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2N4427	1.30	BC168C	10p	BD537	80p
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2N4871	55p	BC169B	10p	BD539	80p
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2N4905	2.75	BC178A	24p	BD677	78p
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2N4921	55p	BC182B	13p	BDY55	1.75
2N4922	69p	BC182L	10p	BDY56	1.60
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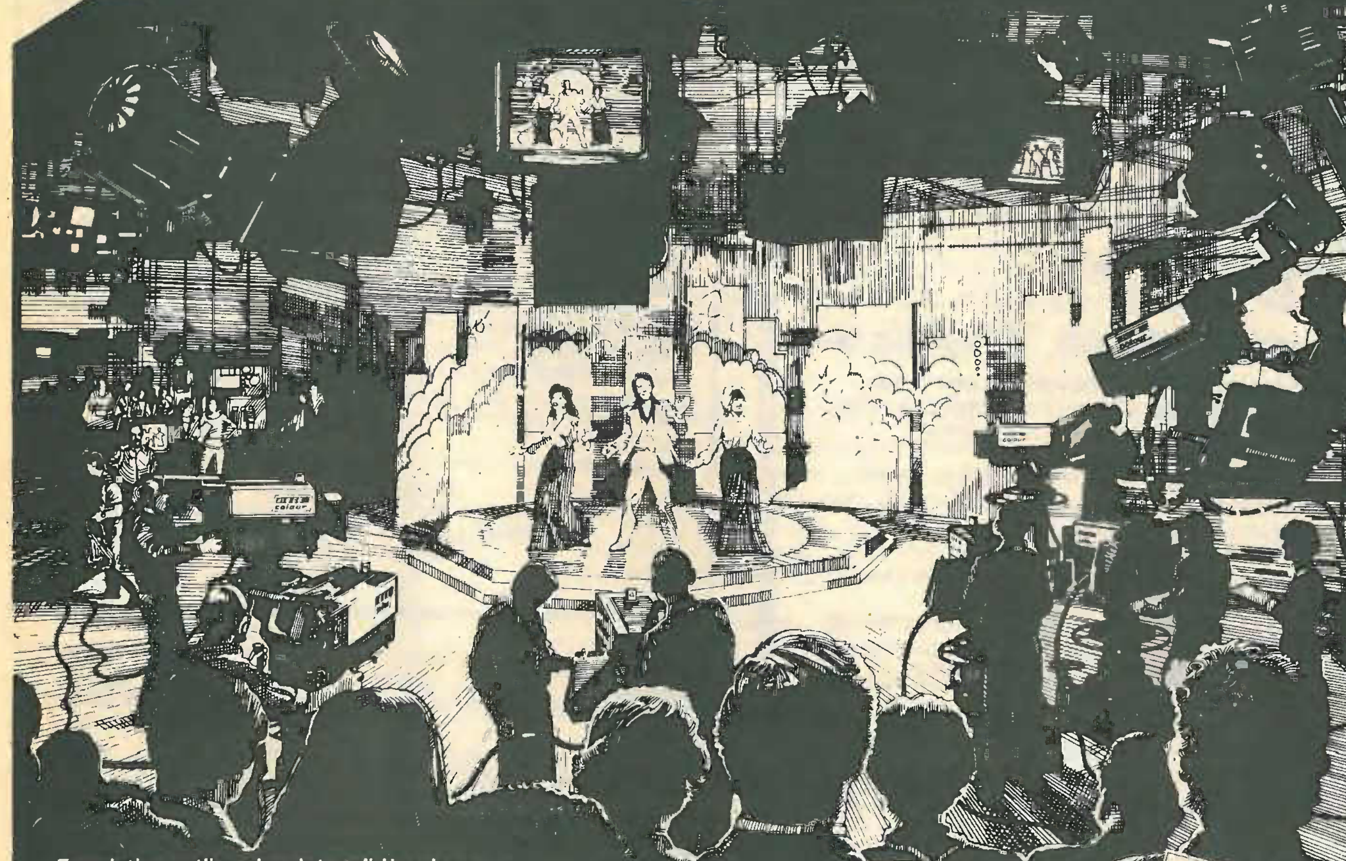

Translating outline plans into solid hardware – tested, debugged and ready-to-run is challenging enough but when these plans involve interfacing several different technologies and producing one totally integrated system, the problems increase a hundredfold.

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We would like to meet people who are interested in gaining experience across a very broad field and learning to apply the experience they have gained in other electronic industries, to the expanding and ever-changing field of broadcast engineering.

We have vacancies for people with a wide range of qualifications and if you have a degree in Electronic Engineering, an HNC, HND, Higher TEC Certificate or Diploma, then why not come along and see what we have to offer. Salaries range initially from a minimum of £8,362 to £10,949 and we would expect most people to be recruited near the top of this range. If you are not promoted in the meantime, annual increments should extend this range to a maximum of £12,327.

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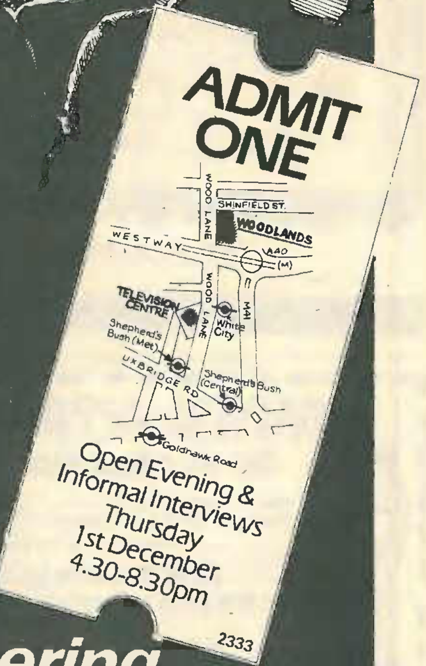
Do come and see us at Woodlands between 4.30pm and 8.30pm on Thursday, 1 December. If you can't come to see us then, telephone Eric Stoves on (01) 743 8000 ext. 2149 and discuss with him the opportunities which are available. Alternatively, you can write for further information and an application form to: Mr. E. Stoves, Studio Capital Projects Dept, BBC, PO Box 2BL, London W1A 2BL (Quote ref. 83E/4127 WW)



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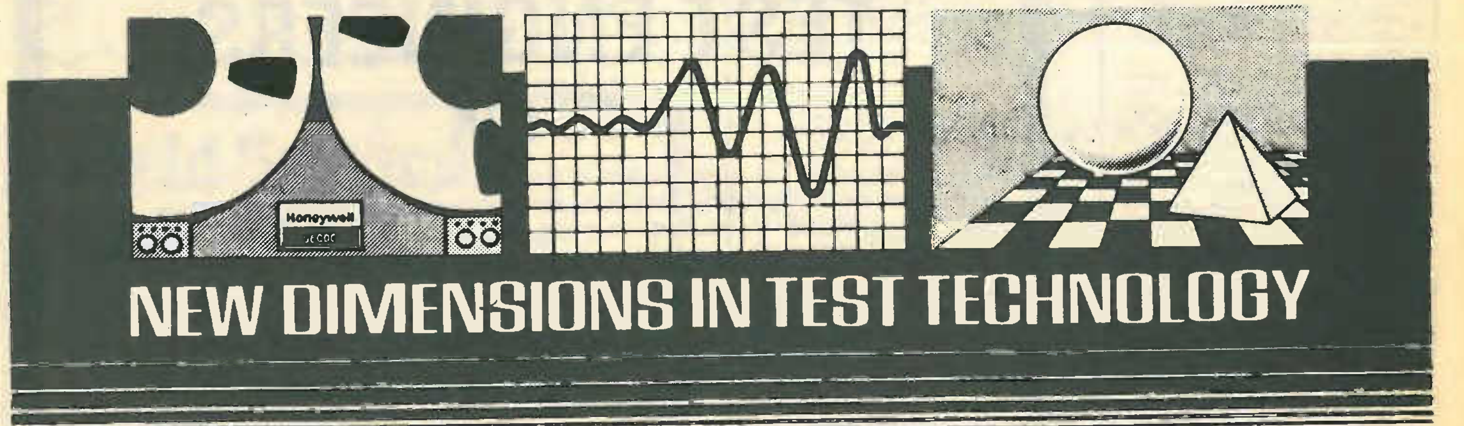

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R. D. GORTON
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Applicants should normally have 4 years' relevant experience (7 years for more senior posts), and must hold one or more of the following:

- ★ ONC in Engineering (with pass in Electrical Engineering 'A');
- ★ ONC in Applied Physics;
- ★ TEC/SCOTEC certificate;
- ★ City & Guilds Telecommunications Technicians Certificate Part II (Course No 271) or Part I plus Maths 'B', telecommunications Principles 'B' and one other subject;
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Ex-Service personnel who have had suitable training and at least 3 years' appropriate service (as Staff Sergeant or equivalent) will also be considered.

Salary: Salary will rise from a minimum of £6,262 p.a. to a maximum of £8,580 p.a. for the Junior Grade and from a minimum of £8,420 p.a. to a maximum of £9,522 p.a. for the Senior Grade. Starting salary in the Junior Grade may be above minimum for those with additional relevant experience.

Relocation assistance may be available.

For an application form please write indicating the position desired to Foreign & Commonwealth Office, Hanslope Park Hanslope, Milton Keynes MK19 7BH, or telephone Milton Keynes (0908) 510444 Ext 232, to be returned by 16th December, 1983. Please quote reference YHU/TT7/83.

FOREIGN AND COMMONWEALTH OFFICE

(2329)

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(2341)

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(2330)

CHANNEL FOUR TELEVISION

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Bristol

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(2345)

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IAL MEDICAL SERVICES RECRUITMENT SERVICES

(2339)

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Ministry of Information
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SITUATIONS VACANT

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DATA GENERAL Micro Nova System comprising MP/200 processor with 64KByte memory, Model 6096 1.26MByte diskette, Model 6101 12.5MByte Winchester disc drive, 4 line synch/asynch terminal multiplexor, Model D200/100 VDU & Model LP2 (6190) 'Dasher' line printer. With RDOS operating system including business Basic. All components are date stamped May/June 1982 by manufacturer. **£3500**

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