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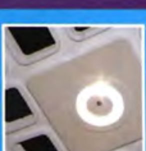

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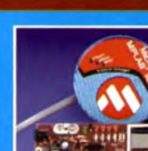

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ELECTRONICS WORLD

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WATCH OUT: COUNTERFEITERS ARE ABOUT

New business is 'in town' and it's running successfully – counterfeiting – making the industry very nervous. Forget smuggling copied fashion goods or counterfeit pharmaceuticals, the organised gangs are onto a new multi-billion dollar craze – counterfeiting electronic components.

And it's not the expensive stuff like semiconductors they are reproducing, but simple, already cheap components – those in the 30-40 pence component value range.

The problem is that some of these 'products' have already entered the authorised value chain. Most of them are so good that it takes a trained eye – and a microscope – to spot the difference between a 'pukka' part and one that is counterfeit.

Electronic components distributors are getting fretful about the issue and this is their fastest growing concern; in fact, it is expected to be the biggest matter for them over the next few years.

The counterfeit gangs are organised and they mostly come from Asia; some 85% of components are counterfeited there, but the rest 15% is a bit closer to home – in Eastern Europe.

In Japan, however, this problem is less pronounced as each manufacturer has its own distributor, so the control of components is tighter. In Europe, however, the trouble is that nobody seems to be doing much about it. Even if a counterfeiting 'offender' is caught, the worse that can happen to them is a 'slap on the wrist'.

The problems is unlikely to go away unless all parties – distributors, OEMs, contract manufacturers, 'gray' channels, buyers and most importantly governments – put their heads together and coordinate their efforts. This is not an easy feat, however, as who is going to be the one responsible of calling on and organising all these parties to get together to prepare a concerted, effective fighting-back method.

To begin with, each party can at least start to do their bit towards it. For example, manufacturers can start to handle their parts of the business in a more controlled way: they'll need to be more careful about what materials they scrap and how they scrap them. They will probably have to track their inventories better too.

Any extra activity will take valuable time and money, so it's no wonder that the industry is getting jittery about it. But, as they say, desperate times call for desperate measures, especially if the industry is to fight this menace successfully.

Svetlana Josifovska
Editor

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ULTRASOUND USED TO REPAIR PUNCTURED LUNGS

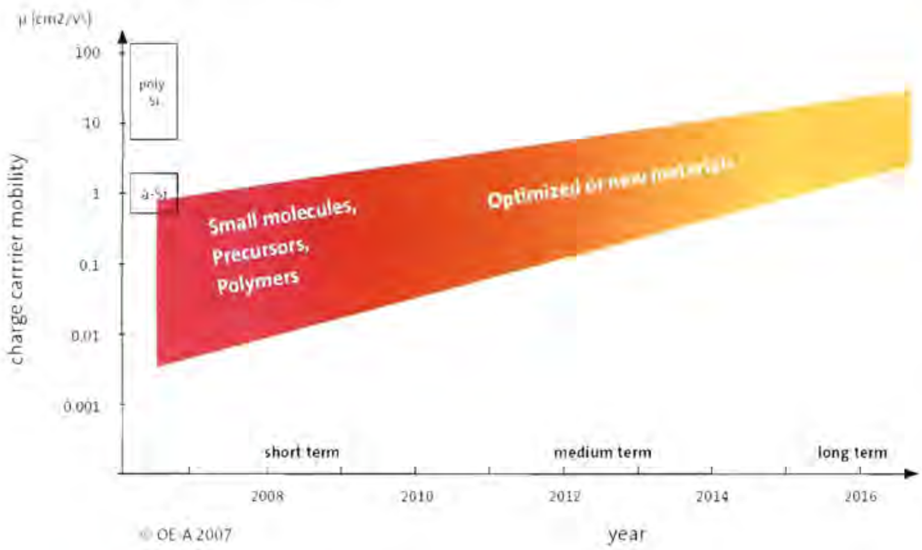
Engineers at the University of Washington are collaborating with doctors at the Harborview Medical Centre to create a Star Trek-like "tricorder" device that uses high-intensity focused ultrasonic waves to seal punctured lungs.

Lenses can be used to focus high intensity ultrasonic beams to a point inside the patient's lungs, which creates a very small, but extremely hot spot. The ultrasonic energy heats the blood cells so that they form a seal over the injury in this 'bloodless surgery' technique. The tissue between the device and the spot being treated does not get hot, as it would with a laser beam.

Thus the beams can penetrate deeply into the body and deliver the energy to the puncture very accurately, so that the leak is sealed in one or two minutes. It is hoped that ultrasonic treatment using frequencies in the range 1-10MHz will be able to replace what is currently a painful and invasive procedure in which a drain must be inserted into the lung.

These trials are believed to be the first experiments on treating lungs with ultrasonic energy and are said to be giving very impressive results, but are still in their early stages.

New Roadmap Announced for Organic Electronics



Forecast improvements of charge carrier mobility in semiconductors for organic electronic applications according to the OE-A roadmap

The second version of the Organic Electronics Association (OE-A) roadmap forecasts that printed electronics will enter the market through 2015 and beyond. It includes seven applications ranging from sensors on radio frequency tags to photovoltaic products.

Organic electronics is a platform technology that will enable multiple applications varying widely in product specifications. The technology is at an early stage, still in transition from the laboratory and prototype work to production, so it is important to achieve agreement on the types of product, processes and materials that will be made available.

"This second roadmap will help the industry, government agencies and scientists to plan and align their R&D activities and product plans," said Wolfgang Mildner, chairman of the OE-A. He added that it will be frequently updated and expanded with the international experts along the value chain.

Organic Electronics is based on the combination of new materials, both organic and inorganic, that are thin, light-weight, flexible and environmentally friendly. It will enable a wide range of electronic components to be produced and integrated directly in low cost reel-to-reel processes. Large area production processes can be used that will open up new fields of application.

Examples of the fields in which the technology is likely to be applied include flexible solar cells, rollable displays, RFID devices, printed batteries and disposable diagnostic devices and games. The first organic electronic products that have already reached the market include flexible lithium polymer batteries, sensors and passive ID cards. Products such as displays with organic TFT backplanes, organic photocells, printed memories and printed RF tags are expected to reach the market place within about a year. Large volumes of all of these products are expected within the next few years.

Improvements in materials, patterning processes and device design are needed to meet future demands. The OE-A is a working group within the German VDMA engineering federation with headquarters in Frankfurt am Main, Germany.

The OE-A was founded in 2004 and now has over 80 companies in Europe, the US and Asia collaborating towards the competitive production infrastructure for organic electronics.

A ZINC BATTERY AGREEMENT SET UP TO HELP HEARING AIDS

Battery maker ReVolt Technology and the hearing aid manufacturer Phonak AG recently signed a collaborative agreement for the development of re-chargeable zinc air batteries for hearing aid applications. Both companies are based in Stäfa, Switzerland.

Zinc is often used in standard non-rechargeable batteries, especially those for medical applications, as it is cheaper, more easily available and perhaps safer than lithium. However, the development of re-chargeable zinc air batteries for hearing aids has proved to be extremely difficult.

The batteries are claimed to have a number of advantages over lithium ion batteries. They can hold their charge for about twice the length of time, they can be produced at prices no greater than lithium ion types and the ignition possibility that occurs with lithium ion cells is avoided.

A design has now been chosen that combines fuel cell technology with a standard battery. It uses zinc oxidation both to produce and store the energy. The battery consists of a negative zinc electrode plus a positive electrode made from a porous structure to catalyse the oxygen reaction. High ionic conductivity is provided between the electrodes by an alkaline electrolyte.

The companies are planning to market the zinc air re-chargeable batteries in late 2009, when they will be included in Phonak hearing aids. Later ReVolt Technology will develop zinc air batteries for various consumer electronics products like laptop computers, mobile phones and digital cameras.

GRAPHENE COULD REPLACE SILICON IN SOME DEVICES

Seven electronics companies announced their support for an industry specification for next-generation removable flash memory cards.

The new specification, Universal Flash Storage (UFS), is being developed by the Jedec standards group. The proposal would create an industry spec for removable memory cards and embedded memory products. The UFS standard is expected to be completed in 2009.

Endorsing the proposed standard are Micron Technology, Nokia, Samsung Electronics, Sony Ericsson, Spansion, STMicroelectronics and Texas Instruments. The companies said UFS would speed access times for flash memories, ease high-speed access to large media files and reduce power consumption in consumer devices. Users currently have a three-minute access time for a 4GB, high-definition movie. The backers said the new standard would reduce that wait to a few seconds.

"Standardisation of flash-based technologies will be crucial in determining how fast storage devices will be able to fully support industry demand for higher densities and faster transmission speeds," said Frankie Roohparvar, vice president of NAND development for Micron Technology.

George Minassian, Spansion vice president, added that the proposed spec "not only provides significantly higher bandwidth, but also supports low latency accesses and is positioned to provide essential infrastructure in future mobile devices".

IN BRIEF

Ofcom in the UK has launched a multi-billion pound auction of airwaves for a new wave of digital services, including more digital TV channels and ultra-fast wireless broadband. Such services could be rolled out over the next decade as radio spectrum is freed up by the digital switchover.
The regulator has packaged the available spectrum into key uses: national digital terrestrial TV in high or standard definition; cognitive radio; high-speed mobile broadband and mobile TV; plus some 25 new local TV stations across the UK.
The regulator has said that the market will decide how the spectrum is used with an open auction.

FREEDOM4 has joined forces with ConnectMK to offer the first UK commercial wireless broadband service using WiMAX technology. In December last year ConnectMK started to provide residents and businesses in the Milton Keynes area with access to FREEDOM4's WiMAX services. Over 1000 people in Milton Keynes have registered interest in joining FREEDOM4's network.
With no BT line required, WiMAX enables broadband to be rapidly installed at customers' premises or homes and offers increased symmetrical broadband delivery. WiMAX service can be offered to those areas where traditional ADSL broadband access is not feasible, giving residents and businesses a cost-effective alternative to access the latest in Internet connectivity.

Frontier Silicon has teamed up with REVO to deliver the world's first radio to combine DAB/DAB+ and Wi-Fi. Called Blik Radiostation and containing Frontier Silicon's Venice 6 multistandard module, it is also the first digital radio on the market to provide plug-and-play reception of both DAB and DAB+ broadcasts.
Venice 6 is the world's first digital module capable of receiving Internet radio via Wi-Fi, DAB/DAB+, FM and music streamed from a network server. Based around Frontier Silicon's Chorus 2 processor, in addition to being able to receive DAB and DAB+, it also streams radio stations and music files in a variety of formats and protocols including MP3, Windows Media Audio (WMA) and Real Audio.

Top Ten Tips

Switch System Optimisation

01. Relay open

In the ideal open relay or switch, the resistance between the contacts is infinite. In reality, there is always some finite resistance value that has to be taken into consideration. The key is to find the magnitude of the open resistance and to determine if it is going to affect the signal passing through the system. There are many different types of switches and each of them has a specification for insulation/isolation resistance. Make sure that the specification is for contact-to-contact resistance in the open state. See Figure 1.

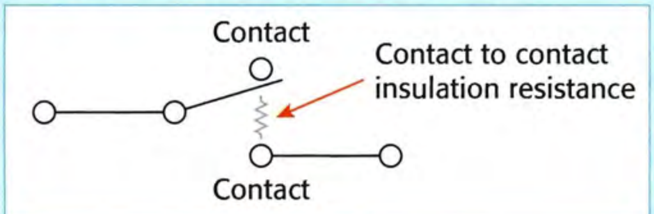


Figure 1

Relay Type	Isolation	Speed[1]	Power
Electromechanical	10^{7}–10^{10} Ω	20–100 ms	10–100 VA
Electromechanical (high frequency)	60–130 dB	20–100 ms	1–120 W
Contactor	10^{6}–10^{9} Ω	100–250 ms	100–4 kVA

***Table 1:** Relay types, resistances, and life cycles*

In general, the higher the resistance in the open state, the less effect on the signal. Most relays have open-state resistance specifications of between 1MΩand 1GΩ, which is usually sufficient for most applications. For example, switching a power supply signal of 5V through a system has little or no effect due to the high open-state resistance. Normally, a power supply has low internal impedance that the high switch impedance does not affect. Table 1 provides examples of different types of relays with different magnitudes of insulation resistance.

02. Relay closed

In the ideal closed relay or switch, there is no resistance between the contacts. Switches in the real world, however, have some resistance, however minute. Even superconductors have some resistance, albeit extremely small. Most contacts have resistance on the order of a few milliohms. Each relay type has different specifications for contact resistance. Most new relays have closed-contact resistance below 0.1Ω. The resistance usually increases with use. Most relays have an end-of-life specification of about 2Ω. Depending on the relay type, this is after millions of cycles of use. Even at such high resistance, the relays can still function, although they may begin to have a greater impact on the signal passing through the switch. See Figure 2.

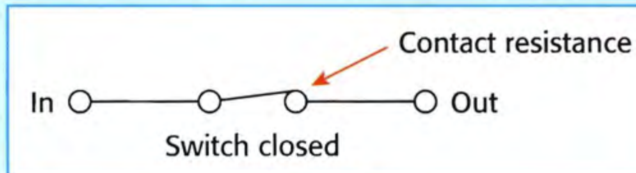


Figure 2

03. Channel-to-channel isolation

Getting crosstalk and signal leakage from adjacent channels can be a tough problem to troubleshoot. It's easier to start out with the proper design and specifications for the correct switching components than to spend precious time troubleshooting an elusive problem. Channel-to-channel isolation is a measure of the electrical isolation of any two adjacent switches. Normally, on a switching or relay card the channels are aligned in order to facilitate the proper voltage spacing and to accommodate the physical dimensions of the switches and other components, such as connectors. The PCB material and spacing could also allow a certain level of isolation between channels. The higher the isolation, the lower the chance of any crosstalk or leakage between channels.

Typical values of channel-to-channel isolation are up to 10GΩ with capacitance of less than 100pF. Still, contact-to-contact resistance must be taken into consideration when designing any switch system. For example, in high-frequency applications, the capacitance becomes

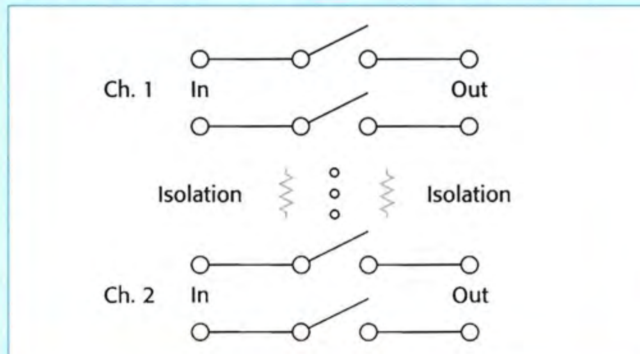


Figure 3

an important consideration. Usually with high frequency applications, the isolation is stated in dB. For instance, 60dB would be an isolation of 1000 to 1 from channel to channel, meaning that 1V on one channel could bleed over and become 1mV on an adjacent channel. The higher the isolation, the better the integrity of the signal passing through the system. See Figure 3.

04. Relay settling time

The settling time is the time it takes for the relay contacts to stop bouncing and make a solid reliable connection. Settling time varies from relay to relay with typical times in the millisecond range. Sometimes relay switching cards have a built-in delay to avoid this phenomenon, while some switching equipment may even have a user programmable delay time.

Some signals take longer to settle, which means that relay contact bounce as well as signal type must be taken into account. If the signal is of extremely high impedance (e.g. very low current), then it may require several seconds or even minutes to settle. Settling time is directly related to the small current charging the cable or stray capacitance in the circuit. The higher the impedance, the lower the current and the more time it takes to settle.

When a relay opens or closes, there is a charge transfer on the order of a few pico Coulombs that causes a current pulse in the circuit. This charge transfer is due to the mechanical release or closure of the contacts, the contact-to-contact capacitance and the stray capacitance between signal and relay drive lines.

Making sure the relay is completely closed and the contacts settled can help ensure the signal will pass with minimal degradation and without added noise that could generate false readings. Some instruments have displays that depict when the relay is closed. However, some relays take several milliseconds to close as the switch bounce settles. You must take this into account. Look at the relay specifications for typical relay settle times.

05. Effect of switching and associated cabling on signal quality

Not using the appropriate cabling for switching signals could degrade signal quality. Each type of signal has some unique unwanted characteristic that you can reduce or eliminate by choosing the appropriate cabling.

In a high-frequency switch system, using a 75Ω coax cable in a 50Ω characteristic impedance system would cause signal reflections and a poor Voltage Standing Wave Ratio (VSWR). Also, using a coax cable in a high magnetic field would help reduce the magnetic field effect, but using shielded twisted-pair cable would be much better. Table 5 provides some examples of signals and appropriate cables.

Signal Type	Unique Parameter	Cable Type
High frequency	Impedance match	e.g. 50Ω to 50Ω
Magnetic field	Magnetic flux	Shielded twisted pair
Low current	Triboelectric effect	Low noise cable (graphite on shield braid)
Low current	Leakage currents	Low noise coax or triax with driven guard
Low voltage	Thermal effect	Copper wires

Table 5: Signal types and appropriate cables

06. Switch element lifecycle implications of hot vs cold switching and scanning rate strategies

Cold switching is defined as opening and closing the switch when no current is flowing. Using cold switching lengthens the contact life of the switch. The carry current is the maximum current that the switch can tolerate once the contacts have been closed and is limited by the cross-sectional area of the path through the switch contacts.

Hot switching is defined as opening and closing the switch when current is flowing or when the signal to be switched is applied. Depending on the switch specifications and the signal passing through, contact life is usually reduced when using hot switching. Switched current is the maximum current that can be handled reliably while opening and closing contacts. Contact material and plating are the primary factors that determine this specification, which is used to determine the life of the switch. If the switched current is too high, the resulting temperature increase and contact arcing will degrade the relay and shorten contact life. In extreme instances, the contacts may weld together.

The rate of the repetitive open and close cycles of the switch also has an affect on the life of the switch. If the switch being used cycles ten times a second for 24 hours a day seven days a week, then it will reach end of life fairly quickly. For example, if a relay life specification is 100,000,000 cycles, which is typical, then at this rate it would reach end of life in about four months.

Ten times in a second is a medium to slow speed for some test systems. Some systems require higher speed and some slower speeds depending on the requirements. So take care when specifying a switch in the test system. Be aware of the switching rate of the system and the life cycle specifications of the relay along with the signals being switched for maximum performance and life of the switches.

07. Non-blocking and blocking matrices

A non-blocking matrix allows simultaneous connections of multiple input/output single paths, up to the full number of matrix inputs. This is the most flexible and most expensive matrix. Although it is possible to close multiple paths, this is only practical in DC testing, such as applying a continuous bias voltage to a number of DUTs.

Impedance considerations preclude closing multiple paths in RF and microwave switching. Given that a switch system is positioned between the measurement instrument and the DUT, matching the impedance levels of all elements in the system is critical. For optimum signal transfer, the output impedance of the source should be equal to the characteristic of the switch, cables and the DUT. Proper impedance matching will improve signal integrity. Refer to Figure 7a.

A blocking matrix allows the connection of a single input to any single output. Therefore, only one signal path is active at any given time. This is somewhat restrictive, but when working with RF and microwave signals, the paths must have impedance matching. Closing several paths at one time could cause reflections and therefore poor VSWRs. This results in loss of signal and power. So a blocking matrix may be restrictive, but most of the time it is necessary for signal quality issues. Refer to Figure 7b.

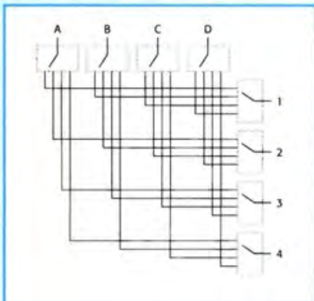


Figure 7a

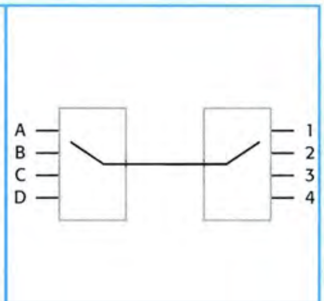


Figure 7b

08. Full or partial matrix

A full or partial matrix allows simultaneous connection of an input to multiple outputs. Switch mainframes would include switching cards where the actual signal switching takes place. Switching cards are normally designed in 1x4 building blocks, meaning one card may have three or four 1x4 switches on them. These can be configured together to obtain a larger matrix, either more rows or more columns or both. But the system would require a power divider at each input and a multiple position switch at the outputs. Again, impedance matching is important. The advantage of matrix configurations includes the absence of unterminated stubs, access to all channels and similar path characteristics. Disadvantages include the need for extensive cabling and the use of many coaxial relays. See Figure 8.

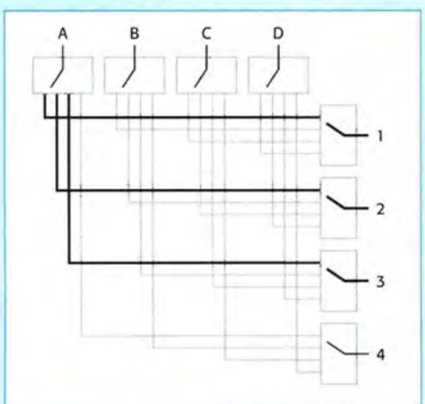


Figure 8

09. Using solid-state switches for fast switching applications

Standard electromechanical relays can switch from one state to another in as little as a few milliseconds, which is fast enough for some applications. However, in production applications, where test time carries a significant dollar value, this switching time may be too long. Solid-state relays (e.g. transistors, FETs) have a much faster switching time, generally below one millisecond. Going from a few milliseconds to a few hundred microseconds could shave off substantial test time and increase test throughput.

Another advantage of solid-state relays is their reliability. Solid-state relays have a switching life of almost 100 times that of electromechanical relays. This would be on the order of about 10 billion switch cycles instead of a good electromechanical relay's life of about 10 million cycles.

One disadvantage is the "on" resistance of solid-state relays, which is on the order of tens of Ohms. Such a high resistance could lead to measurement inaccuracies in a two-wire resistance measurement. Trying to measure a few milliohms with upwards of 10 Ohms of resistance in the circuit from the "on" resistance would effectively bury the low-resistance measurement.

One way around this is to use a so-called golden or standard channel. This is a channel with a short on the device side. The channel is closed, the resistance measurement is made and the measurement is subtracted from all other channels. Therefore, the "on" resistance is essentially zeroed out. The problem is that this holds for only the golden channel and would be slightly different on each channel. Using this method would depend on the magnitude of the resistance to be measured and the accuracy required.

Another method used to correct for this resistance is the four-wire measurement technique, which involves using two channels instead of one. One channel is used to source the current and one to sense the voltage. This is a standard method to measure low resistance. Using an electromechanical or reed relay would only have a contact resistance of tens of milliohms, which would be more advantageous to the low-resistance measurement using the two wire method.

10. Four-wire switching for low resistance applications

Applications such as contact resistance measurements and cable continuity testing typically involve switching low resistance. Low resistance switching (< 100Ω) requires techniques that are normally not required for mid range or high resistances.

As previously mentioned, using four wires for low-resistance applications is an accurate method. Using the four-wire technique eliminates both lead wire and switch contact resistance. This would involve two channels instead of one, where each channel is a two-pole channel.

Normally, these two channels are paired in the four-wire or four-pole mode, which eliminates all the trace and test-lead resistance from the measurement. When measuring low resistance, this is the standard technique. A matrix is not required for low resistance switching applications, with only a multiplexer required for the switch portion. The multiplexer can use both the current source and voltage sense channels in a single four-pole switch. A matrix can connect all of the rows to all of the columns. While this is powerful for some applications, it is not required for the low-resistance application.

This month's tips were supplied by Dale Cigoy, Senior Applications Engineer at Keithley Instruments. To find out more please go to www.keithley.com.

If you have any tips and would like to feature in our column, please contact the Editor by writing to: Svetlana.josifovska@stjohnpatrick.com.

JACK OF ALL TRADES AND MASTER OF ALL

BELGIUM-BASED, UNIVERSITY RESEARCH DRIVEN, ORGANISATION IMEC REPORTS OUTSTANDING PROGRESS IN MANY FIELDS, SAYS BRIAN DANCE

Located in Leuven, Belgium, IMEC (the Inter-University Microelectronics Centre) is the largest independent nanotechnology and nanoelectronics centre in Europe, with over 1,550 employees, including people from over 50 nationalities; some 200 PhD students and visiting scientists; and 350 industrial residents. In the October last year two-day press preview to its Annual Research Review Meeting (ARRM), Gilbert Declerck, president and chief executive officer of IMEC, gave its mission statement as: "To perform research and development, ahead of industrial needs by 3-10 years, in microelectronics, nanotechnology, design methods and technologies for ICT systems."

IMEC was established by the state government of Flanders in 1984 as a non-profit organisation with a staff of 74, but has now grown to be one of the largest independent R&D organisations in its field and enjoys a worldwide collaboration with many partners. Under the new Frame Agreement signed with the Flanders government for 2007-2011, IMEC will receive a government grant of €210m for this five year period towards its total budget of over €1,200m, which includes external funding for the five years of about €1,000m, of which 85% originates from outside Belgium.

Here we can take only a brief look at a few of the developments presented. Although nanolithography and silicon chip design form some of the main fields of its work, IMEC is also heavily involved in device packaging and interconnects, the use of other semiconductor materials, including organic electronics, renewable energy sources, various new radio techniques, applications for biomedical applications and better healthcare and technologies for the intelligent environment.

CLEAN ROOMS AND NANOELECTRONICS

Luc van den Hove, executive vice president and chief operating officer, said that IMEC has Clean Room 1 with 4800m^2 space (1750m^2 Class 1) in continuous 24-hour operation with a 200mm wafer pilot line. It also has a 3,200m^2 Clean Room 2 with a 300mm pilot line and FOUP wafer transport with full flow capability. It aims to move from 32nm towards 22nm half pitch features this year and to develop 22nm during 2008-09, focusing on logic and memory developments. Its EUV (Extreme UV) tool from ASML will be used with a numerical aperture of 1.35 in 2008, using coupling with a liquid of high refractive index. IMEC is advancing copper/low dielectric constant interconnects towards 32nm and less.

Kurt Ronse, Director of the IMEC Advanced Lithography Program, discussed the three main options for 32nm half pitch work that are still being explored. They are based on the following equation for maximum resolution:

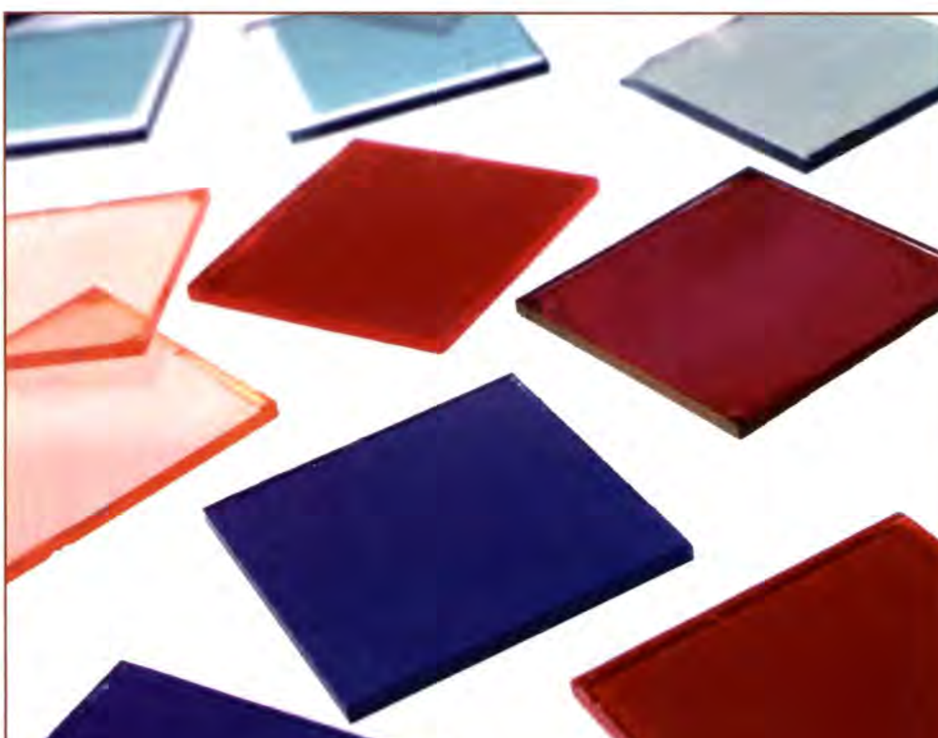
Resolution = $k_1\lambda/NA$

where λ = wavelength

NA = numerical aperture

1. NA Scaling

Single exposure lithography using 193nm radiation from an ArF laser, with immersion in a liquid of high refractive index, can give NA



A broad range of organic semiconductors are investigated for their application in PSC

values of 1.60 to 1.70 and a k_1 of less than 0.3. It is the prime solution for the 45nm mode and possibly even beyond this, but 32nm half pitches will be extremely difficult to resolve with 193nm immersion if single exposures are used. It would require a fluid of higher refractive index than water, and an optical material for the last lens element with a higher index and a high index photoresist. Ronse concluded that high index immersion lithography for 32nm half pitch will be too late, post 2011. It is a possible solution for only a single 45nm lithography generation, after which it would be replaced by a later technique.

2. k1 Scaling

Double patterning exposures with 193nm radiation can give NA values of 1.20-1.35 and k_1 values in the range 0.15-0.20. Ronse suggested that double patterning may be the only solution available in time for the 32nm half pitch, which is feasible with water immersion lithography, but whether it would be cost effective is questionable. The cost of ownership is a concern and techniques for resist freezing will require time for development and may cause double patterning to be replaced by a single exposure method with high index immersion or EUVL when available. He said space-defined patterning is an attractive alternative for memory applications.

3. λ-Scaling

Extreme UV radiation of wavelength 13.5nm provides a NA of only about 0.25, with a k_1 value of 0.6. In Ronse's opinion, EUVL will need several more years for the learning of the technology and for establishing the infrastructure, so it may be too late for the 32nm half pitch. However, cost of ownership, single patterning and large extendibility may make it a worthwhile learning medium towards 22nm technology and beyond.

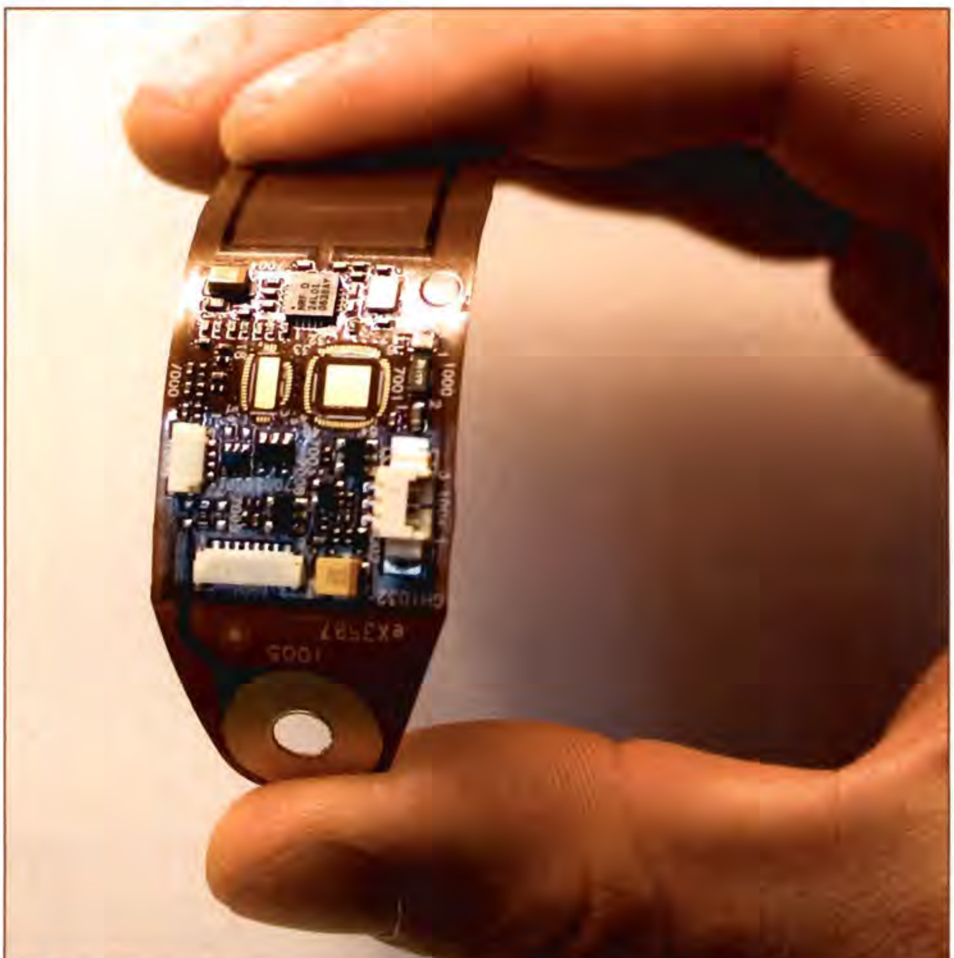
It has been agreed that ASML will install an EUV pre-production tool in IMEC's 300mm facility in 2010, so that IMEC and its partners can research 22nm CMOS on the most advanced lithography system in the world. This follows the use of an ASML demonstration tool using a tin plasma EUV source at IMEC to produce 35nm and 40nm lines in a 100nm MET-2D resist. The pre-production tool will provide much greater source power with optimised optics. Martin van den Brink of ASML said: "Our roadmap shows that ASML's EUV systems have the potential to expose more than 100 wafers per hour, which is well above the minimum required for cost-effective EUV chip manufacturing."

3D Programme

The 3D Integration Programme at IMEC for putting multiple die systems into package was discussed by Eric Beyne, Scientific Director of InterConnect, Packaging and Systems Integration. The driving reasons for 3D interconnects and packaging is size reduction and achieving minimal area/volume ratio for electronic systems. The 3D concept can also avoid the problem of long interconnects, which are too slow and which consume too much power. Hetero-integration or the 'seamless' mixing of different microelectronic technologies at the wafer level can be achieved with 3D systems.

Beyne said that general interest in 3D devices has strongly increased in the past year with industrial application announcements, publications and conferences, most of these activities being either technology or design-orientated. He concluded that, for 3D integration to become successful, a concurrent approach is required. System design should exploit the unique characteristics offered by 3D stacking technologies, while 3D developments should be focused on the system design requirements. IMEC therefore proposes a comprehensive 3D integration programme that integrates its technology with orientated 3D wafer level processing.

When developing a new product, a system upgrade will be possible by using additional layers of silicon containing extra components. IMEC will open a 3D-SOC design program to



IMEC's wireless, flexible and stretchable ECG patch for comfortable cardiac monitoring

complement work on wafer-level packaging (3D-WLP) and stacked IC materials and processes (3D-SIC). A universal communication fabric will be needed (including clock and power distribution) to enable the interconnection of components in separate layers, each possibly produced by the use of different technologies.

DRAM DEVELOPMENTS

IMEC has initiated research into DRAM process technology for its next generation of MIMCAP (metal-insulator-metal capacitors), this being part of its sub-32nm CMOS device scaling programme. The work will allow IMEC and its partners to address the material and integration requirements to scale MIMCAP to future technology generations. In order to scale DRAM towards the 50nm mode and beyond, MIMCAP dielectrics require materials with a higher dielectric constant than current industrial materials, such as ZnO_2. An effective oxide thickness of 0.5nm is targeted for the MIMCAP dielectric in the sub-50nm mode by the middle of next year, falling further to 0.3nm in 2009 for the 45nm mode.

The DRAM industry is facing the major problem of scaling the dielectric equivalent oxide thickness, while attaining very low leakage currents with dielectrics only a few atoms thick. IMEC has set up a baseline process for MIMCAP evaluation based on the TiN electrode and ZrO_2 as the capacitor dielectric. It is being used to screen new materials, such as W, Mo, TaC, Ru, etc. Stringent DRAM requirements, as dictated by the ITRS, will be used as selection criteria, including a leakage current of less than 1fA per cell and a total physical MIM thickness of under 20nm. A MIMCAP deposition process will be developed to investigate major integration issues, while mimicking as far as possible the effect of full DRAM integration, including passivation, annealing, etc.

The MIMCAP subprogram is part of the CMOS scaling program in the IMEC sub-32nm CMOS research platform. It brings the top five leading memory suppliers together with leading logic independent logic manufacturers, including Elpida, Hyniz, Infineon/Qimonda, Intel, Micron, NXP, Panasonic, Samsung, STMicroelectronics, Texas Instruments and TSMC.

Large area i-PERC solar cell on a very thin wafer

BIOMEDICAL WORK

Ultra low power digital signal processing (DSP) devices are required for passing information from sensors on a patient to a base station for analysis. The goal is an application specific processor (ASIP) providing 1000MOPS per 100μW. Applications include ECG, EEG and other monitoring, also hearing devices. For example, a wireless, flexible and stretchable ECG patch is available for comfortable and continuous cardiac monitoring after a heart attack, or after giving cardiac medication or for the diagnosis of an abnormal or dangerous heart rhythm.

Currently most power is required for communication, but in future more will be required for computation and less for communication, said Bert Gyselinckx, programme director Wireless Autonomous Transducer Solutions, the Holst Centre, IMEC-NL, The Netherlands, working with Target Compiler Technologies, a spin-off from IMEC.

A 175mAh lithium ion battery will provide from 12 hours to several days of operation. However, IMEC has also developed a 2-channel wireless EEG system which derives its power from a 2mW thermoelectric generator using body heat from a patient as its power source. Another system developed at the Holst centre monitors sleep disturbances with the patient in his home environment, which is far better and more economical than using a polysomnogram in a sleep centre.

The possibility of using new enabling materials for future CMOS products was discussed by Marc Heyns, IMEC Fellow and Department Director. He concluded that such materials and devices will be needed to

Software-defined-radio analogue front-end

continue performance scaling on silicon based platforms; they include high mobility channel materials, such as Ge and III/V compound semiconductors. The introduction of nanotechnology as nanowires and carbon based materials is also required, plus new device concepts for improved performance with reduced power consumption.

Biomedical IC-centric technology for small implantable devices was the topic discussed by Kris Baert and Chris Van Hoof. Smarter body implants can provide a major step towards fully functional substitution for the restoration of human performance. IMEC aims to be able to increase the autonomy and unobtrusiveness of medical implants by providing silicon based integration technology solutions to dramatically reduce size, increase functionality and permit the cost effective production of reliable implantable systems.

Current implantable devices are mainly hybrid system-in-package solutions that do not use nanosystems, with system complexity limited by size, etc. Power has been a major problem, as the battery occupies a large part of the system volume. Furthermore, most electronic implants have limited mechanical flexibility and little or no stretchability.

PHOTOVOLTAICS

The IMEC Solar+ Programme was presented by its director, Jef Poortmans. It uses crystalline silicon thin film solar cells deposited by five different technologies; the current silicon active layer thickness of 220μm will successively fall to 5μm for silicon on glass by 2020, thereby achieving a 1.5% per year efficiency increase. The programme also includes non-silicon inorganic solar cells using III-V materials and germanium cells for thermophotovoltaics.

Poortmans said the photovoltaic market is booming with annual growth rates of 67%, 45% and 40% in the years 2004-2006. Bulk crystalline p:n silicon solar cells take 92% of the market share and give a laboratory efficiency of 24.7% (industrial 13-17%). Amorphous Si:H p-i-n cells have 5% market share and a laboratory efficiency of some 13%. $CuIn(Ga)Se_2(S_2)$ and CdTe p-n junctions with CdS total only about 3% of the market.

A PV Technology Platform was created in 2005 to contribute to a rapid development of a world-class cost competitive European PV for sustainable electricity production. Poortmans said that photovoltaic generation will be a major source of energy for the future and is often the best enabling technology to ensure energy autonomy of distributed wireless systems. Many more microelectronic companies are increasing their photovoltaic activity.

The typical photovoltaic electricity generation cost in Euro per kWh may fall from its present value of about 0.30 to 0.15 in 2015 (competitive with retail electricity), and to 0.06 (competitive with wholesale electricity) by 2030, with a long term potential to fall to 0.05. Current typical payback time in Southern Europe is two years, estimated to fall to one year in 2015 and further to six months in 2030, with a long term potential of just three months.

Generation costs in Southern Europe with an irradiation level of $1800kWh/m^2$/year are estimated to fall from 0.17€/kWh in 2010 to 0.06€/kWh in 2030. In Northern Europe, where the irradiation level is some $600kWh/m^2$year, the estimated generation costs will be about 0.50€/kWh in 2010, falling to about 0.17€/kWh in 2030. This means that photovoltaic generation will be cost-competitive throughout the whole of Europe by 2030.

Paul Heremans, IMEC Fellow, said that organic solar cells have the potential to reduce the cost of photovoltaic energy production below $1.00 per watt. He forecast that photovoltaic cells based on 'organic' or 'plastic' semiconductors will be available some years from now, with R&D continuing for at least a decade afterwards to improve performance and to reduce cost. He said IMEC can make semiconductor devices based on thin films of such molecules, including not only solar cells, but also transistors, memories and light emitting diodes. The manufacturing processes needed to make these devices are fundamentally very different from those used to produce standard silicon devices. Most of the processes are carried out at near room temperature, so the energy budget is small and the processes environmentally-friendly.

Two classes of organic semiconductors can be identified, namely small insoluble molecules and conjugated soluble polymers. They are manufactured by different techniques and it is not yet clear which will provide the optimum performance for low-cost photovoltaic electricity generation.

Small organic molecules can form very dense films when they are evaporated onto a foil. Evaporation can create multiple layer films relatively easily, but not true bulk heterojunction devices. These evaporated devices are coming close to their optimum efficiency, but this is not yet as high as that of polymers processed in solution.

Heremans said that major improvements are expected from the use of new materials and process innovations. He added that IMEC is building a pilot line, or O-line, as there is a need for a laboratory with stable and reproducible processes for molecular and polymer organic photovoltaic cells to benchmark the processes and to stabilise them for industrial take-up. The production of organic solar cells requires a unique combination of equipment and processes. ■

Gary Nevison is chairman of the AFDEC RoHS team, and Customer Support Manager, Legislation and Environmental Affairs at Premier Farnell. As such he is our industry expert who will try and answer any questions that you might have relating to the issues of RoHS, WEEE and REACH. Your questions will be published together with Gary's answers in the following issues of Electronics World.

ONGOING REVIEWS KEEP THE ELECTRONICS SECTOR OUT OF THE COMFORT ZONE

If your company has ticked the box thinking that RoHS is fully implemented, and a done deal, then think again. As part of the on-going review of RoHS, started by the European Commission (EC), all current exemptions will be reviewed for their validity, as well as seven new ones. This process is extremely rigorous.

With all exemptions the onus is on industry to prove to the EC that a particular exemption is required and that a viable alternative to the exempt substance is not available.

The EC has started two new studies, one covering exemptions and the other looking at the possibility of further restricted substances beyond the existing six. Both studies could well have a significant impact on existing designs that rely on current exemptions, which may be withdrawn, or substances that may be banned.

Once again the Oko Institut in Freiburg, Germany has been awarded the contract to evaluate the exemptions. However, following their previous reviews, there is still no definitive list covering the status of exemption requests, or their outcome, so some remain in limbo which is far from ideal.

Study 1 will review all existing exemptions including those that manufacturers take for granted such as:

- Lead in glass of electronic components (required for many passive surface mount devices);
- Lead in high melting point alloys (required for power devices such as rectifiers, regulators and solid state relays);
- Lead in ceramics (required for piezoelectrics, chip resistors and some MLCCs);
- Lead in solder for network infrastructure and servers etc;
- Cadmium in switch and relay contacts.

The seven new exemption reviews are:

- Lead in silver rings on the exterior lamp surface of induction-type fluorescent lamps;
- Mercury in plasma displays;
- Cadmium in photocells for accurate control of lighting equipment;
- Cadmium-based photo-resistors used in professional audio equipment;
- Relock fuse, model X-09 (lead and cadmium);
- High voltage diodes in glass housings;
- Cadmium and cadmium oxide in thick film pastes used on beryllium oxide substrates.

Exemptions may well be deleted if there is any evidence that substitutes exist. Industry needs to take a pro-active approach and provide any data that suggests alternatives are technically unsuitable or have more of a negative impact on health and the environment than the RoHS substances. Technical evidence will be vital and letters simply supporting an exemption are likely to be of little use.

The EC accepts that research into substitutes will be mainly carried out by large multi-national organisations, not by small and medium enterprises (SMEs). However, SMEs are clearly affected by RoHS exemptions and should make contributions to the study by providing results of their efforts to find substitute materials and designs, and also by encouraging their OEM component suppliers to submit technical data. Doing nothing and relying on others is very risky as almost all electrical products rely on at least one exemption.

Study 2 will look into the possibility of additional substances falling within scope. Member States are likely to suggest many substances that could be considered and these may well be restricted if, once again, industry does not provide clear technical evidence showing that they cannot be replaced or that possible substitutes are unsuitable.

Studies carried out in the US show that lead-free solders are no better (or worse) than lead-based solders, just different, and as a result provide no overall benefit to the environment. These results are not sufficient to allow an exemption for lead in solders, but would have provided significant evidence when the restriction of lead under RoHS was first considered.

According to ERA Technology, who have also done work for the EC in this area, substances that may be considered for restriction include arsenic, berrylium, plasticisers (that aid flexibility in plastics) and many types of flame retardants.

Another consideration here is that many alternatives are not fully tested so the risks are unknown, which is one of the main reasons for the REACH regulations.

This, along with the review of Categories 8 (medical devices) and 9 (monitoring and control instruments) that are likely to be added to the scope of RoHS in the future, could well have profound implications to all sectors of the electronics industry, including those that are currently excluded.

Please email your questions to:
svetlana.josifovska@stjohnpatrick.com
marking them as RoHS or WEEE.

by Myk Dormer

THE BIT OF WIRE ON THE END

Somewhere, and in some form, there's got to be something that radiates the RF energy that makes your data link actually 'wireless'. Your radio module needs an ***aerial.***

Now, to address the brave few readers who haven't already run off: I'm not going to deal with antenna theory, Maxwell's equations or any scary vectors. The subject of aerial design is a huge one and ranges from the simplest free-field dipole, to complex, phased multiple-element directional arrays. For the typical low-power radio application there is a far more limited choice of configurations, so at a practical level, let's look at the options, and more importantly the pitfalls, awaiting the ISM band radio-user.

"POWER LOSSES IN THE AERIAL CAN REDUCE THE GAIN BELOW THAT PREDICTED BY THE RADIATION PATTERN, AS CAN IMPERFECT TUNING AND INCORRECT MATCHING"

The antenna can be considered as a transducer. It converts RF current into electromagnetic waves and radiates them into space. The theoretically simplest antenna is the ***isotropic radiator***: an infinitely small point source that radiates radio waves equally in all directions. No real antenna is ever so perfectly non-directional. Even practical "omni-directional" antennas only radiate equally in a single plane. The radiation pattern of a vertical half wave dipole (an omnidirectional type) in three dimensions looks like a donut: almost no energy is radiated up or down.

Antennas are specified according to their radiation pattern - and directivity, if any - their effective gain, which is expressed in dB relative to an isotropic radiator, and their range of operating frequencies or bandwidth.

Directional antennas usually have positive gain, a result of radiating the power over a limited arc, instead of everywhere, as do a few omni-directional types, by compressing the vertical axis of the radiation pattern or by combining the signal from multiple antenna elements. On the other hand, power losses in the aerial can reduce the gain below that predicted by the radiation pattern, as can imperfect tuning and incorrect matching.

Most ISM band regulations have transmitted power limits which preclude the use of (positive) gain aerials, at least at the transmit-end of the link. This, combined with the portable or mobile nature of many of the likely target applications, limits the usual choice of antenna to a small sub-set of the simpler types (which may be just as well: the ARRL publish a simple *"Antenna Book"* which is 944 pages long).

The same 'mobile' nature of ISM applications also simplifies the choice of aerial polarisation patterns: to achieve a practical omni-directional performance from simple aerial designs, vertical mounting and, hence, vertical polarisation is almost obligatory.

To concentrate on the aerial types frequently used in the ISM bands, there are:

* **Whips:** The most common form of antenna used with radio modules is the quarter-wave whip. It's simple, cheap and can be made in a moment out of wire (length in mm = 71250/frequency in MHz). It also presents a near 50ohm feed-point impedance, without extra matching parts.

But to operate according to theory this aerial needs to be mounted on a groundplane, or on a sufficiently large conducting object to mimic one. With luck, this can be easy to arrange (for instance on a car's roof) but it's all but impossible on a handheld, plastic box. It's often inconveniently long, too (8cm at 869MHz isn't especially onerous, but at 173MHz the length is about 40cm. They aren't nicknamed "eye-pokers" for nothing).

There are other varieties of monopole: base loaded types, with shorter physical lengths, and longer 5/8 or 1/2 wavelength types with higher gain, which are only usually encountered as commercially made parts.

* **Dipoles:** The centre-fed half wave dipole is theoretical start point of any analysis of aerial theory. The commercially produced units, when mounted from a pole or off a building wall by the proper bracket are a good choice for a ***relatively*** inexpensive 'base station' antenna. But they are large and need to be mounted clear of obstructions.

Also encountered are end fed and co-linear dipole antennas. These look physically like (very long) monopoles and offer excellent omni-directional gain characteristics, with some co linear types offering over 6dB of gain, by virtue of a vertically compressed radiation pattern and multiple aerial elements. But they are big, very expensive and rarely encountered in low power radio implementations.

* **Helicals:** A development of the whip, this is a monopole wound into the form of a 'spring'. It can be hand-made (most module manufacturers optimistically provide a recipe for one in their data sheets. Compare them: they're all totally different) and is both, considerably shorter than a whip and theoretically operates independent of any groundplane. Unfortunately, the dimensions are critical and correct behaviour is hard to verify without proper RF test equipment. This type of aerial de-tunes badly in the presence of conducting masses (like your body).

Inexpensive factory made helicals do take a lot of the guesswork out of using this class of aerial, and those fitted with a coaxial connector (SMA, BNC or TNC) permit neat, trouble-free mounting through bulkheads and case walls.

As a rule of thumb, the shorter a helical is for a given frequency (for the popular 144MHz amateur band I've seen helicals between 3cm and 20cm long), the more lossy it will be.

* **Loops:** In the simplest case, this is just a single turn inductor, tuned to resonance by a capacitor. The loop area needs to be maximised, or aerial efficiency will be low; at UHF, it is usual to add extra series capacitors at intervals around the loop to drop the resonant frequency.

Although physically simple, this aerial can be very tricky to use. It presents a higher than 50-ohms impedance at the feed point, requiring further matching parts and, almost certainly, will need to be manually tuned on each unit (the bandwidth of this type of aerial is very narrow). Additionally, the efficiency of such loop antennas can be unacceptably low. Still occasionally seen below about 200MHz are ferrite loaded loops, where the aerial is a coil wound onto a ferrite block or rod. Such units are a black art: composition of the ferrite is critical for high frequency operation; the aerials are highly directional, very narrow in bandwidth and, owing to increasing losses in the ferrite at higher field strengths, almost the only aerial type that is usable only on 'receive'.

* **Patches:** Best considered as a 'flattened monopole', a patch antenna looks like a specific area of conductor, spaced off a groundplane and suitably matched at the feed point.

The patch isn't a useful ISM application antenna as it is; at the frequencies of interest the area of the patch is considerable and they can be awkward to tune, but a variant of it is becoming quite common - the ceramic loaded antenna.

By fabricating the antenna elements on a substrate with a very high dielectric constant, combined with low RF loss characteristics, such as a carefully formulated ceramic, or a teflon/glass composite, the physical dimensions of the aerial can be reduced without incurring unacceptable losses. This is probably the antenna in your cell phone, as a ceramic 900MHz band aerial can be shrunk to under 2cm long.

This class of antenna is becoming more readily available on the ISM frequency bands, and as the price of these originally expensive components falls they are likely to be seen built into more and more modules.

Sometimes it is "just a bit of wire". But it's probably the most important part of your radio.

Myk Dormer is Senior RF Design Engineer at Radiometrix Ltd
www.radiometrix.com

THE CHALLENGE OF SUPPORTING NEW TECHNOLOGY ADOPTION BY SMBs

RESEARCH SHOWS THAT MANY OWNERS OF SMALL AND MEDIUM SIZED BUSINESSES (SMBs) ARE BAFFLED BY TECHNOLOGY AND FAILING TO BENEFIT FROM THE COMPETITIVE ADVANTAGES OFFERED BY A RAFT OF NEW TECHNOLOGIES. TERRY RICHES, COMUNICA'S SENIOR BUSINESS MANAGER, SUPPORT & INTELLIGENT INFRASTRUCTURES, EXPLAINS WHY THIS IS AN IMPORTANT ISSUE FOR THE ECONOMY

Baffled by technology? You're not alone... The EC's ICT Taskforce reported in one study that small and medium sized businesses (SMBs) across Europe are failing to invest sufficiently in technology.

"A wider integration of ICT by businesses throughout Europe would significantly contribute to improve effectiveness and productivity and could potentially revolutionise and maximise processes and organisations in a number of key sectors," say the report's authors.

However, research by Ofcom indicates that many small businesses are either unaware or confused by the raft of new technologies hitting the workplace. Peter Scargill, the National IT Chairman for the Federation of Small Businesses comments: "The major barrier for small businesses is finding the time to keep themselves informed in an age where advances are coming faster and faster and, in many cases, are being driven by the bigger companies."

"BT and others are moving over to VoIP and no doubt will make the technology as simple to use as possible. Meanwhile, WiFi is becoming almost universal, with potentially frightening security implications," he continued. "Those who don't make use of these technologies will be putting themselves at a disadvantage; yet, for those who do make the move, it's important that they have at least an overview of advancing technologies to ensure they are able to use the technology to improve their businesses. If they choose not to embrace change they should be aware that they will have competitors who will."

Telecoms and IT analyst Teresa Cottam adds that it is easy to oversimplify the picture in the SMB market. "This is one of the hardest sectors to analyse, because there are such wide variations in business type. We should remember that there are significant numbers of highly IT-literate SMBs. In fact, SMBs are often at the bleeding edge of technology development and adoption, but we also need to recognise that for a variety of reasons some SMBs are either unwilling to adopt or are less adept at adopting new technologies. Yet these technologies have huge potential to help them become more competitive. Technology can level the playing field between bigger companies and the SMBs."

Whether we like it or not, technology is becoming more and more embedded in the way we live and the way we do business. Many types of business now use a range of technologies that underpin their business processes and no matter what size the business is, it is prudent for business managers to periodically assess what's available and how it can help their business perform better. However, in the case of SMBs, all too frequently they do not derive optimal benefit from their technology investment.

For example, Brunel University conducted research on how long it took staff to conduct various business tasks and the sad conclusion to its research was that there was little evidence that

Many SMBs start with the attitude that they wish to spend as little as possible on technology, disregarding the cumulative cost savings that can be generated if they get it right

Examples of benefits of WiFi and VoIP to small businesses	
WiFi	**VoIP**
• Reduces cost of deploying a network • Allows networks to be deployed where it would be inconvenient or impossible to lay cables • Provides opportunity to offer network services securely to guests • Provides opportunity to offer network services to customers (for free or charged for) • Allows employees to 'roam', enabling collaboration, mobility and more efficient working • Particularly good for growing companies as it minimizes cost and disruption of adding new users to network	• Reduces cost of long-distance telephone calls (ie national or international calls) • Is easier to manage your phones, and to add, remove, move and make changes • Fast to deploy • Reliability and scalability • Supports mobility, distributed working and home working • Innovative applications such as allowing you to talk to multiple people at the same time and to combine voice and data (eg to talk and share files) • Supports unified messaging (allowing you to combine voice, email, fax, voicemail etc)

Table 1: Examples of benefits of WiFi and VoIP to small businesses

broadband was revolutionising SMBs. To exemplify the problem the researchers highlighted the case of a rural marketing company, where getting broadband actually made staff less productive. The reason for this was that while staff had begun to send information electronically to customers, they were also still sending a hard copy in the post.

There are lots of reasons why many SMBs fail to take advantage of new technology, but lack of training and failure to take a strategic approach to technology are the two most common.

Another key problem is that many SMBs start with the attitude that they wish to spend as little as possible on technology, disregarding the cumulative cost savings that can be generated if they get it right. And, as Peter Scargill has highlighted, small business managers often have time pressures which mean that evaluating new technologies is low on a long list of priorities.

While this is understandable, making time to evaluate new technologies should be viewed as an investment in the business that will pay dividends in terms of increased competitiveness. Investing a little time now could save a lot of time in the future. And, bluntly speaking, because of the increases in efficiency that new technologies can bring failure to keep abreast of new technologies will reduce a company's ability to remain competitive.

Investing in a solid network foundation, for instance, creates a range of benefits for an SMB:

• Improved efficiency. An effective network allows workers to become more productive and decreases unproductive 'downtime'. It also enhances collaboration and communication, allowing faster decision-making and improving customer service.

• Increased mobility. The ability to access the company network, e-mail etc while outside the office allows companies to support distributed working and to increase efficiency and effectiveness.

• Greater security. Security threats have both operational and financial consequences for business. Optimising the infrastructure makes securing it much easier.

• Greater flexibility. As the company grows or changes, technology needs will change. Investing wisely means the infrastructure will allow you to add more users as needed and new applications as they become relevant (such as voice over IP, teleconferencing and so on). You can, therefore, ensure that technology you invest in today not only demonstrates a return on investment but also supports your needs tomorrow.

New technologies such as WiFi and VoIP also offer a range of benefits to the small business, as shown in Table 1.

The SMB sector is a vibrant and vital part of the UK economy. Figures from the Federation of Small Businesses state that the 4.3 million small businesses in the UK employ more than 12 million people, or around 58% of the private sector workforce. By enabling the UK's SMBs to take full advantage of new technologies not only do we improve their competitiveness, but we also improve the competitiveness of the UK economy as a whole. ■

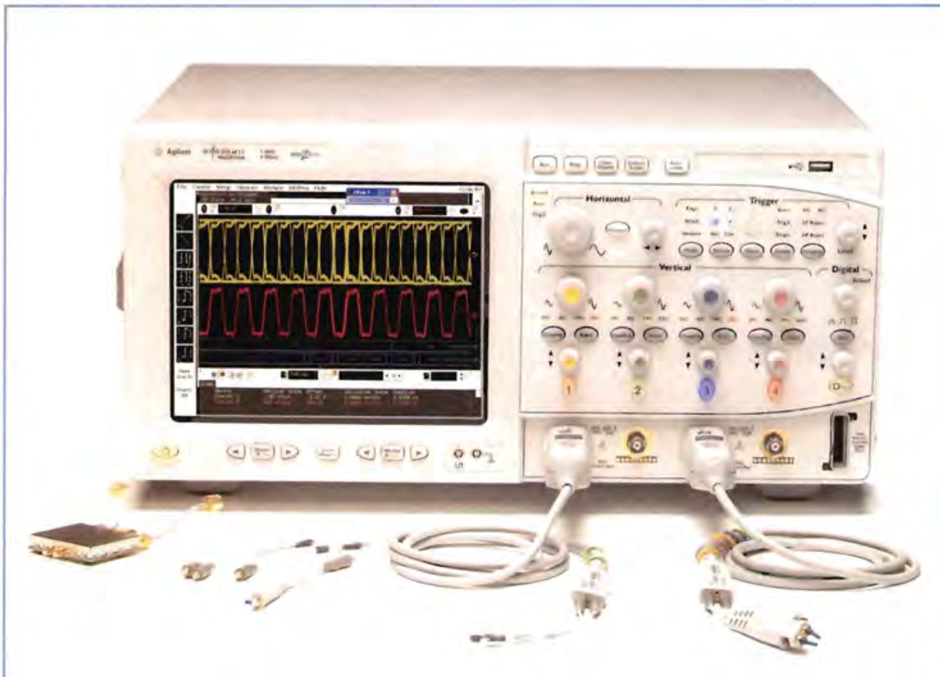
PETER KASENBACHER, EUROPEAN PRODUCT LINE MANAGER FOR OSCILLOSCOPES AT AGILENT TECHNOLOGIES, OUTLINES SOME OF THE MOST EFFICIENT TECHNIQUES AND BEST PRACTICES FOR MEASURING ONE OF THE MOST CHALLENGING SIGNALS IN DESIGN – POWER SUPPLY NOISE

USING AN OSCILLOSCOPE TO MAKE POWER SUPPLY NOISE MEASUREMENTS

The aim, as with any other electronic product, is of course to achieve the highest customer and user satisfaction at the lowest possible production cost.

Today's electronics feature higher-speed switching, faster slew rates, more active pins per package and smaller signal swings. Increased switching speeds and signal slew rates and the increased number of active pins result in more switching noise being induced in power supplies. At the same time, circuits are becoming more susceptible to power supply noise with reduced signal amplitudes translating to reduced noise margins.

As a result, designers are more concerned about power supply noise in new digital designs, in everything from mobile phones to servers. Real-time oscilloscopes are commonly used to measure power supply noise because of the wide bandwidth of power supply noise. This article discusses power supply noise and the techniques for measuring it using an oscilloscope.



A wide bandwidth oscilloscope is ideal for measuring power supply noise

Ideally, there wouldn't be any noise on power supplies so how does it get there? Simple Gaussian noise generated by unavoidable thermal processes is usually not the dominant source. The primary source of noise in most digital circuits arises due to switching.

Switching power supplies create their own undesired noise, usually at harmonics of or coherent to the switching frequency. In addition, when gates and output pin drivers switch, this action creates transient current demands on the power supplies. Although these switching events may appear random in time, they tend to be coherent with clocks in the system. They can, therefore, be considered as "signals" superimposed on the power supply DC level rather than random "noise" (**Figure 1**). By considering noise in this way the analysis becomes simpler and more powerful.

Measurement Challenges

The wide bandwidth nature of power supply noise means that designers tend to choose oscilloscopes as the optimum tool for measuring it. Oscilloscopes can provide unique insights into the cause of noise. Unfortunately real-time, wideband digitising oscilloscopes and wideband scope probes have their own noise, which must be taken into account. If the noise being measured on the power supply is of the same order as the noise floor of the scope and probe, measuring the noise accurately can be challenging.

Another problem is dynamic range. The power supply sits at a DC voltage. The small AC noise superimposed on this is usually a tiny fraction of the DC level. With some oscilloscopes and probes there may be a challenge in offsetting the scope and probe sufficiently to allow the use of a more sensitive range in order to get the optimum view of the noise at a lower scope noise level.

Techniques and Best Practices

There are a number of techniques that can be applied to improve the ability to measure power supply noise.

• Understand how much noise the oscilloscope and probe contributes.

It should go without saying that the oscilloscope and probe should be selected with a sufficiently low noise floor to allow the measurement to be made accurately.

To understand the nature of scope noise, refer to the block diagram shown in **Figure 2**. There are two principal sources of noise in an oscilloscope and probe system. The input amplifier and buffer circuits in the scope contribute some noise, and the probe amplifier has noise inherent in its design. All scopes use an attenuator to vary the vertical scale factor. The scope's noise arises after this attenuation occurs. So when the attenuator is set to any ratio other than 1:1 (i.e. the scope's most sensitive hardware range), the noise will appear to be larger relative to the signal at the input connector. For example, consider a scope that has a basic sensitivity of 5mV/division with no attenuation inserted. Assume it has a noise floor on the 5mV/div range of 500 microvolts RMS.

To change the sensitivity to 50mV/div, the scope inserts a 10:1 attenuator in series with the input. The noise then appears as if it were 5mV RMS relative to the input (500 microvolts times 10). Therefore, there is an advantage to using the most sensitive range possible to avoid "magnifying" the scope's noise unnecessarily. The noise introduced by the probe is introduced before the scope's input attenuator, so it will always contribute the same to the measurement regardless of the scale factor.

• A differential probe should always be used.

In most cases the probe noise is significantly larger than the scope's noise on the most sensitive range. Most power supplies can drive the 50-ohm input on a scope with no problem, so why add the probe's noise into the measurement unnecessarily? The answer has to do with dynamic range.

To measure the noise on a 1.5VDC supply, 1.5V of offset should be used to position the signal at the centre of the screen and centered on the range of the scope's A/D converter. The most sensitive range on which the scope will allow 1.5V offset is the 100mV/division range. On the 100mV/div range, the scope's noise will be ~ 3mV RMS. On the 100mV/div range the noise being measured will only exercise a small portion of the range of the A/D converter, so measurement resolution would be lost.

If the oscilloscope in itself can only provide the required offset on its less sensitive measurement ranges, then using probe offset can rectify the situation. By using active probes that can provide a greater range of offsets, more accurate measurements can be made and the impact of scope noise can be reduced. With an active differential probe, the signal can be offset by 1.5VDC, thereby allowing the more sensitive 10mV/div range to be used for the measurement in order to achieve more accurate results.

AC coupling can also be used to overcome the dynamic range problem, if the scope allows this. If the oscilloscope has 50 ohm inputs and the designer wishes to use 50-ohm coax with a "1:1 probe" (a 1:1 probe can be made fairly easily by stripping back the end of a short

Figure 1: Power supply noise

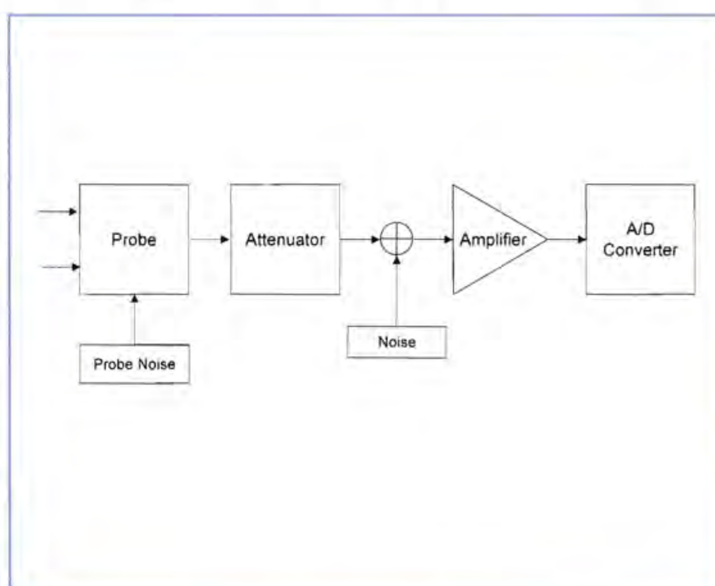


Figure 2: Noise sources in oscilloscope and probe

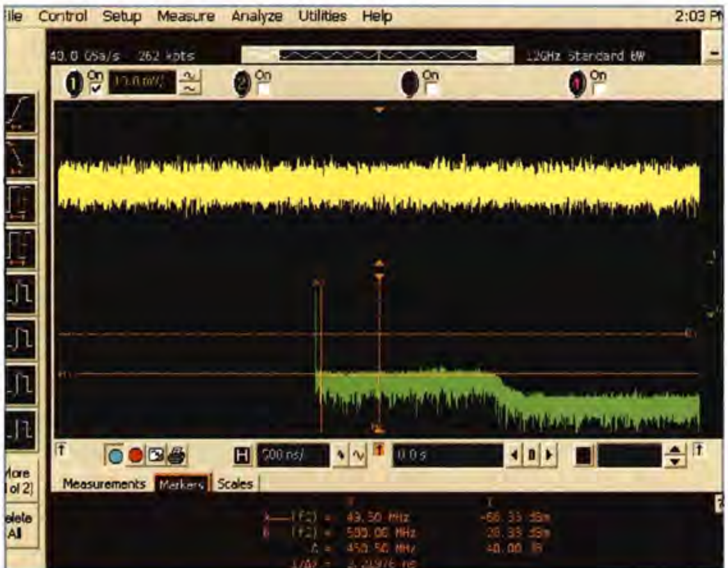


***Figure 3**: Fast Fourier Transform of power supply noise*

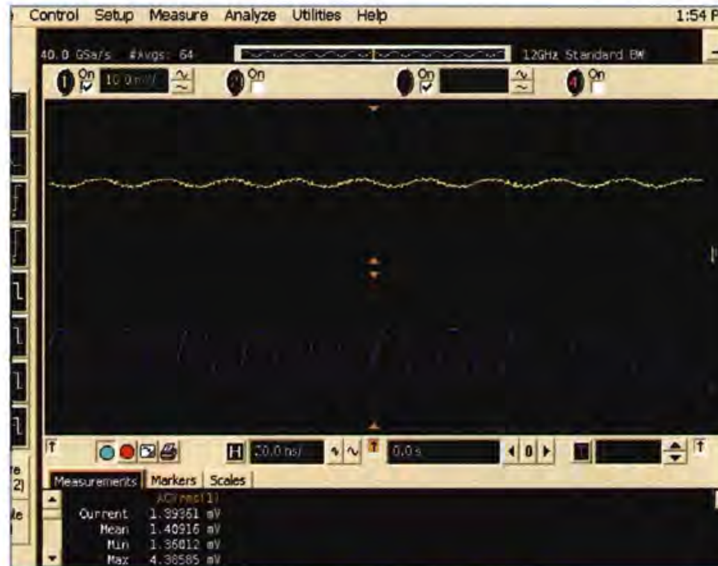


***Figure 4**: Triggering on square wave with averaging*

piece of semi-rigid coax cable and soldering a short ground wire to one side), then a series blocking capacitor can be used to AC couple the signal. The blocking capacitor size should allow the lowest significant frequency in the spectrum of the noise to be viewed. The downside of AC coupling is that it is not possible to see slow drift of the power supply voltage.

• Use FFT for analytical insight.
Most real-time digitising scopes have a built-in Fast Fourier Transform (FFT) function. The oscilloscope will capture a finite amount of time on each trigger, based on the amount of memory and the sampling rate. The FFT cannot "see" frequencies in the incoming signal that are below the inverse of the scope's time capture window. The lowest frequency that can be analysed by the FFT is given by the relationship:

F = 1/[1/(sampling rate) x (memory depth in samples)]

In order to see a suspect source in the FFT, the memory depth has to be set to capture sufficient samples. For example, if the switching power supply operates at 33kHz, it would be necessary to capture 1/(33kHz) or 30 microseconds of signal activity. For a sampling rate of 20GSa/s, this would equate to 600,000 points in memory.

In the Agilent 8000 series DSOs and DSO80000 series oscilloscopes, the FFT operates only on the data that is on the screen. In order to see the lowest frequencies possible for the memory and sampling rate chosen, the time base must be set so that all the memory is on the screen. This can be easily determined by referring to the memory bar above the graticule.

An FFT analysis can provide more insight into the signal. It can provide a quick analysis into the sources of the noise. For example, if a design includes a 33kHz switching power supply and a 500MHz clock, spurs may be seen at 33kHz and at multiples of 500MHz. The relative amplitude of these spurs will give some first-order insight into how much unwanted noise power each is contributing.

Figure 3 is an FFT analysis showing two components in addition to the 'white' noise. There is a component at 49.5MHz and another at 500MHz.

Another technique to improve visibility of the spurs is to average the FFT. The true random noise will be greatly suppressed by averaging the FFT, allowing very small signals to be distilled out of the noise.

• Trigger on suspect sources and use averaging to eliminate uncorrelated noise.

In some circumstances it may be possible to trigger on a signal that is phase-coherent with a non-random noise source and then use averaging. By using averaging all of the components that are not correlated to the trigger signal will be reduced or eliminated. This technique allows signal components to be extracted that would otherwise be swamped by the random noise coming either from the power supply itself or from the scope and probe.

Figure 4 shows an example of triggering on a square wave. The square wave could, for example, represent the switching noise arising from pin drivers or other transient load conditions. The noise components related to the trigger signal are clearly seen extracted from the total noise present.

Optimum Choice

The measurement of power supply noise can be challenging. An oscilloscope is the optimum choice of measurement tool because of its bandwidth. Good results can be achieved when good practices are adopted. This article has listed some of the techniques that can be deployed. These together with the correct selection of oscilloscope and probe means that the measurement of power supply noise can be achieved effectively and efficiently.

ADDITIONAL READING:

"Understanding and Using Offset in InfiniiMax Active Probes," Agilent Application Note 5988-9264EN
"Performance Comparison of Differential and Single-Ended Active Voltage Probes", Agilent Application Note 5988-8006EN.
These and other application notes are available at www.agilent.com/find/scopes

UMA/GAN CAPABILITIES ENABLING FIXED MOBILE CONVERGENCE

PHIL MEDD, PRODUCT MANAGER AT AEROFLEX AND BASED IN BURNHAM, IN THIS ARTICLE EXPLAINS THE BACKGROUND OF UNLICENSED MOBILE ACCESS (UMA) AND GENERIC ACCESS NETWORK (GAN) AND HOW IT WORKS

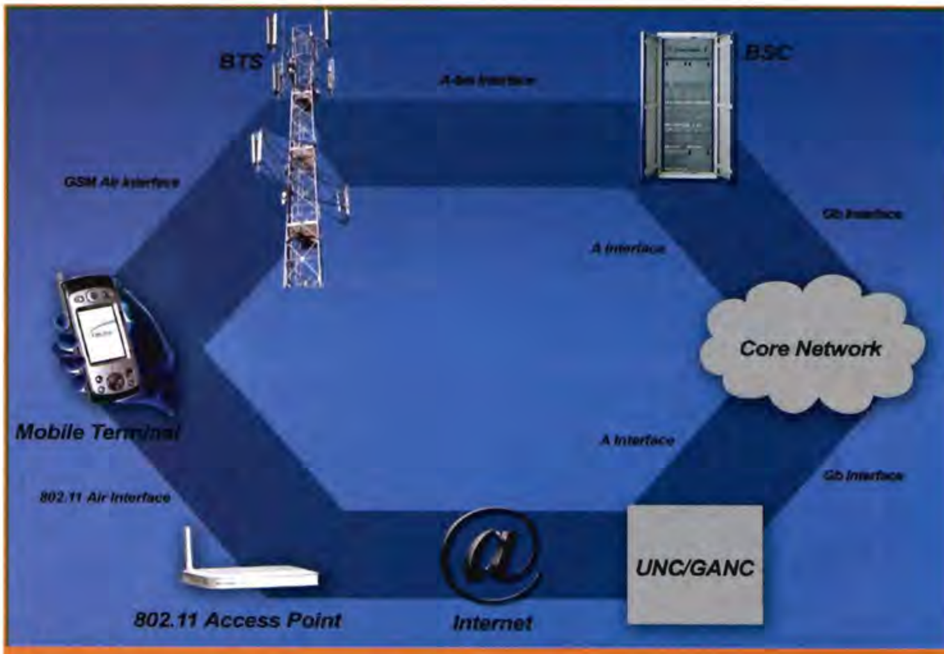


Figure 1: Network functionality with UMA Network Controller (UNC)

Unlicensed Mobile Access (UMA) and Generic Access Network (GAN) hold out the promise of increased revenue growth with low risk for both wireless network operators and mobile device manufacturers, while allowing subscribers the convenience of using a single handset for their home, mobile and office communications. The 3GPP standards are designed to enable this market to take off through the adoption of UMA/GAN.

Mobile phone penetration has now reached well over two billion subscribers globally. Most of them want to use their handset as their one and only device, saying goodbye to the usual rack of numbers for the fixed line home phone and office phones. This is often referred to as fixed-to-mobile substitution. However, the price premium to use a mobile device and often-poor indoor reception has discouraged customers from using just the one device.

Early Attempts

Early attempts at fixed-mobile convergence in the late 1990s looked at using manufacturer-specific micro basestations in the house or office that could route a call made on a cellular handset through a locally installed fixed wire phone line. However, the manufacturer-specific models were not economical for the mass market and still involved the need and costs associated with a fixed telephone line.

Over the last few years the advance in digital subscriber line (DSL) and cable modems have given domestic users a broadband experience for accessing the Internet at a very reasonable price, with most operators offering in excess of 2Mbps of "all you can eat" data plans. Voice over IP (VoIP) has also started to take off with services such as Skype and Vonage and an array of instant messaging programs incorporating free VoIP calls such as MSN or Yahoo Messenger. Lastly, it has also become extremely affordable to purchase a low cost wireless access point, typically conforming to the IEEE 802.11b/g standards.

This growth in broadband and VoIP coupled with low cost wireless access points located everywhere from airports and cafés to homes and offices has opened up a whole new market for fixed mobile convergence and with it the possibility for wireless operators to further displace fixed line phone providers and increase revenues, with little financial risk from what is now considered by many to be a saturated market.

UMA and GAN

This is where UMA/GAN, the 3GPP standard for cellular/Wi-Fi convergence meets both, the desire of the mobile phone user to completely remove the need for any other phone in their life, as well as the needs of wireless operators for low risk growth.

UMA was founded by over a dozen leading operators and manufacturers under the group name of UMA Industry Forum. The work was introduced into 3GPP GSM EDGE Radio Access (GERAN) group in June 2004, and was standardised and ratified by 3GPP as GAN in 3GPP TS43.318 as a release 6 feature during April 2005.

Although being the newer of the two terms, GAN is usually marketed as UMA, despite there being some further enhancements in how the lower layer headers are built up and differences in how the authentication is implemented. Both however work in a similar manner, whereby the user's device and the wireless operator's network are capable of supporting a cellular service such as GSM/GPRS, as well as a wireless LAN access technology such as 802.11.

From a network operator's perspective UMA functionality is a low-cost introduction, by adding an UMA Network Controller (UNC), which acts much like a base station controller (BSC). The UNC is connected on one side to the Internet, thereby connecting to the WLAN access points. On the other side of the UNC is a standard A interface for the circuit-switched communications through to the mobile services switching centre (MSC) and a gigabit interface for the packet switched connectivity through to the serving GPRS support node (SGSN).

GAN also uses the same principle but calls the UNC the GAN controller (GANC). Therefore, when a device hands over from a GSM to a WLAN it appears to the core network as just a different base station.

As the last mile to and from the access point is over the Internet, security is a key requirement. Therefore, when the handset detects a WLAN access point, an IPSec tunnel is started between the device and the security gateway (SEGW), which is located in the UNC/GANC element. This is achieved by using the SIM or USIM credentials and an encryption certificate embedded within the device; detailing addresses of the fully qualified domain name (FQDN) of the SEGW and the public DNS address of the SEGW etc.

Internet Engineering Task Force (IETF) specifications define the protocols for the Authentication procedure. They include IKEv2, EAP-SIM and EAP-AKA, thereby securely authenticating the user and establishing a secure tunnel into the operator's network.

The UMA GAN device has an enhanced protocol stack that duplicates the traditional lower layers of the GSM network. This involves the use of a WLAN transceiver to (de)modulate the 802.11 signal and encode/decode the TCP-IP frames received over the IPSec connection made with the UNC/GANC.

Two additional layers referred to as the generic access circuit switched resources (GA-CSR) and generic access resource control (GA-RC) layers are then used to replace the conventional layer 3 (Radio Resources (RR)), while the TCP-IP link effectively mirrors the GSM layer 2 (LAPDm). Therefore, adding these features to the devices to support UMA/GAN requires an additional level of complexity to develop, integrate and certify compliance to the 3GPP specifications.

Testing UMA/GAN

Recently, the PTCRB, the body responsible for overseeing the certification of handsets for the US market, has added testing of UMA/GAN to the formal certification scheme. Once formally validated test platforms and test cases are available, it will be mandatory for UMA/GAN to be able to pass these tests.

The Aeroflex 6103 AIME/CT, already listed at PTCRB as Test Platform 11, will support the GAN/UMA test cases, as described in the next section.

For essential early R&D requirements to test functionality for protocol development and regression testing, the 6103 AIME system additionally supports integrated GAN testing in either a single test set configuration with GSM/GPRS or up to eight test sets including other GSM evolution technologies such as EDGE up to multi-slot class 32, AMR, DARP and DTM. The system also supports all of the mandatory cryptographic schemes such as IKEv2, EAP-SIM and EAP-AKA.

The system's UMA/GAN and GSM/EGPRS protocol test capability is fully integrated under a single user interface that provides a single point of control for the configuration and operation of the entire UMA/GAN/GSM/EGPRS system, as well as the unified message logging for all the GSM cellular and UMA/GAN WLAN protocol layers. This turnkey approach to protocol testing allows engineers to get far greater productivity from their test tool investment.

Subjective verification of the GSM audio path through the terminal's codecs (both encode and decode) is currently achieved using a voice quality analysis package called VQA. This can be accomplished with real time audio (through a microphone and speaker connected to the 6103 AIME controller PC) or by sending and saving audio files, allowing an engineer to judge subjectively the voice quality or drop outs during a handover or any jitter than may be caused as a result of a channel or encoder issues.

In addition to providing support for a full UMA/GAN implementation, the Aeroflex 6103 AIME/CT can provide support for the complete suite of 83 GAN test cases, listed in 3GPP TS51.101 sections 81, 82 and 83, to facilitate pre-compliance and certification testing of UMA/GAN devices.

In order to accelerate testing, large numbers of test cases can be run as a campaign. The system supports the functionality to create a comprehensive mix of test cases, such as GAN, but also including GSM, GPRS, EGPRS, AMR, DARP and DTM allowing users to create a full regression test plan that can be run every time new software is built and flashed into a prototype device. This enables the system to be run overnight providing next morning results, increasing test lab productivity and return on test tool investment, but ultimately decreasing time-to-market costs.

The addition of UMA/GAN test capability to the Aeroflex 6103 AIME and 6103 AIME/CT provides the first available integrated UMA/GAN terminal protocol and performance test solution in a system designed and manufactured by a single test and measurement company. ■

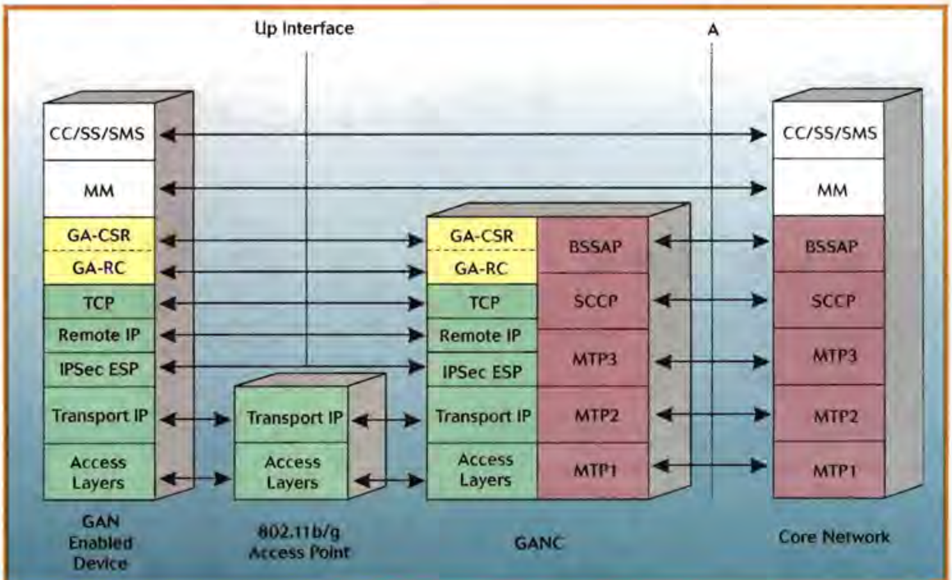


Figure 2: UMA GAN protocol stack

ENHANCING DIGITAL OSCILLOSCOPE MEASUREMENTS

CLIVE DAVIS FROM YOKOGAWA EUROPE LOOKS AT SOME OF THE KEY AREAS OF OSCILLOSCOPE DEVELOPMENT, SUCH AS THE TREND FOR MIXED-SIGNAL TESTING, THE EVOLUTION OF NEW WAVEFORM ACQUISITION TECHNIQUES AND THE GROWING AREA OF SERIAL-BUS TECHNOLOGY

The oscilloscope has been the measurement tool of choice for examining time-varying signals in a variety of electronics applications. As industry evolves to meet the demands of sectors such as consumer electronics and telecommunications, so oscilloscopes are evolving to meet new challenges in both analogue and digital measurements.

The worldwide boom in consumer electronics has placed an increased emphasis on the need for sophisticated designs that combine both analogue and digital technology. Such projects are characterised by short development cycles, market pressures for low cost products and the need for devices that combine flexibility and low power consumption. The circuits involved in these designs increasingly include advanced components such as Flash CPUs, FPGAs, CPLDs and Flash memories, and the debugging of these circuits involves engineers looking at analogue as well as digital characteristics of signals.

The tools of choice to carry out debugging and analysis in mixed analogue and digital signal environments have been the oscilloscope to look at the analogue aspects and the logic analyser to look at multi-channel logic signals. However, as logic speeds increase and signal integrity issues increasingly relate to analogue effects on logic signals, there is an increased need for a single measurement tool that can look at both signal environments.

The Mixed-Signal Environment

Test and measurement (T&M) manufacturers have responded to this challenge by developing instruments known as 'mixed signal oscilloscopes', which combine a digital oscilloscope for looking at analogue waveforms with digital inputs that allow logic channels to be viewed at the same time. However, to date, these instruments have suffered from some significant limitations, since the main emphasis has been on the analogue side.

In particular, existing mixed-signal oscilloscopes have been equipped with only a limited number of logic inputs as standard (typically 16), which has resulted in a poor display for logic signals, no analysis features for logic signals and a slow display refresh rate.

Such instruments are clearly becoming inadequate for today's digital consumer electronics and automotive market sectors, where the demands of high-performance multimedia applications and the networking environment mean that 16-bit embedded processors are rapidly being succeeded by 32-bit devices. Even domestic appliances are moving towards the use of 16-bit processors. At the same time, the number of I/O ports on embedded processors is increasing, to dozens in many cases.

In such circumstances, even 16 logic channels in a measuring instrument are not enough to analyse address and data bus signals, or to analyse a number of I/O ports on an embedded processor. Moreover, engineers familiar with logic analysers want to have full bus display and state analysis capabilities, along with a fast refresh rate on the logic display.

A further challenge is presented by the increased resolution of modern analogue/digital and digital/analogue convertors, typically 10 to 12 bits for video and imaging applications and 20 bits or more for audio applications. Again, 16 bits are not enough to analyse the data bus

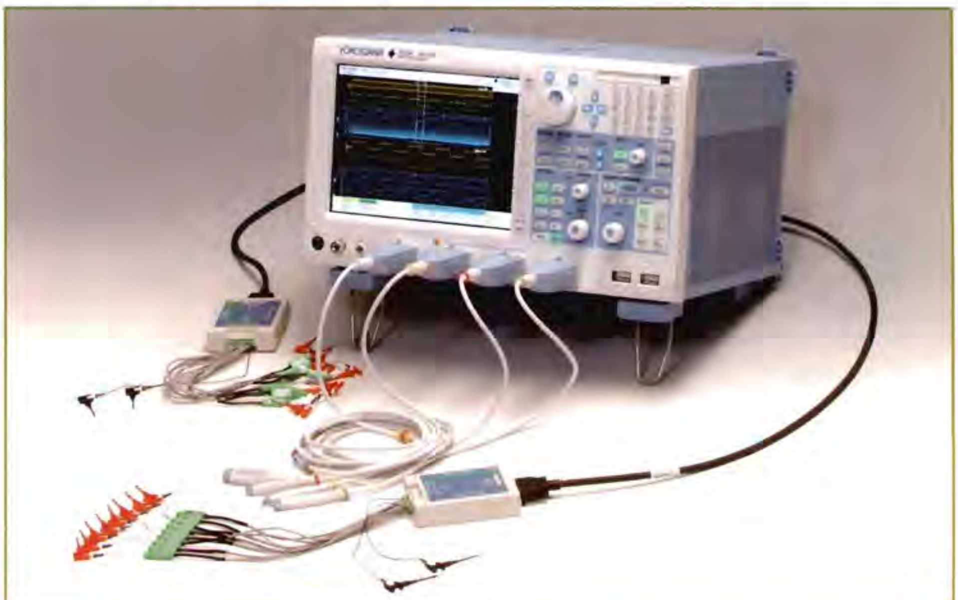


Figure 1: *The Yokogawa SignalXplorer DL9710L is a mixed-signal oscilloscope which combines four 1GHz analogue channels with a 32-bit logic input*

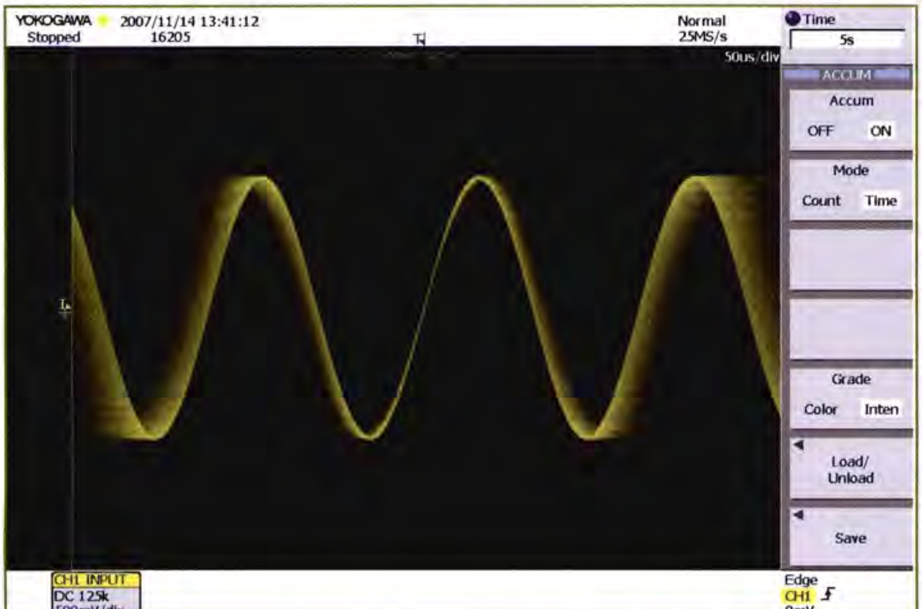


Figure 2: *Image obtained image when waveforms fade and are deleted over the passage of time*

Figure 3: *The ADSE (Advanced Digital Stream Engine) circuit used for waveform processing in digital oscilloscopes*

together with the control bus of the A/D or D/A converter.

Improved Logic Capabilities
These challenges are now being addressed by a new generation of oscilloscopes which combine four analogue channels with 32 bits of logic input. In the instrument shown in **Figure 1**, for example, each analogue channel has a bandwidth of 1GHz, and both analogue and logic inputs have a maximum sampling speed of 5GS/s. Other key performance parameters include a maximum 250MHz toggle rate, when used in conjunction with a high-speed logic probe, and a very high memory depth of 6.25Mword per channel, which is available at all times.

The 32-bit logic input means that these oscilloscopes are optimised for users who wish to analyse logic signals as well as analogue waveforms. In particular, they contain all the features required to analyse multi-channel logic signals, including bus display and state analysis, search and zoom capability, versatile triggering and digital/analogue calculations on logic signals.

Waveform Acquisition
While mixed-signal oscilloscope technology is opening up new application areas for stand-alone instruments, there have also been a number of significant developments in waveform acquisition and display techniques. For example, the instrument shown in Figure 1 has a waveform acquisition update rate of up to 25,000 waveforms per second and incorporates a history memory, which allows the user to recall and display previously acquired data from up to 2000 screens' worth of past waveforms. This ability to redisplay and subsequently analyse data offers significant benefits in troubleshooting and analysis.

One common application sector in which these developments are relevant is the observation of the 'eye pattern' in a transmission channel using an accumulation function. An eye pattern is typically an oscilloscope display in which waveforms of various symbol patterns are superimposed and is not limited to inter-device communication channel signals.

For general logic-circuit applications, observing the eye pattern of several superimposed waveforms can provide valuable information on the physical properties of a signal in the circuit. Parameters such as timing and level can be intuitively obtained, and the eye pattern can be used for debugging of the logic circuit's physical layer. In such applications, it is important for the observer to be able to quickly identify changes in the signal.

To allow this to happen, the accumulation time of the oscilloscope is normally set so that past waveforms that are not required are automatically deleted. This time-based accumulation operation means that, as new bitmap waveforms are plotted one by one, the brightness of ageing waveforms gradually wanes over time until finally the oldest waveforms are deleted.

Another way of observing eye patterns is to use the history memory function mentioned above. With this function, in situations where the memory used for each individual waveform is smaller than the amount of memory that can be assigned to its channel, past waveforms that were previously obtained and

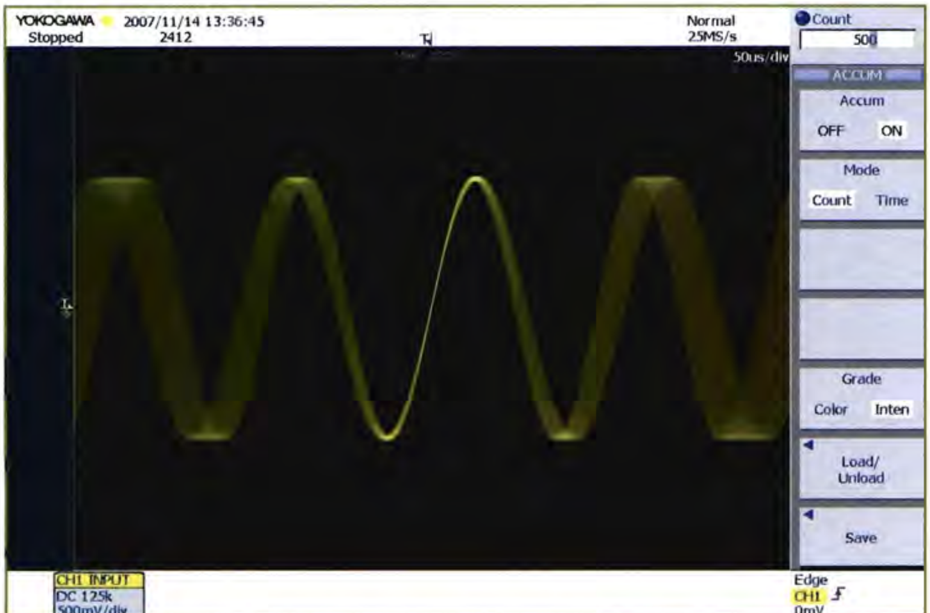


Figure 4: Image in which 500 waveforms are overlapped with the same weight and the degree of overlapping of sample points is assigned a brightness. In this example, the number of data points per single waveform is 12.5k

displayed are held in memory as long as capacity allows. Once waveform acquisition stops, it is possible to search for and display waveforms from memory in a superimposed fashion (**Figure 2**).

The disadvantage of this approach lies in the fact that an enormous amount of data must be processed to generate this image. With conventional oscilloscope models, the user becomes limited by the signal processing speed. Moreover, this way of superimposing waveforms is not practical for continuous waveform observations.

Signal Processing

Now, however, through the development of high-performance signal processing ICs (**Figure 3**), it is possible to implement (in addition to the conventional accumulation function) a function in which an image identical to overwritten history waveforms can be dynamically and continuously generated in parallel with waveform acquisition.

The number of waveforms that can be superimposed using this method is the same as the number of waveforms that can be handled by the history function. If this range is not exceeded, every time a phenomenon occurs it is developed into a bitmap; the number of sample points overlapped on each pixel is then counted, converted to colour or brightness, and used to generate an image.

With this approach, the waveforms are accumulated and displayed, but the impression given by each image is different. When waveforms disappear over time, the image reflects the order in which phenomena occur. On the other hand, when points of the same weight are overlapped, the image reflects the density of sample points (**Figure 4**).

The difference between these two methods can, thus, be summarised by saying that the 'deletion over time' method is appropriate for observing the order of phenomena, while the 'superimposing/equal weighting' method is best for observing the overlapping properties of waveforms.

Regardless of which accumulate operation is employed, the accumulated waveform is sent as an image to the oscilloscope screen for display, so it is possible to acquire and display a large quantity of waveforms without experiencing limits due to the frequency of operation (50 or 60Hz) of the LCD. For 12.5ksample points per waveform, waveforms can be acquired and displayed continuously up to a trigger rate of approximately 9kHz; for waveforms with 2.5ksample points, the figure is 25kHz.

Even if this trigger rate is applied to four channels simultaneously, the result is the same as for only one channel, so, if there are 12.5 points per waveform on four channels, there are 450Mpoints being processed every second by the whole system. The fact, that such a large amount of data can be continuously displayed is very important in helping the observer to grasp the behaviour of the item under test.

This accumulation function means that the instrument can be used with higher-speed triggering. Furthermore, for observations of phenomena in which dead time between triggers poses a problem, there is also a function that allows the use of trigger signals at a dead time of 400ns, which is equivalent to a waveform acquisition rate of 2.5MHz. Data is accumulated in memory until the assigned

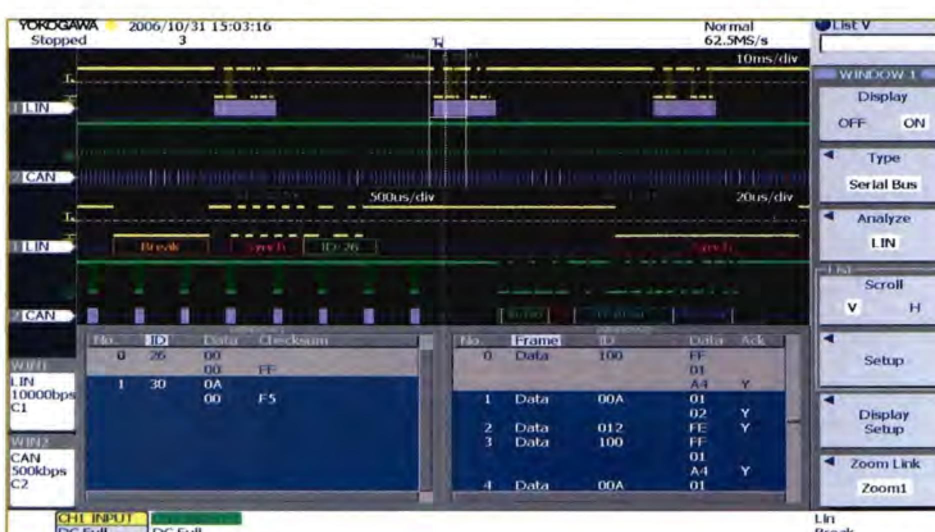


Figure 5: Simultaneous real time decode, analysis and zoom of a LIN bus and a CAN bus

number of acquisitions is met. By removing display processing time between acquisitions, it provides the fastest way to capture signals. Once all the signals are captured, every single acquisition can be viewed and analysed using the history function.

Reference Waveforms

One way of using a digital oscilloscope is to display previously acquired waveforms as reference waveforms for comparison with current conditions. With the enhanced accumulation function described above, the data that can be handled as reference waveforms is expanded to include not only recent waveforms but also multiple past waveforms in history memory. As a result, in addition to multi-waveform images being moved in the vertical position in the same way as conventional reference waveforms, other options are also available: for example, displaying average values from the data of the multiple waveforms, or selecting one of those waveforms for display.

The large number of sample points per second increases the likelihood of capturing rarely occurring phenomena. This is a factor in ascertaining the operating conditions in a circuit in a short period of time, but it is also important for generating an image from a large number of sample points from which one can extract a lot of information. The degree of sample-point overlap can be expressed as brightness or colour, which, when displayed on a wide viewing-angle LCD panel, allows the user to intuitively grasp the characteristics of the phenomenon. As all waveforms are available in memory, detailed measurement and analysis can also be carried out on the individual waveforms which contain anomalies.

Serial Bus Measurements

In addition to being ideal instruments for physical-layer waveform analysis, oscilloscopes are also ideally suited to protocol analysis of common serial data buses such as I^2C (Inter-Integrated Circuit), SPI (Serial Peripheral Interface), CAN (Controller Area Network) and the Flexray automotive bus.

Serial data bus problems come in many forms. However, most bus problems can be classified either as noise, signal quality, timing, or data errors. Signal noise on a data bus can lead to a number of problems and is typically more problematic on high-speed buses, densely populated circuit boards and at lower signal voltage levels. Since these are all trends occurring in today's electronics, noise is a common problem in bus designs. Common noise sources include crosstalk from other signals, radiation from elsewhere (EMI) and switching noise from a power supply.

Signal quality is a general term referring to the overall behaviour of a signal relative to ideal conditions. Waveform quality problems come in many forms, but some of the most common problems are signal levels that are too high or too low, overshoot and undershoot, and rise/fall times that are too slow or too fast. An example of a waveform quality problem is a data signal that has a rise time that is too slow so that, at the time of the clock pulse when the data is to be read, the data signal has not yet risen to a sufficient voltage level and the data is read incorrectly as a 0 instead of a 1.

Signal timing on a bus is another common source of errors and frustration. In the most basic sense, timing problems refer to events on one or more waveforms not occurring at the desired time. For example, a bus specification may refer to data packets occurring no more frequently than every 400us. If two data packets occur less than 400us, the processor may not have sufficient time to process the data. Other timing errors include setup and hold violations.

Data errors simply refer to incorrect data flowing on the bus. Data errors can be a result of a software problem, a damaged IC or any number of other hardware problems. Data errors result in ICs sending and/or receiving incorrect data, data incorrectly addressed to the wrong IC, etc. Even if all the other errors discussed above are under control, but data errors exist, then there will be problems.

Several different types of test equipment have been developed for detecting and analysing the different errors discussed above. Depending on what needs to be looked at, what types of equipment are available and the user's level of comfort with the different types of equipment, the options could include various combinations of oscilloscopes, logic analysers or protocol analysers.

While logic analysers, dedicated bus-specific protocol analysers and digital oscilloscope each offer varying degrees of insight into the problems discussed above, no single piece of test equipment is perfect for identifying or analysing all these different problems.

A logic analyser, while ideal for identifying complex timing issues, does not offer much help in the way of seeing noise or waveform quality problems. Similarly, a dedicated protocol analyser is perfect for identifying exactly what information is flowing on the bus and when it occurs, but it will typically not help to identify a noise or waveform quality issue.

A digital oscilloscope, on the other hand, is certainly more versatile than a logic analyser or protocol analyser, but in its basic form it is still lacking. While oscilloscopes are excellent tools for identifying noise, waveform quality problems and even many timing problems, traditional oscilloscopes do not provide the appropriate insight into the bus protocol. By adding serial data bus triggering and protocol analysis software, however, the oscilloscope takes a big step forward towards being the perfect tool for serial bus analysis.

These additional functions make it easy to discriminate between partial software failures and physical-layer waveform problems when troubleshooting systems by observing the physical-layer characteristics of signals. With the dual-window zoom function now available on some oscilloscopes, it becomes possible to simultaneously analyse and display waveforms from buses running at different speeds (**Figure 5**). Similarly, eye-diagram analysis can be used in conjunction with mask test functions for evaluating the signal quality of data communication in serial buses.

New Generation

The extensive use of ASICs, particularly high-performance signal processing ICs, which store the acquisition data and perform computation, enable the latest generation of digital oscilloscopes to capture waveforms with high acquisition rates, to perform measurements on each individual waveform and to carry out computation and analysis in real time with little or no reduction in performance. These capabilities make it possible for oscilloscopes to meet the new challenges in both analogue and digital measurements. ■

PROTECTION AGAINST DPA AND RELATED ATTACKS

PAUL KOCHER OF CRYPTOGRAPHY RESEARCH IN THE US EXPLAINS HOW TO PROTECT YOUR DEVICES AGAINST POWER ANALYSIS ATTACKS

To be secure, tamper resistant cryptographic devices must be protected against simple power analysis (SPA) and differential power analysis (DPA), including variants such as high-order DPA. (For an introduction to SPA and DPA, see P. Kocher, J. Jaffe, and B. Jun's *"Differential Power Analysis" Advances in Cryptology — Proceedings of Crypto '99*, Lecture Notes in Computer Science, Vol. 1666, Springer-Verlag, 1999, pp388-397.)

Independent testing processes are essential for validating the presence and effectiveness of these countermeasures. Testing methodologies for power analysis vulnerabilities can yield varying degrees of assurance as to the security of the device under test. While insecurity can be demonstrated conclusively, evidence of security is more open-ended.

Confidence in a security evaluation depends on many factors including the comprehensiveness of the evaluation, the skill of the evaluator, the nature of the device's design and the difficulty of exploiting any identified vulnerabilities. This article reviews testing strategies for power analysis and related attacks, including black box and clear box methods. The article also examines how appropriate design architectures and evaluation approaches can be combined to yield the strongest evidence of a device's security.

Security Evaluation

In general, the goal of a security evaluation is to assess the likelihood that a device or system meets some defined security objectives. This process involves analysing both the design and the process used to produce it. For example, a product that has been carefully designed and tested by experienced experts has higher assurance (i.e. a lower probability of failing) than one haphazardly put together by a novice, even if neither has any known defects. While validation efforts may uncover security defects, in which case there is typically zero assurance of security, this article focuses on the question of how to attain assurance in the security of a device that does not have any known defects.

DPA testing presents special testing challenges. Conventional security testing efforts tend to focus on logical characteristics of digital systems and focus on individual layers in a design. In contrast, power analysis attacks combine several disciplines, including transistor physics, cryptanalysis, digital circuit design, statistics, software development, data acquisition and analogue signal processing. The reason for this is that the security issues underlying DPA cross multiple layers of abstraction. At the lowest level, a transistor's power consumption depends on its switching activity and state. A circuit's power consumption depends on the activity of all its transistors and other elements. Ultimately, the power consumption of a device observed during a cryptographic operation is a combination of myriad details related to its software and hardware implementations.

DPA attacks use statistical techniques to turn this complexity to the advantage of the adversary. In particular, attackers can determine secret keys by detecting minute correlations in power consumption measurements, even if the effects of interest are dominated by unrelated "noise" in the measurements. The goal of a validation effort is to assess whether there could be any compromising signals buried in this noise.

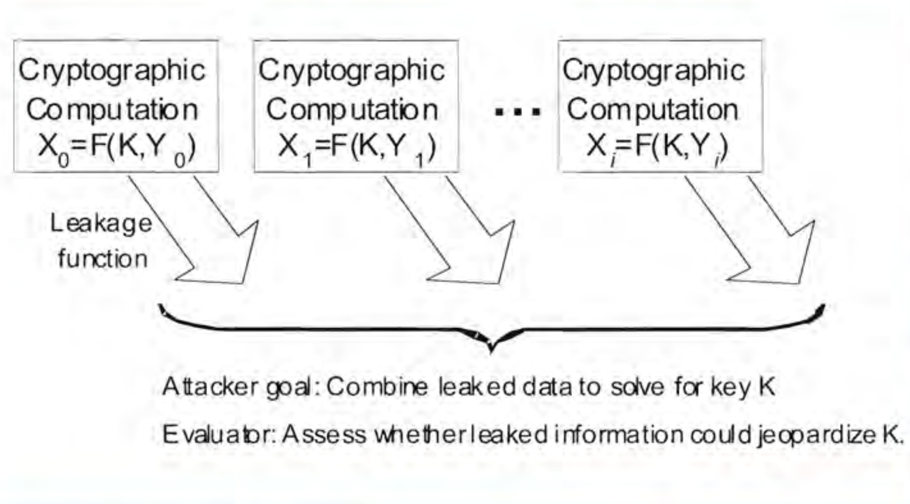


Figure 1: *Assessing the device's state*

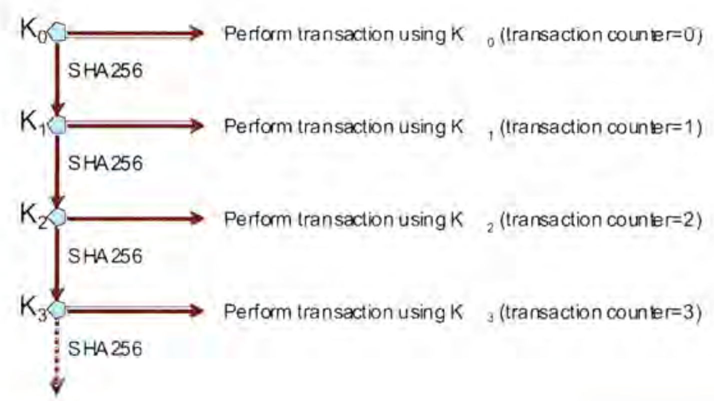


Figure 2: *Leak-resistant cryptographic key update protocol*

From an evaluator's perspective, variations in a device's power consumption can be thought of as a covert channel that provides some - perhaps very complex and noisy - 'leakage function' of the device's state. Variations in actual power measurements can include both entropy (e.g. due to unknown processes or random measurement errors), as well as useful leaked information. The leaked information can include correlations to inputs, outputs, state transitions, intermediates and other elements of the device state. The attacker's goal is to find a way to use the leaked information to find the secret key.

The evaluator has the task of assessing whether information is being leaked that could compromise keys or other secrets. The feasibility and reliability of this assessment depends on many factors, including the evaluation process and the device design (see **Figure 1**). In general, most devices are too complex to completely model the applicable leakage functions, but evaluations can still provide valuable information as to how secure devices are and the risk of compromise.

Black Box Testing: Simple but Limited

For some applications, it is sufficient to have an experienced testing lab perform black-box testing of a product and report whether keys were extracted. The device is deemed to pass testing if the lab is unable to extract the keys.

A basic black-box DPA evaluation uses power traces to infer information about a device's cryptographic implementation, including any DPA countermeasures. The analysis typically involves forming and testing hypotheses about how the target device operates. As a result, problems are unlikely to be detected unless the tester has a strong understanding of the range of possible implementation techniques and countermeasures that might be present.

With respect to lab capabilities, black box testing typically requires using high-speed deep-memory analogue waveform collection equipment along with specialised high-speed software tools for creating selection functions. Tools for averaging, analysing and visualising multi-gigabyte datasets are also needed.

Informal black box DPA testing methodologies have several practical advantages. Product vendors do not need to reveal proprietary design information. Evaluation results tend to be unambiguous; either the device was broken or not. Evaluation laboratories are able to focus on attack strategies that they feel are the most likely to yield results. Labs can also update their test processes quickly as new attack strategies become known. Because minimal documentation and overhead are required, testing can also be relatively inexpensive.

Despite these advantages, black box DPA testing has major limitations. Results tend to be inconsistent, as inexperienced labs will miss flaws that more knowledgeable labs would find. Vendors have been known to choose weaker labs which will have lower costs and higher pass rates, making lab staffing and training a difficult problem. Black box DPA testing also requires expertise that has not traditionally been required for security evaluations of cryptographic devices, such as strong applied number theoretic knowledge. Black box DPA testing is also relatively inefficient and can easily miss vulnerabilities. For example, many countermeasures that might pass "cookbook" black-box DPA testing can be broken by adversaries who know the countermeasure design.

Despite these limitations, most products tested for power analysis at Cryptography Research fail during black box testing. Although such black box testing cannot provide conclusive evidence of a product's security, the process can provide a useful and cost-effective way to differentiate products with at least a moderate level of protection from those that are highly vulnerable.

Basic Clear Box Testing

In a clear box test, the evaluator's objective is to verify evidence provided by a device's designer as to why a device is resistant to attack. Unlike a black box test, the evaluator is assumed to have comprehensive design information about the device.

Clear box evaluations make more efficient use of testing resources than black box evaluations. Testing labs can avoid much of the time-consuming trial-and-error guesswork that black box testing often requires to infer how devices operate. Of course, the benefit directly depends on the quality of the documentation; poorly written or incomplete documentation is of little value. Evaluation efficiency is also increased if vendors provide detailed security claims and justifications for those claims. In this way, evaluators can focus on verifying product designers' results, as opposed to having to search for hidden flaws.

Clear box evaluations are generally easier to conduct than comparable black box evaluations. Less knowledge of implementation techniques and countermeasures is required, since evaluators only have to understand the specific techniques used in a given product as opposed to the universe of possible techniques. Similarly, the amount of data that needs to be collected and processed is typically reduced, since clearly irrelevant experiments can generally be avoided.

The strength of the evidence that can be obtained largely depends on a product's design. For devices that reflect ad-hoc or incompletely documented countermeasures, evaluations are generally limited by the lack of a testable scientific basis for the security claims. As a result, evaluation results typically rely on labs' informed opinions as to whether the techniques employed are appropriate. Even in these cases, a good clear box evaluation can help provide confidence that the security will not fail under black box DPA testing by an adversary with limited resources.

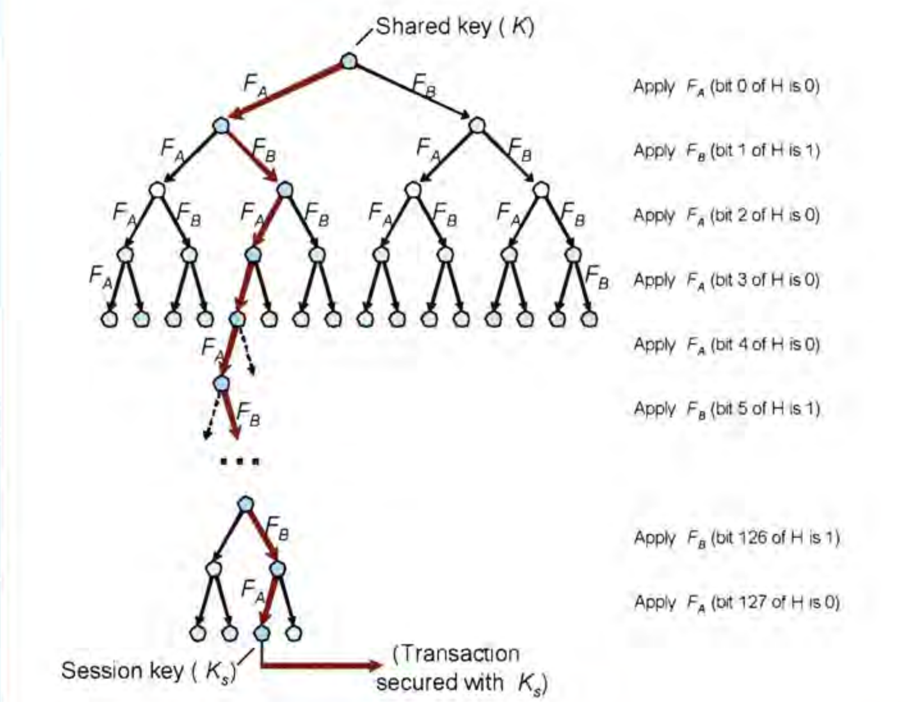


Figure 3: *For each bit of H, the key is transformed in one of two ways, by applying one of two different hash operations, F_A or F_B*

Protocols that Withstand Leakage

To gain higher levels of assurance, devices can use cryptographic constructions that preserve security even if some information about the keys is leaked to adversaries. These approaches can provide fundamentally higher confidence than ad-hoc methods, since they provide a testable justification for the security claims.

In particular, protocol designers can provide cryptographic arguments showing that a given design can survive leakage up to a defined threshold leakage rate; manufacturers can then provide engineering evidence that the product's leakage rate is below the threshold. The validation process consists of verifying the properties of the cryptographic protocols and verifying that the implementation leaks less than this amount of information, hopefully with a substantial safety margin.

Unfortunately, most protocols today are not designed to withstand leakage. For example, conventional protocols that compute session keys by encrypting a counter or hashing a key with a nonce can be attacked using DPA because each counter/nonce value potentially reveals new information about the key to the adversary. As a result, even leaks that reveal tiny amounts of information per transaction, even as low as one thousandth of a bit or less, can compromise secret keys when attackers combine observations from many transactions. For smart cards and similar small devices, there is no reliable way to ensure that tiny leaks do not exist.

Fortunately, protocols that can survive information leakage can be easy to implement. For example, consider a protocol - P. Kocher, *"Leak Resistant Cryptographic Indexed Key Update"*, US Patent No. 6,539,092, where a smart card updates a 256-bit key with SHA256 before each transaction with a server. Each SHA256 update destroys the usefulness of previously leaked partial information to the adversary.

If L_0 is the upper bound on the amount of information (in bits) leaked per SHA256 key update and L_1 is the maximum amount of information leaked per transaction, then the overall cryptographic security is $256\text{-}2L_0\text{-}L_1$ bits. Note that the information content of a leak can be measured in bits even if the leak is probabilistic. L_0 is counted twice, since adversaries could utilise information leaked from both the SHA256 operation before the transaction and SHA256 operation afterward (see **Figure 2**).

In this protocol, it does not matter what information is leaked, provided that the quantity of information obtained is less than the required bound.

Even if the adversary can choose any L_0 bits of information from the computation K_2=SHA256(K_1), the net usable leak will be bounded by $2L_0+L_1$, provided that the leak from SHA256 does not reveal useful information about K_0 or K_3. The update step redistributes un-leaked entropy in the key making it computationally infeasible for an adversary to combine information leaked prior to the start of the update step with information leaked after the conclusion of the update step.

Protocols that can survive leakage can also be defined for applications where there is not a server, such as secure radios. In an example of such a protocol, two or more parties who wish to communicate can generate a shared 128-bit unique value H, for example by hashing random contributions from each participant, then use H to select a sequence of hash operations to transform a shared key K, which must be secured against DPA, into a session key K_S. For each bit of H, the key is transformed in one of two ways, by applying one of two different hash operations, F_A or F_B (see **Figure 3**).

Each intermediate state is only used in three possible ways: it can be derived as the result of either F_A or F_B, can be transformed with F_A, and can be transformed with F_B. Adversaries can observe each of these operations many times, but these computations will not vary. For example, no other data is mixed in. As a result, there are no variable intermediate values for DPA selections functions to exploit. Because selection functions cannot be applied, DPA-type attacks are no longer applicable.

Let L_0 be the maximum number of bits of secret information leaked from each of F_A and F_B for any given input. This is a somewhat more restrictive assumption than used for the iterated SHA256 example, since the adversary is assumed to be able to obtain at most L_0 bits about the input no matter how many times the input is transformed.

Let L_1 be the maximum number of bits of secret information leaked from each transaction using K_S. The adversary can thus obtain at most $2L_0$ bits of information about K, $3L_0$ bits of information about any intermediate, and L_0+L_1 bits of information about any K_S. The initial step of deriving H provides each participant with assurance that K_S values will not be used more than once, even if the other participant chooses its contribution to H maliciously.

Update processes can also be defined for public key algorithms. For example, RSA private key operations can be implemented with key update steps. Update techniques for public key algorithms typically involve encoding the private key as a relationship among a set of randomised parameters. The security of the private key depends on keeping this relationship secret, so it is important that the leakage does not reveal information about the relationship, including if the adversary uses high-order attacks.

High-Assurance Validation

To validate a leak-tolerant device's protection against information leakage attacks, the evaluation lab should begin with the designer's security claims. The general process for the evaluation lab then involves the following two steps:

1. Verifying that the designer has made correct claims about the leak tolerance properties of the device's protocols.
2. Verifying that the hardware does not leak in ways that violate the protocol's assumptions and that there is a suitable safety margin.

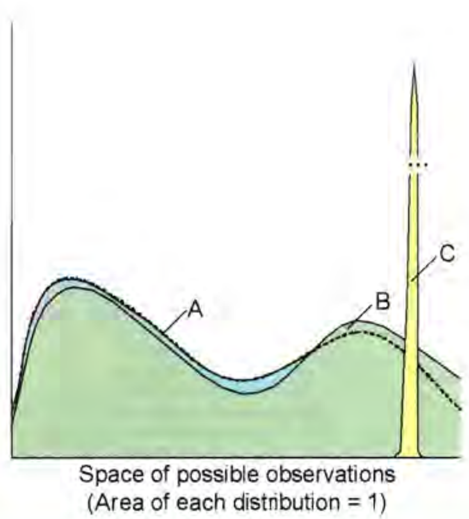
The first step consists of evaluating the designer's claims about the device's cryptographic design. For example, if the designer claims that cryptographic strength of 90 bits is maintained with leakage of up to 5 bits per transaction, this should be verified. Evaluators should pay particular attention to the case where adversaries interrupt transactions, e.g. by disconnecting the target device's power during computations.

As part reviewing the protocol, the evaluator should also verify that the designer has completely documented any forms of leakage that must not occur. There will generally be some leakage functions that the cryptography requires will not exist, although these may be so absurd as to pose no practical risk. For example, it is quite reasonable to assume that L_0 bits of information leaked from the computation K_2=SHA256(K_1) will not reveal any useful information about the value of K_3 (which has not yet been computed). Assumptions about leakage functions for public key algorithms may require additional attention, as update operations may not be as effective at redistributing entropy.

The second part of the analysis involves characterising the actual information leaked from the device. The primary goal of this process is to establish an upper bound on the number of bits of information leaked from each transaction. This process is discussed further in the next section. This step should also review any forms of leakage that the design assumes do not exist to verify that these assumptions are correct.

Analysing Leakage Rates

It is impossible to measure the exact amount of useful information leaking from cryptographic device, but useful



Figures 4: Distinguishing measurements groups taken by using the same key/data

estimates can be produced. The typical characterisation process for devices with countermeasures is as follows:

1. Characterise the leakage from the device with countermeasures disabled.

2. Characterise how countermeasures affect leakage observations.

3. Estimate the overall leakage rate with the countermeasures in effect.

Preferably, the device designer should provide an assessment of the device so that the evaluator can focus on validating security claims.

For step 1, it is particularly important to disable randomising countermeasures, since these are otherwise very difficult to distinguish from serious (but as-yet uncharacterised) leaks. Countermeasures that attenuate leaked information (e.g. filters, balancing, etc) are also helpful to disable, but this is typically not as important.

For step 2, the objective is to characterise how countermeasures affect observations. For countermeasures that use randomness, it is important to verify that the source of the randomness is independent of the secrets and intermediates being protected and cannot be filtered out, for example in the temporal or frequency domains. Protocols that rely on limiting the leakage per input, as opposed to per operation, require a more careful evaluation of randomising countermeasures.

The effect of countermeasures that generate noise or random fluctuations should generally be discounted, since adversaries may be able to perform many transactions with each input. Some countermeasures that statistically randomise the representation of data elements within the computation may actually cause each transaction to leak different information, instead of the same information each time, creating a vulnerability to high-order DPA.

For step 3, the ideal way to characterise the leakage rate is by measuring key/data dependent effects on the distribution of possible measurements. In general, if key-dependent variations are readily apparent, the leakage rate is very high. For devices that leak badly, the evaluator only needs to demonstrate that the leakage exceeds the cryptographic assumptions; actually quantifying the leakage rate is unnecessary.

In contrast, if groups of measurements using the same key/data cannot be distinguished from groups of operation using different keys, the observed leakage rate is low. The area of difference in the observed distributions determines the information content of the observations. For example, distributions A and B are similar and have relatively low information content, while A and C (or B and C) are largely dissimilar (see **Figure 4**).

It is important to note that the x-axis in the figure corresponds to the space of all *possible* measurements across a transaction, *not* power traces themselves. For example, a trace consisting of multiple points would be *one* measurement.

Several caveats need to be considered in the analysis, including:

1. The entire measurement space is generally too large to actually enumerate, so approximation techniques are required. These techniques can over or under-estimate the amount of information leaked.

2. Some keys and/or data inputs may give more information than others. Even if the average case is within the leakage rates tolerated by the cryptographic protocols, the worst case may not. Adversaries may be able to trigger worst-case leakage by choosing malicious inputs.

3. Uncharacterised leakage, whether in the same or different channels, can reveal more information to adversaries.

4. It may be possible to filter out countermeasures whose properties do not exactly match the characteristics of the actual signal.

5. Analogue characteristics of devices can change significantly between revisions, even if the change does not affect the digital functionality.

In general, these caveats need to be considered by the testing laboratory. These issues also make it important to have a comfortable safety margin between the leakage rates that can be tolerated by a device.

The Importance of Good Design

For some products, it is impossible to gain any assurance as to the security against DPA attacks. For example, if the protocols allow adversaries to observe thousands or millions of encryption operations using the same AES key, there is no practical way to verify that leakage rates are low enough to maintain security. Accordingly, such devices will always have some non-negligible risk.

Similarly, some key update processes for some public key algorithms do not provide verifiable protection against high-order DPA attacks, making it unlikely that an evaluation lab can ensure that the private key will remain secret after large numbers of uses. In other cases, systems are too complex to adequately review given the testing resources available. The designer's security claims or documentation may also be inadequate.

In situations where design limitations of these kinds exist, an evaluation lab cannot conclude with high-assurance that the device under test has effective protection against DPA and related attacks.

Efficiency of Testing

Power analysis attacks are non-invasive, fast and leave no physical evidence of tampering. They can be mounted without knowledge of a target's design. As a result, effective testing for DPA and related attacks is essential for devices that must operate securely in hostile environments.

The efficiency of an evaluation and, ultimately, the assurance obtained in a device's security, depends on the both the testing process and the design. Black box testing processes can provide a convenient way to reject devices with obvious flaws, but clear box testing is required to obtain much assurance in the testing result.

For the highest levels of assurance, devices can use cryptographic protocols designed to withstand leakage of up to a threshold amount of information, then evaluators can assess whether the actual implementation leaks less than this amount of information, with a reasonable safety margin. ■

IN THIS ARTICLE RIAZ SOBRANY PROVIDES AN OVERVIEW OF THE HIBRIDAS PHOTOIMAGEABLE THICK-FILM PROCESS AND THE EQUIPMENT INVOLVED IN SETTING UP A SMALL SCALE CIRCUIT FABRICATION FACILITY

THE HIBRIDAS PHOTOIMAGEABLE THICK-FILM PROCESS

A novel process for manufacturing electronic circuits using photosensitive metal and dielectric pastes was developed during the early 1980s by the microelectronics department of the Research Institute for Radiomeasurement (now Hibridas Enterprise Ltd) in Kaunas, Lithuania, which resulted in two Soviet Union patents being awarded in 1986 for the photosensitive dielectric composition and the photosensitive conductor composition.

During 2003, the photosensitive pastes were used to fabricate a number of microwave circuits, including branch-line and rat-race couplers operating up to 110GHz at the University of Surrey.

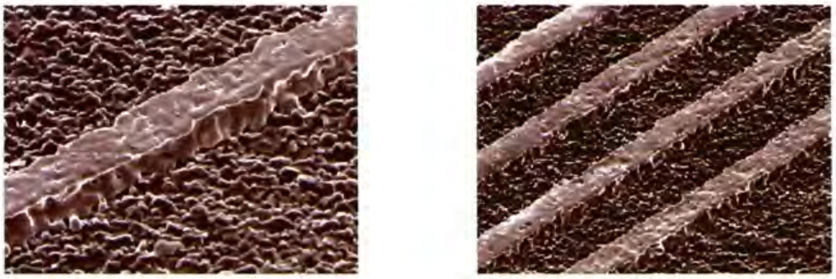


Figure 1: *Photographs of 20µm wide conductor tracks formed using the HC4700 silver paste*

Materials Used in the Hibridas Process

A photosensitive dielectric paste and a variety of photosensitive metal pastes including silver, gold, and platinum are manufactured by Hibridas. The metal pastes are comprised of a metal powder, glass frit, a ceramic powder, an organic binder and a photosensitive vehicle suspended in an organic solvent.

The dielectric paste consists of crystallising glass frit, a ceramic powder, an organic binder and a photosensitive vehicle suspended in an organic solvent. Notable properties of the photosensitive pastes include:

1. Good electrical conductivity for the metal pastes;
2. Low dielectric loss for the dielectric paste;
3. Extremely fine line and conductor capability (20-30µm);
4. Well-defined conductor edges and low surface roughness;
5. Low sensitivity to daylight, so no special lighting conditions are required in the processing area;
6. Low sensitivity to the effects of oxygen, so an inert atmosphere is not required in the processing area;
7. An absence of photopolymerisable side chains in the photosensitive vehicle.

Physical properties of the HD1000 dielectric paste and the HC4700 silver paste after firing are listed in **Tables 1** and **2**.

The photoimageable thick-film process separates the screen printing of pastes from the circuit pattern generation. Pastes are blank-printed onto substrates rather than printed with a patterned mesh. Therefore, the levelling properties of the Hibridas photosensitive pastes are optimised to produce a uniform thick film with a very smooth and dense surface, free of pinholes and screen mesh marks after printing.

A photoresist is not required because when a photosensitive paste is exposed to UV light, the photosensitive vehicle

Approximate fired thickness	7-9µm
Resistivity	3-4mΩ/square
Minimum trace/gap resolution	15µm/20µm
Solderability	Yes
Optimum printing temperature	20-23°C

Table 1: *Typical fired properties of the HC4700 silver paste*

Approximate fired thickness	12-13µm
Dielectric constant	8.0
Loss tangent	0.002
Breakdown voltage	15V/µm
Minimum via hole size	70µm x 70µm
Fired colour	Pale blue
Optimum printing temperature	20-23°C

Table 2: *Typical fired properties of the HD1000 dielectric paste*

polymerises and hardens. By proper use of a UV opaque photomask, it is possible to selectively expose areas of paste printed on a substrate. Unexposed paste is soluble in dilute monoethanol amine solution, whereas polymerised paste is insoluble and remains on the substrate. The handling of unexposed pastes can be performed under normal lighting and atmospheric conditions although care should be taken to avoid exposing the pastes to direct sunlight.

Thick-film pastes have a tendency to settle during storage, so prior to printing the paste should be thoroughly mixed by slow and gentle hand stirring for two minutes with a plastic or stainless steel spatula. An automatic stirrer can also be used, but stirring speeds must be slow as high speeds will beat air into the paste which results in voids in the print. Stirring reduces the viscosity of a thick-film paste, but if the viscosity of a well stirred paste is too high to achieve a sufficiently smooth wet print, then a further reduction in viscosity can be achieved by adding a small amount of benzyl alcohol to a jar of paste and mixing it in. The amount of benzyl alcohol added should be as small as possible as it reduces the percentage mass of solids in the paste which results in an increase in the porosity of fired structures.

Brookfield viscometers are the most commonly used equipment for measuring the viscosity of thick-film pastes.

CoorsTek ADS-96R alumina substrates with properties listed in **Table 3** are approved by Hibridas for use with their pastes. Alumina is an ideal substrate material as it offers the following characteristics:

- High dielectric constant
- Low loss tangent
- Fine surface finish
- Low toxicity
- High inertness
- Low temperature expansion coefficient
- High resistance to warping
- High stiffness.

Before printing, a substrate should be degreased using acetone and spray rinsed with deionised water. It is of utmost importance that the substates are completely dry before use otherwise the pastes will not stick.

Figure 1 shows a photograph using a microscope of 20µm wide conductor tracks formed using the HC4700 silver paste on a CoorsTek ADS-96R alumina substrate. It is noticeable that the conductors have near vertical edges and flat tops.

Composition	96% alumina
Dimensions	2in x 2in
Thickness	635µm
Dielectric constant	9.8
Loss tangent	0.001
Surface roughness	0.89µm
Grain size	3-7µm
Hardness (ASTM-E18, R45N)	82

Table 3: *Properties of the CoorsTek ADS-96R alumina substrates*

Fabrication of Circuits

The process steps required to fabricate circuits with a single layer of metallisation using the Hibridas photosensitive pastes are illustrated in **Figure 4** and explained as follows:

Printing of photoimageable thick-film pastes is carried out using an automatic screen printing machine fitted with a blank (unpatterned) mesh, which operates using the off-contact process where only the section of the screen that is directly under the squeegee is in contact with the substrate.

Figure 2: *Hibridas UV light exposure unit MA3*

Figure 3: *Hibridas developing unit SC4*

Screen printing by hand is acceptable for decorative purposes but totally unacceptable for producing thick-film circuits as it is impossible to ensure uniform printing. In fact, the primary purpose of a printing machine is to produce uniform prints. Thick-film pastes are most commonly printed using a squeegee with a minimum hardness of 65 Shore to ensure well defined edges when a patterned screen is used, but this is not

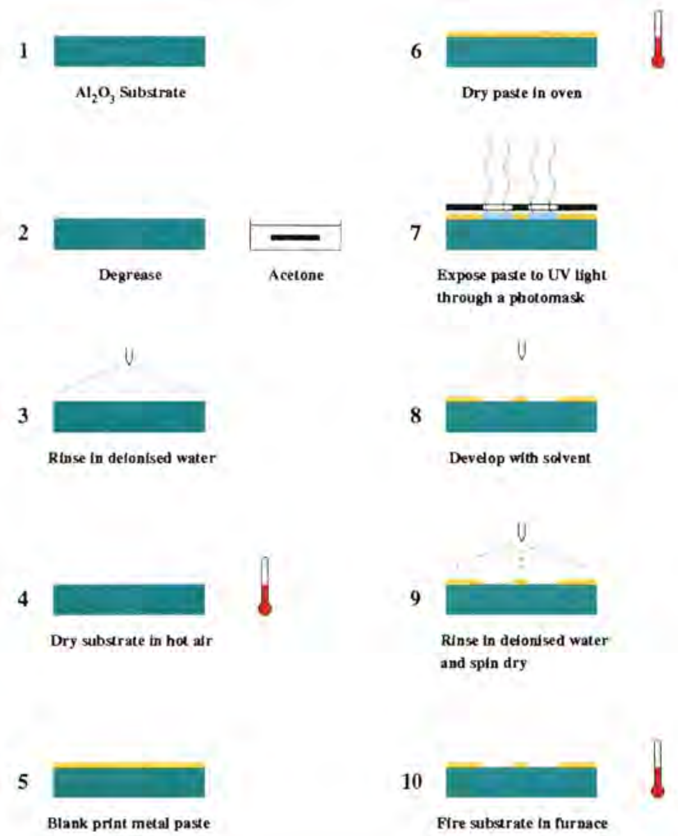


Figure 4: *Process sequence for fabricating circuits using the Hibridas photosensitive pastes*

a requirement when blank printing pastes, so a softer squeegee is recommended in order to reduce pinholes in the print. Hibridas recommends the use of screens fitted with a stainless steel mesh, although a nylon or polyester mesh may be preferable as metal meshes have a tendency to contaminate substrates and dielectric layers with metal particles.

Optimum printing characteristics are achieved in the temperature range 20-23°C. The HD1000 dielectric paste is printed with a 200 mesh screen using a double wet pass and the metal pastes are printed with a 325 or 250 mesh screen using a double wet pass. A double wet pass is required to ensure a uniform coating of the substrate.

The thickness of wet prints using the metal pastes is typically in the region of 15-20μm, depending on the settings of the screen printing machine and the mesh used. A useful article written by the staff of DEK Printing Machines about screen printing for manufacturing thick-film circuits serves as an excellent introduction for those unfamiliar with the screen printing process (A. Hobby, ***"Printing Thick Film Hybrids"*** DEK Printing Machines Ltd, 1997 or online available at **www.g-e-m.com/info/hybrid/hybrid.html).**

After printing, the substrate is placed in a drying oven with a temperature of 80°C for about 10-15 minutes to dry the paste by evaporating the solvents. Optimal drying conditions are critical as insufficient drying time results in tacky pastes that stick to the photomask during exposure as the photomask is held tightly against the substrate using a vacuum, and excessive drying times or too high a temperature deactivates the photosensitive vehicle. The time between drying and exposure should not exceed 24 hours in normal lighting conditions.

Pattern generation is performed by exposing the dried paste to high intensity UV light through a negative photomask of the circuit pattern. Areas of paste exposed to UV light harden as the photosensitive vehicle polymerises, and become insoluble in dilute monoethanol amine solution. The optimum wavelength for polymerisation of the photosensitive vehicle is in the region of 320-400nm produced by a 1-1.2kW metal halide UV light source.

Exposure times of 1-2 seconds are typical for the HD1000 dielectric paste, and 2-5 seconds for the HC4700 silver paste. Several companies manufacture UV light exposure units, but units manufactured by Hibridas such as the MA3 shown in **Figure 2** are recommended as they offer the facilities to vary the exposure time electronically and accurately align the photomask with the substrate. Exposure units manufactured by Hibridas employ a near contact technique where the photomask is adjusted to the alignment marks on the substrate and brought into near contact by a vacuum.

A near contact technique is required to produce structures with well defined edges as fringing of the UV light is minimised at the interface between the UV transparent and opaque regions of the photomask. UV light fringing is not completely eliminated and the minimum required exposure time should be used.

The operating procedure of the MA3 exposure unit is:

* Cool the platform using chilled water,
* Set the current to 12A;
* Switch on the UV lamp and leave for four minutes before using the exposure unit for the first time;
* Insert substrate and hold in place using the vacuum hold;
* Place photomask on top of the substrate;
* Align the photomask with the alignment marks on the substrate using the screw adjusters;

* Close drawer and expose the substrate to UV light;

* After exposure, open drawer and remove the photomask;

* Remove the substrate.

A spin developer with the facility to spray rinse and spin dry a substrate after developing is required for processing exposed metal and dielectric pastes. Hibridas developing units such as the SC4 shown in **Figure 3** are recommended because of the speed of rotation and the duration and pressure of the atomised spray are electronically controlled. Developing the exposed metal or dielectric paste layer is performed by spraying them with a high pressure atomised mist of aqueous 0.5wt.% monoethanol amine solution at a temperature between 15°C and 25°C, which dissolves the unexposed paste whilst leaving the exposed paste structures intact. Developing times are typically in the range of 4-7 seconds for the HD1000 dielectric paste and 2-4 seconds for the HC4700 silver paste.

Excessive etching will result in the metal and dielectric structures having coarse edges and broken fine metal traces. Developing is followed by rinsing the substrate with deionised water for 1-2 seconds and spin drying for approximately 15 seconds. The spray geometry is critical to ensure a regular and evenly spread film of developer solution over the spinning substrate.

Other important variables are the speed of rotation and the spray pressure. Experimental work at the University of Surrey using a Hibridas SC4 developing unit have determined that good results are achieved with a rotation speed of 2000-3500rpm, a spray air pressure of 3.5 bar, a developing solution spray pressure of 1 bar and a rinsing water spray pressure of 0.2-0.4 bar.

Firing should be performed in a well ventilated furnace capable of providing a controlled temperature profile. The flow of air should be of a magnitude and direction such that clean fresh air is drawn through the main firing sections to flush the heating zones of evaporated solvents and combustion products.

Ideally, a belt furnace is used although a cabinet furnace is acceptable for small scale production. Hibridas recommends a 60-minute firing cycle starting with a preheat to 300°C, followed by a temperature rise rate of 10°C/minute in the burn-out zone from 300°C to 500°C, and a peak firing temperature of 850°C for 10 minutes. The remaining time is occupied by a slow cooling off period. During firing, the photosensitive vehicle is volatised and burned off; the organic binders are removed by oxidisation; and the glass frit softens to wet the substrate, and bond the metal or ceramic particles to the substrate in a glass matrix.

It is important to remember that the drying stage fails to remove all of the solvents from the photoimageable pastes and any remaining solvent residue is evaporated during firing. If the substrate is heated excessively early on in the firing stage, then rapid evaporation of remaining solvents can cause laid down structure to crack or peel away from the substrate.

A thick-film circuit manufacturing facility requires a very clean and dust-free environment to prevent dust and airborne particles from contaminating the pastes whilst they are wet. Airborne particles contaminating dielectric layers burn off during firing, leaving voids which are easily filled with metal pastes from structures above the void and result in short circuits.

Clean room conditions are strongly recommended although not essential. Special lint-free wipers must be used for cleaning equipment with as tissue paper releases paper dust. Personnel working in a thick-film manufacturing facility should wear suitable overalls and headwear to prevent dust and fibres from their clothing from being released into the air.

Photomasks

High quality photomasks for use in UV light exposure systems are manufactured by coating one side of a glass panel with a thin layer of UV opaque material, followed by patterning the UV opaque material by chemical etching or laser engraving. Chromium is the traditional UV opaque material but has the disadvantage of being opaque in the visible band, which makes the alignment of the photomask with already laid down structures difficult. Iron oxide is opaque to UV light but transparent in the visible band, so is recommended for photomasks used to fabricate multilayer circuits.

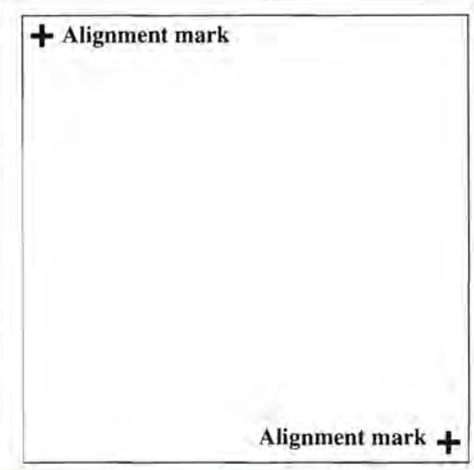


Figure 5: The location of the alignment marks on the substrate formed as part of the first metal layer

A critical factor when fabricating multilayer circuits is the alignment of structures on different layers. If structures on different layers are misaligned with respect to each other then the performance of the circuit will be degraded, and in many instances the circuit will be rendered inoperative.

Alignment tolerances between structures on different layers are typically of the order of a few microns for circuits operating at microwave frequencies, so a system of accurately aligning a photomask with the previously laid down structures is required. The photomask used to create the structures on the first metal layer is designed to produce a pair of alignment marks (also known as fiducial marks) located on opposite corners of the substrate as shown in **Figure 5**, which are used as reference points when positioning the photomasks used to create structures on higher level metal and dielectric layers.

It is essential that the alignment marks on the substrate are not overprinted with subsequent applications of metal and dielectric paste, otherwise they will be obscured. Photomasks used to create structures on higher level metal and dielectric layers include a pair of alignment marks as shown in **Figure 6** which are aligned with the alignment marks on the substrate by positioning the photomask in the Hibridas exposure unit using the screw adjusters.

Metal and Dielectric Layers' Fired Thicknesses

Approximate fired thicknesses of metal and dielectric layers are provided in the Hibridas technical data sheets, although in practice, the exact fired thicknesses of metal and dielectric layers is dependent upon the settings of the screen printing machine, the mesh and the firing profile. Microwave circuits are highly sensitive to the thickness of dielectric and, to a lesser extent, metal layers so it is important that accurate figures are obtained of the thicknesses of metal and dielectric layers produced using the equipment which will be used to fabricate the circuits.

The fired thicknesses of metal and dielectric structures printed using two wet passes with a DEK 1202 screen printing machine, directly onto CoorsTek ADS-96R alumina substrates, were measured using a Talystep profilometer. The thickness of the metal structures ranged from 6.0-6.1µm and the thickness of the dielectric structures ranged from 9.8-10.0µm.

Multilayer Circuits

The formulation of the photoimageable metal and dielectric pastes is ideal for fabricating multilayer circuits and excellent results have been achieved with circuits employing two metal layers separated by a dielectric layer.

A multilayer circuit is fabricated by first creating the lowest level metal structures using the procedure illustrated in Figure 4, followed by repeating stages 5-10 using the dielectric paste to form a dielectric layer complete with via holes above the metal structures. The second layer of metallisation is added by repeating stages 5-10 using a metal paste. This alternating cycle of forming structures using the metal and dielectric pastes is continued until the required numbers of layers are added to complete the circuit.

If the fired thickness of the dielectric layer is greater than the fired thickness of a metal layer, then the upper surface of a dielectric layer covering metal structures as shown in **Figure 7** will usually be very flat. Therefore, complementary printing is unnecessary to achieve a flat upper surface of the dielectric layer.

If the width of a 50Ω transmission line is to be greater than 20µm, then the thickness of the dielectric layer separating the signal conductor from the ground conductor has to be at least 34µm. A 34µm thick dielectric layer is formed by printing four layers (assuming each layer is 10µm thick) of dielectric paste as shown in **Figure 8**, where the previous layer is dried in an oven before the subsequent layer is printed. All four dielectric layers are UV exposed, processed and fired simultaneously.

Metal structures on different layers are interconnected using vias that are created using the process shown in **Figure 9**. Via holes are formed by exposing the dried dielectric paste to UV light through a photomask with UV opaque regions located where the via posts are to be formed, followed by processing to dissolve the unexposed dielectric paste leaving a via hole.

The width of the via holes should be at least 20µm less than the width of the via pads above and below the via post. The substrate is then fired before the via posts are added. Infilling the via holes to form via posts is accomplished by overprinting the fired dielectric with metal paste, either with the same print used for the upper layer of metallisation, or as a separate via hole filling process.

If the depth of the via holes is large in relation to the thickness of a printed layer of wet metal paste then it is recommended that the via posts are formed separately. An additional photomask is required for a separate via filling process, which is the inverse of the photomask used to form the via holes, as only the metal paste filling the via holes needs to be exposed to UV light. The firing of via posts is performed when the upper layer of metallisation is fired as there is no need to fire via posts separately.

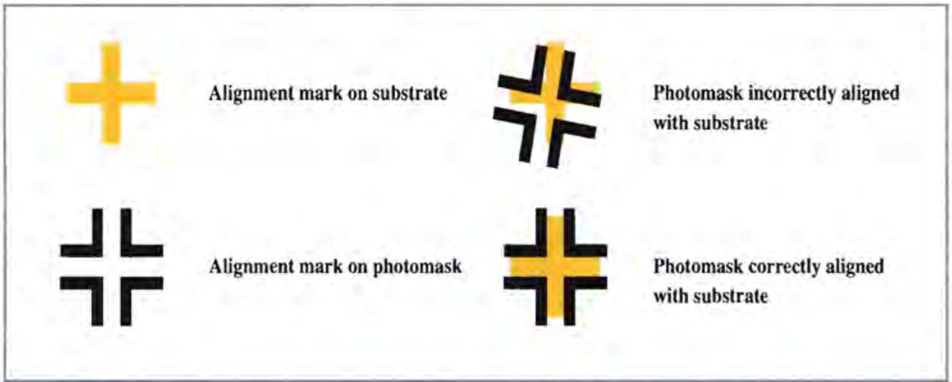


Figure 6: *Alignment marks on the substrate and on the photomasks used to create structures on higher level metal and dielectric layers*

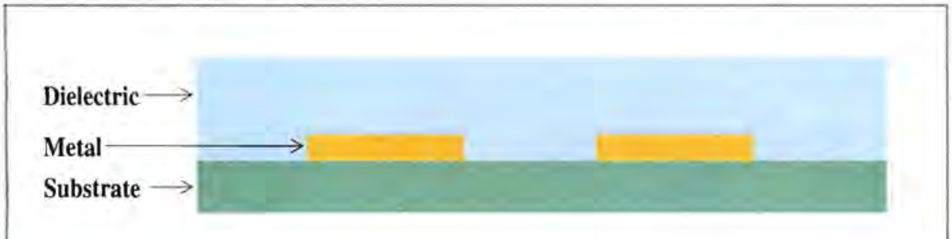


Figure 7: *The upper surface of a dielectric layer is flat even above metal structures*

Fabrication Problems

The most common fabrication problems are:

1. Uneven thickness of print.
2. Rough or uneven edges of fired metal and dielectric structures.
3. Voids in metal and dielectric structures.
4. Poor alignment of structures on different layers of a multilayer circuit.
5. High spots in metal structures which protrude through the upper dielectric layer.

6. Dust and other contaminants embedded in metal and dielectric structures.

7. Smearing of prints.

All of these can be minimised with a suitable production environment and the correct processing of materials. At the time of writing, the Hibridas process is not fully mature and experimentation with the settings of the machines is required to ensure a repeatable and consistent production of high quality circuits with the minimum of defects. The settings of the machines described in this article should only be taken as a guideline and experimentation may be required to achieve the best results.

Figure 8: *Printing four layers of dielectric paste to achieve a total fired thickness of 40µm*

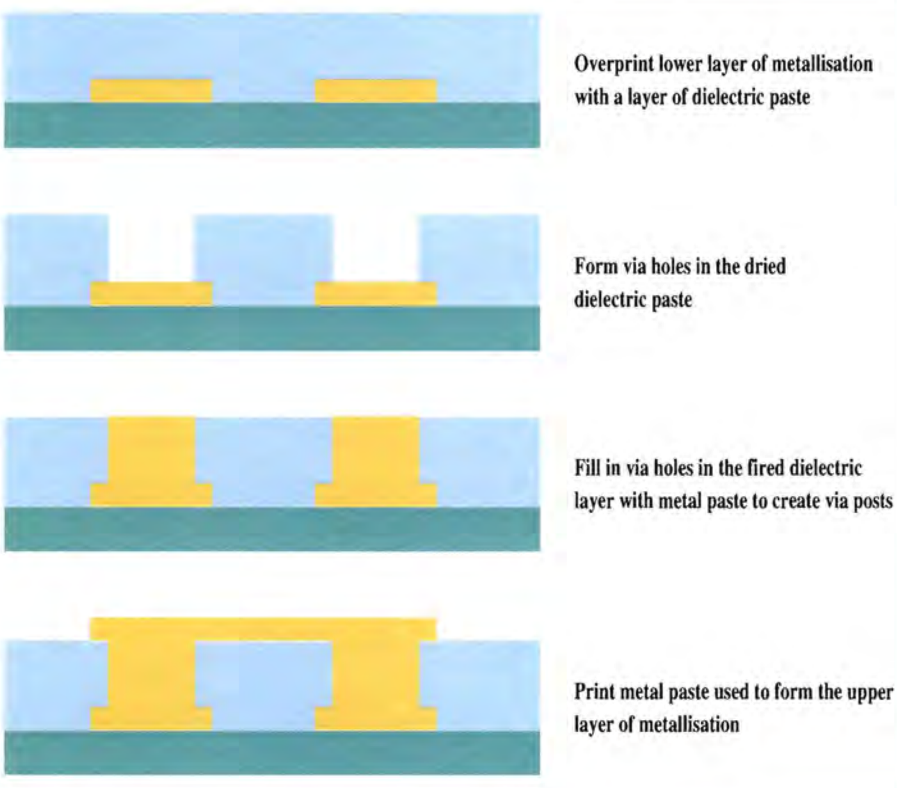


Figure 9: *Process sequence for forming via posts*

Attachment of Wires and Packaged Components

Components packaged with leads or pad terminations can be attached to metal structures by soldering or welding. Wire leads can be attached to metal structures either by soldering, thermocompression bonding, or ultrasonic bonding. If soldering is used then ideally the solder pads should be fabricated in silver. Gold dissolves in ordinary tin-lead solders so special indium alloy solders have to be used when soldering to gold solder pads.

Simple Implementation

The Hibridas photoimageable thick-film process offers a facility to fabricate electronic circuits that is simple to implement, cost effective, suitable for both small scale research and large scale mass production environments, and capable of achieving high quality results competitive with more established manufacturing processes.

It is particularly suitable for microwave circuits operating above 10GHz which are difficult to fabricate using a conventional thick-film process due to roughness of the metallisation, and the inability to produce a sufficiently fine trace and gap resolution. Most circuits operating above 10GHz, or those requiring a trace and gap resolution smaller than approximately 100µm are currently fabricated using the thin-film process. This process is both complicated and expensive to install and use, so it is likely that the Hibridas process will largely supercede the thin-film process in the future.

Uptake of the Hibridas process by industry and research institutions has been quite small despite the equipment and materials being commercially available for over 10 years. Hopefully, the information provided in this article about the Hibridas process and its merits will encourage a widespread adoption of the process in the future. ■

LOOKING AT LIGHT BULBS

By Chris Williams, UKDL

Regular readers will remember that I have raised the question of lighting in several recent issues. My apologies for coming back to the subject again, but there are a couple of points to raise at this time as great topics to use in discussion with relatives and friends.

Depending on how you use this information, you can a) bore people to death, b) frighten them away from modern technology or c) encourage them to learn more about what is happening, and then object noisily to having change just "thrust" upon them by our energy providers.

(1) Did you know that...

Light bulbs contribute to the heating system of the average house and replacing them with "high efficiency" lamps of any technology may not save money at all. We all know the incandescent bulb is inefficient – a typical 60W light bulb is only about 5% efficient at converting electrical energy to light and will waste as much as 55W of the input energy as heat.

But, whether we want it there or not, this heat contributes to the warmth of the room it is located in. Without this background heat, it is quite likely that the average householder may have to nudge up the central heating controller a bit, which will negate the benefit of changing the light bulb in the first place.

(2) Did you know that...

Conventional fluorescent tubes are the most commonly used technology throughout the world for office and industrial lighting. Linear fluorescent tubes have evolved over the years to become increasingly efficient, with the latest version (T5) claiming typically 93 lumens per watt when driven using electronic ballasts. This is an impressive number and is close to the best of any commercially available white light source.

When the linear fluorescent tube is mounted in the light fitting itself, the finished assembly is described as a Luminaire, and this is where the problems can start. The Luminaire product designers develop their products to "look good" and be "stylish", but most of the steps they take destroy the efficiency of the original lamp itself. As an example, a major lighting manufacturer recently admitted that when their T5 lamps (93 lumens/watt) were mounted into their

Fluorescent tube

Energy-saving bulb

own ceiling mounted louvered Luminaire assemblies, the efficiency of the assembly dropped to 38 lumens per watt of 'delivered light". Perhaps we should insist that the metric for the assessment of light bulbs should move away from headline figure of the efficiency of the lamp or the bulb to measure instead the efficiency of the "delivered light".

Here's a small diversion for you. What does the "T" in "T5" stand for? For those outside of our industry, the vocabulary and acronyms we use can be wonderfully obtuse. From the earliest days of lighting, the diameter of a lamp or bulb was measured in multiples of 1/8th of an inch. Decidedly non-metric, this measure has withstood the ravages of time, and fluorescent tubes and LEDs are available in T versions. Therefore, a T5 fluorescent tube is (5 x 1/8th) – 5/8th of an inch in diameter. Similarly, a T8 tube is 1 inch in diameter, and a T1 LED is 1/8th of an inch, or 3mm in diameter.

HOW MANY LOCAL COUNCILS ARE READY AND PREPARED TO EFFICIENTLY COLLECT AND SAFELY DISPOSE OF FAILED COMPACT FLUORESCENT LAMPS?

(3) Did you know that...

Compact fluorescent lamps (CFL) are better for the environment than incandescent bulbs – discuss!

These lamps are the stubby, baby brothers of the conventional fluorescent tubes mentioned above. We are all in danger of being swept along with the rush to replace our incandescent bulbs with compact fluorescent lamps. Indeed, the UK's major energy providers have active programmes to free issue millions of CFLs to their customers as part of their commitment to encourage us to use power more efficiently. But, before we all say "whoopee", maybe there are a couple of areas that deserve closer examination.

We have already looked at the heating effect of bulbs in Item 1 above, so let's focus on environmental and health considerations.

1. *CFLs use mercury. Mercury is a dangerous substance that has been banned under RoHS legislation. Why are we still able to buy lamps with mercury in?*

Every fluorescent lamp and compact fluorescent lamp contains a small amount of mercury that is essential to the

Incandescent bulb

operation of the lamp; it cannot presently function without it - and remain commercially competitive. Mercury is now deemed a dangerous substance and has been banned from use under the Restriction of Hazardous Substances (RoHS) legislation. Thermometers can no longer use mercury and it has been excluded from all areas of electronics, except lighting.

The consortium of lighting manufacturers has successfully lobbied the EU to maintain, and indeed expand, the exposure of the public to mercury. Incandescent bulbs use no mercury, yet we are being encouraged to replace them with CFLs. With 26 million households in the UK, and maybe 10 bulbs per household, we are being encouraged to install up to 260 million mercury-containing bulbs. If we put to one side the argument about power saving, and we similarly ignore comments that power stations emit mercury in their exhaust fumes, and the power saving of using CFLs compensates for the mercury used in their manufacture, we are left with the "disposal at End of Life" question. CFLs don't last forever, so when they die, how do we safely dispose of them? It is no longer legal to dispose of banned substances in landfill, so can we ask the question "How many local councils are ready and prepared to efficiently collect and safely dispose of failed compact fluorescent lamps?" My suggestion is that the answer will be pretty close to zero... you might like to check this by phoning the Environmental Services department of your local council and asking them personally.

2. CFLs can emit large amounts of UV light.

A very recent test performed at a laboratory in the UK has unearthed the surprising fact that commercially purchased CFLs can emit large amounts of ultraviolet radiation at 254nm. The compact fluorescent lamp is similar to the linear fluorescent lamp, except that the lamp is bent at least once to create its compact overall dimensions.

When the lamp is made and bent automatically using careful in-line inspection and test methods, the process of covering every face of the tube with phosphor can be achieved. The low-pressure plasma generated within the tube (using the mercury as an integral component) creates ultraviolet light that impinges on the phosphor coating the tube walls and through the process of photoluminescence the ultraviolet light is absorbed by the phosphor and re-emitted as visible light.

The problem occurs when production moves from modest quantities to high volumes. Regardless of product type or technology, most very high volume production processes are conducted in low-cost labour areas in order to minimise costs, and the focus is on producing products that are cheap and include the minimum amount of materials, since materials equal cost.

You will have seen the price of CFLs reduce from several pounds sterling to less than one pound over the last few years. This reduction in cost has been at a price, and that price is inevitably quality of manufacture. The laboratory tests that have been conducted on CFLs that were bought over the counter at local shops indicate that low-cost CFLs do not appear to have adequate phosphor coverage in the region of the bent tube, and this is allowing the UV generated within the tube to leak out.

Where the CFL is used for room lighting, there is probably no problem, other than the fact that if you use a plastic lampshade the high level of UV will cause premature degradation and the shade may crack and fall apart within weeks or months. If the CFL is being used for task lighting (in a desk lamp for example) the proximity of this UV leakage may be an actual health hazard.

Armed with Information

The points above will arm you with plenty of information to win arguments and discussions, but on a more important note, it does seem necessary to conduct far more tests on products before they are released to the general market to ensure full compliance with health and safety requirements during use and at point of disposal.

From my own perspective – yes, I have some CFLs in use at home for room lighting, but no, I don't use any of them for task lighting.

Chris Williams is Network Director at the UK Display & Lighting Knowledge Transfer Network (UKDL KTN)

THE ADVANTAGES OF FLOATING SERIAL RL SIMULATORS IN LADDER FILTER IMPLEMENTATIONS

The ladder filters are the circuits that show very low sensitivity to component tolerances. In this article, the advantage of a floating serial RL circuit is shown in the realisation of a ladder filter. The serial RL circuit provides ladder filter implementation with less number of components compared to floating lossless inductor circuit. Moreover, the effects of the active component non-idealities can be compensated.

Although there are several examples of floating inductance simulators in the literature, most of the presented topologies use active and passive elements more than necessary.

Floating Serial RL simulators find application area as wide as pure inductor simulators. For example, they can be used in ladder filter applications, or in the implementation of the chaotic circuits. Furthermore, they can be used in the realisation of serial resonance circuits easily.

In this paper we employ a floating serial RL simulator using only one active and three passive components in the implementation of a ladder filter. Since it employs fewer active components than the inductance simulators mentioned above, it will be suitable for low-power required applications. Moreover, the proposed circuit does not require any component matching condition.

The Floating Serial RL Circuit

In one implementation of the floating serial RL circuit (see Singh, V.'s "*A new Active RC Circuit realization of Floating Inductance*", 1979, *Proc. of the IEEE*, **67**, (12), pp. 1659-1660), negative type the second-generation current conveyor (CCII-) is used. The circuit symbol of (CCII-) is shown in **Figure 1**. Considering the non-idealities arising from the physical implementation of CCII, its terminal relationship can be given as:

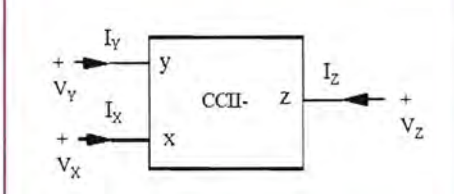


***Figure 1**: Circuit symbol of CCII*

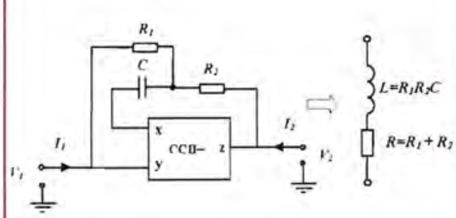


***Figure 2**: The floating serial RL simulator*

$$V_X = \beta V_Y, \quad I_Y = 0, \quad I_Z = \alpha I_X \qquad (1)$$

where α and β are respectively current and voltage gains which can be expressed as $\alpha = 1-\varepsilon_i$, $\beta = 1-\varepsilon_v$ with $|\varepsilon_i| << 1$, $|\varepsilon_v| << 1$. Here, ε_i denotes the current tracking error and ε_v denotes the voltage-tracking error.

The proposed actively simulated floating serial RL circuit is shown in **Figure 2**. The two-port short circuit admittance representation of the circuit is given as:

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \left(\frac{1}{R_1 + R_2 + sCR_1R_2}\right)\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \qquad (2)$$

Thus a floating serial RL circuit can be simulated where the equivalent resistor value is $R = R_1+R_2$ and the equivalent inductance value is $L = CR_1R_2$. Passive sensitivities of the proposed circuit for this L value are: ,

$$|S^L_{R_1}| = 1 \quad |S^L_{R_2}| = 1 \text{ and } |S^L_C| = 1$$

Considering the active element non-idealities as given in **Equation 2** converts to:

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \left(\frac{1}{R_1 + R_2 + sCR_1R_2}\right)\begin{bmatrix} 1 - sCR_2(\beta-1) & -1 \\ -1 + sC(R_2\alpha(\beta-1) + R_1\beta(\alpha-1)) & 1 - sCR_1(\alpha-1) \end{bmatrix}\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \qquad (3)$$

Equation 3 shows that the effects of the non-ideal voltage and current gains can be compensated for the conditions such as

$$|\omega CR_1| << 1 \text{ and } |\omega CR_2| << 1$$

Simulations and a Lossy Ladder Filter Implementation

Unlike active filters, the ladder filters are the circuits that show very low sensitivity to component tolerances. Although these

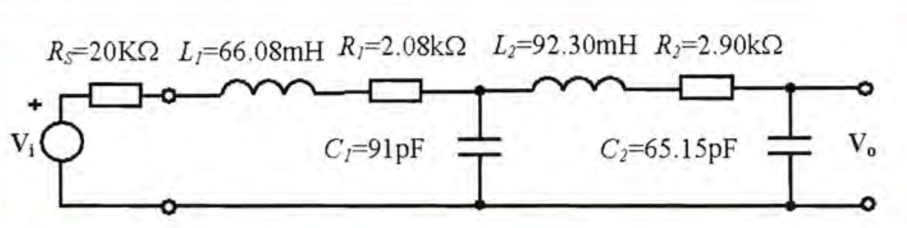


***Figure 3:** Scaled version of the ladder filter example. The proposed circuit in Figure 2 is used for the implementation of serial RL elements R1-L1 and R2-L2 of the ladder filter*

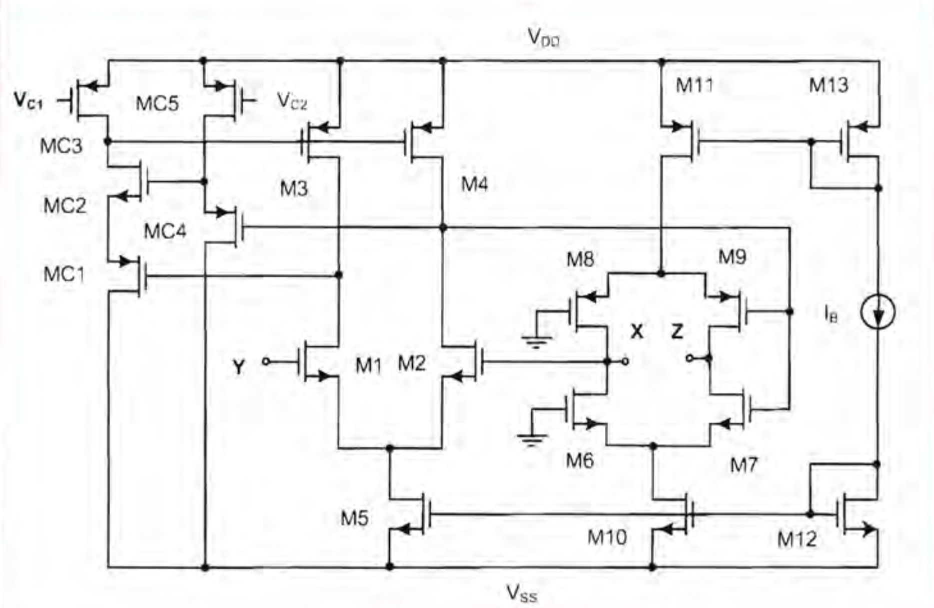


Figure 4: *A CMOS CCII- realisation*

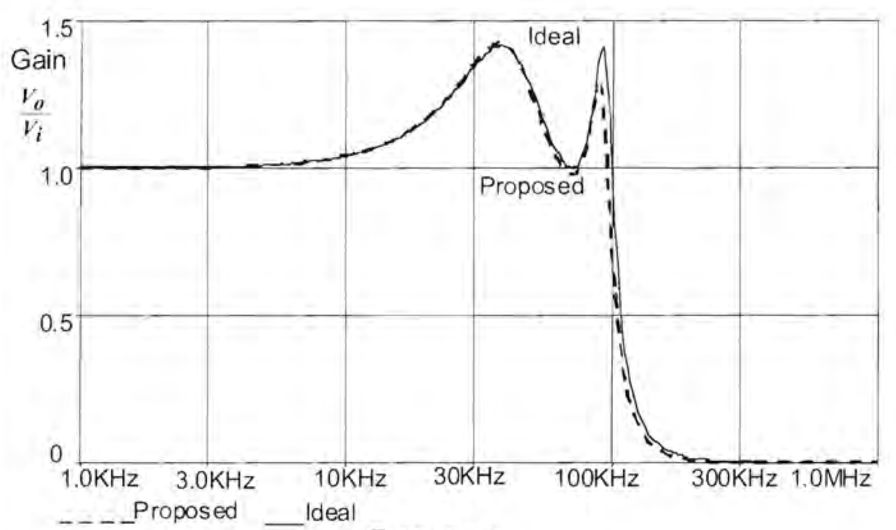


Figure 5: *Ideal and simulated frequency responses*

passive filters have such kind of important advantage over active filters, they may not be frequently used because conveniently sized inductors are components that are not suitable for integrated circuit. Thus, the methods to simulate the behaviour of lossless ladder filter are important.

One such method is using inductor simulators, but this operation may seriously increase the number of components. The usage of the serial floating serial RL circuit provides a simple solution to this problem.

The design approach with passive lossy ladders is given in many textbooks. Employing lossy inductors will only limit the gain parameter of the filter realised but this problem does not play an important role in many designs. A fourth-order equal-ripple (3dB), low-pass realisation example is chosen from Budak, A.'s ***"Passive and active network analysis"***, (Houghton Mifflin Company, Boston, 1974), pp. 543-553, to show the performance of the proposed circuit. Note that for this design example lossy inductors will not reduce the pass-band gain of the ladder. On the other hand an n-th order filter will employ only n/2 current conveyors, n-capacitors and n-resistors that are minimum numbers for simulated ladder type filters.

The proposed circuit in Figure 2 is used for the implementation of serial RL elements R_1-L_1 and R_2-L_2 of the ladder filter given in **Figure 3**. As an active component Awad and Soliman's high performance CMOS realisation shown in **Figure 4** is used to implement (CCII-).

SPICE parameters of the (CCII-) can be found in Cam, U.'s ***"A new high performance realisation of mixed-mode chaotic circuit using current-feedback operational amplifiers"***, Computers and Electrical Engineering, 2004, 30, pp. 281-290. R_1-L_1 serial RL elements in Figure 3 are designed with the passive element values $R_1 = R_2 = 1.04k\Omega$ and $C = 61.09nF$ to obtain $L_1 = 66.08mH$ and $R_1 = 2.08k\Omega$. Similarly, R_2-L_2 are designed with the passive element values $R_1 = R_2 = 1.45k\Omega$ and $C = 43.9nF$ to obtain $L_2 = 92.3mH$ and $R_2 = 2.90k\Omega$. Ideal and simulated frequency responses are given in **Figure 5**. Simulation result shows that proposed circuit works well.

Conclusions

In the ladder filter implementations, floating lossy inductance simulators are more useful compared to lossless ones with respect to number of components. In this study, current conveyor implementation of a low-pass ladder filter design is given. Furthermore, the effects of the active component non-idealities can be compensated for the presented circuit. Simulation results are included to verify theoretical results.

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Turkey

Microchip continues to provide innovative products that are smaller, faster, easier-to-use and more reliable. PIC microcontrollers (MCUs) are used in a wide range of everyday products from washing machines, garage door openers and television remotes to industrial, automotive and medical products. While some designs such as Switch Mode Power Supplies (SMPS) are traditionally implemented using a purely analogue control scheme, these designs can benefit from the configurability and intelligence that can only be realised by adding a microcontroller.

NOTE: The tips 'n' tricks presented here assume a 3.3V supply. However, the techniques work equally well for other supply voltages with the appropriate modifications.

TIP 1: CREATING A DITHERED PWM CLOCK

In order to meet emissions requirements as mandated by the FCC and other regulatory organisations, the switching frequency of a power supply can be varied. Switching at a fixed frequency produces energy at that frequency. By varying the switching frequency, the energy is spread out over a wider range and the resulting magnitude of the emitted energy at each individual frequency is lower.

The PIC10F200 has an internal 4MHz oscillator. A scaled version of oscillator can be output on a pin (FOSC/4). The scaled output is 1/4 of the oscillator frequency (1MHz) and will always have a 50% duty cycle. Figure 1 shows a spectrum analyser shot of the output of the FOSC/4 output.

The PIC10F200 provides an Oscillator Calibration (OSCCAL) register that is used to calibrate the frequency of the oscillator. By varying the value of the OSCCAL setting, the frequency of the clock output can be varied. A pseudo-random sequence was used to vary the OSCCAL setting, allowing frequencies from approximately 600kHz to 1.2MHz. The resulting spectrum is shown in Figure 2.

By spreading the energy over a wider range of frequencies, a drop of more than 20dB is achieved.

Example software is provided for the PIC10F200 that performs the pseudo-random sequence generation and loads the OSCCAL register.

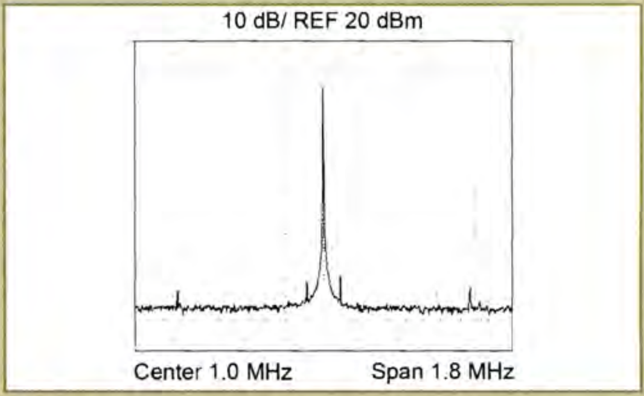


Figure 1: *Spectrum of clock output before dithering*

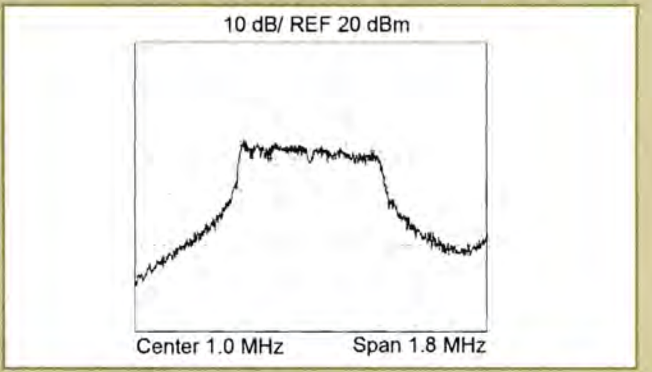


Figure 2: ***Spectrum of clock output after dithering***

TIP 2: USING A PIC MCU AS A CLOCK SOURCE FOR A SMPS PWM GENERATOR

A PIC MCU can be used as the clock source for a PWM generator, such as the MCP1630.

The MCP1630 begins its cycle when its clock/oscillator source transitions from high-to-low, causing its PWM output to go high state.

1. The sensed current in the magnetic device reaches 1/3 of the error amplifier output.
2. The voltage at the Feedback (FB) pin is higher than the reference voltage (VREF).
3. The clock/oscillator source transitions from low-to-high.

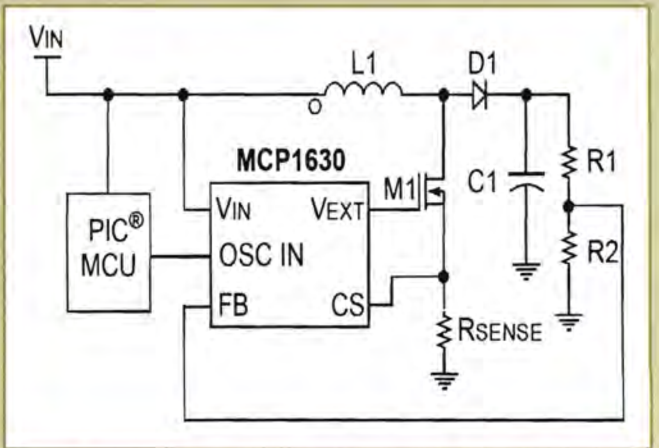


Figure 3: ***PIC MCU and MCP1630 example boost application***

The switching frequency of the MCP1630 can be adjusted by changing the frequency of the clock source. The maximum on-timer of the MCP1630 PWM can be adjusted by changing the duty cycle of the clock source.

The PIC MCU has several options for providing this clock source:

- The FOSC/4 pin can be enabled. This will produce a 50% duty cycle square wave that is 1/4th of the oscillator frequency. Tip 1 provides both example software and information on clock dithering using the FOSC/4 output.
- For PIC MCUs equipped with a Capture/Compare/PWM (CCP) or Enhanced CCP (ECCP) module, a variable frequency, variable duty cycle signal can be created with little software overhead. This PWM signal is entirely under software control and allows advanced features, such as soft-start, to be implemented using software.
- For smaller parts that do not have a CCP or ECCP module, a software PWM can be created.

TIP 3: CURRENT LIMITING USING THE MCP1630

The block diagram for the MCP1630 high-speed PWM driver is shown in Figure 4. One of the features of the MCP1630 is the ability to perform current limiting. As shown in the bottom left corner of the diagram, the output of the Error Amplifier (EA) is limited by a 2.7V clamp. Therefore, regardless of the actual error, the input to the negative terminal of the comparator (labeled Comp) is limited to 2.7V÷3 or 0.9V.

It is possible to implement the current limiting by using a single sense resistor. In this case, the maximum current would be given by using a single sense resistor. In this case, the maximum current would be given by Equation 1:

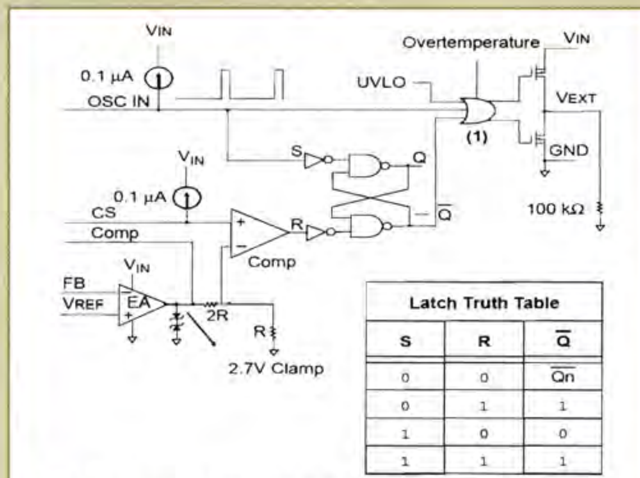
$$I_{MAX} = (0.9V) / R_{SENSE}$$

For high current applications, this method may be acceptable. When lower current limits are required, the size of the sense resistor, RSENSE, must be increased. This will cause additional power dissipation. An alternative method for lower current limits is shown in Figure 5.

In this case, the Current Sense (CS) input of the MCP1630 is biased upward using the R1/R2 resistor divider. The equations for the new current limit are shown in Equation 2:

$$0.9V = \frac{(V_{DD} - I_{MAX} \cdot R_{SENSE}) \cdot R2}{R1 + R2}$$

Equation 2 can be solved to determine the values of R1 and R2 that provide the desired current limit.



Latch Truth Table		
S	R	$\overline{Q}$
0	0	$\overline{Qn}$
0	1	1
1	0	0
1	1	1

Note 1: During overtemperature, VEXT driver is high-impedance.

Figure 4: MCP1630 high-speed PWM

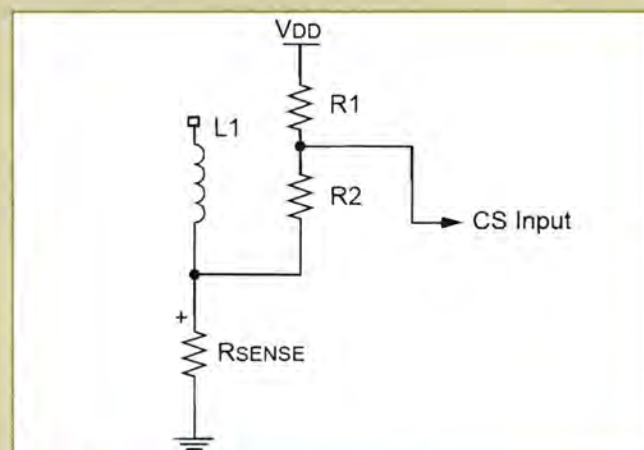


Figure 5: Low current limits

TIP: NICAD BATTERY RECONDITIONING CIRCUIT

By Jim Mahoney, Associate Applications Engineer, Linear Technology

For 45 years, NiCad batteries have plagued me. That's because I like to spend my Sunday afternoons relaxing with radio controlled aircraft, like my Century Predator helicopter. This beauty costs well over a $1,000.

Unfortunately, if the NiCad battery powering here unexpectedly dies before landing, well, let's just say that my whole day is shot. NiCad batteries are notorious for losing their capacity over time and it's not just model plane enthusiasts that suffer. With their high current capability, NiCad batteries are used in everything from computers to power tools. I was thinking about this as I read *"Batteries in a Portable World"*. Right there in Chapter 10, *"Getting the most from your Batteries – Exercise and Recondition"*, I realised that a solution was finally at hand.

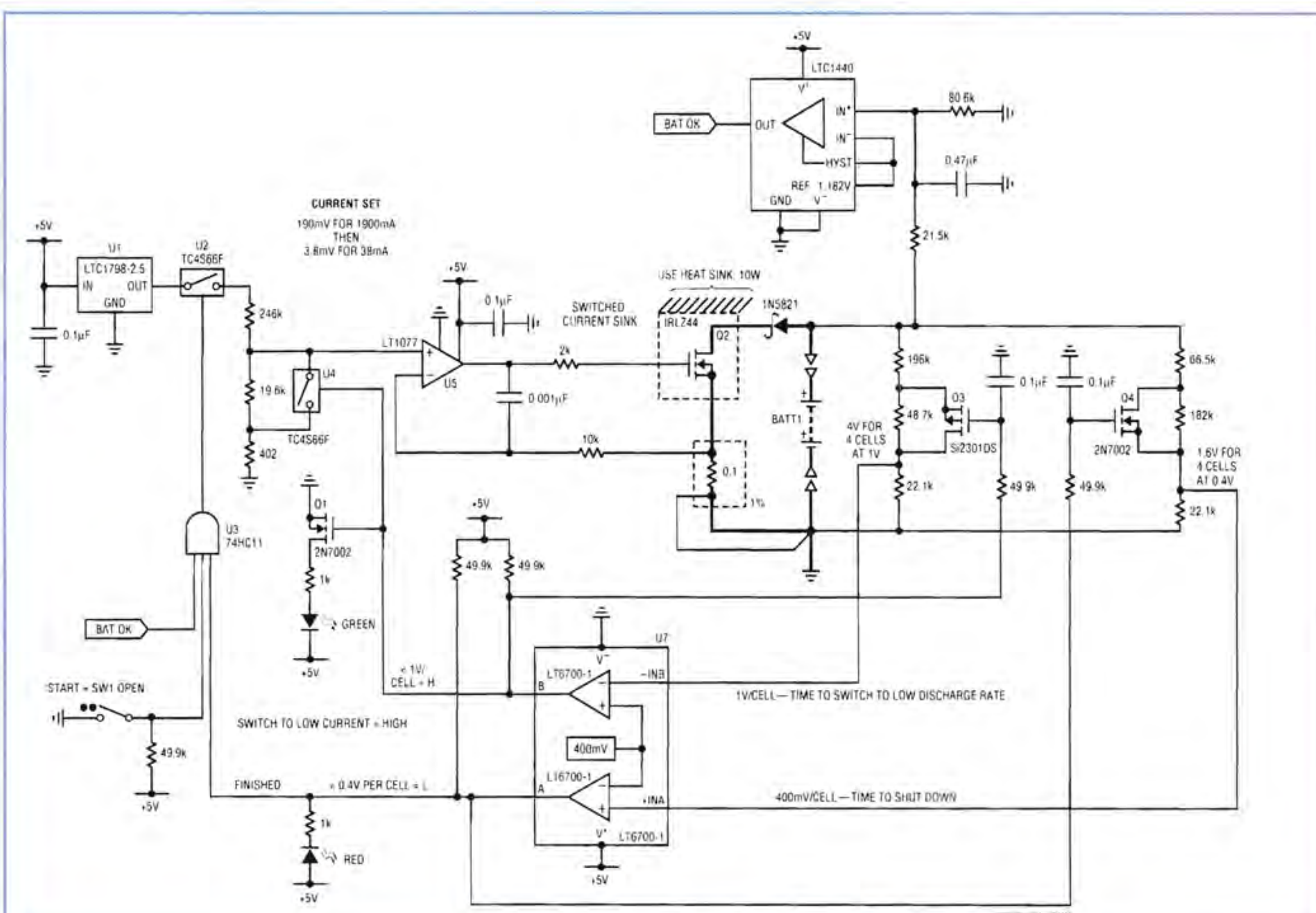
THE ISSUE WITH NICADS

Depending on how they are handled, as NiCads age, the nickel crystals inside them will enlarge. This decreases the total crystal surface area, which, effectively reduces the cell capacity and increases its internal resistance. Fortunately, nickel crystals in a battery can be re-formed by very slowly discharging each NiCad cell from 1V down to 0.4V.

As explained in *"Batteries in a Portable World"*, this helps to restore the cell's capacity and decreases its internal cell resistance. You won't recover 100% capacity, but you can prolong the useful life of a battery by up to 40% with a once per month cycle. How much is recovered will depend on many factors such as the condition of the battery when you start, battery age, how many charge cycles it's gone through, etc. I propose a simple circuit, based on reconditioning a 1900mAh 4-cell battery pack, which handles this task.

CIRCUIT DESCRIPTION

This circuit uses Linear Technology's LT6700-1 dual comparator to



Nicad battery discharge and conditiong circuit example for Nicad cellbattery pack control a constant current discharge circuit. A battery connected to this circuit will be discharged at a rate of 1900mA until its voltage reaches 1V per cell (4V for the 4-cell battery pack in this example). The discharge current is then reduced to 38mA until the battery voltage reaches 0.4V per cell (1.6V for the 4-cell battery pack in this example).

To begin, the start switch (SW1) is CLOSED and the comparator U6 senses if a battery is connected. If the battery voltage is above 4.4V, the output of comparator U6 will be HIGH, the output of comparator A of U7 will be LOW and the output of comparator B of U7 will be HIGH. These comparators control switches U2 and U4 of the current-set circuit (highlighted on the schematic).

The current-set circuit generates 1 of 3 output voltage states, which in turn, establishes the amount of current drawn from the battery by the current sink circuit (pin 3 of U5):

		SWITCH U2	
		OPEN	CLOSED
SWITCH U4	OPEN	0V (No Current)	190mV (1900mA)
	CLOSED	0V (No Current)	3.8mV (38mA)

Reference U1 supplies a stable 2.5V across a resistor divider string. When the battery voltage is above 1V per cell the current set circuit will output 190mV to the current-sink circuit commanding it to discharge the battery pack at a rate of 1900mA.

When the 4-cell battery pack voltage goes below 4V, analogue switch U4 is CLOSED. The current set output control voltage drops down to 3.8mV and the current-sink circuit discharges the battery at a rate of 38mA. When the battery voltage reaches 1.6V (0.4V per cell), the output of comparator B goes low, switch U2 opens, the current control voltage goes to zero and discharge current is set to zero.

MOSFETs, Q3 and Q4 are used in place of positive feedback resistors for the 1V and 0.4V comparators, to generate high values of effective hysteresis.

A lot of hysteresis is needed because when a NiCad's discharge current is very low, the battery voltage can float up above the higher threshold. Without hysteresis to hold off the comparator circuits, the circuit could continuously flip between high and low current discharge. In this version of the circuit, the lower current (38mA) reconditioning cycle is maintained even as the battery voltage floats up above 1.6V.

CONCLUSION

No battery is without problems. But even with all of its shortcomings, the NiCad battery is still the number one choice when high discharge currents are required because the NiCad cell has the lowest internal resistance. The trade off is that the user must take care to keep them in top shape. The circuit presented here is a tool to keep NiCad batteries in the best possible condition and reduce the uncertainties of their use.

Win a Microchip PICDEM 2 Plus Demo Board

Electronics World is offering its readers the chance to win a Microchip PICDEM 2 Demonstration Board. This board now has an ICD port, LCD read-out, sounder and a temperature sensor. The enhanced PICDEM 2 Plus Demonstration Board provides designers with a tool for immediate programming and debugging Flash-based microcontrollers. The board is supplied with software loaded on a PIC18F452 microcontroller to demonstrate the device's features and peripherals. The program also sets up the microcontroller as a real-time clock and measures the local temperature, both of which are displayed on an LCD display. A PWM signal is sent directly to the Piezo sounder. There is an active RS-232 port and on-board Serial EEPROM and there is ample room in the generous prototyping area for project development work. A second Flash-based microcontroller with its own demonstration program, the PIC16F877, is also included.

Source code is provided allowing users to understand and dissect the programming algorithm. Additionally, users with an MPLAB® In-Circuit Debugger 2 can take advantage of the Flash-based microcontroller's in-circuit debugger capability by cutting, pasting, rewriting or adding to the program.

The PICDEM 2 Plus Demonstration Board is available separately or as part of the MPLAB ICD 2 Evaluation Kit, which also includes a power supply, serial cable and USB cable.
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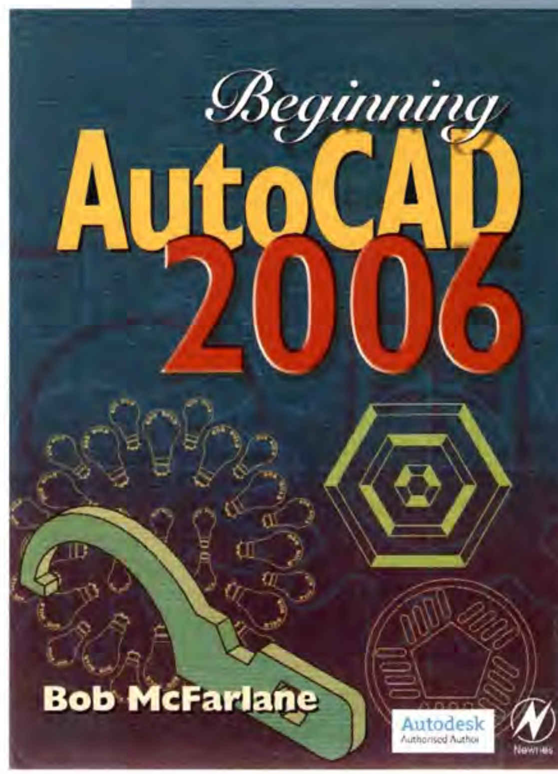
BEGINNING AUTOCAD 2006

BOB MCFARLANE

NEWNES



As the title suggests and the author has rightly put it, this is a book on the subject of 2D drawing using AutoCAD designed essentially for beginners. If you're a novice in CAD packages and you're looking for any good introduction on 2D drawings using AutoCAD, then this book will prove to be very helpful. However, if you are an advanced user and looking for some advanced 3D tips and training, it's not likely that you'll get what you expect from this book.

The book is organised in 36 short chapters that are, to certain extent, independent, meaning that you can jump directly to the chapter of interest to your design without any loss of generality.

> **THE AUTHOR CHOOSES TO DESCRIBE MOST OF THE MATERIALS TEXTUALLY, INSTEAD OF PROVIDING A SNAP-SHOT FROM AUTOCAD DESCRIBING THE INTENDED OPERATION. THIS, OF COURSE, CONSIDERABLY REDUCED THE VOLUME OF THE BOOK BUT ALSO INTRODUCED A MAJOR DRAWBACK**

McFarlane starts by presenting the GUI of AutoCAD, which explains what are the fields, menus, toolbars, etc, encountered when starting AutoCAD 2006. There is no technical info in this chapter; if you have any background in other CAD packages, or even basic knowledge of MSOffice or similar ones, this chapter might seem redundant at this point (though helpful for beginners).

Then, in subsequent chapters, simple and basic drawing examples such as editing and deleting items are explored. Basic configuration such as setting drawing environment to grid, snap, Cartesian and polar coordinates are presented along with how to dynamically display the dimensions (length, angle, diameter, etc) of the lines and curves being drawn. Then, the desktop operations such as "open", "save", "save as", "exit", etc, on different drawing files are introduced in this section.

Although the material presented up to Chapter 5 seems to be very basic for regular computer users, a lot of new techniques can still be learned as, for example, the use of "cross" and "polygone" methods to select items (in order to, say, delete them) which are non-intuitive techniques and presented here in a good and simple way.

In Chapter 6 we learn how to set the template that can be used for later projects. In this chapter we clearly encounter what we have been suspecting for some time: the book has the disadvantage of lacking many explanatory drawings. The author chooses to describe most of the materials textually in form of "prompt" and "answer" fields, instead of providing an actual photo (snap-shot) from AutoCAD describing the intended operation. This, of course, considerably reduced the volume of the book (and probably the price) but also introduced a major drawback as the reader might spend more time in understanding concepts that would be otherwise straightforward and self explanatory was an actual snap-shot provided.

In the subsequent number of chapters (up to Chapter 9) you will get already a taste of what powerful AutoCAD has to offer. Many ways of drawing basic curves such as lines, circles and rectangles are presented. Relative and polar coordinates are also introduced as well as Object Snap (OSNAP), running OSNAP, extension and parallel OSNAP and AutoSnap. These are techniques that make reference to some features of an existing drawing (centre, middle point, intersection, quadrant, tangent, perpendicular, endpoint, etc) in order to use them as aid or reference to what should be drawn next. As an example, you'll be surprised how many methods can be used to draw a circle, for example, using parts of the existing drawing as reference. This is a powerful method that makes life easy for CAD designer and McFarlane has excelled in presenting clearly and succinctly what AutoCAD has to offer in this domain.

Other, relatively more difficult curves are introduced in Chapter 9 such as donuts, polygons and ellipses. To illustrate the might of AutoCAD (as in Chapter 7), here also you'll find a myriad of ways that can be used to draw a given curve.

In Chapter 10, the powerful concept of layers is introduced. Different structures (dimensions, centre lines, text, etc) are defined on separate layers. As the author stated, it's highly recommended to extensively use the layers concept for professional drawings as they make complex drawings easy to comprehend and visualise by turning ON/OFF the different layers.

In following chapters (up to Chapter 25), the author introduces various powerful AutoCAD modify and edit commands such as fillet, chamfer, offset, extend, trim, point filters and construction lines, among others. The usual approach of "learn by example" makes it fairly easy to grasp these rather advanced concepts. The major drawback, as stated earlier, is the economic use of actual screen snap-shots that makes it less attractive and more difficult for the layman to follow the explanations.

The last, but not least, group of chapters deals mainly with drawing configuration and environment such as how to set units and paper sizes; the concepts of blocks and attributes; how to access and use the built-in drawing facilities (Design Center) and more information about templates, standards and file formats.

McFarlane's approach in his book "AutoCAD 2006" is particularly suited for self-study but can be used by professors for class notes as well. The extensive list of exercises makes sure that the concepts introduced in any particular chapter are fully understood by working out the related "activities" provided at the end of the book. The independent structure of the material, presented in many separate chapters, makes this book ideal for use as a reference for both the novice and the more confirmed users.

M. H. El-Husseini

Monitran's Easy-to-Use Product Selector Guide

Sensors-maker Monitran has released a new product selector guide. It presents features and benefits of 64 of Monitran's general and special purpose accelerometers - all in a concise, A4 fold-out booklet.

The guide is free and can be requested as a hardcopy or as a PDF by contacting Monitran on sales@monitran.com.

Within the sensor guide, products are split into three categories: general purpose analysis (AC), general purpose monitoring (DC) and special purpose, and then further refined into families. Icons are used extensively throughout the guide to denote the sensors' applicability to one or more of up to nine industry sectors, including utilities, buildings and maintenance, automotive, petrochemical and R&D.

Monitran's sensor guide also includes a page devoted to selection tips, to help users identify the most suitable products for their requirements. For applicable sensors, approval to ATEX group I or II is highlighted. Also, for each sensor in the guide, its weight, dimensions, sealing (IP rating), type (top or side entry), temperature range and electrical characteristics are given.

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Ocean Optics Produces Its Fastest Spectrometer Yet

For applications that monitor high-speed chemical and biochemical reactions, Ocean Optics has produced its fastest spectrometer ever. The USB2000+ Miniature Fiber Optics Spectrometer can transfer 1000 scans per second into memory when connected to a computer via the high-speed USB 2.0 port.

The spectrometer can measure optical properties within a wavelength band of 200–1100nm. It can be equipped with a custom selected fixed grating which disperses the light to the 2048-element CCD array detector, producing results at a resolution to 0.35nm (FWHM).

Operating the USB2000+ Spectrometer is easy. The user simply installs the user interface SpectraSuite software, and connects the spectrometer to the computer via the USB cable. No other power source is required. SpectraSuite is completely modular, Java-based spectroscopy software that operates on Windows, Macintosh and Linux.

The USB2000+ features a programmable microcontroller that allows flexibility in controlling the spectrometer through its digital and analog GPIO inputs and outputs. It can be used in various trigger modes. The internal EEPROM stores the wavelength calibration which will automatically be used by the operating software.

www.oceanoptics.eu

Software Package for CAN/FMS Systems' Test and Simulation

The PCAN-FMS toolkit from Computer Solutions is a new software package designed to carry out test and simulation functions on the CAN Bus Fleet Management System (FMS) protocols used by truck and bus manufacturers.

The FMS protocols (FMS and Bus-FMS ISO 11992-1) are used by a number of leading bus and truck manufacturers to provide interoperability of systems installed on commercial vehicles and buses. They include a standard set of addresses and layouts for CAN messages used in these industries.

The PCAN-FMS package, along with a CAN interface also available from Computer Solutions, simplifies the process of developing or debugging an FMS application. In its simplest mode of operation, the FMS CAN bus is monitored by a PCAN interface, the FMS messages are decoded, and their values are displayed in a PC window as a 'dashboard' with simple dials and indicators.

The user can then log all of the bus activity to a disk file. Alternatively, a previous log can be input into the FMS package and the result replayed to the CAN bus (and 'dashboard') to as a signal source for stimulus testing of an application.

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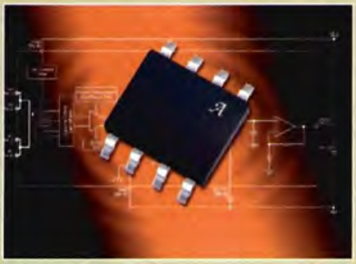
Automotive Hall-Effect High-Accuracy Linear Current Sensors



The new ACS714 and ACS715 from Allegro MicroSystems Europe are a range of automotive-grade Hall-effect linear current sensors combining high accuracy with excellent voltage isolation.

The new devices are designed to provide economical and precise sensing solutions for AC and DC currents in automotive applications such as motor control, load detection and management, switched-mode power supply control and overcurrent fault protection.

Each of the new products consists of a precise, low-offset, linear Hall sensor circuit with a copper conduction path located near the surface of the die. Applied current flowing through this copper conduction path generates a magnetic field, which is sensed by the integrated Hall IC and converted into a proportional voltage. Device accuracy is optimised through the close proximity of the magnetic signal to the Hall transducer.

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Hybrid Connector Handles Ethernet and Power

The new Harting PushPull Hybrid connector integrates Ethernet and power connections into a single compact unit for ease of installation in industrial machines.

The new connector has been developed in response to the increasing use of industrial Ethernet communications in machine installations, where the data wires and the 24V power supply are combined in a single hybrid cable linked by a single hybrid connector within the dimensions of a M12 connector footprint.

Using the Harting PushPull Hybrid connector results in considerable space saving as well as reduction in the number of connectors and cables required for a typical installation. Field installation is also eased through the use of 'plug and play' termination technology.

Safe data transfer is ensured by means of Harting's patent-registered Omega shielding concept. Up to six different codings can be realised by means of coding pins so that improper mating can be avoided.

www.harting.co.uk

Arrow Wireless Solutions Brochure

Arrow has launched a new brochure that will prove an invaluable resource for engineers involved in the development of wireless control and machine-to-machine (M2M) applications, including the addition of wireless functionality to existing designs.

The new 36-page Arrow Wireless Solutions brochure incorporates information into a single document regarding wireless modules and chipsets from some of the world's leading semiconductor and wireless module manufacturers. These include proprietary ISM transmitter and receiver chipsets, chipsets and solutions for 802.15.5/ZigBee applications and modules for Bluetooth, Wireless LAN (WLAN), GSM/GPRS and 3G mobile implementations. Antenna products and wireless module accessories are also covered.

Semiconductor manufacturers featured in the new brochure include Analog Devices, Atmel, Freescale, Infineon, Micrel, National Semiconductor and Renesas. Modular solutions include Bluetooth modules from connectBlue and National Semiconductor, WLAN modules from connectBlue, and GSM/GPRS and 3G modules from Telit.

Arrow Wireless Solutions

To request a copy of the new brochure, or to download a copy, visit

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REMOTE MANAGEMENT

TTI named Kemet 'Charged' Distributor of 2007

TTI has been awarded the Kemet 'Charged' European Distributor of the year award for financial year 2007. This completes a 'Triple Crown' of Distributor awards in North America, Europe and Asia. This recognition has never before been achieved by a Kemet distributor. Kemet places a great deal of value on its distributor business, and its annual awards are based on a number of key factors - sales growth, market share, new product development, ease of doing business, and field and corporate relationships

Andrew Kerr, European Director of Passive Supplier Marketing at TTI said: "Kemet offers one the world's most complete line of surface-mount and through-hole capacitor technologies across tantalum, ceramic, aluminum, film and paper dielectrics. We are delighted to have been named as Kemet's European Distributor of the Year for a second consecutive year, and believe it reflects the value that our two companies place on building excellent partner relationships."

Graeme Dorkings, Director Distribution Sales of EMEA added: "TTI continues to operate a business model which delivers strong performance on all key criteria and this award truly demonstrates that their model works."