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ALSO IN THIS ISSUE: **DDS SIGNAL GENERATOR • INSIGHT • TOP TEN TIPS ON DSPS**

CONTENTS

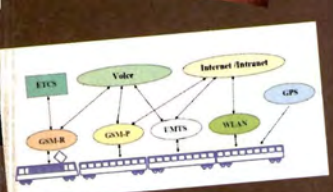
IN THIS ISSUE:

Basestations could be landing on HAPs

Sony's new Walkman

New competition – page 55

Hot Shoe technology connectors



The Virtual Office on a Train

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Multi-disciplinary efforts lead to new ideas

Nanotechnology! Nowadays, we never seem to be too far away from this word. Transistor sizes continue to shrink to the level where it makes more sense to build them bottom up – atom by atom, molecule by molecule.

This, however, is just one of the many challenges that the semiconductor/electronics industry has already started to face or will do in the coming future.

But nanotechnology refers to another field too, one linked to medicine, biology and pharmacology. Luckily, many advances being made in electronics and physics are also intrinsic to the nanotechnology linked to those disciplines. This is good news for our industry as its future is guaranteed, but also because there's the potential to develop new devices, systems, applications and even become part of new disciplines.

At a recent conference on micro- and nanotechnology in medicine, several interesting medical inventions were revealed, which are being used or will be used in the detection or treatment of diseases. All of them are heavily reliant on electronics already, whether the physical principles seen in electronics or the electronic systems themselves.

Light absorption by plasmon resonance, Mie scattering, Raman scattering and optical generation of heat gradients and their application in microscopy are just some techniques used in medicine. Gold particles have also been applied as nanotags that can be injected in the body and, with electronic equipment, problem areas identified quickly through in vivo imaging.

Akubio Limited from Hertfordshire has avoided optical principles altogether and opted for resonant acoustic profiling in the 1MHz to 1GHz range to identify problems in the body. The company has used digital, multiplexing, low power, in-line monitoring as well as remote monitoring technologies to deliver the first such detection system, called RAPid-4.

But one of the most interesting applications at this conference was the use of silicon to create tiny injection needles, which are not going to leave patients in pain or have children grabbing chairs in their distressed effort to get away from the sight of The Needle.

The so-called microneedles, as demonstrated by the University of Cardiff, are microfabricated by either dry or wet etching. They are easy and inexpensive to make, and can be disposable. They are only 100 microns in size and hollow. Normally, an array of many such microneedles will be used to deliver the correct dosage of a drug or vaccine.

Creating the microneedle array involved the efforts of engineers, biologists and pharmacologists – a good collaborative project which indicates that, in the future, the walls between such clearly-defined disciplines are likely to crumble away, leading to new, interesting and fruitful fields of engineering.

Svetlana Josifovska
Editor

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Basestations could be landing on HAPs next

One version of High Altitude Platform (HAP). [Source: NASA]

It's a geo-satellite but located in the stratosphere. It's unmanned, semi-stationary and it can be used as a platform to place other systems on it, such as 3G or WiMax basestations for example, but also for other applications, including broadband coverage, military, broadcast, surveillance and remote sensing, among others. Meet HAP (High Altitude Platform) also known as HALE (High Altitude Long Endurance) or "the very tall mast".

HAP can be an aircraft or solar-powered airship. The goal is to have it up and running for a year at a time at an altitude of between 17 and 22km, well above the other aircraft's flight-paths. It offers a coverage radius of 200km.

Among HAP's key benefits are its rapid and flexible deployment – within hours; it can replace terrestrial or satellite infrastructure for communications purposes; networks can be incremented with it; it offers good line-of-sight propagation but minimal latency as opposed to satellites; it has high capacity and is seen to be more effective than BGAN (Broadband Global Area Network) satellites; it offers 'spot beams' for specific events coverage and is environmentally friendly.

"We have a pretty compelling technology here and I'm surprised that the mobile phone operators have not taken greater interest in it," said Tim Tozer, head of the Communications Research Group at the University of York, who is working on HAPs.

However, the HAP technology is yet to demonstrate a reliable, long endurance (over four months), safe and economic platform. The major drawback in pursuing this is lack of funding. "The problem is: are you funding a communications platform or an aerospace one? What we need are maverick funders," said Tozer, "to some extent the Japanese, Koreans and the Chinese are in that category."

"We also need partnerships across various sectors," added Tozer, "civil, military, government – and bring the aircraft fraternity on board so that HAPs can be flown where pilots are flying, even though it is an unmanned aircraft. So far, the pilots want it out of their space."

Nevertheless, Tozer believes that we may yet see HAP-based services from 2010.

OneSpin 360 MV nets all the design bugs, claims firm

OneSpin Solutions, once part of the German chip giant Infineon, and Siemens before that, has just launched a formal verification technology, dubbed OneSpin 360 Module Verifier (MV), which guarantees 100% bug-catching in designs.

"This package will allow a complete functional sign-off," said Dr Wolfram Büttner, managing director and CEO of OneSpin Solutions.

As it is a formal methodology, it does not require any test vectors or additional hardware. It also takes minutes rather than hours to complete.

There are three reasons why errors escape in a design. One of them is that a test vector does not manage to 'hit an error'; it simply fails to detect some errors. The second reason is that if a test vector does detect an error it may still be overlooked – so, there's a lack of sufficient observation power or so-called "blind spots". The third is that an error is spotted but not recognised, which is referred to as a "falsely accepted error".

"The only way of resolving these is by looking into the specification of the module (an IP block or a SoC). The task is to 'block' those error-escape routes. Traditionally, a lot of energy is spent on achieving this with test vectors, which may or may not work. We provide an algorithm that takes as an input a set of monitors/observers and checks whether they leave any code uninspected. If it finds such a code, it points it out for checking," said Büttner.

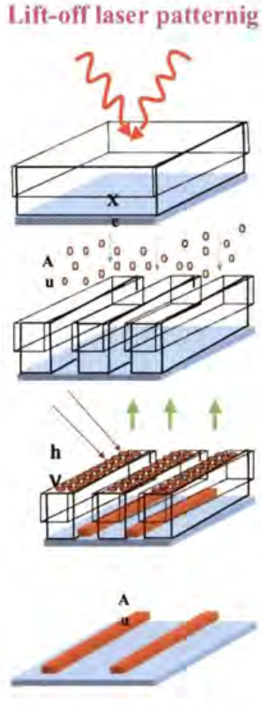
This algorithm, alongside the formal verification technique and raising the level of description of the monitor to the level of the specification, guarantees elimination of all the bugs in the design, claims the firm. "The most important thing to us is to ensure the consistency of the monitors," said Büttner.

The OneSpin 360MV is developed in a proprietary language – ITL of Interval Temporal Language. According to OneSpin's executives, Infineon and Siemens have been checking their own IP and systems with this solution for the past year, reporting no errors in the process.

Researchers develop laser patterning of metallic films

Researchers at the Hebrew University in Jerusalem have developed a novel process to pattern conducting wires at widths of below 50nm, employing a single laser pulse at low power densities.

The technology is based on laser desorption of a physisorbed – an inert buffer layer that evaporates at constructive interference stripes with the metal film on top, in so-called Buffer Layer Assisted Laser Patterning (BLALP). Slow annealing of the remaining "nano coverage grating" leads to fluid evaporation, retaining the pure metallic pattern via "soft landing" on the substrate.



Laser patterning technique on metallic films

"The utilisation of environmentally-friendly materials for buffer layers, e.g. Xe or water, makes this method an ideal candidate to replace the existing lithographic procedures that involve rather hazardous and problematic materials," said Professor Micha Asscher of the Department of Physical Chemistry at the University.

Asscher claims that grating periods of 0.2 microns can readily be achieved with laser technology at wavelengths of 193nm currently used in the industry. Therefore, conducting wires at widths of less than 50nm can potentially be obtained up to several millimeters in diameter.

The commercial advantage of the method is in its simplicity: a single 10ns laser pulse at low pulse energy densities (less than $50mJ/cm^2$) generates macroscopic (depending on the laser beam shape, typically 5mm diameter) patterns at widths in the range of 1000-50nm.

The next step in the research is to perform the laser-patterning procedure through a conventional mask that includes complex structures that will be transferred to a silicon substrate. In addition, experimental verification of the ultimate lateral resolution will be performed employing in-situ AFM and STM imaging.

UWB on track for EU launch despite interference

Regulators are keen to curtail the interfering power of UWB

UltraWideBand (UWB) will appear on the European market as early as next year, say industry experts. Simon Tonks, principal consultant at PA Consulting, based in the UK, said: "UWB will appear as a practical option in the next year or two."

UWB is a short range, high data-rate, radio technology that operates at distances of 10m. According to ETSI, by 2009 we'll see some 543 million UWB-enabled units in Europe alone.

UWB uses the same spectrum as conventional radio networks, however it sits too closely to the GSM spectrum's noise floor, to the greatest discomfort of the mobile phone operators. It has been shown that UWB devices affect the operation of mobile phones. The co-channel noise is seen as the main culprit for the interference, and it has been shown that it can completely block the GSM downlink.

Filtering at the receiver end is not likely to reduce the interference. However, there are two ways of minimising it, says PA Consulting, either by reducing the emission from UWB devices (power level, frequency range or duty cycle), which will be cheaper, or by changing the conventional networks to improve immunity, which will mean more cell sites and carriers, and that is more involved and expensive. "UWB emission level is the only effective control of interference," added Tonks.

The US frequency regulator FCC authorised UWB back in 2002, and in 2005 Japan approved it also but with a narrower spectrum and a detect-and-avoid protocol. The European regulator CEPT, on the other hand, is adopting tighter emission limits to protect the existing spectrum users. "CEPT would have put in a lot tougher technical conditions than the FCC and it's done in a way that there won't be a hardware cost associated with it."

Nevertheless, UWB is coming to Europe once the rules have been decided. "This is clear from the way CEPT is moving," said Tonks.

Image technology from UK firm e2v is currently being used in four different space programmes – ESA's Venus Express, ESA's Mars Express, NASA's Mars Reconnaissance Orbiter and ESA's Envisat. Its image sensing technology will help provide scientific data on the planets in our solar system. The technology is based on a specialist design of high resolution and high sensitivity CCDs, which have proved popular with missions of this type. A similar sensor also helped ESA's Mars Express to reach the Red Planet, which it has been orbiting for over two years.

* * *

This year, several electronics firms received the Queen's Award for Enterprise. Dage Precision Industries won an award for international trade, whilst no less than four other firms in this sector received an award for innovation: e2v Technologies, Siemens Communications, Smiths Aerospace Electronic Systems and Wolfson Microelectronics

* * *

Researchers at the Georgia Institute of Technology have developed a new technique for powering nanometre-scale devices without the need for bulky energy sources such as batteries. By converting mechanical energy from body movement, muscle stretching or water flow into electricity, these 'nanogenerators' could power a new class of sensors, portable electronics and implantable medical devices. They produce current by bending and then releasing zinc oxide nanowires, which are both piezoelectric and semi-conducting.

* * *

Bell Helicopter has created the world's first ever commercial tiltrotor, the BA609, (see below). In the design stages Bell used MathWorks's tools and model-based design, which helped minimise costs and improve the efficiency of the development process.

Optoelectronics devices developed using VLSI technology

Building optical devices based on standard VLSI technology promises to reduce the number of optic-to-electronic conversions in telecommunications infrastructure, leading to lower capital and operational expenditures, confirm researchers at the Hebrew University in Jerusalem.

The combination of two principles – the construction of a waveguiding structure in silicon VLSI technology and the control of the index of refraction of the core of the waveguide by the application of an external electric field – has been dubbed Optimos by the University.

The core of the Optimos structure is a few microns wide silicon-on-insulator (SOI) strip, which by being embedded in silicon oxide cladding is acting as a wave guide operating in the optical communication bandwidth. A thin conducting poly-silicon layer residing on top of the upper thin oxide layer forms a MOS structure similar to that of a standard MOS transistor. Two adjacent, parallel silicon strips constitute a capacitor, which can be charged by applying a voltage difference between them. These charges change the free charge carrier density, thus modifying the index of refraction. These changes in turn yield a change in the optical path of light propagating in the waveguide.

Professor Joseph Shappir of the Department of Applied Physics said: "The voltages required for this function are compatible with the operating voltages of the CMOS devices on the same silicon chip."

The integration of optical communication and digital electronics enables a spectrum of possibilities in data communication and telecommunications. The technology can be used in architectures to obtain modulation, optical switching or variable coupling. The University plans to licence the technology next.

Conducting nanowires promise to help ICs

Bionnections of Israel says it is developing a new type of conducting nanowires that will help the semiconductor industry deliver good chip performances at smaller transistor sizes.

As feature sizes approach 22nm, fundamental physical limitations will emerge making the existing top-down approaches to semiconductor manufacturing challenging and costly. While new techniques are being proposed for fabricating smaller transistors, the technical and cost challenges associated with the conducting interconnects remain unresolved.

"One of the key challenges confronting the interconnection schemes of future VLSI devices is that performance and reliability of commonly used conducting materials are deteriorated as their width is reduced to 22nm and below," says Dr. Miron Hazani, Bionnections's chief scientist. "Higher resistance, heat and sensitivity to electromigration failures become dominant obstacles with the reduction of interconnects' lateral dimensions. Existing processes of multilayer conductors become extremely complex and costly." Bionnections is proposing a new type of nanowire, based on a composite of carbon nanotubes (CNTs) with improved heat dissipation and durability to electromigration failure. In addition, they are easily positioned at "pre-determined" locations through a unique, patent-pending, self-assembly scheme. The superior heat conductance properties make these composites excellent candidates for applications in the field of IC cooling.

The nanowires are created with the help of lithographic techniques. As they feature chemical "handles", these are used to connect to other nanowires on the substrate with a bio-chemical process. This is a bottom-up process, starting with the positioning of just a few elements that code the interconnect "addresses", followed by several self-assembly and self-correction stages. Although the new process is primarily a production process, it will still have implications on new design rules.

Bioconnections is in discussion with semiconductor firms over its technology.

Eurosmart, the 'voice' of the smart-card industry, reported that 2.6 billions smart-cards have been shipped in 2005 and some 3 billion are expected to be shipped in 2006. The industry's activity has increased by 22% in 2005 worldwide and will remain at a steady 19% growth course over 2006. The mobile communications sector is still the largest and fastest growing segment with almost 1.4 billions cards shipped in 2005. Smart-cards in government and health projects, such as electronics passports, grew by 25% in the same year, and over 20 million cards were shipped for contactless systems in transport applications.

* * *

Shoots of recovery are showing in the UK electronics manufacturing industry, says Plimsoll Publishing. This encouraging news however is down to only 23 of the UK's largest 100 companies, even though this sector accounts for 84% of the total electronics manufacturing industry, up from 79% four years ago. In the past four years, these 23 companies have increased sales by 31%, improved profits by 145% and increased staff levels by 8%. David Pattison, senior analyst, said: "These 23 companies are setting themselves apart from the other major players, who look tired by comparison. You don't pull in results like this over such a length of time by accident. They are telling us something about the direction of the market, a sort of elite resurgence".

* * *

Future Horizons predicts the TV set-top box market will increase from 57.3 million units in 2005 to 143 million units in 2010, a growth rate of 20%.

The highest growth will be in the digital subscriber sector as the telecom operators take on the cable and satellite operators. This in turn will be reflected in a very strong growth of semiconductor sales in this sector as more features are added to the set-top boxes.

The satellite industry hopes to bridge the 'digital divide'

Satellite operators are the next group of companies to vie for the attention of broadband subscribers. EADS Astrium is just one operator keen to deliver such services via its satellites.

"Five to eight million premises that are willing and able to pay for broadband have no access to these services, mainly because they are in remote or underdeveloped regions," said Nick Akers, Payload Systems Engineer at EADS Astrium. "Today the majority of the population has broadband access via terrestrial means, but in the future the satellite broadband delivery will bridge the 'digital divide'."

EADS Astrium is resorting to using integrated processors to deliver cost-effective broadband payloads to users

Satellites are seen to be able to offer highly flexible, spectrally-efficient payloads but to make them accessible to the general public, they have to offer lower cost delivery, compatible with terrestrial services.

"Current satellite solutions are not affordable due to the high cost of user terminals, antennas, maintenance and other, but they are coming down in costs," said Akers. To lower these costs, EADS Astrium has started using DSPs in its latest generation of satellites, such as Inmarsat-4, as the processors will allow dynamic allocation of bandwidths to different areas, thus offering flexibility of bandwidth and transmitted power.

One proposal is to use one or more satellites with 100 beams, throughput of 50GHz and 5000 channels in the Ka band to deliver broadband services. The duplex will consist of DVB-S2 downlink and DVB-RCS uplink. "They will offer full adaptive coding and modulation for a better quality of service to more users," said Akers.

There are a number of high-capacity satellite systems in orbit or currently in construction, such as Anik F2 (Telesat) or Wildbird, that could cater for such services.

However, there are doubters that this could work economically.

"Inmarsat's BGAN (Broadband Global Area Network) is a highly complex, high-tech satellite that will be used for the Ka band – why?" asked Tim Tozer, university lecturer in York. "Inmarsat-4 is an expensive satellite and they've gone to a high-tech solution [based on DSPs] instead of many, bog-standard single Ka-band satellites."

The other issue with satellite delivery of broadband services are the obstacles; rain, clouds and heavy vegetation can all stop a satellite signal from reaching its destination.

According to EADS Astrium's reports, by 2010 some 70% of the European population will subscribe to broadband services.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USING A HIGHLY INTEGRATED DSP

TOP 10 TIPS

What are my system requirements?

The first task in system design is to review the overall system requirements, which drive all other decisions. Is the application intended to work with audio, video or RF? At which rates? Using which standards? Which other functions are needed? Is it intended for a mobile appliance where power is at a premium? Such basic decisions often dictate which peripheral functions a system requires.

For instance, systems in the telecom infrastructure market require a far different mix of peripherals as those intended for portable media or wireless handsets. Although telecom systems share some requirements with other application areas, telecom infrastructure designers are chiefly concerned about high channel densities and throughput, along with low cost per channel.

Power per channel is a factor as well in telecom infrastructure, which is impacted mostly by the active power of the DSP. In mobile applications, where battery drain is a chief concern, standby power is very important.

Is there an existing mix of integrated peripherals that closely matches my needs?

Create a list of must-have and secondary functions, and investigate which of them are available integrated in a device. Even engineers who closely follow the latest chip offerings are constantly amazed at the level of integration that each new generation of devices brings, and the trend will only continue. Thanks to process improvements, one chip can accommodate digital, analogue and even RF circuitry. It is difficult to integrate analogue and RF capabilities with a DSP, and adding digital peripherals to a device isn't always easy either. Chip designers can't simply drop in digital peripherals; they must ensure that all subsystems have the proper timings to meet diverse industry standards.

Now, consider an overview of some application areas and how their peripheral mixes differ. In telecom infrastructure systems, a key requirement is plentiful high-speed I/O. Designers working on such applications might consider a device that includes among its peripherals multichannel buffered serial ports (McBSPs); a slave port for UTOPIA (Universal Test and Operations PHY Interface for ATM); a host-port interface; and a PCI interface. By implementing industry-standard interface schemes, these peripherals can eliminate multiple external chips.

Such a device can be used in video infrastructure applications. The drivers for video infrastructure are multi-channel (i.e. higher channel density) and multi-format (e.g. MPEG4, H.264, WMV9 and other codecs). Integration at the chip level can be seen with peripherals like PCI, video ports, external memory interfaces and also the integration up to 1MB of total memory on-chip. Integration at the chip level enables integration at the board level.

To see how analogue and RF can integrate with digital logic, take a look at a device targeted at Bluetooth implementations where low cost, low-power consumption and a small form-factor are essential requirements. A recent SoC combines a digital baseband section, direct RF sampling along with built-in self-test, memory and power management. In operation, a low-noise amplifier boosts the received signal. Next, a multitap direct sampling mixer (MTTDSM) performs RF sampling and then runs sync filtering and downconverting to an intermediate frequency. The signal proceeds through a sigma-delta A/D converter, which runs at half the IF amp's rate to reduce power consumption. Now, a digital receive block drops the data rate to a second IF frequency, after which FIR filtering removes residual close-in interference. The signal is finally down-converted to a zero IF. All these diverse functions fit on one chip.

Must you make performance tradeoffs with on-board peripherals?

As an example, a DSP used for motion control integrates analogue functions such as data converters, it might also limit the DSP's performance. On the other hand, a DSP used for video infrastructure may not be able to afford any performance reductions arising from analogue integration, though it can successfully integrate digital peripherals such as video interfaces.

Peripherals, of course, don't come for free because they take up chip area and power, but the system payoff can be big. For instance, the TMS320C6416T incorporates a Viterbi Decoder Coprocessor (VCP) and a Turbo Decoder Coprocessor (TCP). These two alone account for roughly 10% of the chip area and 10% of the total power, which is quite acceptable for applications that demand significant speeds in channel-decoding operations. In fact, with these coprocessors a system can improve its channel throughput by four times, which is well worth the 10% increase in size and power.

Are some peripherals or memories better placed on or off the chip (partitioning)?

If a system needs A/Ds or D/As, the engineer must determine whether on-board converters supply enough I/O lines, and whether they run at the required sampling rates and resolution. If not, how easily can the selected DSP work with external data converters?

In some video infrastructure systems, the memory requirement from a total system perspective is very large. In some cases, it makes sense for designers to select a DSP with a 256kB to 1MB on chip to complement other memories on the board, as opposed to seeking a device that integrates more than 1MB or 2MB of memory on the DSP chip.

If there's no exact match of peripherals to application requirements, can you program the on-chip processor to perform the needed extra functions?

Even though the selection of integrated peripherals can vary widely, an engineer cannot find a function block that meets some specialised needs, which is often the case in products that chase evolving standards. In that case, a programmable DSP might provide the required flexibility.

An illustration comes from broadband communications, where DSL (digital subscriber line) is a popular method for content delivery. However, there are a number of standards in use today and improved schemes are being developed. With the proper DSPs, designers can adapt their systems quickly to work with any of these standards.

For example, the single-chip DSL customer-premises equipment (CPE) modem supports a variety of standards over both POTS and ISDN phone lines. For ADSL (asymmetric DSL), the device naturally works with the existing G.dmt (discrete multitone modulation) and

At the system level, engineers are accustomed to making tradeoffs among the three Ps: performance, power consumption and price. With today's highly integrated DSPs, though, a fourth P – peripherals – can impact decisions related to the first three and it adds a new set of design considerations. When selecting the right DSP designers must pick the SoC that has the optimal peripheral mix to best meet requirements for the entire system. And the choices of on-chip peripherals are wider than ever because it's now feasible to put analogue and RF circuitry on the same chip as digital logic. Here, we list some of the key questions and discuss possible considerations that might have an impact on your next system design.

G.lite methods. Engineers can also program it to handle newer modulation techniques such as G.dmt.bis, also known as ADSL2 or ADSL2+, which improves modulation efficiency to increase the downstream data rate and provides better performance on long lines where S/N ratios are weak. The device further works with Extended Reach ADSL.

Would the application benefit from multiple cores, such as a DSP/RISC heterogeneous combination?

Consider interrupts from a user interface. If a RISC core was to implement multimedia tasks on an audio player, something as simple as the user adjusting loudness would require that core to pause audio processing to handle the volume-control interrupt. This interrupt handling could result, at best, in an operator interface that does not react smoothly and, at worst, to small gaps in the audio signal.

Recall the DSL modem chip and note that it consists of two CPU cores: one based on the TMS320C62x and the other a MIPS32 4KEc. Together they implement a DSL PHY (physical layer), an analogue front-end subsystem, a line driver/receiver, power management and a broadband controller for an end-to-end bridge/router for residential gateway applications. Besides the C62x core running at 200MHz, the DSP subsystem contains hardware accelerators for dynamic adaptive equalisation that enables higher data rates. This configuration realises all the operations required on the transmit and receive paths including echo cancellation, digital filtering, Trellis coding, Reed Solomon forward error correction, decimation and interpolation. The network subsystem is based on the MIPS core, cache memory and networking peripherals such as a USB controller, 10/100-Base Ethernet MAC/PHY and ATM (asynchronous transfer mode) subsystem.

How do you assign tasks to the different cores in an optimal fashion?

In general, a DSP is best suited for repetitive, numerically intensive tasks, whereas a microcontroller is best for control-oriented applications and interrupt handling. Again, considering a portable music player, note that trying to implement audio algorithms on a RISC core isn't optimal because it takes on average three times as many cycles to perform multimedia algorithms there than on a DSP core.

How easy is it to move data among the cores and on-chip peripherals?

As systems integrate ever more peripherals, issues of data bottlenecks start to arise. Is it possible to get enough data on the chip fast enough? How can the chip move it around internally so that the individual elements are used most efficiently? Again consider the DSL modem. The chip's EMIF external memory interface allows both cores to access the complete external memory address range. In addition, two high-speed integrated serial interfaces enable interoperability with 802.11b/g wireless LAN devices, as well as providing connectivity for external expansion devices.

Interconnecting all the peripherals in the device, including networking subsystems and memory, without creating bottlenecks presents an interesting challenge. The device's designers overcame it by adding an on-chip crossbar switch interconnect fabric that serves as both a peripheral bus as well as an internal system bus. Thus, multiple data transfers can take place simultaneously between different DMA master-slave combinations. Experience shows that such a switched central resource requires only about 15k more gates than a conventional bus, a small investment given the tremendous improvement in performance.

What are the system power implications? Does the chip require a number of voltages and how well does it do at generating them, such as from a single supply voltage?

Many of today's integrated DSPs run off of multiple core voltages. For example, different voltages may be used for the core and for the I/O in an effort to reduce system power.

Again consider the DSL modem chip, which derives multiple voltages from a 3.3V supply using on-chip power management. A buck converter with an integrated Mosfet generates 1.5V/1A for the digital core, and a boost converter with an external FET generates 12V for the line driver. The chip also integrates circuits for power-on reset and loss-of-power detection.

Power also involves cooling. Designers working on systems for telecom infrastructure, where the high-performance DSPs draw considerable power, must pay strict attention to thermal issues such as airflow over boards, whether to use fans and if so which types, and how to heat-sink some devices. By adding the proper thermal design engineers can get more performance out of their systems. DSP vendors can help by leveraging the latest manufacturing capabilities such as the 90nm process technology.

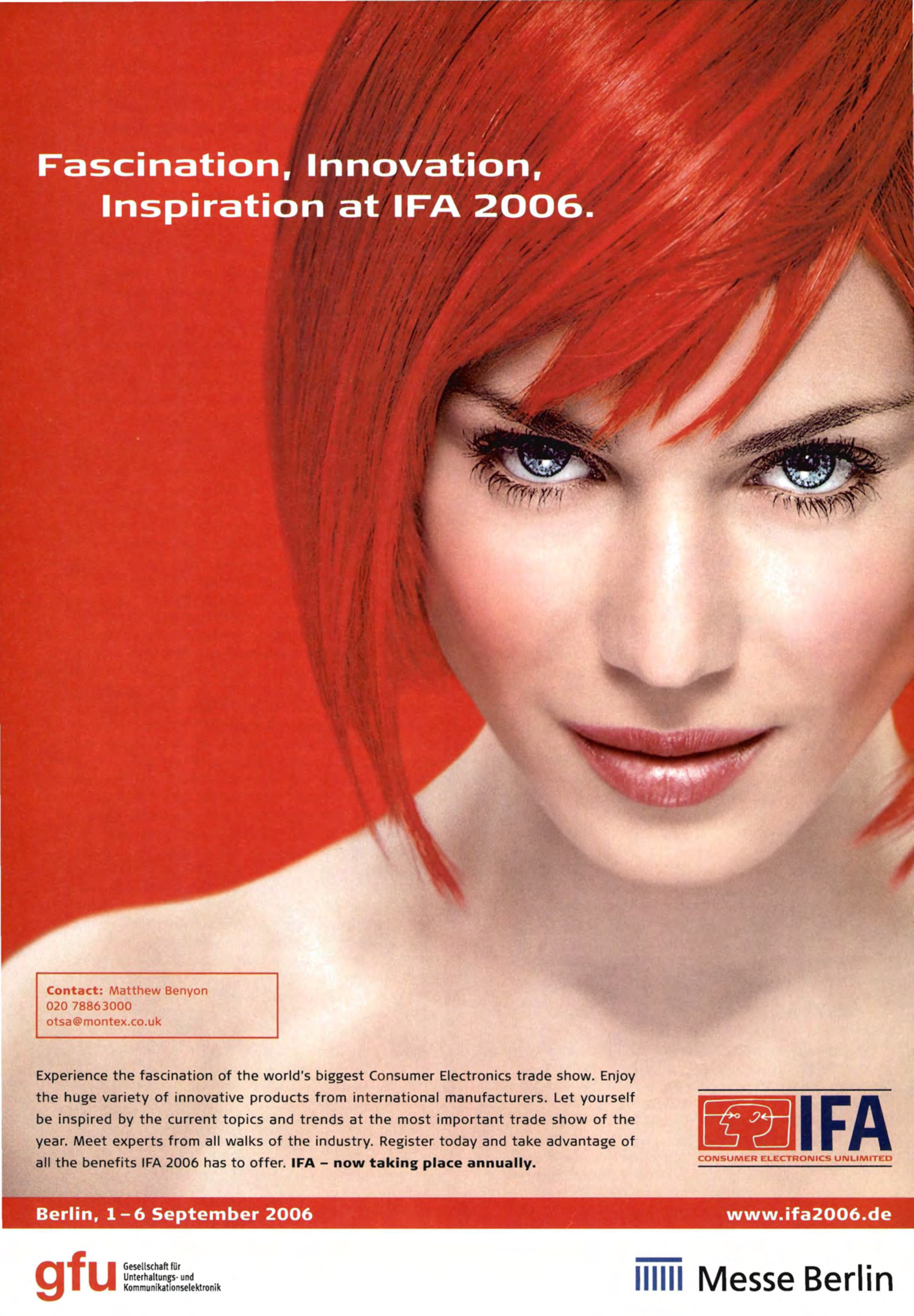
Does the chip supplier have a roadmap that tells you what integration to expect in the future?

Process technologies continue to advance and engineers should ask their suppliers if they can ensure that today's designs can easily scale down to devices using smaller geometries, which give even further advantages in terms of speed, size and cost. Vendors must make considerable investments in wafer fabs to ensure continuity of supply.

Whether designing for audio, video, imaging, RF, telecom infrastructure or even industrial applications, keep tabs on industry trends, because new SoCs are coming off the fab lines at an increasing rate. There could well be one that allows you to cut the development time and cost.

This month's Top Ten Tips were supplied by Thomas Brooks, Senior DSP Product Manager at Texas Instruments.

If you want to send your tips to us, please contact the Editor at EWeditor@nexusmedia.com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Going green could pay dividends

Richard Martin explains how electronic manufacturers can benefit from improving their environmental performance

With significant changes to environmental legislation on the horizon, businesses across the electronics industry are having no choice but to confront their environmental obligations.

While many larger companies have become more switched on to environmental issues in recent years, smaller businesses with more limited time and resources are in danger of lagging behind and could risk prosecution and hefty fines if they fail to comply with the legislation governing their activities.

The recent SME-environment survey (2005) of 5,554 UK small businesses found that as many as 86% of those asked could not name any environmental legislation and only a quarter had an environmental policy in place. Not surprisingly, 58% of small businesses said they would like more help and advice on environmental issues.

Keeping up-to-date with environmental legislation and improving environmental performance is not just good for the environment; it can also result in sound business benefits, of which smaller businesses may be missing out.

Making changes to environmental behaviour – in particular by becoming more resource efficient – can have a real impact on the bottom line, particularly with increasing landfill taxes and rising costs for disposing of hazardous waste. By implementing simple low-cost measures most businesses can reduce waste by 1% of turnover – adding up to significant savings over time. And waste is not just discarded materials, it includes wasted energy, packaging and excessive use of raw materials and water.

In addition, new environmental legislation such as WEEE and RoHS provides an opportunity for businesses to re-assess their product portfolio and invest in cleaner designs that are easier to reuse and recycle. These improved products could not only prove cheaper to produce but also give the business a competitive edge. This is particularly true as larger businesses and customers become increasingly keen to deal with companies with good green credentials.

Unfortunately, single measures such as recycling paper in the office are not enough to deliver real change. Businesses wishing to gain a real edge over competition should consider implementing an environmental management system (EMS). This provides a structured approach to managing a business's environmental performance and must include certain elements, as required by, for instance, the BS 8555 or ISO 14001 standards. Businesses can choose to be certified that they meet the requirements using either internal mechanisms or external certification organisations.

An EMS can bring about a number of benefits. Cost savings can be achieved through continuous assessment of more efficient use of materials and energy. Independent certification of the system to a recognised standard can help improve the public image of a business and relationships with customers and suppliers. An EMS can also help businesses manage their environmental issues and, therefore, comply with environmental legislation, avoiding enforcement action and associated liability costs.

> **“Keeping up-to-date with environmental legislation and improving environmental performance is not just good for the environment; it can also result in sound business benefits”**

If a company is serious about bettering its environmental performance it needs buy-in from all staff from the chief executive to the shop floor. It is usually worthwhile appointing a member of staff to be responsible for driving environmental changes but it is crucial that the changes, the reasons for them and their business benefits are communicated to all employees.

In order to stay ahead in this competitive and ever-changing market, it is vital that small businesses start improving their environmental credentials. The NetRegs website (www.netregs.gov.uk) was set up by the UK's environmental regulators to help small businesses understand their environmental obligations – is a good starting point for businesses seeking straightforward guidance on environmental legislation.

Richard Martin is Programme Manager at NetRegs

Giant's Challenges

These are testing times for the Japanese once untouchable of consumer electronics firms. **Juan Pablo Conti** delves into the issues surrounding its future

"The fact that the Japanese government has allowed all-wave receivers to be used for commercial purposes has encouraged large and small radio companies – including ourselves – to manufacture them". In the 60 years that have passed since these words were written in Tokyo by one of Sony's two founders, what he then called a "small radio company" has grown to become one of the world's top brands in consumer electronics.

During much of that period (notably from the moment the company introduced the Walkman in 1979 and, with it, kick-started the personal audio revolution), Sony even managed to establish a commanding leadership of the market, remaining virtually out of reach of the competition.

But then things suddenly changed. A combination of other Asian OEMs previously seen as no match for Sony now becoming aggressive competitors, old software giants successfully trying their luck in hardware design and emerging new competitors have all shaken the company's grip of the world's living rooms. So where did it all go wrong?

Humble beginnings

Masaru Ibuka was indeed right to call Sony (or Tokyo Telecommunications Engineering Corporation, as the business was initially registered) a "small radio company" in the Founding Prospectus that he drew up in 1946. The Second World War had just ended and much of Japan was badly destroyed. People were eager for news from the rest of the world, but their radios had either been damaged by war action or had their shortwave units disconnected by the military police to prevent them from tuning into enemy propaganda.

There was a huge demand for radio service repair, and that's exactly what Ibuka and his former military colleague Akio Morita set out their new business for. Their factory would also build shortwave adapters that were used to turn medium-wave radios into all-wave receivers.

By 1955, the company had designed Japan's first transistor radio. Two years later, the world's first pocket transistor radio was launched, initiating a tradition of cutting edge innovation in the consumer electronics sector (see panel Sony's famous inventions).

But Sony was still a small radio company. Legend has it that Morita, credited as one of the world's great marketing pioneers, felt so offended when powerful American clockmaker Bulova ordered 100,000 radios to be manufactured carrying the Bulova brand that he simply turned down the precious offer. "Fifty years from now," he replied, "I promise you that our name will be just as famous as your company name is today."

Troubled figures

Still headquartered in Tokyo, Sony Corporation employs just over 150,000 people worldwide. The conglomerate is made up of five business segments. Of these – and by far – the most important is the Electronics division, which has audio, video, information and communications equipment, semiconductors and components as its main products. The other segments comprise the Sony Computer Entertainment group (makers of the PlayStation line of hardware and software), Sony BMG Music Entertainment group (for recorded music), Sony Pictures Entertainment (movies) and the Financial Services branch (banking and insurance).

The Electronics group, based in San Diego, California, generates more than 65% of all Sony sales, followed by the games (approximately 10%), pictures (10%), financial (7%) and music (3%) segments. Revenue is evenly distributed between the US, Europe, Japan and the rest of the world, with each of these four main regions contributing approximately one quarter of total Sony sales.

The company's last published annual revenue figures may look impressive to the untrained eye. After all, $67bn (for fiscal year ended March 2005) does sound like a vast amount of money. However, when you consider that only $1.5bn of that was net income, it isn't hard to see that this is an inefficient organisation. In fact, during the previous year, Sony actually lost money for the first time in a decade.

The most worrying indicator for the Japanese company is that its core Electronics segment is the one faring the worst at the moment. The gradual decline started almost four years ago and – with profit margins for a number of consumer products quickly evaporating – this flagship business unit made a loss in 2004, which then widened one year later.

"At times, they've only really been pulled back into the black by the PlayStation division, or,

Opposite page: Sony's debut Blu-ray disc home player
Below: A shot from the TV advert for the Sony Bravia line of LCD displays

SONY'S FAMOUS INVENTIONS

- Pocket transistor radio (1957)
- Trinitron TV (1968)
- Walkman (1979)
- CD format (co-developed, 1982)
- 3.5-inch floppy disc (1983)
- Digital Betacam (professional broadcasting)
- PlayStation console (1995)
- Vaio laptop (1996)
- DVD format (co-developed, 1998)
- Flash memory stick (1998)
- Blu-ray format (2006)

occasionally, when they have a massive movie such as Spiderman 2, from which Sony Pictures Group makes a ton of money," notes Paul Jackson, principal analyst with Forrester Research.

Slow reaction

So what's hurting Sony? "In general, there's a lot more competition in the consumer electronics market," explains Jackson, "whether that's from PC makers like Dell, Gateway and HP or from new entrants into the consumer electronics world like LG or Samsung, who were always considered as the cheap sort of 'copyists'. So you'd have your high-end Sony products, then you'd have your middle-ground Panasonic and Philips products and then there'd be these sort of 'also-ran brands', which used to be LG, Samsung and the like. But Samsung in particular has done a very good job at raising the perception of its brand premium."

What Samsung also did was to leapfrog Sony in the development of LCD (liquid crystal display) technology. While Sony decided to stay a little longer in the CRT (cathode ray tube) business, operating factories in Japan and the rest of the world dedicated to assembling bulky screens that the general public was beginning to turn their back on, Samsung was busy investing in LCD fabrication process. So far behind was Sony left that, by the time it finally reacted, it was forced to partner the Korean vendor to "jointly" manufacture the new flat panels.

But if it took Sony a while to realise just how quickly the demand was evolving for this particular product, Jackson believes the company is now rediscovering the lost track: "Their new Bravia range of LCD TVs is actually very good. They are well designed, at a price premium, and they are uniquely Sony – whereas for the past two or three years what they had was arguably almost a re-batched Samsung TV."

As if having other OEMs eating into its traditional market share wasn't enough to keep Sony on high alert, a whole new competition front has all of a sudden been presented by what were supposed to be just software or PC developers. Microsoft, first – with its successful entry into the games console market through the Xbox product – and Apple Computers, more recently (with its even more successful iPod portable audio player) are largely responsible for Sony's current woes. Apple has even recently re-launched the Mac Mini as an audio and video player connected to the TV, and it's offering a new hi-fi system based on iPod as the music source.

Playing the gaming game

Sony knows it might now be too difficult to regain the lead it once enjoyed on the portable audio market, where its digital-age version of the Walkman has tumbled to sixth place in the US, and even in Japan iPod's 51% share of the portable digital audio market dwarfs Sony's 16% figure.

However, when it comes to video games, the Japanese company is not prepared to loosen its firm grip on this profitable segment. "Oh, and by the way, Howard, not only did PlayStation 2 outsell Microsoft's new Xbox 360 this holiday season, but so did the PSP," casually said Kaz Hirai, president and CEO of Sony Computer Entertainment America to Howard Stringer, Sony's new – and first non-Japanese – chairman and CEO during a high-profile presentation at this year's International Consumer Electronics Show in Las Vegas.

Last year, the PSP (or PlayStation Portable) became Britain's fastest-selling games console, with more than 185,000 of them sold in the first four days of its retail life. By January, more than 10 million units had been shipped worldwide.

And while the PS2 is already reaching a natural saturation point after six years on the shelves, Sony is seriously banking on the success of its latest version – the PS3, re-scheduled for a November global launch. What's making Sony – and hardcore gamers – so excited is the sheer processing power the new gadget will boast.

The Cell (a 64-bit, multi-core processor clocked at 4.6GHz and co-developed by Sony, Toshiba and IBM) is widely expected to be the most powerful piece of silicon to sit in a PS3 owner's home. Forrester Research's Jackson remains cautious, though: "They've taken a huge risk in terms of the type of architecture they've designed, in that it's extremely powerful – almost absurdly powerful for something that is just designed for playing video games. With that comes a tremendous risk in terms of the cost of the components and being able to get enough of them in time for a global rollout."

The Holy Blu-ray?

Mind you, the PS3 wasn't actually designed 'just for games'. Its optical drive technology will be no other than Blu-ray, the high-density storage format developed by Sony to replace DVDs with a next-generation optical disc fit for the high-definition (HD) video era. Single-layer Blu-ray discs, which Sony recently started selling for around $25 each, are able to store up to 25GB. Dual-layer discs are expected later in the year, and these will be able to hold a massive 50GB of data, more than enough for a director's cut HD movie and accompanying interactive features.

Sony has managed to attract some 170 companies to the Blu-ray Disc Association, from major Hollywood studios (Twentieth Century Fox, Walt Disney, Warner, Paramount and, obviously, Sony Pictures) to competing equipment manufacturers (Apple, Dell, HP, Samsung, Panasonic, LG, Hitachi, Sharp and others). The format is backward compatible with the DVD standard, which means potential buyers of new Blu-ray boxes will be able to use them to play back their existing collections.

What they might not be able to do, though, is to play every new HD movie they buy on them. The ongoing standards battle between Blu-ray and the Toshiba-led HD DVD camp remains far from being solved, with each faction's spec now finalised and ready to do battle on the high street.

Forrester Research analysts have recently concluded that Blu-ray has a stronger chance of winning in the end: "We currently see that Blu-ray has the slight edge in terms of the number of movie studios and content providers who are in that camp," says Jackson. "And of course there's a huge advantage if Sony can roll out the PS3 with that built-in, using it as a Trojan horse for getting Blu-ray into people's homes. Because they will undoubtedly sell 10, 15 or 20 million of those over the next two or three years, far more than they are going to sell of the fairly expensive standalone Blu-ray players."

The first of such players will be – somewhat ironically – a Samsung. The BD-P1000 goes on sale on 25 June in the US, and it will initially retail at $1000. And it's not that Sony won't have its own gadget to compete with Samsung. The BDP-S1 Blu-ray player will start shipping only a couple of months later and equally cost $1000. But unlike Samsung, which has plans together with most other OEMs to build dual-format players and PC drives supporting both Blu-ray and HD DVD, Sony will exclusively and proudly stick to the technology it invented. This can only make the decision over whether for those consumers worried about the next blockbuster video being able to run on their expensive new toy.

It has been a troubled start to the new millennium for the once undisputed world leader of consumer electronics, and only time will tell how much of the damage done by a smart bunch of competitors is just beyond repair. "The next 3-5 years will represent a period of change for Sony as they look at creating networked home products and investigate how they can make money not just from devices but also from services such as downloads and online games," says Jackson. "Their strong brand still carries a lot of cache with consumers, but they will need to be more responsive to market changes and those agile competitors."

Jackson stresses how Sony's new chairman Stringer is trying to shift emphasis from unprofitable legacy technologies such as CRT TVs and robots to new business models. "So far he has had some early successes, but is almost working against a strong 50-year-old corporate culture".

Opposite page: Sony's VAIO FS series laptop
Above: Sony's QRIO robot, A Sony professional HD camera and the Sony Walkman

SONY IN BRIEF

- Founded: 7 May 1946 by Masaru Ibuka and Akio Morita
- Corporate headquarters: Tokyo, Japan
- European headquarters: Berlin, Germany
- Electronics group headquarters: San Diego, California
- Chairman and CEO: Sir Howard Stringer
- President and Electronics CEO: Ryoji Chubachi
- Subsidiaries: 928 worldwide
- Employees: 151,400
- Annual sales: $67bn (fiscal year ended March 2005)
- Net income: $1.5bn (fiscal year ended March 2005)

HAND-HELD DUAL SYNCHRONOUS DDS SIGNAL GENERATOR

A HAND-HELD DUAL SYNCHRONOUS DIRECT DIGITAL SYNTHESIS (DDS) SIGNAL GENERATOR HAS BEEN DEVELOPED BY **ZHONGWEN JIN** AND **WUQIANG YANG** FROM THE SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING AT THE UNIVERSITY OF MANCHESTER, EMPLOYING TWO DDS CHIPS, CAPABLE OF PRODUCING TWO WIDE-FREQUENCY-RANGE SIGNALS WITH FULLY ADJUSTABLE PHASE SHIFT

Signal generators are useful in the laboratory. Often, two synchronous sine-wave signals with a certain phase difference are required. Some application examples include phase-sensitive demodulation (PSD), signal mixer, vector generator, selective voltmeter and rotational torque induction. In those cases, highly versatile signal generators, which can provide full control over amplitude, frequency and phase, are needed.

Direct Digital Synthesis (DDS) is a technique of using digital data processing as a means to generate a frequency- and amplitude-tunable output signal referenced to a fixed-frequency precision clock source and then performing a digital-to-analogue conversion in the form of a single chip. Using low cost and high performance DDS chips, a hand-held dual synchronous DDS signal generator has been designed. This instrument can generate two signals using two DDS chips as a synchronous pair. The phase of one signal can be shifted with respect to the other to produce the required phase difference.

The resulting instrument is of low cost and has all of the advantages of DDS technique. It would be very useful for applications where two signals of adjustable phase are required.

DDS technology

While the amplitude of a sine wave is non-linear, with time the angle is a linear function of time in nature. It changes from 0 to 2π and repeats itself for each cycle of a sine wave as shown in **Figure 1**.

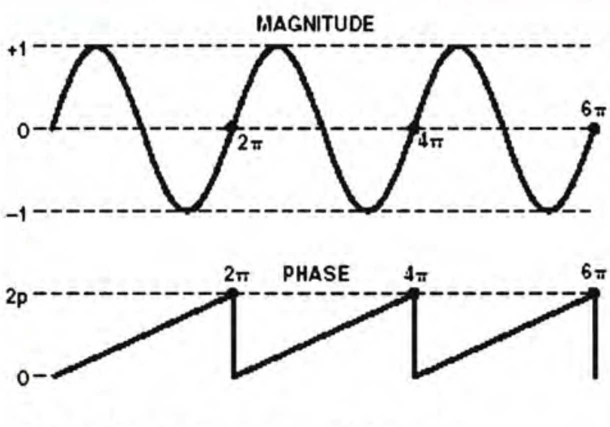


Figure1: Amplitude and phase of sine wave

A DDS produces a sine wave at a given frequency. The frequency depends on two variables: the reference-clock frequency and the binary number programmed into the frequency register, such as a tuning word. The binary number in the frequency register provides the main input to the phase accumulator. If a sine look-up table is used, the phase accumulator computes a phase (or angle) address for the look-up table, which outputs the digital value of amplitude — corresponding to the sine of that phase angle — to a digital-to-analogue converter (DAC), which converts that number to a corresponding value of analogue voltage or current. To generate a fixed-frequency sine wave, a constant value (i.e. the phase increment), which is determined by the binary number, is added to the phase accumulator with each clock cycle. If the phase increment is large, the phase accumulator will step quickly through the sine look-up table and thus generate a high frequency sine wave. If the phase increment is small, the phase accumulator will take many more steps, generating a flow-frequency waveform accordingly.

Knowing that the phase of a sine wave is linear and given a reference interval (i.e. clock period), the phase rotation for that period can be determined by:

$$\Delta Phase = \omega dt \tag{1}$$

Solving for ω :

$$\omega = \frac{\Delta Phase}{dt} = 2\pi f \tag{2}$$

Solving for f and substituting the reference clock frequency f_{clock} for the reference period:

$$\left(\frac{1}{f_{clock}} = dt\right) :$$

$$f = \frac{\Delta Phase \times f_{clock}}{2\pi} \tag{3}$$

In AD7008 DDS ICs from Analog Devices, two 10-bit amplitude multipliers are provided, allowing easy implementation of the I (cosine) and Q (sine) amplitude modulation. The 20-bit IQMOD register is used to control the amplitude of the cosine and sine signals. IQMOD [9:0] controls the I amplitude and IQMOD [19:10] controls the Q amplitude.

$$I + Q = A\cos\omega t + B\sin\omega t = R\sin(\omega t + \theta) \tag{4}$$

Where

$$R = \sqrt{A^2 + B^2}$$

and

$$\cos\theta = \frac{B}{R}, \quad \sin\theta = \frac{A}{R}$$

The output signal of amplitude R and phase shift θ is produced by summing the I and Q signal. The parameters R (amplitude) and θ (phase) of each signal are dependent on the value of A and B. Vice versa, given the desired amplitude R and phase shift θ, the required values of I and Q can be determined:

$$A = R\sin\theta \tag{5}$$

$$B = R\cos\theta \tag{6}$$

Where $0 \leq R \leq 1V_{ppk}$ and $0° \leq \theta \leq 360°$

By storing the determined A and B values (10 bits) into the IQMOD register, a signal of desired amplitude R and phase shift θ can be produced at the DDS chip output.

PIC18F452 microcontroller and MPLAB ICD

The PIC microcontroller PIC18F452 is probably the easiest 8-bit microcontroller. It has large linear register space that can be accessed simply and multiple index registers able to operate like a data stack with push and pop. It has the following features:

- C compiler optimised architecture/instruction set
- Linear program memory addressing to 32Kbytes
- Linear data memory addressing to 1.5Kbytes
- Sufficient I/O ports, PORTA, PORTB, PORTC, PORTD and PORTE
- Supporting high-speed flash program memory
- Supporting external interrupts with programmable triggering edge
- 16-bit wide instructions, 8-bit wide data path
- High current sink/source 25mA/25mA
- Addressable USART module, supports RS-485 and RS-232
- Parallel Slave Port (PSP) module
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code protection
- Power saving SLEEP mode
- Compatible 10-bit ADC with fast sampling rate.

An all-in-one debugger and programmer solution MPLAB ICD2 is a low cost, real-time debugger and programmer for the selected PIC microcontroller. Using the in-circuit debug functions, programs can be downloaded, executed in real time and examined in detail with the debug functions of MPLAB IDE software. Variables, breakpoints and single step operation can be set by symbolic labels in C or assembly language source code. The secret behind in-circuit debugging is the use of two dedicated hardware lines that control in-circuit programming of the device and debugging on-chip firmware through proprietary. The ICD2 debug functions are built in the microcontroller and activated by programming the debug code into the target processor.

The MPLAB ICD2 connects using USB between a PC operating with MPLAB IDE and their circuit board being developed. It acts as an intelligent interface and translator between the two, allowing engineers to look into the active target board's microcontroller, view variables and registers at breakpoints with MPLAB IDE watch windows. A breakpoint can be set to halt the program at a specific location. The program can be single-stepped or run at full speed. At breakpoints, data and program memory can be read and modified. Additionally, the MPLAB ICD2 can be used to program

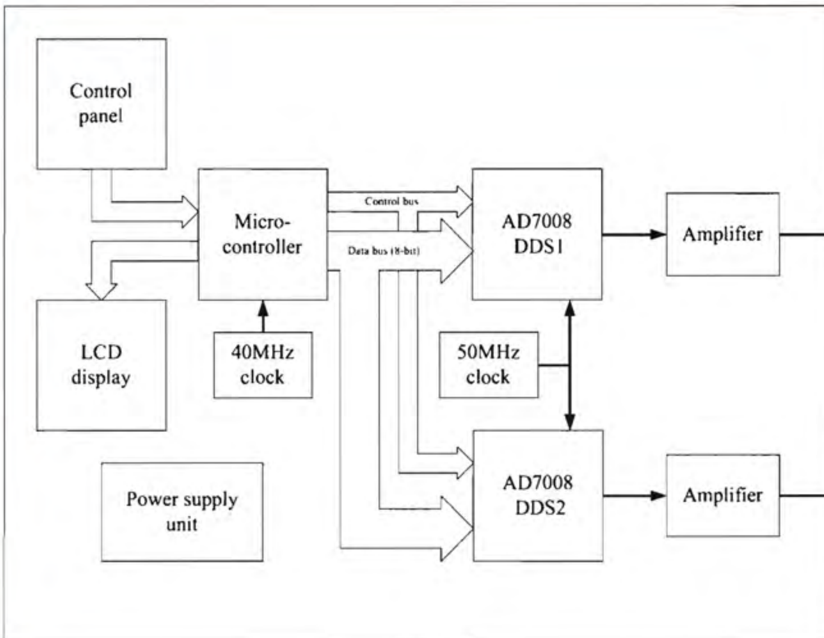


Figure 2: Block diagram of system's hardware design

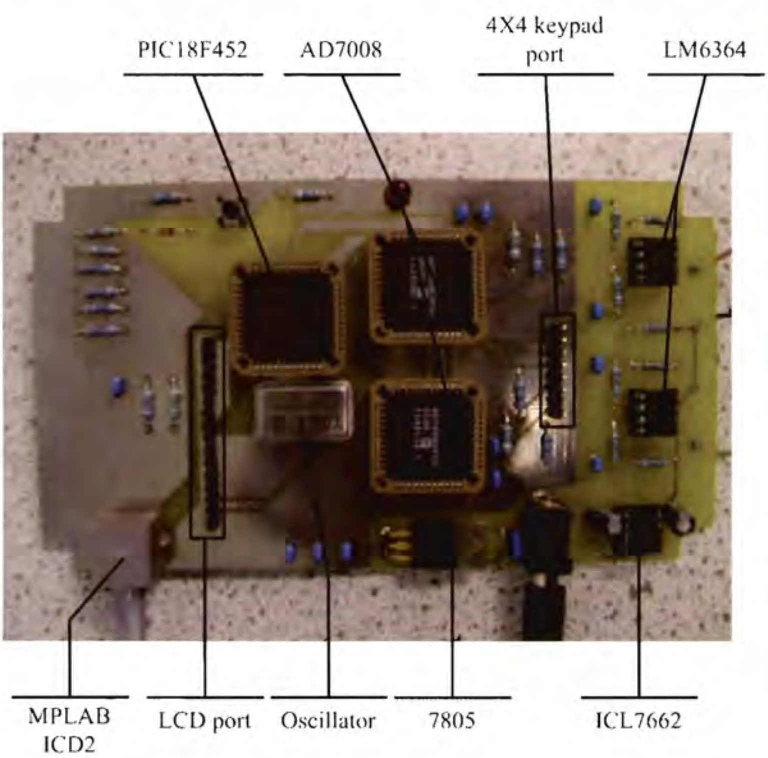


Figure 3: Developed prototype of hand-held dual synchronous DDS signal generator

MPLAB ICD2 has the following features:

- USB (full speed 2Mbit/s) and RS-232 interface to host PC
- Real time background debugging
- Built-in over-voltage/short circuit monitor
- Firmware upgradeable from PC
- Totally enclosed
- Supporting low voltage to 2.0 volts (2.0 to 6.0 range)
- Diagnostic LEDs (Power, Busy, Error)
- Reading/writing memory space and EEDATA areas of target microcontroller
- Programs configuration bits
- Erase of program memory space with verification
- Peripheral freeze-on-halt stops timers at breakpoints.

System design

To develop the hand-held dual synchronous DDS signal generator, hardware has been designed as shown in **Figure 2**.

The control centre of the system is a microcontroller, a high performance RISC CPU, PIC18F452 from Microchip Technology. This PIC microcontroller uses a 40MHz oscillator as the clock input, and it controls two AD7008 DDS chips and the input or output devices. By using a 4x4 keypad as the input device, the user can input desired values frequency, amplitude and phase of the output signals. An LCD is used as the output device, displaying the states of users' input and the information of output signals.

To generate two synchronous sine-wave signals, two AD7008 DDS chips are needed, which are connected to the microcontroller by a control command bus and a data bus. As the maximum value of AD7008 output signal is 1V, which is not big enough for many applications, an amplifier with a gain of 5 is used in this system. Based on the DDS technology theory, a 50MHz oscillator is needed by the two AD7008 DDS chips as the clock input. In order to achieve dual DDS synchronisation, the 50MHz clock oscillator must be placed in the middle of two DDS chips to make its routes to each DDS chip clock input pin equal.

The power supply unit needs to provide the required power for all the components in the system with four different levels of voltages, +5V, +9V, -9V and ground.

During the development, a PCB, a 4x4 keypad, an alphanumeric LCD, a 9V adapter and an MPLAB ICD 2, PIC microcontroller in-circuit debugger/ programmer were used. The software was developed using the MPLAB IDE and MPLAB C18 compiler suite.

User interface

When the system is turned on, the two AD7008 DDS chips are working with default values: frequency 1MHz, phase 0° and amplitude 5V. The LCD display shows the three attributes of both signals with the

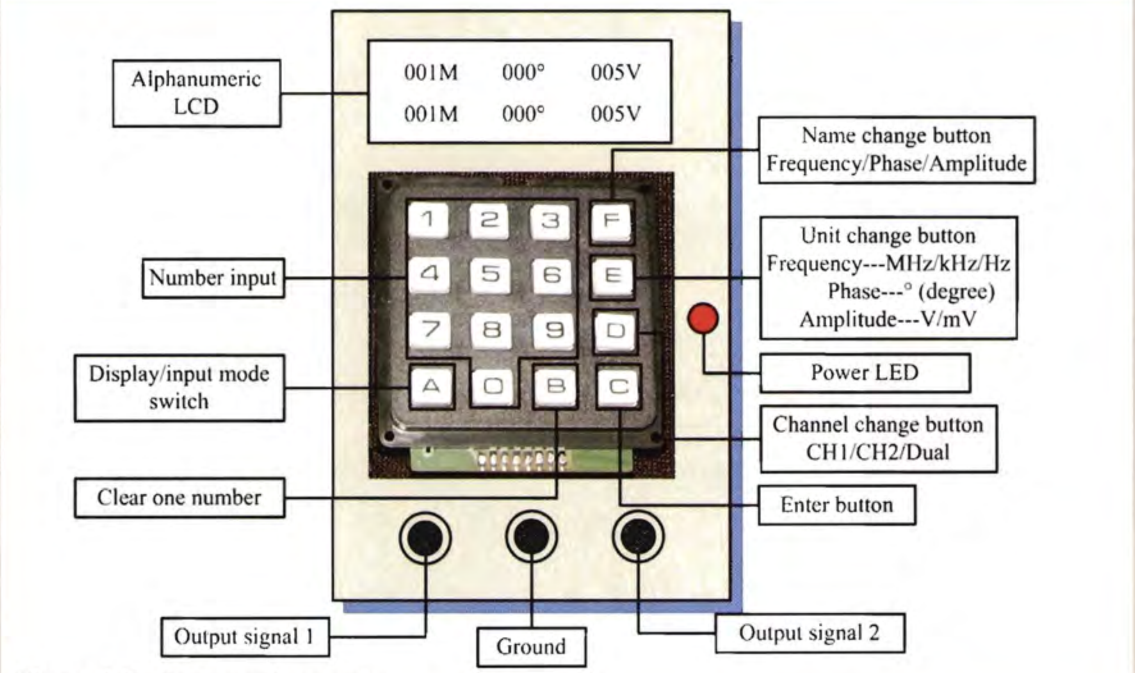


Figure 4: The instrument's operation

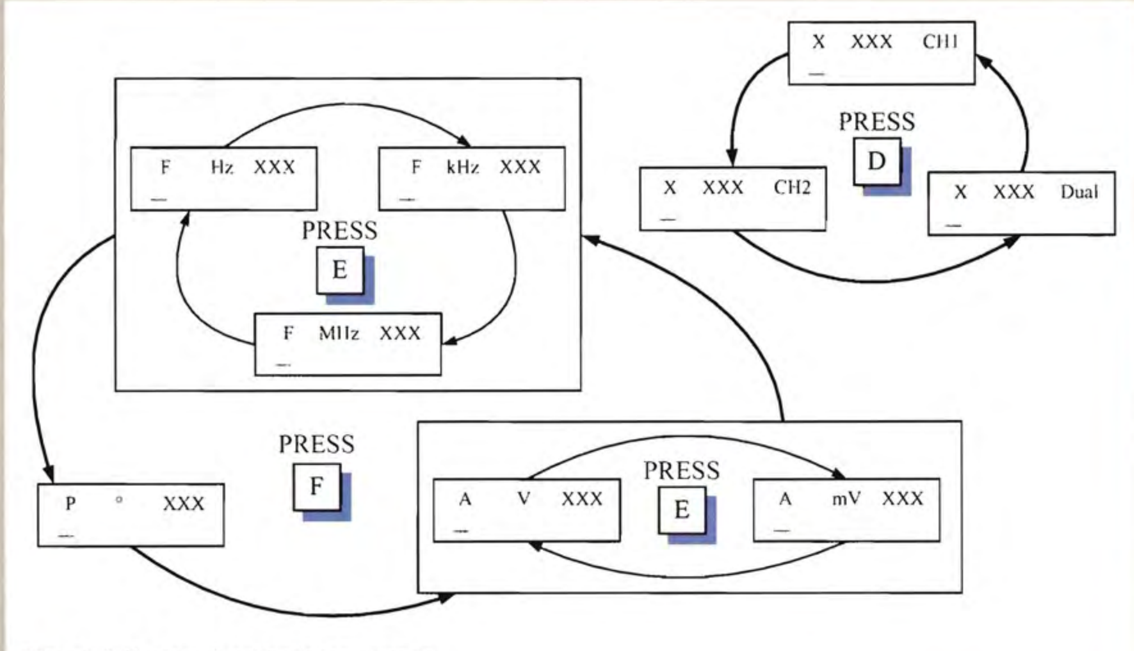


Figure 5: Buttons function in input mode

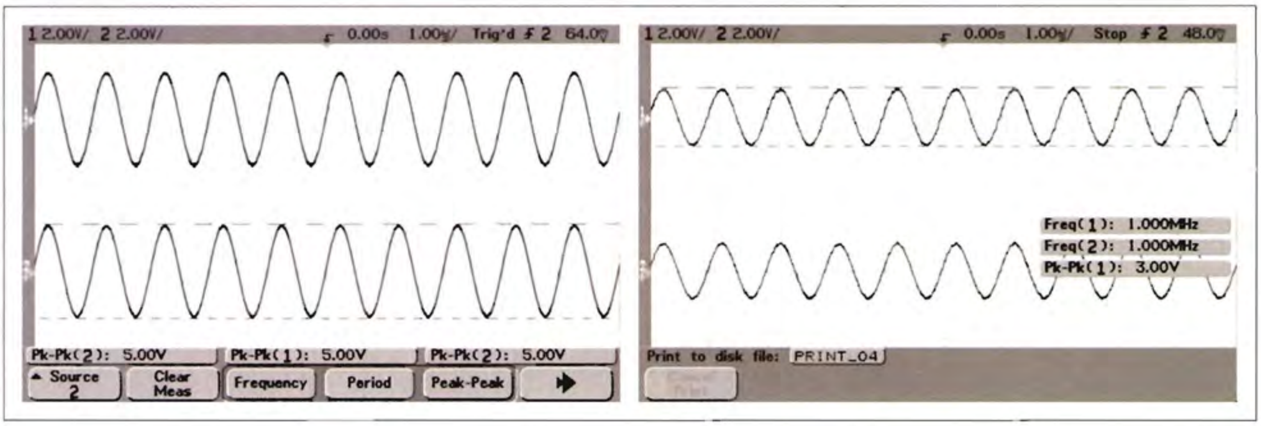


Figure 6: Generated signals with different amplitude, (left) 5V, (right) 3V

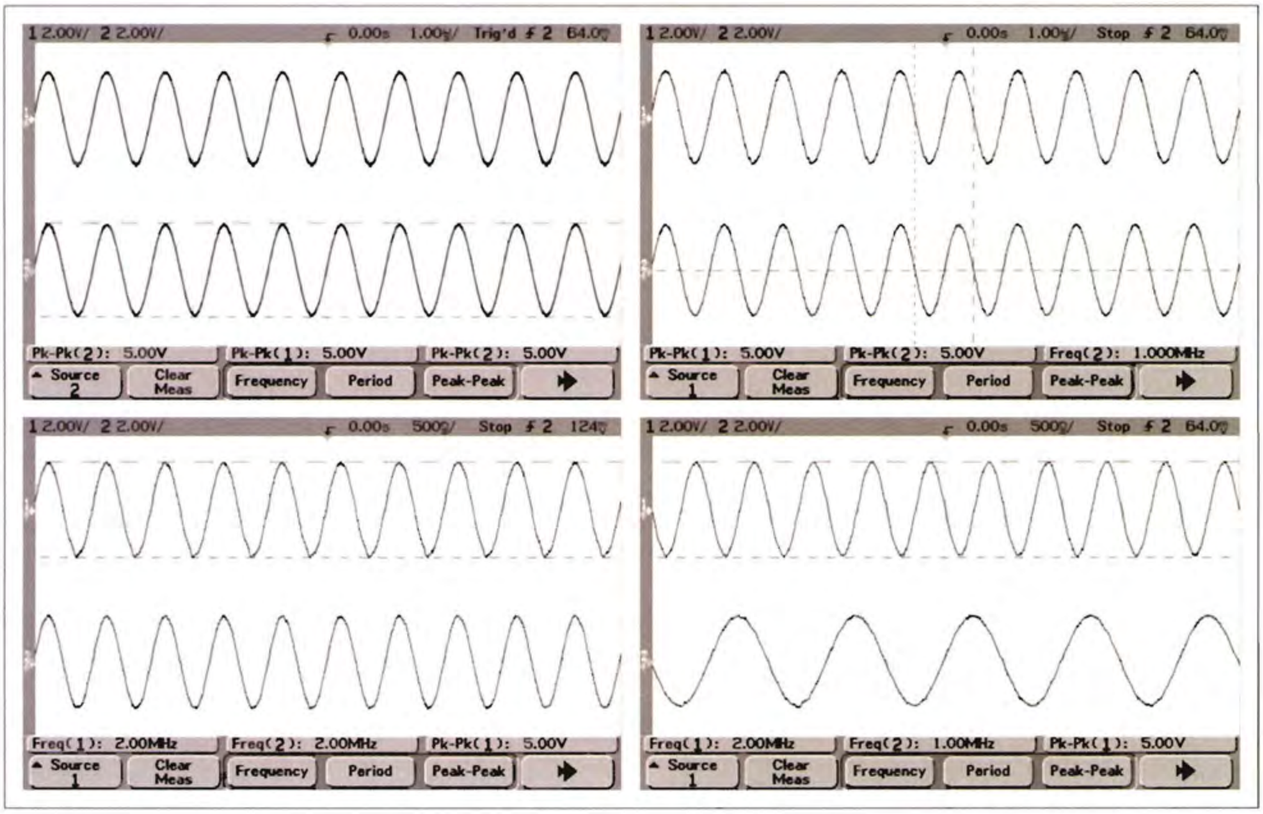


Figure 7: Generated signals with different frequency, (top left) 1MHz as starting frequency, (top right) 1MHz, (bottom left) 2MHz, (bottom right) 1MHz and 2MHz

display mode (see **Figure 4**). Pressing any key of the 4x4 keypad will enter the input mode. In the input mode, users can change the attributes of two output signals using the 4x4 keypad. The "F", "E" and "D" buttons can decide three attributes of the input value: name, unit and channel. The operation is shown in **Figure 5**. If an input value is out of the defined range, frequency 25MHz, phase 360° and amplitude 5V, the LCD displays "Error" and the instrument will ignore input values. Press "A" button to switch between the display mode and the input mode.

Test results

The hand-held dual synchronous DDS signal generator has been tested for different frequency, amplitude and phase. The generated signals were examined using Agilent 54622A oscilloscope and the results are shown in **Figures 5**, **6** and **7**.

The results show that the signals are generated correctly in frequency, amplitude and phase, corresponding to the values entered from the 4x4 keypad. This instrument can now produce fully adjustable signals in terms of frequency, amplitude and phase.

Further developments

This hand-held dual synchronous DDS signal generator has been developed using AD7008 chips, which is an old product from Analog Devices. Some new DDS chips should be used in the future design, such as AD9833 and AD9958. AD9833 chip is a low-power programmable waveform generator capable of producing sine, triangular and square wave outputs. AD9958 chip is a dual channel DDS chip, which is the most suitable for this instrument design.

In addition, amplifiers and filters can be incorporated to increase the amplitude range of the signals and to remove high frequency harmonics. In the near future, this hand-held dual synchronous DDS signal generator may be popular in the market because of their low cost, convenient use and accuracy – they are more accurate than conventional analogue-based signal generators.

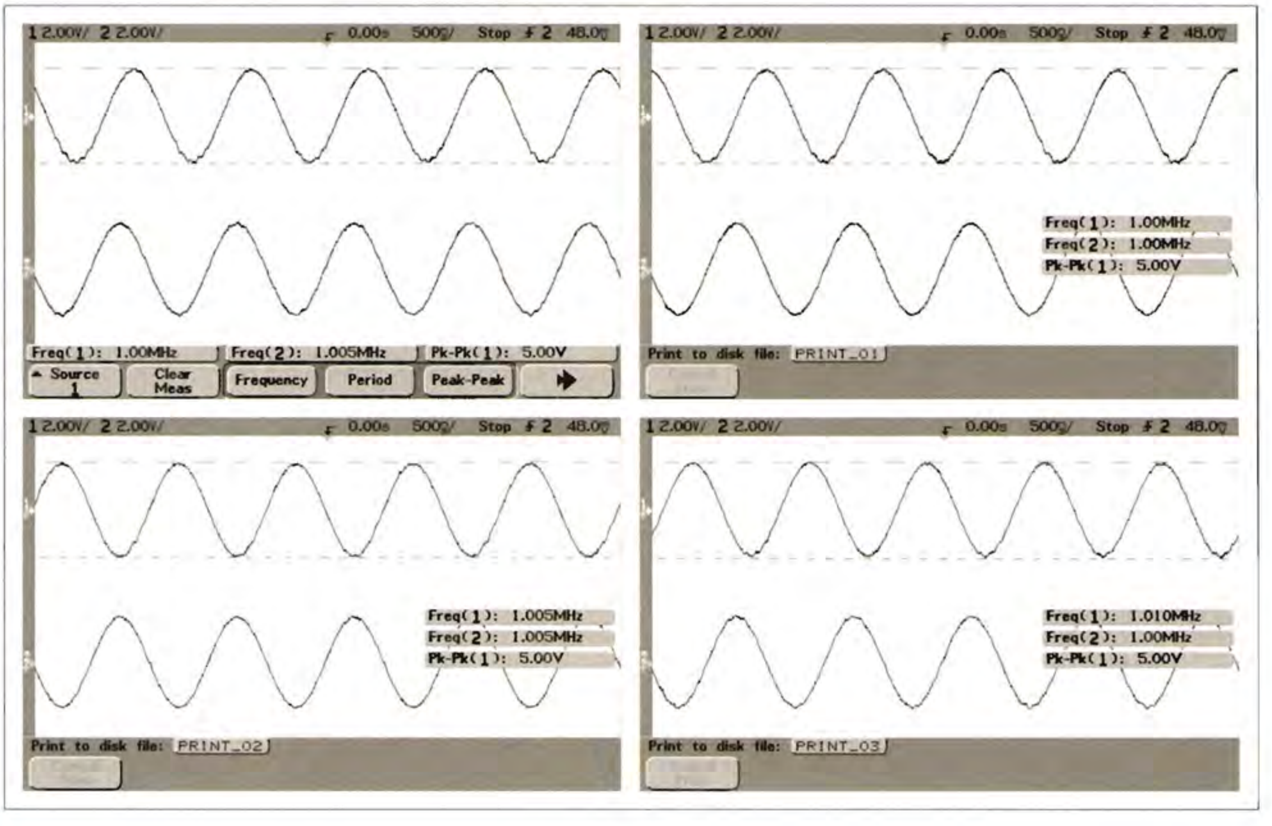


Figure 8: Generated signals with different phase, (top left) 45°, (top right) 90°, (bottom left) 180°, (bottom right) 225°

Resonant Frequency Division

L. Tomawski and **Z. Kukula** from the Institute of Physics at the University of Silesia, Katowice, Poland, here present two yet unpublished resonant networks based on using several RLC and RCL sections in series

Resonant networks can be created by using RLC or RCL sections in succession. In both cases, the last element (C or L) forms a ladder, where the output signal is collected. For the RCL network, the resonant frequency decreases and for the RLC network it increases when the number of connecting sections rises.

The experimental results for the RLC network meet the theoretical results at the frequency range of several hundred kHz. Computer simulations suggest that RLC network can be anticipated as a bandpass amplifier at very high frequencies.

The resonant frequency of the circuit is independent of the series of connecting elements, RLC or RCL. However, adding the second RLC or RCL section in the way shown in **Figure 1** will obtain two different networks with main resonant frequencies shifted in the down and up direction vs frequency.

For the RLC network this shift has constant value vs the number of connecting sections, but for the RCL network this shift decreases when the number of the sections increases.

Interesting behaviour

The RLC network is interesting at the high frequency range, since the obtained resonant frequency can be greater than the resonant frequency of one section of the series resonant circuit. In this way, using a number of the same R, L and C elements creates a bandpass amplifier with a high frequency which is not achievable by using only one section of the series resonant circuit.

For example, let us assume that inductor 10nH and capacitor 10pF are the smallest LC elements we can produce. Using the Kelvin's formula (**Equation 8**) we get the resonant frequency 490MHz, but by using ten 10nH inductors, ten 10pF capacitors and ten 10Ω resistors connected to form the RLC network we can obtain the resonant frequency of 3.37GHz. In addition, at the frequency of 490MHz the gain is 3.2V/V and the quality factor Q=3, but at the frequency of 3.37GHz the gain is 27V/V and Q=21 (from the simulation in the PSPICE program).

The RCL network can find applications in the region of very small frequencies since the use of ten RCL sections is more convenient in practice than using one RCL section with a 64 times greater inductor (provided that ten RCL sections decrease the resonant frequency eight times).

Basic properties

Both analysed resonant networks are shown in Figure 1. For a simple RLC or RCL section, the corresponding resonant curves appear at the same frequency but for two sections the frequencies of the main peaks are shifted either up or down. It is also interesting that the quality factor and the amplification factor also increase with the rise of the number of sections (when the R, L and C elements are assumed constant vs frequency).

The following formula can be derived as the transfer function of the network from two sections:

$$\frac{U_o}{U_i}=\frac{s^2\frac{3LC}{R}+s3C+\frac{1}{R}}{s^4\frac{L^2C^2}{R}+s^3 2LC^2+s^2\left(RC^2+\frac{3LC}{R}\right)+s3C+\frac{1}{R}} \qquad (1)$$

Since all components of the numerator and denominator are admittances, **Equation 1** can be presented as following the "resonant equivalent diagram" shown in **Figure 2**, which is useful in predicting the properties of the network. The complicated construction of the diagram suggests that there isn't a simple formula for either the resonant frequency or the phase angle. Unfortunately, the resonant equivalent diagrams for the network with a higher number of RLC sections are much more complicated.

For the network from Figure 2, the sum of real admittances of all components equals zero and forms the following equation from which the resonant frequencies can be calculated:

$$\omega^4 \frac{L^2C^2}{R^2} - \omega^2 C\left(CR + \frac{3L}{R}\right) + \frac{1}{R} = 0 \tag{2}$$

From **Equation 2**, four angular frequencies can be obtained, but only two of them have positive signs:

$$\omega_1 = \sqrt{\frac{CR^2+3L}{2L^2C} + \frac{R}{2L^2C}\sqrt{C^2R^2+6CL+5\frac{L^2}{R^2}}} \tag{3}$$

$$\omega_2 = \sqrt{\frac{CR^2+3L}{2L^2C} - \frac{R}{2L^2C}\sqrt{C^2R^2+6CL+5\frac{L^2}{R^2}}} \tag{4}$$

Equations 3 and **4** can be simplified when resistance R and capacitance C are suitably small and inductance L is suitably high. Both these conditions can be described as follows:

$$\omega CR \ll Q \tag{5}$$

where Q denotes the quality factor of inductors.

When inequality (**Equation 5**) is fulfilled, Equations 3 and 4 can be rewritten in the following forms:

$$f_1 = \frac{1}{2\pi}\sqrt{\frac{3+\sqrt{5}}{2LC}} = \frac{0.2577}{\sqrt{LC}} \tag{6}$$

$$f_2 = \frac{1}{2\pi}\sqrt{\frac{3-\sqrt{5}}{2LC}} = \frac{0.0984}{\sqrt{LC}} \tag{7}$$

Let us assume that $f_1 = f_{2H}$ and $f_2 = f_{2L}$, since two RLC sections are taken into account, and f_{2H} is the high frequency, whereas f_{2L} is the low frequency. Moreover, the resonant frequency for one RLC section, calculated from Kelvin's formula is:

$$f_0 = \frac{1}{2\pi\sqrt{LC}} = \frac{0.1592}{\sqrt{LC}} \tag{8}$$

Hence, for n RLC sections we have three characteristic frequencies: f_0, f_{nH} and f_{nL} and between them the following relations can be found:

$$f_{nH} = \Delta f(n-1) + f_0 \tag{9}$$

where:

$$\Delta f = f_{2H} - f_0 = \frac{0.0985}{\sqrt{LC}} \tag{10}$$

These very simple **Equations** (**8, 9, 10**) make it possible to calculate the main resonant frequency for arbitrary n (for nRLC network), without the necessity of deriving complicated Equations like 1 and 2.

For RCL network constructed from two RCL sections, the following transfer function equation exists:

$$\frac{U_o}{U_i} = \frac{s^4\frac{L^2C^2}{R} + s^3 3LC^2 + s^2\frac{3LC}{R}}{s^4\frac{L^2C^2}{R} + s^3 3LC^2 + s^2\left(RC^2 + \frac{3LC}{R}\right) + s2C + \frac{1}{R}} \tag{11}$$

The "resonant equivalent diagram" for this network is shown in **Figure 3**. Since all real components are the same as for RLC network from Figure 2, the characteristic equation and formulae for resonant frequencies are the same as in 2, 3 and 4. However, imaginary elements and the way of connecting elements in both diagrams are different and, hence, the quality factors and amplitudes of the peaks are different. **Equations 6-8** are still relevant, but the peak at f_1 has a high amplitude and at f_2 a low amplitude. When the number of RCL sections rises, the main peak frequency decreases slowly, but the value of the frequency shift is not constant and the Equations such as 9 and 10 do not apply.

Simulated and measured results

Equations 6-10 give results in a good accordance with computer simulations and measurements. In **Figure 4**, the continuous lines show the computer simulation in PSPICE program for one and three RLC sections, and each point relates to a measurement result. Measurements were carried out when two operational followers were used at the input and output terminals.

Resistance R consisted of two parts. One of them was the series resistance of coil measured at high frequency f_{2H} and the second was an additive resistor supplementing the total resistance of R value (40Ω). The loss resistance of the capacitors was not taken into account, however, the quality factor of the used capacitors should be high. In the experiment of Figure 4 this quality factor has the value of 300 at 350kHz. Frequency calculated from Equation 9 is about 340kHz, but from PSPICE simulation is 339.1kHz.

Advantages of using RLC or RCL networks

There are at least two distinct advantages of using the RLC and RCL networks and they are:

1. Matching the resonant frequency is easy

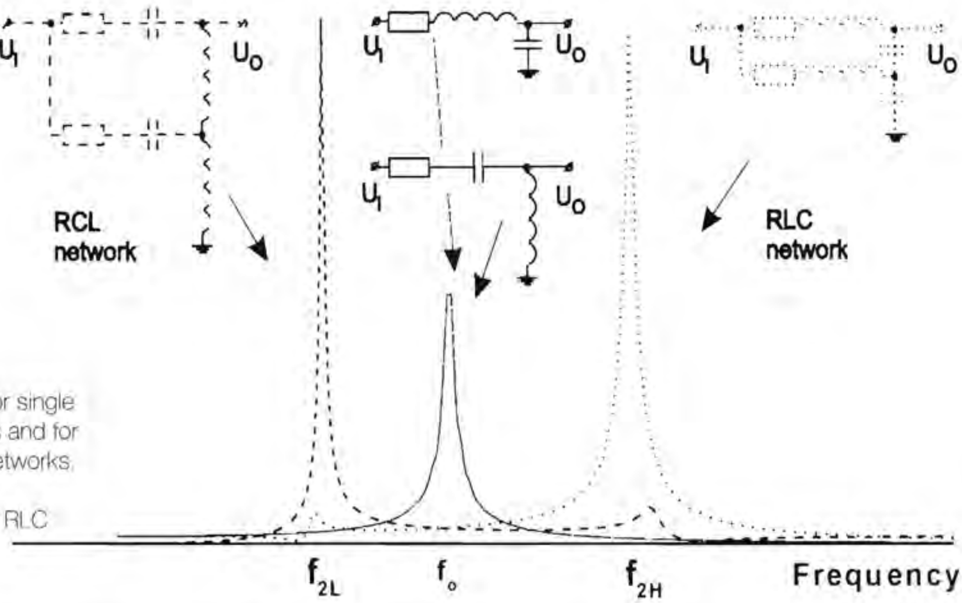


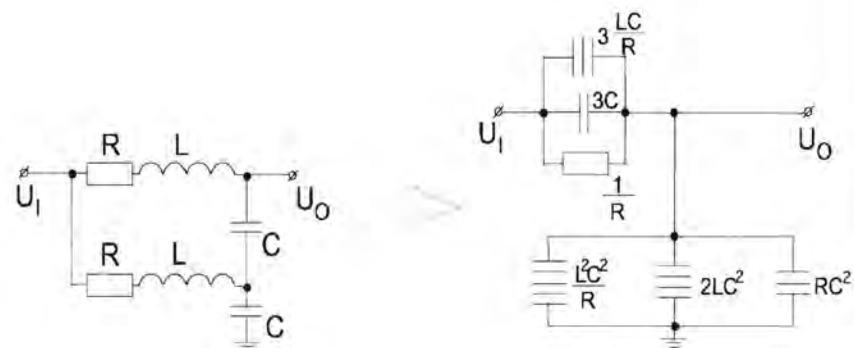
Figure 1: Resonant peaks for single RLC or RCL resonant circuits and for two-section RCL and RLC networks. The f_{2H} and f_{2L} denote the characteristic frequencies for RLC network

Figure 2: Two- section RLC network and its "resonant equivalent diagram"

denotes FDNC-Frequency Dependent Negative Conductance with $Y(s) = S^2D$ where D is constant As^2/V

denotes FDNCap-Frequency Dependent Negative Capacitance with $Y(s) = S^3F$ where F is constant As^3/V

denotes FDPC-Frequency Dependent Positive Conductance with $Y(s) = S^4M$ where M is constant As^4/V



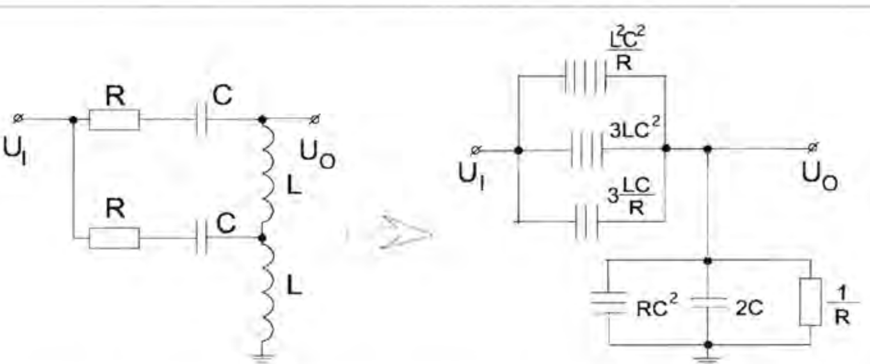


Figure 4: Simulated and measured resonant curves for single RLC resonant circuit and three-section RLC network

The resonant frequency in RLC network is a function of the number of used elements. By changing one of them, we can precisely match this frequency to the appropriate value. For example, if the number of sections is 10 then the change of the inductance of one of the coils by about 50% affects the change of the resonant frequency from about 10% to about 2%, depending on where the changed inductor is located.

2. Setting of the bandwidth and the shape of resonant curve is possible

Assuming that R, L and C elements that can take on different values, there are some strategies of the

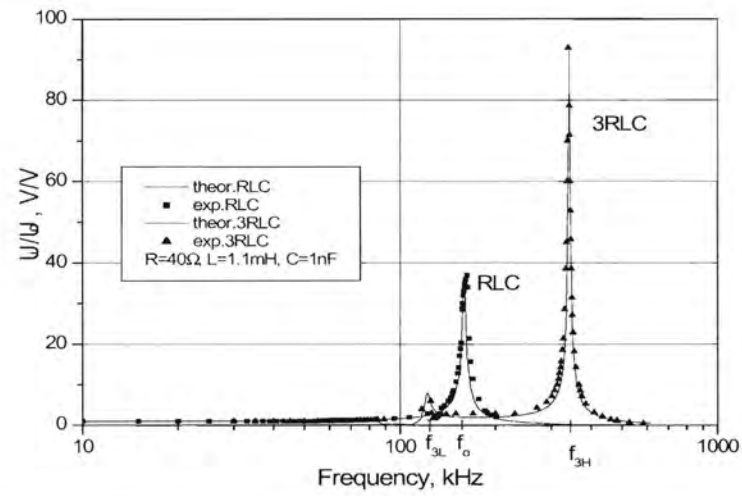


Figure 3: Two-section RCL network and its "resonant equivalent diagram"

matching values of these elements, which makes it possible to obtain the resonant curve with a suitable bandwidth and shape.

New possibilities

RLC and RCL networks give new possibilities of selective amplification of signals keeping the good noise and sensitivity properties of the classical resonant circuits.

In the frequency region of several hundred kHz, the results for both RLC and RCL networks obtained from theory, measurements and computer simulations are in good agreement.

Computer simulations suggest that the resonant frequency in RLC network of about several GHz could be obtained for relative big values of L and C.

It is probable that RLC network will become a useful solution for the very low frequency region.

It is of great importance that with the increase of the number of the RLC or RCL sections, the quality factor and the amplitude of the main resonant peak also rises. Probably both, the RLC and RCL network, can also be constructed with ferroelectric resonators.

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E&OE

What's all the fuss about?

RoHS (the Restriction of the use of certain Hazardous Substances) and **WEEE** (Waste Electrical and Electronic Equipment) is the equivalent of Y2K for the electronics industry. The upcoming EU environmental directives are the most significant developments in electronics legislation to happen in many years and will completely revolutionise the way electrical and electronic products are designed, sold, recovered and recycled. Worryingly, many design engineers are still not fully aware that the upcoming legislation will affect them. For those who are, many questions remain unanswered. Complicated exemption rules, uncertainty about how the directives will be enforced, obsolescence and component availability has left engineers unsure of what they need to do and when. The clock is ticking. With July looming, there's no time to lose in the transition to RoHS. If compliant components aren't already part of the design cycle it could well be too late.

Q: We have a warehouse in Nottingham that we import to from India. The stock is non-compliant but already on our warehouse shelves. Can this stock be sold after 1st July?

A: Yes, as the stock is already in the warehouse it is considered to be on the market. The legislation states that non-compliant components can be sold after the deadline for the purpose of repair or upgrade of equipment that has been put on the market before 1st July 2006.

Q: What about nuts and bolts?

A: The status of nuts and bolts is the same as any other component; they need to comply with RoHS if the equipment that they are part of falls within the directive. However, if these are nuts and bolts that are sold for no specific application and are used, for example, to attach equipment to walls, floors, etc., then these in our opinion are not part of the product and would be outside the scope of WEEE and RoHS.

Q: Is cable included in the RoHS directive?

A: Although the DTI disagrees, the European Commission (EC) states that cable does fall into the directive. The UK's RoHS policing body, National Weights and Measures, says that where there are discrepancies, EC guidelines should be followed.

Q: Are there any rules about donating WEEE, such as old computers, to charities outside of the EU?

A: Firstly, products are only WEEE (and therefore waste), if they are not reusable or not intended to be used again. Secondly, products sent outside of the EU do not need to comply with the RoHS and WEEE legislations, as they are only applicable when traded within the EU. It's worth mentioning that the spirit of both pieces of legislation encourages re-use and recycling wherever possible.

Q: As a UK manufacturer selling products in the UK, I am likely to have non-compliant stock which I won't be able to place on the market before the deadline. Can I still sell this? If not, what can I do with the stock?

A: You will only be able to sell stock placed on the market before the deadline. So, you have two main options for products left in stock. Firstly, you can consider selling the stock to industry sectors that are RoHS exempt, i.e. military or MRO. Secondly, you could consider disposing of them in line with the WEEE Directive.

Q: Would a car radio be within the scope of the RoHS directive?

A: This is an example of the ruling in respect of equipment that is part of another type of (larger) equipment not covered by the RoHS directive. A car does not fall within RoHS, therefore, neither do car radios.

Q: I manufacture test equipment, do I have to worry about RoHS?

A: Not at the moment as test equipment is category 9 and does not fall within the scope of RoHS. A review is currently underway and it is likely to result in test equipment falling within RoHS, but it is not expected until around 2010. However, it is within the scope of the WEEE Directive and should be recycled at the end of its life.

Q: If I manufacture and supply a piece of kit that is built into equipment that has someone else's brand logo on, who is responsible for the recycling at the end of life?

A: The responsibility lies with the brand owner.

Q: What responsibility does a US manufacturer have regarding the WEEE laws?

A: There is currently a lot of discussion within EU states about whether non-EU manufacturers can register. This affects US exporters who supply directly to business customers. The US manufacturer may wish to be responsible for WEEE for commercial reasons as otherwise the business user is responsible. This is not currently possible in most EU states but some, including Portugal, are considering changing their approach. Currently, US manufacturers can register in a few countries including Germany, Ireland and Hungary.

Gary Nevison is chairman of the AFDEC RoHS team, board director at Electronics Yorkshire and head of product market strategy at Farnell InOne. As such he is our industry expert who will try and answer any questions that you might have relating to the issues of RoHS and WEEE. Your questions will be published together with Gary's answers in the following issues of Electronics World. Please email your questions to EWeditor@nexusmedia.com, marking them as RoHS or WEEE.

evolution of POWER OVER ETHERNET

CLAY STANFORD, DESIGN MANAGER, POWER OVER ETHERNET PRODUCTS, AND **TODD NELSON**, PRODUCT MARKETING MANAGER, MIXED SIGNAL PRODUCTS, AT LINEAR TECHNOLOGY CORPORATION GIVE SEVERAL DESIGN TIPS AS TO HOW TO INCREASE THE POWER LEVEL DELIVERED TO A POWERED DEVICE OVER THE ETHERNET

The IEEE 802.3af standard for Power over Ethernet (PoE) introduced a new facet to Ethernet networking, delivering DC power in tandem with 10/100/1000Mbps data. PoE brought with it a unique set of problems and new ways of thinking that were unfamiliar to many engineers with experience designing Ethernet equipment. PoE is now commonly used for VoIP phones, wireless access points and security cameras. As PoE evolves, there is a need for enhancements to the standard to enable emerging applications.

By way of review, the PoE link allows a Powered Device (PD) to draw up to 12.95W from the Power Sourcing Equipment (PSE). The PoE link or port is controlled by the PSE, which identifies PDs via detection and classification before powering and monitoring the port (ICUT, ILIM and disconnect). Much of the burden of PoE rests on the PSE, which must perform detection and disconnect flawlessly to avoid damaging legacy devices. If the PSE does not adequately perform classification, power delivery and monitoring, intermittent failures and instabilities may result. The PSE cannot control everything; when it applies power, it trusts the PD to follow the standard, turn on without oscillating and avoid drawing more power than requested. Because both types of devices must cooperate, PD and PSE designers should consider issues from the perspective of both devices.

Higher power for emerging applications

Power of 13W is adequate for basic IP phones, but motorised cameras, multi-radio access points and devices with large colour screens are seriously constrained. The IEEE is currently working a higher power standard, dubbed PoE+ (officially IEEE 802.3at) that

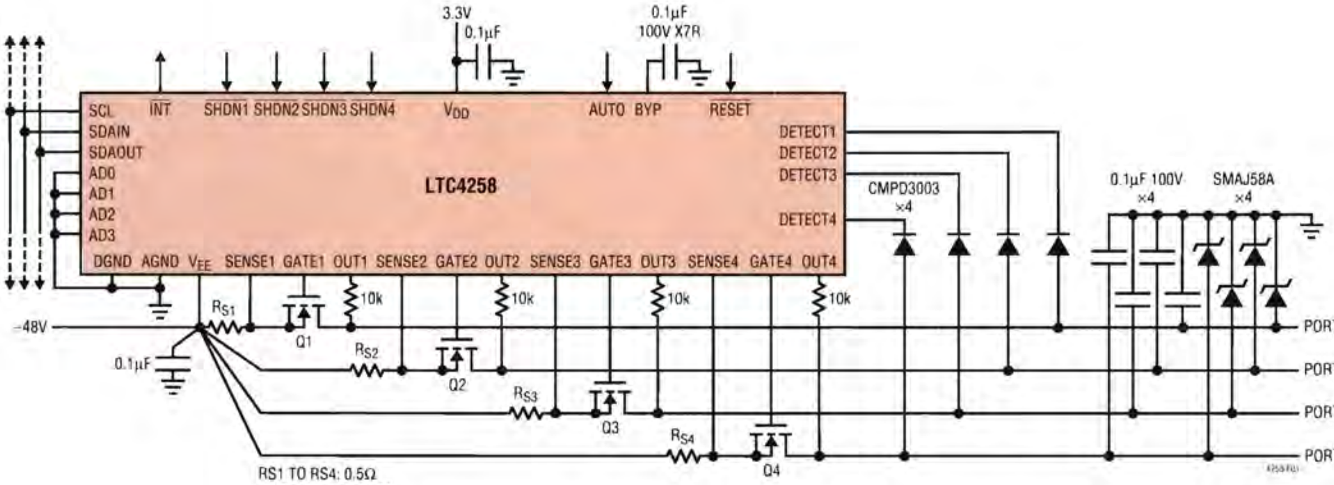

Figure 1a: Basic 802.3af-compliant PSE circuit using LTC4258

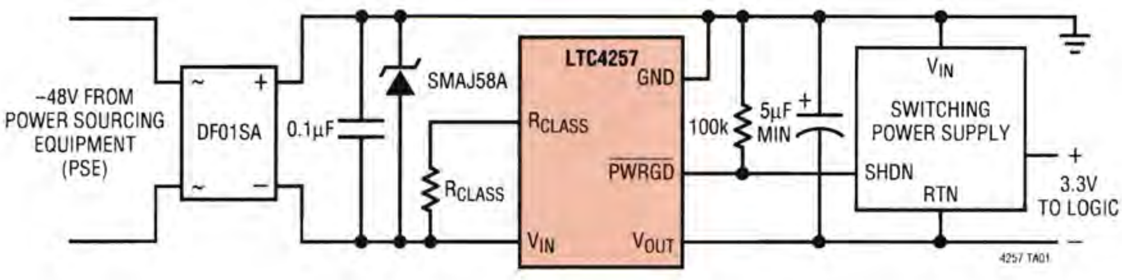

Figure 1b: Basic 802.3af-compliant PD circuit using LTC4257

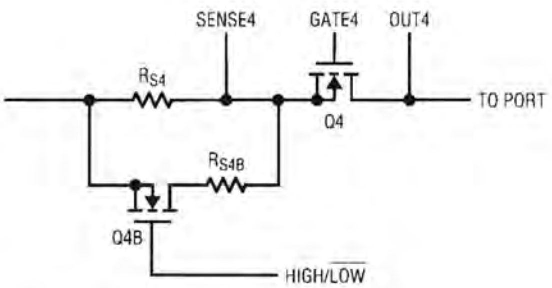

Figure 2a: Dual current high power/802.3af PSE

will coexist with 802.3af devices available today. The ultimate power levels defined by the new standard have not been established, but as of today, it is likely we will see 30W 2-pair systems and 60W 4-pair systems.

The IEEE 802.3at committee has taken on a daunting task to define a world standard that will define a safe, higher-power standard that is backward compatible and interoperable with currently deployed 802.3af equipment. Because of the complexities of writing this specification, we are not likely to see a final specification for $1^1/_2$ to 2 years from now.

Although typical CAT-5 cabling includes four twisted pairs, the 802.3af standard only allows two pairs to carry current at any given time. One option is to allow additional current down the third and fourth pairs, doubling the available power. A second option is to raise the current limit, allowing more power down the same two pairs. Each of these techniques has appeared in proprietary PoE systems. However, each has drawbacks, complicating the choice between them.

Implementing pre-standard high-power PSEs

In the interim, some applications require high power and cannot wait for the new standard. There are several ways to do this. The circuits shown in **Figure 1a** and **1b** are build on the basic 802.3af-complaint PSE circuit using the LTC4258 and the basic PD circuit using the LTC4257, respectively. The LTC4259 can be substituted in the PSE circuit if the application requires AC disconnect; the LTC4267 can be substituted in the PD circuit if the application requires an integrated switching regulator.

The following circuit examples demonstrate several ways that high power operation can be achieved. Note that in some of the following PSE circuits, channel 4 is used to illustrate the circuit changes, but any channel can be used.

▷ Two-pair, high current

The power level can be increased in the PSE simply by changing the value of the sense resistor (R_{S1} – R_{S4} in **Figure 2a**). R_{Sn} is set to 0.5Ω for 802.3af compliance (375mA I_{CUT}, 425mA I_{LIM}). Cutting the value of R_{Sn} to 0.25Ω, for example, doubles all the current limits (750mA I_{CUT}, 850mA I_{LIM}). This doubles the power to the PD when a short cable is used; increased losses in longer cables limit the power delivered to the PD to somewhat less than 2x.

Note that the LTC4258 also uses the sense resistor to detect DC disconnect. Cutting the resistor value to 0.25Ω will double the DC disconnect threshold, rendering it technically non-compliant. Other 802.3af parameters are not affected: detection and classification will remain compliant, and the AC disconnect threshold (LTC4259 only) is not affected by the sense resistor change. Because the raised DC threshold runs a small risk of disconnecting a very low power 802.3af PD, AC disconnect is recommended for interoperability with 802.3af PDs.

Two other components (per channel) need to be modified to handle the extra current. The Mosfet Q4 will typically need to be replaced with a larger device to tolerate the higher power during current limit. In this application, IRF530-type devices in D^2PAK packaging are adequate. The PoE data magnetics also need to be specified to carry higher current. Several magnetics vendors have newly released parts with adequate current capability.

By adding two new components, we can switch between 802.3af-compliant operation and high power. In this case, R_{S4} is set to the original 0.5Ω value and R_{S4B} is

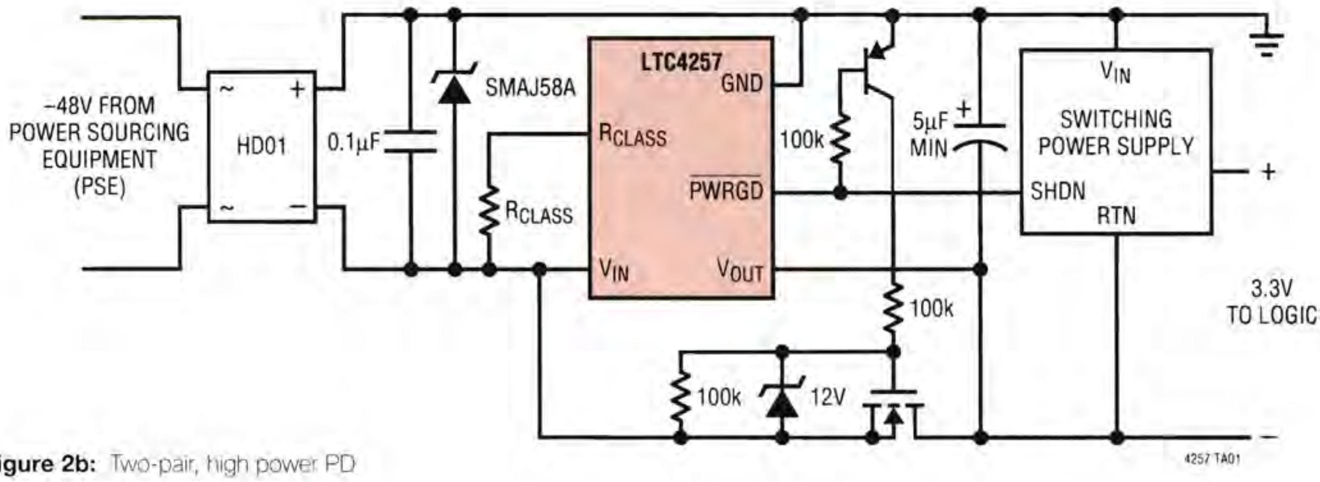

Figure 2b: Two-pair, high power PD

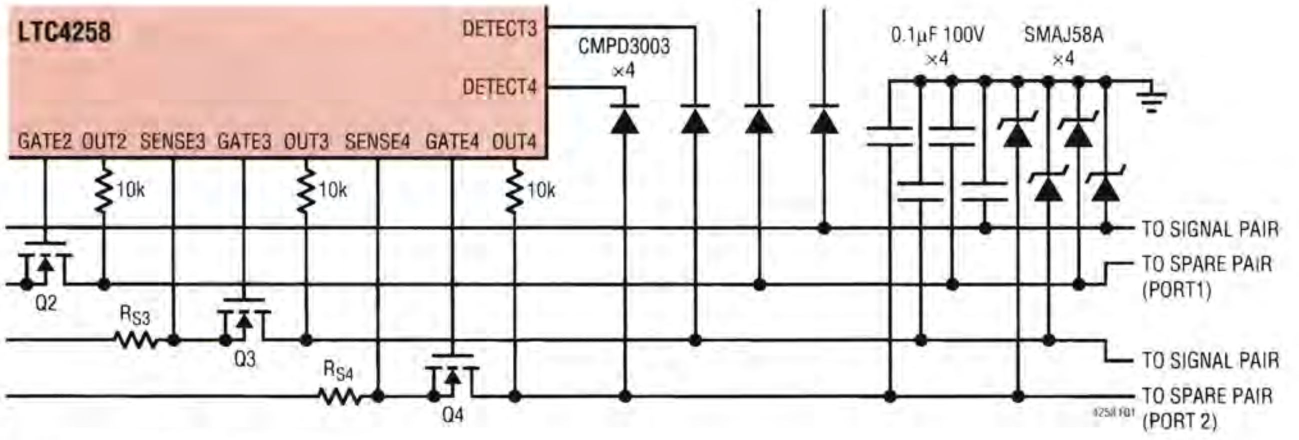

Figure 3a: Four-pair 802.3af power

chosen so that R_{S4} II R_{S4B} gives the desired higher current level. Setting R_{S4B} to 0.5Ω (the same value as R_{S4}) sets the high power mode to twice the power level of 802.3af.

When Q4B is off, the port operates in 802.3af-compliant mode. Turning on Q4B switches the port to high current mode. This transition can be made at any time: before detection/classification; after detection/classification, but before port power-up; or after power is applied. Note that Q4B can be a low-voltage Mosfet, since only the drain of Q4 sees the high port voltage. Q4B should be selected for very low on-resistance to prevent inaccuracies in the higher current limit. The IRLML2502 is an example of a suitable device in a SOT-23 package.

The PD modification (**Figure 2b**) is slightly more complicated since the internal Mosfet is pre-configured for 375mA current limit operation. However, adding an external pass device controlled by the PWRGD pin allows high current operation while maintaining full 802.3af detection and classification signatures and inrush current limiting.

▷ Four-pair, low current

An alternate technique to increase the power delivered to the PD is to power all four pairs in the CAT-5 cable. **Figure 3a** shows a four-pair PSE circuit with standard 802.3af power available on each pair. No changes are required to the sense resistor values.

The bigger change is to the four-pair PD circuit (**Figure 3b**). Two LTC4257 devices are now required and the power supply circuitry must be smart enough to limit the current draw from each channel to stay under the 802.3af limits. It can do this by balancing the current drawn from each pair-set, or by drawing power from one pair set until it approaches (but does not exceed) the ICUT limit, then beginning to draw from the other set. This circuitry can be fairly complex and will vary from design to design.

The four-pair technique has the advantage of using all the conductors in the cable, minimising the total cable resistance and the resulting power lost with long cables. Using standard current levels also comes closest to full 802.3af compliance of any of the high power techniques, since either the signal pairs or the spare pairs used alone will be fully compliant. The primary drawbacks are complexity and expense. The PSE requires two channels of the controller chip per port, halving the effective port density, while the PD requires two controller channels and additional current balancing circuitry to ensure that the current drawn from either pair-set does not exceed the maximum level. In addition, four-pair techniques will not work if only the signal pairs have continuity, as in some CAT-3 building installations.

Because of the cost and complexity penalties of the four pair scheme, two-pair high current is the preferred technique at medium power levels. Four-pair systems are most applicable when the PD power rises above the 35W level.

▷ Four-pair, high current

Combining high current circuitry with four-pair hook-up allows more power down the cable than any other technique. Four-pair high current allows as much as 50W to be delivered to the PD over a 100m CAT-5 cable, more if the cable length is kept short. Although this scheme includes the drawbacks of all of the previous schemes, it is the highest power option available.

Beyond 50W, long cables rapidly approach an 'impedance matched' situation where the cable dissipates more power than it delivers to the PD. If the length of the cable is kept short, the current level can be further increased, ultimately limited by the RJ45 connector, offset current in the magnetics and the temperature rise in the CAT-5 cable. Extremely high power (>50W) should only be used in systems where the entire solution is specified by the same supplier.

Classification: when to apply high power

Notably absent from the above circuits is a method to determine when it is appropriate to apply high power to the line. All of the techniques will successfully power standard 802.3af PDs under normal conditions. The dual-threshold circuits need to have some information from the PD to know when to switch thresholds, and the four-pair schemes need to know when it is appropriate to switch on the second set of conductors. The IEEE 802.3at committee is working to address these issues, but no schemes have yet been finalised. In the interim, ad-hoc solutions are needed to identify high power PDs.

IEEE 802.3af defines an unused class (Class 4) that looks tailor-made for high power, and both the LTC4258/59 PSE chips and the LTC4257/67 PD chips support Class 4. Unfortunately, a Class 4 PD will be powered with Class 3 current limits if it is plugged into a standard 802.3af PSE, which may cause it to cycle on and off repeatedly if it attempts to draw higher power. Class 4 can be used as a "warning" that a high power PD is connected, but it is advisable to have an additional handshake before higher power is delivered. Ideally, a high power PD should receive some sort of signal from a high-power PSE, acknowledging it is acceptable to operate in a high power mode. If no handshake is received, the PD should give some sort of indication to the user that it is plugged into the wrong kind of PSE.

Recommendations

The best technique to use for pre-standard high power depends on the application. At power levels up to 30W, the two-pair high current techniques provide the lowest cost and complexity, and full 802.3af compliance by using the dual-threshold circuit. If maximum power is required (50W or more), the four-pair high current circuit is the best choice.

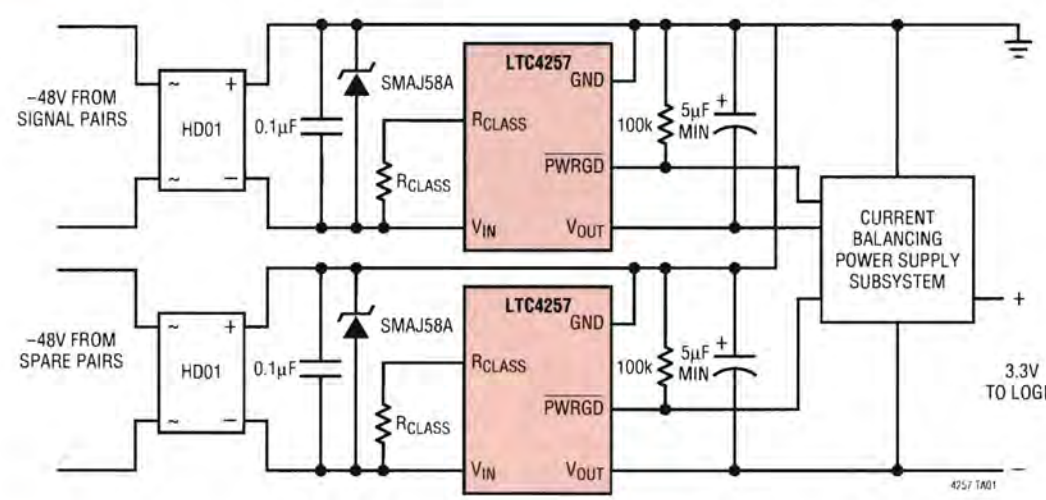

Figure 3b: Four-pair low-current PD

Enabling the virtual office *ON TRAINS*

ROBIN GEORGE – APPLICATION ENGINEER AT HUBER+SUHNER HERE DISCUSSES THE RAIL ANTENNA TECHNOLOGIES CURRENTLY AVAILABLE, AS COMMUNICATIONS SHOULD NOT STOP ONCE YOU BOARD A TRAIN

In the last few years, wireless technology has become an essential part of our modern lifestyle. From various locations workers are able to access emails, the corporate virtual private network (VPN) and the Internet by simply using a wireless-enabled laptop. But the demand for such access now includes onboard trains.

This is encouraging train operators across the developed world to provide useful, value-added services, which may also bring that extra revenue stream. Train radio is paving the way to new applications. Over the next few years, GSM-R will supersede the old analogue train control radio in many European countries. New communication technologies such as GSM-GPRS, Wi-Fi and WiMax are driving the demand for new trainborne services, with real-time passenger information systems, online video surveillance and train monitoring during operation to be implemented soon.

So, there's a growing need for broadband antennas that can enable broadband wireless connectivity for trains and meet the demands of multi-band systems.

Public mobile communications

Being almost a perfect Faraday's cage, the railway carriages will block all radio signals from the outside world and vice versa. There is little chance for any mobile communications operator to provide service inside a train without the use of additional RF equipment i.e. radio repeaters. This is especially true for modern trains using metallic windows for the purpose of climatic comfort.

The configuration shown is one of the first around and it is Huber+Suhner's Sencity Rail broadband antenna that supports six technologies in one convenient unit – GSM-R, GSM-P, UMTS, WLAN, WiMAX and GPS. It comprises a set of three repeaters, one for GSM 900, one for GSM1800 and finally one for UMTS. The repeaters and the combiner network are hosted within special equipment rooms inside the carriages. The new antenna connects to the output of the repeater combiner network, which in this case is a triplexer that multiplexes GSM900, GSM1800 and UMTS. The radio signals that are picked up from outside the carriage by the antenna are re-amplified within the repeaters and transmitted to either a leaky feeder or directional antennas to provide seamless coverage inside the carriage. The signals received or vice versa, from mobile phones, PDAs or notebooks equipped with GSM-GPRS/EDGE/UMTS cards inside the carriage, are transmitted to the antenna which interfaces to the mobile operator's networks.

Depending on the nature of the train, different configurations of antennas and repeaters may be required. High-speed trains and commuter trains are usually built as a fixed train set, therefore, only one set of RF equipment is required. In this case, RF connectivity between carriages utilises corrugated cables which use special cable protection mechanisms. Other trains may comprise of individually coupled units requiring a repeater system and an external pick-up antenna for each carriage.

Wi-Fi on trains

In addition to public mobile communication, Wi-Fi service for passengers will enable Internet and e-mail access at reasonable data rates during the journey. In the initial stages, data interchange between the train and "the outside" world will take place in station areas; in the future, it is planned to offer continuous WLAN coverage along tracks, based either on satellite/DVB-T communication or a network deployment along the track.

Equipment configuration will be similar to that shown in **Figure 1**, except that there is an additional communication server which interfaces between the in-train WLAN network and the antenna.

Wi-Fi signals picked up in train stations or – at a later stage along the track – are routed to the mobile communication server inside the carriage. For the purpose of continuous connectivity along the track a GSM GPRS/EDGE modem may be fitted to the communication server, making use of the existing cellular network coverage. Mobile communication and

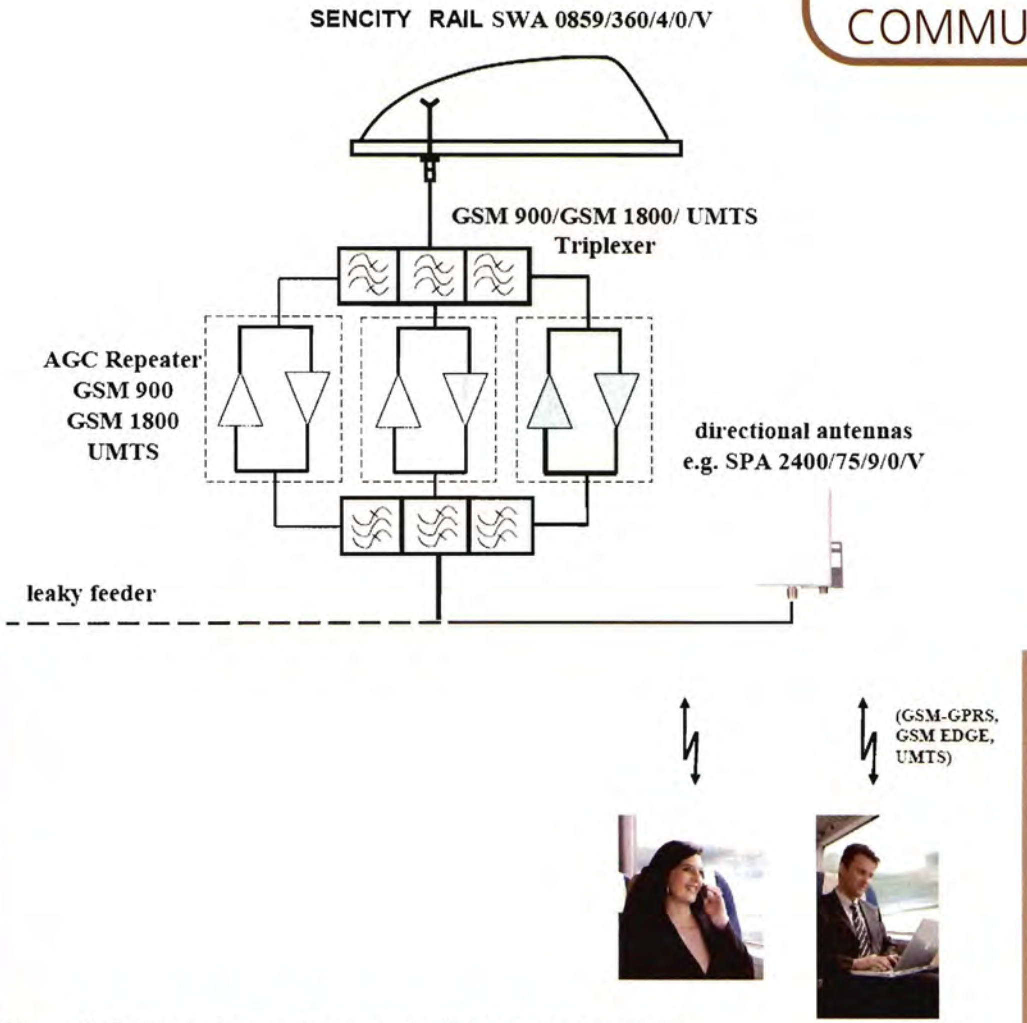

Figure 1: Typical on-train multi-operator/multi-band repeater system

WLAN signals are diplexed to/from the antenna using a WLAN/GSM and UMTS cross-band coupler.

The communication server forms the central unit which connects to a set of access points through Cat-5 type Ethernet cables. The access points provide WLAN coverage inside the carriages, with each access point terminated with either one or two antennas. Propagation measurements inside carriages indicate that diversity does not give additional benefit, therefore, the dual antenna configuration can be used to cover different areas of the train.

Connectivity between carriages is achieved through WLAN bridges using either one of the 802.11b/g (2.4GHz) or 802.11a (5.6GHz) channels. Antennas used for this purpose are the same directional antennas as used for in-carriage coverage, e.g. SPA 2400/75/9/0/V or SPA 5600/60/10/0/V.

Wireless train monitoring

With cellular networks currently evolving from purely voice-based services to increased-data applications, Wi-Fi systems set up in station areas, train monitoring during operation becomes a real world application. This provides the possibility to check the operating conditions of engines, boogies, air-conditioning, power units, etc, while the train is out on the track.

Passenger information systems can be updated with brand new information about connecting trains, delays, expected track number for arrival, current location, etc, making a journey more comfortable. All this is possible with the support of GPS, which provides timing and location information.

To perform train diagnosis or provide real-time

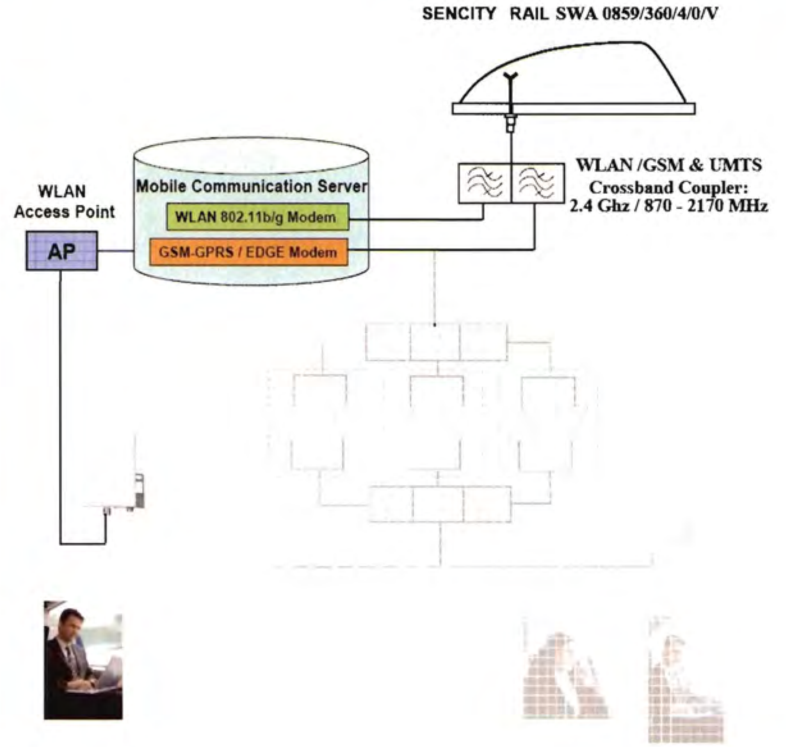

Figure 2: Trainborne Wi-Fi equipment

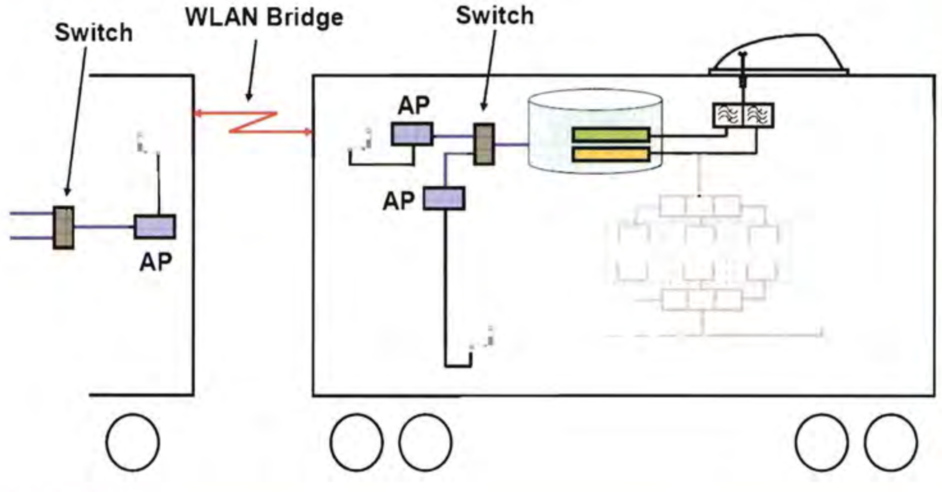

Figure 3: WLAN inter-carriage bridge

passenger information service, public mobile networks and WLAN networks will be used, although the equipment will look different to public mobile and LAN applications. The principle configuration is shown in **Figure 4**.

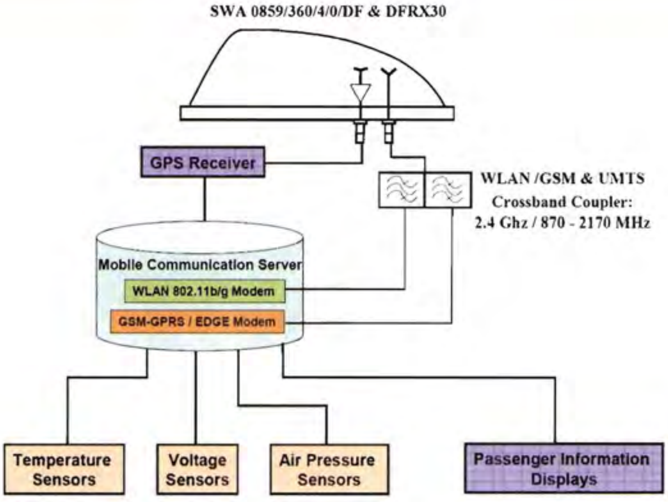

Figure 4: Mobile communication server for train operation using GSM and WLAN data transmission

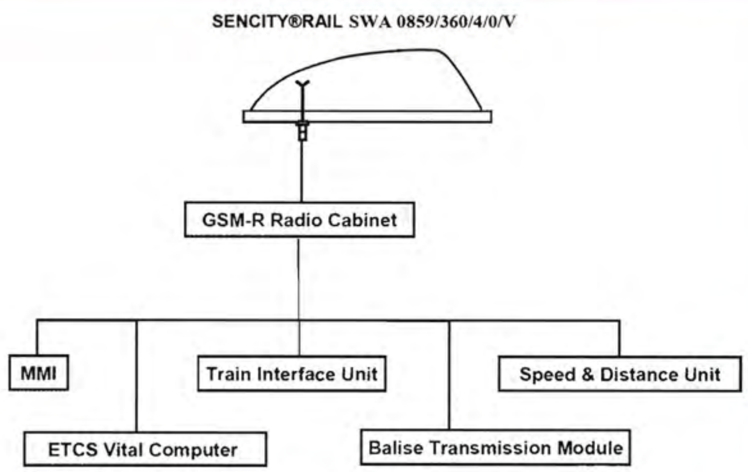

Figure 5: Typical application of Sencity Rail for GSM-R (ETCS)

The Sencity Rail antenna will be connected to the communication server either through GSM-GPRS/EDGE or WLAN. The communication server is the central unit for monitoring and controlling all non-security related, remote trainborne devices. It communicates with the different terminals, sensors, control boards and MMIs onboard the train. All information collected from the remote sensors and terminals will be re-converted to RF and sent back to the train control centres for further processing. The communication server will also handle the passenger information system. As such, it will make use of GPS to provide the passenger information system with exact timing and positioning information.

Security and safety related information will not be handled through this system as it will be exclusively processed by the European Train Control System (ETCS), which utilises a completely different infrastructure based on the GSM-R radio interface.

ETCS and GSM-R

Even though Sencity Rail supports GSM-R, it is not specifically tailored for a single-band application like this. A key advantage of the antenna is its unique broadband design in cases where GSM-R does not play a major role. GSM-R will make use of a completely separate network and will not share equipment with other systems. In fact, a minimum distance plus additional filtering between GSM-R antennas and other rooftop antennas is required for safety reasons.

Trackside antennas

For public mobile communication, the existing cellular networks are used with special equipment for tunnels. Tunnels for high-speed tracks usually have a relatively large profile and, typically, Yagi-type antennas are used, which combine a small profile and high gain. For railway tunnels that have been built along conventional tracks, leaky feeders provide coverage inside the tunnels.

Wi-Fi hotspots are currently widely deployed in station areas to enable high-speed data interchange with trains that have stopped over. To facilitate Wi-Fi coverage in station areas and along the track, Huber+Suhner offers antenna solutions including bi-directional trackside antennas. These can be simply fixed to the catenary poles and, as such, do not require any additional masts and groundings.

For comparison, the different wireless services are summarised in **Figure 7**.

Infrastructure

There are two ways to move data on and off trains: update data or real-time data. The method used depends on the data requirements. Update data is refreshed sporadically and is ideal for news events – relatively small updates are uploaded every 15 minutes to an hour using the wireless LAN links at stations. In addition, a wireless LAN link in the overnight depot would be used to upload large files such as advertising. Real-time data is ideal for Internet surfing, emailing and accessing files from a central server, such as an Office document, for example.

There are three solutions to achieve data transfer with widely varying transfer rates. Firstly, the complete trackside coverage method requires many access points positioned along the track every 10km or so. For example, the London to Edinburgh line would need hundreds of access points, which will lead to a high infrastructure cost.

Secondly, a satellite system offers a fast transfer rate to upload/download large quantities of data. However, latency issues can provide annoying delays as data is bounced up to and down from the satellite. In addition, a major physical problem exists as satellite transfer requires a clear line-of-sight. Getting information onto a train has always been difficult as satellites are positioned near the horizon and many obstacles can obscure them such as cuttings, tunnels, trees and buildings. There are still a few technical issues to resolve to receive satellite on trains, including needing a specialist antenna and losing satellite lock. Finally, a UMTS or GPRS (GSM network) system can be used for limited amount of data, but tends to be slow. The GSM network is already installed, but coverage tends to be poor at the trackside, so requires some infill using additional basestations. While UMTS data rates are faster, it is still not good enough.

There are various antenna options available on the market for rail operators to choose, however, they only focus on an individual network. The best antennas can select the most effective network for that part of the track as the train moves along it.

Design challenge

The 6-in-1 antenna has been a difficult design to achieve for Huber+Suhner's development team, which took two years to develop from initial concept through to fully approved unit. An important requirement was the need to maximise performance across the full bandwidth. Also, it had to be a design that can be

Figure 6: WLAN trackside antenna

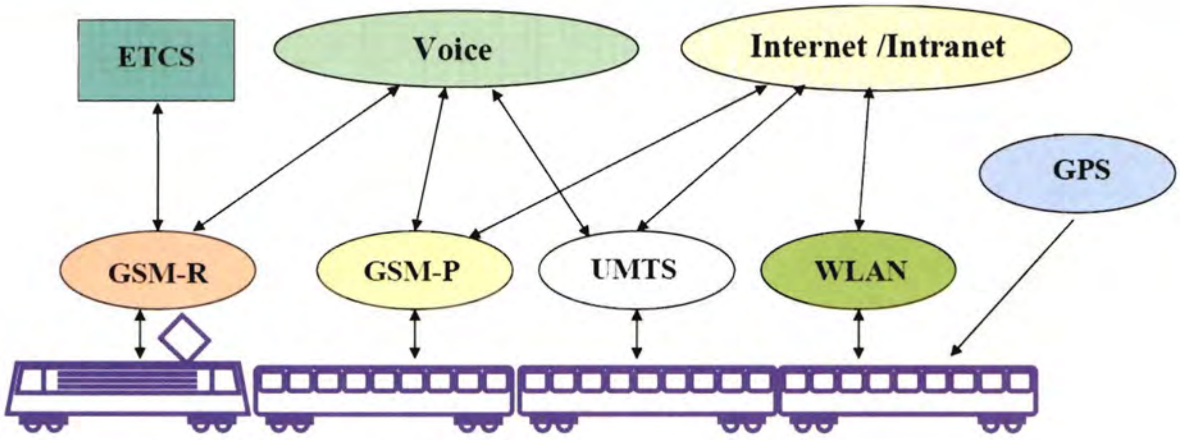

Figure 7: Wireless access for trainborne applications

produced in large quantities, something that takes skill and industry experience, as well as meeting the stringent rail requirements (e.g. waterproof on high-speed trains). As a flexible broadband device, the final solution is something that can be used across the globe.

At the start of the development process, the requirements from rail customers were initially for specific frequencies. Interest from one customer was for an antenna to cover the cellular bands, whilst another wanted to use the 2.4GHz Wi-Fi frequency and then to migrate to 5.8GHz. Rather than building one antenna to do half the job, Huber+Suhner built one that enables customers to select which network to use now, with built-in future-proofing to upgrade later.

Benefits

The benefits of a 6-in-1 system generally depend on the type of application. However, there are a number of common advantages around the physical installation. For example, one antenna covers a number of systems and, as there is very limited roof space, it is difficult to mount multiple roof antennas. Then, the solution will be lower cost, as there are fewer holes to drill in the roof. More importantly, it is much quicker to install than individual antennas – as a train is typically only available overnight for fitting, it can usually be done in one or two nights. Operators don't want the taken train out of service, so if an installation is going to take several days, it has to be done overnight, and this can take 8-10 nights, as the train has to be returned to a usable state each morning.

Upgradeability is important for the rail operator to ensure it keeps its options open. It may not be using all networks at the moment, i.e. not using the antenna to its full capacity, however, in future, if it wants to take advantage of latest technology they can simply plug in new hardware. For example, to move from UMTS/GSM to a 5GHz Wi-Fi system would require a triplexer and a 5GHz access point put in the server rack and plugged in. This is much cheaper and easier to upgrade as, rather than going onto the roof, it is a simple add-on in the server cupboard.

The 6-in-1 design means long cables don't have to be run around the carriage to the separate antennas, which increases loss in the system and degrades performance. Also, maintenance is easier and cheaper – contaminants, especially brake dust, can build up on the antenna dome, which may eventually require a change over. Clearly, changing one antenna rather than four is significantly more cost-effective.

The Future

Next generation systems are moving away from solely broadband networks. Omni- and higher gain antennas are focused on WLAN and, eventually, WiMax systems. The aim is to reduce the number of access points over longer distances and, hence, reduce cost and increase roll-out. Improvements to wireless omni-antennas mean a more controlled radiation pattern to optimise performance.

The 6-in-1 rail antenna design is a leading-edge system, with significant R&D behind it, ready to take advantage of the latest networks to deliver great benefits to rail passengers today. It is now just a question of when a widespread roll-out will begin.

The rail operators will ultimately dictate the take-up. One of the major growth areas will be in off-the-shelf products that combine UMTS/GSM/WLAN access. For example, already available are mobile access routers that automatically select the best network to fit the criteria – i.e. at night it selects UMTS and during peak commuter use it may switch to satellite.

In the long term, we will see migration to more integrated networks and trains/passengers will simply log on to whichever is most appropriate. This seems the most sensible approach and is certainly a better roll-out technically.

In addition, it is a lower cost solution as it doesn't require dedicated networks. Switching between systems is not a new concept, commuters already have laptops that use a GSM card outdoors and then enable a switch to WLAN in airports/hotels wireless hotspots.

CCII-based universal current-mode filter employing grounded passive components only

Second generation current conveyors (CCIIs) are widely used in the realisation of the circuits such as filters, oscillators and simulated inductors because CCIIs are functionally flexible and versitile.

Moreover, current-mode operations have greater linearity, lower power consumption, wider bandwidth and larger dynamic range than their voltage mode counterparts. Grounded passive elements, especially grounded capacitors, are essential for integrated circuit (IC) process and matching is usually not desired condition in IC realisation.

Several current-mode filters have been realised by applying various circuit transformation rules on the operational amplifier based filters. Some papers have reported active RC current-mode filters using current feedback operational amplifiers. In books, quite a great number of circuits based on current conveyors have been devoted to realise universal second-order current-mode filters.

In this study, a universal current-mode cascadable analogue filter for simultaneously realising low-pass, band-pass and high-pass characteristics is proposed. This filter can also realise notch and all-pass characteristics with interconnection of the relevant output currents. The introduced filter employs five one output CCIIs (three port CCIIs), three of them are plus-type CCII (CCII+) and the other two are minus-type CCII (CCII-), thus it is easy to construct the proposed filter with commercially available active devices (AD844s).

The filter does not require active and passive element matching for realising low-pass, band-pass and high-pass responses, and employs only grounded passive elements, thus it is very easy to implement this filter in IC implementation. This filter needs no additional active and passive components to give high output impedance responses. Nevertheless, the introduced filter requires passive component matching for the notch and all-pass responses. All of the active and passive element sensitivities of the proposed filter do not exceed unity. The parameters, angular resonance frequency (ω_o) and quality factor (Q) of the proposed filter can be adjusted arbitrarily.

In other words, the proposed filter offers orthogonal control of ω_o and Q. Both of the time and frequency domain analysis of the introduced filter using SPICE program is given to exhibit the performance of the filter and to verify the theory.

CCII is a three-port active device; the port voltage and current relations are represented by the following matrix equation:

$$\begin{bmatrix} I_z \\ V_x \\ I_y \end{bmatrix} = \begin{bmatrix} \pm\alpha & 0 & 0 \\ 0 & \beta & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_y \\ V_z \end{bmatrix}$$

Here, α and β are the frequency dependent non-ideal current and voltage gains, respectively. These gains are all ideally equal to unity. The sign of α represents the type of the CCII i.e. $+\alpha$ means plus-type CCII (CCII+) and $-\alpha$ means minus-type CCII (CCII-). Current convention is such that all currents flow into the CCIIs.

Routine analysis of the circuit in **Figure 1** gives the following filter transfer functions (TFs) in **Equation 2**:

$$\frac{I_{LP}}{I_{in}} = K_1 \frac{\omega_o^2}{D(s)}$$

$$\frac{I_{BP}}{I_{in}} = -K_2 \frac{s\left(\frac{\omega_o}{Q}\right)}{D(s)}$$

$$\frac{I_{HP}}{I_{in}} = K_3 \frac{s^2}{D(s)}$$

where the denominator $D(s)$, gains K_1, K_2 and K_3, parameters ω_o and Q are found to be in **Equation 3**:

$$D(s) = s^2 + s\left(\frac{\omega_o}{Q}\right) + \omega_o^2$$

$$K_1 = \frac{R_3}{R_5}$$

$$K_2 = \frac{R_1}{R_4}$$

$$K_3 = \frac{C_3}{C_1}$$

$$\omega_o = \sqrt{\frac{1}{C_1 C_2 R_2 R_3}}$$

$$Q = R_1 \sqrt{\frac{C_1}{C_2 R_2 R_3}}$$

Interconnection of the relevant output currents with $K_1 = K_2 = K_3$, notch response ($I_{NH} = I_{LP} + I_{HP}$) and all-pass response ($I_{AP} = I_{LP} + I_{BP} + I_{HP}$) can also be obtained.

Both of the parameters ω_o and Q can be selected arbitrarily without disturbing the other parameter by choosing suitable passive components.

All of the active and passive element sensitivities of and Q are no more than unity in magnitudes.

If non-ideal gains are considered, the filter TFs in Equation 2 and D(s) in Equation 3 convert to **Equation 4**:

$$\frac{I_{LP}}{I_{in}} = K_1 \frac{\omega_o^2 \alpha_5 \beta_5}{D(s)}$$

$$\frac{I_{BP}}{I_{in}} = -K_2 \frac{s\left(\frac{\omega_o}{Q}\right)\alpha_1 \beta_1}{D(s)}$$

$$\frac{I_{HP}}{I_{in}} = K_3 \frac{s^2 \alpha_4 \beta_4}{D(s)}$$

$$D(s) = s^2 + s\left(\frac{\omega_o}{Q}\right) + \omega_o^2 \alpha_2 \alpha_3 \beta_2 \beta_3$$

It can be seen from Equation 4 that non-ideal current gains in each term of the TFs of the proposed filter are in the form of multipliers so gain-variable current conveyors can be replaced instead of the CCIIs to change the coefficients of the filter TFs or to compensate the errors in the values of the current gains α_i (i=1, 2, 3, 4, 5).

On the other hand, the CCII- implementation using two CCII+s is shown in **Figure 2**.

Simulations

The filter in Figure 1 is simulated by using AD844s with DC power supply voltages equal to ± 15 V. The CCII+ and CCII- are constructed using one and two AD844s, respectively. Moreover, the following passive element values are selected in simulations: $R_1 = R_2 = R_3 = R_4 = R_5 = 1\text{k}\Omega$ and $C_1 = C_2 = C_3 = 1\text{nF}$. Also, the parameters Q and f_o are calculated as 1 and 159.15kHz, respectively.

Both of the ideal (theoretical) and simulated low-pass, band-pass and high-pass responses of the filter are depicted in **Figure 3**.

To exhibit the time domain performance of the filter depicted in Figure 1. Both of the theoretical and simulated time domain responses are shown in **Figure 4** in which 0.1mA peak sinusoidal input currents at 159.15kHz are applied to both ideal and proposed filters.

It is observed from Figures 3 and 4 that the simulation results agree with the theoretical ones. However, the difference between ideal and simulated responses mainly stems from the parasitic and non-ideal current and voltage gains of the CCIIs.

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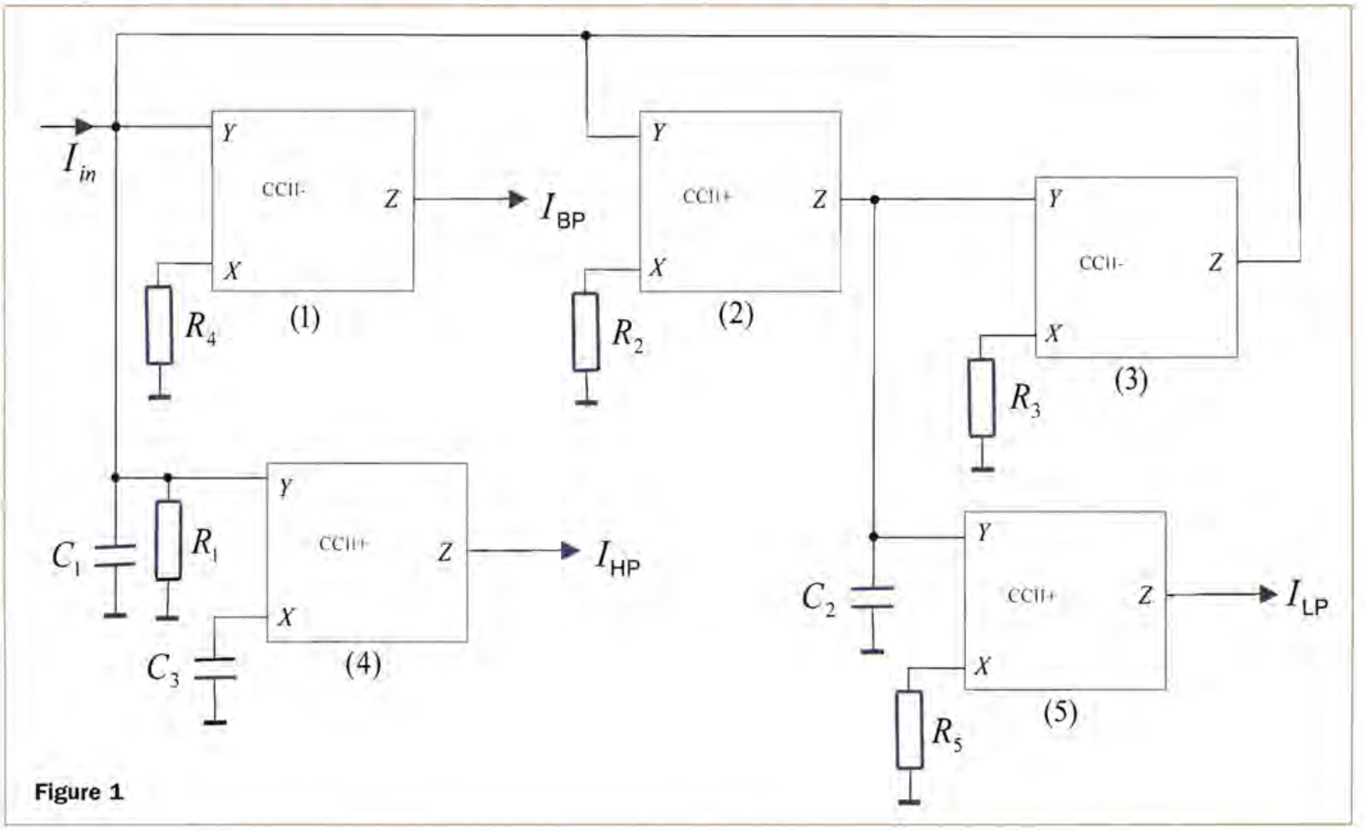


Figure 1

Figure 2

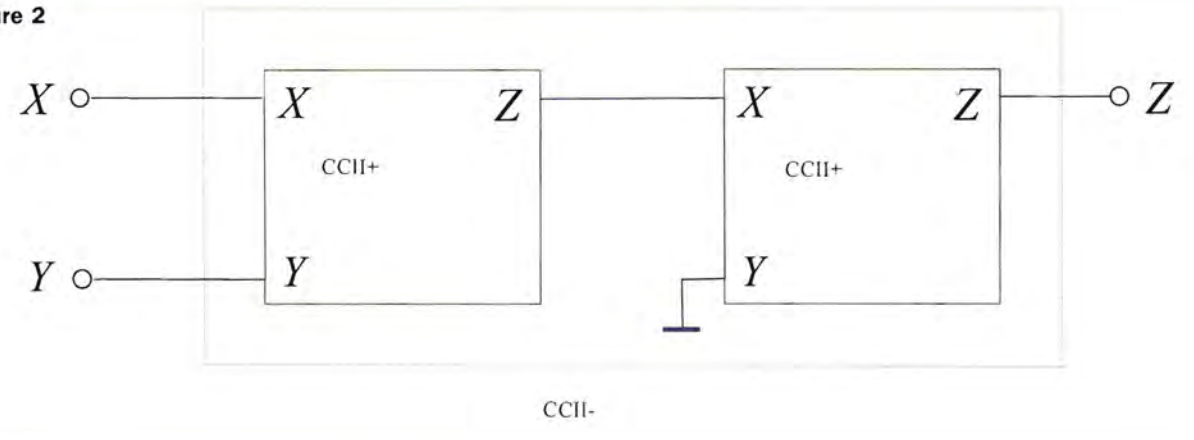


Figure 3

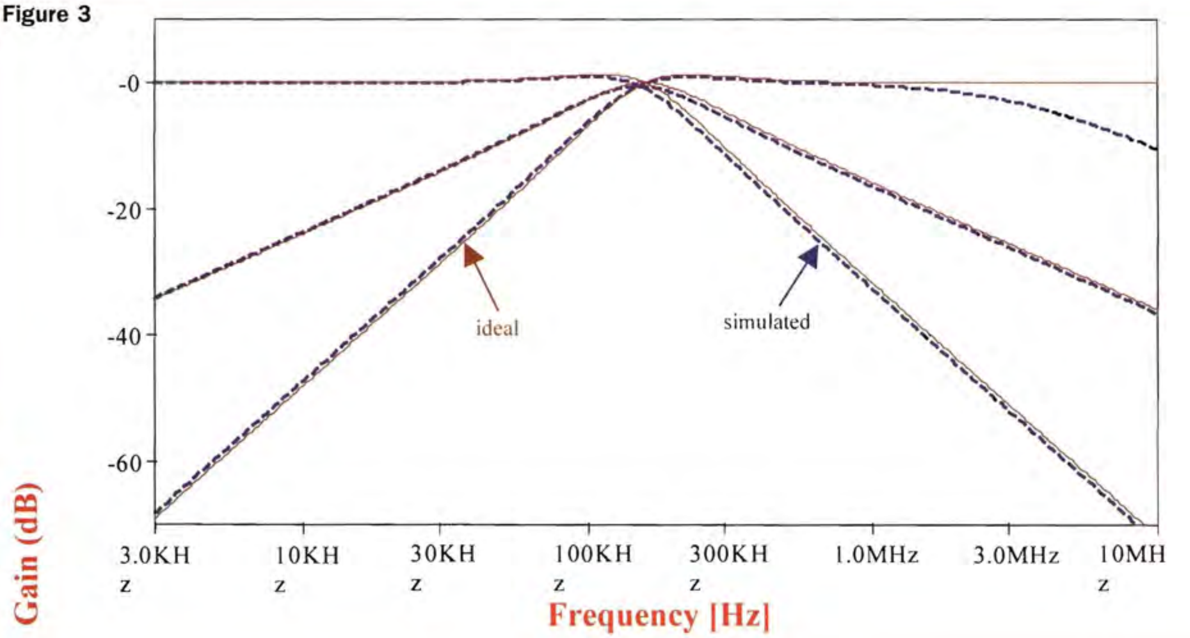
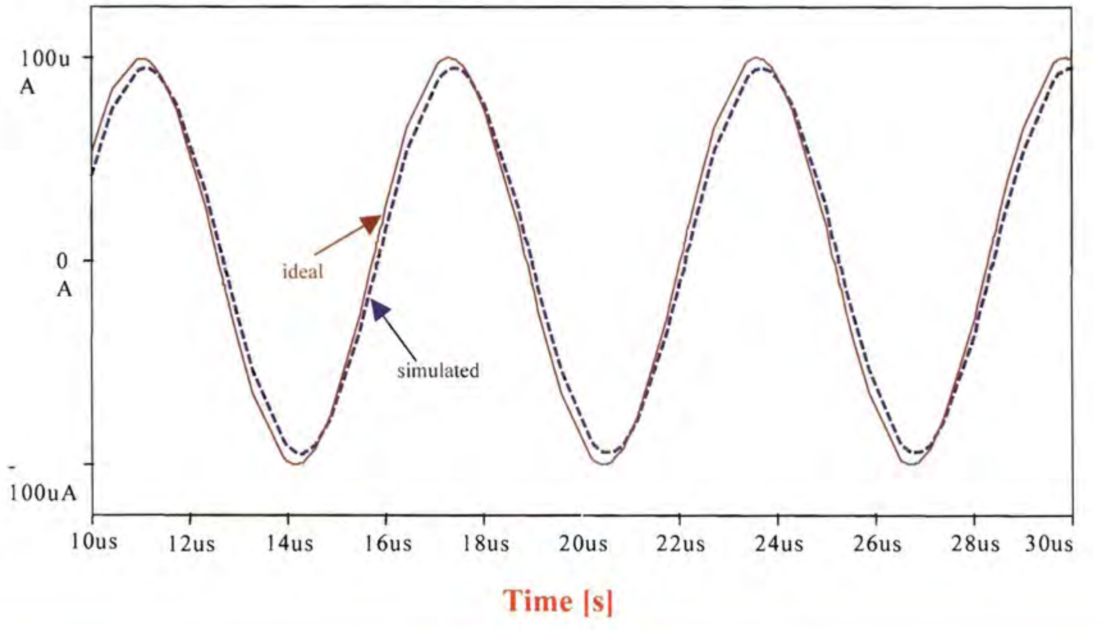


Figure 4



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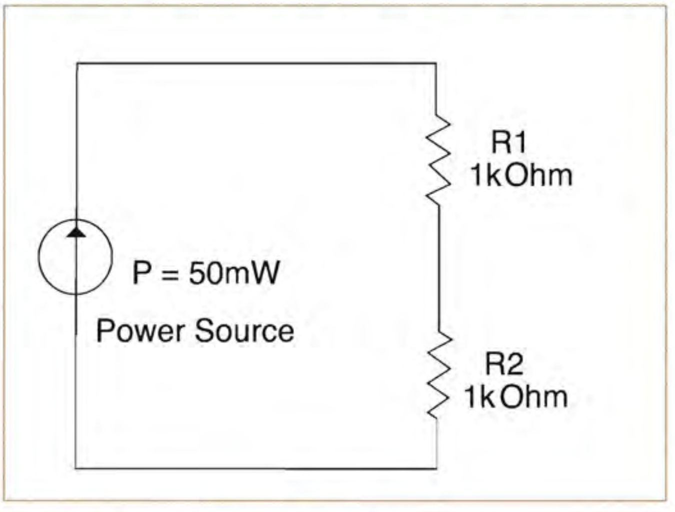
Power Divider Rule

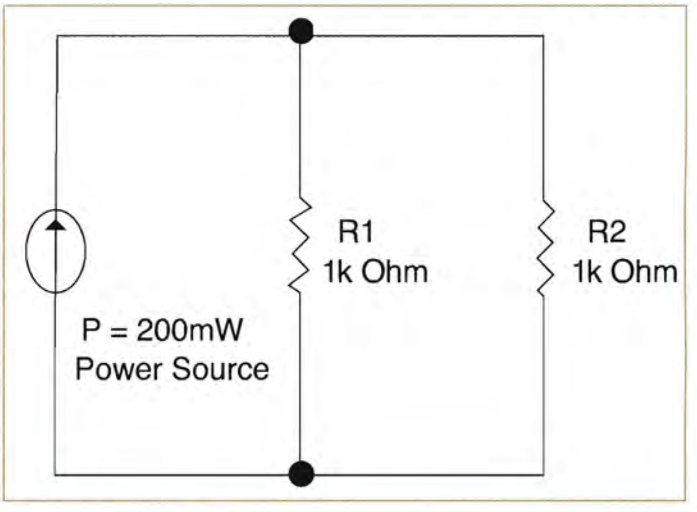
Generally, the Electrical Engineering studies have current and voltage divider formulae for circuit analysis and, also, some general formulae for power. But there is no specific formula for power such as current divider or voltage divider rule. This thought helped me to come up with the 'Power Divider Rule', which stipulates that: "The total dissipated power is equal to the total supplied power regardless of circuit configuration."

On the other hand, Norton and Thevenin had their own way to measure the amount of current flow through any resistor. Although their way is different, their intention is the same. Hence, I came up with my way of finding the amount of power in any circuits.

It should be noted that the total power used by either circuit is the sum of its individual resistors' powers. Therefore, it is clearly proved that: "The total dissipated power is equal to the total supplied power regardless of circuit configuration."

Nachimani Charde
Malaysia





Series circuit analysis:

1) Power across Resistor 1

$$PR1 = \frac{P * R1}{R1 + R2} = \frac{50m * 1k}{1k + 1k} = 25mW$$

2) Power across Resistor 2

$$PR2 = \frac{P * R2}{R1 + R2} = \frac{50m * 1k}{1k + 1k} = 25mW$$

3) Total Power: $P = P_{R1} + P_{R2}$

$= 25mW + 25mW$

$= 50mW$

Parallel circuit analysis:

1) Power across Resistor 1

$$PR1 = \frac{P * R1}{R1 + R2} = \frac{200m * 1k}{1k + 1k} = 200mW$$

2) Power across Resistor 2

$$PR2 = \frac{P * R2}{R1 + R2} = \frac{200m * 1k}{1k + 1k} = 200mW$$

3) Total Power: $P = P_{R1} + P_{R2}$

$= 100mW + 100mW$

$= 200mW$

LCD PICmicro Microcontrollers

Using an LCD PICmicro microcontroller for any embedded application can provide the benefits of system control and human interface via an LCD. Design practices for LCD applications can be further enhanced through the implementation of these suggested Tips 'n' Tricks. These tips describe basic circuits and software building blocks commonly used for driving LCD displays.

TiP 1: IN-CIRCUIT DEBUG (ICD)

There are two potential issues with using the MPLAB ICD to debug LCD applications. First, the LCD controller can Freeze while the device is Halted. Second, the ICD pins are shared with segments on the PIC16F917/916/914/913 MCUs. When debugging, the device is halted at breakpoints and by the user pressing the pause button. If MPLAB ICD is configured to halt the peripherals with the device, the LCD controller will halt and apply DC voltages to the LCD glass.

Over time, these DC levels can cause damage to the glass; however, for most debugging situations, this will not be a consideration. The PIC18F LCD MCUs have a feature that allows the LCD module to continue operating while the device has been Halted during debugging. This is useful for checking the image of the display while the device is Halted and for preventing glass damage if the device will be Halted for a long period of time. The PIC16F917/916/914/913 multiplex the ICSP and ICD pins onto pins shared with LCD segments 6 and 7. If an LCD is attached to these pins, the device can be debugged with MPLAB ICD; however, all the segments driven by those two pins will flicker and be uncontrolled. As soon as debugging is finished and the device is programmed with Debug mode disabled, these segments will be controlled correctly.

TiP 2: LCD IN SLEEP MODE

If you have a power-sensitive application that must display data continuously, the LCD PIC microcontroller can be put to Sleep while the LCD driver module continues to drive the display.

To operate the LCD in Sleep, only two steps are required. First, a time source other than the main oscillator must be selected as the LCD clock source, because during Sleep, the main oscillator is Halted. **Table 1** shows options for the various LCD PIC microcontrollers.

Part	Clock Source	Use in Sleep?
PIC16C925/926	FOSC/256	No
	T1OSC	Yes
	Internal RC Oscillator	Yes
PIC16F917/916/914/913	FOSC/8192	No
	T1OSC/32	Yes
	LFINTOSC/32	Yes
PIC18F8490	(FOSC/4)/8192	No
	T1OSC	Yes
	INTRC/32	Yes

Table 1: Options for LCD in Sleep mode

Second, the Sleep Enable bit (SLPEN) must be cleared. The LCD will then continue to display data while the part is in Sleep. It's that easy!

TiP 3: BLINKING LCD

Information can be displayed in more than one way with an LCD panel. For example, how the user's attention can be drawn to a particular portion of the LCD panel? One way that does not require any additional segments is to create a blinking effect.

Look at a common clock application (**Figure 1**). The (:) between the hours and minutes is commonly made to blink once a second ("on" for half a second and "off" for half a second).

This shows that the clock is counting in absence of the ticking sound or second hand that accompanies the usual analogue face clock. It serves an important purpose of letting the user know that the clock is operating. If there is a power outage, then it is common for the entire clock display to blink. This gives the user of the clock an immediate indication that the clock is no longer showing the correct time.

When the user sets the time, then blinking is commonly used to show that a new mode has been entered, such as blinking the hours to identify that the hours are being set, or blinking the minutes to show that the minutes are being set. In a simple clock, blinking is used for several different purposes. Without blinking effects, the common digital clock would not be nearly as user friendly.

When should you select the internal RC oscillator (or LFINTOSC) over the Timer1 oscillator? It depends on whether your application is time-sensitive enough to require the accuracy of a crystal on the Timer1 oscillator or not. If you have a timekeeping application, then you will probably have a 32kHz crystal oscillator connected to Timer1. Since Timer1 continues to operate during Sleep, there is no penalty in using Timer1 as the LCD clock source. If you don't need to use an external oscillator on Timer1, then the internal RC oscillator (INTRC or LFINTOSC) is more than sufficient to use as the clock source for the LCD and it requires no external components.

Fortunately, blinking is quite easy to implement. There are many ways to implement a blinking effect in software. Any regular event can be used to update a blink period counter. A blink flag can be toggled each time the blink period elapses. Each character or display element that you want to blink can be assigned a corresponding blink-enable flag. The flowchart for updating the display would look as pictured in **Figure 2.**

Figure 1: Common clock application

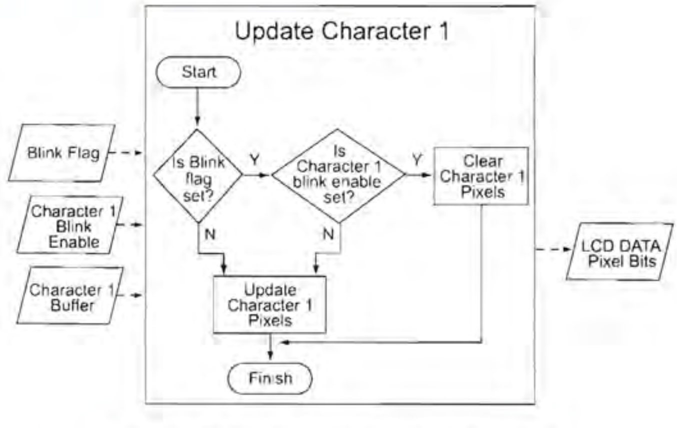


Figure 2: Updating display chart flowchart

TIP 4: 4 X 4 KEYPAD INTERFACE THAT CONSERVES PINS FOR LCD SEGMENT DRIVERS

A typical digital interface to a 4 x 4 keypad uses 8 digital I/O pins. But using eight pins as digital I/Os can take away from the number of segment driver pins available to interface to an LCD. By using 2 digital I/O pins and 2 analogue input pins, it is possible to add a 4 x 4 keypad to the PIC microcontroller without sacrificing any of its LCD segment driver pins. The schematic for keypad hook-up is shown in **Figure 3**. This example uses the PIC18F8490, but the technique could be used on any of the LCD PIC microcontrollers.

The two digital I/O pins that are used are RB0 and RB5, but any two digital I/O pins could work. The two analogue pins used are AN0 and AN1.

To read the keypad, follow the steps below:

1. First, make RB0 an output high and RB5 an input (to present high impedance).
2. Perform two successive A/D conversions: first on AN0, then on AN1.
3. Save the conversion results to their respective variables, for example, RB0_AN0_Result and RB0_AN1_Result.
4. Next, make RB5 an output high and RB0 an input (to present high impedance).
5. Perform two successive A/D conversions: first on AN0, then on AN1.
6. Save the conversion results to their respective variables, for example, RB5_AN0_Result and RB5_AN1_Result.
7. There are now 4 variables that represent a key press in each quadrant of the 4 x 4 keypad:

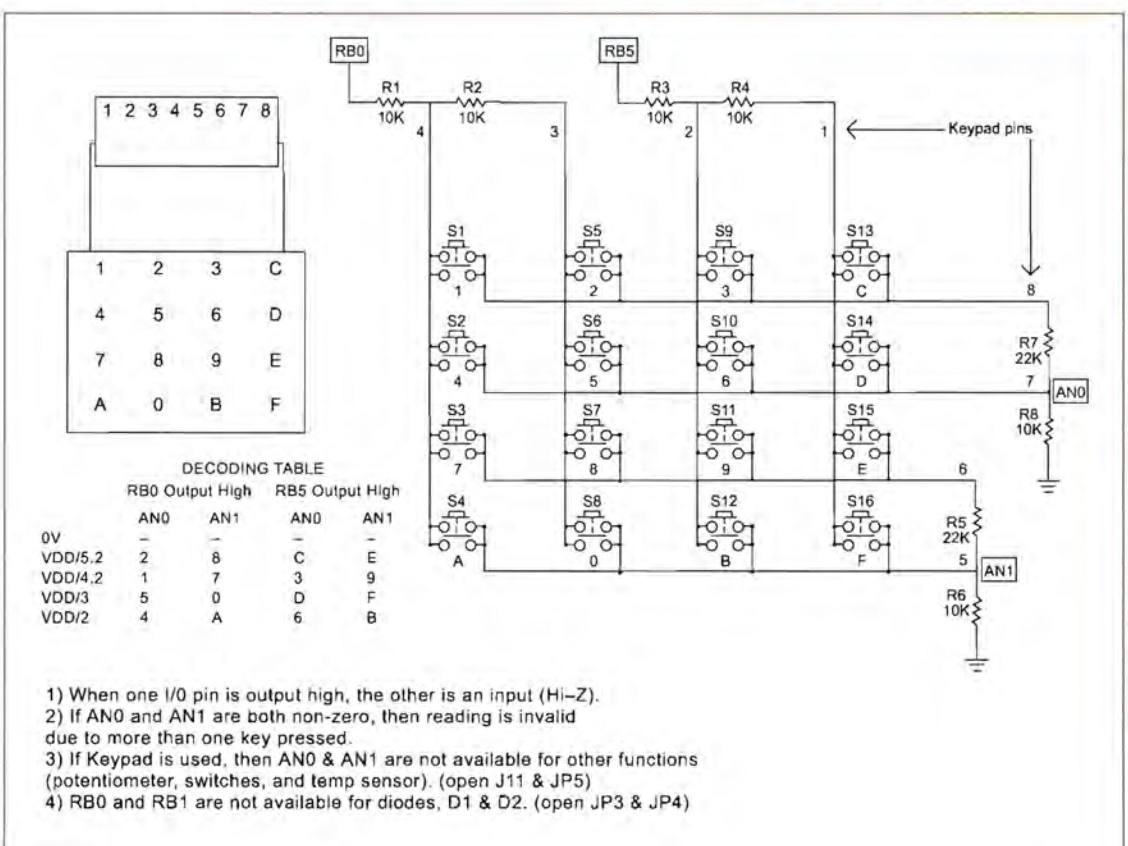


Figure 3: Keypad hook-up schematic

Value ±10%	RB0_AN0	RB0_AN1	RB5_AN0	RB5_AN1
<VDD/10	—	—		
VDD/5.2	2	8	C	E
VDD/4.2	1	7	3	9
VDD/3	5	0	D	F
VDD/2	4	A	6	B

Table 2: Keypad values

- RB0_AN0_Result . denotes key press of 1, 2, 4 or 5
- RB0_AN1_Result . denotes key press of 7, 8, A or 0
- RB5_AN0_Result . denotes key press of 3, C, 6 or D
- RB5_AN1_Result . denotes key press of 9, E, B or F

8. Finally, check each value against the matching column of **Table 2**. If it is within ±10% of a value, then it can be taken to indicate that the corresponding key has been pressed.

9. This loop should be repeated about once every 20ms or so. Don't forget a debounce outline. For example, require the above steps (with 20ms delay between) to return the same key value twice in a row for that key to be considered pressed. Also, require a no key press to be returned at least twice before looking for the next key press. When keys within the same quadrant are pressed simultaneously, voltages other than the four valid levels shown in the table may be generated. These levels can either be ignored, or if you want to use simultaneous key presses to enable certain functions, you can add decoding for those levels as well.

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Harwin's new Hot Shoe technology connectors employ spring loaded or compliant contacts, which maintain a positive contact force against the mating half of the connector, ensuring reliable connection even under the most demanding conditions. Fabricated using highly durable plastics, the connectors are designed to withstand dust, water and chemical agent ingress.

Featuring low mating forces, the Hot Shoe range enables rapid and simple connection. The connectors tolerate mating misalignment and are often polarised ensuring no possibility of mis-mating. The robust nature of the range ensures continued reliability throughout a product's lifecycle, whether on the combat arena or in less harsh environments.

Hot Shoe connectors are also suitable for use in portable equipment where separate battery modules are used, for data transfer docking stations, and for battery charging and data communications equipment. Other applications include thermal imaging cameras, in-vehicle detachable equipment and hand-held scanners.

www.harwin.co.uk

Lead-Free WLAN Module for the Embedded Space

TDC has announced a lead-free intelligent Wireless LAN 802.11b/g module range from Ezurio designed specifically for the embedded market. Thanks to these modules, any machine with a serial interface can take advantage of the proliferation of hotspots, now also becoming a domain for systems using 8-bit and 16-bit microcontrollers.

Four versions are available with Ezurio's own Universal Wireless interface which includes the WLAN protocols, TCP/IP stacks, network drivers, the application processor and serial interfaces.

Two form-factors are available: a 32.5mm x 35mm footprint, compatible with GSM modules such as the Siemens MC55 from TDC and the second, a slightly smaller 25mm x 35mm format compatible with the BISM Bluetooth modules. The footprint compatibility gives designers flexibility in the choice of wireless connectivity. The SLIP interface as an alternative allows designs which are already TCP/IP enabled to use WLAN.

The module also contains two configurable 10-bit ADCs, two configurable 10-bit DACs and nine GPIO ports available for application use. It also contains an embedded web server that will allow the creation of dynamic web pages, allowing products to become accessible securely over the Internet from anywhere in the world.

www.tdc.co.uk

Non-Magnetic Connectors for Medical Applications

Now available in the UK from Quadrant is a range of non-magnetic, D type sub-miniature connectors from FCT, designed for use in medical equipment.

These new connectors have shells manufactured from brass with a tin or zinc plating as opposed to standard 'D' connectors that are manufactured in steel.

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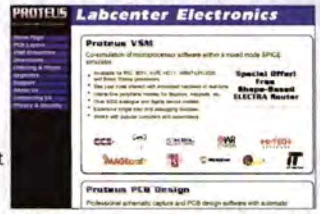

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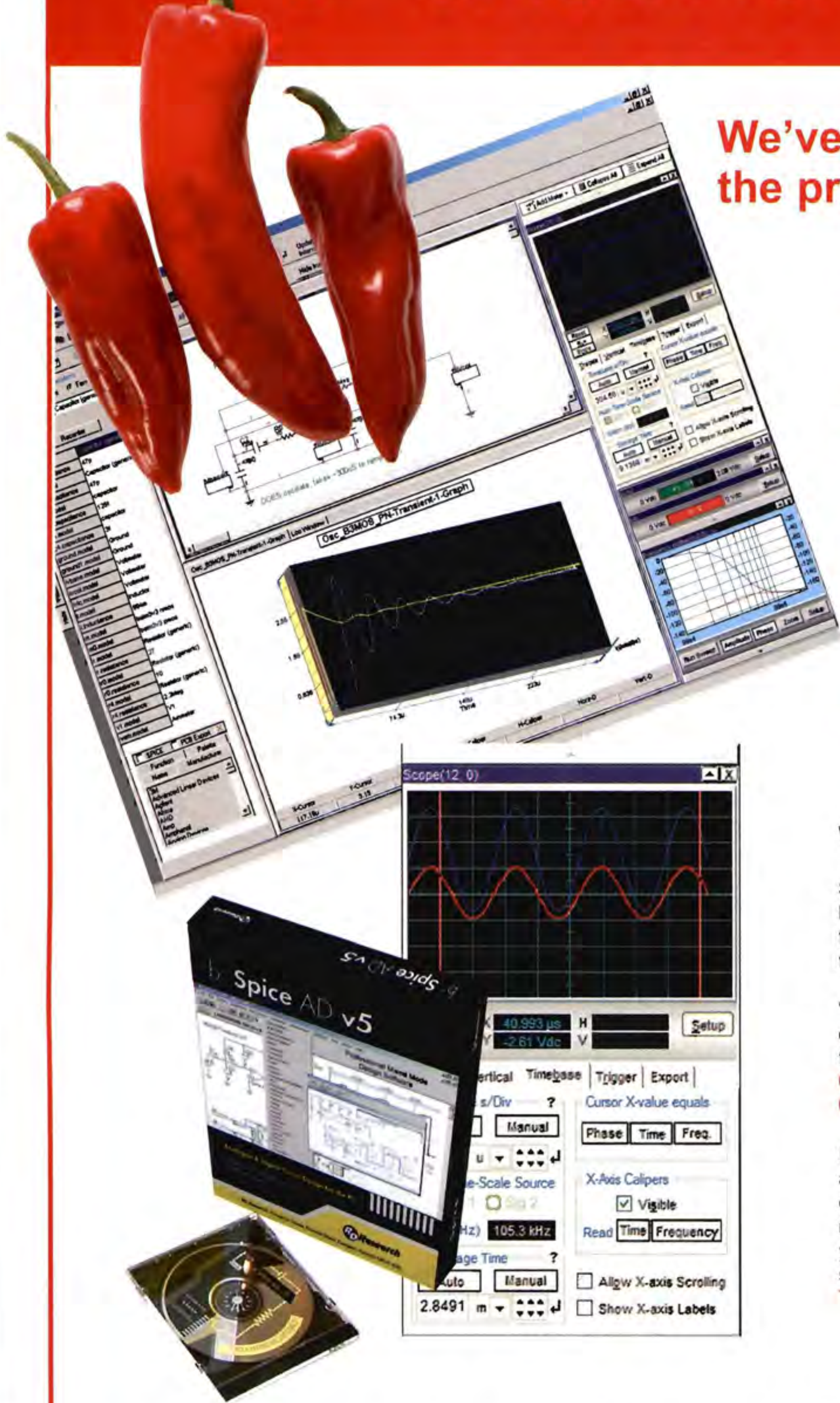

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