# ELECTRONICS WORLD

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## Automotive Wire Harness Design

## New Interconnect Technologies

## Raman Scattering and Optical Fibre Communication

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Front cover image supplied by Tundra Semiconductor

# Learning through light exercise

The Massachusetts Institute of Technology (MIT) has stumbled upon a project that, it says, it has taken the world by storm. FabLab (Fabrication Laboratory rather than Fabulous Lab) is a suite of off-the-shelf, industrial-grade fabrication and electronics tools, wrapped in open source software and programs written by researchers at the Center for Bits and Atoms at the MIT.

According to MIT's director of Bits and Atoms – Dr Neil Gershenfeld, who was recently visiting the UK, the project has proven the sequence of 'empowerment ➢ education ➢ problem solving ➢ job creation ➢ invention' over and over again, wherever the FabLab concept has been adopted. And it has! The tools have been used to create a "muffled scream box" in the US, a domestic animals herd 'supervisor' in the Alps, a milk 'tester' in India and for solar power generation in Ghana among others.

On FabLab's website, the concept has been described as being able to "give users around the world the ability to locally conceptualise, design, develop, fabricate and test almost anything. Since local communities themselves foster innovation, it can lead to sustainable solutions. We believe FabLabs will provide a thriving incubator for local micro-businesses."

Dr Gershenfeld talked fervently of this project, even though to his UK audience it appeared no more than a technically souped-up, wider-reaching Blue Peter. However, one interesting aspect is the project's result, which is bringing electronics to the masses – and the non-technical crowd at that. Most of the takers seem to be in the developing countries rather than the western world, which had prompted an industry observer to say that students here are dropping off engineering courses because "we are boring them" (instead of, what, giving them FabLab?).

This comment leads us nicely into the subject of "what's wrong with the engineering courses". I don't think students in the western world universities and colleges are bored but, rather, ground to death. When I was at university doing my electronic engineering degree, we could have easily done with a 36-hour day to complete all of our lectures, projects and home study. Our fellow students in geography and political sciences, on the other hand, managed to fit all of this in, plus a few beers at the local pub, organise a march or two at the students' union – in less than twelve hours, as well as have a social life to the envy of Tara Palmer-Tomkinson.

We – the engineering crowd – just kept on studying, and to what benefits? Engineering is still not as recognised as some other disciplines, funnily enough, including the extremely woolly "science" of politics. And it is so much easier to gain a degree just about in any discipline (bar a couple) than in engineering. A top boss in a big engineering firm is more likely to be a former economics or business graduate than engineering one. Engineering is still not as well paid as some other professions and certainly it does not command as high a status in society.

So, maybe the right road to attracting students to engineering in the western world would be not necessarily with FabLab and similar 'fun' concepts, but with simplified courses, raised profile of the discipline in society, better rewards (salaries and other benefits) as well as a wider recognition of well-known engineering individuals – and that should be just the beginning.

Svetlana Josifovska
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# THERE IS INTERESTING NEWS


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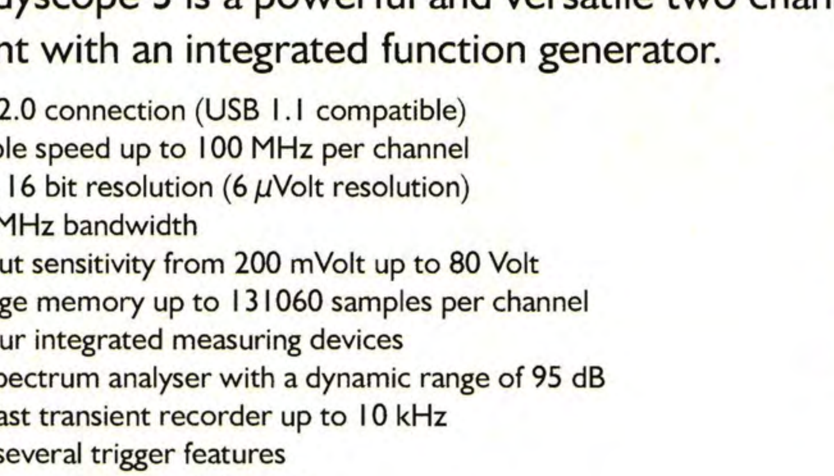


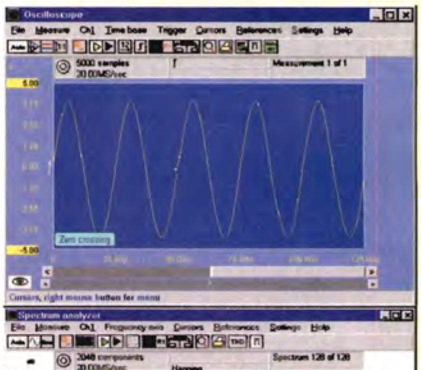


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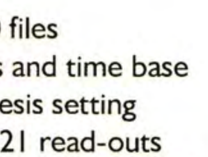

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MicroStencil from Scotland has created a new type of electro-formed stencil that will allow the fabrication of sub-100 micron aperture pitch with very good quality. The product has the potential to deliver considerable advantages in the field of interconnecting technology and offers particular benefits in screen-printing for wafer bumping and chip bonding.

Ω

The market for MEMS (MicroElectroMechanical Systems) will grow at a Compound Annual Growth Rate (CAGR) of up to 20% to nearly six billion units in 2009, reports market research firm In-Stat. Funding for MEMS companies increased by 43.9% in 2004 versus 2003, as the market continued to show strong sales. Year-over-year total MEMS revenues were up 32% from 2003 to 2004. "There was strong growth in 2004 as Texas Instruments moved into the number one position in terms of revenue with $880m in sales of its DLP device," said Frank Dickson, In-Stat analyst.

Ω

Fujitsu has started to sell its new service robot dubbed enon. This is seen as an advanced practical-use, service robot for providing guidance, escorting guests, transporting objects and security patrolling. It is light in weight, small in size and has many safety features. For example, enon can detect when people stand in front of it. The robot offers voice and visual communication. It is a result of the collaboration between Fujitsu Laboratories and Fujitsu Frontech.

Ω

Semiconductor developer Renesas Technology announced that it will start working with the China Automotive Technology and Research Centre (CATARC) to boost the development of electronics technology for the Chinese automotive industry. Renesas will contribute by providing appropriate microcomputers and technical support for automotive systems developed by CATARC.
Renesas provides microcomputer-based system solutions for car audio, dashboard, body control and car navigation systems.

# Industry expects cautious moves to 40Gbit/s

Though only a small number of 40Gbit/s systems have been deployed, and those that have are experimental, the industry is quietly confident that this will be rolled out on a mass scale, the only question is when.

As such, a number of companies are introducing products or at least planning upgrades up to 40Gbit/s. Some of these were on show at ECOC, the largest fibreoptic communications event in Europe, that took place in Glasgow this year.


Southern Photonics, which makes equipment for use in research and development laboratories, has seen a growing demand for products that work with 40Gbit/s.

"For a while, people were saying 40Gbit/s would never see the light of day," said John Harvey, CEO at Southern Photonics. "Now people say it will happen, they just don't know when the telcos are going to invest in the infrastructure."

Terasea, which makes transponders for optical fibre systems, will have its 10Gbit/s system on show but is not expecting to have a 40Gbit/s product out until next year. "The reason we are not pushing hard is because we don't see a real 40Gbit/s market today," said Haim Laufer, Terasea's VP for sales and marketing. "Some providers say they can do 40Gbit/s but when we ask the telcos they say it will be two to three years, and they were saying that three years ago."

One company that has taken the plunge is the Centre for Integrated Photonics (CIP), which will have on show an all-optical 2R regenerator for optical networking up to 40Gbit/s. It is using a technique on its optical circuit board called passive alignment to keep the cost down.

Most equivalent optical components use active alignment where the fibre waveguide is moved around in front of the semiconductor optical amplifier chip until there is sufficient coupling, and then it is welded in place. "This is an expensive process, but most are done that way," said David Smith, chief technical officer at CIP. "It is very labour intensive."

CIP uses lithography to ensure correct position of the waveguide and to build a stop against which the chip can be pushed. This claims CIP gives accuracy to within one micron.

"Our product would be almost impossible to make using active alignment," said Smith. "This is for 40Gbit/s systems; 40Gbit/s is just starting to appear for actual operation. People are starting to get interested in the high speeds."

# Crystal growth speeds switching

A dramatic reduction in the speed of optical switches has been made possible by growing a (Pb,La)(Zr,Ti)O3 (known as PLZT) crystal on an Nb-doped semiconductor substrate.

This technology has let Nozomi Photonics build a one-input, eight-output optical switch the size of a credit card that can achieve a rise and fall time below 10ns. This compares with optical MEMS that go down to about 5ms. The switch was launched at ECOC.

"It is suitable for applications such as optical packet switching and switched delay lines," said Jerome Prieur, sales and marketing director.

The PLZT crystal has a high refractive index and electro-optical coefficient, and is insensitive to polarisation, the combination of which gives it its high speed.

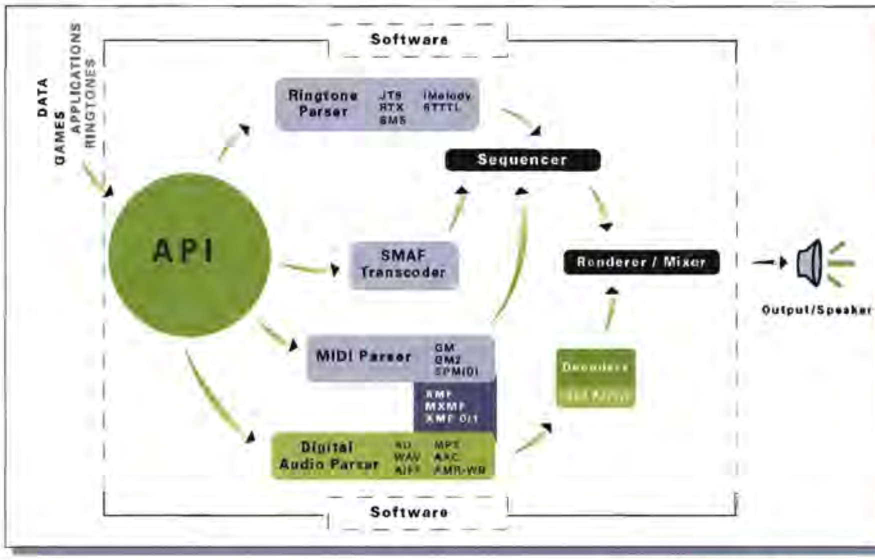
# Beatnik's audio engine goes off the beaten track

The audio side of the mobile phone handset has not been fully exploited by service providers, but its time will come soon. So says Jeremy Copp, chief sales officer of Beatnik, a supplier of audio software.

"Today all is focused on video. But just imagine the services you can offer with an audio engine embedded in the phone. Services like richer multimedia messaging and digital samples – where you can attach a sound clipping or voice before forwarding it on to someone else; 3D audio; advertising – where a sound byte will follow a video clip; gaming – where the sound mimics the pace of the game; and so much more," said Copp.

Beatnik's audio engine – the mobileBAE – is available for licensing and key handset suppliers, like Nokia, Motorola and Sony Ericsson, and chipmakers like Texas Instruments and Freescale, are existing licensees.

"There are 700 million mobile phones shipped this year, 70% of their manufacturers are our lincensees," said Copp.




mobileBAR's data flow model

The engine's program code size is configurable from 160kB to a maximum of 400kB. It takes less than 1MHz of processing power for a polyphonic voice. It is architecture-agnostic, so it can be used with any microprocessor and supported with any acceleration device, like a DSP for example.

The BAE incorporates a synthesiser, mixer, sample rate converter, linear audio player and support for MIDI, SP-MIDI, XMF, RMF and WAV file formats. The synthesiser relies on configurable wavetables (to 300kB) and offers 8-48kHz sampling rates.

"Anyone can write an engine for a PC, where there's lots of memory and processing power available. It's a lot tougher to make it run in a resource-constrained device," said Copp.

Beatnik has only 17 employees today, of which 12 are software developers and technical support. Despite that, the ambition for the firm is to "be in every mobile phone in the world", says Copp.

# Single molecule is enough to be a transistor

Single atom's effects on a molecule prove ground-braking

A team of researchers at the University of Liverpool has confirmed the theory that a molecule can act as a transistor. They created a prototype capable of demonstrating that a single charged atom on a silicon surface can regulate the conductivity of a nearby molecule.

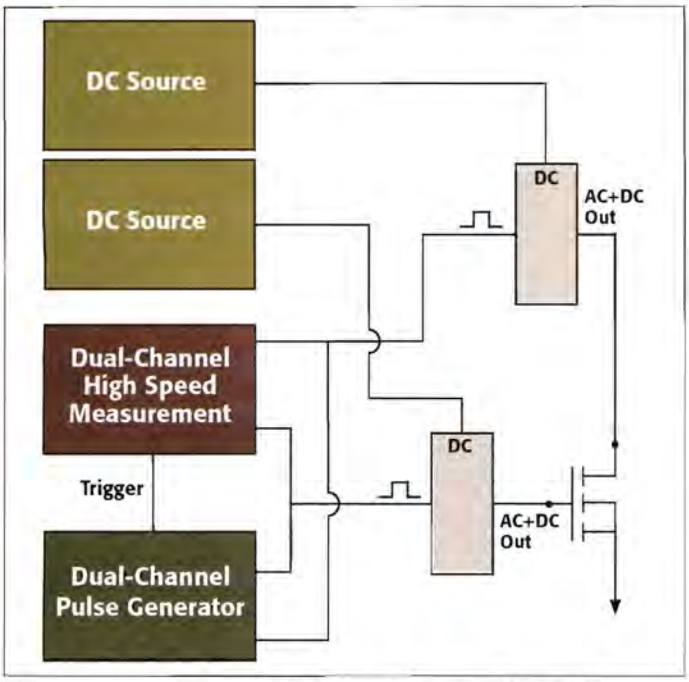
This is seen as a breakthrough in molecular electronics as it paves the way for much smaller transistors without having to involve expensive lithography equipment. It also allows for electronic devices to be devised from materials other than silicon.

The team's setup revolved around the electrostatic field of a single atom. By manipulating this field, the team regulated the conductivity of the molecule, allowing electric current to flow through it. The effects were easily observed at room temperature in contrast to previous molecular experiments, which had to be conducted at temperatures closer to absolute zero and rendered much smaller currents.

The University of Liverpool's team of researchers was led by Dr Werner Hofer and also worked in collaboration with the University of Alberta in the US and the National Research Council's Institute for Nanotechnology in Canada.

"Our experiments demonstrate that we can control the current through a single molecule by charging a single atom on a silicon surface, while all surrounding atoms remain neutral," said Dr Hofer. "Computers and other technologies based on this concept would require much less energy to power, produce much less heat and run much faster. Hence, they would be cheaper and more efficient than current devices and have the potential to power green technology because of the biodegradable nature of the device."

# European universities need technology and motivation to compete




New, advanced, pulse current-voltage instrument from Keithley

Klaus Leutbecher, Germany-based sales and marketing director for Europe at Keithley Instruments says that Western European universities need to "get their act together" if they were not to lose out to universities from India and China in getting funding and research work.

"There's less funding available to universities [from governments], so universities go out and look for industrial partners. But, the industry goes out to places like China and India where students are equally educated, highly motivated and work for a tenth of the western salaries," he told *Electronics World*.

"Universities in Western Europe have to be become more aggressive in adopting technology and motivate their students. They have to generate awareness that they [Western countries' students] are not alone and that they are competing with India. They have to get their act together."

Leutbecher suggests that Western European governments also help out in this quest by keeping local electronics industry alive through better directed funding and benefits promotion. "The benefits [technological advantages] we have today will slowly erode. We need to aggressively promote our advantages: we are closer to technology and we still have capital. But we [also] need to take away [subsidies] from fishing and agriculture and direct it into R&D [for the electronics industry]," said Leutbecher.

"We cannot compete on reducing our salaries but by deploying advantageous technologies we can boost productivity by a factor of 10."

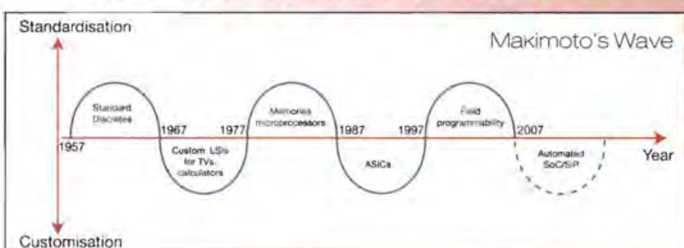
Keithley Instruments prides itself on being at the cutting edge of technology. It recently launched the compact-form 4200 model pulse-current voltage (PIV) instrument aimed at researchers, engineers and designers working on leading-edge semiconductors and processes.

The evolution of semiconductor technology is already beginning to demand new measurement techniques beyond DC source-measure to completely characterise new materials and devices. Pulse is essential for devices with isothermal limitations (SOI devices, FinFETs, Power FETs) to avoid self-heating, charge trapping and charge pumping for high k gate dielectrics and AC stress for device reliability among others.

# New 'hump' for Makimoto's Wave

The next twelve years will give rise to automated system-on-a-chip (SoC) and system-in-package (SiP) technologies in semiconductor manufacture, according to Dr Tsugio Makimoto, a corporate advisor to Japanese electronics giant Sony and the creator of Makimoto's Wave.

"The next wave – from 2007 to 2017 – is automated SoC/SiP, based on maskless technology, JISSO technology and new design methodologies," Dr Makimoto told *Electronics World*. "This leads to configurable structured eASICs, differentiated by one mask only and are NRE [non-recurring expenses] free. And this is just the beginning. All the major processes have to be automated and human intervention minimised. Devices specific to an area – automotive, consumer electronics etc – will be automated, but not so generic [outside their field]."




"This is a challenge not just for the semiconductor people but all engineers in all fields," he added.

JISSO technology is a single word that in Japanese describes a complete solution for interconnecting, assembly, packaging, mounting and integrated system design. It is based on a thorough integration of SoC, SiP and system-on-board (SoB).

# Silicon Laboratories launches "revolutionary" oscillators

US firm Silicon Laboratories claims it has devised a "revolutionary" method for manufacturing frequency control devices and it's using this method to deliver the first in a series of VCXOs – including a quad frequency oscillator.

Instead of building the oscillator and then tuning it in several steps, as in traditional methods – which adds to delivery lead times, the company is taking an oscillator and then adding a circuit to it that will tune it to the best frequency margins. This circuit uses digital signal processing, based on a Silicon Laboratories proprietary architecture optimised for filtering functions, as well as converters to get the best results.

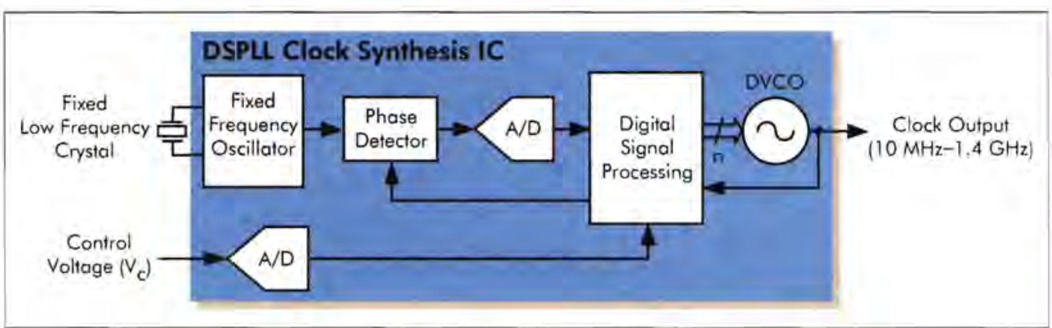
"We assume the oscillators start out with a certain frequency, so the circuit determines the frequency offset (from the final wanted frequency) and takes it out [filters it] by programming for it," said Mike Petrowski, marketing director at Silicon Laboratories. "Today, this [oscillator manufacture] is very much a built-to-order business and what we are offering is revolutionary. We moved the value of the machining of the [traditional] oscillator into the IC. We've eliminated the bulk of a 12-step [traditional] process. What we offer is pre-produced batches of devices that customers can choose from."

In addition, Silicon Laboratories's circuit eliminates the accuracy and stability problems typically associated with the aging of the resonator structures in Surface Acoustic Wave (SAW) oscillators. "Our devices can be optimised for aging," confirmed Petrowski.

For its Si530/Si550 devices, the firm quotes yearly aging of 1ppm, accuracy of 1ppm and tuning linearity of less than 5% BSL, which is 10 times better for accuracy, five times better for aging and three times better for tuning linearity than in inverted Mesa devices (XO/VCXO).

Petrowski says that Silicon Labs's 10-year involvement in PLLs and expertise in CMOS processes has led to come up with such a novel approach to making oscillators.

One of the first devices that the firm is introducing is a single-output, four different frequencies (up to 1.4GHz) oscillator.




DSPLL-based oscillator technology from Silicon Laboratories

• Nanowatch • Nanowatch • Nanowatch • Nanowatch • Nanowatch • Nanowatch • Nanowatch • Nanowatch • Nanowatch •

**Georgia Tech researchers** have developed a nanohelical structure that could provide engineers with a new building block for creating nanometer-scale sensors, transducers, resonators and other devices that rely on electromechanical coupling. It is based on a superlattice composed of alternating single-crystal "stripes" just a few nanometers wide. As such, the "nanohelix" structure is part of a family of nanobelts – tiny ribbon-like structures with semiconducting and piezoelectric properties – that were first reported in 2001.

**A team of chemists from** the University of Edinburgh is one of the first to manipulate nanoscale machines (two millionths of a millimetre high) to move an object that is visible to the naked eye. The breakthrough will offer great advantages in laser technology applications, where for example, people will be able to move objects 'remotely' with laser pointers.

TOP 10 TIPS

## Fault Finding

**CAUTION: These tips are based on experience with high power, high voltage electronic equipment.**

- Switch off the equipment.
- Use the fire extinguisher.
- Don't touch anything.
- Make a cup of tea.
- Sit down.
- Get out the equipment handbook.
- Analyse what was happening immediately before the fault.
- From 7 & 8 narrow down the area of the fault and possible cause.
- Open up and replace damaged components.
- Switch on carefully.

These month's Top Ten Tips were supplied by Chris G Gardiner from the UK. He says: *"On so many occasions, I have seen people follow the sequence 1, 2, 9 in their panic to get the equipment working again; as a result they have destroyed clues to the fault and taken longer to complete the repair than if they had first enjoyed their tea."*

If you'd like to send us your top five or top ten tips on any subject you like, please write to the Editor at **EWadmin@nexusmedia.com**

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# Vive la revolution ...in software design

Paul Hollingsworth advises software developers to throw away the concept of system design and use the data assets that already exist

Over the last forty years, software design and development has had many evolutionary steps but no revolutions, until now. In that time, we've witnessed – or driven – many changes. For example, from structured, procedural coding to object orientation, from server-only UI (user interface) to client-server and the introduction of thin clients and application servers, from flat files to RDBMS (Relational Data Base Management System) and OODBs (Object Oriented Data Bases). In the world of integration we've seen lots of change over the years including transaction management systems, EAI (Enterprise Application Integration) and xml. But without exception, these developments have all been step changes; fundamentally, we've not changed the way we design and develop software systems.

Back in the 'bad old' days, we used to define scope in terms of function. As the designer built lower level detailed functional models, the data required to support the function was identified. By the end of the 70s, or certainly by the mid 80s, most designers had changed around and either developed their data models first or, at least, as an equal partner to the functional model. Today, we're still generally doing exactly the same. This mind-set works on the premise that we have a fixed scope of function and data interest and that in order to deliver complete end-to-end architectures, someone else can have the trouble of integrating. Of course, in some industries such as defence, designers often have the luxury of having an end-to-end scope, but for most of us in the commercial world and, especially those of us building commercial of the shelf (COTS) products, we have no idea of the final completed architecture.

> *"In some industries, designers often have the luxury of having an end-to-end scope, but most of us in the commercial world have no idea of the final completed architecture"*

I believe that the concept of software we all have in our heads is: a set of functions with an associated local data store and with Application Programming Interfaces (APIs) provided to integrate with other systems. End-to-end architectures are built from islands of function and data (usually centred on an RDBMS or OO data store), which are integrated by a 'lucky' designer.

So, why should we change this way of thinking and of building island applications? After all, there is a cart full of technology to help integrators link systems together. What is the problem with continuing to build new functions around a local database? Well, it is clear to most large organisations that they've got enough – or rather too many – databases. Across many industries the direction is to reduce cost and increase agility and this requires reducing the number of databases in the enterprise (or corporate) architecture.

This is where the first software development revolution that I've witnessed comes in and it is remarkably simple: All the data that you need already exists and is in an application that is accessible to you as a designer. We must stop developing systems around a separate new database and start to build applications that use the existing assets of the enterprise that your system will be working in.

This is not so simple, otherwise we'd have had this idea before – and made it work. Some of the problems that face us are: the performance and scalability of APIs to get the data, the vast variation of data schemas and structures that hold the data and the management of data state. However, there are tools available to you that resolve most of these problems. There are a growing number of revolutionary companies building conceptually new software based upon this simple but radical shift of design.

The old king has not yet been overthrown but the revolution has started and is gaining momentum. So throw away your concept of a system design, start using the data assets that already exist and join the revolution.

*Paul Hollingsworth is Director of marketing at Celona Technologies, a radical software company in the product portfolio management arena.*

# Mobile phones for all

By John Walko

Focus on just the basics – voice and maybe text messaging. That is the key to a hugely promising business emerging for electronic component makers, mobile phone network operators and manufacturers, and, perhaps most importantly, for the millions of people in developing countries that don't yet have, or cannot afford, the convenience of mobile telephony.

Making wireless more affordable is an admirable aim. There are considerable challenges to meeting the target and not just for the many semiconductor and electronic component makers, such as Infineon Technologies, Texas Instruments (TI), Freescale Semiconductors, Philips Semiconductors. All of them have started targeting what is becoming known as the 'Ultra Low Cost' handset sector.

At the other end of the supply chain are the handset designers and makers – from small design groups, many based in the Far East, to large Tier 1 handset suppliers such as Motorola and Nokia. They have the technical challenges and, yet, the handset is just one part of the equation. Service providers, especially in the developing markets, will have to work on significantly lower cost, simpler-to-manage infrastructure gear and cost of ownership regimes than are common in developed markets, not to mention imaginative tariff structures. And regulators and governments will have a crucial role to play for this to take off by devising equally imaginative methods for spectrum access and tax regimes.

In the middle of this chain and very much driving the ultra low cost initiative, also known as they the Emerging Markets Handset initiative, is the GSM Association. At the core of this is the reality that even though 80% of the world's population has wireless coverage, or an estimated 1.4 billion GSM users this represents only 25% of the potential.

*"The price of the handset is only one hurdle. We are also pushing hard for further positive changes that can be effected by governments"*
***Rob Conway, Chief Executive, GSMA***

The Association announced the first results of the initiative at this year's 3GSM exhibition and conference, held in Cannes, France, when it revealed Motorola had won the first round of contracts to supply sub-$40 (ex-factory) phones based on its C114 platform. The aim is to make six million of the handsets for eight operators serving countries such as Bangladesh, India, Malaysia, the Philippines, Turkey and Russia.

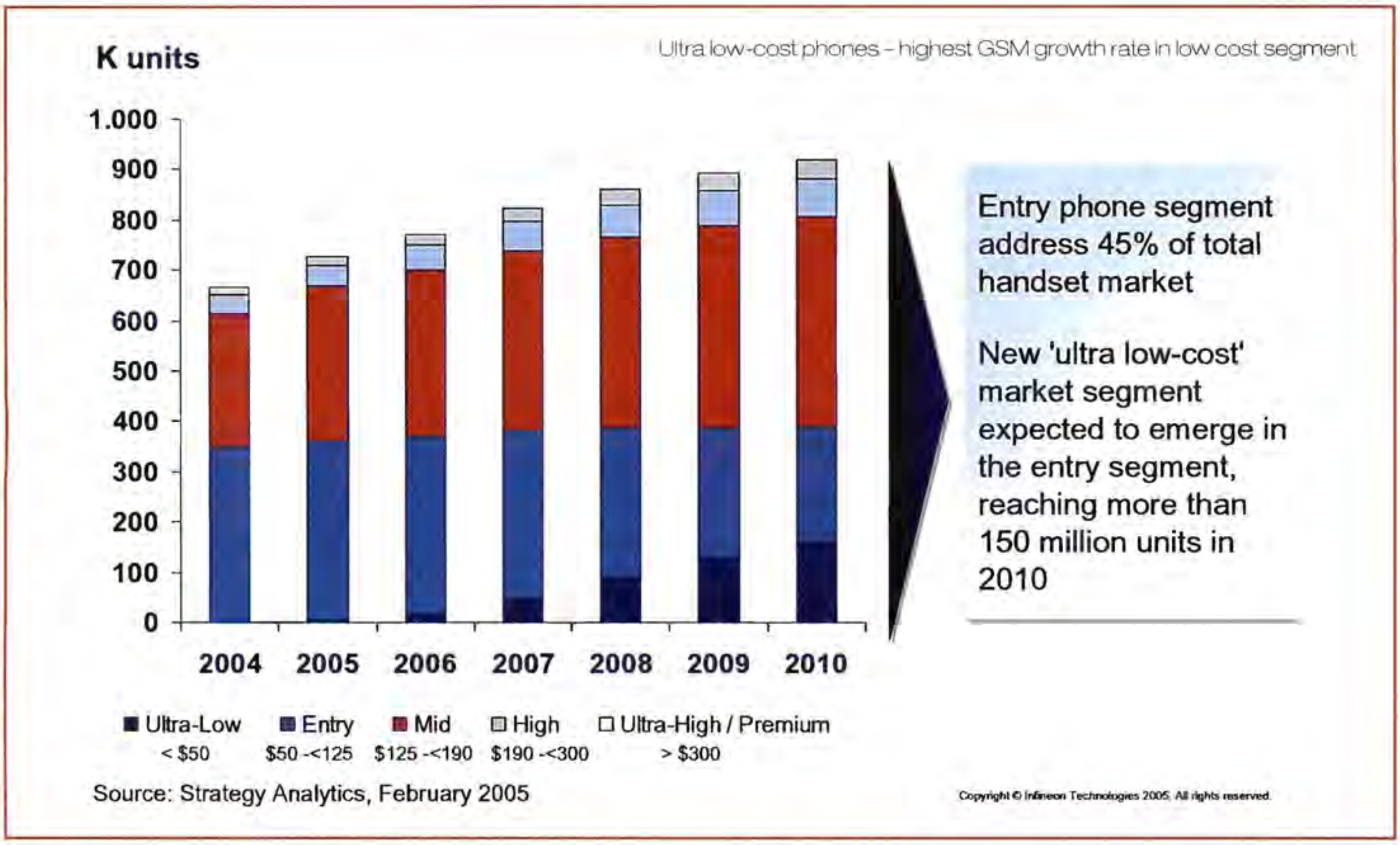
A year earlier, the GSMA brought together a group of its operator members that serve developing markets to create critical mass through a special procurement initiative. This 'leadership summit' then set up a working group to devise a specification for such low cost handsets. Tenders were issued and this resulted in further dialogue with 18 different handset vendors.


Motorola is already making the handsets at factories in the Far East and says it is on track to meet the initial six million handsets shipped target. "The key to success in this high growth market is achieving economies of scale – in procurement, testing, manufacturing and distribution so as to get the most appropriate handsets into the hands of the needy customers at realistic prices," said David Taylor, Motorola's director of strategy, high growth markets for India, South East Asia and Africa. Taylor was talking to *Electronics World* just days after relocating from the UK to India to spearhead the handset maker's efforts.

He admits margins can be tough to achieve, "but we are in business to make money, and this is a commercial business". And while he is very supportive of the GSMA initiatives, Taylor asserts "we have been selling ultra low cost handsets and will continue to do, even without their welcome moves."

The GSMA announced a follow-up tender in July to attract more handset makers and cover more emerging markets. The winner of this was due to be announced in late September, with handsets, this time priced below $30, scheduled to start production from the first quarter of 2006.

The second phase also projects six million handsets to be sold within the first six months. "We are very satisfied with the




way this aspect of the emerging handsets market initiative is proceeding and it is great to see such companies as Texas Instruments, Infineon and Philips take up the challenge and come up with system solutions at the necessary cost levels," Ben Soppitt, who heads the imitative at the GSMA, told *Electronics World*. "We have established that by pooling their resources and thus bargaining power, emerging operators can get more attention from the handset makers, who seem more than willing to service the estimated additional 100 to 150 million customers, provided affordability can be met," he added.

The Association is now beginning to focus more on lobbying governments to reduce taxes on handsets and services. As Soppitt points out, there is little point in eking out a few dollars from the cost of the handset, if governments continue to believe that taxing mobile services can be a cash cow.

As his boss at the GSMA, chief executive Rob Conway, acknowledged recently: "The price of the handset is only one hurdle. We are also pushing hard for further positive changes that can be effected by governments, such as more flexible regulatory decisions and a more favourable approach to taxation". Conway added the Association is also encouraging "innovative payment mechanisms that could further positively reduce the barriers to ownership".

In fact, many believe service may be a bigger issue than handset costs. The magic number may not be the $30 or even $20 handset, but the $5-a-month service fee. Some operators in Asia and Africa are lowering the bar for selling blocks of minutes in prepaid cards. Schemes are also appearing that allow one person to buy a set amount of credit and then resell smaller blocks of time to others. In some markets we are seeing removable SIM cards so that several users may share a single, low-cost cell phone.

But just how low could the cost of handsets go? If the component suppliers are right, quite a lot lower. Product analysis firm Portelligent from Austin, Texas, recently surveyed its customers in the wireless and electronic component sectors, and found that 80% of the chip- and handset makers surveyed thought they could get to a $25 complete bill of materials (BOM) for a finished handset by the first quarter of 2007. Fifty-one percent said they could do it by early 2006.

The breakdown of component costs for such a phone, which would be capable of voice and texting, is shown in the table on these pages. In addition to electronic and mechanical components, the BOM includes a basic battery, monochrome LCD and the cost of final testing and manufacture as well as packaging. "All the pieces are in place for this to become reality, and with big players like Freescale, TI, Infineon and Philips seemingly committed, the mid-2006 target seems achievable," said David Carey, president of Portelligent.

According to the survey, the digital logic is one of the least troublesome factors in hitting the $25 phone, said Portelligent's Carey, especially as the baseband will increasingly fold in more analogue and other capabilities.

The display, on the other hand, is one of the trickier components to reduce in cost. It would have to be cut from an estimated $2.50 bargain-basement price today, for a 96 x 64 pixel monochrome dot-matrix LCD with icon capabilities, to an estimated $1 calculator-like LCD in the $25 phone.

The most troublesome unknown costs in the equation are those related to software and intellectual property (IP). "Those companies that have GSM IP and easy access to embedded software and real-time operating systems will have no problems; those that have to buy this in will struggle," said Carey.

Thus, he and other executives believe it is the major phone suppliers who stand the best chance, because of established supply chain mechanisms and existing relationships with component and platform suppliers. "Motorola is close to Freescale, Nokia has long standing relationships with TI, and Samsung is a known user of Philips's Nexperia platforms," notes Carey. Mind you, he cautions, Motorola opted for TI core devices in its C11x platform in an attempt to get to market quickly.

Integration at the chip and package level is one road to cheaper handsets. For example, TI recently announced digital RF processing technology that moves most of the RF function into digital processing on the baseband. Its 'single-chip' design is due to be used by, among others, Nokia for a range of entry-level handsets, including ultra low cost versions.

However, there is healthy debate in the industry about whether a 'single chip' approach is the most appropriate here. Many emphasise that it is the overall silicon die area, not the number of packages, that determines chip costs. And they, of course, point out that even some of the most sophisticated solutions typically have external memory, power amplifiers and other components.

Philips Semiconductors is even more ambitious on costs, touting a sub-$5 system solution that it believes can drive handset costs to nearer $20 ex-factory in the short term and $15 by late 2008. "The core chip comprises the GSM baseband, power management and radio transmit/receive part, as well as the necessary protocol stacks, and this is already being sampled to numerous ODMs and some major Tier 1 handset makers," said Armand Guerin, marketing manager, cellular systems group at the Dutch chip group. "We are used to getting the most out of low cost manufacturing and testing as well as software optimisation with our Nexperia platform, and we see this drive towards ever lower costs as an extension of that trend," added Guerin.

Philips has just established a special group working on driving down costs at its facility in Shanghai, China. "We see huge design activity and opportunities for these low-cost platforms and handsets in that country," said Guerin.

Infineon Technologies was one of the first to see the opportunities and its platform is based on the company's successful E-GOLD radio and its monolithic integration and CMOS RF expertise. "We started chip design targeting this sector back in 2004 and our parts are already designed in to a host of 'ultra low cost' models," said Horst Pratsch, vice president of product marketing for entry phones at the Infineon communications business group.

The company expects phones based on its package to be available for volume production in the first half of 2006, costing around $20. The platform includes all electronic hardware and software for dual mode handsets complying with GSM900/1800 and GSM900/1900 standards. "This whole business is about designing out costs, as well as ensuring easy manufacturability and very cost-efficient testing for volume runs. If you have achieved that in your hardware and software package, there are sufficient margins to be able to make a commercial business out of this," said Pratsch.

**Portelligent's estimates of bill of materials for voice and text only handsets ($)**

| | *Existing low end phone* | *Ultra-low cost phone* |
|---|---|---|
| Digital baseband | 6 | 6 |
| External memory (any type) | 3.50 | 2 |
| Passives | 2 | 1 |
| Additional RF components (inc. power amplifier, TxRx) | 3 | 2 |
| Analogue ASICs (including power management device) | 3 | 1 |
| Other (including VCO, crystal,switches) | 2 | 1 |
| **Total** semiconductors | 19.50 | 13 |
| Enclosure | 4.50 | 2 |
| PC board | 2.50 | 2 |
| Monochrome LCD | 2.50 | 1 |
| Battery (Typical 800mA) | 3.50 | 2 |
| Embedded software and IP royalties | N/A | N/A |
| Final test | 1.50 | 1 |
| Factory assembly | 1 | 1 |
| Accessories/packaging | 2.50 | 1 |
| **Total** miscellaneous costs | 19 – 20 | 12 |



SEE PAGE 62


# Impacts of stimulated Ra fibre commu

In this paper Shobhit Sachdeva describes the nonlinear properties of fibre and their applications in global optical networks

The wide development of fibre optic communication systems is a result of their large frequency bandwidth and low price. Fibre optical systems that are used today are realised for two technologies – one provides a possibility to get a low attenuation silicon fibre and another allows for a high-speed optical information transmission.

Telecom fibre optical-signal transmissions are influenced by nonlinear optical effects, because small core diameters lead to significant light intensities, even at moderate signal powers. Nonlinear optical effects play a significant role in optical communications, laser technology and optical information processing. The most important and used in communication systems are generation of harmonics, self-phase modulation of the laser beam, nonlinear absorption processes, stimulated Raman and Brillouin scattering. Complete optical fibre transmission systems are developed using nonlinear optical effects and optical amplifiers. Their application is growing but it's being limited by the cost factor.

Nonlinear effects have become significant at high optical power levels and have become even more important since the development of the Erbium-Doped Fibre Amplifier (EDFA) and Wavelength Division Multiplexed (WDM) systems. These amplifiers can boost the power in a number of channels at different wavelengths simultaneously rather than having a separate repeater for each channel. This allows many more channels to be multiplexed into a single fibre than was economically viable with optoelectronic repeaters. Although the individual power in each channel may be below that needed to produce nonlinearities, the combined effects of all channels can quickly become significant. The combination of high total optical power and a large number of channels at closely spaced wavelengths is ideal for many kinds of nonlinear effects.

### Fibre non-linearities

The response of any optical fibre to light becomes nonlinear for intense electromagnetic fields. The origin of a nonlinear response is related to non-harmonic motion of bound electrons under the influence of an applied electric field. The refractive index of silica, the major material of optical fibre, has a slight dependence on the intensity of the optical field. This dependence is known as the optical Kerr effect. The general expression for the refractive index $n$ of silica includes a constant term $n_0$, which is the intensity-independent refractive index and a power density dependent term $n_2I$, where $n_2$ is the Kerr coefficient known as second order refractive index: $n=n_o+n_2I$

Refractive index is a dimensionless parameter, optical power density is measured in Watts per square metre and, therefore, the second-order refractive index has units of square metre per Watt. Typical values of $n_0$ and $n_2$ are 1.5 and 2.5, 10-20m$^2$/W, respectively. Silica has one of the lowest $n_2$ of any optical material. It can easily be shown that high intensities are required to make the intensity-dependent term comparable to the constant one.

In spite of this, appearance of nonlinear phenomena in single- or multi-channel communication systems is frequent. Actually, nonlinearities can occur at reasonable powers of few dBm in the fibre because of large distances and small effective core area.

### Multiplexing

Telecommunications for local access has evolved slowly. Telephones, televisions, fax, the Internet and so on – the primary terminal types in today's access networks – have remained essentially unchanged in function and bandwidth for half a century or more. The limited capacity of these terminals and the fixed nature of the services they support has allowed them to smoothly evolve into efficient carriers of their respective services.

One key difficulty is that the most commonly installed fibre in local area networks does not support this bandwidth over distances of 500 metres due to modal dispersion, which limits the effective bandwidth distance product.

Wavelenght-Division Multiplexing (WDM) offers an attractive solution to increasing LAN bandwidth without disturbing the existing embedded fibre, which populates most buildings and campuses, and continues to be the cable of choice for the near future. By multiplexing several relatively coarsely spaced wavelengths over a single, installed multimode network, the aggregate bandwidth can be increased by the multiplexing factor.

The 100Gbps channel mentioned in the previous section will be a combination of many lower-speed signals, since very few individual applications today use this high bandwidth. These lower-speed channels are multiplexed together in time to form a higher-speed channel. This Time-Division Multiplexing (TDM) can be accomplished in the electrical or optical domain, with each lower-speed channel transmitting a bit (or allocation of bits known as a packet) in a given time slot and then waiting its turn to transmit another bit (or packet) after all the other channels

# four wave mixing and
# man scattering on optical
# ication systems

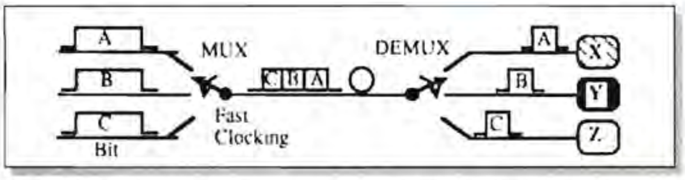



**Figure 1:** Several TDM channels with bit-interleaved multiplexing

have had their opportunity to transmit (**Figure 1**).

TDM is quite popular with today's electrical networks and is fairly straightforward to implement in an optical network at under 100Gbps speeds. This scheme by itself cannot use the available bandwidth because it is limited by the speed of the time multiplexing and de-multiplexing components.

To exploit more of the fibre's THz bandwidth we seek solutions that complement or replace TDM. One obvious choice is WDM, in which several baseband-modulated channels are transmitted along a single fibre, but with each channel located at a different wavelength (**Figure 2**). Each of the N different wavelength lasers is operating at the slower Gbps speeds, but the aggregate system is transmitting at N times the individual laser speed, providing a significant capacity enhancement. The WDM channels are separated in wavelength to avoid crosstalk when they are (de)multiplexed by a non-ideal optical fibre. The wavelengths can be individually routed through a network or individually recovered by wavelength-selective components.

WDM allows the use of much of the fibre bandwidth, although various device, system and network issues will limit the utilisation of the full fibre-bandwidth. Note that each WDM channel may contain a set of even slower time-multiplexed channels.

Another method conceptually related to WDM is Sub-Carrier Multiplexing (SCM). Instead of directly modulating a THz optical carrier wave with 100s of Mbps of baseband data, the baseband data is modulated into a GHz sub-carrier wave that is subsequently modulated into the THz optical carrier.

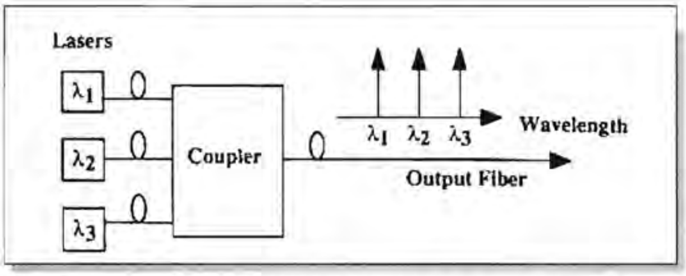



**Figure 2:** Many WDM channels propagating in a single optical fibre

## Four wave mixing

Four-Wave Mixing (FWM) occurs when two or more frequencies of light propagate through an optical fibre together – a condition known as phase matching. Here, light is generated at new frequencies using optical power from the original signals. Generation of light through FWM has serious implications for the rapidly expanding telecommunications field of WDM. The generation of new frequencies from two or three input signals is shown schematically in **Figure 3**.

The equation that defines the frequency of a FWM product is $\omega_{ijk} = \omega_i + \omega_j - \omega_k$

WDM systems send data through an optical fibre, using a number of channels, each with a designated frequency. If two or more channels interact with each other through FWM, optical power will be generated at new frequencies at the cost of reduced power in the original channels. This power loss makes it more difficult to correctly detect the digital data in these chan-

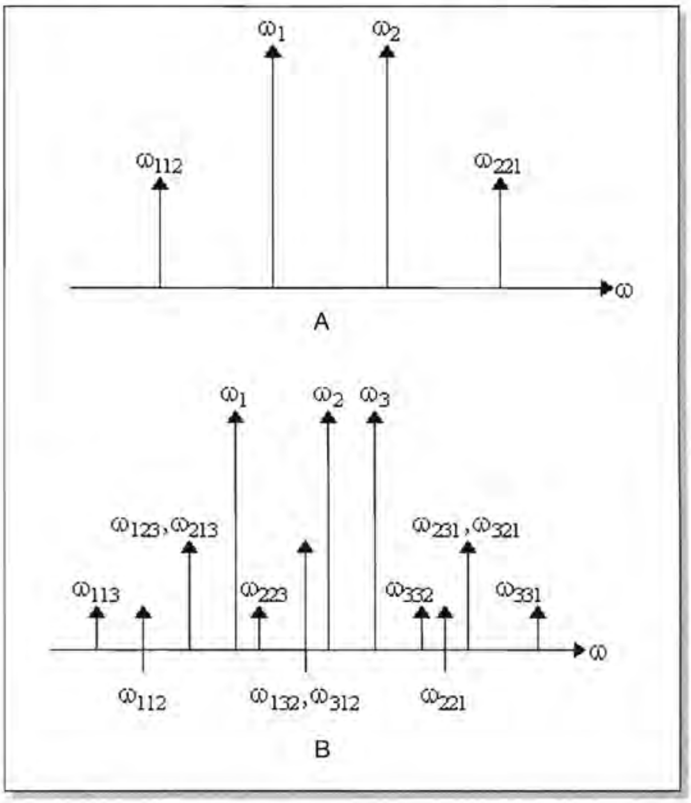



**Figure 3:** Additional frequencies generated through FWM in the partially degenerate (a) and non-degenerate case (b)

nels, making errors more likely and reducing the information bandwidth of the system.

However, four-wave mixing is not just a detrimental effect. Possible applications for FWM in fibre include:

- High-speed, all-optical frequency conversion
- Dispersion compensation in long-haul optical fibre links
- Distributed measurements of dispersion and nonlinear parameters in fibres
- Millimeter-wave generation for microcellular mobile communications

## Stimulated Raman scattering

It is an important nonlinear process that can turn optical fibres into broadband Raman amplifiers and tunable Raman lasers. It can also severely limit the performance of multi-channel lightwave systems by transferring energy from one channel to the neighbouring channels.

The Raman Effect is when in any molecular medium spontaneous Raman scattering can transfer a small fraction of power (typically $10^{-6}$) from one optical field to another field, whose frequency is downshifted, which is determined by the vibration mode of the medium.

In quantum mechanics, it is described as scattering of a photon by one of the molecules to a lower frequency photon, while the molecules make transition to a higher energy state. Incident light acts as a pump for generating the frequency-shifted radiation called Stokes Wave.

## Raman gain spectrum

With the help of Continuous Wave (CW) and quasi-CW conditions, the initial growth of the Stokes Wave is described by: $dIs/dz=g_R*I_pI_s$, where $I$ is the Stokes intensity, $I_p$ is the pump intensity and $g_R$ is the Raman gain coefficient, which is related to cross-section of spontaneous Raman scattering.

The Raman gain spectrum $g_R$ ($\Omega$), where $\Omega$ represents a frequency difference between the pump and the Stokes Wave, is the most important quantity for describing Stimulated Raman

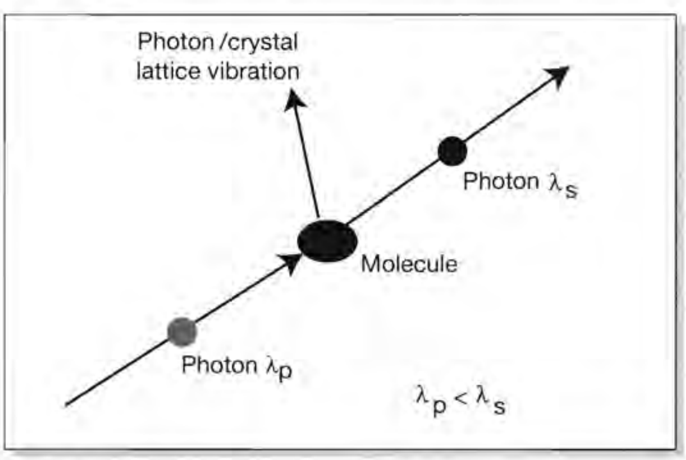



**Figure 4:** Raman Effect

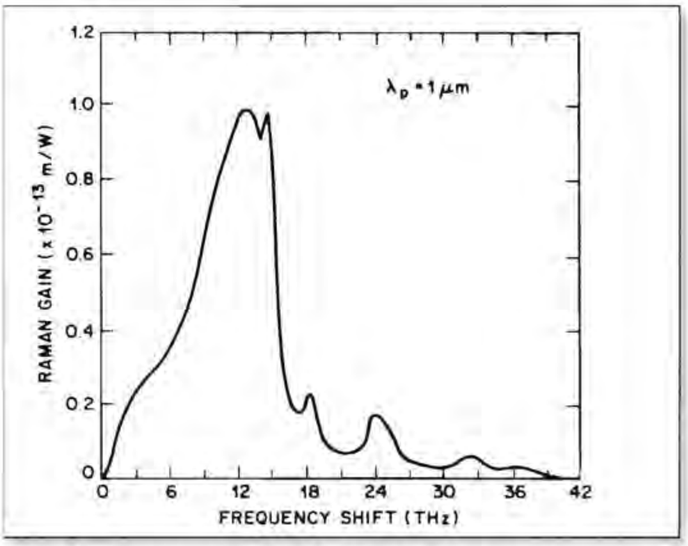



**Figure 5:** Raman gain spectrum for fused silica at a pump wavelength, λp = 1μm

Scattering (SRS). It is basically measured for silica fibres. $g_R$ depends on composition of the fibre code, varying significantly with the use of different dopants. **Figure 5** shows a graph representing $g_R$ for fused silica as function of the frequency shift with pump wavelength $\lambda_p = 1\mu m$.

The most significant feature of the Raman gain in silica fibres is that $g_R$ ($\Omega$) extends over a large frequency range (up to 40THz) with the broad peak located near 13THz. This behaviour is due to the non-crystalline nature of silica glass.

For describing practically the process of SRS, consider a CW pump beam propagating inside a fibre at the optical frequency $\omega_p$. If a probe beam at the frequency $\omega_s$ is coincident with the pump at the fibre input, it will be amplified because of the Raman gain as long as the frequency difference $\Omega = \omega_p - \omega_s$ lies within the bandwidth of the Raman gain spectrum as shown in the graph. If only the pump beam is incident at the fibre input, spontaneous Raman scattering acts as a probe and is amplified with propagation. Spontaneous SRS generates photons within the entire bandwidth of the Raman gain spectrum and all of the frequency components are amplified. However, the frequency components for which $g_R$ is maximum, builds up very quickly. In case of pure silica, $g_R$ is the maximum for the frequency component that is downshifted from the pump frequency by about 13.2THz. When the pump power exceeds a threshold value, this component builds up almost exponentially. As a result, SRS leads to the generation of Stokes waves whose frequency is determined by the peak of the Raman gain. The corresponding frequency shift is called Raman shift or Stokes shift.

## Raman threshold

The nonlinear interaction between the pump and the Stokes wave is used to find the Raman's threshold. In the CW case, this interaction is governed by the following set of equations:

$$dI_s/dz = g_R I_p I_s - \alpha_s I_s \quad (1)$$

$$dI_p/dz = -(\omega_p g_R I_p I_s / \omega_s) - \alpha_p I_p \quad (2)$$

where $\alpha_s$ and $\alpha_p$ account for fibre losses at the Stokes and pump frequencies. In the absence of losses:

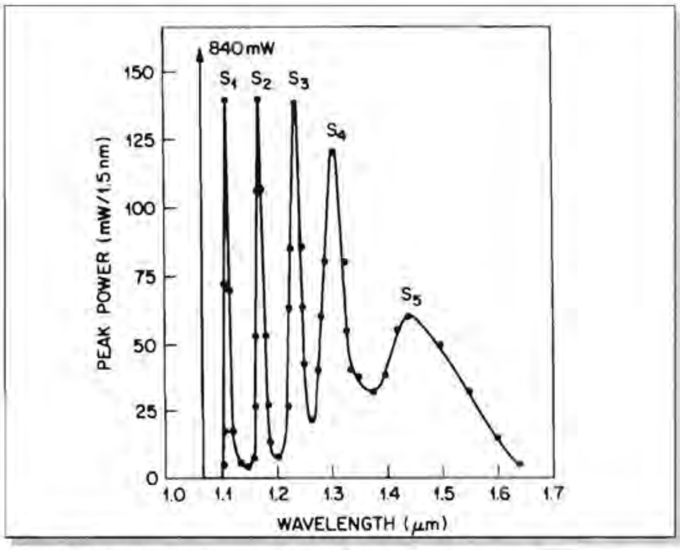



**Figure 6:** Five Stokes lines - S1 to S5 - generated simultaneously using 1.06μm pump pulses

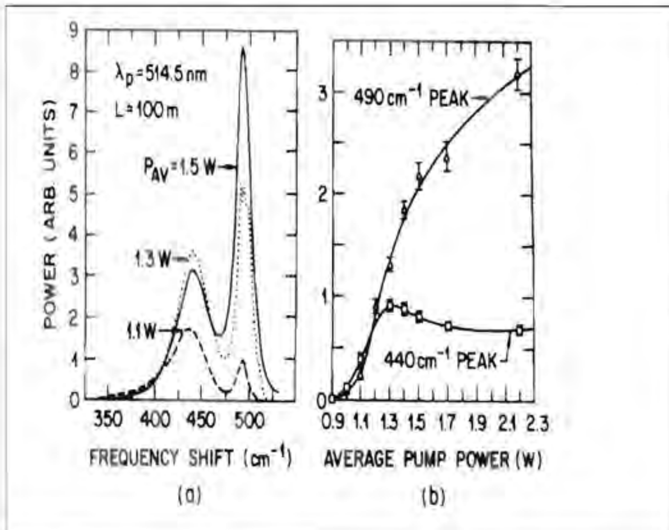



**Figure 7:** (a) Stokes spectra at three pump powers and (b) variations of peak powers with pump power

$d(I_s/\omega_s - I_p/\omega_p)/dz = 0$ (3)

This equation states that the total number of photons in the pump and the Stokes beams remains constant during SRS.

Pump depletion can be neglected for the purpose of estimating the Raman's threshold:

$dI_s/dz = g_R I_0 exp(-\alpha_p z) I_s - I_s$ (4)

Equation 2 can be solved if we neglect the first term on its right side that is responsible for pump depletion. By substituting the solution in Equation 1 we obtain:

$I_s(L)=I_s(0)exp(g_R I_0 L_{eff} - \alpha_s L)$ (5)

where $I_o$ is the incident pump intensity at z=0. From Equation 4 we can obtain:

$L_{eff} = [1-exp(-\alpha_p L)]/\alpha_p$ (6)

where $L$ is the fibre length and Equation 6 shows that, because of pump absorption, the effective interaction length is reduced from $L$ to $L_{eff}$.

Once the Raman threshold is reached, the power is transferred from the pump to the Stokes rapidly except from fibre losses.

## Quasi-continuous SRS

If the SRS is used taking pump pulses of widths in the range 1-100ns, it gives rise to quasi-CW regime. It finds its application in single pass Raman generation, Raman fibre lasers and Raman fibre amplifiers.

**1 - Single pass Raman generation**

Higher order Stokes lines appear at higher pump powers when the Stokes power became large enough to pump next order Stokes line.

The graph in **Figure 6** indicates the optical spectrum at pump power of about 1kW with five Stokes lines. Each successive Stokes line is broader than the preceding one. This broadening is due to nonlinear processes, which limits the total number of Stokes lines. Stokes lines up to 15th order have been generated in the visible region.

Further to dissolve the spectral details of each Stokes line, e.g. the line shape of the first order Stokes line, which is generated by launching a 100 metre long fibre pump pulses of about 1ns duration, obtained from a mode-locked Argon's laser.

The above graphs observe the spectra at three pump powers. They exhibit a broad peak at 13.2THz and a narrow peak at 14.7THz. If pump power is increased, the peak power of the broad peak saturates while that of the narrow peak keeps increasing.

The graphs show that SRS generates Stokes light across the entire frequency range of the Raman gain spectrum. After short length of fibre these weak signals are amplified with the appropriate gain coefficient when more spontaneous light is added. At low pump power the observed Stokes spectrum looks like $exp(g_R(\Omega))$ because of the exponential amplification process. As pump power is increased, the high frequency peak at 440cm$^{-1}$ and can pump the low frequency peak at 490cm$^{-1}$ through the Raman amplification process. The Stokes radiation generated through SRS is generally noisy because it builds up from spontaneous Raman scattering. Due to this, both the width and the energy of Stoke pulses exhibit shot to shot fluctuations, even when the pump pulses have constant width and energy. The relative noise level of pulse energy decreases rapidly as the peak power of pump pulses is increased beyond the Raman threshold. Just before the onset of the second Stokes line, the energy distribution of the first order Stokes pulse becomes considerably narrower with a nearly Gaussian shape.

**2 - Raman fibre lasers**

This is an important application of the SRS phenomenon. Such lasers can be tuned over a wide frequency range (10THz). The diagrammatic representation is shown in **Figure 8**.

A piece of single mode fibre is placed inside a Fabry-Perot cavity, formed by two partially reflecting mirrors M1 and M2. The cavity provides wavelength selective feedback for the Stokes light, generated inside the fibre through SRS. An intracavity prism allows tuning of the laser wavelength by dispersing various Stokes wavelengths spatially, each of which can be selected by turning the mirror M2. The laser threshold corresponds to the pump power at which Raman amplification during a round trip is large enough to balance cavity losses, consisting mainly of the

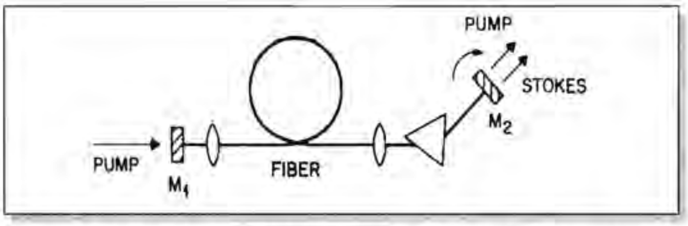



**Figure 8:** Schematic illustration of a tunable Raman laser. Mirrors M1 and M2 form a Fabry-Perot cavity

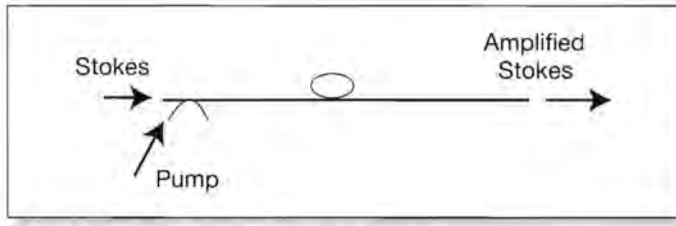



**Figure 9:** Fibre Raman amplifiers

transmission loss at the mirrors and coupling losses at the two ends of the fibre. If we assume a typical value of 10dB for the round trip loss, the threshold condition is:

$G = exp( 2g_R P_0 L_{eff} / A_{eff} ) = 10$

where $L_{eff}$ is given by Equation 6 in Raman threshold. The threshold pump power for a Raman laser is lower by at least one order of magnitude than that of single pass SRS. The threshold power is inversely proportional to the fibre length. The use of an intracavity prism allows tuning of the laser wavelength over a range of about 10nm.

At high pump powers, higher order Stokes wavelengths are generated inside the fibre. These are dispersed spatially by the intracavity prism. By adding separate mirrors for each Stokes beam, such a Raman laser can be operated at several wavelengths simultaneously, each of which can be independently tuned by turning the cavity mirror.

Even a ring cavity configuration was used to generate five orders of tunable Stokes band. Raman lasers have been operated in the infrared region from 1.1-1.6μm, which is a useful region for optical fibre communication.

When the Raman laser is pumped, each Raman pulse after one round-trip should be properly synchronised with one of the succeeding pump pulses. This synchronisation is achieved easily because the laser can select a particular wavelength that fulfills the synchronous pumping requirement among the wide range of possible wavelengths near the peak of the Raman gain spectrum. The laser wavelength can be tuned by simply changing the cavity length. This is called time dispersion tuning, which is different from prism tuning that works due to the spatial dispersion provided by the prism. This technique is very effective in tuning pulsed Raman lasers over a wide wavelength range. If the cavity length is changed by $\Delta L$, the time delay $\Delta t$ should be exactly composed by a wavelength change $\Delta\lambda$ such that:

$\Delta t = \Delta L/c = /D(\lambda)/L\Delta\lambda$

where $L$ is the fibre length and $D$ is the dispersion parameter. The tuning rate is therefore given by:

$\Delta\lambda/\Delta L = 1/cL/D(\lambda) = (\lambda^2)/2\Pi c^2 \cdot L/\beta_2/$

$\beta_2$ is the GVD coefficient for the synchronously pumped Raman lasers used for generating ultra short optical pulses. Therefore, it becomes necessary to take into account the effects of Group Velocity Dispersion (GVD), group velocity mismatch, Self-Phase Modulation (SPM) and Cross-Phase Modulation (XPM) when such lasers are pulsed using pump pulses with widths of below 100ps. If Raman pulse falls in the anomalous GVD regime of the fibre, the soliton effects can create pulses with widths of below 100fs. Such lasers are called Raman soliton lasers.

Nowadays, with the advent of fibre Bragg gratings, it has become possible to replace cavity mirrors. Fused fibre couplers can also be used for this purpose. The three pairs of fibre grating or couplers are arranged such that they form three cavities for the three Raman lasers operating at different wavelengths, corresponding to first, second and third order Stokes lines. The resulting Raman laser is useful for amplifying signals.

**3 – Raman amplifiers**

Optical fibres can be used to amplify a weak signal if that signal is launched together with a strong pump-wave such that their frequency difference lies within the bandwidth of the Raman gain spectrum. This SRS is the physical mechanism behind amplification; such amplifiers are called Raman fibre amplifiers. Their experimental setup is same as that of the Raman lasers, except that the mirrors are not needed.

Applications can vary. For example:

- These lasers could be used as a pre-amplifier before the signal is detected at the receiver of an optical communication system;

- An adaptive feature of the Raman amplifiers is related to their broad bandwidth (5THz). They can be used to amplify several channels simultaneously in a WDM light-wave system.

- Another application of Raman amplifiers is to extend the bandwidth of WDM light wave system operating in 1.55μm region.

The Raman gain from the Raman amplifiers is pursued for distributed amplification of signals. Here, relatively long spells of the transmission fibre are pumped bi-directionally for compensating fibre losses in a distributed manner. This technique is useful for solitons.

## Raman induced crosstalk

The same Raman gain that is beneficial for making fibre amplifiers is detrimental for WDM systems. The reason is that short wavelength channel can act as a pump for longer wavelength channels and, thus, transfer part of the pulse energy to neighbouring channels. It leads to Raman-induced crosstalk among channels that can affect the system's performance considerably.

In a two-channel system with short wavelength acting as a pump having almost equal fibre loss, we obtain pump depletion factor $D_p$ from the power transferred between the two channels. The curves can be used to obtain Raman-induced power penalty, defined as the relative increase in the pump power necessary to maintain the same value of output power as that in the absence of Raman crosstalk.

The power penalty is given by: $\Delta = 10 \log( 1/ D_p)$

The situation is more complicated for multi-channel WDM systems. The intermediate channels not only transfer energy to longer wavelength channels but, at the same time, also receive energy from the shorter wavelength channels. The shortest wavelength channel is most affected by Raman-induced crosstalk because it transfers a part of its energy to all channels lying within the Raman gain bandwidth. However, the transferred amount is different for different channels, as it is determined by the amount of Raman gain corresponding to the relative wavelength spacing.

## Conclusion

This paper lays emphasis on the nonlinear properties of optical communication and their effects on the system. It has also been observed that WDM-based systems are gaining in importance.

The first two nonlinear properties are not of observed much as they do not contribute in the same amount as the latter two do. XPM is basically produced when pulses undergo distortion due to interaction with different channels. This XPM is always accompanied by SPM and occurs because the effective refractive index seen by an optical beam in a nonlinear medium depends not only on the intensity of the beam but also on the intensity of other co-propagating beams. Dependence of intensity of refractive index in nonlinear optical media leads to SPM.

Stimulated Raman scattering has been reviewed, discussing its positive and negative effects, which includes Raman fibre lasers and amplifiers as the important applications.

It can be reduced by:

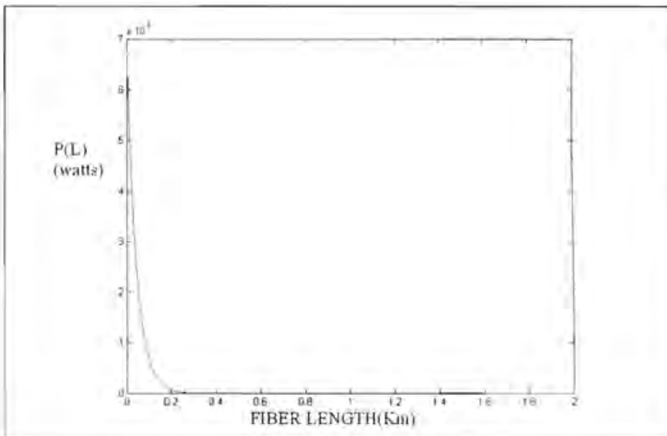
- Reducing the transmitted power
- Reducing the pulse duration
- Lowering the pulse break power
- Unequal channel separation

The characteristics of the energy losses in the Raman scattering were studied using MATLAB (see characteristics graphs).

## Implementation

The implementation code for the above using MATLAB as a tool is as follows:

```
%shobhit's work
a = 23.04;
A = 50·(10^-6);
g = 0.06·(10^-12);
P0 = 0.6;
L=[0:0.001:2];
L0 = (1-exp(-a)·L)/a;
%PL=(P0·exp(g·P0·L0)\A·exp(-a·L)
%where (g·P0·L0)\A = 16
PL= (P0·exp(-16))·exp(-a·L);
plot(L,PL);
title('STROKE'S POWER Vs FIBRE LENGTH');
xlabel('FIBRE LENGTH(in km)');
ylabel('STROKE POWER(in W)');
```



Stokes power vs fibre length

$P(L)=(P(0)*exp(g*P0*L0\backslash A)*exp(-\alpha*L)$

Where P(L) is the Stokes power, L is the fibre length and P(0) is the input pump power.

- From the above study we have deduced some of the methods to counter nonlinear effects. Periodic amplification of the optical signals in their course of propagation is such that at no point the power level crosses the threshold.
- Until power threshold is crossed by the power of the signals propagating in the fibre, these nonlinear effects may not be significant enough.
- Use of Large Effective Area Fibre (LEAF)

## Acknowledgement:

It has been a great pleasure in preparing this paper under the meticulous guidance and help of Mr. Satish Kumar and Mr. H.S. Kamath.

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# Tackling signal integrity

## Serial RapidIO basics

The RapidIO Physical Layer 1x/4x LP-Serial Specification addresses the physical layer requirements for devices utilising an electrical serial connection medium. This specification defines a full duplex serial physical layer interface (link) between devices using unidirectional differential signals. Further, it allows ganging of four serial links for applications requiring higher link performance. It also defines a protocol for link management and packet transport over a link. The introductory text below is part of the RapidIO Interconnect Specification Part VI: Physical Layer 1x/4x LP-Serial Specification.

RapidIO systems are comprised of end-point processing elements and switch processing elements. The RapidIO interconnect architecture is partitioned into a layered hierarchy of specifications which includes the logical, common transport and physical layers. The logical layer specifications define the operations and associated transactions by which end-point processing elements communicate with each other. The common transport layer defines how transactions are routed from one end-point processing element to another through switch processing elements. The physical layer defines how adjacent processing elements electrically connect to each other. RapidIO packets are formed through the combination of bit fields defined in the logical, common transport and physical layer specifications.

The RapidIO physical layer 1x/4x LP-Serial specification defines the protocol for packet delivery between serial RapidIO devices, including packet and control symbol transmission, flow control, error management and other device-to-device functions. A particular device may not implement all of the mode-selectable features presented in the RapidIO specification.

The 1x/4x LP-Serial physical layer specification has the following properties:

- Embeds the transmission clock with data using an 8B/10B encoding scheme
- Supports one serial differential pair, referred to as one lane, or four ganged serial differential pairs, referred to as four lanes, in each direction.
- Allows switching packets between RapidIO 1x/4x LP-Serial ports and RapidIO physical layer 8/16 LP-LVDS ports without requiring packet manipulation
- Employs similar retry and error recovery protocols as the RapidIO physical layer 8/16 LP-LVDS specification
- Supports transmission rates of 1.25, 2.5 and 3.125Gbaud (data rates of 1.0, 2.0 and 2.5Gb/s) per lane

A RapidIO 1x/4x LP-Serial packet is formed by prefixing a 10-bit physical layer header to the combined RapidIO transport and logical layer bit fields, followed by an appended 16-bit CRC field. The sum of all of the bit fields adds 20 bytes to the encapsulated data packet size. The maximum data field size is 256 bytes, resulting in a maximum packet size of 276 bytes.

Two classes of control symbols are defined (stype0 and stype1) and are used for packet acknowledgement, link utility functions, link maintenance and packet delineation. A control symbol is a 24-bit entity (including a 5-bit CRC code). The control symbol is used for packet delineation by placement at the beginning of a packet. The control symbol may also be embedded within a packet for message passing and link status notification, as well as sent when the link is idle.

The processing elements use acknowledgment control symbols to indicate packet transmission status. Utility control symbols are used to communicate buffer status and link recovery synchronisation. Link partner devices use link maintenance control symbols to communicate physical layer status, synchronisation requests and device reset. The physical layer is broken into two sublayers: the PCS and PMA layers describe the Physical Coding Sublayer (PCS) functionality as well as the Physical Media Attachment (PMA) functionality.

The PCS layer functionality includes 8B/10B encoding scheme for embedding the clock with the data. It also manages the transmission rules for the 1x and 4x interfaces and defines the link initialisation sequence for clock synchronisation. This function is also responsible for idle sequence generation, encoding for transmission and lane striping, and decoding, lane alignment and destriping on reception.

The PCS layer also provides mechanisms for determining the operational mode of the port as 4-lane or 1-lane operation and means to detect link states. It provides for clock difference tolerance between the sender and receiver without requiring flow control.

The PMA function is responsible for serialising 10-bit parallel code groups to/from a serial bitstream on a lane-by-lane basis. Upon receiving data, the PMA function provides alignment of the received bitstream to 10-bit code-group boundaries, done independently on a lane-by-lane basis. It then provides a continuous stream of 10-bit code-groups to the PCS, one stream for each lane. The 10-bit code-groups are not observable by layers higher than the PCS.

# ssues in serial interfaces

This article explores the signal integrity (SI) challenges and considerations that the designer must tackle, providing a practical guide to overcoming such challenges. By **André Pirnat**, senior applications engineer, Tundra Semiconductor

Signal integrity has always been a serious issue of concern to analogue engineers, but with the move towards serial data links operating at GHz data rates, the digital hardware designer now equally has to pay attention to this vital topic.

High-speed serial links between chips are now being adopted for a wide variety of applications in order to improve the throughput with a narrower bus width. Some of the latest DSPs and processors, for example, are being introduced with serial RapidIO. For many hardware designers, inter-chip communication using bus speeds over 300MHz is a new challenge they have not yet faced. Furthermore, the design of a high quality data link operating at GHz data rates requires more care and understanding to ensure that performance is not impaired by the effects of board layout and noise.

In this paper, we look at the signal integrity (SI) challenges and considerations that the designer must face, aiming to provide a practical guide to overcoming these challenges. This includes recommendations and suggestions for the successful placing, routing and decoupling of the device on a printed circuit board. A 16-port serial RapidIO switch is described, providing a practical example of how these principles may be applied.

### Signal quality

The quality of a signal is important at all points within a system and in serial RapidIO is quantified by the size of the receive eye. The eye is an infinite persistence trace where the waveform is repeatedly traced over the previous trace (see **Figure 1**). There are many opportunities for the signal quality to be compromised: by the introduction of noise or other random signals onto the signal path, by poor signal trace routing, by means of either conduction or radiation from external sources, or by generation within the system itself. All of these factors combine to shrink the receive eye. The areas that need to be considered include:

- Power supply input to the board, outputs of local regulators and distribution
- Clock generation and distribution
- Decoupling
- PCB substrate material
- Chip-to-chip connections
- Board-to-board and backplane connections
- Board stack-up and impedance control
- Inter-rack connections, cable and connectors

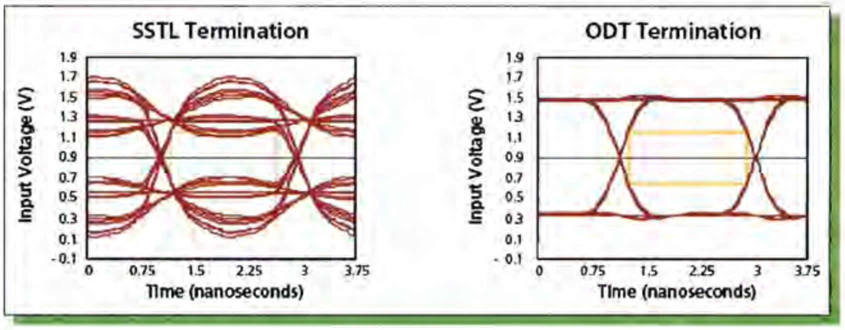
When working at frequencies above 300MHz, the majority of design best practices that are used for board layout at lower frequencies need to be revised. It is necessary to account for factors that arise as the wavelength becomes comparable to the board dimensions. This applies not only to the wavelength of the fundamental frequency but also to the Fourier components that make up the complete waveform. FR4 material may still be used successfully as a substrate, but at higher frequencies not only the permittivity of the material but also the dissipation or loss factor needs to be considered. Through-hole via design also becomes important because unused barrel length, which has a negligible effect at lower frequencies, presents an impedance mismatch in thicker boards and backplanes. The performance of post layout simulation is desirable in order to draw attention to routes of less than ideal signal integrity and point out areas of crosstalk.

Particular challenges in terms of on-board SI are created by the presence of a high-speed processor bus, high-speed memory interface, by clock generation and clock noise, and various sources of board noise such as ground bounce, crosstalk etc.

Sources of noise can typically include:

- **Single-ended parallel buses:** switching noise can result from current transients necessary to charge/discharge all the lines
- **Power distribution:** inadequate power distribu-

**Figure 1:** Scope trace containing an eye diagram



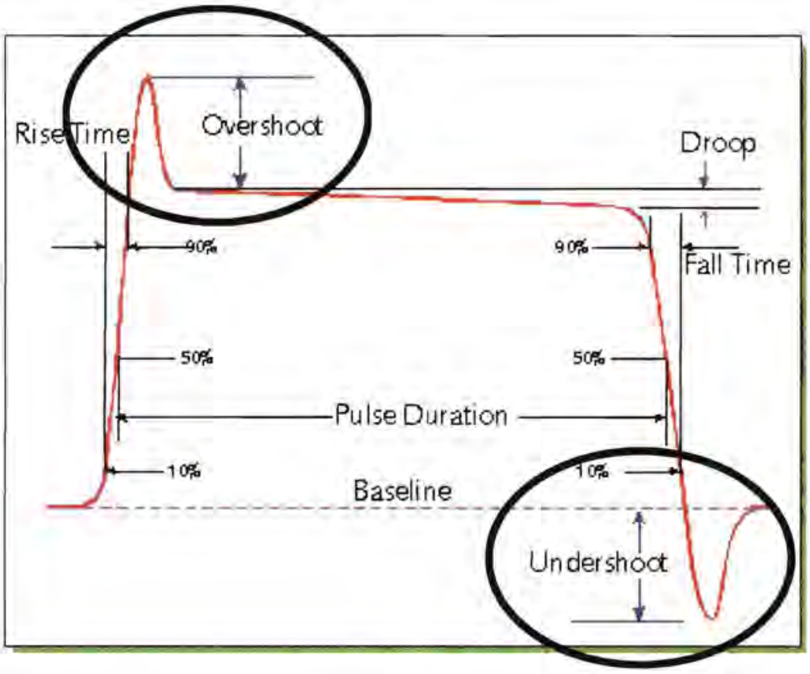



**Figure 2:** Typical overshoot and undershoot characteristics on a pulse

tion aggravates the noise dilemma, particularly if there is inadequate copper for the current demands, or inadequate or improperly positioned decoupling.

– **Impedance matching:** improper impedance matching results in reflections that can cause overshoot, undershoot and ringing on the signal lines that make up the differential pair (see **Figure 2**). This results in a reduced receive eye and increased jitter in the signal. The following items are the main causes for mismatch artifacts being introduced onto a signal:

- changes in routing layers
- poorly designed escape routing from the device

– **Ground bounce:** this causes input thresholds to change and can lead to corrupt bits. Serious cases can cause device latch-up, with power cycling required to recover from it.

– **Crosstalk:** this is caused by the close proximity of traces belonging to different signal groups. The result of crosstalk in a serial communication link is closure of the receive eye due to the imposed jitter. Crosstalk is caused by the following factors:

- insufficient track spacing to other signal
- poorly implemented serpentines for path length matching. This causes edge advancement as part of the signal takes the short path (jumping legs of the serpentine) while the main signal takes the long path.

– **Clock generation:** both clock generation and clock buffering can become noise generators unless careful attention is paid to details such as EMI filtering components and minimising crosstalk. Manufacturer's layout guidelines must be followed in order to obtain the highest quality clock signals from the device. The result of a poorly implemented clock is jitter in excess of that required by the RapidIO device. This causes poor throughput performance (evidence of which is seen in high bit-error rates at the receiver).

## Precautions

How can the designer ensure that these effects are kept under control? First of all, by adequate trace isolation between synchronous signal groups and by restricting track lengths and minimising skew between the signals of a differential pair. Routing should be carried out with a view to limiting parasitics by minimising the number of layer transitions. Vias are costly in unwanted inductance and stray capacitance and should be kept to a minimum. Usually, two vias per trace is the maximum allowable in addition to the BGA pads.

Choosing the right switch can help to meet the high-speed challenge, while more generally good design practices can help board designers take control of signal noise resulting from board level traffic. Some of these design features help in limiting external noise sources, while others are needed to address noise at the device itself.

A properly designed package that minimises parasitics is one of the first considerations, as is the positioning of power and ground pins.

In component package design, it is crucial to use a sufficient number of power and ground pins as well as placing and partitioning them correctly. An inadequate quantity of power and ground pins will increase the return current path length, which can lead to chip core supply instability and increased electromagnetic noise. Improper power and ground pin placement can also negate a decoupling strategy – the pins need to be properly placed in order to allow decoupling to be located directly under the package, with minimal trace length to control inductance. Partitioning of core logic power and ground from I/O power and ground is also critical to controlling noise.

From the perspective of device manufacturing cost, wire bond packaging may appear an attractive option, but from a signal integrity and system reliability point of view, flipchip mounting offers far more advantages. It allows for ample power and ground connections, even for a high signal count package, and power and ground bumps can be used to surround sensitive I/O bumps. With wire bonding, the number of pads is limited by the outer perimeter, so a high signal count package leaves very little room for power/ground connections and necessitates fewer and longer current return paths.

The use of solder bumps rather than wires greatly reduces parasitic inductance, since bumps represent much shorter and thicker connections than wires (**Figure 3**). The length of bond wires also greatly increases the susceptibility to crosstalk and imposes slew rate limits on the signal. Using a ball grid array (BGA) package allows the signal and ground connections to be interspersed in a 'chequerboard' arrangement to effectively shield the signal lines from interfering with each other.

### Clock generation

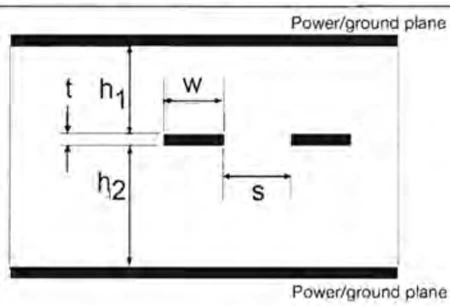
Clock generation circuitry requires particularly careful attention to detail, especially in terms of layout, proper termination and the judicious use of EMI filtering components. The impedance of the traces must also be controlled to avoid unwanted reflections. Improper application of these principles can result in clock generators becoming noise generators. Clock generation and buffering can also lead to unnecessary noise, because of the increased design complexity and the introduction of routing voids in the power and ground planes.

### Cables and connectors

Only cables and connectors specifically designed for high frequency and gigabit Ethernet applications should be used for connecting high bit-rate systems. Use of inappropriate, unshielded or poorly matched cabling can cause unwanted reflections and pick up interference in a similar way to that described for on-board discontinuities. Proprietary types of cable for these applications are available from a variety of manufacturers including Tyco Electronics, Molex and WL Gore.

### Transmission line

The impedance requirements of the serial RapidIO interface are 100Ω. In order to maintain this consistent differential impedance, the options for the construction of the transmission line are limited to either stripline or microstrip. Microstrip is used when the signalling must be routed on an outer layer of the board, while stripline allows the signalling to be




$$Zo = \frac{60}{\sqrt{\varepsilon_r}} \times \ln\left(\frac{1.9(2(h1+h2)+t)}{0.67\pi(0.8w+t)}\right)$$

$$Zdiff = 2 \times Zo\left(1 - 0.374\, e^{-2.9\left[\frac{s}{h1+h2}\right]}\right)$$

Figure 4 (Left): Recommended edge-coupled differential stripline configuration, showing equations for single-ended impedance $Z_0$ and differential impedance $Z_{diff}$

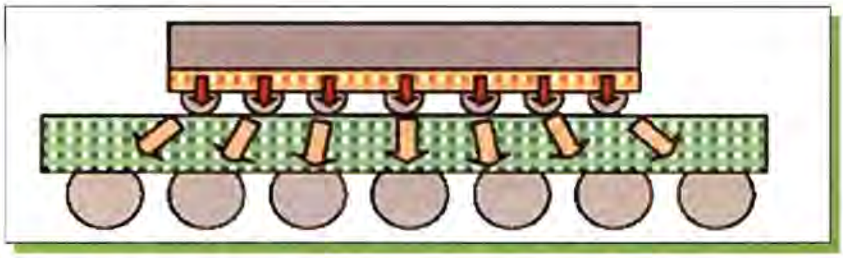


Figure 3: Flipchip ball-grid array (BGA) packaging gives much lower parastics than wire bonding

placed on an inner layer where shielding by adjacent power and ground planes is possible. Edge-coupled differential (or co-planar) stripline, rather than a broadside coupled or dual stripline, is recommended. Edge-coupled differential stripline is shown in **Figure 4**, along with the equations for single-ended and differential impedance. The stripline is symmetrical when h1 = h2. The minimum recommended layer count is six layers and the optimum design has 16 layers.

The signal return path is particularly important and is defined as the route that current takes to return to its source. This may be through ground planes, power planes, other signal paths and through ICs. The current always takes the path of least resistance. A simple way to evaluate the integrity of the return path is to draw a loop tracing the current from the driver through the signal conductor to the receiver – the smaller the area of the loop, the lower will be the parasitic inductance.

**The following design rules apply to all return paths:**

- Always trace out the return current path and provide as much care to the return path as the path of the signal conductors.
- Do not route impedance-controlled signals over splits in the reference planes.
- Do not route signals on the reference planes.
- Do not make signal layer changes that force the return path to make a reference plane change.
- Decoupling capacitors do not adequately compensate for a plane split.
- Do not route over via anti-pads or socket anti-pads.

**If reference plane changes must be made, try to follow the following recommendations:**

- Change from a VSS reference plane to another VSS reference plane and place a via connecting the two planes as close as possible to the signal via. This also applies when making a reference plane change from one VCC plane to another VCC plane.
- For symmetric stripline, provide return path vias for both VSS and VCC.
- Do not switch the reference plane of a signal from VCC to VSS or vice versa.

Guard traces – tracks that run parallel to a signal trace and are connected to the reference plane – may be used to minimise crosstalk, but they do take up board space and will be required to be 'stitched', or connected with vias, to the reference plane at intervals that prevent resonance.

Due to the high frequency content of the serial RapidIO signals, it is necessary to minimise the discontinuities imposed by crossing ground and power planes when it is necessary to transition to different signal layers. The use of a controlled impedance via is desirable. The design of these vias is a complex topic in its own right, and more detailed information can easily be found. Again, the basic principle is to keep the signal path down to a minimum and to ensure that signals travel through the via rather than across it.

### Summary

With some forethought and a knowledge of the basic design rules, it is possible to apply high frequency interconnects such as RapidIO to a system without encountering any of the problems that are traditionally associated with poor signal integrity, such as noise, transient effects or crosstalk and jitter. If traces and signal paths are kept as short as possible and are either shielded by ground planes or kept physically separate from each other, and if care is taken to avoid mismatched impedances or any configuration likely to support resonance, good signal integrity is easily achievable.

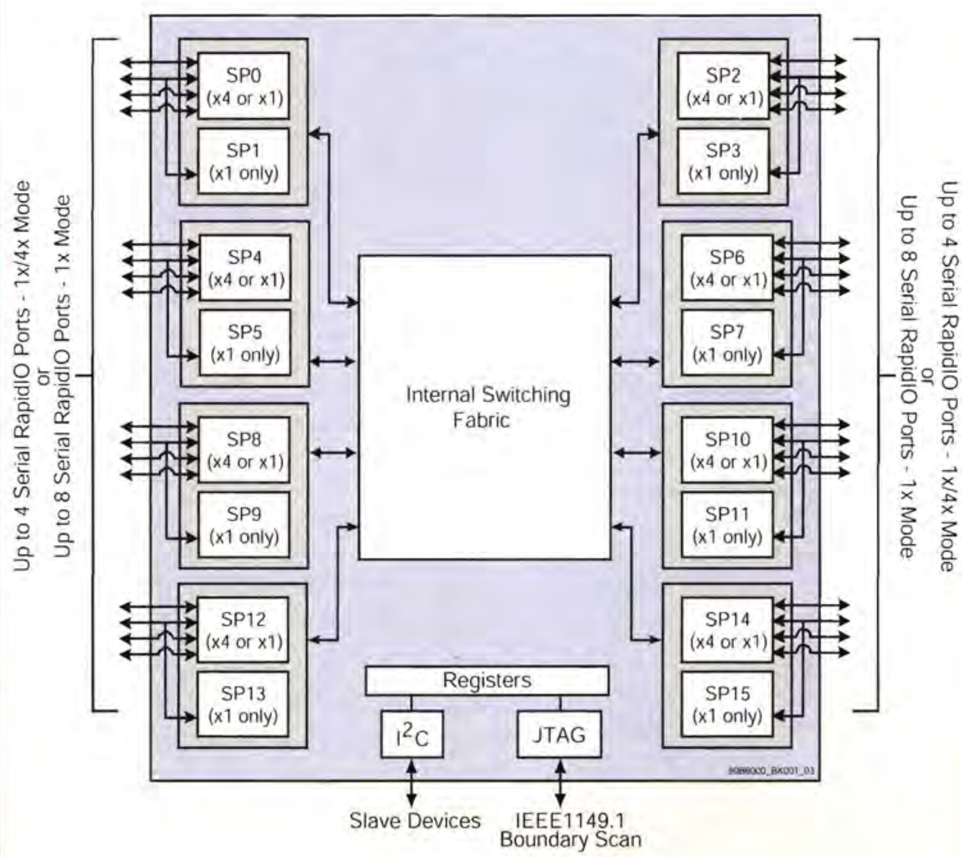
The moral of the story? It is always simpler to avoid signal integrity problems in the first place – by creating a well thought-out design verified by simulation – than to try and correct signal integrity issues in a problematic design.

## 16-port serial switch

RapidIO is a point-to-point, packet-switched interconnect protocol designed to meet the needs of current and future embedded applications. A standards-based, high performance 16-port serial RapidIO switch is available from Tundra. This is the Tsi568A device. The switch can be used to provide a high-speed RapidIO interconnect between processors, bridges, remote memories, or data plane processing elements in embedded applications. The block diagram on the right shows the main components of the device.

Typical applications for the switch are in wireless embedded communications (Node B, radio network controllers and media gateways).

The Tsi568A has been specifically designed to facilitate the highest possible standards of signal integrity and, to this end, includes features such as a low noise logic core as well as a high performance flipchip BGA package. In line with the principles described above, the switch also features adjustable drive current per x4 port and adjustable de-emphasis per x4 port.




Block diagram of Tsi568A serial RapidIO switch interfaces

What's wrong with the PC's form-factor and how can this be helped with PCI Express, asks Dan Jensen from Texas Instruments


# PCI Ex

# Enabling the s

During the past several years, the PC has found itself at the heart of many people's homes, moving from the den or office and into the kitchen, or living room. As the PC becomes commonplace in living spaces, consumers have demanded changes to traditional desktop systems. Changing mechanical form-factors allow the PC to complement living environments, as well as fit it into smaller, more aesthetically pleasing designs.

One fundamental problem with classic desktop towers is the desire to hide the large chassis, yet maintain convenient user access for high-performance I/Os at the table-top. These I/Os include CD and DVD drives, USB and 1394 ports, Flash media card readers and other interfaces. To further complicate the ergonomic problem of system accessibility, how often do users find themselves under their desk with a flashlight trying to find that last spare USB port? These ergonomic challenges have existed for years and consumers are looking for their solutions.

Although potential solutions have surfaced, none have done an adequate job of truly solving the problems without sacrificing the ability for full expansion and upgradeability. With many solutions to date, users trade off performance, as seen with many of the "all-in-one" systems typically targeted at the ultra cost-sensitive markets.

## An evolution is taking place

So, what's currently available to address these problems? Presently, an evolution from the system bus from PCI to PCI Express is under way. Today, a large percentage of desktops and notebooks are shipping with PCI Express support. PCI Express is a low voltage, differential, low pin-count serialised bus, which began replacing the PCI bus late last year.

The advantage of PCI Express is that it provides three to four times the performance of a traditional PCI bus. In the x1 form-factor, PCI Express only requires four pins plus a clock input, versus the minimum of 47 pins required for a PCI bus. In addition, the electrical characteristics of PCI Express allow it to extend beyond the system board and desktop chassis by operating over several feet of low-cost cable. For the first time, this feature will let the I/O system bus to extend outside of the PC platform, enabling OEMs to separate the system's I/O components from the processor, chipset, graphics and memory subsystems.

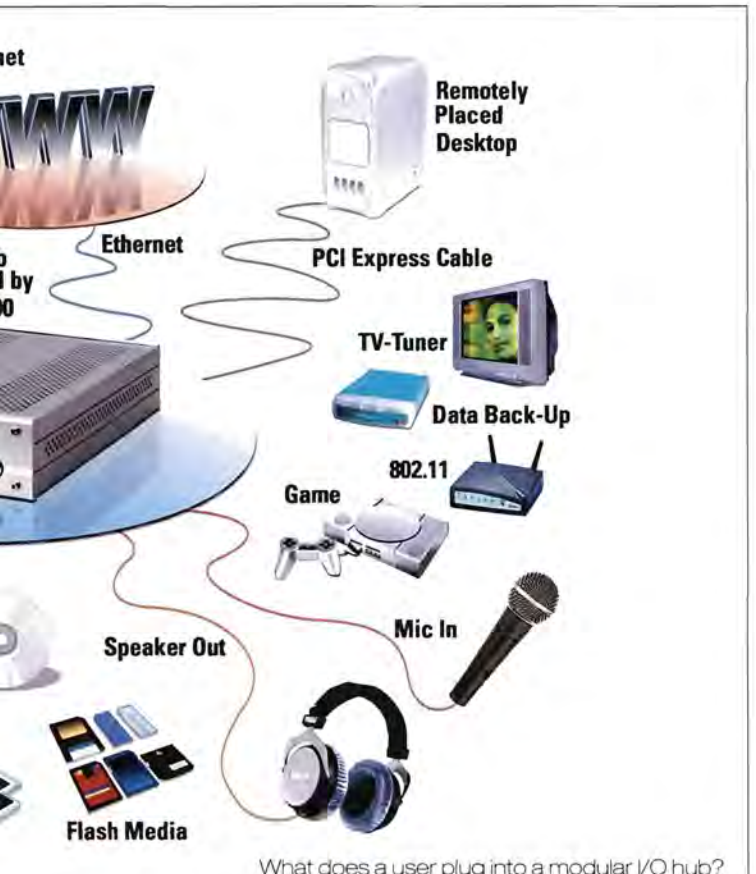
The ability to cable PCI Express outside of the standard desktop chassis allows OEMs to move the user I/O interfaces (CD, DVD, USB, 1394, Flash media etc.) to the table-top in a modular I/O hub, while placing the system tower several feet away, even within a cabinet. In this example, after performing the initial installation, there's no need to access the system tower on a regular basis.


Today's "desktop" PC – an ergonimic mess

With cabled PCI Express, performance or expansion options are not limited. In addition, by extending the primary system bus, all of the software developments are also preserved instead of the solution to migrate to a different I/O bus, like USB 2.0 or 1394.

The split-chassis desktop also helps alleviate fears of obsolescence by providing ways to upgrade targeted hardware individually (modular I/O hub versus system tower). This flexibility allows users to upgrade sub-portions of their computing system instead of the entire platform, which proves less costly.

Split-chassis desktop systems are expected to follow multiple implementation paths. In the simplest form, the desktop is simply split into two pieces. The



What does a user plug into a modular I/O hub?

# press:
# lit-chassis PC


Split-chassis desktop

PCTe/CAT5/Fiber/others

Modular Hub

Main computer

modular I/O hub is placed at the table-top surface with the monitor, keyboard and mouse, while the system tower is hidden several feet away. In a second configuration, OEMs are expected to integrate the modular I/O hub with the PC monitor to provide even less desktop clutter.

Finally, the similarities between the modular I/O hub and the requirements of notebook docking should be highlighted. Their similarities in functionality lend themselves to allowing docking stations to migrate toward the same type of concept as a split-chassis modular I/O hub.

## Momentum update

As with all new technology initiatives, it's challenging for some companies to determine at what point to begin investing and at what point will the market successfully accept a new technology. One company has taken the concept of a split-chassis PC to a greater level with its product line, by using fibre optics as the transmission media between the processing tower and the modular I/O hub. This product provides a solution that separates the two PC components by a much greater distance (hundreds of meters) than a solution using low-cost cable (less than 7m).

The challenge of overcoming initial market momentum for the split-chassis PC concept comes from a variety of different sources. These include market adoption of the PCI Express bus standard, an industry standardised cable and connector scheme, the overall system cost concerns and signal integrity issues. One important aspect to enabling split-chassis adoption is the PC systems adopting the new PCI Express bus standard. To that end, desktop systems began shipping last year that supported this new standard. Early this year, mobile platforms began shipping in volume.

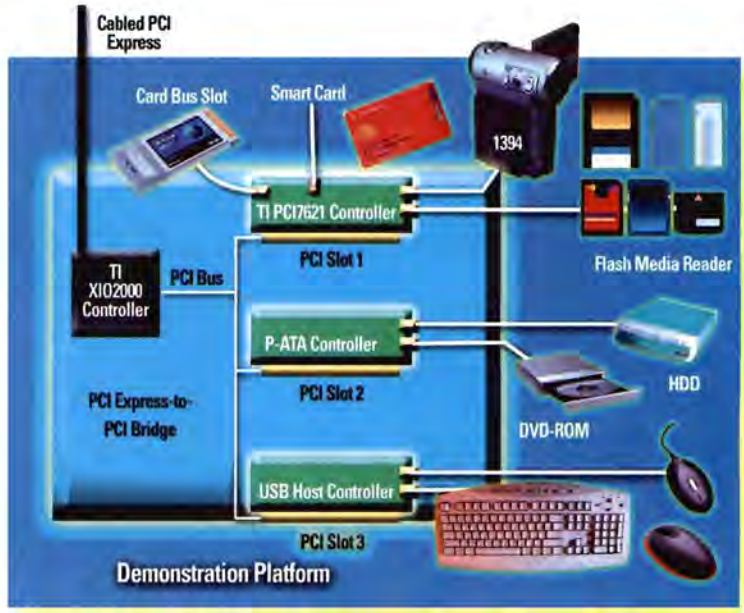
Market momentum and adoption of PCI Express is progressing very rapidly. Analysis of PC chipset roadmaps reveals that all chipsets planned in the near future add support for PCI Express. At this stage of the market, the time it takes for PCI Express to reach 100% adoption is related to the life-cycle of older chipsets. The support of a split-chassis PC system based upon PCI Express, therefore, must follow the adoption of PCI Express. But, at this point in time, PCI Express adoption is no longer seen as a barrier to split-chassis PC adoption.

## Standardised cable and connector

A significant barrier to the split-chassis PC concept adoption is the preference from most customers that a standard cable and connector solution must be adopted by the industry. Although proprietary solutions will begin shipping before a standard cable and connector solution is determined, the broad market adoption of split-chassis PCs will follow the release of a standardised cable and connector.

The PCI SIG (Special Interest Group) organisation (www.pcisig.com), which released the PCI Express specification, also established a Cable Working Group in late 2003. This group is chartered with the development of an industry standard cable and connector scheme specification. The organisation is progressing well and should soon define a standard connector and cable for PCI Express.

TI modular I/O hub demonstration




Block diagram of cabled PCI Express enabled split-chassis or docking station

Cables and connectors from cable manufacturers are expected to follow very soon after the release of the cable specification, if not concurrently. Many customers interested in the split-chassis PC concept are timing product releases, following the availability of the standard PCI Express cable and connector.

An alternative method to provide a PCI Express connection to the platform is via an ExpressCard with an attached cable. The ExpressCard standard, released by the PCMCIA (Personal Computer Memory Card International Association) organisation (www.pcmcia.com) is a credit-card sized technology for the expansion of a platform via either PCI Express or USB. Laptop platforms have already begun shipping from vendors supporting an ExpressCard slot. This solution allows modular IO hub manufacturers the option of providing a cable with an ExpressCard at one end for connection to the platform. However, concerns over the use of an ExpressCard are the difficulty in meeting PCI Express "jitter", as well as loss system budgets over multiple connectors, cables and FR4 board traces.

## Signal integrity

In order for cabled PCI Express to gain mass adoption, system designers must follow guidelines to ensure that the "jitter and loss" budgets for PCI Express can be met. The PCI Express signal leaves the transmitter I/O in a chip through a package onto the system board across FR4 board traces to a cable connector. The signal then traverses the cable to the other end, across a second cable connector, finally through an additional FR4 board trace to reach the receiving chip's I/O.

If the "jitter and loss" of the signal through the transmission medium degrades beyond the budget allotted, then there is no guarantee that the receiver I/O can "capture" and properly decode the information in the signal. The chip's ability to properly receive signals is a function of: the transmission media (board trace, connectors, cable); the quality of the data clock signal; and the performance of the receiver's I/O technology. This means that the quality of the PCI Express receiver I/O is an important part of the cabled PCI Express solution. To aid in receiving signals properly, a repeater chip or a PCI Express switch device can be used to improve performance.

## Overall cost for split-chassis systems

One concern for all customers considering the split-chassis PC concept is related to the cost-effectiveness of the desktop system. As one might expect, the separation of a platform into two physical components is not expected to reduce the total system cost, at least for the near-term. The question is difficult at this point to determine exactly how much additional cost is incurred by a split-chassis product but, regardless, the point that makes split-chassis viable is the fact that it also provides additional value to the end user. As always, users will make decisions that are based on both a product's cost and appeal. Clearly, the LCD monitor trends during the past few years show that consumers will pay for features they value.

The initial deployment of most split-chassis types of systems will more likely be a full desktop tower with a PCI Express cable port. The end user then makes the decision to purchase the additional modular I/O hub for the functionality and versatility it provides. This change adds very little additional cost to the desktop tower (the cost of a PCI Express cable connector). The added system cost will then be contained in the modular I/O hub, which users can either choose to purchase or not.

A major customer concern is the additional cost to any existing platform, since the PC desktop market is extremely cost sensitive. This deployment option helps address the primary concern of not adding significant cost to the base platform, yet providing much of the split-chassis PC's functionality and ergonomic benefits. As users become more interested in such systems, base platforms can potentially be cost-reduced and targeted directly at specific market segments.

The number of applications for cabled PCI Express is also growing as customers evaluate how cabled PCI Express can solve real problems within their systems. Not only will the concept of a split-chassis PC drive the adoption of cabled PCI Express, but additional market demand will drive the adoption higher. Advanced high-performance peripherals (such as a PVR, Blu-Ray DVD, RAID, TV tuners, etc) will generate additional demand for cabled PCI Express ports.

**PCI Express availability**

The key enablers behind split-chassis platforms are developing nicely. Cables, connectors and key silicon components will become readily available this year to support the concept of a split-chassis PC. PCI Express-to-PCI bridge silicon solutions are considered a critical component for the modular I/O hub at this point. They enable the use of high volume, low cost, PCI-based silicon solutions within the modular I/O hub. With this implementation, the PCI Express-to-PCI bridge serves as the link between the cabled PCI Express fabric and the low-cost PCI silicon. Texas Instruments (TI) demonstrated an example of such a platform at the 2004 Windows Hardware Engineering Conference in Seattle, US. A second generation modular I/O hub was demonstrated at 2005 Intel Developers Forum (IDF) in March.

TI's modular I/O hub circuit card


The IDF product demonstration supported a concept modular I/O hub that measured approximately 7x10x2 inches. This version of a modular I/O hub supported a DVD-ROM drive, a secondary hard disk drive, two 1394a ports (one front/one back), four USB 2.0 ports (two front/two back), a 7-in-1 Flash media reader (SD/SDIO/MMC/MS/MS-Pro/SM/xD picture card), one CardBus/Compact Flash socket and an onboard audio controller.

Looking ahead, there may be no limits where engineering and technology will take users and the PC market. For certain, the PC form-factor is changing drastically and this is becoming one of the key differentiators for new product concepts.

The capabilities behind cabled PCI Express simply provide a new technology tool for companies to continue to innovate around the mechanical form-factors of PCs. As in the recent past, companies that embrace this innovation are likely to be the one's enjoying success over the next few years.

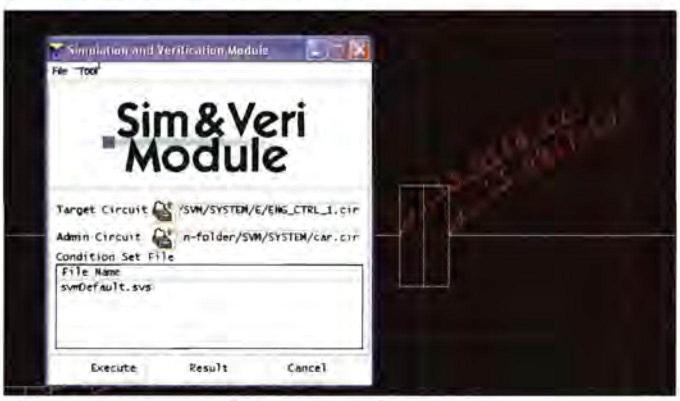
# Basic design flow for vehicle wire harness design

Early and frequent simulation and DRC improves wire harness quality and design productivity, says **Nick Jay**, Applications Engineer at Zuken

Vehicle electronic systems are now immensely complicated and a typical wire harness will contain upwards of 2500 interconnects, with the number rising with each new model. Traditional methods of designing harnesses, even using simple CAD tools, are no longer sufficient to ensure right-first-time outcomes. In addition, the further down the development path a project goes, the more time-consuming and expensive it becomes to correct errors.

In order to detect potential errors as early as possible, two main strategies need to be adopted: regular simulation of the design and frequent design rule checking (DRC). Sophisticated EDA tools are now available to make these processes easier and more automated for engineers and designers. This article looks at these two vital aspects of vehicle wire harness design and references.

## Simulation and verification




Simulation and verification module voltage display

A simulation and verification module within an EDA suite is the engineering tool that is used to make sure that the system conforms to the power and loading of the vehicle, and that cable sizes, weight – and hence costs – are as low as possible. It is also a check that the circuit functions as it should. Unlike simulation in electronics circuits containing active components, this is not about checking rising edges and electronic signals; it's checking basic electrical parameters, such as current and voltage plus related factors such as wire resistance and temperature.

Best practice is to simulate early and simulate often, even though the complete system cannot be simulated in the early stages of the design because it's not yet complete. In wire harness design, various parts of a circuit are simulated individually and as the design progresses, ever larger sections are simulated until it is possible to simulate and verify the complete design. A great deal of simulation is carried out with respect to load charts that define the maximum current on any given pin at a given state i.e. various contacts being open or closed. When the design is progressing successfully, simulations will bring up fewer errors the further along the design flow the harness has been developed.

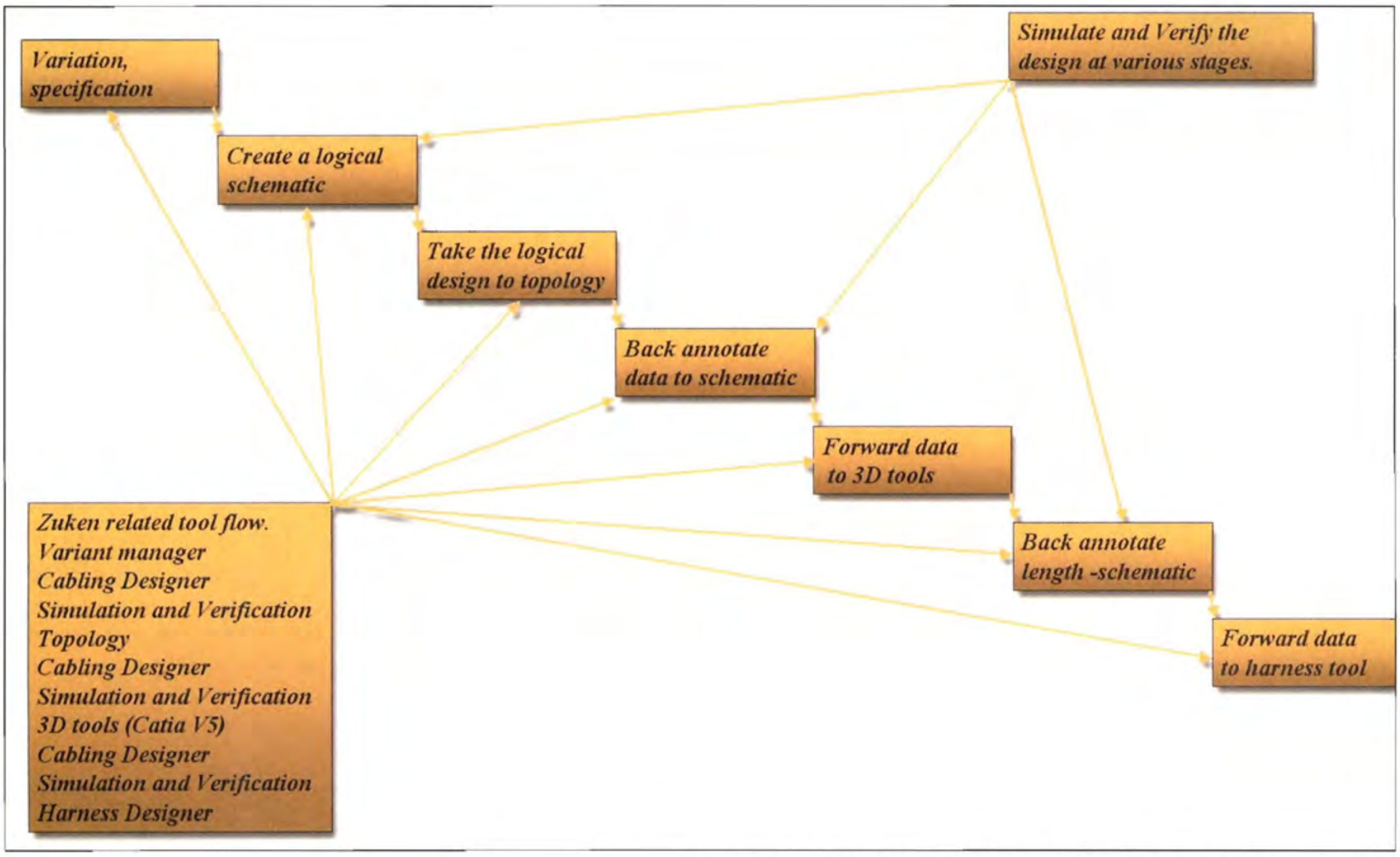
Before running any simulations, a resource file is created within the EDA tool where the attributes and component electrical characteristics are entered. This is normally changed very rarely, a single resource file often being used for many vehicles over an extended period. Ambient temperature will be defined within the resource file on a unit-by-unit basis for the various circuit units within the vehicle; a unit above the engine block is not going to be at the same ambient temperature as a control box behind a door panel.

In Zuken's CR-5000 tool suite, a separate resources file covers the basic physical properties of the cables in the harnesses, such as nominal temperatures, materials properties, copper and aluminium properties, as well as others.

## What attributes simulation addresses

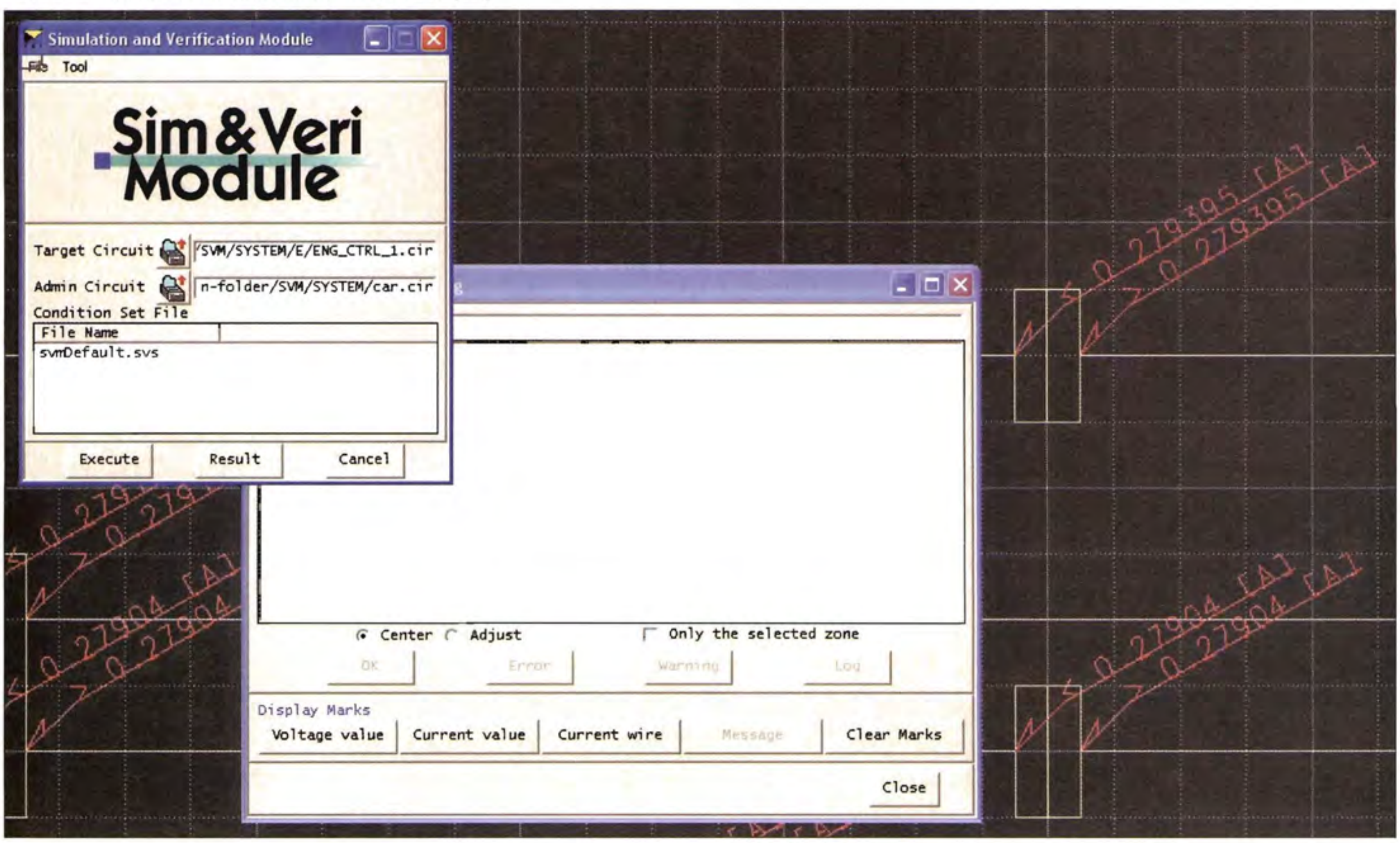
Simulation and verification encompass the following:

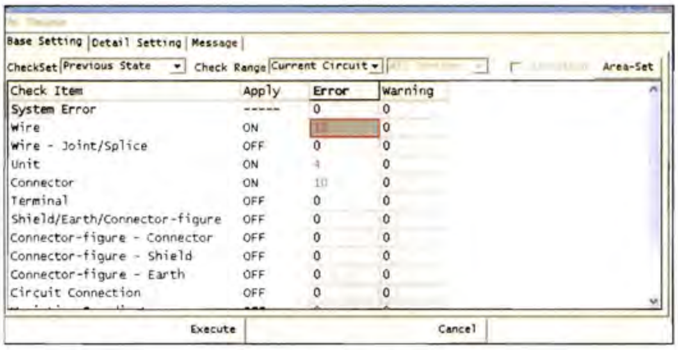
- **Wire operation temperature**: checking both ambient ratings for the unit and conductor sizes needed to maintain the temperature within limits.
- **Wire allowable current**: engineers try to minimise wire sizes to keep down weight and cost, so checks are needed to ensure that this process hasn't been taken too far.
- **Fuse load factor** with respect to both continuous and peak ratings.
- **Fuse rated current**.
- **Wire size vs. fusing**: to make sure that wire sizes and fuse ratings are compatible.
- **Fuse wire matching check**: to make sure that wires do not deteriorate with long term use before the fuse blows – a predetermined threshold rating is set in the resource file.
- **Wire allowable length**: longer wires have higher resistance. This check can only be made after the design has been created in the 3D mechanical CAD tool (typically CATIA).
- **Wire fire point**: is this compatible with the temperatures likely to be encountered.
- **Load terminal voltage check**: to make sure there isn't too




Logical tool design flow showing where the design should be simulated

Simulation and verification module current display






Design rule checker (DRC) output showing errors

much voltage drop along the harness to each terminal.

➢ **Connector current check** based on connector data entered into the resource file.

➢ **Switch current check**.

➢ **Relay current check**.

➢ **Load pin wrap around check**: if there is a fault that causes a reverse current, this check is designed to ensure that it will not reach another part of the circuit by making sure that any fault is isolated at the load pin.

## When to simulate

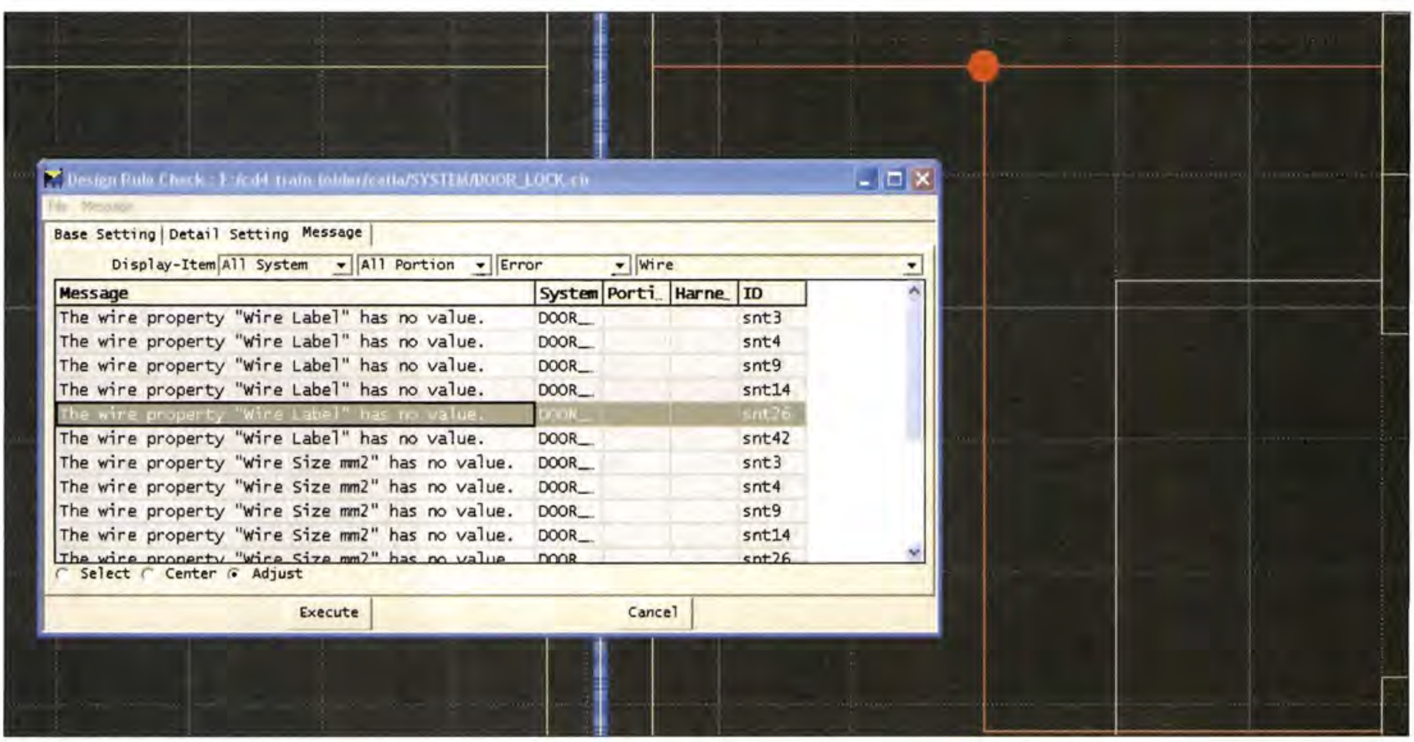
The engineer will normally create a manual drawing of the harness design, complete with variants, on paper. This drawing is then passed to a designer who will create a point-to-point logical circuit of wires and blocks, each with some attributes. The engineer will carry out a first simulation at this point, primarily for circuit integrity, to check that the design matches what was originally drawn. It's also useful to simulate on/off states and check for 'sneak paths' – unintentional paths to ground – at this stage. For example, sneak paths occur if there are three relays and all connections have not been analysed in all conditions, then an unintentional path to ground can be created. At this stage, there is no consideration of connectors but it is important to simulate every possible scenario with respect to the on/off states of various switches and connectors.

The next step is to take the design into a 2.5D topology tool. Here, the designer will add harness breaks and connectors, for example where a door opens. The design is then back-annotated into the original schematic and the individual unit connectors are added. At this point we have a hybrid physical/electrical schematic. It is important to simulate and verify here to make sure that the right gauges of wires are going into the connectors to avoid overloads. By this stage, a lot of the physical attributes have been built up, including wire gauge and colour, and which pins are going to be used for each circuit. The most important thing that's not known at this point is the length of each wire. This is determined when the design is imported into the 3D mechanical CAD tool, such as CATIA V5. Here, wire lengths are established and the design is simulated again to ensure that maximum lengths are not exceeded.

## Design rule checking (DRC)

DRC is a designer's tool that's used to ensure that the design conforms to engineering practices. For example, that the right size of terminal is used for a given wire size and so on. The process is, therefore, primarily checking the manufacturability of the circuit.

Within the EDA tool, the DRC function will have its own




Cross probing from the design rule checker (DRC) highlighting a circuit error checking resource file. Design rule checks are entered into the tool in a simple spreadsheet format. As with simulation and verification, carrying out DRC early and often is best practice. The design must be 100% compliant with the check file at the end of the design or the harness will be either impossible to manufacture or not suited to the purpose for which it was designed. Checks can be carried out on a specific schematic block or via an administration circuit that shows all the circuits to be checked as interconnected blocks at the top-level of the design hierarchy. In Zuken's CR-5000 tool suite, simply clicking on individual blocks in the top level view shows the individual circuit within that block, which can then be checked in detail.

In setting up a DRC run, users can choose to apply or omit individual checks. They can also set the individual checks so that non-compliance is reported as either an error or a warning. An error is totally unacceptable to the design. A warning is something that needs further investigation but is not necessarily a design fault. For example, the physical name of more than one wire will be 'ground'; it is not usually a problem, but could be, so it needs checking.

Design rule checks for vehicle wire harnesses typically include the following:

➢ **Wires**: checks will cover labelling, wire size, colour, the correct wire end connections and identification of label duplicates. In addition to the basic set of rules, customised setting, such as wire clearance, may need to be set.

➢ **Wire joints and splices, loops and T-branching** to ensure that, for example, the number of T-branches permissible in a given wire run is not exceeded.

➢ **Units**: checks to ensure that unit names have been set, pin numbers and part names are set, and group identification (ID) is set for instances where different parts of a unit may appear in different places on a schematic – group ID ties them together.

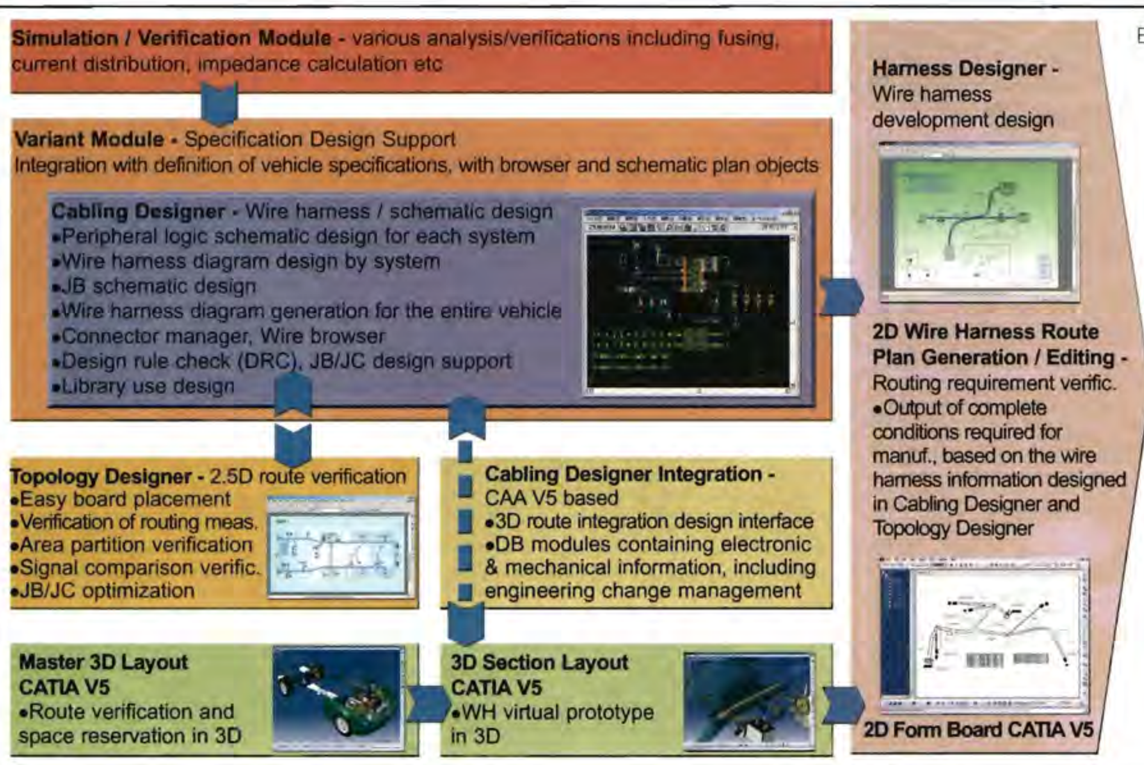
➢ **Connectors**: group ID set, correct gender allocated, terminals, shields, earths and coordinates.

Again, with respect to the Zuken tools, the user can choose to display errors within an individual harness, or for all harnesses together. DRC errors are highlighted in red on a tool's check table, together with a detailed description of each error. Double clicking on the error description causes it to be highlighted in the schematic on the centre of the computer screen, enabling rapid identification and correction. Furthermore, all errors and warnings are held in a text file that can be printed out for review. Each time DRC is run, the text file is overwritten with the latest errors in the design.

## Conclusion

The complexity of modern wire harnesses in all kinds of vehicles is only going to grow. Some 2500 interconnects per vehicle may well rise to 5000 over the next 10 years. Vehicle manufacturers are under the same time-to-market pressures as other makers of consumer goods and anything that can accelerate the design process, whilst improving product quality along the way, is going to deliver significant competitive advantage.

Dedicated wire harness design EDA tools that enable harnesses to be simulated and checked against pre-defined design rules from the earliest schematics through to fully modelled 3D layouts can make a valuable contribution in this respect.




Basic design flow for a wire harness design

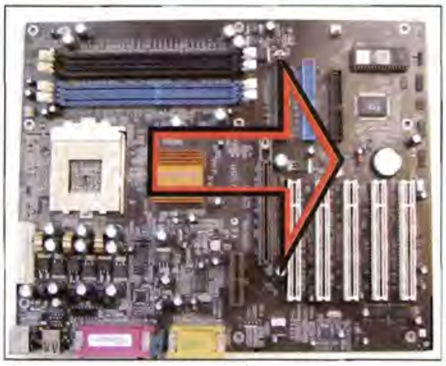
# How to: re-assemble a PC

Having dismantled a PC in last month's issue, Boris Sedacca now invites readers to put one back together

In the opposite photograph is the case and below that is the power supply. Top right are the IDE cables for the hard disk and CD drives, and the diskette cable.

Then working down from there are the CPU and heatsink/fan assembly, the AGP card, 256MB memory and motherboard. Bottom right is the CD writer, on top of which is the 80GB hard disk, and above them is the diskette drive.

The first thing to do is to clear the CMOS memory on the motherboard, usually by temporarily shifting the position of a jumper and then replacing it (shown by the arrow) in its original position. In the case of the Elite K7S5A motherboard shown below, this jumper is designated JP4 and is located to the left of the battery, which is the size of a 10p coin.



Arrow shows location of jumper

If I were working with a mini tower case, I would have to screw down the motherboard and put in the CPU, fan and other components before mounting the power supply.

The elements needed to put the PC together

In this case I am using a midi tower, which allows me to mount the power supply first and still gives me bags of room to work. There's also less need for using flexible screwdriver extensions. The power supply is secured to the case with four screws as shown on the right.

A PC case will typically come with punch-outs for the various motherboard connectors, which are shown to the right of the power supply. Make sure that you punch out all the required holes for your motherboard before attempting to fit it into the case.

The motherboard is secured to the case by pushing mounting screws through-holes in the motherboard and screwing them into standoffs, which will need to be aligned with these holes.

As I am using the same motherboard, I have left the standoffs where they were. Two of them can be seen: one just to the right of the power supply, the other at the right of the photo (follow the arrows).

Arrows show standoffs

Next, place the motherboard so that its connecters go through the punch-outs comfortably. This is easy with the Elite K7S5A, but more difficult with some motherboard manufacturers.

Here, I am using all nine standoffs and motherboard mounting screws provided. This helps as the motherboard tends to move about when the CPU, memory cards and various connectors are pushed in. Once the motherboard is secured to the case you can drop in the CPU, memory and assorted cards. First, remember to pull the lever up on the zero insertion force (ZIF) socket. Please refer to last month for photos.

Remember that there is a hole missing on two of the corners of the socket, which makes it impossible to fit the CPU the wrong way around. Once the CPU is in its socket, remember to return the lever to the lock position, as shown below.

You should also remember to use a small blob of thermal paste on the CPU before securing the heatsink/fan assembly with the spring lever. I always find it easier

Arrow shows CPU lever is in lock position

replacing an assembly than removing it. Do not forget to push the CPU fan connector into its socket on the motherboard. I did forget once and 'cooked' a perfectly good CPU: that 60 pounds down the drain.

Next, push the memory into its socket and secure it with the levers at both ends. Then, insert the AGP card into its slot and secure it to the case with a screw as shown in the photo below. On the K7S5A motherboard, the AGP socket has an additional lever for securing and releasing the AGP card.

The tricky part is connecting the cables. Here you will have to refer to the motherboard manual for specific details. The connectors for the K7S5A are shown in the photo below.

Arrow pointing at the AGP card

The most important convention to observe on most connections is that of the black or white cables going into the earth or ground or negative (-) pins, while just about any other colour will signify a power, signal or positive (+) pins.

The easiest is the speaker connector, shown at the bottom on the right, and designated SPK1.

Nowadays, the case speaker does little more than beep when the machine starts up. Many motherboards will have on-board sound, as this one does, or if they do not, they should have sufficient PCI slots for a sound card.

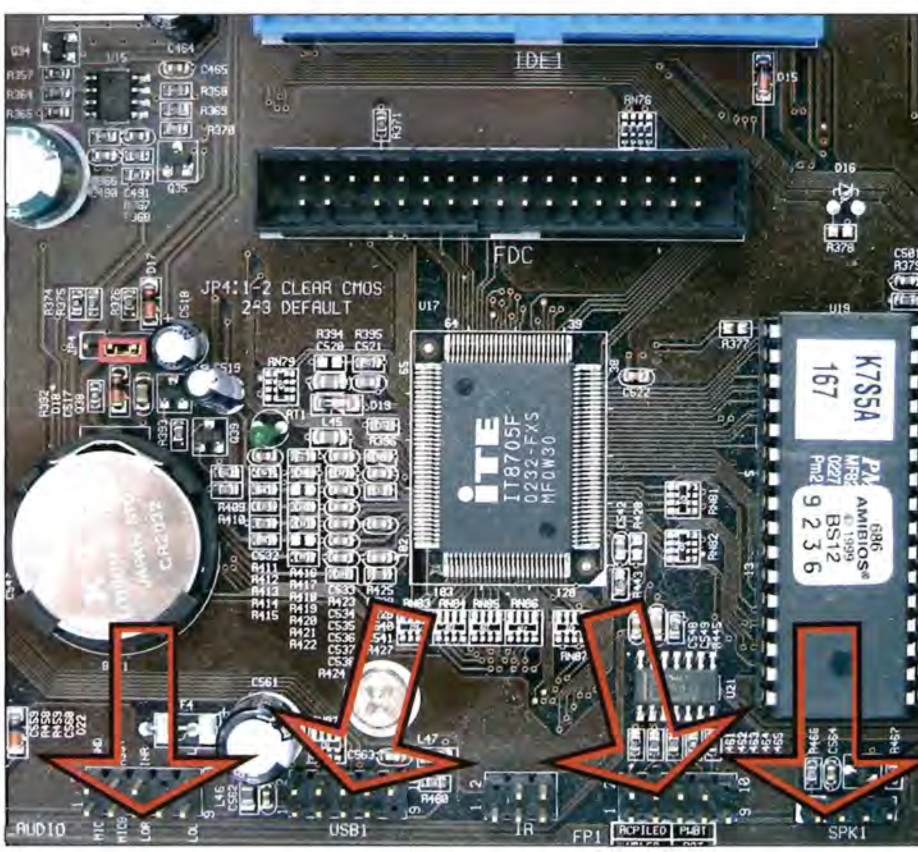
To the left of the speaker connector is the socket for the case's main front panel components, designated FP1. Now you have to take care! What you need to connect are the power on-off switch, reset switch and hard disk LED.

You will see that the pins are numbered 1-10. The K7S5A manual states that pins 1 and 3 are for the hard disk LED, with pin 1 being positive. It is important to observe the correct polarity here, as an LED will not work otherwise.

Pins 2 and 4 are for the power switch, while either pins 5 and 7 or 6 and 8 can be used for the reset switch. Polarity does not matter with the power and reset switches, which can be connected any way around.

The mnemonics used by the motherboard connectors will probably not match those used on the case connector shells exactly. The LED connector on the motherboard is designated HD LED, while on the case connector shell it says H.D.D. LED, which shouldn't cause too much of a problem, but sometimes it might not be as obvious with other motherboard-to-case connections.

The K7S5A provides additional connectors for infrared port, front panel audio (which my case does not provide) and front panel USB (which it does). USB connection is fairly straightforward and this is a useful feature, so I have opted to use it. Next, connect the power connector from the power supply to the connector on the motherboard. This should also be straightforward.




Arrows show positions of audio, USB, front panel and speaker connectors

Then you need to mount the diskette, hard disk and CD drives into the case, making sure you secure them adequately with sufficient screws, particularly the CD drive, which as I explained last month, can cause a lot of vibrations.

Then connect the power supply sockets to the diskette, hard disk and CD drives. This should be fairly straightforward.

Finally, connect the diskette cable from the motherboard socket to the diskette, and the IDE cable from the motherboard socket to the hard disk and CD drives. The photo on the right shows all the completed connections.

Following that, you need to replace the side panels on the case. You are now ready to connect the external devices and cables, including the monitor screen, keyboard and mouse, and, finally, the IEC power cable into the power supply socket. Some power supplies may include a switch, which you will need to switch to the ON position, but this is not always provided because on ATX motherboards, the machine is switched on from the front panel ON/OFF switch.

That's it. Now you can switch on. Good luck!

Re-assembled PC

# When is a radio not a radio?

**By Mike Brookes**

Currently, Project Team PT 43 of the European Communications Committee (ECC) is deliberating on a *"Strategy for the Future of Short Range Devices"* (SRDs) on behalf of the European Commission (EC).

It is vital for PT 43 to get it right in order for a strategy to be produced that will provide a climate of nourishment for successful development of the European SRD industry – the fastest growing of all radio market sectors.

The work of the Project Team, which comprises Radio Administrations and industry representatives involves revisiting current definitions of SRDs and has brought into sharp focus some consequences of selling radio spectrum piecemeal to the highest bidder.

From CEPT/ERC recommendation 70-03, the 'Bible' for the SRD industry in Europe, SRDs "in general operate in short bands and are not permitted to cause harmful interference to other radio services" and "cannot claim protection from interference caused by other radio services".

Originally, SRDs were designated to operate in ISM bands (Industrial, Scientific and Medical), themselves reserved for non-commercial use of radio frequency electromagnetic fields for industrial, scientific and medical purposes. This definition has clearly gone out of the window since radio LAN (local area network) services are now widely available in the 2.4GHz ISM band and are planned for the 5GHz band, which includes another piece of 'reserved' ISM spectrum. These are without doubt commercial services, operating in licence-free conditions, thus avoiding – so far – the Treasury's net for spectrum licences.

Because SRDs operate in shared bands without licence control, interference between different applications is almost inevitable. This has led to an explosion of technical innovations, which has resulted in the availability of low cost radio chipsets (<$5) that feature frequency agility, 'listen before talk', 'dynamic power adjustment' and other techniques to promote efficient spectrum use.

Such developments have led to the SRD industry saying "OK, we've produced super low cost interference-avoiding kit, so why can't we share other parts of the spectrum?" And here we meet the Treasury and purchasers of very expensive operating licences (mobile phone operators, broadcasters etc) head on. They have no intention of allowing SRDs into their patch on the basis that they have paid for sole use of their spectrum and the aggregate effect of millions of SRDs might raise the noise floor and damage their investments.

> *"A new definition of Ultra Low Power (ULP) SRDs is under consideration, but because their range and power is so low, it could be argued that they should not be considered as radio at all"*

On the other hand, the 'benefits' to EU member states of SRD development, while not providing revenue from spectrum sales, include building automation (inherently energy saving), new 'super' alarm systems, including video facilities that protect both property and people and RFID (tagging) which provides a whole raft of 'people services'. In addition, there is a new development in the use of SRDs for social and medical purposes. These include social alarms (to support sick and elderly people in unattended rooms), assistive listening devices and increasingly 'on-body monitors' and medical implants.

For these, a new definition of Ultra Low Power (ULP) SRDs is under consideration. Because the range and power of ULP devices is so low, it could be argued that they should not be considered as radio at all and thus be freed from radio regulations. After all, TVs and dishwashers emit electromagnetic radiation at very low levels and are not considered for radio regulation because they are not 'intentional radiators'. By contrast, medical implants and other ULP devices are intentional radiators and under the R&TTE Directive must be regulated as radios.

Freedom from Radio Regulations of ULPs would undoubtedly have major benefits in the medical world. However, mobile operators might view the prospect of millions of people radiating from ULP devices as further intrusion to their licences.

The ethical versus commercial battle to come will make interesting reading.

The Low Power Radio Association is a European trade body that represents manufacturers and users of short range devices (SRDs).

Mike Brookes is LPRA's chairman.

# Various PIC microcontroller families

### TIP 1: Low energy power supplies (all MCUs)

Designing the power supply for a low-power device can be very tricky. There are many considerations including:

1: Battery capacity
2: Internal battery resistance
3: Battery size
4: Battery cost
5: Battery weight
6: Voltage regulator minimum regulation voltage
7: Voltage regulator quiescent current

Batteries come in all shapes, sizes and chemistry. A small, high capacity battery typically has a higher internal resistance, so it is less useful for high-current applications. Batteries good for high current generally have lower capacity and higher weight than a similar sized high resistance battery. Examples are NiCd and NiMh. The NiMh battery is low in weight, high in capacity and small in size. However, it has a much higher internal resistance than the NiCd.

Rapid discharge of the NiMh will seriously decrease the life. The high internal resistance will not affect most low current applications, but if the application requires a burst of current, it is possible for the voltage to sag and the PICmicro MCU could reset.

Think of an RF transponder. Most of the time it is sitting idle, but upon demand, it must produce a powerful radio burst.

If VDD must be kept constant or the battery voltage is too large, a voltage regulator may be used in the application. If you add a voltage regulator, you increase the current consumption by the quiescent current of the regulator (the current used by the regulator to regulate).

### TIP 2: I/O device control (all MCUs)

When power consumption is crucial in an application, designers look for ways of saving as much power as possible. The most obvious way is to put the microcontroller to SLEEP when there is no need for it to be running.

Another solution is to clock the device at a lower frequency to consume less current. If there are other ICs on the PCB, it is possible to use an I/O pin to turn them off and on when they are not needed. Some of these ICs have a control pin dedicated for this (see Figure 1). If there is no dedicated control pin, the I/O pin can be tied to the VDD pin of the devices.

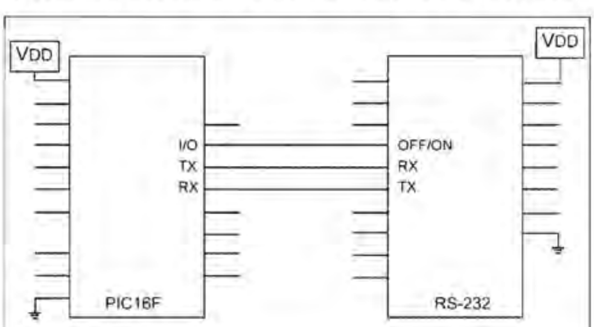



Figure 1

There are limitations to this. The device cannot draw more than the rated source current of the microcontroller I/O pin and must have a VDD requirement equal to the microcontroller's VDD. An alternative would be to tie an output pin to control a switch, which controls power to other devices.

### TIP 3: Low power Timer1 (PIC16 and PIC18 with nanoWatt)

Applications requiring Timer1 to have a clock crystal connected to its T1OSO and T1OSI pins must take PCB layout into consideration. The new low-power Timer1 consumes very little current, therefore making its oscillator circuit sensitive to neighbouring circuits.

To start, the oscillator circuit (including crystal and capacitors) should be located as close as possible to the microcontroller. Other than VDD and VSS, no other circuits should be passing through the oscillator boundaries. If it is unavoidable to have high-speed circuits around the oscillator circuit, then a guard ring should be placed around the oscillator ci cuit and microcontroller pins similar to that shown in Figure 2. It would also help to have the oscillator's circuit placed over a ground plane.

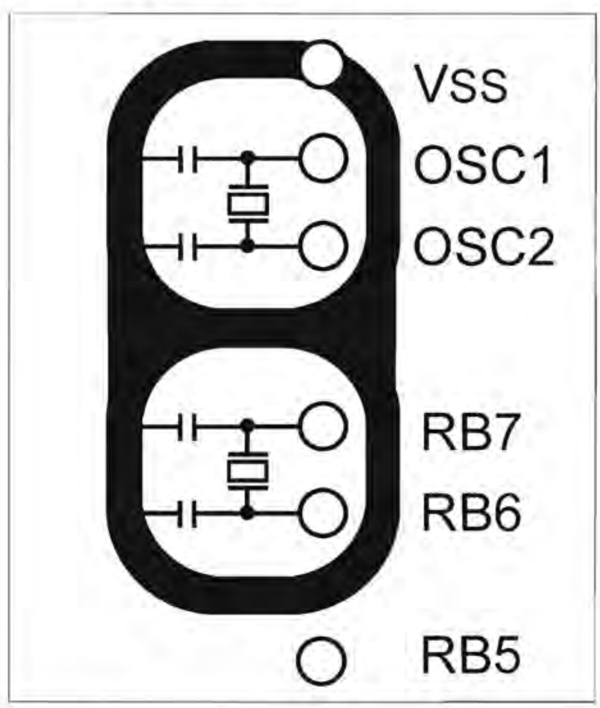



Figure 2

### TIP 4: Clock switching PIC16F dual clock (PIC16F62X)

The PIC16F62X devices are equipped with a second, low-speed internal oscillator. This oscillator is available when the device is operating from internal RC (INTRC), External RC* (EXTRC) or External Resistor** (ER) modes. It can be used to operate the microcontroller at low speeds for reduced power consumption. The actual speed of this oscillator is not calibrated, so expect 20% to 40% variability in the oscillator frequency.

To change oscillators, simply toggle bit 3 (OSCF) in the PCON register. If the bit is clear, the low-speed oscillator is used. If the bit is set, then the oscillator configured by the CONFIG bits is used.

** EXTRC mode only available on A parts.*

*** ER mode only available on the non-A parts.*

### TIP 5: Config port (all MCUs)

All PICmicro MCUs have bi-directional I/O pins. Some of these pins have analogue input capabilities. It is very important to pay attention to the signals applied to these pins so the least amount of power will be consumed.

#### Digital inputs:

A digital input pin consumes the least amount of power when the input voltage is near VDD or VSS. If the input voltage is near the midpoint between VDD and VSS, the transistors inside the PICmicro MCU are biased in a linear region and they will consume a significant amount of current. This current drain is most likely to occur if the application uses pin-overloading tricks, such as using a charging capacitor to read multiple switches or driving many LEDs from a few I/O pins. Sometimes, it may be better to reconfigure inputs to outputs to hold a known condition and minimise current.

#### Digital outputs:

There is no additional current consumed by a digital output pin other than the current going through the pin to power the external circuit. Pay close attention to the external circuits to minimise their current consumption. Pay special attention to any bias circuits or pull-up/down circuits that may be required.

#### Analogue inputs:

Analogue inputs are very high impedance so they consume very little current. They will consume less current than a digital input if the applied voltage would normally be centred between VDD and VSS. Sometimes, it is appropriate and possible to configure digital inputs as analogue inputs when the digital input must go to a low-power state.

Pay attention to the behavior of the pins and determine what the pin I/O state must be when entering and leaving each power mode. The wrong choice for one pin can cause a significant power increase and destroy the application.

### TIP 6: I/O initialisation (PIC16)

Although the following practice may seem routine, PORT I/O initialisation is overlooked many times. On a POR (Power-on Reset), the PORT registers (Ex. PORTB) have an unknown value. If the TRIS registers (Ex. TRISB) are configured before the PORT registers are set or cleared, unexpected code behaviour can result. The instruction sequence below is an example of how I/O initialisation should be handled:

```
banksel   PORTB      ;bank 0
clrf      PORTB      ;clear PORTB
banksel   TRISB      ;bank 1
clrf      TRISB      ;con. gure for outputs
```

### TIP 7: Two-speed start-up (PIC16 and PIC18 with nanoWatt)

This feature is new to the PIC microcontroller family and is available on some of the nanoWatt technology devices. Using the internal oscillator, it allows the user to execute code, while waiting for the Oscillator Start-up (OST) timer to expire (LP, XT or HS modes).

This feature is enabled through the IESO configuration bit. By the default setting of the OSCCON register, two-speed start-up will clock the device from the INTRC (32kHz) until the OST has expired. Switching to a faster internal oscillator frequency can optimise this feature. The example below shows several stages on how this can be achieved. The number of frequency changes is dependent upon the designer's discretion.

Assume a 20MHz crystal (HS mode) in the PIC18F example shown here:

| Tcy (Instruction Time) | Instruction |
|---|---|
| | org 0x05 ;RESET vector |
| 125µs @ 32kHz | bsf STATUS,RP0 ;bank1 |
| 125µs @ 32kHz | bsf OSCCON,IRCF2 ;switch to 1 MHz |
| 4µs @ 1MHz | bsf OSCCON,IRCF1 ;switch to 4 MHz |
| 1µs @ 4MHz | bsf OSCCON,IRCF0 ;switch to 8 MHz |
| 500ns | application code |
| 500ns | application code |
| ... | .... |
| .. | ... |
| (OST expires eventually, 20MHz crystal clocks the device) | |
| 200ns | application code |

# Win a PICkit2 Flash Starter kit


**Electronics World** is offering its readers the chance to win a new Microchip PICkit 2 Flash Starter Kit. The new PICkit 2 Flash Starter Kit enables engineers, students and anyone with an interest, to easily begin development and experimentation with PIC microcontrollers. The PICkit 2 follows the very successful PICkit 1 offering improved ease of use, faster programming and greater flexibility.

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### Short-Range Wireless Communication: Fundamentals of RF System design and application, second edition

**Alan Bensky**

*Elsevier (Newnes)*


This paperback comes with CD-ROM, which includes an electronic copy (PDF) of the book, an evaluation copy of Mathcad and Mathcad worksheets.

The book is a 352-page tome and, on its back cover, there is the suggestion that the CD represent 'The Complete Toolkit for the Hottest Area in RF/Wireless Design'. In a book of this size, this comment is somewhat ambitious, but what the book does do is to provide an insight into the technical and regulatory factors, which need to be considered by system implementers involved with SRDs (short range devices).

**Chapter 1** sets the scene for the rest of the book, providing an introduction and context for short-range radio, often referred to in the UK by the Ofcom term 'Short Range Device' or SRD. In Section 1.3, Characteristics of Short-Range Radio, typical features are mentioned, which define the scope of the book. It may be noted, however, that 'non-critical bandwidth specifications', which traditionally have been an SRD feature, are nowadays less acceptable, as more devices share a limited radio resource.

**Chapters 2 to 6** review basic technologies for SRDs, providing an introduction for engineers unfamiliar with radio practice. Chapter 2, Radio Propagation, gives a very brief introduction to propagation issues, including some that are not applicable to SRDs. The useful parts of this chapter are those references that introduce the concepts of path loss, multipath effects and fading. Maxwell's equations are included at the end of this chapter, though it is difficult to see why, and the web tutorial reference included here illustrates a common web reference problem, however, the link appears to no longer work.

**Chapter 3**, Antennas and Transmission Lines, is practical and includes most of the antenna types appropriate to SRDs, but surprisingly, includes only a brief reference to the inductance-loaded short vertical antenna, which many practical SRDs use. The Smith Chart is introduced in the section on impedance matching, with only a single example – and no reference, despite many excellent Smith Chart tutorials being available on the web and elsewhere.

**Chapter 4**, Communications Protocols and Modulation, attempts to review coding and modulation and does give the reader a feel for the options available. It is unfortunate, however, that in describing advanced digital modulation schemes, that there is only a short paragraph at the end of the section reminding the reader that there are carrier-to-noise implications as the bandwidth efficiency increases. The chapter includes a qualitative introduction to spread-spectrum techniques.

**Chapters 5 and 6**, Transmitters and Receivers, give qualitative descriptions of some common circuit techniques.

**Chapter 7**, Radio System Design, is where the book will be most useful for the majority of SRD users. It explores the basic system parameters (system range, receiver sensitivity, noise figure, bandwidth) and looks at issues such as unwanted receiver responses, intermodulation and dynamic range.

**Chapter 8**, System Implementation, is really a review of modules and devices available at the time of writing (August 2003 for the second edition) and includes reference to some useful industry sources.

**Chapter 9**, Regulations and Standards, is necessarily too brief to cover all the details, but does give the reader a useful overview and comparison of the regulations in the US and Europe, and a reminder that the SRD bands may be unlicensed, but are not unregulated. References are given for the complete standards documentation.

**Chapter 10**, Information Theory, is an oddity – it includes an introduction to error control coding in the second half of the chapter, which could have been expanded, with the earlier discussion on probability reduced.

The final **Chapter 11**, Applications and Technologies, looks at applications such as wireless local-area networks (WLANs), personal-area networks (PANs), Bluetooth and ZigBee and UltraWideBand (UWB). It is useful in reminding the reader of the options available and providing a rough comparison of their capabilities.

There is a list of references, ranging from standards and articles, to manufacturers' application notes, many of which are directly relevant to SRDs.

The CD that comes with the book contains a number of Mathcad worksheets with the relevant basic equations for some of the techniques mentioned in the book. Whilst they in no way replace CAD facilities, they do allow the reader to get a feel for, amongst other things, component values in matching networks, some antenna designs and simple propagation issues.

To conclude, does the book meet its aim? The answer is a qualified 'yes'. In the preface to the First Edition, there is the statement that it is intended primarily for 'adapters of wireless subsystems' who may develop products that incorporate SRDs. The book doesn't provide them with all the answers, but it does give a useful insight into the issues involved. It is a readable book, with few typographic errors.

**Ian Whitworth**

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# Current mode first order all-pass filter using CDTA

All-pass (AP) filters find many applications in analogue signal processing tasks, to shift the phase of a signal with constant amplitude, to produce various types of filtering characteristics and to implement high-Q frequency selective circuits. Literature is full of first-order AP voltage-mode circuits constructed around different contemporary active building blocks. The reported circuits have the drawbacks of being non-canonical and with limited bandwidth performance.

On the other hand, current-mode (CM) filters are receiving much attention owing to the advantages of inherently wider bandwidth, simpler circuitry, lower power consumption and wider dynamic range. Study of the reported CM filters reveals that these use an excessive number of active and/or passive components and are associated with the realisibility condition. But, the circuit that is devoid of this condition lacks the essential feature of electronic gain adjustment, which suits contemporary IC design techniques.

Here we propose a new CM first-order AP filter using a minimum number of components vs two passive components and one recently introduced active device current differencing transconductance amplifier (CDTA). The circuit enjoys the salient features of being devoid of the realisibility condition and gives output current at high impedance, which suits cascadibility without use of additional buffers and permits electronic adjustment of gain. The gain of the circuit is temperature invariant, being ratio of transconductance gains of operational transconductance amplifiers (OTAs), which themselves are temperature dependent. The circuit can yield another type of AP filter through CR:RC transformation. The workability of the filter is checked with PSPICE.

The port relations characterising the CDTA are given in **Table 1**.

A routine analysis of the AP circuit of **Figure 1** yields the following current transfer function:

$$\frac{I_o}{I_{in}} = \frac{g_2}{g_1}\frac{1-sCR}{1+sCR} \qquad (1)$$

The gain and phase are respectively given by:

$$H = \frac{g_2}{g_1} \qquad (2)$$

$$\phi = -2\tan^{-1}(\omega RC) \qquad (3)$$

From Equations 2 and 3 it is clear that gain and phase can be adjusted independent of each other. The tunability of the former parameter can be achieved through $g_2$ and/or $g_1$ while the later through R and/or C, besides the frequency of the applied signal. An examination of Equation 2 reveals that the gain will remain stable against temperature variations, as it is a ratio of transconductance gains. Through implementation of CR:RC transformation, the circuit yields another version of AP circuit for which the transfer function is given by:

$$\frac{I_o}{I_{in}} = -\frac{g_2}{g_1}\frac{1-sCR}{1+sCR}$$

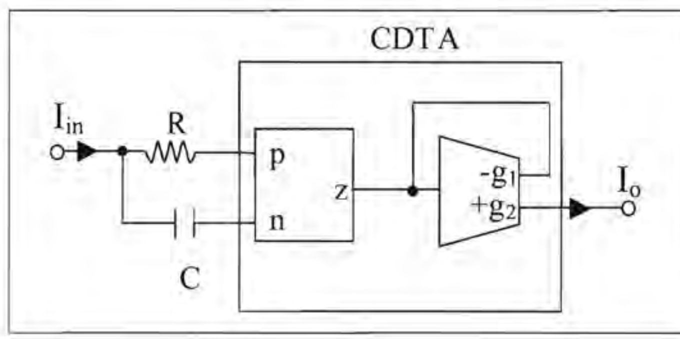
and the phase by:

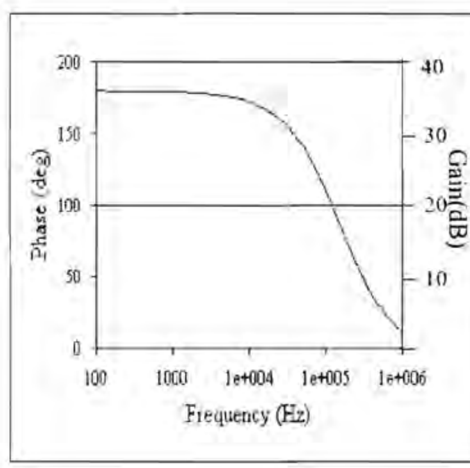
$$\phi = \pi - 2\tan^{-1}(\omega RC)$$

This version offers same advantages as that of the original configuration.

PSPICE simulation was carried out to check the workability of the filter. The filter was designed for pole frequency of 159kHz and gain of 20dB.The designed values are R = 1kΩ, C = 1nF, $g_1$ =1ms and $g_2$ =10ms. **Figure 2** shows the amplitude and phase responses of the circuit.

$$\begin{pmatrix} I_z \\ I_{x+} \\ I_{x-} \\ V_p \\ V_n \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 1 & -1 \\ g_2 & 0 & 0 & 0 & 0 \\ -g_1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} V_z \\ V_{x+} \\ V_{x-} \\ I_p \\ I_n \end{pmatrix}$$




**Top:** Table 1
**Middle:** Figure 1
**Right:** Figure 2

**N. A. Shah, S.Z. Iqbal and Munazah Quadri**
*Department of Electronics and Instrumentation Technology, University of Kashmir, India*

# EPABX battery protector

This circuit was designed specifically to protect the discharge of the battery below the specified limit. This is required because if a battery discharges below the lowest usable value repeatedly and it is still used, the chances of the battery getting damaged are increasing.

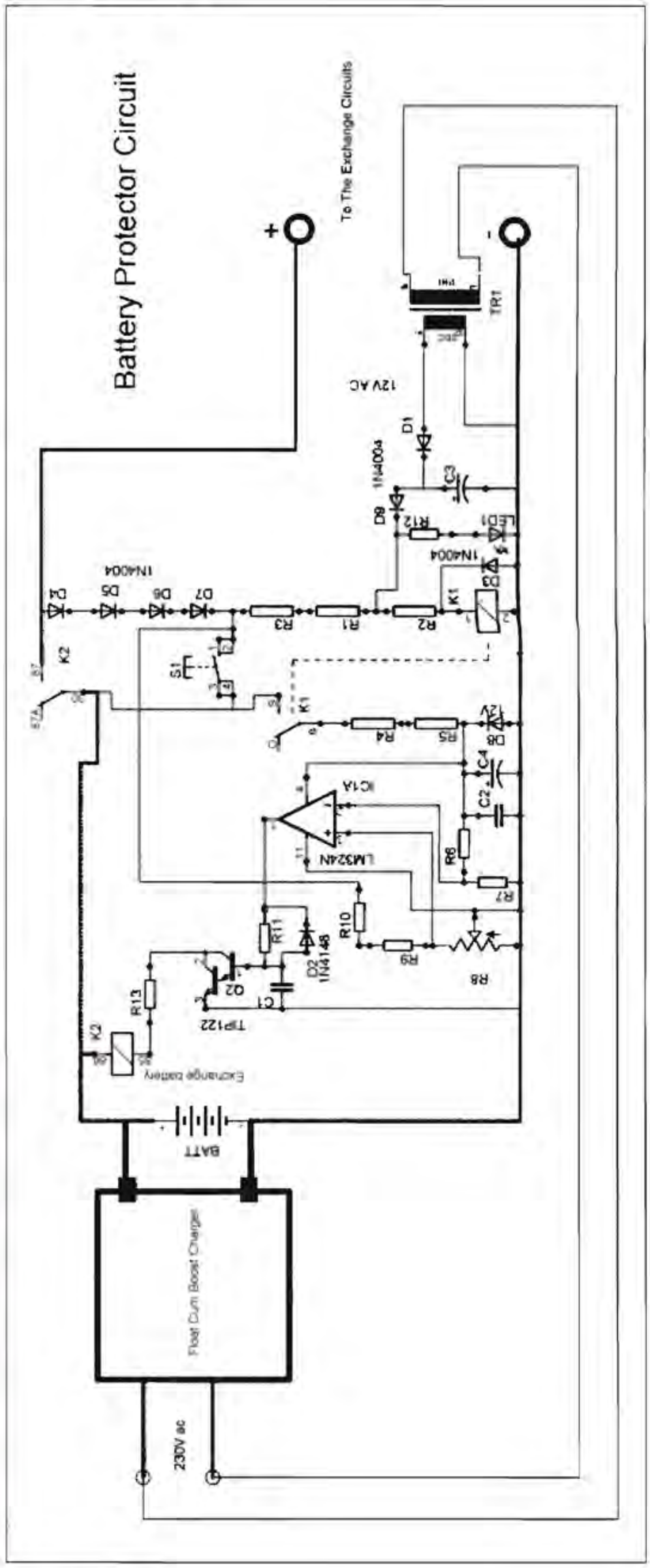
In rural India electricity is interrupted for 4-8h as part of load shedding. This would automatically take the EPABX in those regions to the battery mode. Repeated interruption of electricity means that the time for recharge of battery increases. Hence, the batteries are never charged to the fullest capacity when the demand to supply voltage arises because of the interruption of the electricity.

If batteries are not protected, they would repetitively operate below the specified lower limits and, eventually, they get damaged.

Circuit operation is as follows:

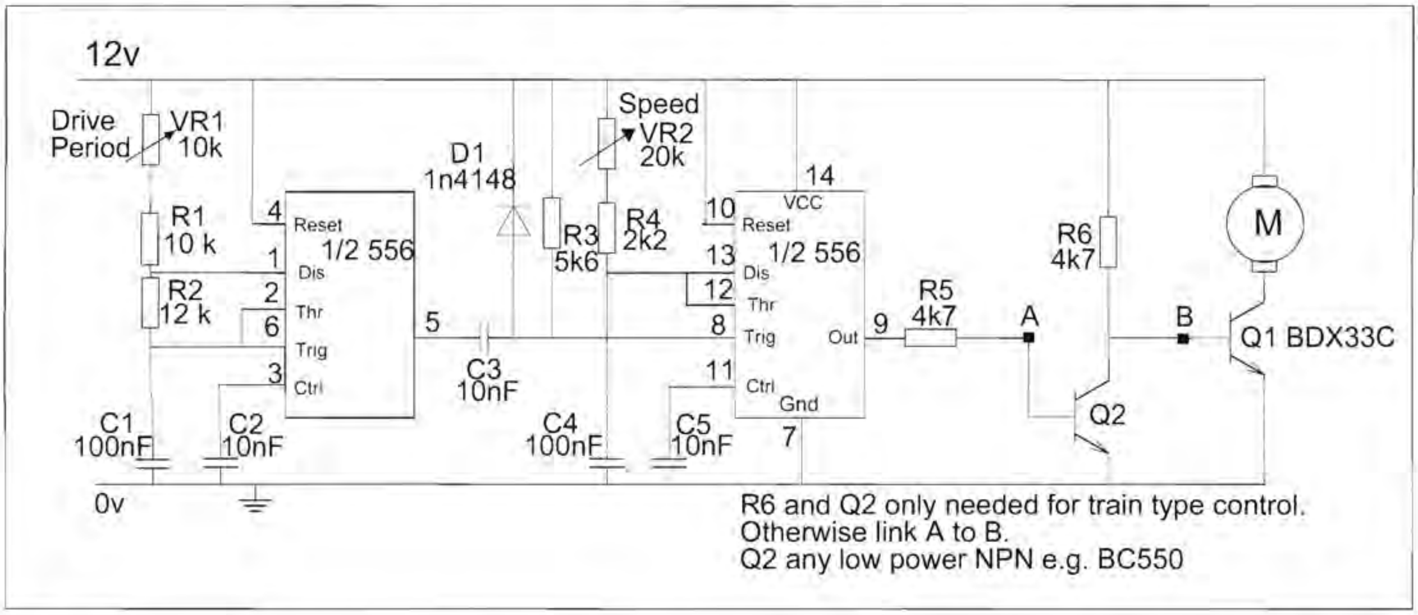
➢ With the mains present, K1 relay gets supply from the transformer output secondary DC through R2.
➢ K1 contact produces a reference voltage 12V across D8.
➢ The reference makes output of comparator IC1A high.
➢ The float-cum-boost-charger is also getting the mains supply and thus supplies 12VDC to op-amp IC1A.
➢ This makes the output of op-amp IC1A high and the transistor Q2 'on', resulting in the contact K2 becoming 'on'.
➢ The circuit remains 'on' for the battery, even if the mains supply is interrupted.
➢ The circuit remains 'on' till the battery voltage is such that the voltage at pin 3 goes below that of pin 2. This is set when the battery voltage reduces to 42VDC or less.
➢ When this happens, the transistor Q2 becomes 'off' and the contact of K2 opens, preventing further discharge of the battery.
➢ When the contact of K2 is opened, the supply to 12V zener breaks and the supply to the op-amp is devoid and, hence, the transistor Q2 remains 'off'. This is important to avoid the chattering (on-off-on) of relay K2. As the voltage of the battery rises back to approximately 48VDC in no load condition.

| Ser. No. | Component label | Value |
|---|---|---|
| 1 | Tr1 | 0-230 /0-12V, 250mA |
| 2 | C3 | 1000uF / 25VDC |
| 3 | K1 | 12V relay, 150ohm |
| 4 | R2 | 470 ohm, 5W |
| 5 | R1 | 150 ohm, 5W |
| 6 | R3 | 470 ohm, 5W |
| 7 | R4 | 1k ohm, 10W |
| 8 | D8 | 12V zener |
| 9 | C4 | 10uF |
| 10 | C2 | 0.1uF |
| 11 | R6,R7,R9,R10,R11 | 10k ohm ? watt |
| 12 | R8 | 10k 10 T pot |
| 13 | C1 | 1uF |
| 14 | Q2 | Tip 122 with heatsink |
| 15 | IC1 | LM324 |
| 16 | K2 ,R13 | Depending upon the exchange battery voltage and battery rated current. I used 470 ohm 5W. |




**Jayant Kathe**
*India*

# An inexpensive pulse width modulated speed control for 12V DC motors




The motive to produce this circuit came from a friend who wished to slow the fridge cooling water pump on his boat, as it was too noisy. There are, of course, other applications.

Whilst looking for motors to test the circuit, I remembered that we had a Doublo train set in the loft and so used the loco as a test load, so that's a possible application (see the note later). It also makes a very good dimmer.

To justify the claim of 'inexpensive': the cost of the semiconductors used (from Maplin's) is just over £1.

One half of the 556 (dual 555) is an astable multivibrator with a period of about 3ms. This period gives a reasonable size for the timing components. The astable device triggers the other section of the 556 – connected as a monostable – via the differentiator R3 C3 to shorten the trigger pulse – as the 'on' period of the monostable cannot be shorter than the trigger pulse. D1 clamps the positive spike from the differentiation that would otherwise go above 12V. The monostable has maximum 'on' period of about 3ms, varied with VR2, the speed control. The output of the monostable drives the base of Q1 (ignoring Q2 and R6 – see later), a 10A Darlington transistor.

Ideally, the monostable should be re-triggerable so that, as its 'on' period approaches that of the drive, the output would change from pulsed to continuous. Unfortunately, the 555 is not re-triggerable. This means that, if the monostable 'on' period exceeds the interval between trigger pulses, the output divides by two.

Accordingly, with the speed control at maximum, VR1 should be adjusted at a point just short of where division by two occurs. This is most easily carried with a scope, but failing that, a voltmeter on the output will show a drop of 50% at the critical point, or the load speed will drop. A stable duty cycle of 98% ($t_{on}/(t_{on}+ t_{off})$) is possible - near enough to continuous.

As VR2 is adjusted over its full range, the duty cycle changes by a factor of 10:1. This may be too large for some applications (too great a dead zone). In which case R4 should be increased to give a smaller range of duty cycle. Increasing R4 causes the maximum 'on' period to increase, so that the drive period must also be increased via VR1 to compensate. With the components as shown, there should be sufficient range of adjustment on VR1 to allow R4 to be increased to 6k8, giving a 4:1 duty cycle range.

**Note for train control:**
A conventional model train controller has a centre stop position and then rotates either clockwise for forward or counter-clockwise for reverse. This type of control is possible with this circuit – with slight modification.

The 20k pot could be replaced with a 100k with the ends of the track connected together. This arrangement gives 0 at each end and 25k in the centre (the law incidentally is parabolic).

It is also necessary to invert the drive to the Darlington transistor Q1. This is the function of Q2 and R6 in the diagram above.

This modification gives maximum speed at each end of the pot with minimum in the middle.

I leave it to the reader to devise an appropriate method of reversing the polarity of the supply to the running rails.

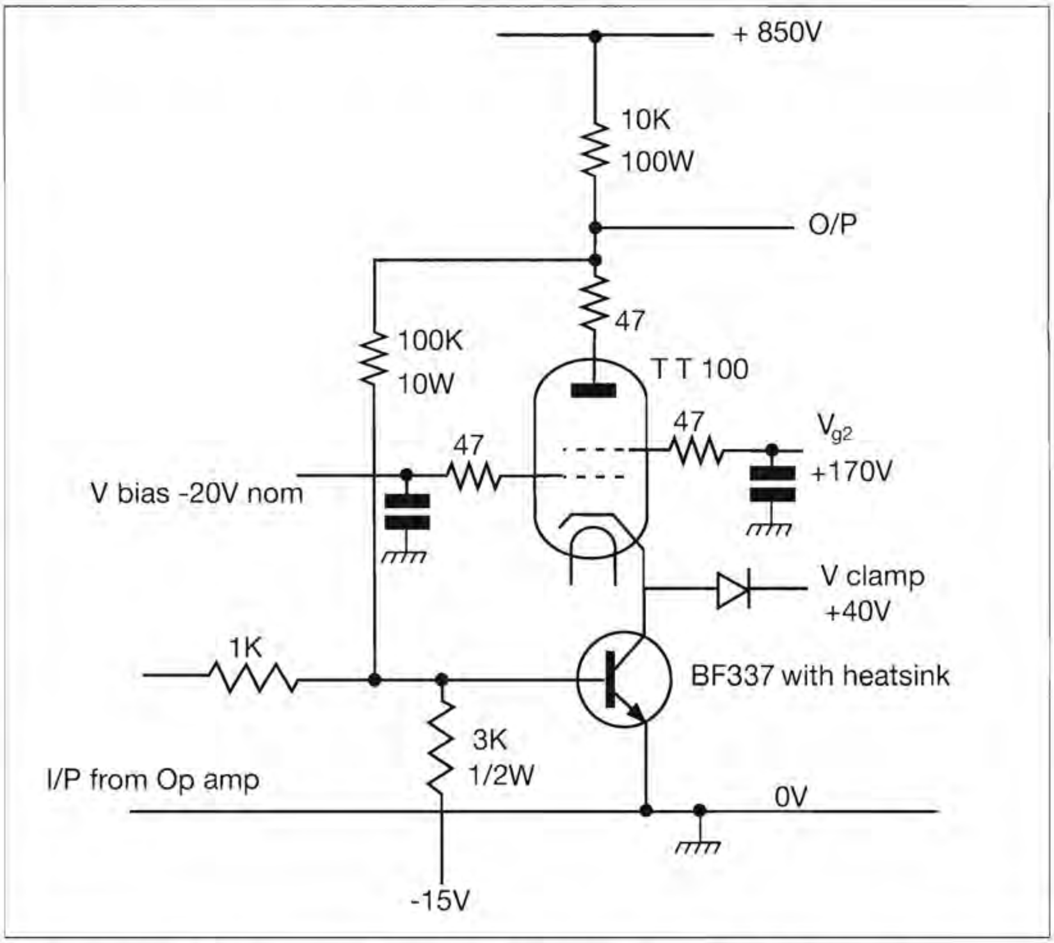
**Tony Meacock**
*UK*

# Cascode buffer gives op-amp 600V output swing

Traditionally, cascode amplifier circuits have been associated with low-level signals in the input stages of VHF receivers. This one is a little different.

This circuit was designed to interface the output of an operational amplifier to the control grid of a high voltage tetrode but it could be used wherever an output swing of several hundred volts is required. It has been used on systems operating at 80kV and has proved to be robust in the presence of flashovers and the repeated operation of crowbar circuits.

The choice of components and the possible addition of zener diode or similar DC offset circuits to the output will depend on the actual job the circuit is used for. The TT100 tetrode is no longer available but various other small transmitting valves could be used instead, depending on the particular application.




The circuit has a nominal voltage gain of 100. With the particular valve of input bias resistor shown (the 3kΩ to -15V) the quiescent output voltage should be 500V. This will allow an output swing of about ±300V. The negative bias applying to grid 1 of the tetrode is dependant on the device used and should be adjusted so that the voltage at the collector of the transistor is about 20V. The clamping diode connected to the collector of the transistor protects the transistor from overvoltage if the input signal goes excessively negative.

If the 10kΩ load resistor was replaced by a tank circuit, the 100kΩ feedback resistor disconnected and the biasing suitably adjusted for the class C operation, it should be possible to make the circuit operate as a 200W grounded grid transmitter output stage having low drive requirements. This has not been tried.

**P. F. Gascoyne**
*UK*

**Warning:**

Circuits such as this one should only be built and used by those proficient in the safe handling and operations of high voltage devices.

**Send new circuit ideas to:**

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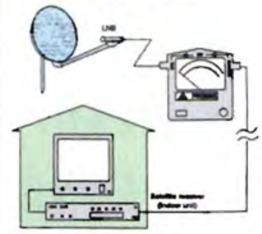


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## EARTH 2160

**PC**

★★★★☆

Earth 2160 affords you four playable parties with different basic technologies and abilities. Modular construction then allows you to customise endless buildings and units, increasing the lifespan of the game.

The actual game engine is incredibly powerful for a real time strategy game, with viewpoints from hundreds of meters high, down to two meters from the ground – all available at the touch of a button.

While some may find it hard to get into straight away, the game will appeal to the more curious among you, as well as diehard RTS fans.

## RIDGE RACER

**PSP**

★★★☆☆

Graphically, playing games on a PSP is like playing portable PS2 games. The screen offers lush widescreen images and games like Ridge Racer take advantage of them; absorbing you into the gameplay.

A simple-to-pick-up racing game, Ridge Racer provides a more than adequate excuse to show off your PSP, keeping you engrossed in the action from start to finish. With numerous different modes from arcade, single race and world tour, you'll run out of battery before you run out of things to do.

Also, if you know others with PSPs, you'll be able to link up wirelessly and take on each other!

## 187 RIDE OR DIE (PREVIEW)

**PS2, Xbox, PC**

**Not rated**

187 is a blending of genres; combat and racing. You play Buck, who's living the thug life in Los Angeles and defending his territory by racing for control. The golden rule is to win by any means necessary, even if it involves 'taking out' your opponents.


Basically, this is a racing game with guns. You control both your car and weapons as you aim for first place, shooting anyone who gets in your way. The controls take a while to get used to and the game adds nothing new to either genre, but if you like the idea of the two melding, then perhaps you may want to check this out.

## SERIOUS SAM II (PREVIEW)

**Xbox, PC**

**Not rated**

When all you want to do after a bad day at work is to blast away at an army of aliens, Serious Sam II offers an outlet for your aggression. It's a simple-to-grasp first-person shooter that really doesn' t take itself seriously. This series is well known for its 'killfest' feel, where the object of the game is to complete missions whilst fighting your way through never-ending waves of assailants; in total there are 45 different creatures to make monster mash from. In addition to its stress relief abilities, 'Sam also offers colourful, detailed backdrops for venting your anger and, even better, you can play multiplayer, both on or offline.

If you're looking for a game that acts as an aggression vent, then Serious Sam II is it.

## Engineers: listen, don't talk....

The mobile communications expert who wanted to 'rip apart the old hospitals...' (Editorial Comment, page 3, September 2005) was no doubt thinking of what interested him (or her) as well as the lucrative contracts that would flow from it. Real time monitoring of patients, coupled with the possibility of instant medical intervention, is a 'sexy' area because it throws up so many interesting problems. But 'batch processing' based upon presently available storage technology, i.e. semiconductor memory, may have much more to contribute to medical and health related support for people.

When a patient has a chronic condition like a cardiac problem or diabetes, the best the doctor can do is to order an ECG or a blood sugar test and base the diagnosis and treatment on the results. All it tells him (or her) is that on that day, at that time, under those conditions, the blood sugar was some particular value. Regular monitoring simply yields more of this. What happens the rest of the time is anyone's guess.

If a suitable sensor is available a week- or month-long record would fit on a typical 'memory stick' and could be retrieved at any time to be replayed for diagnostic purposes or for patient education. For many chronic conditions the problem for the doctor is not how to cure the condition but how to manage it. Modifying patient behaviour is one way of doing this, as are drug therapies. A few hours delay in retrieving this data will make no material difference. Mobile phone, e-mail or snail mail are all equally good means of communication.

Designing such monitors probably falls into the category of what Professor Heinz Wolfe called URINE, (Uninteresting Research into Necessary Equipment). By and large the electronics industry seems to be missing an opening in the market for simple, not very exciting products, which would meet real needs.

Perhaps the most important point to be made is that the electronics industry needs to ask doctors and those involved in the wider aspects of health care what they want and not try to tell them what they can have. Less talking and more listening by electronics engineers might be a good start.

The fact that we can do something with electronics does not mean that we should do something. That is why I would like to see any increase in the use of electronics and computing in health care being driven by those involved in health care not by the electronics industry. (One can make a similar point about computers in education).

**Les May**
*UK*

## ... and try to see the bigger picture

I enjoyed the [September 2005 Electronics World] issue and your editorial upon which I make the following observations from direct experience:

Medical staff and hospitals introduce IT devices such as PDAs, tablet computers, wireless networking and camera phones quite arbitrarily and without considering standing regulations, whether it is licenced or DoH-approved, whether IT can support it, whether it impacts any other services, data protection issues, the business/patient impact of device failure or loss, the high risk of theft of momentarily abandoned items, biological and technical cross-infection issues, the opportunity for third parties to enter into electronic communication with devices to copy, misuse or change medical and private data, the interference with medical devices (Bluetooth and IEEE 802.11 devices operate in the unlicenced SMI bands and can saturate local signalling between medical devices).

The absence of, or default settings for, encryption and the failure to change default account names or passwords gives an unaudited, unfettered path into most medical systems, if they can be accessed.

Examples occur where medical suppliers have designed devices such as scanners that do not employ anti-virus software, incorporate web-technology or use raw Microsoft operating systems. This has resulted in disruptions to surrounding systems and unauthorised connection to the Internet.

The solutions that are rejected are from the 'not-invented-here' type, solutions imposed from the centre, solutions that standardise procedures, solutions that could drive up quality by relevant metrics or security, solutions that dilute/delegate the power of physicians and "gatekeepers". The continuing stream of new "initiatives" also muddies these waters.

The HIPAA in the US, coupled with stringent legal imperatives of a commercial operation in a litigation culture, has raised the awareness and attention of US board management to get security and health and safety issues addressed there. A similar Act here would be buried under bureaucracy and rendered toothless.

Before we get too smug, the same insidious creep of technological vulnerabilities is present in the industrial control and automotive domains and may well lead to tears before too long.

As engineers we enjoy the excitement of the challenges of design and the achievement of amazing miniaturisation or microcircuitry, yet often fail to see the bigger picture.

**Phil Phillips,**
*President, BCS Information Security Specialist Group*
*UK*

## DIY approach is costly

As a sales engineer, electronics firms are often approached me to 'fix' precision motion systems that have been built in house. Such companies have often scoured the motion control industry for an off-the-shelf solution to meet their requirements but come up blank. As a result, they often turn to their in-house engineers to specify a linear motion system.

This team then produces a machine that is outside the sphere of their engineering experience, which inevitably has problems later in its life span. At the very least, the in-house team is likely to over-specify resolution, accuracy or repeatability. At worst, the team might under-specify. The former leads to a machine that is more expensive than it needs to be, the latter to a machine that doesn't meet its objectives. The irony is that, in their own field, these in-house engineers are some of the most informed professionals I have ever met – often working, quite genuinely, at the cutting edge of the electronics industry.

The simple resolution in high precision motion, excuse the pun, is to avoid the DIY approach. Instead, find a partner willing to sit down with a blank sheet of paper and work on the project from day one. This kind of custom build capacity should be the minimum requirement in a high precision linear motion application. With the eco-design directive EuP being introduced on July 6, RoHS already beginning to bite and ATEX still having an impact, design engineers need to be more conscious than ever that specialist projects need specialist advice.

**Philip Wallington**
*Applications Engineer*
*Anorad UK*

### Auto light controller

I would like to point out a few observations regarding the Auto Light Controller in the July 2005 issue (page 14).

The following few comments are just a suggestion, the project as stands is a very good idea and the suggestions here are only in an effort to improve the safety and to ensure long life of the completed item.

1. The rating given for R2 is inadequate. In this position you should use a resistor rated for high voltage use, not a 0.25W unit as given and shown. It must be a metal film one rated for 250VAC use, or, for economy's sake, composed of two or more 0.25W resistors in series. This reduces the voltage stress across the individual resistors and prevents them from arcing over internally. I would recommend three 470k 0.25W resistors in series, connected directly across C1, as if R1 fails C1 will retain charge.

2. R3 should be connected at the junction of D1 and C1, as there is a suitable waveform there, and the comment as above for R2 also applies. If connected to the C1 D1 junction, the value should then be reduced to 1M.

3. Track spacing for the wiring, carrying the full mains voltage is inadequate. The track leading to R3 should be cut with a 5mm or more cut, at the top of the Figure 5b illustration and connected via an insulated link to the C1, D1, R2 junction. This gives a larger creep distance and prevents flash over between live and earth terminals.

4. The tracks carrying current, live, neutral as well as earth, should be tinned and have a wire soldered to them along the track. This is very important on the earth connection as if it is blown open the circuit will still operate, but unsafely.

5. The rear of the PCB should receive a conformal coating of PCB varnish to reduce the risk of flash over if used in areas of high humidity. The circuit is, by definition, to be used in an unoccupied house and needs to be able to operate unattended. A mains fuse in addition to the plugtop one would be better. After all, it is possible for the plugtop fuse to be inadvertently replaced with a 13A one, and as well not all countries use fused plugtops.

6. A 250V transent supressor across the mains inlet as well as the outlet would be a good upgrade.

**Sean Beukes**
*Durban*
*South Africa*

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# Combination MultiMeter and IR thermometer


Extech Instruments has introduced Model Extech 470 – a new ergonomically designed multimeter with a built-in, non-contact infrared (IR) thermometer. The IR thermometer provides fast, easy and safe measurements ranging from -20ºC to 270ºC in a wide variety of applications including locations that are unsafe or hard to reach. A built-in laser pointer targets the area being measured.

Combining temperature with other advanced multimeter functions provides a highly convenient test tool for diagnosing and troubleshooting. Emissivity is fixed at 0.95, covering nearly all applications for non-contact surface temperature measurements.

The Extech 470 is an auto-ranging True RMS multimeter with a 4000 count display, 0.3% basic DCV accuracy, capacitance and frequency functions, and Type K thermocouple measurements, in addition to its IR capability. It is rated CAT III-600V and provides high resolution measurements including 0.1mV resolution for AC/DC voltage and 0.1µA resolution for AC/DC current. Features include MAX and RELATIVE functions, audible and visual input warnings, low current ranges for use with optional current clamp-on adaptors (measure up to 2000A), UL listing and 3-year warranty. The comfortable design allows for one-hand operation. Complete with CAT III test leads, multi-position tilt stand, Velcro strip for hanging, protective holster with test lead holder, bead wire temperature probe and 9V battery. The price is $129.

**www.extech.com**

# Six-channel audio DAC

Cirrus Logic has broadened its portfolio of audio converters for consumer, automotive and professional markets. The CS4361 digital-to-analogue converter is a complete single-chip six-channel solution that offers 105dB dynamic range, negligible distortion and jitter sensitivity. Low-latency digital filtering further preserves the original audio quality and experience and is ideal for real-time and live-sound applications. There are additional features, such as automatic sample-rate detection and on-chip level translators, which reduces the need for external components and circuit-board space.

The CS4361 is currently in volume production and is available in a 20-pin TSSOP package. It is priced at $2.70 in quantities of 10,000 units.

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# PCI Express card edge connector

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This new series AVX offers in a lead-free, RoHS compliant format.

**www.avx.com**

# Single-chip ZigBee module


Sequoia has announced the availability of JMOD01 ZigBee module that measures just 18x30mm. The module contains the JN5121 IEEE802.14.4 ZigBee chip, ceramic antenna, 16MHz crystal, 1MB flash memory and a number of resistors and capacitors. It is mounted on a four-layer PCB.

A version of the module without the on-board antenna is also available.

The on-board 32-bit RISC processor allows for applications to be in included on the module, while the hardware MAC and highly secure AES encryption accelerators, integrated sleep oscillator and power-saving features ensure low power and minimum processor overhead.

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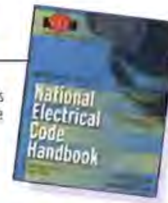


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