ectronics World's renowned news section starts on page 4

ELECTRONICS WORLD

MAY 2004 £3.25

in memoriam – John Linsley Hood MIEE

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Wayne Kerr 3245 - Precision Inductance Analyser	£1750
Bias unit 3220 and 3225L Cal.Coil available if required.	(P.O.A)
Wayne Kerr 3260A + 3265A Precision Magnetics Analyser with Bias Unit	£5500
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CONTENTS

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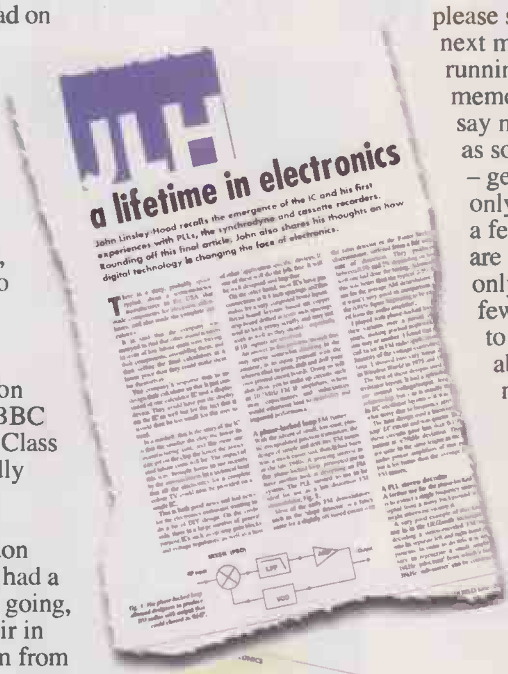
The end of an era

As I'm sure you read on the cover, one of our great audio circuit designers passed away this month. Elsewhere in this issue, Ian Hickman has penned an obituary, so I won't go on too much.

John Linsley Hood's name first came to my attention when I joined the BBC in 1970. The 1969 Class A design was rapidly gaining a 'cult' following. Almost everybody in London studio engineering had a couple of channels going, and I even put a pair in my car! I built them from bits in the junk box and a set of PCBs that a bloke on the other shift was selling through *WW*. In fact, he advertised his extension number in the ad – and got people on the other shift to take messages when he was not there! A bit of brazen profiteering.


JLH
a lifetime in electronics
John Linsley-Hood recalls the emergence of the IC and his first experiences with PLLs, the synchrodyne and cassette recorders. Rounding off this final article, John also shares his thoughts on how digital technology is changing the face of electronics.


JLH
a lifetime in electronics
John Linsley Hood looks back at his evolution from an eight-year old wondering how a crystal set worked, to a renowned analogue electronic design guru. This first article looks at his early wireless encounters.

Completely coincidentally, next month we start a series of audio articles from Graham Maynard, who pulls heavily on JLH's early work. The Class A design is referenced more than once, so I think it is appropriate to reprint the original Class A article as a tribute to the great man.

So, if anybody has any comments, recollections or just plain tributes to pay, please send them in, as next month we will be running a proper memorial to him, When I say next month, I mean as soon as you read this – get them over as we only start the next issue a few days after you are reading this. As we only got the news a few days before going to press, I've not been able to do much this month, but our sympathies go out to his wife, June who kindly phoned us with the sad news.

On a different note, I've been noticing that some of the spats in the letters section have been getting far too personal. It is for this reason that I've pulled some recently. So if you were following a juicy thread, apologies. If you are one of the authors – please keep it down a bit to ensure publication. And I don't care who started it, but suffice to say that I will be handing out detentions!

Phil Reed

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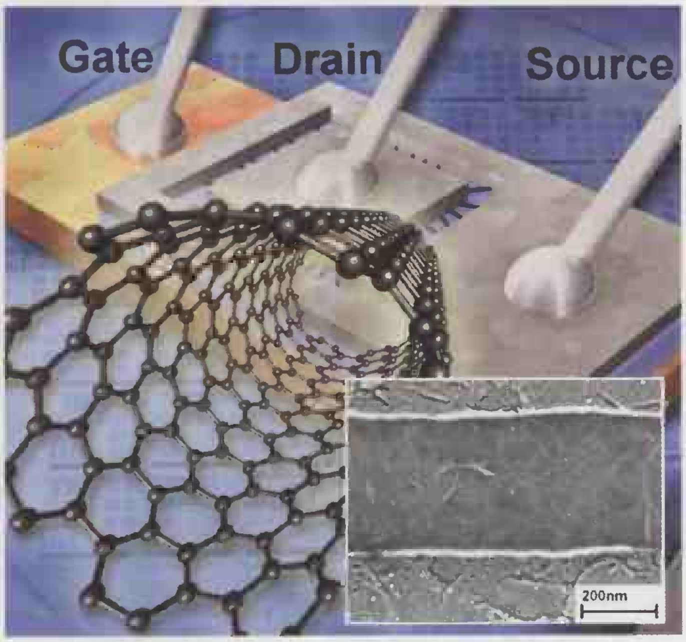
Power fet uses nanotubes



Researchers at Infineon have made a power semiconductor structure using carbon nanotubes.

"This is considered a breakthrough for nanotechnology," said the firm, "since scientists previously assumed that these atomic-sized components were not suitable for the high voltages and currents used in power applications."

Making the mosfets is not complicated. "All process parameters, such as temperature and materials, are suitable for use in conjunction with standard semiconductor manufacturing processes," said Infineon.

The firm first coated a metallic substrate with a thin insulating oxide layer, then grew random nanotubes on that by decomposing a carbon-containing gas mixture.

A random tangle of nanotubes is deposited, much like a plate of spaghetti, or the fibres in felt. In the mix are multi and single-walled tubes, conducting and semi-conducting tubes, and various length tubes.

Drain and source electrodes are then deposited directly onto the nanotube layer using a single lithographic step - leaving a square drain surrounded by a source, with a 90nm gap between them.

Although many do not, hundreds of the tubes have one end in contact with the drain, and the other in contact with the source.

By applying a brief current pulse, conducting-type tubes are vaporised, leaving around 300 desirable semiconducting tubes.

These are a mixture of high-performance single-walled and poor multi-walled tubes, but no practical separation techniques yet exists to cut out the multi-walled tubes.

Potential on the substrate, which acts as a gate, pulls carriers into the semiconducting nanotubes and turns the device on.

Current capability several microamps per tube, and about 2mA per structure. A viable transistor could be built by paralleling thousands of structures. Maximum voltage is 2.5V, limited by the 90nm gap.

The device is not practical for production, said the company. For future use, ways will have to be found to grow mostly single-wall tubes, and grow them with specific orientation.

If this can be achieved, the simple production method could make nanotube power fets commercially viable, said Infineon, and there would be other advantages: "The main advantages offered by the new type of power transistor can be seen in the significantly simpler manufacturing process, higher switching speeds, reduced heat development and in the high current densities that the tightly packed carbon tubes are able to withstand."

Magnetics sound attractive

A firm from Bristol is developing magnetic particles for data storage that are formed and contained within proteins.

NanoMagnetics has won several million pounds in funding to develop its technology, which could dramatically increase data storage density.

"Our technology is unique. It allows consumer electronics manufacturers to integrate a DVD capacity, rewritable, removable storage product in a form factor no larger than a matchbook at a lower cost than any other technology including flash and magnetic tape," said Dr Eric Mayes, chief executive at NanoMagnetics.

The basic technology is dubbed DataInk. It starts with hollow protein spheres with an internal diameter of just eight nanometres inside which are grown the magnetic particles.

The resulting powder can be mixed with resin and used to coat surfaces of disk drives. The uniform nature of the particles means they can be laid down with an even distribution.

"We are receiving a great deal of interest from a range of industries that are increasingly reliant on data storage and have a need to increase storage capacity," said Mayes.

DataInk could also be used as the storage medium in magnetic RAM chips, claimed Mayes.

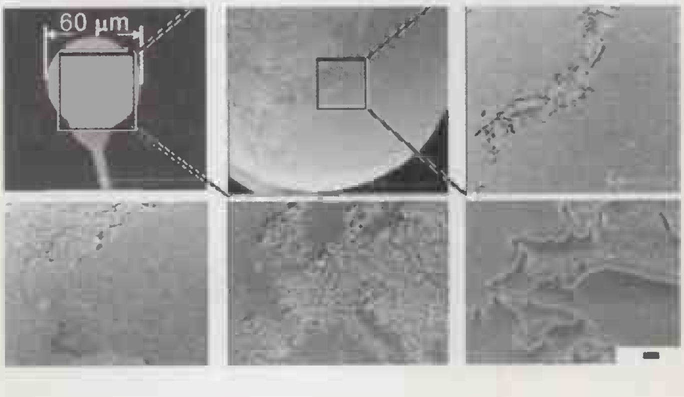
World's smallest globe

NTT, the Japanese telecom carrier, has built an electron beam lithography system that can create three-dimensional structures. To test its system NTT etched the globe pictured.

The small sphere measures 60μm in diameter, with the smallest patterned feature just 10 nanometres wide.

To pattern 3D structures, NTT invented a two-axis rotation system to move the sample. A height sensor made from a confocal laser microscope is used the keep the e-beam focused on the sample.

The resolution of the beam is claimed to be 100 times better that optical or X-ray systems.

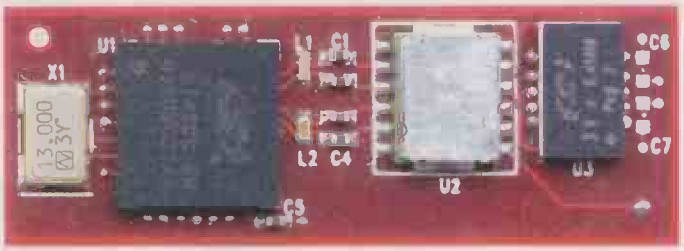


CMOS extends its reach

CMOS, that workhorse process of the chipmaking industry, is extending its influence further into the wireless communications sector.

Two companies, Silicon Laboratories and Axiom Microdevices, have unveiled power amplifiers for mobile phones made entirely in CMOS, while SiGe Semiconductor has power amplifiers made using silicon germanium.

The beauty of using silicon CMOS or SiGe for the power stage of RF equipment is that control circuitry can be integrated alongside the amplifiers. This saves component count, cost, power and improves reliability.



From left to right are the crystal, baseband processor, filter and 6.4x3.9mm power amplifier for a Silicon Labs GSM handset.

All three companies say their power amplifiers require no external components, unlike PAs made using gallium arsenide (GaAs) or indium gallium phosphide (InGaP).

Silicon Labs and Axiom have devices for the GSM mobile phone market. This brings huge design challenges, as the high power demand in GSM, up to 33dBm antenna power, results in high voltages (up to 12V) in the PA when driving a 50 Ohm load. CMOS, with its low breakdown voltage, cannot cope with this, so both firms have done some clever design.

Silicon Labs said it has an architecture that "distributes the high voltage across multiple transistors".

SiGe's device is aimed at wideband-CMDA (3G) phones. At 3x3mm the device is smaller than the GSM devices, but 3G has lower power specifications.

Brain on a chip

Canadian and German scientists have taken a significant step in interfacing brain cells to silicon chips.

Dr Naweed Syed from the University of Calgary's Faculty of Medicine planted neurons on a chip's surface and observed synaptic connections operate as stimuli were applied.

"The nerve cells not only regenerate their synaptic connections on the silicon chip but also exhibit memory traces that were successfully read by the chip," said Syed. Working with the Max Planck Institute for Biochemistry in Munich, Syed cultured nerve cells from a snail before placing them on the chip. A stimulus applied to one cell was communicated to others and read through a transistor on the device.

"We discovered that when we used the chip to stimulate the neurons, their synaptic strength was enhanced. This finding tells us that these neurons are exhibiting signs of learning and memory," said Syed.

The next stage is to connect human brain neurons to silicon. The Calgary team hope the work will one day lead to control of prosthetic limbs or even the restoration of sight.

UK firm marks 20 years in space

UK satellite developer SSTL has celebrated 20 years of successful orbital operations, with its second satellite, UoSAT-2, still in use today.

Thousands of radio amateurs, schools, college and university groups have received, decoded and analysed data transmitted by UoSAT-2. As well as the digital telemetry and whole-orbit data collection files, plain text news bulletins were uploaded to the satellite each week and broadcast around the world.

Schools were also able to listen to digital voice encoded telemetry data transmitted by the satellite direct to two million handheld receivers. All of this culminated in UoSAT-2 supporting a trans-polar trek transmitting the expedition's position using the voice synthesiser.

Signals are still audible on the 2-metre amateur radio band (145.826MHz) and also, but not so strongly, on the 2401.1428MHz S-band beacon.

UoSAT-2 was launched on March 1, 1984 onboard an American Delta rocket from the Western Range, Vandenberg Air Force Base in California.

Since then the firm has built more than 20 satellites, ranging in weight from six to 315kg.

The firm is currently building a 400kg device for ESA, the first in the Galileo constellation of positioning satellites. It is also SSTL's first foray beyond low Earth orbit.

Europe lags on R&D spending

European countries spend two per cent of GDP on research and development in science and technology, but this lags both the US and Japan, which spend almost 3%.

Latest figures from the European Union's statistics service show that the 15 European states spend 1.99% on R&D. Japan spends 2.98%, the US 2.8%.

Spending various from one country to another in the EU. Sweden exceeds 4%, Finland is at 3.5%. The UK spends around 1.84% on R&D.

In terms of absolute values, Germany is the big spender with ¤52bn. France spends around ¤33bn, the UK just over ¤30bn.

In total the EU15 spend ¤176bn, compared to ¤315bn for the US and ¤154bn for Japan.

The EU has set a target of spending 3% of GDP on R&D by the year 2010.

Proton polymer battery nears release

NEC Tokin has further developed its proton polymer battery technology, but still has not put it into production.

First revealed in March 2000, proton polymer batteries can be thought of as half-way between batteries and supercapacitors in capacity, cycle life and discharge capability. In operation, protons (hydrogen ions) shuttle back and forth between two conductive polymer electrodes as the cells is charged and discharged by an oxidation-reduction reaction.

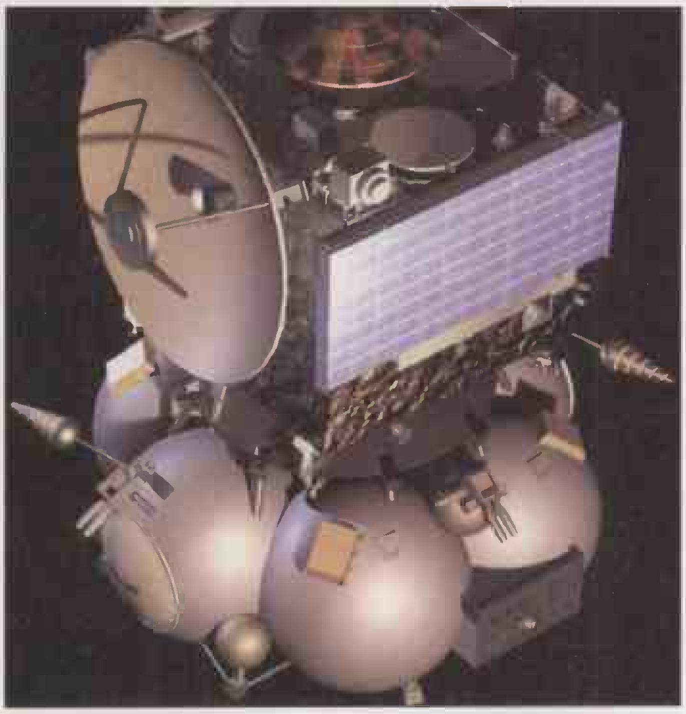
The protons are tiny compared with the ions normally exchanged between battery electrodes and therefore cause almost no life-limiting electrode damage. "A charging-discharging cycle of about 100,000 times can be achieved," said NEC, "surpassing the service life of general electronic systems. It is expected that this battery will be used as an embedded power source that needs no replacement."

The nimbleness of a proton also means high-current charge and discharge is possible. "About 20 times that of a lead battery," said the firm. "Actually, a proton polymer battery can be fully charged in minutes, and even a 200mAh cell is able to apply a current of as much as 10A. This characteristic is closer to a capacitor than a battery."

Any voltage less than a proton polymer cell's rated voltage can be applied indefinitely without damage, and complete discharge is harmless, NEC spokesman Shu Hattori told *Electronics World*.

Capacity is about a tenth of a lithium ion secondary battery, almost as much as a lead-acid battery, and dozens of times more than a super capacitor. At -20°C, 70% of room temperature capacity is maintained.

NEC's reluctance to produce proton polymer cells could be from lack of a clear market. The technology was first developed for memory back-up in phones and PDAs, but these devices are getting on fine without proton polymer. Now the company is emphasising the excellent environmental credentials of its new cells and is producing prototypes in various sizes, possibly in the hope that a potential customer will arrive with an application.



UK batteries go to Mars

The UK's AEA Battery Systems has revealed that its lithium-ion batteries are running the European Space Agency's Mars Express orbiter.

Although it makes its own cells, for military use, the actual cells on Mars Express are made by Sony under AEA patents, then tested and matched by AEA for space use.

By specifying a larger battery than would be used in, say, a computer with similar power demands, depth of discharge is limited and battery life extended to the thousands of cycles needed in an orbiting solar-powered space craft.

Even with generous capacity specification, the Li-ion cells are less than half the size, and lighter, than space-rated NiCd cells.

AEA also provided cells for ill-fated Beagle2.

Mitsubishi Electric has developed a liquid crystal display capable of showing images on both its front and rear surfaces.
The reversible LCD module consists of a single liquid crystal panel sandwiched between two transparent backlights, each of which can be turned on or off.
The display is aimed at devices such as 'clamshell' mobile phones, which have a secondary display on show when the phone is closed.

World radio from UK firm

A UK firm has developed a radio that picks up worldwide stations broadcast over the Internet.

Reciva's Internet radio uses wireless LAN to connect to a broadband link, such as an ADSL modem, without the need for a PC.

"Our first radio product is demonstrable now and allows listeners to choose radio stations from around the world," said Trevor Goldberg, Reciva's chief executive.

"By eliminating the need for a PC, we bring listening enjoyment to where it belongs; the kitchen and living room, rather than the home office and it's incredibly easy to use."

Goldberg said the firm plans to manufacture products, to license the technology to third parties, and also provide an OEM based offering for companies wanting to embed the technology.

Intel has developed an optical transceiver containing a laser tuneable across the entire C-band, used by telecoms carriers for dense wavelength division multiplexing. The C-band contains 80 channels, each spaced by 50GHz. By thermally tuning the laser to any of these channels firms can save money on inventory. The Intel transceiver is able to support 10Gbit/s transmissions.

Wideband radar pinpoints objects

Cambridge Consultants Ltd (CCL) has developed a prototype ultra-wide band (UWB) radar sensor that can pinpoint objects to within 1m range and five degrees angular accuracy, and then track them. Total range is around 100m.

Applications in traffic are planned: "For example, a pedestrian crossing such as the UK's Puffin system might use Doppler radar to sense approaching vehicles, induction loops in the road to detect stationary traffic, and infrared to sense pedestrians," said the company. "CCL's ultra-wide band radar provides all this information in one module, providing a complete image of activity with presence, direction and speed data on objects in its field of view."

The radar operates in the 5.8GHz licence-free band.

It has a single transmit antenna surrounded by four receive antennas. The whole assembly is about 100mm across.

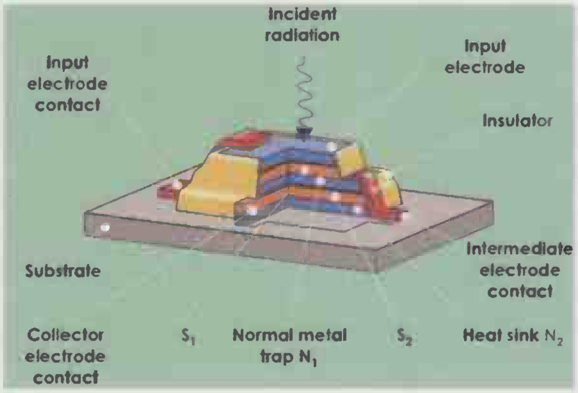
The central antenna transmits an ultra-fast pulse, band-limited to keep it legal. Four sampling receivers detect returns, with their sample delay varied so each detects objects in a hemispherical sub-1m range 'slice' on each transmit pulse. In this way, the entire range is swept slice by slice many times per second.

Digital signal processing analyses the four receiver outputs and extracts a 3-D map of objects.

No exotic integrated circuits are used, so production costs need not be high and complete systems could be installed with limited road digging. "UWB radar sensing provides vehicle and pedestrian detection that is more effective for both authorities and road-users, and lower in cost," said Jon Garnsworthy, head of transport systems at CCL.
www.cambridgeconsultants.com

Detector measures single photons

A detector for single photons has been developed at the University of Oxford, which is now looking for partners to commercialise the device.



"It is a single photon detector with improved sensitivity compared with scintillation counters and any other dispersive photon detector we know of," said Dr Roger Welch of Isis Innovations, the university's intellectual property exploitation arm.

Called Quatratran, for quasi-particle trapping transistor, it is a superconducting device which produces 10 to 20 electrons for every photon hitting its top surface. "It gives you energy resolution as well as detection," said Welch. "It has applications in infrared and X-ray astronomy, materials characterisation, and florescence measurements of biological samples."

In operation, said Welch, a photon hits the top material freeing an electron-hole pair.

Under the influence of a bias field, the electron tunnels over into a superconducting layer where, relative to the local Fermi level, the electron has a lot of energy and frees between 10 to 20 electrons - depending on its energy.

These naturally drift into the adjacent normal metal trap layer where a bias voltage causes them to tunnel through a final insulator into a second superconducting layer from where they can be extracted.

Harvard University contributed to the development, which is continuing at the University of Naples and Oxford.
www.isis-innovation.com

Diamonds are harder, forever

This is a synthetic brilliant cut single-crystal diamond grown by chemical vapour deposition. It is around 2.5mm high and was grown in about one day at Carnegie. The seed crystal is yellow, hence the tint, which is due to internal reflection as the CVD diamond is transparent.

Scientists at the Carnegie Institution have used a standard chip making process to grow synthetic diamonds that are at least 50% harder than natural crystals.

"These are real diamonds made of carbon and identical in structure to those formed in nature and by high pressure and temperature methods," said Chih-shiue Yan from Carnegie.

The US team used chemical vapour deposition (CVD) to grow diamonds on a seed crystal from a mixture of hydrogen and methane. A high temperature (2000°C), high pressure (7GPa) process than 'hardens' the crystals.

"Not only were the diamonds so hard that they broke the measuring equipment, we were able to grow gem-sized crystals in about a day," added Yan.

His team have grown diamonds up to 10mm in diameter and 4.5mm thick.

No fan needed for 1GHz x86

Taiwanese PC component maker VIA Technologies has produced fanless versions of its 800MHz and 1GHz x86-compatible Eden processor.

Called ESP8000 and ESP10000, the chips include the firm's Nehemiah CPU core and the 10000 dissipates 7W maximum at 1GHz.

"The processors are already being designed into computing and communications devices, including thin clients, personal servers and industrial PC platforms," said VIA.

Included is the firm's second-generation PadLock security system with hardware AES encryption and two random number generators. "This produces encryption rates of 12.5Gbit/s with minimal load on the processor," said the firm natively.

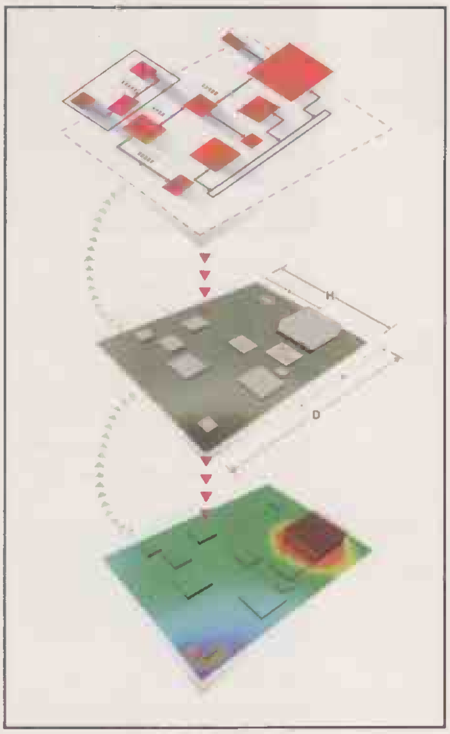
Multimedia capabilities come in the form of VIA's matched CLE266 chipset, which has a hardware MPEG-2 decoder, DDR266 SDRAM support, 6-channel surround sound, USB2.0 ports, and 10/100Mbit/s Ethernet.

VIA's previous processors have appeared on its own-brand miniature motherboards and, although no announcement has been made, the new 800MHz and 1GHz devices are expected to follow suit. www.via.com.tw

Eden specification:

- x86 compatible
- up to 1GHz operation
- 7W max power
- sixteen pipeline stages
- SSE multimedia instructions
- floating point unit
- 64kbyte L2 cache
- 35x12mm35x1.5mm BGA package

Models are hot topics



Electronic engineering professionals can now thermally model products at the earliest design stages through a software package from Surrey-based Flomerics.

Priced at $7,900/seat/year, FLO/PCB as it is called, allows multiple physical and thermal designs to be evaluated without a specialist on-hand.

"The problem [bottleneck] is the rate at which a thermal expert can respond," said Robin Bornoff, Flomerics' PCB product manager. "FLO/PCB automates much of the numerical aspect of analysis with default settings covering 80% of applications. These can be overridden for the remaining 20%."

Flomerics canvassed engineers, looking for a simple way to gather data for thermal analysis. It found that engineers like to draw functional block diagrams, ideal for FLO/PCB, but have no standard way of doing it.

So Flomerics included an easy-to-use functional block diagram drawing tool in FLO/PCB which captures data for thermal analysis as users draw their diagrams.

Users can add power dissipation figures in various ways, from a simple global power/unit area figure for the whole physical structure, through dissipative rectangular blocks representing components, to full device models from the included library.

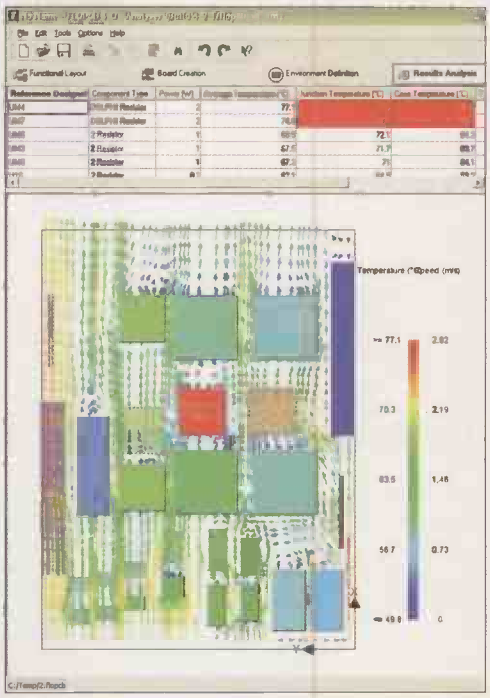
Models for single and multiple board arrangements include cards with mezzanine and daughterboards of arbitrary size and spacing are provided. Forced air and natural convective cooling are catered for.

Modeling is in 3-D. Options are 'trend', a quick coarse-grained evaluation for comparing different options, and 'accurate' which is slower, but produces representative temperatures. Functional block, physical layout, and thermal views are available simultaneously on-screen.

Resultant physical layouts can be exported to the company's full-blown computational fluid dynamics package Flowtherm, and other design tools. Thermal feasibility reports can be generated automatically.

In future, an option to export the functional block diagrams to common schematic capture packages may be added.

Customers buying multiple copies of FLO/PCB, or buying bundles can expect price reductions. A full release is due in April.



Electricity is a flush away

Flushing the toilet could lead to electricity generation, if work at Penn state University sees the light of day.

Environmental engineers at the University have shown that a microbial fuel cell can generate electricity from standard sewage and waste water.

Bruce Logan and lead researcher, Hong Liu.

Microbial fuel cells work through the action of bacteria that can pass electrons to an anode. Electrons are passed to the cathode - a carbon/platinum catalyst/proton exchange membrane - where the electrons combine with hydrogen ions (protons) and oxygen to form water.

Experiments have yielded up to 50mW of power per square metre of electrode surface. The oxidising nature of the process removes most of the oxygen demand from the organic matter in the waste.

"If power generation in these systems can be increased, MFC technology may provide a new method to offset wastewater treatment plant operating costs, making advanced wastewater treatment more affordable for both developing and industrialised nations," said Bruce Logan, professor of environmental engineering and director of the project.

Unlike some other microbial fuel cells, Logan's needs no extra bacteria or enzymes to begin the process.

The cell is a 150mm tube, around 60mm in diameter, containing eight anodes giving a total of 225cm^2 of surface area.

Superconducting processor

Japanese researchers have designed and built a microprocessor from superconducting Josephson junctions.

Over 5,000 junctions made from niobium are used in the CORE1 design, which implements a complete 8-bit processor.

The team from Nagoya University, and Yokohama University and Japan's national superconducting research centre said the design has a clock speed of 15.2GHz and consumes a mere 1.6mW of power.

Low power is achieved by transferring data with very short pulse widths, just a few picoseconds, and with voltages under 1mV. The actual data transfer mechanism is the single flux quantum (SFQ), a well-tested technique.

Circuits using SFQs process data by observing the pulse shape when single quanta pass through a superconducting ring containing the Josephson junctions.

CORE1 has a 32-byte memory shared between instructions and data, a 5-bit program counter, 8-bit instruction register and two data registers. The instruction set is very simple; halt, add, load, store, skip if zero, jump and move.

To reduce complexity and cut the number of data lines, the arithmetic and logic unit is bit serial in form. This helps, as the clock signal's wavelength is significant compared to the die size of the processor.

The processor measures 1.8x2.8mm and because it is superconducting it runs at a temperature of just 4.2K.

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Drives any 5, 6 or 8-lead unipolar stepper motor rated up to 6 Amps max. Provides speed and direction control. Operates in stand-alone or PC-controlled mode. Up to six 3179 driver boards can be connected to a single parallel port. Supply: 9V DC. PCB: 80x50mm.
Kit Order Code: 3179KT - **£9.95**
Assembled Order Code: AS3179 - **£16.95**

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Independently control two unipolar stepper motors (each rated up to 3 Amps max.) using PC parallel port and software interface provided. Four digital inputs available for monitoring external switches and other inputs. Software provides three run modes and will half-step, single-step or manual-step motors. Complete unit neatly housed in an extended D-shell case. All components, case, documentation and software are supplied (stepper motors are NOT provided). Dimensions (mm): 55Wx70Lx15H.
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Assembled Order Code: AS3113 - **£24.95**

NEW! Bi-Polar Stepper Motor Driver

Drive any bi-polar stepper motor using externally supplied 5V levels for stepping and direction control. These usually come from software running on a computer.
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Most items are available in kit form (KT suffix) or assembled and ready for use (AS prefix).

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Additional DS1820 Sensors - **£3.95 each**

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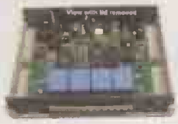
Call your phone number using a DTMF phone from anywhere in the world and remotely turn on/off any of the 4 relays as desired.
User settable Security Password, Anti-Tamper, Rings to Answer, Auto Hang-up and Lockout. Includes plastic case. 130x110x30mm. Power: 12VDC.
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PC controlled 8-Relay Board. 115/250V relay outputs and 4 isolated digital inputs. Useful in a variety of control and sensing applications. Uses PC serial port for programming (using our new Windows interface or batch files). Once programmed unit can operate without PC. Includes plastic case 130x100x30mm. Power: 12VDC/500mA.
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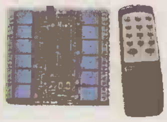
Individually control 12 on-board relays with included infrared remote control unit. Toggle or momentary. 15m+ range. 112x122mm. Supply: 12VDC/0.5A
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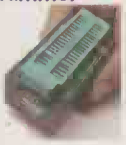
USB PIC programmer for all 'Flash' devices. No external power supply making it truly portable. Supplied complete with 40-pin wide-slot ZIF socket, box and Windows Software.
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USB/Serial connection. Ideal for field use. Header cable for ICSP. Free Windows software. See website for PICs supported. ZIF socket not incl. Supply: 18VDC.
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FPGAs demystified

Starting on any new technology can be a difficult process if the first few steps are not very clear. A typical case is getting to know Programmable Gate Arrays. Eddie Insam explains some of the facts, and describes a step by step guide on getting started and building your own simple programming development kit

A week hardly passes by without us being bombarded with information on new products, new techniques and new devices. Adverts and press releases are peppered with words such as 'solutions' and 'benefits' that to me at least, don't convey much information. Perhaps this is because I cannot see the problem they are addressing in the first place. The press releases themselves don't help much by not mentioning it either! This kind of situation can be very confusing to a newcomer or to a recent graduate. The basic chicken and egg dilemma is that if we know little or nothing about a concept, it is unlikely that we will gain much information from material presented about it in an abstract way. We won't understand what they are trying to say, or appreciate their benefits.

One such area is Gate Array Technology (GA), also known under various other names such as PLDs and FPGAs. This is a typical example of a line of products that live in a jargon fenced world, and which can put a dead stop in anybody's learning curve. The main barriers are a lack of appreciation of the uses they can be put to, a perceived high cost of entry and the difficulty in knowing where to start. Unless you are lucky or rich enough to attend a course or seminar, the only practical way to enter this secret world is by reading existing literature. Unfortunately, a lot of the information available seems to assume you know all about the subject and have a lab full of equipment and software tools, most of which having a purpose in life that appears to be completely unknown. No wonder many designers who have not been brought up on the subject from college days are avoiding or refusing to get involved in this magic world.

This article will dispel some of the myths. Even if you are not interested in using GAs, the article will induce some confidence by introducing some of the jargon. For those wishing to become more involved, there will be a step by step guide, including an easy to build circuit for a CPLD/FPGA device programmer that won't cost a fortune. This, together with the free tools available for download from the internet, will make the inroad into GA know-how accessible to anyone.

Where would I use a gate array?

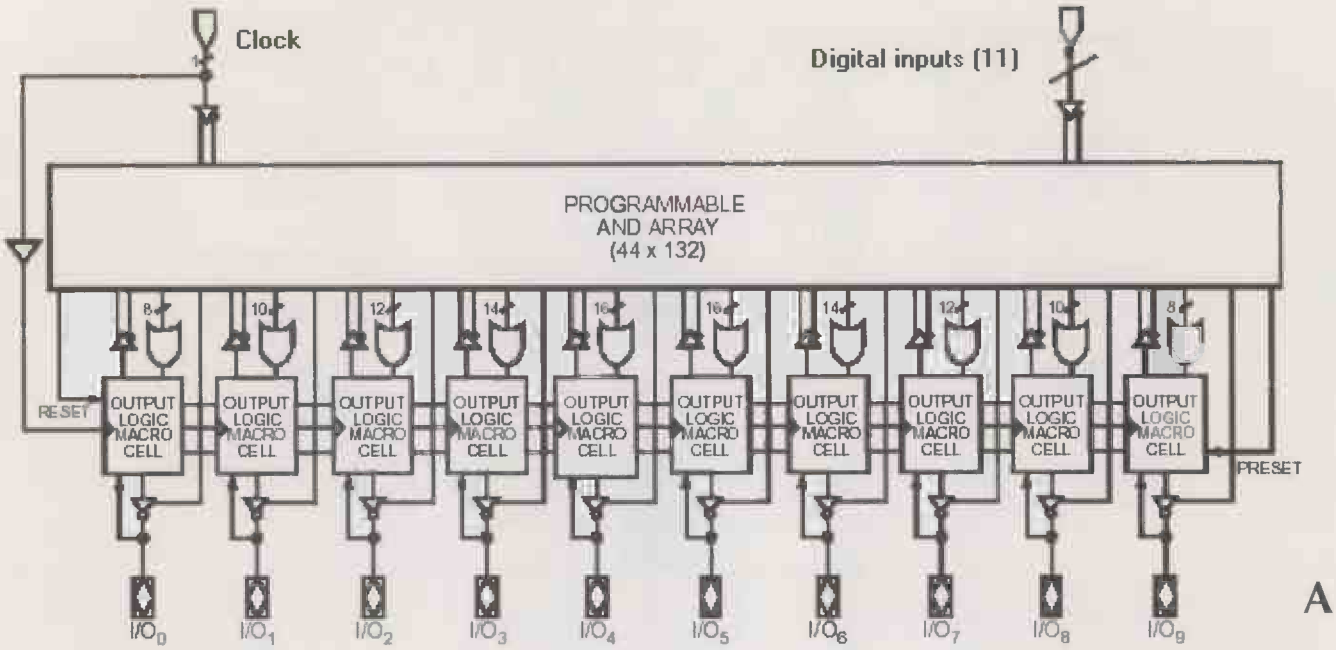
Traditionally, GAs are used as direct replacement for glue logic. This is the term given to the various logic gates, counters and flip-flops that are dispersed around a PCB to provide general interfacing, buffering and address decoding. Their advantage, from a commercial point of view, is that GAs are cheaper and occupy less board space than the discrete ICs they replace. In order to make GAs work, they need to be programmed (not unlike a PROM). The fact that they can be fuse-programmed in place means designs can be tweaked and modified after the PCB has been committed to production.

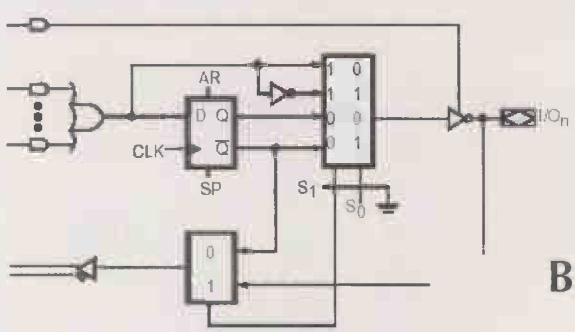
As GAs became more powerful, they started to be used as sub-modules or as complete designs in their own right. For example, as purpose built interfaces to microcontrollers, as fast UARTs or as complex communications controllers for Ethernet or encryption systems. The latest generation of GAs are powerful enough to include their own built in CPU cores, which can be used for standard computing

Not real electronics?

Gate Arrays? Surely they are not 'real' electronics, where is the fun in that? If you are one of those people who think projects involving GAs are not for you because they are not 'true hardware' and would prefer to design projects using discrete CMOS or TTL logic, this article is definitely for you. If it is because you are afraid to get into the technology, even more so. You do not know what you are missing! Even if you are a firm believer in the old ways, there is good information here to allow you to understand a bit on how they work, the jargon they use and what they could do for you.

Admittedly, any new technology takes away established methods that we may feel confident with. Gate Arrays do not take the fun out of electronics; they just place on a different level. There is an odd sense of achievement when you try, modify and improve a logic design on software before you commit to a PCB or even pick up a soldering iron. Welcome to the new order!





A typical PLD consists of a number of macrocells linked to a common cross-wire bus (A). The connections are defined by fuse links that are programmed to be either on or off thus establishing the final operation of the device. Each macrocell consists of a standard circuit using a D flip-flop and a number of combinatorial AND-OR logic inputs (B).

or for specialist applications such as Digital Signal Processing (DSP). Developing your own CPU may sound a bit like re-inventing the wheel, but there are major advantages in adding your own custom instructions to an otherwise standard set. For example, complex procedures that require several 'C' language statements in a standard CPU could be performed within a single clock cycle in a customised set. This can result in a serious increase in performance, an important factor in fast applications such as voice or video communications.

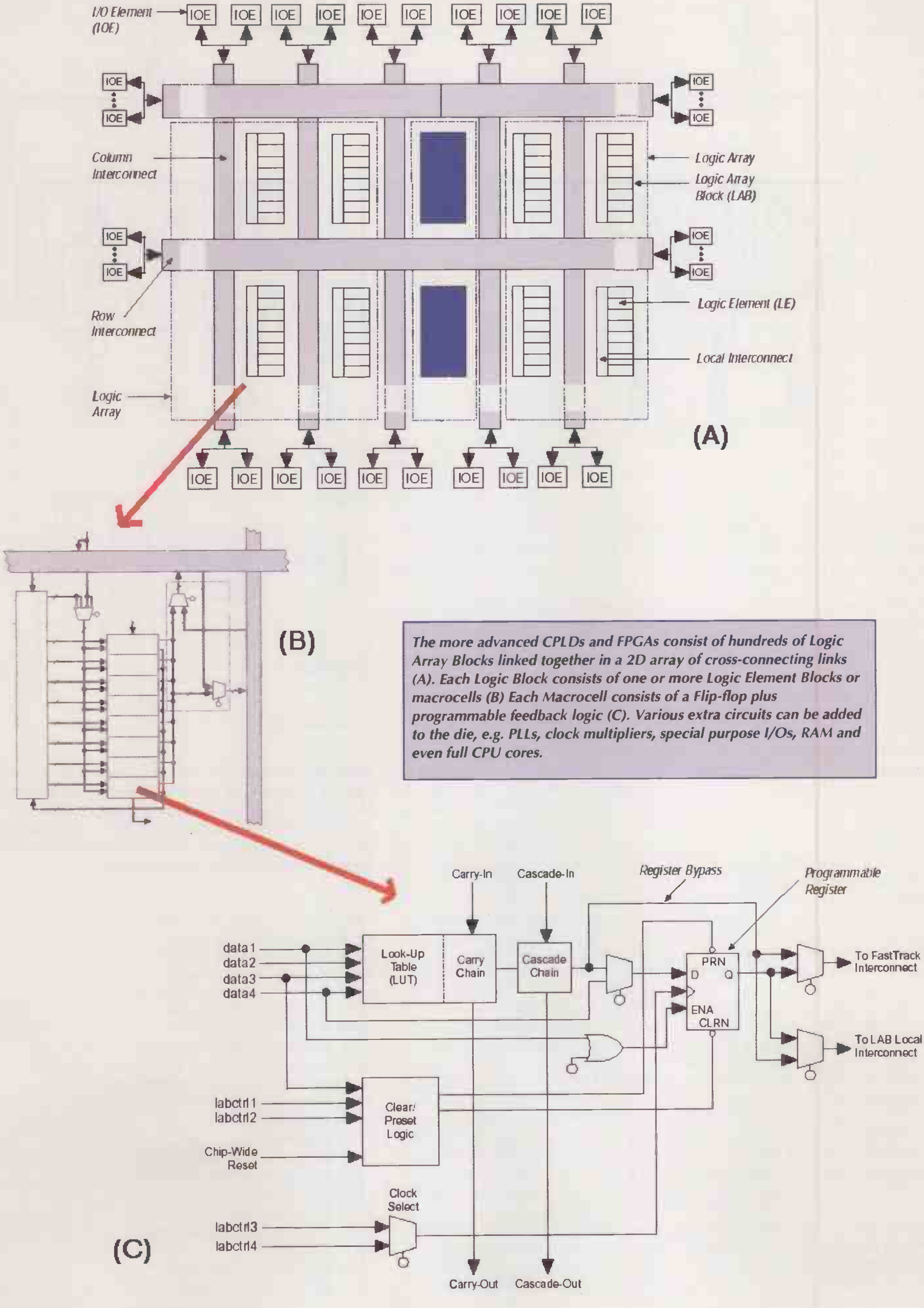
The basics

Like any good old engineering textbook, we shall start at the beginning. Programmable logic arrays have been with us for quite a few years. The original concept was first conceived in the early days of custom integrated circuit design. A few thoughtful manufacturers decided to offer IC 'pizza bases' consisting of gates, flip flops and other components laid out in neat substrate arrays but without the final metalisation layer topping (that is, the wiring connection between the devices). Users only needed to plan a design for this final layer and submit a CAD file containing the node interconnections to the manufacturer for final phase production. The users did not need to get involved in the design of the IC gates, nor they did need to know how they worked apart from knowing there were so many flip-flops, gates or whatever per chip.

Some of you may remember the venerable 82S32 fusible link PROM (still available today amazingly enough!) This was nothing more than a 32x8 cross array of open collector transistors forming a 256 bit memory cell in a standard dual in line package. The device was 'programmed' by applying high voltages to some of the pins, which made the internal die cross links 'blow up' ending up with the equivalent of a one time programmable 32 byte ROM. The device could operate at nanosecond switching speeds, very fast in those days, making it useful in applications such as address decoders and dynamic ram timing generators.

The next evolutionary step saw gates and flip-flops being integrated as building blocks within the interconnected fuse arrays. These devices have the generic name of Programmable Logic (PLD), or Program or Gate Array Logic (PAL or GAL). A typical design has a quantity of islands or blocks of standard flip-flops layouts with programmable feedback paths and programmable random logic inputs (**Figure 1**) A typical device may have 8, 10 or more of these macrocells within a dual in line package. The inputs to the flip-flops are fed from a matrix array of combinatorial inputs, so that various Boolean logic combinations can be programmed to drive the register's D inputs, either from the outside world, or from other flip-flops within the package. This makes PLDs useful as simple address decoders, adders, counters, shift registers, timers, parity generators etc. A separate clock pin usually drives all the flip-flops within the chip, and most devices include separate pins for clear, preset and tri-state output enables. Typical part numbers have names like 16V8, 20L8, 22V10 etc, where the first two digits indicate the number of logic input pins, the last digit the number of flip-flops, and the middle letter or letters, the technology used; with some minor variation among manufacturers. Each of these devices is designed to replace 4-5 equivalent CMOS or TTL packages. Not a world shattering improvement, but useful in context as PCBs get more and more crowded.

Most of the newer PLD families use CMOS technology, whilst the



The more advanced CPLDs and FPGAs consist of hundreds of Logic Array Blocks linked together in a 2D array of cross-connecting links (A). Each Logic Block consists of one or more Logic Element Blocks or macrocells (B) Each Macrocell consists of a Flip-flop plus programmable feedback logic (C). Various extra circuits can be added to the die, e.g. PLLs, clock multipliers, special purpose I/Os, RAM and even full CPU cores.

older use established MOS techniques mainly devised to achieve fast switching speeds, with propagation delays of 5nS or less. One hidden aspect of this technology is that static power dissipation can be quite high; a factor to consider when calculating overall board costs. From the programming point of view, devices are either one-time programmable (in-site or at the factory) or re-programmable by the use of electrically erasable memory cells. Depending on technology, special voltages and pulse patterns may be required, and as programming information is not always openly or freely available from manufacturers, special commercial programmers may need to be obtained.

Programming information takes the form of fuse co-ordinate listings. These are collections of ones and zeros that more or less mimic the fuse map geography within the device. These files can be generated by hand - a rather laborious task - or with the help of computers and compilers using descriptive languages which take as input node allocations in the form of text and logic equations, more on this later.

The next step in the development ladder is Complex Programmable Logic Devices (CPLD). These are in the main, evolutionary variations on the PLD theme. The register flip-flops are placed in a two dimensional row and column grid with the interconnections straddling them, just like the streets on a city map (**Figure** 2). This allows many more registers to be placed on a die. Cell designs can also be more complex, typical CPLD devices can have 256 registers or more in a single package, making them reasonably powerful. The basic flavour of the month technology is CMOS, which has the advantage of low power consumption. Programming in the main is performed at standard logic levels, using a simple serial protocol, doing away for the need for special programming voltages or specialist hardware (a microprocessor can be used to generate the programming signals)

Beyond CPLDs are the generic Gate Arrays (GAs), which include Field Programmable Gate Arrays (FPGAs.) The generic FPGA architecture is similar to that of CPLDs, but using much smaller transistor cells and corresponding miniature MOS technologies (CMOS requires massive surface areas per gate in comparison) FPGA macrocells can be much smaller in size and their building blocks can be far more complex. Figures of several million transistors on a die are not uncommon.

One small price to pay with most current FPGA technology is that programming is not permanent. In other words, the fuse link information is stored in RAM within the device and must be re-loaded every time power is applied. This requires external boot loading circuitry known as configuration devices, which are nothing more than special purpose flash EEPROMs holding an image of the fuse map.

Improved processing techniques now allow whole sections within a FPGA device to be allocated for special tasks such as RAM, special purpose I/O or even complete embedded micro-controllers. As an example of current technology, the Xilinx Virtex II/PRO series contains the equivalent of 4Mb of dual port RAM, over 45,000 registers, I/O that can operate in the Gigahertz range and four (yes four) embedded Power PC CPUs, all in a single package.

Let's talk Klingon

If you already know that 'Spartan delivers Serdes at Gigabyte speeds' has nothing to do with Greeks spreading nasty diseases, you may perhaps want to skip this section. Mythical and obscure product names are ripe in the Gate Array world, possibly one of the reasons why the uninitiated may want to shy away. One should not expect these magic names to be acronyms for anything (at least as far as I know). Just like car model names in TV commercials, they possibly sound good to the ear and convey an element of wizardry to the people who program them.

Four manufacturers dominate the field, of which two: Xilinx and Altera are the brand leaders. Others, such as Lattice, Atmel and Actel, command a smaller section of the market, but provide good competition by the introduction of innovative features and originality in their devices.

Devices are grouped into 'families' with heroic sounding names such as Spartan, Acex or Stratix. These are in the main, variations of a particular fabrication technology, MOS Type, or cell size in microns. Devices are arranged by size, number of devices and external package outline. The more complex devices are used in applications where a large number of I/O pins are required, so they are usually fitted into the larger packages. This is not always the case, and most FPGA designs end up leaving most of their I/O pins unused or unallocated.

Families are also divided into CPLDs and FPGAs as described above. In general, most CPLDs include permanent program storage, and FPGAs require external configuration devices. This division is not always strict, Atmel for example, have an FPGA technology that includes permanent program storage. In the simplest of terms, CPLDs will be used in applications requiring up to 512 registers (flip-flops) and FPGAs where more than these are needed.

The main parameters distinguishing members of a family are the number of gates or macrocells per package, the number of I/O pins, the package type (which limits the total number of I/O pins) and other features such as on chip PLLs and special purpose I/O drivers. Subtle differences in the way the macrocells are designed allow for some manufacturers to offer 'better' implementation of commonly used logic blocks, for example patented ultra-fast carry look-ahead adders, and tricks to improve performance, such as on-chip clock frequency multipliers or phase locked loops.

Families do not always complement each other in a logical way but overlap widely. This may seem confusing and can make device choosing rather complicated. The reason for this is partly because the market is technology driven. New IC fabrication techniques quickly make previous families obsolete. With such short design cycle times, many users out there will still be designing using 'older' families, which could result in a lot of confusion and aggravation. Manufacturers are keen to continue support for previous families, while at the same time nudge users to move to newer processes, which are usually cheaper and more powerful. This can make sense from the manufacturer's point of view, who does not want to be lumbered with many legacy manufacturing processes. From the user's point of view however, this policy can be a disaster, especially when it comes to maintaining a multitude of end products using a range of different devices. Some families have become more settled and popular than others, this is reflected in prices and stock levels from the various suppliers, an important factor to consider when selecting devices in a new design.

The story so far

Here is a summary of current status. Of course, no guarantees that this will all be superseded by the time you read this! The list given below is

Manuf	Type	Family	Supply V	I/O pins	FFs/ logic elems	RAM bits	Equiv gates	Package options
Altera	CPLD	MAX7000	2.5/3.3/5	36-212	21-512			PLCC,TQFP,PQFP,BGA
Altera	CPLD	MAX3000	3.3	34-158	32-256			PLCC,TQFP
Xilinx	CPLD	XC9500	2.5/3.3	36-192				PLCC,PQFP,TQFP,BGA
Xilinx	CPLD	Coolrunner	1.8/3.3	33-270	32-512			PLCC,PQFP,TQFP,BGA
Altera	FPGA	FLEX6000	3.3/5	71/218	880-2000		10k-24k	TQFP,PQFP,BGA
Altera	FPGA	FLEX10K	2.5/3.3/5	59-470	576-12000	6k-41k	10k-250k	PLCC,TQFP,PQFP,BGA
Altera	FPGA	ACEX1K	2.5	66-333	576-5000	13k-50k	10k-100k	TQFP,PQFP,BGA
Altera	FPGA	APEX II	1.5	492-1060	16k-67k	420k-1.1M		BGA
Altera	FPGA	STRATIX	1.5	340-1300	10k-114k	920k-10M		BGA
Altera	FPGA	APEX20K	1.8/2.5	92-808	1200-52k	24k-442k	30k-1.5M	TQFP,PQFP,BGA
Altera	FPGA	EXCALIBUR	1.8	186-711	4k-38k	53k-327k	100k-1M	BGA
Altera	FPGA	HARDCOPY	1.5/1.8	275-1060	16k-62k	220k-2.4M	400k-3M	BGA
Altera	FPGA	MERCURY	1.8	303-486	5k-14k	49k-115k	120k-350k	BGA
Altera	FPGA	CYCLONE	1.5	65-301	3k-20k	60k-300k		TQFP,PQFP,BGA
Xilinx	FPGA	SPARTAN II	2.5	86-284	432-5300	6k-74k	15k-200k	PQFP,TQFP,BGA
Xilinx	FPGA	SPARTAN IIE	1.8	182-330	1700-7000	24k-96k	50k-300k	PQFP,TQFP,BGA
Xilinx	FPGA	VIRTEX E	1.8 1	76-804	1.7k-73k	64k-832k	72k-4M	PQFP,TQFP,BGA
Xilinx	FPGA	VIRTEX II/PRO	1.5	88-1200	3k-125k	216k-10M	40k-8M	BGA

by no means complete and only offered as a general guide. Readers should refer to the published literature and manufacturer's websites for the latest information.

CPLD

The current Altera CPLD families are the MAX7xxx and MAX3xxx. The last three digits indicate the number of flip-flops or registers per device. For example the 7128 is a 128 register device. The 7xxx series is now a 'mature' family (another word for obsolete) and it is one of the few remaining parts that can still operate from 5 volt as well as 3.3 volt power supplies. The newer 3xxx family, recommended for new designs, uses 3.3 volt supplies only but its I/O pins are 5 volt tolerant. Xilinx CPLD families are the 9500 series (with up to 72 registers), and Coolrunner, noted for its low power consumption. Lattice CPLD families are the Mach1, Mach2, Mach4 and the latest Mach4000 series, which offer up to 1024 registers.

Prices for CPLD devices start from less than a dollar each for the smaller devices, making CPLDs very cost effective as a replacement for random glue logic. In general, CPLD prices (and power consumption) are directly proportional to the number of gates in the die whether they are used or not. So it does not pay to over specify a design using a CPLD that is larger than necessary.

FPGA

The more mature Altera FPGA families are the FLEX6000, FLEX10K, and the ACEX1K series. The latest Cyclone family is targeted at superseding these, although there is still plenty of life left in the existing ones. More advanced families include Excalibur, with a built in ARM 922T CPU processor core. Mercury, aimed at high speed I/O intensive products. Hardcopy, aimed at bridging the transition between FPGAs and custom ASICs. APEX, a high power, general-purpose device, culminating with STRATIX at the top end. Xilinx offerings are less complex: their mature technology includes the XC series topped by the SPARTAN series in various disguises, and VIRTEX at the top end, again in various disguises (see table). Top end devices can offer serious processing power, with data bandwidths in the Gigabit per second range and computing power, e.g. DSP with equivalent performance in the 2 GigaMAC range.

On power supplies and interfaces

Here is a little quiz: a large integrated circuit may contain several million transistors; assume for simplicity that each has a dynamic load of about a megohm. Simple calculations (assuming a 50% on/off ratio) tell us that the average resulting load between VCC and GND is less than an ohm. With a five volt supply, the corresponding power dissipation will be about 25 watts. In order to reduce this large sink, manufactures have developed MOS technologies working at lower voltage supplies. Since a device that runs at half the voltage consumes only a quarter of the power, this strategy is sound. Most of the newer FPGAs (and CPLDs) operate at 3.3, 2.5, 1.8 or even 1.5 volts. Many FPGAs have two separate power supplies, one for the internal core (at say 2.5V), and one for the external I/O drivers (at say 3.3V) this makes them compatible with external discrete logic circuitry even though internally they are operating at a lower voltage.

Most CPLDs and FPGAs are not normally compatible with external 5 volt logic, even though some devices with 3.3V I/O drivers can accept 5 volt logic level inputs (a 3.3V output from a GA device can correctly drive a 5V CMOS or TTL logic gate).

Because of their design, CPLDs have a relatively static current consumption, independently of number of gates 'active' and only rising slightly at higher clock speeds. On the other hand, the current consumption of a FPGA is directly dependent on the number of gates active and the clock speed (i.e. number of transitions). Power dissipation is also dependent on the software programming method used, for example a synchronous system where all the clocks are fed from the same high speed source, and the use of clock enables, which may or may not reduce clock dissipation.

The moral of the story is simple, before selecting a device for a project, make sure you have read all the documentation and application notes on power supplies and I/O interfacing. Most give charts of power consumption versus speed, and number of gates in use.

Line driving

FPGAs are heavily used in telecommunications, display panels and CPU bus drivers. No wonder

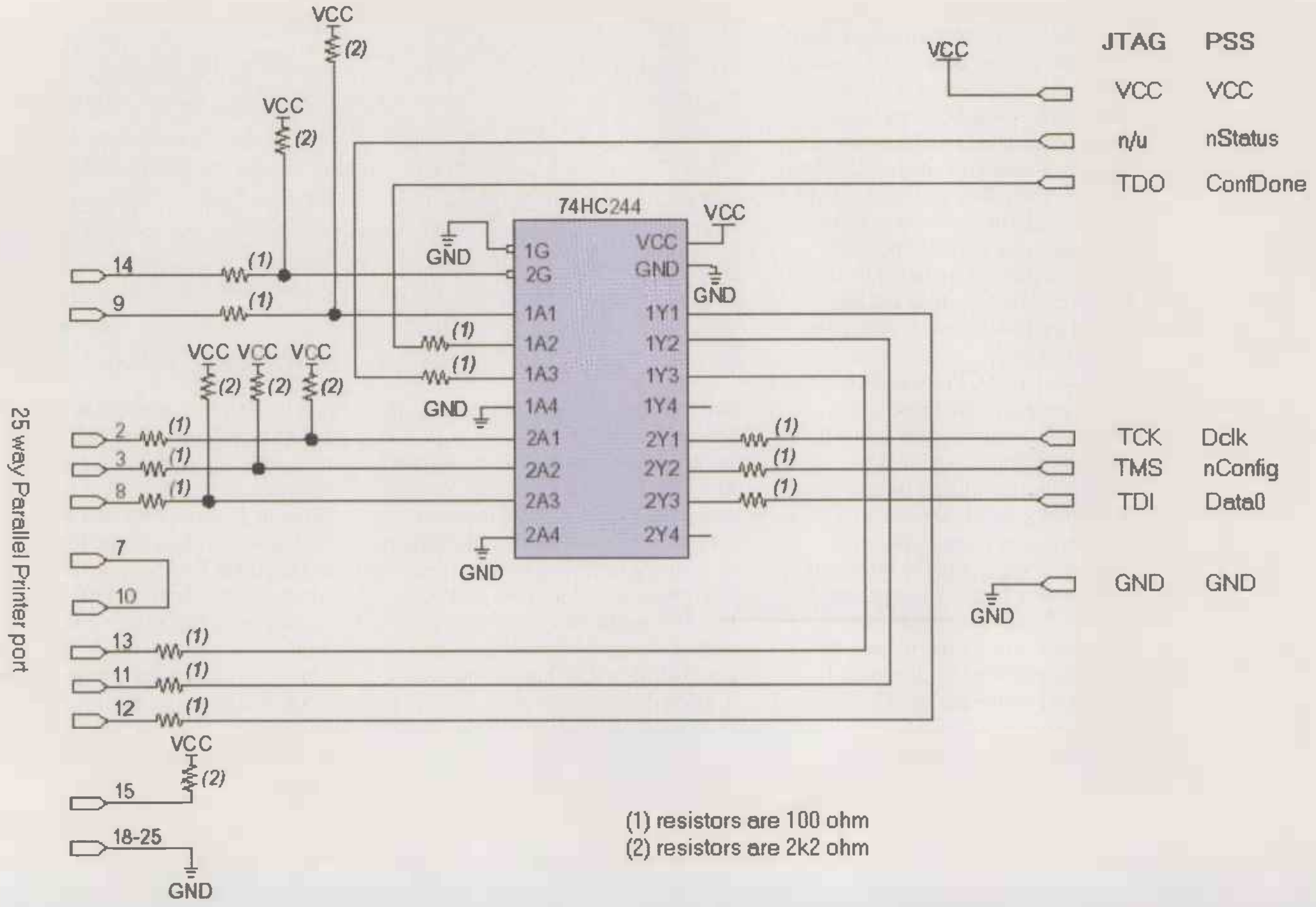


Figure 3: This simple circuit is all that is required to program most CPLDs or FPGAs in the Altera family. The resistors are required to provide compatibility with some of the lower voltage parts. The same circuit is used both for serial programming via the PSS port or for JTAG debugging. A similar layout (but with different pinouts) is used for Xilinx or Lattice devices.

many column inches of advertising are dedicated at profiling the many types of line driving interfacing these devices can handle. In order to reduce external component count, bus interface, logic level and impedance matching components are sometimes built into the GAs themselves. This allows the devices to be connected directly to PCI busses and external transmission lines. Devices can include options for differential outputs and inputs, impedance terminating resistors and various voltage threshold arrangements, including clock recovery circuits. This provides a complete in-out (no external component) interface for external loads and transmission lines.

In general, data transmission is effected as a permutation of voltage levels, transmission impedance and driving methods such as single ended, differential, or parallel form. The electronics to perform the serialisation and de-serialisation (in other words, clock recovery and parallel to serial conversion) is sometimes also built into some FPGA devices as block modules, with some of these working at up to Gigabyte speed.

The common standards for single ended I/O interfacing are LVTTL (3.3V), LVCMOS (3.3/2.5/1.8 and 1.5V). PCI (33 & 66MHz busses). GTL and GTL+ (Xerox 0.8V open drain). HST (IBM 1.5/1.8V). SSTL (IBM-Hitachi 2.5/3.3V). Differential standards include LVDS (2.5V) and its variations BLVDS (bi-directional) and LDT (AMD 2.5V). GAs can be programmed to implement any of these standards by the use of programmable impedance drivers and terminators, input/output levels and slice thresholds.

Packages

Most CPLDs and FPGAs are shipped in Surface mount (SMD) package form, with a few available in PLCC format. There is some standardisation in package size and format, but with the vast number of options regarding package size, pin separation, outline shape and footprint arrangements, each device package is more or less is unique. PCB footprints libraries should be used with caution as not all pinout dimensions are catalogue items. The best strategy is to read the data sheet carefully together with the application notes covering package layouts. If using a PCB layout CAD program do make a visual check to ensure the any library footprints dimensions correspond to the information on the datasheet of the device you are using, better be safe than sorry.

Prototyping and soldering surface mount devices requires a masterful combination of bravery and steady hands. However with some practice this is possible, even with the very fine .5mm pin spacing devices. There are many guidelines on how to do this on the Internet, some with step-by-step pictures. Enter keywords 'soldering SMDs' in an online search engine such as 'Google' to find out more.

Programming

All GAs have a number of dedicated pins for device programming. In general there are two programming methods, serial and parallel. With parallel programming, the fuse file is presented as a series of parallel eight bit bytes clocked in one at a time; an internal auto-increment counter loads the data at their right locations in the fuse map. In the serial method, data is clocked in one bit at a time, using a simple four wire serial protocol. The protocol is simple enough to be implemented with a microprocessor, but clever enough to include facilities to allow more than one device to be programmed in daisy chain fashion from the same source. The more advanced devices include functional JTAG interfaces, which can be shared for programming and for on-site debugging.

CMOS based CPLDs can keep the stored program indefinitely. However, one constraint is that the number of times some of these devices can be reliably programmed is relatively small (about 100 times). FPGAs can be programmed any number of times, but the information is lost when the device is powered off. As already mentioned, the permanent storage has to be kept outside the device in an external EEPROM and transferred across on power on.

During development, device programming is usually done via a PC and an interface cable connected to the USB or parallel port. The programming files take many formats: raw binary, Intel style hex or comma separated lists of decimal numbers.

Figure 3 shows the circuit diagram of a typical programmer for Altera devices using the parallel port of a PC. The multitude of resistors are required to provide voltage level compatibility with both 5Volt and 3.3Volt devices. The programmer can be used to program any device in any of the Altera families, although different value resistors (and supplies) will be required to program the lower voltage parts. The equivalent programmer for Xilinx devices is very similar, but uses different pinouts. Note that two sets of outputs are shown, one for JTAG and the other for PSS (passive serial). Some devices require JTAG format for programming, others PSS (or both).

In the next part of the article, I shall describe how to use the development environment and how a simple development system can be put together.

What is JTAG?

The Joint Test Action Group is a common standard developed to facilitate in-site simulation and debugging. A target system, which can be an IC or a full board, is connected to a debugging station, usually a PC using a simple four wire serial interface, which is used for monitoring status. In the context of GAs, JTAG is used to allow the PC to initialise and read internal registers and I/O states which can then be displayed on the PC during the debug session. JTAG does not strictly support device programming, but the same interface circuit can be used to program devices by means of non-standard commands.

In memoriam J L Linsley Hood M.I.E.E.

It will be with deep regret that many readers will learn of the death of that respected regular contributor to this magazine, John L. Linsley Hood. Born in 1925, John Lawrence Linsley Hood was educated at Reading School, Acton Polytechnic, The Royal Technical College (Glasgow) and, after the war, at Reading University. In 1942 he joined the G.E.C. Research Laboratories at Wembley, working on magnetron development as a junior member of the team. In 1943 he joined the R.A.F. in aircrew but was transferred to work on radar. He subsequently worked with T.R.E. (Malvern) overseas. After a return to university he joined the Windscale Research Laboratories of the Atomic Energy Authority. He was placed in charge of the research laboratories of British Cellophane Ltd. in 1954. In the late 70s John retired from British Cellophane Ltd. and set up his own business from home, as a consultant and writer of books and articles, as Robins Electronics (Robin being the nickname by which he and his brother were known in the forces and elsewhere, on account of the surname Hood). In a long and distinguished career, John published many of state-of-the-art articles, which I always found of the greatest technical interest. From 1962 he lived in Taunton, in a house called "Robins", and I often meant to contact him, with a view to paying a visit when in the area. For one reason or another, it never happened, and now unfortunately the opportunity is gone.

I first started reading *Wireless World* as a sixth former in the early 1950s, and remember many of the names of a distinguished group of regular contributors. John was one of these, along with other famous names such as Thomas Roddam, L. Nelson-Jones, P. J. Baxandall, Colin Pyckett, 'Cathode Ray' (M. G. Scroggie) and others, at least one of whom I know is still with us. John will long be remembered, by many readers including younger ones, for his articles appeared in these pages over a span of many decades. I have two files of articles saved from *WW/EW*, one of my own articles and one of others'. This second file runs to two bulging wallet folders, and a quick trawl through one of them unearthed nine articles by J L L H. The earliest I have is his *15-20W Class AB Audio Amplifier, Wireless World*, July 1970, pp 321 - 324 and the latest *Class A Power, Electronics World*, September 1996, pp 681 - 687, although I'm sure there are more of his articles tucked away somewhere.

But don't get the impression that John was only interested in audio power amplifier design, although he did stand in the great tradition of interest in this topic in *Wireless World*, from D. T. N. Williamson onwards. But other articles of his included *Linear Voltage Controlled Oscillator* (*WW*, Nov. 1973, pp 567 - 569), *Putting the quality back into a.m. radio* (*E&WW*, Oct. 1986, pp 16 - 19) and a then important article called *The Liniac* (*WW*, Sept. 1971, pp 437 - 441). This described what was in essence an opamp, implemented with discretes, in the days when opamps were still fairly new, expensive, and of limited performance.

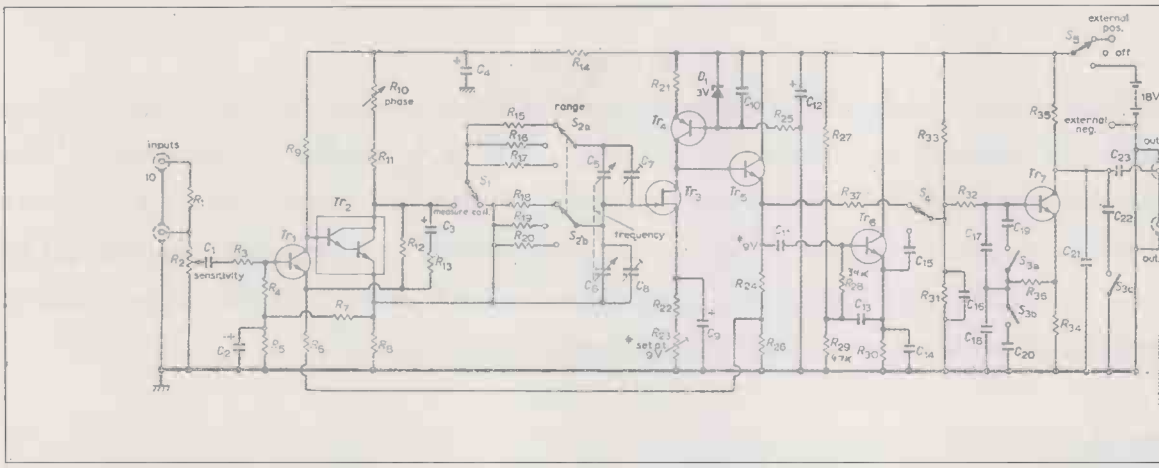


Fig. 2. Circuit diagram of the complete t.h.d. monitor.

307

Components list

Resistors

1 - 900k	19 - 1.5M, 2%
2 - 100k, lin.	20 - 15M, 2%
3 - 22k	21 - 4.7k
4 - 47k	22 - 4.7k
5 - 15k, 5%	23 - 5k, preset
6 - 3.3k, 5%	24 - 3.3k, 5%
7 - 22k, 5%	25 - 15k
8 - 1.8k, 5%	26 - 82Ω, 5%
9 - 470k	27 - 68k, 5%
10 - 2.5k, lin. (10 turns)	29 - 39k, 5%
11 - 3.3k, 5%	29 - 47k, 5%
12 - 120k	30 - 2.7k
13 - 39k, 5%	31 - 68k, 5%
14 - 1k	32 - 33k, 5%
15 - 150k, 2%	22 - 220k, 5%
16 - 1.5M, 2%	34 - 1k
17 - 15M, 2%	35 - 1.8k
18 - 150k, 2%	36 - 3.3k, 5%
	37 - 470Ω

Capacitors

1 - 470n	13 - 100n
2 - 100μ/4V	14 - 1n
3 - 22μ/20V	15 - 10n
4 - 250μ/25V	16 - 120p
5, 6 - 470p, ganged	17 - 68p
7 - trimmer	18 - 330p
8 - trimmer	19 - 680p
9 - 320μ/6.4V	20 - 3.3n
10 - 100n	21 - 680p
11 - 4.7n	22 - 6.8n
12 - 250μ/25V	23 - 220n

Diode

1 - 3V, zener

Transistors

1 - BC109 (C)	4 - 2N4058
2 - MPSA14	5, 6, 7 - BC109
3 - 2N4302	

John's interests included the important topic of measurements. Lord Kelvin or Rutherford or some similar luminary once said that if you cannot measure something, you don't understand it - a truer statement you will not come across in a very long time. An exceedingly useful piece of measurement equipment for anyone interested in audio, is a distortion meter. John published in *WW*, July 1972, pp 306 - 308, a design for a *Portable Distortion Monitor*, designed using discrete semiconductors and based on an all-pass filter section implemented with a Wien Bridge circuit. This was intended for use in conjunction with an oscilloscope to view the "residual" - the distortion products - once the fundamental has been suppressed, or with an AC millivoltmeter to obtain an approximate figure for the THD. I built at least two of these, one using a twin gang 500pF capacitor as in the original design, and one using fixed capacitors and a two-gang pot, to avoid the high circuit impedances otherwise involved. The design, though since overtaken by later developments, was so important in its day and such a good example of what can be achieved by innovative circuit design using discretes, that I have asked the Editor to find room to reproduce the circuit and component list herewith, scanned in from a rather dog-eared, scribbled-on and yellowed-with-age copy from my files, somewhat tidied up with the aid of the ever invaluable Paintshop Pro.

John must have been well known to former editors of *EW/WW*, such as Martin Eccles, Frank Ogden, Phil Darrington, Tom Ivall and others, and many readers, like me, will feel that they had come to know him a little also. He will be sorely missed.

A new monitoring tool for 5.1 audio

In this article Richard Brice proposes a new visual-display monitoring tool for sound engineers working with 5.1 audio. It combines the advantages of the analytical power of the familiar stereo Lissajous display with a visualisation of the periphonic sound-field pioneered in the 'Jellyfish' display. The background and theory are discussed and a practical, analogue circuit implementation is given

Multi-channel audio has its historical roots in the cinema industry where a sense of periphonic sound has long been thought a great benefit to the overall entertainment. Despite a multiplicity of products, a standard has gradually emerged which, whilst it fails to provide accurate periphonic localisation, nonetheless provides a degree of audio 'envelopment' which is deemed by film makers and audiences alike to be the most important factor in the enhancement of their entertainment. That standard has become known as 5.1 multi-channel audio; these numbers referring to the fact that the system comprises five full-bandwidth channels and one reduced bandwidth, low frequency enhancement (LFE) channel arranged as shown in **Figure 1.**

The low frequency channel (LFE) was originally termed the 'Baby Boom' channel for its original adoption in Star Wars in the late nineteen-seventies and is reserved and engineered to provide the physical sensation we associate with deep space explosions (albeit that these take place in a vacuum!).

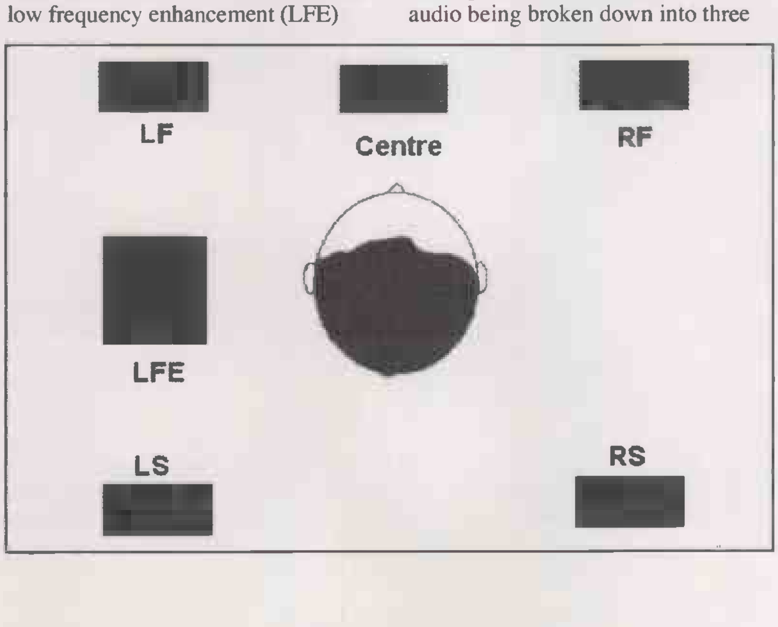


Figure 1: The standard 5.1 listening arrangement

Monitoring

Because of its increasingly wide spread adoption, the requirement for a suitable monitoring device for 5.1 audio is becoming similarly widespread. At the present time, the most common is the presentation of three quasi-stereo channels; the 5.1 audio being broken down into three pairs in the following way:

- left front, right front (LF, RF)
- left surround, right surround (LS, RS)
- centre and low frequency enhancement (C & LFE)

Unfortunately, the presentation of these signals, either on peak-reading type or power-averaging type meters, is both difficult to interpret and gives very little visual information about the 'enveloping' 5.1 sound-field. An attempt has been made to improve upon this situation by DK-Audio A/S of Denmark in what they have termed the 'Jellyfish display' as illustrated in **Figure 2**.

In this computer-generated presentation, the positions of the five, full range loudspeakers are marked on a graticule and the amplitude distribution of the sound-field is used to modulate a visual 'blob' which sits in the middle of the screen. This amplitude induced distortion of the 'blob' is very highly damped, such that if a signal of consistent energy is used to energise - for example - the left front loudspeaker, then a tentacle grows out of the blob in the direction of the speaker position. When energised with complex multi-channel programme the overall affect resembles a dancing jellyfish!

Whilst this approach is rather fun, in my own experimental 5.1 mixing sessions, I have found it to be not terribly useful. The problem is that the damping is so high that the display fails to register all but the largest contours of programme dynamics. In addition, it simply

Figure 2: The 'Jellyfish display' from DK-AUDIO

displays the energy distribution about the periphery of the listening space: which is the one thing your ears can reliably tell you! What is required is a much 'faster' display, and one that gives an indication of phase relationships between the channels.

Phase

The phase relationships that exist between channels of a multi-channel audio system represent critical information to a recording or quality control engineer. This is because – although multi-channel audio systems are largely based on amplitude-derived stereophony – faults in microphone placement and in subsequent engineering and processing can produce phase-errors and anomalies that result in poor localisation or bass cancellation and comb-filter effects; especially when down-mixed to stereo or to mono. An indication of the phase relationships between the channels can alert the sound engineer to these possible problems in a way that tired, over-worked ears cannot always do.

The requirement to view the phase relationships between the channels of a multi-channel audio system relying on summing localisation has been well established for many years: especially so in television, where rapid quality judgements have to be made in perhaps less than ideal conditions. The solution is a display of a complex Lissajous Figure[1], derived from the left and right of the standard stereo inputs. In this type of display the plates of an oscilloscope are fed with an amplified audio signal. This two-dimensional display has a particular advantage in that it permits the engineer easily to inspect the degree to which the left and right signals are correlated; which is to say the degree to which a stereo signal contains in-phase, mono components and the degree to which it contains out-of-phase or stereo components.

In the usual arrangement, the Y plates inside the oscilloscope are driven with a signal that is the sum of the left and right input signal (suitably amplified). The X plates are driven with a signal derived from the stereo difference signal (R-L), as shown in **Figure 3**. Note that the left signal will create a single moving line along the diagonal L axis as shown. The right signal clearly does the same thing along the R axis. A mono (L=R) signal will create a single vertical line and an out-of-phase mono signal will produce a horizontal line. A stereo signal produces a woolly ball centred on the origin; its vertical extent governed by the degree of L/R correlation and its horizontal extent governed by L/R de-correlation. And herein lies the polar display's particular power, that it can be used to asses the character of a stereo signal, alerting the engineer to possible transmission or recording problems, as illustrated in **Figure 3**.

The presentation of simultaneous left and right signals in a Lissajous display may usefully be thought of as the presentation of a complex plane such that any instantaneous sound pressure, caused by the combination of the signals issuing from the left and right loudspeakers, may be thought of as a complex number where the difference component is the real part and the sum, the imaginary.

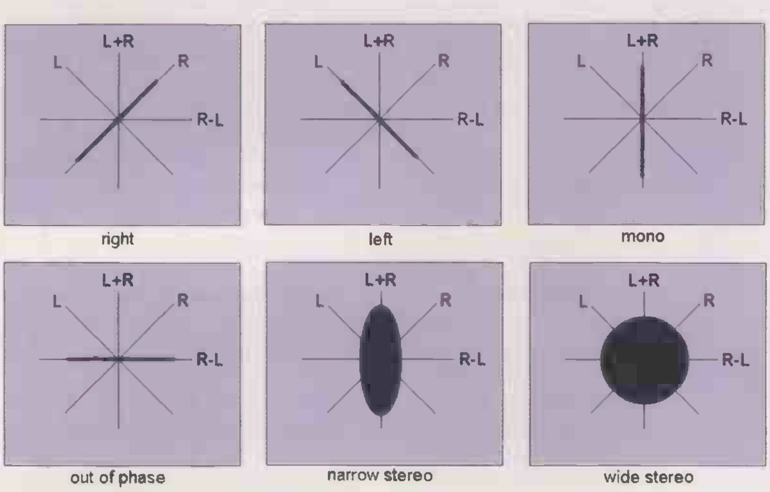


Figure 3: The stereo Lissajous display.

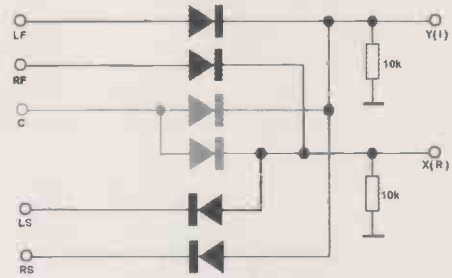


Figure 4: The initial experimental prototype

A New Monitoring Display

This article outlines the development of a new visual display device for the mixing and quality monitoring of 5.1 audio signals. It combines the attributes of the agility of the peak programme meter, the presentation of the distribution of the overall sound field of the Jellyfish display and the analytical power of the complex Lissajous display.

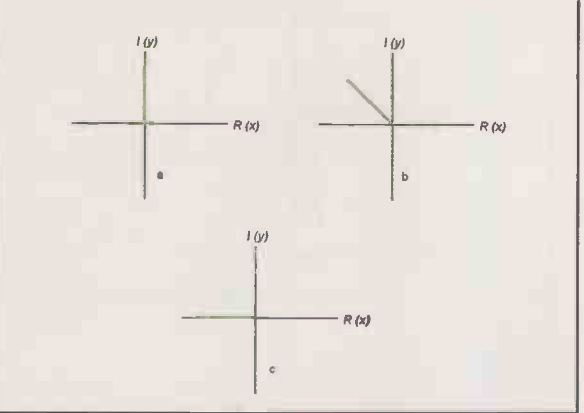
Theory

Practical 5.1 audio systems treat the creation of phantom auditory events on the periphery of the circle on which lie the five cardinal loudspeaker positions by means of a piecewise stereophony. A study of 5.1 audio books and articles, as well as investigation of practical implementations reveals the orthodoxy is the following:

Phantom images are reliably created by the energising – with appropriate amplitude differences – the two adjacent channels to the particular phantom position.

In the case of the forward arc, this is familiar from conventional stereophony. However, the Centre channel loudspeaker complicates the situation and this is dealt with later. Interestingly, contemporary usage tends still towards the use of conventional, two-loudspeaker stereophony (LF, RF only) for music-bed and front effects, with the Centre channel being reserved for dialogue or a mix of dialogue and an arithmetically derived average of left and right. This theory is extended to cover the rear arc (between LS and RS) and for side images between LF and LS and RF and RS. This monitoring tool supports the orthodoxy of 5.1 multi-channel audio and reflects the theoretical and

Figure 5: A front to rear left pan.



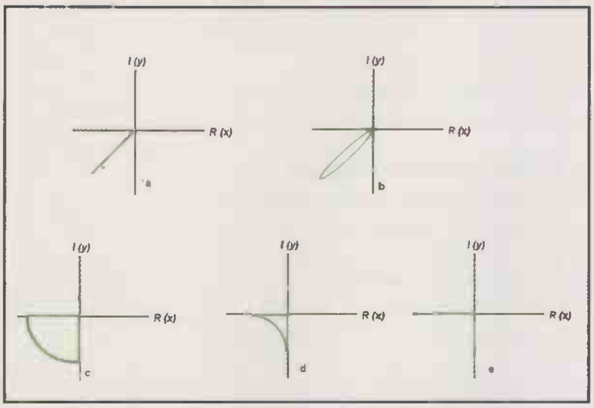


Figure 6: A thru e-adjacent channel display with various interchannel phase relationships.

practical presentation of the virtual sound field according to that orthodoxy, as will be shown below.

The schematic of the initial, experimental prototype of the proposed monitoring system is given in **Figure 4**. Central to the concept are the half wave-rectifiers. Later I will give analogue circuit implementation of the complete monitoring system but, both this rectification part and the subsequent display part, could easily be adapted (and improved) to digital techniques and/or software implementation.

Why half wave rectification of each of the input signals? The answer lies in the piecewise, two-channel stereophonic approach to periphony adopted in 5.1 audio. Think back to the complex visual display used for stereophonic monitoring in which we saw two signals energising the X and Y plates of a cathode ray oscilloscope display. As discussed, one way of rationalising this display was to imagine that one signal represented real values and the other imaginary, and that any instantaneous sound pressure - caused by the combination of these two signals - was represented at a point on the complex plane. Half-wave rectification of the signals (the transformation of bipolar signals into unipolar ones) ensures that the presentation of the signals on the display is confined to one quadrant of the complex plane. And this is exactly what is required given the piecewise, two channel stereophonic approach employed in 5.1 audio.

In the experimental set up shown in **Figure 4**, it can be seen that, with the appropriate direction of rectifier, LF and RF contribute the imaginary and real values in the first quadrant and LS and RS represent the real and imaginary components in the third quadrant. Note also that the Centre channel is added equally to the real and imaginary values in the first quadrant. This ensures that the Centre channel contributes only to a special vector at $+\pi/4$. (The Centre channel is shown greyed-out in **Figure 4** because there is a limitation with the technique as shown, which will be dealt with below.)

Now consider a sound panned from front to back to the left of the listener. A little thought will demonstrate that this will appear on the display as a phasor of length 1 which rotates between the positive imaginary axis and the negative real one as illustrated in **Figure. 5**.

In fact, ignoring the Centre channel for a moment and imagining the four remaining speakers as contributors in a conventional quadraphonic loudspeaker set up, one can imagine that, with the appropriate amplitude panning, it is possible to produce a phasor of a certain length rotating around the origin on the complex plane. Clearly, this is exactly what the recording engineer requires since it gives an accurate picture of the amplitude and position of phantom images within the listening 'circle'.

Phase display

It is instructive to consider the resulting display when, for example, two coherent signals are presented to adjacent stereophonic speakers but at different phase relationships. In this example I will take the example of LS and RS. Imagine that LS is fed with a tone of 1kHz and that RS is presented with a similar tone but with a varying phase relationship with respect to the signal in the LS channel. Experiments have shown that the resulting display is highly informative and is summarised at five important phase relationships in **Figure 6**.

When both signals are entirely coherent and in phase the result is a phasor at 225° (**Figure 6a**). As the phase begins to change at the 90° point, the display has become a hemi semi-circle in the third quadrant (c). As the signals phase relationship moves beyond the 90° point, the hemi semi-circle

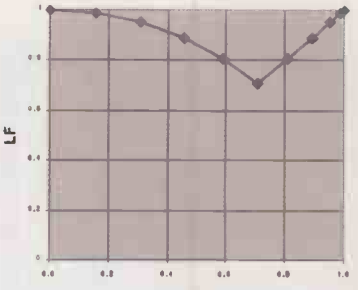


Figure 7: the result of a LF to centre pan when the circuit if Figure 4 is employed.

degenerates (d) to becoming two entirely separated phases on the real and imaginary axis (e). This is remarkably intuitive and correlates well with this objective experience. This demonstrates that the proposed display combines the virtues of:

- a fast acting presentation of five signal amplitudes
- an accurate visualisation of the direction of the phantom sound within the sound field
- the phase relationships which exist between channels.

Incorporating the Centre channel

As described above, if the conventional, two-loudspeaker, stereo panning technique is used, the proposed display will accurately represent the perceived phantom image position as a phasor which rotates between the Y(I) axis and the X(R) axis. However, there exists a problem with the proposed display in relation to the way the Centre channel is introduced as shown above.

The Centre channel represents a complication in the piecewise stereophonic approach of 5.1 theory, because sounds may be panned across the front arc in two ways. Imagine a left-to-right pan across the arc bounded by the loudspeakers LF and RF. This may be accomplished either by means of a conventional stereo pan between LF and RF, or as a pan from LF to C and thence to RF. Several authors recommend the second technique as the preferred method (Holman 2000). However, there is great disagreement between authors on the preferred control law (Rumsey 2001). Gerzon (1992) goes so far as to state that no simple law can ever exist for such a control.

So what will the proposed display indicate as a source is panned between the three front loudspeakers? **Figure 7** represents the result of a LF to Centre pan[2] when the primitive circuit of **Figure 4** is employed. To understand the graph you have to read each point left to right as the position of the tip of the phasor as it

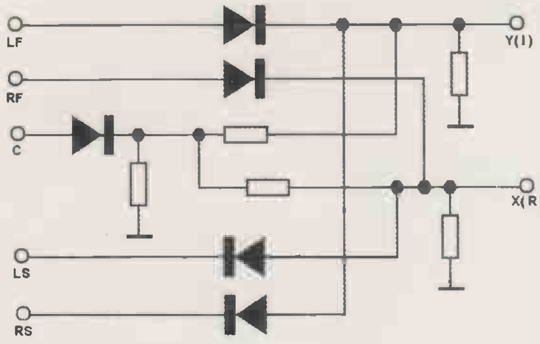


Figure 8: An improved circuit giving better results in the first quadrant.

moves from extreme left (LF) to centre (C) in quadrant 1 as the pan is operated, the various points indicating one-tenth of the overall pan-control rotation. The reason for this non-linear result is the effect of the rectifiers. Looking at the circuit in **Figure 4**, you can see that the positive values presented to the Y(I) output will be the rectified result of the LF signal and the Centre signal and, in each case, the instantaneous, positive value will be whichever is the greater of these two signals. That accounts for the inflection in the curve in **Figure 7**.

This result is neither accurate nor intuitive and something better is evidently required. One way of approaching the problem is to say, 'what is really needed is a fifth oscilloscope deflection plate between the positive Y plate and the positive X plate, energised directly by the Centre signal' (as shown in **Figure A1** in the Appendix). Naturally this would be impossibly expensive and – in any case – unnecessary, because it's possible to produce an identical effect to this extra plate by energising the positive X and Y plates with a Centre signal multiplied by sine 45 degrees and cosine 45 degrees respectively[3]. This is accomplished in circuitry by rectifying the Centre signal, reducing its amplitude by $1/\sqrt{2}$ and summing it with the signals for LF and RF to generate the X(R) and Y(I) signals for the first quadrant. A simplified circuit for so doing is given in **Figure 8**.

Interestingly, this alternative approach has exposed the unexpected result that, depending on the pan law, at some phasor arguments, the phasor magnitude appears distorted as revealed in **Figure 9**. In the figure, the phasor positions are given for twenty points between full LF and RF passing through Centre. Two laws are plotted, constant-power (diamonds) and constant-gain (squares).

However, as **Figure 9** reveals, in spite of the phasor amplitude distortion, the phasor arguments accord well with the pan-control deflection irrespective of pan-law and this is a big improvement over the original circuit. Furthermore, it is widely recognised that neither the piecewise, constant-power (sine-cosine-sine) approach nor the constant-gain approach are ideal for pan-controls for three loudspeakers in the forward arc, being deplored on both psychoacoustic (Rumsey 2001) and theoretical (Gerzon 1992) grounds. Certainly the phasor distortion on the proposed display during LF-C-R pans supports the reservations of these authors. (See Appendix 1 for a further discussion).

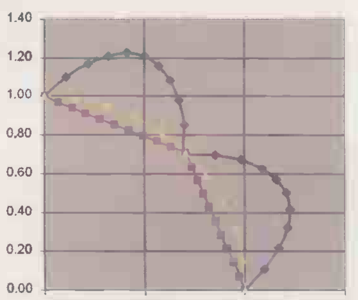


Figure 9 : Various pan laws as displayed on the proposed display.

The Final Design

Comparing the **Figures 5 and 6** with the disposition of the speakers in relation to the listener as shown in **Figure 1**, it is evident that rotating the entire display by 45 degrees would be advantage to the user; because the mapping of the resulting phasors would better coincide with the listening room arrangement. Now, any point (x, y) may be rotated by any angle (a) by means of the matrix multiplication:

$$(x, y) \cdot \begin{matrix} \cos a & \sin a \\ -\sin a & \cos a \end{matrix} = (x^R, y^R)$$

where (x^R, y^R) is the point after rotation.

Because the required rotation is constant, these multiplications are constant too, and simply represent the appropriate scaling of the summing resistors shown in **Figure 11**, which is the final, prototype circuit. Notice too that a precision rectifier circuit has replaced the simple rectifiers of the initial prototype. This is important because the complex exponentials in the two (I / Vak) relationships of the simple diodes translate to strange curly things when viewed on the complex plane!

Further Improvements

Nowadays, an analogue implementation is outdated, but – as stated above – these ideas are easy to translate to either a hardware digital or to a software implementation. One limitation which might easily be addressed in a software implementation would be the addition of a conventional PPM linear meter to monitor the LFE

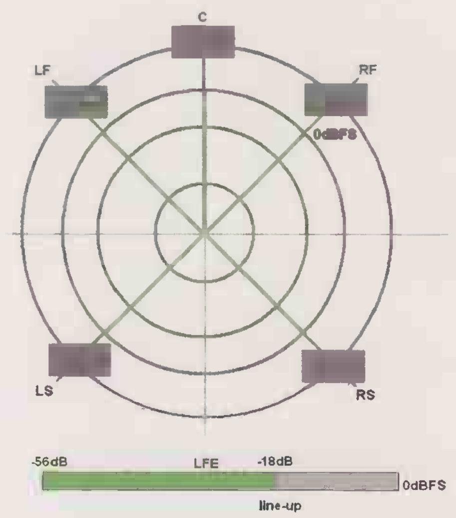


Figure 10 The final graticule for the new monitoring device.

References

Gerzon, Michael A. 1992. *Panpot laws for multispeaker stereo.* 92nd Convention of the Audio Eng. Soc., Vienna. Preprint 3309.

Holman, T. (2000) 5.1 *Surround Sound Up and Running.* Focal Press

Rumsey, F. (2001) *Spatial Audio.* Focal Press.

[1]After Jules Lissajous who was professor of mathematics at the Lycée Saint-Louis in Paris in the mid eighteen-hundreds and who studied vibrations by means of mirrors attached to perpendicularly mounted tuning forks of related frequencies.

[2]Assuming a constant-power (sine-cosine) law.

[3]Assuming linear amplifiers and linear deflection

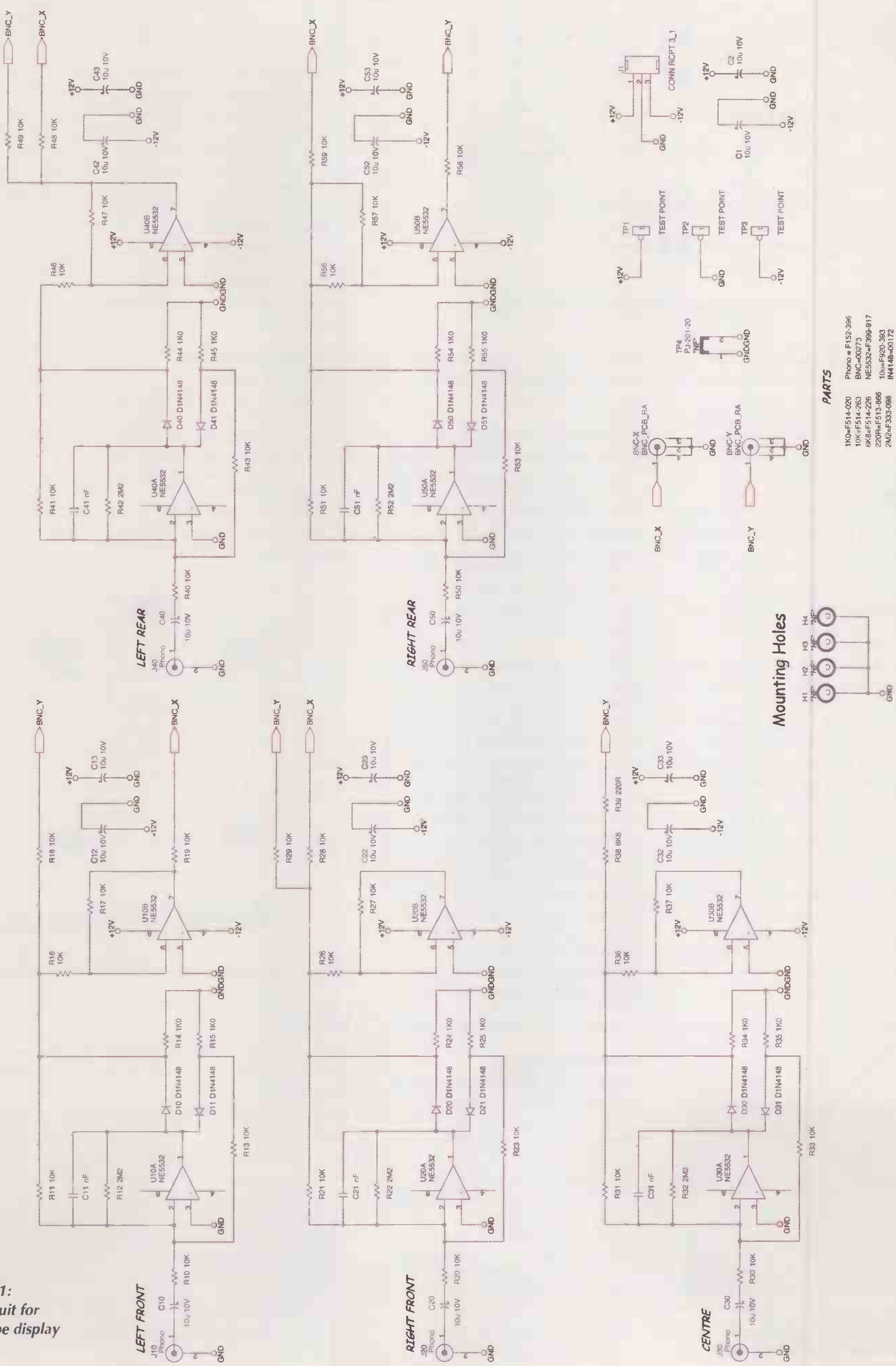


Figure 11: Full circuit for prototype display device.

Appendix

Is there a better LF-C- RF pan-law? Given the fact that the constant-power (sine-cosine) panning law is universally accepted as being the best approach to standard, two-channel stereo panning and that this law produces, on the proposed display, a result that is both theoretically and perceivably justified, it seems not unreasonable to turn the argument 'on its head' and use the display to suggest an improved panning law which will produce – when employed – a similarly consistent result when displayed in the manner described in this article.

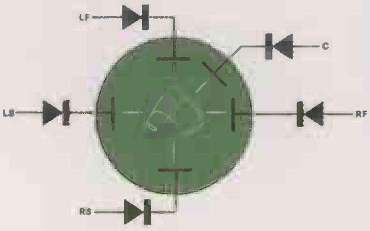


Figure A1: The proposed display rationalised as a five-plate oscilloscope.

If – as shown in **Figure A1** – we imagine the proposed display as a five-plate oscilloscope with an extra plate placed at +45 degrees between the positive X and Y plates (and it is mathematically justifiable to think of it in this way), we can solve simultaneous equations to find the ideal law so that we get an identical display for the three-channel, LF-C-RF pan and for the two-channel LF-RF pan.

This requires that we resolve any phasor into component phasors separated by 45 degrees. In **Figure A2**, phasor (r, s) is the resultant of phasor (c, d) and (a, b).

More generally, we can say that,

$r = a + c$ and

$s = d + b$

We need to solve for a, b, c and d in terms of r and s. But there are too many unknowns. Fortunately, we can simplify. Firstly, because one component of the vector is always aligned with the Y-axis, the value of c will always be zero. Secondly, because the second component is always at 45 degrees, a will always equal b. So we can re-write this,

$r = a$, or $a = r$ and

$s = d + a$, or, $s = d + r$

$d = (s - r)$

But, because we are thinking in terms of the voltages applied to these plates, we must think in terms of the magnitudes of each phasor M(Y) and M(C). Because c is always zero, the M(Y) = d. The magnitude of the phasor (a, b) is given by,

$$M(C) = \sqrt{(a^2 + b^2)}$$

Although this simplifies (because a=b) to,

$$M(C) = \sqrt{2}\, a = \sqrt{2}\, r$$

We can now solve for a and d so that the phasor (r, s) proscribes a circular path; just as it does when it is generated using the sine-cosine relationship in X and Y. The results are given in **Figure A3.**

Note that the LF and RF responses are based on a (sinθ - cosθ) curve and the Centre channel pan is based on an amplified version of the cosine curve between 0 and 45 degrees and its mirror image (both these functions having a similar form). Happily for the analogue designer, the results are very nearly linear and a proposed circuit is given in **Figure A5**.

The results shown in **Figure A4** are plotted on the same axes as **Figure 9** to compare this proposed law with the constant-power and constant-gain regimes discussed in the main text. For comparison, the results of the circuit plotted with the theoretical curve in **Figure A6**.

Returning to the analogy of the five-plate oscilloscope, the proposed display is a consistent analogue of the physical, acoustical situation when five loudspeakers are arranged as in a 5.1 set-up. It thereby represents a consistent, theoretical framework for analysing the 'pan problem' discussed by the authors in the references. Therein lies the possible legitimacy of the new pan-law. Nevertheless, the display is not a perceptual model and the validity (or otherwise) of the proposed pan-law would need to be tested in listening experiments.

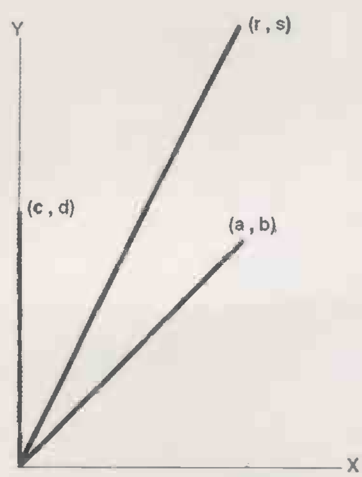


Figure A2: Phasor (r , s) is the vector sum of phasor (c , d) and (a , b).

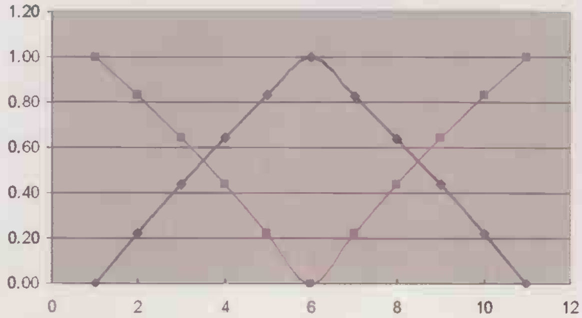


Figure A3: A proposed new panning law.

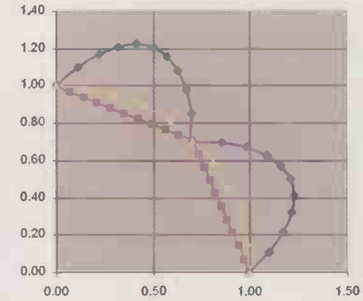


Figure A4 – The result of the new panning law when displayed on proposed display (triangles). Constant-gain (squares) and constant-power laws are plotted for comparison.

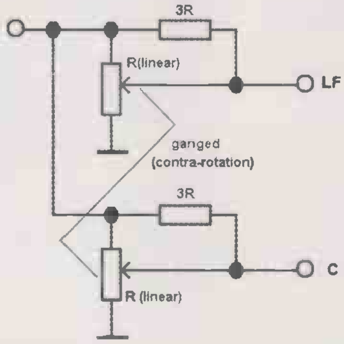


Figure A5: Proposed new pan control and values.

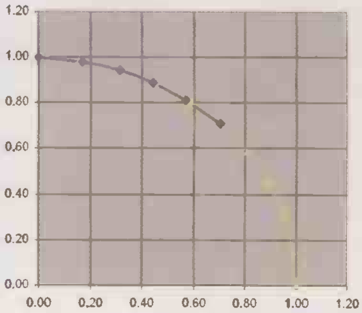


Figure A6: Practical pan-control law and its display on proposed display (theoretical curve is also given – triangles).

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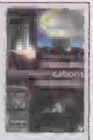

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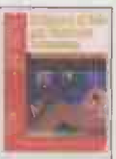

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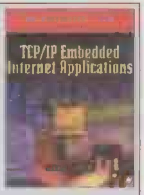

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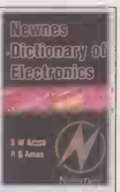

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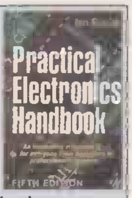

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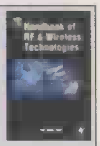

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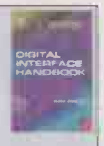

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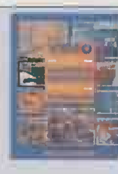

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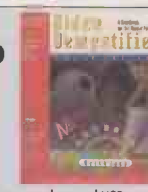

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Precision rectifier circuits

Intrigued by Darren Heywood's precision full wave rectifier circuit described in the January 2003 issue of Circuit Ideas *(EW page 36)*, Alan Bate has come up with some different ideas

As this kind of circuit is usually implemented by linearising a diode rectifier forward characteristic within a negative feedback loop, Figure 1 shows the classic full wave circuit using this approach. The problem with such a circuit is the performance of amplifier 1 which not only needs to have wide small signal bandwidth and but also high slew rate to rapidly switch through the open loop transition when the diodes are shut off. See Figure 2 of a SPICE simulation at 10kHz, using general-purpose small signal Schottky diodes and OP37s. Note the fast transition required of the op amp in the diode drive waveform. However, new op amps like the Analogue Devices AD3038/39, with a small signal bandwidth of 350MHz, and slew rate of 425V/ms would now turn this approach into a 'humdinger of a circuit'!

Mr. Heywood's approach to linearise the rectifier function is novel as it potentially offers wide bandwidth. However, his circuit suffers from a few limitations, which can easily be put right, greatly improving linearity at low signal level and bandwidth. His sensitivity and bandwidth claims of 20µV and 2Mhz are also worth investigating.

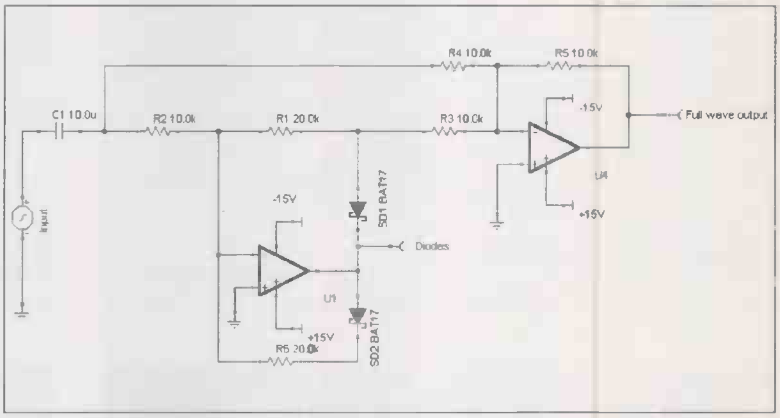


Figure 1: Classic fullwave precision rectifier.

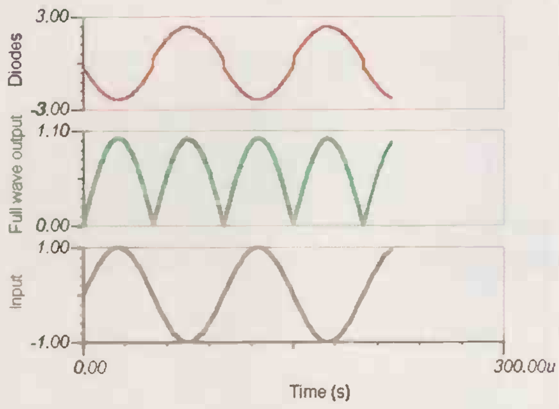


Figure 2: Classic full wave rectifier output.

Rectifier out-put stage

The differential output rectifier stage, uses local feedback pairs in an attempt match the 'rectifier gain' for each quadrant. There are three shortcomings with this circuit, which showed up in SPICE simulations.

Consider one compound pair, Tr4, Tr7. Degenerating the gain in both transistors is not necessary as there is 100% overall feedback applied to dilute the non-linearities in both transistors. The resistor R15 only suppresses precious loop gain and decreases the current transfer efficiency around the loop by raising the ac input impedance of the second transistor Tr7.

Even if the two compound pairs had infinite loop gain, we would still be left with a large dead-band around the null point. This is due to the comparatively large resistance value chosen for the emitter degeneration resistors R19 and R20. At the quiescent bias condition, the resistors equally share the output current. However, at either signal extremity all the output current will pass through one of the emitter resistors while the other compound pair is virtually turned off. This variation in current shifts the turn on threshold at each input, due almost entirely to the volt drop across R19 and R20.

Consider the Figure 3 Model of the output stage DC requirements. Assuming a typical beta of 100, Vbe for silicon of 0.6 Volt, and using the rule of thumb for transistor intrinsic emitter resistance re = (26 / Ie) (based on Schottky's diode law at room temperture where the emitter current Ie is in mA).

Examining the left-hand arm of the output stage Tr4 and Tr7 and letting output current = I_{out} (mA).

Let transistor current gain = 100, compound pair current gain = Ai = approximately Beta Tr4 x Beta Tr7 x say 50% current transfer at Tr7 base, then Ai = 100 x 100 x 0.5 = 5,000.

Max input voltage (seen from the preceding stage) with Tr4 on and Tr5 fully off:

Voltage input for full output = I_{out} (R10/Ai + R20 + R22) + re/Ie (Tr4)+ Vbe4. (Eq 1)

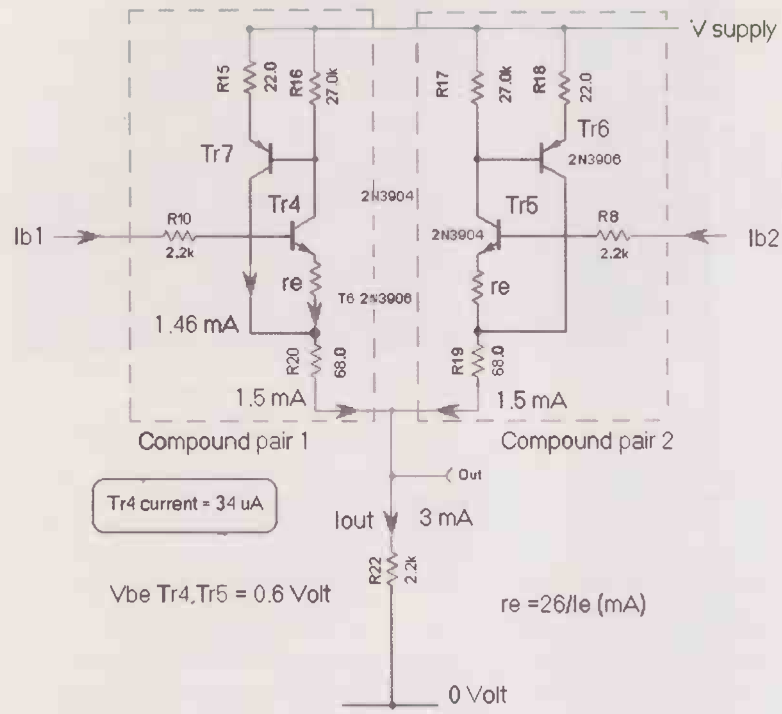


Figure 3: DC conditions of Mr. Haywood's output stage.

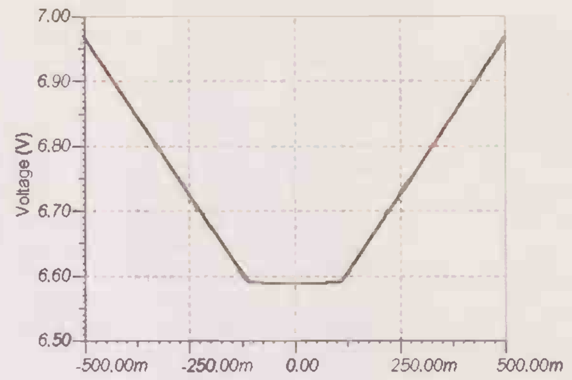


Figure 4: Deadband of 200mV in the original rectifier transfer characteristic

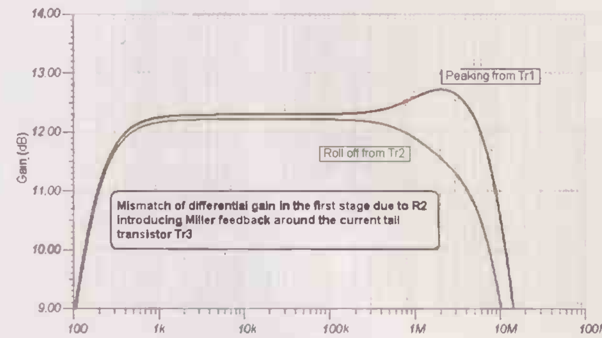


Figure 5a

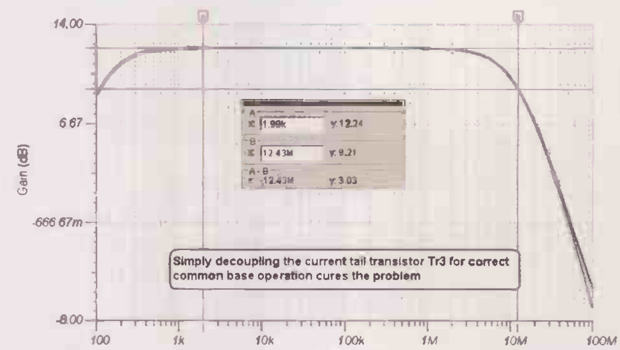


Figure 5b

Figures 5a & 5b: SPICE simulations demonstrating the increasing imbalance in differential gain.

At the mid point the two arms of the output stage equally share the output current, so assuming the compound pair gain remains constant with I_{out} and their Vbes (Tr4, Tr5) are equal;

Voltage input at the null point = (Iout/2) (R10/ Ai + R20) + R22. I_{out} + re/Ie (Tr4) + Vbe4. (Eq 2)

Now, assume the current in Tr4 is << Tr7, i.e. the bulk of the output current passes through Tr7, not through the re of Tr4. Running a DC SPICE analysis showed I_c of Tr7 = 1.46 mA and I_c of TR4 to be only 34.3μA. Hence, we can ignore the volt drop across re. Then:

Change in V_{in} = (Equation 1) - (Equation 2)

Delta V_{in} = I(R10/Ai + R20). $I_{out}/2$

As the compound pair current gain Ai, is very large, we can ignore the volt drop across R10, simplifying the change in V_{in} to:

Delta V_{in} = R20.(I_{out}/2)

For an output current of 3mA which is what Mr. Heywood's circuit runs at:

Rectifier stage dead-band, Delta V_{in} = 1.5(mA) x 68 Ohms = ±102mV

See Figure 4 of the SPICE simulation of the output stage differential DC transfer function about the DC null or steady state showing the dead-band discussed above.

This causes the output circuit to be 'blind' to the middle of the incoming signal, significantly reducing the dynamic range and progressively increasing low level distortion. This effect when referred to the input is diluted only a little by the modest voltage gain (7:1) of the preceding stage.

Looking at the compound pairs, the collector loads R16 and R17 are unnecessarily large. Here there are conflicting requirements as R16, R17 should be:

1. Lowest possible resistance, in order to rapidly remove base charge from Tr7, Tr6 for good high frequency performance.

2. Highest possible value, to efficiently transfer the current signal from Tr4 into Tr7 and achieve the highest current loop gain in the compound pair.

R15 and R18 are not a good idea as they not only suppress gain in the wrong place but also raise the input impedance of Tr6, Tr7 and further reduce the efficient transfer of signal current from Tr4, Tr5.

The third improvement would be to ac couple the long tail pair preamplifier to the output stage.

This blocks any unwanted DC imbalance in the first stage, which any way is ac coupled on its input so there is no point in preserving DC coupling with all the associated temperature drift problems.

The bias requirements of the output stage can then be optimised separately.

Differential pre-amp stage

Considering the long tail pair input stage the current tail transistor Tr3 should be operated as a constant current device for efficient current signal transfer at the emitters of Tr1, Tr2. This means operating Tr3 in grounded base to give the highest ac output impedance (around 1MΩ at low frequency for common base). This requires voltage DC bias of the base and de-coupling it to ac right at the base with a (low inductance) ceramic capacitor. R2 defeats this, allowing a 'soggy' operation somewhere between common emitter and common base, giving a less efficient constant current sink and worse allows Miller feedback around

Tr3 which adds a very undesirable capacitive lag across the current tail. This causes the high frequency gain to peak through Tr1 as it provides ac bypass to Tr1 emitter and to roll off at Tr2's frequency response by shunting the signal path to Tr2 emitter! This in turn, gives an increasing imbalance in the differential ac gain with increasing frequency. **See Figure 5**a and **Figure 5b** SPICE simulations demonstrating this effect. A minimal change is to de-couple Tr3's base. The high frequency bandwidth of the circuit is also limited by the unnecessary resistors R8, R10, which with 'circuit strays' and the input capacitance of the following stage form low pass RC filters.

There is also a second Miller feedback effect from the base collector capacitance of Tr1. Miller feedback is minimal at TR2 due to its de-coupled base and common base operation (with the long tail pair driven single ended). This second Miller effect can easily be demonstrated by driving the input from a low impedance generator rather than the 600Ω source used by Mr. Heywood. Compare **Figure 6** of the SPICE frequency response simulation of the first stage output, driven by a zero Ohm source with the 600Ω source performance of **Figure 5b**. Driving from a low generator source impedance 'absorbs' Tr1's base collector capacitive current. This effectively minimises the 'Miller effect' to the internal workings of the transistor. Adding an emitter follower to the input would be a practical way of achieving the same result.

Re-vamped circuit

With the above points in mind, I have re-vamped the circuit for interest sake, optimising with the aid of SPICE circuit simulation.

See the Figure 7 plot of rectifier gain versus Tr4, (and Tr5) collector loads R16 (R17) values. Examining the plot shows a rapidly diminishing return on gain increase with increasing load value. 3.3kW appears about the optimum value, giving near maximum gain while maintaining a much lower resistance value than used in the original circuit and therefore enabling a faster turn off response. See also Figure 8 of the re-vamped circuit and Figure 9, comparison of linearity with the original circuit at 500kHz. Figures 10a and 10b, comparison of frequency response with the original circuit.

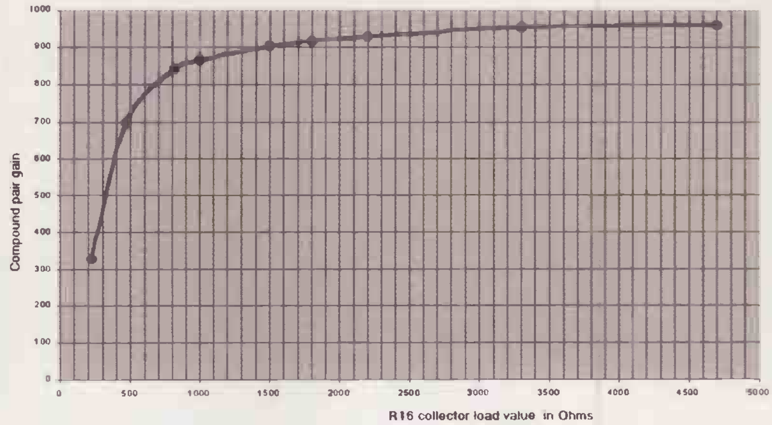


Figure 7: Gain versus R16 value.

Further development.

With bandwidth limited by the Miller effect in the first stage and wishing to find a simpler output stage, my thoughts turned to designing a rectifier output stage, which would use the Cascode principle. The 'Cascode' was an amplifier topology invented back in 'valve days' to overcome Miller feedback. Voltage generation of the signal at the amplifier's first stage output was avoided and hence there was no internal feedback through the anode to grid capacitance (or base collector in transistor talk). The Cascode was used universally as the front end RF amplifier in valve VHF/UHF TV tuners to achieve high gain at RF. See **Figure 11**. The first stage of triode amplification was fed directly into the low ac impedance of the cathode port of a second triode valve, operating in common grid (common base, in transistor talk). The first valve gave no voltage amplification but very high power gain due to the amplified signal current from the valves mutual or transconductance, gm. The second stage had no Miller limitation due to the grounded control grid, preventing any anode to grid Miller capacitive feedback. The common grid topology has high output impedance (analogous to transistor common base), allowing high voltage amplification to be achieved. The cascode principle adapts readily to transistor circuits with the advantage of folding the circuit, avoiding build up of DC levels by using complimentary PNP devices for the second stage. They didn't have the advantage of a 'PNP valve', hence the valve circuit stacked up in its DC requirements. **Figure 12** shows my use of this technique with the output stage configured in differential common base. The low impedance of the PNP emitters clamp the first stage output signal voltage so that the voltage change becomes minimal but near linear signal current is transferred into the output circuit. AC coupling and the high value emitter bias resistors allow each PNP transistor to be accurately biased on the verge of conduction. As soon as each amplified signal from the first stage swings positive the relevant PNP transistor conducts and the signal current flows on into the output resistive load. Common base operation ensures the PNP transistors will have very closely matched gains. Because hfb = hfe/(hfe +1) and with hfe variations of 100 minimum to 300 typical for the 2N3904 devices used, the common base gain or

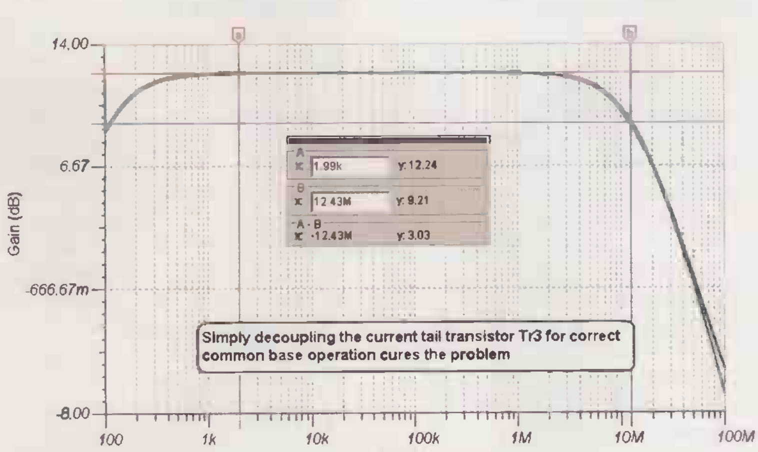


Figure 6: Proof of the unwanted Miller feedback.

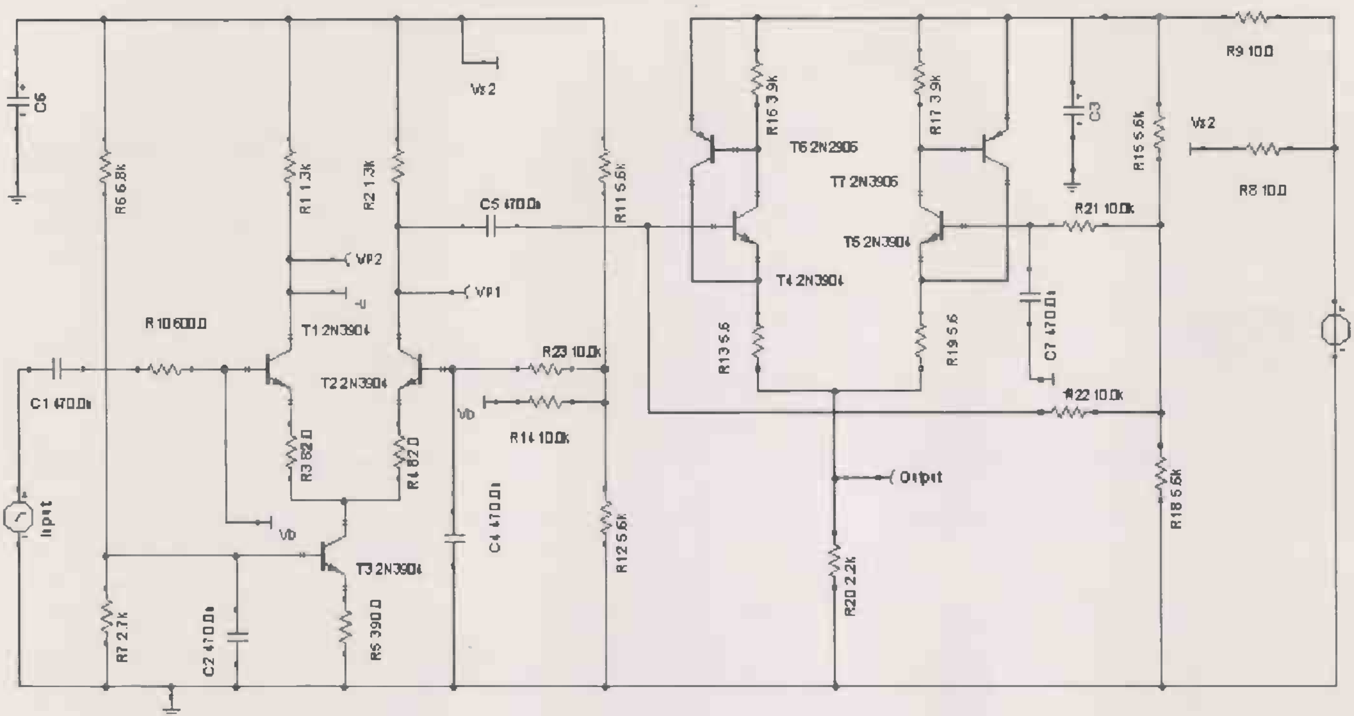


Figure 8a: Revamped circuit.

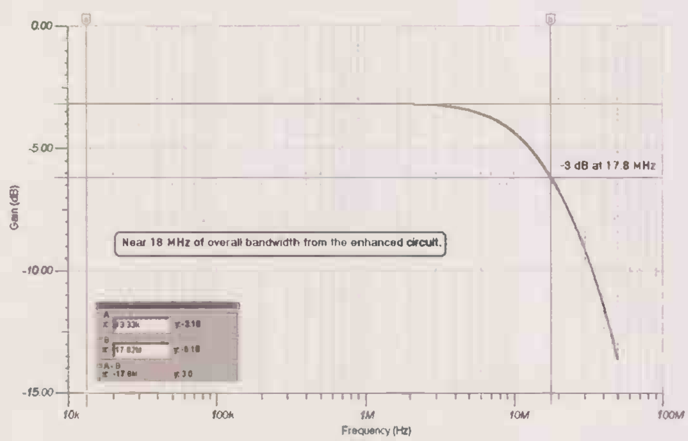


Figure 8b: Overall bandwidth of enhanced circuit.

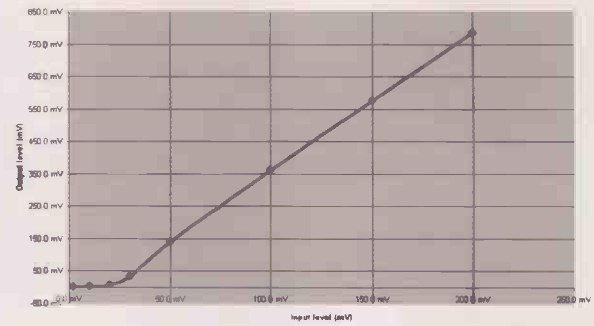


Figure 9a: Original circuit linearity at 500kHz.

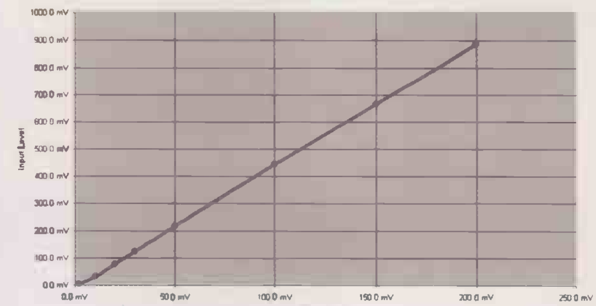


Figure 9b: Revamped linearity at 500kHz.

emitter efficiency will only vary around 0.9901 to 0.99668.

The common base operation also enables high voltage gain to be achieved due to the inherently high output impedance of around 1MΩ at low frequency, allowing a high collector load value. The non-linearity of the Vbe characteristic is effectively diluted by the ratio of output impedance of the first stage (defined by the collector loads of Tr1, Tr2) and the low intrinsic re of the PNP devices. While this circuit is not as linear as the enhanced compound pair approach, it is considerably more linear than the original circuit having a much smaller dead-band of only 10mV. The PNP approach has the potential to give wider bandwidth.

See Figure 13 of the simulated linearity at 500kHz showing non-linearity at very low levels (where re will be large and current gain at its lowest) and the simulated drive and output waveforms at 500kHz (Figure 14). Note the clamping of the pre-amp output voltage on each positive half cycle where the associated PNP turns on. The active part of each signal offers little voltage variation and hence minimal Miller feedback, allowing near full bandwidth to be achieved on the positive half cycles. What happens on the negative cycles is a 'don't care' as the corresponding output device is shut off. This allows some over loading of the first stage to occur on large signals, with the input transistors bottoming on the unwanted negative half cycles. This effectively increases the dynamic range at frequencies where the propagation delay of T1 and T2 can be ignored. Finally a spare NPN transistor (the original circuit uses seven transistors) is used as an input emitter follower to provide a low AC impedance drive, of around 15W to the long tail pair, further minimising Miller feedback. This will also raise the input impedance of the input circuit to over 50kW with the aid of 'bootstrapping', eliminating the loading of the input bias chain from about 10kHz. Stray capacitance of 1pF has been assumed in the simulations across each resistor. Circuit strays have not been included in the simulations, as this will depend on layout.

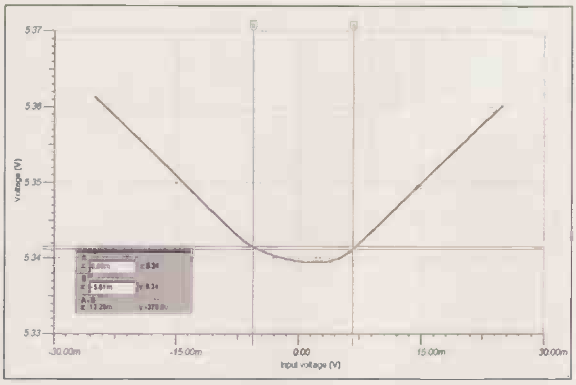


Figure 10: Reduced dead-band enhanced circuit.

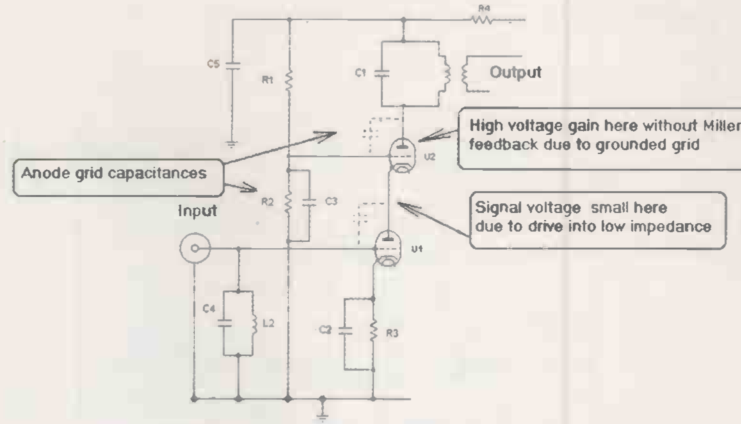


Figure 11: Outline of original valve cascode RF amplifier.

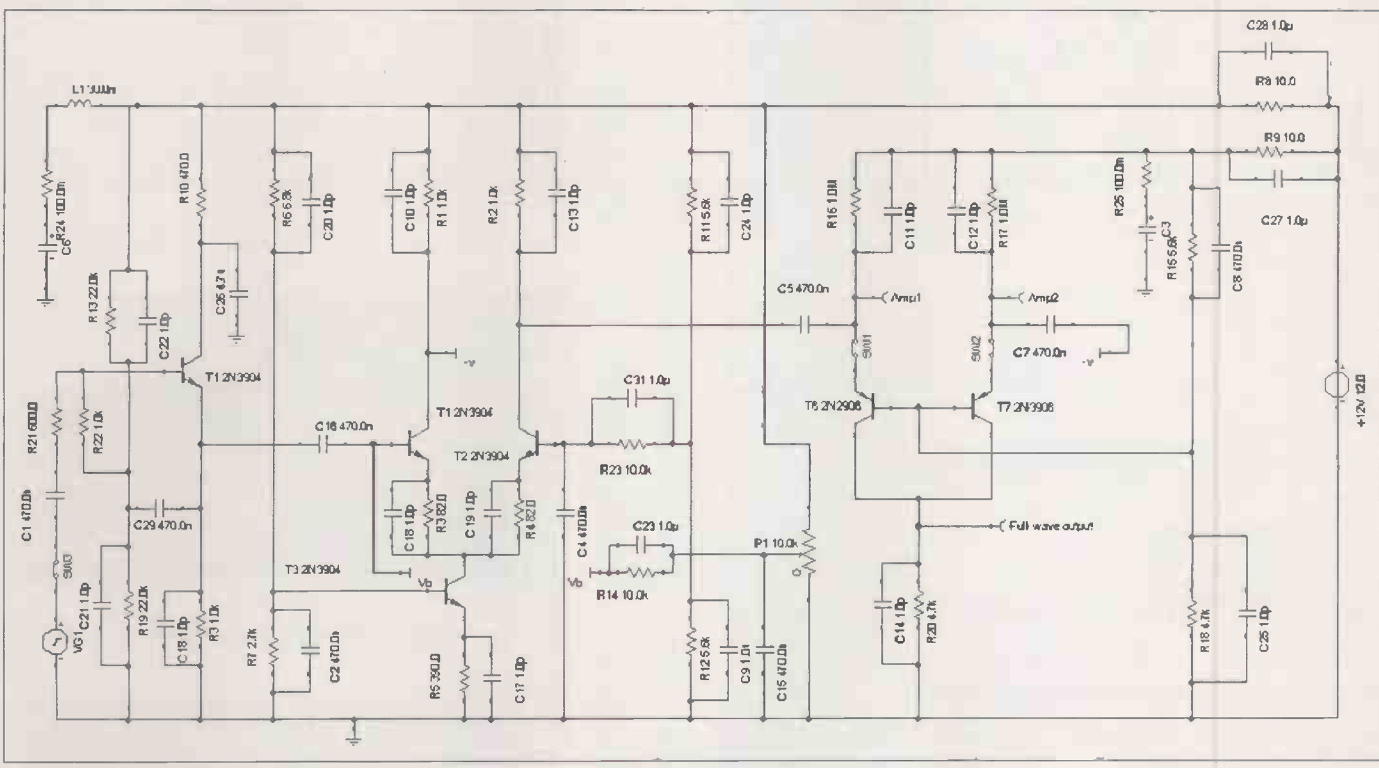


Figure 12: Circuit of folded cascode approach.

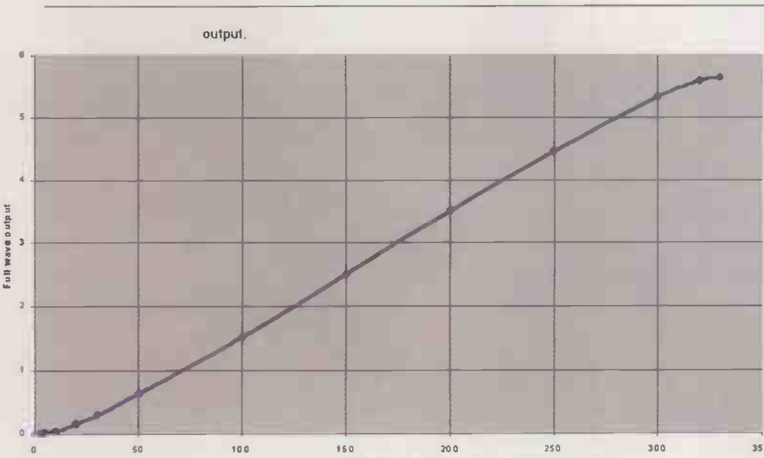


Figure 13: Linearity at 500kHz of the enhanced circuit using the PNP rectifier output.

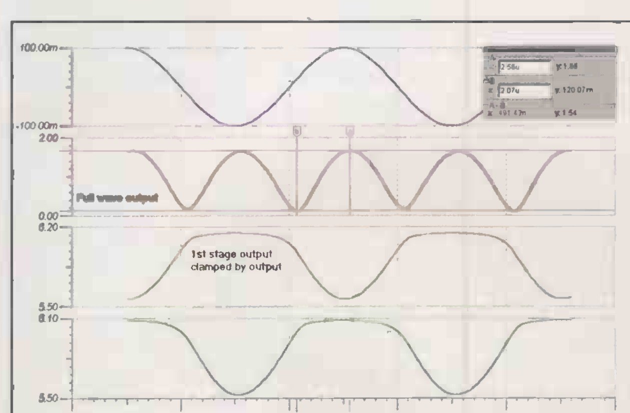


Figure 14: Folded cascode waveforms at 500kHz.

Word on bread boarding

My own bread board method today is to glue surface mount components using 'super glue' to industrial fibre glass FR4 board with copper on the opposite side to serve as the reference (ground) plane. Unpopulated etched boards can also be used with the green masking serving as an insulating barrier. This has perfectly adequate insulation for low voltage circuitry.

If space is not an issue use 0805 size passive chip components as they are easier to manage than the smaller 0603 size components. Use the smaller 0403 components only if you have bionic eyesight! Wire point to point to the chip ends using the fine Kynar insulated wire available from RS or Farnell components. Glue down the wires to the required layout. Keep wiring as short as possible, especially to inputs of active devices.

I have found bread boarding like this gives a reasonable approximation to a final PCB layout using a ground plane.

Note on Miller feedback

This is the effect that unless prevented, kills bandwidth in any voltage amplifier.

Assume we have an amplifier device with a voltage gain Av of 100 and ideal infinite input resistance with zero output impedance. It has unwanted feedback capacitance between the input and output terminals of Cf. The capacitance will cause feedback signal current from output to input. Usually, this feedback capacitance is small say 2pF. The capacitor current will be proportional to the voltage across the capacitor, which in our case is

$Vin -(-Av. Vin)$ or $Vin(1+Av) = 101\ Vin$

If the capacitor volt drop has increased 101 times due to the amplifier gain then the feedback capacitive current will be 101 times larger for the same input voltage. The feedback capacitance Cf, now looks 101 times bigger at the amplifier input! The problem occurs when we drive the amplifier input from a real world generator of finite source impedance Rs. With no voltage gain, the capacitance will be the input capacitance (Cin +Cf) which will form an RC lag with the generator source impedance, giving in turn a low pass RC filter.

$-3\ dB\ bandwidth = 1/(2\pi\ Rs\ (Cin + Cf))$

If we now add gain Av, the bandwidth will shrink accordingly as

$-3\ dB\ bandwidth = 1/(2\pi\ Rs(Cin + Cf(1 + Av)))$

The bandwidth has now reduced in proportion to the voltage gain of the amplifier, in our case by one hundred times! This occurs inside any bipolar transistor due to the collector to base capacitance and the base spreading resistance rbb giving a minimum input source impedance even when voltage driven. This is why the common emitter gain of a transistor is often considerably less than its transition or unity gain frequency would imply.

A curious new result in switching theory

The following account relates how a puzzle brought to light a remarkably simple, highly intriguing, probably useless, but undeniably fundamental new result in switching theory. Spice is added to the story through the role played by construction of a wildly improbable electronic device in helping to establish the new finding. 'Switching theory' has a slightly old-fashioned ring to it, what exactly does it signify? A brief remark on this and a couple of related matters will set our subject in perspective and prepare the way for issues arising later. Lee C.F. Sallows explains

"Gödel turned out to be an unadulterated Platonist, and apparently believed that an eternal 'not' was laid up in heaven, where virtuous logicians might hope to meet it hereafter." – Bertrand Russell[1].

Computer science emerges into view as a separate discipline from a cluster of related topics, chief among them symbolic logic, Boolean algebra, switching and automata theory. Logic, originating with Aristotle, concerns the study of deductive inference, of the conditions of truth-preservation in deriving one statement from another. More than two millennia following Aristotle, George Boole was to design his algebra to model logic, a step largely intended to replace reasoning with calculation, with the rule-governed manipulation of symbols. Boolean algebra, we remind ourselves, comprises a so-called *formal system*: a well-defined set of signs and conventions by means of which, starting with certain symbol strings, certain others may be legally substituted, the latter being deemed equivalent to the former. No meaning is attached to these transformations, except in the loose identification of sign with signified usual when *applying* such formalisms to external systems (such as logic). Whether the algebra applied really is an accurate model of the system in question is of course a problem not resolvable within the algebra itself.

A notable success in the practical application of Boolean algebra occurred with the appearance of C.E. Shannon's *Symbolic Analysis of Relay and Switching Circuits* in 1938[2]. Ever since, the analogy of '0' and '1' with open and closed switch contacts and of series/parallel switch connections with AND/OR Boolean operators has been a stereotypical textbook example. Then, as today, a *relay* was an electromagnetically operated switch, a device opening up new realms of complexity in the possibilities it offered of switches controlling still other switches in endlessly convoluted networks. The problems thrown up in this new domain soon became the concern of 'switching theory'.

Ten years following Shannon, switching theory advanced to a new level of maturity with G.A. Montgomerie's *Sketch for an Algebra of Relay and Contactor Circuits*[3]. By now a vital distinction had been recognised in the division of networks into *combinational* and *sequential* types.

Combinational circuits were those in which the open or closed states of every switch depended purely upon current input values (0,1) to the network. A Boolean formula, simple or complicated, would always describe this relation satisfactorily. Sequential circuits, on the other hand, were those whose response to input patterns also depended in part on their past history: on the foregoing *sequence* of values presented. The behaviour of the circuit might thus change significantly after receipt of some critical input, the latter event thereby being in some sense 'remembered'. In fact *memory* (introduced via feedback effects) was the key property of such networks. Flow tables and state transition diagrams now displaced static formulas in the need to capture this temporal context-dependent behaviour. Thus was launched the study of what came to be called sequential or *finite state machines*, a field later to be known as automata theory.

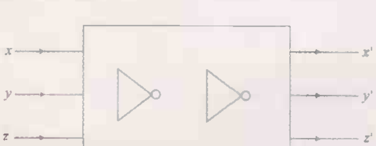
The progress of developments in automata theory is beyond our purpose here: advances were rapid, leading to theoretical results of great moment in connection with Turing machines and mathematical linguistics, the subject soon shading seamlessly into computer science proper. Back in the mainstream of switching theory however, by the 1960s advances in technology had shifted emphasis away from relays and onto 'electronic digital logic' realised in micro-packaged integrated circuits or 'chips'. Mechanically actuated contacts gave way before 'AND-gates' and 'OR-gates' etc., the binary states (0,1) of whose input and output lines were represented by two discrete voltage levels. Soon Boolean algebra was a standard item on the training syllabus of electronics engineers; formerly recondite chapters of the now slightly outmoded-sounding 'switching theory' became the stock-in-trade of every technician.

Hence, overtaken by studies into the more challenging finite state machines, as a subject of research, switching theory dropped into the background, furnishing instead a well-knit body of established results that found daily application in electronic logic design. This is not to say that all the theoretical questions raised had been successfully answered. Many problems, especially in the area of minimization, remained unsolved; later these would provide a point of departure for the currently vigorous *theory of circuit complexity* (see reference [4]), a field closely related to, yet historically distinct from the old switching theory. In any case, mass-production techniques had extinguished any practical need for such solutions. Gone forever was the pioneering impetus of the early days.

Who then would have expected to stumble across an undiscovered nugget still reposing amid the slag-heaps of this abandoned mine?

A Knotty Problem

Recently browsing through *A Computer Science Reader* (Selections from *Abacus*, Springer-Verlag 1988), my eye was caught by an article on Automated Reasoning by Larry Wos[5]. Wos illustrated the working of his reasoning program by means of a few example problems, one of which immediately captured my attention. It was this:



The black box above receives binary inputs (0, 1) at x, y and z. Each output line yields the complement of the corresponding input; that is, if x is 0, x' is 1, and so on. Each of the eight possible 3-bit input words thus gives rise to its complementary word at the outputs. Normally speaking such a transfer function would be achieved by using three inverters (NOTs) connected between each input and output.

Problem: Design a network using any number of AND and OR gates, but *not more than two* (2) NOTs to achieve exactly the same input-output function. (The ANDs and ORs may have as many inputs as required.)

Now relays, gates, switchery and logic hold a powerful fascination for some. The possibility of simulating three inverters by means of two had never so much as crossed my mind before; the bare contingency hinted indefinably at something wonderful. It seemed to call for ingenious circuitry. The puzzle had me hooked in no time.

It turned out to be a far tougher conundrum than first imagined. So much so, in its elusiveness it became hypnotic. In fact, on and off I took almost a fortnight to solve it, succeeding even then only through reasoning aided by trial and error. But the solution was worth waiting for: an intricate network of true Platonic elegance and inevitability. It is a logical constellation that was always there, sooner or later someone was bound to find it: a sheer poem for the switching theorist. As the sequel shows, the name of the man who *did* find it first turned out to be Edward F. Moore, a distinguished pioneer in the field of automata theory. From now on I shall refer to the basic arrangement as Moore's circuit. Incidentally, Wos's automated reasoning program was successful in solving the problem; his method being too complex to outline here, a detailed account can be found in reference [6].

One version of Moore's circuit is shown in **Figure 1**. The network admits of a number of (essentially minor) variations, some more economical in gates than others; our example is picked for its functional clarity. Interested readers might like to seek for a more parsimonious circuit using one gate fewer than **Figure 1** (multi-input gates then being counted as if built up from 2-input equivalents; **Figure 1** thus containing 11 ANDs and 14 ORs). In view of its importance to what follows, a few comments on Moore's circuit will be worthwhile.

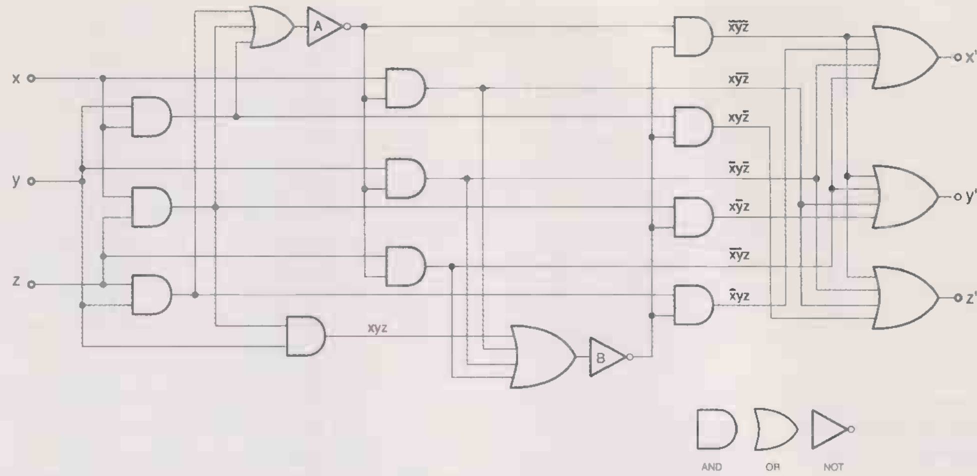


Figure 1: Moore's circuit

Central to every variant of Moore's solution is circuitry leading to a binary representation of the number of zeros present in the input word (xyz) by the four possible states of the two inverter outputs: 00 = none, 01 = one, 10 = two, 11 = three zeros. Simple as this may seem, there is but a single way to achieve it. In effect, each inverter's output state (0 or 1) must represent a classification of xyz according to whether the number of ones it contains falls in the top or bottom row (first inverter), and in the left or right column (second inverter) of the following table:

		B: 1	B: 0
A	1	0	1
	0	2	3

In this way the intersection of A's row and B's column choice pinpoints the number of ones (and thus, zeros) in the input word.

In our circuit, use of AND gates to combine this information with the specific input pattern enables a complete *decoding* of the input word. See how each of the seven lines feeding the three OR gates at the right is uniquely activated by a different input word (indicated). The circuitry to the left is thus a '3-bit to parallel decoder'. Note that although available, the eighth line ($2^3 = 8$) is unused since, when active (i.e. when

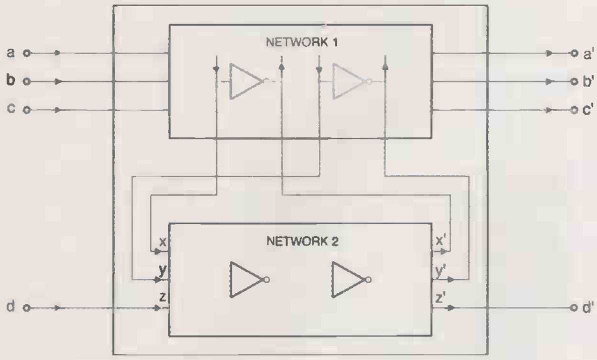


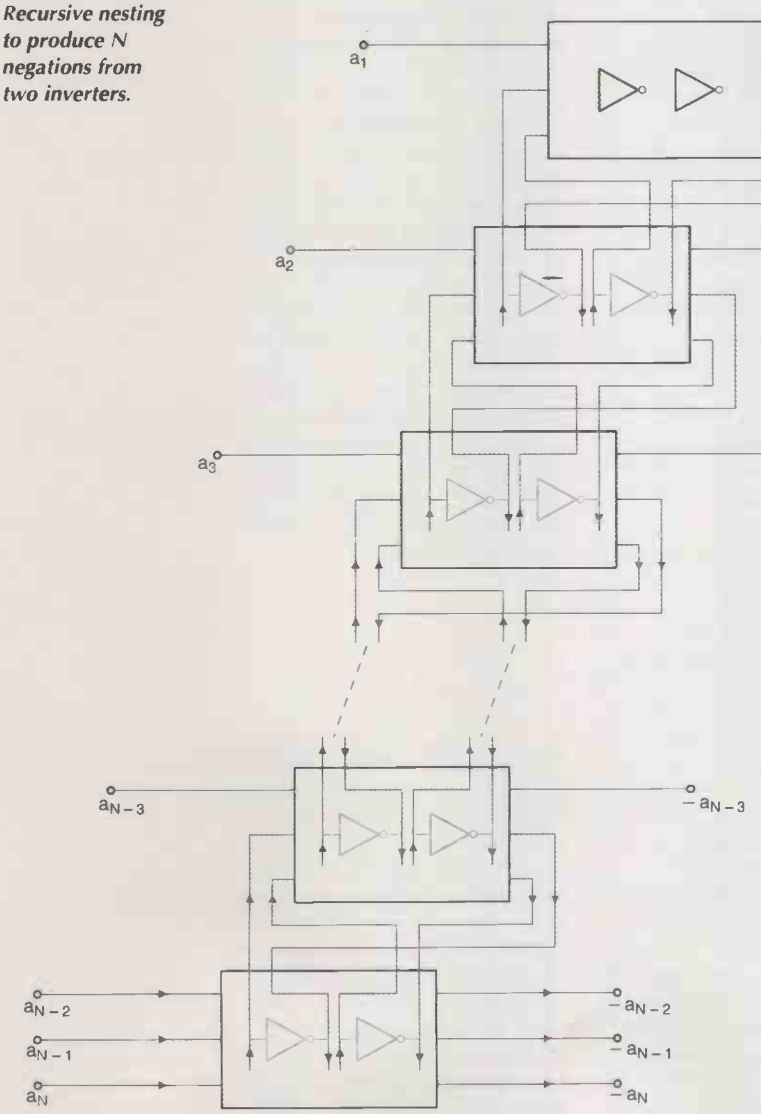
Figure 2: Four NOT-functions from two inverters.

x = y = z = 1), all outputs are to remain 0.

Similarly, the three interconnected output ORs comprise a 'parallel to 3-bit re-coder', the coding in this case ensuring that xyz inputs that are 0 result in corresponding outputs that are 1, and vice versa: an active '$x\overline{yz}$' line turns on outputs y and z, for instance. A point to observe though is that alternative OR combinations could replace (or supplement) this one to produce any desired input-output functions: an output word may have as many bits as we please, and distinct recoders working in parallel could realise unlimited *simultaneous* output words, if required. Already one senses a surprising latent potency here, although, as we shall see, most of the magic in Moore's circuit lies exactly in the mischievous recoding he *did* choose.

Speaking of coding and recoding serves to recall that a circuit diagram is a kind of coded representation and thus itself capable of translation into different symbol systems. A change of medium often brings new aspects into view. An obvious alternative in this connection is Boolean algebra. Re-expressing Moore's circuit in these terms is a mere mechanical exercise.

Figure 3: Recursive nesting to produce N negations from two inverters.



Designating the output of inverter A as *A*, for instance, we can work backwards through the circuitry towards the inputs, transcribing directly as we go:

A = Not[(x & y) Or (x & z) Or (y & z)].

Comparing formula with circuit we find the inverter is replaced by Not, the 3-termed, square-bracketed Or expression deputizes for the OR-gate wired to its input, and the three parenthesised terms stand in for the AND-gates communicating between the input pairs xy, xz and yz and the OR inputs. Note how the nesting of expressions reproduces the pattern of outputs feeding into inputs in the circuit. We are looking at a fragment of Moore's circuit written in a different language.

Analogously, and taking advantage of the above, a compact expression representing the output *B* of inverter B can also be written:

B = Not[(x & A) Or (y & A) Or (z & A) Or (x & y & z)].

Note how the presence of *A* as an argument in the function describing *B* is more than a convenient abbreviation, it reflects *A*'s antecedence in the signal processing path: the value of *A* must already be available in determining that of *B*, but not vice versa, a point we shall have cause to recall later. However, the real convenience of these partial descriptions becomes clear in the crisp encapsulation of the complete Moore circuit they now facilitate:

x' = [(y & A) Or (z & A) Or (B & y & z) Or (A & B)]

y' = [(x & A) Or (z & A) Or (B & x & z) Or (A & B)]

z' = [(x & A) Or (y & A) Or (B & x & y) Or (A & B)]

See how the equations expose a (predictable) three-fold functional symmetry hinted at, but less successfully conveyed, by their equivalent circuit diagram, an obfuscation resulting from the latter's confinement to two dimensions. (An amusing exercise is to design a 3-D version of the circuit recapturing the trilateral balance.) Still later we shall have occasion to recall these formulas. So much then for a preliminary look at Moore's circuit.

Networks and Notworks

This was all fine as far as it went: an intriguing puzzle with a beautiful solution, if lacking in practical application. During an early stage in reaching that solution however, a rather astounding thought hit me. As an electronics engineer, the idea occurred to mind quite easily and, although perhaps ingenious in small degree, is certainly no creative *tour de force*. Nevertheless, the implications struck me as luminous and compelling. The idea was simply this: If it is possible to simulate three independent NOT-functions using only two primary NOTs (or real inverters) then couldn't we *use* two of those three in order to simulate a *second* set of three NOT-functions? At this stage, having used only two of the first set of three, there would still be one over. That means that a total of FOUR independent NOT-functions would have been simulated while still using only two real inverters. **Figure 2** makes the proposal explicit.

Consider the circuit shown. Network 2 is the straightforward Moore circuit; as such its behaviour is functionally equivalent to an outwardly similar box containing three separate NOTs or inverters connected between each of its three inputs and outputs.

Network 1 is identical to Network 2 except that its two inverters have been removed. The internal input-output connections normally made to the missing inverters have been brought out and connected instead to two channels of Network 2. Network 2 thus furnishes the two NOT functions required for normal working of Network 1 (channels *a, b, c*) while still leaving a fourth independent complement function over (channel *d*). That is all.

The ramifications of this stratagem ripple swiftly outwards. For clearly the four newly created NOT-functions can again be nested in an endlessly expandable recursive hierarchy to produce an unlimited number of independent negation functions; see **Figure 3**. In other words (and striving for the infinite in the name of logic):

Theorem I

In any universe, exactly two fundamental negators suffice for concomitant synthesis of all others.

But this soon leads us to a couple of other interesting consequences:

Theorem II

A device whose input-output relations are described by some system of Boolean functions is always constructible using a network comprising some number of AND- and OR-gates but no more that two inverters.

Or, still more ambitiously, (and relying on other well-known results in the field):

Theorem III

Every possible finite state machine (automaton) is realisable using no more than two primary complement functions.

Am I alone in continuing to feel a sense of wonder in this simple discovery?

As I say, the idea for the above configuration occurred to me at the time of reading Wos' article, even before solving his problem. Taking it to be a merely personal rediscovery of a presumably well-established result in logic, thought of any further development never arose. Being satisfied the idea was sound, as an engineer I felt only sheer surprise that, in principle, all the millions of inverters in use throughout the world could be 'seeded' from a single pair. Having a romantic turn of mind, it conjured an imaginative vision of a sort of Yin-Yang dyad of inverters occupying a dusty, temperature-controlled glass case at the National Bureau of Standards. Wires leading away from the four old-fashioned knurled brass input and output terminals lead off for distribution to other boxes scattered about the nation. (I should say *five* terminals: a 'common' or reference would also be required.)

Well-established result or no, the self-duplicating inverter circuit was a revelation to me and continued to exercise fascination. Having nothing better to do, for fun I typed out a devilish new version of Wos' problem, sending it around to tease friends and colleagues at computer science and mathematics departments at the University of Nijmegen. In the new version, otherwise identical to the old, *four* complement functions are to be realised instead of three. As before, of course, only two inverters are allowed. (As a matter of fact, by Theorem II above, the input-output functions demanded by any severer version of the problem could be made as complicated as one wished. Asking for four NOT-functions is the obvious choice, this representing the least jump in difficulty at the new level of complexity.)

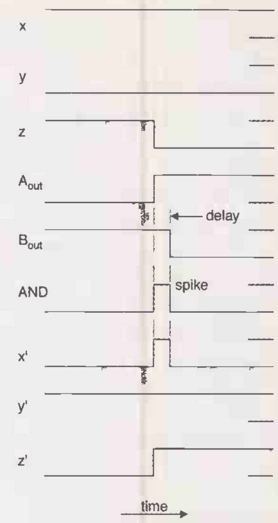
In a few cases the response to this teasing was sharper than anticipated. I suppose the problem is so clear-cut and inescapable it poses a provocative challenge to one's self-estimate as an engineer, mathematician, logician or whatever. Prevarication in the face of this kind of simplicity is difficult; admitting one cannot solve such an apparently elementary problem, even more so. The trouble is, unless you happen to be aware of Moore's circuit (as most people are not), the two separate insights needed for reaching the solution put it well beyond all reasonable ingenuity. It would be a creative act to re-invent Moore's circuit from scratch; penetrating to the fact that such a circuit is necessary as a *component* in the 4-complement configuration asks too much of human imagination. In light of this, some of the scepticism poured on my assurances that the solution was complex but straightforward, involving absolutely no hanky-panky, becomes explicable.

It was at this stage that Hans Cornet, a mathematical friend at The Hague, ran across what proved to be the original source of the 3-complement problem. This was in Marvin Minsky's book *Computation: Finite and Infinite Machines* (Prentice-Hall Inc., 1967, p. 65), a confirmation of my assumption that Wos had merely borrowed rather than invented the problem. Looking up Minsky's book in Nijmegen I learned the problem had first been 'suggested by E.F. Moore'. Admittedly the solution circuit (shown only in skeletal form) is not overtly attributed to Moore but surely no one could pose such a riddle without first having unravelled it?

A comment by Minsky following the problem statement drew from me an appreciative smile: "The solution net ... is quite hard to find, but it is an extremely instructive problem to work on, so keep trying! Do not look at the solution unless desperate." It was a final remark of his however, that brought me up with a jolt. With deepening puzzlement I ran my eye again and again over his two terminal sentences: *To what extent can this result be applied to itself - that is, how many NOTs are needed to obtain K simultaneous complements? This leads to a whole theory in itself; see Gilbert [1954] and Markov [1958].*

Clearly the sufficiency of two NOTs in obtaining *K* (an arbitrary number of) complements was unknown to Minsky. Yet to speak of "applying the result to itself" was a pretty reasonable description of exactly the trick used in my 4-complement circuit. How *could* it be that he had envisioned the self-same possibility without ending up at the same idea? Why on earth should a "whole theory" be required?

My thoughts sped back to those sceptical friends who could "almost *prove* your 4-complement problem is insoluble". Previously I could afford to be smug, now it was me against Minsky, Gilbert and Markov — the latter a name of intimidating



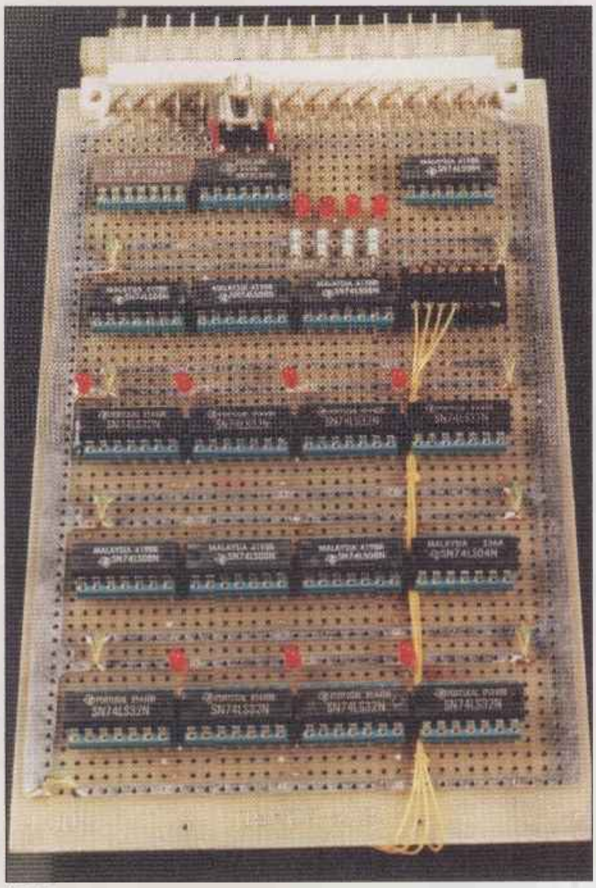
Right – Figure 4: Race condition – input word xyz changes from 101 to 100. Delayed reaction of second inverter (B) to first (A) causes brief pulse at the output of the AND to which they are connected

authority in the world of mathematics. Was it likely his theory would turn out to be wrong? Hadn't I after all overlooked some inherent logical flaw that rendered reflexive re-application of the circuit to itself in fact unworkable? I lost no time in hunting up the papers from Gilbert and Markov. Alas, the journals were not available in Nijmegen; there was nothing for it but to order copies. That would take a week or so. In the meantime I returned to the 4-complement circuit, re-examining it from every angle.

Later that evening I banged a defiant fist on the table. It was no good: Markov or no Markov, theory or no theory, there was nothing wrong with that circuit: it *had* to work! — And why not demonstrate my reasoning agreed with reality by *building* it? The very next day saw me launched on construction.

The 4-Complement Simulator

Physical realisation of the circuit followed conventional electronic practice. Taking standard TTL integrated circuits lying to hand (six SN74LS08s and eight SN74LS32s: 14 pin packages containing four 2-input ANDs and ORs, respectively) and a prototype-development printed circuit card fitted out with 14-pin chip holders, using a wire-wrap pistol to make interconnections, assembly was completed within a matter of hours.



An obvious approach in implementing the device was dictated by the very principle of operation: first build and test two quite independent Moore circuits, afterwards remove the inverters from one (a single SN74LS04 chip) and replace with connections to two inputs and outputs on the other. This is exactly what I did. In the photograph below, the twin Moore circuits are formed by the two groups of eight chips furthest from the connector. In one circuit, four wires leading from the underside of the card to a small plug that replaces the discarded inverter chip are plain to see.

Finally, to facilitate testing, a push button controlled 4-bit binary counter and a sprinkling of light-emitting diodes (LEDs) were added. Successive presses on the button (seen adjacent to the main connector) run the counter through 0000, 0001, 0010, .. , 1111, the sequence of sixteen possible 4-bit words. Counter outputs are wired to the four NOT-simulator inputs, the presently activated word being indicated by a line of four adjacent LEDs situated close by (on = 0, off = 1). Six remaining LEDs dotted about the board report on the high/low status of the 2 X 3 Moore circuit outputs. For ease of comparability one of these is duplicated so as to form a single line of four evenly spaced LEDs monitoring the four main outputs.

These additions account for two of the three extra chips at one end of the board: an SN74LS93 binary counter and an SN74LS00 4 × two-input NAND used as a so-called set-reset flip-flop to eliminate push-button contact bounce problems. The need for still a further chip made itself felt when, having completed and tested the two separate Moore circuits, the final 4-complement simulator produced by combining them failed to work as anticipated!

At first this was unnerving. Using an oscilloscope, however, the source of the trouble was soon tracked down: under certain input transitions Moore's circuit exhibits *race conditions*. Race conditions arise when delays introduced by hardware inertia result in unintended overlaps between logical state durations, leading to transitory 'spikes' or pulses of very short duration (the antecedence of inverter A in the signal processing path now shows its significance; see **Figure 4**). Such spikes can be innocuous enough in many applications, but not so in the 4-complement simulator. Here, a spike emerging from output x' of the nested circuit becomes gated through the outer circuit to the input of the second inverter (B, see **Figures 1 and 2**) - itself, however, now simulated by channel *y* of the nested circuit. Our spike, in other words, traverses a sneaky feedback loop and now finds itself re-entering an input of the inner Moore circuit! A vicious circle has been established: regenerative oscillation sets in.

Notice that the culprit here is not the feedback loop — an intrinsic feature of the nested scheme (to which we shall return) — but the pulse generated by the race condition. Happily, a cure is easily effected through interposing a delay in the appropriate line (connecting the output of inverter A to the AND-gate input so as to ensure the latter cannot receive a 1 from the former until after the output of inverter B has changed to 0). This accounts for the last remaining chip in the photo (another SN74LS08; four ANDs connected together head to tail, each contributing its own share to the aggregate delay thus created). With this modification completed, turning on the power once again, I finally had the satisfaction of verifying a perfectly functioning 4-complement simulator. It was a happy moment of vindication and triumph.

The 4-complement circuit thus stood acquitted — though in hindsight it is amusing to recall exultation on completion of one of the most futile or, at least, redundant items of electronic apparatus ever constructed! The Great Unanswered Question now remaining, however, was how this success could ever be reconciled with the apparently contradictory theory of Gilbert and Markov? The working device was an unshakeable fact, yet a theorem in logic cannot be validated via any empirical demonstration, however suggestive. Could some sort of disillusionment still lurk in the publications awaited?

A Gordian Not Unravelled

Following eventual receipt of the anxiously awaited material, a rapid glance at Markov's and Gilbert's conclusions confirmed Minsky's original remark: blatant contradiction of the two-inverters-always-suffice idea. Steeling myself to the mathematics, I settled down to read. Gilbert's is the earlier, exploratory paper, his partial result later subsumed by Markov's more embracing work, *On the Inversion Complexity of a System of Functions* (translated by Morris D. Friedman). We confine ourselves to the latter.

Markov begins his monograph with a series of careful definitions. A small *alphabet* of the signs familiar from Boolean algebra is introduced, *constants* and *variables* included: {0, 1, x_1, ... , x_n , &, Or, Not, (,)}. Certain *words* or strings of these are specified as *formulas* and *sub-formulas*, *negative sub-formulas* being characterised as those prefixed by 'Not'. The so-called *inversion complexity of a system of sub-formulas* is now identified with the number of distinct negative sub-formulas occurring in it.

My précis lacks his precision, but the outline of what is going on here is already clear: substituting concatenations of discrete symbols for the tangled Celtic knotwork language of the switching engineer, Boolean formulas replace circuit diagrams: 'Nots' are to be counted instead of inverters.

So far so good. Moore's problem itself might well have been so reformulated as to ask for a system of Boolean functions equivalent to x' = Not(x), y' = Not(y), z' = Not(z), but in which 'Not' (preceding a distinct sub-formula) would occur no more than twice. Our previously derived set of three formulas describing Moore's circuit is just such a solution. As before, we are merely talking about the same thing in a different language.

Markov's list of definitions ends abruptly with a bold statement of his result, followed by a one-page lemma running into sub-subscripted, sub-superscripted variables that "plays an essential role in the proof". The full proof is spared us — the author doubtless feeling that a recapitulation of the obvious would be too tedious — and so ends his paper. It is just as well: that lemma might have been written in Celtic for all I could make of it (printing errors abound too). Not that I questioned his result for a moment. This was a good instance of what Richard Guy calls *proof by intimidation*.

But what was that result? Following Markov we must be quite precise here.

Consider a system of *m* Boolean functions of *n* arguments. It can be defined by different systems of *m* formulas in *n* variables. Take now a worst-case instance of such a system of functions in which the number of distinct negative sub-formulas necessary to their definition is at its greatest. Then, says Markov, the least number of negative sub-formulas that will have to appear in the formulas defining the functions will be $\|\log_2 n\|+1$ = the number of digits in the binary representation of *n*. (The vertical strokes indicate the truncated value of $\log_2 n$)

In other words, $\|\log_2 n\|+1$, otherwise known as *I* or the inversion complexity of the system of functions, is indeed the Markovian equivalent to the minimum number of separate inverters that would be required in any network implementation of its formulas. Note that *m*, the number of functions (or formulas) does not actually enter into it. (Think of all the recoders that can be connected to Moore's 3-bit to parallel decoder, each yielding a new output function, none demanding extra negations).

We can examine this further by taking Moore's problem as an example. Translating into Boolean terms, our question concerns a system of three functions (x' = Not(x), y' = Not(y), z' = Not(z), of three arguments x, y, z). Applying Markov's result we find $n = 3$, $\log_2 3 = 1.5849...$, hence $I = 1 + 1 = 2$. That agrees with our conclusion: two inverters sufficient.

But what about the 4-complement problem? Now $n = 4$, $\log_2 4 = 2$, $I = 2 + 1 = 3$. Three inverters are required. That disagrees with our conclusion. In effect, Theorem I above would assert that $I = 2$, irrespective of *m* and *n*. Here is the contradiction.

The collision here is so acute that something will have to give way. And so it proves. Forcing the issue to a head, an obvious step now is to produce a counter-example to Markov's result by writing out the 4-complement circuit as a system of Boolean formulas, thus demonstrating that only two distinct negative sub-formulas need appear.

And indeed, with this comes a breakthrough and the resolution to this whole curious dilemma. The scales, so to speak, are about to fall from our *I*'s. For with an attempt to write out a set of formulas depicting the 4-complement circuit comes the discovery that *no Boolean representation of it exists*.

The barrier to deriving a Boolean representation is revealing. Looking back at the 4-complement block diagram (**Figure 2**), recall that Network 2, the nested box, is a pure Moore circuit for which we already have a system of formulas. To represent the complete 4-complement box, however, we first need to re-specify *x*, *y* and *z* — the inputs to the nested box — in terms of the new set of arguments: *a*, *b*, *c* and *d*, the main inputs. The obstacle to achieving this appears in finding that no expression for y can be derived without y occurring as one of its own arguments!

How does this come about? It is our old friend the sneaky feedback loop, reminding us that this is no longer a simple *combinational* circuit like Moore's. Through the nesting of one box in another a primitive form of memory has been introduced whereby it has become a *sequential* switching circuit whose subsequent internal state depends both upon present inputs and current state: the present value of *y* plays a part in determining *y*'s new value. In short, the 4-complement circuit is really a *finite state machine*, a device whose context-sensitive action lies beyond the descriptive scope of Boolean formulas. The facile notion that everything can always be 'talked about in a different language' is thus not without its pitfalls.

Still sneakier, (and this really is rather subtle) the 4-complement circuit is a finite state machine *mimicking* the behaviour of a non-sequential machine, the latter comprising a humble combinational circuit of just four inverters: a' = Not(a), b' = Not(b), c' = Not(c), d' = Not(d). Here we have the peculiar case of a higher or meta-Boolean form of life disguised as a lower or Boolean form. The camouflage is truly effective too, since no experiment conducted on the terminals of the 4-complement (black) box could determine whether it contained Boolean or non-Boolean-representable entrails. (Although curiously — and here is another tricky twist — the non-Boolean circuit is actually composed entirely of *Boolean components*: ANDs, ORs and NOTs, an indication both of the import of their *interconnection pattern* and of the source of weakness in the algebra that cannot describe it.)

A fine distinction is involved in all this that it is worth being clear about.

A Boolean *function* describes a relation or mapping between one two-valued variable (the value of the function) and others (its arguments). As such it may be expressed or specified in different ways; in a tabulation of corresponding values, for instance. Often we represent it as a Boolean *formula*, that is to say, as a legal expression in the formalism called Boolean algebra. In that case, the dependence of the formula's value on that of its variables will strictly mirror that of the function on its arguments. Moreover, any Boolean function *can* always be described by a Boolean formula.

But that is not to say that it *has* to be so represented or that a specification or implementation of the function must depend on some analogous structure or mechanism. The 4-complement finite state machine is an example of an alternative implementation, its *effect* representable by $a' = \text{Not}(a)$, etc., but its internal operation (as embodied in its circuit diagram) having no counterpart in Boolean algebra. The importance of this is that generalizations about Boolean functions are not to be reliably based solely on inferences about Boolean representations of those functions.

So it is that the supposed discrepancy between Markov's conclusion and Theorem I turns out to be illusory. The meticulous definitions at the beginning of his paper are not for nothing. As a careful re-examination of the account above will show, the result he proves is explicitly restricted to Boolean functions *realized in Boolean formulas*. Our concern, on the other hand, (if only lately appreciated) has been with Boolean functions realised otherwise. Minsky's implication notwithstanding, Markov's work is simply *inapplicable* to the case in hand. Like the 4-complement box, the K-complement box need employ no more than two inverters. But at least $\lceil \log_2 K \rceil + 1$ distinct negative sub-formulas will be required in any Boolean formulas describing the input-output functions of the latter. No contradiction is implied. E.N. Gilbert's paper, incidentally, which also addresses the minimum inverter requirement question, is equivalently restricted, his analysis being confined to loop-free networks.

Even so, doesn't a suspicion linger that the K-complement simulator is in some way yielding something for nothing? After all, inverting binary signals is a concrete if trivial operation, analogous to flipping over coins so as to make heads from tails or tails from heads. In the end, just how *is* it that K such reversals can be effected given only two reversing machines?

The answer is simple. It is done by using those machines more than once. Through reiterated application we can achieve serially the same result as K single-action machines working in parallel. But at a price, to be sure. Here is how John E. Savage puts it in *The Complexity of Computing*[4]: "Sequential machines compute logic functions, just as do logic circuits. However, since sequential machines use their memories to reuse their logic circuitry, they can realise functions with less circuitry than a no-memory machine but *at the expense of time*" [my italics]. As we saw earlier, hardware-implemented logic introduces lag. As K increases, so will the number of passes through feedback paths in the nested circuitry, and the longer final outputs will take in responding to changing input patterns. In practice this would be a serious factor to consider.

Lastly, note how Savage casts incidental light on the reason why a single inverter – however combined with ANDs and ORs – is inadequate for simulating further negators. Negation of externally presented bits on one channel will always require one inverter. But at least a second will be demanded in creating the *memory* needed in re-utilising that first. In fact, as we have seen, two inverters are both necessary and sufficient.

Simple but hard-won insights are compressed into the foregoing paragraphs. Having gained clearer understanding, a letter to the author whose casual remarks unwittingly triggered this improbable detective story seemed not inapposite. I was gratified thus when, in a subsequent communication, Marvin Minsky warmly concurred in the above analysis, graciously conceding a too hasty perusal of Gilbert and Markov's articles. Likewise, his "To what extent can this result be applied to itself?" turned out to be a mere chance form of words, no reference to recursion intended, but resonant to me under the circumstances.

Thus were K-nots disentangled from a Markov chain of deduction, and the sufficiency of two negators in producing Moore inverters *ad libitum* confirmed.

Conclusion

The inception of this narrative was a puzzle appearing in *Abacus*. As a matter of fact, the question there posed came in two, supposedly equivalent, versions: Moore's original problem in circuit design and an analogous problem in computer programming. In the latter form we are asked to "write an [assembly language] program that will store in locations U, V, W the 1's complement of locations x, y and z. You can use as many COPY, OR and AND instructions as you like, but you cannot use more than two COMP (1's complement) instructions." This second version is absent from Wos et al's *Automated Reasoning*[6], appearing only subsequently in his synoptic Abacus article. The trouble is, although aimed at preserving the essence of the former, the conditions imposed are actually more restrictive than Moore's: a whole class of solutions becoming inadvertently excluded.

What is it that makes the program version different? In effect, it is a silent prohibition against certain kinds of perfectly valid circuit configurations: a ruling out of the use of feedback loops implicit in the *preclusion of a JUMP instruction*. Self-modifying functions would be excluded from representation in software. That is, for every program solution there would be an equivalent circuit, but not vice versa. Just as sequential networks defy description in the notation of Boolean algebra, so loops in any circuit solution will defeat implementation in such a program.

The slip is an easy one to make, and especially so when Moore's own circuit uses no feedback. Perhaps it was familiarity with this that unconsciously acted to restrict Wos's contemplation to combinational type solutions only. Let us make no mistake however: discarding one channel from the 4-complement simulator would leave a three-channel device answering all the demands of Moore's problem. Here we have a finite state machine solution (one of an infinity) that cannot be represented in the reduced instruction code. I suspect that in the urge to translate Moore's problem into terms suited to his automatic reasoning program, Larry Wos temporarily underestimates and thus misrepresents the complexity and potential of networks using ANDs, ORs and NOTs. [In passing - and without any reference to the aforementioned author - the tendency to see circuit diagrams as engineer's easy-to-read-picture-book-explications of 'real mathematics' envisioned in putative formulas, is not uncommon among mathematicians. Engineers, I may add, humble as their mental endowment may be, will be more impressed when condescension can be matched with insight into the advantages of a two-dimensional language.] Whether or not the automated reasoning technique could be successfully applied to the 4-complement problem is a further interesting question.

Following the lead suggested here, the 4-complement circuit is elegantly modelled in a simple computer program using iteration to imitate the feedback loop (see listing). A series of assignment statements based on the earlier derived formulas describing Moore's circuit make up the body of the program. **Figure 5** shows a version written in Turbo Pascal. Read in conjunction with Moore's circuit and **Figure 2**, the program is self-explanatory: more eloquent in fact than any verbal commentary on circuit operation. Interested readers may like to try the effect of including a write statement in the Repeat loop so as to expose the behaviour of *y* under different input sequences.

A final observation on Markov's result must bring this account to a close. **Figure 3** depicted the endlessly expandable system of recursively nested Moore circuits for producing an arbitrary number of NOTs. Winning three NOTs from two, every level of nesting yields a spare inverting channel. In practice, however, the mass-production of NOT-functions can be enormously accelerated. How? Notice that Markov's I is still only 3 for n as high as 7. But this is another way of saying that a simple combinational circuit exists that can simulate seven inverters directly from three. Similarly, from these seven a further 127 can be produced at only the third level of nesting (2 -> 3 -> 7 -> 127 -> ...). Readers may like to test their grasp of the foregoing by writing a program that implements seven inversions while using only two Not operators.

In conclusion, and before any false hopes are raised though, I ought to say that the above suggestion is intended merely as an exercise. Patents, it must be explained, have already been granted and the Sal-Mar International Inverter Hire Company Inc. is due for launching at an early date. Prompt negations of the highest quality will be available to customers via standard phone lines. Charges are expected to be modest.

In the meantime, call me an *adulterated* Platonist if you will, up in heaven two eternal NOTs await the arrival of virtuous logicians (and the occasional virtuous engineer). I look forward to rubbing that in with Gödel and Russell hereafter.

• Grateful thanks are due to Jim Propp, formerly of the Department of Mathematics, University of Maryland, whose searching criticisms brought to light various errors and made for substantial improvements to an earlier draft of this paper.

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```
Program Four_Complement_Simulator; {Turbo Pascal Version 3}
{Compare Fig.2 and Moore circuit diagram for all that follows}

 Var
   a,b,c,d,x,y,z, {main and nested inputs}
   A1,B1,A2,B2,  {inverter outputs Networks 1/2}
   aa,bb,cc,dd,  {main outputs a',b',c',d' in Fig.2}
   initial_y     {previous y state} : Boolean;

 Procedure Specify_inputs; Var ai,bi,ci,di : char;
  Begin
    Writeln('Input 4 truth-values for a,b,c,d: T(rue)/F(alse)');
    Read(Kbd,ai,bi,ci,di);
    If ai='T' Then a:=True Else a:=False;
    If bi='T' Then b:=True Else b:=False;
    If ci='T' Then c:=True Else c:=False;
    If di='T' Then d:=True Else d:=False;
    Writeln('Inputs: ',a:8,b:8,c:8,d:8);
  End;

 Begin {Main}
   Specify_inputs;
      {Nested box inputs x and z first respecified in terms of a,b,c,d:}
   x:= ((a And b) Or (a And c) Or (b And c));
      {Expression for 1st inverter input in Moore circuit}
   z:= d;
      {z is connected to input d}
      {Input y feedback involvement calls for iteration:}
    Repeat
     initial_y:=y;
     A2:= Not((x And z) Or (x And y) Or (y And z));
        {Nested box first inverter output defined}
     B2:= Not((x And A2) Or (y And A2) Or (z And A2) Or (x And y And z));
        {Nested box second inverter output defined}
     A1:= ((y And A2) Or (z And A2) Or (y And z And B2) Or (A2 And B2));
        {A1 = x' output of nested box, see Fig.2}
     y:=  ((a And A1) Or (b And A1) Or (c And A1) Or (a And b And c));
        {Expression for 2nd inverter input in Moore circuit. y may have
         changed value, or not, depending on previous input pattern}
    Until  y = initial_y;
        {Remain in loop until y stabilizes; two loop passes always
         suffice: y's value self-confirming after one change. A
         simple 2-cycle Do-loop would serve equally well here}
  B1:= (x And A2) Or (z And A2) Or (x And z And B2) Or (A2 And B2);
        {B1 = y' output of nested box, see Fig. 2}

        {Standard Moore circuit formulas follow}

  aa:= ((b And A1) Or (c And A1) Or (b And c And B1) Or (A1 And B1));
  bb:= ((a And A1) Or (c And A1) Or (a And c And B1) Or (A1 And B1));
  cc:= ((a And A1) Or (b And A1) Or (a And b And B1) Or (A1 And B1));
  dd:= ((x And A2) Or (y And A2) Or (x And y And B2) Or (A2 And B2));

  Writeln('Outputs: ',aa:8,bb:8,cc:8,dd:8);
 End.
```

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Jitter generator

Within my company, BCD Audio, we had a requirement for a unit that could inject a small amount of jitter onto a suitable square wave. The resulting circuit also had some other desirable features; the output level was exactly 5V p-p from exactly 75R impedance, and the oscillator module used was accurate to 1PPM.

The circuit works as follows: a noise generator is produced from the zener-like breakdown of transistor Q1. RV2 sets the current into the transistor and is adjusted for maximum noise generation. R2 and 12V Zener D2 roughly regulate the supply to the noise generator, making the unit independent of supply variations.

The 5V regulator used was trimmed via RV1 for a supply slightly higher than 5V, so that the outputs were exactly 5V P-P.

The noise generator diode is amplified by transistor Q2, filtered and taken to RV3 which is used as the front panel jitter level adjustment. The resulting noise signal is amplified by Q3, filtered by C10 and superimposed on the square wave signal at U3. The range of jitter produced is around 0 to 100nS. The noise signal is injected onto both edges of the signal.

A Dallas DS32K oscillator module was used as the square-wave generator; the circuit would work with other modules provided their jitter performance was adequate. The signal is fed down two Schmitt triggered inverter chains, that include a small amount of high pass filtering to slow the rise and fall times, and then recover the speed. The final inverter stages are paralleled for low output impedance. Two chains are used so that one output is subject to a controlled amount of jitter, and the other output is not, but has the same propagation delay.

The clean output may be used to trigger an oscilloscope, the jittered output can then be applied to the equipment under test, and the resulting signal measured by the oscilloscope. Keep in mind that this circuit produces jitter on both clock edges, but some circuits are more sensitive to jitter on one edge than the other.

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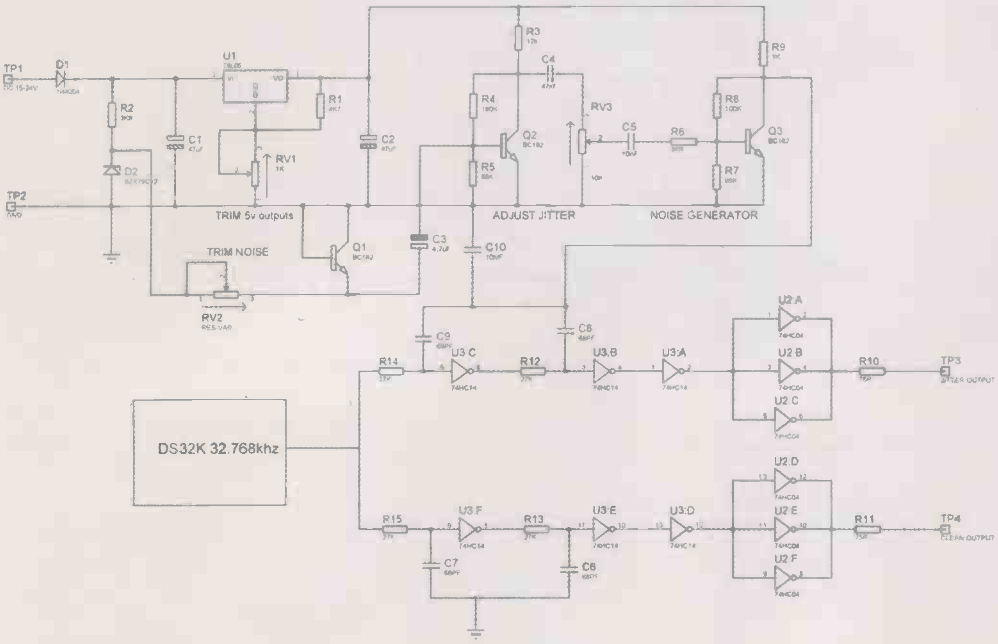


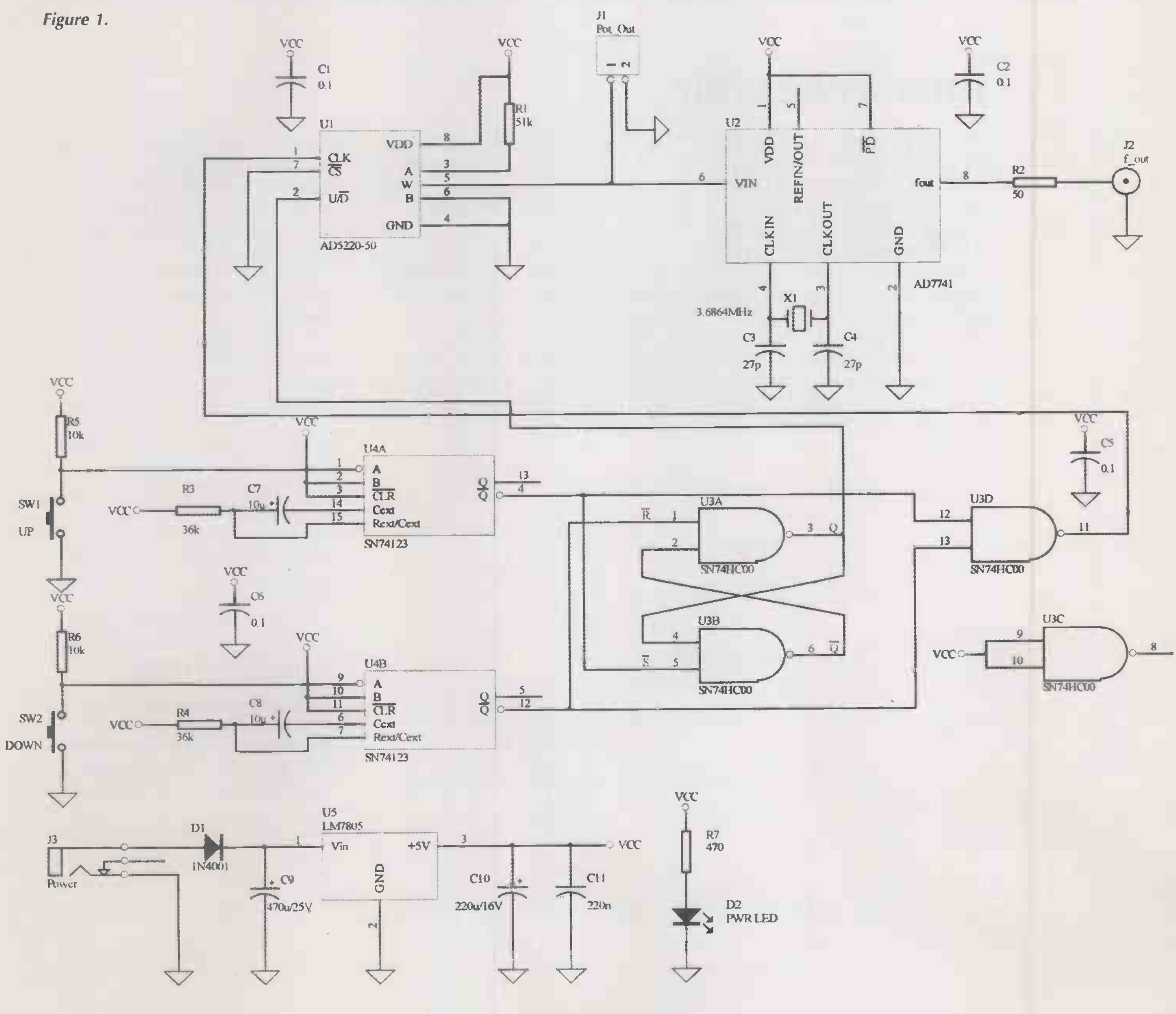
Up-Down-pushbutton control for digital potentiometers

The schematic presented, **Figure 1**, is intended to provide a simple, no-microprocessor control for the Analog Devices AD5220 Increment/Decrement Digital Potentiometer U_1, which is used to control a voltage-to-frequency converter (AD7741) U2.

The AD5220 is a simple 8-pin device with nominal resistance of 10, 50 and 100kΩ, in the design proposed the 50kΩ version was used. The digital potentiometer is designed to interface to a microprocessor or to simple logic circuitry, which will drive the U/D (increment/decrement) and the CLK (Clock) lines of the IC.

As the manufacturer does not suggest a circuit for simple pushbutton interface and the idea of including a whole microprocessor system only for the task of controlling this device sounds ridiculous, I designed this simple pushbutton-circuit, which provides both Up/Down Control with Clock Pulses and pushbutton debouncing. The pushbuttons are SW_1 and SW_2 with pull-up resistors R_5 and R_6. The U4 74123 device is used as one-shot multivibrator with a time-constant of around 120ms to provide the pushbutton debouncing. The multivibrators are retriggerable, so only the first negative-going pulse on the A-gate will trigger the multivibrator to produce the over 100ms output pulse. Any other pulses resulting from pushbutton bouncing will only make the duration of the output pulse longer, but will not contribute to additional clock edges to the CLK-input of the potentiometer. The timeconstant can be adjusted to suit your actual needs by changing the R_3-C_7 and R_4-C_8 components. To provide for the Clock line of the AD5220, the two resulting

Figure 1.



debounced negative going pulses from the two pushbuttons at the Q\-outputs of the U_4-multivibrators are AND-ed by the U_{3D} gate. It is assumed that the user will press only one of the two pushbuttons at a time, pressing together the two buttons is illegal with this circuit. The U_{3D} produces the positive-going debounced pulse at the CLK-input of the digital potentiometer. As the AD5220 is negative-edge triggered, the falling edge of this pulse will actually adjust the potentiometer.

The pulse duration (of more than 100ms) will be more than adequate to provide for the R\-S\-Flip-Flop, formed around the U_{3A} and U_{3B} gates, to settle to the appropriate Up-, respective Down-Direction. The Q\-outputs of U_4 will SET or RESET\ the flip-flop depending on the pushbutton pressed. The Q-output of the flip-flop controls the U/D\-line of the AD5220 and is settled to the correct level, before the low-going edge is applied to the CLK-input. The circuit has its own power supply around U_5 and the J_3, D_1, C_9, C_{10} and C_{11} parts.

The, simple pushbutton-interface presented here gives the user the opportunity to build a programmable voltage divider around the digital potentiometer with the range (0 divided by 2.48)V, 128 steps and output at the J_1 -connector and a programmable frequency synthesiser (Quartz stabilized through X_1) with the range (0 18 divided by 1.66)MHz in 11.52kHz steps and output at connector J_2. At Power-On the digital potentiometer is reset to middle position. All timing diagrams associated with the described circuit behavior are presented below in **Figure 2**.

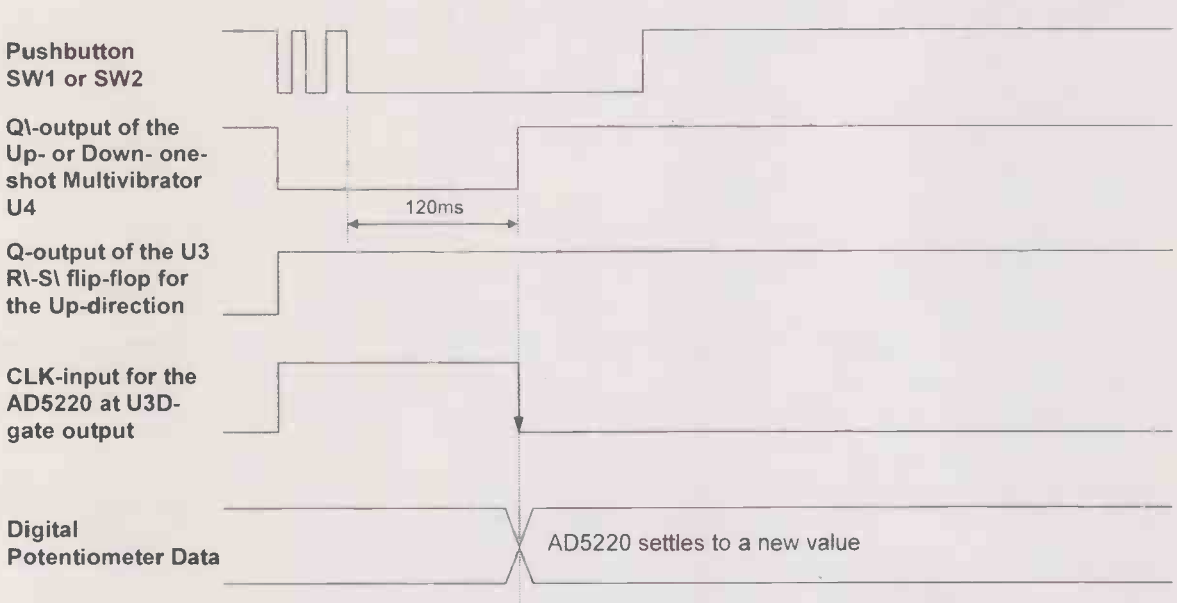
Emil Vladkov
Sofia
Bulgaria

References

1 AD5220 Increment/Decrement Digital Potentiometer, Analog Devices Inc., Rev.0.

2 AD7741/AD7742 Single and Multichannel, Synchronous Voltage-to-Frequency Converters, Analog Devices Inc., Rev.0.

Figure 2.



Ultrasonic oscillator

Ultrasonic transducers for use in intruder detectors and similar applications of the well-known Doppler principle typically have a resonant frequency of 40kHz, ±1kHz tolerance. For best output from the transmitter, it is important to drive it at or near resonance. Though transmitters and receivers normally come in factory-matched pairs, maximum area coverage and range can be achieved only if the two transducers are accurately tuned to each other.

A fairly simple method of achieving this is to drive the transmitter from a variable frequency source, and examine the amplified output of the receiver for maximum signal. However, the potential resonance of the transmitting transducer is then wasted, and drift in the frequency of the source can easily lead to appreciable fall-off in the received signal. Therefore a self-oscillating but nevertheless tuneable driver-circuit is called for. With care, even if the frequency of the transmitter does change with temperature, it will be matched by a corresponding change in the receiver (normally mounted alongside).

A wide-band op-amp with good slew-rate is needed; the LF356 is adequate, and cheap. Also, it has low consumption and a JFET front end. In **Figure 1**, the non-inverting input of A_1 is biased to half V_s by means of the divider R_1 R_2, and feedback from R_3 to the inverting input sets the quiescent level of V_o at half V_s too. The ultrasonic transducer C_x has high Q, and at resonance its current is in phase with the voltage applied across it. By stringing it between V_o and 0V via the resistors R_4 and R_5, a suitable signal can be picked off at R_5 and fed to the non-inverting input, hence providing positive feedback at the resonant frequency of C_x. Furthermore, the frequency at which the circuit actually oscillates can be tuned upwards by reducing R_5, or downwards by reducing R_4. Raising C_1 has a frequency-lowering effect too, but it is preferable to keep this capacitor as a fixed-value low-temp coefficient ceramic (NPO). The value of the coupling capacitor C_2 has a secondary influence (bigger C_2 lowers f_{osc}). Thus the ultrasonic output can easily be trimmed until a maximum is observed at the receiver, adding parallel resistance at R_4 or R_5 as necessary.

The overall frequency stability is fairly good, for example with the circuit tuned to f = 39.665kHz the drift was less than 10Hz over three hours, after five minutes to warm up. The power consumption is modest, about 2mA at 12V. The circuit will oscillate consistently down to approx 6.5V, and is safe up to at least 30V (the limit of the op-amp being 36V total). The shift in frequency with V_s is roughly 20Hz per volt.

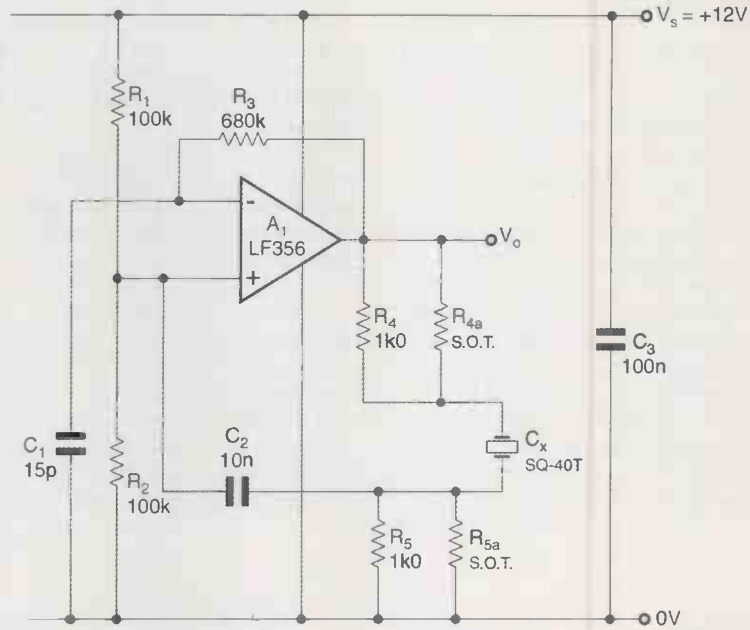


Figure 1.

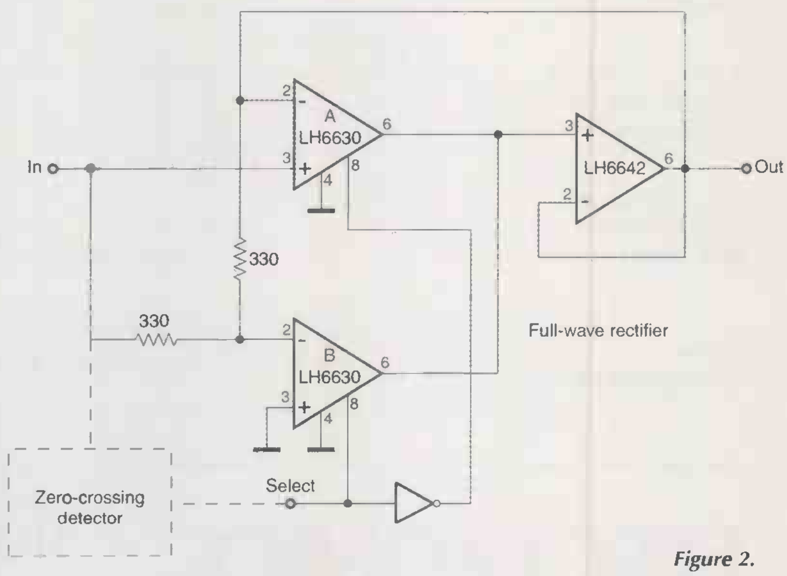


Figure 2.

C J D Catto
Cambridge
UK

Low battery warning device

The circuit in **Figure 1** was designed to give an audible blip and a visual flash warning when the battery voltage dropped below a certain threshold. The frequency increases as the battery voltage continues to fall. The approximate frequency relative to voltage is given in **Figure 2**.

The circuit uses a Programmable Unijunction Transistor (PUT) as a relaxation oscillator. The voltage at point B varies with battery voltage and if it drops to 4.4V (i.e. 5.0 - 0.6) the PUT conducts and discharges the capacitor through the LED and bleeper. As the battery voltage continues to decrease the voltage at trigger point B tracks the decreasing battery voltage, consequently lowering the trigger voltage. With the decreasing trigger voltage the PUT switches on earlier in the capacitor charge curve thus increasing the frequency of the warning devices.

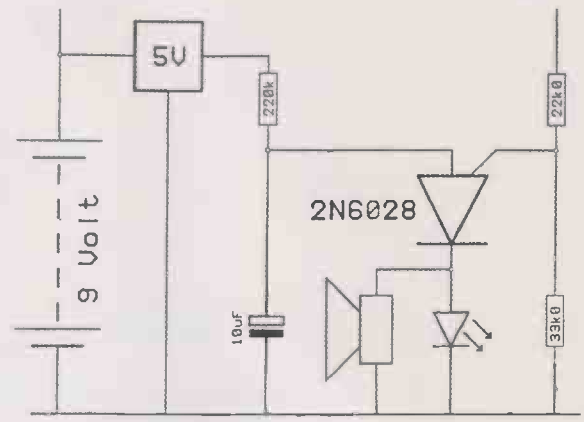
This particular circuit was used in a 9 Volt battery powered instrument with a 5 Volt stabilised power supply requirement, but the circuit could be easily modified to suit different requirements.

Des Kepple
Co. Carlow
Ireland

Figure 2.

Battery (Volts)	Frequency (Hz)
8.0	0.0
7.5	0.15
7.0	0.25
6.5	0.33
6.0	0.45
5.5	0.66

Figure 1.

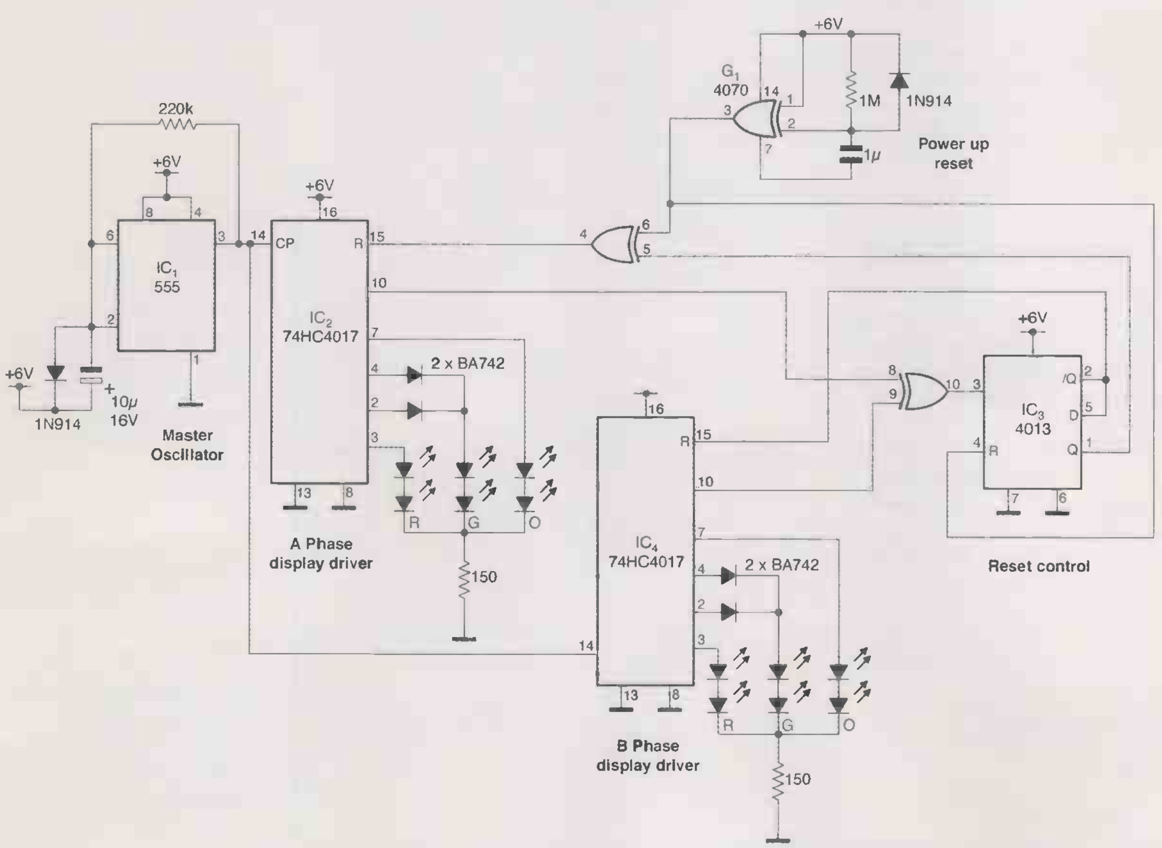


Traffic light simulator

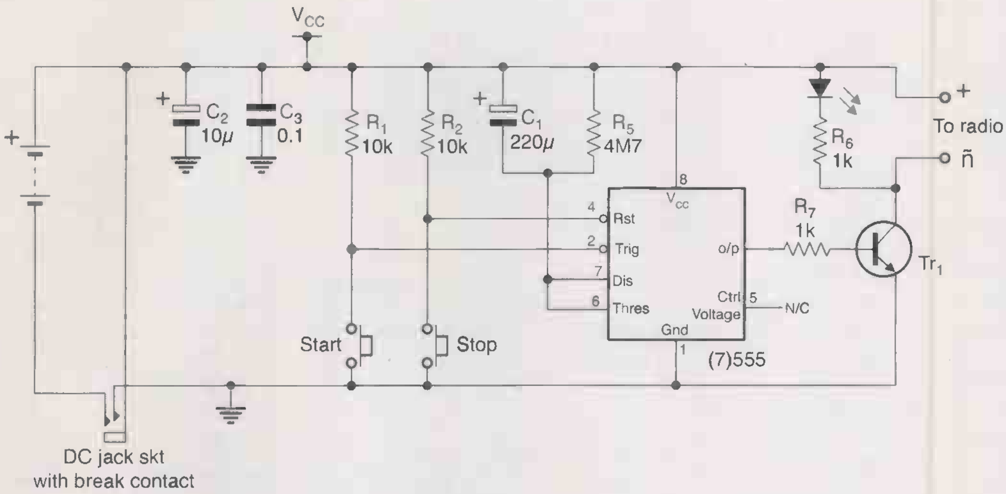
At power up, pin 3 of G1 immediately goes high, this forces IC3 to reset, forcing its Q output to 0. This low together with the power up reset signal forces IC2 to reset. The high on the Q output of IC3 also resets IC4. Hence the red LEDs are all lit indicating the all red condition. As the power up reset times out, pin 4 of G1 goes low, removing the reset on IC2, hence IC2 steps through its cycle red to green to orange. At the end of the orange period a pulse is generated at pin 10 of IC2. This toggles IC3 reversing the resets to IC2 and IC4. The all red period now reappears and after 3 seconds IC4 now cycles red to green to orange. At the end of the orange period for B phase, IC4 also generates a pulse at pin 10, again toggling IC3, again reversing the resets. This again brings up the all red period and so the cycle continues.

Two LEDs are used for each colour, so there is one for each side of the approach. IC1 is set up so it always powers up, low, at its output, before oscillation. All unused inputs should be tied to a supply rail.

Gregory Freeman
Mt. Barker
Australia



Long delay timer using only one 555 chip



The example sleep timer uses a transistor as a switch but other applications could use it to drive a relay or isolated triac for heavier loads.

My first attempt to build a simple one chip (7555) battery saving 30 minute sleep timer for a personal radio failed due the electrolytic capacitor's leakage current preventing the monostable from timing out. I then used the standard long timer circuit of a 555 astable and digital counter IC, which worked as desired but I felt there must be someway of making a single 555 do the job.

The solution seemed rather simple, the circuit is shown in diagram 1:

The main circuit uses a CMOS 7555CN (for the low quiescent current (60mA) to turn the radio on for up to 25 minutes using TR1 as a switch. TR1 has a low 1k base resistor to ensure it is saturated. The reset button turns the radio off, and the Start button turns it on (thus starting the timeout period), or restarts the timeout period. I also added a DC jack with make break contact so that I could plug in a solar panel/mains battery eliminator to further save batteries.

The timing components C1 and R5 have been re-arranged so that the discharge pin actually charges C1 and so the timing period is set by the C1 - R5 discharge time, which means that any leakage current will simply slightly shorten the delay by discharging C1 faster. By referencing C1 to Vcc rather than ground, the 555 threshold pin sees the voltage (Vcc – Voltage Across C1), which makes it appear as if C1 was charging as expected. Thus the delay remains 1.1C1R5 seconds.

I wasn't sure if any diode clamps on were needed at the threshold input, so just decided to rely on those present in the IC as part of its static protection circuitry. The power indicator LED1 only uses 1mA.

I housed the timer PCB and 2AA cell batteries in a case of similar size to the radio, joined the two with stick on Velcro pads and connected power to the radio using wires ending in dummy AA cells (for example, Maplin YX92A)

My 555 CR timing circuit section seemed so simple that I searched on the internet to check whether anyone had already thought of it but found nothing.

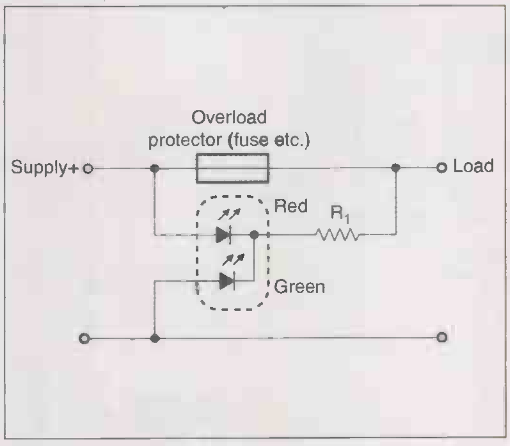
Alan Bradley.
Belfast
UK

Blown fuse indicator

This circuit is a simplified version of Alastair Borthwick's idea in the February 2003 edition for indicating the status of a fuse or other type of overload protection.

Normally the fuse shorts out the red LED and supplies current via R1 to illuminate the given LED. R1 is chosen according to the supply voltage. When the fuse ruptures, current is interrupted to the given LED and the supply voltage is dropped across the fuse illuminating the red LED. As with Mr Borthwick's design, shunt diodes across the LEDs allow operation on A.C. supplies and may offer reverse voltage protection for the LEDs, a situation which could occur if the supply fails.

Rod Brown
Nottingham
UK



Warning

Last month we published a couple of Circuit Ideas that could be dangerous if precautions are not taken.

Firstly, the Intelligent Electric Fence should not be built as it stands. Connecting a metal fence almost to the mains is not a clever thing to do – so this circuit should be only used via a low current source – for example a protected isolating transformer. On no account should a fence be connected directly to mains.

Secondly, the 3-phase selector has no protection should any relay coil go short. Low current protection should be used.

I must point out that circuits in this section are just ideas. They do not normally constitute a full, tested project, and so great care must be taken with any of them that get connected to a mains power supply.

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NEW PRODUCTS

Please quote *Electronics World* when seeking further information

Ultracapacitors deliver instant power bursts

NessCap Co. Ltd.has introduced the addition of 3F to 100F models to their 2.7 volt ultracapacitor product line.Available in seven different capacitance ratings designed to meet a variety of primary or backup energy needs for compact electronics., they enable designers of power systems to increase product life, reduce or eliminate battery use and improve peak power availability.

When used in conjunction with batteries, the ultracapacitors deliver peak power to reduce the required battery size while minimizing battery discharge cycles to effectively extend battery life. With the new compact sizes and ability to withstand 500,000 discharges with no maintenance, NessCap ultracapacitors allow designers to use smaller batteries that will last longer, while keeping overall product size and cost to a minimum. In many cases the ultracapacitor will never need to be replaced.

Available now with ratings of 3F, 5F, 10F, 25F, 50F, 90F and 100F, pricing for the new models is based on the quantity ordered starting at US $ 0.8 for sample quantities of the 3F device. All of the new models feature a convenient cylindrical cell form-factor and boast an operating temperature range of -40°C to +60°C and a projected operating life of 10 years.

NessCap Co Ltd
www.nesscap.com

Rewritable visual card system offers versatility across applications

Star Micronics have launched a new low cost, 'communicating' rewritable card unit offering versatility to work with other component peripherals including proximity RF/ID, magnetic stripe, IC chip or barcode reader/writers.

Called the MRS100, the new visual card system uses ISO standard cards, but with a special Ricoh or Mitsubishi coating to enable text or graphics to be re-written to the card up to 500 times. Its re-usability makes it ideal across a diversity of applications, including visitor/employee access, security ID, travel tickets, transportation tracking, loyalty schemes and club memberships, as well as electronic wallets.

Capable of writing text or detailed graphics (e.g. portrait photograph) to the blue or black cards in seven and 45 seconds respectively, the MRS100 is palm-sized in design and affords both front and rear card entry and ejection, depending on the process requirements.

StarMicronics
www.StarMicronicsEurope.com

Signal source equipment sets the industry standard

Tektronix have recently introduced DTG5000 Series of signal source equipment. Designed in response to ever higher clock rates and tighter timing margins, it combines the power of a data generator with the capabilities of a pulse generator in a versatile, bench-top form factor. Used in a variety of applications, the DTG5000 Series consists of two mainframes – the DTG5078 and DTG5274 – and three plug-in output modules that combine to cover a range of applications from legacy devices to the latest technologies. In addition, eight low-current, independently controlled DC outputs can substitute for external power supplies. Each mainframe incorporates a full complement of auxiliary input and output channels to easily integrate with other instruments, such as oscilloscopes and logic analysers, to create a flexible and powerful laboratory set-up.

Tektronix
www.tektronix.com

Simultaneous connection of up to 480 contacts

The new G2 mass interconnection system from Virginia Panel Corporation, available exclusively in the UK from The Peak Group, is a compact, high-density unit that can simultaneously engage up to 480 signal contacts in seconds.

Designed to speed the interfacing of UUTs (units under test) in ATE applications, the G2 provides a rapid alternative to the repeated connection and disconnection of individual leads and contacts in a rugged, reliable system.

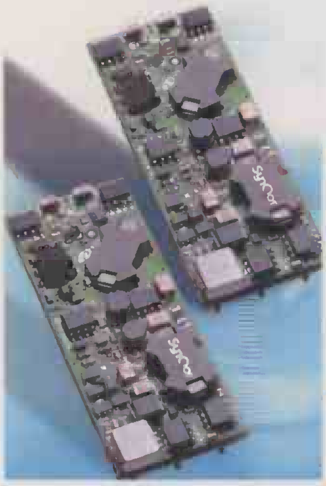
The two-piece, EMI-shielded ITA enclosure features a large adjustable cable clamp to accommodate various sized wire bundles, and slides open for easy access to modules and contacts.

A small footprint and rugged construction make the G2 a versatile connector solution for use in military, aerospace, medical, automotive, telecommunications, industrial, and factory automation applications.

The Peak Group
www.thepeakgroup.com

Please quote *Electronics World* when seeking further information

Eighth-brick line of DC/DC converters offers higher power levels and more output voltages



SynQor, has recently expanded its popular line of Eighth-brick dc/dc converters. The PowerQor™ Eighth-brick family will now include modules up to 75W and include output voltages as low as 1.0V.

The new eighth-brick Giga series now includes additional modules of 1.0V at 25A, 2.5V at 25A (63W), 3.3V at 20A (66W), and 5.0V at 15A (75W), and it has recently added a 12V module to their 50W Mega series. All units operate from an input voltage of 35V to 75V and employ the established industry standard eighth-brick footprint and pin out. The eighth-brick converters occupy only 60% of the board space of a standard quarter-brick, yet their ultra high efficiency results in minimal power derating. This allows designers to replace existing quarter-bricks in many applications.

SynQor's eighth-brick family is currently offered with through-hole mounting and will also be available in a surface mount configuration.

All converters use a single board, open frame design and are manufactured in their fully automated production facility in Boxborough, MA.

The expanded Eighth-brick series complements SynQor's existing broad line of Quarter-bricks and Half-bricks from 15-100 amps to provide the widest and most scalable product offering for high-efficiency, no-heatsink dc/dc converters.

The eighth-brick converters include a full complement of control and protection features such as on/off control, voltage trim, remote sense, short circuit, output OVP, thermal shutdown and 2000Vdc isolation rating. These features allow advanced functionality, while standard safety certifications allow easy integration into the end user's product.

SynQor
www.synqor.com

Micro sized connectors carry VDE approvals

Micro Mate-N-Lock connectors, based on 3mm centrelines, available in wire-to-wire, wire-to-board, single row and double row configurations have been awarded the VDE certification mark, allowing the product to be used throughout Europe and certifies compliance with European standards.

They are suitable for a variety of industrial and commercial applications including medical devices, household appliances, commercial appliances, industrial controls and other applications that require small centreline power and signal I/O connections

Tyco Electronics
www.tycoelectronics.com

Insulated metal substrate technologies reduce cost of thermal management in high power density applications

Bergquist's latest Thermal Clad (T-Clad) Insulated Metal Substrate (IMS) technologies will reduce the cost and the complexity of thermal management in high power density surface mount applications. The new materials are ideal substrates for power conversion designs, motor drives, solid sate relays, power LED displays, and other applications where size constraints, die size reductions and high component densities make semiconductor heat dissipation a major design challenge.

They minimise thermal impedance and conduct heat more efficiently than standard printed circuit board materials. As a result, cooling can help to extend die life through lower operating temperatures, reduce PCB size, increase power densities, and simplify assembly through the elimination of heat sinks, device clips, cooling fans and other hardware. In addition, T-Clad substrates minimise interconnects and are more robust than the fragile thick-film ceramics and direct bond copper (DBC) constructions often used in modem applications.

Based on a three-layered system, T-Clad boards typically comprise the printed circuit foil layer, the dielectric layer, and the base layer. Circuit layers range in thickness from 35 to 350μm. Base layers are typically 1.0mm thick aluminium, although other thicknesses and other metals including copper may be used. Circuit layer and base layer are bonded together by the multiple layer dielectric, which combines electrical isolation with minimum thermal resistance. T-Clad can be used to replace FR-4 in conventional multi-layer assemblies to reduce the thickness of the copper circuit layer.

The latest T-Clad dielectrics are based on a proprietary polymer/ceramic blend and are available in options of multi-purpose (MP), low thermal impedance (L TI), and high temperature (HT), depending on specific application requirements. Dielectric thicknesses range from 75μm to 300μm depending on specific isolation needs. Operating temperatures are up to 140°C, while dielectric breakdown voltages range from 6.0kV AC to 12.5V AC. Thermal impedances are from 0.90°C/W to just 0.45°C/W.

Bergquist
www.bergquistcompany.com

Cell phones surge ahead

Ian Poole reports on the 3GSM World Cellular Telecommunications Congress in Cannes, France

3GSM, the world's largest cellular telecommunications congress was held in Cannes France between 23 and 26 February 2004. It took place in the famous Palais des Festivals, the same place where the Cannes Film Festival is held, and this year was bigger and more exciting than before. With over 35,000 visitors registered this showed an increase of 30% over the previous year, and following a similar trend the number of exhibitors increased to a total of 624, and as a result a larger exhibition space was needed.

In addition to the exhibition there was a lecture programme with an impressive line-up of nearly 200 speakers ranging from technical experts to the industry leaders including people like Arun Sarin CEO Vodafone Group, and Rene Obermann, Chairman of T Mobile International.

After the recent years of financial recession, the feel of the show was upbeat, with the exhibitors indicating that it had been better than last year. Many new products were being launched. One new idea is that of Push to Talk over Cellular phones (PoC). This enables phones to connect to other users in a group and be used a little like walkie-talkies. Operators are already looking at the idea very seriously, with Orange, for example launching the idea in France to business users in April and the mass market about six months later. Manufacturers including Nokia and many others are also investing heavily in this technology.

Another area of interest is the location services market. By linking phones to the GPS system, it is possible to provide many location services, including using the phone to give location instructions.

As far as 3G was concerned there were plenty of demonstrations of 3G video services, showing what can be achieved now. One of the keys to the success of this will be the processing within the phone and a solution supplier named Emblaze Semiconductor, who make the chips and also the accompanying software, were demonstrating a very impressive high quality video solution.

Chip manufacturers and solution providers were also in evidence. Qualcomm, a little known name in Europe outside the cellular telecommunications industry were there. This company, effectively the founder of CDMA technology is one of the largest solution providers in the industry. They have focussed their efforts on providing complete chip sets with the associated software. This removes the integration effort required by phone manufacturers who only need to focus their efforts on customising the solution to their needs and packaging it in the right way. By adopting this approach they now supply 3G chipsets to 17 customers worldwide. Interestingly for the CDMA 2000 family of standards used widely in the US and Asia Pacific regions, they supply their solutions to over 65 customers – no mean achievement. Currently one of their development boards for W-CDMA solutions fits onto a board a little over an inch square.

As one would expect there are many other famous names manufacturing chips. Analog Devices, TI and many others were all showing their new offerings, each fielding an impressive set of parameters.

However with over 600 exhibitors there with large companies from Agilent to Sony Ericsson, and smaller ones from Antenova to Followap, the range of products and innovations was enormous, including everything from test equipment to antennas, and software to hardware, in fact anything associated with cellular telecommunications was there.

And as if was not enough, next year is already being planned for 14th to 17th February, and if this year's event is anything to go by, it should be even larger and more exciting.

Not me, guv

Ivor Catt discusses the interference when an electronic module is switched on, every second half cycle

The DC power supply market tends to be very competitive, so that there is minimal surplus and minimal margin of safety in the performance of any component. It will follow that nearly all the area in the BH curve in the input transformer will be used. Also, competition and pride will drive the material choice towards magnetic material as shown in **Figure 1**, with the smallest, narrowest area to minimise the heating from hysteresis. The area inside the closed curve represents the amount of power lost. This power has to be expensively removed as heat. Avoidance of this heating leads to high Remanent Magnetism, indicated by the point where the graph cuts the vertical axis. Minimal area within the closed curve indicates maximum remanent magnetism.

Let us assume that when switched off, the transformer core will retain its remanent magnetism, see **Figure 1**. On the next switch on, the first half cycle of the 50Hz may be positive or negative. If negative, it will take the transformer's magnetic core through its normal cycle. However, should it be positive, it will take it upwards by the vertical distance, resulting in a massive value for H, which means a massive electric current. In other words, this puts the core hard into saturation. When saturated, the transformer core behaves like air, so that the secondary loses linkage with the primary, which degrades into an air-cored choke. Such an inductor places only a small restraint on the rapidly rising input current.

In 1970, Guido Watson did the difficult experiment for me. This involved keeping the oscilloscope calm. He found mains current of some 100A in every second half cycle.

The best estimate we can make of the source impedance of the 50Hz mains is half an ohm. Thus, 100 amps will cause the mains to drop through 50 volts for the half second or so that it takes the input transformer to gradually recover towards normal working within the

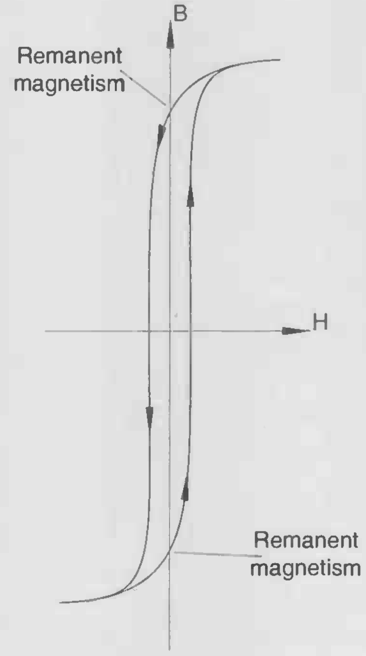


Figure 1.

BH curve, and stop saturating.

The designer of an identical piece of equipment plugged in nearby has demanded in his specification that the mains should not drop by more than 6%, or 14V. The customer, or user, has agreed to this. Thus, when our equipment is switched on, the loss of logic bits in the other equipment will be the fault of the 50Hz power supplier, not of the equipment. The customer will have read the small print of the equipment, and agree that the mains voltage must not drop by more than 6%. The only blameless party will be the manufacturer who supplied the saturating transformer. Nobody has ever suggested that power switch on should or should not depress the 50Hz supply. The EMC community have slept through these problems.

Every half cycle

When a classical DC power supply is switched on, the first raw decoupling capacitor is uncharged. Let us follow the path of the initial charging current, **Figure 2**. The input voltage builds up according to the transformer's turns ratio, perhaps to 7V RMS or 10V peak. This confronts a negligible resistance in the transformer primary and then a source impedance in the secondary of perhaps 250mΩ. The impedance of the full bridge rectifier can be more or less ignored, each diode presenting less than one volt drop but no resistive drop. Thus, perhaps 8V proceeds to the uncharged capacitor, which presents no significant impedance. This means that the resulting electric current into the capacitor is defined by the resistance of the transformer secondary.

Again, the measured current pulses are 100A, in this case every half cycle, lasting for a fraction of a second.

Since another piece of digital equipment will crash when the mains voltage sags by 50V for half a second, its manufacturer will increase the capacity of his first raw capacitor. However, should he also manufacture the rogue equipment, it will drag down the mains voltage for twice as long. The manufacturer will chase his own tail.

The simplest way out for the EMC community is to cover the whole subject with a smokescreen of mathematics, tell us not to use our mobile phone or computer while flying in an aeroplane, and so forth.

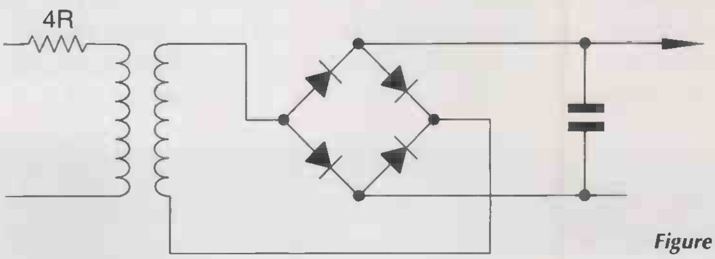


Figure 2.

That is the way the EMC community deals with its failure is to solemnly tell us not to use more than one piece of equipment at the same time. A piece of equipment which is not in use is likely to be compatible with an active piece of equipment, without the aid of half a century of EMC pontification.

Put a four ohm resistor in series with the transformer primary. That will ameliorate the problem, which is that during the critical quarter of a second after switch-on, nothing limits the primary current. The long-term solution is to include the transient behaviour of a piece of equipment along with its steady state behaviour. The people who should have been doing this, of course, are the EMC punkah-wallahs. The problem is a physical one, and mathematical high trapeze acts will not help.

Broadening out

Transformer, bridge rectifier followed by raw capacitor is not the only way in which AC is converted into DC. The circuit may use a swinging choke, which probably gets even more upset during power switch-on. My warning is that, the EMC community and the rest of us having apparently ignored the problem of switch-on for more than a half century of digital electronics, questions have to raised about the hazard to other equipment presented by switching on all other types of power supply. Looking behind this, we have to ask whether, and why, the glamorous, well funded EMC community have ignored the subject. (Probably this is because you have to know what you are doing, rather than just brew up fancy maths.) If so, I would argue that enforcement of their regulations by the EEC using criminal sanctions must end. We must not allow incompetents to control our profession and industry. In particular, they must not be allowed to take control of the necessary similar analyses needed for other DC power supply circuits. Note that my analysis above contains no mathematics. If EMC wallahs are allowed to bury such problems in fancy maths, with the support of criminal sanctions, they will create a terrible mess.

It has only just occurred to me that the reason why the necessary investigations are so difficult is that, as my colleague Guido Watson found, an oscilloscope is traumatised when something else is switched on, so that more skill and care is needed when looking at these effects than EMC hotshots could muster. Buried in the necessary experiments is the very problem being investigated!

Background

Three engineers including myself were concerned that professional engineers did not have the information and understanding that they needed to design and build digital electronic systems. Education remained in the hands of radio men who had migrated from the lab to take college jobs.

We began giving private seminars in 1977. I have found the letter acknowledging our deposit paid to Theobalds Park College towards £900 to rent the Stately Home for two days to give residential courses, 26-28 October 1977 and 14-16 December 1977. We used the umbrella of Middlesex Polytechnic, who were developing my WSI invention (see Wireless World July 1981), to give us further credibility, but took all the risk ourselves. We made the mistake of charging too little - £45, or £60 residential – but then hurriedly increased the price to reach £240, so that in future engineers would be able to attend with honour. These courses continued for ten years, and I have the 1987 brochure. Companies who sent their engineers to more than one of our courses included STL Harlow; ITT Cockfosters; Shell, Chester; Square D, Swindon; BTel Holborn; ICI Plastics, Welwyn; Redifon, Crawley; GEC, Coventry; Royal Free Hospital, Hampstead. We discussed many of the subjects ignored (and still ignored) by the EMC Community and by academia.

I find that every item on our list (www.ivorcatt.com/43.htm) is still ignored, although most of them remain important today, a quarter of a century later. All the course notes were later published privately, and most of them were republished by Macmillan in our 1979 book *Digital Hardware Design*. Macmillan quickly took the book out of print.

In sixteen hours of lecturing, we had to omit some critical problems. The one discussed in this article has never before seen the light of day.

LETTERS to the editor

Letters to "Electronics World" Highbury Business Communications, Nexus House, Azalea Drive, Swanley, Kent, BR8 8HU
e-mail EWletters@highburybiz.com using subject heading 'Letters'.

Clangers

I must apologise to readers for errors in my article A pseudo-sine wave inverter, in the April issue, page 11. In Figures 3 and 4, "2ms" should have read "2μs". I can offer no excuses, only apologies, since I proof read the article myself. My only consolation is that readers of this magazine will doubtless all have realised that microseconds were in fact intended. It is the sort of slip, which would never have escaped Geoff Arnold's eagle eye. Evidently I'm not the calibre of proof-reader for whom Phil appealed in the leader page of that issue!

Ian Hickman
By email

The character of EW

I just bought the February 2004 *Electronics World* at the Cape Town Waterfront. I sat up on a balcony overlooking the Atlantic for breakfast, and read your editorial.

I have written for six electronics magazines during the past year, which included several cover articles (*EPE, Silicon Chip, Elektor*). I'm also a contributing editor of *Nuts & Volts* magazine.

Firstly, the fact that *Electronics World* still exists should be of great encouragement to you, only a handful of electronics magazines still do, and that is only because their editors were a cut above the rest, both in intellect and character.

Clearly *Electronics World* has had a distinctive character, and I myself have seen it as a magazine, above all, that goes just that much deeper than e.g. EPE magazine, while not becoming esoteric. A good example is Douglas Self's recent article on Electronic Analogue Switching.

In my view, the electronics magazines that succeed, do so mainly due to two things:

1. Substance, substance, substance, and
2. Giving contributors priority, with a warm and low-hurdle policy

Poptronics recently ceased publication as you will know, and I think that was due largely to their inordinate emphasis on flash, with little substance, and setting up unnecessary barriers for authors (e.g. the use of cutting edge cameras only, and a months-long approval process). I had the sense that the editor was a publisher first, not an electronics enthusiast.

EPE magazine, on the other hand, has been frowned upon by one or two of its competitors for its lack of flash; I was in one editor's office, and he was flapping about an edition of EPE, and he didn't think much of it, but EPE has substance, and I believe that that is what matters.

Diversity of content would probably also be a plus, and that would likely limit the length of articles. In my view, the SDI to Analogue Converter in my latest *EW*, at 13 pages, is very long, and is reminiscent of the overly long features that filled PE magazine towards the end of its life, not to detract from the value of the article in itself.

Your news items are good. Thinking again of Poptronics, they had news items, but again they were focussed on flash or hype, not on substance, and so they seemed empty. News items are good if they have substance, and identify truly significant developments, and I think you have that more or less right. It would also fit with a profile of 'going deeper'.

Well having said this, I wouldn't presume to know with any confidence what makes a magazine succeed, so these are just some thoughts from the ground. I hope you will both persevere and go from strength to strength.

Thomas Scarborough
Cape Town
Republic of South Africa

Thank you for your comments. It's good to think that we are read under such nice conditions. – Ed

Archiving

With regard to your suggestion of a workforce mobilisation to copy *EW/WW* back issues. I have, over many years, seen copies of documentation made by 'those who should know better' and even 'professional' copiers. Most of the copies have had either or all of the following: skewed, off centre, bottom missing, top missing, unreadable pages, pages with the most relevant information missing. No, I don't think it would be a good idea to have the average reader archive *EW/WW* to electronic media. I realise the cost of 'professional' companies and the return on sales of the finished result. I have *Wireless World* and *Electronics World* dating back to the Forties and earlier copies that are disintegrating into a pile if flakes. The most useful tool I find is a good index, preferably covering from the first issue (Vol1 No1) to date. More realistically it could be broken into 10-year lots. Those who do not have the advantage of such a vast library will most benefit from a set of archive CDs, 90 or so years worth. Which brings up another question - how far back would be a reasonable assessment for archiving? Some might argue that anything over, say 10 years would be too far, as the technology that far back would be outdated, outmoded and irrelevant. I, though, would not agree.

On the politically correct subject – 'master' and 'slave' are terms that cover more devices than one would, at first, appreciate. If it is to be taboo to use these words then 'primary' and 'secondary' would cover most of present master/slave usage and have the advantage of tertiary and perhaps quaternary, quinary, senary, septenary, octanary, nonary, denary undenary, duodenary etc. Other suggestions could be 'master' and 'submaster', 'master' and 'subordinate'. In personal computer usage 'primary' and 'secondary' are used to describe the IDE buss'. As the hard disk drives are not really 'master' and 'slave' devices they can be, and sometimes are, called Drive 0(zero) and Drive 1 - problem solved. Where two or more devices are configured in a manner that one device controls another, it is common to name the devices 'master' and 'slave' as it describes their function concisely and unambiguously. If it is the word 'master' that is objected to then we really are in trouble.

There are Harbour Masters, Headmasters (or are they called Head Teachers now), Ship's Master and many more. It is even possible to gain a Master's Degree. If it is the word 'slave' that is objected to, there is no equivalent word in the English language, so we will have to 'borrow' one from another language or invent a word which means 'slave'. But a slave by any other name is still a slave.

And anyone who equates the function of an inanimate object to that of a human being should first ask themselves who's thinking needs to change.

John E. Lavender
By email

802.11

Regarding Mr Long's letter in *EW* March referring to the paragraph in my 802.11 article (Jan 2004 *EW* issue page 46, bottom of middle column) about the numbering scheme used for the 802 committee.

The correct description should have been that the IEEE named their 802 committee after the second month of year 80, not the eighth week of the second month as printed.

Won't feel too guilty about this slip. I am sure many people ensnared in long drawn committees may quite believe that February has eight weeks rather than four.

Eddie Insam
By email

802.11

May I join the rush of email to claim the editor's special prize.

It is not *Electronics World* that Mr. Long should be castigating for inaccuracy. His ire should be directed to the IEEE.

Jan 2004 *EW* Page 46, centre column, last paragraph, says "IEEE sub- committees follow rather unsophisticated numbering scheme based on the week of creation: 802 is the 8th week of the second month, February."

Maybe they are operating in a different time frame to the rest of us?

Tony Meacock.
Norwich
UK

I'd often thought that was the case – Ed

Help wanted

I wonder if any of your readers can help me with a circuit I saw back in the 1960s or early 1970s.

It was a simple parametric down-converter that used ordinary transistors and allowed them to operate well above their cut-off frequency, e.g. up to 1GHz for a 300MHz silicon planar transistor.

I don't think it was a Wireless World circuit, though I could be wrong. In those days several magazines printed reader's circuits. Any pointers would be gratefully received.

Walter Gray
By email

Cathode Ray and M. G. Scroggie

In both guises, this gentleman served as my mentor. His lucid explanations of engineering fundamentals gave me an understanding that still serves me well fifty years later. I have amassed a collection of his books from used book Web sources like www.abebooks.com and www.alibris.com.

Cathode Ray wrote the excellent *Second Thoughts on Radio Theory* (1956). Both Scroggie and Cathode Ray gave us further thoughts in *Essays in Electronics* (1963). Scroggie authored; *Foundations of Wireless* (1958), *Radio Laboratory Handbook* (1961), *Principals of Semiconductors* (1961), *Television* (1952), *The Electron in Electronics* (1965). These are the details of my collection; titles do vary with impression and World region.

Sadly many of the books came from places like Bell Research Laboratories and Goonhilly Downs. These works strengthen our understanding of fundamental principals, what has replaced them? I would welcome further publications that collected the *Wireless World* articles by Cathode Ray.

M. J. Maytum, Senior Member, IEEE
Bedford
Bedfordshire
UK

Political correctness

I guess these will have been suggested, but I like the sound of:
'Dominant' and 'Submissive' or 'Mistress' (more PC) and 'Servant' or 'Menial' or any other bondage inspired names could be good, alternatively: 'Sayid' - Arabic name meaning Master and 'Obaid' ironically meaning Slave.

Alex Copland.
By email

CD offer

As a long time reader of more than 40 years, how about an offer on the archive CDs for subscribers (All 5 of them no messing about)?

Bearing in mind that we are mainly BOFs (Boring Old Farts) and on limited incomes it would help the groaning shelves.

A friend recently lent me some *Audio Amateur* magazines from the United States and I was amazed to read an interview with Peter Baxandall (issue dated 1/1980) in which he mentions an audio sweep generator. This was prompted by a *Circuit Idea* in *Wireless World*. He failed to get it taken up and into production. Someone must know of this device and I would urge you to publish a request for details. It would, I think, make a fitting memorial to a great man, and in the best traditions of 'our' magazine.

Keep up the good work and I hope we will still have the option of a 3 year subscription again this year.

Peter Dorey
Bournmouth
Dorset
UK

We are running a 'buy four, get one free' offer at the moment and you can now 'trade in' payment for Circuit Ideas for one. Unfortunately, these cost a lot to produce, as the labour involved in cataloguing, and generally 'electrifying' some of the older stuff is very time consuming. However, I am currently working out a 'points' system for those of you who have offered to help with the scanning of old issues, which you could use to purloin free CDs. – Ed

Audible distortion

A while back articles for beginners were printed in *EW/WW* to interest young people to buy *EW/WW* and learn basic electronics what would they fell like if Seb criticised them for writing in, he is the reason lots of ordinary people like myself stopped Buying *EW/WW*. Is Seb saying that certain manufacturers introduce distortion into Power Amps?

My amp started out as a basic JLH design with distortion of –78dB at 10kHz, after expansion by me it is now –95dB at 20kHz. No added 'niceness'. On the contrary, I am in total agreement with Graham Maynard, *Letters* January 2001, I quote "the resulting reproduction might sound sweet, but is not accurate." I am also in agreement, "with his God." D.Self, there is no filter at my amp's input. Regarding Graham's comment about loss of definition on transient and sibilant sounds, I have tested and found to be correct, no computer here. I also agree with Cyril Bateman, all my small value capacitors are 1950s air-spaced 'beehive' capacitors, you can't beat air.

Time and again I found amps I repaired had inbuilt crossover distortion and large amounts of noise both cause sibilance to sound very rough, I wasn't being paid to improve fidelity only bring to working order. I found it is a total waste of time fitting high quality capacitors and resistors at the input under those conditions and that 'golden ears' approval of low/nil negative feedback causing large amounts of crossover distortion can never sound good, I also used D.Self's methods of power-supply noise rejection, and while working on my expanded amp I found JLM's tuning and feed-back methods were no longer viable after testing by various methods. I found that D.Self's methods were reliable under change of circuit conditions and all that was required to obtain a 90° leading edge on a 1kHz square wave was a slight adjustment of the small value variable capacitor in series with a resistor from the out put to the inner base of the input differential pair. So you see I put my money where my mouth is - if it works I use it, no bigotry here, or subjectivity. And what about Cyril Bateman's 'capacitor sounds'? He's proved electronics and PET capacitors at the input and negative feedback can introduce distortion, a man who has said in the past that he is 'anti-subjective.' I've had polyprop capacitors in those positions for 14 years - are you going to argue with Cyril? Using Seb's logic, D. Self builds and sells nil distortion amps. Thousands of others at home and abroad sell nil distortion amps do they sound the same and if not why not? Are you saying some amplifier designers and manufacturers introduce distortion into their amps? I hope you've a good lawyer - a straight yes or no. Seb, are you saying that there are components fitted to power amps that change the 'sound' of that amp without showing up as distortion? If so why do you not believe that types of capacitors affect the fidelity of power amps, you can't have it both ways?

On a different tack why do many audio designers and engineers have audio amps designed by others, usually very expensive? If I were an audio designer I would lock myself in a room with a fridge, cooker and bed and not come out till I had designed a nil distortion amp, to equal the top of the range models. My amp is different from anybody else's and I get great enjoyment knowing that I built it myself.

Lastly, when working on my amp, I kept blowing the small signal mosfets in the Vas stage - the series BJT never blew, I put in a high current mosfet in both channels till I had finished working on the circuits. It proved bomb proof. When I had sorted things out I was so fed up with them I bought several SND mosfets from Maplin and using my bench magnifier and weller pointed tip soldering iron, I soldered them in to both channels, you could hardly see the SND for the solder blobs, and the result totally reliable, so my next power amp will be all SND components, in the future.

D. Lucas
Anstruther
Fife
Scotland UK

Political correctness

With regard to the requirements of Los Angeles County - who have objected to the use of 'master' and 'slave' - they could try what I just did and use quotes. They would probably love 'Hierarchical address sending and synchronising reference unit' giving not instructions, but helpful suggestions that other devices would only act on if they really wanted to. If they chose to, these devices could call themselves 'Synchronous address location units'. My first choice was Monarch and subject, with leader and follower a close second. VTR manufacturers have it covered already - the sockets are labelled 'RS422'.

In the actual world where VTRs are connected to edit controllers and audio workstations, the VTR master is actually controlled by the slave - play, stop, and rewind are usually software controls on the slave device the editor is using.

Los Angeles County might want to consider their name. 'The Angels' could cause considerable offence to those whose religious beliefs did not incorporate angels, and someone with no religious beliefs might well consider the beliefs of others were being imposed on them. The use of Spanish denies knowledge to non-speakers of this language. 'The County Of The Mythical Flying Sub-Deities' (in Esperanto) would surely be less likely to cause any offence.

Do you think we should let them know that the master VTR is itself slaved, or would the use of the terms 'black' and 'colourburst' further muddy these uncharted waters?

Colin Macnab (freelance sound mixer)
Edinburgh
UK

Airborne lasers

I think that Edward Phelan has been unintentionally misled by the pilot he talked to (Airborne lasers letters *EW* March 2004). It is virtually impossible for any laser light to escape from a CD or DVD player and affect any system, never mind get into the avionics bay, inside an inertial navigation system and affect the ring laser gyro therein. The reason for banning the use of electronic devices during critical phases of flight, i.e. takeoff and landing is to prevent EMC of the RF variety. In the cruse phase the pilot has time to recognise and respond to problems, this may not be the case when close to the ground. Reported incidents span many frequencies and systems. The problem was first noted when 'Walkman' tape players became popular. Some models had bias oscillators that ran at frequencies close to the Omega VLF long-range navigation system. The problem was normally isolated to certain seats near the antenna. It fact the pilots got to the point of telling the cabin crew which seat the offender was in! This particular problem has ceased with the demise of the Omega system. However other possibilities for interference exist. The local oscillator of a VHF FM radio can fall in the VOR/ILS band, and while a problem should be signalled by a failure flag in the pilot's display, a dormant fault could prevent adequate warning. Harmonics of VHF local oscillators can also affect GPS signals. Even some aircraft radios themselves have caused this problem. Cell phone spurious emissions can fall in the DME frequency range and any powerful RF such as from a cell phone can be induced into the aircraft wiring. The Aircraft and Avionics manufacturers are working to improve immunity, but the consumer market moves much faster than conservative aviation.

Robert Atkinson, MRAeS, G8RPI
Christchurch,
Dorset

Airborne Lasers

Referring to the letter in *EW* March, I think Edward Phelan has 'been had', we pilots do enjoy the same game as any other activity that involves a certain amount of specialist knowledge, namely 'what misinformation can we make some gullible member of the public believe'. I know I've been on the receiving end from sailing friends!

Consider this, your laser light escapes from a CD player. Once it's away from the zone where the disk may reasonably be found it quickly loses focus. The materials lining the cabin are not exactly highly reflective so any energy 'bouncing around' will quickly disperse - it would be well and truly scattered (or absorbed) by the first reflection.

The light would then have to make it's way through closed hatches into the avionics bay, into a sealed box, and break into the fibre arrangement which is tightly coupled to the optical transmitters and receivers. No, I don't think we need worry about that!

.As to the preference for 'an old type spinning top', well I'd prefer a ring laser gyro - far more accurate and reliable. Not many people realise that the best, most accurate, gyrocompasses drift by 15' per hour and need to be corrected. To this end, on all but the most basic aircraft the compass is being constantly corrected by reference to the earth's magnetic field detected by a sensor placed (typically) right at the end of a wing away from anything in the plane that could upset it. In the event of a malfunction, then this would be more apparent with a ring laser gyro as it can be monitored much more comprehensively (and an alarm raised in the event of malfunction) than an 'old type spinning top' where the only practical monitoring is 'is it spinning?'

However, that all assumes that the compass is as important as some people believe. Apart from the fact that there is more than compass one on a commercial aircraft (even the biggest jumbo still has a magnetic compass in the cockpit), it is only used as part of the navigation. While within range, ground based radio facilities are used for navigation, with the compass only used to maintain a steady heading. Should the compass drift then the heading would be adjusted to maintain the correct track according to the radio navigation - this is no different to the adjustments required to cater for variations in wind speed and direction.

The main principles of air navigation are driven by the basic principle of redundancy - use one tool for primary navigation, and at least one other tool as a check. Don't forget that most of the time, there are two pairs of the oldest navigation tool in existence at work - the Mk1 eyeball!

Only when out of range of land based radio navigation facilities would the compass and dead-reckoning become the primary navigation tool. The airways across the Atlantic are very wide to allow for the uncertainties inherent in dead reckoning.

And finally, bear in mind that anything with an avionics fit modern enough to include a ring laser gyro is almost certain to include a GPS which is by far the most accurate navigation tool available.

Simon Hobson
Ulverston
Cumbria
UK

More errors

I was pleased to see my circuit idea Absolute Harmonic Filter for RF which appeared in the March 2004 edition. I was disappointed, however, to see that all the omega symbols had been changed to capital Ws. I understand that Quark on the Mac 'scrambles' several Word 95 symbols, but it has always done this. Indeed in a previous article, there were a couple of letters sent in by readers to correct 'my error' which was another editorially induced translation artefact (converting a mu symbol to an "m"). Come on Phil, 'fess up, and issue a final layout checklist item to view the original source for symbols which will not have converted correctly. In the meantime, readers can take it as a challenge to decrypt the articles, working out where the 'W' means watts and where it means ohms, and where an 'm' means micro-rather than milli-.

Whilst we are on the subject of editorial checklists, the article Hybrid Audio Amplifier in the March edition had a generous helping of that old favourite techno-babble phrase 'Watts RMS'. The checklist item should say something like, 'If Watts, or W, appears next to RMS it is wrong. Delete the 'RMS' and replace it by 'mean'."

Leslie Green CEng MIEE
Ilford, Essex
UK

As I mentioned in last month's editorial, we do have a vacancy for a part-time proof reader. And yes, even in today's 'interoperable' world, PCs and Macs still do not completely see eye to eye and Quark remains one of the most awful pieces of software around, if you are an engineer. Apologies to all. – Ed.

Pedant Club

Your response to Paul Bartlett is unfortunate. As editor, surely you should be keen to uphold standards of good grammar, for the sake of clarity, if nothing else. Treating those of your readers who clearly care about the quality of your publication's content a good deal more than you do in such a flippant, offensive manner is not conducive to improving its reputation.

Martin Sadler
By email

Of course. But sometimes I do think that letter writer's time might be spent more productively – by addressing more important issues. – Ed

A *v* D

Sorry, Ed. On this one I'm with 'pedant' Mr. Paul Bartlett (Letters, March 04). 'Less' is an analogue word while 'fewer' is digital. They are not interchangeable. Would you say: 'I shall take less calories by eating fewer butter'?

In electronics we demand nothing fewer than precision. We should therefore expect no fewer precision in the use of the language which describes our interest.

David Ponting
Clutton, Bristol
UK

OK – I give up. – Ed

The safe route

Your editorial plea (February issue) for comments from non-readers deserves some replies. Your predecessor made EW a rather dull read for the most part. However, one of your earlier predecessors made it very interesting, by publishing articles by people with interesting ideas that could not get printed in the standard scientific and technical journals.

The problem, as Ivor Catt has pointed out many times, is orthodoxy. The former editor of Nature remarked that these days even Watson and Crick's paper on the double helix could not get published. This reveals a fearful protection of safe thinking rather than scientific thinking.

The basic point we should keep in mind is that all our theories are models of reality, not reality itself. I do not believe the human mind is capable of any idea that is 'right'. The history of ideas and specifically of scientific theories, should be enough to convince anyone of that, who is not determined to believe that suddenly, in this generation, we have acquired perceptions and mental skills denied to all our ancestors.

In electronics, there is now a great deal of work on 'evolutionary design', by which a computerised design process iteratively changes the design of a circuit until its performance is very good at which point typically electronic theory is unable to explain how it works. As the old joke went, avionics design is 'two days to design and four years to get the bugs out'. The two days is according to theory, the four years is struggling to accommodate to reality.

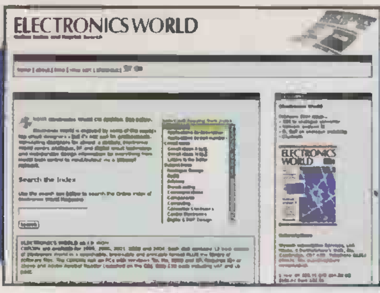
One topic recently in the letters is Maxwell's equations. I do not need to denigrate them: they are an awesome achievement. However, Hertz (or was it Helmholtz?) found their meaning baffling, which is not surprising. Maxwell based them on behaviour of fluids, but modern physical theory says there are no fluid and nothing that behaves like a fluid.

On basic principle, then, there has to be something wrong with the underlying assumptions. Also, as Phipps has remarked, they conflict with the relativity principle at first order; and deal with field source motions but not field sink motions.

I would urge you, then, to be more adventurous.

Roderick Rees
Woodinville
Washington
U.S.A

Thank you for the laying down of that particular gauntlet. – Ed



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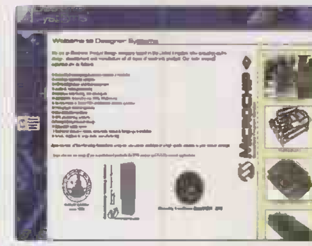

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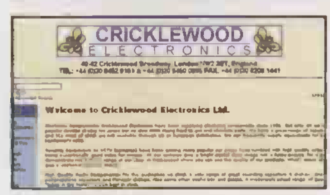

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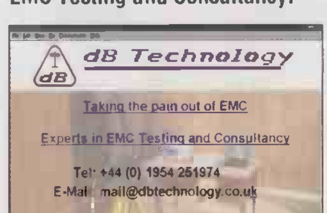

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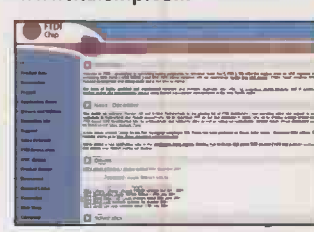

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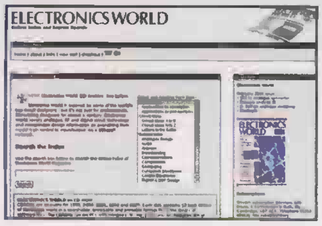

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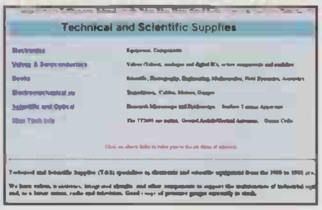

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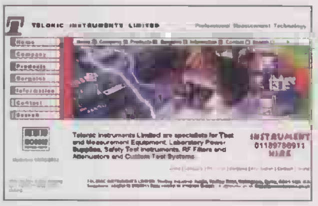

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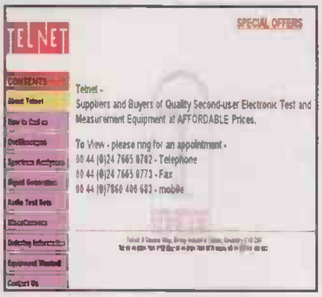

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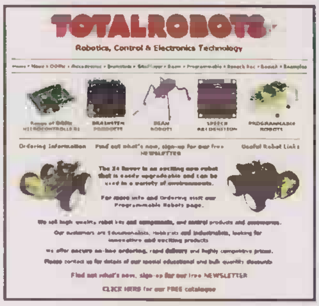

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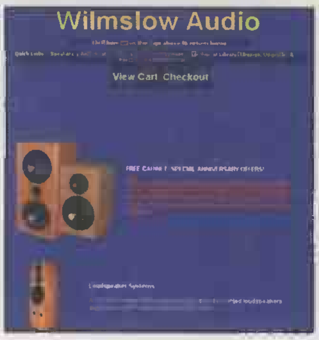

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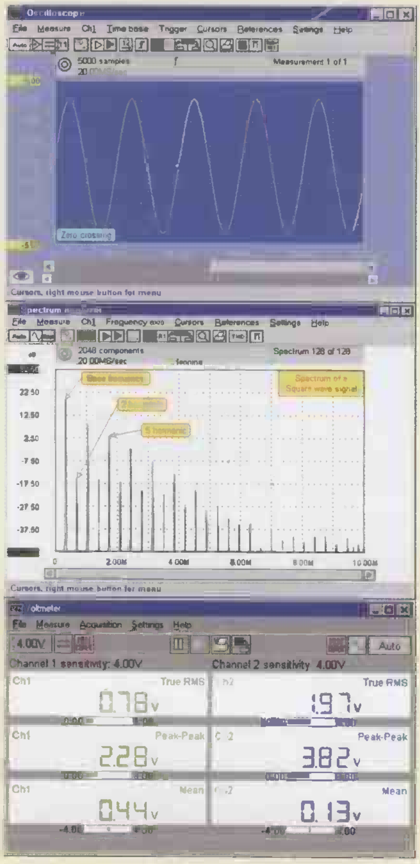

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