Australia $1.50 New Zealand $1.75 Malaysia $4.95

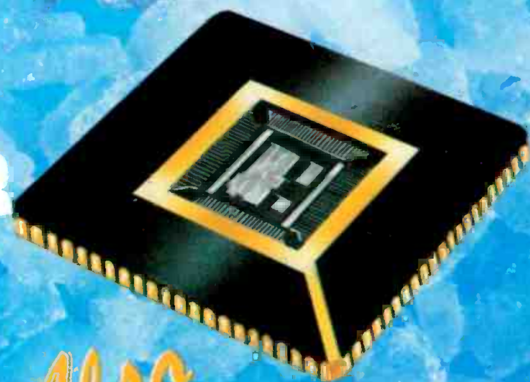
PRACTICAL ELECTRONICS

90p

APRIL 1984

STEP & FREEZE INSTRUCTIONS with the MICROSTEPPER

FEATURE ARTICLE
TRANSPUTER



FREE PE LOGIC DESIGN CARD-No2

Also in this issue!

PRACTICAL
ELECTRONICS

VOLUME 20 No. 4 APRIL 1984

CONSTRUCTIONAL PROJECTS

GENERAL FEATURES

NEWS AND COMMENT

OUR MAY ISSUE WILL BE ON SALE FRIDAY, APRIL 6th, 1984
(for details of contents see page 61)

WATFORD ELECTRONICS

33, CARDIFF ROAD, WATFORD, HERTS WD1 8ED, ENGLAND

Tel. Watford (0923) 40588. Telex: 8956095 WAELEC

ORDERS NORMALLY DESPATCHED BY RETURN OF POST

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POLYESTER RADIAL LEAD CAPACITORS: 250V; 10n, 20n, 15n, 22n, 27n **6p**; 33n, 47n, 68n, 100n **8p**; 150n, 220n **10p**; 330n, 470n **15p**; 680n **19p**; 1µ **23p**; 1µ5 **40p**; 2µ2 **46p**.

ELECTROLYTIC CAPACITORS (Values in µF) **500V:** 10µF **52p**; 47 **78p**; **63V:** 0·47, 1·0, 1·5, 2·2, 3·3, **8p**; 4·7 **9p**; 10 **10p**; 15, 22 **12p**; 33 **15p**; 47 **12p**; 68 **16p**; 100 **19p**; 220 **26p**; 1000 **70p**; 2200 **99p**; **50V:** 68 **20p**; 100 **17p**; 220 **24p**; **40V:** 6·8 **15p**; 22 **9p**; 33 **12p**; 330, 470 **32p**; 1000 **46p**; 2200 **90p**; **25V:** 4·7, 10, 22, 47 **8p**; 100 **11p**; 150 **12p**; 220 **15p**; 330 **22p**; 470 **25p**; 680, 1000 **34p**; 1500 **42p**; 2200 **50p**; 3300 **76p**; 4700 **92p**; **16V:** 2·5, 40 **8p**; 47, 68, 100 **9p**; 125 **12p**; 220 **13p**; 330 **16p**; 470 **20p**; 680 **34p**; 1000 **27p**; 1500 **31p**; 2200 **36p**; 4700 **79p**.

TAG-END TYPE: 64V: 4700 **245p**; 3300 **198p**; 2200 **139p**; **50V:** 3300 **154p**; 2200 **110p**; **40V:** 4700 **160p**; **25V:** 4700 **98p**; 10,000 **320p**; 15,000 **345p**.

TANTALUM BEAD CAPACITORS:
35V: 0·1µ, 0·22, 0·33 **15p**; 0·47, 0·68, 1·0, 1·5 **16p**; 2·2, 3·3 **18p**; 4·7, 6·8 **22p**; 10 **28p**; **16V:** 2·2, 3·3, **16p**; 4·7, 6·8, 10 **18p**; 15 **36p**; 22 **36p**; 33, 47 **50p**; 100 **95p**; 220 **100p**; **10V:** 15, 22 **26p**; 33, 47 **50p**; 100 **75p**.

POTENTIOMETERS: Carbon Track, 0·25W Log & Linear Values.

500Ω, 1K & 2K (LIN ONLY) Single	34p
5KΩ-2MΩ single gang	34p
5KΩ-2MΩ single gang D/P switch	80p
5KΩ-2MΩ dual gang stereo	90p

SLIDER POTENTIOMETERS
0·25W log and linear values 60mm track 5KΩ-500KΩ Single gang **70p**

SILVER MICA (pf)
2, 3·3, 4·7, 6·8, 8·2, 10, 12, 18, 22, 27, 33, 39, 47, 50, 56, 68, 75, 82, 85, 100, 120, 150, 180 **15p**. 220, 250, 270, 330, 360, 390, 470, 600, 800 & 820pF **21p**. 1000, 1200, 1800 **30p each**. 3300, 4700 **60p each**

SIEMENS multilayer miniature capacitors. **250V:** 1nF, 1n5, 2n2, 3n3, 4n7, 6n8, 8n2, 10n, 15n, 22n **7p**; 18n, 27n, 33n, 47n **8p**; 39n, 56n, 68n **9p**, 100nF **11p**.
100V: 100n, 120n, **10p**; 150n **11p**; 220n **13p**; 330n **18p**; 470n **23p**; 680n **30p**; 1µF **34p**; 2µ2 **50p**.

PRESET POTENTIOMETERS

0·1W 50Ω-2·2M Mini Vert. & Horiz.	8p
0·25W 220Ω-4M7 Vert. & Horiz.	12p

RESISTORS Hi-stab, Miniature, 5% Carbon.

	RANGE	Val.	1-99	100+
0·25W	2Ω2-4·M7	E24	3p	1p
0·5W	2Ω2-4·M7	E12	3p	1p
1W	2Ω2-10M	E12	6p	4p
1% Metal Film 51Ω-1M		E24	8p	6p

CERAMIC Capacitors: 50V
Range 1pF to 6800pF **4p**; 10nF, 15n, 33n, 47nF **5p**; 100nF/30V **7p**.

POLYSTYRENE Caps:

10pF to 1nF	8p
1n5 to 12nF	10p

RESISTORS S.I.L. Package: 7 Commoned, 100Ω, 680Ω, 1K, 2K2, 4K7, 10K, 47K, 100K **24p**.
8 Commoned: (9 pins) 150Ω, 180Ω, 270Ω, 330Ω, 1K, 2K2, 4K7, 6K8, 10K, 22K, 47K, 100K **26p**.

TRANSISTORS

AC127/8	35
AC141/2	35
AC176	35
AC187/8	35
AC188	35
AD142	120
AD149	79
AD161/2	42
AF118	95
AF139	40
AF239	55
BC107/8	12
BC107B	14
BC108B	14
BC108C	14
BC109	12
BC109B	14
BC109C	14
BC114/5	30
BC117/8	25
BC140	38
BC142/3	38
BC147/8	12
BC147B	15
BC148C	10
BC149	12
BC149C	15
BC153/4	30
BC157/8	14
BC159	11
BC167A	14
BC168C	12
BC169C	12
BC171/2	12
BC173	15
BC177/8	16
BC179/81	20
BC181	30
BC182/3	10
BC184	10
BC182L	10
BC183L	10
BC184L	10
BC186/7	28
BC212/3	12
BC212L	10
BC213L	12
BC214	10
BC214L	12
BC237/B	15
BC307B	15

BC308B	16
BC327/8	15
BC337/8	15
BC441	34
BC461	34
BC477/8	40
BC516/7	40
BC547/8	12
BC549C	15
BC556/7	15
BC558/9	15
BCY41/42	30
BCY70	18
BCY71/2	20
BCY72	25
BCY78	30
BD131/2	65
BD133	60
BD135	45
BD136/7	40
BD138/9	40
BD140	40
BD158	68
BD245	65
BD434	70
BD695A	150
BD696A	150
BF115	45
BF154/8	30
BF167	35
BF173	35
BF177	35
BF178	35
BF179	40
BF194/5	12
BF198/9	18
BF200	30
BF224	40
BF244A	28
BF244B	29
BF245	50
BF256B	50
BF257/8	32
BF259	40
BF394	40
BF451	40
BF494/5	40
BF594/5	30
BFR39/40	25
BFR41/79	28
BFR80/81	25

BFR98	105
BFX29/84	35
BFX84	35
BFX85/86	35
BFX87/88	28
BFY50/51	30
BFY52	30
BFY53	35
BFY55	35
BFY56	35
BFY64	40
BFY90	80
BRY39	50
BSX20	30
BSX29	45
BSY26	35
BSY95	35
BU105	180
BU205	190
BU206	200
BU208	200
MJ2955	90
MJE340	54
MJE371	100
MJE2955	99
MJE3055	70
MPF102	40
MPF103/4	30
MPF105	30
MPSA05	30
MPSA06	25
MPSA08	30
MPSA12	32
MPSA55	30
MPSA56	30
MPSA70	40
MPSU02	58
MPSU05	60
MPSU06	60
MPSU52	65
MPSU55	60
MPSU56	60
OC23	170
OC28/36	220
OC41/42	75
OC70	40
OC72	50
OC75/76	55
OC76	50
OC81/82	50
OC83/84	70
TIP29A	32
TIP29C	38
TIP30A	35

TIP30C	37
TIP31A	38
TIP31C	45
TIP32A	43
TIP32C	45
TIP33A	70
TIP33C	75
TIP34A	85
TIP34C	105
TIP35A	120
TIP35C	130
TIP36A	130
TIP36C	140
TIP41A	50
TIP41B	52
TIP42A	55
TIP42B	58
TIP120	70
TIP121	73
TIP141	120
TIP142	120
TIP147	120
TIP2955	70
TIP3055	70
TIS43	50
TIS44	45
TIS88A	50
TIS90	30
TIS91/93	32
VK1010	99
VN10KM	70
VN46AF	95
VN66AF	110
VN88AF	120
VN89AF	120
ZTX107/8	12
ZTX109	12
ZTX212	28
ZTX300	13
ZTX301/2	16
ZTX303	25
ZTX304	17
ZTX320/26	30
ZTX500/1	14
ZTX502/3	18
ZTX504	25
ZTX531	25
ZTX550	25
2N696	30
2N697	23
2N698	40
2N699	48
2N706A	25
2N708	25

2N914/5	32
2N918	40
2N930	20
2N1131/2	30
2N1303/4/5	
2N1307/8	65
2N1613	30
2N1671B	160
2N2160	325
2N2219A/20A/	
21A/22A	25
2N2369A	18
2N2646	45
2N2846	80
2N2904A/05A/	
06A/07A	26
2N2926G	10
2N3053	25
2N3054	55
2N3055	50
2N3442	140
2N3615	199
2N3663	20
2N3702/3	10
2N3704/5	10
2N3706/7	10
2N3708/9	10
2N3710	10
2N3771	179
2N3772	195
2N3773	210
2N3819	30
2N3820	50
2N3822/3	45
2N3866	90
2N3903/4	15
2N3906/5	15
2N4037	60
2N4058	15
2N4061/2	15
2N4264	30
2N4286	25
2N4289	25
2N4400	25
2N4427	80
2N4859	78
2N5135	30
2N5138	25
2N5172	25
2N5180	45
2N5191	75
2N5194	80
2N5305	24
2N5457	30

2N5458/9	30
2N5485	36
2N5777	45
2N6027	32
2N6109	60
2N6290	70
2SA636	250
2SA671	250
2SA715	75
2SC495/6	85
2SC1061	250
2SC1096	85
2SC1162	45
2SC1172/3	125
2SC1306	100
2SC1307	150
2SC1449	95
2SC1679	190
2SC1678	140
2SC1923	65
2SC1945	225
2SC1953	90
2SC1957	90
2SC1969	140
2SC2028	85
2SC2029	200
2SC2078	170
2SC2091	85
2SC2166	165
2SC2314	85
2SC2335	200
2SC2465	125
2SC2547	40
2SC2612	200
2SD234	75
2SK45	90
2SK288	225
2SJ83	225
2SJ85	225
3N128	115
3N140	115
40251	150
40311	60
40313	130
40361/62	70
40408	76
40412	90
40467	130
40468	85
40594	105
40595	110
40603	110
40673	70
40871/2	90

LINEAR IC's

555 CMOS	95
702	75
709C 8 pin	35
710	48
741	16
747C 14 pin	70
748C 8 pin	30
753 8 pin	185
810	159
9400CJ	375
AY-1-1320	225
AY-1-5050	99
AY-1-5051	160
AY-1-6720	210
AY-3-1270	730
AY-3-8910	400
AY-3-8912	500
AY-5-1230	450
AY-5-1317A	630
CA3011	130
CA3012	175
CA3014	275
CA3018	86
CA3019	80
CA3020	210
CA3023	210
CA3028A	110
CA3035	255
CA3036	270
CA3043	275
CA3045	365
CA3046	70
CA3048	220
CA3059	325
CA3075	213
CA3080E	70
CA3081	190
CA3085	00
CA3086	60
CA3089E	200
CA3090AO	375
CA3123	165
CA3130	90
CA3140	45
CA3160	95
CA3161E	160
CA3189	275
CA3240	110
HA1366	175
HA1388	255
ICL7106	690
ICL7107	975
ICL7611	99
ICL7660	248
ICL8038CC	300
ICL8211	350
ICM7205	1150
ICM7207	475
ICM7215	1050
ICM7216A	£22
ICM7217A	750
ICM7224	785
ICM7240	300
ICM7555	95
ICM7556	150
LA3350	250
LA4031P	340
LA4032	295
LA4400	350
LA4422	320
LC7120	300
LC7130	320
LC7137	350
LF347	150
LF351	50
LF353	90
LF355	90
LF356	95
LF357	110
LF398	495
LM10	350
LM301A	25
LM307	45
LM308	95
LM311	65
LM318	150
LM319	160
LM324	35

LM334Z	90
LM335	135
LM337	00
LM339	40
LM348	60
LM349	125
LM358	60
LM377	215
LM379	495
LM380	75
LM381N	175
LM382	115
LM384	190
LM386	90
LM387	120
LM389	95
LM393	85
LM394CH	290
LM558	170
LM725CN	300
LM733	60
LM1871	300
LM1889	350
LM2907	00
LM2917	200
LM3900	50
LM3909	85
LM3911	150
LM3914	200
LM3915	200
LM3916	250
LS7220	280
M51513L	230
M51515L	320
M51516L	475
M706B1	150
MB3712	200
MB3756	440
MC1204	250
MC1301	90
MC1303	98
MC1304P	260
MC1310P	150
MC1445	250
MC1455	50
MC1458	35
MC1469	300
MC1494	694
MC1495	350
MC1496L	70
MC1596	225
MC1648	290
MC3302	75
MC3340	145
MC3360	145
MC3401	50
MC3403	65
MC3404	65
MC3405	150
MC3442	00
MC3423P	80
MC3487	00
MC4016	00
MF10	350
MFC6040	75
MK50398	775
ML924	275
NE515	275
NE529	225
NE531	140
NE543	225
NE544	200
NE555	18
NE556DB	45
NE558	170
NE560	350
NE561	395
NE562B	410
NE564	420
NE565A	120
NE566	155
NE567	140
NE570	410
NE571	400
NE5532	175
NE5534	105
OM335	750
RC4136D	60

RC4558	60
S566B	225
SAB3209	425
SAB3210	325
SAB3271	485
SAB4209	595
SG3402	295
SL490	350
SL924	00
SL6270	150
SN76013N	350
SN76023N	350
SN76033	350
SN76488	480
SP8629	00
SP0256AL	850
TA7120	140
TA7130	125
TA7204	150
TA7205	175
TA7222	150
TA7310	00
TAA900	395
TAA621	275
TAA661	190
TAA700	275
TAD100	159
TBA120S	70
TBA540	275
TBA550Q	330
TBA641	290
TBA651	190
TBA800	80
TBA810S	95
TBA820	80
TBA920Q	200
TBA990	350
TCA270	350
TCA280A	220
TCA940	175
TCA950	00
TCA965	125
TDA1004	350
TDA1008	310
TDA1010	225
TDA1022	499
TDA1024	115
TDA1034	350
TDA1054	00
TDA1490	350
TDA2002	325
TDA2003	250
TDA2004	400
TDA2006	330
TDA2020	320
TDB0791	420
TL061CP	40
TL062CP	60
TL064CN	98
TL071CP	30
TL072CP	45
TL074CN	100
TL081CP	24
TL082CP	45
TL083CP	75
TL084CP	90
TL091CP	55
TL170	50
TL430C	90
TL507	110
TL509	110
UA2240	120
UA78540	230
UAA170	180
UAA180	180
ULN2003	75
ULN2004	75
ULN2283	100
UPC556	00
UPC575	275
UPC1025H	375
UPC1156H	295
UPC1181	00
UPC1182	425
UPC1366	195
XR2206	375
XR2207	400
XR2211	575
XR2216	675
XR2266	360

ZN414	90
ZN419CE	180
ZN423E	130
ZN424E	130
ZN425E-8	345
ZN426E-8	300
ZN427E-8	590
ZN428E	435
ZN429E-8	210
ZN459	280
ZN1034E	200
ZN1040E	665
ZNA234E	925

COMPUTER IC's

2102L	100
2114L-200n	150
2147-3	425
2532-3	270
25L32	450
2564	700
27L08	450
2716-5V	270
2732	320
2764-250	595
26501	75
27128/250n	£18
3242	590
4027	95
4116-150	100
4116-200	495
4416-2	475
4532-3	325
4816-100ns	300
5101	220
5514	250
6116-150ns	495
6116L-120ns	525
6117-100n	490
6167-6	795
6264L-15	£26
6402	350
6502 CPU	325
6502A	650
6503	650
6504	600
6505	650
6520	00
6522 VIA	295
6530 RRIOT	£11
6532 RIOT	570
6545 CRTC	899
6551 ACIA	650
6592	00
6800	220
6802	250
6803	350
6805	670
6808	520
6809	350
6810	115
6821	120
6840	370
6843	750
6845	625
6846	250
6847	180
6850	110
6852	250
6854	799
68B54	780
6875	700
68000	550
8035	650
8080A	800
8085A	850
8088	725
81LS95/96	120
81LS97/98	120
8123	120
8131	275
8154	£9
8155	350
8156	350
8202	£25
8212	150

8214	425
8216	100
8224	150
8226	250
8228	220
8236	00
8243	270
8250	950
8251A	250
8253	400
8255	275
8256A	£35
8257A	400
8259	395
8271	£55
8272	£17
8279	385
8282	450
8283	450
8284	350
8288	00
8T26A	99
8T27	150
8T28A	120
8T31	350
8T95N	90
8T97N	90
9364AP	550
9602	220
AM26LS31C	125
AM26LS32	100
AM26LS32A	125
AM26LS33	150
AY-3-1015	300
AY-5-1013	300
AY-5-1350	388
AY-5-2376	600
AY-5-3600	750
COM8017	275
COM8116	700
DM8131	275
DP8303	00
DP8304BN	250
DS3647	00
DS3691N	00
DS8820	110
DS8830	110
DS8831	125
DS8832	250
DS88LS120	00
E9364	00
E9365	£38
FD1691	£15
FD1771	£15
FD1791	£22
FD1793	£23
FD1795	£28
FD1797	£28
HD26501	75
IM6402	350
INS8060N	1050
MC1488	55
MC1489	55
MC14411	675
MC14412	725
MC3242	590
MC3446	250
MC3447P	315
MC3486	175
MC3487	175
MK3886-2M	£7
MM5280D	695
MM5303	635
MM5307	1275
MM5387A	475
MM58174	700
RO-3-2513L	550
RO-3-2513U	650
SFF96364E	800
SP0256AL2	850
TMS2716-3	725
TMS4047	100
TMS4164-15	395
TMS4416-2	475
TMS4500	£14
TMS4532-3	350
TMS5100	600
TMS6011	500
TMS9927	£14
TMS9928	£20

TMS9929	£16
TMS9980	£20
TMS9995	£12
ULN2003	75
UPD7002	425
WD1691	£14
Z80CPU 2·5	299
Z80ACPU4M	300
Z80ACTC	260
Z80B	875
Z80DART	495
Z80ADART	550
Z80ADMA	895
Z80DMA	695
Z80P10	260
Z80AP10	275
Z80S10-1	850
Z80AS10	900
Z80AS10-2	00
Z8002CPU	00

74S

74S00	30
74S02	30
74S03	35
74S04	40
74S05	60
74S08	60
74S09	00
74S10	40
74S11	50
74S15	00
74S20	40
74S22	50
74S30	40
74S32	70
74S37	60
74S38	00
74S40	00
74S51	00
74S64	00
74S65	00
74S74	75
74S85	295
74S86	70
74S112	90
74S113	90
74S114	80
74S124	300
74S132	110
74S133	60
74S134	00
74S135	00
74S138	100
74S139	115
74S140	60
74S151	180
74S153	182
74S157	250
74S158	195
74S162	00
74S163	300
74S168	00
74S169	00
74S174	250
74S175	320
74S181	00
74S182	00
74S188	140
74S189	140
74S194	295
74S195	275
74S196	00
74S197	400
74S201	350
74S225	500
74S226	00
74S240	300
74S241	300
74S244	290
74S251	225
74S257	225
74S258	250
74S260	70
74S262	850
74S274	00
74S275	00
74S280	00
74S281	00

74S283	00
74S287	225
74S288	210
74S289	200
74S299	540
74S301	350
74S365	250
74S373	400
74S374	365
74S412	380
74S470	325
74S471	620
74S472	1150
74S473	00
74S474	400
74S475	800
74S571	620
74S573	950

75

75107/8/	95
75110	90
75114	00
75121	00
75122	00
75150	125
75151	00
75154	195
75158	00
75159	125
75182/3	99
75188/9	55
75322	140
75324	00
75325	00
75353	00
75361	00
75365	00
75376	00
75450	86
75451/2	52
75454	70
75491/2	65

TTL 74

7400	20
7401	20
7402	20
7403	22
7404	22
74L04	00
7405	25
7406	125
7407	125
7408	25
7409	25
7410	25
7411	25
7412	25
7413	35
7414	50
7416	35
7417	35
7420	22
7421	22
7422	30
7423	30
7425	30
7426	45
7427	30
7428	30
7430	25
7432	25
7433	25
7437	30
7438	55
7440	25
7441	65
7442	55
7443	70
7444	65
7445	80
7446	78
7447	70
7448	75
7450	25
7451	25
7453	25

7454	25
7460	25
7470	35
7472	35
7473	35
7474	35
7475	60
7476	40
7480	55
7481	120
7482	100
7483	65
7484	90
7485	110
7486	40
7489	175
7490	40
7491	55
7492	45
7493	40
7494	80
7495	50
7496	60
7497	120
74100	100
74104	55
74105	55
74107	40
74109	50
74110	50
74111	60
74112	170
74116	100
74118	100
74119	105
74120	90
74121	40
74122	50
74123	80
74125	50
74126	50
74128	60
74132	60
74136	40
74141	75
74142	195
74143	200
74144	200
74145	80
74147	105
74148	105
74150	125
74151	50
74153	50
74154	100
74155	50
74156	50
74157	50
74159	130
74160	50
74161	50
74162	55
74163	55
74164	65
74165	65
74166	80
74167	200
74170	175
74172	280
74173	80
74174	100
74175	70
74176	50
74177	50
74178	80
74179	80
74180	50
74181	140
74182	55
74184	110
74185	110
74186	70
74188	75
74190	70
74191	75
74192	75
74193	60
74194	50
74195	50
74196	60

74197	50
74198	110
74199	110
74221	90
74246	120
74247	120
74248	175
74249	120
74251	55
74259	150
74265	50
74273	170
74276	120
74278	120
74279	45
74283	65
74284	220
74285	180
74290	120
74293	75
74297	900
74298	100
74351	120
74365	60
74366	60
74367	60
74368	50
74376	90
74390	80
74393	120
74490	110

74C

C244	195
C245	195
C373	240
C374	245
C922	420
C923	500
C925	400

74LS

LS00	20
LS01	18
LS02	18
LS03	18
LS04	25
LS05	18
LS08	18
LS09	18
LS10	20
LS11	18
LS12	20
LS13	30
LS14	45
LS15	20
LS19	00
LS20	20
LS21	20
LS22	18
LS24	20
LS26	25
LS27	20
LS28	20
LS30	20
LS32	50
LS33	20
LS37	20
LS38	50
LS40	25
LS42	40
LS47	50
LS48	50
LS49	60
LS51	20
LS52	20
LS54	20
LS55	20
LS63	55
LS73	30
LS74	35
LS75	40
LS76	30
LS78	40
LS83	45
LS85	60
LS86	34
LS90	30

LS91	60
LS92	35
LS93	35
LS95	40
LS96	80
LS107	40
LS109	40
LS112	40
LS113	35
LS114	35
LS122	60
LS123	100
LS124	150
LS125	45
LS126	45
LS132	40
LS133	32
LS135	28
LS136	30
LS138	40
LS139	40
LS145	80
LS147	120
LS148	100
LS151	50
LS153	50
LS154	150
LS155	35
LS156	35
LS157	35
LS158	35
LS160	50
LS161	50
LS162	50
LS163	70
LS164	55
LS165	65
LS166	100
LS168	140
LS169	90
LS170	100
LS173	100
LS174	50
LS175	90
LS181	110
LS183	110
LS190	55
LS191	50
LS192	55
LS193	55
LS194	45
LS195	45
LS196	55
LS197	55
LS221	90
LS240	100
LS241	100
LS242	75
LS243	75
LS244	125
LS245	150
LS247	65
LS248	65
LS249	65
LS251	40
LS253	40
LS256	175
LS257	40
LS258	40
LS259	120
LS260	30
LS261	150
LS266	30
LS273	100
LS275	165
LS279	45
LS280	175
LS283	45
LS290	45
LS292	900
LS293	45
LS294	999
LS295	70
LS298	70
LS299	160
LS320	180
LS323	185
LS324	150
LS325	150
LS326	290

LS327	290
LS347	65
LS348	125
LS352	65
LS353	65
LS356	180
LS363	175
LS364	175
LS365	45
LS366	45
LS367	45
LS368	45
LS373	100
LS374	100
LS375	50
LS377	95
LS378	85
LS379	106
LS384	475
LS385	180
LS386	50
LS390	60
LS393	100
LS395	85
LS396	300
LS398	120
LS399	100
LS445	125
LS447	50
LS465	120
LS467	120
LS490	110
LS540	100
LS541	120
LS624	150
LS629	150
LS640	200
LS641	200
LS645	200
LS668	60
LS669	60
LS670	120
LS673	950
LS674	800
LS682	250

CMOS

4000	14
4001	16
4002	16
4006	50
4007	16
4008	40
4009	24
4010	26
4011	16
4012	18
4013	40
4014	46
4015	45
4016	29
4017	42
4018	45
4019	30
4020	50
4021	40
4022	67
4023	22
4024	37
4025	22
4026	95
4027	48
4028	45
4029	47
4030	35
4031	130
4032	80
4033	130
4034	140
4035	46
4036	275
4037	115
4038	110
4039	260
4040	42
4041	57
4042	40
4043	42
4044	42

4045	110
4046	60
4047	60
4048	55
4049	30
4050	30
4051	45
4052	60
4053	50
4054	85
4055	85
4056	85
4057	£10
4059	435
4060	58
4061	£5
4062	995
4063	85
4066	30
4067	245
4068	20
4069	22
4070	20
4071	22
4072	20
4073	22
4075	20
4076	55
4077	20
4078	20
4081	20
4082	20
4085	60
4086	60
4089	125
4093	37
4094	70
4095	95
4096	100
4097	275
4098	80
4099	75
4160	95
4161	99
4162	99
4163	99
4174	99
4175	105
4194	105
4408	850
4409	850
4410	725
4411	675
4412	790
4415	590
4419	280
4422	770
4433	770
4435	850
4440	999
4450	350
4490	450
4500	395
4501	28
4502	60
4503	40
4504	99
4505	385
4506	60
4507	32
4508	130
4510	46
4511	46
4512	45
4513	199
4514	115
4515	125
4516	65
4517	275
4518	53
4519	32
4520	53
4521	115
4522	125
4526	60
4527	85
4528	50
4529	150
4530	90
4531	130

4532	65
4534	400
4536	275
4538	80
4539	90
4541	95
4543	70
4544	150
4549	400
4553	245
4554	180
4555	35
4556	55
4557	250
4558	120
4559	395
4560	160
4561	104
4562	350
4566	165
4568	250
4569	175
4572	45
4580	255
4581	125
4582	99
4583	100
4584	48
4585	70
4599	165
40097	45
40098	42
40100	215
40101	130
40102	140
40103	412
40104	120
40105	220
40106	38
40107	38
40108	198
40109	100
40110	175
40114	240
40161	194
40163	50
40174	45
40175	50
40181	220
40192	75
40193	95
40194	90
40195	80
40244	195
40245	195
40257	198
40373	240
40374	245

JUST PHONE YOUR ORDER THROUGH, WE DO THE REST. 0923 50234

SPEAKERS

8Ω, 0·3W, 2"; 2·25", 2·5", 3"	80p
0·3W, 2·5" 40Ω; 64Ω or 80Ω	80p

DIODES

AA119	15
AA129	20
AAY30	15
BA100	15
BAX13	20
BY100	24
BY126	12
BY127	14
CRO33	250
OA9	40
OA47	12
OA70	12
OA79	15
OA81	20
OA85	15
OA90	8
OA91	8
OA95	8
OA200	8
OA202	8
1N914	4
1N916	5
1N4001/2	5
1N4003	6
1N4004/5	6
1N4006/7	7
1N4148	4
1N5401	15
1N5404	16
1N5406	17
1N5408	19
1S44	9
1S921	9
6A/100V	40
6A/400V	50
6A/800V	65

BRIDGE RECTIFIERS

(plastic case)

1A/50V	18
1A/100V	20
1A/400V	25
1A/600V	34
2A/50V	30
2A/200V	40
2A/400V	46
2A/600V	65
6A/100V	83
6A/600V	125
10A/200V	215
10A/600V	298
25A/200V	240
25A/600V	396
BY164	56
VM18	50

ZENERS

Range: 2V7 to 39V 400mW **8p each**

Range: 3V3 to 33V. 1·3W **15p each**

VARICAPS

MVAM2	165
BA102	30
BB105B	40
BB106	40

SCR's Thyristors

0·8A-100V	32
5A/300V	38
5A/400V	40
5A/600V	48
8A/300V	60
8A/600V	95
12A/100V	78
12A/400V	95
12A/800V	188
BT106	150
BT116	180
C106D	38
TIC44	24
TIC45	29
TIC47	35
2N5064	38
2N4444	130

TRIACS

3A/100V	48
3A/400V	56
3A/800V	85
8A/100V	60
8A/400V	69
8A/800V	115
12A/100V	78
12A/400V	82
12A/800V	135
16A/100V	103
16A/400V	105
16A/800V	220
25A/400V	185
25A/800V	295
25A/1000V	480
30A/400V	525
T2800D	120

SOLDERCON PINS

100	75p
500	370p

DIAC

ST2	25

OPTO

LEDS price includes Clips

TIL209 Red 3mm	10
TIL211 Green 3mm	14
TIL212 Yellow	14
TIL220 ·2" Red	12
0·2" Yel, Grn, Amber	14
Rectangular LEDs with two part clip. R, G & Y	45
Rectangl. Stackable LEDS	18
Triangular LEDs R&G	18
0·2" Flashing LED Red	56
0·2" Bi colour LEDs Red/Green	65
Green/Yellow	80
0·2" Tri colour LEDs Red/Green/Yellow	85
0·2" Red High Bright	59
High Bright Green or Yellow	65
LD271 Infra Red (emit)	46
TIL32 Infra Red (emit)	52
SFH205 (detector)	118
TIL78 (detector)	55
TIL38	50
TIL81 82; TIL100	90

7 Segment Displays

TIL321 ·5" C.An	120
TIL322 ·5" C.th	120
DL704 ·3" C.Cth	125
DL707 ·3" C.Anod	125
FND357 or 500	130
·3" Green C.A.	140
±1 ·3" Red or Green	150
Bargraph 10 seg. Red	250
Bargraph NSM3914	500

0·5" LIQUID CRYSTAL DISPLAYS

3½ digit	495
4 digit	530
6 digit	625

BPX25	250
BPW21	320
BPX65	320
IL74	65
ILD74	115
ILQ74	220
ILCT6 Darlington Isolator	135
TIL111	70
OCP71	120
ORP12	78
2N5777	50
4N33	135
Pin diode	720
Schmitt Receiver	715

OPTO SWITCH

Reflective TIL139	225
Slotted similar to RS	186

ALUM.BOXES

4×2½×2"	100
4×2½×2½"	103
4×4×2½"	120
5×4×2"	105
5×2½×1½"	90
5×2½×2½"	130
5×4×1½"	99
5×4×2½"	120
6×4×2"	120
6×4×3"	150
7×5×3"	180
8×6×3"	210
10×4½×3"	240
10×7×3"	275
12×5×3"	260
12×8×3"	295

FERRIC CHLORIDE

Crystals 1lb

195p + 50p p&p

DALO ETCH RESIST

Pen plus spare tip **100p**

COPPER CLAD BOARDS

Fibre Glass	Single-sided	Double-sided	SRBP 9·5"×8·5"
6"×6"	100p	125p	110p
6"×12"	175p	225p	

VEROBOARDS 0·1"

	Clad	Plain		
2½×3¾"	85-95	—	'VQ' Board	180
2½×5"	100-110	—	'DIP' Board	395
3¾×3¾"	100-110	—	Vero Strip	144
3¾×5"	115-125	95p	**PROTO-DECs**	
3¾×17"	390-420	275p	Veroblock	405
4¾×18"	495p	—	S-Dec	395
Pkt. of 100 pins		55p	Eurobreadboard	590
Spot Face Cutter		150p	Bimboard 1	695
Pin Insertion Tool		185p	Superstrip SS2	£13

VERO WIRING PEN and Spool **350p**
Spare Wire (Spool) **75p**; Combs **6p** ea.
Wire Wrapping Stakes 100 **250p**

VOLTAGE REGULATORS

1A T0220 Plastic Casing

	+ve		−ve	
5V	7805	40p	7905	45p
12V	7812	40p	7912	45p
15V	7815	40p	7915	45p
18V	7818	40p	7918	45p
24V	7824	40p		

100mA T092 Plastic Casing

5V	78L05	30p	79L05	50p
6V	78L62	30p	—	
8V	78L82	30p	—	
12V	78L12	30p	79L12	50p
15V	78L15	30p	79L15	50p

ICL7660	248	LM317K	250
78H05 5V/5A	550	LM317P	99
78H12 12V/5A	640	LM323K	500
78HG +5 to		LM337T	175
+24V 5A	599	LM723	30
79HG −2.25V to		TBA625B	75
−24V 5A	685	RC4194	375
LM309K	120	RC4195	160

SWITCHES

SLIDE 250V

1A DPDT	14
1A DPDT C/OFF	15
½A DP on/on/on	40

PUSH BUTTON
Spring loaded
Latching or Momentary 5A

SPDT c/over	110
DPDT c/over	160

MINIATURE
Non Locking

Push to make	15p
Push break	25p

TOGGLE 2A 250V

SPST	35
DPDT	48
4 pole on off	54

SUB-MIN TOGGLE 2 amp

SP changeover	60
SPST on off	54
SPDT c/off	85
SPDT Biased	105
DPDT 6 tags	75
DPDT C/OFF	88
DPDT on/on/on	185
DPDT Biased	145
3 pole c/over	205

ROTARY: (Adjustable Stop Type)
1 pole/2 to 12 way, 2p/2 to 6 way, 3 pole/2 to 4 way, 4 pole/2 to 3 way **48p**

ROTARY: Mains 250V AC, 4 Amp **64p**

DIP SWITCHES: (SPST) 4 way **65p**; 6 way **80p**; 8 way **87p**; 10 way **100p**; (SPDT) 4 way **190p**.

AMPHENOL PLUG

	IDC	Solder
24 way IEEE	475p	450p
36 way Centronics	525p	485p

ASTEC UHF MODULATORS

6MHz Standard	325p
8MHz Wideband	450p

Telephone orders by Access. Simply phone your order through 0923-50234 & we do the rest.

DIL SOCKETS

	Low profile	Wire wrap
8 pin	8p	25p
14 pin	10p	35p
16 pin	10p	42p
18 pin	16p	52p
20 pin	20p	60p
22 pin	22p	65p
24 pin	25p	70p
28 pin	28p	80p
40 pin	30p	99p

ZIF DIL SOCKET

24 way	565p
28 way	750p
40 way	799p

DIL PLUGS (Headers)

Pins	Solder	IDC
14	38p	95p
16	42p	100p
24	88p	138p
28	185p	290p
40	195p	218p

RIBBON CABLE

(price per foot)

Ways	Grey	Colour
10	15p	28p
16	25p	40p
20	30p	50p
26	40p	65p
34	60p	85p
40	70p	90p
64	100p	135p

'D' CONNECTORS:

Pins	9 way	15 way	25 way	37 way
MALE				
Solder	80p	110p	160p	240p
Angle	150p	210p	250p	355p
Strait	170p	160p	220p	310p
FEMALE				
Solder	105p	160p	200p	338p
Angle	165p	215p	290p	440p
Strait	175p	200p	300p	420p
COVERS	80p	75p	75p	90p

IDC 25 way Plg. 385p, Skt. 450p

SIL Sockets

0.1"
20 way **65p**
32 way **95p**

EDGE CONNECTORS

·1"

2×18 way	180p
2×22 way	199p
2×23 way	170p
2×25 way	225p
2×28 way	210p
2×30 way	245p
2×36 way	295p
2×40 way	315p
2×43 way	395p
2×75 way	550p

BEEBFONT ROM

This is a character FONT ROM that gives you 5 16×16 predefined FONT. The ROM is ideal for high quality demonstration on screen and when used in conjunction with EPSON printer, allows printing of letters etc. in mixed type faces. The package is complete, including an Editor to design your own Fonts and several spare Fonts which could not be fitted in the ROM can still be run from RAM. Supplied complete with ROM, software on DISC/tape and Manual. **Price £45**

IDC CONNECTORS (Speed block type)

2 rows	PCB Male with latch Strt. Pins	PCB Male with latch Angle Pins	Female Header Socket	Female Card-Edge Connector
10 way	90p	99p	85p	120p
16 way	130p	150p	110p	195p
20 way	145p	166p	125p	240p
26 way	175p	200p	150p	320p
34 way	205p	236p	169p	340p
40 way	220p	250p	190p	420p
50 way	235p	270p	200p	470p

EURO CONNECTORS

Gold flashed contacts	FEMALE SOCKETS Strt.	FEMALE SOCKETS Angle	MALE PLUGS Strt.	MALE PLUGS Angle
DIN 41612 2×32 way	275p	320p	220p	285p
DIN 41612 2-3×32 way	295p	340p	240p	300p
DIN 41612 3×32 way	360p	385p	260p	395p

TRANSFORMERS (mains Prim. 220-240V)

3-0-3V, 6-0-6V 100mA; 9-0-9V 75mA; 12-0-12V 75mA; 15-0-15V 75mA **98p**

6VA: 2x6V-5A; 2x9V-4A; 2x12V-0·3A; 2x15V-25A **250p**

12VA: 2x4V5-1·3A; 2x6V-1·2A; 2x12V-5A; 2x15V-4A **345p** (35p p&p)

24VA: 6V-1·5A 6V-1·5A; 9V-1·2A 9V-1·2A; 12V-1A 12V-1A; 15-8A 15-8A; 20V-6A 20V-6A **385p** (60p p&p)

50VA: 2×6V-4A; 2×9V-2·5A; 2×12V-2A; 2×15V-1·5A; 2×20V-1·2A; 2×25V-2A; 2×30V-0·8A **520p** (60p p&p)

100VA: 2×12V-4A; 2×15V-3A; 2×20V-2·5A; 2×30V-1·5A; 2×40V-1·25A; 2×50V-1A **965p** (60p p&p)

JUMPER LEADS Ribbon Cable Assembly

OIL Plug (Headers)
Single Ended Lead, 24" long

Length	14pin	16pin	24 pin	40 pin
24"	145p	165p	240p	325p
Double Ended Leads				
6"	185p	205p	300p	465p
12"	198p	215p	315p	490p
24"	210p	235p	345p	540p
36"	230p	250p	375p	595p

IDC FEMALE RECEPTACLE Jumper Leads 36"

	20pin	26pin	34pin	40pin
1 end	160p	200p	260p	300p
2 ends	290p	370p	480p	525p

COMPUTER CORNER

- **SEIKOSHA GP100A** – Unihammer Printer, normal & double width characters, dot resolution graphics 10" Tractor feed, parallel interface standard. **FREE 500 Sheets** **£155**
- **SEIKOSHA GP 250X** Printer **£199**
- **EPSON FX80 PRINTER** 160 CPS, 11×9 matrix, proportional spacing, superscript, subscript, dot addressable graphics, Normal, Italic & Elite characters. Up to 256 user definable characters. Down loadable character set. Condensed and double width printing. 4 user define margin positions. Tractor and Friction feed. 10" maximum width, Bi-directional, logic seeking. Centronix Interface standard. **£349**
- **EPSON RX80 PRINTER** **£235**
- **EPSON RX80 FT PRINTER** **£259**
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1·6MHz	395
1·8MHz	395
1·8432M	200
2·0MHz	225
2·4576M	200
2·5MHz	225
2·56250M	220
3·2768M	150
3·57954M	98
3·6864M	300
4·0MHz	150
4·032MHz	290
4·194304M	200
4·433619M	100
4·608MHz	200
4·80MHz	200
5·0MHz	160
5·185MHz	300
5·24288M	390
6·0MHz	140
6·144MHz	150
6·5536MHz	200
7·0MHz	150
7·168MHz	250
7·68MHz	200
8·0MHz	150
8·08333M	395
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9·00MHz	200
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10·0MHz	175
10·5MHz	250
10·7MHz	150
10·24MHz	200
12·0MHz	175
12·528MHz	300
14·31818M	170
14·7456M	175
14·765MHz	250
15·0MHz	200
16·0MHz	200
18·0MHz	180
18·432M	150
19·968MHz	150
20·0MHz	200
24·0MHz	170
24·930MHz	325
29·695MHz	150
26·670MHz	325
27·125MHz	295
27·145M	190
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4416-20	D2	6.60
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5516-25		7.73
6116-3	D1	3.72
6116-LP3	D2	4.67
2532-45	D2	3.50
2708-45	D2	3.25
2716-35	D1	4.50
2716-45	D1	3.50
2716-3	D1	4.50
2732-35	D1	4.58
2732-45	D1	3.75
2764-30	D1	3.92
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6810	D1	1.25
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6862		0.00
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6520	D1	2.67
6520A	D1	2.80
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6522A	D5	4.40
6532	D2	5.33
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LM319		2.23
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LM339N		0.37
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LM358N		0.28
LM393N		0.34
LM725CN		1.33
LM741CP		0.18
LM747CP		0.48
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MC1416	D1	0.66
MC1458CPL		0.26
MC1495L		7.13
MC1496P		0.65
MC1723P		0.32
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MC14412		11.87
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RO3-2513U	D1	7.82
SN75107BN		0.58
SN75110AN		0.68
SN75150P		0.72
SN75154N		0.87
SN75159N		1.19
SN75160AN		2.15
SN75161AN		2.35
SN75162AN		3.31
SN75172NG		1.64
SN75173N		1.21
SN75174		1.64
SN75175		1.21
SN75182		0.62
SN75183		0.62
SN75188		0.44
SN75189		0.44
SN75451BP		0.24
SN75452BP		0.24
SN75453BP		0.24
SN75454BP		0.24
SN75468N		1.08
SN75491AN		0.46
SN75492AN		0.61
TL010CP		0.38
TL061CLP		0.28
TL062CP		0.47
TL064CN		0.89
TL066CP		0.28
TL071CP		0.28
TL072CP		0.47
TL074CN		0.91
TL081CP		0.24
TL082CP		0.41
TL084CN		0.85
TL091CP		0.41
TL092CP		0.60
TL094CN		1.37
TL487CP		0.55
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20	0.17	0.41	1.23
22	0.17	0.48	1.31
24	0.20	0.63	1.44
28	0.23	0.57	1.59
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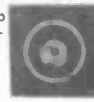

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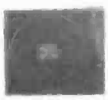

3 speed, auto, set-down; with auto return. Fitted with viscous damped cue, tubular aluminium counter-weighted arm, fitted with ceramic head. Ideally suited for home or disco use.
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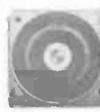

Manual single play record deck with auto return and cueing lever. Fitted with stereo ceramic cartridge 2 speeds with 45 rpm spindle adaptor ideally suited for home or disco. 13"x11" approx.
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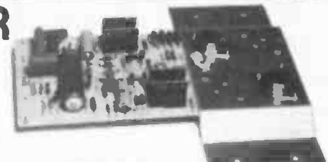
125W HIGH POWER AMP MODULES



The power amp kit is a module for high power applications - disco units, guitar amplifiers, public address systems and even high power domestic systems. The unit is protected against short circuiting of the load and is safe in an open circuit condition. A large safety margin exists by use of generously rated components, result, a high powered rugged unit. The PC board is back printed, etched and ready to drill for ease of construction and the aluminium chassis is preformed and ready to use. Supplied with all parts, circuit diagrams and instructions.

Accessories: Stereo mains power supply kit with trans. £10.50 + £2p&p. Mono: £7.50 + £2p&p.

SPECIFICATIONS:
Max. output power (RMS): 125 W. Operating voltage (DC): 50 - 80 max. Loads: 4 - 16 ohm. Frequency response measured @ 100 watts: 25Hz - 20KHz. Sensitivity for 100w: 400mV @ 47K. Typical T.H.D. @ 50 watts, 4 ohms: 0.1%. Dimensions: 205x90 and 190x36mm.

KIT **£10.50** +£1.15 p&p. BUILT **£14.25** +£1.15 p&p.

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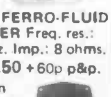
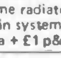
AUDAX 8" SPEAKER £5.95 + £2.20 p&p.



High quality 40 watts RMS bass/mid. Ideal for either HiFi or Disco use this speaker features an aluminium voice coil and a heavy 70mm dia. magnet. Freq. Res.: 20Hz to 7kHz. Imp.: 8 ohms.



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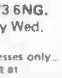

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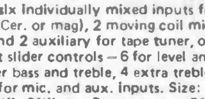
£45.00
+ £2 p&p.



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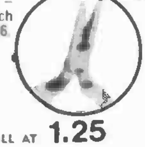

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Consumption	20mW
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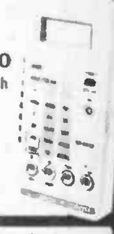

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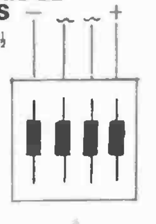

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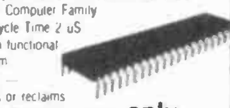

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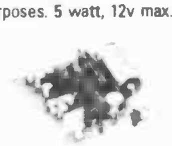

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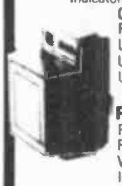

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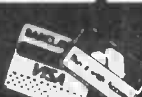

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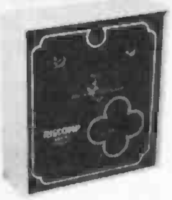

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DIGITAL ULTRASONIC DETECTOR US 5063

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- 3 levels of discrimination against false alarms
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- Built-in delays
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This advanced new module uses digital signal processing to provide the highest level of sensitivity whilst discriminating against potential false alarm conditions. The module has a built-in exit delay and timed alarm period, together with a selectable entrance delay, plus many more outstanding features.

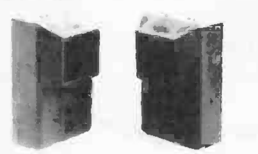
ULTRASONIC MODULE US 4012

£10.95 +V.A.T.

- Adjustable range from 5-25ft.

This popular low cost ultrasonic detector is already used in a wider range of applications from intruder detectors to automatic light switches and door opening equipment, featuring 2 LED indicators for ease of setting up.

INFRA-RED SYSTEM IR 1470 only £25.61 +V.A.T.



Consisting of separate transmitter and receiver both of which are housed in attractive moulded cases, the system provides an invisible modulated beam over distances of up to 50ft, operating a relay when the beam is broken. Intended for use in security systems, but also ideal for photographic and measurement applications. Size 80 by 50 by 35mm.

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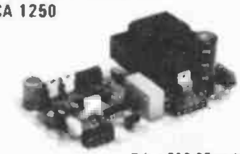
ALARM CONTROL UNIT CA 1250



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- Test loop facility

SIREN & POWER SUPPLY MODULE PSL 1865

only £9.95 + V.A.T.

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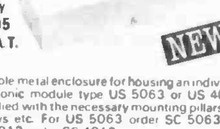

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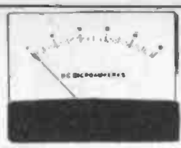

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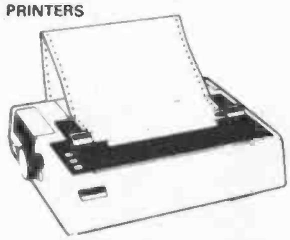

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Just look at the specification:-

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   6. The Text Editor.
   7. Assembler and Disassembler.
   8. System Hardware Configuration.
2. Experiment Manual. 16 experiments.
3. Monitor Program Source Listing with full commenting.
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PE

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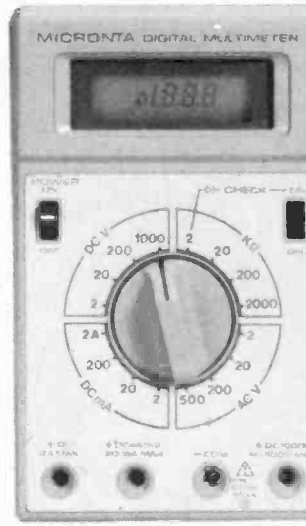

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PE VOLUME 20 No. 4 APRIL 1984

ELECTRONICS has really emerged from recession with a predicted growth for 1984 in every area of the market. Much can be blamed on the microprocessor which has made possible the integration of computers in automation, manufacture and communications. Fastest growth predicted, not surprisingly, is for memories, but the microprocessor is dragging along all the associated areas like p.s.u.s, lithium batteries, connectors, switches, displays—l.c.d. for hand held computers and c.r.t.s for v.d.u.s—and of course the passives, capacitors and resistors.

SMD

The humble resistor is about to lead (no pun intended) the march into SMDs (surface mounted devices) with a market which is expected to grow from $90m in 1983 to $140m in '84. The introduction of SMDs has already started in a big way, with the Japanese (who else?) setting the pace. The technology is concerned with cost saving by doing away with costly p.c.b. holes, the space they take and the simplification achieved when mounting on both sides of the p.c.b. or with multilayer boards. Fast, automatic "onsertion" (as opposed to insertion) and additional savings on connectors and mechanical hardware, as a result of smaller boards, also provide significant cost reductions. We will be publishing a feature on SMDs in the near future.

Of course a whole new area of industry has now come of age, again with thanks to the m.p.u. CAD/CAM or computer aided design and manufacture has taken off with a predicted growth for '84 of 30–40 per cent. CAE (computer aided engineering) has also taken on a significant role and it is predicted that this area will stay on 80 per cent growth rate for the next few years. Clearly the potential is vast.

HOBBY

What does all this mean to the hobbyist? It is obvious that components with leads will be around for a long time yet; although it is possible to hand mount SMD's, so even with them we will be able to continue our hobby.

Of course the microprocessor has had a significant impact on what the hobbyist can build and indeed on what he wants to build. Would we have needed a Logic Analyser or the Microstepper (see page 18) a few years ago? How many people would have wanted an EPROM Duplicator or a Computer Terminal in the 70's?

It is obvious that each time industry steps forward the benefits are quickly felt in the hobby area, usually long before they become obvious to the general consumer. We can however see one disadvantage in this fast growth—component shortages and the resulting price increases.

Three years ago I wrote the following:

> "Unfortunately the present buying spree by industry is creating component supply problems and once again we suspect the hobbyist is beginning to suffer. Delivery dates are lengthening and sometimes being broken by manufacturers, so have some sympathy with your component retailer if he is out of stock and says it could be a month or two before a certain device is again available—very often he can only pass on information from the manufacturer and that information has sometimes proved to be unreliable."

We anticipate that this situation may return towards the end of '84 so it may not be a bad time to stock up with a few components!

Mike Kenward

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Components and p.c.b.s are usually available from advertisers; where we anticipate difficulties a source will be suggested.

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Items mentioned are available through normal retail outlets, unless otherwise specified. Prices correct at time of going to press.

...NEWS &

DRAGON MEMORY UP 32K

Following in the steps of the Dragon 32 home computer is their latest model, the Dragon 64K which utilises the 6809E microprocessor. Compared to the 8055 and 6502 processors used by many of Dragon's competitors, the 6809 contains several 16-bit registers to allow for flexible address mode capabilities, making high level language implementation more practical. BASIC, PASCAL and COBOL can all be used in conjunction with the Dragon 64.

The new model was launched late last year along with their disk based OS-9 operating system designed specifically for the Dragon 64, which will give the user a wide range of possible business applications.

The OS-9 system is seen by Dragon Data as the user's passport to professional software, which will include packages for stock control, invoicing, accounting, payroll and even spreadsheet analysis.

The Dragon 32 has proved to be a successful machine and has placed Dragon Data high in the home computer market. The introduction of the powerful Dragon 64, the OS-9 operating system and the recent introduction of their disk drives gives them the means to enter other markets, where they are confident and expect to achieve equal success.

The Dragon 64 offers three different operating modes. The '32' mode allows the user to operate the machine as a Dragon 32. The '48K Mode' gives 48K RAM and 16K Basic Interpreter and the '64K Mode' enables full use of the 64K RAM.

It is important to note that all the features on the Dragon 64 are in addition to, and not at the expense of, those offered on the Dragon 32. The high resolution display of 256 x 192 pixels is retained and all the currently available software for the 32, both in plug-in cartridge and cassette form, is compatible with the 64.

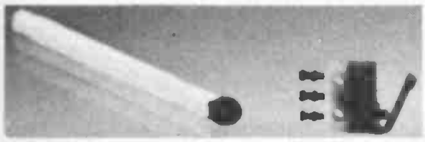
In addition the recently launched Dragon Disk Drives will run on both the 32 and 64.

The Dragon 64 costs £225 and will be available through the usual Dragon dealerships, including both Boots and Dixons.

Match That

An ultra-miniature 50-volt microswitch with actuator arm has been announced by Semiconductor Supplies International. This 300mA single pole changeover switch weighs 0·3 grams. Dimensions are height (inclusive of pins and with lever compressed) 10mm, width 8mm, thickness 3mm. The actuating lever of this switch is shaped for cam-follower applications as well as for ordinary compression applications.

Uses include the tamper proofing or safety switching of small equipment including security equipment such as sensors or for switching models etc. Price per pack of 10 is £4.00 inc p & p. Semiconductor Supplies, Sutton, Surrey SM1 4RS (01-643 1126).



DE-SOLDERER

A new electric desoldering iron from OK Industries combines the virtues of a hand-held, manual unit with the performance of an industrial desolder station. The lightweight SA-6 features 'one-hand' desoldering and eliminates the need for two tools, combining heat and suction in one.

The vacuum chamber is easily removed for cleaning, and replacement tips are available with 1·5mm and 1·77mm hole diameters. 115 or 230V a.c. 50/60Hz versions are offered; the 230V type costs £18 all inc.

OK Industries UK Ltd, Dutton Lane, Eastleigh, Hants SO5 4AA (0703 619841).

OXYGEN IONS

A £1.2m ion blasting machine, to be built at the Atomic Energy Authority's Harwell research laboratories, could give Britain a world lead in an area of advanced chip production.

To be completed by next year, the machine will be capable of creating a circuit *beneath* the surface of a slice of silicon.

What happens is this: The silicon is bombarded with high energy oxygen ions at a minimum of 10^{17} ions/sq. cm. Because of their high energy, these ions rip through the surface of the silicon and come to rest at about one micron deep, where they form a subsurface layer of silicon dioxide. The technique is currently known as ion implantation, and is used to introduce dopants, such as boron and arsenic. But with ten times the ion current, Harwell's machine will be able to create a "buried dielectric" because the absorbed oxygen ions form an insulating layer which can be patterned so as to create circuit elements. It is necessary to maintain the silicon at a temperature of 500 deg. C in order to create a self-healing effect where the ions tear through the silicon's surface.

Mechamorphosis

A simple yet innovative joystick has been developed by E.E.C. Ltd. It is designed for use with the ZX Spectrum and is purely a mechanical device.

The joystick clips onto the machine and directly depresses the relevant keys without obstructing any other command keys, neither will it interfere with any of the Spectrum peripherals. This UK patented invention was launched late last year and is already being exported to many European countries. Although High Street availability is planned by the company the device is only presently available on a mail order basis.

Perhaps the most appealing feature of this unit is its price, £9.95 plus 55p p&p. Details from, E.E.C. Ltd, 1 Whitehouse Close, Chalfont St Peter, Bucks SL9 ODA (0753 885401).

MARKET PLACE

Briefly...

Whilst the Home Office's position is that the protection afforded UK laboratory animals represents a satisfactory balance between the need to experiment on living creatures and public revulsion at their suffering, it does point out that the 1876 Cruelty to Animals Act is to be reviewed when Parliamentary time permits.

Meanwhile, the rodents and monkeys behind bars may diminish in numbers thanks to computer models of their body chemistry. Computers that can simulate the cardiovascular and respiratory systems, and graphically illustrate changes therein, will increasingly be substituted as research aids.

• • • •

Available from Verospeed, is a unique non-volatile RAM that can retain its data for ten years without a power supply.

Manufactured by Mostek, the MK48ZO2 incorporates 16K (2K × 8 bits) of static RAM and two moulded-in lithium batteries, all in a standard 24-pin d.i.l. package. The device operates from 5V at 385mW (10mW standby), at a speed of 250ns.

• • • •

Sir Keith Joseph's proposed changes in the school curriculum should improve skills in school-leavers, better fitting them for immediate employment. Surprisingly, for Sir Keith has many critics, there was general agreement from all sectors of education that this was a good thing. The young are also getting the message as is shown by the sharp increase in demand for Polytechnic places in science, mathematics, engineering and technology.

Silicon News Corner

Burr-Brown ▶ MPY100 is a low cost, precision multiplier/divider. Four quadrant multiplication, square root, r.m.s. to d.c., linearisation and algebraic computation often without need of amps or potentiometers.
▶ JFET op amp, called OPA 100, has initial bias current of 0·5pA @ room temp., and only 35pA at 125°C!
Burr-Brown, Cassiobury House, Station Rd., Watford WD1 1EA.

National Semiconductor ▶ New series of 16 large 0·43 in. 7-seg. l.e.d. display. Red, yellow and green are 5082-760, 5082-7660 & 5082-7670 respectively.
National Semiconductor, 301 Harpur Centre, Horne Lane, Bedford.

TRW LSI ▶ Launches 3 member family of economical Flash ADCs. TDC 1029 offers 6-bits at 100 MSPS at bandwidth of 50MHz. Places video speed A/D within reach of more applications.
MCP Electronics, 38 Rosemont Rd., Alperton, Wembley, Mddsx HA0 4PE.

Plessey ▶ New range of CCDs. MS 1002-1/3 is 850 bit register. MS 1003-1/3 is 910 bit register. Both have video bandwidth above 5MHz and clock frequency of 13·3MHz.
▶ High speed ECL 10-bit synchronous up-/down counter is SP9215. Clock to 50MHz.
Information: Charles Baker Lyons, 30 Farringdon St., London EC4A 4EA.

IR ▶ Two new ranges to power MOSFETs (HEXFETs). Range 1: 30 parts in TO39 package in N & P channel, eight different voltages. Range 2: Extension to d.i.l. MOSFETs. 4-pin device is "stackable" to make arrays of N or P channel switches. Rated 200V.
International Rectifier, Hurst Green, Oxted, Surrey RH8 9BB.

TI ▶ First two in series of CMOS 8-bit, single-chip microcomputers add to TMS7000 family. NMOS capability with CMOS power advantage. TMS70C00 and TMS70C20.
Texas Instruments, Manton Lane, Bedford MK41 7PA.

POINTS ARISING...

COMPUTER TERMINAL
February '84
The CRT controller chip SFF96364 (manufactured by Thomson CSF) will continue its existence under a new part number, and although it may be seen in catalogues as 96364E (E for plastic) for some time to come, as far as the maker is concerned it is now known as the EF9364, with suffix P for plastic and C for ceramic. The device is available from *Technomatic Ltd.*, and *Watford Electronics.*

• • •

CLOCK TIMER
February '84
The value of C2 should be 15nF not 150nF.

Countdown...

Please check dates before setting out, as we cannot *guarantee* the accuracy of the information presented below. Note: some exhibitions may be trade only. If you are organising any electrical/electronics, radio or scientific event, big or small, we shall be glad to include it here. Address details to Mike Abbott.

Computer Trade Show March 13–15. Wemb. Conf. Cntr. **Z1**
Business Telecom March 13–15. Barbican Cntr., London. **O**
Visit to Firefly Electric Vehicles (Milton Keynes). March 17. **R1**
Electro-Optics/Laser Int. March 20–22. Metropole, Brighton. **T1**
Information Technology (Conf. & Ex.) March 20–22. London. ✆ 01-828 2333
Nortest March 20–22. Spectrum Centre, Birchwood, Warrington. **T**
Sensors & Systems (concurrent with Nortest)
Scottish Computer Show March '84. Holiday Inn, Glasgow. **T1**
Tectronica April 16–18. Earls Court, London. **T**
London Computer Fair 19th, 21st & 23rd April. **J3**
Fibre Optics May 1–3. Porter Tun Room, Whitbread Brewery. **E**
All Electronics/ECIF May 1–3. Barbican, London. **E**
Biotech Europe May 15–17. Wembley Conf. Cntr., London. **O**
Micro City May 15–17. Exhibition Complex, Bristol. **F3**
Scotelex June 5–7. Royal Highland Exhibition Halls, Ingliston, Edinburgh. **O5**
IBM System User Show June 12–14. Wembley Conf. Cntr., London. **O**
Qualex June 19–21. Corn Exchange, Brighton. **D4**
Surface Treatment & Finishing Show June 25–29. Birmingham. **M**
Networks July 3–5. Wembley Conf. Cntr., London. **O**
Cable July 10–12. Wembley Conf. Cntr., London. **O**
Testmex Sept. 11–13. Grosvenor Ho. Pk. Lane, London. **E**
Building & Home Improvement Sept. 25–30. Earls Court, London. **M**
Computer Graphics Oct. 9–11. Wemb. Conf. Cntr., London. **O**
Software Expo Oct. 16–18. Wemb. Conf. Cntr., London. **O**
Computers In The City Nov. 20–22. Barbican, London. **O**
Data Security Nov. 20–22. Barbican, London. **O**

D4	Network ✆ 0280 815226
E	Evan Steadman ✆ 0799 26699
F3	Tomorrow's World ✆ 0272 292156
J3	Computer Market Place ✆ 01-930 1612
M	Montbuild ✆ 01-486 1951
O	Online ✆ 01-868 4466
O5	Institute of Electronics ✆ 0706 43661
R1	Battery Vehicle Association. ✆ Brian Hampton, 0908 316991
T	Trident ✆ 0822 4671
T1	Cahners ✆ 0483 38085
Z1	IPC ✆ 01-643 8040

STEP & FREEZE INSTRUCTIONS with the MICROSTEPPER

L. G. PARKIN BA

THE Microstepper described here is a "clip-on" device which allows you to follow the operation of a microprocessor system. Unlike other electronic systems, the operation of a microprocessor system cannot be seen with standard test equipment such as the C.R.O. and multimeter etc. The address bus and data bus lines transfer large amounts of data at high speed—typically 24 bits of data one million times per second.

To understand or debug such a system, a detailed analysis is required of all this, slowed down to "human" speed, and presented on some form of visual display.

The professional answer is to use a logic analyser. This is a very versatile instrument, which can store, and then display, a sequence of binary states of bus and control lines in any logic system. Logic analysers are expensive, and considerable expertise is required in setting up the instrument, and interpreting results.

The Microstepper device is dedicated to microprocessor systems. In use, it is attached to the system under test, and puts it into "single step" mode. In this mode, each individual step of a program can be followed. Data can be "seen" going to or from memory, I/O ports etc.

Quite apart from the obvious hardware and software debugging uses, a fascinating method of self teaching is provided. To see a program executed by the hardware before your eyes is the surest way to understand both hardware and software.

OPERATION

There are only three controls:

S1—A push button labelled "GO" which, when pressed, runs the system to the next step.

S2—A three position switch, labelled "RUN", "STEP", and "BREAK". These functions are explained later.

S3–10 and S11–18—a total of 16 "in-line" switches, for setting up a binary address "break point".

Data display is by six 7-segment l.e.d.s, four for the address bus, and two for the data bus. Connections to the Microstepper are shown for a Z80, but the device is adaptable to other microprocessors. A 40 pin test clip is used to attach the Microstepper to the microprocessor chip in the system under test. In the illustrations, this is shown wired directly to the circuit board.

If, however, operation with more than one type of microprocessor is envisaged, the Microstepper connections to the 40 pin test clip should be made via a 30 pin plug/socket on the Microstepper board. Each different type of microprocessor can then have a separate test connector, wired appropriately for that chip.

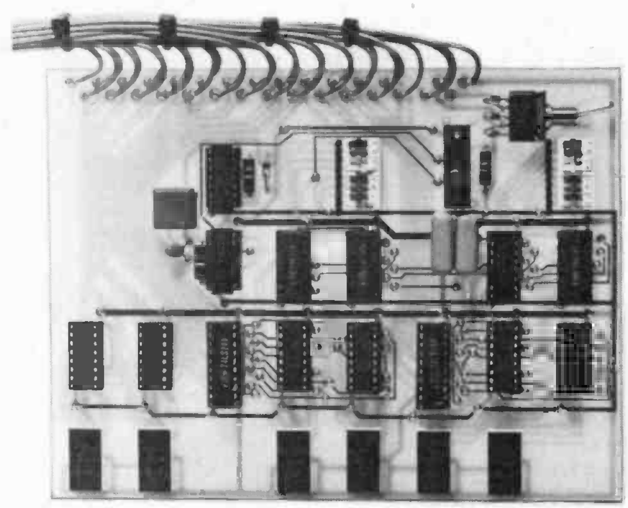
Power supply may be taken from the system under test, or from an external supply, the choice being made by S19. Power supply requirements are 5V at 600 mA.

To use the device, attach the test clip to the microprocessor, before applying power. Switch S2 to "STEP". Apply power, and press "GO" to reset the Microstepper. Reset the system being tested.

SINGLE STEP MODE

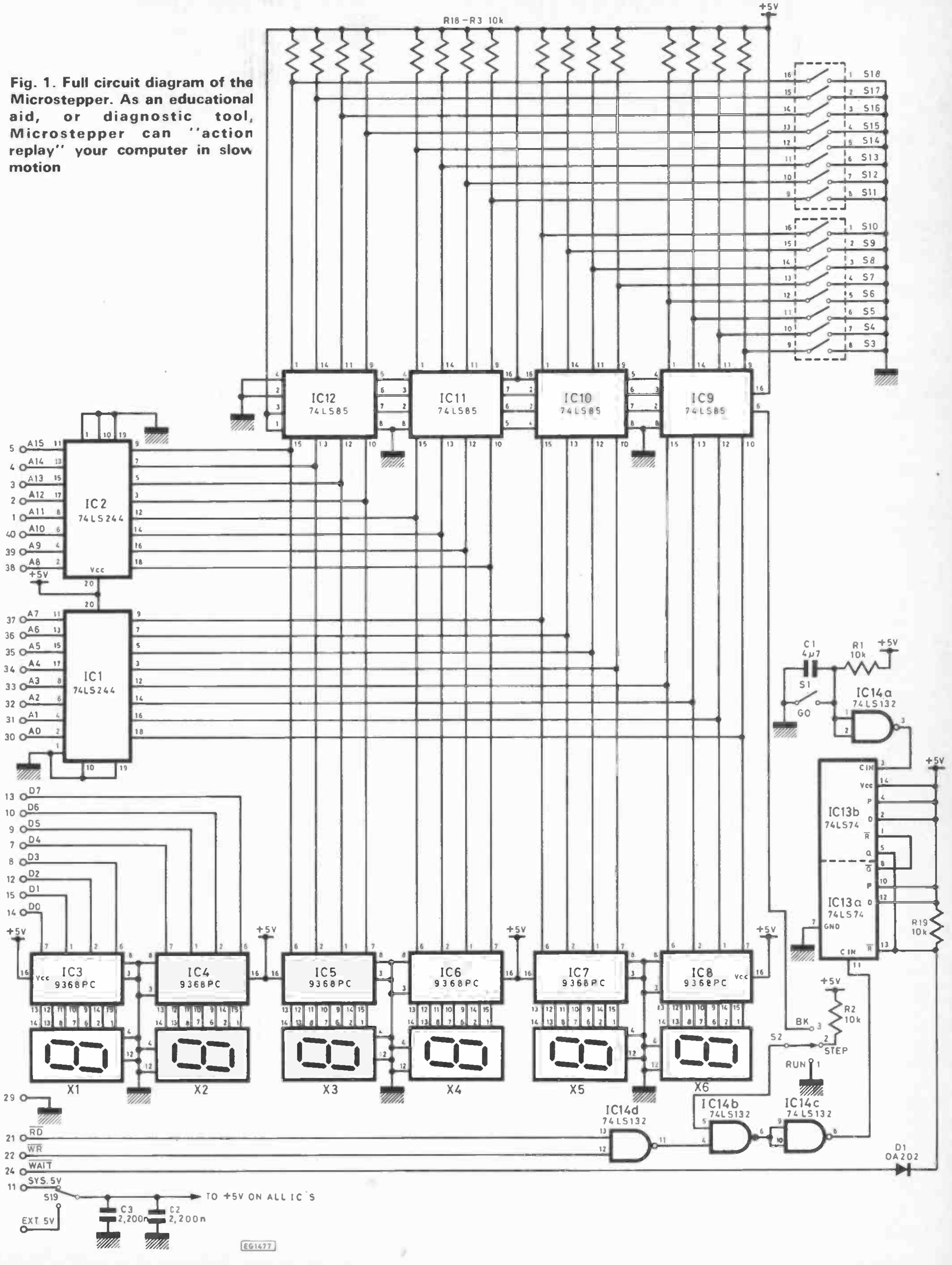
The first address (0000 Hex in the case of the Z80) will appear on the address display, and the contents of that memory address will appear on the data display, both in hexadecimal form.

Step through the program by pressing "GO". Each time "GO" is pressed, the next "read" or "write" operation will be displayed. Compare the observed results with the program at each step. Any software bugs will be evident because the system does exactly what the program tells it to do, which may not be what the programer intended! Hardware faults are evident when the program is correct, but the system responds incorrectly—perhaps with unexpected address or data displays. Frequent causes of this type of fault are bus lines open circuit, earthed, or interconnected, producing strange symptoms.



This is the printed circuit version of Microstepper. Sheer speed in a computer creates the illusion of intelligence, but the illusion can be removed to allow measurements and readings to be taken step by step

Fig. 1. Full circuit diagram of the Microstepper. As an educational aid, or diagnostic tool, Microstepper can "action replay" your computer in slow motion



An example will show how to deal with this type of fault. Suppose part of a program reads:

Address	*Code*	*Mnemonic*
0010	3E 34	LD. A 34
0012	32 12 10	LD. (3012). A

In a good system, stepping through from address 0010 should show on the displays—

Address	*Data*	*Operation*
0010	3E	Opcode fetch
0011	34	Second byte
0012	32	Opcode fetch
0013	12	Low byte address
0014	10	High byte address
1012	34	Write from Accumulator to memory location 1012

Note that we see not only code held in ROM, but also data being written to RAM. Now, suppose a faulty system gives these displays—

Address	*Data*	*Operation*
0010	3E	Opcode fetch
0011	34	Second byte
0012	32	Opcode fetch
0013	12	Low byte of address
0010	3E	High byte of address
3E12	34	Write from Accumulator to memory location 3E12 (?)

The last step shows the processor attempting to write data into a strange address—3E12 Hex. This is because, in the previous step, the high byte of the address was read from RCM location 0010 instead of 0014. If we reset the system, and go to the 5th. step, where things appeared to go awry, a simple voltage check on bit 3 of the address bus shows zero volts (logic 0) instead of logic 1, possibly caused by an earth.

That caused binary address 0000 0000 0001 0100
= 0014 Hex
to become 0000 0000 0001 0000
= 0010 Hex

This example illustrates another point , which is, hold the process at any point, and you can check for correct logic levels, under static conditions, with a simple multimeter.

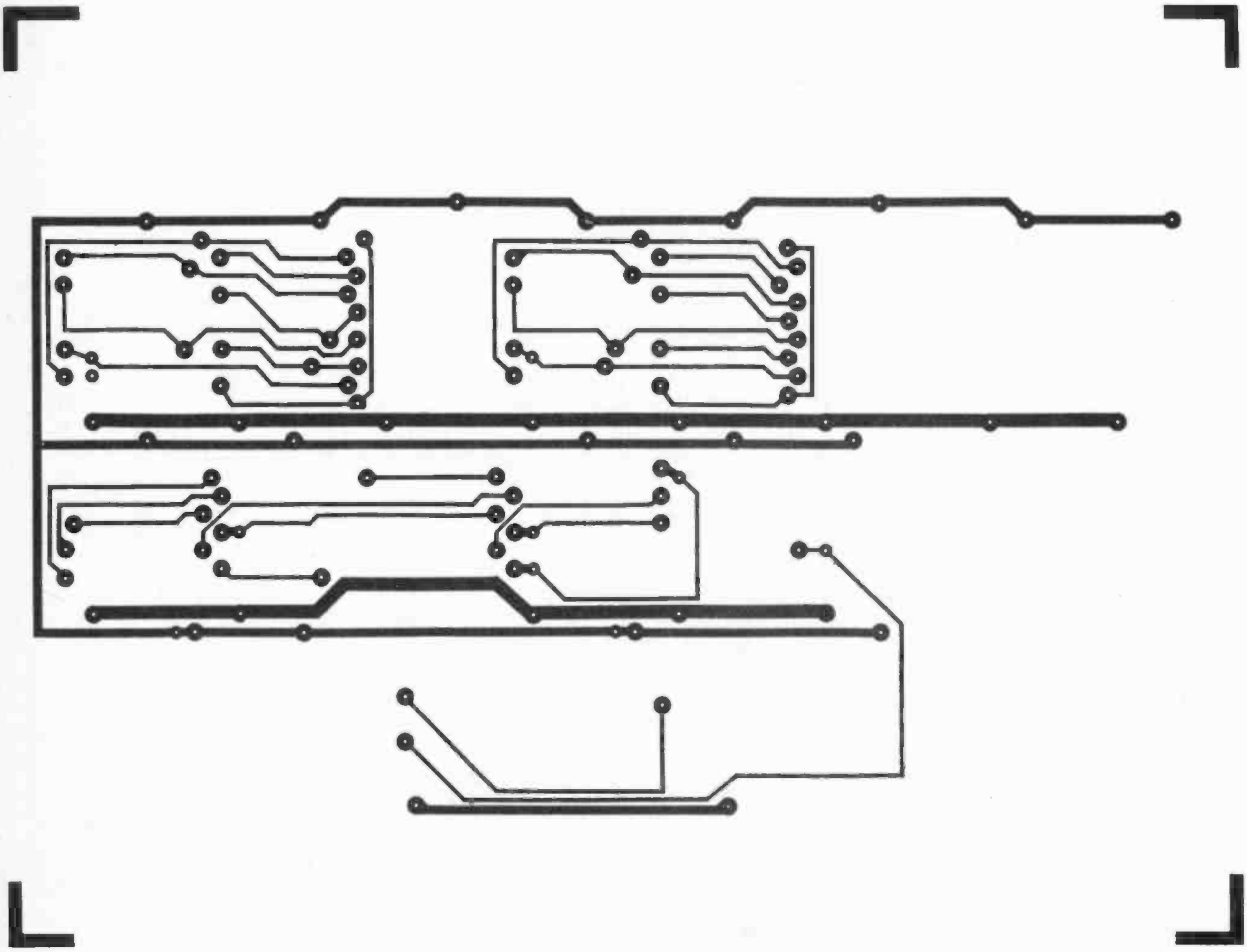


Fig. 2. Printed circuit board layout of the Microstepper. This is the "copper-side" view at full size

BREAK POINT OPERATION

Pressing "GO" to get to a particular part of a program can be tedious. Imagine going round a counting loop 10,000 times! To go to a particular address quickly, set S2 to "BREAK", and set up the desired address as a binary pattern on S3–18. Reset the processor, and press "GO". The system will run normally until the required address is reached, when the Microstepper holds the processor, displaying address and data as before. Now switch to "STEP", and step through the program from there. Alternatively, set S3–18 to a new address, press "GO", and the program will run up to the new address.

RUN MODE

With S2 in the "RUN" position, press "GO", and normal program execution will result.

DYNAMIC RAM

Note that where any dynamic RAM in the system is refreshed by the microprocessor, as in the Z80, refresh will not take place whilst the processor is halted by the Microstepper. In this case, ROM and program operation can still be observed, using "break" operation to skip over all data storage operations up to an area of interest in the program.

CIRCUIT DESCRIPTION

Consider first S2 at "STEP". Pressing "GO" takes IC14 pins 1, 2 low, making IC14 pin 3 high. IC13 is an edge triggered data bistable, so it is "set" by the rising voltage on IC13 pin 3. The resulting "high" on IC13 pin 5 is connected to the microprocessor "$\overline{\text{WAIT}}$" line, so the processor is free to run normally. After reset of the processor, the first address (0000 Hex in the case of the Z80) appears on bits 0 to 15 of the address bus, and the processor signals a READ operation, by pulling $\overline{\text{RD}}$ low. IC14 pin 11 goes high, IC14 pin 5 is high due to S2, so IC14 pin 6 is low, and IC14 pin 8 goes high to set IC13b. IC13b pin 5, now low, resets IC13a, and pulls the $\overline{\text{WAIT}}$ line low, stopping the processor.

In this state, the 16 bits of the address bus are buffered by IC1, IC2, to drive the comparators IC9, IC10, IC11, IC12, and decoders IC5, IC6, IC7, IC8. Each decoder takes one 4-bit "nibble" to produce a hexadecimal readout on the 7-segment displays X3 to X6.

Meanwhile, the memory in the system under test responds by placing data on the data bus, which is decoded by IC3, IC4, and displayed on X1 and X2.

This condition holds until the "GO" button is pressed, taking IC14 pins 1, 2 low, IC14 pin 3 high, thus setting IC13b. IC13b pin 5, now high, removes the reset from IC13a, and places a "high" on the $\overline{\text{WAIT}}$ line. The processor now runs to

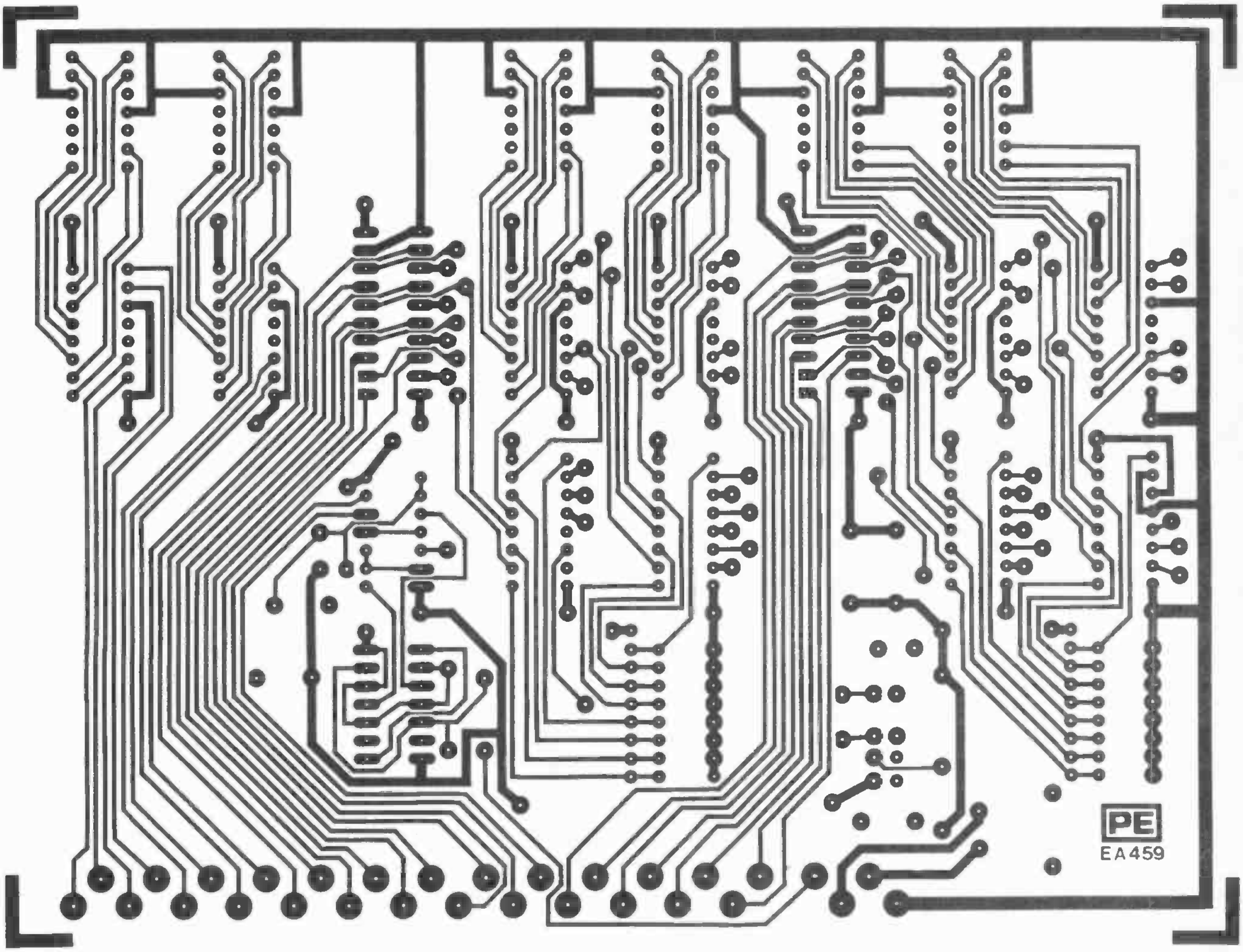


Fig. 3. P.c.b. layout of "component-side" (actual size)

COMPONENTS . . .

Resistors

R1, 2, 19	10k (3 off)
R3–10, R11–18	8 x 10k s.i.l. (2 off)

Capacitors

C1	4μ7 tant.
C2, C3	220n poly (2 off)

Integrated Circuits

IC1, IC2	74LS244 (2 off)
IC3–8	9368PC (6 off)
IC9–12	74LS85 (4 off)
IC13	74LS74
IC14	74LS132

Displays

X1–6	DL704 comm. cath. (6 off)

Diodes

D1	OA202

Switches

S1	Keyboard push-button (p.c.b. mounting)
S2	2P3W slide switch (only one pole used)
S3–10, S11–18	8-way d.i.l. switch (2 off)
S19	1P2W toggle switch

I.c. sockets

20-pin	2 off
16-pin	10 off
14-pin	2 off

Sockets for the d.i.l. switches and displays may also be desired

Miscellaneous

Printed circuit board
40-pin test clip (RS 424 153)
Ribbon cable for above
Supply leads (for power supply)
Eyelets, or pins for "through board" connections
Solder pins for wire terminations

Constructor's Note

If the test clip can only be found in the RS Components catalogue, it may interest non-trade readers to know that components can be obtained from RS indirectly, via **Ace Mailtronix,** 3a Commercial St., Batley, West Yorkshire.

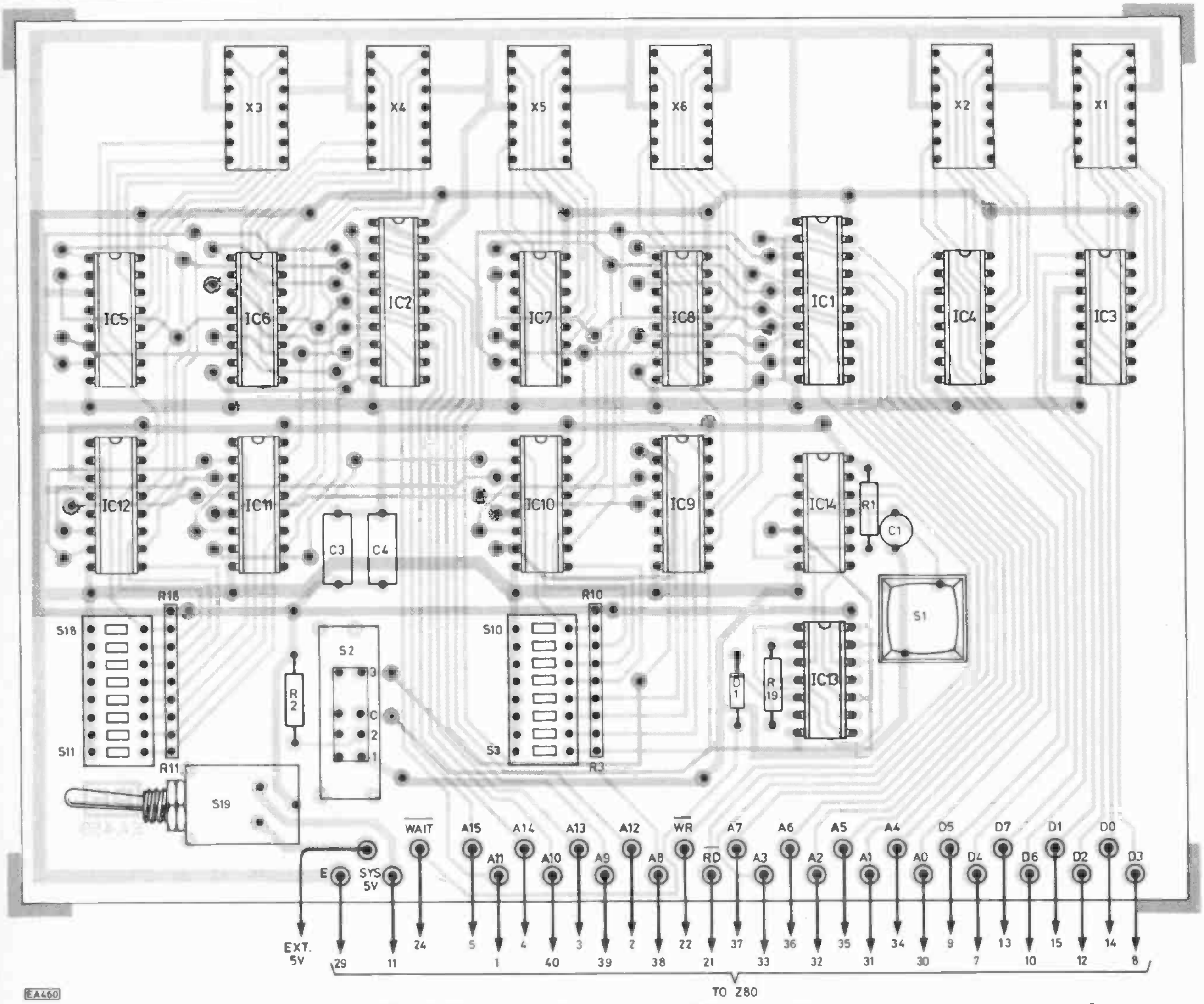


Fig. 4. Component layout of the Microstepper

Cont. page 25

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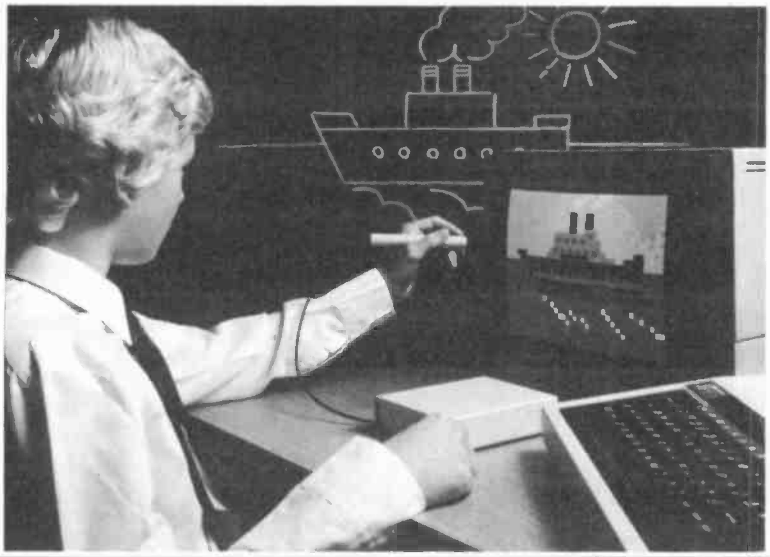
GOODIES FOR THE BBC MICROCOMPUTER



RH Lightpen

The RH lightpen is compact, little bigger than a felt-tip. It is versatile, with a sophisticated microswitch at its point which responds to the slightest pressure, and an LED lamp at the user's end to indicate data transmission. Both microswitch and LED are fully programmable.
The RH lightpen is reliable, with a rugged metal case to provide physical and electronic protection. Its sensitivity can be adjusted to the thickness and type of your TV screen, giving the highest levels of accuracy.
With the lightpen connected to your BBC Micro you can draw lines on the screen, or give commands simply by pointing to a menu.

Colour-Graphic software

This additional software is available so that all the colours of the BBC Micro's palette are available at the tip of your pen. Complex graphics can be created in minutes.

Art-Fun software

This program is guaranteed to bring out the artist in you. It provides inspiration for users of the lightpen and provides full interaction between pen and screen.
Lightpen **£45.95** — 40 track disc version of lightpen software **£5.95** — Colour-graphic software (tape) **£9.95** — Art-fun software (tape) **£9.95**

RH Software

RH Electronics has a whole series of excellent software for the BBC Microcomputer Model B. For games, business and education, they will be highly valued by any BBC Micro owner.

Plegaron People Eaters £8.95
Stop the Plegaron's path of destruction by walling them in. A game of skill (9 levels) and cunning.

Galactic Wipeout £8.95
Fight off alien attackers and meteor showers as you transport the survivors of the human race to a new planet.

Ski Slalom £8.95
Guide the skier through the 40 gate course avoiding deadly ice and landsliding snowballs.

Viper £8.95
Guide the snake around its electric cage devouring as much food as you can. Avoid touching the electrified walls, swallowing unsavoury food or causing the snake to eat its own tail.

3 In 1 (A) £7.50
This set of three games for the younger enthusiast includes: Task Force — a strategic battle of sea and air; Demolish — blast your way to freedom avoiding radioactive fall-out and falling masonry as you go; Cosmos — where you have to defend the earth from an invading battle fleet.

Ed-master £12.95
This program uses the quiz format, combining the element of fun with educational teaching. 160 questions may be programmed by the teacher, divided into eight subject areas of 20 questions each. Questions and answers can be changed as often as you wish. The computer will tell the pupil whether he or she has the correct answer or not, but cheating is prevented as pupils cannot access the program to find out the correct answers. The scores of up to 40 pupils are stored in the quiz memory and easily recalled for comparison.

Snail Trail £4.95
Help the snail escape from the maze he's fallen into before he starves to death. There are two skill levels to this cassette.

Database £12.95
A cassette for the business of home. It enables you to file, sort and access a great number of items such as diary entries, addresses, telephone numbers, accounts or other information.

AT LAST!! A worthwhile peripheral

"These computers are all very well but they can't REALLY do anything can they?"

R.H.ELECTRONICS (SALES) LTD.
Exclusive Distributors of DCP Microdevelopment products

How many times have you heard that sentence and realised that you are inclined to agree? That's all in the past with these long awaited exciting new products from DCP.

For the BBC Microcomputer:

INTERBEEB

The self-powered INTERBEEB is a rugged new peripheral, housed in a neat thermo-plastic case the INTERBEEB contains the following hardware to allow your computer to control the outside world . . . and get an answer WITHOUT having to re-invent the wheel!
1) an 8 bit, 8 channel Analogue to Digital convertor (ADC). 2) 4 high current relay outputs. 3) an 8 bit input port and a SEPARATE 8 bit output port. 4) 4 switch inputs. 5) DCP bus connection allows communication with other units in the DCP range.
The unit comes complete with all the necessary cables, a mains power unit and a manual giving examples for beginners, all for **£59.95** + postage and packing.

For the ZX Spectrum or ZX81:

INTERSPEC

The INTERSPEC gives users of Sinclair computers the same facilities for control and interrogation of the outside world as the INTERBEEB and with the advantage of the DCP bus connector, which presents all the necessary bus connections and power lines to the user, upto 4 further packs may be added allowing (for instance) proportional control of analogue driven equipment.
The INTERSPEC comes complete with a comprehensive manual including examples of use and hints for ZX81 users. Control of your environment can be yours for only **£39.95** + post and packing.

DAC PACK

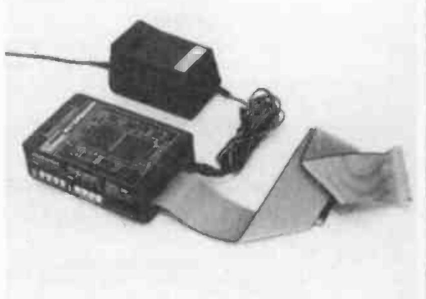
The DAC PACK (Digital to Analogue Convertor) will give your computer, for the first time, the capability to communicate with the outside world in its own language. The DAC PACK features a 2.55 volt internal reference voltage for rock-steady output and a step resolution of 10mV in 255 levels and high quality connectors for reliable operation. The DAC PACK connects to the DCP bus and therefore requires that either the INTERSPEC or INTERBEEB be present.
As with all other DCP products the DAC PACK comes complete with a comprehensive manual and costs **£19.95** + post & packing.

AD PACK

The AD PACK (Analogue to Digital Convertor) is easy to both use and understand and consists of a fast A to D convertor with an internal precision voltage reference source for accurate conversions. The input voltage swing is 0 to 2.55V with a tolerance allowable of ±5%, therefore giving a 10mV input resolution. The AD PACK is connected using the DCP bus and will therefore require either the INTERSPEC or INTERBEEB to be connected to the host computer.
The AD PACK comes with a manual which includes examples of operation and costs **£19.95** + postage & packing.

S-PACK

The Speech Pack is a completely self-contained add-on speech synthesiser for the ZX81 or Spectrum Computers which may be used in addition to a ZX RAM PACK, DCP PACK and/or ZX printer. The S-PACK is supplied complete with Word Pack ROM 1 which contains all the letters of the alphabet, numbers 0 to over a million and some other general words which can all be 'spoken' under computer control. Up to three more Word Pack Rom's can be fitted to expand the vocabulary, details of which are available on request. The 2 versions of the speech pack for the ZX81 and Spectrum operate in similar manners but are NOT interchangeable, therefore the type of host computer should be specified when ordering.
The S-PACK comes complete with an operating manual and is available for **£59.95** plus postage & packing.
Word Packs 2, 3 and 4 are **£14.95** + postage & packing.
Dealer and Quantity enquiries welcome. For further information regarding the above range please contact **RH Electronics (Sales) Ltd.**

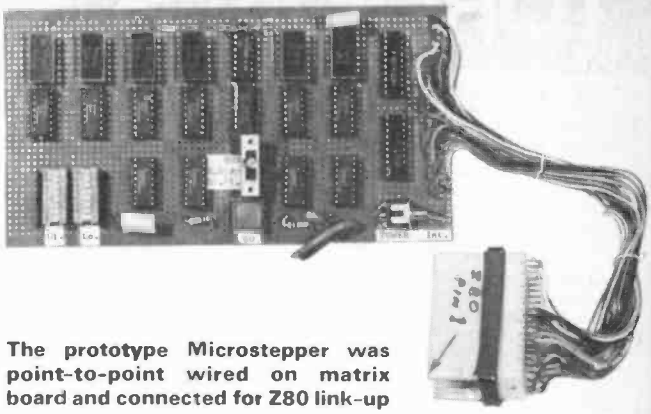


Make cheque or PO payable to **RH Electronics (Sales) Ltd.** allowing 28 days for delivery. All prices include VAT and p&p
Send or telephone your order to: **RH Electronics (Sales) Ltd., Chesterton Mill, French's Rd, Cambridge CB4 3NP. Tel: (0223) 311290**

the next $\overline{RD}$ or $\overline{WR}$ signal, when the next program step appears on the displays.

"Break point" operation is selected by S2 on "BK". Now, a "low" can only appear on IC14 pin 6 to set IC13a and stop the processor if IC14 pin 5 and IC14 pin 4 are both high. This will happen only if the processor is performing a read or write operation, *and* the address bus bit pattern matches that on S3–18. When this happens, comparators IC12, IC11, IC10, IC9, will all give "=" outputs, producing a "high" on IC15 pin 6, giving the required "high" on IC14 pin 5.

If "RUN" is selected by S2, IC14 pin 5 is held low, so, after pressing "GO" IC13a cannot be set, IC13b cannot be reset, and $\overline{WAIT}$ is held high. S19 selects 5V supply from either the system 5V. rail, labelled "Sys. 5V." on the diagram, or from an external, separate supply, labelled "Ext. 5V."



The prototype Microstepper was point-to-point wired on matrix board and connected for Z80 link-up

40-pin test clip

CONSTRUCTION

All i.c.s and displays are in sockets on my prototype (see photograph) mounted on matrix board, and connected by the "Vero" or "Roadrunner" pen wiring system. The technique is based on a "wiring pen", carrying a spool of fine, polyurethane insulated wire, which emerges from the tip. Using the pen, wire is connected from pin to pin of i.c. sockets, along "wiring combs" which hold the wires neatly. Subsequently, connections are soldered, using a very hot (800°F) soldering iron which melts the insulation and solders the joint at the same time. A very neat, high density circuit board results, but the wiring must be systematic.

It was decided to present a p.c.b. layout for this article, which, although is less compact than that which can be achieved using the prototype approach, does allow an easier and neater approach for the less experienced. The p.c.b. and its component layout is shown in Figs. 2–4.

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Each idea submitted must be accompanied by a declaration to the effect that it has been tried and tested, is the original work of the undersigned, and that it has not been offered or accepted for publication elsewhere. It should be emphasised that these designs have not been proven by us. They will at any rate stimulate further thought.

Articles submitted for publication should conform to the usual practices of this journal, e.g. with regard to abbreviations and circuit symbols. Diagrams should be on separate sheets, not in the text.

MONOSTABLE FREQUENCY DIVIDER

A MONOSTABLE may be used as a versatile frequency divider, as in the circuit shown in Fig. 1.

Here the monostable is triggered by the positive edge of a signal applied to the B input. The R/C timing components are chosen so that the monostable will time-out in the centre of the positive half of the number of cycles that it is being divided by. So that in a divide by three situation such as this the output will time-out in the centre of the positive half of the third cycle of the input (Fig. 2). This provides enough leeway to allow for timing-drift whilst maintaining an adequate duty cycle for jitter-free operation.

This circuit will divide an incoming waveform by any integer up to a practical maximum of eight. The waveforms shown illustrate the circuit in operation for a divide by three.

P. Thompson,
Glasgow.

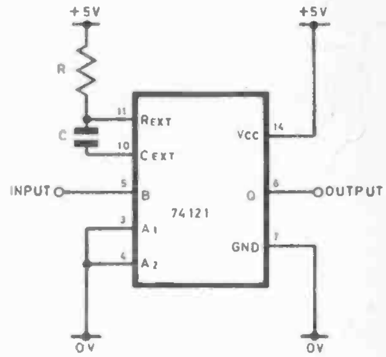
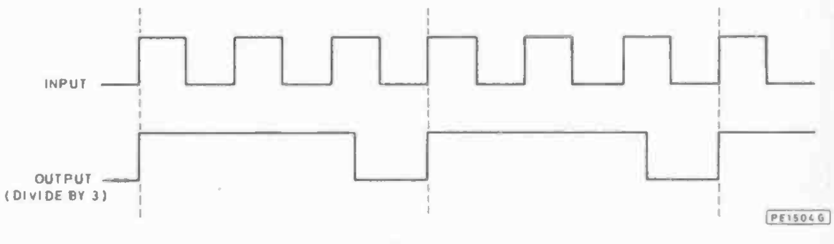


Fig. 1

Fig. 2



THE TRANSPUTER
A COMPONENT FOR THE FIFTH GENERATION
R.W. COLES

OVER the last ten years or so we have witnessed an exponential rise in the performance of microprocessor chips. Four bit processors rapidly gave way to eight bits, then sixteen, and now manufacturers are jostling for position in the race to introduce thirty two bit devices which promise to bestow the power of a midi-computer to the most humble office and domestic applications well before the end of the decade, the new Sinclair Quantum Leap (QL) being a fine example both in name and computing capability. Clock speeds have increased from a few hundred kHz to several MHz, and already 25MHz has been promised for advanced versions of devices now in production. To make all this possible, semiconductor manufacturers have been shrinking the geometrics of the individual active components on the chip so that line widths of only one micron (10^{-6} metres) will soon be routine, and up to one million components will be possible on each chip.

An uninformed statistician could no doubt analyse these trends and draw elegant graphs which would probably predict that by the year 2000 the average home computer would have a 512 bit word size, a clock speed of 1GHz, and would contain a CPU chip with one thousand million active components using line widths of one hundredth of a micron. A similar exercise carried out at the zenith of railway development would probably have predicted that by now, every house would be on a branch line carrying Mach 2 locomotives. A prediction which, fortunately, has not been fulfilled due both to a strictly limited need for such travel facilities, and to the development of other more convenient forms of travel which have, to some extent, made railway travel obsolete.

Similar limitations apply to microprocessor development. There is no real need for word sizes much beyond 32 bits, and although we may get as far as 64 bits for some specialised applications, we will soon see this particular growth curve flatten out. As to shrinking chip component geometrics, unfortunately this fundamental route to growth will soon be up against limits set by the physics of semiconductor materials and the resolution available, even theoretically, from the lithographic process used in chip manufacture. Clock speeds too, are unlikely to go much above 100MHz.

One of the few remaining routes to growth will involve the eventual production of larger chips, using the so-called wafer-scale integration technique, but this process is more likely to be used for building complete systems which include lots of memory and I/O, than it is for the creation of bigger and better microprocessor devices. So, are we about to witness the end of the microprocessor revolution? Not if Inmos have their way!

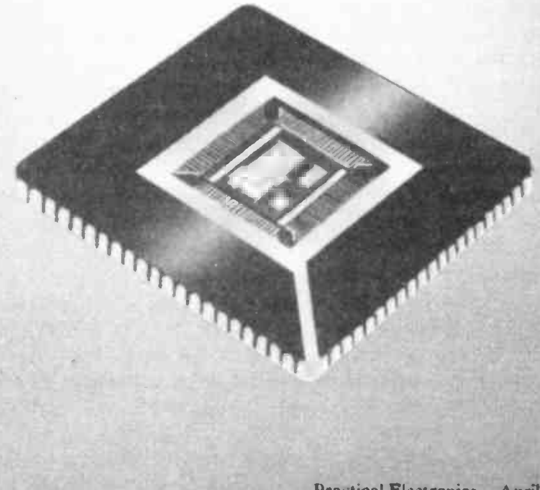
The real root of the problem is that nearly all current computers and microprocessors use the same conceptual approach to data processing, an approach which relies on a single, central, processor, which can run only one program at a time. This concept is so fundamental to our thinking that in the constant deluge of microprocessor enhancements and developments, we hardly even notice that all the "new" devices are based on exactly the same basic principles; principles which were in fact laid down as the bed-rock of digital data processing way back in the nineteen forties. This so-called Von Neumann approach to computer architecture has served us well, but the limits to growth we have already examined will ensure that it will eventually have to be replaced by something radically different, and one of the first attempts to formulate a new approach has come from the British based semiconductor manufacturer, Inmos.

INMOS

Inmos, you may recall, was set up by a group of expatriate British chip designers based in the USA with the help of massive financial backing from the good old British taxpayer. For once, our money was not used to subsidise or prop-up ailing industries within the UK, but was instead bet fairly and squarely on the roulette wheel of international semiconductor development, an enterprise renowned for its high stakes, high risks, and high pay-offs for the winners.

Inmos was not set up to be a half hearted "me-too" semiconductor house to second-source other manufacturers' successful products. From the outset it was planned and organised to become just one thing: a market leader. To begin with, Inmos concentrated on the memory market, introducing a string of innovative devices which quickly established its reputation as a supplier of the fastest memories available. Its first products, the 1400 series of 16K static RAM chips, were designed in the USA and launched on a receptive world in 1981. Since then, Inmos has built a new manufacturing facility in South Wales and has introduced a family of high speed 64K dynamic RAMs which will assure them a secure place among the memory leaders.

While building up its capabilities in the specialist memory area though, Inmos has not forgotten other aspects of system design, and has been very busy at its second design centre in Bristol working on the development of a show-stopping new microprocessor concept, which, if it succeeds, will change the



whole face of digital data processing as we know it today.

Inmos itself does not use the word "microprocessor" very often when describing its new processor. Instead, the new term "Transputer" (which is a contraction of Trans(istor) and (com)puter) has been coined to underline the expectation that its new devices will become universal components, used together in large quantities just as transistors are today.

TRANSPUTER

The first Transputer product, the T424, is a 32 bit microcomputer with all the resources normally required by a computer system, including processor, memory and communications, all available on a single chip of silicon containing 250,000 separate active devices. The first T424 devices are not planned for release until late 1984, but in view of the radical design and programming concepts involved, Inmos have wisely decided to "launch" the Transputer concept early so that potential users can become familiar with its capabilities. No doubt the need to raise further funding to complete development also figured in the decision!

The basic architecture of the T424 is shown in Fig. 1, and at first sight there is nothing particularly remarkable about it, except perhaps the ambitious scale of the device with a 32 bit processor, memory, and I/O all on one chip. The most important features of the Transputer though, are not to be found in its sheer size (or lack of it), but are more intimately related to its communications links and its simple, even primitive, instruction set.

The Transputer is *not* designed, as most other processors are, to be the Prima Donna of a microcomputer system, sitting in the centre of a large supporting cast of memory and peripheral devices. Instead, it is at its best when used as part of a team of other Transputers, all tightly coupled and working closely together to increase processing power and system throughput.

Despite this unusual propensity for team-work, a Transputer *can* be used alone like a conventional processor if required, and many of the initial applications for this device will probably use it alone or in small numbers, if for no other reason than that it will initially be quite expensive. Later, as prices fall and as other processors run out of steam in the continuing race for higher performance, the building-block capabilities of the Transputer will enable powerful data processing systems to be built up on a single circuit board containing tens, or even hundreds, of separate T424 chips, all working in concert. Furthermore, when the wafer-scale integration technique mentioned earlier becomes a practical reality, large arrays of Transputers can be interconnected directly on a single wafer of silicon to create, for example, a processing engine for the supercomputers of the so-called fifth generation.

As can be seen in Fig. 1, the T424 is unusual in having six separate interface channels on the chip. The memory interface is a 32 bit, multiplexed address/data channel with a 25Mbytes per second bandwidth, able to access up to four gigabytes of external static or dynamic memory at very high speed. The 32 bit address range includes the 4Kbytes of 50ns on-chip RAM, and when the Transputer is used as a jelly-bean component in an array, this may be all the memory required to hold both instructions and data. Even in array applications however, there will probably need to be at least one Transputer with access to a large conventional memory array holding the main operating program and the data base.

The peripheral interface is unusual in that it is separated from, and can act concurrently with, the memory interface to access standard peripheral devices such as I/O processors and controllers at high speed, while normal external memory operations take place at the same time. At 4Mbytes per second, the bidirectional peripheral interface is no slouch, and can even be used to perform block memory transfers (from ROM for example) if required.

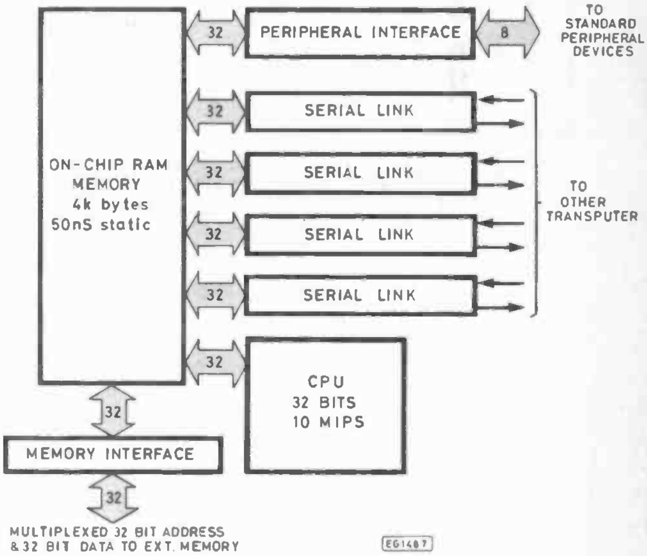


Fig. 1. The revolutionary architecture of the new T424 Inmos Transputer chip

Finally, and most importantly, there are four bi-directional serial communications channels which can also operate concurrently with each other and with the memory or peripheral interfaces. A collection of four serial interfaces would be of benefit to any microprocessor of course, but the serial channels on the T424 are not intended for traditional and mundane tasks such as driving printers or Modems. These serial interfaces are provided purely as inter-Transputer communication links, and with four available, a two dimensional array of Transputers can easily be constructed with tight coupling to neighbours in the up, down, left and right directions. Each inter-Transputer link can transfer data at 1·5Mbytes per second in both directions simultaneously, using a byte organised message format which can transmit data blocks of any length for memory to memory or CPU to CPU communications. The use of a serial protocol and separate links for each channel has obvious advantages over the shared parallel bus approach used by other inter-processor communications schemes, simplifying board layout and increasing the overall communications data rate by facilitating the simultaneous operation of multiple links in each system.

The on-chip memory array uses the much vaunted high-speed static memory technology already in use in other Inmos products to achieve an impressive 50ns cycle time with separate access ports for the CPU, the peripheral interface, and all four of the serial channels.

The CPU itself is a very fast 32 bit parallel processor which can execute most of its instructions in just 50ns. The CPU utilises the "Reduced Instruction Set Computer" or RISC approach, having only 70 instructions in all, and keeping data access operations separate from logical or arithmetic operations. This approach avoids the usual requirement to cater for multiple combination of data types and addressing modes which often cause the total instruction sets of more conventional microprocessors to mushroom to many thousands of variations. Despite the simplicity of the RISC approach however, Inmos claim that the functionality of the instruction set is high, and that programs require no more code than would be required by the more conventional approach used in most other microprocessors.

CONCURRENCY

As we saw earlier, current computer architectures are based on the historical premise that the processor is more expensive than the memory which serves it, and this has resulted in the "Von Neumann bottleneck" which puts constant emphasis on improvements to the central processing "engine" for the achievement of increased performance. With the coming of VLSI (Very Large Scale Integration) this economic perspective no longer holds true, and perhaps even more significant, the performance which can be squeezed from a single processor is fast approaching a physical limit. It is therefore time for the "railway-engine" approach of the all-powerful Von Neumann architecture to give way to the "private-car" approach of multiple, concurrent processing activity. This approach is at the very heart of the Transputer concept.

Unfortunately, the tangled infrastructure of today's data processing methodology, including all the high level languages such as BASIC and PASCAL, caters only for the Von Neumann approach to computer design, making the re-education burden now shouldered by Inmos all the more daunting. Realising the problems they would face in overcoming the inertia inherent in such an ingrained methodology, Inmos wisely recognised that simply presenting the world with a revolutionary piece of new hardware would not be enough to effect any change. To back up their Transputer they needed to introduce a new software approach to handle concurrency, and to satisfy this need they have developed a brand new computer language called Occam after the fourteenth century philosopher who first formalised the concept known as "Occam's razor" which in a nutshell states: keep it simple!

Occam and the Transputer operate hand-in-glove to implement what is known as the "process model" of computing as illustrated in Fig. 2. A process is an independent sequential computation, complete with its own program and data, which can communicate with other processes executing at the same time. Communication between processes is by message passing using explicitly defined channels which may either be implemented using physical links (such as an inter-Transputer serial channel) or by using software organised channels using memory buffers as the link. Communication between processes is synchronised so that a message can only be sent over a channel when both the sender and receiver are ready, and as a consequence, the process which first becomes ready must wait for the second process before the link is completed.

The Transputer directly implements the Occam model of a process to the extent that internally it can behave like any Occam process which is within its capability. In particular, a Transputer can implement *internal* concurrency by timesharing processes using the instruction set facilities provided directly for that purpose, and can implement *external* concurrency by using its inter-Transputer links for message exchange with processes running on other devices. As a result, the same Occam program may be executed either by a single Transputer, or by a whole network, with consequent gains in performance.

OCCAM

The Occam language is a high level language when judged against conventional criteria, but it is also the lowest level at which a Transputer will be programmed. The instruction set of the processor is not pure Occam however, and represents a somewhat more primitive level of operation which is optimised for direct compilation from Occam itself. Direct use of the Transputer instruction set is not supported, and no assembler will be available, because compiled Occam will be at least as efficient as a hand coded alternative.

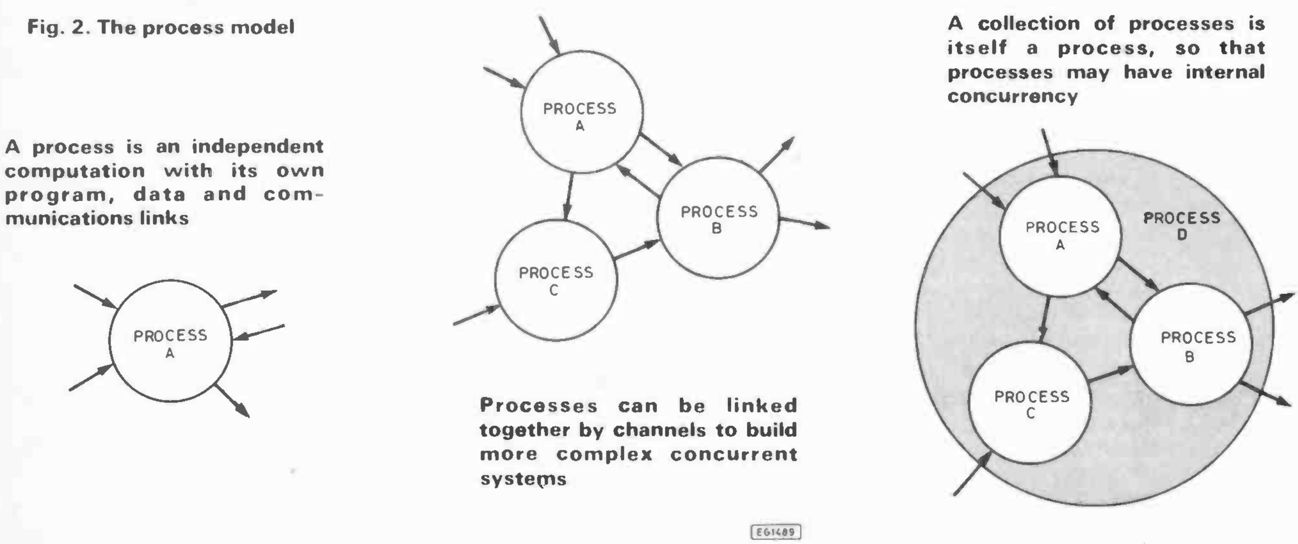
Occam may have been developed specifically for the Transputer, but it is not limited to use on that processor and software development tools are already available to facilitate its use on a number of other systems including the Apple II, the Sirius, and the IBM PC. Although practical working Occam software can therefore be developed for other processors, the full potential of the language will not be realised until the Transputer itself is in widespread use.

Even the Transputer, though, is not limited to the use of Occam alone, since its instruction set has also been optimised for efficient compilation from other high level languages such as PASCAL, ADA, and even BASIC. As a result, the Transputer programmer may use Occam alone to take advantage of its efficient handling of concurrency, or may simply use it as a harness to link software modules written in other high level languages which may be better suited to certain types of data processing task.

CPU ARCHITECTURE

The Transputer CPU architecture (Fig. 3) overturns many of the old established concepts of "desirability" which have been preached in the PE Microfile series and elsewhere. An array of general purpose registers is nowhere to be seen, there is no stack

Fig. 2. The process model



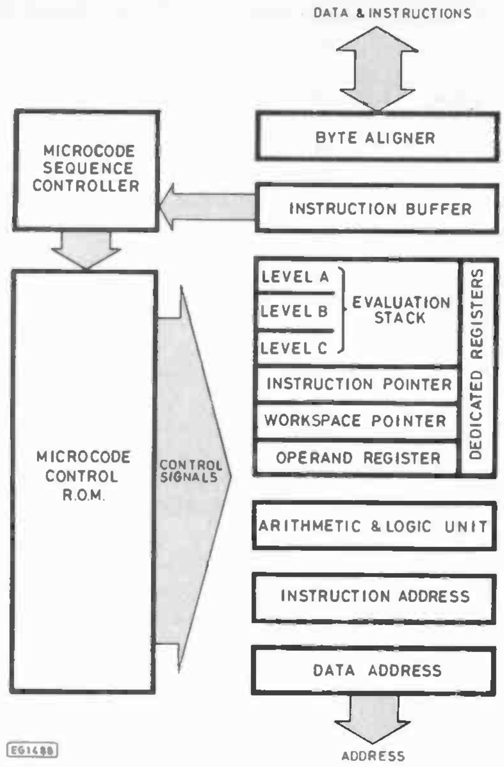


Fig. 3. CPU architecture of the Transputer showing the six dedicated registers

in the conventional sense, and the long sought after concept of virtual memory addressing is ignored. The reason for this upturned apple-cart, however, is not hard to find.

Take a look at any conventional 16 or 32 bit microprocessor and you can see the lengths to which chip designers have had to go to squeeze the ultimate in performance from their Prima-Donna processor. Every conceivable useful concept and add-on hardware extra has been included to overcome the restrictions which result directly from the Von Neumann bottleneck. As a result, data manuals are getting thicker, and learning a new processor has become a time-consuming business for both the hardware designer and the programmer.

A Transputer system, on the other hand, is not constrained by the single CPU bottleneck, and as a result "Occam's razor" can be applied to the processor architecture to keep everything as simple as possible. Unlike other microprocessors the Transputer does not have a large register file, instead, it has a minimum set of functionally dedicated registers and an evaluation stack. This approach simplifies compiler design since all of the operands are in a uniformly addressed data space. It also minimises the context switching time required for interrupts by eliminating the need to save lots of registers on a stack. This in turn reduces the time overheads involved when executing concurrent processes and improves the real-time response of the system.

A sequential process is executed using just six registers, each one word long, or 32 bits for the T424. This register arrangement is also shown in Fig. 3, and is the ultimate in simplicity.

The instruction pointer defines the next instruction to be executed, and is therefore what we generally call a program counter, the operand register is used in the formation of instruction operands, and the workspace pointer defines an area of RAM memory where local variables are held. Programmers never have to refer to these registers directly since their function is implicit in any instruction which uses them, as is the function of the remaining three registers together forming the evaluation stack.

The evaluation stack operates in a similar way to the stack used in the famous Hewlett Packard range of scientific calculators, and anyone who has learned to use one of *those* would never swop it for the messy algebraic notation used by most of the competition. Expressions are evaluated on the three entry stack, and instructions refer to the stack implicitly. When an Add instruction is executed for example, the top two values in the stack are added and their sum is placed on the top of the stack. The use of an evaluation stack removes the need for

One address instructions

Load local	Load constant
Store local	Add constant
Load local pointer	Add to memory
Load non-local	Jump
Store non-local	Conditional jump
Load non-local pointer	Call
	Adjust workspace

Zero address instructions

Add	Load byte
Subtract	Store byte
Multiply	Byte count
Divide	Word count
Remainder	Byte subscript
Long add	Word subscript
Long subtract	Check subscript
Long multiply	Extend to word
Long divide	Check partword
Normalise	Extend to double
	Check word
Difference	Read timer
Greater than	Test error
Equal zero	Reverse
	Return
And	Minimum integer
Or	Initialise
Xor	
	Start process
	End process
Shift left	Alt start
Shift right	Enable channel
	Enable timer
Move message	Disable channel
Input message	Disable timer
Output message	Alt wait

Fig. 4. The basic Transputer machine code instruction set

		Program size (bytes)	Execution time (ns)	External program access† (ns)	External data access† (ns)
Arithmetic operators	+, −	1	50	p	0
	★ (multiplication)	1	950	0	0
	/ (division)	2	1950	0	0
	\ (remainder)	2	1950	0	0
Comparison operators	>, =, <>, <, <=, >=	2	100	2p	0
Logical operators	AND, OR	1	50	p	0
	/\, \/, >< (xor)	2	100	2p	0
Shift operators	<< [n], >> [n]	2	50n+50	0	0
Identifiers	variable	1.7	120	1.7p	d
	vector variable	2.7	160	2.7p	d
Expression evaluation	constant	1.3	70	1.3p	0
	parenthesis	0.5	50	0.5p	0.5d
Constructors	SEQ [n]	0	0	0	0
	PAR [n]	9n-7	450n-200	7np+nd	d+4nd
	ALT [n]	8n+7	600n+600	8p+2d	5d+4nd
	IF [n]	3n	150n	2nd	0
	WHILE	4	200	2d	0
Primitives	! (output), ? (input)	4	625	3p	5d
	! [n], ? [n] (vector)	4	50n+625	3p	5d+nd
	:= (assignment)	0	0	0	0
	:= [n] (vector)	4	100n+300	3p	2nd

†The additional time for access to external memory depends on the type of memory. The parameters for various types of INMOS memory are:

	p	d
IMS 1400-70 static RAM	20	100
IMS 2600-12 dynamic RAM	40	150
IMS 2600-15 dynamic RAM	55	200
IMS 3630-20 erasable ROM	55	200

Fig. 5. The Occam language syntax. The 'program size' column shows how few bytes are required for machine code instruction sequences

instructions to continually respecify their operand locations.

Also implemented in the CPU logic is a hardware scheduler which enables any number of concurrent processes to be executed together and to share the processor time in a controlled way. Two process status levels are supported, normal and priority, with the priority classification reserved for processes which would normally be performed using interrupt routines.

If a normal process is being executed and a message arrives from a priority process (over an inter-Transputer link for example), the processor saves the context of the current process in the RAM workspace area and begins to execute the priority process within 2 microseconds. Normal processes will only be resumed when all priority processes are unable to proceed or have been completed. Special instructions are provided to support the concept of concurrent processing on the Transputer.

INSTRUCTION SET

Like the architecture of the Transputer CPU, the instruction set is simple and straightforward, with all instructions being only one byte long. One consequence of this simple approach is the incredible speed of processing which the Transputer can attain, up to 10 Million Instructions Per Second (10 MIPS) when running from internal memory. The very best conventional microprocessors, such as the Motorola 68000, can manage only about 1 MIPS.

Each one byte instruction is divided into two four bit fields:

1 Byte							
7	6	5	4	3	2	1	0
Function				Data			

The four most significant bits are a function code, and the four least significant bits are a data or address offset value. There are two basic types of instructions as follows:

One Address Instructions:

These instructions, of which there are thirteen, represent the most common operations performed by a program such as loading or storing one of a small number of variables, or loading a constant. With only four bits available for variable addressing there is clearly no way to access the 4Gbyte memory space directly. To overcome this limitation, the four bits are used as an offset, relative to either the 32 bit workspace pointer or to a previously computed 32 bit pointer in the operand register. The basic single address instruction format therefore provides for immediate access to 16 locations in the workspace area and another 16 locations which may be located anywhere in memory. This is considered sufficient for over 80% of memory access operations. When larger offsets are required, the rather unusual approach of using a sequence of instructions to extend the offset by four bits for each instruction can be employed. In effect, memory addresses are frequency encoded which is more efficient overall than the use of a fixed, full width address for every access, even for locations in close proximity.

Zero Address Instructions:

All the remaining instructions use the evaluation stack as the implicit source for operands, and this type can be subdivided into the following classes:—Arithmetic, Logical, Conditional, Data Structure and Process.

The arithmetic operations include multiplication and division, and support multilength and floating point arithmetic with overflow monitoring. The basic division operation, for example, is division of a signed 32 bit number, giving a signed 32 bit result and remainder.

The data structure operations provide the means to access byte and word data structures which may include multidimensional arrays, and enable data structure access to be independent of word length.

The process instructions support the Occam model of processes. They include instructions analogous to the input, output, block move and procedure call instructions of other microprocessors, with the difference that the Transputer instructions are designed to support a well-defined model of concurrency in which all process communication is synchronised.

As mentioned earlier, it is not proposed that Transputer programmers will have access to the basic instruction set, but it is listed here for completeness in Fig. 4. Of more relevance to programmers is the Occam syntax, which is listed in Fig. 5. It is easy to see why the basic machine code instruction set can be ignored in favour of Occam by looking at the "Program Size" column which shows that most Occam statements compile into very short machine code instruction sequences, often of only 1 or 2 bytes.

TRANSPUTER SYSTEMS

So far we have looked exclusively at the 32 bit T424 Transputer which will be the first device to become available in late 1984. A great advantage of the Transputer concept, though, is the fact that many other compatible configurations are

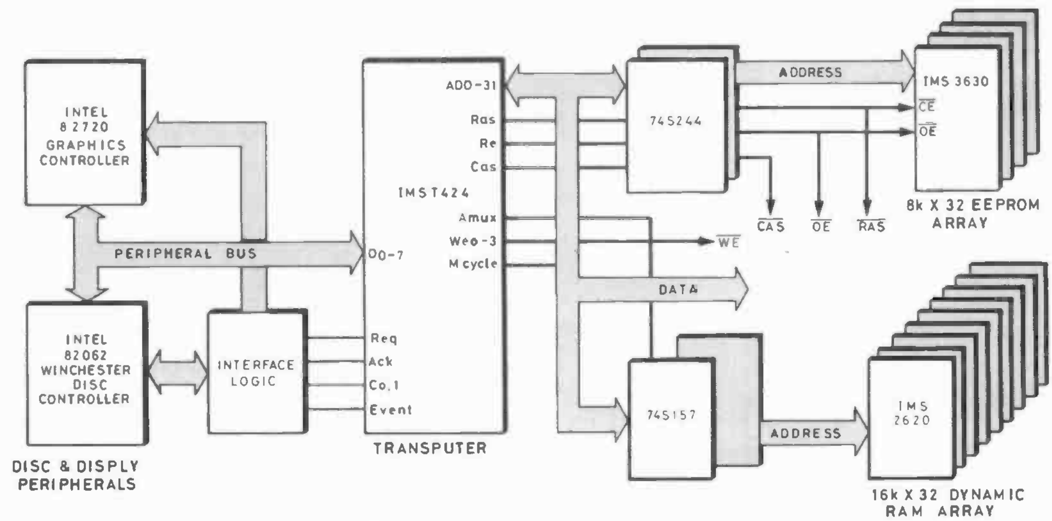


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Fig. 6. A single Transputer microcomputer circuit

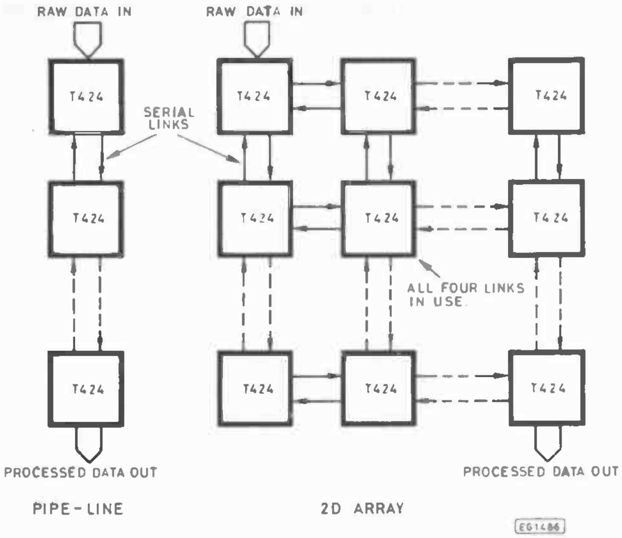


Fig. 7. Two examples of multi-Transputer networks. Such configurations are possible with other microprocessors but the complexities of interconnection and the nightmare of software design make the concept generally impracticable

possible without the need to change the Occam syntax.

Also planned is a 16 bit version, the T222, which will have an identical instruction set and will operate at the same speed as the T424 within the restrictions of its shorter word length. Also planned are specialised Transputer devices such as the G213 graphics processor, and the M212 disc processor which will both be based on the 16 bit architecture of the T222.

The package style chosen for all Transputer products is the ceramic Leadless Chip Carrier (LCC) which is also being used for advanced conventional microprocessors such as the Intel 80286. The T424 will use an 84 connection LCC roughly one inch square (Page 26), while the T222 will use a 68 connection package. All Transputers will be fabricated using a CMOS process and will run from a 5MHz system clock. The T424 will operate from a 5 volt supply and will dissipate only 900mW.

A basic single Transputer system can be assembled with relatively few components as shown in Fig. 6. This simple system is comparable to any other high performance single CPU disc based microcomputer and demonstrates how conventional a Transputer system *can* be. The two arrangements shown in outline form in Fig. 7 provide a glimpse of the more exotic system architectures which are more likely to justify the use of the Transputer in large numbers. With networks like these available, the age of the truly intelligent supercomputer cannot be far away! ★

35 LED TACHO

THIS circuit uses the MM5451N shift register and l.e.d. driver to provide a bargraph display of engine revs.

The circuit operates as follows: When the output of IC1d is high, pulses are received from the points via IC1a & b which operate as a Schmitt trigger, and are used to clock the shift register—the data input is held high. When the output of IC1d is low the data input is low and IC1e & f provide clock pulses to fill the shift register with zeros—the shift register will not accept any more data after it is full until the data input goes high again. Thus, a number of l.e.d.s are switched on corresponding to the number of ignition pulses received. The display updates every 0·3 seconds.

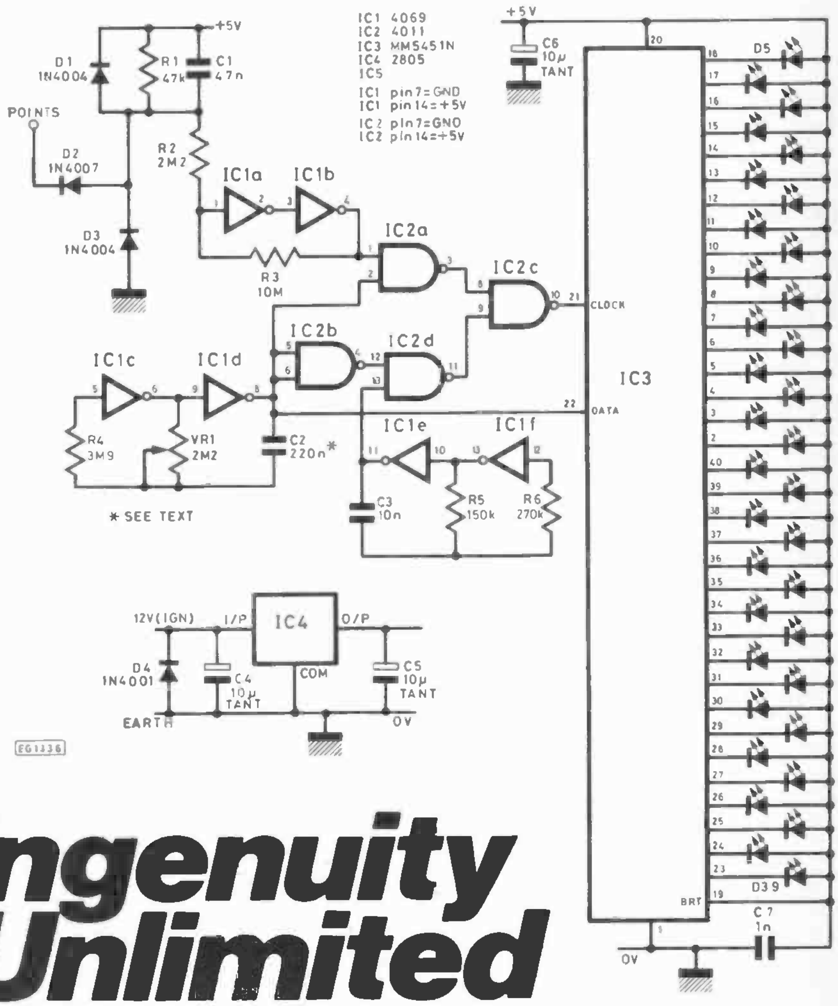
The IC1a & b clock should be set to 3·33Hz for a four cylinder engine (5Hz for a six- and 6·67Hz for an eight-cylinder engine). This gives a maximum reading of 7000 r.p.m. The value of capacitor C2 may need to be decreased.

C4, 5 and 6 are decoupling capacitors and should be connected as close to the i.c.s as possible. C7 decouples the brightness input which is set to maximum. IC4 provides a stable 5V supply and requires a heatsink.

The MM5450N could be used instead—this only has 34 outputs and a 'data enable' input on pin 23 which should be tied to 0V.

This circuit is suitable for negative earth vehicles.

I. Benton,
Bardney,
Lincoln.



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I HAVE never, as a journalist, been much of a scoop-artist. Let others, if they must, spend fruitless nights on the steps of No. 10 in the vain hope that, as the result of a dubious tip-off, they'll nab the PM coming home stoned from a summit meeting. Let others seek to build up evidence that Dean Martin is secretly addicted to lemonade and that Robert Mitchum really lives. Personally I've always taken the authenticated news as it comes.

Yet this philosophy, Kismet being what it is, does not prevent one stumbling across the occasional exclusive. Such a thing happened to me last week when taking a milk and honey in one of the better class bars with someone in a high place in the engineering industry who ought to have kept his mouth shut—or stuck to the straight milk.

To explain the importance of his revelations to me, it would help to hark back to August 1982 when an article appeared in a leading industry weekly. It told how a group of senior engineers—long in both tooth and memory—were planning to mark the 100th anniversary of the discovery of Gummidge's Gangulating Gyrator.

Without going into a lot of technical detail, this was a contrivance of incredible versatility. It was capable of performing a host of functions, from the liquidisation of solids to the taking of passport pictures, from cutting keys to playing simulated versions of the light classics. The fact that it was eventually superseded by the American-born Goldblatter's Gyrating Gangulator—which could also fell a forest in a matter of minutes—is neither here nor there. The seed of multi-function had been well and truly sown.

But Gummidge and Goldblatter were reduced in my mind to the status of bungling rat-finks by the story unfolded to me by this milk-and-honey-sodden mole whose tongue flapped untiringly for the best part of an hour like the Royal Standard in a high wind. If only half of what he told me comes to pass, it will create turmoil in the race for technological supremacy throughout the world.

In case you think that, in my usual fashion, I am treating what could be a major revolution in the electronics industry in a flippant manner, let me give you some solid facts.

A powerful consortium of top US engineers, drawn from every interested discipline—electronic, electrical, medical, ergonomic, constructional and so on—and funded by massive sums from both State and Federal resources, have set up a research and development facility, the size of a small town, in the wastes of the Nevada desert, to produce what they believe is the ultimate in robotics.

The project has been provisionally named 'Manservant'. It is virtually a single unit, utilising to the full all the potential of advanced engineering technology, designed to cater for every conceivable human need.

The concept is based on a set of micromin modules—supported by scaled-down mechanical assemblies—and a microprocessor-controlled master unit at the heart.

My informant, being a sot rather than a scientist, was unable to go very deeply into specifications. But he was obviously near enough to the centre of things to reveal with some authority what 'Manservant' is likely to be capable of doing.

First of all, as might be expected, it provides the full range of consumer services: cable/satellite colour TV and stereo sound on an almost limitless number of channels. In addition it comprises a full range of recording facilities, video and audio, and an impressive selection of high-quality reproduction equipment.

On the professional side, it embodies a sophisticated data processing unit and inputs not only to our very own Prestel, but also to lesser-known foreign electronic information services such as Denmark's 'Danksgen', West Germany's 'Informatzionengas', and Spain's new and promising 'El Tellu'.

"A shoe polishing unit is an optional extra"

Perhaps the most exciting feature is a stunningly-designed personal helicopter. It consists of an ultra-lightweight yoke assembly which, when clipped to the shoulders, enables the user to cruise comfortably at an altitude of 50ft at a speed of about five miles an hour—ideal for getting from shop to shop when doing your Christmas shopping in Oxford Street. Power is supplied by one of 'Manservant's' vast range of modules. Controls, set in a chest-mounted panel, are no more complicated than those of a basic gas cooker.

Talking of cooking, 'Manservant' includes, as well as a super high-speed microwave oven, a subsidiary unit, tentatively named 'Maidservant', which will peel potatoes, slice meat, shred cabbage, skin onions, dice carrots and turn out an acceptable strawberry mousse. It can even handle the washing-up and serve coffee and brandy.

'Manservant', let it be made clear, is no ill-chosen name. For the lonely and helpless bachelor it will handle—including ironing and trouser pressing—a full 14lb load of washing and, if needs be, remove soup stains from the lapels of sloppy diners. A shoe-polishing unit is an optional extra.

These are but a few of the blessings—there are many more too numerous to be mentioned here—which in the near future will enrich the lives and increase the leisure of those of us fortunate enough to have been born in the electronic age. The fact that the complete 'Manservant' unit packs compactly into a carrying case the size of a piano accordian is a consideration not to be sneezed (or should it be squeezed?) at.

As usual, the one obstacle to its universal adoption could be the matter of cost. So far around $200 million has been sunk into R&D. The cost of manufacture has not yet been looked at. However, it is probable that 'Manservant', if and when available in the UK, would rank in price with a seven-bedroom, two-bathroom, double-garage, centrally-heated family house standing in six acres in the stockbroker belt of South-East England. Maybe some enterprising building society will come up with a 'Manservant' mortgage scheme.

In the meantime, the US consortium cannot afford to be complacent. A state research establishment, sited in the bowels of a defunct volcano on the shores of the Black Sea, is already working on a Soviet version called 'Dogsbodya'.

The race, then, will be to the swiftest.

* * *

You may recall that I recently drew attention to the plight of the middle-aged engineer who couldn't come to terms with modern technology. In particular he was bugged by the new gobbledegook which is so cruelly disfiguring the noble English tongue.

Since then I've been reflecting upon his distress and I've come to the conclusion that I've got a touch of the same trouble. Every day some fresh distortion is thrust upon us. Indeed, I have the feeling that somewhere in the electronics industry there is a little clique whose only contribution to progress is to think up grotesque words and phrases for foisting upon those who once took a pride in speaking English as she ought to be spoken.

My view was not changed when there plopped through my letter-box the other day—along with some bumph about double-glazing and a red notice from the Gas Board—a newly-published glossary of terms used in Satellite and cable TV.

The document was a revelation. And to show the extent to which the mists of my misunderstanding have been dispelled, let me give you some examples of my former interpretations of well-known expressions which are now being bandied about—with entirely new meanings—by those in the SCT know.

Tiers: Lachrymal secretions which exude from the eyes when watching a sick-making wedding or convenient demise on Coronation Street. Another form of this condition is called the Russell Harty syndrome. *Premium Channels:* The electronic means we shall shortly be using to pay our life, house and car insurance contributions. *Narrowcasters:* News readers on diets. *Addressability:* The possibility of communication with anybody with a fixed abode. *MAC:* What you leave at home—because Michael Fish seems such a reliable lad—and subsequently need. *Scrambling:* Something fighter pilots used to do during World War II and what housewives have been doing with eggs ever since the hen was invented.

(It is the April issue! Ed.)

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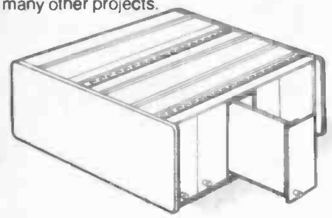

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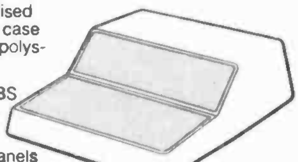
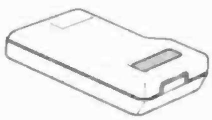


Hand Held Box



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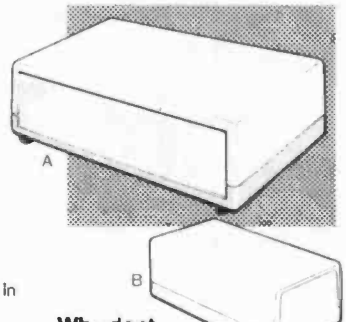

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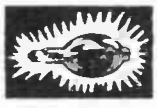

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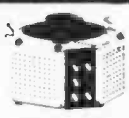

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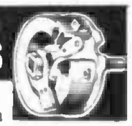

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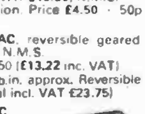

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MICRO-BUS and MICROPROMPT

Appearing every month, Micro-Bus now presents ideas, applications and programs for the most popular micro-computers and all micro-related projects so far published in PE. Ideas must be original, and payment will be made for any contribution featured.

UK101

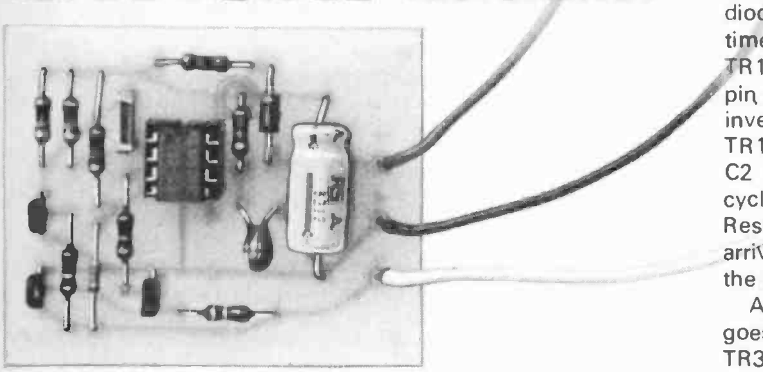
Sir—This program will display an enlarged character set on the UK101 in which the full ASCII upper case character set may be displayed. The program will ask you to input your message. This is stored in N$ and may contain any upper case ASCII character. To start a new line use CONTRL N. The space bar inserts a space between characters. The display is 9 character wide by 5 high on a 32 line screen. For a 16 line screen the variable TX should be 54272. The character definitions are stored in A$(J).

P. N. Martin,
Weymouth.

```
170 REM**** READ IN THE CHARACTER DEFINITIONS
180 READ A$:IF A$<>"Ø" THEN NC=NC+1:GOTO18Ø
190 RESTORE:DIM A$(NC—1)
200 FOR J=Ø TO NC-1:READ A$(J):NEXT
210 READ A$:J=Ø
220 READ CH(J):IF CH(J) THEN J=J+1:GOTO22Ø
230 TØ=53261:TX=55296:REM**** START AND FINISH OF DISPLAY 32 LINES
240 A=ASC ("A"):Z=ASC("Z")
250 ZE=ASC("Ø"):NI=ASC("9")
260 PRINTCHR$(26);:REM**** CLEAR SRCREEN CEGMON
270 INPUT "Message"; IN$
280 PRINT CHR$(26);:T1=TØ:TL=TØ
290 FOR T=1 TO 6:PRINT;:NEXT:PRINTCHR$(13);
300 FOR I=1 TO LEN(IN$):REM ** EXTRACT THE CHARACTER TO BE DISPLAYED
310 CH=ASC(MID$(IN$,I,1))
320 IF CH>=32 THEN36Ø:REM IF NOT SPACE THEN SKIP
330 FOR T=1 TO 6:PRINT:NEXT
340 T1=T1+384:IF T1>TX THEN T1=TX
350 TL=T1:GOTO48Ø
360 CH$=A$(CH-32):REM EXTRACT THE RELEVANT DEFINITION STRING
370 FOR J=2 TOLEN(CH$)
380 C=161
390 CØ=ASC(MID$(CH$,J))
400 IF CØ>=A AND CØ<=Z THEN43Ø
410 C=CH(CØ-ZE):J=J+1:IF J<=LEN(CH$) THEN39Ø
420 GOTO47Ø
430 Y=INT((CØ-A)/5)
440 X=CØ-A-5*Y
450 POKE TL+X+Y*64,C
460 NEXT J
470 TL=TL+ASC(CH$)-ZE+1
480 NEXT I
490 GOTO27Ø
500 REM**** DEFINITIONS OF CHARACTERS, ARRANGED IN ASCENDING ASCII
510 REM**** VALUE, STARTING WITH ASCII SPACE
520 DATA 4ØA
530 DATA 1AFKU
540 DATA 3AC
550 DATA 45A6B5C6DFGHI5K6L5M6NPQRS5U6V5W6X
560 DATA 4DCB1AF3KLM2NS4XWVU5G6H5Q6R
570 DATA 41D4I1H4M1L4Q1P4UAX
580 DATA 43X6SR2ML2G3F1AB2C4H1KP3UV4W1N
590 DATA 1AF
600 DATA 24B1AFKP3U2V
610 DATA 23A2BGLQ4V1U
620 DATA 4KLMN3F2G3R2S4I1H4Q1P
630 DATA 4GLQKM
640 DATA 2Q4V1U
650 DATA 3KLM
660 DATA 1U
670 DATA 41D4I1H4M1L4Q1P4U
680 DATA 4B1AFKP3UVW4XSNI2DC
690 DATA 331ABGLQUVW
700 DATA 41ABC2DI4NML1KPUVWX
710 DATA 41ABC2D4I1HLM2NS4XWV3U
720 DATA 41CH1G4L1KPQRSHMW
730 DATA 4DCBAFKLM2NS4XWV3U
740 DATA 42DCB1AFKP3UVW4XS2NML
750 DATA 4ABCD4I1H4M1L4Q1P4U
760 DATA 4B1A3F2G3LM2NS4XWV3UP1KL1H4I2DC
770 DATA 4ML3KF1ABC2DINS4XWV3U
780 DATA 1FP
790 DATA 1FP1U
800 DATA 21G4L1K3P2Q3V
810 DATA 3FGHPQR
820 DATA 22F3K2L4Q1P4U
830 DATA 41ABC2DI4NM1LV
840 DATA 4ØA:REM at(can't be typed!)
850 DATA 4UPKF1ABC2DINSXQR
860 DATA 4AFKPUBC2D1H4ILM2NS4XWV
870 DATA 42DCB1AFKP3UVW4X
880 DATA 4AFKPUBC2DINS4XWV
890 DATA 4DCBAFKPUVWXLM
900 DATA 4DCBAFKPULM
910 DATA 42DCB1AFKP3UVWXSNM
920 DATA 4AFKPULMDINSX
930 DATA 2AB5F6G5K6L5P6QUV
940 DATA 4CHMR4WV3U2PABD
950 DATA 4AFKPU4D1C4H1GL3Q2R3W2X
960 DATA 4AFKPUVWX
970 DATA 5UPKF2A2G3LM4N1I1EJOTY
980 DATA 4UPKFA2G3L2M3RXSNID
990 DATA 4B1AFKP3UVW4XSNI2DC
1000 DATA 4UPKFABC2DI4NML
1010 DATA 4B1AFKP3UVW4XSNI2DCX2Y
1020 DATA 4UPKFABC2DI4NML3Q2R3W2X
1030 DATA 42DCB1AF3KLM2NS4XWV3U
1040 DATA 45B6C5G6H5L6M5Q6R5V6WABCD
1050 DATA 4AFKP3UVW4XSNID
1060 DATA 4AFK3P2Q3V4W1R4SNID
1070 DATA 5AFKP3U4V1QRM2S3X4YTOJE
1080 DATA 4A3F2G3L2M3R2SXD4I1HML4Q1PU
1090 DATA 53A2B3GH4I1D4EMRW
1100 DATA 4ABCD4I1H4M1L4Q1PUVWX
1110 DATA 2BAFKPUV
1120 DATA 42A3F2G3L2M3R2S3X
1130 DATA 2ABGLQVU
1140 DATA 41F1B2C2IGH5L6M5Q6R5V6W
1150 DATA 4ØA:REM -:USE FOR BLANK
1160 DATA Ø : REM** INDICATES THE END OF DEFINITIONS
1170 DATA 32,176,178,177,175,157,156,Ø:REM** GRAPHIC VALUES
```

Car Interior Light Delay Switch

N.J.CHAFFEY



Let there be light!
And let it remain whilst we are grappling with our seat belts.

THIS circuit, for a car interior light delay switch, is designed for permanent addition to the car wiring system without having to break any wires in the existing harness. Other features include low quiescent current consumption—less than 100µA, solid state switching, and an abort facility if the door is reopened during the timing cycle.

The circuit is designed around the popular CMOS 555 timer package. Although the bipolar device may be used as a direct substitute, the quiescent current consumption will rise to about 4 mA. The device is suitable only for NEGATIVE ground vehicles with a +12 volt battery supply and with ground line door switches.

The design is economical in that costly electromechanical devices such as relays are eliminated through the use of semiconductor switching. Samples of the design have been fitted to British and foreign cars, and they have shown total reliability over a period of six months.

Typical cost of the components involved is about £3, exclusive of the printed circuit board or Veroboard, and the wiring connectors.

CIRCUIT DESCRIPTION

The CMOS 555 is wired as a monostable or "one-shot". The length of the *on* period is determined by R4 and C3. Capacitor C3 should be a low-leakage tantalum capacitor to ensure good timing consistency. The timing period is determined by the following formula:

T seconds $= 1{\cdot}1 \times R \times C$ (R = Ohms. C = Farads)
or $1{\cdot}1 \times R \times C$ (R = Mohms. C = µF)

In the circuit illustrated: T = $1{\cdot}1 \times 1 \times 10$ seconds
= 11 seconds

Desired variations in the timing cycle may be made using the formula above, bearing in mind the limited availability of high value low leakage tantalum capacitors at the specified voltage. Also, that the value of R4 should preferably lie between 3k3 and 10M.

Diode D1 is a polarity protection diode in the positive supply line. Resistor R1 and capacitor C1 provide smoothing and filtering of the supply line.

OPERATION

Whilst the car door is shut, S1 is open and the circuit is in its quiescent state. If the door is opened, S1 closes and the interior light comes on, but the circuit remains inactive since pin 4 (Reset) is momentarily held low through D2 to ground, disabling the timer. When the door is closed S1 opens, pin 4 goes high via the pull-up resistor R5—there are now two diode drops to ground, D2 and transistor TR3. At the same time a positive pulse appears by way of R8 at the base of TR1. This pulse is blocked by D2 which is forward biased so pin 4 is not affected. Transistor TR1 is a switch and also an inverter so the pulse which now appears at the collector of TR1 is negative going. This negative pulse is a.c. coupled by C2 to pin 2 (Trigger) of the 555, and initiates the timing cycle. Pin 2 is returned to rail voltage by the resistor R3. Resistor R2 supplies the collector of TR1. Any further pulses arriving at pin 2 are ignored during the timing cycle unless the cycle is aborted and reset.

As soon as the timing cycle begins, the output from pin 3 goes high, turning the solid state switch, transistors TR2 and TR3 fully on and shunting the switch S1 so that the interior light remains on for the duration of the timing cycle.

Transistors TR2 and TR3 are a made up complementary Darlington pair in order to reduce the total V_{be} to one diode drop, that is, to about 0·7 volt. An n.p.n. Darlington, which is available as an on-chip device would have added offset voltages of about 1·4 volts causing a decrease in lamp brightness. If this is tolerable then an n.p.n. device such as the ZTX 600 may be used. R7 and TR2 and TR3 are omitted and the ZTX 600 is used in place of TR2, R7 being replaced with a wire link.

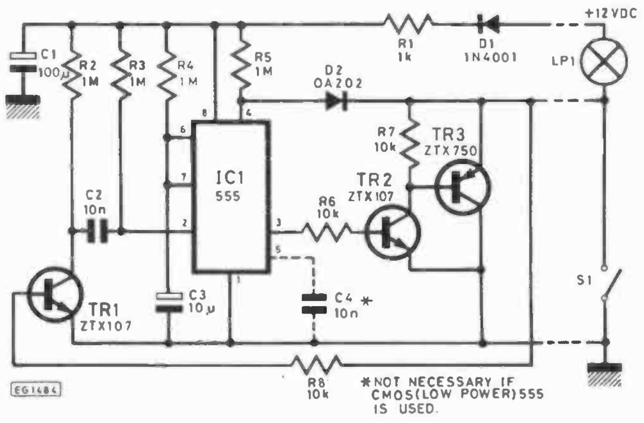


Fig. 1. Full circuit diagram

Transistors TR2 and TR3 are silicon devices, so the base of TR3 would provide an adequate collector current for TR2. However, for peace of mind R7 is included to ensure that TR2 operates correctly.

When the delay period is over, pin 3 goes low, snapping off TR2 and TR3 extinguishing the interior light. If the door is opened during the delay period, a negative pulse arising from the closure of S1 passes through the diode D2 to the reset pin 4 of the 555 pulling it below its operational voltage and aborting the timing cycle. Thus every time the door is opened and closed a complete delay cycle occurs regardless of the state of the circuit.

CONSTRUCTION

A printed circuit layout is shown in Fig. 2, and a component overlay is shown in Fig. 3. Alternatively the circuit may be built on a small piece of stripboard. If the bipolar 555 is to be used then a 10n capacitor (C4) should be connected from pin 5 to ground. It is omitted if the CMOS 555 is used.

All the resistors are soldered in place first, followed by diodes and capacitors—*observe polarity*! The use of a socket is recommended for the integrated circuit. Finally, solder the three connecting wires in place.

Insert the 555 correctly in its socket. Although CMOS devices *can* be damaged by static discharge, they are usually robust enough to withstand normal handling. However, the device should be removed if any soldering "afterwork" is to be done. Also the i.c. should neither be inserted nor removed from its socket whilst the circuit is connected to a power supply.

The circuit may now be added to the car wiring system. Scotchlok connectors are useful at this stage (available from motoring accessory dealers), or spade connectors can be used. It is a good idea to disconnect the car battery whilst wiring up. It is also worthwhile to add an in-line fuse in series with the positive line—the lowest value fuse available will do. Reconnect the battery and operate the car doors to check for correct action.

Two, possibly three 6 watt lamps may be operated with this circuit. If it is required to operate more lamps then a "beefier" transistor must be used in place of TR3, possibly with a heatsink. A BD140 or a PNP 3055 may be used, mounted on a small piece of aluminium, away from the circuit board. The circuit board inself may be mounted in a small box, or bolted to the car metalwork with spacers or brackets, or merely wrapped in stout plastic and wedged in the wiring loom. ★

COMPONENTS . . .

Resistors

R1	1k
R2,3,4,5	1M (4 off)
R6,7,8	10k (3 off)

All resistors ¼W (or ⅓W) 5% carbon film

Capacitors

C1	100µ 25V elect. axial
C2	10n polyester
C3	10µ 25V. tant.
C4*	10n polyester

* Not necessary if IC1 is CMOS

Semiconductors

D1	1N4007
D2	OA202 or similar gen. purpose silicon
IC1	CMOS 555 (sometimes called low power 555)
TR1, 2	ZTX107/8/9 (Ferranti E-line or similar)
TR3	ZTX750/1/2/3 Ferranti E-line only. (Technomatic)

Miscellaneous

P.C.B. or stripboard
8 pin d.i.l. socket
Wire and connectors
In-line fuse holder and fuse at 1 or 2A

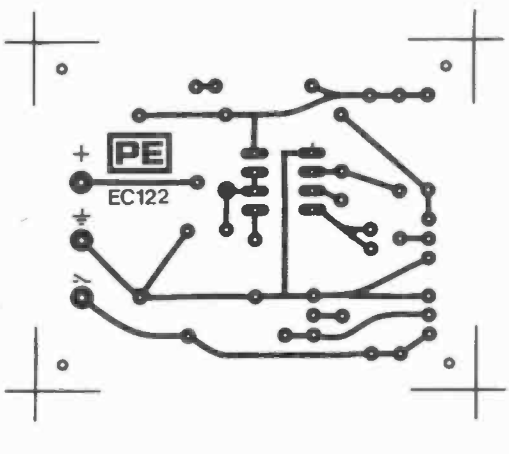


Fig. 2. P.c.b. track layout (actual size)

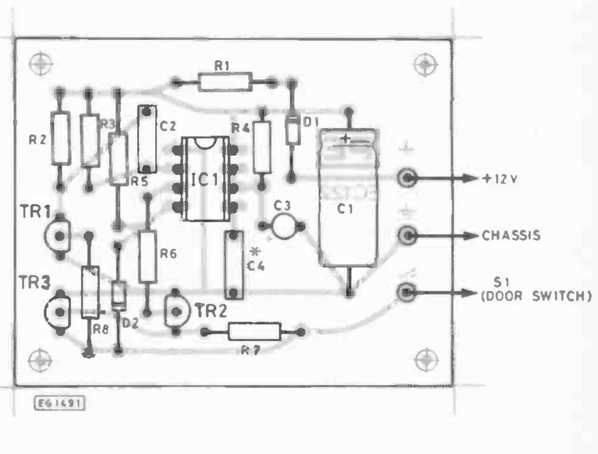


Fig. 3. Component layout

SEMICONDUCTOR CIRCUITS

TOM GASKELL B.A.(Hons)

WINDOW DISCRIMINATOR (TCA 965)

THERE are many instances in electronic circuitry where analogue voltages must be compared with each other. The conventional way to implement this is to use a comparator with a differential input stage. If one of the two inputs is higher in voltage than the other, the output is at a 'high' level, and if the reverse is true, then the output becomes a 'low' level.

In many cases, however, a simple comparison of two voltages is insufficient. We may wish to know if a voltage lies within a certain range, and if not, whether it is above the top limit of that range, or below the bottom limit. The range of voltage in question is known as a 'window', and we look for voltages within the window, or outside it, as appropriate. The voltage range is referred to as the 'width' of the window, and is defined as the difference between the upper voltage limit and the lower voltage limit. This type of circuit arrangement can be implemented by a pair of comparators, with their inputs fed by a common input signal and by voltage references, as appropriate. Logic gates can be used to derive the 'inside window' and 'outside window' signals. Fortunately, Siemens now produce the TCA 965, a 14 pin i.c. which provides a complete window discrimination circuit, including an internal voltage reference.

BASIC OPERATION

Fig. 1 shows the pinout and specification for the device, and Fig. 2 the block diagram. A pair of comparators are used to detect the upper and lower voltage limits of the window. These comparators have a small hysteresis built-in, to help suppress unwanted oscillations. The output of comparator 'A' goes high when the signal fed to its non-inverting input exceeds the upper voltage limit as defined at pin 6. Similarly, the output of comparator 'B' goes high when the signal fed to its inverting input falls below the lower voltage limit as defined at pin 7. A NOR gate is used to combine the two comparator outputs so that if either comparator turns on, the input signal is deemed to be outside the window. The complement of this, derived by an inverter, is that the signal must be inside the window. Either comparator can be inhibited by connecting its inhibit line, pin 4 or pin 12, to 0 volts.

All four logic outputs, pins 2, 3, 13 and 14, are provided as open collector negative logic, or 'active low' outputs, so any load should be connected between the relevant pin and the positive supply rail. Even if the i.c. is driving into high impedance loads, such as logic i.c.s, pullup resistors should be fitted; typically 10k to 100k for CMOS, and 1k for TTL. Because of the negative logic used, logic 0 means that the output is turned On, and logic 1 means that the output is turned Off.

OPERATING MODES

There are actually two window inputs to the comparators, one defining the centre of the window, and the other defining the width of 'Half' the window. The voltage V_h at pin 9 is added to the voltage V_c at pin 8 and fed to comparator B, but is subtracted from V_c before being fed to comparator A; the difference between the voltages fed to the comparators is therefore the full window width. This allows the i.c. to be used in two different modes, as shown in Figs. 3 & 4. The limits mode shown in Fig. 3 is the simpler of the two. Here, the resistive divider R1, R2, and R3 sets the upper and lower window limits at pins 6 and 7. Although R4 and R5 are shown setting a half window width voltage at pin 9, this would only rarely be used in the limits mode, and would normally be set near to 0 volts. Hence, the voltage at pin 8 is directly compared with the voltage at pins 6 and 7. The results of this comparison are presented at pins 2, 3, 13 and 14, as shown.

In the window mode of Fig. 4 we provide the limit conditions in a rather different way. The voltage at pin 8, set by R1 and R2, defines the centre of the voltage window, and the voltage at pin 9, set by R3 and R4, defines the half window width. This mode is especially useful when the window remains constant in width, but needs to be 'tuned' in its position, i.e. its centre voltage. Pins 6 and 7 are commoned and fed with the input signal. Because this input signal is now being fed into the op-

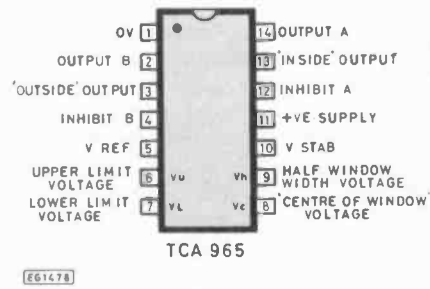


Fig. 1. Pin out with specification below

Characteristic	Notes	Minimum value	Typically	Maximum value	Units
Supply voltage	All spec's measured at +10V	4·75	10	27	V
Quiescent current	Pins 2 and 13 at high level (logic 1)		5	7	mA
Temperature range		−25		85	°C
Input current	Pins 6, 7, 8		20	50	nA
Input current	Pin 9		−0·4	−3	µA
Input current	Pins 4, 12 (inhibit)		−100		µA
Output current	Pins 2, 3, 13, 14			50	mA
Output current	V_{stab} (pin 10)			10	mA
Input voltage range	Pins 6, 7, 8	1·5		(+ve supply −1)	V
Input voltage range	Pin 9	0·05		(+ve supply)/2	V
Input offset voltage	Pins 6 & 8, or pins 7 & 8	−20	±10	+20	mV
V_{ref}	Without load	2·8	3·0	3·2	V
V_{stab}	Supply voltage >7·9V	5·5	6·0	6·5	V
V_{ref} line regulation			3		mV/V
V_{ref} temp. coefficient			0·5		mV/°C
O/P saturation voltage	Pins 2, 3, 13, 14; (current=10mA)			200	mV
O/P reverse current	Pins 2, 3, 13, 14			10	µA
Comparator hysteresis		14	22	30	mV
Inhibit threshold	Pull pins 4 & 12 towards 0V to inhibit		1·5		V

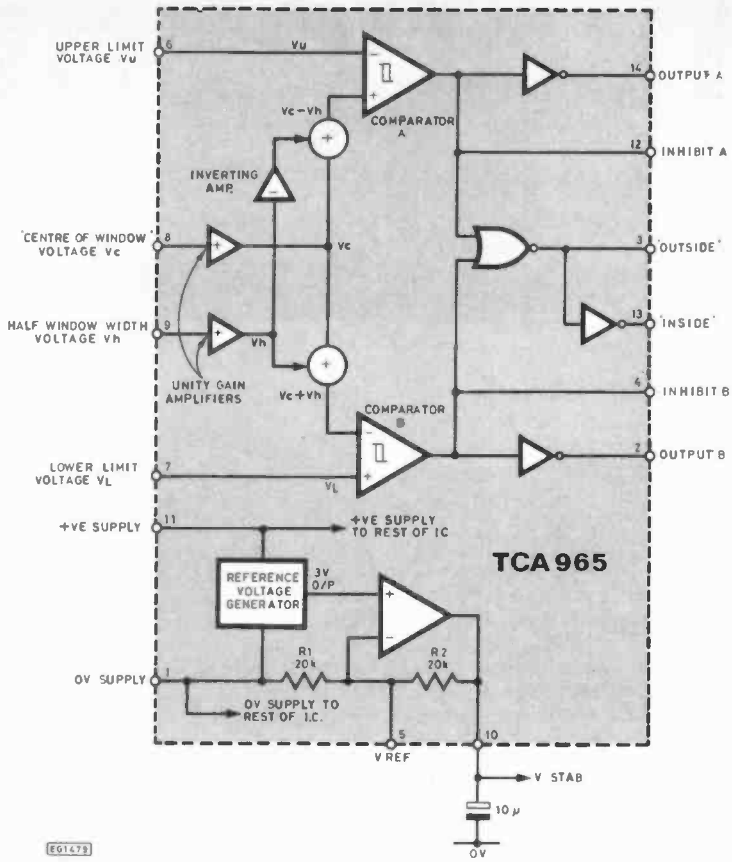


Fig. 2. Block diagram of the TCA 965

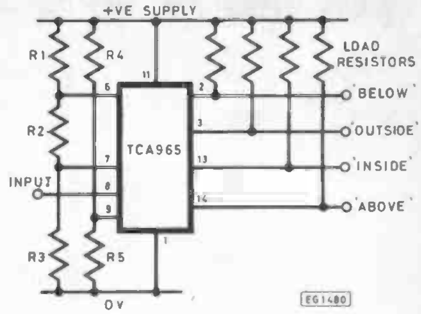


Fig. 3. Basic circuit, limits mode

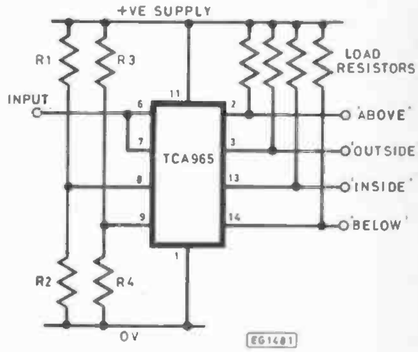


Fig. 4. Basic circuit, window mode

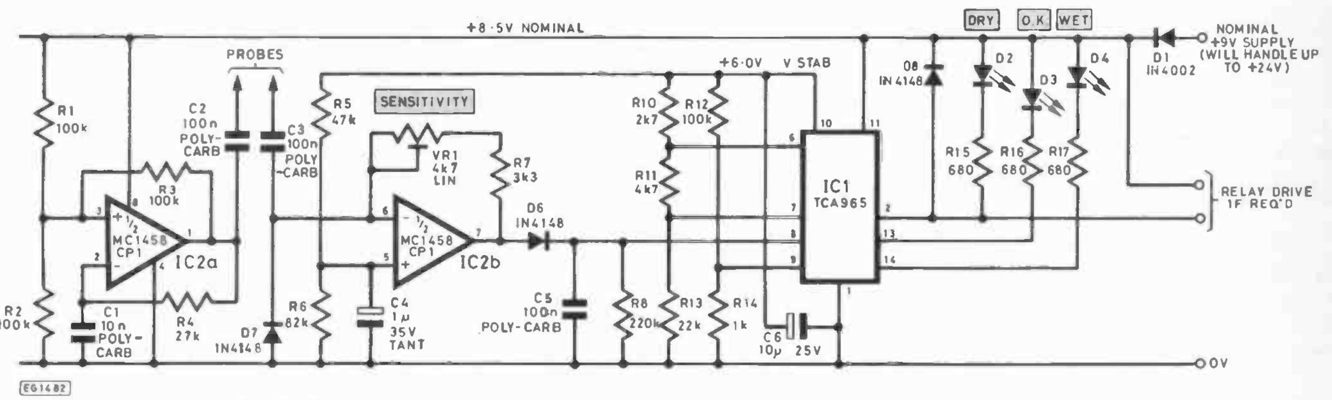


Fig. 5. Circuit diagram of the Plant Watering Meter (N.B. There is no D5 in the circuit)

posite comparator inputs to those used in Fig. 3, the output polarities at pin 2 and pin 14 are reversed; pin 2 is now the 'above' output, and pin 14 is the 'below' output.

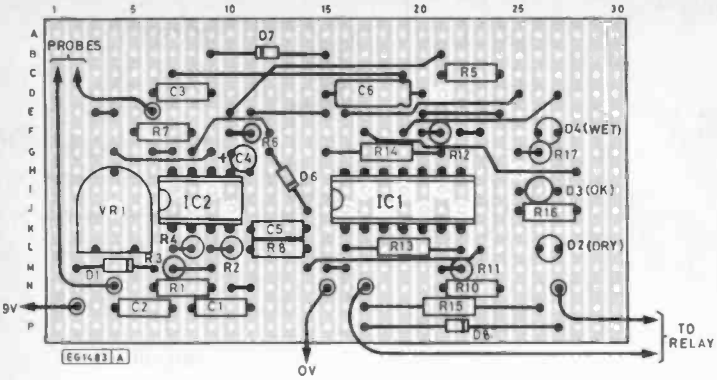
VOLTAGE REFERENCE

Although resistive dividers between the supply rails can be used to set the various limit or window voltages, this is not usually a very accurate arrangement due to the possibility of supply voltage variations, noise, etc. The TCA 965 has an internal reference voltage generator to help overcome these problems. Fig. 2 shows the arrangement of this generator. A 3 volt reference voltage is amplified by a non-inverting amplifier. R1 and R2 set the gain at x2, so the voltage V_{stab} at pin 10 is nominally 6 volts. This voltage can be changed, however, by connecting external resistors between pin 5 and 0 volts, or between pin 5 and pin 10. To stabilise the output voltage, a 10µF electrolytic capacitor must be provided between pin 10 and 0 volts, as close to the i.c. as possible. Up to 10mA is available from this V_{stab} output.

APPLICATIONS

Because of its very flexible internal configuration, this i.c. lends itself well to a whole myriad of applications. It can be run from supplies as low as 4·75 volts, enabling its use within 5 volt logic systems, yet can also handle supplies of up to 27 volts. The main outputs (pins 2, 3, 13 and 14) can each sink up to 50mA current from a load, enabling the direct driving of relays, lamps, l.e.d.s, etc. Be cautious, however, with the input voltage range which the i.c. will work normally with; on pins 6, 7 and 8, this is defined as 1·5V to the positive supply less 1 volt. The upper limit should present no problems, but the 1·5 volt lower one might limit its usefulness in some situations.

The TCA 965 will be an obvious choice in many system control applications. The window can be configured as a 'dead space' between a control turning on and turning off again, and as such the i.c. is ideal for use with temperature control systems, providing a flexible and easily defined hysteresis. The other main area of use is within measurement systems, setting limits of acceptance on incoming d.c. values. For example, coupled to a simple analogue measurement system it could



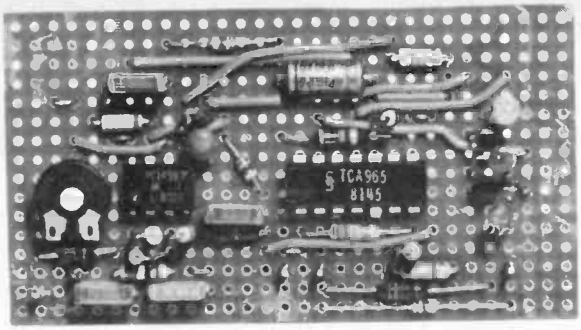


Fig. 6. Veroboard layout

make a limits tester for checking batches of components; components within a certain tolerance of a specified value would be indicated as 'OK', but outside that tolerance would be indicated as 'reject'.

PLANT WATERING METER

To illustrate the basic principles of use of the i.c., Fig. 5 shows a simple plant watering meter, loosely based on the front end of the moisture meter described in *Semiconductor Circuits* last September. IC2a forms a square wave oscillator with a frequency of approximately 2·8kHz. This is a.c. coupled via C2 to one probe, with the other probe in turn feeding into IC2b, which is configured as an inverting amplifier. D6, C5 and R8 provide rectification and smoothing of the received waveform. The TCA 965 is set up in the limits mode as shown in Fig. 3, but using V_{stab} (+6V) as the reference supply for resistive dividers. R10, R11 and R13 provide voltages of approximately +4·5V on pin 7, and +5·5V on pin 6. Pin 9 is biased to only 60mV by R12 and R14, just enough to be inside the specifications shown in Fig. 1. L.e.d.s D2, D3 and D4 show the state of the soil when the probes are pushed in. If required, up to 40mA extra sink current is available from each of the l.e.d. driving outputs to control other transducers, etc. In this case the 'dry' output has been made available to drive an external relay, with D8 protecting against back e.m.f. spikes. This relay could be used to drive a small pump motor, for example, to automatically top-up the plant pot with water. As soon as the soil became wet enough, the pump would turn off again.

Fig. 6 shows the Veroboard layout for this circuit. The probes can be made from stiff copper wire glued inside old ball-point pen cases. The components specified have been deliberately chosen to be very small devices, since the aim was to get the size down as far as possible, so $\frac{1}{8}$ watt resistors, or $\frac{1}{4}$ watt, should be used throughout to be consistent with this. In use, adjust VR1 to give the correct reading for your preferred moisture level, or change R10, R11, and R13 to give an even greater range of possible settings. IC2 is a dual op-amp of the 741 type, so almost any similar device would suffice. Finally, note that diode D1 protects against reverse connection if a battery is being used to supply the current; be extremely careful if a mains-derived supply is to be used, since the proximity of water or moisture could be very dangerous indeed.

Although this is an extremely simple applications circuit, it does demonstrate the great versatility of the TCA 965, which should find considerable use in the field of analogue control and measurement.

The TCA 965 is available from **Electrovalue Ltd, 28 St Jude's Road, Englefield Green, Egham, Surrey.**

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Articles submitted for publication should conform to the usual practices of this Journal, e.g. with regard to abbreviations and circuit symbols. Diagrams should be on separate sheets, not in the text.

FOOLPROOF SWITCH BANK

IU OF THE MONTH

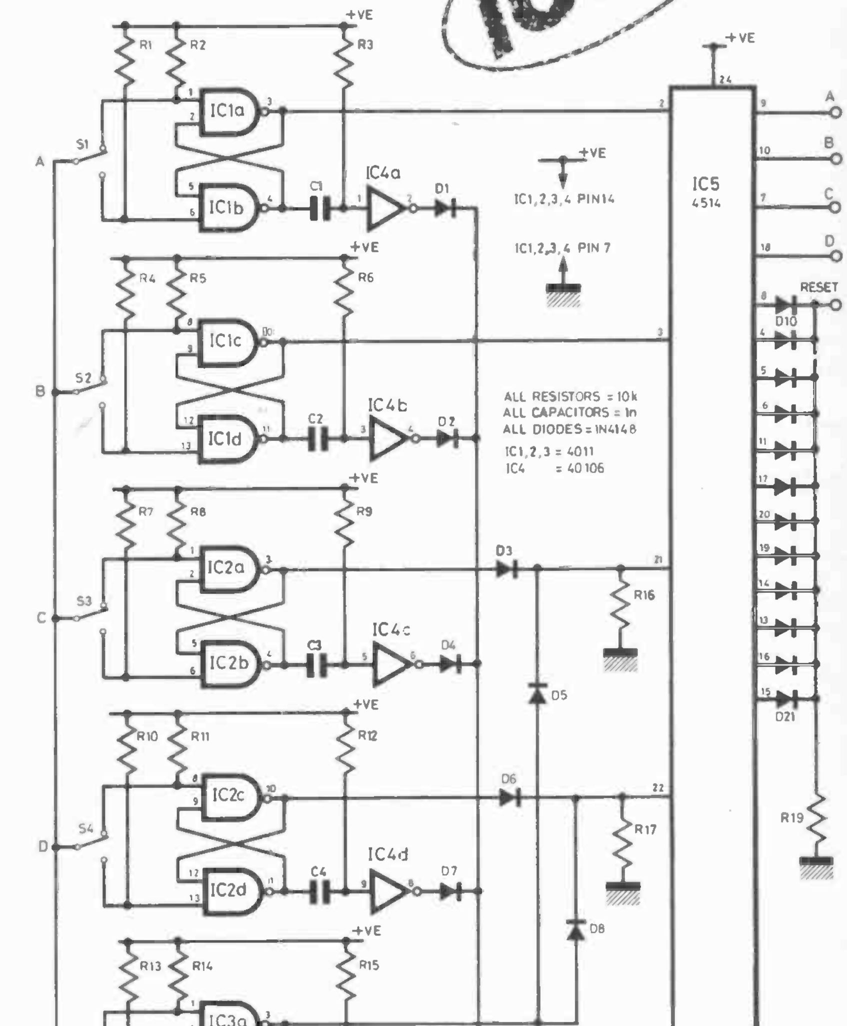
THIS circuit allows four momentary action switches to be used as a push button bank, whereby the last button operated is latched electronically, and if another button is operated, its output supersedes. This of course may be achieved mechanically as indeed it is; however, mechanical switch banks do not guard against more than one switch being operated at the same time. This may prove disastrous in say motor control systems, as if Forward and Reverse were operated simultaneously something would have to give. This circuit is automatically reset if more than one button is operated at the same time. The circuit was originally designed for a logic controlled reel to reel tape deck for the function keyboard, so that say 'play' and 'rewind' pressed at the same time would not result in ten yards of tape on the floor and a pair of smoking motors inside the deck.

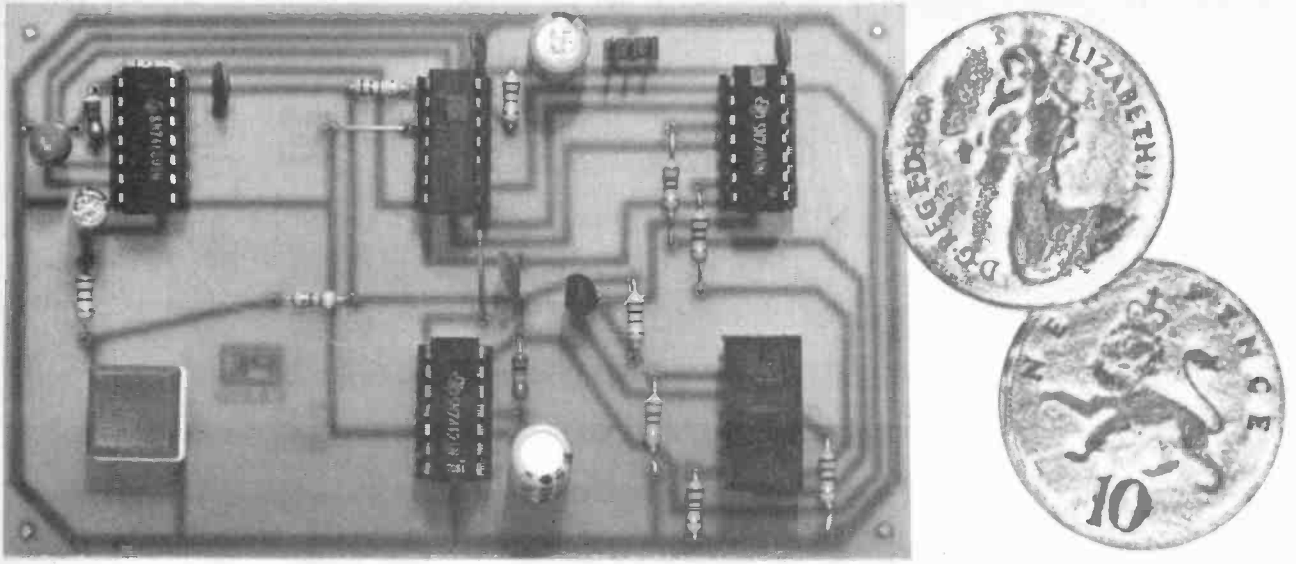
The switches are debounced using S-R latches formed around IC1, 2 and 3. The outputs which are normally high go to a falling edge detector formed around a Schmitt trigger in IC4. The outputs of these are commoned via diodes so as to give a short pulse every time a switch is operated. This strobes the latches.

The outputs of the debouncing latches which are normally low, go to IC5, the heart of the circuit. IC5, a 4514, latches the binary input when strobed, and converts it into a one of sixteen output. As the inputs are connected each to a binary input pin, if one switch is pressed, the appropriate '1', '2', '4' or '8' output latches high. If, however, more than one switch is pressed simultaneously, a binary input other than 1, 2, 4 or 8 is set up at the input, so another output pin goes high. An optional 'reset' output may be built by commoning all the unused outputs via diodes. Also, an optional 'reset' switch may be added as shown by making it form a non single bit number to appear at the input.

Many variations of this circuit may be designed, including the use of more than one 4514 to give more switch capability. It may also be useful to note that if IC5 is substituted for a 4515, the outputs will all be inverted, as this i.c. uses negative output logic.

G. Durant,
Selby,
N. Yorks.





HEADS & TAILS GENERATOR

MICHAEL TOOLEY BA **DAVID WHITFIELD** MA MSc CEng MIEE

SEVERAL popular games rely on the toss of a coin to introduce an element of chance when a simple decision is to be made. Furthermore, the teaching of statistics also invariably involves some reference to the probability of obtaining a 'head' or 'tail' when tossing a coin. Students are usually asked to investigate this by repeatedly throwing a coin and noting the outcome on each occasion. The results of a large number of observations are then collated and the probability of a 'head' or 'tail' is verified as being 0·5, or 1:2. Such an outcome is, of course, independent of a previous result, i.e. if tossing a coin five times produces a 'head' on each occasion, there is still an even chance of producing a 'head' on the sixth throw. Since the outcome of tossing a conventional coin is quite predictable, the teacher of statistics may require a teaching aid in which there are similarly only two outcomes (we will dismiss the possibility that the coin might land on its edge!) but in which the odds can be loaded in favour of one or other of the states.

This month's Digital Project, therefore, is a device which finds applications in both the classroom and home. The Heads and Tails Generator produces an output consisting of a letter 'h' or 't' displayed on a seven segment l.e.d. indicator. A coin toss is initiated from a momentary push-button; as soon as the button is depressed, the display is blanked but returns a few seconds later to display the outcome. The odds may be weighted in favour of either a 'head' or 'tail', or may be set precisely to an even chance.

CIRCUIT DESCRIPTION

The complete circuit of the Heads and Tails Generator is shown in Fig. 1. IC1a acts as a clock oscillator which produces a square wave of near 50% duty cycle. This stage is followed by an inverting buffer, IC1b, and a further inverter, IC1c. Complementary outputs are derived from these latter two stages and fed to D-type bistables, IC2a and IC2b. The clock inputs to the bistables are commoned and fed from the de-bounced switch arrangement formed by IC1d and associated components. This circuit produces a logic 1 on the clock line whenever the switch is depressed. The outputs of the bistable stages, IC2a and IC2b, are fed to the two-input NAND gates, IC3b and IC3a, respectivley. These are used to gate the outputs of the bistables to the display such that the outputs of IC3a and IC3b will only go low when their common input is taken high. Readers should note that it is only necessary to make changes to the state of two of the display segments on the transition from 'h' to 't', and vice versa. The remaining unaffected segments are simply wired permanently 'on'. It is, however, necessary to ensure that the whole display is blanked during the period in which a conventional coin is in the air. This is achieved by means of the monostable, IC4, and series pass transistor TR1. This latter device interrupts the positive supply to the common anodes of the display during the monostable timing period.

CONSTRUCTION

The Heads and Tails Generator is built on a single sided p.c.b. measuring approximately 120x70mm, the copper foil layout of which is shown in Fig. 2. The corresponding component layout on the top surface of the p.c.b. is shown in Fig. 3. Interconnection from the p.c.b. to the 5Vd.c. supply is made via a 0·1" matrix p.c.b. connector, the wiring scheme for which is also shown in Fig. 1.

Components should be assembled on the p.c.b. in the following sequence: d.i.l. sockets, p.c.b. connector, links, resistors, capacitors, switch, transistor, and l.e.d display. Once assembly is complete, the underside of the p.c.b. should be carefully checked for solder splashes, bridges between adjacent tracks, and dry joints. Finally, the i.c.s may be inserted in their respective holders, taking care to ensure the correct orientation of each device. Constructional details of the enclosure have not been given since this will undoubtedly be a matter of preference for the individual constructor. A small ABS case will normally be found to be quite adequate in this respect. Constructional details of a suitable

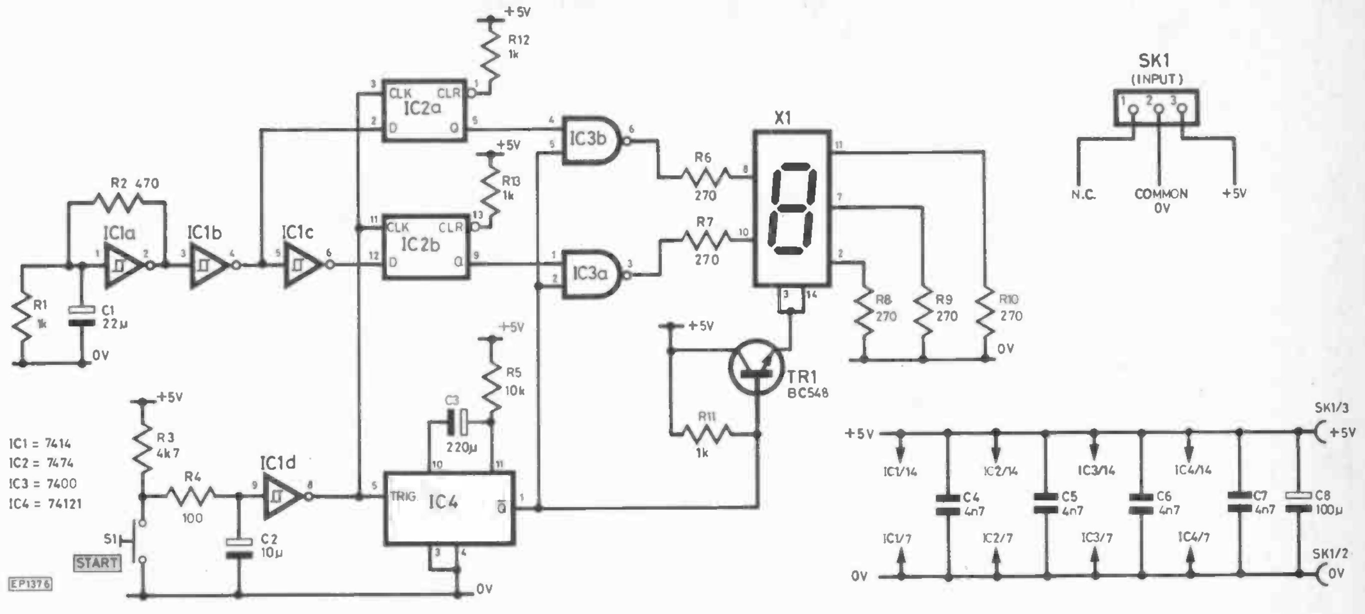


Fig. 1. Circuit diagram of the Heads and Tails Generator

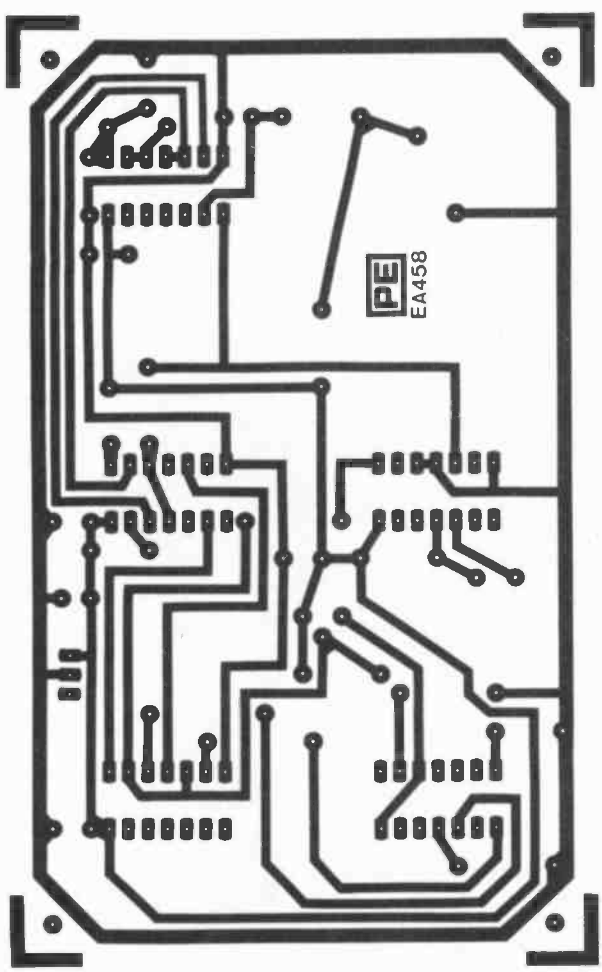


Fig. 2. P.c.b. design

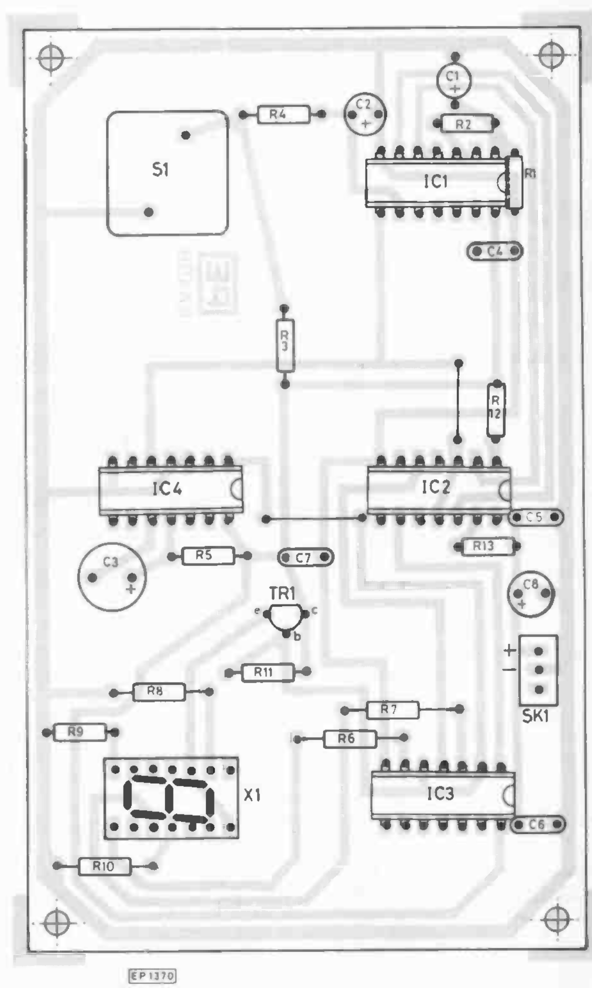


Fig. 3. Component layout

COMPONENTS . . .

Resistors

R1	1k
R2	470
R3	4k7
R4	100
R5	10k
R6-R10	270 (5 off)
R11-R13	1k (3 off)

All resistors are 0·25W 5% carbon

Capacitors

C1	22µ 25V tantalum
C2	10µ 16V p.c. electrolytic
C3	220µ 16V p.c. electrolytic
C4-C7	4n7 ceramic (4 off)
C8	100µ 16V p.c. electrolytic

Semiconductors

TR1	BC548
IC1	7414
IC2	7474
IC3	7400
IC4	74121
X1	Seven segment common anode l.e.d. indicator

Miscellaneous

p.c.b.
Push-to-make p.c.b. mounting switch
14-pin d.i.l. sockets (4 off)
3-way 0·1" p.c.b. plug and socket

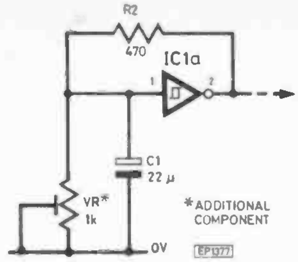


Fig. 4. Modification for changing the odds

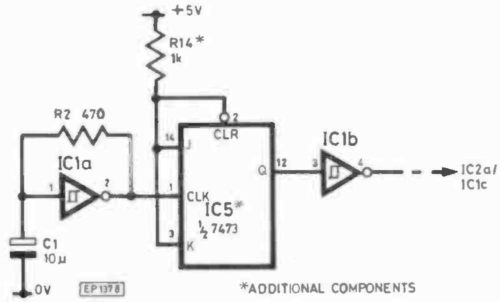


Fig. 5. Modification for a precise evens chance

power supply module were given in the January issue of PE; alternatively, for portable applications, power may be derived from three fresh 1·5V dry cells connected in series. These should be connected to the Heads and Tails Generator via a suitable miniature toggle or slide switch.

CHANGING THE ODDS

The probability of obtaining a 'head' or 'tail' depends primarily upon the mark to space ratio of the square wave produced by the clock oscillator. The odds can thus easily be changed by means of appropriate modifications to the clock oscillator. With the values of R1 and R2 as specified, the mark to space ratio is very nearly 50%. If, however, R1 is made variable, the mark to space ratio can be varied and the odds changed in favour of either 'heads' or 'tails', as desired. The appropriate circuit modification is depicted in Fig. 4.

If, alternatively, a precise evens chance is required, it is only necessary to ensure that the clock waveform is a perfectly symmetrical square wave. This can be accomplished by inserting an extra J–K bistable stage between IC1a and IC1b, as shown in Fig. 5. The bistable produces a symmetrical square wave output regardless of the mark to space ratio of its clock input. It should be noted that, since the output of the bistable is at half the frequency of its clock input, it is necessary to alter the value of C1 if the clock frequency is to remain approximately the same. ★

Patents Review

Copies of British Patents can be obtained from: The Patent Office, Sales, St. Mary Cray, Orpington, Kent (£1.75); and copies of Foreign Patents can be obtained from The Science Reference Library, 25 Southampton Buildings, London, WC2A 1AJ. (Prices on application.)

HI-FI VIDEO SYSTEMS

This year both the VHS and Beta home video manufacturers will be launching hi-fi sound systems. In a conventional helical scan domestic video recorder, the luminance and chrominance vision signals are recorded by rotating video heads and the sound is recorded by a stationary head. Because tape speed is low (one inch per second or less) the sound quality is poor, especially in stereo where the already narrow track must be split into two. In June 1982 Sony announced an alternative approach; using the video heads to record stereo sound as f.m. buried in the video waveform.

The Sony Beta Hi-Fi system has been on sale in NTSC countries, Japan and the USA, since last summer. But Sony has been cagey over exactly how the system works. This is because the Beta Hi-Fi system to be launched in Europe, for PAL and SECAM, will *not* be the same as Beta Hi-Fi in the USA and Japan. In fact Beta Hi-Fi in Europe will be almost exactly the same as the VHS Hi-Fi system. Two extra heads on the rotating drum lay down the f.m. sound carriers a fraction of a second in advance of the video heads. The f.m. sound carrier is of relatively low frequency, consequently it records deep into the magnetic coating of the tape.

The video signal is on a higher frequency f.m. carrier which wipes out and replaces the top layer of the sound carrier. The result is a layered recording, video on top and audio below. The technique is called depth multiplex recording.

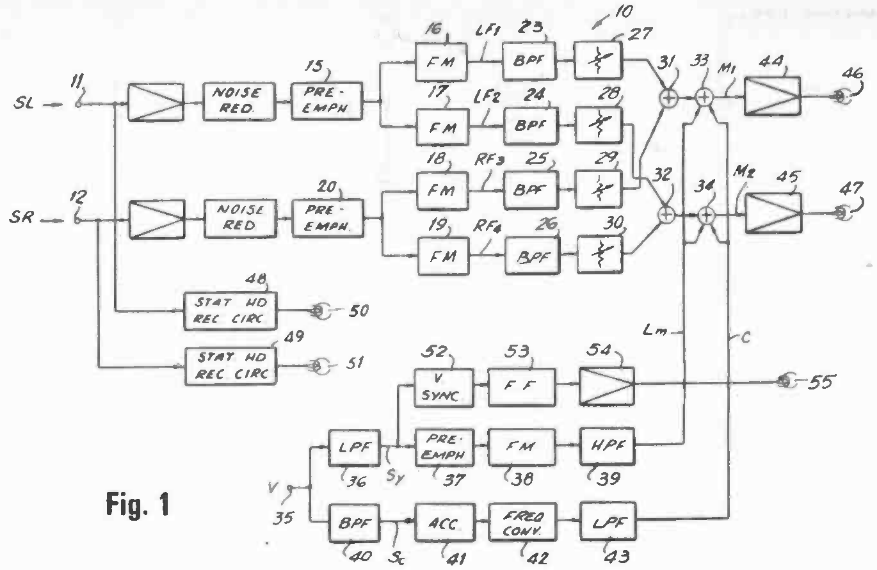


Fig. 1

Recent British patent application 2113894 from Sony explains how the two head Beta Hi-Fi system works and gives a clue to the problems which Sony has found insuperable for Europe.

Fig. 1 shows the schematic circuit. Left channel audio enters at 11, and right channel audio at 12. The right channel frequency modulates a carrier of frequency F1 (1·325MHz) at 16, and simultaneously modulates a second carrier at frequency F2 (1·475MHz) at 17. The right hand channel modulates carrier F3 (1·625MHz) at 18 and carrier F4 (1·775MHz) at 19. One left channel signal (LF1) and one right channel signal (RF3) are combined at 31, mixed with the luminance (LM) and chrominance (C) video signals at 33 and sent to helical scan recording head 46. The other left signal LF2, and the other right signal, RF4, are combined at 32, mixed with chrominance and luminance at 34 and sent to recording head 47. The frequency spectrum is shown in Fig. 2.

Fig. 3 shows the signals sent to video head 46, and Fig. 4 shows the signals sent to video head 47. So the helical tracks across the tape alternately have the spectrum of Fig. 3, then the spectrum of Fig. 4, then the spectrum of Fig. 3 again, and so on. As a result, adjacent tracks do not use the same frequencies. This reduces the problem of crosstalk between the sound carriers of adjacent tracks. Video crosstalk is handled in the usual way, by making two video heads with gaps of different azimuth and altering the video signal phase so that unwanted signals are ignored. The level of the carriers is automatically adjusted before recording, to compensate for the non-linear characteristic of magnetic tape at high frequencies.

The system works, for NTSC recorders in Japan and the USA, because NTSC video needs less bandwidth than European video. So there is room in the spectrum for the four carriers needed. But in Europe there is not enough room in the spectrum. Hence the adoption by both Beta and VHS of systems which rely on extra heads and depth multiplex recording. But why is Sony filing patents in Europe for a system which won't be used in Europe? Probably because when the patents were filed here (December 1982) the company still hoped to make the NTSC system work for PAL and SECAM.

Incidentally, anyone checking application 2113894 in a library, should also look at the patent on the shelf next to it. Number 2113893 was filed by JVC and describes the technology used to reduce the size of the head drum in a portable video recorder and camera combined 'camcorder' while still retaining compatibility with machines of standard drum size. In fact this patent reveals the startling news that JVC is working on a VHS camcorder with video drum *half* the normal size. JVC's prototype camcorder, VHS Video Movie, sneak-previewed at the Berlin Radio Show, uses a head drum two thirds normal size. So a camcorder with half size drum and commensurately smaller mechanics, could be even smaller than VHS Video Movie.

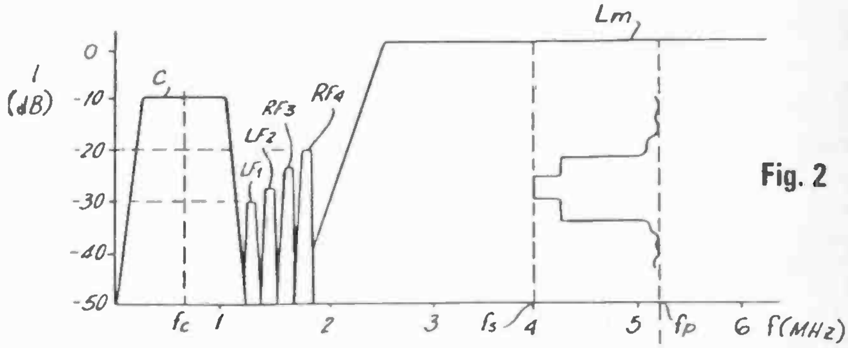


Fig. 2

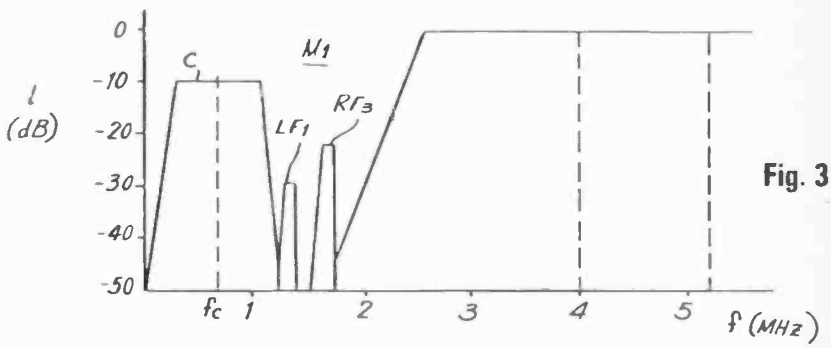


Fig. 3

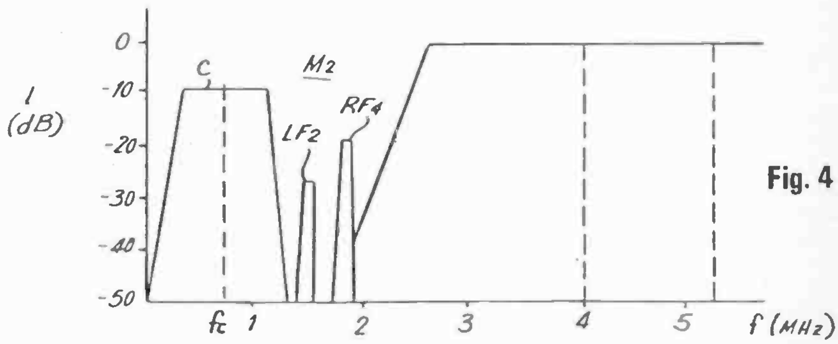


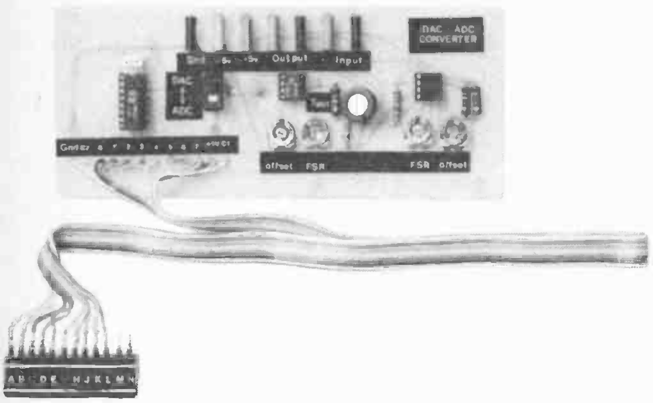
Fig. 4

EXPANDING THE VIC 20

PART SIX

SAM WITHEY

ADC/DAC BOARD . . .



FOR AROUND £8

LAST month we looked at a stepper motor controller. This month we examine the applications and control techniques of stepper motors, and include suitable software. This is followed by a new interface for VIC 20 which allows DAC and ADC.

Apart from robotic applications, where all four motors could be used to control separate functions, yet be used simultaneously, the most likely use will be for control of linear movement or plotting on an X–Y axis.

A single motor has many useful applications including control of length and depth as well as rack and pinion linear positioning. Two motors enable X–Y plotting as well as applications such as for azimuth and elevation control.

Simple BASIC programming is best carried out by the use of subroutines. To start with, a simple forward and reverse step for each motor, with timing accessible from the keyboard. Next a subroutine to be able to step one pair of motors (two if required) diagonally either on a horizontal or a vertical plane. To give three dimensional movement, such as to move from a corner of a cube towards the centre, three motors need to be stepped simultaneously. These three motors would normally work in association with each other, in pairs, or on their own. Then there is the fourth motor, which might work simultaneously with, yet independent of, the others. The four motors can be controlled independently in 8 subroutines and X–Y movement of two motors in another four. This is sufficient to get moving.

First we'll try a short program to make one motor step CCW, then CW.

SDB 520 CONTROLLER

Let P0 control Motor 1 CCW and P1 control it CW. P2 and P3 would control Motor 2 similarly. Finally P4 and P5 to Motor 3 and P6 and P7 to Motor 4.

SAA 1027 CONTROLLER

Let P0 pulse Motor 1 and P1 logic "0" step it CCW, P1 logic "1" to step it CW. Because of the opto-isolator, the logic for direction is the reverse of that expected, as stated in the manufacturer's specifications. The change of logic does not affect the pulse. Pair off P2/P3 to Motor 2, etc.

Write subroutines for stepping CCW and CW.

SDB 520

```
200 POKE 37136,1:REM Set I/O for pulse to IC1 pin 1
    (CCW)
201 POKE 37136,0:REM Negative going pulse
202 FOR I=1 TO 200:NEXT:RETURN:REM Set speed
300 POKE 37136,2:REM Set I/O for pulse to IC1 pin 2 (CW)
301 POKE 37136,0:REM Negative going pulse
302 FOR I=1 TO 200:NEXT:RETURN
```

SAA 1027

```
200 POKE 37136,1:REM Set I/O for pulse to IC1 pin 15
    (Pulse)
201 POKE 37136,0:REM Step CCW (See note on reversed
    logic)
202 FOR I=1 TO 200:NEXT:RETURN
300 POKE 37136,3:REM Set I/O for pulse to IC1 pins 15
    and 3
301 POKE 37136,0:REM Step CW
302 FOR I=1 TO 200:NEXT:RETURN
```

EITHER CONTROLLER

```
10 POKE 37138,255:REM Set DDR for all ports as outputs
20 GOSUB200:GOSUB200:GOSUB200:GOSUB200:REM
   Step CCW 4 steps
25 FOR I=1 TO 800:NEXT:REM Delay before changing
   direction
30 GOSUB300:GOSUB300:GOSUB300:GOSUB300:REM
   Step CW 4 steps
35 FOR I=1 TO 800:NEXT
40 GOTO20:REM Loop until stopped from keyboard
```

Having already written subroutines for stepping Motor 1 CCW and CW, we now do the same for Motor 2.

SDB 520

```
400 POKE 37136,4:REM Set I/O for pulse to IC2 pin 1
    (CCW)
401 POKE 37136,0:REM Negative going pulse
402 FOR I=1 TO 200:NEXT:RETURN:REM Set speed
500 POKE 37136,8:REM Set I/O for pulse to IC2 pin 2 (CW)
501 POKE 37136,0:REM Negative going pulse
502 FOR I=1 TO 200:NEXT:RETURN
```

SAA 1027

```
400 POKE 37136,4:REM Set I/O for pulse to IC2 pin 15
    (Pulse)
401 POKE 37136,0:REM Step CCW (See note on reversed
    logic)
402 FOR I=1 TO 200:NEXT:RETURN
500 POKE 37136,12:REM Set I/O for pulse to IC2 pins 15
    and 3
501 POKE 37136,0:REM Step CW
502 FOR I=1 TO 200:NEXT:RETURN
```

The next stage is to program motors 1 and 2 to provide an X–Y plot movement.

SDB 520

```
600 POKE 37136,5:REM Motors 1 & 2 CCW Binary
    00000101
601 POKE 37136,0
602 FOR I=1 TO 200:NEXT:RETURN
605 POKE 37136,10:REM Motors 1 & 2 CW Binary
    00001010
606 POKE 37136,0
607 FOR I=1 TO 200:NEXT:RETURN
610 POKE 37136,9:REM M1 CCW M2 CW Binary
    00001001
611 POKE 37136,0
612 FOR I=1 TO 200:NEXT:RETURN
615 POKE 37136,6:REM M1 CW M2 CCW Binary
    00000110
616 POKE 37136,0
617 FOR I=1 TO 200:NEXT:RETURN
```

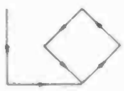
SAA 1027

```
600 POKE 37136,5:REM Motors 1 & 2 CCW Binary
    00000101
601 POKE 37136,0
602 FOR I=1 TO 200:NEXT:RETURN
605 POKE 37136,15:REM Motors 1 & 2 CW Binary
    00001111
606 POKE 37136,0
607 FOR I=1 TO 200:NEXT:RETURN
610 POKE 37136,13:REM M1 CCW M2 CW Binary
    00001101
611 POKE 37136,0
612 FOR I=1 TO 200:NEXT:RETURN
615 POKE 37136,7:REM M1 CW M2 CCW Binary
    00000111
616 POKE 37136,0
617 FOR I=1 TO 200:NEXT:RETURN
```

We'll try some X–Y movements. Motor 1 moves plotter vertical. Motor 2 moves plotter horizontal.

EITHER CONTROLLER

```
10 POKE 37138,255:REM Set DDR for output at all ports
20 GOSUB300:GOSUB300:GOSUB300:GOSUB300 Start
30 GOSUB500:GOSUB500:GOSUB500:GOSUB500
40 GOSUB610:GOSUB610:GOSUB610:GOSUB610
50 GOSUB600:GOSUB600:GOSUB600:GOSUB600
60 GOSUB615:GOSUB615:GOSUB615:GOSUB615
70 GOSUB605:GOSUB605:GOSUB605:GOSUB605
80 END
```



For users of Z80 based computers the method of programming is similar to that for the l.e.d.s simulator. Stepping movement values are the same as for those used with the VIC 20, but are placed in the A register in Hex form. In summary, these are as follows:

SDB 520

Motor 1 CCW 01H CW 02H
Motor 2 CCW 04H CW 08H
Motors 1 & 2 CCW 05H CW 0AH
Motor 1 CCW Motor 2 CW 09H
Motor 1 CW Motor 2 CCW 06H

SAA 1027

Motor 1 CCW 01H CW 03H
Motor 2 CCW 04H CW 0CH
Motors 1 & 2 CCW 05H CW 0FH
Motor 1 CCW Motor 2 CW 0DH
Motor 1 CW Motor 2 CCW 07H

Again, the delay is put at the beginning of the program to enable easy introduction of stepping sequences and is placed at 1000H to allow relocation. No system monitor routines are included, so the program should work on any Z80 computer without further modification.

An X–Y program similar to that for the VIC 20 could take a similar form.

```
1000           0010          ORG    £1000;X–Y Plot Routine
1000 0640      0020 DELAY    LD,    B£40;Set up delay count
1002 08        0030 DELY1    EX     AF,AF'
1003 AF        0040          XOR    A;Set A to zero to start
1004 F5        0050 DELY2    PUSH   AF;Loop 256 times
1005 F1        0060          POP    AF;Recall contents of A
1006 F5        0070          PUSH   AF;Repeat last 2 steps
1007 F1        0080          POP    AF
1008 3D        0090          DEC    A;Decrement A register
1009 20F9      0100          JR     NZ,DELY2;Repeat until
                                    A is zero
100B 00        0110          NOP
100C 10F4      0120          DJNZ   DELY1;Repeat until
                                    count is zero
100E C9        0130          RET;   Return to program
100F 00        0140          NOP
```

SDB 520

```
1010 3E01      0150 M1CCW    LD     A,£01;Motor 1 CCW
1012 D304      0160          OUT    (£04),A;Output through
                                    PIO
1014 3E00      0170          LD     A,£00;Clear A to
                                    complete
1016 D304      0180          OUT    (£04),A;pulse shape
1018 C9        0190          RET
1019 00        0200          NOP
101A 3E02      0210 M1CW     LD     A,£02;Motor 1 CW
101C D304      0220          OUT    (£04),A
101E 3E00      0230          LD     A,£00
1020 D304      0240          OUT    (£04),A
1022 C9        0250          RET
1023 00        0260          NOP
1024 3E04      0270 M2CCW    LD     A,£04;Motor 2 CCW
1026 D304      0280          OUT    (£04),A;Output through
                                    PIO
1028 3E00      0290          LD     A,£00;Clear A to
                                    complete
102A D304      0300          OUT    (£04),A;pulse shape
102C C9        0310          RET
102D 00        0320          NOP
102E 3E08      0330 M2CW     LD     A,£08;Motor 2 CW
1030 D304      0340          OUT    (£04),A
1032 3E00      0350          LD     A,£00
1034 D304      0360          OUT    (£04),A
1036 C9        0370          RET
1037 00        0380          NOP
```

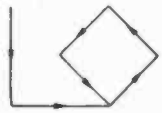
```
1038 3E05  0390 1/2CCW   LD    A,£05;Motors 1/2 CCW
103A D304  0400          OUT   (£04),A;Output through
                               PIO
103C 3E00  0410          LD    A,£00;Clear A to
                               complete
103E D304  0420          OUT   (£04),A;pulse shape
1040 C9    0430          RET
1041 00    0440          NOP
1042 3E0A  0450 1/2CW    LD    A,£0A;Motors 1/2 CW
1044 D304  0460          OUT   (£04),A
1046 3E00  0470          LD    A,£00
1048 D304  0480          OUT   (£04),A
104A C9    0490          RET
104B 00    0500          NOP
104C 3E09  0510 CCWCW    LD    A,£09;Motor 1 CCW
                               Motor 2 CW
104E D304  0520          OUT   (£04),A:Output through
                               PIO
1050 3E00  0530          LD    A,£00;Clear A to
                               complete
1052 D304  0540          OUT   (£04),A;pulse shape
1054 C9    0550          RET
1055 00    0560          NOP
1056 3E06  0570 CWCCW    LD    A,£06;Motor 1 CW
                               Motor 2 CCW
1058 D304  0580          OUT   (£04),A
105A 3E00  0590          LD    A,£00
105C D304  0600          OUT   (£04),A
105E C9    0610          RET
105F 00    0620          NOP
```

SAA 1027

```
1010 3E01  0150 M1CCW    LD    A,£01;Motor 1 CCW
1012 D304  0160          OUT   (£04),A;Output through
                               PIO
1014 3E00  0170          LD    A,£00;Clear A to
                               complete
1016 D304  0180          OUT   (£04),A;pulse shape
1018 C9    0190          RET
1019 00    0200          NOP
101A 3E03  0210 M1CW     LD    A,£03;Motor 1 CW
101C D304  0220          OUT   (£04),A
101E 3E00  0230          LD    A,£00
1020 D304  0240          OUT   (£04),A
1022 C9    0250          RET
1023 00    0260          NOP
1024 3E04  0270 M2CCW    LD    A,£04;Motor 2 CCW
1026 D304  0280          OUT   (£04),A;Output through
                               PIO
1028 3E00  0290          LD    A,£00;Clear A to
                               complete
102A D304  0300          OUT   (£04),A;pulse shape
102C C9    0310          RET
102D 00    0320          NOP
102E 3E0C  0330 M2CW     LD    A,£0C;Motor 2 CW
1030 D304  0340          OUT   (£04),A
1032 3E00  0350          LD    A,£00
1034 D304  0360          OUT   (£04),A
1036 C9    0370          RET
1037 00    0380          NOP
1038 3E05  0390 1/2CCW   LD    A,£05;Motors 1/2 CCW
103A D304  0400          OUT   (£04),A;Output through
                               PIO
103C 3E00  0410          LD    A,£00;Clear A to
                               complete
103E D304  0420          OUT   (£04),A;pulse shape
1040 C9    0430          RET
1041 00    0440          NOP
1042 3E0F  0450 1/2CW    LD    A,£0F;Motors 1/2 CW
1044 D304  0460          OUT   (£04),A
1046 3E00  0470          LD    A,£00
1048 D304  0480          OUT   (£04),A
104A C9    0490          RET
104B 00    0500          NOP
104C 3E0D  0510 CCWCW    LD    A,£0D;Motor 1 CCW
                               Motor 2 CW
104E D304  0520          OUT   (£04),A;Output through
                               PIO
1050 3E00  0530          LD    A,£00;Clear A to
                               complete
1052 D304  0540          OUT   (£04),A;pulse shape
1054 C9    0550          RET
1055 00    0560          NOP
1056 3E07  0570 CWCCW    LD    A,£07;Motor 1 CW
                               Motor 2 CCW
1058 D304  0580          OUT   (£04),A
105A 3E00  0590          LD    A,£00
105C D304  0600          OUT   (£04),A
105E C9    0610          RET
105F 00    0620          NOP
```

EITHER CONTROLLER

```
1100 3E0F    0630 START  LD    A,0F;Set up Port A
1102 D306    0640        OUT   (06),A;all lines as
                               outputs
1104 CD1A10  0650        CALL  M1CW
1107 CD0010  0660        CALL  DELAY
110A CD2E10  0670        CALL  M2CW
110D CD0010  0680        CALL  DELAY
1110 CD4C10  0690        CALL  CCWCW
1113 CD0010  0700        CALL  DELAY
1116 CD3810  0710        CALL  1/2CCW
1119 CD0010  0720        CALL  DELAY
111C CD5610  0730        CALL  CWCCW
111F CD0010  0740        CALL  DELAY
1122 CD4210  0750        CALL  1/2CW
1125 00      0760        NOP
```



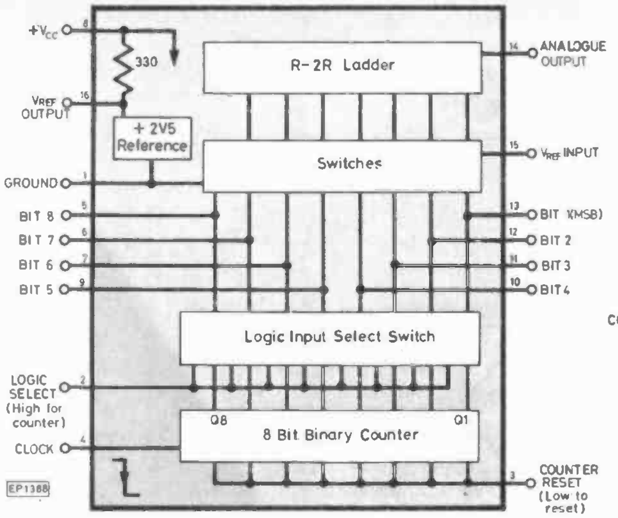
The start can be moved back to Memory Location 1060 if space is at a premium. The SAA 1027 is being advertised currently at around £5·50, but it should be possible to better this price with careful shopping.

ADC/DAC CONVERTERS

In any electronic system, two basic kinds of signals are generated or measured. These are analogue or digital signals. Analogue signals exist as a continuous range of values, whereas digital signals are only apparent when a predetermined threshold level is reached. Typical examples of analogue signals are the varying speed of a motor, the varying intensity of a light source and the changing temperature of an oven. Each of these, being an analogue variable, are able to assume an infinite number of intermediate values between zero and maximum. On the other hand, a binary signal is a digital signal, which assumes one of two states. Either "on", logic 1, or "off", logic 0.

In this part of the series we explain briefly the principles of digital to analogue conversion (DAC) and analogue to digital conversion (ADC) and describe the construction of a low priced board which performs both functions, whilst using the minimum of components. The heart of the system is the Ferranti ZN425E 8 bit D-to-A/A-to-D Converter i.c.

In DAC and ADC applications, two important factors arise, resolution and speed, and these generally relate to the cost of the system. Converters are normally designed as 4 bit, with 16 stages of resolution; 8 bit, with 256 stages of resolution and 16 bit, with 65536 stages of resolution. With 16 bit systems, problems regarding stability are encountered, which leads to complexity of circuit design and a corresponding increase in cost. There are many low priced separate 8 bit DACs and ADCs on the market, including some in the Ferranti range. However, the ZN425E is an easy i.c. to use. It makes an ideal compromise with regard to resolution and though a little slow for some practical purposes, serves to illustrate the functions of D/A and A/D conversion with little outlay.



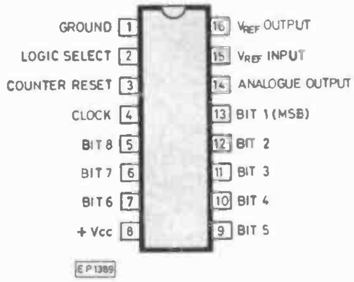


Fig. 6.1. The ZN425E ADC/DAC

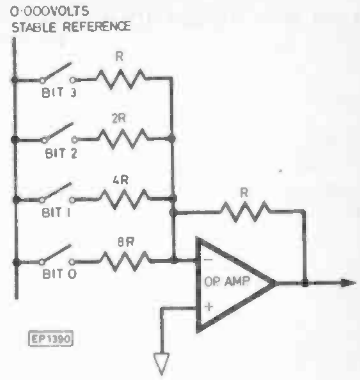


Fig. 6.2. DAC using binary weighted resistors and a current summing amplifier

THE ZN425E 8 BIT D TO A/A TO D CONVERTER

The ZN425E is an 8-bit dual mode analogue/digital, digital to analogue converter. It contains an 8 bit D-to-A converter, using an advance design of R–2R ladder network and an array of precision bipolar switches, which results in full 8 bit accuracy. The inclusion of an 8 bit binary counter on the chip and the addition of an external camparator enables analogue to digital conversion. A logic input select switch is incorporated, which determines whether the precision switches accept the outputs from the binary counter or external inputs, depending upon whether the control signal is respectively high or low. Use of the on-chip 2·5V precision voltage reference is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted. The ZN425E gives an analogue voltage output directly from pin 14, therefore the usual current to voltage converting amplifier is not required. A buffer amplifier is necessary, however, in order to remove the offset voltage and to calibrate the converter.

The problem of converting a binary number into an analogue voltage is solved by the following simple solution: a voltage is generated for each bit position of the binary number, the value of this voltage being proportional to the binary weighting of the bit. For example, bit 0 will generate a voltage V(2x0); bit 1 will generate a voltage 2V(2x1); bit 2, a voltage 4V(2x2) and bit 'n' a voltage 2nxV. The resulting voltages are added and the result is proportional to the original binary number. This is simply illustrated in Fig. 6.2. The D/A consists of 4 switches, 4 summing resistors in the proportion 1,2,4,8, an operational amplifier and a proportional feedback resistor. Resulting in gains of: −1/8, −1/4, −1/2, and −1. With the switches in the open position, there is no input to the operational amplifier, therefore the output will be 0V. The operational amplifier is in inverting and adding mode. Closing bit '0' switch results in the formula $-V\frac{Rf}{8R}$ being applied $=\frac{1}{8}$V. By closing bit switch '1' a gain of −1/4V is added at the output. And so on. The 4 bit binary number represented by the 4 switches is converted into a voltage, which is the analogue representation of one of the 16 possible digital values that can be derived from this circuit.

In practical applications, a precision R − 2R ladder network and fixed reference voltage is employed, switching being carried out by f.e.t. transistors. A typical arrangement of an R − 2R network is depicted in Fig. 6.3. If a bit is set to logic '1', its associated f.e.t. switch is closed, connecting VRef into the R − 2R network. It is clear from the previous example that in an 8 bit Digital to Analogue converter, Data Bit 7 would provide a greater contribution to the analogue output when set, than Bit 0. As the number increases, its contribution to the output is double that of the previous bit, the ladder being binary weighted. In an 8 bit converter, Bit 7 is weighted at 1/2, whilst Bit 0 is weighted at 1/256. Note, that whilst there are 256 stages of resolution in an 8 bit converter, this only realises 255/256VRef when all bits are set. As opposed to the circuits used in Figs. 6.2 and 6.3 to illustrate the operation of DACs, the ZN425E is a *unipolar* device, assuming all inputs to be positive and its output is always a positive value.

The conversion of an analogue signal into a digital quantity is always a sampling process, the instantaneous value of an analogue signal being read and stored as a binary number at different instances of time. In the circuit which is to be described later, the output port of the computer is connected to the DAC's inputs, the output from which is fed into a comparator. The analogue signal to be converted is fed into the other input of the comparator, whose output is fed back into an input port of the computer. The digital value from the computer is then scanned until a comparison occurs between the analogue input signal and the output from the DAC. The digital value at the output from the computer then represents the analogue input signal to the comparator at that instant of time. There are several methods of arriving at this value and we will discuss some of them in the following paragraphs.

SINGLE RAMP OR STEPWISE CONVERSION

This technique uses an upwards count whose final value is controlled by the comparator output. The conversion starts at zero and the count is incremented until the output from the DAC compares with the value of the analogue input to the comparator. This causes the comparator output to switch to logic 0, which in turn inhibits the counter. The digital value now existing on the input to the DAC represents the analogue voltage at the input to the comparator. This can be converted from a digital value into an analogue value displayed on the screen by the writing of a short software routine. The disadvantage of this method is that whilst a near zero signal can be rapidly compared and converted, a full scale input requires 256 iterations.

THE TRACKING CONVERTER

In a tracking type ADC, the up-count is replaced by an up/down count. The condition of the comparator output dictates the direction of the count so that the DAC output can track the analogue input. The starting point for each conversion is the end point of the previous conversion. Obviously, the success or failure of this type of conversion depends on the frequency of value changes and the differential values of the changes.

CONVERSION BY SUCCESSIVE APPROXIMATION

The successive approximation technique of A/D conversion is probably the one most frequently used with microprocessors, as it is characterised by high speed, high resolution and low cost. This method of conversion, whilst being based upon trial and error principles, ensures a result in a finite number of steps. It involves making a preliminary guess at the analogue value and then, from the result of that guess, making a series of intelligent guesses, each based upon the previous result until a final conversion value is reached. In practice, for an 8 bit DAC, the number of iterations is always 8. The preliminary value sampled is always half the full scale for the converter or Bit 7 of the computer output port. The comparator output then indicates whether the input analogue signal is greater than or less than half the full scale value. If it is more than half full scale value a further quarter scale value or Bit 6 of the computer output port is added to make three quarters full scale. If it is less than half full scale value, Bit 7 is removed and is substituted by Bit 6, or half of half full scale value. By successive addition or subtraction of half the previous set value, a new test value is produced. This method requires 'N' iterations where 'N' is the computer word size or the DAC word size. As stated earlier, in our case 8 iterations are needed to find the final value. The convert time is therefore independent of the size of the analogue quantity to be converted. In the event of the analogue value being in excess of the full scale value of the converter, the conversion stops at the full scale value.

EXAMPLE OF 8 BIT SUCCESSIVE APPROXIMATION

Initial Value > (1) < (2) > (3)
(1) 10000000 (2) 11000000 (3) 10100000 (4) 10110000
< (4) > (5) > (6) < (7)
(5) 10101000 (6) 10101100 (7) 10101110 (8) 10101101

The result is 173/256 of the full scale value of the signal. If the full scale value of the input signal is expected to be 5 volts, this would be displayed on the screen through a software routine as 3·37890625 volts.

Whichever method of sampling is used, programming for ADC is carried out by putting an analogue signal into the non-inverting input of the comparator and another signal from the DAC into the inverting input of the comparator. On the signals becoming of equal value, the output of the comparator becomes 0 volts. The computer looks for this signal and on it being present, should stop the sampling from the DAC. The state of the DAC output at that stage indicates the value of the analogue signal input to the comparator. The direct output from the DAC via switch 1 with all bits set (255) is approximately 2·53 volts and near enough to FSR (2·56V)—1LSB. With bit 7 set (128), the output is 1·28 volts etc. This makes a useful starting point. Should the FSR of the comparator also be adjusted to 2·53 volts, this makes initial experiments fairly easy. Using 4·5 volt batteries to power the board, the output from the 741 is approx. 3·8 volts and provision is made for linking this to the comparator by making a small underside link on the board from the base pad of Transistor 1, to the small pad provided. Also, of course, the switch can be left out and the output from the converter connected directly to both op-amp and comparator.

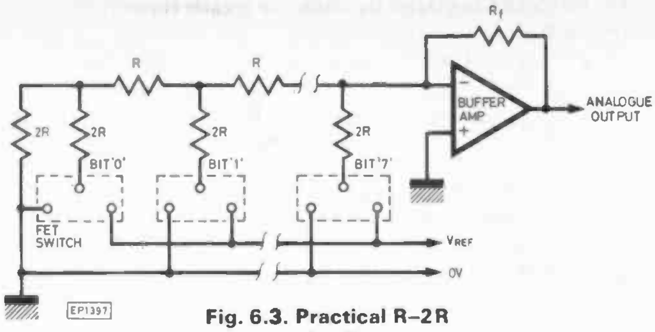


Fig. 6.3. Practical R–2R circuit

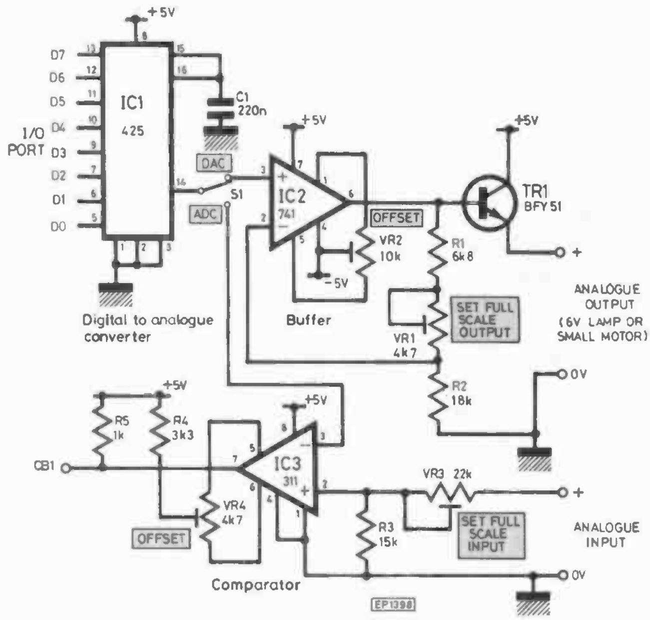


Fig. 6.4. Full circuit diagram

If CB1 Control—Bit 4 of the Peripheral Control Register (PCR) (37148) is used to input the output of the comparator into the computer, Bit 4 is set to logic "0". The CB1 interrupt flag will then be set by a negative transition on the CB1 line. (The line goes from a logic High to a logic Low.) The PCR cannot be read directly. It is designed to set a flag (Bit 4 for CB1) in the Interrupt Flag Register (IFR) (37149) when a transition occurs in the CB1 line. Once the CB1 flag is set, it will stay set until cleared by a POKE to PORT B, which resets the CB1 flag bit.

Initial experiments should be carried out by following these lines:
Set DDR with all lines as outputs, POKE 37138,255
Input a small, known, analogue value
INPUT values into I/O register
Set PCR—Bit 4, POKE 37148
If the IFR is set by a transition, PEEK(37149)
PRINT message on screen
Clear I/O register, POKE 37136,0
Restart sampling.

The following listing is suitable for running the DAC from the keyboard with very quick response.

```
01 PRINT"Shift/ClrHome":REM Clear screen
02 PRINT"To start the DAC function you must"
03 PRINT"enter a value 0 to 255 in the I/O register":
   PRINT:PRINT
04 PRINT"Typing in a new value changes the status of the
   port":PRINT:PRINT
```

```
05 PRINT"The greater the value the greater the output"
08 FOR I=1 TO 10000:NEXT
09 PRINT"Shift/ClrHome":REM Clear screen
10 POKE 37138,255:REM Set DDR to required state
15 PRINT"DDR SET WITH ALL PORTS FOR OUTPUT"
16 PRINT PEEK(37138):REM Display DDR setting
17 PRINT:PRINT:REM Spaces
19 PRINT"TO STAR DAC OUTPUT:"
20 PRINT"SET I/O REGISTER WITH A VALUE 0 TO
   255"
30 INPUT X:REM To put a decimal value in I/O Register
35 IF X<0 OR X>255 GOTO 20:REM Must be 0 to 255 in-
   clusive
40 POKE 37136,X:REM Enter decimal value
42 PRINT:PRINT
45 PRINT"INITIAL STATE OF PORT"
50 Z=X:REM Put value in X into Z
55 GOSUB 200:REM Go to decimal to binary conversion
   routine
60 PRINT"CHANGE OUTPUT VALUE?":PRINT:PRINT
65 INPUT Y:REM Enter decimal value
70 IF Y<0 OR Y>255 GOTO 60
72 Z=Y:REM Put value of Y into Z
75 GOSUB 200
90 POKE 37136,Y
95 PRINT:PRINT:PRINT:PRINT
100 PRINT"VALUE SENT TO I/O REGISTER"
105 PRINT PEEK(37136):REM Display it:PRINT:PRINT
110 PRINT"STATE OF PORTS"
120 PRINT"P7 P6 P5 P4 P3 P2 P1 P0":Z=Y
130 GOSUB 200:REM Go to Decimal to Binary conversion
    routine
140 GOTO 60:REM To reset I/O Registers
200 P0=Z—INT (Z/2) *2:REM Decimal to Binary conversion
205 Z=INT (Z/2)
210 P1=Z—INT (Z/2) *2
215 Z=INT (Z/2)
220 P2=Z—INT (Z/2) *2
225 Z=INT (Z/2)
230 P3=Z—INT (Z/2) *2
235 Z=INT (Z/2)
240 P4=Z—INT (Z/2) *2
245 Z=INT (Z/2)
250 P5=Z—INT (Z/2) *2
255 Z=INT (Z/2)
260 P6=Z—INT (Z/2) *2
265 Z=INT (Z/2)
270 P7=Z—INT (Z/2) *2
275 Z=INT (Z/2)
200 PRINT P7;P6;P5;P4;P3;P2;P1;P0:REM Display ports in
    Binary
205 PRINT:PRINT
210 RETURN:REM Return to line 140 in program
```

CIRCUIT DESCRIPTION AND CONSTRUCTION

The circuit is a combined DAC and ADC using the Ferranti ZN425E 8 Bit converter i.c. When used in DAC mode, a 741 operational amplifier is used as a buffer in order to adjust offset voltage and calibrate Full Scale Reading. These functions are carried out by way of VR2 and VR1 respectively.

(a) The offset null is adjusted by setting all bits to OFF (Low) and adjusting VR2 until Vout = 0·000V.

(b) Calibrate with all bits set to ON (High) and adjust VR1 until Vout=Normal Full Scale Reading—1LSB (FSR/256) e.g. Set f.s.r. to 2·5V −1LSB = 2·49V. (Where 1LSB = 10mV.)

(c) Repeat stages (a) and (b).

A SPDT switch is provided at pin 14 of IC1 to switch the output of the ZN425E between the 741 (IC2) and the LM311N (IC3) comparator, which is used when in the ADC mode.

The author used a small p.c.b. type switch, but pads have been provided, so that for those who wish to use a toggle, a hole can be drilled and connecting leads taken from the switch to the pads.

The output of the comparator is taken to CB1, pin B of the I/O port. (Bit 7 Port 4 for Z80 PIO).

Provision has been made for adjustment of offset voltage and normal full scale reading at the comparator with VR4 and VR3 respectively. These are adjusted in the same manner as described above. Once set there should be no need for re-adjustment, apart from periodic checks or following accidental displacement.

A small power transistor of the 2N3055/BFY51 700mW, 1A n.p.n. type has been included at the output from the DAC circuit to enable small motors to be driven and bulbs to be lit up. Power is taken from the 5 volt rail which supplies the 741 and 311, the ZN425E being powered by the host computer. A −5 volt supply is also used by the 741 op-amp. This is taken from the negative side of two batteries connected in series, the centre, + − , point being connected to ground. Two short links are made on the component side of the board. These should not be mounted flush, because they are useful as a test point at the output of the converter and a ground rail for all tests. A test point is also provided at the output from the 741 op-amp. The DAC function can be tested at these points with a meter.

Pads at the front edge of the board include CB1 and CB2 in addition to +5 volts, Ground and Data bits 0 to 7. Notice that on the ZN425E, Data Bits are marked from 1 to 8, with Bit 1 as most significant bit (MSB) and Bit 8 as the least significant bit (LSB). The reverse value of bits from the I/O ports of a computer.

Whilst the author has used 2mm p.c.b. test points (ex-computer panels) for input, output and power sockets, large copper pads are provided so that the constructor can choose to use whatever type of connector is available or preferred.

No provision has been made for opto-isolation from the computer since the circuit is intended for use with external supplies up to 5 volts. Provided care is taken with the polarity of the external power lines and the analogue input to the comparator everything should work fine.

TESTING

After typing in the DAC program, test it with the "l.e.d.s and switches" board (Part 2), to ensure that you have copied the listing correctly. When satisfied that the program is working, record it and turn the machine off.

First tests on the board should be to ensure that there are no shorts or badly soldered joints. If satisfied, plug into the I/O port of the computer *without* the ZN425E on board. Load and run the DAC program, placing 0 value at the ports. Test that you have +5 volts on the correct rail. Now put in 128 and check that you have approximately +5 volts on Data Bit 7 (Bit 1 of converter). Next input 64 through to 1, each time checking for the +5 volt signal. If satisfied that your leads are connected correctly, turn off the computer, insert the ZN425E and start again. This time, connect your meter, digital if you have one, between the two links previously mentioned. Having read the instruction set for the DAC program type in RUN10 to start program without having to wait. On initialisation the output to the ports should be 00000000 and the output from the DAC also 0.00. Enter 255. The ports show 11111111 and the meter reads 2·53

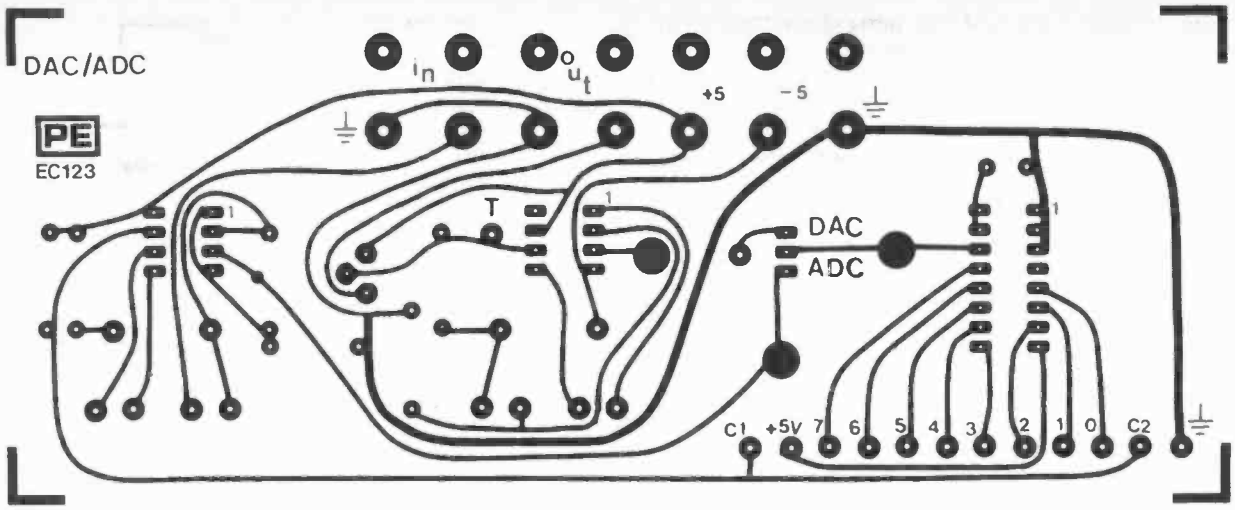


Fig. 6.5. Printed circuit layout (actual size)

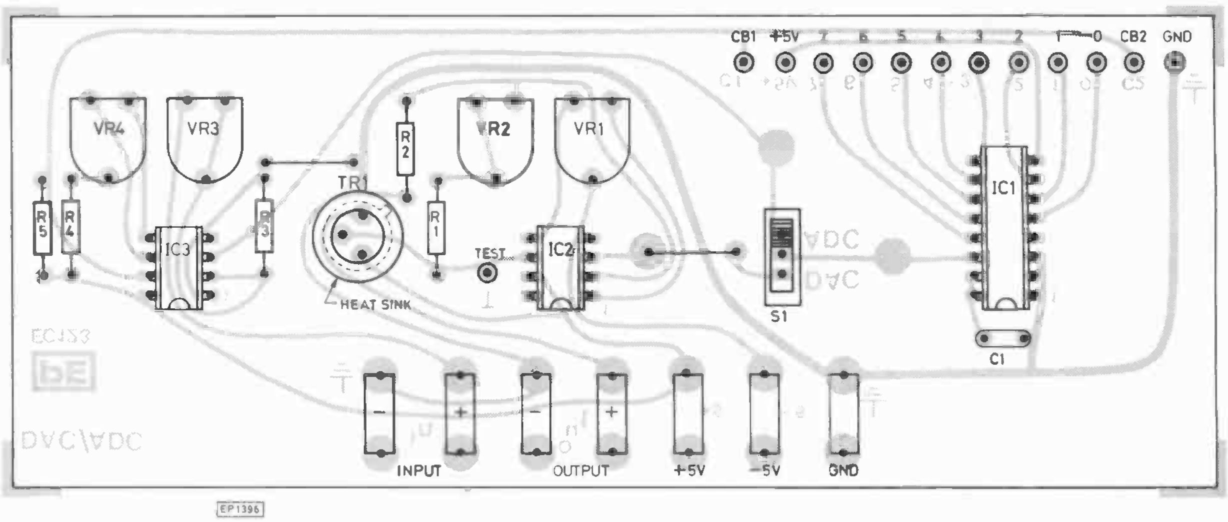


Fig. 6.6. Component layout

COMPONENTS . . .

Resistors

R1	6k8
R2	18k
R3	15k
R4	3k3
R5	1k

All resistors $\frac{1}{4}$W 5%

Potentiometers

VR1, VR4	4k7 (2 off)
VR2	10k
VR3	22k

Capacitors

C1	220n

Semiconductors

TR1	BFY51 or 2N3053
IC1	ZN425E AD/DA converter
IC2	741 op. amp.
IC3	LM311N comparator

Miscellaneous

S1	SPDT p.c.b. mounting
Sockets	2mm p.c.b. mounting

Printed circuit board

Constructors' Note

Printed circuit boards for this series are available from **Proto Design,** 14 Downham Rd., Ramsden Heath, Billericay, Essex CM11 1PU (0268 710722) and **Bradley Printed Circuits,** 9 Harcourt Terrace, Oxford OX3 7QF (0235 32681).

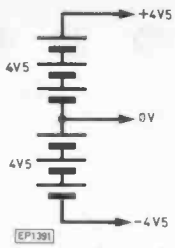
volts (approx.). Next enter 128. The ports show 10000000 and the meter 1·28 (approx.). By changing over your meter range you should get more accurate readings, but the numerals are fairly relative to the decimal value of the binary signal on your screen. Go through 64,32,16,8,4,2 and 1. Any intermediate values will be approx. proportional to the reference voltage.

When happy that your DAC is working, turn to the output of the 741 op-amp. With 4·5 volt batteries, the output for an input of 255 will be around 3·8 volts, for 128, around 1·9 volts etc. Connect a small motor or lamp at the output and observe the results. Don't forget that there is a minimum voltage at which a motor will run and before the glow of a lamp becomes apparent.

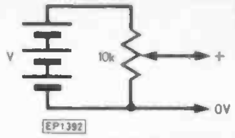
It is assumed that you have set your offset nulls by now. That is, for no inputs there should be zero output. Put an analogue voltage of 3 to 5 volts at the analogue input and adjust the FSR to 2·53 volts. Input 255 from the keyboard and your meter should read 0 volts. This proves that the comparator is working. Try other values. Programs in BASIC that bring the results automatically to the screen will present only a moderate challenge to the computerist.

Having made the initial tests, experiments can now be made in conjunction with a low range voltmeter, passing on to small motors, 6 volt bulbs etc. Broken Christmas toys can provide a useful source for some of these. Why not connect up to a model car with a couple of wires. Not as good as some of the small robots on the market, but a start in the right direction. To test the ADC, a potential divider can be made with a 10k linear pot. across a battery.

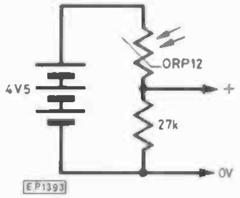
Test the ADC with 1·5 batteries, LDRs, transducers and solar cells. If you have no solar cells, cut the top off a surplus n.p.n. power transistor. Do not use p.n.p. as some of these are filled with a poisonous paste. Do not be disappointed that this interface only measures small voltages. In industrial applications, such as temperature control, the output voltage from a thermo-coupled device is very small. Some simple test circuits are illustrated above.



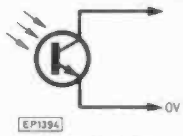
External supply



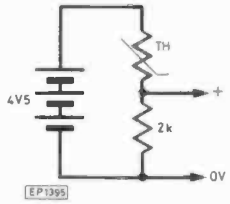
Potential divider



LDR (light) sensor



Transistor as photocell



Temperature sensor

TEST CIRCUITS

NEXT MONTH: The hardware for an EPROM programmer.

BAZAAR

SINCLAIR 48K Spectrum Interface, 1 ZX-Microdrive ZX-Printer Kempston Interface + Spectrum Specific books and other items £280. Tel: Uxbridge 34704.

YESTERYEAR equipment: Scopes, Counters with Temperature Controlled Crystals, large photo flash reduction gear motors. Offers 01-904 9432 Mr. A.G. Hurrion, 193 Woodcock Hill, Kenton, Harrow, Middlesex.

SPEAKER Drive Units (Radford) X-Over, Wood and plans for floor-mounting pair of Radford Speakers. £30. Mr. Peter Brearey, Flat 3, 36 Leopold Road, Wimbledon, London SW19 Tel: 01-946 8861.

3 BOXES assorted valves. All new incl. DA 42, KT66, SU46, Z63, EL34, etc. No reasonable offer refused. Mrs. E. Moult, 81 Knutsford Road, Alderley Edge, Cheshire. Tel: 0625 582098.

MAPLIN 4600 Synth:—Home built case, unfinished project. Need the space. Offers. Mr. D. Lewing, 94 Carville Crescent, Brentford, Middlesex TW8 9RD. Tel: 01-568 4018.

TRANSCENDENT DPX Polyphonic Touch-Sensitive Synth. with built-In chorus, minor filtering problem, £200 ono (£350 new). Mr. Z. Kowszun, 4 Witan Way, Wantage, Oxon OX12 9EU. Tel: 02357 3560.

UK101 40K RAM, 4/8000 Baud Cass. I/F fitted but faulty, also slight video fault. Offers? Mr. S. Nicholls, 18 Warwick Terrace, St. George's Road, Barnstaple, Devon EX32 7AR.

COLOUR Genie 32K + Joysticks Total value £200. Asking £110 ono. Tel: Wickford 62943 after 6 pm. Mr. A.A. Ding, 71 Ethelred Gardens, Wickford, Essex SS11 7ET.

UK101 8K RAM, cased with leads, new monitor, eleven cassettes software including Exmon, disassembler and assembler. Mr. T.J. West, 354 Wolverhampton Road, Cannock, Staffs. Tel: Cannock 4963.

FOR Sale Clef Bandbox with Master Rhythm, fully working £150. Telephone: 01-670 8420 evenings. Mr. R.C. Smith, 62 South Croxted Road, West Dulwich SE21 8BD.

WANTED Sinclair IC12 Amplifier built/unbuilt. Mr. D. Clark Tel: (Aberdeen) 0224 321336.

SHARP scientific Calculator EL-508A book price £5 + postage. Mr. A.C. Holdway, No. 20 Studland Close, Millbrook, Southampton, Hants.

SINCLAIR DM2 Meter £40 Heath IG-4505 Scope Calibrator £40. DSI frequency counter 512MHz £75 Buyers collect. Mr. A.Y. Parekh, 34 St. Margarets Road, Great Barr, Birmingham B43 6LD. Tel: 021-358 6299.

EPROM and manual for wordwise £25. Tel: Oxford (0865) 779855.

HELP ZX81 computer details, program in order to use Creed 7E teleprinter as a printer. P. Wilkins, 12 Chadcote Way, Catshill, Bromsgrove, Worcs. B61 0JT. Tel: Bromsgrove 71692.

WANTED Sinclair ZX printer. Must be in working order. Please write with offers. Stephen Jones, 48 Irsha Street, Appledore, Bideford, Devon.

CENTRONICS 306 dot matrix printer 120 cps, tractor feed with manual, £120 o.n.o. Tel: (0473) 328013. D. S. Francis, 22 Clifton Wood, Holbrook, Ipswich IP9 2PY.

WANTED Manual for telequipment scope model No. D1010, will copy or buy. D. Jeynes, No. 3 Moorend Cottages, Muchcouarne, Bromyard, Herefordshire.

CURRAH Mini-digital recorder 6,000 bits/sec., suit UK101, connects direct to expansion BUS, almost new, £140. Brian Faller, 25 Manor Road, Barnet, Herts. Tel: 01-449 1808, after 6p.m.

DUAL drive/computer case, 15" x 12" x 5", 40/80 units, p+d leads, £35 Astec PSU £35. 051 644 6568. Mr. D. Edwards, 216A Bebington Road, Birkenhead, Merseyside L42 4QF.

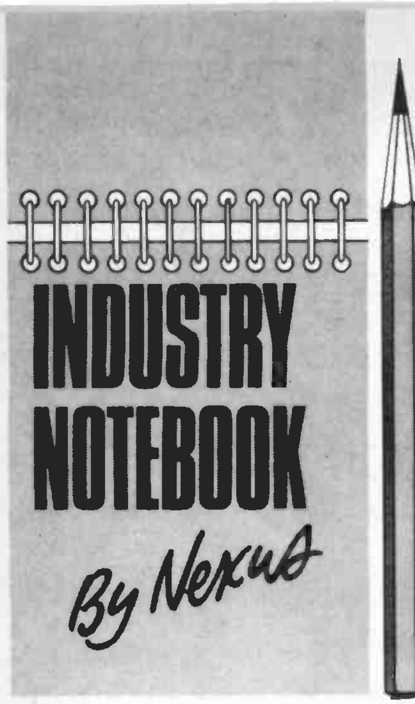
NASCOM 2 48K RAM NAS-SYS3 ZEAP NAS-DIS DEE-BUG Parallel Printer Cable £250 Ian Doble Tel: (087255) 2121. Mr. I. Doble, "Wickham", Quay Road, St. Agnes, Cornwall TR5 0RP.

R.S. Components 19" Sub Rack Kit Stock No. 504-434 new in box £10. Buyer collects/postage. Mr. F. Lucas, 6 West Fryerne, Yateley, Nr. Camberley, Surrey GU17 7SU.

SIGNAL Generator, Marconi TF1066B a.m./f.m., 10–470MHz, 10mV to 0·5μV, fully working £195 o.n.o., Guildford 34954. Mr. A.C. Hewat, Redwood, Blanchards Hill, Jacobs Well, Surrey.

A FEW components previously advertised still available. Must now clear or dump. List sae. No callers. Mr. G.A. Noble, 50 Croft Hill Road, Slough, Berks. SG2 1HF.

BASS Guitar and bass ampolifier for sale. Good condition £250 o.n.o. Mail only please a.s.a.p. G. Wheating, Allhallows School, Rousden, Nr. Lyme Regis, Dorset.



Lost Hope?

Those of us who had hoped for a constructive alternative to Thatcherite economic policy from a rejuvenated Labour party must be disappointed. The 'dream ticket' leadership has produced nothing new and the 1983 manifesto stays intact.

Of course there are vague statements about back-room boys (possibly girls, too) engaged in long-term planning and some new policies will have to emerge in time for the autumn party conference.

The snag is that as economic recovery continues, as is now generally agreed, Mrs Thatcher's claim that There Is No Alternative (TINA) will appear to be more than justified. It will appear that her resolute approach has made British industry more competitive, more efficient. I say 'appear' because, at least in part, the US economy is the locomotive that is pulling the world out of recession, including Britain. Nonetheless it has been Thatcher toughness that has thinned out, if not entirely eliminated, gross overmanning and other deficiencies affecting economic performance.

So where does this leave Mr Kinnock? He can move to the right and try to out-Thatcher Thatcher, beating her at her own game. Or agree, as is his natural inclination, to retain his loyalty to full-blooded socialism. The first would be totally unacceptable by the trade unions, his party paymasters. The second is largely unacceptable by the electorate at the present time.

Labour had hoped that the success of socialist France would have been the example to highlight the comparative failure of Thatcherism. Alas, even this hope has now disappeared in economic failure in France.

With the middle ground already occupied by the Liberal/SDP alliance and with the handicap of inexperience in government Mr Kinnock has a difficult future. The revelation that he, equally with Mrs Thatcher, shops at Marks and Spencer is no substitute for a realistic policy. Nor does his pledge to return the Elgin marbles to Greece if he gains power look like being a vote-winner.

ASMI

Recent runway collisions involving loss of life as well as aircraft is bound to stimulate new demand for Airport Surface Movement Indicator (ASMI) installations. ASMI is a very high definition radar system which concentrates entirely on ground movements. It surveys main and auxiliary runways, aprons, entry and departure lanes, and perimeter tracks. Definition is such that aircraft types can be identified by wing shape and size, tugs, tankers and other replenishment vehicles equally so. Even birds are detectable through fog and rain as well as darkness.

The high cost of such equipment has resulted in a sluggish market. Only those airports with very high international traffic density have so far been equipped, such as those at Heathrow, Rome and Paris.

Racal Avionics has now gone some way to easing the cost barrier by using a mass-produced existing output stage in their latest ASMI, the 18X. One is being installed at Australia's busiest airport at Sydney with follow-ons at London-Gatwick and Stockholm. The Sydney installation has another cost-cutting feature. The ASMI scanner is sited 1·5km from the control tower and the radar data is transmitted by fibre optic links, thus enabling existing cable trunks to be used without fear of external electrical interference or cross-talk with other services.

200kHz Switch

There seems no limit to ingenuity in extending applications to existing systems. A prime example is the novel idea of using the BBC's 200kHz broadcast transmitters at Droitwich, Burghead and Westerglen to switch on and off our off-peak tariff electricity supply. Bad news maybe for existing time-switch manufacturers but a bright opening for the replacement device which will incorporate a narrow-bandwidth fixed-tuned radio receiver.

Switching to the off-peak tariff at consumers' premises will be by phase modulating the 200kHz carrier and, because of the narrow bandwidth of the receiver, reception will be possible even in basements of steel-framed buildings.

The new system has been developed by GEC Meters and technical trials have apparently been running for at least four years. Now the Electricity Council has signed a contract with the BBC and consumer acceptance is being evaluated on a sample of 1,500 consumers.

Don't assume that if this idea reaches fruition that the whole nation's off-peak electricity will be switched simultaneously. By signal coding, each electricity area board can operate its own switching regime. And within each area there can be as many as 256 groups of consumers which can be separately controlled.

For the electricity boards there is the tremendous advantage of flexible load control. For the consumer the extra goodie of, say, an afternoon boost to his water heater at off-peak rate.

Airborne

Marconi Avionics continues to demonstrate outstanding ability both in technology and marketing. After developing digital speech communications which had successful trials at the Royal Aircraft Establishment the company has won a £12 million plus order for production equipment. The new digital speech system is scheduled for air-to-air and air-to-surface duty in all Royal Navy aircraft and in RAF maritime reconnaissance Nimrods. It is the biggest order ever to be won by the Basildon plant.

The Rochester plant also got off to a good start in 1984 with an order for submarine detection systems for the Royal Swedish Navy who have chosen the AQS 902 which won a Queen's Award for Technological Achievement last year. I don't often have an opportunity to thank the Soviet Union for anything but I do so on this occasion because their suspected submarine intrusions into Swedish territorial waters prompted Sweden to improve her underwater detection. The AQS 902 has already proved itself in Sea King helicopters of the Royal Navy.

Pioneer

Few of the younger generation will have heard of Sir Harold Bishop who died recently at the good age of 82. Apart from his first two years he spent the whole of his working life in broadcasting, first at 2LO run by Marconi Wireless Telegraph Company and in 1922 transferring with the station to the BBC. As an engineer he progressed upwards, eventually becoming BBC Director of Engineering leading a team of 5,000. He was connected with every major development in broadcasting, including television, and he and his colleagues in the BBC set technical standards which led and still lead the world to the benefit of UK electronics.

Sir Harold was a true pioneer. He was there at 2LO when it had a single microphone feeding a 500 watt transmitter in London's Strand with an aerial on the roof and only a handful of listeners. The latest BBC handbook estimates that there are now 1,500 million radio sets in use around the world. How's that for explosive growth in a single lifetime?

Apropos of the increasing pace of life today I was much taken with a comment from the US politician George W. Ball's autobiography, 'The increasing compression of events now means that by medieval standards I have lived at least five centuries'.

Cable

Britain is not the only country gearing up for the cable TV revolution. East Germany is reported to be speeding up plans for a network. Western observers are probably correct in assuming that this, far from increasing the number of programmes, is a restrictive move. Large numbers of East German viewers regularly watch Western programmes transmitted from Berlin. By installing cable and then banning TV aerials their minds would remain uncontaminated by Western influence.

Space Watch...

THE HALLEY COMET MISSION

Now that agreement has been reached by the agencies involved as to 'who does what', the general scheme of the mission may be said to be finalised. The three agencies involved are the European Space Agency, the Soviet Union and the United States of America. The general strategy of these three has also been reinforced by the Japanese with their two spacecraft: Planet and MS-T5. Thus, this is now a truly international undertaking. It is hoped that the mission's close look at Halley's comet will answer some of the age-old questions regarding comet composition and formation. We have, since the last return of Halley's comet in 1910, developed the technology which may solve the puzzle, in a century that will see two returns.

A few of the important facts of the strategy will be helpful in getting the feeling for the mission. First, the position of the Nucleus of the comet must be established. At the moment we have to make an educated guess because the Halley Nucleus is only ten kilometres or so in diameter, and has never been seen from Earth. This is because although the Coma, that is the cometary atmosphere that surrounds the Nucleus, extends for hundreds of thousands of kilometres, and is so bright that the Nucleus is not discernible. Therefore the European Space Agency has asked the Soviet Union to use the Vega spacecraft to provide the latest information. This is because the launch date of the first Vega will be up to seven days before that of Giotto, the ESA Halley spacecraft. Giotto will then be able to plot the orbit and make its final encounter manoeuvre. The final manoeuvre will be made about two days before the actual fly-by. The ESA want Giotto to intercept the comet's orbit at a point some 500 to 1000km from the Nucleus on the sunward side of the Nucleus. We shall be relying on the Soviet Union for the correction and monitoring data.

Comets are usually described as very primitive bodies that are formed of debris, the most popular theory is that this is from the debris which remained after the formation of sun-like bodies, and that it was mostly ice and dust. Whatever ideas exist at the moment, the encounter will certainly provide sound evidence on which to discuss this matter in the future. One of the matters creating much interest will be the puzzle of the way in which the Coma grows spectacularly as the comet approaches the Sun. There is also the interaction of the atmosphere of a comet with the Solar wind.

Solar heating causes the molecules to become sublimed out of the Nucleus, or as sometimes happens to pass from solid to the vapour state as the comet is heated up. During the time that a comet is being subjected to changes of environment the various reactions that take place often give rise to the creation of a variety of compounds. The Nucleus is so small and its gravity so low that the Coma becomes enormous, and may be millions of kilometres in extent. Under these circumstances the mechanism which makes it appear so bright must be directly related to a considerable amount of dust being present; the extent of this must be important. The Solar wind's ultra-violet radiation ionises the neutral molecules and this creates a plasma that is swept up in a tail. The effect of this reaction is that the Solar wind and the embedded magnetic field creates large electric currents. This, in turn, generates an induced magnetosphere much larger than that of the Earth itself. There may be a bow-shock in the Solar wind that is ahead of the Nucleus, so that the comet experiences a bow-shock within its ionosphere.

The five spacecraft will have similar experiments on board which will be in addition to their routine assignments. Each encounter will therefore be carried out over a period of eight days in March 1986. The information will vary, thus giving the maximum data to pass to scientists. The actual tasks to be carried out, so far as the comet is concerned, are quite varied, but the broad details are set out here as they are known at the moment. It is certain, however, that there will be changes.

MISSION TASKS

The imagery from the Soviet Union spacecraft, Vega 1 and Vega 2, will be at two levels. A resolution of 180 metres is aimed at. For Giotto, however, this will be 50 metres at the Nucleus.

Identification of the composition of gases and dust particles of the comet and the confirmation and examination of the physical processes and chemical reactions in the Coma will also be carried out. Other tasks include measurement of gas production rates and the dust flux and the study of cometary plasma and Solar wind reactions.

SPACECRAFT DEPLOYMENT

The pathfinder will be the Soviet Union's Vega 1. This is to be launched in mid-December 1984. It will fly past Halley at a distance of 10,000 kilometres on March 6th 1986. Japan is sending their first spacecraft to escape the Earth's gravitational field; this will be the MS-T5. It will be launched in January 1985, and will cross Halley's path at about one million kilometres from the Nucleus. This will be on the 8th March 1986. Planet-A will be sent by the Japanese in the middle of August 1985 and fly past at 200,000 kilometres on March 7th 1986.

Vega 2 will be launched in late December 1984 and is planned to intercept the comet on March 9th, 1986;,the distance from the comet being 3000 kilometres. The spacecraft involved deserve a general description.

The two Vegas are three axis stabilised Venera class spacecraft. They are modified for the Venus/Halley international mission. The modified features include an extended Solar array. There are other optical instruments and television cameras for which a special platform has been provided. The spacecraft will be fitted also with a multilayer dust shield to protect the most sensitive areas from potentially lethal dust.

The Venus part of the Soviet Union mission will be accomplished first. The spacecraft will fly past Venus in mid-June 1985, and each will eject a probe into the Venusian atmosphere.

The velocity of the encounter with Halley will be 78km/sec and each Vega will carry 129 kilogrammes of load for the Halley mission. About two and a half hours before the encounter with the comet, the Vega telemetry will be switched to 65 kilobits/sec data rate. Forty kilobits/sec of this will be required for the television monitoring.

The Japanese spacecraft MS-T5 was planned initially as a test vehicle for Planet-A. It was made as part of the Halley mission to overcome pay-load weight problems. The MS-T5 will carry a magnetometer, solar wind detector and plasma wave probes. Planet-A will carry an ultra-violet imager and a magnetic particles detector. It is not expected that these craft will fly close to the comet Nucleus. They should, however, be able to detect the bow-shock waves if they exist, and may encounter the ionosphere boundary. These two spacecraft, each of which weighs 150 kilogrammes, will be launched by an M-382 rocket. They too are spin-stabilised craft and will spin at 5 rpm.

The Giotto has 10 experiments on board using 16 sensors which are to be switched on 4 hours before the point of closest approach. Because of the close approach the pointing accuracy must be held to within 1 degree. The spacecraft is spin-stabilised and will spin at 15 rpm. As it will be travelling in an unknown environment it will carry batteries to back-up the solar cells. This is in case the dust degrades the array. The actual velocity of fly-past is expected to be 68km/sec. At that time the Halley comet is expected to be somewhere about 0·89AU from the Sun and 0·97AU from Earth. The spacecraft will approach the comet from the antisun side. This means that the chance of being overwhelmed by dust is minimised and therefore increases the chances of its survival.

IMAGING

Four of the spacecraft of the Halley mission are carrying imaging instruments and will therefore pass to the Sunward side of the comet to avoid as much interference as possible. The only craft which does not is the ISEE-3. This is well equipped to observe solar wind interaction with a cometary atmosphere. It will, therefore, be possible to observe from the comet side of the Sun. The spacecraft is expected to cross the comet's tail at about 15,000 kilometres from the Nucleus.

Frank W. Hyde

Micro-Professor MPF-1 Plus

*MICHAEL TOOLEY BA

SOME eighteen months ago I was fortunate enough to be asked to carry out a review of the Microprofessor MPF1; a low-cost Z80 based microprocessor learning aid. This basic system, of which over 4000 have been sold, consisted of a single-board fitted with a Z80 CPU, 2K ROM, 2K RAM, 36-key keyboard, and a display comprising six seven-segment LED indicators. The package was supported with documentation including a monitor listing, and a "User's Experiment Manual". Although I had a few minor reservations about the package, I was able to give it a firm recommendation and my overall conclusion was that it represented good value for money for those about to enter the world of microprocessors. I am now pleased to report that Multitech have produced a new and much improved version of the Microprofessor, known appropriately as the Microprofessor MPF–1 PLUS.

MICROPROFESSOR LEARNING AIDS

Hardware, software and documentation make up the trio of essential components in any microprocessor learning package. Whereas these items may appear at first sight to be quite separate and distinct, there is a high degree of interdependence. Indeed, if any one of the three is found to have serious shortcomings then this is likely to be to the detriment of the package as a whole. It is a great shame that some learning aids fail quite badly in this respect. Excellent hardware, for example, is of little use if the accompanying software and documentation are lacking in depth and clarity.

Hardware must be built to a high standard such that it is both reliable and durable. As far as possible all i.c. devices should be mounted in sockets which facilitate easy removal in the event of failure. Connectors should be both electrically and mechanically robust, and only first quality 'industry standard' components should be used. In addition, the printed circuit board should be neatly laid out and screen printed so that all components can be readily identified.

Software, which will invariably be resident in ROM, should incorporate monitor facilities with commands and prompts which are both easy to understand and simple to remember! Ideally, both assembler and disassembler facilities should be incorporated. The accompanying documentation should be properly structured and should cater for the complete newcomer as well as those having some previous knowledge. Texts should incorporate relevant examples and applications should be introduced where appropriate. A full commented monitor source listing should be considered essential.

FIRST IMPRESSIONS

Like its predecessor, the Microprofessor MPF–1 PLUS comes securely packed in a corrugated cardboard box and, inside, the unit itself is contained in a neat, if rather 'plastic', book-style case. The case, which measures 255 × 200 × 48mm (approx), is secured by means of a press-stud fastener and opens to reveal the microprocessor board in the right hand leaf and a recess in the left hand leaf. This latter space is designed to accommodate one or more of the various options available which include an EPROM programmer, speech synthesiser, printer/disassembler, and I/O board. A separate a.c. mains adaptor is supplied which operates from a 240V 50Hz supply and provides a nominal 9V output at 600mA. The mains unit is fully encapsulated and is fitted with an integral 13A mains plug.

A 49-key keyboard, which uses a conventional QWERTY layout, replaces the previous 36-key hex and dedicated function unit. Despite the relatively small size of the keys, there is plenty of clearance around them and they have a pleasantly reassuring positive action.

Another very significant area of improvement is the twenty-character fourteen-segment vacuum fluorescent display. This is angled for convenient viewing and replaces the six seven-segment LED displays of its predecessor. The display is bright and extremely easy to read even in difficult lighting conditions. The fourteen-segment display is naturally capable of displaying a much wider range of characters and symbols than its seven-segment counterpart.

CLOSER EXAMINATION

Close examination of the p.c.b. reveals the same high standard of construction common to all Multitech products. The screen printed p.c.b. is neatly laid out and all major devices are socketed. The monolithic voltage regulator (a 7805) has been relocated to the centre of the p.c.b. and now uses the substantial heatsinking properties of the aluminium sub-frame which supports the vacuum fluorescent display. Consequently, the regulator now runs very much cooler than previously. The breadboard area of the original Microprofessor is absent. This, however, is no great loss since breadboarding directly onto the MPF–1 p.c.b. cannot really be recommended since it invariably tends to be a 'one-off' operation!

Removal of the p.c.b. (it is simply a press-fit into the plastic book) reveals a battery holder designed to accommodate four UM3 dry batteries. This new facility provides back-up of the RAM such that, with the CMOS devices fitted, memory can be retained for up to twelve months. This was found to be a most useful facility, enabling partly

*Mike Tooley is Principal Lecturer in Electronics at Brooklands Technical College, Weybridge.

finished programs to be retained during software development without the need to perform a tape load/save on each occasion of use.

The Microprofessor now uses an 8K ROM (2764) and has 4K static RAM (2 × 6116). An optional 8K BASIC ROM is available. FORTH is also planned for the MPF–1 PLUS but the ROM was unfortunately not available at the time of review.

DOCUMENTATION

In keeping with other changes, MPF–1 PLUS documentation is also vastly improved. The basic unit is supplied with three handbooks; a User's Manual, Experiment Manual, and a Monitor Source Listing. In addition, a Student Work Book is also available. The User's Manual contains chapters entitled Overview and Installation, Specification, System Description, Operating MPF–1P, Useful Subroutines, Text Editor, Assembler and Disassembler, and System Hardware Configuration. The English is still a little quaint in places however the manual is otherwise extremely good.

The 311-page Student Workbook also has some 'oriental' English and does contain a few rather obvious errors (why on earth don't Multitech get someone proficient in English to proof read their texts?). The manual is well structured, and includes questions or exercises at the end of each chapter. The Workbook is suitable for an absolute beginner and is also ideal for the individual who is not following a formal course of instruction. Chapters are included on Keyboard Familiarisation, Hand Assembly, Introduction to Hardware, Using the Text Editor, Using the Two Pass Assembler, and How to Read a Schematic. This last title is somewhat misleading and the chapter leaves a number of questions unanswered.

ASSEMBLER AND DISASSEMBLER

One of the main criticisms of the original Microprofessor was the absence of a resident assembler. This meant that all programs had to be hand assembled and entered in hex. This tedious process is prone to error and rarely used for serious software development. Multitech have recognised this fact and have included a two-pass Z80 assembler in the MPF–1 PLUS.

Programs are entered, using standard Z80 mnemonics, line-by-line from the keyboard and resident text editor. The programs are then assembled and the appropriate source code is generated. An unfortunate disadvantage is that the reverse process (i.e. disassembly) can only be carried out in conjunction with the companion printer module, PRT–MPF–1P. This unit contains the disassembler software in ROM and, whilst one might argue that program disassembly is usually made direct to a printer, it would be nice to be able to disassemble on a minimum system without a printer.

BASIC

The optional BASIC ROM is entered from the keyboard via 'CONTROL–B'. BASIC statements exceeding twenty characters in length are automatically scrolled left when the display is filled. When editing long program lines the overflow may be displayed by appropriate use of the left-arrow. It is, however, a little disconcerting to find that later use of the right-arrow does not restore the display (i.e. characters shifted to the left of the first display digit are lost!). Three characters, '<', '?', and '@', are used to indicate monitor, input, and command level.

The 8K BASIC is reasonably powerful and will accept hex as well as decimal inputs. Editing is somewhat crude and lacking in the facilities which are normally found in low-cost personal computers. Furthermore, since only one line is displayed at a time, a printer soon becomes almost essential for any other than the most elementary of programs.

The 181-page BASIC manual is quite acceptable and consists of a step-by-step introduction to Microprofessor BASIC. It is ideal for the beginner wishing to make a first step into programming in a high level language. By the time that you read this review, an alternative 8K FORTH ROM should be available. This should bridge the gap between BASIC and assembler and appeal to those wishing to explore this excellent control-oriented language.

PRINTER

The first Microprofessor option which most users will want to consider is the high speed twenty character thermal printer. I frankly admit that my first reaction on unpacking the unit was surprise and reinforcement of the commonly held conviction that one doesn't get very much for one's money these days! I am now prepared to admit that I was wrong since, despite its apparent simplicity, the unit does work extremely well. It is quiet and reliable in operation and the printed text is very pleasing. The printer is supplied with a roll of thermal paper, a connecting cable, and the necessary mains adaptor. The printer is accompanied by a brief but perfectly adequate manual.

INPUT/OUTPUT

One of the most commendable features of the Microprofessor system is the level of expansion which is possible. An option which will undoubtedly prove to be very popular with both the electronic enthusiast and the equipment designer is the I/O board. This exciting module facilitates connection to the outside world in a variety of different forms. The hands-on experience of microprocessor interfacing which can be gained from this board is second to none!

The I/O board is the same size as the basic Microprofessor p.c.b. and incorporates both serial I/O in the form of an 8251 programmable communications interface and parallel I/O in the form of the Z80–P10 (programmable input/output). Thrown in for good measure is the Z80–CTC (counter timer circuit) and a sizeable breadboarding area. A further 4K ROM and 6K RAM are also provided. Like the printer, the I/O board has its own mains power supply and connects to the CPU board using a short length of 40-way ribbon cable.

A 113 page manual contains applications examples for the

SPECIFICATION

CPU	Z80A
RAM	2 × 6116 CMOS static (4K total)
ROM	8K system monitor 8K BASIC or 8K FORTH (optional)
DISPLAY	20 character 14 segment vacuum fluorescent
KEYBOARD	49-key 'QWERTY' layout
CASSETTE INTERFACE	165 baud serial read/write
LOUDSPEAKER	63mm (2·5 inch)
I/O	48 parallel system lines
SOFTWARE	Z80/8080 machine code plus resident line and two-pass assembler
POWER SUPPLY	240V 50Hz mains (plus four 1·5V dry batteries for memory back-up)

The MPF–1 PLUS with the PRT, EPB and I/O boards and manuals

Z80–P10, Z80–CTC and 8251 devices together with relevant data sheets for each device contained in an appendix. Applications discussed are respectively a traffic light system, clock, and an RS–232C selectable baud rate interface. Demonstration software is contained in ROM and entered by means of an appropriate monitor command and starting address.

CONCLUSIONS

The MPF–1 PLUS is ideal for use both in the formal educational environment and for the individual working on his own. Hardware, software, and documentation have all been much improved. An alternative approach to learning assembly language programming involves the use of an assembler package based on a personal computer. Whilst the cost of such a package is commensurate with that of the Microprofessor (when one includes the cost of the microcomputer itself) it has several drawbacks as far as the electronic enthusiast is concerned. Firstly this is because few home computers are designed with a view to extensive hardware development and, secondly, a computer designed primarily for the domestic and games market is unlikely to have the I/O capability of a machine intended for real-world control applications.

At £140 (plus VAT and carriage) the MPF–1 PLUS costs nearly twice as much as its predecessor. For this one gets a very much enhanced machine and one that still represents good value for money. It is, however, important to also bear in mind at the outset the cost of further expanding the system. Whilst the additional cost of a printer and I/O board may prove to be prohibitive for the hobbyist it may be affordable for the educational institution (particularly where several Microprofessors may share an I/O board, printer, or EPROM programmer).

For those concerned rather more with the hardware than the software aspects of microprocessors and wishing to gain a firm grounding in Z80 family applications, the Microprofessor can be very strongly recommended. It is bound to be another winner for Multitech!

The Microprofessor MPF–1 PLUS is available from Flight Electronics Ltd., Quayside Road, Southampton, Hants, SO2 4AD. Tel. (0703) 34003/27721.

The following accessories are currently available:

PRT–MPF–1P	**Twenty character high speed thermal printer**
EPB–MPF–1P	**EPROM programmer**
SSB–MPF–1P	**Speech Synthesiser**
SGB–MPF–1P	**Sound Synthesiser**
I/O–MPF–1P	**Input/output board**

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URGENT ULA chip for ZX81 needed, up to £5.00; also graphic ROM for same needed, up to £10.00. C. Tuckwood (Chris), 19 Holmwood Avenue, Plymstock, Plymouth, Devon PL9 9JP.

WANTED Image intensifier tube Mullard type, XX1060 ideally. Must be in excellent working order, cash offered. M. Gillett, 11 Broadway, 'Rodbourne Cheney', Swindon, Wilts SN2 3BN.

PYE AM 25B crystal 4 metres 70·26 mH TX RX, vgc £12. DX2001 receiver covers all bands to 30 MH, £75 v.g.c. Mr. R. Pearson. Tel: Swansea 582941.

WANTED Frame and plug or complete chassis CX1571 XY plotter for CD 1400 solatron oscilloscope. J. F. Radley, 28 Queen Street, Geddington, Northants. Tel: (0536) 743524.

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INTRODUCTION TO DIGITAL ELECTRONICS

MICHAEL TOOLEY BA DAVID WHITFIELD MA MSc CEng MIEE

O & A Level Part Seven

THE 74121 is an integrated circuit monostable which can be triggered by either positive or negative edges depending upon the configuration employed. The device has complementary outputs and requires only two components (one resistor and one capacitor) to define the monostable pulse duration. The internal arrangement of the i.c. is shown in Fig. 7.1. Control inputs,

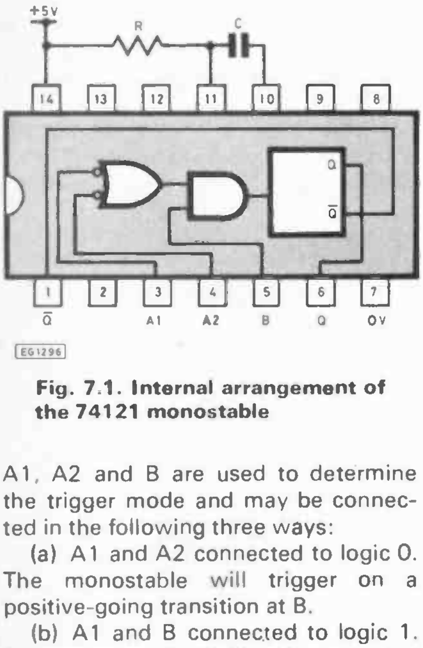


Fig. 7.1. Internal arrangement of the 74121 monostable

A1, A2 and B are used to determine the trigger mode and may be connected in the following three ways:

(a) A1 and A2 connected to logic 0. The monostable will trigger on a positive-going transition at B.

(b) A1 and B connected to logic 1. The monostable will trigger on a negative edge applied to A2.

(c) A2 and B connected to logic 1. The monostable will trigger on a negative edge applied to A1.

It should be noted that, unlike some other monostable types, the 74121 is not retriggerable during its monostable period. This means that any input transitions received during the period of the output pulse will be ignored. Furthermore, in normal use, a recovery time equal in length to the monostable pulse should be allowed before attempting to re-trigger the device.

PULSE STRETCHER USING THE 74121 MONOSTABLE

The following investigation involves using the 74121 monostable as a 'pulse stretcher'. As the name implies, a pulse stretcher is a device for elongating the duration of a pulse. A 74121 monostable is an ideal device to provide this function; it can be triggered by a pulse of fairly short duration and will continue to provide its fixed duration output pulse long after the input signal has reverted to its original state. The only requirement is that, to ensure reliable triggering, the

RESISTANCE, R	CAPACITANCE, C	APPX. MONOSTABLE PERIOD, t
10k	10p	70ns
2k2	100p	150ns
10k	100p	700ns
2k2	1n	1·5μs
10k	1n	7μs
2k2	10n	15μs
10k	10n	70μs
2k2	100n	150μs
10k	100n	700μs
2k2	1μ	1·5ms
10k	1μ	7ms
2k2	10μ	15ms
10k	10μ	70ms
2k2	100μ	150ms
10k	100μ	700ms

EG1278

Table 7.1. Typical values of CR and monostable period for the circuit of Fig. 7.1

input pulse should have a width of at least 50ns. For a 74121, the values of external timing resistor should normally lie in the range 1·5kohm to 39kohm. The minimum recommended value of external capacitor is 10pF; however, the maximum value is only dictated by leakage current of the capacitor employed. In practice this means that, if necessary, values of several hundred μF can be used. This results in a monostable device which can provide a very much wider range of monostable periods than the simple types discussed earlier. Typical values of monostable period for some common C–R values are given in Table 7.1. In this particular example we are concerned with relatively long monostable periods, i.e. ones which we can detect using the l.e.d. indicators of the Logic Tutor. In practical circuits we will generally find that the monostable periods are a great deal shorter than this!

The circuit diagram of the pulse stretcher is shown in Fig. 7.2. The following links are required on the Logic Tutor:

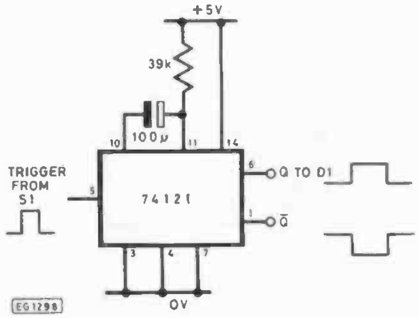


Fig. 7.2. Monostable pulse stretcher using the 74121

A3	to	0V	(A1 control input logic 0)
A4	to	0V	(A2 control input logic 0)
A5	to	S1	(S1 will provide trigger pulse)
A6	to	D1	(D1 will indicate the output)
A7	to	0V	(0V)
A12	to	A13	via 100μF capacitor (+ve to A13)
A13	to	+5V	via 39kΩ resistor
A16	to	+5V	(positive supply)

Insert the 74121 in socket A of the Logic Tutor. Check that D1 is initially extinguished. Press, and immediately release, S1 to generate a short 0 —> 1 —> 0 pulse. D1 should become illuminated immediately S1 is depressed and should remain illuminated for approximately 3 seconds. Once the monostable period has started, the 74121 will ignore any further attempts at triggering. Readers should find that D1 must be extinguished before another monostable timing period can be generated. If desired, the investigation can be repeated using different values of capacitor and resistor in order to obtain other monostable periods.

VARIABLE WIDTH REPETITIVE PULSE GENERATOR

To conclude our look at monostables this exercise involves putting into practice several of the techniques introduced thus far. It will, however, be necessary for readers to have access to an oscilloscope in order to derive full benefit from this particular investigation. Such an instrument will allow readers to display time related waveforms within the circuit and, ideally, it should be a dual beam type.

The investigation uses a 74S124 to provide a symmetrical square wave clock operating at approximately 11kHz. The output of the clock is taken to a 74121 monostable which has a variable resistance connected as part of its timing circuit as shown in Fig. 7.3. The configuration and values employed produces a monostable period which is adjustable over a range of approximately 10:1 (30μs maximum to 3μs minimum approximately). The output of the monostable is repetitive since it is retriggered on the falling edge of each clock cycle (the clock cycle has a period of approximately 90μs which is, of course, smaller than the monostable period). The monostable output thus consists of a train of pulses having a duty cycle which may be varied by means of the variable resistor. Typical waveforms for the pulse generator are shown in Fig. 7.4.

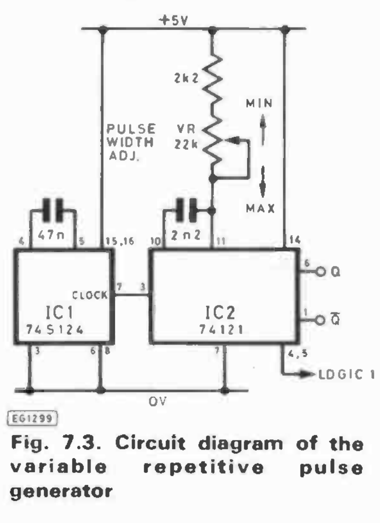


Fig. 7.3. Circuit diagram of the variable repetitive pulse generator

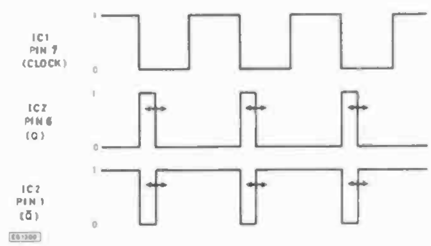


Fig. 7.4. Typical waveforms for the pulse generator of Fig. 7.3

The 74S124 and 74121 devices should be inserted into sockets A and B of the Logic Tutor respectively. As usual, pin 1 of each device should be orientated so that it aligns correctly with pin 1 of the relevant socket. The following links are required:

A4	to	A5	via 47n capacitor
A6	to	A8	
A7	to	B3	(clock output)
A8	to	0V	(0V)
A15	to	A16	
A16	to	+5V	(positive supply)
B3	to	Y1	(clock displayed on Y1 channel of 'scope)
B4	to	logic 1	(A2 control input logic 1)
B5	to	logic 1	(B control input logic 1)
B6	to	Y2	(output displayed on Y2 channel)
B7	to	0V	(0V)
B12	to	B13	via 2n2 capacitor
B13	to	+5V	via 22k variable and 2k2 fixed resistors
B16	to	+5V	(positive supply)
0V	to	oscilloscope common earth	

Now we will look at a problem. Suppose that a certain logic control system requires an input signal consisting of a logic 1 pulse for precisely the duration of one complete clock cycle. The input signal is to be obtained from a push button whilst the output signal should not be retriggerable until the push button is released and pressed again. The problem can be solved using the devices and techniques described earlier.

DE MORGAN'S THEOREM

De Morgan's theorem is an extremely useful tool in the analysis and simplification of logic expressions. By applying De Morgan's theorem it is possible to construct arrangements of logic gates using either NAND or NOR (or a mixture of both) to satisfy any desired logical function. Furthermore, the technique can help us to use the minimum number of logic gates. This process, which is essential in many practical applications, is known as "minimisation".

In Part Six we mentioned that a particular pattern in the output column of a truth table could help us find an alternative Boolean expression for the gate concerned. It is worth looking at this again as a prelude to De Morgan's theorem.

Table 7.2 shows the truth table for two-input NAND and two-input OR gates, arranged with their output columns side by side. It should immediately be obvious that, although the two output columns look almost the same, the three 1's and 0's in each column are not quite coincident. If, however, we were to invert the A and B inputs for one of the gates and then compare the truth tables again we would get two identical output columns, as shown in Table 7.3. We therefore conclude that the NAND function is identical to the OR function with both inputs inverted. Thus, for two

		NAND OUTPUT	OR OUTPUT
A	B	$\overline{A\cdot B}$	A+B
0	0	1	0
0	1	1	1
1	0	1	1
1	1	0	1

EG1438

Table 7.2. Truth tables for two-input NAND and OR gates

A	B	$\overline{A\cdot B}$	$\bar{A}$	$\bar{B}$	$\bar{A}+\bar{B}$
0	0	1	1	1	1
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	0	0	0

EG1439

Table 7.3. Comparison of truth tables for a two-input NAND gate and a two-input OR gate with inverted inputs

inputs, NOT (A AND B) is the same as (NOT A) OR (NOT B). In Boolean form this is written:

$$\overline{A\,.\,B} = \bar{A} + \bar{B}$$

Complementing each side of the expression, and recalling that a double complement cancels, gives:

$$A\,.\,B = \overline{\bar{A} + \bar{B}}$$

Had we started with NOR rather than NAND gates, we would have obtained the truth tables shown in Table 7.4. This in turn yields the result that

A	B	$\overline{A+B}$	$\bar{A}$	$\bar{B}$	$\bar{A}\cdot\bar{B}$
0	0	1	1	1	1
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	0

EG1440

Table 7.4. Comparison of truth tables for a two-input NOR gate and a two-input AND gate with inverted inputs

NOT (A OR B) is the same as (NOT A) AND (NOT B). Writing this in Boolean form gives:

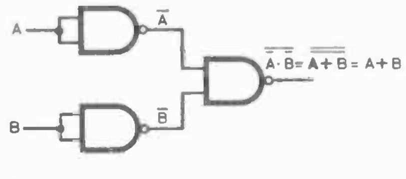
$$\overline{A + B} = \bar{A}\,.\,\bar{B}$$

Similarly, complementing both sides gives:

$$A + B = \overline{\bar{A}\,.\,\bar{B}}$$

These two expressions, which jointly constitute De Morgan's theorem are, of course, exactly the same as those arrived at earlier. Whichever type of gate we start with the result is the same. So much for the theorem, now let's see what we can do with it!

Suppose that we need to construct a two-input OR gate but we only have two-input NAND gates available. De Morgan makes it simple; all we need to do is to invert each input, using NAND gates with the two inputs tied together to act as an inverter, and then apply the outputs to a third NAND gate, as shown in Fig. 7.5. If, alternatively, we had a quantity of two-input NOR gates and needed a two-input AND gate this

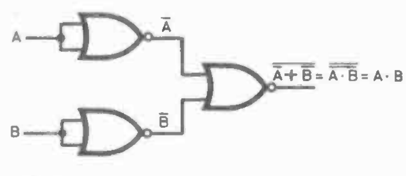


EG1441

Fig. 7.5. Two-input OR gate from two-input NAND gates

could be easily achieved by means of the arrangement shown in Fig. 7.6.

Readers wishing to put De Morgan's theorem to the test may like to try the following exercises based on the 7400 quad two-input NAND and 7402 quad two-input NOR gates.



EG1442

Fig. 7.6. Two-input AND gate from two-input NOR gates

OR FROM NAND

This investigation shows how a two-input OR gate can be built using three of the four two-input NAND gates of a 7400. The logic arrangement is the same as that already seen in Fig. 7.5. The 7400 should be inserted in socket A of the Logic Tutor, checking as usual that pin 1 aligns with 'A1'. The following links are then required:

A1	to S3	(S3 acts as the A input)
A2	to A1	
A3	to A15	($\bar{A}$)
A4	to S4	(S4 acts as the B input)
A5	to A4	
A6	to A14	($\bar{B}$)
A7	to 0V	(0V)
A13	to D1	(D1 indicates the output)
A16	to +5V	(positive supply)

Operating S3 and S4 whilst observing the state of D1 should confirm that the combination behaves as an OR gate. D1 should become illuminated whenever either S3 or S4 (or both) are providing logic 1.

AND FROM NOR

This investigation shows how an AND gate can be realised from three of the four two-input NOR gates of a 7402 following the arrangement shown in Fig. 7.6. Insert the 7402 into socket A of the Logic Tutor (checking that pin 1 aligns with 'A1') and make the following connections:

A1	to A14	($\bar{A}$)
A2	to S3	(S3 acts as the A input)
A3	to A2	
A4	to A13	($\bar{B}$)
A5	to S4	(S4 acts as the B input)
A6	to A5	
A7	to 0V	(0V)
A15	to D1	(D1 indicates the output)
A16	to +5V	(positive supply)

Operating S3 and S4 whilst observing D1 should confirm that the combination behaves as an AND gate. D1 should only become illuminated when both S3 and S4 are producing logic 1.

EXCLUSIVE–OR FROM NAND

As a final example of the use of De Morgan's theorem, and of the technique of minimisation, let us assume that we need an Exclusive–OR gate but only have NAND gates available. (The 7400 quad two-input NAND gate is, in any event, far more plentiful than the 7486 quad two-input Exclusive–OR gate.) To make the example easier to follow we shall divide the task into several simple stages and draw the logic arrangement of each.

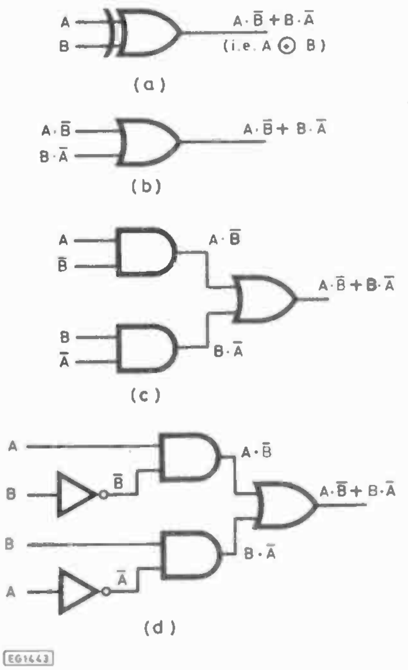
Stage 1. Write down the Boolean expression for the desired output. In this case we require the output, X, to be:

$$X = A\,.\,\bar{B} + B\,.\,\bar{A}$$

Stage 2. Separate the expression into its constituent parts and identify the logical connective between them. In this case we have two expressions: A AND (NOT B) and B AND (NOT A) which are OR'd together to produce the final output, X. This allows us to establish the nature of the last logic gate (OR in this case), and we can then write down the Boolean expressions for its inputs, as shown in Fig. 7.7(b).

Stage 3. Repeat the process of Stage 2 again dividing the Boolean expressions into constituent terms or expressions. The A AND (NOT B) term, for example, can be produced by using an AND gate fed with inputs of A and $\bar{B}$. Similarly, B AND (NOT A) can be produced by a further AND gate which, in this case, is fed with inputs of B and $\bar{A}$.

Stage 4. By further repetition (if necessary) one should eventually arrive at individual terms (e.g. A, B, etc.).



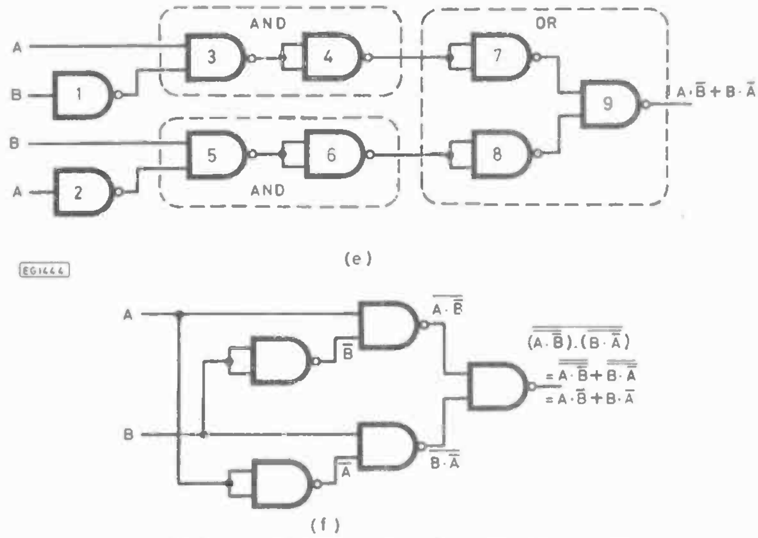
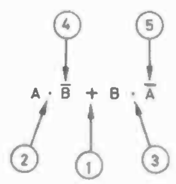


Fig. 7.7 (a to f). Stages in producing an Ex-OR gate from two-input NAND gates

Where these are inverted (e.g. $\overline{A}$) this can be easily achieved by means of additional inverter stages. Now draw the complete logic diagram, as shown in Fig. 7.7(d). Check that there are as many gates present as there are logical connectives (i.e. ., +, and ‾‾) in the original expression. In this case there are five such connectives and we have numbered them below in the order in which they have been dealt with:



Stage 5. Replace each gate by its De Morgan equivalent using NAND or NOR, as required. Remember that inverters may be produced by linking two, or more, inputs together. In this case we are constrained to using two-input NAND gates only, the result of using these connected to form the required OR, AND and inverters, is shown in Fig. 7.7(e). At this stage the logic gate arrangement may begin to look rather complex and it is, therefore, often a good idea to number the logic gates.

Stage 6. Simplify the arrangement arrived at in Stage 5 by removing all redundant gates (e.g. two inverters following one another) and then group together all of the inputs. In this particular example gates 4, 7, 6 and 8 are redundant. Sketch the final logic arrangement and, if desired, check by means of Boolean algebra following the logical inputs through, stage by stage, from input to output.

Readers may now like to check for themselves that the Exclusive–OR arrangement really does work! Since we shall require a total of five gates, two 7400's will be required. These should be inserted into sockets A and B of the Logic Tutor, taking care to observe the usual convention of pin 1 to 'A1' etc. The following links are required:

A1 to S3	(S3 acts as the A input)
A2 to A1	
A3 to A14	($\overline{A}$)
A4 to S4	(S4 acts as the B input)
A5 to A4	
A6 to A11	($\overline{B}$)
A7 to 0V	(0V)
A10 to B2	($\overline{A.\overline{B}}$)
A12 to A2	
A13 to B1	($\overline{B.\overline{A}}$)
A15 to A5	
A16 to +5V	(positive supply)
B3 to D1	(D1 indicates the output)
B7 to 0V	(0V)
B16 to +5V	(positive supply)

D1 should, of course, become illuminated when either S3 or S4 is producing a logic 1. It should not, however, remain illuminated when both S3 and S4 are at logic 1, or both at logic 0.

KARNAUGH MAPS

Karnaugh Maps form the basis of a powerful graphical technique which can be used to minimise logic systems. The map simply consists of a number of cells linked together, each cell representing a unique logical condition. The number of cells in the map depends upon the number of variables present; a system with one variable will have two cells, a system with two variables will have four cells, a system with three variables will have eight cells, and so on. In general, a system with n variables can be mapped using 2^n cells. To put this into perspective let's consider a simple system with just two variables, A and B. The four cells of the map are arranged in two columns (A and $\overline{A}$) and two rows (B and $\overline{B}$), as shown in Fig. 7.8. The cell coincident

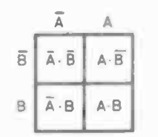


Fig. 7.8. Karnaugh Map for two variables

with column $\overline{A}$ and row $\overline{B}$ is equivalent to the Boolean condition (NOT A) AND (NOT B) or $\overline{A}.\overline{B}$.

In terms of the truth table this corresponds to the input condition A = 0, B = 0. Fig. 7.9 shows all four possible input conditions together with their corresponding cells on the Map.

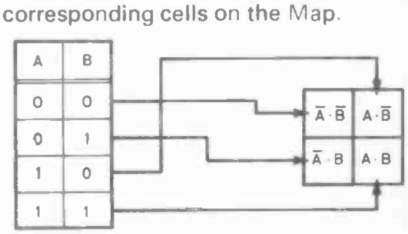


Fig. 7.9. Relationship between a Karnaugh Map and a truth table

To show how the Karnaugh Map works, a useful exercise is to consider the pattern produced by some familiar two-input logic gates: AND, NAND, OR and NOR. These are shown in Fig. 7.10. The shaded area in each map is equivalent to a logic 1 in the output column of the respective truth table. Sometimes 1's and 0's are used instead of shaded and unshaded areas, respectively. In this series, we shall use shading exclusively, if for no other reason than it is a little clearer! The maps shown in Fig. 7.10 clearly show the complementary relationships which exist between AND and NAND, and OR and NOR. What else can we do with the maps?

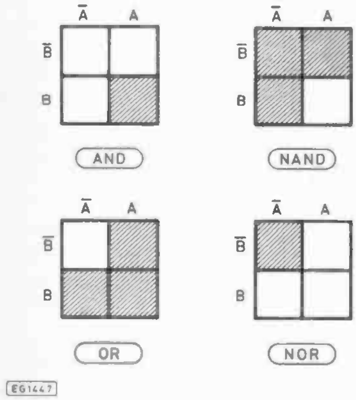


Fig. 7.10. Karnaugh Maps for AND, NAND, OR and NOR gates with two inputs

A single shaded cell involves two variables. Adjacent cells can be grouped together and, by so doing, we can eliminate one of the two variables. Let's take the OR gate for example. The three shaded cells can be considered as two adjacent pairs with one cell common to both, as shown ringed in Fig. 7.11. One of the pairs occupies all

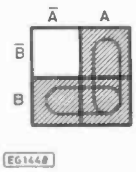


Fig. 7.11. Grouping together adjacent cells in a Karnaugh Map

of column A, the other occupies all of row B. The shaded area is thus, as we might expect A OR B or, in Boolean, A + B. We could, however, have represented the shaded area using the expressions for each of its constituent cells. The Boolean expression for this would be $(\overline{A}\,.\,B) + (A\,.\,\overline{B}) + (A\,.\,B)$. Since the shaded area has remained the same we must conclude that:

$$A + B = (\overline{A}\,.\,B) + (A\,.\,\overline{B}) + (A\,.\,B)$$

At first sight this result may not appear to be very useful and we may have easily arrived at it from the truth table. Let's go on, however, to see the result of carrying out a similar exercise using a NOR gate. The shaded area is the opposite (complement) of that for the corresponding OR gate. It should be noted that the shaded area is coincident with the $\overline{A}$ column and the $\overline{B}$ row. It may thus be represented by (NOT A) AND (NOT B) or, in Boolean terms, $\overline{A}\,.\,\overline{B}$. We could, however, also represent it by NOT (A OR B) or $\overline{A + B}$. Thus we may conclude that:

$$\overline{A + B} = \overline{A}\,.\,\overline{B}$$

If this doesn't ring a loud bell—it should! It's simply De Morgan's theorem yet again.

Karnaugh Maps really come into their own when it is necessary to simplify complex logic arrangements. This usually occurs when we are dealing with gate circuits which have three, or more, inputs. A Karnaugh Map with three variables is shown in Fig. 7.12.

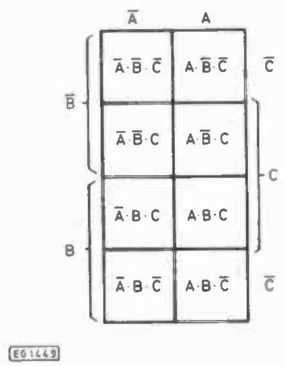


Fig. 7.12. Karnaugh Map for three variables

Here there are 2^3 (= 8) cells which we have arranged in two columns and four rows. (We could have used four columns and two rows, but the result is the same.) Note that B, $\overline{B}$, C and $\overline{C}$ cover two rows each and an overlap is arranged so that all eight different logical states are included. Each of the eight cells has a unique Boolean expression in terms of the three variables, A, B and C. Where two adjacent cells are grouped together, the result is a Boolean expression which eliminates one of the three variables, i.e. the resulting Boolean expression involves only two variables. Similarly, if four adjacent cells are grouped together the resulting Boolean expression involves one single variable only.

When dealing with adjacent cells it is important to note that the map is continuous in either axis. This means that it is possible to 'wraparound' the opposite ends to produce adjacent cells which may otherwise appear to be widely separated. Fig. 7.13 illustrates this point. Here we have

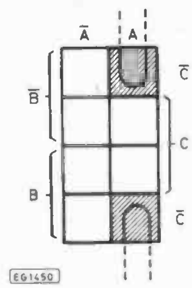


Fig. 7.13. Grouping cells at opposite ends of the Karnaugh Map

grouped together two cells to form a two-variable expression: A AND (NOT C) or, in Boolean form, $A.\overline{C}$.

To conclude this section on Karnaugh Maps it is worth considering a simple example of their use. Suppose that we have been asked to provide a simple electronic system to assist in a voting procedure. There are to be three judges and a simple majority vote is required to determine a successful candidate. Each member of the judging panel is equipped with a switch with which he makes a simple 'yes/no' decision. If two, or more, of the judges vote 'yes' then a light is to come on. Let us suppose that the three judges are called Andrew, Brian and Charles. There are four conditions in which a candidate would be successful:

Andrew	Brian	Charles	Boolean Equivalent
NO	YES	YES	$\overline{A}.B.C$
YES	NO	YES	$A.\overline{B}.C$
YES	YES	NO	$A.B.\overline{C}$
YES	YES	YES	$A.B.C$

Plotting the Boolean expressions on the Karnaugh Map gives the resulting area marked in Fig. 7.14. The shaded area comprises three pairs of adjacent cells, the Boolean expressions for which are: A.C, B.C and A.B. The output, X, of our logic arrangement (corresponding to the entire shaded area) should thus be:

$$X = (A.C) + (B.C) + (A.B)$$

This can be obtained from a three-

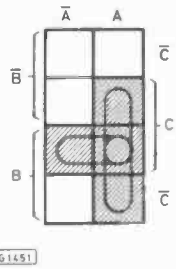


Fig. 7.14. Karnaugh Map for the majority vote

input OR gate preceded by three two-input AND gates in an arrangement similar to that of Fig. 7.15. Note that, had we not attempted to simplify the expression first, we might have ended up with a much more complex arrangement.

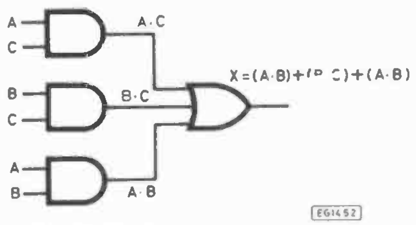


Fig. 7.15. Logic arrangement for the majority vote

BINARY COUNTERS

In Part Five we showed how a D-type bistable could form the basis of a simple binary counter. With such a circuit, a single bistable stage produces, in any given time interval, half as many output pulses as clock input pulses, thus effectively dividing the input frequency by two. This concept can be extended in order to produce circuits which can count the number of input pulses. If several bistables are connected in tandem such that the Q output drives the subsequent CLOCK input, the state of the Q outputs is dependent upon the number of input pulses received. If we take the simple two stage arrangement shown in Fig. 7.16, for example, the state of the Q outputs in response to a number of clock input pulses, n, is shown below:

n	Q1	Q2
0	0	0
1	1	0
2	0	1
3	1	1
4	0	0
5	1	0
6	0	1
7	1	1
8	0	0
etc	etc	etc

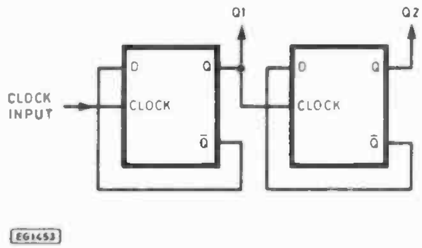


Fig. 7.16. Simple two-stage binary divider

We have, of course, assumed that the initial state of both the Q outputs is logic 0. In practice this could be easily accomplished using the CLEAR inputs provided on the bistables. It should be noted that the pattern of 0's and 1's repeats itself after the third clock input pulse, i.e. the output state for a count of 4 is the same as that for a count of 0. Furthermore, if we just concentrate on the first four states (n = 0 to n = 3), the Q outputs are a binary representation of the number of input pulses, Q2 being the most significant bit (MSB), whilst Q1 is the least significant bit (LSB). The circuit thus effectively counts to 3 and then repeats itself. If we wish to know the state of the count (number of pulses which have arrived) all we need to do is examine the Q2 and Q1 outputs and convert back from binary.

A four stage binary counter is shown in Fig. 7.17. Here four J–K bistable elements have been connected in cascade. The J and K inputs of each stage are connected to logic 1, and the Q output of each stage is connected to the CLOCK input of the subsequent stage. The circuit will count 15 input pulses before reverting to an output state of zero and recommencing. Since there are 16 different output states (including 0000), the circuit forms a divide-by-16 arrangement. We shall now examine a practical divide-by-16 arrangement based upon the 7473 bistable.

BINARY ÷ 16 COUNTER USING TWO 7473's

The circuit of the 7473 ÷16 binary counter is shown in Fig. 7.17. In order to enable operation as a binary divider, the J and K inputs are all taken to logic 1. So that the counter can be reset to zero at the start of counting, the CLEAR inputs are all linked together and taken to S3. A logic 0 from this switch resets the counter whereas a logic 1 permits normal counting (remember that the CLEAR input is "active low"). The 7473's should be inserted in sockets A and B carefully ensuring that pin-1 aligns with socket 1 in each case. The following interconnecting links are required:

A1	to clock	
A2	to A6	
A3	to logic 1	
A4	to +5V	(positive supply)
A5	to A14	
A6	to B2	
A7	to logic 1	
A11	to D3	(D3 indicates the Q2 output)
A12	to A7	
A13	to 0V	(0V)
A14	to D4	(D4 indicates the Q1 output)
A16	to A3	
B1	to A11	
B2	to B6	
B3	to logic 1	
B4	to +5V	(positive supply)
B5	to B14	
B6	to S3	(S3 provides the reset facility)
B7	to logic 1	
B11	to D1	(D1 indicates the Q4 output)
B12	to B7	
B13	to 0V	(0V)
B14	to D2	(D2 indicates the Q3 output)
B16	to B3	

(Total of 24 links)

It should be noted that the l.e.d.s have been arranged in the conventional

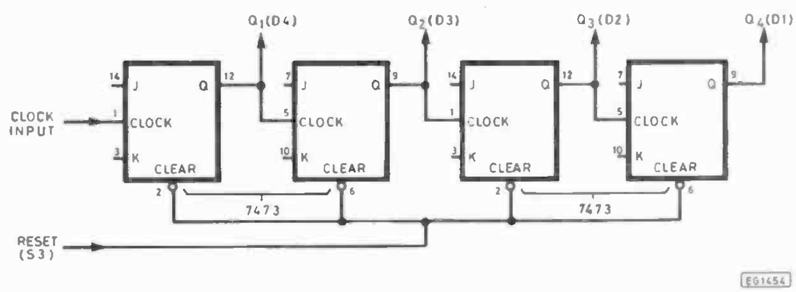


Fig. 7.17. Four-stage binary divider using JK bistables (NB All J and K inputs are taken to logic 1)

order with the most significant bit appearing on the left (D1) and the least significant on the right (D4).

S3 should be set initially to produce logic 0. D1 to D4 should now all be extinguished, indicating an output of 0000 in the reset condition. Wait until the clock goes to 0V (l.e.d. off) and then press S3 again. This produces a logic 1 on the CLEAR line and counting should commence with the first falling ($1 \longrightarrow 0$) clock pulse. When this happens (at the point where the clock l.e.d. goes off again), D4 should become illuminated indicating a count of 0001 (binary 1). After the next clock pulse, and again on the falling edge, the count should increase by 1 to 0010 (binary 2). Note that all changes are initiated on the falling edge of the clock pulse. Carefully observe the subsequent binary counting sequence and confirm that the arrangement follows the timing diagram shown in Fig. 7.18 and the logic state table shown below:

Clock pulse number	Q4	Q3	Q2	Q1
0 (reset)	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

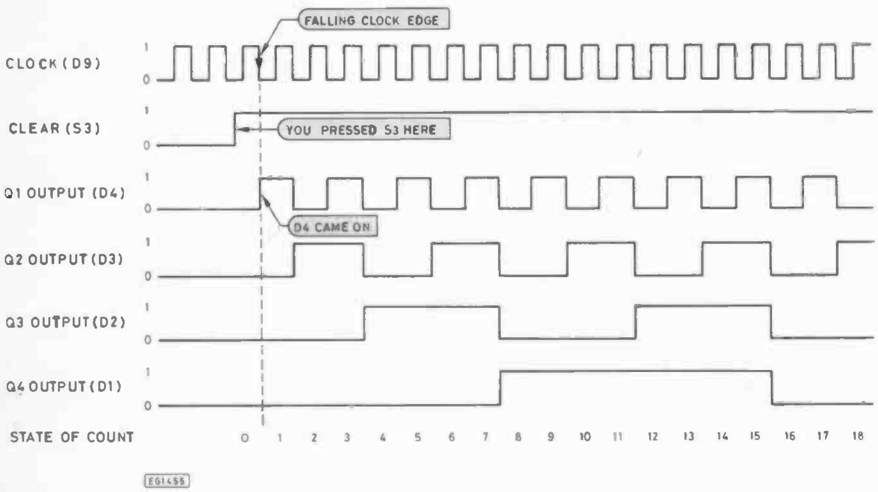


Fig. 7.18. Timing diagram for the four-stage binary divider of Fig. 7.17

The counting sequence should then recommence with 0000. At any time, however, it should be possible to interrupt the counting sequence using S3 to reset the count to 0000.

DECADE COUNTERS

In many applications we require counters which are capable of counting to a base other than a power of 2. We might, for example, be concerned with packing items into boxes in batches of six, ten or twelve. At a particular stage in the process a counter would be required to check that the correct number of items are present before sealing the boxes. In order to do this, we can easily modify the basic binary counter such that a reset signal is automatically generated to clear the counter when a specific state of count has been reached.

Taking the decade counter (÷10) as an example, let us imagine that an electrical component manufacturer produces 13A plugs using a simple automated assembly line. After the assembly process is complete, each plug is visually inspected on a moving conveyor belt, before being passed to the packing machine. The machine arranges the plugs into batches of ten and then seals them into a plastic container in which the wholesaler receives the plugs.

After inspection, the plugs can be detected by a photocell as they arrive at the packing machine. The photocell can be arranged such that, after suitable processing, a $0 \rightarrow 1 \rightarrow 0$ pulse is produced as each plug passes by. This pulse is fed to the clock input of a counter which counts to ten before activating the heat-shrink sealing process. The state of the count corresponding to 10 (binary 1010) can be easily detected using a logic gate which not only initiates the sealing process but also resets the counter to zero (binary 0000). The counter is thus made ready for the next batch of 10 plugs.

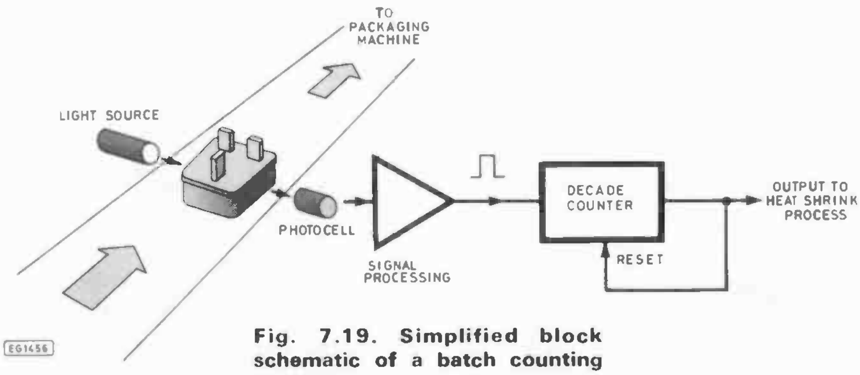
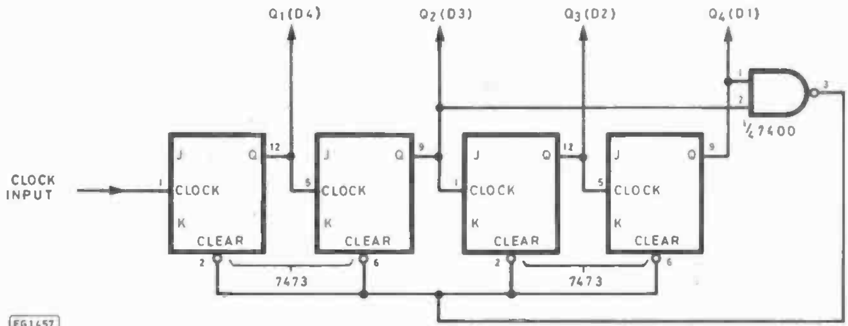


Fig. 7.19. Simplified block schematic of a batch counting system

The process is shown in block schematic form in Fig. 7.19. The circuit of a typical decade counter is shown in Fig. 7.20. This arrangement uses a two-input NAND gate to detect the count of 10 (binary 1010). Note that this is only a transitory state and the counter will be immediately cleared whenever Q2 and Q4 are both at logic 1. The counter thus has ten states (0 to 9) and counting will recommence with an output of 0000 immediately after resetting.

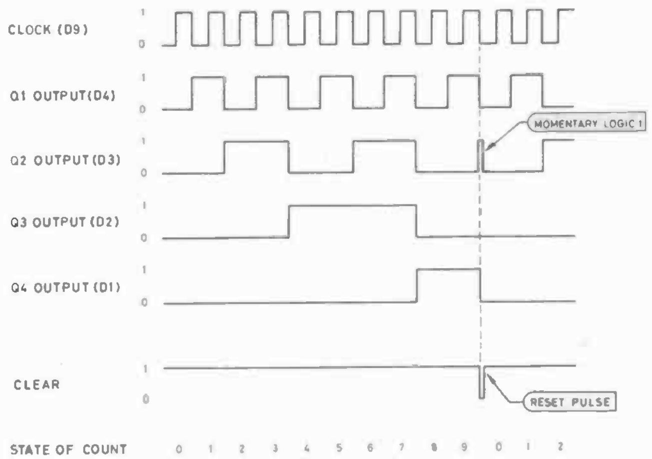
The ÷16 arrangement using two 7473's can easily be modified for use as a decade counter by adding an additional 7400 (fitted in socket C) and making the following links:

C1 to D1
C2 to D3
C3 to B6 (remove the link from S3 to B6)



EG1457

Fig. 7.20. Typical decade counter (NB All J and K inputs are taken to logic 1)



EG1458

Fig. 7.21. Timing diagram for the decade counter of Fig. 7.20

C7 to 0V (0V)
C16 to +5V (positive supply)
(New total of 28 links)

The decade counter should follow the timing diagram shown in Fig. 7.21 and obey the logic state table shown below:

Clock pulse number	Q4	Q3	Q2	Q1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10 (0)	0	0	0	0
11 (1)	0	0	0	1
12 (2)	0	0	1	0
13 (3)	0	0	1	1
etc.	etc.			

Please Note

In Part 6 Table 6.8 should refer to Fig. 6.8 and Table 6.9 should refer to Fig. 6.9. Table 6.10 should be ignored.

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4.7 16V 18p
4.7 25V 20p
6.8 25V 20p
6.8 35V 21p
10 16V 18p
10 35V 27p
15 10V 22p
15 16V 30p
15 25V 32p
22 6.3V 26p
22 16V 29p
33 10V 30p
47 3V 14p
47 6.3V 34p
47 16V 39p
100 3V 32p
100 3V 55p
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µFd	V	
.47	63	8p
.47	100	9p
.47	350	30p
1	63	8p
1	100	9p
1	500	40p
2.2	25	8p
2.2	63	9p
2.2	100	11p
2.2	350	30p
3.3	25	10p
3.3	40	11p
3.3	63	12p
4.7	16	8p
4.7	25	9p
4.7	40	11p
4.7	63	12p
4.7	100	14p
10	25	8p
10	40	12p
10	63	14p
10	100	19p
10	350	55p
22	25	11p
22	40	14p
22	63	16p
22	100	21p
47	25	14p
47	40	17p
47	63	26p
47	100	28p
100	16	14p
100	25	16p
100	40	22p
100	63	25p
100	100	30p
220	10	16p
220	16	17p
220	25	22p
220	40	25p
220	63	30p
220	100	40p
470	16	22p
470	25	28p
470	40	33p
470	63	43p
470	100	60p
1000	16	30p
1000	25	38p
1000	40	46p
1000	63	65p
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2200	40	70p
2200	63	1.34p
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µFd	V	
10	16	6p
22	10	6p
22	16	7p
47	10	7p
47	16	8p
100	10	9p
100	16	10p
100	25	11p
220	10	12p
220	16	17p
470	10	18p
470	16	20p
1000	10	24p
1000	16	34p
2200	10	44p
2200	16	44p
3300	10	50p
3300	16	65p
4700	10	65p
4700	16	95p

74TTL

7400 7401 7402 7403 7404 7405 7408 7409 7410 7411 7412 7413 7414 7416 7417 7420 7421 7422 7423 7425 7426 7427 7428 7430 7432 7433 7437 7438 7440 7441 7442 7443 7444 7445 7446 7447 7448 7450 7451 7453 7454 7460 7470 7472 7473 7474 7475 7476 7480 7481 7482 7483 7484 7485 7486 7489 7490 7491 7492 7493 7494 7495 7496 7497 74100 74104 74105 74107 74109 74110 74116 74118 74119 74120 74121 74122 74123 74125 74126 74128 74132 74136 74141 74142 74143 74144 74145 74147 74148 74150 74151 74153 74154 74155 74156 74157 74159 74160 74161 74162 74163 74164 74165 74166 74170 74172 74173 74174 74175 74176 74177 74178 74180 74181 74182 74184 74185 74186 74188 74190 74191 74192 74193 74194 74195 74196 74197 74198 74199 74221

74LS TTL

74LS00 74LS01 74LS02 74LS03 74LS04 74LS05 74LS08 74LS10 74LS11 74LS12 74LS13 74LS14 74LS15 74LS20 74LS21 74LS22 74LS27 74LS28 74LS30 74LS32 74LS33 74LS37 74LS38 74LS40 74LS42 74LS47 74LS51 74LS54 74LS55 74LS73 74LS74 74LS75 74LS76 74LS78 74LS83 74LS85 74LS86 74LS90 74LS92 74LS93 74LS95 74LS96 74LS107 74LS109 74LS112 74LS113 74LS114 74LS122 74LS123 74LS124 74LS125 74LS126 74LS132 74LS136 74LS138 74LS139 74LS145 74LS147 74LS148 74LS151 74LS153 74LS154 74LS155 74LS156 74LS157 74LS158 74LS160 74LS161 74LS162 74LS163 74LS164 74LS165 74LS168 74LS169 74LS170 74LS173 74LS174 74LS175 74LS181 74LS183 74LS190 74LS191 74LS192 74LS193 74LS194 74LS195 74LS196 74LS197 74LS221 74LS240 74LS241 74LS242 74LS243 74LS244 74LS245 74LS247 74LS248 74LS249 74LS251 74LS253 74LS257 74LS258 74LS259 74LS261 74LS266 74LS273 74LS275 74LS279 74LS280 74LS283 74LS289 74LS290 74LS293 74LS295 74LS298 74LS299 74LS323 74LS324 74LS325 74LS326 74LS327 74LS347 74LS348 74LS352 74LS353 74LS362 74LS365 74LS366 74LS367 74LS368 74LS373 74LS378 74LS386 74LS390 74LS393 74LS395 74LS396 74LS398 74LS399 74LS445 74LS490 74LS540 74LS541 74LS640 74LS641

CMOS

4000	16p
4001	16p
4002	16p
4006	49p
4007	19p
4008	32p
4009	24p
4010	24p
4011	16p
4012	19p
4013	19p
4014	46p
4015	39p
4016	19p
4017	32p
4018	39p
4019	24p
4020	42p
4021	39p
4022	39p
4023	19p
4024	32p
4025	19p
4026	79p
4027	28p
4028	39p
4029	43p
4030	19p
4031	1.19
4032	79p
4033	1.19
4034	1.29
4035	44p
4036	2.49
4037	1.13
4038	99p
4039	2.45
4040	39p
4041	39p
4042	39p
4043	39p
4044	39p
4045	99p
4046	44p
4047	69p
4048	39p
4049	22p
4050	23p
4051	44p
4052	58p
4053	49p
4054	79p
4055	83p
4056	83p
4059	4.35
4060	42p
4063	79p
4066	22p
4067	2.39
4068	19p
4069	19p
4070	19p
4071	19p
4072	19p
4073	19p
4075	19p
4076	45p
4077	19p
4078	19p
4081	19p
4082	19p
4085	49p
4086	60p
4089	1.23
4093	19p
4094	69p
4095	71p
4096	69p
4097	2.88
4098	74p
4099	89p
4502	55p
4503	39p
4507	33p
4508	1.26
4510	44p
4511	44p
4512	48p
4514	1.13
4515	1.13
4516	55p
4518	39p
4519	29p
4520	48p
4521	88p
4526	68p
4527	62p
4528	74p
4532	69p
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Z80ACTC	2.60
Z80ADART	5.50
Z80ADMA	6.70
Z80APIO	2.70
ZN426E8	2.99
ZN427E8	5.99

V.REGS

Positive 100mA

78L05A	29p
78L12A	29p
78L15A	29p
78L24A	29p

1 Amp TO202

7805T	45p
78121	45p
7815T	45p
7824T	45p

Negative 100mA TO92

79L05	49p
79L12	49p
79L15	49p

1 Amp TO220

7905T	57p
7912T	57p
7915T	57p
7924T	57p

TRANSISTORS

2N2219	27p
2N2219A	28p
2N2220	22p
2N2221	22p
2N2221A	23p
2N2222	24p
2N2222A	25p
2N2223	2.60
2N2223A	4.15
2N2368	25p
2N2369	19p
2N2369A	20p
2N2904A	27p
2N2905	28p
2N2905A	29p
2N2906	25p
2N2906A	30p
2N2907	25p
2N2907A	26p
2N2920	9.25
2N2926	10p
2N3053	27p
2N3054	56p
2N3055	60p
2N3055H	1.20
2N3439	98p
2N3440	80p
2N3441	1.25
2N3442	1.35
2N3553	2.65
2N3638	55p
2N3702	10p
2N3703	10p
2N3704	10p
2N3705	10p
2N3706	10p
2N3707	10p
2N3708	10p
2N3709	10p
2N3710	10p
2N3711	10p
2N3712	2.00
2N3713	1.38
2N3714	2.98
2N3715	3.31
2N3716	3.60
2N3773	1.99
2N3819	35p
2N3820	68p
2N3866	90p
2N3903	13p
2N3904	13p
2N3905	13p
2N3906	13p
2N4030	75p
2N4031	65p
2N4032	69p
2N4036	63p
2N4037	49p
2N4240	3.00
2N4400	15p
2N4401	27p
2N4402	20p
2N4902	1.85
2N4903	1.98
2N4904	2.15
2N4905	2.75
2N4906	2.99
2N4907	3.20
2N4908	3.15
2N4909	2.90
2N5089	37p
2N5190	68p
2N5191	70p
2N5193	90p
2N5194	79p
2N5245	37p
2N5246	40p
2N5247	45p
2N5248	40p
2N5249	48p
2N5266	2.88
2N5293	98p
2N5294	1.28
2N5295	1.37
2N5401	35p
2N5415	1.10
2N5416	1.54
2N5447	16p
2N5448	19p
2N5449	21p
2N5450	20p
2N5451	25p
2N5457	29p
2N5458	29p
2N5459	29p
2N5460	72p
2N5551	37p
2N5884	5.95
2N5886	5.95
2N6121	57p
2N6122	59p
2N6123	65p
2N6124	59p
2N6125	65p
2N6129	75p
2N6130	93p
2N6131	98p
2N6132	83p
2N6133	1.14
2N6134	1.38
2N6253	1.45
2N6254	1.55
2SC1306	95p
2SC2078	1.75
2SJ49	3.95
2SJ50	4.50
2SJ82	3.95
2SK134	3.95
2SK135	4.50
2SK226	4.75
3N128	1.12
3N140	1.07
3N200	6.93
3N201	2.98
40360	60p
40361	67p
40362	67p
40363	2.95
40406	1.39
40407	75p
40408	1.59
40409	1.80
40410	1.80
40411	3.95
40412	90p
40673	70p
40822	1.80
40871	1.00
40872	1.00
AC125	49p
AC126	32p
AC127	32p
AC128	35p
AC132	68p
AC141K	28p
AC142K	28p
AC151	51p
AC152	45p
AC153	55p
AC153K	64p
AC176	27p
AC176K	37p
AC187	25p
AC187K	28p
AC188	25p
AC188K	40p
AF239	55p
AF240	1.00
BC107	10p
BC107A	12p
BC107B	12p
BC108	10p
BC108A	12p
BC108B	12p
BC108C	14p
BC109	10p
BC109B	12p
BC109C	12p
BC140	29p
BC141	27p
BC142	29p
BC143	30p
BC147	10p
BC147A	10p
BC147B	10p
BC147C	20p
BC148	10p
BC148A	12p
BC148B	13p
BC148C	13p
BC149	10p
BC149B	12p
BC149C	13p
BC152	35p
BC153	23p
BC154	27p
BC157	11p
BC157A	12p
BC157B	13p
BC158	10p
BC158A	12p
BC158B	13p
BC159	11p
BC159A	12p
BC159B	13p
BC159C	13p
BC160	42p
BC161	48p
BC167	10p
BC167A	12p
BC167B	13p
BC168	10p
BC168B	10p
BC168C	10p
BC169	10p
BC169B	10p
BC169C	10p
BC177	16p
BC177A	25p
BC177B	26p
BC178	24p
BC178A	20p
BC178B	25p
BC179	25p
BC179A	25p
BC179B	25p
BC179C	27p
BC182	10p
BC182A	12p
BC182B	13p
BC182L	10p
BC182LA	12p
BC182LB	14p
BC183	10p
BC183A	11p
BC183B	12p
BC183C	13p
BC183L	10p
BC183LA	13p
BC183LB	13p
BC183LC	14p
BC184	10p
BC184B	12p
BC184C	13p
BC184L	10p
BC184LB	13p
BC184LC	14p
BC186	24p
BC187	24p
BC212	10p
BC212A	12p
BC212B	13p
BC212L	10p
BC212LA	13p
BC212LB	14p
BC213	10p
BC213A	11p
BC213B	12p
BC213C	13p
BC213L	10p
BC213LA	13p
BC213LB	13p
BC213LC	14p
BC214	10p
BC214B	12p
BC214C	13p
BC214L	10p
BC214LB	13p
BC214LC	14p
BC237	16p
BC237A	16p
BC237B	17p
BC237C	17p
BC238	18p
BC238A	15p
BC238B	16p
BC238C	17p
BC239	17p
BC239A	15p
BC239B	17p
BC239C	18p
BC300	45p
BC301	44p
BC302	47p
BC303	14p
BC327	14p
BC328	14p
BC337	15p
BC338	15p
BC440	32p
BC441	33p
BC460	32p
BC461	33p
BC516	40p
BC517	40p
BC546B	15p
BC547	13p
BC556B	15p
BC547A	14p
BC547B	14p
BC548	12p
BC548A	13p
BC548B	14p
BC548C	15p
BC549	13p
BC549B	14p
BC549C	15p
BC550	15p
BC550C	25p
BC557	15p
BC557A	16p
BC557B	16p
BC558	15p
BC558A	16p
BC558B	16p
BC558C	17p
BC559	15p
BC559B	16p
BC559C	17p
BC560	25p
BC560C	25p
BC650	45p
BC651	46p
BCY70	16p
BCY72	19p
BD131	44p
BD132	44p
BD135	35p
BD136	35p
BD137	37p
BD138	37p
BD139	38p
BD140	38p
BD237	98p
BD238	98p
BD239A	57p
BD239C	64p
BD240A	59p
BD240C	73p
BD241A	61p
BD241C	65p
BD242A	70p
BD242C	72p
BD243A	80p
BD243C	85p
BD244A	82p
BD244C	1.00
BD245A	1.14
BD245C	1.20
BD246A	1.30
BD246C	1.50
BD249A	2.00
BD250A	2.31
BD250C	2.46
BD419	1.29
BD420	1.37
BD437	88p
BD438	88p
BD439	90p
BD440	91p
BD441	91p
BD442	93p
BD529	1.20
BD530	1.30
BD535	75p
BD536	75p
BD537	80p
BD538	80p
BD539	80p
BD539C	1.00
BD540	85p
BD540C	1.10
BD675	1.20
BD676	77p
BD677	78p
BD678	83p
BD711	1.32
BD712	1.32
BDX32	3.47
BDX66B	5.95
BDX67B	5.95
BDY54	1.70
BDY55	1.75
BDY56	1.80
BDY57	5.25
BDY58	6.15
BF194	12p
BF195	12p
BF196	12p
BF197	12p
BF198	15p
BF199	15p
BF200	15p
BF224J	32p
BF225J	35p
BF244A	55p
BF244B	55p
BF245A	55p
BF245B	65p
BF246	70p
BF246A	70p
BF246B	70p
BF247A	75p
BF247B	75p
BF254	42p
BF255	28p
BF256A	58p
BF256B	58p
BF256C	65p
BF257	30p
BF258	32p
BF259	35p
BF451	46p
BF458	56p
BF459	62p
BF469	86p
BF470	86p
BFR39	25p
BFR41	25p
BFR79	25p
BFR80	25p
BFR81	25p
BFR90	2.11
BFS28	2.95
BFS61	1.00
BFS98	1.00
BFX29	26p
BFX30	27p
BFY50	23p
BFY51	23p
BFY52	23p
BFY53	31p
BSX19	24p
BSX20	24p
BSX21	40p
BU104	2.22
BU105	1.70
BU108	3.95
BU109	3.29
BU126	1.47
BU204	2.25
BU205	1.75
BU206	1.89
BU208	1.98
BU226	3.95
BU326S	2.35
BU406	1.45
BU407	1.45
BU408	1.35
BU500	2.95
BUY18S	3.95
E430	5.95
J300	70p
J310	70p
MJ802	3.99
MJ900	2.90
MJ901	3.10
MJ1000	2.50
MJ1001	3.00
MJ1800	3.60
MJ2500	2.19
MJ2501	2.25
MJ2955	1.00
MJ3000	2.19
MJ3001	2.25
MJ4502	3.99
MJ15003	4.85
MJ14004	5.55
MJ15015	2.45
MJ15016	3.34
MJE340	53p
MJE350	1.50
MJE2955	1.95
MJE3055	1.95
MJE2955T	99p
MJE3055T	69p
MPSA05	25p
MPSA06	25p
MPSA12	29p
MPSA13	48p
MPSA14	49p
MPSA16	30p
MPSA18	65p
MPSA20	48p
MPSA42	49p
MPSA43	49p
MPSA55	28p
MPSA56	30p
MPSA65	40p
MPSA66	47p
MPSA70	45p
MPSA92	39p
MPSA93	39p
MPSL01	46p
MPSL51	49p
MPSU01	84p
MPSU04	1.32
MPSU05	55p
MPSU06	56p
MPSU07	1.05
MPSU51	88p
MPSU55	58p
MPSU56	59p
MPSU57	1.20
MPS6532	1.65
TIP29A	29p
TIP29C	38p
TIP30A	35p
TIP30C	36p
TIP31A	33p
TIP31C	36p
TIP32A	38p
TIP32C	42p
TIP33A	65p
TIP33C	78p
TIP34A	74p
TIP34C	80p
TIP35A	1.09
TIP35C	1.28
TIP36A	1.29
TIP36C	1.39
TIP41A	49p
TIP41C	55p
TIP42A	50p
TIP42C	55p
TIP49	79p
TIP50	1.40
TIP53	1.57
TIP54	1.59
TIP110	74p
TIP112	90p
TIP115	81p
TIP117	96p
TIP120	73p
TIP122	80p
TIP125	84p
TIP127	88p
TIP130	93p
TIP132	93p
TIP135	99p
TIP137	99p
TIP140	1.04
TIP142	1.34
TIP145	1.15
TIP147	4.95
TIP2955	77p
TIP3055	70p
TIS43	50p
TIS88A	40p
VN10KM	60p
VN46AF	95p
VN66AF	99p
ZTX107	10p
ZTX108	10p
ZTX109	12p
ZTX300	13p
ZTX301	15p
ZTX302	19p
ZTX303	20p
ZTX310	35p
ZTX311	35p
ZTX312	32p
ZTX313	36p
ZTX314	35p
ZTX320	35p
ZTX330	35p
ZTX341	35p
ZTX450	39p
ZTX500	14p
ZTX501	14p
ZTX502	14p
ZTX503	17p
ZTX504	24p
ZTX510	24p
ZTX530	24p
ZTX531	25p
ZTX550	45p

DIODES

1N34A	30p
1N821	70p
1N823	92p
1N914	4p
1N916	6p
1N4001	4p
1N4002	4½p
1N4003	5p
1N4004	5½p
1N4005	6p
1N4006	6½p
1N4007	7p
1N4009	20p
1N4148	3p
1N4150	18p
1N4448	22p
1N5400	12p
1N5401	13p
1N5402	14p
1N5404	16p
1N5406	18p
1N5407	19p
1N5408	20p
1N5024	52p
1S44	10p
BA102	25p
BA115	25p
BA133	40p
BA138	30p
BA142	20p
BA155	15p
BA156	38p
BA157	25p
BA158	30p
BA150	32p
BA182	40p
BA201	18p
BA202	26p
BA316	25p
BA317	28p
BA318	30p
BAV10	16p
BAV19	15p
BAV20	15p
BAX13	10p
BB109G	65p
BY126	11p
BY127	12p

SCR's, TRIACS DIACS

THYRISTORS 4, 8 & 12 Amps Texas TO220
Suffix A 100V
B 200V
C 300V
D 400V
M 600V

TIC106A	46p
TIC106B	47p
TIC106C	48p

4A

TIC106D	49p
TIC106M	68p
TIC116A	66p
TIC116B	68p

8A

TIC116C	71p
TIC116D	73p
TIC116M	80p
TIC126A	72p
TIC126B	72p

12A

TIC126C	73p
TIC126D	77p
TIC126M	96p

TRIACS Texas 400V TO220 Case

TIC206D 4A	66p
TIC225D 6A	74p
TIC226D 8A	88p
TIC236D 12A	1.16
TIC246D 16A	1.22
TIC253D 20A	1.90
TIC263D 25A	2.11

DIACS

BR100	29p
ST2	29p

ZENER'S

many inc specials see cat
400 500mW 24 Series 2.4-47V 7p
1.3 Watt E24 Series 3.3-82V 14p

BRIDGE

(PIV shown in brackets) 1 amp type

WC1 (100)	28p
WG2 (200)	34p
WG4 (200)	38p
WG8 (800)	50p

2 amp type Square with hole

S0 (100)	46p
S02 (200)	50p
S04 (400)	55p
S08 (800)	66p

6 amp type Square with hole

PW01 (100)	95p
PW02 (200)	99p
PW04 (400)	1.30
PW06 (600)	1.39

25 amp type Metal clad with hole

KO1 (100)	2.62
KO2 (200)	2.75
KO4 (400)	3.25
KO6 (600)	4.10
BYW64	
35A 400V	4.50

OPTO

many inc specials see our CAT

LED LAMPS
R - Red
G - Green
Y - Yellow
Large Diffused

R5C	1
R5D	9p
G5D	15p
Y5D	15p

Small diffused

R3D	8p
G3D	12p
Y3D	12p

Micro 0.1

R1M	25p
G1M	27p
Y1M	27p

Large clear

R5C	12p
G5C	17p
Y5C	17p

Super bright high efficiency Large (100 times brighter)

R5U	38p
G5U	42p
Y5U	42p

Rectangular Stackable LEDs

R5R	17p
G5R	18p
Y5R	19p

LIN ICS

AY1 5050	95p
AY3 8910	3.99
AY3 8912	4.95
CA3048	2.15
CA3059	2.80
CA3090AQ	3.70
CA3130E	87p
CA3130T	2.35
CA3140E	39p
CA3140T	1.40
HA1366W	2.40
HA388	2.54
ICL7106	7.50
ICL7107	9.50
ICL7611	97p
ICL8038	2.99
ICM7555	80p
ICM7556	1.50
LC7120	3.20
LC7130	3.40
LC7137	3.95
LF347	1.50
LF351	47p
LF353	92p
LF355	83p
LF356	92p
LF357	1.30
LF398	4.62
LM3352	1.60
LM348N	62p
LM349N	1.09
LM350K	4.60
LM379S	5.10
LM380N14	75p
LM380N8	1.50
LM381AN	2.26
LM381N	1.40
LM382N	1.12
LM383T	3.25
LM384N	1.40
LM386	88p
LM388N	2.43
LM391N60	2.10
LM391N80	2.40
LM723CH	95p
LM723CN	35p
LM725CH	3.40
LM725CN	3.19
LM741CH	96p
LM741CN	18p
LM741CN14	80p
LM747CN	69p
LM748CH	1.00
LM748CN	35p
LM1871	3.25
LM1872	4.39
LM1877	5.95
LM1886	7.44
LM1889	3.77
LM2907N	2.75
LM2907N8	2.60
LM2917N	2.40
LM2917N8	2.40
LM3900	48p
LM3911	1.20
LM3914	3.25
LM3915	3.25
LM13600	1.15
MF10	3.50
NE531N	1.36
NE543N	2.00
NE544N	1.95
NE555	18p
NE556	65p
NE558	1.89
NE560	3.25
NE565	1.18
NE566	1.49
NE567	1.37
NE570	4.07
NE571	3.99
NE5534A	1.45
RC4194	3.95
RC4195	2.95
RC4558	44p
SL470	3.47
SL480	2.99
SL490	3.47
SN76003	2.95
SN76013	2.95
SN76023	2.95
SN76033	2.95
TA7204	1.99
TA7205	1.20
TA7222	1.75
TA7227	5.82
TBA500	2.97
TBA500Q	3.11
TBA510	2.95
TBA510Q	3.05
TBA520	2.57
TBA520Q	2.75
TBA530	2.55
TBA530Q	2.76
TBA540	2.72
TBA540Q	2.74
TBA550	3.25
TBA5500	3.27
TBA560C	2.87
TBA570	2.37
TBA5700	2.48
TDA1002	3.39
TDA1003	3.94
TDA1004	3.94
TDA1005	3.94
TDA1010A	2.25
TDA1022	4.95
TDA2002	3.25
TDA2003	3.25
TDA2020	2.99
TDA2030	2.85
TDA2611A	2.50
TDA7000	3.45
TL061	40p
TL062	60p
TL064	1.35
TL071	34p
TL072	45p
TL074	1.35
TL081	34p
TL082	45p
TL084	1.20
UAA170	2.49
UAA180	2.49
ULN2003	75p
UPC575C2	2.00
UPC1156	2.75
UPC1156H	2.75
UPC1182	3.75
UPC1185	1.95
UPC2002	2.95
XR2206	3.95
ZN409	2.25
ZN414	1.00
ZN1034	1.99

TRANS FORMERS

All 240V Primary
6-0-6V 9.0-9V
12-0-12V
15-0-15V
100mA 95p
1A 2.65
20-0-20V
1.25A 2.65
12-0-12V
50VA 5.25
12-0-12V
100VA 9.50
0-6-6-9-9
1.25A 4.25
These goods are heavy send extra p&p We will credit any difference

VERO

0.1 COPPER TRACKS

2.5 × 3.7	83p
2.5 × 5	99p
3.75 × 3.75	99p
3.75 × 5	1.14
2.5 × 17	2.99
3.75 × 17	3.85
4.79 × 17	4.93
VQ Board	1.92
DIP Board	3.90
Track Cutter	1.48
Pin Insertor	1.79
100 Pins	55p
Veroblock	3.99
Vero Wiring Pen + Spool	3.35
Spare Spool	75p
Combs	6p

PCB

FERRIC CHLORIDE Quick dissolving Enough to make over 1 litre 1.69
ETCH RESIST TRANSFERS
1 Thin lines
2 Thick lines
3 Thin bends
4 Thick bends
5 DIL pads
6 Transistor pads
7 Dots + holes
8 0.1" edge connectors
9 Mixture
Any sheet of above 35p
GRADE ONE GLASS PCB SINGLE SIDED
178 × 240mm 150p
420 × 195mm 1.95
420 × 245mm 2.95
DALO ETCH RESIST PEN spare nib 1.20
PHOTO SENSITIVE PCB 1st Class Epoxy Glass For better results than spraying Expose to UV

Single sided

100 × 160	2.10
100 × 220	2.50
203 × 114	2.40
233 × 220	5.20

Double Sided

100 × 160	2.10
100 × 200	2.80
203 × 114	2.90
233 × 220	5.90

Developer for above (do not use Sodium Hydroxide) 500ml 2.95

WIRE

PRICES PER METRE
Solid connecting wire
MAINS SPEAKER
Twin 1 Amp 14p
Twin 2½ Amp 16p
3 Core 2½ Amp 18p
3 Core 6 Amp 31p
3 Core 13 Amp 56p
SCREENED
Single 14p
Stereo 27p
Mini Single 12p
Mini Stereo 15p
4 Core 4 Screens 44p
4 Core, Single Screen 54p
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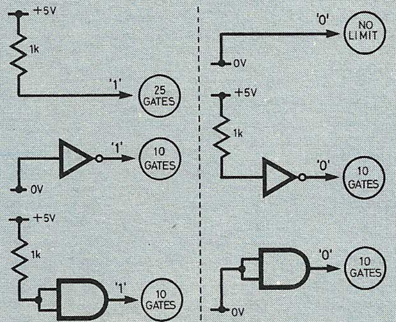
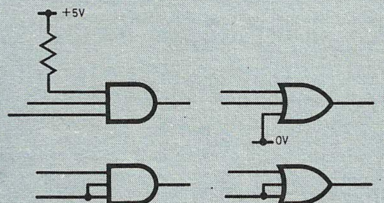
LOGIC SOURCES

The standard TTL levels for 0 and 1 are well defined. In many cases, a circuit will need to use one of these levels to either prevent or ensure particular circuit behaviour, e.g. to be certain that the RESET input of a latch is kept inactive. A logic 0 or 1 source (as appropriate) is then used to drive the appropriate gate input. Some of the standard ways of generating logic 0 and logic 1 are shown below. Also included is the number of standard TTL gates which can be connected to each type of source.



UNUSED INPUTS

When the input of a TTL gate is left unconnected, the gate will behave as if that input is at logic 1. However, even though a 1 may be what is logically appropriate, leaving gate inputs 'floating' makes the circuit susceptible to noise, and affects the maximum operating speed. The recommended action, therefore, is to 'tie' a floating input to an appropriate logic source. The most convenient ways of doing this use either a 1kΩ resistor between the input and +5 volt (for 1), or a direct link to 0V (for 0). Up to 25 unused inputs can be tied to logic 1 with a single resistor. For unused inputs on multi-input gates, an alternative approach is to connect them to one of the used inputs on the same gate; this will have no effect on the fan-in.



TTL SUPPLIES

TTL operates from a single +5V d.c. supply. At no time should the voltage at the i.c. supply pin exceed +7V. The supply should ideally be regulated to within 250mV of the nominal +5V, and the ripple should be less than 250mV. The greater the number of i.c.s in a circuit, the more important is the need for a well-regulated supply. When designing power supplies for TTL, there are three important requirements to be satisfied:—

★ A regulated supply of voltage.
★ Low-impedance supply distribution.
★ Effective supply decoupling.

These are all necessary characteristics if a TTL circuit's behaviour is to be unaffected by its power supply.

LOAD CURRENT

Designing a power supply unit (p.s.u.) for a TTL circuit requires a knowledge of the maximum current to be supplied. The TTL data books give supply figures in either mA or mW, quoted either per-gate or per-package. Any mW figures should first be converted to mA by dividing by 5. The total current for each package is then worked out by multiplying any per-gate figures by the number of gates in the i.c. (whether or not they are actually used). Then total up the current for all of the TTL i.c.s, and add in any other circuit loads (relays, l.e.d.s, etc.). This gives the expected overall load current for the circuit. A useful p.s.u. design current is obtained by adding a safety margin of (say) 20% to this last figure.

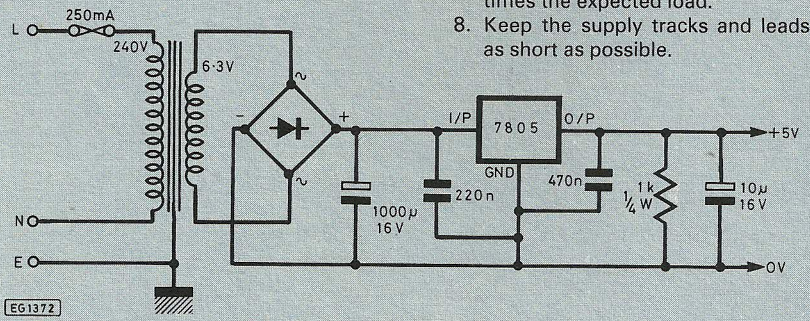
PSUs FOR TTL

The most convenient p.s.u.s for TTL essentially use a mains transformer, a bridge rectifier and an i.c. voltage regulator. This arrangement provides an extremely stable, protected supply at reasonable cost, using only a small number of readily available components. By selection of an appropriate transformer, bridge and regulator, the same circuit may be used for a wide range of applications. The circuit shown below is suitable for use with TTL circuits which impose a load of up to 1A.

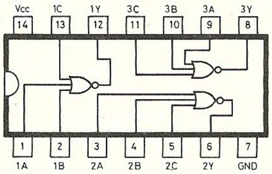
SUPPLY DISTRIBUTION

Good power distribution is essential in any TTL circuit. The power supply wiring must have a low impedance at all frequencies up to around 35MHz (125MHz for Schottky TTL). This prevents sudden bursts of high speed operation in one part of the circuit affecting another area via the power supply lines. A low impedance supply requires both good distribution and good decoupling (see later). A number of simple rules will help avoid problems with supply distribution.

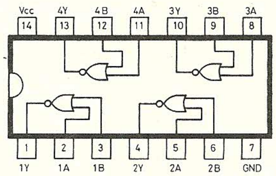
1. Use wide p.c.b. tracks for the main 0V and +5V rails.
2. The main 0V rail should ideally be at least 8mm wide.
3. The main +5V rail should ideally be at least 6mm wide.
4. Try to run the main 0V track around the edge of the board.
5. Keep connections between the i.c. and 0V short.
6. Use supply leads rated at 5–10 times the expected load.
7. Use connectors rated at 5–10 times the expected load.
8. Keep the supply tracks and leads as short as possible.



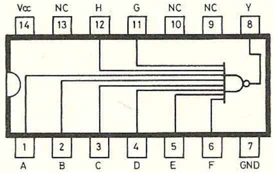
Regulators = 78L05 (0·1A), 78M05 (0·5A), 7805 (1A), LM309K (1·2A), 78H05 (5A).



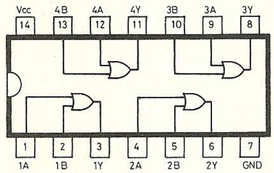
7427 Triple 2-input NOR



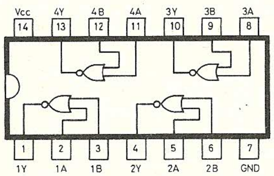
7428 Quad 2-input NOR buffer



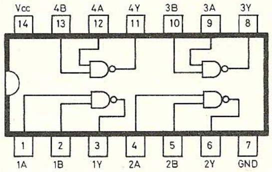
7430 8-input NAND



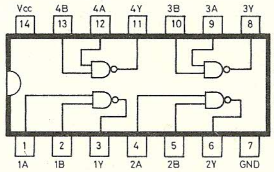
7432 Quad 2-input OR



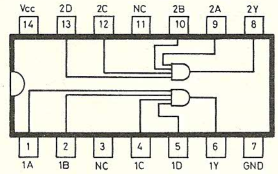
7433 Quad 2-input NOR oc



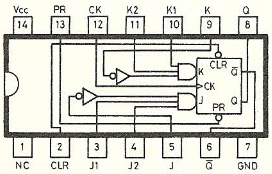
7437 Quad 2-input NAND buffer



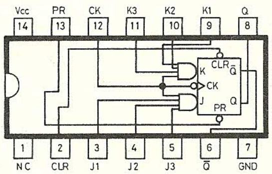
7438 Quad 2-input NAND buffer oc



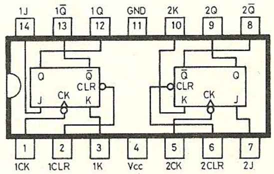
7440 Dual 4-input NAND buffer



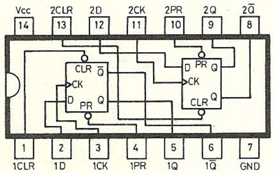
7470 J–K preset and clear



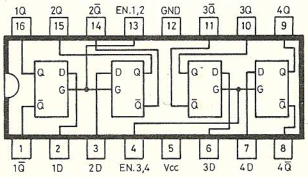
7472 J–K preset and clear



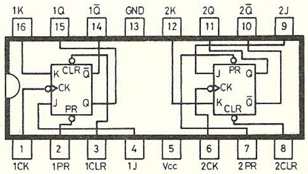
7473 Dual J–K



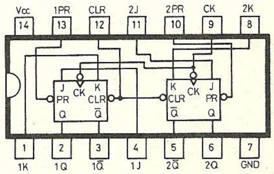
7474 Dual D-type



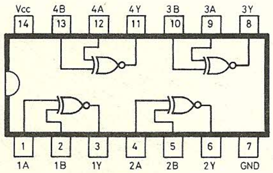
7475 Quad bistable latch with enable



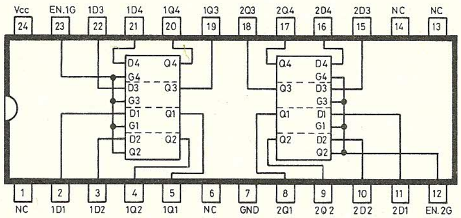
7476 Dual J–K



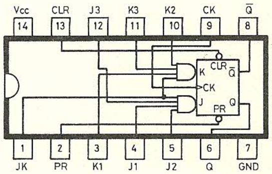
7478 Dual J–K LS



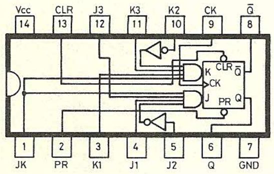
7486 Quad 2-input Ex-OR



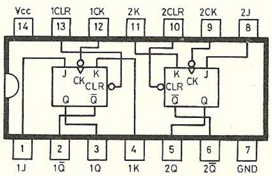
74100 Dual 4-bit latch with enable



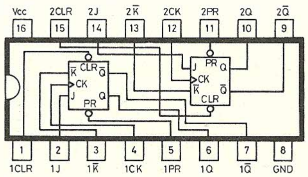
74104 Gated J–K preset and clear



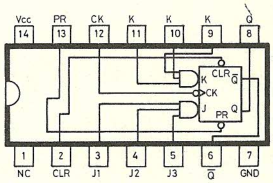
74105 Gated J–K preset and clear



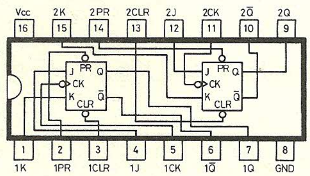
74107 Dual J–K with clear



74109 Dual J–K preset and clear



74110 J–K with data lock-out



74111 Dual J–K with data lock-out