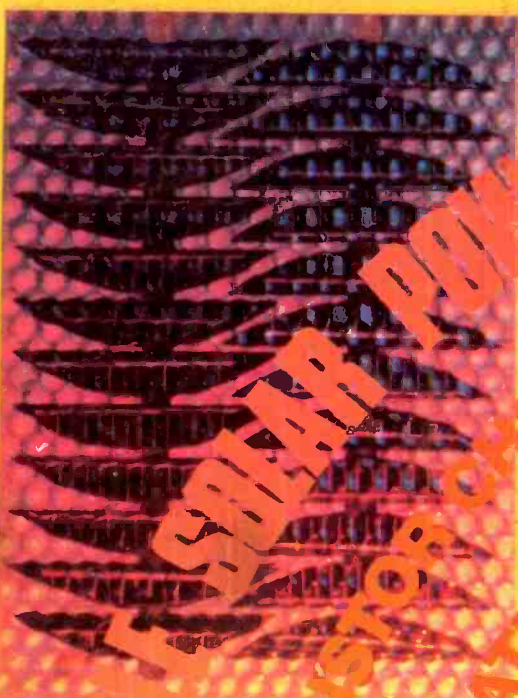
PRACTICAL
ELECTRONICS
AUGUST 1983
85p
Australia $1.50 New Zealand $1.60 Malaysia $4.95 IR £1.23 (inc. VAT)



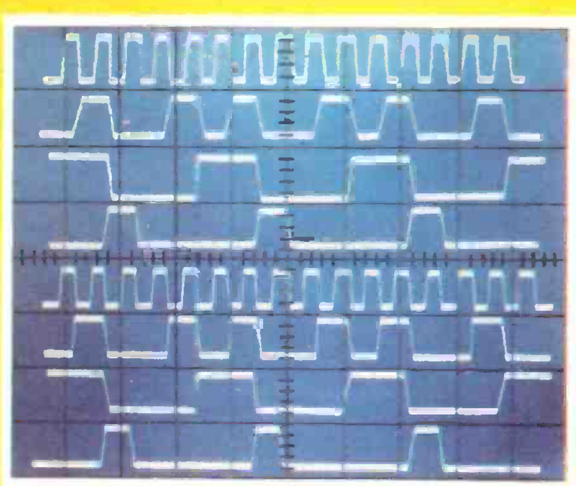
SIMPLE SOLAR POWERED PROJECTS....

TRANSISTOR CHECKER: THERMOMETER

INEBRIATION DETECTOR: RADIO

SOIL MOISTURE METER

CONTINUITY TESTER



COMPUTER DIAGNOSIS LOGIC ANALYSER Part One

ROBOT VISION

Plus! Used Computer & Equipment Bargains

Get moving with these new developments in UK Robotics

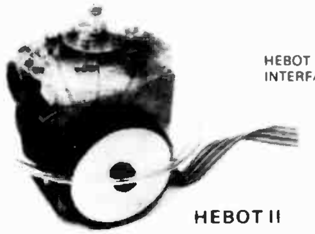
— advanced electrohydraulic designs for education, industry and now available to the home constructor.

Hebot II is a turtle-type robot which takes programming out of the two dimensional world of the VDU into the real three dimensional world. Given a DC supply of 9 15V it can perform a bewildering number of moves under computer control — forwards backwards left and right — with each wheel independently controlled. It has blinking eyes, bleeps with a choice of two tones and has a solenoid operated pen to chart its progress. Touch sensors coupled to its shell return data about its environment to the computer for it to calculate evasive or exploratory action. Hebot II connects directly to an I/O port or alternatively with the universal interface board to the expansion bus of a ZX81 or other computer.

Robotic experience is becoming as essential a subject as computing. MICROGRASP provides the lowest cost means of acquiring that experience but despite its ultra low price the robot has considerable versatility. There are 5 axes each using a servo motor and there is feedback from each of the arm movements. Control is by any computer with an expansion bus - the ZX81 being particularly suitable. Servoing is achieved with hardware on the interface board to keep programming simple and the robot is operated under BASIC commands with no computer specific software required. The interface board is memory mapped using only 64 bytes at any of 1024 switch selectable locations.

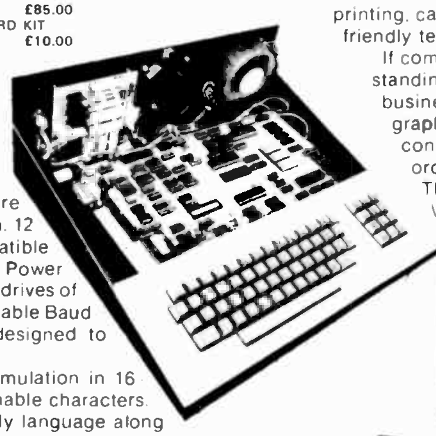
MICROGRASP robot kit with power supply	£145.00
Universal computer interface board kit	£48.50
23 way edge connector	£2.50
ZX81 peripheral RAM Pack splitter board	£3.00

MICROGRASP, INTERFACE BOARD AND ZX81



HEBOT KIT £85.00
INTERFACE BOARD KIT £10.00

HEBOT II



Up to the nano-second hard, firm and software developments embodied in a complete system. 12 Mega Hertz 16 bit CPU: 64K upwardly compatible DRAM: separate 16K video DRAM and 24K TI Power Basic with overwrite. Supports up to four Disc drives of mixed type with 16 serial I/O ports. Programmable Baud rate and comprehensive E Bus interface designed to support real world applications.

Very high resolution graphics gives 3D simulation in 16 colours on 36 prioritised planes of user definable characters. Software FORTH coming includes this trendy language along with NOS C/PM.

Hardware components available separately with details in Nov, Dec. and Jan issues of ETI. Software features include; Real time clock, full renumber command, buffered I/O to free machine whilst printing, call to machine code routines, hexadecimal support and user-friendly textual error trapping messages.

If computers interest you then the Cortex will expand your understanding infinitely more than off the shelf machines. Use it in business, education, research or just play with the incredible graphics capability. At Powertran we are using these machines in conventional roles, in product control and R & D. We shall co-ordinate the Cortex user group and distribute software for the TMS 9995 CPU. Complete 16 bit 64K computer kit **£295.00** + VAT. Complete 16 bit 64K computer ready built **£395.00** + VAT

Top of the range is the Genesis P102 which has dual speed control, continuous servo operation and double acting cylinders for increased torque on the wrist and arm rotation joints. The microprocessor based control system has additional memory, position interrogation via the RS232C interface increasing the versatility of computer control and inputs are provided for machine tool interfacing.

6 axis system READY BUILT £1950.00

Example prices and specifications

Genesis S101
Base: 19.5" × 11" × 7.5"
Lifting capacity: 1500gm
Arm lift: 6.6"
Weight: 29Kg

4 axis model in kit form	£425
5 axis model in kit form	£475

Genesis P101
Base: 19.5" × 11" × 7.5"
Lifting capacity: 2000gm
Arm lengths between axles: 14.0"
Weight: 34Kg

6 axis model in kit form	£675

Complete Systems as shown in Photograph on right

Genesis S101

4 axis system in kit form	£681.50
5 axis system in kit form	£737.50
5 axis system Ready Built	£1450

Genesis P101

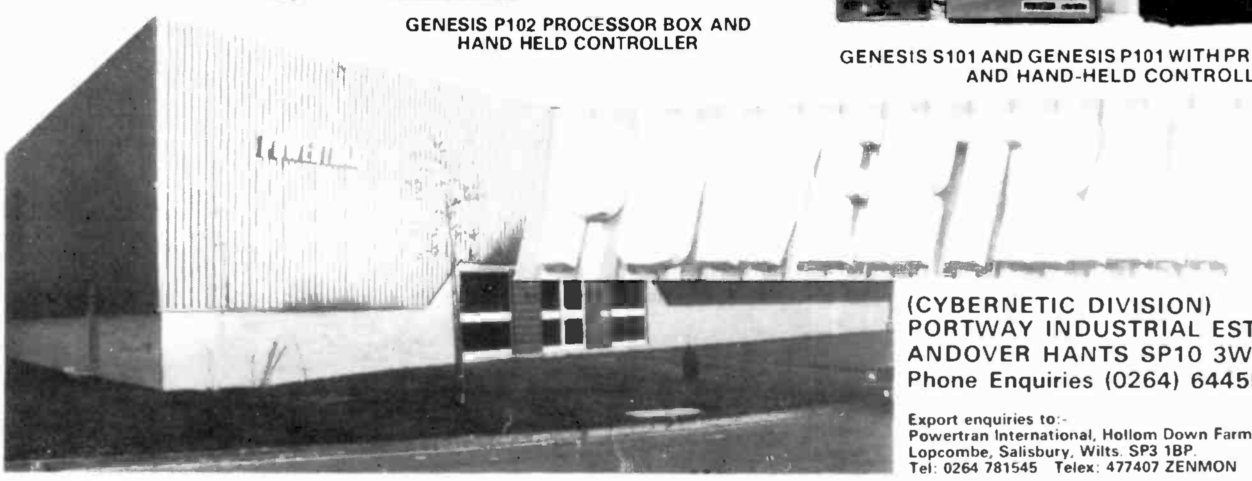
6 axis system in kit form	£945.00
6 axis system Ready Built	£1650

All prices exclusive of VAT

With prices starting below £1,000 the Genesis range of general purpose robots provide a first rate introduction to robotics for both education and industry. Each has a self-contained hydraulic power source which enables loads of several pounds to be smoothly handled. The system operated from a single phase 240 or 120V AC supply or a 12V DC supply. The machine can be supplied with up to 6 axes each of which is fully independent but capable of simultaneous operation. Position control is achieved by means of a closed-loop feedback system based around a dedicated microprocessor. Movement sequences can be entered, stored and replayed by use of a hand held controller, alternatively the systems can also be interfaced to an external computer via a standard RS 232C link.

GENESIS P102 PROCESSOR BOX AND HAND HELD CONTROLLER

GENESIS S101 AND GENESIS P101 WITH PROCESSOR BOXES AND HAND-HELD CONTROLLERS



WORLD LEADERS IN ELECTRONIC KIT DESIGN AND SUPPLY

(CYBERNETIC DIVISION)
PORTWAY INDUSTRIAL ESTATE
ANDOVER HANTS SP10 3WN
Phone Enquiries (0264) 64455

Export enquiries to:-
Powertran International, Hollom Down Farm, Lopcombe, Salisbury, Wilts. SP3 1BP.
Tel: 0264 781545 Telex: 477407 ZENMON

PRACTICAL
ELECTRONICS

VOLUME 19 **No. 8** **AUGUST 1983**

CONSTRUCTIONAL PROJECTS

GENERAL FEATURES

NEWS AND COMMENT

SPECIAL SUPPLEMENT

OUR SEPTEMBER ISSUE WILL BE ON SALE FRIDAY, AUGUST 5th, 1983
(for details of contents see page 39)

SPEAKERS

8Ω, 0.3W, 2", 2.25", 2.5", 3"	80p
0.3W, 2.5" 40Ω; 64Ω or 80Ω	80p

DIODES

AA119	15
AA129	20
AAY30	15
BA100	15
BAX13	20
BY100	24
BY126	12
BY127	12
CRO33	250
OA9	40
OA47	12
OA70	12
OA79	15
OA81	20
OA85	15
OA90	8
OA91	8
OA95	8
OA200	8
OA202	8
1N914	4
1N916	5
1N4001/2	5
1N4003	6
1N4004/5	6
1N4006/7	7
1N4148	4
1N5401	15
1N5404	16
1N5406	17
1N5408	19
1S44	9
1S921	9
6A/100V	40
6A/400V	50
6A/800V	65

BRIDGE RECTIFIERS

(plastic case)

1A/50V	18
1A/100V	20
1A/400V	25
1A/600V	34
2A/50V	30
2A/200V	40
2A/400V	46
2A/600V	65
6A/100V	83
6A/400V	95
6A/600V	125
10A/200V	215
10A/600V	298
25A/200V	240
25A/600V	396
BY164	56
VM18	50

ZENERS

Range 2V7 to 39V 400mW **8p each**

Range 3V3 to 33V 1.3W **15p each**

VARICAPS

MVAM2	165
BA102	30
BB105B	40
BB106	40

TRIACS

3A/100V	48
3A/400V	56
3A/800V	85
8A/100V	60
8A/400V	69
8A/800V	115
12A/100V	78
12A/400V	82
12A/800V	135
16A/100V	103
16A/400V	105
16A/800V	220
25A/400V	185
25A/800V	295
25A/1000V	480
30A/400V	525
T2800D	120

SOLDERCON PINS

100	75p
500	370p

SCR's Thyristors

0.8A-100V	32
5A/300V	38
5A/400V	40
5A/600V	48
8A/300V	60
8A/600V	95
12A/100V	78
12A/400V	95
12A/800V	188
BT106	150
BT116	180
C106D	38
TIC44	24
TIC45	29
TIC47	35
2N5064	38
2N4444	130

DIAC

ST2	25

OPTO

LEDS price includes Clips

TIL209 Red 3mm	10
TIL211 Green 3mm	14
TIL212 Yellow	14
TIL220 .2" Red	12
0.2" Yel, Grn, Amber	14
Rectangular LEDs with two part clip, R, G & Y	29
Rectangl. Stackable LEDS	18
Triangular LEDs R&G	18
0.2" Flashing LED Red	56
0.2" Bi colour LEDs Red/Green	65
Green/Yellow	80
0.2" Tri colour LEDs Red/Green/Yellow	85
0.2" Red High Bright	59
LD271 Infra Red (emit)	46
TIL32 Infra Red (emit)	52
SFH205 (detector)	118
TIL78 (detector)	54
TIL38	45
TIL81	82
TIL100	90

0.6" LIQUID CRYSTAL DISPLAYS

3½ digit	496
4 digit	530
6 digit	625
BPX25	195
BPW21	295
IL74	48
ILD74	99
ILQ74	185
TIL111	75
OCP71	120
ORP12	78
2N5777	45
4N33	135
Pin diode	610
Schmitt Receiver	620

OPTO SWITCH

Reflective TIL139	170
Slotted similar to RS	186

7 Segment Displays

TIL321 .5" C.An	115
TIL322 .5" C.th	115
DL704 .3" C.Cth	99
DL707 .3" C.Anod	99
FND357 or 500	120
.3" Green C.A.	140
±1 .3" Red or Green	150
Bargraph 10 seg. Red	225
Bargraph NSM3914	500

ALUM.BOXES

4×2½×2"	85
4×2½×2½"	103
4×4×2½"	120
5×4×2"	105
5×2½×1½"	90
5×2½×2½"	130
5×4×1½"	99
5×4×2½"	120
6×4×2"	120
6×4×3"	150
7×5×3"	180
8×6×3"	210
10×4½×3"	240
10×7×3"	275
12×5×3"	260
12×8×3"	295

FERRIC CHLORIDE

Crystals 1lb

195p + 50p p&p

DALO ETCH RESIST

Pen plus spare tip 100p

COPPER CLAD BOARDS

Fibre Glass	Single-sided	Double-sided	SRBP 9.5"x8.5"
6"×6"	100p	125p	110p
6"×12"	175p	225p	

VEROBOARDS 0.1"

	Clad	Plain
2½×3"	85p	—
2½×5"	100p	—
3¾×3"	100p	—
3¾×5"	115p	95p
3¾×17"	390p	275p
4¾×18"	495p	—
Pkt. of 100 pins	55p	
Spot Face Cutter	150p	
Pin Insertion Tool	185p	

'VQ' Board	180
'DIP' Board	374
Vero Strip	144

PROTO-DECs

Veroblock	405
S-Dec	350
Eurobreadboard	520
Bimboard 1	695
Superstrip SS2	£13

VERO WIRING PEN and Spool 350p

Spare Wire (Spool) 75p; Combs 6p ea.

Wire Wrapping Stakes 100 250p

VOLTAGE REGULATORS

1A T0220 Plastic Casing

	+ve		-ve	
5V	7805	40p	7905	45p
12V	7812	40p	7912	45p
15V	7815	40p	7915	45p
18V	7818	40p	7918	45p
24V	7824	40p		

100mA T092 Plastic Casing

5V	78L05	30p	79L05	60p
6V	78L62	30p	—	
8V	78L82	30p	—	
12V	78L12	30p	79L12	60p
15V	78L15	30p	79L15	60p

ICL7660	248	LM317K	320
78H05 5V/5A	550	LM317P	99
78H12 12V/5A	580	LM323K	500
		LM337T	175
78HG+5 to +24V 5A	599	LM723	35
		TBA625B	75
79HG −2.25V to −24V 5A	685	RC4194	375
LM309K	120	RC4195	160

SWITCHES

SLIDE 250V

1A DPDT	14
1A DPDT C/OFF	15
½A DP on/on/on	40

PUSH BUTTON Spring loaded

Latching or Momentary 6A	
SPDT c/over	99
DPDT c/over	145

MINIATURE Non Locking

Push to make	15p
Push break	25p

TOGGLE 2A 250V

SPST	33
DPDT	44
4 pole on off	54

SUB-MIN TOGGLE 2 amp

SP changeover	60
SPST on off	54
SPDT c/off	85
SPDT Biased	105
DPDT 6 tags	75
DPDT C/OFF	88
DPDT on/on/on	185
DPDT Biased	145
3 pole c/over	205

ROTARY: (Adjustable Stop Type) 1 pole/2 to 12 way, 2p/2 to 6 way, 3 pole/2 to 4 way, 4 pole/2 to 3 way 45p

ROTARY: Mains 250V AC. 4 Amp 64p

DIL SWITCHES: (SPST) 4 way **65p**; 6 way **80p**; 8 way **87p**; 10 way **100p**; (SPDT) 4 way **190p**.

★ SPECIAL OFFER ★

1 MEGABYTE DRIVES

Mitsubishi Slim Line, Uncased, Double track, Double density, 5¼". Track Density 96TPI, track to track Access time: 3mSec. **Only £210.**

EPSON RX80

Available from stock £295

DIL SOCKETS

	Low profile	Wire wrap
8 pin	8p	25p
14 pin	10p	35p
16 pin	10p	42p
18 pin	16p	52p
20 pin	20p	60p
22 pin	22p	65p
24 pin	25p	70p
28 pin	28p	80p
40 pin	30p	99p

ZIF DIL SOCKET

16 way	475p
24 way	575p
28 way	850p
40 way	975p

DIL PLUGS (Headers)

Pins	Solder	IDC
14	38p	95p
16	42p	100p
24	88p	138p
40	195p	218p

RIBBON CABLE (price per foot)

Ways	Grey	Colour
10	15p	28p
16	25p	40p
20	30p	50p
26	40p	65p
34	60p	85p
40	70p	90p
64	100p	135p

'D' CONNECTORS:

Pins	9 way	15 way	25 way	37 way
MALE				
Solder	80p	110p	160p	240p
Angle	150p	210p	250p	355p
Strait	170p	160p	220p	310p
FEMALE				
Solder	105p	160p	200p	338p
Angle	165p	215p	290p	440p
Strait	175p	200p	300p	420p
COVERS	80p	75p	75p	90p

IDC 25 way Plg. 385p, Skt. 450p

ULTIMUM

WATFORD'S most versatile MICRO EXPANSION SYSTEM. Interfaces with: APPLE, ATOM, DRAGON, PET, RESEARCH MACHINE, SPECTRUM, SUPERBOARD, VIDEO GENIE, ZX81, etc. As published in P.E. starting from Nov., 1982.

Send SAE for details.

IDC CONNECTORS (Speed block type)

2 rows	PCB Male with latch Strt. Pins	Angle Pins	Female Header Socket	Female Card-Edge Connector
10 way	90p	99p	85p	120p
16 way	130p	150p	110p	195p
20 way	145p	166p	125p	240p
26 way	175p	200p	150p	320p
34 way	205p	236p	169p	340p
40 way	220p	250p	190p	420p
50 way	235p	270p	200p	470p

EURO CONNECTORS

	FEMALE SOCKETS Strt.	Angle	MALE PLUGS Strt.	Angle
DIN 41617 31 way	170p	—	—	175p
DIN 41612 2×32 way	275p	320p	220p	285p
DIN 41612 2-3×32 way	295p	340p	240p	300p
DIN 41612 3×32 way	360p	385p	260p	395p

TRANSFORMERS (mains Prim. 220-240V)

3-0-3V, 6-0-6V 100mA; 9-0-9V 75mA; 12-0-12V 75mA; 15-0-15V 75mA **98p**

6VA: 2x6V-5A; 2x9V-4A; 2x12V-0.3A; 2x15V-.25A **220p**

12VA: 2x4V5-1.3A; 2x6V-1.2A; 2x12V-.5A; 2x15V-.4A **295p** (35p p&p)

24VA: 6V-1.5A 6V-1.5A; 9V-1.2A 9V-1.2A; 12V-1A 12V-1A; 15-8A 15-8A; 20V-6A 20V-6A **330p** (60p p&p)

50VA: 2x6V-4A, 2x9V-2.5A; 2x12V-2A; 2x15V-1.5A; 2x20V-1.2A; 2x25V-2A; 2x30V-0.8A **465p** (60p p&p)

100VA: 2×12V-4A; 2×15V-3A; 2×20V-2.5A; 2×30V-1.5A; 2×40V-1.25A; 2×50V-1A **920p** (60p p&p)

JUMPER LEADS Ribbon Cable Assembly

DIL Plug (Headers)

Single Ended Lead, 24" long

Length	14pin	16pin	24 pin	40 pin
24"	145p	165p	240p	325p
Double Ended Leads				
6"	185p	205p	300p	465p
12"	198p	215p	315p	490p
24"	210p	235p	345p	540p
36"	230p	250p	375p	595p

IDC FEMALE RECEPTACLE Jumper Leads 36"

	20pin	26pin	34pin	40pin
1 end	160p	200p	260p	300p
2 ends	290p	370p	480p	525p

SIL Sock-Sockets

0.1"

20 way 65p

32 way 95p

EDGE CONNECTORS

	.1"	.156"
2×10 way	—	135p
2×15 way	—	140p
2×18 way	180p	145p
2×22 way	199p	200p
2×23 way	170p	190p
2×25 way	225p	280p
2×28 way	210p	—
2×30 way	245p	—
2×36 way	295p	—
2×40 way	315p	—
2×43 way	395p	—
2×75 way	550p	—

COMPUTER CORNER

- **SEIKOSHA GP100A** – Unihammer Printer, normal & double width characters, dot resolution graphics 10" Tractor feed, parallel interface standard. **FREE 500 Sheets** **£175**
- **SEIKOSHA GP 250X** Printer **£230**
- **ORIC-I. 48K** now available. **£147**
- **JUPITER ACE** Microcomputer **£78**
- **SOFTY – 2.** The complete Microprocessor development system. New powerful instructions. Accepts any 24 pin 5V single rail EPROM. Supplied fully built & tested. **£169**
- **WEMON.** Watford's 4K Ultimate Monitor IC for Superboard & UK101. **£10**
- **ZENITH 12" Hi-RES.** Green Monitor 40/80 column select switch, value for money. **£75**
- **SANYO 14" colour monitor, RGB & V.H. sync. screened metal cabinet** **£199**
- **MICROVITEC** 14" colour monitor. RGB input. Lead incl. **£249**
- **TEX EPROM ERASER.** Erases up to 32 ICs in 15-30 min. **£33**
- **TEX EPROM ERASER** with the Solid-State 30 minute Electronic Timer. **£43**
- **SOLID STATE** 30 minute Electronic **TIMER** for above UV Erasors **£14**
- **Spare** 'UV lamp bulbs **£9**
- **POWER SUPPLY** Regulated, Variable from +5V to +15V. 4A. Fully Cased **£39**
- **MULTIRAIL PSU KIT.** Output: +5V/5A; +12V; +25V; −5V; −12V @ 1A. **£40**
- **4 × 4 matrix keypad** (reed switch assembly) **£4**
- **C12 COMPUTER Grade BASF Cassettes** in Library Cases **40p**
- **8½" & 9½" Fan fold paper** (1000 sheets) **£7 (150p)**
- **Teleprinter Roll** (no VAT) **£3.50**

(P&P on some of the above items is extra) Call in at our shop for demonstration of any of the above items. Be satisfied before you buy.

- **MICROLINE-82A.** 10" Tractor & Friction Feed. 9×9 matrix, 80 column, 120 CPS. Bi-directional **£320** (£7 carr.)

★ NEW ★

- **DP80 PRINTER.** 80CPS, dot matrix printer, 80 column, logic seeking, italics, graphic resolution, true decenders, Tractor/Friction feed. Carbon ribbon. Ideal with BBC Micro complete with paper rack. Introductory offer: **£299** (carr. £7)
- **EPSON FX80 10"** 160cps, Tractor/Friction, Bi-directional, logic seeking, 9 × 11 matrix, Hi-res bit image, normal, italic & elite char. Super & subscript. Proportional spacing. Underlining. **£395** (£7 carr.)

CRYSTALS

32.768KHz	100
100KHz	235
200KHz	268
455KHz	370
1MHz	275
1.008M	275
1.28MHz	392
1.5MHz	420
1.6MHz	395
1.8MHz	395
1.8432M	200
2.0MHz	225
2.4576M	200
2.5MHz	225
2.56250M	220
3.2768M	150
3.57954M	98
3.6864M	300
4.0MHz	150
4.032MHz	290
4.194304M	200
4.433619M	100
4.608MHz	200
4.80MHz	200
5.0MHz	160
5.185MHz	300
5.24288M	390
6.0MHz	140
6.144MHz	150
6.5536MHz	200
7.0MHz	150
7.168MHz	250
7.68MHz	200
8.0MHz	150
8.08333M	395
8.867237M	175
9.00MHz	200
9.375MHz	350
10.0MHz	175
10.5MHz	250
10.7MHz	150
10.24MHz	200
12.0MHz	175
12.528MHz	300
14.31818M	170
14.7456M	175
14.765MHz	250
15.0MHz	200
16.0MHz	200
18.0MHz	180
18.432M	150
19.968MHz	150
20.0MHz	200
24.0MHz	170
24.930MHz	325
29.695MHz	150
26.670MHz	325
27.125MHz	295
27.145M	190
27.648MHz	300
38.66667M	175
48.0MHz	175
55.5MHz	400
100MHz	350
116.0MHz	300
145.8MHz	225

AMPHENOL PLUGS

	IDC	Solder
24 way IEE	475p	450p
36 way Centronix	525p	485p

ASTEC UHF MODULATORS

6MHz	325p
8MHz Wideband	450p

BBC MICRO & UPGRADE KITS

- BBC Micro A **£299;** MODEL B **£399** (incl.)
- 16K MEMORY (8×4816-100ns) BBC1 **£16.00**
- Printer User I/O Port BBC2 **£6.98**
- Complete Printer Cable 36" **£12.00**
- Disc Interface Kit incl. DOS **£65.00**
- BBC Joysticks **£12/pr**
- Analogue I/O Kit BBC4 **£6.45**
- Serial I/O Kit BBC5 **£6.70**
- Expansion Bus Kit BBC6 **£6.10**
- Complete Upgrade Kit from Model A to B **£42**
- Complete range of Connectors, Cables, Quality Software, Accessories, Books, etc. for BBC available. Send SAE for detail list.

DISC DRIVES (BBC Compatible) (12 months warranty on Drives)

- CS50A – TEAC Single Cased with PSU, 40 track, 5¼". Single sided, 100K **£180**
- CD50A – TEAC Twin Cased with PSU, 40 track, 5¼". Single sided, 200K **£350**
- CS50E – TEAC Single Cased with PSU, 80 track, 5¼". Single sided, 200K **£250**
- CD50E – TEAC Twin Cased with PSU, 80 track, 5¼". Single sided, 400K **£475**
- **MITSUBISHI** Slim line, Single Cased with PSU, 5¼". 80 tracks, D.S.D.D. 1 Megabytes (400K-BBC) **£275**
- **MITSUBISHI** Slim line, Dual Cased with PSU, 5¼", 80 tracks, D.S.D.D. 2 Megabytes (800K-BBC) **£550**

ANTEX Soldering Irons

C15W	495
G517W	495
G18W	520
XS25W	525
Spare bits	85
Elements	225
Iron stands	175
Heat Shunt	30

Access

Just phone your order through, we do the rest. 0923-50234

WATFORD ELECTRONICS

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MAIL ORDER ADVERTISING

British Code of Advertising Practice

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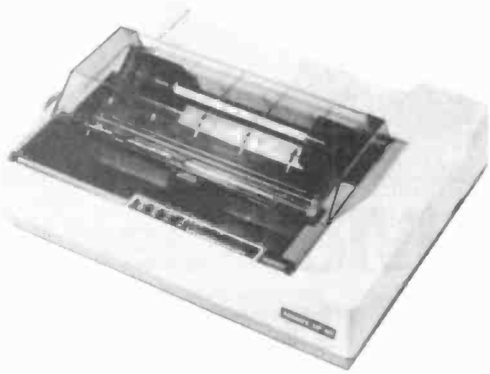
WHAT USE A MICRO WITHOUT A PRINTER?



NEW A.D.M. 80 COL. DOT MATRIX WITH TRACTOR FEED. BACKED BY ONE OF BRITAINS LARGEST MANUFACTURERS, IT IS NOW STOCKED BY US.

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£311.00 + VAT. Carriage £7.50 or collect from our warehouse.

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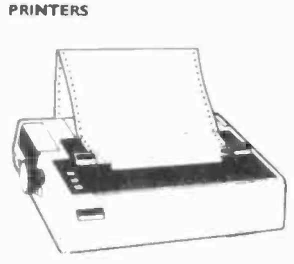
ORIC AND SINCLAIR COMPUTERS

Oric I 48K computer **£147 (£158)**. Oric I 16K n/a (n/a). Sinclair Spectrum 48K **£113 (£133)**. Spectrum 16K **£86.91 (£107)**. 32K memory upgrade kit for 16K Spectrum (Issue 2 only) **£26.09 (£28)**. Fuller master unit for the Spectrum including speech synthesizer, sound synthesizer, amplifier and joystick ports **£47.78 (£56)**. ZX microdrive n/a (n/a). ZX rs232 n/a (n/a). Keyboards with space bars for the ZX81 and the Spectrum **£36 (£41)**. ZX printer **£34.74 (£50)**. 5 printer rolls **£10.43 (£16)**. ZX81 **£43.43 (£52)**. ZX81 16K ram packs **£26.04 (£28)**. New luxury spectrum computers 48K with full sized typewriter keyboards complete with normal space bar enclosed in a larger plastic case which also houses the power supply and the computer pcb **£138.20 (£174)**.

COMMODORE COMPUTERS
Commodore 64 **£299 (£309)**. Vic 20 **£130 (£140)**. Special offer package:– Vic 20 + cassette recorder + basic course + 4 games **£139 (£149)**. Convertor to allow the use of most ordinary mono cassette recorders with the Vic 20 and the Commodore 64 built **£8 (£9)**, kit **£6 (£7)**. Commodore cassette recorder **£36.50 (£44)**. We stock most accessories.

OTHER COMPUTERS
Colour Genie **£168 (£178)**. BBC Model B **£424 (£440)**. Texas TI99/4A **£139 (£169)**. Atari 800 **£347 (£380)**. Atari 400 16K with basic **£173 (£215)**.

PRINTERS



The Epson MX80FT/3 has been replaced by the almost identical CTI CP80 **£262 (£282)** and the very similar Star DP510 **£262 (£282)**. Epson FX80 **£378 (£408)**. Epson MX100/3 **£425 (£465)**. New Star DP515 15" carriage printer **£374 (£414)**. Seikosha GP100A **£199 (£219)**. Oki Microline 80 **£207 (£227)**. Oki Microline 82A **£360 (£400)**. Oki Microline 84 **£730**. Oki Microline 92 **£470**. The Bytewriter, the latest miracle, a combined daisy wheel printer and electric typewriter for only **£418 (£448)**. We can supply interfaces to run any of the above printers from Sharp computers.

SWANLEY ELECTRONICS
Dept PE, 32 Goldsel Rd., Swanley, Kent BR8 8EZ, England.
Please allow 7 days for delivery.

UK prices are shown first. UK customers must add postage (£1 on Sinclair products, £3.50 on other computers and disc drives and £4.50 on other printers) and the 15% VAT. The bracketed prices are European export prices and include insured airmail postage to all the countries of Europe including Norway, Sweden, Finland, Denmark, Spain and Italy. No VAT should be added to export prices. We are the leading computer export specialist. Official UK credit orders welcome from government laboratories and educational establishments.

---

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hi! reliability hi! service hi! performance hi! reliability hi! service hi! performance hi! competitive

hi! reliability hi! service hi! performance hi! competitive hi! performance hi! competitive

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nearly 50% more with the NEW LARGE 6 inch rectangular CRT with illuminated inner face graticule, 6KV accelerator voltage for a brighter, higher resolution display with guaranteed accuracy.

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1 milli Volt per cm in the vertical axis, valuable for observing complex low level waveforms especially with 20 nano sec per cm Sweep Speed.

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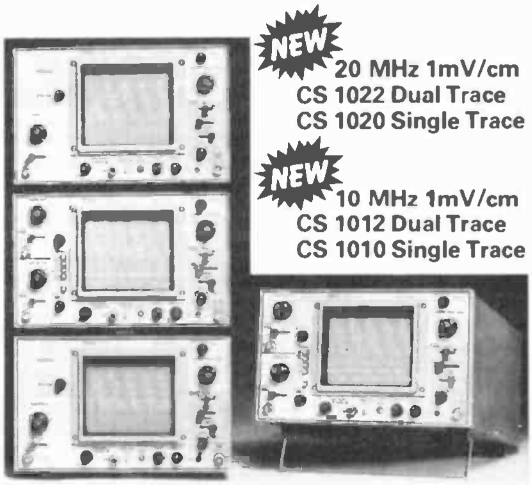

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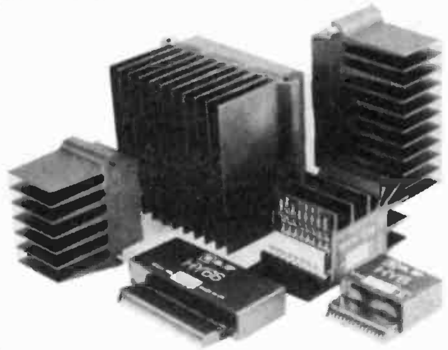

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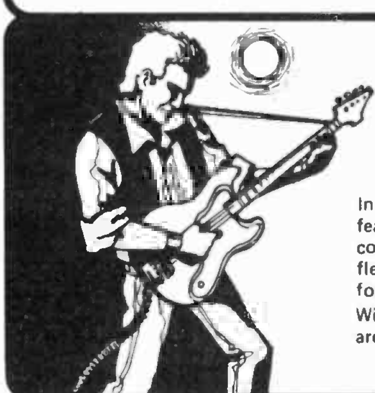
the third generation

Due to continous improvements in components and design ILP now launch the largest and most advanced generation of modules ever.



WE'RE INSTRUMENTAL IN MAKING A LOT OF POWER

In keeping with ILP's tradition of entirely self-contained modules featuring, integral heatsinks, no external components and only 5 connections required, the range has been optimized for efficiency, flexibility, reliability, easy usage, outstanding performance, value for money.

With over 10 years experience in audio amplifier technology ILP are recognised as world leaders.

BIPOLAR MODULES

Module Number	Output Power Watts rms	Load Impedence Ω	DISTORTION T.H.D. Typ at 1KHz	DISTORTION I.M.D. 60Hz/7KHz 4:1	Supply Voltage Typ	Size mm	WT gms	Price inc. VAT
HY30	15	4-8	0.015%	<0.006%	± 18	76 x 68 x 40	240	£8.40
HY60	30	4-8	0.015%	<0.006%	± 25	76 x 68 x 40	240	£9.55
HY6060	30 + 30	4-8	0.015%	<0.006%	± 25	120 x 78 x 40	420	£18.69
HY124	60	4	0.01%	<0.006%	± 26	120 x 78 x 40	410	£20.75
HY128	60	8	0.01%	<0.006%	± 35	120 x 78 x 40	410	£20.75
HY244	120	4	0.01%	<0.006%	± 35	120 x 78 x 50	520	£25.47
HY248	120	8	0.01%	<0.006%	± 50	120 x 78 x 50	520	£25.47
HY364	180	4	0.01%	<0.006%	± 45	120 x 78 x 100	1030	£38.41
HY368	180	8	0.01%	<0.006%	± 60	120 x 78 x 100	1030	£38.41

Protection: Full load line, Slew Rate: 15v/µs. Risetime: 5µs. S/N ratio: 100db.
Frequency response (−3dB) 15Hz – 50KHz. Input sensitivity: 500mV rms.
Input Impedance: 100K Ω. Damping factor: 100Hz >400.

PRE-AMP SYSTEMS

Module Number	Module	Functions	Current Required	Price inc. VAT
HY6	Mono pre amp	Mic/Mag. Cartridge/Tuner/Tape/ Aux + Vol/Bass/Treble	10mA	£7.60
HY66	Stereo pre amp	Mic/Mag. Cartridge/Tuner/Tape/ Aux + Vol/Bass/Treble/Balance	20mA	£14.32
HY73	Guitar pre amp	Two Guitar (Bass Lead) and Mic + separate Volume Bass Treble + Mix	20mA	£15.36
HY78	Stereo pre amp	As HY66 less tone controls	20mA	£14.20

Most pre-amp modules can be driven by the PSU driving the main power amp. A separate PSU 30 is available purely for pre amp modules if required for £5.47 (inc. VAT). Pre-amp and mixing modules in 18 different variations. Please send for details.

Mounting Boards

For ease of construction we recommend the **B6** for modules HY6–HY13 £1.05 (inc. VAT) and the **B66** for modules HY66–HY78 £1.29 (inc. VAT).

MOSFET MODULES

Module Number	Output Power Watts rms	Load Impedence Ω	DISTORTION T.H.D. Typ at 1KHz	DISTORTION I.M.D. 60Hz/7KHz 4:1	Supply Voltage Typ	Size mm	WT gms	Price inc. VAT
MOS 128	60	4-8	<0.005%	<0.006%	± 45	120 x 78 x 40	420	£30.41
MOS 248	120	4-8	<0.005%	<0.006%	± 55	120 x 78 x 80	850	£39.86
MOS 364	180	4	<0.005%	<0.006%	± 55	120 x 78 x 100	1025	£45.54

Protection: Able to cope with complex loads without the need for very special protection circuitry (fuses will suffice).
Slew rate: 20v/µs. Rise time 3µs. S/N ratio: 100db
Frequency response (−3dB): 15Hz – 100KHz. Input sensitivity 500mV rms
Input impedance: 100K Ω. Damping factor. 100Hz > 400.

'NEW to ILP' In Car Entertainments

C15

Mono Power Booster Amplifier to increase the output of your existing car radio or cassette player to a nominal 15 watts rms.

Very easy to use.

Robust construction. **£9.14 (inc. VAT)**

Mounts anywhere in car.

Automatic switch on.

Output power maximum 22w peak into 4Ω.
Frequency response (−3dB) 15Hz to 30KHz, T.H.D. 0.1% at 10w 1KHz
S/N ratio (DIN AUDIO) 80dB, Load Impedance 3Ω
Input Sensitivity and impedance (selectable) 700mV rms into 15K Ω 3V rms into 8Ω
Size 95 x 48 x 50mm. Weight 256 gms.

C1515

Stereo version of C15. **£17.19 (inc. VAT)**

Size 95 x 40 x 80. Weight 410 gms.

POWER SUPPLY UNITS (Incorporating our own toroidal transformers)

Model Number	For Use With	Price inc. VAT
PSU 21X	1 or 2 HY30	£11.93
PSU 41X	1 or 2 HY60, 1 x HY6060, 1 x HY124	£13.83
PSU 42X	1 x HY128	£15.90
PSU 43X	1 x MOS128	£16.70
PSU 51X	2 x HY128, 1 x HY244	£17.07

Model Number	For Use With	Price inc. VAT
PSU 52X	2 x HY124	£17.07
PSU 53X	2 x MOS128	£17.86
PSU 54X	1 x HY248	£17.86
PSU 55X	1 x MOS248	£19.52
PSU 71X	2 x HY244	£21.75

Model Number	For Use With	Price inc. VAT
PSU 72X	2 x HY248	£22.54
PSU 73X	1 x HY364	£22.54
PSU 74X	1 x HY368	£24.20
PSU 75X	2 x MOS248, 1 x MOS368	£24.20

Please note: X in part no. indicates primary voltage. Please insert "0" in place of X for 110V, "1" in place of X for 220V, and "2" in place of X for 240V.

WITH A LOT OF HELP FROM ILP ELECTRONICS LTD

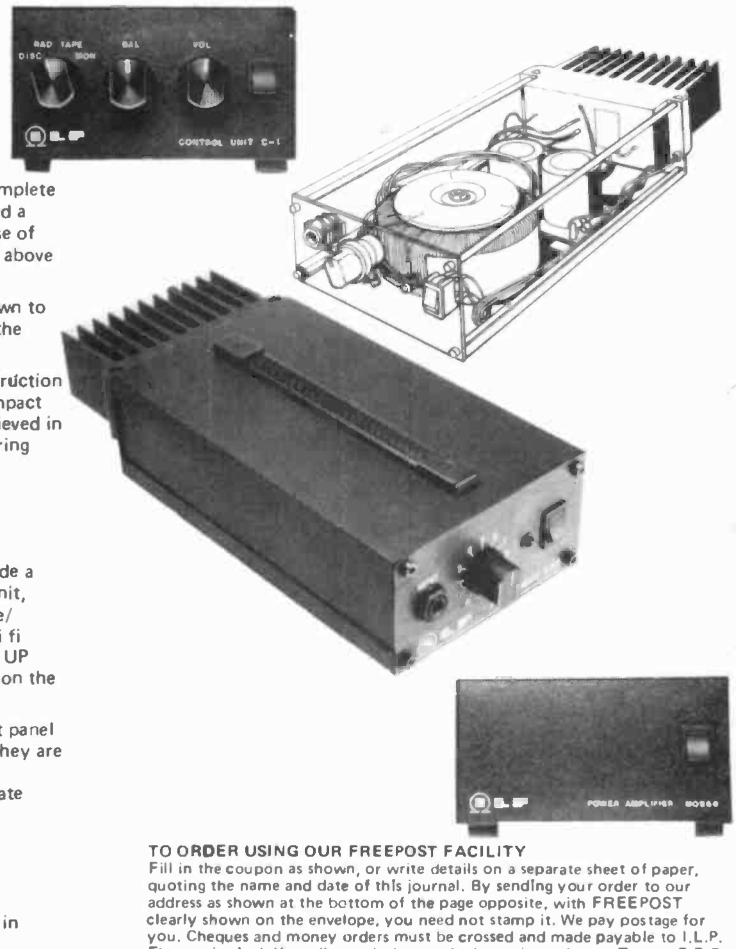
PROFESSIONAL HI-FI THAT EVERY ENTHUSIAST CAN HANDLE...

Unicase

Over the years ILP has been aware of the need for a complete packaging system for it's products, it has now developed a unique system which meets all the requirements for ease of assembly, adaptability, ruggedness, modern styling and above all price.

Each Unicase kit contains all the hardware required down to the last nut and bolt to build a complete unit without the need for any special tools.

Because of ILP's modular approach, "open plan" construction is used and final assembly of the unit parts forms a compact aesthetic unit. By this method construction can be achieved in under two hours with little experience of electronic wiring and mechanical assembly.



Hi Fi Separates

UC1 PRE AMP UNIT: Incorporates the HY78 to provide a "no frills", low distortion, (<0.01%), stereo control unit, providing inputs for magnetic cartridge, tuner, and tape/ monitor facilities. This unit provides the heart of the hi fi system and can be used in conjunction with any of the UP Unicase series of power amps. For ultimate hum rejection the UC1 draws its power from the power amp unit.

POWER AMPS: The UP series feature a clean line front panel incorporating on/off switch and concealed indicator. They are designed to compliment the style of the UC1 pre-amp. Performance for each unit which includes the appropriate power supply, is as specified on the facing page.

Power Slaves

Our power slaves, which have numerous uses i.e. instrument, discotheque, sound reinforcement, feature in addition to the hi fi series, front panel input jack, level control, and a carrying handle. Providing the smallest, lowest cost, slave on the market in this format.

UNICASES

HIFI Separates					Price Inc. VAT
UC1	Preamp				£29.95
UP1X	30 + 30W/4–8Ω	Bipolar	Stereo	HiFi	£54.95
UP2X	60W/4Ω	Bipolar	Mono	HiFi	£54.95
UP3X	60W/8Ω	Bipolar	Mono	HiFi	£54.95
UP4X	120W/4Ω	Bipolar	Mono	HiFi	£74.95
UP5X	120W/8Ω	Bipolar	Mono	HiFi	£74.95
UP6X	60W/4–8Ω	MOS	Mono	HiFi	£64.95
UP7X	120W/4–8Ω	MOS	Mono	HiFi	£84.95
Power Slaves					
US1X	60W/4Ω	Bipolar	Power	Slave	£59.95
US2X	120W/4Ω	Bipolar	Power	Slave	£79.95
US3X	60W/4–8Ω	MOS	Power	Slave	£69.96
US4X	120W/4–8Ω	MOS	Power	Slave	£89.95

Please note X in part number denotes mains voltage. Please insert '0' in place of X for 110V, '1' in place of X for 220V (Europe), and '2' in place of X for 240V (U.K.) All units except UC1 incorporate our own toroidal transformers.

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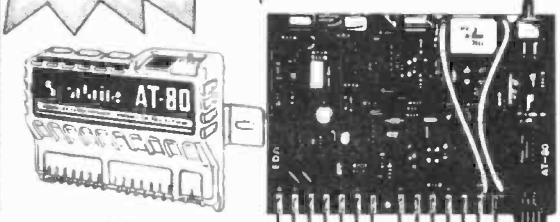

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Electronic Car Security System

- Arms doors, boot, bonnet and has security loop to protect fog/spot lamps, radio/tape, CB equipment
- Programmable personal code entry system
- Armed and disarmed from outside vehicle using a special magnetic key fob against a windscreen sensor pad adhered to the inside of the screen ● Fits all 12V neg earth vehicles
- Over 250 components to assemble

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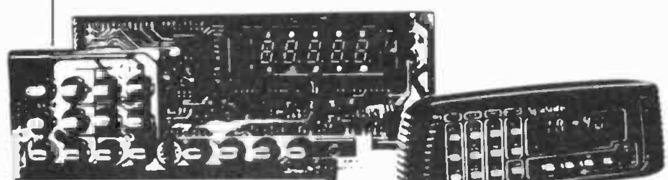
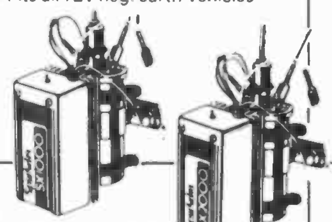
A real challenge for the electronics enthusiast!



SX1000

Electronic Ignition

- Inductive Discharge
- Extended coil energy storage circuit
- Contact breaker driven
- Three position changeover switch
- Over 65 components to assemble
- Patented clip-to-coil fitting
- Fits all 12v neg. earth vehicles

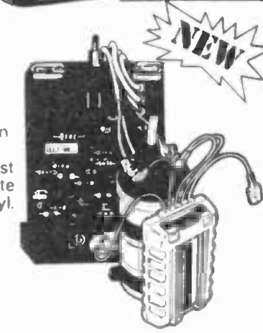


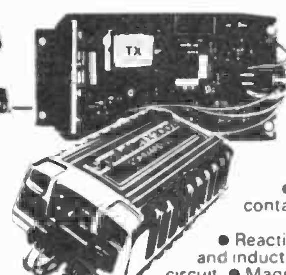
TX1002

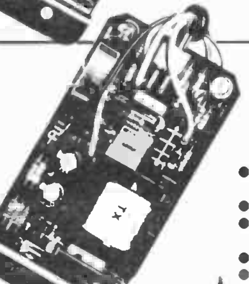
Electronic Ignition

NEW

● Contactless or contact triggered ● Extended coil energy storage circuit ● Inductive Discharge ● Three position changeover switch ● Distributor triggerhead adaptors included ● Die cast weatherproof case ● Clip-to-coil or remote mounting facility ● Fits majority of 4 & 6 cyl. 12V. neg. earth vehicles ● Over 145 components to assemble.







SX2000

Electronic Ignition

- The brandleading system on the market today
- Unique Reactive Discharge
- Combined Inductive and Capacitive Discharge
- Contact breaker driven
- Three position changeover switch
- Over 130 components to assemble
- Patented clip-to-coil fitting
- Fits all 12v neg. earth vehicles

TX2002

Electronic Ignition

● The ultimate system ● Switchable contactless ● Three position switch with Auxiliary back-up inductive circuit ● Reactive Discharge. Combined capacitive and inductive ● Extended coil energy storage circuit ● Magnetic contactless distributor trigger-head ● Distributor triggerhead adaptors included ● Can also be triggered by existing contact breakers ● Die cast waterproof case with clip-to-coil fitting ● Fits majority of 4 and 6 cylinder 12v neg. earth vehicles ● Over 150 components to assemble

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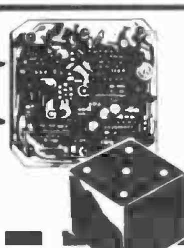

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Electronic Dice

- Not an auto item but great fun for the family
- Total random selection
- Triggered by waving of hand over dice
- Bleeps and flashes during a 4 second tumble sequence
- Throw displayed for 10 seconds
- Auto display of last throw 1 second in 5
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- Hours of continuous use from PP7 battery
- Over 100 components to assemble

SPARKRITE, 82 Bath St., Walsall, W. Midlands WS1 3DE

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83....as from 5 May 1983.....as from 5

HM 103 **£158** *UK List ex V.A.T.*

the original oscilloscope with built-in component tester

Capacitor 33uF | Transistor E-C | Transistor B-E | B-E 1uF + 68 ohms

NOW WITH IMPROVED SPECIFICATIONS

Y Deflection
Bandwidth: DC-10 MHz (-3dB)
Overshoot: Less than 1%
Sensitivity: 2mV-20 V/cm
Input Imp: 1M ohm//25pf
Variable Control

X Deflection
Timebase: 0.2s - 0.2us/cm
Triggering: 2Hz - 30MHz(3mm)
Auto + level control
Bandwidth: 2Hz - 1MHz
Variable Control

GENERAL INFORMATION

Component Tester	For single components and in circuit
Calibrator	0.2V ± 1% for probe alignment
Power Supplies	Regulated including high voltage
A.C. Input	110, 120, 220, 240, V.A.C., 50-60 Hz
Weight	8¼ Lbs.
Size	4½"(H) X 8 3/8"(W) X 10 7/16"(D)
CRT	Rectangular internal graticule
Accuracy	3% in vertical amplifier
Filter	T.V. trigger filter
Trace rotation	via front panel

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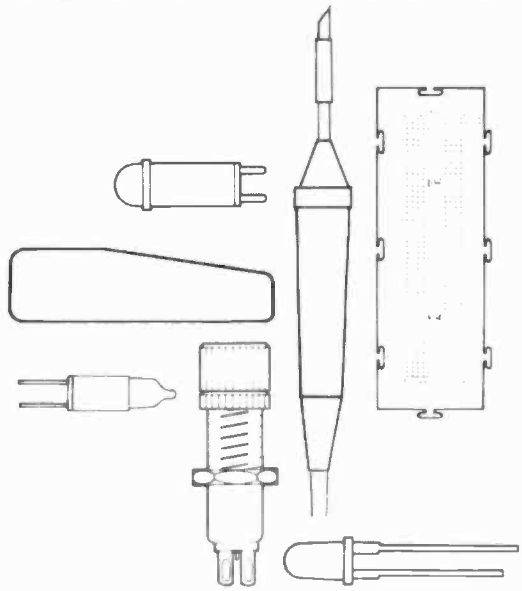

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556CMOS	140
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AY-3-8912	540
CA3046	60
CA3080	65
CA3089	190
CA3090AQ	370
CA3130E	85
CA3140E	36
CA3161E	100
CA3189	200
CA3240E	110
ICL7106	680
ICL7611	95
ICL7621	180
ICL7622	180
ICL8038	290
ICL8211A	150
ICM7224	775
ICM7555	80
LF353	85
LF356	90
LM10	325
LM301A	24
LM311	70
LM318	120
LM324	30
LM334Z	90
LM335Z	120
LM339	45
LM348	60
LM358	55
LM377	165
LM380	65
LM381	120
LM382	110
LM384	130
LM386	65
LM387	120
LM393	95
LM711	60
LM725	325
LM733	69
LM747	60
LM1458	40
LM2917	185
LM3900	45
LM3909	70
LM3911	120
LM3914	175
LM3915	195
LM13600	105
MC1496	68
MC3340	120
MC10CN	350
ML924	195
NE529	225
NE531	135
NE544	180
NE555	16
NE556	45
NE565	110
NE566	140
NE567	100
NE570	370
NE571	370
RC4136	55
RC4558	45
SL490	250
SL76477	380
SP8629	250
TBA120S	70
TBA800	75
TBA810	95
TBA820	70
TBA950	220
TDA1008	310
TDA1022	480
TDA1024	115
TL061	40.
TL062	60
TL064	95
TL071	25
TL072	45
TL074	95
TL081	24
TL082	45
TL084	90
TL170	49
UA2240	115
ULN2003	75
ULN2004	75
XR2206	285
ZN414	79
ZN423	130
ZN424	130
ZN425E	340
ZN426E	290
ZN427E	575
ZN428E	395
ZN459	285
ZN1034E	200

LOGIC ICs

AY5-2376	590
MC1488	55
MC1489	55
MM5303	625
MM5307	1250
MM58174	700
TMS6011	365
ULN2003	75
8T26	99
8T28	120
8T95	90
8T97	90
81LS95	80
81LS96	80
81LS97	80
81LS98	85
6522	310
6532	675
6821	110
6845	650
6847	650
6850	110
6852	250
6875	485
8155	350
8212	110
8216	100
8224	110
8226	250
8228	220
8243	270
8250	865
8251	250
8253	400
8255	225
8257	400
8259	395
8279	385
8832	250
9602	220
Z80ACTC	260
Z80ADART	775
Z80ADMA	975
Z80AP10	270
ZN425E8	320
ZN426E8	320
ZN427E8	575
ZN428E8	395

CMOS

4000	11
4001	11
4002	11
4007	14
4008	34
4009	24
4011	11
4012	14
4013	20
4015	39
4016	20
4017	32
4020	42
4021	39
4022	39
4023	12
4024	32
4025	12
4027	20
4028	37
4029	43
4035	45
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4076	44
4078	13
4081	12
4082	12
4093	23
4099	70
4502	50
4508	110
4510	45
4511	45
4512	42
4514	110
4515	110
4516	50
4518	39
4520	48
4521	90
4522	105
4526	55
4527	55
4528	45
4531	65
4532	60
4538	60
4539	80
4543	60
4555	35
4556	35
4561	100
4583	80
4584	40
4585	50

COMPUTER ICs

1802	650
2650A	1175
6502	320
6800	220
6802	250
6809	615
8035	345
8060	1090
8080A	250
8085A	345
Z80A	315

MEMORIES

2101	395
2114 (200ns)	85
2532	295
2564	1000
2708	225
2716 (5V)	210
2764	750
4116 (200ns)	80
4118-3	325
4164	420
5101 (450ns)	150
5204	725
6116 (150ns)	375
6514	330
6810	115

74LS

LS00	11
LS01	11
LS02	11
LS03	11
LS04	12
LS05	12
LS08	12
LS09	12
LS10	12
LS11	12
LS12	12
LS14	22
LS15	12
LS20	12
LS21	12
LS22	12
LS27	12
LS28	14
LS30	12
LS32	13
LS33	14
LS37	14
LS38	14
LS40	12
LS42	28
LS47	35
LS48	40
LS49	50
LS51	14
LS54	14
LS55	14
LS74	16
LS75	16
LS76	16
LS78	17
LS83	33
LS85	39
LS86	15
LS90	22
LS92	25
LS93	22
LS95	36
LS109	21
LS112	20
LS113	20
LS114	21
LS123	34
LS125	24
LS126	25
LS132	29
LS136	23
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LS151	30
LS153	38
LS155	29
LS156	33
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LS160	30
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LS162	35
LS163	35
LS164	40
LS165	50
LS168	80
LS170	70
LS173	47
LS174	36
LS175	36
LS181	87
LS183	105
LS190	35
LS191	35
LS192	35
LS193	36
LS194	32
LS195	32
LS196	43
LS197	45
LS221	50
LS240	55
LS241	55
LS242	55
LS243	55
LS244	55
LS245	70
LS251	28
LS253	30
LS257	29
LS258	32
LS259	53
LS266	18
LS273	53
LS279	30
LS283	38
LS290	40
LS293	40
LS365	27
LS366	27
LS367	27
LS368	27

MICRO-MINI 100V CERAMIC PLATE CAPS

1pF 10nF	7

TANTALUM BEADS

0.1/35	12
0.22/35	12
0.33/35	12
0.47/35	12
0.68/35	12
1.0/35	12
1.5/35	14
2.2/35	16
3.3/35	17
10/25	18
15/25	28
2.2/16	14
3.3/16	14
4.7/16	16
6.8/16	16
10/16	18
15/16	27
22/16	27
33/16	40
47/16	40
100/16	75
15/10	22
22/10	24
33/10	30
47/10	35
100/10	55
100/6.3	42

63V MINI MONOLITHIC CERAMIC

10nF	10
22nF	10
33nF	10
47nF	10
68nF	10
100nF	14

DIODES

0A47	10
1N4001	4
1N4002	4
1N4003	5
1N4004	5
1N4005	6
1N4006	7
1N4007	7
1N4148	2
1N5401	12
1N5404	14
1N5406	17
1N5408	19

ZENER DIODES

2V7-33V 500 MW	7
5V1-75V 1.3W	14

BRIDGE RECTIFIERS

1A/100V	20
1A/200V	23
1A/400V	25
1A/800V	38
2A/100V	36
2A/200V	40
2A/400V	40
2A/800V	52
25/100V	215
25/200V	225
25/400V	270
25/600V	325

REGULATORS

78L05	30
78L12	30
78L15	30
78L24	30
7805T	36
7812T	36
7815T	36
7824T	36
79L05	60
79L12	60
79L15	60
7905T	42
7912T	42
7915T	42
7924T	42
LM309K	130
LM317K	270
LM317T	120
LM323K	350
LM723	35
78H05-5A/5V	550

RESISTORS

Carbon Film	
High Stab 5%	
¼W 10 –1M	2
½W 10 –10M	2
Metal Oxide/Film	
2% Met. Film E24	5
1% Met. Film E24	8

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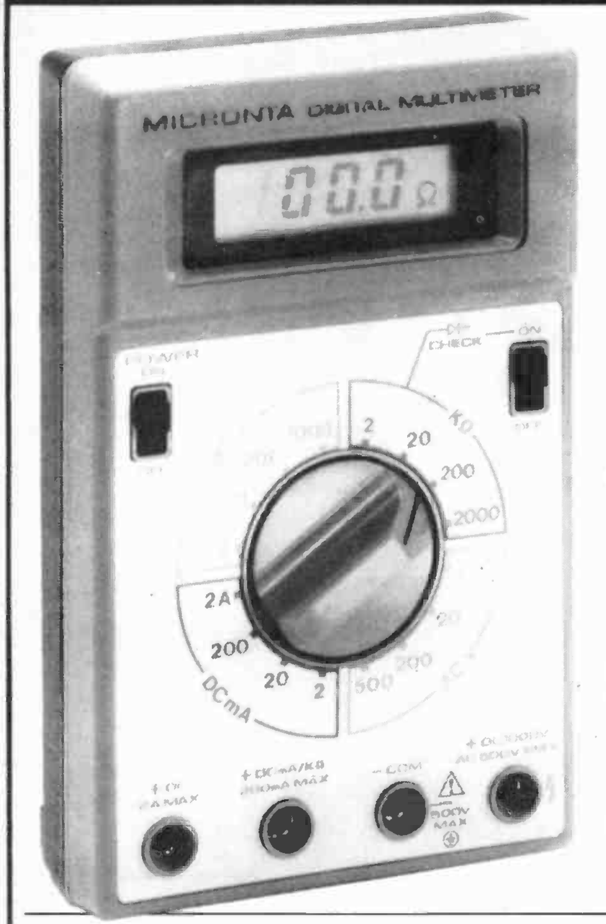

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Digital accuracy at a practical price. Features easy-to-read display. Single-IC design assures extremely low battery drain and high accuracy. Single-knob switch, full auto-polarity operation. Low-battery and overrange indicators. Diode check on/off switch. **DC volts:** 2-20-200-2000V (max. 1000V), **AC volts:** 2-20-200-2000V (max. 500V), accurate from 45 Hz to 10 kHz. **DC Current:** 2-20-200mA-2A. **Resistance:** 2-20-200-2000k Ohms. 5 3/16 x 3 1/4 x 1 7/16". Includes spare fuse, test leads. Requires 2 "AA" batteries. **22-189**

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Prior to this advertisement, all quoted regular prices have been charged during the last six months at the Tandy Store, Tameway Tower, Bridge Street, Walsall, West Midlands. WS1 1LA

PE

VOLUME 19 No. 8 AUGUST 1983

CABLE—A BREAKTHROUGH?

WITH the recent news of a cable service for most UK homes and the exciting possibilities that have been dreamed up by the media it is sobering to read what follows, written more than eleven years ago by Fred Bennett who was then editor of PE.

"With commendable boldness and confidence in the future growth of telecommunications for domestic purposes, the Post Office is currently involved in the installation of a 'communication main' system in the new city of Milton Keynes, now arising in Buckinghamshire. Every house in the new city will be linked to this communication system. The cables will, so far as possible, be laid in a communal trench, with the other essential services, water, gas, electricity, and drainage.

"A standard telephone pair forms part of this 'main'. This cable is accompanied throughout, right up to every front door, by a high performance coaxial cable. Besides being capable of carrying radio and television signals, this wideband coaxial cable provides for the transmission of two-way signals such as could be employed to operate viewphones and computer data terminals, and permits the carrying out of other useful functions, like the remote reading of gas and electricity supply meters.

"What happens in Milton Keynes *may* become the pattern for the future throughout the country. At any rate, this pioneer installation is worth noting and musing upon. It could herald another technological explosion making direct impact upon the domestic or 'consumer' section. We don't doubt that fertile minds will seize eagerly the opportunity it promises for further imaginative and useful exploitation of electronics."

Obviously with the increase in consumers resulting from wide scale cabling the cost of suitable equipment will fall. However, we cannot help wondering if it will all be worthwhile when the use of Viewdata is still so limited. The wonders of Information Technology will not be forced on a community that sees little advantage in the system. The availability of a vast range of cheaply hired video cassettes already reduces the chance of any "film channel" being successful.

As Vernon Trent indicates this month, technology can move as fast as it likes, the consumers are setting their own pace.

PRICE INCREASE

Unfortunately rising costs have forced us to make a cover price increase. From next month PE will cost an extra five pence; this is slightly less than a six per cent increase. The last increase was a year ago.

Mike Kenward

Technical *and* Editorial *queries and letters (see note below) to:*
Practical Electronics Editorial,
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West Quay Road, Poole,
Dorset BH15 1JG
Phone: *Editorial* Poole 671191

We regret that lengthy technical enquiries cannot be answered over the telephone

Queries and letters concerning **advertisements** *to:*
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Telex: 915748 MAGDIV-G

Letters and Queries

We are unable to offer any advice on the use or purchase of commercial equipment or the incorporation or modification of designs published in PE. All letters requiring a reply should be accompanied by a stamped, self addressed envelope, or addressed envelope and international reply coupons, and each letter should relate to one **published project only.**

Components and p.c.b.s are usually available from advertisers; where we anticipate difficulties a source will be suggested.

Back Numbers

Copies of most of our recent issues are available from: Post Sales Department (Practical Electronics), IPC Magazines Ltd., Lavington House, 25 Lavington Street, London SE1 0PF, at £1 each including Inland/Overseas p&p. Please state month and year of issue required.

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Subscriptions

Copies of PE are available by post, inland or overseas, for £13·00 per 12 issues, from: Practical Electronics, Subscription Department, Oakfield House, Perrymount Road, Haywards Heath, West Sussex RH16 3DH. Cheques, postal orders and international money orders should be made payable to IPC Magazines Limited. Payment can also be made using any credit card and orders placed via Teledata Tel. 01-200 0200.

Items mentioned are available through normal retail outlets, unless otherwise specified. Prices correct at time of going to press.

Farewell Analogue TV

It was hardly likely that the humble domestic television receiver would remain outside the swelling compass of digital technology for much longer. The bell tolls, and ITT is the campanologer with its "Digivision" system.

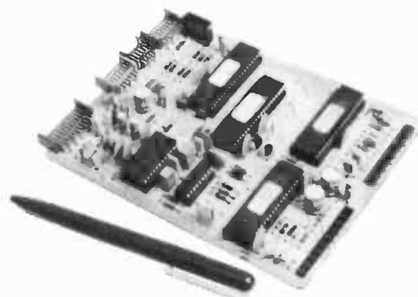
Until now, digital electronics has been applied only to two sections of the television set, these being the infra-red remote control and the local oscillator of the tuner. The situation has changed dramatically. In what is claimed to be the biggest revolution in television since the introduction of colour 30 years ago, ITT's Digivision offers an entirely new system which changes fundamentally almost every section of the receiver. Although Digivision is designed to receive conventional TV broadcast signals, it is almost 100 per cent digital in operation, and it is already on the commercial horizon. Receivers based on the Digivision chip set will be on sale in West Germany, the country of origin, in late 1983. They will become available in the UK in early 1984. ITT expects that in the future 50 per cent of all television sets sold throughout the world will incorporate Digivision. An understandable anticipation, it being the culmination of a 10 year, £20m investment project.

The benefits of a micro' based receiver, to both the user and the service engineer, are manifold. The end-user gets a television which makes an "intelligent" effort to optimise reception under all conditions (including ageing) by comparing performance characteristics with factory preset values stored in memory, and, naturally, making all necessary adjustments automatically. Sound quality is also improved with digital processing right to the loudspeaker (mono or stereo) using pulse-width modulation.

The service engineer will benefit from a tool that ITT calls an "electronic screwdriver". This diagnostics computer runs tests and makes adjustments to the receiver's EAROM data by way of an umbilical cable. The chassis has only one preset potentiometer. The engineer will be able to carry out most adjustments from the front of the set, following prompts on the screen.

Some amazing possibilities accompany the digital television era. Line and field storage is envisaged, which will allow display scanning standards to be defined and varied locally. For example, a 625 line, 50 fields/sec interlaced picture could be displayed at 1250 line, 150 fields/sec non-interlaced, yielding improvements in subjective definition and stability. Picture data storage will also make possible selective "zoom" and "freeze" of any broadcast picture. Noise, interference and flicker will be eliminated, and ghost images will be "exorcised". The intriguing prospect of pictures from other channels being inset into one corner of the channel being watched, is with us.

These features by no means represent the extent of exciting possibilities that should become reality between 1983 and 1986. Digivision will be able to accept signals directly from Prestel or a home computer, or from a video cassette recorder or video disc player operating on any television standard (PAL, SECAM, NTSC).



The Digivision component board

ITT's first production designs would comprise up to 300 components if they were analogue, but will instead comprise just seven VLSI chips.

Piezoelectric Plastic

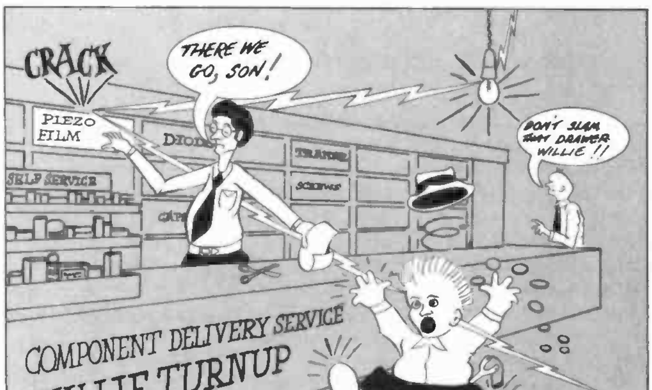
The electronics hobbyist of yore, enthused by experimentation with an OC71 transistor, a piece of paxolin and a tobacco tin, would have scoffed at the idea of discovering electronics, or physics using pre-designed circuits conveniently packed into little plastic bricks, no matter how many leads emerge from them. But he wouldn't have scoffed at the opportunities afforded by a new product from Metal Box's R&D lab's at Wantage, which opens up a whole new can of worms (as they say) for the experimentalist.

Think what could be done witb a sheet of piezoelectric plastic which can be cut to any shape or size, to make a custom transducer. The idea is not new; the Japanese (of course) have been making a similar material for some time, but it has never been widely available. Metal Box make theirs from polyvinylidene fluoride (PVDF) which is metallised, and undergoes rather special treatment to give it the potential to be used in microphones, loudspeakers, impact detectors and push buttons, and who knows what else?

When acting as an audio transducer the material can be its own diaphragm, opening up amazing possibilities, which include large area microphones, flat loudspeakers, vibrating surfaces or platforms and ultrasonics. Other applications spring to mind: How about a flexometer (if there is such a thing)? Or an optical deflector, or perhaps an acoustically controlled LF oscillator? Or even a liquid atomiser?

The pure experimentalist's odyssey is assured with this film, because it is also pyroelectric, enabling it to be used for thermal imaging, heat sensing, fire detection, temperature measurement, and doubtless other applications as yet to be conjured. The plastic film is readily formed into complex shapes. The film is available in thicknesses of 10 and 22 micrometre, and is already proving valuable in medical applications.

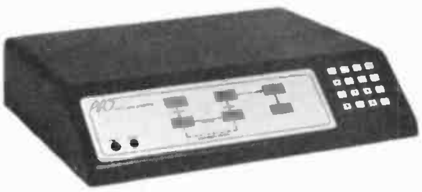
Sadly, at £20 for 200 sq. cm. (minimum qty.) Metal Box's piezoelectric film is at the moment a little expensive for dabbling with, but the manufacturer sees the price coming down as its use increases. Perhaps in the meantime, hobbyist suppliers will bulk buy and make the film available in less costly amounts.



MARKET PLACE

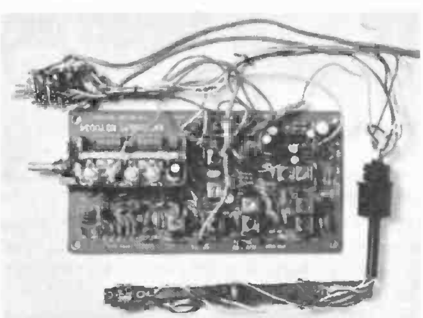
Viewdata Bargain

The PAT Viewdata adaptor shown here is available for £55 (including VAT, plus postage) but before you reach for your cheque book there is just one point we should mention! Although they are in the manufacturer's packing and are new and unused they can only be purchased from J. Bull (Electrical) Ltd., untested and without guarantee. However, the components alone



are worth more than the cost and "if all else fails" the GI chips could be used for your own design system. The unit shown in the photo is now providing Prestel in the PE office, following installation of a jack (£15) by British Telecom. The equipment is beautifully made and at the price is obviously too good to miss, provided you are prepared to take a chance. But make up your mind quickly as the quantity is limited.

Also from J. Bull is an excellent Amstrad a.m./f.m. tuner head. F.M. coverage is 87·5—108MHz at 2·5μV for 30dB signal to noise and a.m. coverage is: m.w. 525-1650kHz; l.w. 155-270kHz at 320μV/M.



Connections for a tuning meter, stereo beacon and a.f.c. switch are provided. With the addition of a 12V supply and simple stereo amp this would make a high quality portable radio or it could form the heart of a hi-fi system, as it was originally intended to do in the EX222 receiver. The tuners are new and the price is £6, including VAT plus postage.

J. Bull (Electrical) Ltd. (Dept PE), 34-36 America Lane, Haywards Heath, Sussex RH16 3QU. Tel: 0444 454563.

Amorphous Solar Cells

Mitsubishi Electric Corporation of Japan has managed the successful manufacture of an experimental 100cm^2 solar cell with an energy conversion efficiency of 8·25%. Although this may not sound like a very exciting event, this level of efficiency is claimed to be the world's highest for such a large element size.

The high performance solar cell, which comprises one amorphous germanium and two amorphous silicon layers, has an open-circuit output of 2·24V. It is low cost, using less than 1% of semiconductor materials as compared with a single crystal solar cell, and furthermore large element sizes are possible. Exposure to the sun gradually changes the characteristics of conventional cells, but does so far less with Mitsubishi's cells. Production costs are also lower, since the amorphous cell can use a cheap and comparatively unsmooth steel plate as its substrate.

As part of the solar cell research venture called the "Sunshine Project" Mitsubishi is in charge of amorphous cell development. The project, started in 1980 by the Japanese Agency of Industrial Science and Technology, had targeted the objective of a 10x10cm element with an efficiency greater than 8% by the close of 1982. This it achieved, and now Mitsubishi is working towards the production item.

Amorphous solar cell panels of Mitsubishi Electric

Silicon News Corner

Bulletins announcing new semiconductor devices arrive at PE daily, so it is possible only to describe them briefly. Details of how to obtain further information are included, however.

United Components ▶ Two new enhancement mode, 400MHz power f.e.t.s, UMP1 & UMP2. Operating from 25–30V, UMP1 gives 5W at 10dB gain, and UMP2 gives 10W at 7dB. Almost infinite VSWR mismatch tol.

▶ New stackable rectangular (2 x 5mm) l.e.d. series. The high efficiency MV5X123 is available in red and yellow and high brightness green.

▶ Optically isolated gate, triac driver i.c. (6-pin) called MCP30XX series. 120 & 240V versions can drive up to 24VA loads. Pin replacements for MOC3000 series.

▶ Data Books: GI Opto £2.50. **Plessey** High Speed Data Processing £1·20, High Speed Dividers £1·50, Consumer Devices (inc. remote control) £1·50, Telecoms £1·50, & Linear (inc. power control) £1·50. **Siliconix** FET Design cat. £1·75, Analogue Switch £2·50, MOSpower Design cat. £2·50. United Components, Unit 5, Wye Industrial Estate, London Road, High Wycombe, Bucks HP11 1LH.

Rastra ▶ The CH1812 module provides Direct Connect Protective Hybrid (DCPH) interface to telephone line, conforming to regulations. Measures 0·66 x 2·1 x 1·1 in.

▶ DAC 9331–16 series comprises 16-bit latched D to A in monolithic technology. Features 0·0008% linearity, 2-chip construction, I/P registers, low power, HI-REL 24-pin d.i.p., 2 & 4 quadrant multiplication, single +15V supply. Cheap, ultra-robust commercial device. Rastra Electronics, 275 King Street, Hammersmith, London W6 9NF.

Ferranti ▶ TO92 style radio receiver, designated ZN414Z is the widely available TRF circuit, now in alternative package.

▶ Motor speed controller i.c. called ZN411E provides precise speed control for electric power drills. On-chip shunt regulator, soft-start and reverse capability. Hall effect compatible "Tacho" I/P, and current limit. Ferranti Electronics, Fields New Road, Chadderton, Oldham, Lancs OL9 8NP.

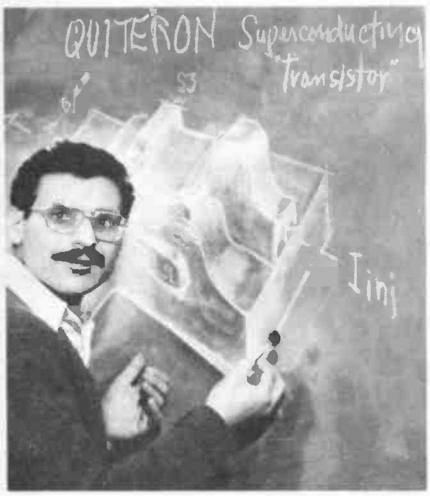
Siliconix ▶ Six new additions to the VN series power f.e.t.s offer 250W ratings, BVdss from 60–500V at 20A. These TO-3 packaged devices have on-resistance of 0·035–0·3. Siliconix Ltd., Morriston, Swansea SA6 6NE.

Motorola ▶ The marriage of the DIAC and the TRIAC results in a bilateral switch called the SIDAC, which conducts up to 1A when the voltage across it exceeds 115V for the MKIV-115, and 135V for the MKIV-135. Housed in "surmetic" 50 axial lead package, it is intended for pulse applications and fluorescent lamp starters. Motorola Ltd., York House, Empire Way, Wembley, Middlesex.

'Quiteron'

In the quest for the superconducting switch one early attempt (called the Cryotron) achieved a switching action by way of the transition from superconductor to normal metal—an action that was too slow for practical application. Another attempt, a three-terminal device invented at Argonne National Laboratory, did show small-signal current gain; but the most widely known breakthrough, called the Josephson Tunnel-Junction switch, functions with promisingly high speed and low power.

However, IBM's Thomas J. Watson research centre in Yorktown Heights, New York, has come up with a superconducting "transistor." The patented device is called the "quiteron" by its inventor, Sadeg M. Faris (shown in the photograph, holding a wafer of experimental samples).

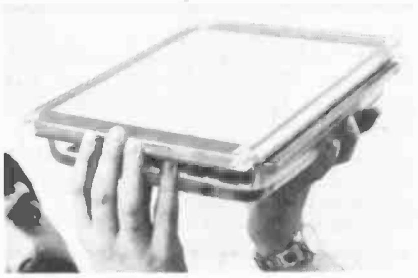


The quiteron has yet to be optimised, but it is the first three-terminal superconducting device that can both amplify and switch, consequently having potential applications in analogue and digital circuitry. Like the familiar Josephson Junction, the quiteron is a cryogenic device that employs superconductivity, a phenomenon occurring near absolute zero (0 deg. K, or −273 deg. C) at which temperature certain metals lose *all* resistance to electrical current flow. The two devices are, nevertheless, based on entirely different principles.

The quiteron consists of two tunnel junctions formed by three thin films of superconducting materials separated from one another by two, even thinner, films of insulating material. Structures of this nature have been studied before, but the quiteron is the first to make use of the "non-equilibrium" superconductivity phenomenon known as the "heavy-QUasiparticle-Injection Tunnelling Effect" (pardon?). The name qu-i-t-e-ron was derived from this.

Plasma Display Breakthrough

The secret of Siemens' success, where others have failed, in combining the flatness of the plasma display with the high intensity/resolution and colour potential of the c.r.t., is in the fact that *its* plasma is *not* used as a source of *light*, but as a source of *electrons*. The electrons are then guided by a specially developed grid to a conventional phosphor screen. The flat display developed by Siemens of Munich, West Germany, can illuminate up to 10^6 pixels *without* compromising other parameters—as in the past. The 14 inch plasma-discharge panel shown in the photograph is only six centimetres thick.



Because plasma acts as an electron source, as opposed to the hot cathode in a conventional c.r.t., this display requires a mere 4kV for its acceleration electrode (c.r.t. requires 20kV), and so it produces virtually no X-rays. This is a nice feature since the display will first begin to appear in VDU applications; and with a resolution of 3·1 dots/mm horizontally, and 2·5 dots/mm vertically, arbitrary graphical images are possible. Power drain for the entire panel is 20W, and flicker is eliminated by a refresh frequency of 80Hz.

The display surface is perfectly flat, which allows a good focus right into its extreme corners. Also the electron flight-path is much shorter than in a c.r.t., being one millimetre between the control plate and the phosphor, so that the natural divergence of the beam electrons due to mutual electrostatic repulsion is minimised. This improves the focal sharpness still further.

As a VDU, the display may be driven entirely digitally, each pixel being addressable on a row-and-column basis. Pulse durations determine illumination levels, thereby allowing a full greyscale. But there is nothing grey about the future of this development, which is quite capable of invading the television market in due course.

Trains and Boats and Planes

"What is this life if, full of care,
We have no time to stand and stare?"—*William Henry Davies.*

And what better place to stand and stare than the South Kensington Science Museum's new gallery called "Telecommunications — A Technology For Change," which is heavily sponsored for its first year of life by STC to mark the company's Centenary.

The public may enjoy the story of telecommunications by way of two adjoining galleries. The first describes the subject's chronology, whilst the second demonstrates the technologies that make distant communication possible.

Life size mock-ups include the telegraph office at Tonbridge railway station in 1850, a ship's radio cabin of 1910 and the radio operator's position in a World War II Lancaster bomber.

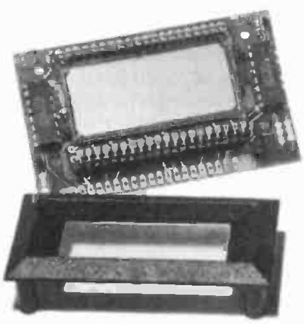
Tape recorded reminiscences of life in the service of cable companies throughout the period 1920–1950 add to the atmosphere, and working demonstrations and computer graphics displays illustrate aspects of modern telecommunications techniques. Packet switching and pulse code modulation principles are illustrated in this way, and a simulation of the System X digital exchange increases the visitor's understanding of services we all take for granted. A purpose-built cinema shows films produced by STC, but for those with an itch to twiddle knobs there is the remote controlled camera and monitor which may be operated by visitors. This installation oversees the museum's entrance, from a vantage point on the neighbouring Victoria and Albert Museum.

MARKET PLACE

PANEL METERS

A recently formed company called Martel has been set up to manufacture and market low cost, high quality instruments, control modules and counter timers.

Two particularly interesting items, from their range, are the MCM 3554/1 voltmeter and the MCF 4544/1 frequency meter. Both of these versatile digital panel mounting instruments have been designed



by Martin Kent the author of many projects published in PE.

The two instruments which are fully assembled and calibrated have many applications including uses in multimeter, thermometer and pH meter designs.

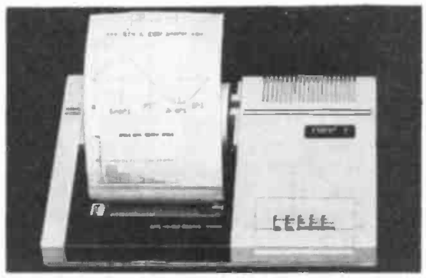
The voltmeter, based around the 7126 chip, has a ±200mV full scale and 3½ digits (0·5in high). The frequency meter, based around the 7224 chip, has three ranges (2MHz, 200kHz and 20kHz) and 4½ digits.

Both meters are available to PE readers at a special offer price (valid to 31.8.83) of £9·95 plus VAT for the voltmeter and £19·95 plus VAT for the frequency meter. Data sheets are supplied with both devices.

Martel Instruments Limited, Knight House, Foxhill Road, Southminster, Essex.

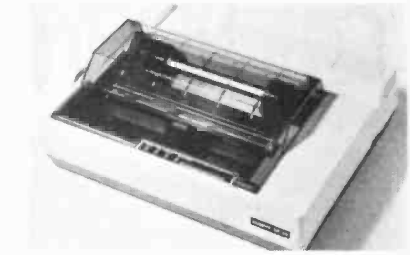
PRINTERS

Two new printers have just been launched by Oric Products and Crofton Electronics. The Oric unit which is the first peripheral for the Oric 1 is a colour system with an inter-



nal power supply and a standard Centronics interface. The printer is priced at £169.95.

The second unit is the AMD printer which is similar to the Epson having the Graftrax plus facility and is a 80 column, tractor feed machine with a parallel Cen-



tronics port. Crofton are offering the machine at a special launch price of £311·00 plus VAT and £7·50 carriage.

Crofton Electronics Ltd., 35 Grosvenor Road, Twickenham, Middlesex.

and Finally...

The recently formed Irish Amateur Computer Club is seeking to add to its throng of 70+ members, with a particular desire to enrol more "hardware specialists". The IACC currently meets at least once a month in the Power's Hotel, Dublin (second Sunday of each month 10am to 2pm). Members receive regular bulletins and newsletters, and enjoy a good range of benefits and events. Sub-groups are envisaged, concentrating on specific tasks, topics and brands of computer.

For further details contact: Nigel Carey, 166 McKee Avenue, Finglas East, Dublin 11.

Countdown . . .

Please check dates before setting out, as we cannot *guarantee* the accuracy of the information presented below. Note: some exhibitions may be trade only. If you are organising any electrical/electronics, radio or scientific event, big or small, we shall be glad to include it here. Address details to Mike Abbott.

IBM User Show July 12–14. Wembley. O
Internoise (noise control conf.) July 13–15. A7
BAEC Amateur Electronics July 16–24. Shelter, Esplanade, Penarth, S. Glamorgan. B9
Laboratory Edinburgh July 18–20. University. E
Star '83 Aerospace July 21–24. RAF Greenham Common. Z1
Acorn Exhibition Aug. 25–28. Cunard Int. Hotel, Hammersmith, London. J3
BARTAG Rally (radio teleprinter) Aug. 29. Sandown Park, Esher, Surrey. E2
Light Aviation Show Sept. 1–3. Cranfield Institute, Bedfordshire. Z1
Electro West Sept. 6–8. Bristol Exhibition Centre. Q
CAST (Cable And Satellite Television) Sept. 11–14. NEC. F5
Weldex Sept. 12–16. NEC B/ham. I
Testmex Sept. 13–15. Grosvenor House, Park Lane, London. E
Home Entertainment Spectacular Sept. 17–25. Olympia. I2
Peterborough R & ES Mobile Rally Sept. 18. Wirrina Stadium, Bishops Rd., Peterborough. L2
Personal Computer World Show Sept. 28–Oct. 2. London. M
Laboratory London Oct. 12–14. Barbican Centre. E
Drives/Motors/Controls Oct. 12–14. Leeds University. E
Computer Graphics Oct. 18–20. Wembley. O
PARC (computers in architecture, conf.) Oct. 18–20.Wembley. O
International Business Show Oct. 18–26. NEC. T
Business Efficiency Exhibition Oct. 22–26. Earls Court, London. Z
Electronics Hobbies Fair Oct. 27–30. Alex Pavilion, London. Z1
Electronic Displays Nov. 1–3. Kensington Ex. Centre, London. D4
Brainwave (computing/video) Nov. 4–6. NEC Birmingham. G2
Compec Nov. 15–18. Olympia, London. Z1
Northern Computer Fair Nov. 24–26. Belle Vue, Manchester. Z1
Intron Nov. 22–24. RDS Hall, Dublin. V
Automatic Testing/Test/Instruments. Dec. 13–15. Metropole, Brighton. D4

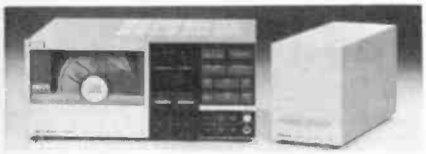
A7	Institute of Acoustics ✆ 031-225 2143
B9	Cyril Bogod, British Am. Elect. Club ✆ 0222 707813
D4	Network ✆ 02802 5226
E	Evan Steadman ✆ 0799 22612
E2	BARTG 89 Linden Gdns., Enfield, Middx.
F5	Cable & Satellite ✆ 01-487 4937
G2	Clapp & Poliak ✆ 01-747 3131
I	Industrial Trade Fairs ✆ 021 705 6707
I2	Alan Taylor ✆ 01-486 1951
J3	Computer Marketplace ✆ 01-930 1612
L2	D. T. Wilson, 4 Conway Ave., Peterborough
M	Montbuild ✆ 01-486 1951
O	Online ✆ 09274 28211
Q	Exhibitions for Industry ✆ 08833 4371
T	Trident ✆ 0822 4671
V	SDL Exhibitions ✆ Dublin 763 871
Z	BETA Exhibitions ✆ 01-405 6233
Z1	IPC Exhibitions ✆ 01-643 8040

...SPRING

COMPACT DISC SYSTEMS

This year's Spring Trade Shows saw the arrival of the audio compact disc (CD), the revolution in recorded sound. Since its launch back in March of this year every major record company has announced that it will enthusiastically support the CD format.

It is estimated that over 1000 titles will be available by the end of the year and most of these will be made in Hanover, West Germany by PolyGram but plans are already underway by two UK manufacturing companies to establish CD pressing plants in this country.



The Fisher AD800

The real breakthrough with CD has been that both the hardware and software producers worldwide have accepted the format originally developed jointly by Sony and Philips as the world standard with over 30 manufacturers now licensed.

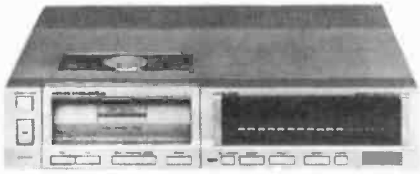
Although at around £500 the systems are expensive many retailers believe the sales of CD units will be followed by an increase in speaker and amplifier sales because many people will prefer to buy their new systems from scratch.

For this reason Philips have produced a "flat membrane" range of speakers which they have designed for use with CD. The company say the new speakers reduce distortion and improve the overall sound quality when compared to normal speakers on both CD and conventional systems.

Another manufacturer following this line of thought is Pioneer who have updated their HPM series of speakers with power capabilities ranging from 90W to 240W.

Included in the wide range of models on show were the Fisher AD800, the Marantz CD–73 and the Hitachi DA100.

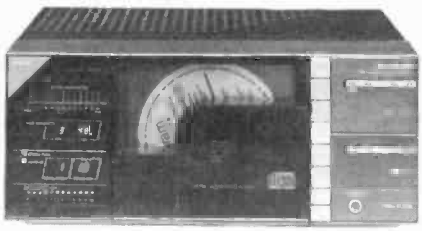
The Fisher AD800 model is fitted with a detachable storage unit which can hold up to five discs and enables the AD800 to fit a 19in. rack system. Once the disc is placed in the holder it is automatically taken into the unit and the front loading door closed. The AD800 allows easy selection search of 16 tracks in any sequence and touch controls include fast forward, reverse/play/pause and stop. Priced at £479·95 inc. VAT the AD800 comes complete with the ADP105 CD storage unit.



The Marantz CD–73

The Marantz CD–73 system is a drawer loading unit which can be programmed to play track selections in any order, to skip specific tracks or to repeat them. The CD–73 is priced at £559·90 including VAT.

The Hitachi DA100 also has random programming and skip features and includes a disc scan facility which when used will give a brief sample of the current disc program and then advances to a point 30 seconds ahead on the disc and plays another brief sample. The DA100 is priced at around £500.



The Hitachi DA100

SORD GAMES

The home computer market abounds with versatile machines competing for our custom and the M5 is no exception. Manufactured by Sord of Japan and marketed in the UK by Computer Games Ltd its graphic capabilities will undoubtedly be the main selling point. With sixteen colours available the user will be able to create impressive animations from scratch or by using a pre-programmed cassette. With a BASIC 1 manual, p.s.u., connecting leads and two game cassette the M5 will retail at around £190 inc VAT.

Interestingly, 'joypads' will also be available—the joy 'stick' being replaced by a rather large button which when pressed at the relevant point on its circumference will transfer that directional information.

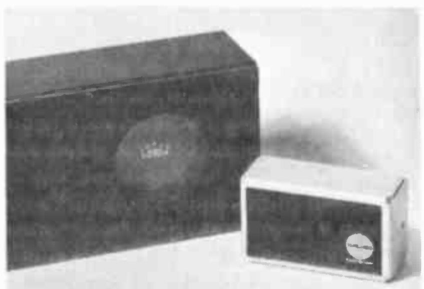
Also from CGL are a range of chess computer games including the Pocket Micro with a folding board. Players will be able to interrupt a game at any stage, pack it away and re-start at a later date. This feature will make the game unique, it will retail at around £32.

MINI-MINDER

With the ever-increasing popularity of home intruder detection systems comes the inevitable jockeying for market position by the manufacturers.

Songuard are offering a system which incorporates an ultrasonic device that can be placed where protection is needed without actually running any wires. Known as the Songuard Bug it will act as a miniature detector and can be attached to doors, windows, cupboards or even the jewellery box. What's the catch? Well the only non-wiring is between the device and its receiver, but it is indeed a very handy contrivance. The freestanding detector and alarm unit will retail at around £169.

The Songuard system is modular and also includes personal attack buttons, entry/exit keyswitch units and internal/external siren units. All auxiliary paraphernalia is also available from Songuard, Sales and Service, Mill Mead, Staines, Middlesex (0784 62016).



TRADE SHOWS

WATER BABY

Remember when the Walkman units first encouraged us to whistle while we worked, or jog with Jimmy Young? Well if you so desire you can now sing in the surf with a completely waterproof and sand-resistant model. The Sony Sports Walkman WMF5 has a disc drive system designed to reduce distortion. It incorporates an FM tuner and belt-clamp.

The Walkman will soon be available from retailers at around £111.

On the other side of the micro-electronic fence comes a new range of calculators from Sharp. A series of packs is the latest idea and besides the usual scientific types we now have one for the shopper, motorist, student, handyman, salesman and lady. There is also of course the inevitable school-pack which includes the ever-popular ruler, protractor and compasses etc. Function permutations are immense and it seems to make good sense to keep calculators simple and direct the resultant machines at a particular market requirement, hence the new range.

HOME PHONE SYSTEMS

The telephone which seems to have been forgotten by everyone as a consumer product has recently been enjoying a revival of interest due to two new designs from Fidelity Radio.

The Wanderer

The first is the Fidelity Wanderer a completely cordless handset which can be used up to 200 metres from its base unit. The base unit itself is plugged into the normal BT socket and is also connected to the mains. The cordless handset incorporates a push-button dialling system and operates on frequencies of 47·46/47·54 MHz from the handset to the base and 1·642/1·782 MHz from the base to the handset. The unit also features a unique digital coding system to prevent unauthorised dialling from other handsets in the same locality, a single push-button redial facility, a memory which stores a number entered whilst the phone is in use (ideal for Directory Enquiries), a call button on the base unit to page the handset user and an automatic recharging system for the Ni-Cad batteries. The Wanderer will retail at around £170.

The CRP 100

The TAS–1G

The second design is the clock radio phone, the CRP 100, which incorporates the three facilities of a radio, alarm clock and telephone in one unit. It operates in precisely the same way as a conventional clock radio but has an automatic cut off when the telephone receiver is lifted. The radio operates an LW, MW and FM with selector switches for the radio, alarm radio, alarm buzz and off. A snooze touch sensor is provided and the readout is from a red l.e.d. display.

The TAS–1G from Sanyo is a basic telephone answering system which has several interesting features particularly its ability to detect the pay-tone from call-boxes. The machine accepts the call but automatically pauses until the pay-tone has finished before giving its recorded message. This avoids the caller losing part or possibly all of the message whilst the coins are being inserted. It will retail at around £148.

NO CHARGE

Rechargeable batteries are becoming increasingly popular and Sanyo, the largest manufacturer of Ni-Cads, have experienced a doubling of demand over the last year for batteries and chargers in the UK.

To maintain their market position Sanyo have updated their Cadnica range of batteries, improving their sealing so they remain leakproof longer and enhancing the overcharge and overdischarge (forced discharge) resistance. A typical forced discharge occurs when batteries with different levels of charge are not fully recharged and therefore balanced before being used in one piece of equipment.

Sanyo have also introduced a new universal multicharger, the NC1239, which is capable of charging every battery in their range, whilst the NC–AM1 charger for HP7 batteries is a solar powered system which is driven by a high power solar panel developed by Sanyo.

6 *Simple* SOLAR POWERED PROJECTS

R.A. PENFOLD

ON the face of it there is no point in having designs for solar powered projects since any electronic project could be powered from a suitable array of solar cells. While this is indeed true, it does not take into account the fact that most solar cells are only capable of providing quite small currents, and all solar cells provide a modest output voltage of only about 500 millivolts. Most electronic projects would, therefore, require a large array of medium or high current cells in order to produce sufficient power, even under good operating conditions.

Although the difference in cost between solar cells and ordinary batteries has tended to reduce over the years, for most purposes a large array of solar cells is not a practical proposition. Of course, all these projects can be battery operated if so desired.

M/W RADIO

THE MW radio, like the other five projects in this set, has been designed to operate at low levels of supply voltage and current. In fact, this receiver will operate quite well at a supply voltage of 1 volt with a current consumption of under 1 milliamp. In other words it requires an input power of under 1 milliwatt for satisfactory results! Under reasonably bright conditions this enables the set to operate from just two small solar cells.

THE CIRCUIT

The receiver is a simple MW Band type which has a ferrite rod aerial and an output which is intended to drive a crystal earphone (and which is unlikely to be suitable for any other type of earphone or headphones). Circuits using a couple of silicon transistors were tried, but the final design gave significantly superior results using a ZN414 plus a single transistor audio stage, and the full circuit of the set is shown in Fig. 1.

The ZN414 is ideal for this type of application as it gives a level of performance which is superior to that provided by most discrete T.R.F. designs, and it requires a nominal supply potential of only about 1·2 volts at a supply current of approximately 1 milliamp. It provides r.f. amplification, a.m. demodulation, and a simple automatic gain control (A.G.C.) action.

The ZN414 has a high input impedance so that it can be fed direct from the tuned winding of the ferrite aerial and the low impedance coupling winding is left unused. R1 is used to bias IC1 via the aerial winding (so that this resistor does not shunt the input impedance of IC1), and C1 couples one end of the ferrite aerial to the negative supply rail. R2 is the load resistor for IC1 and C2 is the r.f. filter capacitor for the detector stage of IC1. Note that IC1 obtains its positive supply only via R2 and there is no direct connection from IC1 to the positive supply rail.

The audio output level from IC1 is up to about 30

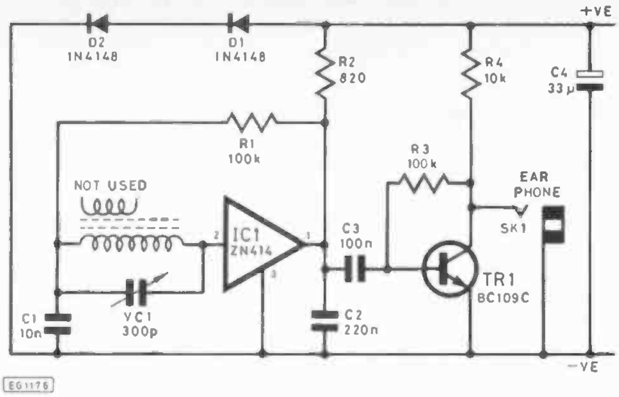


Fig. 1. Circuit diagram of the MW Radio

millivolts r.m.s., and this is just about sufficient to drive a crystal earphone at reasonable volume. However, better results are obtained using a small amount of audio amplification, especially when receiving weaker stations or when the supply voltage has fallen to a barely adequate level.

A simple common emitter audio amplifier based on TR1 is therefore used to boost the output from IC1. An amplifier of this type would normally be expected to have a voltage gain of about 40dB (one hundred times) or more, but in this case the voltage gain obtained is only about 20dB (ten times) or

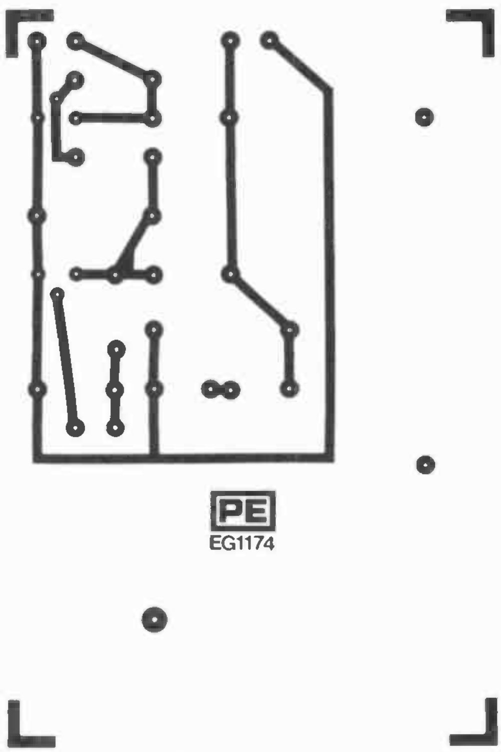


Fig. 2. P.c.b. design

so due to the very low levels of collector current and voltage that are used.

D1 and D2 are used to prevent the supply voltage from exceeding a suitable level, and C1 is a supply decoupling and smoothing capacitor. The output from the solar cells can contain a certain amount of noise, including mains hum if an artificial light source is used to power the circuit. Noise is not too much of a problem, though, mainly due to the very slow response time of solar cells, and C4 should give adequate smoothing when necessary.

CONSTRUCTION

With the only exceptions being the earphone socket (SK1) and solar cells the components are mounted on the printed circuit board. Details of the printed circuit are shown in Fig. 2 with the component layout shown in Fig. 3.

The specified tuning capacitor requires a single 10mm diameter mounting hole, and the mounting bush and nut of this component can be used to effectively bolt the completed board inside the case. Note that the case must be made from a non-metallic substance, otherwise it will screen the ferrite aerial and prevent any signal pick-up. With a little ingenuity it should be possible to use any variable capacitor having a maximum value of about 250p to 350p in the VC1 position.

The ferrite aerial used in the prototype is an Ambit MWC2 aerial coil fitted on a 140mm x 9·5mm ferrite rod which is in turn mounted on the printed circuit board using a pair of plastic mounting clips. These are bolted to the board using short 6BA bolts and fixing nuts. The set also works well using a Denco MW5FR ferrite aerial (which comes complete with a 140mm long ferrite rod), and this can be mounted on the board using a couple of large "P" type cable grips. The unit should, in fact, work perfectly well using any normal

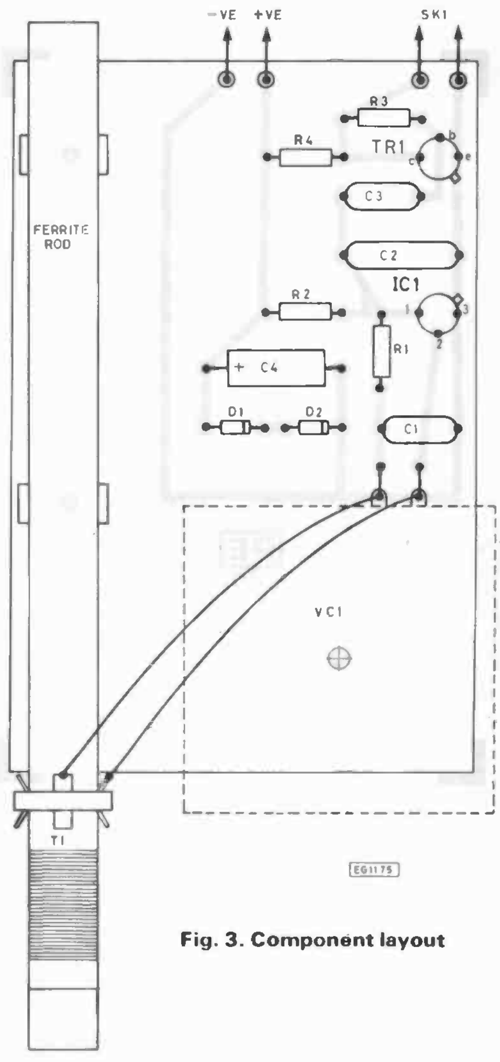


Fig. 3. Component layout

medium-wave ferrite aerial. Whatever aerial is used, only the larger winding is used and the small coupling winding is either removed or just ignored.

It is possible to use a shorter ferrite rod if a 140mm type will be too long to fit in the selected case. It is also possible to break a piece from a ferrite rod to shorten it, but sawing through the rod is practically impossible as ferrite is an extremely hard material. The rod can usually be persuaded to break at the desired point by filing or cutting a groove around the rod at this point, but great care must be taken when breaking the rod. It can easily take three whole rods to make one half if due care is not taken. Do not use a ferrite rod of less than about 75mm in length.

Obviously the solar cells must be mounted on the exterior of the case with the sensitive surface facing outwards. The set will operate from a couple of MS4A solar cells in direct sunlight, even if this is of the weak winter variety. However, three cells give better results and enables the set to work even in bright overcast conditions. The solar cells are connected in series, and with the MS4A type the sensitive surface is the dark side of the component. It is the negative leadout wire which connects to this side of the cell and the positive leadout which connects to the underside of the device.

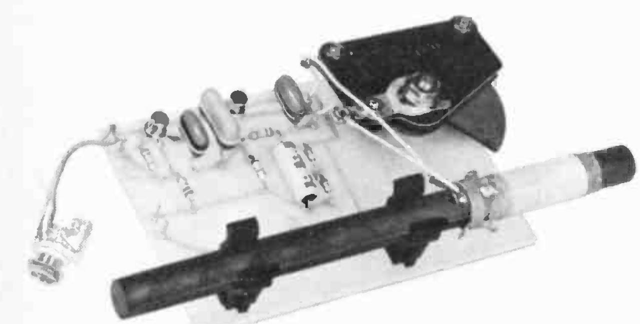
As the circuit has such a low current requirement it should be possible to use any other solar cells as a power source, although very high current types would not be a very practical choice. Medium current types do not really have any advantage over low current types in applications where only a low current is required. The output voltage from a solar cell remains virtually constant as the load current is increased until a certain threshold level is reached, and the output voltage then falls sharply with the output current remaining virtually constant. If the light level received by the cell is reduced this gives a reduction in the output voltage, and the voltage obtained will be virtually the same whether a low or high current cell is used.

For operation in relatively low light levels it is therefore necessary to use several cells in series rather than just using two or three high current cells. Using a dozen or more cells in series is not an economically attractive proposition, but inexpensive 6, 9 and 12 volt solar panels are available and represent a more practical alternative. Using a 9 volt panel it was found to be possible to operate the set even on a dull winter day, or from artificial light (which provides a similar light level).

IN USE

The position of the coil on the ferrite rod controls the frequency coverage of the receiver to some extent, and the coil must be placed in a position that permits full coverage of the band. VC1 gives slightly more than complete coverage of the MW Band, and this slight excess of coverage prevents the positioning of the coil from being too critical.

Despite the simple A.G.C. action of the ZN414 the set can be overloaded in strong reception areas, but if necessary the directivity of the ferrite aerial can be used to reduce the strength of received signals. ★



COMPONENTS ...

Resistors

R1, R3	100k (2 off)
R2	820
R4	10k

All resistors ¼W 5% carbon

Capacitors

C1	10n polyester
C2	220n polyester
C3	100n polyester
C4	33µ 16V axial elect

Semiconductors

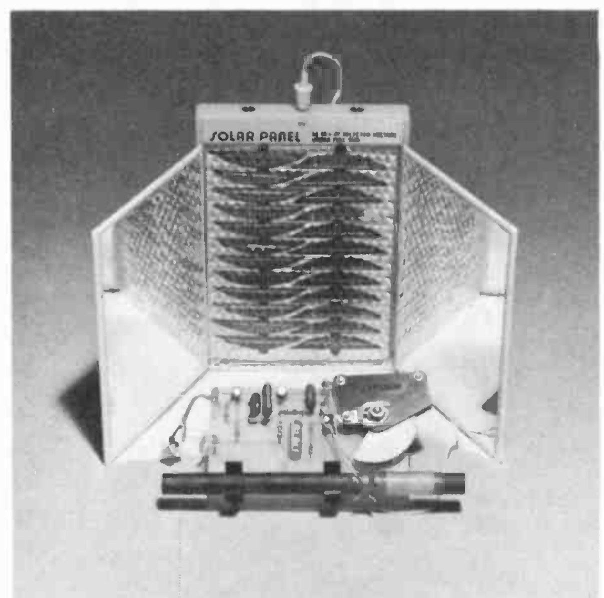
D1, D2	1N4148 (2 off)
TR1	BC109C
IC1	ZN414

Miscellaneous

	Medium wave ferrite aerial with mounting clips
VC1	300p solid dielectric (Jackson Dilecon)
SK1	3·5mm jack socket
	Printed circuit board
	Control knobs
	Three MS4A solar cells or solar panel (RK23A)
	Wire, solder, etc.

Constructor's Note

The solar power cells MS4A and panels are available from **Maplin Electronic Supplies Ltd., P.O. Box 3, Rayleigh, Essex.**



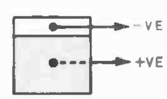


Fig. 4. Connection diagram for the MS4A solar cell

EG1203

SOIL MOISTURE METER

A SOIL moisture meter is really just a form of resistance indicator, and units of this type rely on the fact that the resistance through dry soil is very much higher than the resistance through a comparable sample of moist soil. Soil moisture meters are used primarily with potted plants where the surface of the soil can be very dry even though the soil only a little deeper may be quite wet. This can lead to over-watering and possibly the demise of the plant. The probes of a soil moisture meter avoid this by penetrating about 25 to 50mm below the surface of the soil so that the moisture reading obtained does not just indicate the moisture content of the surface soil, and can be used as a reliable guide.

Circuits of this kind indicate the soil moisture content in a variety of ways such as producing an audio tone that rises in pitch with increasing moisture content, or having a l.e.d. indicator which flashes at a rate that depends on the water content of the soil. A number of systems were tried, and the one finally adopted was to simply use a low cost moving coil meter to provide the moisture indication. This may seem less imaginative than the alternative methods, but it gives a clear and unambiguous indication of the soil's moisture content, and it enables a low voltage low current circuit to be used.

THE CIRCUIT

The very simple circuit of the Soil Moisture Meter appears in Fig. 1. Using a circuit consisting merely of the probes and the meter connected in series across a low voltage supply was found to give a slightly inadequate level of sensitivity. The final circuit, therefore, uses an emitter follower buffer stage to drive the meter, and R2 is used to shunt the input of this stage so that the sensitivity of the unit can be adjusted and set at a level that makes it easy to interpret meter readings.

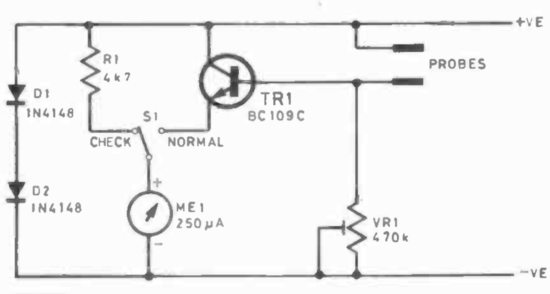


Fig. 1. Circuit diagram

D1 and D2 stabilise the supply voltage at about 1·3 volts so that consistent results are obtained. S1 can be used to switch ME1 across the supply lines (via series resistor R1) so that a check to ensure that an adequate supply voltage is present can be made.

Under direct sunlight two solar cells in series are sufficient to power the circuit, but it would probably be better to use three cells in series as the unit would then operate on any reasonably bright day. Using a solar panel as the power source, the unit would operate under comparatively dim conditions, and the actual power level taken by the circuit is only about 0·5mW or less.

CONSTRUCTION

Fig. 2 shows the printed circuit design for the Soil Moisture Meter. If the specified meter is used the completed board can be soldered onto the tags of the meter, and the tags can be bent through 90 degrees so that the board fits vertically behind the meter. It should be possible to use any meter having a full scale deflection sensitivity of about 1mA or less.

The probes can be made from a pair of inexpensive test prods of the type sold as replacements for multimeters. The two prods must be fixed together so that they are a constant distance apart when measurements are made and consistent results are obtained. There should be no problem in gluing or taping the two prods firmly together. Of course, any similar arrangement which provides a couple of thin metal prods about 25 to 50mm long should work equally well.

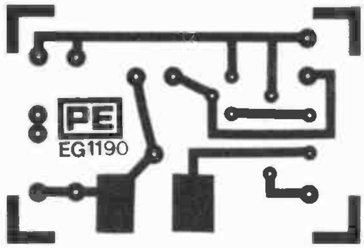


Fig. 2: P.c.b. design

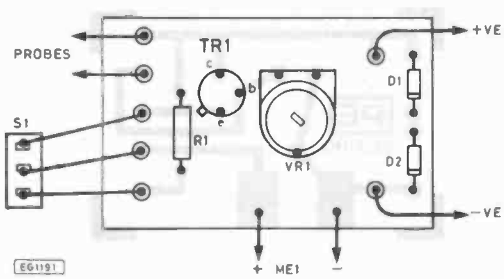


Fig. 3. Component layout

ADJUSTMENT

It is important to carefully adjust VR2 to give the unit a suitable level of sensitivity if the unit is to give useful and helpful results. The most reliable way of setting VR2 is to first set up a few samples of soil having various moisture levels. VR2 should be given a setting that only gives a large deflection of the meter with the probes pushed into moist soil

COMPONENTS . . .

Resistors

R1	4k7 ¼W 5% carbon
VR1	470k 0·1W hor. preset

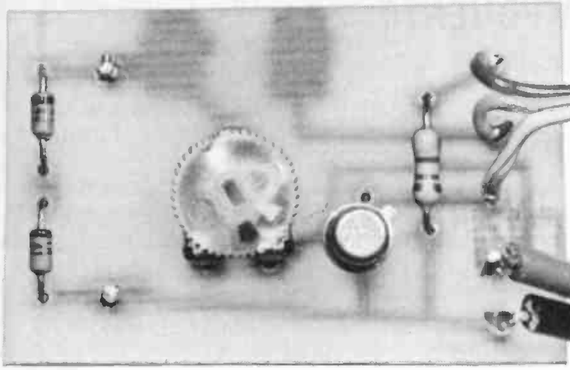
Semiconductors

D1,D2	IN4148 (2 off)
TR1	BC109C

Miscellaneous

ME1	250µA moving coil meter (Maplin, see text)
S1	Toggle, push-button or slider type switch s.p.d.t.

Pair of test prods and leads
Printed circuit board
Three MS4A solar cells or solar panel (Maplin)
Wire, solder, etc.



samples. The purpose of the unit is really to indicate whether or not the soil is excessively dry rather than how wet it is, and with the unit adjusted in this way a low reading on the meter will indicate that watering is needed. Always make sure that the probes are pushed right down into the soil and are making good contact with it.

With the solar cells subjected to a strong light level, set S1 to the "check" position and make a note of the reading on the meter (this should be about 80 or 90% of full scale deflection). On any future occasions when the unit is used, if there are any doubts about the adequacy of the light level the battery check facility can be used to check the supply voltage, and the reading obtained should not be substantially lower than that obtained when making this initial trial. Note that the value of R1 will need to be altered if a meter having a full scale sensitivity other than 250µA is used, and the change in value is inversely proportional to the change in meter sensitivity (e.g. R1 should be about 1k2 using a 1mA meter. ★

THERMOMETER

THIS thermometer covers a range of zero to one hundred degrees centigrade, and despite the simplicity of the circuit it provides accurate results that are primarily limited by the accuracy with which the meter can be read. The sensor is a silicon diode which can be located remotely if desired, and connected to the rest of the circuit by a twin lead.

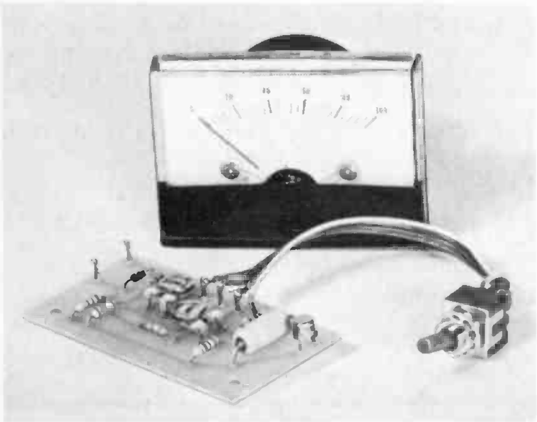
The circuit is designed to be powered from a solar panel, but a supply potential of only about 1·2 volts at a current of approximately 1·2 milliamps is required and the unit could be powered from three small solar cells under reasonably strong light.

THE CIRCUIT

A simple bridge circuit is used, and the circuit diagram of the thermometer appears in Fig. 1. One side of the bridge circuit is formed by R4 and sensor diode D2. The latter is forward biased and a potential of about 0·6 volts is therefore produced across this component, but the precise voltage produced will vary slightly from one component to another, and more importantly, it varies with temperature. A reasonably linear relationship between temperature change and voltage change is obtained, with increased temperature giving a reduction in voltage. However, the voltage change is not very great, and is likely to be only about 2 millivolts or so per degree centigrade. With a thermometer that covers a range of one hundred degrees centigrade this gives a voltage swing of about two hundred to two hundred and fifty millivolts over the full temperature span, and this is sufficient to drive a moving coil meter without the need for any amplification.

The second section of the bridge circuit is formed by R1, R2 and VR1 is adjusted so that the bridge is balanced and the meter reads zero with D2 at zero degrees centigrade. If the sensor is then raised in temperature the voltage at the negative terminal of ME1 reduces, and a forward deflection of the meter is produced. VR2 is adjusted to give the circuit the correct sensitivity so that (say) a fifty degree rise in temperature would give a reading of fifty microamps on ME1. The existing zero to one hundred scale of the meter can therefore be retained.

It is essential for the supply fed to the bridge circuit to be extremely stable indeed as a change in supply voltage of just a few tens of millivolts would give a significant change in the reading on ME1 and hopeless accuracy. Using a simple shunt regulator circuit with a couple of forward biased silicon diodes in series would not be adequate in this case, and it is necessary to use a precision, temperature compensated, voltage reference. D1 is a precision 1·2 volt shunt stabiliser, and R5 is its load resistor. D3 ensures that the input potential cannot rise to a level that would produce an excessive current through D1 and a consequent loss of regulation efficiency.



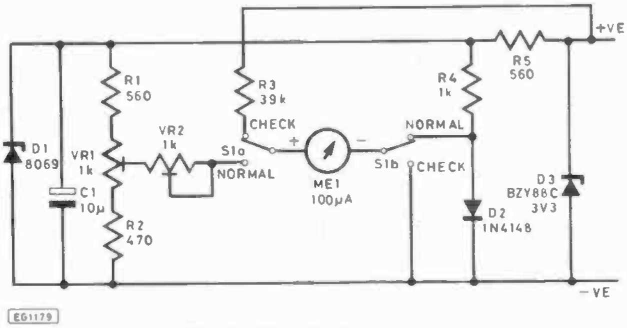
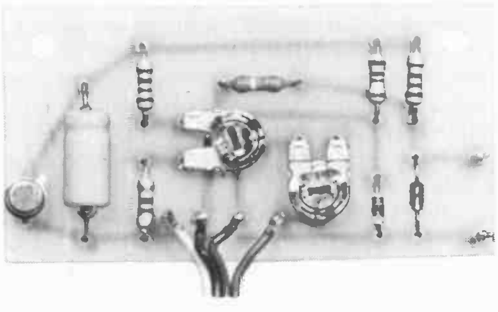


Fig. 1. Circuit diagram



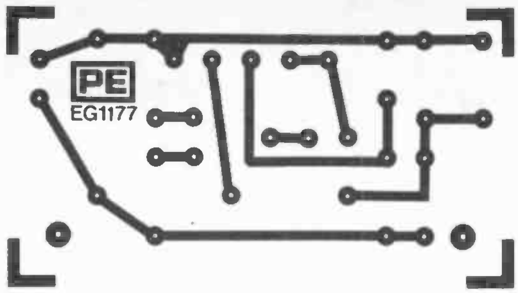


Fig. 2. P.c.b. design

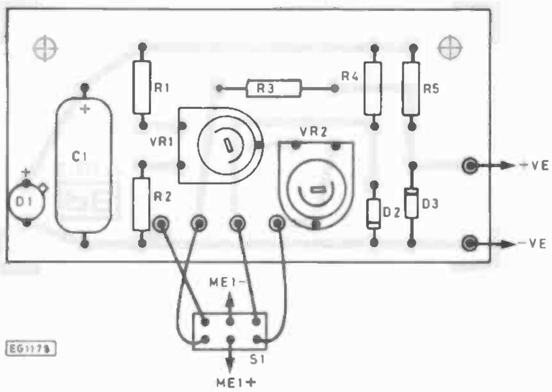


Fig. 3. Component layout

COMPONENTS . . .

Resistors

R1, R5	560 (2 off)
R2	470
R3	39k
R4	1k
VR1, VR2	1k 0·1W hor. preset (2 off)
All resistors $\frac{1}{4}$W 5% carbon	

Capacitor

C1	10µ 25V axial elect

Semiconductors

D1	8069 precision 1·2 volt reference
D2	1N4148
D3	BZY88C3V3 3·3 volt 400mW Zener

Miscellaneous

ME1	100µA moving coil panel meter
S1	Miniature toggle type d.p.d.t.
	Solar cells or solar panel (Maplin)
	Printed circuit board
	Wire, solder, etc.

If the circuit is operated from three small solar cells in series (such as MS4As) D3 can be omitted since the available supply current would be inadequate to overdrive D1. R5 should be reduced to about 56 ohms in value as well.

S1 can be used to connect ME1 across the input from the solar cells, and series resistor R3 gives ME1 a full scale sensitivity of about 4 volts. This enables a check to be made to ensure that an adequate input voltage is present.

CONSTRUCTION

The printed circuit design and wiring are shown in Figs. 2 and 3. Sensor diode D2 is shown as being mounted on the printed circuit board, but as mentioned earlier, it can be remotely located and connected to the main unit via a twin cable if desired. Even if it will eventually be mounted on the board it is a good idea to initially connect it to the board by way of a twin lead about half a metre or so in length as this will make it easier to set-up the unit ready for use.

Initially VR1 should be set with the wiper at about the middle of its track, and VR2 should be adjusted for maximum resistance (set fully anticlockwise). With D2 placed in ice cubes or iced water to reduce its temperature to zero centigrade and S1 set to the "normal" position, with power connected to the circuit VR1 should be adjusted immediately to zero the meter. D2 is then placed in warm water to increase its temperature to anything from about 50 to 100 degrees centigrade, but a thermometer must be used to measure the temperature of the water so that VR2 can be adjusted to give the appropriate reading on ME1. This procedure should then be repeated a few times to make sure VR1 and VR2 are set accurately.

With S1 placed in the "check" position ME1 should read at least half full scale deflection, and there is inadequate voltage from the solar cells if it does not. If the unit is powered from three small solar cells a slightly lower reading of about 30% of full scale deflection is acceptable. If this method of powering the unit is adopted it is a good idea to check the reading obtained with the cells in direct and fairly strong sunlight. If a significantly lower reading is obtained at some later occasion the supply potential is inadequate. ★

INEBRIATION DETECTOR

THIS inebriation detector is really a simple reaction testing game using a row of eight light emitting diodes to give a relative indication of the operator's reaction speed. The unit is very simple to use, and about ten seconds after switch-on the first l.e.d. in the display switches on, and a push button switch must then be operated as quickly as possible. Soon after the first l.e.d. has switched on it cuts off again and the second l.e.d. lights instead, then this l.e.d. cuts off and the third l.e.d. lights up, and so on with the light appearing to move along the display. Operating the push button halts the display, and the quicker the button is operated the less far the light will have progressed along the display. Thus any degradation in reaction speed due to the consumption of alcohol can be detected.

To start a new sequence the push button is released, the circuit is reset by switching off, and a new cycle commences when the unit is switched on again. The push button must be held down until the score has been read from the display as the display will continue to operate when the button is released.

This circuit requires somewhat more power than the other five solar powered projects, but it still only requires about 4 to 9 volts at a few milliamps in order to operate reliably. It can therefore be powered from a 6 or 9 volt solar panel in reasonably strong light.

THE CIRCUIT

The circuit is comprised of two main stages: a clock oscillator and the display driver. Fig. 1 shows the full circuit diagram of the Inebriation Detector.

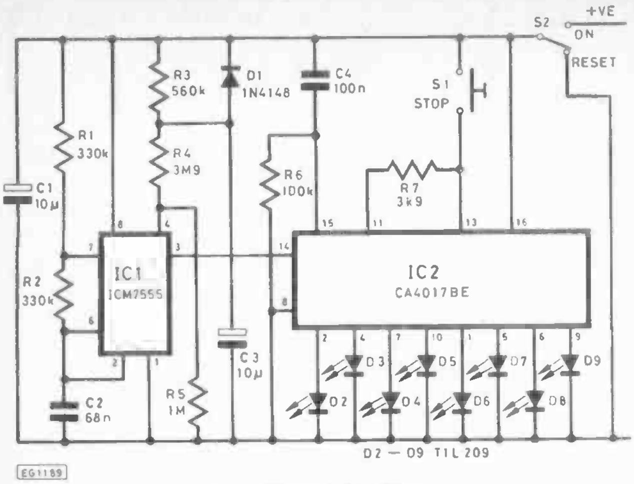
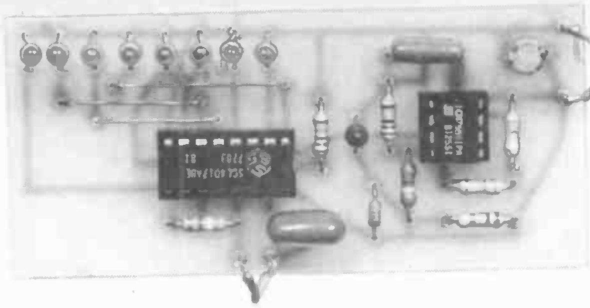


Fig. 1. Circuit diagram

The clock oscillator uses an ICM7555 (IC1) and this also provides the delay between switch-on and the display starting to count. IC1 is used in what is virtually the standard 555 astable configuration, and the values used for timing components R1, R2 and C2, give an operating frequency of about 20 hertz. With an eight l.e.d. display and human reaction times normally between about 200 and 400 milliseconds, this clock frequency should be suitable, but if necessary the clock can be made to run a little faster by reducing C2 to 47n, or a little slower by increasing it to 100n.

The clock oscillator is given a switch-on delay by providing a suitable control voltage to pin 4 of the device using a simple C–R timing circuit. Operation of IC1 is blocked if pin 4 is taken to less than about 0·5 volts, and at switch-on R5 takes this terminal to the negative supply potential so that oscillation is blocked. However, as C3 charges via R3 part of the potential across C3 is fed to pin 4 of IC1 by the potential divider formed by R4 and R5. After approximately ten seconds the potential at pin 4 becomes sufficient to activate IC1 and the clock signal is produced at pin 3 of the device.



It is impossible to specify the switch-on delay time with any degree of accuracy since it varies considerably with fluctuations in the supply voltage. However, this is not really a disadvantage since it makes it impossible to predict the time when the display will start to operate and prevents contestants from obtaining low scores by having good anticipation rather than good reactions.

A CMOS 4017BE is used as the display driver, and at switch-on this is reset by the positive pulse generated by C4 and R6. Output "0" of the device then goes high while the other nine outputs are low. There is no l.e.d. connected to this output of the device (pin 3) and all eight display l.e.d.s are therefore switched off at this stage.

When the clock oscillator starts to operate, the 4017 is incremented by each clock pulse. Thus the first clock pulse causes output "1" to go high and D2 is switched on, the next clock pulse sends output "2" high and D3 switches on in place of D2, then output "3" goes high and D4 switches on, and so on. This continues until S1 is operated so that the

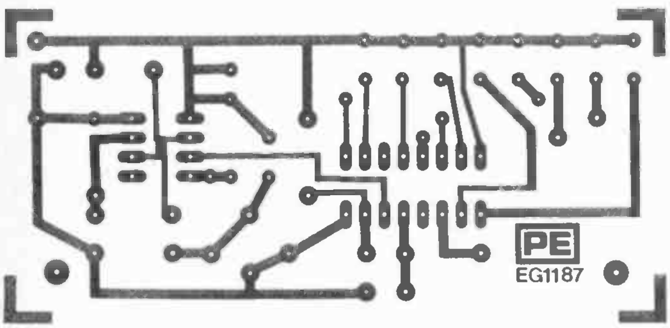


Fig. 2. P.c.b. design

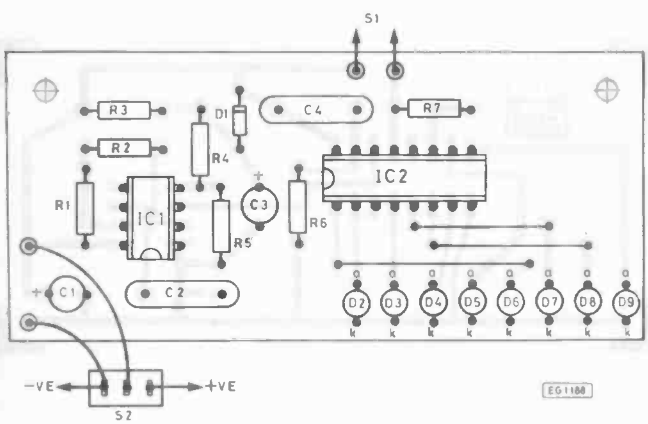


Fig. 3. Component layout

COMPONENTS . . .

Resistors

R1, R2	330k (2 off)
R3	560k
R4	3M9
R5	1M
R6	100k
R7	3k9

All resistors ¼W 5% carbon

Capacitors

C1	10μ 16V radial elect
C2	68n polyester
C3	1·0μ 16V tantalum
C4	100n polyester

Semiconductors

D1	1N4148
D2 to D9	TIL209 3mm red l.e.d.s (8 off)
IC1	ICM7555
IC2	4017BE

Miscellaneous

S1	Push to make, release to break type
S2	Miniature toggle switch s.p.d.t.
	Printed circuit board
	Solar panel (Maplin)
	Wire, solder, etc.

clock inhibit terminal of IC2 is taken high and the counting action is halted. The display then stops, and whatever l.e.d. happened to be switched on at the instant S1 was operated remains switched on so that the player's score is shown on the display.

If S1 is operated too slowly, output "9" of IC2 (pin 11) goes high, and due to the coupling through R7 it takes the clock inhibit terminal high so that the count is halted and the display does not continuously cycle through "0" to "9". This prevents a score from being obtained if S1 is operated too slowly.

When S2 is set to the "reset" position a short circuit is placed on the supply lines so that C1 and C4 discharge fairly rapidly, and the unit operates properly when S2 is set back to the "on" position. D1 is included so that C3 is also discharged and a new switch-on delay is produced when the unit is switched on again.

CONSTRUCTION

Construction of the unit is quite straight forward using the printed circuit design shown in Fig. 2. Note that there are three link wires on the board (Fig. 3) just above the display l.e.d.s. IC2 is a CMOS device and the usual MOS handling precautions should therefore be implemented, and IC2 should be fitted in a 16 pin d.i.l. socket. IC1 is also a CMOS component, but it has internal protection circuitry which renders MOS handling precautions unnecessary. As the ICM7555 is not the cheapest of i.c.s it is still probably worthwhile using a socket for this device.

As mentioned earlier, a solar panel is probably the best power source for this project since it would be uneconomic to buy a sufficiently large number of single cells (at least eight would be needed). The solar panel could be mounted on the case of the unit, but in use it would probably be more convenient to leave the inebriation detector and solar panel as separate units. The panels are provided complete with about one metre of twin cable, and this can be terminated in a 3·5mm jack plug with a matching power socket being mounted on the case of the inebriation detector.

If the output from the panel falls to an inadequate level either no operation at all will be obtained, or the first l.e.d. in the display might light up after the switch-on delay, but loading of the supply will produce a large voltage drop which will result in the display progressing no further. Adding a capacitor of about 680µ in value across the solar panel helps to give proper results in marginal lighting conditions, but obviously this can be of no help if the light level is totally inadequate. ★

CONTINUITY TESTER

THIS very simple continuity tester produces an audio tone when a suitably low resistance is present across the test probes, and unlike some continuity tester designs it will not indicate continuity if a forward biased silicon junction is placed across the test prods. This helps to avoid confusing results when checking complex circuit boards where there can be a large number of semiconductor junctions and continuity would otherwise be indicated between virtually any two points in the circuit!

In order to keep the voltage and current requirements of the circuit to a minimum, it is based on the LM3909N low power oscillator i.c. This gives a very high level of efficiency and the unit will produce an audio tone of moderate volume from an input of only about 1·3 volts at a supply current of around 3 milliamps.

Fig. 1 shows the LM3909N in block diagram form, and as can be seen from this, the device is little more than an electronic switch. The LM3909N can be used in a variety of configurations to suit particular applications, but it is always used in what is really a simple relaxation oscillator circuit.

THE CIRCUIT

The full circuit diagram of the Continuity Tester is shown in Fig. 2. In this circuit the LM3909N is used in its most simple configuration, and although this does not give quite the efficiency of some of the alternative configurations, it gives good results and excellent reliability at very low supply voltages. All that happens using this arrangement is that C2 charges via LS1 and R1 until the control voltage for the electronic switch falls below the trigger threshold, and the switch then closes so that LS1 is effectively connected across the supply rails and therefore passes a high current. It is not necessary for the solar cells to be able to provide the full current required by LS1 since it is only a short pulse of current that flows, and supply decoupling capacitor C1 can provide some of this current. During the periods when the electronic switch is in the off state the current consumption of the circuit is quite low and C1 can then recharge so that it is ready to supply another current pulse when the switch closes again. The circuit will oscillate with C1 removed, but the volume obtained is reduced drastically.

The electronic switch does not hold in the on state because once it has closed C2 discharges through R1 and

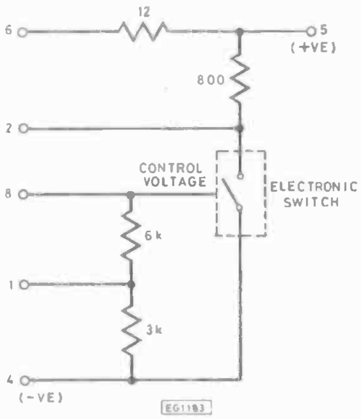


Fig. 1. Basic circuit

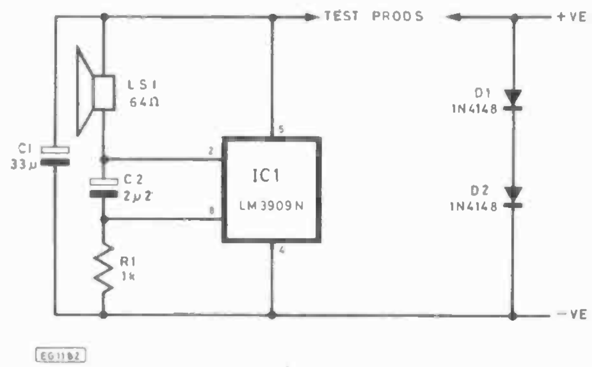


Fig. 2. Full circuit

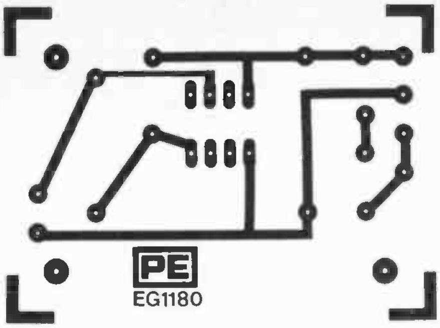


Fig. 3. P.c.b. design

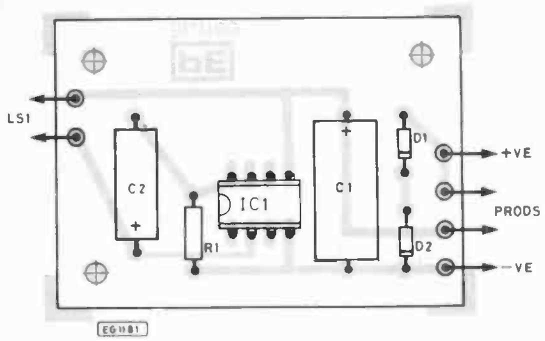
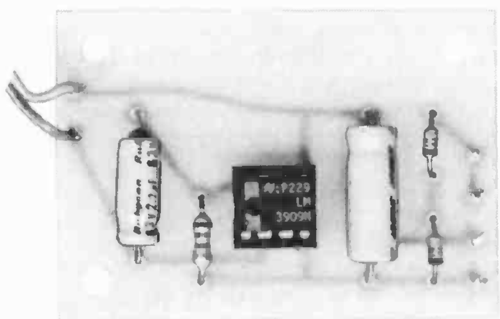


Fig. 4. Component layout



COMPONENTS . . .

Resistor

R1 1k $\frac{1}{4}$W 5% carbon

Capacitors

C1 33µ 16V axial elect
C2 2µ2 63V axial elect

Semiconductors

D1,D2 1N4148 (2 off)
IC1 LM3909N

Miscellaneous

LS1 64 ohm impedance miniature loudspeaker
Test prods
Printed circuit board
Three solar cells type MS4A or solar panel (Maplin)
Wire, solder, etc.

the switch until the control voltage goes above the switch-off threshold voltage. C2 then starts to charge via LS1 and R1 again, and continuous oscillation is produced.

D1 and D2 are used to limit the supply voltage to no more than about 1·4 volts. This is essential since the circuit will cease to operate if the supply voltage goes substantially above this figure.

CONSTRUCTION

Details of the Continuity Tester printed circuit board are given in Fig. 3, and construction of the unit is perfectly straightforward (Fig. 4). The unit will work using an 8 ohm impedance loudspeaker for LS1, but this would increase the current consumption of the circuit and it is better to use a component having an impedance of 40 ohms or more.

In direct sunlight two small solar cells are sufficient to power the circuit, but three cells in series or a solar panel would be a more realistic power source.

The maximum voltage across the test prods is only about 1·4 volts and the maximum current flow between them is only about four milliamps or so. Both figures are sufficiently low to give no real risk of damaging delicate components when using the unit. ★

TRANSISTOR CHECKER

SOLAR POWER has an obvious appeal for items of equipment that will receive only brief and intermittent use, and where the use of ordinary batteries would result in them running flat largely due to ageing rather than use. Solar cells are more expensive initially, but will go on operating year after year and have a certain novelty appeal as well.

A Transistor Checker is a good example of a piece of equipment in the category mentioned above. It is not a piece of test gear that is likely to be used every day, but on occasions a transistor checker of some kind is an essential piece of equipment. This simple design is a go/no go checker which can be used to test low, high, or medium gain devices, and an l.e.d. indicator light flashes on and off if the test device is serviceable. If the l.e.d. lights continuously the device under test has gone closed circuit, and if the l.e.d. fails to light the test device is open circuit.

The circuit requires a supply potential of 2 volts at a current of a few milliamps, and it could therefore be run from four MS4A or similar solar cells under bright conditions. However, a 6 or 9 volt solar panel would permit operation under lower light levels and would be less expensive.

THE CIRCUIT

Fig. 1 shows the circuit diagram of the Transistor Checker. The circuit is little more than an oscillator which pulses the base of the transistor under investigation with a small current, plus an l.e.d. indicator connected in the collector circuit of the transistor so that it lights up when the device is pulsed into conduction. The oscillator is based on an ICM7555 (IC1) and this has a couple of advantages over the standard 555 device in this application. One is simply that it requires a much lower supply current and will operate at a supply current of only about 50 to 100 microamps rather than the 5 to 10 milliamps required by the standard 555. Of greater importance though, the ICM7555 will operate from a supply potential of only about 2 volts which compares with

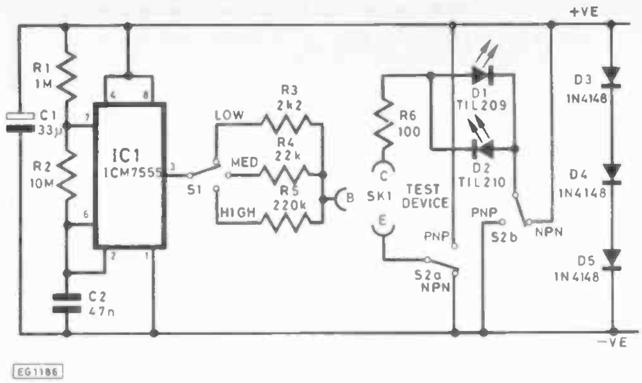
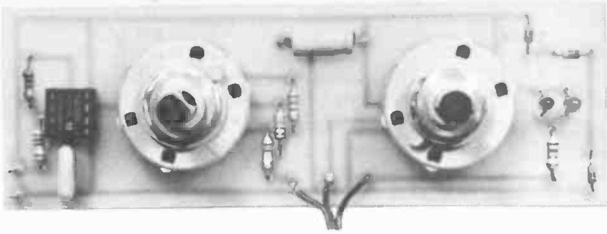


Fig. 1. Circuit diagram



a minimum figure of about 5 volts for the 555.

IC1 is used in the standard 555 astable configuration, and timing resistors R1 and R2 have been given fairly high values in order to keep the supply current drawn by this part of the circuit down to a reasonable level. Timing capacitor C2 has a value which gives an operating frequency of nearly 2 hertz. R2 has been made fairly high in value when compared to R1 so that an almost squarewave signal is produced at the output of IC1. This signal has a peak to peak value that is virtually equal to the supply voltage, and it therefore switches the test device fully on and fully off so that unreliable and ambiguous results are avoided.

The output of IC1 is connected to the base of the device under test via whichever of the three resistors (R3 to R5) is selected using S1. With R3 in circuit the test device is fed with a base current of about 0·6 milliamps or so, and a current gain of only about 5 times or more through the test transistor is sufficient to give a collector current of a few milliamps and cause the l.e.d. indicator to light up.

With R4 switched into circuit the base current is reduced by a factor of ten, and the device under test then requires a current gain of about 50 or more in order to operate the l.e.d. indicator. With R5 switched into circuit the base current is reduced by a further factor of ten, and a current gain of about 500 times or more through the test device is needed in order to operate the indicator l.e.d. This gives only a very rough assessment of the current gain provided by the device being checked, but it does avoid the situation which can occur with some simple checkers where only a single base current is used, and a high gain device seems to be fully operational, whereas it actually has a very low level of current gain.

S2 is the npn/pnp mode switch, and one pole of this connects the emitter terminal of test socket SK1 to either the positive supply rail or the negative one, as appropriate. The other pole of S2 provides complementary switching in the collector circuit of the test device. In order to enable simple npn/pnp switching to be used, two l.e.d. indicators are incorporated in the circuit. D2 is connected with the correct polarity when the unit is used in the npn mode while D1 becomes operational in the pnp mode. These l.e.d.s are different colours so that they indicate the mode in use and help to prevent the unit from being used with the mode switch

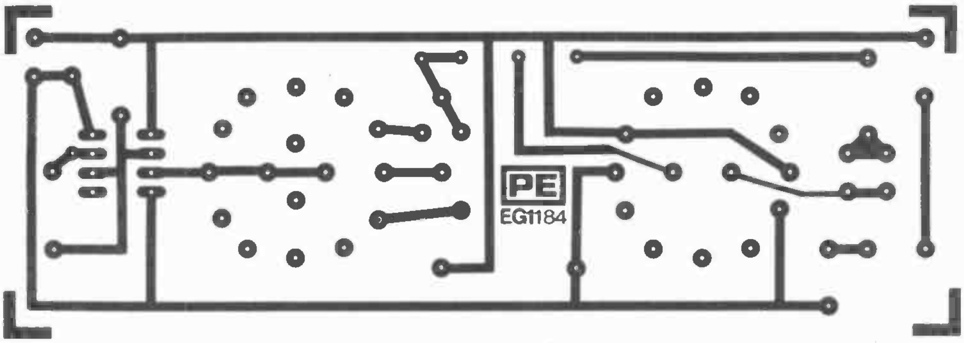


Fig. 2. P.c.b. design

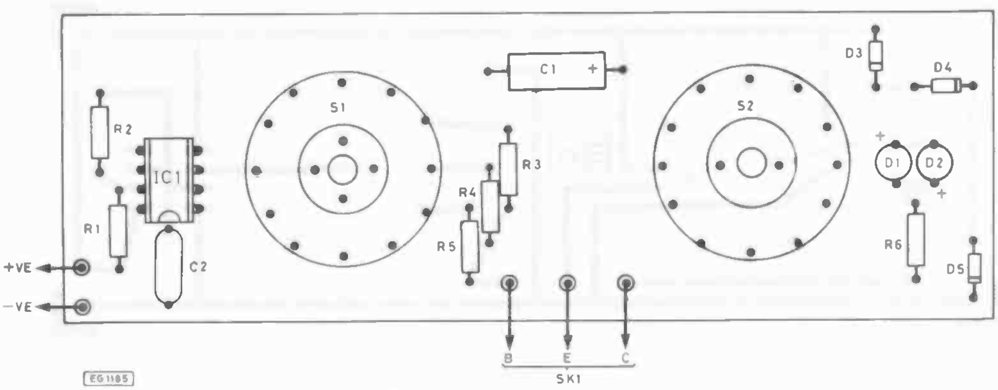


Fig. 3. Component layout

inadvertently left in the wrong position. R6 is simply a current limiting resistor.

D3 to D5 are used to stabilise the supply voltage at about 2 volts so that a reasonably consistent base current is produced by the unit, even if a solar panel (which would otherwise give a very unstable supply voltage) is used as the power source.

CONSTRUCTION

The printed circuit board for the Transistor Checker is shown in Fig. 2. This takes all the components apart from the solar cells and test socket SK1. The latter is a three way DIN type and most transistors can be plugged direct into one of these. A set of crocodile clip test leads must be made up so that other types can be connected to the unit.

If the two rotary switches used for S1 and S2 have printed circuit tags, they will fit onto the board without difficulty, but most component suppliers sell the type which has ordinary tags. It is possible to use this type of switch, but the ends of the tags must be cut off to leave what are effectively printed circuit pins, but do not remove any more of the tags than is absolutely essential. Push the switches right down onto the board before soldering them in place. The printed circuit board is mounted securely in the case when S1 and S2 are fitted onto the front panel, and no additional mounting of any kind is required.

The finished unit is very easy to use, but always make quite sure that S1 is set to a suitable position for the device being checked, and that S2 is set to the correct mode. Also make sure that the device under test is connected properly if D1 or D2 fail to flash on and off and the device appears to be faulty.

A simple way to check that the supply voltage is adequate is to simply place a short circuit across the emitter and collector terminals of SK1. D1 or D2 (depending on the setting of S2) should light up if the supply voltage is adequate. ★

COMPONENTS . . .

Resistors

R1	1M
R2	10M
R3	2k2
R4	22k
R5	220k
R6	100

All resistors ¼W 5% carbon

Capacitors

C1	33µ 16V axial elect
C2	47n polyester

Semiconductors

IC1	ICM7555
D1	TIL209 3mm red l.e.d.
D2	TIL210 3mm green l.e.d.
D3, D4, D5	1N4148 (3 off)

Miscellaneous

S1	3 way 4 pole rotary switch
S2	6 way 2 pole rotary switch with adjustable end-stop
SK1	3 way DIN socket
	Printed circuit board
	Control knobs
	Solar panel (Maplin)
	Wire, solder, etc.

Space Watch...

SHUTTLE 6 RE-ENTRY

The precisely guided re-entry of Challenger-6 into touchdown at the Edwards Air Force Base, California, at precisely 10.53 am, was a triumph for the team of Astronauts. They were Paul J. Weitz, USAF Col. Karol J. Bodko, Donald H. Peterson and Dr. Story Musgrave. This flight has increased the confidence in the procedures for the next Shuttle at Kennedy Space Centre, Florida.

Hypersonic and Supersonic manoeuvres carried out by the Shuttle were entirely satisfactory. They were carried out on re-entry before touchdown at Edwards Field. Confidence in the procedures for re-entry in the way of Lateral control, Stability and Reaction control were satisfactory, and so were the manoeuvres designed to check system capability and Rudder Authority.

There were three main questions to be answered about flight characteristics. These were designed to involve some thirty firings of jet-energy during descent. They were commanded instructions but were monitored by the astronauts for safety. The three hypersonic S-turns were made as is usual with re-entry. However, this time there were eight other sets of instructions to be accomplished.

The re-entry was made first at an angle of 40° as usual. The initial flight testing was made at 24,000 ft/s at an altitude of 261,000 ft. The test involved an aileron pulse followed by right-hand jet input as well as right-hand yaw jet pulse input. The crew then fired the orbital system engines for the vehicle to leave its orbit and commence its descent south of the Mauritius Islands of the Indian Ocean. The spacecraft then had a 27 second burn which brought it to 292,000 ft/s and a height of 400,000 ft, an interface required to bring it 4043 miles to Edwards Field. When the spacecraft reached a speed of 230,000 ft/s and sensed it was at 0·76 g. the first command to roll 80–85° was made. It was held at this speed until it had reached the crossrange of 377 n. miles from touchdown. At this point the attitude was corrected and Challenger's nose was pointed in Azimuth 10° to the north of the landing site.

The next test was made at 240,000 ft, and when the speed was 23,000 ft/s. This test involved yaw thrusters and was designed to check the behaviour of the ailerons and other surfaces which experience very thin air when reaching thin atmosphere. Another test was made at a height of 205,000 ft and at speeds of 18 and 15·6 mach to check the effectiveness of the ailerons and their resistance to the pressure put on them at this time. Aileron stability is very necessary when carrying heavy loads such as will be encountered with Space-lab. This successful trip surely means that the re-usable vehicle is here to stay.

Many photographs were taken during this trip and some of these will be described, they are important. One of these pictures showed the astronauts climbing around the shuttle, and it was clear that they were making rather heavy weather of it. They did have some training in a water tank but it seems that this had not been sufficient. This may of course be lack of training, but this seems a little unusual. If this part of the de-briefing is released there might be some better understanding. There seems to have been trouble with the tethering lines. These did not work according to plan, though they had appeared satisfactory in the water tank. It is a little difficult for those on Earth to realise that as far as the astronauts are concerned they are free to move in any direction, it is not just a matter of up and down and side to side. It has already been decided that in the next trip a non-tethered extra-vehicular exercise would take place.

One of the pictures also showed the Earth and its clouds against the background of Space while the astronauts were working in the payload bay. All the pictures were taken with a 35 mm camera attached to the spacesuit. Another thing was noticed by the monitoring devices: the heartbeat of Musgrave was still at 60 beats per minute whilst Peterson's had jumped to between 130 and 140; readers will remember that this happened with a previous crew. Challenger-6 was at that time in darkness and all lights were on as the 35 ft long Tracking and Data Relay satellite was raised to 59°. After the satellite had been launched the upper stage could be seen attached and inert to the disappointment of all concerned. At the moment it is not yet decided what its future fate might be.

THE RED SHIFT AS A MEASURE

At last there seems to be a real attack on the question of the Red Shift. It has been more than a decade since Chris Arp of the California Institute of Technology was displaying photographs and models of objects which have thrown doubt on the idea that Doppler shift and Red shift are always the same. Several teams have sought to refute his views and even suggested that the connecting filaments which he saw were a figment of his imagination. It so happens that Jack Sulentic of the University of Alabama has recently confirmed Chris Arp's and his team's results. This was done using some hitherto unpublished photographic plates of the galaxy NGC 4319 and the object Markarion 205. When it is confirmed it will show that at least part of the Red shift in the light from astronomical objects is not produced simply by their receding from us in the expanding Universe.

Arguments have been made before about the Red shift with regard to some very important bodies and not all astronomers demand that the Doppler effect of sound is exactly the same as Red shift. That it applies to ordinary galaxies is true—this can easily be checked by measuring the speed in different ways simultaneously or by using different methods and comparing measurements. However, there have been protagonists on both sides. It is therefore now becoming more and more important that some solution be found. As time passes, new discoveries are made and more sophisticated techniques devised so it is now imperative that what we believe to be true, is proved to be true. It is significant that recently a small group of people who were interested in this subject because very long baseline interferometry (VLBI) had revealed 'faster than light' speeds in Quasars. VLBI had shown that the quasar 3C279 showed an expansion rate which, when converted by the Hubble law, gave a figure 10 times the speed of light. The astronomers at Jodrell Bank, a small group set up to look into this matter and to provide at least some ideas about the future procedure, set out to discuss it.

There are now seven known radio sources that show these superluminal characteristics. These range up to at least 10 times the speed of light in their motions. These are 3C120, BL Lac, 3C273, 3C279, 3C345, 3C179 and NRAO 140. These were revealed because of the increased technique reliability. This was due to the many VLBI arrays and the routine production of milli-arc-second-scale maps. Some indirect measurements show that the variable velocities in some cases may be due to several components. The theoreticians do not believe the results, they do not believe that real faster-than-light motions exist. This breaks Einstein's light speed limit, therefore it must be an illusion. It is true that initially it had been admitted that, seen from a certain angle, it appeared that the law was violated; indeed the law itself was disputed. This was a very serious discussion and the matter was thrashed out thoroughly. No answers were found, though many suggestions were made.

The conclusion was that during the past 12 years more questions had been raised than had been answered. What now then, stalemate? Surely not. Are mathematics confounded or has something been missed? Are matters, then, to be left to others more adventurous? If one reporter is to be believed, the matter is to be left there and hope that during the next 12 years some solution will emerge. Is it then a return to the past, must Einstein be preserved right or wrong? Who mentioned Darwin . . ?

TAILPIECE

It is rare for this column to be concerned with such mundane matters as insurance, yet this is the second time that it has arisen, since it directly involves the recent failure of the Tracking and Data Relay satellite which failed to be sent to its planned orbit. There has been some criticism lately about insuring against this sort of thing. It seems that the constant failure of Ariane has already led to some rethinking in London and New York. The average cost of a rocket is high and the composite of satellite and launch runs on average at three-quarters of a million pounds. The normal premium now seems to be about 10%, but only about 5% for a shuttle launch. It is easy to see that those looking for the biggest profit will prefer the shuttle.

Frank W. Hyde

ROBOT VISION

GEOFF MORTIMER
& LIZ NEWBURY

BEFORE we can start discussing any particular aspect of robotics it is only sensible to ask the question, 'What exactly is a robot?' The word was coined in 1921 by Czech playwright Karel Capek and is derived from a Czech word meaning 'worker'. Capek's play, entitled 'RUR' (Rossum's Universal Robots), tells how a brilliant scientist named Rossum manufactures an army of mechanical 'robot' slaves to free mankind from the drudgery of work. However, after an irresponsible scientist in Rossum's laboratory gives the robots feelings, they grow to resent their lot and rebel against their creators, finally annihilating the human race.

Clearly Rossum's robots were far more sophisticated compared with those that current technology is capable of producing. The modern industrial robot is a cumbersome beast by comparison, needing many thousands of instructions to perform even a simple task, and certainly lacking both initiative and ability to oil its own springs. So what distinguishes a robot from just another piece of computer-controlled machinery? There are those who would say there is no difference, in Japan for example, any NC (numerically controlled) machine is considered for statistical purposes to be a robot. Since this is obviously not a very useful definition, we must draw a line somewhere.

Consider the difference between a digital alarm clock chip and a microprocessor. The former will undoubtedly be programmable (since the alarm would be of little use if the manufacturer had pre-set it to say, 7a.m!) but even the most ingenious electronics engineer would have difficulty adapting that chip to control his washing machine. Although a microprocessor can easily be programmed to perform the same function as the digital alarm clock chip, everyone knows that this is by no means the limit of its capabilities.

We can usefully think of the robot then, as the 'microprocessor' of the machinery world. As with the micro, the robot's hallmark is versatility, so there is no need for its designer to try and foresee its every possible use. A robot arm for instance, given an adequate reach, speed and lift capability, should be able to turn its hand (or gripper perhaps) to anything.

WHY SENSORS?

Imagine a human brain completely divorced from its senses, unable to touch, hear, smell or see anything of its surroundings, and unaware of the positions of the limbs in its body. It is most unlikely that the brain would develop at all under these circumstances, and it is arguable that intelligence as we understand it depends entirely on the brain's ability to acquire sensory information. A computer without sensors would likewise be unprogrammable, since it would be impossible to input any code.

A robot cannot be 'intelligent' if it cannot directly acquire information about itself or its surroundings. Thus when you give a robot the ability to 'perceive' and so acquire information, you reap the immediate benefits of an artificial intelligence. These benefits are considerable: Firstly, programming can be simplified, and carried out at a higher level, and be more readily understood by the user. Secondly, the machine is able to learn about its environment during operation; and thirdly, obstacles can be avoided automatically without the need for specific programmed commands.

If a visual perception system is implemented, a robot can distinguish patterns and objects, and then act on the information. In manufacturing, for instance, it can identify and automatically reject broken or damaged parts on a production line. Another example might be a robot which picks up chocolates and automatically deposits them in the correct compartments of a box. Besides performing regular activities like these a seeing robot may intervene in abnormal situations, such as tools accidentally being dropped on to a conveyor belt, where the outcome is potentially dangerous or costly. Evidently, sensors in general and visual ones in particular are going to play a very important role in the advancement of robotics engineering.

HOW CAN ROBOTS SEE?

In human beings the seeing process is essentially a dual one: Visual information is acquired by the eye, then processed or 'understood' by the brain. Neither the eye nor the brain can 'see' on its own—both are necessary if the visual perception system is to function. So in order for a robot to see, it must be equipped with mechanisms for acquiring and for processing images. In the area of vision, as in many fields of robotics, engineers have attempted to simulate human systems as far as possible. Visual data is normally acquired by some form of camera which transmits the visual signal to a computer for processing. Camera technology is generally agreed to be adequate for most current requirements but, as has been the case in other fields, the computer technology itself is still lagging behind.

Ideally a computer should 'understand' an image by describing it in terms similar to those a human being might employ, then use the 'knowledge' so gained in future problem-solving situations. The way to achieving this lies in the development of more powerful computers, and more importantly, the improvement of software techniques. In many industrial situations, potential robot applications have needed some form of visual feedback, and recent developments have provided solutions to a number of such problems. It is also true that many situations exist which do not demand an ideal vision system, and with which current technology can cope quite adequately. Let us now consider some of the techniques in use today.

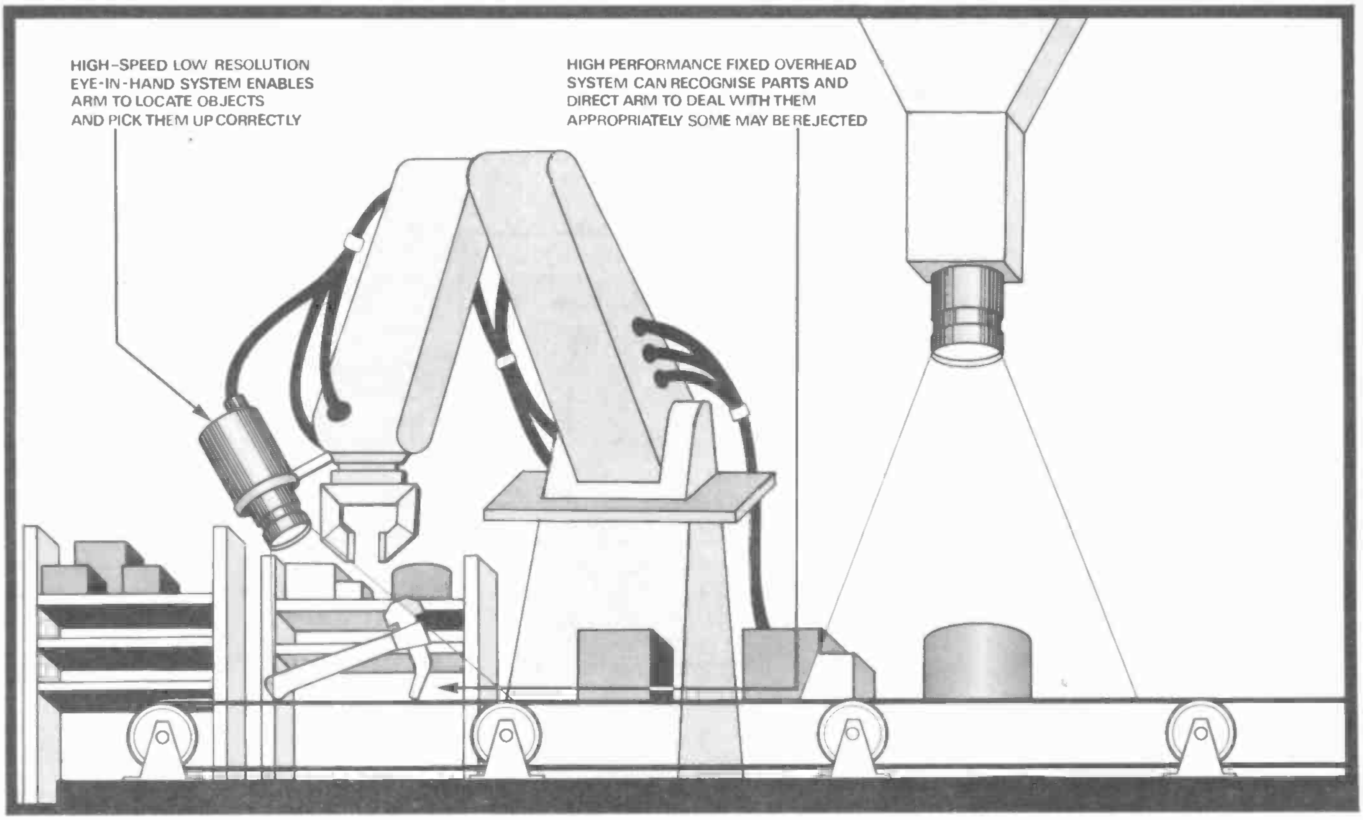
VISION SENSORS

The simplest form of optical sensor is the photo-electric cell, the original 'electric eye'. A single photo-cell, however, is able to convey only one piece of information at a time. A robot (or computer) vision system usually requires a large amount of picture information to be supplied relatively quickly, and the solution lies in the use of some form of camera. Until quite recently the best sensor available was the TV camera tube, unfortunately rather a fragile device. Now, however, solid state 'retinas' employing charge coupled device (CCD) technology have been developed. These units are far more robust than their glass counterparts, so are more suitable for use in industrial environments. They also have the advantage that they are much easier to interface to computers.

VISION BASICS

Although computer vision systems may vary considerably in sophistication, a number of techniques are common to all of them. Before an image from a camera can be usefully processed, it has to be converted to a form which can be understood by the computer. This conversion process, known as digitisation, involves the division of the image into a grid of squares (or pixels), each of which is then stored in memory as a number (or pixel value). In a 'grey-scale' system the pixel value is called the grey-level, and is proportional to the brightness of that portion of the image represented by the pixel. In binary systems, the pixel value is either 1 or 0, corresponding to a brightness greater or less than a predetermined threshold, the stored image being basically a silhouette.

The resolution of a system is a measure of the number of pixels into which the image is digitised. Thus the higher the resolution, the more precise and detailed the stored image. However, if a very large amount of information is stored, the computing power required to process it becomes prohibitively large: a 256 x 256 pixel image contains 65536 pixels, a number equal to the total addressable memory capacity of most of today's microcomputers! A technique known as run-length encoding is often used to overcome the space problem, in which a string of numbers called a run code is set up, instead of storing every pixel. Each number corresponds to a number of adjacent pixels with the same value, together with the value itself. This allows a considerable reduction of the memory required, especially when



A typical example of the use of visual feedback: A two vision system enabling a robot arm to pick up different objects from a conveyor belt and place them in appropriate containers.

high resolution binary images are being processed. Let us look in detail at two vision systems representative of existing techniques.

HIGH RESOLUTION GREY-SCALE SYSTEMS

The most sophisticated vision systems in use today attempt to extract and process the maximum possible information from an image. The resolution of such a system is typically 100,000 or more pixels, and perhaps 256 or more grey levels are distinguished.

Comprehensive signal processing and feature extraction algorithms are used to determine the shape, size, position and orientation of an object (or a number of objects) in view. Powerful mainframe or mini-computers are used in the processing of the image, often needing several processors to achieve sufficient computing power. By storing information about an object such as the relative positions of features like corners and holes, complex networks of tubes and pipes or contoured metal castings can be consistently recognised. Powerful contrast enhancement techniques enable information invisible to the human eye, such as hairline cracks in printed circuit board tracks, to be detected.

Using systems such as these in conjunction with robots it is possible to automate processes in which the type and orientation of parts to be manipulated is outside the control of the programmer. Here the robot uses its 'eye' to direct it in its task. However, even high-resolution systems have their limitations. Three-dimensional and mobile vision technology is still in its infancy, and it is not normally possible to compensate for the effects of variable lighting conditions. The high level of performance indicated above is generally attainable only in clear environments, using a fixed camera position and carefully controlled lighting. The advantages of high resolution systems lie in their increased information—handling capacity. These are offset though, by drawbacks such as considerable bulk, slow operation and high cost (typically over £20,000).

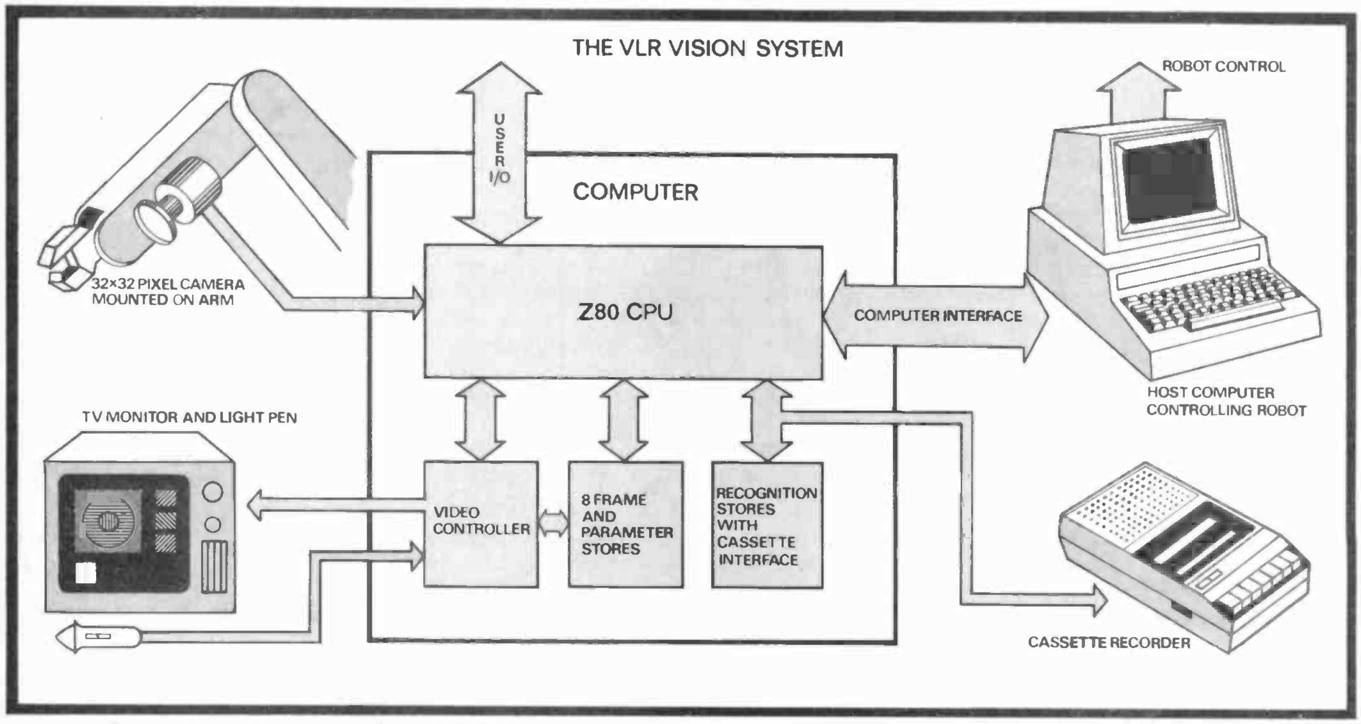
LOW RESOLUTION BINARY SYSTEMS

An alternative approach is gaining favour in some areas of robotics applications. This minimises processing overheads, cost and complexity by using very low resolution (VLR) binary (i.e. silhouette) vision systems. These use typically only one or two thousand pixels of digitisation, and a limited number of feature extraction functions. They are able to process visual information at speeds comparable to that at which an efficient robot arm might move. In other words, direct real-time visual feedback loops can be established. The recognition-ability of such systems is usually limited to a small set of criteria. These might include area, perimeter, the number of 'holes' in an image, and so on. Nonetheless, since the camera is compact enough to be mounted on the end of the robot arm itself, areas of interest can be magnified simply by moving it nearer to the object. Calculating the position of the centre of gravity, provides a basis for location and orientation algorithms which are often fast and precise enough for the arm to follow a moving object. Unimation Ltd recently demonstrated this ability using a PUMA robot arm fitted with a 32 x 32 pixel camera. The robot followed a plastic toy building brick as it was moved across a surface, picking it up correctly when it remained stationary for longer than about four seconds.

VLR systems are of greatest use in situations where the identity of an object has been pre-determined, and where high-speed operation is important. Because VLR systems are simple and relatively inexpensive (typically under £1,000), they are popular among hobbyists and educational establishments. Though less sophisticated than their high-resolution counterparts, they employ many of the same techniques.

THE COLVIS VLR VISION SYSTEM

An example of VLR technology is the COLVIS vision system, manufactured in the UK by Colne Robotics Co Ltd. This system employs a 32 x 32 pixel, binary solid-state camera using a dedicated Z80-based micro-



A typical configuration of the COLVIS high-speed system: Commands may be entered either with the light pen or via the user I/O channel. The host computer interrogates the system for visual information which it then uses to control the robot

computer. It can be used either on its own, or under the control of any micro or mini-computer fitted with an 8-bit bi-directional port. In stand-alone mode the system can perform simple vision-based control functions, and is programmed via a TV monitor and light pen. When under computer control, the system can be interrogated for either raw or processed vision data which is then transmitted back to the 'host' computer. In this way, a computer controlling a robot arm can be supplied with vision information on demand, and at no cost to its own processing time.

The system is supplied with software enabling it to determine the position, orientation and identity of objects in its field of view. The commands available to the user are in three groups:

(i) Data acquisition
(ii) Image processing (including feature extraction)
(iii) Learning/recognition

Eight picture stores are provided, and the camera image can be read into any one of these, one at a time. Each picture store has an associated area of memory in which any of the following parameters can be updated on command:

PARAMETER	FUNCTION
Centre of gravity:	**Position, orientation**
Direction of longest dia:	**Orientation**
Direction of shortest dia:	**Orientation**
Area:	**Recognition**
Perimeter:	**Recognition**
Number of holes:	**Recognition**
Perimeter^2/Area (compactness):	**Recognition**
Longest diameter:	**Recognition**
Shortest diameter:	**Recognition**

Measures are taken to ensure that the system always operates at its fastest possible speed. A comprehensive range of learning functions has been implemented, enabling the system to be taught to identify objects on the basis of some or all of the recognition parameters listed above. A 'Learn' command is given, together with a name for the object to be learnt. The system then calculates, and records the required recognition parameters in a data structure which incorporates a set of tolerances associated with each parameter. These tolerances are automatically initialised to a useful set of values, but for each learnt object the user can adjust them individually, in both the positive and negative axis. Learnt objects can be deleted or re-learnt; they can be saved on cassette tape or loaded from it. When the 'Recognise' command is given, the list of learnt objects is scanned, and those parameters in use are compared with ones calculated from the camera image. If the new parameters all fall within the specified tolerance for a learnt object, the system notifies the user (or host computer) that it has recognised that particular object. Up to 64 different kind of objects can be learnt at any one time. In normal use an operator would teach the system a new object, adjusting tolerances and changing the criteria (i.e. parameters used) for recognition, until optimum performance was achieved, before handing back control to the host computer.

Additional commands enable the system to pre-process picture information before parameters are calculated. These include picture inversion, exposure control, choice of light or dark background and several noise-reducing functions which strip or fill-in isolated pixels. A macro construction facility enables strings of commands to be stored in memory and executed as single instructions. The contents of any two frame stores may be displayed simultaneously on the

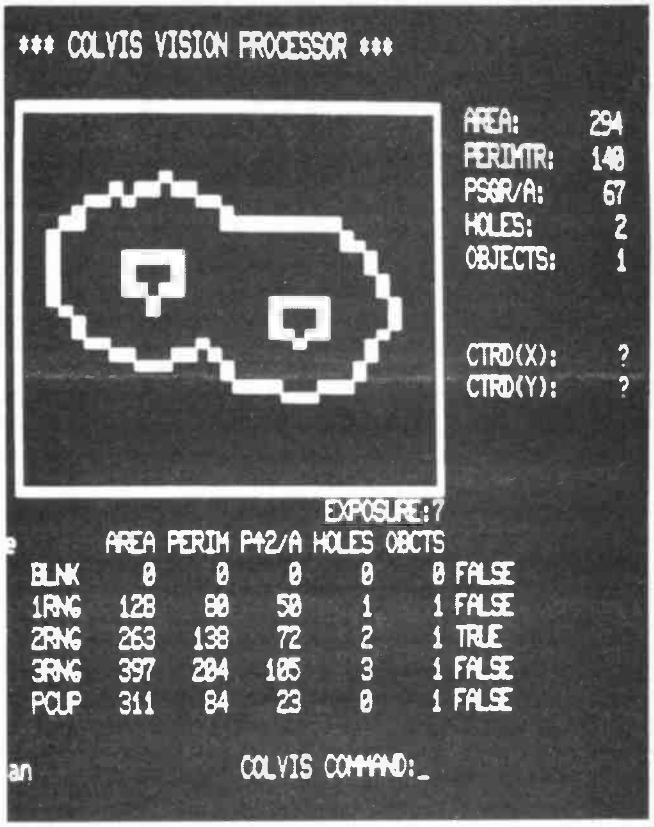


Fig. 1. VDU showing object identification

monitor screen, together with their associated parameter lists. When under computer control, all parameter, learning and frame store information can be transmitted on request to the master system.

In Fig. 1, the VDU shows an object (coded BLNK) which the system has learnt and identified: In the top right of the screen the parameter requirements are shown and are represented by the picture in the square. The list of parameters closest to those learnt, is shown in the lower part of the display, and has been identified as TRUE; the other possibilities being rejected as FALSE.

The COLVIS system is simple to use and fast-operating, making it ideal for educational purposes, though undoubtedly it will find its way into a number of industrial situations as well. An important aspect, particularly for educational establishments, is the low cost of this system; around £400.

LOOKING AT THE FUTURE

There is considerable scope at present for improving visual perception techniques. The vision system of the future will be able to process picture information far more efficiently than its relatively primitive predecessors, using extremely sophisticated high-level programming languages developed solely for such a purpose. We can expect computers themselves to be hundreds, perhaps thousands of times faster and more powerful. If technology within this field continues to advance at its present rate, some seemingly far-fetched predictions will rapidly become probabilities rather than remote fantasies. We can foresee vision systems installed overlooking large and complicated scenes—factory floors or perhaps crowded city centres. There, they will survey the area for abnormal events, capable of detecting fires, accidents and maybe even crimes! We must remain alert to the value and importance of robot vision, a field whose enormous potential is still to be explored and exploited. ★

VERNON TRENT *at Large!*

V.T.'s views and opinions are entirely his own and not necessarily those of PE

You must have heard of the House of Floggit, to my mind one of the most interesting department stores in South London. Family-owned, it first opened its doors towards the end of the 19th century and, until recently, remained an undying echo of the Victorian era of retail trading when the customer was king.

Floggit's merchandise was, and still is, of superb quality. Its standards of service impeccable. The lady assistants wore modest frocks that suppressed any gender-indicating undulations. The gentlemen were dressed in formal suits, the jackets of which were never discarded, even on the most sweltering day. And such frivolities as the use of forenames and remarks of a jokey nature were OUT.

Accounting and stock control systems were equally traditional. Cash was handled with genteel disdain. The customer's payment—he wasn't up to much if he didn't have an account—would be placed in a kind of torpedo tube and shot off to the counting house by an overhead railway. If change was involved, it would be returned by the same means. All this gave the impression that so far as the management was concerned, the handing over of the money was no more than a slightly indecent incidental.

In those pre-VDU days a basement-based covey of brown-coated retainers, all with unnaturally-tapered index fingers, carried out a digital stock count at the end of each day, recording their findings in copperplate handwriting on a series of lists. The store was open six days a week and no matter how late the hour, no one was allowed to leave their post so long as there was a customer about.

This respectable, dependable and thoroughtly stuffy and unprogressive profile began to change after Arnold Floggit took over the helm a few months ago. He succeeded his uncle Horace, the former chairman, who died without notice from a fit of the vapours on discovering Miss Playful (Toys and Games) up to no good in the stockroom with Mr. Stiff (Hardware).

Arnold, a very much younger man than his predecessor, was well and truly into electronics and—having once been stuck with Kenneth Baker at a cocktail party—had developed a special interest in information technology. And he was therefore aghast at the archaic and non-technical way in which the outfit was being run. There had to be fundamental changes.

His first tycoonic ploy was to set up an in-depth survey. This is, of course, standard procedure for anyone who can spell Harvard and consists of hiring hordes of expensive young analysts who dash around asking irrelevant questions and getting equally irrelevant answers. This leads to the production of a report, sometimes bound in limp leather and always costing a fortune.

On the basis of the report which eventually landed on his desk, Arnold decided to sink an odd million or so quid in a computer-based system which would do away with that absurd overhead railway, pep up accounting and stock-control and provide a constant flow of management information.

One day a team of young experts wearing Imperial College ties arrived to set up the computer. The staff didn't take much notice at first. All they knew was that a load of layabouts were mucking about in the basement.

But the course of events was soon brought home to them when one day one of the layabouts marched into Perfumery and dumped an electronic cash register on the counter. Miss Sniff, the buyer, 30 years with the firm, ignored it completely to begin with and continued to have fun with her overhead railway. The next sinister happening was a summons from above for all senior buyers. It was there that Arnold unveiled his grand plan and then handed the group over to Mr. Teachem, the training officer, for an intensive course of instruction in the modern miracle which was to transform their lives.

It was a frightening contraption so far as the conservative senior staff was concerned. It had more buttons than a cardinal's cassock and a habit of bleeping and popping whenever anyone laid a finger on it.

That first training session is not a happy occasion to record. Miss Silk of Haberdashery announced her intention to seek early retirement. Miss Swish of Ladies Fashions went all hysterical and had to be sedated with a swig of mint tea from the canteen. Mr. Spark (Major Domestic Appliances) eased his feelings by giving the thing a sly kick.

One cannot blame any of those present for their attitude when you consider the circumstances. Here they were, loyal servants who had grown grey in service, brought up in a world of dignified and calm, if stick-in-the-mud, working methods, being asked to become user-friendly with something which, in their opinion, belonged to another planet.

Arnold Floggit had not done things by halves and had gone all-out for sophistication. The cash register—which was not a cash register at all, but a thing called a terminal—was a multi-function beast. It could record both cash and credit transactions, log the date and time of each sale, with the identity number of the assistant concerned, and provide accurate, highly-detailed and easily-accessible data on stock movements. "I bet," said Mr. Crepe (Footwear) with dry cynicism, "it would boil an egg if you asked it nicely."

The day that the new system came into active public service had, for the younger members of the staff, a touch of carnival. Weaned on digital watches, up-market calculators and even home computers, they found little difficulty in adapting themselves to the revolution. Indeed, some of them regarded the occasion as the start of an era of liberation from the outmoded and sometimes despotic Floggit regime. Hopes were expressed by a few, including fashion-conscious little Wendy Penn (Stationery), that they could soon start turning up for work in flashy tops instead of bust-flattening blouses. Young Tom Channel (Radio and TV) prophesied that soon he'd be wearing cords and bomber jacket.

The over-40s were not so happy. The complicated procedures needed a strong mental digestion. An ordinary cash transaction, for example, involved the pressing of some 15 buttons, all in the correct order without, alas, a comforting cancel facility for the correction of cock-ups. Credit sales were even more complex. Barclaycard and Access, popular and convenient as they are, brought fresh terrors, as did the handling of cheques. And when some clever dick decided he wanted a refund, the effect on the hard-pressed salesperson was frightful to behold.

It will come as no surprise to you that all this sophisticated technology had adverse repercussions on customer-relations. The chap who'd just popped in for a set of batteries for his tranny on the way to the betting shop instinctively resented having to stand for 15 minutes witnessing a dazzling display of terminal trickery instead of merely slapping his money on the counter and pushing off.

In those departments where the older generation presided long queues were the order of the day. There was much muttering of "things aren't like this at Comet". The carriage trade, accustomed for generations to sedate service, switched to Harrods where they could hope for service almost as efficient as that accorded to the Queen. Turnover dipped, morale sagged and the star called Floggit began to dim in the retail firmanent.

Arnold Floggit, dedicated technologist as he was, began to wonder whether or not he hadn't dropped one. A realistic fellow, he reasoned that by equipping his goose with a golden facility he may well have retarded her ability to lay golden eggs. And it was with a sigh of resignation and a fondly wave to his not inconsiderable investment that he did a swift turnabout. One could not help salute him.

Out went the computer and its attendant terminals. Back went the overhead railway and the brown-coated stock counters. All hopes of dress reform faded into the middle distance. The older generation had their happiness restored.

There is an obvious moral to this story. You will recall that in a previous issue of PE I enjoined the Church to adopt electronics techniques in the name of greater efficiency.

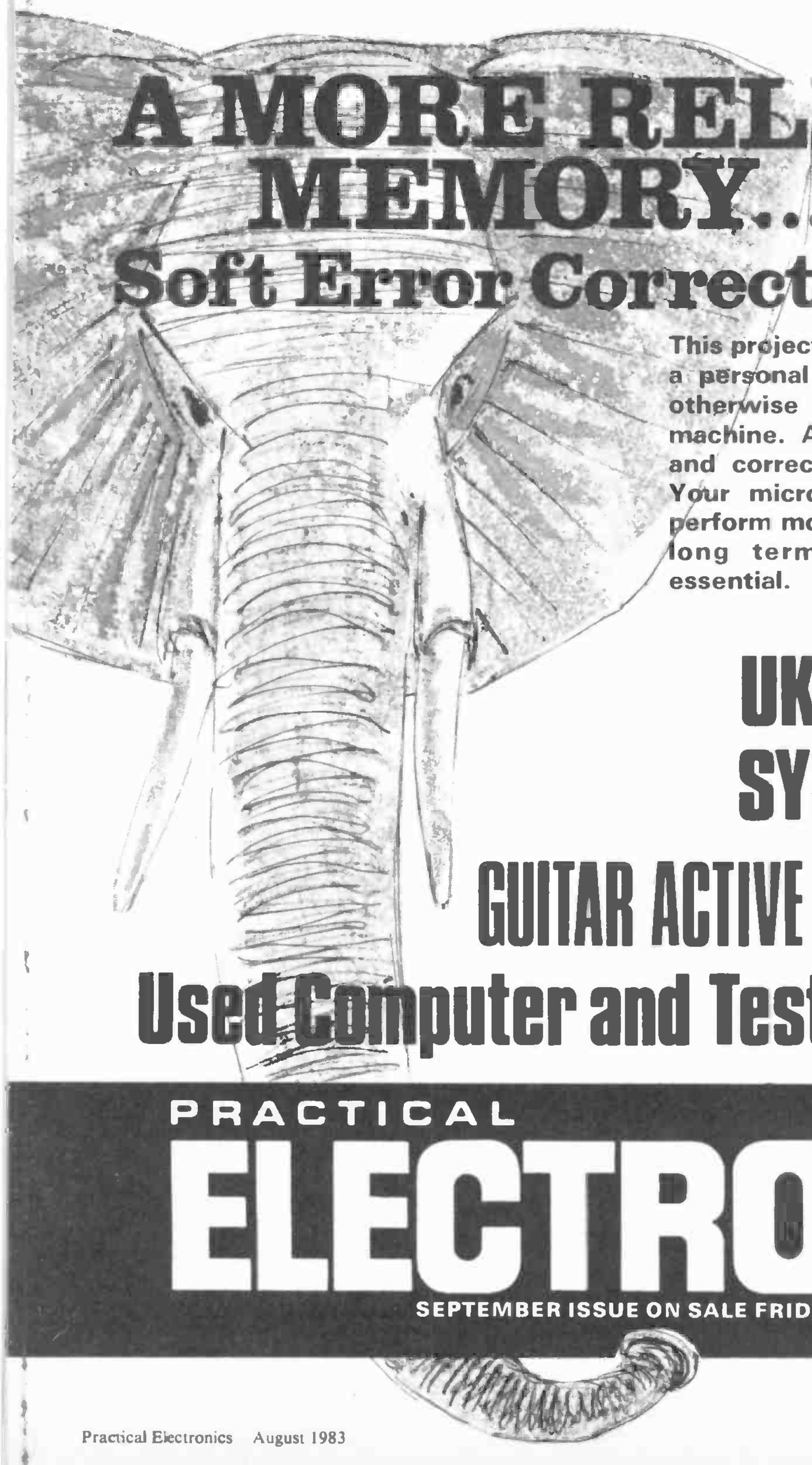
Perhaps at the same time I should have pondered on the problems of such retail houses as the House of Floggit and exhorted leaders like whiz-kid Arnold to pause before hurling themselves headlong into the electronics age.

Mind you, it's only a matter of time before Floggits, like other concerns, will have to succumb. In the meantime I shall take a middle-aged satisfaction in guessing at the mysteries of the formal frock, watching my money whizzing between counting house and counter by overhead railway and sympathising with youngsters in their heavy serge.

all in your

SEPTEMBER

issue!



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SEMICONDUCTOR CIRCUITS

TOM GASKELL B.A.(Hons)

VOLTAGE CONVERTER (ICL 7660)

MOST modern logic and microprocessor circuitry take power from a single supply rail; either +5V for TTL and microprocessor-based systems, or higher voltages for some CMOS circuitry. The incorporation of any other supply rails within such a system can be a considerable nuisance, adding complexity, size, and cost to the final project. A frequent requirement is for a low current negative supply, used to provide power to a small amount of analogue circuitry within the logic system. Digital to analogue, and analogue to digital converters are examples of circuitry which sometimes requires this negative rail; likewise many op-amp circuits, and certain memory i.c.s. (especially dynamic RAMs). In all cases the power requirements are so small that it seems to be an 'overkill' to have to provide a complete negative supply system, whether derived from the mains supply or from extra batteries. The ICL 7660 is designed to help solve this problem. It is an 8 pin CMOS i.c. which converts a positive supply into a negative supply voltage. Hence, any nominal supply of +1·5V to +10V is converted to a negative supply of −1·5V to −10V, with sufficient drive current for most applications (typically up to 40mA for a +5V input).

BASIC CIRCUIT

Fig. 2 shows the circuit design principle on which the ICL 7660 is based. Under the control of an internal 10kHz oscillator and switch control logic, four MOS power switches are used to charge up, and transfer charge between, C1 and C2. These capacitors are external to the i.c., since they must be relatively large; 10 µF is typical. The sequence is as follows: S1 and S2 turn on, while S3 and S4 remain off. As a result, C1 is charged up to the positive supply voltage. Then, S1 and S2 turn off, while S3 and S4 turn on. The positive end of C1 is now taken from the positive supply down to 0V. The negative end of C1, which was previously at 0V, then becomes forced negative; for a positive supply of +5V, the negative end of C1 is taken to −5V. The charge on C1 transfers to C2, the reservoir capacitor, which then supplies current into the load. S3 and S4 turn off, S1 and S2 turn on, C1 charges up again, and the whole cycle repeats continuously.

USING THE CHIP

The pin-out of the ICL 7660 is shown in Fig. 1, complete with its specifications. There are several important points to note about the specifications, and about the way that the i.c. is used in practical circuits. The absolute maximum supply voltage is +10·5V, so do not try to use it with supplies of over 10V; 15V CMOS is definitely not on! As with most CMOS i.c.s, connecting any pin to voltages outside its supply rails will cause damage, so ensure that no external signals are applied to the i.c. before its own supply is turned on. An internal voltage regulator is provided to prevent latching up (and potential damage) when supply voltages higher than +3·5V are used. This can adversely affect low voltage performance, so for voltages below +3·5V connect pin 6 to 0 volts, disabling this regulator. However, when voltages of +3·5V or more are used, this pin *must* be left floating, i.e. unconnected.

Finally, for supplies of +6·5V or more, or use at high temperatures, a diode *must* be added in series with the output. Fig. 3 shows the basic voltage converter circuit, and D1 is the extra series diode if required. For the lowest forward voltage drop a germanium diode is the best choice; an OA47 is specified, but any similar diode will do. A 1N4148 or similar will work satisfactorily, but will drop slightly more voltage. Take care with the polarity of D1; the feed from pin 5 of the i.c. is a negative, not a positive one!

Because the negative supply is generated by the charging up and discharging of capacitors, it is far from being a perfect voltage source. As would be expected, the output voltage becomes less (i.e. nearer to 0V) as more current is drawn. In practice, the relationship between the output voltage and the current drawn is linear; the effect is the same as

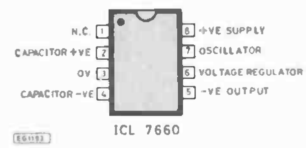


Fig. 1 Voltage converter integrated circuit pin-out with its specification below

Characteristic	Notes	Min. Value	Typically	Max. Value	Units
Supply voltage	All spec's measured at +5V supply	1·5	5	10·5	V
Quiescent current	No load on negative output		170	500	µA
Temperature range		−20		+70	°C
Power dissipation				300	mW
Oscillator frequency			10		kHz
Output resistance	20mA load current		55	100	Ω
Output resistance	Positive supply = 2V, 3mA load current		150	300	Ω
Output voltage (as percentage of positive supply)	No load on negative output	−97	−99·9		%
Output ripple, pk/pk	5mA load current		0·1		V
Output ripple, pk/pk	20mA load current		0·2		V

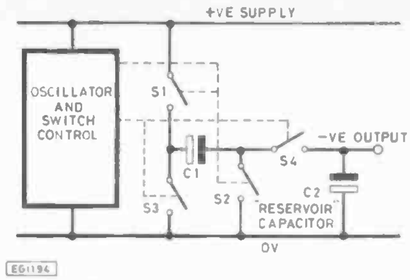


Fig. 2 Principle of i.c. operation

putting a resistor in series with a perfect voltage source. The value of this effective output resistance is dependent on the supply voltage, with 55 ohms being typical for a 5V supply, and 150 ohms for a 2V supply.

The graph of output voltage versus output current for a +5V supply is shown in Fig. 4. For most op-amps, A-D converters, D-A converters, etc., the current drawn is small, and the slight variations in negative supply voltage have no significant effect, but this characteristic of the i.c. should be borne in mind when designing appropriate circuitry.

Similarly, the relatively high level of ripple (typically up to a few hundred millivolts) should be noted, although again this should not normally cause any problems.

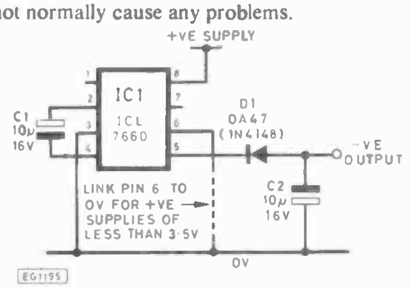


Fig. 3 Basic voltage converter circuit. D1 is not necessary for supplies >6.5V. Include it if high temperatures are anticipated

IMPROVING PERFORMANCE

Figs. 5, 6 and 7 show ways of improving the output characteristics of the ICL 7660. In Fig. 5 two devices are connected in parallel to give a lower effective output resistance to the negative supply. The reservoir capacitor C2 can be shared between the i.c.s. Any number of devices can be connected in parallel, the overall output resistance being the individual i.c. output resistance divided by the number of i.c.s used. For best performance, the output diodes, D1, D2, should be used at all voltages above 3·5V.

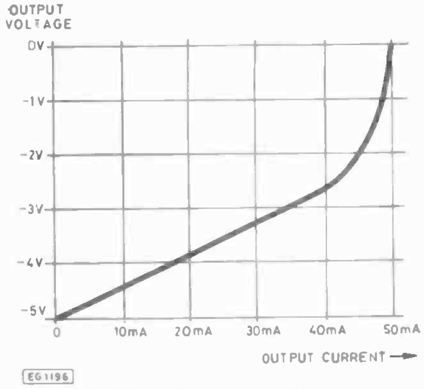


Fig. 4 Graph of output voltage versus output current for positive supply

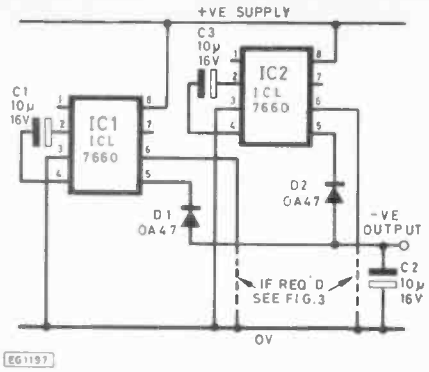


Fig. 5 Parallel connection if i.c.s

Fig. 6 shows a way of using the i.c. to provide a positive to positive voltage conversion! In this circuit the output voltage is twice the input voltage, less the two forward diode drops. This can provide up to approximately

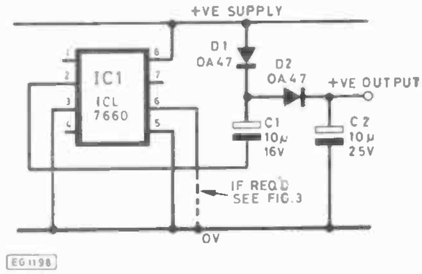


Fig. 6 Positive voltage converter circuit

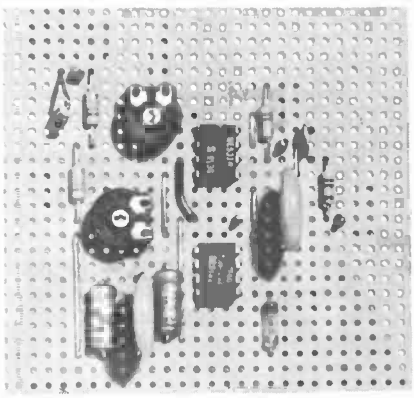
19V, since the voltage doubling is performed only by C1, C2, D1 and D2. The +10·5 voltage limit on the i.c. is not exceeded, since D2 prevents the high voltage ever feeding back into the i.c. Note that C2 can't be a 16V type for all supply voltages, so use a 25V type instead.

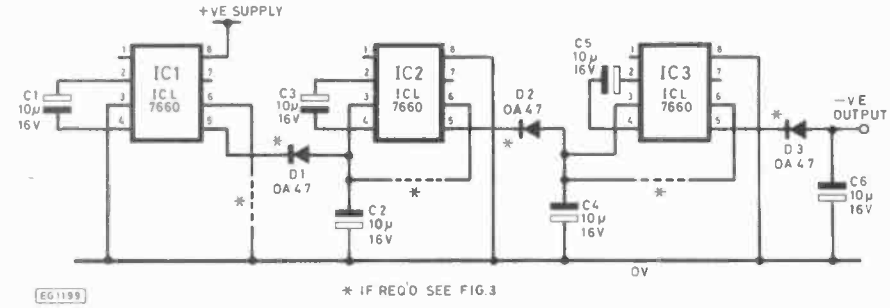
Fig. 7 shows three devices connected in series to provide a larger negative supply voltage. Up to ten i.c.s can be connected in this manner, within the limits of a maximum negative voltage of −10V. However, in this configuration, the output resistances *sum*.

EXTERNAL CLOCK

Finally, the oscillator frequency of the ICL 7660 can be changed, if required, by feeding an external clock into pin 7. When fed from CMOS logic, a 1k series resistor should be provided, while for TTL a 4k7 pull-up resistor to the positive supply is needed. If an external clock is to be used, note that the conversion frequency is *half* the applied clock frequency, due to an internal divide-by-two circuit. The internal oscillator can be lowered in frequency by adding a capacitor (typically 33 to 330pF) between pin 7 and the positive supply. If the frequency is lowered, C1 and C2 should be increased proportionally to maintain the performance.

Veroboard application of Fig. 8





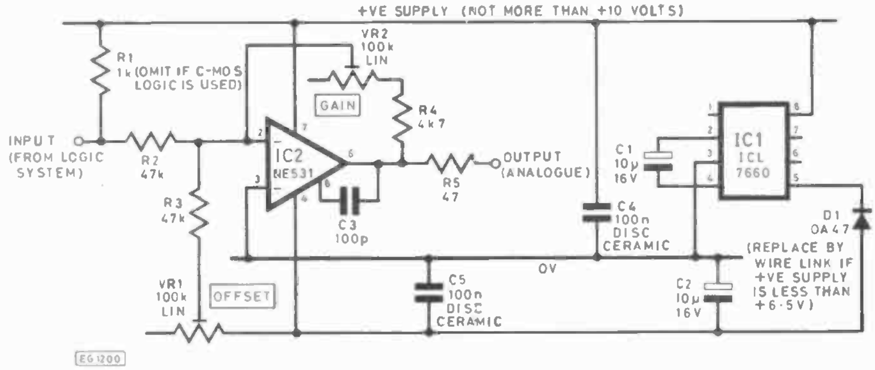


Fig. 8 Logic level to analogue converter circuit

APPLICATIONS CIRCUIT

Fig. 8 shows a simple application of this i.c. The circuit provides a logic system with a d.c. coupled analogue output, which is variable in level and symmetrical about 0V, rather than between 0V and the positive supply voltage. IC1 is the voltage converter used in a standard configuration to provide the negative supply to IC2, a high slew rate (i.e. high speed) op-amp. It is all powered from the logic system's own power rails, which are unlikely to be below 3·5V, so pin 6 of IC1 should be left open circuit. D1 can be replaced by a wire link for supplies of less than 6·5V. IC2 is used as an inverting amplifier, so precede this circuit with an inverting logic gate if polarity is important. The gain is variable between × 0·1 and × 2, and is adjusted via VR2. VR1 provides an offset control, which provides biassing from the negative supply to the inverting input of IC2. This ensures that the output can be corrected to be exactly symmetrical about 0V, although it does put a small amount of high frequency ripple on the output, of course. Typically, a few tens of millivolts.

An NE 531 op-amp has been used to provide a very fast edge on the square wave output, but if this is not critical it can be replaced by a 741. If this is done, omit C3, the compensation capacitor, as 741s have internal compensation. Finally, C4 and C5 are extra supply decoupling capacitors, and C1 and C2 can be 16V types or higher; 25V is quite acceptable.

This circuit is a fairly simple, but hopefully effective, demonstration of the way in which voltage conversion can provide a low power alternative supply rail in a larger system. Bear in mind the intrinsic limitations of the device, and it can prove to be an extremely useful circuit element. The ICL 7660 is readily available from a number of suppliers, such as **Technomatic, Maplin, and Watford Electronics.**

Note: in Semiconductor Circuits (June 1983): In Fig. 1 pin 8 should be positive supply.

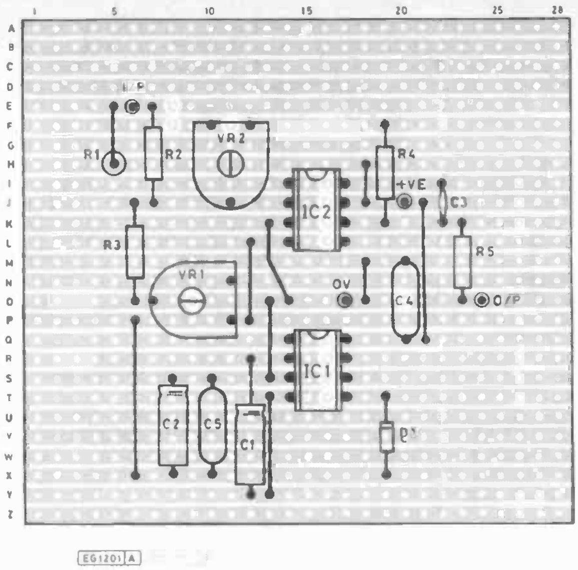


Fig. 9 Logic system with a d.c. coupled analogue output. Omit R1 if input is CMOS logic

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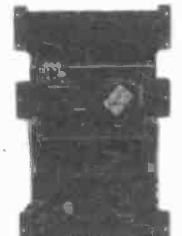

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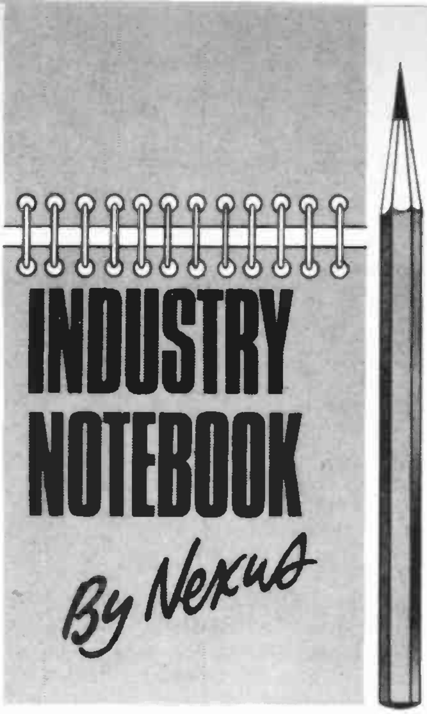


Go-Ahead

The recommendations of the Alvey Committee that some £300 million should be invested in a cooperative research programme on advanced information technology have been endorsed by the Government. The taxpayers' contribution via the Department of Education and Science, the Ministry of Defence and the Department of Industry will cover half the cost with the remainder coming from industry. Hard-cash involvement by industry should ensure that research will be down-to-earth with marketable end-products both in software and hardware.

The Department of Industry will run the programme through a five-member directorate under Brian Oakley, seconded from his post as head of the Science and Engineering Research Council, and the directorate will report to a supervisory board of industrialists headed by Sir Robert Telford who is chairman of Marconi.

The Cabling of Britain programme has also got the go-ahead with the publication of the Government White Paper. It will be recalled that when first mooted the idea was universally applauded. Since that early flush of enthusiasm potential investors and manufacturers have had second thoughts. The flop of TV-am and generally reduced viewing figures suggest that a possible 30 channels of cable TV will not be a licence to print money. Those days are gone. Nonetheless, if cabling goes ahead as it inevitably will there will be a steady living as a reward for success.

Predictably the Opposition wanted monopoly powers granted to British Telecom and complained that the whole idea was divisive in that some poor people may not be able to afford the service. But, of course, there is nothing to prevent BT competing in the market and BT's chairman, Sir George Jefferson, positively welcomed the go-ahead and appointed Donald Wray as supremo of BT's spearhead thrust into the whole area of broadband local networks including interactive services. The argument on divisiveness is plainly silly. Few of us can afford to motor in a Rolls-Royce but that is no reason why luxury cars shouldn't be built for those who can. The provisional indication of a £5 per week subscription is hardly likely to deter keen viewers.

Industry will benefit almost immediately. Racal-Oak have announced a £3 million initial contract from British Telecom for the supply of decoding equipment which ensures that viewers can access only those programmes and services to which they have subscribed.

Inmos

Since my last comment on Inmos the company has revealed at a press conference the latest state of play. For newcomers, Inmos was born in 1978 during Labour's last administration using as midwife the National Enterprise Board who were to finance the company with £50 million in two instalments of £25 million. The objective was to build up an all-British VLSI chip capability while at the same time creating 4,000 new jobs in the UK. The business target was set at £150 million of profitable turnover by 1984.

Inmos started trading in 1981 and in that year (to December 31) achieved £2·1 million turnover with a trading loss of £13 million. Last year sales accelerated to £13·7 million and the loss rose to £20·4 million. This year turnover is running at some £20 million, whether profitably or not is as yet unclear.

Total new jobs created in the UK are 275, expected to increase to 575 during the coming year. Current forecast is that no more than 1,000 jobs will be available at the Newport, Gwent, factory and a second factory, scheduled in the original plans, is not shelved but certainly far in the future.

All is not gloom. The Transputer, described as a single-chip micro-computer, should hit the market at the end of next year although not contributing profit until 1985. Meantime the memory products can reasonably expect to be generating profits as the capacity for high volume production at Newport is steadily increased.

Back-Up

No manufacturer can succeed without adequate after-sales service. But good engineers are in short supply, transport costs are high and hotels and meals don't get any cheaper. But even more important than cost is speed and quality of service on which the whole reputation of a company may well depend.

Engineering for reliability, testability and maintainability has made great advances in electronics manufacturing and overall reliability has greatly improved through LSI and other modern techniques. Against this there is the ever-increasing complexity of equipment and systems. At the end of the day things can and do go wrong and service engineers continue to be needed.

With high costs and a shortage of skilled people is there a better way of organising service visits, particularly those occasioned by panic? Digital Equipment has found an answer not by putting more men on the road but taking their most skilled engineers off the road completely.

Not for them the tedium of traffic jams or living out of a suitcase. Instead, 16 of the best are housed in air-conditioned comfort at the company's Basingstoke customer service centre, offering a 24hr service.

The key to successful service is diagnosis and it is in this key role that the Basingstoke experts excel. Once the fault has been pin-pointed to component or, at worst, p.c.b. level, rectification is a simple matter and can be completed by a less skilled travelling engineer.

The operation depends on a data communications network over which the Basingstoke diagnosticians can access the faulty DEC minicomputer and, backed up by a large mainframe computer, perform powerful test routines even though the remote faulty mini may be hundreds of miles away. The European network is continually extended as every new DEC mini delivered is supplied with the necessary modem and auto-dialler to complete the remote testing link.

So now the experts, instead of making one or at most two service calls a day, can service many more just by staying put.

Upturn

It is now clear that the current upturn in activity started last year with an increase in consumer spending. It is heartening to report that consumer electronics is back in business after so long in the doldrums. TV sales were a record last year and this year looks even better. Home computers are a brisk and expanding market and it is a pity that of over two million VTRs sold in the UK none were manufactured here.

Capital equipment sales remain buoyant with the defence sector aided by the replacement programme following the Falklands campaign. The Electronic Engineering Association reported an eight percent increase in output during the past year at £2,125 million. Direct exports totalled £740 million but is probably about £1,000 million after taking account of equipment fitted in, for example, aircraft or other systems sold as a complete package.

Some sectors have fared better than others. Marine electronics has slipped back as a direct reflection of the world slump in shipping. The UK market for military tactical radio has slackened now that the British army has been re-equipped but exports are still doing well. Avionics remains in the superstar class and won Marconi Avionics two Queen's Awards this year, one each in technology and exports. Latest Marconi scoop is a £25 million order from the Royal Australian Air Force for airborne anti-submarine systems. The company has also teamed with Honeywell in military application of ring laser gyroscopes for inertial navigation.

The EEA reports a drop in employment in the capital goods sector of three percent to 98,000, the result of modernisation in manufacturing and assembly techniques. A chief constraint to rapid expansion is the shortage of engineers, a perennial problem.

LOGIC ANALYSER

Part One
D. MANDELZWEIG

IT IS evident by looking at recent projects in this magazine, that digital electronics in general, and microprocessors in particular, are playing an ever-increasing role in amateur projects. Many hobbyists are designing their own, building from kits, or just using home computers. There comes a time when it is necessary to test new designs, debug built projects, or fault-find digital circuitry. The most useful piece of test equipment for this is a logic analyser. However, due to the price of commercially available equipment, such a luxury is normally out of reach of the amateur.

The logic analyser to be described was designed to overcome this problem. The unit is used with an oscilloscope (when the 'scope display option is fitted), a piece of test equipment more easily affordable to the hobbyist. With a guaranteed maximum working frequency of 5MHz (the prototype worked to 7·9MHz), the analyser can cope with nearly all microprocessor systems found in the home today. Even systems working at a faster clock frequency can be tested by running the system (while testing) at a lower clock frequency. Comparison of the logic analyser's specifications (see Table 1.1) with those of commercially available units shows that the facilities offered compare favourably, for a much smaller outlay.

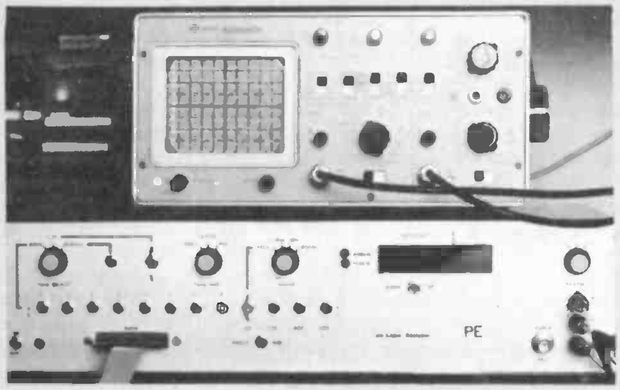
The analyser was designed to be as modular as possible. This allows the power of the analyser to be increased as and when it is needed, and is affordable. Five options can be fitted to the basic unit. Only one option is required to have a useful instrument. All the options are plug-in, and therefore have retrofit capability, and can be fitted in virtually any order.

Since the majority of microprocessors run with a clock frequency less than 5MHz, and it was a design requirement to be able to test 5MHz systems, the use of a µP was ruled out. However, even using Schottky TTL, some clever use had to be made of available i.c.s, in order to achieve the design requirement. For this reason, it may still be of interest to readers who do not intend building the unit to read the paragraphs on the circuit operation description.

WHAT IS A LOGIC ANALYSER?

An oscilloscope can display two (*four* on expensive models) traces of real-time information. When testing digital circuits, it is useful to be able to see the timing relationship between various signals, or alternatively, if looking for example at a data bus, to be able to look at the sequential data being put out on the bus. A logic analyser enables one to do this. Synchronously with the clock of the system under test, it captures and stores a number (depending on the memory size) of bytes, each byte being 8, 16 or 32 bits wide, depending on the design. The analyser then subsequently displays the timing diagram of the captured data on a CRT display. In order to make the analyser more useful, a number of facilities are usually incorporated. As mentioned, the analyser can be driven synchronously with an external clock. When using the external clock, the negative or positive edge can be selected, and clock qualifiers are provided. These can be switch-selected such that a logical 1, 0 or X (don't care) makes the input valid, so that external signals can control when the analyser stores information. There are usually three methods of triggering an analyser to start (or stop) storing data. A word recogniser can be used to compare the incoming data with a previously set up bank of switches (one switch for each input, allowing a 1, 0 or X to be selected) when the data is equal to the present word, the analyser is triggered. An external input, with the rising or falling edge selectable, is also provided for triggering, or manual trigger is possible with a switch. To further enhance the triggering capability, the user can select how the analyser must store the data with respect to the trigger. The trigger can be used to stop storing data (for a 1K byte memory, the analyser will store 1024 bytes *before* the trigger occurs), called post trigger, start storing data on the trigger (store 1024 bytes *after* the trigger), called pre trigger, or store 512 bytes *before* and 512 bytes *after* the trigger, called centre trigger. A more detailed explanation of the uses and working of these facilities will be given below. Since it is normally impossible to display all the bytes of data stored simultaneously (the display would be unreadable) only a portion of the memory is displayed, and the user can scan up and down the memory. Expand facilities can also be provided, so that although less bytes are displayed, more display resolution is achieved. The more expensive analysers provide cursors which can be moved across the display. Some also provide the capability to store two sets of data in two separate memories, and then compare the memories for differences.

This logic analyser includes most of these facilities. Eight input lines and a 1K x 8 memory allow 1K bytes of 8 bit



SPECIFICATION

TABLE 1.1. Specifications, modes and facilities

DATA IN:

NO. OF INPUT LINES : 8
INPUT LOAD : 1 LSTTL LOAD EACH
DATA MUST BE VALID AT THE RISING (FALLING) EDGE OF THE INPUT CLOCK
DATA HOLD TIME : 60ns
(ie DATA must be valid for at least 60ns after the rising (falling) edge of the clock occurs)
STORAGE DEPTH : 1024 BYTES
OPTIONAL : CMOS HI-Z INPUTS

CLOCK:

EXT IN (Synchronous) : MAX 5MHz
RISING (FALLING) EDGE SELECTABLE CLOCK MUST BE HIGH (LOW) FOR 50ns MIN
INPUT LOAD : 1 LSTTL
MIN MARK OR SPACE : 60ns

INTERNAL (Asynchronous) : (OPTIONAL)
5MHz CRYSTAL CONTROLLED
5MHz, 1MHz, 100kHz SELECTABLE FOR ASYNCHRONOUS OPERATION

When SYNCH clock is selected, 5MHz is available for synchronisation or as a clock drive at CLOCK OUT. When either 5MHz, 1MHz, or 100kHz asynchronous clock is selected, then the selected frequency is available at CLOCK OUT.

CLOCK OUT:

SEE OPTIONAL INTERNAL CLOCK ABOVE

CLOCK QUALIFIERS:

NUMBER: 3 POS OR NEG LEVEL SENSITIVE
Any or all may be chosen as negative, positive or don't care.

LEVELS MUST BE VALID A MINIMUM OF 2ns BEFORE THE CLOCK EDGE.

NOTE: The qualifiers are level sensitive, and must be valid for the duration of the sample.

ARMING:

THE UNIT IS MANUALLY ARMED, AND CAN BE RESET AT ANY TIME.

NOTE: To ensure that all old data is over-written by the new data when POST or CENTRE trigger is selected, the unit must be armed at least $\frac{1024}{fin}$ secs before the trigger occurs.

TRIGGERING:

WORD RECOGNISER : SELECT INPUT WORD ON SWITCHES, INCLUDING DON'T CARES.

EXT TRIG : RISING OR FALLING EDGE SELECTABLE
TRIGGER IS EDGE SENSITIVE
TRIGGER MUST OCCUR WITHIN 70ns OF THE RISING (FALLING) EDGE OF THE CLOCK

MANUAL TRIGGER : MANUAL SWITCH
TRIGGER SELECT : PRE TRIGGER, POST TRIGGER OR CENTRE TRIGGER SELECTABLE.

DISPLAY MODES:

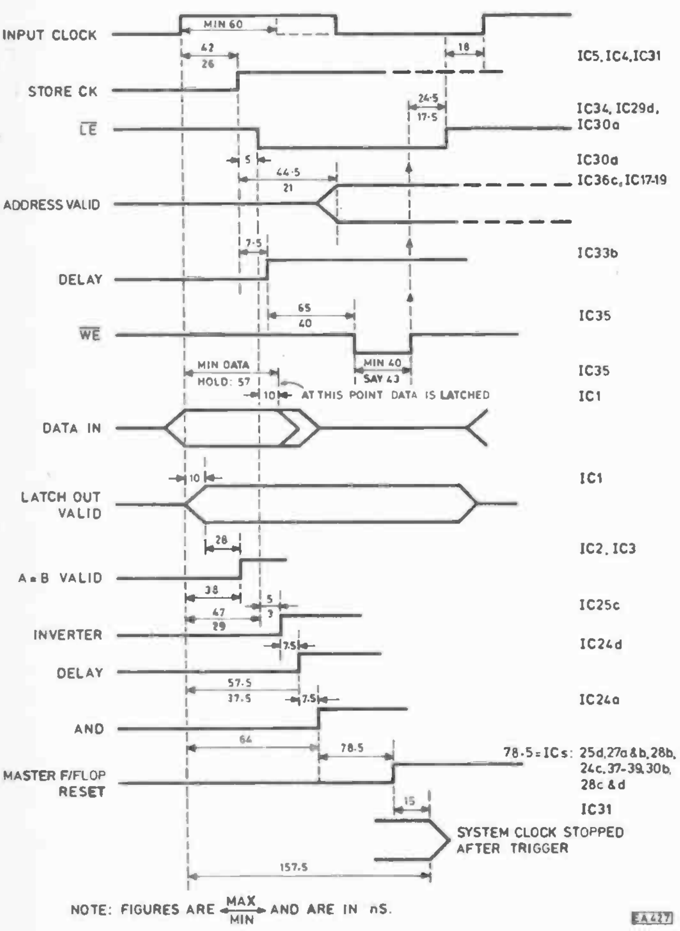
HEX DATA DISPLAY (OPTION 2)
2 DIGIT HEX DISPLAY OF DATA BYTE. ANY DATA BYTE WITH RESPECT TO THE TRIGGER WORD CAN BE DISPLAYED BY THE UP/DOWN SWITCH. THERE IS A DECIMAL DISPLAY OF THE ADDRESS OF THE DATA WORD BEING DISPLAYED

SCOPE DISPLAY (OPTION 1)
DISPLAYS 8 BITS BY 64, 32 or 16 BYTES. THE START BYTE IS SELECTED BY THE UP/DOWN SWITCH, AND THE DECIMAL DISPLAY SHOWS THE ADDRESS OF THE START BYTE.

BOTH OPTIONS MAY BE FITTED SIMULTANEOUSLY. IF THE SCOPE OPTION IS USED, A FURTHER OPTION MAY BE ADDED. THIS OPTION HIGHLIGHTS THE TRIGGER WORD WHEN IT IS DISPLAYED ON THE SCOPE.

data words to be stored. The analyser has an external clock input (up to 5MHz), with the clock edge switch selectable. Three clock qualifiers are provided, and each can be selected for a 1, 0 or X. With the clock option fitted, the analyser can also run asynchronously at three selectable frequencies—5MHz, 1MHz and 100kHz. The selected clock frequency is buffered and is brought out to the front panel, so that the circuit under test can be driven by the analyser's clock. The three modes of triggering discussed above are provided: external (edge selectable), manual, and word recogniser. A bank of 8 switches is provided for this, and each input line can individually be set for a 1, 0 or X. The analyser allows the selection of pre, centre and post triggering as defined above. Two data display options are possible, one of which must be fitted to make the unit useful, although both can be fitted if desired. The one option displays 64 bytes by 8 bits (8 traces) of timing diagrams on a normal oscilloscope display (the oscilloscope must be a dual trace one with X-Y capability). The display can be expanded so that only 32 or 16 bytes are displayed. The display can also be scanned up and down the memory. The other option allows the Hex value of the data to be displayed on two 7-segment displays. For both options, a 4-digit display indicates the address of the data byte with respect to the trigger point for either the data being displayed in Hex for the Hex display option, or the first data byte of the set of 16, 32 or 64 bytes being displayed by the scope option. When both options are installed, the Hex data corresponds to the first (left-most) byte being displayed on the scope. A further option available which can only be used in conjunction with the scope display option, uses the Z-MOD input of the oscilloscope to brighten up the trigger byte (the byte at which the analyser was triggered) when that byte is being displayed on the oscilloscope. Finally, the basic analyser accepts TTL compatible inputs, however the last option available will allow the testing of CMOS or other circuitry, at user defined supply rails.

Fig. 1.1. Analyser timing diagram



SPECIFICATIONS

A complete list of specifications is given in Table 1.1, and these are self-explanatory. Perhaps the only extra explanation required is that of ARMing. Normally the analyser is in the display mode, displaying previously captured data. To get the analyser ready to capture new data, the unit must be ARMed. This is done manually with a switch, and when it occurs, the ARM l.e.d. lights, the data being displayed becomes invalid, and the analyser awaits the trigger. During this time, the analyser is storing data, so that when a trigger comes, and POST triggering, for example, has been selected, the analyser can stop storing data immediately. If the trigger arrives too soon after the analyser is armed, then in this case (POST triggering) the memory will not be completely overwritten, and some old data will remain. This is the reason for the note given in the specifications. In any event, when the trigger arrives, the TRIG l.e.d. lights, and both remain on until the data has been stored. At this point, the l.e.d.s extinguish, and the analyser automatically reverts to displaying the new data. At any stage, the ARM/RESET switch can be used to reset the analyser from the ARMed state to the display state.

CIRCUIT DESCRIPTION

Before considering how the circuit works, it is necessary to keep two factors in mind. The first is that with a 5MHz clock, only 200ns is available to do the following: increment the RAM address, check for a valid trigger, generate the Write pulse to the RAM, and then be ready to repeat the sequence. A look at the circuit diagram shows that signals

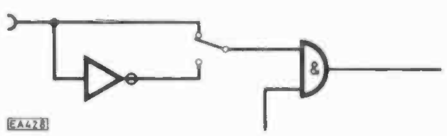


Fig. 1.2. Simple positive/negative selection

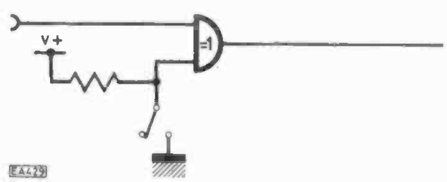


Fig. 1.3. Improved positive/negative selection

have to pass through quite a few i.c.s, and the propagation delays through each begin to add up. For this reason, one has to firstly be careful that the total worst case time to complete a cycle does not exceed 200ns, and secondly that the Enable, Latch, Data, and Clock pulses are generated in the correct time slots and sequence, to ensure reliable operation. With the aid of the timing diagram shown in Fig. 1.1, we will be looking at how correct timing was achieved.

The second factor concerns data skew. For example, consider the EXT. TRIG. input where either positive or negative edge triggering is possible. A simple way to achieve selection is shown in Fig. 1.2. The problem with this circuit is that:

1. When negative edge is selected, the input sees only one gate input, and when positive edge triggered, the input sees two gates.
2. Because of the extra invertor, the propagation delay for negative edge triggering is longer than that for positive edge triggering.

To overcome this, the circuit of Fig. 1.3 is used. This circuit has one further advantage, that the input signal itself is not physically switched—the switching is done by a d.c. level applied to the EX-OR gate. This second factor also applies to the clock and qualifiers' inputs, as well as to the word recogniser. In these two cases a different method was used to overcome the problem.

Refer to Figs. 1.4, 1.5 and 1.6 for the block diagram, front panel circuitry, and main board circuitry respectively. Assume that the unit is on, and has been reset. We now want to store data, so we must ARM the analyser using switch S16. This sets the master flip-flop consisting of IC28c & d L (low) on STORE, and H (high) on STORE become valid, with the following effect: IC1's outputs become valid (no longer in Tri-State). IC15 gates data from the data bus to the RAM, the RAM is put in the WRITE mode, IC27b and IC31 are enabled. Depending on the setting of S14, IC31 selects either the SYNC CLOCK, or one of the three asynchronous clock frequencies from the CLOCK OPTION, if it is fitted. Since the inputs to the i.c. are paralleled to both halves of the i.c., the same selected clock appears at both outputs (except in the case of SYNC CLOCK selection, where the internal 5MHz clock appears at output 2Y). Thus the internal clock frequencies are buffered and made available at SK7 on the front panel. The output of 1Y is called the STORE CK. Normal gates were considered for the selection of STORE CK, but calculations of propagation delays proved that using IC31 would be faster, with the advantage of a smaller total chip count. Assume now that the SYNCH CLOCK has been selected. However, before continuing with the STORE CK, let us see how the SYNCH CLOCK was derived. Since the clock qualifiers must act on the input clock, some sort of gating must be incorporated. We also want to be able to select positive or negative clock edge, and the qualifier level. At the same time we must be careful of data skew. To solve the problem, all four inputs are buffered with a single LS TTL gate (IC5) each. This allows the lowest possible load to be applied to the circuit under test. The clock and qualifier inputs are fed to one set of inputs of a 4-bit magnitude comparator, IC4. The i.c. gives an output on pin 6 only when all the bits in one set of inputs correspond to the bits in the second set of inputs. Consider selecting positive edge for the CLOCK, positive level for CQ1, negative level for CQ2, and don't care for CQ3. For CQ1 positive, B2 input is low, and thus S2a is switched such that A2 is low. Similarly, for CQ2, B3 will be high, and with S3a in the position shown, R20 will hold A3 high. In the don't care case, S4 is switched such that R25 and R21 pull B4 and A4 high respectively. So when the correct inputs are applied to the qualifiers, the respective B inputs will be equal to the A inputs. For positive clock edge S1a wiper is at 0V, i.e. A1 is low, when the clock goes high, B1 will become low (due to the inverter) and because these inputs as well as the qualifier inputs are now equal, IC4 pin 6 goes high. When the clock falls, A1 is not equal to B1, so pin 6 goes low, and

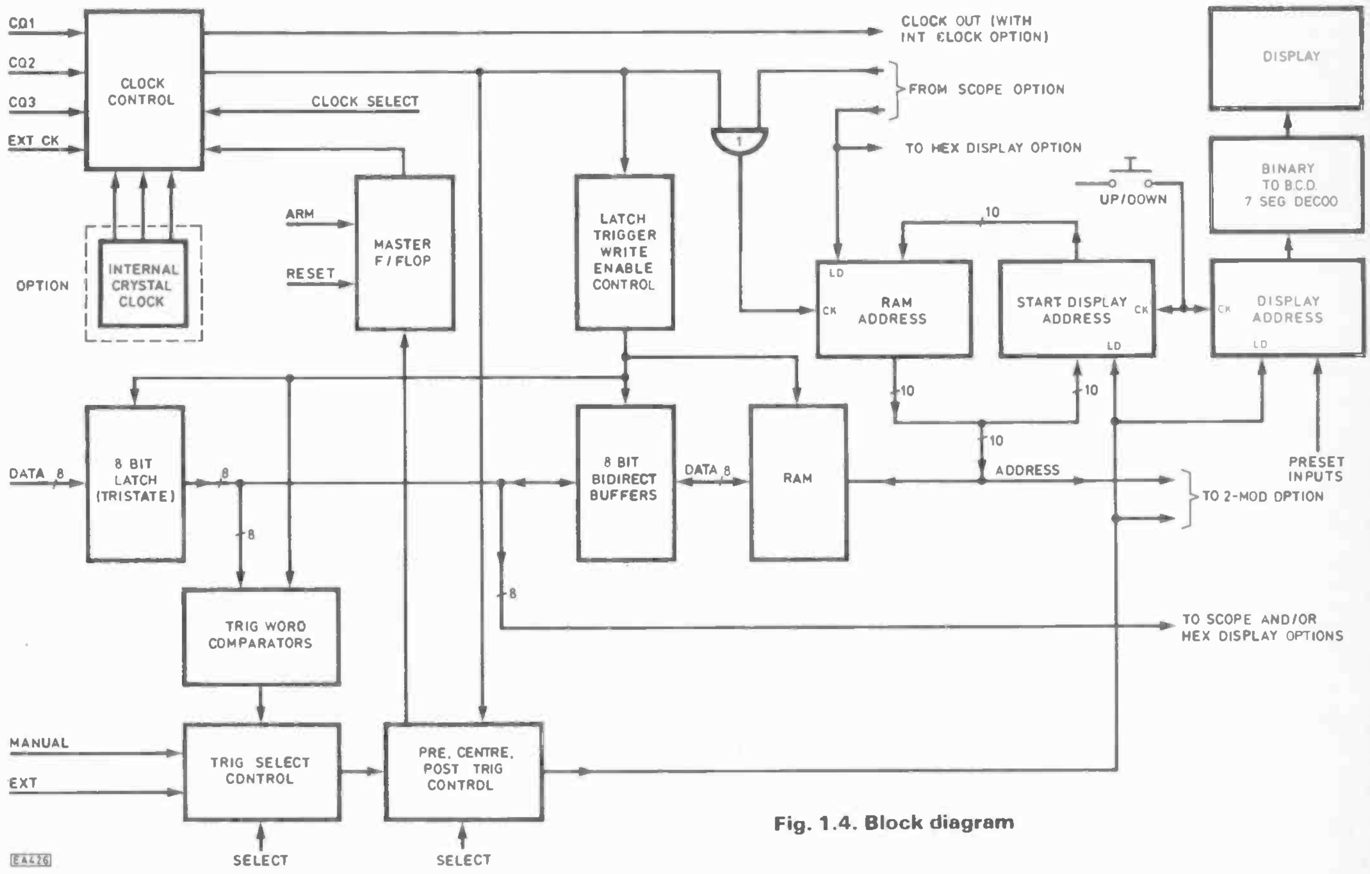


Fig. 1.4. Block diagram

thus follows the input clock. If a qualifier became invalid, the clock would stop, and that if negative clock edge is selected, the output at pin 6 would be an inverted version of the input clock. By the use of only one i.c., all the clock functions have been implemented, propagation delay has been kept to a minimum, and data skew has been avoided, as all inputs to the i.c. have similar propagation delays through the i.c.

Now to come back to the STORE CK. IC24b has been disabled by L on STORE, and its output is high. The STORE CK passes through IC36c, and is applied to the RAM address counters' clocks (ICs 17–19). Pin 1 of IC23a is low, and therefore pin 3 is high, with the result that the LD inputs of the RAM counters are high. Therefore the counters are being clocked, and the RAM is being addressed in time with the input clock. Now every time IC31 pin 7 (STORE CK) goes high, the output of IC30a ($\overline{LE}$) goes low, latching the data into IC1. There are two further requirements of the STORE CK. Firstly a WRITE pulse with a minimum width of 40ns must be generated to store the data in the RAM, but only when the address and the data are valid. Secondly, the input latch, IC1, must remain latched for just long enough so that the memory stores valid data. The circuit works like this. When the analyser is ARMED, H on STORE goes high, and this sets the Q1 and Q2 outputs of IC34 (via the CLR inputs) to low. The output of IC29d is thus low, and because pin 12 of IC31 is still low, $\overline{LE}$ is high. When the STORE CK goes high, $\overline{LE}$ goes low, and the input data is latched. One cannot rely on the STORE CK to hold $\overline{LE}$ low, because for a 1:1 mark-space ratio 5MHz clock, the high level is only valid for 100ns which, as we will see, is too short. So what happens is that the STORE CK clocks the first D-TYPE, and Q1 goes high. IC29d output thus goes high, and now regardless of whether the STORE CK falls away or not, $\overline{LE}$ remains low. Q1 of IC35 goes low after the propagation delays of IC33b and IC35, and remains low for approximately 43ns, which is long enough to write the data into RAM. On the rising edge of Q1 (IC35), Q2 of IC34 is clocked high, IC29d goes low, and if the STORE CK has become low, $\overline{LE}$ once again becomes high. If STORE CK is not yet low, $\overline{LE}$ will remain low until this occurs. When the next STORE CK comes, the sequence is repeated. With this little bit of circuitry then, input data is latched, held long enough to be stored, the store pulse ($\overline{WE}$) is produced, and the latch is disabled once again.

At this stage we have the input clock clocking the RAM, and input data being stored in the RAM. The counters IC17 to IC19 are cycling through a count of 1023. Now we must consider the trigger circuitry. The type of trigger is selected by S19, and IC25a, b & d. Manual trigger is simple: IC26 produces a pulse, IC25b goes low, IC27a goes high and IC27b goes low. EXT works similarly, with IC29c and S18 allowing the rising or falling edge to be selected. For this case S19 enables IC25a.

WORD RECOGNISER

The word recogniser works in a similar fashion to the clock and its qualifiers, in that the incoming data is compared to data set up on switches S6 to S13. ICs 2 and 3 do the comparison, and produce a high level output when the data sets are equal. This output is gated via IC24a through IC25d to IC27a, if the word recogniser trigger has been selected. The requirement for gating the output is that a false trigger may occur while the latch outputs are settling, or input data is changing. To avoid this, $\overline{LE}$, suitably inverted (by IC25c) and delayed (IC24d) to allow for latch settling time, only enables IC24a when the data at the output of IC1 is valid.

Now when IC27b goes low, the flip-flop consisting of IC28a & b sets. The flip-flop is capacitively coupled, and this allows pin 5 to go high even if IC27b stays low so that the flip-flop can be reset when necessary (this ensures that triggering is only edge sensitive for all the triggering modes). IC28a goes low, lighting the TRIG l.e.d. The flip-flop consisting of IC30c & d is set by IC28b via C7, which again allows the second flip-flop to reset before the first one does. The flip-flop triggers the monostable IC32, which provides a positive and negative pulse. The positive pulse is used to reset the second flip-flop, and also for the Z-MOD option, to be described in a future part. The reason for the second flip-flop being necessary, as will shortly be explained, is that the first flip-flop can be reset immediately after being set. Thus the time for which the flip-flop is set is virtually that of the propagation delays of two STTL gates, being approximately 10ns. Since a 74121 requires a minimum input pulse of 50ns, this lengthened pulse is provided by the second flip-flop. The negative pulse produced by IC32 (ADL) firstly loads the address that was on the address bus into ICs 20–22, so that the address at which the analyser was triggered, is stored. ADL also loads the preset binary number 0, 511 or 1023, depending on S5 into the counters ICs 7–9. IC10 and IC11, two EPROMS, decode the binary number into BCD, and the number is displayed on displays 1–4. Thus the display is preset with a number depending on which TRIG POSition is selected—0 for POST, 511 for CENTRE, or 1023 for PRE trigger. With IC28b output low, counters IC37–39 are preset to zero, and when POST goes high, the counters and IC24c are enabled. This allows STORE CK to clock ICs 37–39. Again, depending on position of S5, either POST, or QA or QB is switched to IC30b. If PRE trigger is selected, QB is connected, allowing the counter to count to 1023 before a pulse is produced which resets the main flip-flop. The count of 1023 allows the memory to be filled with 1K of data from when the trigger occurs. In other words, the analyser was triggered to start storing data, and this is thus called PRE-trigger. If CENTRE trigger is selected, the counters count to 511 before resetting the main flip-flop. Here the memory is only filled with 512 bytes of data after the trigger and thus contains 512 bytes of stored data before the trigger occurred. Hence the name centre trigger.

POST TRIGGER

Finally for POST trigger, it is required that the analyser stops storing immediately, so POST signal is connected directly to the reset. As can now be seen, when POST is selected, IC28b causes itself to be reset via the switch and IC30b, and for this reason IC30 c & d are required as explained above. Once the main flip-flop and IC28 a & b have been reset, the ARM and TRIG l.e.d.s extinguish, IC1 becomes Tristate, IC15 gates RAM data to the data bus, the RAM goes into its read mode, IC31 (and thus the STORE CK) is disabled, and ICs 17–19 have their LD input taken low by IC23a, so that the trigger address loaded into ICs 20–22 now passes through ICs 17–19. This means that the data stored when the analyser was triggered is on the data bus, and the data corresponds to the trigger position being displayed on the address display. If POST trigger had been selected, 0 would be displayed, showing that the data byte on the bus is the first data byte stored, i.e. the trigger data byte. For CENTRE trigger, 511 would be displayed, implying that the trigger data byte is in the middle of the RAM, and similarly, for PRE trigger, 1023 will be displayed, indicating that the trigger byte was the last byte stored. Before discussing briefly how the data is displayed (the display options will be described in Part 3), let us now look at the timing diagram, Fig. 1.1.

SYSTEM TIMING

We will take the rising edge of the input clock as reference. Using maximum and minimum propagation delays as given in the Texas Instruments TTL Data Book, STORE CK will go high a maximum of 42ns later and a minimum of 25ns, due to the delays through IC5, IC4 and IC31. Taking into account the delay through IC30a, $\overline{\mathrm{LE}}$ goes low 5ns later. Also, 44·5ns after STORE CK goes high, the address on the data bus becomes valid (delays are due to IC36c and the counters IC17–19). Now if IC33b is not in circuit, and the minimum propagation time across IC35 is assumed, it is possible that $\overline{\mathrm{WE}}$ will become valid 2·5ns before the address is valid. Thus the delay through IC33b is included to ensure that this cannot happen. Now since it takes (worst case) 47ns for $\overline{\mathrm{LE}}$ to go low, and then 10ns for $\overline{\mathrm{LE}}$ to latch the data, the input data must remain valid for 57ns, hence the 60ns data hold time specified. Also, to ensure that $\overline{\mathrm{LE}}$ remains low for fast clocks, the input clock must remain high for at least 62ns, to allow the clock propagated through IC34 and IC29d to hold $\overline{\mathrm{LE}}$ low. After a worst case delay of 65ns across IC35, the $\overline{\mathrm{WE}}$ becomes valid for 43ns and then 24·5ns later (due to IC34, IC29d and IC30a) $\overline{\mathrm{LE}}$ goes high again (assuming of course that the STORE CK is already low). This would then be a worst case total of 182ns after the input clock edge, which allows 18ns spare before the next clock edge arrives. As is specified, the data input must be valid at the rising edge of the input clock, and becomes valid at the output of IC1 10ns later due to the delay through IC1. The comparators take 28ns for the compare, and including the delay of IC1, the A = B output is valid 38ns after the rising clock edge. Now including the delay of IC25c, $\overline{\mathrm{LE}}$ applied to IC24a (without IC24d) would take a minimum of 29 + 3 = 32ns, which would mean that IC24a could be enabled 6ns too early. Thus the delay of IC24d is included to ensure that the A = B signal is valid before IC24a is enabled. IC24a adds 7·5ns and then the trigger path adds a further 78·5ns before the master flip-flop is reset. This means that the time taken between the rising edge of the input clock and the point at which a word recogniser trigger stops the STORE CK, is 157·5ns. This last calculation ensures that the analyser is reset within 200ns, i.e. before the next clock edge arrives.

COMPONENTS . . .

Resistors

R1–R25, R34, R35, R40, R68, R70	10k (30 off)
R26–R29, R36–R39, R63–R67, R72–R75, R77–R88	1k (29 off)
R30, R32, R69	100k (3 off)
R31, R33	27k (2 off)
R42–R62	470 (21 off)
R41	270
R71	220
R76	2k 1% $\frac{1}{4}$W

All resistors are 5% $\frac{1}{4}$W unless otherwise stated

Capacitors

C1, C2	2μ2/16V tant. (2 off)
C3, C4, C9–C26	100n/16V tant. (18 off)
C5	4μ7/16V tant.
C6, C7	150p ceramic (2 off)
C8	30p ceramic
C28, C30, C32	1μ/35V tant. (3 off)
C27, C29, C31	10μ/35V tant. (3 off)
C33	4700μ/25V elect.
C34, C35	2200μ/25V elect.

Transistors & Diodes

TR1	BC108
REC1	100V p.i.v. 5A
REC2	100V p.i.v. 1A
D1, D2, D3	3mm red l.e.d. (3 off)

Integrated Circuits

IC1	74LS373
IC2, IC3, IC4	74S85 (3 off)
IC5	74LS04
IC6	ICM7556
IC7–9, IC20–22	74LS193 (6 off)
IC10, IC11	2716 (2 off)
IC12–14	74LS47 (3 off)
IC15	74LS245
IC16	MK4801A–55
IC17–19, IC37–39	74LS191 (6 off)
IC23	74LS00
IC24, IC33	74S08 (2 off)
IC25, IC28	74S00 (2 off)
IC26, IC32, IC35	74121 (3 off)
IC27	74S20
IC29	74S86
IC30	74S02
IC31	74S153
IC34	74S74
IC36	74S32
IC40	7912CT
IC41	7812CT
IC42	LM323K

Switches

S1, S18, S21	DPDT min. toggle (3 off)
S2–4, S6–13	DPDT (with centre off) min. toggle (11 off)
S5, S19, S20*	4P3W rotary (3 off)
S14	3P4W rotary
S15	DPDT momentary action
S16, S17	DPDT momentary action (with centre off) (2 off)

Miscellaneous

T1	Transformer 9V @ 3A
T2	15–0–15 @ 150mA
SK101*	Red banana socket
SK102*	Black banana socket
SK103*	Green banana socket
SK7	BNC female chassis mount
SK4, SK5	16 pin i.c. socket (2 off)
SK3	14 pin i.c. socket
SK1, SK2, SK6, SK8	Double-sided wire-wrap p.c.b. edge connector. See text (4 off)

14 pin wire-wrap sockets for displays (6 off)
Sockets for i.c.s: See text
Heatsink, nuts & bolts, stand-off pillars.
Case: 440mm x 110m x 200mm deep.
Soldercon i.c. socket strips (see text)
16-way ribbon cable
Ribbon cable headers to fit 16-pin i.c. sockets (4 off)
Fuse and fuseholder (chassis mount 500mA)
Coloured "Easy-Hooks"
X1–X4 0·3" l.e.d. 7-seg. display (Maplin common anode type)
X5–X6 0·3" l.e.d. 7-seg. display (FND357)

*These items are used with the display options. Since they are relatively cheap, it is recommended that they are fitted to ease retro-fitting of these options. Refer to text.

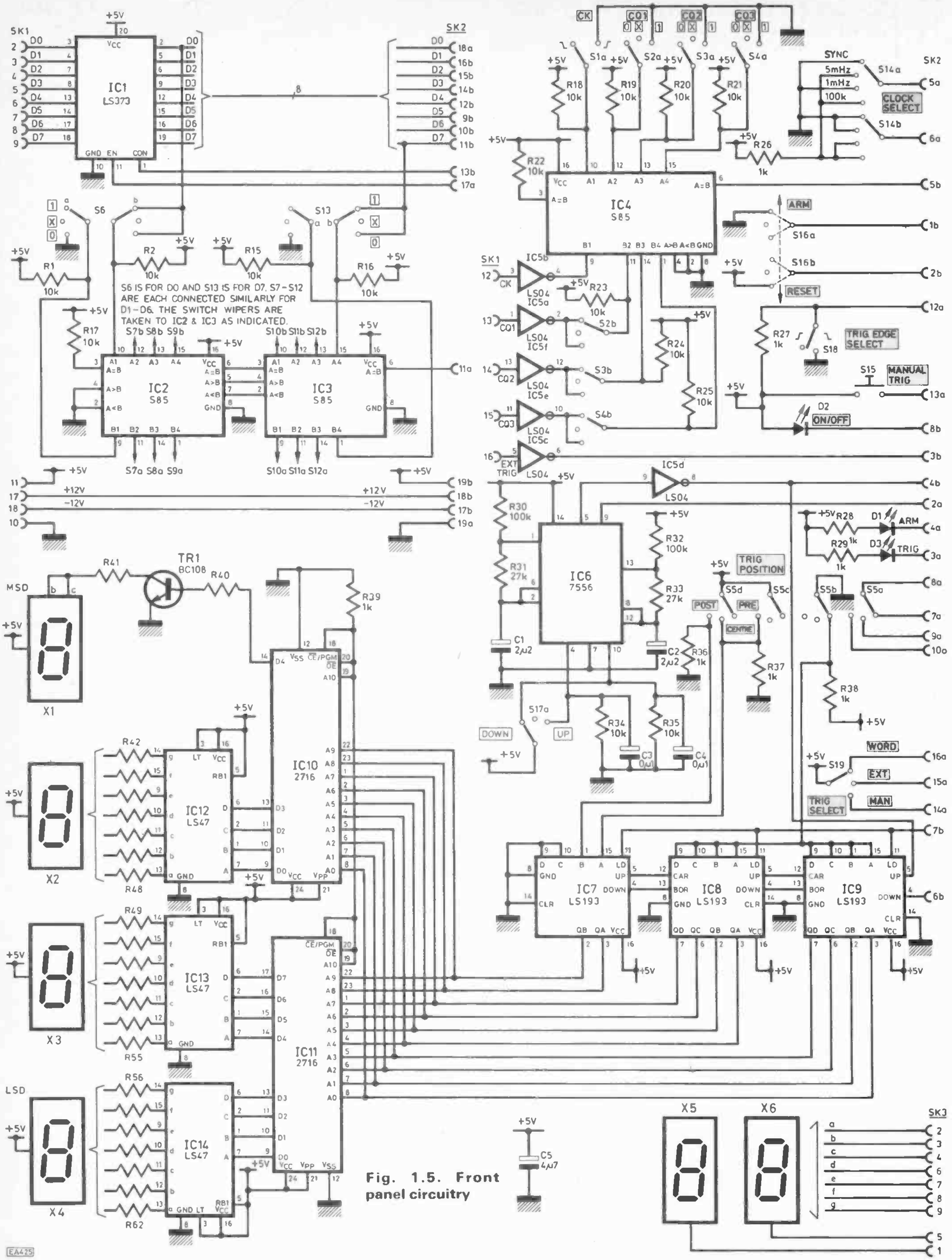


Fig. 1.5. Front panel circuitry

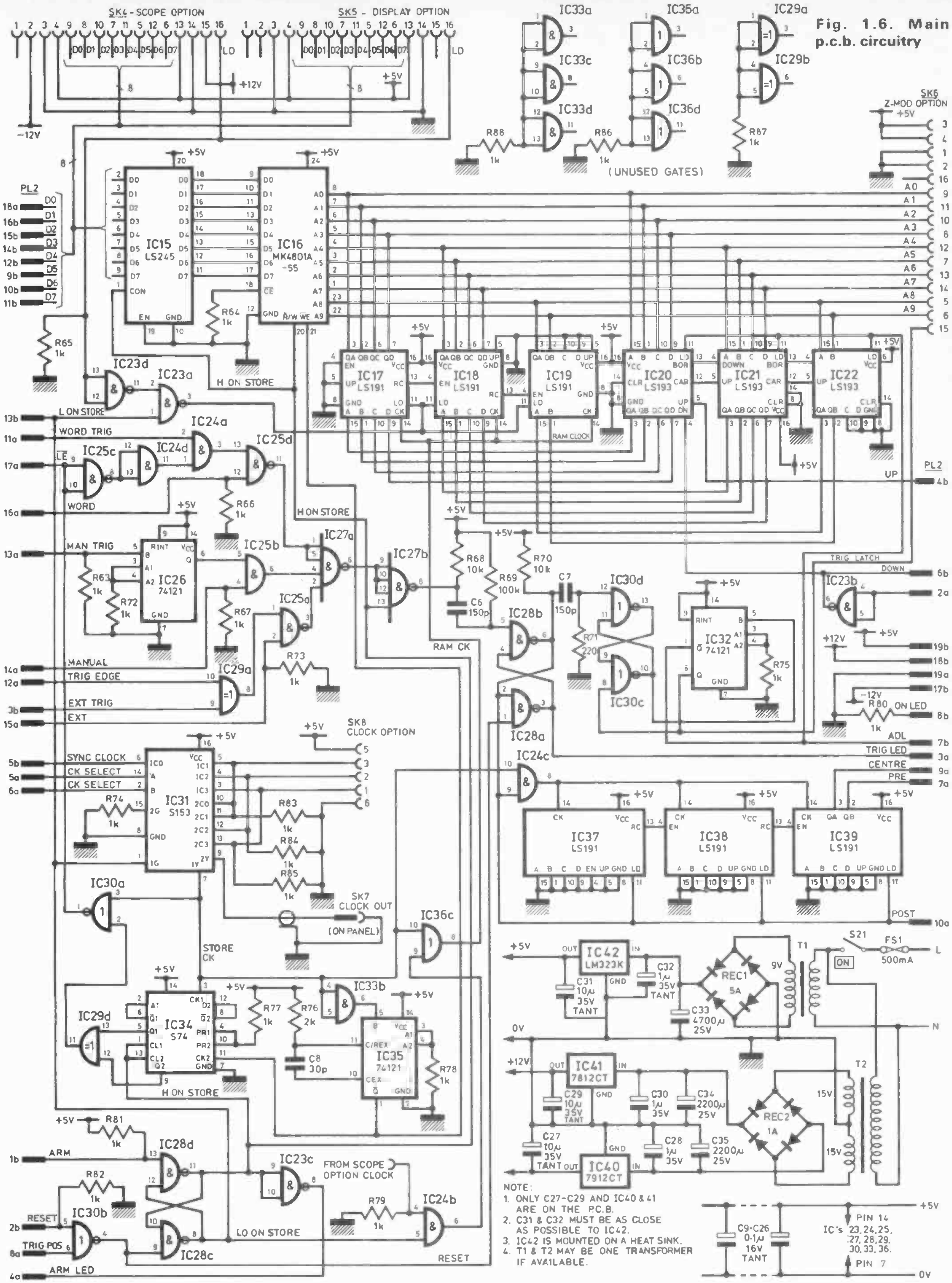


Fig. 1.6. Main p.c.b. circuitry

The clock modifiers *must* be valid before the trigger word appears, to get the analyser triggered. Once triggered, the modifiers can then be used to select data to be stored, i.e. to start and stop storage as required. The reason for this requirement is that the trigger pulse is gated through by IC24a, which is enabled by $\overline{LE}$, which is in turn derived from the STORE CK. So if the modifiers are invalid there is no SYNC CLOCK, which means no STORE CK. Hence the trigger word will never get through. Once IC28b and IC28a have been set, it does not matter if no more pulses come through, therefore the modifiers can be used.

All unused inputs of the probe (including unused modifiers and EXT input) should be tied high or low, especially when operating at higher frequencies. Floating gate inputs can affect other inputs of the same i.c., and although no problems were experienced with the prototype, this is good practice.

DATA DISPLAY

Assuming no scope option, the input to IC23d (LD) is low, and the output of IC23a is therefore low. As already explained, the address on the outputs of ICs 20–22 are therefore passed through ICs 17–19, and the data corresponding to that address is on the data bus. Because LD is low, the latch on the Hex display option is disabled (not latched) and the data on the data bus is displayed. If S17 is now activated, one of the halves of IC6 oscillates, and the counters ICs 7–9 and ICs 20–22 increment or decrement in unison. ICs 7–9 keep track of the address of the data byte being displayed, while the RAM address is being set by ICs 20–22. If now the scope option is fitted, the option applies a 64kHz, 32kHz or 16kHz clock (depending on the option's expand switch) to IC24b, which at this time is enabled. This clocks ICs 17–19. LD is also being held high, so the LD inputs of ICs 17–19 are invalid. However, every 64, 32 or 16 clock pulses, LD is pulsed low, reloading ICs 17–19 with the base address stored in ICs 20–22. Also, the Hex display option gets the pulse, so the latch on the option latches in the data only when the base address (from ICs 20–22) is valid. Now similarly, when S17 is operated, the base address in ICs 20–22 change, and so the starting point from which the scope displays its 64, 32 or 16 bytes is changed. In this way, the whole memory can be scanned up and down in segments of 64, 32 or 16 bytes.

POWER SUPPLY

The power supply is conventional, using 3-terminal regulators. Although the ±12V has not yet been made use of, it is used for the CMOS input option, and the scope display option. The transformer supplying the +5V must have a rating of at least 2A, as the total current consumption of the complete unit exceeds 1A.

COMPONENTS

Full constructional details of the basic unit will be given in the next issue; however, a comment on the components is necessary. The Schottky TTL must not be replaced by LS TTL, otherwise the 5MHz specification will not be achieved. Double-sided p.c.b.s have had to be used, but do not have to be through-hole plated. Since it is not wise to solder i.c.s direct to the p.c.b., it is recommended that Soldercon i.c. socket strips are used. These allow soldering on both sides of the p.c.b. and are cost effective. The alternative is to use wire-wrap sockets, to allow the sockets to stand proud of the p.c.b., so that the pins can be soldered both sides where necessary. The prototype was built using Soldercon strips, and these worked well, while providing a neat solution.

Patents Review

Copies of Patents can be obtained from:
the Patents Office Sales, St. Mary Cray, Orpington, Kent. Price £1.60 each.

INFRA-RED HELMET LINK

Motor cyclists and their pillion passengers have a problem with communication, largely because British law (very reasonably) compels them to wear crash helmets. The obvious solution is a radio link. But if the legal CB wavelengths are used the link is likely to be useless, especially in city areas, because these frequencies are now so cluttered and blitzed by illegal high-powered transmitters, that normal use is impractical.

David Thompson of London W8 and Nicholas Hobson of SW3 have filed a British patent application (2 103 043) on an alternative approach. They suggest using an infra-red transmitter and receiver system built into the crash helmets. This seems a sensible approach, because the distance between rider and passenger is small, and their front-back positioning is fixed. The system can be modified, however, for sideways use with a side car.

Fig. 1 shows two helmets, each with microphone 3 and headphones 4 inside. L.e.d. 5 serves as an infra-red emitter and photo diode 6 as a receiver, on the front, rear and/or side of the helmet as necessary.

Inside each helmet there is an infra-red transceiver, shown schematically in Fig. 2. Speech picked up by microphone 14 is amplified at 15 and split into two paths. One path triggers threshold switch 16 and the other controls AGC circuit 17. The controlled signal is limited at 18 and band-pass filtered at 19 to around 300–330Hz. The processed signal is then fed to one input of Pulse Width Modulator 20, while the other input receives a triangle carrier generated by oscillator 21 at around 20kHz. The pulse width modulated output is converted to Pulse Position Modulation by circuit 22. The inventors say PPM allows average transmitted power to be greatly reduced.

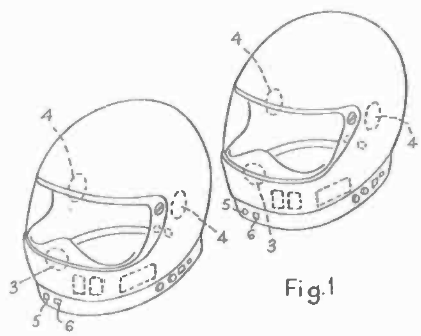
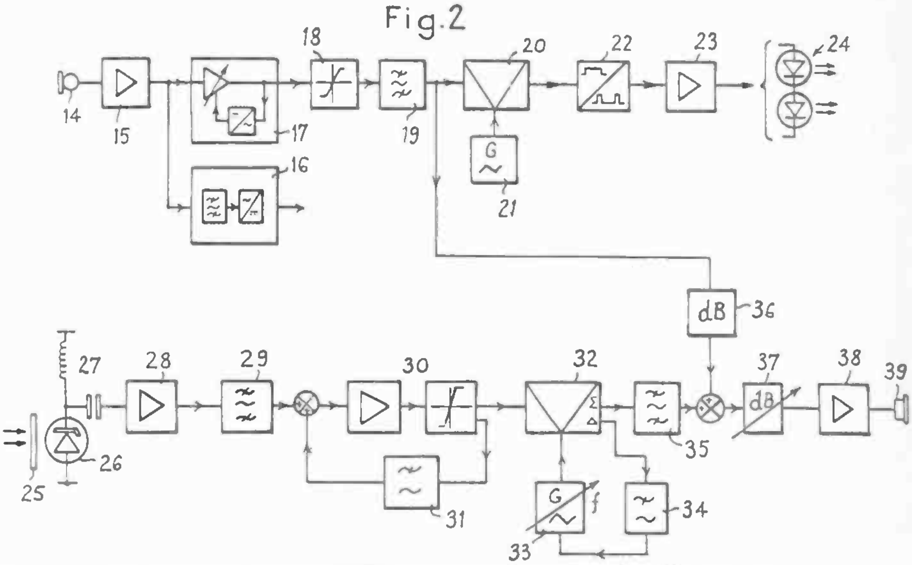


Fig.1

The pulse train is applied via amplifier 23 to l.e.d. 24, operated on a 940nm wavelength (eg Siemens type LD 241).

In the receiver photo diode 26 (type BPW 34, for instance) outputs to LC filter 27, so that d.c. and low frequency components are shunted to earth. The wanted HF signal is amplified at 28 and band limited at 29 to optimize signal-to-noise ratio at the input of amplifier 30. This outputs a pulse train similar to that produced at converter 22 in the transmitter. Demodulator 32 uses the pulse train to sample a triangle wave locally generated by oscillator 33, phase locked to the transmitter oscillator. Both the positive and negative slopes of the triangle are sampled. The difference between the samples corresponds to the phase error between the two oscillators and is used to control the oscillator 33 to close the phase locked loop. The sum voltage of the samples is the audio signal which is band-pass filtered at 35, amplified at 38 and fed to earphone loudspeaker 39.

Fig.2



DOUBLE-CARRIER STEREO TV

There is currently a move in Germany to protect the native TV manufacturers from foreign competition, by the use of a patented stereo sound system. For the last sixteen years Europe has been able to limit the number and type of colour sets made by Far Eastern firms, both in the Far East and in Europe, by clever use of the Telefunken patents on the PAL signal coding system. But now the PAL patents are running out and in Germany IGR (Interessengemeinschaft fur Rundfunkschutzrechte GmbH) is hoping to do the same with a folio of patents on the double-carrier system now being used to transmit stereo sound with some TV programmes in West Germany. This is one very good reason why the Germans adopted a very different approach to that used in Japan.

In that country the two channels of sound are multiplexed on a single carrier, whereas in Germany they are transmitted on two separate carriers. Unfortunately the German patents on stereo TV sound are likely to prove far weaker than the PAL patents, for the simple reason that there is nothing new in twin carrier transmission. IGR's only hope is to patent details of the system.

European patent application 0 069 864 is an example of what looks increasingly like a doomed attempt at fending off foreign competition. The patent application, in the name of IGR, has been filed in all the major European countries, including Britain. This is an expensive tactic but the application covers only a trivial circuit detail.

Even if IGR can persuade the European Patent Office that such a simple idea is new, and worthy of a patent, it is hard to see how it can be used to ward off the Japanese competition.

Deglitching Techniques

L.N. Owen B.Sc.

TO most hobbyists the function or even existence of a Deglitcher is somewhat obscure. However, with the increasing interest generated in these pages over recent years concerning microprocessor interfacing, particularly in digital to analogue conversion, a number of experimenters may well have been 'glitched' without being fully aware of their situation, the results being curious logic spikes and consequently distortion of the desired output.

THE GLITCH DEFINED

A glitch is a transient spike which occurs at the output of any DAC (digital to analogue converter) when the input code is changed. All DACs suffer from glitching. The transients are due to the finite, variable times taken for digital signals to drive analogue switches. These variations are caused by small imperfections introduced to the integrated circuit during fabrication, hence stored charge, or gate to drain capacity, is inconsistent. The resultant effect is that both digital and analogue switches turn on and off at different rates at different times. Consequently a series of states is experienced when the input, and hence the output, is changed.

This behaviour is most pronounced when small changes occur about the most significant bit (MSB). To illustrate this point consider the incrementing of data from 127_{10} to 128_{10}; in binary form this corresponds to a transfer of 01111111_2 to 10000000_2; in other words a complete change of state is required for each logic input. If this is analysed further the DAC must switch the MSB on and switch off the other lesser seven bits in order to synthesise the corresponding analogue voltage. However these switches of logic level do not occur simultaneously and thus for a small space of time there are many possible input values. The two worst cases are 11111111_2 (the MSB switches on while the lesser bits are still on) and 00000000_2 (the lesser bits turn off prior to the MSB turning on). Both of these cases are shown in Fig. 1.

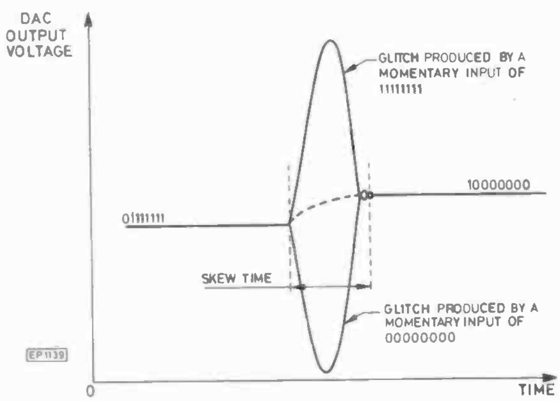


Fig. 1. Glitch effects

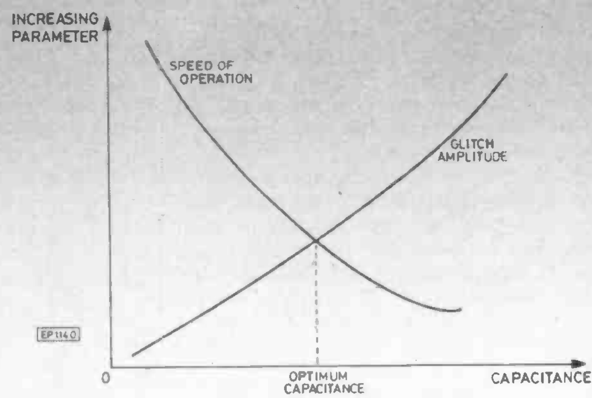


Fig. 2. Effect of damping

DEGLITCHING

The immediate concern is the various methods of glitch elimination. The first point to make is that complete deglitching is only possible by over-damping the system. In most cases this is possible but wholly undesirable due to the sluggish response. However the principle of damping is a useful one and is commonplace in comparatively slower systems.

In its simplest form a capacitor strapped across the DAC's output acts as a reservoir for smoothing purposes. The choice of capacitance depends on a compromise between response time and glitch amplitude. Unfortunately these two parameters work against each other and hence alternative methods are necessary for higher speeds (Fig. 2).

One such method is to load all the logic bits into a storage register before updating the DAC. In this way the skew time of the digital drive circuitry is reduced simply by ensuring

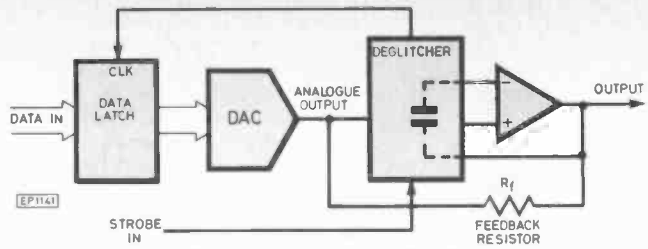


Fig. 3. Switched feedback Deglitcher

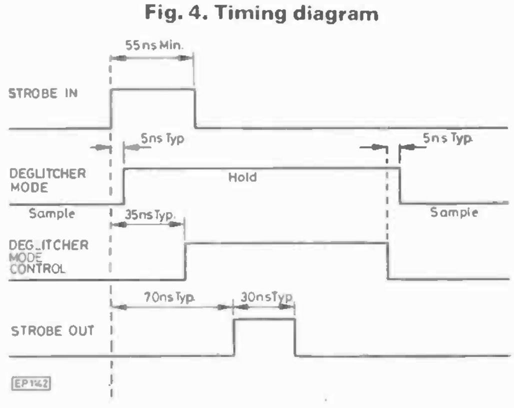
that all the data bits are input at the same time. However the output stages are still prone to fabrication problems as mentioned earlier. Another problem with the storage register system is that significant propagation delay times are added to the signal processing and this hinders fast operation.

This leads to the third, and most efficient, method of reducing glitches: a Deglitcher. In making this statement it must be noted that glitches cannot be eliminated, only reduced. A Deglitcher is a switched feedback element, and as such a device it must be included in the feedback loop of an operational amplifier used at the output stage of the DAC. They are essentially analogue devices with some clock functions, closely related to sample and hold amplifiers. The principle of a Deglitcher circuit is to isolate a DAC glitch and substitute its own small glitch. This latter glitch comes from charge dumping on the Deglitcher hold capacitor during transitions from sample to hold and hold to sample. Since this is independent of the DAC, changes in the digital input codes will have no bearing on the glitch size. Therefore the glitch is small and constant.

Implementation of a Deglitcher is shown in the block diagram of a DAC system in Fig. 3. The timing of the circuit is given in Fig. 4. Here, when the external storage registers are full a pulse, 'Strobe In', is applied to the Deglitcher. The rising edge of this pulse places the Deglitcher into its hold mode and then triggers an internal mode control gate pulse. At a small but specified time after the 'Strobe In' pulse has been received, a 'Strobe Out' pulse is generated. This allows data to be transmitted from the storage registers to update the DAC. After the DAC has assumed its new data level the falling edge of the Deglitcher mode control switches the mode from hold to sample and hence reconnects the DAC output to the amplifier, which quickly assumes its new value. Obviously a sufficiently fast op-amp must be used.

Minimising glitches in this manner results in an essentially linear analogue representation of a digital input. This is extremely important in applications such as cathode ray tube display driving where large high speed transients are integrated over a number of microseconds thus affecting accuracy, lengthening system settling time and creating distortion.

Fig. 4. Timing diagram



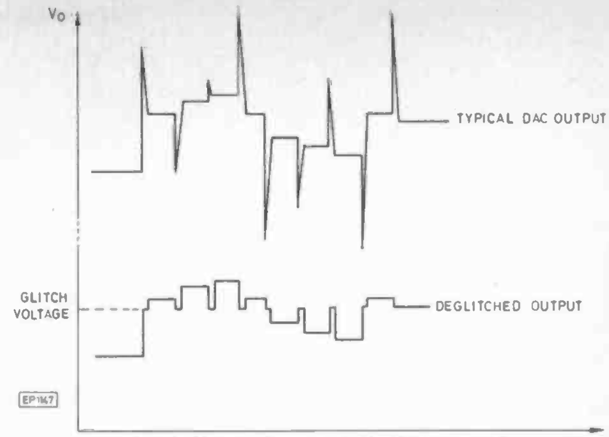


Fig. 6. Normal and deglitched output

PRACTICAL SYSTEM

Such a system is realised in Fig. 5. In this particular example the DAC is an 8 bit device, but it could be of any resolution. The particular Deglitcher is the Teledyne Philbrick 4902 which is a high reliability hybrid module. This device requires an f.e.t. op-amp and hence an LF 351 is used. The Deglitcher has three externally controllable variables. The 'Jump Trim' determines the voltage of the hold signal and the 'EOS Trim' is the offset voltage compensation for the device.

Other features of the circuit are the clamped output of the DAC using two Schottky diodes, the debounce of the strobe input and the feedback resistor R_f. The diodes prevent damage due to over voltage, and glitches, by supplying a low resistance path to ground. The debounce network consists of low value components in order to attain a reasonably fast, clean edge for the Deglitcher to trigger from; situations such as these always call for a compromise between speed and effectiveness. The feedback resistor R_f is one of the major components in the circuit. During the sample mode the constant glitch is generated. The amplitude of the glitch is a function of the DAC output current and the feedback resistor. Hence, during the sample mode $V_0 = -I_0R_f$. The output becomes that of Fig. 6. Pin 11 is the strobe o/p which enables the data latches to update their registers.

Typical applications where this sort of circuit is employed are CRT display systems, fast process controllers, camp generators, automatic test equipment and symbol recognition devices. ★

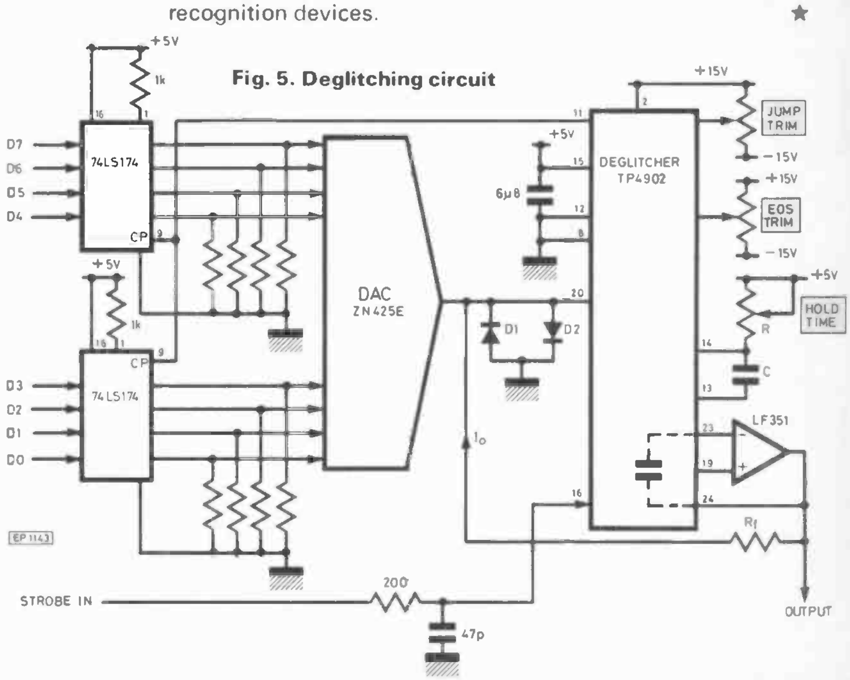


Fig. 5. Deglitching circuit

MICRO PROMPT

The hardware and software exchange point for PE computer projects

Increasing RAM to 3K

Sir—The available user-RAM on the PE Microcontroller is 1K bytes. More complex control programs become restricted due to lack of user-RAM. The circuit described increases this memory by 2K bytes whilst retaining:

a) battery backup facility

b) "DISBUG" monitor facilities

with the minimum of p.c.b. modifications, and at very low cost.

The RAM chip used is the Hitachi HM6116LP-3. Being pin compatible with the 2516 EPROM, it will plug into the spare 24-pin socket (for IC26) on the Microcontroller. As with the DISBUG EPROM (IC3) the use of an additional low profile socket is required with pins 18, 20, 21 and 24 being bent out before insertion, allowing access for modifications. The p.c.b. wiring of address and data lines are compatible. Modifications are however required for the control signals—p.c.b. modifications being:

1) cut track between IC24 pin 4 and IC25 pin 1

2) cut track to IC7 pin 3 (near IC7) and join the now isolated track to IC7 pin 4

3) carefully lift IC7 pin 1 (to allow access to this pin only, for wiring)

Additional wiring required is as shown on the circuit diagram. The 74L500 chip (IC27) can be sited above IC10 (spare socket) on the Microcontroller or on adjacent Veroboard. All wiring connections can be made on top of the p.c.b. wire as follows (6116 chip removed):

1) 74LS00 interconnections, power supply, ground

2) IC25 pin 6 to IC26 pin 21

3) Join IC26 pins 18 and 20, wire to IC7 pin 3

4) IC27 pins 12, 13 to IC6 pins 13, 14 respectively

5) IC27 pin 2 to BUS Ø2

6) IC27 pin 4 to IC6 pin 15

7) IC27 pin 6 to IC24 pin 4

8) IC27 pin 3 to IC7 pin 1 (i.c. pin only)

9) IC26 pin 24 to VRAM

10) Connect 3k3 resistor from IC7 pin 1 to +Vcc

IC6 (address decoder) output Y1 is enabled for a valid memory address between ØØØØ and Ø3FF, generating a chip select for the 1K RAM (IC8, 9). The additional 2K RAM is located at addresses Ø4ØØ to ØBFF, utilising the outputs Y2 and Y3 of IC6. If either of these outputs is true, IC27 pin 11 goes high. This enables IC27 pin 1, which is phased with BUS Ø2 clock, to generate chip select to IC26, provided the +5 volt power supply rail is held.

The Microcontroller uses a clock stretching input to IC1 (clock generator) whenever any address in RAM is assessed. For compatibility of software timing this is used in the modified circuit. IC27 gates provide a preset to IC24 (dual D type flip-flop) whenever any of IC6 outputs Y1, Y2 or Y3 are true. This enables the clock and D inputs to generate: i) memory ready to IC1 pin 6; ii) enable to the other flip-flop (IC24).

This second flip-flop (IC24) generating the "write enable" signal to IC25 pin 5, enabling this gate to provide a read or write signal to all of the RAMs.

Memory standby/supply power is taken from the supply (VRAM) and Use of the HM 6116 LP RAM device ensures low power consumption. This device has a standby power of 20 microwatts (typical), ensuring the Microcontroller will still retain memory data for many months, when not used—a prime requirement.

The memory map shows the user locations of RAM. It must be remembered to avoid the area of DISBUG RAM when combining the existing 1K RAM and the additional 2K RAM in any software routine.

Before making any modifications to the Microcontroller p.c.b. it is essential the wiring of IC25 is examined. The gates used within this package may differ from the circuit diagram supplied with the Microcontroller. Modification details refer to IC25 pin/gates as on my Microcontroller p.c.b. Use a low-profile 24-pin d.i.l. socket for IC26.

S. Marke,
Towcester.

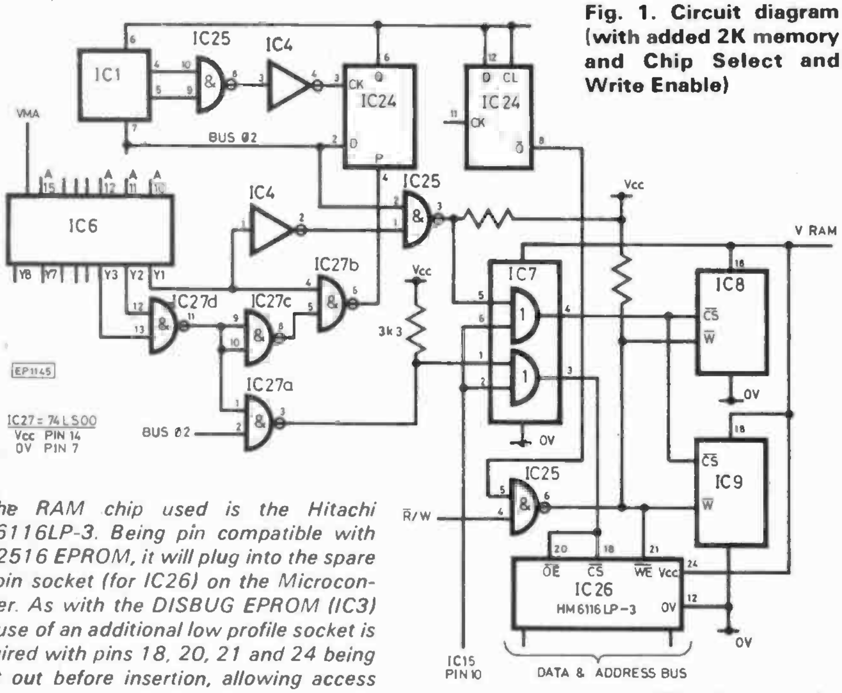


Fig. 1. Circuit diagram (with added 2K memory and Chip Select and Write Enable)

Table 1. Memory map

DISBUG MONITOR	FFFF
	F800
KEYBOARD P.I.A.	1C00 → 1C03
DISPLAY P.I.A.	1800 → 1803
USER P.I.A.	1400 → 1403
USER P.I.A.	1000 → 1003
	0BFF (0BFF)
ADDITIONAL 2K RAM (USER)	07FF
	0400
DISBUG RAM (USER STACK)	
RAM (USER)	0000

QUADRUPLES

*Sir—The adjacent M/C subroutines effectively **quadruples** the screen resolution of the UK101 with **no** hardware mods.*

It does this by dividing each character slot on the screen into 4 (see below).

1	**2**
4	**8**

EP1137

The routines decide which quarter to light, which quarters are already lit, then displays the appropriate "chunky" graphics block in the slot. This gives a resolution of 92 × 62 on my system.

The routines supplied allow either very fast point or line drawing in white or black (plot or unplot). They may be called from BASIC with USR( ) or in M/C programs by JSR XXXX.

To use the routines as supplied:
POKE $F0 with X0-co-ordinate
POKE $F1 with Y0-co-ordinate
POKE $F9 with X1-co-ordinate
POKE $FA with Y1-co-ordinate
POKE $F2—00 for black (unplot)
not 00 for white (plot)

***THEN** JSR $1EB1 to plot the point (X0, Y0)*

OR

JSR $1F33 to plot the line (X0, Y0) to (X1, Y1) at the same resolution.

Both drawing routines are very fast and although not quite the 279 × 192 of an Apple II they do give a creditable performance on the graphics programs written for the Apple.

Other 6502 systems can use the same routines if they have chunky graphics available (e.g. Tangerine). The codes for the graphics blocks for that system are then put in place of BLOCKS at $1EA1 of the routines and then everything else will work.

Steven Lomas,
Bath.

```
$1E9D          PIXELS 01           This is the binary
                      02           for each of the
                      04           quarter pixels.
                      08
$1EA1          BLOCKS 20  empty    This is the
                      A8           data giving the
                      A6           "chunky" graphics
                      9B           characters which
                      A7           fill in appropriate
                      9C           quarters of the
                      AA           block, according
                      AF           to which of
                      A5           the "pixels" (quarters)
                      A9           are lit.
                      9D
                      B1
                      9A
                      B2
                      B0
                      A1    full (all lit)
$1EB1  A9 CD   POINT  LDA #$CD     Set the top of
       85 F4          STA VDU      the screen in
       A9 CF          LDA #$CF     VDU, VDUHY
       85 F5          STA VDUHY    (must be consecutive)
       A5 F0          LDA XX       get the double X-co-ordinate
       4A             LSR A        and divide by 2
       85 F7          STA XP       store actual X co-ordinate
       0A             ASL A        multiply up again
       85 F3          STA TEMP     save it
       38             SEC          and now
       A5 F0          LDA XX       QUART = XX - INT (XX)
       E5 F3          SBC TEMP     to find which
       85 F6          STA QUART    quarter of
       A5 F1          LDA YY       the block is
       4A             LSR A        referred to,
       85 F8          STA YP       .·. use
       0A             ASL A        QUART as a pointer
       85 F3          STA TEMP     to the table
       38             SEC          PIXELS (above)
       A5 F1          LDA YY
       E5 F3          SBC TEMP     QUART = (YY - INT(YY))*2
       0A             ASL A                + (XX - INT(XX))
       18             CLC          (i.e.) which quarter?
       65 F6          ADC QUART    01, 02, 04, 08
       85 F6          STA QUART    | 01 | 02 |
                                   | 04 | 08 |
       A6 F8          LDX YP       actual Y pointer
       18      B2     CLC
       A5 F4          LDA VDU      load VDU address (low)
       69 40          ADC #$40     add a line
       85 F4          STA VDU
       90 02          BCC B1
       E6 F5          INC VDUHY
       CA      B1     DEX          decrement pointer
       10 F2          BPL B2       if not done go back
       18             CLC          now add
       A5 F4          LDA VDU      on the X value
       65 F7          ADC XP
       85 F4          STA VDU      and store the
       90 02          BCC B3       screen location of
       E6 F5          INC VDUHY    the block referred to
       A0 00   B3     LDY #$00     in VDU/VDUHY
       B1 F4          LDA (VDU), Y load the character
       A2 0F          LDX #$0F     on the screen already
       DD A1 1E B6    CMP BLOCKS, X identify the block.
       D0 05          BNE B4       if not equal then
       86 F3          STX CHAR     jump over this
       18             CLC          which saves the
       90 03          BCC B5       pointer
       CA      B4     DEX          go back to
       10 F3          BPL B6       identify character
       A6 F6   B5     LDX QUART    load the binary
       BD 9D 1E       LDA PIXELS, X of the quarter pixel
       85 F6          STA QUART    and save it in QUART
       25 F3          AND CHAR     and with what's there
       F0 0E          BEQ B7       already. Is it lit?
       A5 F2          LDA ZZ       if here then pixel
       F0 01          BEQ B8       required is lit
       60             RTS          ZZ is switch —
       A5 F3   B8     LDA CHAR     If ZZ = 0 then "unplot"
       38             SEC          ZZ ≠ 0 then plot
       E5 F6          SBC QUART    switch off pixel
       AA             TAX          save pointer
       4C 2D 1F       JMP PLOT     plot it
       A5 F2   B7     LDA ZZ       plot or unplot?
       D0 01          BNE B9
       60             RTS
       18      B9     CLC          add pixel to CHAR
       A5 F3          LDA CHAR     to switch pixel on
       65 F6          ADC QUART
       AA             TAX          save pointer
       BD A1 1E PLOT  LDA BLOCK, X and plot it.
       91 F4          STA (VDU), Y
       60             RTS
$1F33  A5 F9   LINE   LDA X1       joins points
       C5 F0          CMP X0       (X0, Y0)(X1, Y1)
       B0 12          BCS B1A      with a straight
       48             PHA          line either black
       A5 F0          LDA X0       (ZZ = 0) or white
       85 F9          STA X1       (ZZ ≠ 0)
       68             PLA          uses point at $1EB1
       85 F0          STA X0
       A5 F1          LDA Y0
```

48		PHA	85 F9		STA Z5	A5 F0	B9A	LDA X0	85 FD		STA Z3
A5 FA		LDA Y1	85 FA		STA Z6	18		CLC	A5 F0		LDA X0
85 F1		STA Y0	A9 01		LDA #$01	65 FE		ADC Z4	18		CLC
68		PLA	85 FE		STA Z4	85 F0		STA X0	65 FA		ADC Z6
85 FA		STA Y1	85 FF		STA Z7	A5 FD		LDA Z3	85 F0		STA X0
20 B1 1E	B1A	JSR POINT	A5 FB		LDA Z1	18		CLC	A5 EF		LDA FLAG
A5 F9		LDA X1	C5 FC		CMP Z2	65 FC		ADC Z2	C9 01		CMP #$01
38		SEC	B0 1A		BCS B4A	85 FD		STA Z3	90 09		BCC B8A
E5 F0		SBC X0	48		PHA	A5 EF		LDA FLAG	A5 F1		LDA Y0
85 FB		STA Z1	A5 FC		LDA Z2	C9 03		CMP #$03	38		SEC
A5 FA		LDA Y1	85 FB		STA Z1	B0 09		BCS B5A	E5 FF		SBC Z7
C5 F1		CMP Y0	68		PLA	A5 F1		LDA Y0	85 F1		STA Y0
B0 0D		BCS B2A	85 FC		STA Z2	18		CLC	B0 07		BCS B7A
A9 01		LDA #$01	A5 FE		LDA Z4	65 F9		ADC Z5	A5 F1	B8A	LDA Y0
85 EF		STA FLAG	85 FA		STA Z6	85 F1		STA Y0	18		CLC
A5 F1		LDA Y0	A5 FF		LDA Z7	90 07		BCC B6A	65 FF		ADC Z7
38		SEC	85 F9		STA Z5	A5 F1	B5A	LDA Y0	85 F1		STA Y0
E5 FA		SBC Y1	E6 EF		INC FLAG	38		SEC	8A	B7A	TXA
85 FC		STA Z2	E6 EF		INC FLAG	E5 F9		SBC Z5	48		PHA
B0 09		BCS B3A	A9 00		LDA #$00	85 F1		STA Y0	20 B1 1E		JSR POINT
38	B2A	SEC	85 FE		STA Z4	A5 FB	B6A	LDA Z1	68		PLA
E5 F1		SBC Y0	85 FF		STA Z7	C5 FD		CMP Z3	AA		TAX
85 FC		STA Z2	A5 FB	B4A	LDA Z1	B0 24		BCS B7A	E8		INX
A9 00		LDA #$00	85 FD		STA Z3	A5 FD		LDA Z3	E4 FB		CPX Z1
85 EF		STA FLAG	46 FD		LSR Z3	38		SEC	90 A6		BCC B9A
A9 00	B3A	LDA #$00	A2 00		LDX #$00	E5 FB		SBC Z1	60		RTS

MICROCONTROLLER CLOCK

Many people have noticed that the Microcontroller clock is not accurate and typically loses 10 to 20 secs every 24 hours. David Whitfield, a co-author of the project, has investigated this problem and encountered difficulty in tracing a missing second every 5 to 10 minutes. In the end he used a BBC micro programmed as a rather crude logic analyser to monitor the 1 Hz clock and compare it with the internal clock on the BBC machine. This, in conjunction with the test program published in the December copy of PE, showed the following:

1. The 1Hz clock does not "swallow" whole seconds due to the circuitry associated with IC2. This would have been a convenient solution.
2. The accuracy of the Microcontroller's 1Hz clock is better than that of the BBC micro's system clock over a long period. This is probably due to the higher interrupt load on the BBC's CPU and its dependence on the CPU clock for timing.
3. The internal DISBUG clock *does* lose count at a long term rate of around 1 in 400. The loss is in the form of a random "missed" second, which seems to occur at random intervals.

These observations confirm the behaviour of the unit can be repeated, and is therefore probably shown by all units. To try and examine the problem further, David ran the program listed. This sets up an alternative count to TICK (which he called TOCK!) at RAM location Ø3C1. TOCK is driven by the IRQ interrupt handler which already manages the 1Hz count in TICK; the modification to the interrupt handler starts at address ØØ32, and is added by the first two instructions (see the data sheet in May PE). The TOCK count uses a spare space in DISBUG RAM to set up the clock.

The main difference between TICK and TOCK is that TICK only updates the count when an interrupt has occurred AND the B-side of PIA IC12 shows that it was caused by the 1Hz clock. TOCK, however, is updated whenever an interrupt occurs. Since there is only one interrupt set up by DISBUG (the 1Hz clock), the results from TICK and TOCK should be the same. If anything, TOCK might be expected to gain on TICK due to the effects of spurious noise-induced interrupts; TICK does a check on the PIA status to avoid this problem. The test program, when run from ØØØØ, and compared with a "real" clock, allows the two counts to be displayed simultaneously. The full TICK count is shown in the address area of the display, while only the two least significant digits of TOCK are shown in the data area. After a few hours of running, watching and comparing, it is evident that TICK loses counts, but that TOCK does not appear to gain any.

Further tests show that the problem is that the 1Hz interrupt is sometimes not reflected in the control register of PIA IC12. As to why this might be so, David is still investigating. In the meantime he has developed a short "fix" to allow TOCK to be used in place of TICK; just use Ø3C1/2 in place of Ø3E2/3. The "fix" should be included in the initialisation code of any program (remembering to set the address shown accordingly), just before the main loop. DISBUG will initialise TOCK in the same way as TICK, setting it to ØØØØ at power-up or restart.

Table 2. Real time clock test program

Address (Hex)	Label	Instruction Mnemonic		Op Code		
ØØØØ	START:	LDX	#ALTINT	CE	ØØ	32
ØØØ3		STX	IRQSRA	FF	Ø3	DC
ØØØ6		LDX	#$ØØØØ	CE	ØØ	ØØ
ØØØ9		STX	TICK	FF	Ø3	E2
ØØØC		STX	TOCK	FF	Ø3	C1
ØØØF		LDA	#$15	86	15	
ØØ11		JSR	PROMPT	BD	F9	BD
ØØ14	AGAIN:	LDX	#ADDDIS	CE	Ø3	FB
ØØ17		LDA	A (TICK + 1)	B6	Ø3	E3
ØØ1A		JSR	TWODIG	BD	F8	F7
ØØ1D		LDA	A TICK	B6	Ø3	E2
ØØ2Ø		JSR	TWODIG	BD	F8	F7
ØØ23		LDX	#DATADIS	CE	Ø3	F8
ØØ26		LDA	A (TOCK + 1)	B6	Ø3	C2
ØØ29		JSR	TWODIG	BD	F8	F7
ØØ2C		JSR	DISPLAY	BD	F8	14
ØØ2F		JMP	AGAIN	7E	ØØ	14
ØØ32	ALTINT:	LDX	TOCK	FE	Ø3	C1
ØØ35		INX		Ø8		
ØØ36		STX	TOCK	FF	Ø3	C1
ØØ39		RTI		3B		

Table 1. Software fix for the real time clock: setting up 'TOCK'. Include this code at the start of a user program which wants to use TOCK, which is located at Ø3C1/2, instead of TICK (which is located at Ø3E2/3)

LDX	#ALTINT	CE	Put address where code below starts (e.g. Ø3 8Ø) in these two bytes
STX	IRQSRA	FF	Ø3 DC

Include this code IN ADDITION to that above at any convenient position in RAM which is unused (suggestion is to locate it at location Ø38Ø)

ALTINT:	LDX	TOCK	FE	Ø3	C1
	INX		Ø8		
	STX	TOCK	FF	Ø3	C1
	RTI		3B		

If an addition to the IRQ interrupt handler is already made by the program, omit the first patch (since the program must already contain an equivalent), and add the first 3 instructions only of the last patch to the new interrupt handler. The reason is that only one additional handler may be defined.

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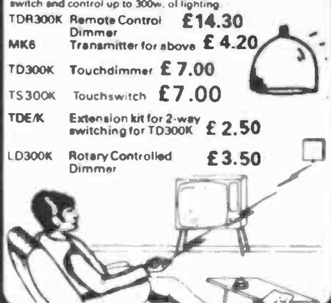

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MM74C926	4 50
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NE567	.97
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SAB0600	2 50
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TMS1601	10 00
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TL062	60
TL064	98
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TL072	.50
TL074	96
TL081	25
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15	35
7905	80
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LM338K	4 60
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4000	11
4001	11
4002	11
4007	12
4011	11
4012	12
4013	20
4015	.39
4016	20
4017	29
4019	24
4023	15
4025	15
4026	72
4027	.20
4028	38
4040	39
4043	.38
4046	46
4049	21
4050	21
4060	.42
4069	13
4070	13
4071	13
4077	16
4081	12
4093	20
4501	24
4511	155
4514	1 15

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This new design is based on the ICL7126 (a lower power version of the ICL7106 chip) and a 3½ digit liquid crystal display. This kit will form the basis of a digital multimeter (only a few additional resistors and switches are required—details supplied), or a sensitive digital thermometer (−50°C to +150°C) reading to 0.1°C. The basic kit has a sensitivity of 200mV for a full scale reading, automatic polarity indication and an ultra low power requirement—giving a 2 year typical battery life from a standard 9V PP3 when used 8 hours a day, 7 days a week

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Strictly

by K. Lenton-Smith

GLENN MILLER

Students of light music will be familiar with the problem that faced Glenn Miller 45 years ago. He was searching for a particular sound that would set his band apart from others—and inadvertently found his answer through a mishap to his lead trumpet. The player concerned had split his lip and the trumpet part had to be taken by the clarinet (both instruments being pitched in B♭, the same music could be used).

In fact, Miller re-arranged his parts to suit this event and the resulting blend of *soli* saxes and clarinet produced a sound unmistakable today.

I feel sure that modern combo groups have that same problem—how to sound different from the rest. In the Miller era, pure musicianship was the only method: if the mains supply failed, only the announcer's microphone was affected. Today, complete failure of the electronics would bring most music to an abrupt halt, and render vocalists inaudible!

Electronic effects, especially those used in recording studios, are limitless in popular music today, and it is a moot point whether the standard of musicianship has fallen as a direct result. Combo groups look carefully at the equipment they buy and how to make the most of it. In this article we will look at what the world's largest manufacturer, Yamaha, has to offer.

COMBO

As the electric guitar is the mainstay of the group, it ought to be dealt with before other instruments. Yamaha has introduced new instruments recently, many of them featuring 'through-neck' design: in this case the neck extends right through the body of the instrument to its heel, giving more uniform transmission of string vibration to the pick-up. The SG series and SF series have solid bodies with humbucking coils. The SC series use a single coil. SA series guitars are semi-acoustic with single coil/humbucking and have exceptional tonal ability. AE series are acoustic and provide that warm and intimate sound for contemporary jazz. Among these, the hard-rock musician would probably choose the SF series for its extensive distortion control and powerful Alnico-5 pick up magnets.

The new BB series of electric basses has been developed with the aid of leading performers. They offer full, balanced response with plenty of punch and definition.

A range of effectors that can be fitted in-line include phasing, chorus, flanger, octaver, distortion, tone booster, compressor, parametric EQ, limiter, noise gate and noise selector. When the inbuilt guitar controls are also taken into account, performers have ample scope for modifying waveforms from the pickup.

KEYBOARDS

Among Yamaha's pianos, one of the most interesting is Digital Keyboard GS1. This 88-key model looks like a small baby grand and features touch-response: up to 16 notes may be played simultaneously, 16 voices are available and it will read magnetic cards for voicing, vibrato may be applied and piano-type pedals control this, damper and tremolo are also featured. GS2 is a smaller, 73-key version with a similar specification.

Models CP-80 and CP-70B are 88 and 73-key acoustic pianos with amplification, the latter model being portable despite the metal frame carrying the strings. Both instruments allow the player to control timbre over three distinct parts of the keyboard compass, with variable tremolo depth and speed.

CP35 and CP25 are 73 and 61-key digital pianos with 16 note capacity in two pitches, decay, tremolo, flanger, filter and equaliser controls. The CP25 keyboard may be split, when each section then allows 8-note capacity.

A useful keyboard to use at home is the CP11. This is also digital (10 note polyphonic) but the keyboard can be split and 6 notes are then reserved for the chord section. Eight rhythm patterns are provided and these control the auto-accompaniment. The available tones are Piano 1, Piano 2 and Harpsichord. Sustain operates normally but the EG control allows decay only after the playing key has been released—producing organ-like tones. Tremolo is fitted and the instrument has an internal 5W speaker.

Yamaha's Symphonic Ensembles are best described as very comprehensive portable organs: they have one/two manuals with organ tone, solo synth, poly synth and string chorus etc. Optional 13 note pedalboards may be attached. This SK series is ideally suited to a skilled keyboard player in a group.

Synthesisers from Yamaha range from CS70M—a polyphonic programmable instrument with 61 keys and 12 VCOs—to the CS-5, a 3-octave monophonic keyboard with a single VCO.

PRODUCER SERIES

This idea from Yamaha should be very welcome to any neighbour of a practising pop enthusiast! The sound capabilities of stage and recording equipment have been compressed into a small and affordable system that can be used without disturbance to others. It is based on three units—MA10, MM10 and CS01.

MA10 is a headphone amplifier which will drive two sets of MH10 stereo phones and has a Monitor Out facility to feed other MA10s or a power amplifier. The input jack accepts signals from guitar or keyboard and input connections can also be made through Monitor In and Aux.

MM10 is a stereo Mic/Line mixer, each of the four channels having individual pan pots and level controls. CS01 is a $2\frac{1}{2}$-octave monophonic synthesiser with VCO, VCF, VCA and EG (Envelope Generator): a Breath Controller allows alteration of the VCO and VCF characteristics, leaving both hands free to use the keyboard and sliders. All three units run from mains adaptors providing 9–12 v.d.c. (Type PA-1).

By interconnecting these units, a group of instrumentalist/vocalists can hear the combined stereo output through headphones with total realism and clarity. Interconnections require some thought, though Yamaha can offer suggestions in this respect. The Producer Series should be a boon to practising musicians and neighbours alike as one word that appears to be synonymous with combo music is decibels!

AMPLIFIERS

These are comprehensive and fall into three categories. The JX series cover outputs from 20W to 50W into 8. . at 3% THD and have integral controls. G and B Mk II series handle from 50W to 100W into 8. . at 10% THD. Alternatively, stackable amplifiers can be supplied using G100II amplifier head or B100II head with one of the S Series speaker enclosures in conjunction: outputs up to 240W are available by this method. Different amplifiers are used for guitar and bass (indicated by codes G and B) because of the differences in tonal spectrum. New preamplifiers PG1 and PB1 (for bass) have recently been introduced.

Mixing consoles from Yamaha will accept up to 32 inputs, depending on the model concerned, with faders, equaliser, echo panpots and talkback. Analogue Delay Units E1010 and E1005, Graphic Equaliser Q1027, frequency Dividing Networks F1040 and F1030 are other items to interest groups. General speaker systems, individual drivers and horns are supplied for those that prefer to assemble to their own specification.

PERCUSSION

The company is well known for its orchestral instruments, including its System Drums. The YD-9000RA system includes two bass drums, snare drum, seven mounted toms, hi-hat and seven mounted cymbals of various sizes—surely enough for any drummer to be in his element? Certainly, Peter Erskine, Cozy Powell, Al Foster and Jim Keltner appear to be, as users of Yamaha percussion.

Individual drum units in any of 14 colour finishes are available. Shell and hardware sets, cymbal stands, snare drum stands, single and double tom stands, foot pedals, thrones, mutes and other hardware can be purchased singly to build up a user-defined system.

ORGANS

While looking at Yamaha's products, their highly reliable organs must be included, especially as the musical back-up—through the Yamaha Music School—is excellent: it is the world's largest teaching organisation. How it came into being and has helped 6 million people with a systematic approach to music is a long story, obtainable from Kemble (Organ Sales) Milton Keynes, the UK end of Nippon Gakki. I am sure that Len Rawle, Musical Director and a well-known organist, will be prepared to help.

The whole of the Yamaha organ family is based on the 'block-builder' principle where each time you move up the range you find all the previous features plus extra ones. All are based on PASS (Pulse Analogue Synthesis System), which produces a range of instrument sounds unobtainable until recently.

A and B series organs have two 37 or 44-note manuals, 13 pedals, presets and 12 auto rhythms. From B-55N upwards, organs are fitted with an arpeggiator and Variable Tone Levers. C series instruments have a roll-top fallboard to exclude dust (and small children's intrusion) when not in use. A doppler speaker is fitted from C55-N onwards.

Programmable Rhythm comes with the D series, also polyphonic synthesiser voices and multi-channel sound. Model DB5 has an extra 37 note manual with 12 synthesiser presets and can be coupled to upper or pedal.

Serious musicians will choose the E series for its full 5-octave manuals and 25-note pedalboard. Preset pistons allow instant change from baroque to cinema or entertainment organ.

Flagship of the organ range is the EX models, which are space age designs both in terms of the console (column mounted) and the electronics. PASS technology has been taken to its limits to produce a vast number of instrumental voices and sound effects. But you will need £50,000 to purchase the GX1!

Readout...

INMOS

Sir—Re the little note about INMOS in the April Industry Notebook.

Some of the things that Nexus says about INMOS may very well be true but don't forget that the company was messed around by the present government for political reasons. They were forced to set-up their factory in a place they didn't want and their second investment payment of some £50 million was delayed for several months whilst the government tried to wriggle out of the original contract.

In fact the original INMOS investment was made by the NEB and any loss to the taxpayer must be taken from the NEB books and not INMOS. Your view—sorry the view of Nexus that if a product is worthwhile then private capital will automatically be attracted to it is naive. How does he explain the problem Ferranti had when they wanted money for their ULA project. Not one merchant bank would look at them. In the end they went to the NEB and asked Tony Benn for £7 million. Obviously the NEB could smell success better than the banks. Later Thatcher sold those Ferranti shares on the open market for £54 million to the very people who refused the original investment. Could we possibly offset the losses that INMOS are making with the profits made on the Ferranti deal? Nexus should be criticising the government for killing off the NEB when it was doing a good job helping small business men (and large), creating jobs and making a profit as well. Does Nexus imagine that the Japanese stand back and let private enterprise do everything—their government hands out plenty of money for their banks to invest in industrial research and development—and where would the American electronics industry be without those big defence contracts?

And anyway what is £100 million? It represents just 4 or 5 weeks subsidy to the EEC agricultural fund for food that could be bought cheaper on the world market and is either destroyed or sold off cheaply to the Russians. Or it represents 3 months for the defence of those barren rocks in the South Atlantic, and that after an initial investment of some £2000 million.

The remarks about C&W were equally silly. C&W were making handsome profits during the whole time they were owned by the taxpayer. Selling them off was a political not economic decision.

Please keep us informed about what is happening in the industrial world with a more balanced view of the political and economic problems that have to be faced by governments and industries.

If any of the statements I have made in this letter are inaccurate then it is partly your fault for not keeping me better informed. I do not wish to offend but if I need puerile political views then I would subscribe to the Telegraph or the Mail—they do it so much better than your magazine.

John Hunt
UNDP
Rangoon
Burma.

Nexus comments:-

Inmos cannot be compared directly with Ferranti. The respective investments were different in kind, in quantity, in time and made for quite different reasons. It remains true that a worthwhile product or service attracts private capital. Indeed, as Mr Hunt points out, Ferranti had no difficulty in attracting £54 million once it became worthwhile. Similarly, Cable & Wireless, modestly profitable, was heavily oversubscribed when brought to the market. C&W's performance and profit can only now be fairly described as 'handsome'. The problem, as I am sure Mr Hunt would agree, is spotting the winners and although he may think £100 million is peanuts, by ordinary investment standards it is a large gamble on an outsider only just beginning, after four years, to show any form. The NEB's betting record has been no better than the average punter.

POSITIVE FEEDBACK

Sir—In response to your recent encouragement to readers to provide some feedback I am putting pen to paper.

I have subscribed regularly to your magazine for many years, am aged 32 and my interest in electronics is through hobby only. I often buy the odd issue of your competitors' magazines to see what's available and find I prefer your magazine for the following reasons:

The projects are presented clearly, are detailed and complete.

The content on the whole is what I want.

The style avoids the chatty slightly flippant style evident in at least one competitor.

Now some criticisms:-

Why terminate "Semiconductor Update", I certainly appreciated the feature.

I'm afraid this new feature 'Vernon Trent' just leaves me cold. I buy your magazine for information, not the sort of article common in the daily press.

My PE Micro-controller does not keep good time. The internal clock in the monitor loses approximately 1 second every 300 seconds or so. Is the crystal at fault or is there a bug in the monitor? I know I can allow for this in my own software but I may be short of space for this. I enclose s.a.e.

Colin A. Kerr
Edinburgh.

Thank you for all your comments; we are always pleased to receive them. The only other comments we have had regarding VT have been in favour—more views welcome! Regarding Semiconductor Update this was replaced by Semiconductor Circuits, which not only introduces a new chip each month but provides data plus a working circuit and layout. We have also added Silicon News Corner to News and Market Place, thus providing information on a range of new chips as they are announced. Our intention was to cover this area more fully and show how to use the chips that are now available.

Your query on the Micro-controller is answered in Microprompt.

Ingenuity Unlimited

A selection of readers' original circuit ideas.

Why not submit *your* idea? Any idea published will be awarded payment according to its merits.

Each idea submitted must be accompanied by a declaration to the effect that it has been tried and tested, is the original work of the undersigned, and that it has not been offered or accepted for publication elsewhere. It should be emphasised that these designs have not been proven by us. They will at any rate stimulate further thought.

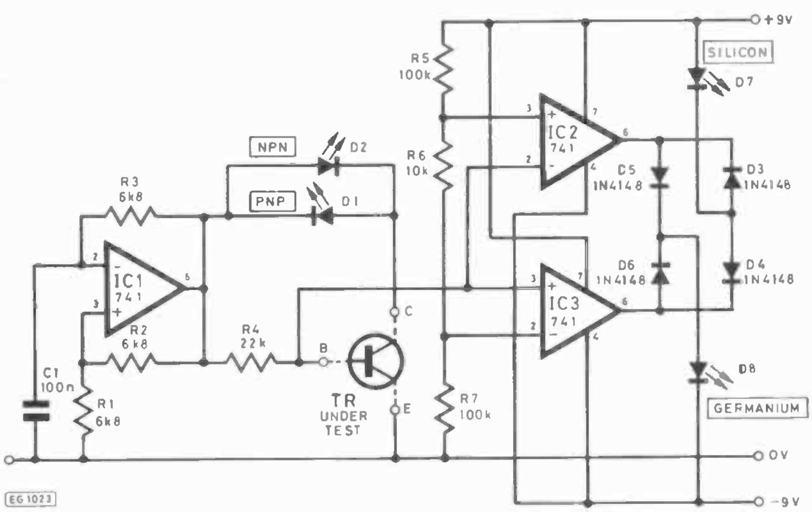
Articles submitted for publication should conform to the usual practices of this journal, e.g. with regard to abbreviations and circuit symbols. Diagrams should be on separate sheets, not in the text.

TRANSISTOR ANALYSER

THIS unit was designed and built to help with the sorting out of large bags of untested transistors. It indicates whether the transistor under test is:

1) Functional/non-functional
2) npn/pnp
3) Germanium/silicon.

IC1 and associated components forms a conventional astable multivibrator, the output of which drives the collector and base (through R4) of TR1, the transistor under test, alternately positive and negative with respect to ground. If the transistor is of the pnp type, negative pulses will drive it into conduction so lighting indicator D1; if it is npn D2 will be lit (a faulty transistor will either light both lights or neither).



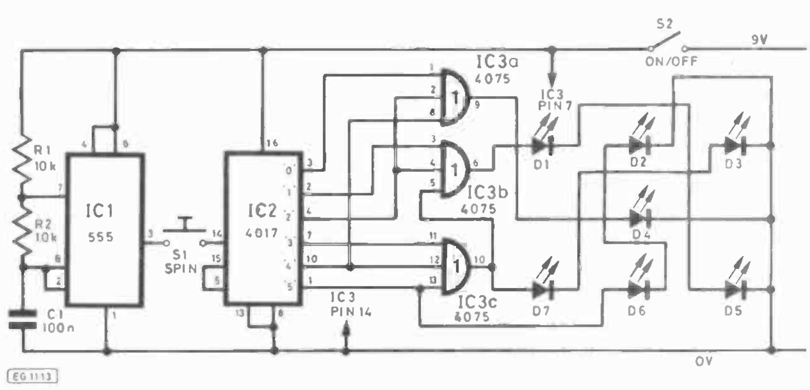
Simultaneously, the base voltage of the transistor (which will be varying between ground and Vbe) is fed to window detector IC2/3 and associated components, which gives a high output in the range ±4V. A high output will light D8 indicating a germanium transistor whilst a low output will light D7 indicating a silicon transistor. D3–D6 can be any medium power diodes which come to hand, whilst the output is more legible if different colour diodes are used for D1 and D2, and for D3 and D4.

S. D. Draper,
Sudbrooke,
Lincoln.

ELECTRONIC DIE

THIS circuit is for an electronic die. When the 'spin' button (S1) is pressed then released the l.e.d. display shows a random number between 1 and 6, arranged in the standard die format.

The 555 (IC1) is in the astable mode running at 1kHz. When S1 is pressed pulses are fed into the 4017 (IC2) decade counter, this sends a pulse out of each of the nine outputs in turn. The sixth pin is connected to the reset pin (15) so that it counts up to 6 then resets. When S1 is released the counter will stop at one output and current will flow through the OR gates of the 4075 (IC3) and light up the l.e.d.s at a number between 1 and 6. While S1 is depressed all the l.e.d.s will appear to light up at once as the unit flashes through its cycle.



Stephen Ives,
Burnham-on-Crouch,
Essex.

CAR LIGHTS-ON WARNING

The circuit in Fig. 1 has been fitted to the author's car for over a year and works well. It is an audible alarm which sounds when the door is opened with the lights on. An extra feature of this simple design is a time limit so that the alarm does not continue to sound if the door is left open with the lights on. This could be the case at a petrol station or when dropping off a passenger.

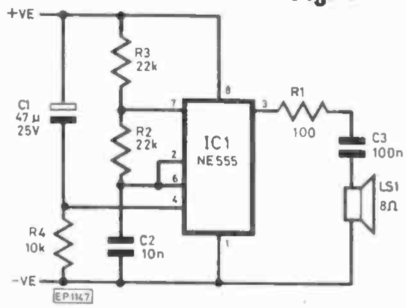
The alarm needs only two connections to the car electrics (Fig. 2). The first is to the feed for the panel lights and the second is to the wire which runs from the door courtesy-light switch to the light itself. The whole circuit, including the speaker, was mounted on Veroboard behind the dashboard.

The key to the design is D1. This detects the closure of the necessary switches and feeds current to the alarm. The alarm itself is an NE555 timer i.c. connected as an astable oscillator, running at audio frequency. The output from this component is sufficient to directly drive the speaker.

The time limit is provided by the combination of C1 and R4, connected to the reset pin of the timer. When the alarm initially sounds, C1 is discharged and gates the timer into oscillation. As C1 charges, the voltage at pin 4 becomes more negative and eventually turns off the sound. In fact, the result is not an abruptly ending tone, owing to a feature of the internal design of the NE555. The pitch of the oscillation is low for about three seconds, then quite high for three seconds—before it stops.

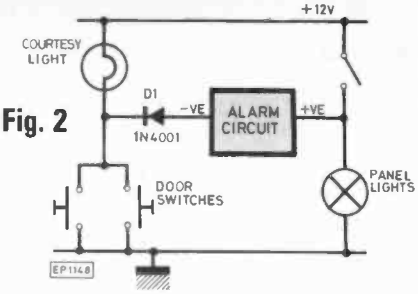
D. J. Greaves,
Cambridge.

Fig. 1



Alarm circuit

Fig. 2



Connections to car electrics

MICRO MULTIPLEXED DISPLAY

THE circuit shown (Fig. 1) is driven from a 6802 evaluation unit and can operate up to eighteen displays although only six are used in this application.

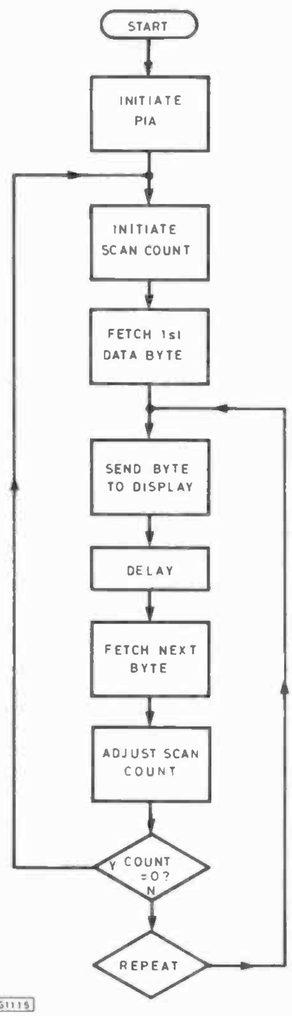
HARDWARE: The hex display requires four data lines, therefore the 8 bits on the PIA output lines (PB0–PB7) can supply data to two displays at any instance.

The PIA CB2 port is programmed to produce a strobe pulse on each 'write' operation and this is used via the 7493 and 7442 to generate three 'blanking' signals in sequence which multiplex two displays per occasion.

Decimal 3 output from the 7442 is used to reset the 7493 following generation of the blanking pulses.

Before transmitting data to the display, it is necessary to ensure that the 7493 is in the 'ready' position. This is achieved by means of the 74LS132 (IC9). When the reset switch (S1) is depressed then the oscillator formed by IC9 is enabled via TR2 and the 7493 is clocked until output 3 (Pin 4) on the 7442 is low. The reset circuit 'locks up' at this point and the 'ready' l.e.d. is energised via TR1. The display is now ready to accept data from the 6802.

SOFTWARE: The 6821 PIA is iniatiated with 'B' side as outputs and CB2 producing a strobe pulse on each write operation. Address 0030 is used as a scan counter and is loaded with 04 (pin). The first data byte is obtained from address 0040 and after sending to the display, the next byte is read from 004 etc. When three bytes have been transmitted to the display the programme jumps back to re-load the scan counter, and thus the cycle is repeated. As mentioned earlier, it is possible to expand the system to cater for 18



Flow chart

Add	Code	Mnemonics	Comments
0000	7F 4003	CLR PIA CRB	Set all PIA 'B' I/O lines as outputs and select CB2 to produce o/p strobe pulse.
0003	86 FF	LDAA# FF	
0005	B7 4001	STAA PIA DRB	
0008	86 2C	LDAA# 2C	
000A	B7 4003	STAA PIA CRB	
000D	C6 04	LDAB# 04	Set up scan count at addr 0030
000F	07 30	STAB $ 30	
0011	CE 0040	LDX# 0040	Fetch 1st data byte from addr 0040
0014	A6 00	LDAA#00	
0016	B7 4001	STAA PIA DRB	Send byte to display
0019	01	NOP	External data bus 'settling' time delay
001A	01	NOP	
001B	08	INX	Fetch next byte
001C	7A 0030	DEC $0030	Adjust scan count
001F	27 EC	BEQ	Start new scan
0021	20 F1	BRA	Send next byte to display

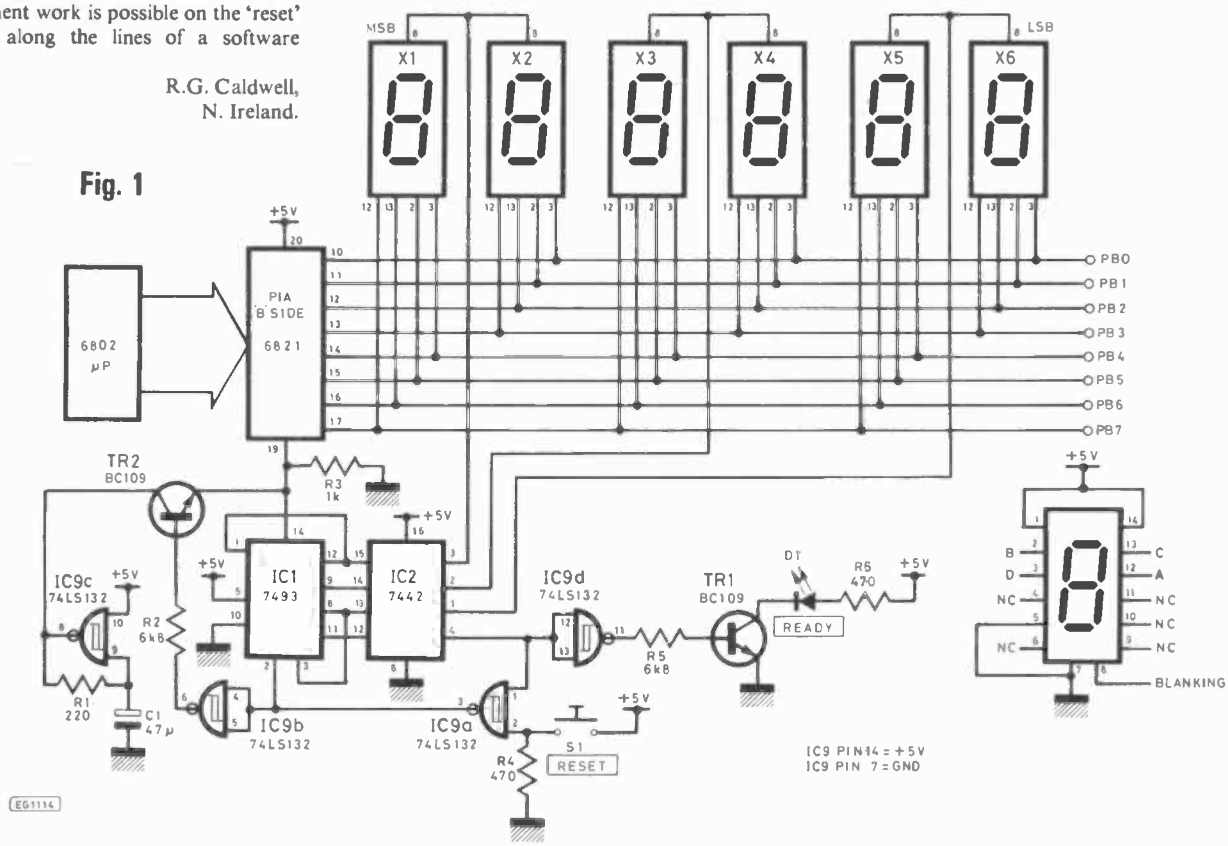
Notes:
1 Scan Count is located at addr 0030.
2 PIA CBR is located at addr 4003.
3 PIA DRB is located at addr 4001.
4 Display data located at addr's 0040, 41 and 42.

Software table

displays this being limited only by the 0-9 outputs on the 7442 i.c. Also, further development work is possible on the 'reset' circuitry along the lines of a software solution.

R.G. Caldwell,
N. Ireland.

Fig. 1



ROGER 'BLEEP BLEEP'

UNLIKE most published designs which only bleep at the end of transmission, this design bleeps both at the beginning and the end of transmission.

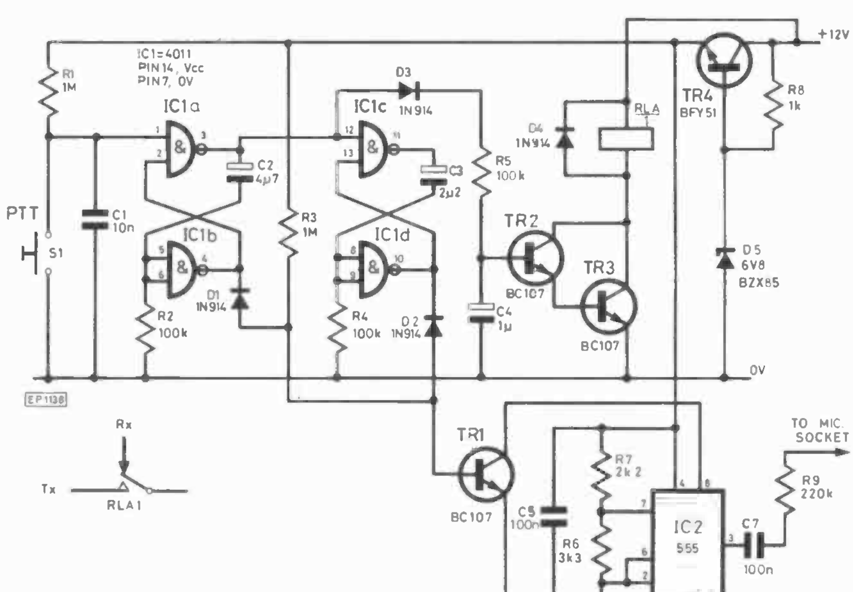
When the push to talk button (PTT) is pressed, flip-flop one (IC1a and b) controls bleep one via D1 and R3. Flip-flop two (IC1c and d) controls bleep two via D2 and R3 when the button is released.

The 555 tone generator (IC2) is switched on and off by pin 4 through TR1.

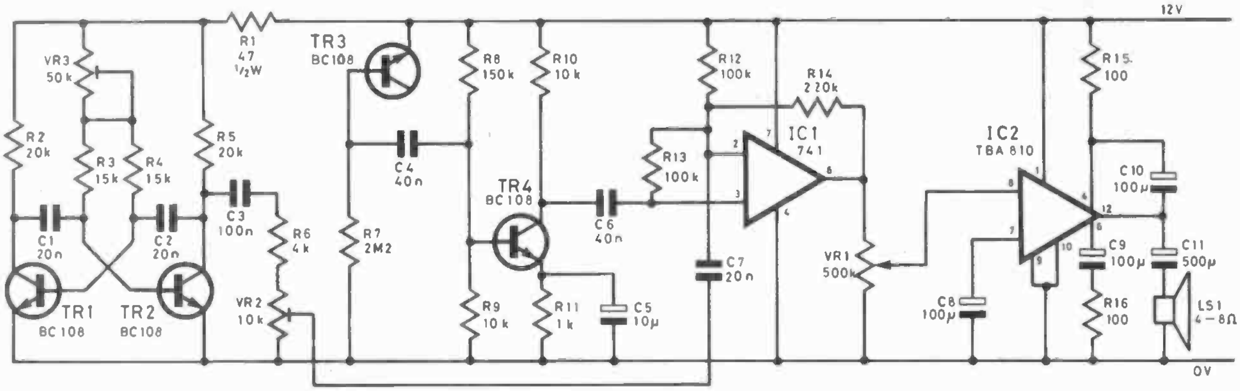
D5, C4 and R5 control the carrier delay via Darlington transistors TR2, TR3 and the relay (RLA1). The length of each bleep and carrier delay can be adjusted by altering the value of the electrolytics C2, C3 and C4.

A single bleep only at the end of transmission can be achieved by omitting D1, and the tone can be varied by altering the value of R6.

J. L. Colwill,
North Devon.



STEAM WHISTLE



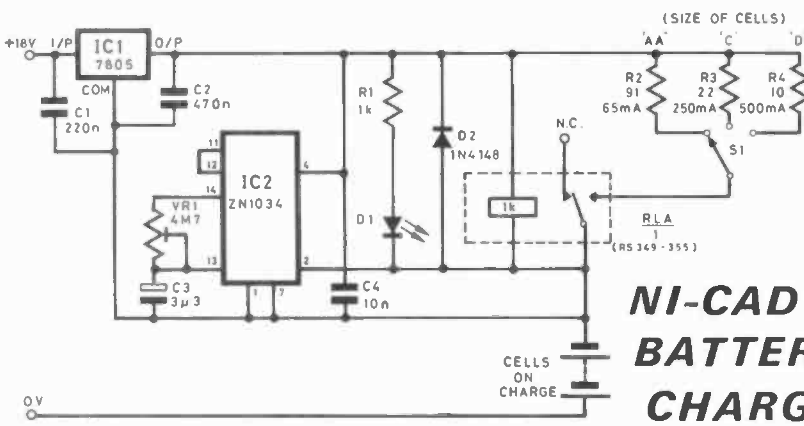
EG995

THIS circuit produces a sound similar to that of a steam locomotive whistle. TR1 and TR2 form a multivibrator, the frequency of which is set by VR3. This is the "toot" part of the whistle. TR4 amplifies white noise generated across the reverse biased transistor TR3. White noise and "toot" are mixed by IC1, the ratio of each being set by VR2. The output from IC1 is fed to a simple amplifier based around the TBA 810 device.

The positive 12V could be fed to the circuit by a push switch near the controller or by the model train itself by means of reeds or microswitch devices.

David John,
Alvaston,
Derby.

NI-CAD BATTERY CHARGER



EG1014

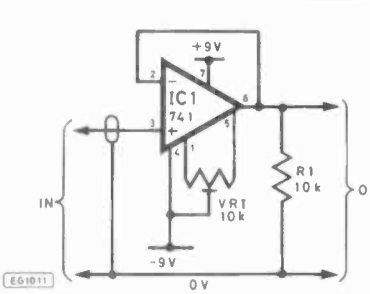
THE circuit shown is for a constant current Ni-Cad battery charger. It features a timed charge rate followed by a trickle charge for an indefinite period.

At switch on the output of the ZN1034 timer goes low bringing on the relay. This in turn passes a constant current from a 7805 voltage regulator to charge the batteries. After a delay of up to 12 hours, as set by the potentiometer, the output goes high switching off the relay. The cells now pass only the quiescent current of the circuit which is approximately 12 mA.

Up to six cells may be charged in series and an l.e.d. is included to indicate when the batteries are on full charge.

P. Thompson,
Glasgow.

HIGH Z INPUT FOR VOLTMETER



EG1011

FOR measuring voltages in circuits where currents are very small and resistances large, an ordinary multimeter is unsuitable because it draws an appreciable current from the circuit and therefore gives erroneous readings. It may also upset the operation of the circuit. This very simple impedance converter makes it possible to get true readings with even the most ordinary meter.

The op amp is connected as a unity-gain voltage follower. The voltage to be measured is applied between the non-inverting terminal and 0V. In this mode the input impedance can be very high—many tens of megohms maybe—but the output of the op amp is of very low impedance and will easily drive an ordinary meter. The voltage at the output will follow exactly that at the input, and the use of the offset nulling facility in a 741 ensures precise tracking between input and output. The nulling preset should be adjusted so that, with the input shorted, there is exactly nil voltage between output and the 0V line, as measured with the most sensitive range of a meter. The current drawn from the supply is minimal, and if two little 9V batteries are used, voltages up to about 8V may be measured. If only one battery is used, the junction between two 1k resistors across the supply will provide the 0V point, allowing measurement of voltages up to about 4·5V. To avoid any interference or hum pick-up, the input must be screened to 0V, and the whole ought to be in a metal case grounded to 0V.

Make input and output connections before switching power on; if pin 3 is left floating pin 6 will quickly drift into saturation and perhaps damage the sensitive range of a good meter.

S. A. R. Guest,
Truro.

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8/83

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7401	11p
7402	11p
7403	12p
7404	12p
7405	15p
7406	18p
7407	18p
7408	14p
7409	14p
7410	16p
7411	16p
7412	14p
7413	16p
7414	18p
7416	18p
7417	18p
7420	14p
7421	18p
7422	20p
7423	18p
7425	18p
7426	18p
7427	18p
7428	18p
7430	14p
7432	18p
7433	22p
7437	22p
7438	22p
7440	15p
7441	55p
7442A	30p
7445	50p
7446A	50p
7447A	36p
7448	45p
7450	15p
7451	15p
7453	15p
7454	15p
7460	15p
7470	30p
7472	25p
7473	25p
7474	18p
7475	22p
7476	25p
7483A	38p
7485	60p
7486	18p
7489	170p
7490A	20p
7491	35p
7492A	25p
7493A	24p
7494	35p
7495A	35p
7496	35p
7497	90p
74100	80p
74107	22p
74109	25p
74116	50p
74118	55p
74119	60p
74120	60p
74121	25p
74122	30p
74123	36p
74125	30p
74126	30p
74128	35p
74132	30p
74136	28p
74141	55p
74142	175p
74145	40p
74147	75p
74148	60p
74150	50p
74151A	36p
74153	36p
74154	50p
74155	36p
74156	40p
74157	30p
74159	75p
74160	40p
74161	40p
74162	40p
74163	40p
74164	45p
74165	45p
74166	48p
74170	120p
74172	250p
74173	50p
74174	55p
74175	50p
74176	40p
74177	45p
74178	70p
74180	40p
74181	115p
74182	40p
74184	90p
74185A	90p
74186	470p
74188	250p
74190	45p
74191	45p
74192	45p
74193	45p
74194	40p
74195	40p
74196	40p
74197	40p
74198	80p
74199	80p
74221	55p
74259	100p
74278	140p
74279	40p
74283	50p
74284	160p
74285	160p
74290	75p
74293	80p
74298	100p
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74376	100p
74390	75p
74393	90p
74490	95p

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74LS12	13p
74LS13	15p
74LS14	25p
74LS15	12p
74LS20	12p
74LS21	13p
74LS22	13p
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74LS28	14p
74LS30	13p
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74LS38	14p
74LS42	30p
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74LS48	45p
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74LS55	14p
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74LS74	16p
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74LS83	36p
74LS85	40p
74LS86	16p
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74LS112	20p
74LS113	20p
74LS114	22p
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74LS124	90p
74LS125A	24p
74LS126A	25p
74LS132	34p
74LS133	25p
74LS136	25p
74LS138	27p
74LS139	27p
74LS145	70p
74LS147	100p
74LS148	75p
74LS151	40p
74LS153	40p
74LS154	80p
74LS155	30p
74LS156	36p
74LS157	25p
74LS158	30p
74LS160A	36p
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74LS162A	36p
74LS163A	36p
74LS164	40p
74LS165A	50p
74LS166A	55p
74LS168	85p
74LS169	85p
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74LS294	700p
74LS295	90p
74LS297	900p
74LS298	90p
74LS299	150p
74LS321	150p
74LS323	160p
74LS324	150p
74LS348	90p
74LS352	60p
74LS353	60p
74LS356	250p
74LS363	140p
74LS364	140p
74LS365A	30p
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74LS368A	30p
74LS373	55p
74LS374	55p
74LS375	45p
74LS377	70p
74LS378	70p
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74LS393	45p
74LS395	90p
74LS399	160p
74LS445	100p
74LS612	£19
74LS640	100p
74LS641	100p
74LS642	100p
74LS643	100p
74LS644	100p
74LS645	100p
74LS668	100p
74LS669	100p
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74S02	30p
74S04	30p
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74S08	60p
74S10	40p
74S11	50p
74S20	40p
74S22	50p
74S30	40p
74S32	70p
74S37	60p
74S38	70p
74S51	70p
74S74	75p
74S85	300p
74S86	180p
74S112	90p
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74S114	90p
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74S138	110p
74S139	120p
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74S174	250p
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74C08	20p
74C10	20p
74C14	80p
74C20	20p
74C42	60p
74C73	
74C74	
74C76	
74C85	
74C90	70p
74C157	150p
74C160	90p
74C161	90p
74C163	90p
74C164	100p
74C173	48p
74C174	90p
74C175	90p
74C192	115p
74C193	115p
74C194	120p
74C195	100p
74C221	150p
74C244	160p
74C245	160p
74C373	180p
74C374	160p
74C902	70p
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74C922	470p
74C923	500p
74C925	550p
74C926	550p
74C928	550p

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4001	10p
4002	12p
4004	10p
4007	14p
4008	36p
4009	24p
4010	24p
4011	11p
4012	16p
4013	20p
4014	48p
4015	40p
4016	20p
4017	32p
4018	45p
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4059	450p
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4067	225p
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4094	90p
4095	75p
4096	70p
4097	290p
4098	90p
4099	100p
40102	150p
40103	180p
40105	120p
40106	40p
40109	100p
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4501	28p
4502	60p
4503	45p
4504	75p
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4507	35p
4508	130p
4510	45p
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4557	300p
4560	120p
4566	160p
4568	250p
4569	170p
4572	30p
4583	90p
4584	36p
4585	75p
40014	40p
40085	90p
40097	45p
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CA3019	80p
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CA3089E	200p
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CA3140E	40p
CA3160E	100p
CA3161E	150p
CA3162E	450p
CA3189E	300p
CA3240E	110p
CA3280G	200p
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DAC0808	200p
DG308	300p
HA1366	195p
HA1388	250p
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ICL7650	400p
ICL7660	250p
ICL8038	300p
LC7120	300p
LC7130	350p
LC7137	270p
LF347	150p
LF351	48p
LF353	95p
LF356P	95p
LF357	110p
LM10C	325p
LM301A	25p
LM310	120p
LM311	70p
LM318	150p
LM319	215p
LM324	30p
LM334Z	90p
LM335Z	140p
LM339	50p
LM348	65p
LM358P	60p
LM377	175p
LM380	75p
LM381AN	180p
LM382	120p
LM386	90p
LM387	120p
LM389	95p
LM393	100p
LM394CH	300p
LM709	36p
LM710	50p
LM711	170p
LM725	300p
LM733	60p
LM741	18p
LM747	70p
LM748	35p
LM1011	480p
LM1886	£5
LM1889	350p
LM2917	200p
LM3302	75p
LM3900	50p
LM3909	85p
LM3911	125p
LM3914	200p
LM3915	200p
LM3916	225p
LM13600	110p
M51513L	230p
M51516L	500p
MB3712	200p
MC1310P	150p
MC1413	100p
MC1458	36p
MC1495L	350p
MC1496	70p
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MC3401	50p
MC3403	65p
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NE556	45p
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NE565	120p
NE566	155p
NE567	140p
NE570	410p
NE571	400p
NE5534A	125p
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RC4136	60p
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S5668	225p
S50240	900p
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SN76477	450p
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TA7205	90p
TA7222	150p
TA7310	150p
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TBA800	80p
TBA810	100p
TBA820	80p
TBA950	225p
TC9109	750p
TCA210	350p
TCA220	350p
TCA940	175p
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TDA1008	320p
TDA1010	200p
TDA1022	500p
TDA1024	120p
TDA1170	300p
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TDA2003	325p
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TL072/82	45p
TL064/74	95p
TL084	90p
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TL430C	70p
UAA170	170p
UA2240	120p
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XR2206	300p
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ZNA234	850p
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ZN419C	190p
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ZN425E	340p
ZN427E	580p
ZN428E	490p
ZN429E	210p
ZN450E	790p
ZN459	600p
ZN1034E	200p
ZN1040E	670p

Microprocessors

1802CE	650p
2650A	£12
6502	350p
6502A	500p
6800	225p
6802	225p
6809	650p
6809E	£12
68809	£12
3035	350p
8039	£3
8080A	250p
8085A	450p
8086	£22
8748	£16
INS8060	£11
TMS9980	£20
Z8	£24
Z80	290p
Z80A	320p
Z80B	£12
8088	£18
TMS5100	£10
TMS9995	£12

SUPPORT DEVICES

2651	£12
3242	800p
3245	450p
6520	280p
6522	310p
6522A	550p
6532	550p
6551	650p
6821	100p
68821	220p
6840	375p
68840	650p
6850	110p
68850	220p
6852	250p
6854	770p
6875	500p
8154	950p
8155	350p
8156	350p
8205	225p
8212	110p
8216	100p
8224	110p
8226	250p
8228	270p
8243	280p
8250	850p
8251	250p
8253	390p
8255	255p
8256	£36
8257	£4
8259	£4
8279	440p
8284	350p
3288	100p
3755A	£15
9901	£10
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Z80CTC	250p
Z80ACTC	250p
Z80ADART	£7
Z80ADMA	£9
Z80SIO-0/1/2	£9

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CRT6545	900p
CRT5027	£18
CRT5037	£18
EF9365	£36
EF9366	£36
MC6845	£6
MC6847	650p
SFF96364	£8
TMS1601	£12
TMS9918	£36
TMS9927	£18
TMS9928	£20
TMS9929	£20

ZIF SKTS (TEXTOOL)

24 pin	575p
28 pin	£8
40 pin	975p

MEMORIES

2101A	400p
2102-3L	120p
2107B	500p
2111A	300p
2112-A	300p
2114-2L	100p
2147	450p
4027-3	300p
4116-15	120p
4116-20	100p
4118-3	500p
4118-4	450p
4164-2	450p
4164-15(TI)	450p
4416-20	500p
4532-20	300p
4552-2	350p
4816AP-3	280p
5101	210p
5516	850p
6116P-3	350p
6116PL-3	550p
6514	250p
6810	120p
74S189	150p
74S201	350p
74S289	150p
93415	600p
93425	600p
93L422	950p

ROMs/PROMs

74S188	150p
74S225	550p
74S287	225p
74S288	150p
74S387	650p
74S471	650p
74S473	650p
74S474	400p
74S570	650p
74S571	650p
74S573	900p

EPROMs

2532	350p
2564	£6
2708	£3
2716 (+5V)	250p
2716 (350ns)	500p
2732 (300ns)	350p
2764 25	£11
TMS2716	750p
27128 25	£25

UARTs

AY 3 1015P	300p
AY 5 1013P	300p
COM8017	300p
IM6402	360p
TR1602	300p

INTERFACE ICs

AD558CJ	775p
AD561J	£20
AM25S10	350p
AM25LS2521	£2
AM26LS31	125p
AM26LS32	125p
D7002	420p
DAC80	£28
DM8131	275p
DP8304	250p
DS3691	300p
DS8830	140p
DS8831	140p
DS8832	250p
DS8833	225p
DS8836	150p
DS8838	225p
MC1488	55p
MC1489	55p
MC3446	250p
MC3480	850p
MC3486	500p
MC3487	300p
MC4024	325p
MC4044	325p
MC14411	675p
MC14412	750p
ULN2003A	75p
75107	90p
75108/9	90p
75110/12	90p
75114/15	160p
75121/22	140p
75150P	120p
75154	140p
75159	220p
75365	150p
75451/2	72p
75453/4	72p
75491/2	65p
8T26	120p
8T28	120p
8T95/96	80p
8T97/98	80p
81LS95	80p
81LS96	80p
81LS97	80p
81LS98	80p
81LS120	250p
9602	220p
9637AP	160p
ZN425E-8	350p
ZN426E-8	350p
ZN427E-8	650p
ZN428E-8	500p

DISC CONTROL

FD1771	£20
FD1791	£22
FD1793	£23
FD1795	£28
FD1797	£28
FD2793	£42
FD2797	£42
WD1691	£15
WD2143	550p
8271	£26

CHARACTER GENERATORS

RO-3-2513UC	750p
RO-3-2513LC	700p
SN74S262AN	£10
MC66760	750p

CRYSTALS

32 768KHz	100p
100KHz	250p
200KHz	280p
1 0MHz	290p
1 008MHz	275p
1 8432MHz	210p
2 00MHz	225p
2 45760MHz	210p
2 5MHz	250p
2 662MHz	250p
3 276MHz	150p
3 5795MHz	100p
3 686MHz	300p
4 00MHz	150p
4 194MHz	200p
4 43MHz	110p
4 608MHz	250p
4 9152MHz	250p
5 00MHz	175p
6 00MHz	150p
6 144MHz	150p
7 00MHz	150p
7·168MHz	175p
8 00MHz	175p
8 86MHz	175p
10 00MHz	175p
10 50MHz	250p
10 70Hz	150p
12 00MHz	150p
14 318M	175p
14 756MHz	250p
15 00MHz	200p
16 00MHz	200p
17 7MHz	200p
18 00MHz	200p
18 432MHz	150p
19 968MHz	150p
20 000MHz	200p
26 690 MHz	150p
27 145MHz	200p
38 6667MHz	175p
48 0MHz	175p
55 5MHz	400p
116MHz	300p
145 80MHz	250p

KEYBOARD ENCODER

AY-5-2376	700p
74C922	420p
74C923	500p

MODULATORS

6MHz UHF	375p
8MHz UHF	450p

BAUD RATE GENERATOR

MC14411	675p
COM8116	700p
4702B	750p

TELETEXT DECODER ICs

SAA5020	£6
SAA5030	£7
SAA5041	£16
SAA5050	£9

REAL TIME CLOCK

MM58174	800p
MCM66760	700p

WIRE WRAP SOCKETS BY TEXAS

8 pin	25p	18 pin	50p	24 pin	70p
14 pin	35p	20 pin	60p	28 pin	80p
16 pin	40p	22 pin	65p	40 pin	100p

LOW PROFILE DIL SOCKETS BY TEXAS

8 pin	9p	18 pin	16p	24 pin	24p
14 pin	10p	20 pin	18p	28 pin	26p
16 pin	11p	22 pin	22p	40 pin	30p

VOLTAGE REGULATORS
FIXED PLASTIC

1A	+ve		−ve	
5V 1A	7805	•40p	7905	45p
12V 1A	7812	•40p	7906	45p
15V 1A	7815	•40p	7912	45p
18V 1A	7818	•40p	7915	45p
24V 1A	7824	•40p	7918	45p
5V 100mA	78L05	30p	7924	45p
12V 100mA	78L12	30p	79L05	50p
15V 100mA	78L15	30p	79L12	50p
			79L15	50p

OTHER REGULATORS

LM309K 1A 5V	135p	78HGKC	600p
LM317K	250p	78HO5KC	550p
LM317T 1A Adj	200p	78MGT2C	140p
LM337T	100p	78GUIC	200p
LM323K 3A 5V	450p	79GUIC	225p
LM723 150mA Adj	37p	79HGKC	700p
TL494	400p	TL497	300p
78S40	300p	LM350T	350p

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OCP71	180p	ORP60	120p	TIL78	55p

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MCT26	100p	TIL 112	70p
MCS2400	190p	TIL 113	70p
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TIL212 Ye	15p	Rectangular LEDs (R, G, Y)	30p
TIL216 Red	18p	NSB5881	670p
		TIL311	600p

DISPLAYS

		TIL312/3	110p
		TIL321/2	130p
DL704	140p	TIL330	140p
DL707 Red	140p	7750/60	200p
FND357	120p		
FND500	90p		
FND507	90p		
MAN3640	175p		
MAN4640	200p		

DRIVERS

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9370	300p
UDN6118	320p
UDN6184	320p

TRANSISTORS

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BC107/8	14p
BC108B	15p
BC109C	16p
BC169C	10p
BC172	12p
BC177/8	17p
BC179	18p
BC182/3	10p
BC184	10p
BC187	30p
BC212/3	10p
BC214	12p
BC237	10p
BC327	16p
BC337	10p
BC338	15p
BC461	30p
BC477/8	30p
BC516/7	36p
BC547B	12p
BC548C	12p
BC549C	12p
BC557B	14p
BC559C	16p
BCY70	20p
BCY71/2	20p
BD131	60p
BD132	80p
BD135	40p
BD136	35p
BD139	40p
BD140	40p
BD189	60p
BD242A	60p
BD379	40p
BD380	40p
BF244B	25p
BF256B	50p
BF257/8	30p
BF259	35p
BF337	30p
BFR39	20p
BFR40/1	20p
BFR79	20p
BFR80/1	25p
BFX29	40p
BFX30	34p
BFX84	25p
BFX85	30p
BFX88	25p
BFX89	150p
BFY50	24p
BFY51/2	24p
BFY56	30p
BFY90	80p
BRY39	40p
BSX19/20	24p
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MJ802	400p
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MJE3055	70p
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MPF105	30p
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MPSA13	50p
MPSA20	50p
MPSA42	50p
MPSA43	50p
MPSA56	25p
MPSA70	50p
MPSU06	55p
MPSU07	60p
MPSU45	90p
MPSU65	78p
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TIP31C	50p
TIP32A	40p
TIP32B	45p
TIP32C	50p
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2N2907A	25p
2N2926	9p
2N3053	25p
2N3054	55p
2N3055	48p
2N3442	140p
2N3553	240p
2N3584	250p
2N3643/4	48p
2N3702/3	10p
2N3704/5	10p
2N3706/7	14p
2N3708/9	12p
2N3773	300p
2N3819	25p
2N3820	40p
2N3823	50p
2N3866	90p
2N3902	700p
2N3903/4	16p
2N3905/6	16p
2N4037	65p
2N4056	65p
2N4123/4	27p
2N4125/6	27p
2N4401/3	25p
2N4427	90p
2N4871	50p
2N5087	27p
2N5089	27p
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2N5191	70p
2N5194	75p
2N5245	40p
2N5296	65p
2N5401	50p
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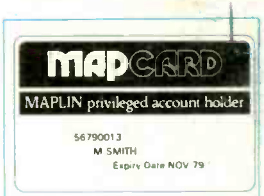

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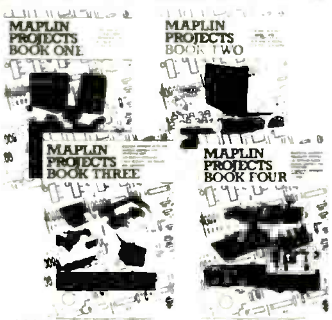

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309