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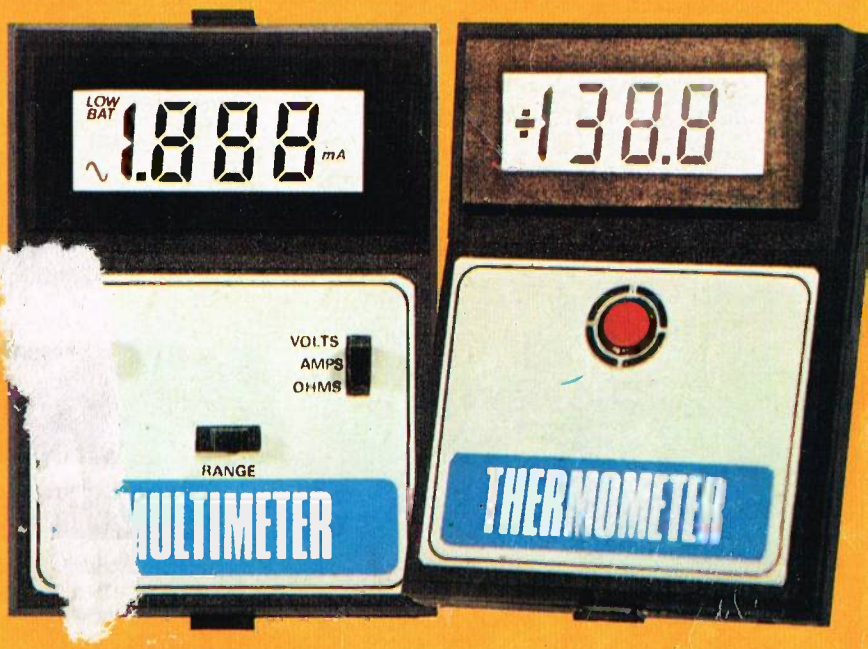
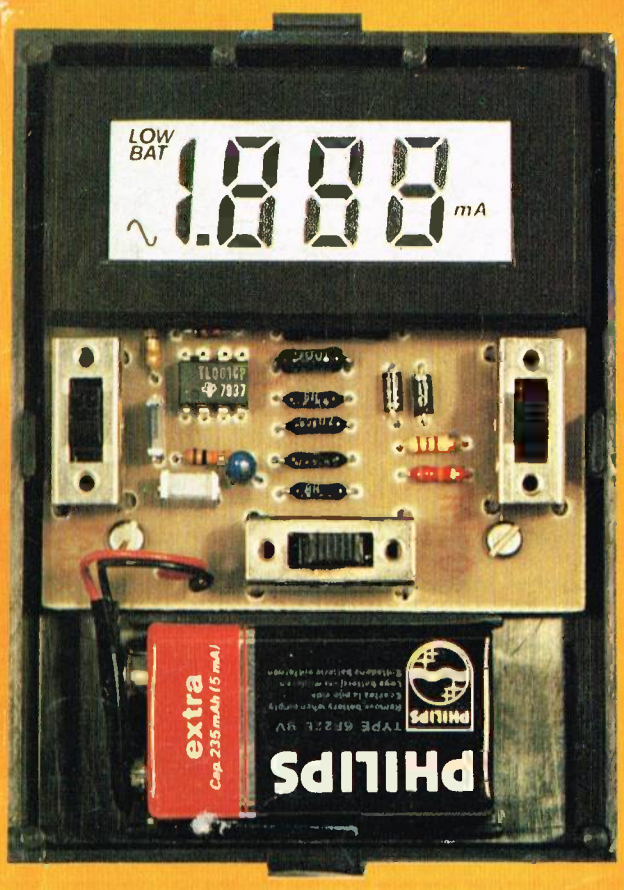
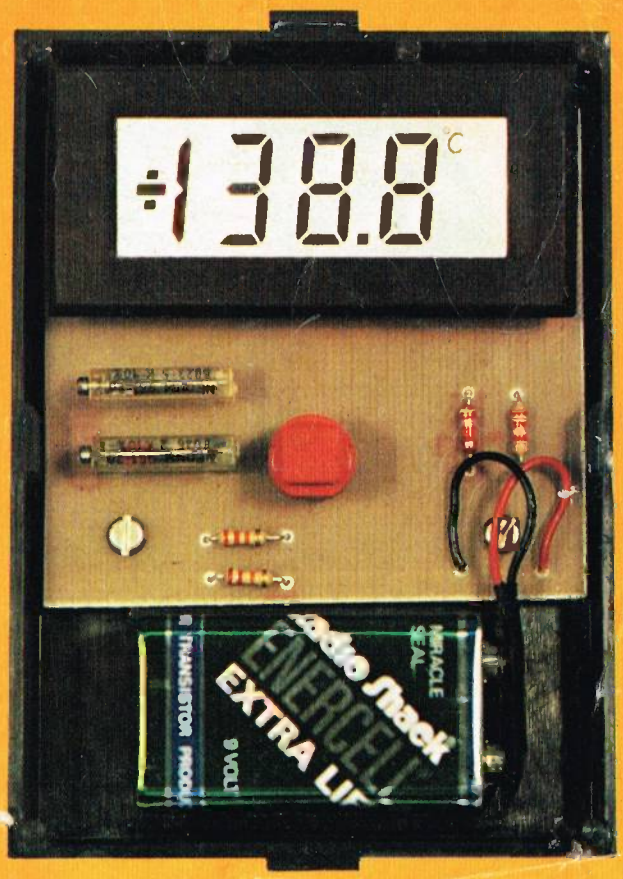






PRACTICAL
ELECTRONICS

VOLUME 17 No. 5 MAY 1981

CONSTRUCTIONAL PROJECTS

GENERAL FEATURES

NEWS AND COMMENT

OUR JUNE ISSUE WILL BE ON SALE FRIDAY, 8 MAY 1981
(for details of contents see page 29)

PE VOLUME 17 No. 5 MAY 1981

PE PROMOTION

As you will see from our free case on the front cover, this issue represents the start of a major promotion in PE. The case we have given you can be used to house any of the eight projects we will describe—or others of your own design. We will also be making extra cases available for regular UK readers who can send in the coupons (plus a small payment) from the June and July issues.

Tied up with the case is a DPM special offer and a competition—details of all these special features will be found in this issue. Next month we will give constructional details of three more case projects, a case coupon, the issue will carry a free pull out catalogue, have four "new look" *News and Market Place* pages and also include a special offer on a car booster amplifier for those that like to blow their minds whilst driving.

In July, we will bring you the remaining three case projects, a case coupon, DPM offer and all the usual features. In August we will bring you a special audio project, tied up with an offer on a graphic equaliser and hopefully the start of an excellent new series on digital design.

Why are we giving away all our plans now? To get you to buy issues of course. One of the problems that the recesssion has created is that the newsagents, like everyone else in business at the present time, must make sure of their profitability, one way they can do this is by only ordering the number of magazines they are certain to sell. In this way they have none left at the end of the month that they have paid for but not sold, so they maximise their profit. What it often means is that, if demand for a particular issue is high and you have not ordered one, you may miss out. With some issues (like this one) we can help by convincing the newsagent that our free gift—or whatever—will create extra demand and therefore persuade them to stock more issues; but we can't do it continually, so you can only make sure of your copy by ordering it.

ORDER!

Being realistic we know that not every reader buys every issue and, in these days of tight finance, few are willing to commit themselves to a year's supply in advance; but you can order just one issue—or two or three or more from any newsagent. It means you will get the ones you want without over-committing yourself and that we won't have to disappoint you or charge you 95p when you write in for a back number later!

By the way if you have ordered your copy and have still been unable to get one, do let us know—preferably by letter with a note of your suppliers name and address—so that we can investigate any distribution failure and correct it. We can also get you the copy you require. By giving us this information you can help to ensure a regular supply for yourself. Let us say once again PE has been published on time for seven months now, so please don't be put off by stories to the contrary.

We have said much of the above many times, but unfortunately some readers still appear to have problems in securing issues.

Mike Kenward

Technical Queries
We are unable to offer any advice on the use or purchase of commercial equipment or the incorporation or modification of designs published in Practical Electronics.

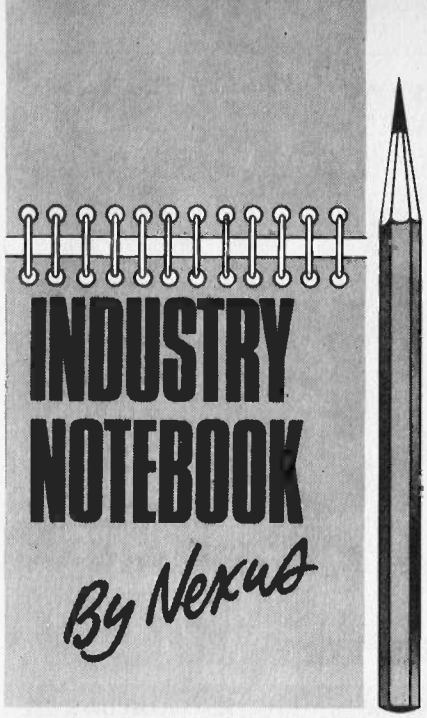
All letters requiring a reply should be accompanied by a stamped, self addressed envelope and each letter should relate to **one published project only.**

Components and p.c.b.s are usually available from advertisers; where we anticipate difficulties a source will be suggested.

Back Numbers
Copies of some of our recent issues are available from: Post Sales Department (Practical Electronics), IPC Magazines Ltd., Lavington House, 25 Lavington Street, London SE1 0PF, at 95p each including Inland/Overseas p&p.

Binders
Binders for PE are available from the same address as back numbers at £4·30 each to UK or overseas addresses, including postage and packing, and VAT where appropriate. Orders should state the year and volume required.

Subscriptions
Copies of PE are available by post, inland or overseas, for £11·80 per 12 issues, from: Practical Electronics, Subscription Department, Oakfield House, Perrymount Road, Haywards Heath, West Sussex RH16 3DH. Cheques and postal orders should be made payable to IPC Magazines Limited.



Dreamland

Imagine a TV and Hi-Fi production plant run on strict disciplinarian lines by former enemy nationals with a reputation for ruthlessness. Within that plant great use is made of wall-posters exhorting workers to produce more and better products. If propaganda fails there is the back-up of real fear of dismissal from safe, clean and profitable employment.

This could be a description of a Soviet-controlled operation in, say, The German Democratic Republic. In fact it is an albeit over-simplified and stark description of a highly successful operation run by the Japanese in, of all places, South Wales. An area of sturdy independence with a long and in-bred tradition of industrial militancy.

On the face of it we have the classic formula for discontent. The unyielding discipline, the drudgery of the production line, the carrot and the stick wielded in greater or lesser proportion, the endless propaganda, all the ingredients suggesting the wage slave conditions of 19th Century industrialisation.

This is a clear case for union intervention. How can people get away with it in late 20th Century Britain? Well, I have to report that this company is already unionised. The shop stewards like, if not actually love, the Japanese management. The workers love their work, the Japanese love the workers and also the local golf which is far cheaper and more accessible than in Japan. Best of all, the customers, most of them in mainland Europe, love the National Panasonic products pouring out daily from the factory. In fact there is so much love there must be a catch in it somewhere. Of course I use the word love rather loosely in this context and in contrast to the atmosphere in the longer-established coal and steel industries nearby.

I have been trying to analyse why this plant is apparently so successful, not only in the financial sense with a fine export performance, but also in harmonius relations and even joy at the workbench. After all, this is just an ordinary factory, there are hundreds of others like it. Discipline is really tough but this ought to make things worse. In practice it doesn't.

After long thought I came to the conclusion that it is simply a matter of attitude. Of the bosses, of the workers, of the union concerned and its on-site representative.

The company had the undoubted advantage of starting from scratch. There were no hurdles of ancient work-practice to be overcome. People were anxious to work there, willing to be trained and accepted that the work-methods they were taught and the general discipline were in their best interests for continuity of employment.

So far, all common sense. The only master stroke, hardly deserving of being called a touch of genius although it is little less, was to drive home a simple message, understood by the Japanese and ignored or unknown to large sections of the working population in the UK.

The message is a simple reminder that the company and the local bosses don't pay the wages. They are paid entirely by the customer. The customer is the real boss. If he buys a rival product, no wages.

Once this message gets home the rest follows automatically. The local management is there only to help keep the plant well-oiled and running smoothly. The workers are those most involved in keeping the boss-customer happy. Thus, the wall-posters and frequent pep-talks emphasising quality, quality, quality. And the workers respond by forgetting they are line operatives. They are now something nobler, real craftsmen and craftswomen with pride in the quality of their work and satisfaction in its doing. There then follows the exquisite feeling of success, success, as more and more orders flow in. The boss-customer out there in Germany or Italy, or wherever, really needs you. You make him happy and he pays your wages. You are now important—a valuable member of society performing a worthwhile service on which other people depend.

The cynics, not to mention those obsessed by class-struggle and conflict, may observe that nothing has changed except further refinements in brain-washing. Perhaps this contented body of peope are living in a dream world of their own. It's worth thinking about. But, on balance, my own preference is for contentment rather than bitterness, for enjoying work rather than hating it, for being a member of a successful team rather than a failing one, and for prosperity rather than poverty. In this I rather think I share a common feeling with the people I have described in South Wales.

With the recent announcement that Canadian-owned Mitel is to set up a plant in Wales it will be interesting to compare management style and worker acceptance in due course. A further interesting comparison, again in the future, will be whether Japanese-style management will work as well in the automobile industry in the UK as it apparently does in electronics. Time alone will tell.

The Times

As so often happens, my reference to The Times newspaper in the March issue was overtaken by events. As readers will be aware, The Times was acquired by another owner and thus saved from closure. The context in which I wrote, however, remains valid. The new technology had, in the end, to be accepted in the interests of survival with resultant redundancies. Nobody won the battle. There were only losers.

Racal

Again, in the March issue, I gave a guesstimate of Racal results. Since then the half-year results have been released and I was not far off target. The turnover for the half-year was £240·6 million and pre-tax profit £26·5 million, up 13·4 per cent. As this includes Decca losses in the period, not to mention the world recession in trade, again this was another triumph of Racal performance for the umpteenth time, in fact the 26th successive year of uninterrupted growth and profit. Ernie Harrison was completely confident of an exciting and prosperous future. The enthusiastic workforce now numbers 16,000 with 4,000 of them beavering away in the USA.

MEDL

The re-organisation of the microelectronics interests and operations in the GEC-Group is now bearing fruit under the banner of Marconi Electronic Devices Ltd.

Integration is going on apace with the prospect of MEDL becoming the biggest British-owned semiconductor company in the UK. HQ will be at Lincoln together with a large new plant and there is also a new custom-design centre at Wembley.

It's early days yet but MEDL is already forecasting taking a 40 per cent share of the UK market for custom-built LSI and has hopes of capturing 15 to 20 per cent of the European market as well.

Looking round the electronics industry it is hard to see a gloomy face, the only major exception being ICL, currently in a bad patch but still optimistic for the future.

Popular Myths

A high-value pound is bad for exports, yet exports are increasing. A tight monetary policy is needed to bring down inflation, yet inflation is dropping faster than expected while money supply is way over target. There is no money about for investment, yet high-risk shares in British Aerospace were over subscribed by 350 per cent. Last year would reveal a serious balance of payments deficit, yet it turned out as a record year in surplus. This year it clearly couldn't last, yet in January returns showed the biggest-ever surplus, nearly a billion pounds in a single month. We are all being crushed by the recession, yet personal savings are higher than ever and still increasing.

One thing is certain—economists and forecasters are consistently wrong in their theories and crystal-gazing. Or else officially-issued statistics are full of computer errors.

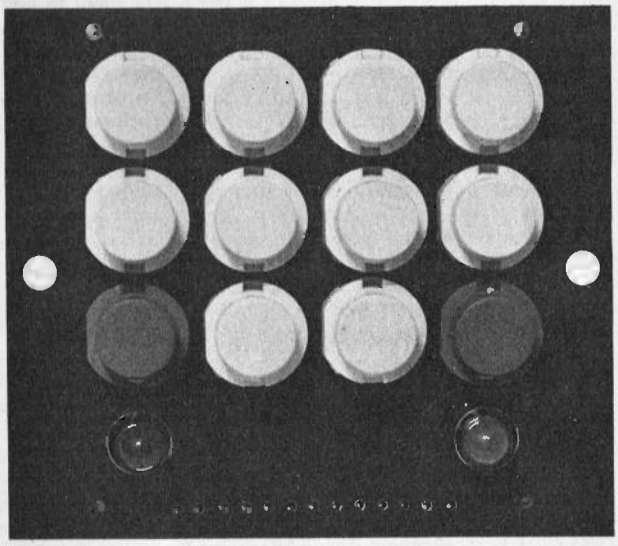
DIGITAL LOCK

BART TREPAK

Dedicated chip provides keyless lock alternatives

THIS simple project should be equally applauded by anyone who has locked him or herself out of the house or had their car stolen or towed away. Apart from these two obvious applications, the lock could be used to prevent operation of other electrical or electronic equipment (e.g. burglar alarms, garage door openers, etc.) by unauthorised persons, or when used in the momentary mode with some modification as a device to prevent you from drinking and driving. The advantages of the unit over its mechanical counterparts are manifold. Persons may be "authorised" simply by telling them the code while changing the lock will be a thing of the past, as the code may easily be changed by means of a small hard-wired plug. Another useful facility is the "save" mode, which will be explained later.

The circuit will operate on supplies of 5 to 18V requiring a mere 40μA standby current. **There are over 5,000 (5,040 to be exact) different four digit combinations,** which should discourage even the most persistent intruder.



Keyboard for latching lock. The alternative "momentary output" keyboard loses the coloured keys and l.e.d.s

CIRCUIT

The printed circuit board permits either of the two circuits shown to be built. The first circuit gives a static output, i.e. the output once "opened" stays open until "locked", and is ideally suited to automotive anti-theft applications where the ignition may be disabled until the correct key sequence is pressed.

The "Sense" input is connected to the ignition switch so that when the ignition is switched on, this input goes high and the unit is ready to accept the correct key sequence. All the keys from the keyboard are connected to the 16-pin socket, the plug being wired so that six of the keys are connected to the reset input (pin 2) of the i.c., while the remaining 4 keys go to inputs 1, 2, 3 and 4 (pins 3, 4, 5 and 6 of the i.c. respectively). The two remaining keys "Lock" (red) and "Save" (green) are not connected through the plug and socket and are wired directly to pins 7 and 11 of the i.c. If the keys are pressed so that inputs 1, 2, 3 and 4 are activated in that sequence, the output will turn on and activate the relay. This state will be indicated by the red l.e.d. turning off. If the keys are depressed in any sequence other than that described, the internal sequence detector will be reset and the entire sequence must be repeated.

The on condition of the lock may be saved when the ignition switch is turned off (i.e. when the sense input becomes low) by depressing the "Save" key. This will cause the green l.e.d. to light. If the ignition switch is turned off while the green l.e.d. is on, the output status will be stored in the internal memory, so that when the ignition switch is turned on again there is no need to go through the input sequence. This is useful if the car is to be left in a garage for servicing or parked by a person who does not know the code. The "Save" status may be cancelled by pressing the "Lock" key and turning the ignition off for a time determined by capacitor C1 to pin 12. This will also turn off the lock control output.

The second circuit provides momentary operation, the output switching on for a duration (determined by C1) after a correct input code sequence and then switching off. This mode of operation is useful in door locks and similar applications, where low power drain is required and the output only needs to be on while the door is being opened. In this case, the "Lock" and "Save" switches, and l.e.d.s, are not required. An output status l.e.d. may be connected to the output (in series with a suitable resistor) to indicate when the lock "opens" if required.

The incorporation of the plug and socket in the design enables the user to choose the "open" sequence and also to enable the sequence to be changed if required for greater security.

'Latched' and 'timed period' locks

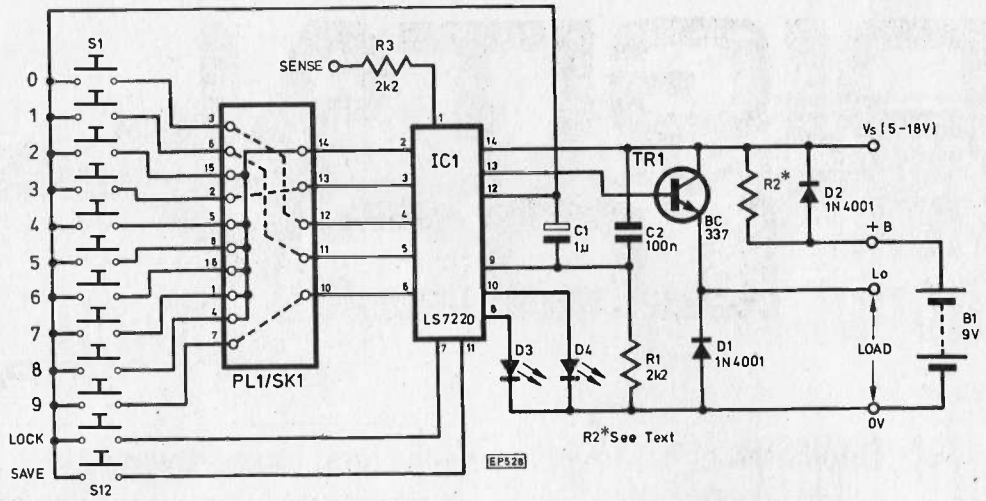


Fig. 1. In this circuit the load is not switched in until the correct digital sequence is keyed in. Here this is 3019

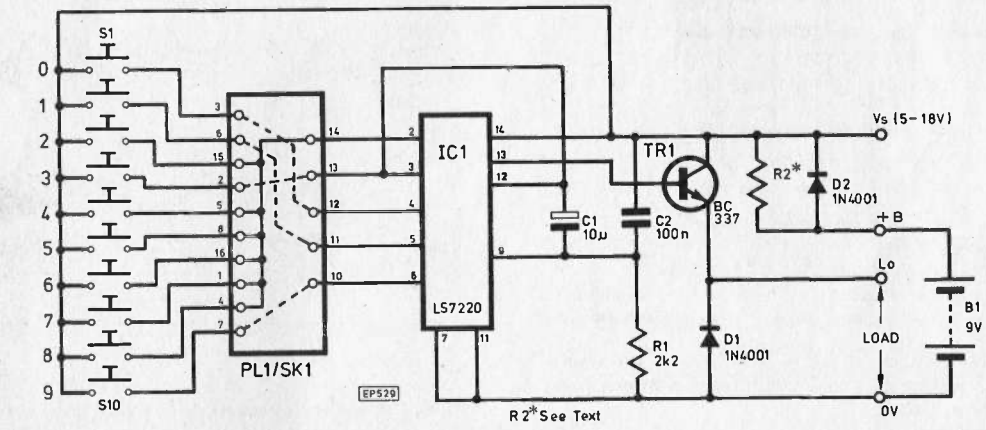
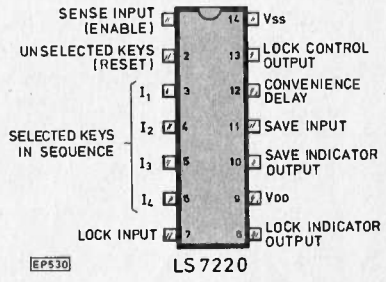


Fig. 2. In this alternative circuit a time delay is introduced before switching takes place. The wired code is again 3019



COMPONENTS

Resistors

R1	2k2
R2	See text
R3	2k2

Capacitors

C1	1µ or 10µ elects (appropriate to circuit) 16V
C2	100n

Switches

S1–S10	Key switches (white)
S11	Key switch (red)
S12	Key switch (green)

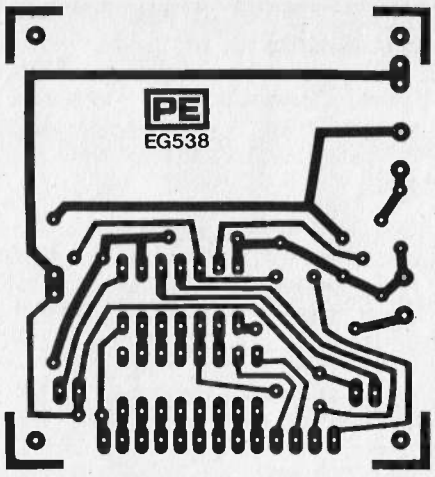
Miscellaneous

P.c.b.s, 16 pin d.i.l. plug, 14 and 16 pin d.i.l. sockets

A complete kit of parts is available from **TK Electronics, 11 Boston Road, London W7 3SJ.**

TABLE 1

Switch No.	Plug Pin No.	Function	Plug Pin No.
0	3	Invalid Keys	14
1	6	First Key	13
2	15	Second Key	12
3	2	Third Key	11
4	5	Fourth Key	10
5	8	Not Used	9
6	16		
7	1		
8	4		
9	7		



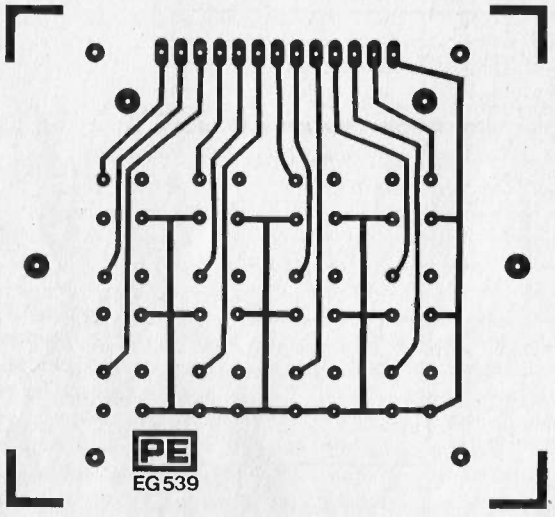
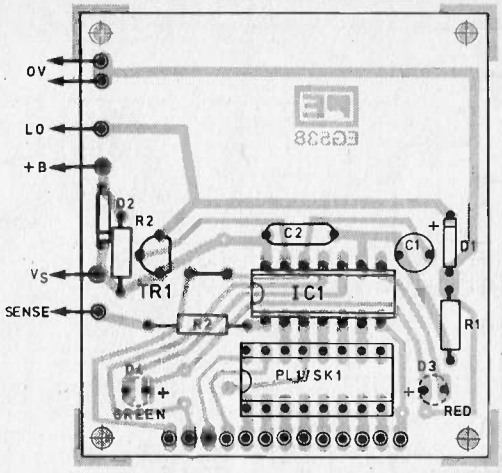
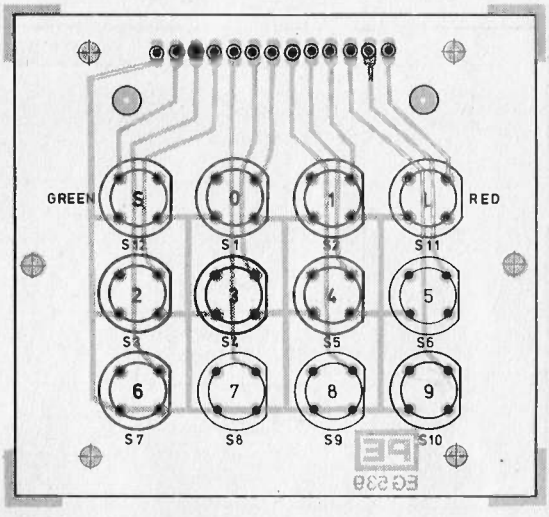


Fig. 3. Below is the keyboard p.c.b. and above the main p.c.b. The pair fit together as a sandwich hinged about pins soldered to the common pads





E0541

Fig. 4. Component assembly for 'latching' sandwich

The unit will operate on any supply in the range of 5 to 18V d.c., and draw a maximum standby current of 70μA, excluding the l.e.d.s and any load, such as a solenoid. This makes the unit ideal for 12V (car battery) or a mains derived supply. A 9V rechargeable NiCad battery may be used to enable the unit to operate during power failures. Provision is made for trickle charging the battery via resistor R2.

CONSTRUCTION

The circuit is constructed on two p.c.b.s, the main p.c.b. and the keyboard.

The keyboard should be constructed first by inserting the key switches into the p.c.b. and soldering, paying particular attention to the switch orientation. If the second circuit is to be built, the red and green switches should be omitted.

The main p.c.b. should now be constructed as shown in the diagrams, following the layout for the selected circuit. Care should be taken to ensure that diodes, electrolytic capacitors and transistors are inserted into the p.c.b. with the correct polarity.

Since the i.c. is a p.m.o.s. device it may be easily damaged by static. Avoid touching the pins and remove it from its packaging only when it is required. The use of a 14-pin i.c. socket is strongly recommended.

The two p.c.b.s should now be mated back-to-back by inserting four pins on the keyboard p.c.b. into the main p.c.b. and soldering. Since the p.c.b.s are mated with their copper sides together, ensure that there is adequate separation between them to prevent the switch leads from touching tracks on the main p.c.b. The two l.e.d.s should now be mounted (if required) by inserting them through the holes in the keyboard and soldered to the main p.c.b. Since the l.e.d.s are mounted on the copper side of the p.c.b. (unlike the rest of the components) great care should be taken to ensure that no solder bridges are formed between adjacent tracks. The length of the l.e.d. leads will depend upon the way in which the unit is mounted, as these will be mounted on any front panel used.

Using tinned copper wire make the 13 connections between the two p.c.b.s, ensuring that no two wires touch or that there are no solder splashes between the p.c.b. tracks or pads. If a rechargeable 9V battery (PP3 type) is to be used, this should be placed in position, below the i.c. on the main p.c.b., and secured with a double-sided adhesive pad. A battery connector should also be soldered to B+ and 0V. The value of resistor R2 will depend upon the supply voltage Vs, and the required charging current. PP3 type rechargeable batteries normally have a maximum continuous charging current of 1mA. The value of the resistor is given by (Vs − 9) kilohms. Thus with a 12V supply, for example, a resistor of about 3k (3·3k) should be used.

The plug should now be wired to give the desired "open

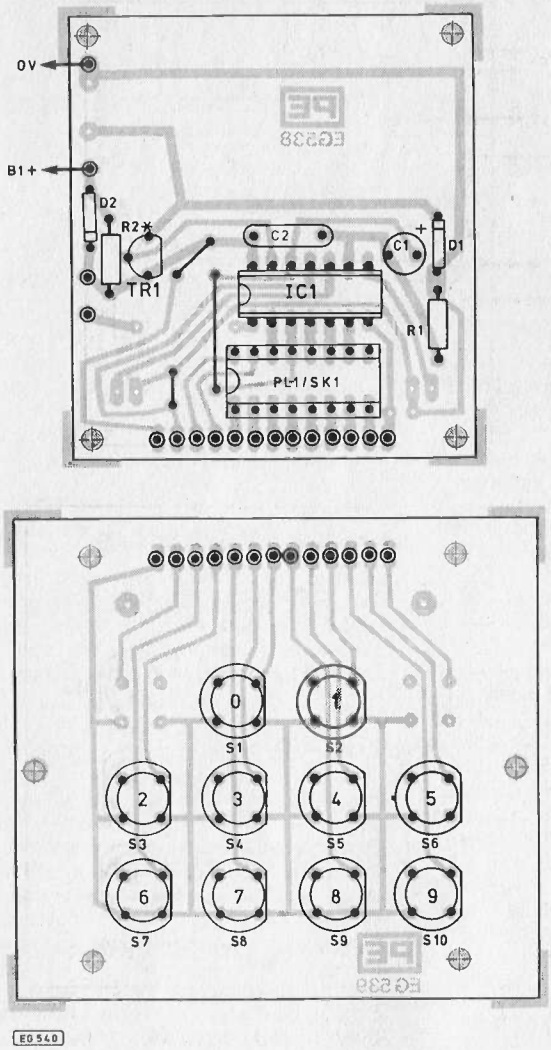


Fig. 5. Component assembly for 'timed period' sandwich

sequence" code. The keyboard switch numbers corresponding to the socket numbers are given in the table. Thus for an input code of say 3019, the plug would be wired with pin 2 (key 3) connected to pin 13 (input 1); pin 3 (key 0) connected to pin 12 (input 2); pin 6 (key 1) to pin 11 (input 3); pin 7 (key 9) to pin 10 (input 4) and all the unused pins (1, 5, 4, 8, 15 and 16) connected to pin 3 (reset input). Similarly, any other four digit code may be wired. Spare dual in line plugs can be wired to enable a number of different codes to be plugged into the unit if required. In the circuit the code is 3019.

The unit has been designed to mount on any suitably drilled front panel. In automotive applications this will, of course, involve drilling ten or twelve 9 mm. diameter holes plus two 5 mm holes for mounting the l.e.d.s and a further two holes for securing the unit to the dashboard. If the unit is to be used as a door lock, then it should be mounted in the doorframe. A suitable front panel would be a metal blanking plate as used in house wiring. These are available in chrome or brass finish from most electrical suppliers and have the mounting holes already drilled.

As in all security applications thought should, of course, be given to ways of preventing the unit from being removed and bypassed from the front (i.e. without first gaining access by entering the required code).

LOCK MODIFICATIONS

Apart from the obvious uses already described, the unit can be modified to provide other useful features.

In both circuits, capacitor C1 must be charged before the unit will respond to inputs. In the latching circuit, this is done by means of the "Sense" input which activates a circuit within the i.c. which charges the capacitor. In the momentary circuit C1 is charged when the first correct key is pressed (see circuit diagram), after which it begins to discharge via a resistor within the i.c. Thus, in the momentary mode, the complete code has to be entered before the capacitor discharges for an output to be produced. This can, for example, be useful in a "drink and drive tester", where the time taken to enter the correct code would depend upon how sober the driver was. The value of the capacitor should be selected by experiment—a value of 1µ and two pints being a good starting point.

Another point to notice is that all invalid keys are connected to pin 2 and the i.c. By monitoring this pin, an anti-tamper circuit could be added to disable the lock for a period of time and/or sound an alarm after a few incorrect entries. CMOS logic i.c.s should, of course, be usd as these will not consume a lot of current and will interface easily with the circuit. ★

News Briefs

CB: FM IN AUTUMN

CB Radio is to be legalised in this country on two frequencies: 27MHz FM and 930MHz FM. This was announced by the Home Secretary Mr William Whitelaw on February 26th, in a Parliamentary answer to Mr Patrick Wall MP. The use of 27MHz AM equipment remains illegal.

Users of the new service will have to buy an annually renewable licence which will entitle them to the use of both frequencies. It has not yet been decided what the cost of a licence will be.

All 27MHz FM equipment will have to conform to set standards, in order to ensure a minimum of interference to other users, and the equipment will have to be permanently marked to show that it meets the standards required.

The Home Secretary stated that he hopes to be able to introduce the new service by early autumn. Should any reader wish to contact the Home Office about CB Radio, they should *write* to the following address:

The Radio Regulatory Department, Waterloo Bridge House, Waterloo Road, London SW1 8UA.

POINTS ARISING

DIGITAL COUNTER-TIMER *(February 1981)*

On page 35 the captions "(a) Input Attenuator" and "(b) Preamplifier" should be transposed. On the same page, the link shorting +5V to GND across TR1 (TR101) should be a 100n disc ceramic decoupling capacitor.

In Fig. 1 (page 34), C3 should be 1n1 in value and not 1µ1. Fig. 8 (page 37): TR3 is an n.p.n. type transistor.

Semiconductor UPDATE...

FEATURING TMS 9909 AD 636 SAB 0600

R.W. Coles

DISC CONTROL

Most owner of microprocessor based home computers like the UK101 and the NASCOM have to make do with a cassette system for bulk storage, and it can be frustrating waiting for those big BASIC programs to load at 300 baud.

Whilst waiting, we can drool over the advertisements for floppy disc systems, and then come down to earth with a bump on reading the price at the foot of the page!

The advantages of floppy discs extend beyond the ability to load lots of data in a very short time, nice though that feature is. Equally important is the random access rather than sequential nature of disc storage, but best of all for my money is the fact that discs come with a software disc operating system, or DOS which makes any microcomputer seem like a "big" computer to the programmer. Droolers can take heart at the ever decreasing price of the disc drives themselves, but by the time the necessary "disc controller" circuitry is added to the total, the piggy-bank still shows little sign of coping.

What is needed perhaps, is a constructional project for a disc controller, and this could be one step closer now that Texas Instruments have introduced the TMS 9909. This new chip together with only a few other components can be used to build a full function disc controller which hitherto would have needed dozens of seperate packages, and an expensive p.c.b. A particularly useful feature of the TMS 9909 is its great versatility. It can cope with up to four drives which can be 8 inch (standard floppy), $5\frac{1}{4}$ inch (mini-floppy), single or double sided, single or double density, hard or soft sectored, and it can handle all three types of modulation, FM, MFM, and MMFM. Internally, the controller is actually a dedicated microprocessor, but it is easily interfaced to most existing microprocessor systems via the data bus and certain control lines. Available controller functions include read data, write data, step to a track and format a track. Once instructed to perform a function by the host system, the TMS 9909 will complete the task independently, transferring data to and from the host using Direct Memory Access (DMA). Completion of the task can be signalled by an interrupt, or the host may poll the controller by reading its current status, to determine whether the task is finished and whether any error conditions have occurred. The chip both generates and validates cyclic redundancy check bits which are added to the data written. During read the CRC bits are regenerated and compared with the bits on the disc, any discrepancies are flagged.

The TMS 9909 is housed in a 40 pin package and runs from a five volt supply. External components required include a 6MHz crystal and the high speed data separation logic. Perhaps we'll soon be able to stop drooling!

CHIP CHIME

If you, like me, find the prospect of a door chime which plays the "funeral march" under microprocessor control just a bit *too* avant garde, you may be happy to know that a rather less radical approach to the electronic doorbell is on its way. For all us soppy traditionalists, Siemens AG have produced a nifty little chip which doesn't play jolly tunes, or even greet you with "Have a nice day!" it just sits there and produces a melodious chime sequence without even the hint of an electronic raspberry.

The new device is the SAB 0600, and unlike its flashy microprocessor rivals, it lives in a diminutive 8 pin mini-d.i.p. and needs only one resistor, three capacitors and a small 8 ohm speaker to function. It generates three harmonically related tones at 440, 550 and 660Hz using a digital divider chain running from a 13·2 kHz RC oscillator. A further division produces a lower frequency count which then drives a four bit digital-to-analogue converter to provide a decay voltage for gradually attenuating the output of each tone in the sequence. The output stage can drive the speaker with about 150mW, insufficient to frighten the most timid moggy, and at the cessation of the melodious chimes, the chip shuts itself down to take less than 1 microamp from a supply of between 7 and 11 volts, typically provided by a PP3 battery.

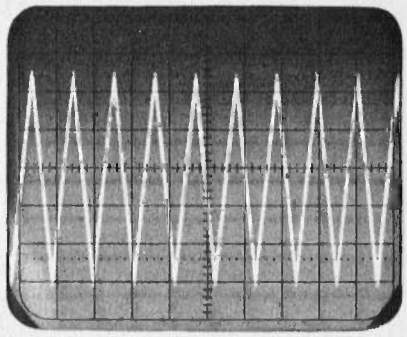
The SAB 0600 can be used in many applications other than door chimes, such as car alarms, clocks, toys and kitchen appliances. The brave can also experiment by combining two or more chips with detuned oscillators to generate richer tones, and the performance of the speaker can be modified by encasing it in a tube or horn.

IT'S TRUE

As we all learn at school or in college, the best way to display any a.c. voltage or current is to use its root-mean-square (r.m.s.) value. We also learn that most a.c. meters do not actually display a true r.m.s, only a rectified average which is scaled to show an r.m.s. equivalent. The averaging ploy has the big disadvantage that the scaling relationship only works for waveforms of one shape, and most meters are calibrated only for the case of a sine wave. Displaying any signal with a *different* shape gives an incorrect r.m.s. value which can be quite misleading.

The reason most meters do not display true r.m.s. lies in the complexity of the function itself, literally the problem of calculating the square root of the mean sum of the input values squared, and providing an equivalent d.c. output voltage or current to drive the meter. True r.m.s. meters *have* been available, at high cost, but there hasn't been much chance of getting such goodies on your favourite pocket multimeter, at least until now.

Enter the AD636 from Analog Devies, a low cost, analogue, monolithic i.c. in a 14 pin d.i.l. package which performs true r.m.s. to d.c. conversion with an excellent frequency response and a typical error of plus or minus 0·2%, depending on crest factor. The input range of the new chip is 200 mV and it consumes less than 1mA from supplies of between 5 and 24 volts. An added bonus is the provision of a dB output pin which gives a d.c. output equivalent to the log of the r.m.s. value, with a variable 0dB reference level which can be set externally. The chip also has an uncommitted buffer amplifier available which can be used as a high impedance input stage or as a high current output stage, perhaps to drive a moving coil meter.



Oscilloscopes ....HOW THEY WORK

Part Two... Circuitry... by Ian Hickman

This feature is taken from the last two chapters of a new book by this well-known author. Published by Newnes Technical Books the paperback is entitled *Oscilloscopes. How to use them. How they work.*

THE block diagram of a typical dual-trace, high-performance oscilloscope is shown in Fig. 12. Two identical input channels A and B are switched alternately to a common amplifier, which drives a delay line. This is shown diagrammatically as composed of discrete inductors and capacitors, although in a modern instrument it would usually consist of a length of delay cable. This is similar to co-axial cable, except that is has a centre conductor wound in the form of a spiral and hence provides much greater delay per unit length. As the drive to the trigger circuit is picked off before the delay line, the delay introduced by the latter permits the whole of the leading edge from which the scan was triggered to be observed. This assumes of course that the rise time of the leading edge and the "wake-up time" of the trigger circuit are together less than the delay introduced by the delay line, which is generally tens of nanoseconds.

The final Y amplifier produces the push-pull voltages that drive the Y plates, and in a higher-performance instrument the peak-to-peak output swings required might be little more than a few tens of volts, especially if using a tube with a high p.d.a. ratio and a scan-expansion lens. The X amplifier has to provide several times as much voltage swing as the Y amplifier, as the X-plate sensitivity is less than that of the Y plates. Fortunately, a substantially smaller bandwidth suffices for the X amplifier, easing the circuit design problems; the c.r.t. designer takes advantage of this to maximise the Y-plate sensitivity at the expense of the X-plate sensitivity.

The X deflection amplifier is driven with a sawtooth waveform produced by a "sweep" or "timebase" generator, which itself is triggered by a pulse from the trigger circuit. The trigger circuit produces a pulse each time the Y input voltage crosses a given threshold voltage, which is usually adjustable by the front-panel trigger level control. Thus the sweep always starts at the same point on the waveform, the sweep generator thereafter being insensitive to further trigger pulses until it has completed both the trace and the following (blanked) "retrace" or "flyback".

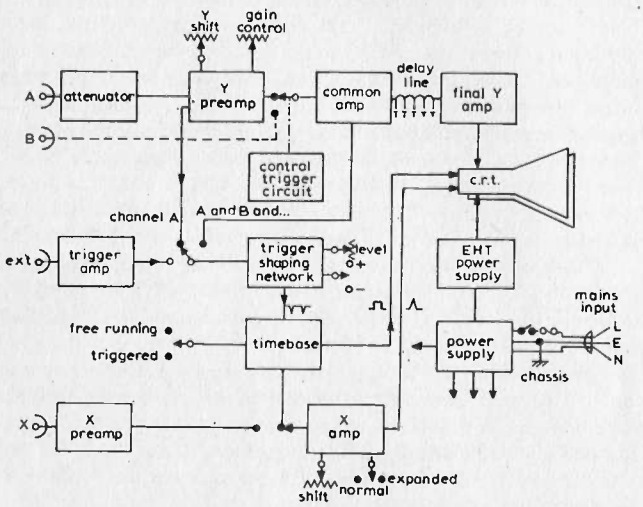


Fig. 12. Block diagram of dual-trace mains-operated oscilloscope *(courtesy Enertec Instrumentation Ltd.)*

CIRCUIT ELEMENTS

It is probably true to say that, at the time of writing, the majority of oscilloscope designs make use mainly of discrete components. However, integrated circuits are being used to an increasing degree, especially in high-performance oscilloscopes, and this trend will doubtless continue and accelerate. Few if any integrated circuits are produced by the major semiconductor manufacturers specifically for oscilloscopes, in the way that i.c.s are mass-produced specially for TV sets. The largest oscilloscope manufacturers have their own in-house i.c. facilities, often producing i.c.s in hybrid form, since in scope applications one is always seeking to wring the last ounce of performance out of every circuit. The same consideration is likely to ensure that certain sections of oscilloscopes will continue to be designed using mainly discrete components.

Two of the basic circuit "building blocks" used in oscilloscopes are shown in Fig. 13. The long-tailed pair is widely used in both forms shown, the second being especially common in analogue integrated circuits. It provides balanced push-pull outputs, even if only one input terminal is driven; i.e. it converts from unbalanced to balanced signals. This is an important function, as oscilloscope inputs are usually "single-ended" or unbalanced, whereas a push-pull or balanced drive is almost in-

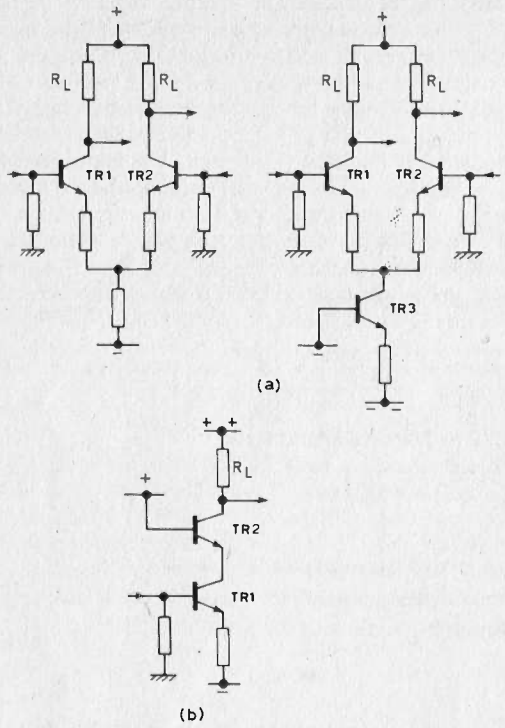


Fig. 13. Basic circuit "building blocks" commonly used in oscilloscopes: (a) long-tailed pairs; (b) cascode circuit

variably applied to the Y (and X) plates. The reason for this is simple. If balanced drive is used, only half the peak-to-peak voltage swing is required at each plate compared to the swing required for the case where only one plate is driven, the other remaining at a constant potential. Thus with balanced drive the supply voltage to the transistors driving the plates can be halved. With only half the voltage across each transistor, the current through it can be doubled without increasing its heat dissipation, which is important in the output stage of a deflection amplifier, as these transistors are invariably run very near the maximum permitted dissipation. With half the supply voltage and twice the current, the load resistor R_L will only be one-quarter of what it would have been for single-ended deflection, resulting in a substantial increase in bandwidth.

The cascode circuit (Fig. 13b) can be seen to consist of a common-emitter stage with a common-base stage as its collector load. This arrangement has two advantages. First, the maximum voltage that can be applied to TR2's collector is equal to the collector-base breakdown voltage V_{cb}, which for high-frequency transistors is often substantially higher than the common-emitter breakdown voltage V_{ce}, enabling a larger output voltage swing to be obtained from the stage. Second, there is inevitably, owing to the construction of a transistor, a capacitance of a few picofarads between its collector and base terminals, denoted C_{cb}. In the cascode circuit, the input capacitance at the base of TR1 is approximately $C_{cb1} + C_{be1}$ (where C_{be1} is the base-emitter capacitance of TR1), since the input impedance at the emitter of grounded-base stage TR2 is very low and there is therefore negligible signal voltage at TR1 collector. If a simple common-emitter stage were used in place of the cascode stage, the input capacitance would appear much larger, as the end of C_{cb} connected to the output would be changing in the opposite sense to the input voltage, by an amount greater than the input voltage swing. In fact, if the stage gain is A, the input capacitance would be approximately $C_{be} + (A + 1)C_{cb}$, the well-known Miller effect. If A is large it would prove difficult to drive the stage satisfactorily, a problem that is avoided by the cascode circuit.

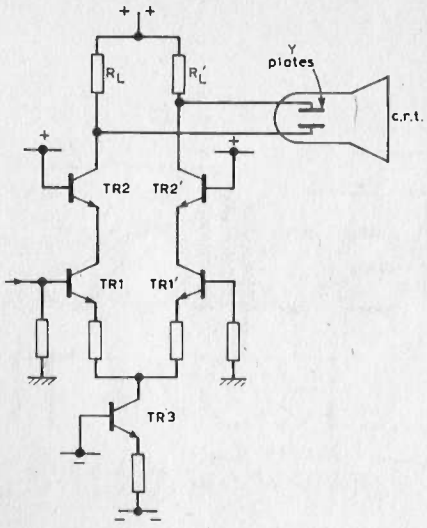


Fig. 14. Basic deflection-amplifier circuit

Y DEFLECTION AMPLIFIER

Oscilloscope designers frequently make use of the advantages of both the long-tailed pair and the cascode, as shown in Fig. 14. Here, the total output capacitance C_t shunting R_L is equal to C_{cb2} plus the load capacitance, several picofarads if this is a deflection plate of a cathode-ray tube. If both transistors have high cut-off frequencies, the −3dB bandwidth (70·7 per cent response) of the stage is given by $f_{-3dB} = 1/2\pi R_L C_t$, showing that for maximum bandwidth both R_L and C_t should be as small as possible. There is little the oscilloscope designer can do about the plate capacitance of the c.r.t., other than find another tube with the same sensitivity and lower plate capacitance if possible, but TR2 should have both a high collector dissipation rating and a low C_{cb}. Note that if TR2 is changed for another type with twice the dissipation rating, enabling the standing current to be doubled and R_L halved, the bandwidth would be increased even though the C_{cb} of the more powerful transistor were twice that of the original one. This is because C_{cb2} generally constitutes less than 50 per cent of C_t, which will therefore have increases by a much smaller factor than two.

INDUCTIVE PEAKING

A bandwidth greater than the above f_{-3dB} can be obtained by the use of inductive peaking circuits to offset the effect of C_t. Note that C_t includes the collector capacitance of the plate-driving transistor, the capacitance of the connecting lead to the plate, and the effective plate capacitance. The last is generally listed by the c.r.t. manufacturer as $C_{y1\text{-}all}$, meaning the capacitance of one Y plate to everything else *except* the other Y plate, and $C_{y1\text{-}y2}$, meaning the capacitance between the Y plates. The effective plate capacitance is $C_{pe} = C_{y1\text{-}all} + C_{y1\text{-}y2}$ if only one plate is driven, or $C_{pe} = C_{y1\text{-}all} + 2C_{y1\text{-}y2}$ if, as is usually the case, the two Y plates are driven in antiphase.

A deflection-amplifier output stage using shunt peaking is shown in Fig. 15a. If we define Q such that $Q = L/R_L^2C_t$, *then if* L is chosen such that $Q = 0{\cdot}25$ the pulse response of the stage will show no overshoot, while for $Q = 0{\cdot}414$ there will be 3·1 per cent overshoot. However, the rise time will be 71 per cent and 59 per cent respectively of that of the same stage without the inductive peaking. By using a capacitance $C = 0{\cdot}22C_t$ in parallel with a value of peaking inductance $L = 0{\cdot}35R_L^2C_t$, the rise time falls to 56·5 per cent of the uncompensated value and the overshoot is only 1 per cent.

The above are examples of "two-terminal" compensation networks; improved performance at the expense of increased

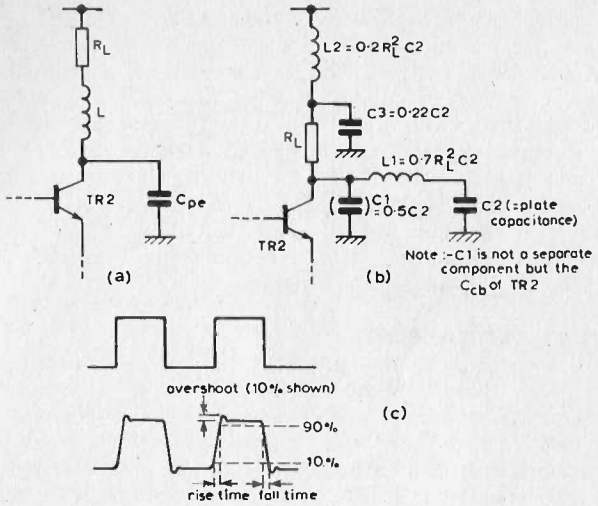


Fig. 15. Output-stage compensation: (a) simple two-terminal peaking; (b) four-terminal compensation; (c) rise time and overshoot defined

complexity can be obtained by splitting C_t into its component parts. C_{cb} and C_{pe} are compensated separately; the capacitance of the plate connection lead can be included with either of these two to help make up the relative values of capacitance shown in Fig. 15b. With this four-terminal peaking circuit, the rise time is only 40 per cent of that of the amplifier without compensation, and overshoot is less than 1 per cent. The improvement in frequency response is much less marked than the reduction in rise time, although if different L and C values are chosen a circuit can be produced with a frequency-response level up to 2·4 times the −3dB point of the uncompensated amplifier. However, this is of limited use in an oscilloscope as it shows a marked degree of overshoot on fast pulses. Overshoot is illustrated in Fig. 15c.

(The whole subject of peaking is covered succinctly in Chapter 9 of Electronic and Radio Engineering, *by F. E. Terman, McGraw-Hill, 4th edition, 1955, where an extensive list of further references can be found.)*

EMITTER COMPENSATION

With the inductive peaking schemes described above, the improvement in rise time over an uncompensated amplifier is independent of the amplitude of the displayed trace, and is limited to a factor of about 2·5:1 using a four-terminal compensation network. The trend recently has been to abandon inductive peaking of deflection-amplifier output stages in favour of emitter compensation.

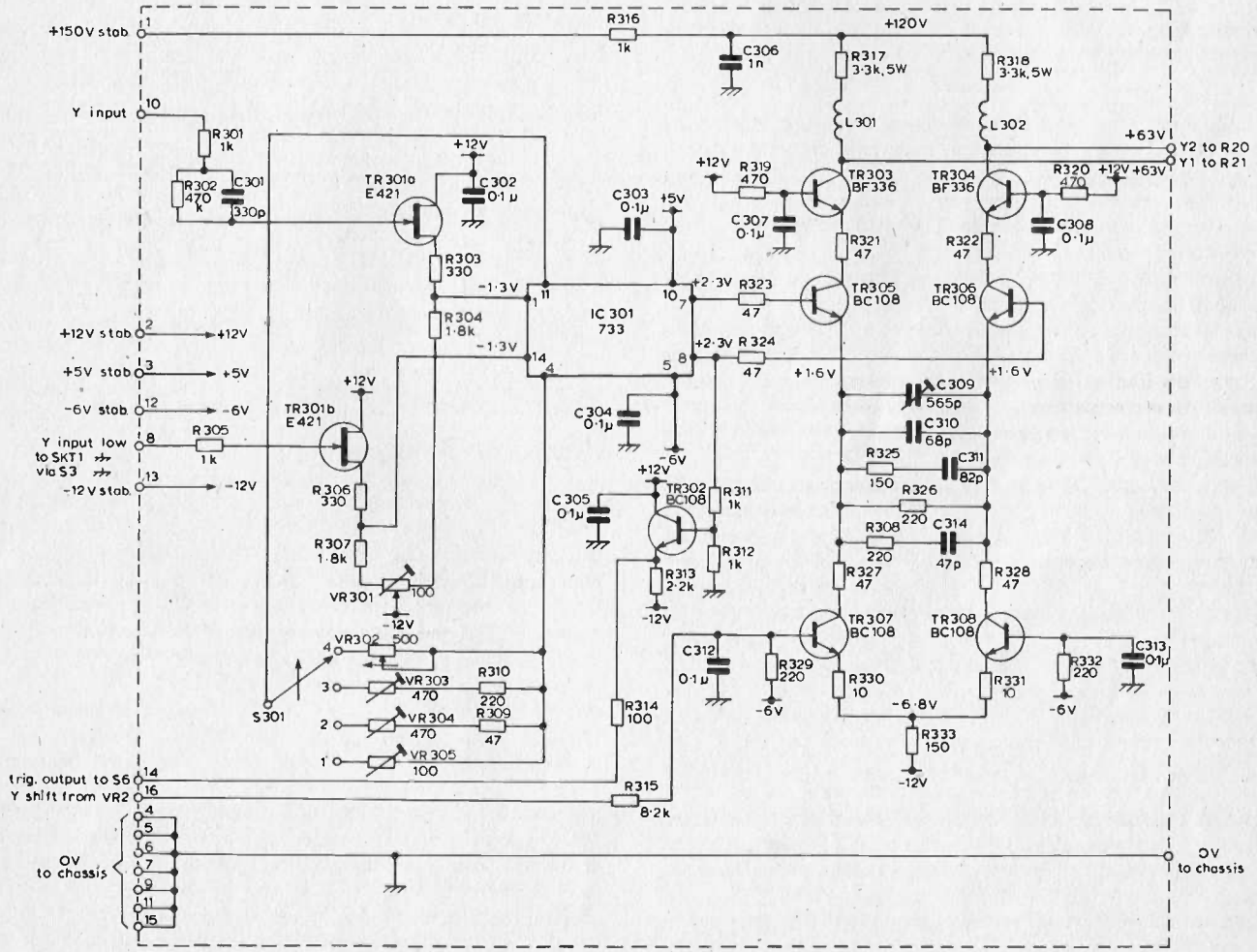


Fig. 16. Y-deflection amplifier designed by the author for use with c.r.t. type 3BP1

This scheme is exemplified in Fig. 16, which shows the circuit of a Y amplifier designed by the author for minimum rise time when using a 3BP1, an insensitive and very outmoded design of c.r.t., but cheap and readily available. Here, the gain of the output amplifier output stage at d.c. and over most of its frequency range is determined by R326, but at higher frequencies C309, 310 tend to bypass R326, resulting in a gain that rises with frequency, compensating for the loading effect of C_t. In fact, the gain of the amplifier transistors is also beginning to fall, with the result that it is not a simple RC load circuit that we are trying to compensate. Consequently, additional components R325, C311 and R308, C314 are included to ensure the smooth roll-off of the frequency response necessary for the faithful reproduction of pulse waveforms.

This type of circuit makes use of the fact that a deflection amplifier is always designed to be able to overscan the available screen display area by up to 100 per cent or more, so that the spot can be deflected way beyond the top or bottom of the graticule. When a very fast rising edge is applied to the Y amplifier, the long-tailed pair TR305, 306 will be overdriven, as their emitters are tied together by C309, 310. The result is that all the available tail current (set by R333; TR307, 308 serve only to introduce the Y shift voltage) is momentarily diverted through, say, TR305 while TR306 is cut off. The load capacitance C_t at each collector is therefore charged at the maximum possible rate set by the available tail current. As C_t charges, so do the emitter-compensation capacitors C309 and C310, resulting in the steady-state deflection being reached with minimal overshoot.

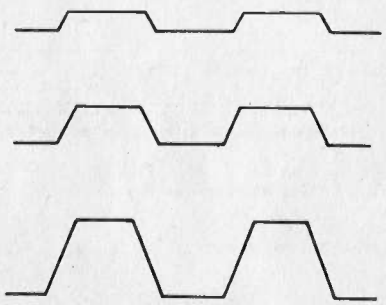


Fig. 17. Output of slew-rate limited amplifier for three increasing input amplitudes of an ideal square wave

This deflection amplifier is said to be "slew-rate limited" (Fig. 17), as the maximum speed at which the Y-plate voltage can change is determined by C_t and the magnitude of the tail current. Thus, in contrast to inductive peaking, with emitter compensation fast square waves are reproduced more faithfully when they are displayed at small amplitude than when displayed at full screen height. Likewise, the −3dB bandwidth is greater for small deflections than large; this explains the growing practice of quoting bandwidths at half-screen deflection, which might possibly be reasonable in the case of dual-trace instruments, but is really not fair in a single-channel scope.

INPUT ATTENUATOR

We have dwelt at some length on the Y amplifier because it determines the bandwidth and thus in large measure the usefulness of an oscilloscope. However, the other sections such as the Y input attenuator, trigger and timebase (sweep generator) departments are equally important, so let us complete the description of the Y deflection system by looking at the input attenuator.

The Y amplifier of an oscilloscope normally runs at a fixed value of gain, equal to what it provides on the most sensitive range. For the less sensitive ranges, the input signal is attenuated to bring it down to the same level as on the most sensitive range. Normally, wideband unbalanced variable attenuators are designed with a low, purely resistive characteristic impedance. However, as previously stated, for oscilloscope work a high input impedance (especially at low frequencies) is generally required, the standard value being 1M. At this impedance level the stray capacitance associated with the attenuator resistors, switch, etc., must be taken into account if the attenuation is to remain constant over a bandwidth of even a few megahertz, let alone hundreds of megahertz. This is achieved by absorbing the stray capacitance of the components into larger, deliberately introduced capacitances and then adjusting the latter so that the frequency response is constant.

A typical input attenuator such as might be found in an oscilloscope of 5 or 10MHz bandwidth is shown in Fig. 18. It is in fact that used in the Scopex 4S6 oscilloscope. It can be seen that each attenuator pad, e.g. the ÷ 10 position using R3 (900k) and R4 (effectively 100k owing to R9 plus R10 in parallel with it) has a capacitive divider CV4 and C3 in parallel. CV4 is adjusted so that its value is one-ninth of C3 + CV9 + the input capacitance of the Y amplifier. Thus the resistive and capacitive

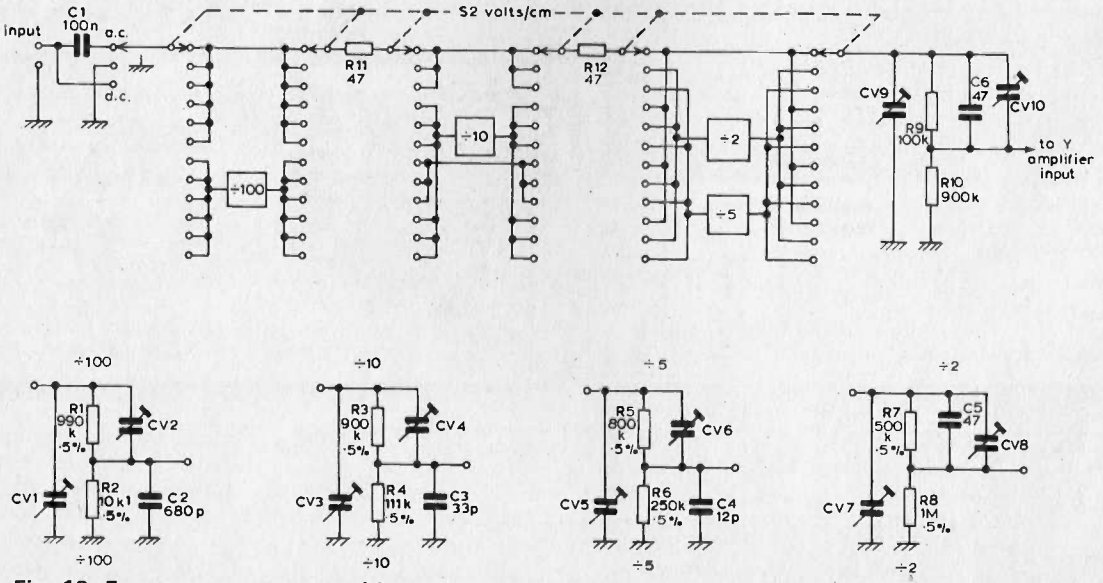


Fig. 18. Frequency-compensated input attenuator as used in the Scopex 4S6 *(courtesy Scopex Instruments Ltd.)*

division ratios are the same and the attenuation is independent of frequency. CV9 is used to set the input capacitance of the scope on the most sensitive range to a standard value, while CV1, CV3, CV5 and CV7 enable this same input capacitance to be achieved on all the other input ranges. This is important when using a passive divider probe. R9, C6 and CV10 protect the field-effect transistor forming the first stages of the Y amplifier from damage in the event of a large input at d.c. or low frequency being applied to the oscilloscope when on the most sensitive range, while passing high frequencies largely unattenuated. It is therefore important that large-amplitude signals at high frequencies, e.g. the output of a radio transmitter, should not be applied to an oscilloscope on the more sensitive ranges, as damage may result. It is also worth noting that the input impedance of an oscilloscope is not constant. At d.c. it is 1M, and virtually 1M up to a few hundred hertz. Thereafter, it becomes predominantly a capacitive reactance falling with increasing frequency, being typically only 4k at 1MHz.

The circuit of Fig. 18 is reasonably simple, but it will only perform satisfactorily if the layout is suitable, a comment that applies to the Y amplifier and indeed every section of an oscilloscope. Poor layout or construction in the Y input attenuator can result in partial shunting of the series elements of one pad by the unused components of other ranges. This will result in a non-constant frequency response, which will result in its being impossible to obtain a true square-wave response, except on the most sensitive range where no attenuation is in circuit. Needless to say, the attenuator shown in Fig. 18 and incorporated in the 4S6 oscilloscope is designed with intersection screens, to avoid such problems.

Due to lack of space the remainder of this feature describing Trigger, Timebase, X Deflection and Power Supply circuitry has been held over to next month.

FREE CASE PROJECT

MULTIMETER

PE Digital Precision Multimeter DP200

MARTIN KENT

USING the DPM200 panel meter, this compact multimeter with twenty-one ranges and six functions may be easily constructed with a minimum of additional components. It is also possible to achieve good accuracy without undertaking any calibration adjustments whereas the two input terminals ensure that the instrument is simple to use.

CIRCUIT DESCRIPTION

The panel meter module forms a 200mV full scale voltmeter and drives the liquid crystal display direct.

The versatile nature of the module ensures that function changing is straightforward to implement and a full list of ranges and the specification for the multimeter are listed below.

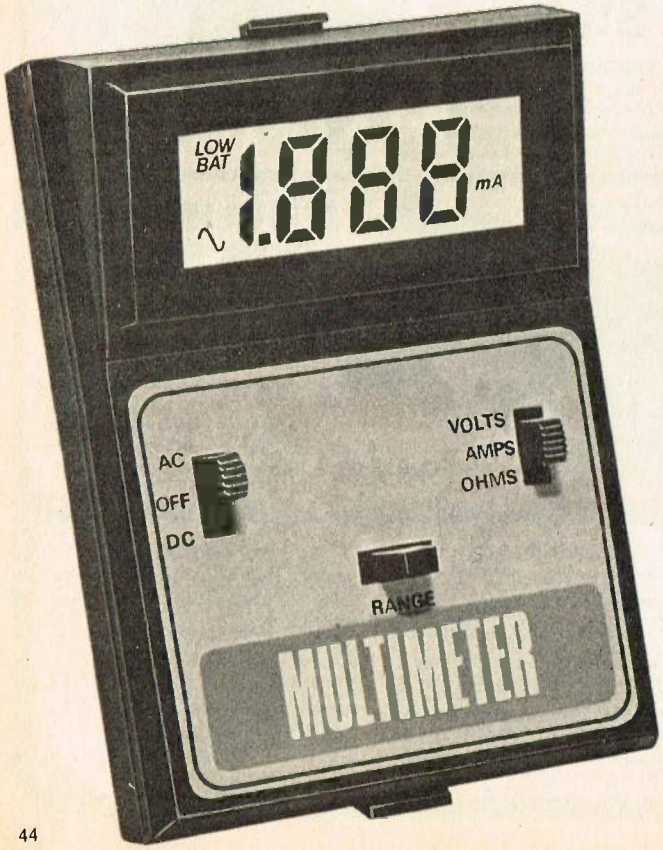
The circuit diagram of the DP200 is shown in Fig 1. Switch S3 selects d.c. or a.c. functions whilst connecting the battery to the appropriate circuitry via S3c and S3d. When the switch is in the centre 'off' position, S3a and S3b isolate the input to the module to prevent damage. Switch sections S1a and S1b route the input to voltage, current, resistance or diode check stages.

For the measurement of a d.c. voltage an input attenuator is formed by resistors R1 to R5 which are high stability metal film types. The attenuator settings ensure that each input range is reduced to 200mV full scale for input to the module. The input impedance of the multimeter is the standard value of 10 megohms and ensures that negligible current is drawn from the voltage source.

The voltage dependent resistor R6 is connected across the input terminals to clamp any transient high voltage spikes which may otherwise cause damage to the instrument.

When a current range is selected, S2b selects one of four shunt resistors R7 to R10, each of which should develop 200mV with full scale current input. The value of R10 is chosen to allow for the effect of switch resistance. A series chain configuration could have been used for current sensing but the low value resistors required could be difficult to obtain.

A 2A fuse protects against excessive input currents and diodes D1 and D2 protect the instrument from the application of high input voltages.



SPECIFICATION

Function	f.s.d.	Resolution	Accuracy	Protection
Volts (d.c.)	2V	1mV	0·5% ± 1 digit	500V for one minute
	20V	10mV	0·5% ± 1 digit	
	200V	100mV	0·5% ± 1 digit	
	500V	1V	0·5% ± 1 digit	
Current (d.c.)	2mA	1µA	0·5% ± 1 digit	2A/250V
	20mA	10µA	0·5% ± 1 digit	
	200mA	100µA	2% ± 1 digit	
	2000mA	1mA	5% ± 1 digit	
Volts (a.c.)	2V	1mV	1% ± 5 digit	500V for one minute
	20V	10mV	1% ± 5 digit	
	200V	100mV	1% ± 5 digit	
	500V	1V	1% ± 5 digit	
Current (a.c.)	2mA	1µA	1·5% ± 5 digit	2A/250V
	20mA	10µA	1·5% ± 5 digit	
	200mA	100µA	3% ± 5 digit	
	2000mA	1mA	6% ± 5 digit	
Resistance	2k	1Ω	0·5% ± 1 digit	260V r.m.s.
	20k	10Ω	0·5% ± 1 digit	
	200k	100Ω	0·5% ± 1 digit	
	2000k	1k	0·5% ± 1 digit	
Diode Test	2V	1mV	0·5% ± 1 digit	260V r.m.s.

**Please note the Front Cover and this photograph show the prototype Multimeter.*

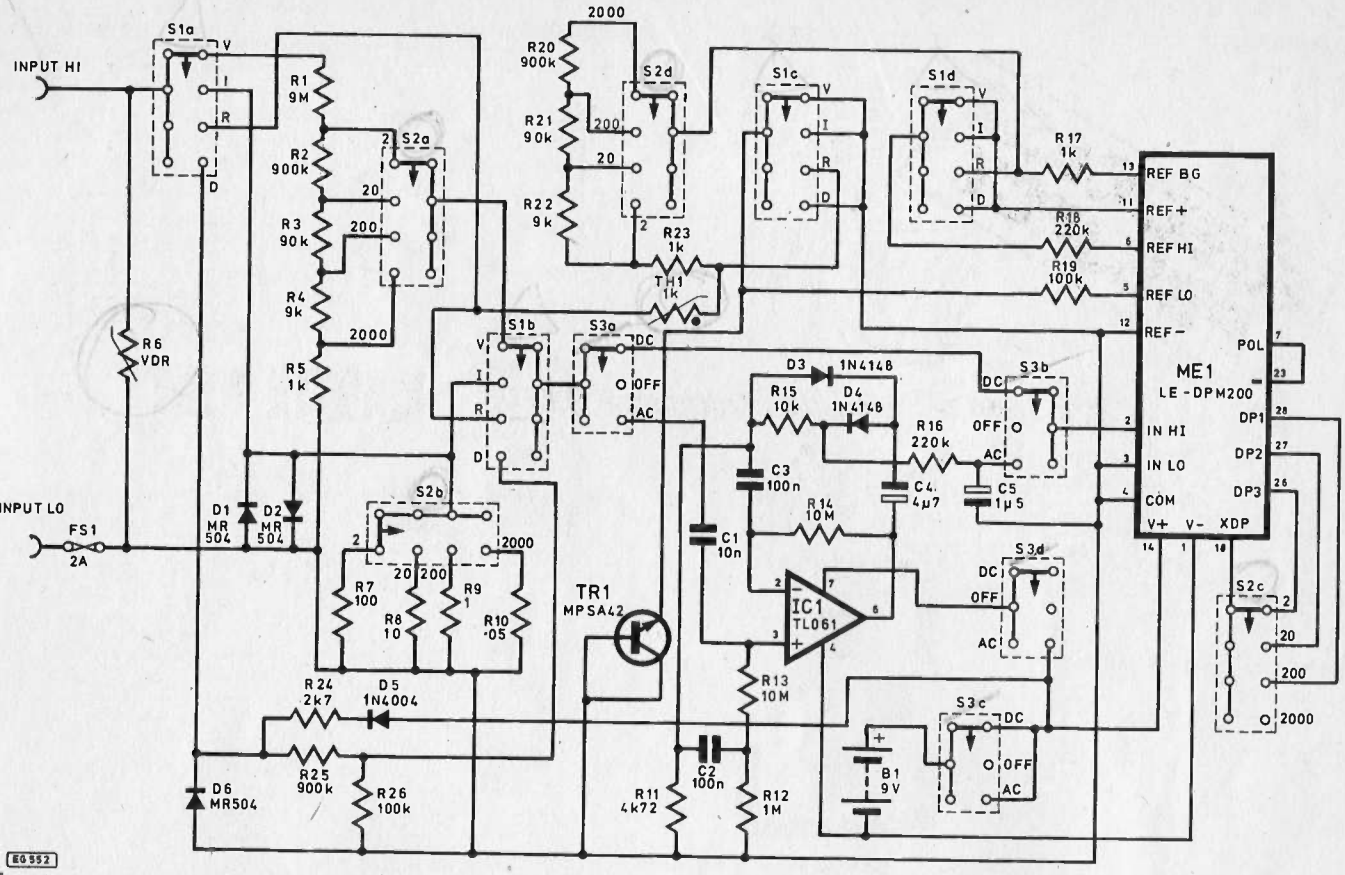


Fig. 1. Circuit diagram of the DP200 Multimeter

AC VOLTAGE AND CURRENT RANGES

When S3a selects a.c. functions the output from either the voltage attenuator or current shunts is fed through C1 to remove any d.c. component.

The operational amplifier IC1 is a TL061 connected as a precision rectifier. The j.f.e.t. input results in high input impedance and although the supply consumption is only 250µA, use of a.c. functions will more than double the multimeter's consumption. Diodes D3 and D4 rectify the alternating input and the positive component is sampled by R14 and filtered by R16 and C5. The circuit is mean sensing and calibrated to indicate the r.m.s. value of sine wave inputs by establishing the correct gain of the amplifier stage. The gain is set by R15 and R11 and use of the values indicated will eliminate the need for calibration. Alternatively, a 10k potentiometer could be substituted for R11.

RESISTANCE RANGES

In order to minimise the components required for resistance measurement and eliminate the need for calibration adjustment, a ratiometric method of resistance measurement is employed.

For all other multimeter functions, the bandgap reference within the module is employed and the 100mV output is connected to the module reference inputs via S1c and S1d. All inputs to the module are thus compared against the reference voltage. The arrangement for resistance measurement is shown in Fig. 2.

The 1·2V bandgap reference forms a stable voltage source which is applied across the reference resistor Rr and the unknown resistor Rx. The voltage developed across each resistor is dependent upon the ratio of the two resistors and the value of the unknown resistor may be read directly,

Reading=1000 Rx/Rr

Metal film resistors R20 to R23 are used as references. It would have been possible to use the resistors from the voltage attenuator as references but the resistors required are in reverse order to those for the voltage ranges, resulting

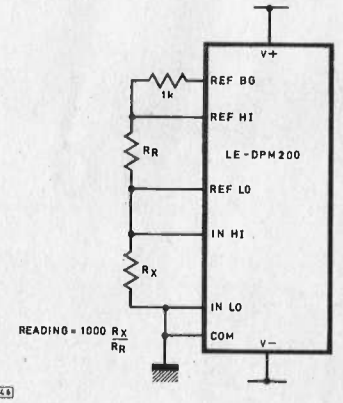


Fig. 2. Ratiometric method of resistance measurement

in the decimal points on the display being incorrectly positioned. Additional switch sections would be required to provide correct decimal point location and to isolate R5 from circuit common.

Resistance measurements should not be made on live circuits but protection against the application of high input voltages is provided. Thermistor TH1 has a nominal value of 1k at room temperature and transistor TR1 will turn on at approximately 10V to shunt the applied voltage. When TR1 draws current through TH1 the thermistor temperature rises and due to the positive temperature coefficient the resistance increases so limiting the input current.

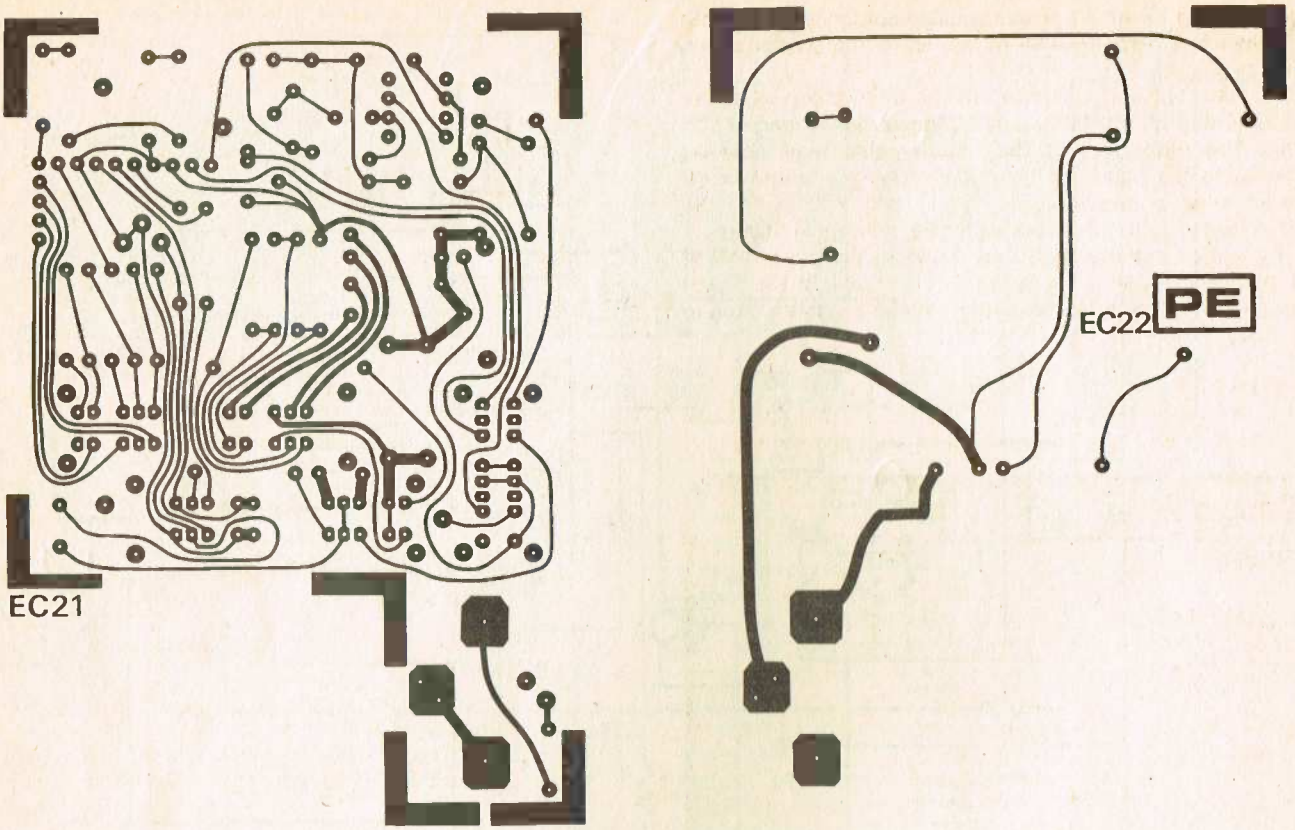


Fig. 3. Double sided p.c.b. design for the Multimeter

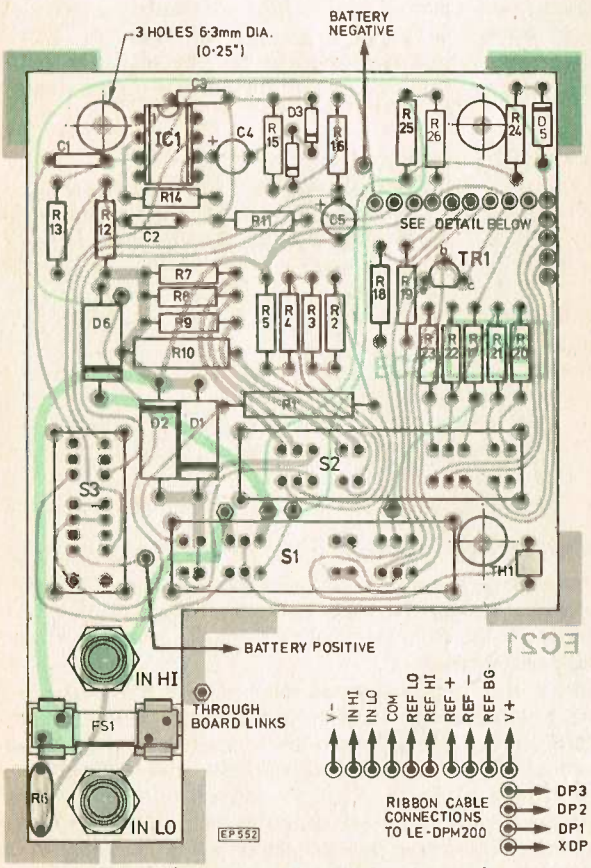


Fig. 4. Component layout for the p.c.b.

DIODE TEST

When a silicon diode is forward-biased into conduction the voltage drop across the device is approximately 0·7V. The 200mV full scale of the module is however too low to measure this voltage drop. When S1 selects Diode Test function, biasing from the battery is available via D5 and R24. When the applied diode is forward-biased the voltage drop will be attenuated by a factor of 10 by R25 and R26 to bring it within the measurement range of the module. If the 2V range is selected the decimal point will be correctly positioned on the display for direct readout of the diode voltage.

If the applied diode is open-circuit or reverse-biased it will not conduct and the display will be over-range. If the diode is short-circuit the display will read zero. Because of the accuracy of measurement available close matching of transistor Vbe can be carried out.

The diode test should not be made on live circuits but diode D6 will protect the instrument from the application of high negative input voltages which would otherwise be shunted onto the supply by D5. Positive input voltages are held off by D5 and safely attenuated by R25 and R26.

CONSTRUCTION

Construction of the DP200 multimeter is greatly simplified by the use of the panel meter which is supplied tested and calibrated.

Components should be checked against the component list and assembly commenced by soldering the through-board pins in place. As assembly proceeds, the solder pads on the top surface of the p.c.b. should all be soldered to ensure circuit continuity.

Solder the resistors and capacitors in place, followed by the diodes, transistor, and integrated circuit carefully noting the orientation of the latter. The three slider switches should

now be fitted to the p.c.b. and prior to soldering check that each switch is perpendicular to the board and pushed down as far as possible.

The fuse clips and fuse may now be fitted followed by the p.c. mounting terminals, battery connector leads, and ribbon cable. The other end of the ribbon cable may now be soldered to the panel meter module. Using a length of insulated wire, connect pins 7 (POL) and 23 (—) of the module together to provide drive for the polarity indication.

The switch cutouts should be made in the upper-half of the instrument case using the template shown in Fig. 5 and after checking the switch alignment the label can be fitted to the case.

TESTING

The testing of the instrument should be carried out before the case is fitted and after checking all the soldering the battery should be connected.

With the input switched to 20V d.c. the display should be 0.00 and the voltage between Input LO and battery positive should be approximately 2·8V. The voltage between pins 5 and 6 of the module should be 100mV. Apply a 10V input and check that the display reads 10.00.

Switch to 20mA d.c. and check the reading with a 10mA source connected.

Switch to 20k range and check that with the input open circuit the display shows a 1 in the most significant digit with the other three digits suppressed, which is the over-range indication. Connect a standard 10k resistor and check that the reading is 10.00.

With the instrument switched to 20V a.c. apply a 10V a.c. source and check the display.

The diode test function should be checked with a known diode and the reading should be approximately .700V with a silicon diode or .300V with a germanium diode.

FINAL ASSEMBLY

When the instrument has been tested the panel meter module should be located in the case cutout and the printed circuit board secured to the case by the self-tapping screws. Note the interior of the case should be modified as shown in Fig. 6.

Locate the PP3 battery in the moulded guides then clip the two halves of the case together. It will be found easiest to engage the clips at the display end of the case first.

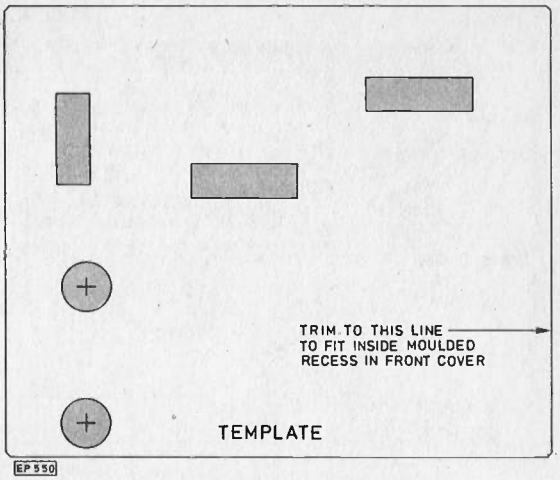


Fig. 5. Front panel template

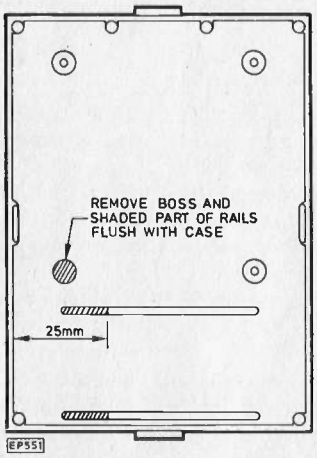


Fig. 6. Interior case cutting details

Components . . .

Resistors

R1	9M	
R2, R20, R25	900k (3 off)	Metal film 0·25%
R3, R21	90k (2 off)	
R4, R22	9k (2 off)	
R5, R23	1k (2 off)	
R6	VDR 400V	
R7	100 Metal film 0·5%	
R8	10 Metal film 0·5%	
R9	1Ω0 Metal glaze 2%	
R10	Ω05 Wirewound 2%	
R11	4k72 Metal film 0·25%	
R12	1M Carbon film 5%	
R13, R14	10M (2 off) Carbon film 5%	
R15	10k Metal film 0·25%	
R16, R18	220k (2 off)	Carbon film 5%
R17	1k	
R19, R26	100k (2 off)	
R24	2k7 Carbon film 5%	
TH1	Thermistor PTC 1k 260V a.c.	

Capacitors

C1	10n polyester 100V
C2, C3	100n polyester 100V (2 off)
C4	4µ7 elect. 16V
C5	1µ5 elect. 16V

Semiconductors

D1, D2, D6	MR 504 (3 off)
D3, D4	IN4148 (2 off)
D5	IN4004
TR1	MPSA 42
IC1	TL061 CP

Switches

S1, S2	4 pole 4 way slide (2 off)
S3	4 pole 3 way

Miscellaneous

ME1 panel meter LE-DPM200
Case
20mm p.c.b. fuse clips
20mm 2A fuse
PP3 battery and connector
4mm terminals
p.c.b.
Through board pins (5 off)
Ribbon cables

Constructor's Note

A complete kit of parts for the DP200 is available from **Lascar Electronics Ltd, Unit 1, Thomasin Road, Burnt Mills, Basildon, Essex. (Price £14·95 inc. VAT).**

PE DIGISOUNDER PART 2

BRIAN CURRIE

THE p.c.b. design for the display board is shown in Fig. 2.1, with the component layout shown in Fig. 2.2. This p.c.b. should be soldered first.

The p.c.b. mounting plug (PL1) should be inserted from the front of the board and is ultimately used to mount the display board at right angles to the main (mother) board. When soldering the plug in position, care must be taken not to allow solder onto the part of the pin surface which will mate with the socket on the mother board. The two soldercon pin sockets (SK3) used for mounting the l.c.d. should be fitted into the nylon nests and inserted into the p.c.b. After soldering the strips in place, the connecting bars may be broken off by gentle and gradual bending. IC7, should now be inserted and soldered in position, noting carefully its direction on the board.

When soldering is complete carefully check for short circuits. A fine-tipped iron is recommended as the joints are very close together. The liquid crystal display should be removed from its packing and gently inserted into the soldercon sockets. Note that two dots identify the left hand of the display (opposite pins 20 and 21 of IC7). The display pins are very fragile and it will be found easiest if one row of pins is located first, but not pushed in. The second row should now be located in the sockets and after checking all the pins are correctly lined, the display should be pushed in with an even all-round pressure.

This display board is now complete and ready for testing at a later stage.

MAIN BOARD

The main p.c.b. design is shown in Fig. 2.3, with the component layout shown in Fig 2.4.

All items plug directly onto the board with the exception of the transformer which has to be wound and assembled, so this should be done first.

When making up the transformer from the pot core kit, it is vital that the primary and secondary windings are wired to the correct pins as in Fig. 2.4. The primary and secondary can both be hand wound, with even, well tensioned turns. The primary (wound first) should consist of 3 turns of 22 s.w.g. (0·71mm) enamelled copper wire. The secondary should consist of 77 turns of 36 s.w.g. (0·22mm) enamelled copper wire. After winding the coils can be held in position by dipping the transformer in a suitable lacquer. The tuning core has little effect because of the very low Q factor of the transformer (due to the 4k7 resistor) and should just be adjusted to a central position. The enamel should be removed from the ends of the leads (approx. 10mm) and the transformer soldered into position.

The tinned copper wire links should now be fitted.

After all components are fitted and soldered, all the joints should be checked.

Finally the external wiring should be completed. The transducer output should be connected to the coaxial socket with a small piece of screened cable. The on-off-range

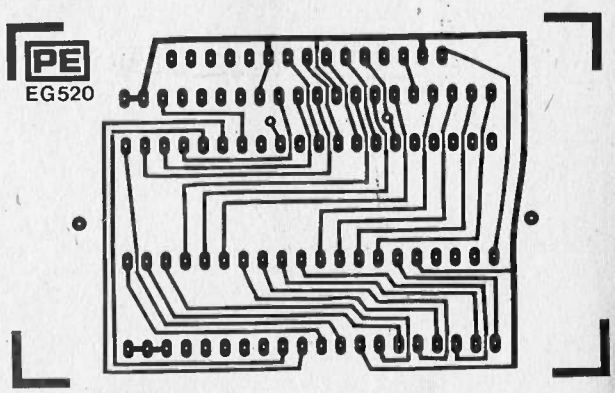


Fig. 2.1 Display board p.c.b. design

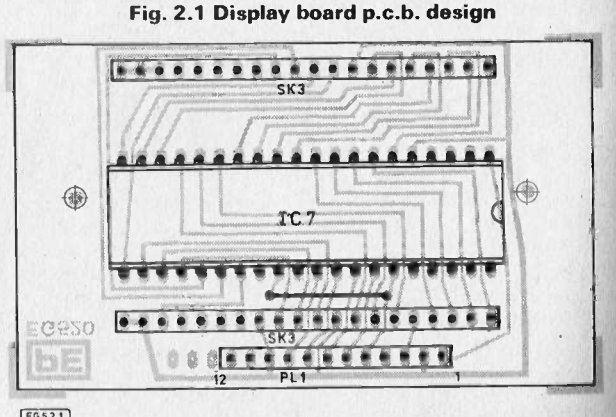


Fig. 2.2. Component layout for the Display Board

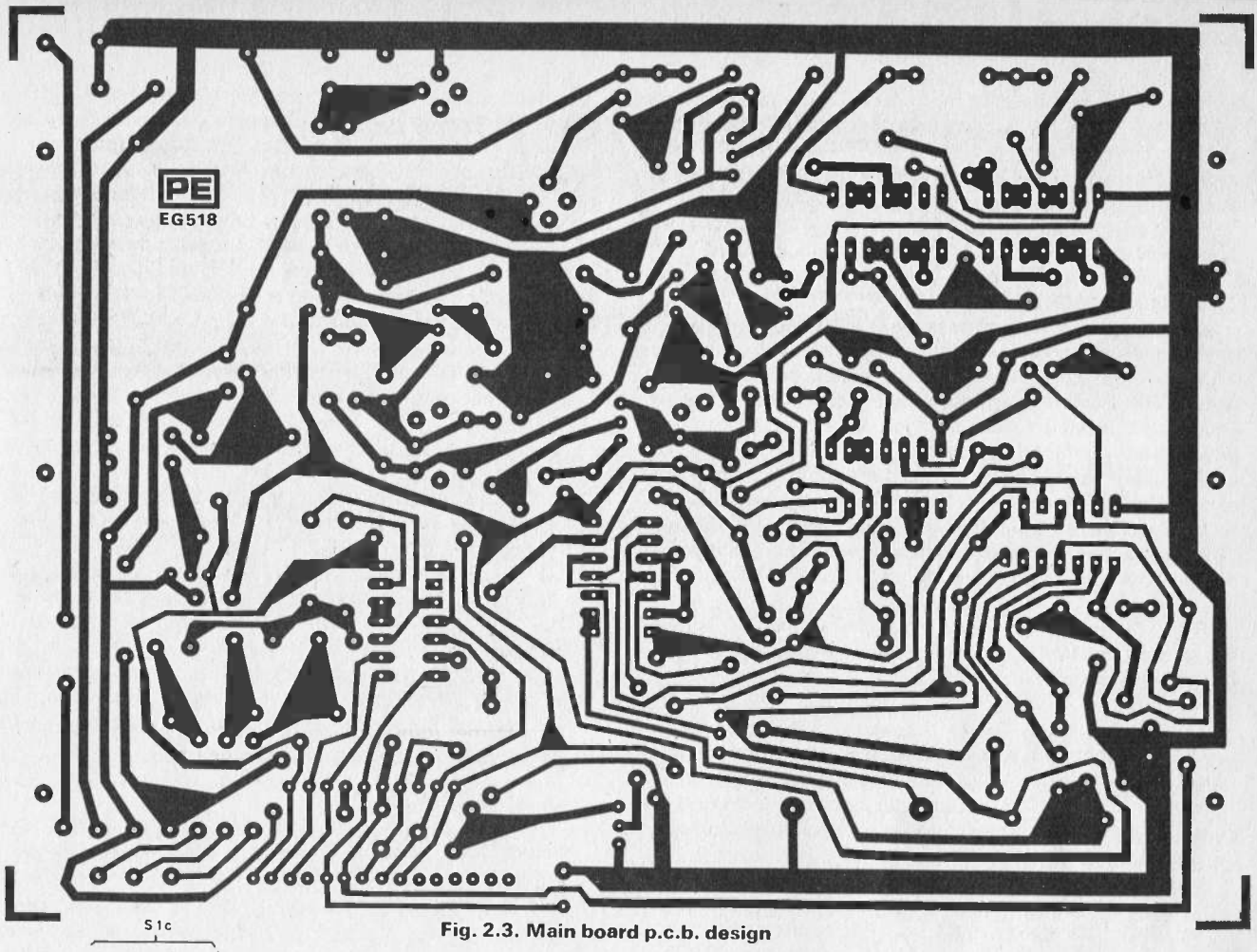


Fig. 2.3. Main board p.c.b. design

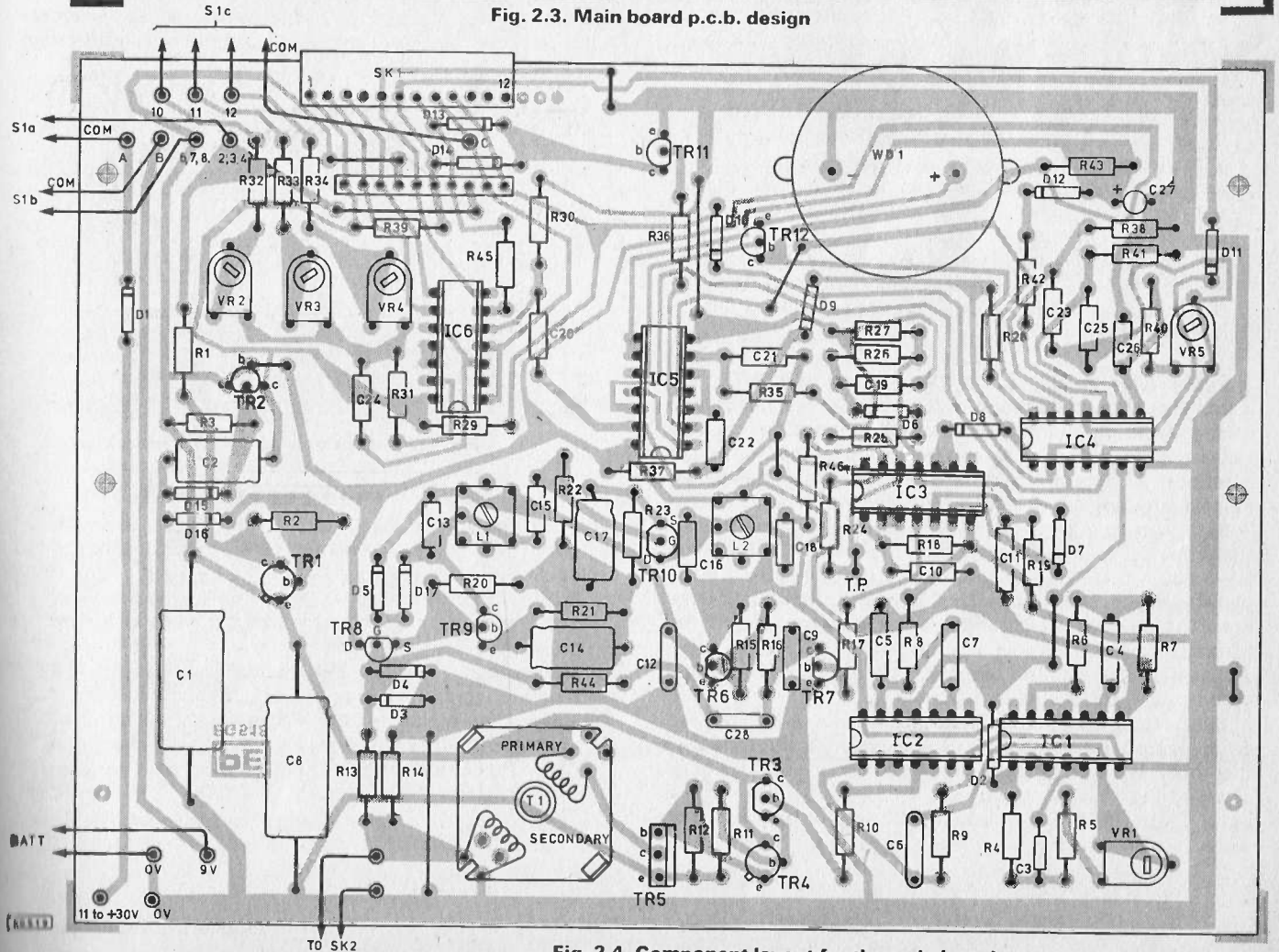


Fig. 2.4. Component layout for the main board

switch (SI) should then be wired up using suitable equipment wire. If it is decided to have connections at the rear for an external power supply, they should be fitted. If an internal PP7 battery is to be used then battery snaps should be inserted.

The display board should now be plugged into the main board and the unit is ready for testing and calibration.

TESTING, CALIBRATION AND FITTING

Although not strictly necessary, it is extremely helpful to have an oscilloscope available for testing and calibration. With the transducer disconnected, switch on power to the board. The audible warning device will sound for several seconds as capacitor C27 charges up. First check that the power supply is functioning and that the 5V and 9V rails are at the correct level. The i.c.s. 1 to 5 are run from the 9V supply, IC 6 and IC 7 are run on 5V. This system allows invertors to be used in the amplification stages and to drive tuned power amplifier and piezo sounder, which all run from 9V, but permits easy interfacing of the 7224 which runs from the 5V supply.

When the power rails have been checked then it is possible to start testing other parts of the circuit. The following order is suggested

(1) 1Hz oscillator. This is checked by looking at pin 8 on IC1 either with an oscilloscope or a high impedance multimeter. You should see the level changing between ground and 9V approximately once per second.
(2) Depth Oscillator—You should see pulses of approximately 35–250kHz at pin 4 of IC6. They may be checked with an oscilloscope or a frequency meter. The frequency should change depending on range selected. The approximate frequencies are as follows: feet—225kHz—meters 75kHz—fathoms 37kHz. However the oscillator will be set up accurately when calibrating.
(3) Counter and l.c.d.—This is best checked by feeding in the output from the depth oscillator previously checked. Hold the junction of D14 and R39 to ground and the counter should count rapidly. When this junction is returned to normal, the display freezes for up to 0·5 secs before resetting to zero.
(4) Gated Oscillator—This 150kHz oscillator should switch on for 500µ seconds once per second. Check the output at pin 6 on IC1 with oscilloscope or frequency meter.

The transducer should now be plugged into the rear of the instrument for system checks and setting up. It is possible to do final setting up in free air although the ultrasonic pulses travel at a different velocity and the 'range' of the instrument is reduced to approximately 4–6 feet. Place the transducer as accurately as possible at a right angle to a solid wall or floor, and exactly 1 metre (39·37") from it. Connect the oscilloscope to the transducer output (junction of R13 and R14) and adjust VR1 to give the largest possible 150Hz pulse envelope. (Approximately 400V peak to peak). You are actually tuning the oscillator to the resonant frequency of the transducer which although a nominal 150kHz, is often somewhat different. The transmitter is now tuned for maximum power, and optimum matching.

Please note that even when fitted into the boat, the lead on the transducer should not be subsequently shortened, as the matching will be upset. Now move the oscilloscope probe to the Test Point and set it to trigger on the transmit pulse. (Note: if the oscilloscope will not trigger on a 1Hz signal, the rate can be increased to 10Hz by temporarily connecting a 100k resistor across R7. Do not increase the sample rate beyond 10Hz). The smaller received pulse should appear approximately 6ms later. Slight adjustment of L1 and L2 is now permissible to tune for maximum pulse size.

As the transmitter and receiver are now tuned and matched to the transducer, the ranges can now be set up.

Set the range switch to 'feet' and with the transducer still 1 metre from the target adjust VR2 for a reading of 14·8 feet. Switch to 'meters' and adjust VR3 for 4·5 meters, and finally switch to 'fathoms' and adjust VR4 for 2·5 fathoms. These odd readings are the result of the different propagation speed in water, and when used in water will revert to the correct readings. The setting up can be done in water if required, but is rarely more accurate. This is because the velocity of the pulse varies with water temperature (5 per cent slower at 0°C than at 15°C in sea water) and salinity. These effects can sometimes be the cause of false readings, for example when river water meets sea water it tends to flow over the top. This can produce a reflective 'boundary'.

The final setting up of the alarm depth is best done in the water. Turn VR5 completely clockwise and sail the boat until the depth display indicates the required alarm depth. Turn VR5 slowly anti-clockwise until the alarm sounds. Three successive readings are necessary for alarm to activate. It will stop when you sail into deeper water. The alarm operates at the same actual depth, irrespective of range selected.

BOAT INSTALLATION

It is vital that the transducer is mounted properly so as to ensure good acoustic coupling to the water and at right angles to the seabed. Three methods are shown in Fig. 2.5.

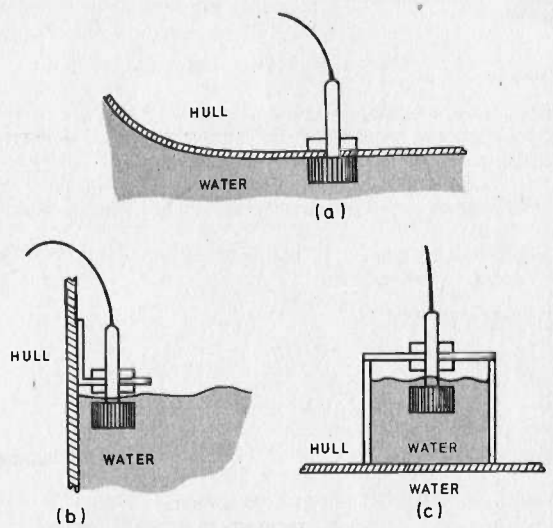


Fig. 2.5. Transducer mounting details

(a) Through the Hull—this is the most desirable method, but possibly the most difficult as a hole has to be drilled in the hull.
(b) On a Stern Bracket—this method can be useful on a sailing boat, but on a motor boat the propellor would probably cause false readings.
(c) Inside the Hull—if this method is employed, the transmitting surface should be below the bilge water surface, or below water in a specially constructed chamber. This method considerably reduces the range of the instrument and can only be used with wooden or fibre hulls. ★

We hope to publish a calibration unit for echo sounders in our July issue.

PATENTS REVIEW...

Copies of Patents can be obtained from: the Patent Office Sales, St. Mary Cray, Orpington, Kent. Price £1·25 each.

STEREO SOUND SYNTH

The RCA Corporation of New York has filed a European patent application (0 015 770) on a stereophonic sound synthesizer which is designed especially for use with TV receivers. Although Japanese TV stations now transmit some programmes in stereo, or bi-lingual sound, the Western world is several years behind in this respect. Moreover in the UK we are unlikely to see stereo sound with TV for many years because the BBC distribution network, which encodes the sound digitally and slots it into the sync pulse gaps of the picture waveform to enable both sound and vision to travel along a single link, cannot cope with full frequency stereo.

RCA proposes a two-loudspeaker receiver with circuitry to trick up mono into pseudo-stereo. Grundig in Germany is working along similar lines and a recent demonstration by Grundig of a pseudo-stereo TV receiver prototype backs up the RCA claim that synthesized stereo sound may even be better for TV than genuine stereo. It can be very unnatural to watch a small TV screen while hearing a wide spread of stereo which creates "off stage" sounds.

The RCA system, following work begun by Lauridsen of Danish Radio in 1956, creates a sensation of depth, presence and ambience but does not attempt to recreate directionality. Figure 1 shows the basic circuit. Mono sound signal M of full frequency range is split, and one half fed direct to the positive input of differential amplifier 40. The other half of the input signal is fed to circuit 20 with an amplitude response which varies with frequency. So the output of circuit 20 is sharply attenuated at specific frequencies and untouched at other frequencies. This "notched" output signal H (s) is now split. One half of the split signal constitutes a first output from the system (B) and the other half of the split signal is fed to the negative input of the differential amplifier 40. The output of amplifier 40, produced by subtracting notched signal H (s) from the mono signal, forms the second system output (C). This output is a complement of output B because it contains all the frequency components of the original mono signal which the output B lacks. Thus the entire sound spectrum of the original mono input is preserved in the two channels. But when they are separately reproduced through a stereo pair of loudspeakers the resultant sound field has artificial ambience created by the frequency distribution between channels.

Figure 2 shows a design for the transfer function circuit 20. Two twin-tee notch filters 200, 220 are cascaded. The first filter notches at 150Hz because the signal supplied by capacitor 206 leads the signal supplied by resistor 212 by 180° and self cancels. The second filter 220 notches in similar fashion at 4·6kHz.

The output of circuit 20 couples to power amplifier 42 and differential amplifier 40 by capacitor 112. To provide user control the input mono signal is coupled to amplifier 40 via resistor 104 and potentiometer 106. Pot 106 thereby adjusts the depth of the notches developed by amplifier 40.

Although the patented circuit is intended primarily for synthesizing stereo from mono TV sound, similar circuits are already in use by some record companies to reprocess mono recordings into stereo. This represents an improvement over the previous, and deplorable, technique of simply routing LF to one channel and HF to the other with added artificial echo.

Note incidentally that a copy of this European patent costs more than a UK patent because copying is charged at page rate.

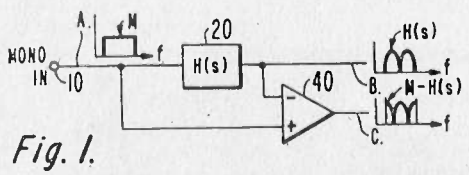


Fig. 1.

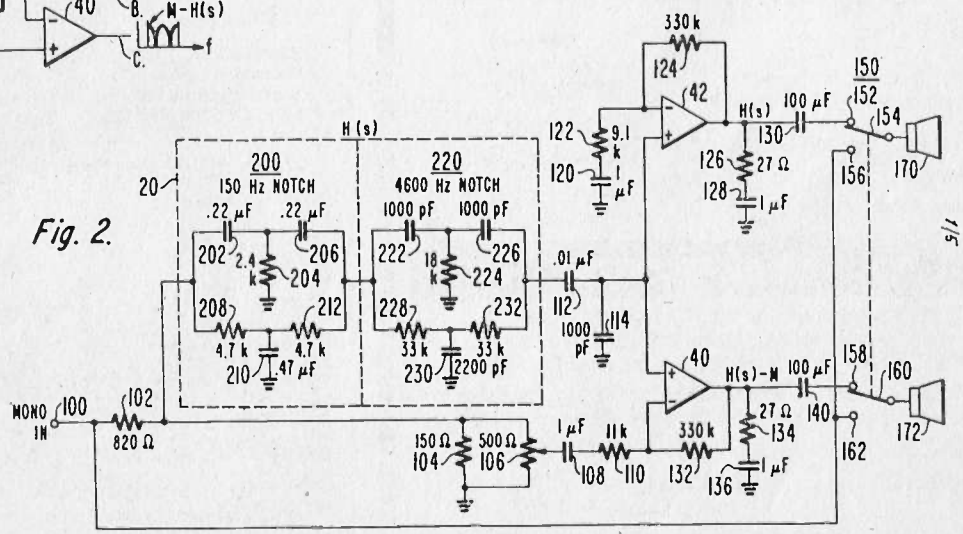


Fig. 2.

COURTESEY LIGHT DELAY

PHILLIP DAKIN

A SIMPLE AND EFFECTIVE VEHICLE INTERIOR LIGHT DELAY

THE device to be described here, is a simple circuit using one of the latest VFET transistors and the minimum of components. The circuit provides a maximum delay of 30 seconds on a vehicle's interior light, and has the added facility of an ignition inhibit.

CIRCUIT DESCRIPTION

The circuit operation is based on the characteristics of the VFET VN66AF manufactured by *Siliconix*. A VFET, unlike most semiconductors, is not current controlled, but voltage controlled. The voltage applied between the Gate and the Source of a VFET will determine how much current will flow between its Drain and Source; the greater the voltage the greater the current, until the impedance of the load limits this current. The great advantage of these devices (besides a high input impedance Gate to Source), is their low "on" resistance, in this case approximately 2 ohms with 12 volts Gate to Source.

Fig 1 shows the full circuit diagram, and it operates as follows: Assume the vehicle's doors are closed, that is S1 and S2 are open. Capacitor C1 is charged to the supply voltage via LP1 and D3. The transistor TR2 is turned full on via LP1, D2, R3 and R4. TR2 conducting keeps the gate of TR1 at zero volts, preventing TR1 from passing current. When a door is opened S1 or S2 closes so lighting the lamp LP1, but because point A is now at zero volts, TR2 is turned off, and D3 reversed biased because of the potential stored on C1. This potential is the gate voltage for TR1, which allows it to conduct when both S1 and S2 are opened by closing the doors. Because TR1 is a voltage controlled device, no current flows into the gate of TR1, therefore C1 will discharge via R2 and R1. As C1 discharges the voltage across R1 decreases exponentially, slowly turning off TR1. This action produces a small increasing volt drop across TR1 which is monitored by TR2 via D2, R3 and R4. When the potential difference across TR1 reaches approximately 1·5 volts, T2 will be turned on, pulling the gate of TR1 to zero volts, turning it off, and extinguishing the lamp LP1. The time taken for this to happen is approximately 30 seconds with the components shown.

However, if during this time the ignition is activated, TR2 is turned on, again pulling the gate of TR1 to zero volts, turning off the interior lamp.

With the ignition circuit activated the time delay is inoperable, but the lamp will light normally when a door is opened. This avoids the possible distraction of having the interior lamp on for a short time whilst the vehicle is being driven. When leaving the vehicle, the ignition must be turned off before the door is opened, otherwise TR1 gate will remain at zero volts; point A being zero volts, and TR2 turned on via the ignition, therefore discharging C1 via R2.

Diode D1 is high voltage protection, and will prevent excessive voltages on C1 and TR1. Reverse polarity protection is inherent in TR1 because a VFET acts as a low impedance with a negative potential Drain to Source. D2 and D4 are to prevent intercircuit action from the lamp supply to the ignition circuit and vice versa.

CIRCUIT CONSTRUCTION

Figs 2 and 3 show a simple p.c.b. layout. No components are critical, but if a shorter delay is required, C1 can be reduced appropriately. If longer times are required, increase

C1 or R1 as necessary. If TR1 is substituted for a similar device, the ratio of R3, R4 may have to be adjusted. The circuit is designed for use with one 6 watt 12V lamp only. Two 6 watt lamps produce too large a volt drop across TR1, immediately turning on TR2, so cancelling the delay. A heatsink is shown for TR1 but it is really only required if the time delay greatly exceeds 30 seconds, or the unit is mounted in such a position that the VFET will get warm.

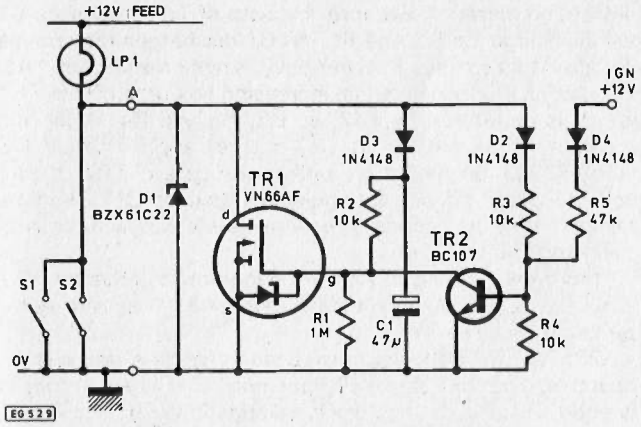


Fig. 1. Complete circuit diagram

TESTING AND HOUSING

The unit can be tested using a spare 6W 12V lamp and a 12 volt supply, but first, before any connections are made, check all component values and their orientation. When the circuit functions correctly, it may be contained in any suitable box or housing.

INSTALLATION

This is fairly simple and straightforward on most vehicles. A convenient position should be found for the unit near a door switch connection and a switched ignition supply. The wiring circuit is shown in Fig. 4. Take the lamp/switch connection to the door switch, usually a Violet/White cable and the ignition connection to a switched ignition supply, usually a White cable. If you are in doubt of your vehicle's wiring colours, consult the vehicle handbook or workshop manual. The unit is virtually indestructible: if the lamp/switch connection is inadvertently connected to the supply in some way,

COMPONENTS . . .

Resistors

R1	1M
R2, R3, R4	10k (3 off)
R5	47k
All resistors 0·25 watt 5%	

Capacitors

C1	47µF/25V

Semiconductors

TR1	VN66AF (Siliconix)
TR2	BC107 or equivalent
D1	BZX61C22 or equivalent
D2–D4	1N4148 or 1N916 (3 off)

Miscellaneous

P.c.b. 46 x 46mm
Heat sink 20°C/watt
0·25" p.c.b. spade connectors

TR2 is turned on preventing TR1 from conducting. A good safety feature!

When connected, check the operation of the unit and fix permanently in place.

The unit will now provide you with light to find the ignition lock, and fasten your seat belt without having to grope in the dark! ★

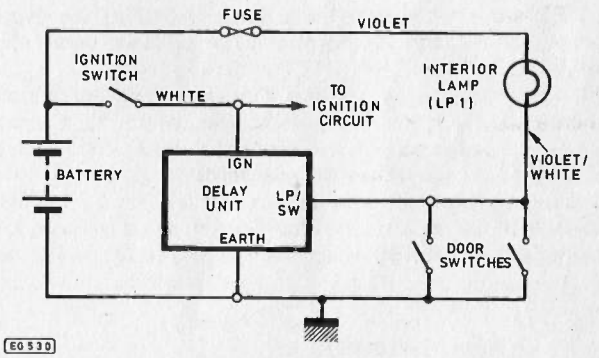


Fig. 4. Wiring diagram

Fig. 2. Printed circuit design

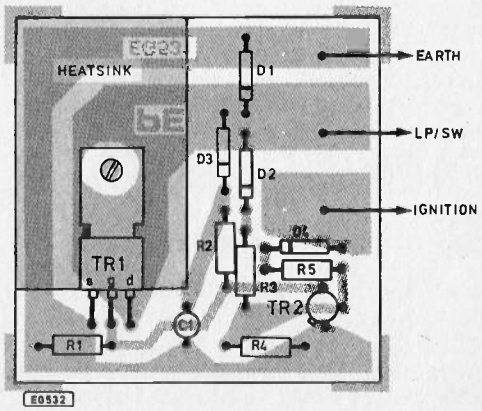
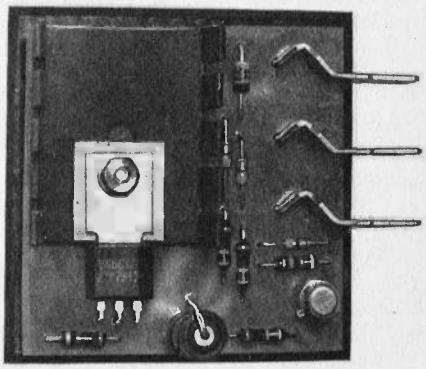


Fig. 3. Component layout



600 BAUD CASSETTE INTERFACE

By P. MARTIN

THE COMPUKIT as supplied has a 300 Baud cassette interface which performs very well.

This article describes the hardware required to uprate your Compukit's interface to 600 Baud, without modifying it other than the addition of three i.c.s on a small board with five connections. No printed circuit tracks have to be cut.

The modification is designed so that you can use the original 300 Baud or 600 Baud. This means that original tapes at 300 Baud can still be used.

CIRCUIT OPERATION

The clock for the serial interface is derived from the divider chain, and for a Baud rate of 600, C2 needs to be used instead of C3. This is done by IC1. When the Select line is low then C2 is selected. Since the output tones are derived from the ACIA clock when the clock is doubled in frequency the output tones will also double in frequency. This will be a problem with many cassettes as their frequency response drops off quite rapidly after 6KHz. To overcome this, IC2 is used to divide the output tones by 2 when using the higher clock rate. IC3 is used to switch this stage.

CONNECTION TO THE COMPUKIT

There are 5 connections to make to the computer:

1) C1
2) C3
3) Input to IC57 (Pin 2)
4) Q output from IC64 (Pin 11)
5) Output to the cassette jack

Fig. 1 shows where to pick off the C2 and C3 signals. The input to IC57 and the output from IC64 are done in the same manner.

Remove the i.c. from its socket and very carefully bend the required pin to a horizontal position. Put the i.c. back into its socket and solder the required wire to the pin. The output to the cassette can be made directly to pin 9 of J2.

If you find that you have problems with the new interface, it may be that the value of R53 is not correct, and it will need to be changed. The correct value may be found by replacing R53 with a 22k preset pot, and adjusting it to get zero errors on loading a program.

FURTHER MODIFICATIONS

Since the input for 300/600 Baud operation is a single TTL level input by using a simple interface such as a PIA chip, the Baud rate can be controlled by software; this may have applications where you have a cassette file-keeping system using tapes recorded at both speeds.

The second modification concerns even higher Baud rates, and this is where you may run into problems.

The first problem is that standard hardware is not reliable above 1200 Baud due to several factors; the main ones being:

1) The signal generated by the cassette interface is not a sinewave, but an integrated square wave. During playback this contains many high harmonics which during the detection stage can interfere with the wanted signal.

2) The receive circuitry introduces jitter which makes it hard for the monostable to quickly decode the signal.

The answer to the above is a better interface using, for instance, synthesised sinewaves and a phase locked loop detector.

The second major problem when using a high speed interface is the software not being able to keep up with the incoming data. The prime villain is the interpreter, which after it receives a carriage return decodes that line into token symbols, finds where to put it into memory, and then inserts that line. All this takes

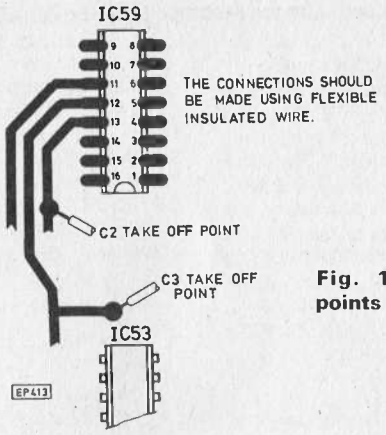


Fig. 1. The pick-off points for C2 and C3

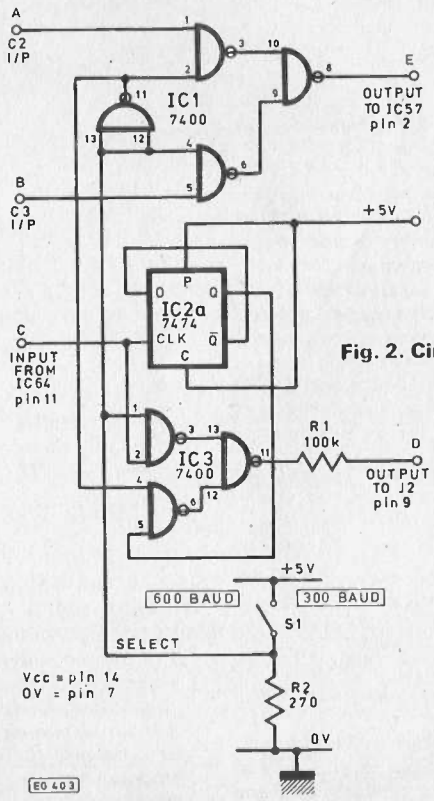


Fig. 2. Circuit diagram

time, and if the interface is delivering another line during this operation then data will be lost. To overcome this the standard Compukit outputs 10 null characters after each carriage return, which gives the interpreter time to do its chores. At higher Baud rates you must provide for more nulls to be printed. One way of doing this is to POKE 13 with the number of nulls you want printed.

CONCLUSION

I have been using this modification for several months now with very good results, and it has certainly made keeping programs on cassette easier. The present Baud rate of 600 is about the highest you can go without substantial modifications to your Compukit and I hope that the problems I have outlined will help those who want a faster interface.

MICRO PROMPT

The hardware and software exchange point for PE computer projects

MAKE THE MOST OF USR

Sir—Although readers will know that Y = USR(X) transfers control from BASIC to a machine code routine on the UK101, many may not realise that parameters may also be passed back and forth between BASIC and machine code using this function.

Executing Y = USR(X) puts the value of X in the floating accumulator. On returning to BASIC with an RTS, the number in the floating accumulator is assigned to Y. Therefore, by changing the contents of the floating accumulator before returning to BASIC, a new function can be implemented.

The floating accumulator is a group of zero page locations at $AC to $BO. X is put there as a floating point number:

$ AC Exponent
$ AD-$AF Mantissa
$ BO Sign

Although this is useful for implementing certain functions—for instance new mathematical functions—most applications require values to be passed from BASIC to machine code as two byte hex numbers. Whereas this can be achieved by POKING the number into a memory location before entering the m.c. program, transferring numbers above 255 becomes messy and slow. Luckily a subroutine resides at $AE01 which converts the floating point number in the floating accumulator to a two byte hex number. This number is returned in $AE (high byte) and $AF (low byte). Hence, to transfer X to a machine code program as a two byte number in $AE. $AF:

POKE 11, 34: POKE 12, 2: X= USR(X)
Location

Machine Code:

Ø222	*JSR $AEØ1*	*2Ø Ø1 AE*
	Main routine	
	RTS	*6Ø*

Unfortunately, the subroutine at $AEØ1 jumps to BASIC if X is larger than 2^{15} (32768) with a "function call" error. One of the main uses of the USR(X) function would be in passing video RAM addresses to machine code routines to provide fast dynamic screen layouts, such as in LIFE and Space Invaders type games. The video RAM is at DØØØ—D3FF (53248—54271), and so the above problem must be overcome. The simplest solution is to subtract 53248 from X before X = USR(X), then to add it on again in the machine code program, as shown below.

```
100 REM TRANSFER VDU PIXEL AD-
DRESS TO A MACHINE
200 REM CODE ROUTINE. X= ADDRESS
300 A = 53248: POKE 11, 34: POKE 12,
02
400 . . . . Main Program. X defined here
.
.
.
1000 X = USR (X – A)
1100 REM (PIXEL ADDRESS—DØØØ)
NOW IN FLOATING ACCUMULATOR.
LOCATION

Ø222 JSR $AEØ1 20 Ø1 AE;  Convert to
                           Double Byte
CLC          18
LDA $AE      A5 AE;        Add $DØ to
                           high byte
ADC $ DØ     69 DØ
STA $ AE     85 AE;        Replace in $
                           AE
.                          Result hi $AE
.
.                          lo $AF
Main program               Video address
RTS          6Ø;           now in $AF,
                           $AE.
```

T.D. Allen,
Poole,
Dorset.

AUTO LINE NUMBER

Sir—I enclose a listing of a program I have written which you might like to print in your Micro Prompt series.

This program automatically outputs the BASIC line numbers, followed by a space. This is done by pressing Control–N instead of Return, at the end of each line. The program as printed uses a start line of 100, with an increment of 10. These can easily be changed by suitable POKEs. The program is loaded via BASIC into the "free RAM" area of the UK101. The current line number and the increment are each stored as three pairs of BCD digits, at locations 570–575 (023A–023F hex). Six zero page locations are used for two indirect pointers, and two temporary stores at addresses 240–245 (00F0–00F5).

If the new CEGMON monitor is used line 9110 should be changed from . . . . 186, 255,201,14 to . . . . 70,251,201,14.

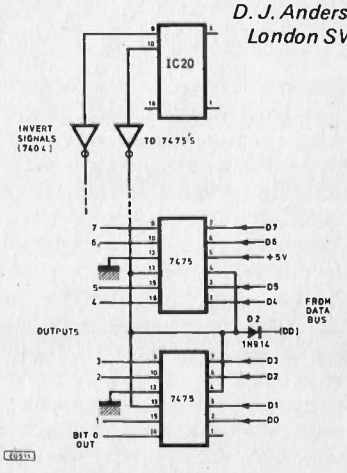
A. Scott,
Ashtead,
Surrey.

```
9000 REM  AUTO-NUMBER
9010 REM  BY A. SCOTT
9020 REM  19/11/80
9030 FORI = 570TO667
9040 READJ:POKEI,J:NEXT
9050 POKE240,58: POKE241,2
9060 POKE242,61:POKE243,2
9070 POKE536,64:POKE537,2
9080 ?"AUTO-NUMBER READY":?
9090 ?"PRESS CTRL-N TO OUTPUT
     LINE NUMBER"
9100 NEW
9110 DATA0,1,0,0,0,16,32,186,255,
     201,14
9120 DATA240,3,76,153,163,169,84,
     141,24
9130 DATA2,169,13,76,153,163,169,
     3,133
9140 DATA244,160,0,132,245,169,
     108,141
9150 DATA24,2,177,240,74,74,74,74,
     9,48
9160 DATA76,153,163,169,124,141,
     24,2
9170 DATA164,245,177,240,41,15,9,
     48,76
9180 DATA153,163,230,245,164,245,
     198
9190 DATA244,208,216,160,2,24,
     248,177
9200 DATA240,113,242,145,240,136,
     16,247
9210 DATA216,169,64,141,24,2,169,
     32,76
9220 DATA153,163
```

LOW COST I/O

Sir—I have found a cheap way of providing two 8 bit latched outputs from my UK1Ø1. At present, IC2Ø is a 74138, which is used to decode the video RAM and keyboard latch. It also will decode two other memory blocks at D4ØØ (pin 9 of IC2Ø) and D8ØØ (pin 1Ø of IC2Ø). These pins are normally high, but go low when data is written to the above addresses. These signals from IC2Ø can be used to control data latches, receiving data from the data bus. I used two pairs of 7475s. These are arranged like IC2 and 3, taking care to remember to invert the signals from IC2Ø. The latches can have information POKEd in from BASIC, using locations 53272 and 55296 (pin 9 and 1Ø latch control signals). I intend to use the data from one of the latches for automatic tape recorder control, but at present they are still flashing l.e.d.s!

D. J. Anderson,
London SW4.



It should be emphasised that material presented in Prompt has not necessarily been proven by us. Neither can compatability with *all generations* of the computer equipment to which it relates be guaranteed.

Software and hardware designs submitted should be accompanied by a declaration to the effect that it is the original work of the undersigned, and that it has not been accepted for publication elsewhere.

MEMORY CHECK

Sir—I am writing to tell you of a useful technique for Compukit machine code programming. When writing a m.c. program it is usually best to write it such that it may be run in any part of the RAM. This is often impossible because the program may modify its own instructions. An example is a RAM check program which should check every byte possible by storing a value in it and then recovering the value and checking it has not changed. If this program tried to check the RAM in which itself was stored it would go wrong. To get round this problem you must write a program which can find its own start address so it knows where it is in the RAM, and can avoid itself.

This can be done by executing a "JSR" and then decrementing the stack pointer twice and then reading from the stack the return address of the "JSR" previously executed.

```
JSR     FEC9
TSX
DEX
DEX
TXS
PLA
STA     $Ø3
PLA
STA     $Ø4
```

"FEC9" is a location in the monitor which contains "6Ø" (RTS). The above program would put the address of the last byte of the JSR FEC9 instruction into stores 'Ø3' (High port) and Ø4 (low port). After executing this routine the stack will be unaffacted.

What follows is a fully relocatable RAM check program.

This program can be located anywhere from ØØØ5 up. It will check every byte except for ØØØØ to ØØØ4 and the RAM which it is stored in. To check the RAM to see that every bit cell will set to "1" and "0" it stores 10101010 and then 01010101 in each byte. The program runs through until it meets on error (the end of the RAM if your 2114's are okay). The program will display the first non reacting byte's address using the monitors output routine.

The contents of each byte is restored after checking.

The program runs as a subroutine and will return whatever it found. The only stores affected by running are ØØØ1-ØØØ4 and ØØFE, ØØFF.

Chris Dunning,
Bristol.

ADDRESS	HEX	NEMONIC
0300	20C9FE	JSR $FEC9
0303	BA	TSX
0304	CA	DEX
0305	CA	DEX
0306	9A	TXS
0307	68	PLA
0308	8503	STA $03
030A	68	PLA
030B	8504	STA $04
030D	A900	LDA $00
030F	A8	TAY
0310	8502	STA $02
0312	A905	LDA $05
0314	8501	STA $01
0316	A504	LDA $04
0318	C502	CMP $02
031A	D013	BNE $032F
031C	A503	LDA $03
031E	C501	CMP $01
0320	D00D	BNE $032F
0322	18	CLC
0323	A501	LDA $01
0325	6970	ADC $70
0327	8501	STA $01
0329	A502	LDA $02
032B	6900	ADC $00
032D	8502	STA $02
032F	8101	LDA ($01),Y
0331	8500	STA $00
0333	A900	LDA $00
0335	9101	STA ($01),Y
0337	D101	CMP ($01),Y
0339	D025	BNE $0360
033B	A955	LDA $55
033D	9101	STA ($01),Y
033F	D101	CMP ($01),Y
0341	D01D	BNE $0360
0343	A9AA	LDA $AA
0345	9101	STA ($01),Y
0347	D101	CMP ($01),Y
0349	D015	BNE $0360
034B	A9FF	LDA $FF
034D	9101	STA ($01),Y
034F	D101	CMP ($01),Y
0351	D00D	BNE $0360
0353	A500	LDA $00
0355	9101	STA ($01),Y
0357	E601	INC $01
0359	D002	BNE $035D
035B	E602	INC $02
035D	18	CLC
035E	90B6	BCC $0316
0360	A501	LDA $01
0362	85FE	STA $FE
0364	A502	LDA $02
0366	85FF	STA $FF
0368	20ACFE	JSR $FEAC
036B	60	RTS

EDITOR CUT

Sir—Having now completed the cutting down of the UK101 BASIC SCREEN EDITOR I feel you may care to publish it.

The program now uses 210 bytes (rather than the original 325) and uses locations $FB to $FF as temporary stores—these locations are also used by the reset routine.

The program is poked into locations from $022F to $02FF so does not use any BASIC workspace and also survives a Reset/cold start only needing the two appropriate Pokes.

Having spent about 50 hours cutting this program down I would like to see it made available to other enthusiasts who still have the original monitor.

Incidentally, the RUBOUT key will no longer give line feeds—it can be returned to the original program logic by making line 80, 4th DATA number 106 instead of 40.

Also it is likely that with the mark 2 monitor line 260, 2nd DATA number should be 205 instead of 204—This affected the edit cursor original horizontal position.

Hoping you can find room in Micro Prompt.

J. D. Owen,
Pendine, Dyfed.

```
4Ø Shortened Editor
5Ø POKE 250,211
6Ø DATA164,253,165,252,145,249,2ØØ,2Ø8,2,23Ø
7Ø DATA25Ø,2Ø8,41,198,253,76,111,2,2Ø2,16
8Ø DATA3,232,16,4Ø,172,Ø,2,169,32,153
9Ø DATAØ,211,136,2Ø6,Ø,2,198,251,169,95
1ØØ DATA153,Ø,211,165,254,24Ø,222,164,253,165
11Ø DATA252,145,249,136,132,253,177,249,133,252
12Ø DATA169,95,145,249,164,255,169,Ø,96,32
13Ø DATA186,255,132,255,2Ø1,21,24Ø,55,2Ø1,28
14Ø DATA24Ø,192,2Ø1,2,24Ø,217,2Ø1,13,24Ø,96
15Ø DATA72,173,Ø,2,197,251,16,11,56,165
16Ø DATA253,233,64,176,2,198,25Ø,133,253,173
17Ø DATAØ,2,133,251,1Ø4,2Ø1,4,24Ø,137,2Ø1
18Ø DATA6,2Ø8,7,165,252,72,32,47,2,1Ø4
19Ø DATA76,153,163,56,165,254,24Ø,6,164,253
2ØØ DATA165,252,145,249,23Ø,254,165,254,2Ø1,16
21Ø DATA24Ø,21,2Ø1,1,2Ø8,5,173,Ø,2,133
22Ø DATA253,165,253,233,64,176,2,198,25Ø,168
23Ø DATA76,1Ø1,2,169,Ø,133,254,169,211,133
24Ø DATA25Ø,173,Ø,2,2Ø8,239,169,Ø,133,254
25Ø DATA133,249,169,211,133,25Ø,169,32,133,252
26Ø DATA169,2Ø4,133,251,133,253,169,13,96
27Ø FORZ=559TO767:READ A:POKE Z,A:NEXT
28Ø POKE536,116:POKE537,2
OK 290 NEW
```

STRING PUZZLE

Sir—For a mild surprise, UK101 owners might care to answer the question "MEMORY SIZE" with the letter A.

Can anyone help with this problem. It seems that the string created by using STR$ is not the same as that which comes from putting the same material in quotes.

The following program illustrates the difference:—

```
10 X = 8: X$ = STR$(X)
20 PRINT X$; ASC(X$);
ASC(MID$(X$,2,1))
RUN
 8 32 56
```

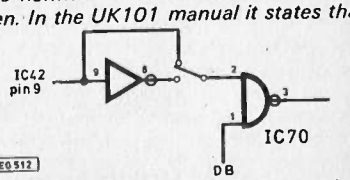
Thus the STR function appears to place a blank character at the left hand side of the 8, yielding "32" when examined, and to find the 8 requires looking at the second character, whose ASCII value is of course 56.

This does not happen if the first statement is X$ = "8".

R. J. Newman,
Chesham.

REVERSE VIDEO

Sir—The following modification will allow black characters on a white screen instead of the normal white characters on a black screen. In the UK101 manual it states that



the white dot is stored as a "1" and black as an "0", so by inverting this, a white dot becomes "0" and a black dot becomes "1". This can be done by the following modification. By inverting the output of IC42 this changes the serial video data from "1" to "0" and "0" to "1". There are a number of spare invertors on the board. I have also put a switch across the gate so that I can use both types.

I suggest that screened leads should be used to connect the switch as interference upsets the video signal.

Gerhart Ellett,
Gt. Yarmouth.

Interfacing COMPUKIT

Part 5 D. E. Graham

THIS month we will be looking at the Programmable Sound Generator on the Analogue Board. A separate page is also included which elaborates on the use of SK4 and SK5 of the Decoding Module.

THE AY-3-8910 PROGRAMMABLE SOUND GENERATOR

Fig. 5.1 gives the circuit of the audio section of the Analogue Board. This consists of a General Instrument AY-3-8910 Programmable Sound Generator feeding an LM386 audio amplifier which produces 200mW into an 8 Ohm load. The audio circuitry is based on a design from G.I.'s data manual.

The 8910 is a sixteen register device containing three independent tone generators, a variable pitch white noise generator, mixers and an envelope controller. Details of the operation of the very similar 8912 were given in the *September 1980* issue of *P.E.*, and for this reason a full device description will not be given here. For additional information on the device the reader is referred both to that article, to G.I.'s data manual on the chip, and to the article *Micro Sounds* in *Personal Computer World, October 1980.*

Although the 8910 is a sixteen register device, it is intended for CPUs which use a shared address and data bus, and for this reason cannot be used directly with 6502 based machines. This difficulty may, however, be circumvented by using the data bus to carry data which the 8910 can use either as true data or as an address, depending on the state of its control lines (which are designed to inform it of such things). One has then simply to set up the correct configuration on its control lines before furnishing it with appropriate data on its shared bus.

This task is performed by IC8c and IC8d on the Decoding Module. The required configuration of the two control lines (coded BDIR and BC1) is given in Table 5.1. From this it may be seen that to select any one of the P.S.G.'s 16 internal registers, both BDIR and BC1 must go high, and at the same time the number of the register required must be placed on the data bus by the CPU for the P.S.G. to read. Once the operation is completed, both BDIR and BC1 must be taken low. If it is then required to write data into the particular register just called up, BDIR must be taken high. Any data on the data bus will then be written into the given P.S.G. register.

The two signals BDIR and BC1 are produced by the Decoding Module in response to the R6, W6 and W7 lines, as may be seen from the circuit of Fig 5.2. This is organised so that reading and writing to the P.S.G. is performed in the following way. To place the value 100 (decimal) into P.S.G. register 4, one simply executes:

POKE 61317, 4
POKE 61318, 100

The first command calls up register 4. The second places the data into it. To read the contents of register 7, execute:

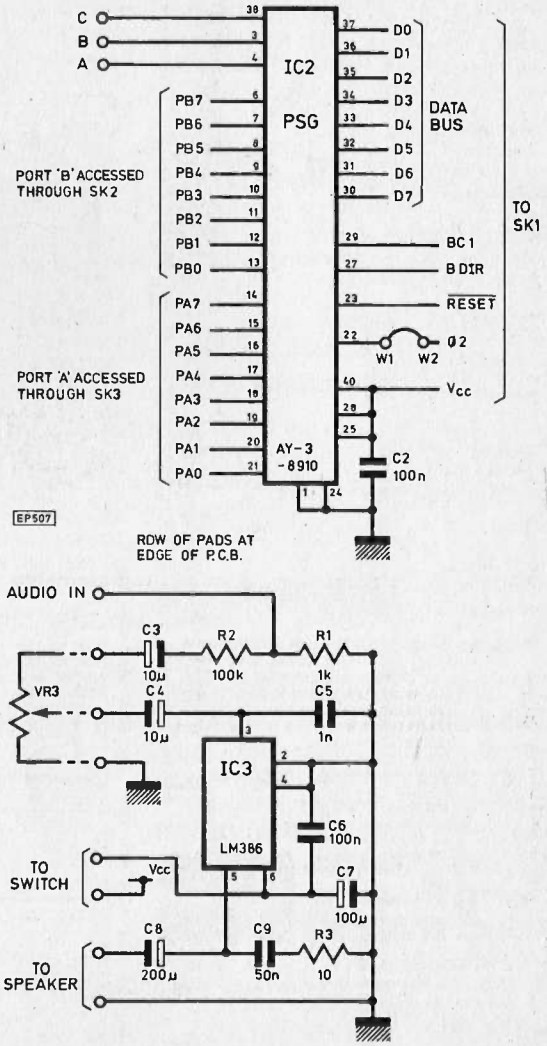
POKE 61317, 7
PRINT PEEK (61318)

This calls up register 7, then reads from it.

TESTING THE PSG

When setting up the PSG for the first time, connect the pads as shown in Fig 5.3, and switch on S1. Check that the audio amplifier is working by setting the volume control VR3

Fig. 5.1. PSG section of Analogue Board. W1 and W2 allow alternative clock drive (1–2MHz) if desired.



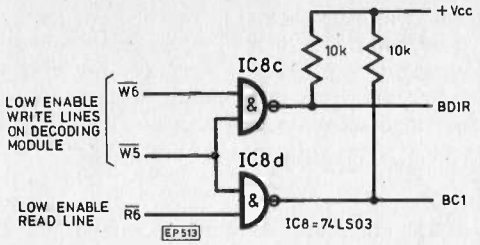


Fig. 5.2. PSG decoding circuitry on Decoding Module Board.

Table 5.1. PSG Control line functions

Function	BDIR	BC1
Inactive	Ø	Ø
CPU read from PSG	Ø	1
CPU write to PSG	1	Ø
Latch address of PSG register	1	1

Fig. 5.3. Connection of PSG pads for normal operation.

Fig. 5.4. Connection of PSG pads for normal operation on channel C, with analogue output on channels A and B.

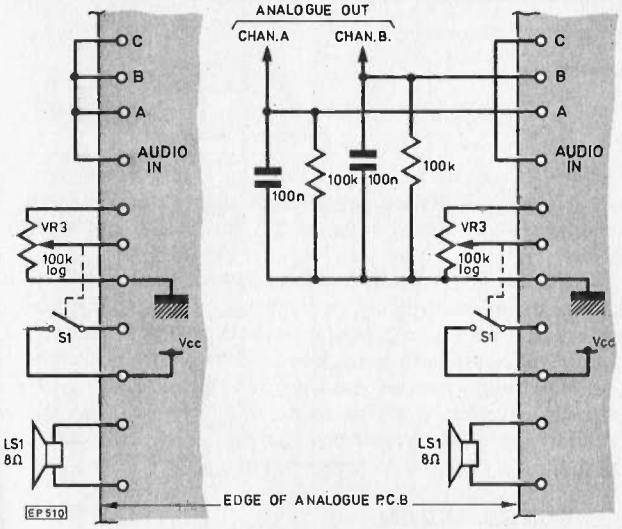


Table 5.2. Manual operation of Programmable Sound Generator.

```
50 REM INTERFACING UK101 PROGRAM 9
80 REM AY-3-8910 MANUAL ENTRY PROGRAM
100 FORS=1TO16:PRINT:NEXT
110 PRINT,"AY-3-8910 POKE/PEEK ROUTINE"
120 PRINT,"USING ADDRESSES 61317 & 61318
124 PRINT,"(NOTE DATA > 255 CAUSES A READ)"
125 PRINT:PRINT
130 A=61317:D=61318
135 REM*********************************
140 REM ZERO ALL REGISTERS
150 FORX=0TO15
160 POKEA,X
170 POKED,0
180 NEXT
190 REM*********************************
200 REM POKE/PEEK ROUTINE
210 INPUT"    REGISTER";A1
220 POKEA,A1
230 INPUT"    DATA";D1
240 IFD1>255THEN300
250 POKED,D1
260 GOTO210
300 PRINT,"CONTENTS OF REG";A1;" :   ";PEEK(D)
310 GOTO210
```

to full volume, and touching the wiper pin. If this produces hum, then run the program shown in Table 5.2. This has been written for manually controlling the contents of the P.S.G.'s registers. It first zeroes all registers, and then requests a register number. When this is entered, it requests the data that is to be put into it (any integer form 0 to 255). If a number greater than 255 is entered, the program will read from the register instead of writing to it, and print out the results.

Run the program and use it to examine the contents of the P.S.G.'s registers: all should be at zero. Data may then be placed in registers 0 to 13, and a check made to verify that the data has been properly stored. Remember here however, that certain registers (1, 3, 5, 6, 8, 9, 10 and 13) are only 4 or 5 bits wide, and attempting to place the value 255 say, into register 1 will cause the value 15 to be stored in that 4-bit register.

If registers 0 to 13 do not read or write correctly, first check the status of all lines to the P.S.G. (supply, Ø2, etc.). Next check the functioning of the control lines BDIR and BC1 with a 74LS75 latch (or similar) in the manner indicated in part 2 of the series. Their states should be checked against those given in Table 5.1. If these are incorrect, then the decoding circuitry should be checked. If they are functioning correctly, then a way should be devised of testing the P.S.G. chip itself. This could be done using the PIA on the Decoding Module, with one port connected to the 8 data/address lines of the P.S.G. and two lines of the other port supplying the BDIR and BC1 signals.

Once the registers read and write correctly, it should be possible to produce some sounds. The fastest way to make noise is to enter 15 into register 8 after resetting the P.S.G. This should produce white noise whose colour may be altered by placing data into the lowest 5 bits of register 6. To stop the noise, place 254 into register 7. If this is followed by placing 100 into register 0, a pure tone should be produced whose note may be varied by changing the data in registers 0 and 1.

If audio is not forthcoming, but the registers read and write correctly, then the audio circuitry should be checked, and pins 4, 3 and 38 of the P.S.G. examined for audio output.

THE P.S.G.'s REGISTERS

In order to produce more subtle sounds, it is necessary to be acquainted with the functions of the P.S.G.'s full set of registers. These are represented diagrammatically in Table 5.3.

Perhaps the most important register is number 7, the master enable. This is organised, somewhat inconveniently, to be active-low, so that placing a zero into it enables all tone and noise channels, 255 silences them all, while 254 enables tone on channel A only, etc. Note frequencies must then be set using the first six registers (two for each channel); and then amplitudes (registers 8, 9 and 10 for channels A, B and C respectively). Data from 0 to 15 in these registers produces differing amplitudes, while data of 16 in any of the three registers puts the associated channel over to envelope control.

Registers 11 and 12 control the time period of the envelope, while 13 controls, its shape, and whether it is repeating or not. For more precise details of this register the reader is referred to one of the three works cited earlier, but in Table 5.4 we give a selection of useful data for this register.

Registers 14 and 15 are two 8 bit ports, whose function is controlled by the top two bits of register 7 (0 for input, 1 for output). The connections to these two ports have been taken

out to the 16 pin d.i.l. sockets SK2 and 3. See Table 5.5 for connections. It will be seen that they have been made similar to those for the PIA on the Decoding Module, although it should be noted that the two sockets face the opposite direction to those on the Decoding Module.

Register	Function	BIT 7	6	5	4	3	2	1	0
R0	Channel A tone period	8-bit fine tune A							
R1						4-bit coarse tune A			
R2	Channel B tone period	8-bit fine tune B							
R3						4-bit coarse tune B			
R4	Channel C tone period	8-bit fine tune C							
R5						4-bit coarse tune C			
R6	Noise period				5-bit period control				
R7	Enable	In/out I/O B	I/O A	Noise C	B	A	Tone C	B	A
R8	Channel A amplitude			Env en	4-bit amplitude				
R9	Channel B amplitude			Env en	4-bit amplitude				
R10	Channel C amplitude			Env en	4-bit amplitude				
R11	Envelope period	8-bit fine tune							
R12		8-bit coarse tune							
R13	Envelope profile					4-bit control			
R14	I/O port A	8-bit parallel port							
R15	I/O port B	8-bit parallel port							

Table 5.3. Programmable Sound Generator registers.

Table 5.4. Selected functions of register 13 of PSG —envelope control

Data	Function
Ø	Non repeating, fast attack, slow decay
4	Non repeating, slow attack, fast decay
8	Repeating, fast attack, slow decay
12	Repeating, slow attack, fast decay
14	Repeating, slow attack, slow decay

Table 5.5. Connections to SK2 and SK3
SK3 = Port A of PSG
SK2 = Port B of PSG

Pin	Function	Pin	Function
1	GND	9	P7
2	NC	10	P6
3	NC	11	P5
4	GND	12	P4
5	GND	13	P3
6	GND	14	P2
7	NC	15	P1
8	VCC	16	P0

MAKING SOUNDS

We now give one or two sequences that may be entered using the program in Table 5.2 to produce some simple sounds. The short sequence below will produce a continuous note:

7—248
8—15
0—100

The number to the left is the register number, that to the right, the data to be placed in it. The first line sets register 7 to give tone output on all three channels, the second sets maximum volume on channel A, while the third selects a note. Entering alternative values into register 0 will change the note, and placing data in register 1 will considerably lower its pitch. If this sequence is followed by:

9—15
2—102

the note will change in timbre, becoming richer as the results of the beating of notes from channels A and B.

It is also possible to place this composite tone under envelope control. The following sequence achieves this:

8—16
9—16
12—30

The first two entries place channels A and B under envelope control, while the third determines the envelope period. Subsequently placing zero into register 13 (even if it already contains zero) will produce a one-shot decaying chime, which may be repeated by placing further zeros into 13. Alternatively, placing an 8 into 13 will produce a repeating chime or electronic piano note. This note may be further enriched by adding sounds from channel C.

For a different effect, if the following data is entered after the P.S.G. has been reset (either by rerunning the program, or by pressing the Reset button on the Decoding Module), the sound of an explosion will be produced.

6—31
7—7
8—16
9—16
10—16
12—20
13—0

Further entries of 13—0 will repeat the effect, while entering 13—8 will cause continuous repetition. Register 12 determines the decay rate, and 6 the colour of the white noise.

The program in Table 5.2 is useful for testing the P.S.G. and for experimenting with simple sound effects, but a richer variety of effects can be obtained with a little practice when the P.S.G.'s registers are altered under program control using FOR loops to vary the frequencies, timbres, and amplitudes of notes. To give an example of this, the program listed in Table 5.6 produces a two part effect by varying the frequency of channel A in different ways.

KEYBOARD ORGAN

As an example of a somewhat different usage, the program listing in Table 5.7, which should just squeeze into a 4K machine, is for a 14 note organ operated from the Compukit keyboard. When the program is run, a four part menu appears on the screen:

KEYBOARD ORGAN PROGRAM
CONTENTS
1. To play press P (or GOTO 2000).
2. To hear press H (or GOTO 4000).
3. To record press R (or GOTO 5000).
4. To load press L (or GOTO 6000).
NOTE: Space Bar Exits Routines

If P is pressed, the program requests a note period (try around 30 for this) and then a further integer which determines the difference between the two frequencies used for the organ note. The organ may then be played using keyboard letters W–I and S–K. Once 100 notes have been played, or if the space bar is pressed, the program will exit this routine, and return to the menu.

Table 5.6. Dynamic sound effects.

```
70 REM INTERFACING UK101 PROCRAM 10
80 REM SOUND EFFECTS PRODUCED BY
85 REM VARYING DATA IN PSG REGISTER A
90 REM INITIALISATION********************
100 J=61317
110 K=J+1
120 POKEJ,7:POKEK,248
130 POKEJ,8:POKEK,15
140 POKEJ,0
200 REM FIRST EFFECT*********************
220 FORA=0TO128
230 POKEK,A-64*INT(A/64)
240 POKEK,128-A
260 POKEK,A
270 NEXT
290 POKEK,0
300 FORZ=1TO100:NEXT
380 REM SECOND EFFECT********************
390 FORB=1TO10
400 FORA=0TO255STEP10
420 POKEK,A
440 NEXT
450 NEXT
500 POKEK,0
600 INPUT"  AGAIN";YY$
610 IFLEFT$(YY$,1)="Y"THEN200
```

Table 5.7. Keyboard organ using the UK101 and its QWERTY keyboard.

```
20 REM INTERFACING UK101 PROGRAM 11
30 REM AY-3-8910 KEYBOARD ORGAN
50 QA=61808
55 QD=QA+1
60 K=57088
65 DIML(100)
100 PRINT:PRINT:PRINT:PRINT:PRINT,"KEYBOARD ORGAN PROCRAM"
110 PRINT:PRINT," CONTENTS"
120 PRINT:PRINT:PRINT"  1. To play press P (or GOTO 2000)."
130 PRINT:PRINT"  2. To hear press H (or GOTO 4000)."
140 PRINT:PRINT"  3. To record press R (or GOTO 5000)."
150 PRINT:PRINT"  4. To load press L (or GOTO 6000)."
155 PRINT:PRINT"     NOTE  Space Bar Exits Routines"
160 INPUTY$
170 IFY$="P"THEN2000
180 IFY$="H"THEN4000
190 IFY$="R"THEN5000
200 IFY$="L"THEN6000
220 PRINT,"NOT RECOGNISED"
225 PRINT,"ENTER AGAIN PLEASE"
230 GOTO160
2000 REM ORGAN
2003 GOSUB8000
2007 PRINT:PRINT:PRINT
2020 Z=0
2021 INPUT"  TONE QUALITY 0,1,2 ETC";XX
2022 PRINT:PRINT,"KEYBOARD READY":PRINT:PRINT:PRINT
2030 POKE530,0
2040 POKE530,1
2050 POKEK,247
2060 P=PEEK(K)
2080 FORA=9TO15
2090 READB
2100 IFB=PTHENL=A:A=20
2110 NEXT
2120 RESTORE
2122 IFA>19THEN2220
2125 POKEK,239
2130 P=PEEK(K)
2135 FORA=2TO8
2140 READB
2145 IFB=PTHENL=A:A=20
2150 NEXT
2155 RESTORE
2220 POKEK,253
2230 IFPEEK(K)=239THEN3600
2240 IFA<19THEN2030
3000 POKEQA,2
3005 POKEQD,L*5+40
3010 POKEQA,0
3015 POKEQD,L*10+80+XX
3020 POKEQA,13
3030 POKEQD,0
3040 IFL=L1THEN2050
3045 L(Z)=L:L1=L
3050 Z=Z+1
3200 IFZ<101THEN2030
3500 DATA127,191,223,239,247,251,253
3600 POKEQD,0
3602 S=Z-1
3605 POKE530,0
3610 GOTO100
3990 REM AUTO REPLAY ROUTINE
4000 PRINT:PRINT:PRINT:PRINT:PRINT
4001 GOSUB8000
4003 POKEQA,2
4005 PRINT,"AUTO REPLAY"
4010 PRINT,"SEQUENCE LENGTH ";S
4012 PRINT,"FILE NAME  ";FL$
4015 PRINT:PRINT:PRINT
4020 INPUT"REPEATING? Y OR N";R$
4030 INPUT"NOTE LENGTH? 0 - 2000";NL
4100 FORZ=0TOS
4105 POKEQA,2:POKEQD,L(Z)*5+40
4110 POKEQA,0:POKEQD,L(Z)*10+80+XX
4115 POKEQA,13:POKEQD,0
4120 FORA=1TONL:NEXT
4123 POKE530,1
4125 POKE57088,253:IFPEEK(57088)=239THEN4140
4127 POKE530,0
4130 NEXT
4132 POKE57088,253:IFPEEK(57088)=239THEN4140
4135 IFR$="Y"THEN4100
4140 POKEQD,0
4145 POKE530,0
4150 GOTO100
4990 REM SAVE ROUTINE
5000 PRINT:PRINT:PRINT,"FILE CREATION"
5002 INPUT"    ENTER FILE NAME";FL$
5004 PRINT:PRINT:PRINT
5010 PRINT,"SET RECORDER, AND PRESS"
5020 PRINT,"ANY KEY"
5030 INPUTX$
5040 SAVE
5044 PRINT"ZZZ"
5045 PRINTFL$
5050 PRINTS
5055 PRINTXX
5060 FORZ=0TOS
5070 PRINTL(Z)
5080 NEXT
5090 POKE517,0
5095 PRINT:PRINT:PRINT,"RECORDING COMPLETE"
5100 GOTO100
5990 REM LOAD ROUTINE
6000 PRINT,"NOTE SEQUENCE LOADER"
6002 INPUT"    NAME OF FILE REQUIRED";FL$
6004 PRINT:PRINT:PRINT
6010 PRINT,"START TAPE, & PRESS ANY KEY"
6020 INPUTX$
6030 LOAD
6032 INPUTFF$
6034 IFFF$<>FL$THEN6032
6036 PRINT,"FILE   ";FF$;"  FOUND"
6040 INPUTS
6045 INPUTXX
6050 FORZ=0TOS
6060 INPUTL(Z)
6070 NEXT
6075 POKE515,0
6080 PRINT:PRINT:PRINT,"LOAD COMPLETE"
6090 PRINT,"PLAY?"
6130 GOTO100
8000 REM AY-3 INITIALISE
8110 POKEQA,0:POKEQD,0
8120 POKEQA,1:POKEQD,0
8130 POKEQA,3:POKEQD,0
8140 POKEQA,7:POKEQD,248
8150 POKEQA,8:POKEQD,16
8160 POKEQA,9:POKEQD,16
8170 POKEQA,11:POKEQD,0
8180 POKEQA,12:INPUT" PERIOD";PE:POKEQD,PE
8200 RETURN
```

If H is then entered, a replay routine is initiated providing an opportunity to hear again the sequence just played, and to alter note length and replay speed. The replay may be put in a repeating mode if desired.

There is also a facility to save on tape the sequence of digits representing the notes played, and, using a load routine, to reload them on a subsequent occasion.

The save routine uses a file name system, and when a tape is reloaded, the program asks for the name of the file required, and will ignore all other files that it comes across. A vital part of the SAVE/LOAD routines is the PRINT "ZZZ" statement in line 5044. This data (ie, ZZZ) is subsequently read and ignored by the load routine, and ensures that the loading of data is not confused by random noise or unwanted data preceeding the file name. The sequence of data used by the routines is as follows: File Name, Length of Note Sequence, and Timbre Indicator. This data is followed by a sequence of numbers representing the notes played.

SEPARATE USE OF THE 8910's D/A CONVERTERS

The 8910 P.S.G. contains three internal D/A converters, one of which is used for each channel. These may be employed separately for 4 bit D/A conversion, to supplement the ZN425 converter on the Analogue Board. One could, for example, use channels A and B each as 4 bit converters, while retaining channel C for audio output. Fig. 5.4 shows the wiring of the 8910 pads on the Analogue Board for this contingency. Channels A and B are then controlled simply by registers 8 and 9 which, under normal circumstances, would have controlled audio output level. Now, data from 0 to 15 in these registers will determine the d.c. voltage on pads A and B, while data of 16 will place the d.c. voltage under

envelope control. The envelope facility might prove to be particularly useful in a number of different applications. Each of the 3 channels of the P.S.G. could be used to control the level of banks of lights for example, in which case each or all of them could be brought under envelope control to give a slow fade, etc. In such an application each channel output could be made to drive a 741 op. amp. followed by an opto isolator and thyristor or triac controller. It should be noted, however, that the PSG's 4-bit converters may not provide sufficient resolution for some applications.

When using the D/A converter in this way the state of register 7 should be borne in mind. The converter will function whether the associated channel's noise or tone outputs are enabled or not. But with both disabled a non-linearity appears in the transition from 0–1. This is minimised by enabling tone and noise, although the latter places some noise on the d.c. output. The effect can be reduced by increasing the capacitor taken from the pad outputs to ground.

Constructor's Note

A C60 cassette tape containing all the numbered programs of this series is available from *Technomatic Ltd.*, (see advertiser's index), at £3·50 + VAT and p & p.

Next month we shall explore the facilities by the 6522 Versatile Interface Adaptor on the Analogue Board, and will discuss such applications as frequency counters and real time clocks.

PIN CONNECTIONS TO SK3 AND SK4 OF THE DECODING MODULE

One or two readers have asked for specific pin connections for interfacing the devices described in part 2 of the series.

Interfaces such as the light sensor, sound detector or joystick control box described in part 2 of the series, or the l.e.d. indicator or relay output described in part 3 are accessed directly through SK3 or SK4 of the Decoding Module.

The pin connections of these two sockets (SK3 for port A and SK4 for port B) are identical, and were given in Table 1.6 of part 1 of the series.

Devices which require a single port line, a ground and +5V line (such as the l.d.r. circuit of Fig. 2.10 in part 2 of the series) should be connected as indicated in Fig. 5.5.

Pin 8 of SK3 and 4 carries Vcc (+5 volts), pin 1 ground, and pin 16 data line DØ of the port (sometimes labelled PAØ). If the header wired as in Fig. 5.5 is plugged into SK3 of the Decoding Module, and the Logic Tester program of Table 2.5 (part 2 of the series) is run, DØ of the screen display should register a zero for dark conditions, and a 1 in daylight.

The joystick control box of Fig. 2.9 of part 2 connects directly to a 16-pin header that may be inserted into SK3 or SK4 of the Decoding Module. The wiring for this is given in Fig. 5.6. If the header is plugged into SK3 it may be used in conjunction with the screen drawing program listed in Table 2.4 of part 2.

Sirnilar pin connections are made to SK3 or SK4 when using the PIA for digital output. As an example, Fig. 5.7 gives the pin connections for simple audio output from the PIA. Again use is made of the 5 volt line supplied by the Decoding Module. In this instance it is used to power the 2N2926 audio amplifier. This circuit should be used in conjunction with the programs in Table 3.5 and 3.6 of part 3 of the series.

Other input and output applications use similar connections to SK3 and SK4.

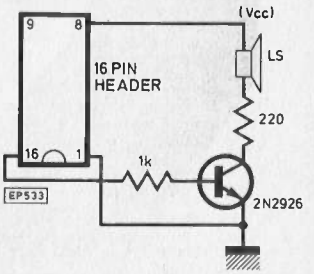


Fig. 5.4. Pin connections to 16-pin header for simple audio output from PIA

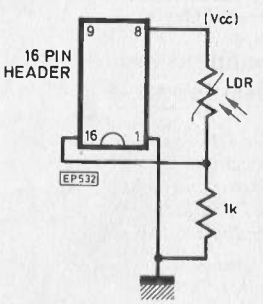


Fig. 5.5. Pin connections to 16-pin header for use with LDR. The header plugs into SK3 or SK4 of the Decoding Module

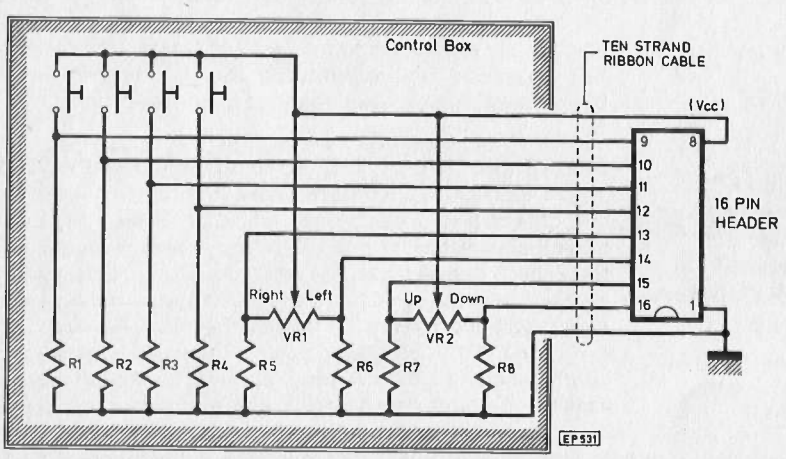
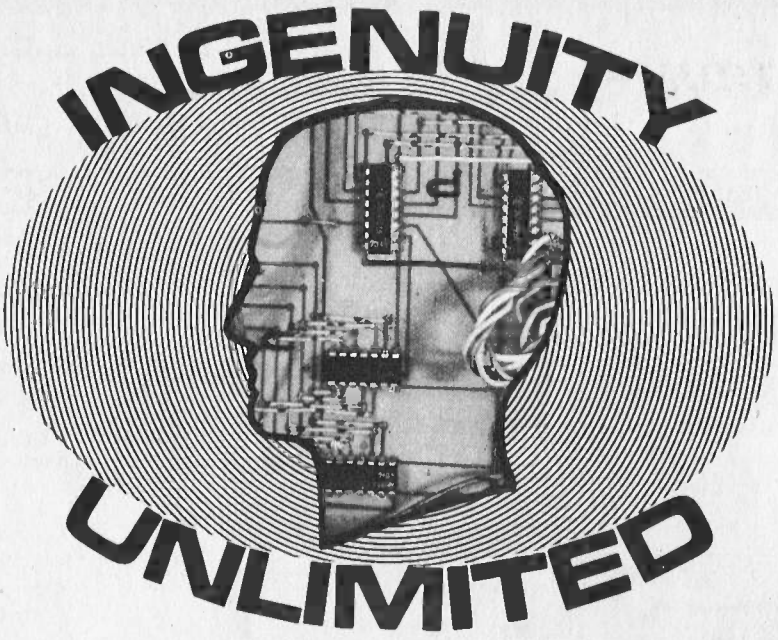


Fig. 5.6. Joystick control box giving connections to 16-pin header to be plugged into SK3 of the Decoding Module



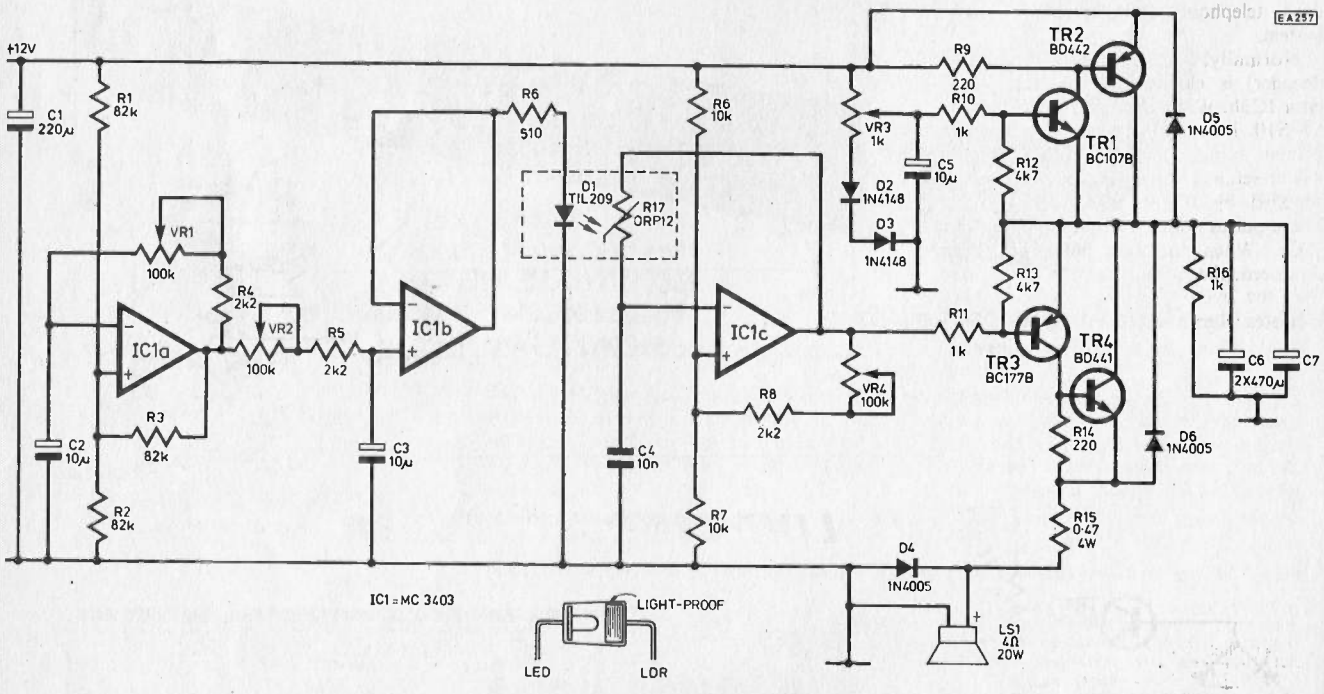
A selection of readers' original circuit ideas. It should be emphasised that these designs have not been proven by us. They will at any rate stimulate further thought.

Each idea submitted must be accompanied by a declaration to the effect that it has been tried and tested, is the original work of the undersigned, and that it has not been offered or accepted for publication elsewhere.

Why not submit *your* idea? Any idea published will be awarded payment according to its merits.

Articles submitted for publication should conform to the usual practices of this journal, e.g. with regard to abbreviations and circuit symbols. Diagrams should be on separate sheets, not inserted in the text.

BOAT HORN



THIS circuit was designed to inject some tonal variation from the dull flat sound of my boat horn.

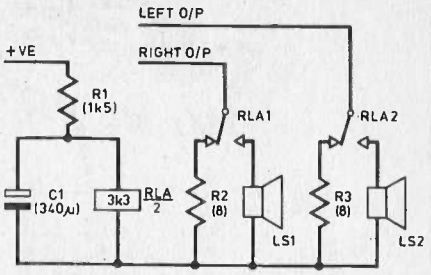
This circuit includes three op-amplifiers. The first amplifier oscillates at an adjustable frequency which is transferred to op-amp IC1b via a 100 kilohm potentiometer. To this op-amp is connected a l.c.d. which together with the l.d.r. is used as an opto-isolator. It's important that light from outside can't reach the l.d.r. A simple opto-isolator can be built as shown.

After the isolator a third op-amp is connected and after that an ordinary amplifier.

The volume is adjustable with the 1 kilohm pot all the other pots are built in to adjust the output signal.

Leif Ljung,
Soedertalje,
Sweden

THUMP ELIMINATOR



THIS circuit was used to eliminate the considerable switch on thump generated by my amplifier, but is equally applicable to any transistor amplifier that suffers from this problem. R2, R3 are initially connected across the amplifier outputs, in place of the speakers, by means of the relay changeover contacts. When the power supply is switched on, C1 charges via R1, and the potential across C1 reaches the operating potential of the relay after approximately 4 seconds. During this time, the output of the amplifier has stabilised, and the changeover from resistor-loading to loudspeaker-loading of the outputs occurs silently.

R2, R3 should have values equal to the loudspeaker impedance; R1, C1 will depend on the type of relay employed. (If the relay operating voltage is 2/3 of the amp supply voltage, R1 should be slightly less than ½ of the relay coil resistance. C1 is then chosen to give a suitable delay-time.) For my Sinclair 2000, a miniature TMC relay was used, with a coil resistance of 3·3K; R1=1·5K, C1=340μF. All components are mounted within the amplifier case: R1–R3 make use of some spare sections of track in the power-supply area of the p.c.b. and the relay is mounted on an empty area of board near the equilisation switches. The speaker output sockets are p.c.b. mounted on this amp, so it was necessary to break the two output tracks in order to wire in the relay contacts and R2, R3, so care must be taken when performing this sort of modification.

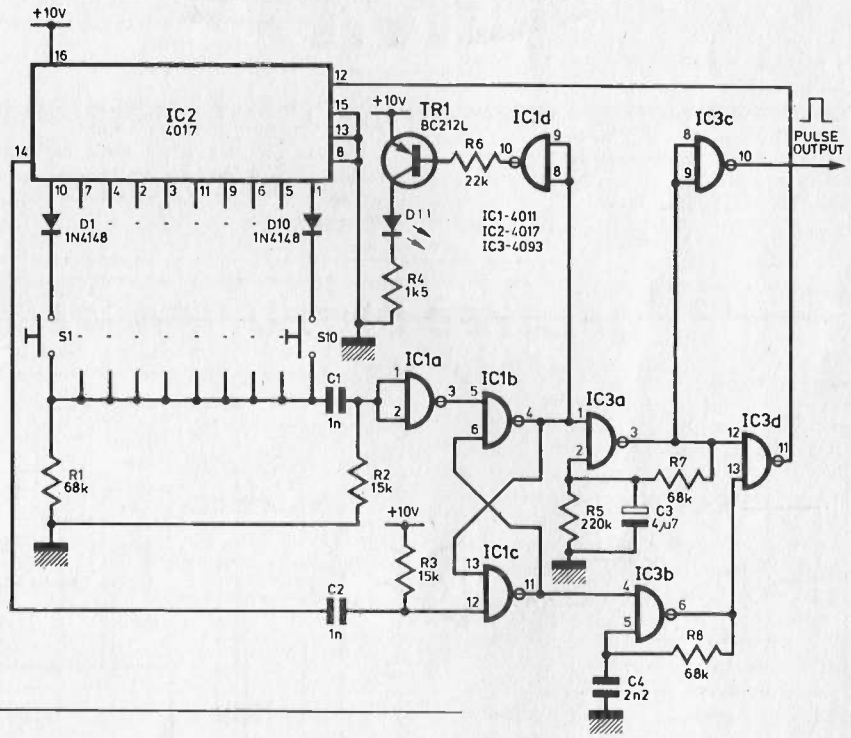
A. A. Jeffree,
Letchworth,
Herts.

PUSH-BUTTON PULSE GENERATOR

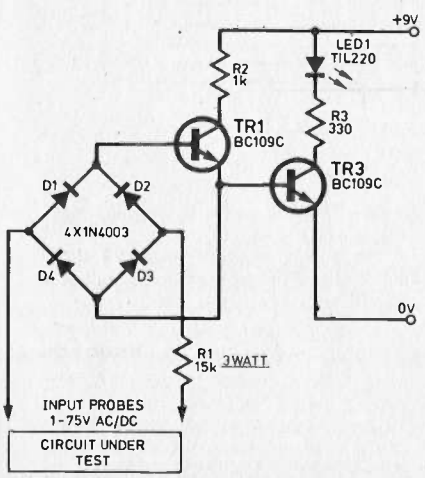
THIS circuit produces from 1 to 10 pulses, depending on which key is pressed. The prototypes used ex-calculator keyboards and were used in place of standard telephone dials in an intercom system.

Normally, IC2 (a 4017 counter/decoder) is clocked by the 'fast' oscillator IC3b. When one of the push-buttons S1–S10 is closed and the appropriate counter output is high, the bistable IC1b/c will be set, and clock pulses for IC2 will be supplied by the 'slow' oscillator IC3a. These pulses are also fed to the output via IC3c. When the last pulse has been produced, the bistable is reset by a pulse from the 'overflow' output from IC2. D11 indicates when pulses are being produced.

T. P. Hopkins,
Didsbury,
Manchester.



LIVE CIRCUIT TESTER



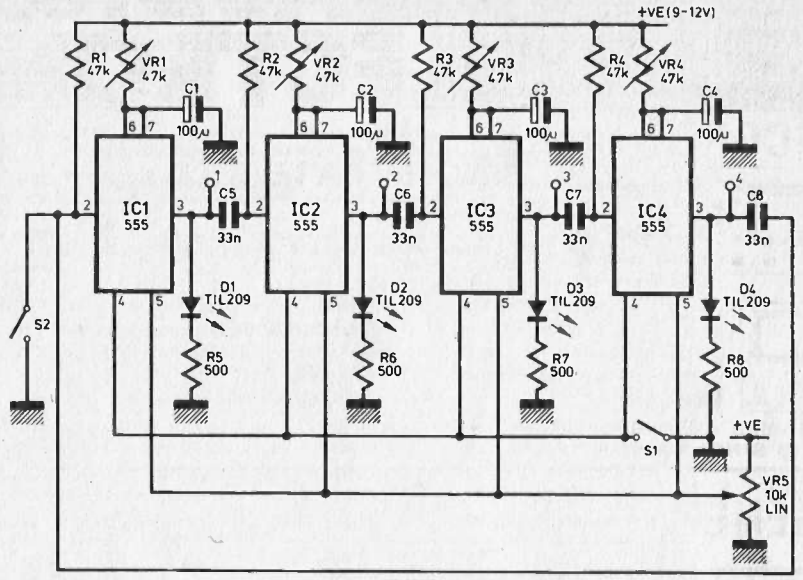
THE tester shown was designed to give a live/dead indication on both electronic and electrical circuits. The tester is safe to use on circuits working in the range 1-75V a.c./d.c., and may be used for checking car wiring, door chimes, transformer windings, continuity and batteries etc.

R1 is the input impedance resistor and should have a power rating of 3W. D1-D4 form a full-wave bridge rectifier and ensure that the correct voltage polarity is applied to the base of TR1. When a voltage greater than 1V is present at the input, TR1 is turned on which switches on TR2 via R2, the diode then lights indicating the presence of a live circuit.

The circuit can be mounted on a small piece of 0·1in. veroboard and the 9V supply can be obtained from a PP3 battery.

B.J. Lowery,
Lincoln.

DISCO LIGHT SEQUENCER



MY problem was to design a sequencer to control lights for a disco. This would need only four channels and must be able to vary not only the overall rate of the sequencing but also the mark—space ratio of each of the channels. The commonly used 4017 would not therefore be suitable for this.

The circuit was designed around four 555 timers (or two 556) connected as negative edge triggered monostables. These are arranged in a ring so that as one goes low it triggers the next one and so on. This provides the sequence. Adjustment of VR1-4 control the time each channel is on, and VR5 which applies a variable voltage to all the pin 5s (control voltage) simultaneously acts as a master speed control.

The sequencer is a dynamic circuit, and once stopped will not self start so S2, a push to make switch, is provided to restart it. S1 acts as a reset. D1-4, 0·2 in red leds, indicate which channel is on.

VR1-4 are 47k linear pots, and C1-4 are 100µ capacitors, but these can be varied to alter the range of speeds. R1-4 are 47k and C5-8 are 33n but again these are not critical. R5-8 depend on the supply voltage, for 9-12V they should be about 500 ohms.

In the original device the four outputs, on pin 3 of the 555s, were used to control thyristors switching full wave rectified mains voltage.

J. Rennie,
Wookey Hole, Somerset.

DELAYED OUTPUT PROTECTED MONO

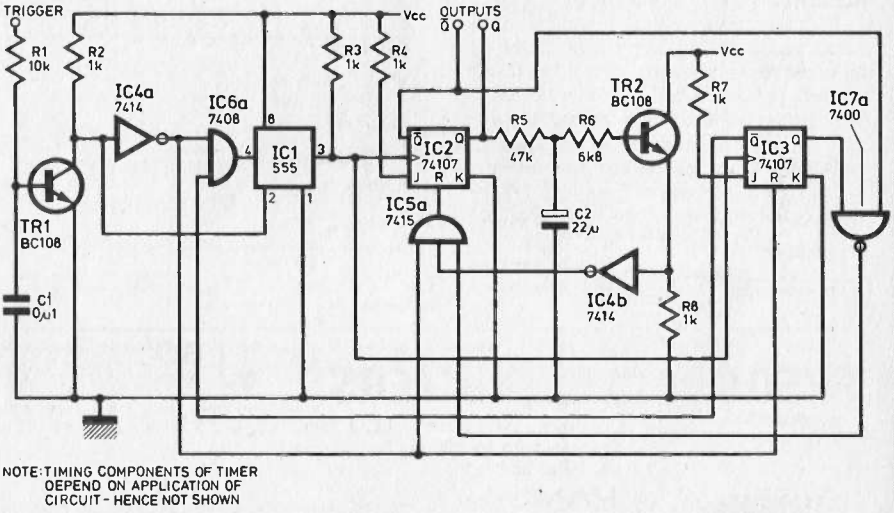
THIS circuit was designed to work in a fairly high noise environment. Its purpose was to produce an output pulse of an adjustable duration after a certain delay had elapsed; initiated by a continuous trigger voltage. Once the pulse had been delivered, a permanent reset and hold facility is incorporated in the design so that despite glitches and induced spikes in the vicinity, the circuit could not retrigger.

Removing the trigger voltage at any time would reset the circuit, and again, hold in this mode.

With reference to the diagram in the quiescent state the 555 timer and both IC2 and IC7a are held in the reset state as long as TR1 base is either grounded or open circuit.

On the application of a continuous positive bias to TR1, the reset pin of the timer goes high, while the trigger pin goes low. Also, the reset condition is removed from IC2 and IC3. The 555 goes into its quasistable state. After the time delay set by the CR network in the timer, the output pin goes low and in so doing, IC2 and IC3 both trigger and latch. As the 555 has completed its task, it is no longer needed, so the $\overline{Q}$ output of IC3 keeps the timer reset via the AND gate. Meanwhile, the Q output of IC2 goes high and via the resistor, C2 begins to change up towards the 5V rail.

TR2 being connected in its common collector mode, it presents a high impedence connection across C2 allowing the latter to charge up relatively unhindered.



NOTE: TIMING COMPONENTS OF TIMER DEPEND ON APPLICATION OF CIRCUIT - HENCE NOT SHOWN

The emitter voltage of the transistor will steadily rise until the Schmitt trigger will switch and via the three input AND gate, resets IC2.

Here again, protection is provided, by a two input NAND gate across the $\overline{Q}$ and Q of IC2 and IC3 respectively, causing IC2 to be permanently reset.

The output pulse is taken from either Q or $\overline{Q}$ of IC2. The duration of the pulse starts when TR1 is triggered and ends when it is reset. Naturally, the duration is dependant on R3/C2.

Removing the bias from TR1 base both triggers and resets the 555, but this action is too fast for any triggering of the circuit to occur, whilst IC2 is reset.

The circuit is once more in the quiescent condition, protected from spurious pulses, C1 assures a fast pulse at the trigger pin on triggering the circuit.

C. Embleton,
Gillingham, Kent,