PROJECTS BOOK 23

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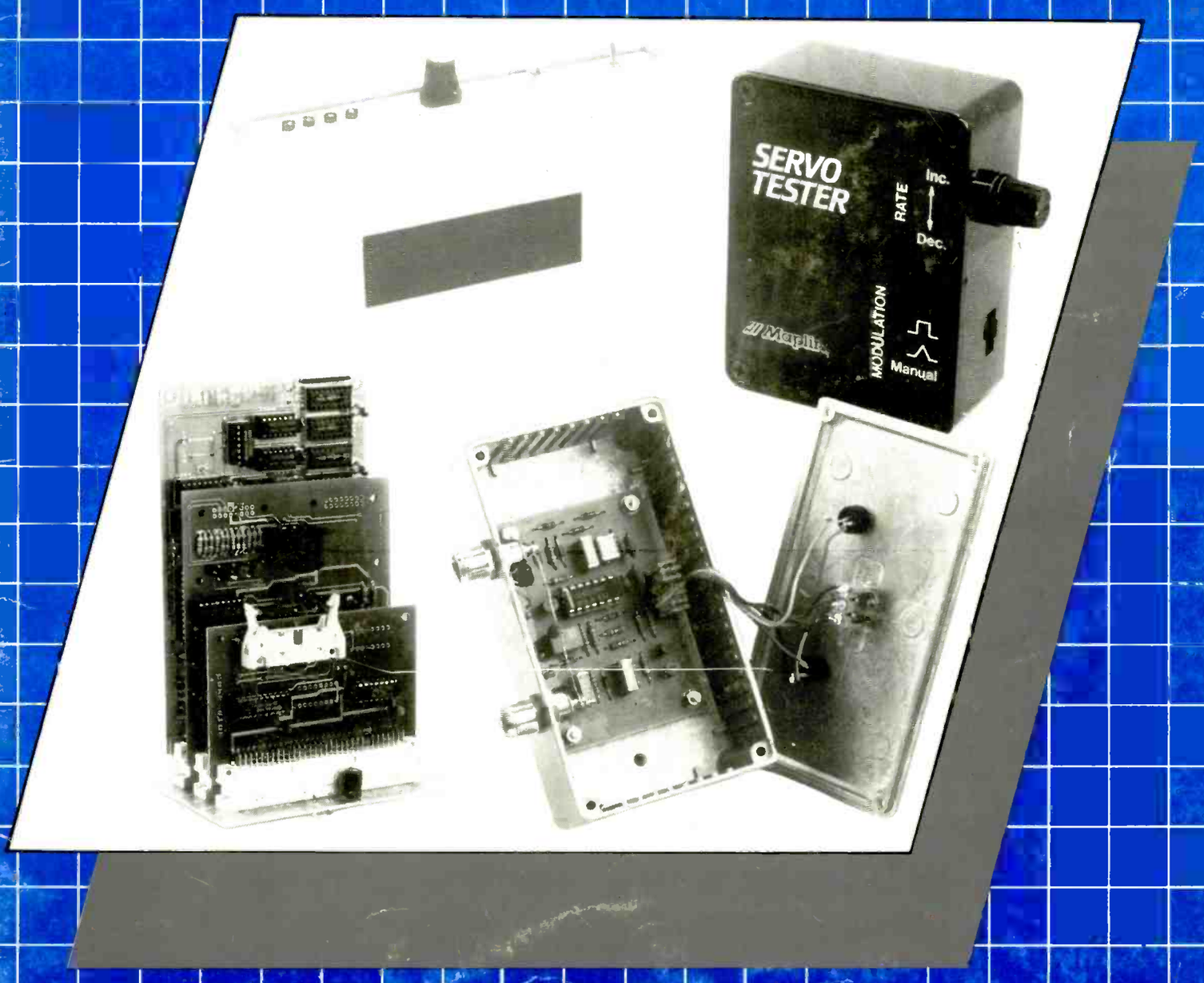

SERVO TESTER

MINI CIRCUITS

WEATHER SATELLITE CHANNEL SWITCHING UNIT

DIGITAL CAPACITANCE METER

Z80B CPU CARD

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MAPLIN PROJECTS BOOK TWENTY THREE

EDITORIAL

'Maplin Projects Book Twenty Three' is a compilation of the projects from 'Electronics – The Maplin Magazine, Issue 23', which is now out of print. Other issues of 'Electronics – The Maplin Magazine' will be replaced by projects books as they go out of print. For kit prices, please consult the latest Maplin catalogue and free price change leaflet, order as CA99H.

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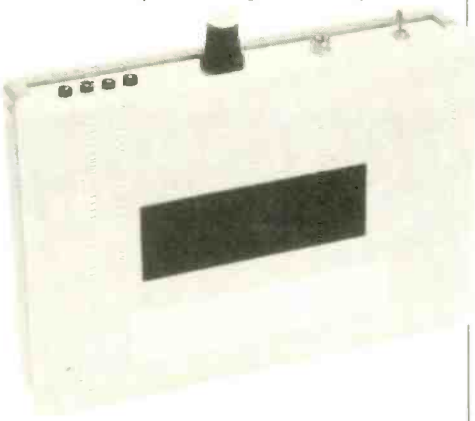

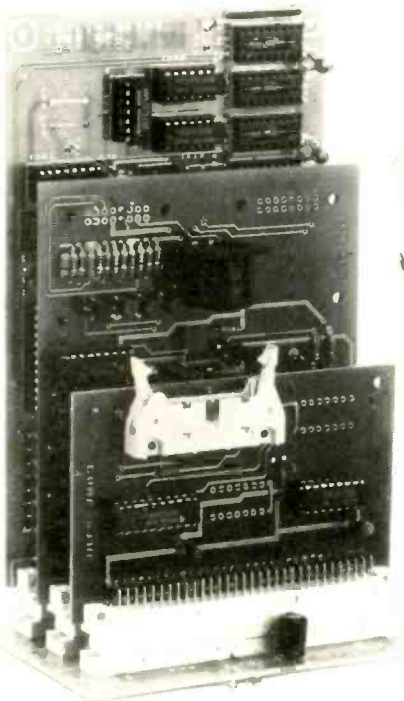

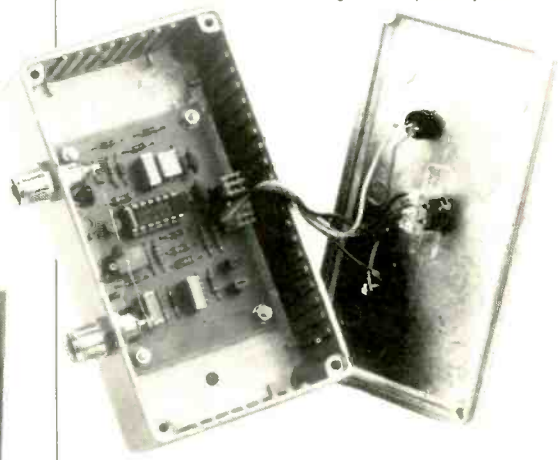

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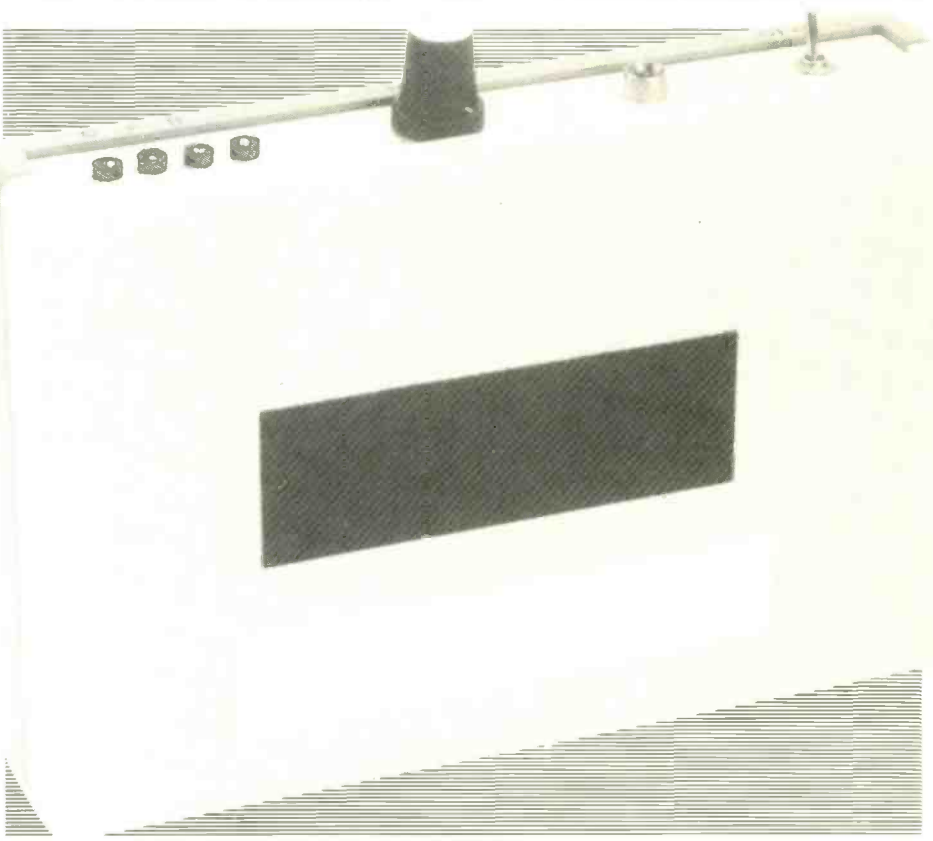
DIGITAL CAPACITANCE METER

by Robert Penfold



Practically every constructional project includes a number of capacitors, and the ability to test these components is a decided assett for any electronics constructor. Unfortunately, testing capacitors properly is something that is beyond the capability of most multimeters and other items of test equipment that are likely to be found in the average amateur electronics workshop. It is possible to make a few rough checks on capacitors using many analogue multimeters, and some modern oscilloscopes have a built-in component tester function that can be used to give some idea of a test capacitor's value, but for accurate measurement of capacitance a proper capacitance meter is required.

This design has a three digit LED display, and it covers five ranges which are as follows:-

Range 1	0 to 9.99nF
Range 2	0 to 99.9nF
Range 3	0 to 999nF
Range 4	0 to 9.99μF
Range 5	0 to 99.9μF

This coverage includes all the common values, but the unit cannot measure very low values of just a few picofarads, or high value electrolytic components. In practice this is not likely to matter too much as very low value components are little used in modern circuits, and large values can be checked by using two components wired in series, as will be explained more fully later in this article. An overflow indicator LED is included so that misleading results are avoided if an unsuitable range is selected. The unit is powered from an internal 9 volt battery, and is in consequence fully portable.

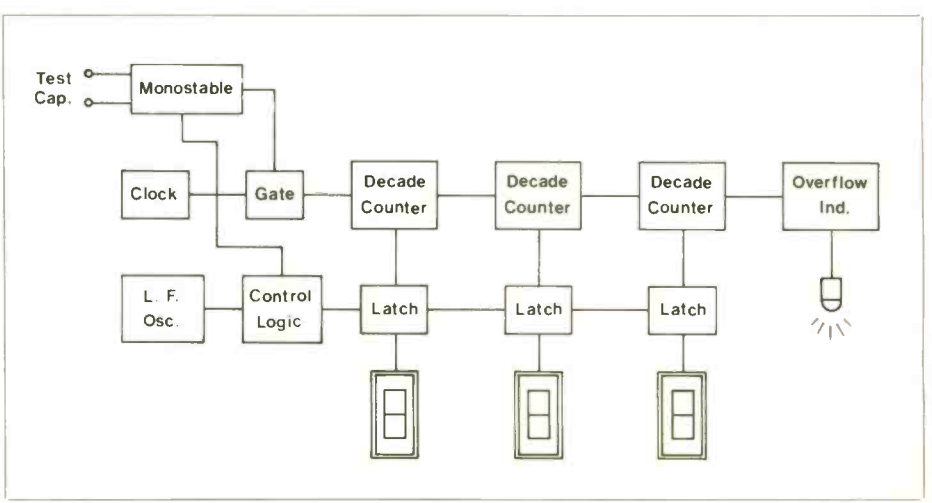


Figure 1. Block schematic.

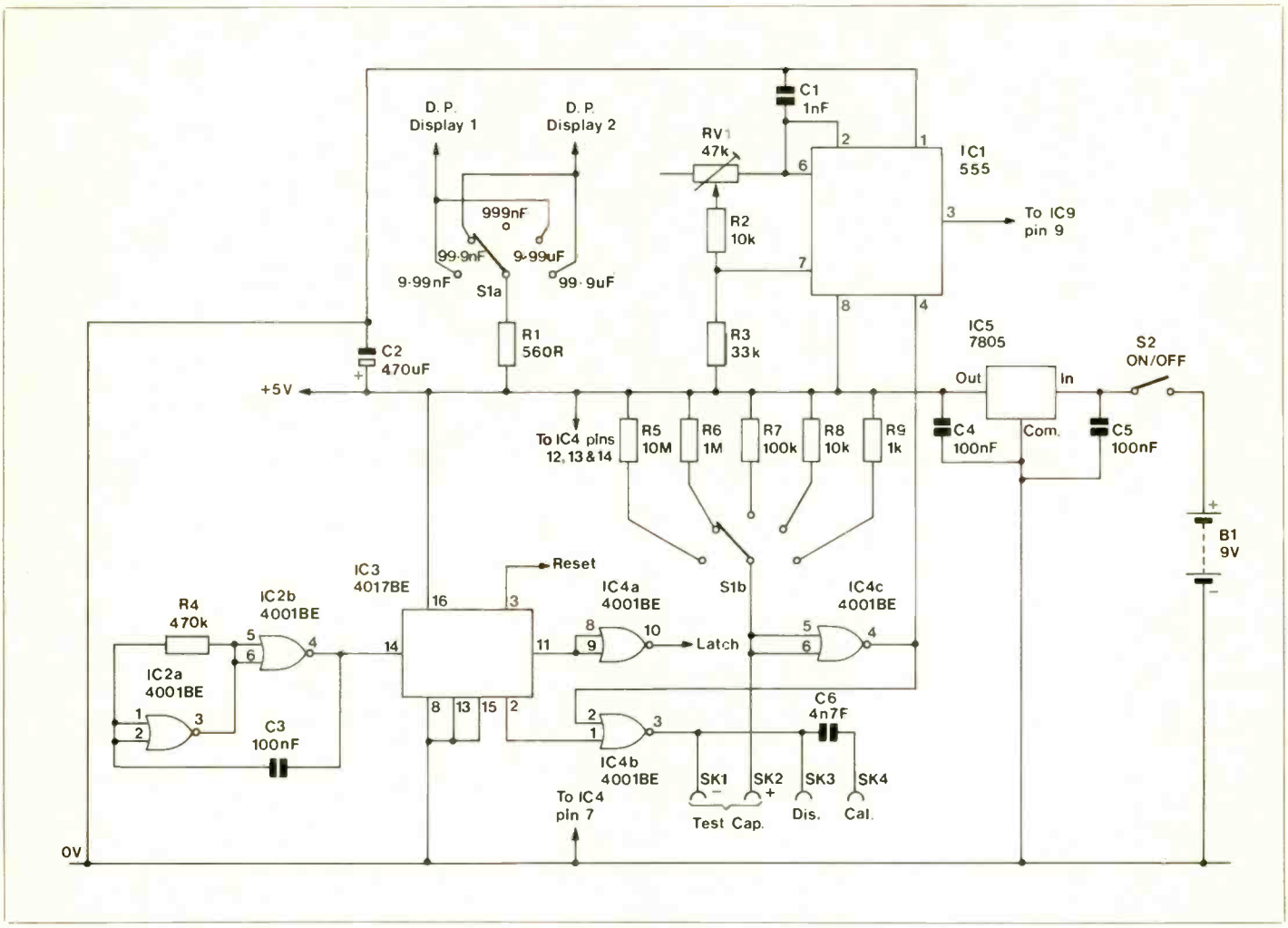
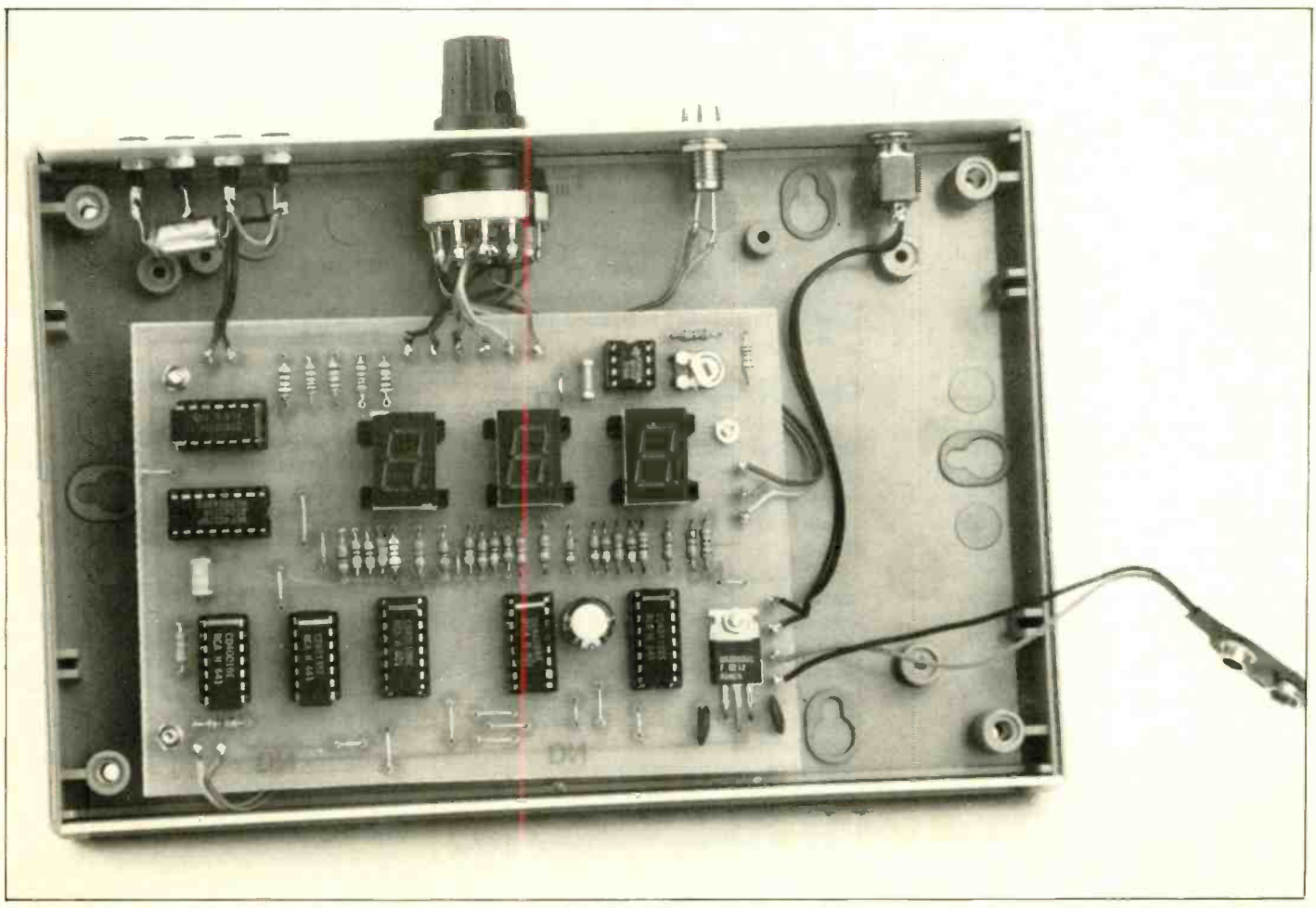


Figure 2. Clock, control and monostable circuit.



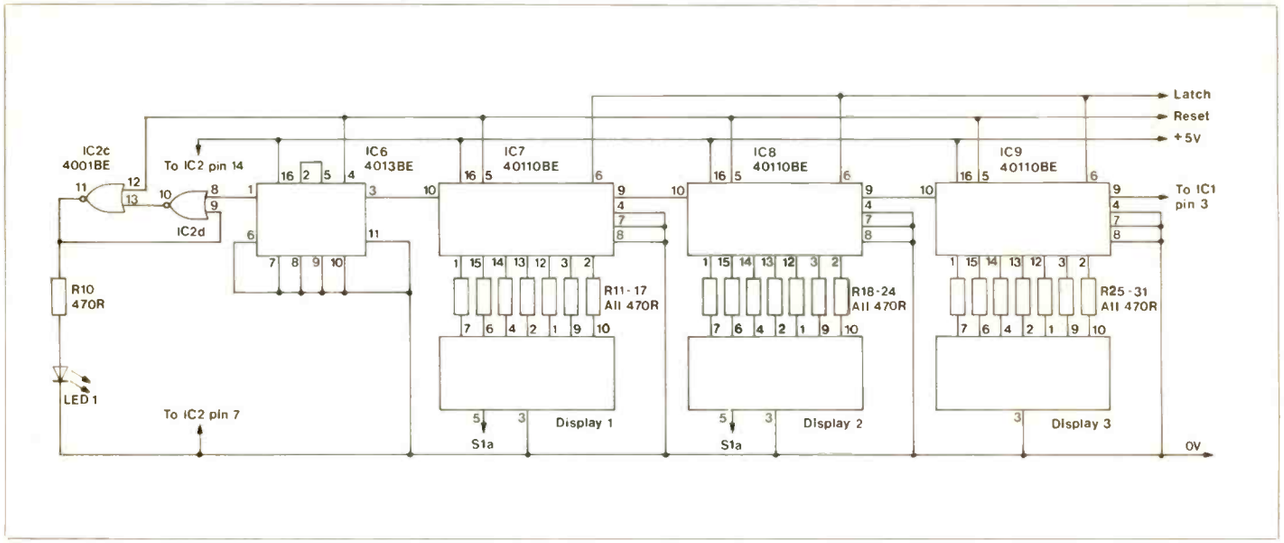


Figure 3. Counter and overflow indicator circuit.

System Operation

In common with most capacitance measuring devices, this one operates by using the test component as the capacitive element in a C-R timing network. In this case the timing network forms part of a monostable multivibrator, and the higher the value of the test component the longer the output pulse of this circuit. There is a linear relationship between the value of the test component and the output pulse duration, and this makes it relatively easy to employ the pulse in controlling a display circuit that gives a reading directly in nanofarads or microfarads (nF or μF). The block diagram of Figure 1 helps to explain the way in which the unit functions.

A low frequency oscillator controls the rate at which readings are taken, and this gives readings at just under one second intervals. The output of the oscillator drives a simple control logic circuit, and this provides pulses that sequence the rest of the circuit correctly. The first operation in the sequence is for a trigger pulse to be sent to the monostable multivibrator, and this then generates an output pulse that is used as the gate pulse for a clock oscillator and a three digit counter circuit. The longer the gate pulse, the higher the count value that the display will reach at the end of the gate pulse, where the count is 'frozen'. In practice, the clock frequency is adjusted so that the display readings are accurate capacitance values. With a three digit counter only a rather restricted range of values can be accommodated with good accuracy, and so the monostable is equipped with five switched timing resistors. These give the unit its five measuring ranges, and enable a wide range of values to be catered for.

The counter circuit is of conventional design, having latches and seven segment decoder/drivers. The value held within the counters is therefore not displayed immediately, but is held in the counters until the control logic circuit provides the latches with a latching pulse. The new value is then displayed, and remains displayed even when the control logic circuit sends a reset pulse to the counter circuit. This reset pulse is essential as it is needed to ensure that the counter starts at '000' when the next gate pulse commences. The point of including the latches instead of driving the decoder/drivers direct from the counters is that it permits a continuous display to be provided. Without the latches the reset and counting action would be displayed, which would give unacceptable results in practice.

If the test capacitor has a value which is beyond the full scale value of the range in use, the counter circuit will go through one or more complete cycles, and will display an erroneous result. To prevent the user from being misled, an overflow indicator circuit is included, and this simply switches on an LED indicator if a complete output cycle is produced by the final decade counter stage. A full output cycle is only produced from this stage if it cycles through a complete 0 to 9 count and then back to zero again.

Circuit Operation

Figure 2 shows the circuit diagram for the clock oscillator, low frequency oscillator, control logic, and monostable stages of the unit. The counter/driver and overflow circuit is shown separately in Figure 3.

Starting with Figure 2, IC5 is a 5 volt monolithic voltage regulator which gives a well stabilised 5 volt output from the 9 volt battery supply. All circuitry is powered from the stabilised 5 volt supply rail. The battery needs to be a fairly high capacity type (such as six HP7 size cells in a plastic holder) as the current consumption of the circuit is quite high at around 85 mA. The current consumption can exceed 100mA when most or all of the display segments are driven, and for this reason a low power voltage regulator is inadequate for the IC5 position.

The low frequency oscillator is based on IC2a and IC2b which are CMOS NOR gates. However, in this circuit they are wired as simple inverters and are used in a standard CMOS astable configuration. Note that the operating frequency of the oscillator is much higher than the frequency at which readings are taken, since ten output cycles are needed from this oscillator in order to complete one reading cycle.

IC3 and IC4a form the control logic block. IC3 is a CMOS 4017BE one-of-ten decoder, and this has ten outputs ('0' to '9') which each go high, in sequence, for a single input cycle. In this circuit output '0' provides the reset pulse to the counters. Output '1' then goes high and triggers the monostable which generates the gate pulse for the clock/counter circuit. Outputs '2' to '8' are unused, and the period during which these go high provides time for the gate pulse to finish and the count to be completed. Output '9' provides the pulse that latches the new reading onto the display, but a negative latching pulse is required. IC4a is therefore used to invert the signal so as to give a suitable pulse. The timing diagram, Figure 4, shows the sequence of events and may help to clarify operation of the unit.

The monostable multivibrator is a conventional CMOS type which is formed from two 2 input NOR gates (IC4b and IC4c). Although a very simple form of monostable, it has characteristics which make it well suited to the present application. It is a non-retriggerable type, and consequently it can provide an output pulse that is shorter than the trigger pulse from IC3. This is important, as with a retriggerable type the minimum display reading would be quite high. The self capacitance of the circuit is quite low, and this is important as a high level of local capacitance would upset the linearity of the circuit, and would give a large minimum display reading. On the prototype the display reads '000' on all five ranges with no test capacitor connected.

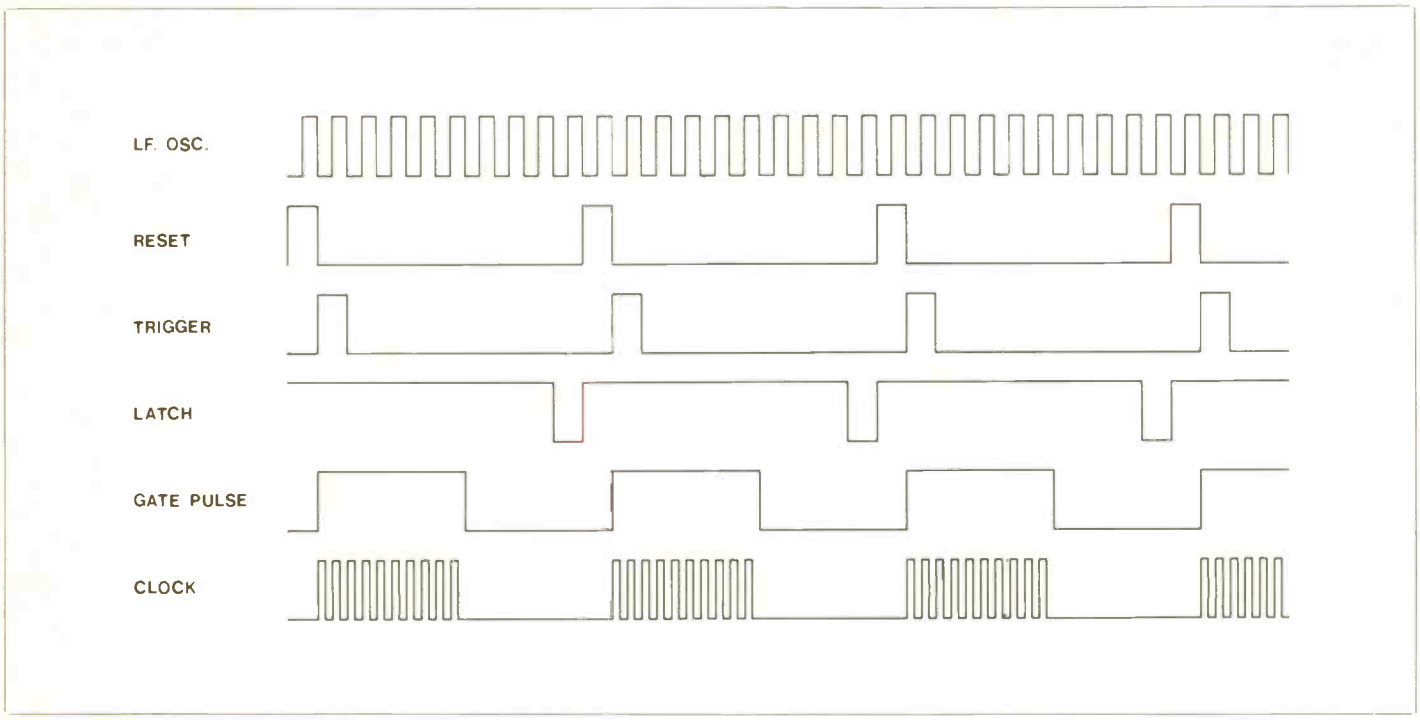


Figure 4. Timing diagram.

R5 to R9 are the range resistors, and by reducing the timing resistance in decade steps the timing capacitance needed for a given reading is boosted in decade increments. Provided the range resistors have a tolerance of 1% or better, this arrangement seems to give consistent results, and there is no need to have each range individually calibrated. R1 and S1a are used to drive the decimal point segment of the appropriate display, except on Range 3 (999nF) where no decimal point indication is needed.

The clock oscillator is a standard 555 astable circuit. RV1 controls the clock frequency, and this is used to calibrate the unit. The output of the monostable drives pin 4 of IC1, and the clock oscillator is only operative during the gate period. This avoids the need for a separate signal gate.

Turning our attention to Figure 3 now, the counter circuit is based on three CMOS 40110BE devices. These are perhaps not the best known of the CMOS logic family, but they are very versatile components which deserve greater usage. They are actually up/down counters with separate clock inputs and carry/borrow outputs. As it happens the ability to operate in a down counter mode is of no value here, and the down clock input is simply tied to the negative supply rail. The three counters are wired in series to give a standard three digit display, with IC9 providing the least significant digit and IC7 furnishing the most significant digit. The 40110BE contains a decade counter, a seven segment decoder, and a latch/display driver circuit. Each chip can therefore replace a standard three chip TTL style counter/driver/latch arrangement. The outputs can directly drive a common cathode seven segment LED display and, unusually for a CMOS logic device, a high drive current is available from each output. Even with a supply potential of just 5 volts it is essential to drive each display segment via a current limiting resistor in order to keep the current consumption of the unit down to a reasonable level.

The 'carry' output of IC7 is fed to the clock input of IC6, which is a dual D type divide by two flip/flop, but in this circuit only one section of the device is utilised. The output of IC6 changes state in the event of an overload, but with a severe overload there could be several output cycles from IC7. Directly driving the LED indicator LED1 from IC6 would not be totally satisfactory, since this output is transitory and the LED might only give one or two brief flashes which could easily be missed. To avoid this the output of IC7 is used to drive a simple set/reset bistable circuit formed from two otherwise unused gates of IC2, and the latch drives LED indicator LED1. Both IC6 and the latch are reset from IC3 so that the overflow circuit starts afresh when a new reading is taken.

Safety First

Simple but important additions to the circuit (in Figure 2) are the two extra sockets at the input (SK3 and SK4) and capacitor C6. The purpose of SK3 is to enable test components to be discharged between SK1 and SK3 prior to connecting them across SK1 and SK2 and making a measurement. This applies only to components which have been in use in a circuit and might contain a residual charge prior to testing. Higher value types which have been used in fairly high voltage circuits are the ones which are most likely to cause problems. Of course, in extreme cases capacitors must be slowly discharged through a 'bleed' resistor before removing them from the circuit. This is as much for your own protection as for that of the capacitance meter, and great care must be exercised when dealing with charged, high voltage components of other than very low values. Building a protection system into the meter input circuit was considered, but it is difficult to produce a really effective circuit that does not impair the performance of the unit. This simple alternative was therefore considered to be the more practical solution to the problem.

C6 is a built-in calibration capacitor. This is not an essential part of the unit, but it is handy when initially calibrating the unit, and therafter it is very useful to have a calibration component that is always immediately available for testing purposes. If a test component gives a slightly erroneous reading it is then just a matter of switching to range 1, connecting SK2 to SK4 to connect C6 into circuit, and then checking that a valid reading is obtained (4.70nF). A word of warning is due here though, and this is simply to point out that the meter itself is only likely to be accurate to within a couple of percent or so, except at values equal to or close to the calibration value. Another point to bear in mind is that the values of capacitors are dependent on temperature and other factors. If a test component should happen to give a reading that is in error by slightly more than its tolerance, this probably means that it is perfectly satisfactory rather than faulty.

Construction

Virtually all the components fit onto the printed circuit board, and details of the board are provided in Figure 5. Construction of the board is not particularly difficult, but there are a few points which should be borne in mind when assembling it. The main point to note is that, apart from IC1 and IC5, the integrated circuits are CMOS types, and

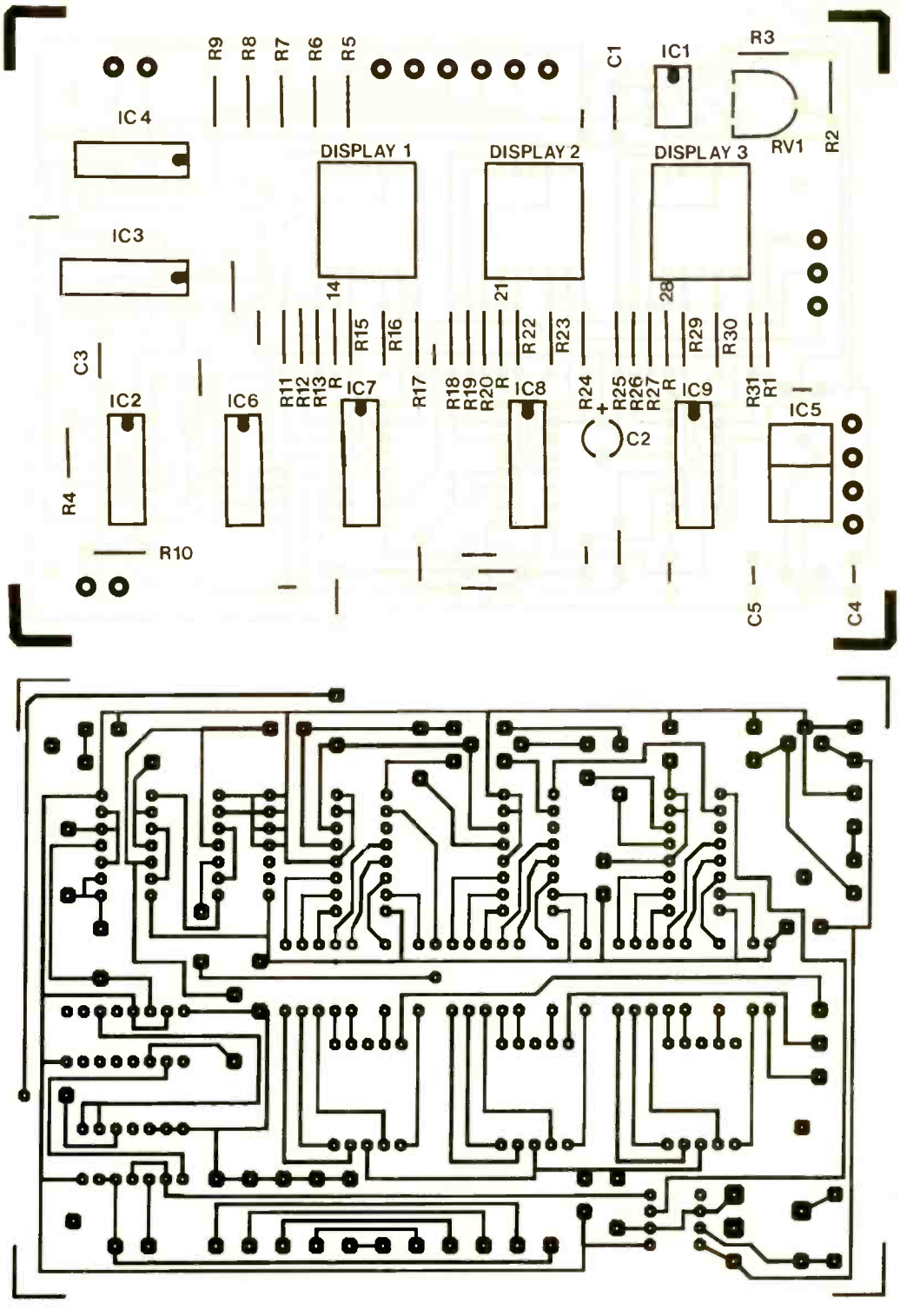


Figure 5. PCB layout and component references.

are therefore vulnerable to damage by static charges. To avoid this they should be fitted in integrated circuit holders, but not be plugged into circuit until the board has been completed and wired to the off-board components (see Figure 6). Until then they should be left in the anti-static packaging. Handle the devices as little as possible when fitting them into the holders, and be particularly careful with the three counter ICs, which are not the cheapest of CMOS devices. If in any doubt, or you are not an experienced constructor, then read the Constructor's Guide leaflet supplied with this kit.

IC5 is mounted horizontally on the board and it is a good idea to use a short 6BA or M3 screw and matching nut to fix it securely to the board.

The three seven segment LED displays are mounted in holders which help to raise them to a suitable height above the surface of the board as well as reducing the risk of heat damage when connecting them. Suitable ten pin holders seem to be unavailable, but it is not difficult to improvise suitable holders from three ordinary 14-pin DIL integrated circuit holders. First the holders are cut in half lengthwise using a hacksaw to give six seven pin SIL types. The pins at each end of the holders are then pushed out using pliers or simply trimmed off using wire clippers. This leaves six 5-pin SIL holders which can be used for the displays. The spacing between the displays is sufficient to make it unnecessary to trim off the excess pieces at each end of the holders.

Pins are fitted to the board at the positions where connections to off-board components will be made. There are a number of link wires (sixteen in fact) and these are made from about 22 s.w.g. enamelled copper wire, or trimmings

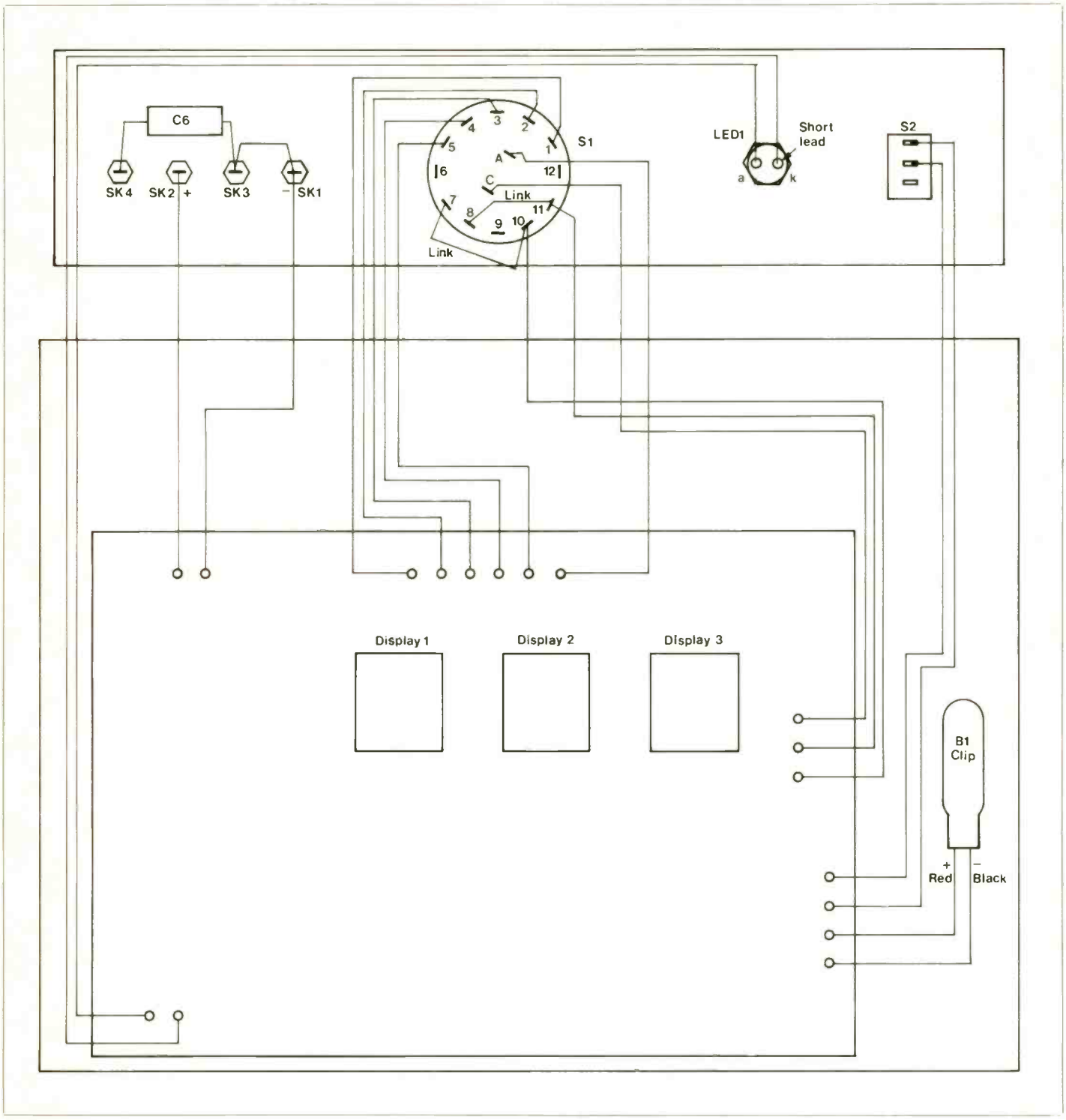
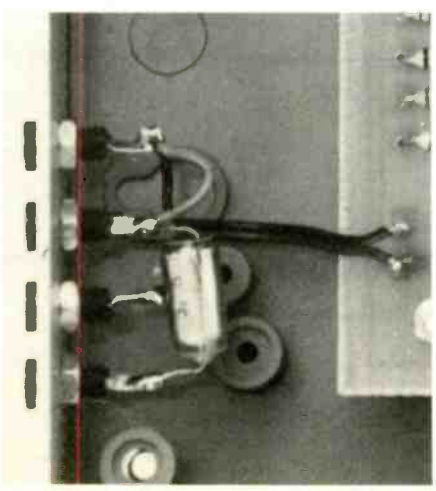


Figure 6. Wiring.

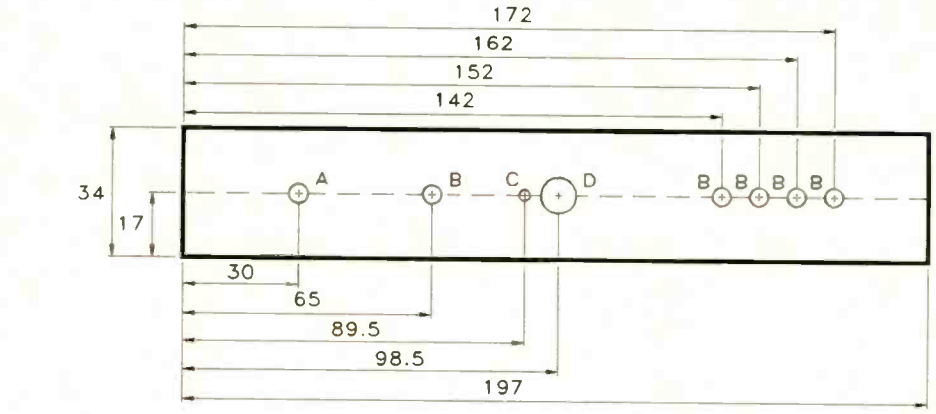
from resistor lead-out wires can be used.

A Verocase having approximate outside dimensions of 205 by 140 by 40 millimetres makes a good housing for this project. It is used vertically with a display window cut in the front panel (which would normally be the top panel), while the controls and sockets are mounted on the top panel (which would usually be the front of the case). The printed circuit board is mounted on the rear panel using one inch long 6BA screws and half inch spacers, which are needed to bring the fronts of the displays close to the display window. The board is positioned well towards the bottom left hand corner of the unit so as to bring the display close to the middle of the front



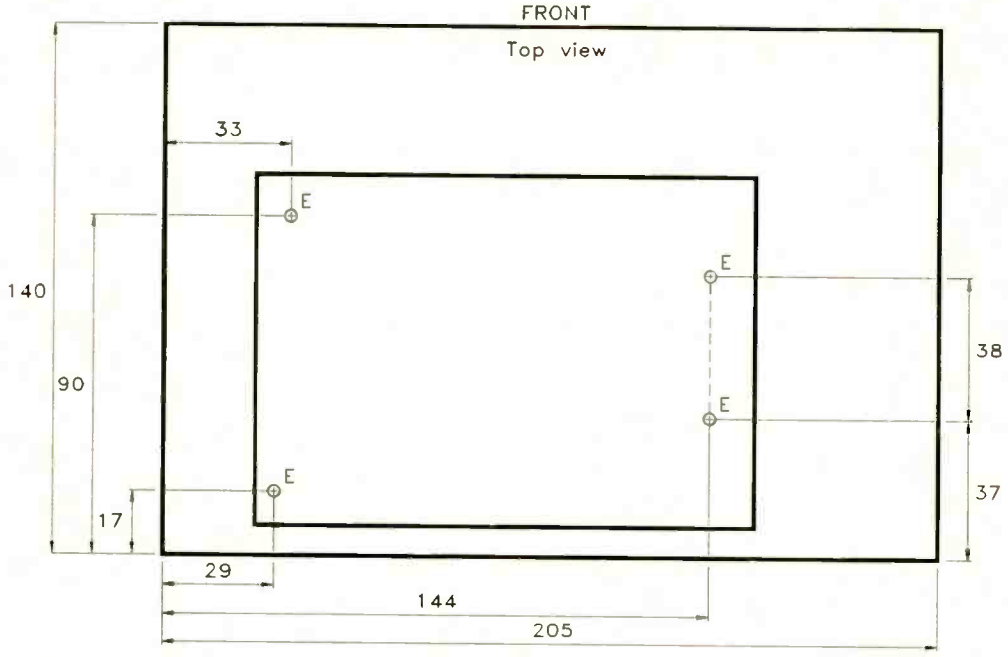
panel. The display window must obviously be positioned accurately in front of the display, and it can be cut using a fretsaw, coping saw, or a miniature round file. A piece of red display filter is glued in place over or behind the cutout, and any general purpose material is suitable for this. Note that the Maplin display filter material has an anti-glare finish on one surface, and this less reflective surface should be the one that faces forward or outwards.

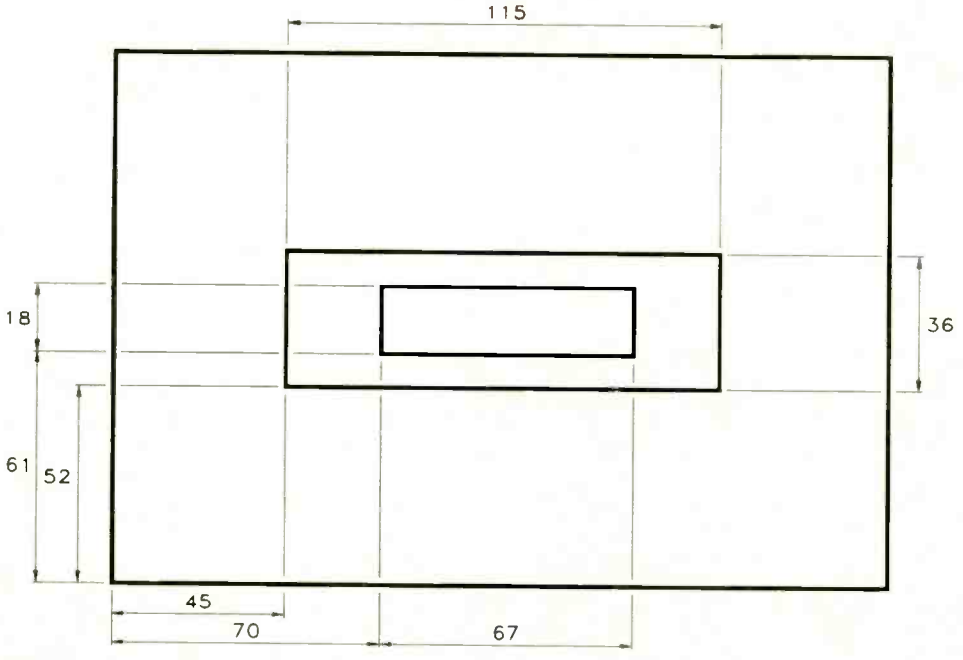
On the prototype SK1 to SK4 are 1 millimetre sockets mounted with about 9.5 millimetres spacing. C6 is mounted direct across SK3 and SK4 so as to minimise stray capacitance, and preserve good accuracy at low readings.



REF.	SIZE
A	ø5.2
B	ø5
C	ø3
D	ø9.5
E	ø3.2

All sizes in millimeters
Scale = 1:2





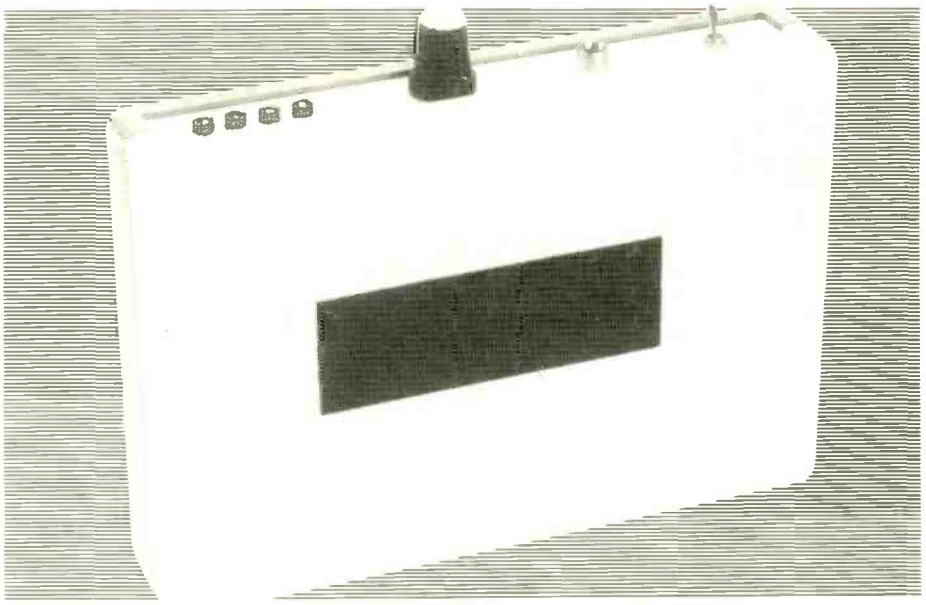
Drilling details.

Most capacitors will plug straight into SK1 and SK2 satisfactorily. However, some types, especially miniature printed circuit mounting polyester types will not, and a set of test leads should be made up so that these can be accommodated. All that is needed here is a pair of short insulated leads fitted with 1 millimetre plugs to connect to SK1 and SK2, and small crocodile clips which connect to the component under test.

S1 is a six way switch having an adjustable end-stop which is set for five way operation. Details of the wiring to S1 are shown in Figure 6. LED1 is specified as a panel mounting LED, but if preferred it would not be difficult to utilise the otherwise unused decimal point segment of display 3. If six HP7 size cells in a plastic holder are used as the power source, the connection to the holder is made by way of a standard PP3 style battery connector. It has to be emphasised that a reasonably high capacity battery is needed due to the high current consumption of the circuit, and a small type such as a PP3 is not adequate.

Calibration

In order to calibrate the unit it is necessary to have a close tolerance capacitor of a value that represents about 50 to 100% of the full scale value of one range. Assuming that C6 has been included in the unit and will be used to calibrate it, set the unit to range 1 (9.99nF full scale) and place a shorting link across SK2 and SK4. Then carefully adjust RV1 for the correct display reading of 4.7nF. The unit should then give appropriate readings if it is tried with a range of capacitors, but do not expect



readings to be absolutely spot on. The capacitance meter itself is reasonably accurate, although, as explained previously, it will almost certainly produce small errors. Most capacitors have quite high tolerances though, with few types having an accuracy of better than 5%, and 20% being quite typical. With electrolytic types a tolerance of +50% and −20% is quite normal. Really the inclusion of a third digit in the display is not justified in terms of the required accuracy, but it is useful in that it effectively extends the minimum capacitance which the unit can read by a full decade. If you hold a capacitor in place across the sockets you may well find that the displayed readings steadily increase. This does not indicate a fault in either the capacitor or the capacitance meter, it is simply due to heat from your fingers causing the value of the capacitor to rise slightly. When holding a capacitor in place across SK1 and SK2, always hold the body of the component and do not touch either of the lead-out wires.

High value capacitors can be checked by wiring them in series with a lower value type and then measuring the series capacitance of the two components. For example, a 470µF component could be checked by wiring it in series with 100µF capacitor. The series capacitance is equal to (C1 x C2)/(C1 + C2), which in this example is (470 x 100)/(470 + 100), which gives 47000/570, and a final value of 82.5µF. The capacitors will presumably be electrolytic types, but the polarity of both components is unimportant.

DIGITAL CAPACITANCE METER PARTS LIST

RESISTORS: All 0·6W 1% Metal Film (Unless specified)

R1	560Ω	1	(M560R)
R2,8	10k	2	(M10K)
R3	33k	1	(M33K)
R4	470k	1	(M470K)
R5	10M	1	(M10M)
R6	1M	1	(M1M)
R7	100k	1	(M100K)
R9	1k	1	(M1K)
R10-31	470Ω	22	(M470R)
RV1	47k Hor Encl Preset	1	(UH05F)

CAPACITORS

C1	1nF Poly Layer	1	(WW22Y)
C2	470µF 16V PC Elect	1	(FF15R)
C3	100nF Poly Layer	1	(WW41U)
C4,5	100nF 16V Minidisc	2	(YR75S)
C6	47nF 1% Polysty	1	(BX64U)

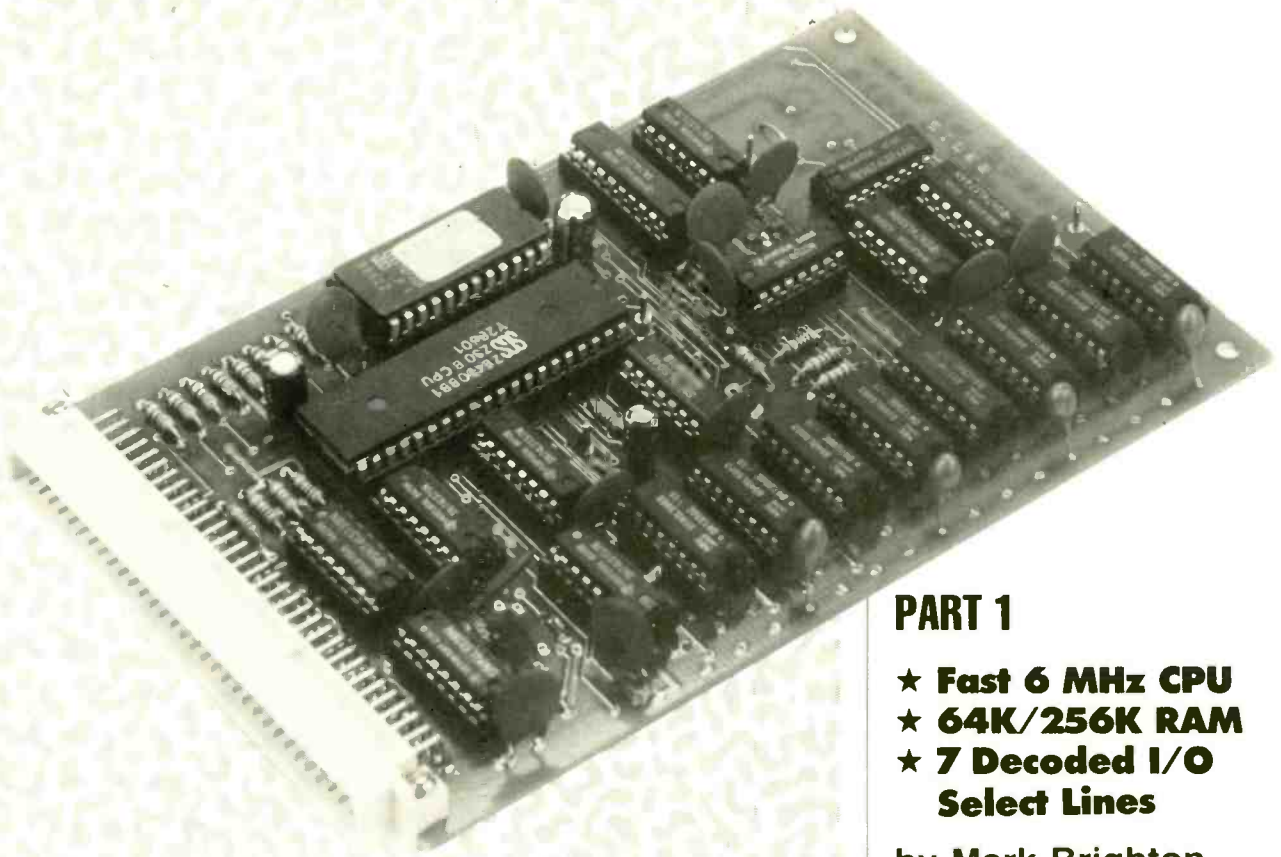
SEMICONDUCTORS

IC1	NE 555	1	(QH66W)
IC2,4	4001BE	2	(QX01B)
IC3	4017BE	1	(QX09K)
IC5	µA7805UC	1	(QL31J)
IC6	4013BE	1	(QX07H)
IC7-9	40110BE	3	(QW68Y)

MISCELLANEOUS

Display 1-3	Display Type 4 ½ ir	3	(FR41U)
LED1	Chrome LED Large Red	1	(YY60Q)
S1	Rotary SW6	1	(FH43W)
S2	SPST Ultra Min Toggle	1	(FH97F)
SK1-4	Socket 1mm Black	4	(WL59P)
	DIL Socket 8-pin	1	(BL17T)
	DIL Socket 14-pin	6	(BL18U)
	DIL Socket 16-pin	4	(BL19V)
	Verobox 201	1	(LL05F)
	PCB	1	(GD59P)
	Low-Cost Collet Knob	1	(YG40T)
	LC Cap Grey	1	(QY03D)
	PP3 Clip	1	(HF28F)
	Filter Red	1	(FR34M)
	Bolt 6BA × 1 in.	1 Pkt	(BF07H)
	Nut 6BA	1 Pkt	(BF18U)
	Spacer 6BA × ¼ in.	1 Pkt	(FW34M)
	Pin 2145	1 Pkt	(FL24B)
	Instruction Leaflet	1	(XT76H)
	Constructors' Guide	1	(XH79L)

The above items are available as a kit:
Order As LM28F (Digi Cap Meter Kit).
The following item (which is included in the kit) is also available separately.
Capacitance Meter Bd **Order As GD59P.**



FRAME STORE

PART 1

- ★ Fast 6 MHz CPU
- ★ 64K/256K RAM
- ★ 7 Decoded I/O Select Lines

by Mark Brighton

Z80B CPU CARD

This article describes the first part of a modular Z80 based micro-controller system, designed to meet the needs of a wide range of control monitor and display applications, where it is often not desirable to dedicate a home micro to a single task. Some applications for the system will be presented in future issues of "Electronics", the first being as part of a video display for WEFAX weather satellite pictures, received by the "Mapsat" Receiver/Decoder System, described in previous issues.

Two expansion modules are under development at the time of writing, a parallel/serial I/O card using the Z80 SIO and DART peripheral chips, and a high resolution graphics card using the Yamaha/Microsoft V9938 MSX graphics processor. These modules will be connected to the Z80B CPU card by means of a common motherboard, the whole system being in eurocard format.

The modules themselves will be equipped for expansion, being supplied as a basic kit, with optional extra parts to bring them up to full capability. In this way it is hoped that the system may be tailored by the user to suit his/her particular application (and finances!), without the built in redundancy that often results from using 'off-the-peg' computers (high resolution colour graphics and six octave polyphonic sound are a little excessive for a central heating controller or a home security system!).

The CPU card described here is no exception to the expandable concept just out-lined, being supplied in basic form as a 'bare bones' minimum computer circuit which forms the foundation module of

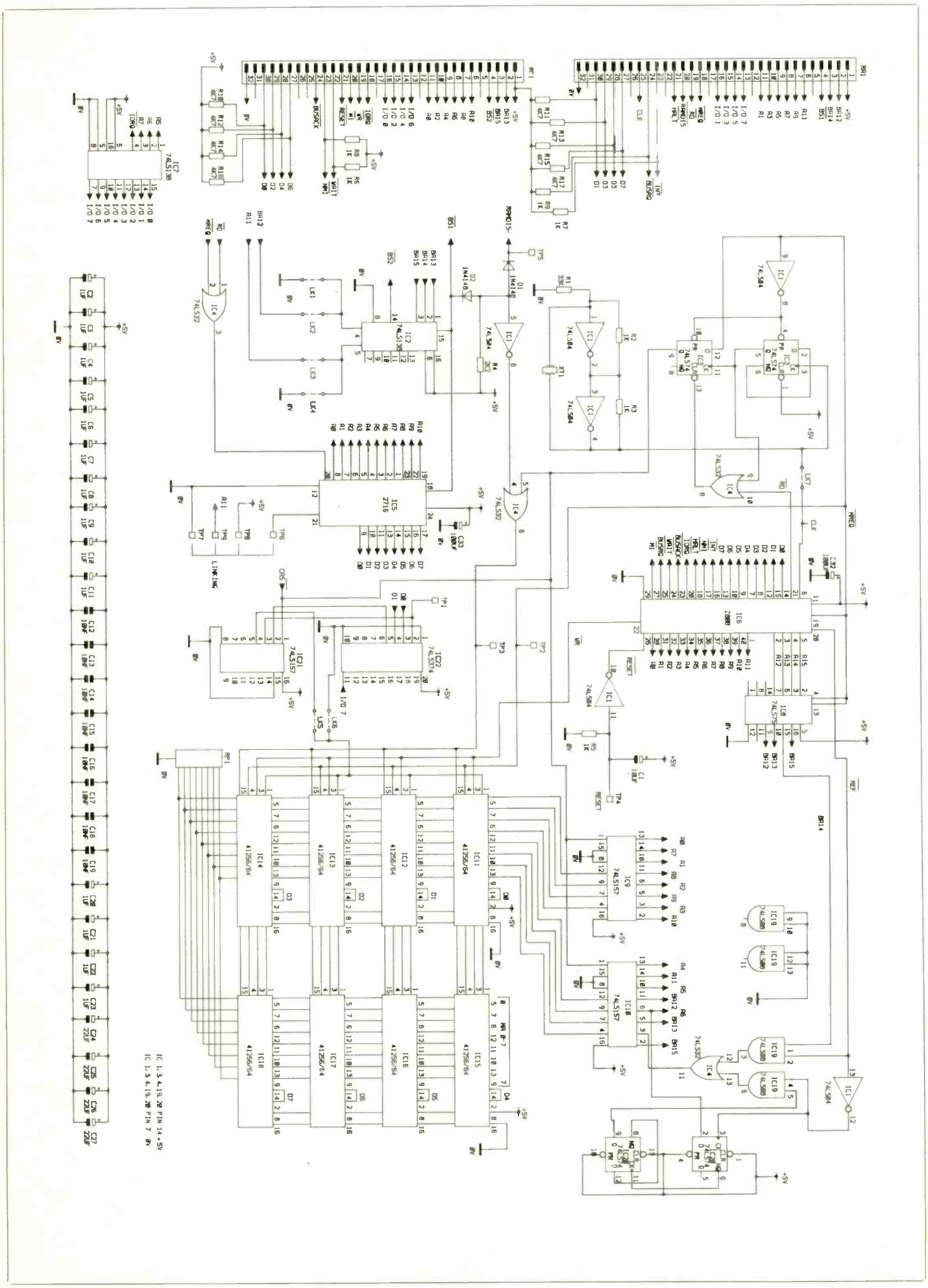


Figure 1. Circuit Diagram.

any dedicated system built up by the addition of a combination of expansion modules. Optional parts for this board consist of a number of logic chips which provide all the multiplexed address and refresh circuitry for dynamic RAMs, with linking options to enable the use of 64K or 256K DRAMs. The operation of these circuits will be covered at the end of the following basic circuit description.

NOTE: Only the basic kit is required for the WEFAX Frame Store.

Circuit Description

The heart of the circuit, shown in Figure 1, is a Z80B CPU chip (IC6) running at 6.144MHz, which makes it half as fast again as its older brother the Z80A, still to be found in many popular personal computers. The clock circuit is formed by inverters IC1a and IC1b, R1, R2, R3 and XT1, and provides a system clock on the edge connector, as well as clocking the column address strobe (CAS) generator IC3 (if fitted). If an external system clock signal is available, Link 7 may be omitted and the external clock connected to the system clock pin on the edge connector (PA1.25). This should be a single phase square wave clock with a 50/50 mark/space ratio. RESET for the processor (and any other boards connected to the system) is provided via inverter IC1e by RC network R5/C1. An active high reset signal may be input on reset pin TP4 to Cold Start the system.

The four most significant address lines out of the processor (A12-A15) are buffered by IC8, a dual two bit transparent latch clocked by the Memory Request (MREQ) line from the CPU. The buffered products BA12-BA15 are taken to an address decoder chip IC2, which provides two memory mapped ROM select lines BS1, starting at $0000 and BS2 starting at $2000. These blocks may be 2K, 4K or 8K long, depending on the positions of links 1 to 4 (see Table 1).

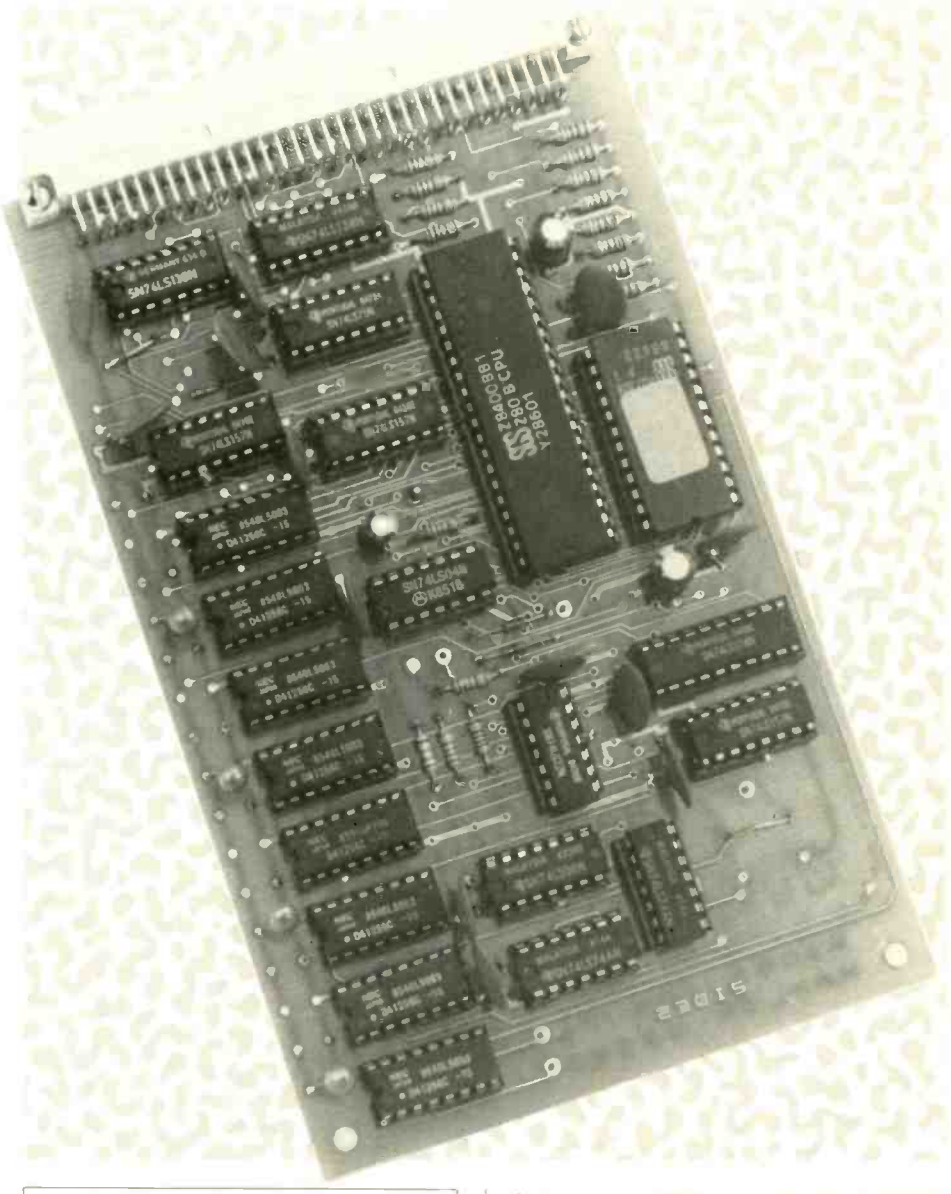
NOTE: If an external ROM/RAM is to be enabled by BS2, the RAM disable line (RAMDIS) should be connected to BS2 to avoid contention on the data bus (BS1 is already so connected, being used to enable the internal ROM).

The internal ROM position IC5 is a 24-pin standard 'byte-wide' pin-out and will accept single rail 2716 or 2732 EPROMs. When buying ROMs for this board, bear in mind that they will have to have an access time less than or equal

	LINK			
	1	2	3	4
2K	×	√	√	×
4K	×	√	×	√
8K	√	×	×	√

√ = Fit Link × = No Link

Table 1.



	LINK		
OPTIONS	1.	TP6 —	TP8
	2.	TP6 —	TP7
	3.	TP6 —	SWITCH*
	4.	TP6 —	TP9

*See Text

Table 2.

to 250ns when running the system at the maximum clock speed of 6.144MHz. In practical terms this may mean that it is not possible to use a 2716 at full clock speed, since it is usually only available up to about 350ns access time, but as the board will function quite normally at any clock speed less than maximum, some lower speed applications will suit the 2716 ROM's less frantic way of life admirably.

The function of IC5, pin 21, varies depending on the type of ROM fitted, and several strapping options have therefore been provided (see Table 2). For the sake of clarity I will summarise the options provided as follows:

1. When using a 2716 EPROM pin 21 (Vpp) should be connected to +5V during normal use.
2. If using a 2732 for reasons of speed alone, where less than 2K of space is needed for the control program, pin 21 (A11) may be linked to 0V and Links 1 to 4 wired to select a 2K ROM. Only the low half of the ROM is then used, which results in an extra 8K of RAM being available if 256K DRAMs are fitted, since the ROM overlays the first 2, 4 or 8K of each 64K block of RAM. This is unavoidable, due to the 64K address range of the Z80, and the need to have the control program accessable to the processor at any time, regardless of which block of RAM is selected.
3. When using a 2732 for programs less than 2K in length, it is possible to treat the two halves of the ROM as separate "SUBROMs", as follows. Two separate programs are developed and burnt into the EPROM along with their jump vector tables if required. The first, in the lower half of the ROM, is jumped to by means of the cold start vector, at address $0000, in the normal way. The second program is burnt into the upper half of the EPROM, from ROM address $1000 onwards. The

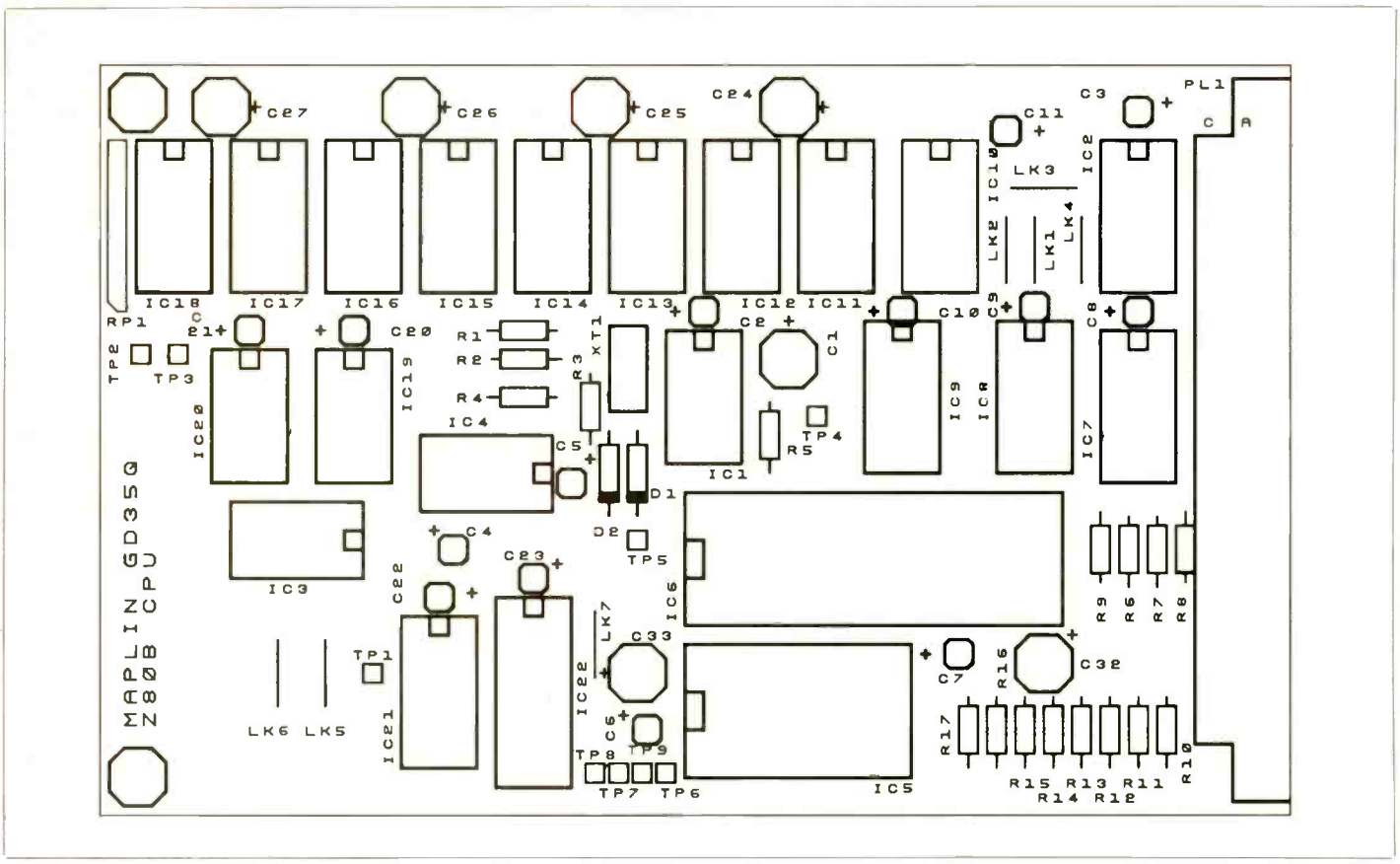


Figure 2. PCB Layout.

program is written to run from address $0000 however, including the duplicate jump vector table starting at ROM address $1000. Pin 21 on the EPROM is then wired to the centre pole of a SPDT toggle switch whose outer contacts are wired one to 5V and one to 0V. Whichever half of the ROM is selected by this switch will slot into the first 2K of the memory map, and run on power up. In this way the CPU board may fulfill two completely different functions at the flick of a switch, or run two different versions of the same program for different conditions.

4. The last option is simply to wire pin 21 on the 2732 to the processor A11 line, and select a 4K space with Links 1 to 4. This allows for up to 4K of control program/data.

The Z80 architecture allows the first 256 addresses to be used as I/O ports to control or monitor external devices. It is the common practice to interface all peripheral devices to these special I/O locations, thereby leaving the maximum space available in the memory map for ROM/RAM. IC7 decodes these addresses into eight I/O block select signals (I/O 0 - 7, active low) which may be used to enable external peripheral devices. Each block is 32 bytes long, so devices which have a number of addressable internal registers can be connected to a number of address lines (A0 - A4) to I/O map the individual registers. IC7 is enabled by the I/O request (IOREQ) line from the processor, as opposed to the usual Memory Request control line, in order to locate any devices selected by it in the I/O map instead of the memory map.

NOTE: If 256K DRAMs are fitted, I/O7 is used to enable the memory block select circuitry, and is not, therefore, available for external use.

The DRAM support circuitry consists of several stages having the following interrelationship:

Access to a memory location within a static RAM is accomplished by presenting the chip with a parallel binary address, and enabling the chip by means of a block select pulse, which is directly compatible with the information coming from the processor. Dynamic RAMs, however, are not arranged as a long linear sequence of locations, but as a two dimensional matrix. They therefore require a two part address to access any one location, a row address and a column address. To further complicate matters, both addresses are input on the same set of inputs to reduce the pin count of the chip, so separate row and column address strobes have to be derived to clock the addresses into the DRAMs. In this design, the processor MREQ signal provides the row address strobe (RAS) and IC3, a dual D-type flip/flop, along with IC1d and IC4c, derives the column address strobe (CAS) from MREQ, CLK and RD. The length of the CAS pulse depends on whether the access to RAM is a write cycle or a read cycle, CAS starting later for write cycles to prevent the DRAMs placing data on the bus at the same time as the processor. The CAS signal is gated to the DRAMs via IC4b, which blocks the CAS signal during ROM access, thus preventing the DRAMs from responding to a READ in the ROM address space. Row and column addresses are formed by splitting the address bus into two groups, the eight least significant bits being presented during RAS time, and the most significant during CAS time via multiplexer chips IC9 and IC10.

Dynamic RAM chips must be accessed at certain periodic intervals in order to retain their contents. This process is called 'refresh' and the Z80 has a built in refresh control line to simplify the refresh circuitry required. The refresh mode chosen for this circuit is called 'RAS Only Refresh', which requires that all rows be accessed within the stipulated refresh period (in the case of the 41256 DRAM refresh cycle time is 4ms maximum). Fortunately the Z80 has a built in refresh counter which generates the row addresses, places them on the bus when it is otherwise unused, and outputs a pulse on the refresh line, so it would seem that little or no external circuitry would be required. Unfortunately, since the basic design of the Z80 is getting a little long in the tooth, the refresh address is intended for the older generation of DRAMs, which only required a six bit refresh address as opposed to the current generation which requires a seven bit address. This limitation is overcome by using the top bit of the Z80 refresh counter to clock an external one bit counter formed by IC20, a dual D-type flip/flop. The output of this counter, (FA7), is switched in to replace

BA14 during refresh time by IC1f, IC19a, IC19b and IC4d.

NOTE: If using the WAIT input to interface slow peripherals etc. it should be noted that refresh of DRAMs will cease for as long as WAIT states exist in the processor. Use of BUSRQ will have a similar effect.

If 64K DRAMs are fitted, no block switching of RAM is necessary, so IC21 and IC22 may be omitted, and Link 6 wired in to select 64K RAM. Where 256K DRAMs are used, Link 5 should be fitted. Fit only Link 5 or Link 6, not both! IC22 is an eight bit latch, I/O mapped between $E0 and $FF. The two least significant bits of data written to this port determine which RAM block is slotted into the memory map (%XXXXXX00 to %XXXXXX11). This Block Select Address is then multiplexed onto the DRAMs' MA8 line by IC21.

If DRAMS are used and an external clock is required, you must not omit Link 7. Instead omit R3 and XT1, and bend up pin 4 of IC1 so that it does not make contact with its socket. This ensures that IC3 and IC4 are still able to provide RAM refresh.

Construction

Before commencing construction of this unit, read the Constructors' Guide which accompanies the kit. Referring to the pcb legend and Parts List, insert and solder all resistors, capacitors and IC sockets. Special care should be taken to ensure that no short-circuits are created whilst soldering, especially around the IC sockets. Links should now be fitted as required; these are described in Tables 1 and 2. Link 7 should also be fitted if using the 6.144 MHz internal clock.

Bolt the 64-way edge connector into position on the pcb, and solder the pins onto the board. Fit all ICs carefully into their sockets noting correct orientation. This completes assembly of the unit.

For reference purposes, Figure 3 shows the functions of the 64 pins on the edge connector.

Testing and Use

Those of you who are building this project as part of the WEFAX Satellite Display System need not worry overmuch about this section, unless you have access to a Z80 assembler and EPROM programmer, and are particularly interested in getting to grips with the working of the system. The Frame Store Project will include a ROM which will contain a program to input and display picture information from the MAPSAT decoder. This may be used to test the complete system.

It is not practical to test all facilities on a CPU system such as this without specialised test equipment, and/or a huge set of machine code test routines. Therefore the test routine included here in Listing 1 is a simple 'go/no-go' test which, when run, will take the RAM block select line at TP1 alternately high and low, each cycle occurring at (approx.) one second intervals. This may be monitored with a multimeter, oscilloscope, logic probe or a light emitting diode in series with a 470Ω resistor.

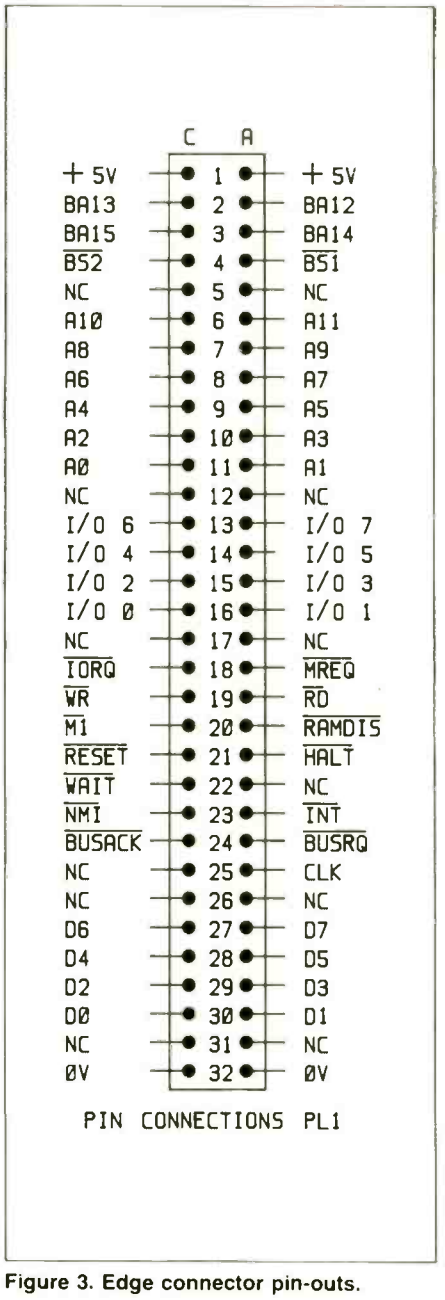


Figure 3. Edge connector pin-outs.

NOTE: This test requires that a 74LS374 is fitted at IC22.

Listing 1 was produced using the Amstrad CPC128 and Hisoft assembler, but it should not prove too difficult to enter the program on any other Z80 assembler system providing the following stipulations can be met.

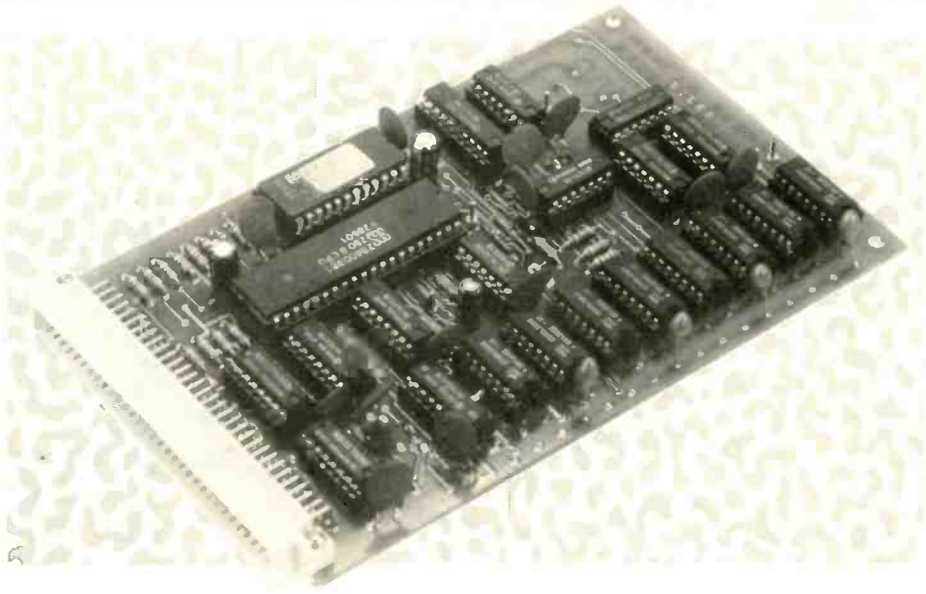
1. The assembler should be capable of assembling programs to run in the first 2K, 4K, or 8K of memory (the host machine will probably have a ROM in this area and it will not therefore be possible to assemble a program to actually reside in it), either to disk or tape or some other area of memory. If this is not possible, the program will have to be manually re-coded to correct jump instructions, etc.
2. Those of you who are not using a full blown development system, with on-board EPROM programming or ROMulation facilities, will know that it can be very tedious entering a hexadecimal version of your program manually on EPROM programmers such as the Softy. This can be overcome on EPROM programmers having an RS232 interface (Softy, Gang-of-eight plus, etc.), by down-loading the assembled program directly into the programmer having first converted the object code file information into a format which the programmer can accept. This obviates the need for much laborious typing, and makes the process of testing and subsequent evolution of programs far easier. Information about the data formats required by the programmers is usually included in the handbooks accompanying them.

```
0100                    10          ORG   #0100
0100                    20          ENT   $
00FD                    30 PORT:    EQU   #00FD
0100  3EFF              40 START:   LD    A,#FF
0102  D3FD              50          OUT   (PORT),A
0104  01FFFF            60          LD    BC,#FFFF
0107  0B                70 LOOP1:   DEC   BC
0108  78                80          LD    A,B
0109  B1                90          OR    C
010A  20FB             100          JR    NZ,LOOP1
010C  3E00             110          LD    A,#00
010E  D3FD             120          OUT   (PORT),A
0110  01FFFF           130          LD    BC,#FFFF
0113  0B               140 LOOP2:   DEC   BC
0114  78               150          LD    A,B
0115  B1               160          OR    C
0116  20FB             170          JR    NZ,LOOP2
0118  C30001           180          JP    START
```

Listing 1.

NOTE: It is not possible to use the ROMulation facilities of some systems on this Z80B card since their slower clock speeds can cause timing problems upon access.

While it is not possible to present any further information about the use of such an open ended system here, application information will be included in this magazine as it becomes available. In the meantime, I would be glad to receive any comments concerning application details or criticism (preferably constructive) developed by readers or users of the system. Application information received may, if of sufficient interest, be considered for inclusion in future issues of this magazine, and should be addressed to myself at the Magazine address.



Z80B FRAME STORE CARD PARTS LIST

RESISTORS: All 0·6W 1% Metal Film (Unless specified)

R1	33k	1	(M33K)
R2,3,5-9	1k	7	(M1K)
R4	2k2	1	(M2K2)
R10-17	4k7	8	(M4K7)
RP1	SIL Resistor 2k2	1	(RA28F)

CAPACITORS

C1	470nF 35V Tant	1	(WW58N)
C2-11,20-23	1μF 35V Tant	14	(WW60Q)
	100μF 10V PC Elect	2	(FF10L)

SEMICONDUCTORS

D1,2	1N4148	2	(QL80B)
XT1	6·144MHz MP Crystal	1	(FY83E)
IC1	74LS04	1	(YF04E)
IC2,7	74LS138	2	(YF53H)
IC3	74LS74	1	(YF31J)
IC4	74LS32	1	(YF21X)
IC6	Z80B CPU	1	(UF74R)
IC8	74LS75	1	(YF32K)

MISCELLANEOUS

PL1	RAPL64AC Connector	1	(FJ51F)
	DIL Socket 14-pin	5	(BL18U)
	DIL Socket 16-pin	6	(BL19V)
	DIL Socket 20-pin	1	(HQ77J)
	DIL Socket 24-pin	1	(BL20W)
	DIL Socket 40-pin	1	(HQ38R)
	Z80B CPU Card	1	(GD35Q)
	Steel Screw M2·5mm	1 Pkt	(JY31J)
	Steel Nut M2·5mm	1 Pkt	(JD62S)
	Shake Washer M2·5mm	1 Pkt	(BF45Y)
	Instruction Leaflet	1	(XT77J)
	Constructors' Guide	1	(XH79L)

OPTIONAL (Not in Kit)

IC5	2716 for 450ns	1	(QQ07H)
	or 2732 for 350ns	1	(QQ08J)
	or 2732 for 200ns	1	(UH88V)

In addition to the basic CPU the following RAM extensions are shown below:

	Decoupled DIL Socket 16-pin	8	(FP79L)
C24-27	47μF 16V Tantalum	4	(WW76H)
IC9,10	74LS157	2	(YF61R)
IC19	74LS08	1	(YF06G)
IC20	74LS74	1	(YF31J)

OPTIONAL: 64K RAM version

IC11-18	4164	8	(QQ06G)

OPTIONAL: 256K RAM version

IC11-18	41256	8	(QY74R)
IC21	74LS157	1	(YF61R)
IC22	74LS374	1	(YH16S)

The above items (excluding optional) are available as a kit:
Order As LM29G (Z80B CPU (Basic) Kit).
The following item (which is included in the kit) is also available separately.
Z80B CPU Card **Order As GD35Q.**

SERVO TESTER

★ Two Automatic Check Modes.
★ Manual Switch Incorporated.
★ Checks Servo Travel, Sensitivity, Transit Times and Overshoot.
★ Simple Construction.

by Dr. Mike Roberts

This tester has been designed to measure the performance of servos and aid fault finding. It allows manual adjustment of the servo output and has two automatic modes. In the first automatic mode the output signal is slowly changed from one end of the range to the other and back again. This tests the slow response of the servo (regulator response). The speed of change is adjustable from about 0.2 seconds to 50 seconds for full travel. The second automatic mode switches the output signal from one end of the range to the other. This tests the fast response of the servo (servo response). The time between switching is adjustable over the same range as in the first automatic mode.

The signal that has to be generated is a train of positive pulses each of length between 1ms and 2ms at a repetition rate (frame) of 20ms. A 1ms pulse represents one end of the servo travel, and a 2ms pulse the other. Pulses in between these values drive the servo proportionally between the two extremes.

Circuit Description

The circuit is shown in Figure 1. It is built up from three sections. These are: the frame generator, a voltage controlled pulse width generator, and a waveform generator.

The frame generator centres around IC1b and c. This is a standard CMOS

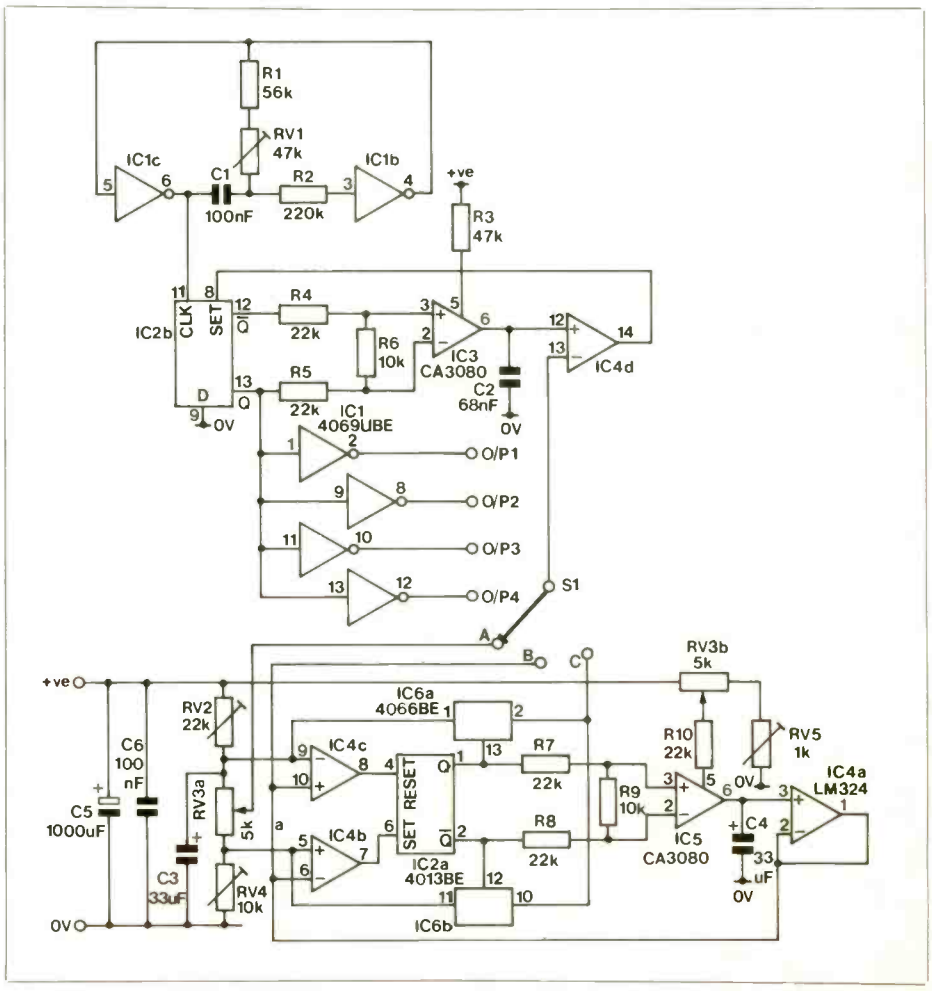


Figure 1. Circuit diagram.

oscillator circuit. It generates a square wave with a frequency which corresponds to the desired 20ms frame. The frame length can be adjusted by RV1. However, this adjustment is not critical, as will be seen later, and those without access to timing equipment can happily leave RV1 in its mid-position.

Both the pulse generator and the waveform generator use the CA3080 operational transconductance amplifier to generate triangular waveforms. This amplifier is similar to conventional operational amplifiers except that it is the output current rather than the output voltage that is proportional to the difference in input voltages. Also, the gain of the amplifier is set by the current allowed into pin 5 (amplifier bias current). The amplifier responds linearly for input voltage differences up to 0.1V. At this point the maximum output current is achieved. This maximum current is equal in magnitude to the amplifier bias current.

A ramp waveform can be generated by applying a fixed current to a capacitor. The rate of rise is governed by:

$$\frac{\text{Voltage (V)}}{\text{Time (s)}} = \frac{\text{Current (A)}}{\text{Capacitance (F)}}$$

A triangular waveform can be generated by alternating the direction of the fixed current. The CA3080 is a convenient device to use to achieve this. By alternating the input voltage differential from +1V to −1V, the output current is at the maximum (saturation) level (equal to the amplifier bias current) and the direction alternates with the polarity of the input.

Now back to our circuit. The pulse generator produces pulses of width between 1 and 2ms. The length is governed by the input voltage (from the waveform generator), and the repetition rate is governed by the frame generator.

IC3 is the CA3080 operational transconductance amplifier. IC4d is a voltage comparator, and IC2b is a 'D' type flip-flop. In its idle state Q is high (5V) and $\overline{Q}$ is low (0V). Hence IC3 is trying to discharge C2. However, when C2 is completely discharged it can go no further and it sits close to 0V. When a rising edge is received into the clock input of the flip-flop, the Q output is set equal to the 'D' input, i.e. 0V. Conversely, $\overline{Q}$ flips to 5V. This gives a positive voltage to IC3 and it starts charging C2. Initially the voltage on C2 is lower than the control voltage. Hence the output from IC4d is low (0V). The voltage on C2 rises at a steady rate set by R3 and C2. When this voltage exceeds the control voltage, the output of IC4d goes high (5V). This immediately 'SETS' the flip-flop, i.e. Q = high (5V), $\overline{Q}$ = low (0V). This in turn reverses the input to IC3 and C2 starts to discharge.

The time that Q is low is set by the rate of rise of the voltage on C2 and the control voltage. The rate of rise of the voltage on C2 is fixed. Hence the length of time that Q is low is proportional to the control voltage. The output from Q is inverted and buffered by IC1a, d, e, and f, so that up to four servos can be driven at once. Overall then, the output pulses are of length governed by the input voltage and the repetition rate is set by the frame generator. The various waveforms are shown in Figure 2.

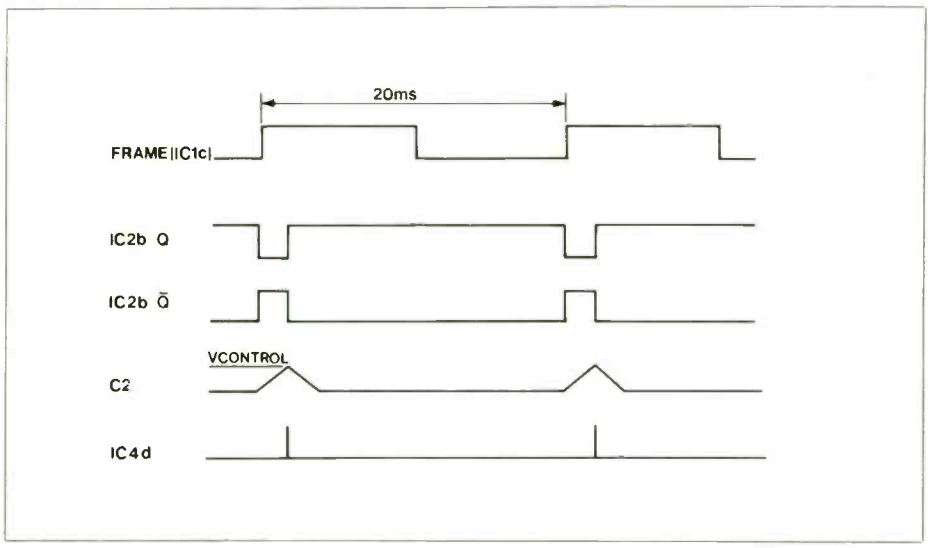


Figure 2. Waveforms.

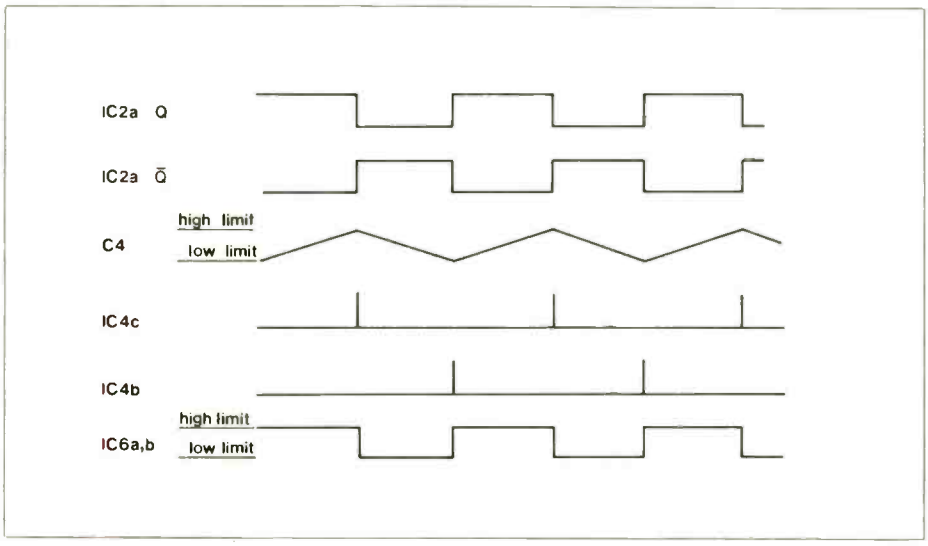


Figure 3. More Waveforms.

The waveform generator produces one of three outputs. These are all generated at the same time but only one is selected by S1. The outputs are: manually controlled output, triangular wave output (for testing the 'regulator' response) and a square wave output (for testing the 'servo' response).

The manual output is adjusted by RV3a. The low and high limits are governed by RV2 and RV4. These are normally set so that the minimum and maximum voltages correspond to output pulses of 1ms and 2ms. These limits also set the high and low points on the triangular and square waveforms.

The triangular waveform is generated using the CA3080 IC (IC5) to switch a fixed current in and out of a capacitor (C4). The frequency of the waveform generated is a function of the time taken for the voltage on C4 to change from the high limit to the low limit and back again. This is governed by the amplifier bias current, which is set by RV3b. The slowest time is set by RV5. The direction of the output current from IC5 is governed by the 'D' type flip-flop IC2a in a similar manner to the pulse generator. However, IC2a is driven in a different way. Whilst the voltage on C4 is in between the high and low limits the outputs from IC4b and IC4c are low. When the voltage on C4 exceeds the high limit the output on IC4c goes high and resets IC2a. This then makes Q low and $\overline{Q}$ high and C4 starts to discharge. When the voltage on C4 goes below the low limit IC4b sets IC2a and C4 starts to charge. IC4a is purely a buffer amplifier.

The square waveform is generated by a simple add-on to the triangular waveform generator described above. IC6a and IC6b are analogue switches. The analogue inputs are connected to the high and low limits, and the logic inputs (pins 12, 13) are connected to the Q and $\overline{Q}$ outputs of IC2a. Hence while C4 is charging, the output 'C' is connected to the high limit, and while C4 is discharging, the output 'C' is connected to the low limit. See Figure 3 for waveforms.

Construction

This is straightforward. Refer to Figure 4 for the pcb layout and legend. Some care should be taken to avoid static charges when handling the CMOS IC's. Try to fit these last if possible, and always fit them after the power supply smoothing capacitors (C5 and C6) have been installed. Solder the power rail pins first (pins 7 and 14). Otherwise solder at will! A good plan is to do resistors first, then capacitors then the three wire links, using cut off resistor leads, and lastly the IC's. It is not necessary to connect all the 4 outputs. These can be connected in parallel if extra power is needed. When connecting the output sockets make sure that the correct wire goes to each pin. Also take care when testing different servos. There are some manufacturers who use the same sockets but different pin conventions.

Figure 5 shows box cut-out details. Mount the completed board into the box using M3 fixings as shown in Figure 6. Cut the shaft of RV3 to approximately 12mm, and fit a knob. The tang of S1 should also protrude through the slot cut in the side of the box. Fit the lid with the power wires and output connections protruding through the notches. To finish, stick on the front panel.

Set-up and Testing

The Servo Tester was designed to be powered by a 4.8V standard radio control battery pack. Alternatively, a 5V 1A power supply could be used.

Start by positioning all the potentiometers in their mid-positions, and setting the selector switch S1 to manual. Connect the battery/power supply. If an oscilloscope is available, the frame can be set to 20ms by adjusting RV1. This is not critical. Some radio control systems have a variable frame. Here the frame is set by the sum of the pulse widths of all the channels plus the 'sync' pulse, which is usually about 8ms long. Hence on a seven channel system the frame can vary from 15ms to 22ms.

Next set the high and low limits (RV2 and RV4). A good starting point is to adjust these so that the ends of RV3a are at 1.8V and 2.8V. Final setting can then be performed using an oscilloscope or by using a servo on which the output arm movement range has been noted from its use on another radio control system. Adjust RV2 to give 2ms with RV3 fully clockwise and RV4 to give 1ms with RV3 fully anticlockwise. There is some interaction between these settings so it will be necessary to alternately adjust RV2 and RV4 several times.

Now connect a servo (if you have not done so already). Movement of RV3 should give a corresponding movement in the servo. Set S1 to triangular wave. The servo arm should now be moving from one extreme to the other at a rate determined by RV3. With RV3 in the fully anticlockwise position, adjust RV5 to give the slowest desired transit time. A time of about 50 seconds is recommended.

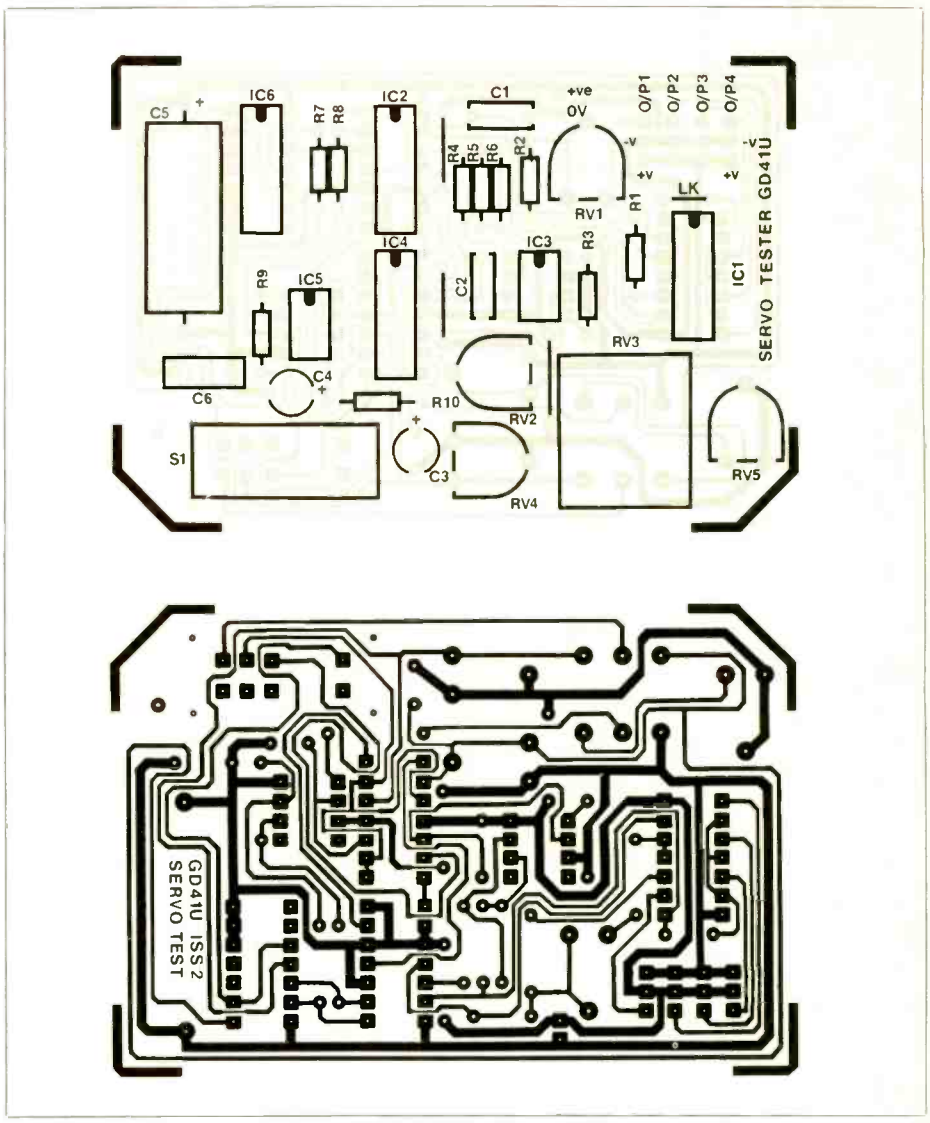


Figure 4. Pcb layout and circuit references.

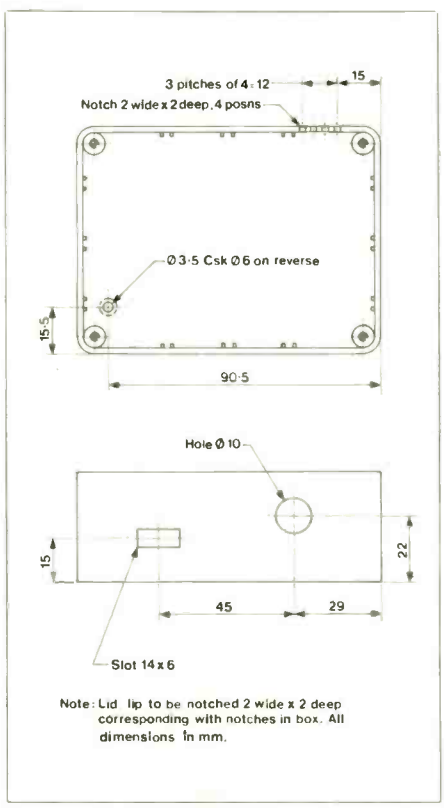


Figure 5. Box drilling.

Use of the Servo Tester

1. Servo Travel

Use the manual control to set the servo from one extreme to the other. Then with a protractor measure the servo travel. Typical values are 70° - 90° for regular servos or 180° for 'retract' servos.

2. Servo Resolution (or Sensitivity)

Set the selector switch (S1) to the mid-position (triangular wave) and set

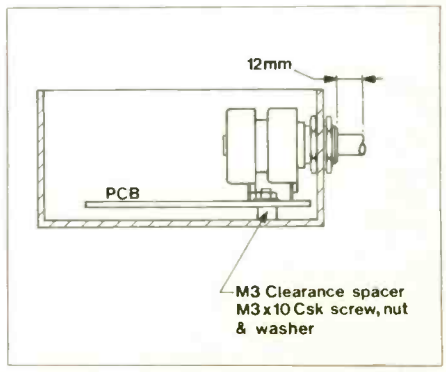


Figure 6. Mounting pcb in box.

RV3 fully anticlockwise. As the pulse slowly changes the servo will respond in small jumps. The servo travel divided by the number of jumps will give the resolution (typically 0.5°). If the slowest transit time has been set to 50 seconds it will only be necessary to count the jumps over 10 seconds and multiply by 5. This test is also useful for showing up any problems with the servo feedback potentiometer.

3. Servo Transit Time

Start with S1 in the squarewave position and RV3 fully anticlockwise. The servo will now switch from one extreme to the other every 50 seconds. Slowly turn RV3 clockwise while listening carefully for the gaps in the servo movements. When these disappear the servo is moving at its maximum speed. Measure the time for 20 swings and divide by 20 to get the transit time, (typically 0.3 to 0.5 seconds). This can be divided by the servo travel to give the servo speed in terms of seconds per degree.

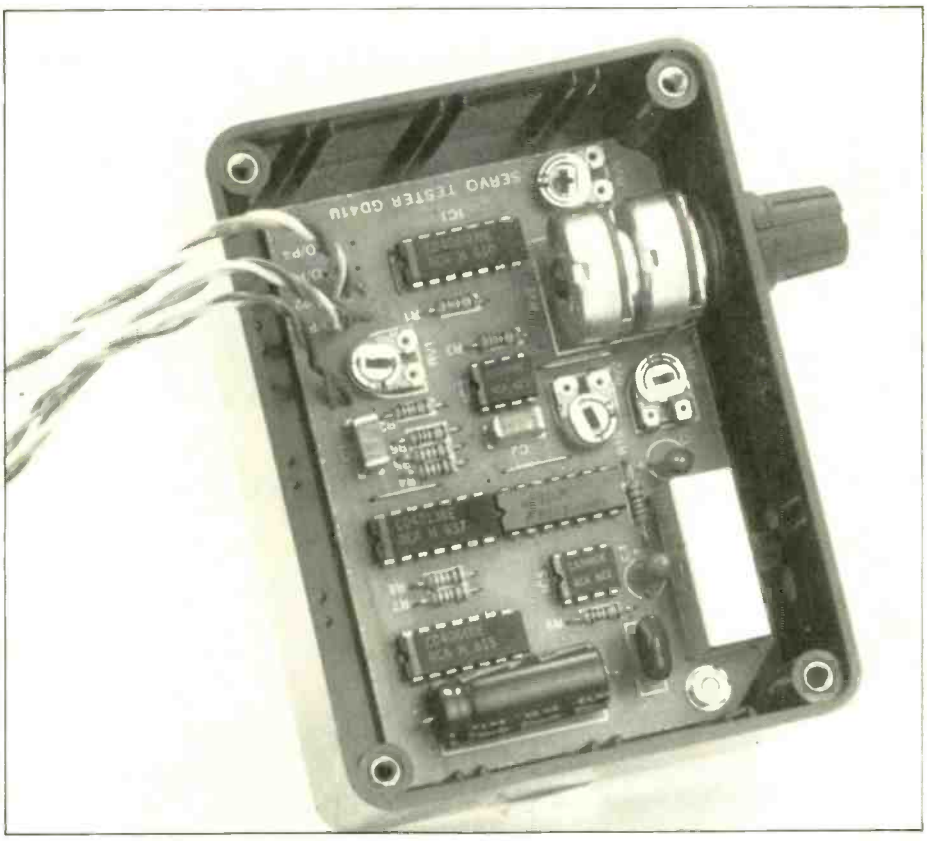
4. Overshoot

With S1 in the squarewave position and RV3 set to get the servo to move full travel about once per second, use a protractor above the servo arm to measure the overshoot, (typical values 0 - 5°).

5. Compare Two Servos

Plug both servos into the tester and run through all the tests. The advantage of doing two at once is that one can get a feel for their differences.

One last thought. Before descending on your local model shop to test his servos, make absolutely certain that your tester is working correctly on each of the outputs, and, of course, that the pin conventions that you have used on your sockets correspond to the pin conventions of the servos being tested.



SERVO TESTER PARTS LIST

RESISTORS: All 0·6W 1% Metal Film (Unless specified)			
R1	56k	1	(M56K)
R2	220k	1	(M220K)
R3	47k	1	(M47K)
R4,5,7,8,10	22k	5	(M22K)
R6,9	10k	2	(M10K)
RV1	47k Hor Encl Preset	1	(UH05F)
RV2	22k Hor Encl Preset	1	(UH04E)
RV3	4k7 Dual Pot Lin	1	(FW84F)
RV4	10k Hor Encl Preset	1	(UH03D)
RV5	1k Hor Encl Preset	1	(UH00A)
CAPACITORS			
C1	100nF Poly Layer	1	(WW41U)
C2	68nF Poly Layer	1	(WW39N)
C3,4	33µF 10V Tant	2	(WW74R)
C5	1000µF 10V Axial	1	(FB81C)
C6	100nF Mylar	1	(WW21X)
SEMICONDUCTORS			
IC1	4069UBE	1	(QX25C)
IC2	4013BE	1	(QX07H)
IC3,5	CA3080E	2	(YH58N)
IC4	LM324	1	(UF26D)
IC6	4066BE	1	(QX23A)
MISCELLANEOUS			
S1	R/A DT3T Slide	1	(FV02C)
	PCB	1	(GD41U)
	Knob K14 A	1	(FK38R)
	ABS Box MB2	1	(LH21X)
	Spacer M3 × ⅛ in.	1 Pkt	(FG32K)
	Pozi Screw M3 × 10m	1 Pkt	(LR57M)
	Isowasher M3	1 Pkt	(BF62S)
	Isonut M3	1 Pkt	(BF58N)
	Wire 7/0·2 10m Black	1 Pkt	(BL00A)
	Wire 7/0·2 10m Red	1 Pkt	(BL07H)
	Wire 7/0·2 10m White	1 Pkt	(BL09K)
	Front Panel	1	(FP75S)
	Instruction Leaflet	1	(XT78K)
	Constructors' Guide	1	(XH79L)

The above items are available as a kit:
Order As LM23A (Servo Tester Kit).
The following items (which are included in the kit) are also available separately.
PCB **Order As GD41U.**
Front Panel **Order As FP75S.**

Weather Satellite Down Converter

by Robert Kirsch Part 2

This is the second article describing a Down Converter for use with the MAPSAT VHF Receiver and Decoder. The previous article covered the Meteosat System with a technical description of the Down Converter and Pre-amplifier, as well as the requirements necessary for the sighting of the aerial system. This article describes the installation and testing of the complete system and also the circuit description and construction details for the Channel Switching Unit.

Aerial and Pre-amplifier

The aerial kit (LM22Y) is supplied with all metalwork pre-drilled and cut to length, all necessary screws, nuts and washers are also included together with full assembly instructions. The ready-built and pre-aligned Pre-amplifier is also included with this kit. **Note:** This kit does not include a mast or lashings, and something suitable should be chosen for your particular installation, bearing in mind the sighting requirements described in the previous article. The system should, if possible, be tested at ground level before the aerial is installed in its final position, see 'Pre-Installation Tests' below.

Down Converter

This unit is ready-built and aligned and requires no action at this stage other than roughly determining its final position in order to find the approximate length of feeder that will be used, as this is required during testing.

Channel Switching Unit

This unit is required in order to change the channel being received by the Down Converter. The unit is connected in series with the aerial cable that exits from the Down Converter, and then connects to the aerial socket of the Mapsat Receiver.

When the Receiver and Down Converter are first powered up, channel 1 is automatically selected. Channel 2 is selected by operating the toggle switch located on the front panel of the control unit in the appropriate direction. This causes a short break in the power supply which is detected by the channel switching logic in the Down Converter, and switches the channel 2 crystal into circuit. The toggle switch, when moved to the channel 1 position, causes a longer break in the supply to the Down Converter and the switching logic will now select the channel 1 crystal.

Channel Switching Unit.

Circuit Description

Figure 1 shows the circuit of the Channel Switching Unit. Figure 5 of the Down Converter article includes the channel switching logic and crystal oscillator circuits.

The radio frequency signals from the Down Converter enter the unit via SK1 and are directly coupled to the Receiver via C6 and SK2. The supply from the Receiver (positive on the coax centre conductor and negative on the screen) is separated from the RF signals by L2 which provides a high impedance to the signals at 137.5MHz, but has a low resistance to DC. This supply is connected via the contacts of RL1, L1 and SK1 to the Down Converter.

When the toggle switch is moved to channel 2 position, the input of the inverter IC1e is pulled high, the output goes low and the pulse caused by C8 charging is inverted by IC1f, turns on TR3 and operates RL1 for a short period. The contacts of RL1 are normally made and thus this pulse causes a short break in the supply to the Down Converter. When the switch is moved to the channel 1 position the same sequence of events occur but in this case the pulse length is determined by C7, this being a higher capacity, the pulse is longer and the supply is interrupted for a greater period of time.

The circuit formed by IC1a, b and c is used to mimic the channel switching logic in the Down Converter in order to drive the LEDs that show which channel has been selected. The input to this circuit is via D1 and C3, which are connected to the switched side of the unit. When a short duration interruption occurs C3 produces a short positive going pulse at the point when the power is restored, this causes the latch formed by IC1a and c to change state. During this process, C1 has remained charged and the output of the inverter IC1b remains low and has no effect on the latch. When

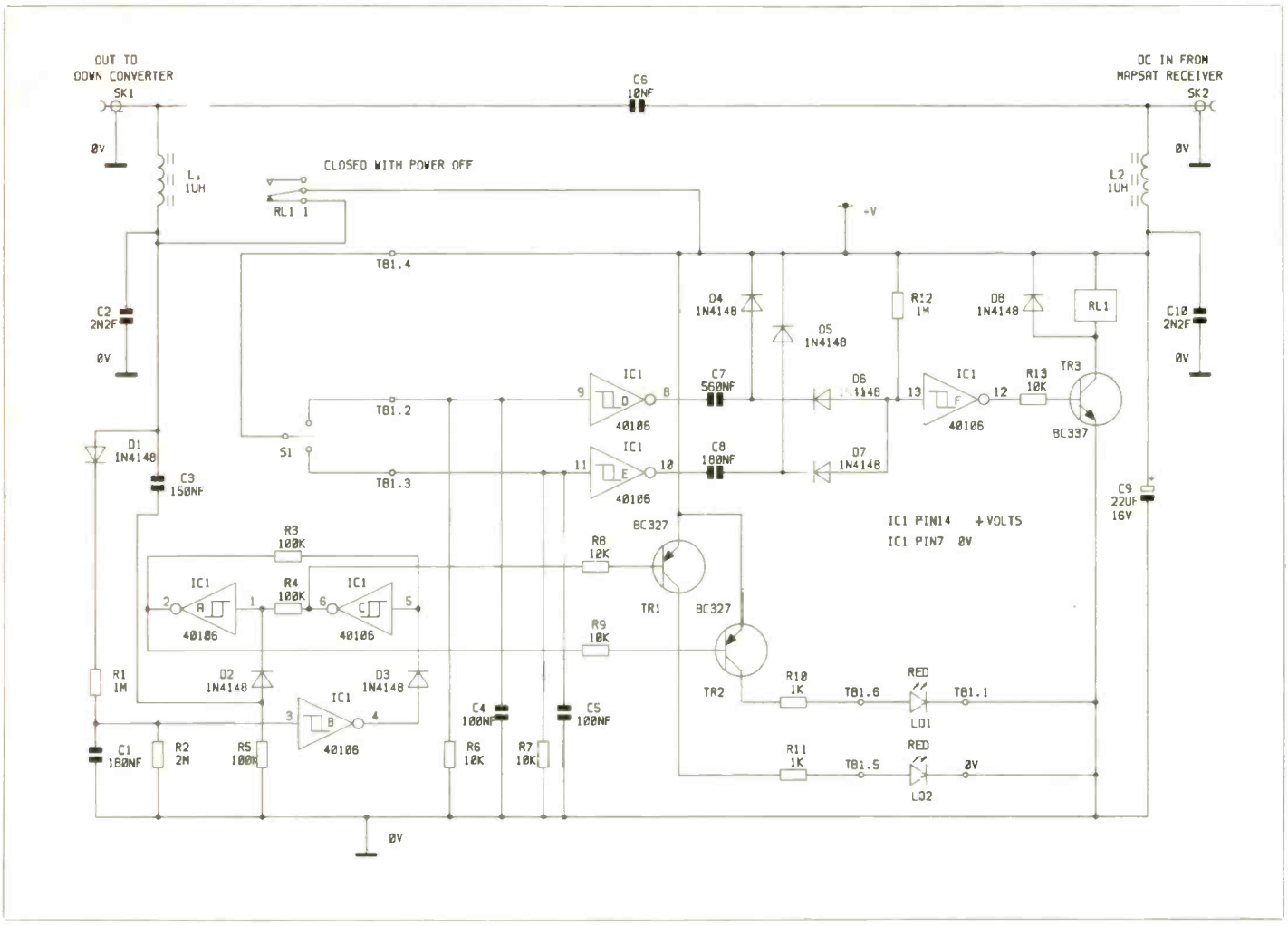


Figure 1. Channel Switching unit ci. cuit.

the longer duration channel 1 pulse occurs (generated at initial switch on), the same sequence occurs but this time C1 has discharged. The pulse from C3 still tries to switch the latch it has held in the opposite state by the output of IC1a being high due to the slow charging time of C1 via R1. The two indicator LEDs are driven by TR1 and TR2 from the appropriate latch outputs.

The channel switching logic in the Down Converter works in the same way, but in this case as the whole power supply is interrupted, it is necessary to maintain the power to IC2 (Part 1, Figure 5) during the switching period. This is accomplished by C18 which is charged via D4. The short duration pulse is produced by C19, and C17 determines the long charge time. In this case the output from the latch is used to bias either D6 and D8 or D9 and D7 on, thus grounding either XT1 or XT2 in the crystal oscillator circuit.

Construction

Referring to the Parts List and the circuit board layout shown in Figure 2, insert and solder all components. **Note:** The two chokes, L1 and L2, are only soldered to the board at *one end* as the other ends connect to the *centre terminal* of the input and output sockets. C6 is not mounted on the circuit board, but is connected directly between the centre

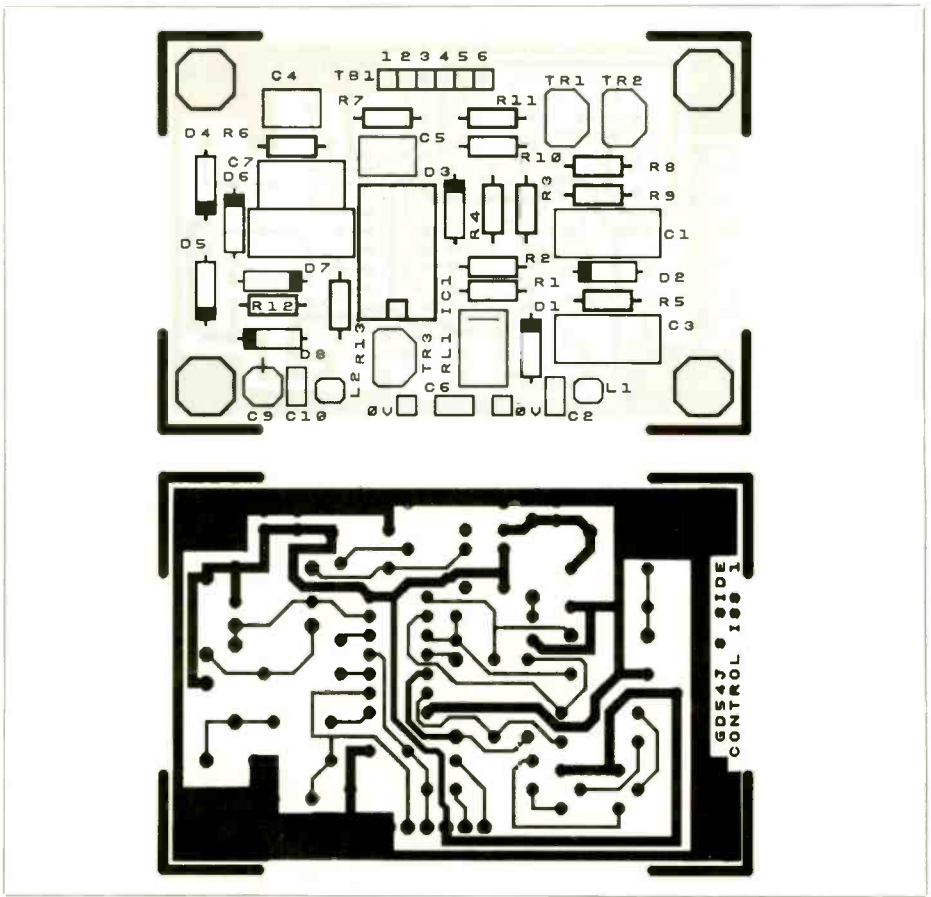


Figure 2. Channel Switching board track and layout.

terminals of the sockets. Drill the die-cast box as shown in Figure 3, and fit the stick-on front panel. Mount the two LEDs and the toggle switch to the lid of the box and terminate about 10cm of ribbon cable to them whilst following the wiring diagram in Figure 4. Terminate the other end of the ribbon cable in the IDC connector, ensuring that the wires are in the correct order. Each wire should be carefully laid in its groove and then firmly pressed into position using an IDC insertion tool.

Fit the two coax sockets to the box with the solder tags on the inside using the screws, spacers, lock washers and nuts provided, and terminate L1 and L2 to the centre pins of the sockets. Connect a short length of tinned copper wire to each of the Veropins on the lower edge of the board, and solder the other end of these to the solder tags on the sockets. The IDC connector may now be plugged onto the circuit board and the lid secured with the four countersunk screws provided. The control unit is now ready for testing.

Modifications to the MAPSAT Receiver

The Mapsat Receiver requires a minor modification in order to supply the extra power required of it by the Down Converter and Pre-amplifier. Remove the top cover from the Receiver to gain access to the circuit board. Locate the resistor R1 near the aerial input coil, and carefully solder a short length of tinned copper wire across this resistor, being careful *not* to make contact with the earth plane surrounding the resistor pads!

Pre-Installation Tests

For these tests the assembled aerial should be attached to a temporary mast in a position that will enable adjustments to be carried out on the pre-amplifier. The aerial should be pointed at un-obstructed sky in the direction of the satellite, see previous article. Connect the F type plug on the end of the cable attached to the Pre-amplifier to the appropriate socket on the Down Converter (SK1). After determining the approximate length of the down lead, prepare this length of cable with coax plugs at each end. Connect this lead to the remaining socket on the Down converter and to the right-hand socket of the Channel Switching Unit. Make up the short coax lead that connects the Channel Switching Unit to the MAPSAT Receiver, using two coax plugs (shown as optional in the Channel Switching Unit parts list). Connect the Receiver to the left-hand socket of the Switching Unit. The MAPSAT Receiver may be powered from batteries for these tests, if it is more convenient than using a mains operated power supply. For these tests the Receiver should be located near the aerial system so that the effect of adjustments can be observed.

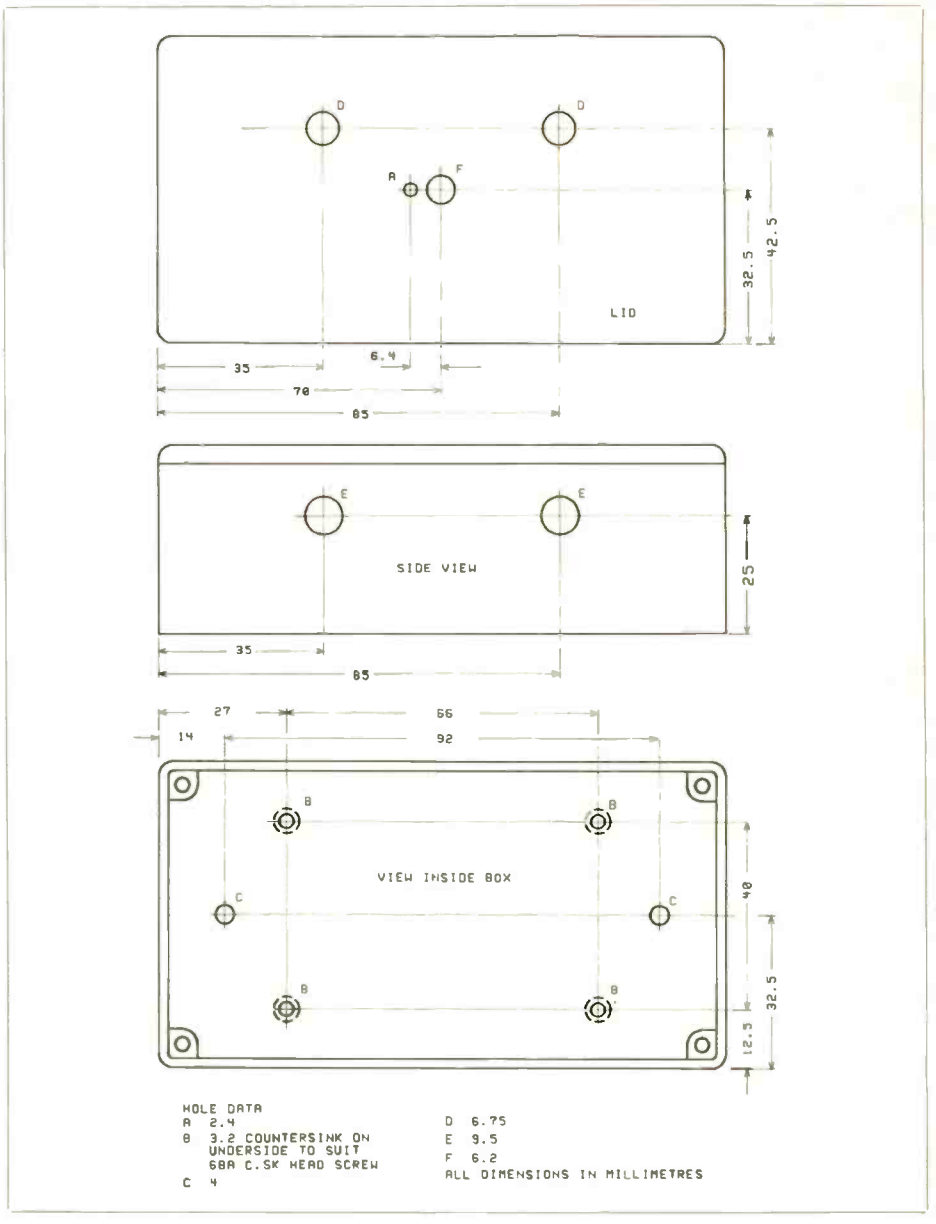
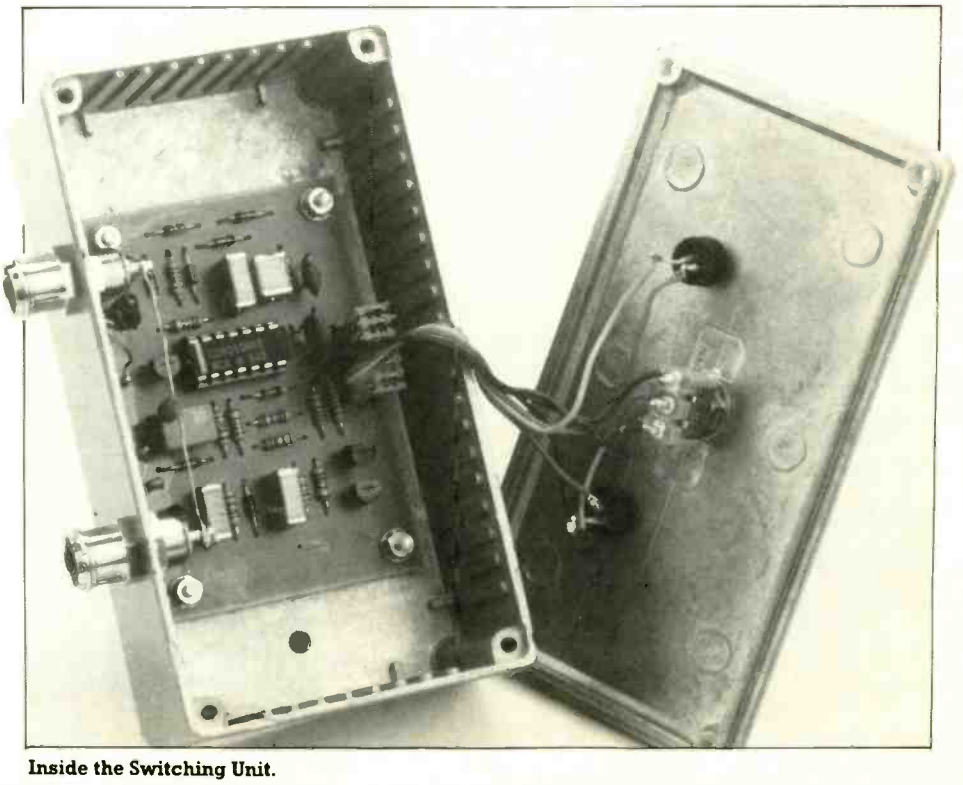


Figure 3. Case drilling.



Inside the Switching Unit.

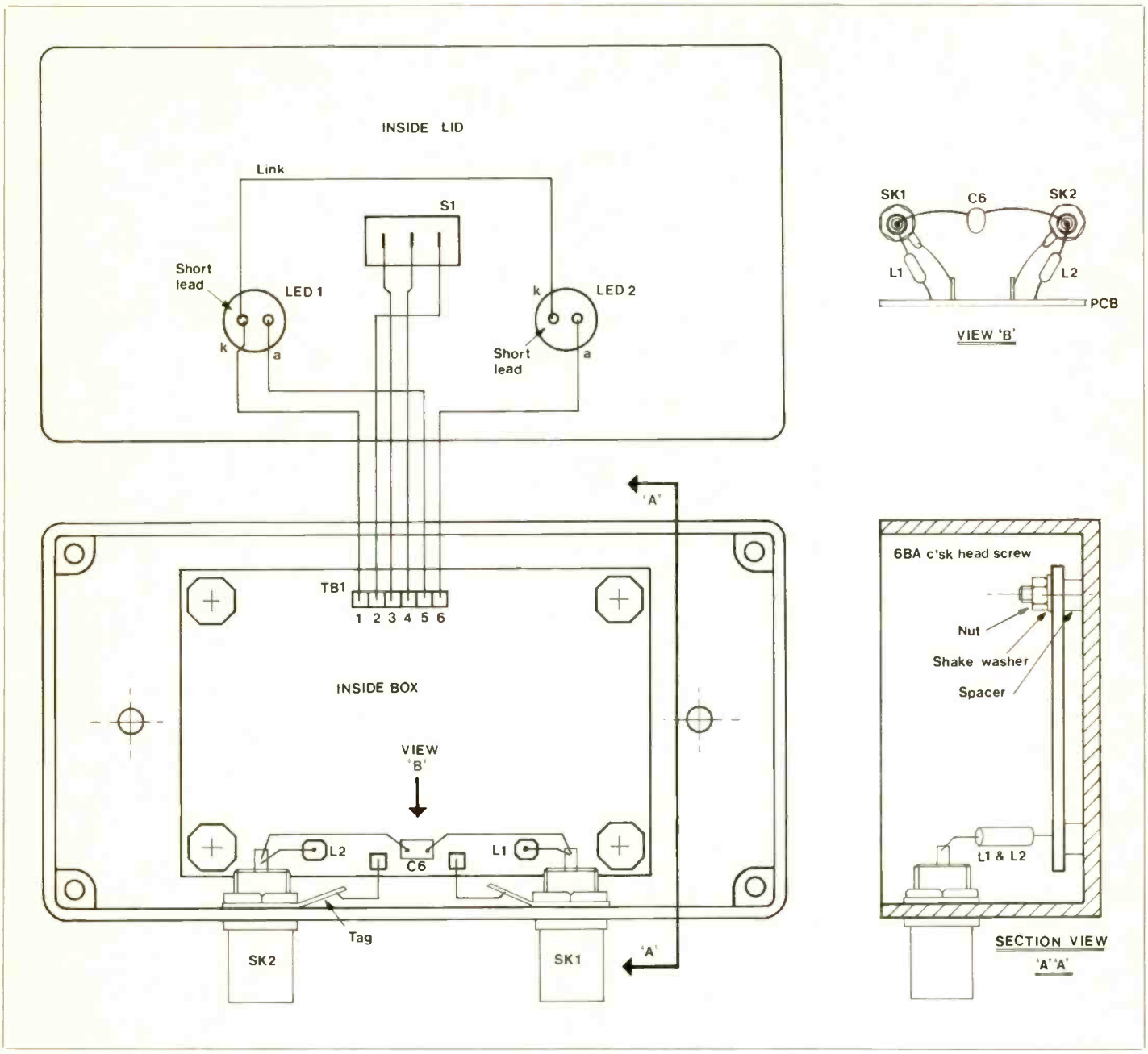


Figure 4. Wiring and assembly.

Switch on the power to the Receiver and check that the channel 1 LED on the Switching Unit is illuminated. Move the toggle switch to the channel 2 position and check that the channel 2 LED is now illuminated, and that the channel 1 LED goes out. **Note:** The toggle switch is centre-biased and must be held in the required position for a short time until the switching sequence is complete. (No more than 2 seconds.) Repeat the test in the opposite direction and check that the LED's return to their starting condition.

Signals are transmitted by Meteosat 2 on channel 1 most of the time, but, it is advisable to check the Prediction Chart (Table 1) to ensure that signals are available. Set the volume control to a convenient level and tune the receiver until signals from the satellite are heard. (Approximately 5 on the tuning dial; 137.5MHz). The position of the aerial should be adjusted for maximum signal strength. *Very carefully* adjust the screw

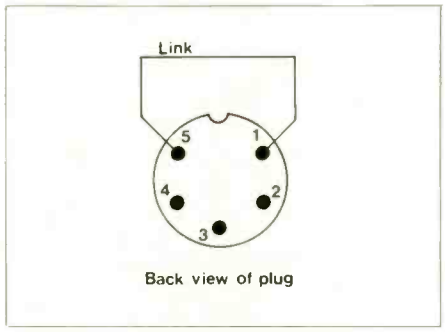


Figure 5. Receiver by-pass plug.

type trimmer on the Pre-amplifier for maximum signal strength. This trimmer is located towards the front of the Pre-amplifier and is accessible through a small hole in the case. After this adjustment has been completed, the hole should be sealed with silicon rubber to prevent the ingress of water.

Assuming that a reasonably strong noise free signal is obtained, the unit is now ready for installation in its permanent position.

Using the System

Signals from orbiting weather satellites are usually recorded before being decoded and displayed, as they are only receivable for short periods during the day. The majority of pictures transmitted by Meteosat 2 on channel 1 are updated every hour, so it is often unnecessary to record them, as they may be displayed as they are received. To operate the MAPSAT system without a tape recorder connected, a by-pass plug must be inserted in the socket at the rear of the Receiver in place of the recorder, see Figure 5. The audio level out of the Receiver may be found to be too low to operate the Decoder in this mode; if this is the case, resistor R57 on the Receiver board may be reduced in value or shorted out altogether. All pictures

METEOSAT DISSEMINATION SCHEDULE

Hrs Mins	00 UT CH1	00 UT CH2	03 UT CH1	03 UT CH2	06 UT CH1	06 UT CH2	09 UT CH1	09 UT CH2	12 UT CH1	12 UT CH2	15 UT CH1	15 UT CH2	18 UT CH1	18 UT CH2	21 UT CH1	21 UT CH2	Hrs Mins
2	E3 47				E3 11	WEFA 2			E3 22	— —		WEFA 4	E3 34				2
6						— —				— —		— —					6
10	D2 48	BIW 48	D2 6	BIW 6	D2 12	BIVW 12	B2 18	BIVW 18	D2 24	BIVW 24	D2 30	BIVW 30	D2 36	BIVW 36	D2 42	BIW 42	10
14	D1 48		D1 6		C02 12	DTOT 12	C02 18		C02 24	DTOT 24	C02 30		D1 36	DTOT 36	D1 42		14
18	D3 48	AI 48	D3 6	AI 6	C03 12	AIVH 12	C03 18	AIVH 18	C03 24	AIVH 24	C03 30	AIVH 30	D3 36	AI 36	D3 42	AI 42	18
22	D4 48	— —	D4 6	— —	D1 12	— —	D1 18	— —	D1 24	— —	D1 30	— —	D4 36	— —	D4 42	— —	22
26	D5 48	LY 48	D5 6	DTOT 6	D3 12	— —	D3 18	— —	D3 24	— —	D3 30	— —	D5 36	LY 36	D5 42	DTOT 42	26
30	D6 48	LR 48	D6 6		D4 12	LY 12	D4 18	DTOT 18	D4 24	LY 24	D4 30	DTOT 30	D6 36	LR 36	D6 42		30
34	D7 48	DTOT 48	D7 6		D5 12	LR 12	D5 18	CTOT 18	D5 24	LR 24	D5 30	ETOT 30	D7 36	WEFA 5	D7 42		34
38	D8 48		D8 6		D6 12	ETOT 12	D6 18	ETOT 18	D6 24	CTOT 24	D6 30		D8 36	— —	D8 42		38
42	D2 1	BIW 1	D2 7	BIW 7	D2 13	BIV 13	D2 19	BIV 19	D2 25	BIV 25	D2 31	BIV 31	D2 37	BIVW 37	D2 43	BIW 43	42
46	D9 1	LX 48	D9 7		C02 13	LX 12	C02 19		C02 25	LX 24	C02 31		D9 37	LX 36	D9 43		46
50	D1 1	— —	D1 7	AI 7	C03 13	— —	C03 19		C03 25	— —	C03 31		D1 37	— —	D1 43	AI 43	50
54	D3 1	AI 1	D3 7	— —	C3D 13	AI 13	C1D 19	AI 19	C1D 25	AI 25	C1D 31	AI 31	D3 37	AI 37	D3 43	— —	54
58		— —			C2D 13	— —	C2D 19	- —	C2D 25	— —	C2D 31	— —		— —			58

Hrs Mins	01 UT CH1	01 UT CH2	04 UT CH1	04 UT CH2	07 UT CH1	07 UT CH2	10 UT CH1	10 UT CH2	13 UT CH1	13 UT CH2	16 UT CH1	16 UT CH2	19 UT CH1	19 UT CH2	22 UT CH1	22 UT CH2	Hrs Mins
2							C3D 19		C3D 25	ETOT 24	C3D 31						2
6							C4D 19		C4D 25	L2 24	C4D 31						6
10	D2 2	BIW 2	D2 8	BIW 8	D2 14	BIVW 14	D2 20	BIVW 20	D2 26	BIVW 26	D2 32	BIVW 32	D2 38	BIVW 38	D2 44	BIW 44	10
14	D1 2		D1 8		C02 14		C02 20		C02 26	DTOT 26	C02 32		D1 38		D1 44		14
18	D3 2	AI 2	D3 8	AI 8	C03 14	AIVH 14	C03 20	AIVH 20	C03 26	AIVH 26	C03 32	AIVH 32	D3 38	AI 38	D3 44	AI 44	18
22		— —	E1 8	— —	C5D 14	— —	C5D 20	— —	C5D 26	— —	C5D 32	— —	E1 38	— —		— —	22
26		AW 2	E2 8	AW 8	C6D 14	— —	C6D 20	— —	C6D 26	— —	C6D 32	— —	E2 38	AW 37		AW 44	26
30		— —	E3 8	— —	D7 14		D7 20		D7 26		D7 32	AW 32	E3 38	— —		— —	30
34			E4 8		D8 14		D8 20		D8 26	C8D 26	D8 32	— —	E4 38				34
38			E5 8		D9 14		D9 20		D9 26	C9D 26	D9 32		E5 38				38
42	D2 3	BIW 3	D2 9	BIW 9	D2 15	BIV 15	D2 21	BIV 21	D2 27	BIV 27	D2 33	BIV 33	D2 39	BIVW 39	D2 45	BIW 45	42
46	D1 3		D1 9		C02 15		C02 21		C02 27	AW 27	C02 33		D1 39		D1 45		46
50	D3 3	AI 3	D3 9	AI 9	C03 15	AI 15	C03 21		C03 27	— —	C03 33	AI 33	D3 39	AI 39	D3 45	AI 45	50
54		— —	E6 9	— —	C8D 15	— —	C7D 21	AI 21	C7D 27	AI 27	C7D 33	— —	E6 39	— —		— —	54
58		WEFA 1	E7 9		C9D 15		C8D 21	— —	C8D 27	— —	C8D 33		E7 39				58

Hrs Mins	02 UT CH1	02 UT CH2	05 UT CH1	05 UT CH2	08 UT CH1	08 UT CH2	11 UT CH1	11 UT CH2	14 UT CH1	14 UT CH2	17 UT CH1	17 UT CH2	20 UT CH1	20 UT CH2	23 UT CH1	23 UT CH2	Hrs Mins
2		— —	E8 9			WEFA 3	C9D 21		C9D 27		C9D 33		E8 39				2
6			E9 9			— —							E9 39				6
10	D2 4	BIW 4	D2 10	BIW 10	D2 16	BIVW 16	D2 22	BIVW 22	D2 28	BIVW 28	D2 34	BIVW 34	D2 40	BIW 40	D2 46	BIW 46	10
14	D1 4	TEST 4	D1 10	ADMN 0	C02 16	TEST 0	C02 22	ADMN 0	C02 28	TEST 4	C02 34	ADMN 0	D1 40	TEST 0	D1 46	ADMN 0	14
18	D3 4	AI 4	D3 10	AI 10	C03 16	AIVH 16	C03 22	AIVH 22	C03 28	AIVH 28	C03 34	AIVH 34	D3 40	AI 40	D3 46	AI 46	18
22	TEST 0	— —	ADMN 0	— —	TEST 4	— —	ADMN 0	— —	TEST 0	— —	ADMN 0	— —	TEST 4	— —	ADMN 0	— —	22
26						— —		— —		— —		— —		WEFA 6			26
30														— —			30
34	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	34
38	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	38
42	D2 5	BIW 5	D2 11	BIW 11	D2 17	BIV 17	D2 23	BIV 23	D2 29	BIV 29	D2 35	BIV 35	D2 41	BIW 41	D2 47	BIW 47	42
46	D1 5		D1 11		C02 17		C02 23	AV 23	C02 29		D1 35		D1 41		D1 47		46
50	D3 5	AI 5	D3 11	AI 11	C03 17	AI 17	C03 23	— —	C03 29	AI 29	D3 35	AI 35	D3 41	AI 41	D3 47	AI 47	50
54		— —	E1 11	— —	TEST 4	— —	E1 22	— —		— —	E1 34	— —		— —	E1 47	— —	54
58		CTH 0	E2 11		TEST 4	CTH 0	E2 22	— —		CTH 0	E2 34			CTH 0	E2 47		58

Table 1. Prediction Chart.

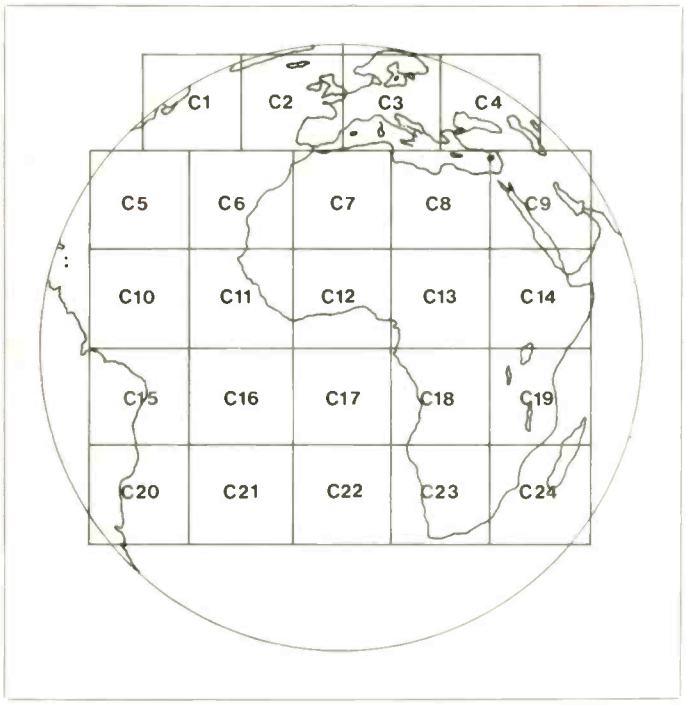


Figure 6. WEFAX visible formats.

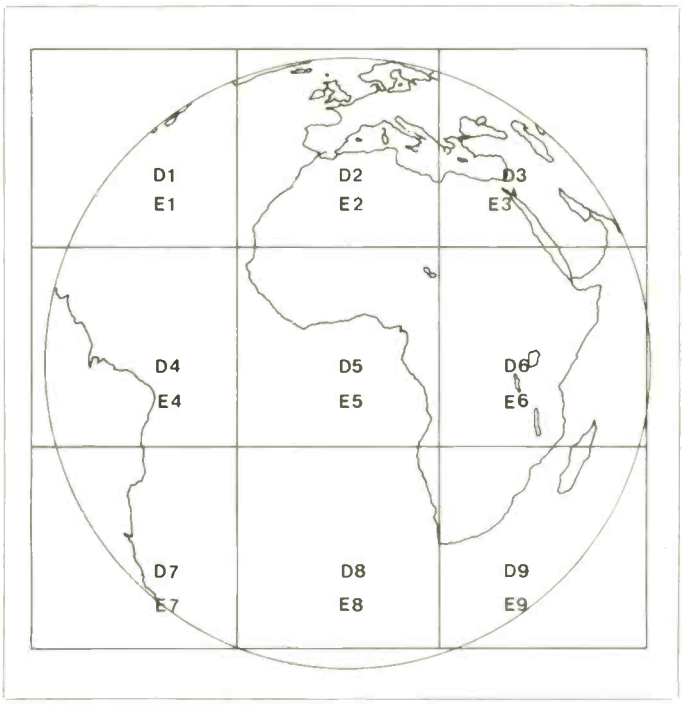


Figure 7. WEFAX IR (formats D) and WV (formats E).

transmitted by Meteosat are preceded by a 5 second burst of peak white signal, the Input Level control on the Decoder should be adjusted to give a full scale reading on the level meter during this tone.

Types of Pictures

Meteosat transmits the following three types of picture:

1. Visible (C format).
2. Infra-red (D format).
3. Water vapour (E format).

All pictures include date, time and format information and by using the maps shown in Figures 6 and 7, as well as Table 1, it is possible to identify the area of the Earth covered by the picture being received. Thus the visible image that covers the largest area of the British Isles is labelled C02. (An infra-red picture of the same area would be labelled C2D).

Channel 1 also transmits test pictures and administrative (ADMN) information. Channel 2 transmits pictures of the whole of Earth's disk (TOT) and also meteorological charts (WEFA).

Information about Meteosat and NOAA satellites may be obtained by calling UK Weatherwatch on 0256 83448, between 1715 and 0845, Monday to Friday or all day Saturday and Sunday.

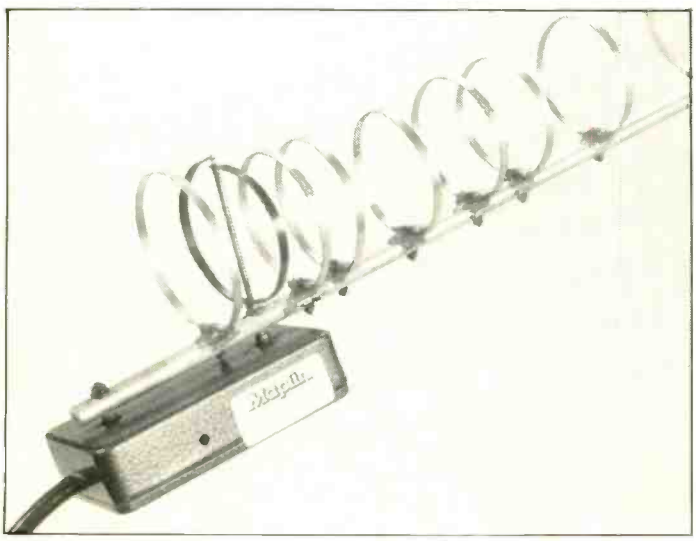
Final Installation

The aerial may be attached permanently to a standard television aerial lashing kit in a convenient position that enables the sighting requirements to be met, but bear in mind that for the final positioning it is best to adjust the aerial direction and angle whilst monitoring the signal strength on the Receiver.

The Down Converter may be mounted up to 4 metres from the aerial; this could enable it to be located inside a building but if this is not possible the unit should be installed in a weather-proof box (YM92A). Cable entry should be at the bottom of the box and any gaps around the cables sealed with silicon rubber (YJ91Y). Avoid locations where the Down Converter may get too hot and mount it in a shady position if possible.

The down lead from the Down Converter to the Receiver should be kept as short as possible to minimise signal losses, although the system has been found to work well with feeders of 15 metres and over. Avoid running the down lead close to sources of electrical interference such as computers, printers, disk drives or video monitors. Longer down leads may be used by inserting an inline 137.5MHz amplifier close to the Down Converter. This extra unit will also help where high levels of interference (at VHF) cannot be avoided. (Details next issue.)

As a matter of routine, a regular check should be made on all external units and the aerial elements should be cleaned from time to time, taking care not to damage the protective varnish applied during construction.



Aerial Pre-amplifier.

Down Converter mounted on a wall.

CHANNEL SWITCHING UNIT PARTS LIST

RESISTORS: All 0·6W 1% Metal Film			
R1,12	1M	2	(M1M)
R2	2M2	1	(M2M2)
R3,4,5	100k	3	(M100K)
R6-9,13	10k	5	(M10K)
R10,11	1k	2	(M1K)
CAPACITORS			
C1,8	180nF Poly Layer	2	(WW44X)
C2,10	2n2F Monores Cap	2	(RA40T)
C3	150nF Poly Layer	1	(WW43W)
C4,5	100nF 16V Minidisc	2	(YR75S)
C6	10nF 50V Disc	1	(BX00A)
C7	560nF Poly Layer	1	(WW50E)
C9	22μF 25V PC Elect	1	(FF06G)
SEMICONDUCTORS			
IC1	40106BE	1	(QW64U)
TR1,2	BC327	2	(QB66W)
TR3	BC337	1	(QB68Y)
D1-8	1N4148	8	(QL80B)
MISCELLANEOUS			
L1,2	Choke 1mH	2	(WH47B)
LED1,2	LED Red	2	(WL27E)
SK1	HQ Co-ax Socket	2	(FE10L)
RL1	Micro-Min Relay 12V	1	(BK47B)
S1	Sub-Min Toggle D	1	(FH03D)
TB1	PCB Latch Pl 6-way	1	(YW12N)
	PCB Latch Hsng 6-way	1	(BH65V)
	PCB Terminal	1 Pkt	(YW25C)
	LED Clip 5mm	2	(YY40T)
	Box DCM5004	1	(LH71N)
	PCB	1	(GD54J)
	Front Panel	1	(FP76H)
	C/S Screw 6BA × ½ in.	1 Pkt	(BF12N)
	Shakeproof 6BA	1 Pkt	(BF26D)
	Nut 6BA	1 Pkt	(BF18U)
	Spacer 6BA × ⅛ in.	1 Pkt	(FW33L)
	Ribbon Cable 10-way	1m	(XR06G)
	Pin 2145	1 Pkt	(FL24B)
	Instruction Leaflet	1	(XT79L)
	Constructors' Guide	1	(XH79L)
OPTIONAL (Not in Kit)			
	HQ Coax Plug	2	(FD85G)
	Low-Loss Coax White	As Req	(XR87U)

The above items (excluding Optional) are available as a kit:
Order As LM26D (Channel Switch Unit).
The following item (which is included in the kit) is also available separately.
PCB **Order As GD54J.**

Bob's MINI-CIRCUITS

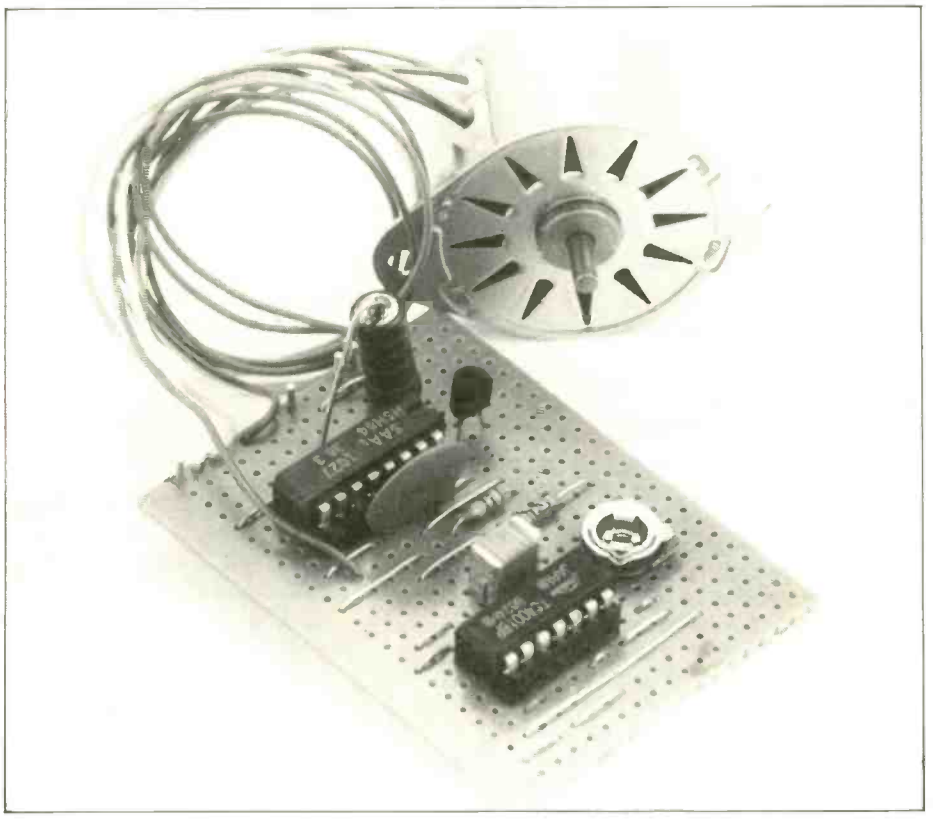
by Robert Penfold

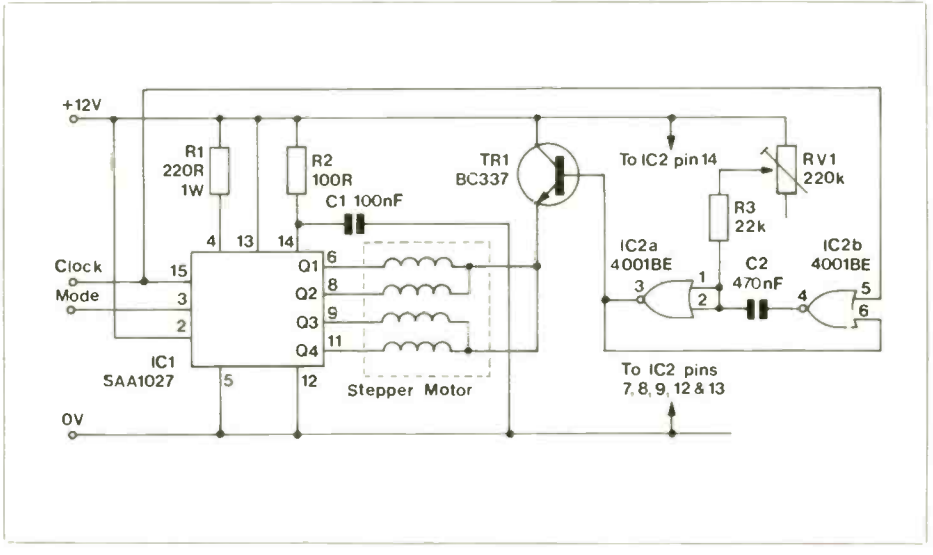
Stepper Motor Driver

The Mullard SAA1027 seems to have become the standard stepper motor driver device for home constructor designs, and it certainly offers good performance at relatively low cost. It is a fairly basic driver though, and it has the shortcoming of continuously driving the stepper motor with power even when it is not being stepped from one position to the next (for the uninitiated, with stepper motors it is the switching of power between its coils and not simply the application of power that operates the device). The continuous application of power is not likely to cause any damage to either the motor or the driver circuit, but it will often result in the motor running quite warm, and in an application where battery power is used it represents a terrific waste of the battery's capacity.

It is not difficult to incorporate some form of power economy circuit, and there are several possible approaches to the problem. The one used in the circuit shown here probably represents the best method as it does not require the use of any additional control lines from the computer or other controlling circuit, and it is totally 'invisible' to the user. It nevertheless cuts down the current consumption of the circuit to something very close to the minimum that can be achieved.

IC1 is the stepper motor driver, and this is really just the standard SAA1027 configuration. Pulses applied to the 'CLOCK' input step the motor, and the logic level applied to the 'MODE' input controls the direction of rotation. Although pin 2 is shown as connecting to positive supply rail, this can be used as a reset input if required, and it sets the outputs to their reset states (Q1 and Q3 low, Q2 and Q4 high) when it is taken to the low state. Note that the input signals must be between 7.5V and V+ for a 'high', and 0V to 4.5V for a 'low'. A simple level shifting circuit is therefore needed for control by ordinary 5 volt logic levels.





Stepper Motor Driver Circuit.

The current economy is obtained by having the 'common' terminals of the motor normally left open circuit, and only briefly connecting them to the positive supply rail when a clock pulse is received and IC1's outputs change state. This is achieved by having IC2 operate as a simple monostable multivibrator which is triggered by the clock pulses. Its output pulses activate TR1 which connects power through to the 'common' terminals of the motor. RV1 controls the monostable's output pulse duration, and this should be set for the minimum value which gives reliable operation of the circuit. Apart from minimising current consumption, this ensures that the monostable can provide output pulses at a rate which can match the stepping speed of the clock signal and the motor. The optimum pulse duration depends on the particular motor used, but the adjustment range of RV1 is sufficient to accommodate any normal type.

The reduction in static current consumption is likely to be quite large, but it is obviously dependent on the coil resistance of the motor concerned (which should have a resistance of about 75Ω or more through each coil). On test with a Maplin stepper motor (type No. 1) the prototype had a quiescent current consumption of just over 50 milliamps, which compares with about five to six times this figure without the power economy circuit. Of course, the amount of power saved in use depends on how often or otherwise the motor is stepped, but the saving will normally be quite substantial.

Only two gates of IC2 are utilised in this circuit, and the only connections to the other two are to tie their inputs to ground to protect them against static charges. Note that in the monostable configuration the 4011BE is not a suitable substitute for the 4001BE.

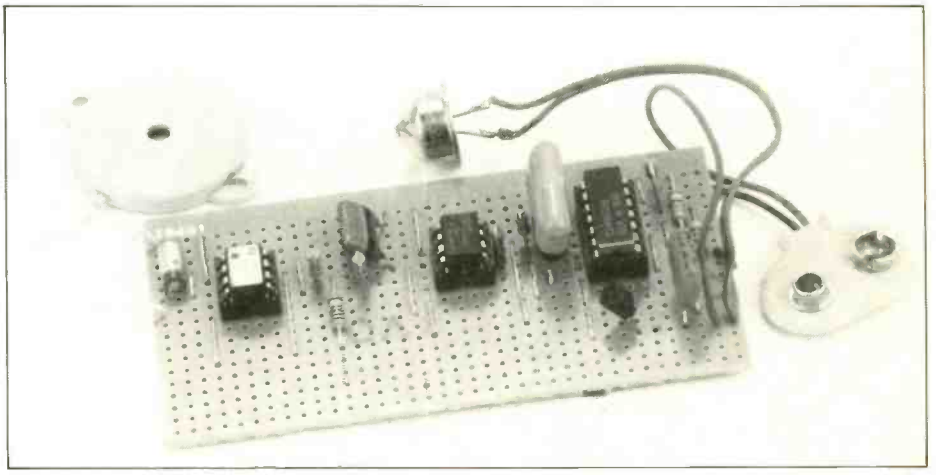
STEPPER MOTOR DRIVER PARTS LIST

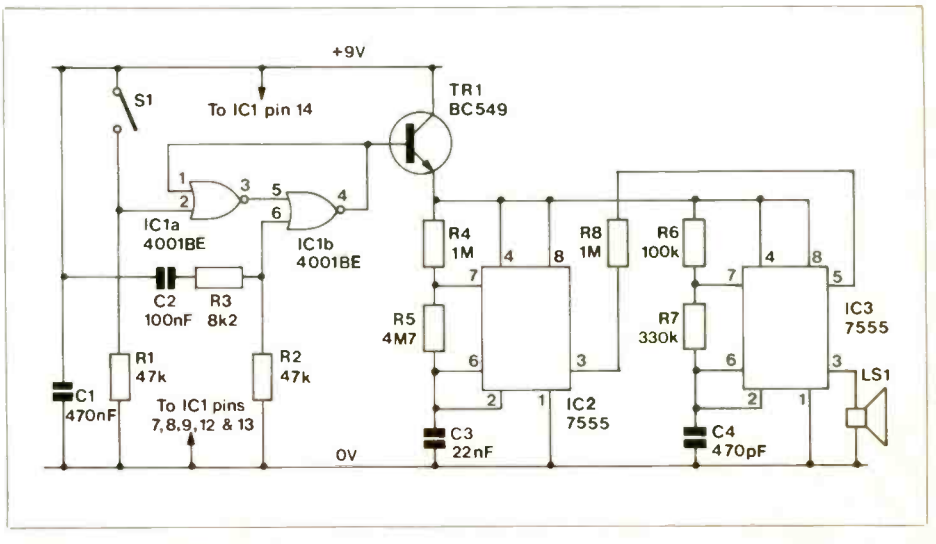
RESISTORS: All 0·6W 1% Metal Film (Unless specified)			
R1	220Ω 1W Res	1	(C220R)
R2	100Ω	1	(M100R)
R3	22k	1	(M22K)
RV1	220k Hor Encl Preset	1	(UH04E)
CAPACITORS			
C1	100nF Ceramic	1	(YR75S)
C2	470nF Poly Layer	1	(WW49D)
SEMICONDUCTORS			
IC1	SAA1027	1	(QY76H)
IC2	4001BE	1	(QX01B)
TR1	BC337	1	(QB68Y)
MISCELLANEOUS			
M1	Stepper Motor Size 1	1	(FT73Q)
	DIL Socket 14-pin	1	(BL18U)
	DIL Socket 16-pin	1	(BL19V)

Movement Alarm

This simple but versatile alarm is triggered by movement of the unit, and it can be used in a variety of ways. As a burglar alarm it could be mounted on a door so that the unit is triggered when someone opens the door, and this could be the door of a car or caravan and not necessarily that of a building. The self-contained and portable nature of the unit also makes it well suited to applications such as a suitcase or television alarm, where the alarm will be activated if someone tries to remove the protected object. The unit could be made quite compact, making it suitable as protection for practically anything valuable which cannot be reliably screwed down.

There are various types of sensor which could be used, but a mercury switch is the obvious type to opt for. This type of switch is basically just two electrodes in a container made of an insulating material, and partially filled with mercury, where at some orientations the mercury only comes into contact with one or neither of the electrodes so that there is a very high resistance between them, but at other orientations the mercury touches both electrodes and completes electrical contact between the two. In an application of this type the switch should be set so that it is just off a point where it provides electrical contact, so that any slight movement or vibration at least momentarily activates the switch and triggers the alarm circuit.





Movement Alarm Circuit.

Basically, all that the circuit has to do is to provide a latching action from what might only be a momentary switching action from the sensor, and then use this signal to drive some form of audible alarm generator. If the unit is to be battery powered, it must also have an extremely low stand-by current consumption so that it can be left operating for long periods of time without significantly discharging the battery. In this design the latching is provided by a conventional set/reset flip/flop formed by IC1a and IC1b. The other two NOR gates of IC1 are left unused, but their inputs are tied to the negative supply rail in order to protect them against static charges, and also to ensure that the unused gates have an insignificant current consumption. In fact, by using a CMOS latch the quiescent current consumption of the circuit is kept down to just a fraction of a microamp, and it was found to be immeasurably low with my test gear. C2 provides the initial 'reset' pulse, to set the flip/flop to the correct output state at switch-on, while S1 is the mercury switch which sets the output to the high state when it is activated.

The output of the latch controls the alarm generator circuit via emitter follower buffer stage TR1. The latter is a silicon device with a low leakage level so that when the alarm is switched off it does not consume a significant amount of current. The alarm generator circuit is based on two 555 astable circuits with IC3 providing the audio tone and IC2 frequency modulating it. The modulation is obtained by loosely coupling the output of IC2 to the control voltage input of IC3 via R8, and this gives a simple but effective two tone 'warbling' alarm sound. LS1 is a cased ceramic resonator which gives high efficiency and a penetrating output at the relatively high audio frequencies involved here. If optimum volume is important, R7 can be replaced by a 1M preset which can then be adjusted to find the two frequencies which provide the greatest output.

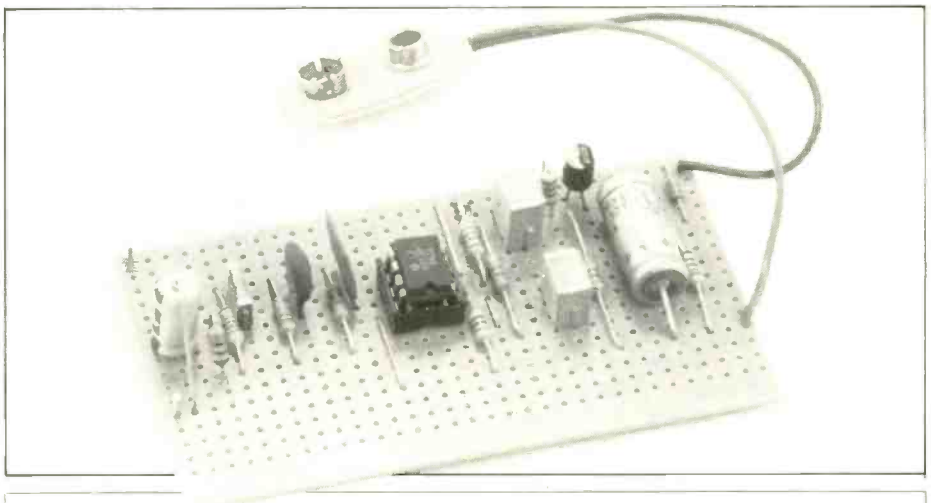
MOVEMENT ALARM PARTS LIST

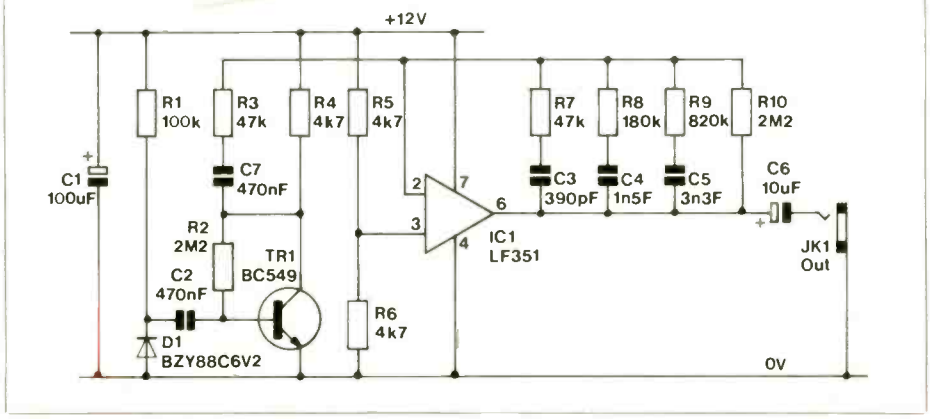
RESISTORS: All 0·6W 1% Metal Film			
R1,2	47k	2	(M47K)
R3	8k2	1	(M8K2)
R4,8	1M	2	(M1M)
R5	4M7	1	(M4M7)
R6	100k	1	(M100K)
R7	330k	1	(M330K)
CAPACITORS			
C1	470nF Poly Layer	1	(WW49D)
C2	100nF Poly Layer	1	(WW41U)
C3	22nF Poly Layer	1	(WW33L)
C4	470pF Polystyrene	1	(BX32K)
SEMICONDUCTORS			
IC1	4001BE	1	(QX01B)
IC2,3	ICM7555	2	(YH63T)
TR1	BC549	1	(QQ15R)
MISCELLANEOUS			
S1	Mercury Switch	1	(FA76H)
LS1	Piezo Sounder	1	(FM59P)
	DIL Socket 8-pin	1	(BL17T)
	DIL Socket 14-pin	1	(BL18U)

Pink Noise Generator

'White noise' is a well known term in the electronics world, and it is generally thought of as the 'hissing' background sound produced by audio circuits. White noise has a more precise definition though, and it is a noise signal which has equal amplitude at all frequencies. In other words, there is the same energy in (say) any 100Hz wide chunk of the spectrum, and would therefore be the same energy from 100Hz to 200Hz as there would from 20000Hz to 20100Hz. Logarithmic scaling is normally used on the frequency axis in frequency response charts, etc., and this is a more realistic way of looking at things. This has equal energy in octave or decade frequency bands, or to take a simple example, there would be the same amount of energy from 100Hz to 200Hz as there would from 20000Hz to 40000Hz.

The noise generated by audio circuits is generally of the genuine 'white' variety and is free from any significant colouration unless the circuit includes de-emphasis or some other form of frequency response tailoring. While white noise is ideal for many applications where noise is a help rather than a hinderance (percussion synthesisers, etc.), there are occasions when the alternative of 'pink' noise is required.





Pink Noise Generator Circuit.

This type of signal has equal energy over octave or decade bands, and could be regarded as noise having logarithmic scaling rather than the linear scaling of white noise. As far as the sound is concerned, white noise has the familiar high pitched 'hissing' sound, whereas pink noise is a deeper 'rushing' sound which is often likened to the sound of rain falling.

Pink noise is primarily used in audio testing, and in particular it is used in conjunction with an audio analyser as a very quick means of displaying irregularities in the frequency response of audio equipment. The main point here is that with the noise signal fed direct to the input of the analyser, all channels should indicate the same input level. Any lack of flatness in the frequency response, or anything interposed between the noise source and the analyser will be instantly and clearly displayed on the analyser.

It is probably impossible to directly generate pink noise, and it is therefore produced by first generating a white noise signal and then applying top cut filtering. This is the method adopted in the circuit shown here which uses zener diode D1 as the noise source, TR1 as a high gain amplifier to boost the noise signal to a usable level, and IC1 as an inverting amplifier with frequency selective negative feedback to provide the tailoring of the frequency response. The required slope is 3dB per octave, which is awkward in practice as a single stage C-R filter provides double this. Consequently a three stage feedback network is required, with a resistor added in series with each filter capacitor to prevent it from ever providing the full 6dB per octave roll-off. C3 provides the high frequency roll-off, with C4 and C5 providing the filtering at middle and bass frequencies respectively. The typical output level is around 2 volts peak to peak from a low source impedance, and the current consumption of the circuit is only about 4 milliamps. When constructing and using the unit, bear in mind that it has a substantial voltage, particularly at low frequencies, and it is therefore quite sensitive to pick-up of mains 'hum'.

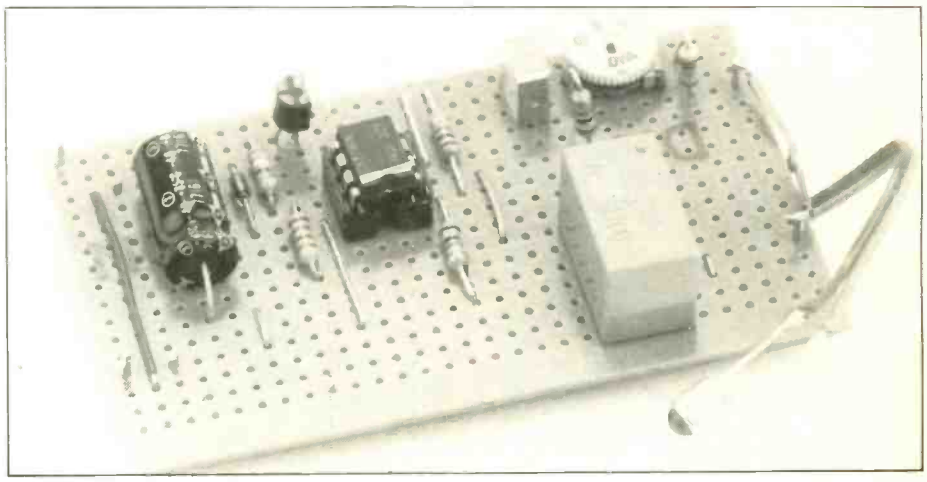
PINK NOISE GENERATOR PARTS LIST

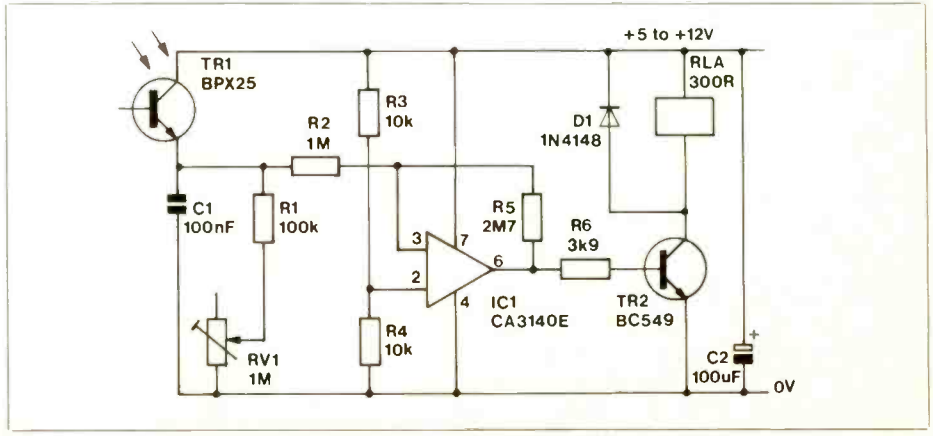
RESISTORS: All 0·6W 1% Metal Film			
R1	100k	1	(M100K)
R2,10	2M2	2	(M2M2)
R3,7	47k	2	(M4K7)
R8	180k	1	(M180K)
R9	820k	1	(M820K)
CAPACITORS			
C1	100µF 35V Axial	1	(FB49D)
C2,7	470nF Poly Layer	2	(WW49D)
C3	390pF Ceramic	1	(WX63T)
C4	1n5F Poly Layer	1	(WW23A)
C5	3n3F Poly Layer	1	(WW25C)
C6	10µF 50V PC Electrolytic	1	(FF04E)
SEMICONDUCTORS			
IC1	LF351	1	(WQ30H)
TR1	BC549	1	(QQ15R)
D1	BZY88C6V2	1	(QH09K)
MISCELLANEOUS			
JK1	Jack Socket 3·5mm	1	(HF82D)
	DIL Socket 8-pin	1	(BL17T)

Opto-Port

The standard approach to controlling external devices from a computer is to either use a built-in port such as a user or printer port, or to add a few latches onto the expansion bus. If a number of output lines are required this is certainly the most practical method, and probably represents the only practical way of doing things. If, on the other hand, only one or two output lines are required and operating speed is not of prime importance there are simple alternatives. The main two are to use either the sound output or the screen to control a simple switching circuit, and the circuit shown here is a simple screen operated switch (which is more generally applicable than the sound activated type).

In principle this type of circuit is very straightforward, with a photocell aimed at a small area of the screen. A simple software routine lights up that area of the screen to switch on the controlled device, or blanks out that part of the screen in order to switch it off. Things are complicated very slightly by the fact that the scanning process which is used to build up the television or monitor display results in a strong 50Hz ripple on the output from the photocell, and the circuit must smooth this out in





Opto-Port Circuit.

order to give a clean output signal. It is this factor which gives very limited operating speed in comparison to a conventional computer output port, but performance is still adequate in this respect for the majority of applications, including the obvious one of a relay driver.

TR1 is the photocell, and the TIL81 phototransistor is a fair choice for this as it offers good directivity, reasonable sensitivity, and is cheap (but more expensive devices such as the BPX25, which is the device shown in the circuit and Parts List, and the BPY62 will work in the circuit just as well, as will virtually any silicon npn phototransistor). It is used here as a sort of light dependant resistor with no connection being made to its base terminal. When subjected to darkness only minute leakage currents flow through TR1, giving virtually zero volts at its emitter terminal. When subjected to a reasonably strong light source quite high leakage currents flow, resulting in the voltage at its emitter approaching the positive supply voltage.

This gives roughly the required switching action, but the noise infested and high impedance output of TR1 needs to be both cleaned up and buffered in order to give a useful output signal. C1 smooths out much of the noise on the output signal, but its value has been kept low enough to keep the switching time down to a fraction of a second. This leaves a significant amount of noise on the signal, but this is counteracted by the large amount of hysteresis in the trigger circuit based on IC1.

OPTO-PORT PARTS LIST

RESISTORS: All 0·6W 1% Metal Film (Unless specified)			
R1	100k	1	(M100K)
R2	1MΩ	1	(M1M)
R3,4	10k	2	(M10K)
R5	2M7Ω	1	(M2M7)
R6	3k9	1	(M3K9)
RV1	1MΩ Hor Encl Preset	1	(UH09K)
CAPACITORS			
C1	100nF Poly Layer	1	(WW41U)
C2	100μF 35V Axial Electrolytic	1	(FB49D)
SEMICONDUCTORS			
IC1	CA3140E	1	(QH29G)
TR1	BPX25	1	(QF30H)
TR2	BC549	1	(QQ15R)
D1	1N4148	1	(QL80B)
MISCELLANEOUS			
RLA	Ultra-min Relay 12V DPDT	1	(YX95D)
	DIL Socket 8-pin	1	(BL17T)

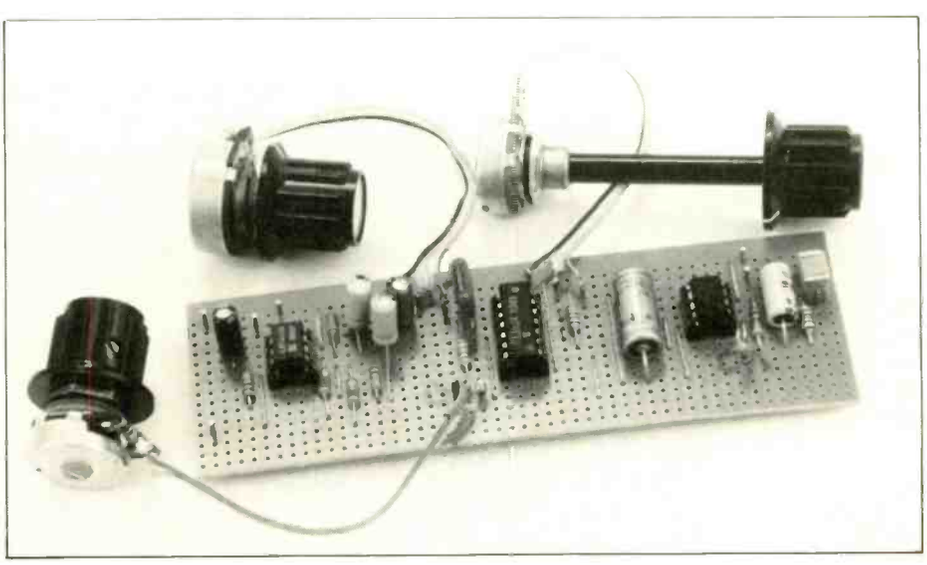
TR2 operates as the relay driver, and the relay can be any type with a coil resistance of around 300Ω or more, and a suitable operating voltage. The supply voltage can be anything from 5 to 12 volts, and must be chosen to suit the particular relay used. If a TTL compatible output is required it is merely necessary to use a 5 volt supply, omit D1, and to replace the relay with a 1kΩ resistor. Note though, that switching on the on-screen character sends the output low and not to the high state.

The circuit is quite sensitive and TR1 does not have to be fitted right up against the screen, although it will probably need to be no more than about 30 millimetres away. It is not necessary for the on-screen character to be a solid block, and something like a '@' symbol should suffice. TR1 is quite directional and must therefore be aimed at the character quite accurately. RV1 is adjusted by trial and error to find a setting that gives reliable results, and the exact setting will be very critical.

Metal Pedal

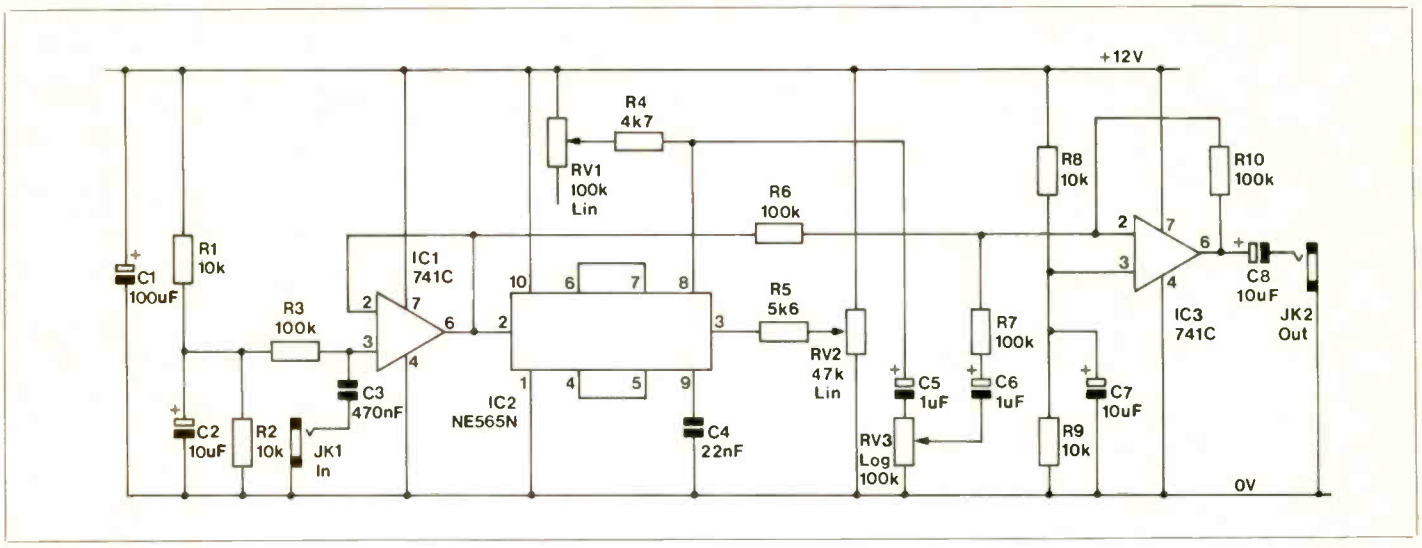
While not perhaps to everyone's taste, the so-called 'metal' sound is now an established electronic musical effect. Technically it is produced by mixing two signals creating sum and difference frequencies, neither of which are normally harmonically related to the original input frequencies. The result can be very discordant, or with the two input frequencies spaced at suitable musical intervals the result is a very rich sound, like bells, gongs, and similar metalic instruments (hence the 'metal' name).

The effect is simple in theory, but in practice it can be more difficult to get really good results. The usual set-up is to have a variable frequency oscillator feeding one input of the mixer (or 'ring modulator' as it is generally known in this application), with the output from a guitar or other instrument feeding into the second input. The ring modulated signal is then mixed into the straight-through signal in the required quantity. The usual problem is that of breakthrough of the oscillator signal at the output, and even if the ring modulator gives a respectable 40dB or so of carrier suppression this still leaves a clearly audible signal under no



input conditions. A noise gate is therefore normally required in order to render the breakthrough inaudible.

In this design, the need for a noise gate is avoided by having a very high degree of carrier suppression in the ring modulator, and the latter is actually the phase comparator of an NE565N phase locked loop (IC2). The VCO stage of this device acts as the carrier oscillator, and it provides a frequency range of approximately 100Hz to 2kHz with RV1 acting as the frequency control. RV2 is the carrier balance control, and this is carefully adjusted to minimise the carrier breakthrough at the output. It is a front



Metal Pedal Circuit.

panel control rather than a preset, as the optimum setting varies very slightly with changes in the carrier frequency, and although a good compromise setting can be found it was felt to be better to have the ability to null out the carrier as much as possible. The maximum degree of carrier suppression seems to be quite high, with around 80dB being achievable with the prototype.

IC1 simply acts as an input buffer stage which provides the unit with an input impedance of about 100kΩ. Its output is direct coupled to the input of IC2, for which it provides with the necessary input bias voltage. IC3 acts as a conventional summing mode mixer circuit which combines the modulated and straight-through signals. RV3 controls the amount or ring modulated signal that is mixed into the unprocessed signal. Signal levels of up to about 8 volts peak to peak can be handled using a 12 volt supply (the use of a 9 volt battery supply is not recommended). The current consumption is about 10 milliamps.

METAL PEDAL PARTS LIST

RESISTORS: All 0·6W 1% Metal Film (Unless specified)

R1,2,8,9	10k	4	(M10K)
R3,6,7,10	100k	4	(M100K)
R4	4k7	1	(M4K7)
R5	5k6	1	(M5K6)
RV1	100k LIN Pot	1	(FW05F)
RV2	47k LIN Pot	1	(FW04E)
RV3	100k LOG Pot	1	(FW25C)

CAPACITORS

C1	100μF 35V Axial Electrolytic	1	(FB49D)
C2,7,8	10μF 50V PC Electrolytic	3	(FF04E)
C3	470nF Poly Layer	1	(WW49D)
C4	22nF Poly Layer	1	(WW33L)
C5,6	1μF 100V PC Electrolytic	2	(FF01B)

SEMICONDUCTORS

IC1,3	μA741C (8-pin DIL)	2	(QL22Y)
IC2	NE565	1	(WQ56L)

MISCELLANEOUS

JK1,2	Standard Jack Socket	2	(HF91Y)
	DIL Socket 8-pin	2	(BL17T)
	DIL Socket 14-pin	1	(BL18U)

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