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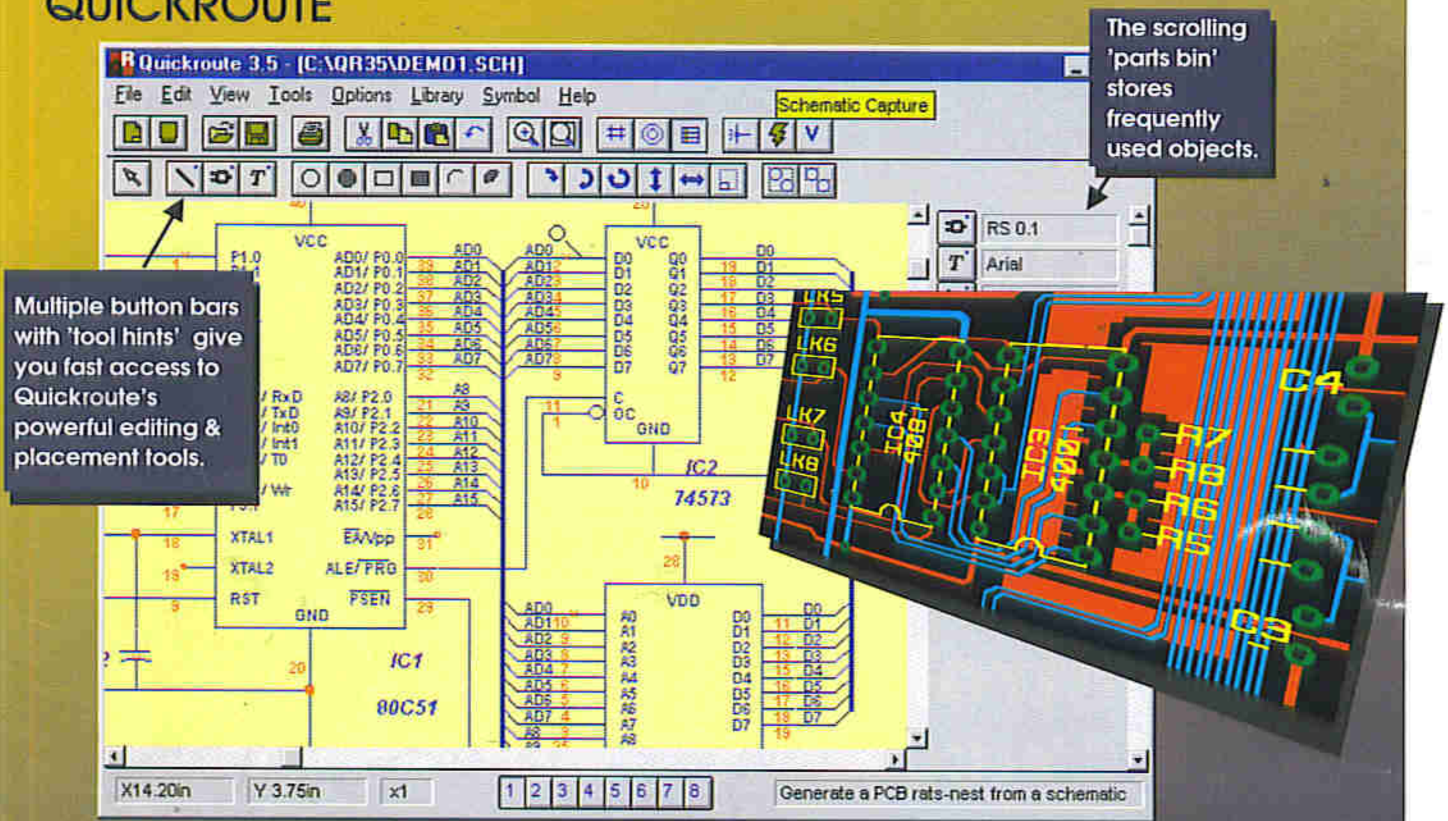

"..of all the products included here, this is my personal favourite... Really, thats all I have to say about Quickroute - it certainly gets my vote!" Review of QR 3.0 & other products Computer Shopper Nov 95

EASY TO USE
Quickroute 3.5 is a powerful, affordable and easy to use integrated schematic & PCB design system for Windows.™ With its multiple button bars, 'tool hints' and 'parts bin', Quickroute helps you to design quickly and efficiently

POWERFUL
There are four different versions of Quickroute giving you a choice of features & price. Quickroute is available with multi-sheet schematic capture, auto-routing, 'engineering change' (modification of a PCB from a schematic), copper fill, and a range of file import/export options. See the table for a selection of features.

AFFORDABLE
Prices are Designer (£149), PRO (£249) and PRO+ (£399). The Personal edition is available for just £68, but has the manual provided on disk as on-line help. Post & Packing is £5 (UK), £8 (EC), £12 (World). VAT must be added to the total price.

	Personal	Designer	PRO	PRO+
PCB & Schematic Design	✓	✓	✓	✓
Schematic Capture		✓	✓	✓
Auto router			✓	✓
Design Rule Checking			✓	✓
Export WMF & Tango			✓	✓
Export Gerber/NC-Drill			✓	✓
Extended Libraries			✓	✓
Tango + Gerber Import				✓
Update PCB from schematic				✓
DXF & SPICE Export				✓
Copper Fill				✓

QUICKROUTE SYSTEMS

MasterCard VISA SWITCH

Tel/Fax 0161 449 7101

Quickroute Systems Ltd., 14 Ley Lane, Marple Bridge, Stockport, SK6 5DD, U.K.
email info@quicksys.demon.co.uk

Phone now for more information

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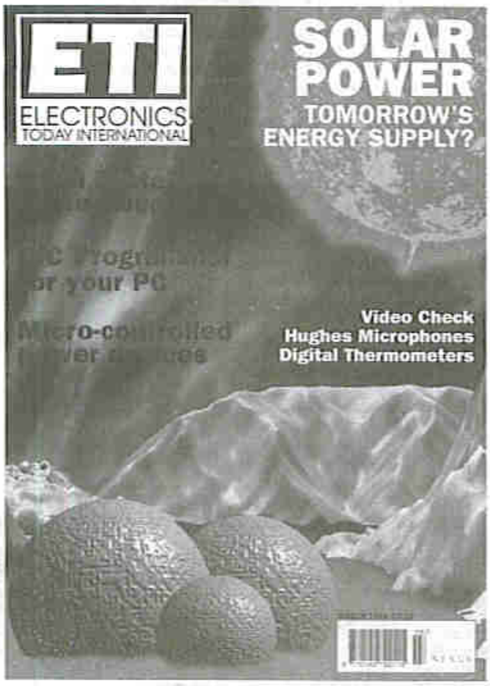
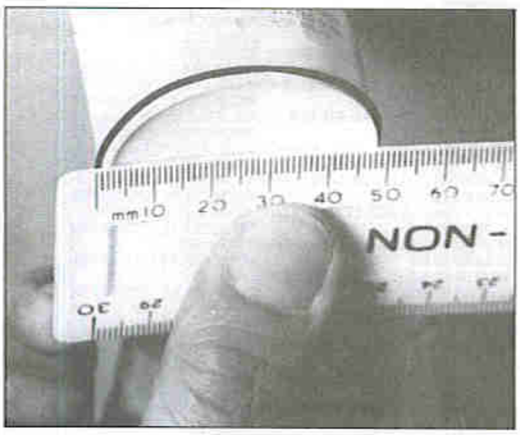
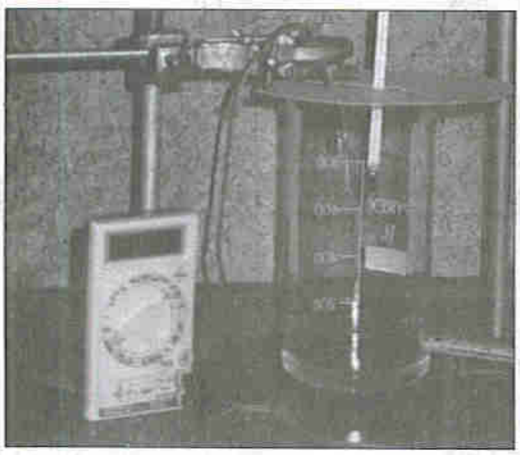
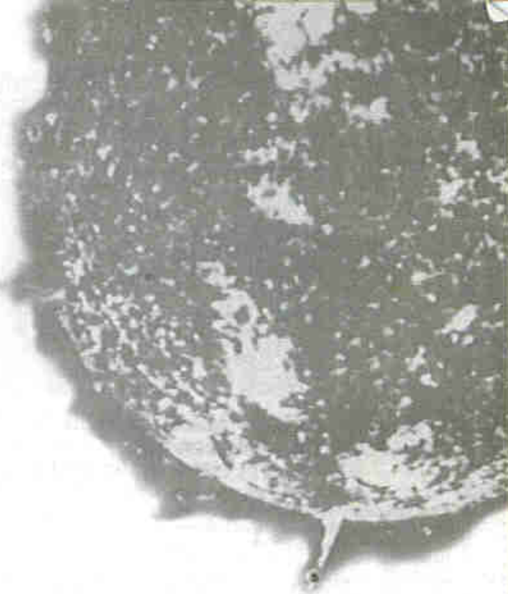


Volume 25 No.3

& Features Projects







Regulars

POWER AMPLIFIER MODULES-TURNTABLES-DIMMERS-LOUDSPEAKERS-19 INCH STEREO RACK AMPLIFIERS

★ PRICES INCLUDE V.A.T. ★ PROMPT DELIVERIES ★ FRIENDLY SERVICE ★ LARGE (A4) S.A.E., 60p STAMPED FOR CATALOGUE ★

OMP MOS-FET POWER AMPLIFIERS HIGH POWER, TWO CHANNEL 19 INCH RACK

THOUSANDS PURCHASED BY PROFESSIONAL USERS

THE RENOWNED MXF SERIES OF POWER AMPLIFIERS

FOUR MODELS:- **MXF200** (100W + 100W) **MXF400** (200W + 200W)
MXF600 (300W + 300W) **MXF900** (450W + 450W)

ALL POWER RATINGS R.M.S. INTO 4 OHMS, BOTH CHANNELS DRIVEN

FEATURES: ★Independent power supplies with two toroidal transformers ★ Twin L.E.D. Vu meters ★ Level controls ★ Illuminated on/off switch ★ XLR connectors ★ Standard 775mV inputs ★ Open and short circuit proof ★ Latest Mos-Fets for stress free power delivery into virtually any load ★ High slew rate ★ Very low distortion ★ Aluminium cases ★ MXF600 & MXF900 fan cooled with D.C. loudspeaker and thermal protection.

USED THE WORLD OVER IN CLUBS, PUBS, CINEMAS, DISCOS ETC.

SIZES:- MXF200 W19"xH3½" (2U)xD11"
MXF400 W19"xH5¼" (3U)xD12"
MXF600 W19"xH5¼" (3U)xD13"
MXF900 W19"xH5¼" (3U)xD14¾"

PRICES:-MXF200 £175.00 MXF400 £233.85
MXF600 £329.00 MXF900 £449.15
SPECIALIST CARRIER DEL. £12.50 EACH

OMP XO3 STEREO 3-WAY ACTIVE CROSS-OVER

Advanced 3-Way Stereo Active Cross-Over, housed in a 19" x 1U case. Each channel has three level controls: bass, mid & top. The removable front fascia allows access to the programmable DIL switches to adjust the cross-over frequency: Bass-Mid 250/500/800Hz, Mid-Top 1.8/3/5KHz, all at 24dB per octave. Bass invert switches on each bass channel. Nominal 775mV input/output. Fully compatible with OMP rack amplifier and modules.

Price £117.44 + £5.00 P&P

STEREO DISCO MIXER SDJ3400SE

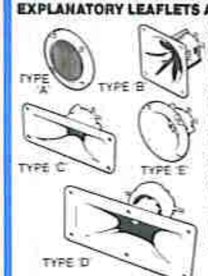
★ ECHO & SOUND EFFECTS★

STEREO DISCO MIXER with 2 x 7 band L & R graphic equalisers with bar graph LED Vu meters. **MANY OUTSTANDING FEATURES:-** including Echo with repeat & speed control, DJ Mic with talk-over switch, 6 Channels with individual faders plus cross fade, Cue Headphone Monitor. 8 Sound Effects. Useful combination of the following inputs:- 3 turntables (mag), 3 mics, 5 Line for CD, Tape, Video etc.

Price £144.99 + £5.00 P&P SIZE: 482 x 240 x 120mm

PIEZO ELECTRIC TWEETERS - MOTOROLA

Join the Piezo revolution! The low dynamic mass (no voice coil) of a Piezo tweeter produces an improved transient response with a lower distortion level than ordinary dynamic tweeters. As a crossover is not required these units can be added to existing speaker systems of up to 100 watts (more if two are put in series. **FREE EXPLANATORY LEAFLETS ARE SUPPLIED WITH EACH TWEETER.**



TYPE 'A' (KSN1036A) 3" round with protective wire mesh. Ideal for bookshelf and medium sized Hi-Fi apeakers. **Price £4.90 + 50p P&P.**

TYPE 'B' (KSN1005A) 3½" super horn for general purpose speakers, disco and P.A. systems etc. **Price £5.99 + 50p P&P.**

TYPE 'C' (KSN1016A) 2"x5" wide dispersion horn for quality Hi-Fi systems and quality discos etc. **Price £6.99 + 50p P&P.**

TYPE 'D' (KSN1025A) 2"x6" wide dispersion horn. Upper frequency response retained extending down to mid-range (2KHz). Suitable for high quality Hi-Fi systems and quality discos. **Price £9.99 + 50p P&P.**

TYPE 'E' (KSN1038A) 3¾" horn tweeter with attractive silver finish trim. Suitable for Hi-Fi monitor systems etc. **Price £5.99 + 50p P&P.**

LEVEL CONTROL Combines, on a recessed mounting plate, level control and cabinet input jack socket. 85x85mm. **Price £4.10 + 50p P&P.**

ibl FLIGHT CASED LOUDSPEAKERS

A new range of quality loudspeakers, designed to take advantage of the latest speaker technology and enclosure designs. Both models utilize studio quality 12" cast aluminium loudspeakers with factory fitted grilles, wide dispersion constant directivity horns, extruded aluminium corner protection and steel ball corners, complimented with heavy duty black covering. The enclosures are fitted as standard with top hats for optional loudspeaker stands.

POWER RATINGS QUOTED IN WATTS RMS FOR EACH CABINET FREQUENCY RESPONSE FULL RANGE 45Hz - 20KHz

***ibl* FC 12-100WATTS (100dB) PRICE £159.00 PER PAIR**
***ibl* FC 12-200WATTS (100dB) PRICE £175.00 PER PAIR**
SPECIALIST CARRIER DEL. £12.50 PER PAIR

OPTIONAL STANDS PRICE PER PAIR £49.00
Delivery £6.00 per pair

IN-CAR STEREO BOOSTER AMPS

THREE SUPERB HIGH POWER CAR STEREO BOOSTER AMPLIFIERS
150 WATTS (75 + 75) Stereo, 150W Bridged Mono
250 WATTS (125 + 125) Stereo, 250W Bridged Mono
400 WATTS (200 + 200) Stereo, 400W Bridged Mono
ALL POWERS INTO 4 OHMS

Features:
★ Stereo, bridgable mono ★ Choice of high & low level inputs ★ L & R level controls ★ Remote on-off ★ Speaker & thermal protection.

PRICES: 150W £49.99 250W £99.99
400W £109.95 P&P £2.00 EACH

OMP MOS-FET POWER AMPLIFIER MODULES

SUPPLIED READY BUILT AND TESTED.

These modules now enjoy a world-wide reputation for quality, reliability and performance at a realistic price. Four models are available to suit the needs of the professional and hobby market i.e. Industry, Leisure, Instrumental and Hi-Fi etc. When comparing prices, NOTE that all models include toroidal power supply, integral heat sink, glass fibre P.C.B. and drive circuits to power a compatible Vu meter. All models are open and short circuit proof.

THOUSANDS OF MODULES PURCHASED BY PROFESSIONAL USERS

OMP/MF 100 Mos-Fet Output power 110 watts R.M.S. into 4 ohms, frequency response 1Hz - 100KHz -3dB, Damping Factor >300, Slew Rate 45V/uS, T.H.D. typical 0.002%, Input Sensitivity 500mV, S.N.R. -110 dB. Size 300 x 123 x 60mm.
PRICE £40.85 + £3.50 P&P

OMP/MF 200 Mos-Fet Output power 200 watts R.M.S. into 4 ohms, frequency response 1Hz - 100KHz -3dB, Damping Factor >300, Slew Rate 50V/uS, T.H.D. typical 0.001%, Input Sensitivity 500mV, S.N.R. -110 dB. Size 300 x 155 x 100mm.
PRICE £64.35 + £4.00 P&P

OMP/MF 300 Mos-Fet Output power 300 watts R.M.S. into 4 ohms, frequency response 1Hz - 100KHz -3dB, Damping Factor >300, Slew Rate 60V/uS, T.H.D. typical 0.001%, Input Sensitivity 500mV, S.N.R. -110 dB. Size 330 x 175 x 100mm.
PRICE £81.75 + £5.00 P&P

OMP/MF 450 Mos-Fet Output power 450 watts R.M.S. into 4 ohms, frequency response 1Hz - 100KHz -3dB, Damping Factor >300, Slew Rate 75V/uS, T.H.D. typical 0.001%, Input Sensitivity 500mV, S.N.R. -110 dB, Fan Cooled, D.C. Loudspeaker Protection, 2 Second Anti-Thump Delay. Size 385 x 210 x 105mm.
PRICE £132.85 + £5.00 P&P

OMP/MF 1000 Mos-Fet Output power 1000 watts R.M.S. into 2 ohms, 725 watts R.M.S. into 4 ohms, frequency response 1Hz - 100KHz -3dB, Damping Factor >300, Slew Rate 75V/uS, T.H.D. typical 0.002%, Input Sensitivity 500mV, S.N.R. -110 dB, Fan Cooled, D.C. Loudspeaker Protection, 2 Second Anti-Thump Delay. Size 422 x 300 x 125mm.
PRICE £259.00 + £12.00 P&P

NOTE: MOS-FET MODULES ARE AVAILABLE IN TWO VERSIONS: STANDARD - INPUT SENS 500mV, BAND WIDTH 100KHz. PEC (PROFESSIONAL EQUIPMENT COMPATIBLE) - INPUT SENS 775mV, BAND WIDTH 50KHz. ORDER STANDARD OR PEC.

LOUDSPEAKERS

LARGE SELECTION OF SPECIALIST LOUDSPEAKERS AVAILABLE, INCLUDING CABINET FITTINGS, SPEAKER GRILLES, CROSS-OVERS AND HIGH POWER, HIGH FREQUENCY BULLETS AND HORNS, LARGE (A4) S.A.E. (60p STAMPED) FOR COMPLETE LIST.

McKenzie and Fane Loudspeakers are also available.

EMINENCE:- INSTRUMENTS, P.A., DISCO, ETC

ALL EMINENCE UNITS 8 OHMS IMPEDANCE

8" 100 WATT R.M.S. ME8-100 GEN. PURPOSE, LEAD GUITAR, EXCELLENT MID, DISCO.
RES. FREQ. 72Hz, FREQ. RESP. TO 4KHz, SENS 97dB. PRICE £32.71 + £2.00 P&P

10" 100 WATT R.M.S. ME10-100 GUITAR, VOCAL, KEYBOARD, DISCO, EXCELLENT MID.
RES. FREQ. 71Hz, FREQ. RESP. TO 7KHz, SENS97dB. PRICE £33.74 + £2.50 P&P

10" 200 WATT R.M.S. ME10-200 GUITAR, KEYB'D, DISCO, VOCAL, EXCELLENT HIGH POWER MID.
RES. FREQ. 65Hz, FREQ. RESP. TO 3.5KHz, SENS 99dB. PRICE £43.47 + £2.50 P&P

12" 100 WATT R.M.S. ME12-100LE GEN. PURPOSE, LEAD GUITAR, DISCO, STAGE MONITOR.
RES.FREQ. 49Hz, FREQ. RESP. TO 6KHz, SENS 100dB. PRICE £35.64 + £3.50 P&P

12" 100 WATT R.M.S. ME12-100LT (TWIN CONE) WIDE RESPONSE, P.A., VOCAL, STAGE MONITOR. RES. FREQ 42Hz, FREQ. RESP. TO 10KHz, SENS 98dB. PRICE £36.67 + £3.50 P&P

12" 200 WATT R.M.S. ME12-200 GEN. PURPOSE, GUITAR, DISCO, VOCAL, EXCELLENT MID.
RES. FREQ. 58Hz, FREQ. RESP. TO 6KHz, SENS 98dB. PRICE £46.71 + £3.50 P&P

12" 300 WATT R.M.S ME12-300GP HIGH POWER BASS, LEAD GUITAR, KEYBOARD, DISCO ETC.
RES. FREQ. 47Hz, FREQ. RESP. TO 5KHz, SENS 103dB. PRICE £70.19 + £3.50 P&P

15" 200 WATT R.M.S. ME15-200 GEN. PURPOSE BASS, INCLUDING BASS GUITAR.
RES. FREQ. 46Hz, FREQ. RESP. TO 5KHz, SENS 99dB. PRICE £50.72 + £4.00 P&P

15" 300 WATT R.M.S. ME15-300 HIGH POWER BASS, INCLUDING BASS GUITAR.
RES. FREQ. 39Hz, FREQ. RESP. TO 3KHz, SENS 103dB. PRICE £73.34 + £4.00 P&P

EARBENDERS:- HI-FI, STUDIO, IN-CAR, ETC

ALL EARBENDER UNITS 8 OHMS (Except EB8-50 & EB10-50 which are dual impedance tapped @ 4 & 8 ohm)

BASS, SINGLE CONE, HIGH COMPLIANCE, ROLLED SURROUND

8" 50watt EB8-50 DUAL IMPEDENCE, TAPPED 4/8 OHM BASS, HI-FI, IN-CAR.
RES. FREQ. 40Hz, FREQ. RESP. TO 7KHz SENS 97dB. PRICE £8.90 + £2.00 P&P

10" 50WATT EB10-50 DUAL IMPEDENCE, TAPPED 4/8 OHM BASS, HI-FI, IN-CAR.
RES. FREQ. 40Hz, FREQ. RESP. TO 5KHz, SENS. 99dB. PRICE £13.65 + £2.50 P&P

10" 100WATT EB10-100 BASS, HI-FI, STUDIO.
RES. FREQ. 35Hz, FREQ. RESP. TO 3KHz, SENS 96dB. PRICE £30.39 + £3.50 P&P

12" 100WATT EB12-100 BASS, STUDIO, HI-FI, EXCELLENT DISCO.
RES. FREQ. 26Hz, FREQ. RESP. TO 3 KHz, SENS 93dB. PRICE £42.12 + £3.50 P&P

FULL RANGE TWIN CONE, HIGH COMPLIANCE, ROLLED SURROUND

5¼" 60WATT EB5-60TC (TWIN CONE) HI-FI, MULTI-ARRAY DISCO ETC.
RES. FREQ. 63Hz, FREQ. RESP. TO 20KHz, SENS 92dB. PRICE £9.99 + £1.50 P&P

6½" 60WATT EB6-60TC (TWIN CONE) HI-FI, MULTI-ARRAY DISCO ETC.
RES. FREQ. 38Hz, FREQ. RESP. TO 20KHz, SENS 94dB. PRICE £10.99 + 1.50 P&P

8" 60WATT EB8-60TC (TWIN CONE) HI-FI, MILTI-ARRAY DISCO ETC.
RES. FREQ. 40Hz, FREQ. RESP. TO 18KHz, SENS 89dB. PRICE £12.99 + £1.50 P&P

10" 60WATT EB10-60TC (TWIN CONE) HI-FI, MULTI ARRAY DISCO ETC.
RES. FREQ. 35Hz, FREQ. RESP. TO 12KHz, SENS 98dB. PRICE £16.49 + £2.00 P&P

TRANSMITTER HOBBY KITS

PROVEN TRANSMITTER DESIGNS INCLUDING GLASS FIBRE PRINTED CIRCUIT BOARD AND HIGH QUALITY COMPONENTS COMPLETE WITH CIRCUIT AND INSTRUCTIONS

3W TRANSMITTER 80-108MHz, VARICAP CONTROLLED PROFESSIONAL PERFORMANCE, RANGE UP TO 3 MILES, SIZE 38 x 123mm, SUPPLY 12V @ 0.5AMP.
PRICE £14.85 + £1.00 P&P

FM MICRO TRANSMITTER 100-108MHz, VARICAP TUNED, COMPLETE WITH VERY SENS FET MIC, RANGE 100-300m, SIZE 56 x 46mm, SUPPLY 9V BATTERY.
PRICE £8.80 + £1.00 P&P

PHOTO: 3W FM TRANSMITTER

POSTAL CHARGES PER ORDER £1.00 MINIMUM. OFFICIAL ORDERS FROM SCHOOLS, COLLEGES, GOVT. BODIES, PLC's ETC. PRICES INCLUSIVE OF V.A.T. SALES COUNTER. VISA AND ACCESS ACCEPTED BY POST, PHONE OR FAX.

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News...

Flexible transistor analyser

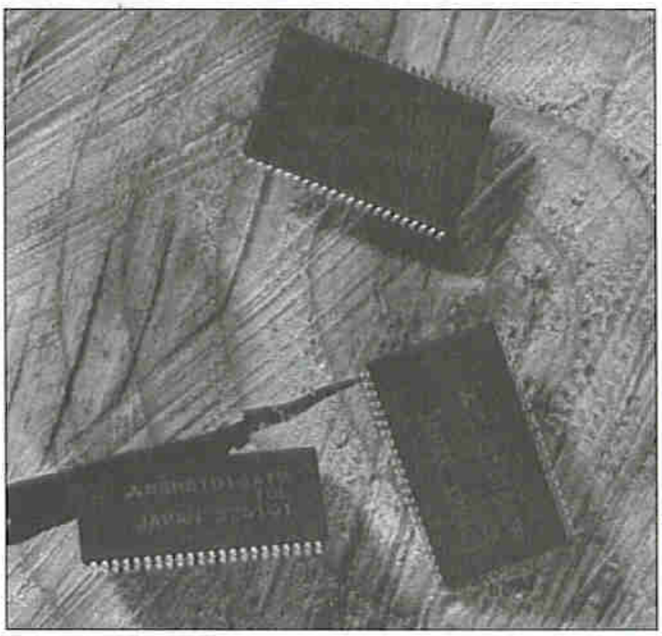
Originally a prizewinner in The Young Engineer for Britain Competition, the DTA30 is now in full production.

The DTA30 is a microcontrolled instrument that quickly and easily analyses any type of bipolar transistor. Complex signals are applied to the transistor under test and their effects are analysed by the internal microcontroller. The results of these signal tests are used to determine the transistor lead identities and the transistor type.

Each lead identity is displayed by a multicolour LED illuminating the colour of the test lead that is connected to the base, emitter and collector. The transistor type is also displayed by one of the NPN/PNP LEDs. Three flashing red LEDs indicate a fault condition.

For further information, contact Peak Electronic Design Ltd, 70 Nunsfield Road, Buxton, Derbyshire SK17 7BW.

Mitsubishi sets up 1Mb SRAM second sourcing agreement with Seiko Epson



Mitsubishi Electric is announcing a second sourcing agreement with Seiko Epson for the mass production of x16bit organised 1 Mbit SRAMs. Mitsubishi's M5M51016A device is the market standard and Seiko Epson will begin mass production of its compatible SRM21016 device by Spring '96.

The SRAM devices are ideal for mobile communications applications, with the x16bit organisation making for efficient high-speed data transfer, with low power consumption and low noise. Seiko Epson will mass produce the devices at its Fujimi-Works and Tohoku-Epson factories with expected production at around 300,000/month.

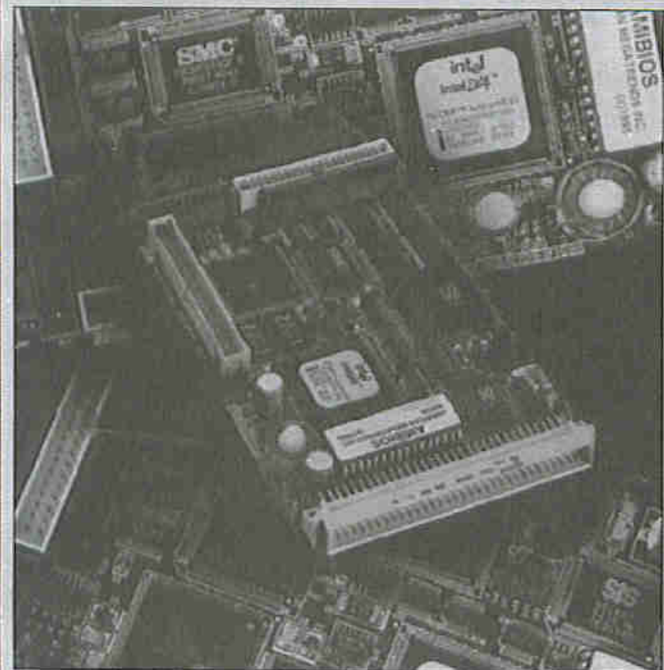
Mitsubishi is Europe's leading supplier of low power SRAM devices with an 80% share of the x16bit 1Mbit SRAM market. The company produces 200,000 devices/month for European mobile phone applications alone.

Mitsubishi is also driving the leading edge of SRAM technology and is now shipping in production quantities its new 4Mbit thin film transistor (TFT) cell based SRAM. The TFT cell, in conjunction with the chip's 0.5um full CMOS circuitry, has resulted in the high density, low-power design which is ideal for high reliability, portable applications and telecommunications equipment, as well as IC and memory card type applications where battery back-up is used to provide portable, non-volatile mass data storage.

Mitsubishi low power 1 Mbit SRAMs are also available in 128kx8bit configuration as well as the word wide 64kx16bit version which is the subject of the Seiko Epson agreement. Both are ideal for portable and battery powered applications such as mobile phones and computer equipment. The word wide 64kx 16bit device further provides an ideal space and power efficient, single chip replacement for shallow memory applications using 32kx8bit and 128kx8bit organised SRAMs.

For further information contact: Mitsubishi Electric UK Ltd, Semiconductor Division. Tel:01707-276100

Industrial-grade PC controller



Arcom Control Systems is launching the most powerful and highly-integrated STEbus PC-compatible ever made, providing a 486-based single-board solution capable of handling the most demanding embedded DOS and Windows applications. Called SCPC486DX it is based on the full 32-bit Intel 486DX4 processor running at l00MHz.

The new board combines the CPU with up to l6Mbytes DRAM, 4Mbytes Flash EPROM for diskless operation, plus local-bus SVGA with outputs for either CRT or flat-panel/LCD, onto a compact 100xl6Omm single Eurocard designed specifically for industrial applications.

SCPC486DX is targeted at machinery and process automation system builders seeking exceptional levels of computing and graphics performance, for use in demanding realtime control applications, or as a powerful man-machine interface for sophisticated, graphical-intensive instrumentation.

Further on-board hardware includes keyboard-, mouse-, IDE- and floppy-interfaces, battery-backed real-time clock and watchdog timer, and COMl, COM2 and LPTl ports.

Because SCPC486DX is fully PC AT-compatible, applications software can be developed on the board itself. This greatly speeds the realtime systems design process, allowing debug to take place directly on the target hardware. When development is complete, Arcom offers a support package called SiliconDrive which allows software to be blown into ROMdisk/RAMdisk, for operation in harsh industrial environments where conventional disks are unsuitable. The company has also ported Microsoft's Flash Filing System 2 onto the board, providing full rewrite solid-state disk emulation.

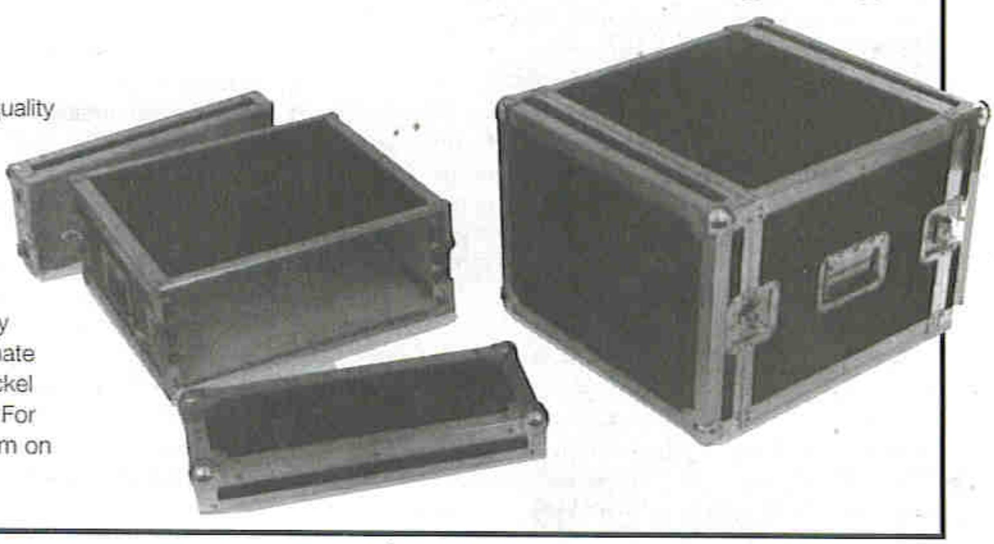
Based on the international IEEE-l000 STEbus standard, SCPC486DX can be expanded to create high-functionality control systems in rugged 3U card cages. Implemented via the reliable 2-part DIN4l612 connector, the backplane bus interface allows systems to utilise up to 21 boards - providing space for hundreds of I/O channels; the board also includes full multi-master arbitration, allowing designers to construct very high performance computers employing parallel processing techniques.

For further information, contact Arcom Control Systems on +44 (0) 1223 411200; fax 410457

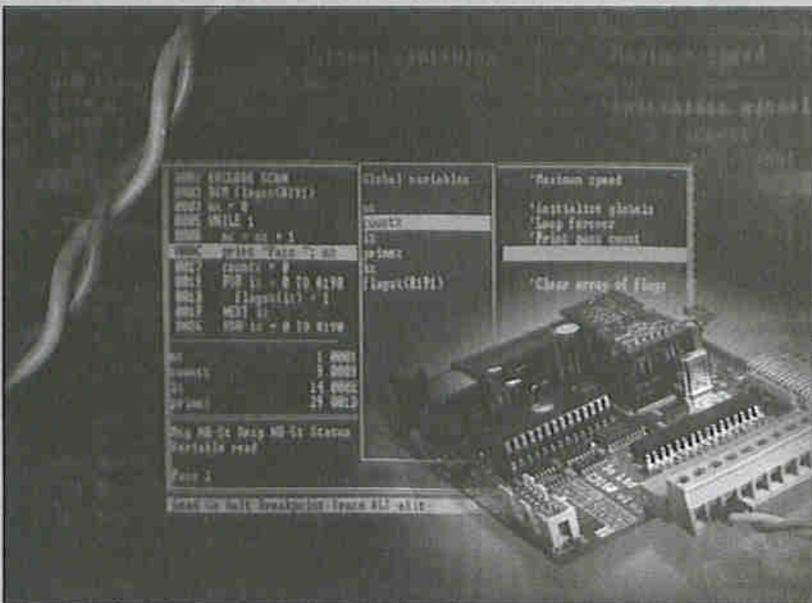
Electronics on the move

Grovestream Engineering Services of Hampshire specialise in building high quality cases for the transport of sensitive electronic equipment and also offer custom-size cases with a minimal change in price over the standard range.

All flight cases, 19" rack cabinets and boxes are constructed from high quality birch ply, with aluminium or black laminate finish, extruded aluminium sections, nickel plated steel ball corners and brackets. For further information, contact Grovestream on 01734-713309.



Low cost BASIC programming for control networks



Io Ltd has launched an independent application development tool for Echelon's powerful LonWorks control network technology. Called NetBasic, it provides engineers with a PC-hosted Basic programming environment for an outlay of under £500, cutting thousands from the normal cost of a development system, and providing an ideal entry point for the many companies currently considering the use of fieldbuses. The new package generates code for the IoNet range of remote I/O modules which provide processor, analog, digital and high power I/O functions in the form of cost-effective multi-channel modules. OEM licenses are also available.

Io developed this tool to overcome the single biggest barrier to the take-up of fieldbus technology - its high entry cost. The company has seen immense interest in its LonWorks-based

I/O, but encountered resistance, particularly from smaller companies and users with relatively small-scale projects who have typically elected to stay with current products until development costs fall. NetBasic resolves this issue. With this new tool, engineers can equip a PC with a LonWorks programming environment for less than £500, and add some real networked hardware to begin evaluating distributed control ideas, all for under a thousand pounds.

NetBasic is designed to provide a much simpler route to the design of LonWorks-compatible networked control systems, by opting for the familiar BASIC language in preference to the C environment available up to now. The overhead of designing for networked operation is also minimised through the use of intrinsically-simple extensions to the BASIC language. These additions provide a method of developing software for distributed system operation which allow communications with any other LonWorks nodes using just an address plus simple rewrite-type commands. For familiarity, NetBasic uses syntax which is similar to Visual Basic.

The NetBasic development environment costs £490 for a single user licence; there are no run-time royalties. Io is also offering a bundled 'starter kit' to help companies explore the powerful LonWorks fieldbus. This combines NetBasic with a serial adapter node to link a PC to a LonWorks network, together with a remote I/O node containing a Neuron 3150 CPU and eight I/O channels, for just £995. Optionally, NetBasic can be supplied for use with Echelon's serial adapter interfaces.

Initially, NetBasic generates code for IoNet remote I/O sub-systems, or nodes. These perform conventional industrial I/O functions, but may be transparently linked to any other IonWorks node to extend capability. As input or output variables - regardless of which node on the network they originate from - can be treated by an IoNet system as local data, powerful integrated systems can be built by siting intelligent building blocks exactly where they are needed. This provides very significant cable and termination savings, together with higher levels of fault tolerance and reliability. The cable savings alone from such a digital fieldbus system can trim costs by as much as a third. And, as a company's automation requirements evolve, functionality may be extended by simply plugging further nodes onto the network.

Nodes are configured from a range of l00xl00mm PCBs, offering processor, analog, digital and high current I/O with optional man-machine interfaces and communications gateways to other platforms/networks. Modules are interconnected using an industry standard serial highway, and packaged in compact EMC-compliant, DINrail- or panel-mounting, IP30 metal cases suitable for harsh environments. Each node comes with built-in firmware allowing it to perform simple data acquisition and control. Standard digital I/O functions available include bit, nibble and byte input; pulse count, time, frequency and period measurement; level detection; quadrature input; edge-log input for measuring low and high periods; analog I/O functions include high-resolution 4-20mA and voltage inputs.

For further information, contact Io Ltd on +44 (0)1638 742390.

New from NEC

NEC Electronics has announced a new range of SIMMS memory modules that utilises its recently launched I6MB EDO DRAM. The range includes 4 MByte, 8 MByte and 16 KByte modules. The 16KB EDO DRAM provides the modules with more than a 25% speed increase, from a page mode cycle time of only 25 nanoseconds.

Because of their increased bandwidth and compatibility with fast page devices, EDO DRAMs are becoming the preferred device over standard fast page memories, and their incorporation into SIMMS modules is seen as natural progression.

EDO DRAMs maintain valid data on their output even after the CAS (column address strobe) has been toggled to a high state, enabling the data to be used during the CAS pre-charge time. The benefit of this architecture is that it allows the cycle time to be reduced to 25ns, thus increasing overall bandwidth.

The range of SIMMS is designated as MG-421000F32 (IM word by 32 bit), MG-422000F32 (2M word by 32 bit) and MG-424000F32 (4M word by 32 bit). On the 4 MByte and 8 MByte SIMMS the 16MB DRAM is a uPD42I8I65 while a I6MB EDO DRAM type uPD4217405 is used on the 16 MByte SIMM.

Power consumption is 11 mW, 22 mW and 44 mW in standby for the 4 MByte, 8 MByte and 16 MByte modules respectively. Decoupling capacitors are mounted on the power supply line for noise reduction.

These modules provide high density and large quantities of memory in a small space without utilising the surface-mounting technology on the printed circuit board. The SIMMS are supplied in 72-pin single in-line modules.

For more information contact: NEC Electronics (UK) Ltd Tel: 01908 691133

High sound quality from real musical instruments

NEC Electronics' new wave table synthesis chipset generates the high quality sound required by the new generation of multimedia personal computers. Jointly developed with Spectrum Signal Processing Ltd, the Sound Festa chipset is based on samples from real musical instruments and meets the MPC3 standard proposed by the Software Publishers Association.

Whilst sound boards have traditionally been used in personal computers to generate sound effects for video games, there is now an increasing requirement to use them as the source of much higher quality music. Wave table synthesis technology is capable of delivering this quality but requires complex and high-speed data processing and, as such, has not been widely used to date.

NEC's Sound Festa solves these problems and allows wave table synthesis to be used for practical purposes. It consists of a sound processor (NPD77525), a music controller (UPD77526) and a sound codec (UPD63310).

The small size of the Sound Festa chipset enables the sound board to be halved in size providing space saving benefits for manufacturers. Furthermore, by using data sampled from real musical instruments, a maximum of 32 voices can be generated simultaneously. NEC co-operated with musical instrument manufacturer Korg for a definition of the wave table and this has contributed to the high level of sound quality.

The chipset contains on-chip SoundBlaster Pro™ functions to provide compatibility with a variety of games software, and FM sound synthesis is realised by OPL2/3 emulation on the uPD77525 DSP circuit. Various acoustic effects are also possible such as two-speaker 3D sound effects (Qsound™), reverberation and a chorus of musical instruments.

Sound Festa also uses PCM/ADPCM compression techniques to allow recording of audio signals from all inputs and simultaneous recording and playback. The chipset supports different memory and FM synthesiser configurations so that it can be easily adapted to individual performance and cost requirements.

NEC will support the Sound Festa chipset with driver software capable of playing MIDI and wave data, an MS Windows™ based graphical user interface and high-quality wave-table data and hardware design documentation.

Contact:NEC Electronics (UK) Ltd on 01908 691133

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Solar Electric Power

Douglas Clarkson looks at the future for solar power, and finds that even in the UK the future is bright

Without consciously developing as such, modern industrialised society has become critically dependent upon the availability and also the cost of energy. In almost every manufactured item is a net energy cost - from that of a glass milk-bottle to that of a modern jet airliner. At present the contribution of solar electric power to the world's energy is minuscule but likely to grow rapidly as new fabrication techniques of thin film photovoltaic materials come on stream.

Energy carelessness

A lot of scientific and technological effort goes into developing alternative sources of energy and this is both relevant and appropriate. There is, however, what may be described as the effect of inherited carelessness in the use of energy. In looking at the domestic supply, if the assortment of kitchen appliances, home entertainment equipment, lighting - interior and exterior is examined, then an annual consumption value of 5000 kWH would probably be typical. With the use of more energy-efficient appliances, however, this could probably be reduced by at least 15% to 20%. Where, for example, a solar enthusiast has invested in solar electric power for domestic use to produce this same percentage of base power needs, the same power saving could have been achieved merely through wiser selection of appliances. Clearly, if significant investment is going to be made in solar electric power, it is common sense to minimise power needs initially and then implement solar electric power systems.

All is one in the sun

With the probable exception of nuclear energy and tidal energy, all key forms of energy currently in use are derived ultimately from the sun. Fossil fuels, for example, are the legacy of more youthful sunshine. Wind and wave power energies derive their energy from the energy imparted to the earth's weather systems by solar radiation.

Solar radiation can be directly utilised in forms of passive heating, active heating, solar 'thermal' electric conversion and

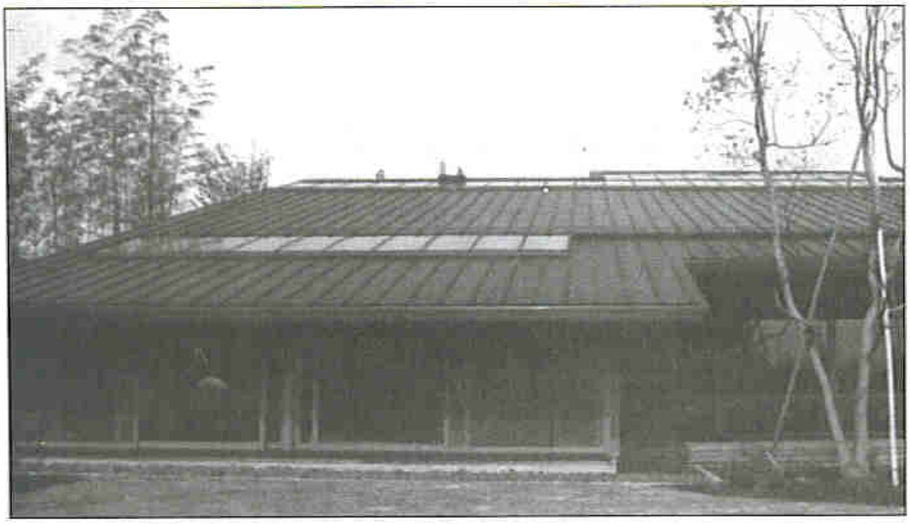


photo-electric conversion. In passive heating, sunlight streaming through windows provides a heating effect and can often be used to reduce heating costs. In active heating, heat can be collected in solar thermal collectors and stored in hot water tanks.

Significant investment has also been undertaken on solar thermal 'electric' systems. In the so-called 'trough' concentrator, sunlight is focused along a mirror trough onto a vacuum collector tube and the heated fluid used to drive a turbine generator. Over a million square metres of collector capacity is located at the SEGS plant in Kramer Junction, California - providing 354 MW of peak capacity. Such installations, however, require economies of scale to improve efficiencies and are not cost-effective for domestic or small scale applications. The cost of maintenance of such systems - although being reduced, is higher than that of photovoltaic systems.

In photovoltaic systems, the solar energy is converted to electrical energy and stored in battery systems or converted to alternating current and fed directly back into the distribution grid. This article is primarily referencing such photovoltaic systems.

World levels of insolation

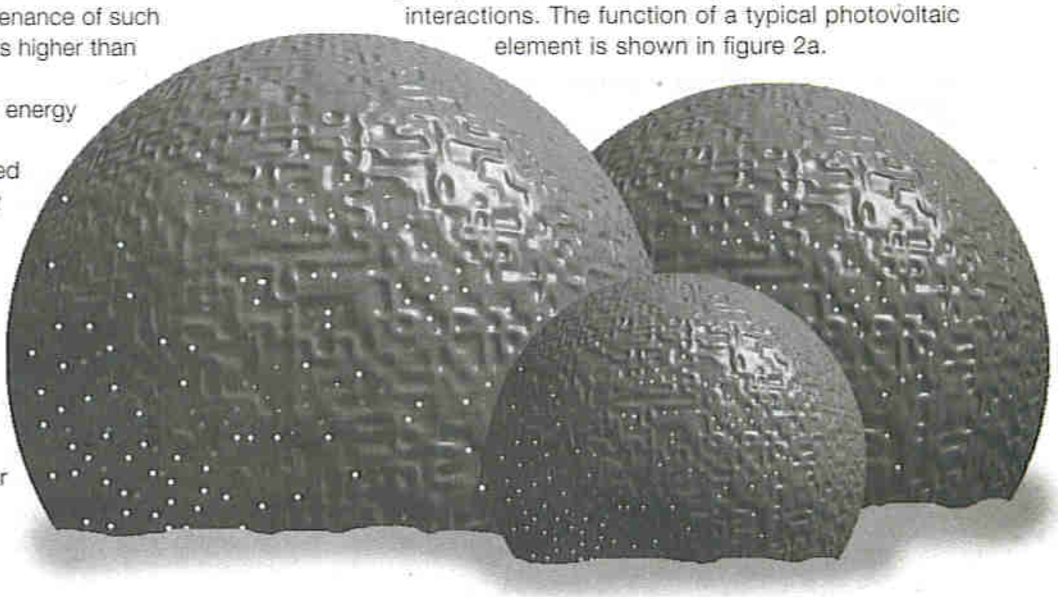
There may be some significance that, in the main, it is the developing world which has a clear advantage of high levels of insolation. Thus, over major areas of Africa, India and South America there is considerable potential for solar photovoltaic power. As may be expected, higher levels of sunshine are found closer to the equator. Values can range from as high as 7 kWhrs/m2 per day in parts of Western USA to less than 0.5 kWhrs/m2 per day in latitudes greater than 65 degrees north or south. A useful reference of world levels of insolation is published by the Solarex Corporation. In many ways, the location of maximum levels of sunshine coincide with areas of low population density - e.g. hot, arid desert regions of North Africa and Australia. Within Europe, the southern fringe of Spain exceeds levels of 4 kWhrs/m2 per day compared with between 0.6 kWhrs/m2 per day and 1.5 kWhrs/m2 per day in the UK. This reduction in solar radiation in high latitudes, however, is in some way compensated for by the corresponding increase in available wind power.

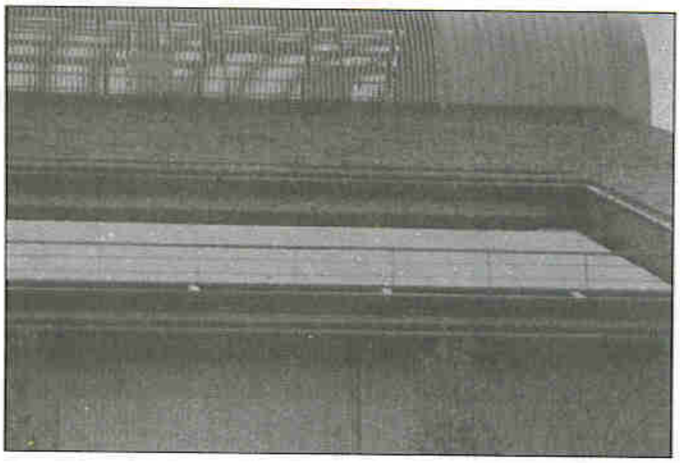
Figure 1 indicates how solar radiation in reaching the surface of the earth can travel through different extents of the atmosphere. The air mass from direct overhead illumination is termed AM1 - air mass one. In space, above the atmosphere, the air mass factor is referenced as AM0 - air mass zero. In solar studies where the performance of solar panels is being measured, great care is required to reference measurements against a specific AM value. It is typical to quote value of panel performance at AM1.5. At higher air mass values, the atmosphere progressively absorbs energy output.

Photovoltaic cell technology

Light is absorbed in approximately 2 to 3mm thick elements of silicon with most being absorbed in the first 0.5 mm of standard silicon. If the cell thickness is made too thin then light absorption will be incomplete and cell efficiency correspondingly low.

Most conventional processes for solar cell production still utilise conventional CZ silicon grown by standard crystallography methods. The silicon elements are cut, suitably doped with typically front layer doped n-type and rear layer doped p type. The cell has metallisation applied to carry away the electrons freed by the photovoltaic interactions. The function of a typical photovoltaic element is shown in figure 2a.





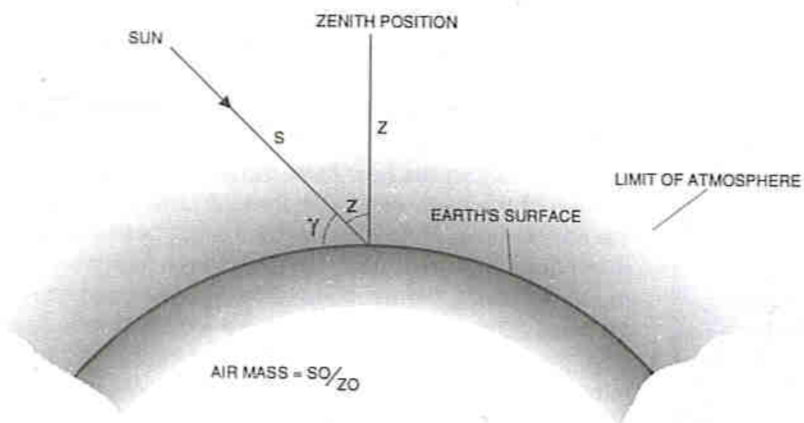


Figure 1: Derivation of air mass terms for solar radiation.

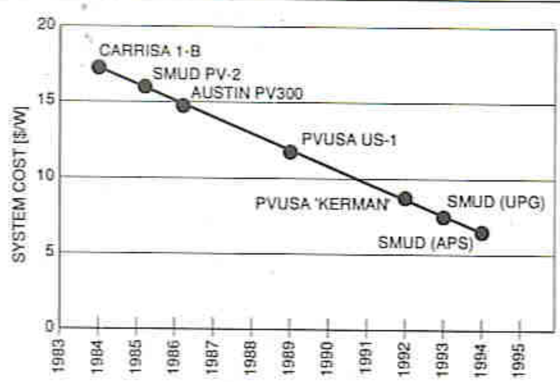


Figure 10: Reduction in cost of utility PV installation (Courtesy US Department of Energy)

In assessing photovoltaic efficiency of crystalline silicon, approximately half of the sunlight is not sufficiently energetic to eject photons from the silicon material. Of the electrons which are emitted, roughly half is lost due to random motion of electrons due to thermal agitation. A variety of processes results in further losses depending on the level of impurities in the silicon material.

A key parameter of any cell is its response as a function of wavelength. Figure 2b indicates the response of a range of semiconductor materials with reference to sunlight spectra. Most materials tend to have a poor response between 400 nm and 600 nm - in a region where the solar spectrum is peaking. The response of amorphous silicon (a-Si) is cutting off at about 700 nm.

In order to try and improve this response, so-called multijunction cells are being developed with layers which are sensitive in specific parts of the solar spectrum. Figure 9c indicates a set of layer responses for three layer and two layer materials being researched in Japan. An efficiency of 29.5% has been achieved for a small multijunction GInP/Ga As cell by the NREL in the USA while the best amorphous silicon based devices have an efficiency of around 12.4%.

Even now, however, preference is given to the reliability and higher efficiencies of solar cells manufactured using crystalline silicon. The higher efficiencies of crystalline silicon allow for installations to produce higher outputs from a specific solar catchment areaThe highest conversion efficiency of crystalline silicon is now around 23%.

Researchers at Sandia National Laboratories in New Mexico, USA, have assisted manufacturers in producing multi crystalline silicon cells with an efficiency in excess of 15%. The multicrystalline silicon cells have higher reflectance than single crystalline cells and consequently considerable work has been undertaken to improve the cell efficiency by reducing such reflectance. One approach is to physically machine the surface of the multicrystalline cell to make the surface smoother. The other approach is to coat the multicrystalline cell with an encapsulation layer so that light scattered from the multicrystalline layer is reflected off the upper air/coating interface as indicated in figure 3.

Thin films of amorphous silicon are manufactured having layers between 1 micron and 10 microns in thickness - about 30 to 100 times thinner than wafer manufactured cells. While production efficiencies of such amorphous silicon are around 6%, prototype materials are already being demonstrated with efficiencies in excess of 12%. There is also interest in Cadmium Telluride (CdTe) and CIGS (CuInGeSe) cells. CIGS cells can now achieve an efficiency of 13.9% and CdTe cells can now be produced with an efficiency of 15.8%.

In photovoltaics at present around 85% of production is crystalline silicon and the 15% remainder thin film. There must be a point, however, where new faster fabrication techniques will dominate the production of photovoltaic materials. There is, however, considerable caution being exercised since no manufacturer wants to supply material which degrades in use and requires replacement. Photovoltaic materials are now being supplied with 10-year warranties with expected useful operating times of 30 years.

Where products are for occasional domestic use - for example, on holiday homes or boats - then total area of panel is not a prime factor, since there is usually plenty of area available for siting such panels. The modules manufactured by Uni-Solar in the USA, for example, which use an amorphous silicon production technique, have an efficiency of around 5%. This type of product, however, is more adaptable to develop as a roof tile 'look alike' product which has a high level of environmental acceptance as indicated in figure 4. Uni-Solar has several

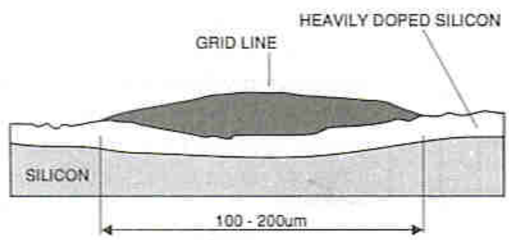


Figure 3: Function of encapsulation layer to reduce reflections from surface of multicrystalline silicon cell.

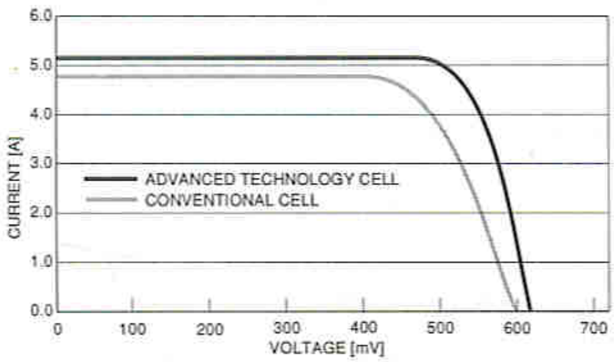
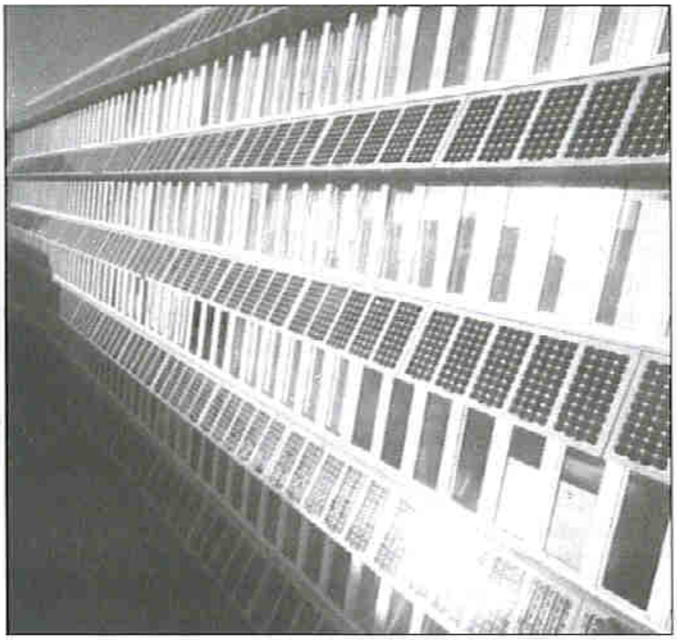


Figure 14: Performance of encapsulated 123 mm cells compared with conventional cells.(Courtesy BP Solar Ltd.)



demonstration sites of its products around the world.

There is also considerable interest in the fabrication of concentrator units operating at typical levels of concentration of between 10 and 20. Since a major cost of the current 'one sun' solar cell is the semiconductor material, to reduce this cost and offset it against additional costs of focusing and possibly sun tracking systems can make good economic sense. BP Solar are currently researching the efficiency of CZ silicon cells with concentrated sunlight. Efficiency in excess of 20% has been achieved at 10 suns concentration and 19.8 % at 19 suns.

While concentrator systems have been extensively researched and developed, current production is relatively

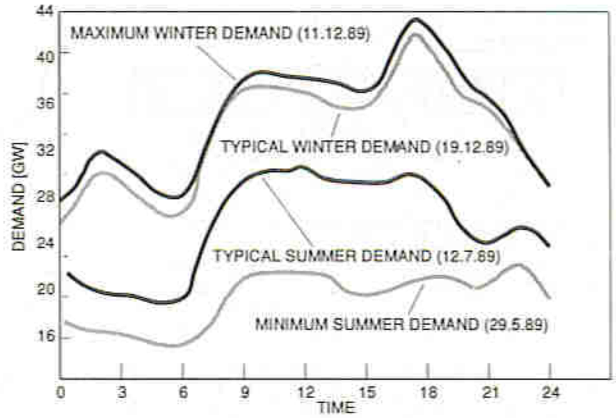


Figure 15: Typical grid power loading, UK - summer and winter.

low - less than 0.5% of total capacity. While such cells are expected to be potentially cheaper in mass production than 'one sun' devices, the lack of uptake of such units can be explained in part by the lag in 'balance of system' components such as sun tracking units. As the 'solar infrastructure' industries develop, however, concentrator systems could rapidly increase in utilisation and ultimately overtake 'one sun' devices. The National Renewable Energy Laboratory at Golden, Colorado, in the USA produced a small area cell made from crystalline gallium indium phosphide/gallium arsenide with a record efficiency of 30.2% at 180 suns concentration.

Solar power in space

Solar cells have been used for a considerable time as a power source for spacecraft and it was indeed the intense development of this technology which has made possible the rapid advances in photovoltaic technology. This is one of the positive spin-offs of the Space Race. The essential requirement for absolute reliability of such sources of power has tended to focus development on providing highly reliable sources of power. Protective coatings of quartz are used to protect the silicon from high energy electrons which are principally found in the earth's radiation belts.

The increased efficiency of solar cells and the experience gained of fabricating large arrays of cells has significantly increased the power now typically provided to satellites. While a capacity of 1.5 kW was considered appreciable several years ago, systems are now routinely launched with peak Watt capacities of 5 kW.

While plans for the Space Station have blown hot and cold - the need for extensive solar cell arrays for the project has long since been appreciated and manufacture of the cells required has been taking place for some years for the project. The estimated 200,000 kW capacity of the space station will be provided by an array of cells each 8cm square. The total area of 1280 square metres is equivalent to an area approximately 36 metres by 36 metres.

The Trans Australia Race

The first Trans-Australian Solar Car Race, the brainchild of Hans Tholstrup, was held in 1987 and has been subsequently held in 1990 and 1993. The rules of the race are relatively simple. Cars can race between 8 am and 5 pm and vehicle sizes can be no larger than would occupy a volume 4 metres by 2 metres by 1.6 metres. Battery

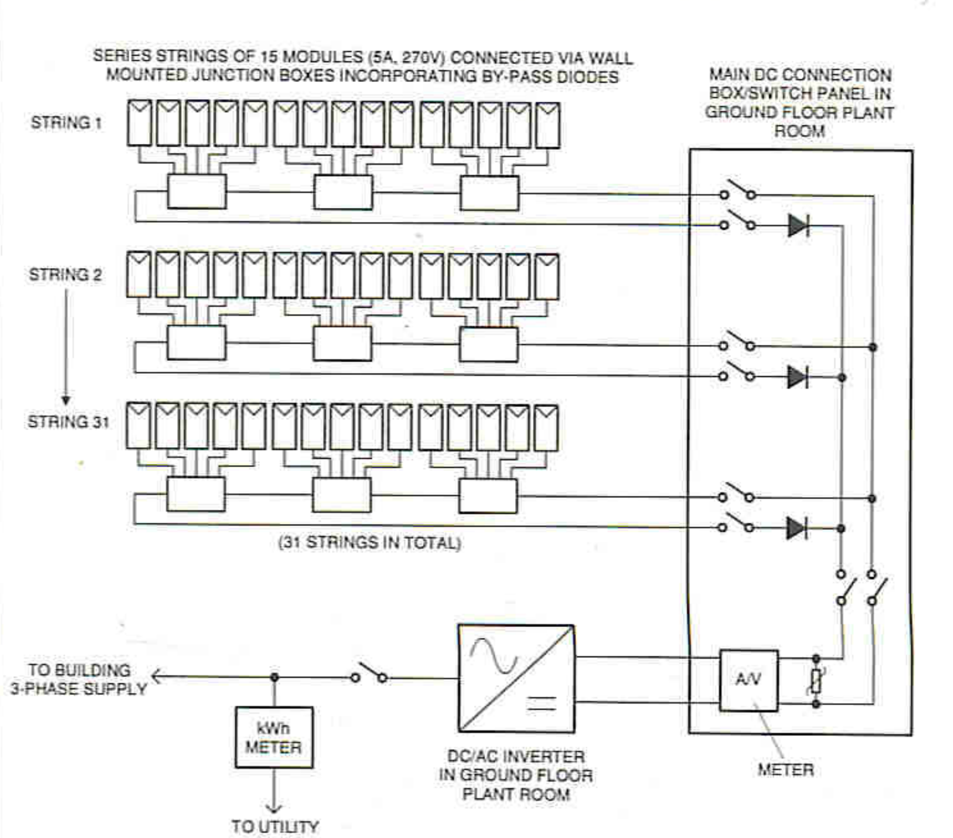


Figure 17: Configuration of the Northumberland Building photovoltaic system. (Courtesy BP Solar Ltd.)

Balance of system costs

While the cost of photovoltaic modules is related to the cost of processing associated with semiconductor fabrication, the cost of grid connected power facilities takes into account a broader range of factors referenced as 'balance of system' costs. In any large-scale photovoltaic system these costs are every bit as important as the cost of the modules themselves.

In terms of photovoltaic installations, the 'balance-of-system' components (BOS) can represent around 50% of a typical photovoltaic system. Such items include tracking systems, foundations, interconnect hardware, batteries and inverters. As the photovoltaic market develops, so increasing attention is being paid to providing more cost-effective BOS components. As production gears up for solar modules, so production costs of associated BOS components will also decrease. As much care, however, is required in the design, manufacture and testing of such BOS units as that of the solar modules in order to ensure total system reliability.

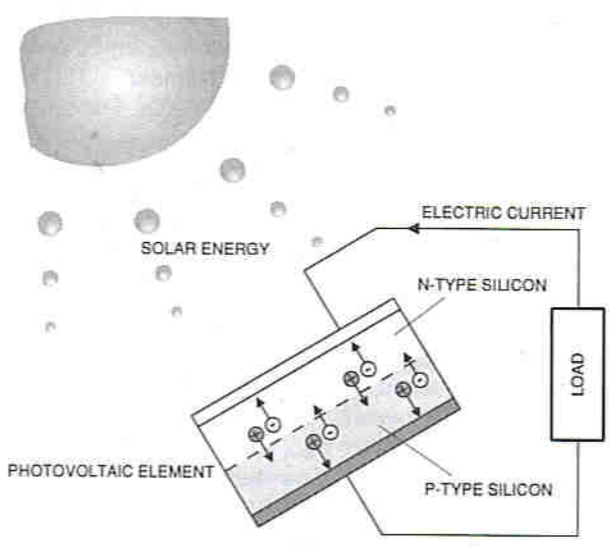


Figure 2a: Function of typical photovoltaic cell. Electrons and positive holes are generated by sunlight. The electron moves to the n-type layer while positive hole flows to p-type layer resulting in potential difference between the two electrodes.

capacity is limited to 5 kWh though there is no cost limit of the solar cells used to power the car. The winning car of the 1993 race, the Honda Dream, averaged 53 mph over the 3,000 kilometre journey between Darwin and Adelaide with the winning team of the 1990 race from the college of Biel University in Switzerland achieving a reputable second place at an average speed of around 49 mph. Efficiencies of the cells varied from 15% to 21% and array power from 950 W to 1600 W. The race is an excellent shop window for demonstrating this dynamic technology.

World trends

Figure 5 indicates the growth of photovoltaics in MW of production by year. The market share of the USA which slipped to less than 30% in the late 1980s has recovered to 36% in 1994. Production is expected to reach 90MW in 1995 and with substantial gains in 1996 as new production facilities for thin film modules come into production and also as various law suits in the USA are resolved.

Figure 6 indicates the projected US manufactured cumulative photovoltaic generating capacity till the year 2000 as detailed from a Department of Energy report. Assuming that US production maintains its current ranking of around one-third of total production, the world's position can be very roughly estimated by multiplying these figures by a factor of three so that the cumulative global capacity will be in the region of 4500 MW by the year 2000. This would indicate that globally around the year 2000 something like 1000 MW of additional capacity will be being added each year.

In 1994 MITI (Ministry of International Trade and Industry) made available a 50% subsidy for the implementation of residential photovoltaic systems in Japan. It was scheduled to include an additional 1500 houses in 1995 in the scheme. Through its agent in Japan, M. Setek Company, BP Solar has been supplying modules for this programme and also to Panasonic's housing company, Panahome. A typical house with 24 modules supplying a total peak level of 1.8 kW is shown in figure 7.

The Japan Quality Assurance Organisation in Tokyo provides accredited testing of photovoltaic materials and is also conducting tests on a range of utility power systems with a total capacity of 112 kW. One approach which the Japanese are investigating is the use of layers of photovoltaic absorbers which are energy-dependent,

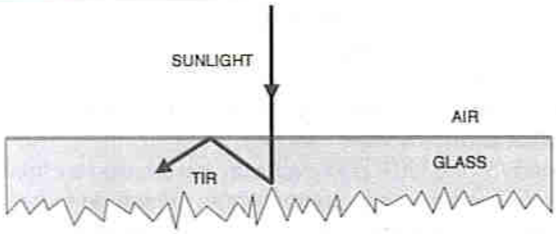


Figure 13a): Conventional metalisation strip used with screen printed solar silicon cells (Courtesy BP Solar Ltd.)

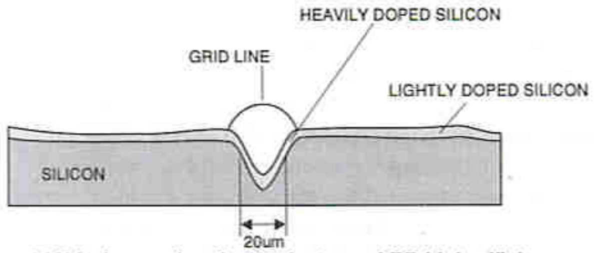


Figure 13b): Innovative design feature of BP high efficiency solar cell showing narrow laser-cut metallisation strip. (Courtesy BP Solar Ltd.)

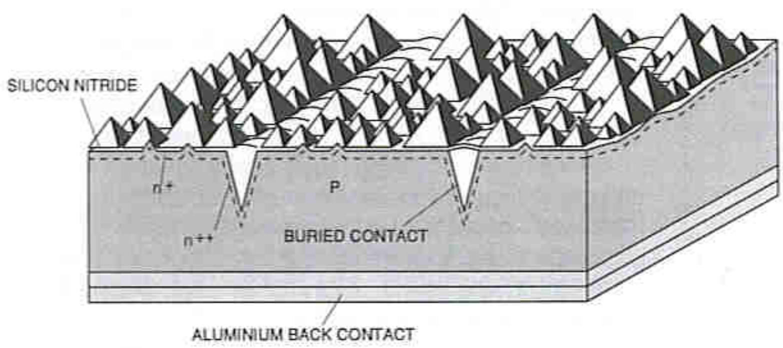


Figure 13c: Cell with Silver Nitride anti-reflection layer. (Courtesy BP Solar Ltd.)

multilayer devices. Japan also supplies systems for mass production of amorphous silicon sheets to other countries. The high value of the Yen, however, is restricting exports of photovoltaic modules and the USA has overtaken Japan as a manufacturer of photovoltaic modules.

In Germany, restructuring among manufacturers has led to a reduction of manufactured capacity. As a global player, however, BP Solar is making a major impact across the world in implementing photovoltaic power. Also, for some years, Intersolar at High Wycombe has met with considerable success in manufacturing and marketing consumer products such are car ventilation systems which are powered using solar cells.

The present key role of photovoltaics is for 'off grid' power production. Even in Norway, around 30,000 summer houses in 'off grid' locations have electric power courtesy of photovoltaics. Around 100,000 houses in Spain also have photovoltaics. In Indonesia, around 35,000 systems are installed with 10,000 coming on stream each year. Many of these are of 100W capacity or less - provided by a panel some four feet by four feet.

A significant level of interest is being shown in photovoltaic systems in Australia. The recent development of a 21.5% efficiency silicon solar cell, led by Martin Green of University of New South Wales, has awakened significant interest is photovoltaics in Australia. This technology has subsequently been licensed to BP Solar Ltd. A major power utility company, Pacific Power, is launching Pacific Solar - an entity designed to develop photovoltaic power in Australia.

USA initiatives

The rapid expansion of worldwide photovoltaic production has also seen the market share of the USA fall from 80% in 1980 to around 30% in 1988 as the USA failed to increase its sales as fast as its competitors. In order to reverse this trend, the US government initiated in 1990 a $100 million Photovoltaic Manufacturing Technology (PVMaT) project. The first set of eight companies receiving funding from PVMaT have been able to reduce module costs from $4.50 per watt to currently around $2.70. It is estimated that costs should further fall to around $1.50 per watt by 1997 as indicated in figure 8. This is a specific example of the price falling with increasing production. Specific companies receiving funding from PVMaT include Astropower Inc., ENTECH Inc and Siemens Solar Industries - the latter company being the world's largest producer of photovoltaic systems.

The involvement of PVMaT has allowed, in particular, Astropower to develop so-called 'Silicon-Film' cells which can be made in a process that takes only 20 to 30 minutes in contrast with conventional silicon crystal technology which takes typically 20 hours. The efficiency of these cells has been logged at 11.8%. Recently, a 19.3 kW installation using the new film technology was completed in Davis, California. Astropower Inc, in common with other photovoltaic suppliers invest in new technologies while also manufacturing conventional crystalline silicon photovoltaic systems.

There is particular interest in using photovoltaics in the commercial environment. Many large commercial buildings in the USA have under-utilised roof tops. In one demonstration installation, AstroPower Inc. supplied the PV modules for a 14.6 kW installation on the roof of a power company. There is particular interest from power companies in reducing the peak demand to customers in order to minimise the generating capacity which is on line and available. One way of achieving this is to allow photovoltaic systems to offset peak demand by direct operation and with supplementary input from battery reserves.

Figure 9 indicates how the array responds with time of

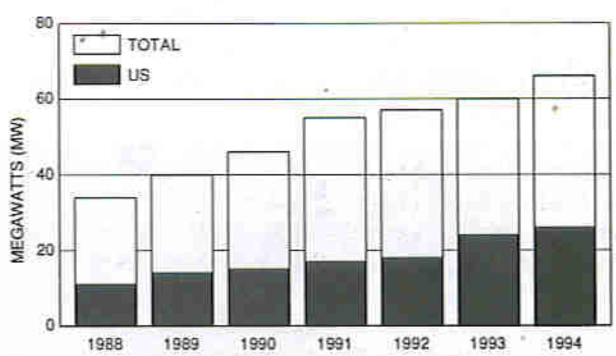


Figure 5: Growth in photovoltaic production (Courtesy US Department of Energy)

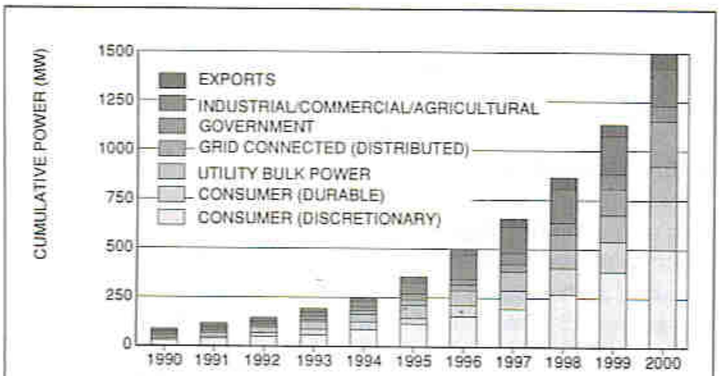


Figure 6: Predicted cumulative capacity of photovoltaics manufactured by the USA. (Courtesy US Department of Energy)

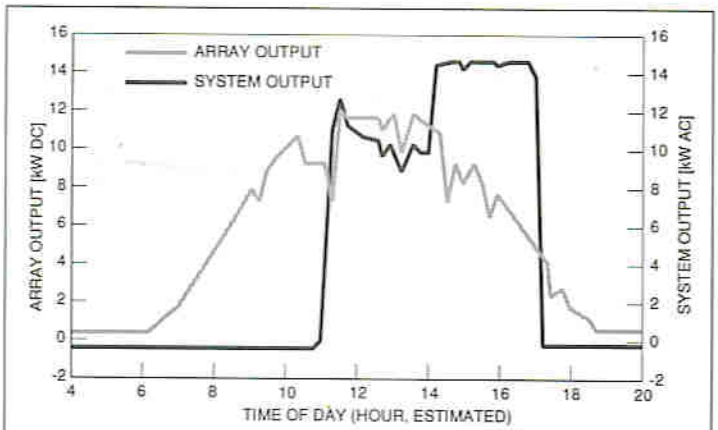


Figure 9: Loading data of a rooftop photovoltaic array. (Courtesy Astropower Inc)

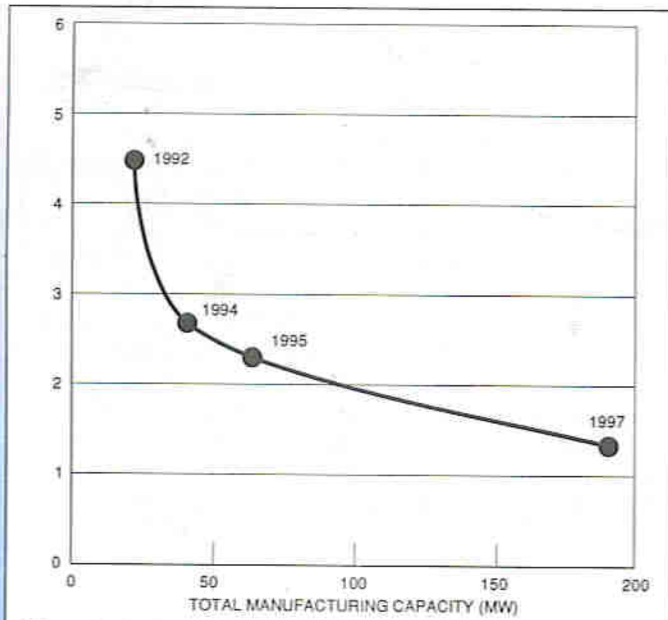


Figure 8: Projected costs of US utility photovoltaic module generation per Watt of capacity. (Courtesy US Department of Energy)

day (solid symbols) and how the system output is controlled to charge the battery till 11.00 , supply directly power from the PV array till 14.00 (float mode) and then operate from the batteries from 14.00 till 17.00 (dispatch mode).

Figure 10 indicates how the cost of a range of commercial photovoltaic installations in the USA has decreased almost linearly with time. There is evidence also of a quickening of cost reduction from an underlying cost reduction of $1 per Watt/peak of system cost per year. Currently, costs are falling below $5 per Watt of capacity. It is anticipated that when costs fall below $3 per Watt then this will, in turn, kick-start the demand for several 1000 MW of additional photovoltaic capacity.

Already in the USA photovoltaics can provide a cheaper option for the powering of street lights compared to the cost of extension of the grid supply. Figure 11 indicates sun power street lights in Albuquerque, New Mexico. In the USA, there is considerable government investment for PV technology. At the Sandia National Laboratories extensive facilities exist for the design, fabrication, testing and calibration of a range of photovoltaic materials and under a range of standard simulated solar conditions.

Telecommunications, oil and gas

Telecommunications is making increasing use of photovoltaics for powering remote installations such as repeater stations. In Peru, for example, Solarex power modules provide power to repeater stations which allows Lima to maintain contact with interior Peruvian communities. Also, Solarex systems powers around 50 remote telecom sites in Thailand. Such systems also power remote cellular emergency call boxes in Arizona. A 400 Watt repeater unit can be typically powered using a 3840 W peak array with four peak watt sun hours and a battery rated at 60 kWh. Systems are also used in fibre optic links, earth stations, cellular phone networks and UHF/UVF transmissions.

Extensive use has been made of photovoltaics for the oil and gas industry for power for remote installations. Significant contracts have been placed for pipeline protection projects where solar powered units minimise corrosion of installations. Figure 12 indicates such a system installed by BP Solar in Pakistan.

Rural infrastructure projects

Immunisation programmes in developing countries depend on availability of refrigeration for vaccine storage. It is estimated, for example, that in 1986, up to 45% of imported vaccines were lost in Honduras due to poor storage. In remote communities, local diesel generators can fail and require maintenance or fuel supplies can be intermittent. A typical solar installation, however, with 180 W peak will power a 4 cubic feet vaccine refrigerator (20 W consumption) with a battery rated at 3 kWh.

While in many communities water has been traditionally been in short supply, problems of expanding populations or changing local climate have tended to increase the problems of obtaining sufficient water for drinking, livestock and irrigation. Today, some 2 billion people - around 30% of the world's population - are facing these problems. Increasingly, use is being made of underground aquifiers to meet demands. Photovoltaics are proving of considerable use in implementing reliable pumping systems where there is no grid supply of electricity or where diesel pumps are unreliable due to mechanical failure or lack of fuel. A typical 480 W peak array is able to pump in excess of 1000 gallons from a depth of 100 feet. No battery backup is usually required for such installations since the water requirements are typically met by the system's operation during daylight hours.

South Africa is set to rapidly increase the number of photovoltaic systems at present in use. Approximately 20% of South Africa's population will remain unconnected to ESKOM - South Africa's national electrical utility for the

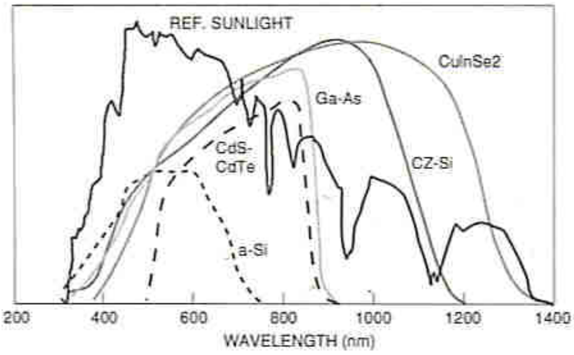


Figure 2b) Spectral irradience of reference sunlight and spectral response of some typical solar cells. Few cells have an adequate response in the region between 400 nm and 600 nm while that of amorphous silicon (a-Si) cuts off at around 700 nm. (Courtesy Japan Quality Assurance Organisation)

foreseeable future. The SAFIRE (South African Financing and Implementation for Renewable Energy) programme will play a key role in providing photovoltaic systems for a wide range of uses.

Flying the flag : BP Solar and Intersolar

BP Solar, a wholly owned company of BP International, has rapidly achieved a major increase in global market - being now among the top three global producers of photovoltaic modules. Certainly in Europe, BP Solar is the major manufacturer with its chief manufacturing facility in Spain. BP Solar manufacturers a set of high efficiency silicon cell panels. In conventional screen printed metal contact lines, the width of the line is typically around 100 and 200 microns. This takes up around 10% of the area of the surface of the cell. By making use of a laser to cut the metalisation grid to around 20 microns wide, less area of silicon is obscured and efficiency is correspondingly increased.

Figures 13a indicates the size of conventional metalisation strip while figure 13b indicates the key laser groove feature of the BP Solar high efficiency cells. Also plating the grooves by copper lowers the resistivity of the cells which ,in turn, boosts efficiency. Figure 13c indicates the use of a layer of silicon nitride on the surface to reduce reflections. While conventional screen printed monocrystalline solar cells have efficiencies in the range 11 to 15%, BP Solar cells have efficiencies in the range 16 to 18%. Figure 14 indicates the performance of encapsulated 123mm cells compared with conventional cells. BP Solar is also extensively researching thin film and concentrator cell technology.

The 'building block' modules provided by BP Solar are listed in table 2.

		BP585	BP275	BP255	Typical Peak
Power (Pmax)		85.00	75.00	55.00	
Maximum voltage (V)		18.00	17.00	17.00	
Maximum current (A)		4.72	4.45	3.23	
Length	(m)	1.18	1.18	1.04	
Width(m)		0.53	0.53	0.45	
Depth	(m)	0.038	0.038	0.0385	
Weight	(kg)	7.5	7.5	5.9	
No Cells		36	36	36	

Table 2: Characteristics of current BP Solar modules

A recent landmark development for BP Solar has been the installation of a 1 MW grid connected facility in Spain.

Intersolar of High Wycombe in the UK is the sole manufacturer of solar cells in the UK. Production utilises thin film techniques to produce a wide range of products with emphasis on products which use photovoltaic power as a key part of their function. Specific products include solar-powered car ventilator units and flashing safety lights. Also, a range of sample modules ranging in peak power output from 1.2 W to 30 mW are available for incorporation into prototype consumer product designs. Intersolar also provide technical advice in the use of their solar modules with consumer products.

Photovoltaics and Buildings

A recent Department of Trade and Industry report - 'The Potential for Building - Integrated Photovoltaic Systems' has reviewed the potential for deriving power from photovoltaic systems attached to building walls and mounted on roof spaces. The general consensus of opinion in the report was that photovoltaic cladding of new buildings will be competitive by around 2005. In assessing the various types of building considered, such schemes are most attractive where the additional photovoltaic power meets the rising demand in commerce and industry as indicated in figure 15. In summer there is a typical increase in demand of 12 GW from 6 o'clock to noon. In winter, this similar step is present and, in addition ,a further 6 GW increment takes place in later afternoon. The concept of photovoltaics meeting this additional demand is certainly being considered seriously.

In the domestic situation, however, there is a greater

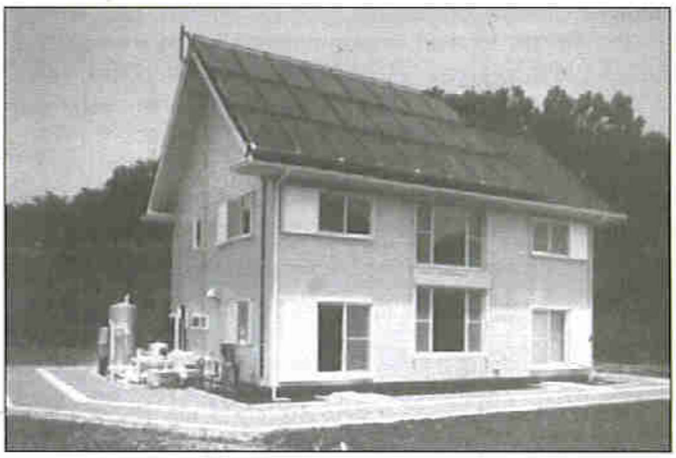


Figure 7: A Japanese house fitted with 1.8 kW of peak solar capacity by BP Solar as part of the New Sunshine Project. (Courtesy BP Solar Ltd.)

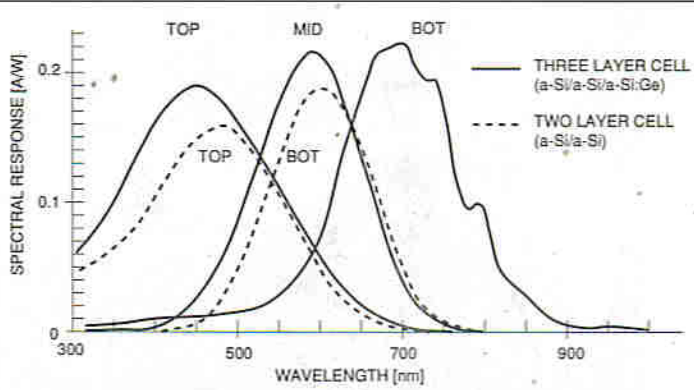
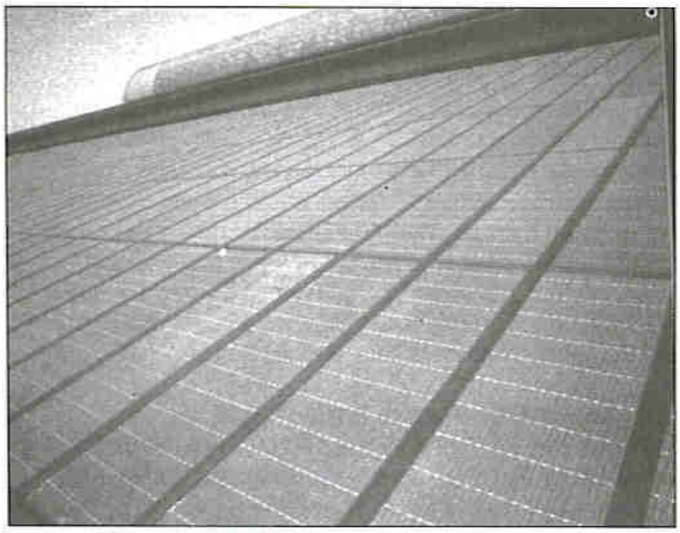


Figure 2c) Concept of multistage solar cells where layers in the solar cell have a separate response to try to maximise sensitivity. (Courtesy Japan Quality Assurance Organisation)



mismatch between the solar supply of electricity and demand. There would be extensive periods where there was an excess of supply and periods where there was a deficit of supply. In this situation, systems could be made to export power to the grid and receive it back as appropriate. At present the Non-Fossil Fuel Obligation (NFFO) does not recognise PV technology and the Regional Electricity companies are not obliged to purchase power from the independent owners of PV systems.

The rear roof of the house of Dr. Susan Roaf, lecturer at Oxford Brookes University School of Architecture, incorporates 48 of BP Solar's high power solar modules to provide about 4kW of peak electricity which is converted from DC to AC via an inverter. It is anticipated that the house should export around 1000 kWhrs of surplus energy.

The models for such implementation for commercial building to incorporate PV technology remain 'conservative' in determining when PV technology will become cost-effective. With costs of PV modules falling in recent years by 20% per year there is on the one hand an anticipated model of cost projections with also the potential of a more rapid realisation of the technology accelerating the drive for PV cladding of buildings. In terms of building design, therefore, the 21st century will be the first century where PV technology forces a re-evaluation of building design and fabrication. It does not take much imagination, however, to anticipate the potential world market for customised style PV cladding panels.

The Northumberland Building

A key development in the UK has been the grid integrated 40 kW system at the University of Northumbria in Newcastle-uponTyne.The system configuration is shown in figure 16 and the frontage of the building in figure 17. Based on the BP Solar Saturn cell of 85W rating, 31 strings of 15 such modules in parallel can either be connected to the utility grid or the to the building 3-phase supply. The array size of 290 m2 gives an array rating of 39.5 kW peak.

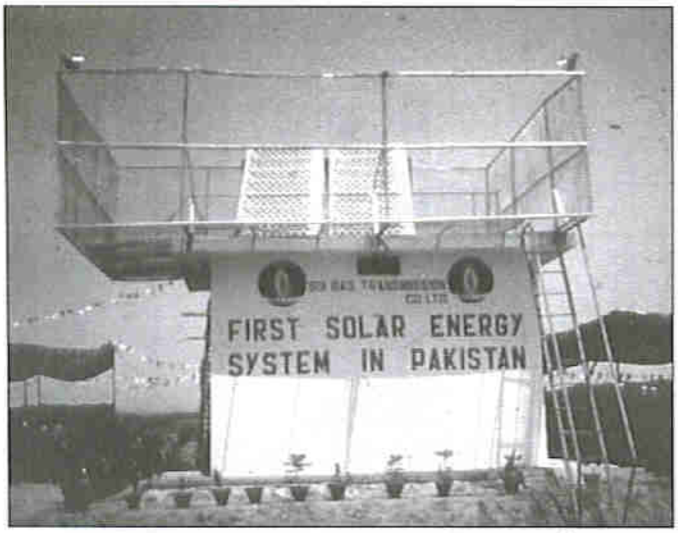
The power output of the system is being extensively studied to assess the implementation of this type of technology. It is anticipated that the buildData obtained also indicates that recovered power is relatively uniform between March and September. This is in part due to the loss of efficiency in mid summer due to the angle of incidence of the sun on the panels.

This project is being designed as the marker for future developments to allow building structures, even in the UK, to generate significant amounts of electricity. The systems as described has no facility to store energy. Such systems could have a key role in reducing peak electricity demand and hence reducing the number of power stations that utility companies require to maintain on-line to meet demand. There would also be a welcome reduction in carbon dioxide emissions.

A star is born

Solar photovoltaic power is now regarded by many observers as a key energy source for the 21st century and beyond. This is coming at a time where the future of nuclear power systems is increasingly coming under critical

Figure 4: 'Roof tile' structures of amorphous silicon designed to be environmentally acceptable. (Courtesy Uni-Solar Systems Inc.)



examination due in part to the huge cost of decommissioning such systems and the unsolved problem of production and storage of nuclear waste. The collapse of the oil price in the late 1980s, however, has merely acted to postpone the date at which power from the sun will begin to eclipse the power and influence of fossil fuel energy producers.

The developments that have undertaken in solar cell technology, however, have been achieved largely by 'sideline' funding when compared to the massive defence and space budgets and also the budgets presently allocated to fusion research. This has also tended to delay the cross-over into solar technology. It is therefore a tribute to all those who have developed photovoltaic technology that they have realised that the prize of cheap and safe power was achievable and that the rhetoric of compromised energy monopolies would one day fall curiously silent as they begin to take solar photovoltaic power seriously.

The immense challenge of photovoltaic power is a global one and therefore one which must be at the core of interests of UK research and manufacturing.

The world of solar energy, however, may bring to light some strange paradoxes. In a decade where, in the UK, house prices are at a lower value than five years previously, there is more than certain scope for Building Societies and Power Utilities to combine their respective finance and business skills and initiate a Sunshine UK initiative for UK home owners. As a catchphrase, they could always use - 'Bring a little sunshine into your life'.

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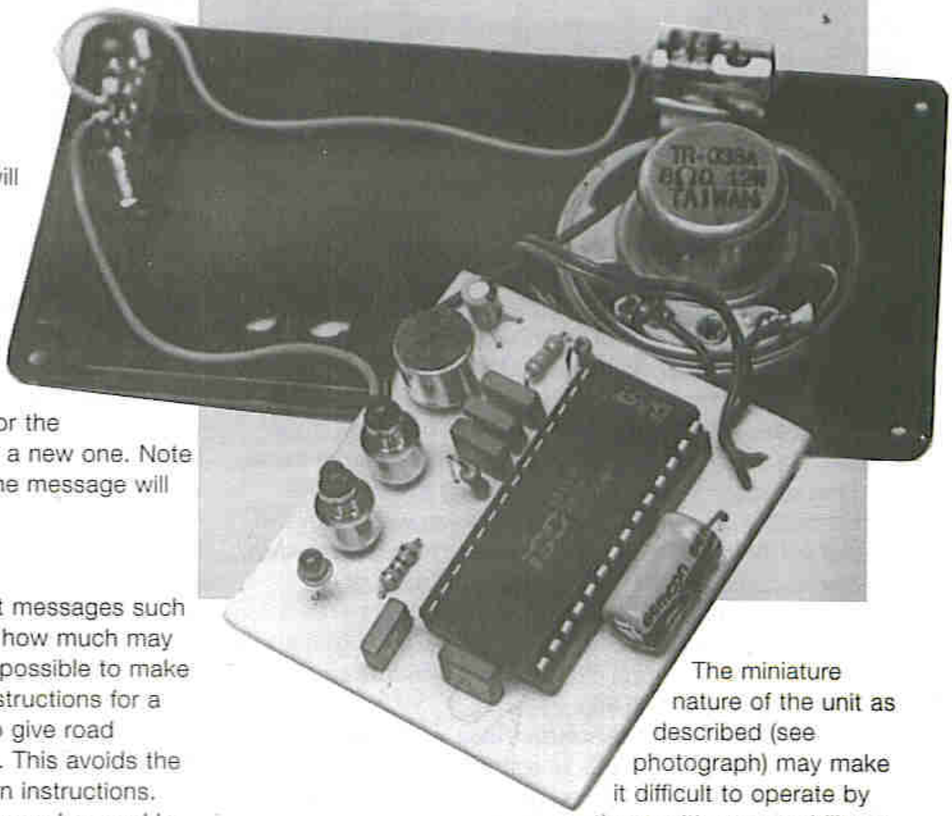
Figure 11: Use of solar photovoltaic systems for street lighting in Albuquerque, New Mexico. (Courtesy US Department of Energy)

sweet-TALK

A handy ten-second voice recorder designed by Terry Balbirnie



This miniature sound recorder will store up to ten seconds of speech and play it back through an internal speaker any time afterwards. The message may be repeated as often as needed simply by pressing a button. New items may be recorded with the previous one being erased automatically or the recording may be cleared without making a new one. Note that even when the unit is switched off, the message will be retained for as long as required.

Help!

Sweet Talk will be useful for leaving short messages such as "dinner is in the oven!". It is surprising how much may be said in ten seconds - try it! It is quite possible to make a brief shopping list or provide spoken instructions for a recipe. The prototype was found useful to give road numbers or directions when driving alone. This avoids the danger of having to look at a set of written instructions. Placed over the telephone mouthpiece, it may be used by the elderly to give instructions or to summon help using a pre-recorded message. The blind would find it useful as a "memo pad". Note that the recording will have a slight background buzzing noise. For these and similar purposes, this will not matter. For more critical uses, it may be obtrusive.

This unit differs from a conventional dictating machine because it is totally electronic - there are no moving parts. There is no cassette to wear out or stick, no heads to clean or tape to rewind. It is also robust and extremely easy to use. The current requirement is much less than a cassette recorder - about 20mA when recording and 30mA when playing back. A small battery will therefore provide good service. The standby current consumption is only 150mA approximately so if the user forgets to switch off occasionally, the battery will still last for a long time.

Absent what?

Sweet-Talk is built in a plastic case with an on-off slide switch and two push-buttons on top - one (red) to initiate recording and the other (black) to play it back. There is also an LED to confirm that recording is in progress.

The miniature nature of the unit as described (see photograph) may make it difficult to operate by those with poor mobility or unsteady hands. In such cases, it would be a simple matter to use a larger box and fit bigger click-type switches. Also, a higher-capacity battery could be used which would provide a longer life if the unit was used often or left switched on for long periods. For the absent-minded, four "AA" alkaline cells could be used as the power supply. It would then be possible to omit the on-off switch. These batteries would last for about a year depending on how often the recorder was used.

Happy memory

The principle component is a 28-pin sound recorder chip. This is an unusual device in that its method of storage is analogue. It may be regarded as a hybrid circuit where the memory is analogue by nature while it is written to and read from digitally. Built on the chip is an array of 64,000 non-volatile EEPROM memory cells, a 6.4kHz oscillator, filtering circuitry, microphone pre-amplifier and a low-power speaker output stage.

While the record button is pressed, the incoming sound is picked up by a microphone and the resulting electrical signal boosted by the on-chip pre-amplifier. An AGC

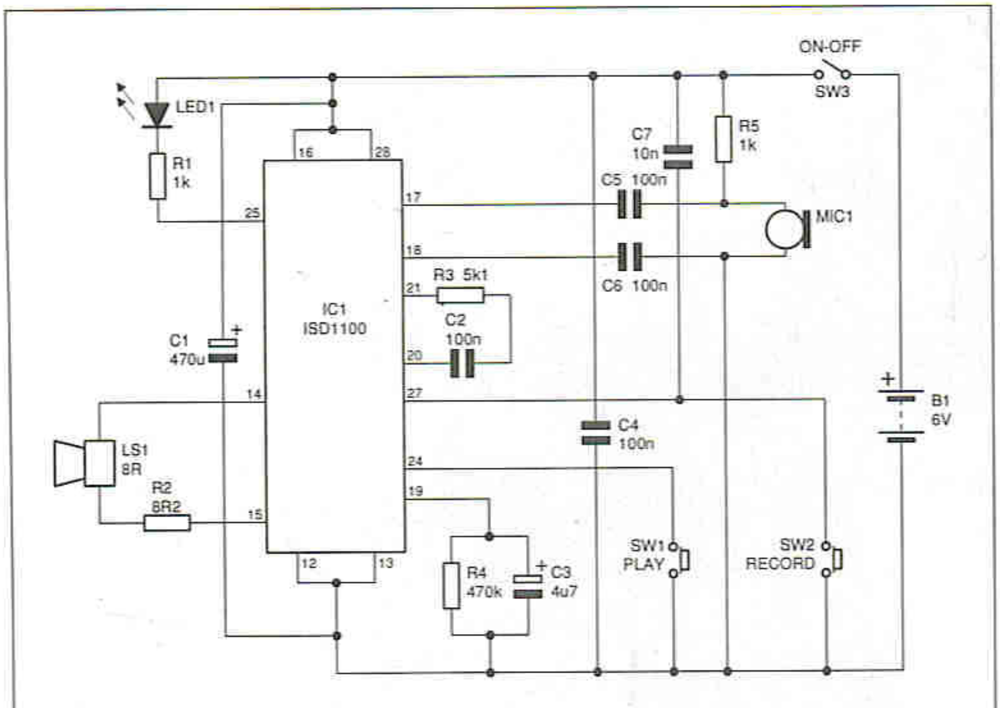


Fig 1. Sweet talk Circuit

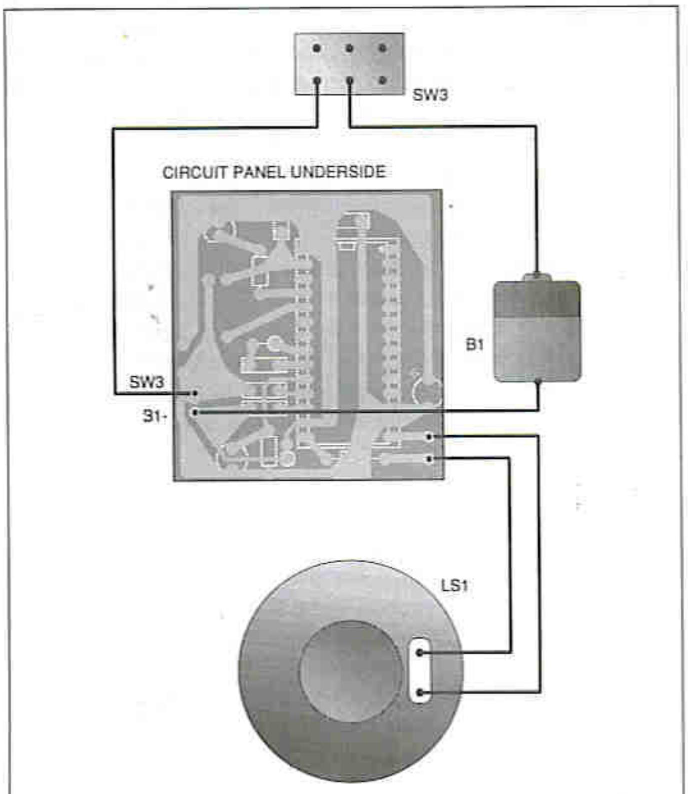


Fig 3. Wiring Diagram

(automatic gain control) circuit provides a compression effect so that loud sounds are amplified less than quiet ones. Thus, sounds having a wide range of volume levels will be recorded correctly and without distortion. The result is sampled at clock frequency and, on each pulse, the amplitude of the wave is stored in successive memory locations. There is no digital conversion - points on the wave are stored directly as voltage levels. Since there are 64,000 memory cells, and because sampling takes place 6,400 times each second, there is a maximum recording time of ten seconds.

When the play button is pressed, the contents of the memory cells are read in the same order as when the recording was made and the information retrieved. The result is boosted by the power amplifier which operates the speaker. At the end of playback, the device reverts to standby mode (ready to read from the beginning of memory) so that replay begins instantly when the play button is pressed again. Note that, if the full available time is not used, a marker is inserted in memory at the end of the recording. On playback, the chip will revert to standby mode when it reaches the marker. When making a recording, the LED will go off when the memory is full. The process then stops and any sound made after that is ignored.

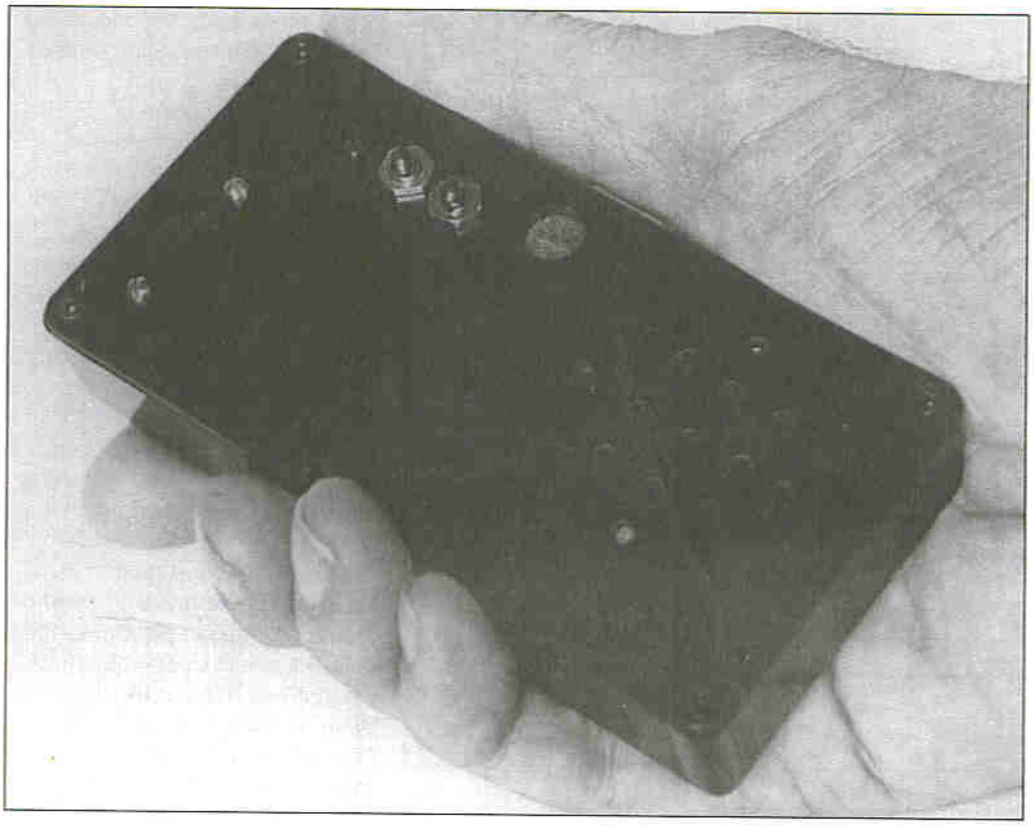
Circuit description

Fig. 1 shows the complete circuit for Sweet Talk. In fact, much of it is fabricated within IC1 and this makes construction very straightforward. The power supply consists of a 6V battery, B1. It is important not to use a higher voltage than this - the maximum permitted value for IC1 is 7V.

IC1 pins 1 to 11 inclusive and pins 22, 23 and 26 are unconnected. Pins 12 and 13 are the earth (supply negative) connections for the digital and analogue sections respectively, while pins 28 and 16 are the corresponding positive battery feeds. Pins 14 and 15 are the power amplifier output. Note that this is designed to drive a 16 ohm speaker. It seems, however, that small units having this impedance are not listed. It is therefore necessary to use a standard 8 ohm speaker with the 8.2 ohm fixed resistor, R2, connected in series with it as shown. The audio output will be reduced since some power is wasted in the resistor. Even so, it will be sufficiently loud for the purpose.

Pins 17 and 18 are the inputs to the pre-amplifier. These are fed via capacitors C5 and C6 from electret microphone insert, MIC1. This needs a power supply of its own to operate an internal FET amplifier which boosts the signal sufficiently to operate the on-chip pre-amplifier. This supply is obtained from the 6V supply line through resistor, R5. With SW2 pressed, pin 27 is made low and this enables recording. At the same time, pin 25 goes low and operates light-emitting diode indicator, LED1, through current-limiting resistor, R1. Capacitor C7 keeps pin 27 high at the instant of switching on. Without this, a marker would be inserted and previously-recorded material would be erased. Resistor R4 and capacitor C3 connected in parallel to pin 19 set the characteristics of the AGC circuit referred to earlier.

With SW1 pressed momentarily, pin 24 is made low and this begins the playback cycle. Pins 20 and 21 (analogue in



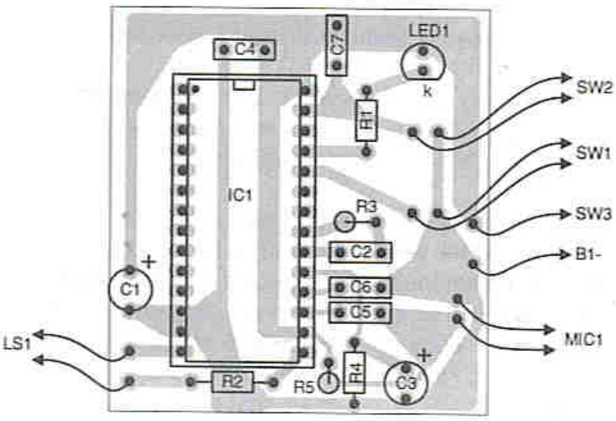


Fig 2. PCB component overlay

and analogue out) are coupled together using resistor R3 and capacitor C2 connected in series as shown.

Construction

The printed circuit board (PCB) component overlay for the sound recorder is shown in Fig. 2. Solder the i.c. socket in place. Do not solder the i.c. direct to the board. Follow with all resistors and capacitors (except C1), the push-button switches SW1/SW2 and the LED. Note that the red (record) switch, SW2, is the one nearest the LED. The LED should be mounted so that its tip stands 10mm above the PCB. Bend C1 end leads at right-angles and solder them to the pads so that its body lies flat with the PCB (see photograph). Take care that the leads do not touch and cause a short-circuit - insulate them with sleeving if necessary. Note that this capacitor, together with capacitor C3 and the LED, are polarity-sensitive so take care to observe the correct orientation.

Solder the microphone in position. If this has pad connections rather than pins, it will be necessary to solder pieces of single-strand wire to them so that they may be passed through the holes in the PCB and soldered in place. Look first at the underside of the microphone and it will be seen that one of the pins or pads is connected to the case. This one should be soldered to the PCB pad leading to capacitor C6. Solder short pieces of light-duty stranded wire to the points labelled "LS1", "SW3" and "B1-". If off-board push-button switches are to be used, solder pieces of wire to SW1 and SW2 pads. A single hole will then be used to secure the circuit panel in the case. A suitable position to drill it would be in the free area around the original SW1/SW2 position.

The circuit panel is attached to the lid of the case using the push-button switch fixings and needs no further support. Carefully measure the position of these switches, LED and microphone then drill holes in the lid to correspond with them. A single hole of 10mm diameter should be made for the sound to pass to the microphone. The holes for the push-button switches should each have a diameter of 5mm so that their bodies may be passed through and secured using the nuts on the outside. The LED hole should be of 3mm diameter. Make the hole for the on-off switch and a matrix of holes for the sound to pass through from the speaker. Make small clips as necessary to hold the battery in position and to make the connections to its terminals. Any 6V battery may be used, providing it fits inside the case. For heavy duty use, one with the highest possible capacity should be used. In the prototype, the wires were soldered direct to the battery terminals and it was attached to the lid using an adhesive fixing pad. The use of small clips, however, would allow it to be more easily replaced. Take care that no short-circuits are formed at the battery connections.

Secure the push-button switches, thereby attaching the PCB. Adjust the LED leads as necessary so that the tip rests in its hole but does not protrude through it. Attach the speaker using a little quick-setting epoxy resin adhesive around the rim. Refer to Fig. 3 and complete the wiring to the speaker, on-off switch and battery. If off-board record and play switches are used, connect them to the wires already soldered to the PCB. Note that everything is attached to the lid so that this may be removed to replace the battery without imposing any strain on connecting wires. Assemble the enclosure, checking for trapped wires and short circuits.

Testing

Testing is simply a matter of checking for correct operation and finding the best technique for making a recording.

Press the record button and hold it down. Check that the LED lights and make a test recording. Speak normally at a distance of about 2" (5cm) to begin with. When making a real recording, begin speaking immediately after pressing the record button. If you hesitate, this time uses memory and effectively reduces the actual recording period. Note that the LED goes off after 10 seconds as a reminder that the memory is full. After recording, release the record button and press play momentarily. The sound should be heard clearly. The LED will flash briefly at the end of the playback cycle. To erase a recording without making a new one, simply press the record button for an instant.

Good recordings may be made until the supply voltage falls below 4V approximately. When the recorder fails to work properly (the sound breaking up, whistles and distortion), the battery should be replaced.

PARTS LIST

PARTS LIST

Resistors

R1, R5 1k
R2 8R2
R3 5k1
R4 470k

All 0.25W 5% carbon film.

Capacitors

C1 470m 16V PCB elect
C2, C4, C5, C6 100n metallised polyester - 5mm pin spacing
C3 4m7 35V PCB electrolytic
C7 10n metallised polyester - 5mm pin spacing

Semiconductors

LED1 3mm red LED
IC1 ISD 1110P sound recorder

Miscellaneous

MIC1 Miniature electret microphone 2-pin type. 10mm diameter approximately, with pin (preferably) or pad connections
SW1, SW2 Sub-miniature push-to-make switches 7mm diameter - one red, one black.
SW3 Miniature slide switch
B1 6V battery type GP11A, GP476A, etc. See text.
LS1 35mm diameter 8 ohm speaker
28-pin DIL socket
PCB materials
Stranded connecting wire
Plastic box, size 111 x 57 x 22mm

Buylines

It is better for the microphone to have pins rather than pad connections. These are not stocked by most suppliers. The alternative is to buy one with pad connections and solder short wires to these as described in the text. The sound recording chip is stocked by Maplin (order code KU92A). Other components are freely available.

a PIC Programmer

R.Grodzik shows how to build a simple two-chip PIC microcontroller programmer

The Microchip PIC has opened up a new era in micro-electronics. Conventional microprocessor technology utilising such processors as the 6502,Z80,8080,8088,6800 etc required the provision of external ROM and RAM and support peripherals. Associated with each processor was a formidable instruction set, detailing the operation of each opcode, in some cases covering several pages.The PIC has on-board ROM/EPROM,IO and timers. Its reduced instruction set comprises 32 instructions which surprisingly allow any logic algorithm to be created with a minimum of effort.

The smallest of the PIC family, the PIC16C54, is an 18 pin 0.3" DIL i.c. and could easily be mistaken for a standard TTL i.c. package. But that it is not. It is a very powerful 12 bit processor capable of clock speeds to 20 Mhz, providing an execution time of 200 nanoseconds/instruction (400 ns for conditional branch instructions). If that is not enough, a dozen bit addressable I/0 port lines are provided. These can supply enough current to light a heavy LED.

Internal ROM/EPROM memory capacity is 512 words (12 bit) with an additional 32 bytes of RAM registers serving as general purpose 'file' working registers and as scratch pads. In common with microprocessors, a flag register keeps track of results of operations and a watchdog timer will reset a program if a 'crash' is imminent. Finally, the current consumption of the PIC is a couple of milliamps, a matter of nanoamps in sleep mode, ideal for battery operation.

Project development

Development tools for embedded controllers can be very sophisticated and in the case of I.C.E. (in circuit emulators) can cost several thousand pounds. However there is a simpler and cheaper way. Here's how. The PIC16C54JW ceramic packaged PIG contains EPROM and a quartz window which allows the erasure of the EPROM contents by exposure to U.V. light just like conventional EPROMS. This device is very robust and the author has repeated the programming/erasure cycle literally hundreds of times.

Once a definitive version of the software has been developed, the code can then be programmed into an O.T.P (one time programmable) and much cheaper PIC. So how is the program developed? It's impossible to use conventional techniques such as an EPROM emulator.The answer is to use the MPSIM simulator which runs on any P.C. Single stepping of the program in the simulator allows the user to examine register contents at each instruction; external logic changes on the I/O pins can be simulated in single step and run mode. Here as a few examples of the commands available to the MPSIM simulator:

```
SE RB0 RB:0          ;Change logic level on
input pin
DK 1,RA3,T           ;Pressing ALT + F1 keys
                     will toggle the
                     ;RA3 pin
                     ,in RUN mode
SC                   1    ,Set clock cycle time
                     to 1 microsecond
                     ;i.e. 4 Mhz clock
B4                   ,'break'stop at address 4
RS                   ,Reset to start of program
ZT                   ,Zero the elapsed time
                     counter
                     ,Delays can be accurately
                     measured
$5                   ,Enter single step mode
E                    ,Execute program
F2                   ,Modify program counters
                     contents
```

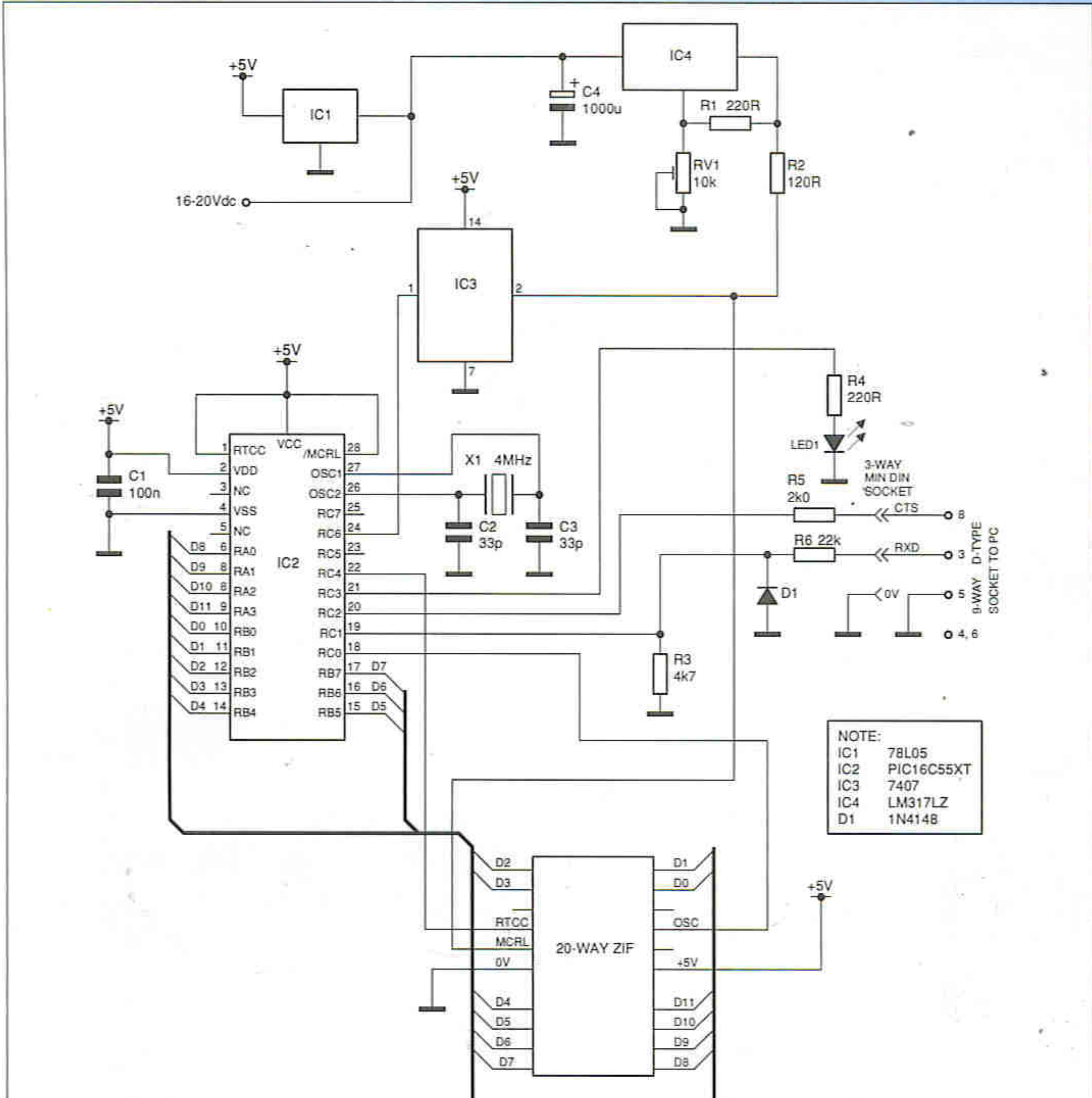
When the software has been successfully simulated, the next step is to burn the PIC. Use the EPROM version for program development since it is very rare the first attempt of the software will produce 100% operational and functional confidence. It happened to the author once, several years ago, but then again the total software overhead was approximately 70 bytes and this had been single-stepped under DEBUG.

The PIC programmer described here programs the PIC in a fraction of a second. Connect the PC's serial port to the programmer and send the object code using any PC terminal emulator which has a hardware CTS/RTS handshake capability. The MPALC assembler provided free on the user disc (together with the MPSIM simulator) produces object code which the programmer will recognize. Use the following assembler directives (File PASM.BAT)

```
MPALC %1.ASM /f picice/t 8/p 16C54
```

This will generate an object file (FILENAME.OBJ) consisting of 1024 bytes. These bytes are arranged as LSB (XXH) and MSB (0XH) thus forming 512 12 bit words which is the capacity f the PIC16C54. Part of a typical hexdump is shown below:

0000: 00 00 00 09 40 0c 2c 00 20 0c 2d 00 25 07 55 00
0010: 07 0a 05 04 08 0c 2b 00 29 09 6a 00 03 04 2a 03



PIC Programmer Circuit

```
0020: 25 06 ea 05 23 09 eb 02 0e 0a  ff  0c 8a 01 26 00
0030: 45 05 23 09 45 04 ec 01 07 0a 40 0c 2c 00 ed 02
0040: 07 0a 05 08 03 0a 20 0c 29 00 e9 02 25 0a 04 00
0050: 00 08 30 0c 29 00 e9 02 2b 0a 04 00 00 08 02 0c
0060: 05 00 00 0E 06 00  ff  0c 26 00 45 04 05 05 65 05
0070: 0c 08  ff  0f  ff  0f  ff  0f  ff  0f  ff  0f  ff  0f  ff  0f
0080:  ff  0f  ff  0f  ff  0f  ff  0f  ff  0f  ff  0f  ff  0f  ff  0f
0090:  ff  0f  ff  0f  ff  0f  ff  0f  ff  0f  ff  0f  ff  0f  ff  0f
00A0:  ff  0f  ff  0f  ff  0f  ff  0f  ff  0f  ff  0f  ff  0f  ff  0f
```

Note that the most significant nibble of the most significant byte is always 0 i.e. 0XXXH = one 12 bit word, and that the INTEL HEX format is not used. To invoke the assembler, type PASM TRY 'ENTER','TRY.ASM' being the ASCII text source code of the program to be assembled.The MPASM cross assembler will not produce romable object code.

Programming

The EPROM version of the PIC (I6GS4JW/P) can be configured for any clock oscillator - RC or crystal, whereas the OTP device has to be selected when purchasing for a particular clock source. PICs with the suffix 'A' are now available allowing the configuration of the 'clock' fuse to take place at the programming stage.

Apply power to the programmer and invoke the PC's terminal emulator ensuring that the CTS/RTS handshake facility has been engaged.

Selection of PIC programming fuse is by entering a number or letter on the keyboard followed by 'ENTER'. Note not to select P 'Protect' initially, since this will lock the PIC and render it unprogrammable.

SELECTION FUSE FUNCTION PIG TYPE AND CLOCK

0	FDH	BURN XT	U.V. ERASABLE IOOKKZ-4MHZ XTAL
1	FFH	BURN RC	U.V. ERASABLE DC-100KHZ
2	FEH	BURN HS	U.V. EAASABLE 4-20MHZ
3	FCH	BURN LP	U.V. ERASABLE 32KHZ-200KHZ XTAL
A or a	FFH	BURN OTP	ALL OTP DEVICES
P or p	F7H	PROTECT	ALL DEVICES
W or w	FBH	WDT	DISABLE WATCHDOG TIMER

It can be seen that the U.V. erasable cerdip PIC (JW/P) can be configured for any oscillator (R-C or Crystal), whereas the OTP (one time programmable) PIC device has to be selected for a particular frequency source. All PICs can have their ROM contents protected by selecting option P/p AT THE COMPLETION OF PROGRAMMING. Note that for all selections, the watchdog timer is enabled. To disable select W/w.

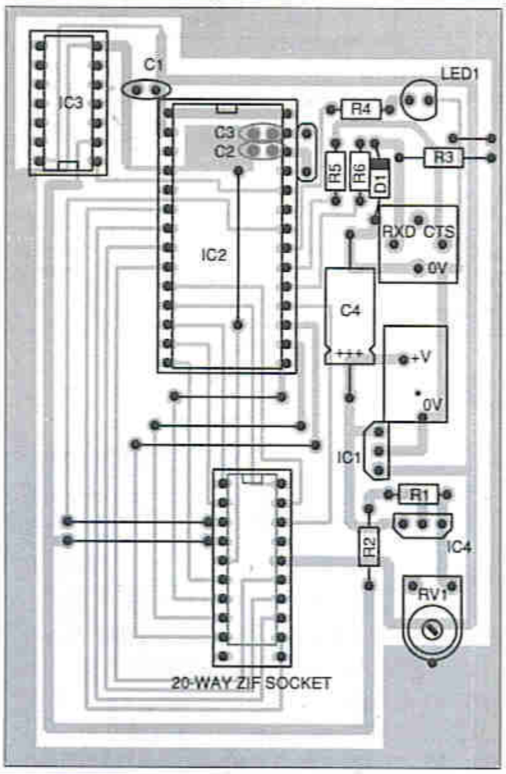
Once the configuration fuse has been selected,download the object file to the programmer. Ensure that the file size is 1024 (400H) bytes: (Filename.OBJ).

A pre-programmed PIC (type PIC16GSS) is available from the author:

Mr.R.Grodzik (MICROS), 53 Chelmsford Road, Bradford BD3 8QN U.K.

Price £30.OO P&P inc.

Includes free disc containing DOS printable PCB file,Program examples,MPALC,MPASM.



PCB overlay

Features:
()Serial RS232 9600 baud input ()Minimal chip count (2)
()16-20v d.c. power supply
()Uses any terminal emulator with CTS/RTS handshake

DIGITAL thermometers

Graham Reith takes a look at how to build, calibrate and use digital temperature sensors

There are many different ways of telling temperature. The first natural thermometer we ever use is the human skin, a life-saving organ with considerable sensitivity to changes in ambient temperature. However, we quickly learn that the skin, like any other thermometer, has a limited range of quite specific uses and limitations.

In the kitchen, for example, we need a thermometer with two particular characteristics which the skin does not have - we need safety and accuracy; a finger is not much use when trying to find the setting point of a pot of boiling jam. For that sort of purpose, we are better to use a tube of tough glass marked off in degrees containing some appropriate material such as mercury.

For some other purposes, a scale on a tube may be too awkward, and we may need the information to be given to us in a different way. A dial thermometer can be constructed using a spiral of two metals with different co-efficients of expandability to wind and unwind, turning a needle to show higher and lower temperatures with considerable accuracy. Meteorologists used to use thermographs, which depended upon the curvature of a flexible filled tube, bending or straightening according to the expansion of a liquid.

All these traditional thermometers share the twin disadvantages of being slow to react to changes in temperature, and of presenting the information in a way which is slow - and, in some cases, like a clinical thermometer, downright difficult to read. Electronics can provide a better answer with a simple system using a fast-reacting probe which produces a digital reading in whatever scale (Centigrade, Fahrenheit, Kelvin or whatever) is desired.

In this article I shall discuss one particular type of such a digital thermometer. This example has been designed so that it can be used indoors to measure the temperature outside. The problem with the human skin, or with mercury and alcohol thermometers, is that you have actually to go outside to find out what temperature it is. On a pleasant summer day, this may not seem too much of a problem, but trudging out in winter to find out exactly how cold it is is not much fun.

This thermometer allows you to do this within the comfort of your own home. What is more, it is not particularly difficult to construct and, for the more adventurous, there is some challenging calibration which, while not essential, results a much more accurate product. For standard convenience, it has been designed to show temperatures both in degrees Centigrade and degrees Fahrenheit.

This article has been set out so that those who wish to just get on and make a digital thermometer can do so, by turning to the end of this article and following the instructions given there. For more accurate results, however, it would be better to follow through the steps suggested in the first part of this article. The reason for this is that thermistors, the sensor in this project, can vary quite dramatically in their characteristics, and the thermistor I have used may vary slightly from the one you will use - so some calibration may be required to make it more accurate. This article will also follow through all the stages taken in the design of this thermometer, as some experimenters may wish to develop ideas of their own based on this system.

The first stage in the design is to work out a 'plan of attack'. In this case, it is a simple block diagram. (Figure 1)

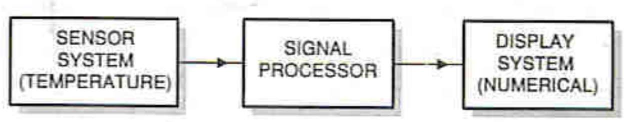


Figure 1:

The first element of the design is obviously the sensor system itself. This must be something which changes its output voltage as the temperature changes. This must clearly be based around a thermistor. The thermistor I have chosen to use is a 100k bead thermistor which is accurate to ±2%, being one of the most accurate available on the present-day market. They are also inexpensive and compact. Since a thermistor's resistance falls as the temperature increases, it should be made the top half of a potential divider as in figure 2, so that the output voltage is proportional to the temperature.

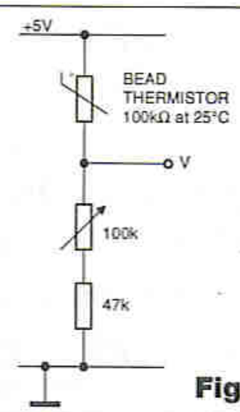


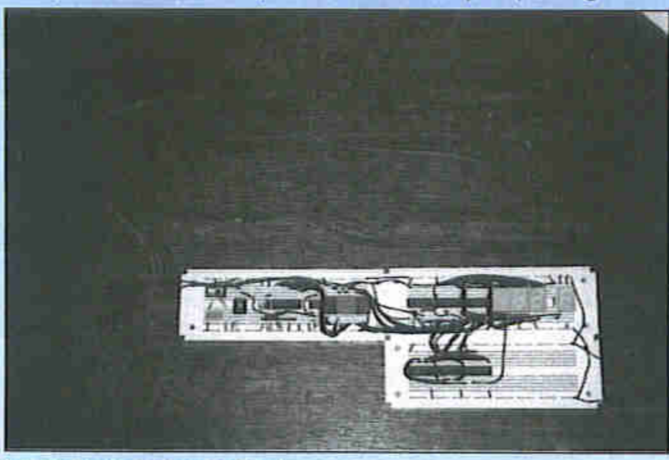
Figure 2

Thermistors are usually non-linear devices and therefore notoriously difficult to use. Books provide a formula for calculating the resistance of the thermistors at different temperatures, but experience shows that the formula is only an approximation which will probably not be accurate enough for our purposes. The formula is:

RT1 = RT2.e(B/T1 - B/T2)

RT1 and RT2 in Kelvin.
B is a constant - e.g. 4450

RT1 is the resistance at a temperature T1, in degrees Kelvin. RT2 is the resistance at a temperature T2, which is given in the data about the thermistor found in catalogues. B is a constant specific to each thermistor, which is also given in the catalogues. If we use this formula, using RT2 = 100k at 298K, we find that the resistance varies with temperature in the way shown in the graph (Figure 3).
This is all right as an approximation, but if we actually work this out by taking one of these thermistors and varying the temperature between about +40∞C and -14∞C and measuring the resistance with a meter, we find that the graph is slightly different. The graph shown in Figure 4 is what I found for my thermistor. All thermistors are slightly different so, for a more accurate thermometer, a test is best performed individually This can be done by suspending the thermistor above a beaker of water and positioning a standard thermometer very close by. Varying the temperature of the water by adding hot/cold water varies the temperature of the thermistor, which can be measured using the thermometer. The resistance can then be measured using the resistance meter. This will only provide a range of temperatures from about 14∞C upwards - it will not provide a complete range of temperatures. To reach the lower temperatures, some experimentation has to be done with refrigerators and their ice compartments, or alternatively with freeze sprays.



'MEASURING APPARATUS'

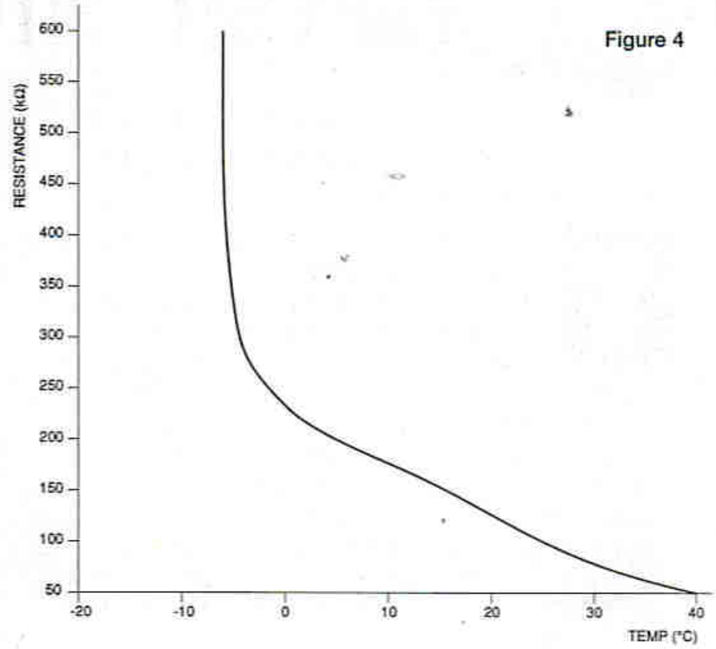


Figure 4

Looking at this graph, it becomes clear that between 0∞C and 30∞C the relationship is almost perfectly linear but is not so outside these temperatures, particularly below 0∞C. Finding exact values for the resistance below 0∞ will prove very difficult, and below -5∞ one is forced to form an approximation based on the two graphs. As the resistance of the thermistor is varying so much with only small changes in temperature, this approximation should not affect its accuracy below 0∞C very much. It should still be accurate to within one degree or less.

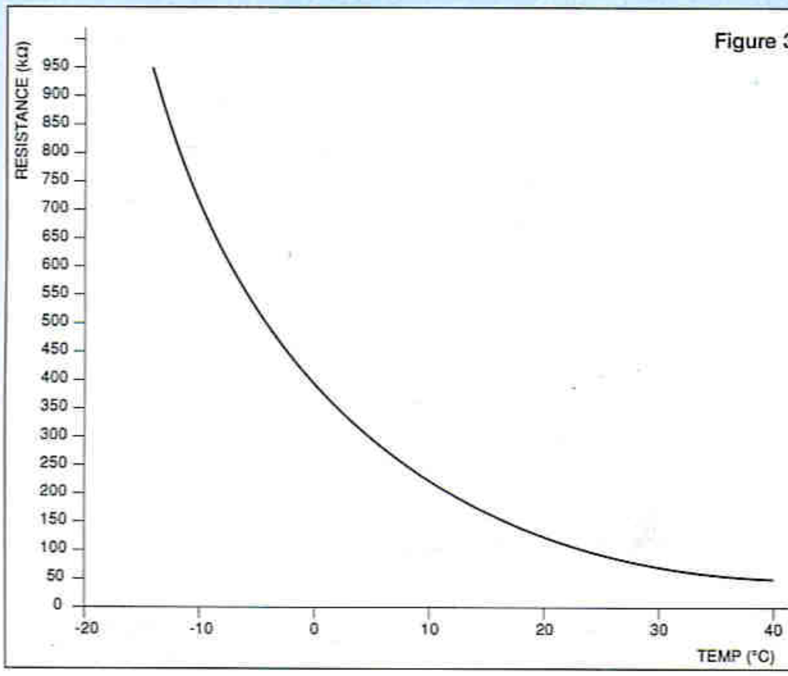
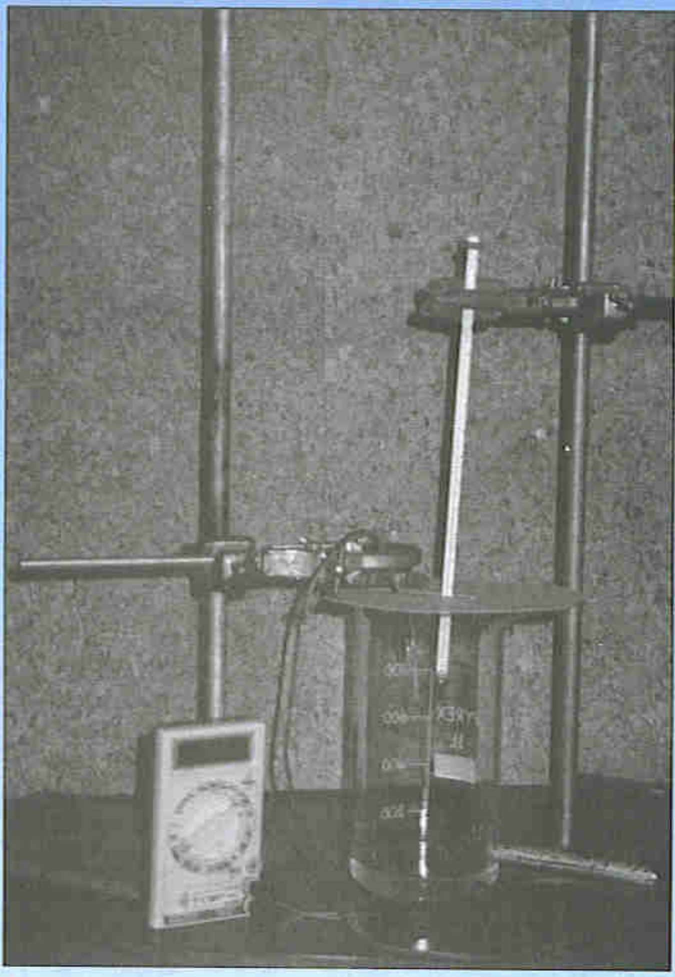


Figure 3

The next stage is to design the processing system. This must convert the analogue signal coming out of the potential divider into a digital signal which describes the temperature. As the temperature ranges from -14∞C to +40∞C, or from 7∞F to 104∞F, only 10 bits of digital data will be required at the output; 4 bits for the units, 4 bits for the tens, 1 bit for the hundreds and one bit to describe the polarity (+/-). Since our aim is to change an analogue signal into a digital one, the obvious component to base this system upon is an analogue-to-digital converter, or ADC. A simple ADC is the ADC0804LCN although other similar chips could be used. This is an 8-bit ADC; in other words, it converts the analogue input into a binary word 8 bits long. Its pin-out diagram is shown in figure 5.

With the bottom half of the potential divider shown in Figure 1 at 100k, the voltages going into pin 6 should vary between 0.45V and 3.33V. Pin 7 should be held at 0V and pin 9 should be held at 2.5V, ensuring that the entire range is covered. Pin 9 is



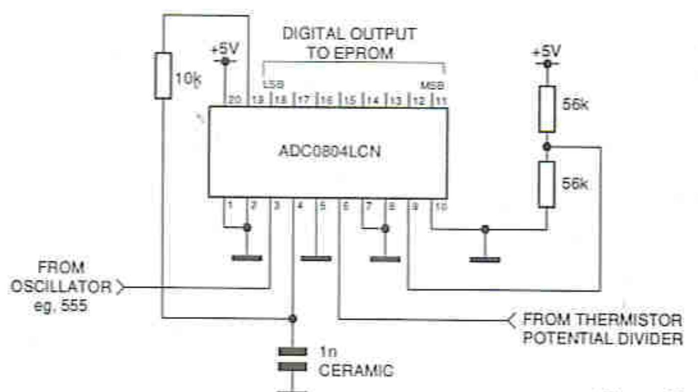


Figure 5

held at 2.5V because the component requires it to be held at half of the range voltage. The range voltage is 5V. The digital data then comes out of pins 11 - 18. The digital data that came out of the ADC when I applied different voltages across it, corresponding to the different temperatures, is shown in Figure 6 This data is purely the digital voltage we had earlier but expressed in a different form, and so the relationship between the magnitude of this voltage and temperature is still not linear. This digital number, however, is much easier to play with. It would probably be easiest to convert this analogue voltage into the actual temperature by using an EPROM. One of the cheapest and easiest to use is probably the 2716 EPROM. We can convert Figure 6 into an EPROM program fairly easily, by just filling in all the gaps in the data with numbers that would probably be about right. We can also fill in appropriate numbers for the temperature in Fahrenheit in the addresses 100 to 1FF, as the

Table of relationship between temperature and both analogue and digital output

Temperature (C	Analogue Output	Digital Output
40	3.33	01010101
39	3.29	11100101
38	3.23	00100101
37	3.18	01000101
36	3.13	01111001
35	3.07	00111001
34	2.99	10011001
33	2.98	11101001
32	2.92	00101001
31	2.84	00001001
30	2.81	11110001
29	2.73	11010001
28	2.70	10010001
27	2.65	11100001
26	2.58	11000001
25	2.50	11111110
24	2.45	10111110
23	2.39	01011110
22	2.34	11101110
21	2.28	00101110
20	2.24	01001110
19	2.19	11110110
18	2.15	01110110
17	2.10	11010110
16	2.05	00010110
15	2.00	01100110
14	1.96	00100110
13	1.92	01000110
12	1.88	00000110
11	1.84	01111010
10	1.79	11011010
9	1.76	10011010
8	1.73	00011010
7	1.69	10101010
6	1.66	00101010
5	1.62	01001010
4	1.61	10001010
3	1.58	00001010
2	1.56	11110010
1	1.53	01110010
0	1.51	10110010
-1	1.47	11010010
-2	1.41	00010010
-3	1.34	00100010
-4	1.25	00000010
-5	1.14	01011100
-6	0.75	01100100
-7	0.71	00100100
-8	0.67	01000100
-9	0.64	00000100
-10	0.60	01111000
-11	0.57	10111000
-12	0.54	11011000
-13	0.51	01011000
-14	0.48	10011000

system will incorporate a switch to allow the user to choose between Centigrade and Fahrenheit. This switch will make the I8 pin high if Fahrenheit is chosen or low if Centigrade is chosen. The complete EPROM program which suits my thermistor is shown in figure 7.

Where there is a negative sign involved, I have placed a '1' at output O7. The reason for this will be explained later.
Even if you have decided to follow through all the steps I have given in designing this thermometer, you need not necessarily develop your own EPROM program. If your graph of the variance of resistance of the thermistor with respect to temperature is the same or very similar to mine, then the program would turn out to be almost identical. A new program is only really necessary if your graph is significantly different.

EPROM programming code - A=Address D=Data

A	D	A	D	A	D	A	D
000	00	037	85	06E	18	0A5	38
001	00	038	85	06F	19	0A6	39
002	00	039	85	070	19	0A7	39
003	00	03A	85	071	20	0A8	39
004	00	03B	84	072	20	0A9	39
005	00	03C	84	073	20	0AA	40
006	00	03D	84	074	21	0AB	40
007	00	03E	84	075	21	0AC	40
008	00	03F	84	076	22	0AD	40
009	00	040	84	077	22	0AE	40
00A	00	041	83	078	22	0AF	40
00B	00	042	83	079	23	0B0	
00C	00	043	83	07A	23	Ø	00
00D	00	044	83	07B	23	0FF	
00E	00	045	83	07C	24		
00F	00	046	82	07D	24		
010	00	047	82	07E	24		
011	00	048	82	07F	25		
012	00	049	82	080	25		
013	00	04A	81	081	25		
014	00	04B	81	082	26		
015	94	04C	00	083	26		
016	94	04D	00	084	26		
017	94	04E	01	085	27		
018	94	04F	02	086	27		
019	94	050	03	087	27		
01A	93	051	04	088	28		
01B	92	052	05	089	28		
01C	91	053	06	08A	28		
01D	91	054	06	08B	29		
01E	90	055	07	08C	29		
01F	90	056	07	08D	30		
020	89	057	08	08E	30		
021	89	058	08	08F	30		
022	88	059	09	090	31		
023	88	05A	09	091	31		
024	87	05B	10	092	31		
025	87	05C	10	093	32		
026	86	05D	11	094	32		
027	86	05E	11	095	32		
028	86	05F	12	096	33		
029	86	060	12	097	33		
02A	86	061	13	098	33		
02B	86	062	13	099	34		
02C	86	063	14	09A	34		
02D	86	064	14	09B	35		
02E	86	065	15	09C	35		
02F	86	066	15	09D	35		
030	86	067	15	09E	36		
031	86	068	16	09F	36		
032	85	069	16	0A0	36		
033	85	06A	17	0A1	37		
034	85	06B	17	0A2	37		
035	85	06C	17	0A3	37		
036	85	06D	18	0A4	38		

As the EPROM has only 8 outputs, a problem arises when the temperature rises above 99∞F or if it becomes negative. Using a larger EPROM would greatly increase the cost of the system so this should be avoided if at all possible. As I mentioned earlier, when a negative was involved, I placed a '1' at output O7 in the program. This problem only occurs when the thermometer is operating in Centigrade, as -14∞C is +7∞F. When operating in Centigrade, the thermometer does not rise above 40. This means that when the thermometer is operating in Centigrade, the most significant bit of the output, O7, can be used to indicate whether the value is positive or negative. When in Fahrenheit, this bit cannot be used as it is needed to describe the temperature. Therefore, the switch which allows the user to choose between Fahrenheit and Centigrade must also allow the negative sign to be used when appropriate, and also prevent output O7 from causing incorrect information to be displayed. This is done by using a couple of analogue switches, found on the 4066 IC. One of them disconnects O7 from the displays when it is operating in Centigrade; the other disconnects the negative sign when it is operating in Fahrenheit. These two analogue switches can be seen in the full circuit diagram.

A problem still arises when the temperature rises above 99∞F. All the EPROM outputs are used to describe the range of temperatures in Fahrenheit, and so one of these cannot be used. It is not worth using a bigger EPROM, so I have used a bit of logic to operate the 'one hundred' display. The range in Fahrenheit is from 07 to 104. The one is only needed on the hundreds display if the output from the EPROM is 00, 01, 02, 03, or 04; but not if it is 07, 08, 09 or anything higher.

The obvious first step is to devise a method of identifying the first number being 0. This is a simple task involving three OR gates and a NOT gate. This simplifies the problem down to identifying 0, 1, 2, 3, and 4; but not 7, 8, or 9. 8 and 9 both have 1 at the most significant bit, (1000 and 1001). 7 has a 1 at both bits B and C (0111), a feature which is not present with any of the other numbers. The resulting logic system is shown in figure 8.

The next stage in the design is the display system . This should consist of numerical (seven-segment) displays and a display to indicate whether it is operating in Fahrenheit or Centigrade. Both an 'F' and a 'C' can be easily shown on a seven-segment display, which is the most attractive and sensible method. Both the negative sign and the one hundred mark can be put on the same display, again a seven-segment. We are now using four seven-segment displays, but only two of them need drivers as the others can be driven directly from their respective switches.

The design of the system is now complete. The next stage is the actual construction. The complete circuit diagram is shown overleaf in figure 9.

Building the system:

The foil required to make the printed circuit board for this thermometer can be found at the rear of this publication. For those of you who have skipped to this point after the first paragraph, a 2716 or 2516 EPROM is required, and should be loaded with the program given in figure 7. Apart from that, it is merely a case of soldering in chips, resistors, capacitors and wires in the right places. To help you with this, there is, of course, a table indicating

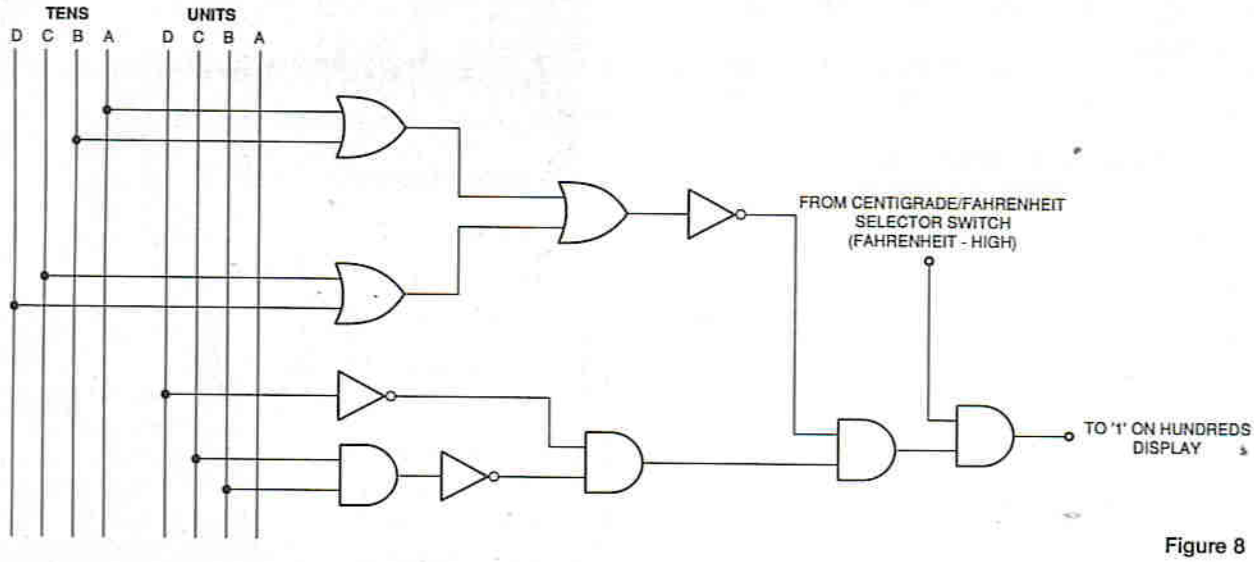
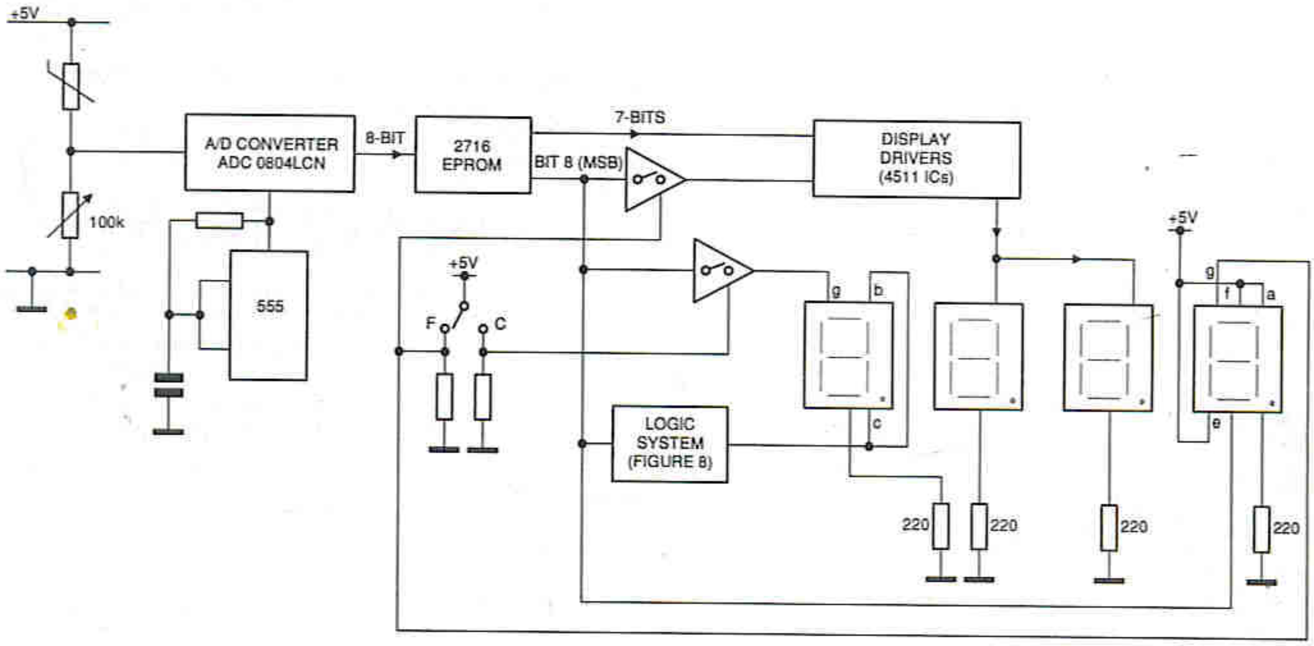


Figure 8

Figure 9



what value each resistor etc should be. There is also a diagram of the system to the same scale as the PCB which does not show where the printed wires are but shows everything else instead. This enables you to work out where all the chips etc. should go. On this diagram, WL stands for wire link, and the chip numbers are given where the chips should be. Please note that when making the printed circuit board, the writing (DIGITAL THERMOMETER etc.) should appear the correct way up on the completed board when looking at it from the solder side. The thermometer should work normally if run off a 6V battery, which should last a long time, as current is only drawn when the push switch is pressed.

A	D	A	D	A	D	A	D
100	00	134	22	168	61	19C	95
101	00	135	22	169	61	19D	95
102	00	136	23	16A	62	19E	96
103	00	137	23	16B	63	19F	97
104	00	138	23	16C	63	1A0	97
105	00	139	23	16D	64	1A1	98
106	00	13A	23	16E	65	1A2	99
107	00	13B	24	16F	65	1A3	99
108	00	13C	24	170	66	1A4	00
109	00	13D	24	171	67	1A5	00
10A	00	13E	25	172	68	1A6	01
10B	00	13F	25	173	68	1A7	02
10C	00	140	25	174	69	1A8	02
10D	00	141	26	175	70	1A9	02
10E	00	142	26	176	71	1AA	03
10F	00	143	26	177	72	1AB	03
110	00	144	27	178	72	1AC	04
111	00	145	27	179	73	1AD	04
112	00	146	28	17A	73	1AE	04

A	D	A	D	A	D	A	D
113	00	147	28	17B	74	1AF	04
114	00	148	28	17C	75	1B0	
115	07	149	29	17D	75	Ø	00
116	07	14A	30	17E	76	1FF	
117	07	14B	31	17F	77		
118	08	14C	32	180	77		
119	08	14D	33	181	78		
11A	09	14E	34	182	79		
11B	10	14F	35	183	79		
11C	11	150	37	184	80		
11D	12	151	39	185	81		
11E	13	152	41	186	81		
11F	14	153	42	187	81		
120	15	154	43	188	82		
121	16	155	44	189	82		
122	17	156	45	18A	83		
123	18	157	46	18B	84		
124	19	158	47	18C	84		
125	19	159	48	18D	85		
126	20	15A	49	18E	86		
127	20	15B	50	18F	86		
128	20	15C	51	190	87		
129	20	15D	52	191	88		
12A	20	15E	53	192	88		
12B	20	15F	54	193	89		
12C	21	160	54	194	90		
12D	21	161	55	195	90		
12E	21	162	56	196	91		
12F	21	163	57	197	91		
130	21	164	58	198	92		
131	21	165	59	199	93		
132	22	166	59	19A	93		
133	22	167	60	19B	94		

PARTS LIST

RESISTORS

R1	56k
R2	47k
R3	10k
R4	220k
R5	220k
R6	4.7k
R7	220
RT	Thermistor
Rva	100K variable resistor

Capacitors

C1	1 nF
C2	1 F

Miscellaneous

SW1	Push button switch
SW2	SPDT Switch
WL	Wire Link
555	555 IC (Oscillator)
ADC0804	ADC0804 IC A/D Converter
2516	2516 / 2716 IC 16K EPROM
4066	4066 IC Quad Analogue Switch
4071	4071 IC Quad OR Gate
4081	4081 IC Quad AND Gate
4069	4069 IC Quad NOT Gate
4511	4511 IC Display Driver

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DRIVING TRIACS WITH THE PIC MICRO-CONTROLLER

Bart Trepak takes a look at some of the problems associated with using a PIC to control mains power devices

The PIC16C series of micro-controllers are being used more and more in projects featured in this magazine as well as in commercially built equipment. There are many reasons for this not least of which is cost, as such a chip can easily replace a dozen or more digital logic ICs at a fraction of the price especially when the cost of assembly, stock ordering and holding are taken into account.

For the hobbyist and experimenter this is also an advantage - he no longer needs to have scores of chips and components in stock to be able to "knock up" a circuit to test his latest idea and the small number of external components means that the complete circuit can be built on a breadboard in a matter of minutes.

Programming of course takes a bit longer but is much more fun - you can never run out of instructions like you can with 10k resistors and the chances of your newly-built project going up in smoke because you accidentally left the supply on when you tried to solder a different value resistor are (almost) non existent as most of the development is done sitting in front of a computer screen.

Another big advantage is the low power consumption of the device which makes it an ideal candidate for battery powered equipment where current drain must be kept to a minimum. The low power consumption can also be used to advantage in mains powered equipment which would not normally be considered to be "low power" by enabling smaller and thus cheaper power supply components to be used.

A typical application would be in driving a triac which could control many hundreds of watts of power to a motor, heater or lamp while the control logic consumed only a few milliwatts. Here, if the control section of the circuit required a current of a few hundred milli-amps, the designer would have little choice but to use a mains transformer to obtain the necessary low voltage supply.

Often this is mandatory on safety grounds, especially if it is essential to have the input of the control logic earthed, but in many applications this is not the case as the device has no input which can be touched by the user other than perhaps a switch or potentiometer which will normally have the electrical parts well isolated anyway. If isolation from the mains is not required, and the power requirement of the drive circuit can be reduced, a simple capacitor or resistive mains dropper which is, of course, much smaller and cheaper than a mains transformer can be used.

Capacitor mains dropper circuits have the advantage of consuming less power themselves and thus generating less heat than either a transformer or resistor so these tend to be

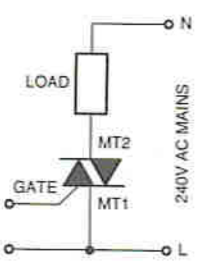

Fig 1.

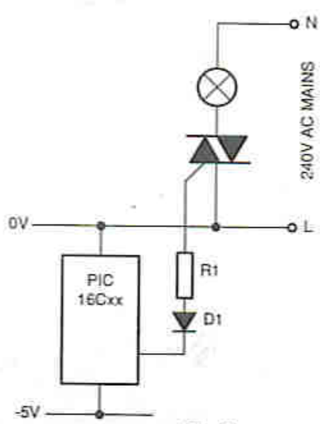

Fig 2.

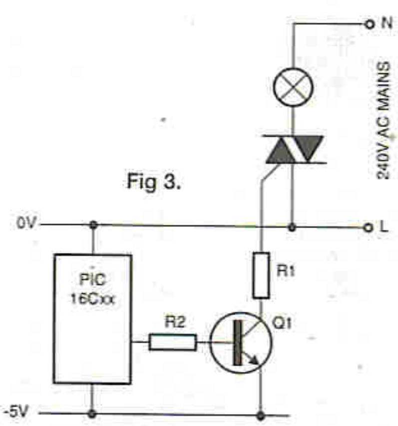

Fig 3.

favoured in many designs and the low power consumption of the PIC micro-controller can be used to advantage in such circuits. This article will deal with interfacing mains voltages to PIC inputs and driving triacs from the output ports of the micro-controller but before we do this, a few words about Triacs may be helpful.

The Triac

The Triac is a semiconductor device which was developed in the 1960s to switch high voltage AC supplies and is used extensively in lamp dimmers, washing machine motor speed controllers and other domestic appliances and, despite more recent advances in the design of power FETs, it remains the cheapest and most widely available component for this function. Many readers are no doubt familiar with it but it does have some characteristics which may not be so widely known but which must nevertheless be considered.

The triac has three terminals called MT1 (main terminal 1), MT2 and the gate as shown in Fig 1. Normally, the device blocks current flow between MT1 and MT2 ensuring that no current flows into the load which could be a mains lamp, a heater, a motor etc. When a small current (typically a few tens of milli-amps) is allowed to flow between the gate and MT1, the device switches on enabling the lamp to light or the motor to turn. Once this happens, the main current will continue to flow, even if the gate current is stopped. To switch the device off, the main current must be reduced by some external means to below a value known as the holding current. This happens automatically on mains supplies when the mains voltage drops to zero at the end of each half cycle. The triac will then switch off and will need to be re-triggered in the following half-cycle if the load is still required to be switched on.

Not only can the main current flow in either direction but the device can be triggered into conduction by either polarity of gate current and the triac is most sensitive (i.e. requires the smallest gate trigger current) when the gate current is negative. For the lowest possible supply current for the trigger circuit, it is therefore best to trigger the triac with a negative gate current which can be achieved simply by using a negative d.c. supply as shown in fig 2.

In general, lower power triacs require a lower gate current to guarantee triggering than do higher current devices with a typical 3 Amp device such as the TIC206 requiring a maximum current of 5-10mA. An 8 Amp device such as the TIC226 which could control up to 2KW of mains power could require up to 50mA but sensitive versions are available which would switch reliably with only 10mA. With capacitor dropper supplies, it is therefore best to use sensitive gate devices.

Note that, because continuous gate current is not required, but only a pulse lasting, say, 100uS, considerable savings in supply current drain can be achieved by pulsing the gate current, thus reducing further the average supply current required. This would reduce the value of the required mains dropper capacitor and as the maximum supply current from such circuits is limited to some 30mA if very large capacitor values are to be avoided, it could make the difference between making a transformer-less circuit feasible or not.

One thing which is often forgotten when using pulse triggering is that for the triac to remain in conduction after it has been triggered, the load current must exceed a value known as the latching current before the trigger current ceases. Unlike the holding current which has a typical value of 10-20mA for small devices, this can be as high as 80 -100mA. With resistive loads, this is not often a problem because even if the trigger pulse is short, this current is usually achieved before the gate pulse terminates.

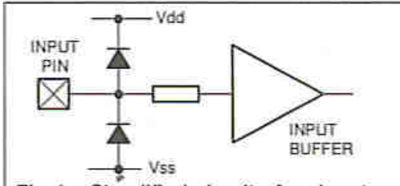

Fig 4a. Simplified circuit of an input port

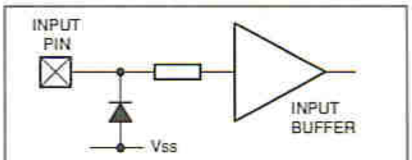

Fig 4a. Simplified circuit of RTCC input

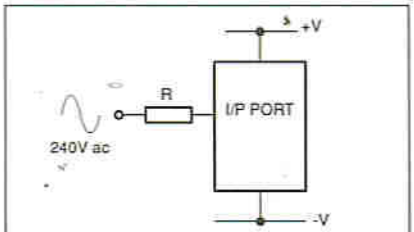

Fig 4c. Circuit a for Port input

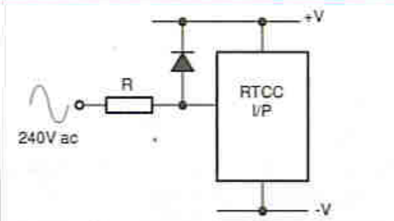

Fig 4c. Circuit a for RTCC input

It can be a problem however, if low power (high resistance) loads are used or with transformers or solenoids where the build-up of load current after triggering is much slower because of the inductive nature of the load. It is also important if triggering very early in the half-cycle is required when the mains voltage may be too low to enable a sufficiently large current to flow to guarantee latching.

In these circumstances where the latching current may cause problems, d.c. triggering should be used with the gate current flowing continuously throughout the mains half-cycle. This is possible because a triac will stay in the conducting state even if the main terminal current is below the latching current value, provided that the trigger current is maintained. If this cannot be done because of other considerations, then the trigger pulse should be lengthened or multiple trigger pulses should be provided rather than relying on one pulse per half-cycle to switch the triac on.

PIC your circuit

The diagram in Fig 2. also shows a triac connected to the output of a PIC16C. Since the output ports of this micro-controller can sink up to 20mA or more, they can drive the gate of most small triacs directly. If more current is required, a driver transistor may be used as shown in Fig 3. The programmer thus only needs to define the port in question as an output (using the TRIS instruction or equivalent) and then write a 'zero' to enable gate current to flow or a 'one' to switch it off. If an NPN transistor is used as shown in Fig 3, a logic 0 would switch the triac off and a 1 would switch it on.

In figures 2 and 3, resistor R1 defines the triac gate current and is chosen to give a value which will guarantee to trigger all triacs of the type specified. This can be calculated from Ohm's Law knowing the supply voltage (usually 5 Volts) and the MT1-gate voltage which is about 1 Volt. Thus if a value of 10mA is required, R1 will be (5-1)/10 which is .4kOhms or 390 Ohms to the nearest preferred value. Assuming a transistor current gain of 20 in Fig. 3, R2 would need to be about 8k2 or less. If the micro-controller supply voltage is lower (it could be as low as 3V) then a 220 or 180 Ohm resistor should be used for R1.

The diode in Fig. 2 may seem a bit superfluous until it is realised that when a triac is triggered, current can flow out of the triac gate (in phase with the main current) and is limited by

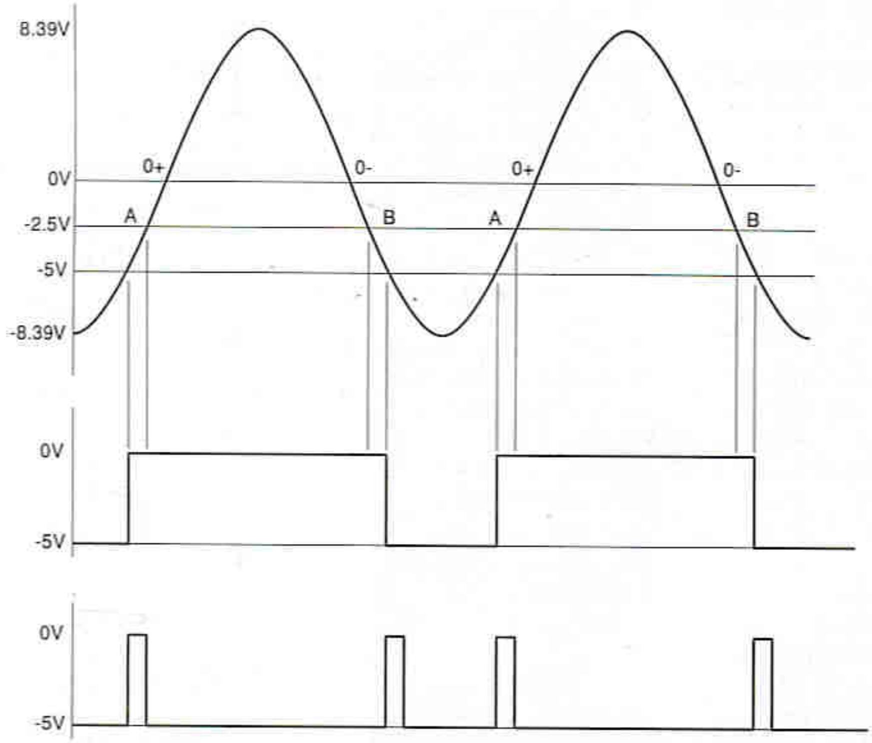

Fig 5. Mains waveform, Input waveform and resulting Zero Crossing Signal

half-cycle when the mains voltage has dropped to zero before triggering the triac. For this, a zero crossing detector is required and many discrete circuits have been published over the years and many integrated circuits are also available to perform this function, often in conjunction with extra circuits for driving triacs and sensing temperature using thermistors. If you are already using a PIC in your project, however, it would seem extravagant to use another IC to perform this simple function when it could be done with a few more lines of programme code in software.

the series resistor. Although the PIC does not seem to be worried by this, caution suggests that it is probably not a good idea to shove a.c. into its output and the diode prevents this. Allowance for the volt drop in this component should be made giving a slightly lower value of say 100 Ohms for R1 in Fig 2.

Zero crossing

One of the problems with switching the mains on, is that this often occurs when the instantaneous mains voltage is rather high - certainly over 20V, which is not surprising since the mains waveform spends only a relatively short time below this value during the zero crossing points. This means that the load current increases suddenly from zero (before the triac is triggered) to a relatively high value limited by the load resistance and the instantaneous voltage across it. This leads to a pulse of interference which can often be heard in a radio loudspeaker when a light is switched on in a room.

A triac is capable of being switched on (and turning off) once every mains half-cycle and could therefore generate a large amount of interference which would cause a continuous buzz in the speaker. Even if it is not switched on so often, large interference pulses could still be radiated or conducted through the mains wiring to upset computers or other equipment sharing the same supply, especially if heavy loads such as heaters are being switched.

Another problem which occurs when lamps are switched on, is that a very large surge current can flow at initial switch-on because the filament is cold and has a low resistance. This can result in the premature failure of the lamp and the triac. Lamps often appear to fail when they are first switched on but hardly ever when they are on.

The trick used to overcome these problems is to switch the triac on only when the mains voltage is near zero, often below 5 Volts, irrespective of when the command to switch on is received. Thus if a thermistor sensor in a heater controller signals that more heat is required half way through a mains half-cycle, the controller will wait until the beginning of the next

Mains inputs

Before we go on to describe a suitable programme, the a.c. mains signal must first be connected to the input of the PIC so that the mains crossing point can be detected. Since the PIC operates from a 5V d.c. supply while the mains is 230V a.c., it would seem that some form of rectifier and potential divider would be required to prevent damage to the device but, in practice, nothing so elaborate is required.

The diagram in Fig. 4a shows the input circuit of a typical I/O port (configured as an input) which shows two diodes which form part of the static protection circuit of the PIC series of micro-controllers. It is therefore only necessary to connect the mains to the input through a current limiting resistor as shown in Fig. 4c and the diodes will then clamp the input voltage appearing at the pin to within 0.6V of the positive or negative supply rail, depending on the polarity of the signal, thus preventing any damage to the chip.

Since the input impedance is very high, almost any value resistor of a few MOhms or so will do as the current requirements and the power dissipation are negligible. A 4M7 resistor will limit the peak input current to less than 80uA for a 265V a.c. input which is well within the safety limits and dissipate a mere 12mW. Because most quarter watt resistors only have a voltage rating of 250V, it is better to use a 1/2W resistor or two 2M2 1/4W components in series.

Note that the input circuit for the RTCC input is slightly different having only one clamping diode (Fig. 4b) so that a separate diode must be fitted as shown in Fig. 4d if this input is to be used for sensing the mains voltage. The resulting waveform at the input port of the PIC during the positive and negative mains half-cycles is shown in Fig. 5 immediately below the mains waveform.

Software

One way to detect a zero crossing would be to apply the mains signal to an input and test it to see when it became high using the BTFSS or BTFSC instruction and either repeat the test if it was not or branch to execute the zero crossing routine each time the test was successful. Here the decision would be made on whether or not to switch the triac on depending on the other parameters in the programme such as 'is the temperature too low ?' or 'is it Tuesday afternoon?' etc.

As this decision would only be made at the beginning of the positive mains half-cycle, the triac could only be switched on then ensuring zero voltage switching. Also, because the PIC

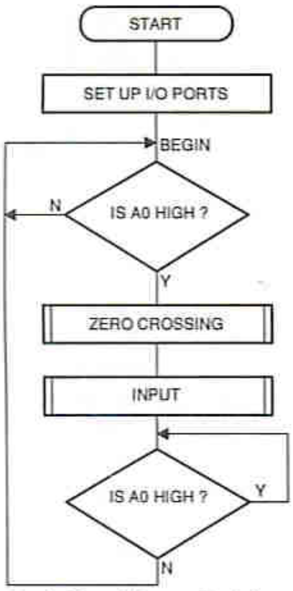

Fig 6. Zero Voltage Switch Flowchart

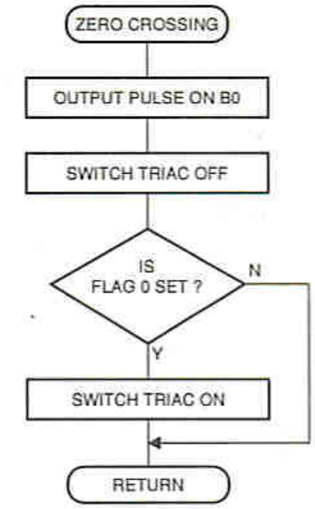

Fig 6a Zero Crossing Subroutine

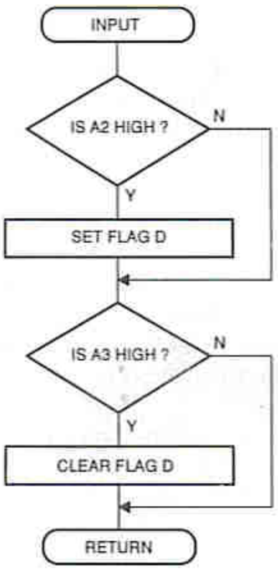

Fig 6b. Input subroutine

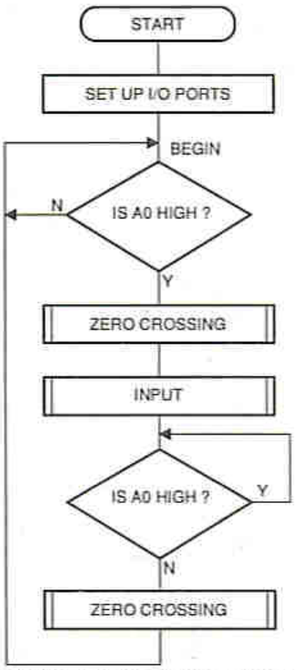

Fig 6c. Modified zero voltage switch Flowchart to detect both zero crossing

output would, once switched on, remain on throughout the positive and succeeding negative half-cycle, this would ensure that the triac stayed on for the full mains cycle. In many applications where only on/off control is required, it will not make any difference if only the positive or negative mains zero transition is detected as long as the output remains on throughout the cycle.

Indeed, when switching very high power loads or transformers, it would be an advantage to switch only integral cycles with equal numbers of positive and negative half-cycles being applied to the load. This would avoid introducing a d.c. component into the mains and reduce initial inrush currents when switching transformers by ensuring that the core always remained magnetised in the opposite direction at switch-off to the one it would assume at switch-on.

The Zero Crossing routine is a short piece of code which could be executed by the PIC in a few micro-seconds, resulting in multiple "sucessful" tests of the input port being carried out during the positive half-cycle. The programme would therefore have to be written so that only the first positive crossing was detected and not the fact that the input was high, which would be the case throughout the positive half-cycle and could result in the triac being switched on at any time during the positive half-cycle. This can be done by testing for a subsequent low input voltage following a successful test as would occur during the succeeding negative half-cycle before returning to the original test for a logic high input. This is shown in the flowchart of Fig. 6.

The above method of implementing a zero crossing detector is fine but uses up one line of an I/O port which may be required for other purposes. This can be avoided by connecting the mains signal to the RTCC input instead. In this case, the RTCC register would first be loaded with 0FFh (255 in decimal) and the OPTION register set up to increment the RTCC register on the positive transition of the signal on the RTCC pin so that the counter would 'overflow' to zero at the beginning of each positive half-cycle. The programme would then need to continuously test the RTCC register for zero by testing the zero bit (2) of the status register (movf RTCC,1 followed by btfss STATUS,2) instead of an input high and the first instructions in the zero crossing subroutine would reload the RTCC register with 0FFh before switching the triac or not as required.

Figure 7 shows a listing for a static zero voltage switch for the circuit shown in Fig. 8. Here, the triac is triggered from output port A1 while the mains is applied to the input A0 via a resistor. Port B0 has been configured as an output and generates a pulse each time the zero crossing routine is executed. This can be displayed on an oscilloscope for reference if required. (Note that the circuit is connected to the mains and must not be earthed even via the 'scope probe.) This output is not required for the operation of the circuit and after testing, the instructions which perform this function (bsf PORTB,0 and bcf PORTB,0 in the ZRX subroutine) can be removed leaving the whole of port B free to perform any other functions which you may need in your application. Ports A3 and A4 are ON and OFF inputs respectively and operate when switches S1 or S2 are pressed.

Because the triac is triggered by a continuous d.c. current, it switches on very early in each half-cycle irrespective of the load resistance so that there are no problems with the latching current. In consequence, no noise is generated but the penalty is a fairly high supply current which requires a larger value of "mains dropper" capacitor. The programme could be written to provide a pulsed trigger current resulting in a lower average supply current and hence a smaller value capacitor but the triac would then be triggered on the first or second gate pulse after the positive zero crossing by which time the mains voltage could be as high as 20 or 30 Volts resulting in a noticeable increase in the radio interference.

The assembler programme listing shown in Fig. 7 should be quite easy to follow in conjunction with the flowchart of Fig. 6. A register called "FLAG" is first defined (the other registers such as STATUS, PORTA, PORTB etc. being declared in the PIC.H file) and after the power on reset, the programme goes to the label SETUP where the ports are set up as inputs or outputs as required. The programme proper starts at the label BEGIN calling the subroutines ZRX and INPUT when the input

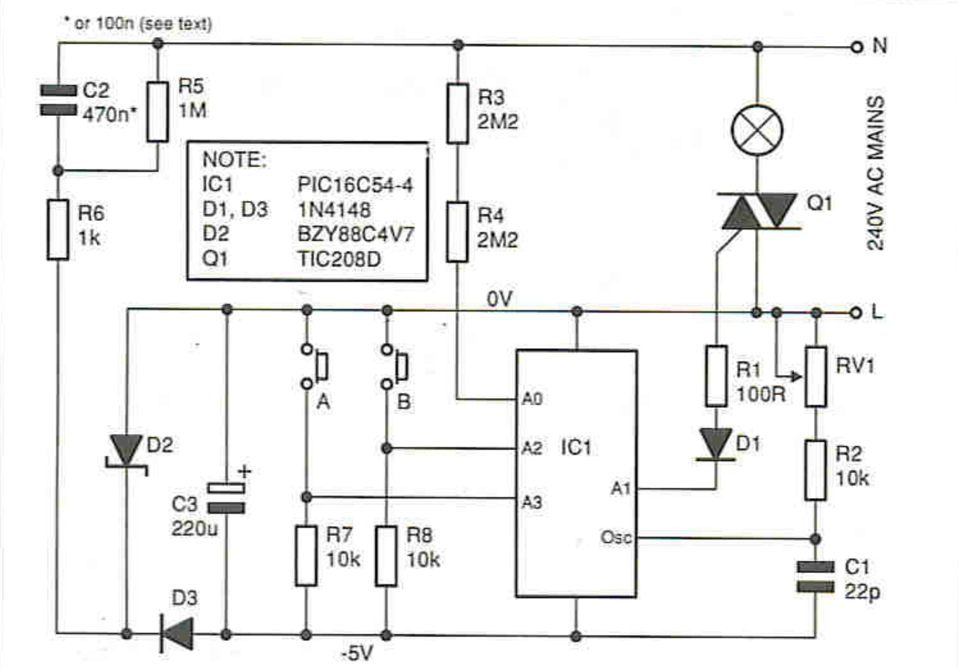

Fig 8. Circuit diagram of Zero Voltage Switch/Dimmer

port A0 goes positive. The ZRX routine produces a pulse on port B0 and clears A1 if bit 0 of the flag register is set switching on the triac. The INPUT routine checks ports A2 and A3 for possible inputs and either sets or clears bit 0 in the FLAG register depending on which one is high. FLAG 0 therefore acts as a memory to remember which switch was pressed last and thus whether the output should be on or off. This is a simple (almost trivial) application of a PIC but it could easily be modified and extended. By suitably altering the INPUT routine a toggle function could be implemented, or the output could be made to switch on if the designated input was high and off if low without the need for the FLAG register. This could be further combined with inputs from sensors or the states of other registers within the PIC counting real time for example, to make a sophisticated central heating controller.

Negative half-cycle

For static on/off switching applications, the above routine is perfectly adequate but in some applications, both the negative and positive mains zero crossing transitions may have to be detected. This can be done by modifying the flowchart of Fig. 6 slightly to that shown in Fig. 6c. A similar modification could be used if the RTCC input were being used instead.

To better understand how this programme works and its limitations, refer again to Fig. 5. This shows the mains waveform and superimposed on this (greatly exaggerated) is the d.c. supply for the PIC which is negative, with the dotted line showing the voltage at which the microcomputer input recognises a logic 1 or logic 0. Because this is a CMOS device, it is assumed that this threshold voltage is at half of the micro-controller supply rail (i.e. -2.5Volts) and, for simplicity, it is the same for positive or negative input transitions.

The second waveform shows the signal at the input pin which is just a clamped version of the mains waveform. From this it will be seen that the positive zero crossing edge 'A' occurs slightly before, while the negative one 'B' slightly after, the actual mains zero crossing points designated '0+' and '0-'. This is greatly exaggerated by the way that the waveforms have been drawn but in practice it could cause a problem. If continuous (or d.c. or pulse) triggering is employed, the triac trigger signal will only be switched on or off at points A or B so that in the positive going mains transition it will mean is that if the triac were triggered at 'A', gate current would continue to flow until point "B". At "0-" (the true zero crossing), the triac would try to switch off but would be re-triggered as gate current was still flowing.

The triac would therefore continue to conduct throughout the negative half-cycle even if the trigger current had been terminated at point "B". In zero voltage switching circuits, this would be of little consequence as the output would then simply remain on for one half-cycle longer than was required. Since this did not matter, it would have been rather pointless in going to the trouble in detecting the negative zero crossing point if no effective action could be taken there anyway - which is why it was not used in Fig. 7. In dimming applications, for example, where both zero crossing points must be detected but triggering at the beginning of the half-cycle is not required, this would be unacceptable.

For continuous and multiple pulse triggering therefore, gate current must not be allowed to flow beyond the true zero crossing point if independent control of positive and negative half-cycles is required. Since the circuit cannot detect these points directly, the micro-controller must determine when to terminate the trigger signal by timing it. How this is done will depend on the type of triggering employed. If the RTCC is not being used, it could be loaded with a suitable number and allowed to count the micro-controller clock pulses (with the prescaler and further counters if necessary) until it overflowed to zero which would be arranged to occur after a delay of just under 10mS (the mains half-cycle period at 50Hz) when the trigger pulse would be terminated.

The actual time could be adjusted by careful choice of the initial number loaded and/or the clock frequency which can be easily done if the RC clock option for the PIC clock is used instead of a crystal. If pulse triggering is used, the actual number of pulses generated can be counted which would achieve the same result and ensure that trigger pulses always ceased before a zero crossing.

A point to note if single pulse triggering is employed, is that the trigger pulse generated at "A" would need to be wide enough to extend beyond 0+ to ensure that the triac remained triggered during the positive mains half-cycle instead of switching off shortly after being triggered by the zero crossing at 0+. There would, of course, be no problem with single pulse triggering in the negative half-cycle, assuming that triac latching current requirements were met and, other than a slight asymmetry in the conduction times (A to 0- in the positive and B to 0+ in the negative half-cycles) the circuit would function correctly. This could also be corrected by inserting a short delay routine in the positive zero crossing programme to delay the trigger pulse until slightly after the true zero-crossing point 0+ if required.

It is perhaps worth mentioning that since the zero crossing subroutines will be entered every 10mS (20mS if only the positive zero crossing is detected), the number of times this routine is executed could easily be counted to generate a time base of 1 second, a minute or even a few weeks enabling a timer or real time clock to be added to the application with no

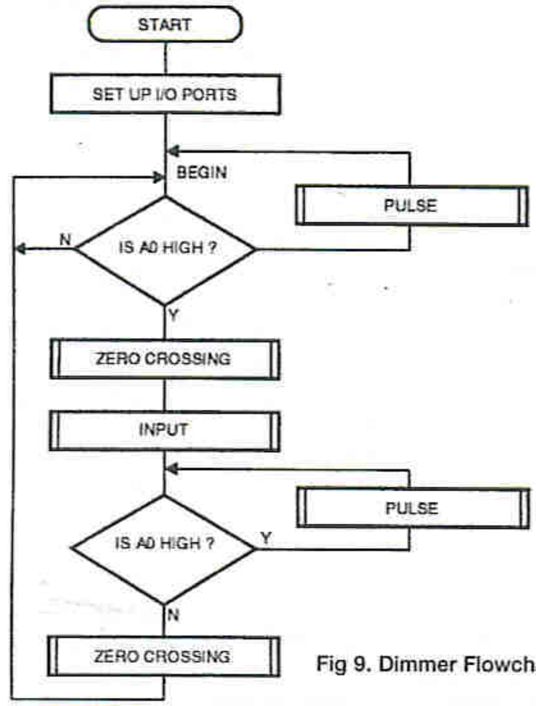

Fig 9. Dimmer Flowchart

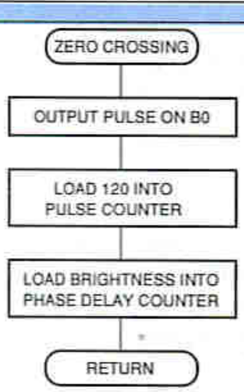

Fig a. Zero Crossing Subroutine

extra circuitry. This would have an accuracy dependent not on the RC oscillator but on the mains waveform which (in the long term) is, of course, very good.

Varying the power

In many applications, the power delivered to the load needs to be varied rather than just switched on or off. Despite the fact that a triac can only be in two states - ON or OFF, we can vary the power by switching it on for longer or shorter periods compared to the time for which it remains off. For example, switching a triac on for every other mains cycle will clearly result in half of the available power reaching the load while if only every fourth cycle was passed, the load would be run atone quarter of full power. If the load is a heater in an oven which can take say 60 seconds (3000 mains cycles) to reach full temperature or to cool down, then switching the triac on for one cycle every five seconds (250 cycles) will result in a very low power level being applied while if the triac is switched on for 250 cycles every five seconds, full power will flow to the load.

Intermediate numbers of cycles will result in power levels between these two extremes. Because of the long thermal time constant of the load, a relatively smooth control of the temperature will result even though it is, in effect, being varied in 250 discrete steps. By choosing a longer period, say ten seconds (500 cycles), a finer control in 500 discrete steps will be possible. As long as this period is much shorter than the time constant of the heater and enclosure, but contains enough mains cycles to enable a sufficient number of steps to be accommodated, smooth control of power will be possible allowing the temperature to be set to the required value and accuracy.

This kind of control (known as Burst Fire control) is used to achieve very accurate temperature control of enclosures such as incubators or even rooms and can easily be implemented using a micro-controller. The 250 cycle time base can easily be generated by loading a register with 250 decimal (0FAh) and decrementing it every time that the positive zero crossing routine is called. After this, it can be compared to another register containing the fraction of the power which is to be passed to the load and when these are equal, the triac can be switched on.

No further comparisons are then required and the first register will continue to count down at every positive zero crossing until it reaches zero where it will be re-loaded 250 and the triac switched off (trigger current terminated). Thus if the second register contains 100 decimal, the triac will remain off for the first 150 mains cycles and on for the next 100 cycles resulting in 40% power. Varying the contents of this register would allow the power in the load to be varied between 0 and 100% in 250 discrete steps.

The value in the second register may be incremented or decremented using the INCF or DECF instructions in response to the two switches to set the power to any required value. It can also be changed depending on the temperature as sensed by a thermistor connected to an A/D converter. The latter could be implemented by software (plus a few external components) using the PIC16C54 or the built in A/D converter in the PIC16C71 used instead.

Dimming

The routine outlined above can be employed In applications where the load has a long time constant compared to a mains cycle, but if the load to be controlled is a lamp or small motor this would result in unacceptable flicker in the case of a lamp or a continuous variation in the motor speed as the motor slowed down between the pulses. In these situations a technique called phase control is normally employed. This, instead of switching the triac on for full cycles or even full half-cycles, switches it on for varying portions of each half-cycle by delaying the trigger pulses until some time after the zero crossing point.

The longer this delay, the less power is delivered to the load. If the triac is triggered into conduction 9mS after the zero crossing, it will only conduct for a further 1mS before the next zero crossing point is reached and the triac turns off, resulting in very little power reaching the load. Triggering the triac after 1mS will leave the triac conducting for 9mS resulting in almost full power.

To prevent lamps from flickering, the time delay after the zero crossing point in the positive and negative half-cycle must be (ideally) the same but because the triac is no longer switched on at or near the mains zero crossing point, large amounts of radio frequency interference will be generated which must be eliminated by filters consisting of chokes and capacitors. This becomes progressively more difficult and expensive as power levels are increased beyond about 500W so it is used only when other techniques would not be suitable.

Once we have obtained a mains zero crossing, dimming is not very hard to achieve and requires only a delay to be inserted after the zero crossing point in the program before the trigger pulse or pulses are generated. This is best done in the conventional way by loading a register with a number representing the brightness (i.e. the delay) required when the zero crossing is detected and counting down (at the micro-controller clock rate) until it reaches zero using the DECFSZ F,1 instruction. By changing the number, the brightness of the

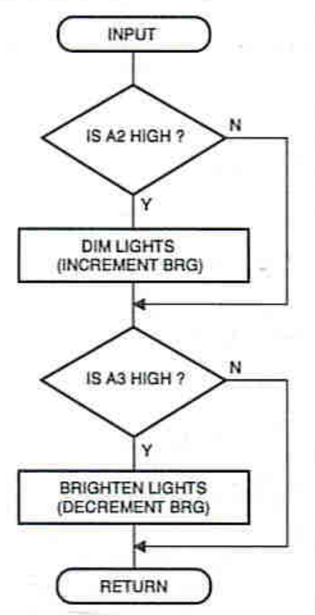

Fig 9b Input Subroutine

lamp can thus easily be changed.

As mentioned, the actual delay must be varied between 0 and just under 10mS in order to achieve a maximum variation of brightness from near zero (10mS delay) to full on. Since this depends not only on the number loaded into the counter but also on the time it takes to execute the DECFSZ instruction which in turn depends on the clock speed, it is a good idea to make the clock speed variable by replacing the resistor with a pre-set in series with a fixed resistor. This will enable the clock frequency and thus the delay to be 'fine tuned' so that the minimum brightness can be set at any level including off depending on the application.

The maximum number chosen should be greater than 32 decimal (i.e. 5 bits). This will then give a fine control over the brightness and a change of one count will be barely noticeable giving a smooth variation in brightness as the number is changed rather than a series of steps. This would require a rather low microprocessor clock speed and if more instructions must be carried out in a given application, a higher clock speed and larger numbers could of course be used.

Things are not quite so simple however because of the asymmetry in the zero crossing detector mentioned previously. As it stands, the zero crossing routine would not be suitable because of the automatic triggering of the triac in the negative half-cycle mentioned above. Since it is not now necessary to switch the triac on as soon after the zero crossing as possible and a minimum delay of even a millisecond will not make much difference, pulse triggering can be employed and the pulses can easily be counted to terminate the output once the full number have been generated.

Thus if the brightness is to be controlled in, say, 120 steps,

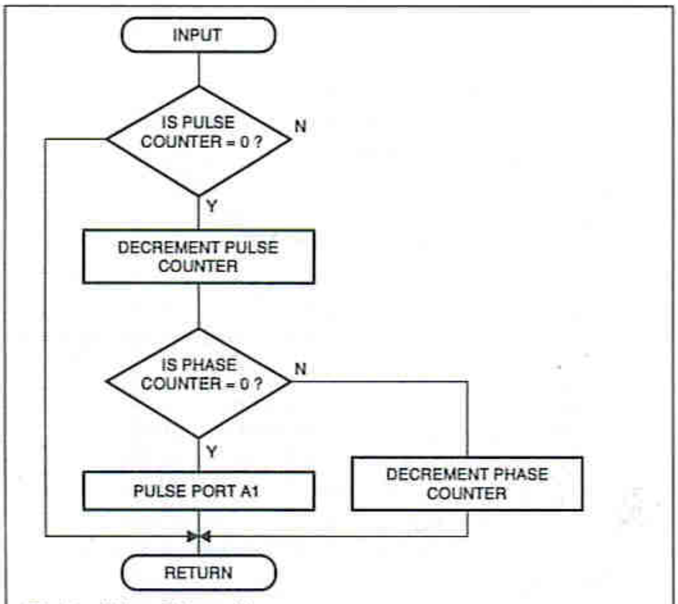

Fig 9c. Pulse Subroutine

the clock speed would be adjusted so that 120 trigger pulses could be generated in each mains half-cycle and these would be counted. Depending on the actual brightness required not all of these will actually be output on port A1 and if only a low brightness is required, the first 100, for example, would not be produced. The pulse count would continue however, and would reach 100 by the time that the first pulse was actually produced and the triac triggered. After a further 20 pulses, no more would be generated until the next zero crossing had been detected which would signal the beginning of the following half-cycle.

By adjusting the clock speed so that 120 pulses could be produced in say the 9mS following the zero crossing point, no trigger pulses will be generated in the last millisecond allowing the triac to turn off at the end of each half-cycle. Since the first and last millisecond of the mains half-cycle contribute less than 5% of the total available power in a cycle, this will still allow the power to be varied between about 3% and 97% of full power.

Figure 9 shows the flowchart for a dimmer programme which can be realised by plugging a suitably programmed chip into the circuit of Fig. 8. In this case, operating switch A2 will cause the brightness to increase while A3 will cause it to decrease rather than causing the light to switch on or off. Because of the smaller supply current requirements due to pulse triggering, C1 may be reduced to 0.1uF/250V a.c. Suitable suppressor components comprising a choke in series with the triac and a capacitor should also be fitted to this circuit if it is to be built as a permanent assembly.

The programme listing is shown in Fig. 10 and again is quite straightforward. This time three registers are defined; PHCTR, BRG and PLSCTR. BRG is the brightness register and holds the value corresponding to the current brightness required which, in this programme, has been set as 1 for full brightness and 120 for minimum brightness. PHCTR is the phase control counter which generates the delay prior to the first trigger pulse and is loaded with the value in BRG when a zero crossing is detected. PLSCTR is the pulse counter and is loaded with 120 during the zero crossing subroutine.

After the usual SET UP routine, the programme again reads A0 at label BEGIN to see if it is high. This time, if it is not, instead of going back to BEGIN it goes to BEGA where it first calls the subroutine PULSE which generates a pulse on A1 (bcf PORTA,1 and bsf PORTA,1) but only if the pulse counter PLSCTR has not yet reached zero (i.e. all 120 pulses have not yet been generated) and the phase delay counter PHSCTR has reached zero (ie. the time delay required before the first trigger pulse is produced has expired), before returning to BEGIN.

Otherwise both counters are decremented and the programme returns to BEGIN with no trigger pulse having been produced. (Note that once the pulse counter has reached zero, it is no longer decremented.) This happens continuously until the test on A0 is successful, when the programme calls the zero crossing routine ZRX where PHCTR and PLSCTR are loaded as mentioned above.

The INPUT subroutine is then called and depending on the status of inputs A2 and A3 the BRG register is incremented or decremented at the FADEDN and FADEUP labels or not altered if neither switch is pressed. This will cause the lamp brightness to decrease, increase or not to change. This routine is written so that BRG is not allowed to get to a value below 0 or above 120 (decimal). The programme execution then proceeds to label LOOP where it checks for the negative zero crossing, again calling the PULSE subroutine until this is detected when ZRX is again called and the programme returns to BEGIN.

The sky's the limit

With the brightness level of the lamp (or speed of the motor) now reduced to a number, the possibilities become endless. Numbers representing various brightness levels could be stored in a memory as a look-up table and recalled at the touch of a button to set the mood in your room to match any activity that you may have in mind! Or how about a sequencer to set the stage lighting levels to previously set levels for various scenes in your school play or amateur dramatics society? Or that up-market disco lighting rig which not only flashes the lights but also dims them ...

More interesting possibilities are opened up because the number representing the brightness is stored in a register (the brightness register) and the delay counter is loaded from this at each zero crossing point as in the above example. By incrementing or decrementing the counter the brightness level may be made to ramp up or down to any level. The speed at which the brightness level changes will of course depend on how often the counter value is changed and this could be done every mains cycle or every 50,000 mains cycles or more, providing ramp times of less than one second to over eight hours or more - try doing that with op-amps or one of the dimmer chips available on the market! In this circuit it can be done easily by altering the INPUT routine.

Assembler listing 1

```
;PICART1.ASM Zero voltage switch programme. A0 -
50Hz i/p; A1 triac drive
;A2 - ON i/p; A3 - OFF i/p - Fig 7
;*****************************************************
*********************
;
FLAG  equ 08h ; FLAG register
;
 LIST P=16C54
 include "PIC.h"
;*****************************************************
*********************
;
 goto START
;
;*****************************************************
*********************
;
ZRX   clrwdt                ;**********ZERO CROSSING
SUBROUTINE**************
 bsf PORTB,0                ; PULSE B0 (TEST PULSE)
 btfss FLAG,0               ; is flag 0 set?
 goto SWTOF                 ; no - switch off triac
 bcf PORTA,1                ; yes - switch on triac
 goto ZRXEND
;
SWTOF bsf PORTA,1            ;
ZRXEND                      bcf PORTB,0 ; END TEST
PULSE
 retlw 00
;
;*****************************************************
*********************
;
INPUT btfsc PORTA,2         ;*************INPUT
SUBROUTINE******************
 bsf FLAG,0                 ; A2 is high - set FLAG
0 high
 btfsc PORTA,3              ; is A3 low?
 bcf FLAG,0                 ; A3 is high - clear
FLAG 0
 retlw 00
;
;*****************************************************
*********************
;
START  nop
;
SETUP movlw 0Dh             ; ie 0000 1101 - make
portA 0 i/p except A1
 tris PORTA
 movlw 00h
 TRIS PORTB                 ; make PORTB o/p
(TEMPORARY)
 movlw 0FFh
 movwf PORTA                ; make A1 high
;
BEGIN btfss PORTA,0         ; A0 = 1?
 goto BEGIN                 ; no
 call ZRX                   ; yes - zero crossing
 call INPUT
LOOP  btfsc PORTA,0         ; A0 = 0?
 goto LOOP                  ; no
 goto BEGIN                 ; yes
;
;*****************************************************
*********************
 org 1FFh
 END
```

Assembler listing 2

```
;PICART2.asm - Fig. 10 (Triac drivers) This
programme is for a dimmer.
;A0 is the input input for zero crossing detector.
A1 is the output.
;A3 causes brightness to decrease while A2 causes
it to increase.
;PHCTR is loaded from BRG1 register at the
beginning of each half cycle
;and counts down to zero before producing a pulse
on A1 (DIMR subroutine)
;To change the brightness i.e. ramp up or down,
BRG register is incremented
;or decremented each time INPUT is read (once per
mains cycle).
;*****************************************************
*********************
;
PHCTR equ 08h ; PHase CounTeR1
BRG    equ 0Ch ; BRiGhtness register1
PLSCTR                       equ 1Bh ; PuLSe CounTeR
counts 120 steps ie. full ramp
;
 LIST P=16C54
 include "PIC.h"
;*****************************************************
*********************
;
 goto START
;
;*****************************************************
*********************
;
ZRX   clrwdt                ;**********ZERO CROSSING
SUBROUTINE**************
 bsf PORTB,0                ; PULSE B0 (TEST ONLY)
 movlw .120
 movwf PLSCTR               ; load pulse counter with
120 decimal
 movf BRG,w
 movwf PHCTR                ; load PHCTR from BRG
 bcf PORTB,0                ; END B0 TEST PULSE
;
;*****************************************************
*********************
;
PULSE clrwdt                ;*************DIMMING
SUBROUTINE****************
 movf PLSCTR,1
```

```
 btfsc STATUS,2              ; PLSCTR =0?
  retlw 00                   ; yes - no more trigger
pulses
  decf PLSCTR,1              ; no- decrement PLSCTR
  movf PHCTR,1
  btfss STATUS,2             ; PHCTR1 = 0?
  goto PULSE1                ; no
  bcf PORTA,1                ; yes - make pulse switch
on triac
  bsf PORTA,1                ; switch off triac
  retlw 00
;
PULSE1                       decf PHCTR,1; decrement
PHCTR
  retlw 00
;
;***********************************************
*********************
      ; **************FADE
SUBROUTINE*****************
;
FADEUP                       decf BRG,1  ; bit set -
brighten
  btfss STATUS,2             ; is BRG = 0?
  retlw 00                   ; no
  movlw 01                   ; yes - reload BRG with 1
  movwf BRG
  retlw 00
;
FADEDN                       incf BRG,1  ; DMDR bit
clear - fade down
  movlw .121
  xorwf BRG,w                ; is BRG = 121?
  btfss STATUS,2
  retlw 00                   ; not equal
  movlw .120                  ; equal - make it 120
  movwf BRG
  retlw 00
;
INPUT btfss PORTA,3          ; is A3 on?
  goto INPT2                 ; no - is A2 on?
  goto FADEDN                ; yes - fade DOWN
;
INPT2 btfss PORTA,2          ; is A2 on?
  retlw 00                   ; no
  goto FADEUP                    ; yes
;
;***********************************************
*********************
;
START nop
;
SETUP movlw 0Dh              ; i.e. 0000 1101 - make
portA 0 i/p
  tris PORTA
  movlw 00h
  TRIS PORTB    ; make PORTB o/p
  movwf PORTA
;
  movlw .60
  movwf BRG                  ; make BRG = 60 decimal
(half brightness)
;

BEGIN btfss PORTA,0          ; A0 = 1?
  goto BEGA                  ; no
  call ZRX                   ; yes
  call INPUT
LOOP  btfsc PORTA,0          ; A0 = 0?
  goto LOOPA                 ; no
  call ZRX                   ; yes
  goto BEGIN
;
BEGA  call PULSE
  goto BEGIN
;
LOOPA call PULSE
  goto LOOP
;***********************************************
*********************
  org 1FFh
  END
```

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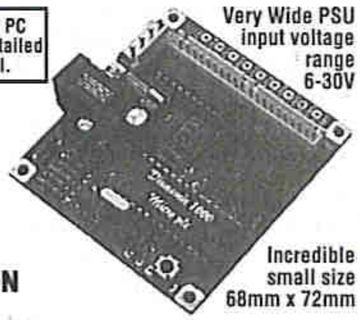

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using the I²C bus

Robin Abbott concludes his series on the ETI PIC BASIC microcontroller with an in-depth look at using the I²C bus

The I²C bus is a proprietary standard designed by Phillips/Signetics. It is used to provide low-speed serial communication between devices on a two-wire bus. It is used to great advantage with devices which traditionally have a large number of pins, and which can be fitted in to much smaller packages such as EEPROMs and RAMs in 8-pin DIL packages. In addition a large number of devices can be driven on a single two wire bus which reduces the I/O count on processor circuitry, and which eases PCB layout. This flexibility comes at the expense of increased interface complexity and of relatively slow transfers. In this article we shall look at the bus, and at the software which might be used to drive it.

Master and slaves

The I²C bus is a two-wire interface. Devices on this interface can be master devices, slave devices or both. There must be at least one master and any number of slaves (limited by the addressing range of devices).

Figure 1 shows a typical configuration with two master devices and three slave devices. The two wires on the interface are the clock line, SCL, and the data line, SDA. The master device controls the clock line SCL. Normally devices use open collector drivers on the I²C bus, and so the bus usually has a pull up resistor on SCL and SDA. This allows multiple devices to drive the bus simultaneously so that if two masters attempt to access the bus simultaneously then there is no excessive current drain. (See the later section on use of multiple masters for a further discussion of bus clashes.)

In any transfer of data there is always one device which acts as the master and one device which acts as the slave. The master device supplies the clock for the transfer, and defines which device is to be addressed, and whether the transfer is a read or a write access. The slave checks the address and, if it is correct, responds as defined by the master. In any transfer there will be 8 bits sent and one acknowledgement bit. The acknowledgement bit is always sent by the device which is reading from the bus. Thus, if the master is transferring data to the slave, then the slave device acknowledges; if the slave is transferring data to the master, then the master device acknowledges.

Bus states and data transfer

The idle state of the bus is defined by both the data and clock lines being high. If a multi-master system is in use, then it is normal for all master devices to tri-state the clock and data lines in the idle state. In a single master system, then the clock line is normally driven all the time. When the clock line is low then the data line can change without affecting the state of the bus, when the clock is high then the data line can only change to alter the state of the bus.

To gain control of the bus, a master device must issue a start condition. When it has finished with the bus, then it should issue a stop condition. A start condition is defined as the data line falling from high to low when the clock line is high; a stop condition is defined as the data line rising from low to high when the clock line is high. These state changes are illustrated in figure 2.

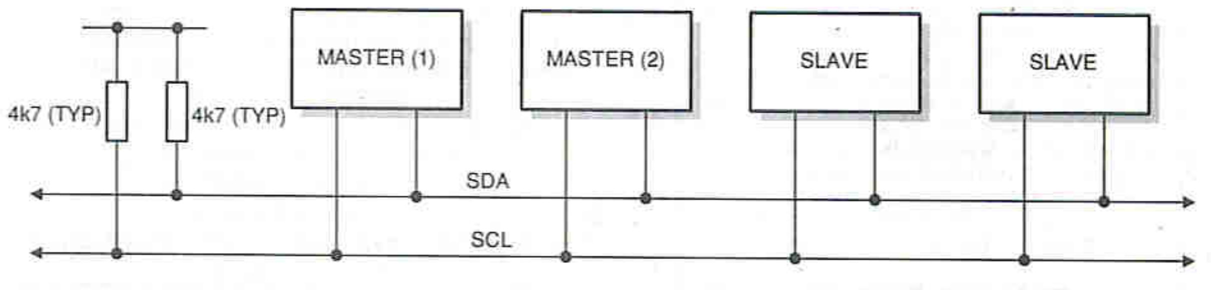


Fig 1. Typical I²C Bus Configeration

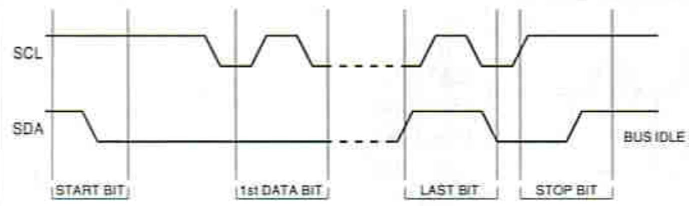


Fig 2. Start and Stop conditions

Once a start condition has been issued then the master device can initiate transfer of one or more bytes to or from the slave device. Data is transferred using the clock. Each clock pulse (defined as a high period of the clock) transfers a single bit. The data can change when the clock is low, but must stay stable whilst the clock is high. Data is transferred in 8 bits with the most significant bit transferred first. Following the 8 data bits, the master must issue one final pulse for the acknowledgement. The transfer of a single byte with an acknowledgement is illustrated in figure 3.

Addressing and controlling slave devices

Most I²C slave devices have an address which is sent by the master device immediately after the start bit. The address forms the first seven bits of the first byte. The final bit of the first byte transferred is normally the read/write bit which defines whether a read or write transfer is to be initiated. This bit is low to write, and high to read.

The address of slave devices usually has a fixed part and a variable part. The fixed part occupies the upper bits of the address and the variable part allows several devices of the same type to share the same bus.

The fixed part is the same for a group For instance I²C memory devices such as serial EEPROMs and serial RAM devices have a fixed address part of 1010 (binary).

The lower bits of the address (the variable part) can be selected using pins of the device. Some I²C devices have address pins, normally named A0, A1 etc. These pins can be connected to Vss or Vdd. Thus to define the address as 001 on a device with three address pins then A0 would be connected to Vdd, and pins A1 and A2 would be connected to Vss.

Some devices use the variable part of the address for internal decoding. For example, the 24LC16 EEPROM device uses the three variable address bits to provide the top three address bits of the EEPROM memory. Thus, there can only be one 24LC16 device on an I²C bus, and no other devices with the same fixed address part can share that bus, or the devices will clash.

Figure 4 shows a typical "real" circuit with three slave devices connected to a single master device. These devices are the 24LC65 serial 8Kx8 EEPROM, the 8570 256x8 serial RAM chip, and the 8573 real time clock/calendar chip. Note the address pin connections of the slave devices. These devices have the following addresses:

24LC65 - Fixed address 1010, variable part 001. Overall address is 1010001.

8570 - Fixed address 1010, variable part 000. Overall address is 101000.

8573 - Fixed address 11010, variable part 00. Overall address is 1101000.

So the sequence to read a byte from the LC65 shown in figure 4 is as follows:

Start Bit
Send the byte 10100011 (Read from address 1010001)
Receive single bit acknowledgement from the LC65
Receive byte from LC65
Send single bit acknowledgement to the LC65
Send stop bit

The acknowledgement bit sent by the slave is low if the slave device recognises the address and has acted on the command, and high otherwise. The acknowledgement bit sent by the master is low if further bytes are to be received, and high if this is the last byte read. This protocol is described further in the section below which describes using an LC65 device in detail.

Once a master device has control of the bus having sent a start bit and an address, then that master, and the addressed slave, can send or receive further bytes until a stop bit is sent and the bus returns to the idle state. The further bytes sent depend on the specific device. For example, an address and a write bit sent to the 8570 serial RAM is followed by a single 8 bit internal address which is the RAM address to be written, followed by one or more bytes to be written to that address and the following addresses sequentially.

Interface

Those who have been following the ETI PIC BASIC series will recognise the 24LC65 device as being the EEPROM used in all the variants of the project for 8K storage. We will look in detail at the interface used for this device as it is a good example of the use of the I²C bus, and there has been quite a lot of interest in using it for other applications. It is very likely that other 8Kx8 devices will have a very similar (or identical) interface.

The fixed address part of this device is 1010, and the variable part of the address is programmable from the address pins, A0, A1 and A2. In this example we'll look at a device which has pins A0, A1 and A2 wired to Vss. Thus up to 8 LC65 devices (or 8 devices which use the fixed address 1010) can connect to the same bus to provide up to 64Kx8 of EEPROM.

Figure 5 shows the sequence for writing a single byte to an address in the LC65. The start bit is followed by the address of the device together with the write bit (which is low to write); in this case the address byte will be 10100000. Now the next two bytes sent are the word address to be written, the high order byte first, followed by the low order byte. The high order address byte has only 5 significant bits, so the top three bits should be set to 0. Finally the byte to be written is sent to the LC65. The LC65 will acknowledge all four byte transfers with a low bit, following the last transfer a stop bit should be sent. Following the stop bit, the LC65 will initiate a write cycle. This takes 10mS during which time no further transfers can take place, although other devices on the bus can be addressed. The controlling program may either wait 10mS before attempting further access to the device, or can attempt a further transaction. If there is no acknowledgement from the LC65 then the write cycle is not complete.

More rapid writing to the EEPROM is possible using page writes. The LC65 contains an internal cache of 8 pages of 8 bytes each. Up to 64 bytes can be loaded at once by using the write command, followed by the address and then the bytes to be loaded to the cache. Each byte is transmitted in turn, followed by an acknowledgement from the LC65. The last byte is followed by a stop bit, after which each page of up to 8 bytes is written to the EEPROM array, each page taking 10mS to write.

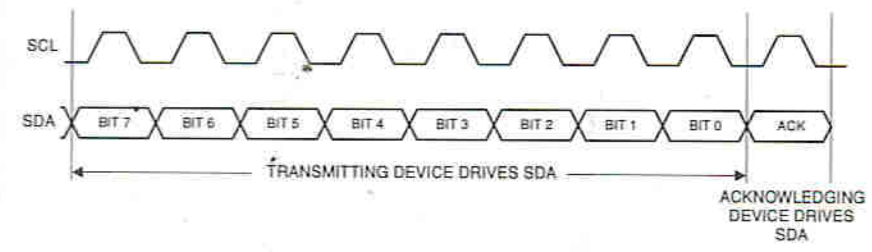


Fig 3. Transferring a complete bite

This allows writing at up to 8 times the speed of individual byte writes.

Figure 6 shows the sequence for reading a byte, or a sequence of bytes from the LC65. The first example shows the case where an address is to be provided and the byte read. The LC65 has an internal address counter and, after each byte is read from an LC65, the address counter is incremented to the next memory location. Thus it is possible to read out a number of locations with a minimum number of transfers. This is shown in the second example.

To set the address, a write cycle is initiated with the write definition byte - 1010 0000, followed by the address to be read in a transfer of the high order part. This is followed by the low order part as shown for the write operation. This sets the internal address counter. Following the second address byte transfer, a new start bit is sent by the master. This terminates the write operation. Now a read definition byte can be sent - 1010 0001 - and then finally a byte may be read from the slave device. Following the 8 bits read from the LC65 the master issues an acknowledgement. If this is low then the LC65 will send the contents of the next memory location when the master clocks out the next 8 bits. If the acknowledgement from the master is high, then the acknowledgement should be followed by a stop bit which will terminate transfer and leave the bus in the idle state.

To read the current address from the LC65 (and to increment the internal address counter afterwards), then the master can send a start bit, the read definition byte 1010 0001, and then read 8 bits followed by a high or low acknowledgement from the master dependant on whether further bytes are to be read.

Note that even running at 400KHz, the transfer times for the bus can be very slow due to the number of bytes which must be sent. Thus to read a single byte from a random address requires 5 bytes to be transferred, each of which needs 9 bits, plus a start and a stop bit for the whole transfer. This totals around 120uS. If use can be made of sequential mode then each byte can be read in around 25uS. For comparison, a 2MHz Z80 can achieve an 8 bit read from the data bus in 5uS.

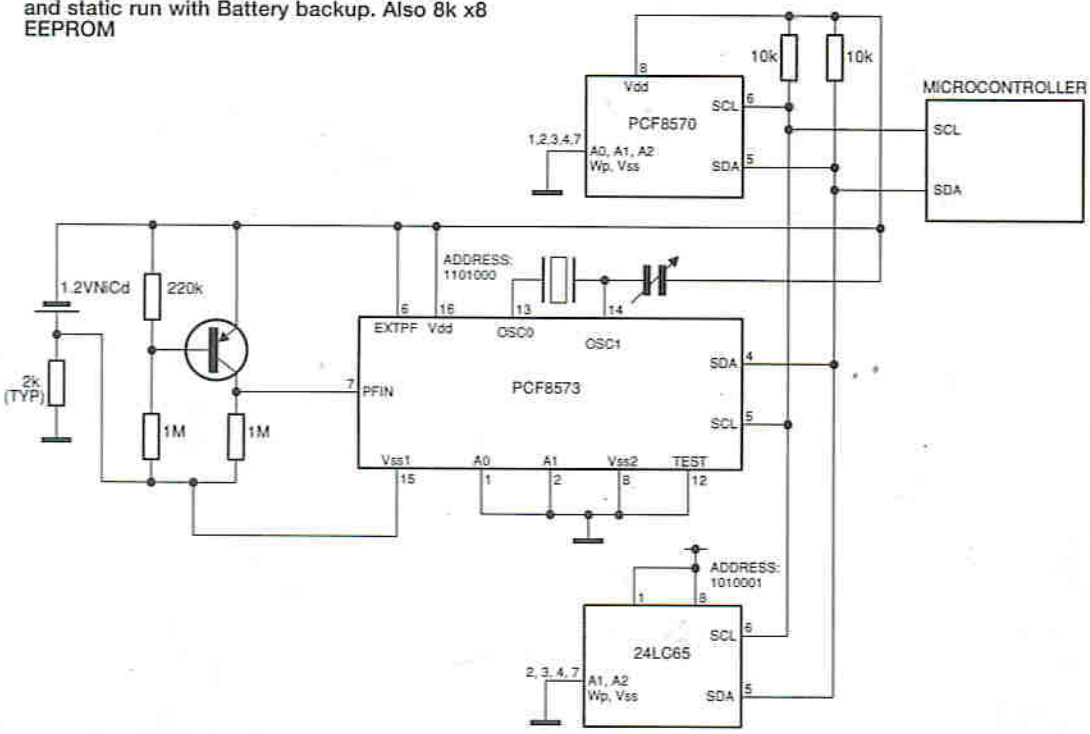
Using program control for the bus is almost inevitably slower, and for 4MHz versions of ETI PIC BASIC, the sequential read time is around 50uS and the random read time around 300uS. The random read is needed for program jumps, and for when EEPROM variables are read, (after an EEPROM variable read, a random read is then required for the continuation of the main program). For EEPROM variable writes then the 10mS delay swamps the bus access delays.

Driving the I²C bus from a microcontroller

Most I²C buses will be driven from a microprocessor. Although devices exist to convert an 8 bit parallel bus interface into an I2C bus interface, this does rather spoil the point of the two-wire interface! For the purpose of this article we shall look at the central routine used in the PIC16C64 version of ETI PIC BASIC, for the interface to the serial EEPROM, serial RAM, and the peripheral I²C interface. Familiarity with PIC assembler is assumed; however the routine is fairly straightforward. The main instruction type which may not be familiar to other assembly programmers is the PIC assembler BTFSS and BTFSC instructions. These instructions stand for Bit Test File register and Skip if Set (or Clear), thus "BTFSC temp,2", tests bit 2 of the memory location temp and, if it is 0, then the next instruction is ignored. The FSR register is the indirect address - anything written to, or read from, register 0 will use the address in FSR. Finally, the BSF and BCF instructions set and clear a bit in the specified registers respectively.

This routine is shown in figure 7 and occupies 54 words of program memory. The routine writes or reads 8 bits to the I²C bus, and can send a start bit and/or a stop bit, or neither. For this routine, there are two buses used; one is the EEPROM/RAM bus used by PIC BASIC, and the

Fig A. Example I2C circuit. Real time clock and static run with Battery backup. Also 8k x8 EEPROM



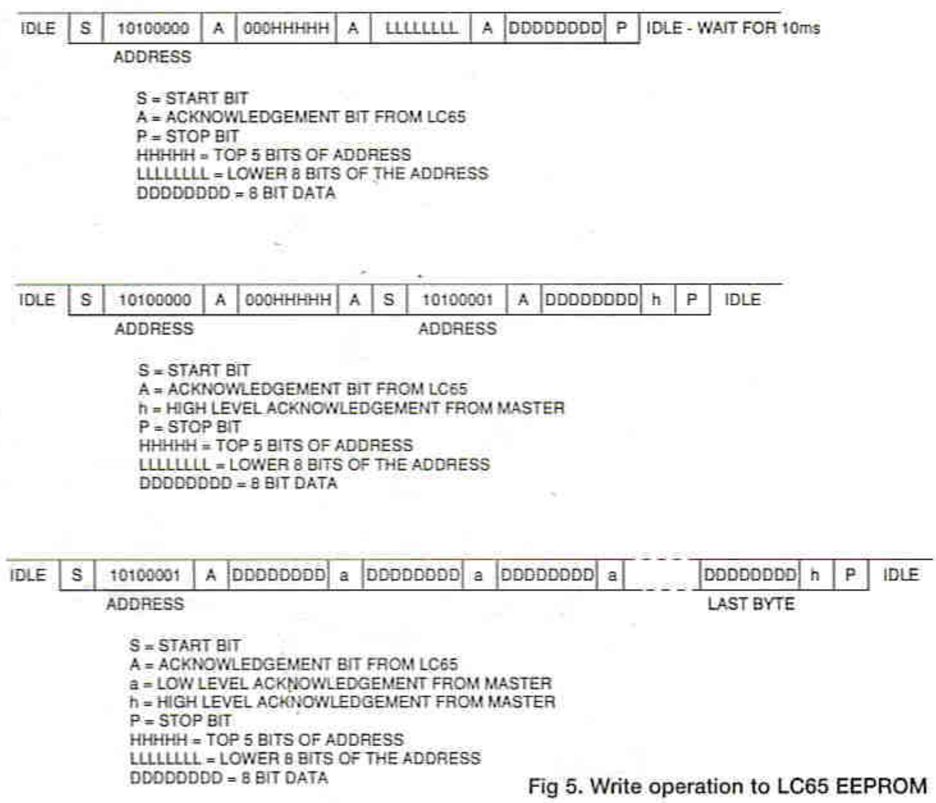


Fig 5. Write operation to LC65 EEPROM

other is the peripheral I^2C bus. The EEPROM/RAM bus uses bits 3 and 4 of port C, the peripheral I2C bus uses bits 3 and 4 of port A. Selection between the buses is performed by using the FSR register to point to the port to be used for the transfer. There are four entry points, which are all called with the W register holding the value to be written to the slave device in a write transfer (in a read transfer, the W register is ignored).These entry points are as follows:

1 - weeprom0w sends a start bit and transfers 8 bits to or from the EEPROM/RAM bus
2 - weepromns sends no start bit and transfers 8 bits to or from the EEPROM/RAM bus.
3 - I^2C0w sends a start bit and transfers 8 bits to or from the EEPROM/RAM peripheral I^2C bus.
4 - I^2C0w sends no start bit and transfers 8 bits to or from the EEPROM/RAM peripheral I^2C bus.

To read from the bus, the SDA bit should be defined as an input on calling the routine; to write, the SDA bit should be set to drive. The routine always returns with the SDA line driving as an output, and driving high after the last clock. The SCL line should be set to drive on calling the routine. On return the SCL line will be low unless a stop bit was requested, in which case it will be high. Three temporary variables are used: temp5, temp6, and temp7. temp6 is used to define the functions of the routine. If bit 1 of temp6 is set then a stop bit will be generated after the transfer, if bit 2 is set then an acknowledgement will be generated by the master, otherwise an acknowledgement will be read. Bit 3 defines a read from the slave if it is set; a write otherwise. temp5 holds the state of the acknowledge signal read from the slave device when the routine returns. Finally, temp7 holds the byte read from the slave in a read transfer.
Figure 8 shows the routines from PIC BASIC which handle the LC65. These are not fully documented here, but the three functions are as follows:
1 - eereadrand. This routine takes the address (which is in the location pointed to by FSR) and reads a byte from that address leaving the bus ready to read the next byte sequentially.
2 - eereadnext. Following the eereadrand routine this reads the next byte from the EEPROM and leaves the bus ready to read the next byte sequentially.
3 - eewrite. This writes a byte to EEPROM. The address (which is in the location pointed to by FSR) has the byte in the memory location tos written to it.
These routines need additional variables defined: temp3, temp4 and tos.
Note that timings for the bus are met for the LC65 with a 4MHz clock. Faster processor clocks will require nop instructions between clock changes to maintain the clock high and low and data setup and hold requirements detailed in specific data sheets.

Multiple master systems

In a multiple master system, operation follows the same procedures as shown above, except that the master devices must keep track of other devices which are using the bus, and wait when another device is accessing the bus. For microcontroller applications, this requires implementation of hardware to detect the start and stop bits. Fortunately the PIC16C64 contains the slave circuitry required to do this. There is still the possibility of a clash if two mastering devices try to access the bus simultaneously. In this case, each master must monitor the bus and in the case that one is sending a high state whilst the other is sending a low state on the SDA line, then the master sending the high state should yield to the other device.

```
; Write/read 8 bits to IIC, check ack
; Call weeprom0w for start bit to the local IIC
bus
; Call weepromns for no start bit to the local IIC
; Call IIC0w for start bit to the peripheral IIC
bus
; Call IICns for no start bit to the peripheral
IIC bus
; Call with scl driving
; sda is set to read for a read, and drive for
write
; temp5 is index, but returns state of ACK bit
; temp6 bit 0 is not used; temp6 bit 1 indicates
to generate stop
; temp6 bit 2 indicates to generate ack if set
(Read ack if reset)
; temp6 bit 3 indicates to read
; temp7 reads input byte, or writes output byte
; Ends driving sda & scl

IIC0w            bcf iicbus,sda         ; Start
bit call point
IICns            movwf temp7
                 movlw iicbus
                 goto doiic
weeprom0w        bcf picio,sda          ; start
bit drops data
```

```
weepromns        movwf temp7
                  movlw picio                  ; Move
default bus to FSR
doiic            movwf FSR
                  movlw 8
                  movwf temp5
                  bcf 0,scl                    ; drop
clock
                  btfsc temp6,3                ; leap
forward if read
                  goto rdeelop
;
wrteelop         bcf 0,sda                    ;This
writes 8 bits to the IIC
                  rlf temp7                    ; now
get correct port bit
                  skpnc                        ;
                  bsf 0,sda                    ;
                  bsf 0,scl                    ; clock
now high
                  bcf 0,scl                    ; clock
low again
                  bcf 0,sda                    ; No
clash with ack on last bit
                  decfsz temp5                 ; and
loop
                  goto wrteelop                ;
                  goto endthis
;
rdeelop          clrf temp7                   ; This
reads 8 bits from the IIC
                  clrc
rdee2            bsf 0,scl                    ; clock
now high
                  btfsc 0,sda                  ; now
read input
                  setc                         ;
                  rlf temp7                    ; Read
in bit
                  bcf 0,scl                    ; clock
low again
                  decfsz temp5                 ; and
loop
                  goto rdee2
;
;
; This section handles the last bit (acknowledge
or read ack), and handles stop
;
endthis          bcf 0,sda              ;
Acknowledgement is low
etstop           bsf FSR,7              ; either read
or drive SDA
                  bsf 0,sda              ; Read from
data line
                  btfsc temp6,2
                  bcf 0,sda              ; Now drive
data line if ack
                  bcf FSR,7
                  bsf 0,scl              ; Send the last
clock
                  btfsc 0,sda            ; Test state of
acknowledgement bit
                  incf temp5             ; and if 1,
then leave in temp 5
                  bcf 0,scl
                  bsf 0,sda              ; Data line
high
                  bsf FSR,7              ; End by
driving the data line
                  bcf 0,sda
                  bcf FSR,7
                  btfss temp6,1                ; 1/2
                  return                       ; 1
If no stop bit return with scl low
dostop           bcf 0,sda                    ; Call
here to do a stop bit
                  bsf 0,scl                    ;
otherwise clock high
                  bsf 0,sda                    ; If
stop return driving high on scl/sda
                  return
```

Figure 7 - 8 bit transfer routine for the I2C bus in the PIC BASIC project

```
; Read a random byte from EEPROM - address pointed
to by FSR return in temp7 & w
eereadrand       call eewrtadd                ; set
write address
                  movlw 4
                  movwf temp6                  ; read,
ack & start bit
                  movlw 0A1h
                  bsf picio,scl                ; drive
clock high for start bit
                  call weeprom0w               ; Write,
ack & start bit

; Read next byte from EEPROM return in temp7 & w

eereadnext       tstf cpc                     ; First
see if we moved from lower to
                  skpz                         ;
upper EEPROM
                  goto dordnxt                 ;
when address will be 2000h
                  movlw 20h
                  xorwf cpch,w
                  skpnz
                  goto eereadrand              ; Set
address to upper EEPROM
dordnxt          bsf STATUS,RP0               ; Read
from data line
                  bsf picio,sda
                  bcf STATUS,RP0
                  movlw 0ch
                  movwf temp6                  ; read,
ack, no start or stop
                  call weepromns               ; read
byte
retee            movfw temp7
                  return

; Write a byte to EEPROM, address in FSR, byte in
TOS

eewrite          call eewrtadd
                  movlw 6
                  movwf temp6                  ; ack &
stop bit
                  movfw tos
                  goto weepromns               ; No
start bit

; Write address part of read or write algorithm;
This routine leaves the address written in temp3
(L) and temp4 (H)

eewrtadd         movfw 0
                  movwf temp3                  ; save
the lower address
                  INCMEM FSR                   ; Now
the upper byte
                  movfw 0
                  movwf temp4                  ; Upper
address in temp4
                  call quikstop                ; Set
bus to stop state
                  movlw 4
                  movwf temp6                  ; ack &
start bit
                  movlw 0A0h                   ;
control byte
                  btfsc temp4,5                ; Test
upper lc65 bit
                  movlw 0A2h                   ;
Control byte for upper lc65
                  call weeprom0w               ; write
control byte with start bit
                  movfw temp4                  ;
address upper
                  call weepromns
                  movfw temp3
                  goto weepromns               ; ack,
no start bit
```

Figure 8 - Use of general purpose IIC routine by PIC BASIC

HUGHES MICROPHONES

George Pickworth continues his look at early microphone designs

PART 2

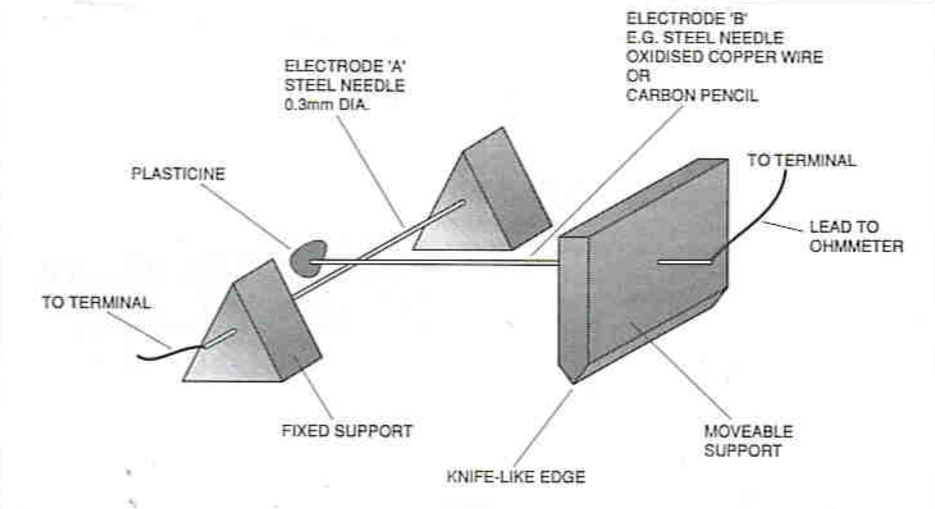


Fig 1. Experimental Loose-Joint based on a design used by Branly

In last month's issue of ETI, we looked at the broad principles behind some early electric devices - in particular, Hughes or loose joint microphones. Here we examine some more devices.

Two electrode microphones : self-restoring types

A. Hughes' needle & coke
This seems to be the earliest example of a Hughes' microphone. One electrode was a steel needle arranged so that the point just rested on a piece of coke.

B. Hughes' carbon pencil/steel needle (Fig 3)
This consisted of a carbon "pencil" resting across a horizontal steel needle. The carbon pencil was attached to a springy metal strip and contact pressure could be adjusted by means of a micrometer screw.

C. Hughes' oxidized copper wire/steel needle (Fig 4)
This consisted of a loop of fine copper wire that had been smoked and oxidised in the flame of a spirit lamp. The inside of the loop rested against a steel needle. My reproduction employed an arrangement to vary contact pressure.

D. Lodge's aluminium/steel needle (Fig 5)
This consisted of a steel point resting on an aluminium plate. My replica consisted of a strip of springy aluminium, cut from a beer can, resting against a needle point.

E. Hughes' platinum wire/mercury/steel point
This consisted of a steel needle with the point just touching the surface of a globule of mercury contained in a tiny ebonite cup. A platinum wire immersed in the mercury formed the other terminal. This microphone evolved into the Italian Navy Detector and the Lodge-Muirhead Detector.

Three element devices: self-restoring

A. Italian navy detector (Fig 6)
This consisted of a glass tube with steel plugs at both ends, or steel at one end and carbon on the other end. A globule of mercury was inserted between the plugs.

In some designs the inner faces of the plugs were ground off at an angle, so that by axially rotating the tube, contact area could be varied; this, of course, altered the height of the mercury globule and thereby contact area and pressure.

Some designs had one electrode attached to a micrometer screw so that the actual gap width could be

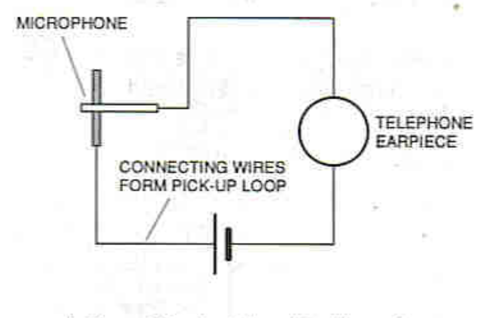


Fig 2. Representation of Hughes' hand-held receiver

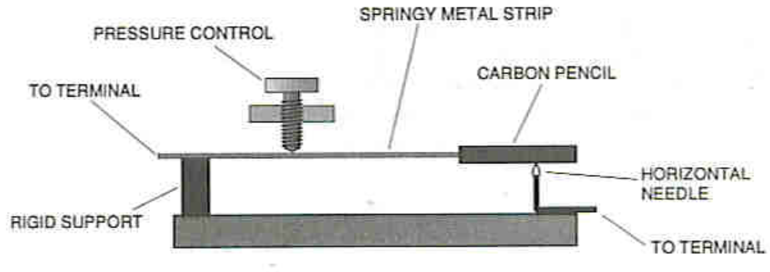


Fig 3. Reproduction of Prof Hughes' carbon/steel detector

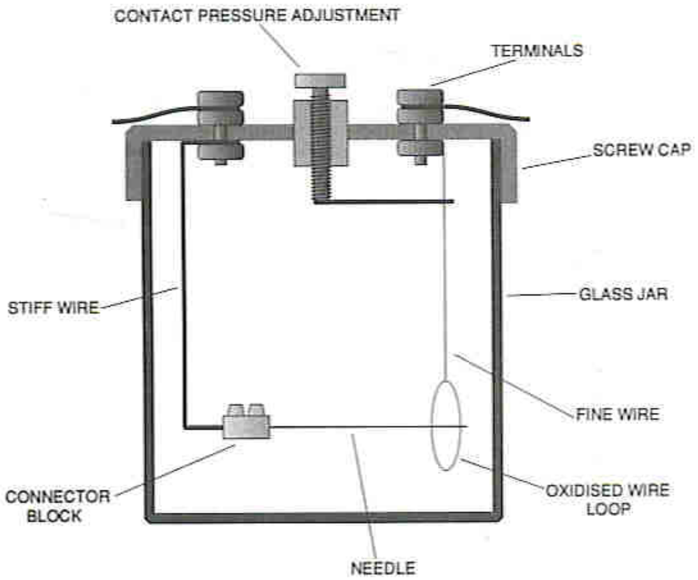


Fig 4. Reproduction of Prof Hughes' oxydised-wire-loop detector

varied. Alternatively, the tube was mounted on a pivot so that its angle of inclination could be varied.

B. My steel/aluminium/steel design

This consisted of a length of aluminium foil rolled into thin tube which rested on a pair of horizontal steel needles. Contact pressure was adjusted by varying the weight of the foil tube.

C. Massie's oscillophone (Fig 7)

This consisted of two carbon blocks filed to give the tops a triangular cross-section. A steel needle rested on the sharp edges. A small permanent magnet or alternatively an electromagnet caused a slight downward pressure on the carbon rods. Contact pressure could be adjusted by varying the position of the permanent magnet, or the current through the electromagnet.

Mechanically restored devices

Lodge's steel/platinum point detector (Fig 8) consisted of a length of clock spring firmly anchored at one end. A platinum point rested lightly on the spring and contact pressure was varied by means of a micrometer screw. Restoration was by causing the spring to vibrate by means of a clockwork motor and a ratchet wheel; it was not a success.

The Lodge-Muirhead detector (Fig 9), also known as a coherer, had its roots in Hughes' steel point/mercury detector but the steel point was replaced by a small steel disc with its circumference ground to a knife-like edge; it rotated at about 1.0 rev/sec. A thin film of oil covered the surface of the mercury which was just tipped by the edge of the disc.

Three principal hypotheses for the operation of microphones are based on an oxide film forming on metal electrodes. As already mentioned, this has a resistance so high that it behaves as an insulator with dielectric strength of about 10V; the same probably applies to the oil film of the Lodge-Muirhead detector.

However, carbon/carbon electrodes were apparently used by some pioneers; here the oxide film theory falls down as carbon oxides are, of course, gases but, having said that, my replicas responded very feebly.

A popular explanation for the operation of the Lodge-Muirhead detector is that the trigger pulse set up an electrostatic force which squeezed the oil dielectric from between the disc and mercury, thereby allowing the disc to make actual contact with the mercury. The dielectric healed as the disc rotated, thereby restoring the device to its high resistance state.

With regard to microphones with metal/metal or metal/carbon, one theory is that electrostatic forces produced by the trigger pulse increase the electrode contact pressure to the point where the oxide dielectric is ruptured. However, assuming electrostatic forces could create sufficient pressure, the question remains as to what could maintain this pressure when electrostatic forces are no longer present.

Resistance coefficient

Another possible explanation is that the resistance of the oxide film has a negative coefficient of resistance with regard to change in temperature. So, provided that the trigger pulse has a potential high enough to puncture the

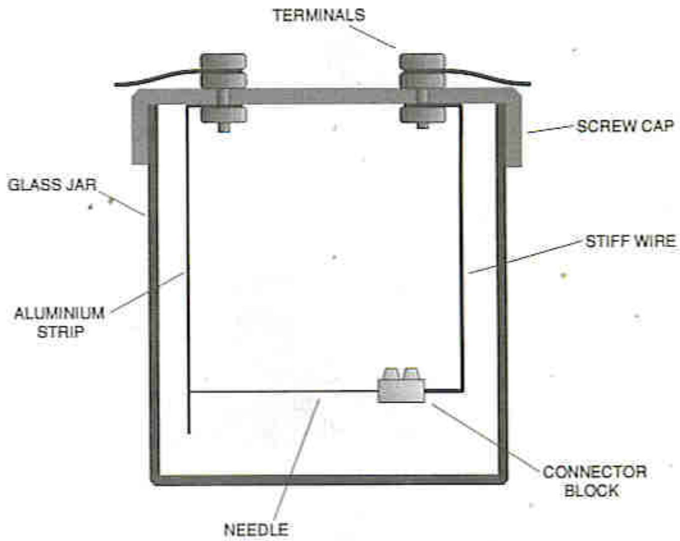


Fig 5. Reproduction of Lodges steel point/aluminium detector

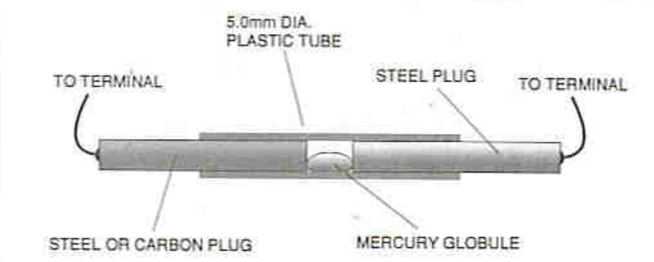


Fig 6. Reproduction of Italian Navy detector

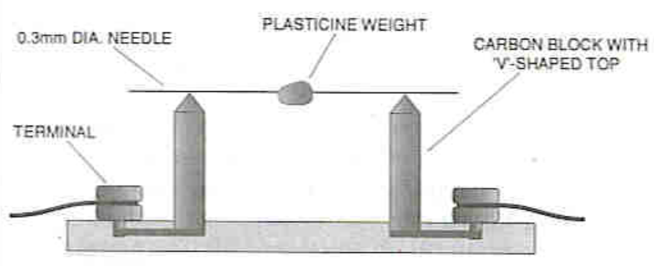


Fig 7. The Massie oscillophone detector

dielectric and allow local DC to flow across the joint, heating occurs and this reduces the resistance of the oxide film.

However, I found that the microphone's resistance falls in response to a trigger pulse even when not connected to a local DC source and remains low even when the local DC is repeatedly switched off and on.

Welding

An explanation favoured by myself is that the induced pulse punctures the oxide film and causes the electrodes to fuse or weld together; this could explain restoration by slight vibration which would break the weld.

It might seem unrealistic that the minute amount of energy needed to trigger the microphone could cause welding, but it must be remembered that the contact area is almost microscopic.

It is perhaps difficult to reconcile welding with metal/carbon electrodes, but vaporised metal may well condense on the carbon electrode.

Welding is, of course, out of the question with the steel/mercury, Italian Navy type detector, but as already mentioned, this is a strange device!

Immune

Remarkably, the near-field of the high power VLF transmitter BGR, Rugby, had no effect on my replicas of Hughes' hand-held receiver. Yet, in this environment, the microphones were instantly triggered by a single wave train radiated by the piezo energised transmitter at a distance of 20m. The piezo excited transmitter is described later (Fig 11).

Presumably, the peak potential of sine waves induced by GBR was much less than that induced by the piezo energised transmitter. However, the input to the radiator of transmitter was only about 12mJ so the actual energy induced in the hand-held receiver was minute.

Branly's experiments

It was mentioned in part 1 that in his paper entitled "Variations in Conductivity under Electrical Influence" (1891) Branly described how the resistance of a loose joint dropped from almost infinity to a few ohms when exposed to electrical influence.

To produce the electrical influence, Branly employed a two-plate Holzt machine (static machine). The Leyden jars normally attached to the machine were replaced by a pair of 150mm diameter brass tubes 400mm apart and with a length estimated to be about 1.0m; these are referred to as "horns" The spark-gap knobs were 0.5 - 1.0mm apart(see Fig 10).

Branly placed the loose-joint between the horns and connected it to one arm of a Wheatstone bridge. When the plates of the Holzt machine were rotated, an electric charge built up in the horns and ultimately discharged across the spark gap; the result was that the resistance of the loose joint instantly dropped from almost infinity to a few ohms.

Branly's influence machine was obviously a small VHF transmitter which foreshadowed Hertz's transmitter. So, the electrical influence was obviously electric and magnetic. Branly perceived the joint responding directly to the electrical influence.

Reproduction

As Holtz machines are hard to come by, my reproduction of Branly's "influence generator" was energised by a piezo electric gas igniter; this not only simplified construction but

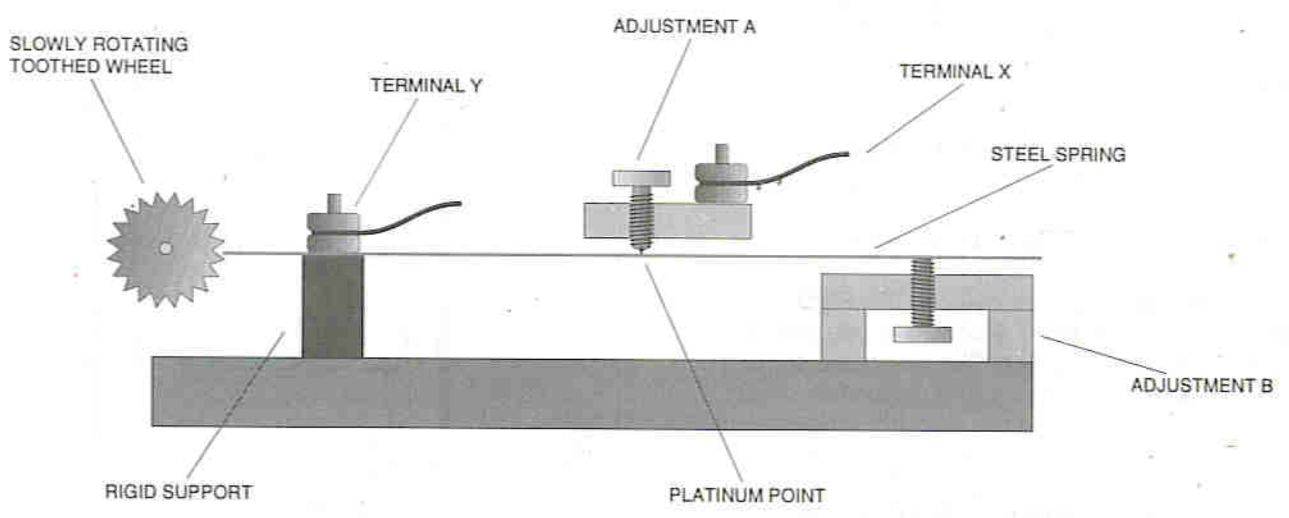


Fig 8. Lodges mechanically restored loose contact detector

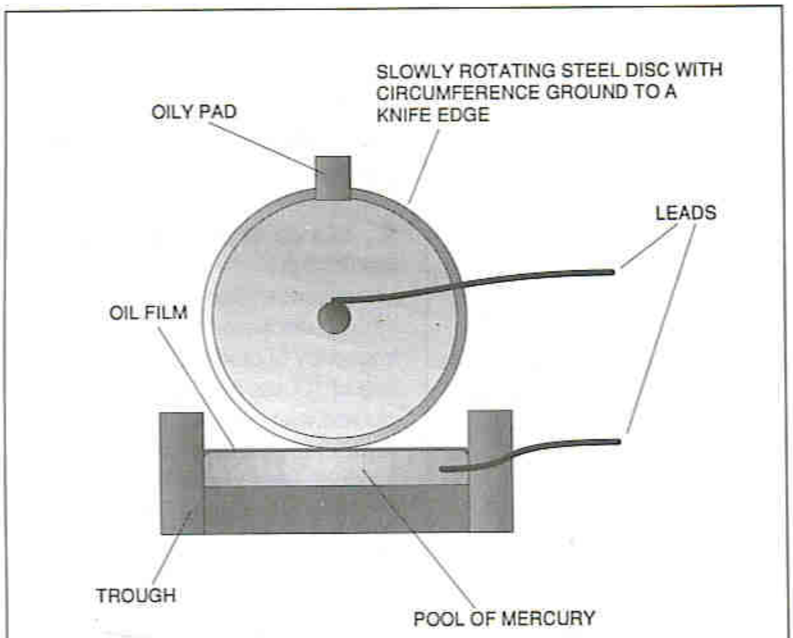


Fig 9. Simplified representation of the LOdge-muirhead detector

radio interference was reduced to a minimum as each discharge radiated only a single wave train.

British Gas informed me that gas-igniters release about 12mJ so the energy present in successive discharges was virtually the same.

Replica microphones were placed between the horns and connected to an ohmmeter. A single discharge caused its resistance to fall to less than 10Ω. The logical explanation is that a voltage pulse was induced in connecting wires and this triggered the loose-joint; moreover, this effect was maintained as the microphone was incrementally moved away from the horns up to a distance of 10m when the effect suddenly became erratic. At 15m there was no effect.

At distances between 10 and 15m there was either no effect or resistance dropped to less than 10Ω; it was rare for resistance to fall to some intermediate value.

Without local DC

A phenomena which does not seem to have been observed by Branly was that resistance drop still occurred when the ohmmeter (which provided the local DC) and its leads were not connected to the microphone; this effect was observed by reconnecting the ohmmeter after the microphone had been exposed to a discharge and could be repeated at a distance up to 7.0m from the horns. This experiment seems to rule out operation based on local heating.

Twisted connecting wires

Even more remarkable, resistance drop still occurred when the leads connecting the microphone with the ohmmeter were tightly twisted together. It is therefore not surprising that Branly seems to have believed that the microphone responded directly to electrical influence; indeed, I began to wonder myself if this could be the case.

Placed in a metal box

The microphone and ohmmeter were placed inside a metal biscuit tin. A small hole covered with fine metal gauze allowed the ohmmeter to be observed. As expected there was no response to discharges, but when the gauze was removed from the observation window, the microphone was readily triggered.

Microwaves

I assumed that my influence generator was radiating microwaves and these were unable to induce a pulse in the microphone's actual electrodes which served as an antenna. I also assumed that microwaves entered the metal box through the unscreened observation window.

Presumably, Branly's influence generator did likewise so Branly was probably quite right in believing that the loose joint responded directly to electrical influence.

Response to trains of very short waves

Whilst I favour the theory that Hughes' sender propagated energy along underground metal pipes, there was a possibility that his sender may have radiated microwaves and further experiments are planned to try and confirm this.

Whilst the following experiment could not confirm that Hughes' sender did radiate Hertzian waves, it did show that his handheld receiver could respond to trains of very short Hertzian waves. Moreover, it gave a good indication of the sensitivity of microphones.

Thanks to co-operation by the DTI, I was able to conduct a number of experiments in a fairly large, empty car park but the number of wave-trains radiated was the minimal necessary.

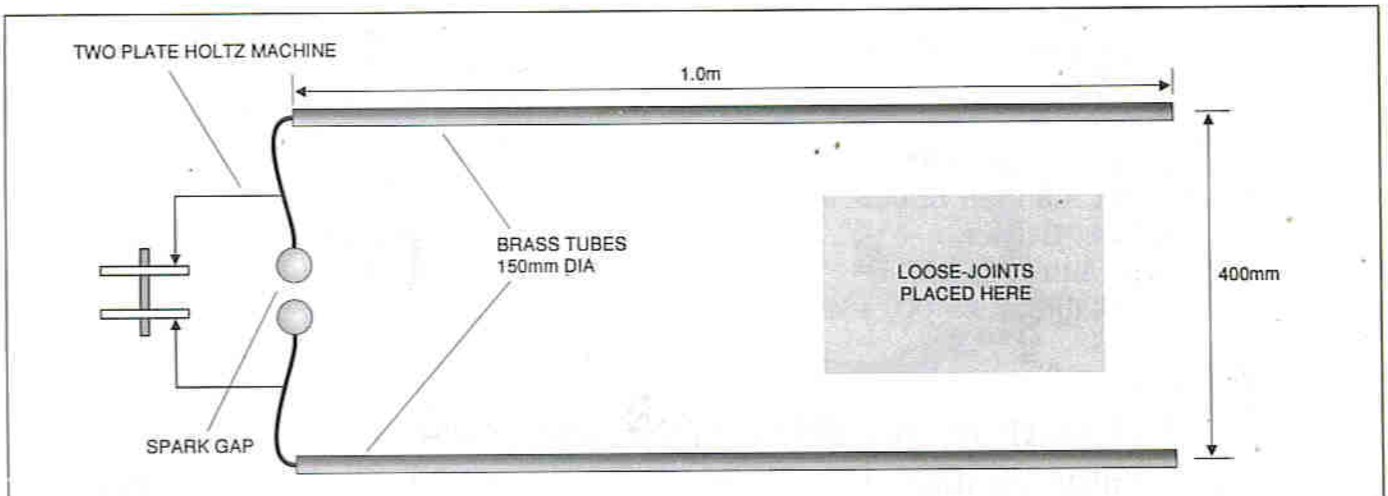


Fig 10. Simplified representation of Branlys' "Infuence Generator"

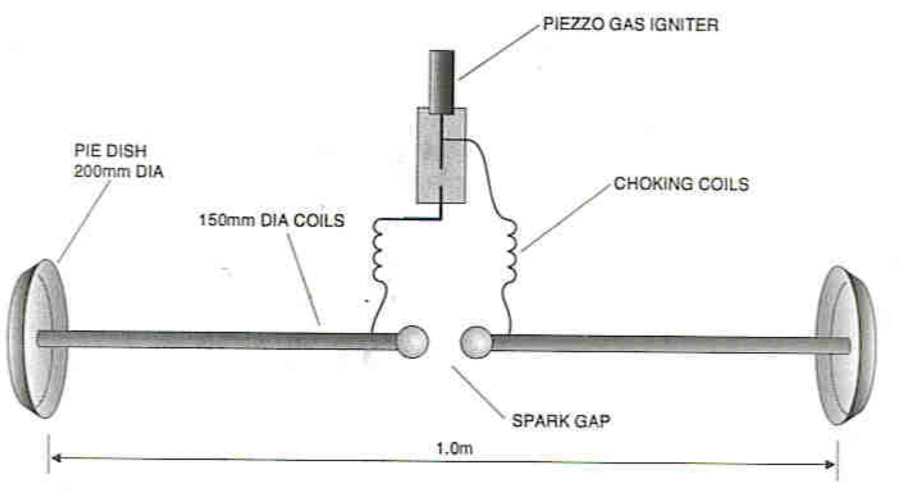


Fig 11. Representation of the Hertz-type transmitter employing the Piezo Gas Igniter

Sender

The horns of the "influence machine" were modified so as to be in line with each other. Fig 11. The fundamental wavelength was about 3.0m but was obviously rich in harmonics and probably microwaves.

My steel needle/aluminium strip microphone was taken as a representative example and range achieved with the radiation of a single wave train is plotted in Graph B. The potential of the induced trigger pulse was estimated from measurements described in Note A. The microphone was restored by lightly tapping with a pencil immediately before radiation of a wave train.

NOTE A: Measuring peak potential of the trigger pulse

A. Wave train generator method

My wave train generator was set up to produce wave-trains with a frequency of 50kHz and a repetition rate of 100Hz. The microphone to be studied was connected across the wave train generator's output terminals, and in parallel with the oscilloscope input terminals.
The wave train generator was first adjusted to produce wave-trains with a peak potential too low to trigger the microphone; it therefore placed virtually no load on the generator and a trace was observed on the oscilloscope screen.

Generator output voltage was then incrementally increased until the microphone was triggered; this effectively shorted the generator output and the oscilloscope trace disappeared.

B. Capacitor discharge method

A 2. OnF low inductance capacitor was incrementally charged and discharged through the microphone via a high speed electronic switch until triggering occurred.

the VIDEOCHECK PART 2

Bart Trepak concludes his construction of a device whch enables you to have compete control of the televison set

This programme is for a timed digital lock for disabling TV sets. At POR a preset 4-digit code (1111) is selected and a 24-hour timer is started together with another timer "A" which times 6 hours. Entering 1111 will turn on the output on and pressing * lights the programme LED. A new code can be entered followed by * to accept. LED will extinguish, but output will remain on until this new code is entered. Once the unit is in the programme mode, pressing # will move it to VIEW TIME mode allowing the number of minutes viewing allowed per evening to be changed. A three-digit number representing the number of minutes can be entered. The last three digits entered before the * or # is pressed will be accepted. The max number allowed is 359 i.e. three hours. Incorrect entries will generate 3 BLEEPs If # is pressed again, the unit will enter the TIME MODE which allows the real time to be set. This will accept 4-digit times in 24-hour format e.g. 0316 or 2237. Only valid times will be accepted which will be the last 4 digits before # or * is pressed. Incorrect entries will result in 3 BLEEPs. A general reset will occur at 9pm (2100hrs) when the relay will switch off unless the disarm code has been entered. If the TV is switched off during the allowed viewing time, the relay will not switch off allowing the TV to be switched on again, but if it is switched off during the disallowed time, the relay will also switch off. To switch on the TV in this case, the disarm code will need to be re-entered.

Videocheck Assembler Code

```
LKP equ 1Ch                  ; holds Last Key Pressed
HSCTR equ 08h                ; Half Second CounTeR
HRCTR equ 09h                ; HouR CounTeR (REAL
TIME)
MINCTR equ 0Ah               ; MINuite CounTeR (REAL
TIME)
MTMR equ 0Bh                 ; Minute TiMeR
QSTMR equ 0Ch                ; Quarter Second TiMeR
FLAG equ 0Eh                 ; FLAG register
FSTMR equ 0Dh                ; Five Second TiMeR
INCTR equ 1Dh                ; input counter used
during programming
CTR1 equ 1Eh                 ; holds delay value
) BEEP
CTR2 equ 1Fh                 ; which determines the
frequency) BEEP
;
CUST1 equ 10h                ;output open codes 1st
digit
CUST2 equ 11h                ; 2nd digit
CUST3 equ 12h                ; 3rd digit
CUST4 equ 13h                ; 4th digit
;
VTIM1 equ 14h                ; allowed viewing time
(MSD)
VTIM2 equ 15h                ; (NSD & LSD)
;
VCTR1 equ 16h                ; view time counter
VCTR2 equ 17h                ; view time counter
;
DLCTR1 equ 18h               ; DeLay CounTeR
DLCTR2 equ 19h               ; DeLay CounTeR
;
 LIST P=16C54;f=inhx16
 INCLUDE "PIC.H"
;**************************************************
 goto START
;
TIME decfsz QSTMR,same       ; ****TIME SUBROUTINE***
 goto T4                     ; if QSTMR is not zero
 movlw .12                   ;
 movwf QSTMR
;
 movf CTR1,same              ; controls BEEP generator
 btfsc STATUS,2              ; is CTR1=0
 goto T4                     ; yes
 movlw 01h                   no make BEEP
 xorwf PORTA,same            ; compliment A0
 decf CTR1,same
;
T4    btfss FLAG,3           ; programming mode?
 goto T10                    ; no
 bcf PORTA,1                 ; yes - switch off clock
running LED
 retlw 00
;
T10   decfsz HSCTR,same
 retlw 00                    ; if not zero
 movlw .25
 movwf HSCTR                 ; reload HSCTR with 25 if
zero
;
FLASH movlw 02h              ; ie 0000 0010
 xorwf PORTA,same ; toggle A1 - flash led
 btfsc PORTA,2               ; is TV on ie. A2 low?
 goto LEDON                  no - switch on LED
 btfsc FLAG,6                ; yes - has code been
entered? ie F6=1
LEDON bsf PORTA,1            ; yes - switch on LED
;
T13   btfss FLAG,4           ; is 5 Sec timer
counting?
 goto T1                     ; no
 btfsc FLAG,3                ; is unit in programme
mode?
 goto T1                     ; yes - do not decrement
timer
 decfsz FSTMR
 goto T1
 bcf FLAG,4                  ; reset 5 sec timer flag
 bcf FLAG,7                  ; clear flag 7  - new key
 movlw 10h
 movwf FSR                   ; reset pointer to 1st
```

```
digit
;
T1    decfsz MTMR             ; MINUTE TIMER
 retlw 00                     ; if minute timer is not
zero
 movlw .120
 movwf MTMR                   ; reload minute timer
with 120 dec
;
 btfsc PORTA,2                ; ***ROUTINE TO COUNT
                                TIME IF TV ON***
 goto T6                      ; TV is off
 btfsc FLAG,6                 ; TV on but is code
entered?
 goto T6                      ; yes - viewing permitted
 decf VCTR2,same
 btfsc STATUS,2               ; VCTR2=00h?
 goto  T9                     ; yes - check if VCTR1=0
 movf VCTR2,w
 xorlw 0FFh
 btfss STATUS,2               ; VCTR2=0FFh?
 goto T12                     ; no
 decf VCTR1,same              ; decrement MSD
 movlw 99h
 movwf VCTR2                  ; make VCTR2 = 99
;
T12   movlw 0Fh               ; BCD ADJUST
 andwf VCTR2,w                ; mask upper nibble of
VCTR2
 xorlw 0Fh
 btfss STATUS,2               ; VCTR2 = xFh?
 goto T8                      ; no
 movlw .6                     ; yes - subtract 6 from
VCTR2
 subwf VCTR2,same
;
T8    movf VCTR1,same         ; LIMITED TIME ALARM
 btfss STATUS,2               ; VCTR1=0?
 goto T6                      ; no - still plenty of
time left
 movf VCTR2,w                 ; yes - hundreds counter
=0
 xorlw 10h
 btfsc STATUS,2               ; 10mins left?
 goto BP5                     ; yes - make 5 beep
;
 movf VCTR2,w                 ; no
 xorlw 05h
 btfsc STATUS,2               ; 5mins left?
 goto BP5                     ; yes - make 5 beep
;
 movf VCTR2,w                 ; no
 xorlw 04h
 btfsc STATUS,2               ; 4mins left?
 goto BP4                     ; yes - make 4 beep
;
 movf VCTR2,w                 ; no
 xorlw 03h
 btfsc STATUS,2               ; 3mins left?
 goto BP3                     ; yes - make 3 beep
;
 movf VCTR2,w                 ; no
 xorlw 02h
 btfsc STATUS,2               ; 2mins left?
 goto BP2                     ; yes - make 2 beep
;
 movf VCTR2,w                 ; no
 xorlw 01h
 btfss STATUS,2               ; 1mins left?
 goto T6                      ; no - go to clock
 movlw 14h                    ; yes - make 10 beep
BP    movwf CTR1
 goto T6
;
BP5   movlw 0Ah
 goto BP
BP4   movlw 08h
 goto BP
BP3   movlw 06h
 goto BP
BP2   movlw 04h
 goto BP
```

```
;
T9    movf VCTR1,same
 btfss STATUS,2               ; VCTR1=0?
 goto T8                      ; no
;
ENDTIM                        bcF PORTA,3 ; yes -
switch off relay
 bcf FLAG,5                   ; viewing disallowed
;
T6    incf MINCTR,same        ; CLOCK - MINUTES COUNT
 movf MINCTR,w
 andlw 0Fh                    ; ie 0000 1111 mask out
lower nibble
 xorlw 0Ah                    ; ie 0000 1010 (10
decimal)
 btfss STATUS,2
 retlw 00                     ; if MINCTR lower nibble
not ten
 movlw .6
 addwf MINCTR,same            ; add 6 (dec) to MINCTR
if equal to ten
;
 movf MINCTR,w                ; check if minute counter
has reached 60
 xorlw 60h
 btfss STATUS,2
 retlw 00                     ; MINCTR not 60
 clrf MINCTR                  ; =60 clear it
;
T2    incf HRCTR,same         ; CLOCK - HOURS COUNT
 movf HRCTR,w
 andlw 0Fh                    ; ie 0000 1111 mask out
lower nibble
 xorlw 0Ah                    ; ie 0000 1010 (10
decimal)
 btfss STATUS,2
 goto T5                      ; if HRCTR lower nibble
not ten
 movlw .6
 addwf HRCTR,same             ; add 6 (dec) to HRCTR if
equal to ten
;
T5    movf HRCTR,w            ; check if counter has
reached 15:00
 xorlw 15h
 btfss STATUS,2
 goto T7                      ; time is not 15:00
 movf VTIM2,w                 ; time is 15:00 - viewing
allowed
 movwf VCTR2                  ; reload VCTR2
 movf VTIM1,w
 movwf VCTR1                  ; reload VCTR1
;
 movf VCTR1,same              ; check if viewing time
has been set
 btfss STATUS,2               ; is VCTR1=0?
 goto T11                       ; no
 movf VCTR2,same              ; yes - is VCRT2 also =0?
 btfsc STATUS,2
 goto T7                      ; yes both VCTR1 and
VCTR2 are zero
T11   bsf FLAG,5              ; viewing time set -
enable relay
 bsf PORTA,3
;
T7    movf HRCTR,w            ; check if counter has
reached 21:00
 xorlw 21h
 btfss STATUS,2
 goto T3                      ; no -
 bcf FLAG,5                   ; time is 21:00 - viewing
NOT allowed
 btfss FLAG,6                 ; but if Flag 6 is not
set
 bcf PORTA,3                  ; switch off output
;
T3    movf HRCTR,w            ; check if hour counter
has reached 24
 xorlw 24h
 btfss STATUS,2
 retlw 00                     ; HRCTR not 24
 clrf HRCTR                   ; =24 clear it
```

```
;
KEYBD movlw 0F0h                ;
*KEYBOARD SUBROUTINE*
 TRIS PORTB                     ; change PORTB i/o pins
B0-B3 o/p B4-B7 i
;
 movlw 0Ah                      ; ie. 0000 1010
 movwf PORTB                    ; make B1 and B3 high
 nop
 btfsc PORTB,4
 retlw 81h                      ; skip if B4 clear
 btfsc PORTB,7
 retlw 84h
 btfsc PORTB,6
 retlw 87h
 btfsc PORTB,5
 retlw 90h
;
 movlw 09h                      ; ie 0000 1001
 movwf PORTB                    ; make B0 and B3 high
 nop
 btfsc PORTB,4
 retlw 82h                      ; skip if B4 clear
 btfsc PORTB,7
 retlw 85h
 btfsc PORTB,6
 retlw 88h
 btfsc PORTB,5
 retlw 80h
;
 movlw 0Ch                      ; ie 0000 1100
 movwf PORTB                    ; make B2 and B3 high
 nop
 btfsc PORTB,4
 retlw 83h                      ; skip if B4 clear
 btfsc PORTB,7
 retlw 86h
 btfsc PORTB,6
 retlw 89h
 btfsc PORTB,5
 retlw 0A0h
;
 retlw 00
;
;**************************************************
;
LDSPLY  movf FLAG,w             ;******LED DRIVER
SUBROUTINE**************
 andlw 07h                      ; ie 0000 0111 mask out 3
ls bits
 movwf PORTB
 call DLY
 retlw 00
;
;**************************************************
;
DLY   movlw 04h                 ; *************DELAY
routine***************
 movwf DLCTR2
DLY2  movlw 0FFh
 movwf DLCTR1
DLY1  decfsz DLCTR1
 goto DLY1
 decfsz DLCTR2
 goto DLY2
;
;**************************************************
MATCH movwf LKP                 ;****this subroutine
compares LKP with****
                                ;**CUST1,2,3 & 4
etc.********************
 btfss LKP,7                    ; is a key pressed?
 goto NOKEY                     ; no
 bsf FLAG,4                     ; set 5 sec timer flag
 movlw .10
 movwf FSTMR                    ; reload 5 sec timer
 btfsc FLAG,7                   ; has key already been
processed?
 retlw 00                       ; yes
 bsf FLAG,7
 btfsc FLAG,6                   ; has correct code been
entered?
 goto PROG                      ; yes - go to program
mode
;
CMPRE movf 0,w                  ; COMPARE reads in code
via pointer
 xorwf LKP,w                    ; compare with key
pressed
 btfss STATUS,2                 ; zero bit set if same
 goto ERROR                     ; if no match
 incf FSR,same                  ; if match point to the
next digit
 movlw 0F4h                     ; test if all digits
entered. Note if FSR
 xorwf FSR,w                    ; is loaded with 10 it
reads as F0h
 btfss STATUS,2                 ; all digits entered
correctly?
 retlw 00                       ; not yet
 movlw 40h                      ; ie. 0100 0000
 xorwf FLAG,same                ; correct code entered -
toggle flag 6
 clrf CTR1                      ; inhibit BEEP
 bcf PORTA,0
 movlw 08h                      ; ie 0000 1000
 btfss FLAG,5
 xorwf PORTA,same               ; if not allowed view
time - toggle o/p
 retlw 00
;
ERROR movlw 10h
 movwf FSR                      ; reset pointer if
incorrect key pressed
 retlw 00
;
PROG  btfss LKP,4               ; was * key pressed?
 goto PROG1                     ; no - test if # key
 btfsc FLAG,3                   ; is unit in program
mode?
 goto PROG2                     ; yes - end program mode?
 bsf FLAG,3                     ; set program mode
 bsf FLAG,0                     ; select PRGRAM CODE
 movlw 04h
 movwf INCTR                    ; load INCTR with 4
 movlw 10h
 movwf FSR                      ; initialise FSR register
 retlw 00
;
PROG1 btfsc LKP,5               ; was # key pressed
 goto PROG3                     ; yes - select next mode?
 btfsc FLAG,3                   ; is unit in program
mode?
 goto STORE                     ; yes - store entry in
next location
 goto CMPRE
;
ERRBP movlw 06h                 ; no - BEEP error
 movwf CTR1
 retlw 00
;
PROG2 movf INCTR,same
 btfss STATUS,2                 ; INCTR = zero?
 goto ERRBP                     ; no - error beep
ENDPRG                          movlw 0B0h  ; ie. 1011
0000
 andwf FLAG,same                ; clear FLAG 0,1,2,3 and
6
 movlw 10h
 movwf FSR                      ; reload pointer
 bcf PORTA,3                    ; switch off relay
 bcf FLAG,5                     ; switch off VIEWING
ALLOWED flag
;
 movlw .120
 movwf MTMR                     ; reset minute timer when
leaving prog mde
;
 movlw 21h                      ; CHECK IF 15:00 < HRTMR
< 21:00
 subwf HRCTR,w                  ; if HRTMR < 21 then C=1
 btfsc STATUS,0
 retlw 00                       ; time past 21:00
 movlw 15h                      ; time not yet 21:00
```

```
 subwf HRCTR,w              ; if 15 < HRTMR then C=1
 btfss STATUS,0
 retlw 00                   ; time not yet 15:00
;
 movf VTIM1,w               ; time is passed 15:00
but before 21:00
 movwf VCTR1                ; load VTIM1 & VTIM2 into
VCTR1 & VCTR2
 movf VTIM2,w
 movwf VCTR2
 movf VCTR1,same
 btfss STATUS,2             ; VCTR1=0?
 goto PROG6                 ; no
 movf VCTR2,same            ; yes - test VCTR2
 btfsc STATUS,2             ; VCTR2=0?
 retlw 00                   ; yes
PROG6 bsf PORTA,3           ; no - switch on relay
 bsf FLAG,5                 ; and enable VIEWING
ALLOWED flag
 retlw 00
;
PROG3 btfss FLAG,3          ; is  unit in programme
mode?
 retlw 00                   ; no - ignore
 movf INCTR,same            ; select next mode?
 btfss STATUS,2             ; test if INCTR=0
 goto ERRBP                   ; no - present mode not
programmed
 btfss FLAG,0               ; flag 0 set?
 goto PROG4                 ; no, flag 0 not set -
try flag 1
 bcf FLAG,0                 ; yes - clear flag 0 and
set flag 1
 bsf FLAG,1
 retlw 00
;
PROG4 btfss FLAG,1          ; flag 1 set?
 goto PROG5                 ; no, flag 1 not set -
try flag 2
 bcf FLAG,1                 ; yes - clear flag 1 and
set flag 2
 bsf FLAG,2
 retlw 00
;
PROG5 bcf FLAG,2            ; flag 2 is set - clear
it and set flag 0
 bsf FLAG,0                 ; set flag 0
 retlw 00
;
STORE btfsc FLAG,0          ; is Flag 0 set?
 goto STRCOD                ; yes - store new code
 movlw 0Fh                  ; ie 0000 1111
 andwf LKP,same             ; utilise only low order
bits of LKP
 btfsc FLAG,1               ; no - is flag 1 set?
 goto STRVIW                ; yes - store allowed
viewing time
;
STRTIM                      movlw 4h     ; flag 2 set
- set time
 xorwf INCTR,w
 btfsc STATUS,2             ; INCTR=4?
 goto ST1                   ; yes - store MSD
 movlw 3h                   ; no
 xorwf INCTR,w
 btfsc STATUS,2             ; INCTR=3?
 goto ST2                   ; yes - store NSD
 movlw 2h                   ; no
 xorwf INCTR,w
 btfsc STATUS,2             ; INCTR=2?
 goto ST3                   ; yes - store NSD
 movlw 1h                   ; no
 xorwf INCTR,w
 btfsc STATUS,2             ; INCTR=1?
 goto ST4                   ; yes - store LSD
 movlw 4h                   ; no - then
 movwf INCTR                ; make INCTR=4
;
ST1   clrf MINCTR
 clrf HRCTR
 movlw 3h                   ; check that digit <3
 subwf LKP,w
```

```
 btfsc STATUS,0             ; is LKP>2?
 goto BEEP3                 ; yes - error - beep 3
times
 swapf HRCTR,same           ; no
 movf LKP,w
 movwf HRCTR                ; load HRCTR with last
key pressed
 swapf HRCTR
 goto SM5
;
ST2   movlw 20h
 xorwf HRCTR,w              ; test if first digit
 btfsc STATUS,2             ; is 2
 goto ST5                   ; yes - test next digit
ST6   movf LKP,w            ; no
 iorwf HRCTR,same
 goto SM5
;
ST5   movlw 4h              ; 1st digit is 2 - next
digit <4?
 subwf LKP,w
 btfsc STATUS,0
 goto BEEP3                 ; error next digit >3
 goto ST6                   ; no
;
ST3   movlw 6h              ; check that digit <6
 subwf LKP,w
 btfsc STATUS,0             ; is LKP>6?
 goto BEEP3                 ; yes - error - beep 3
times
 swapf MINCTR,same          ; no
 movf LKP,w
 movwf MINCTR               ;load HRCTR with last key
pressed
 swapf MINCTR
 goto SM5
;
ST4   movf LKP,w
 iorwf MINCTR,same          ; load MINCTR
 goto SM5
;
STRCOD                      movf CUST2,w
 movwf CUST1                ; move CUST2 to CUST1
 movf CUST3,w
 movwf CUST2                ; move CUST3 to CUST2
 movf CUST4,w
 movwf CUST3                ; move CUST4 to CUST3
 movf LKP,w
 movwf CUST4                ; move Last key pressed
into CUST4
 movf INCTR,same
 btfss STATUS,2             ; INCTR=0?
 decf INCTR,same            ; no
 retlw 00                   ; yes
;
STRVIW                      movlw 3h
 xorwf INCTR,w
 btfsc STATUS,2             ; INCTR=3?
 goto SM1                   ; yes - store MSD
 movlw 2h                   ; no
 xorwf INCTR,w
 btfsc STATUS,2             ; INCTR=2?
 goto SM2                    ; yes - store NSD
 movlw 1h                   ; no
 xorwf INCTR,w
 btfsc STATUS,2             ; INCTR=1?
 goto SM3                   ; yes - store LSD
 movlw 3h                   ; no - then
 movwf INCTR                ; make INCTR=3
;
SM1   clrf VTIM1
 clrf VTIM2                 ; clear any set times
already set
 movlw 4h
 subwf LKP,w
 btfsc STATUS,0             ; is LKP>4?
 goto BEEP3                 ; yes - error - beep 3
times
 movf LKP,w                 ; no
 movwf VTIM1                ; load VTIM1 with last
key pressed
 goto SM5
```

```
;
SM2   movlw 3h
 xorwf VTIM1,w
 btfss STATUS,2              ; is VTIM1 =3?
 goto SM4                    ; no
 movlw 6h                    ; yes - check that next
digit <6
 subwf LKP,w
 btfsc STATUS,0              ; is LKP>6?
 goto BEEP3                  ; yes - error - beep 3
times
SM4   swapf VTIM2,same       ; no
 movf LKP,w
 movwf VTIM2                 ; load VTIM2 with last
key pressed
 swapf VTIM2
 goto SM5
;
SM3   movf LKP,w
 iorwf VTIM2,same            ; combine LSD with LKP
SM5   decf INCTR,same
 retlw 00
;
BEEP3 movlw 6h
 movwf CTR1                  ; load 6 into CTR1 to
make 3 beeps
 retlw 00
;
NOKEY bcf FLAG,7             ; clear flag 7 - next key
will be new
 retlw 00
;
;*************************************************
;
;START                          ; initialise lock
memory, timers etc.
;
START movlw 00               ; *INITIALISE SUBROUTINE*
movlw 04h                    ; ie xxxx 0100
 tris PORTA                  ; make PORTA o/p except
A2
 clrf PORTA
 clrf FLAG
 movlw 0F8h
 tris PORTB                  ; make B0-B2 o/p & B3 and
B4-B7 i/p
 movlw 81h                   ; set 1234 as open code
 movwf CUST1                 ; move 1 into F10
 movwf CUST2                 ; move 1 into F11
 movwf CUST3                 ; move 1 into F12
 movwf CUST4                 ; move 1 into F13
;
 movlw 21h
 movwf HRCTR                 ; load 21:00 into clock
 clrf MINCTR
;
 movlw 38h
 option                      ; set prescaler for RTCC
CLK/256
 movlw .120
 movwf MTMR                  ; minuite timer (120 dec)
 movlw .5
 movwf QSTMR                 ; set up quater second
timer (5 dec)
 movlw .25
 movwf HSCTR                 ; set up half second
counter (25 dec)
 clrf VTIM1
 clrf VTIM2
 clrf VCTR1
 clrf VCTR2
;
 clrf INCTR                  ; load 0 into INCTR
 movlw 15h
 movwf CTR1                  ; set up beep counter (10
BEEPS)
 movlw 10h
 movwf FSR                   ; set first customer code
number
;
BEGIN movf RTCC,w
 btfss STATUS,2              ; test if RTCC=0
 goto BEGIN                  ; RTCC not zero
 movlw .255
 movwf RTCC                  ; reload RTCC with 255
dec
;
 call TIME                   ; count time
 call LDSPLY
 call KEYBD
 call MATCH
;
RDIP  btfsc FLAG,4           ;**RDIP ROUTINE check if
                              5sec timer**
 goto BEGIN                  ; is running, yes - take
no action
 btfsc FLAG,5                ; no - check if viewing
is allowed
 goto BEGIN                  ; viewing allowed - flag
5 set.
 btfss PORTA,2               ; not set - is TV on?
 goto BEGIN                  ; yes
 bcf PORTA,3                 ; no - TV is off so
switch off relay
 bcf FLAG,6                  ; yes - it is on
 goto BEGIN
;
;*************************************************
;  START OF PROGRAM
;
 ORG 1FFh
 goto START
;
 END
```

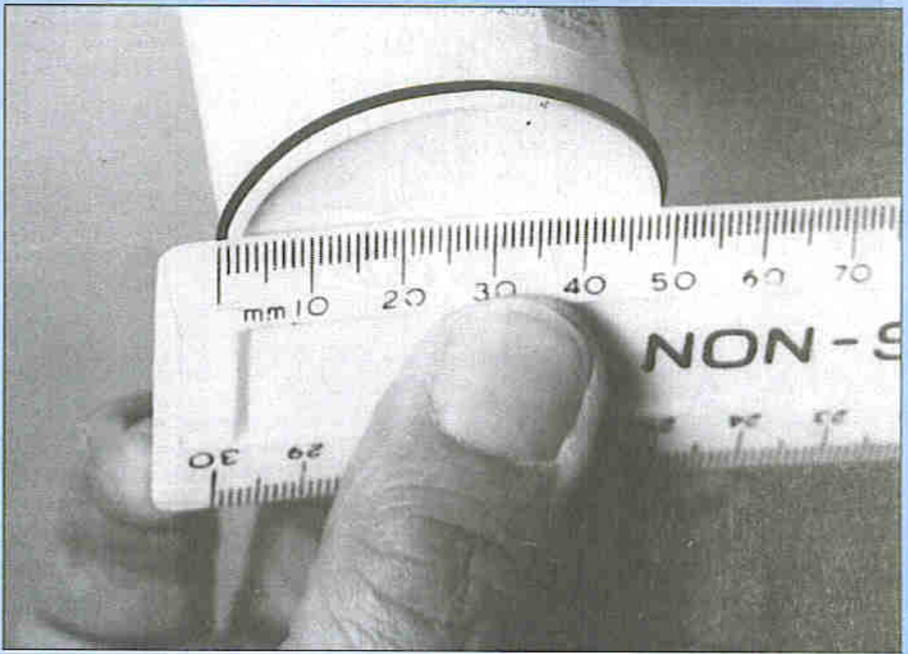
Practically SPEAKING

Cassette Recorders PART 3

Last month, Terry Balbirnie looked at some of the problems which the amateur may encounter when repairing cassette players. This month he continues with a few more

If none of the measures discussed over the last two months effect a restoration to as-new performance, it is quite possible that the record/playback head is worn out.

Note that the head is referred to as the "record/playback" head because the same head is used for both these purposes in most domestic machines. High-quality and professional equipment often have separate ones. Replacement heads are available quite cheaply - for example, those listed by Maplin (catalogue p88-89) and Hart (Tel: 01691 652894). Fortunately, the fixings and electrical characteristics are generally standard. With careful methodical work, it is certainly within the scope of the average amateur to replace a head. It involves dismantling to expose the attaching screws, de-soldering the wires from the tags on the back of the head and removing it.



Replacement follows the reverse process. This must be followed by careful alignment as described last month in Practically Speaking.

Belt up!

Another common problem with cassette machines is worn-out drive belts. These sometimes break but more usually they stretch over a period of time. This results in failure to transfer the drive from the motor at all or to slip and give erratic results. The only cure is replacement - never make do with rubber bands. Belts are obtained from electronics suppliers such as those listed in the Maplin catalogue (p88). They are sold in various sizes. For the Walkman type, the correct diameter is about 26 or 30mm or, for full-size cassette machines, about 19mm to 110mm. The Walkman type usually has a square section of area 1mm2 and the standard type an area of 1.2mm2.

Depending on the model of tape player, it may need some dismantling to remove the old belt and insert the new one. Measuring the diameter of the worn out belt will provide a clue to the correct length to buy. Remember, it will have stretched by a few millimetres. If badly stretched, cut it and overlap the ends so that it provides the correct tension and measure that. One way is to place it round a circular object such as a drinking glass and measure its diameter.

If the pinch roller is worn, the tape will not pass through regularly or fail to move at all. Check the spring which holds the pinch roller in contact with the capstan. If this is stretched unduly it could cause a problem. These spare parts are specific to the machine and replacements will probably need to be ordered from the appropriate dealer. Although easily replaced, they are sometimes expensive. Sometimes, it is uneconomic to do this type of overhaul since the cost of parts may approach the replacement value of a new machine.

In the Walkman type of tape player, it is often reported that only one of the pair of earphones works or that one or both work intermittently. It is always a good idea to substitute a good pair and check whether intermittent operation still exists. Also, try the original earphones on another (good) machine. This will quickly identify whether it is the player which is at fault or the earphones.

Assume for a moment that the fault is in the earphones. Try bending the wire along its length. You may feel a break somewhere inside. If it is near the plug end, it may be worth cutting off the faulty section and fitting a new plug. The problem is often inside the plug itself but usually these are moulded on. Again, the cure is to cut off the plug and fit a replacement. However, it should be remembered that unless the headphones are expensive ones it may be hardly worthwhile doing this type of repair job. If the fault is inside the machine, it is likely to be in the socket itself and, depending on type it may be a simple matter to remove it and solder in a replacement. With luck, it is only a wire which has become detached.

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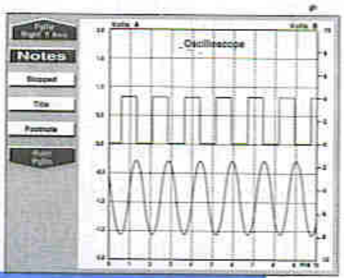

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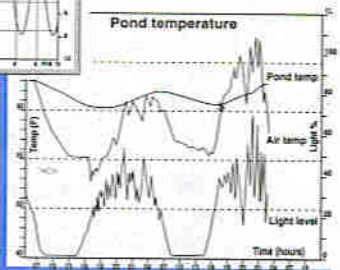

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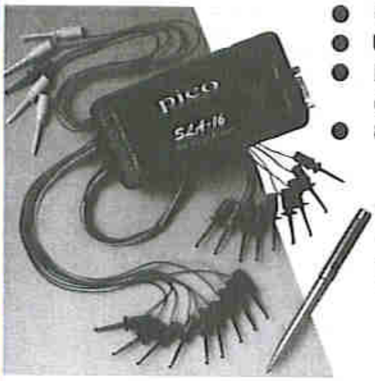

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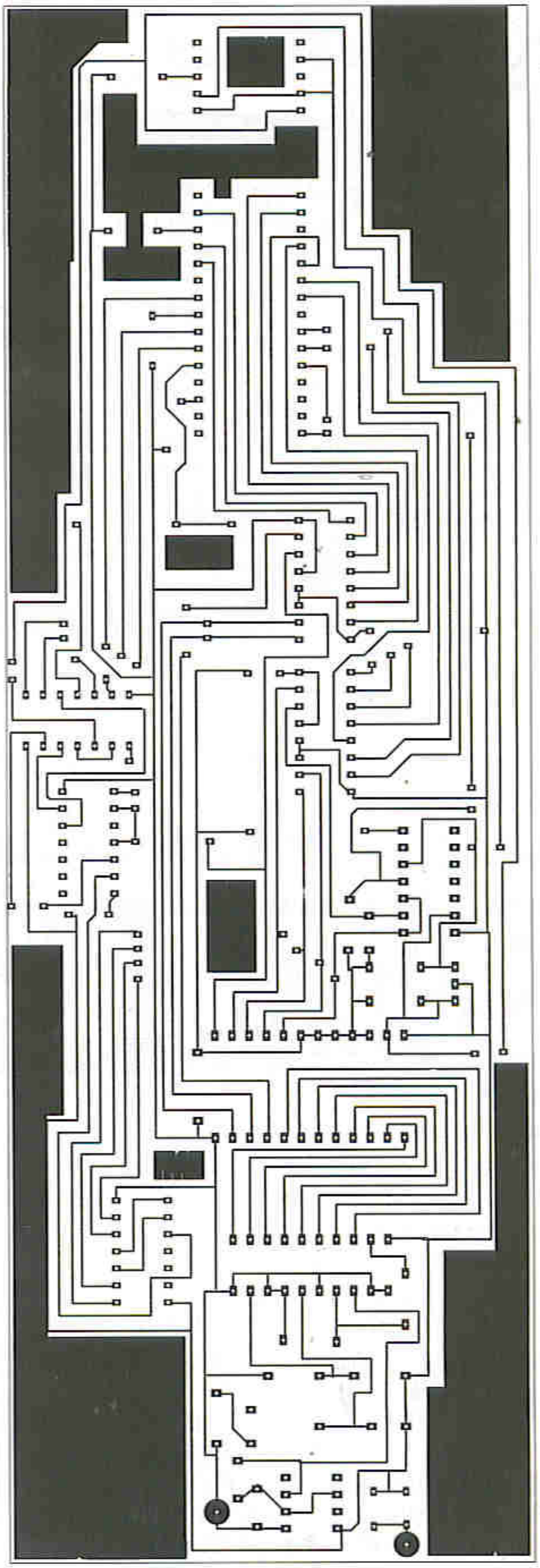

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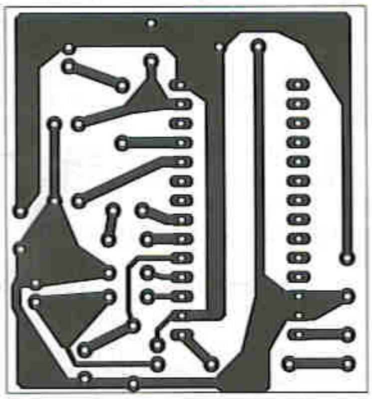

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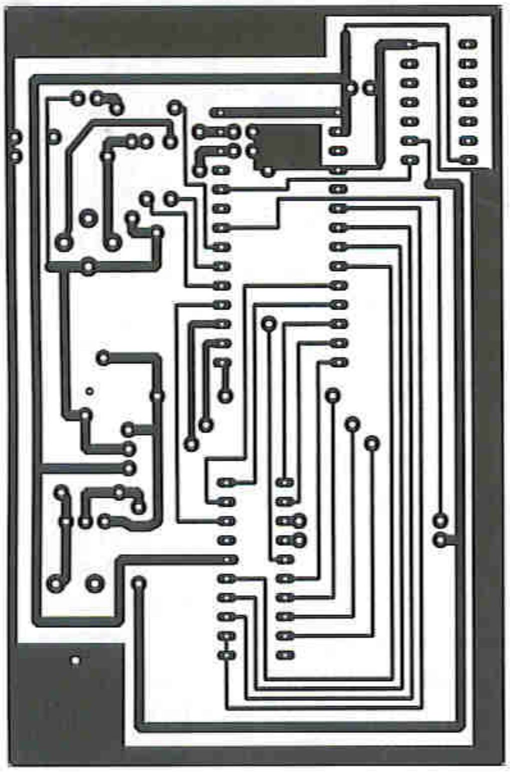

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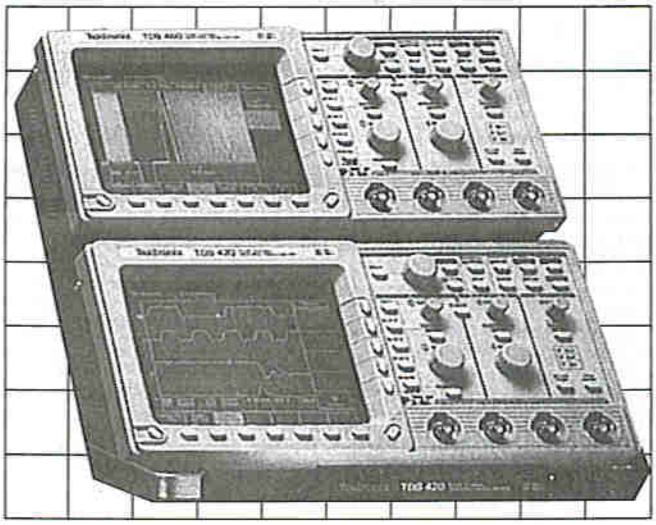

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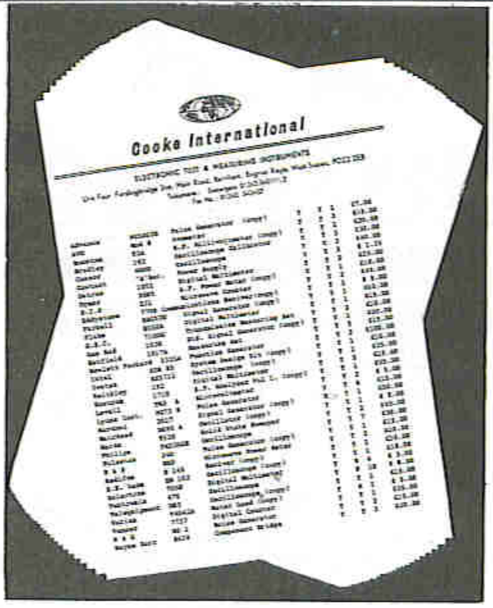

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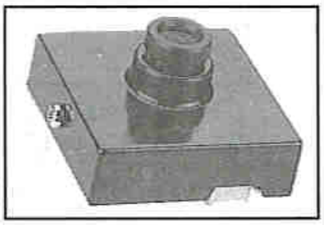

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Around the Corner

Nick Hampshire looks at an innovative incentive for inventors

Regular readers of ETI will be familiar with my repeated calls for much greater recognition for the part that inventors and their innovations play in ensuring the commercial prosperity of this country. Britain is a country with a technology based economy; without technology we could not afford to import grain from Canada, fruit from South Africa or wine for France, let alone take holidays abroad, or buy Japanese consumer goods.

The powerhouse behind technology is innovation, engineering is about creating things that have never been done before - as opposed to science, which is about discovering how the world around us works.

The UK has an unsurpassed record when it comes to innovation. Over half the world's most important commercial inventions of the last 50 years have come from this country.

Unfortunately these and many other concepts were invented here but developed and commercially exploited elsewhere - a fact which has worried governments since the 1940s. Their response has been a chain of initiatives, starting with the National Research and Development Council, now part of the privatised British Technology Group and, most recently, the 150 regionally based Business Link Centres set up by the DTI.

But, although these schemes have been partially successful in 'selling' and exploiting developments coming from government research and universities, they have often been less than successful when it comes to promoting the inventions of individuals and small companies.

These are two areas where once again the UK is very successful. Indeed, according to the Patent Office over 7,000 private individuals go through the enormously time-consuming and expensive process of inventing something and then patenting it every year. Unfortunately most of these inventions never see the commercial light of day.

Similarly many small companies, particularly those in high technology areas, are developing new products and new ideas, but then failing through lack of official and commercial backup, to convert these ideas into the global businesses that so many deserve to become. Without such support this innovation is wasted, only to be picked up and exploited elsewhere.

However, there is a very good chance that things will change for the better if proposals now being placed before the Millenium Commission for funding come to fruition. The proposal comes from a group of UK businessmen and is for the creation of a National Innovation Centre.

The idea has come from the Intellectual Property Development Confederation, a Southampton based 'club' of 350 UK inventors and businessmen which has close ties to Nottingham Trent University. The Innovation Centre will probably be based in Nottingham, with half the £8million capital cost coming from business and the other half from the National Lottery.

The Centre is seen as a way of filling the gap which currently exists between what the inventor needs in the way of financial, technological, and marketing support, and what is currently available for City venture capitalists. After proper screening procedures, the Centre should be able to take several hundred inventions a year to a commercial stage. Operating on strictly commercial lines, the Centre would do this by either licensing the invention, or taking over the intellectual property rights from the inventor.

The idea for the National Innovation Centre has been warmly welcomed by many industrialists, inventors and those involved in technology transfer. It is seen as a way in which to help stop Britain losing out on the billions of pounds of potential sales which are lost every year through failure to properly commercially exploit ideas invented in this country.

It is an idea which deserves support from all, especially those of us involved in technology. The request for funding from the Millenium Commission is for a relatively small sum, the benefits to all of us could be enormous.

Next Month

In the April 1996 issue of Electronics Today International, Robin Abbott looks at how to construct a large matrix display, whilst Terry Balbirnie offers a NiCad charge checker project.

Bart Trepak introduces a PIC microcontroller dimmer project, whilst from Dr Pei An there is an 8051/80535 single board computer project.

The feature articles will include a look at nanotechnology by Dave Clarkeson, and a practical look at repairing and restoring antique electronic equipment from Paul Stenning. Plus reviews of some more PC software and books of interest to readers.

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