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ELECTRONICS DIGEST

DATA ISSUE

DEDICATED DEVICES

SPECIAL PURPOSE ICs FOR:

MUSIC

COMPUTERS

DOMESTIC

AUDIO

TIMING

RADIO

From the Publishers of ELECTRONICS TODAY INTERNATIONAL

FAIRCHILD
A Schlumberger Company

1200 bps Full Duplex Modem

Description

The μAV22 1200 bps full duplex modes I.C. is fabricated in Fairchild's advanced Double-Poly Silicon-Gate CMOS process. The monolithic I.C. performs all the signal processing functions required of a CCITT V.22, alternative B compatible modem. Handshaking protocols, dialing control and mode control functions can be handled by a general purpose, single chip μC. The μAV22, μC and several components to perform the telephone line interface and control provide a high performance, cost effective and ultra-low power solution for V.22-compatible modem designs.

The modem chip performs the modulation, demodulation, filtering and certain control and self-test functions required for a CCITT V.22-compatible modem, as well as additional enhancements. Both 550 Hz and 1800 Hz guard tones and notch filters and DTMF tone generator are on-chip. Switched-capacitor filters provide channel isolation, spectral shaping and fixed compromise equalization. A novel switched-capacitor modulator and a digital coherent demodulator provide 1200 DPSK operation.

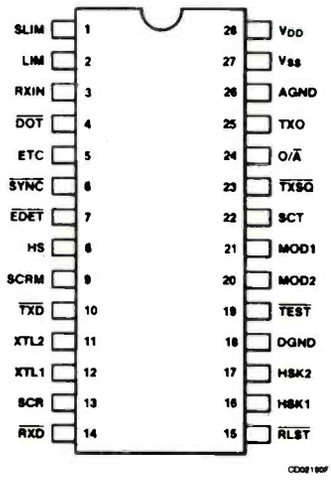
The receive filter and energy detector may be configured for call progress tone detection (dialtone, busy, ringback, voice) providing the front end for a smart dialer.

- **Functions as a CCITT V.22-compatible modem**
- **Interfaces to Single Chip μC Which Handles Handshaking Protocols and Mode Control Functions**
- **DTMF Tone Generation and Call Progress Tone Detection for Smart Dialer Applications**
- **1300 Hz Calling Tone Generator On Chip**
- **Pin and function compatible with the μA212A**
- **On Chip Oscillator Uses 3.6864 MHz Crystal**
- **Few External Components Required**
- **Operates from +5 and −5 Volt Supplies**
- **Low Operating Power: 35 mW Typical**
- **550 Hz and 1200 Hz guard tones and notch filters are on-chip**

Absolute Maximum Ratings

V_{DD} to DGND or AGND	7.0 V
V_{SS} to DGND or AGND	−7.0 V
Voltage at any Input	V_{DD} + 0.3 to V_{SS} −0.3 V
Voltage at any Digital Output	V_{DD} + 0.3 V to DGND −0.3V
Voltage at any Analog Output	V_{DD} + 0.3 V to V_{SS} −0.3 V
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 seconds)	300°C

Connection Diagram
28-Lead Dip
(Top View)



Order Information

Device Code	Package Code	Package Description
μAV22DC	FM	Ceramic DIP
μAV22PC	*	Molded DIP
μAV22QC	*	Molded Surface Mount

*Consult Factory

ELECTRONICS DIGEST

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Welcome to the Summer of 1987. In this issue of Electronics Digest we present full data sheets for more than a dozen selected ICs. They have only one thing in common: each is a complete electronic sub-system on a chip, performing multiple functions that, not too long ago, would have required a circuit board of discrete elements. The selection ranges from relatively simple devices such as smoke and fluid detectors, through single chip AM and FM radios to a universal timer employing a 4-bit computer. Audio circuits include a digitally controlled graphic equaliser IC, a programmable compandor, and a number of sound synthesisers. The datasheets reveal the inner working of the various devices and provide all the information needed by an adventurous constructor to design and build a simple radio, tunes synthesizer, DC motor controller etc.

Contents

Thanks to Mullard/Signetics, National Semiconductor, Fairchild, Texas Instruments, General Instrument, Ferranti, SGS-ATES, and Maplin, for their assistance in compiling this edition of Electronics Digest.

FM Radio Circuit

DESCRIPTION

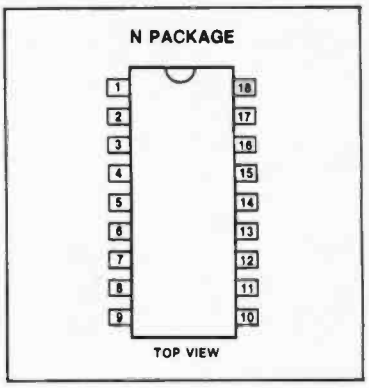
The TDA7000 is a monolithic integrated circuit for mono FM portable radios where a minimum of peripheral components is important (small dimensions and low costs).

The IC has an FLL (Frequency-Locked-Loop) system with an intermediate frequency of 70 kHz. The I.F. selectivity is obtained by active RC filters. The only function which needs alignment is the resonant circuit for the oscillator, thus selecting the reception frequency. Spurious reception is avoided by means of a mute circuit, which also eliminates too-noisy input signals. Special precautions are taken to meet the radiation requirements.

FEATURES

- R.F. input stage
- Mixer
- Local oscillator
- I.F. amplifier/limiter
- Phase demodulator
- Mute detector
- Mute switch

PIN CONFIGURATION



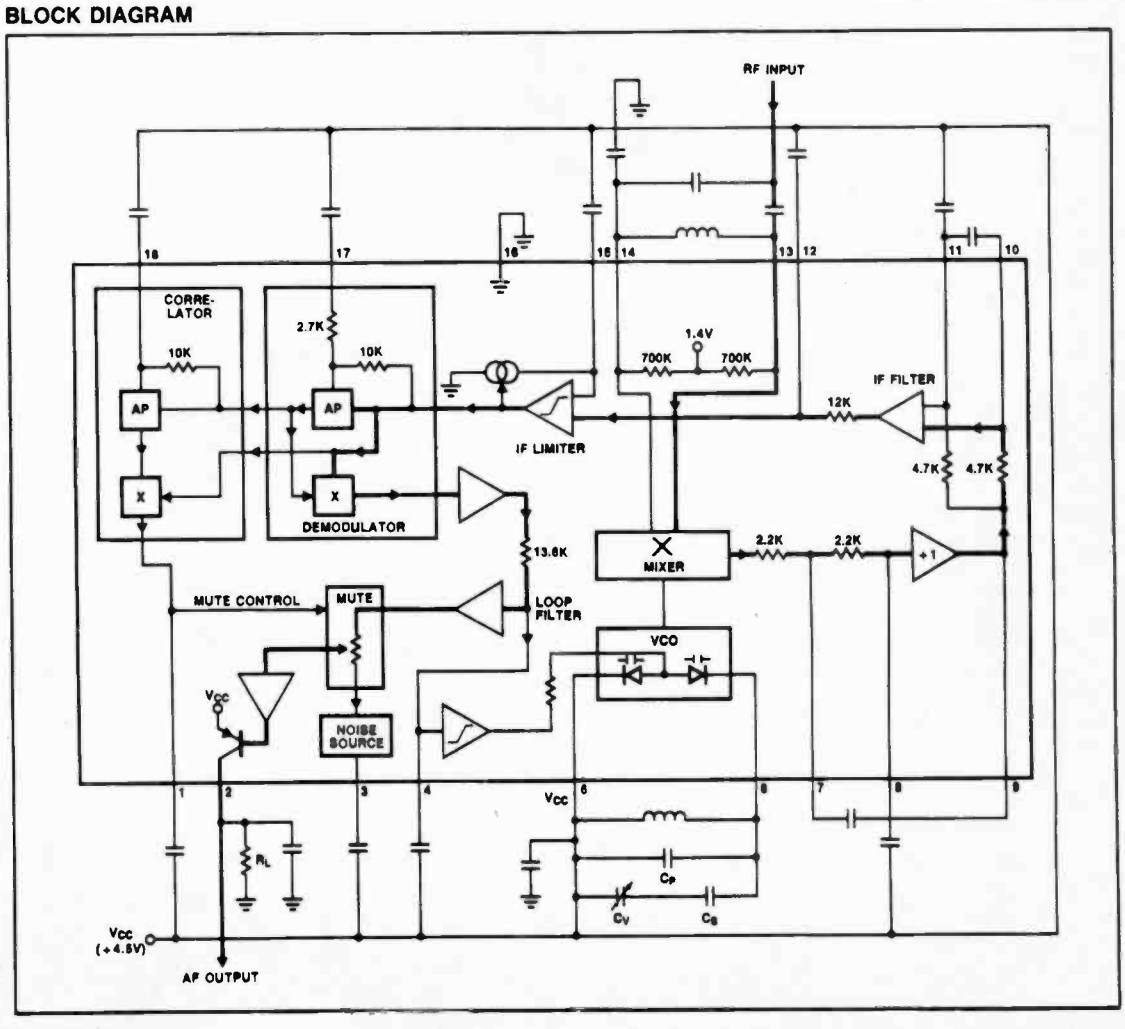
ABSOLUTE MAXIMUM RATINGS

SYMBOL AND PARAMETER		RATING	UNIT
V_{CC}	Supply voltage (pin 5)	12	V
$V_{6\text{-}5}$	Oscillator voltage (pin 6)	V_{CC}−0.5 to V_{CC}+0.5	V
	Total power dissipation	See derating curve Figure 2	
T_{STG}	Storage temperature range	−55 to +150	°C
T_A	Operating ambient temperature range	0 to +60	°C

FUNCTIONAL PIN DESCRIPTION

PIN NO	NAME AND FUNCTION
1	Muting capacitor
2	Audio frequency output
3	Noise source
4	Loop filter capacitor
5	Supply voltage
6	VCO
7	1st integrator capacitor (to pin 9)
8	2nd integrator capacitor
9	1st integrator capacitor (to pin 7)
10	IF filter capacitor (to pin 11)
11	IF filter capacitor
12	IF limiter capacitor
13	RF input
14	Mixer
15	Current source capacitor
16	Ground
17	Demodulator capacitor
18	Correlator capacitor

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5V; T_A = 25°C: measured in Figure 3; unless otherwise specified

SYMBOL AND PARAMETER		TEST CONDITION	TDA7000			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage	(Pin 5)	2.7	4.5	10	V
I_{CC}	Supply current	V_{CC} = 4.5V		8		mA
I_6	Oscillator current	(Pin 6)		280		μA
V_{14-16}	Voltage	(Pin 14)		1.35		V
I_2	Output current	(Pin 2)		60		μA
V_{2-16}	Output voltage	(Pin 2) R_L = 22 kΩ		1.3		V

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5 V; T_A = 25°C; measured in Figure 3 (mute switch open, enabled); f_{rf} = 96 MHz (tuned to max. signal at 5 μV e.m.f.) modulated with Δf = ±22.5 kHz; f_m = 1 kHz; EMF = 0.2 mV (e.m.f. voltage at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified.

SYMBOL AND PARAMETER		TEST CONDITION	TDA7000			UNIT
			Min	Typ	Max	
EMF	Sensitivity (see Figure 2) (e.m.f. voltage)	−3 dB limiting; muting disabled		1.5		μV
		−3 dB muting		6		
		S/N = 26 dB		5.5		
EMF	Signal handling (e.m.f. voltage)	THD < 10%; Δf = ± 75 kHz		200		mV
S/N	Signal-to-noise ratio			60		dB
THD	Total harmonic distortion	Δf = ±22.5 kHz		0.7		%
		Δf = ±75 kHz		2.3		
AMS	AM suppression of output voltage	(ratio of the AM output signal referred to the FM output signal) FM signal: f_m = 1 kHz; Δf = ±75 kHz AM signal: f_m = 1 kHz; m = 80%		50		dB
RR	Ripple rejection	(ΔV_{CC} = 100 mV; f = 1 kHz)		10		dB
$V_{6-5(rms)}$	Oscillator voltage (r.m.s. value)	(Pin 6)		250		mV
Δf_{osc}	Variation of oscillator frequency	Supply voltage (ΔV_{CC} = 1V)		80		kHz/V
S_{+300}	Selectivity			45		dB
S_{-300}				35		
Δf_{rf}	A.F.C. range			±300		kHz
B	Audio bandwidth	ΔV_O = 3 dB measured with pre-emphasis (t = 50 μs)		10		kHz
$V_{O(rms)}$	A.F. output voltage (r.m.s. value)	R_L = 22 kΩ		75		mV
R_L	Load resistance	V_{CC} = 4.5V			22	kΩ
		V_{CC} = 9.0V			47	

NOTES:

1. The muting system can be disabled by feeding a current of about 20 μA into pin 1.
2. The interstation noise level can be decreased by choosing a low-value capacitor at pin 3. Silent tuning can be achieved by omitting this capacitor.

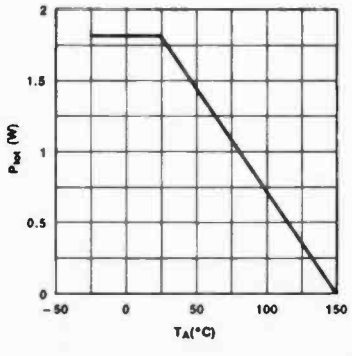


Figure 1. Power Derating Curve.

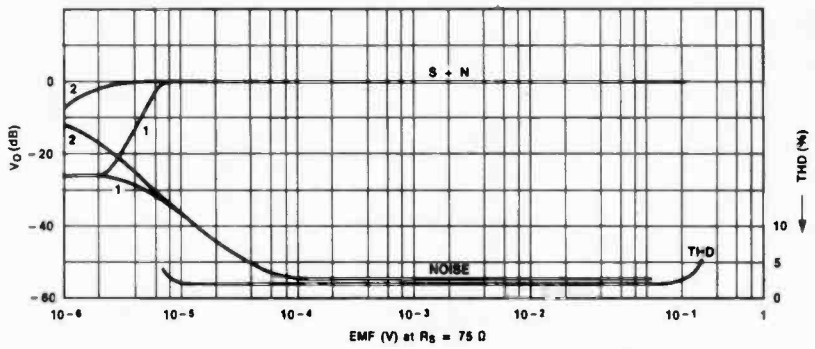


Figure 2. AF output voltage (V_O) and total harmonic distortion (THD) as a function of the e.m.f. input voltage (EMF) with a source impedance (R_S) of 75 Ω: (1) muting system enabled; (2) muting system disabled.

Conditions: 0dB = 75mV; f_{rf} = 98 MHz
for S + N curve: Δf = ± 22.5 kHz f_m = 1 kHz
for THD curve: Δf = ± 75 kHz f_m = 1 kHz

NOTES:
1. The muting system can be disabled by feeding a current of about 20μA into pin 1.
2. The interstation noise level can be decreased by choosing a low-value capacitor at pin 3. Silent tuning can be achieved by omitting this capacitor.

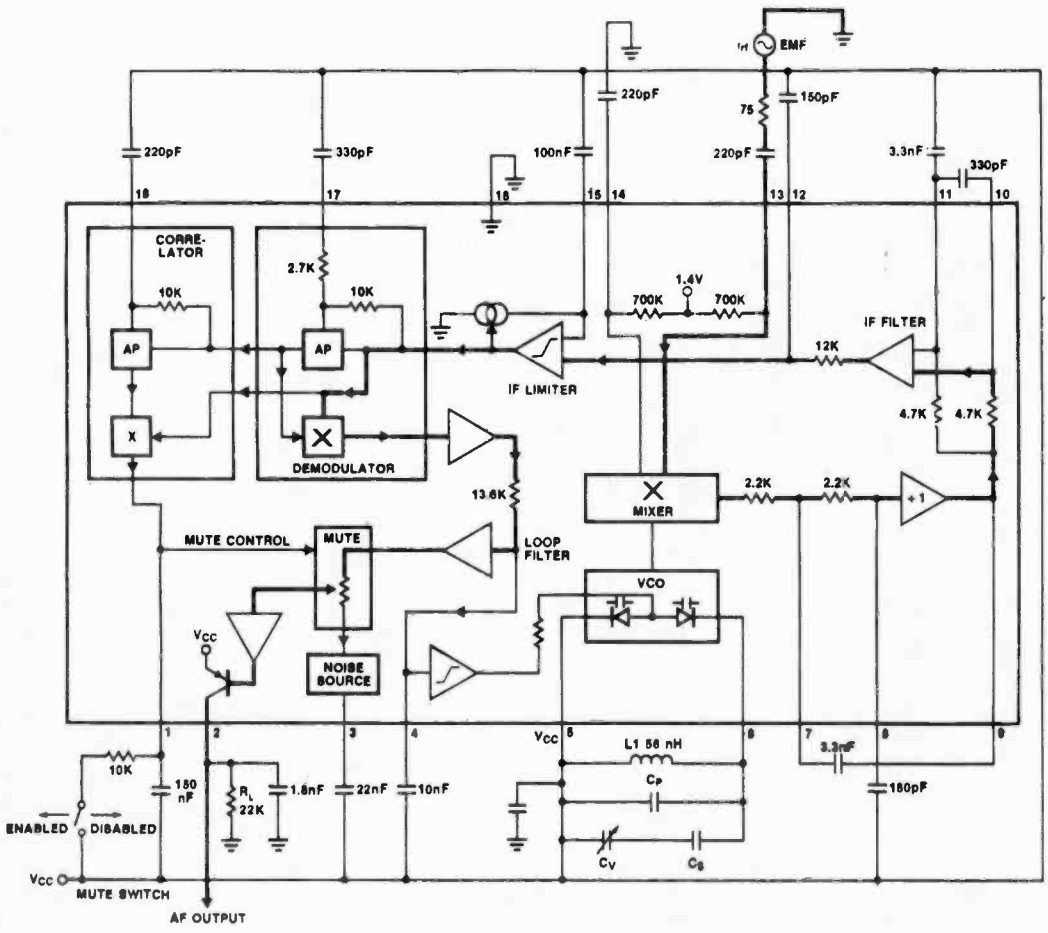


Figure 3. Test Circuit

DC Motor Speed Control Circuit

Description

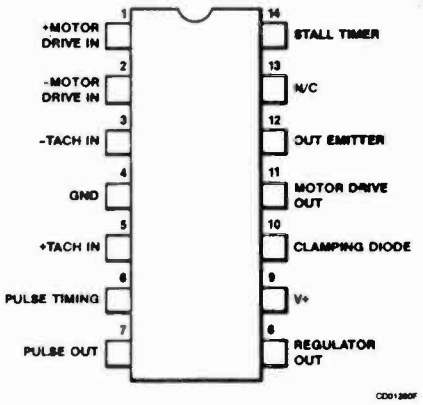
The μA7392 is designed for precision, closed loop, motor speed control systems. It regulates the speed of capstan drive motors in automotive and portable tape players and is useful in a variety of industrial and military control applications, e.g., floppy disc drive systems and data cartridge drive systems. The device is constructed using the Fairchild Planar Epitaxial process.

The μA7392 compares actual motor speed to an externally presettable reference voltage. The motor speed is determined by frequency to voltage conversion of the input signal provided by the tachometer generator. The result of the comparison controls the duty cycle of the pulse width modulated switching motor drive output stage to close the system's negative feedback loop.

Thermal and over voltage shutdown are included for self-protection, and a stall-timer feature allows the motor to be protected from burn out during extended mechanical jams.

- **Precision Performance**
- **High Current Performance**
- **Wide Range Tachometer Input**
- **Thermal Shutdown, Over Voltage And Stall Protection**
- **Internal Regulator**
- **Wide Supply Voltage Range 6.3 V To 16 V**

Connection Diagram
14-Lead DIP
(Top View)



Order Information

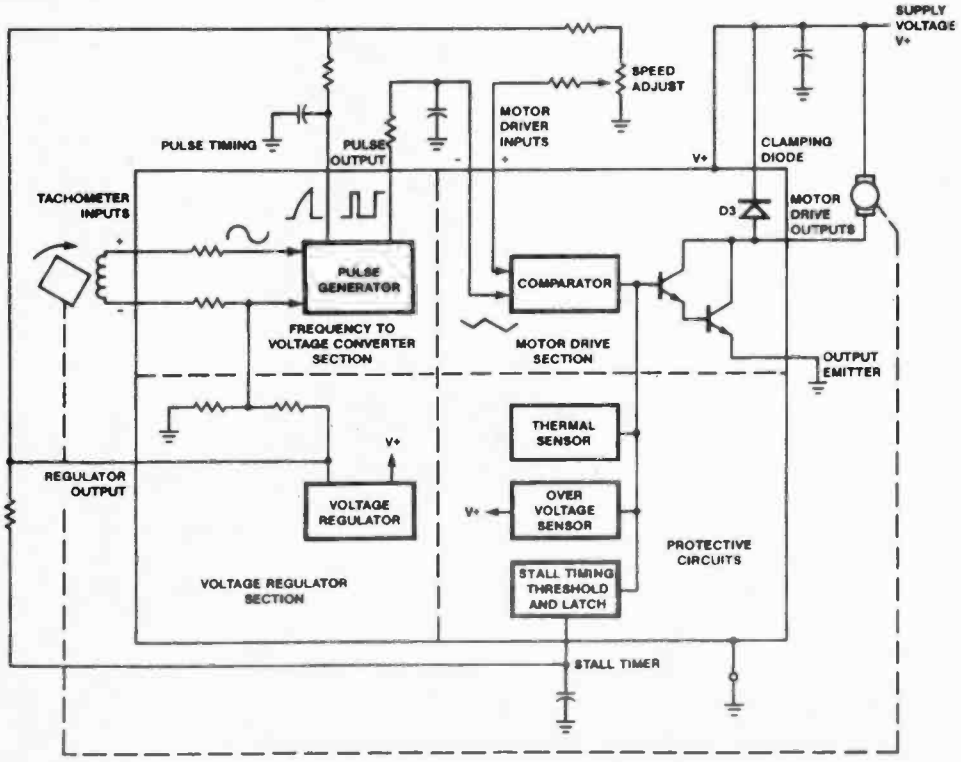
Device Code	Package Code	Package Description
μA7392DV	6A	Ceramic DIP
μA7392PV	9A	Molded DIP

Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1-3]	
14L-Ceramic DIP	1.36 W
14L-Molded DIP	1.04 W
Supply Voltage (V+), V_9, V_{10}, V_{11}	24 V
Regulator Output Current, I_8	15 mA
Voltage Applied to Lead 6 (Tachometer Pulse Timing)	7.0 V
Voltage Applied Between Leads 3 and 5 (Tachometer Inputs)	±6.0 V
Continuous Current through Leads 11 and 12 Motor Drive Output ON	0.3 A
Repetitive Surge Current through Leads 11 and 12 (Motor Drive ON)	1.0 A
Repetitive Surge Current through Leads 10 and 11 (Motor Drive OFF)	0.3 A

Notes
1. $T_{J\ Max}$ = 150°C for the Molded DIP, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 14L-Ceramic DIP at 9.1 mW/°C, the 14L-Molded DIP at 8.3 mW/°C.
3. Internally Limited.

Block Diagram



μA7392
Electrical Characteristics T_A = 25°C, V+ = 14.5 V, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
Voltage Regulator Section (Test Circuit 1)						
I_{CC}	Supply Current	Excluding Current into Lead 11		7.5	10	mA
V_{Reg}	Regulator Output Voltage		4.5	5.0	5.5	V
$LINE_{Reg}$	Regulator Output Line Regulation (ΔV_8)	V+ = 10 V to 16 V		6.0	20	mV
		V+ = 6.3 V to 16 V		12	50	
$LOAD_{Reg}$	Regulator Output Load Regulation (ΔV_8)	I_8 from 10 mA to 0		40		mV
Frequency to Voltage Converter Section (Test Circuit 2)						
V_{IN}	Tachometer (−) Input Bias Voltage			2.4		V
I_{IN}	Tachometer (+) Input Bias Current	$V_5 = V_3$		1.0	10	μA
V_{DIFF}	Tachometer Input Positive Threshold	($V_5 - V_3$)	10	25	50	mV_{p-p}
V_{HY}	Tachometer Input Hysteresis		20	50	100	mV_{p-p}
R	Pulse Timing ON Resistance	V_6 = 1.0 V		300	500	Ω
V_{TH}	Pulse Timing Switch Threshold		45	50	55	$\%V_8$
t_r	Output Pulse Rise Time			0.3		μs
t_f	Output Pulse Fall Time			0.1		μs
$V_{Sat-LOW}$	Pulse Output LOW Saturation (V_7)			0.13	0.25	V
V_{Sat-HI}	Pulse Output HIGH Saturation ($V_8 - V_7$)			0.12	0.2	V
I_{Source}	Pulse Output HIGH Source Current	V_7 = 1.0 V	−340	−260	−180	μA
SVS	Frequency-to-Voltage Conversion Supply Voltage Stability[1]	$V_{FV} = 0.25\ V_8$[2] V_+ = 10 V to 16 V		0.1		%
TS	Frequency-to-Voltage Conversion Temperature Stability[3]	$V_{FV} = 0.25\ V_8$[2] T_A = −40°C to +85°C		0.3		%
Motor Drive Section						
V_{IO}	Input Offset Voltage				20	mV
I_{IB}	Input Bias Current			0.1	10	μA
CMR	Commoh Mode Range		0.8		2.5	V
V_{SAT}	Motor Drive Output Saturation	I_{11} = 300 mA		1.3	2.0	V
I_{LEAK}	Motor Drive Output Leakage	$V_{11} = V_{10}$ = 16 V			5.0	μA
I_D	Flyback Diode Leakage	V_{10} = 16 V, V_{11} = 0 V			30	μA
V_D	Flyback Diode Clamp Voltage	I_{11} = 300 mA Motor Drive Output OFF		1.1	1.3	V
Protective Circuits						
J-T°C	Thermal Shutdown Junction Temperature[4]			160		°C
Over Voltage	Overvoltage Shutdown[4]		18	21	24	V
V_{TH}	Stall Timer Threshold Voltage[5]		2.5	2.9	3.5	V
I_{TH}	Stall Timer Threshold Current[5]			0.3	3.0	μA

Notes

1. Frequency-to-voltage conversion, supply voltage stability is defined as:

$$\frac{V_{FV}(16\ V)}{V_8(16\ V)} - \frac{V_{FV}(10\ V)}{V_8(10\ V)} \div \frac{V_{FV}(14.5\ V)}{V_8(14.5\ V)} \times 100\%$$

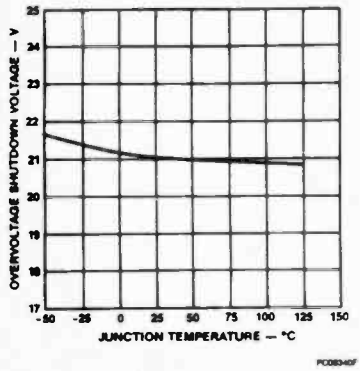
2. V_{FV} is the integrated DC output voltage from the pulse generator (Lead 7)
3. Frequency-to-voltage conversion temperature stability is defined as:

$$\frac{V_{FV}(85°C)}{V_8(85°C)} - \frac{V_{FV}(-40°C)}{V_8(-40°C)} \div \frac{V_{FV}(25°C)}{V_8(25°C)} \times 100\%$$

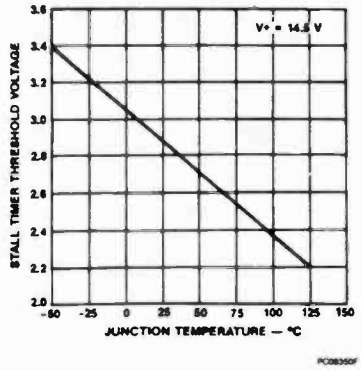
4. Motor Drive circuitry is disabled when these limits are exceeded. If the condition continues for the duration set by the external stall timer components, the circuit is latched off until reset by temporarily opening the power supply input line.
5. If stall timer protection is not required, lead 14 should be grounded.

Typical Performance Curves

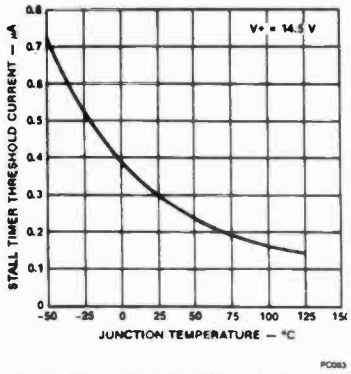
Overvoltage Shutdown Voltage vs Junction Temperature



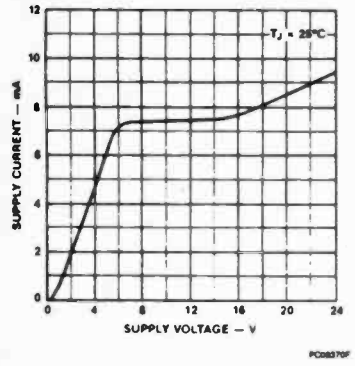
Stall Timer Threshold Voltage vs Junction Temperature



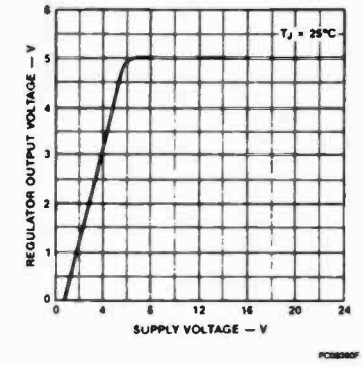
Stall Timer Threshold Current vs Junction Temperature



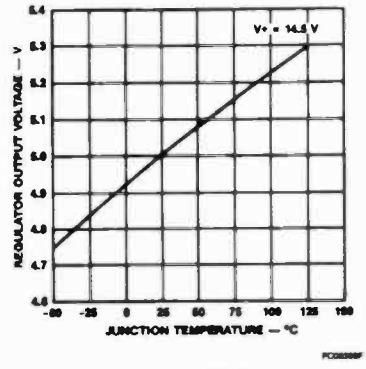
Supply Current vs Supply Voltage



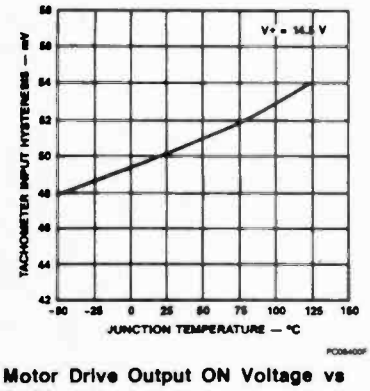
Regulator Output Voltage vs Supply Voltage



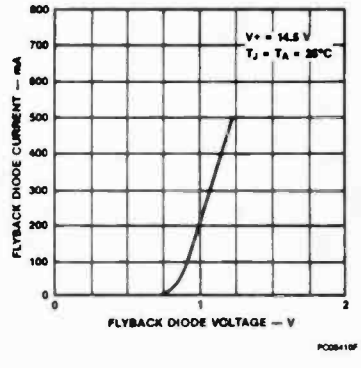
Regulator Output Voltage vs Junction Temperature



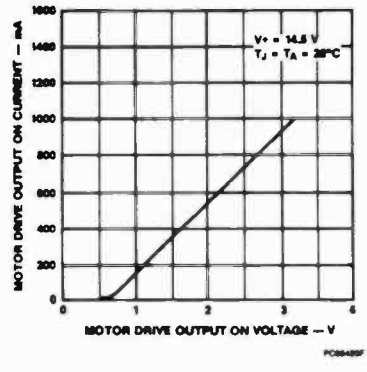
Tachometer Input Hysteresis vs Junction Temperature



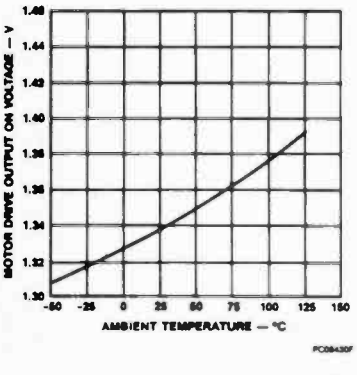
Flyback Diode Current (D3) vs Flyback Diode Voltage



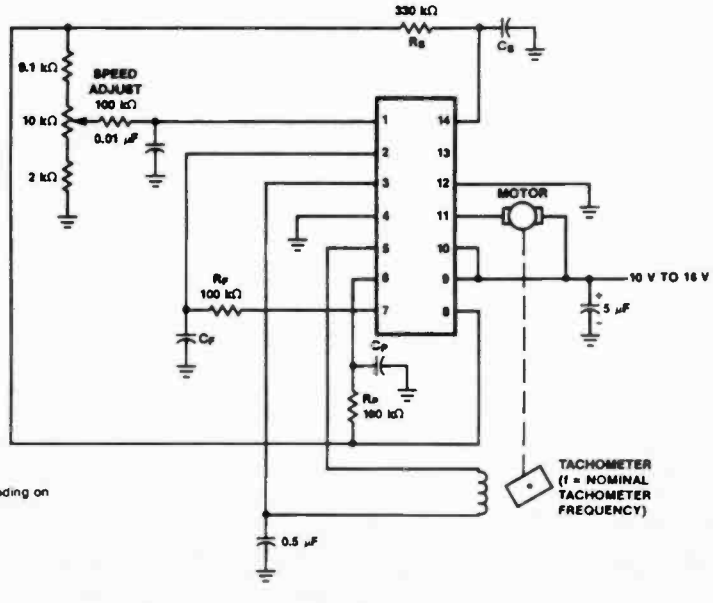
Motor Drive Output ON Current vs Motor Drive Output ON Voltage



Motor Drive Output ON Voltage vs Ambient Temperature



Typical Application Using Magnetic Tachometer



Typical component values:

$C_P = \frac{1}{4\ R_{PF}}$

C_F = 10 Cp to 1000 Cp depending on system requirements

$C_S = \frac{2 \times \text{stall time-out}}{R_S}$

$R_{Motor} \geq 5\ \Omega$

Polyphonic Sound Generator

- 8 μP PROGRAMMABLE SOUND GENERATOR CHANNELS
- 2MHz CLOCK
- INTERNAL TOS WITH POSSIBILITY OF EXTERNAL SYNCHRONIZATION FOR MULTICHIP USE
- 6 COMPLETE OCTAVE KEYBOARDS (72 KEYS)
- FIVE HOMOGENEOUS FOOTAGES μP PROGRAMMABLE BY ADDING A CONSTANT K TO THE KEYBOARD SITUATION
- SEVEN OCTAVE RELATED OUTPUTS ENVELOPED WITHOUT CONSTANT DC LEVEL (4 FOOTAGES)
- SEVEN FOOTAGE RELATED OUTPUTS WITH DIFFERENT CONFIGURATIONS FOR: FOOTAGES WITH ENVELOPE (WITHOUT CONSTANT DC LEVEL) AND FOOTAGES WITHOUT ENVELOPE (WITH CONSTANT DC LEVEL) AND VARIOUS SOUND CHANNEL DIVISIONS (SEE OPTION I, II AND III).
- POSSIBILITY OF EXCLUDING ONE OR MORE SOUND CHANNELS FROM THE NON ENVELOPED FOOTAGE OUTPUTS
- ONE MONOPHONIC OUTPUT NON ENVELOPED RELATED TO SOUND CHANNEL 1 WITH THE POSSIBILITY OF CHOOSING THE FOOTAGE (TWO ADDITIONAL MONOPHONIC OUTPUTS ON OPTION II).
- 50% DUTY CYCLE ON ALL OUTPUTS
- DIGITAL DRAWBAR CONTROL (32 LEVELS)
- ATTACK-DECAY-SUSTAIN-RELEASE (ADSR) ENVELOPE DEFINITION WITH DIGITAL CONTROL ON A.D.R. AND ANALOG CONTROL ON S
- ADDITIONAL ANALOG CONTROL ON RELEASE
- ANALOG PERCUSSION INPUT TO ENVELOPE ONE FOOTAGE (M2) ON THE OCTAVE RELATED OUTPUTS
- SPECIAL EXTERNAL ENVELOPE POSSIBILITY USING HOLD AND/OR RELEASE ∞. HOLD AND RELASE ∞ ARE DEDICATED TO DECAY AND PEDAL EFFECT.
- N-CHANNEL TECHNOLOGY - 12V SINGLE SUPPLY.

The M112 is a polyphonic sound generator that combines eight generators with envelope shapers and drawbar circuitry in a single package.
This versatile circuit simplifies the design of a wide range of polyphonic instruments and, interfacing directly with a microcomputer chip, gives designers an unprecedented degree of flexibility.
The M112 is realized on a single monolithic silicon chip using low threshold N-channel silicon gate MOS tecnology. It is available in a 40 lead plastic package.

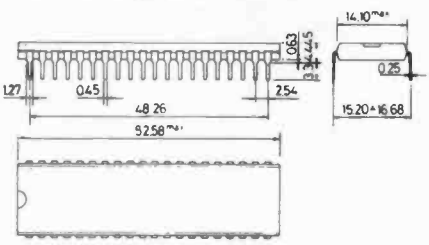
ABSOLUTE MAXIMUM RATINGS

V_{DD} *	Supply voltage	-0.3 to 20	V
V_I	Input voltage	-0.3 to V_{DD}	
$V_{O(off)}$	Off state output voltage	-0.3 to 20	V
P_{tot}	Total package power dissipation	500	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

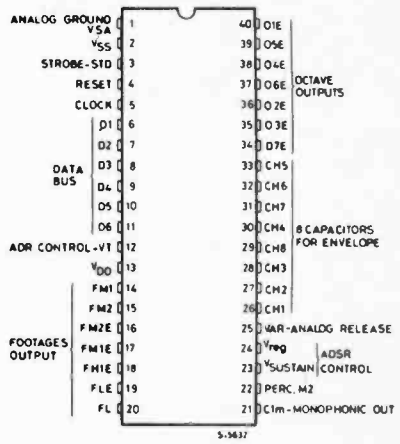
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* All voltages are with respect to V_{SS}.

MECHANICAL DATA (Dimension in mm)



PIN CONNECTIONS

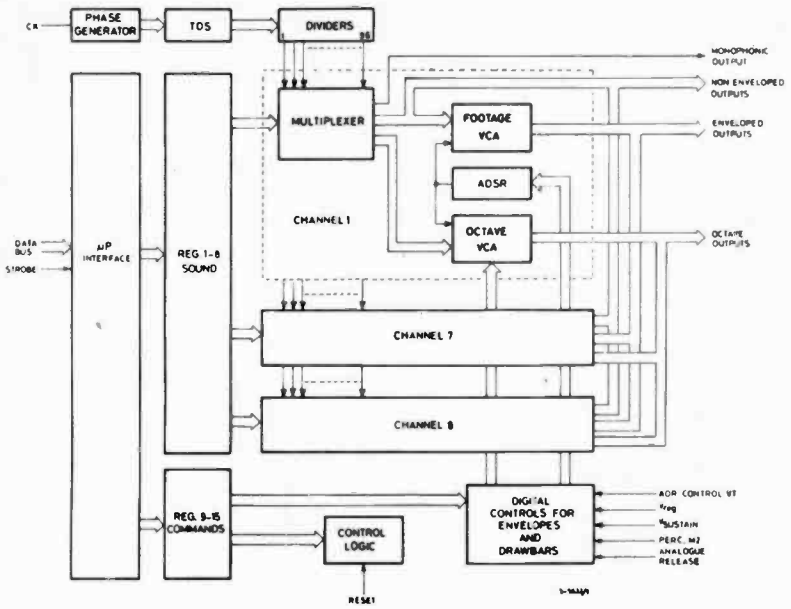


RECOMMENDED OPERATING CONDITIONS

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
V_{DD}	Highest Supply Voltage		11.4	12	12.6	V

BLOCK DIAGRAM

Fig. 1



STATIC ELECTRICAL CHARACTERISTICS

(V_{DD} = 12V ± 5%, V_{SS} = 0V, T_{amb} = 0 to 50°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
INPUT SIGNALS						
V_{IH}	Input High Voltage	Pins 3, 6 to 11	2.4		V_{DD}	V
		All other inputs	6		V_{DD}	V
V_{IL}	Input Low Voltage	Pins 3, 6 to 11	-0.3		0.8	V
		All other inputs	-0.3		1	V
VSA	Analog Ground	R < 10Ω C = 100µF	0	0	1	V
VT	ADR Control Time	R = 1K C = 1µF	0		V_{DD}	V
VAR	Analog Release	R = 10K C = 0.1µ	0		V_{DD}	V
V_{reg}	Control OFF Asymptote	R < 10Ω C = 100µ	0	0	1	V
V_{SUST}	Control Level Sustain	R = 1K C = 100µ	0		V_{DD}	V
Perc. M2	Control Level Percussion	R = 10K	0		V_{DD}	V
I_{LI}	Input Leakage Current	$V_I = V_{DD}$			1	µA
OUTPUT SIGNALS (One key pressed)						
I_{OL}	Output Low current	$V_{OL} = V_{DD/2-1V}$ (note 1)	10	30	50	µA
I_{OH}	Output High Current	$V_{OH} = V_{DD/2+1V}$ (note 1)	10	30	50	µA
		V_{OH} = 10V (note 2)	100	300	500	µA
		V_{OH} = 10V	10	30	50	µA
$I_{O(off)}$	Off state output current	$V_O = V_{DD}$ (all output pins)			1	uA
		$V_O = V_{SS}$ (pins 14-15-20 in 3rd state)			-1	µA
POWER DISSIPATION						
I_{DD}	Supply current	T_{amb} = 25°C			50	mA

Notes: 1. Refers only to FL, FM1, FM2 (pins 20, 15, 14).
2. Refers only to octave outputs with drawbar max.

DYNAMIC ELECTRICAL CHARACTERISTICS

Parameter		Test conditions	Min.	Typ.	Max.	Unit
CLOCK						
f_I	Input Clock Frequency		250	2000.24	2.300	kHz
t_r, t_f	Rise and Fall Times 10% to 90%				30	ns
t_{on}, t_{off}	ON and OFF Times		150			ns
RESET						
t_w	Pulse Width	Clock = 2 MHz	10			µs
t_f	Fall Time				30	ns
OUTPUT SIGNALS						
t_{on}, t_{off}	Outptu duty cycle			50		%

GENERAL DESCRIPTION

The M112 contains a microprocessor interface, eight programmable sound generator channels, a top octave synthesiser, a divider chain and control circuitry, (see fig. 1). Each generator consists of logic to select the desired notes and harmonics from 96 frequencies obtained by division, an ADSR envelope generator and two voltage-controlled amplifiers. Programmable attenuators are included for drawbar control of the harmonic content of the sound.

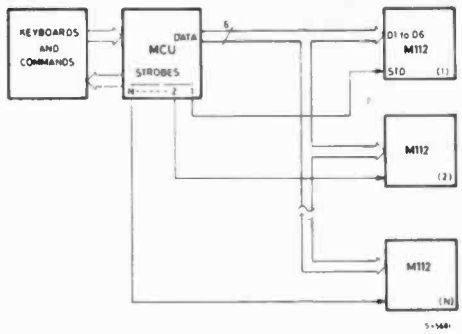
To simplify system design the signals generated in each channel are directed to octave separated outputs and footage outputs. Two voltage-controlled amplifiers are provided for each channel to keep the octave and footage outputs separate.

The attack time, decay time, release time and sustain level are set for all eight channels by common controls. Tone selection, the attack, decay, release parameters, drawbars and special effects are all software controlled.

In a typical configuration (fig. 2), one or more M112s are connected to a microprocessor which scans the keyboard and front panel controls in a matrix arrangement. When the microprocessor detects a key depression it chooses one of the sound generators and allocates it to that note. If another key is pressed the microprocessor allocates another sound generator and so on. This process can be repeated until there are no more free channels, i.e. when 8N keys are pressed simultaneously where N is the number of M112s used.

When one of the keys is released the microprocessor resets a control bit in the appropriate generator channel which will then be re-allocated to another key when needed.

Fig. 2



OUTPUTS

The M112 has 15 music output pins. Seven of these are octave outputs, seven are footage outputs and the last is a monophonic output from channel one. This standard configuration can be changed under program control.

The octave outputs, which are enveloped, are so called because there is one output for each octave, i.e. output signals from all eight channels that fall within the same octave are routed to the same output. These outputs are provided to simplify the generation of sinewaves from the squarewaves generated by the M112s digital circuitry. Since each of these outputs handles a limited range of frequencies – exactly one octave – a simple low pass or bandpass filter will do the job. The blend of harmonics sent to the octave outputs is controlled by the drawbar attenuators.

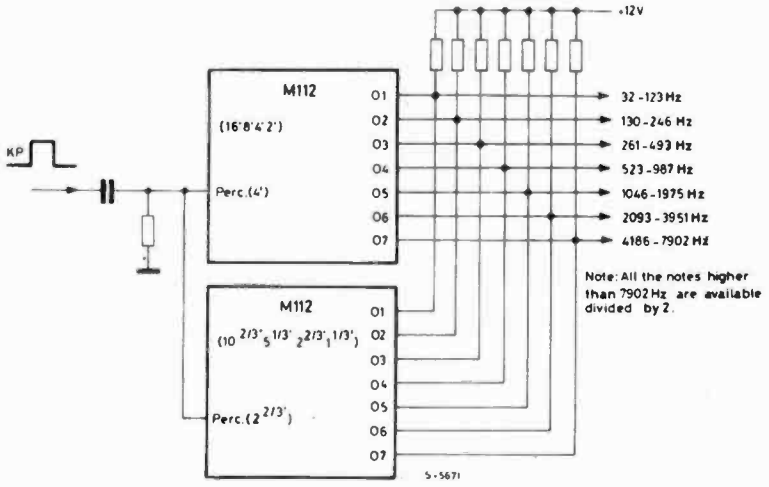
The footage outputs are related to the five footages generated by the M112. These are referred to as L, M1, M2, H1 and H2 (L = Low, M = mid, H = high) and can be programmed to give the three different ranges given in table 1, adding a constant K (number of half tones) to the keyboard information.

All five footages can be obtained from these outputs but only four are mixed by the drawbar circuitry and routed to the octave outputs.

TABLE 1 - THE THREE FOOTAGE RANGES OF THE M112

	Enveloped footage outputs (option 2)				
	Octave outputs				
	Non Enveloped Footage Outputs				
Footage / K	L	M1	M2	H1	H2
0	16'	8'	4'	2'	1'
7	10 2/3'	5 1/3'	2 2/3'	1 1/3'	2/3'
4	12 4/5'	6 2/5'	3 1/5'	1 3/5'	4/5'

Fig. 3 - Example of octave related output "EVEN" and "ODD" with Percussion input.



In no case will the maximum frequency be higher than 7902 Hz (with a 2 MHz clock).
The output configuration for the octave and footage outputs can be changed under program control as mentioned above. There are three options, including the standard configuration, and these are:

- Option 1, the normal configuration gives four enveloped footage outputs, LE, M1E, M2E, H1E, and three non-enveloped outputs, L, M1 and M2. All eight channels are present on each output.
- Option 2 is a special configuration for sawtooth generation (sawtooth waveforms are frequently used in sound synthesis). In this case channels two and three appear only on the outputs FM1 and FM2 (footages M1 and M2) and are excluded from the rest. All five footages are available as enveloped outputs.
- Option 3 is intended for sophisticated automatic accompaniment circuits. All the channels appear on three non-enveloped outputs (FL, FM1, FM2) for chord generation and can be disconnected or command. Channels 4, 5, 6 and 7 appear on four enveloped outputs for arpeggi. The octave outputs are used for the bass and include only channel 8.

TABLE 2 - OUTPUT CONFIGURATIONS

Pin	Option I	Option II	Option III	Option IV
15	FM2	FM2 (Channel 3)	FM2 } All channels	FM2 (Ch. 3)
14	FM1	FM1 (Channel 2)	FM1 } (see note 3)	FM1 (Ch. 2)
20	FL	FH2E }	FL }	FH2E (Ch. 4, 5, 6, 7, 8)
18	FH1E	FH1E	FH1E }	FH1E }
16	FM2E	FM2E	FM2E } only channels	FM2E } only channels
17	FM1E	FM1E	FM1E } 4-5-6-7	FM1E } 4-5-6-7
19	FLE } For the	FLE	FLE }	FLE }
40	O1E } 8 channels	O1E } Only channels	O1E }	O1E }
36	O2E	O2E } 1-4-5-6-7-8	O2E }	O2E }
35	O3E	O3E	O3E }	O3E }
38	O4E	O4E	O4E } only channel 8	O4E } only channel 8
39	O5E	O5E	O5E }	O5E }
37	O6E	O6E	O6E }	O6E }
34	O7E	O7E }	O7E }	O7E }
21	Monophonic out (channel 1)	Mono (channel 1)	Mono (channel 1)	Mono (channel 1)
	Standard use	Special for sawtooth generation etc.	Special for high class accompaniment	Only for information (no musical meaning)

- FL, FM1, FM2 are footage outputs not enveloped (with constant DC level)
- FLE, FM1E, FM2E, FH1E, FH2E are enveloped (without constant DC level).

Notes: 1) H2 is available only in option 2 on FH2 enveloped outputs. It is not available on octave related outputs.

2) In the option 2 the Sound channels 2 and 3 are available only on pins 14 and 15 and consequently are excluded from the other outputs.

3) Each channel can be disconnected with commands NC1 to NC8 (register 10).

DRAWBARS AND EFFECTS

One of the significant features of the M112 is the implementation of drawbar control circuitry. This consists of four programmable attenuators, one for each of the footages routed to the octave outputs, which are used to blend harmonics to produce the desired sound.

Other features of the M112 include hold, pedal and percussion effects, all of which are enabled/disabled under software control. Hold, when active, interrupts the decay of the ADSR envelope and Pedal interrupts the release curve. Hold and pedal permit external control of the envelope. This feature can be used, for example, to synthesize very realistic piano and harpisichord sounds.

A piano effect can be produced by suitably programming the envelope shapers but by using the hold and pedal controls and a few external components much greater realism can be obtained. Fig. 4 shows a simplified schematic of one of the envelope shapers together with the type of envelope generated. The envelope parameters are controlled by RA, RD, RR and V_{SUS} (RA, RD and RR are programmed resistors controlling attack, decay and release). Disabling the natural decay and release and adding a handful of components a close approximation to the ideal waveform can be produced (fig. 5). R1 is a very large resistance (typically 3 MΩ) to give the long (several seconds) time constant for the second decay.

Fig. 4 - With an external capacitor the M112's envelope shapers produce the standard ADSR envelope.

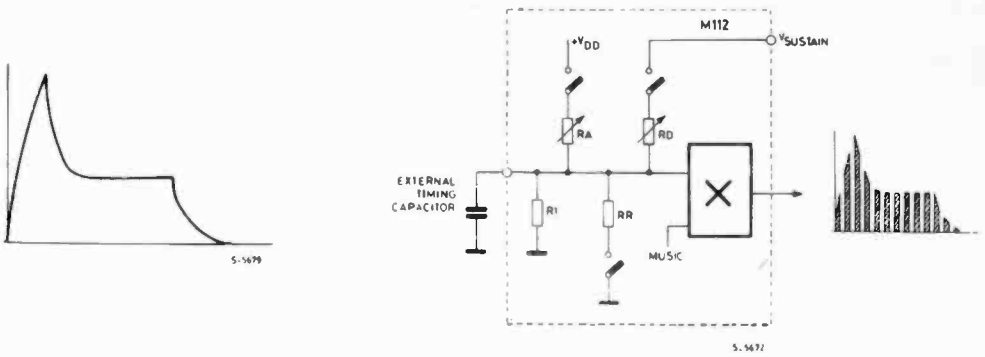
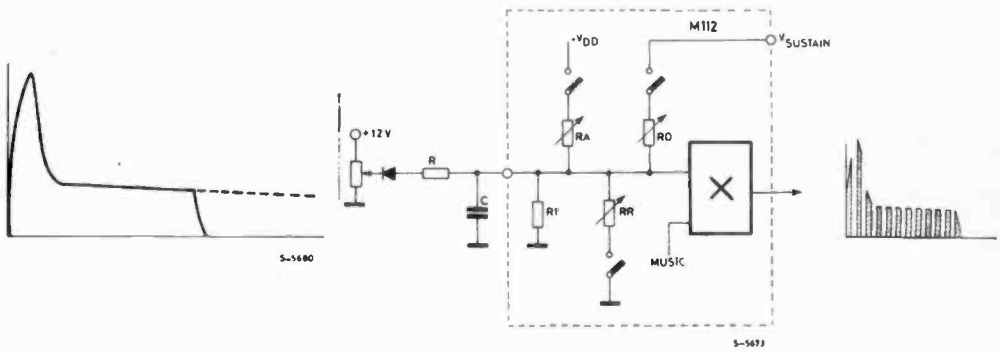


Fig. 5 - Disabling the normal decay and release and adding a few external components a realistic piano envelope can be produced.



INPUTS

Eight pins on the M112 are used to define the elementary time interval of the ADSR envelope shapers (Pins 26 to 33). Capacitors, nominally 1μF, are connected to these pins. Eight separate capacitors are necessary because the envelope shapers are independently triggered. Analog inputs are also provided to adjust the asymptotic release level (V_{reg} pin 24) and the charge/discharge current for attack, decay and release (VT pin 12) in order to compensate the differences of ADR time constant between several M112s used in the same instrument.
The sustain level is fixed by the voltage at pin 23.
The release time constant, digitally controlled by software, can also be fine adjusted by a trimmer connected at pin 25.

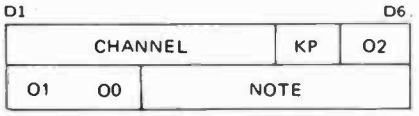
PROGRAMMING

The M112 is programmed using five basic commands:

- CHANNEL PROGRAM
- ADSR PROGRAM
- NON-ENVELOPED OUTPUT MASK
- LOAD CONTROL REGISTER
- DRAWBAR PROGRAM

These commands all consist of 12 bits transferred to the M112 (or one of the M112s) in two six-bit bytes through six data lines. Data is latched into the M112 synchronously by a strobe signal. The M112 can be connected directly to an M387X series microcomputer.
Each command contains the address of the Register in which data is to be memorized (there are 16 registers) and the data.

Channel program commands consist of the channel code (4 bits), octave code (3 bits), note code (4 bits) and a control bit, KP (key pressed). KP must be set if the key has just been pressed and reset if the note has just been released.

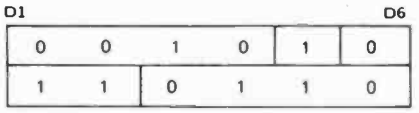


CHANNEL PROGRAM

Resetting KP does not necessarily silence the channel because the sound continues after the key has been released if the release time is non-zero. To stop a channel completely the unused note and octave codes are used.

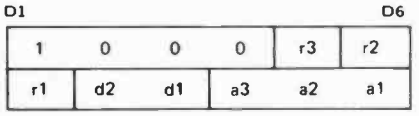
If an unused note code is programmed the channel is turned off with the output transistor in the ON state and if an unused octave code is used the channel is turned off with the output transistor in the OFF state. Six octave codes and twelve note codes are recognized, giving a keyboard span of 72 keys.

For example, to tell an M112 that channel three is to play F# in the third octave the command is:



CHANNEL 3 CODE IS 0010
OCTAVE 3 CODE IS 011
F # NOTE CODE IS 0110
KP IS SET

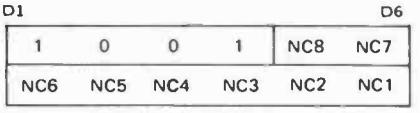
The ADSR Program command sets the attack, decay and release times for all the envelope shapers. This command takes the form:



ADSR PROGRAM

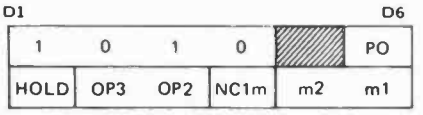
The code 1000 selects the ADSR control register, a3/a2/a1 is the attack time, d2/d1 is the decay time and r3/r2/r1 is the relase time. These times are all multiples of the time interval set by external capacitors. With the suggested 1μF values this time interval is 15ms. The release code 000 is used to enable the pedal effect.

The Non-Enveloped Output Mask command is used to select which channels are to be routed to the non-enveloped footage outputs. Any or all of the eight channels can be excluded by setting the appropriate bit.



OUTPUT MASK

The Load Control Register command selects the footage and output options and enables/disables the hold and percussion facilities.



LOAD CONTROL REGISTER

"NC1m" is a control bit that excludes channel one from all outputs except the three non-enveloped footages outputs. PO is the percussion disable bit, m2/m1 is the footage option select code for the monophonic output and OP2/OP1 the output configuration select code.

The drawbar-controlled attenuators are set independently for each footage using the Drawbar Program Command which has the form:

DRAWBAR PROGRAM

Footage is selected by addressing registers R12 to R15.
Attenuation is controlled in 32 linear steps which can be conveniently reduced to the conventional 16 or 8-step logarithmic scale using a lookup table.

APPLICATIONS

The M112 is intended for a wide range of applications ranging from simple single-keyboard organs to 2-3 manual instruments with sophisticated synthesis and accompaniment facilities. It can also be used in electronic pianos, harpsichords, string synthesizers etc.

DESCRIPTION

Pin 1 - VSA Analog ground

Ground connection of all outputs. It is typically connected to V_{SS}. By adjusting its value with respect to V_{SS} (plus/minus) it is possible to modify the output current and compensate the differences in current between several M112s used in the same applications.

Pins 2 and 13 - V_{SS}, V_{DD}

Power supply connections. V_{DD} is nominally 12V; V_{SS} is to be connected to GND.

Pin 4 - Reset input

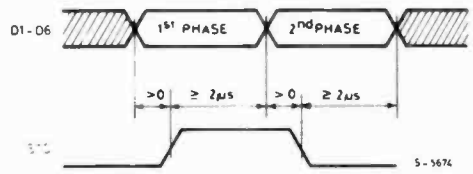
It is used to synchronize various M112s in multichip use. The reset is activated when the input is at H Level. In this condition the chip is blocked.

Pin 5 - Clock input

It has to be connected to an external oscillator of 2 MHz.

Pin 6 to 11 - D1, D6 Data bus input
Pin 3 - STD Data Strobe input

These pins are used to transfer the 12 bits of data from the microprocessor to the registers of various M112s using a two phase procedure.
The first six bits of data are latched on the positive edge of STD, while the other six bits are latched on the negative edge of STD.



Each 2 x 6 bit of information contains the address of the register (4 bit/16 registers) and the data up to 8 bits to be memorized in the selected register.

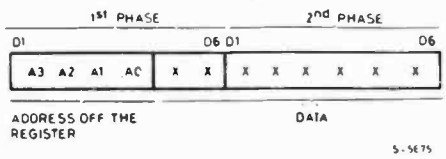


TABLE 3 - REGISTER SELECTION

A0	A1	A2	A3	Register n°	Register function
0	0	0	0	1	Note-octave etc. For Sound channel
1	0	0	0	2	
0	1	0	0	3	
1	1	0	0	4	
0	0	1	0	5	
1	0	1	0	6	
0	1	1	0	7	
1	1	1	0	8	
0	0	0	1	9	Control Commands
1	0	0	1	10	
0	1	0	1	11	
1	1	0	1	12	
0	0	1	1	13	
1	0	1	1	14	
0	1	1	1	15	
1	1	1	1	16	Used for test*

* This address sets the Ic in a test condition that can only be modified by a Reset command on pin 4.

Registers 1 to 8

There registers are related to the sound channels

	Bus	Data	
PHASE 1	D1	A3	must be "0"
	D2	A2	Sound Channel Selection
	D3	A1	
	D4	A0	
	D5	KP	Key information
	D6	O2	
PHASE 2	D1	O1	
	D2	O0	
	D3	N3	
	D4	N2	
	D5	N1	
	D6	N0	

A0-A2: Sound channel selection with reference to table 3, register 1 is related to channel 1, register 2 to channel 2 and so on up to channel 8.

KP : 1 = pressed key 0 = relased key
O0-O1-O2: Octave code of the note (Table 4).

TABLE 4

O0	O1	O2	Code	Octave	
0	0	0	0		Note OFF
1	0	0	1	1	
0	1	0	2	2	
1	1	0	3	3	
0	0	1	4	4	
1	0	1	5	5	
0	1	1	6	6	
1	1	1	7		Note OFF

Output transistor "OFF"

N0-N1-N2-N3 = Note Code (Table 5)

TABLE 5

N0	N1	N2	N3	Code	Note	
0	0	0	0	0	DO	
1	0	0	0	1	DO#	
0	1	0	0	2	RE	
1	1	0	0	3	RE#	
0	0	1	0	4	MI	
1	0	1	0	5	FA	
0	1	1	0	6	FA#	
1	1	1	0	7	SOL	
0	0	0	1	8	SOL#	
1	0	0	1	9	LA	
0	1	0	1	10	LA#	
1	1	0	1	11	SI	
0	0	1	1	12	Note "OFF"	
1	0	1	1	13	Note "OFF"	
0	1	1	1	14	Note "OFF"	
1	1	1	1	15	Note "OFF"	

Output transistor "ON"

Regişter 9 to 15

These registers are related to the various control commands

TABLE 6

	Register / Data Bus	R9	R10	R11	R12	R13	R14	R15	R16
PHASE 1	D1	1	1	1	1	1	1	1	1
	D2	0	0	0	0	1	1	1	1
	D3	0	0	1	1	0	0	1	1
	D4	0	1	0	1	0	1	0	1
	D5	r3	NC8	X	X	X	X	X	X
	D6	r2	NC7	PO	X	X	X	X	X
PHASE 2	D1	r1	NC6	HOLD	X	X	X	X	X
	D2	d2	NC5	OP3	L5	M1 5	M2 5	H1 5	X
	D3	d1	NC4	OP2	L4	M1 4	M2 4	H1 4	X
	D4	a3	NC3	NC1m	L3	M1 3	M2 3	H1 3	X
	D5	a2	NC2	m2	L2	M1 2	M2 2	H1 2	X
	D6	a1	NC1	m1	L1	M1 1	M2 1	H1 1	X
		Envelope	Channel off	Various	Drawbar level on four footages only for octave outputs				Test

Register 9 - R9 selects the ADR envelope parameters for ADSR control (see fig. 6)

Attack – a1 - a2 - a3 = 3 bit
Decay – d1 - d2 = 2 bit
Release – r1 - r2 - r3 = 3 bit
} 8 bit

Fig. 6 - ADSR envelope control

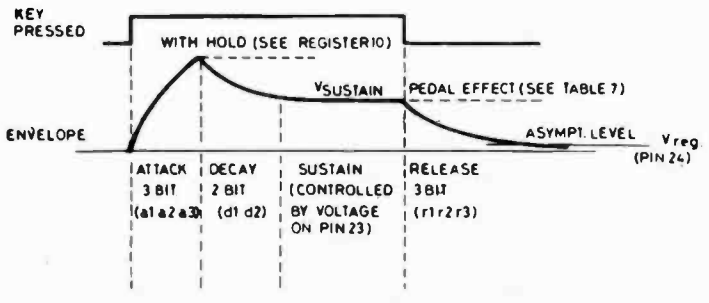


Table 7 shows the various time constants for Attack, Decay and Release.

TABLE 7

s3	s2	s1	Attack		
	d2	d1		Decay	
r3	r2	r1			Release
0	0	0	T/2	4T	* ∞
0	0	1	T	8T	T
0	1	0	2T	16T	2T
0	1	1	4T	32T	4T
1	0	0	8T		8T
1	0	1	16T		16T
1	1	0	32T		32T
1	1	1	64T		64T

* In this case it is possible to obtain the pedal effect.
T = 3 ms is the typical time constant unit with 8 external capacitors of 1 μF connected to pins 26 to 33.

Register 10 - Contains 8 commands to exclude the corresponding sound channel from the non-enveloped footage outputs (FL-FM1-FM2)
0 = ON 1 = OFF

Register 11 - Contains the following 8 commands: m1 and m2 select one of the four footages available for the monophonic output (C1m) according to table 8.

TABLE 8

m1		0	1	0	1
m2		0	0	1	1
K	0	16'	8'	4'	2'
	7	10 2/3'	5 1/3'	2 2/3'	1 1/3'
	4	12 4/5'	6 2/5'	3 1/5'	1 3/5'

OP2-OP3 – Select the four output options described in table 1 according to table 9.

TABLE 9

BIT / OPTION	OP2	OP3
I	0	0
II	1	0
III	0	1
IV	1	1

HOLD - If 0, disconnects the external 8 capacitors of envelope (1 μF) and the $V_{SUSTAIN}$ pin (pin 23) in the decay phase.

PO (Percussion Off) - If 1, the percussion input is inhibited (see pin 22 description).

NC1m-If1, eliminates channel 1 from all outputs except the 3 footage outputs not enveloped (it can be eliminated from these outputs through the command NC1 of register 10).

N.B. NC1m command is inoperative on the monophonic output (C1m) where channel 1 is always present.

Registers 12-13-14-15
These registers contain the drawbar control for 4 footages on the octave related output.
Footages L, M1, M2 and H1 are controlled in 32 linear levels or for example, using conversion table in the microprocessor in 8 or 16 logarithmic levels.
Table 10 shows an example of footage L with 32, 16 and 8 step control in dB.

Pin 12 - VT - ADR Control

It is used to adjust the ADR time constant for several M112s used in the same application. Using a single M112 it has to be connected to V_{DD}.

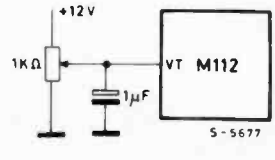


TABLE 10

L 5	L 4	L 3	L 2	L 1	Attenuation in dB		
					32 steps	16 steps	8 steps
0	0	0	0	0	OFF	OFF	OFF
0	0	0	0	1	-29.8	-29.8	-29.8
0	0	0	1	0	-23.8	-23.8	-23.8
0	0	0	1	1	-20.3	-20.3	-20.3
0	0	1	0	0	-17.8	-17.8	
0	0	1	0	1	-15.8	-15.8	
0	0	1	1	0	-14.3	-14.3	-14.3
0	0	1	1	1	-12.9		
0	1	0	0	0	-11.8	-11.8	
0	1	0	0	1	-10.7		
0	1	0	1	0	-9.8	-9.8	
0	1	0	1	1	-9.0		-9.0
0	1	1	0	0	-8.2	-8.2	
0	1	1	0	1	-7.5		
0	1	1	1	0	-6.9	-6.9	
0	1	1	1	1	-6.3		
1	0	0	0	0	-5.7	-5.7	
1	0	0	0	1	-5.2		
1	0	0	1	0	-4.7		
1	0	0	1	1	-4.2	-4.2	-4.2
1	0	1	0	0	-3.8		
1	0	1	0	1	-3.4		
1	0	1	1	0	-3.0	-3.0	
1	0	1	1	1	-2.6		
1	1	0	0	0	-2.2		
1	1	0	0	1	-1.9		
1	1	0	1	0	-1.5	-1.5	
1	1	0	1	1	-1.2		
1	1	1	0	0	-0.9		
1	1	1	0	1	-0.58		
1	1	1	1	0	-0.29		
1	1	1	1	1	0	0	0

Pin 14 to 20 - FM1, FM2, FM2E, FM1E, FH1E, FLE, FL (Footages output)

The "wired-or" function is possible on all outputs.
The non enveloped outputs (with constant DC level) are push-pull current generators.
The enveloped outputs (with non constant DC level) are open drain sink current generators. Output duty cycle is 50%.

Pin 21 - C1m

Monophonic output of channel 1 (always present). Duty cycle of the waveform is 50%.

Pin 22 - Percussion M2

Using a specific signal on this input it is possible to have a percussion effect on M2 footage for the octave related output.

Pin 23 - $V_{SUSTAIN}$

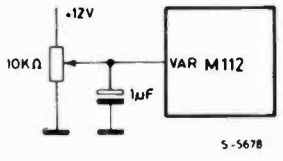
This input defines the level of sustain (see fig. 6).

Pin 24 - V_{reg}

This pin controls the asymptote of $V_{RELEASE}$ through the gate of a transistor which discharges the envelope capacitor. If the performance at the end of release time is considered satisfactory, this pin must be connected to V_{SS}. Otherwise this input can be connected to a voltage not higher than 1V.

Pin 25 - VAR Analog release

This pin is intended for analog control of the release time constant when it is required in addition to the digital one controlled by software.



It allows intermediate values not included in table 7 (see explanation of register 9). In the case of pedal effect connect this input to V_{SS}.

Pin 26 to 33 - CH1, CH8 Envelope capacitor inputs

8 capacitors (typical value = 1μF) have to be connected for the ADSR envelopes.

Pin 34 to 40 - O1E, O7E Octave Outputs

Octave related outputs. Duty cycle is 50%.

Programmable Analog Compandor

DESCRIPTION

The NE572 is a dual channel, high performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full wave rectifier to detect the average value of input signal; a linearized, temperature compensated variable gain cell (ΔG) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

The NE572 is intended for noise reduction in high performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

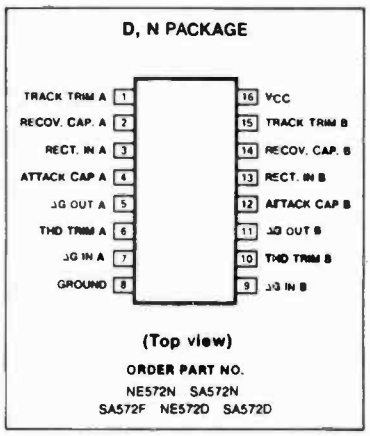
FEATURES

- Independent control of attack and recovery time.
- Improved low frequency gain control ripple
- Complementary gain compression and expansion with external Op Amp
- Wide dynamic range—greater than 110dB
- Temperature compensated gain control
- Low distortion gain cell
- Low noise—6μV typical
- Wide supply voltage range—6V-22V
- System level adjustable with external components.

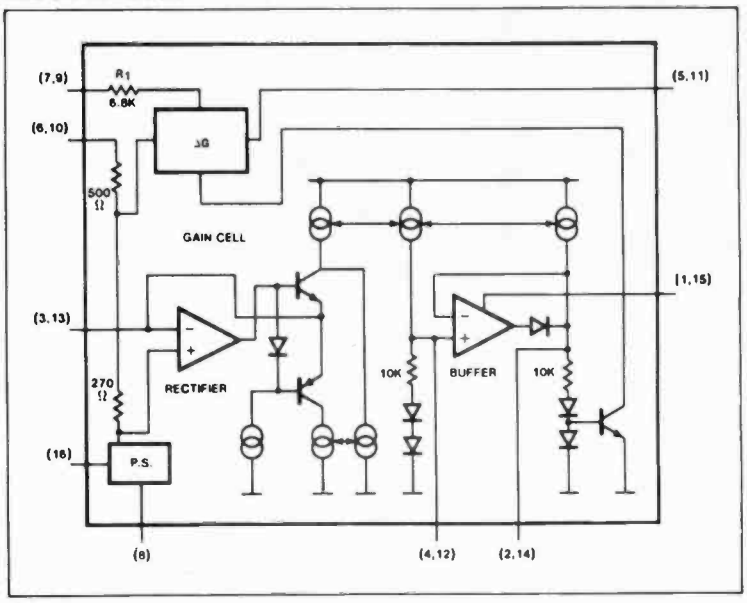
APPLICATIONS

- Dynamic noise reduction system
- Voltage control amplifier
- Stereo expandor
- Automatic level control
- High level limiter
- Low level noise gate
- State variable filter

PIN CONFIGURATION



BLOCK DIAGRAM



Note:
1. Supplied only in large SO (Small Outline) package.

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	22	VDC
T_A	Operating temperature range	0 to 70	°C
P_D	Power dissipation	500	mW

AUDIO SIGNAL PROCESSING IC COMBINES VCA AND FAST ATTACK-SLOW RECOVERY LEVEL SENSOR

In high performance audio gain control applications it is desirable to independently control the attack and recovery time of the gain control signal. This is true, for example, in compandor applications for noise reduction. In high end systems the input signal is usually split into two or more frequency bands to optimize the dynamic behavior for each band. This reduces low frequency distortion due to control signal ripple, phase distortion, high frequency channel overload and noise modulation. Because of the expense in hardware, multiple band signal processing up to now was limited to professional audio applications.

With the introduction of the Signetics NE572 this high performance noise reduction concept becomes feasible for consumer hi fi applications. The NE572 is a dual channel gain control IC. Each channel has a linearized, temperature compensated gain cell and an improved level sensor. In conjunction with an external low noise op amp for current to voltage conversion, the VCA features low distortion, low noise and wide dynamic range. The novel level sensor which provides gain control current for the VCA gives lower gain control ripple and independent control of fast attack, slow recovery dynamic response. An attack capacitor CA with an internal 10K resistor RA defines the attack time TA. The recovery time TR of a tone burst is defined by a recovery capacitor CR and an internal 10K resistor R_R. Typical attack time of 4MS for the high frequency spectrum and 40MS for the low frequency band can be obtained with .1μF and 1.0μF attack capacitors respectively. Recovery time of 200MS can be obtained with a 4.7μF external capacitor. With the recovery capacitor added in the level sensor, the gain control ripple for low frequency signals is much lower than that of a simple RC ripple filter. As a result the residual third harmonic distortion of low frequency signal in a two quad transconductance amplifier is greatly improved. With the 1.0μF attack capacitor and 4.7μF recovery capacitor for a 100HZ signal the third harmonic distortion is improved by more than 10db over the simple RC ripple filter with a single 1.0μF attack and recovery capacitor, while the attack time remains the same.

The NE572 is assembled in a standard 16 pin dual in line plastic package and in oversized SO (Small Outline) package. It operates over wide supply range from 6V to 22V. Supply current is less than 6mA. The NE572 is designed for consumer application over a temperature range 0-70°C. The SA572 is intended for applications from – 40°C to + 85°C.

NE572 BASIC APPLICATIONS

Description

The NE572 consists of two linearized, temperature compensated gain cells (ΔG) each with a full-wave rectifier and a buffer amplifier as shown in the block diagram. The two channels share a 2.5V common bias reference derived from the power supply but otherwise operate independently. Because of inherent low distortion, low noise and the capability to linearize large signals, a wide dynamic range can be obtained. The buffer amplifiers are provided to permit control of attack time and recovery time independent of each other. Partitioned as shown in the block diagram, the IC allows flexibility in the design of system levels that optimize DC shift, ripple distortion, tracking accuracy and noise floor for a wide range of application requirements.

Gain Cell

Figure 1 shows the circuit configuration of the gain cell. Bases of the differential pairs

$Q_1 - Q_2$ and $Q_3 - Q_4$ are both tied to the output and inputs of OPA A_1. The negative feedback through Q_1 holds the V_{BE} of $Q_1 - Q_2$ and the V_{BE} of $Q_3 - Q_4$ equal. The following relationship can be derived from the transistor model equation in the forward active region.

$$\Delta V_{BE_{Q_3-Q_4}} = \Delta_{BE_{Q_1-Q_2}}$$

$(V_{BE} = V_T \ln IC/IS)$

$$V_T \ln\left(\frac{\frac{1}{2}I_G + \frac{1}{2}I_O}{I_S}\right) - V_T \ln\left(\frac{\frac{1}{2}I_G - \frac{1}{2}I_O}{I_S}\right)$$

$$= V_T \ln\left(\frac{I_1 + I_{in}}{I_S}\right) - V_T \ln\left(\frac{I_2 - I_1 - I_{in}}{I_S}\right) \quad \text{--(2)}$$

where $I_{in} = \frac{V_{in}}{R_1}$

$R_1 = 6.8K$

$I_1 = 140\mu A$

$I_2 = 280\mu A$

I_O is the differential output current of the gain cell and I_G is the gain control current of the gain cell.

If all transistors Q_1 through Q_4 are of the same size, equation (2) can be simplified to:

$$I_O = \frac{2}{I_2} \cdot I_{in} \cdot I_G - \frac{1}{I_2}(I_2 - 2I_1) \cdot I_G \qquad (3)$$

The first term of eqn. (3) shows the multiplier relationship of a linearized two quadrant transconductance amplifier. The second term is the gain control feed through due to the mismatch of devices. In the design this has been minimized by large matched devices and careful layout. Offset voltage is caused by the device mismatch and it leads to even harmonic distortion. The offset voltage can be trimmed out by feeding a current source within $\pm 25\mu A$ into the THD trim pin. The residual distortion is third harmonic distortion and is caused by gain control ripple. In a compandor system, available control of fast attack and slow recovery improves ripple distortion significantly. At the unity gain level of 100mV, the gain cell gives THD (total harmonic distortion) of .17% TYP. Output noise with no input signals is only $6\mu V$ in the audio spectrum (10HZ-20KHZ). The output current I_O must feed the virtual ground input of an operational amplifier with a resistor from output to inverting input. The non-inverting input of the operational amplifier has to be biased at VREF if the output current I_O is dc coupled.

Rectifier

The rectifier is a full-wave design as shown in Figure 2. The input voltage is converted to current through the input resistor R2 and turns on either Q5 or Q6 depending on the signal polarity. Deadband of the voltage to current converter is reduced by the loop gain of the gain block A2. If AC coupling is used, the rectifier error comes only from input bias current of gain block A2. The input bias current is typically about 70nA. Frequency response of the gain block A2 also causes second order error at high frequency. The collector current of Q6 is mirrored and summed at the collector of Q5 to form the full wave rectified output current I_R. The rectifier transfer function is

$$\frac{V_{IN} - V_{REF}}{R_2} \qquad (4)$$

If Vin is A.C. coupled, then the equation will be reduced to:

$$I_{RAC} = \frac{Vin\,(AVG)}{R_2}$$

The internal bias scheme limits the maximum output current I_R to be around $300\mu A$. Within a $\pm$ 1dB error band the input range of the rectifier is about 52dB.

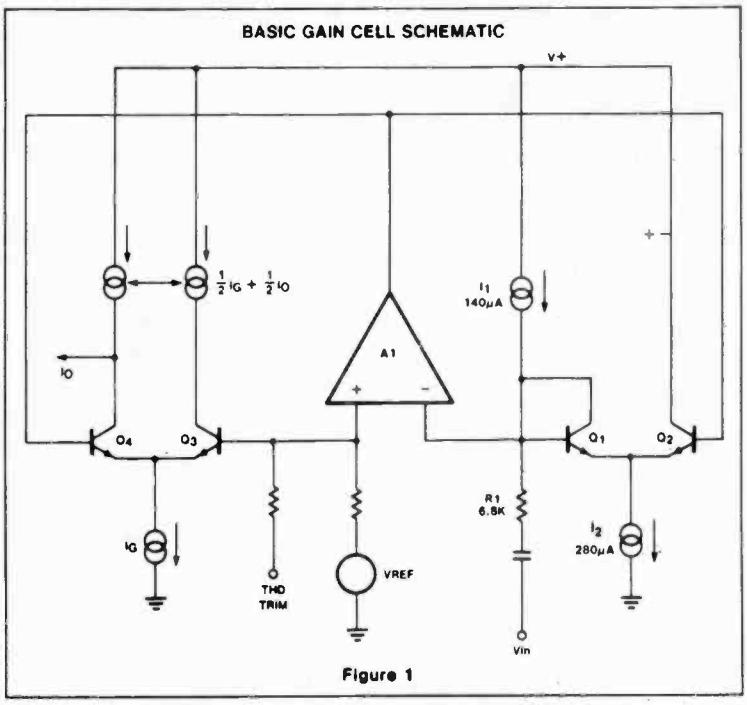


Figure 1

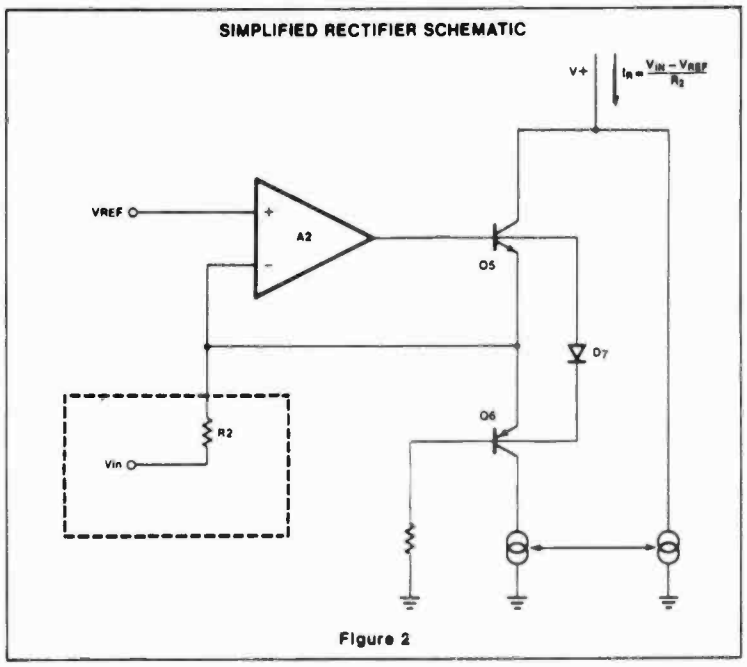


Figure 2

Buffer Amplifier

In audio systems, it is desirable to have fast attack time and slow recovery time for a tone burst input. The fast attack time reduces transient channel overload but also causes low frequency ripple distortion. The low frequency ripple distortion can be improved with the slow recovery time. If different attack times are implemented in corresponding frequency spectrums in a split band audio system, high quality performance can be achieved. The buffer amplifier is designed to make this feature available with minimum external components. Referring to Figure 3, the rectifier output current is mirrored into the input and output of the unipolar buffer amplifier A_3 through Q_8, Q_9 and Q_{10}. Diodes D_{11} and D_{12} improve tracking accuracy and provide common mode bias for A_3. For a positive going input signal, the buffer amplifier acts like a voltage follower. Therefore, the output impedance of A_3 makes the contribution of capacitor CR to attack time insignificant. Neglecting diode impedance the gain Ga(t) for ΔG can be expressed as follows.

$$Ga(t) = (Ga_{INT} - Ga_{FNL}) \cdot e^{\frac{-t}{\tau A}} + Ga_{FNL}$$

Ga_{INT} = Initial Gain

$\tau A = R_A \cdot CA = 10K \cdot CA$ Ga_{FNL} = Final Gain

where τA is the attack time constant and RA is a 10K internal resistor. Diode D_{15} opens the feedback loop of A_3 for a negative going signal if the value of capacitor CR is larger than capacitor CA. The recovery time depends only on CR • R_R. If the diode impedance is assumed negligible, the dynamic gain G_R (t) for ΔG is expressed as follows.

$$G_R(t) = (G_{R\,INT} - G_{R\,FNL}) \cdot e^{\frac{-t}{\tau R}} + G_{R\,FNL}$$

$$\tau R = R_R \cdot CR = 10K \cdot CR$$

where τR is the recovery time constant and R_R is a 10K internal resistor. The gain control current is mirrored to the gain cell through Q_{14}. The low level gain errors due

to input bias current of A_2 and A_3 can be trimmed through the tracking trim PIN into A_3 with a current source of $\pm 3\mu A$.

Basic Expandor

Figure 4 shows an application of the circuit as a simple expandor. The gain expression of the system is given by

$$\frac{V_{OUT}}{V_{IN}} = \frac{2}{I_1} \cdot \frac{R_3 \cdot V_{IN(AVG)}}{R_2 \cdot R_1 \ (I_1 = 140\mu A)} \quad (5)$$

Both the resistors R_1 and R_2 are tied to internal summing nodes. R_1 is a 6.8K internal resistor. The maximum input current into the gain cell can be as large as 140μA. This corresponds to a voltage level of 140μA • 6.8K = 952mV peak. The input peak current into the rectifier is limited to 300μA by the internal bias system. Note that the value of R_1 can be increased to accommodate higher input level. R_2 and R_3 are external resistors. It is easy to adjust the ratio of R3/R2 for desirable system voltage and current levels. A small R2 results in higher gain control current and smaller static and dynamic tracking error. However, an impedance buffer A_1 may be necessary if the input is voltage drive with large source impedance.

The gain cell output current feeds the summing node of the external OPA A_2. R_3 and A_2 convert the gain cell output current to the output voltage. In high performance applications, A_2 has to be low noise, high speed and wide band so that the high performance output of the gain cell will not be degraded. The non-inverting input of A_2 can be biased at the low noise internal reference PIN 6 or 10. Resistor R_4 is used to biased up the output DC level of A_2 for maximum swing. The output DC level of A_2 is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R_3}{R_4}\right) - V_B \frac{R_3}{R_4} \quad (6)$$

V_B can be tied to a regulated power supply for a dual supply system and be grounded for a single supply system. CA sets the attack time constant and CR sets the recovery time constant.

Basic Compressor

Figure 5 shows the hook-up of the circuit as a compressor. The IC is put in the feedback loop of the OPA A_1. The system gain expression is as follows:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{I_1}{2} \cdot \frac{R_2 \cdot R_1}{R_3 \cdot V_{IN\,(AVG)}}\right)^{1/2} \quad (7)$$

RDC1, RDC2, and CDC form a dc feedback for A_1. The output DC level of A_1 is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R_{DC1} + R_{DC2}}{R_4}\right) - V_B \cdot \left(\frac{R_{DC1} + R_{DC2}}{R_4}\right) \quad (8)$$

The zener diodes D_1 and D_2 are used for channel overload protection.

Basic Compandor System

The above basic compressor and expandor can be applied to systems such as tape/disc noise reduction, digital audio, bucket brigade delay lines. Additional system design techniques such as bandlimiting, band splitting, pre-emphasis, de-emphasis and equalization are easy to incorporate. The IC is a versatile functional block to achieve a high performance audio system. Figure 6 shows the system level diagram for reference.

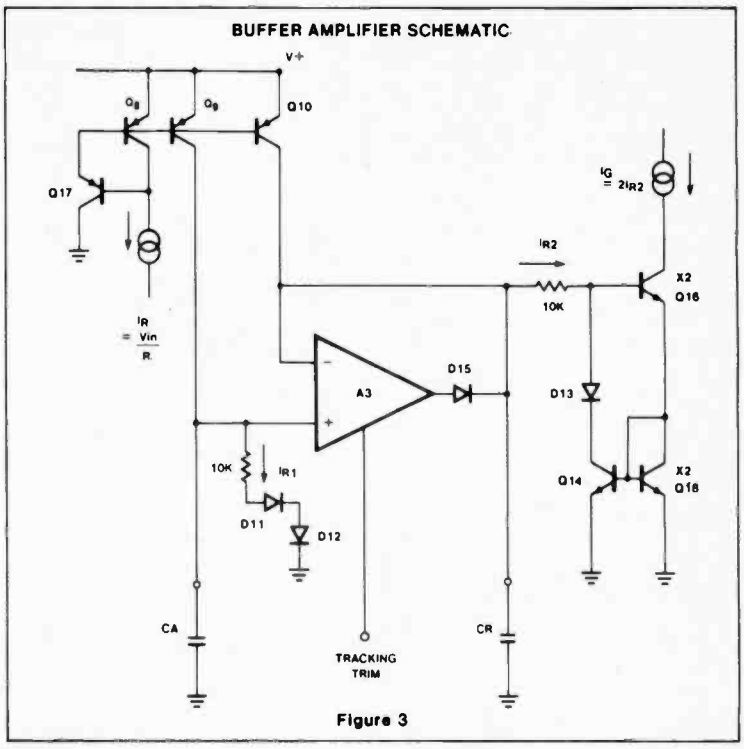


Figure 3

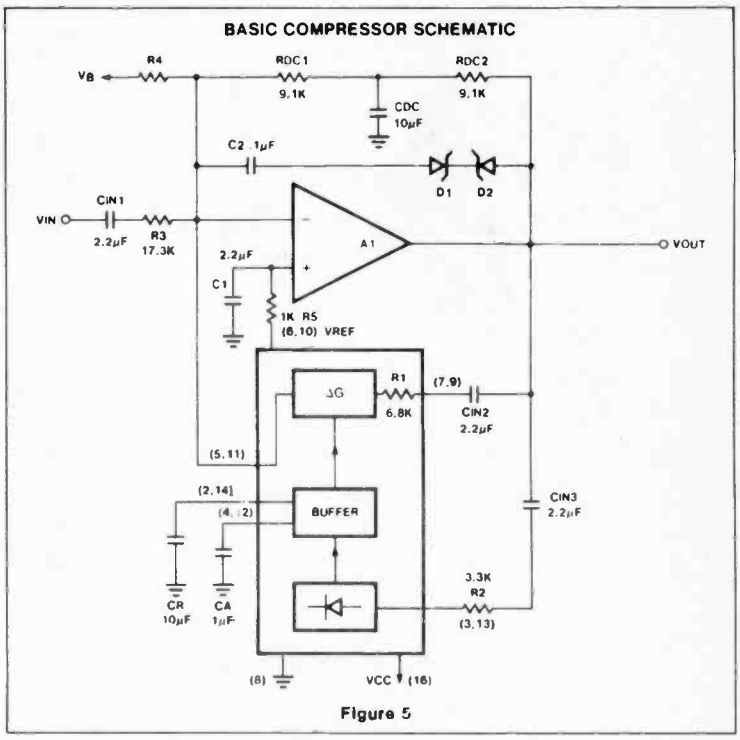


Figure 5

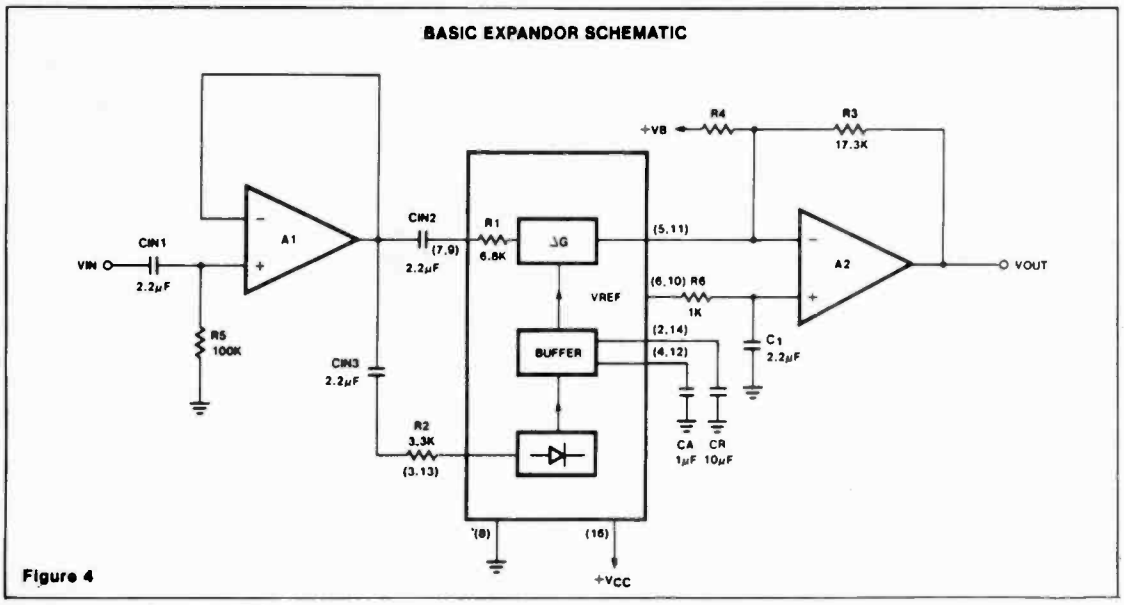


Figure 4

ELECTRICAL CHARACTERISTICS Standard Test Conditions (unless otherwise noted) V_{CC} = 15V TA = 25°C Expandor mode (see test circuit) Input signals at unity gain level (OdB) = 100mV RMS at 1KHz, $V_1 = V_2$, R_2 = 3.3K, R_3 = 17.3K

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		6		22	V_{DC}
I_{CC}	Supply current	No Signal			6	mA
	Internal voltage reference		2.3	2.5	2.7	V_{DC}
THD	(untrimmed)	1kHz C_A = 1.0μF		.2	1.0	%
THD	(trimmed)	1kHz C_R = 10μF		.05		%
THD	(trimmed)	100Hz		.25		%
	No signal output noise	Input to V_1 and V_2 grounded (20-20kHz)		6	25	uV
	DC level shift (untrimmed)	Input change from no signal to 100mV RMS		±20	±50	MV
	Unity gain level		−1	0	+1	dB
	Large signal distortion	$V_1 = V_2$ = 400mV		0.7	3.0	%
	Tracking error (measured relative to value at unity gain output) = [$V_O - V_O$(unity gain)] dB − V_2 (dBm)	Rectifier input V_2 = +6dB, V_1 = OdB V_2 = −30dB, V_1 = OdB		±.2 ±.5	 −1.5 +.8	dB
	Channel crosstalk	200mV RMS into channel A, measured output on channel B	60			dB
	Power supply rejection ratio	120Hz		70		dB

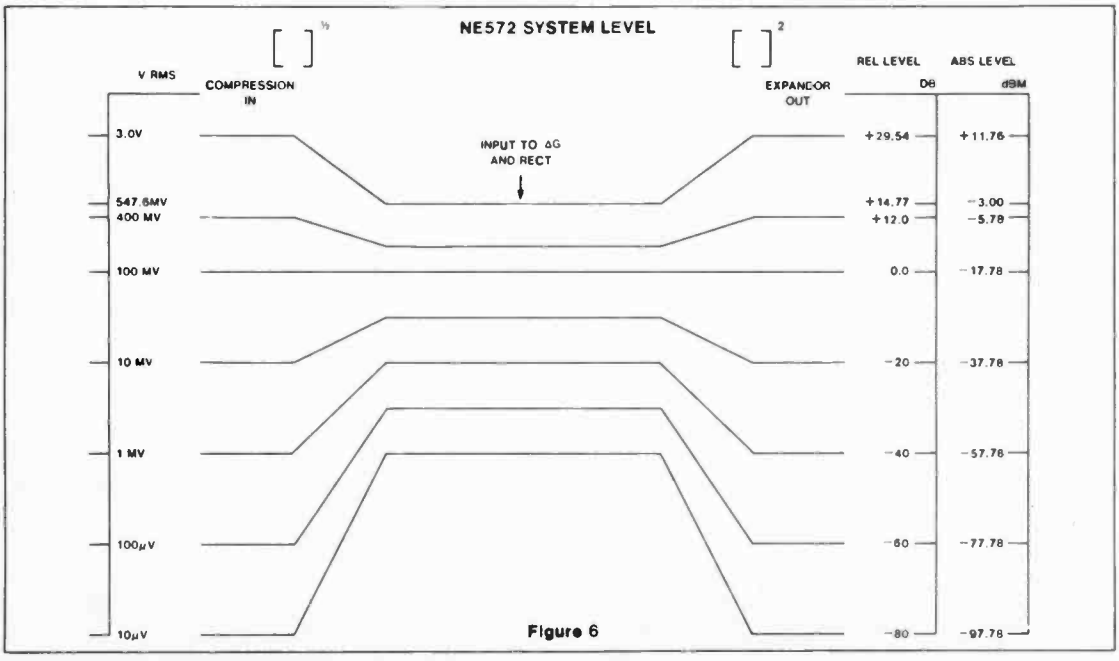


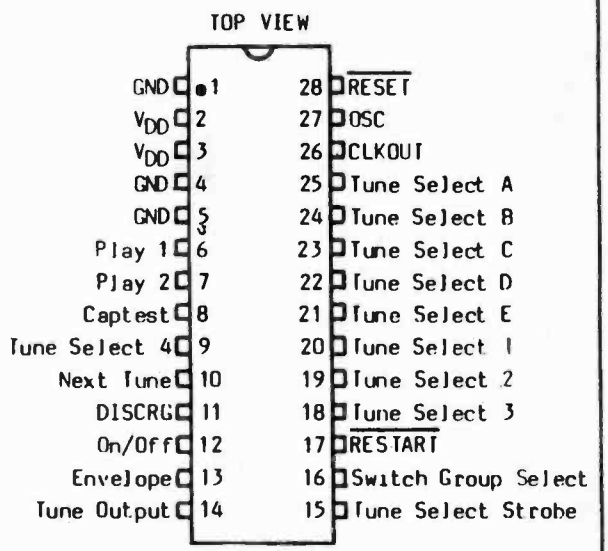
Figure 6

TUNES SYNTHESIZER

FEATURES

- 25 Different Tunes Plus 3 Chimes
- Mask Programmable with Customer Specified Tunes for Toys, Musical Boxes, etc.
- Minimal External Components
- Automatic Switch-Off Signal at End of Tune for Power Savings
- Sequential Tune Mode
- Envelope Control to Give Organ or Piano Quality
- 4 Door Capability When Used as Doorchime
- Operation with Tunes in External PROM if Required
- Single Supply Operation

PIN CONFIGURATION
28 LEAD DUAL IN LINE



DESCRIPTION

The AY-3-1350 is an N-Channel MOS microcomputer based synthesizer of preprogramed tunes for applications in toys, musical boxes, and door-chimes. The standard device has a set of 25 different popular and classical tunes chosen for their international acceptance. In addition there are 3 chimes making a total of 28 tunes.

The chip is mask-programable during manufacture enabling the quantity user to select his own music. Up to 28 tunes of varying length can be chosen.

TUNES

The standard AY-3-1350 contains the following tunes:

A0	Toreador	A3	O Sole Mio
B0	William Tell	B3	Santa Lucia
C0	Hallelujah Chorus	C3	The End
D0	Star Spangled Banner	D3	Blue Danube
E0	Yankee Doodle	E3	Brahms' Lullaby
A1	John Brown's Body	A4	Bell's Bells
B1	Clementine	B4	Jingle Bells
C1	God Save the Queen	C4	La Vie en Rose
D1	Colonel Bogey	D4	Star Wars
E1	Marseillaise	E4	Beethoven's 9th
A2	America, America	Chime X	Westminster Chime
B2	Deutschland Leid	Chime Y	Simple Chime
C3	Wedding March	Chime Z	Descending Octave Chime
D2	Beethoven's 5th		
E2	Augustine		

PIN FUNCTIONS

Pin #'s	Signal	Function
1,4,5	GND	Ground.
2,3	V_{DD}	Primary supply voltage.
6	Play 1	When activated by a logic low, it generates Decending Octave Chime.
7	Play 2	When activated by a logic low, it generates one of the five tunes depending upon selection of Tune Select A through Tune Select E pins (Tunes AØ-EØ). If Tune Select A thru Tune Select E is not selected, simple chime is played.
8	Captest	Works in conjunction with signal DISCRG to determine the speed of the tune. Depending upon the rise time of the voltage at this pin, the tune will play faster or slower.
20,19,18,9	Tune Select 1 thru Tune Select 4	When power is applied to pin 2, the chip scans Play 1, Play 2, Tune Select A thru E and Tune Select 1 thru 4 (Ref. Table 2, 3, & 4) and plays the tune as selected by these pins.
21,22,23, 24,25	Tune Select A thru Tune Select E	
10	Next Tune	Scanned externally by Tune Select 4 (Pin 9). If Pin #10 is at a logic low, then the next tune selected will play.
11	DISCRG	Works in conjunction with Captest (Pin 8). Controls the speed of the tune.
12	On/Off	At power on, it is logic low voltage. At the end of the tune, it goes to open. This pin can be used to control the power of the chip.
13	Envelope	Controls overall volume and quality of the tune. Relates to the tapering of the musical notes.
14	Tune Output	Outputs the tune.
15	Tune Select Strobe	Detects selection of Tune Select 1-4. If none is selected, Tune Select Ø is assumed.
16	Switch Group Select	Based upon the connection of this pin to Tune Select 1-4, one of the five tunes will be played. The tunes selected are based upon the position of the Tune Select A thru F (Reference Table 1).
17	$\overline{\text{RESTART}}$	Scanned externally by Tune Select 4 (Pin 9). If $\overline{\text{RESTART}}$ is at a logic low, then the same tune will play providing power is continued to be applied to the chip.
26	CLKOUT (output)	Signal timing of frequency equal to oscillator frequency (Pin 27) divided by four. May be used by external devices to synchronize to the oscillator timing.
27	OSC (input)	Oscillator input. This signal can be driven by an external oscillator if a precise frequency of operation is required or an external RC network can be used to set the frequency of operation of the internal clock generator. This is a Schmitt trigger input. Oscillator frequency determines the pitch of the tune.
28	$\overline{\text{RESET}}$	Resets the system and initializes it.

OPERATION SUMMARY

Use of the AY-3-1350 can be split into three groups which are described in detail in separate sections:

ONE CHIP STANDARD AY-3-1350 SYSTEM generating 25 tunes plus 3 chimes which have been preprogramed into the standard device.

ONE CHIP CUSTOM TUNES SYSTEM generating any number of tunes desired. This involves mask programing during manufacture and is usually not suitable for small quantity production.

TWO CHIP STANDARD AY-3-1350/PROM SYSTEM generating any tunes desired as above, but using the standard device so that applications, including small quantities, become feasible.

ONE CHIP STANDARD AY-3-1350 SYSTEM

Typical Implementation

There are many ways to connect the standard device depending on the exact application. Figure 1 shows just one implementation of the device in a door-chime. This circuit gives access to all 25 tunes from switch A and one of 5 tunes from switch C as well as the descending octive chime from switch B. The tune selected for switch A follows the tunes list according to the setting of the two tune select switches (A-E and 0-4). The tune selected from switch C in Figure 1 is one of the five tunes A0 through E0 depending on the setting of the letter switch. Switch B always selects Descending Octave Chime independent of Tune Select switches. For example, with the letter switch set at E and number switch set at 4, the tunes available will be:

Switch A: Beethoven's 9th (E4)
Switch C: Yankee Doodle (E0)
Switch B: Descending Octave Chime (Chime Z)

When the letter switch is in position F there will be chimes on all doors independent of the number switch setting as follows:

Switch A: Westminster Chime
Switch C: Simple Chime
Switch B: Descending Octave Chime

There is virtually no power consumption in the standby condition (external transistor leakages only). When any door switch is activated the circuit powers up, plays a tune, and then automatically powers down again to conserve the battery, even if the operator keeps his finger on the switch to the end of the tune. He must release it and re-press to play again with the circuit in Figure 1. Activating any of the door switches will pull point A to ground turning on the PNP transistor in the power supply line. This causes +5V to be applied to the AY-3-1350 and the first operation of the chip is to put ON/OFF (pin 12) to logic 0. This maintains the power through the PNP, even after the switch is released. The device can turn off its own power at the end of a tune by raising ON/OFF to logic 1.

Figure 1 shows only a typical one-chip implementation. Further options come from use of different switching and/or from use of the next tune facilities built into the chip. These will now be considered in turn.

Switching Options

In figure 1 the Switch Group Select pin (16) is not connected, and one of the five tunes (A0 through E0) will play if switch C is activated. Other number groups can be chosen by connecting the Switch Group Select pin as follows:

TABLE 1

Switch Group Select pin (16) is connected to:	Tunes
no other pin	A0-E0
Tune Select 1 (pin 20)	A1-E1
Tune Select 2 (pin 19)	A2-E2
Tune Select 3 (pin 18)	A3-E3
Tune Select 4 (pin 9)	A4-E4

Which of the five possible tunes will be played depends on the current setting of the letter switch A-E.

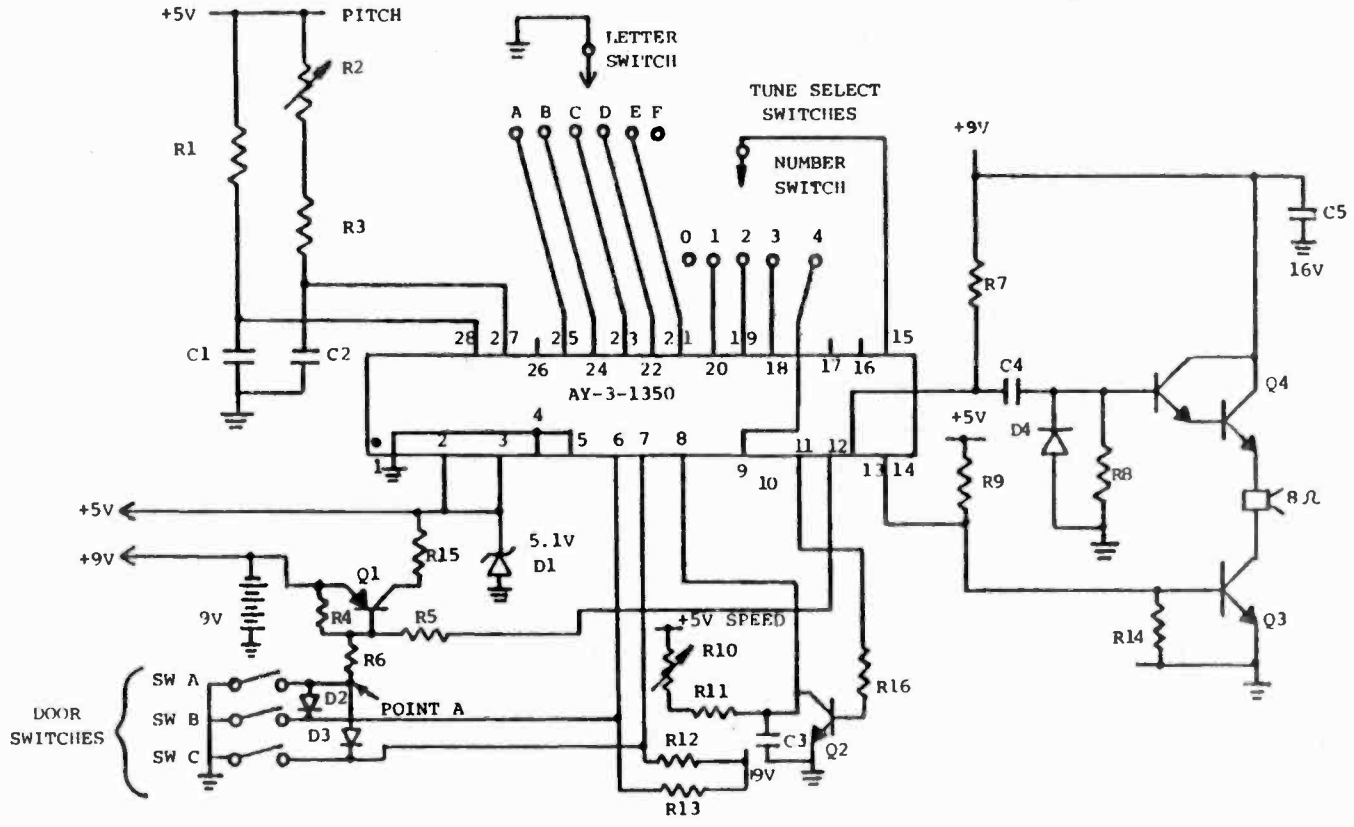
Switch Group Selection can be made by hard-wire connection for a permanent selection or a third switch can be added for an additional group selection feature.

Next Tune Facilities

At the end of tune play, the circuit of Figure 1 powers down because ON/OFF (pin 12) is raised to a logic 1. The simplified flow diagram in Figure 5 shows that before the power down there is a test for connection between NEXT TUNE (pin 10) or $\overline{\text{RESTART}}$ (pin 17) with TUNE SELECT 4 (pin 9). At this time NEXT TUNE (pin 10) then $\overline{\text{RESTART}}$ (pin 17), which are normally at logic 1, output a logic 0. This is looked for at input TUNE SELECT 4 (pin 9). If neither is found the power down system is reached as in Figure 1.

A NEXT TUNE (pin 10) - TUNE SELECT 4 (pin 9) connection at the moment of test causes the next tune in the list to be played after a short pause (equal to a musical breve - the actual time depends on the setting of the tune speed control). The order of the tunes is A0 to E4 as given in the listing of standard AY-3-1350 tunes. If the last tune (E4) was played then the circuit will go on to play the first tune A0 (and then successive ones). The chimes are not included in the cycling sequence.

Fig. 1 SYSTEM DIAGRAM



PARTS LIST

Resistors

Reference	Value
R1	100KΩ(1/4 or 1/2w)
R2	25KΩ(POT)
R3	4KΩ(1/4 or 1/2w)
R4, 16	10KΩ(1/4 or 1/2w)
R5,6,7	3.3KΩ(1/4 or 1/2w)
R8	47KΩ(1/4 or 1/2w)
R9	2.2KΩ(1/4 or 1/2w)
R10	1MΩ(POT)
R11	330KΩ(1/4 or 1/2w)
R12,13,14	33KΩ(1/4 or 1/2w)
R15	27 Ω(1/2w)

Capacitors

C1	0.1 μF (ceramic)
C2	47 pF
C3	0.22 μF
C4, 5	10 μF

Transistors

Reference	Value
Q1	PNP Transistor (MPS 2907)
Q2,3	NPN Transistor (MPS 3904)
Q4	Darlington Transistor (MPS A13)

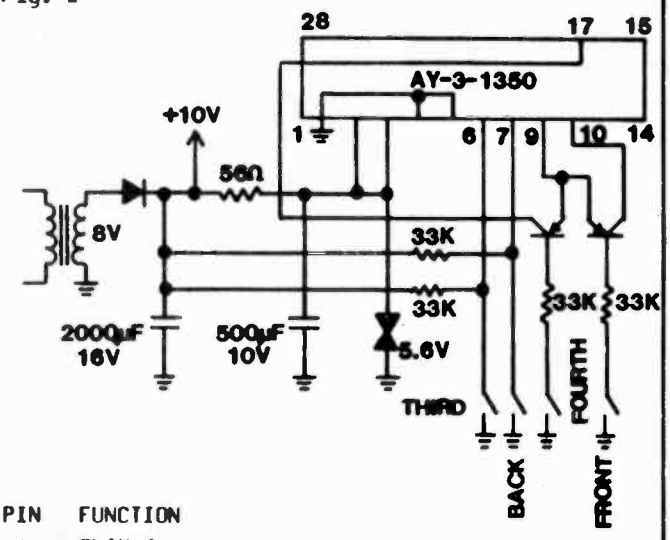
Diodes

D1	Zener Diode (5.1V) (1N4733)
D2,D3, D4	Diodes (1N914)
Speaker	8 ohms

A $\overline{\text{RESTART}}$ (pin 17) - TUNE SELECT 4 (pin 9) connection at the moment of test at the end of a tune causes the same selected tune to be played again. Figure 5 shows that in this case the tune sensing mechanism is passed through once more so the tune would be different the second time if the switches were altered while the first tune was playing.

The connections referred to cannot be permanent because otherwise the circuit would never stop playing tunes. Figure 2 shows how transistors are used to make the connection in a practical application.

Fig. 2



PIN	FUNCTION
6	PLAY 1
7	PLAY 2
9	TUNE SELECT 4
10	NEXT TUNE
17	$\overline{\text{RESTART}}$

ONE CHIP CUSTOM TUNES SYSTEM

Customizing the Tunes

The AY-3-1350 has pre-programmed tunes, but the device is mask programmable during manufacture with any music required. A minimum of 1 tune to a maximum of 28 tunes can be incorporated. Examples as follows:

Tunes	Total No. of notes, all tunes together	Average notes per tune
1	252	252
2	251	126
5	248	50
10	245	24
20	235	12
25	228	9

(The general formula is Total No. of notes = 255 - No. of tunes.)

Fig. 4 NOTE LENGTH TABLE

Name	Musical Notation	Octal	Binary
Sixteenth note		0	000
Eighth note		1	001
Three-sixteenth note		2	010
Quarter note		3	011
Three-eighths note		4	100
Half note		5	101
Three-quarter note		6	110
Whole note		7	111

Fig. 5 PROM Memory Allocation

Address	DATA	
0	377	(tunes select timeslot)
		Tune 1
	377	(end of tune marker)
		Tune 2
	377	(end of tune marker)
		More tunes
		Last tune
	377	(end of tune marker)
	376	(end of listing)
	000	
	000	
	000	Not used
	000	
377	125	(external ROM enable key)

Fig. 6 STAR SPANGLED BANNER - MUSIC

Fig. 3 SIMPLIFIED FLOW DIAGRAM

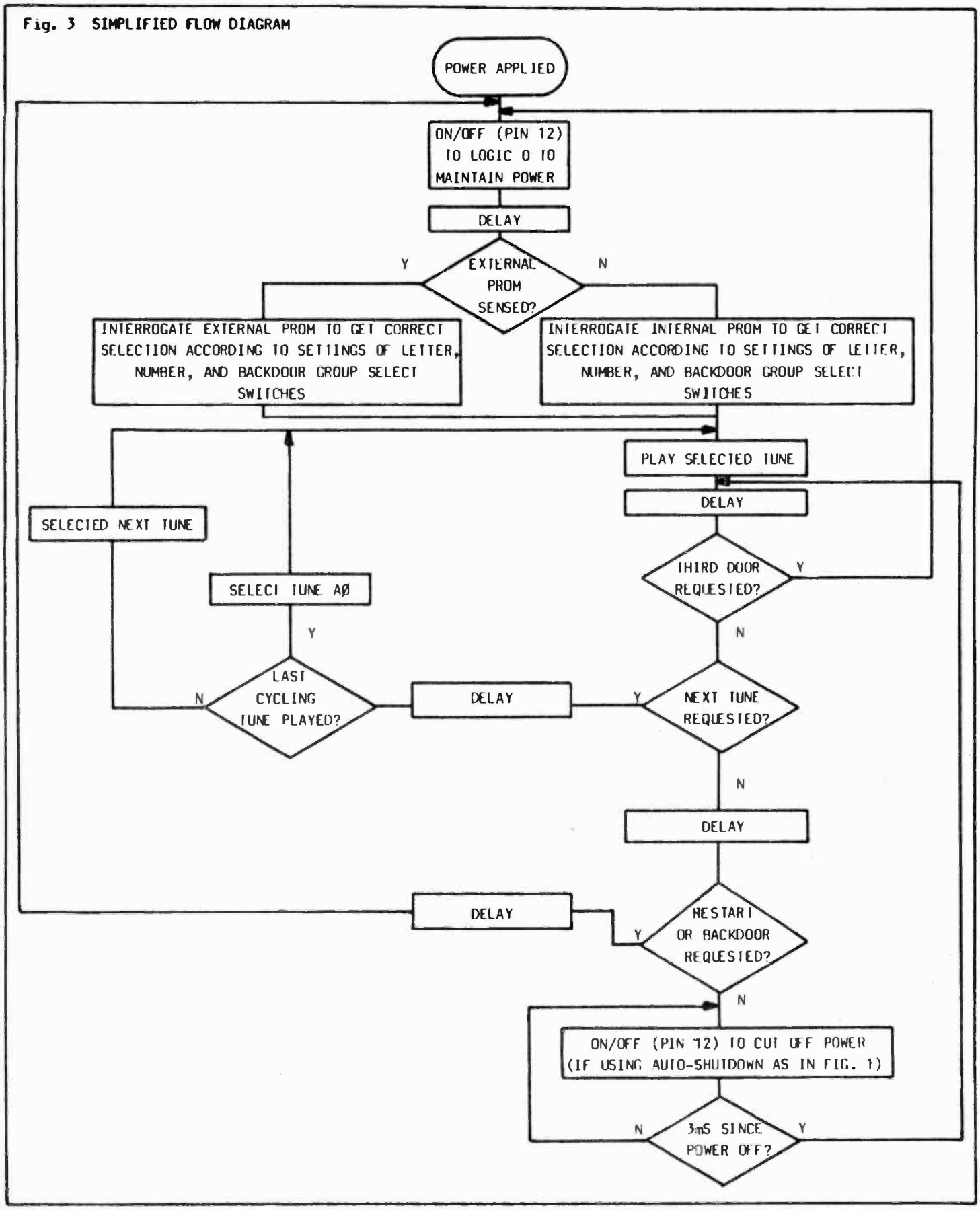


TABLE 2

SELECTION OF CHIMES

TUNE SELECT					TUNE SELECT				PLAY 1	PLAY 2	TUNE PLAYED
A	B	C	D	E	1	2	3	4			
1	1	1	1	1	X	X	X	X	1	1	Westminster Chime
1	1	1	1	1	X	X	X	X	0	1	Descending Octave Chime
1	1	1	1	1	X	X	X	X	1	0	Simple Chime

TABLE 3

SELECTION OF TUNES*

TUNE SELECT*					TUNE SELECT				PLAY 1	PLAY 2	TUNE PLAYED
A	B	C	D	E	1	2	3	4	1	1	
0	1	1	1	1	1	1	1	1	1	1	AØ
0	1	1	1	1	0	1	1	1	1	1	A1
0	1	1	1	1	1	0	1	1	1	1	A2
0	1	1	1	1	1	1	0	1	1	1	A3
0	1	1	1	1	1	1	1	0	1	1	A4
1	0	1	1	1	1	1	1	1	1	1	BØ
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
1	1	1	1	0	1	1	1	0	1	1	E4

*These tunes are activated when power is applied to the chip. In Fig. 1, it is achieved when switch A is depressed. Also, switch B = PLAY 1 and switch C = PLAY 2

TABLE 4

SELECTION OF TUNES

TUNE SELECT					TUNE SELECT				PLAY 1	PLAY 2	TUNE PLAYED
A	B	C	D	E	1	2	3	4			
1	1	1	1	1	X	X	X	X	1	0	Simple Chime
0	1	1	1	1	X	X	X	X	1	0	AØ
1	0	1	1	1	X	X	X	X	1	0	BØ
1	1	0	1	1	X	X	X	X	1	0	CØ
1	1	1	0	1	X	X	X	X	1	0	DØ
1	1	1	1	0	X	X	X	X	1	0	EØ
X	X	X	X	X	X	X	X	X	0	X	Descending Chimes

KEY: 0 = Switch activated
1 = Switch not activated
X = Do not care

As an indication, about 90 seconds of music can be incorporated. All musical rests are counted as one note. Semiquavers, quavers, dotted quavers, crotchets, dotted crotchets, minims, dotted minims and semibreves can all be accommodated. The range is about 2 1/2 octaves. The position of these octaves can be chosen by the user up to a maximum pitch of A=1760Hz.

Applications for Customized Tunes

If the number of tunes is less than the number of switch positions then the circuit will automatically proceed directly to power down if this power down mode is being used, or will find the next available tune if in the sequential mode.

All the different facilities described are still available when user tunes are masked into the device.

For toys, sequential tune playing adds variety and reduces the number of switches required, keeping costs to a minimum.

For musical boxes, playing the same tune repeatedly preserves the traditional features.

TWO CHIP STANDARD AY-3-1350/PROM SYSTEM

Introduction

With the addition of an external ROM or PROM the standard AY-3-1350 will play almost any tune or tunes desired. 28 tunes averaging 9 notes each or one tune of up to 252 notes is available, providing in all, about 1 to 2 minutes worth of music. General Instrument can later integrate the external tunes into the main synthesizer to give a one chip system.

Overall Coding Scheme

The external PROM should be 256 x 8 bits and of any static TTL compatible type.

It can have more words, but the tunes synthesizer will only use 256 x 8 bits at a time, e.g. if PROM type 2716 is used (2K x 8 bits), the three higher order address lines should be connected to ground or switches put on them to give 8 times the amount of music (see logic diagram Figure 9). The rest of this article will assume a 256 x 8 bit PROM, and the addresses will be referred to as 000 to 377. Octal notation is used throughout.

The PROM address 000 must contain data 377 and address 377 must contain data 125 which is a key to open up the external PROM features. All other addresses can contain tune data.

Each tune consists of a series of notes with one byte of PROM for each. Every tune must have a tune end marker byte 377 after the last note, and the final tune must have a byte 376 after the 377 end

Fig. 7 NOTE PITCH TABLE

NAME	FREQUENCY (Hz)	OCTAL	BINARY
F	175	00	00000
F#	185	01	00001
G	196	02	00010
G#	208	03	00011
A	220	04	00100
A#	233	05	00101
B	247	06	00110
C (middle C)	262	07	00111
C#	277	10	01000
D	294	11	01001
D#	311	12	01010
E	330	13	01011
F	349	14	01100
F#	370	15	01101
G	392	16	01110
G#	415	17	01111
A (international A)	440	20	10000
A#	466	21	10001
B	494	22	10010
C	523	23	10011
C#	554	24	10100
D	587	25	10101
D#	622	26	10110
E	659	27	10111
F	698	30	11000
F#	740	31	11001
G	784	32	11010
G#	831	33	11011
A	880	34	11100
A#	932	35	11101
B	988	36	11110
Rest	Silent	37	11111

Fig. 8 STAR SPANGLED BANNER - CODING

OCTAL DATA	BINARY DATA
232	10011010
200	10000000
143	01100011
203	10000011
233	10011011
305	11000101
377*	11111111

*The last 377 is the end of tune code

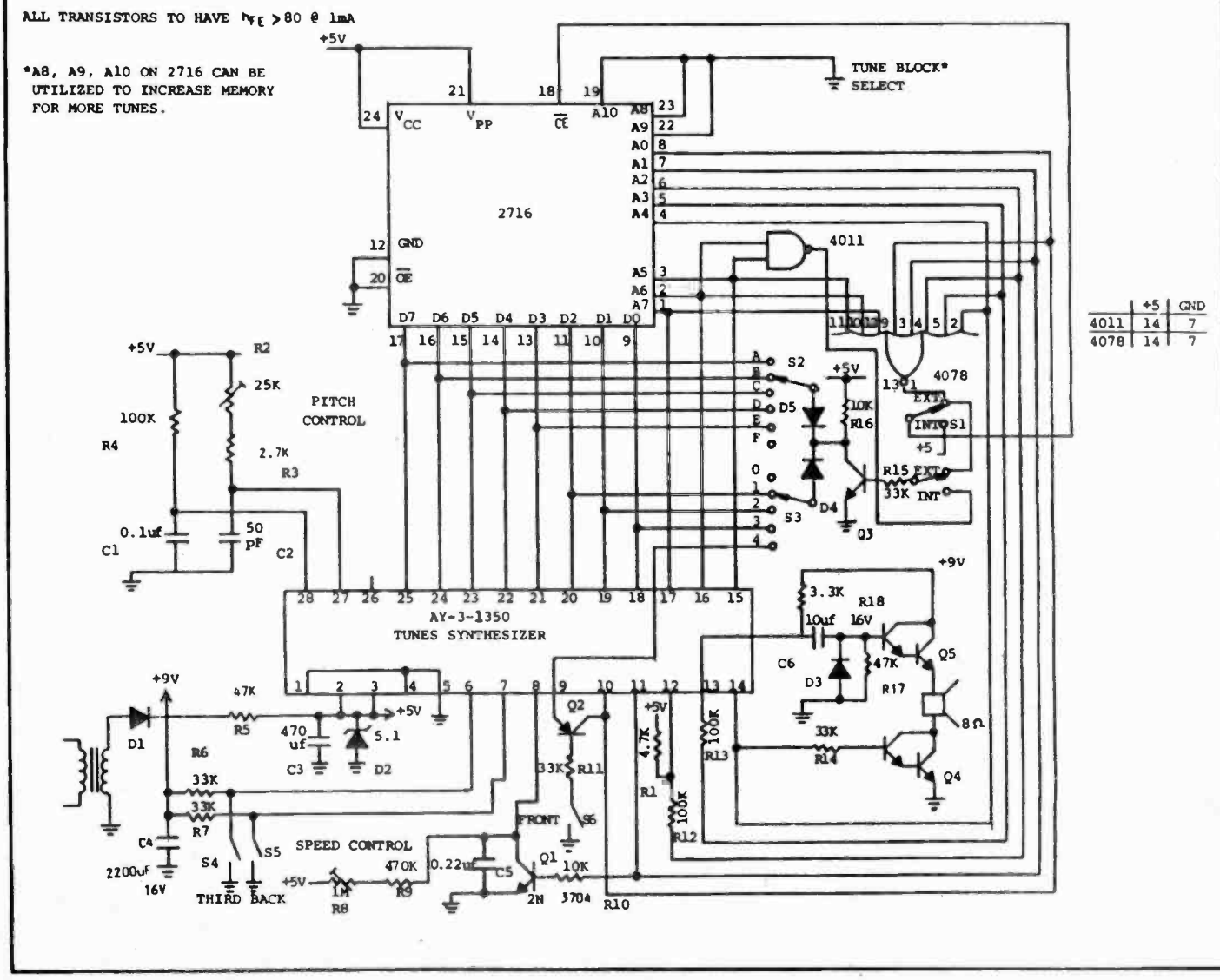
marker. The memory allocation is shown diagrammatically in Figure 5. Tunes can be of any length and there can be any number of them subject only to the memory limit (28 max.).

Each note of a tune occupies 1 byte (8 bits) of PROM, and this can be considered as split into two fields:

7	6	5	4	3	2	1	0
pitch					length		

The three least significant bits specify the length (half note, quarter note, etc.) and the five most significant bits specify the pitch. This gives 2^5 = 32 different pitches and 2^3 = 8 different lengths. In practice one pitch code is allocated as silence to allow musical rests of different lengths to be implemented. Figure 4 gives the length table and Figure 7 the note pitch table. It can be seen that the lengths from a sixteenth to a whole note, and 2 1/2 octaves of notes can be produced. The pitches shown assume that the on-chip clock of the AY-3-1350 is trimmed to 1MHz. The pitches can be made lower by using a slower clock. Every reduction by 5.61257% decreases the pitch by a semitone. The note pitches produced by the AY-3-1350 are approximately equi-tempered. It should be noted that codes 377 and 376 are used as end of tune markers and are illegal as notes. They correspond to whole and three-quarter note rests which can, however, be made up by combining two smaller rests in place of the required 377.

Fig. 9 PLAYING YOUR OWN TUNES WITH EXTERNAL PROM (OR INTERNAL TUNES)



	+5	GND
4011	14	7
4078	14	7

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Ambient temperature Under Bias..... 125°C
Storage Temperature..... -55°C to +150°C
Voltage on any pin
with Respect to V_{SS}..... -0.3V to +10.0V
Power Dissipation (Note 1)..... 1000mW

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied -- operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Conditions (unless otherwise stated):

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS
Operating Temperature T_A = 0°C to +70°C

Characteristic	Sym	Min	Typ*	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.5	-	7.0	V	
Primary Supply Current	I_{DD}	-	30	50	mA	All I/O pins @ V_{DD}
Input Low Voltage	V_{IL}	-0.2	-	0.8	V	
Input High Voltage (except $\overline{RESET}$, OSC, & pins 6, 7 and 8)	V_{IH}	2.4	-	V_{DD}	V	(Note 2)
Input Low-to-High Threshold Voltage ($\overline{RESET}$ & OSC)	V_{ILH}	V_{DD}-1	2.6	V_{DD}	V	
Output High Voltage (Note 3)	V_{OH}	2.4	-	V_{DD}	V	I_{OH}=-100μA (Note 1)
		3.5	-	V_{DD}	V	I_{OH}=0
Output Low Voltage	V_{OL}	-	-	0.45	V	I_{OL}=1.6mA, V_{XX}=4.5V
Input Leakage Current ($\overline{RESET}$, pins 6, 7, & 8)	I_{LC}	-5	-	+5	μA	$V_{SS} \leq V_{IN} \leq V_{DD}$
Output Leakage Current (open drain I/O pins 12 & 13)	I_{OLC}	-	-	10	μA	$V_{SS} \leq V_{PIN} \leq 10V$
Input Low Current (all I/O ports)	I_{IL}	-0.2	-0.6	-1.6	mA	V_{IL}=0.4V internal pullup
Input High Current (all I/O ports)	I_{IH}	-0.1	-0.4	-1.4	mA	V_{IH}=2.4V

*Typical data is at T_A = 25°C, V_{DD} = 5.0V

NOTES:
1. Positive current indicates current into pin. Negative current indicates current out of pin.
2. Pins 6, 7 and 8 have open drain inputs (no internal pullup resistor).
3. Except pins 12 and 13 which have open drain outputs.

Hardware Implementations

To play the 28 internal tunes of the AY-3-1350 Tunes Synthesizer, the device should be connected up as shown in the One Chip Standard AY-3-1350 System section. To play tunes which you have written into the PROM in the manner described above, the AY-3-1350 and the PROM should be interconnected as shown in Figure 9. This can be used for demonstrations, on-off implementations or small scale productions. This circuit will also play the internal tunes (See internal/external switch).

One Chip Implementation

For manufacturing purposes, send PROM and code listing to General Instrument and we will incorporate your tunes into a specially made one chip Tunes Synthesizer in place of the standard 28 tunes.

As a specific example, the music for the first part of Star Spangled Banner is shown in Figure 6 with the notes coded in octal below the music. Figure 8 represents just one of the tunes shown in the overall memory scheme of Figure 5 and it shows the actual data that would have to be incorporated into the external PROM to get a tune consisting of these 6 notes.

National Semiconductor

Digital Controlled Graphic Equalizer

General Description

The LMC835 is a monolithic, digitally-controlled graphic equalizer CMOS LSI for Hi-Fi audio. The LMC835 consists of a Logic section and a Signal Path section made of analog switches and thin-film silicon-chromium resistor networks. The LMC835 is used with external resonator circuits to make a stereo equalizer with seven bands, ±12 dB or ±6 dB gain range and 25 steps each. Only three digital inputs are needed to control the equalization. The LMC835 makes it easy to build a μP-controlled equalizer.

The signal path is designed for very low noise and distortion, resulting in very high performance, compatible with PCM audio.

Features

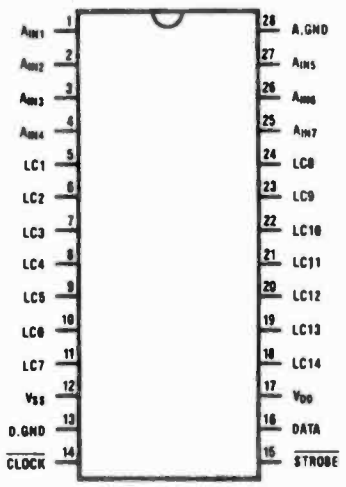
- No volume controls required
- Three-wire interface
- 14 bands, 25 steps each
- ±12 dB or ±6 dB gain ranges
- Low noise and distortion
- TTL, CMOS logic compatible

Applications

- Hi-Fi equalizer
- Receiver
- Car stereo
- Musical instrument
- Tape equalization
- Mixer
- Volume controller

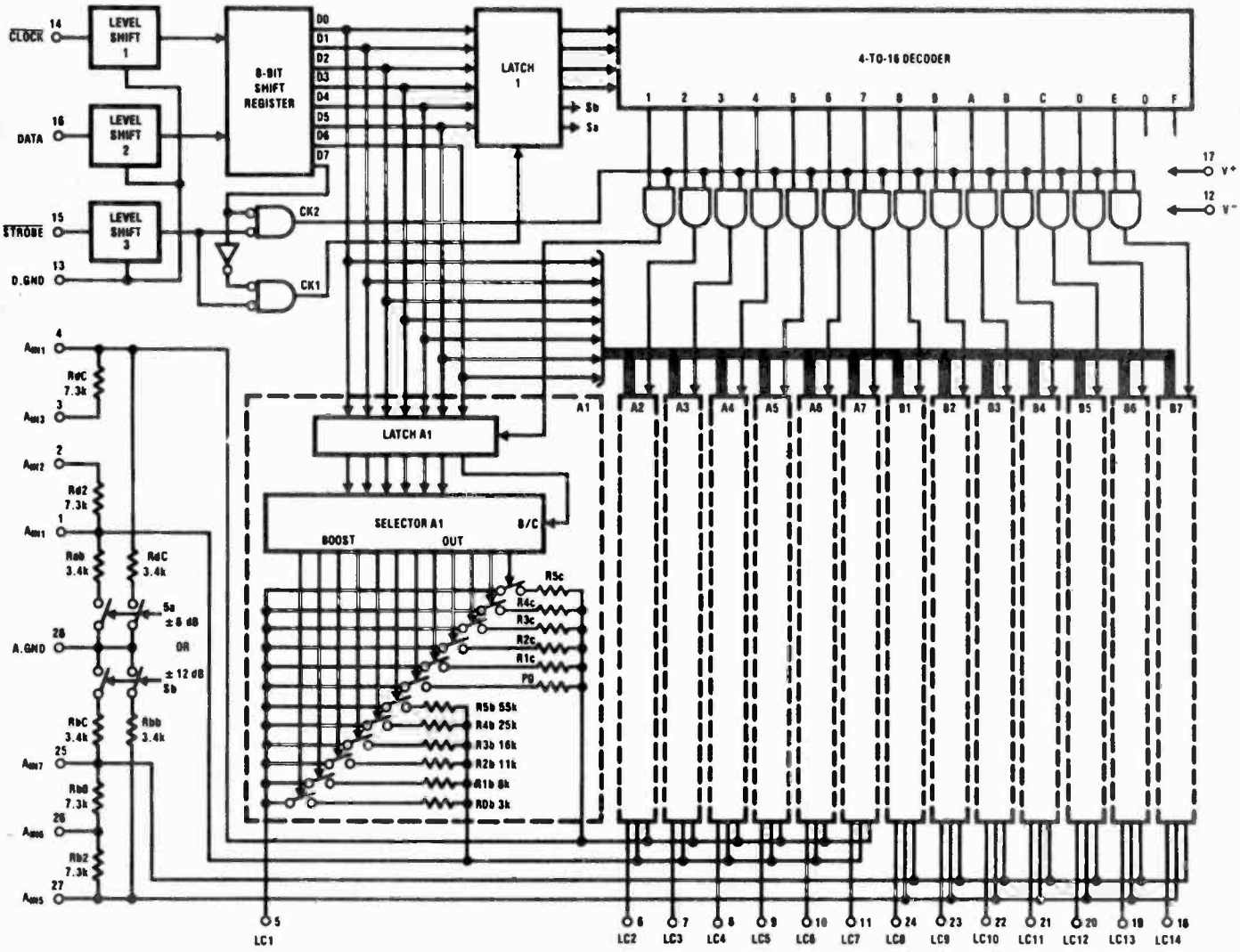
Connection Diagram

Dual-In-Line Package



Top View

Block Diagram



Absolute Maximum Ratings

Supply Voltage, $V_{DD} - V_{SS}$	18V
Allowable Input Voltage (Note 1)	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Storage Temperature, T_{stg}	−60°C to +150°C
Lead Temperature (Soldering, 10 sec), T_L	+300°C

Operating Ratings

Supply Voltage, $V_{DD} - V_{SS}$	5V to 16V
Digital Ground (Pin 13)	V_{SS} to V_{DD}
Digital Input (Pins 14, 15, 16)	V_{SS} to V_{DD}
Analog Input (Pins 1, 2, 3, 4, 25, 26, 27) (Note 1)	V_{SS} to V_{DD}
Operating Temperature, T_{ope}	−40°C to +85°C

Data supplied by National Semiconductor.

Electrical Characteristics (Note 2) $V_{DD} = 7.5V$, $V_{SS} = -7.5V$, A.GND = 0V

LOGIC SECTION

Symbol	Parameter	Test Conditions	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Unit (Limit)
I_{DDL}	Supply Current	Pins 14, 15, 16 are 0V	0.01	0.5	**0.5**	mA (Max)
I_{SSL}		Pins 14, 15, 16 are 0V	0.01	0.5	**0.5**	mA (Max)
I_{DDH}		Pins 14, 15, 16 are 5V	1.3	5	**5**	mA (Max)
I_{SSH}		Pins 14, 15, 16 are 5V	0.9	5	**5**	mA (Max)
V_{IH}	High-Level Input Voltage	@Pins 14, 15, 16	1.8	2.3	**2.5**	V (Min)
V_{IL}	Low-Level Input Voltage	@Pins 14, 15, 16	0.9	0.6	**0.4**	V (Max)
f_o	Clock Frequency	@Pin 14	2000	500	**500**	kHz (Max)
$t_{w(\overline{STB})}$	Width of $\overline{STB}$ Input	See *Figure 1*	0.25	1	1	μS (Min)
t_{setup}	Data Setup Time	See *Figure 1*	0.25	1	1	μS (Min)
t_{hold}	Data Hold Time	See *Figure 1*	0.25	1	1	μS (Min)
t_{cs}	Delay from Rising Edge of $\overline{CLOCK}$ to $\overline{STB}$	See *Figure 1*	0.25	1	1	μS (Min)
I_{IN}	Input Current	@Pins 14, 15, 16 $0V < V_{IN} < 5V$	±0.01	±1		μA (Max)
C_{IN}	Input Capacitance	@Pins 14, 15, 16 f = 1 MHz	5			pF

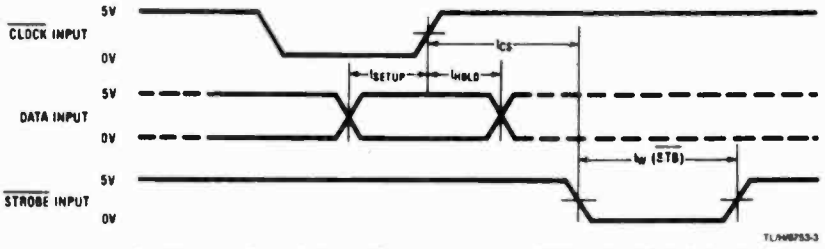
Note 1: Pins 2, 3 and 26 have a maximum input voltage range of ±22V for the typical application shown in *Figure 7*.

Note 2: Bold numbers apply at temperature extremes. All other numbers apply at $T_A = 25°C$, $V_{DD} = 7.5V$, $V_{SS} = -7.5V$, D.GND = A.GND = 0V as shown in the test circuit, *Figures 3* and *4*.

Note 3: Guaranteed and 100% production tested.

Note 4: Guaranteed (but not 100% production tested) over the operating temperature range. These limits are not used to calculate outgoing quality levels.

Timing Diagram



Note: To change the gain of the presently selected band, it is not necessary to send DATA 1 (Band Selection) each time.

FIGURE 1

Test Circuits

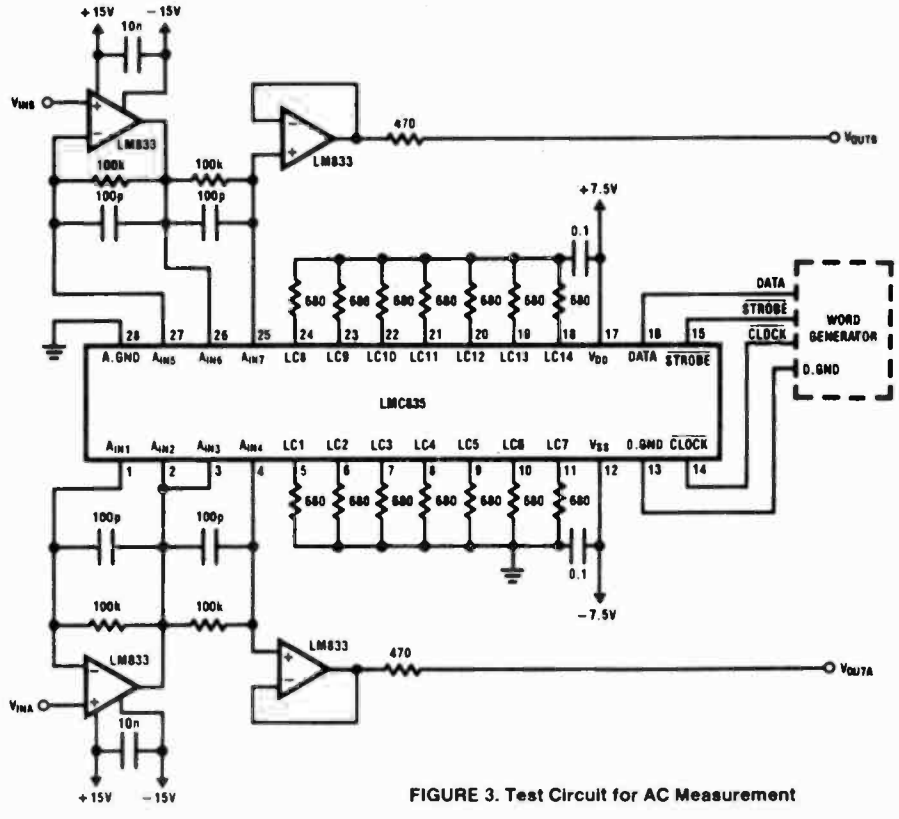


FIGURE 3. Test Circuit for AC Measurement

Electrical Characteristics (Note 2) $V_{DD} = 7.5V$, $V_{SS} = -7.5V$, D.GND = A.GND = 0V

SIGNAL PATH SECTION

Symbol	Parameter	Test Conditions	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Unit (Limit)
AA_V	Gain Error	$A_V = 0$ dB @ ± 12 dB Range	0.1	0.5	0.5	dB (Max)
		$A_V = 0$ dB @ ± 6 dB Range	0.1	1	1	dB (Max)
		$A_V = \pm 1$ dB @ ± dB Range (R_{b5} or R_{c5} is ON)	0.1	0.5	0.6	dB (Max)
		$A_V = \pm 2$ dB @ ± 12 dB Range (R_{b4} or R_{c4} is ON)	0.1	0.5	0.6	dB (Max)
		$A_V = \pm 3$ dB @ ± 12 dB Range (R_{b3} or R_{c3} is ON)	0.1	0.5	0.6	dB (Max)
		$A_V = \pm 4$ dB @ ± 12 dB Range (R_{b2} or R_{c2} is ON)	0.1	0.5	0.7	dB (Max)
		$A_V = \pm 5$ dB @ ± 12 dB Range (R_{b1} or R_{c1} is ON)	0.1	0.5	0.7	dB (Max)
		$A_V = \pm 9$ dB @ ± 12 dB Range (R_{b0} or R_{c0} is ON)	0.2	1	1.3	dB (Max)
THD	Total Harmonic	$A_V = 0$ dB @ ± 12 dB Range $V_{IN} = 4V_{rms}$, f = 1 kHz	0.0015			%
		$A_V = 12$ dB @ ± 12 dB Range				
		$V_{IN} = 1V_{rms}$, f = 1 kHz	0.01	0.1		% (Max)
		$V_{IN} = 1V_{rms}$, f = 20 kHz	0.1	0.5		% (Max)
		$A_V = -12$ dB @ ± 12 dB Range				
		$V_{IN} = 4V_{rms}$, f = 1 kHz	0.01	0.1		% (Max)
		$V_{IN} = 4V_{rms}$, f = 20 kHz	0.1	0.5		% (Max)
$V_{O\ Max}$	Maximum Output Voltage	$A_V = 0$ dB @ ± 12 dB Range THD < 1%, f = 1 kHz	5.5	5.1	5	V_{rms} (Min)
S/N	Signal to Noise	$A_V = 0$ dB @ ± 12 dB Range $V_{ref} = 1\ V_{rms}$	114			dB
		$A_V = 12$ dB @ ± 12 dB Range $V_{ref} = 1V_{rms}$	106			dB
		$A_V = -12$ dB @ ± 12 dB Range $V_{ref} = 1V_{rms}$	116			dB
I_{LEAK}	Leakage Current	$A_V = 0$ dB @ ± 12 dB Range (All internal switches are OFF)				
		Pin 2 + 3, Pin 26		500		nA (Max)
		Pin 5 ~ Pin 11, Pin 18 ~ Pin 24		50		nA (Max)

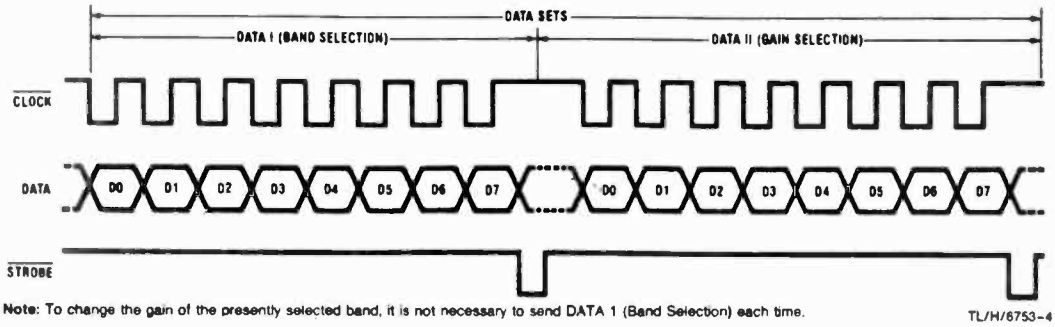
Note 1: Pins 2, 3 and 26 have a maximum input voltage range of ±22V for the typical application shown in *Figure 7*.

Note 2: Boldface numbers apply at temperature extremes. All other numbers apply at $T_A = 25°C$, $V_{DD} = 7.5V$, $V_{SS} = -7.5V$, D.GND = A.GND = 0V as shown in the test circuit, *Figures 3* and *4*.

Note 3: Guaranteed and 100% production tested.

Note 4: Guaranteed (but not 100% production tested) over the operating temperature range. These limits are not used to calculate outgoing quality levels.

Timing Diagrams



Note: To change the gain of the presently selected band, it is not necessary to send DATA 1 (Band Selection) each time.

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FIGURE 2

Test Circuits (Continued)

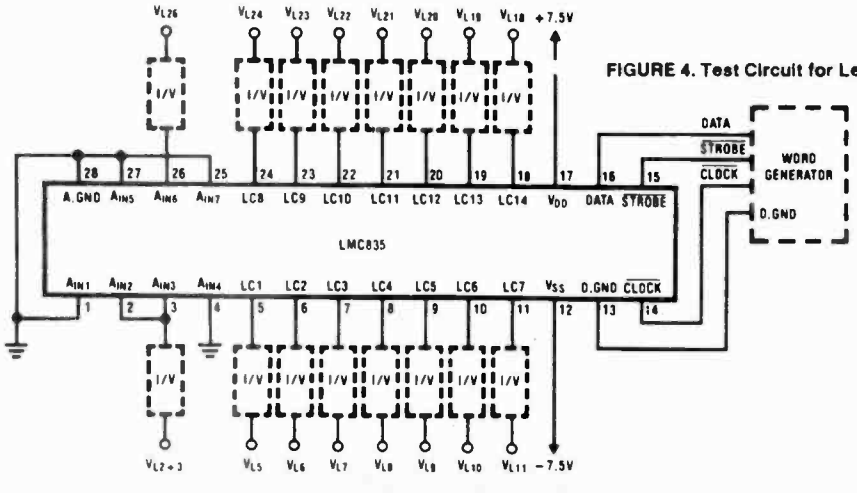


FIGURE 4. Test Circuit for Leakage Current Measurement

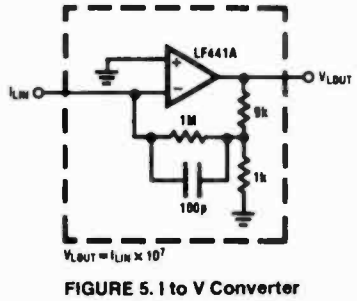


FIGURE 5. I to V Converter

Truth Tables

DATA I (Band Selection)

D7	D6	D5	D4	D3	D2	D1	D0	
H	X	L	L	L	L	L	L	(Ch A: Band 1 ~ 7, Ch B: Band 8 ~ 14)
H	X	L	L	L	L	L	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, No Band Selection
H	X	L	L	L	L	H	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 1
H	X	L	L	L	L	H	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 2
H	X	L	L	L	H	L	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 3
H	X	L	L	L	H	L	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 4
H	X	L	L	L	H	H	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 5
H	X	L	L	L	H	H	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 6
H	X	L	L	H	L	L	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 7
H	X	L	L	H	L	L	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 8
H	X	L	L	H	L	H	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 9
H	X	L	L	H	L	H	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 10
H	X	L	L	H	H	L	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 11
H	X	L	L	H	H	L	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 12
H	X	L	L	H	H	H	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 13
H	X	L	L	H	H	H	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 14
H	X	L	H	Valid Binary Input				Ch A ± 12 dB Range, Ch B ± 12 dB Range, No Band Selection
H	X	H	L	Valid Binary Input				Ch A ± 12 dB Range, Ch B ± 6 dB Range, Band 1 ~ 14
H	X	H	H	Valid Binary Input				Ch A ± 6 dB Range, Ch B ± 12 dB Range, Band 1 ~ 14
↑ ①	↑ ②	↑ ③	↑ ④	← Band Code →				Ch A ± 6 dB Range, Ch B ± 6 dB Range, Band 1 ~ 14

① DATA 1
② Don't Care
③ Ch A ±6 dB/±12 dB Range
④ Ch B ±6 dB/±12 dB Range

This is the gain if the ±12 dB range is selected by DATA I. If the ±6 dB range is selected, then the values shown must be approximately halved. See the characteristics curves for more exact data.

⑤ DATA II
⑥ Boost/Cut

DATA II (Gain Selection)

	D7	D6	D5	D4	D3	D2	D1	D0
Flat	L	X	L	L	L	L	L	L
1 dB Boost	L	H	H	L	L	L	L	L
2 dB Boost	L	H	L	H	L	L	L	L
3 dB Boost	L	H	L	L	H	L	L	L
4 dB Boost	L	H	L	L	L	H	L	L
5 dB Boost	L	H	L	L	L	L	H	L
6 dB Boost	L	H	L	H	L	L	H	L
7 dB Boost	L	H	H	L	H	L	H	L
8 dB Boost	L	H	L	H	L	H	H	L
9 dB Boost	L	H	L	L	L	L	L	H
10 dB Boost	L	H	H	L	H	L	L	H
11 dB Boost	L	H	H	L	H	H	L	H
12 dB Boost	L	H	H	L	H	H	H	H
1 dB ~ 12 dB Cut	L	L	Valid Above Input					
	↑ ⑤	↑ ⑥	← Gain Code →					

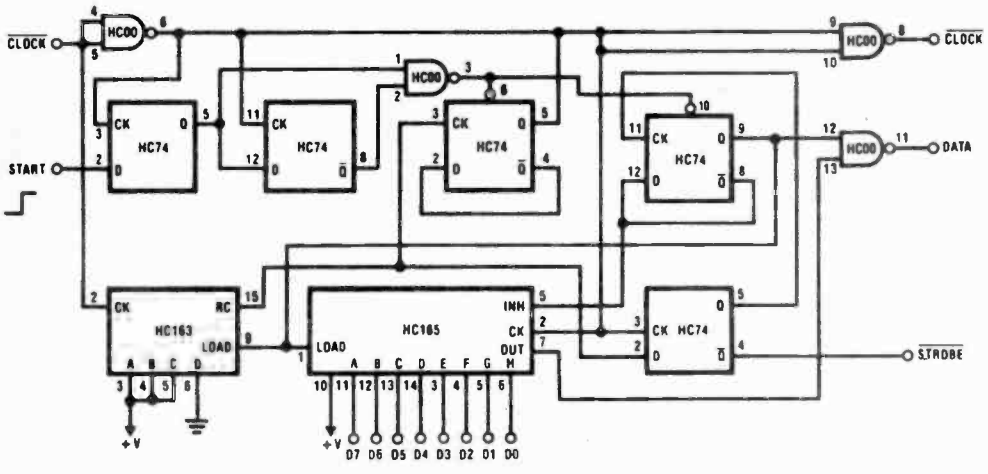
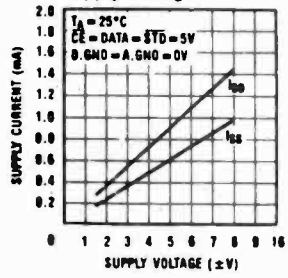


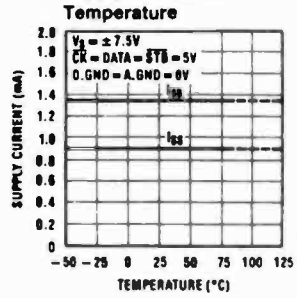
FIGURE 6. Simple Word Generator

Typical Performance Characteristics

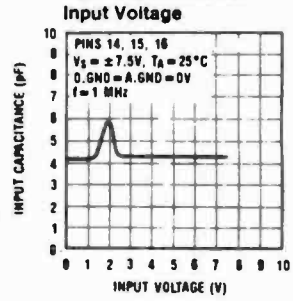
Supply Current vs Supply Voltage



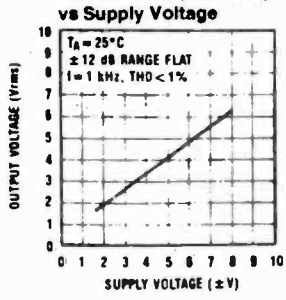
Supply Current vs Temperature



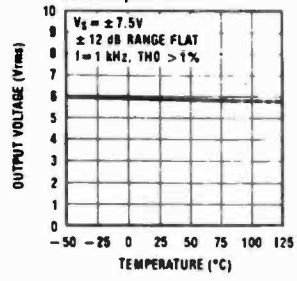
Input Capacitance vs Input Voltage



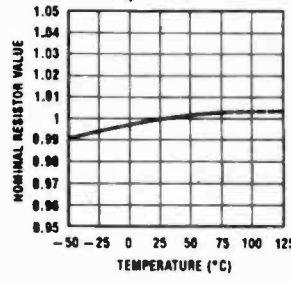
Maximum Output Voltage vs Supply Voltage



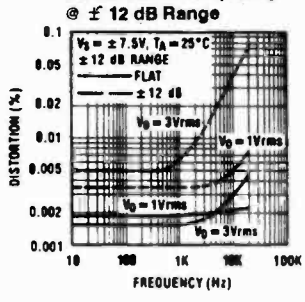
Maximum Output Voltage vs Temperature



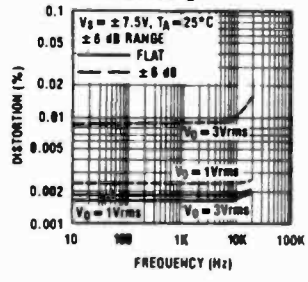
Nominal Resistor vs Temperature



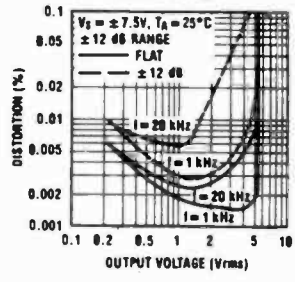
Distortion vs Frequency @ ±12 dB Range



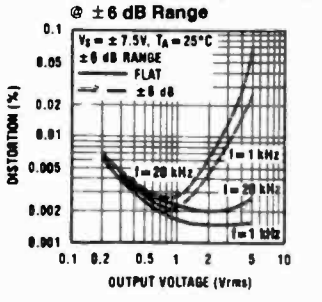
Distortion vs Frequency @ ±6 dB Range



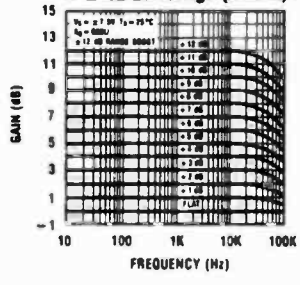
Distortion vs Output Voltage @ ± 12 dB Range



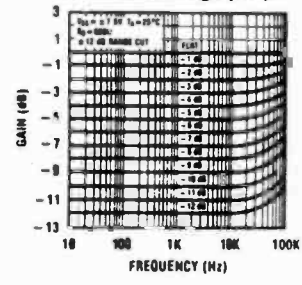
Distortion vs Output Voltage @ ±6 dB Range



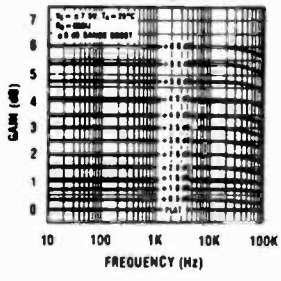
Gain vs Frequency @ ± 12 dB Range (Boost)



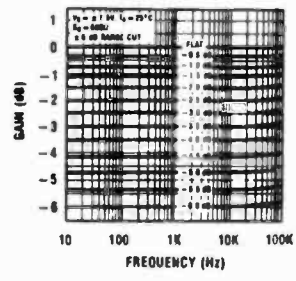
Gain vs Frequency @ ± 12 dB Range (Cut)



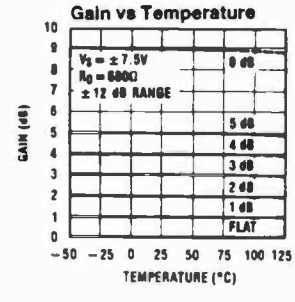
Gain vs Frequency @ ±6 dB Range (Boost)



Gain vs Frequency @ ±6 dB Range (Cut)



Gain vs Temperature



Typical Applications

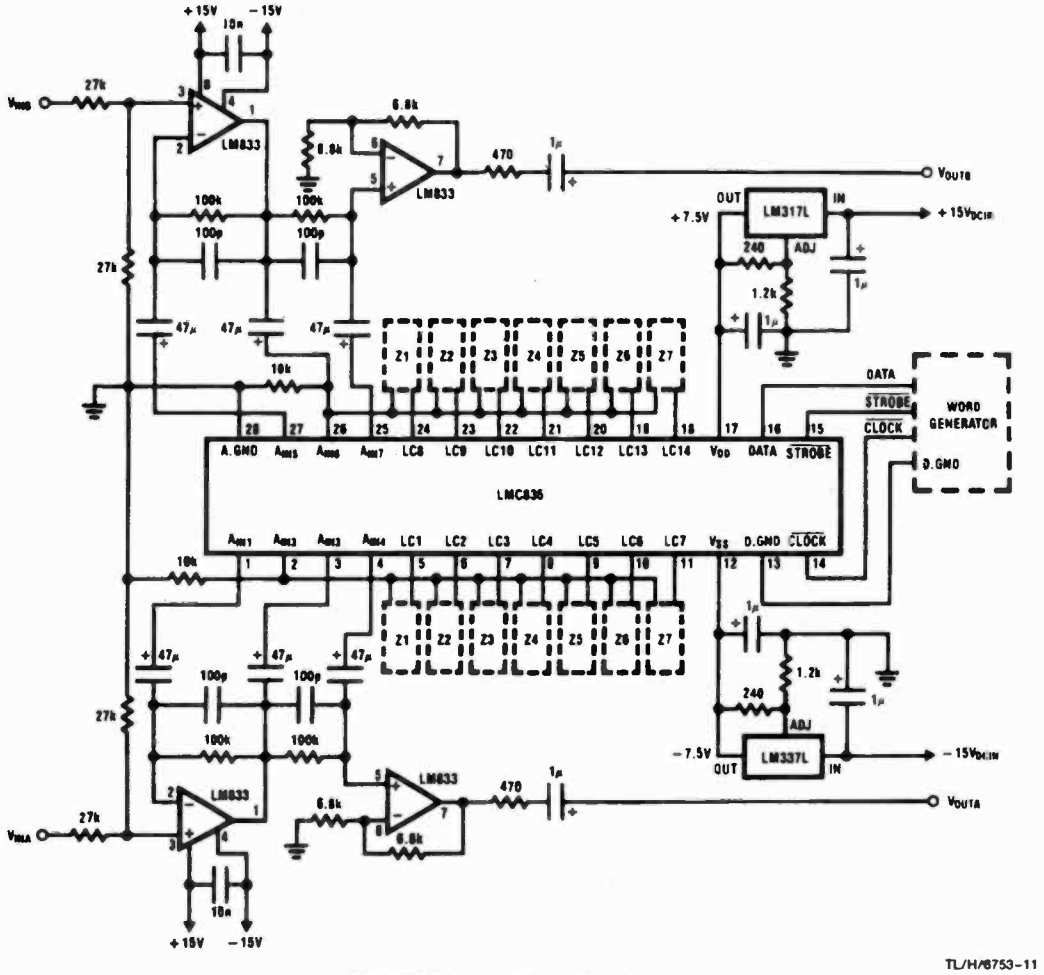


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FIGURE 7. Stereo 7-Band Equalizer

TABLE I: Tuned Circuit Elements

$Q_0 = 3.5, Q_{12dB} = 1.05$					
Z1	f_0 (Hz)	C_O (F)	C_L (F)	R_L (Ω)	R_O (Ω)
Z1	63	1μ	0.1μ	100k	680
Z2	160	0.47μ	0.033μ	100k	680
Z3	400	0.15μ	0.015μ	100k	680
Z4	1k	0.068μ	0.0068μ	82k	680
Z5	2.5k	0.022μ	0.0033μ	82k	680
Z6	6.3k	0.01μ	0.0015μ	62k	680
Z7	16k	0.0047μ	680p	47k	680

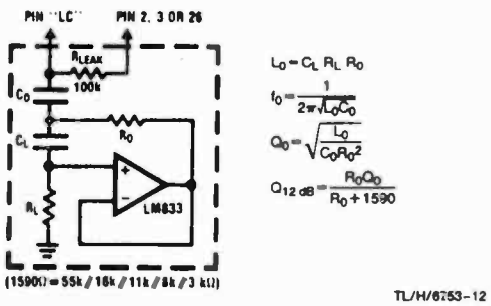

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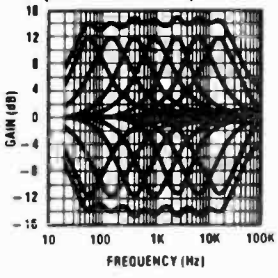
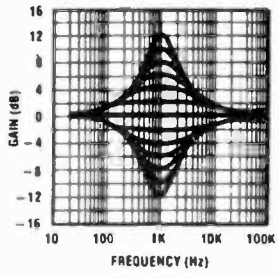
FIGURE 8. Tuned Circuit for Stereo 7-Band Equalizer (*Figure 7*)

Performance Characteristics (Circuit of *Figure 7*)

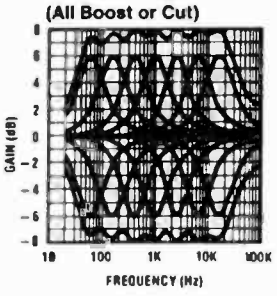
LM835 Gain vs Frequency @ ± 12 dB Range (All Boost or Cut)



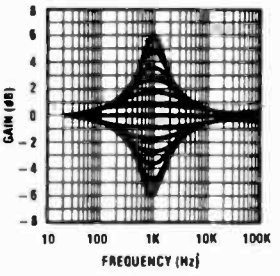
LM835 Gain vs Frequency @ ± 12 dB Range (1 kHz Boost or Cut)



LM835 Gain vs Frequency @ ±6 dB Range (All Boost or Cut)



LM835 Gain vs Frequency @ ±6 dB Range (1 kHz Boost or Cut)



Typical Applications (Continued)

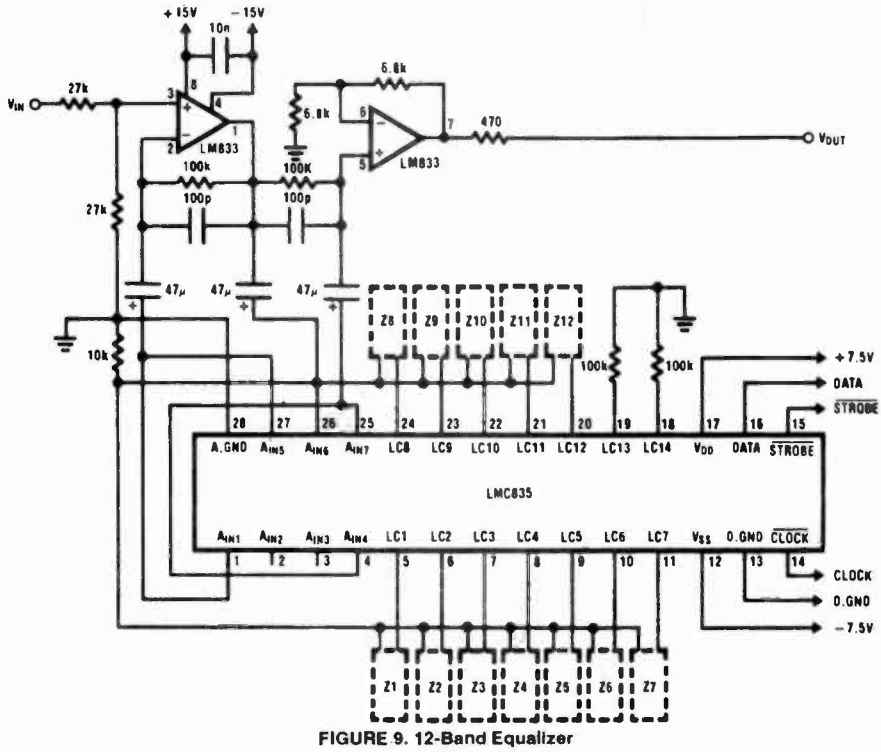
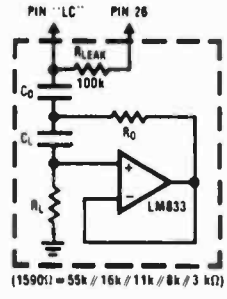


FIGURE 9. 12-Band Equalizer



$$L_O = C_L R_L R_O$$

$$f_0 = \frac{1}{2\pi\sqrt{L_O C_O}}$$

$$Q_O = \sqrt{\frac{L_O}{C_O R_O^2}}$$

$$Q_{12\,dB} = \frac{R_O Q_O}{R_O + 1590}$$

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FIGURE 10. Tuned Circuit for 12-Band Equalizer (*Figure 9*)

Performance Characteristics (Circuit of Figure 9)

12 Band Equalizer Application
LM835 Gain vs Frequency
@ ±6 dB Range
(All Boost or Cut)

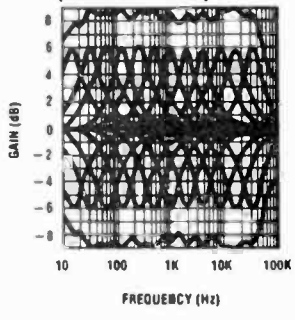
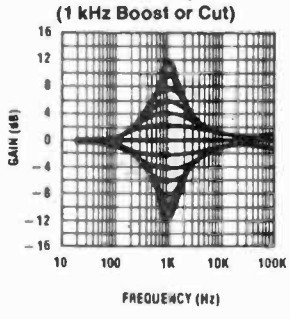


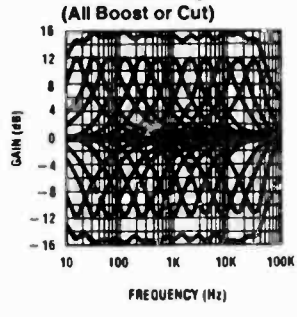
TABLE II. Tuned Circuit Elements

	$Q_O = 4.7$, $Q_{12\,dB} = 1.4$				
	f_o (Hz)	C_O (F)	C_L (F)	R_L (Ω)	R_O (Ω)
Z1	16	3.3µ	0.47µ	100k	680
Z2	31.5	15µ	0.22µ	110k	680
Z3	63	1µ	0.1µ	100k	680
Z4	125	0.39µ	0.068µ	91k	680
Z5	250	0.22µ	0.033µ	82k	680
Z6	500	0.1µ	0.015µ	100k	680
Z7	1k	0.047µ	0.01µ	82k	680
Z8	2k	0.022µ	0.0047µ	91k	680
Z9	4k	0.01µ	0.0022µ	110k	680
Z10	8k	0.0068µ	0.001µ	82k	680
Z11	16k	0.0033µ	680p	62k	680
Z12	32k	0.0015µ	470p	68k	510

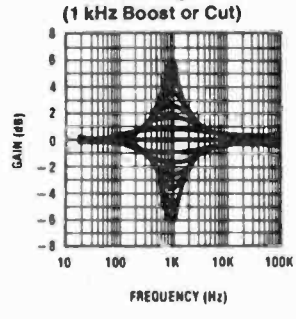
LM835 12 Band E.Q. Application
Gain vs Frequency
@ ±12 dB Range
(1 kHz Boost or Cut)



12 Band Equalizer Application
LM835 Gain vs Frequency
@ ± 12 dB Range
(All Boost or Cut)



LM835 12 Band E.Q. Application
Gain vs Frequency
@ ±6dB Range
(1 kHz Boost or Cut)



Typical Applications (Continued)

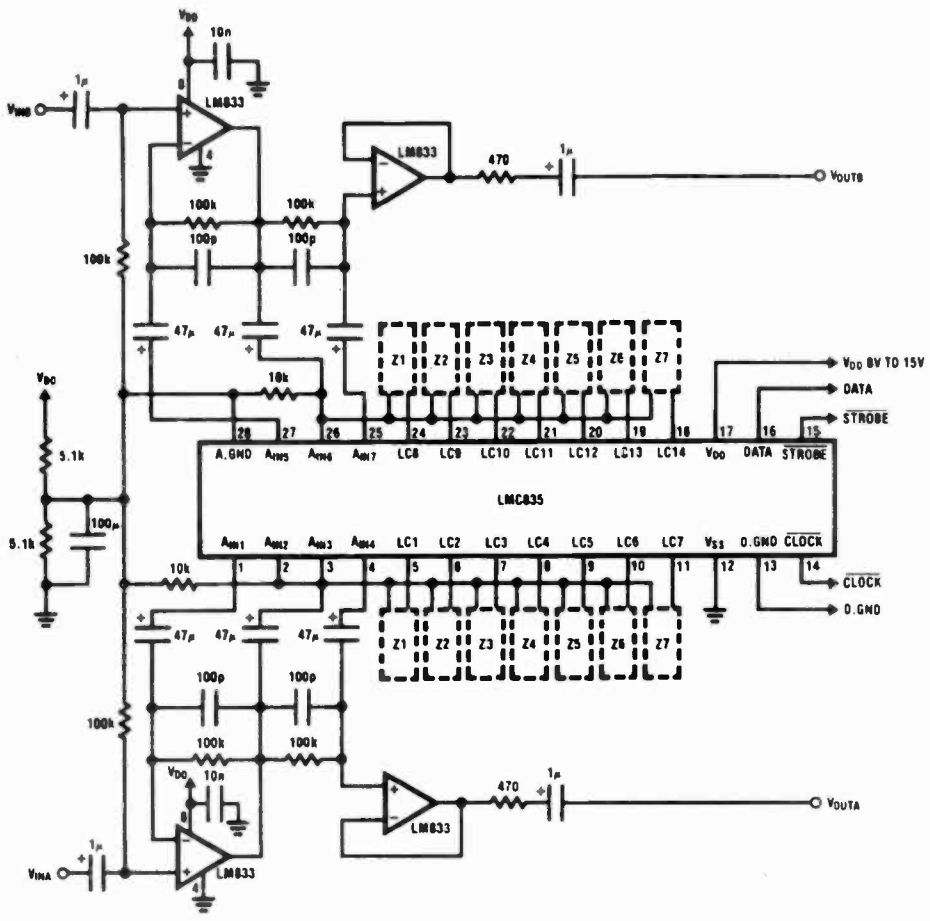


FIGURE 11. Single Supply Stereo Equalizer

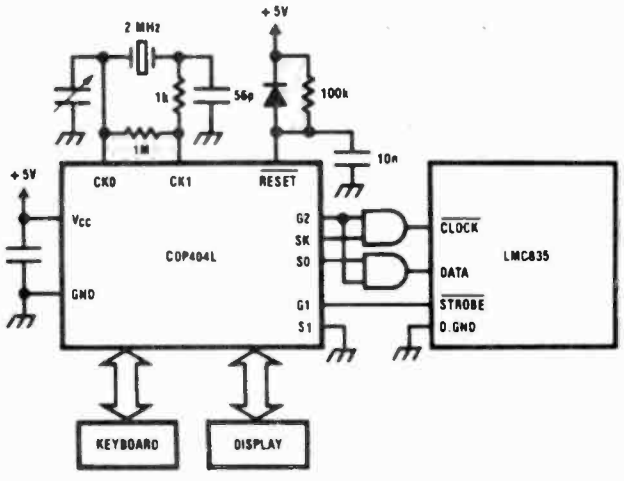


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FIGURE 14. LMC835-COP404L CPU Interface

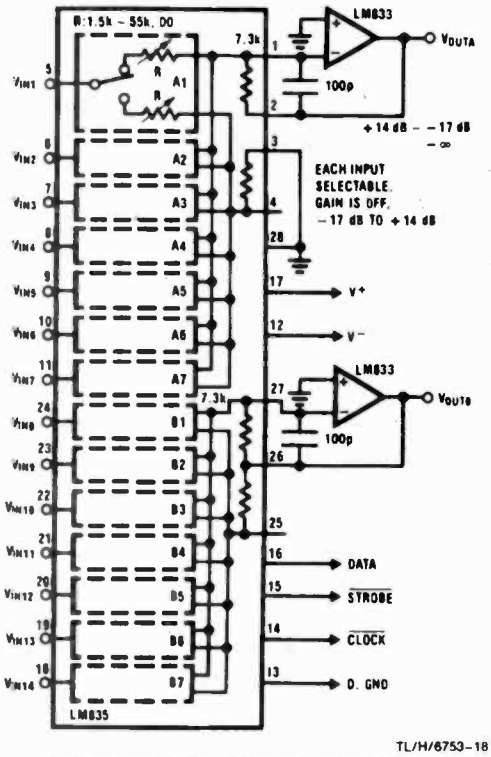

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FIGURE 12. Stereo 7-Input/1-Output Mixers (THD is not as low as equalizer circuit)

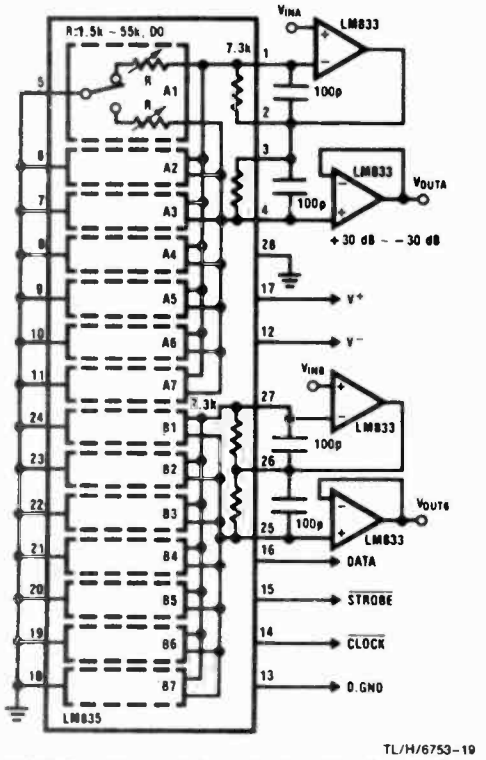

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FIGURE 13. Stereo Volume Control, Very Low THD

Application Hints

SWITCHING NOISE

The LMC835 uses CMOS analog switches that have small leakages (less than 50 nA). When a band is selected for flat gain, all the switches in that band are open and the resonator circuit is not connected to the LMC835 resistor network. It is only in the flat mode that the small leakage currents can cause problems. The input to the resonator circuit is usually a capacitor and the leakage currents will slowly charge up this capacitor to a large voltage if there is no resistive path to limit it. When the band is set to any value other than flat, the charge on the capacitor will be discharged by the resistor network and there will be a transient at the output. To limit the size of this transient, R_{LEAK} is necessary.

HOW TO AVOID SWITCHING NOISE DUE TO LEAKAGE CURRENT (Refer to *Figures 7* and *8*)

To avoid switching noise due to leakage currents when changing the gain, it is recommended to put R_{LEAK} = 100 KΩ between Pin 3 and Pin 5—11 each, Pin 26 and Pin 12—24 each. The resistor limits the voltage that the capacitor can charge to, with minimal effects on the equalization. The frequency response change due to R_{LEAK} are shown in *Figure 15*. The gain error is only 0.2 dB and Q error is only 5% at 12 dB boost or cut.

Typical Applications (Continued)

Sample Subroutine Program for *Figure 14*, LMC835-COP404L CPU Interface

```
HEX
CODE    LABEL      MNEMONICS          COMMENTS
3F      LMC835:    LBI     3F     ;POINT TO RAMADDRESS 3F
05      SEND       LD             ;RAMDATA TO A
22                 SC             ; SET CARRY
335F               OGI            ;SET PORT G= 1111, OPEN THE AND GATES
4F                 XAS            ;SWAP A AND SIO, CLOCK START
05                 LD             ;RAMDATA TO A, MAKE SURE A = DATA
07                 XDS            ;SWAP A AND RAMDATA, RAMADDRESS=RAMADDRESS-1
05                 LD             ;RAMDATA TO A
4F                 XAS            ;SWAP A AND SIO
05                 LD             ;RAMDATA TO A, MAKE SURE A=NEWDATA
07                 XDS            ;SWAP A AND RAMDATA, RAMADDRESS=RAMADDRESS-1
32                 RC             ;RESET CARRY
4F                 XAS            ;SWAP A AND SIO, CLOCK STOP
335D               OGJ     13     ;SET PORT G=1101, MAKE STROBE LOW
335B               OGI     11     ;SET PORT G=1011, MAKE STROBE HIGH, CLOSE THE
                                                                     GATES
4E                 CBA            ;BD TO A
43                 AISC    3      ;RAMADDRESS<3C THEN RETURN
48                 RET
80                 JP      SEND

        RAM
      ADDRESS          COMMENTS
3C      DATA     ;GAIN DATA D4–D7
3D      DATA     ;GAIN DATA D0–D3
3E      DATA     ;BAND DATA D4–D7
3F      DATA     ;BAND DATA D0–D3
```

Application Hints (Continued)

REDUCING EXTERNAL COMPONENTS

The typical application shown in *Figure 7* is switching noise free. The DC-coupled circuit in *Figure 16* is also switching noise free, except at 12 dB/6 dB switch turn ON/OFF. This switching noise is caused by the I_{bias} and V_{offset} of the op amps. Selecting a low I_{bias} and V_{offset} op amp can minimize the switching noise due to the 12 dB/6 dB switch. The DC-coupled application can also eliminate the R_F = 100k resistors with only a 0.5 dB gain error at 12 dB boost or cut.

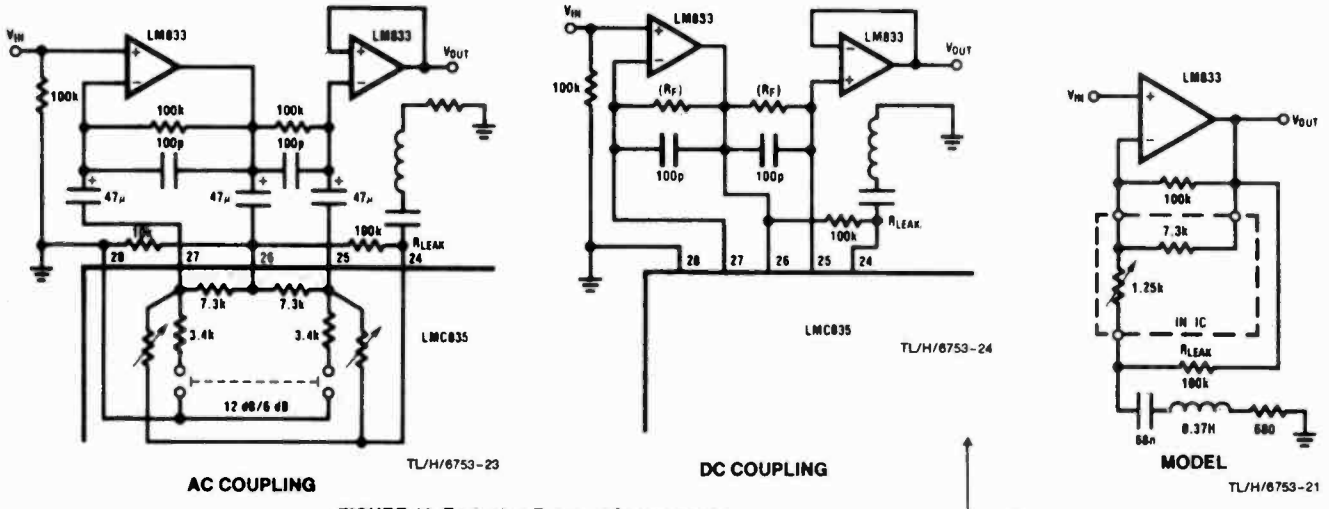


FIGURE 16. Reducing External Components

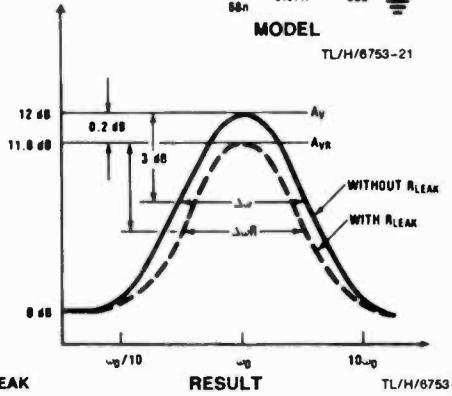


FIGURE 15. Effect of R_{LEAK}

1200/300 bps Full duplex Modem

Description

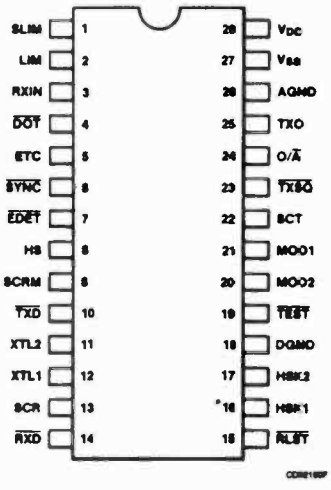
The μA212A and the μA212AT 1200 bps modem circuits are fabricated in Fairchild's advanced Double-Poly Silicon-Gate CMOS process. Either monolithic chip performs all signal processing functions required for a Bell 212A/103 compatible modem. Dialing, handshaking protocols, and mode control functions can be provided by a general purpose single-chip μC. The μA212A or μA212AT and μC; along with several components to handle the control and telephone line interfaces, provide a high performance, cost-effective solution for an intelligent Bell 212A-compatible modem design.

Either modem chip performs the modulation, demodulation, filtering and certain control and self-test functions required for a Bell 212A-compatible modem, as well as additional functional enhancements. Switched capacitor filters provide channel isolation, spectral shaping and fixed compromise equalization for both high and low speed modes.

A novel switched-capacitor modulator and a digital coherent demodulator provide 1200 bps QPSK operation while a separate digital FSK modulator and demodulator handle the 0-300 bps requirement. The μA212AT includes an integral DTMF tone generator on-chip. The μA212A without DTMF generator, is cost optimal for answer-only applications or if an external dialer is present. The μA212A and μA212AT are otherwise pin and firmware compatible. Existing μA212A applications can be easily upgraded to the μA212AT with minor software changes *(see technical bulletin M-1 appended.)* The receive filter and energy detector may be configured for call progress tone detection (dial-tone, busy, ringback, voice), providing the front end for a smart dialer on either the μA212A or μA212AT.

- **Functions as 212A and 103 Compatible Modem**
- **Performs all Signal Processing Functions**
- **Interfaces to Single Chip μC Which Handles Handshaking Protocols and Mode Control Functions**
- **DTMF Tone Generation (μA212AT)**
- **μA212A is Pin and Firmware Compatible with the μA212AT for Easy Upgrade**
- **Call Progress Tone Detection for Smart Dialer Applications**
- **On Chip Oscillator Uses Standard 3.6864 MHz Crystal**
- **Few External Components Required**
- **Industrial Temperature Range Option (−40°C to +85°C)**
- **Operates from +5 and −5 Volt Supplies**
- **Low Operating Power: 35 mW Typical**
- **28-Lead Ceramic DIP, 28-Lead Plastic DIP, and 28-Lead Surface Mount Packages**
- **A μA212A Designer's Kit is Available**

Connection Diagram
28-Lead Dip
(Top View)



Order Information

Type	Temperature Range	Code	Package
μA212ATDC	0 to +70°C	FM	28-Lead Ceramic DIP
μA212ATDV	−40°C to +85°C	FM	28-Lead Ceramic DIP
μA212ATPC	0 to +70°C	*	28-Lead Molded DIP
μA212ATQC	0 to +70°C	*	28-Lead Molded Surface Mount
μA212ADC	0 to +70°C	FM	28-Lead Ceramic DIP
μA212ADV	−40°C to +85°C	FM	28-Lead Ceramic DIP
μA212APC	0 to +70°C	*	28-Lead Molded DIP

*Consult Factory

Absolute Maximum Ratings

V_{DD} to DGND or AGND	7.0 V
V_{SS} to DGND or AGND	−7.0 V
Voltage at any Input	V_{DD} + 0.3 to V_{SS} −0.3 V
Voltage at any Digital Output	V_{DD} + 0.3 V to DGND −0.3 V
Voltage at any Analog Output	V_{DD} + 0.3 V to V_{SS} −0.3 V
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−85°C to +150°C
Lead Temperature (soldering, 10 s)	300°C

Pin No.	Pin Description	
28	V_{DD}	Positive power supply V_{DD} = +5 V
26	AGND	Analog Ground
18	DGND	Digital Ground
27	V_{SS}	Negative power supply V_{SS} = −5 V
3	RXIN	Line signal to modem. From active or passive Hybrid output.
25	TXO	Line signal from modem. To active or passive Hybrid input.
24	O/Ā	Orig/answer Mode Select. Assigns channels to XMTRS/RCVRS. 1 = Originate mode, 0 = Answer mode. (Note)
23	TXSQ	Squelch XMTRS in date mode. 0 = Both XMTRS off; 1 = turns on XMTR selected by HS pin. μA212AT: In dialer mode, 0 = DTMF generator OFF/call progress detection. 1 = DTMF generator ON. μA212A: In dialer mode call progress detection only. TXSQ must be set to 0.
9	SCRM	Scrambler. "0" disables scrambler and descrambler for testing purposes.
12	XTL1	Frequency control. 3.6864 MHz
11	XTL2	XTAL oscillator, operating parallel mode. Provides timing, sample clocks and L.O.'s.
8	HS	Selects modem speed. 1 selects 1200 bps. 0 selects 300 bps. (Note)
6	SYNC	Selects CHAR ASYNC or BIT SYNC mode. 1 = ASYNC mode: enables XMIT & RCV buffers, sets character length according to MOD1, MOD2 pins. 0 = SYNC mode: disables buffers, selects TX clock source according to MOD1, MOD2 pins. Active only if HS = 1.
21	MOD1	Selects character length (ASYNC) or

Note
For μA212AT in dialer mode, O/Ā, HS, MOD1 and MOD2 select the DTMF to be generated (see *Table 2*).

Pin No.	Pin Description	
20	MOD2	TX clock (SYNC). In ASYNC mode, selects 8, 9, 10 or 11 bit character length; in SYNC mode, selects internal, external or recovered RCV clock as XMTR data clock source. Active only if HS = 1. (See *Table 1*) (Note)
10	$\overline{TXD}$	XMIT Data. Serial data from host. Disconnected when in digital loop.
14	$\overline{RXD}$	RCVD Data. Serial data to host, internally clamped to mark (= 1) when modem is in digital loop or $\overline{EDET}$ is inactive (= 1).
22	SCT	Serial Clock Transmit. 1200 Hz clock providing XMTR timing in SYNC mode. SCT source (INT., EXT., SLAVE) selected by MOD1, MOD2 pins. $\overline{TXD}$ changes on negative edge, sampled on positive edge. Internal clock provided in ASYNC mode.
5	ETC	External Transmit Clock. 1200 Hz external clock providing XMTR timing in SYNC mode, selected by MOD1, MOD2 pins. $\overline{TXD}$ changes on negative edge, sampled on positive edge. Provided on SCT pin if selected.
13	SCR	Serial Clock Receive. In SYNC mode, 1200 Hz bit clock recovered from RCVD signal. May be pin-selected (MOD1, MOD2) as local transmit clock (SLAVE mode); provided on SCT pin if selected. $\overline{RXD}$ changes on negative edge, sampled on positive edge. Undefined in ASYNC mode.
7	$\overline{EDET}$	Energy Detect. In data mode, $\overline{EDET}$ = 0 if valid signal above threshold is present for 155 ± 50 ms, $\overline{EDET}$ = 1 if signal below threshold for ' > 17 ± 7 ms. In dialer mode, follows on/off variations of call-progress tones, when $\overline{TXSQ}$ = 0
15	$\overline{RLST}$	Remote Loop Status, used in RDL mode. Responding modem: sets $\overline{RLST}$ = 0 upon receipt of unscrambled mark for 154 – 231 ms. initiating modem: asserts $\overline{RLST}$ = 0 upon receipt of scrambled mark for 231 – 308 ms. (See *Table 3*).
1	SLIM	Soft Limiter Output. Connect external 0.033 μF capacitor here.
2	LIM	Comparator input. Connected external 0.033 μF capacitor here.
4	$\overline{DOT}$	If HS = 1, forces a 1200 bps dotting pattern on the transmit path, for use when programming the 212AT high speed self-test mode. Both RCV and XMIT paths are in $\overline{SYNC}$ mode during dotting transmission, overriding the setting of $\overline{SYNC}$, and of HSK1, HSK2. If HS = 0, $\overline{DOT}$ forces a 155 bps dotting pattern for use in lowspeed self-test mode. 1 = Normal Path, 0 = Dotting.
19 16 17	$\overline{TEST}$ HSK1, HSK2	When the $\overline{TEST}$ pin is inactive (high), HSK1 and HSK2 select one of four transmit conditions, for use when programming the Handshake sequences. (*See Table 1*). When $\overline{TEST}$ is active (low), the HSK1 and HSK2 pins select one of three test conditions, or, alternatively, the dialer mode used for call progress tone detection and DTMF tone generation, μA212AT only.

Functional Description*

Refer to Figure 1.

Transmitter

The transmitter consists of high-speed and low-speed modulators, a transmit buffer and scrambler, and a transmit filter and line driver. In high-speed asynchronous mode, transmit data from the Data Terminal Equipment enters the transmit buffer, which synchronizes the data to the internal 1200 bps clock. Data which is underspeed relative to 1200 bps periodically has the last stop bit sampled twice resulting in an added stop bit. Similarly, overspeed input data periodically has unsampled — and therefore deleted — stop bits. The MOD1 and MOD2 pins choose 8, 9, 10 or 11 bit character lengths. In synchronous mode the transmit buffer is disabled. The transmitter clock source may be chosen by MOD1 and MOD2 internal, external or derived from the recovered received data. A scrambler preceeds encoding to ensure that the line spectrum is sufficiently distributed to avoid interference with the in-band supervisory single-frequency signaling system employed in most Bell System toll trunks. The randomized spectrum also facilitates timing recovery in the receiver. The scrambler is characterized by the following recursive equation:

$$Y_i = X_i \oplus Y_{i-14} \oplus Y_{i-17}$$

where X_i is the scrambler input bit at time i. Y_i is the scrambler output bit at time i and $\oplus$ denotes the XOR operation.

212A-type modems achieve full-duplex 1200 bps operation by encoding transmitted data by bit-pairs (dibits), thereby halving the apparent data rate. The resultant reduced spectral width allows both frequency channels to coexist in a limited bandwidth telephone channel with practical levels of filtering. The four unique dibits thus obtained are gray-coded and differentially phase modulated onto a carrier at either 1200 Hz (originate mode) or 2400 Hz (answer mode). Each dibit is encoded as a phase change relative to the phase of the preceding signal dibit element:

Dibit	Phase Shift (deg)
00	+90
01	0
11	−90
10	180

At the receiver, the dibits are decoded and the bits are reassembled in the correct sequence. The left-hand digit of the dibit is the one occurring first in the data stream as it enters the modulator after the scrambler. The lowspeed transmitter generates phase-coherent FSK using one of two programmable tone generators. Answer mode mark (2225 Hz) is also utilized as answer tone in both low and high speed operation.

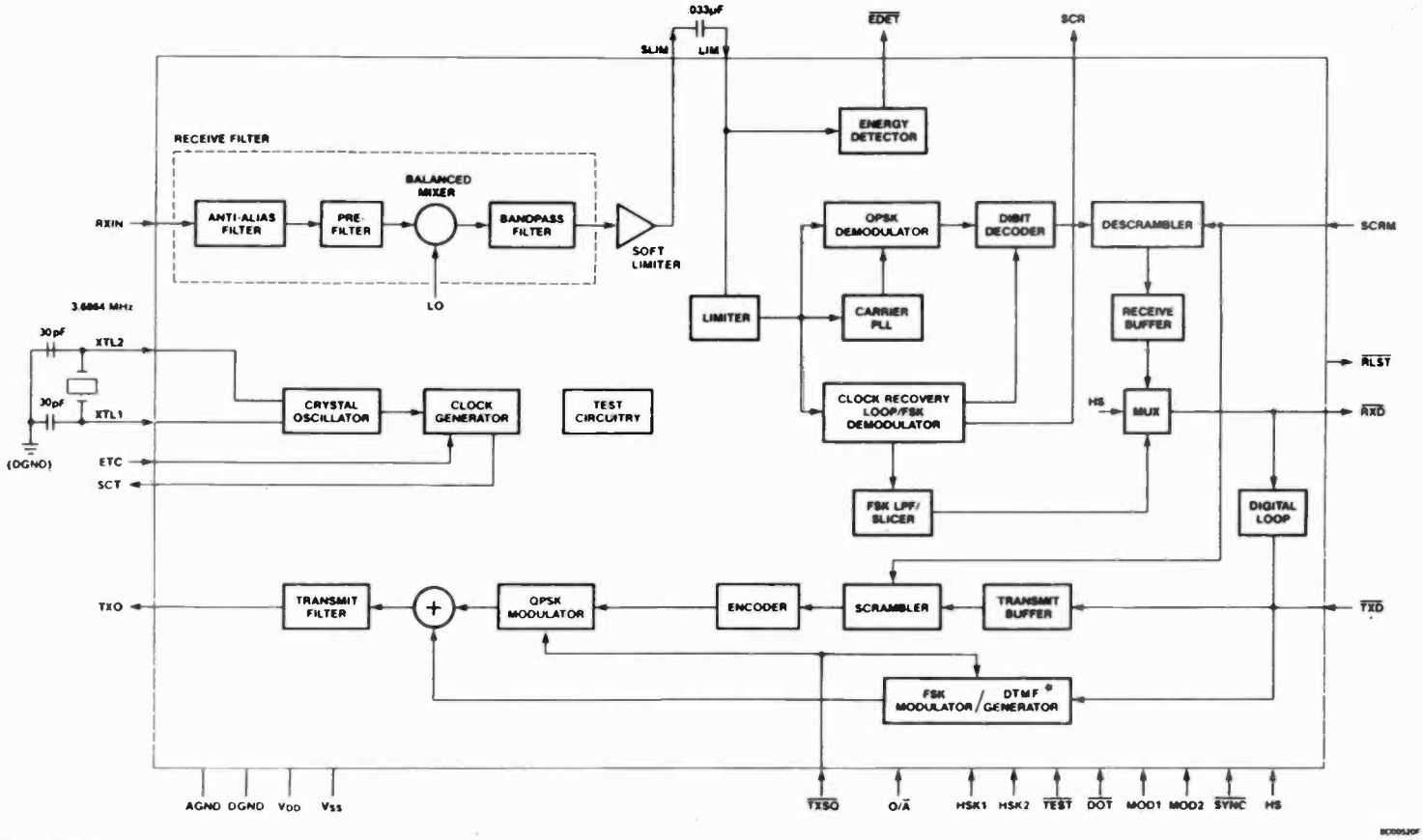
In Dialer mode, both tone generators are employed to generate DTMF tone pairs. The summed modulator outputs drive a lowpass filter which serves as a fixed compromise amplitude and delay equalizer for the phone line and reduces output harmonic energy well below maximum specified levels. The filter output drives an output buffer amplifier with low output impedance. The buffer provides 700 mVrms in data mode, for a nominal −9 dBm level at the line, assuming 2 dB loss in the data access arrangement.

DTMF Tone Generation

The μA212AT includes on-chip DTMF generation, using two programmable tone generators. Dialer mode must be selected on $\overline{TEST}$, HSK1 and HSK2 for DTMF dialing. The O/$\overline{A}$, HS, MOD1 and MOD2 pins are used to select the required digit according to the encoding scheme shown in *Table 2*, and the tones are turned on and off by the logic level on $\overline{TXSQ}$. The generated tones meet the applicable CCITT and EIA requirement for tone dialing. DTMF output levels are 1.0 Vrms (low group) and 1.25 Vrms (high group).

*For additional information contact sales office for Applications Note ASP-1 "Theory of Operation — μA212A" and Technical Bulletins M1, M3 & M4.

Figure 1 Block Diagram



*μA212AT only

Receiver

The received signal from the line-connection circuitry passes through a lowpass filter which performs anti-aliasing and compromise amplitude and delay equalization of the incoming signal. Depending upon mode selection (originate/answer) the following mixer either passes or down converts the signal to the 1200 Hz bandpass filter. In analog loopback mode, the receiver originate and answer mode assignments are inverted, which forces the receiver to operate in the transmitter frequency band. The 1200 Hz bandpass filter passes the desired received signal while attenuating the adjacent transmitted signal component reflected from the line (talker echo). The chosen passband shape converts the spectrum of the received high-speed signal to 100% raised cosine to minimize intersymbol interference in the recovered data. Following the filter is a soft limiter and a signal energy detector. An external capacitor is used to eliminate offset between the soft limiter output and the following limiter.

The energy detector provides a digital indication that energy is present within the filter passband at a level above a preset threshold. Approximately 3 dB of hysteresis is provided between on and off levels to stabilize the detector output. In dialer mode, the detector output is used to provide logic level indication of the presence of call progress tones.

The limiter output drives the QPSK demodulator and the carrier and clock recovery phase-locked loops. The low speed FSK demodulator shares part of the clock recovery loop. The QPSK demodulator and carrier loop form a digital coherent detector. This technique offers a 2 dB advantage in error performance compared to a differential demodulator. The demodulator output are in-phase (I) and quadrature (Q) binary signals which together represent the recovered dibit stream. The dibit decoder circuit utilizes the recovered clock signal to convert this dibit stream to serial data at 1200 bps.

The recovered bit stream is then descrambled, using the inverse of the transmit scrambler algorithm. In synchronous mode the descrambler output is identically the received data, while in asynchronous mode the descrambler output stream is selectively processed by the receive buffer. Underspeed data presented to the transmitting modem passes essentially unchanged through the receive buffer. Overspeed data, which had stop bits deleted at the transmitter, has those stop bits reinserted by the receive buffer. (Generally, stop bit lengths will be elastic). The receive buffer output is then presented to the receive data pin (RXD) at a nominal intracharacter rate of 1219.05 bps.

Master Clock/Oscillator/Divider Chain

The μA212A or μA212AT may be controlled by either a quartz crystal operating in parallel mode or by an external signal source at 3.6864 MHz. The crystal should be connected between XTL1 and XTL2 pins, with a 30 pF capacitor from each pin to digital ground *(see Figure 1)*. Crystal requirements; $R_S < 150$ ohms, $C_L = 18$ pF, parallel mode, tolerance (accuracy, temp, aging) less than ±75 ppm. An external TTL drive may be applied to the XTL2 pin, with XTL1 grounded. Internal divider chains provide the timing signals required for modulation, demodulation, filtering, buffering, encoding/decoding, energy detection and remote digital loopback. Timing for line connect and disconnect sequences (handshaking) derives from the host controller, ensuring maximum applications flexibility.

Control Considerations

The host controller, whether a dedicated microcontroller or a digital interface, controls the μA212A or μA212AT as well as the line connect circuit and other IC's. On-chip timing and logic circuitry has been specifically designed to simplify the development of control firmware.

Operating and Test Modes

Table 1 indicates the operating and test modes defined by the eight control pins. The μA212A and μA212AT (together with the host controller) supports analog loopback, and local and remote digital loopback modes. Analog loopback forces the receiver to the transmitter channel. The controller forces the line control circuit on-hook but continues to monitor the ring indicator. This mode is available for low-

speed, highspeed synchronous and highspeed asynchronous operation. In local digital loop, the modem I.C. isolates the interface, slaves the transmit clock to SCR (high-speed mode), and loops received data back to the transmitter. In remote digital loop, local digital loop is initiated in the far-end modem by request of the near-end modem, if the far-end modem is so enabled. The μA212A and μA212AT includes the handshake sequences required for this mode; the controller merely monitors $\overline{RLST}$ and controls remote loopback according to *Table 3*. Remote loop is only available in high-speed mode.

Answer Tone In this mode, 2225 Hz answer tone is transmitted provided $\overline{TXSQ}$ is inactive high (= 1). Receive speed is selected as normal with the HS pin. This permits the speed of the originating modem to be determined while answer tone is continuously transmitted.

Force Continuous Mark Disconnects $\overline{TXD}$ pin from the transmitter and forces the signal internally to a mark (logic 1).

Force Continuous Space Disconnects $\overline{TXD}$ pin from the transmitter and forces the signal internally to a space (logic 0).

Analog Loop Receiver is forced to the transmitter channel. With modem on-hook (disconnected from line) signal from TXO is reflected through hybrid to RXIN.

Local Digital Loop Internally connects $\overline{RXD}$ to $\overline{TXD}$ and SCR to SCT. Transmitted data ($\overline{TXD}$) and clock (ETC) are ignored. SCR and SCT are provided. $\overline{RXD}$ is forced to 1.

Remote Digital Loop Initiating modem: If RDL is initiated ($\overline{TEST}$ = 0, HSK1 = 1, HSK2 = 0), $\overline{TXD}$ is isolated, $\overline{RXD}$ is clamped to a 1 and unscrambled mark is transmitted. When high speed scrambled dotting pattern is detected, scrambled mark is transmitted. At this point, upon receipt of scrambled mark, $\overline{RLST}$ is set to 0.

Responding modem: Upon receipt of unscrambled mark when in data mode ($\overline{TEST}$ = HSK1 = HSK2 = 1), $\overline{RLST}$ is set to 0. Upon detecting this the controller responds by setting $\overline{TEST}$ and HSK2 to 0, and the modem I.C. isolates $\overline{TXD}$, clamps $\overline{RXD}$ to 1, and transmits a 1200 bps scrambled dotting pattern. At this point, upon receipt of a scrambled mark signal, the modem I.C. internally loops RCVR data and clock to the XMTR, and sets $\overline{RLST}$ back to 1. (*See Table 3*)

Dialer Mode The μA212AT provides DTMF tone generation and energy indication at $\overline{EDET}$ pin to identify call progress tones, i.e. dial, busy and ringback. The DTMF digit is selected by the levels on O/$\overline{A}$, HS. MOD1 and MOD2 according to Table 2. Tone generation is turned on and off by the level on $\overline{TXSQ}$. 1 = on, 0 = off. The μA212A provides call progress indication only. $\overline{TXSQ}$ must be set to 0.

Table 2 DTMF Encoding[2] (μA212AT only)

O/$\overline{A}$	HS	MOD1	MOD2	DTMF Digit
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	*
1	0	1	1	#
1	1	0	0	A
1	1	0	1	B
1	1	1	0	C
1	1	1	1	D

Notes
1. DTMF digit is selected according to Table 2 for the μA212AT. $\overline{TXSQ}$ enables the tone generator: 1 = ON, 0 = OFF. $\overline{TXSQ}$ = 0 allows energy detection of call progress tone in both the μA212A and μA212AT.
2. For DTMF to operate dialer mode must be asserted. $\overline{TEST}$, HSK1 and HSK2 must be = 0.

Electrical Characteristics Unless otherwise noted: V_{DD} = 5.0 V ±5%, V_{SS} = −5.0 V ±5%, DGND = AGND = 0 V, T_A = 0°C to 70°C, typical characteristics specified at V_{DD} = 5.0 V, V_{SS} = −5.0 V, T_A = 25°C; all digital signals are referenced to DGND, all analog signals are referenced to AGND.

Table 1 Operating and Test Modes

$\overline{DOT}$	HS	$\overline{SYNC}$	MOD1	MOD2	$\overline{TEST}$	HSK1	HSK2	Description	SCT
0	–	X	X	X	1	1	1	Dotting Pattern (155 or 1200 bps)	INT
1	–	–	–	–	1	0	0	Answer Tone	X
1	–	–	–	–	1	0	1	Force Continuous Mark	X
1	–	–	–	–	1	1	0	Force Continuous Space	X
1	1	1	0	0	1	1	1	ASYNC, 8 Bit	INT
1	1	1	0	1	1	1	1	ASYNC, 9 Bit	INT
1	1	1	1	1	1	1	1	ASYNC, 10 Bit	INT
1	1	1	1	0	1	1	1	ASYNC, 11 Bit	INT
1	1	0	1	1	1	1	1	SYNC, Internal	INT
1	1	0	1	0	1	1	1	SYNC, Slave	SCR
1	1	0	0	1	1	1	1	SYNC, External	ETC
–	–	–	–	–	0	0	1	Analog Loop	ETC
1	–	X	X	X	0	1	1	Local Digital Loop	SCR
1	1	X	X	X	0	1	0	Response to Far End Request for RDL	SCR
1	0	X	X	X	–	–	–	Low Speed Mode	X
1	X	X	X	X	0	0	0	Dialer Mode, Note 1	X
1	1	–	–	–	0	1	0	Remote Digital Loop Initiate	X

Key:
SCT – TX Buffer and PSK Modulator Clock
SCR – Receive Clock
ETC – External Clock Input
INT – Internal 1200 Hz Clock
X – Don't Care
– – Set as appropriate for desired operating condition.

Table 3 Remote Digital Loopback (RDL) Command Sequences

Modem Action	Controller Action	$\overline{TEST}$	HSK1	HSK2	$\overline{RLST}$
Data Mode		1	1	1	1
Initiate RDL:	"INITIATE RDL"	0	1	0	1
Disable scrambler					
Disconnect $\overline{TXD}$					
Force 1 on $\overline{RXD}$					
Transmit unscrambled mark (U.M.)					
Recognize Dotting for 231 – 308 ms					
Enable scrambler					
Transmit scrambled mark (S.M.)					
Recognize S.M. for 231 – 308 ms					
Connect $\overline{TXD}$					
Unclamp $\overline{RXD}$					
"RDL ESTABLISHED"		0	1	0	0
Response to far end request:		1	1	1	0
U.M. recognized for 154 – 231 ms					
"RDL REQUESTED"	"RDL RESPONSE OK"	0	1	0	0
Disconnect $\overline{TXD}$					
Force 1 on $\overline{RXD}$					
Force Sync Slave Mode					
Transmit Dotting					
S.M. recognized					
Internally loop Receiver to Transmitter					
"RDL ESTABLISHED"		0	1	0	1
Terminate RDL:	$\overline{TXSO}$ active 80 ms	1	1	1*	0
Reset to Data Mode		1	1	1	1

*$\overline{TEST}$ = HSK1 = HSK2 = 1 may be asserted at anytime after "RDL ESTABLISHED" and before terminating.

Energy Detector

Symbol	Characteristic	Condition	Min	Typ	Max	Units
V_{thon}	Off/On Threshold	Voltage Level at RXIN		6.5		mV_{rms}
V_{thoff}	On/Off Threshold	Pin In Data Mode		5.2		
t_{on}	Energy Detect Time Data Mode	at $\overline{EDET}$ Pin	105	155	205	ms
t_{off}	Loss of Energy Detect Time		10	17	24	ms
V_{thon}	Dialer Mode					
V_{thon}	Off/On Threshold Dialtone	Voltage Level at RXIN		10		mV_{rms}
V_{thon}	Off/On Threshold Busy/Ringback	Pin in Dialer Mode		4.6		
t_{on}	Energy Detect in the Dialer Mode (Detecting Call Progress Tones)	At $\overline{EDET}$ Pin	25	30	35	ms
t_{off}	Energy Detect in the Dialer Mode (Detecting Call Progress Tones)		30	36	42	ms

System Performance

Symbol	Characteristic	Condition	Min	Typ	Max	Units
BER	**Bit Error Rate:** SNR required for BER = 10^{-5} @ 1200 bps on a 3002-C0 line, with 5 kHz white noise referred to 3 KHz. Figures shown are for originate mode. (Note: P_{line} values assume 4 dB net gain from line to RXIN)	P_{line} = –30 dBm P_{line} = –44 dBm		13 14		dB dB
	Telegraph Distortion	Back-to-Back, 300 bps (Low Speed Mode)		10		% Peak

Analog Line Interface

Symbol	Characteristic	Condition	Min	Typ	Max	Units
V_{line}	Output Level at TXO: Data Mode			0.7		V_{rms}
V_{tonh}	Output Level at TXO: DTMF HIGH Group			1.1		V_{rms}
V_{tonl}	Output Level at TXO: DTMF LOW Group			0.9		V_{rms}
$V_{\overline{TXSO}}$	Output level at TXO:			0.5		mV_{rms}
P_{ext}	Extraneous frequency output relative to DTMF power.	Any DTMF digit			–20	dB
V_{oo}	Output Offset at TXO			5.0		mV

Masterclock Input

Symbol	Characteristic	Condition	Min	Typ	Max	Units
F_{clock}	Clock Frequency			3.6864		MHz
T_{olclk}	Clock Frequency Tolerance		-.01		+.01	%
V_{exth}	External Clock Input HIGH	XTL2 driven and XTL1 grounded	4.5			V
V_{extl}	External Clock Input LOW	XTL2 driven and XTL1 grounded			0.5	V

Digital Interface

Symbol	Characteristic	Condition	Min	Typ	Max	Units
V_{IL}	Input Voltage LOW				0.6	V
V_{IH}	Input Voltage HIGH		2.2			V
V_{OL}	Output Voltage LOW	I_L = 2.0 mA			0.6	V
V_{OH}	Output Voltage HIGH	I_L = −2.0 mA	3.0			V
I_L	Input Current LOW	DGND ≤ V_{IN} ≤ V_{IL}, All Digital Inputs	−100			μA
I_{IH}	Input Current HIGH	V_{IH} ≤ V_{IN} ≤ V_{DD}	−50			μA
I_{DD}	Operating Current	V_{DD} = 5.0 V No Analog Signals		4.3	10	mA
I_{SS}	Operating Current	V_{SS} = −5.0 V No Analog Signals		−2.7	−5.0	mA

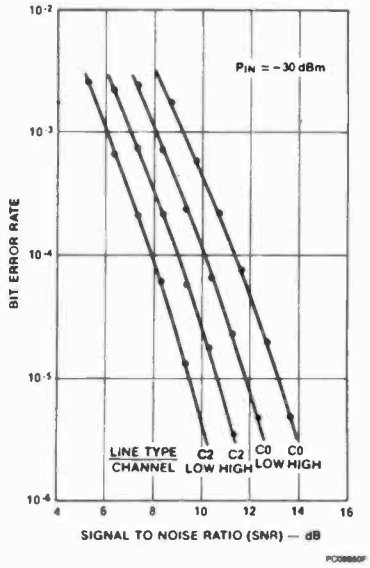
Transmit Buffer (Character Asynchronous Mode)

Symbol	Characteristic	Condition	Min	Typ	Max	Units
L_{txchar}	Input Character Length	Start bit + data bits + stop bit	8		11	bits
R_{txchar}	Intracharacter Signaling Rate	At $\overline{TXD}$ pin	1170	1200	1212	bps
L_{break}	Input Break Sequence Length	At $\overline{TXD}$ pin	23			bits

Receive Buffer (Character Asynchronous Mode) Carrier Frequencies and Signaling Rates

Symbol	Characteristic	Condition	Min	Typ	Max	Units
R_{txchar}	Intracharacter Signaling Rate	At $\overline{RXD}$ pin		1219.05		bps
F_{cxr} (ORIG)	HS Cxr Freq. (Orig. Mode)	Unmodulated Carrier		1200		Hz
F_{cxr} (ANS)	HS Cxr Freq. (Ans. Mode)	Unmodulated Carrier		2400		Hz
Baud	Dibit Rate	High Speed Mode		600		Baud
F_{mark} (ORIG)	Mark Frequency Originate Mode (1270)	Low Speed Mode		1269.42		Hz
F_{space} (ORIG)	Space Frequency Originate Mode (1070)	Low Speed Mode		1066.67		Hz
F_{mark} (ANS)	Mark Frequency Answer Mode/Answer Tone (2225)	Low Speed Mode		2226.09		Hz
F_{space} (ANS)	Space Frequency Answer Mode (2025)	Low Speed Mode		2021.05		Hz
F_{tonl}	DTMF Low Frequency Tone Group	Dialer Mode		698.2 771.9 853.3 942.3		Hz
F_{tonh}	DTMF High Frequency Tone Group	Dialer Mode		1209.4 1335.7 1476.9 1634.0		Hz
T_{ol}	Tolerance of all above Frequencies/Data Rates		-0.01		+0.01	%
bps	Data Rate	Low Speed Mode	0		300	bps

Figure 2 Bit Error Rate vs Signal-to-Noise Ratio



Note
BER measured in synchronous mode, using an AEA S3A channel simulator.

DTMF Dialing, the μA212A and μA212AT

The μA212A — the world's first and lowest power 1200/300 b/s single-chip modem — will be joined, at about mid-year, by the μA212AT. The second in a series of Fairchild modem IC products, the μA212AT is pin-compatible with the μA212A with the addition of an *integral DTMF tone generator*. This Bulletin summarizes factors to be considered in current μA212A-based modem designs for migration to the μA212AT.

DTMF Access

The μA212AT DTMF tone generator is accessed via the *Dialer* mode, which is asserted by setting $\overline{TEST}$ = HSK1 = HSK2 = 0. In the μA212A, *Dialer* mode offers only call-progress tone detection, but, in the μA212AT, both call-progress tone detection and DTMF tone generation are provided. The DTMF output is enabled by $\overline{TXSQ}$ = 1 and disabled by $\overline{TXSQ}$ = 0; $\overline{EDET}$ should be ignored when DTMF tones are being generated. *See Table 1.1.*

Table 1.1. Dialer Mode

$\overline{TXSQ}$	μA212A	μA212AT
0	Call-progress	Call-progress
1	Call-progress	DTMF generation

DTMF Tone-Pair Selection

The μA212AT employs 4 pins (O/$\overline{A}$, HS, MOD1, and MOD2) to generate 1 each of the 4 LOW and 4 HIGH group DTMF tones; nominal tone frequencies are shown in *Table 1.2. Table 1.3* displays the DTMF Encoding matrix.

Table 1.2 Tone Frequencies (Hz)

Low Group		High Group	
F (Nom.)	F (Act.)	F (Nom.)	F (Act.)
697	698.2	1209	1209.4
770	771.9	1336	1335.7
852	853.3	1477	1476.9
941	942.3	1633	1634.0

Output Characteristics

Table 1.4 summarizes nominal output levels at the TXO pin for Data mode, and for the DTMF Low and High tone groups. Absolute values and values relative to Data mode are shown.

Mode	$V_{txo(rms)}$	Relative (dB)
Data	0.70	0
DTMF Low	0.88	+2
DTMF High	1.11	+4

Therefore, if Data mode output power to a 600 Ω load is −9 dBm, tone output power is −7 dBm (Low group) and −5 dBm (HIGH group). These levels, as well as harmonic and out-of-band energy values conform to the requirements of EIA RS-496.

μA212AT Design-In Considerations

The μA212A and μA212AT are pin-compatible and functionally identical for all modes except DTMF tone generation. The μA212AT can therefore replace the μA212A in all current and future designs, provided that the following considerations are observed:

- **Ensure Proper Control Of The $\overline{TXSQ}$ Pin When In Dialer Mode.** *See Table 1.1.*
- **Provide μController Lines For The O/$\overline{A}$, HS, MOD1 And MOD2 Pins,** if any are not presently provided.
- **Plan For Replacement Of The Present Tone Dialing Scheme.** Current μA212A designs with DTMF dialing often employ a dialer chip or a DAC. Ensure that downstream removal of such parts will not affect the design.
- **Allow ROM Space.** Since DTMF control code replaces the previous scheme, this should not usually be a problem.

Table 1.3 DTMF Encoding Matrix ($\overline{TEST}$ = HSK1 = HSK2 = 0, $\overline{TXSQ}$ = 1)

O/$\overline{A}$	H/S	MOD1	MOD2	DTMF Digit
0	0	0	0	0
		0	1	1
		1	0	2
		1	1	3
0	1	0	0	4
		0	1	5
		1	0	6
		1	1	7
1	0	0	0	8
		0	1	9
		1	0	*
		1	1	#
1	1	0	0	A
		0	1	B
		1	0	C
		1	1	D

1. TMS 1121 UNIVERSAL TIMER CONTROLLER INTRODUCTION

The TMS 1121 Universal Timer Controller is a mask-programmed version of the TMS 1000 Family 4-bit single chip microcomputer providing the function of a programmable time of day, day of week controller. When the TMS 1121 is used to implement the general purpose timer controller function, as shown in Figure 1, the system features:

- 18 daily or weekly programmable timer sets
- Memory display of programmed timer sets for switches and day of week
- 4 independent switch outputs with buffer
- Display day of week, AM/PM, switch, clock, ON/OFF/SLEEP status
- Key entry for clock set and timer set
- 50 Hz or 60 Hz clock synchronization

The system is configured with a keyboard for user inputs, a 4-digit LED clock display, and LED's to indicate AM/PM, day of week, switches, and ON/OFF/SLEEP status. The device operates from a 9-volt power supply, and is packaged in a 28-pin plastic package. A system incorporating the TMS 1121 is capable of performing both as a digital clock and as a timer/controller.

CLOCK OPERATION

The TMS 1121 operates as a real-time clock which displays the time of day, AM or PM, and the day of the week. The accuracy of the clock is defined by the variation of the 50/60 Hz signal supplied to the device. Time of day and day of the week are entered through the keyboard and displayed on a 4-digit LED display.

TIMER/CONTROLLER

The TMS 1121 is capable of retaining up to 18 timer sets (programs) which are entered through the keyboard. Each of these timer sets can control one of four independent output switches which, in turn, can be used to control external devices.

Timer sets can be segregated into two types: (1) Fixed time programs which toggle an output switch at a specific time, and (2) Interval programs which toggle an output switch after a specified interval of time has elapsed. Each timer set will toggle only one switch. The SLEEP function (SLP) is used to turn a switch ON for one hour and then OFF, thereby using one timer set to perform two functions and thus saving one timer set. Interval programs are automatically deleted from memory upon execution. Fixed-time programs will be retained in memory and repeatedly executed.

The TMS 1121 has been designed so that the user can easily interface with the system via the keyboard (Figure 2). For example, using the keyboard the user can turn any output switch ON or OFF without programming the action into memory, thus providing direct control of the switches. Additionally, the user can change the timer settings by either selectively deleting all the timer sets which refer to one day or one switch, or by deleting all timer sets in order to start programming into a cleared memory. Finally, any program in memory can be called to the display with the proper keyboard sequence in order to verify that the TMS 1121 had been programmed correctly.

2. OPERATION

2.1 POWER-UP

When the TMS 1121 is powered up, the internal clock is automatically initialized to 12:00 PM on Sunday with all switches OFF and no programs stored. If the AC signal is 60 Hz, the clock setting is displayed immediately, if the AC signal is 50 Hz, the CLK key must be pressed to start and display the clock. After power-up the clock setting may be changed to a new value at any time.

Data supplied by Texas Instruments Limited.

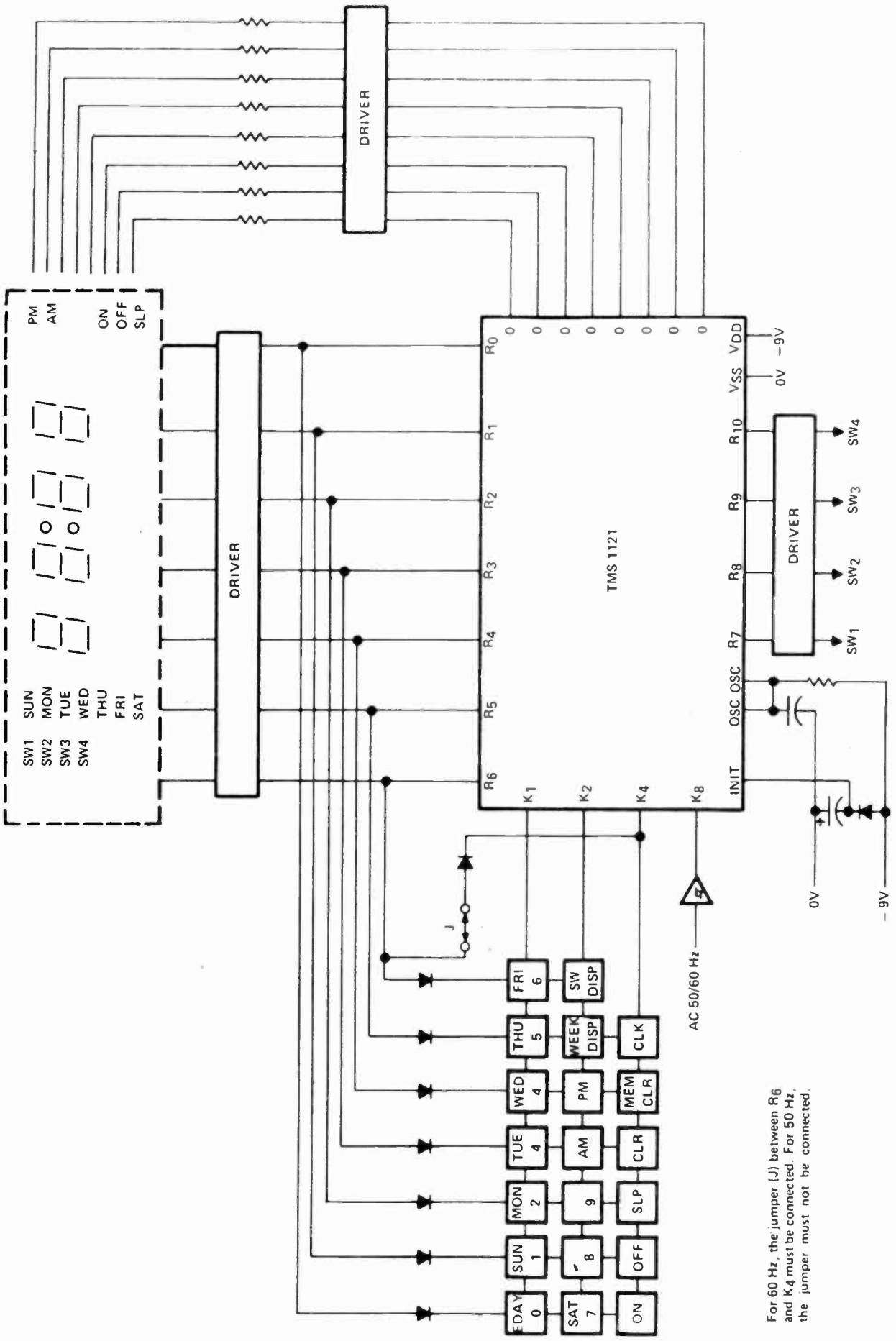
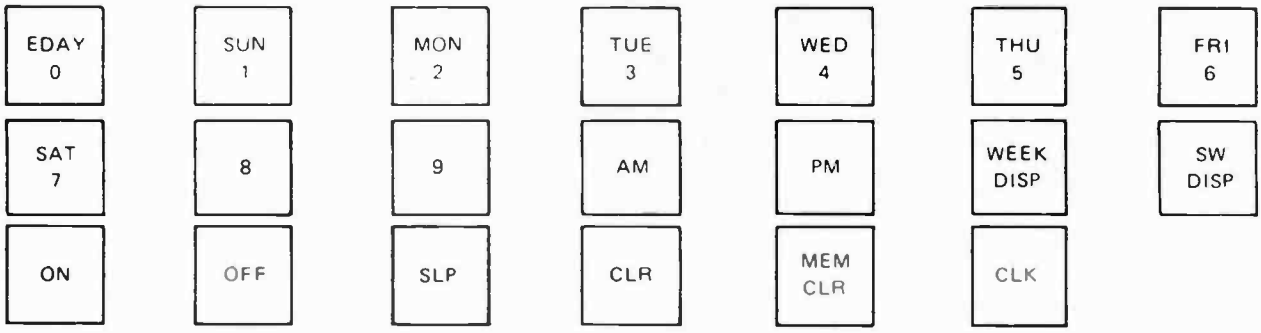


FIGURE 1. UNIVERSAL TIMER BLOCK DIAGRAM



Double functions key inputs

EDAY/0	–	Everyday or Numeric 0
SUN/1	–	Sunday or Numeric 1
MON/2	–	Monday or Numeric 2
TUE/3	–	Tuesday or Numeric 3
WED/4	–	Wednesday or Numeric 4
THU/5	–	Thursday or Numeric 5
FRI/6	–	Friday or Numeric 6
SAT/7	–	Saturday or Numeric 7
SW/DISP	–	Switch or Display of memory for switch
WEEK/DISP	–	Week or Display of memory for day of week and everyday

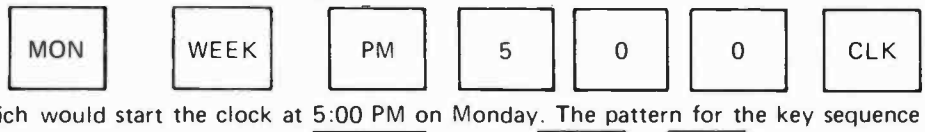
Single function key inputs

8	–	Numeric 8
9	–	Numeric 9
AM	–	AM setting
PM	–	PM setting
ON	–	ON setting
OFF	–	OFF setting
SLP	–	SLEEP setting
CLR	–	Clear entry and error
MEM CLR	–	Clear Memory
CLK	–	Clock Setting

FIGURE 2. KEYBOARD FOR THE UNIVERSAL TIMER CONTROLLER

2.2 SETTING THE CLOCK

A typical key sequence for setting the clock would be:



which would start the clock at 5:00 PM on Monday. The pattern for the key sequence is always the same. A day of of the week is registered with [WEEK] key. An [AM] or [PM] key is pressed and the desired time is entered, then the [CLK] key is pressed. Because the clock is not actually started from the new value until the [CLK] key is pressed, the timer clock may easily be synchronized with another clock. The value of the clock will only be changed if the key sequence has been correct, otherwise, the [CLK] key returns the display to the previous value of the clock, updated to the time the [CLK] key is pressed.

Errors in the key sequence may also be corrected before the [CLK] key is pressed. Correction Procedures are explained in the ERRORS section (2.5).

2.3 PROGRAMMING THE TIMER

2.3.1 FIXED-TIME PROGRAMS

Fixed-time programs change the state of a switch when the clock reaches a preset time. A typical key sequence for entering a fixed-time program would be:

, which would turn on switch number one on Monday at 5:10 PM. Keys [1], [2], [3], or [4] select the switch affected when followed by the [SW] key. The day and time are entered next, in the same order as the clock setting entry (section 2.2). The last key assigns a function to the program: [ON], [OFF], or [SLP]. [ON] or [OFF] turns the affected switch on or off at the programmed time. [SLP] causes the switch to be turned on at the time setting that has been entered, then turned off one hour later.

As the key sequence is entered, the digital readout and LED indicators display the program settings. The day of the week, time of day, switch number, and function of the program may remain on display without halting the operation of the timer; the clock runs and the switches are turned on or off regardless of the display status. Clock information may be redisplayed by pressing the [CLK] key.

If the next program is completely different from its predecessor, the above key sequence must be repeated in its entirety with the new parameters. If the switch affected and the day of the week are the same, a shortened key sequence suffices to store the program. An example of the shortened key sequence would be:

[PM] [5] [1] [5] [OFF]

If this sequence followed the above long sequence, output number one would be turned off at 5:15 PM on Monday. The shortened key sequence must follow the long one directly, without pressing the [CLK] key between programs. A succession of short sequences may follow each other, to program several actions of one switch on one day.

The [EDAY] key may be used in fixed-time programming in place of a day-of-the-week key. Programming an action with [EDAY] causes that action to occur at the programmed time on every day of the week.

2.3.2 INTERVAL PROGRAMS

In an interval program, the switch number, time interval (in hours and minutes) and function are entered. The function is performed after the time interval has passed. A typical interval program key sequence would be:

[3] [SW] [2] [0] [0] [ON]

In this case, switch number three would be turned on two hours after the [ON] key was pressed. Either the [ON], [OFF], or [SLP] functions may be used with an interval program. If [SLP] is used, the switch is turned on after the programmed interval, then turned off one hour later. As with fixed-time programs, a shortened key sequence may be used for a succession of programs following one with the ordinary sequence, as long as the switch is the same. An example of the short sequence for interval programs would be:

[2] [0] [1] [OFF]

Following the above entry, this sequence would turn switch three off two hours and one minute after the [OFF] key was pressed. The maximum time length for any interval is 11 hours, 59 minutes.

2.3.3 OVERLAPPING PROGRAMS

Programs may be overlapped in time. When several functions are programmed to occur at the same time on the same day, all of them are ignored except the last one. For example, if the memory contained the following programs:

[1] [SW] [MON] [WEEK] [AM] [1] [0] [0] [ON]
[1] [SW] [MON] [WEEK] [AM] [1] [0] [0] [OFF]
[1] [SW] [MON] [WEEK] [AM] [1] [0] [0] [ON]

the result would be to turn on switch one on Monday at 1:00 AM. Another example, the set of programs:

[4] [SW] [EDAY] [WEEK] [PM] [6] [4] [5] [ON]
[4] [SW] [SAT] [WEEK] [PM] [6] [4] [5] [OFF]

turns switch four on at 6:45 PM every day of the week except Saturday. Finally, the set of programs

[2] [SW] [FRI] [WEEK] [AM] [7] [0] [0] [SLP]
[2] [SW] [FRI] [WEEK] [AM] [7] [3] [0] [OFF]

would turn switch two off at 7:30 AM on Friday instead of 8:00 AM.

2.4 DIRECT SWITCH CONTROL

A switch may be operated directly from the keyboard. A sample key sequence would be:

[2] [SW] [SLP]

In this case, the [SLP] function would be immediately executed on switch number two. This switch would be turned on as soon as the [SLP] key is pushed and turned off one hour later. Any of the three functions may be specified for any of the four switches in this manner. The direct manipulations are not stored in RAM as programs.

2.5 ERRORS

The usual error indication is 99:99 on the display. This occurs if the key sequence is incorrect or if a program is attempted with an invalid time. The timer will convert times from the 24-hour system to 12-hour times for both clock setting and programming. The 12-hour time is found by subtracting 12 hours from a 24 hour time. If a 24-hour time, e.g. 22:10, is entered, it will be accepted as its 12-hour analog, 10:10, but the AM/PM selection is not affected by this conversion. Time values incorrect in both the 12-hour and 24-hour systems result in the 99:99 error indication.

The time conversion also holds true in interval programs and for this reason the interval length is limited to 11 hours, 59 minutes. Intervals up to 23 hours, 59 minutes will be accepted but corrected to 12-hour time-lengths. Again, interval programs incorrect in both systems will produce 99:99 on the display. The indication of 88:88 on the display occurs if an attempt is made to store more than 18 programs.

During program input, errors may be corrected by several methods. Depressing the [CLK] key will display the current clock setting and erase program or change of clock attempts that have not yet been stored, i.e. before keys [ON], [OFF], [SLP], or [MEM CLR] are pressed. The [CLR] key clears the display, and may therefore be used to clear errors before a program is stored. When more than four digits are entered from the keyboard, the leftmost digit is rolled off the display. Only the digits shown on the display when a key sequence is completed will be stored.

2.6 PROGRAM DISPLAY

The programs stored in memory can be displayed by depressing the [DISP] keys twice. For example, the key sequence:

[1] [SW/DISP] [SW/DISP] ...

displays the programs for switch number one. One program is displayed for every two times [SW/DISP] is pressed. The programs for a day of the week are displayed in the same way but using the [WEEK/DISP] key. A key sequence for Wednesday would be:

[WED] [WEEK/DISP] [WEEK/DISP] ...

Programs entered with the [EDAY] are displayed using that key and the [WEEK/DISP] key. For example,

[EDAY] [WEEK/DISP] [WEEK/DISP]

This key sequence only displays programs originally entered with [EDAY]. Programs entered on a specific day of the week must be displayed with the key corresponding to that day.

When a program is displayed, the digital readout shows the programmed time of the switch state change and the LED indicators show the day of the week, the number of the switch affected, and the function programmed. Both fixed-time and interval programs (before execution) can be displayed. When an interval program is shown, the display shows the programmed time of its execution, i.e. the time of day and day of the week corresponding to the end of the interval.

When programs using the [SLP] function are displayed, the display changes with the progress of the program execution. For example, the following key sequence would be used to turn switch three on for one hour on Friday at 10:00 AM.

[3] [SW] [FRI] [WEEK] [AM] [1] [0] [0] [0] [SLP]

Before this program is executed, displaying it would show it as a [SLP] program. The LED's would indicate switch three, Friday, 10:00 AM, and [SLP]. Between 10:00 and 11:00 AM on Friday, however, when the switch is on, displaying the program shows the time when the switch is to be turned off. In this case the LED's would show switch three, Friday, 11:00 AM, and OFF. After this time, the program display returns to the [SLP] settings. Each time the switch state of a [SLP] program changes, the program display is updated to show the next change in the switch state.

2.7 PROGRAM DELETE

The memory may be cleared entirely or selectively using the [MEM CLR] key. When pressed twice, this key clears everything stored in the RAM. The programs for an individual switch or day of the week may also be cleared without disturbing other stored programs.

[1] [SW] [MEM CLR]

is an example of a key sequence for deleting all the programs for switch number one.

[THU] [WEEK] [MEM CLR]

would delete the programs for Thursday. Programs stored specifically with the [EDAY] key are cleared using that key in place of a day of the week.

3. APPLICATIONS EXAMPLES

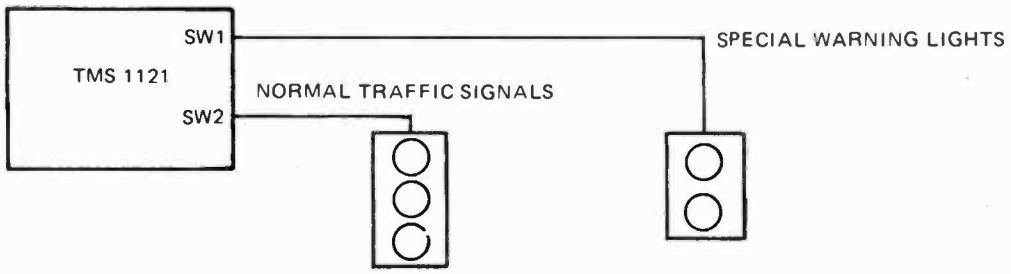
The TMS 1121 Universal Timer Controller can be used in systems designed for industrial, consumer and other applications. The four switches of the TMS 1121 can be used to control (turn ON and OFF) lights, sound signals, home appliances, etc.

The examples given below are intended only as illustrations to show how systems with TMS 1121 can be used and programmed. Design and implementation details are not discussed here and are left to the user's discretion.

3.1 TRAFFIC SIGNAL LIGHTS AT A SCHOOL ZONE (example)

Suppose it is desired that the timer control the signal lights at a street intersection near a school. For two hours in the morning and two hours in the afternoon, five days a week, the regular traffic signal at the intersection is to be turned off, to allow traffic to be manually directed, and special warning lights are to be turned on.

A block diagram of the system would be:



A set of programs for the TMS 1121 would begin by turning the traffic signal on initially with the sequence:

[2] [SW] [ON] .

The operation of the normal traffic signal would be governed by the set of programs:

2	SW	EDAY	WEEK	AM	7	0	0	OFF
				AM	9	0	0	ON
				PM	2	0	0	OFF
				PM	4	0	0	ON
2	SW	SAT	WEEK	AM	7	0	0	ON
				PM	2	0	0	ON
2	SW	SUN	WEEK	AM	7	0	0	ON
				PM	2	0	0	ON

This program set would turn the traffic signal off between 7:00 AM and 9:00 AM and between 2:00 PM and 4:00 PM, Monday through Friday. The signal would operate normally on Saturday and Sunday. In order to minimize memory usage, overlapping programs are used to keep the signal from being turned off over the weekend.

The operation of the special warning lights would be governed by the set of programs:

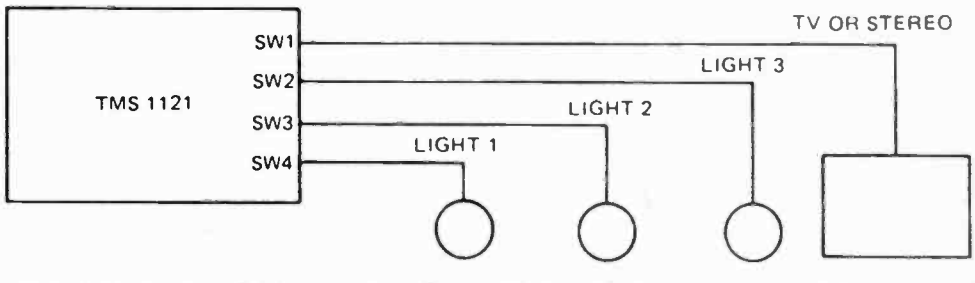
1	SW	EDAY	WEEK	AM	7	0	0	ON
				AM	9	0	0	OFF
				PM	2	0	0	ON
				PM	4	0	0	OFF
1	SW	SAT	WEEK	AM	7	0	0	OFF
				PM	2	0	0	OFF
1	SW	SUN	WEEK	AM	7	0	0	OFF
				PM	2	0	0	OFF

This set operates in the same manner as the previous one. In all, 16 programs are used.

3.2 HOME SECURITY (example)

The timer can be used to control the lighting in a home as a deterrent to potential burglars. The timer can be used to turn on lights and other electrical devices and make the house seem occupied when the residents are away. One problem with the implementation of this idea is that patterns in the lighting control are recognizable; the TMS 1121 has an advantage in this respect because of the number of programs that can be stored, and the long weekly cycle.

A block diagram of a system to control lights and other devices in a house would be:

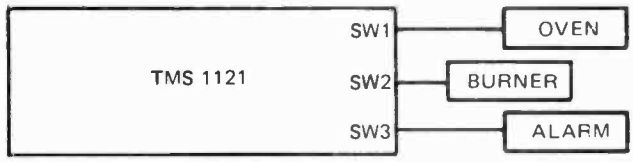


Programs operating the lights and television may be spread through a week in any order. An example for one evening might be:

1	SW	TUE	WEEK	PM		7	0	0	SLP
2	SW	TUE	WEEK	PM		6	1	7	ON
				PM	1	0	0	6	OFF
3	SW	TUE	WEEK	PM		6	3	3	ON
				PM		7	2	5	OFF
4	SW	TUE	WEEK	PM		8	1	1	ON
				PM	1	1	1	6	OFF

3.3 KITCHEN APPLIANCES (example)

A timer has numerous applications in the kitchen. In the control of an oven especially, timing is important. One example of connection to kitchen appliances is shown by the block diagram.:



In this example the sequence:

1	SW	ON		
1	SW	2	5	OFF

would turn the oven on when the ON key was pressed and off 25 minutes later.

The sequence

3	SW	2	5	ON
		2	6	OFF

entered at the same time as the oven program would sound the alarm for a minute after the oven has been turned off. The alarm could be stopped from the keyboard, before the minute was up, by the sequence

3	SW	OFF

Turning the oven on for 25 minutes could also be accomplished with fixed-time programs. They would turn the oven on between specific times of the day. The set of programs:

1	SW	TUE	WEEK	PM	6	0	0	ON
				PM	6	2	5	OFF
3	SW	TUE	WEEK	PM	6	2	5	ON
				PM	6	2	6	OFF

is an example for turning on the oven on Tuesday night between 6:00 and 6:25 PM.

A timed burner could be used in several ways. After turning it on the sequence

2	SW	ON

the cook could wait until it came up to a desired temperature before starting the timer. After this period, the program

2	SW	3	0	OFF

could be used to insure that the burner only remained on for thirty minutes, and an alarm could be sounded at the end of this period with

3	SW	3	0	ON
		3	0	OFF

4. TMS 1121 ELECTRICAL SPECIFICATIONS

4.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (Unless Otherwise Noted)*

Voltage applied to any device terminal (see Note 1)	−15 V
Supply voltage, V_{DD}	−15 V to 0.3 V
Data input voltage	−15 V to 0.3 V
Clock input voltage	−15 V to 0.3 V
Average output current (see Note 2)	
O outputs	−24 mA
R outputs	−14 mA
Peak output current: O outputs	−48 mA
R outputs	−28 mA
Continuous power dissipation: TMS 1121NLL	400 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

4.2 RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (see Note 3)		−8	−9	−10	V
High-level input voltage, V_{IH} (see Note 4)	K	−1.0	−0.8	0.3	V
	INIT or Clock	−1.0	−0.8	0.3	V
Low-level input voltage, V_{IL}	K	V_{DD}		−4	V
	INIT or Clock	V_{DD}	−9	−6	V
Clock cycle time, t_c (ϕ)		2.8	3	10	μs
Instruction cycle time, t_c		17		60	μs
Pulse width, clock high, t_w (ϕH)		1.2			μs
Pulse width, clock low, t_w (ϕL)		1.2			μs
Sum or rise time and pulse width, clock high, $t_r + t_w$ (ϕH)		1.4			μs
Sum of fall time and pulse width, clock low, $t_f + t_w$ (ϕL)		1.4			μs
Oscillator frequency, f_{osc}		250		350	kHz
Operating free-air temperature, t_A		0		70	°C

NOTES: 1. Unless otherwise noted all voltages are with respect to V_{SS}.
2. These average values apply for any 100 ms period.
3. Ripple must not exceed 0.2 volts peak to peak in the operating frequency range.
4. The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this specification for voltage levels only.

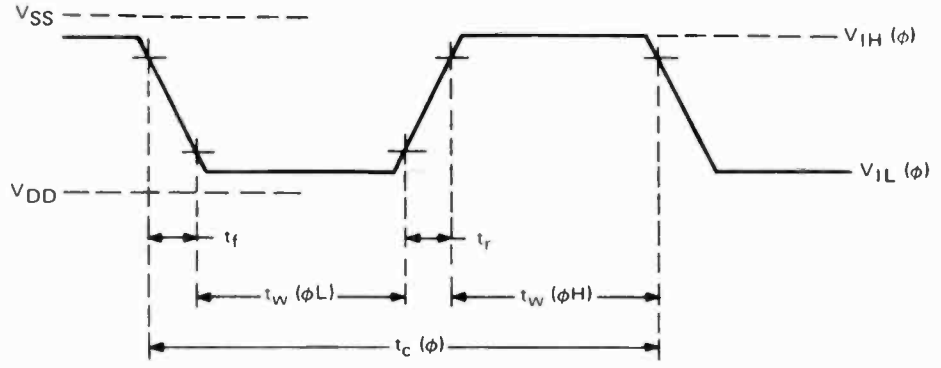


FIGURE 3. EXTERNALLY DRIVEN CLOCK INPUT WAVEFORM

4.3 ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (Unless Otherwise Noted)

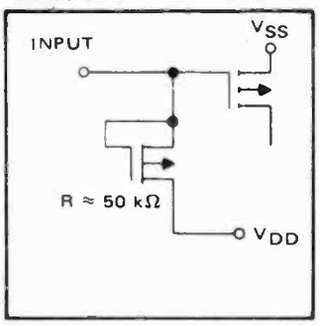
PARAMETER			TEST CONDITIONS	MIN	TYP*	MAX	UNIT
I_I	Input current, K inputs		V_I = 0 V	40	200	350	μA
V_{OH}	High-level output voltage (see Note 1)	O outputs	I_O = −6 mA	−1.1	−0.6		V
		R outputs	I_O = −1.2 mA	−0.75	−0.4		
I_{OL}	Low-level output current		$V_{OL} = V_{DD}$			−100	μA
I_{DD}	Average supply current from V_{DD}		All outputs open		−5	−10	mA
$P_{(AV)}$	Average power dissipation		All outputs open		45	100	mW
f_{osc}	Internal oscillator frequency		R_{ext} = 50KΩ, C_{ext} = 47 pF	250	300	350	kHz
C_i	Small-signal input capacitance, K inputs		V_I = 0, f = 1 kHz		10		pF
$C_{i(\phi)}$	Input capacitance, clock input		V_I = 0, f = 100 kHz		25		pF

*All typical values are at V_{DD} = −9 V, T_A = 25°C.

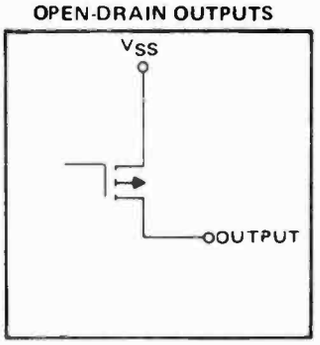
NOTE: 1. The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this specification for logic voltage levels only.

4.4 SCHEMATICS OF INPUTS AND OUTPUTS

TYPICAL OF ALL K INPUTS



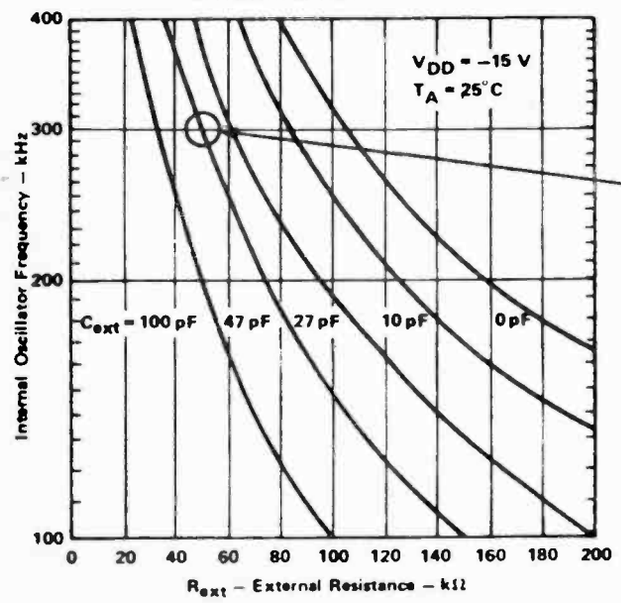
TYPICAL OF ALL O AND R OPEN-DRAIN OUTPUTS



The O outputs have nominally 60 Ω on-state impedance.

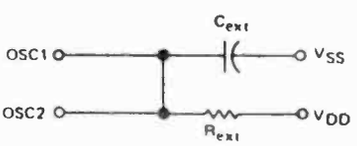
4.5 INTERNAL CLOCK

TYPICAL INTERNAL OSCILLATOR FREQUENCY vs EXTERNAL RESISTANCE



RECOMMENDED OPERATING POINT

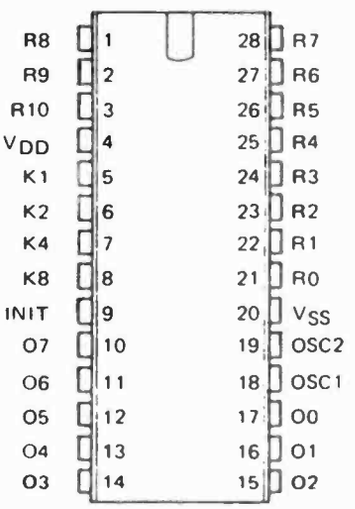
CONNECTION FOR INTERNAL OSCILLATOR

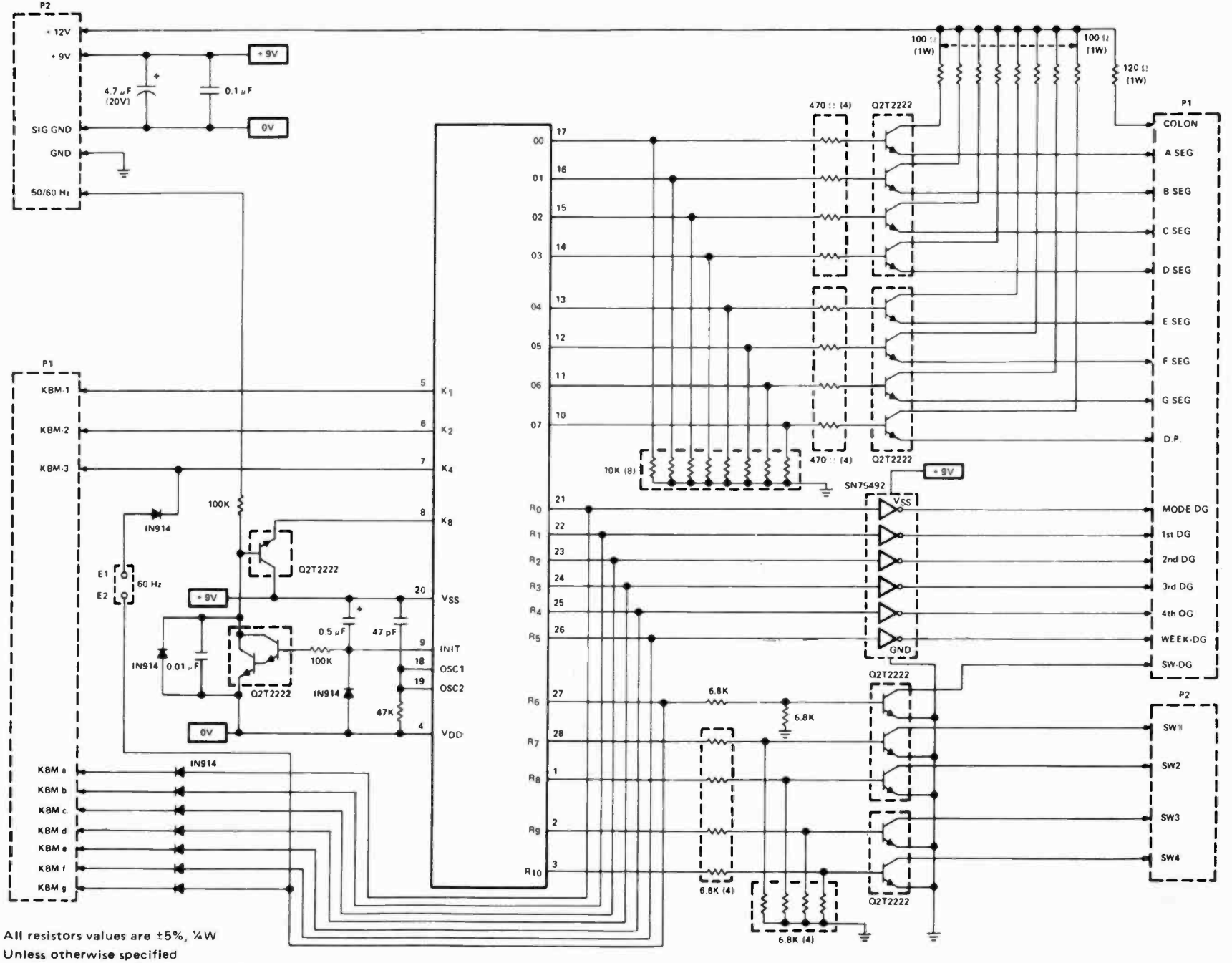


To use the internal oscillator, the OSC1 and OSC2 terminals are shorted together and tied to an external resistor to V_{DD} and a capacitor to V_{SS}.

4.6 TERMINAL ASSIGNMENTS

TMS 1121





NOTE: All resistors values are ±5%, ¼W
Unless otherwise specified
E1, E2 connection for 60Hz operation

FIGURE 4. UNIVERSAL TIMER CONTROLLER SYSTEM DIAGRAM

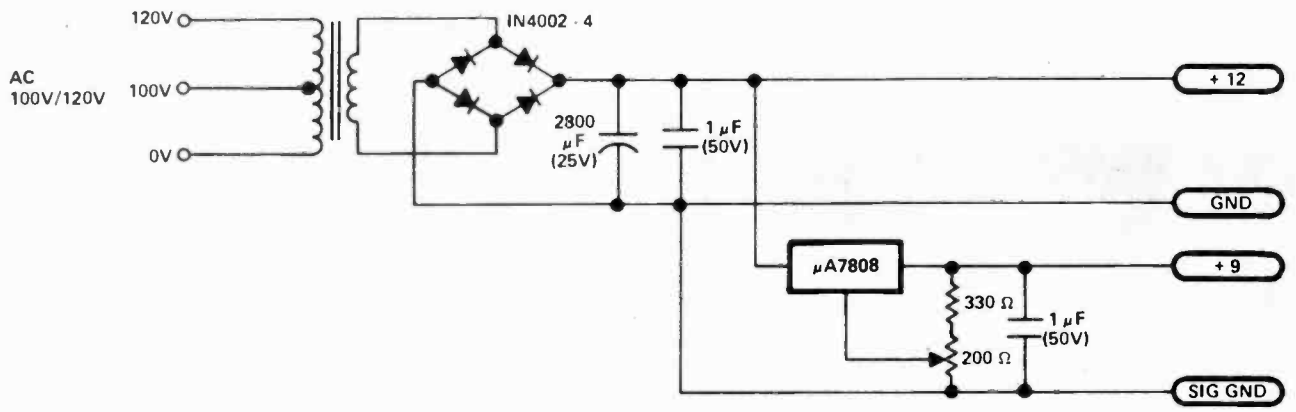
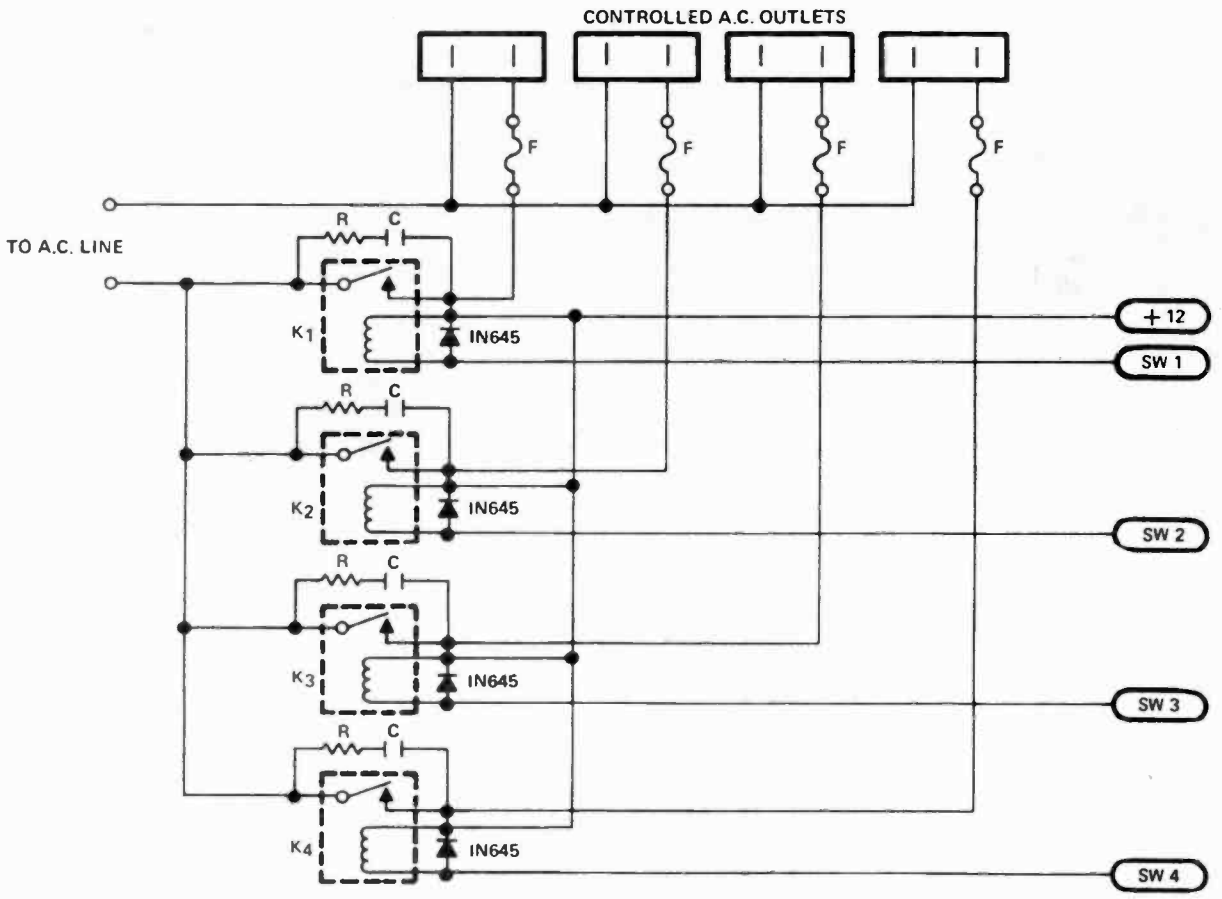


FIGURE 5. TYPICAL POWER SUPPLY FOR THE UNIVERSAL TIMER CONTROLLER



NOTE: R AND C ARE CONTACT ARCING SUPPRESSOR
R: 10 20 Ω (TYP)
C: 0.1 μF

FIGURE 6. TYPICAL A.C. OUTLET SWITCHING CIRCUIT FOR THE UNIVERSAL TIMER CONTROLLER

6. TMS 1122

These are the functional differences between the TMS 1121 and TMS 1122 TIMER circuits.

- POWER UP display by flashing LED, connected across 06 and R5 outputs.
- SET CLOCK by depressing "CLK" (across the matrix points K2/R4). AM/PM keys and LED's do not exist.
- MAXIMUM interval timer set remains at 11 hours 56 minutes.
- ERROR DISPLAY of 9999 when entry exceeds "24" hours.

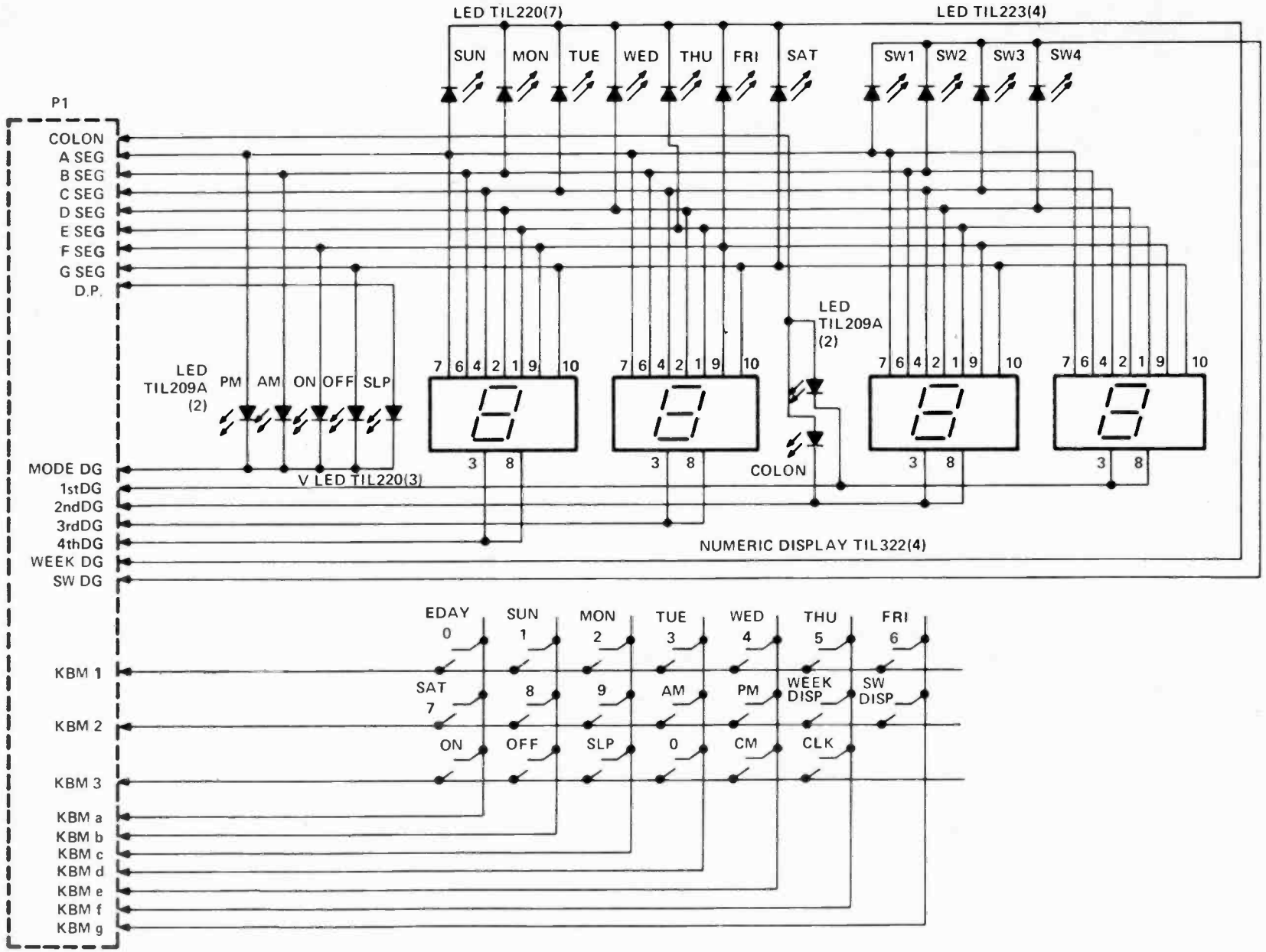
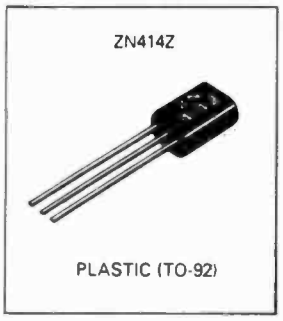
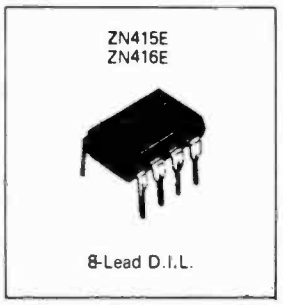


FIGURE 7. TMS 1121 DISPLAY AND KEYBOARD DIAGRAM

ZN415E, ZN416E AM Radio Receivers





FEATURES

- Single cell operation (1.1 to 1.6 volt operating range)
- Low current consumption
- 150kHz to 3MHz frequency range (i.e. full coverage of medium and long wavebands)
- Easy to assemble, no alignment necessary
- Simple and effective AGC action
- Will drive crystal earphone direct (ZN414Z)
- Will drive headphones direct (ZN415E and ZN416E)
- Excellent audio quality
- Typical power gain of 72dB (ZN414Z)
- Minimum of external components required

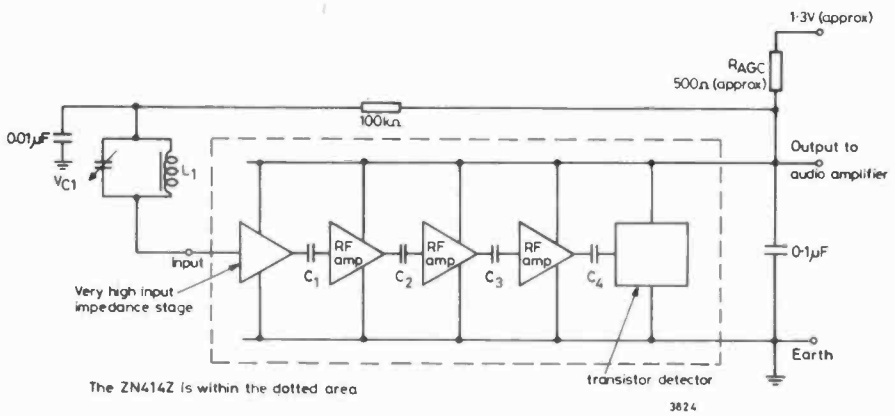
GENERAL DESCRIPTION

The ZN414Z is a 10 transistor tuned radio frequency (TRF) circuit packaged in a 3-pin TO-92 plastic package for simplicity and space economy.

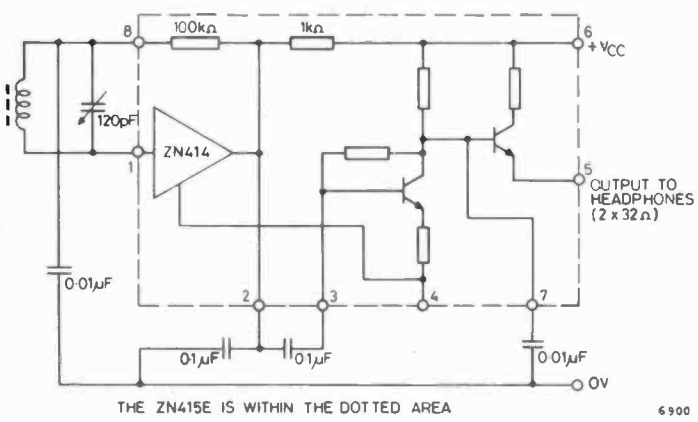
The circuit provides a complete R.F. amplifier, detector and AGC circuit which requires only six external components to give a high quality A.M. tuner. Effective AGC action is available and is simply adjusted by selecting one external resistor value. Excellent audio quality can be achieved, and current consumption is extremely low. No setting-up or alignment is required and the circuit is completely stable in use.

The ZN415E retains all the features of the ZN414Z but also incorporates a buffer stage giving sufficient output to drive headphones directly from the 8 pin DIL.

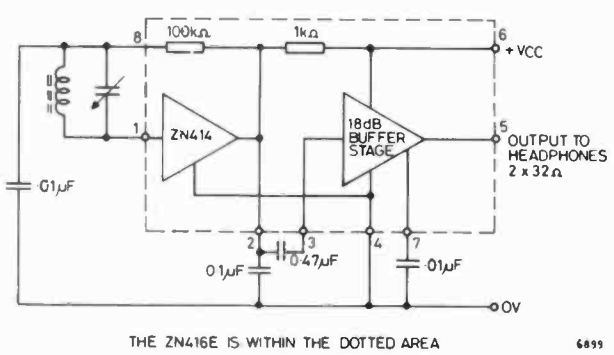
Similarly the ZN416E is a buffered output version of the ZN414Z giving typically 120mV (r.m.s.) output into a 64Ω load. The same package and pinning is used for the ZN416E as the ZN415E.



ZN414Z System Diagram



ZN415E System Diagram



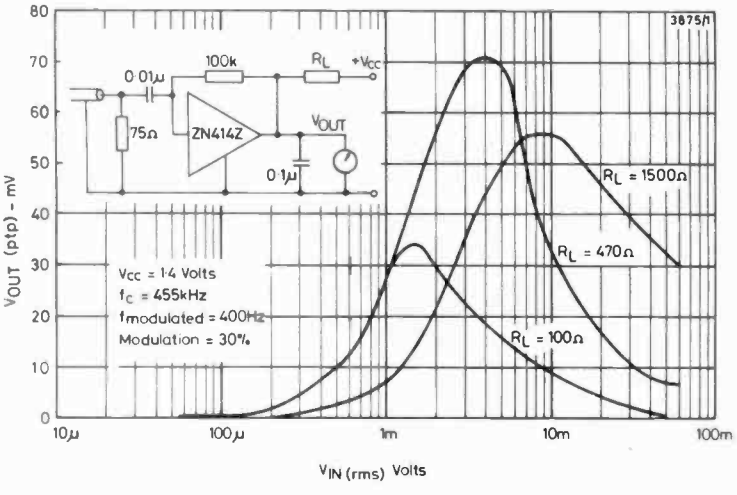
ZN416E System Diagram

DEVICE SPECIFICATIONS $T_{amb} = 25°C$, $V_{CC} = 1.4V$. Parameters apply to all types unless otherwise stated.

Parameter		Min.	Typ	Max.	Units
Supply voltage, V_{CC}		1.1	1.4	1.6	volts
Supply current, I_S	ZN414Z	-	0.3	0.5	mA
with 64 Ω	ZN415E		2.3	3	
headphones	ZN416E		4	5	
Input frequency range		0.15	-	3.0	MHz
Input resistance		-	4.0	-	MΩ
Threshold sensitivity (Dependant on Q of coil)			50		μV
Selectivity		-	4.0	-	kHz
Total harmonic distortion		-	3.0	-	%
AGC range		-	20	-	dB
Power gain (ZN414Z)			72		dB
Voltage gain of output stage	ZN415E	-	6	-	dB
	ZN416E		18		
Output voltage into 470Ω	ZN414Z	-	60	-	mVpp
Output voltage into 64Ω load	ZN415E		120		
before clipping	ZN416E		340		
Upper cut-off frequency of output stage, No capacitor, (ZN415E and ZN416E)		20	-	-	kHz
With 0.01μF between pin 7 and 0V (ZN415E)		-	6	-	kHz
With 0.01μF between pin 7 and 0V (ZN416E)		-	10	-	kHz
Lower cut-off frequency of output stage 0.1μF between pins 2 and 3 for ZN415E 0.47μF between pins 2 and 3 for ZN416E		-	50	-	Hz
Quiescent output voltage	ZN415E	-	80	-	mV
	ZN416E		200		
(See page 5 for ZN414Z)					
Operating temperature range		0	-	70	°C
Maximum storage temperature		−65	-	125	°C

ZN414Z CHARACTERISTICS – All measurements performed with 30% modulation, $F_M = 400Hz$

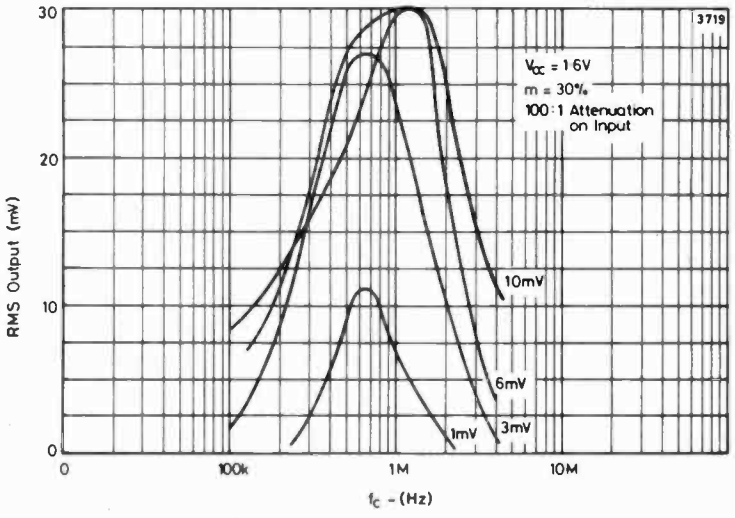
Gain and AGC characteristics



See operating notes for explanation of AGC action.

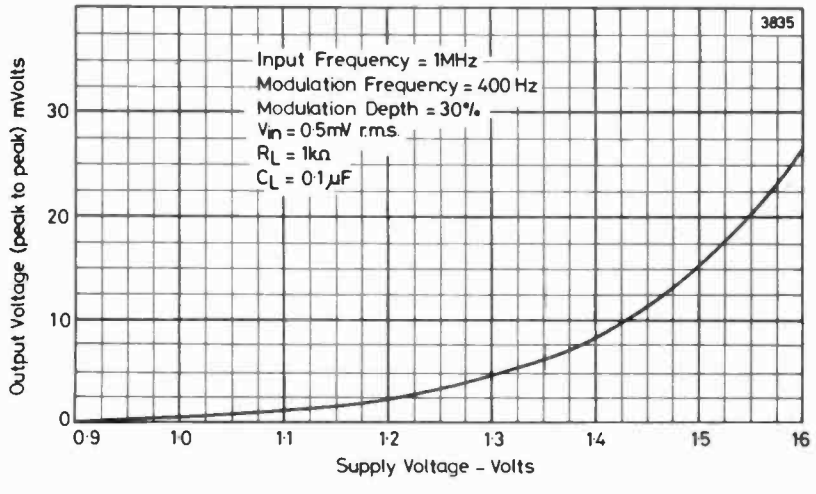
ZN414Z CHARACTERISTICS – *(Continued)*

Frequency response of the ZN414Z

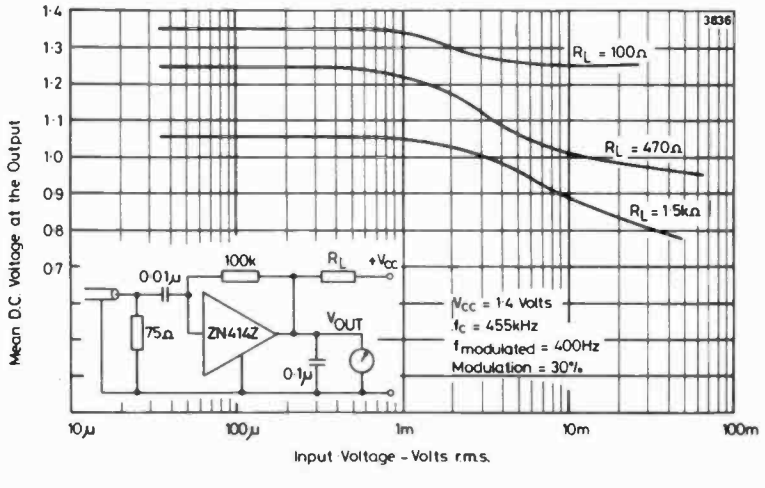


Note that this graph represents the chip response, and not the receiver bandwidth.

Gain variation with supply volts.



D.C. level at output



LAYOUT REQUIREMENTS

As with any high gain R.F. device, certain basic layout rules must be adhered to if stable and reliable operation is to be obtained. These are listed below:

1. The output decoupling capacitor should be soldered as near as possible to the output and earth leads of the ZN414Z. Furthermore, its value together with the AGC resistor (R_{AGC}) should be calculated at ≈4kHz, i.e.:

$$C\ (\text{farads}) = \frac{1}{2\pi \cdot R_{AGC} \cdot 4 \cdot 10^3}$$

2. All leeds should be kept as short as possible, especially those in close proximity to the ZN414Z.
3. The tuning assembly should be some distance from the battery, loudspeaker and their associated leads.
4. The 'earthy' side of the tuning capacitor should be connected to the junction of the 100kΩ resistor and the 0.01μF capacitor.

OPERATING NOTES

(a) Selectivity

To obtain good selectivity, essential with any T.R.F. device, the ZN414Z must be fed from an efficient, high 'Q' coil and capacitor tuning network. With suitable components the selectivity is comparable to superhet designs, except that a very strong signal in proximity to the receiver may swamp the device unless the ferrite rod aerial is rotated to "null-out" the strong signal.

Two other factors affect the apparent selectivity of the device. Firstly, the gain of the ZN414Z is voltage sensitive *(shown on page 5)* so that, in strong signal areas, less supply voltage will be needed tc obtain correct AGC action. Incorrect adjustment of the AGC causes a strong station to occupy a much wider bandwidth than necessary and in extreme cases can cause the RF stages to saturate before the AGC can limit RF gain. This gives the effect of swamping together with reduced AF output. All the above factors have to be considered if optimum performance is to be obtained.

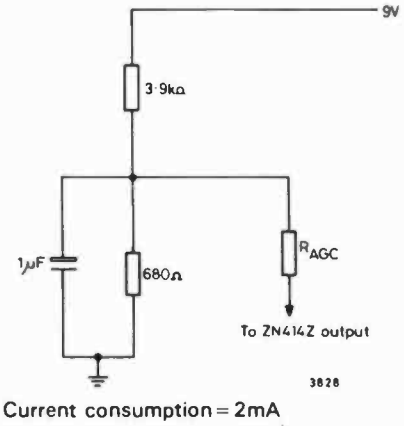
(b) Ferrite aerial size

Because of the gain variation available by altering supply voltage, the size of the ferrite rod is relatively unimportant. However, the ratio of aerial rod length to diameter should ideally be large to give the receiver better directional properties. Successful receivers have been constructed with ferrite rod aerials of 4cm (1.5") and up to 20cm (8").

(c) Trimmer

A suitable variable capacitor with a range of 10-120pF is available from Murata as the TZ03R1214.

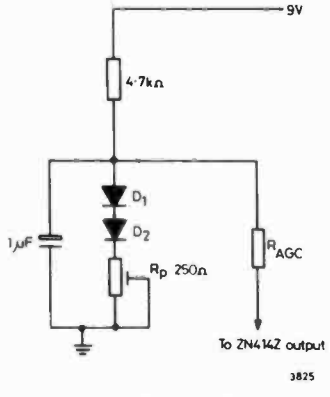
1. Resistive Divider



Current consumption = 2mA

Note: Replacing the 680Ω resistor with a 500Ω resistor and a 250Ω preset, sensitivity may be adjusted and will enable optimum reception to be realised under most conditions.

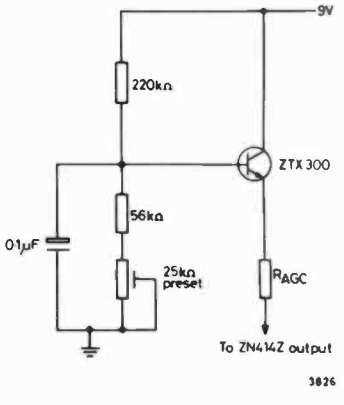
2. Diode Drive



Current consumption ≈ 1.5mA

$D_1 = D_2$ = Any general purpose silicon diode
R_p = Optional sensitivity control, a recommended value being 250Ω.

3. Transistor Drive



Current consumption is virtually that which is taken by the ZN414Z (0.3mA)

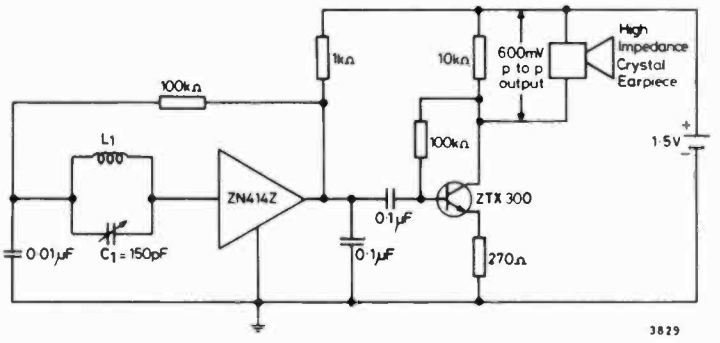
DRIVE CIRCUITS

Three types of drive circuit are shown, each has been used successfully. The choice is largely an economic one, but circuit 3 is recommended wherever possible, having several advantages over the other circuits. Values for 9V supplies are shown, simple calculations will give values for other supplies.

RECOMMENDED CIRCUITS

(a) Earphone radio

The ZN414Z will drive a sensitive earpiece directly. In this case, an earpiece of equivalent impedance to R_{AGC} is substituted for R_{AGC} in the basic tuner circuit. Unfortunately, the cost of a sensitive earpiece is high, and unless an ultra-miniature radio is wanted, it is considerably cheaper to use a low cost crystal earpiece and add a single gain stage. One further advantage of this technique is that provision for a volume control can be made. A suitable circuit is shown below.

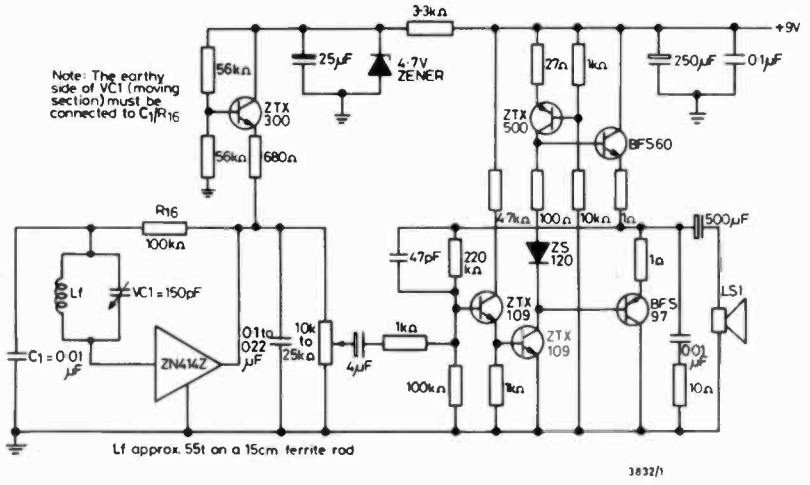


$L_1 \approx 80$ turns of 0.3mm dia. enamelled copper wire on a 5cm or 7.5cm long ferrite rod. Do not expect to adhere rigidly to the coil-capacitor details given. Any value of L_1 and C_1 which will give a high 'Q' at the desired frequency may be used.

Volume Control: a 250Ω potentiometer in series with a 100Ω fixed resistor substituted for the 270Ω emitter resistor provides an effective volume control.

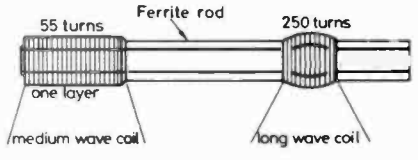
(b) Domestic portable receiver

The circuit shown is capable of excellent quality, and its cost relative to conventional designs is much lower.

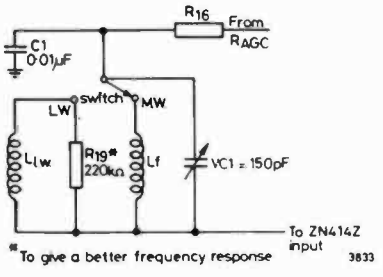


The complete circuit diagram of the Triffid receiver

(b)i



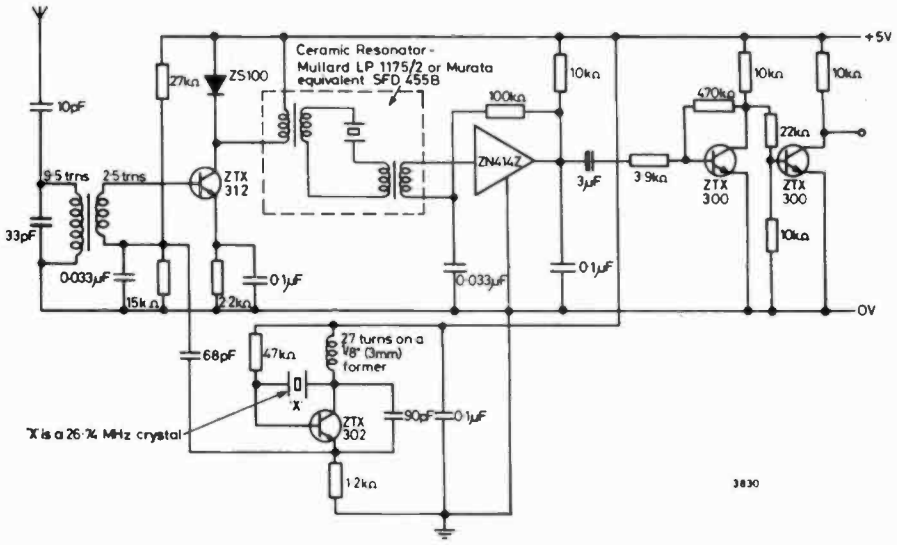
28 swg Wire
FERRITE ROD 6", ⅜" dia.



Coil winding details and waveband selection

(c) Use in model control receiver

The circuit below shows a ZN414Z used as an I.F. amplifier for a 27MHz superhet receiver.



Performance Details:

Sensitivity = 2.5μV for a 5V p.t.p. output measured at f_C = 27.21MHz, 100% modulated with 100Hz square wave.

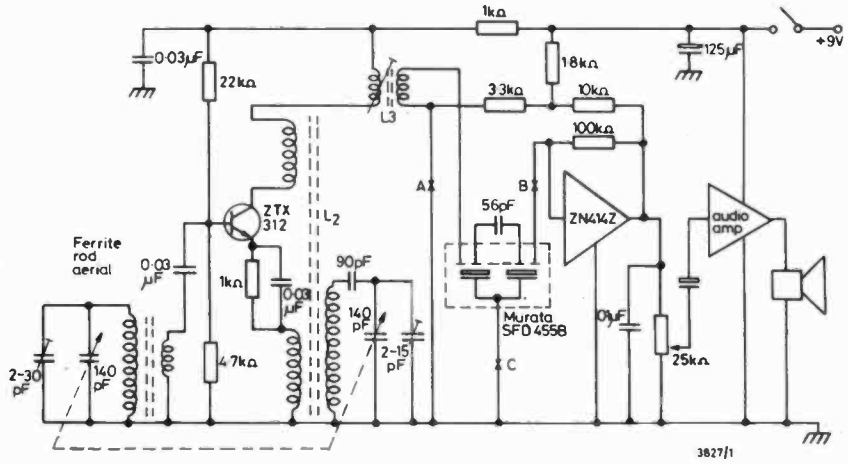
Selectivity: ±5kHz for <100mV p.t.p. output.

Input Signal Range: 2.5μV to 25mV (i.e. 80dB)

Supply Current: ≈4.5mA.

(d) Broadcast band superhet using ZN414Z

The ZN414Z coupled with the modern ceramic resonators offers a very good I.F. amplifier at modest cost, whilst maintaining simplicity and minimal alignment requirements. A typical circuit is shown below:



– 6dB Bandwidth = 6kHz

– 30dB Bandwidth = 8kHz

AGC Range ≈ 40dB

(For 10dB change in A.F. output).

FURTHER APPLICATIONS

The ZN414Z is an extremely versatile device and, in a data sheet, it is not possible to show all its varied applications. A comprehensive applications note on the device is available which gives full details of various radio receivers, I.F. amplifiers and frequency standards together with comprehensive technical information.

Fluid Detector

General Description

The LM1830 is a monolithic bipolar integrated circuit designed for use in fluid detection systems. The circuit is ideal for detecting the presence, absence, or level of water, or other polar liquids. An ac signal is passed through two probes within the fluid. A detector determines the presence or absence of the fluid by comparing the resistance of the fluid between the probes with the resistance internal to the integrated circuit. An ac signal is used to overcome plating problems incurred by using a dc source. A pin is available for connecting an external resistance in cases where the fluid impedance is of a different magnitude than that of the internal resistor. When the probe resistance increases above the preset value, the oscillator signal is coupled to the base of the open-collector output transistor. In a typical application, the output could be used to drive a LED, loud speaker or a low current relay.

Features

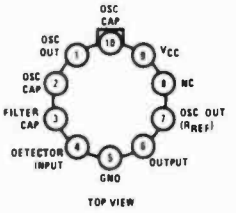
- Low external parts count
- Wide supply operating range
- One side of probe input can be grounded
- ac coupling to probe to prevent plating
- Internally regulated supply
- ac or dc output

Applications

- Beverage dispensers
- Water softeners
- Irrigation
- Sump pumps
- Aquaria
- Radiators
- Washing machines
- Reservoirs
- Boilers

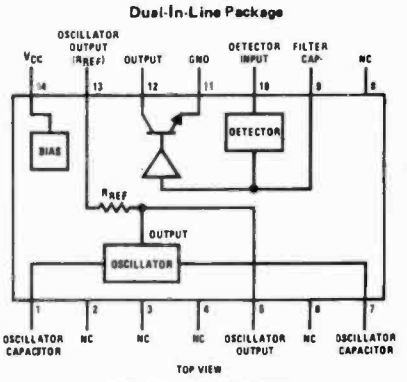
Logic and Connection Diagrams

Metal Can Package



Order Number LM1830H
See NS Package H10C

Dual-In-Line Package



Order Number LM1830N
See NS Package N14A

Absolute Maximum Ratings

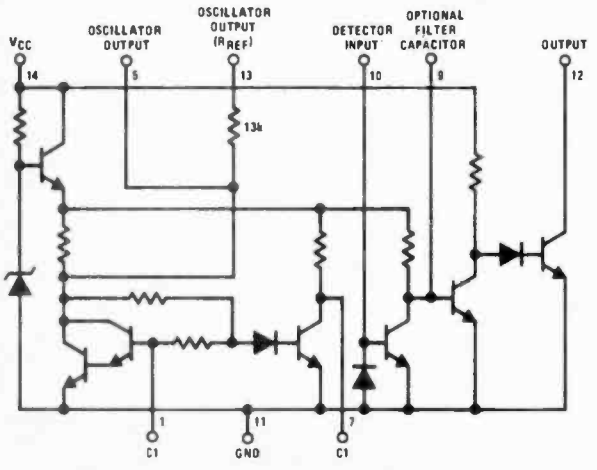
Supply Voltage	28V
Power Dissipation (Note 1)	300 mW
Output Sink Current	20 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−40°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

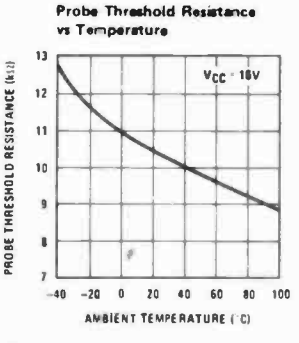
Electrical Characteristics (V^+ = 16V, T_A = 25°C unless otherwise specified)

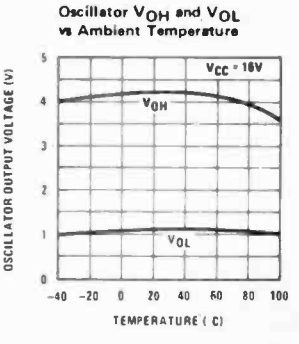
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current			5.5	10	mA
Oscillator Output Voltage					
Low			1.1		V
High			4.2		V
Internal Reference Resistor		8	13	25	kΩ
Detector Threshold Voltage			680		mV
Detector Threshold Resistance		5	10	15	kΩ
Output Saturation Voltage	I_O = 10 mA		0.5	2.0	V
Output Leakage	$V_{PIN\ 12}$ = 16V			10	μA
Oscillator Frequency	C1 = 0.001μF	4	7	12	kHz

Note 1: The maximum junction temperature rating of the LM1830N is 150°C. For operation at elevated temperatures, devices in the dual-in-line plastic package must be derated based on a thermal resistance of 175°C/W.

Schematic Diagram







Data supplied by National Semiconductor.

Application Hints

The LM1830 requires only an external capacitor to complete the oscillator circuit. The frequency of oscillation is inversely proportional to the external capacitor value. Using 0.001μF capacitor, the output frequency is approximately 6 kHz. The output from the oscillator is available at pin 5. In normal applications, the output is taken from pin 13 so that the internal 13k resistor can be used to compare with the probe resistance. Pin 13 is coupled to the probe by a blocking capacitor so that there is no net dc on the probe.

Since the output amplitude from the oscillator is approximately 4 V_{BE}, the detector (which is an emitter base junction) will be turned "ON" when the probe resistance to ground is equal to the internal 13 kΩ resistor. An internal diode across the detector emitter base junction provides symmetrical limiting of the detector input signal so that the probe is excited with ±2 V_{BE} from a 13 kΩ source. In cases where the 13 kΩ resistor is not compatible with the probe resistance range, an external resistor may be added by coupling the probe to pin 5 through the external resistor as shown in *Figure 2*. The collector of the detecting transistor is brought out to pin 9 enabling a filter capacitor to be connected so that the output will switch "ON" or "OFF" depending on the probe resistance. If this capacitor is omitted, the output will be switched at approximately 50% duty cycle when the probe resistance exceeds the reference resistance. This can be useful when an audio output is required and the output transistor can be used to directly drive a loud speaker. In addition, LED indicators do not require dc excitation. Therefore, the cost of a capacitor for filtering can be saved.

In the case of inductive loads or incandescent lamp loads, it is recommended that a filter capacitor be employed.

In a typical application where the device is employed for sensing low water level in a tank, a simple steel probe may be inserted in the top of the tank with the tank grounded. Then when the water level drops below the tip of the probe, the resistance will rise between the probe and the tank and the alarm will be operated. This is illustrated in *Figure 3*. In situations where a non-conductive container is used, the probe may be designed in a number of ways. In some cases a simple phono plug can be employed. Other probe designs include conductive parallel strips on printed circuit boards.

It is possible to calculate the resistance of any aqueous solution of an electrolyte for different concentrations, provided the dimensions of the electrodes and their spacing is known.

The resistance of a simple parallel plate probe is given by:

$$R = \frac{1000}{c.p} \cdot \frac{d}{A} \quad \Omega$$

where A = area of plates (cm^2)
d = separation of plates (cm)
c = concentration (gm. mol. equivalent/litre)
p = equivalent conductance ($\Omega^{-1}\ cm^2\ equiv.^{-1}$)

(An equivalent is the number of moles of a substance that gives one mole of positive charge and one mole of negative charge. For example, one mole of NaCl gives $Na^+ + Cl^-$ so the equivalent is 1. One mole of $CaCl_2$ gives $Ca^{++} + 2Cl^-$ so the equivalent is 1/2.)

Usually the probe dimensions are not measured physically, but the ratio d/A is determined by measuring the resistance of a cell of known concentration c and equivalent conductance of 1. A graph of common solutions and their equivalent conductances is shown for reference. The data was derived from D.A. MacInnes, "The Principles of Electrochemistry," Reinhold Publishing Corp., New York., 1939.

In automotive and other applications where the power source is known to contain significant transient voltages, the internal regulator on the LM1830 allows protection to be provided by the simple means of using a series resistor in the power supply line as illustrated in *Figure 4*. If the output load is required to be returned directly to the power supply because of the high current required, it will be necessary to provide protection for the output transistor if the voltages are expected to exceed the data sheet limits.

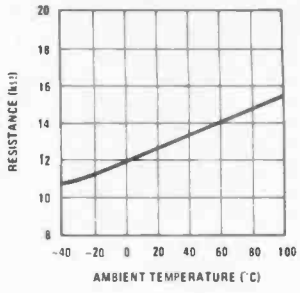
Although the LM1830 is designed primarily for use in sensing conductive fluids, it can be used with any variable resistance device, such as light dependent resistor or thermistor or resistive position transducer.

The following table lists some common fluids which may and may not be detected by resistive probe techniques.

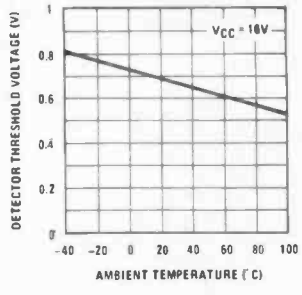
Conductive Fluids	Non-Conductive Fluids
City water	Pure water
Sea water	Gasoline
Copper sulphate solution	Oil
Weak acid	Brake fluid
Weak base	Alcohol
Household ammonia	Ethylene glycol
Water and glycol mixture	Paraffin
Wet soil	Dry soil
Coffee	Whiskey

Typical Performance Characteristics

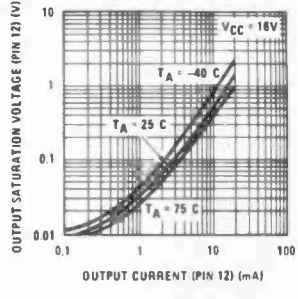
Reference Resistor vs Ambient Temperature



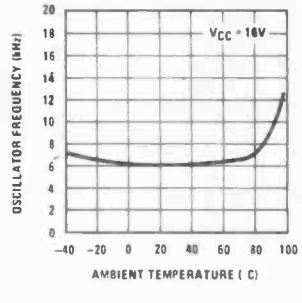
Detector Threshold Voltage vs Temperature



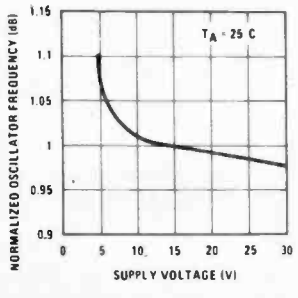
Output Saturation Voltage vs Output Current



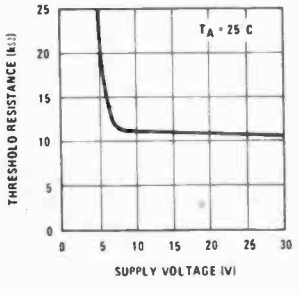
Oscillator Frequency vs Ambient Temperature



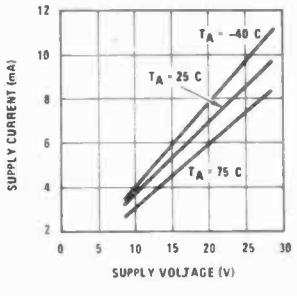
Normalized Oscillator Frequency vs Supply Voltage



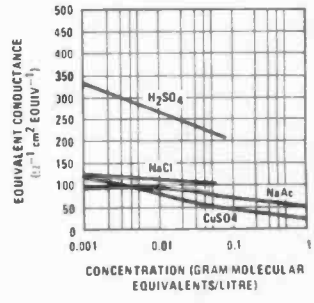
Threshold Resistance vs Supply Voltage



Power Supply Current vs Supply Voltage



Equivalent Resistance vs Concentration of Several Solutions



Application Hints (Continued)

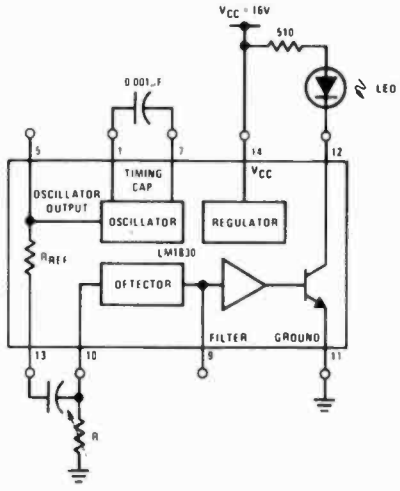


FIGURE 1. Test Circuit

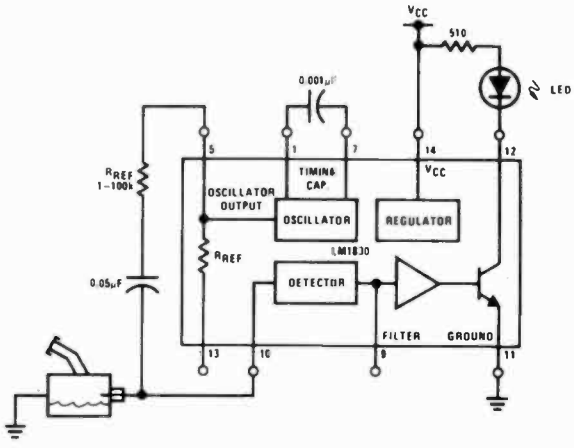


FIGURE 2. Application Using External Reference Resistor

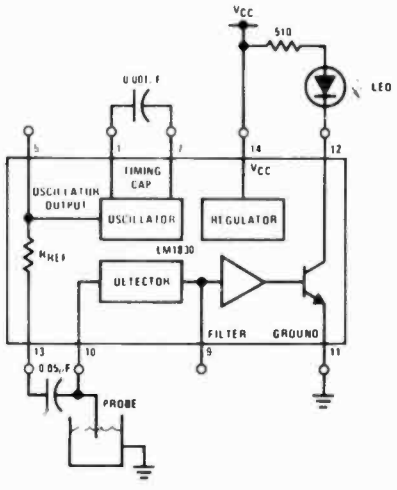
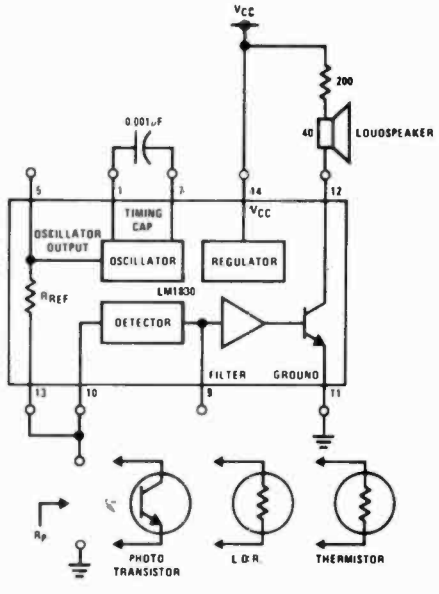


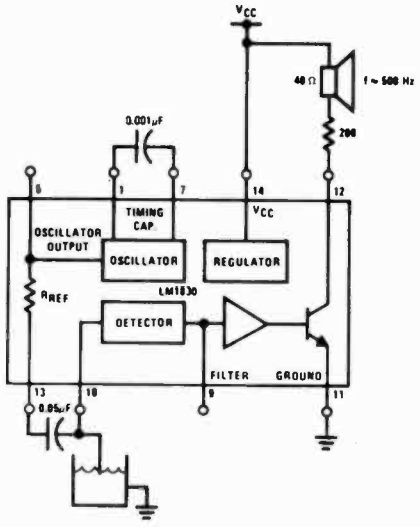
FIGURE 3. Basic Low Level Warning Device with LED Indication



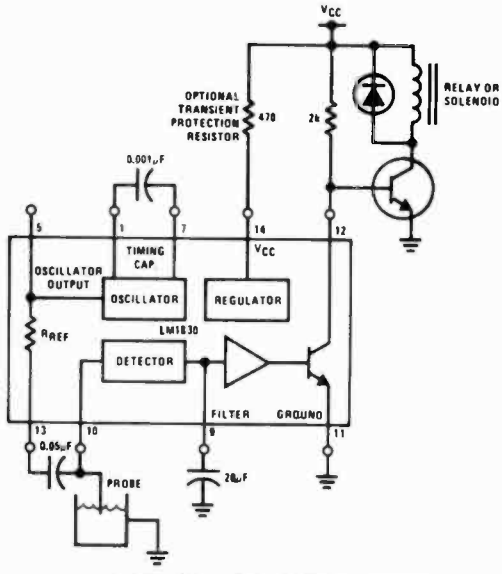
Output is activated when $R_p \gtrsim 1/3\ R_{REF}$

FIGURE 4. Direct Coupled Applications

Typical Applications



Low Level Warning with Audio Output



The output is suitable for driving a sump pump or opening a drain valve, etc.

High Level Warning Device

Programmable Sound Generator

FEATURES:

- Full software control of sound generation
- Interfaces to most 8-bit and 16-bit microprocessors
- Three independently programmable analog outputs
- One or two 8-bit I/O ports
- Single 5 volt supply
- Full 0° to 70°C operation
- 40 pin or 28 pin package option

DESCRIPTION

The AY-3-8910A/8912A Programmable Sound Generator (PSG) is an LSI circuit which can produce a wide variety of complex sounds under software control. The AY-3-8910A/8912A is manufactured in the General Instrument Microelectronics N-Channel Ion Implant Process. Operation requires a single +5V power supply, a TTL compatible clock, and a microprocessor controller, such as the General Instrument 16-bit CP1610 or one of the PIC1650 series of 8-bit microcomputers.

The PSG is easily interfaced to any bus oriented system. Its flexibility makes it useful in applications such as music synthesis, sound effects generation, audible alarms, tone signaling, and home computer usage. In order to generate sound effects while allowing the processor to perform other tasks, the PSG can continue to produce sound after the initial commands have been given by the control processor. The fact that realistic sound production often involves more than one component is satisfied by the three independently controllable analog sound output channels available in the PSG. These analog sound output channels can each provide 4 bits of logarithmic digital to analog conversion, greatly enhancing the dynamic range of the sounds produced.

All circuit control signals are digital in nature and may be provided directly by a microprocessor/microcomputer. Therefore, one PSG can produce the full range of required sounds with no change in external circuitry. Since the frequency response of the PSG ranges from sub-audible at its lowest frequency to post-audible at its highest frequency, there are few sounds which are beyond reproduction.

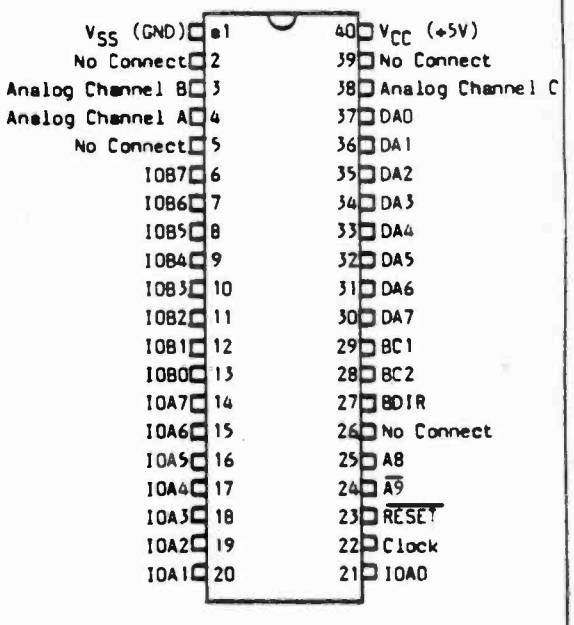
PIN FUNCTIONS

DA7—DA0 (Input/Output/High Impedance)
Data/Address Bits 7-0: Pins 30-37 (AY-3-8910A)
Pins 21-28 (AY-3-8912A)

These 8 lines comprise the 8-bit bidirectional bus used by the microprocessor to send both data and addresses to the PSG, and to receive data from the PSG. In the address mode, DA3—DA0 select the internal register address ($0—17_8$) and DA7—DA4 in conjunction with address inputs $\overline{A9}$ and A8, form the chip select function. When the high order address bits are "incorrect", the bidirectional buffers are forced to a high impedance state.

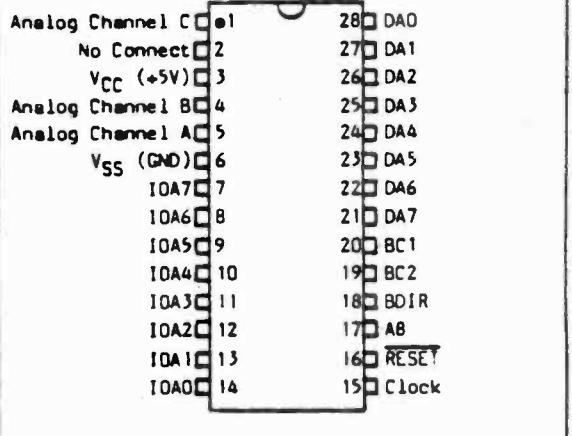
PIN CONFIGURATION
40 LEAD DUAL IN LINE

AY-3-8910A Top View



28 LEAD DUAL IN LINE

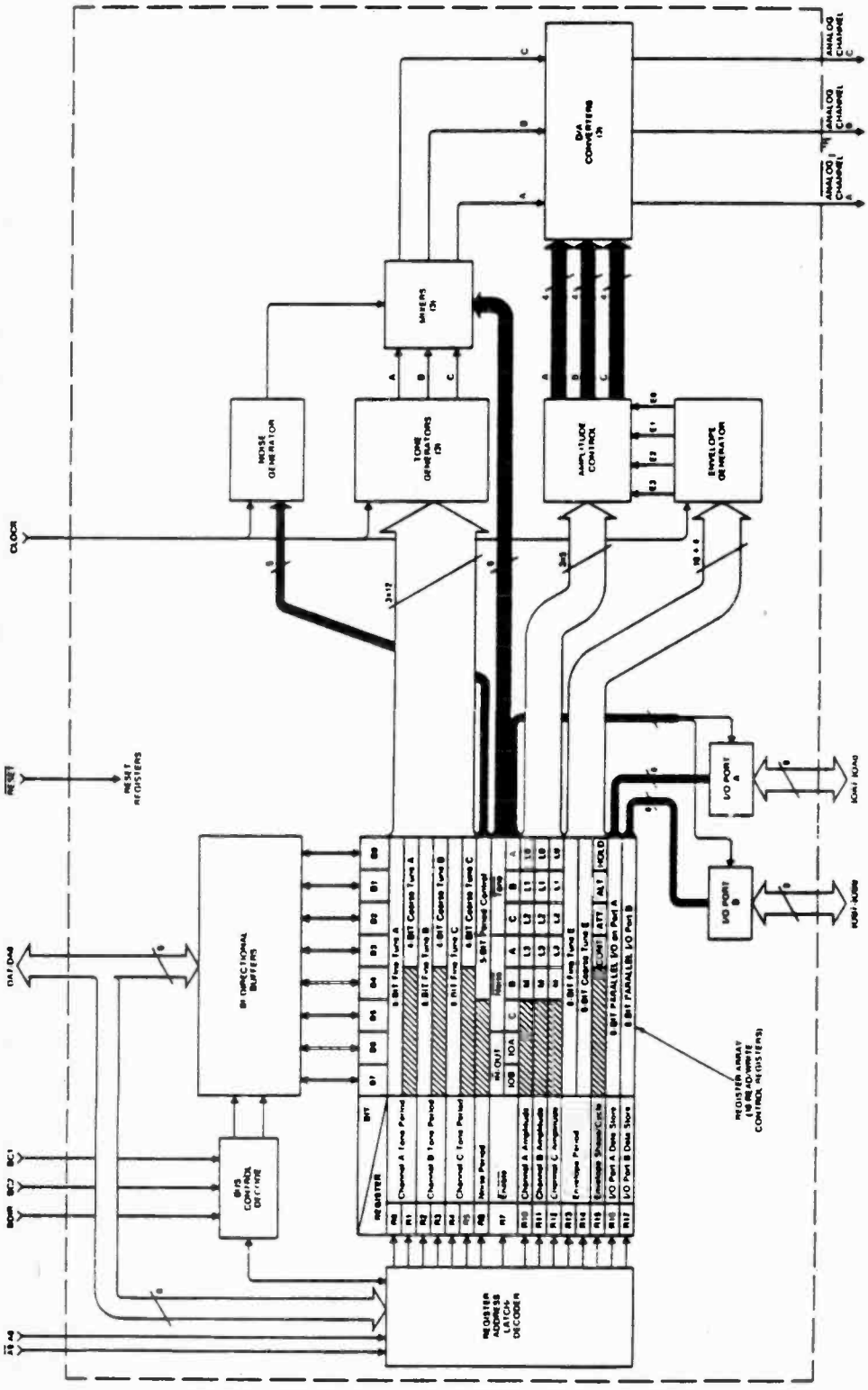
AY-3-8912A Top View



$\overline{A9}$, A8
A8 (input): Pin 25 (AY-3-8910A)
Pin 17 (AY-3-8912A)
$\overline{A9}$* (input): Pin 24 (AY-3-8910A)

High order address bits $\overline{A9}$ and A8 are fixed to recognize a "01" code. They may be left unconnected, as each is provided with either an on-chip pull-down ($\overline{A9}$) or pull-up (A8) resistor. In noisy environments, however, it is recommended that $\overline{A9}$ and A8 be tied to external ground and +5V respectively, if they are not to be used.

*This input is not available on the AY-3-8912A.


D/A CONVERTERS (3)
ANALOG CHANNEL C
ANALOG CHANNEL B
ANALOG CHANNEL A
MIXERS (3)
NOISE GENERATOR
TONE GENERATORS (3)
AMPLITUDE CONTROL
ENVELOPE GENERATOR
CLOCK
RESET
RESET REGISTERS
I/O PORT A
I/O PORT B
8 BIT DIRECTIONAL BUFFERS
BC1
BDIR
BC2
BUS CONTROL DECODE
REGISTER ARRAY (16 READ/WRITE CONTROL REGISTERS)
REGISTER ADDRESS LATCH/ DECODER

$\overline{\text{RESET}}$ (Input): Pin 23 (AY-3-8910A)
Pin 16 (AY-3-8912A)

For initialization/power-on purposes, applying a low level input to the $\overline{\text{RESET}}$ pin will reset all registers to 0_8. The $\overline{\text{RESET}}$ pin is provided with an on-chip pull-up resistor.

CLOCK (Input): Pin 22 (AY-3-8910A)
Pin 15 (AY-3-8912A)

This TTL compatible input supplies the timing reference for the Tone, Noise, and Envelope Generators.

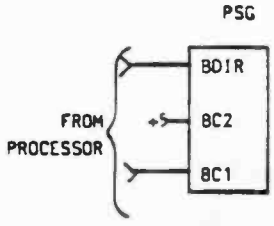
BDIR, BC2, BC1 (Inputs): Pins 27,28,29 (AY-3-8910A)
Pins 18,19,20 (AY-3-8912A)
BUS Direction, BUS Control 2, Bus Control 1

These bus control signals are generated directly by the CP1610 microprocessor to control all bus operations internal and external to the PSG.

BDIR	BC2	BC1	CP1600 FUNCTION	PSG FUNCTION
0	0	0	NACT	INACTIVE. See 010 (IAB) below.
0	0	1	ADAR	LATCH ADDRESS. See 111 (INTAK) below.
0	1	0	IAB	INACTIVE: The PSG/CPU bus is inactive. DA7-DA0 are in a high impedance state.
0	1	1	DTB	READ FROM PSG. This signal causes the contents of the register which is currently addressed to appear on the PSG/CPU bus. DA7-DA0 are in the output mode.
1	0	0	BAR	LATCH ADDRESS. See 111 (INTAK) below.
1	0	1	DW	INACTIVE. See 010 (IAB) above.
1	1	0	DWS	WRITE TO PSG. This signal indicates that the bus contains register data which should be latched into the currently addressed register. DA7--DA0 are in the input mode.
1	1	1	INTAK	LATCH ADDRESS. This signal indicates that the bus contains a register address which should be latched in the PSG. DA7--DA0 are in the input mode.

While interfacing to a processor other than the CP1600 would simply require simulating the above decoding, the redundancies in the PSG functions vs. bus control signals can be used to advantage in that only four of the eight possible decoded bus functions are required by the PSG. This could simplify the programming of the bus control signals to the following, which would only require that the processor generate two bus control signals (BDIR and BC1, with BC2 tied to +5V):

BDIR	BC2	BC1	PSG FUNCTION
0	1	0	INACTIVE.
0	1	1	READ FROM PSG.
1	1	0	WRITE TO PSG.
1	1	1	LATCH ADDRESS.



Analog Channel A, B, C (Outputs):
Pins 4,3,38(AY-3-8910A)
Pins 5,4,1 (AY-3-8912A)

Each of these signals is the output of its corresponding digital to analog converter, and provides 1V peak-peak (max) signal representing the complex sound waveshape generated by the PSG.

Pins 2,5,26,39 (AY-3-8910A), Pins 2 (AY-3-8912A)

These pins are for General Instrument test purposes only and should be left open. Do not use as tie-points.

V_{CC}: Pin 40 (AY-3-8910A), Pin 3 (AY-3-8912A)
Nominal +5 Volt power supply to the PSG.

V_{SS}: Pin 1 (AY-3-8910A), Pin 6 (AY-3-8912A)
Ground reference for the PSG.

ARCHITECTURE:

The AY-3-8910A/8912A is a register oriented Programmable Sound Generator (PSG). Communication between the processor and the PSG is based on the concept of memory-mapped I/O. Control commands are issued to the PSG by writing to 16 memory-mapped registers. Each of the 16 registers within the PSG is also readable so that the microprocessor can determine, as necessary, present states or stored data values. All functions of the PSG are controlled through the 16 registers which, once programmed, generate and sustain the sounds, thus freeing the system processor for other tasks.

REGISTER ARRAY:

The principal element of the PSG is the array of 16 read/write control registers. These 16 registers look to the CPU as a block of memory and, as such, occupy a 16 word block out of 1,024 possible addresses. The 10 address bits (8 bits on the common data/address bus, and 2 separate address bits) are decoded as follows:

$\overline{A9}$	A8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
0	1	0	0	0	0	0	0	0	0
THROUGH									
0	1	0	0	0	0	1	1	1	1
HIGH ORDER (Chip Select)						LOW ORDER (Register No.)			

The four low order address bits select one of the 16 registers ($R0-R17_8$). The six high order address bits function as chip selects to control the tri-state bidirectional buffers (when the high order address bits are incorrect, the bidirectional buffers are forced to a high impedance state). High order address bits $\overline{A9}$, A8 are fixed in the PSG design to recognize a "01" code; high order address bits DA7--DA4 are programmed to recognize only a "0000" code. All addresses are latched internally. This internally latched address is updated and modified on every latch address signal presented to the PSG via the BDIR, BC2, and BC1 inputs. A latched address will remain valid until the receipt of a new address, enabling multiple reads and writes of the same register contents without the need for redundant re-addressing.

Conditioning of the Register Address Latch/Decoder and the Bidirectional Buffers to recognize the bus function required (Inactive, Latch Address, Write Data), is accomplished by the Bus Control Decode block.

SOUND GENERATING BLOCKS:

The basic blocks in the PSG which produce the programed sounds include:

Tone Generators	Produce the basic square wave tone frequencies for each channel (A, B, C).
Noise Generator	Produces a pulse width modulated pseudo-random square wave output.
Mixers	Combine the outputs of the Tone Generators and the Noise Generator; per channel (A, B, C).
Envelope Generator	Produces an envelope pattern which can be used to amplitude modulate the output of each Mixer.
Amplitude Control	Provides the D/A Converters with either a fixed or variable amplitude pattern. Fixed amplitude is under direct CPU control. Variable amplitude is accomplished via the output of the Envelope Generator.
D/A Converters	The three D/A Converters each produce a 16 level (max) output signal as determined by the Amplitude Control.

OPERATION:

Since all PSG functions are processor controlled by writing to the internal registers, a detailed description of the PSG operation may best be accomplished by relating each PSG function to control of the corresponding register. The function of creating or programing a specific sound effect logically follows the control sequence listed:

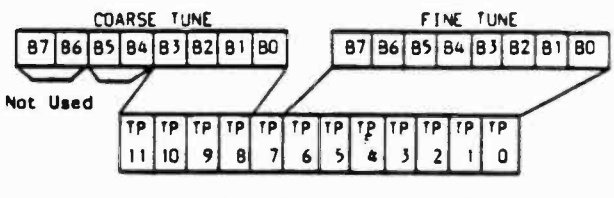
Operation	Registers	Function
Tone Generator Control	R0--R5	Program tone periods
Noise Generator Control	R6	Program noise period
Mixer Control	R7	Enable tone and/or noise on selected channels
Amplitude Control	R10-R12	Select fixed or variable (envelope) amplitudes
Envelope Generator Control	R13-R15	Program envelope period and select envelope pattern

Tone Generator Control

(Registers R0, R1, R2, R3, R4, R5)

The frequency of each square wave generated by the three Tone Generators (one each for Channels A, B, and C) is obtained by first dividing the input clock by 16 then by further dividing the result by the programed 12 bit Tone Period value. Each 12-bit tone period value is obtained by combining the contents of the respective Coarse and Fine Tune registers, as illustrated:

Coarse Tune Register	Channel	Fine Tune Register
R1	A	R0
R3	B	R2
R5	C	R4



12-bit Tone Period (TP) to Tone Generator

The period of the output of the tone generator is therefore determined by:

16 x TP x P where P = the period of the input clock.

NOTE: If the Coarse and Fine Tune registers are both set to 000_8, the resulting period will be minimum, i.e., the generated tone period will be as if the Coarse Tune register was set to 000_8 and the Fine Tune register set to 001_8.

Noise Generator Control

(Register R6)

The frequency of the noise source is obtained by dividing the input clock by 16, then by further dividing the result by the programed 5 bit Noise Period value. This 5 bit value consists of the lower 5 bits (B4--B0) of register R6, as illustrated:

Noise Period
Register R6

Not Used 5-bit Noise Period (NP) to Noise Generator

Mixer Control - I/O Enable

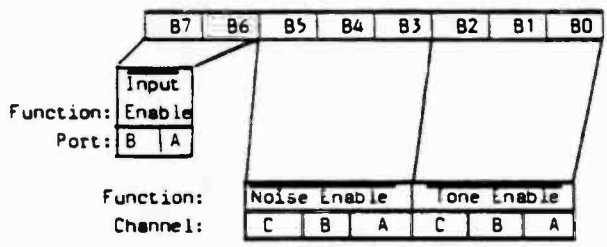
(Register R7)

Register R7 is a multi-function $\overline{\text{ENABLE}}$ register which controls the three Noise/Tone Mixers.

The Mixers, as previously described, combine the noise and tone frequencies for each of the three channels. The determination of combining neither/either/both noise and tone frequencies on each channel is made by the state of bits B5--B0 of register R7, as illustrated.

The direction (input or output) of the general purpose I/O ports (I/OA and I/OB) is determined by the state of bits B7 and B6 of R7, as illustrated.

MIXER CONTROL REGISTER - R7



NOISE ENABLE TRUTH TABLE

R7 Bits B5	B4	B2	Noise Enabled on Channel
0	0	0	C B A
0	0	1	C B -
0	1	0	C - A
0	1	1	C - -
1	0	0	- B A
1	0	1	- B -
1	1	0	- - A
1	1	1	- - -

TONE ENABLE TRUTH TABLE

R7 Bits B2	B1	B0	Tone Enabled on Channel
0	0	0	C B A
0	0	1	C B -
0	1	0	C - A
0	1	1	C - -
1	0	0	- B A
1	0	1	- B -
1	1	0	- - A
1	1	1	- - -

I/O PORT TRUTH TABLE

R7 Bits B7	B6	I/O Port Status I/OB	I/OA
0	0	Input	Input
0	1	Input	Output
1	0	Output	Input
1	1	Output	Output

NOTE: Disabling noise and tone does not turn off a channel. Turning a channel off can only be accomplished by writing all zeros into the corresponding Amplitude Control Register.

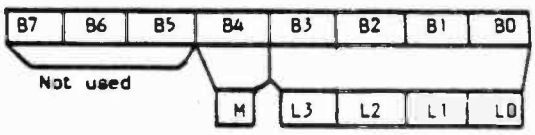
Amplitude Control

(Registers R10, R11, R12)

The amplitude of the signals generated by each of the three D/A Converters (one each for Channels A, B, and C) is determined by the content of the lowers bits (B4-B0) of registers R10, R11, and R12 as illustrated.

These five bits consist of a 1-bit mode select ("M" bit) and a 4-bit "fixed" amplitude level (L3-L0). When the M bit is low, the output level of the analog channel is defined by the 4-bit "fixed" amplitude level of the Amplitude Control Register. This amplitude level is fixed in the sense that the amplitude level is under direct control of the system processor. When the M bit is high, the output level of the analog channel is defined by the 4-bits of the Envelope Generator (bits E3-E0). The amplitude mode bit can also be thought of as an "envelope enable" bit.

Amplitude Control Register	Channel
R10	A
R11	B
R12	C



Amplitude Mode	4 bit fixed Amplitude Level	
0	0 0 0 0	Amplitude Defined By L0-L3
'	' ' '	
'	' ' '	
'	' ' '	
0	1 1 1 1	
1	X X X X	Amplitude Defined By E0-E3

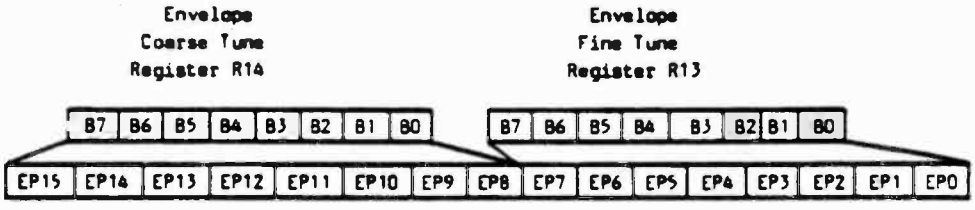
ENVELOPE GENERATOR CONTROL

To accomplish the generation of complex envelope patterns, two independent methods of control are provided: first, it is possible to vary the frequency of the envelope using registers R13 and R14; second, the relative shape and cycle pattern of the envelope can be varied using register R15. The following paragraphs explain the details of the envelope control functions, describing first the envelope period control and then the envelope shape/cycle control. (See Figure 1 and 2).

ENVELOPE PERIOD CONTROL

(Registers R13, R14)

The frequency of the envelope is obtained by first dividing the input clock by 256, then by further dividing the result by the programmed 16 bit Envelope Period value. This 16 bit value is obtained by combining the contents of the Envelope Coarse and Fine Tune registers, as illustrated:



16-bit Envelope Period (EP) to Envelope Generator
Thus the envelope period is given by:
256 x EP x P Where P = period of input clock

NOTE: If the Coarse and Fine Tune registers are both set to 000_8, the resulting period will be minimum, i.e., the generated tone period will be as if the Coarse Tune register was set to 000_8 and the Fine Tune register set to 001_8.

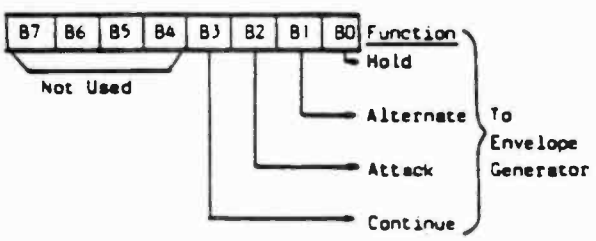
ENVELOPE SHAPE/CYCLE CONTROL

(Register R15)

The Envelope Generator further divides the envelope period by 16, producing a 16-state per cycle envelope pattern as defined by the 4-bit counter output, E3, E2, E1 and E0. The particular shape and cycle pattern of any desired envelope is accomplished by controlling the count pattern of the 4-bit counter. (See Figure 4 and 5).

This envelope shape/cycle control is contained in the lower 4 bits (B3--B0) of register R15. Each of these 4 bits controls a function in the envelope generator, as illustrated:

Envelope Shape/Cycle
Control Register (R15)



Bit 0: HOLD — When this is set high (logic 1) the envelope is limited to one cycle, the value of the envelope at the end of the cycle being held.

Bit 1: ALTERNATE — When set high (logic 1) the envelope counter reverses direction at end of each cycle (i.e. performs as an up/down counter).

Bit 2: ATTACK — When set high (logic 1) the envelope counter will count up (attack). When set low (logic 0) the counter will count down (decay).

Bit 3: CONTINUE — When set high (logic 1) the cycle pattern will be defined by the HOLD bit. When set low (logic 0) the envelope counter will reset to 0000 after one cycle, and hold that value.

D/A CONVERTER OPERATION

Since the primary use of the PSG is to produce sound for the non-linear amplitude detection mechanism of the human ear, the D/A conversion is performed in logarithmic steps with a normalized voltage range from 0 to 1 volt. The specific amplitude control of each of the three D/A Converters is accomplished by the three sets of 4 bit outputs of the Amplitude Control block, while the Mixer outputs provide the base signal frequency (Noise and/or Tone). (See Fig. 3).

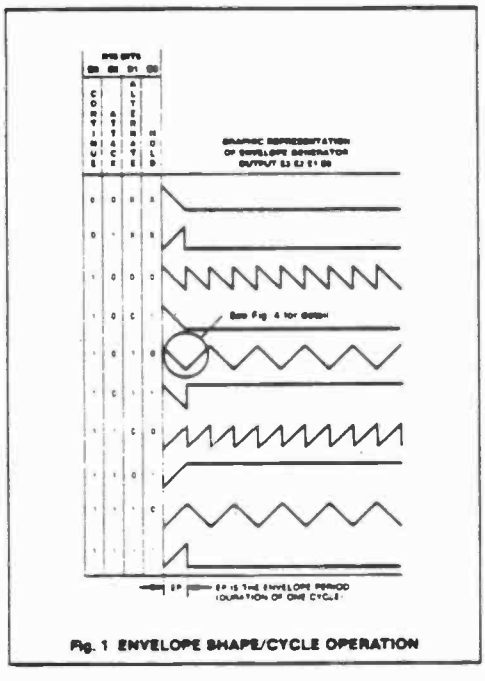


Fig. 1 ENVELOPE SHAPE/CYCLE OPERATION

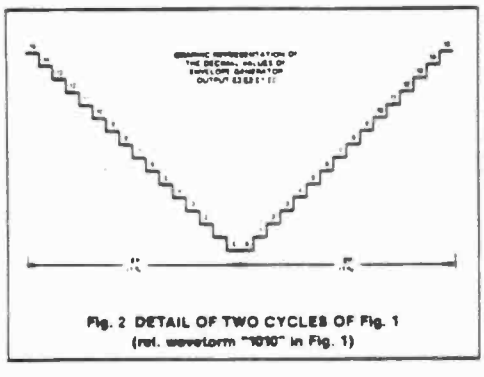


Fig. 2 DETAIL OF TWO CYCLES OF Fig. 1
(ref. waveform "1010" in Fig. 1)

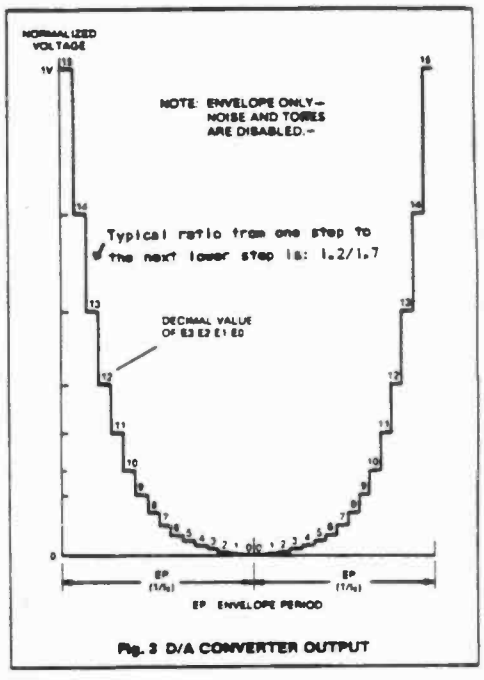


Fig. 3 D/A CONVERTER OUTPUT

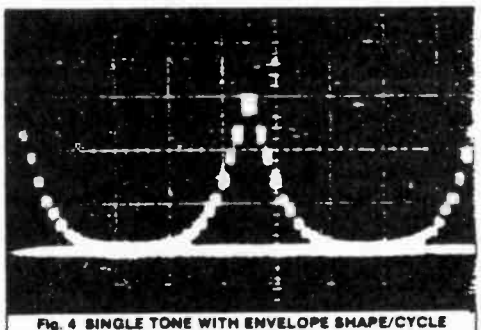


Fig. 4 SINGLE TONE WITH ENVELOPE SHAPE/CYCLE PATTERN 1010

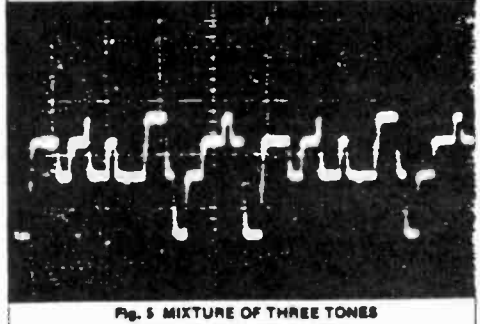


Fig. 5 MIXTURE OF THREE TONES WITH FIXED AMPLITUDES

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Storage Temperature..... -55°C to +150°C
Operating Temperature..... 0°C to +70°C
V_{CC} and all other Input/Output Voltages with Respect to V_{SS}.... -0.3V to +8.0V

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied--operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (Unless otherwise noted)

V_{CC} = +5V ± 5%
V_{SS} = GND
Operating Temperature = 0°C to +70°C

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ**	Max	Units	Conditions
All Inputs						
Low Level	V_{IL}	-0.2	-	0.8	V	
High Level	V_{IH}	2.2	-	V_{CC}	V	
Data Bus (DA7...DA0) Output Levels						
Low Level	V_{OL}	0	-	0.4	V	I_{OL} = 1.6mA, 150pF
High Level	V_{OH}	2.4	-	V_{CC}	V	I_{OH} = 100µA, 150pF
Data Bus (DA7...DA0)						
Input Leakage	I_{IAL}	-10	-	10	µA	V_{IN} = 0.4V to V_{CC}
Analog Channel Outputs						
Output Volume	Vo	0	-	60	dB	Test Circuit: Fig. 6
Power Supply Current	I_{CC}	-	70	90	mA	
I/O Ports						
Pull Up Current Low	I_{IL}	20	-	200	µA	V_{IN} = 0.4V, Outputs disabled
Pull Up Current High	I_{IH}	10	-	100	µA	V_{IN} = 3.5V
As Outputs (A7-A0, B7-B0)						
Low Level	V_{OL}	0	-	0.5	V	I_{IL} = 1.6mA
High Level	V_{OHh}	3.5	-	V_{CC}	V	I_{OHh} = -10µA See
	V_{OHl}	2.4	-	V_{CC}	V	I_{OHl} = 85µA Note 1
As Inputs (A7-A0, B7-B0)						
Low Level	V_{IL}	0	-	0.8	V	
High Level	V_{IH}	2.4	-	V_{CC}	V	
A8 and Reset Input						
Pullup Current	I_{ILpu}	-10	-	-100	µA	V_{IN} = 0.4V
	I_{IHpu}	-10	-	-50	µA	V_{IN} = 2.4V
$\overline{A9}$						
Pull down Current	I_{IHpd}	10	-	100	µA	V_{IN} = 2.4V
BC1,BDIR, Clock Inputs						
Input Leakage	I_{ICL}	-10	-	10	µA	V_{IN} = 0.4V to V_{CC}
Analog Outputs						
Max. Current (per channel)	-	0.4	2.0	-	mA	V_{OUT} = 0.7V, Amplitude Control Set To F

**Typical values are at +25°C and nominal voltages.

NOTE 1:
The active pull-up during an output operation will achieve a logic 1 of 2.4 volts in a time of typically 1 microsecond. However, from 2.4 volts to the high level of 3.5 volts the available pull up current will reduce significantly and further edge transition will be highly dependent upon load capacitance.

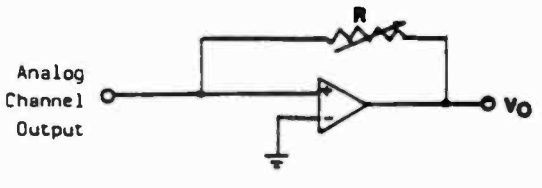
ELECTRICAL CHARACTERISTICS (continued...)

AC CHARACTERISTICS

Characteristics	Sym	Min	Typ**	Max	Units	Conditions
Clock Input						F_C
Frequency	f_c	1	-	2	MHz	
Rise Time	t_r	-	-	50	ns	Fig. 7
Fall Time	t_f	-	-	50	ns	
Duty Cycle	-	40	50	60	%	
Bus Signals (BDIR, BC2, BC1)						
Associative Delay Time	t_{BD}	-	-	40	ns	
$\overline{\text{Reset}}$						
Reset Pulse Width	t_{RW}	500	-	-	ns	Fig. 8
$\overline{A9}$, A8, DA7..DA0 (Address Mode)						
Address Setup Time	t_{AS}	300	-	-	ns	
Address Hold Time	t_{AH}	65	-	-	ns	Fig. 9
DA7...DA0 (Write Mode)						
Write Data Pulse Width	t_{DW}	500	-	10,000	ns	
Write Data Setup Time	t_{DS}	300	-	-	ns	Fig. 10
Write Data Hold Time	t_{DH}	65	-	-	ns	
DA7...DA0 (Read Mode)						
Data Access Time from DTB	t_{DA}	-	-	200	ns	Fig. 11
DA7...DA0 (Inactive Mode)						
Tri-state Delay Time from DTB	t_{TS}	-	-	100	ns	
I/O Ports (A7-A0, B7-B0)						
Pull-Up Recovery Time	t_{PN}	-	-	50	usec	V_{OH} = 3.5V C_{LOAD} = 100pf See Note 2

**Typical values are at +25°c and nominal voltages

NOTE 2:
Pull-up recovery time is defined as the time required for any I/O pin A7-A0 or B7-B0 to change up to a 100pf capacitor load from 0.0 volts to 3.5 volts. This recovery time is conditional on the output function of Port A or Port B being deselected via Bits B7 and B6 of register R10.

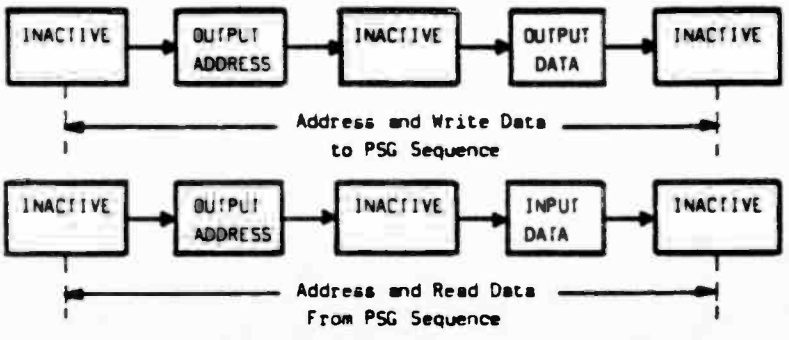


(OP AMP Must Not Saturate)

Fig. 6 ANALOG CHANNEL OUTPUT TEST CIRCUIT

STATE TIMING

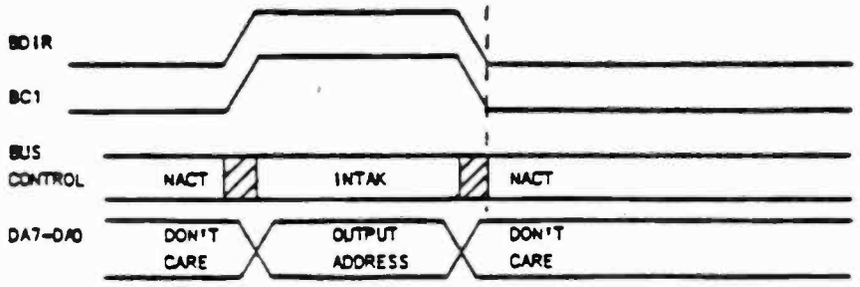
While the state flow for many microprocessors can be somewhat involved for certain operations, the sequence of events necessary to control the PSG is simple and straightforward. Each of the three major state sequences (Latch Address, Write to PSG, and Read from PSG) consists of several operations (indicated below by rectangular blocks), defined by the pattern of bus control signals (BDIR, $\overline{BC1}$).



The functional operation and relative timing of the PSG control sequences are described in the following paragraphs.

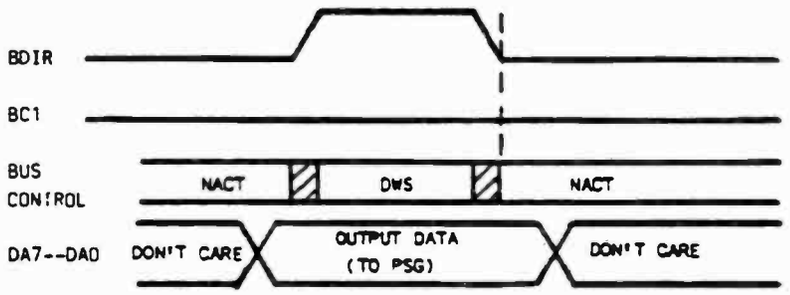
ADDRESS PSG REGISTER SEQUENCE

The Latch Address sequence is normally an integral part of the write or read sequences, but for simplicity is illustrated here as in individual sequence. Depending upon the processor used, the program sequence will normally require four principal microstates: (1) send NACT (inactive); (2) send INTAK (latch address); (3) put address on bus; (4) send NACT (inactive).



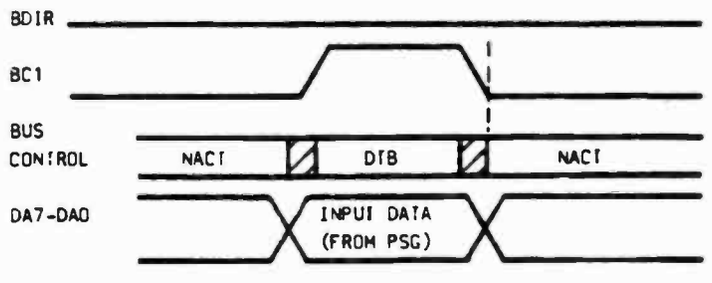
WRITE DATA TO PSG SEQUENCE

The Write to PSG sequence, which would normally follow immediately after an address sequence, requires four principal microstates: (1) send NACT (inactive); (2) put data on bus; (3) send DWS (write to PSG); (4) send NACT (inactive).



READ DATA FROM PSG SEQUENCE

As with the Write to PSG sequence, the Read from PSG sequence would also normally follow immediately after an address sequence. The four principal microstates of the read sequence are: (1) send NACT (inactive); (2) send DTB (read from PSG); (3) read data on bus; (4) send NACT (inactive).



TIMING DIAGRAMS

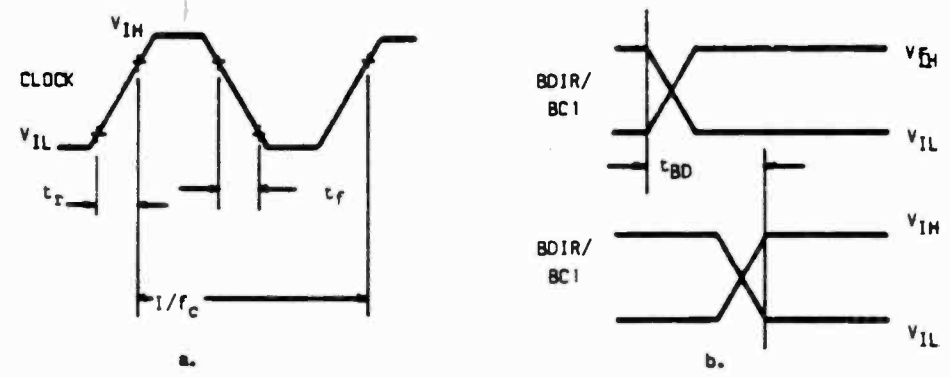


Fig. 7 CLOCK AND BUS SIGNAL TIMING

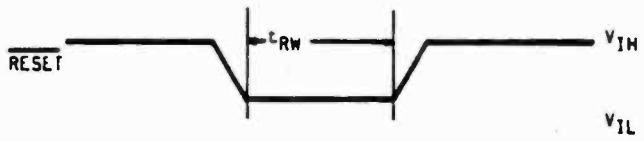


FIG. 8 RESET TIMING

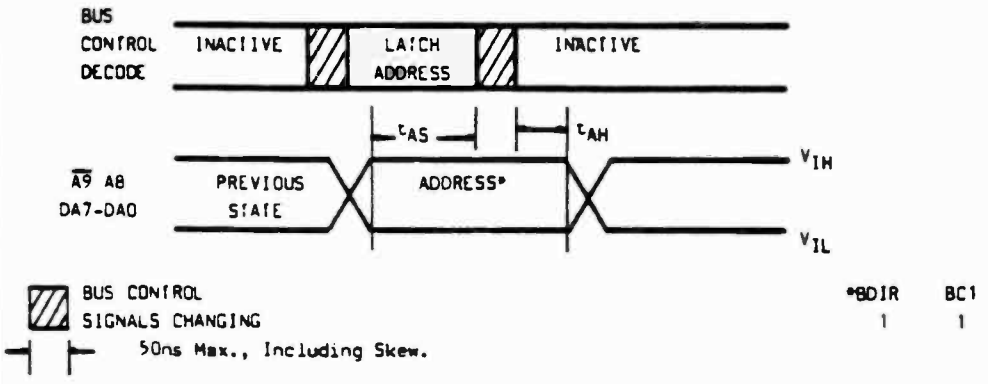


Fig. 9 LATCH ADDRESS TIMING

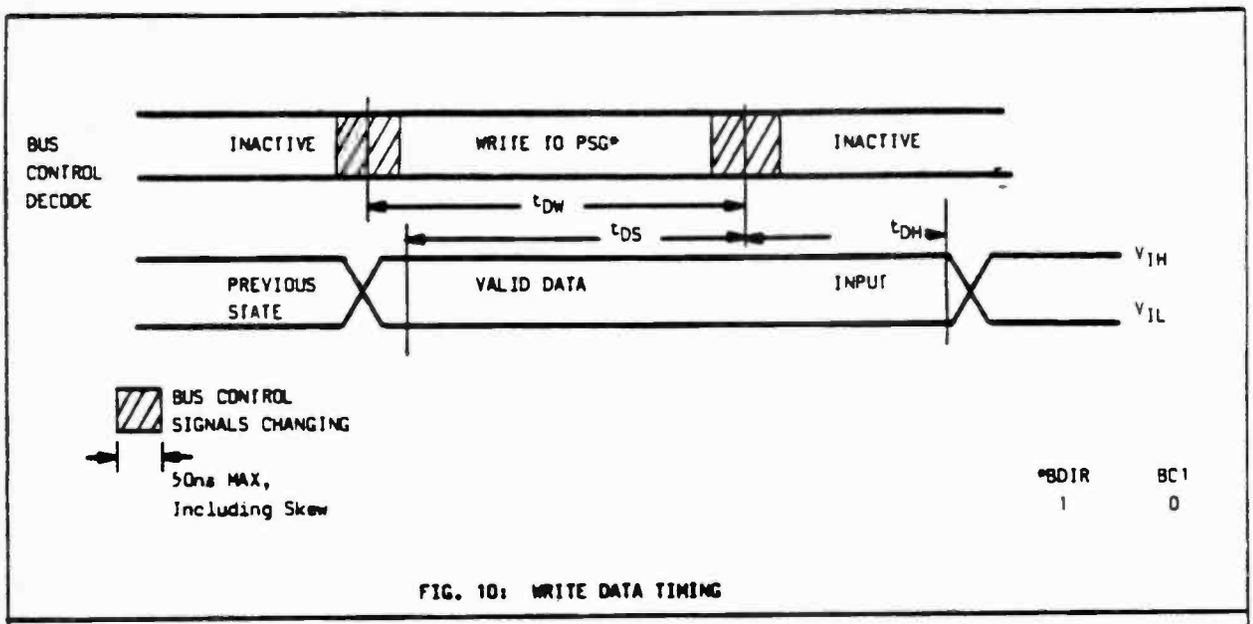


FIG. 10: WRITE DATA TIMING

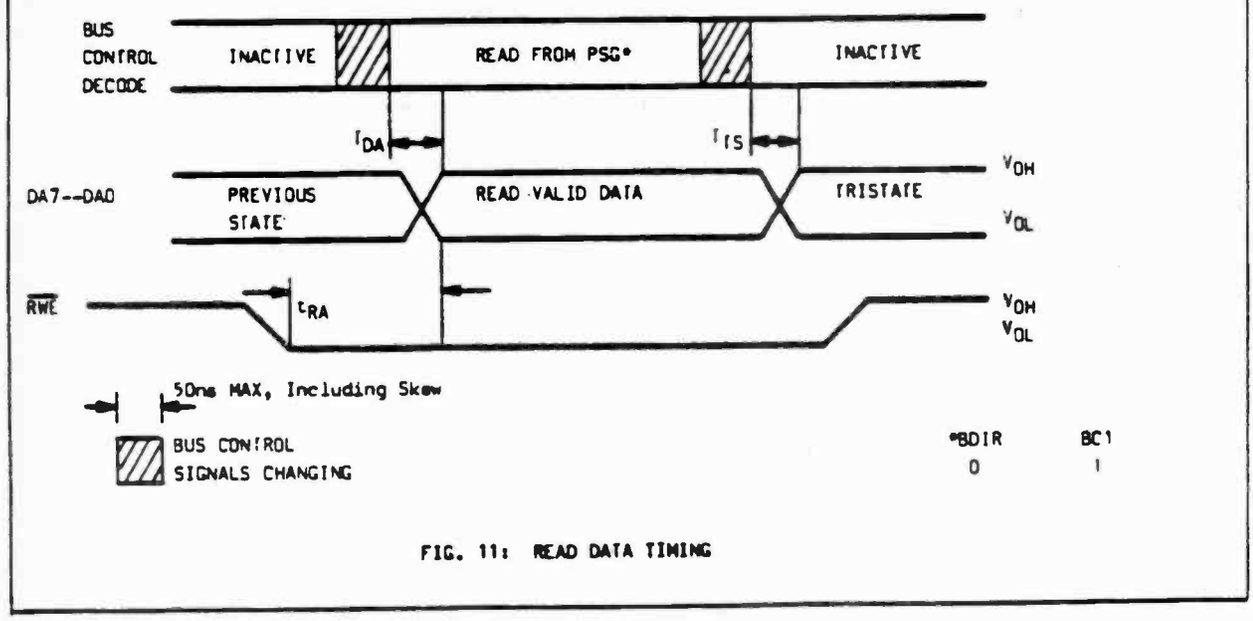


FIG. 11: READ DATA TIMING

FAIRCHILD
A Schlumberger Company

Programmable Counter/Timer

Description

The μA2240 Programmable Timer/Counter is a monolithic controller capable of producing accurate microsecond to five day time delays. Long delays, up to three years, can easily be generated by cascading two timers. The timer consists of a time-base oscillator, programmable 8-bit counter and control flip-flop. An external resistor capacitor (RC) network sets the oscillator frequency and allows delay times from 1 RC to 255 RC to be selected. In the astable mode of operation, 255 frequencies or pulse patterns can be generated from a single RC network. These frequencies or pulse patterns can also easily be synchronized to an external signal. The trigger, reset and outputs are all TTL and DTL compatible for easy interface with digital systems. The timer's high accuracy and versatility in producing a wide range of time delays makes it ideal as a direct replacement for mechanical or electromechanical devices.

- **Accurate Timing From Microseconds To Days**
- **Programmable Delays From 1 RC To 255 RC**
- **TTL, DTL And CMOS Compatible Outputs**
- **Timing Directly Proportional To RC Time Constant**
- **High Accuracy**
- **External Sync And Modulation Capability**
- **Wide Supply Voltage Range**
- **Excellent Supply Voltage Rejection**

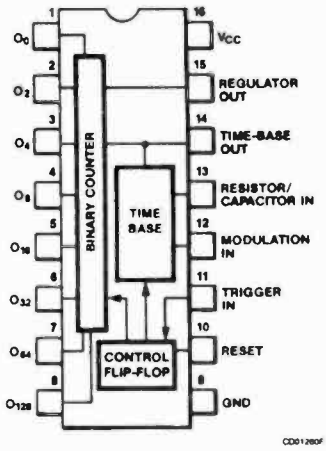
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	0°C to 70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
16L-Ceramic DIP	1.50 W
16L-Molded DIP	1.04 W
Supply Voltage	18 V
Output Current	10 mA
Output Voltage	18 V
Regulator Output Current	5.0 mA

Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Ceramic DIP at 10 mW/°C, and the 16L-Molded DIP at 8.3 mW/°C.

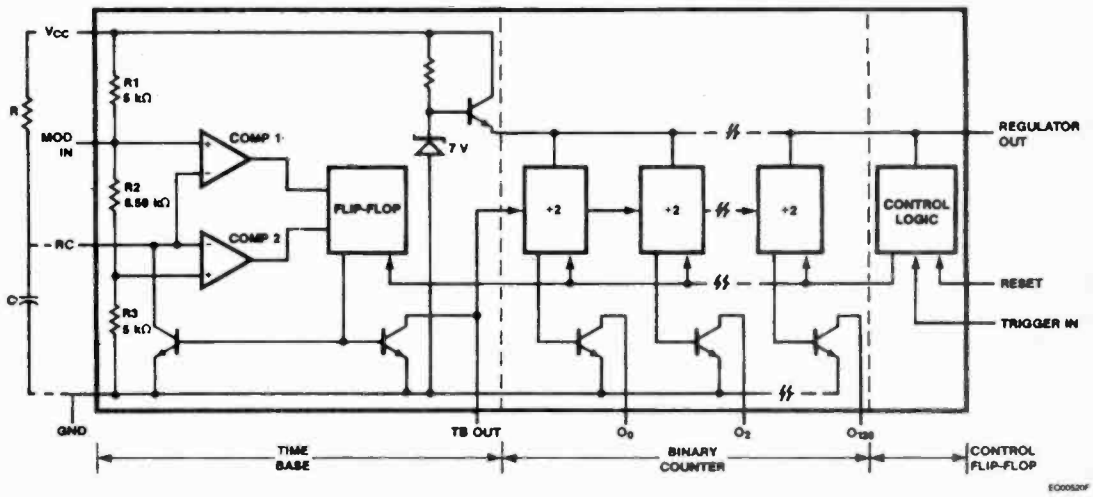
Connection Diagram 16-Lead DIP (Top View)



Order Information

Device Code	Package Code	Package Description
μA2240DC	7B	Ceramic DIP
μA2240PC	9B	Molded DIP

Block Diagram



Data supplied by Fairchild Semiconductor Ltd.

Functional Description

(*Figure 1* and Block Diagram)
When power is applied to the μA2240 with no trigger or reset inputs, the circuit starts with all outputs HIGH. Application of a positive going trigger pulse to trigger lead 11, initiates the timing cycle. The trigger input activates the time-base oscillator, enables the counter section and sets the counter outputs LOW. The time-base oscillator generates timing pulses with a period T = 1 RC. These clock pulses are counted by the binary counter section. The timing sequence is completed when a positive going reset pulse is applied to Reset, lead 10.

Once triggered, the circuit is immune from additional trigger inputs until the timing cycle is completed or a reset input is applied. If both the reset and trigger are activated simultaneously, the trigger takes precedence.

Figure 2 gives the timing sequence of output waveforms at various circuit terminals, subsequent to a trigger input. When the circuit is in a reset state, both the time-base and the counter sections are disabled and all the counter outputs are HIGH.

Figure 1 Logic Symbol

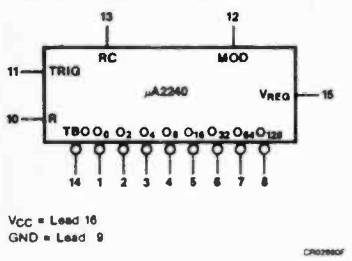
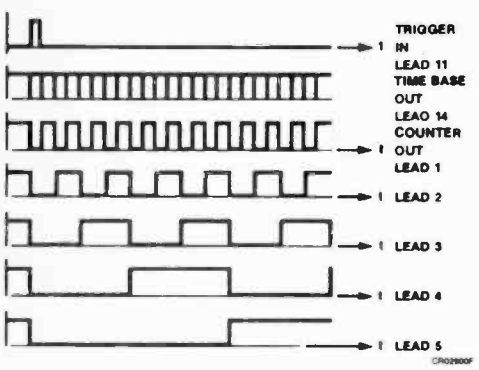


Figure 2 Timing Diagram of Output Waveforms



In most timing applications, one or more of the counter outputs are connected to the reset terminal with S1 closed (*Figure 3*). The circuit starts timing when a trigger is applied and automatically resets itself to complete the timing cycle when a programmed count is completed. If none of the counter outputs are connected back to the reset terminal (switch S1 open), the circuit operates in an astable or free running mode, following a trigger input.

Important Operating Information

Ground connection is lead 9.

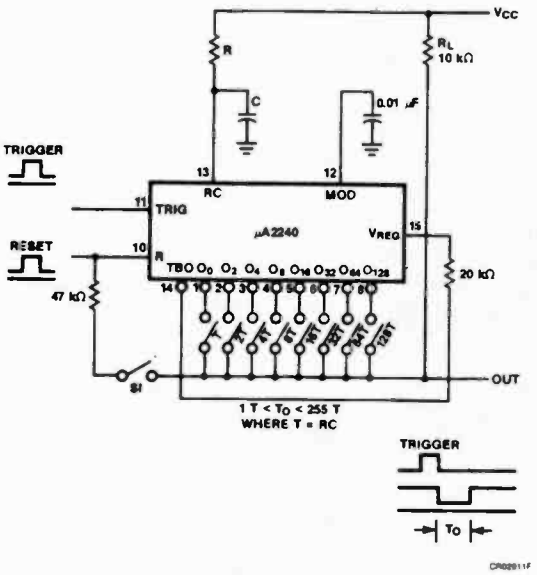
Reset (R) (lead 10) sets all outputs HIGH.

Trigger (TRIG) (lead 11) sets all outputs LOW.

Time-base output (TBO) (lead 14) can be disabled by bringing the RC Input (lead 13) LOW via a 1.0 kΩ resistor.

Normal TBO (lead 14) is a negative going pulse greater than 500 ns.

Figure 3 Basic Circuit Connection for Timing Applications
Monostable: S1 Closed
Astable: S1 Open



Note: Under the conditions of high supply voltages ($V_{CC} > 7.0$ V) and low values of timing capacitor ($C_T < 0.1\mu F$), the pulse width of TBO may be too narrow to trigger the counter section. This can be corrected by connecting a 600 pF capacitor from TBO (lead 14) to ground (lead 9).

Reset (lead 10) stops the time-base oscillator.

Outputs ($O_0 \ldots O_{128}$) (leads 1 – 8) sink 2.0 mA current with $V_{OL} \leq 0.4$ V.

For use with external clock, minimum clock pulse amplitude should be 3.0 V, with greater than 1.0 μs pulse duration.

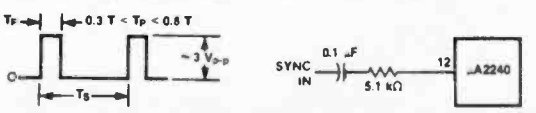
Circuit Controls

Counter Outputs ($O_0 \ldots O_{128}$, leads 1 thru 8)
The binary counter outputs are buffered open collector type stages, as shown in the block diagram. Each output is capable of sinking 2.0 mA at 0.4 V V_{OL}. In the reset condition, all the counter outputs are HIGH or in the non-conducting state. Following a trigger input, the outputs change state in accordance with the timing diagram of *Figure 2*. The counter outputs can be used individually, or can be connected together in a wired-OR configuration, as described in the programming segment of this data sheet.

Reset and Trigger Inputs (R and TRIG, 10 and 11)
The circuit is reset or triggered with positive going control pulses applied to leads 10 and 11 respectively. The threshold level for these controls is approximately two diode drops (≈ 1.4 V) above ground. Minimum pulse widths for reset and trigger inputs are shown in the Performance Curves. Once triggered, the circuit is immune to additional trigger inputs until the end of the timing cycle.

Modulation and Sync Input (MOD, lead 12)
The oscillator time-base period (T) can be modulated by applying a DC voltage to MOD, lead 12 (see Performance Curves). The time-base oscillator can be synchronized to an external clock by applying a sync pulse to MOD, lead 12, as shown in *Figure 4*. Recommended sync pulse widths and amplitudes are also given.

Figure 4 Operation with External Sync Signal



The time-base can be synchronized by setting T to be an integer multiple of the sync pulse period (T_S). This can be done by choosing the timing components R and C at lead 13 such that:

$$T = RC = (T_S/m)$$

where:

m is an integer, $1.0 \leq m \leq 10$

Figure 5 gives the typical pull-in range for harmonic synchronization for various values of harmonic modulus, m. For $m < 10$, typical pull-in range is greater than ±4% of time-base frequency.

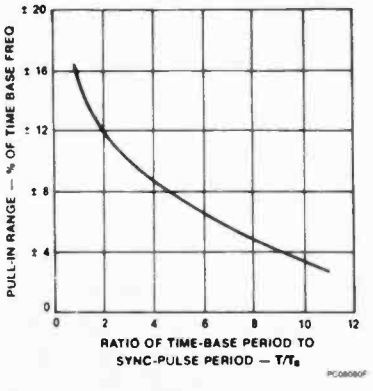
RC Terminal (lead 13)
The time-base period T is determined by the external RC network connected to RC, lead 13. When the time-base is triggered, the waveform at lead 13 is an exponential ramp with a period T = 1 RC.

Time-Base Output (TBO, lead 14)
The time-base output is an open-collector type stage as shown in the block diagram, and requires a 20 kΩ pull-up resistor to lead 15 for proper circuit operation. In the reset state, the time-base output is HIGH. After triggering, it produces a negative going pulse train with a period T = RC, as shown in the diagram of *Figure 2*. The time-base output is internally connected to the binary counter section and can also serve as the input for the external clock signal when the circuit is operated with an external time base. The counter section triggers on the negative going edge of the timing or clock pulses generated at TBO, lead 14. The trigger threshold for the counter section is ≈ +1.4 V. The counter section can be disabled by clamping the voltage level at lead 14 to ground.

When using high supply voltages ($V_{CC} > 7.0$ V) and a small value timing capacitor ($C_T < 0.1$ μF), the pulse width at TBO lead 14 may be too narrow to trigger the counter section. This can be corrected by connecting a 600 pF capacitor from lead 14 to ground.

Regular Output (V_{REG}, lead 15)
The regulator output V_{REG} is used internally to drive the binary counter and the control logic. This terminal can also be used as a supply to additional μA2240 circuits when several timer circuits are cascaded *(see Figure 6)* to minimize power dissipation. For circuit operation with an external clock, V_{REG} can be used as the V_{CC} input terminal to power down the internal time-base and reduce power dissipation. When supply voltages less than 4.5 V are used with the internal time-base, lead 15 should be shorted to lead 16.

Figure 5 Typical Pull-in Range for Harmonic Synchronization



Monostable Operation

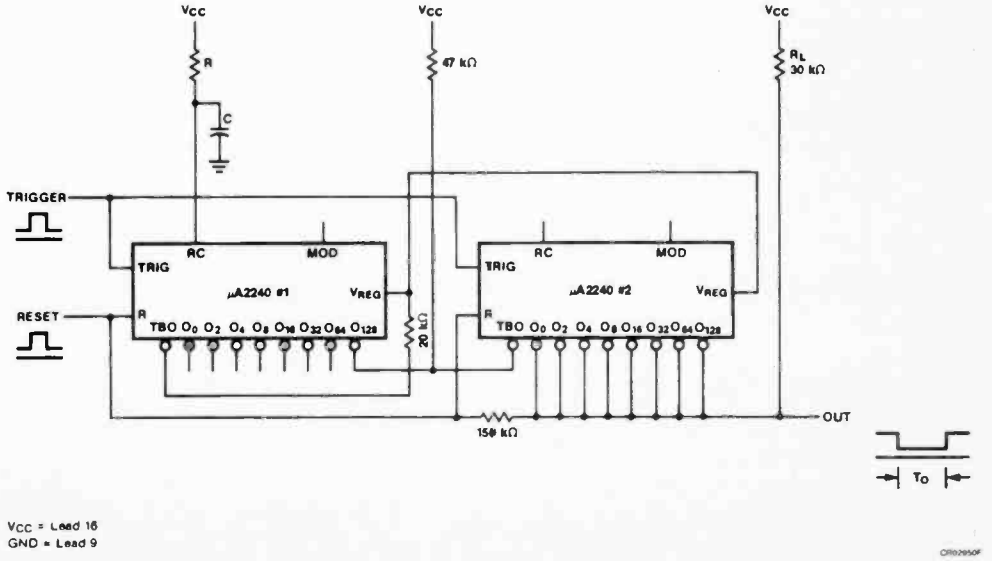
Precision Timing
In precision timing applications, the μA2240 is used in its monostable or self-resetting mode. The generalized circuit connection for this application is shown in *Figure 3*. The output is normally HIGH and goes LOW following a trigger input. It remains LOW for the time duration (T_O) and then returns to the HIGH state. The duration of the timing cycle T_O is given as:

$$T_O = nT = NRC$$

where T = RC is the time-base period as set by the choice of timing components at RC lead 13 (see Performance Curves) and n is an integer in the range of $1 \leq n \leq 255$ as determined by the combination of counter outputs ($O_0 \ldots O_{128}$), leads 1 through 8, connected to the output bus.

Counter Output Programming
The binary counter outputs, $O_0 \ldots O_{128}$, leads 1 through 8 are open collector type stages and can be shorted together to a common pull-up resistor to form a wired-OR connection; the combined output will be LOW as long as any one of the outputs is LOW. The time delays associated with each counter output can be added together. This is done by simply shorting the outputs together to form a common output bus as shown in *Figure 3*. For example, if only lead 6 is connected to the output and the rest left open, the total duration of the timing cycle, T_O, is 32 T. Similarly, if leads 1, 5, and 6 are shorted to the output bus, the total time delay is $T_O = (1 + 16 + 32)$ T = 49 T. In this manner, by proper choice of counter terminals connected to the output bus, the timing cycle can be programmed to be $1 T \leq T_O \leq 255$ T.

Figure 6 Low Power Operation of Cascaded Timers



Vcc = Lead 16
GND = Lead 9

Ultra Long Time Delay Application

Two μA2240 units can be cascaded as shown in *Figure 7* to generate extremely long time delays. Total timing cycle of two cascaded units can be programmed from $T_O = 256$ RC to $T_O = 65{,}536$ RC in 256 discrete steps by selectively shorting one or more of the counter outputs from Unit 2 to the output bus. In this application, the reset and the trigger terminals of both units are tied together and the Unit 2 time base is disabled. Normally, the output is HIGH when the system is reset. On triggering, the output goes LOW where it remains for a total of $(256)^2$ or 65,536 cycles of the time-base oscillator.

In cascaded operation, the time-base section of Unit 2 can be powered down to reduce power consumption by using the circuit connection of *Figure 6*. In this case, the V_{CC} terminal (lead 16) of Unit 2 is left open, and the second unit is powered from the regulator output of Unit 1 by connecting the V_{REG} (lead 15) of both units together.

Astable Operation

The μA2240 can be operated in its astable or free running mode by disconnecting the reset terminal (lead 10) from the counter outputs. Two typical circuits are shown in *Figures 8* and *9*. The circuit in *Figure 8* operates in its free running mode with external trigger and reset signals. It starts counting and timing following a trigger input until an external reset pulse is applied. Upon application of a positive going reset signal to lead 10, the circuit reverts back to its reset state. This circuit is essentially the same as that of *Figure 3* with the feedback switch S1 open.

The circuit of *Figure 9* is designed for continuous operation. It self triggers automatically when the power supply is turned on, and continues to operate in its free running mode indefinitely. In astable or free running operation, each of the counter outputs can be used individually as synchronized oscillators, or they can be interconnected to generate complex pulse patterns.

Binary Pattern Generation

In astable operation, as shown in *Figure 8*, the output of the μA2240 appears as a complex pulse pattern. The waveform of the output pulse train can be determined directly from the timing diagram of *Figure 2* which shows the phase relations between the counter outputs. *Figures 10* and *11* show some of the complex pulse patterns that can be generated. The pulse pattern repeats itself at a rate equal to the period of the highest counter bit connected to the common output bus. The minimum pulse width contained in the pulse train is determined by the lowest counter bit connected to the output.

Figure 8 Operation with Trigger and Reset Inputs (Note 1)

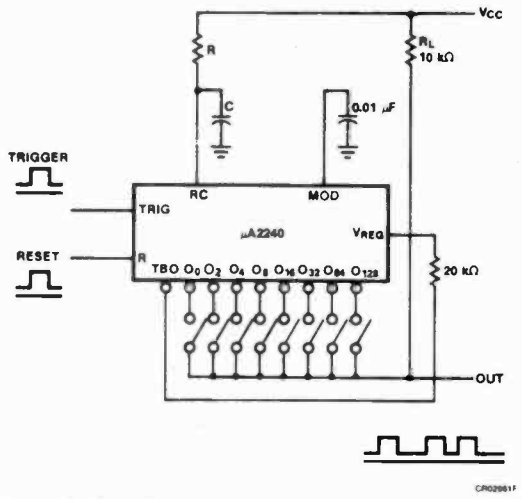


Figure 9 Free Running or Continuous Operation (Note 1)

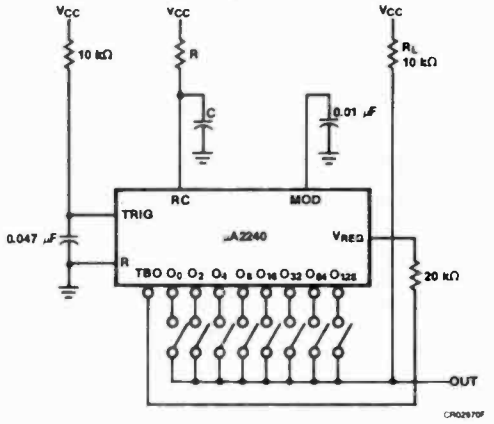
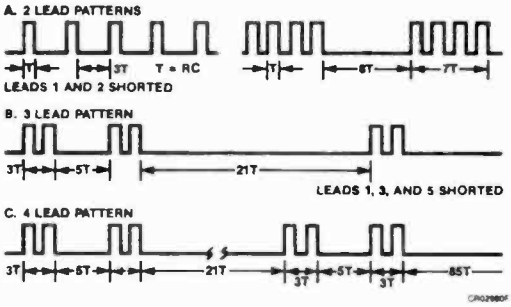


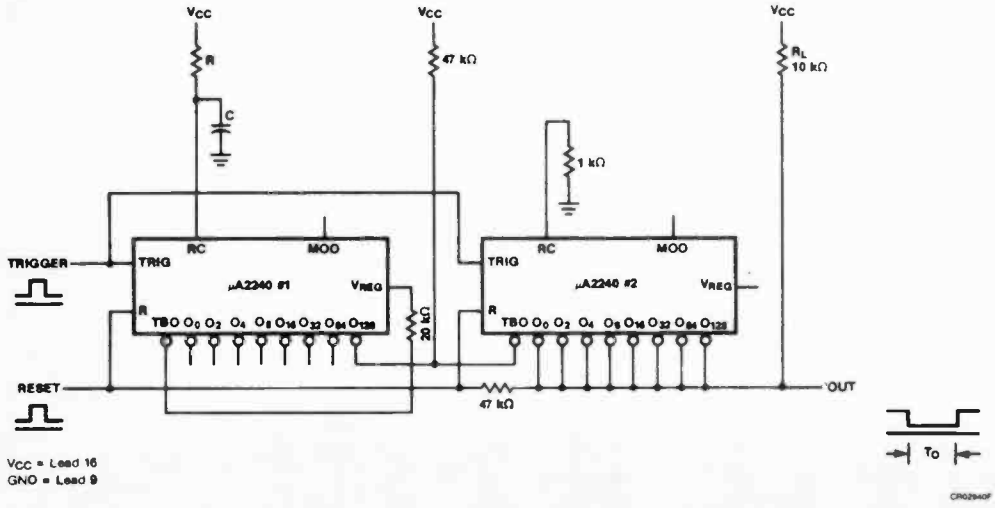
Figure 10 Binary Pulse Patterns Obtained by Shorting Various Counter Outputs



Note

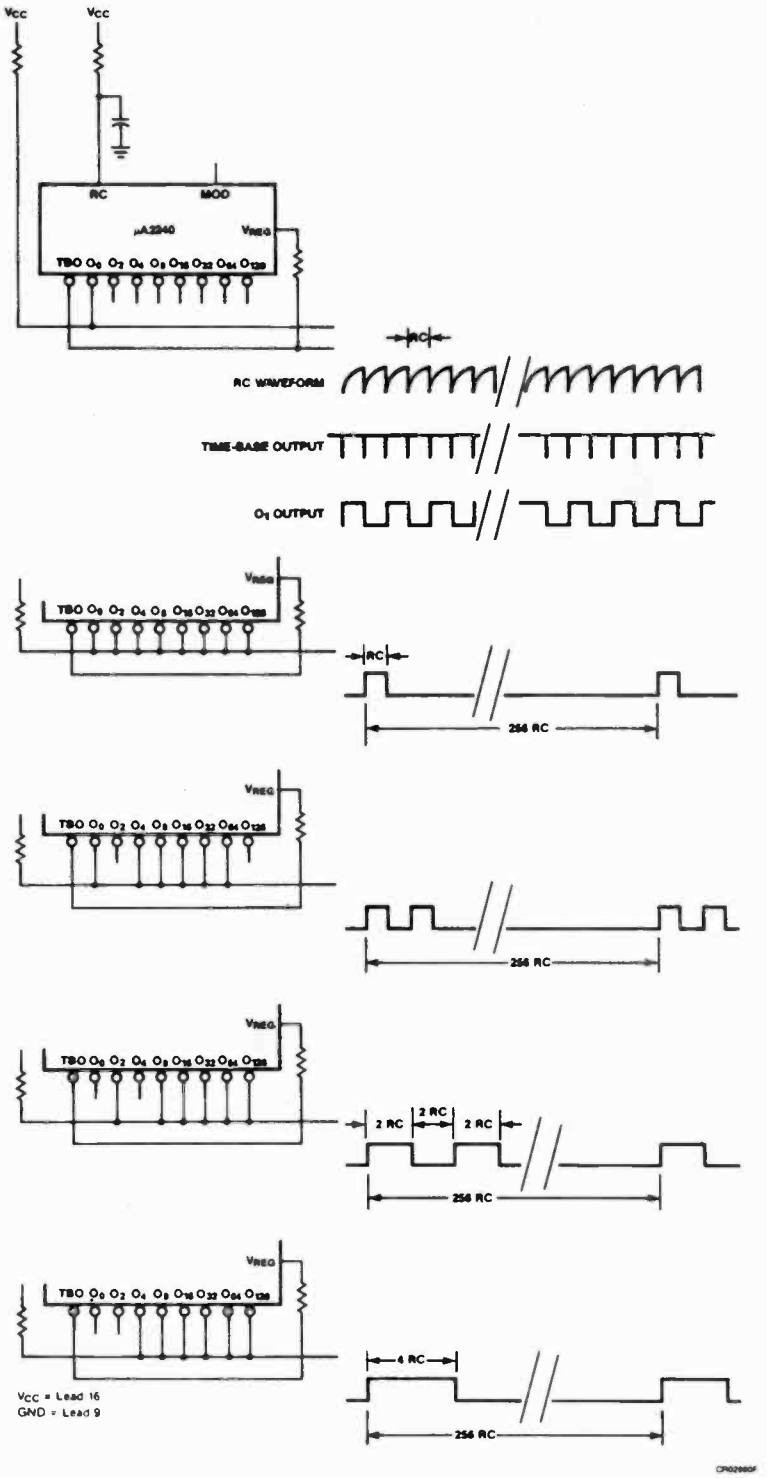
1. V_{CC} = Lead 16
   GND = Lead 9

Figure 7 Cascaded Operation for Long Delays



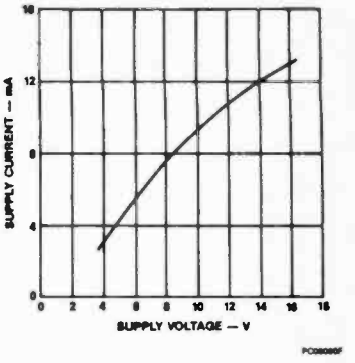
Vcc = Lead 16
GND = Lead 9

Figure 11 Continuous Free run Operation Examples of Output

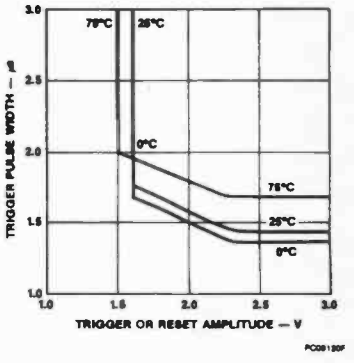


Typical Performance Curves

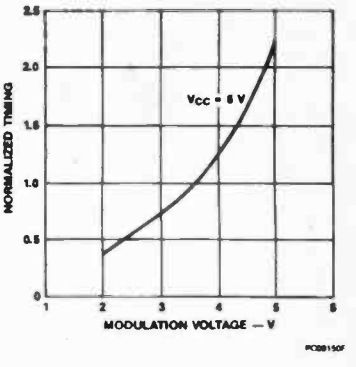
Supply Current vs Supply Voltage in Reset Condition



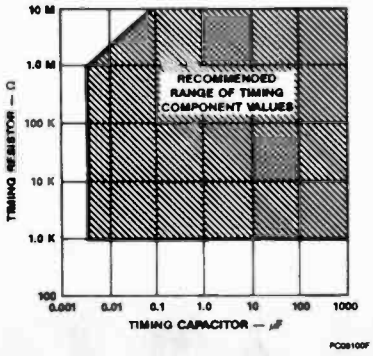
Minimum Trigger Pulse Width vs Trigger and Reset Amplitude



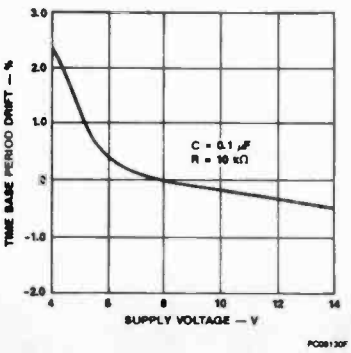
Normalized Change in Time-Base Period vs Modulation Voltage



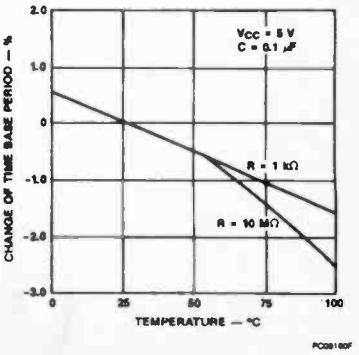
Recommended Range of Timing Component Values



Time-Base Period Drift vs Supply Voltage



Time-Base Period vs Temperature



Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0$ V, $R = 10$ kΩ, $C = 0.1$ μF, unless otherwise specified.

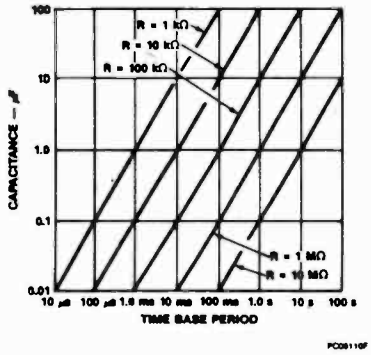
Symbol	Characteristic		Condition		Min	Typ	Max	Unit
General Characteristic								
V_{CC}	Supply Voltage		For $V_{CC} \leq 4.5$ V, Short Lead 15 to Lead 16		4.0		15	V
I_{CC}	Supply Current	Total Circuit	$V_{CC} = 5.0$ V, $V_{TR} = 0$ V, $V_{RS} = 5.0$ V			4.0	7.0	mA
			$V_{CC} = 15$ V, $V_{TR} = 0$ V, $V_{RS} = 5.0$ V			13	18	
		Counter Only				1.5		
V_{REG}	Regulator Output		Measured at Lead 15	$V_{CC} = 5.0$ V	3.9	4.4		V
				$V_{CC} = 15$ V	5.8	6.3	6.8	
Time-Base								
t_{ACC}	Timing Accuracy[1]		$V_{RS} = 0$, $V_{TR} = 5.0$ V			3.5	5.0	%
$\Delta t/\Delta T$	Temperature Drift		$0°C \leq T_J \leq 75°C$	$V_{CC} = 5.0$ V		200		ppm/°C
				$V_{CC} = 15$ V		80		
$\Delta t/\Delta V$	Supply Drift		$V_{CC} \geq 8.0$ V (See Performance Curves)			0.08	0.3	%/V
f_{Max}	Max Frequency		$R = 1.0$ kΩ, $C = 0.007$ μF			130		kHz
V_{MOD}	Modulation Voltage Level		Measured at Lead 12	$V_{CC} = 5.0$ V	2.80	3.50	4.20	V
				$V_{CC} = 15$ V		10.5		
R_T	Recommended Range of Timing Components Timing Resistor		(See Performance Curves)		0.001		10	MΩ

Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0$ V, $R = 10$ kΩ, $C = 0.1$ μF, unless otherwise specified.

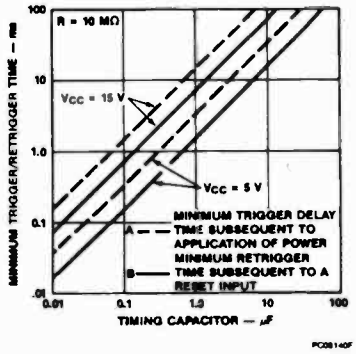
Symbol	Characteristic	Condition	Min	Typ	Max	Unit
C_T	Timing Capacitor		0.01		1000	μF
Trigger/Reset Controls						
V_{TR}	Trigger Threshold	Measured at Lead 11, $V_{RS} = 0$ V		1.4	2.0	V
I_{TR}	Trigger Current	$V_{RS} = 0$ V, $V_{TR} = 2.0$ V		10		μA
Z_T	Trigger Impedance			25		kΩ
t_{RSPT}	Trigger Response Time[2]			1.0		μs
V_{RS}	Reset Threshold	Measured at Lead 10, $V_{TR} = 0$ V		1.4	2.0	V
I_R	Reset Current	$V_{TR} = 0$ V, $V_{RS} = 2.0$ V		10		μA
Z_R	Reset Impedance			25		kΩ
t_{RSPT}	Reset Response Time[2]			0.8		μs
Counter						
TR_{Max}	Max Toggle Rate	Measured at Lead 14, $V_{RS} = 0$ V, $V_{TR} = 5.0$ V		1.5		MHz
Z_I	Input Impedance			20		kΩ
V_{TH}	Input Threshold		1.0	1.4		V
t_r	Output Rise Time	Measured at Leads 1 through 8, $R_L = 3.0$ kΩ, $C_L = 10$ pF		180		ns
t_f	Fall Time			180		
I_{O-}	Sink Current	$V_{OL} \leq 0.4$ V	2.0	4.0		mA
I_{CEX}	Leakage Current	$V_{OH} = 15$ V		0.01	15	μA

Notes
1. Timing error solely introduced by μA2240 measured as % of ideal time-base period of T=RC.
2. Propagation delay from application of trigger (or reset) input to corresponding change of state in counter output at lead 1.

Time-Base Period vs External RC



Minimum Trigger/Retrigger Timing vs Timing Capacitor



Time-Base Period vs Temperature