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"To promote the advancement of radio, electronics and kindred subjects by the exchange of information in these branches of engineering."

THE RADIO AND ELECTRONIC ENGINEER

The Journal of the Institution of Electronic and Radio Engineers

VOLUME 37 No. 4 APRIL 1969

Making the Journal More Useful

TO the pure scientist, confined to furthering knowledge of the fundamentals of his chosen subject, the final step in each investigation is to present his new experimental results, ideas and understanding in the form of a paper. The subject matter of that given branch of science may therefore be mastered by studying the contents of the academic literature. For the engineer, however, the final step is to describe the specific hardware which he has created. Can one then hope to master that particular branch of engineering by a study of the literature? Of course not. If one wishes to become familiar with present-day electronic engineering practice, one is likely to learn much more from a visit to a manufacturer, or failing that by examination of the firm's products, than from a visit to the library.

How then can one further this *Journal's* aims within the limitations of mere written words, equations and diagrams? To be frank, there are many practising engineers who hold that 'learned journals' of the professional institutions, particularly in electronics, are far removed from the real business of the engineer—and may do a positive disservice to the profession. A frequent target for criticism is the undue prominence of abstract mathematical argument. This tends to rob sound engineering of both credit and importance by giving the impression that 'engineering' matters, *per se*, are not suitable subjects for papers. Much of the published theoretical work, because it is based on assumptions which do not accord with practical realities, could indeed be highly misleading to any practising engineer who took it seriously. Now it is not the purpose of this editorial to seek out the causes of this state of affairs, but rather to suggest remedies. Nonetheless, it is regrettably true that a university lecturer in electronics, in search of promotion, is at present better advised to contribute academic calculations to the journals than to try to make a success of the design and development of an actual engineering product. This in turn has a detrimental effect on the departmental teaching and research.

To return to the matter of remedies, in recent months the Institution has been re-assessing the function of the *Journal*. One of the earlier results of this work was the recommendation by the Papers Committee that the *Journal* should feature more papers of the 'interpretive' type.† Paper type apart, we have now decided how we should assess future papers as to their suitability for inclusion in the *Journal*. The present selection criteria of originality and quality of presentation will still be very relevant. Besides these we intend to judge every future contribution on the basis of how immediately useful it will be to the practising engineer. In this way we hope that we can increase the interest of the *Journal*, while maintaining its intellectual standard at the level appropriate to that of the graduate electronic engineer. This means, for example, that we still expect prospective authors to be well-informed, self-critical, and to strive for absolute scientific integrity.

In future then we hope to attract *Journal* contributions (however short) which will be characterized not least by their timeliness and intrinsic usefulness. The encouragement is extended to the authors of all those different categories, or types, of paper enumerated in previous statements. This should enable the *Journal* to enhance its usefulness as the authoritative source of the best current thought and practice in the field of electronic engineering.

E. A. FAULKNER
E. ROBINSON

† 'Papers for the practising designer', *The Radio and Electronic Engineer*, **36**, No. 1, p. 3, July 1968.

INSTITUTION NOTICES

Student and Graduate Fees

The Council of the Institution has decided that as from 1st April 1969 no entry fee will be charged to applicants for Student or Graduate membership.

Furthermore, students in full-time courses for a first degree or post-graduate award, or in a course leading towards a professional qualification (such as the Higher National Diploma which exempts from Part 1 of the C.E.I. Examination), will now only pay an annual subscription of £1. To obtain this concession a certificate, obtainable from the Institution, must be completed by the applicant and signed by a responsible member of a teaching establishment.

The Council hopes that these steps will enable students and younger engineers still under training to join in Institution activities to the benefit of their own careers and to the industry in which ultimately they will work.

Measurement Education

The Institution of Electrical Engineers, together with the I.E.R.E., the I.P.P.S., the Institute of Mathematics and its Applications and the Institute of Measurement and Control, is organizing a conference on Measurement Education, to be held at the University of Warwick from 8th to 10th July 1969.

The Conference will discuss the need for measurement education courses and their content and method of presentation at various levels of education. All aspects of measurement will be covered, but particular emphasis will be given to:

Measurement in British industry; measurement education—present practice; proposals for improvement of measurement education.

Further details and registration forms are available from the I.E.E., Savoy Place, London, W.C.2.

Florey Memorial Appeal

The Councils of the Royal Society and the Australian National University have decided to commemorate the late Lord Florey, President of the Royal Society from 1960 to 1965 and Chancellor of the Australian National University from 1965 until his death on 21st February 1968, by establishing a memorial fund to be used for visiting research fellowships in the biomedical sciences between Australia and the United Kingdom to be known as Florey Fellowships.

The minimum capital sum required is £150,000—one half from the United Kingdom and one half from Australia—and it is hoped that the appeal will meet with a generous response. Donations may be sent to The Royal Society (Florey Fund), at 6 Carlton House Terrace, London, S.W.1, from which further particulars of the appeal can be obtained.

Earth Station Technology

The Institution of Electrical Engineers and the I.E.R.E. are co-sponsoring an international conference on Earth Station Technology for Satellite Communications to be held in London during October 1970. The effect of using higher frequencies and different modulation methods in future systems will be discussed, and it is hoped that the programme will also include: the Earth segment/space segment interface and resulting Earth station performance requirements; Earth station configuration; Earth station aerials; servo control systems; aerial feed and tracking systems; low-noise amplifiers; frequency conversion equipment; and modems.

Further details will be available shortly from the I.E.E.

Current Control Theory

This year the University of Warwick, with the support of the Science Research Council, the Nuffield Foundation and Shell International Petroleum, is bringing a number of distinguished workers in control theory to Britain. An Exposition on Current Control Theory is to be held at the University from 7th to 11th July, 1969, to enable European control engineers and mathematicians to hear state-of-the-art lectures from world authorities. It will be organized by the I.E.E., in association with the Institute of Mathematics and its Applications, and the I.E.R.E. As well as formal lectures and informal discussions on subjects related to this field, a report will be given of the I.F.A.C. Congress in Warsaw.

Further information may be obtained from the Control and Automation Division of the I.E.E., Savoy Place, London, W.C.2.

The Radio and Electronic Engineer

The circulation of *The Radio and Electronic Engineer* continues to rise steadily. The Audit Bureau of Circulations (ABC) figure for July to December 1968 gives an average certified circulation of 13 731 copies a month. This compares with 13 154 copies a month for the period January to June 1968.

In 'An Evaluation of British Scientific Journals' recently published by Aslib it is concluded, on the hypothesis that citation of a document indicates use of the document, that the bulk of useful scientific information is contained in a relatively small number of journals. Over 95% of citations were to 165 of the 1842 British journals considered. *The Radio and Electronic Engineer* is among these 165 journals and is, therefore, in the top 9% of the most quoted scientific publications.

U.D.C. 621.376.56:621.396.65

The Use of Pulse Code Modulation for Point-to-Point Music Transmission

By

E. R. ROUT, C.Eng., M.I.E.E.†

AND

A. H. JONES, B.Sc.†

Presented at a meeting of the Institution's Communications Group held in London on 17th October, 1968.

Summary: The advent of pulse code modulation (p.c.m.) techniques heralds the possibility of extremely reliable and completely distortionless distribution and processing of audio signals. In this paper, the basic requirements for audio circuits of broadcast quality are reviewed, and the specification of a p.c.m. system satisfying these requirements is developed. Means for reducing the required number of digits, without sacrificing quality, are considered.

The use of p.c.m. as a means of distributing sound signals for radio must await the availability of p.c.m. circuits of sufficient capacity. However, the links already in use for video signal distribution are of sufficient bandwidth for p.c.m. sound, and the idea of combining the sound signal with the accompanying video signal as a means of television programme distribution is very attractive. A short description is given of a method of composite sound and vision distribution by means of pulse code modulated sound inserted into the 625-line television waveform during sync pulse periods.

Finally, the feasibility of a widespread adoption of p.c.m. within studio centres is examined, and prospects for digital mixing, recording and artificial reverberation are considered.

1. The Progress of Electrical Communication

1.1. *Historical*

The first attempts to use electric currents as a means of communication between distant points were made at a time when the apparatus for generating and detecting electricity was comparatively crude. Thus systems relying on simple 'on/off' codes, such as the Morse code and the railway telegraph code, were devised; both of these techniques are still in use today because of their ability to maintain communication even under adverse conditions. The desirability of reproducing the human voice at a distance was quickly realized, and was achieved with the invention of the carbon microphone and the earphone. A long battle between the engineer and the impairment inherent in analogue audio processes then commenced.

During the past fifty years a vast amount of skill and money has been absorbed in developing more and more refined apparatus, and we are now able to come close to the goal of faithful reproduction, but at a very considerable price. The analogue systems on which we depend are subject to variations, distortions and spurious signals, which can only be kept at bay by expensive equipment, carefully designed and maintained transmission paths and an army of operators, maintenance men and engineers.

The principal requirements of an analogue system which necessitate this costly human intervention are:

(i) flat response/frequency characteristic
(ii) high signal/noise ratio
(iii) linear relationship between the input to the system and its output
(iv) constant attenuation between input and output
(v) reasonably low dispersion.

1.2. *Modern Concepts in Communications*

In more recent years, workers in the theoretical fields have tried to analyse and understand the fundamental principles of communication. One of the most important contributions was made by Shannon,[1] who evolved equations enabling the theoretical capabilities of a transmission channel to be evaluated in terms of its information carrying capacity, and thereby defined the minimum requirements for a transmission circuit capable of conveying a given flow of information.

One of Shannon's equations states that the information contained within a given signal is approximately given by the bandwidth which it occupies multiplied

† British Broadcasting Corporation, Research Department, Kingswood Warren, Tadworth, Surrey.

by the signal/noise ratio expressed in logarithmic terms. (This statement assumes that the signal is appreciably greater than the noise, that the signal and the noise have sufficiently random amplitude distributions and similar spectral distributions, and that the signal/noise ratio is calculated in terms of mean signal and noise powers.) It follows that if the signal is encoded so as to occupy M times its original bandwidth, it can, by suitable coding, be transmitted through a channel whose signal/noise ratio in decibels is $1/M$ times that required at the output of the decoder. Therefore, if a circuit has a bandwidth which exceeds that of the analogue information it is required to convey, then the effective signal/noise ratio of that circuit can be greatly improved by dispersing the information over the broader spectrum.

Another contributor in this field was Nyquist[2] who showed that analogue information which is inherently represented by a continuous function can be correctly represented by a number of discrete samples.† If the number of samples per second is equal to or greater than twice the bandwidth in cycles per second occupied by the analogue signal, then the original information is preserved in the sampled signal.

In 1938, Reeves devised a practical transmission system which made use of the theoretical concepts described by Nyquist. He conceived the idea of representing each Nyquist sample by a binary number, and transmitting these binary numbers in the form of groups of pulses, the presence or absence of a pulse indicating the state of each binary digit. Reeves called his system 'pulse code modulation'.[4,5] The minimum bandwidth required by pulse code modulation is equal to the original analogue bandwidth multiplied by the number of pulses used to describe each sample.

Although at first sight it seems extravagant to use many pulses of identical height instead of one pulse of variable height, this apparently extravagant use of bandwidth is, in fact, the strength of pulse code modulation. By forcing the signal to occupy a larger bandwidth Reeves was, in effect, making use of Shannon's theory to provide a form of signal coding which can tolerate very high noise levels. At the receiving end of a transmission system using pulse code modulation the message can be correctly decoded so long as the presence or absence of each pulse can be correctly established; only a peak noise level greater than half the magnitude of the transmitted pulses can cause errors.

The groups of pulses forming a p.c.m. signal can be stored and delayed by simple devices and it is thus possible to convert a wide-band p.c.m. signal carried by a single channel into a number of lower bandwidth signals each carried by a separate channel. This flexibility allows available circuits to be used efficiently and is frequently used in tape-recording digital data.

In addition to the virtue of resistance to impairment a pulse code modulation signal can easily be repaired or regenerated en route. A simple circuit containing a threshold detector and a pulse generator can reconstruct a 'clean' version of the original signal which is in all practical respects as good as new. Thus the use of pulse code modulation with its inherent ruggedness and easy regeneration enables the quality of the decoded signal to be made independent of the characteristics of the transmission channel. It is then only necessary to ensure that the original coding process describes the given analogue signal in sufficient detail to satisfy the requirements of the recipient.

2. Parameters of a P.C.M. Audio System

The basic parameters of a p.c.m. system for music transmission can be determined from the required audio bandwidth and signal/noise ratio. It is generally accepted that the upper limit of the audio band should lie between 12 and 15 kHz, and that the ratio of peak-to-peak signal to r.m.s. (unweighted) white noise should be greater than 78 dB.

In Section 1 it was pointed out that a minimum sampling frequency of twice the analogue bandwidth is essential if the received signal is to be free of distortion. This is a theoretical figure, and in practice a somewhat higher ratio of sampling-frequency to bandwidth is necessary in order to allow for the limitations of practical filters. In terms of practical audio frequency filters the required ratio is about 2·3 and the sampling frequency corresponding to a bandwidth of 15 kHz is thus about 35 kHz.

In a p.c.m. system the effective signal/noise ratio is determined by the number of signal levels that can be described. Since each level is described by a number, it is necessary to ensure that a sufficient choice of discrete numbers, each identifying one signal level, is available in the coding equipment. If n binary digits are used, the number of levels that can be described is given by 2^n. In general, the signal samples will not have magnitudes exactly equal to one of the levels that can be described. The nearest permissible level is therefore selected. If the waveform of the input signal is sufficiently complicated, the errors thus introduced change in an arbitrary way from sample to sample, and in effect, add to the original signal a spurious signal which is very similar to white noise. The magnitude of this so-called 'quantizing noise' is decreased when the number of available levels is increased. Thus the required output signal/noise ratio

† This theorem, although commonly attributed to Nyquist, has been stated by several authors, the first of whom appears to have been Cauchy.[3]

specifies the minimum number of signal levels which must be described by a p.c.m. system.

The number of quantizing levels corresponding to the desirable signal/noise ratio of 78 dB is in excess of 2000, and thus a straightforward p.c.m. system for audio signals should employ at least 11 digits to describe each sample.† The use of well-established artifices such as pre- and de-emphasis and companding can improve the effective signal/noise ratio for a given number of digits, or permit the number of digits to be reduced for the same signal/noise ratio. However, these techniques must be applied with discretion in order to avoid undesirable side effects. The converters whose operation will be described in Section 4 were intended to be used in conjunction with a companding system.

The previous arguments have established typical sampling rates and number of digits per sample. Taking a sampling rate of 35 000 per second and 11 digits per sample, 385 000 bits per second result. The maximum rate at which the digital signal can vary occurs when successive bits take the form 1 0 1 0 1 0 etc. In order to convey this information, the fundamental spectral component, at least, of the bit stream must be preserved. This means that to convey 385 kbits per second one needs a channel bandwidth of at least 192·5 kHz; note however that the ruggedness of p.c.m. permits a level of distortion and interference which would render that circuit unusable for analogue signals. So long as the p.c.m. signals are regenerated before the accumulated noise and distortion prevent correct detection of 0s and 1s, the wanted information will be unimpaired by transmission. If this condition is satisfied the quality of the audio signal recovered at the receiving terminal will depend only on the parameters of the p.c.m. system and the performance of the terminal equipment. The terminal equipment, in particular the analogue-to-digital and digital-to-analogue converters, must fully satisfy all the requirements for good performance listed in Section 1.1.

3. Choice of Suitable Principles for Analogue-to-Digital Converters and Digital-to-Analogue Converters

Analogue-to-digital converters (a.d.c.) and digital-to-analogue converters (d.a.c.) having sufficient speed and accuracy to satisfy the basic requirements of audio signals are commercially available at the present time. However, these devices are primarily intended to handle data, and in so doing to preserve absolute accuracy. The aim of the designer is therefore to retain the precision of the converter throughout the whole range of operation, the precision of each level being important in absolute terms.

The specialized nature of an audio signal permits relaxation of the a.d.c. and d.a.c. specification in some respects but demands tighter control in others. The audio signal is tolerant of inequalities which result in small gain errors, and of slow drifts which add spurious signals at sub-audio frequencies. On the other hand audio signals cannot tolerate arbitrary errors between consecutive quantum levels, but demand a smooth or monotonic transfer characteristic. For these reasons the counter type of converter is most appropriate for audio signals, its transfer characteristic being primarily determined by the size and shape of a voltage ramp. Although the slope and absolute level of the ramp are subject to instrumental errors, these errors will not adversely affect the quality of the audio signal. At the same time the intrinsic monotonicity of the ramp can give the required freedom from distortion.

It is worth noting that because the number of signal levels available in a p.c.m. system is finite, care should be taken to avoid 'over modulation' or severe distortion will result. In practice, it is prudent to allow a little headroom and, as a further precaution, a limiter similar to those fitted to broadcasting transmitters can be provided at the input to the a.d.c.

4. Instrumentation of A.D.C.s and D.A.C.s

Figure 1 gives a functional block diagram of an a.d.c. that uses the counter principle. Its operation is controlled by a sequencer unit initiated by trigger pulses at sampling rate.

First a sample taken from the input signal is applied to one side of a voltage comparator unit. A clock pulse generator is then connected to a binary counter (here shown having 10 stages), which begins to count up from zero. The first clock pulse counted initiates the rise of the voltage ramp applied to the other side of the comparator. The voltage at which the ramp begins corresponds to the maximum negative signal excursion. When the ramp voltage reaches that of the sample, an output from the comparator stops the counting process. A clock pulse frequency of about 40 MHz is required in order that the maximum count of 1023 can be reached in the 25 μs available between samples.

The states of the individual stages in the counting circuit now describes a binary number representing the magnitude of the sample. These states, in the form of voltages, are then transferred to an output register from which they can be extracted when required by the next process. Finally, the saw-tooth

† To give complete freedom from impairment to the reproduced sound under the most critical listening conditions and when the input programme is slowly faded to a very low level, at least 13 digits per sample are required.

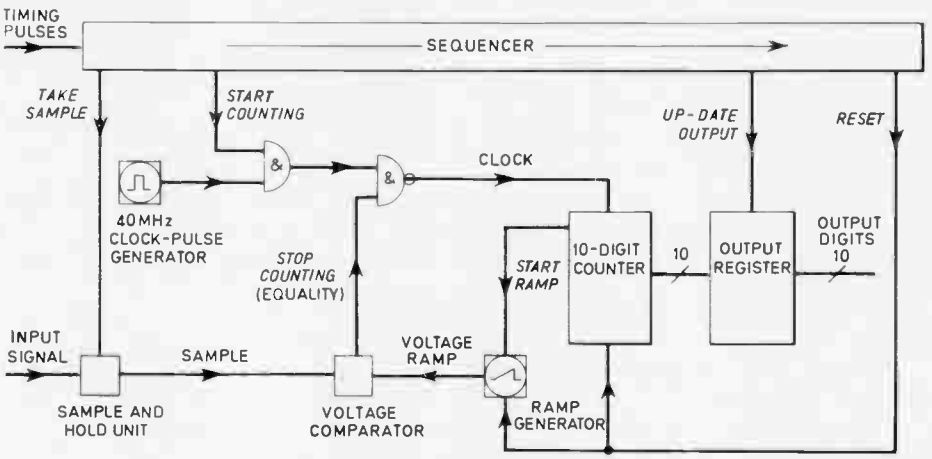

Fig. 1. Block diagram of an analogue-to-digital converter.

generator and the counter are reset so that encoding of the next sample may begin.

Counter-type d.a.c.s are constructed similarly but operate in the reverse sequence. The incoming digital word is set into a 10-digit binary counter which is then made to count down. The rise of a voltage ramp is initiated at the start of the counting process and arrested when the counter reaches zero. The ramp has then reached a voltage proportional to the incoming digital number and this voltage is sampled and filtered to form the output signal.

The operations of the d.a.c. are also controlled by a sequencer which is synchronized to the incoming signal.

A number of a.d.c.s and d.a.c.s of the above form have been built, making extensive use of integrated digital circuits. The input to output performance of any system in which they are used depends only on the performance of the a.d.c. and d.a.c. Measurements carried out on an a.d.c.–d.a.c. pair have shown that the theoretical signal/noise ratio was achieved. When a 1 kHz tone of almost maximum permitted level was injected into the a.d.c., distortion components of the following amplitudes were observed at the output of the d.a.c.:

2nd-harmonic 0·38%, 3rd-harmonic 0·14%, 4th-harmonic 0·03%.

5. The Need for Alternative Music Transmission Systems

At the present time there is a shortage of high quality music circuits within the United Kingdom. This results from the combined effects of two quite separate trends. On the one hand, the broadcasting services of the United Kingdom are expanding their requirements for music circuits as a consequence of the increase in the number of radio and television programmes and the introduction of stereo, and on the other hand the General Post Office is modernizing the telephone system by increased use of multi-channel carrier equipment. This creates a problem in providing circuits to the standard required for high-grade audio transmission because multi-channel circuits, whilst capable of providing sufficient bandwidth for music, suffer from a higher noise level than do traditional baseband circuits.

High-quality music circuits are thus at a premium at the present time and the B.B.C. has sought ways of alleviating this shortage. In the course of the next decade or so the G.P.O. will be installing pulse code modulation systems which, although primarily designed for telephony, will almost certainly be able to accommodate digitized audio signals, in which case the performance will depend only upon the number of digits that can be made available for each connection. For this purpose alone, a study of the application of digits to high quality sound is worthwhile, but there is a more immediate incentive in the case of sound signals that accompany television signals.

Special video circuits are provided by the G.P.O. to convey picture signals from studio centres to transmitters, and during the synchronizing pulse periods, the information carrying capacity of these circuits is not fully utilized. Thus a channel bandwidth of several megahertz is available for additional use during periods of a few microseconds which recur at television line frequency. Although the noise level on typical television circuits is too high to allow analogue samples of the audio signal to be used, the time × bandwidth product is sufficient to permit the use of pulse code modulation. Here then is an immediate oppor-

tunity to relieve the demand on conventional music circuits by utilizing the line synchronizing periods of television waveforms for the distribution of the accompanying sound signals.

It is fortunate that at the present time, when p.c.m. for high-quality audio signals is technically feasible, the B.B.C. is planning to discontinue the use of 405-line television signals for distribution of B.B.C.–1 programmes to the transmitters and to use 625-line signals for both B.B.C.–1 and B.B.C.–2 distribution. The latter line frequency is better suited to sound-in-vision. (Standards converters will provide the 405-line B.B.C.–1 picture at the v.h.f. transmitters as the use of this line standard will continue for v.h.f. transmissions for several years.)

6. Description of the 'Sound-in-Vision' System

The 625-line television system has a line frequency of 15·625 kHz. An audio signal having a bandwidth of about 14 kHz may therefore be carried by a p.c.m. system using twice line frequency as its sampling rate. In the present sound-in-vision system the incoming audio signal is sampled once every half line period, and digital words representing two consecutive samples are inserted into the television waveform (in a 'combiner unit') during each line-synchronizing period. At the receiving terminal, the sound pulses are extracted from the video waveform (in a unit called the 'separator') and presented to a d.a.c. from which the analogue form of the audio signal is recovered. The a.d.c. and d.a.c. in the present experimental apparatus are of the counter-type described earlier; they handle 10-digit words in parallel form and operate synchronously with the television system at twice line-frequency.

The sound pulses occupy a period of 3·8 μs which is symmetrically disposed with respect to the leading and trailing edges of each line synchronizing pulse. Care is taken to ensure that the leading edge of the synchronizing pulse is not in any way disturbed by the introduction of the sound pulses.

The television waveform includes a number of equalizing pulses which take the place of line synchronizing pulses in the vicinity of the field-synchronizing pulses during the field suppression interval. These equalizing pulses have a width equal to half that of the line synchronizing pulses and must therefore be widened at the sending terminal in order to accommodate the sound pulse groups. The waveform is restored to normal at the receiving terminal, after the sound pulses have been extracted.

The sound pulses are of 'raised cosine' form having a half-amplitude-duration of about 182 ns. They are therefore identical to the '2*T*' pulses used for the routine testing of television links, and have a spectrum that is entirely contained within the nominal video bandwidth.

Two features are included to ensure immunity to noise on the link. Firstly, the peak-to-peak excursion of the sound pulses equals the maximum permitted excursion of the picture signal and extends from synchronizing-level to peak-white level. Secondly, the maximum possible spacing between pulses is used and this is approximately equal to the half-amplitude-duration of the pulses. Thus, since the peak of each pulse occurs when the previous pulse has very nearly finished and the following is only just beginning, no one combination of pulses will cause a significantly higher or lower peak amplitude than any other combination; 21 pulses are fitted into the permitted time slot in this way, two groups of 10 and an extra pulse which is always present in order to initiate the sound-pulse detection circuits at the receiving terminal.

The above measures ensure that the sound signal is immune to all but the most severe interference and distortion on the television link. However, it is equally important to ensure that the presence of the sound pulse does not in any way impair the vision signal. If the phase and/or amplitude of low-frequency components is not correctly preserved in the transmission circuit the post-line-synchronizing blanking level may be perturbed by variation in the mean level of the sound groups preceding it. If clamping were subsequently used, this perturbation would affect the television signal during the active line period, producing an effect similar to that of 'sound-on-vision'. Three techniques are therefore used during the formation of the sound pulse groups to minimize this effect. They rely on the fact that substantial changes in coding between one audio sample and the next are rare, and that the changes that do occur are most likely to affect the least significant digits. First, one of the two words within each synchronizing pulse is complemented—that is, ones are exchanged for zeros and vice versa. Secondly, the two pulse groups are interleaved, so that the *n*th digits from each group appear consecutively. Finally, the digits are arranged in the reverse of the normal order, so that the least significant instead of the most significant digits come first. Thus the complete pulse train is made up as follows: marker pulse, the two least significant digits, one of which is complemented, the two next significant digits, one of which is complemented, and so on, ending with the two most significant digits. The complementing and interleaving of digits from alternate groups provides a signal which has the appearance of a frequency modulated wave; this can be seen clearly in Fig. 2 which was photographed with a d.c. input to the a.d.c. Figure 3 shows the waveform usually seen on an oscilloscope, in which many different words are superimposed.

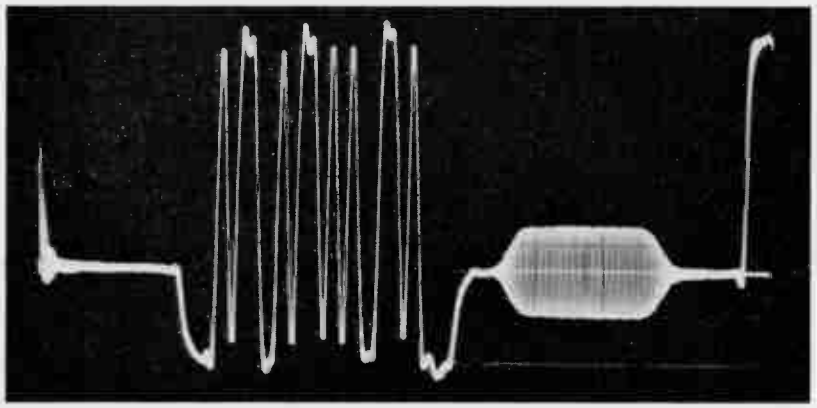

Fig. 2. The sound-in-vision waveform, d.c. input to a.d.c.

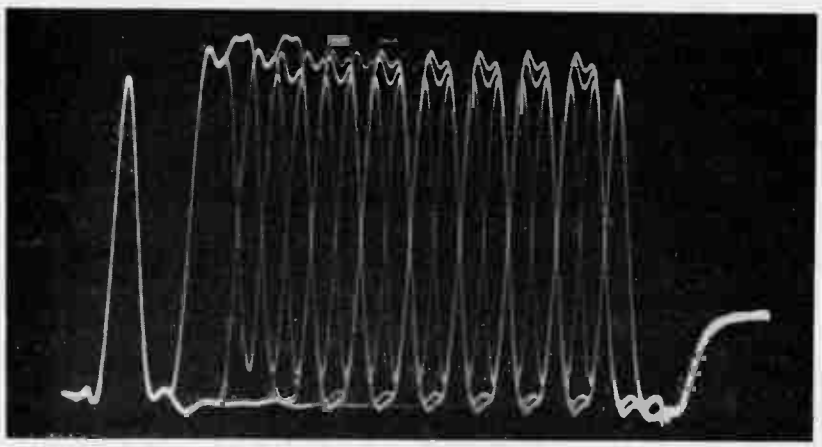

Fig. 3. The sound-in-vision waveform, normal programme input.

A specially developed 'companding' arrangement is provided for the sound-in-vision system to ensure maximum use of the channel capacity and thus reduce the effect of quantizing noise. At the sending end, the signal is pre-emphasized according to the characteristic recommended for carrier systems by the C.C.I.T.T.[6] and then passed through a limiter. The limiter is actuated only by the pre-emphasized high-frequency components of the signal; the presence of these components during gain changes masks variations in the reproduced level of quantizing noise and thus avoids 'hush-hush' effects.

Gain variations effected by the limiter are compensated by an expander at the receiving terminal. The action of the expander is controlled by a pilot tone added to the programme signal at the input to the limiter. The pilot tone is at television line frequency, its phase being adjusted so that it is sampled in the a.d.c. at peaks and troughs. Like the programme signal, its amplitude is varied in the limiter. The expander restores the pilot-tone amplitude to a constant value, thereby restoring the programme signal to normal level. Finally a de-emphasis network restores the signal to its original form.

Figure 4 shows the spectrum of the combined programme signal and amplitude modulated pilot tone. The pilot tone and its sidebands occupy the spectral region centred on half the sampling frequency. Even in the absence of a pilot-tone the programme signal could not occupy this region where image-frequency components are introduced by the sampling process. The rate of change of gain at the limiter must be limited to prevent pilot-tone sidebands from intruding into the audio band. On the other hand not even a momentary overloading of the p.c.m. system can be allowed. The limiter is therefore syllabic in action, and delay circuits are built into the compressor between the points of level detection and level control to prevent the p.c.m. circuit from being overloaded[7] while the gain is being changed.

The use of this pilot tone 'compandor' reduces the audibility of quantizing-noise by about 13 dB and in conjunction with 10-digit p.c.m. gives a performance similar to that obtained from 'straight' p.c.m. with at least 12-digits per word.

Figure 5 gives a simplified block diagram of a complete sound-in-vision installation. The sending and receiving ends of this installation are shown in Figs. 6 and 7; each occupies a volume of about 1·75 ft^3, and uses about 150 integrated circuits to perform the digital operations, together with discrete components for the analogue circuitry.

The system will withstand gross impairments to the combined signal in the form of noise, distortion, etc. The sound signal may be recovered without any impairment unless the link distortions are so severe that equipment within the video signal chain ceases to function correctly.

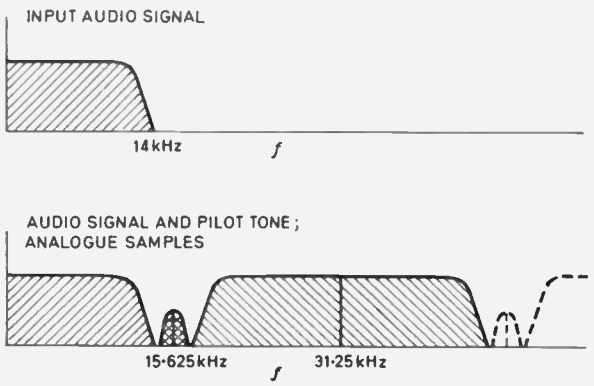

Fig. 4. Spectrum of input signal and of analogue samples.

7. Other Future Uses

The above system enables the sound signal associated with a television programme to be distributed using p.c.m. It is quite likely that one day the vision signal may also be distributed in the form of p.c.m. Once again sound and vision signals could be combined by time-division multiplexing, though it is not clear what form the combined digital signal might take. Such developments, like the p.c.m. distribution of sound signals for radio broadcasts, await the provision of nationwide data links. In the meantime, however, sound-in-vision provides an opportunity to gain experience in converting high-quality sound signals to digital form and in processing these digits in a limited but useful way.

Sound-in-vision may be expected to extend to most of the television links between B.B.C. premises so that ultimately most sound signals entering and leaving a television studio centre will be in digital form. It is thus logical to consider the pros and cons of handling sound signals in digital form within the studio centre. The advantages of digital codes are not confined to transmission and certain of the operations carried out on sound signals within studio centres would be more reliable and probably less costly if digital rather than analogue equipment were used. An example of such an operation is sound recording. The normal noise level introduced by tape recording exceeds that of most signal sources and also exceeds the quantizing-noise associated with p.c.m. systems of the type described above. Analogue tape recorders, moreover, need careful setting up and maintenance. Some form of digital recording, on either magnetic tape or some other medium, would therefore be advantageous, since the recording and replay process would not change the signal/noise ratio of the p.c.m. signal. Indeed, there is no fundamental reason why video tape machines should not be modified to record the complete sound-in-vision signal, thus avoiding the necessity to decode and recode, as well as providing a sound recording free of intrinsic degradation.

In the studio centre, other operations, such as mixing, fading and filtering, which are at present

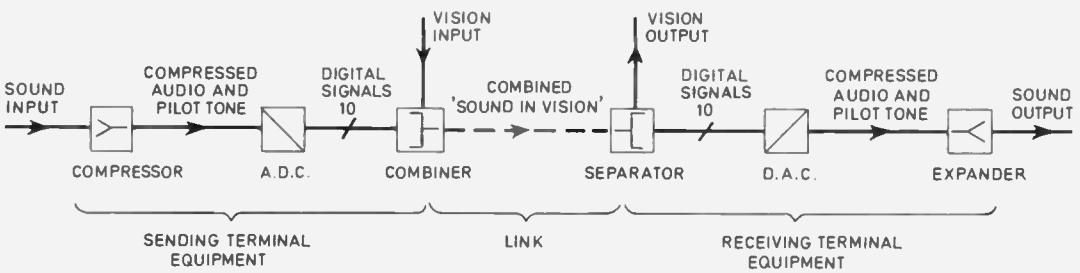

Fig. 5. Block diagram of sound-in-vision system.

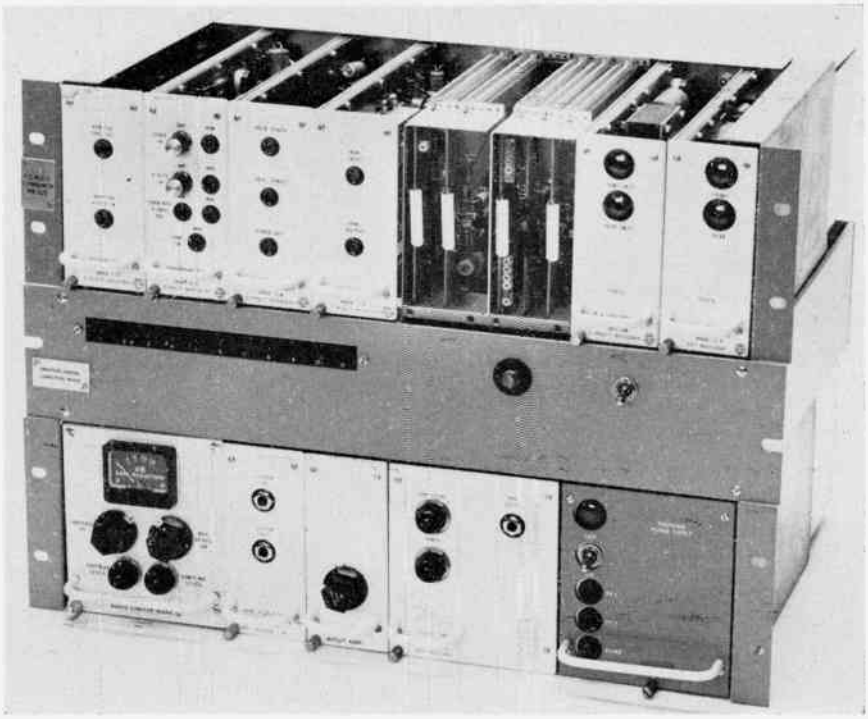

Fig. 6. Sound-in-vision, prototype sending terminal.

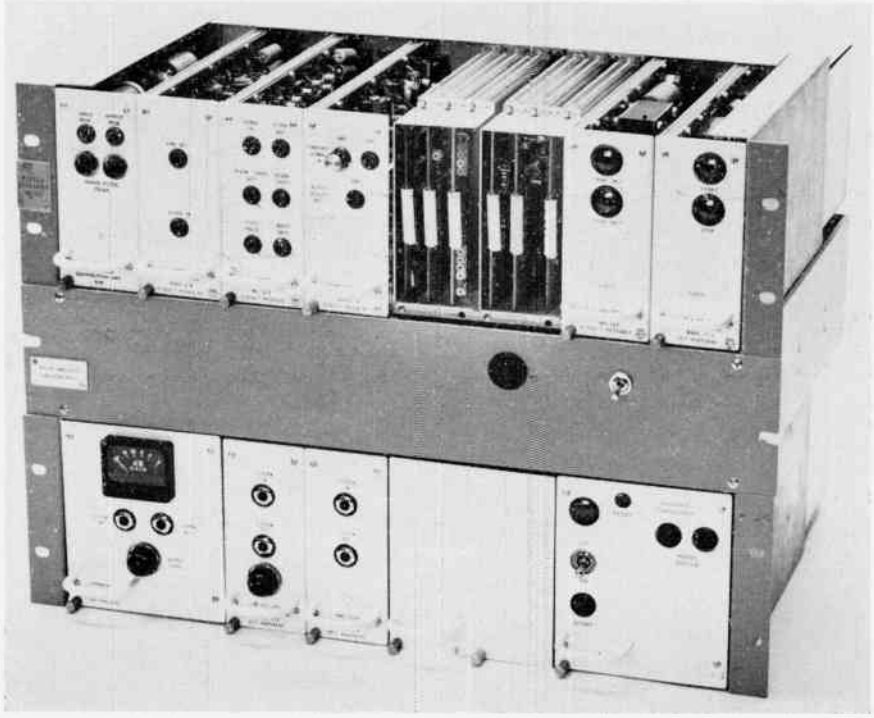

Fig. 7. Sound-in-vision, prototype receiving terminal.

more easily performed on analogue signals, are necessary. In the context of a widespread use of digital signals, however, it would be better to carry out these operations by digital methods to avoid the necessity for a large number of a.d.c.s and d.a.c.s and the increase in quantizing-noise that inevitably results.

8. Acknowledgments

The authors wish to thank the Director of Engineering of the British Broadcasting Corporation for permission to publish this paper.

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Manuscript first received by the Institution on 20th November 1969 and in final form on 3rd February 1969. (Paper No. 1249/Com. 9).

Contributors to this Issue

Eric R. Rout, C.Eng., M.I.E.E., (*left*) is Head of the Electronics Group in the B.B.C.'s Research Department at Kingswood Warren. He studied electrical and radio engineering at the Cambridgeshire Technical College and the Borough Polytechnic, London, whilst in the employ of Pye Radio Ltd. In 1950 he joined the Engineering Research Department of the B.B.C. and became Head of the Video Frequency Section in 1962. Before his appointment to his present post in 1967 he was for a year Head of Special Projects Section. Mr. Rout has been closely connected with developments in television standards conversion since the first cross-channel exchanges in 1952.

Howard Jones (*right*) is with the B.B.C. Research Department at Kingswood Warren. After gaining an honours degree in Electrical Engineering at Birmingham University, he spent two years in the R.A.F., during which time he was involved at the Royal Radar Establishment, Malvern, in the development of new radar equipment. He joined the B.B.C. Research Department in 1960, working on camera tubes, standards conversion, colorimetry and spatial filtering. Since joining th B.B.C. Baseband Systems Section in 1967, he has been responsible for various work on pulse code modulation, including the development of the experimental sound-in-vision system.

J. T. Starbuck, M.A., C.Eng., M.I.E.E., is with the Plessey Company at Braxted Park, where for the last four years he has been head of a group concerned with studying problems of h.f. and v.h.f. aerial systems and associated equipment. He attended Sebright School, Wolverley, and read for the Mechanical Sciences Tripos at Cambridge, graduating in 1950. In the same year he joined the Marconi Company, Chelmsford, as a Graduate Apprentice, and was afterwards employed as a development engineer in v.h.f. and u.h.f. multi-channel telephony link equipment at the Company's Writtle and Great Baddow Laboratories. In 1956 he was appointed a Senior Engineer at the Plessey Company and worked on u.h.f. receiving equipment until his present appointment in 1965.

A. C. Davies, B.Sc.(Eng.), M.Phil., C.Eng., M.I.E.E., has been a lecturer in the Department of Electrical and Electronic Engineering at the City University, London, since 1963. At present he is on leave of absence at the University of British Columbia, Vancouver. He holds the degree of B.Sc.(Eng.) in Electrical Engineering of the University of Southampton and obtained his M.Phil. at the University of London in 1967, for research on active networks. From 1961 to 1963 he worked for the General Electric Co. (Telecommunications) Ltd. at Coventry on filter design and pulse code modulation systems. Mr. Davies' research interests include active networks, digital systems and pseudo-random sequences.

John I. Sewell, Ph.D., B.Sc., (*left*) has been a lecturer in the Department of Electronic Engineering, University of Hull, since 1968. He studied at Sunderland Technical College and Kings' College, University of Durham, graduating in electrical engineering in 1963. In 1966 he received the Ph.D. degree in electrical engineering from the University of Newcastle upon Tyne, where he became a Senior Research Associate in 1968. While at Newcastle he was engaged in study of computational methods in the design of active networks.

Frederick William Stephenson, Ph.D., B.Sc., (*right*) is a lecturer in the Department of Electronic Engineering at the University of Hull. He was educated at Rutherford College of Technology and King's College, Newcastle, from which he graduated in 1961 with first class honours in electrical engineering. In 1965 he was awarded the degree of Ph.D. by the University of Newcastle for research in active filters. For the next two-and-a-half years Dr. Stephenson was employed by Electrosil Ltd. and held the post of Technical Manager in the Company's Microelectronics Division. In May 1967 he returned to the University of Newcastle upon Tyne as a Senior Research Associate in Network Theory, under the sponsorship of the Ministry of Technology. He took up his present appointment in October 1968. Dr. Stephenson is a co-author of several papers on R-C active networks and circuit theory published in this *Journal.*

R. A. Morris, B.Sc., (*left*) is Head of Electronics Section of the Physics and Engineering Laboratory, Department of Scientific and Industrial Research, Lower Hutt, New Zealand. From 1948 to 1952 he was in the Industrial Development Department of Canterbury College, New Zealand, where he obtained his B.Sc. degree in 1951. He was at the Royal Radar Establishment, Malvern, from 1952 to 1955, and joined the Physics and Engineering Laboratory of D.S.I.R., New Zealand, in 1958. Mr. Morris was scientific leader at Scott Base, Antarctica during the Summer of 1963–64.

Rodney Graeme Brown (*right*) is a Technician at the Physics and Engineering Laboratory, D.S.I.R., New Zealand. He was educated at Wellington Polytechnic and obtained the New Zealand Certificate of Science in 1966. He is a Student member of the Institution of Electronic and Radio Engineers and has recently completed the academic requirements for Graduate membership of the Institution.

UDC 621.377.622.12

An Electronically Programmable Shift Register

By

Professor J. W. R. GRIFFITHS, Ph.D., C.Eng., F.I.E.R.E.†

AND

M. TOMLINSON, B.Sc.†

Summary: A shift register is described, the connections of which can be electronically programmed as desired, causing it to act as a feedback shift register, a multiplier, or as a divider. The characteristic equation of the feedback shift register may be readily altered at high speed, and the polynomial for multiplication or division may be similarly varied. The register may be realized in the form of a microcircuit on a single semiconductor chip.

1. Introduction

A binary shift register is an extremely versatile circuit configuration and its use has extended far beyond its simple beginning. For instance, with the addition of logic gates it can be used for the multiplication and division of binary sequences, or by feedback connections, it can operate as a generator of sequences—in particular, maximum length sequences which have such interesting properties. Its use as a correlator or as a transversal filter is also well known.

The simple circuit described in this paper enables many of these functions to be realized without physical alteration of the circuit. It offers the following advantages:

It may be used as a pseudo-random sequence generator as well as for multiplication and division of binary sequences.

Inter-stage connections can be altered electronically at high speed.

As a result of its simplicity, the whole circuit could be constructed on a single chip with relatively few input and output leads.

2. The Polynomial Notation of Shift Registers

The behaviour of a shift register is best described in terms of polynomial representation. A binary word can be represented as a polynomial. For example, 101011 can be represented by

$$1\times D^5+0\times D^4+1\times D^3+0\times D^2+1\times D^1+1\times D^0 = 1+D+D^3+D^5.$$

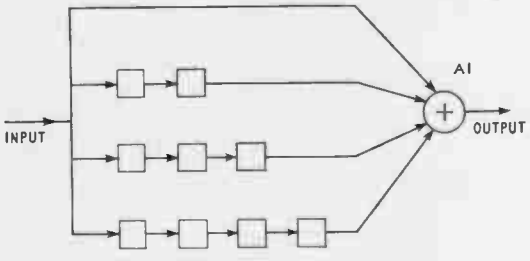


Fig. 1.
Circuit for multiplying by the polynomial $1+D^2+D^3+D^4$.

If the word is represented in serial form electrically as a stream of binary digits and such a stream is fed into a shift register, the first digit to enter will be the coefficient of the lowest power of D followed by the coefficient of the next higher power and so on, i.e. the powers of D increase with time.

3. The Shift Register Multiplier

The action of a stage of the shift register is to delay the sequence by one unit of time (one clock period) so that at the instant the coefficient of D^n is entering the stage, the coefficient of D^{n-1} is leaving it. Therefore, to obtain the sequence emerging from the single-stage shift we multiply the input sequence by D. Similarly for k stages we multiply by D^k. Thus an input sequence may be multiplied by another polynomial simply by having a set of shift registers of the appropriate number of stages. The addition involved could be normal binary addition or modulo-2 addition—modulo-2 addition is binary addition with the carry digits neglected, i.e.,

$0 \oplus 0 = 0$, $0 \oplus 1 = 1$, $1 \oplus 0 = 1$, and $1 \oplus 1 = 0$.

where the symbol $\oplus$ indicates modulo-2 addition.

Since D^m indicates a 1 in position D^m it follows that

$$D^m \oplus D^m = 0.$$

In binary arithmetic this would produce a carry digit, hence

$$D^m+D^m = D^{m+1}$$

with usual binary addition.

The system shown in Fig. 1 would multiply the input by the polynomial

$$(1+D^2+D^3+D^4)$$

or

$$(1 \oplus D^2 \oplus D^3 \oplus D^4)$$

depending on which arithmetic the adder A1 is based.

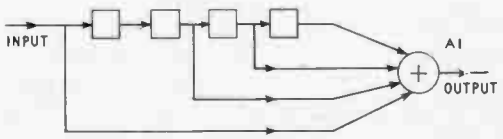
† Department of Electronic and Electrical Engineering, Loughborough University of Technology.

The circuit in Fig. 2(a) obviously performs the same function as that of Fig. 1 and economizes on shift register stages. Since the addition is linear we can redraw this circuit in the form of Fig. 2(b) using 2-input adders instead of the more complex 4-input adder, A1. When the addition is modulo-2 we can also re-arrange the circuit as shown in Fig. 3 without changing its function. Here, if the input sequence is A then the output of adder A1 is (A ⊕ DA). At the output of adder A2 we have D(A ⊕ DA) ⊕ A and finally at the output of adder A3,

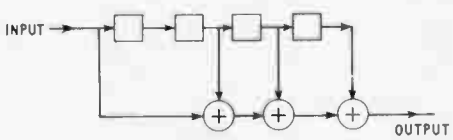
$$D^2 [D(A \oplus DA) \oplus A] \oplus A = (D^4 \oplus D^3 \oplus D^2 \oplus 1) A$$

which is the desired result.

Figure 4 shows an example of a more generalized form of shift register, namely, a 4-stage shift register which will enable multiplication by any polynomial to the power of 4 to be obtained simply by closing the appropriate switches.



(a) Alternative form of Fig. 1.



(b) Another circuit for multiplying by $1+D^2+D^3+D^4$.

Fig. 2.

4. The Feedback Shift Register

The circuit in Fig. 5 multiplies the input by $D^3 \oplus D^4$ so that, if the input sequence is A and output sequence is B then,

$$B = (D^3 \oplus D^4) A \qquad \ldots.(1)$$

If the output is connected back as the input to form a feedback shift register, then by equating B to A in eqn. (1) we have the characteristic equation for the device:

$$D^4 \oplus D^3 = 1 \qquad \ldots.(2)$$

In modulo-2 addition $1 \oplus 1 = 0$, so that by adding 1 to each side, eqn. (2) may be rewritten as:

$$1 \oplus D^3 \oplus D^4 = 0 \qquad \ldots.(3)$$

Another form of this circuit which may be more familiar to those readers accustomed to feedback shift registers is shown in Fig. 6.

5. The Programmable Shift Register

A multi-purpose shift register of the form shown in Fig. 4 is readily constructed and, by means of simple switching, made to operate as a multiplier or as a feedback shift register. The use of the modulo-2 adders A1, A2 and A3 between the shift register stages enables changes of interstage connections to be made without the need for complex switching arrangements; it also gives the circuit other useful properties.

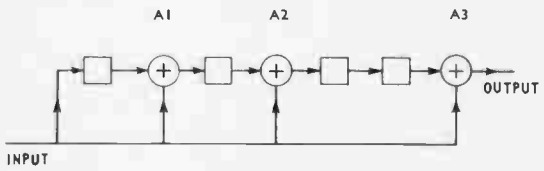


Fig. 3.
Circuit for multiplying by the polynomial $1 \oplus D^2 \oplus D^3 \oplus D^4$.

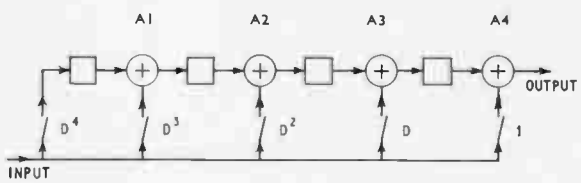


Fig. 4. Generalized form of shift register multiplier.

Recent advances in microcircuitry have made it possible to form a large number of shift register stages, typically 100, on a single chip, but to bring out a connection for each stage would create severe practical difficulties. However, by using a set of AND gates and a second control shift register as shown in Fig. 7 the number of outside connections may be reduced to a very small number.

5.1 *Operation*

A binary word is first fed into the control shift register and those stages containing a '1' cause the connection to close between the adder of the corresponding stage in the main shift register and the common line A. Thus if, for instance, the word 110101 is established in the control register then any input applied at A is multiplied by the polynomial,

$$D^6 \oplus D^5 \oplus D^3 \oplus D$$

By connecting A to B and feeding the appropriate word into the control register any one of the complete range of shift register connections can be realized.

The device can also be used as a divider. Consider the elementary circuit shown in Fig. 8; the output B is given by

$$D^3C \oplus D^3B \oplus D^2B,$$

so that

$$D^3C \oplus (D^3 \oplus D^2) B = B$$

Therefore, $$B = \frac{D^3C}{D^3 \oplus D^2 \oplus 1}$$

i.e. the output B is a delayed version of the input sequence divided by the polynomial $D^3 \oplus D^2 \oplus 1$. Similarly, if A is connected to B in Fig. 7 and the input is fed in at C, then with the particular word

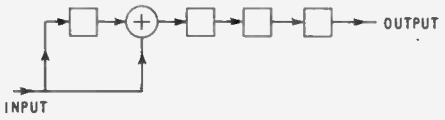


Fig. 5. Circuit for multiplying by the polynomial $D^4 \oplus D^3$.

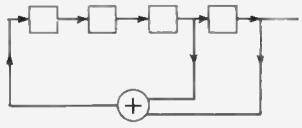


Fig. 6. Familiar form of the circuit of the multiplier when it is used as a sequence generator.

110101 established in the control register the output will be

$$A = \frac{D^6C}{D^6 \oplus D^5 \oplus D^3 \oplus D \oplus 1}$$

6. Applications

There are obviously numerous applications of this versatile circuit. As a feedback shift register it could be used as a pseudo-random sequence generator.[1, 2] The most usual feedback connections are those which give the maximum length of binary sequence for a particular number of shift register stages, i.e. for N stages a periodic sequence of length $2^N - 1$ is obtained. However, more than one sequence length is frequently required, and sometimes non-maximum length sequences are needed. The shift register device described above may be programmed to produce any

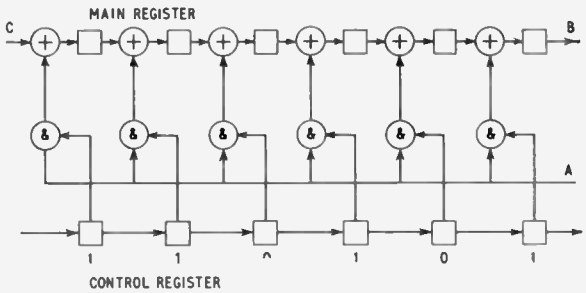


Fig. 7. Programmable shift register (6 stages) with few external connections.

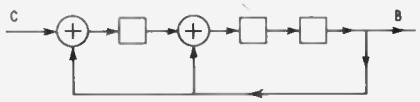


Fig. 8. Circuit for division by $1 \oplus D^2 \oplus D^3$.

periodic sequence within the capabilities of the total number of stages.

The device may also be applied as a cyclic error correcting or detecting encoder, or used for scrambling binary sequences. The latter is achieved by dividing by a polynomial at the transmitter, and multiplying by the same polynomial at the receiver. When connected as a multiplier the device could be used as a cross-correlation detector in applications where one is looking for a particular code word 'hidden' in a random sequence of digits.

The feature of rapid variation of the connections by electronic means opens up very many interesting possibilities and applications.

7. References

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Manuscript first received by the Institution on 13th November 1968 and in final form on 3rd February 1969. (Contribution No. 112/CC42.)

Standards for Nuclear Electronic Equipment

International agreement has been reached between 26 national and international nuclear laboratories in Europe on a standard—known as CAMAC*—for the design and manufacture of electronic instruments. Instruments designed to meet the new standard are electrically and mechanically compatible and can be interconnected through a specified data highway to form simple or complex systems for signal and data processing. Such systems are independent of the choice of computer or other processing device. The new standard, if widely adopted, will not only simplify the task of designing and commissioning measurement and control instrumentation systems but will also permit manufacturers to sell their products in wider markets than has hitherto been possible. The CAMAC design specification may be used free of charge and without seeking permission by any organization or company: full details will shortly be available in a Euratom report.†

The CAMAC standard was developed by the European Standards of Nuclear Electronics (ESONE) Committee. The Committee is an informal forum of nucleonic instrumentation and data processing experts in Europe which was originally set up, in 1960, on the initiative of the Euratom Research Centre, Ispra. The membership is drawn exclusively from national and international laboratories and universities in Europe. The need for new standards for advanced data processing in the nucleonic field was recognized by the ESONE Committee in 1966 and final technical agreement was reached in the autumn of 1968. There is liaison with the equivalent committee on nucleonic standards in the United States (the N.I.M. Committee).

The CAMAC standard anticipates and exploits the growing use of automatic means for data acquisition and processing (especially on-line to digital computers or equivalent equipment), and the widespread adoption of integrated circuit components. The standard prescribes the physical format of the modular instrument units, the electrical characteristics of power supplies and signals, and the means used to transfer data on a multi-wire highway. These features are independent of the types of transducer or computer used in any specific measurement or control system and they are defined in such a way that operational needs may readily be met in both simple and complex systems.

The uniformity of 'hardware' is based on a basic '19-inch' crate (overall dimensions are 483 × 221·5 × 306 mm) which can contain up to 25 modules at a mounting pitch of 17·2 mm; 24 of these modules would be standard units fulfilling the various functions required in the system while the 25th module acts as a control station for the 'dataway' which interconnects the units and links them to input and output devices and computers. Each module, which is basically a printed circuit card and a front panel is connected to the dataway and power supplies by an 86-way connector. The design of the crate permits the incorporation of instrumentation units designed to the American NIM. standard by means of an adaptor linking the unit to the crate wiring.

Although the CAMAC system is designed primarily to meet computer-based measurement and control requirements in the nuclear field it is emphasized that it is also likely to be of value in many other measurement and control situations, especially those which involve the use of a controlling computer. In these applications CAMAC is complementary to other schemes that have been or are being developed.

Harwell staff of the U.K. Atomic Energy Authority have played a leading role in the development of the CAMAC system and originally proposed the basic principles to the ESONE Committee. Since then detailed study of the mechanical, electrical, signal and data transfer aspects of the scheme, by the national and international laboratories involved, has led to the complete formulation of the standard and its final approval and publication. Care was taken throughout to ensure that equipment designed to the U.S.A.E.C. (NIM) standard would also be compatible with equipment designed to CAMAC standards.

There are many ways in which the CAMAC specification can be fulfilled in a series of modular electronic instruments. One method has been worked out in detail at the Atomic Energy Research Establishment and this forms the basis of the 'Harwell 7000 Series' of nuclear and data processing instruments.‡ This series is being developed rapidly by a design team from the Electronics and Applied Physics Division at Harwell working in close partnership with design teams from the two principal licensees for the series, namely, Dynatron Electronics Division of Ekco Electronics Ltd., and Nuclear Enterprises Ltd. The two companies are now marketing the first instruments of the series. As a further service to industry, a series of one-day appreciation courses on the CAMAC system are being arranged at the Education and Training Centre, A.E.R.E., Harwell, Didcot, Berkshire; interested firms or organizations are invited to apply direct to the Centre for information about these courses.

* The name CAMAC was chosen quite arbitrarily—it is not an acronym of the initials of any organization or function.

† 'CAMAC. A modular instrumentation system for data handling: a description and specification.' ESONE Committee Preprint, December 1968. Advance copies are obtainable from the Electronics and Applied Physics Division, A.E.R.E. Harwell, Didcot, Berkshire.

‡ Although the approach of the '7000 Series' has been influenced by the earlier 'Harwell 2000 Series', described by H. Bisby in a paper in *The Radio and Electronic Engineer* (29, No. 3, pp. 185–195, March 1965), there is no compatibility between the two standards.

U.D.C. 621 374.72

The Design of Feedback Shift Registers and other Synchronous Counters

By

A. C. DAVIES,
B.Sc.(Eng.), M.Phil.†

Summary: This paper is concerned with digital sub-systems comprising bistable flip-flops connected to a common source of clock-pulses. This configuration, of which the feedback shift register is the most important special case, is useful for the generation of periodic binary codes and sequences. It is assumed that the building-blocks for these circuits are integrated J-K flip-flops and NAND gates, and design techniques appropriate for this situation are described.

1. Introduction

Some years ago, the present author, together with P. E. K. Chow, described the design and use of feedback shift registers (f.s.r.) as counters and code generators.[1] At that time, the bistable flip-flop used in such circuits was almost invariably a discrete-component pulse-triggered type, having diode-capacitor steering gates.

Since then, the use of digital integrated circuits has become widespread, and the J-K bistable flip-flop[2] is now generally used. The properties of the J-K flip-flop are such that in comparison with the pulse-triggered flip-flop referred to above, more systematic, and in many cases simpler, design techniques can be used and the resulting circuits are themselves often simpler. It is the purpose of this paper to give a more complete, systematic, and up-to-date presentation of the subject matter of the previous paper, taking into account these integrated-circuit developments.

2. The J-K Bistable Flip-flop

The clocked set-reset (S-R) flip-flop, of which the discrete-component pulse-triggered circuit is an example, suffers from the disadvantage that if both the 'set' and 'reset' inputs are allowed to become '1' simultaneously, the ensuing state of the flip-flop is indeterminate. With the J-K flip-flop, all possible input conditions are permissible and the indeterminate condition does not arise. To achieve this, the J-K flip-flop requires a more complex internal structure, which made its use uneconomic prior to the introduction of silicon integrated circuits. The behaviour is defined as in Table 1, from which it can be seen that the J input corresponds to the 'set' input of the simpler S-R flip-flop and the K input corresponds to the 'reset' input. If J and K inputs are both '1', the J-K flip-flop changes state at each clock pulse (e.g. it acts as a 'divide-by-two' element, as is used in asynchronous 'ripple-through' counters).

The information in Table 1 may be given more compactly in the form of an equation as follows:

$$Q_{n+1} = Q'_n . J_n + Q_n . K'_n \qquad \text{.....(1)}$$

where Q_{n+1} denotes the state after the $(n+1)$th clock pulse, and Q_n denotes the state, and J_n, K_n the inputs, after the nth clock pulse.

The corresponding equation for an S-R flip-flop would be

$$Q_{n+1} = Q'_n S_n + Q_n R'_n \qquad \text{.....(2)}$$

but would be valid *only* if the additional condition

$$S_n . R_n \neq 1$$

were satisfied. Equation (1) is not subject to such a restriction, and this is one reason why design using the J-K flip-flop is more straightforward.

Table 1

J-K flip-flop behaviour

Conditions before clock-pulse				Conditions after clock-pulse	
J	K	Q	Q′	Q	Q′
0	0	X	X′	X	X′ (no change)
0	1	X	X′	0	1
1	0	X	X′	1	0
1	1	X	X′	X′	X (toggles)

2.1. *Conventions*

For a given J-K flip-flop element, a change from a 'positive-logic' convention to a 'negative-logic' convention would result in the no-change condition being (J, K) = (1, 1) and the toggle condition being (J, K) = (0, 0). In addition, the J, K labels attached to the inputs would have to be interchanged. The

† Department of Electrical and Electronic Engineering, The City University, London, E.C.1; now at the Department of Electrical Engineering, The University of British Columbia, Vancouver, 8, Canada.

element is then best referred to as an 'inverse J-K flip-flop',[2] and behaves according to the equation,

$$Q_{n+1} = Q_n.J_n + Q_n'K_n' \qquad \text{.....(3)}$$

Because of this, some care is needed in the interpretation of data sheets, as manufacturers are not always consistent in their conventions.

It will be assumed for the rest of this paper that the J-K flip-flop performs in accordance with eqn. (1), and that any additional gates used are NAND gates. These assumptions are appropriate where a positive logic convention is used with d.t.l. or t.t.l. integrated circuits, which are at present the most popular types.

The building blocks for the systems to be discussed are therefore those shown in Fig. 1.

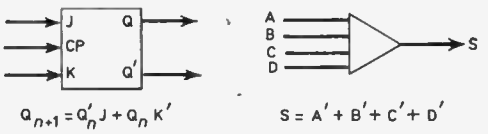

Fig. 1. Symbols for J-K flip-flop and for NAND gates.

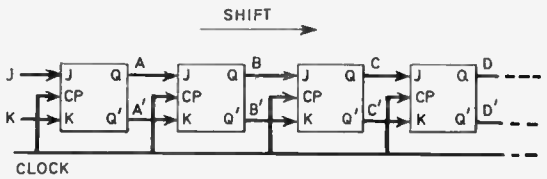

Fig. 2. Shift register constructed from J-K flip-flops.

2.2. *Construction of a Shift register*

If a number of J-K flip-flops are connected to a common source of clock pulses and interconnected as shown in Fig. 2, a shift register is obtained. Thus, from eqn. (1), for the second flip-flop

$$B_{n+1} = B_n' A_n + B_n(A_n')'$$
$$= (B_n' + B_n)A_n = A_n$$

Similarly,

$$C_{n+1} = B_n$$
$$D_{n+1} = C_n$$

and so on. Each clock pulse causes the pattern of stored digits (ABCD...) to be moved along by one stage. (It may be noted that since the Q, Q' outputs are always complementary, the special ability of the J-K flip-flop to accept a (1, 1) input is not made use of except for the input stage, A.)

3. The Feedback Shift register

The feedback shift register (f.s.r.) is a structure in which the input, and hence 'next' state of the first stage, is some Boolean function, S, of the 'present' states (Fig. 3). By appropriate choices for the feedback

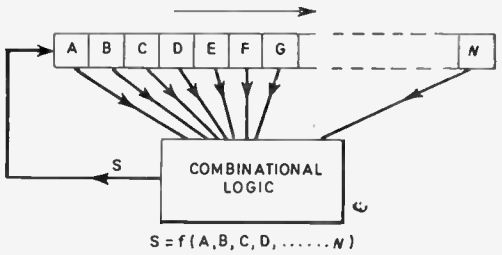

Fig. 3. Feedback shift register configuration.

function, S, a wide variety of forms of behaviour is possible. Engineering applications derive mainly from the ability of this structure to generate cyclic, periodic patterns of states.

As an example of f.s.r. behaviour, suppose that there are three stages, and that the feedback function S is given by

$$S = A'.C + B'.C' \qquad \text{.....(4)}$$

Then, a cyclic pattern of six states is generated, as follows:

A	B	C
0	1	1
1	0	1
0	1	0
0	0	1
1	0	0
1	1	0

repeats

This type of code, in which each state is a shifted version of its predecessor, is termed a cyclic-code or a chain-code.

3.1. *Self-starting Operation*

For a three-stage f.s.r., there are eight ($=2^3$) possible states, whereas the above code includes only six.

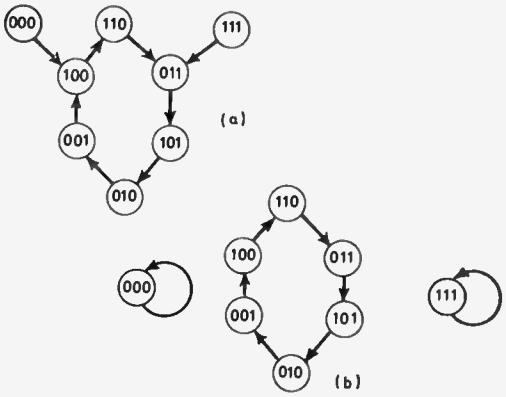

Fig. 4. State-transition diagrams: (a) from eqn. (4); (b) from eqn. (5).

It can be verified from eqn. (4) that if a non-included state does occur initially, it is followed by a state of the code. If, on the other hand, the feedback function had been

$$S = A'C + A(B'C' + BC) \qquad \ldots\ldots(5)$$

the performance would depend on the initial-state of the register. This difference is shown clearly by the state-transition diagrams in Fig. 4. For most practical applications, 'self-starting' operation is essential, and a state-transition diagram having separate parts (as Fig. 4(b)) would be unacceptable.

3.2. *Determination of the* J, K *inputs*

The combinational-logic circuit which provides the feedback must have two outputs if the shift register is to be constructed from J-K flip-flops (as Fig. 2); one output provides the J input and the other provides the K input.

However, given the feedback function, S, it is a simple matter to express it in the form of eqn. (1). One possibility is to write

$$A_{n+1} = A_n'S + A_nS \qquad J = S \qquad K = S'$$

so that S is applied directly to the J input and the complement, S', obtained via an inverter, is applied to the K input.

Alternatively, S may be decomposed as follows (as can be done for any Boolean function):

$$\begin{aligned} S &= f(A, B, C, D, \ldots) \\ &= A'.g(B, C, D, \ldots) + A.h(B, C, D, \ldots) \qquad \ldots\ldots(6) \end{aligned}$$

where g and h are functions of one less variable than f. Then, by comparison with eqn. (1):

$$J = g \qquad K = h'$$

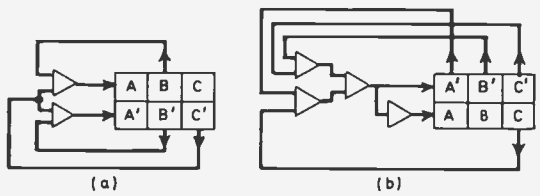

Fig. 5. Two alternative realizations of Fig. 4(a) state-transition diagram.

The second approach often requires less gates: a saving over the first approach is possible when the variable A (corresponding to the input stage of the register) appears explicitly in the minimal form of the feedback function, S.

In the previous example, the first approach requires four NAND gates, while the second requires only two (see Fig. 5).

A further advantage of the second approach is that, for an n-stage register, the design involves minimization of functions of only $(n-1)$ variables, rather than n variables (see Section 6).

4. Special Classes of F.S.R.

There are $(2)^{2^n}$ Boolean functions of n variables, and this is therefore the number of different choices of feedback function for an n-stage f.s.r. This number, $G(n)$, increases rapidly with increase in n (see Table 2), and except for $n < 5$, the various possibilities cannot be investigated thoroughly by trial-and-error techniques even with the aid of a high-speed digital computer. However, special classes of feedback function have been extensively studied, either because of their tractable mathematical properties or because of their ability to generate practically-useful codes and sequences.[3]

In this section, some properties of the more important classes of f.s.r. are outlined.

4.1. *Ring Counter*

This is the simplest possible f.s.r., in which the feedback function is simply the state of the final stage. Thus. any initial pattern in the register circulates continuously. The maximum cycle length is obviously equal to n. the number of stages, but there are always other, snorter, cycles, which may be generated, depending on the initial state (including two unit-length cycles, formed from the (1 1 1 1 . . . 1) state and the (0 0 0 0 . . . 0) state). The shoraer cycles include one of length two when n is even.

The number of cycles $Z(n)$ for each n is given by[3]

$$Z(n) = \frac{1}{n}\sum_d \phi(d)2^{n/d} \qquad \ldots\ldots(7)$$

where $\phi(.)$ is the Euler ϕ-function, and the summation is over all divisors, d, of n. Table 2 gives $Z(n)$ for the first few values of n.

4.1.1. Principal cycle

A practically-useful cycle is that in which a single '1' circulates around the ring, as shown below for $n = 5$:

0 0 0 0 1
1 0 0 0 0
0 1 0 0 0
0 0 1 0 0
0 0 0 1 0
repeats

Self-starting generation of this pattern can be ensured by the logic

$$J = B'.C'.D' \qquad K = 1$$

In general, J must be the product of the complements of all but the first and last stages.

4.2. *Twisted-ring Counter*

By making the feedback function the complement of the state of the final stage (equivalent to introducing a twist in the interconnections between an odd number of stages of a ring counter) a configuration which can generate a cycle of length $2n$ is obtained. Again, there are a variety of possible cycles (except in the trivial cases of $n = 1$, or 2) including a cycle of length 2 whenever n is odd. The number of cycles, $Y(n)$ is given by[3]

$$Y(n) = \tfrac{1}{2}Z(n) - \frac{1}{2n}\sum_{2d}\phi(2d)2^{n/2d} \quad \text{.....(8)}$$

where the summation is over the even divisors, $2d$, of n. In particular if n is odd,

$$Y(n) = \tfrac{1}{2}Z(n) \quad \text{.....(9)}$$

Table 2 gives $Y(n)$ for the first few values of n.

4.2.1. Principal cycle

A practically-useful cycle is that containing the (1 1 1 1...1) and (0 0 0 0...0) states, having the form shown below for $n = 5$. A waveform of unity mark/space ratio is produced from each stage, which has the particular advantage that individual stages change state only twice per cycle, permitting high-speed operation.

A B C D E	Decoding
1 1 1 1 1	A E
0 1 1 1 1	A′B
0 0 1 1 1	B′C
0 0 0 1 1	C′D
0 0 0 0 1	D′E
0 0 0 0 0	A′E′
1 0 0 0 0	A B′
1 1 0 0 0	B C′
1 1 1 0 0	C D′
1 1 1 1 0	D E′
repeats	

A further advantage is that decoding of each state requires two-input gates only (as listed in the right-hand column above).

Because of the usefulness of this particular cyclic pattern, it is desirable to be able to ensure self-starting. The required feedback functions are listed below for small n:

3 stages:	J = C′	K = B.C
4 stages:	J = D′	K = C.D
5 stages:	J = E′	K = D.E
6 stages:	J = F′	K = E.F
7 stages:	J = G′	K = E.F.G
8 stages:	J = H′	K = F.G.H

Table 2

Numbers associated with feedback shift registers

n	2^n	G(n)	Z(n)	Y(n)	L(n)	D(n)	$\phi(n)$
1	2	4	2	1	1	1	1
2	4	16	3	1	1	1	1
3	8	256	4	2	2	2	2
4	16	65 536	6	2	2	16	2
5	32	4 294 967 296	8	4	6	2048	4
6	64	—	14	6	6	2^{28}	2
7	128	—	20	10	18	2^{57}	6
8	256	—	36	16	16	2^{119}	4
9	512	—	60	30	48	—	6
10	1024	—	108	52	60	—	4

As n is increased, the number of unused states, $(2^n - 2n)$, becomes very large in comparison to the used states $(2n)$, and the configuration becomes less attractive.

4.3. M-*sequence Generator*

Certain binary sequences of periodic length $2^n - 1$, called maximal-length linear sequences (M-sequences), have many applications. Although deterministic and periodic, they possess characteristics which make them appear random and they pass several statistical tests for randomness. For this reason they are often termed pseudo-random.† M-sequences are widely used in linear system identification, digital communication and simulation of random noise.[4,9]

M-sequences of length $2^n - 1$ can be generated by an n-stage f.s.r. for which the feedback is a suitable linear (modulo-2) function. This is a function which can be written in the form;

$$S = a_1 A \oplus a_2 B \oplus a_3 C \oplus \ldots \quad \text{.....(10)}$$

where $a_1, a_2, a_3 \ldots$ are 0 or 1 and $\oplus$ denotes the exclusive-OR operation ($A \oplus B = A'B + AB'$). Thus, in a linear function there are no terms involving products of variables, such as A.B or B.C or A.B.C.

In order that the sequence generated shall be an M-sequence, a polynomial formed from the coefficients $(a_1, a_2 \ldots)$ as follows

$$1 \oplus a_1 D \oplus a_2 D^2 \oplus a_3 D^3 \oplus \ldots \oplus a_n D^n \quad \text{.....(11)}$$

must be irreducible and primitive.[3] The theory on

† Not all binary sequences of period $2^n - 1$ are pseudo-random. Also, there are pseudo-random binary sequences, having periods other than $2^n - 1$.

Table 3

Feedback connections for generating M-sequences

n	2^n-1	Polynomial	J input	K input	No. of NAND gates reqd.
3	7	$1\oplus D\oplus D^3$	C	+	0
4	15	$1\oplus D\oplus D^4$	D	+	0
5	31	$1\oplus D^2\oplus D^5$	C⊕E	*	4
6	63	$1\oplus D\oplus D^6$	F	+	0
7	127	$1\oplus D\oplus D^7$	G	+	0
8	255	$1\oplus D\oplus D^3\oplus D^5\oplus D^8$	C⊕E⊕H	+	5
9	511	$1\oplus D^4\oplus D^9$	D⊕I	*	4
10	1023	$1\oplus D^3\oplus D^{10}$	C⊕J	*	4
11	2047	$1\oplus D^2\oplus D^{11}$	B⊕K	*	4
12	4095	$1\oplus D\oplus D^4\oplus D^6\oplus D^{12}$	D⊕F⊕L	+	5
13	8191	$1\oplus D\oplus D^3\oplus D^4\oplus D^{13}$	C⊕D⊕M	+	5
14	16383	$1\oplus D\oplus D^6\oplus D^{10}\oplus D^{14}$	F⊕J⊕N	+	5
15	32767	$1\oplus D\oplus D^{15}$	O	+	0
16	65535	$1\oplus D\oplus D^3\oplus D^{12}\oplus D^{16}$	C⊕L⊕P	+	5
17	131071	$1\oplus D^3\oplus D^{17}$	C⊕Q	*	4
18	262143	$1\oplus D^7\oplus D^{18}$	D⊕R	*	4

\+ Denotes that K input is same as J input.
* Denotes that K input is complement of J input.
Stages of register labelled alphabetically: A, B, C..... P, Q, R.

$$X\oplus Y = X'Y + XY'$$
$$X\oplus Y\oplus Z = XY'Z' + X'YZ' + X'Y'Z + XYZ$$

which this statement is based is outside the scope of this paper. Table 3 lists feedback functions for generating M-sequences of lengths up to 262 143. There are many alternative M-sequences for each n, the actual number, $L(n)$ being given by

$$L(n) = \frac{\phi(2^n-1)}{n} \qquad .....(12)$$

where $\phi(.)$ is again the Euler ϕ-function. Table 2 gives $L(n)$ for the first few values of n.

The particular M-sequences chosen for Table 3 are those which require the simplest circuit realization assuming that J-K flip-flops are used.

The (0 0 0...0) state does not form part of the cyclic code corresponding to an M-sequence, and if self-starting operation from this state is required, the feedback functions listed in Table 3 must be modified.

Linear feedback functions corresponding to polynomials which are not irreducible and primitive give rise to forms of f.s.r. behaviour which are convenient for mathematical analysis but which do not have significant practical applications except in codes for error correction and detection in data transmission.

It is of interest to note that very long M-sequences can be generated with simple hardware. Thus, a 60-stage f.s.r. having the J, K inputs both connected to the output of the 60th stage generates a sequence of length $2^{60}-1 = 1\,152\,921\,504\,606\,846\,975$ (the corresponding polynomial being $1 \oplus D \oplus D^{60}$). The significance of this may be appreciated by noting that, if the f.s.r. were started in the 'all ones' state, with a clock frequency of 10 MHz, over 3000 years would elapse before a return to the starting state.

4.4. Sequences of Length 2^n

The longest sequence of states that can be generated by an n-stage f.s.r. is obviously 2^n. De Bruijn has proved[5] that the number of possible alternative sequences of this length is given by

$$D(n) = (2)^{2^{n-1}-n} \qquad .....(13)$$

Table 2 gives $D(n)$ for the first few n. The simplest method of finding a feedback function to generate such a sequence is to start with an M-sequence of length 2^n-1 and to modify the feedback function so that the (0 0 0...0) state is included between the (0 0 0...1) and (1 0 0...0) states.

The feedback functions, and hence the combinational-logic circuits required for the generation of a sequence of length 2^n are never simple (in contrast with M-sequences). Golomb[3] gives a proof that the feedback function must be an explicit function of all n variables. Thus, to increase the sequence length of the 60-stage f.s.r. described above by only one digit to 2^{60}, would require sufficient additional gates to form a 59-input combinational-logic circuit (whereas the M-sequence of length $2^{60}-1$ is generated without any gates at all).

5. The General Synchronous Counter

The feedback shift register is a special case of a more general configuration, sometimes called a synchronous counter, an example being shown in Fig. 6. The connection of all flip-flops to a common source of clock-pulses is the feature which gives rise to the term synchronous, and distinguishes these counters from asynchronous 'ripple-through' types.

For the configuration shown in Fig. 6, the states $(A_{n+1}, B_{n+1}, C_{n+1})$ can be related to the states

(A_n, B_n, C_n) one clock-pulse earlier by using eqn. (1) as follows:

$$A_{n+1} = A'_n(B_n + C_n) + A_n B'_n$$
$$B_{n+1} = B'_n A_n + B_n A_n$$
$$C_{n+1} = C'_n A'_n + C_n A_n$$

A repeating pattern of six states is again obtained as follows:

1 0 1
1 1 1
0 1 1
1 0 0
1 1 0
0 1 0
repeats

The state (000) is followed by (001) and the state (001) is followed by (100).

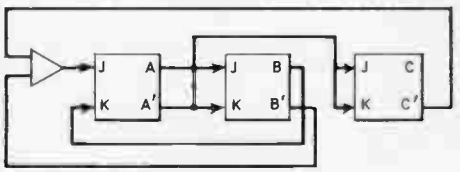

Fig. 6. Synchronous counter.

This pattern of states (code) does not possess the shifting property of the one generated by the feedback shift register (and it is therefore not a cyclic code).

Any given state-transition diagram, having the 2^n binary states already assigned, can be realized by an n-stage synchronous counter. This applies whether the diagram is in one part or several parts (as Fig. 4(b)). Circuits for the generation of many commonly used codes (e.g. pure binary, various binary-coded-decimal, etc.) can be found in applications reports produced by most of the major integrated-circuit manufacturers.

6. Synthesis

The preceding sections are mainly concerned with the analysis of a given circuit. In practice, the converse situation arises, the code, or a binary sequence, or perhaps just the period length, is given, and a circuit configuration must be obtained. It is convenient to discuss the various requirements separately.

6.1. *Completely-specified State-transition Diagram*

If the state-transition diagram is completely specified, then for any given state, the next state is determined uniquely, and no choices arise in the synthesis. A particular example of this arises in the generation of an n-digit code of period 2^n. All possible states must appear once in the code, and their order is prescribed.

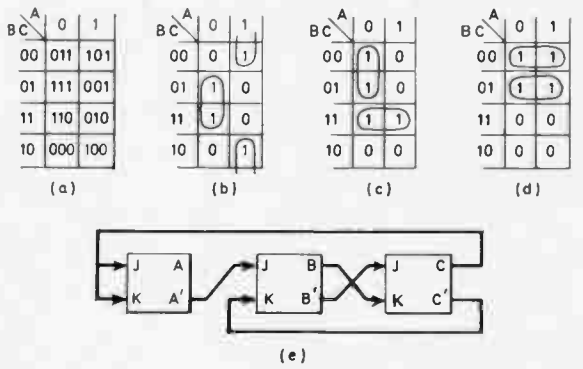

Fig. 7. (a) Complete 'next-state' Karnaugh map. (b), (c), (d) 'Next-state' maps for flip-flops A, B, C. (e) Circuit configuration.

The state-transition diagram is a closed loop of 2^n states.

Thus, suppose that $n = 3$, and that the given code is as follows:

(ABC) = (100), (101), (001), (111), (010), (000), (011), (110), repeats.

By drawing Karnaugh maps, one for the next-state of each of three flip-flops, A, B, C, and comparing the functions obtained with eqn. (1), the following results are obtained:

$A_{n+1} = A'_n C'_n + A_n C'_n$ $\quad J = K = C$
$B_{n+1} = B'_n A'_n + B_n C_n$ $\quad J = A', K = C'$
$C_{n+1} = C'_n B'_n + C_n B'_n$ $\quad J = B', K = B$

giving the circuit of Fig. 7. For this example, no additional gates are required.

6.2. *Partially-specified State-transition Diagrams*

If certain of the possible 2^n states are not included in the specified behaviour, some choice arises in their treatment. They give rise to 'don't-care' conditions on the Karnaugh maps, to which values could be assigned in order to give the simplest logic. Normally, however, there is an overriding requirement for self-starting operation. Such a situation arises in the generation of an n-digit code of period less than 2^n.

Thus, suppose that the desired code is:

(ABC) = (111), (101), (110), (000), (011), repeating.

Three states, (001), (010) and (100) are not included, and give rise to 'don't care' conditions. A possible choice gives

$A_{n+1} = A'_n C_n + A_n C_n$ $\quad J = C, K = C'$
$B_{n+1} = B'_n(C'_n + A_n C_n) + B_n(A'_n C_n)$ $\quad J = C' + AC, K = A + C'$
$C_{n+1} = C'_n A'_n + C_n B_n$ $\quad J = A', K = B'$

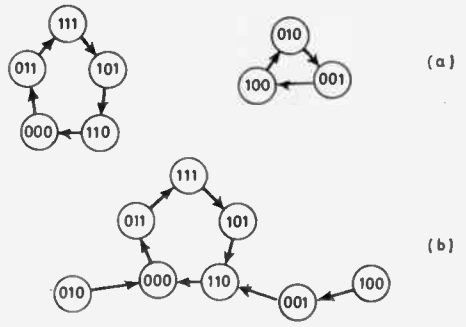

Fig. 8. State-transition diagrams: (a) showing formation of minor-cycle; (b) with minor-cycle eliminated.

This would be unsatisfactory for most applications, because the unused states form a code of length three (see Fig. 8(a)). A better choice gives

$$A_{n+1} = A'_n C_n + A_n C_n \qquad \text{(as before)}$$

$$B_{n+1} = B'_n(A'_n + C_n) + B_n(A'_n C_n) \qquad J = A' + C,\ K = A + C'$$

$$C_{n+1} = C'_n B'_n + C_n B_n \qquad J = K = B'$$

for which the state-transition diagram is shown in Fig. 8(b).

6.3. *Generation of a Given Cyclic-code*

If the code to be generated is cyclic, it can be generated by an f.s.r.; only the J, K inputs of the first stage, A, need be determined, and consequently only one 'next-state' map is required. The remaining stages are interconnected as Fig. 2.

The design is thus considerably simplified if the code is cyclic, and so a given non-cyclic code should be studied to see whether it can be transformed to a cyclic-code by complementation or column interchange. Thus, the code WXYZ, listed on the left below, does not look cyclic, but by interchanging W and X and complementing Y it becomes the cyclic-code ABCD, listed on the right (which is incidentally an M-sequence).

W X Y Z	A B C D	
1 1 0 1	1 1 1 1	
1 0 0 1	0 1 1 1	
0 1 0 1	1 0 1 1	
1 0 1 1	0 1 0 1	A = X
0 1 0 0	1 0 1 0	
1 1 1 1	1 1 0 1	B = W
1 0 0 0	0 1 1 0	
0 0 0 1	0 0 1 1	C = Y′
0 1 1 1	1 0 0 1	
1 0 1 0	0 1 0 0	D = Z
0 0 0 0	0 0 1 0	
0 0 1 1	0 0 0 1	
0 1 1 0	1 0 0 0	
1 1 1 0	1 1 0 0	
1 1 0 0	1 1 1 0	

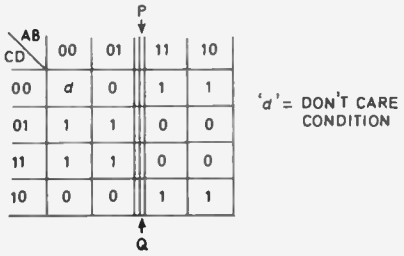

Fig. 9. 'Next-state' map for 15-state cyclic-code.

Figure 9 shows the Karnaugh map for the next-state of A. By comparison with eqn. (1) it can be seen that the 'ones' to the left of PQ give the function for the J input, and the 'zeros' to the right of PQ give the function for the K input. (The 'zeros' are collected because K is complemented in eqn. (1).)

Thus,

$$J = D$$

$$K = D$$

No additional gates are required, though to guarantee self-starting operation, it would be necessary to assign a '1' to the (0000) state, so modifying J to $(D + B'C')$.

The same circuit would have been obtained even if WXYZ had not been transformed to ABCD; only the design procedure is simplified.

Two '3-variable' maps could have been used instead of one '4-variable' map, because of eqns. (1) and (6). In general, '$(n-1)$ variable' maps can be used for the design of an n-stage f.s.r. constructed from J-K flip-flops, which is a significant simplification if n is greater than four.

6.4. *Generation of a Specified Binary Sequence*

When an n-digit code is specified (as in Sections 6.1, 6.2 and 6.3) there is an implication that the outputs of all n stages are to be utilized. Often, however, only a single output is required, from which a specified binary sequence is required. There is then obviously considerable freedom of choice in the circuit realization. The design is made easier by selecting an f.s.r. structure, and this has the advantage for some applications that the same binary sequence is available from each stage of the shift register, but with a precise time delay between each version.

If the sequence has period L, the required number of

register stages, n, lies between the limits

$$\log_2 L \leqslant n \leqslant L \qquad \text{.....(14)}$$

The upper limit corresponds to the use of a ring counter, which is generally impractical because of the large number of stages required and the difficulty of suppressing unwanted cycles, of which, by eqn. (7), there will be $(Z(n)-1)$.

The lower limit corresponds to the case where all states are on the wanted cycle.

Having decided to use an f.s.r., a cyclic code must be obtained from the given sequence. Suppose that the latter is ...01101001... having $L = 8$. At least three stages are needed, since $2^3 = 8$. However, if construction of a three-digit code is attempted, it is found that certain states are repeated (see columns A, B, C). It is necessary to add another column (D), and hence add another stage to the f.s.r.

A	B	C	D
0	1	0	0
1	0	1	0
1	1	0	1
0	1	1	0
1	0	1	1
0	1	0	1
0	0	1	0
1	0	0	1

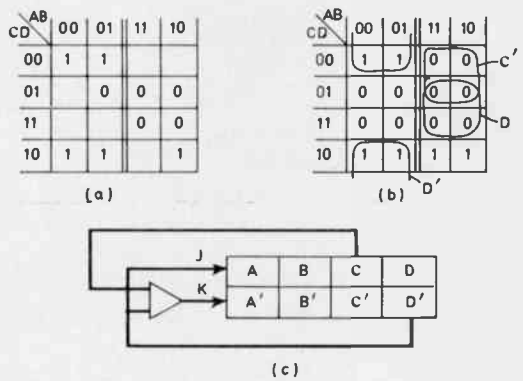

Fig. 10. 'Next-state' maps and circuit for the sequence ...01101001...

Figure 10(a) shows a 'next-state' map for this code. In addition, the (0000) entry is chosen as '1' and the (1111) entry as '0', to avoid the possibility of the f.s.r. remaining permanently in either of these states.

A choice of the other 'don't care' conditions which gives self-starting operation is shown in Fig. 10(b), from which

$J = D'$ (ones from left-hand half of map)

$K = C' + D$ (zeros from right-hand side of map)

The circuit is shown in Fig. 10(c). The apparently simpler choice of K = D results in the unused states forming an additional cycle of length 8.

This method of generating a given binary sequence is usually satisfactory only if the number of stages is at or near the lower bound specified in eqn. (14). Otherwise, it is difficult to ensure self-starting operation because of the large number $(= 2^n - L)$ of 'don't care' conditions.

Where this approach does not give a satisfactory circuit realization, an indirect method of generation may be used. A circuit for generating any sequence of the same length, L, is first designed (using methods described in other sections of this paper) and the desired sequence obtained from this through combinational-logic.

For example, the sequence above could be generated from Fig. 7 circuit by

$$X = B'C + BC'$$

In order to find the simplest logic, it is necessary to work systematically through all distinct delayed versions of the given sequence.

As a further example, consider the generation of the sequence ...0000100000... By the direct method, this would require a 10-stage f.s.r. A more practical solution would be to use a five-stage f.s.r. with J = E′, K = DE, and obtain the sequence via combinational logic A.E (see the section on the 'twisted-ring' counter).

6.5. *Cases where only the Cycle Structure is Specified*

When only the cycle structure of the state-transition diagram is specified, the order of particular states being immaterial, it is necessary to assign the available states to each position of the diagram.

Frequently the requirement is the generation of an arbitrary sequence of states of given period, L (e.g. for counter applications). The number of possible state-assignments is obviously enormous, and so the choice of a cyclic-code simplifies the design. The problem of devising cyclic codes of prescribed period therefore arises.

6.5.1. Jump technique

A convenient method is by shortening an M-sequence. It has been proved[6] that given an M-sequence of period $2^n - 1$ it is always possible to introduce a 'jump' over certain states to obtain a cyclic-code of period L, for all L in the range $0 < L < 2^n - 1$. The method used ensures self-starting operation of the f.s.r. which is an advantage over a similar technique and proof given by Golomb.[3]

Heath and Gribble[7] have tabulated the 'jump-state' required for all L up to 127.

As an example, consider the generation of a cyclic-code of period 12. This can be done by shortening the M-sequence of period 15 described in Section 6.3. Three adjacent states have to be omitted; they can be found by inspecting the code to find a pair of states differing only in the first digit, and separated by exactly two other states. The relevant part is listed below:

```
. . . .
0 0 1 1
1 0 0 1 *
0 1 0 0
0 0 1 0
0 0 0 1 *
. . . .
```

The states (1 0 0 1), (0 1 0 0), (0 0 1 0) can be eliminated.

0 0 1 1 is followed by 0 0 0 1, and the resulting code has period 12 but is still cyclic.

The original feedback function, $S = A'D + AD'$ must be modified to

$$S = (A'D + AD').(A'B'CD)'$$
$$= AD' + A'(BD + C'D)$$

Therefore, $J = (B + C')D$

and $K = D$

An additional modification would be needed in practice, to give self-starting from the (0 0 0 0) state. Use of the 'jump' technique gives no guarantee that other cyclic-codes requiring simpler logic do not exist.

Table 4 lists feedback functions for generating short cyclic-codes. In each case, the simplest functions known to the author are given.

6.5.2. Co-prime factors

If the period L can be split into co-prime factors $(L_1, L_2, \ldots, L_i)$, it may be easier to design separate circuits for each of the periods $L_1, L_2, \ldots, L_i$, and to operate them simultaneously from a common source of clock pulses. They will only be in synchronism once per L pulses, and this condition can be recognized by suitable combinational-logic.

For example, if the circuits of Figs. 8(b) and 7 were operated simultaneously, and an output pulse generated when both were in the '1 1 1' state this output would occur once per 40 $(= 5 \times 8)$ clock pulses.

6.6. *Avoidance of Unwanted Minor Cycles*

Minor cycles of unit length can arise only from the (1 1 1 . . . 1) or (0 0 0 . . . 0) states, and can be avoided by ensuring that, on the 'next-state' map,

Table 4

Feedback connections for generating self-starting cyclic-codes

n	*L*	J	K	No. of NAND gates reqd.
1	1	0	1	0
	2	1	1	0
2	3	1	B	0
	4	B′	B	0
3	5	B′	C	0
	6	B′C′	C	2
	7	B′ + C	C	1
	8	BC + B′C′	C	3
4	9	CD + B′C′	D	3
	10	B′C′ + B′D + C′D	D	4
	11	B′ + D	D(B + C)	4
	12	BD + B′C′	D	3
	13	BD + C′D′	D	3
	14	D + B′C′	D + BC	4
	15	D + B′C′	D	2
	16	D(B + C) + B′C′D′	D	4
5	17	B′C′D′ + B′D′E + BDE	E	4
	18	B′CE + B′D′E′ + BDE	E	4
	19	B′E + BCD + B′C′D′	E	4
	20	B′C′D′ + B′E + DE	E + CD	5
	21	B′E + DE + B′C′D′	E	4
	22	DE + B′CE + B′C′D′E′	E	4

$$(A.B.C.D\ldots) = 0$$
$$(A'.B'.C'.D'\ldots) = 1$$

A cycle of length two can be formed from the states (1 0 1 0 . . .) and (0 1 0 1 . . .). To avoid this, the next-state must not have more than one of the following entries:

$$(A.B'.C.D'\ldots) = 0$$
$$(A'.B.C'.D\ldots) = 1$$

Rules of this type for the avoidance of other short cycles can be devised, but they seem too complicated to be useful.

Certain methods (such as the jump technique described in Section 6.5) guarantee self-starting, but in other cases it is usually necessary to try various choices for the 'don't care' conditions until a self-starting design is discovered. Alternatively, use may be made of 'reset' facilities available on some flip-flops (see Appendix).

7. External Control of the Generated Sequence

By providing an f.s.r. with controlling input connections in addition to the clock pulse input, the generation of alternative cyclic codes of various lengths is made possible.[8]

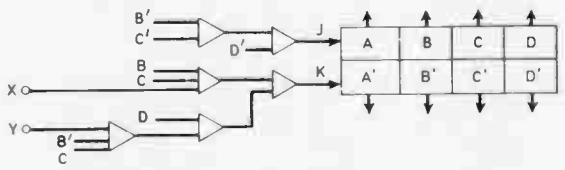

Fig. 11. Variable-period cyclic-code generator.

Figure 11 shows an example of this; this configuration can generate codes of lengths 12, 13, 14 or 15, according to the logic levels applied at X and Y, as follows:

Input X	Input Y	Cycle length
1	1	12
0	1	13
1	0	14
0	0	15

In principle, 2^n different cycle-lengths can be selected by means of n input connections.

8. Conclusions

The digital sub-systems described in this paper have a wide range of applications for binary code and sequence generation, and for counting.

In those rather rare cases where a complete state-transition diagram is specified, a unique realization is obtained. In most practical situations, however, the choice between many possible alternative state-assignments confronts the designer; the simplicity and hence the suitability of the final circuit realization is very dependant on the choice that is made. Often, the use of a cyclic-code results in a simpler design process and a simpler circuit.

9. References

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10. Appendix

The Use of Alternative Building Blocks

Instead of the J-K flip-flop, there are several alternative building-blocks which may be used, some of which are described below.

10.1. *The* D *Flip-flop*

This is an element having a single input, D (in addition to the clock-pulse input) and outputs Q, Q′ such that

$$Q_{n+1} = D_n \qquad \text{for any } Q_n$$

Functionally the element behaves as a J-K flip-flop having J brought out and labelled D, and K obtained internally from J via an inverter (the actual internal construction need not have this form).

The D flip-flop can be used directly as a shift register stage. When used as the first stage of an f.s.r., more gates may be required than when using a J-K flip-flop.

10.2. *Multiple-input* J-K *Flip-flop*

Flip-flops are often available having inputs $J_1, J_2, J_3 \ldots$ and $K_1, K_2, K_3 \ldots$ and are equivalent to a conventional J-K flip-flop preceded either by AND or OR gates. For example,

$$J = J_1.J_2.J_3 \quad \text{and} \quad K = K_1.K_2.K_3$$

or, for other types,

$$J = J_1 + J_2 + J_3 \quad \text{and} \quad K = K_1 + K_2 + K_3$$

The use of such elements can obviously reduce the amount of additional, external gates that are needed.

Some elements have a K′ input, which can be connected directly to J to provide the action of a D flip-flop.

10.3. *Shift-registers*

Multi-stage shift registers in a single package (typically comprising four stages) are at present available from several manufacturers. Because of the limited number of external connections provided by the packages, the complementary outputs A′, B′, C′ D′ may not be brought out, so that some increase in complexity of the external feedback logic is often inevitable.

10.4. *Resetting*

Most J-K flip-flops have a facility for asynchronous setting of the state in addition to the normal synchronous entry via J and K inputs. The asynchronous entry may or may not override the synchronous entry, depending upon the design of the particular units being used.

Such facilities make it possible to reset the f.s.r. when a particular state is reached. This provides considerable additional flexibility. For example, generation of codes comprising cyclic sections separated by non-cyclic discontinuities is made easier. Arrangements to ensure self-starting operation may also be made simpler.

10.5. '*Wired*-OR' *Operation*

With certain types of integrated circuit, it is permissible to connect the outputs of two gates directly together (termed 'wired-OR' operation). Generally, this is possible with d.t.l. but not t.t.l. circuits.

For example, if two such NAND gates, having inputs A, B and C, D respectively, are so connected, the function P obtained is given by

$$P = (A' + B').(C' + D')$$
$$= A'C' + A'D' + B'C' + B'D'$$

The numbers of NAND gates listed in Tables 3 and 4 are based on the assumption that wired-OR is *not* being used. If it is, the numbers can be reduced.

Manuscript first received by the Institution on 23rd July 1968 and in final form on 3rd December 1968. (Paper No. 1250/Comp. 115.)

STANDARD FREQUENCY TRANSMISSIONS—March 1969

(Communication from the National Physical Laboratory)

March 1969	Deviation from nominal frequency in parts in 10^{10} (24-hour mean centred on 0300 UT)			Relative phase readings in microseconds N.P.L.—Station (Readings at 1500 UT)		March 1969	Deviation from nominal frequency in parts in 10^{10} (24-hour mean centred on 0300 UT)			Relative phase readings in microseconds N.P.L.—Station (Readings at 1500 UT)	
	GBR 16 kHz	MSF 60 kHz	Droitwich 200 kHz	*GBR 16 kHz	†MSF 60 kHz		GBR 16 kHz	MSF 60 kHz	Droitwich 200 kHz	*GBR 16 kHz	†MSF 60 kHz
1	— 300·1	— 0·1	+ 0·1	527	430·5	17	— 300·0	— 0·3	0	534	441·7
2	— 300·0	0	+ 0·1	527	430·7	18	— 300·1	— 0·2	0	535	443·2
3	— 300·0	0	0	527	430·4	19	— 300·0	0	+ 0·1	535	442·6
4	— 300·1	0	+ 0·1	528	434·4	20	— 300·1	— 0·1	+ 0·1	536	443·7
5	— 300·0	0	+ 0·1	528	434·3	21	— 300·0	0	+ 0·2	536	444·1
6	— 300·0	0	+ 0·1	528	434·4	22	— 300·0	0	+ 0·1	536	444·0
7	— 300·0	0	+ 0·1	528	434·5	23	— 299·9	0	+ 0·1	535	443·9
8	— 300·1	— 0·1	+ 0·1	529	435·1	24	— 300·0	0	+ 0·1	535	443·9
9	— 300·1	0	+ 0·1	530	435·4	25	— 300·1	— 0·1	+ 0·1	536	444·6
10	— 300·1	0	+ 0·1	531	435·4	26	— 299·7	0	+ 0·1	534	445·0
11	— 300·0	0	+ 0·1	531	435·7	27	— 299·7	0	+ 0·1	532	444·5
12	— 299·9	— 0·2	0	530	435·9	28	— 299·8	0	+ 0·1	533	444·8
13	— 300·0	— 0·2	0	530	437·9	29	— 299·8	0	+ 0·1	533	444·5
14	— 300·1	— 0·1	0	531	438·9	30	— 299·9	— 0·1	+ 0·1	534	444·9
15	— 300·1	— 0·2	0	532	439·7	31	— 299·8	— 0·1	+ 0·1	533	446·9
16	— 300·2	— 0·3	0	534	441·1						

All measurements in terms of H.P. Caesium Standard No. 334, which agrees with the N.P.L. Caesium Standard to 1 part in 10^{11}.
* Relative to UTC Scale; (UTC_{NPL} — Station) = + 500 at 1500 UT 31st December 1968.
† Relative to AT Scale; (AT_{NPL} — Station) = + 468·6 at 1500 UT 31st December 1968.

Note: A correction of —10 microseconds should be applied to the phase readings for MSF 60kHz from 18th to 28th February 1969 inclusive; e.g. 18th February: issued result 435·8, correct result 425·8.

Skynet: The British Defence Satellite Communications System

This year will see the introduction of *Skynet*—the United Kingdom's Defence Satellite Communications System. The overall system has been designed by the Ministry of Technology for the Ministry of Defence. The system will comprise two satellites, one operational and one standby, in a closely-defined synchronous orbit some 23 000 miles above the Indian Ocean, and a total of nine Earth stations. Five of the stations will be placed at fixed locations, two installed in the assault ships H.M.S. *Fearless* and H.M.S. *Intrepid*, and two air-transportable mobile stations will be held available for rapid deployment to meet contingency requirements. The network of stations and the satellites will provide better and more reliable communications for all arms of Britain's forces, and will provide a national communication capability from the Atlantic to the Far East including Hong Kong.

The first of the ground stations has just been delivered and will be followed by a rapid build-up of the remainder of the ground network. The first satellite will be launched in the late summer of 1969 and the *Skynet* system will become available for operational traffic early next year.

The Earth stations are of advanced design and are being built for *Skynet* at fixed prices by British electronics firms in extremely short contractual periods. A fixed station will be situated at Oakhanger, Hants, to provide the *Skynet* system's U.K. terminal, which will be linked with other elements of the defence communications system. A second station at Oakhanger will provide command and monitoring facilities for satellite control. A further station (not part of *Skynet*) at the Ministry of Technology's Signals Research and Development Establishment, Christchurch, Hants, will support the *Skynet* project by making highly accurate measurements for initial calibration and testing of the satellites in orbit.

Technically, *Skynet* represents a major step forward in defence satellite communications. All the Earth stations, which are of five basic types to suit different operating environments, will handle many simultaneous channels of information by means of advanced equipment designed and built in the U.K. for the system.

The G.E.C.–A.E.I. (Electronics) terminals are constructed in three basic sections which are light enough to be air-transported to the operational zone by standard transport aircraft and by helicopter. Once a station has arrived 'on-site', six semi-skilled men can erect it, and 'lock' it on to the satellite's wavelength in only three hours. Each station's 21 ft diameter reflective dish is constructed of 12 petal sections to facilitate transportation and erection.

The satellites and launchers and certain specialized control and monitoring equipment are being built in the U.S.A. under an agreement with the United States Government which allows the U.K. to benefit greatly from the vast American investment in space. The satellite will, however, incorporate novel British concepts, particularly for meeting the stringent U.K. requirements for communicating to large and small stations simultaneously. The operating functions of the satellites and their position in the sky, will be controlled from the U.K. command and monitoring station at Oakhanger. Communications will be precisely focused towards Earth by the satellite's automatically controlled aerial. For reliability sufficient switchable duplicate equipment has been installed in each satellite to give a designed life of 3–5 years in orbit before replacement is necessary.

Skynet will be complementary to, and inter-operable with, the U.S. Initial Defense Satellite Communications System (IDSCS).

The first 21 ft (6·4 m) diameter dish for *Skynet* at a G.E.C.–A.E.I. (Electronics) establishment.

In *Skynet* the U.K. will possess a defence satellite communications system, with an operational communications capability far more flexible and of greater capacity than ever before. Furthermore it will be free from the atmospheric effects which interrupt the high-frequency radio circuits on which most of the long distance defence communications depend at present.

The total G.E.C.-Marconi Electronics involvement in *Skynet* amounts to more than £2 million, and the group is designing and building six of the nine communications stations which go to make up the system. The Marconi Company has a £1 million contract to supply and install a complete fixed satellite communications terminal at Oakhanger in Hampshire, and to modernize two existing stations overseas for continuous operation with *Skynet* satellites. Both these stations employ 40 ft (12.2 m) diameter dishes.

U.D.C. 621.374.4

Some Applications of Cellular Logic Arithmetic Arrays

By

K. J. DEAN, M.Sc., F.Inst.P., C.Eng., F.I.E.E., F.I.E.R.E.†

Presented at the Conference on 'Electronic Switching and Logic Circuit Design', organized by the College of Technology, Letchworth, with the support of the I.E.R.E., and held at Letchworth on 24th October 1968.

Summary: The paper describes two types of full multiplier. These are combinational logic networks based on a cellular structure. Some applications of these multipliers are outlined, including approximation methods for obtaining the reciprocal of a binary number, and for the quotient of two binary numbers.

1. Introduction

Cellular arrays of logic elements were first analysed by Hennie[1] and many of the terms used in this branch of logic were suggested by him. A comprehensive review of the literature is given by Minnick.[2] This deals with attempts at devising arrays of a general nature as well as for special purposes such as military code scrambling. It is only recently that there has been interest in the use of cellular logic arrays for carrying out arithmetic operations although a 3-dimensional array has been suggested for a computer control system. The development of integrated circuit technology has progressed sufficiently so that it is now possible to implement arrays consisting of some hundreds of gates on a single silicon chip, or to use flip-chip circuits in conjunction with a metallized ceramic substrate.

2. Multiplier Arrays

Early in 1968 research papers drew attention to the use of cellular arrays as multipliers.[3,4] These arrays were the parallel equivalents of serial shift-and-add methods. The cells of some of these arrays were controlled so that they were either full adders or half adders[5] depending on the numbers being manipulated in the arrays. Also the interconnection pattern between cells in the array was regular. Thus the arrays were called *iterative* arrays of cells.

In Fig. 1, S is the sum and P is the carry from the addition of the inputs, A, B and C. When D = 1 the cell is a full adder, but when D = 0 it is a half adder of the inputs A and C, whilst B is ignored. Also Q = D and R = B. As shown in the figure, the cell can be implemented with 12 2-input gates, so that an array of perhaps 20–50 of these cells could be put very easily on a single chip. The cell shown in the figure has been designed for fabrication with d.t.l. bipolar circuits, so that the wired-OR facility of these cells can be exploited here. An iterative array of these cells is referred to as a full multiplier and may be regarded as a logical building block, in some ways analogous to a full adder. Modifications to the interconnection pattern have been suggested to reduce the propagation time across the array.[6] When the array has four inputs, X, Y, K and M, as shown in Fig. 2, it has been demonstrated that the output is the function, XY + K + M.

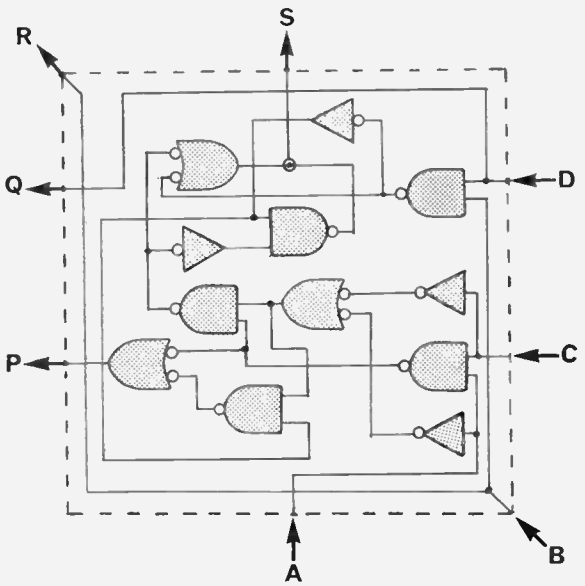

Fig. 1. Basic cell of addition-type multiplier array.

This array is more general than many logic circuits, and is, in this case, of very high complexity. It is more general, for example, than decade counters, astable and monostable circuits, and shift registers in its applications. If there are four inputs to the multiplier, of perhaps 10 bits each, the complexity of the array can be calculated. Complexity may be measured

† Vice-Principal, Twickenham College of Technology Twickenham, Middlesex.

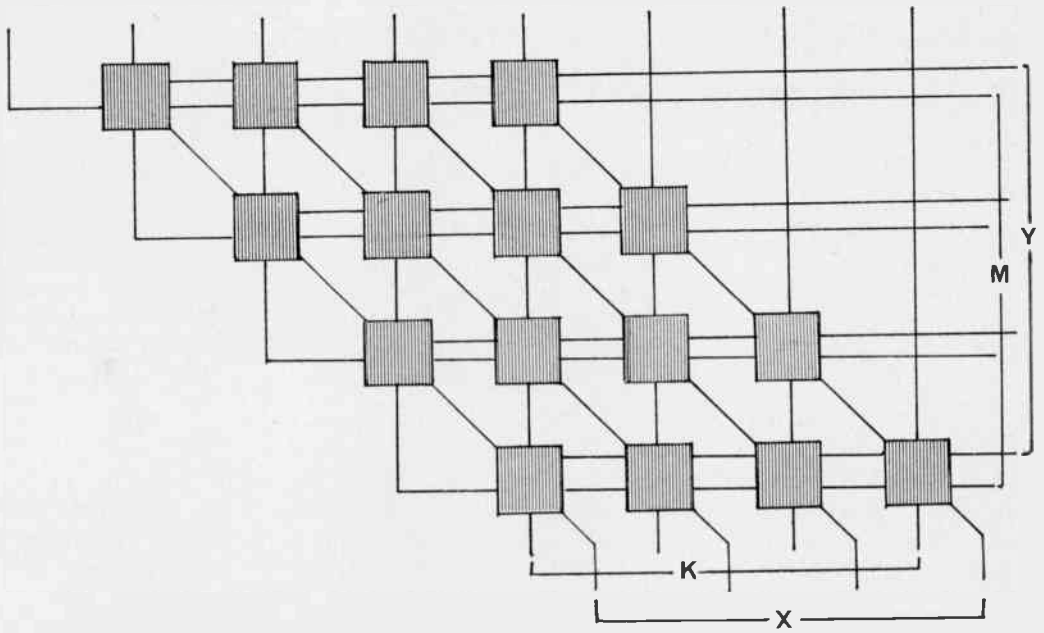

Fig. 2. Array showing full multiplier with four 4-bit inputs, yielding an 8-bit output.

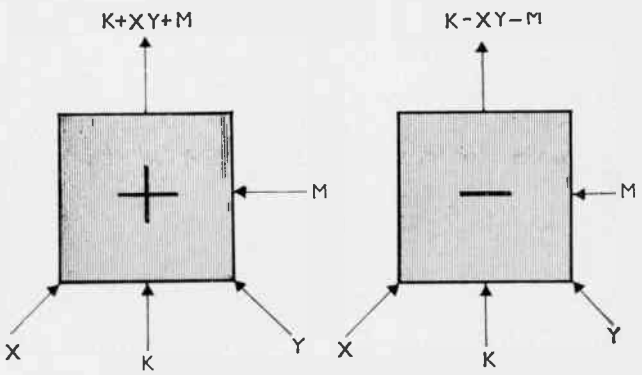

Fig. 3. Proposed logical symbols for addition-type and subtraction-type full multipliers.

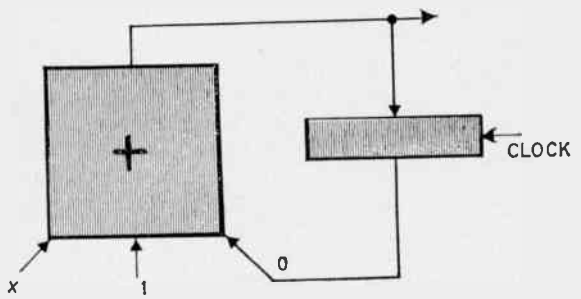

Fig. 4. Digital feedback system using an addition-type multiplier.

in the number of gates in the array for each necessary connection to it, i.e. in gates per pin. In the example suggested there would be 40 input connections, 20 outputs and 2 power supply pins. Also, such an array would consist of 100 cells or 1200 gates. Thus, the complexity is about 20 gates per pin. This compares very favourably with other circuits (a decade counter requires 2·5 gates per pin and a 10-bit serial shift register with no parallel access requires 8 gates per pin).

A multiplier array can also be designed with the same number of interconnections between the cells, but in which the cells are subtractors rather than adders. The inputs are arranged so that only borrows are propagated between cells. With these restrictions, the function that the array can handle without propagating carries is $K-XY-M$. This array also requires that $K \not< (XY+M)$.

3. Applications of Arrays

The two full multipliers can be regarded as viable l.s.i. system elements and a natural consequence of their development is to consider ways in which they can be used to generate more complex functions. Some examples of the use of these full multipliers in special-purpose machines will be given to illustrate this.

Figure 4 shows how the addition-type multiplier can be used with a storage register in a digital feedback system which is stabilized by the clock pulses

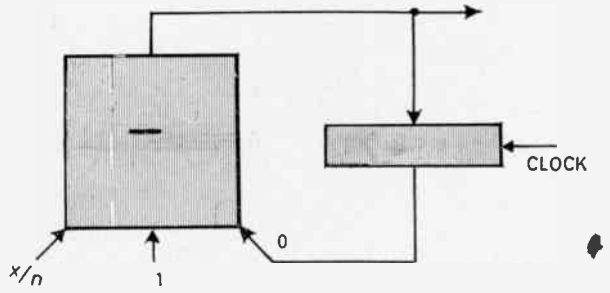

Fig. 5. Digital feedback system using a subtraction type multiplier.

which are fed to the register. Each clock pulse transfers the output from the multiplier to become one of the inputs for a successive multiplication. Thus the output from the multiplier at successive clock times is as follows:

$$1;\ 1+x;\ 1+x+x^2;\ 1+x+x^2+x^3 \text{ etc.}$$

Provided $|x|<1$ the sum to infinity of this series is $1/(1-x)$. If, in general the summing input (shown as 1 in Fig. 4) is x/m, and the multiplying input (x in the figure) is x/n, the sum to infinity is

$$\frac{nx}{m(n-x)}.$$

The subtracting type multiplier can also be used in a similar way to generate a series which may be summed for $|x|<1$. In this case the repetitive subtractions result in a series with alternating signs, the sequence of which is as follows:

$$1;\ 1-\frac{x}{n};\ 1-\frac{x}{n}+\frac{x^2}{n^2};\ 1-\frac{x}{n}+\frac{x^2}{n^2}-\frac{x^3}{n^3} \text{ etc.}$$

The sum to infinity for this series is $n/(n+x)$.

Here, if $n = 1$, the sum is $1/(1+x)$. If, in addition $y = 1+x$, then the sum $= 1/y$. Thus, if the multiplier is operated for a number of cycles it can be used to obtain an approximation for the reciprocal of a function, the accuracy of the approximation depending on the number of cycles which are allowed to take place. Also, if the summing input in Fig. 5 carries a number, z, where $z > x/n$, the sum of the series becomes z/y. Hence a quotient can be obtained from the multiplier.

A series which converges more rapidly can be implemented if one of each of the two types of multiplier are available. The system is based on the use of Newton's approximation in which, if α is a guess at the approximation, α' is a better guess if

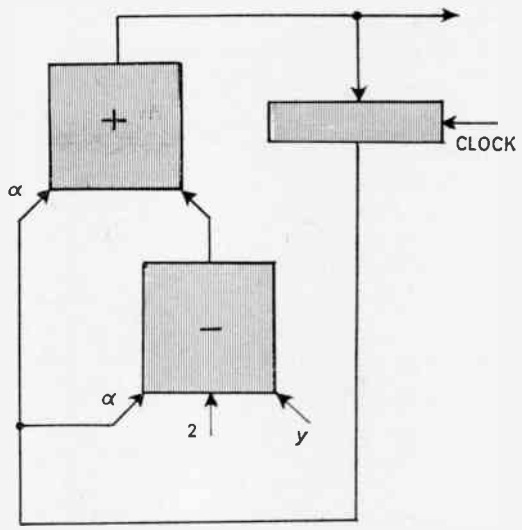

Fig. 6. System to implement Newton's approximation for the reciprocal of a function.

$\alpha' = \alpha - f(\alpha)/f'(\alpha)$. In the case of a reciprocal, this becomes $\alpha' = \alpha(2-\alpha y)$, and may be implemented as shown in Fig. 6.

4. Conclusion

It has been shown that these two full multipliers can be used as system elements to generate a reciprocal or a quotient. Other functions can be generated or other series obtained if the storage register in the systems which have been described is replaced by a shift register, in which one or more shift pulses are applied after the transfer clock pulse. Alternatively, counters can be used to supply either the summing input or one of the multiplying inputs to the multipliers.

5. References

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Manuscript first received by the Institution on 6th November 1968. (Contribution No. 113/Comp. 116).

Forthcoming Conferences

Organization and Management of R. & D.

The External and Professional Matters Sub-Committee of The Institute of Physics and The Physical Society is arranging a conference on Organization and Management of Research and Development, to be held at the Institution of Electrical Engineers, Savoy Place, London, on Monday, 5th May, 1969. The Chair will be taken by P. T. Menzies (Deputy Chairman, I.C.I. Ltd.) and speakers will include:

P. E. Trier (Mullard Research Laboratories); R. L. R. Nicholson (Program Analysis Unit, Mintech/U.K.A.E.A.); J. Bullock (Robson, Morrow and Co.); B. C. Lindley (Electrical Research Association); S. H. Clarke, C.B.E. (formerly Careers Adviser, Ministry of Technology); and D. Cobern (Research Division, Unilever Ltd.).

The conference is intended to give guidance on the techniques of research organization and management and their use, and on sources of further information and training. It should, therefore, be of interest to all who are concerned now, or are likely to be concerned in the future, with the management of research and development, whether as group leaders, project leaders or as research managers and directors.

Further information may be obtained from the Meetings Officer, I.P.P.S., 47 Belgrave Square, London, S.W.1.

Aerospace Instrumentation Symposium

The Sixth International Aerospace Instrumentation Symposium will be held at the College of Aeronautics, Cranfield, from 23rd to 26th March 1970. The Symposium is sponsored by the College of Aeronautics and the Instrument Society of America (Aerospace Industry Division).

Papers are invited for presentation at the Symposium and brief summaries should be submitted to the sponsors by 1st June 1969. Contributions should treat of appropriate subjects in the applied science and technology of instrumentation of aerospace vehicles, with particular reference to:

Instrumentation data systems for flight test of specific aircraft projects; in-flight vibration recording and analysis with particular reference to engine vibration recording; automatic test equipment for in-flight checking of complex aircraft electronic systems; general papers on transducer developments.

Full details may be obtained from Mr. N. O. Matthews, Department of Flight, College of Aeronautics, Cranfield, Bedfordshire.

Dielectric Materials, Measurements and Applications

The Institution of Electrical Engineers, in conjunction with the I.E.E.E. (United Kingdom and Republic of Ireland Section) is arranging a Conference on Dielectric Materials, Measurements and Applications, to take place at the University of Lancaster from 20th to 24th July 1970. It is expected that the conference will be of interest to those engaged in research on solid and liquid dielectrics and their applications in the power and communication industries.

The conference organizing committee invites the submission of papers on the following specific topics:

Permittivity; conduction and loss; high field behaviour; breakdown; discharges associated with solids and liquids; dielectric properties at low temperatures; impregnated systems; the influence of environment on properties; materials for high temperatures; materials with new characteristics; evaluation of thermal stability; evaluation of mechanical properties; new systems for the insulation of equipments; methods of measurement associated with any of these topics.

Intending contributors are asked to submit preliminary synopses before 30th May to the I.E.E. Conference Department. Full texts will be required before 1st January 1970.

Further details and registration forms will be available shortly from the I.E.E. Conference Department, Savoy Place, London, W.C.2.

Computational Physics

A Conference on Computational Physics will be held at the United Kingdom Atomic Energy Authority's Culham Laboratory from 28th to 30th July 1969. The conference will deal with the use of computers in solving physics problems. Papers are invited in the fields of astrophysics, meteorology and nuclear, plasma and solid-state devices. It is hoped to match the range of physics problems with an equally wide range of computing techniques: on-line control of experiments, computer simulation, non-numerical and graphical, and cine-film analysis.

Intending contributors are requested to send short abstracts of their papers to the Honorary Conference Secretary, Mr. B. McNamara, U.K.A.E.A., Culham Laboratory, Culham, Nr. Abingdon, Berkshire. Complete manuscripts will be required before 14th July. Further details concerning the Conference are obtainable from the Meetings Officer, Institute of Physics and The Physical Society, 47 Belgrave Square, London, S.W.1.

U.D.C. 621.396.677.3

A Multiple-beam High-frequency Receiving Aerial System

By

J. T. STARBUCK,
M.A., C.Eng., M.I.E.E.†

Summary: The paper describes a system, covering the band 1·5 MHz to 10 MHz, designed to give good beam-forming capability with all-round azimuthal coverage and occupying a much smaller area than a corresponding conventional rhombic aerial system. Although unsuitable for transmitting purposes, it provides, in general, externally noise-limited conditions to receiving equipment. Limited tests indicate, on the basis of error rate measurements, that the system described is as good as a rhombic array.

The parts of the system are discussed in detail and references are made to ideas concerning the upwards extension of the frequency range and the size reduction of the beam-forming networks.

1. Introduction

The aerial system described in this paper was designed and constructed for the Ministry of Technology. It was devised as an alternative arrangement to the more conventional practice of using rhombic aerials for directional reception in the h.f. band.

The equipment was built at the end of a study looking into the possibility of using a circular array of aerials, in conjunction with delay line networks, to yield fixed direction beams. The main design parameters of the array, which provided the framework of the study, were as follows:

(i) the set of fixed beams should give 360° coverage in azimuth;
(ii) the frequency range should lie between 1·5 and 10 MHz;
(iii) the directivity of each beam should be comparable with that obtainable from a corresponding rhombic aerial;
(iv) the area occupied by the array should be as small as possible compatible with achieving acceptable directivity; and
(v) the array was required for reception only.

It should be remarked that the present system, with its arrangement of fixed beams produced by passive networks, is much simpler in concept than automatically steered array designs such as the MUSA (multiple unit steerable antenna) system[1,2] (in which the beam is directed at the required elevation angle) and the MEDUSA (multiple-direction universally steerable antenna) system[3,4] (in which the beams are steerable by computer control in both azimuth and elevation).

Rhombic aerials have excellent directional properties and this partly accounts for their frequent employment in the h.f. band. Physically, they are very large and their side length may be anything from 2 to 4 (or more) wavelengths long. Consequently, the area occupied by a group or 'farm' of rhombic aerials to give complete azimuthal coverage is considerable. For example, an area of 50 acres (202 000 m^2) might be required by rhombic aerials covering the band 5 to 10 MHz. The study indicated that a circular array of 500 ft (153 m) diameter, that is, occupying an area of less than 5 acres (20 200 m^2) could give similar directional performance. The system would yield 24 independent, fixed direction, beams at 15° intervals in azimuth using 24 aerials equally spaced round the circle. Figure 1 is an artist's impression of the array; the hut in the centre houses the beam-forming networks.

In the lower part of the h.f. band, noise field strengths in the medium are generally high and usually it can be expected that the medium noise will predominate over receiver noise, the receiver typically having a noise factor of 10 dB. An improvement in signal/noise ratio can then be obtained by means of a directional aerial (such as a rhombic aerial or a combination of several simple aerial elements) which increases the signal level whilst yielding the same average noise level from the medium.

The high power gain property of rhombic aerials, commonly 12 to 20 dB, is well known. This is not always an advantage for reception in the h.f. band because large unwanted signals impressed upon the receiver can give rise to intermodulation distortion products. The present system is broadband and untuned and the monopole aerials are about 40 ft (12 m) high, being quarter-wave resonant at approximately mid-band. A combination of eight such aerials, positioned adjacently around the circle, produces beams of comparable directivity to those obtained from rhombic aerials covering the same

† The Plessey Company Limited, Radio Systems Division, Braxted Park Laboratory, near Witham, Essex.

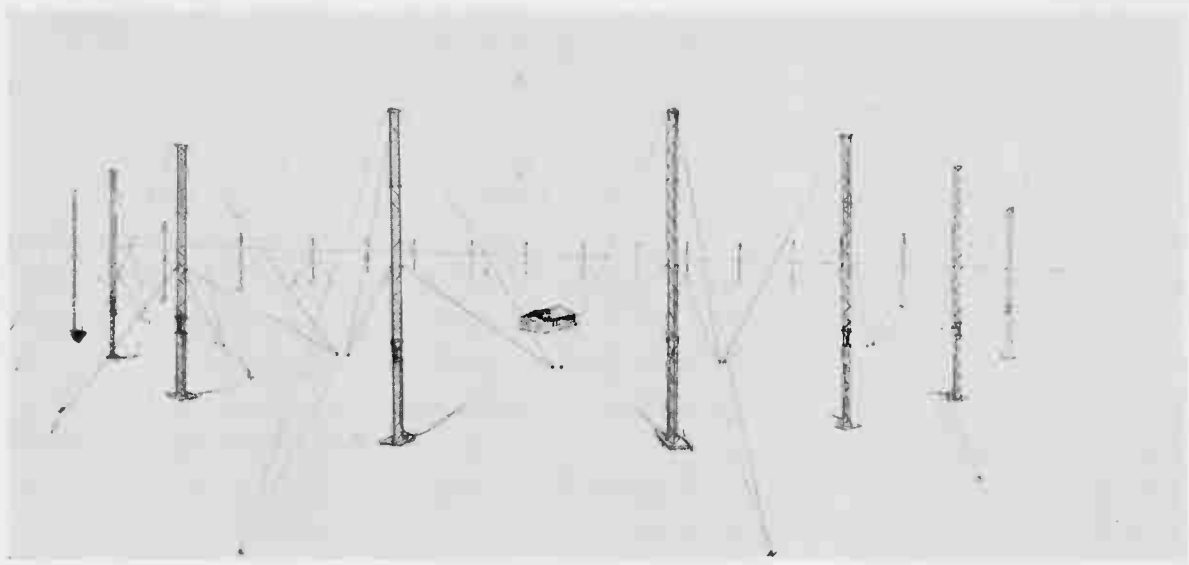


Fig. 1. Impression of system.

frequency band (for example, a beamwidth of 16° at 8 MHz, as shown in Fig. 5) and gives a worthwhile improvement over a single aerial in signal/medium-noise ratio. In forming 24, simultaneously available, beams from 24 aerials, taking eight at a time, use is made of power splitters to divide the output of each element eight ways. The resultant loss in beam output power together with the losses in feeder cables and the beam-forming networks does not materially affect the signal/noise ratio because the level of medium noise impressed on the receiver is still greater than receiver noise.

In this context, it is worth pointing out that a limited number of tests comparing rhombic aerials with the circular array have been carried out. The rhombic aerials had side lengths of 390 ft (120 m) and because it was not possible to co-site the circular aerial system with the rhombic farm, similar reference monopoles were erected at each site to form a standard for comparison. The measurements consisted of the setting up of the aerial systems and monopoles to receive teleprinter transmissions and counting the number of errors received in each. The tests occupied a period of 60 hours and yielded the following overall percentage error rates:

Site A: rhombic 1·7%; monopole 2·4%.

Site B: circular array 1·4%; monopole 4·6%

The error rates of the two monopole aerials suggest that site A was better than site B from which it may be concluded that the overall performance of the circular array would have been better had it been located on site A.

If these results are sorted into frequency bands, the error rate of the circular array for the band 3 MHz to 7 MHz lay between 1% and 1·5% while the corresponding figures for the rhombic aerials were 1·5% to 2%. For the band 7 MHz to 9 MHz, the rates were ½% to 3½% and ½% to 2½%, respectively. These figures suggest that the circular array system performed better in the lower part of its range but was somewhat inferior to the rhombic aerials between 7 MHz and 9 MHz.

The best overall picture is probably obtained from an analysis of the quality of the traffic information yielded by the four systems of aerials. A comparison of the performance of the two monopoles shows that when the error rates were low (i.e. good signal/noise conditions existed) the effects due to site difference were small: these effects increased with increase in error rate. In a similar comparison between the circular array and the rhombic system, the former was better at high error rates. Taken together, the results indicate that the circular array and rhombics had similar performance when the error rate was low and that, for high error rate conditions, the circular array probably had some advantage.

2. System Description

Figure 2 is a plan view of the system. It will be noted that 24 aerials equi-spaced round the circle are employed. They are connected to the beam-forming networks in the centre by feeder cables of equal electrical length. In this way, the relative phases of any signal received at the aerials are preserved at the inputs to the networks.

The system synthesizes 24 independent beams from the 24 aerials. Each beam is made up of the signals derived from a group of eight adjacent aerials round the circle and Fig. 2 draws attention to the array of aerials concerned with the formation of one particular beam. This beam (which is typical of all 24) is arranged to give maximum response to signals arriving from the direction shown (that is, perpendicular to the chord drawn through the outermost aerials of the array). The maximum possible response would occur if the signals at the array aerials were in phase; however, as the aerials lie on the arc of a circle, the signals will not be in phase. The method used for optimizing the response is to introduce time delays (in the form of coaxial cable) into the signal paths.[5] These delays equal the various times that a wave, travelling in the direction shown, would take to traverse the distances D_1, D_2 and D_3. The amounts of these delays are slightly modified by optimizing the beam for reception from a small arbitrary elevation angle, in this case 15°, so as to take better account of signals arriving from a range of elevations.

The adjacent beam is formed from the group of eight aerials obtained by stepping round the circle by one aerial. Thus the beam shown in Fig. 2 uses aerials 3–10, the next beam uses aerials 4–11 and so on. There is thus an angle of 15° in azimuth between the best direction of response of adjacent beams. It can now be seen that each aerial is employed in eight independent roles as one element in eight of the beam arrays. It may also be noted that in two of these roles its signals are undelayed; and, in the case of the other six, the amounts of the delays to be imposed on its signals fall into three pairs of different values. This enables the beam-forming system to be built using only three delays per aerial.

Figure 3 indicates schematically the use of a hybrid transformer unit as a means of splitting signal-energy equally into two paths and also as a technique for combining two signals.

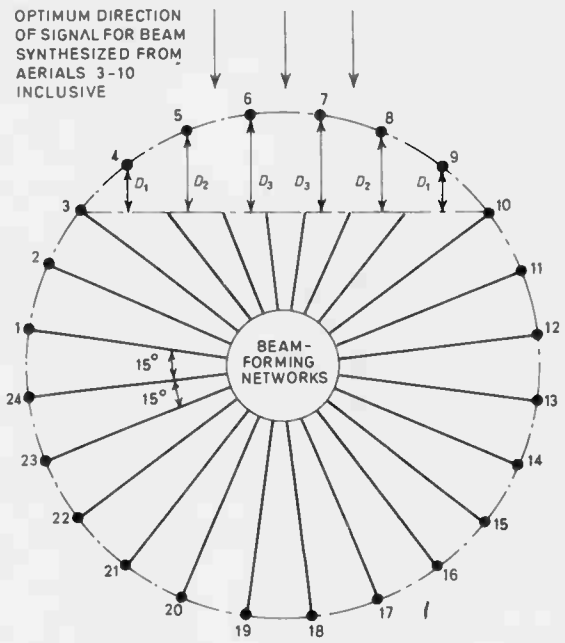


Fig. 2. Schematic plan of system.

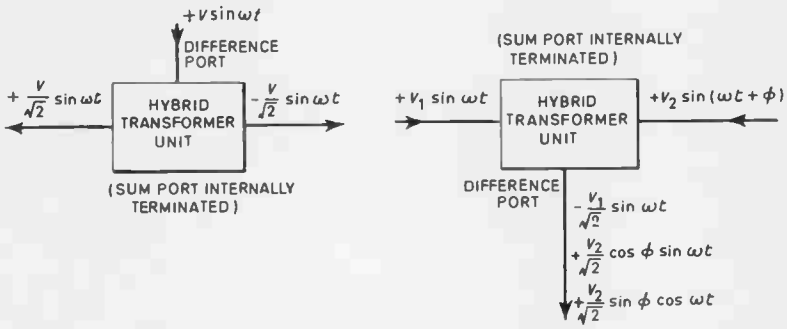
The aerial system comprises:

(i) 24 elevated feed monopoles equispaced on a 500 ft (153 m) diameter circle.

(ii) 24 feeder cables, of equal electrical length, joining the aerials to the beam-forming networks.

(iii) Beam-forming networks synthesizing 24 beams at 15° intervals in azimuth. Each beam is a combination of the signals from 8 adjacent aerials (for example, from aerials 3–10 inclusive, as shown).

The hybrid is shown in its 'difference' form, that is, the energy of signals having equal frequency and amplitude, applied in antiphase to its side ports, would ideally all appear at the third port when this is terminated in its design impedance. The fourth, or 'sum', port of the hybrid is not used in the present application and is permanently resistively-terminated.



(a) As signal splitter.

(b) As signal combiner.

Fig. 3. Use of hybrid transformer unit.

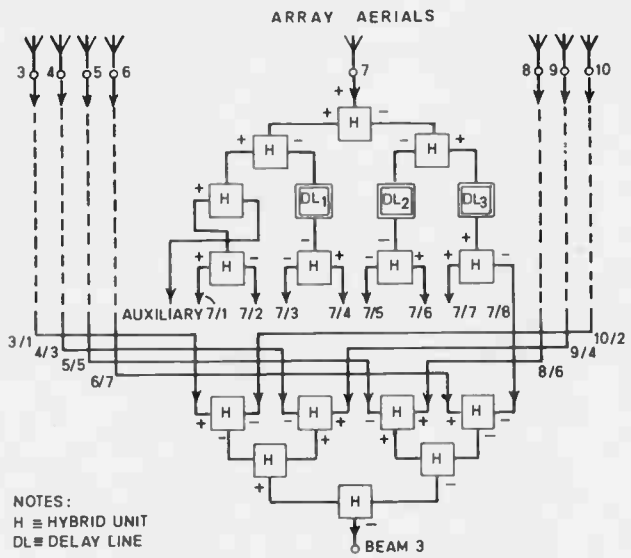


Fig. 4. Typical portion of beam-forming networks.

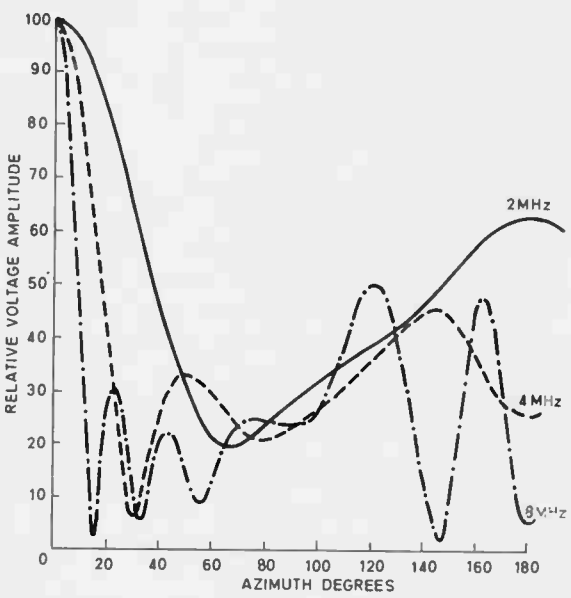


Fig. 5. Theoretical beam responses.

Notes: (i) 24 aerial elements per circle.
(ii) 8 aerial elements per array.
(iii) Array optimized to 15° elevation.

Figure 4 illustrates a typical portion of the beam-forming network; it will be observed that it consists largely of many such hybrid units. The manner of splitting the signal from each aerial into eight independent ways can be seen in the top centre of the figure where it may also be noted that delay lines are inserted in three of the paths, these paths being subsequently divided into six. The undelayed paths are slightly complicated because, when the system was being planned, it was thought worthwhile to make available an aerial auxiliary output at reduced power level (approximately 9 dB). An extra splitting hybrid has therefore been introduced and the undelayed outputs are consequently at a level 3 dB below that of the delayed outputs. This marginally broadens the beam width which is a useful factor at the top of the frequency band.

The bottom centre of Fig. 4 shows how a beam is synthesized. Eight signals, one from each of eight adjacent aerials and appropriately chosen for delay and polarity, are added together in a group of seven hybrid transformer units. Ideally, the beam output power for a signal received from the optimum direction would be the same as that of one aerial. Allowing for the amplitude taper of the outside aerials and the losses in the hybrid units and delay cables, the beam output is less than 3 dB down on an aerial output.

Figure 5 indicates the expected responses of a beam, calculated at 2, 4 and 8 MHz, and making the assumption that there is no mutual impedance interaction between the aerials. The practical conditions were found to approach this theoretical condition very closely as shown in the following experiment. A series of checks measuring the aerial feed-point impedance under various conditions was undertaken over the frequency band. These conditions were with the aerial (a) by itself and (b) in the presence of a similar aerial whose feed-point was, in turn, (i) open-circuited, (ii) short-circuited and (iii) terminated in a 400 Ω resistor (the working load). The two aerials were separated by a distance corresponding with the spacing of adjacent aerials in the circular array. The impedances recorded under tests (a), (b) (i) and (b) (iii) were identical at each frequency, within the limitations of the measurement technique, whereas the values obtained with the ancillary aerial short-circuited (case (b) (ii)) were noticeably different over the band. The effective interaction due to mutual impedance between adjacent aerials when terminated in their working load of 400 Ω was therefore adjudged as negligible. A series of practical tests using a transmitter at short range gave good confirmation of the theoretical predictions. It can be seen from Fig. 5 that the limitations of the system, with regard to beam-response, are poor front-to-back directivity and a very broad main beam at the bottom of the band, and too narrow a main beam as the frequency is increased much beyond 8 MHz. Above 8 MHz, in particular, adjacent beams would fail to overlap sufficiently for the system to provide good all-round azimuthal coverage.

3. Description of System Units

The various pieces of the system are described below. The type of aerial[1] selected was an elevated feed monopole,[6] 42 ft (12·8 m) high, having its feed-point at 10·5 ft (3·2 m) (i.e., at one quarter of the aerial height) above ground. The aerial is of an economical structure consisting of galvanized steel tubes and lattice work, and a glass fibre insulated section joins together the upper and lower parts at the feed-point. It is a simple matter to erect or lower the aerial, which is held in position by means of guy ropes attached to its top and mid-point. Various factors contributed to the choice of the elevated feed arrangement in preference to the use of a ground feed-point. For instance, the elevated feed aerial has better low-angle cover, particularly at the upper end of the band. Secondly, measurements suggest that the impedance of the aerial is more independent of variations in ground conductivity than its ground-fed equivalent. The elevated feed aerial may also be used to advantage on ground subject to flooding or on saltings.

In choosing a suitable aerial element for use in a broadband receiving system, the question of tuning out the reactive part of the aerial's impedance does not arise. It follows that for a given field strength, the power delivered by the aerial into a resistive load of fixed value depends upon the load, the size of the aerial and the frequency. If a very short element is used, its effective height is small and a small aerial e.m.f. results. The impedance of an aerial very much shorter than a quarter-wavelength comprises the radiation and loss resistance in series with a very large capacitive reactance: the reactance and not the resistance would thus be the determining factor in the amount of power delivered to the load. From these considerations, it became clear that the practical approach would be to use an aerial having its lowest impedance condition, that is, its quarter-wave point, near the middle of the frequency band. The band centre was 4 MHz, but an aerial a quarter-wave long at this frequency would be at half-wave resonance (high impedance and therefore relatively insensitive) at 8 MHz. Accordingly, the aerial was arranged to be at quarter-wave resonance at some frequency above 5 MHz. The use of standard lengths of lattice work for the aerial fixed the quarter-wave point at 5·5 MHz and the half-wave point, out of band, at 11 MHz.

The aerial-end of the feeder cables presents substantially a 75 Ω resistive load (i.e. the input impedance of the beam-forming networks) and the best impedance match to the aerial was arrived at on a compromise basis for the whole band. Measurements of the aerial impedance at various frequencies indicated that the most uniform power transfer between 1·5 and 10 MHz, assuming a constant aerial e.m.f., would be achieved by loading the aerial with 400 Ω (using a 400 : 75 Ω transformer). Such a loading has the effect of optimizing the power transfer at the band edges at the expense of that at the band centre where the aerial is at quarter-wave (that is, low impedance) resonance. The importance of extracting maximum signal power from the aerials at the upper frequencies has to be stressed because, in this region, the external noise level is falling off and externally noise-limited conditions are less likely to be realized. The choice of a 400 Ω load for the aerials provides an additional benefit, namely that the small amount of mutual impedance existing between adjacent aerials, which might be expected to modify the shape of the directivity pattern, can be almost entirely discounted in practice, as mentioned in Section 2.

An adjustable air spark gap is connected across the primary winding of the transformer to give protection against induced lightning discharges. A gap of 0·004 in (0·10 mm) was chosen, which breaks down for potentials greater than 1 to 1·5 kV.

In a system of this kind it is important that all corresponding r.f. connections be of equal electrical length so that the phase relationships between the aerial signals are preserved. For the short interconnections in the beam-forming cabinet, their equal physical lengths have proved to be accurate enough. On the other hand, the aerial feeder cables are some 280 ft (85 m) long and it was therefore necessary that their lengths be equated in electrical terms. It is estimated that the overall phase tolerance on the cables lies within a range of 4° at 10 MHz.

It is mentioned in Section 2 that the splitting and recombining of the signals is accomplished by the use of hybrid transformer units, in this case of 75 Ω impedance. The units were constructed by using small blocks of ferrite pierced with two holes through which the windings were passed. These units have very low winding and core losses (0·25 dB typically) and the overall splitting and recombining loss in forming a beam is only about 1·5 dB. If the signal 'difference' and 'sum' ports of a hybrid are reasonably well terminated and the coupling factor between the windings is high (a property available when using these ferrite blocks), the hybrid has the useful attribute of good signal isolation between its side ports. The 'difference' port is employed in preference to the 'sum' port because it is a simple matter to establish the former's impedance at the required value (75 Ω) by the correct choice of transformer turns ratio. Use of the 'sum' port, on the other hand, would demand an additional impedance transformer to yield a 75 Ω input resistance. The 'sum' ports in the present system are terminated in non-inductive, 1% tolerance,

37·5 Ω resistors. The isolation feature is particularly important in summing together the signals from the various aerials in that it minimizes unwanted cross-talk between the signal paths. The isolation property (at least 30 dB) is related to good phase coherence between input and output ports. When discussing the r.f. cables in the previous paragraph, the necessity for preserving the phase relationships was stressed; the hybrids also give very good results in this respect. As an example, it was found possible to achieve and repeat phase coherence for the eight paths of the recombining unit of better than 8° over the band. A computer program was run to check the effect of these errors on the beam pointing direction. A normal distribution of phase errors in hybrids and cables was assumed, with a standard deviation corresponding to 10° of phase at 8 MHz. The distribution was quantized and a random selection of errors taken. Fifty such selections were made and the beam pointing errors were found to lie within the acceptable range $\pm 1°$ of azimuth.

In the design of receivers and receiving systems, particular care has to be taken to maintain the odd-order intermodulation products of incoming signals at as low a level as possible. This is because the interaction between two signals of frequency f_1 and f_2 in a non-linear circuit generates products (amongst others) at frequencies $2f_1-f_2$, $2f_2-f_1$ (third-order), $3f_1-2f_2$, $3f_2-2f_1$ (fifth-order) and so on. The frequencies of the signals, f_1 and f_2, may lie within the receiver's band, for example, as in the case of two transmissions or as in the case of side-bands of a single transmission. When this is so, the frequencies of the above odd-order products approximate to f_1 (or f_2) and appear as in-band distortion which may significantly reduce the signal/noise ratio in the receiver. Normally, if the third-order products are small enough, higher order products may be neglected. For these reasons, the linearities of the hybrids are of importance. The third-order intermodulation product levels created in a hybrid by two 1 V e.m.f. signals have been measured and are lower than 300 μV, that is, better than 70 dB down. This is satisfactory performance for such unusually large signals: the products for two 100 mV signals would fall to 0·3 μV (110 dB down).

Figure 6 illustrates the beam-forming cabinet. The recombining boxes occupy the top three rows and the splitting boxes are immediately below.

The delay lines can be seen in the bottom of the cabinet. These are pieces of coaxial cable coiled into reels, made to the correct electrical length as measured at some suitable frequency in the band. The cables also introduce a small attenuation of the signals, but the effect on the beam pattern is negligible.

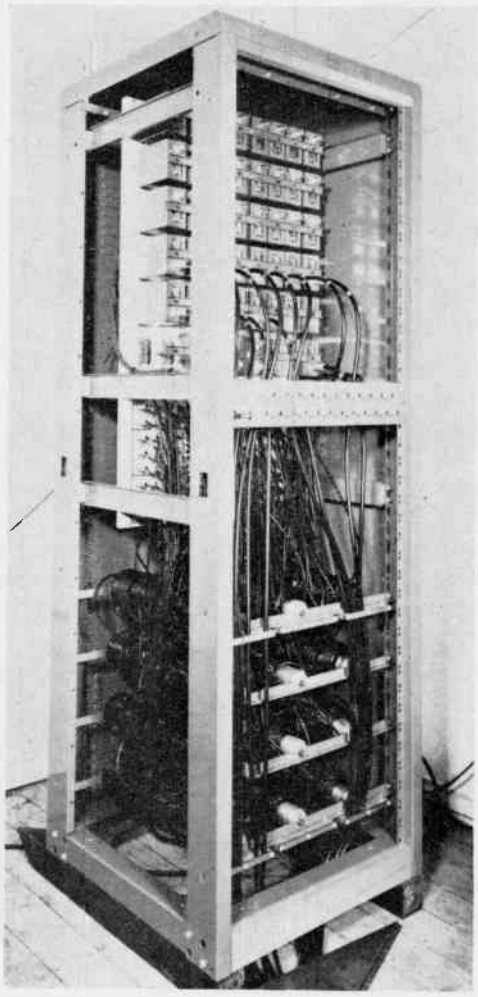


Fig. 6. Beam-forming cabinet.

In this context, it should be noted that the 3 dB amplitude taper on the outermost aerials of each array caused by the provision of the aerial auxiliary output gives a small broadening of the beam width—a useful effect at the top of the band. Referring to Fig. 3(b), it may be noted that the loss of power at the difference port incurred by unequal inputs depends upon the relative values of V_1 and V_2 and the value of φ. In the present case where φ is arranged to be 180°, the loss resulting in combining eight signals to form a beam (see the lower part of Fig. 4) is approximately 0·7 dB in addition to the hybrid transformer losses of 1·5 dB mentioned above. No incorrectness of phasing is caused by the unequal signal inputs.

Each of the beam signals produced by this equipment is independent of the others and may be used to drive an h.f. receiver directly. In addition to the system described, an ancillary unit has been devised

to sample each beam output in turn. This, in conjunction with a receiver tuned to the required signal, provides the operator with a histogram type of display on a cathode-ray tube indicating the relative signal levels of each beam. This immediately enables the best beam to be selected.

If a receiving station having several operators employed this aerial system, it might be inconvenient to house the staff in the hut used for the beam-forming networks. In this case the 24 beams would be fed along individual feeder cables to the main building. The signals could be passed through band-pass filters to corresponding broad band amplifiers and splitter and selector units so that any of the operators could use any of the beams at all times.

4. New Developments

Work is currently proceeding on the problems of extending the frequency range of the aerial system to cover the band from 1·5 to 30 MHz. The existing design fails above 10 MHz chiefly because the beam width becomes too narrow and adjacent beams do not overlap sufficiently to give good all-round coverage. Another factor is that the zenithal directivity pattern of the 42 ft (12·8 m) aerials would be multi-lobed and less suitable for low angle reception at the upper extremes of the band.

It is thought that an elegant solution for the band 10—30 MHz would be to use a second concentric ring of physically shorter aerials on a smaller diameter in conjunction with a further set of beam-forming networks. Mutual impedance tests suggest that the performance of one ring would not suffer in the presence of the other.

The networks for the smaller ring of aerials would, however, take up much the same volume as those of the original system. Only the delay lines would be altered in size to correspond with the smaller circle. The coils of delay cable and their associated connections in the original equipment occupied rather more than half of the cabinet space and the system is being re-examined to see whether it would be possible to employ lumped constant delay lines in place of lengths of cable. A study of the problem indicates that lumped constant delays can be constructed to the required accuracy with good phase linearity (that is, constant delay over the frequency range). Furthermore, they exhibit a lower attenuation than that obtainable from the coaxial cables used hitherto. These lumped constant delays would be small enough to fit into the boxes containing the signal-splitting hybrid units. In this way, it should be possible to fit all the beam-forming networks for the whole band 1·5—30 MHz into the same size of cabinet used for the original system.

It would be a simple matter to combine each upper frequency beam with the corresponding lower frequency beam via suitable band-pass filters to enable the composite signals to be fed along a single set of 24 feeders to the receiving station.

5. Conclusion

The circularly-disposed aerial system described provides good directivity combined with all-round azimuthal coverage for reception in the frequency band 1·5–10 MHz whilst occupying only one-tenth of the area of a corresponding conventional rhombic aerial system. Although unsuitable for transmitting purposes, it gives excellent receiving performance and, generally speaking, provides externally noise limited conditions when using receivers having noise factors in the region of 10 dB and below. The system is entirely passive. Limited tests have indicated, on the basis of an analysis of error rates, that this system is as good as a rhombic array.

6. Acknowledgments

The author would like to thank the Ministry of Technology and the Plessey Company Limited for permission to present this paper.

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Manuscript first received by the Institution on 21st May 1968 and in final form on 15th December 1968. (Paper No. 1251/Com.10).

Conference on 'Lasers and Opto-Electronics'

The first major Conference on lasers and their applications to take place in Great Britain for five years was held at the University of Southampton from 25th–28th March. Organized by the Institution of Electronic and Radio Engineers with the association of the Institution of Electrical Engineers (Electronics Division), the Institute of Physics and the Physical Society, and the Institute of Electrical and Electronics Engineers (United Kingdom and Republic of Ireland Section), the Conference was also supported by the University itself, through its Electronics Department. Southampton is indeed a most appropriate venue for such a Conference since it has one of the strongest university teams working on lasers and opto-electronics in this country; Professor W. A. Gambling who is concerned principally with this work and is also a Vice-President of the I.E.R.E., was Chairman of the Joint Organizing Committee.

The emphasis of the theme of the Conference, as set out by the Organizing Committee, was to lie on applications having relevance to electronic and radio engineering and the Conference divided broadly into two halves, the first two days dealing mainly with the basic theory and techniques of lasers as devices, while the second half dealt mainly with applications. Attendance however was uniformly high throughout the Conference and registrations totalled 375. It was apparent from the list of participants that work on lasers and opto-electronics is taking place in many countries; papers came from France, Germany, Holland, Italy, Switzerland, U.S.A. and the U.S.S.R., while in addition a further ten countries were represented in the audience. This international attendance gave added point to the Conference being mainly residential, and ample opportunities were given for informal discussions outside the framework of the sessions.

Among the informal events of the Conference were a Cocktail Party on the first evening which was followed next day by the Conference Dinner held at a hotel in Southampton. The chair at the Dinner was taken by the President of the I.E.R.E., Major General Sir Leonard Atkinson, who was supported by the President of the I.E.E., Professor J. M. Meek, and the Chairman of the I.E.E.E. Section, Professor J. R. Mortlock. In his speech welcoming overseas visitors Sir Leonard also paid tribute to the contributions of the authors of papers to the success of the Conference to which a reply was made by Professor A. F. Gibson of the University of Essex. The third speech, replying on behalf of the Institutions and the University to Professor Gibson's toast, was made by Professor G. D. Sims, Dean of the Faculty of Engineering at the University of Southampton and himself a member of the two engineering Institutions.

Apart from these primarily social occasions, demonstrations and exhibitions of lasers and opto-electronics equipment were given during each day and on two evenings. The laboratories of the Department of Electronics also attracted much interest when they were opened for visits on the final afternoon of the Conference.

Among the applications which led to considerable discussion were those related to storage of information, often using holographic techniques. The stored information is usually in the form of characters on a photographic plate and the laser beam is employed to scan the hologram and extract information which has been packed together into an almost unbelievably small area. The potentialities of this type of optical storage which has a capacity far larger than magnetic stores of similar access times was particularly remarked upon by Earl Mountbatten of Burma when he gave a closing address on the final day of the Conference. Lord Mountbatten also made mention of another application of opto-electronics which he believed had even greater immediate value, namely the development of communications systems using optical glass fibres. There are of course many problems to be solved before the optical fibre waveguide can be regarded as the competitor of present day techniques in high-capacity long-distance communications, but most of these problems are associated with the study of fibre-forming conditions and glass materials. Bearing in mind the achievements in semi-conductor materials technology since the invention of the transistor it seems probable that practical systems are not very far away in time.

It is hoped to collect together the majority of the 74 papers read at the Conference and to prepare a final volume of 'Proceedings' during the course of the next three or four months. An announcement about the availability of this volume, including its price, will be made in the *Journal* shortly. In addition to the papers listed in the February issue of *The Radio and Electronic Engineer*, this volume will contain the following papers which were added to the published programme.

'Mode Locking of the Neodymium Relaxation Laser by Loss Modulation'. A. C. Selden and G. Magyar, *Royal Holloway College.*

'Mode Conversion and Transmission by a Circular Aperture'. O. O. Andrade and G. C. Thomas, *University of Southampton.*

'Band Pass Filter Using Coupled Open Resonators'. P. F. Checcacci and A. M. Scheggi, *Istituto di Ricerca sulle Onde Elettromagnetiche, Florence.*

'Interaction Mechanisms of Laser Transitions in Argon and Krypton Ion Laser'. A. Ferrario, A. Sironi and A. Sona, *Laboratori C.I.S.E.*, and *University of Milan.*

'Vibrational Energy Transfer in CO_2 under Laser Conditions With and Without Water Vapour'. R. J. Carbone and W. J. Witteman, *Philips Research Laboratories, Eindhoven.*

'Gas Lasers for the Far Infra-Red'. E. J. S. Becklake and M. A. Smith, *E.M.I. Electronics Ltd., Wells.*

'Semiconductor Diodes as Detectors and Mixers at Sub-millimetre Wavelengths'. C. D. Payne and B. E. Prewer, *E.M.I. Electronics Ltd., Wells.*

'An Electro-optic Polarization Modulator'. Th. H. Peek, H. de Lang and G. Bouwhuis, *Philips Research Laboratories, Eindhoven.*

'A Simplified Real-time Optical Matched-filter'. C. Atzeni and L. Pantani, *Istituto di Ricerca sulle Onde Elettromagnetiche, Florence.*

'Underwater Acoustic Holography'. J. R. Coldrick, *B.A.C. Ltd., Guided Weapons Division, Bristol.*

'Speech Recognition Using Optical Filtering'. D. Leverington, *B.A.C. Ltd., Guided Weapons Division, Bristol.*

'Evaluation of the Visibility Improvement in the Fog by the Range Gating Technique'. S. Donati and A. Sona, *Laboratori C.I.S.E., Milan.*

U.D.C. 621.396.677

Helix Antenna for Spacecraft

ALLEN DAS, M.Sc. †

Summary: This paper describes the development and performance of a light-weight, high-gain, high-efficiency, rigid helix antenna and discusses a light-weight deployable helix antenna.

The weight of the rigid helix was 0·16 kg (0·35 lb) and had a measured gain of 16·5 dB at 2·3 GHz. The estimated weight of the deployable helix is 0·06 kg (0·13 lb). Such antenna elements can be used for phased arrays for spacecraft.

1. Introduction

Many applications may require the use of phased arrays on spacecraft, for example, ballistic missile defence system, direct television broadcast, Data Relay Satellite (DRS) to mention a few of them. The phased arrays for spacecraft require a high-gain, light-weight antenna, and a 16-dipole antennule[1] and a helix[2] have been recommended for the antenna element for the DRS phased array. The estimated weight of the antennas are 0·36 kg and 0·34 kg (0·8 and 0·75 lb), respectively.

A theoretical and experimental study has been reported[3] resulting in the development of a dual circularly polarized disk-on-rod antenna using a unipole cavity feed and operated over a 1·775 to 1 bandwidth (225 to 400 MHz), with gain between 10 dB and 14·7 dB. A full-scale (4·1 m or 13·56 ft long) deployable disk-on-rod element weighing 0·14 kg (0·31 lb) was designed, developed, and fabricated. *Nitinol* metal, which exhibits a memory characteristic, was used in the deployment mechanism. The power required for space deployment for each antenna is 0·6 W. From the considerations of the electrical characteristics and the physical size, the helix was selected as a suitable antenna element for phased arrays for spacecraft.

2. Design Considerations

One of the most important considerations in the design of any phased array is the choice of the radiating element. From the point of view of the electrical performance over the frequency band, the element characteristics of interest are: gain, impedance, beamwidth, mutual coupling, polarization and efficiency. From the point of view of the environments (from launch until operation in orbit) the element characteristics of interest are the weight, the structural integrity and the packaging factor. The thermal effects, in orbit, may have an important bearing on the electrical characteristics of the antenna.

The following elements were considered: (i) helical antenna, (ii) disk-on-rod antenna, (iii) horn antenna, (iv) array of crossed slots and, (v) array of crossed dipoles. In Table 1, the relative performance of these alternative elements are compared on a qualitative basis for most of the characteristics of interest. On the basis of the results of this evaluation, the helical antenna element was chosen for a phased array for a particular spacecraft application.

A detailed study is required to determine the optimum number of elements necessary for obtaining a specified gain for a phased array. A high-gain element is necessary to reduce the number of elements, but, for a number of reasons, the efficiency of the high-gain helix decreases as the gain increases. Although the optimum gain per element has not been determined, a 16·4 dB directive gain was chosen as a compromise for a particular design for a phased array element. A 28 cm (11 in) effective aperture diameter at 2·28 GHz corresponds to this directive gain.

The helical antenna has enjoyed widespread use as an element for radiating electromagnetic waves over a broad spectrum of frequencies for twenty years or more. When the dimensions in terms of the wavelength are properly chosen, it operates as an end-fire beam radiator of circularly-polarized waves. Consider the design[4] of a 23-turn light-weight helix at the mid-band frequency of 2 GHz, ($\lambda = 15$ cm). The parameters of interest are then as follows:

diameter of helix $= 0{\cdot}32\lambda = 4{\cdot}8$ cm (1·9 in),
turn spacing $S = 0{\cdot}22\lambda = 3{\cdot}3$ cm (1·3 in)
helix length $L = nS = 75$ cm (30 in),
$\theta_{HP} = (52°)/[(C/\lambda)(\sqrt{nS/\lambda})] = 23°$,
directivity gain $= 15(C/\lambda)^2(nS/\lambda) = 76$ or 18·8 dB

where C is the circumference and n is the number of turns of the helix antenna.

3. Construction and Results

The helix was made of aluminium tubing of outer diameter 3·18 mm (0·125 in) and 0·5 mm (0·02 in) wall thickness wound on polyfoam mounted on an

†Formerly with TRW Systems, Redondo Beach, California, U.S.A.

Table 1 Qualitative comparisons of antenna elements

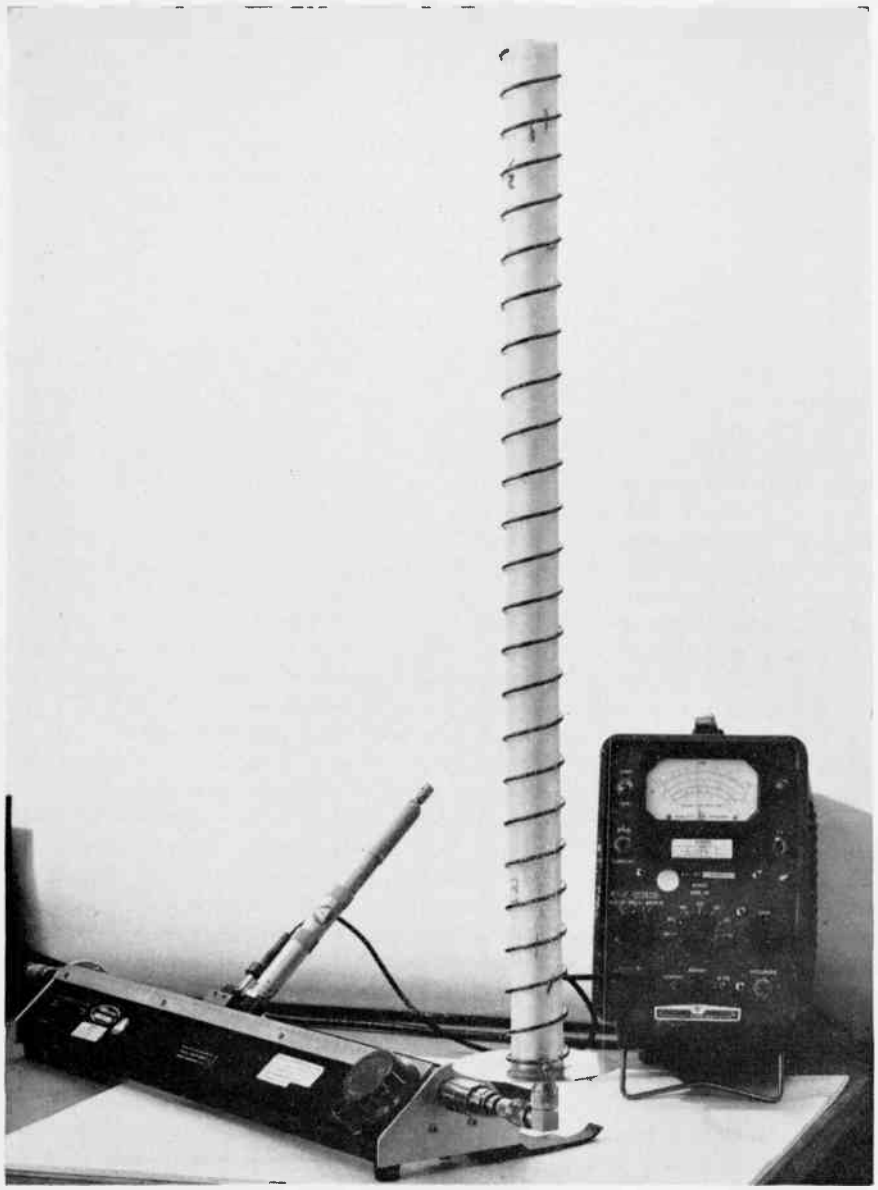
	Helix	Disk on rod	Horn	Crossed dipole array	Crossed slot array
Gain	excellent	excellent	good	poor	poor
Efficiency	good	good	excellent	good	good
Beam width	good	good (rigid)	good	poor	poor
Polarization	excellent	good	good	good	poor
Lack of mutual coupling	excellent	excellent	good	poor	poor
V.s.w.r. over operating band	excellent	good	good	poor	poor
Packing factor	good (deployable) poor (rigid)	good (deployable) poor (rigid)	bad	good	excellent
Weight	good	(see packing factor)	poor	poor	good
Dimensions	(see packing factor)	poor	bad	good	excellent
Structural integrity	(see packing factor)	(see packing factor)	good	excellent	excellent

Table 2 Performance of 24-turn helix

Frequency GHz	V.S.W.R.	Measured beamwidth	Equivalent aperture diameter	Directive gain, dB (calculated)	Measured gain dB	Axial ratio (boresight) dB
1·8	1·7	38°	10.5″	14·1	13·4	0·2
1·85	1·6	36°	10·8″	14·5	13·4	0·2
1·9	1·6	34°	11″	14·9	—	—
2·0	1·65	31·8°	11·1″	15·4	14·5	0·6
2·21	2·1	25°	12·4″	17·4	16·3	0·3
2·25	1·9	23·7°	12·9″	17·7	16·2	0·2
2·30	2·0	21·7°	13·8″	18·5	16·5	0·8

aluminium plate. The outer diameter of the helix was 4·7 cm (1·83 in). A quarter-wave transformer, made from the end of the helix, was used for impedance matching. The weight of the helix was 0·16 kg (0·35 lb) with the N-type connector and 0·11 kg (0·25 lb) without the connector. A photograph of the antenna is shown in Fig. 1(a).

The results of the measurements are listed in Table 2. The measured pattern, impedance, and gain characteristics show that the electrical operational requirements can be met with an appropriately designed helical antenna. The v.s.w.r. results shown in Table 2 are not representative of the best values that can be obtained. For the purpose of these tests, an optimum



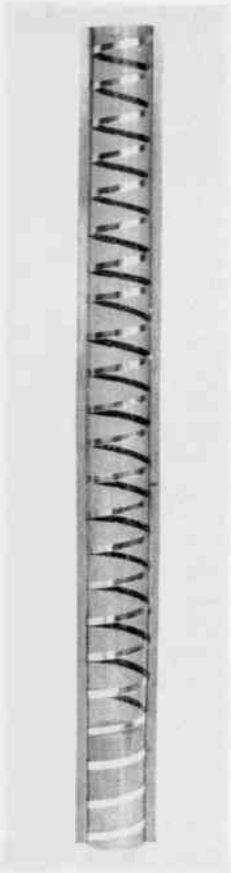


Fig. 1(b) (*above*). Deployable helix.

Fig. 1(a) (*left*). High-gain, light-weight, rigid helix antenna.

matching network was not necessary. The polarization characteristics of the helical antenna with respect to its ellipticity ratio are excellent as can be seen from Table 2. A representative radiation pattern of the antenna beam is shown in Fig. 2. Since the pattern was obtained with a rapidly rotating linearly polarized transmitting antenna while the circularly polarized test helical antenna was rotated in azimuth, it can also be seen that the ellipticity ratio characteristics are excellent over the entire beam. Both the equivalent aperture diameter and the directive gain of uniformly illuminated circular aperture were theoretically calculated from the corresponding measured 3 dB beamwidth. The measured gain includes the reflection loss due to the antenna v.s.w.r. Additional measurements were made on the same test helical antenna with two turns removed. This tended to increase the efficiency of the antenna. The results are shown in Table 3.

4. Deployable Helix

The requirement of deploying a large number of helical antenna elements makes it useful that these elements can be extremely light-weight and can be stored in compact volume during launch and then deployed in space. Considerable efforts have been devoted by TRW Systems, in recent years, to the development of new technology for erectile space structures. Significant progress has been made in the

Table 3 Performance of 22-turn helix

Frequency GHz	V.S.W.R.	Measured beamwidth	Equivalent aperture diameter	Directive gain, dB (calculated)	Measured gain, dB	Axial ratio (boresight) dB
1·70	2·1	—	—	—	12·0	0·4
1·75	1·95	—	—	—	13·2	0·5
1·8	1·85	40°	10″	13·6	14·2	0·2
1·85	1·7	38·6°	10·1″	14·0	14·2	0·4
1·9	1·7	—	—	—	14·1	—
2·0	1·65	32·6°	10·9″	15·2	14·3	0·7
2·21	1·9	26°	12·0″	17	16·1	0·2
2·25	2·0	25·3°	12·2″	17·2	16·3	0·6
2·3	1·9	24·1°	12·5″	17·6	16·5	0·6

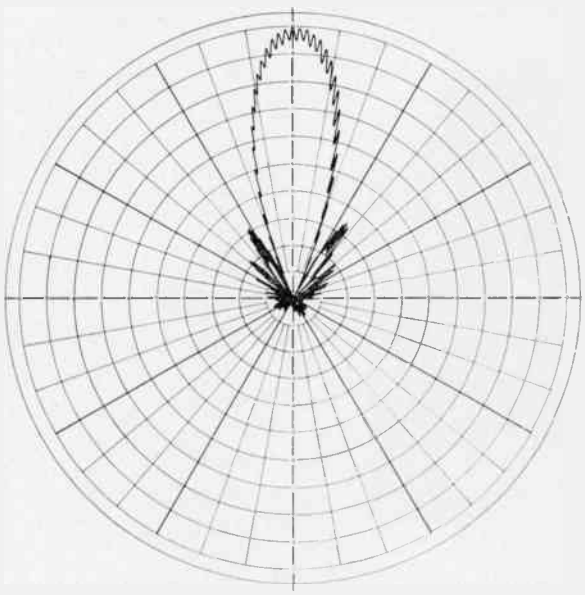


Fig. 2. Azimuthal radiation pattern of the light-weight high-gain, rigid 24-turn helix antenna. Frequency 2·25 GHz.

concept of deploying structures using the stored strain energy. The feasibility of deploying light-weight structures of good stiffness and small storage volume has been demonstrated in several company-funded projects.

The deployable antenna element, shown in Fig. 1(b), basically consists of two parts, namely the supporting tube and the helix. The supporting tube is a strain energy self-erectile thin-wall tube made of electromagnetically-transparent material with high ultraviolet resistance property. At present DuPont's Kapton (polyimide) appears to be a good choice of material. The helical element is attached to the tube. The estimated weight of this antenna to give a 16·5 dB directive gain at 2·28 GHz is 0·05 kg (0·13 lb). The element can be folded over or wrapped around a small spool for stowed configuration. Upon deployment, the tube erects itself and the helix assumes its designed shape. No mechanical contrivance or electrical power is necessary for deployment. The helix is under development and the results will be reported later.

5. Acknowledgments

The author is grateful to Dr. J. W. Duncan and Mr. L. E. Swarts for their support and suggestions, to Mr. C. L. Cooperman for the mechanical design of the rigid helix, to Mr. R. W. Silberberg for the measurements on the rigid helix and to Dr. P. K. Dai for the deployable Kapton tube.

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Manuscript first received by the Institution on 28th October 1968 and in final form on 17th January 1969 (Contribution No. 114/Com 11)..

U.D.C. 621.316.73:537.13

A Proton Resonance Magnetic Field Stabilizer

By

R. A. MORRIS, B.Sc.†

AND

R. G. BROWN†

Presented at the Second New Zealand Electronics Conference (Nelcon II) organized by the New Zealand Section of the I.E.R.E. and the New Zealand Electronics Institute and held in Auckland in August 1968.

Summary: An instrument is described which controls the value of the field strength of an electromagnet by comparing the resonance frequency of protons in that field with a reference frequency and acting to decrease the difference between them. The reference is generated by a digital frequency synthesizer which is so arranged that its dials are calibrated directly in field strength. The method by which this is achieved and some of the circuits used are described in this paper.

1. Introduction

Modern scientific research in such fields as electron spin resonance spectroscopy frequently requires the provision of stable, homogeneous, magnetic fields with field strengths of the order of some thousands of gauss. These requirements are usually met by an electromagnet energized from a stabilized current source. With this arrangement it is possible to obtain stabilities of one part in 10^5 over a period of some minutes. Recent requirements at this Laboratory call for stabilities an order better than this. This paper describes an instrument which was developed to meet these requirements.

Because the field in an electromagnet does not depend solely on the current flowing in the windings, the increased stability could not be achieved by improvements in the stability of the current supply alone. For this reason it was decided to measure the magnetic field directly and to derive a control signal from this measurement. Two methods by which the field could be measured were considered. First was a method relying on the Hall-effect and the second depends on the measurement of the proton resonance frequency of the magnetic field. Hall-effect devices are relatively easy to use, but the measurement is not an absolute one and is subject to drifts. Proton resonance devices are widely used to measure both the absolute value of magnetic fields and their homogeneity but require complex electronic circuitry to produce a direct setting magnetic field controller. The remainder of this paper is concerned with these circuits.

2. General Description

The requirement is for the control of magnetic field strength over the range 3000–3500 gauss (0·3–0·35 tesla) with a stability of 1 part in 10^6 over 10 minutes. Two modes of operation are required: in the first the field has to be set to a given value with a resolution of 10 mG; in the second mode a value of magnetic field, determined by readings taken with the electron spin resonance spectrometer and maintained by current from a stable current regulated supply, has to have its strength determined, and then be locked to this value by the proton resonance stabilizer. For the second mode of operation, it is necessary to use a manually tunable oscillator, incorporating as its tuned circuit a proton resonance probe, to find the resonance frequency of the field. It was decided to use the same oscillator when controlling the magnetic field and to ensure its stability by locking its frequency to that of a digital frequency synthesizer by means of a phase lock loop.

To determine the proton resonance frequency of the magnetic field with respect to the oscillator frequency, it is necessary to modulate either the magnetic field or the frequency. In the experiments for which the magnet is used, the magnetic field is not modulated and hence modulation has to be provided by this instrument. Frequency modulation of the phase-locked oscillator was tried, but the resulting amplitude modulation could not be eliminated. It was therefore necessary to place the proton resonance probe between a small pair of Helmholtz coils and modulate the local magnetic field. The field must be homogeneous to 1 part in 10^5 or better within the volume of the probe to obtain satisfactory signals. The water proton resonance frequencies corresponding to 3000 and 3500 G are 12·77302 MHz and 14·90184 MHz respectively and this is the range the oscillator and synthesizer must cover. The smallest field increment is 10 mG corresponding to 42·5767 Hz and to make the digital synthesizer direct reading in gauss this is the smallest increment of frequency which has to be generated.

3. Circuit Description

A block diagram of the complete instrument is given in Fig. 1. It consists of two main parts: the phase lock frequency loop, and the proton resonance, magnet locking loop.

† Physics and Engineering Laboratory, Department of Scientific and Industrial Research, Lower Hutt, New Zealand.

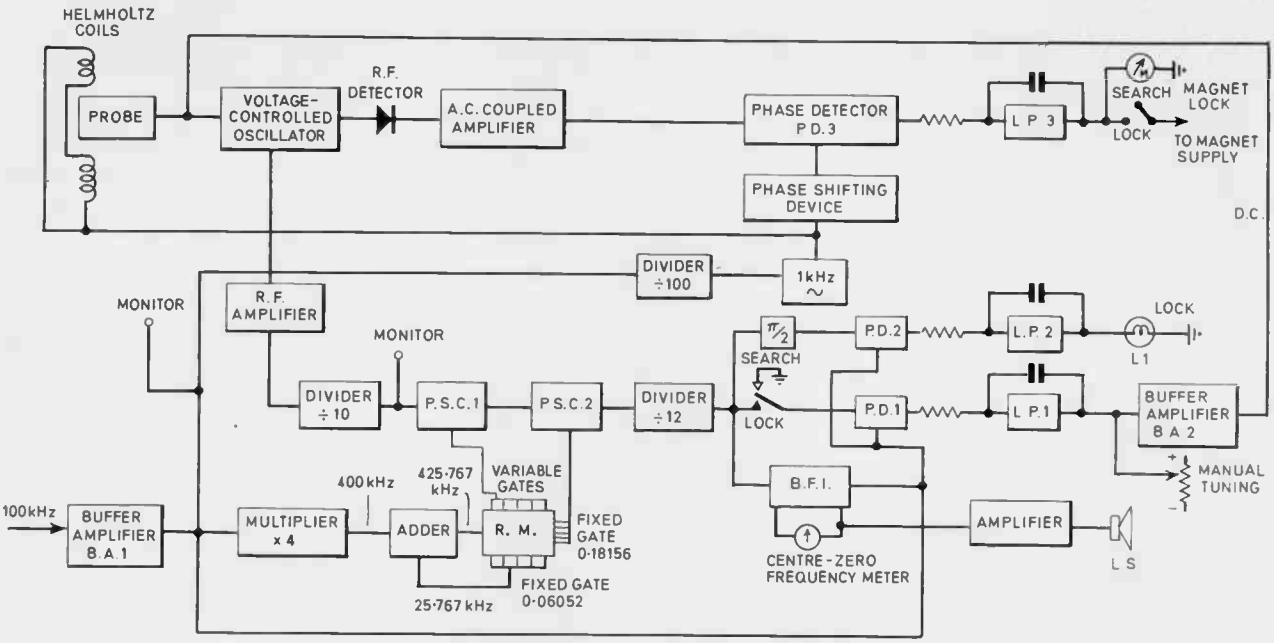

Fig. 1. Block diagram of the proton resonance magnetic field stabilizer.

3.1. *The Frequency Loop*

This consists of a voltage-controlled oscillator (v.c.o.) block (Fig. 1) which is tuned electrically by means of varactor diodes. A signal from this oscillator is amplified in a wideband r.f. amplifier and its frequency is divided by 10 in a digital frequency divider. The output of this divider, in the form of a uniform train of pulses, passes to two identical pulse subtraction circuits (P.S.C.1, P.S.C.2) in series. Each circuit has an input and output line and a subtract line. When a pulse is received on the subtract line from a binary coded decimal rate multiplier (R.M.),† one pulse received from the decade divider is deleted so that there is one less pulse on the output line of the subtractor than there is on the input. The output of the second subtractor goes to a further digital frequency divider where its frequency is divided by 12 (÷12). When the oscillator is locked to the digital synthesizer, the output of this divider passes to a phase detector (P.D.1) where it is compared with a 100 kHz signal derived from a buffer amplifier (B.A.1) and an external frequency standard. For the oscillator to be locked to the digital frequency synthesizer the output of the ÷12 divider must have a frequency of 100 kHz also. The output of the phase detector is smoothed by a low-pass filter (L.P.1), mixed with a voltage from a manual tuning control, and after passing through a second buffer amplifier (B.A.2), controls the frequency of the v.c.o. through varactor diodes. It will be obvious that if the number of pulses derived from R.M. and supplied to the subtractors is increased, then the frequency of the oscillator must also increase if the output of the frequency divider (÷12) is to remain at 100 kHz and the loop is to remain in lock. This is how the digital circuits control the frequency of the oscillator.

Examining these digital circuits in more detail: a 100 kHz signal is received from an external frequency standard and is filtered and passed through a buffer amplifier (B.A.1). Now the smallest frequency step, corresponding to a 10 mG change of field, is 42·5767 Hz which, after a division of 10, corresponds to a frequency increment on the subtract line of P.S.C.1, of 4·25767 Hz. This signal is derived from a five-stage binary coded decimal rate multiplier, the input frequency of which must be 425·767 kHz. A frequency of 425·767 kHz is first synthesized from the 100 kHz input as follows. The input frequency is multiplied by a factor of 4 in the multiplier (×4) to give an output of 400 kHz. This output is converted into a pulse train and is one input to a pulse addition circuit. The output of this adder is the input of R.M. It is assumed that the input to R.M. is 425·767 kHz and a set of fixed gates in R.M., with a fractional value of 0·06052, is used to derive a pulse train with a frequency of 25·767 kHz and this is added to the 400 kHz input in the adder.

With the decade switches of R.M. it is possible to select any decimal fraction of the input frequency with a precision of one part in 10^5. These pulses appear on

† A binary coded decimal rate multiplier is a device which allows an exact fraction of the input frequency to be selected by decade dials and appear as a pulse train on an output line. Such devices have been described extensively in the literature.[1,2]

the variable gates in Fig. 1, and go to the subtract input of the first subtractor (P.S.C.1). The most significant switch of R.M. is limited to the values 0·0 to 0·5 inclusive corresponding to the 500 gauss range which must be covered. With the switches set to zero it is required that the frequency of the oscillator corresponds to the proton resonance frequency of a field of 3000 G, or 12·77302 MHz. This corresponds to a frequency of 1·277302 MHz at the output of the decade divider, and it is necessary to subtract from this value 0·077302 MHz to give a frequency of 1·2 MHz at the input of the ÷12 divider, so ensuring that a 100 kHz pulse train appears at the phase detector (P.D.1). The 0·077302 MHz pulse train is derived from another set of fixed gates with a fractional value of 0·18156 on R.M. By these means the oscillator may be locked in frequency to a frequency standard anywhere in the range 12·77301–14·90184 MHz with a setting accuracy of 42·5767 Hz.

Several subsidiary circuits are provided to help the operator lock the oscillator to the digital synthesizer. Another phase detector (P.D.2) supplied with the same reference as the first phase detector (P.D.1), receives a signal shifted in phase by 90° from that supplied to P.D.1. The action of the phase lock loop is always to ensure that the signal from the ÷12 divider, and the reference signal from the buffer amplifier (B.A.1), are in quadrature so that the output of the phase detector (P.D.1) is a minimum. Because of the 90° phase shift in the signal supplied to detector P.D.2, its output will be a maximum and after smoothing through a second low-pass filter, is used to indicate that the lock condition obtains by means of a lamp L1. For the purposes of acquiring the lock condition, the bandwidth of the first low-pass filter is made approximately 1 Hz, but after frequency lock has been obtained a signal from the second low-pass filter switches in a longer time-constant in the first filter, and so reduces its bandwidth. It is necessary to do this as the signals derived from R.M. are non-uniform in frequency which results in phase jitter on the signal supplied to the phase detector. The output of the detector must be well smoothed to prevent this phase jitter causing frequency modulation of the oscillator.

The oscillator may be manually tuned by means of a ten-turn potentiometer mounted on the front panel. The voltage from this potentiometer is added to that from the first low-pass filter and provides the coarse tuning of the oscillator. When locking the oscillator to the synthesizer it is useful to have an indication of the frequency difference between them. This is provided by the beat frequency indicator (B.F.I.) which compares the output of the ÷12 divider with the 100 kHz reference signal. It provides two indications, one on a centre-zero frequency meter and the other an audio signal through amplifier (A) and loudspeaker (L.S.). When the oscillator is locked the beat frequency indicator and meter function as a phase detector and show the deviation from the quadrature condition of the signal and the reference.

3.2. *The Proton Resonance, Magnet Locking Loop*

The phenomenon of proton resonance is observed in a small bottle containing water which has been doped with ferric chloride to reduce its relaxation time. When this sample is simultaneously subjected to a radio-frequency field and a slowly varying magnetic field it is found that at some value of magnetic field strength the sample absorbs power from the radio-frequency source. This dissipation is due to the phenomenon of proton resonance in the sample. The

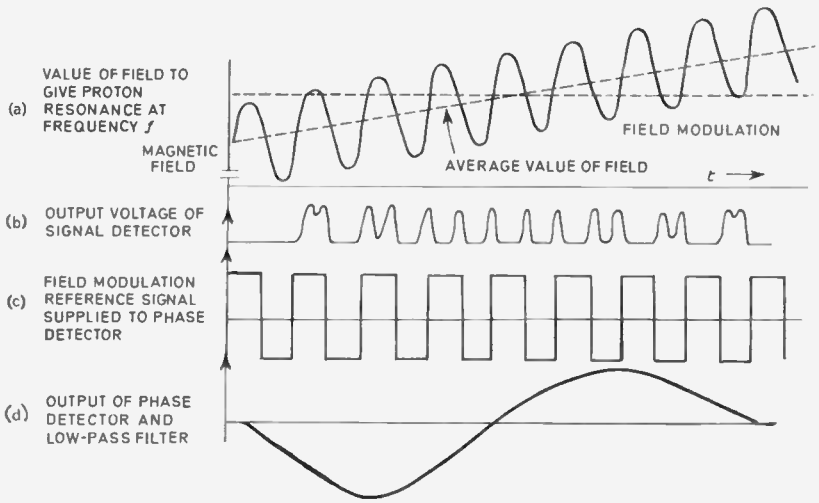

Fig. 2. Generation of proton resonance signal.

radio frequency and the field strength are related by the expression: field strength $= f \times 2{\cdot}34870 \times 10^{-4}$ for protons in hydrogen where f is the frequency in MHz and the field strength is in gauss. It is observed that the line width of the resonant signal is less than 1 gauss wide. The probe consists of the water bottle on which is wound the oscillator coil and this is placed in the centre of a pair of Helmholtz coils which supply magnetic field modulation. The complete probe is placed between the poles of the electromagnet with the field due to the Helmholtz coils aligned with that of the magnet. When proton resonance occurs the radio frequency voltage across the sample coil decreases and it is this decrease of voltage which is detected as the proton resonance signal. Because this effect is small, considerable amplification is required to make it detectable.

The modulation supplied by the Helmholtz coils is sinusoidal, with a frequency of 1 kHz and a peak amplitude of ± 1 gauss. Figure 2 illustrates the signals which are obtained when the proton resonance frequency is swept past the oscillator frequency by slowly increasing the magnetic field. When the magnetic field is within the modulation depth of the value at which proton resonance occurs, two resonance signals will be observed for each cycle of modulation. When the average value of the field is exactly equal to the proton resonance value these two peaks will be equally spaced. It is this condition of equal spacing of the proton resonance signals which is detected by the signal processing circuits consisting of the r.f. detector a.c.-coupled amplifier, phase detector (P.D.3) and low-pass filter (L.P.3). Any deviation from the condition of equal spacing of the proton resonance signals results in a voltage appearing at the output of the low-pass filter which depends in sign and magnitude on the sign and magnitude of the deviation of the magnetic field from the desired control value as shown in Fig. 2(d). This deviation is indicated on a meter (M), and is fed to the regulated current supply of the electromagnet as a supplementary control signal. The proton resonance control loop operates with a loop gain of 100, that is, changes in the magnetic field due to any cause are reduced by a factor of 100 due to the operation of this loop.

The 1 kHz sinusoidal modulation signal is obtained by frequency division ($\div 100$) from the 100 kHz reference signal. A phase-shifting device shifts the phase of the 1 kHz signal supplied as reference to the phase detector (P.D.3) to ensure that its output is zero for the condition that the proton resonance signals are equally spaced.

4. Detailed Circuit Descriptions

Most of the circuits used in this instrument are of standard design and will not be described here. For those wanting a complete description it is available as a publication by the Physics and Engineering Laboratory.[3]

The only circuits which will be described in detail are the pulse adder and the pulse subtractor. These circuits enable a precise number of pulses to be added to and subtracted from incident pulse trains without any overlap or slicing of the pulses.

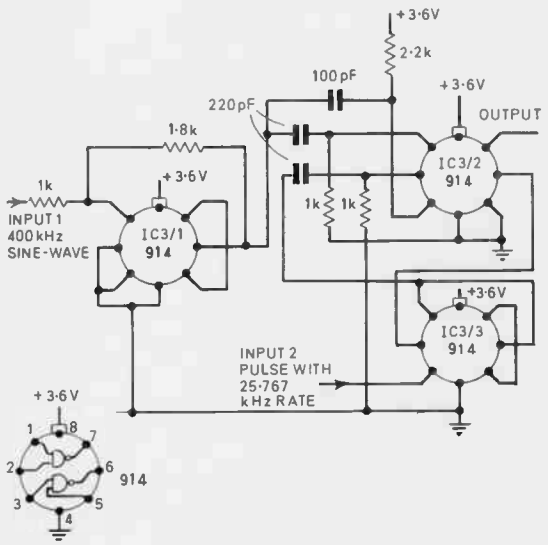

Fig. 3. Pulse adder.

4.1. *Pulse Adder Circuit*

This circuit is shown in Fig. 3 and consists of three integrated circuits IC3/1, IC3/2 and IC3/3. IC3/1 is a Schmitt trigger circuit which converts a 400 kHz sinusoidal input signal to a square-wave at its output. The 400 kHz square wave is differentiated and the short positive pulses applied to pin 1 of the dual two-input gate IC3/2 cause short negative pulses to appear at the output pin 7. Differentiated pulses are also applied to pin 3 which is normally held positive by a fixed bias current so that negative pulses at this input cause positive pulses at the output pin 6. These pulses are of the opposite polarity, and will appear 180° out of phase with respect to the 400 kHz pulses on pin 7. The positive pulses from pin 6 are applied as one input to an R-S flip-flop constructed from another dual two-input gate IC3/3. The other input to pin 3 of this flip-flop is the train of positive pulses which is to be added to the 400 kHz pulse train. When one pulse is received on pin 3, IC3/3, the flip-flop reverses its state causing pin 6 to become positive low. When the next 400 kHz pulse is received on pin 2 IC3/3 the R-S flip-flop returns to its original state, pin 6 goes positive high, and this transition is differentiated and applied to pin 2 of IC3/2, the second input of the gate circuit which is

carrying the original 400 kHz pulse train. This additive pulse will arrive midway between two pulses of the 400 kHz pulse train and be interleaved with them on the output, pin 7 of IC3/2. This output signal goes to the input of the b.c.d. rate multiplier pulse generator. An inspection of the propagation times of R.M. shows that it is impossible for pulses to be received simultaneously on pins 2 and 3 of IC3/3. By these means a pulse has been added to the 400 kHz pulse train with no possibility of pulse cancellation or pulse overlap.

4.2. *Pulse Subtractor Circuit*

This circuit is shown in Fig. 4 and consists of integrated circuits IC4/1, IC4/2 and IC4/3. In the absence of any subtract pulses, the pulses from the ÷10 divider, which are taken to pin 1 of IC4/1, are inverted twice and appear at the output pin 6 and pass

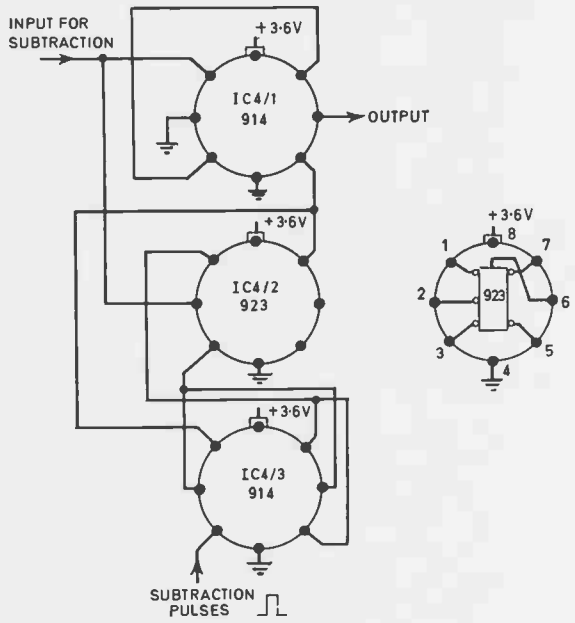

Fig. 4. Pulse subtractor.

on to the next subtractor unit. Thus a positive high signal at pin 1 produces a positive high signal at pin 6. The integrated circuit IC4/3 is a dual, two-input gate connected as an R-S flip-flop and in the absence of subtract pulses the pin 6 output is positive high. On the receipt of a positive high pulse, on the input pin 3, the state of this flip-flop is reversed. The two outputs of this flip-flop pins 6 and 7 are connected to the gate inputs pins 3 and 1 respectively of the J-K flip-flop IC4/2. After the receipt of a subtract pulse pin 3 of IC4/2 goes positive low and pin 1 goes positive high. The next negative transition on the count input pin 2 of IC4/2 will reverse the state of this flip-flop. Pin 2 is connected to the output of the ÷10 divider, and because it is positive transitions at this point which produce positive output transitions from the subtractor, pin 6, IC4/1, the transitions of the J-K flip-flop take place at the end of one output pulse from the subtractor and not during a pulse. The transition of the J-K flip-flop results in its output pin 7 IC4/2 going positive high which in turn makes the input pin 5 of IC4/1 positive high. The output pin 6 of IC4/1 is already positive low and it must stay in this condition until the J-K flip-flop IC4/2 has reversed its state. Pin 7 of IC4/2 is also connected to pin 1 of IC4/3 and the positive transition on pin 7 reverses the state of the R-S flip-flop IC4/3 and cancels the effect of the subtract pulse. This reverses the potentials on the gate inputs of the J-K flip-flop IC4/2 so that the next negative transition from the ÷10 divider will reverse its state, but before this transition can take place there is first a positive transition which is now blocked by IC4/2 from producing an output at the subtractor. Thus one subtract pulse has prevented one pulse from the ÷10 divider from reaching the output of the subtractor and it has been done in such a way that there is no possibility of pulse slicing.

There are two limitations on the speed of operation of this circuit: firstly the interval between two subtract pulses must be greater than twice the interval between two input pulses from the divider and secondly the length of a subtract pulse must be less than the interval between two input pulses.

5. Operating Procedure

As mentioned in the Introduction, there are two operating modes for this instrument and its use in the first will be described. A required value of field is set on the synthesizer dials with the phase lock and magnet lock switches in the search position. The coarse tuning control of the oscillator is now swept through its range until zero beat is indicated by the audio monitor, and at this point the phase lock switch is set to the lock position, the oscillator frequency is captured by the synthesizer and this is indicated by the lighting of the 'lock' lamp on the front panel. The magnet current controls are now varied until a proton resonance signal is observed on the meter (M). With the current controls adjusted to bring the meter to the centre of the proton resonance characteristic (Fig. 2(d)), the magnet lock switch is thrown to the 'lock' position and the magnet field will now be locked to the value set on the synthesizer dials. A further slight adjustment of the magnet current controls may be required to bring the meter to exactly zero thereby making the values of the field close to the dial settings. Alternatively these controls allow some interpolation between the 10 mG steps of the synthesizer. With a loop gain of 100 and a stable current supply the

magnetic field has a stability of the order of 10 mG over one hour.

6. Conclusion

An instrument has been described which locks the value of the field strength in an electromagnet to the resonance frequency of protons in that field. The frequencies used to achieve this are synthesized from an external frequency standard of high stability and some of the circuits used to achieve this are described. By use of novel techniques the synthesizer dials may be calibrated directly in magnetic field strength making the instrument direct setting and easy to operate. Due to the small amplitude of the proton resonance signals in comparison with the modulating and digital signals, extreme care is required in the placement of parts, earthing arrangements and the bypassing of d.c. supplies if satisfactory operation is to be obtained.

7. References

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Manuscript received by the Institution on 25th November 1968. (Paper No. 1252/IC4.)

U.D.C. 621.372.63

Matrix Tables for the Generalized 5-Terminal Amplifier

By

J. I. SEWELL,
B.Sc., Ph.D.†
AND
F. W. STEPHENSON,
B.Sc., Ph.D.†

Summary: The paper considers the admittance matrices of the generalized 5-terminal amplifier and shows that the more commonly used amplifiers are special cases of the model. It is noted that the single operational amplifiers are equivalent when included in a network.

The admittance matrices of a number of familiar amplifier networks are listed in the tables.

1. Introduction

Voltage operational amplifiers are familiar active elements in electronics. Their characteristics have been relatively simple to attain using valves and, latterly, transistors.

The present design practice allows the engineer to produce other forms of operational amplifiers such as the transimpedance, transadmittance and current types.

The paper considers these different configurations from a matrix standpoint. The admittance matrices of the various amplifiers are listed and their properties are discussed. It is noted that networks made up from operational amplifiers have transfer characteristics which do not depend upon the particular type of amplifier used.

In the final Section of the paper, the admittance matrices for a number of familiar feedback sections are presented.

2. The 5-terminal Active Device

For the device shown in Fig. 1, it is assumed that the internal feedback terms are zero over the range of frequencies of interest. The definite admittance matrix can be written down immediately. It is logical to use the definite admittance matrix as in the majority of practical cases node 5 is grounded, hence this may be treated as the reference node. The matrix is shown in Fig. 2.

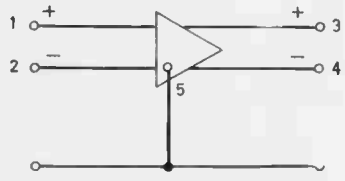


Fig. 1. 5-terminal active device.

In the majority of cases it is reasonable to assume that the common-mode input admittance $y_{12} = y_{21} \to 0$. Similarly, the common-mode output admittance $y_{34} = y_{43} \to 0$. Hence, in the tables developed, these terms are assumed to be zero. If in a particular case this is not true then the appropriate terms should be included.

3. Amplifier Admittance Matrices

3.1. *The Amplifier ABCD Parameters*

Using the amplifier driving point admittances it is of value to derive the remaining admittance entries in terms of certain parameters and these admittances. It is found that only four extra parameters are needed: open-circuit voltage gain A, short-circuit current gain B, transfer admittance C, transfer impedance D.

Thus, in the case of a voltage amplifier the forward transfer admittance $y_{n1} = -Ay_{nn}$ or, for a current amplifier, $y_{n1} = -By_{11}$. For the transadmittance amplifier the only parameter which appears is the transfer admittance C. The forward transfer admittance of a transimpedance amplifier whose transfer impedance is D, is $y_{n1} = -Dy_{11}y_{nn}$, since the amplifier is assumed to be completely non-reciprocal.

3.2. *The Matrix Tables*

These tables are derived from the matrix of Fig. 2 by assuming the arbitrarily assigned voltage polarities as shown in Fig. 1. Tables 1 to 4 give the matrices

	1	2	3	4
1	y_{11}	$-y_{12}$	0	0
2	$-y_{21}$	y_{22}	0	0
3	$-y_{31}$	$-y_{32}$	y_{33}	$-y_{34}$
4	$-y_{41}$	$-y_{42}$	$-y_{43}$	y_{44}

Fig. 2. Admittance matrix for the 5-terminal active device shown in Fig. 1.

† Department of Electronic Engineering, The University of Hull.

for practical and operational cases, the parameter K is a constant which tends to infinity.

Included in these tables are the matrices for the common amplifier configurations, which are obtained by eliminating certain nodes.

An interesting point to note is that the single operational amplifiers are equivalent when included in a network. This can be shown by simple transformation.[1]

The hybrid amplifiers are given in Tables 5 to 7. If there is 1 : 1 conversion from voltage to current, then $A = C$.

3.3. *A Comparison of the Different Types of Amplifiers*

In the physical realization of the various operational types it is obvious that some will be easier to construct than others. With modern techniques using f.e.t.s it is possible to obtain extremely high input resistances (10^{11} Ω) and, for a limited frequency range, $y_{11} \to 0$. The realization of very low output impedances (< 100 Ω) is common practice and application of suitable feedback can produce very low values indeed. Thus $y_{22} \to \infty$, at least in comparison with surrounding network elements, provided denormalization is suitably performed. The voltage operational amplifier is therefore a practical proposition and in fact is the most common type at the present time.

The realization of extremely high input admittances is not particularly difficult with a common-base circuit or with suitable feedback. But zero output admittances present a somewhat more difficult problem, although circuits approaching this (output resistances of the order of 50 MΩ or even 1000 MΩ) are not unknown.[2] This makes the current operational amplifier quite feasible, although, perhaps, rather more complex than the above.

The transimpedance operational type is probably the most suitable of all, i.e. zero input impedance and zero output impedance, both of which can be realized fairly accurately and simply.

The amplifier which presents the most practical problems in construction is the transadmittance one, which requires high input resistance and high output resistance. Although realization of this type is not at all beyond present techniques.

With regard to usage, if the forward gain parameter (voltage, current, impedance, admittance) of an

Table 1 Admittance matrices for the voltage type amplifier

Configuration		General amplifier				Operational amplifier			
		1	2	3	4	1	2	3	4
General	1	0	0	0	0	0	0	0	0
	2	0	0	0	0	0	0	0	0
	3	$-Ay_{33}$	Ay_{33}	y_{33}	0	K^2	$-K^2$	K	0
	4	Ay_{44}	$-Ay_{44}$	0	y_{44}	K^2	$-K^2$	0	K
Difference	1	0	0	×	0	0	0	×	0
	2	0	0	×	0	0	0	×	0
	3	×	×	×	×	×	×	×	×
	4	Ay_{44}	$-Ay_{44}$	×	y_{44}	K^2	$-K^2$	×	K
Paraphase	1	0	×	0	0	0	×	0	0
	2	×	×	×	×	×	×	×	×
	3	$-Ay_{33}$	×	y_{33}	0	$-K^2$	×	K	0
	4	Ay_{44}	×	0	y_{44}	K^2	×	0	K
Single in/out	1	0	×	×	0	0	×	×	0
	2	×	×	×	×	×	×	×	×
	3	×	×	×	×	×	×	×	×
	4	Ay_{44}	×	×	y_{44}	K^2	×	×	K

Table 2 Admittance matrices for the current type amplifier

Configuration		General amplifier				Operational amplifier			
		1	2	3	4	1	2	3	4
General	1	y_{11}	0	0	0	K	0	0	0
	2	0	y_{22}	0	0	0	K	0	0
	3	$-By_{11}$	By_{22}	0	0	$-K^2$	K^2	0	0
	4	By_{11}	$-By_{22}$	0	0	K^2	$-K^2$	0	0
Difference	1	y_{11}	0	×	0	K	0	×	0
	2	0	y_{22}	×	0	0	K	×	0
	3	×	×	×	×	×	×	×	×
	4	By_{11}	$-By_{22}$	×	0	K^2	$-K^2$	×	0
Paraphase	1	y_{11}	×	0	0	K	×	0	0
	2	×	×	×	×	×	×	×	×
	3	$-By_{11}$	×	0	0	$-K^2$	×	0	0
	4	By_{11}	×	0	0	K^2	×	0	0
Single in/out	1	y_{11}	×	×	0	K	×	×	0
	2	×	×	×	×	×	×	×	×
	3	×	×	×	×	×	×	×	×
	4	By_{11}	×	×	0	K^2	×	×	0

Table 3 Admittance matrices for the transadmittance type amplifier

Configuration		General amplifier				Operational amplifier			
		1	2	3	4	1	2	3	4
General	1	0	0	0	0	0	0	0	0
	2	0	0	0	0	0	0	0	0
	3	$-C$	C	0	0	$-K$	K	0	0
	4	C	$-C$	0	0	K	$-K$	0	0
Difference	1	0	0	×	0	0	0	×	0
	2	0	0	×	0	0	0	×	0
	3	×	×	×	×	×	×	×	×
	4	C	$-C$	×	0	K	$-K$	×	0
Paraphase	1	0	×	0	0	0	×	0	0
	2	×	×	×	×	×	×	×	×
	3	$-C$	×	0	0	$-K$	×	0	0
	4	C	×	0	0	K	×	0	0
Single in/out	1	0	×	×	0	0	×	×	0
	2	×	×	×	×	×	×	×	×
	3	×	×	×	×	×	×	×	×
	4	C	×	×	0	K	×	×	0

Table 4 Admittance matrices for the transimpedance type amplifier

Configuration		General amplifier				Operational amplifier			
		1	2	3	4	1	2	3	4
General	1	y_{11}	0	0	0	K	0	0	0
	2	0	y_{22}	0	0	0	K	0	0
	3	$-Dy_{11}y_{33}$	$Dy_{22}y_{33}$	y_{33}	0	$-K^3$	K^3	K	0
	4	$Dy_{11}y_{44}$	$-Dy_{22}y_{44}$	0	y_{44}	K^3	$-K^3$	0	K
Difference	1	y_{11}	0	×	0	K	0	×	0
	2	0	y_{22}	×	0	0	K	×	0
	3	×	×	×	×	×	×	×	×
	4	$Dy_{11}y_{44}$	$-Dy_{22}y_{44}$	×	y_{44}	K^3	$-K^3$	×	K
Paraphase	1	y_{11}	×	0	0	K	×	0	0
	2	×	×	×	×	×	×	×	×
	3	$-Dy_{11}y_{33}$	×	y_{33}	0	$-K^3$	×	K	0
	4	$Dy_{11}y_{44}$	×	0	y_{44}	K^3	×	0	K
Single in/out	1	y_{11}	×	×	0	K	×	×	0
	2	×	×	×	×	×	×	×	×
	3	×	×	×	×	×	×	×	×
	4	$Dy_{11}y_{44}$	×	×	y_{44}	K^3	×	×	K

Table 5 Admittance matrices for an amplifier with hybrid input admittances

Type		General amplifier				Operational amplifier			
		1	2	3	4	1	2	3	4
Voltage output	1	y_{11}	0	0	0	K	0	0	0
	2	0	0	0	0	0	0	0	0
	3	$-Dy_{11}y_{33}$	Ay_{33}	y_{33}	0	$-K^3$	K^2	K	0
	4	$Dy_{11}y_{44}$	$-Ay_{44}$	0	y_{44}	K^3	$-K^2$	0	K
Voltage output	1	0	0	0	0	0	0	0	0
	2	0	y_{22}	0	0	0	K	0	0
	3	$-Ay_{33}$	$Dy_{22}y_{33}$	y_{33}	0	$-K^2$	K^3	K	0
	4	Ay_{44}	$-Dy_{22}y_{44}$	0	y_{44}	K^2	$-K^3$	0	K
Current output	1	y_{11}	0	0	0	K	0	0	0
	2	0	0	0	0	0	0	0	0
	3	$-By_{11}$	C	0	0	$-K^2$	K	0	0
	4	By_{11}	$-C$	0	0	K^2	$-K$	0	0
Current output	1	0	0	0	0	0	0	0	0
	2	0	y_{22}	0	0	0	K	0	0
	3	$-C$	By_{22}	0	0	$-K$	K^2	0	0
	4	C	$-By_{22}$	0	0	K	$-K^2$	0	0

Table 6 Admittance matrices for an amplifier with hybrid output admittances

Type		General amplifier				Operational amplifier			
		1	2	3	4	1	2	3	4
Voltage input	1	0	0	0	0	0	0	0	0
	2	0	0	0	0	0	0	0	0
	3	$-C$	C	0	0	$-K$	K	0	0
	4	Ay_{44}	$-Ay_{44}$	0	y_{44}	K^2	$-K^2$	0	K
Voltage input	1	0	0	0	0	0	0	0	0
	2	0	0	0	0	0	0	0	0
	3	$-Ay_{33}$	Ay_{33}	0	y_{33}	$-K^2$	K^2	0	K
	4	C	$-C$	0	0	K	$-K$	0	0
Current input	1	y_{11}	0	0	0	K	0	0	0
	2	0	y_{22}	0	0	0	K	0	0
	3	$-Dy_{11}y_{33}$	$Dy_{22}y_{33}$	y_{33}	0	$-K^3$	K^3	K	0
	4	By_{11}	$-By_{22}$	0	0	K^2	$-K^2$	0	0
Current input	1	y_{11}	0	0	0	K	0	0	0
	2	0	y_{22}	0	0	0	K	0	0
	3	$-By_{11}$	By_{22}	0	0	$-K^2$	K^2	0	0
	4	$Dy_{11}y_{44}$	$-Dy_{22}y_{44}$	0	y_{44}	K^3	$-K^3$	0	K

Table 7 Admittance matrices for a complete hybrid amplifier

Type		General amplifier				Operational amplifier			
		1	2	3	4	1	2	3	4
Complete hybrid	1	0	0	0	0	0	0	0	0
	2	0	y_{22}	0	0	0	K	0	0
	3	$-C$	By_{22}	0	0	$-K$	K^2	0	0
	4	Ay_{44}	$-Dy_{22}y_{44}$	0	y_{44}	K^2	$-K^3$	0	K
Complete hybrid	1	y_{11}	0	0	0	K	0	0	0
	2	0	0	0	0	0	0	0	0
	3	$-By_{33}$	C	0	0	$-K^2$	K	0	0
	4	$Dy_{11}y_{44}$	$-Ay_{44}$	0	y_{44}	K^3	$-K^2$	0	K
Complete hybrid	1	0	0	0	0	0	0	0	0
	2	0	y_{22}	0	0	0	K	0	0
	3	$-Ay_{33}$	$Dy_{22}y_{33}$	y_{33}	0	$-K^2$	K^3	K	0
	4	C	$-By_{22}$	0	0	K	$-K^2$	0	0
Complete hybrid	1	y_{11}	0	0	0	K	0	0	0
	2	0	0	0	0	0	0	0	0
	3	$-Dy_{11}y_{33}$	Ay_{33}	y_{33}	0	$-K^3$	K^2	K	0
	4	By_{11}	$-C$	0	0	K^2	$-K$	0	0

amplifier is extremely large and approaching infinity then the values of the input and output admittances are immaterial.

4. Network Matrices

In this Section a number of familiar amplifier configurations are considered, together with their respective matrices.

4.1. *Basic Feedback Network*

The circuit shown in Fig. 3 has the definite admittance matrix shown in Table 8. For a conventional voltage operational amplifier

$$\frac{e_4}{e_s} = \frac{-y_{4s}}{y_{44}} = \frac{Y_1(Ay_{44}-Y_2)}{(y_{44}+Y_2)(y_{11}+Y_1+Y_2)+Y_2(Ay_{44}-Y_2)} \quad \ldots\ldots(1)$$

This expression reduces to the more familiar one:

$$\frac{e_4}{e_s} = -\frac{Y_1}{Y_2} \quad \ldots\ldots(2)$$

if y_{11}, $1/A \to 0$, where A denotes the amplifier gain.

4.2. *Non-inverting Amplifier I*

Figure 4 and Table 9 show the circuit and definite admittance matrix respectively.

In the derivation of the matrix it was assumed that

$$A_{14} = -A_{24} = -A \quad \text{and} \quad y_{12} = y_{21}$$

If we further assume that

$$y_{44} \to \infty \quad \text{and} \quad y_{11}, y_{12} \to 0$$

then

$$\frac{e_4}{e_s} = \frac{(Y_1+Y_2)A}{Y_1+Y_2(1+A)} = \left(1+\frac{Y_1}{Y_2}\right) \quad \ldots\ldots(3)$$

if $A \gg 1$.

4.3. *Non-inverting Amplifier II*

The network shown in Fig. 5 illustrates a further method of obtaining a non-inverted relationship between input and output voltages. From Table 10, if we let

$$y_{11}, y_{12} \to 0$$

and

$$Y_1 = Y_2 = Y_3 = Y_4 = Y$$

then

$$\frac{e_4}{e_s} = \frac{Y(Y+y_{44}A)}{[(2Y+Y_5)\left\{2Y+y_{44}+\dfrac{Y(y_{44}A-Y)}{2Y}\right\}-Y(y_{44}A+Y)]} \quad \ldots\ldots(4)$$

Now, if y_{44} and $A \to \infty$, then

$$\frac{e_4}{e_s} = \frac{2Y}{Y_5} \quad \ldots\ldots(5)$$

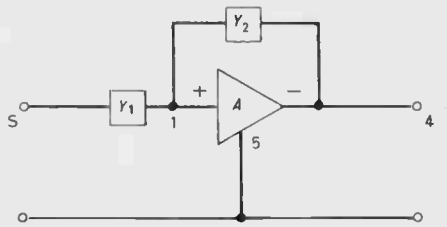


Fig. 3. Basic feedback network.

Table 8

Admittance matrix for a basic feedback network

$Y_1 - \dfrac{Y_1^2}{y_{11}+Y_1+Y_2}$	$\dfrac{-Y_1Y_2}{y_{11}+Y_1+Y_2}$
$\dfrac{Y_1(Ay_{44}-Y_2)}{y_{11}+Y_1+Y_2}$	$(y_{44}+Y_2) + \dfrac{Y_2(Ay_{44}-Y_2)}{y_{11}+Y_1+Y_2}$

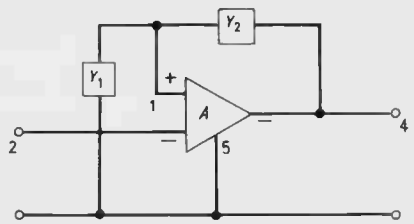


Fig. 4. Non-inverting amplifier (I).

Table 9 Admittance matrix for the non-inverting amplifier (I) (Fig. 4)

$(y_{22}+y_{12}) - \dfrac{y_{12}^2}{y_{11}+y_{12}+Y_1+Y_2}$	$-\dfrac{y_{12}Y_2}{y_{11}+y_{12}+Y_1+Y_2}$
$-y_{44}A + \dfrac{y_{12}(y_{44}A-Y_2)}{y_{11}+y_{12}+Y_1+Y_2}$	$(y_{44}+Y_2) + \dfrac{Y_2(y_{44}A-Y_2)}{y_{11}+y_{12}+Y_1+Y_2}$

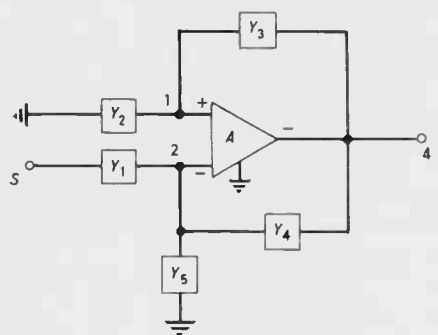


Fig. 5. Non-inverting amplifier (II).

Table 10 Admittance matrix for the non-inverting amplifier (II) (Fig. 5)

S	$Y_1 - \dfrac{Y_1^2}{\left\{\begin{matrix} y_{22}+y_{12}+Y_1+Y_4+Y_5 \\ -\dfrac{y_{12}^2}{y_{11}+y_{12}+Y_2+Y_3}\end{matrix}\right\}}$	$\dfrac{-Y_1\left\{Y_4+\dfrac{Y_3 y_{12}}{y_{11}+y_{12}+Y_2+Y_3}\right\}}{\left\{\begin{matrix} y_{22}+y_{12}+Y_1+Y_4+Y_5 \\ -\dfrac{y_{12}^2}{y_{11}+y_{12}+Y_2+Y_3}\end{matrix}\right\}}$
4	$\dfrac{Y_1\left\{\begin{matrix} -(Y_4+y_{44}A) \\ +\dfrac{Y_{12}(y_{44}A-Y_3)}{y_{11}+y_{12}+Y_2+Y_3}\end{matrix}\right\}}{\left\{\begin{matrix} y_{22}+y_{12}+Y_1+Y_4+Y_5 \\ -\dfrac{y_{12}^2}{y_{11}+y_{12}+Y_2+Y_3}\end{matrix}\right\}}$	$\dfrac{\left(y_{44}+Y_4+Y_3+\dfrac{Y_3(y_{44}A-Y_3)}{y_{11}+y_{12}+Y_2+Y_3}\right)}{-\left\{Y_4+\dfrac{Y_3 y_{12}}{y_{11}+y_{12}+Y_2+Y_3}\right\}\left\{\dfrac{\begin{matrix}-(y_{44}A+Y_4) \\ +y_{12}(y_{44}A-Y_3)\end{matrix}}{y_{11}+y_{12}+Y_2+Y_3}\right\}}{\left\{\begin{matrix} y_{22}+y_{12}+Y_1+Y_4+Y_5 \\ -\dfrac{y_{12}^2}{y_{11}+y_{12}+Y_2+Y_3}\end{matrix}\right\}}$

Table 11

Admittance matrix for the voltage follower (Fig. 6)

y_{12}	$-y_{12}$
$-(y_{44}A+y_{12})$	$y_{44}(1+A)+y_{12}$

This network can be used as a positive integrator.[3] If

$$Y_1 = 1/2R \quad \text{and} \quad Y_5 = \rho C$$

then

$$\frac{e_4}{e_s} = \frac{1}{\rho CR} \qquad \text{.....(6)}$$

4.4. *Voltage Follower*

The circuit and its matrix are shown in Fig. 6 and Table 11 respectively.

4.5. *Summing Network*

The familiar summing network is shown in Fig. 7 and its admittance matrix is shown in Table 12. In general, the matrix elements may be calculated from the following expressions:

(i) Diagonal elements (except y_{44}):

$$Y_{S_n,S_n} = Y_n - \frac{Y_n^2}{y_{11}+\sum_{i=1}^{n} Y_i} \qquad \text{.....(7)}$$

(ii) Off-diagonal elements (except those including node 4):

$$Y_{S_j,S_k} = \frac{-Y_j Y_k}{y_{11}+\sum_{i=1}^{n} Y_i} \quad j,k = 1 \rightarrow n \qquad \text{.....(8)}$$

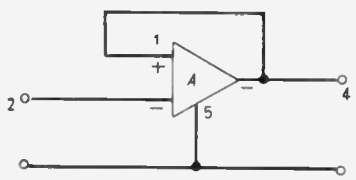


Fig. 6. Voltage follower.

(iii) Node 4 off-diagonal elements:

$$Y_{S_j,4} = \frac{-Y_j Y_f}{y_{11}+\sum_{i=1}^{n} Y_i} \quad = 1 \rightarrow n \qquad \text{.....(9)}$$

$$Y_{4,S_k} = \frac{Y_k(Ay_{44}-Y_f)}{y_{11}+\sum_{i=1}^{n} Y_i} \quad k = 1 \rightarrow n \qquad \text{.....(10)}$$

Y_{44} is listed in Table 12.

4.5. *Differential Output Network*

A configuration suitable for, say, a dual integrator is shown in Fig. 8 and its matrix is given in Table 13.

As $y_{11} \rightarrow 0$ and $y_{44} \rightarrow \infty$

$$\frac{e_4}{e_s} = \frac{-Y_1 A_{14}}{Y_1 + Y_2(1+A_{14})} \qquad \text{.....(11)}$$

If $A_{14} \gg 1$, then

$$\frac{e_4}{e_s} = \frac{-Y_1}{Y_2} \qquad \text{.....(12)}$$

Also, if $y_{33} \rightarrow \infty$

$$\frac{e_3}{e_s} = \frac{Y_1 A_{13}}{Y_2(1+A_{13})+Y_1} \qquad \text{.....(13)}$$

Table 12 Admittance matrix for the summing amplifier network (Fig. 7)

	S_1	S_2	S_n	4
S_1	$Y_1 - \dfrac{Y_1^2}{y_{11}+\sum Y_i}$	$\dfrac{-Y_1 Y_2}{y_{11}+\sum Y_i}$	$\dfrac{-Y_1 Y_n}{y_{11}+\sum Y_i}$	$\dfrac{-Y_1 Y_f}{y_{11}+\sum Y_i}$
S_2	$\dfrac{-Y_1 Y_2}{y_{11}+\sum Y_i}$	$Y_2 - \dfrac{Y_2^2}{y_{11}+\sum Y_i}$	$\dfrac{-Y_2 Y_n}{y_{11}+\sum Y_i}$	$\dfrac{-Y_2 Y_f}{y_{11}+\sum Y_i}$
S_n	$\dfrac{-Y_1 Y_n}{y_{11}+\sum Y_i}$	$\dfrac{-Y_2 Y_n}{y_{11}+\sum Y_i}$	$Y_n - \dfrac{Y_n^2}{y_{11}+\sum Y_i}$	$\dfrac{-Y_n Y_f}{y_{11}+\sum Y_i}$
4	$\dfrac{Y_1(Ay_{44}-Y_f)}{y_{11}+\sum Y_i}$	$\dfrac{Y_2(Ay_{44}-Y_f)}{y_{11}+\sum Y_i}$	$\dfrac{Y_n(Ay_{44}-Y_f)}{y_{11}+\sum Y_i}$	$\dfrac{(y_{44}+Y_f)+Y_f(Ay_{44}-Y_f)}{y_{11}+\sum Y_i}$

Table 13 Differential output network

	S	3	4
S	$Y_1 - \dfrac{Y_1^2}{Y_1+Y_2+y_{11}}$	0	$\dfrac{-Y_1 Y_2}{Y_1+Y_2+y_{11}}$
3	$\dfrac{-Y_1 y_{33} A_{13}}{Y_1+Y_2+y_{11}}$	y_{33}	$\dfrac{-Y_2 y_{33} A_{13}}{Y_1+Y_2+y_{11}}$
4	$\dfrac{Y_1(y_{44}A_{14}-Y_2)}{Y_1+Y_2+y_{11}}$	0	$Y_2+y_{44}+\dfrac{Y_2(y_{44}A_{14}-Y_2)}{Y_1+Y_2+y_{11}}$

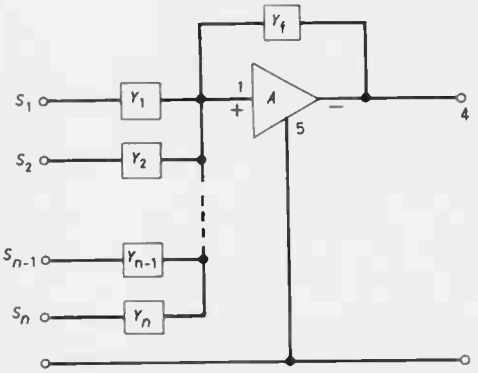


Fig. 7. Summing network.

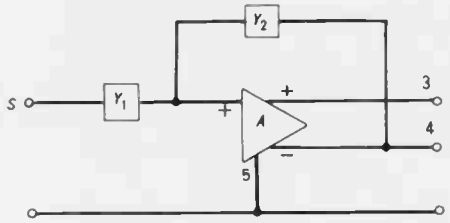


Fig. 8. Differential output network.

If $A_{13} \gg 1$, then

$$\frac{e_3}{e_s} = \frac{Y_1}{Y_2} \qquad \text{.....(14)}$$

If $Y_2 = \rho C$ and $Y_1 = 1/R$, then the network can be used as a dual integrator giving positive and negative integrals of the input signal.

5. Acknowledgments

The authors have pleasure in acknowledging financial support from the Ministry of Technology.

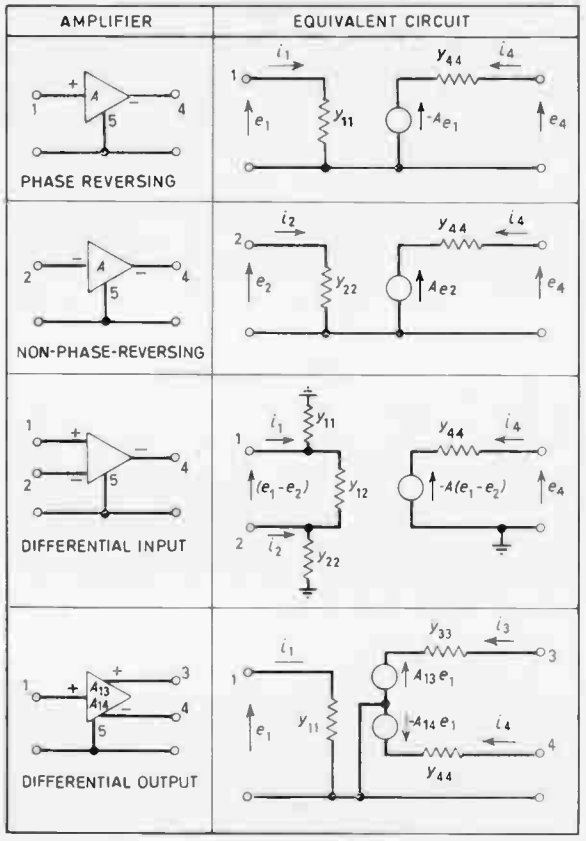
6. References

1. Sewell, J. I., 'The Application of Analogue Computing Techniques to the Design of Active Filters', Ph.D. Thesis, University of Newcastle-upon-Tyne, 1966.
2. Baxandall, P. J. and Shallow, E. W., 'Constant-current-source with unusually high internal resistance and good temperature stability', *Electronics Letters*, **2**, No. 9, pp. 351–2, September 1966.
3. Kerwin, W. J., Huelsman, L. P. and Newcomb, R. W., 'State-variable Synthesis for Insensitive Integrated Circuit Transfer Functions', Stanford University Technical Report No. 6560–10, p. 4.

7. Appendix

The equivalent circuits and admittance matrices for the various amplifiers used in Section 4 are listed in Tables 14 and 15.

Table 14
Amplifier equivalent circuits



Manuscript first received by the Institution on 19th September 1968 and in final form on 11th December 1968. (Paper No. 1253/CC43.)

Table 15
Amplifier matrices

Amplifier		Admittance matrix		
		1		4
Phase reversing	1	y_{11}		0
	4	Ay_{44}		y_{44}
		2		4
Non-phase reversing	2	y_{22}		0
	4	$-Ay_{44}$		y_{44}
		1	2	4
Differential input $\left\{\begin{matrix} y_{12}=y_{21} \\ A_{14}=A_{24}=A \end{matrix}\right\}$	1	$y_{11}+y_{12}$	$-y_{12}$	0
	2	$-y_{12}$	$y_{22}+y_{12}$	0
	4	$y_{44}A$	$-y_{44}A$	y_{44}
		1	3	4
Differential output	1	y_{11}	0	0
	3	$-y_{33}A_{13}$	y_{33}	0
	4	$y_{44}A_{14}$	0	y_{44}

Radio Engineering Overseas . . .

The following abstracts are taken from Commonwealth, European and Asian journals received by the Institution's Library. Abstracts of papers published in American journals are not included because they are available in many other publications. Members who wish to consult any of the papers quoted should apply to the Librarian giving full bibliographical details, i.e. title, author, journal and date, of the paper required. All papers are in the language of the country of origin of the journal unless otherwise stated. Translations cannot be supplied.

MEDIUM WAVE DIRECTIONAL BROADCASTING

The operating conditions for the wide-band, directional, medium wave broadcasting antenna such as the horizontal and vertical radiation patterns to be independent of frequency in the 525–1600 kHz band, high attenuation of radiation at angles of elevation from 40° to 50°, easy adjustment without the use of additional complexity, etc., are considered in a Soviet paper. It is shown that use of logarithmic-periodic aerials employing a central mast with three or four rows of other masts of progressively decreasing height can satisfy the conditions. The merits of a zig-zag log-periodic antenna for m.w. broadcasting are discussed and relevant experimental results are quoted.

'Wide-band directional antennas for m.w. broadcasting', G. A. Kliger. *Telecommunications and Radio Engineering* (English language edition of *Elektrosvyaz'* and *Radiotekhnika*), No. 12, pp. 93–99, December 1967.

THERMOGRAPHIC TECHNIQUES IN ELECTRONICS

In a paper from the School of Electrical Engineering of the University of New South Wales, it is shown that the use of a scanning photographic density comparator to analyse the photographed brightness pattern of u.v.-irradiated, temperature sensitive, phosphor films, deposited on electronic components, permits the accurate determination of temperature distribution. A spatial resolution of 10 microns with a temperature sensitivity better than 0·5 degC is readily achieved.

A stroboscopic method can be used for thermal transients but the minimum time constant of phenomena which can be studied is limited by the phosphor thermal quench time constant. With recognized available thermographic phosphors this limit is currently somewhat above 1 ms.

'Thermographic analysis of electronic components', H. S. Blanks. *Proceedings of the Institution of Radio and Electronics Engineers Australia*, **26**, No. 10, pp. 337–342, October 1968.

MODELLING A RADAR DISPLAY

In modern aircraft the information from several sensors has to be presented on a single time-shared display. Superimposed on the video signals tactical information has to be simultaneously presented. The horizontal situation display is normally used together with a head-up display, and certain restraints on the common tactical symbology are necessary. Together with the circuitry for symbol generation these displays form the display system.

Two typical modes of operation are forward-looking ground mapping and air-to-air search, and in these modes the display is used as a conventional radar display. In order to optimize a radar display it is advantageous if the total system and its different parts can be described analytically in a mathematical model. Several authors have treated the performance of a pulse radar system with the major emphasis on the radar and its parameters. The display has normally been characterized by two parameters, namely collapsing loss and integration over the beam width.

A paper from Svenska Radio AB presents a mathematical model of the radar display including such parameters as luminance curve, contrast transfer function, ambient conditions, acuity and threshold sensitivity of the human eye, etc. In the model the ultimate 'detector' is assumed to be the pilot and his ability to perceive a contrast on the display. The model may be used for different types of display tubes, e.g. the Tonotron.

'A mathematical model of a radar display', L. Alfredsson, *Ericcson Technics*, **24**, No. 3, pp. 133–159, 1968 (In English).

FAST LOGIC CIRCUITS

A circuit which is closely related to the Schmitt trigger can be used as a basis for logic circuits, with the advantage that good discrimination is obtained using only a very small 'swing', according to a paper from the Philips Research Laboratories, Eindhoven. The amount of heat dissipated is thus quite small (3 or 4 mW or so), so that numerous logic functions can be accommodated on a single chip in an integrated circuit, without sacrificing switching speed; switching times may still be as low as from 2 to 5 ns. This new circuit can be used in large-scale integration.

'Fast logic circuits with low energy consumption', A. Slob. *Philips Technical Review*, **29**, No. 12, pp. 363–367, 1968 (In English).

RADIATION PATTERN MEASUREMENTS

For measuring the radiation characteristics of television transmitter antennas, a method was adopted by the German Post Office which permits a bird's-eye-view of the characteristics to be obtained with reasonably inexpensive and quick means. The essential grounds for the efficiency of the procedure were measurement flights using a helicopter as the carrier for the instruments and the Decca navigator equipment. The conditions under which the vertical and horizontal diagrams may be calculated with an error of less than $\pm 0{\cdot}5$ dB in the frequency range of 470 to 790 MHz using the relative values of the free space field strengths are depicted. The determination of the gain of the antenna system with an error of less than 1·0 dB using the absolute measured values of the field strengths is also described.

'Measurement of the radiation of television transmitter antennas of the Deutsche Bundepost using a helicopter and Decca navigator', Ph. Henss and G. Mahlow. *Nachrichtentechnische Zeitschrift*, **22**, No. 1, pp. 40–48, 1969.