FOUNDED 1925
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"To promote the advancement of radio, electronics and kindred subjects by the exchange of information in these branches of engineering."

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Return to Cambridge

THE University of Cambridge has a special significance in the history of the science of radio and electronics since, as engineers will hardly need reminding, James Clerk Maxwell, whose electromagnetic theory laid the foundations of twentieth-century electronics, was the first professor of experimental physics and founder of the Cavendish Laboratory. Many of his successors in that Chair, as well as workers in the laboratory, have made great contributions to the development of radio and electronic science.

As the learned society most closely associated with this discipline, the I.E.R.E. therefore regards Cambridge with much affection. Since the war there have been four major Institution conventions or conferences held at the University, and in each case the technical part of the programme was held in the Cavendish Laboratory itself. The themes of these meetings were, respectively, television (on two occasions), electronics in automation, and cold-cathode tubes. Each of these was, to a certain extent, relatively specialized in interest.

The Institution's Council believes, however, that specialized conferences and symposia should, from time to time, be complemented by conventions which deal with matters of interest to a broad cross-section of members. It is appropriate that the first of this new kind of convention should be held in Cambridge in the first week of July 1968. Most of the convention sessions will be held, once again, in the lecture theatres of the Cavendish Laboratory and other sessions will take place in lecture rooms of King's College which will also provide residential accommodation for most of the delegates.

The 1968 Convention will be concerned with the more important new techniques which have emerged in the last few years and which are now becoming established as new branches of technology within the field of radio and electronic engineering. These subjects will be covered by several symposia of papers which will discuss the present 'state of the art' and also the way ahead over the next few years. Shorter symposia will provide authoritative discussions of even newer topics, developments which are barely out of the research laboratory or feasibility study stage. Education and management problems will also receive attention.

In order to keep the programme of the Convention as flexible as possible and to permit the inclusion of work which may, at the time of writing these words, be incomplete, the full programme will not be announced until the spring. Contributions are now invited on new developments in the whole field of radio and electronics. New technical themes to be developed in the course of the Convention will attempt to answer the broad question 'where is electronics going?': materials and devices, circuits and systems, all will fall into place in making this a meeting of maximum interest and value to the greatest possible number of members.

The Sixth Clerk Maxwell Memorial Lecture will be included in the programme. The Institution's tradition of including functions which are generally termed social events, for instance the Convention Dinner, will also provide excellent opportunities for informal discussion and renewal of international professional association on the occasion of this return to Cambridge.

G. D. C.

INSTITUTION NOTICES

Annual General Meeting of the Institution

Members are reminded that the Sixth Annual General Meeting of the Institution since incorporation by Royal Charter will be held in London on Tuesday, 5th December at 6 p.m. The Notice and Agenda of the meeting as well as the Annual Report of the Council are published in the current issue of the *Proceedings of the I.E.R.E.* Members overseas who do not receive the *Proceedings* can obtain a copy on application to the Secretary. Members of all classes may attend the Annual General Meeting, but only Corporate Members are eligible to vote.

The Annual General Meeting will be followed by the Presidential Address of Major-General Sir Leonard Atkinson, K.B.E. The Address will commence at approximately 7 p.m. and the presence of non-members will be welcomed for this part of the meeting. The text of Sir Leonard's Address will be published in the January 1968 issue of *The Radio and Electronic Engineer*.

Special General Meeting of the Institution

At a Special General Meeting of Corporate Members of the Institution, held at 9 Bedford Square, London, on 18th October 1967, two Resolutions were passed for the purpose of altering and amending the Royal Charter and Bye-Laws of the Institution. Subject to the alterations and amendments being allowed by Her Majesty's Privy Council the present classes of Members and Associate Members will be known as 'Fellows' and 'Members' respectively. Additionally the requirements for the class of Associates will be changed to enable senior technicians who have the appropriate experience and proven technical training to become associated with the Institution.

Members will be informed in due course of the date on which these changes become effective and may then purchase a copy of the booklet containing the revised Charter and Bye-Laws.

International Conference of Engineering Organizations

The project to set up a world-wide organization for professional engineers—proposed a year ago by E.U.S.E.C.—is now to take practical form. The inaugural meeting will take place in Paris in early March 1968 with the substantial support of UNESCO. The Conference will be composed of national and international organizations representing engineers of a professional level of technical competence.

So far 61 professional engineering societies representing 26 countries including Czechoslovakia, Hungary and the U.S.S.R., have expressed a wish to participate in the new organization. International organizations which are joining the Conference are:

F.E.A.N.I. Fédération Européenne d'Associations Nationales d'Ingenieurs.

C.E.C. Commonwealth Engineering Conference.

U.P.A.D.I. Union Panamericana de Associations de Ingenieurs.

British participation will be both on a national basis, and internationally through membership of F.E.A.N.I., C.E.C. and E.U.S.E.C.

Obituary

Sir John Cockcroft, O.M., K.C.B., C.B.E., F.R.S., who died suddenly on 18th September last, was Master of Churchill College, Cambridge, and during his lifetime had combined the rôles of scientist, engineer and administrator to a notable degree. However, he is probably best known for his nuclear research work in the thirties at the Cavendish Laboratory when, with E. T. S. Walton, he produced transmutation of light elements by high-speed protons, and for his periods of office as Director of the Atomic Energy Laboratory at Chalk River (1944–1946) and as Director of the Atomic Energy Research Establishment at Harwell (1946–1958). He was Member for Scientific Research on the U.K. Atomic Energy Authority from 1954 until his return to Cambridge in 1959.

Members of the Institution will recall that in 1954 Sir John delivered the Second Clerk Maxwell Memorial Lecture in which he very graphically related Maxwell's work to developments which have taken place in 'the age of radio'.

* * *

The many engineers who count music among their interests will have learned with sorrow of the death of Sir Malcolm Sargent on 3rd October last. His own interests were unusually broad and in 1944 he took part in a memorable discussion meeting arranged by the Institution in London on 'High Fidelity Reproduction of Music'. In this he put forward some of the principles which must govern collaboration between the engineer and the musician in the broadcasting and recording of music.

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The Significance of Nullators, Norators and Nullors in Active-network Theory

By

A. C. DAVIES,
B.Sc.(Eng.), M.Phil.†

Summary: Although proposed in 1961, the nullator and norator have not been widely used or understood. At first sight these elements appear rather remote from reality, and in this paper an attempt is made to relate them to some practical devices. It is suggested that a nullator-norator pair (nullor) may be regarded as a reasonable idealization of a number of physical devices, but that the nullator and norator, considered individually, cannot be so regarded, and are not physically meaningful.

'Controlled-source' behaviour can usefully be represented by nullors in conjunction with passive two-terminal elements, and by generalization of the nodal and loop methods of analysis to deal with networks containing nullors, this can result in significant simplification in the analysis of some active networks. Topological methods of solution may also be used.

It is concluded that there are no outstanding difficulties involved in incorporating the nullor into the framework of conventional network theory, and that nullors may be useful in the analysis of practical active networks.

1. Introduction

The nullator is a two-terminal element for which both terminal current and terminal voltage are zero, and the norator is a two-terminal element for which terminal current and terminal voltage are arbitrary and can independently take on any value (Fig. 1). These elements were proposed in 1961[1] as ideal circuit elements to be added to the set of passive elements to form a set sufficient for the realization of all linear active non-reciprocal networks, but they have not been widely used or understood. The nullator has often been described[1-3] as a two-terminal element which is simultaneously an open-circuit and a short-circuit. Such a paradoxical description may encourage the opinion that these elements are too abstract to be useful, but it is misleading because the nullator does not completely fit the specification of either the short-circuit or the open-circuit. This can be summarized as follows:

	short-circuit	open-circuit	nullator	norator
Voltage	zero	arbitrary	zero	arbitrary
Current	arbitrary	zero	zero	arbitrary

Most ideal circuit elements are introduced either for mathematical convenience or because they may be regarded as idealizations of commonly used physical devices. It is therefore relevant to consider the extent to which the latter is true of the nullator and norator.

If a network contains more nullators than norators, inconsistencies in the network equilibrium equations may occur[11] (see Appendix 1) and if it contains more norators than nullators, the additional norators are redundant and carry no current. Because of this the nullator and norator cannot be regarded as separate, independent elements.

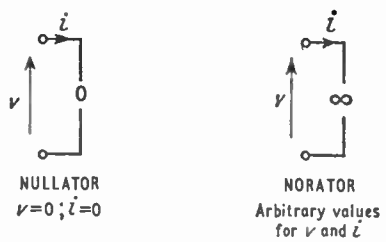

Fig. 1. Definition of nullator and norator.

However, it is possible to devise one-port networks composed of widely accepted ideal elements (usually positive and negative resistors and gyrators) which appear to possess the ($v = 0$, $i = 0$) property. Figure 12, Appendix 2, shows such a one-port.[1,5] Clearly, if networks of accepted ideal elements can possess this property, there is justification for considering the nullator and norator as independent elements.

However, although the nullator property (eqn. (25), Appendix 2) appears to follow from eqns. (23) and (24), this would not be so if v_1 and v_2 were both infinite and the network would merely behave as a resistor of resistance R. Infinite voltages are not unreasonable because of the zero-resistance loops within the network and such an interpretation is physically

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satisfactory since it is certain that if the network were constructed, instability would occur. A further objection is that if any of the component values depart from their nominal values (by any amount, however small) the one-port merely behaves as a resistor.[5] Figure 12 cannot therefore be regarded as a valid representation of the nullator. Recently, Tellegen has published[6] a detailed analysis of this network and has arrived at the same conclusion.

Thus such networks cannot be regarded as justification for considering the nullator as an independent element. (Zero resistance loops can occur and give rise to similar anomalies in equivalent circuits for various other ideal elements such as ideal transformers and negative impedance inverters, and they do not require special consideration.) Similar arguments apply in the case of one-port networks which allegedly possess the norator property. It may be concluded that the concept of the nullator and norator as separate independent elements is neither useful nor physically meaningful. On the other hand, if a nullator is introduced into a passive network (so producing an 'impossible' constraint) the inconsistency may be resolved by introducing a norator into the network. The norator provides the additional degree of freedom needed to permit the constraint imposed by the nullator.

Thus, in order to obtain meaningful results, it is necessary for networks to contain equal numbers of nullators and norators (for separable networks, equal numbers must occur in each separable part). The nullator-norator pair is termed the nullor. This name originated with Carlin[5] but similar concepts had been considered previously by Tellegen[7], Belevitch[2], Keen[8,9] and Myers.[10] The nullor is satisfactory in that its presence in a network does not lead to inconsistencies in the network equations.

It will now be shown that a number of idealized devices may be conveniently represented with the aid of the nullor.

2. Nullors in Network Models of Idealized Physical Devices

2.1. *Transistor Circuits*

In the approximate analysis of many transistor circuits, it is often permissible to assume that base currents are negligible in comparison with collector currents and that base-emitter voltages are zero (or equivalently, that $h_{ie} = 0$ and $h_{fe} = \infty$). Such idealized transistors may be precisely represented by nullors[3,10-12] as shown in Fig. 2. For more accurate analysis, the circuit model may easily be improved (for example, by the addition of y_{ie} and y_{fe}). Practical transistor amplifiers are usually satisfactory only if sufficient local feedback is provided to make the overall

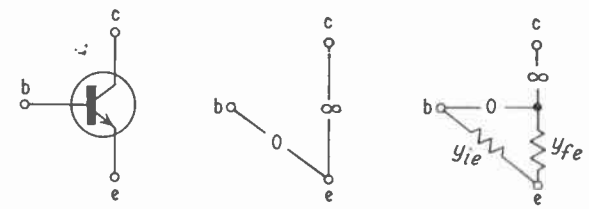


Fig. 2. Nullor model for transistor (Ideal: $V_{be} = 0$, $i_b = 0$).

performance independent of production spreads in transistor parameters,[13] and in such circumstances the simpler model is likely to be quite adequate.

2.2. *Virtual Earth*

The virtual earth is a well-established concept with much in common with the nullator. Figure 3 shows an operational-amplifier network, and it is well known that provided that the amplifier has a large, negative voltage gain, K, high input impedance and low output impedance,

$$\frac{V_0}{V_i} = -\frac{Z_2}{Z_1}$$

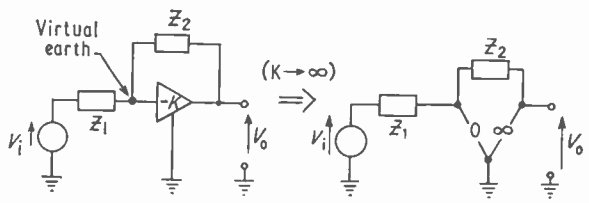


Fig. 3. Nullor model for operational amplifier.

The nullor representation shown also gives this result, and thus forms a convenient model for an ideal operational amplifier. Because the sign of the gain K does not appear in the nullor model (it disappears in the limit as $K \to \pm \infty$) the distinction between positive and negative feedback disappears and it is not meaningful to discuss stability in terms of such nullor models.

2.3. *Negative Impedance Convertor and Gyrator*

Figure 4 shows nullor models of a unity-ratio negative impedance convertor and of a gyrator. In both cases the models are valid only on a two-port basis and are of little practical value. However, more general representations are possible.

In most of these examples, the nullator and norator forming each nullor share a node, e.g. the nullor has been a three-terminal element. In this form it is

essentially the same as a unitor.[8,9] In the majority of cases nullors in which nullator and norator do not share a node are not required. However, the equations of networks containing separated nullators and norators do not show any inconsistencies provided

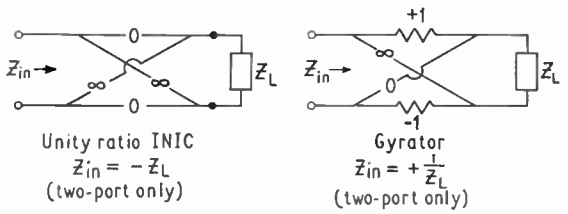


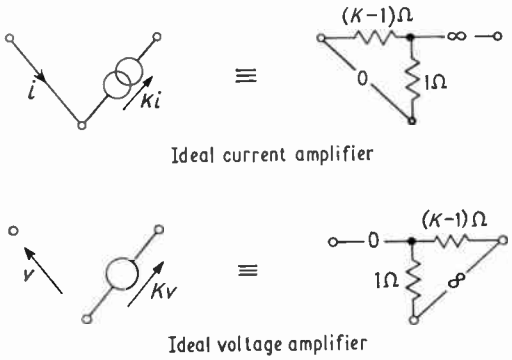
Fig. 4. Nullor models for negative impedance convertor and gyrator.

that equal numbers are present, and as shown in the next section, ideal current amplifiers and voltage amplifiers can be represented by networks in which such a separation does occur. Attention need not, therefore, be restricted to three-terminal nullors.

3. Nullors Instead of Controlled-sources

The most widely used ideal elements for representing non-reciprocal and active behaviour are the various controlled-sources. Nullors may be used instead, as shown by the equivalent networks in Figs. 5 and 6. A complete set of such equivalent networks has been published elsewhere by the author.[14] Nullor equivalents of four-terminal controlled-sources are also known. Duality is often useful for interrelating such networks; nullors remain unchanged in forming the dual.

Although these nullor equivalents of controlled-sources are rather cumbersome, they have some important advantages. There is a definite difference in kind between the controlled-source and the independent-source, yet the same symbol is used for



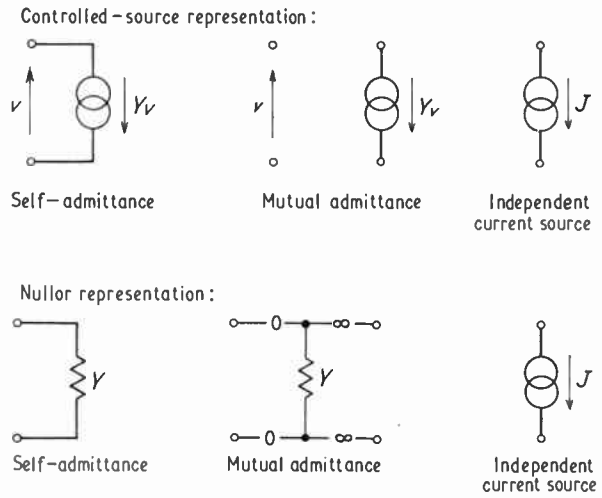
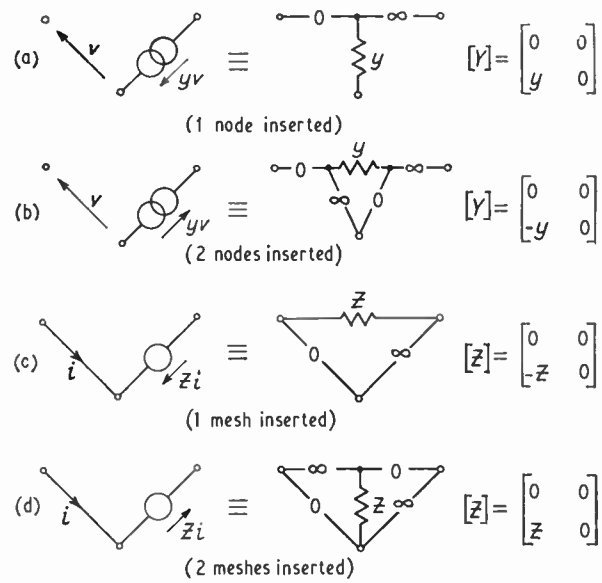


Fig. 7. Comparison between the controlled-source method and the nullor method of representing a mutual-admittance parameter.

both. For example, the voltage-controlled current-source has far more in common with the two-terminal admittance than with the independent current-source (in fact, it is a mutual admittance and not a source at all). This is shown more clearly by the use of the nullor (Fig. 7). This matter is discussed in more detail by Guillemin,[15] who points out that whereas independent-sources are constraints, controlled-sources are merely mutual parameters. Further, a similarity may be noted between the nullor equivalents and the manner in which controlled-source behaviour would



Figs. 5 and 6. Nullor networks equivalent to controlled-sources.

be achieved by adding passive feedback components to a suitable high-gain amplifier.

It will be shown (see Section 5) that these nullor equivalents for controlled-sources are also useful for simplifying analysis techniques.

4. Analysis of Networks containing Nullors

Having shown that nullors may be useful in representing various physical devices and ideal multi-terminal elements including all the controlled-sources, it remains to show that networks containing nullors can be analysed by simple modifications of conventional methods.

4.1. *Nodal Analysis*

In the nodal analysis of conventional two-terminal elements the following relationships are involved:[16]

$$\boldsymbol{i}_b = \boldsymbol{Y}\boldsymbol{v}_b \qquad \text{.....(1)}$$

$$\boldsymbol{j} = \boldsymbol{A}\boldsymbol{i}_b \qquad \text{.....(2)}$$

$$\boldsymbol{v}_b = \boldsymbol{A}'\boldsymbol{v}_n \qquad \text{.....(3)}$$

$\boldsymbol{A}$ denotes the node-branch incidence matrix, $\boldsymbol{Y}$ the diagonal branch-admittance matrix, $\boldsymbol{j}$ the source-current vector, $\boldsymbol{i}_b$ and $\boldsymbol{v}_b$ the branch-current and -voltage vectors respectively, and $\boldsymbol{v}_n$ the nodal voltage vector. A prime denotes the transpose.

Hence

$$\boldsymbol{j} = \boldsymbol{A}\boldsymbol{Y}\boldsymbol{A}'\boldsymbol{v}_n \qquad \text{.....(4)}$$

The author has shown previously[17,18] that for a network N containing nullors, eqn. (4) becomes

$$\boldsymbol{j} = \boldsymbol{A}_r\boldsymbol{Y}\boldsymbol{A}_c'\boldsymbol{v}_n \qquad \text{.....(5)}$$

where $A_r(A_c)$ is the incidence matrix of a network $N_r(N_c)$ obtained from N by short-circuiting all norators (nullators) and open-circuiting all nullators (norators).

4.2. *Loop Analysis*

A similar result may be derived for loop analysis. Here, the fundamental relationships are

$$\boldsymbol{v}_b = \boldsymbol{Z}\boldsymbol{i}_b \qquad \text{.....(6)}$$

$$\boldsymbol{e} = \boldsymbol{B}\boldsymbol{v}_b \qquad \text{.....(7)}$$

$$\boldsymbol{i}_b = \boldsymbol{B}'\boldsymbol{i}_l \qquad \text{.....(8)}$$

$\boldsymbol{B}$ denotes the loop-branch incidence matrix, $\boldsymbol{Z}$ is the diagonal branch-impedance matrix ($= \boldsymbol{Y}^{-1}$ for a network of two-terminal elements), $\boldsymbol{e}$ is the source-voltage vector, and $\boldsymbol{i}_l$ the loop-current vector.

Hence

$$\boldsymbol{e} = \boldsymbol{B}\boldsymbol{Z}\boldsymbol{B}'\boldsymbol{i}_l \qquad \text{.....(9)}$$

In eqn. (7), nullators may be regarded as short-circuits (they do not affect the summation of voltages round a loop) while norators may be regarded as open-circuits (the norator voltages are not needed to solve for the loop currents, and so the Kirchhoff voltage equations need not be written for any loops closed by norators). In eqn. (8), nullators may be regarded as open-circuits (no current flows through them) and norators as short-circuits (they provide paths for the loop currents).

Thus, for a network N containing nullors, eqn. (9) becomes

$$\boldsymbol{e} = \boldsymbol{B}_c\boldsymbol{Z}\boldsymbol{B}_r'\boldsymbol{i}_l \qquad \text{.....(10)}$$

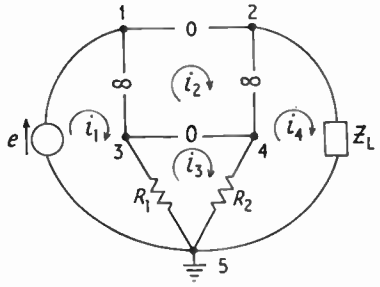
where $\boldsymbol{B}_r(\boldsymbol{B}_c)$ is the loop-branch incidence matrix of $N_r(N_c)$.

As an example, the negative impedance convertor shown in Fig. 8 is analysed by this method.

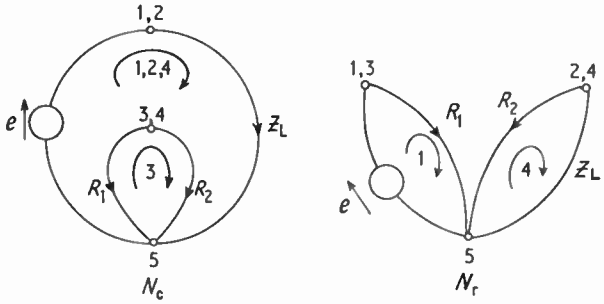
$$\boldsymbol{B}_c = \begin{matrix}1,2,4\\3\end{matrix}\begin{matrix}\begin{bmatrix}+1 & -1 & +1\\ -1 & +1 & 0\end{bmatrix}\end{matrix}\begin{matrix}R_1 & R_2 & Z_L\end{matrix}; \quad \boldsymbol{B}_r = \begin{matrix}1\\3\end{matrix}\begin{matrix}\begin{bmatrix}+1 & 0 & 0\\ 0 & -1 & +1\end{bmatrix}\end{matrix}\begin{matrix}R_1 & R_2 & Z_L\end{matrix}$$

Therefore

$$\begin{bmatrix}e_{1,2,4}\\ 0\end{bmatrix} = \begin{bmatrix}+1 & -1 & +1\\ -1 & +1 & 0\end{bmatrix}\begin{bmatrix}R_1 & 0 & 0\\ 0 & R_2 & 0\\ 0 & 0 & Z_L\end{bmatrix}\times \begin{bmatrix}+1 & 0\\ 0 & -1\\ 0 & +1\end{bmatrix}\begin{bmatrix}i_1\\ i_2\end{bmatrix}$$



(a) Negative impedance convertor.



(b) Graphs of N_c and N_r.

Fig. 8.

and

$$\begin{bmatrix} e_{1,2,4} \\ 0 \end{bmatrix} = \begin{bmatrix} R_1 & R_2+Z_L \\ -R_1 & -R_2 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \quad \text{.....(11)}$$

Also,

$$Z_{in} = \frac{e_{1,2,4}}{i_1} = \frac{\Delta}{M_{11}} = -\left(\frac{R_1}{R_2}\right)Z_L \quad \text{.....(12)}$$

$\Delta \equiv$ determinant and $M_{ij} \equiv$ co-factor: $(-1)^{i+j}$ times the determinant obtained by deleting ith row and jth column from Δ.

4.3. *Practical Methods*

In the practical analysis of networks it is generally neither necessary nor desirable to set up the equations in this manner. For mesh analysis of planar networks and for node-to-datum analysis, the loop impedance and nodal admittance matrices are normally written directly, by inspection. If nullors are present, similar practical methods exist.

The derivation of the procedure for nodal analysis has been given elsewhere by the author;[17] the nodal admittance matrix is first written for the network with all nullators and norators open-circuited. Then pairs of columns corresponding to node-pairs with nullators connected between them are added, and pairs of rows corresponding to node-pairs with norators connected between them are added. If a nullator or a norator is connected to the reference node, the appropriate column or row may be deleted altogether (this situation cannot, of course, arise if the indefinite admittance matrix is being used).

Figure 9(a) shows a transistor amplifier with combined current and voltage feedback. Using nullors as approximate models for the transistors, Fig. 9(b) is obtained.

With nullors removed,

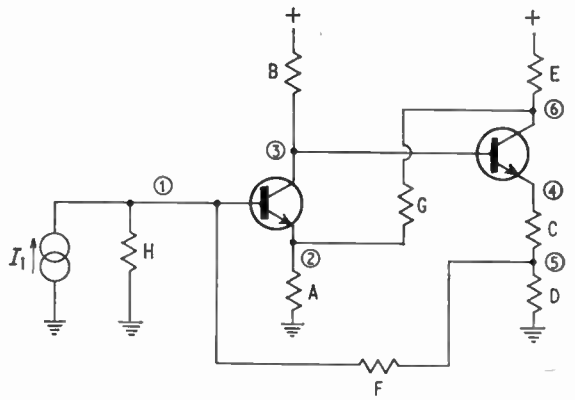
$$\begin{bmatrix} I_1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} F+H & 0 & 0 & 0 & -F & 0 \\ 0 & A+G & 0 & 0 & 0 & -G \\ 0 & 0 & B & 0 & 0 & 0 \\ 0 & 0 & 0 & C & -C & 0 \\ -F & 0 & 0 & -C & C+D+F & 0 \\ 0 & -G & 0 & 0 & 0 & E+G \end{bmatrix} \cdot \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \\ v_5 \\ v_6 \end{bmatrix} \quad \text{.....(13)}$$

Adding colums 2 to 1, and 4 to 3 and rows 3 to 2, and 6 to 4, gives

$$\begin{bmatrix} I_1 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} F+H & 0 & -F & 0 \\ A+G & B & 0 & -G \\ -G & C & -C & E+G \\ -F & -C & C+D+F & 0 \end{bmatrix} \cdot \begin{bmatrix} v_{1,2} \\ v_{3,4} \\ v_5 \\ v_6 \end{bmatrix} \quad \text{.....(14)}$$

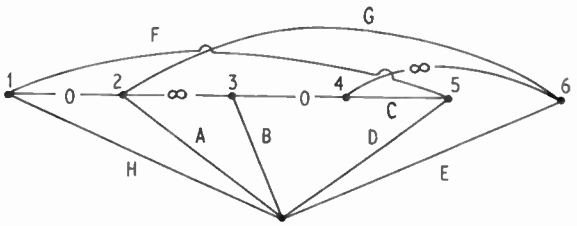
which may be solved for the nodal voltages.

A dual procedure can be used for mesh analysis. The mesh-impedance matrix is first written for the network with all nullators and norators short-circuited. Then pairs of columns corresponding to mesh-pairs which share a nullator are added (since the two meshes must have equal mesh-currents) and pairs of rows corresponding to mesh-pairs which share a norator are added. Any rows and columns corresponding to unshared nullators and norators are deleted altogether. Re-analysing Fig. 8 by this procedure, with nullators and norators short-circuited:



A,B,C,D,E,F,G,H. denote Admittances

(a) Transistor amplifier network.



(b) Graph of network incorporating nullors.

Fig. 9.

$$\begin{bmatrix} e \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} R_1 & 0 & -R_1 & 0 \\ 0 & 0 & 0 & 0 \\ -R_1 & 0 & R_1+R_2 & -R_2 \\ 0 & 0 & -R_2 & R_2+Z_L \end{bmatrix} \cdot \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} \quad \text{.....(15)}$$

Adding columns 3 to 2 and then deleting this column (since the upper norator is in an outer loop and appears in only one mesh) and adding rows 2 to 1 and 4 to 2, gives

$$\begin{bmatrix} e \\ 0 \end{bmatrix} = \begin{bmatrix} R_1 & R_2+Z_L \\ -R_1 & -R_2 \end{bmatrix} \begin{bmatrix} i_1 \\ i_4 \end{bmatrix} \quad \text{.....(16)}$$

which is the same result as before (eqn. (11)).

It must be emphasized that this simplified procedure can only be used for planar networks. The loops must

be chosen as the meshes or 'windows' of the network, and they must all have the same orientation (i.e. all clockwise or all anti-clockwise). Equation (10), on the other hand, applies for the general case.

4.4. *Topological Methods*

Topological methods are of interest for the alternative insight they provide, and they are useful in two aspects of the solution of networks by digital computer. Firstly, they provide a method of avoiding redundant terms in the expansion of determinants and they may therefore give more accurate numerical results. Secondly, and more important, they enable an algebraic rather than a numerical solution to be obtained. The author has shown elsewhere that topological methods can be used for analysis of networks containing nullors.[18] The use of nullors provides an alternative approach to other topological methods[19] of solving networks containing operational amplifiers.

5. Simplification of Active-network Analysis

The previous sections have shown that the analysis of networks containing nullors is straightforward, and requires only slight modification to conventional methods. In this section, examples are given to show that in certain circumstances the use of nullors can result in a significant simplification of active-network analysis.

The best-known systematic methods of analysis are the nodal and loop methods. However, the former cannot easily be used for the analysis of networks containing controlled-sources other than the voltage-controlled current-source type, while the latter cannot easily be used for the analysis of networks containing controlled-sources other than the current-controlled voltage-source type. With the aid of the nullor equivalents for controlled-sources[14] (Figs. 5 and 6), this restriction is completely removed.

Figure 10(a) shows a network containing a current-controlled voltage-source, which is not easy to solve by conventional nodal analysis. However, if the controlled-source is replaced by a suitable nullor equivalent as in Fig. 10(b), this difficulty is overcome.

Thus, with nullator and norator open-circuited,

$$\begin{bmatrix} I_1 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 1+Y & -1-Y & 0 \\ -1-Y & 2+Y & 0 \\ 0 & 0 & 1 \end{bmatrix} . \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} \qquad \text{.....(17)}$$

where $Y = \dfrac{1}{Z}$.

Adding column 1 to 3 and row 2 to 3,

$$\begin{bmatrix} I_1 \\ 0 \end{bmatrix} = \begin{bmatrix} 1+Y & -1-Y \\ -Y & 2+Y \end{bmatrix} \begin{bmatrix} V_{1,3} \\ V_2 \end{bmatrix} \qquad \text{.....(18)}$$

Thus, the input impedance $\dfrac{V_1}{I_1}$ is given by

$$\frac{V_1}{I_1} = Z_{in} = \frac{M_{11}}{\Delta} = \frac{2+Y}{2+2Y} = \frac{-2Z+1}{2Z+2}$$

and the voltage transfer-function $\dfrac{V_2}{V_1}$ by

$$\frac{V_2}{V_1} = \frac{M_{12}}{M_{11}} = \frac{Y}{2+Y} = \frac{1}{2Z+1}$$

Figure 10(a) could be solved directly by loop analysis although three simultaneous equations would be required, the above method requiring solution of only two.

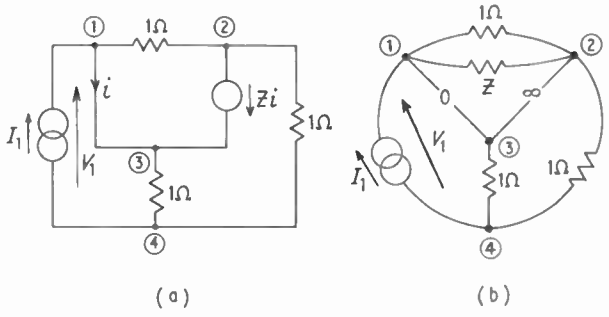


Fig. 10.
(a) Network containing current-controlled voltage-source.
(b) Nullor equivalent of (a).

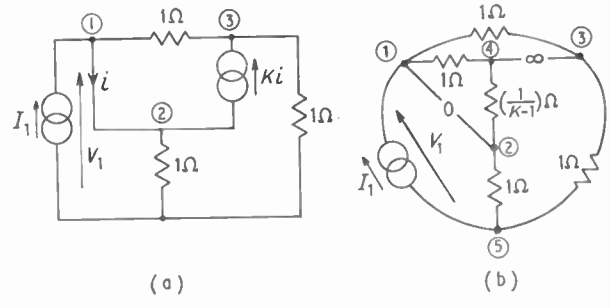


Fig. 11.
(a) Network containing current-controlled current-source.
(b) Nullor equivalent of (a).

As a second example, Fig. 11(a) shows a network containing a current-controlled current-source, not easy to solve by either nodal or loop analysis. However, the use of the nullor overcomes this difficulty (Fig. 11(b)).

With the nullator and norator open-circuited,

$$\begin{bmatrix} I_1 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 2 & 0 & -1 & -1 \\ 0 & K & 0 & -K+1 \\ -1 & 0 & 2 & 0 \\ -1 & -K+1 & 0 & K \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} \quad \text{.....(19)}$$

Adding column 1 to 2 and row 3 to 4,

$$\begin{bmatrix} I_1 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 2 & -1 & -1 \\ K & 0 & -K+1 \\ -1-K & 2 & K \end{bmatrix} \begin{bmatrix} V_{1,2} \\ V_3 \\ V_4 \end{bmatrix} \quad \text{.....(20)}$$

Thus,

$$\frac{V_1}{I_1} = Z_{in} = \frac{M_{11}}{\Delta} = \frac{2(K-1)}{2K-3}$$

As a final example, consider again Fig. 9(a), assuming that the components have the following numerical values:

$A = 1$ $\quad B = 0{\cdot}1$ $\quad C = 2$

$D = 2$ $\quad E = 0{\cdot}5$ $\quad F = 1$

$G = 0{\cdot}05$ $\quad H = 0{\cdot}1$ $\quad$ (All in millimhos)

If the transistors are assumed sufficiently ideal to be replaced by nullors, then eqn. (14) applies, and becomes

$$\begin{bmatrix} I_1 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 1{\cdot}1 & 0 & -1 & 0 \\ 1{\cdot}05 & 0{\cdot}1 & 0 & -0{\cdot}05 \\ -0{\cdot}05 & 2 & -2 & 0{\cdot}55 \\ -1 & -2 & 5 & 0 \end{bmatrix} \begin{bmatrix} V_{1,2} \\ V_{3,4} \\ V_5 \\ V_6 \end{bmatrix} \quad \text{.....(21)}$$

Solving these gives, for example,

$$\frac{V_6}{V_1} = 11{\cdot}35 \quad \text{and} \quad \frac{V_1}{I_1} = 354\ \Omega$$

Four simultaneous equations have to be solved. On the other hand conventional nodal analysis of Fig. 9(a) requires six simultaneous equations. If $y_{ie} = 1$ millimho, $y_{fe} = 100$ millimho, and y_{oe} and y_{re} are negligible, then these are,

$$\begin{bmatrix} I_1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 2{\cdot}1 & -1 & 0 & 0 & -1 & 0 \\ -101 & 102{\cdot}05 & 0 & 0 & 0 & -0{\cdot}05 \\ 100 & -100 & +1{\cdot}1 & -1 & 0 & 0 \\ 0 & 0 & -101 & 103 & -2 & 0 \\ -1 & 0 & 0 & -2 & 5 & 0 \\ 0 & -0{\cdot}05 & 100 & -100 & 0 & 0{\cdot}55 \end{bmatrix} \times \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \end{bmatrix} \quad \text{.....(22)}$$

for which

$$\frac{V_6}{V_1} = 10{\cdot}53 \quad \text{and} \quad \frac{V_1}{I_1} = 370\ \Omega$$

These results do not differ significantly from those obtained by the simpler approach, yet substantially more work is required to obtain them.

In comparing the above solutions with alternative methods not making use of the nullor, it is important to make a comparison with systematic methods. For circuits as simple as those chosen in the first two examples it is easy to write by inspection a few equations which enable a solution to be obtained as quickly or even more quickly than by the use of nullors. However, such methods are applicable in simple cases only, whereas the systematic methods can always be used. The nodal method is particularly suitable for network analysis by digital computer. It can be seen from Section 4.3 that each nullor in a network reduces by one the rank of the initial $\boldsymbol{Y}$ or $\boldsymbol{Z}$ matrix. The methods are therefore particularly attractive when large numbers of active elements are present. Such a situation arises in monolithic integrated circuits, where it is desirable on economic grounds to have a very high ratio of active to passive components.

6. Synthesis using Nullors

The methods described in Section 4.3 can be reversed and used to a limited extent for synthesis. A given $(n \times n)$ non-symmetric nodal admittance matrix may be enlarged to form an $(n+k) \times (n+k)$ symmetric matrix for which a reciprocal network realization is easily obtained, and insertion of k nullors into the network realizes the original non-symmetric matrix. The procedure involves the insertion of k additional nodes into the network. Similarly, non-symmetric mesh-impedance matrices may be realized by a mesh-insertion process.

An active-R–C transfer synthesis procedure using the nullor as the active element has been given by Martinelli,[11] who has also obtained some general theorems about R–C networks containing nullors.[20] Various aspects of the synthesis of non-reciprocal networks have been described by Keen[21-22] using the unitor (equivalent to a three-terminal nullor) who has shown that classical passive network synthesis procedures can be unified and generalized by the introduction of unitors.

7. Conclusions

It has been shown that although the nullator and norator, considered independently, cannot be regarded as physically meaningful, a nullator-norator pair (nullor) is a useful concept. Many idealized physical devices and all controlled-sources can be represented by networks incorporating nullors and conventional passive elements. The nullor is particularly useful in approximate models for high-gain amplifiers and it is likely that developments in integrated circuits will

make such amplifiers the commonest 'building-block' in the linear active networks of the future. Analysis techniques for networks containing nullors are similar to conventional ones, and significant simplifications in active network analysis may be achieved by replacing conventional active elements by nullors before commencing the analysis.

8. References

1. H. J. Carlin and D. C. Youla, 'Network synthesis with negative resistors', *Proc. Inst. Radio Engrs*, **49**, p. 907, 1961.
2. V. Belevitch, 'On the algebraic structure of formal realizability theory', *Revue HF*, **4**, No. **8**, p. 183, 1959.
3. W. Saraga, 'Analysis of active networks', presented at the Instn Elect. Engrs Colloquium on Network Analysis, London, 1965.
4. G. Martinelli, 'On the nullor', *Proc. Inst. Elect. Electronics Engrs*, **53**, p. 332, 1965. (Letters).
5. H. J. Carlin, 'Singular network elements', *Trans. I.E.E.E. on Circuit Theory*, **CT-11**, p. 67, 1964.
6. B. D. H. Tellegen, 'On nullators and norators', *Trans. I.E.E.E.*, **CT-13**, p. 466, 1966. (Letters).
7. B. D. H. Tellegen, 'La recherche pour une série complete d'élements de circuits idéaux nonlinéaires', *R. C. Seminario Matematico e Fisico, Milano*, **25**, p. 134, 1953–54.
8. A. W. Keen, 'A topological non-reciprocal network element,' *Proc. I.R.E.*, **47**, p. 1148, 1959.
9. A. W. Keen, 'Ideal three-terminal active elements', Polytech. Inst. of Brooklyn, MRI Symposia Series, Vol. X, p. 201, 1961.
10. B. R. Myers, 'Nullor model of the transistor', *Proc. I.E.E.E.*, **53**, p. 758, July 1965. (Letters).
11. G. Martinelli, 'Sintesi di una generica funzione de transferamento mediante il nullator ed il norator', *Alta Frequenza*, **32**, p. 274, 1963.
12. J. Braun, 'Equivalent NIC networks with nullators and norators', *Trans. I.E.E.E.*, **CT-12**, p. 441, 1965.
13. E. M. Cherry, 'An engineering approach to the design of transistor feedback amplifiers', *The Radio and Electronic Engineer*, **25**, No. 2, p. 127, February 1963.
14. A. C. Davies, 'Nullator-norator equivalent networks for controlled sources', *Proc. I.E.E.E.*, **55**, p. 722, May 1967. (Letters).
15. E. A. Guillemin, 'Theory of Linear Physical Systems', Chapter 6, p. 153 (Wiley, New York, 1963).
16. A. Nathan, 'A proof of the generalized topological Kirchhoff's rules', *Proc. Instn Elect. Engrs*, **109C**, p. 45, 1962. (I.E.E. Monograph No. 460E).
17. A. C. Davies, 'Matrix analysis of networks containing nullators and norators', *Electronics Letters*, **2**, No. 2, p. 48, February 1966.
18. A. C. Davies, 'Topological solution of networks containing nullators and norators', *Electronics Letters*, **2**, No. 3, p. 90, March 1966.
19. V. P. Sinha, 'Topological formulas for passive transformerless 3-terminal networks constrained by one operational amplifier', *Trans. I.R.E.*, **CT-10**, p. 125, 1963. (Letters).
20. G. Martinelli, 'RC transformerless networks embedding nullors', *Alta Frequenza*, **35**, p. 156, 1966.
21. A. W. Keen, 'Network synthesis in the non-reciprocal domain', in 'Recent Advances in Network Theory' (Pergamon Press, London, 1963).
22. A. W. Keen, 'Immittance synthesis in the non-reciprocal domain', *Proc. I.E.E.*, **110**, No. 12, p. 2118, 1963.

9. Appendix 1

The Effect of Independent Nullators and Norators

Consider a network of conventional passive elements and suppose that a nullator is connected between a pair of nodes. The presence of the nullator cannot affect the $\sum i = 0$ equations for the network, but some of the $\sum v = 0$ equations must be affected (except in the trivial case where the nullator is connected between nodes already at the same potential). However, the $\sum i = 0$ and $\sum v = 0$ equations are not all independent. [Suppose the network has N nodes, B branches and L closed loops. Then $(L+N)$ Kirchhoff equations can be written, but there are only B independent variables and $(L+N) \gg B$]. Consequently, the presence of the nullator introduces an inconsistency into the network equilibrium equations which may then have no unique solution and the network could not correspond to any meaningful system.

If a norator is connected into an otherwise passive network, it has no effect and carries no current since the network variables are determined by the passive network. The presence of the norator does not change the network equilibrium equations and is therefore irrelevant.

10. Appendix 2

Analysis of Network shown in Fig. 12

For the gyrator:

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} 0 & R \\ -R & 0 \end{bmatrix} \begin{bmatrix} i_3 \\ i_1 \end{bmatrix}$$

For the resistors:

$$v_1 = Ri_4; \quad v_2 = -Ri_2$$

$$I = i_1 + i_2 = \frac{v_1}{R} - \frac{v_2}{R}$$

and

$$I = -i_3 - i_4 = \frac{v_2}{R} - \frac{v_1}{R}$$

It follows that

$$\frac{2v_1}{R} = \frac{2v_2}{R}$$

Therefore

$$v_1 = v_2 \qquad \text{.....(23)}$$

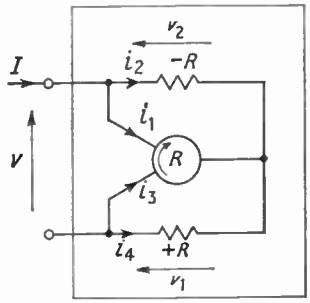


Fig. 12. An anomalous one-port.

But,

$$\left.\begin{aligned} V &= v_2 - v_1 \\ I &= \frac{1}{R}(v_2 - v_1) \\ \frac{V}{I} &= R \end{aligned}\right\} \qquad \text{.....(24)}$$

from eqn. (23), provided that v_1 and v_2 are not both infinite

$$V = 0, \quad I = 0 \qquad \text{.....(25)}$$

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STANDARD FREQUENCY TRANSMISSIONS

(Communication from the National Physical Laboratory)

Deviations, in parts in 10^{10}, from nominal frequency for October 1967

October 1967	24-hour mean centred on 0300 U.T.			October 1967	24-hour mean centred on 0300 U.T.		
	GBR 16 kHz	MSF 60 kHz	Droitwich 200 kHz		GBR 16 kHz	MSF 60 kHz	Droitwich 200 kHz
1	− 299·8	+ 0·1	+ 0·2	17	− 300·0	− 0·4	− 0·3
2	− 299·9	+ 0·2	+ 0·2	18	− 299·8	0	− 0·1
3	− 299·8	+ 0·1	+ 0·1	19	—	− 0·6	− 0·2
4	− 299·9	+ 0·1	+ 0·1	20	− 300·1	− 0·3	− 0·2
5	− 299·7	+ 0·2	+ 0·1	21	− 300·3	− 0·1	− 0·2
6	− 299·9	− 0·1	+ 0·2	22	− 300·2	− 0·1	− 0·2
7	− 299·9	+ 0·2	+ 0·2	23	− 300·1	− 0·3	− 0·2
8	− 299·9	+ 0·1	+ 0·2	24	− 300·2	0	− 0·1
9	− 299·8	+ 0·2	+ 0·3	25	− 300·3	− 0·4	− 0·2
10	− 299·8	+ 0·2	+ 0·3	26	− 300·3	− 0·1	− 0·2
11	− 299·8	+ 0·1	+ 0·2	27	− 300·0	− 0·2	− 0·2
12	− 299·9	+ 0·5	− 0·2	28	− 300·2	− 0·1	− 0·2
13	− 299·9	+ 0·3	− 0·2	29	− 300·3	− 0·2	− 0·2
14	− 299·8	− 0·3	− 0·2	30	− 300·2	− 0·2	− 0·1
15	− 299·8	0	− 0·2	31	− 300·2	− 0·2	− 0·2
16	− 299·7	− 0·1	− 0·2				

Nominal frequency corresponds to a value of 9 192 631 770·0 Hz for the caesium F,m (4,0)–F,m (3,0) transition at zero field.

Conferences in 1968

Conference on Thick Film Technology

The Council of the I.E.R.E. has approved a proposal that the Institution should sponsor a two-day conference on Thick Film Technology at Imperial College on 8th to 9th April, 1968. The Institution of Electrical Engineers has accepted an invitation to be a co-sponsor and the Organizing Committee will shortly be drawing up the programme.

It is probable that the subject matter of the Conference will fall into four groups:

Substrates;

Materials, inks and deposition techniques;

Assembly techniques;

Packaging techniques.

Offers of papers on this important new technology are invited and should be sent, in the form of a synopsis, to the Conference Secretariat, Institution of Electronic and Radio Engineers, 9 Bedford Square, London, W.C.1.

U.K. Seminar on Communication-Satellite Earth Stations

An international Seminar on Communication-Satellite Earth Stations is being organized jointly by the Post Office, the Ministry of Technology and British industry. It will be held from 20th to 31st May, 1968.

The first week of the Seminar at the Royal Lancaster Hotel in London will be allocated to the presentation of papers; the second week to visits to the Post Office Earth Station at Goonhilly and to scientific and industrial establishments engaged on work in the field of satellite communications.

The Seminar is expected to be of special interest to overseas administrations concerned with the planning, specification, purchasing and operation of earth stations. It will provide a comprehensive survey of the techniques involved in the planning and operation of earth stations for civil communications, and will be supported by an exhibition.

The major part of the Seminar will be devoted to the type of station designed for the *Intelsat* Global Communication System; but papers will also be presented on small earth stations and other specialized aspects of satellite communications. Technical and financial questions will be discussed together with operating procedures, training and maintenance.

A number of overseas countries will be invited to participate. Observers from British industry and other interested organizations in the United Kingdom will also be invited to attend.

Enquiries should be addressed to the Chairman of the Organizing Committee, Mr. R. E. G. Back, U.K. Seminar on Communication-Satellite Earth Stations Planning and Operation, Post Office Engineering Department, WS2, 207 Old Street, London, E.C.1.

Digital Control of Large Industrial Systems

The International Federation of Automatic Control and the International Federation for Information Processing are joint sponsors of a Symposium on Digital Control of Large Industrial Systems, which is to be held at the University of Toronto from 17th to 19th June 1968. The organizers are the Associate Committee on Automatic Control of the National Research Council of Canada, the Canadian Computer Society and the University of Toronto.

The Symposium is intended to focus on the state of the art in applying digital computers to the control of industrial processes, systems and machines, and on progress being made in applying recent theoretical advances to industrial problems. The following are the areas of interest:

Performance of Installations: performance records and technical and economic evaluation of installations of some maturity; reliability records and techniques.

Design Techniques: design trends in closing control loops through a computer; developments in the structure of computer-control systems; applications of modern developments in control theory to computer-controlled systems.

Implementation of Control: computer specifications and performance requirements; instrumentation, control devices, and interface problems; programming techniques.

Authors who wish to present papers are asked to inform the Symposium Secretary as soon as possible and to enclose abstracts of their papers. The closing date for papers in final form, ready for printing, is 15th January 1968. All enquiries should be addressed to the Secretary, I.F.A.C./I.F.I.P. Symposium, Toronto 1968, Division of University Extension, University of Toronto, Toronto 5, Canada.

U.D.C. 621.523:629.13

Automatic Testing of Electronic Equipment for Aircraft

By

J. W. ANSTEAD†

Reprinted from the Proceedings of the Joint I.E.R.E.–I.Prod.E.–I.E.E. Conference on 'The Integration of Design and Production in the Electronics Industry' held at the University of Nottingham on 10th to 13th July 1967.

Summary: This paper discusses applications where automatic testing can be a requirement, some of the advantages and disadvantages to both manufacturer and customer, and the demands its use makes upon the aircraft electronic equipment designer.

Some of the problems which exist at present are due to the lack of consideration given to the use of automatic testing by the equipment designer. These can be overcome in the future if design, production and test methods are organized to take proper account of them. The constraints that these requirements place on the design processes are discussed.

1. Introduction

Evidence of the benefits to be obtained from the use of automatic testing has been published by airline operators,[1] who have a very considerable flow of a wide variety of electronic units into their repair organizations. Their need for automation has been rather more urgent than that of the manufacturers, whose rate of production of equipment is often much less than the rate at which present equipment is removed from the aircraft for testing. Nevertheless it is shown in the paper that automatic testing offers widespread advantages for the manufacturer too, although these are more difficult to assess in economic terms, and may take some time to take full effect. If a manufacturer is to make use of his automatic test machine, then there will have to be a clear understanding by the equipment designers of its requirements and limitations. The equipment design and construction, the test methods, performance specifications, and overhaul instructions will all have to be made compatible with automatic testing. Since increasing numbers of airlines, who are the customers, are buying automatic machines, there is already a strong requirement for this compatibility.

The large general-purpose automatic test machine, capable of testing complex electronic flight control equipment, is the type which is discussed in the paper.

2. Requirements for Automatic Testing

Some of the first complex automatic test machines were developed for rapid checkout of missiles. This was an application for which they were ideally suited. When similar machines were used for checking aircraft electronic systems *in situ* there were a number of difficulties, because the systems had not been designed for automatic testing, and because the machines could not take the place of the human aircrew who normally operate the systems.

Although such machines are used for testing some military aircraft systems *in situ*, civil airlines have rather different requirements in that the time available between flights may be as little as 30 minutes, and their aircraft operate from more than one base. The cost of operating machines at several airports, and the difficulty of applying them retrospectively to existing aircraft, makes their use unattractive in this particular application.

To solve the problem of checking electronic systems in the aircraft, there is likely to be a trend towards the inclusion of automatic self-testing facilities in future systems. The use of digital systems, under the control of general purpose airborne digital computers, will make this a practicable proposition, although there will be weight, cost and integrity penalties.[2] The computers would have access to all incoming signals and could monitor these continuously. If a fault occurred, the computers would recognize this, would inform the aircrew, and would provide an indication so that ground maintenance personnel would have no doubt which unit had failed. The eventual availability of automatic data transmission might enable details of faults to be sent to base, so that appropriate replacement units could be ready for the aircraft as soon as it lands.

The cost of delaying a flight of the coming 500-passenger 'jumbo-jets' or the supersonic transport aircraft is so formidable that it is considered that the provision of automatic self-testing facilities will be a design requirement for future aircraft systems.

The problems encountered by the airlines at the present time in maintenance work on electronic equipment are similar to those encountered by the manufacturers in 'inspection' testing, but the former have an

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additional major problem associated with inaccurate fault diagnosis in complex systems in the aircraft. Airlines all over the world report that approximately half of the units removed as faulty are in fact serviceable. The situation may be improved by the use of built-in testing facilities, but the need to get this equipment back into use in the shortest possible time, so as to minimize spares holdings, has encouraged airlines to go ahead and buy general-purpose automatic test machines.

Automatic test centres are being established at hangar floor level to receive equipment removed from aircraft and to filter the good from the bad units, so that serviceable units can be returned to stores with the minimum of delay, and without causing congestion in the repair workshops. The expense of setting up these centres was justified originally by the savings in the quantity of spares required to maintain the aircraft. There is a 'bonus', which appears to have been much more valuable than was anticipated, in that it is possible to make simple repairs to certain equipment at the automatic test centre and so further reduce the load on the repair workshops. For this to be practicable, the equipment has to be designed on a replaceable module basis, and there has to be a sufficient number of test points for the faulty module to be positively identified.

One airline reports[1] that of several hundred units of a particular piece of equipment which had a very high mechanical content, 56% of the units were returned to stores from the test centre, and the remainder had to be sent on to the repair workshops. Several hundred other units tested consisted of nine types of amplifier and analogue computer devices, and of these the centre was able to clear 93¾%. This dramatic reduction in the load on the workshops has allowed skilled labour to be used more profitably in repairing modules and mechanical items, instead of looking for faults which do not exist. Although the machine tended to reject modules which had marginal performance, this ultimately appeared to improve the equipment performance and to reduce the rate of removal of units from the aircraft.

Airlines are now proposing to install automatic test machines in the repair workshops to perform final tests on equipment after it has been repaired, as well as using machines as pre-workshop filters.

It is considered that manufacturers can best use general purpose automatic test machines for the 'inspection' tests on completed electronic units. The airlines have shown that the machines are well suited to this application, provided that the equipment has been designed for rapid testing. In general, equipment having a mechanical content takes longer to test than all-electronic equipment, because the response of the mechanism is often slow, and the test often involves scrutiny of a pointer or other moving part by a human tester. There might be no significant reduction in test time resulting from the use of automatic testing on such equipment, but there are other advantages, which might still be considered valuable. The manufacturers of the various automatic test machines have listed numerous advantages, and some of these will be discussed later in the paper.

3. Brief Description of a Typical Automatic Test Machine

A typical machine consists of a central control unit which is programmed by a punched tape, a number of signal injectors and measuring instruments, and a means of connecting the required facilities to the equipment under test. Frequently adaptor panels are required to match the equipment under test to the automatic test machine, and to provide specified source and load impedances, or special circuitry to simulate the normal electrical environment.

Typical facilities provided for testing aircraft electronic equipment are:

(1) Simultaneous injection of a number of a.c. and d.c. signals, including modulated signals.

(2) Measurement of alternating and direct voltages and currents, frequency, time interval, resistance, alternating and direct voltage ratio, frequency response, and phase angle.

(3) Provision of real or simulated synchro signals, and measurement of synchro outputs.

The provision of special test equipment, such as is required for testing manometric and gyroscopic aircraft units, is possible.

Some machines have added facilities so that they can automatically perform arithmetical calculations, such as are associated with averaging results, and can perform tests which involve the storage of test data.

The machine compares the measured result of each test with the upper and lower limits specified in the test program. If the result is within limits, the machine proceeds to the next test, printing and displaying the serial number of the test, the measured result and whether the test was passed or failed. Some machines also print out the upper and lower limits. If the test failed, the machine can be programmed to perform a check on itself, and then to perform diagnostic tests to localize the fault.

If the equipment under test is not all-electronic, it may be necessary for an operator to perform operations such as reading displays and setting controls. The machine can indicate when such actions are required, and the operator reads instructions from a card bearing the serial number of the test.

A machine of this type might take the form of a console containing three or four 19-inch racks, and could cost between £50 000 and £100 000, depending on the facilities required.

The future trend is probably towards using digital computers for controlling and organizing purposes. One computer could control a number of test stations. A special computer for instrumentation systems has already been introduced.[3]

4. The Advantages of Automatic Testing

The following are some of the advantages of automatic testing:

(1) The automatic test machine is general-purpose, so it can be programmed to test a range of equipment and the programme can be changed to cope with modifications to the unit under test. Considerable economic savings should be obtained, due to the reduction in the number of special-to-type test sets required, and the corresponding reduction in skilled labour. The largest savings would be expected in factories producing a wide range of complex all-electronic equipment, where a considerable quantity of special-to-type test equipment, not in full use, could be replaced by an automatic machine.

(2) Testing time (as distinct from the time for connecting and setting up the unit under test and the coupling adaptor) should be reduced. Again, the saving will be greatest on complex all-electronic units, and may be negligible on very simple units, or mechanical units, or those which have a slow response. Since the manual testing of complex units can take eight hours or even more, and since aircraft equipment is usually subjected to double testing, impressive savings result if the automatic test machine can reduce test times by a factor of five.

(3) Testing should be more consistent. On all-electronic equipment, the judgment of the operator is not involved in making the tests, and he cannot omit any tests. There is less risk of damage to the equipment due to mis-operation. If, as seems probable, airlines use automatic test machines to a greater extent than at present, then they will want overhaul test instructions written in a form from which program tapes can be punched with the minimum of translation. There is already a movement towards the adoption of an international standardized 'pseudo-English machine language' for use in writing such instructions.[4, 5] If the manufacturer is already using automatic test methods, he will have the information in a suitable form, and will have proved that the test methods are satisfactory, and there should be a minimum of disagreement between factory and customer on the performance of equipment. The cost of producing overhaul manuals should be reduced.

(4) The results of tests are printed on paper so that there is no need for the operator to write down results, as is sometimes required. A punched or magnetic tape record of results can also be provided in a form which is suitable for processing by a computer. This technique can be used for investigating failures, to feed back useful information to the designer, showing which areas of the equipment are prone to failure, and perhaps recording stress levels. Such records are valuable for quality control and trend analysis. Additional tests can be included without increasing testing time unduly.

(5) There is likely to be more use of digital techniques in future aircraft electronic equipment. Automatic testing is much more practicable than hand testing of digital equipment, although a different form of machine from that described might be appropriate.

5. Some Difficulties

The adoption of automatic testing methods do however lead to certain problems:

(1) The purchase of an automatic test machine involves a considerable capital outlay, and it will be necessary to demonstrate that this will be offset in a reasonable time by the economies resulting from its use.

(2) If these economies are to be made, then the equipment to be tested must be designed so that it is suitable for use with automatic testing methods. Features which would make equipment unsuitable for automatic testing are generally those which would make equipment difficult to test and maintain by any other means. In addition, very slow tests, or tests which involve many manual operations of controls, do not take advantage of the high-speed capability of automatic machines.

(3) Test and performance specifications may have to be re-written to suit new test methods and tolerances, if they were not written with the particular machine in mind. It will be necessary for the engineers responsible for the specifications to understand the behaviour and limitations of the automatic test machine. For example, it might be necessary to test the response of equipment to ramp or step inputs, rather than to sinusoidal variations, or to make special allowance in the programs for small delays, inherent in manual testing, which affect the test results.

(4) The provision of an interface or coupling panel between the machine and each type of unit under test is not merely a matter of selecting the correct connections. Special supplies and source and load impedances might be required to simulate the normal working conditions. Such a panel resembles a manual test set without selector switches, signal generators or measuring instruments, so it might be convenient to make the panel dual-purpose. If there are some units

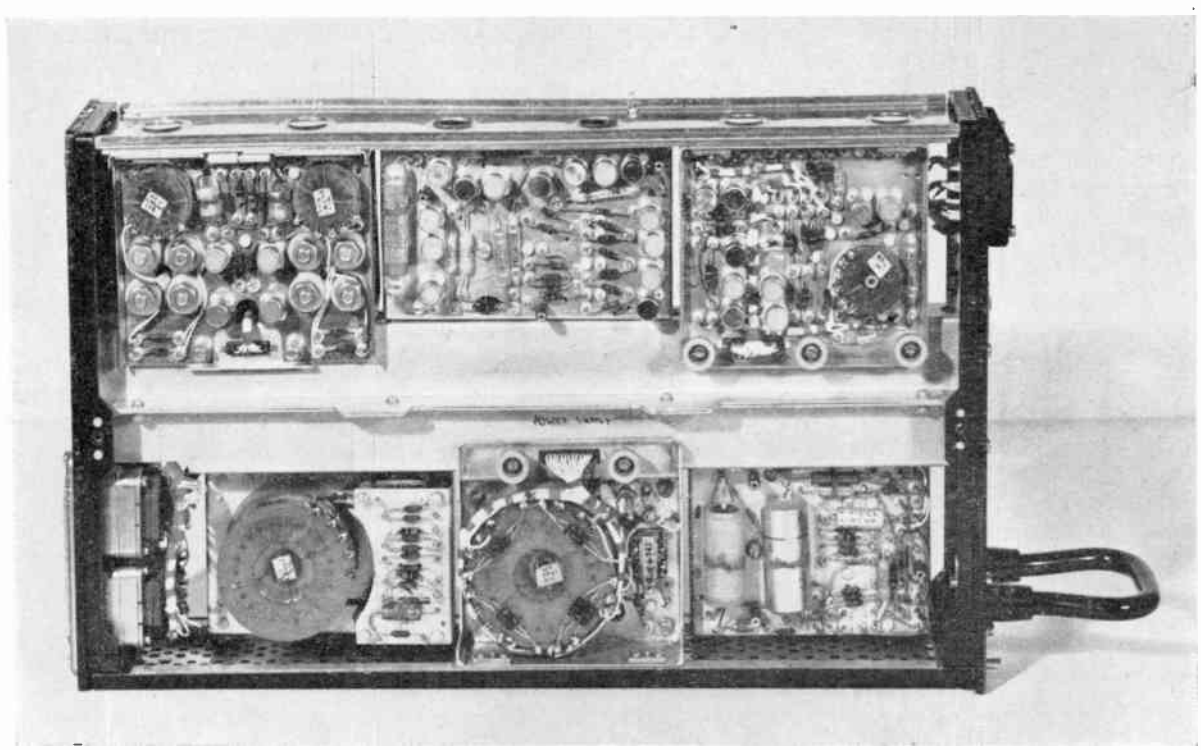

Fig. 1. A typical unit of aircraft electronic equipment.

where there are insufficient test points, or some modules which are not readily removable, then it is not possible for the automatic test machine to diagnose faults down to a level which dispenses with the need for manual test sets (unless the covers are removed from the units and they are tested using the machine in a manual mode—this is probably uneconomic). The adaptor panel could be fitted with selector switches so that it can be used with standard signal injectors and measuring instruments similar to those used in the machine. This type of manual test equipment can then be used for test and repair work on the aircraft units which cannot be fully tested on the machine.

(5) Since the automatic test machines are quite large, long lengths of cable are involved, and trouble with 'pick up' might be experienced. Special adaptors might be required, for example, for changing gearing, or feedback resistors when testing high-gain amplifiers.

(6) The reliability of the machine must be of a high order. A breakdown of the only automatic tester in a factory could stop or seriously impede equipment flow. Most machines not only test themselves, but also indicate which part has failed. Provided that spares are available, and that faulty parts can be identified and replaced easily, such breakdowns should be of short duration.

(7) Skilled engineering effort is required to write test programs and to prove that the automatic testing is satisfactory when the machine is first used on a unit. Corrections to the program and to the test system sometimes involve weeks of work.

6. Effects on the Design of the Equipment to be Tested

Since the justification for investing in automatic testing is the speeding-up of testing, and the reduction in the quantity of special-to-type test sets, good maintainability in the aircraft equipment becomes a more obvious requirement. It is important for the equipment designer to be extremely conscious of this need. Features which should be included are:

(1) The inclusion of sufficient test points to allow the automatic test machine to isolate any fault to a particular module within the unit. These test points must be accessible from outside the case of the unit.

(2) The equipment should be constructed from standard modules or sub-assemblies which have self-contained functions. Modules of any one type must be interchangeable without the need for any adjustment, and readily removable, preferably plugged in. (Figs. 1 and 2.)

(3) Modules and connectors should be standardized as far as possible, even if this means that performance is better than is necessary for a particular application. This is decided by the economics of design and production but standardization does reduce the number of test programs and test adaptors.

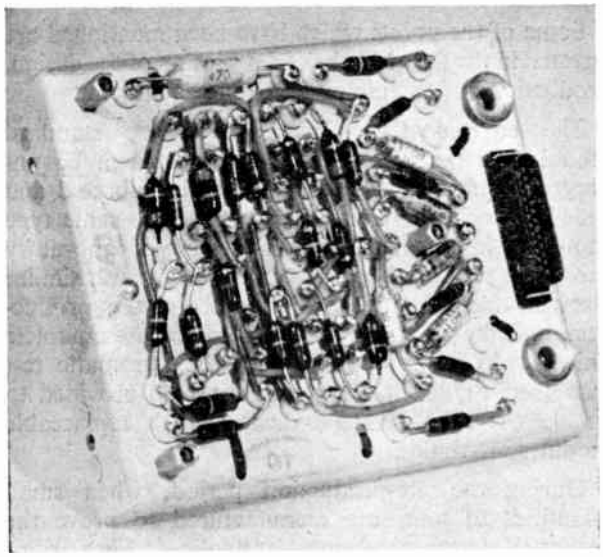

Fig. 2. A typical plug-in module.

7. Some Points to be Avoided

(1) Do not expect 'instant' or complete automation of the inspection department—the introduction of automatic testing might affect the work of many departments in an engineering company. Time is required to gain experience and to amend procedures.

(2) Do not write equipment specifications in terms of particular test gear. Specifications should be written in terms of absolute quantities, and should not conceal the performance by relating it to what are often ill-defined test sets. Precise specifications can be assessed to see if automatic testing is practicable. This is impossible if the designer has failed to meet his responsibilities and has defined the performance of the equipment in terms of switch positions and unscaled meter readings.

(3) Do not use vague phrases in specifications such as 'check that the output rises to approximately ten volts'. Remember that an automatic test machine has no intelligence and can carry out only precise instructions.

(4) Do not specify performance tests which involve the removal of covers to gain access to internal test points. This is bad practice as the unit may be damaged when the cover is replaced after the test. Sufficient test points should be brought out so that full performance tests can be carried out, and so that, as far as possible, faults can be isolated to a sub-assembly, with the covers in place.

(5) Do not use differing test methods in the various departments concerned with the design, development, production, inspection and repair of equipment. Try to use similar test methods and measuring instruments to avoid the rewriting of test instructions and the development of special-to-type test sets. This helps to reduce disagreements between departments and between the factory and customers. Automatic test machines can use measuring instruments and test methods similar to those of manual test rigs.

8. Effects on the Design of Manual Test Equipment

The general purpose automatic test machine is too expensive to be used for slow, intermittent testing of the type which occurs during assembly and repair. Simple manual or semi-automatic test equipment is required for calibration and testing during production or for use in the customer's repair workshops.

The design and use of special-to-type manual test sets should be minimized, as they are by their nature of limited application and are expensive. As far as possible they should be replaced by standardized switching and interconnection panels, which make use of external signal generators and measuring instruments. The efforts of test equipment designers should be directed towards the production of these instruments, which should be capable of being made programmable so that they can be used either manually or under the control of automatic test machines. Ideally, similar test instruments would be used with both the manual and the automatic test equipment, to reduce inconsistency between test methods.

For modules or sub-assemblies, and for units having less than about 40 connector pins, manual test circuit connections can conveniently be made by using a standard matrix board. Test cards for each module fit over the board and have holes punched in them, so that pins can be inserted through the holes to make appropriate connections between the pins of the module, and instruments and power supplies. A small load box, which is the only test equipment peculiar to the module, is usually required. Identical test equipment can be offered to the customer for module testing in his repair workshops, and the same test instructions can be used. If the module does not pass the standard performance tests, then it is very easy to make alternative connections on the matrix board to locate the fault. Figure 3 shows the matrix with a test card in place and Fig. 4 shows the card removed for fault finding. Measuring instruments and supplies are connected to the terminals.

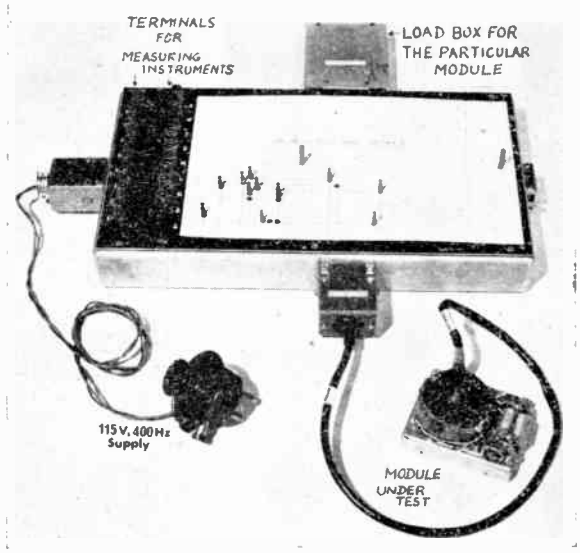

Fig. 3. Standard matrix board for module tests.

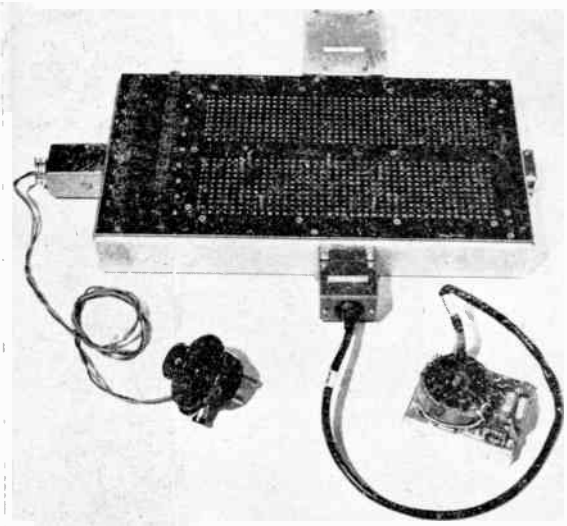

Fig. 4. Test card removed to permit fault finding.

9. Automatic Testing in the Factory

The use of automatic machines for testing mass produced components, such as resistors, is well established. This is a straightforward decision and the economic advantages are clear. Complications such as interface units, manual test sets and organizational problems do not occur.

The economies resulting from the automation of the testing of one range of items such as synchros, where there are many tests to be performed, are also easy to assess. It is more difficult to balance the expenditure of a large sum of money on a general-purpose machine against savings which are spread over many departments and over a period of time. To achieve best results, the use of modular construction and the standardization of test methods are necessary, but the organization of these will bring advantages even if automatic testing is not adopted.

Some of the points which have been mentioned are restated in the following brief description of the design, production and testing of electronic equipment.

The equipment designer should use standard modules so that all the active circuits can be unplugged from the case assembly, and calibrated and tested as separate items. Modules of the same type should be interchangeable. The testing of laboratory prototype modules should be carried out with similar test instruments to those which will be used in production, and the test methods specified for the complete unit should be compatible with the automatic test machine. Sufficient test points must be provided to enable the machine to indicate which replaceable modules are faulty.

During the pre-production period, when small quantities of units are manufactured to prove the design, the test methods must be finalized. The various test adaptors and test cards for the modules must be designed, built and tried out, and so must the manual test sets and/or coupling panels for testing complete units on the automatic test machine. The test program must be written in a form from which program tapes can be prepared. A completed unit, which is known to be correct, must then be tried on the automatic test machine to prove the whole set of equipment. This work might continue for some time, before a satisfactory test program can be established. It will be helpful to arrange the program so that it is not necessary to go through the whole test, and the unit and the test equipment can be set up to start at convenient points for investigating particular aspects of unit performance. Special tests can be included to provide data for fault analysis and quality control.

When production commences, the modules can be made, calibrated, and tested independently of the case assembly. This is devoid of active components, and its wiring can be tested quickly and accurately with comparatively inexpensive automatic test sets.

The tested modules are then fitted into the case and the complete unit is submitted for final inspection on the automatic test machine. The time saved by the use of the machine can be as much as 80 or 90% on some types of electronic unit, but can be very little on other units, where each test is lengthy due to the unit response. Such units might be better dealt with by manual testing to avoid 'bottle necks'.

10. Conclusions

The use of automatic testing has a generally beneficial effect on equipment design and production as it emphasizes the need for improved maintainability. The use of standardized, interchangeable modules reduces design, production, documentation, and maintenance costs for the equipment. The use of general-purpose automatic test machines reduces the quantity of special-to-type manual test equipment required and makes corresponding savings in skilled labour and time.

11. Acknowledgment

The author wishes to thank Mr. A. G. Studd for his encouragement and constructive comments.

12. References

1. Minutes of Eighth European Airlines Electronics Meeting, Helsinki, July 1966. Statement by Mr. Barnes, pp. 115–6.
2. E. S. Eccles, 'Flight management by digital computers', *World Aerospace Systems*, **2**, No. 1, p. 12, January 1966.
3. K. B. Magleby, 'A computer for instrumentation systems', *Hewlett Packard Journal*, **18**, No. 7, p. 2, March 1967.
4. 'Towards automatic checkout', *Aeroplane*, **113**, No. 2886, p. 35, 9th February 1967.
5. B. H. Scheff, 'An application of decision tables as the source language for automatic testing', *Trans. Inst. Elect. Electronics Engrs on Aerospace*, **AS-3**, No. 1, p. 47, February 1965.

Manuscript received by the Institution on 10th May 1967. (Paper No. 1153).

Space Research Projects

First Results from *Ariel III*

First results from experiments carried by *Ariel III*, the first all-British satellite launched successfully by the U.S. National Aeronautics and Space Administration (N.A.S.A.) for the Science Research Council on 5th May last, indicated that the satellite and its five experiments were continuing to operate satisfactorily. Considerable scientific information of much interest has been obtained and papers presented at the recent Symposium organized by the I.E.R.E. on 'The *Ariel III* Satellite' referred to preliminary results. (Several of the 13 contributions to this Symposium are being considered for publication in *The Radio and Electronic Engineer*.)

All mechanical systems operated satisfactorily during the launch phase and the spacecraft itself has maintained predicted temperatures. The power supply, telemetry and telecommand and data handling systems have all functioned well, and the tape recorder has replayed data of good quality whenever commanded.

The S.R.C. Radio and Space Research Station terrestrial noise experiment has already provided information about noise levels over the equatorial regions and also recorded intense storms over Western Europe during the first few days after launch. The voltage levels due to this terrestrial noise were on occasion greater than 100 times the galactic noise.

The intensity of cosmic radio waves on frequencies lower than those which normally penetrate the ionosphere is measured in the Manchester University experiment which investigates the variation of intensity from different parts of the sky. An unexpected interaction, through the ionospheric plasma, between signals on the Birmingham electron density probe and the Manchester loop aerial has been encountered, and the Manchester team are experimenting with duplicate satellite equipment so that points known to be affected in this way can be deleted from the data before analysis.

The Sheffield University apparatus for the study of the nature, intensity and world-wide occurrence of radio waves at frequencies below 20 kHz has recorded signals on every orbit with intensities up to 10^6 times the minimum detectable level. Zones of emissions at high latitudes are probably associated with auroral activity (energetic charged particles precipitating into the Earth's atmosphere): those at lower latitudes have uncertain origin. Intense whistler activity (which originates in lightning discharges) has been observed at medium latitudes. Strong signals from GBR Rugby have been received both when the satellite is near the transmitter and when it is over South Africa, which shows that energy from the transmitter can penetrate the ionosphere and travel approximately along a magnetic field line to the other hemisphere. However, on some orbits GBR has been picked up at locations remote from both the U.K. and South Africa.

Orbiting Solar Observatory Experiments

Instruments designed at University College, London and the University of Leicester, and financed by the Science Research Council, that will record information about the Sun and its influence on the Earth's atmosphere, are included in the payload of nine experiments carried by *OSO-D*, the Orbiting Solar Observatory satellite which was successfully launched by the U.S. National Aeronautics and Space Administration from Cape Kennedy on 18th October. Initial information received at ground stations in the United States shows that the two British experiments are functioning satisfactorily.

The broadband solar x-ray detector devised at the Mullard Space Science Laboratory, University College London, as a joint project with Leicester University, is designed to detect solar x-rays in the wavelength ranges of 1–20 Å and 44–60 Å. More information about the radiation in this region of the spectrum under both quiet and active solar conditions is needed for a better understanding of the solar corona. The measurements may lead to a method of providing an early warning of energetic particle fluxes from large solar flares, which are hazardous to high-flying aircraft and manned operations in space.

The second experiment, an ultra-violet monochromator devised at the Mullard Space Science Laboratory, is monitoring the total fluxes of helium II radiation at 304 Å and hydrogen Lyman-alpha radiation at 1216 Å. The information it sends back to Earth will show how changes in the helium radiation from the Sun affect the Earth's ionosphere.

The Orbiting Solar Observatory is a standardized spacecraft designed primarily as a stabilized platform for solar-orientated scientific instruments, placed in a circular orbit of 300 nautical miles (550 km) in altitude and about 33° inclination, orbiting about every 95 minutes. *OSO-D* carries, in addition to the British equipment, seven experiments for American research laboratories.

Indian Space Research Experiments

On 16th March 1967 the National Physical Laboratory of India conducted a rocket experiment with the collaboration of N.A.S.A. at Wallops Island, U.S.A. in which a riometer payload (relative ionospheric opacity meter), operating on a frequency of 13·265 MHz was sent to a peak altitude of 138 km. The equipment uses a cosmic noise receiver switched alternately between the dipole aerial and a standard noise source. The receiver output is arranged to be proportionate to the difference between the two sources.

Besides the riometer, the payload contained other instrumentation for a Faraday rotation experiment, a Lyman-alpha experiment and a probe. Preliminary data showed that the experiment was successful. It is proposed to conduct further flights from Thumba Equatorial Rocket Launching Base near Trivandrum.

Further details of these experiments appear in the *NPL Technical Bulletin* for July 1967.

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Design of Simple Frequency-division-multiplex Communication Systems without Band-pass Filters, with particular reference to the Use of Constant-resistance Modulators

By

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Summary: Consideration is given to the design problems of low-cost f.d.m. systems which achieve economy by the avoidance of band-pass filters for each channel at both ends of the system. It is shown that the best basis of design is the use of constant-resistance modulators.

1. Introduction

There is at the present time a considerable need for an economical multiplex transmission system for speech channels on junction circuits in the telephone network. The use of what were originally audio cables for wideband multi-channel systems involves a large number of problems, such as noise and inter-pair crosstalk, which become dominant when the frequencies involved are megahertz in place of the kilohertz for which the cable was designed. Because of these problems, the use of pulse-code modulation (p.c.m.) has been proposed and developed for such applications.[2] But this system sacrifices bandwidth for its relative insensitivity to noise and crosstalk, and typically requires a bandwidth of over 30 kHz multiplied by the number of channels. It is possible therefore that a cheap kind of frequency-division-multiplex (f.d.m.) system, possibly using double-sideband transmission but even so requiring only 8 kHz per channel, could be competitive in such an application. Separate 'go' and 'return' cables might be needed, and possibly more frequent repeaters, but the economics might still be in its favour.

There are doubtless other applications for a cheap f.d.m. terminal equipment, and not only for speech but also for telegraph and data signals.

In a normal f.d.m. terminal equipment, whether of the common single-sideband type or of the double-sideband type used in rural systems,[2] the channels are combined at the sending end and separated at the receiving end through band-pass filters. These filters are required to give a high performance and are normally of the type using crystal elements. They are expensive, and indeed may represent a very sizeable fraction of the total cost of the equipment.

The aim of the f.d.m. system design to be outlined in this paper is to avoid the need for channel band-pass filters and thus to permit the cost of the terminal equipment to be greatly reduced.

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2. General Requirements

As stated above, the band-pass filters normally used to separate channels in a frequency-division-multiplex carrier telephone system are expensive, and a system which can dispense with them without introducing other expensive items is therefore economically attractive. For single-sideband systems, band-pass filters can be dispensed with at the expense of introducing phase-shifting networks which are rather difficult to design but not necessarily expensive to make. For double-sideband systems band-pass filters can in principle be dispensed with without requiring other equipment in compensation. In both cases, however, successful operation without channel-separating filters is dependent on the use of low-pass filters (which are usually quite inexpensive) to limit the audio bandwidth to that appropriate to the channel spacing, on the avoidance of second-order modulation at the channel multiplexing terminals, and on the avoidance of direct rectification of channel signals with carrier leak; otherwise interchannel crosstalk occurs. If the overall frequency band of the group of channels at the multiplexing terminals is appreciably less than an octave, no crosstalk due to orders of modulation other than the second can occur.

One practical problem of some difficulty, therefore, is the avoidance of second-order modulation at the multiplexing terminals. If the carrier frequency of a particular channel is ω_p, and if ω_a represents an audio frequency, then two kinds of second-order modulation can exist:

(i) Second-order modulation of the audio signal, giving $2\omega_p \pm \omega_a$ at the multiplexing terminals; this does not cause interchannel crosstalk if the multiplex bandwidth is less than an octave by at least one channel bandwidth; it is in any case of a low level in a ring modulator being due either to second-harmonic components in the carrier supply or to unbalance in the modulator.

(ii) Second-order modulation of signals in the multiplexed band from other channels, due to

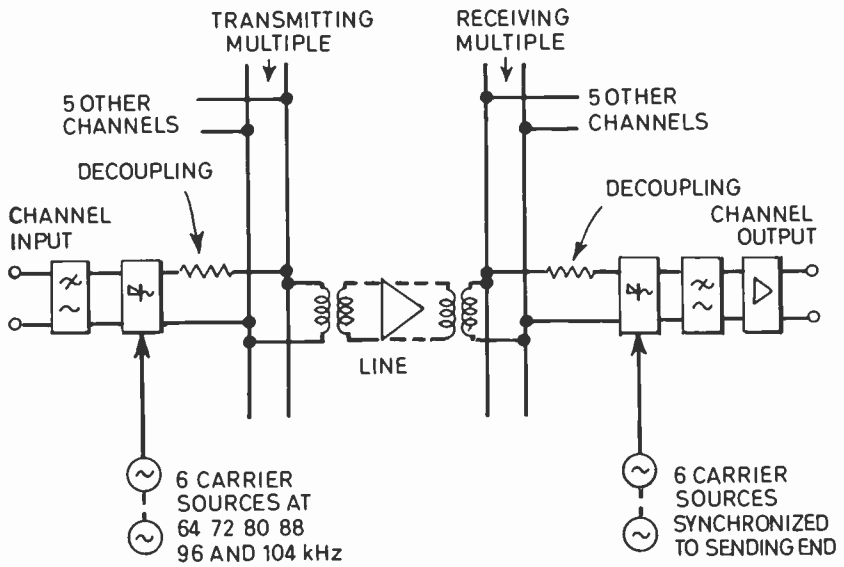


Fig. 1. General schematic of f.d.m. six-channel communication system without band-pass filters. The decoupling arrangement shown is only symbolic.

the variation with time of the modulator impedance seen at the multiplexing terminals. This applies equally to the sending and receiving ends of the system, and does cause interchannel crosstalk. For example, the signal from channel n is of frequency $\omega_{pn} \pm \omega_a$; if this gets modulated by twice the carrier frequency of channel $(n+1)$, i.e. by $2(\omega_{pn}+\omega_s)$ where ω_s is the channel separation, then frequency $\omega_{pn}+2\omega_s \pm \omega_a$ is produced—which falls in channel $(n+2)$ and thus represents interchannel crosstalk.

It is clear, therefore, that it is the second kind of second-order modulation which limits the use of systems without band-pass filters in practice. If an ordinary channel modulator is used, with a low-pass filter of Zobel image type directly connected to the audio terminals of the modulator, the second-order modulation effect type (ii), when the other end of the modulator is nominally matched, produces interfering sidebands only about 12 dB below the main ones (see Appendix 2). For the crosstalk to be acceptable (of the order of 60 dB), it is necessary either

(*a*) to use modulators which produce very little second-order modulation at their input terminals, or

(*b*) to use decoupling resistors, attenuators, or buffer amplifiers in each channel.

The constant-resistance modulator, as described in some detail in other papers,[3,4] meets requirement (*a*) and its application to the present problem is dealt with in the following section.

A general schematic diagram of a six-channel system using double-sideband transmission and no band-pass filters is shown in Fig. 1. It occupies the frequency band from 60 to 108 kHz (which is the band used in the experimental work described later), but any band of less than an octave could be used.

3. F.D.M. System using Constant-resistance Ring Modulators

The use of constant-resistance ring modulators leads to a system design of maximum simplicity. This is because of the property that the impedance at one port of the modulator is a resistance which does not vary over the carrier cycle and so produces no modulation at this port. If, therefore, this port is connected directly to the channel-combining multiple at transmitting or receiving end, no interference with other channels is produced. In practice, of course, a perfectly constant resistance is not obtained, but it has been shown[4] that if the other port of each modulator is correctly terminated in a pure resistance, if suitable rectifiers are used, and signal levels are not excessive, then modulation of the input resistance of little more than 0·1% at the second harmonic of the carrier frequency (i.e. at $2\omega_p$) can be achieved. Such a low figure cannot be expected to be maintainable over a range of operating temperature and with commercial rectifiers used without special matching, but a figure of 1% ought to be maintainable.

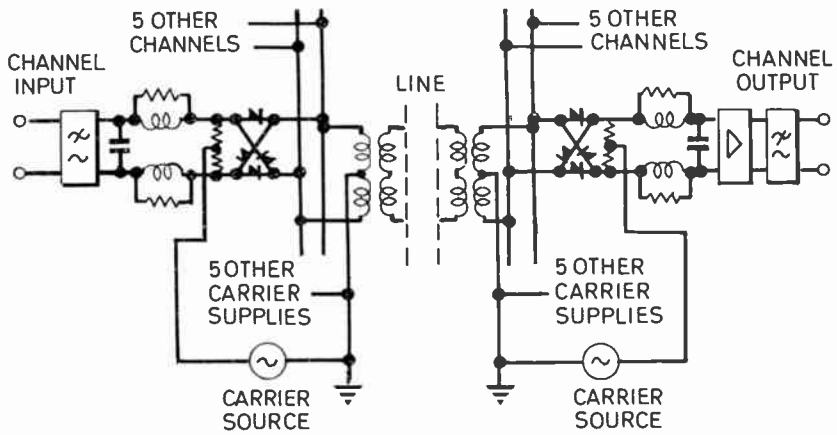


Fig. 2.

Circuit arrangement of six-channel system using constant-resistance modulators.

Note. Carrier supplies at the two ends must be synchronized in frequency and phase and must be free of interference from one to another to the extent demanded by the inter-channel crosstalk specification.

3.1. *Design Considerations*

The modulation of the input resistance of the modulator mentioned above is not a direct measure of the inter-channel crosstalk which it causes. Consider the receiving end of the system. The modulator input is fed from a low-resistance source (i.e. the multiple) comprising the other modulators in parallel with one another and with the output impedance of the line. Let this form a source resistance R_o and let the 'constant' resistance of the modulator be R_i. Then the actual crosstalk ratio, i.e. the ratio of voltage at a frequency $2\omega_p - \omega_q$, where ω_q is a sideband frequency, to voltage at the sideband frequency ω_q, is the modulation of the modulator resistance (at $2\omega_p$) reduced by the ratio $R_o/(R_o+R_i)$. In the six-channel system, assuming the line is matched to $R_i/6$, this ratio is 1/12. Expressed in decibels, the crosstalk should be 21·6 dB better than the modulation of R_i. Thus a 1% modulation (−40 dB) should lead to interchannel crosstalk, measured in terms of individual sidebands at the multiple, of about −61 dB. If the carrier frequencies are commensurate (i.e. all harmonics of a common basic frequency) the individual crosstalk sidebands add coherently in the channel in which they fall just as the wanted signal sidebands do, so that the overall crosstalk ratio due to the receiving end is also −61 dB. A similar amount of crosstalk would, however, be expected to be added at the transmitting multiple and, as this adds coherently, the overall system crosstalk would be about −55 dB.

It has been shown[4] that a suitable modulator can be made by using two rectifiers type OA85 in parallel as each element of a ring modulator, with a signal circuit impedance of around 18 kΩ, with carrier voltages across the rectifiers of the order of 100 mV and with signal levels of around 10 to 20 mV per channel. The carrier voltage can be fed via the centre point of the twin-wound 'office' winding of the line transformer; all six carrier supplies can be commoned at this point. At the other end of each modulator the use of a transformer should be avoided[3] in order to give the modulator as non-reactive a termination as possible, and a double resistance feed should be used. The arrangements are shown in detail in Fig. 2.

The arrangement of the low-pass filters and channel amplifiers in the individual channels needs some discussion. Since a non-reactive constant-resistance termination is required by the modulators on the audio side, the main filter should not be immediately adjacent to the modulator. At the receiving end the channel amplifier (which needs about 50 dB gain to give an output at zero dBm) could in principle follow the modulator directly, but in case it might be overloaded by the signals from other channels, or its input impedance should fall off and become reactive at the upper sideband of the output, $\omega_p+\omega_q$ which is of the order of $2\omega_p$, it may be advisable to precede it by a low-pass constant-resistance network[5] as shown. This network has a constant-resistance at all frequencies at the terminals facing the modulator, but can absorb stray (and other) capacitance at its other port. It has only a slow cut-off and will not be effective in restricting the output frequency range to below 4 kHz. To prevent signals from the adjacent channels appearing in the output as signals of frequency above 4 kHz, a low-pass filter should follow the amplifier or be built into it. Since these higher frequencies represent an unintelligible crosstalk at frequencies where the ear is less sensitive, a psopho-

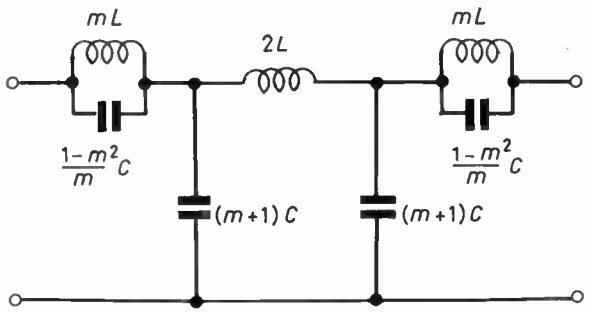


Fig. 3. Suitable low-pass filter for channels ($m = 0{\cdot}6$, L, C tune to 3·6 kHz).

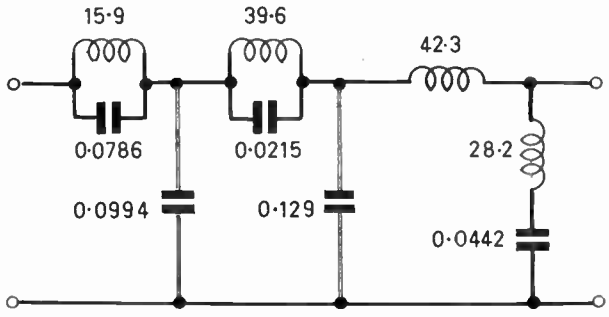


Fig. 4. Low-pass channel filter made for experimental system. Inductance values in mH, capacitance values in μF, design resistance 600 Ω.

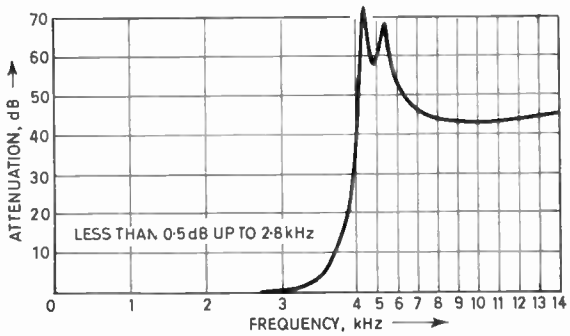


Fig. 5. Measured response of low-pass filter shown in Fig. 4.

metric weighting may be allowed; thus a reasonable filter design should give perhaps 20 dB attenuation at 4 kHz, rising to 40 dB at 4·4 kHz. The three-inductor filter shown in Fig. 3 is probably adequate. The four-inductor filter which was made for the experimental equipment (discussed later) was as shown in Fig. 4, but its measured attenuation/frequency response shown in Fig. 5 is rather better than is really needed.

At the sending end there will probably need to be an attenuator preceding the modulator in order to reduce the signal level to the 10 to 20 mV in 18 kΩ which is the maximum permissible for the constant-resistance modulator. If this is the case, the low-pass filter can probably precede the attenuator and be adequately decoupled from the modulator. If no attenuator is needed, or if its attenuation does not provide adequate decoupling, then a constant-resistance low-pass network should be used as shown in Fig. 2, with its constant-resistance port facing the modulator.

As indicated earlier, only one transformer is needed at each end. It should match the impedance of the line amplifier to that of six modulators in parallel; in the specific modulator design mentioned above this would be 3 kΩ. The loss per channel due to this parallelling of the modulators is $10 \log_{10} 6$ or approximately 7·8 dB. It is necessary that the tapped winding be wound as two twinned windings (as is usual in modulator transformers) to ensure a very low leakage inductance in the carrier path. The conversion loss of each modulator is about 5 dB.

In passing, it should be noted that each carrier supply must be quite pure, other tones being about 60 dB down if interchannel crosstalk from this cause is to be avoided.

3.2. *Other Causes of Interchannel Crosstalk*

There are several possible mechanisms for interchannel crosstalk in this system in addition to the second-order modulation of the input impedance of the modulators. Three mechanisms of which the author is aware are as follows:

(i) Harmonic sidebands may be produced in the sending-end modulators, for example if ω_p is the carrier frequency and ω_a an audio frequency, then $\omega_p \pm n\omega_a$ may be produced; if $n\omega_a$ lies outside the frequency band allocated to the channel, this product will fall within the band of another channel and will be demodulated with it, thus causing crosstalk.

(ii) Carrier leak at frequency $2\omega_p$ will be produced at the multiplexing bus-bars (or 'multiples') due to unbalance in the modulators. If this leak can be modulated by signals on the multiples, then products of the type $2\omega_p - \omega_q$ can be produced and cause crosstalk.

(iii) Carrier leak at frequency ω_p will also be produced at the multiples, and thus in the transmitted signal from each channel there will be a component corresponding to an envelope-modulated carrier, i.e. carrier plus two-sidebands. If any receiving modulator is suitably unbalanced, it can produce some rectification of this component, leading to its direct demodulation into a channel for which it is not intended.

Examining each of these causes in turn, we find that (i) is hard to calculate for the type of modulator

being used here. For a ring modulator using ideal rectifiers, however, the calculation is straightforward,[6] and the voltage ratio of a third harmonic sideband ($\omega_p \pm 3\omega_a$) to the first-order sideband can be shown to be $x^2/24$, where x is the ratio of signal voltage to carrier voltage on the modulator elements. In our case x would be of the order of 0·1, rising to perhaps 0·2 on a very strong speech signal. This would give a harmonic-sideband/first-order sideband ratio of about 4×10^{-4} rising to perhaps 16×10^{-4}, or -68 dB rising to -56 dB. This does therefore appear to be a potentially serious source of crosstalk, but in the experimental system no crosstalk due to this cause could be detected at levels (relative to the wanted signal) down to -70 dB.

Mechanism (ii) is much more difficult to deal with. Experimentally it cannot be separated from the modulation of signal by the input resistance when it departs from the constant-resistance condition. Furthermore, all carrier leak and unbalance effects are intractable in theoretical calculations. A method of determining the distribution of the products of unbalance at both input and output ports of a ring modulator is given in Appendix 1, and this is useful in showing what products *can* occur at each port, and how they may be controlled by adjustment of potentiometers in the circuit; but it does not determine the relative amplitudes.

As far as can be determined from this approach, a voltage of $2\omega_p \pm \omega_q$ is to be expected at the input port of the receiving modulators (and at the output port of the sending modulators if ω_q is still taken as the single-sideband frequency at the multiplexing bus-bars) due to the unbalance in the modulator, and it will not respond to adjustment of the potentiometers. We know, of course, that this frequency is produced by departure from the constant-resistance condition, and it is possible that the two effects are the same when the latter is due to differences between one rectifier and another. Certainly, in all the experimental work reported on the constant-resistance modulator,[3,4,7] no dependence on balancing conditions was found for the $2\omega_p \pm \omega_q$ product.

From Appendix 1 it can be seen that unbalance can lead to the products $2\omega_p \pm 2r\omega_q$, where r is an integer, but by the same arguments as used for mechanism (i), with the need for unbalance in addition, it can be seen that the effect may be expected to be negligible in practice. No crosstalk due to this effect has been detected in the experimental system.

This leaves mechanism (iii), and unfortunately this one is not negligible. In the type of modulator being considered here, leak of the carrier frequency is likely to be as large as 3 mV if specially-matched rectifiers are not used nor special balancing carried out with potentiometers. This is only a few decibels below the sideband level. As far as rectification of the envelope-modulated component is concerned, none can take place in a perfectly-balanced modulator; but, with unbalance present, there is some rectification and the outputs of the receiving modulators will all contain some of the audio signal from other channels.

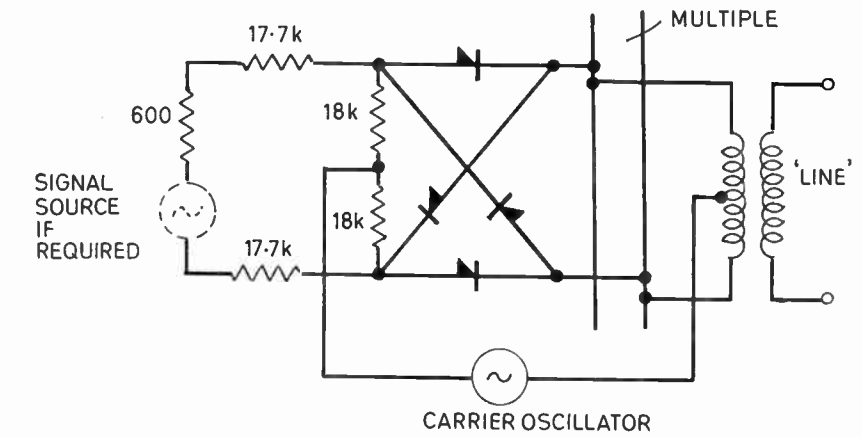
Once again, the calculation of the rectification is difficult for the actual type of modulator used, but if we consider instead the effect in a modulator using a single ideal or perfect-switch rectifier, we find it is essentially the same as the 'detector discrimination' effect in ratio detectors.[8,9] Here the well-known result is that if the weaker carrier has an amplitude ratio of x relative to the stronger carrier, then the output voltage of the demodulated signal from the weaker carrier is $mx^2/4$ times the voltage of the stronger carrier, where m is the depth of modulation in the weaker signal. If we apply this to one of the rectifiers in our modulator, we can take x as 3 mV/100 mV, i.e. 0·03, and m as unity. This gives a demodulated output of about 0·2 mV. If we then assume the balance of the modulator is such that the opposing voltages on the two sides cancel to within 3%, the resultant demodulated output is about 0·006 mV. This is the crosstalk level at a point where the signal level is of the order of 6 to 10 mV. The crosstalk ratio is therefore about -60 dB. This is the order of crosstalk due to this cause actually measured in the experimental equipment.

3.3. *Practical Experience using the Constant-resistance Modulator*

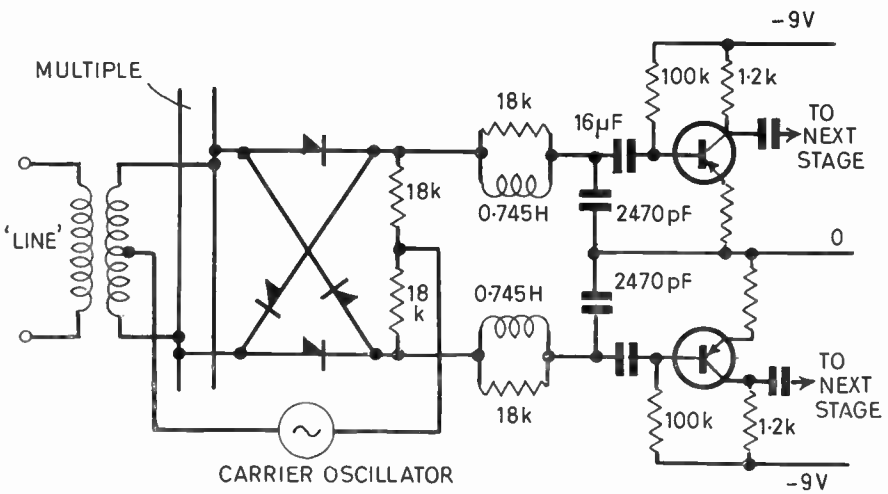
A six-channel experimental equipment was made according to the scheme of Fig. 2, with more detailed circuit information shown in Fig. 6. For tone tests, it was not necessary to use low-pass filters, and only one channel needed audio equipment, all others being terminated by a resistance at the audio side of the modulators. By interchanging carriers, all crosstalk paths could be tested. No line was used except that an attenuator was connected between transmit and receive multiples, and it was checked that no adverse effect occurred when all the attenuation was removed, leaving the multiples directly connected.

The carrier supplies were taken from six independent oscillators, each one supplying the appropriate modulators at sending and receiving ends. Since there was negligible phase-shift in the system between the modulators at the two ends, correct phasing was thus assured.

If the carriers had been harmonically related (e.g. by being harmonics of a common basic frequency), then crosstalk occurring by the second-order modulation of the modulator impedance and that due to mechanism (iii) mentioned in Section 3.2 would be



(a) Transmit end.



(b) Receive end.

Fig. 6. Details of experimental system.
Note. Each rectifier shown is two OA85's in parallel.

indistinguishable, a tone of frequency f being received by both mechanisms in the channel suffering crosstalk when f was being transmitted on the sending channel; the only difference would be that mechanism (iii) would cause crosstalk into all channels and the second-order modulation would cause it only in one channel. But as only one channel was equipped for full reception, this slight distinction could not be used. Consequently, use was made of the independence of the carrier oscillators to cause the crosstalk outputs to be separated in frequency.

Consider a particular crosstalk test. A tone of 2·2 kHz was fed into channel 1 (64 kHz carrier). Second-order crosstalk was produced by the channel 2 modulators, the carrier frequency of which was $(72+\delta_1)$ kHz. Crosstalk was measured in channel 3 with a carrier frequency of $(80+\delta_2)$ kHz. Here δ_1 and δ_2 are arbitrary small frequency errors. The signal sidebands at the multiplexing bus-bars were 61·8 and 66·2 kHz. The former produced a crosstalk into channel 3 at $2{\cdot}2-(2\delta_1-\delta_2)$ kHz; the latter produced crosstalk at $2{\cdot}2+(2\delta_1-\delta_2)$ kHz. Crosstalk due to the rectification effect of mechanism (iii) was at 2·2 kHz since no frequency-translation was involved. Thus the separate causes could easily be distinguished and separately measured. Other tests were also made to check the mechanisms of crosstalk, e.g. by showing that the crosstalk at 2·2 kHz was independent of the 72 and 80 kHz oscillators, while the other crosstalk outputs were dependent on them.

It was found that there was comparatively little variation in crosstalk ratios from channel to channel,

although the modulators had been made up under production conditions without special matching of the rectifiers. The crosstalk at 2·2 kHz, due to carrier leak and rectification, was consistently of the order of −65 dB relative to the wanted signal level, with carrier leak at the multiplexing bus-bars of the order of 10 dB below the sideband levels. It could be made worse by adding resistors in the modulators to deliberately unbalance them by large amounts. It was not very sensitive to signal level at the sending modulators, presumably because the component of envelope modulation was not affected much so long as there was a surplus of signal-sideband over carrier leak. An addition of 10 dB in the line loss reduced the crosstalk output by only 5 dB, and this seems more surprising.

The crosstalk ratio at $2{\cdot}2 \pm (2\delta_1 - \delta_2)$ kHz, due to second-order modulation in the modulator impedances, was consistently worse than that at 2·2 kHz, being typically −55 to −60 dB for each tone. Variations occurred over periods of time, presumably due to temperature variations (which were very considerable during the period of test, but were not recorded). Crosstalk ratios as bad as −45 dB were obtained. Such ratios were not at all sensitive to the level of the signal applied to the channels. If better crosstalk ratios are essential in a particular design, it would be wise to add some swamping (or decoupling) resistance at the modulator ports on the multiplexing side. For example, 6 kΩ resistors connected across each modulator port, or 1 kΩ across the multiple, with consequent rematching of the line transformer ratio, would improve crosstalk by 12 dB at the expense of 6 dB in the channel attenuation at each end.

When the carrier oscillators were set up carefully to be harmonically related, so that the various crosstalk outputs in each channel coincided in frequency, it was found possible to cause the two mechanisms of crosstalk to cancel out very substantially. The second-order crosstalk could not readily be controlled, but the addition of a potentiometer in the connection of the carriers to the centre of the transformer winding enabled carrier leak to be adjusted in magnitude and polarity, and resultant crosstalk ratios in the range −60 to −70 dB could easily be obtained. Such results were not, of course, very stable over a period of time and would hardly form a satisfactory basis for an operational system.

4. The Use of Ordinary Ring Modulators

Since one has to go to some trouble to obtain the constant-resistance condition, it is worth enquiring as to whether a modulator used at a more normal impedance level (say 600 Ω) and with more tolerance of higher signal levels could give an adequate performance.

Experimental measurements of the input modulation were made[7] on a ring modulator using the same OA85 rectifiers as the constant-resistance modulator, but with higher carrier voltages and terminating resistance of 600 Ω on the audio side. The relative level of the $(2\omega_p - \omega_a)$ product occurring at the input terminals when the signal at frequency $(\omega_p - \omega_a)$ was fed from a constant-current source is shown in the table below. Here $\hat{V}_c$ is the peak carrier voltage across the rectifiers, the carrier being fed from a high-resistance source so that the waveform of V_c was nearer to a square shape than a sinusoid.

$\hat{V}_c$ (volts)	0·5	1·0	1·5	2·0
Level of $(2\omega_p - \omega_a)$ relative to signal voltage (dB)	−19	−27	−29	−31

These results were found to be insensitive to signal voltage level up to at least 100 mV.

Use of a low-impedance carrier supply (which would be more economical of carrier power) would worsen these figures considerably, and although no systematic investigation was made using a low-impedance carrier, some rough tests suggested that the relative levels of $(2\omega_p - \omega_a)$ would not be better than −20 dB at any carrier voltage.

These figures lead to interchannel crosstalk of the order of −40 dB, which is of course unacceptable. It could be improved by inserting attenuators between the modulator and the multiplexing terminals, and this would be reasonably convenient in view of the higher signal levels that are usable with these modulators of low-impedance and high carrier voltage. Attention then needs to be paid to the carrier feed arrangements, since the use of a common return to the centre-point of the line transformer is no longer reasonable. A separate transformer for each modulator is really required, but this unfortunately adds to the cost.

The low-impedance arrangement discussed above is still, of course, an approximation to a constant-resistance modulator. The increased carrier voltage ensures that over a large part of the carrier cycle the rectifiers are either very low or very high resistances, so that if the load is a constant pure resistance at all frequencies, the input resistance is not grossly different from it. But if the modulator is used with no attempt at all to approximate to the constant-resistance condition, very much worse results are obtained. For example, it is shown in Appendix 2 that if a modulator is terminated at the audio end by a Zobel-type *filter* instead of the constant-resistance selective network shown in Fig. 1, the relative level of $(2\omega_p - \omega_a)$ is only about −12 dB.

The crosstalk due to carrier leak and rectification in these modulators tends to be worse than in the constant-resistance modulators because the much larger carrier voltages cause a disproportionately very much larger carrier leak. The insertion of attenuators between the multiplexing bus-bars and the modulators at the receiving end, however, has a beneficial compensating effect because it reduces the level of the signal relative to the carrier voltage of the receiving modulator. Experiments made using modulators as above suggest that crosstalk ratios of the order of -55 to -65 dB may be expected from this cause.

The carrier power required to drive the low-impedance modulators is, of course, vastly greater than that used in the constant-resistance system, and might be a source of considerable extra cost.

All in all, it seems that the constant-resistance modulator forms a much better basis for system design than the use of ordinary modulators.

5. The Use of Shunt Modulators

If constant-resistance modulators (preferably of the ring type) are used as recommended in the simple system of Fig. 2, then not only is the very undesirable second-order modulation avoided, but there is, in principle, no modulation at the multiplexing terminals of any kind whatever. If the system bandwidth is restricted to less than an octave, this last fact is of only secondary value, although it would become vital if larger bandwidths were required. Therefore, in the system of less than an octave, it is not strictly necessary to specify a constant-resistance modulator, but only a modulator which does not give second-order modulation at the multiplexing terminals. The shunt modulator (or for that matter, the series modulator) can be made[10] to produce no even-order modulation if

(i) the resistance/voltage law of the rectifiers is the same as is required for the constant-resistance ring modulator, namely

$$r(V_c) = a\exp(-bV_c)+r_0 \qquad \text{.....(1)}$$

over the relevant range of the carrier voltage V_c; here a, b and r_0 are constants;

(ii) the resultant circuit impedance (i.e. the signal source impedance and the load impedance in parallel for the shunt modulator or in series for the series modulator) is a constant resistance over time and at all relevant frequencies, such that its value R conforms to the equation

$$[r(+V_c)-r_0][r(-V_c)-r_0] = (R+r_0)^2 \qquad \text{.....(2)}$$

and

(iii) the carrier waveform must be the same on the backward half-cycle as on the forward; this can be achieved by connecting the corresponding modulators of another system to the carrier supply in opposite polarity.

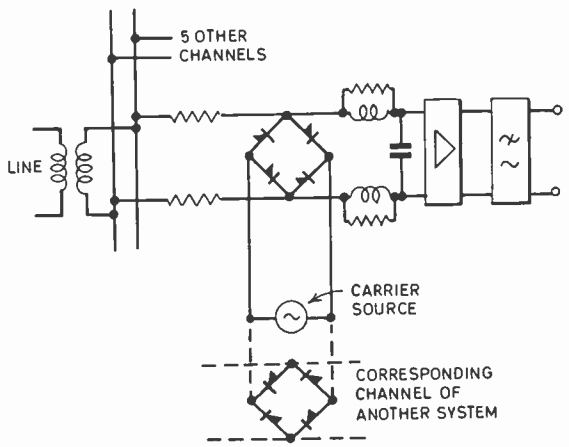


Fig. 7. Receiving-end circuit using shunt modulator.

It thus seems that the shunt (or series) modulator can be used in this application. It appears at first sight that condition (ii) may be spoilt by the fact that the other modulators, paralleled across the input or output of a particular channel modulator, provide a contribution to R which is varying with time. But the time variations of the other modulators contain no even-order harmonics of the carrier frequency, and are therefore not such as to spoil the operation of the one we are considering. There is, however, also an additional factor: it is not possible for the other modulator impedances connected in parallel with one another (in parallel with the line impedance too) to give the required resultant impedance at the level of $2R$, which when taken in parallel with an audio impedance of $2R$ would provide the resistance R required by eqn. (2). Thus a series resistance is needed in the connection between the multiplexing terminals and the modulator, giving the overall circuit schematic shown in Fig. 7. The series resistance produces about 10 dB loss in the channel, but of course gives 20 dB reduction in any second-order modulation which is produced due to errors in the rectifier law of eqn. (1). Since the shunt (or series) modulator has a conversion loss which is 6 dB greater than that of the corresponding ring modulator, it is evident that counting the series resistance the channel loss is very much greater than with the constant-resistance modulator in the scheme of Fig. 2. Clearly the system shown in Fig. 2 is preferable to that of Fig. 7.

6. Conclusions

Although it is apparent that there are several possibilities in the design of a f.d.m. system without band-pass filters, it is reasonable to conclude that the use of a properly-designed constant-resistance modulator is the best basis for a design of maximum economy.

7. Acknowledgments

The author wishes to record his thanks to Messrs. G. Terreault and J. R. Robertson, whose experimental work on the constant-resistance modulator formed the foundation for this study, and to Messrs. B. L. J. Kulesza and C. S. Nokes, who built and carried out the tests on the experimental six-channel system.

8. References

1. See series of seven papers on p.c.m. for this application in *G.E.C. Telecommunications*, No. 35, 1967.
2. 'Rural carrier telephone equipment for open-wire lines', *G.E.C. Telecommunications*, No. 23, p. 42, 1957.
3. D. G. Tucker and G. Terreault, 'The performance of practical constant-resistance modulators in relation to their use in f.d.m. systems', *The Radio and Electronic Engineer*, **31**, No. 5, p. 314, May 1966.
4. D. G. Tucker, 'Input modulation (i.e. inter-channel cross-talk) in constant-resistance modulators for use in f.d.m. systems', *Proc. Instn Elect. Engrs.*, **114**, p. 1385, October 1967.
5. O. J. Zobel, 'Distortion correction in electrical circuits with constant resistance recurrent networks', *Bell Syst. Tech. J.*, **7**, p. 438, 1928.
6. D. G. Tucker, 'Intermodulation distortion in rectifier modulators', *Wireless Engineer*, **31**, p. 145, 1954.
7. J. R. Robertson, unpublished report, Department of Electronic and Electrical Engineering, University of Birmingham, September 1966.
8. E. V. Appleton and D. Boohariwalla, 'The mutual interference of wireless signals in simultaneous detection', *Wireless Engineer and Experimental Wireless*, 9, p. 136, March 1932.
9. D. G. Tucker, 'Modulators and Frequency Changers', p. 39, (Macdonald, London, 1953).
10. D. G. Tucker, 'Circuits with Periodically-Varying Parameters', Chapter 8, (Macdonald, London, 1964).
11. D. G. Tucker, 'Unbalance effects in modulators', *J. Brit. Instn Radio Engrs*, **15**, p. 199, April 1955.
12. D. G. Tucker, 'Zero-loss second-order ring modulator', *Electronics Letters*, **1**, p. 245, October 1965.
13. D. G. Tucker, 'The second-order ring modulator: calculations of losses and some design considerations', *Proc. Instn Elect. Engrs*, **113**, p. 1457, September 1966.

9. Appendix 1:

Unbalance Effects at the Input and Output Terminals of Ring Modulators

Unbalance effects in modulators are difficult to calculate in terms of magnitudes, but a previous paper[11] has shown a basis for the deduction of the nature of the effects, and, in particular, for the use of potentiometers to reduce or eliminate leakage of particular products. The previous work was directed to the normal kind of modulators, and in considering the ring modulator was concerned only with leakage of unwanted frequencies into the output of the lattice. In the present paper we have seen that unbalance effects are important at the input as well as the output port. There are other applications too where input-port leak is important, e.g. the second-order ring modulator[12,13] where the normal output port of the lattice is terminated in an 'idler' load, and the required modulation-product output (at $2f_c \pm f_s$, where f_c is the carrier frequency and f_s is the signal frequency) is taken from the *input* port of the lattice.

We consider, for purposes of analysis, the ring modulator shown in Fig. 8. P1, P2, P3 and P4 are balancing potentiometers; R_1 and R_2 are provided to compensate for the mean resistance of P2 and P4. Since we are attempting to analyse only the nature and not the magnitude of the effects, several simplifications can be made. These are

(i) the circuit is wholly non-reactive and the transformers are ideal,

(ii) the signal and carrier sources have zero impedance (i.e. Z_s and $R_c = 0$),

(iii) the wanted products are taken as the current through a zero load impedance (i.e. $Z_L = 0$),

(iv) one-half of the signal voltage $V_s \cos 2\pi f_s t = 2b$ appears across each rectifier in spite of unbalances.

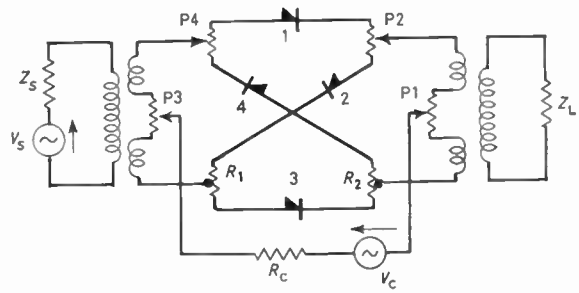


Fig. 8. Ring modulator with balancing potentiometers.

The carrier voltage $V_c \cos 2\pi f_c t$ is called a, and taking the polarity of currents and voltages in each rectifier relative to the direction of best conduction, the voltages across the four rectifiers 1, 2, 3 and 4 are respectively $(a+b)$, $-(a-b)$, $(a-b)$ and $-(a+b)$.

Let the current through a rectifier be related to the voltage across it by the power series

$$i = \sum_{n=0}^{\infty} d_n v^n \qquad \text{.....(3)}$$

In general the four rectifiers have different sets of coefficients d_{n1}, d_{n2}, d_{n3} and d_{n4}.

The current through the input terminals of the lattice is

$$\begin{aligned} i_1+i_2-i_3-i_4 &= \sum d_{n1}(a+b)^n+\sum d_{n2}(-1)^n(a-b)^n- \\ &\quad -\sum d_{n3}(a-b)^n-\sum d_{n4}(-1)^n(a+b)^n \quad \ldots\ldots(4) \\ &= \tfrac{1}{2}\sum[d_{n1}-(-1)^n d_{n2}+d_{n3}-(-1)^n d_{n4}]\times \\ &\quad \times[(a+b)^n-(a-b)^n]+ \\ &\quad +\tfrac{1}{2}\sum[d_{n1}+(-1)^n d_{n2}-d_{n3}-(-1)^n d_{n4}]\times \\ &\quad \times[(a+b)^n+(a-b)^n] \quad \ldots\ldots(5) \end{aligned}$$

Now a few trial expansions of $[(a+b)^n \pm (a-b)^n]$ for different values of n will quickly show that there are four groups of frequencies (where m and n are integers or zero):

(A) $2mf_c \pm (2r+1)f_s$ arising from $(a+b)^n-(a-b)^n$, n odd.

(B) $2mf_c \pm 2rf_s$ arising from $(a+b)^n+(a-b)^n$, n even.

(C) $(2m+1)f_c \pm 2rf_s$ arising from $(a+b)^n+(a-b)^n$, n odd.

(D) $(2m+1)f_c \pm (2r+1)f_s$ arising from $(a+b)^n-(a-b)^n$, n even.

Group (A) clearly includes the unwanted products $2f_c \pm f_s$ and has amplitude

$$d_{n1}+d_{n2}+d_{n3}+d_{n4} \quad \ldots\ldots(6)$$

which of course cannot be brought to zero by adjustment of any of the potentiometers, although it does reduce to zero in the constant-resistance condition.

Group (B) can be balanced out if we can obtain

$$d_{n1}+d_{n2}-d_{n3}-d_{n4}=0 \quad \ldots\ldots(7)$$

and this can be achieved (for a particular value of n) by adjustment of either P1 or P4.

Group (C) can be balanced out if we can obtain

$$d_{n1}-d_{n2}-d_{n3}+d_{n4}=0 \quad \ldots\ldots(8)$$

and this can be achieved by adjustment of P2 or P3.

Group (D) can be balanced out if we can obtain

$$d_{n1}-d_{n2}+d_{n3}-d_{n4}=0 \quad \ldots\ldots(9)$$

and this can be achieved by adjustment of P2 or P4.

To a first approximation only three of the four potentiometers are needed to give a zero current at the greatest possible number of particular frequencies from Groups B, C and D since there are only three independent eqns. (7, 8 and 9) to be satisfied. Only if the appropriate condition (7), (8) or (9) can be met simultaneously for all values of n can all frequencies in a group be balanced out, and this is clearly unlikely with practical rectifiers; but as the differences between rectifiers are likely to be greater in the scale of the current/voltage characteristic than in its shape, one would expect some tendency for the unbalance currents at all frequencies in a group to be small as one of them is brought to zero by a potentiometer adjustment. This expectation is supported by the experimental observations reported for the currents at the output of the lattice in reference 11.

Experience (as e.g. in Fig. 4 of Reference 11) suggests that those leakage or unbalance currents of frequencies which involve f_s (i.e. all product frequencies other than harmonics of the carrier) have usually-negligible magnitudes, very much smaller than the carrier leak multiplied by V_s/V_c; and this is largely due to the fact that in practical modulators (as compared with the simplified model used above) the signal voltage appearing across the rectifiers is only a fraction of the signal voltage applied to the modulator owing to the effect of a finite load impedance. Thus in the second-order ring modulator the unwanted current at frequency $f_c \pm f_s$ (for example) at the input of the lattice is very small compared with the wanted current at $2f_c \pm f_s$. In the constant-resistance modulator, where ideally no modulation product frequencies occur at the input, it is normally departures from the constant-resistance condition which cause $2f_c \pm f_s$ to appear there and this has been found in experiments [3,7] to be the dominant effect.

Table 1

Summary of effects of potentiometers (m and r are integers or may be zero)

Potentiometer	Frequencies controlled at input of lattice	Frequencies controlled at output of lattice
P1	$2mf_o \pm 2rf_s$	$(2m+1)f_o \pm 2rf_s$
P2	$(2m+1)f_o \pm 2rf_s$	$2mf_o \pm 2rf_s$
	$(2m+1)f_o \pm (2r+1)f_s$	$2mf_o \pm (2r+1)f_s$
P3	$(2m+1)f_o \pm 2rf_s$	$2mf_o \pm 2rf_s$
P4	$2mf_o \pm 2rf_s$	$(2m+1)f_o \pm 2rf_s$
	$(2m+1)f_o \pm (2r+1)f_s$	$2mf_o \pm (2r+1)f_s$

Finally the results of both this and the previous examination[11] of the effects of the potentiometers are summarized in Table 1. This is a useful comparison of the effects at the input and output of the lattice, for it shows, among other things, that carrier leak (i.e. f_c and harmonics of f_o) can be controlled by P1 to give a good balancing-out of f_c at the output of the lattice or of $2f_c$ at the input; and often one balancing adjustment will give low leaks of both simultaneously. Similarly P3 will deal with d.c. and $2f_c$ at the output and f_c at the input. P1 and P3 are the balancing

potentiometers normally used in modulators, since carrier leak is usually the most serious unbalance product. The use of P2 and P4 is unusual, but one or other is essential if leakage of the input signal into the output of the lattice is to be eliminated, or leakage of $f_c \pm f_s$ into the input.

10. Appendix 2:

Second-order Modulation in Ring Modulators Terminated by a Filter

The problem considered here is the calculation of the second-order modulation at the input terminals of the modulator when its output is connected directly to a low-pass filter of normal type (e.g. Zobel image-type filter). Such a filter has an image impedance which is a frequency-dependent resistance in the pass-band and a pure reactance in the stop-band. The actual input impedance of the filter is only the same as the image impedance when the filter is image-matched at its output, but clearly the input impedance departs very greatly from the constant resistance needed to terminate the modulator used in the constant-resistance mode of Fig. 2.

If we take as an example the extreme case when the input impedance is the image impedance, and then take this to be a pure resistance at the wanted audio frequency $\omega_p - \omega_q$ (where ω_p = carrier and ω_q = frequency at the multiplexing bus-bars) and a zero† reactance (i.e. short-circuit) at all other output side-band frequencies, we find that, instead of being a constant-resistance modulator with negligible even-order modulation at the input terminals, the modulator is in fact a highly-efficient even-order modulator giving even-order products at the input terminals only a few decibels below the applied signal. Indeed, a very similar arrangement has recently been put forward and investigated as an advantageous modulator for second-order modulation.[12,13] Adapting the analysis of Reference 13, the actual value of the ratio of the currents at ω_q and $2\omega_p - \omega_q$ at the input is calculated below with some specified assumptions.

We make the following assumptions:

(*a*) the rectifiers are ideal switches without resistance (i.e. forward resistance = 0, backward resistance = ∞);

(*b*) the output of the modulator is terminated with a filter which effectively gives a termination of R_1 at the audio frequency $\omega_p - \omega_q$ but zero at all other relevant frequencies;

(*c*) the signal source has a resistance R at all frequencies.

† If the filter has the other type of image impedance, so that 'zero' should here be replaced by 'infinite', then the whole of the results apply just the same provided the ratio R_1/R is inverted to R/R_1.

These differ from the conditions considered in Section 4 of Reference 13 only in respect of the substitution of the resistance R_1 for a finite reactance. The analysis of Reference 13 can thus be easily adapted, and with $V \cos \omega_q t$ representing the applied signal, eqn. (48) of Reference 13 becomes for the present case:

$$V - [R + R_1(4/\pi^2)]i_0 = R_1(4/\pi^2)\left(\frac{\pi^2}{4} - 1\right) i_2 \quad \ldots\ldots(10)$$

where i_0 is the input current at frequency ω_q and i_2 is the current at the input terminals at frequency $2\omega_p - \omega_q$. Also eqn. (39) of Reference 13 gives us for the present case

$$\frac{i_0}{i_2} = -\frac{R + R_1(4/\pi^2)\left(\frac{\pi^2}{4} - 1\right)}{R_1(4/\pi^2)} \quad \ldots\ldots(11)$$

The ratio of the currents, i_0/i_2, is probably of main interest here, but the use of eqn. (11) applied to eqn. (10) will also enable us to obtain the ratio of the voltages at ω_q and $2\omega_p - \omega_q$, i.e. $(V - Ri_0)/Ri_2$.

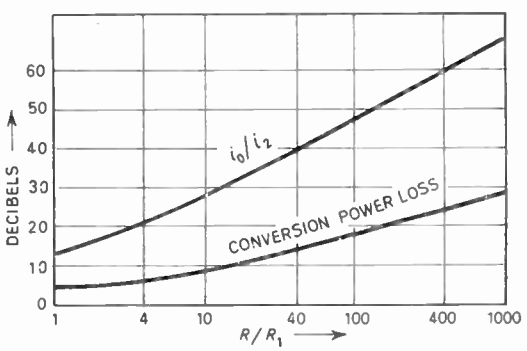


Fig. 9. Graph showing second-order modulation in a ring modulator terminated in an image-type low-pass filter, together with conversion power loss, plotted as functions of R/R_1, where R is the nominal circuit impedance before the modulator and R_1 is the pass-band image impedance of the filter.

The ratio i_0/i_2 expressed in decibels is plotted in Fig. 9 as a function of R/R_1. One would suppose a normal choice of R_1 would be to make it equal to R. The second-order interference current i_2 is then only 12 dB below the input current, and this is the figure which has already been quoted in the paper.

As R_1 is increased, this ratio worsens to a limit of 1·67 dB when R_1 becomes infinite. As R_1 is decreased, however, the ratio improves, and the desired ratio, which we may take to be 60 dB, is attained when $R_1 = R/400$. It is thus important to know what happens to the conversion loss of the modulator when

R_1 is made very small, as this might be an alternative to the use of decoupling circuits between the multiplexing bus-bars and the modulator.

The relevant measure of the conversion loss is the conversion-power loss (c.p.l.) ratio defined as:

$$\text{c.p.l. ratio} = \frac{\text{power available from signal source}}{\text{power in load at } \omega_p - \omega_q} \qquad \text{.....(12)}$$

$$= V^2/4RR_1 i_1^2 \qquad \text{.....(13)}$$

where i_1 is current at frequency $\omega_p - \omega_q$. From eqn. (13), therefore,

$$\text{c.p.l. ratio} = \frac{\pi^2}{4} \cdot \frac{(R+R_1)^2}{4RR_1} \qquad \text{.....(14)}$$

This ratio, expressed in decibels, is also plotted in Fig. 9, and will be seen to increase as R_1 decreases. At the value $R_1 = R/400$ which was required to reduce the interference to 60 dB below the signal, the conversion power loss is 24 dB. The difference in dB between the interference ratio and the c.p.l. ratio is seen from eqns. (11) and (14) to approach the value

$$20 \log_{10} \pi \sqrt{R/R_1} \quad \text{dB} \qquad \text{.....(15)}$$

as R_1 becomes very small compared with R.

It should be remembered that the above calculations have assumed that the rectifiers operate as perfect switches. When used in the exponential region (as in the constant-resistance design considered in this paper) with a reasonable carrier voltage, so that a high ratio of maximum to minimum resistance is obtained, and with normal terminating impedances, the conversion loss is increased by between 1 and 2 dB, and the interference current is reduced by perhaps 2 to 3 dB. But with the extremely low values of R_1 discussed above, this difference is probably greatly increased.

It can be seen that this method of reducing the second-order modulation at the multiplexing bus-bars has exactly the same effect on the overall attenuation in the channel as the decoupling method discussed in the paper.

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V.H.F. Field Strength Measurements over Medium Length Land Paths

By

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Summary: Field strength measurements were made over several overland transmission paths on Bands I and II, at distances up to 274 km. The measurements when corrected for transmitting aerial height above mean terrain and also for receiving site variation factor give field-strength/distance curves which are in reasonable agreement with the current C.C.I.R. tropospheric propagation curves. The range of fading and field strength exceeded in each month for specified time-percentages are also discussed.

1. Introduction

During 1959 the European Broadcasting Union submitted a document to the C.C.I.R. Study Group V in the form of a draft study programme which pointed out the desirability of obtaining statistical information on the fading characteristics of v.h.f. and u.h.f. signals within the distance range 0–200 km. The importance of this information arose from the fact that with the planning of v.h.f. and u.h.f. transmitter networks minimum distance separations between transmissions on adjacent or image channels might be relatively small, whereas the separation distances of co-channel stations could be readily assessed by means of the then existing (and subsequently revised) C.C.I.R. tropospheric propagation curves. The C.C.I.R. Los Angeles Plenary Assembly accepted the draft study programme, which was then formulated as Study Programme No. 140 and subsequently revised as part of the current Study Programme No. 189 of the Geneva Assembly in 1963.

This paper describes measurements made by the B.B.C. during 1961 and 1962 which were submitted to the C.C.I.R. as a contribution to the Study Programmes. Although the data are primarily for v.h.f. broadcast planning the radio wave propagation information is of interest in assessing the performance of the Instrument Landing System for aircraft.[1] It is decided, therefore, to give a wider circulation to the detailed measurements.

Field strength records were made of a selection of B.B.C. transmissions over paths ranging in length from 62 to 274 kilometres. Two receiving sites were used, one at the B.B.C. Monitoring Station, Caversham Park, Oxfordshire, and the other at an unattended radio station at Mursley, Buckinghamshire. Four Band I television sound and four Band II f.m. sound broadcasting transmissions were measured at each of the receiving sites, giving in all propagation data for sixteen transmission paths. The measurements were carried out over the period from June 1961 to December 1962. Further measurements were made during the latter half of 1963 for the purpose of obtaining corrections for normalizing the long-term measured field strengths to be representative for 50% of locations.

2. Sites, Equipment and Analysis

2.1. *Sites*

Figure 1 shows the geographical distribution of the transmitting and receiving sites. Further details of the sites are also given in Tables 1 and 2.

2.2. *Equipment*

The main features of the receivers are their reliability and gain stability when used over a long period of time. The Band I receiver intermediate frequency is 270 kHz and the selectivity response is substantially constant over ± 5 kHz, falling by 45 dB at ± 20 kHz. This narrow pass-band rejects the sound carriers of other co-channel transmitters offset by 20 kHz. The Band II receiver intermediate frequency is 2·2 MHz and the selectivity response is reasonably constant over a range of ± 40 kHz, falling by 6 dB at ± 75 kHz and 50 dB at ± 200 kHz. The receivers for both bands have a logarithmic input/output characteristic over a range of 50 dB, but the overall gain of the receivers may be adjusted to suit the median signal for a particular path by means of attenuators inserted between the signal- and intermediate-frequency units.

At the receiving sites, the output of each receiver was connected to a voltage coder[2] which was common to the eight receivers. The coder sampled the signal of each receiver sequentially and, depending upon the field strength value, converted it to one of thirty-one levels of a five-unit binary code. The signal level was then recorded on punched paper tape. The time

† British Broadcasting Corporation, London, W.1.

Table 1

Transmitting site details

Location	Frequency MHz	Site height a.m.s.l. m	Aerial height a.g.l. m	Aerial polarization	Latitude	Longitude
Crystal Palace	41·5	110	130	V	51°25′20″N	00°04′17″W
North Hessary Tor	48·23	509	193	V	50°32′59″N	04°00′26″W
North Hessary Tor	88·1	509	164	H	50°32′59″N	04°00′26″W
Peterborough	63·27	56	127	H	53°30′26″N	00°20′30″W
Peterborough	90·1	56	99	H	53°30′26″N	00°20′30″W
Rowridge	88·5	137	90	H	50°40′34″N	01°22′02″W
Sutton Coldfield	58·25	169	224	V	52°35′59″N	01°49′57″W
Sutton Coldfield	88·3	169	197	H	52°35′59″N	01°49′57″W
Wenvoe	63·25	128	224	V	51°27′32″N	03°16′48″W
Wenvoe	89·95	128	197	H	51°27′32″N	03°16′48″W
Wrotham	89·1	219	124	H	51°19′11″N	00°17′20″E

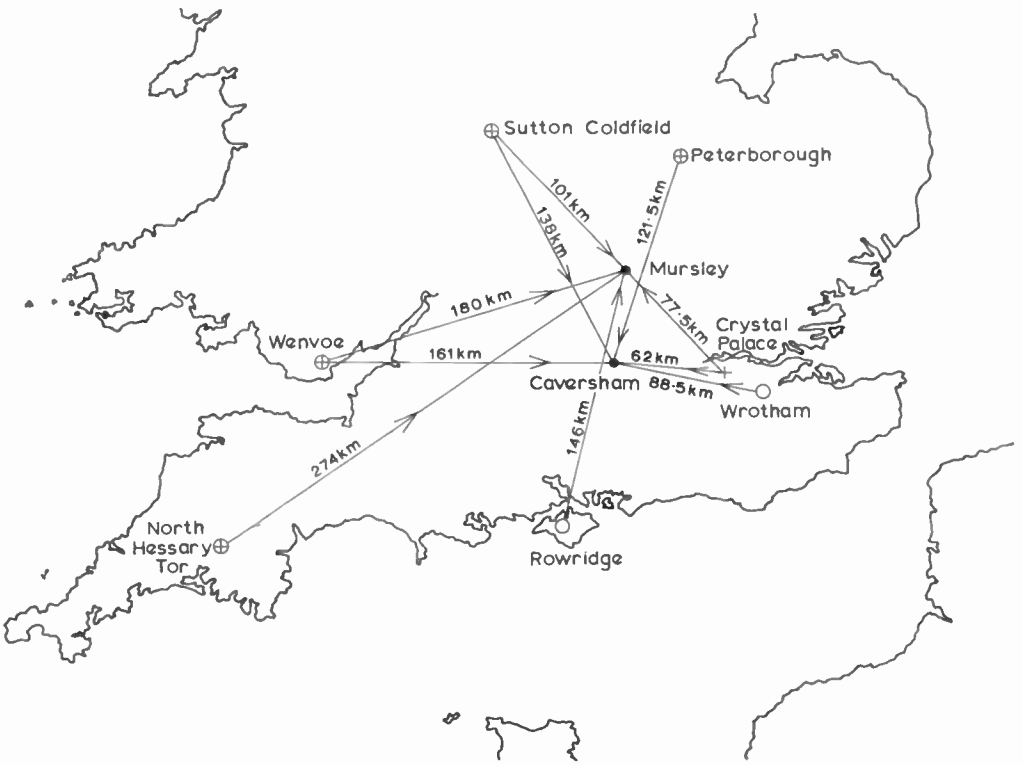


Fig. 1. Geographical distribution of transmitting and receiving sites.

● Receiving sites
○ Transmitting site (Band II)
+ Transmitting site (Band I)
⊕ Transmitting sites (Bands I and II)

Table 2

Receiving site details

Receiver location	Transmitter location	Path distance	Receiving site				
			Site height a.m.s.l.	Approximate aerial height a.g.l.	True bearing to transmitter	Latitude	Longitude
		km	m	m			
Caversham	Crystal Palace	62·0	82·3	11·0	95°	51°28′52″N	00°57′23″W
,,	Peterborough	121·5	,,	,,	19°	,,	,,
,,	Sutton Coldfield	138·0	,,	,,	334°	,,	,,
,,	Wenvoe	161·0	,,	,,	270°	,,	,,
,,	Wrotham	88·5	,,	,,	101°	,,	,,
Mursley	Crystal Palace	77·5	158	9·1	140°	51°57′12″N	00°48′05″W
,,	North Hessary Tor	274·0	,,	,,	236°	,,	,,
,,	Rowridge	146·0	,,	,,	195°	,,	,,
,,	Sutton Coldfield	101·0	,,	,,	317°	,,	,,
,,	Wenvoe	180·0	,,	,,	253°	,,	,,

required for a complete cycle for sampling the output of the eight receivers was four minutes and the signal from each receiver was thus sampled fifteen times per hour.

Pen recorders were also connected to the outputs of the receivers to provide signal records that could be visually examined for the presence of interference and for occasional checking of the accuracy of the punched paper tape data. The recording charts were run at a speed of 2 inches (5·1 cm) per hour.

Conventional commercial-type Bands I and II dipoles or 'H' aerials were used at the receiving sites. At Caversham they were mounted on the top of a building at a height of approximately 36 ft (11 m) above ground level (a.g.l.). Similar aerials were used at Mursley, mounted on tubular masts at a height of about 30 ft (9·1 m) a.g.l.

2.3. *Analysis*

The punched tape at each receiving site was renewed at the end of every month and the used tape returned to base for analysis. Originally, the tape containing the field strength data was fed into a thirty-one level analyser which counted the number of times each level of field strength was recorded. The field strength exceeded for certain fixed time-percentages was then manually calculated from the cumulative distribution of the sampled data. During the series of measurements, however, the B.B.C. acquired a computer and the work of analysing the punched tape was subsequently transferred to the computer.

The records of the measurements were analysed to determine the length of time during which the signal levels exceeded various values of field strength. These time durations, expressed as percentages of the overall valid recording time, were then plotted against field strength normalized for an effective radiated power (e.r.p.) of 1 kW. Separate graphs were prepared for each transmission path.

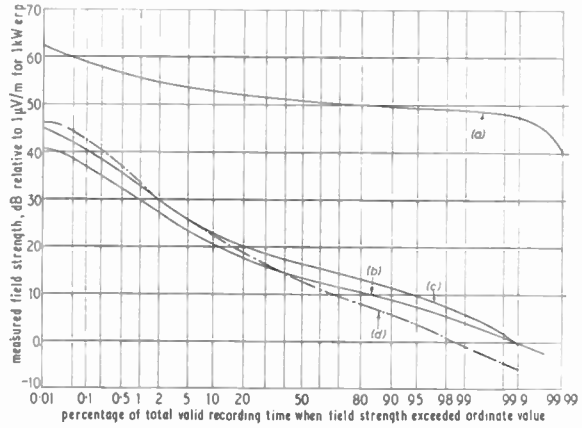
3. Results

3.1. *Variation of Field Strength with Time*

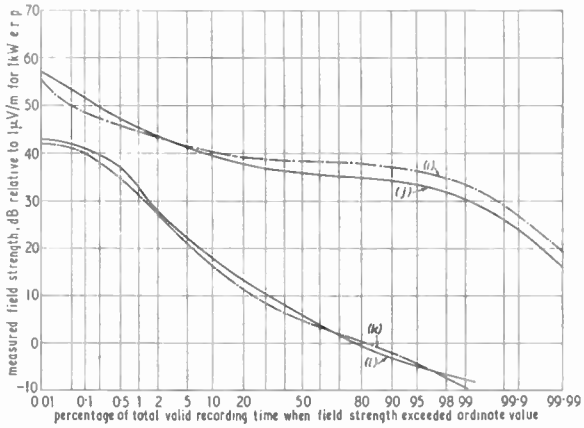
The results of the Caversham and Mursley Bands I and II measurements are plotted in Fig. 2 as field strength exceeded against percentage of the total valid recording time. The curves for each receiving site and frequency band are shown separately and are accompanied by a table giving the total number of hours relating to each curve and the free-space field strength for the different paths. The field strengths for selected time-percentages derived from Fig. 2 are listed in Table 3.

An inspection of Fig. 2 shows that, in general, the slope of the curves increases with distance. The figures also reveal that the curves converge at the low time-percentage values. This implies that for the high amplitude signals, that is, during abnormal conditions, the signal values are less dependent upon distance.

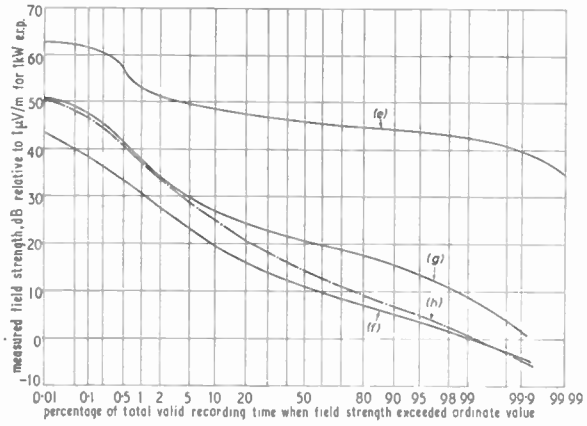
Curves (a), (e), (i), (j) and (m) in these figures relate to the shorter paths where, during normal propagation conditions, the signal is virtually con-



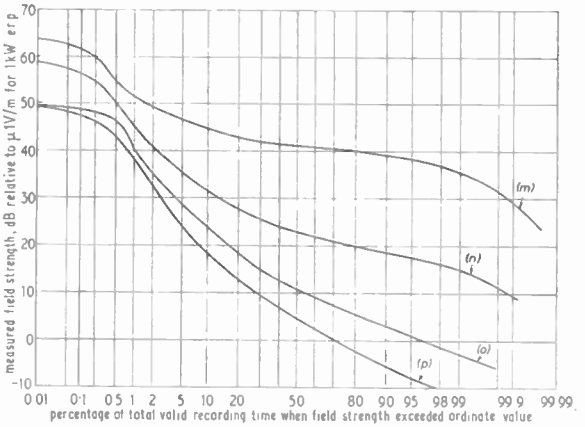
Curve	Transmitting site	Receiving site	Frequency MHz	Distance km	Total hours recorded	Free space field dB (μV/m) for 1 kW e.r.p.
(a)	Crystal Palace	Caversham	41·5	62·0	7072	71·0
(b)	Peterborough	Caversham	63·27	121·5	6898	65·2
(c)	Sutton Coldfield	Caversham	58·25	138·0	7137	64·1
(d)	Wenvoe	Caversham	63·25	161·0	6923	62·7



Curve	Transmitting site	Receiving site	Frequency MHz	Distance km	Total hours recorded	Free space field dB (μV/m) for 1 kW e.r.p.
(i)	Crystal Palace	Mursley	41·5	77·5	5814	69·1
(j)	Sutton Coldfield	Mursley	58·25	101·0	5507	66·8
(k)	Wenvoe	Mursley	63·25	180·0	5508	61·8
(l)	North Hessary Tor	Mursley	48·23	274·0	5661	58·2



Curve	Transmitting site	Receiving site	Frequency MHz	Distance km	Total hours recorded	Free space field dB (μV/m) for 1 kW e.r.p.
(e)	Wrotham	Caversham	89·1	88·5	7106	68·0
(f)	Peterborough	Caversham	90·1	121·5	6287	65·2
(g)	Sutton Coldfield	Caversham	88·3	138·0	7115	64·1
(h)	Wenvoe	Caversham	89·95	161·0	6982	62·7



Curve	Transmitting site	Receiving site	Frequency MHz	Distance km	Total hours recorded	Free space field dB (μV/m) for 1 kW e.r.p.
(m)	Sutton Coldfield	Mursley	88·3	101·0	5912	66·8
(n)	Rowridge	Mursley	88·5	146·0	5870	63·5
(o)	Wenvoe	Mursley	89·95	180·0	5503	61·8
(p)	North Hessary Tor	Mursley	88·1	274·0	5705	58·2

Fig. 2. Variation of field strength with time.

Table 3

Measured field strengths at Caversham and Mursley

Curves in Fig. 2	Transmitting site	Receiving site	Frequency MHz	Distance km	Field strength, dB (μV/m) for 1 kW e.r.p., exceeded for stated percentage of the time						
					0·1%	1%	10%	50%	90%	99%	99·9%
(a)	Crystal Palace	Caversham	41·5	62·0	59·0	55·5	53·0	51·0	49·5	49·0	47·5
(b)	Peterborough	,,	63·27	121·5	37·0	30·0	20·5	13·5	9·0	4·0	0
(c)	Sutton Coldfield	,,	58·25	138·0	40·5	33·0	23·0	16·5	11·5	6·0	−0·5
(d)	Wenvoe	,,	63·25	161·0	42·5	33·5	22·5	13·0	6·0	−1·0	−5·5*
(e)	Wrotham	,,	89·1	88·5	61·5	53·0	48·5	45·5	44·0	42·5	39·5
(f)	Peterborough	,,	90·1	121·5	38·5	30·5	19·5	11·0	5·0	0	−4·0
(g)	Sutton Coldfield	,,	88·3	138·0	47·5	37·5	27·0	20·5	15·5	9·0	1·5
(h)	Wenvoe	,,	89·95	161·0	46·5	37·0	25·0	14·5	7·0	0·5	−4·5
(i)	Crystal Palace	Mursley	41·5	77·5	48·5	44·5	40·0	38·5	37·0	33·5	27·0
(j)	Sutton Coldfield	,,	58·25	101·0	51·5	45·5	39·5	36·0	34·5	30·5	24·0
(k)	Wenvoe	,,	63·25	180·0	40·0	31·5	16·5	5·0	−2·0	−9·0*	N.L.
(l)	North Hessary Tor	,,	48·23	274·0	41·0	33·0	18·0	6·0	−3·0	−7·5	N.L.
(m)	Sutton Coldfield	,,	88·3	101·0	61·5	51·5	44·5	41·0	39·0	35·5	29·5
(n)	Rowridge	,,	88·5	146·0	56·5	45·0	31·5	23·0	18·5	15·0	N.L.
(o)	Wenvoe	,,	89·95	180·0	48·5	40·0	23·5	10·5	3·0	−3·0	N.L.
(p)	North Hessary Tor	,,	88·1	274·0	47·5	38·0	18·0	4·5	−5·5	−12·0*	N.L.

* Extrapolated value. N.L. Noise level.

stant. During abnormal propagation conditions, however, these signals fade slowly about the median. The signals received over the longer transmission paths are subject to varying degrees of slow and fast fading when propagation conditions are normal. High level signals of virtually constant amplitude are, however, also received at the greater distances when abnormal propagation conditions prevail.

3.2. *Range of Fading between Various Time-percentages*

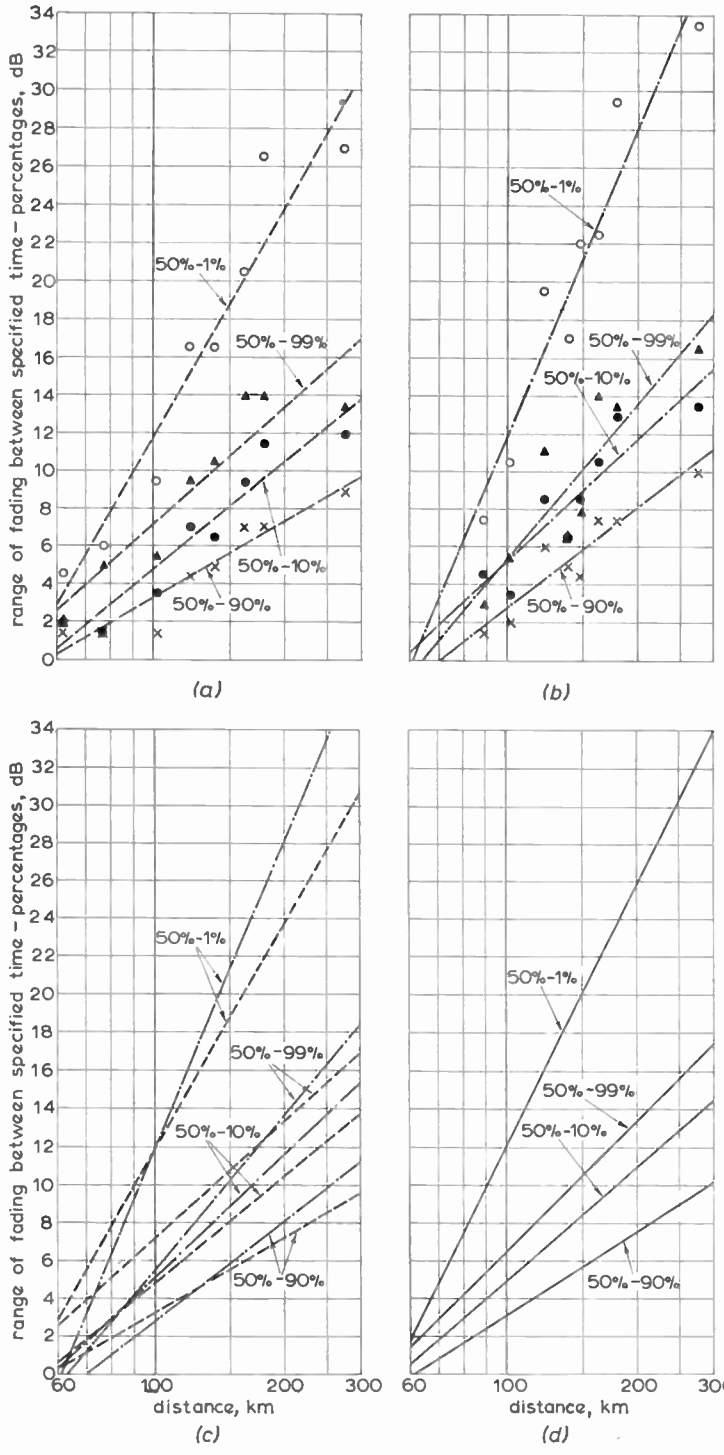
The range of fading is defined as the signal strength exceeded for given percentages of time, expressed as a ratio of the median value. The ranges are given in Table 4 and plotted against distance in Fig. 3(a) and (b) for Bands I and II respectively. With fading ratios expressed in decibels a linear relationship gave a reasonable approximation to the measurements provided distance is plotted to a logarithmic rather than to a linear scale. This relationship must therefore be taken to give the 'best-fit'.

Two aspects of the fading displayed by the curves are of interest. The high field-strength values that occur for less than 10% of the time are important, because in planning broadcast services it is usual to protect a transmission from co-channel interference for at least 90% of the time. From the point of view of reception, and in particular reception for use as a rebroadcast service, it is important to know the incidence of 'fade-outs', that is the ratio of the median to the value occurring for 90% of the time, or for at least 99% of the time.

Figures 3(a) and (b) show that both in Bands I and II the range of fading increases with distance.

It will be noted that the slope of the 50%–1% line is in each case greater than the 50%–99% line, and that the slope of the 50%–10% line is similarly greater than that of the 50%–90% line, indicating that the long-term variation of field strength (expressed in decibels) about the median signal value is asymmetrical; the range of fading relative to the median is greater for the low time-percentages than for the high time-percentage values.

Figure 3(c) reproduces, for comparison purposes, the Bands I and II best-fit lines shown in Figs. 3(a) and (b). It will be seen that at the greater distances Band II signals vary over a wider range than Band I, and although differences exist between the signal characteristics in Bands I and II they are not very great. The combined Bands I and II best-fit lines for the various fading ranges were therefore calculated and appear in Fig. 3(d).



(a) Band I.

(b) Band II.

(c) Comparison of Bands I and II.

(d) Combined Bands I and II.

Fig. 3. Range of fading between various time-percentages.

○ 50%–1% ● 50%–10% × 50%–90% ▲ 50%–99%

— — — — Band I —·—·—·— Band II ——— Bands I and II

Table 4

Fading range between time-percentages

Curves in Fig. 2	Transmitting site	Receiving site	Frequency MHz	Distance km	Range of fading between various time-percentages 50%–1%	50%–10%	50%–90%	50%–99%
(a)	Crystal Palace	Caversham	41·5	62·0	4·5	2·0	1·5	2·0
(b)	Peterborough	,,	63·27	121·5	16·5	7·0	4·5	9·5
(c)	Sutton Coldfield	,,	58·25	138·0	16·5	6·5	5·0	10·5
(d)	Wenvoe	,,	63·25	161·0	20·5	9·5	7·0	14·0
(e)	Wrotham	,,	89·1	88·5	7·5	4·5	1·5	3·0
(f)	Peterborough	,,	90·1	121·5	19·5	8·5	6·0	11·0
(g)	Sutton Coldfield	,,	88·3	138·0	17·0	6·5	5·0	6·5
(h)	Wenvoe	,,	89·95	161·0	22·5	10·5	7·5	14·0
(i)	Crystal Palace	Mursley	41·5	77·5	6·0	1·5	1·5	5·0
(j)	Sutton Coldfield	,,	58·25	101·0	9·5	3·5	1·5	5·5
(k)	Wenvoe	,,	63·25	180·0	26·5	11·5	7·0	14·0
(l)	North Hessary Tor	,,	48·23	274·0	27·0	12·0	9·0	13·5
(m)	Sutton Coldfield	,,	88·3	101·0	10·5	3·5	2·0	5·5
(n)	Rowridge	,,	88·5	146·0	22·0	8·5	4·5	8·0
(o)	Wenvoe	,,	89·95	180·0	29·5	13·0	7·5	13·5
(p)	North Hessary Tor	,,	88·1	274·0	33·5	13·5	10·0	16·5

3.3. *Variation of Monthly Field Strengths for Selected Time-percentages*

The field strengths exceeded in each month for selected time-percentages are plotted in order of distance in Figs. 4 and 5. The 99·9 time-percentages could not be given for some of the longer transmission paths as the corresponding field strengths were below the noise level of the receivers.

The standard deviations of these monthly field strengths were calculated for the different transmission paths and selected time-percentages. Using the standard deviation values, the combined Bands I and II standard deviation best-fit lines for each time-percentage are given in Fig. 6. The standard deviation lines show that the month-to-month field strength variations increase with distance for all time-percentages. In general, the gradient of the line decreases with an increase in time-percentage.

An inspection of Figs. 4 and 5 shows that the 0·1% and 1% monthly field strength values are enhanced, particularly for September and October 1961 and December 1962. These high signals invariably occur during days when the weather is anticyclonic. Such weather may cause an inverse of temperature or lapse of humidity with height in the lower atmosphere and subsiding air then spreads out above a cold and moist layer of air. At the boundary between the dry and moist air a greater-than-normal negative refractive-index gradient occurs, causing increased refraction, reflection or partial reflection of the radio waves. In general, during these abnormal propagation conditions higher-than-average field strengths are received.

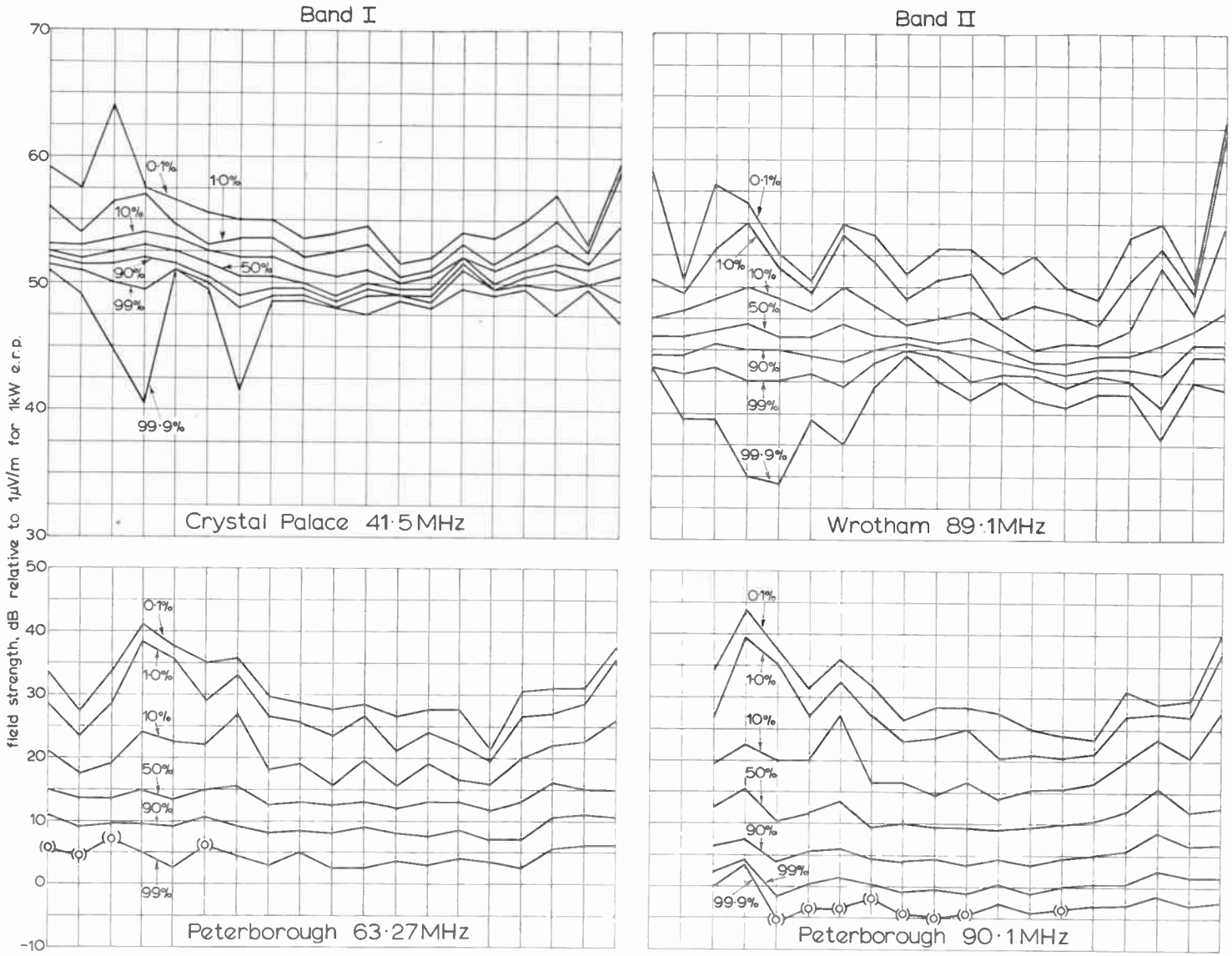
The received signal for the shorter paths is virtually constant during normal (cyclonic weather) propagation conditions. However, during abnormal propagation conditions the signal fades slowly about the median and although the signals are generally enhanced there are occasions when drop-outs occur. This phenomenon is clearly shown in Fig. 5 for the December 1961, Crystal Palace, 99·9% field strength value. These drop-outs are probably caused by two-ray paths giving at times a signal cancellation.

It would be unwise to draw any firm conclusion from Figs. 4 and 5 concerning seasonal variations in propagation as the measurements only cover a period of 16–19 months.

3.4. *Variation of Field Strength with Distance*

3.4.1. Site variation factor

In order to determine whether the two receiving sites chosen for the experiment were representative of the areas in which they were situated, field strength



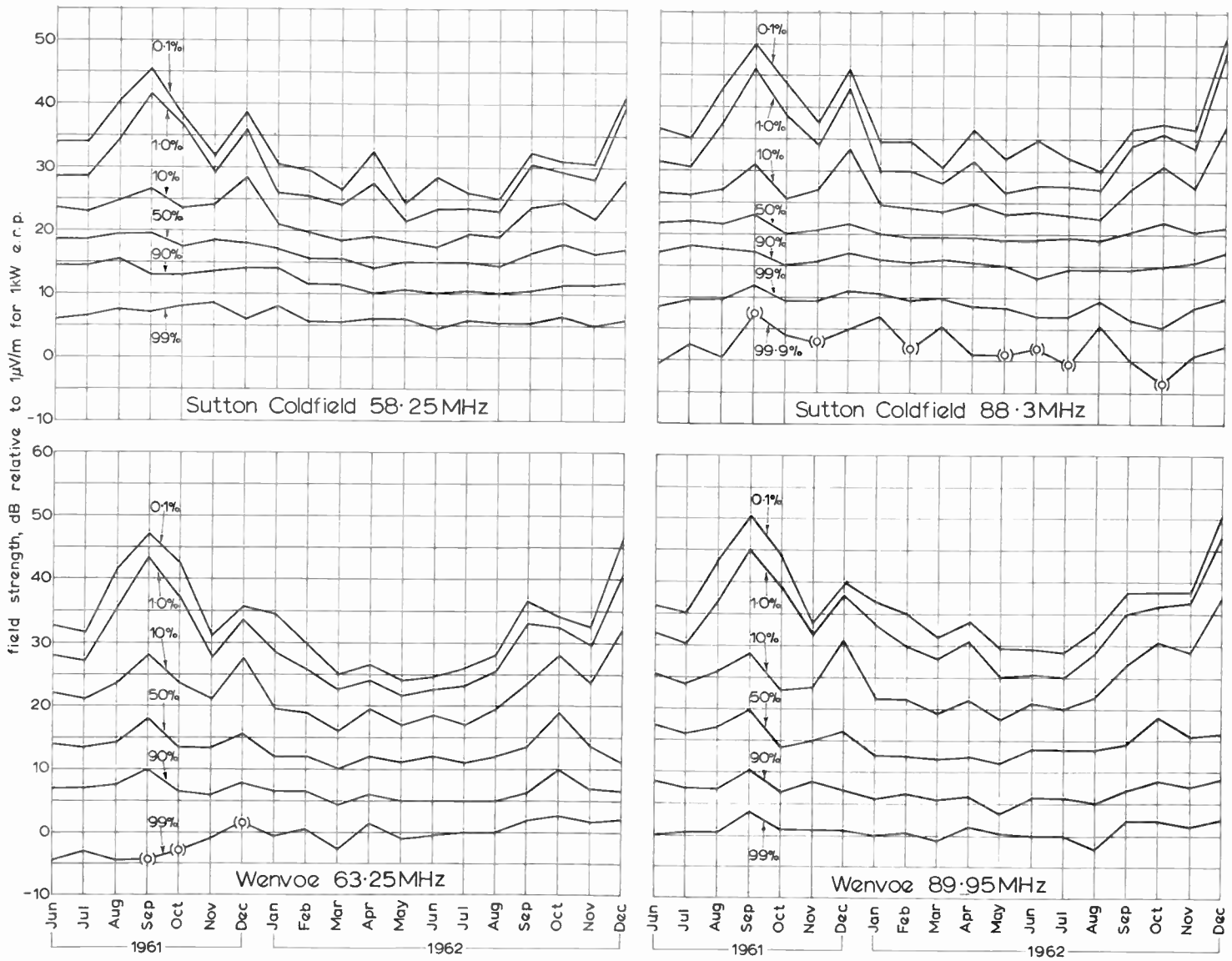
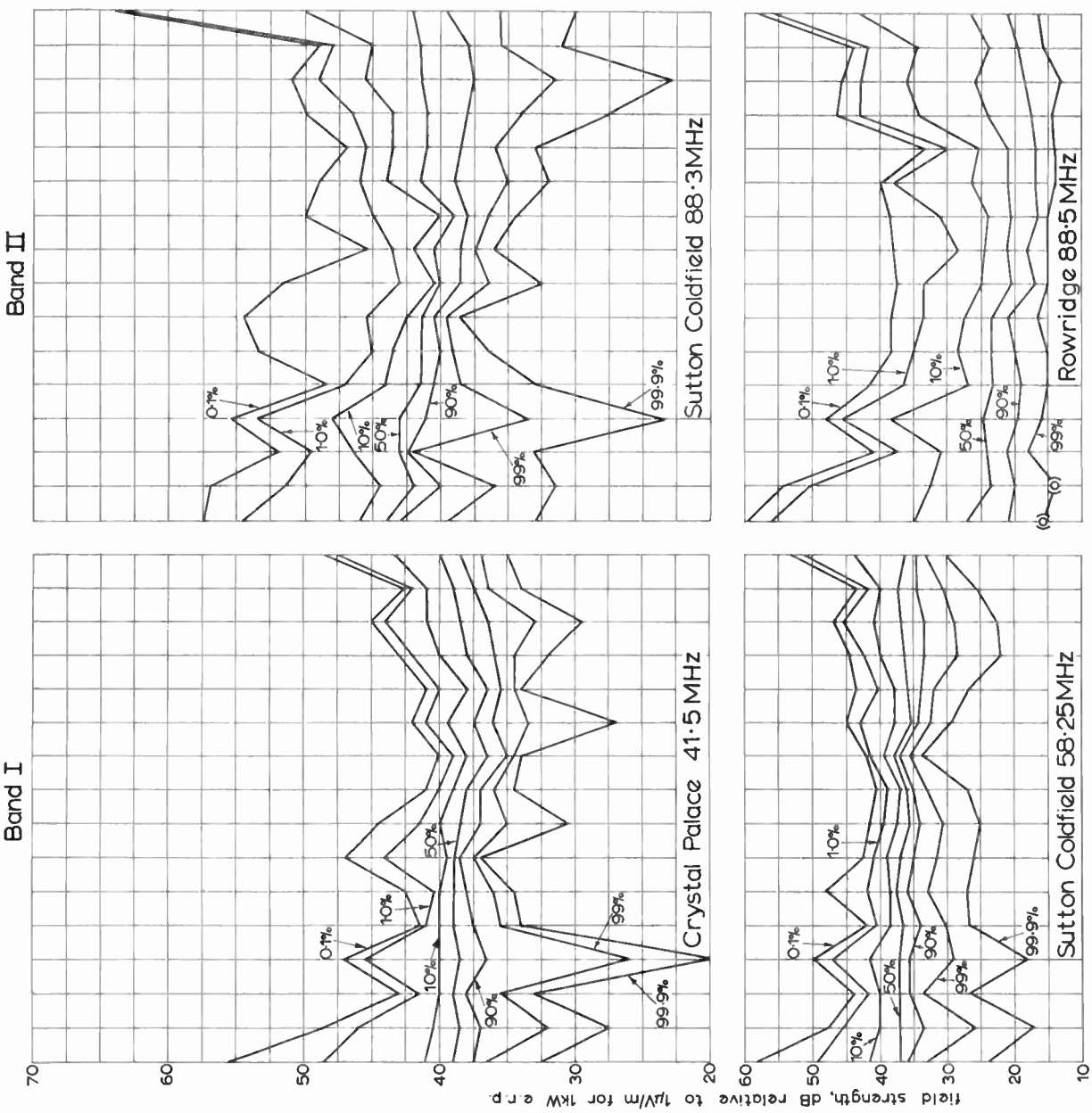


Fig. 4. Field strengths exceeded in each month for selected time-percentages (Caversham). (○) Extrapolated
Crystal Palace 62·0 km; Wrotham 88·5 km; Peterborough 121·5 km; Sutton Coldfield 138·0 km; Wenvoe 161·0 km.


Band II
Band I
Sutton Coldfield 88·3MHz
Rowridge 88·5MHz
Crystal Palace 41·5MHz
Sutton Coldfield 58·25MHz
0·1%
1·0%
10%
50%
90%
99%
99·9%
field strength, dB relative to 1μV/m for 1kW e.r.p.
70
60
50
40
30
20
10

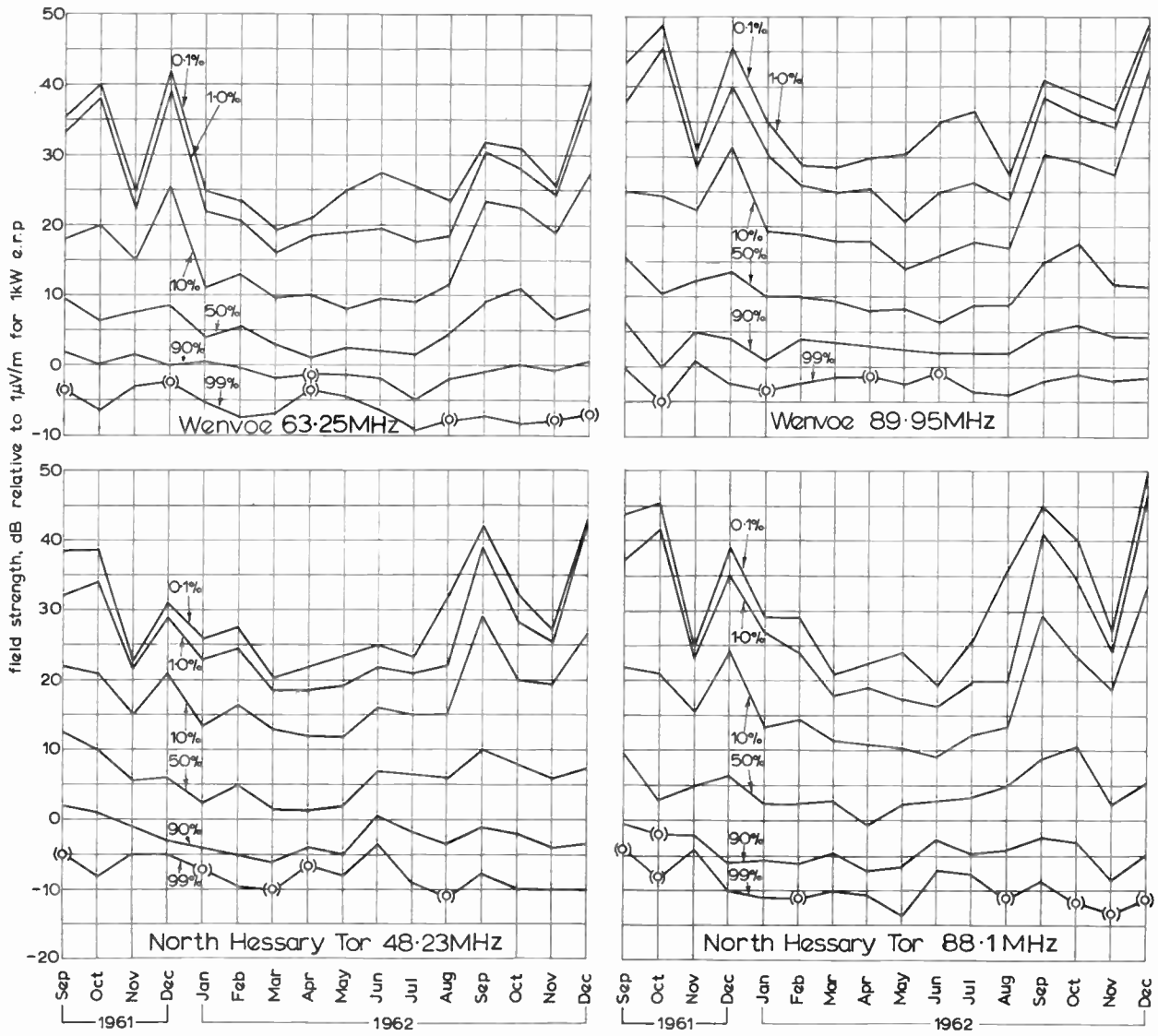


Fig. 5. Field strengths exceeded in each month for selected time percentages (Mursley). (○) Extrapolated

Crystal Palace 77·5 km; Sutton Coldfield 101·0 km; Rowridge 146·0 km; Wenvoe 180·0 km; North Hessary Tor 274·0 km.

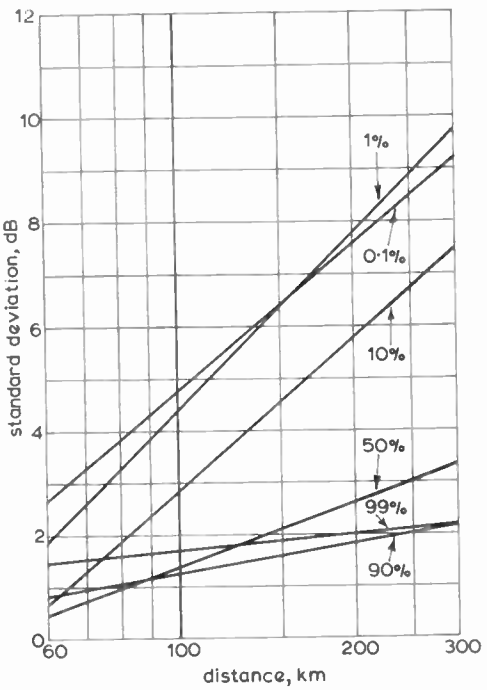


Fig. 6. Bands I and II—Standard deviation of field strengths exceeded in each month for selected time-percentages.

Table 5

Site variation factors

Transmitting site	Receiving site	Frequency MHz	Site variation factor dB
Crystal Palace	Caversham	41·5	−12·0
Peterborough	,,	63·27	+3·5
Sutton Coldfield	,,	58·25	− 5·0
Wenvoe	,,	63·25	−15·0
Wrotham	,,	89·1	− 4·5
Peterborough	,,	90·1	− 2·5
Sutton Coldfield	,,	88·3	− 8·0
Wenvoe	,,	89·95	−10·5
Crystal Palace	Mursley	41·5	− 7·5
Sutton Coldfield	,,	58·25	− 5·0
Wenvoe	,,	63·25	+ 4·0
North Hessary Tor	,,	48·23	− 6·0
Sutton Coldfield	,,	88·3	−10·0
Rowridge	,,	88·5	−10·5
Wenvoe	,,	89·95	− 0·5
North Hessary Tor	,,	88·1	− 5·0

Table 6

Corrections for a transmitting aerial height above mean terrain of 300 metres

Transmitting site	Receiving site	Frequency MHz	Distance km	Aerial height above mean terrain m	Corrections to normalize the measured field strengths for an aerial height of 300 metres above mean terrain dB 1%	10%	50%
Crystal Palace	Caversham	41·5	62·0	160	+4·5	+6·0	+7·0
Peterborough	,,	63·27	121·5	183	+1·5	+2·0	+3·0
Sutton Coldfield	,,	58·25	138·0	325	−0·5	−0·5	−0·5
Wenvoe	,,	63·25	161·0	234	+1·0	+1·0	+1·0
Wrotham	,,	89·1	88·5	250	+1·0	+1·0	+1·5
Peterborough	,,	90·1	121·5	155	+2·5	+4·0	+4·0
Sutton Coldfield	,,	88·3	138·0	298	0	0	0
Wenvoe	,,	89·95	161·0	207	+1·0	+1·5	+2·5
Crystal Palace	Mursley	41·5	77·5	150	+3·5	+5·5	+6·0
Sutton Coldfield	,,	58·25	101·0	315	−0·5	−0·5	−0·5
Wenvoe	,,	63·25	180·0	235	+0·5	+0·5	+0·5
North Hessary Tor	,,	48·23	274·0	583	−3·0	−3·5	−4·0
Sutton Coldfield	,,	88·3	101·0	287	+0·5	+0·5	0
Rowridge	,,	88·5	146·0	99	+3·5	+5·5	+5·5
Wenvoe	,,	89·95	180·0	208	+1·5	+2·0	+1·5
North Hessary Tor	,,	88·1	274·0	554	−2·0	−3·5	−3·5

measurements were made at various locations in their vicinity. Measurements of approximately 30 minutes duration were carried out at temporary sites within a radius of 8 km from each permanent site. The ratio of the median field strength at the temporary sites to that for the same period at the permanent site was calculated. The average of these ratios is known as the site variation factor (s.v.f.), and was measured for each transmission frequency and each of the two permanent receiving sites. The appropriate s.v.f. was then used as a correction to the measured field strengths to give the fields that would have been measured at 50% of locations in the vicinity of each permanent site.

The results of the Caversham and Mursley s.v.f. measurements are listed in Table 5. These show that with the exceptions of the Band I Peterborough–Caversham and Wenvoe–Mursley transmission paths, the s.v.f.s have negative values, indicating that the Caversham and Mursley sites receive higher fields than the average in their area. Table 5 also reveals that at each receiving site the s.v.f.s vary according to the direction of reception, as would be expected. In addition, for the same transmission path, the s.v.f.s vary with the frequency. The transmission paths involved in this comparison are not identical, as the Bands I and II transmitting aerials are mounted at different heights on the mast and separate receiving aerials are used.

3.4.2. Transmitting aerial height above mean terrain

Because there were differences between the heights of the different transmitting sites above the surrounding terrain and the heights of the different transmitting aerials above ground level, it seemed desirable to apply, beside the s.v.f. correction, a correction for the differences in the transmitting aerial heights. This was done for comparison with the C.C.I.R. Recommendation 370 (Geneva 1963), in which field-strength/distance curves relating to overland paths are used in the planning of broadcast services. Separate curves are drawn for different transmitter aerial heights above mean terrain for the v.h.f. and u.h.f. frequency bands, mean terrain being somewhat arbitrarily defined as the height of the aerial above the average level of the ground between the distances of 3 km and 15 km from the transmitter.

Table 6 lists the aerial height above mean terrain for each transmission path and also shows the correction derived from the curves in Recommendation 370, which normalizes the field strength for other transmitting heights to a height of 300 m. Recommendation 370 gives the field-strength/distance curves for the 1, 10 and 50 time-percentages and thus corrections for these time-percentages only are given in Table 6. The 1% corrections have been used for time-percentages less than 1% and similarly the 50% corrections used for time-percentages greater than 50%. Though not strictly applicable, they help to reduce the differences in field strength due to differences in transmitting aerial height for time-percentage curves for which no values are available in Recommendation 370. These corrections have been applied to the measured field strengths listed in Table 3 and give, together with the s.v.f.s, the corrected values in Table 7.

3.4.3. Field-strength/distance curves

The field strengths (corrected for transmitting aerial height and s.v.f.) listed in Table 7 are used to derive, by the method of least squares, the field-strength/distance curves for selected time-percentages; the results are shown in Fig. 7. The relationship between field-strength plotted in decibels and distance plotted to a logarithmic scale are drawn as straight lines, for the reason given in Section 3.2. This implies that the field E varies with distance d,

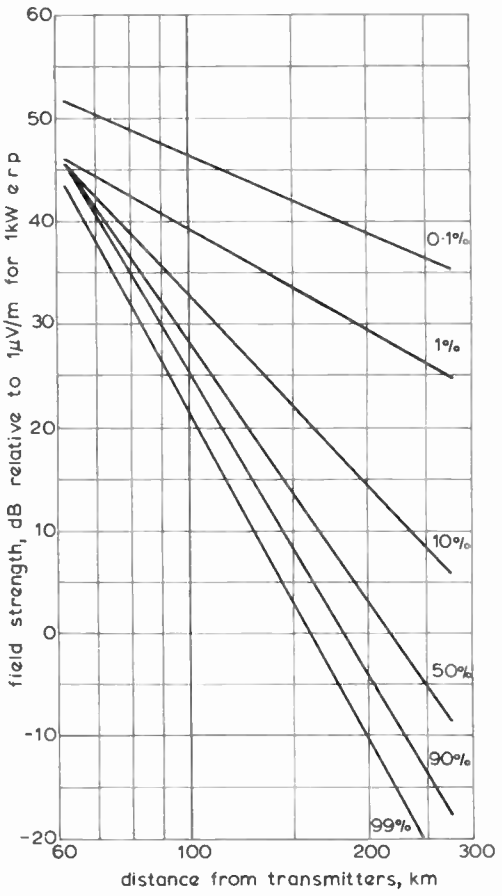


Fig. 7. Variation of Bands I and II field strengths as a function of distance. The curves show the field strength exceeded for different time-percentages.

Table 7

Field strength corrected for s.v.f. and transmitter aerial height above mean terrain of 300 metres

Transmitting site	Receiving site	Frequency MHz	Distance km	Field strength, dB (μV/m) for 1 kW e.r.p. (corrected for s.v.f. and mean terrain) exceeded for stated percentage of the time 0·1%	1%	10%	50%	90%	99%	99·9%
Crystal Palace	Caversham	41·5	62·0	51·5	48·0	47·0	46·0	44·5	44·0	42·5
Peterborough	,,	63·27	121·5	42·0	35·0	26·0	20·0	15·5	10·5	6·5
Sutton Coldfield	,,	58·25	138·0	35·0	27·5	17·5	11·0	6·0	0·5	−6·0
Wenvoe	,,	63·25	161·0	28·5	19·5	8·5	−1·0	−8·0	−15·0	−19·5
Wrotham	,,	89·1	88·5	58·0	49·5	45·0	42·5	41·0	39·5	36·5
Peterborough	,,	90·1	121·5	38·5	30·5	21·0	12·5	6·5	1·5	−2·5
Sutton Coldfield	,,	88·3	138·0	39·5	29·5	19·0	12·5	7·5	1·0	−6·5
Wenvoe	,,	89·95	161·0	37·0	27·5	16·0	6·5	−1·0	−7·5	−12·5
Crystal Palace	Mursley	41·5	77·5	44·5	40·5	38·0	37·0	35·5	32·0	25·5
Sutton Coldfield	,,	58·25	101·0	46·0	40·0	34·0	30·5	29·0	25·0	18·5
Wenvoe	,,	63·25	180·0	44·5	36·0	21·0	9·5	2·5	−4·5	—
North Hessary Tor	,,	48·23	274·0	32·0	24·0	8·5	−4·0	−13·0	−17·5	—
Sutton Coldfield	,,	88·3	101·0	52·0	42·0	35·0	31·0	29·0	25·5	19·5
Rowridge	,,	88·5	146·0	49·5	38·0	26·5	18·0	13·5	10·0	—
Wenvoe	,,	89·95	180·0	49·5	41·0	25·0	11·5	4·0	−2·0	—
North Hessary Tor	,,	88·1	274·0	40·5	31·0	9·5	−4·0	−14·0	−20·5	—

according to the law $E = kd^m$, where k is a parameter related to the transmission path and m is the slope of the best fit line. The values of m and $20 \log k$ are given in Table 8.

The field-strength/distance curves in Fig. 7 show that the slope of the curves increases with the increasing time-percentage and indicates a reduced dependence of field strength on distance for small time-percentages.

The 1, 10 and 50 time-percentage curves from Fig. 7 are re-drawn in Fig. 8, together with the appropriate C.C.I.R. field-strength/distance curves.[3] The B.B.C. Bands I and II measurements cover the frequency range 41·5 to 90·1 MHz, whereas the Bands I to III C.C.I.R. curves are for the frequency range 40 to 250 MHz. The B.B.C., however, have previously carried out Band III overland measurements utilizing a frequency of 180·4 MHz and these field-strength/distance curves are also shown in Fig. 8. The Band III measurements, which lasted for a period of almost $3\frac{1}{2}$ years, are corrected for s.v.f. and aerial height of approximately 300 m above mean terrain.

An inspection of Fig. 8 reveals that there is good agreement between the B.B.C. Bands I and II curves and the earlier Band III curves. In general, the Band III curves are higher than the Bands I and II curves, but only by a few decibels.

Table 8

Field strength/distance parameters

Time-percentage	m	$20 \log k$
0·1	−1·252	96·3
1	−1·608	103·4
10	−3·047	154·6
50	−4·165	194·7
90	−4·916	221·7
99	−5·312	233·8

The B.B.C. 1% curves indicate a higher received field than the C.C.I.R. 1% curve, the difference increasing to about 8 dB at 274 km. The B.B.C. and C.C.I.R. 10% curves are in good agreement. The same applies for the 50% curves up to about 200 km. Beyond 200 km the B.B.C. 50% curves indicate a lower field than the C.C.I.R. 50% curve by approximately 2·5 to 5 dB, at least up to 274 km.

4. Conclusions

The range of fading between the 50 and 1, 50 and 10, 50 and 90, and 50 and 99 time-percentage field strengths increases with distance. The range of fading

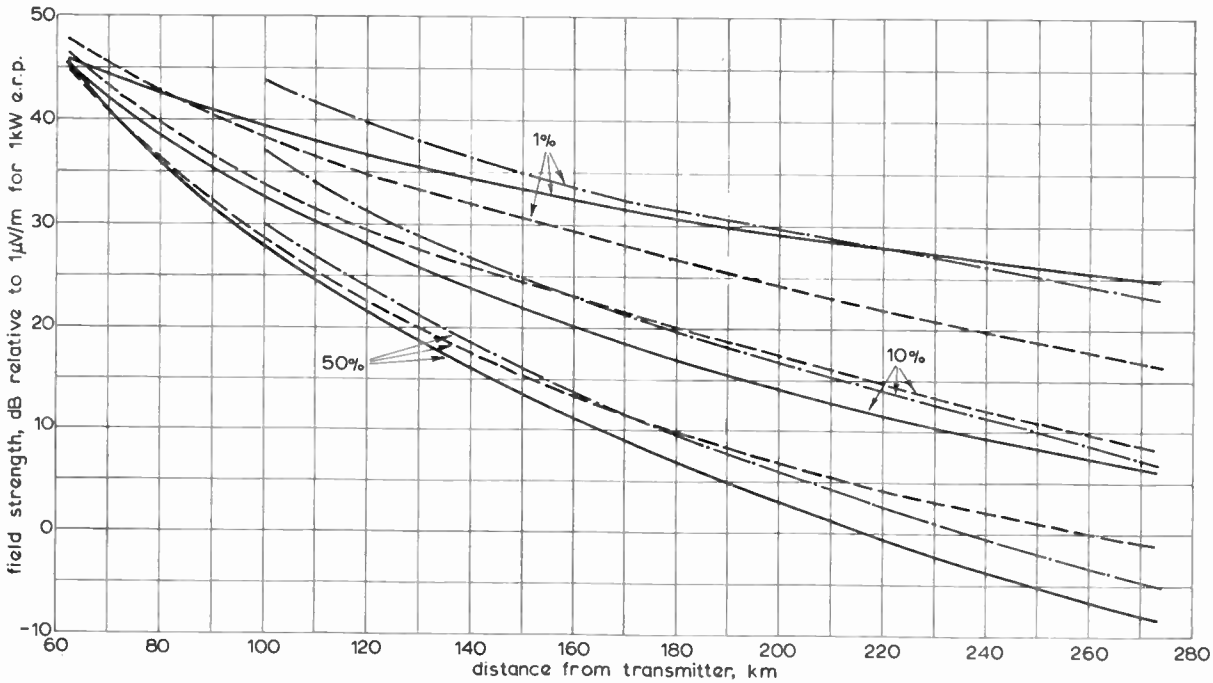


Fig. 8. Comparison of B.B.C. and C.C.I.R. field-strength/distance curves.

——— Bands I and II (B.B.C.) —·—·— Band III (B.B.C.) — — — Bands I to III (C.C.I.R.)

relative to the median field strength is greater for the low time-percentage field strengths as compared with the high time-percentage values.

The variation of monthly field strengths for the selected time-percentages increases with distance; this is, however, less pronounced for the higher time-percentage values.

The B.B.C. Bands I and II and the Band III field-strength/distance curves are similar. The 10% and 50% B.B.C. curves are in reasonable agreement with the equivalent C.C.I.R. curves, but the B.B.C. 1% curves indicate higher fields than the C.C.I.R. 1% curve by about 8 dB at 274 km.

5. Acknowledgments

The B.B.C. acknowledges with grateful thanks the site facilities given at Mursley by the Buckinghamshire County Constabulary.

The author is grateful for the assistance given in this work by the Engineer-in-Charge and his staff at the B.B.C. Monitoring Station, Caversham and by his many colleagues of the B.B.C. Research Department.

Finally the author wishes to express his thanks to the Director of Engineering of the British Broadcasting Corporation for permission to publish this paper.

6. References

1. S. A. W. Jolliffe *et al.*, 'The character of the received i.l.s. signal and its relation to monitoring', *The Radio and Electronic Engineer*, **32**, No. 5, pp. 293–311, November 1966.
2. D. G. Beadle and D. E. Susans, 'Digital coding equipment for recording field strength measurements', *Electronic Engng*, **39**, No. 470, pp. 233–9, April 1967.
3. Documents of the C.C.I.R. Xth Plenary Assembly, Geneva 1963, Vol. II, p. 24.

Manuscript first received by the Institution on 12th June 1967 and in final form on 4th September 1967. (Paper No. 1155.)

Some Papers Published in Recent Issues of the *Proceedings of the Indian Division* of the Institution

F.M. Noise in Reflex Klystrons. B. V. RAO. (*Indian Institute of Technology, Bombay.*)

From a theory developed by Middleton, of phenomenological models for a microwave oscillator perturbed by noise, a strictly theoretical value of the coupling coefficient D_0 for f.m. noise has been obtained. The f.m. noise power spectrum for a typical reflex klystron has then been determined and the slope of the spectrum found to agree quite well with the value obtained from noise measurements.

Proc. Indian Div. I.E.R.E., 5, No. 1, pp. 4–8, January–March 1967.

Direction of Maximum Radiation from Non-resonant End-fed Aerials. V. L. TALEKAR. (*Malaviya Regional Engineering College, Jaipur.*)

In an earlier work by the author the approximation involved in Bruce's formula for direction of maximum radiation from the end-fed aerials of finite lengths was pointed out. Using graphical method for solution, an asymptotic value of the constant involved in the expression for the tilt angle was obtained. The present paper shows that this constant is not independent of the length of aerial and has got values ranging from 0·205 for quarter wave length to 0·372 for sixteen wave lengths long aerials. From these considerations it is observed that the degree of approximation involved in the value of tilt angle as per Bruce's formula is considerable and for the optimized six wave lengths long aerial the error is 3·4 degrees.

Proc. Indian Div. I.E.R.E., 5, No. 1, pp. 9–11, January–March 1967.

Carrier Suppression Filters for Microwave Noise Measurement. B. V. RAO. (*Indian Institute of Technology, Bombay.*)

In the study of sideband noise of microwave devices, it is sometimes necessary to employ carrier suppression filters. The suppression characteristics of two separate kinds of such filters for frequencies in the sidebands of a carrier are discussed.

The minimum insertion loss obtainable with the magic-T filter is found to be not less than 6 dB. The loop filter has lower insertion loss. However, the magic-T filter has the advantage of simpler construction and is more compact.

Proc. Indian Div. I.E.R.E., 5, No. 2, pp. 42–47, April–June 1967.

Waveguide Twists and Bends. A. MUKHERJEE, *et. al.* (*Defence Electronics Research Labratory, Hyderabad.*)

Waveguide twists and bends have been fabricated at the Defence Electronics Research Laboratory in Hyderabad by adopting different design and fabrication techniques. The advantages and limitations of these methods are discussed and the performance figures of the developed components are graphically represented.

The merits and limitations of the different types have been discussed in detail. From the collected data on the performance of the twists and bends designed and fabricated by different methods, the authors conclude that, subject to some limitations, it is possible to design and fabricate waveguide twists and bends for X and S band operation with any degree of compactness and excellent performance over any desired range of the spectrum in these bands can be expected.

Proc. Indian Div. I.E.R.E., 5, No. 2, pp. 37–41, April–June 1967.

Some Applications of Radio Characteristics in a Tropical Standard Atmosphere. H. N. SRIVASTAVA. (*Meteorological Office, New Delhi.*)

The profiles of M, the modified radio refractive index, in a standard atmosphere for tropics, have been given for 20%, 40%, 60% and 80% relative humidity values from mean sea level to 2500 metres. They were utilized to verify the propagation conditions associated with tropical cyclones and inversions.

It has been concluded that the M profiles in the standard tropical atmosphere may be conveniently used for propagation work associated with any synoptic weather situation in India.

Proc. Indian Div. I.E.R.E., 5, No. 3, pp. 73–76, July–September 1967.

A High Frequency Electronic Wattmeter. S. MADHU SUDHANA RAO. (*Department of Electrical Engineering, Indian Institute of Technology, Bombay.*)

A electronic wattmeter for measurements in the frequency range 20 kHz to 1 MHz is described, which employs a modified form of the bootstrap ohmic multiplier. The original multiplier circuit necessitated the use of isolated power supplies, and these have been derived from a grounded power supply, thereby making the scheme more practicable. It is hoped that the wattmeter will be of use for power measurements in radio frequency heating.

Proc. Indian Div. I.E.R.E., 5, No. 3, pp. 86–92, July–September 1967.

Transistorized Tuned Amplifiers. H. SINGH and D. SINGH. (*Central Electronics Engineering Research Institute, Pilani, Rajasthan.*)

Designs of transistorized tuned amplifiers for absolutely stable as well as potentially unstable regions of frequencies are described. The limitations on the gain imposed by the requirements of stability, bandwidth and selectivity for tuned amplifiers are mentioned and a design example of an r.f. tuned single stage amplifier having continuously variable tuning frequency is given.

Proc. Indian Div. I.E.R.E., 5, No. 3, pp. 77–85, July-September 1967

U.D.C. 621-52: 681.32

The Application of Automation to Assembly and Testing in Computer Manufacture

By

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Reprinted from the Proceedings of the Joint I.E.R.E.–I.Prod.E.–I.E.E. Conference on 'The Integration of Design and Production in the Electronics Industry' held at the University of Nottingham on 10th to 13th July 1967.

Summary: The layout and construction of a typical second-generation digital computer is outlined, and an account given of the manual methods of assembly and testing in use until comparatively recently. The feasibility of introducing automation techniques is discussed, and an analysis made of those areas of production and testing most amenable to such treatment. Three applications are described, demonstrating the direct application of automation to the processes of wiring, logic-card testing and final commissioning, emphasizing the dramatic reduction in manufacturing time-scale made possible by the resulting increases in production efficiency and machine reliability.

1. Introduction

This paper is given against the background of a company producing a wide range of automation equipment, and in particular specializing in the production of digital computers for applications ranging from large-scale commercial data-processing installations to microminiature airborne flight-control systems.

The production of the modern digital computer poses many problems, both administrative and technical. Nearly all of these have as their common root the immense scale of the project, probably one of the largest for equipment in quantity production. The sheer number of its constituent components makes it inevitable that even a minimal defect rate in the basic components or error rate in the assembly processes will result in a large number of faults in the completed assembly, any one of which may absolutely inhibit operation of the machine.

Design and production engineers have not been slow to realize the potentialities of the computer as a design aid, and much work in this field has already proved fruitful. It is now commonplace for production documentation, work-flow, component-ordering and marshalling, costing and suchlike tasks to be under direct computer-control, and in the technical design stage much of the tedium of circuit design and tolerancing, optimization of wiring routes, preparation of component assembly drawings and checking of circuit loadings is now relieved by presenting these jobs to the computer for routine processing.

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The economies of time and effort that these schemes realize are only too obvious, and automated design and documentation of computer projects is becoming increasingly advanced as the techniques are further developed. Less happy perhaps is the state of the true production process, that is to say the mechanical assembly of the computer and subsequent electrical testing and fault correction. Hitherto this has been almost entirely a manual process, from the basic assembly of discrete components on to printed circuit cards through to the final program testing of the completed machine.

As with all processes involving a large number of human operations the introduction of errors is inevitable, and these can only be minimized by rigid standards of inspection at every stage of sub-assembly. Manual labour and inspection are two of the most costly and inefficient items of production; the productivity of an inspector is zero, and indeed his very presence on the production floor could in some ways be regarded as an admission of some measure of defeat.

In recent years the philosophy adopted has been to assemble the computer by hand, with simple visual and electrical inspection at all stages, and then to clear all remaining faults in an intensive test period known as the 'commissioning' stage, loosely defined as the time between switch-on of the computer's power system and the ability to run test programs.

Once the machine has reached program-running capability the problems are well-nigh solved, for the more subtle faults, such as those causing data errors as opposed to loss of program control, are readily detected and located by running suitable diagnostic routines.

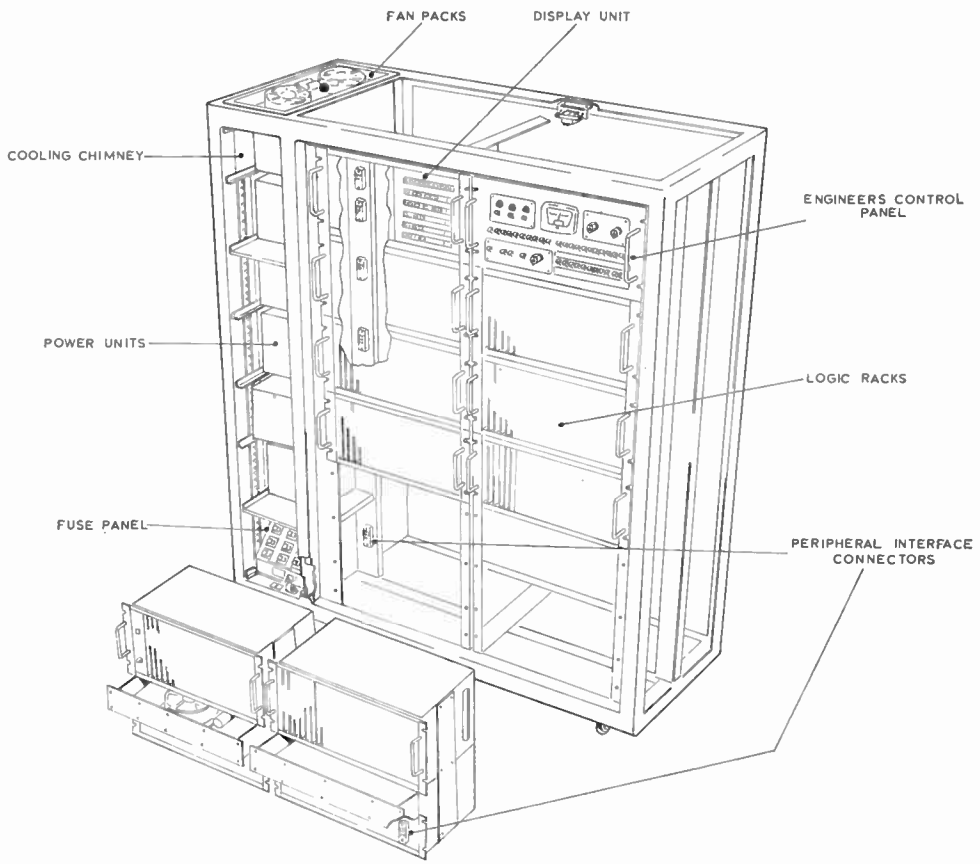

Fig. 1. Typical layout of a central processor.

The improvements which could be made in the production process are now self-evident: reduction of the amount of manual labour, manual inspection and manual testing. The application of automation techniques to these three aims forms the subject of this paper. The computer manufacturer is of course ideally placed to attack these problems, since he has at his disposal not only the tools for the job, but also the essential skills of engineering and programming required for its implementation.

2. The Layout and Construction of a Computer

Before attempting to discuss in detail the techniques for improving the various stages of manufacture it is first necessary to devote a little thought to the general layout and construction of the machine, and to provide a background against which the problems can best be seen.

A computer consists of two main units, the central processor and the store. The store is the machine's memory unit, in which is filed the list of coded instructions comprising the program to be executed, together with the data to be computed. The central processor extracts from the store the instructions to be obeyed singly, and in the sequence specified by the program itself. Each instruction is first extracted and then obeyed. Thus it is the central processor which is in fact the computational unit.

2.1 *The Central Processor*

The central processor is essentially a large array of logic elements, i.e. circuits performing the basic mathematical AND and OR functions, so inter-connected as to form a complex logical system capable of extracting a coded instruction from the store, decoding it and obeying it, which latter may consist of selecting the contents of a specified register, performing an arithmetic operation on it and returning it to the same or different register.

Since the central processor is purely a complex of logic elements it could of course be built on one giant-size printed-circuit card, covering several square feet. Clearly this is neither practical nor desirable. From the purely technical consideration of the speed of operation of the logic elements all inter-connections have to be kept as short as possible, and from the production and maintenance standpoints it is essential to split the logic complex into more easily handled modules.

In practice it is usual to reduce the size of the logic module to a printed-circuit card holding some twenty to thirty logic elements, and a medium-power central processor would contain perhaps two to five hundred of these cards. Some cards would be unique, as for instance in the register control logic; others may occur several times in the machine where, for example, each forms one 'bit' of a register system.

Wherever possible the logical inter-connections between the elements are made with wire links or printed-tracking on the cards themselves, but obviously the logic cards must in addition be wired to one or more of their neighbours to complete the logic network. Thus on one edge of each card the printed circuit is tracked so as to mate up with a conventional printed-circuit edge-connector.

The edge-connectors are contained within the main framework of the computer, the logic inter-connections between them being called the 'backwiring'.

The network of backwiring and the set of logic cards form the bulk of the central processor, other items having no part to play in the functional operation of the system except insomuch as to provide ancillary requirements such as power-supply, cooling, visual display of register contents, manual control facilities etc. A typical constructional layout is shown in Fig. 1.

The main framework usually houses several 'logic racks', i.e. modules containing a row of printed-circuit edge-connectors, each with its associated guide-runner for location of the printed-circuit card. These logic racks are individually wired during manufacture, then assembled into larger modules of several such racks, which are then inter-connected. Dependent on the final size of the system this process is repeated until the complete backwiring system is constructed.

2.2 *The Store*

The construction of the store, usually a ferrite-core device, follows the same lines as the central processor. There are some differences, notably in that the printed circuit cards may carry analogue circuits, e.g. read/write amplifiers, in addition to digital logic circuits as used in the processor. Additionally, the ferrite-core stack presents an extra module for connection to the backwiring. The general layout and constructional technique, however, is similar to that described for the central processor.

2.3 *Ancillary Equipment*

In addition to the logic circuitry and backwiring the computer will contain ancillary equipment essential for its operation, such as power supply units and fan-packs, together with optional features such as control panels, display units and other monitor or control facilities appropriate to the size and intended application of the machine.

Power is normally distributed along bus lines routed throughout the backwiring in the same way as the logic inter-connections, each logic rack being connected at its ends to the main power feeders. The power supply units are usually housed in a totally-enclosed section of the equipment cabinet, through which filtered cooling air is blown, the cooling ducts serving the important secondary function of screening the power units and their associated mains supply cables from the logic system.

The remaining ancillaries, of which fan-packs, control panels and display units provide the most frequent examples, are wherever possible designed as plug-in modules, this simplifying both the production and servicing of the computer.

3. Non-automatic Assembly and Testing

By far the greater proportion of the computers in current production is of the type intended for incorporation in commercial data-processing installations, these computers falling into the medium to large classification, both in terms of computing power and speed, and also the physical size of the equipment. The miniature and microminiature machines finding applications in military and airborne environments are of highly specialized construction, discussion of which falls outside the scope of this paper.

It is worthwhile at this stage to include a brief description of the non-automated system of assembly and testing in force until comparatively recently, for this provides an essential background to appreciating the automation techniques, especially insomuch as these were themselves devised following a careful study of the then current production methods, the application of automation being directed firstly to those areas most lacking in efficiency and most amenable to treatment.

3.1 *Basic Assembly*

The computer starts life as a metal skeleton on the production floor, consisting at this stage only of the painted metal equipment frame. Initial assembly, the addition of all the mechanical 'hardware', results in an assembly complete with power unit shelves, power distribution busbars, logic rack mounting brackets and all the smaller metal fitments necessary for the location of the larger modules.

The next phase, following inspection of the completed mechanical assembly, is to install the power distribution system, usually in the form of a pre-assembled cable harness, and to bolt into place all ancillary modules, including the control panel, fan-packs, fuse panels, and display unit. Each of these plug-in modules will have been separately assembled and inspected at an earlier stage, the production work-flow scheme being prepared by computer to ensure

that the correct modules arrive at the assembly area in the sequence required, and at the right time.

The computer now lacks only the backwiring system, logic cards and power units before assembly is complete.

3.2 *The Backwiring System*

For the medium-sized computer which will serve as an example for the purposes of this paper the backwiring system incorporates ten logic racks each housing a row of twenty-six edge-connectors. The ten racks are arranged in two vertically mounted columns each five racks high.

The edge-connectors, mounted vertically, have a double row or 32 wire-wrap terminals (pins) catering for a double-sided printed-circuit card with a total of 64 contacts. Thus every logic frame presents a matrix of pins for backwiring, and in this instance these are disposed on an X-Y grid of 32 pins high by 52 pins long.

The logic racks are assembled and wired individually, each being fitted with its complement of 26 edge-connectors and card guides. The wiring is performed according to a printed wiring schedule, i.e. a list of wire links, this being the output of a special computer program. Data for this program are in a master file of information containing, amongst other items, a list of all points in the logic system to be interconnected. The program performs a first-level sort on this list, selecting the shortest possible path for wiring each group of pins to be connected, restricted only by the rule of not more than three wire-wraps per pin. A second-level sort is then made, in which the links are split into two classes, i.e. those between two points on the same rack and those between two points on different racks. Finally the program outputs the wiring schedules on a printer, and also on punched paper tape for further copies to be made off-line, one schedule for each rack to be wired and one schedule for each of the inter-rack combinations.

Reading the source pin from the printed schedule, the operator strips the correct length of insulation from the free end of a reel of wire and loads the bared end into his wire-wrap 'gun', selects the source pin and pushes the gun over the pin. Depressing the trigger of the gun energizes the wrapping head, which is either electrically or pneumatically powered, and the wire-wrap joint is made. After reading the destination pin from the schedule the operator completes the link by measuring, cutting and stripping the wire before forming the second wrap joint. This procedure is followed until the wiring for that rack is completed, a time of three minutes per wire link being typical.

As each rack is completed the wiring is checked by an inspector using a battery operated tester giving an audible indication of continuity, working from the same wiring schedules as the gun operator, but testing from the 'blind' side of the back-wiring, that is to say from the printed-circuit card side of the edge-connectors.

When all ten racks are completed the two sets of five are bolted together, and the two sub-assemblies so formed are inter-wired in the same manner. After inspection the two sub-assemblies are located in the computer frame, the backwiring system being completed by adding the links between the two sub-assemblies, and inspecting.

Following completion of the backwiring the machine is delivered to the commissioning area where the logic cards and power units are installed, prior to switch-on.

3.3 *The Logic Cards*

There will be some two hundred printed-circuit cards in the central processor described, each of which is assembled by hand. Starting from a fibreglass blank, which is first etched, plated and roller-tinned, the printed circuit card is drilled and component layout information silk-screened on to it prior to assembly. Each of these preliminary operations is followed by inspection, following which the card is ready for component assembly.

Working from assembly drawings specifying position, part number and (where appropriate) polarity of the components, the operators mount each item on the card. All components will have previously been prepared for use, their leads being solder-dipped, cropped to length and pre-formed so as to locate precisely into the drilled printed-circuit card. The operator has only to secure each item temporarily by folding the leads over on the underside of the card.

When all components have been mounted the card is visually inspected before wiring. The inspection process is aided by a visual comparison machine, in which the newly assembled card is placed alongside a correctly assembled 'master' model. The two cards are viewed through a twin optical system, images of the two cards passing first through mutually perpendicular polarizing filters and then through a superimposing system. The superimposed images are viewed through a rotating polarizing filter, the rotational speed being controlled by the operator. By this means the master card and the newly assembled card are displayed alternately, any differences in construction being readily detectable. A binocular attachment gives a 5 : 1 magnification of the logic cards, and missing, misplaced, reversed or damaged components are quickly located. Inspection rates of at least seven times that of simple visual methods are easily attained.

Wiring schedules for the printed-circuit cards are prepared by the program already described. For each wire on the schedule the operator will note the source and destination positions, measure the length of wire

required, prepare this wire length and temporarily secure it to the card in the same way as the components. The completed assembly is then again inspected, the wiring being 'buzzed' for continuity, and after acceptance is sent for flow-soldering.

On return from the flow-solder machine the card is inspected for solder troubles (dry areas, bridges etc.) and then forwarded to the computer commissioning bay.

3.4 *Commissioning*

In the commissioning bay the completed computer is fitted with its plug-in power supply units, each pretested, and its complement of logic cards. At this stage the logic cards are merely located in their guides, and not plugged into their respective edge-connectors until the power system is operative. First steps in the commissioning procedure are directed to switching on the complete power system, usually a sequencing process whereby successful operation of the first power unit provides the turn-on signal for the second, until all units are at rated voltage. The process of setting up the power system will take only a matter of hours.

Having ensured that power exists on all racks in the logic system, there remains no alternative but to plug in the logic cards and attempt to run test programs. Before this can be achieved it is essential to make sure that the machine is able to perform every instruction in its specification correctly, and these are attempted singly, and in slow motion, by the commissioning engineers.

Using the engineer's control panel contained within the central processor, the machine is put into step-by-step mode, in which each press of the 'operate' key will advance the central timer by one beat, one cycle, one address of the internal 'micro-program' or one complete instruction, depending upon the mode selected. A set of keys is provided enabling the engineer to set up the instruction to be executed, and for each instruction set up the machine is stepped through the micro-program of operations necessary for its execution. Each address in the micro-program provides both the control signals required for execution of the instruction and the address of the next point in the micro-program. Thus the instruction is first decoded, this providing the address of the first point in the micro-program, and this address selected. Selecting the first address will generate the appropriate control signals, and the second address. Selecting the second address will generate further control signals and a third address, the process continuing until the starting address is re-selected, by which time the sequence of control signals will have performed the instruction specified, all being well.

The operation of the address selection mechanism, together with the data-flow produced by the control signals, is checked by watching the display panel, this giving a visual display of the contents of all the registers in the computer, the current micro-program address, the address of the next point to be selected and the logical state of the more important control signals in the machine. Errors in the control logic will be seen as the selection of incorrect addresses in the micro-program, or no address, or several addresses simultaneously. Errors in the data logic will be seen as information bits lost or 'picked-up' as data are transferred between registers.

As the machine is carefully stepped through the instruction repertoire the commissioning engineer will stop when an error condition is indicated on the display panel, and locate the offending signal, which will be caused by either an error in the backwiring or on a logic card. The error is corrected and the search continued.

As the control sequence for each instruction is established, and control returns to the start point, it is possible to switch the timer to full speed and to find data-flow errors much more quickly. If, for example, the control sequence for the instruction 'add to main accumulator' is cleared of errors, and the machine set up to perform the instruction repetitively with operand 'one', the operator will observe that the display of the main accumulator shows a count process. Any error in the data-flow logic will upset the count at some point, and this will be seen and investigated.

When all instructions possible have been cleared of faults the machine is ready for connection to the store unit. This will have been commissioned in a similar manner, and thoroughly tested by program on a working central processor. A set of basic peripherals (tape reader, tape punch, teleprinter), all fully commissioned and operational, is connected to the processor and an attempt made to read in the first test-program. When this is successful the commissioning process speeds up markedly, the remaining errors in the data-paths being located by special programs designed to test all possible combinations of data patterns in the data-registers and arithmetic units, reporting on the teleprinter any error conditions detected.

During the program-running stage of commissioning there will of course be occasional failures of the computer logic due to burn-in of isolated components, and also failures due to intermittent faults caused by defective components, dry solder joints, loose connections and the like. These faults are located by applying stimuli in the form of mechanical vibration and thermal cycling, the latter by placing the computer in an environmental chamber and subjecting it to alternate hot and cold conditions while running test-programs.

Following a lengthy period of such testing the machine is delivered to the final test area, where it is fitted with its complete complement of peripheral equipments, and the system as a whole put on evaluation trials. Finally, and immediately prior to despatch, the installation is subjected to a rigorous quality control check embracing all aspects of manufacture, from program operation under worst case power margins to the standard of paintwork on the cabinets.

4. The Feasibility of Automation

While it is obvious that the system of production and testing just described falls considerably short of the ideal, it is equally apparent that, due to the large number of differing assembly operations and techniques required in computer manufacture, a completely automated system of computer mass-production would not be viable at the present time.

More important, and more practical, is to assess which operations introduce the most errors into the system, and in consequence cause the most trouble in commissioning. The briefest analysis points at once to the backwiring and the logic cards, not surprisingly, for these constitute the bulk of the computer itself and account for the majority of the assembly operations. Of the remaining items the assembly of the mechanical hardware takes but a short time, and is simple to inspect, installation of the power cable harness seldom causes difficulties and this coupled with the installation of pre-tested power supply units usually limits the time taken to commission the power system to a matter of minutes or hours only.

Both the backwiring and the logic cards however present a less satisfactory picture. Each backwiring system comprises some five thousand wire links, and each of the two hundred logic cards entails some eleven hundred assembly operations. Added to all this is the visual and electrical inspection at all stages of manufacture. All these operations are performed manually and are both tedious and repetitive, requiring intense concentration, care and meticulous precision. It is asking too much of human endurance to expect that the thousands of assembly operations called for will be executed without error and the results bear out these fears.

4.1 *The Backwiring*

Although the high standard of inspection produces a remarkably low error rate in the backwriting, typically 0·1% to 0·2%, the system in use provides ample scope for improvement. Errors are introduced in several ways: in the first instance the operator has to read the wire termination locations from a printed schedule, remember them, and insert the wire. It is all too easy to misread or forget the true location. In locating the correct terminal to wire-wrap, the operator then has to count down the terminal column, as the preceding layers of wiring soon obscure the identifications on the edge-connector moulding. Errors due to mis-counting are frequent. Admittedly careful inspection will reveal any missing links, and also those with one end on the correct terminal and the other incorrect. This process of inspection is thus invaluable, but still inadequate, for any links completely misplaced, i.e. with both ends on an incorrect and possibly unused terminal, will be missed. Errors of this type can usually be located by a statistical checking process of counting the number of wire-wraps on each terminal pin, and comparing with a list showing the correct counts. This method of inspection, which is capable of excellent results, is time-consuming and relies on the inspector carrying out a particularly tedious operation with the utmost care. Any inspection process is really one of 'bolting the stable door after the horse has gone', and this is no exception. What is required is some system that will ensure that it is completely impossible to insert a link incorrectly, and thus to eliminate entirely the need for inspection. Ideally this would take the form of an automatic wiring machine, with a power driven wrapping head driven by remote-control from a program source of wiring information. Such machines do exist, but are usually limited in application and necessitate a high capital outlay, not only in respect of the wiring machine itself, but also for the tooling of the computer mechanical assembly. The wiring machines are not intended for, and are incapable of, 'homing' on to the terminal pins of the edge-connectors, but merely for positioning the wrapping head at a specified grid position prior to wrapping. Thus it is a prime requirement that the edge-connectors are accurately located in the machine frame and that the wire-wrap terminals are rigidly retained and made to lie precisely on the grid of the wiring machine. These requirements make for very high tooling costs in the computer main-frame construction, the logic racks and the edge-connectors. Additionally, the high packing density of the backwiring in modern fast computers calls for close mounting of the edge-connectors and fine pitching of the terminal pins, both factors resulting in a compacted array of terminal pins leaving the minimum of room for routeing of the wires. On these grounds alone it is found impossible to use a fully automatic wiring machine, and a better solution is to apply the automatic control to the present manually operated wiring system so as to eliminate the operator's responsibility for reading the terminal locations, selecting the wire length and identifying the correct terminal before wrapping. Final quality control of the process is ensured by linking the power supply of the wrapping gun to the automatic control such that the gun is rendered powerless until the

correct terminal is located, fulfilling the prime requirement that an incorrect link cannot now be introduced into the backwiring. This one precaution eliminates the need for any inspection other than for quality control, and removes at once about a third of the errors to be corrected in the commissioning stage. With the power system operational and the backwiring system guaranteed to be 100% correct there remains only the logic cards to cause trouble.

4.2 *The Logic Cards*

The approach in this case has to be different. The backwiring uses only one component type (the wire link), the variable parameters being just those of length and location. The logic cards, however, are built up of many different component types, and even those of the same type, e.g. resistors, have many different values. The grid for component positioning is vastly more complex, polarity may be important and each computer may incorporate some fifty to a hundred different types of logic card.

It would perhaps be possible to devise a method of automatic component insertion, and simple systems already exist. In practice it is found that the number of parameters is too great for such a system, and in any case the wired inter-connections still have to be made.

The solution chosen is to attack the problem at the testing stage, keeping the cards as simple as possible by printing as much of the wiring as is feasible and reducing the number of component types to the minimum. Careful inspection at present ensures that with a logic card on which over a thousand assembly operations are performed the final error content is typically only one or two per card. It is thus now a problem of locating the errors rapidly and accurately, and ensuring that they are eliminated before the card is installed in the computer. First attempts on these lines were to apply a simple d.c. test for logical function of the card, a bank of switches being used to apply input conditions, output conditions being observed on an oscilloscope. The test engineer would work from a logic diagram for the card in question, devising his own test routines, and systematically check each logic element in turn. Certainly this method improved matters, and obvious deficiencies such as missing components, incorrect wiring, solder-bridges and open-circuit components were usually found. Nevertheless, the process was time-consuming and inefficient. Typically it would take an hour to test a logic card. The test was only as good as the operator devised, only d.c., and there was little chance of detecting intermittent faults. There was no possibility of continually cycling the test while environmental conditions were changed, and indeed every time a card of the same type was presented for testing the operator had to re-think the test procedure. All in all there was perhaps little to be gained by manual testing, and it was often deemed preferable to install the full complement of logic cards in the computer and to detect and correct the faults *in situ*.

The testing requirements are really quite simple. The logic contained on each printed-circuit card can be tested purely as a group of connected logic elements, the true function of that logic in the complete computer being irrelevant for this purpose. All that is required is to present to the logic a set of digital patterns to the inputs, and observe the resulting set of patterns on the outputs, this constituting a complete logical test of the card, assuming of course that appropriate test patterns are applied. Furthermore, the test can be applied under a.c. conditions simply by arranging that, after the input patterns are applied, a specified time is allowed to elapse before the output patterns are inspected. This process is happily entirely suited for computer control, and the system adopted entails the storage of the test patterns applied to the card together with the expected output patterns in the computer core store, a special purpose peripheral unit being employed to assemble the patterns and control the input/output timing of the testing.

5. The Application of Automation Techniques

5.1 *A Semi-automatic Backwiring Machine*

There are three principal design features incorporated in the backwiring machine, each contributing fundamentally to the end-product of 100% correct wiring. These are:

(*a*) The information source is a punched paper tape, prepared by computer.

(*b*) Terminal pin indication is by a visual display of two co-ordinates.

(*c*) Correct terminal pin selection is verified by the machine before wiring is permitted, thereby totally eliminating incorrect connections.

The backwiring machine consists of a worktable carrying the wiring panel and visual display, a rack of tubes containing prepared lengths of wire, a paper-tape reader and the machine control unit.

The tape reader is located at one end of the worktable, the wiring panel in the centre, and the rack of tubes at the other end. The control unit for the machine is housed under the worktable.

The wiring panel is shown in Fig. 2, and consists of a retaining frame for the logic rack to be wired, together with sets of indicator lamps for display of pin co-ordinates, control signals and error states. An outlet is provided for connecting the wire-wrap gun, and also a key-operated switch for starting the machine.

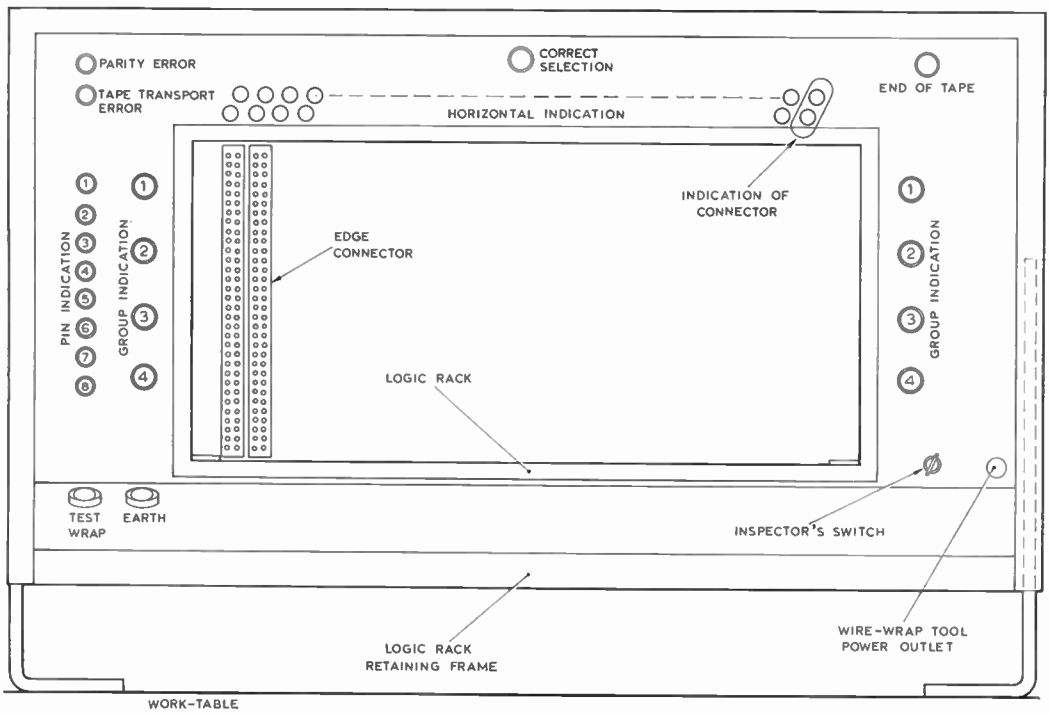

Fig. 2. Semi-automatic backwiring machine. (Operator's view of the wiring panel.)

Wiring information for the logic rack is carried on a reel of punched paper tape, this being loaded into the machine tape reader. From this tape the wiring machine gives a visual display of the co-ordinates of the pin to be wired, and an indication of the wire-length to be used. Connecting the wrapping bit of the wire-wrap gun to the correct pin lights an indicator lamp and applies power to the wiring gun. Operation of the gun then advances the tape transport, giving the next pin co-ordinates.

5.1.1 Operation of the wiring machine

Figure 3 shows a simplified block schematic of the backwiring machine, some of the less important features being omitted for the sake of clarity.

The information source is a reel of five-hole punched paper tape, prepared by the computer program mentioned earlier in this paper, but with minor alterations to the format of the final tape. The information is carried on the least significant four tracks of the tape, track five being punched to make each character odd parity. The tape reader is a low speed mechanical sensing device, with built in odd-parity checking.

For each connection to be wired the punched tape carries the following information:

(*a*) the column number (horizontal co-ordinate) and the pin number (vertical co-ordinate) of the first terminal pin,

(*b*) the wire length required for the connection and

(*c*) the column and pin number of the second terminal pin.

This information is recorded on the tape in two groups each of four characters. The first group carries the wire length information and the co-ordinates of the first (source) pin, and the second group the co-ordinates of the second (destination) pin. There is no requirement for wire length information with the second pin co-ordinates, the spare space on the tape being used for control purposes.

Before wiring can begin, the logic rack to be connected is clamped into the retaining frame, the wire-wrap edge-connectors locating under the row of horizontal indicator lamps. The backwiring information tape is then loaded into the tape reader, and the wire-wrap gun plugged into the power outlet.

Power is switched on to the wiring machine, and the start switch operated. The start switch is key-operated, the key being retained by the wiring-shop inspector. Operation of the start switch sends a 'start' pulse to the sequence control logic, initiates a tape-transport

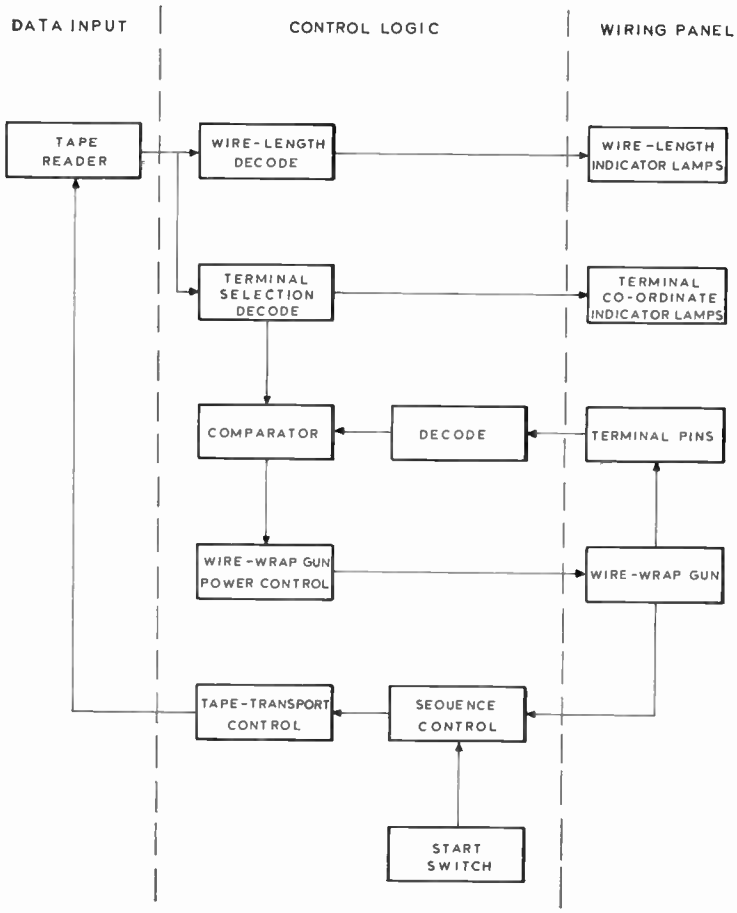

Fig. 3. Simplified block schematic of semi-automatic backwiring machine.

signal and energizes the tape reader. The first group of information characters is read and decoded, lighting a lamp opposite the tube carrying the required wire length and the co-ordinate selection lamps for the first pin to be wired.

Horizontal indication is by a single lamp over the selected column of terminal pins. Each edge-connector has two columns of pins and there are thus two lamps per connector, the upper lamp specifying the right-hand column of pins.

Vertical indication is by two lamps. The column of thirty-two pins is regarded as being split into four groups of eight pins, the display giving both the pin group and the position of the selected pin without the group. Group boundaries are prominently marked on the logic rack by stretching coloured tapes across the rack before wiring is started. It is found that this method of presentation makes for easier identification of the pins on the part of the operator, and has the secondary advantage of simplifying the decode system within the machine.

The operator selects a wire from the tube indicated and loads it into the wrapping bit of the wiring gun. All wires carried in the tubes are pre-stripped at each end, and are ready for use without any further preparation. Having loaded the gun the operator now inspects the visual display of pin co-ordinates and applies the wrapping gun to the pin he thinks is indicated. If his selection is correct the 'correct selection' lamp on the display panel is lit, together with a repeater lamp on the wiring gun.

This is the principal safeguard of the wiring machine. If the wrong pin is selected the indicator lamp is not lit; more important, no power is available at the wiring gun, and an incorrect connection cannot be made. Positive identification of the correct pin is easily achieved. The wrapping bit of the wiring gun carries a small direct voltage. A set of dummy logic

cards plugged into the edge-connectors connects every pin in the backwiring system to a decode in the machine logic. As the wrapping bit is applied to any pin in the system the direct voltage is sensed and transmitted via a decode to the comparator. If the selected pin is that specified by the information tape the comparator gives an output signal to the wire-wrap gun control logic, lighting the indicator lamps and applying power to the gun.

The operator completes the connection by operating the trigger switch on the gun, wrapping the wire end to the pin. Releasing the trigger switch sends an 'advance' signal to the sequence control logic, initiating a second movement of the tape transport and displaying the co-ordinates of the second pin to be wired. The operator then loads the free end of the wire into the gun, identifies the correct pin and completes the wire link with a second wrap, giving a new 'start' signal to the sequence control logic, the complete cycle then being repeated for succeeding wires.

In addition to the machine's basic check system for positive identification of the pin to be wired there are several ancillary protection systems built in, and worthy of mention.

The machine logic and decode system is constructed of solid-state devices and magnetic reed relays, ensuring reliable operation. The tape reader performs a mechanical parity check on each character, the machine logic performing an electrical parity check simultaneously. Detection of incorrect parity by either system locks the tape transport, lights the 'parity error' lamp on the wiring panel and sets an error bistable in the machine logic. This bistable can be reset only by removing the error condition, in this case the parity-incorrect character, and restarting the machine using the inspector's key switch.

Failure of the tape transport mechanism due to a torn tape jamming under the reading head causes a similar error state, lighting the 'tape transport error' lamp and setting the error bistable. As before, the error condition is removed and the error bistable reset using the inspector's key switch.

There are three possible control characters that can be punched on the information tape, to signify a test-wrap, earth connection or end of tape. To ensure a consistent high standard of reliability in the wire-wrapped connections it is essential that the condition of the wrapping bit be checked at frequent intervals. This is accomplished by performing a test-wrap operation, i.e. wrapping a wire on to a dummy terminal pin. The test-wrap is then visually inspected for obvious defects, and given a mechanical test, in which the pull-off force required to break the joint is measured. If the test-wrap is below standard a replacement wrapping head is fitted, and tested, the defective unit being sent for readjustment.

The backwiring information tape is punched with a test-wrap bit after every two hundred normal connections. Detection of the test-wrap bit by the control logic lights the 'test-wrap' lamp and sets the error bistable, locking the sequence control logic. The operator now performs the test-wrap and calls over the inspector who, after checking the test-wrap, restarts the machine by operating the key switch.

Most links in the backwiring are between two logic pins. There are some signals in the logic system requiring connection to earth. In these cases the first co-ordinate specifies the source pin in the usual manner, but the co-ordinates of the second pin are not displayed, being replaced by the 'earth' lamp. When this is lit the operator is required to route the free end of the wire to the nearest pin on the earth frame surrounding the edge-connectors.

The last character punched on the information tape contains the end-of-tape marker bit, detection of which lights the 'end of tape' lamp and sets the error bistable. The completely wired logic rack can then be removed, and a fresh one inserted. The tape reader is reloaded, and operation of the inspector's key switch clears the error bistable and restarts the machine.

The machine is designed for safety of operation. All units operate at low voltage, including the wire-wrapping gun which is battery-powered. The power pack is housed in the gun handle, and is rechargeable.

5.1.2 The economics of the machine

It is found that even untrained operators rapidly gain familiarity and confidence in this technique, and after only a few hours experience can reach a wiring rate of over 130 wires per hour, or just over five times the manual rate of a skilled wireman. Moreover the removal of the translation process of reading the wire co-ordinates from a printed schedule puts far less strain on the operators, reducing mental and physical fatigue. Preparing the wire lengths on a cutting and stripping machine eliminates the risk of wire damage during manual stripping of the insulation material caused by incorrectly set strippers, with an obvious saving in time and labour.

The largest savings result from the removal of the inspection process on completion of wiring, and the reduction in commissioning time resulting from 100% correct backwiring. Accurate quality control of the joints made, by means of frequent test-wraps, contributes to increased reliability of the completed computer.

The backwiring machine is completely flexible in application. The unit described is suitable for single logic racks. More complex machines suitable for inter-wiring completed single racks, and for wiring to plugs and sockets, are in use and are similar in

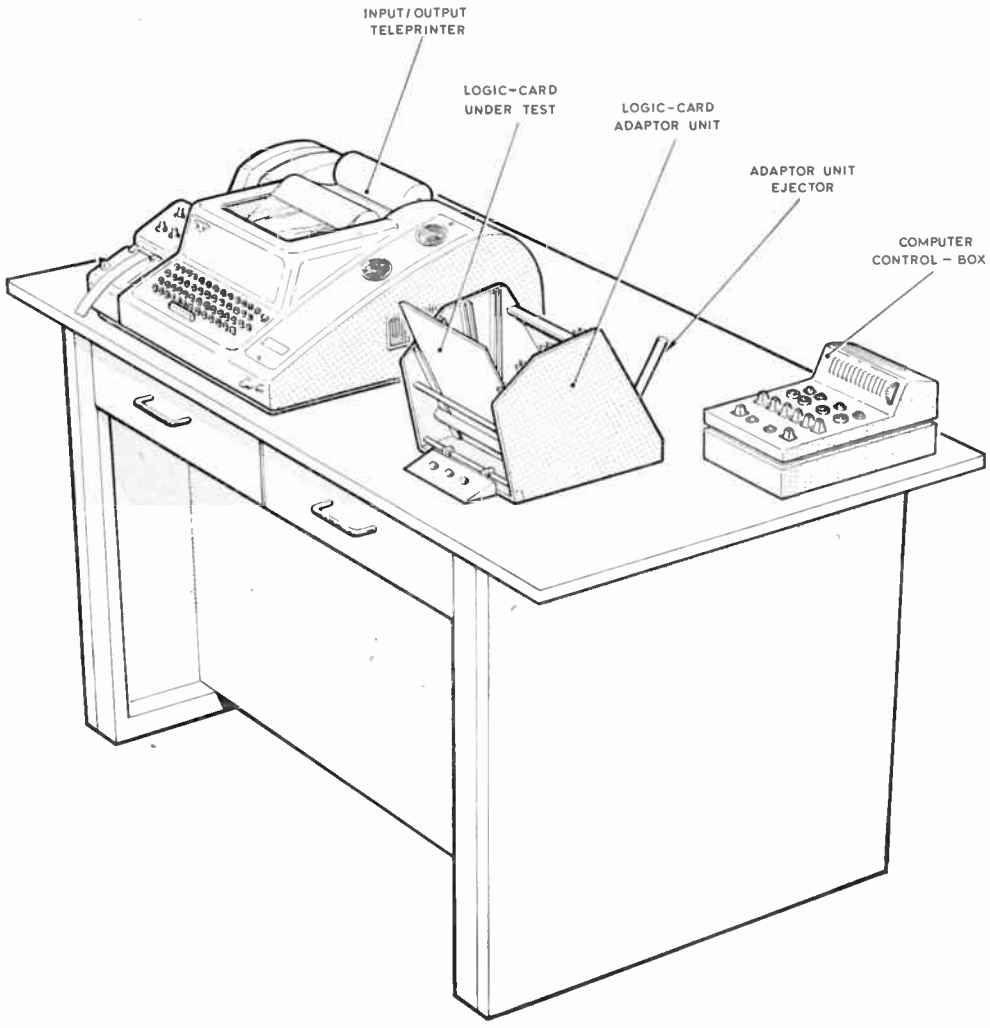

Fig. 4. Computer-controlled logic card tester—the tester unit.

operation, differing only in the size of the decode system and the layout of the wiring panel.

5.2 *Automated Testing of Logic Cards*

5.2.1 The computer-controlled logic card tester

Figure 4 shows a sketch of the tester unit, which is designed as a peripheral to any central processor in the National-Elliott 4100 data processing system. The tester unit is engineered for direct connection to the standard peripheral interface, is self-powered, and built into a free-standing desk cabinet. The desk top carries the 'adaptor' unit (into which the card to be tested is plugged), the computer control console and the input/output teleprinter used for two-way communication between operator and computer.

The desk cabinet houses the tester logic system, and power supply units able to meet the requirements of both the tester and the card under test. Drawer space is provided for storage of program and test-data tapes, and the cabinet dimensioned to enable the operator to remain seated while testing logic cards, knee space being provided beneath the drawers.

The system is designed for extremely simple operation, and is suitable for use by a single unskilled operator. The card to be tested is plugged into the test socket on the adaptor unit, and the five-digit card identifier number typed on the teleprinter. The complete test sequence is then performed automatically and at high speed. Successful completion of the test is indicated by a teleprinter message, any fault found on

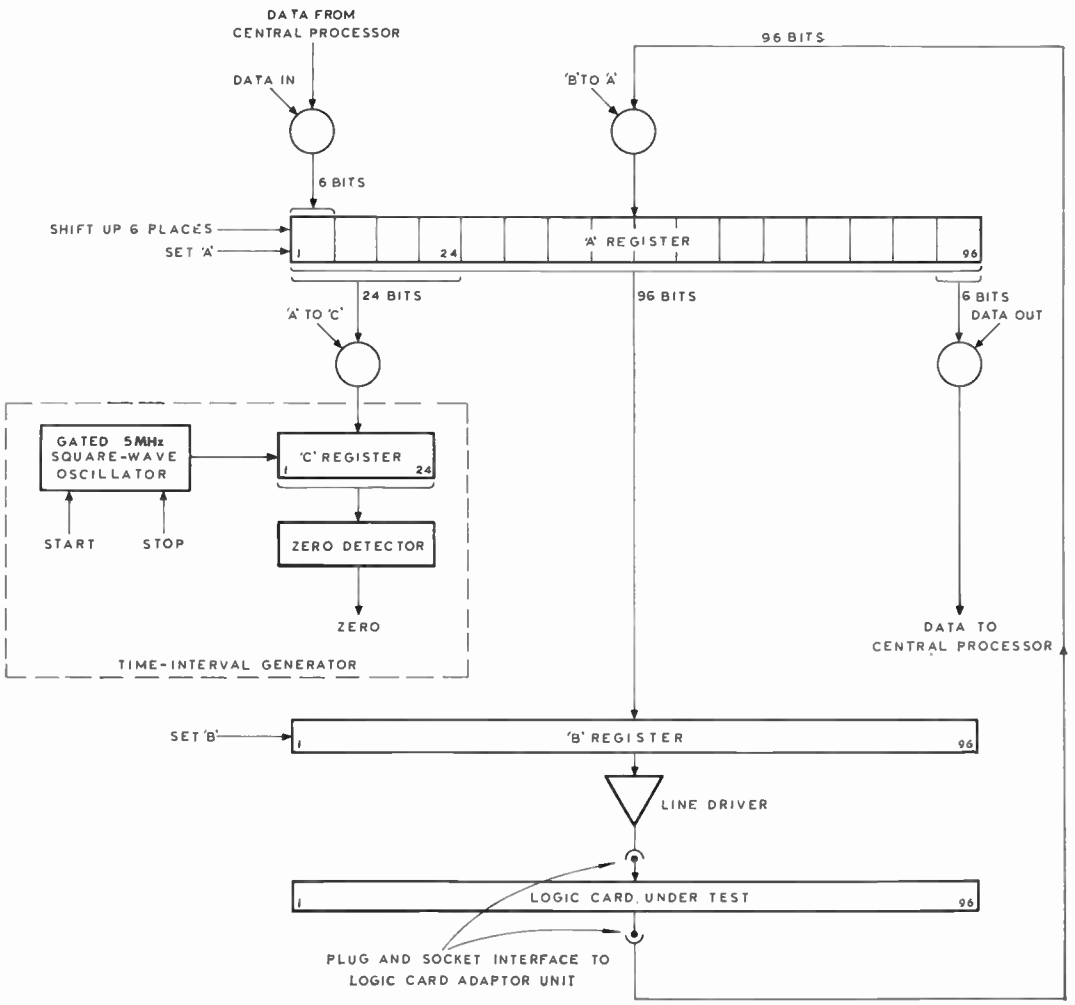

Fig. 5. Simplified block schematic of computer-controlled logic card tester.

the card resulting in an appropriate error print-out. The teleprinter pass-note or rejection slip is torn off and stapled to the tie-on progress label already attached to the card, following which the card is removed from the adaptor unit and sent either to the commissioning area for installation in a machine or for off-line rectification. Where rectification is required the failing test is reproduced on a manually operated tester, and the fault located and corrected.

A simplified block diagram of the tester logic system is shown in Fig. 5. Each test performed on the logic card consists of applying a logic pattern to the input pins, waiting a short time, and reading back the logic pattern of the output pins. In practice the pattern is both applied to and read back from all pins on the card edge-connector, the test data being written to differentiate between output and inputs.

The pattern to be applied to the card is output from the computer to the tester as a stream of sixteen six-bit characters, and is assembled into the 'A' register to form a 96-bit word. On receipt of a control character the contents of the 'A' register are transferred to the 'B' register, which is connected via line drivers to the test socket. The action of setting the 'B' register thus applies the input pattern to the card under test.

After a short, preset delay (to allow the logic on the card to settle), the resulting logic pattern on the card connector pins is set into the 'A' register, and stored ready for input to the computer for checking.

The card output pattern is transmitted to the computer as a stream of sixteen six-bit characters, both input and output of data thus being handled by the 'A' register. Input is by shifting the data pattern into

the 'A' register at the least significant end in six-bit blocks, and output by a similar process, shifting up and out of the most significant end.

The standard delay chosen between applying the input conditions to the card and inspecting the outputs is 200ns. Where purely d.c. logic elements are being tested the operation of the tester is precisely as described, the input patterns applied being selected to test fully the logic on the card under test, the output pattern for each being checked against the expected conditions as stored in the computer.

Where the card contains a.c. logic elements, such as pulse generators, there is a requirement for specifying a longer time after which the output pattern should be inspected, and this function is provided by a time-interval generator. When testing a.c. elements the input conditions are applied to the logic card, the outputs being set into the 'A' register only on receipt of a signal from the time-interval generator.

The time-interval generator comprises an oscillator, count register and zero detector. A specified time-interval is generated by loading the 'C' register with the number of 200ns time units required. Setting the 'B' register simultaneously applies input conditions to the card under test and sends a 'start' signal to the gated oscillator, each cycle of which reduces the count by one. When, after the time required, the count in the 'C' register becomes zero, as indicated by the detector, a signal is generated which sets the card output conditions into the 'A' register. At the same time a 'stop' signal is sent to the oscillator, so that the contents of the 'C' register remain at zero.

Where a timed test is specified in the test-data the program loads the correct number into the 'C' register before outputting the data pattern into the 'A' register. This is accomplished by outputting four six-bit characters to the 'A' register, opening the 'A' to 'C' gate, and setting the 'C' register to the 24-bit number assembled in the least significant 24 bits of 'A'.

The 24-bit length of the 'C' register provides for time-intervals from 200ns to a little over 3 seconds, in steps of 200ns. Where longer times are required these are generated by software, using a time reference derived from mains frequency.

The oscillator used to control the time-interval generator is an astable device comprising two high-speed integrated logic-circuit packages connected via coaxial cable delay lines, giving a low-cost frequency source accurate to within $\pm 1\%$ over a wide range of temperature and power supply variations.

The tester logic is constructed from the proven high-reliability diode-transistor logic used in the 4100 computing system, and is thus matched for testing logic cards for this system. Interfacing logic, when required for testing different logic types, is housed in the adaptor unit into which the card under test is plugged, the adaptor unit acting as both an electrical and a mechanical interface between the tester and the card under test. The adaptor unit is connected to the tester by a set of multi-pin plugs and sockets, and is readily interchangeable by means of the ejector/insertor handle, this being necessary to overcome the high insertion and withdrawal forces incurred by the multi-pin connector interface.

A range of adaptor units exists, covering the various combinations of logic and edge-connector types in current production. The introduction of a new combination is met by producing an appropriate adaptor unit.

5.2.2 The software system

The system software is specifically designed to be both simple and compact. The tester is operated by a single control program occupying only 1000 words of core store, leaving over 7000 words of test-data storage, assuming a (minimum) store size of 8192 words.

The control program handles the input of test-data, assembly of test patterns, servicing of the tester, checking of test results and two-way teleprinter communication with the operator.

To optimize the utilization of store space the test-data are presented to the control program in a highly compact precompiled format. The test-data are written as a list of logical conditions, e.g. switching input X from logic 'one' to logic 'zero' should make output Y switch from logic 'zero' to logic 'one' after time Z. The data are first punched on paper tape complete with all the layout characters necessary to preserve a legible print-out, and then converted to the format acceptable to the control program using a special data compiler.

Essentially the economy of data storage space results from the conversion of the original test-data into an entirely digital form. The initial test applied to the card is fully specified, i.e. the logical state of every pin on the connector is described. From this fully-defined starting point subsequent tests are listed as a set of 'change' instructions, e.g. change pin X and expect pins Y and Z to change: then change pin P and expect pin Q to change. There is thus no need to distinguish between input and output pins, or to store the logical state of each pin for every test, but merely to specify the sequence of changes to be made and expected, starting from the original state. There is thus only one item of information relevant to each pin mentioned in the test, namely that its logical state is switched with respect to the preceding test. The compiler translates the test-data from the full format as punched to the pin-change list required by the control program. Typically a complete test schedule

for a logic card, comprising some 50 tests each involving an average of three pin changes, will after compilation require only 100 words of store, giving a storage capacity of some 70 test schedules in 7000 words of store. The data compiler outputs on paper tape the precompiled test data for each logic card, followed by a dictionary enabling the control program to locate the address in store of individual test schedules.

The complete precompiled data tape (plus dictionary) is read into store by the control program on receipt of a teleprinter message. The control program incorporates a self-dump routine, enabling the store contents (program + data + dictionary) to be output on paper tape in a 'load and go' form, giving a means of reproducing worn tapes.

All data tapes are punched in 8-hole even-parity sum-checked format, the programs checking both parity and sum-check on input.

The control program incorporates a number of refinements which widen the scope of the testing process to include detection of intermittent faults, slow logic elements and short-circuits between logic pins and power rails.

The facility exists for continuously cycling the test schedule with a card under test, using teleprinter control to start and stop the program cycling. Thus while a logic card is undergoing continuous testing it may be subjected to vibration and/or temperature variations, this proving invaluable for detecting intermittent faults such as dry joints, diodes with damaged glass seals, cracked metal film resistors, low-gain transistors etc. It is found that even the most rudimentary of environmental tests is effective in locating faults of this nature, typical examples being the use of a rubber hammer to tap components on the card, a portable hair-drier to blow warm air over the logic elements and an aerosol spray for localized cooling. The importance of this facility cannot be over-emphasized, for in the absence of a means of detecting intermittents at the card test stage there is no alternative but to apply environmental tests to the entire computer during program running. This is far less desirable, as the occurrence of an intermittent fault often causes loss of control of the test program with little or no indication of the source of the fault. Worse still, there may be several intermittents to find, occurring in random order and producing differing symptoms. Detection and elimination of such faults at the card test stage may often save hours of commissioning time, and in addition contributes to increased reliability of the computer.

The control program also incorporates a routine for detecting slow logic elements. When any test fails to produce the expected output the program automatically re-enters the test schedule, and on reaching the failing test repeats it with a longer time allowed between applying the inputs and inspecting the outputs, this process being repeated with an additional 200ns allowed on each succeeding attempt, until an upper limit of 2 μs is reached. If the test still fails a normal error message is printed, otherwise the message contains an additional line stating the time-interval required for successful operation.

To ensure that the tester is not damaged by short circuits on the card under test special circuitry is built in to check the impedance between each logic pin and the power rails before testing proper is attempted. The circuitry is biased off during normal testing and is switched into use by the control program immediately prior to testing a card. Where a low impedance path is detected an error message is output on the teleprinter identifying the offending logic pins, and in this case testing is inhibited, no power being applied to the card under test. By this means both the tester and the card under test are protected against damage.

A valuable safeguard provided in the control program is an automatic check of the bulk of the tester logic system. At the completion of every card test, and following removal of the card, the tester data-registers and control logic are examined by the transmission of test patterns to the (empty) card test socket. Figure 5 shows that there is a closed loop containing the 'A' register, 'B' register, line-drivers and card test socket, enabling test patterns to be assembled in 'A', transferred to 'B' and read back into 'A', this procedure checking the two data registers, data lines and control logic. Any fault detected results in an error print-out identifying the data line at fault and the card responsible. A set of spare cards is kept, enabling a serviceable spare to be fitted, and the tester then used to diagnose the fault on the defective card. The speed of the tester is principally a function of the instruction-time of the computer used to control it. Typically, using a 4120 computer with a 6 μs store, a test takes 350 μs, with 1 ms between successive tests. Thus a card test schedule of several hundred discrete tests would take less than a second to perform, and indeed more time is consumed in handling the cards to be tested and typing teleprinter messages than is spent in actual testing. An operational speed of from 150 to 250 cards per hour is easily attained, compared with one per hour using manual techniques. It is now perfectly feasible to test the full complement of logic cards used in a computer in the time formerly taken to test any one of them by hand.

6. The Trend towards Further Automation

The two automation techniques described were designed to fulfil a basic need in the current production of second-generation computers, and at the same time

were regarded as the first tentative steps towards a more comprehensive scheme for automating the production and testing of both second- and third-generation machines. The problems which these techniques help to overcome arise principally from the vast numbers of discrete components used in the construction of second-generation equipment, entailing a correspondingly large number of assembly operations and inspection stages.

The introduction of the third-generation computers dramatically reduces the number of components necessary to construct a computer. Several logic elements are now contained within a small monolithic package which fulfils the function previously requiring perhaps fifty discrete components, and occupies about a fifth of the space. The logic card becomes a multilayer structure with all power and logic inter-connections tracked, and the backwiring system a printed-circuit card with only 20–30% of the inter-connections as wired links.

In consequence the reduction in the number of assembly operations, coupled with automatic checking of the remaining wire links in the backwiring and fully automated testing of the logic cards, results in an assembled machine with a high probability of immediate and correct operation at switch-on. At worst the commissioning problem is one of locating the very few faults in what may be a large and complex computer with a repertoire of several hundred instructions. The conventional method of stepping through the micro-program for each instruction proves most inefficient, most of the time being spent in a painfully slow process which serves only to verify that the majority of instructions are in fact obeyed correctly. At this stage of manufacture the capital value of the equipment undergoing commissioning may well be many thousands of pounds, and any wastage of time is costly. An automated commissioning technique becomes imperative, and an obvious development is the use of one computer to commission another. A more sophisticated version of the computer-controlled logic-card tester is at present being applied in this direction, the 96-bit tester interface being used to supply the instruction to be obeyed, to simulate operation of the step-by-step timer control and to monitor the micro-program address selection logic and data-register contents. By this means the computer under test can be made to execute every instruction in its repertoire at high speed, with a continuous watch kept on the micro-program addressing and data flow between registers. Any errors occurring are detected by the controlling computer, which is programmed to give a detailed print-out of the fault condition, the instruction being executed and the probable location of the trouble.

The advantages to be gained from the use of an external computer as a test device are plainly apparent in this application. A very large and complex test schedule can be run in a short space of time, enabling the fault condition to be detected quickly, and accurately identified.

The high speed of computer aided testing permits a test sequence formerly taking many days to be cycled once every few seconds, so that when the last fault has been cleared from the machine under test the controlling program may be cycled to search for intermittents, with the computer subjected to vibration and thermal disturbance. Most important of all, the occurrence of an intermittent fault is detected and the origin located without loss of the test program, since this is now run by the external computer.

7. Conclusions

The progressive introduction of the automation techniques described in this paper is already making an impact on present computer production, and the results so far obtained are most encouraging.

The recent advances in multi-layer printed-circuit techniques and the use of monolithic integrated-circuit packages have realized a several-fold increase in both the packing density and the overall reliability of logic systems. In consequence there is a growing tendency for third-generation computers to be logically of far greater complexity than their predecessors, and data processing systems of immense computing power are now either in production or advanced stages of design.

As logic systems increase in speed and complexity, the problems of fault-finding in manufacture become harder, and the costs of delays become greater. In the author's opinion the application of automation to all stages of manufacture (design, documentation, assembly, testing and commissioning) will soon be regarded not simply as a desirable aid, but as an essential tool for commercial viability.

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Radio Engineering Overseas . . .

The following abstracts are taken from Commonwealth, European and Asian journals received by the Institution's Library. Abstracts of papers published in American journals are not included because they are available in many other publications. Members who wish to consult any of the papers quoted should apply to the Librarian giving full bibliographical details, i.e. title, author, journal and date, of the paper required. All papers are in the language of the country of origin of the journal unless otherwise stated. Translations cannot be supplied.

VARACTOR DIODES AS FREQUENCY MODULATORS

In f.m. broadband audio links klystrons have generally been used for modulation of the carrier. Recently, however, a solid-state device for this purpose has been developed by Japanese engineers.

Capacitance-voltage characteristics for hyper-abrupt junction diodes operating in the 70 MHz band were plotted and their modulation linearity was determined. The modulation linearity was found to be satisfactory over a wide frequency range and a communication system consisting of 1800 channels was realized by using this type of modulator.

This modulator was found to be superior to the klystron modulator in respect of stability, reliability and cost. The noise figure is very much improved and the circuitry is simple. Further studies to improve the characteristics of the diode and to decrease the total number of diodes used in the modulator have also been successful.

'Frequency modulators using variable capacitance diodes', K. Noda, *Review of the Electrical Communication Laboratory NTT*, **15**, 7–8, pp. 507–30, July–August 1967.

OPERATIONAL AMPLIFIER

A d.c. amplifier with feed-forward coupling is described in a recent German paper. This amplifier is particularly suitable for use as an operational amplifier in analogue computers in addition to conventional applications. Attention has been given in the design not only to a large bandwidth but also to a high stability under capacitive load conditions at the input and output.

Another special feature of the design is the roll-off of the voltage gain of about 20 dB per decade in the region from 0·2 kHz (110 dB) to 100 MHz (0 dB), which leads to a good pulse response in addition to wideband applications.

Possibilities for improving the dynamic range and the drift characteristics are mentioned. A design with drift figures of 1 μV/degC and 0·1 nA/degC without a substantial reduction in bandwidth is quoted.

'A wideband operational amplifier with feed-forward coupling', R. Bladowski, B. Murari and G. M. Riva, *Nachrichtentechnische Zeitschrift*, **20**, No. 9, pp. 521–9, September 1967.

PUNCHED-TAPE READER

A new high-speed punched-tape reader has been developed in Holland which is capable of reading-speeds up to 2500 characters per second without requiring a buffer store. This speed is possible because the tape can be stopped extremely quickly, 'on' a character: if the 'stop' signal is given as soon as a character appears, the same character is still visible when the tape has stopped. At a tape speed of 1200 characters/s the stopping distance is no greater than 0·5 mm. Use is made of double optical character read-out. The punched tape is transported by pressing it against a permanently rotating driving roller by means of a pressure roller controlled by an electro-magnet. Braking is effected by energizing a very fast electromagnet whose armature is in permanent sliding contact with the tape, so that the distance to be travelled by the armature is extremely small. Upon braking, a shock wave is generated in the tape, and this travels along the moving tape at the speed of sound. The stopping distance calculated on this basis is found to be in good agreement with the measurements. A description is given of the optimum design of the braking magnet for rapid braking. This braking magnet is energized by a special transistor circuit which applies a very high voltage to the magnet for a very short time enabling the desired current to be reached in a much shorter time than might be expected from the time constant of the magnet.

'A high-speed punched-tape reader', J. M. Visscher, *Philips Technical Review*, **28**, No. 9, pp. 259–70, 1967.

AERIALS IN MOVING MEDIA

With the rapid advancement of space technology and rocket technology, analysis of electromagnetic fields in a moving system is becoming an important technological problem.

Two Japanese engineers discuss the problem by first deriving the principle of radiation pattern synthesis of an antenna array in an isotropic linear medium moving with a uniform speed sufficiently small compared to the velocity of light. This principle states that the radiation pattern of an antenna array composed of several arbitrary antennas in a moving medium can, if the current amplitude and the directivity of each antenna are the same, be obtained as the product of the radiation pattern of a single antenna in the moving medium and the radiation pattern of the array in which isotropic point sources of equal amplitude are arranged at the reference points of all the antennas in the moving medium.

With this result, it becomes clear that the study of the radiation pattern of an array composed of isotropic point sources in a moving medium has an important practical significance. As typical examples, the radiation patterns of a linear array and of a circular array composed of isotropic point sources in a moving medium are found. Numerical examples for each case are given, and it is shown that not only the propagation constant of its radiation field but also its radiation pattern changes compared to the case of a stationary medium.

'Radiation characteristics of antenna arrays in a moving medium', H. Fujioka and N. Kumagain, *Electronics and Communications in Japan* (English language edition of *Denki Tsushin Gakkai Zasshi*), **49**, No. 8, pp. 100–7, August 1966.