

RF

Transistor

**Thyristor &
Diode
Manual**

Technical Series SC-14 | Suggested Price \$ 2⁵⁰

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RCA

Transistor Thyristor & Diode Manual

This manual, like its preceding edition, has been prepared to assist those who work or experiment with semiconductor devices and circuits. It will be useful to engineers, educators, students, radio amateurs, hobbyists, and others technically interested in bipolar transistors. MOS field-effect transistors, thyristors (SCR's and triacs), silicon rectifiers, and other semiconductor diodes.

This edition has been thoroughly revised to cover the latest changes in semiconductor-device technology and applications. The **Technical Data Section**, as well as the text material, has been greatly expanded and brought up to date. Of particular interest to the hobbyist and experimenter are the many practical and timely additions to the **Circuits Section**.

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Typical Packages



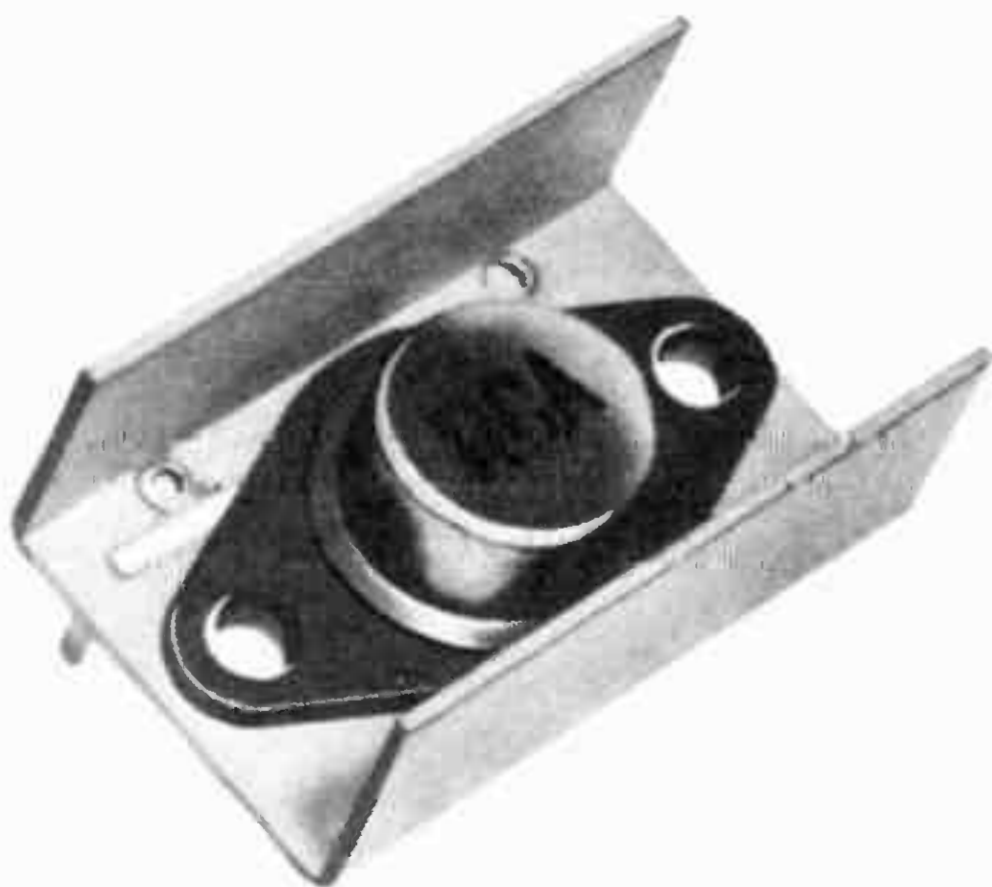
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Materials, Junctions, and Devices

SEMICONDUCTOR devices are small but versatile units that can perform an amazing variety of control functions in electronic equipment. Like other electron devices, they have the ability to control almost instantly the movement of charges of electricity. They are used as rectifiers, detectors, amplifiers, oscillators, electronic switches, mixers, and modulators.

In addition, semiconductor devices have many important advantages over other types of electron devices. They are very small and light in weight (some are less than an inch long and weigh just a fraction of an ounce). They have no filaments or heaters, and therefore require no heating power or warm-up time. They consume very little power. They are solid in construction, extremely rugged, free from microphonics, and can be made impervious to many severe environmental conditions. The circuits required for their operation are usually simple.

SEMICONDUCTOR MATERIALS

Unlike other electron devices, which depend for their functioning on the flow of electric charges through a vacuum or a gas, semiconductor devices make use of the flow of current in a solid. In general, all materials may be classified in three major categories—conductors, semiconductors, and insulators—depending upon their ability to conduct an electric

current. As the name indicates, a semiconductor material has poorer conductivity than a conductor, but better conductivity than an insulator.

The materials most often used in semiconductor devices are germanium and silicon. Germanium has higher electrical conductivity (less resistance to current flow) than silicon, and is used in devices intended for applications that require low voltage drops at high currents and in some small-signal transistors. Silicon is more suitable for high-power devices than germanium. One reason is that it can be used at much higher temperatures. In general, silicon is preferred over germanium because processing techniques yield more economical devices. As a result, today, silicon tends to supersede germanium in almost every type of application, including the small-signal area, unless a very low device voltage drop is required.

Resistivity

The ability of a material to conduct current (conductivity) is directly proportional to the number of free (loosely held) electrons in the material. Good conductors, such as silver, copper, and aluminum, have large numbers of free electrons; their resistivities are of the order of a few millionths of an ohm-centimeter. Insulators such as glass, rubber, and mica, which have very few loosely held electrons, have resistivities of several million ohm-centimeters.

Semiconductor materials lie in the range between these two extremes, as shown in Fig. 1. Pure germanium has a resistivity of 60 ohm-centimeters. Pure silicon has a considerably higher resistivity, in the order of 60,000 ohm-centimeters. As used in semiconductor devices, however, these materials contain carefully controlled amounts of certain impurities

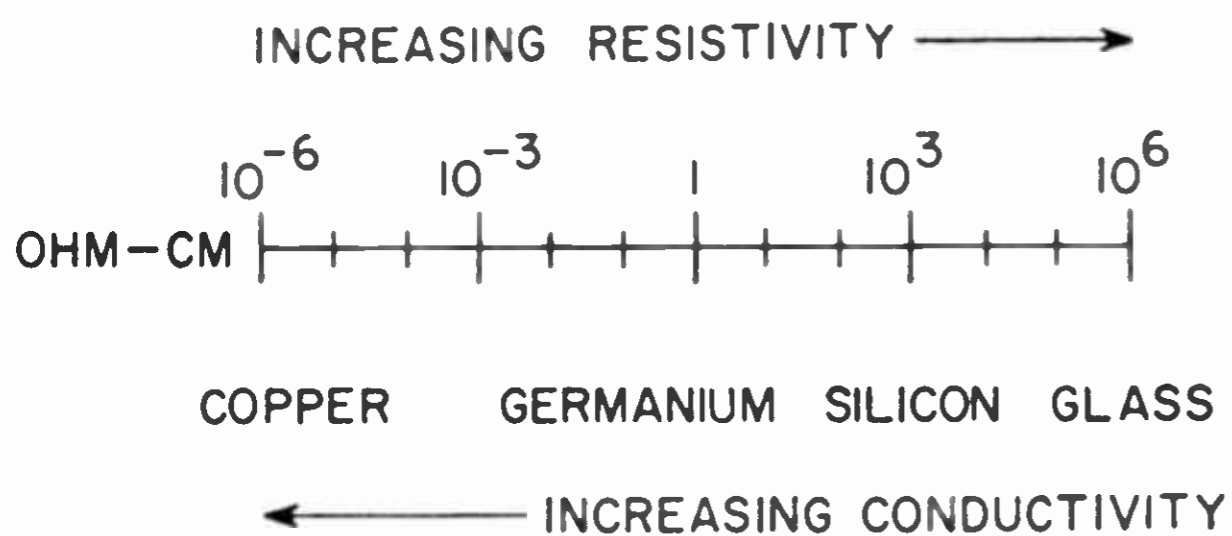


Fig. 1—Resistivity of typical conductor, semiconductors, and insulator.

which reduce their resistivity to about 2 ohm-centimeters at room temperature (this resistivity decreases rapidly as temperature rises).

Impurities

Carefully prepared semiconductor materials have a crystal structure. In this type of structure, which is called a lattice, the outer or valence electrons of individual atoms are tightly bound to the electrons of adjacent atoms in electron-pair bonds, as shown in Fig. 2. Because such a

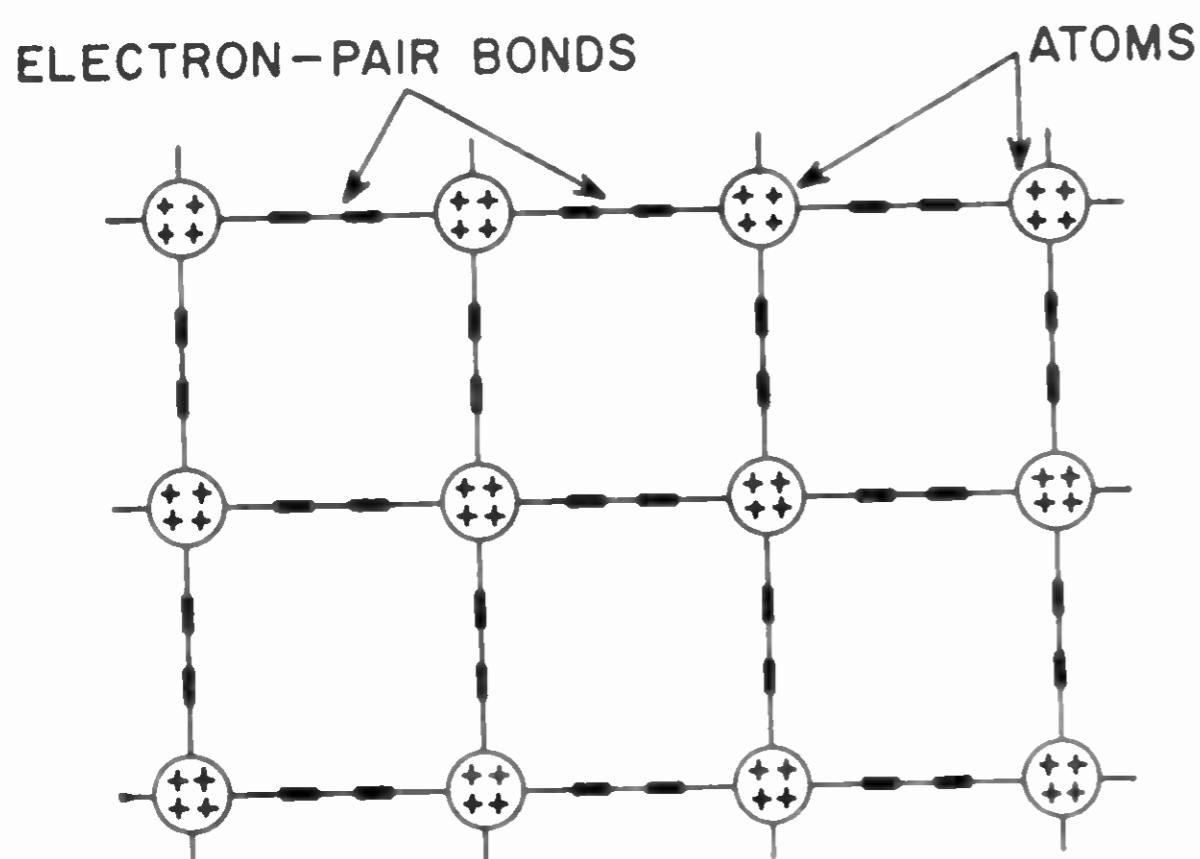


Fig. 2—Crystal lattice structure.

structure has no loosely held electrons, semiconductor materials are poor conductors under normal conditions. In order to separate the electron-pair bonds and provide free electrons for electrical conduction,

it would be necessary to apply high temperatures or strong electric fields.

Another way to alter the lattice structure and thereby obtain free electrons, however, is to add small amounts of other elements having a different atomic structure. By the addition of almost infinitesimal amounts of such other elements, called "impurities", the basic electrical properties of pure semiconductor materials can be modified and controlled. The ratio of impurity to the semiconductor material is usually extremely small, in the order of one part in ten million.

When the impurity elements are added to the semiconductor material, impurity atoms take the place of semiconductor atoms in the lattice structure. If the impurity atoms added have the same number of valence electrons as the atoms of the original semiconductor material, they fit neatly into the lattice, forming the required number of electron-pair bonds with semiconductor atoms. In this case, the electrical properties of the material are essentially unchanged.

When the impurity atom has one more valence electron than the semiconductor atom, however, this extra electron cannot form an electron-pair bond because no adjacent valence electron is available. The excess electron is then held very loosely by the atom, as shown in Fig. 3, and

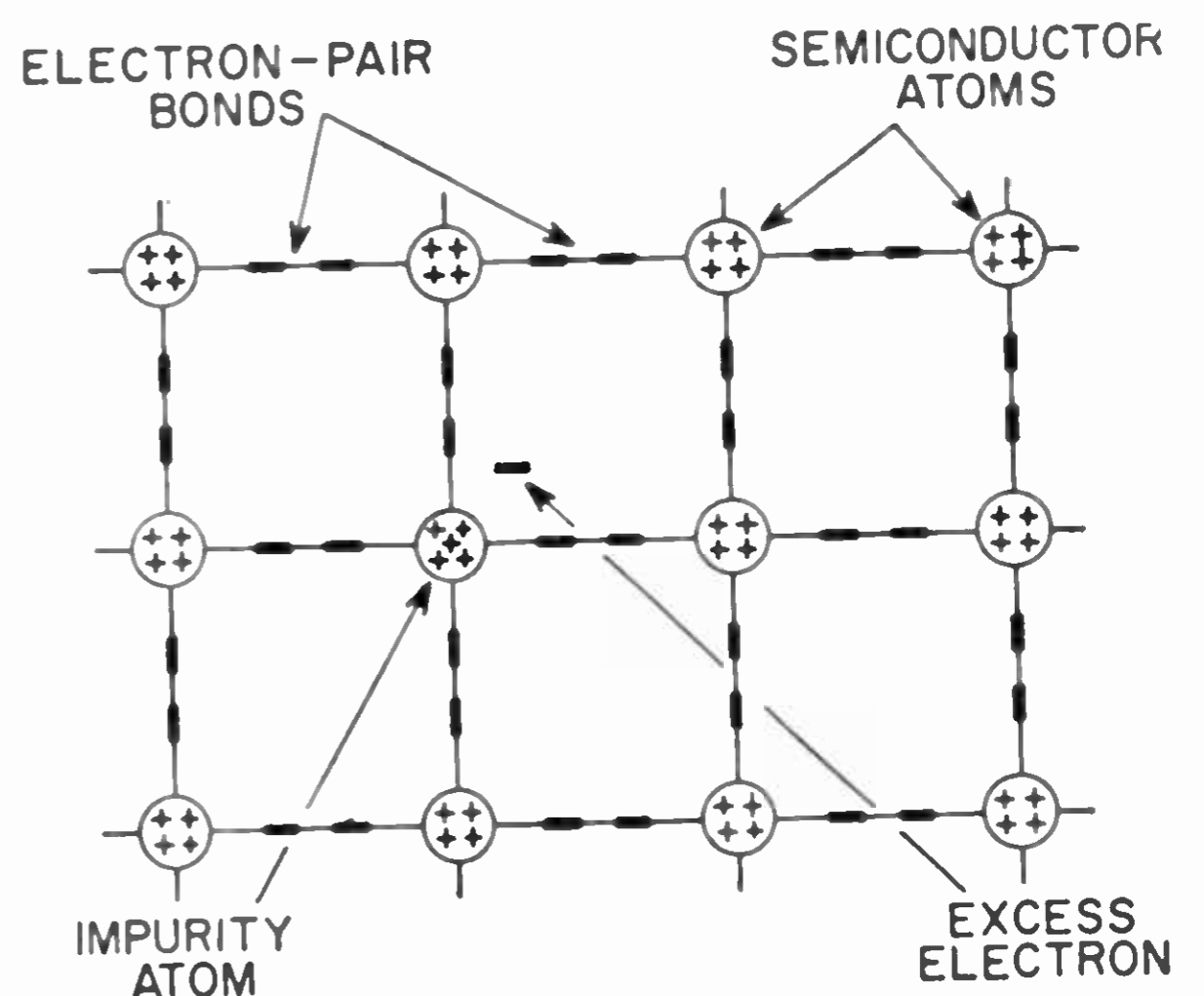


Fig. 3—Lattice structure of n-type material.

requires only slight excitation to break away. Consequently, the presence of such excess electrons makes the material a better conductor, i.e., its resistance to current flow is reduced.

Impurity elements which are added to germanium and silicon crystals to provide excess electrons include arsenic and antimony. When these elements are introduced, the resulting material is called n-type because the excess free electrons have a negative charge. (It should be noted, however, that the negative charge of the electrons is balanced by an equivalent positive charge in the center of the impurity atoms. Therefore, the net electrical charge of the semiconductor material is not changed.)

A different effect is produced when an impurity atom having one less valence electron than the semiconductor atom is substituted in the lattice structure. Although all the valence electrons of the impurity atom form electron-pair bonds with electrons of neighboring semiconductor atoms, one of the bonds in the lattice structure cannot be completed because the impurity atom lacks the final valence electron. As a result, a vacancy or "hole" exists in the lattice, as shown in Fig. 4. An electron from an adjacent electron-pair bond may then absorb enough energy to break its bond and move through the lattice to fill the hole. As in the

case of excess electrons, the presence of "holes" encourages the flow of electrons in the semiconductor material; consequently, the conductivity is increased and the resistivity is reduced.

The vacancy or hole in the crystal structure is considered to have a positive electrical charge because it represents the absence of an electron. (Again, however, the net charge of the crystal is unchanged.) Semiconductor material which contains these "holes" or positive charges is called p-type material. P-type materials are formed by the addition of aluminum, gallium, or indium.

Although the difference in the chemical composition of n-type and p-type materials is slight, the differences in the electrical characteristics of the two types are substantial, and are very important in the operation of semiconductor devices.

P-N JUNCTIONS

When n-type and p-type materials are joined together, as shown in Fig. 5, an unusual but very important phenomenon occurs at the interface

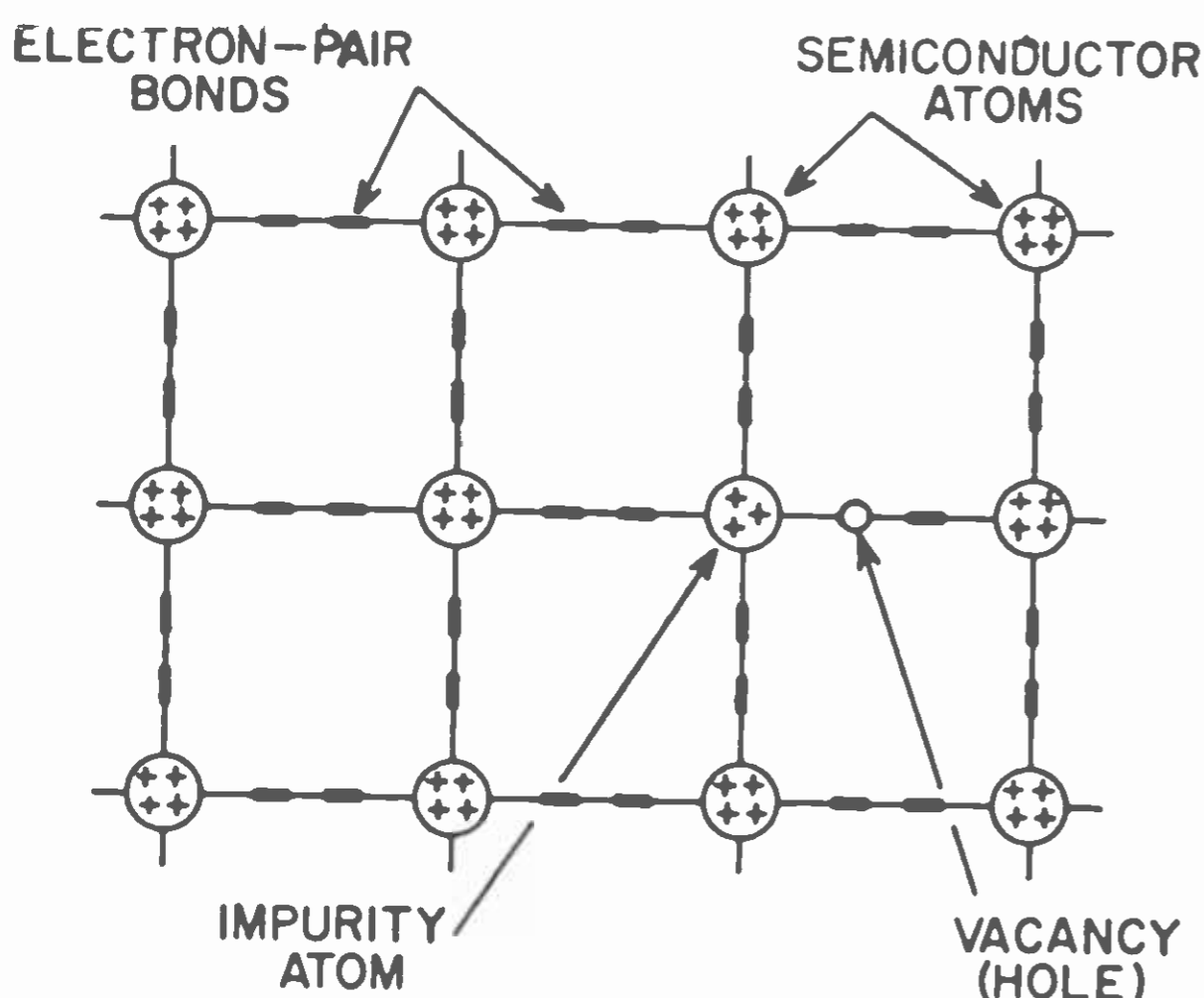


Fig. 4—Lattice structure of p-type material.

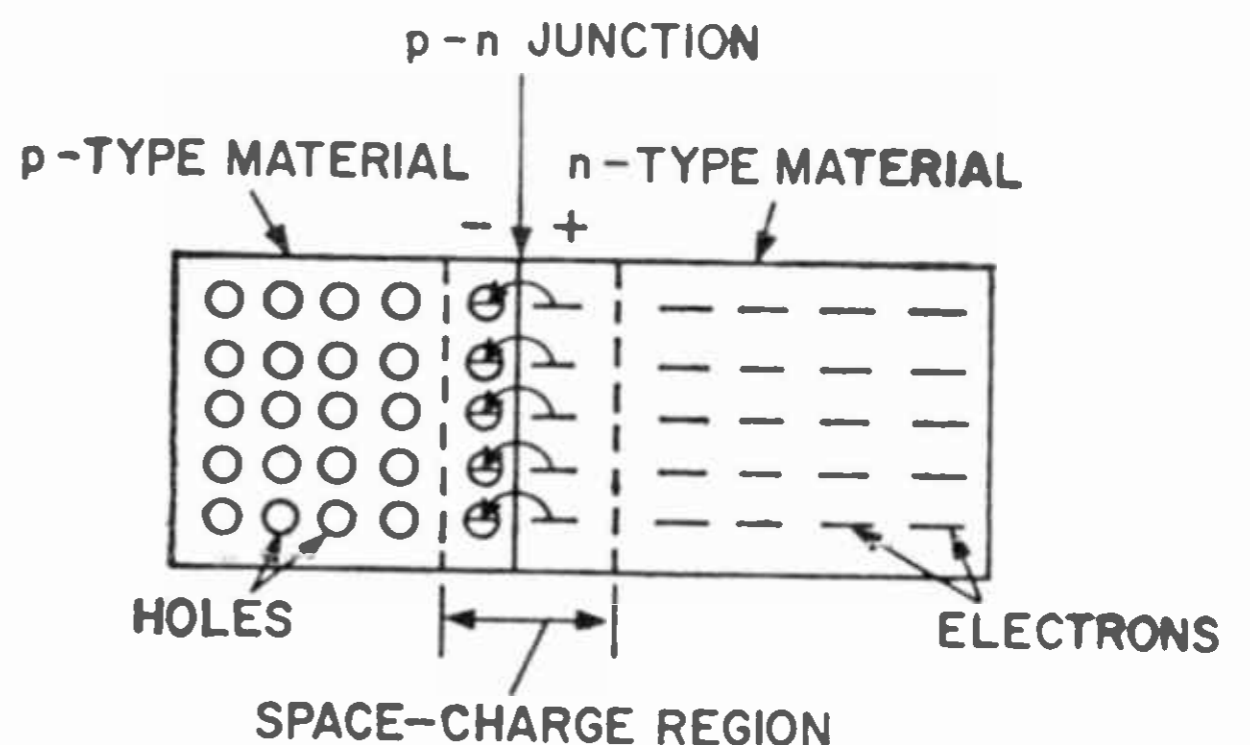


Fig. 5—Interaction of holes and electrons at p-n junction.

where the two materials meet (called the p-n junction). An interaction takes place between the two types of material at the junction as a result of the holes in one material and the excess electrons in the other.

When a p-n junction is formed, some of the free electrons from the n-type material diffuse across the junction and recombine with holes in

the lattice structure of the p-type material; similarly, some of the holes in the p-type material diffuse across the junction and recombine with free electrons in the lattice structure of the n-type material. This interaction or diffusion is brought into equilibrium by a small space-charge region (sometimes called the **transition region** or **depletion layer**). The p-type material thus acquires a slight negative charge and the n-type material acquires a slight positive charge.

Thermal energy causes charge carriers (electrons and holes) to diffuse from one side of the p-n junction to the other side; this flow of charge carriers is called **diffusion current**. As a result of the diffusion process, however, a potential gradient builds up across the space-charge region. This potential gradient can be represented, as shown in Fig. 6, by an imaginary battery connected across the p-n junction. (The battery symbol

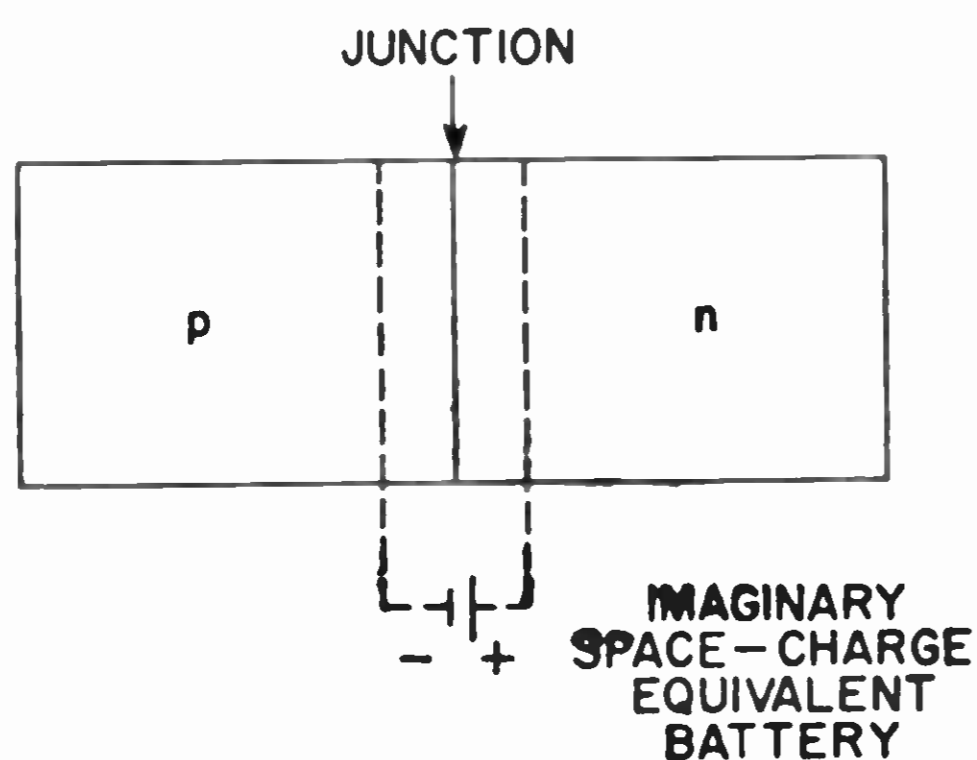


Fig. 6—Potential gradient across space-charge region.

is used merely to illustrate internal effects; the potential it represents is not directly measurable.) The potential gradient causes a flow

of charge carriers, referred to as **drift current**, in the opposite direction to the diffusion current. Under equilibrium conditions, the diffusion current is exactly balanced by the drift current so that the net current across the p-n junction is zero. In other words, when no external current or voltage is applied to the p-n junction, the potential gradient forms an **energy barrier** that prevents further diffusion of charge carriers across the junction. In effect, electrons from the n-type material that tend to diffuse across the junction are repelled by the slight negative charge induced in the p-type material by the potential gradient, and holes from the p-type material are repelled by the slight positive charge induced in the n-type material. The potential gradient (or energy barrier, as it is sometimes called), therefore, prevents total interaction between the two types of materials, and thus preserves the differences in their characteristics.

CURRENT FLOW

When an external battery is connected across a p-n junction, the amount of current flow is determined by the polarity of the applied voltage and its effect on the space-charge region. In Fig. 7(a), the positive terminal of the battery is connected to the n-type material and the negative terminal to the p-type material. In this arrangement, the free electrons in the n-type material are attracted toward the positive terminal of the battery and away from the junction. At the same time, holes from the

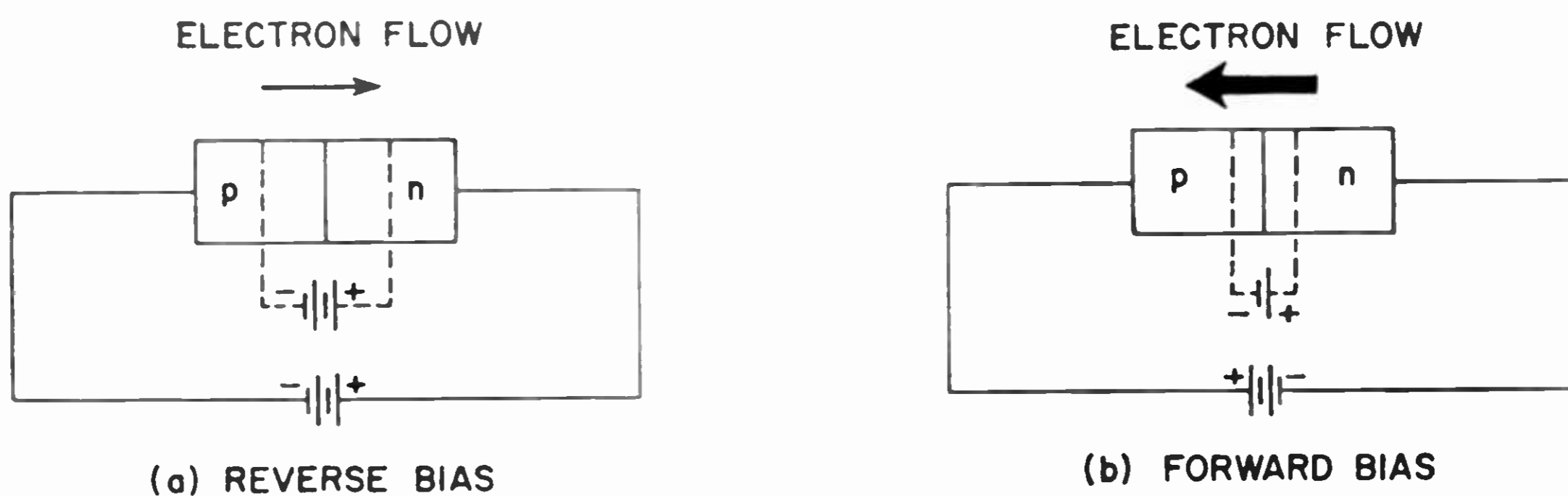


Fig. 7—Electron current flow in biased p-n junctions.

p-type material are attracted toward the negative terminal of the battery and away from the junction. As a result, the space-charge region at the junction becomes effectively wider, and the potential gradient increases until it approaches the potential of the external battery. Current flow is then extremely small because no voltage difference (electric field) exists across either the p-type or the n-type region. Under these conditions, the p-n junction is said to be reverse-biased.

In Fig. 7(b), the positive terminal of the external battery is connected to the p-type material and the negative terminal to the n-type material. In this arrangement, electrons in the p-type material near the positive terminal of the battery break their electron-pair bonds and enter the battery, creating new holes. At the same time, electrons from the negative terminal of the battery enter the n-type material and diffuse toward the junction. As a result, the space-charge region becomes effectively narrower, and the energy barrier decreases to an insignificant value. Excess electrons from the n-type material can then penetrate the space-charge region, flow across the junction, and move by way of the holes in the p-type material toward the positive terminal of the battery. This electron flow continues as long as the external voltage is applied. Under these conditions, the junction is said to be forward-biased.

The generalized voltage-current characteristic for a p-n junction in Fig. 8 shows both the reverse-bias and forward-bias regions. In the forward-bias region, current rises rapidly as the voltage is increased and is quite high. Current in the reverse-bias region is usually much lower. Excessive voltage (bias) in either direction should be avoided in normal applications because excessive currents and the resulting high temperatures may permanently damage the semiconductor device.

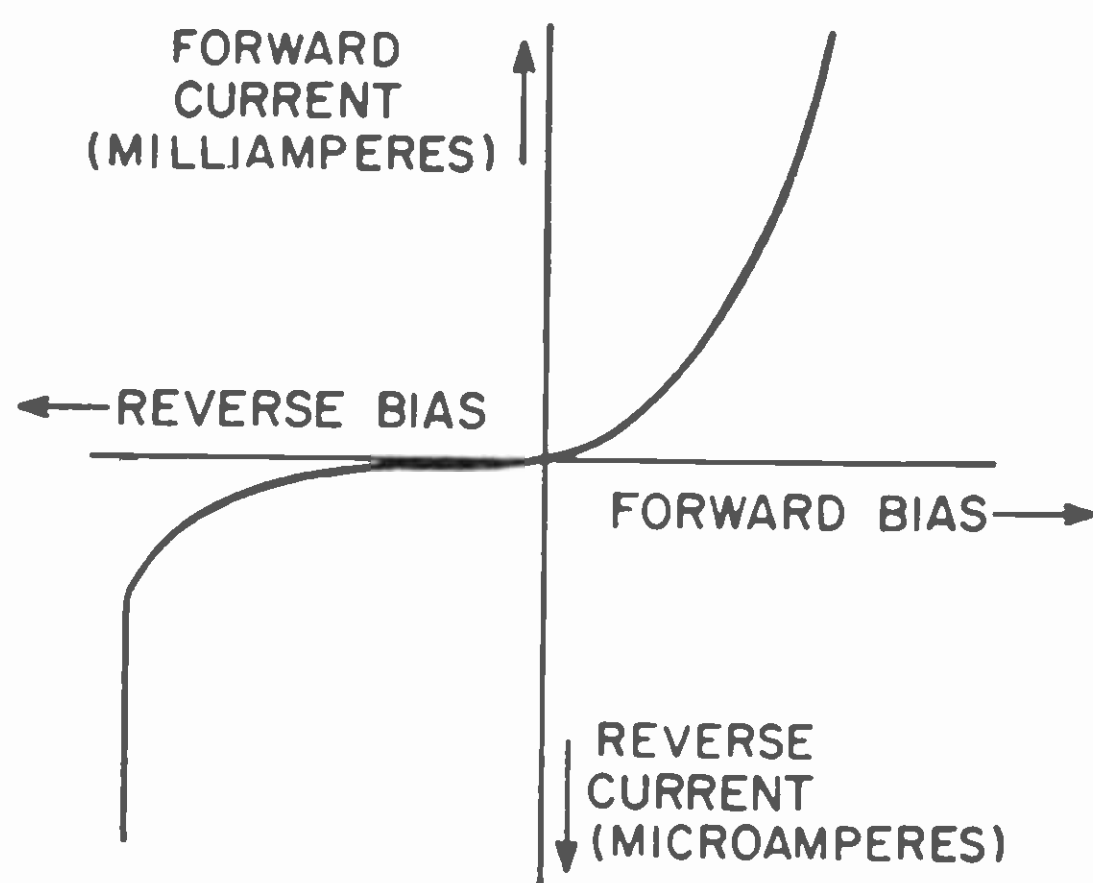


Fig. 8—Voltage-current characteristic for a p-n junction.

TYPES OF DEVICES

The simplest type of semiconductor device is the diode, which is represented by the symbol shown in Fig. 9. Structurally, the diode is basically a p-n junction similar to those shown in Fig. 7. The n-type material which serves as the negative electrode is referred to as the cathode, and the p-type material which serves as the positive electrode is referred to as the anode. The arrow symbol used for the anode represents the direction of "conventional current flow";

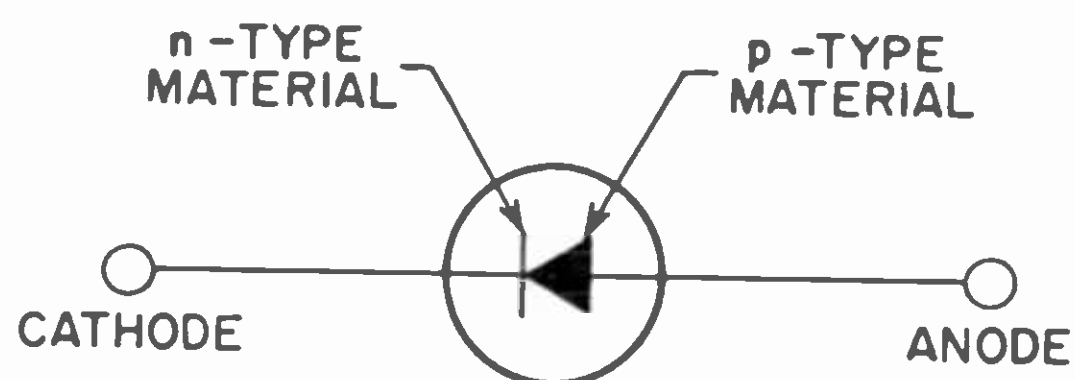


Fig. 9—Schematic symbol for a semiconductor diode.

electron current flows in a direction opposite to the arrow.

Because the junction diode conducts current more easily in one direction than in the other, it is an effective rectifying device. If an ac signal is applied, as shown in Fig. 10, electron current flows freely during the positive half cycle, but little or no current flows during the negative half cycle.

One of the most widely used types of semiconductor diode is the silicon rectifier. These devices are available in a wide range of current

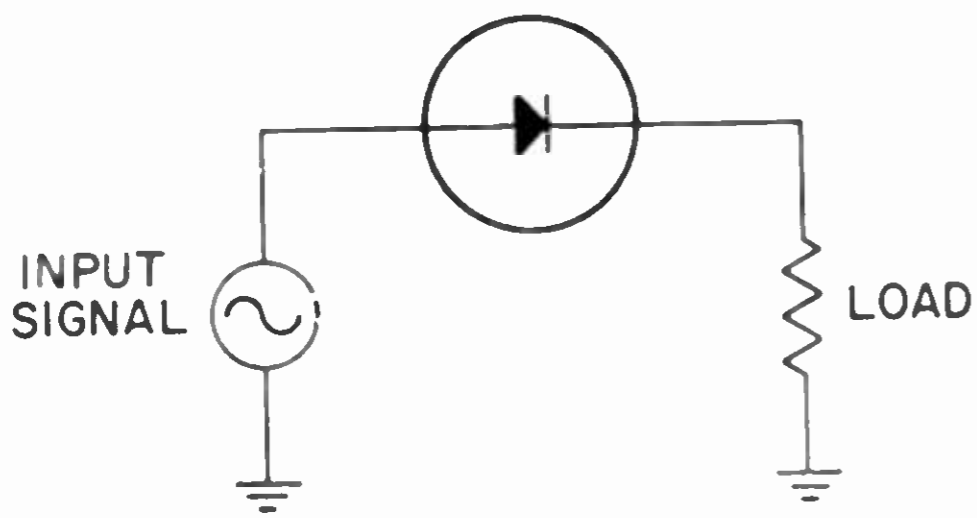


Fig. 10—Simple diode rectifying circuit.

capabilities, ranging from tenths of an ampere to several hundred amperes or more, and are capable of operation at voltages as high as 1000 volts or more. Parallel and series arrangements of silicon rectifiers permit even further extension of current and voltage limits. Characteristics and applications of these devices are discussed in detail in the section on **Silicon Rectifiers**.

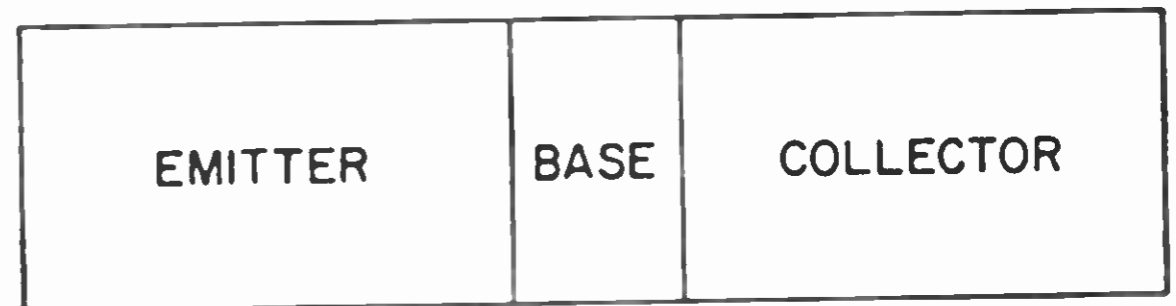
Several variations of the basic junction diode structure have been developed for use in special applications. One of the most important of these developments is the **tunnel diode**, which is used for amplification, switching, and pulse generation. This special diode is described in the section on **Other Semiconductor Diodes**.

When another layer is added to a semiconductor diode to form three layers (two junctions), a device is produced which provides power or voltage amplification. The resulting device is called a **bipolar transistor**. The three regions of the device are called the **emitter**, the **base**, and the **collector**, as shown in Fig. 11(a). In normal operation, the emitter-to-base junction is biased in the forward direction, and the collector-to-base junction in the reverse direction.

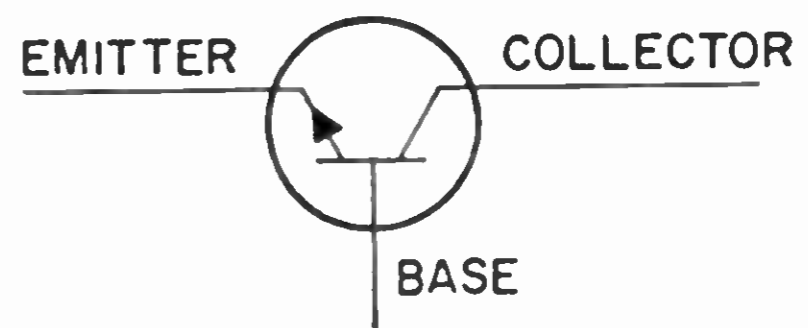
Different symbols are used for n-p-n and p-n-p transistors to show the difference in the direction of current flow in the two types of devices. In the n-p-n transistor shown in Fig. 11(b), electrons flow from the emitter to the collector. In the p-n-p transistor shown in Fig. 11(c), electrons flow from the collector to the emitter. In other words, the direction of dc electron current is always opposite to that of the arrow on the

emitter lead. (As in the case of semiconductor diodes, the arrow indicates the direction of "conventional current flow" in the circuit.)

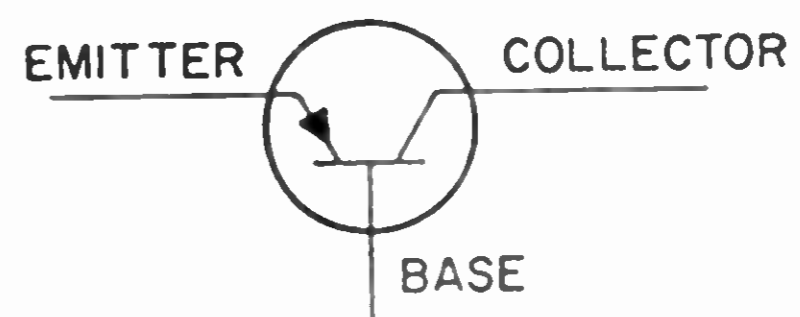
The first two letters of the n-p-n and p-n-p designations indicate the respective polarities of the voltages applied to the emitter and the collector in normal operation. In



(a) FUNCTIONAL DIAGRAM



(b) n-p-n TRANSISTOR



(c) p-n-p TRANSISTOR

Fig. 11—Functional diagram and schematic symbols for bipolar transistors.

an n-p-n transmitter the emitter is made negative with respect to both the collector and the base, and the collector is made positive with respect to both the emitter and the base. In a p-n-p transistor, the emitter is made positive with respect to both the collector and the base, and the collector is made negative with respect to both emitter and base.

The transistor, which is a three-element device, can be used for a wide variety of control functions, including amplification, oscillation, and frequency conversion. A complete description of the fabrication, electrical characteristics, and basic circuits of bipolar transistors is given in the section on **Bipolar Transistors**.

A relatively new type of transistor is called the **MOS field-effect transistor**. The structural diagrams of the enhancement type and the depletion type in Fig. 12 show the **gate**, **source**, and **drain** electrodes, which are equivalent to the base,

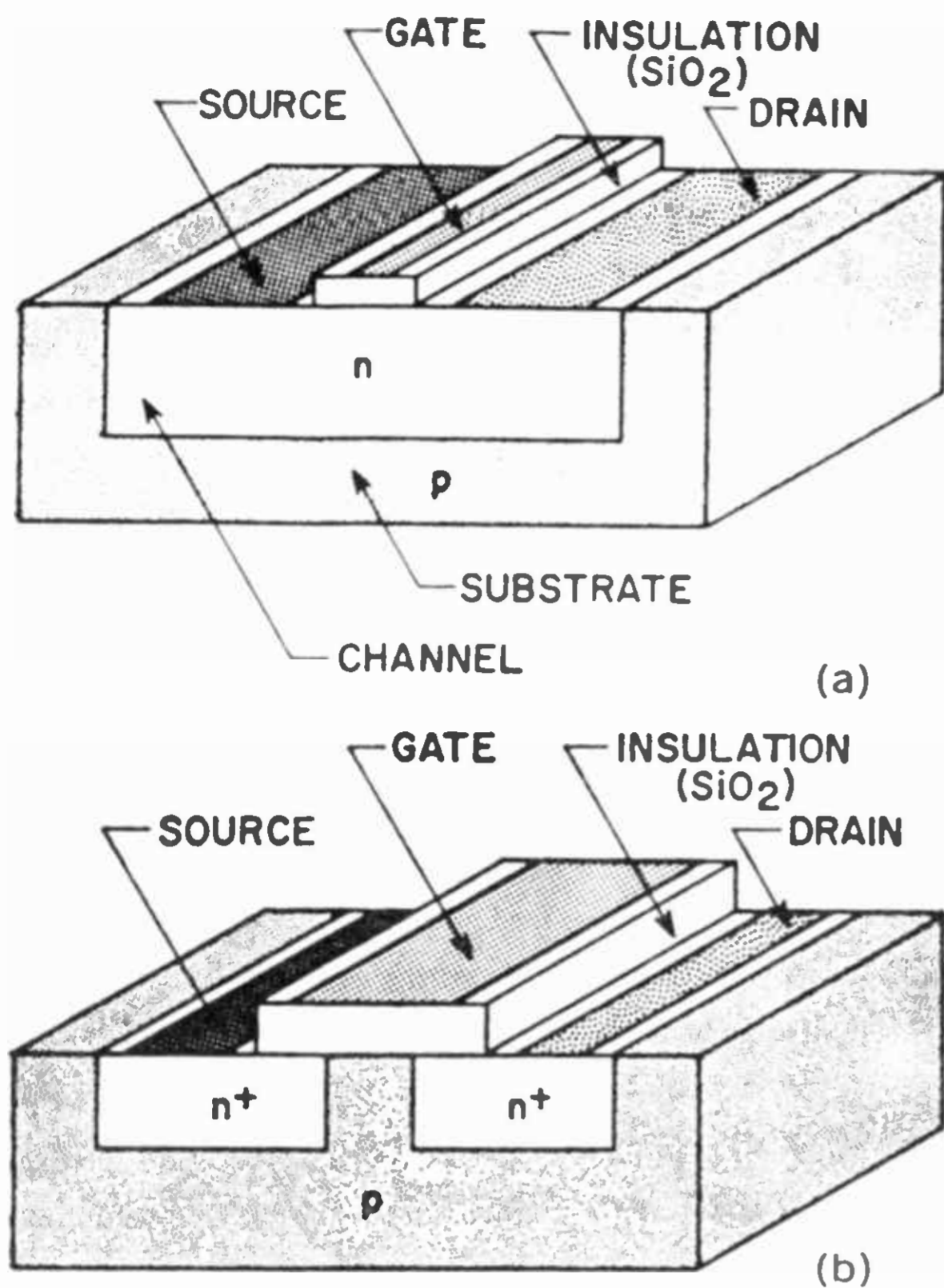


Fig. 12—MOS field-effect transistor structures: (a) depletion type, (b) enhancement type.

emitter, and collector electrodes, respectively, of a bipolar transistor. The signal voltage applied to the gate electrode is used to control the conductivity of the semiconductor layer immediately below the gate and between the source and drain layers. Because of their very high input impedance and square-law transfer characteristics, MOS transistors are especially suitable for use as voltage amplifiers. Fig. 13 shows the schematic symbols which indicate whether the transistor is

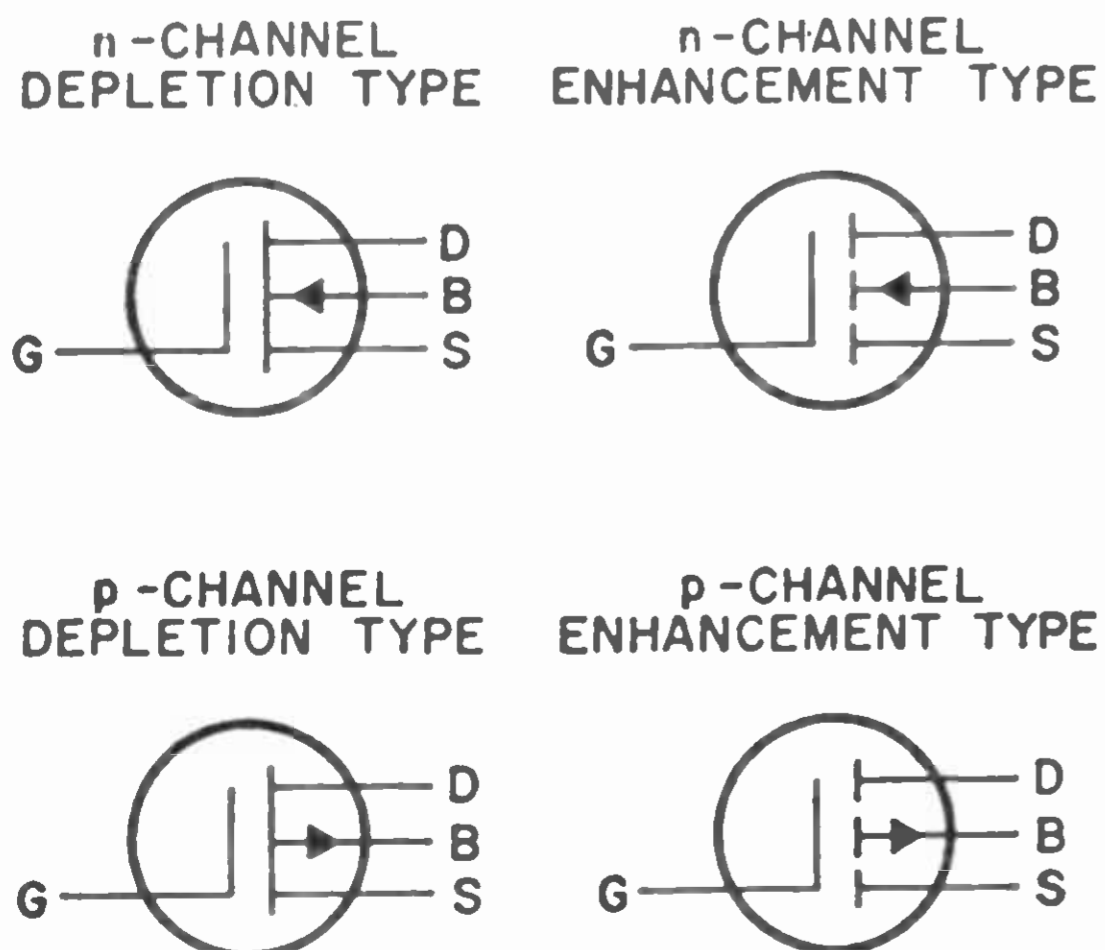


Fig. 13—Schematic symbols for MOS transistors (G = gate, D = drain, B = active bulk, S = source).

n-channel or p-channel, depletion-type or enhancement-type. A full description of these devices is given in the section on MOS Field-Effect Transistors.

When alternate layers of p-type and n-type semiconductor materials are arranged in a series array, various types of thyristors can be produced. The term thyristor is the generic name for semiconductor devices that have electrical characteristics similar to those of thyatron tubes. The three basic types of thyristors are the bidirectional trigger diode called the diac, the reverse blocking triode called the silicon controlled rectifier or SCR, and the bidirectional triode thyristor, called the triac. The diac, shown in Fig. 14, is a two-electrode, three-layer device having the same doping level at both junctions and a "floating" base. The device conducts current in

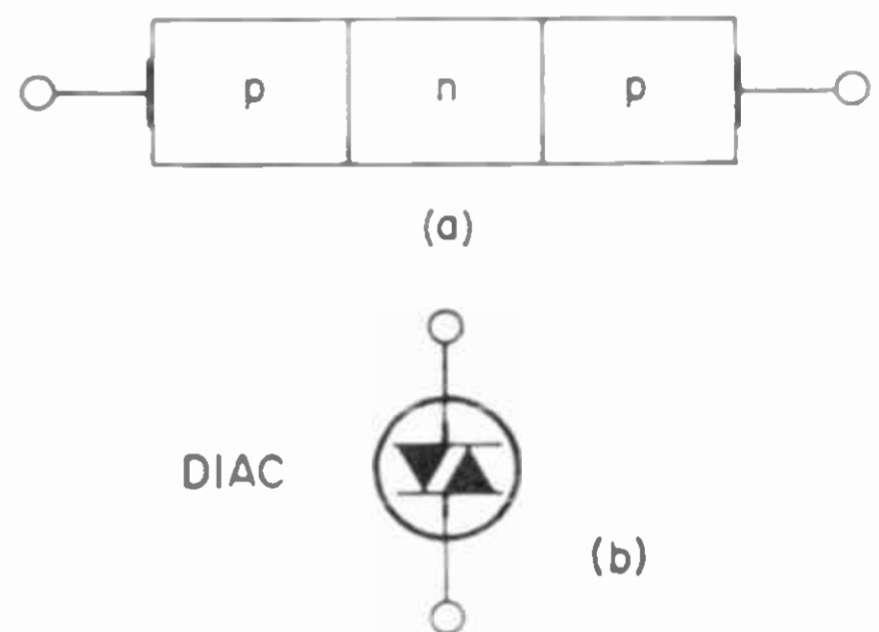


Fig. 14—Junction diagram (a) and schematic symbol (b) for a diac.

either direction after the applied voltage exceeds a certain value called the "breakover voltage." The SCR is a three-electrode, four-layer device, as shown in Fig. 15. The SCR behaves as a conventional rectifier to block current flow in the reverse direction and as a transistor switch in the forward direction to first block current and then conduct through the device when a current pulse of sufficient magnitude is applied to the gate electrode. The triac is a three-electrode, five-layer device, as shown in Fig. 16, which exhibits the forward-blocking—forward-conducting voltage-current characteristic of the SCR structure for either direction of voltage applied to the main terminals. The

schematic symbols for these thyristor devices are also shown in Figs. 14, 15, and 16. A complete descrip-

tion of these devices is given in the section on Thyristors.

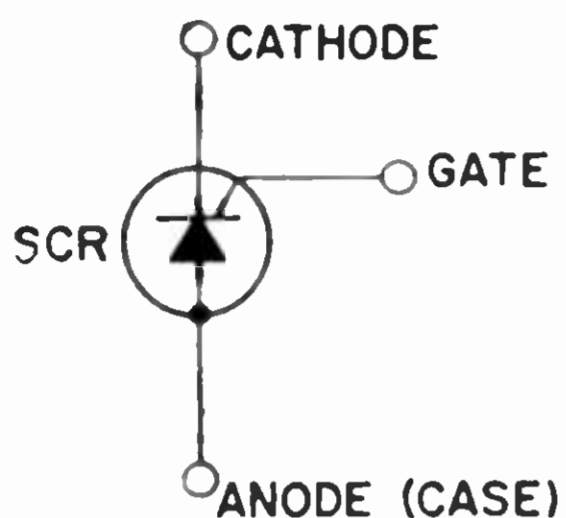
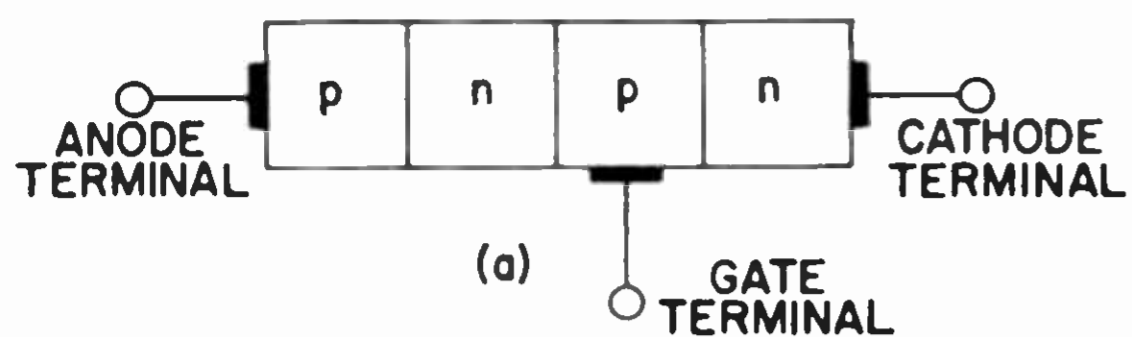


Fig. 15—Junction diagram (a) and schematic symbol (b) for a silicon controlled rectifier or SCR.

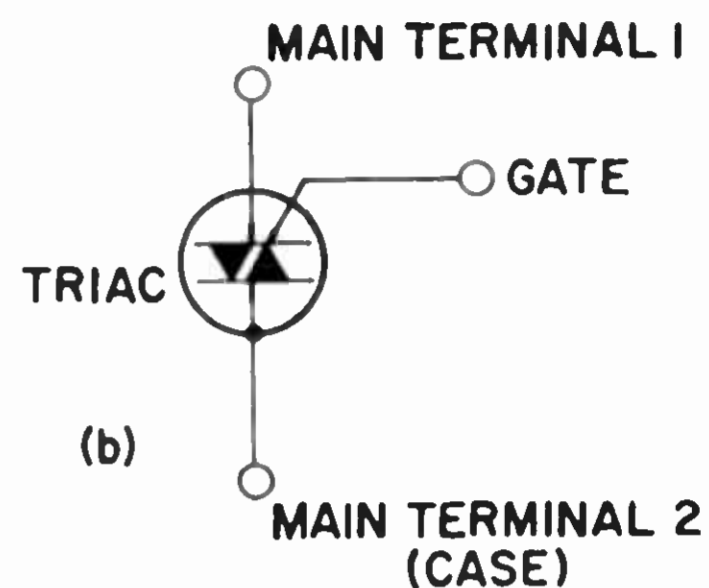
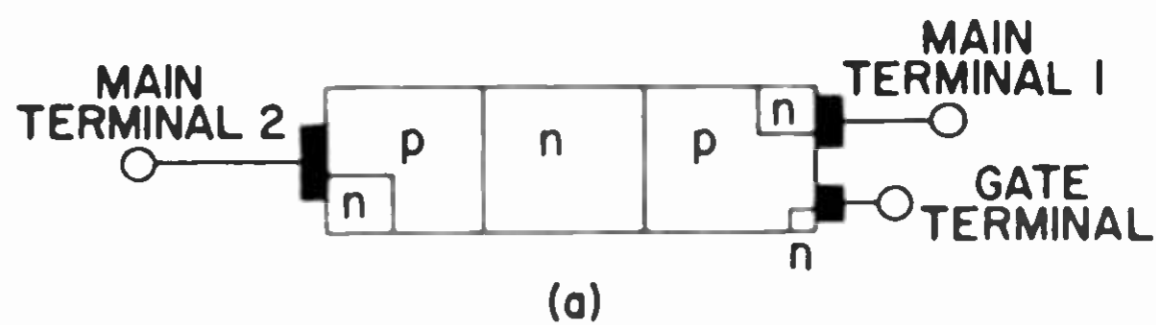


Fig. 16—Junction diagram (a) and schematic symbol (b) for a triac.

Bipolar Transistors

A p-n junction biased in the reverse direction is equivalent to a high-resistance element (low current for a given applied voltage), while a junction biased in the forward direction is equivalent to a low-resistance element (high current for a given applied voltage). Because the power developed by a given current is greater in a high-resistance element than in a low-resistance element ($P = I^2R$), power gain can be obtained in a structure containing two such resistance elements if the current flow is not materially reduced. A device containing two p-n junctions biased in opposite directions is called a junction or bipolar transistor.

Such a two-junction device is shown in Fig. 17. The thick end layers are made of the same type of material (n-type in this case), and are separated by a very thin layer of the opposite type of material (p-type in the device shown). By means of the

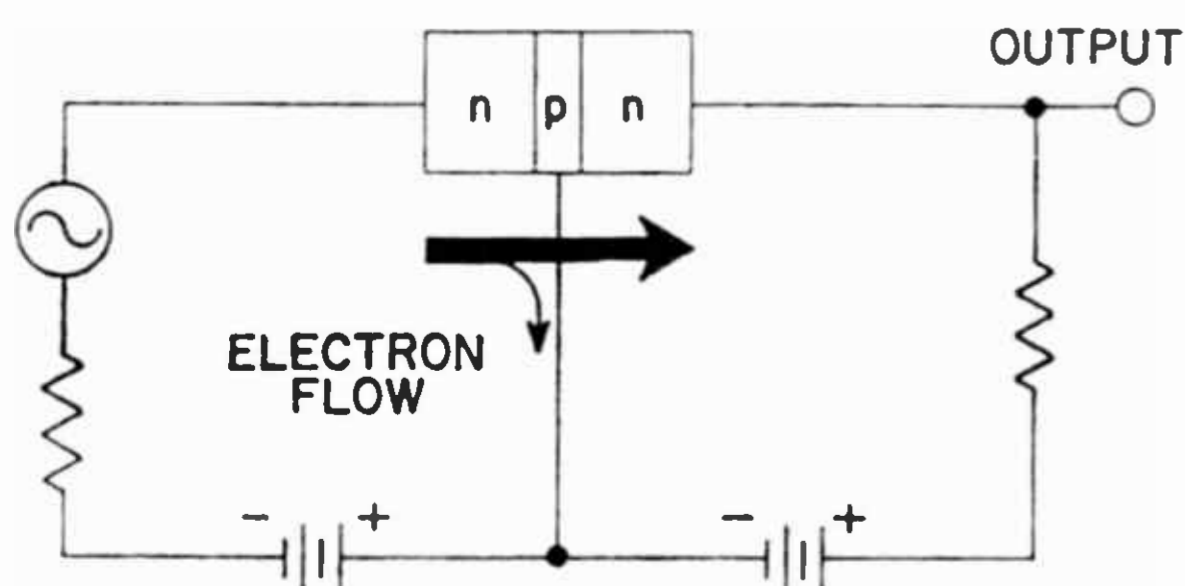


Fig. 17—An n-p-n structure biased for power gain.

external batteries, the left-hand (n-p) junction is biased in the forward

direction to provide a low-resistance input circuit, and the right-hand (p-n) junction is biased in the reverse direction to provide a high-resistance output circuit.

Electrons flow easily from the left-hand n-type region to the center p-type region as a result of the forward biasing. Most of these electrons diffuse through the thin p-type region, however, and are attracted by the positive potential of the external battery across the right-hand junction. In practical devices, approximately 95 to 99.5 per cent of the electron current reaches the right-hand n-type region. This high percentage of current penetration provides power gain in the high-resistance output circuit and is the basis for transistor amplification capability.

The operation of p-n-p devices is similar to that shown for the n-p-n device, except that the bias-voltage polarities are reversed, and electron-current flow is in the opposite direction. (Many discussions of semiconductor theory assume that the “holes” in semiconductor material constitute the charge carriers in p-n-p devices, and discuss “hole currents” for these devices and “electron currents” for n-p-n devices. Other texts discuss neither hole current nor electron current, but rather “conventional current flow”, which is assumed to travel through a circuit in a direction from the positive terminal of the external battery back to its negative terminal. For the sake of simplicity, this dis-

cussion will be restricted to the concept of electron current flow, which travels from a negative to a positive terminal.)

DESIGN AND FABRICATION

The ultimate aim of all transistor fabrication techniques is the construction of two parallel p-n junctions with controlled spacing between the junctions and controlled impurity levels on both sides of each junction. A variety of structures has been developed in the course of transistor evolution.

The earliest transistors made were of the point-contact type. In this type of structure, two pointed wires were placed next to each other on an n-type block of semiconductor material. The p-n junctions were formed by electrical pulsing of the wires. This type has been superseded by junction transistors, which are fabricated by various alloy, diffusion, and crystal-growth techniques.

In grown-junction transistors, the impurity content of the semiconductor material is changed during the growth of the original crystal ingot to provide the p-n-p or n-p-n regions. The grown crystal is then sliced into a large number of small-area devices, and contacts are made to each region of the devices. Fig. 18(a) shows a cross-section of a grown-junction transistor.

In alloy-junction transistors, two small "dots" of a p-type or n-type impurity element are placed on opposite sides of a thin wafer of n-type or p-type semiconductor material, respectively, as shown in Fig. 18(b). After proper heating, the impurity "dots" alloy with the semiconductor material to form the regions for the emitter and collector junctions. The base connection in this structure is made to the original semiconductor wafer.

The drift-field transistor is a modified alloy-junction device in which the impurity concentration in the base wafer is diffused or graded, as

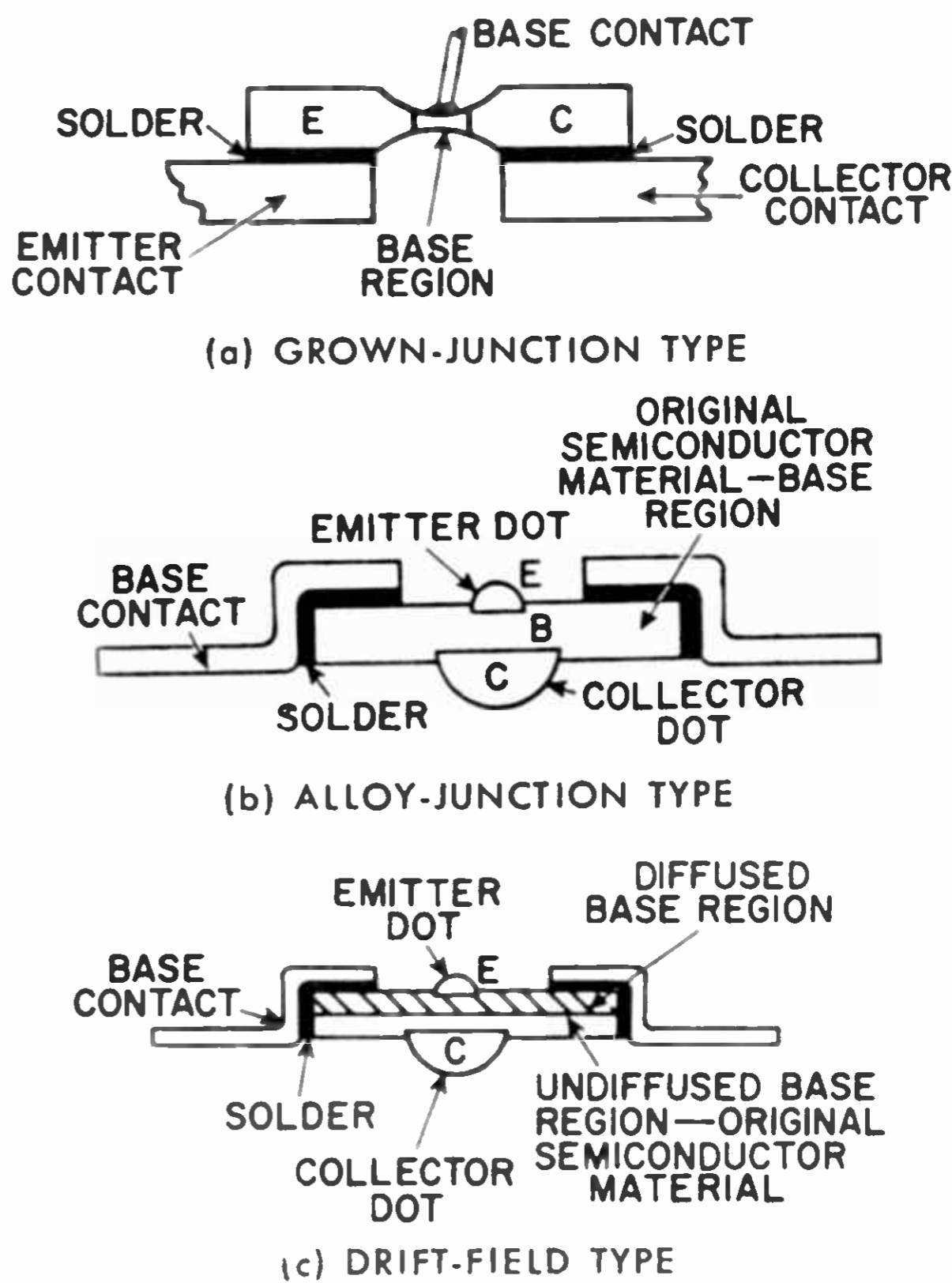


Fig. 18—Cross-sections of junction transistors.

shown in Fig. 18(c). Two advantages are derived from this structure: (a) the resultant built-in voltage or "drift field" speeds current flow, and (b) the ability to use a heavy impurity concentration in the vicinity of the emitter and a light concentration in the vicinity of the collector makes it possible to minimize capacitive charging times. Both these advantages lead to a substantial extension of the frequency performance over the alloy-junction device.

The **diffused-junction** transistor represents a major advance in transistor technology because increased control over junction spacings and impurity levels makes possible significant improvements in transistor performance capabilities. A cross-section of a **single-diffused** "hometaxial" structure is shown in Fig. 19(a). Hometaxial transistors are fabricated by simultaneous diffusion of impurity from each side of a homogeneously doped base wafer. A mesa or flat-topped peak is etched on one side of the wafer in an intricate design to define the transistor emitter

and expose the base region for connection of metal contacts. Large amounts of heat can be dissipated from a homotaxial structure through the highly conductive solder joint between the semiconductor material and the device package. This structure provides a very low collector resistance.

Double-diffused transistors have an additional degree of freedom for selection of the impurity levels and junction spacings of the base, emitter, and collector. This structure provides high voltage capability through a lightly doped collector region without compromise of the junction spacings which determine device frequency response and other important characteristics. Fig. 19(b) shows a typical double-diffused transistor; the emitter and base junctions are diffused into the same side of the original semiconductor wafer, which serves as the collector. A mesa is usually etched through the base region to reduce the collector area at the base-to-collector junction and to provide a stable semiconductor surface.

Double-diffused planar transistors provide the added advantage of protection or passivation of the emitter-to-base and collector-to-base junction surfaces. Fig. 19(c) shows a typical double-diffused planar transistor. The base and emitter regions terminate

at the top surface of the semiconductor wafer under the protection of an insulating layer. Photolithographic and masking techniques are used to provide for diffusion of both base and emitter impurities in selective areas of the semiconductor wafer.

In triple-diffused transistors, a heavily doped region diffused from the bottom of the semiconductor wafer effectively reduces the thickness of the lightly doped collector region to a value dictated only by electric-field considerations. Thus, the thickness of the lightly doped or high-resistivity portion of the collector is minimized to obtain a low collector resistance. A section of a triple-diffused planar structure is shown in Fig. 19(d).

Epitaxial transistors differ from diffused structures in the manner in which the various regions are fabricated. Epitaxial structures are grown on top of a semiconductor wafer in a high-temperature reaction chamber. The growth proceeds atom by atom, and is a perfect extension of the crystal lattice of the wafer on which it is grown. In the epitaxial-base transistor shown in Fig. 20(a) a lightly doped base region is deposited by epitaxial techniques on a heavily doped collector wafer of opposite-type dopant. Photolithographic and masking techniques and

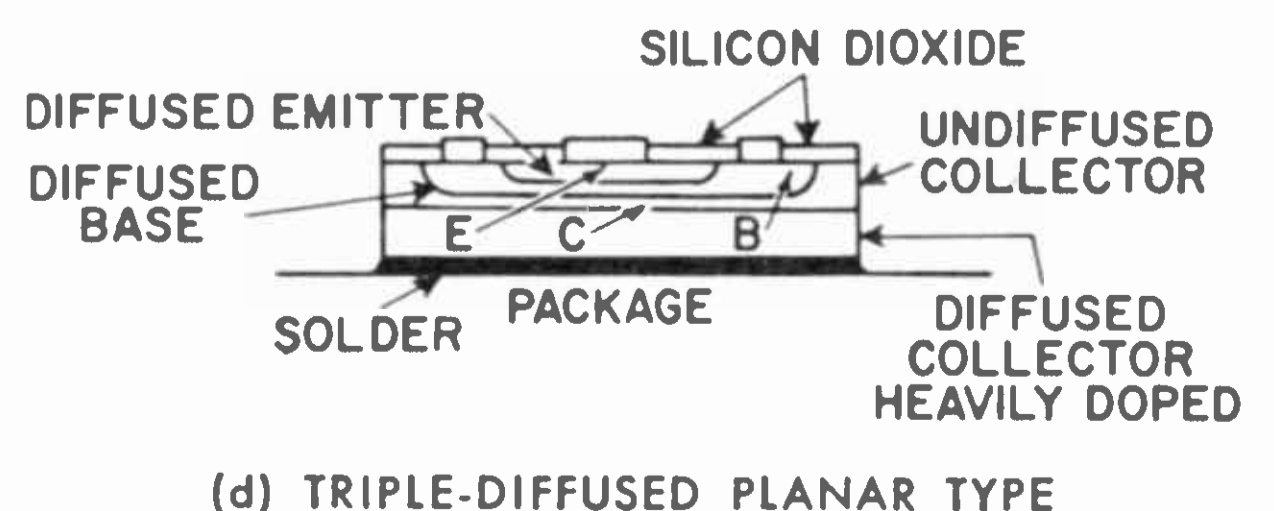
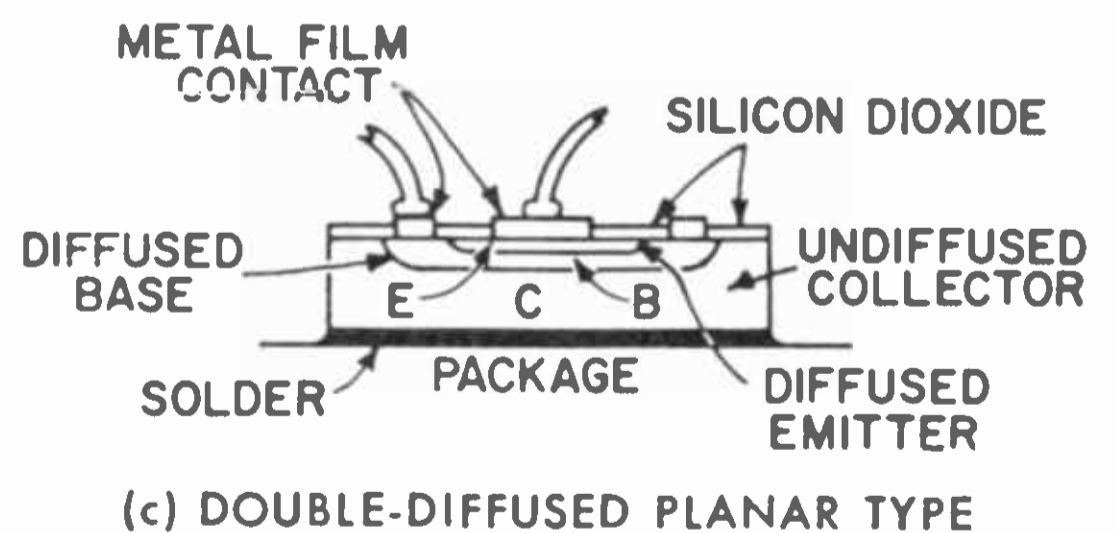
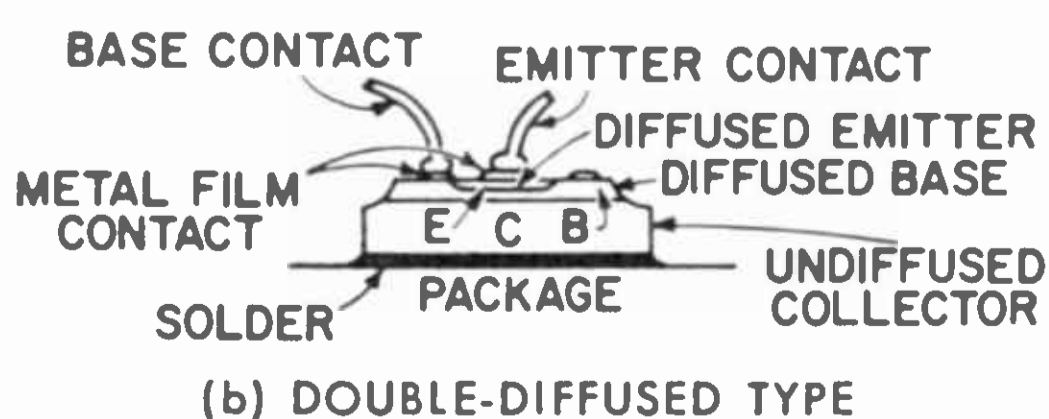
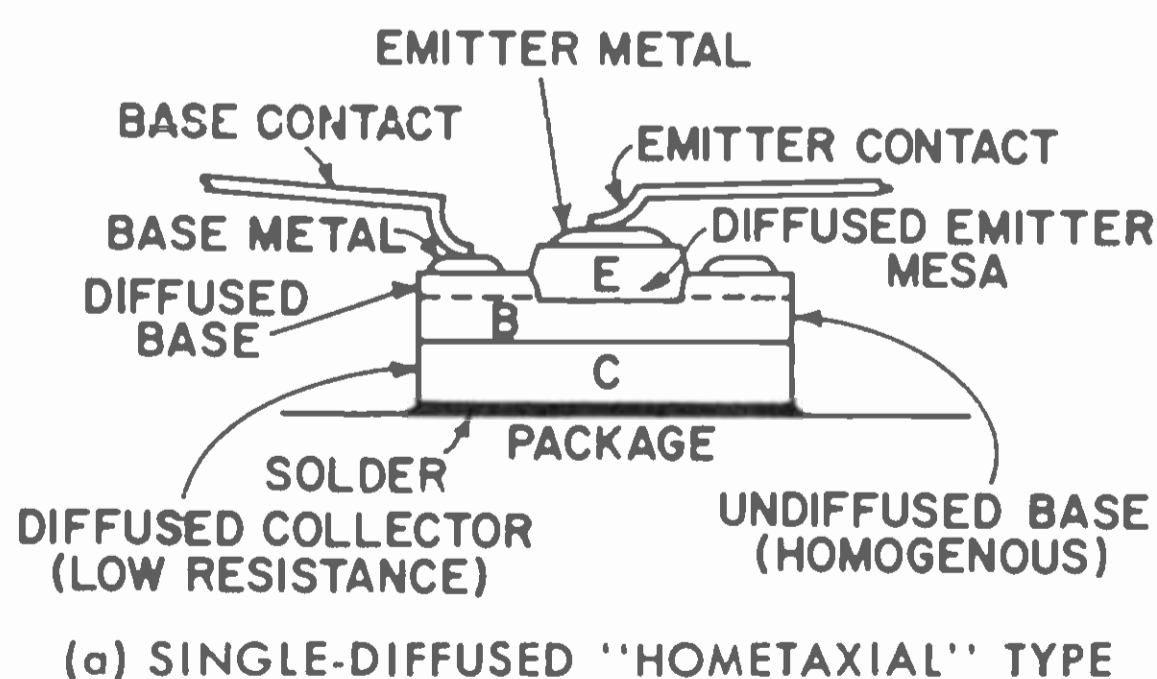


Fig. 19—Cross-sections of diffused transistors.

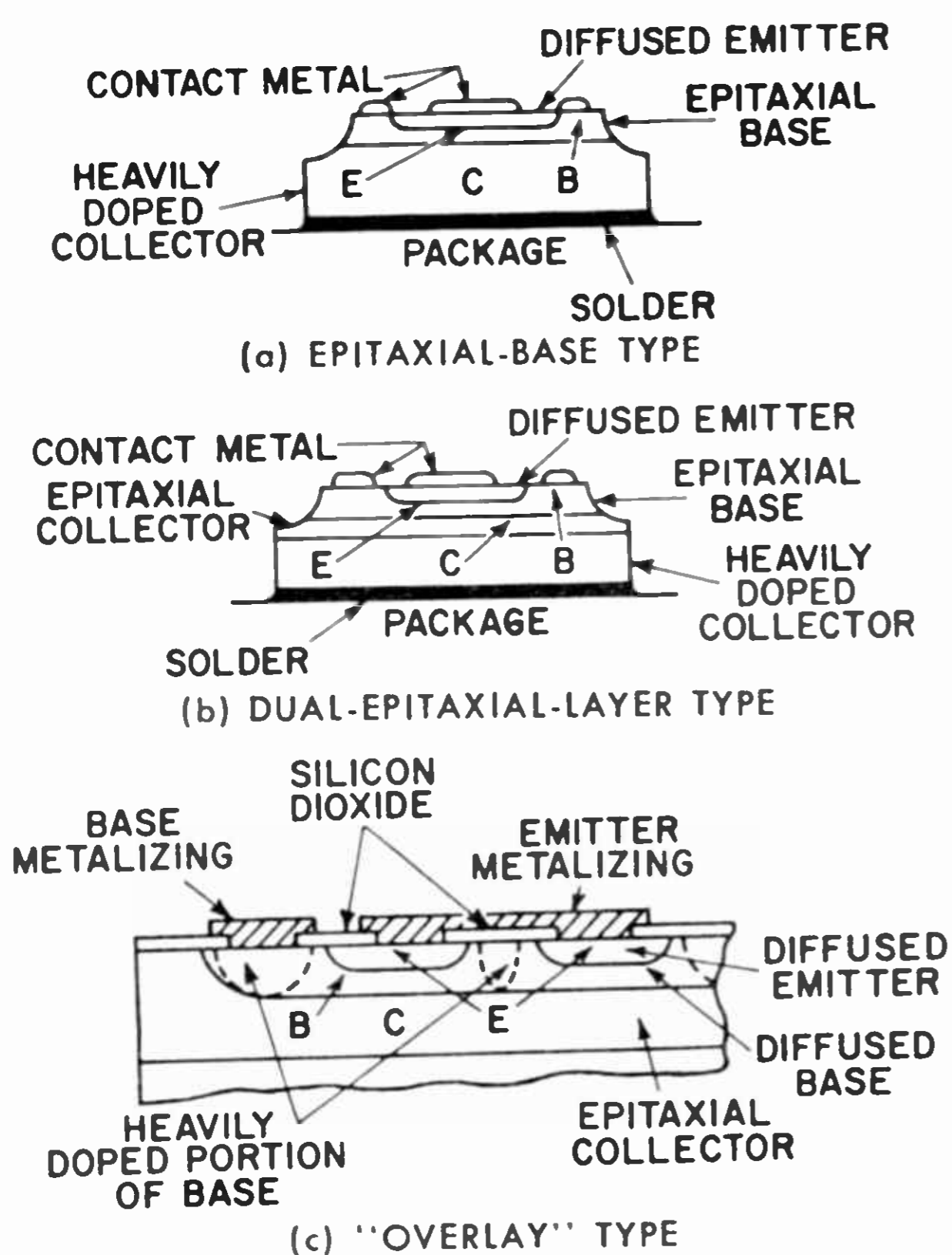


Fig. 20—Cross-sections of epitaxial transistors.

a single impurity diffusion are used to define the emitter region. This structure offers the advantages of low collector resistance and easy control of impurity spacings and emitter geometry. A variation of this structure uses two epitaxial layers. A thin lightly doped epitaxial layer used for the collector is deposited over the original heavily doped semiconductor wafer prior to the epitaxial deposition of the base region. The collector epitaxial layer is of opposite-type dopant to the epitaxial base layer. This structure, shown in Fig. 20(b), has the added advantage of higher voltage ratings provided by the epitaxial collector layer.

The **overlay** transistor is a double-diffused epitaxial device which employs a unique emitter structure. A large number of separate emitters are tied together by diffused and metalized regions to increase the emitter edge-to-area ratio and reduce the charging-time constants of the transistor without compromise of current- and power-handling capability. Fig. 20(c) shows a section

through a typical overlay emitter region.

After fabrication, individual transistor chips are mechanically separated and mounted on individual headers. Connector wires are then bonded to the metalized regions, and each unit is encased in plastic or a hermetically sealed enclosure. In power transistors, the wafer is usually soldered or alloyed to a solid metal header to provide for high thermal conductivity and low-resistance collector contacts, and low-resistance contacts are soldered or metal-bonded from the emitter or base metalizing contacts to the appropriate package leads. This packaging concept results in a simple structure that can be readily attached to a variety of circuit heat sinks and can safely withstand power dissipations of hundreds of watts and currents of tens of amperes.

BASIC CIRCUITS

Bipolar transistors are ideal current amplifiers. When a small signal current is applied to the input terminals of a bipolar transistor, an amplified reproduction of this signal appears at the output terminals. Although there are six possible ways of connecting the input signal, only three useful circuit configurations exist for current or power amplification: common-base, common-emitter, and common-collector. In the **common-base** (or ground-base) connection shown in Fig. 21, the signal is introduced into the emitter-base circuit and extracted from the collector-base circuit. (Thus the base element of the transistor is common to both the input and output circuits). Because the input or emitter-base circuit has a low impedance (resistance plus reactance) in the order of 0.5 to 50 ohms, and the output or collector-base circuit has a high impedance in the order of 1000 ohms to one megohm, the voltage or power gain in this type of configuration may be in the order of 1500.

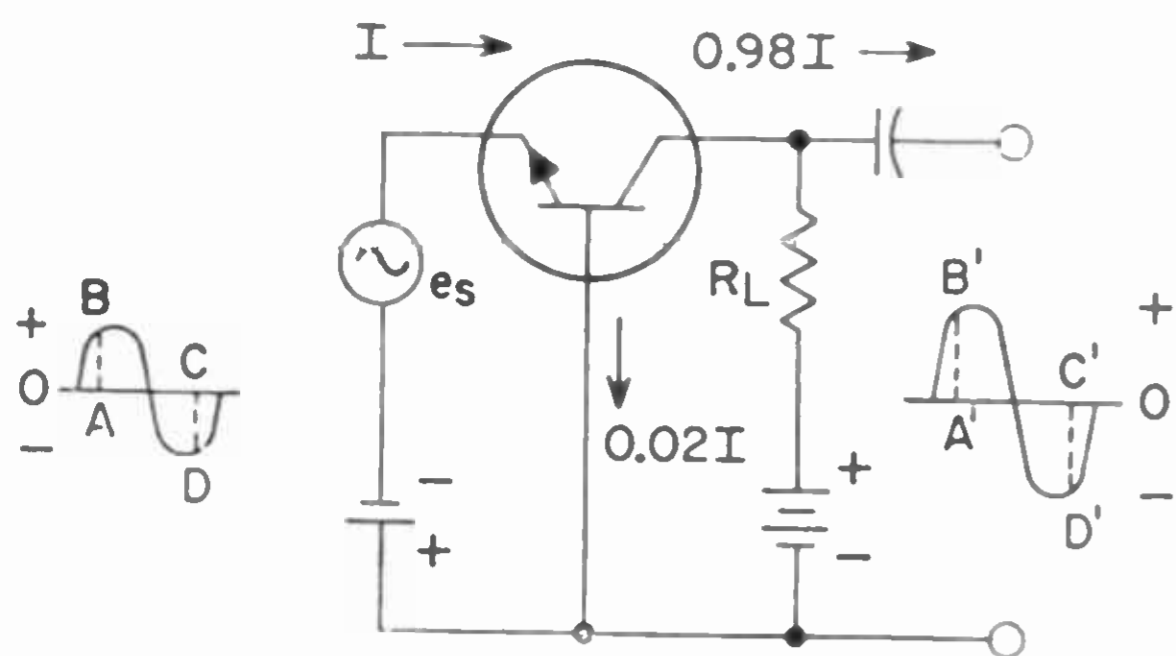


Fig. 21—Common-base circuit configuration.

The direction of the arrows in Fig. 17 indicates electron current flow. As stated previously, most of the current from the emitter flows to the collector; the remainder flows through the base. In practical transistors, from 95 to 99.5 per cent of the emitter current reaches the collector. The current gain of this configuration, therefore, is always less than unity, usually in the order of 0.95 to 0.995.

The waveforms in Fig. 21 represent the input voltage produced by the signal generator e_s and the output voltage developed across the load resistor R_L . When the input voltage is positive, as shown at AB, it opposes the forward bias produced by the base-emitter battery, and thus reduces current flow through the n-p-n transistor. The reduced electron current flow through R_L then causes the top point of the resistor to become less negative (or more positive) with respect to the lower point, as shown at A'B' on the output waveform. Conversely, when the input signal is negative, as at CD, the output signal is also negative, as at C'D'. Thus, the phase of the signal remains unchanged in this circuit, i.e., there is no voltage phase reversal between the input and the output of a common-base amplifier.

In the common-emitter (or grounded-emitter) connection shown in Fig. 22 the signal is introduced into the base-emitter circuit and extracted from the collector-emitter circuit. This configuration has more moderate input and output impedances than the common-base circuit. The input (base-emitter) impedance

is in the range of 20 to 5000 ohms, and the output (collector-emitter) impedance is about 50 to 50,000 ohms. Power gains in the order of 10,000 (or approximately 40 dB) can be realized with this circuit because it provides both current gain and voltage gain.

Current gain in the common-emitter configuration is measured between the base and the collector, rather than between the emitter and the collector as in the common-base circuit. Because a very small change in base current produces a relatively large change in collector current, the current gain is always greater than unity in a common-emitter circuit; a typical value is about 50.

The input signal voltage undergoes a phase reversal of 180 degrees in a common-emitter amplifier, as shown by the waveforms in Fig. 22.

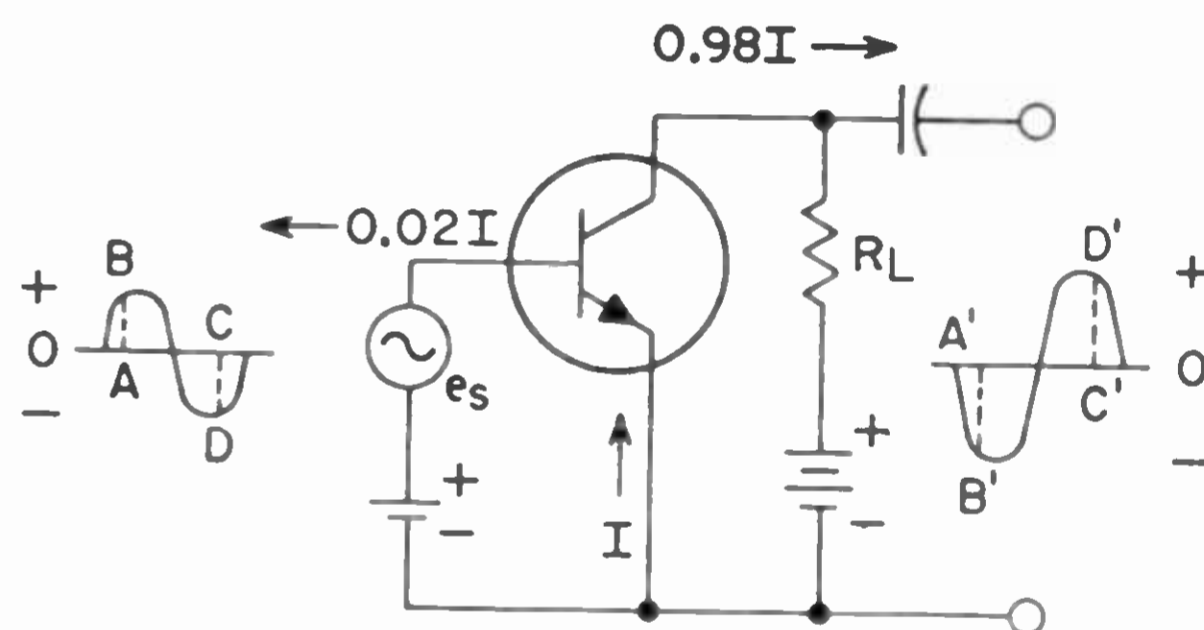


Fig. 22—Common-emitter circuit configuration.

When the input voltage is positive, as shown at AB, it increases the forward bias across the base-emitter junction, and thus increases the total current flow through the transistor. The increased electron flow through R_L then causes the output voltage to become negative, as shown at A'B'. During the second half-cycle of the waveform, the process is reversed, i.e., when the input signal is negative, the output signal is positive (as shown at CD and C'D').

The third type of connection, shown in Fig. 23, is the common-collector (or grounded-collector) circuit. In this configuration, the signal is introduced into the base-collector circuit and extracted from the emitter-collector circuit. Because the input

impedance of the transistor is high and the output impedance low in this connection, the voltage gain is less than unity and the power gain is usually lower than that obtained in either a common-base or a common-emitter circuit. The common-collector circuit is used primarily as

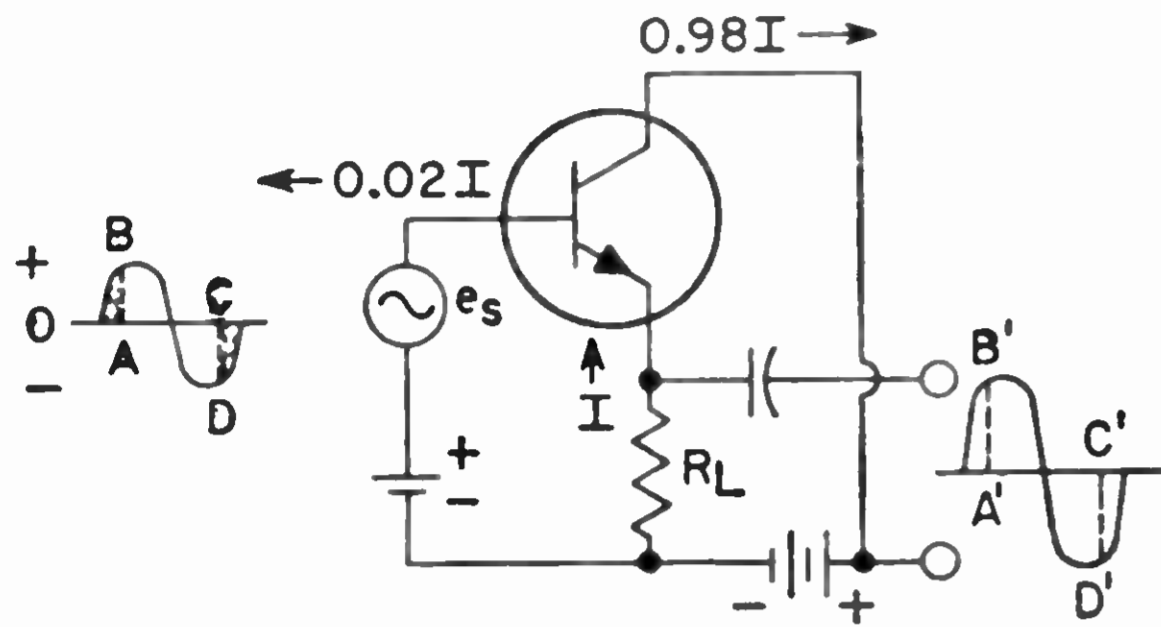


Fig. 23—Common-collector circuit configuration.

an impedance-matching device. As in the case of the common-base circuit, there is no phase reversal of the signal between the input and the output.

The circuits shown in Figs. 21 through 23 are biased for n-p-n transistors. When p-n-p transistors are used, the polarities of the batteries must be reversed. The voltage phase relationships, however, remain the same.

CHARACTERISTICS

THE term "characteristic" is used to identify the distinguishing electrical features and values of a transistor. These values may be shown in curve form or they may be tabulated. When the characteristics values are given in curve form, the curves may be used for the determination of transistor performance and the calculation of additional transistor parameters.

Characteristics values are obtained from electrical measurements of transistors in various circuits under certain definite conditions of current and voltage. **Static** characteristics are obtained with dc potentials applied to the transistor electrodes. **Dynamic** characteristics are obtained with an ac voltage on one electrode under various conditions of dc potentials

on all the electrodes. The dynamic characteristics, therefore, are indicative of the performance capabilities of the transistor under actual working conditions.

Published data for transistors include both electrode characteristic curves and transfer characteristic curves. These curves present the same information, but in two different forms to provide more useful data. Because transistors are used most often in the common-emitter configuration, characteristic curves are usually shown for the collector or output electrode. The **collector-characteristic curve** is obtained by varying collector-to-emitter voltage and measuring collector current for different values of base current. The **transfer-characteristic curve** is obtained by varying the base-to-emitter (bias) voltage or current at a specified or constant collector voltage, and measuring collector current. A collector-characteristic family of curves is shown in Fig. 24. Fig. 25 shows transfer-characteristic curves for the same transistor.

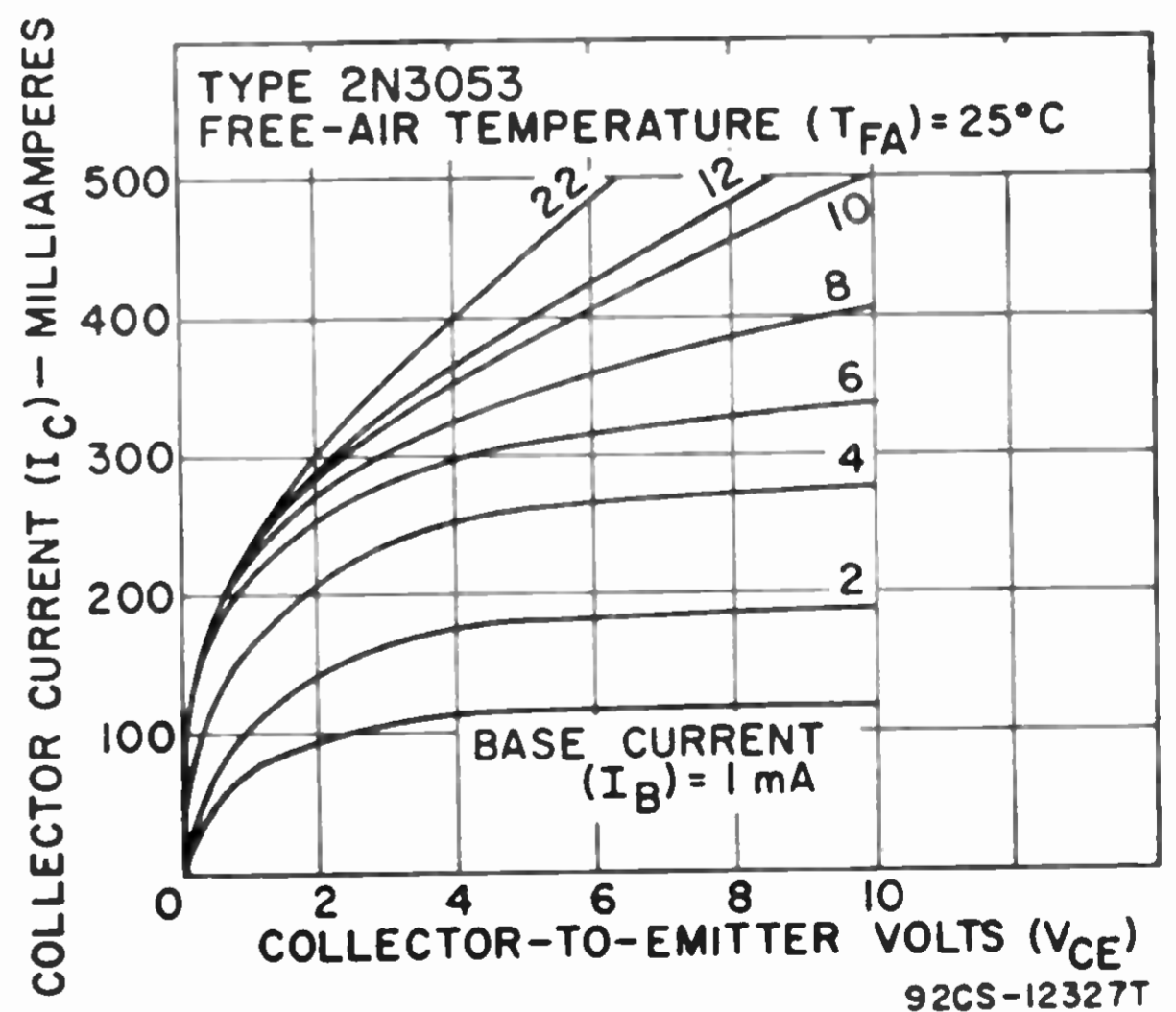


Fig. 24—Collector-characteristic curves.

A measure of the current gain of a transistor is its **forward current-transfer ratio**, i.e., the ratio of the current in the output electrode to the current in the input electrode. Because of the different ways in which transistors may be connected in circuits, the forward current-transfer ratio is specified for a

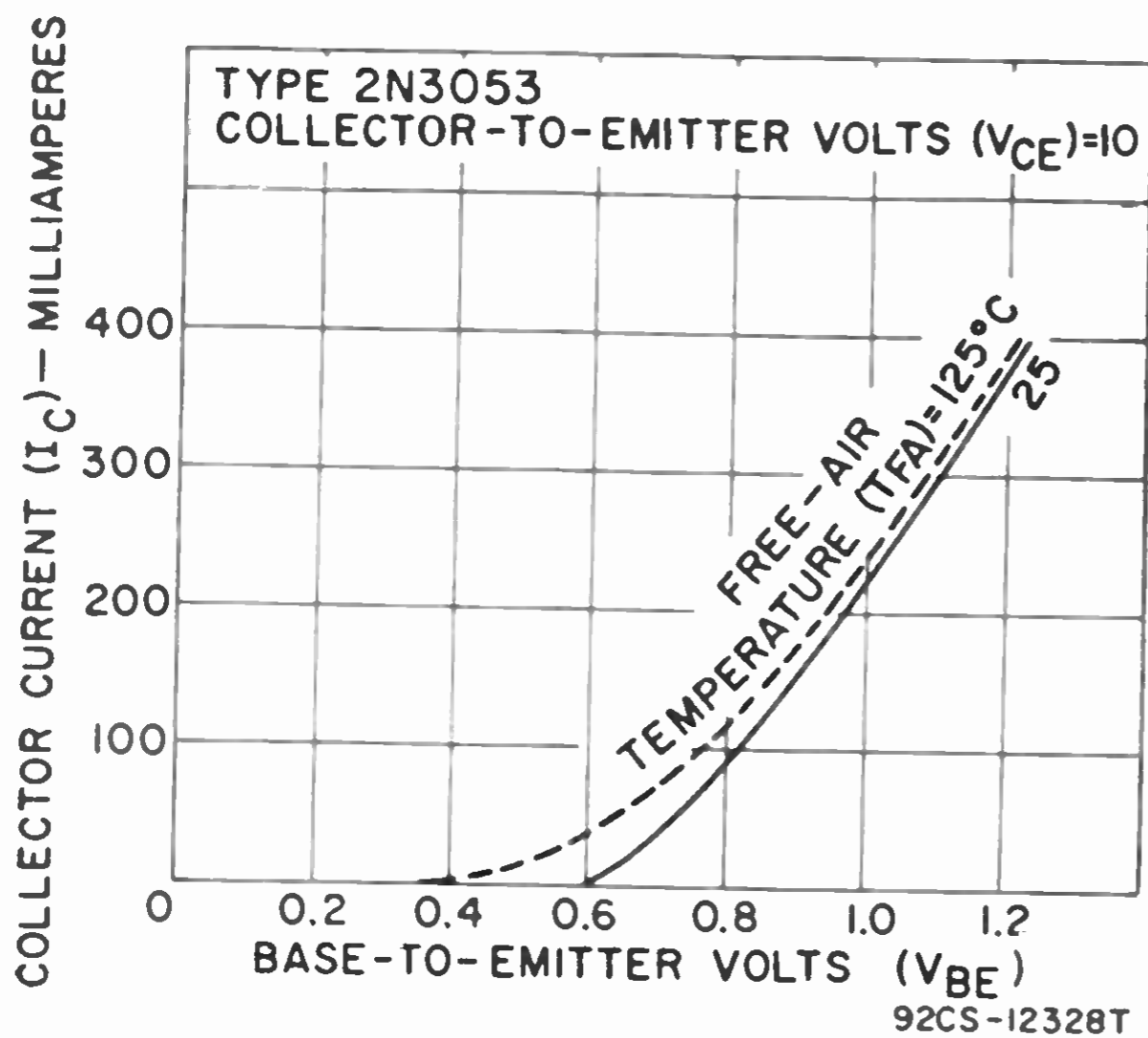


Fig. 25—Transfer-characteristic curves.

particular circuit configuration. The common-base forward current-transfer ratio is often called alpha (or α), and the common-emitter forward current-transfer ratio is often called beta (or β).

In the common-base circuit shown in Fig. 21 the emitter is the input electrode and the collector is the output electrode. The dc alpha, therefore, is the ratio of the steady-state collector current I_c to the steady-state emitter current I_e :

$$\alpha = \frac{I_c}{I_e} = \frac{0.98 I}{I} = 0.98$$

In the common-emitter circuit shown in Fig. 22, the base is the input electrode and the collector is the output electrode. The dc beta, therefore, is the ratio of the steady-state collector current I_c to the steady-state base current I_b :

$$\beta = \frac{I_c}{I_b} = \frac{0.98 I}{0.02 I} = 49$$

Because the ratios given above are based on steady-state currents, they are properly called dc alpha and dc beta. It is more common, however, for the current-transfer ratio to be given in terms of the ratio of signal currents in the input and output electrodes, or the ratio of a change in the output current to the input signal current which causes the change. Fig. 26 shows

typical electrode currents in a common-emitter circuit (a) under no-signal conditions and (b) with a one-microampere signal applied to the base. The signal current of one microampere in the base causes a change of 49 microamperes (147-98) in the collector current. Thus the ac beta for the transistor is 49.

The cutoff frequency of a transistor is defined as the frequency at

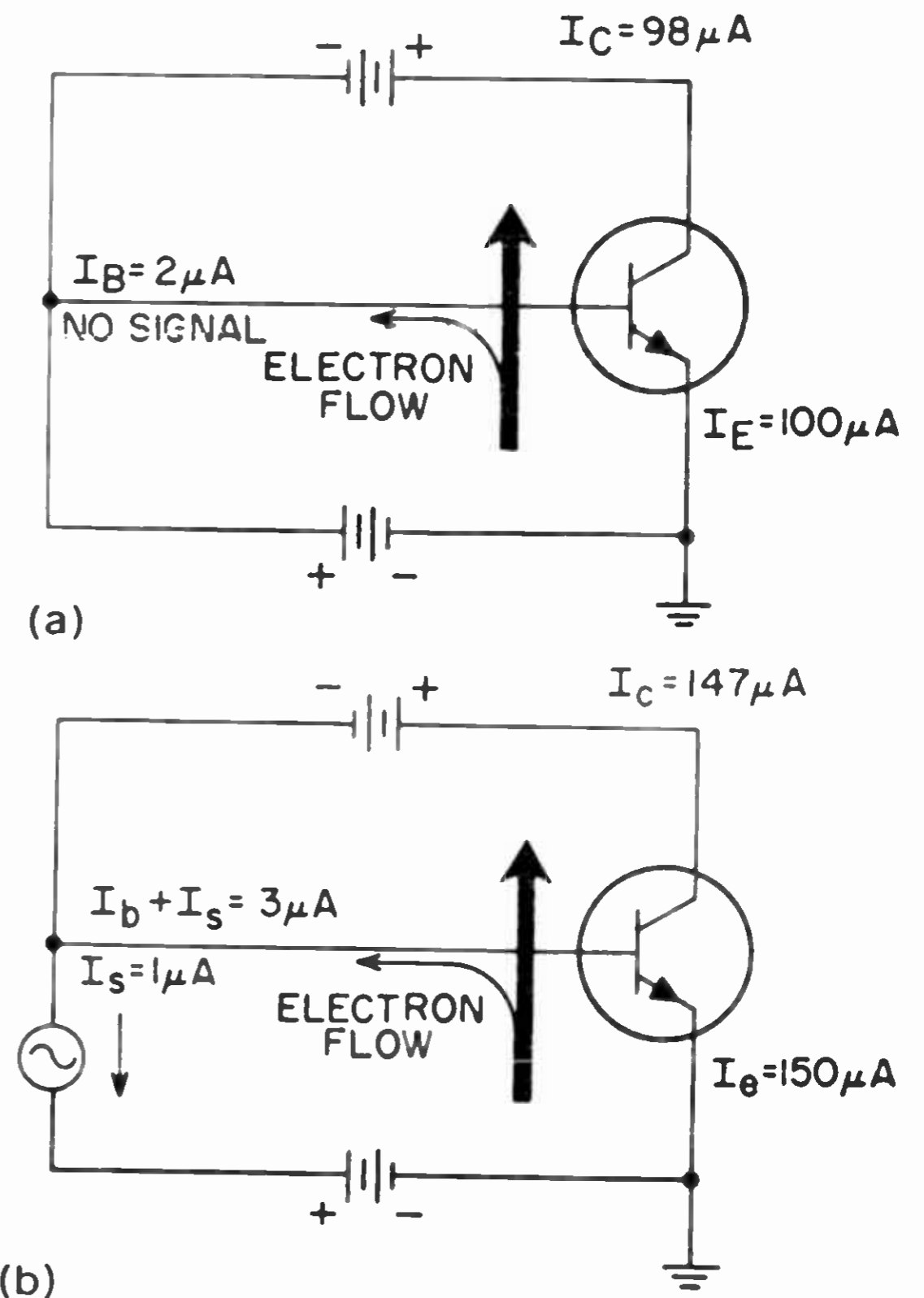


Fig. 26—Electrode currents under (a) no-signal and (b) signal conditions.

which the value of alpha (for a common-base circuit) or beta (for a common-emitter circuit) drops to 0.707 times its 1-kHz value. The **gain-bandwidth product** is the frequency at which the common-emitter forward current-transfer ratio (beta) is equal to unity. These characteristics provide an approximate indication of the useful frequency range of the device, and help to determine the most suitable circuit configuration for a particular application. Fig. 27 shows typical curves of alpha and beta as functions of frequency.

Extrinsic transconductance may be defined as the quotient of a small change in collector current divided

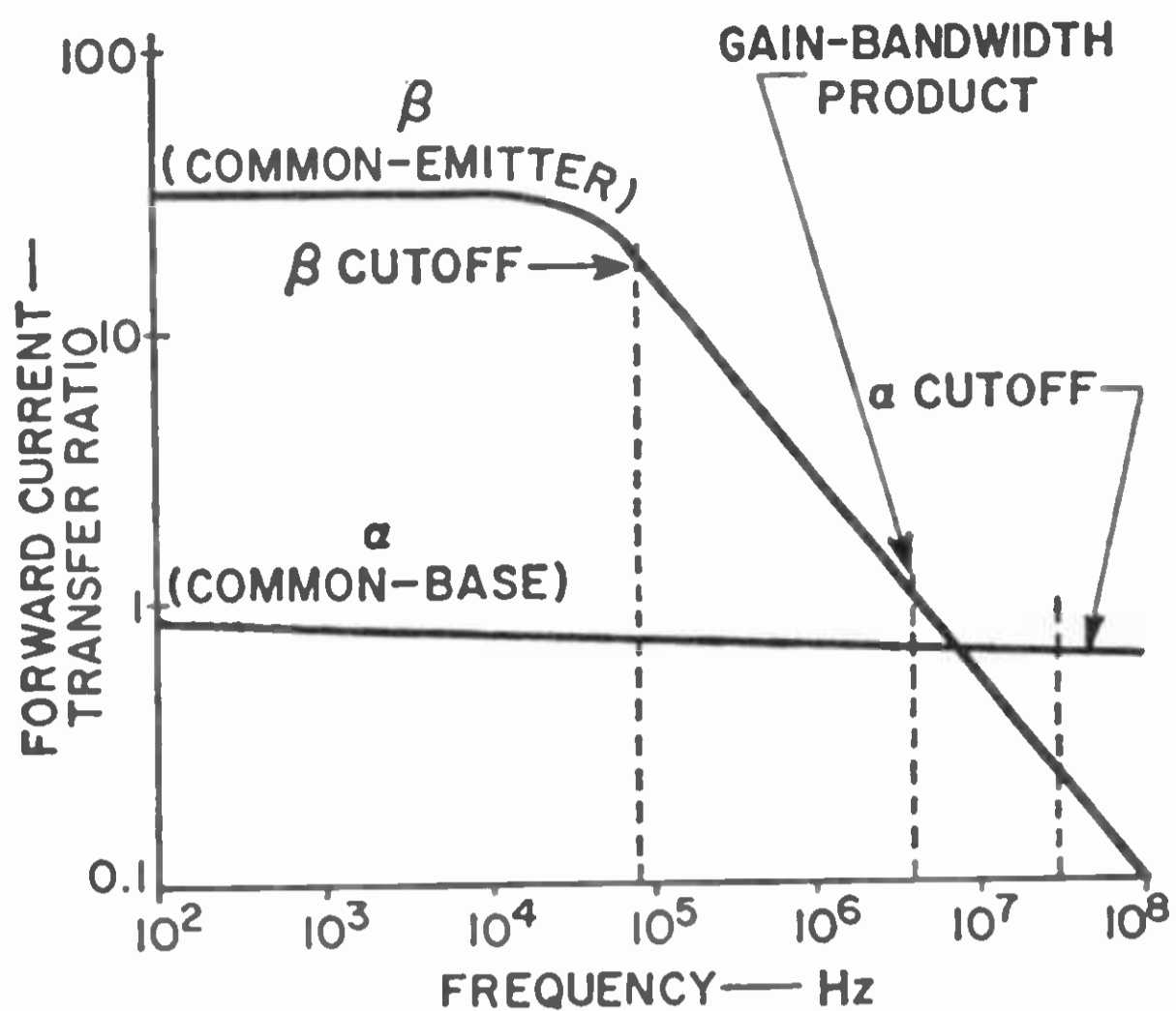


Fig. 27—Forward current-transfer ratio as a function of frequency.

by the small change in emitter-to-base voltage producing it, under the condition that other voltages remain unchanged. Thus, if an emitter-to-base voltage change of 0.1 volt causes a collector-current change of 3 milliamperes (0.003 ampere) with other voltages constant, the transconductance is 0.003 divided by 0.1, or 0.03 mho. (A "mho" is the unit of conductance, and was named by spelling "ohm" backward.) For convenience, a millionth of a mho, or a micro-mho (μ mho), is used to express transconductance. Thus, in the example, 0.03 mho is 30,000 micromhos.

Cutoff currents are small steady-state reverse currents which flow when a transistor is biased into non-conduction. They consist of leakage currents, which are related to the surface characteristics of the semiconductor material, and saturation currents, which are related to the impurity concentration in the material and which increase with increasing temperatures. Collector-cutoff current is the steady-state current which flows in the reverse-biased collector-to-base circuit when the emitter-to-base circuit is open. Emitter-cutoff current is the current which flows in the reverse-biased emitter-to-base circuit when the collector-to-base circuit is open.

Transistor breakdown voltages define the voltage values between two

specified electrodes at which the crystal structure changes and current begins to rise rapidly. The voltage then remains relatively constant over a wide range of electrode currents. Breakdown voltages may be measured with the third electrode open, shorted, or biased in either the forward or the reverse direction. For example, Fig. 28 shows a series of collector-characteristic curves for different base-bias conditions. It can

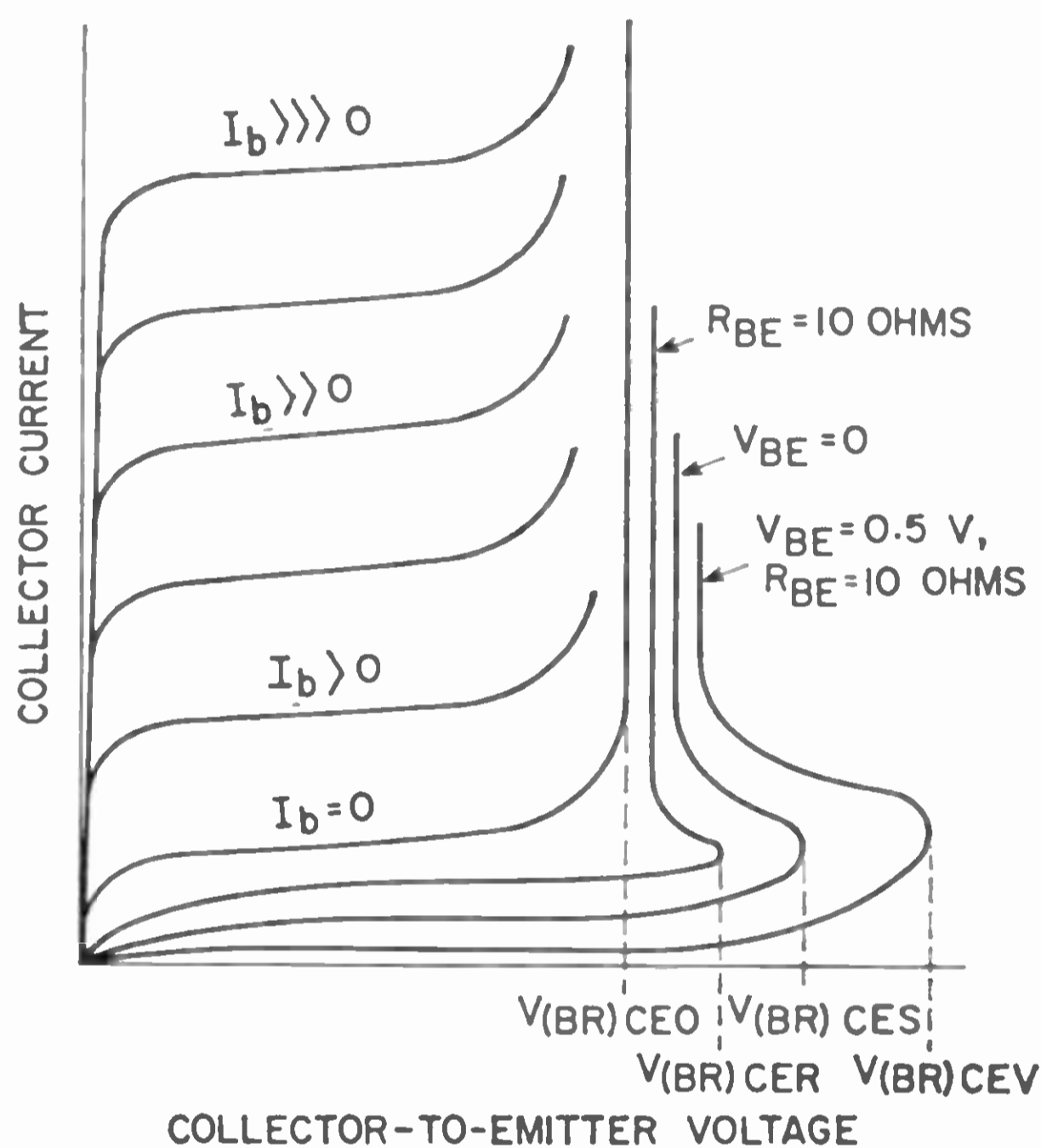


Fig. 28—Typical collector-characteristic curves showing location of various breakdown voltages.

be seen that the collector-to-emitter breakdown voltage increases as the base-to-emitter bias decreases from the normal forward values through zero to reverse values. The symbols shown on the abscissa are sometimes used to designate collector-to-emitter breakdown voltages with the base open $V_{(BR)CEO}$, with external base-to-emitter resistance $V_{(BR)CER}$, with the base shorted to the emitter $V_{(BR)CES}$, and with a reverse base-to-emitter voltage $V_{(BR)CEV}$.

As the resistance in the base-to-emitter circuit decreases, the collector characteristic develops two breakdown points, as shown in Fig. 24. After the initial breakdown, the collector-to-emitter voltage decreases with increasing collector current

until another breakdown occurs at a lower voltage. This minimum collector-to-emitter breakdown voltage is called the **sustaining voltage**.

In large-area power transistors, there is a limiting mechanism referred to as "second breakdown". This condition is not a voltage breakdown, but rather an electrically and thermally regenerative process in which current is focused in a very small area of the order of the diameter of a human hair. The very high current, together with the voltage across the transistor, causes a localized heating that may melt a minute hole from the collector to the emitter of the transistor and thus cause a short circuit. This regenerative process is not initiated unless certain high voltages and currents are coincident for certain finite lengths of time.

In conventional transistor structures, the limiting effects of second breakdown vary directly with the amplitude of the applied voltage and inversely with the width of the base region. These effects are most severe in power transistors in which narrow base structures are used to achieve good high-frequency response. In RCA "overlay" power transistors, a special emitter configuration is used to provide greater current-handling capability and minimize the possibility of "hot spots" occurring at the emitter-base junction. This new design extends the range of power and frequency over which transistors can be operated before second breakdown begins to limit performance.

The curves at the left of Fig. 28 show typical collector characteristics under normal forward-bias conditions. For a given base input current, the collector-to-emitter saturation voltage is the minimum voltage required to maintain the transistor in full conduction (i.e., in the saturation region). Under saturation conditions, a further increase in forward bias produces no corresponding increase in collector current. Saturation voltages are very important in switch-

ing applications, and are usually specified for several conditions of electrode currents and ambient temperatures.

Reach-through (or **punch-through**) voltage defines the voltage value at which the depletion region in the collector region passes completely through the base region and makes contact at some point with the emitter region. This "reach-through" phenomenon results in a relatively low-resistance path between the emitter and the collector, and causes a sharp increase in current. Punch-through voltage does not result in permanent damage to a transistor, provided there is sufficient impedance in the power-supply source to limit transistor dissipation to safe values.

BIASING

For most non-switching applications, the operating point for a particular transistor is established by the quiescent (dc, no-signal) values of collector voltage and emitter current. In general, a transistor may be considered as a current-operated device, i.e., the current flowing in the emitter-base circuit controls the current flowing in the collector circuit. The voltage and current values selected, as well as the particular biasing arrangement used, depend upon both the transistor characteristics and the specific requirements of the application.

As mentioned previously, biasing of a transistor for most applications consists of forward bias across the emitter-base junction and reverse bias across the collector-base junction. In Figs. 21, 22, and 23, two batteries were used to establish bias of the correct polarity for an n-p-n transistor in the common-base, common-emitter, and common-collector circuits, respectively. Many variations of these basic circuits can also be used. (In these simplified dc circuits, inductors and transformers are represented only by their series resistance.)

A simplified biasing arrangement for the common-base circuit is shown in Fig. 29. Bias for both the collector-base junction and the emitter-base

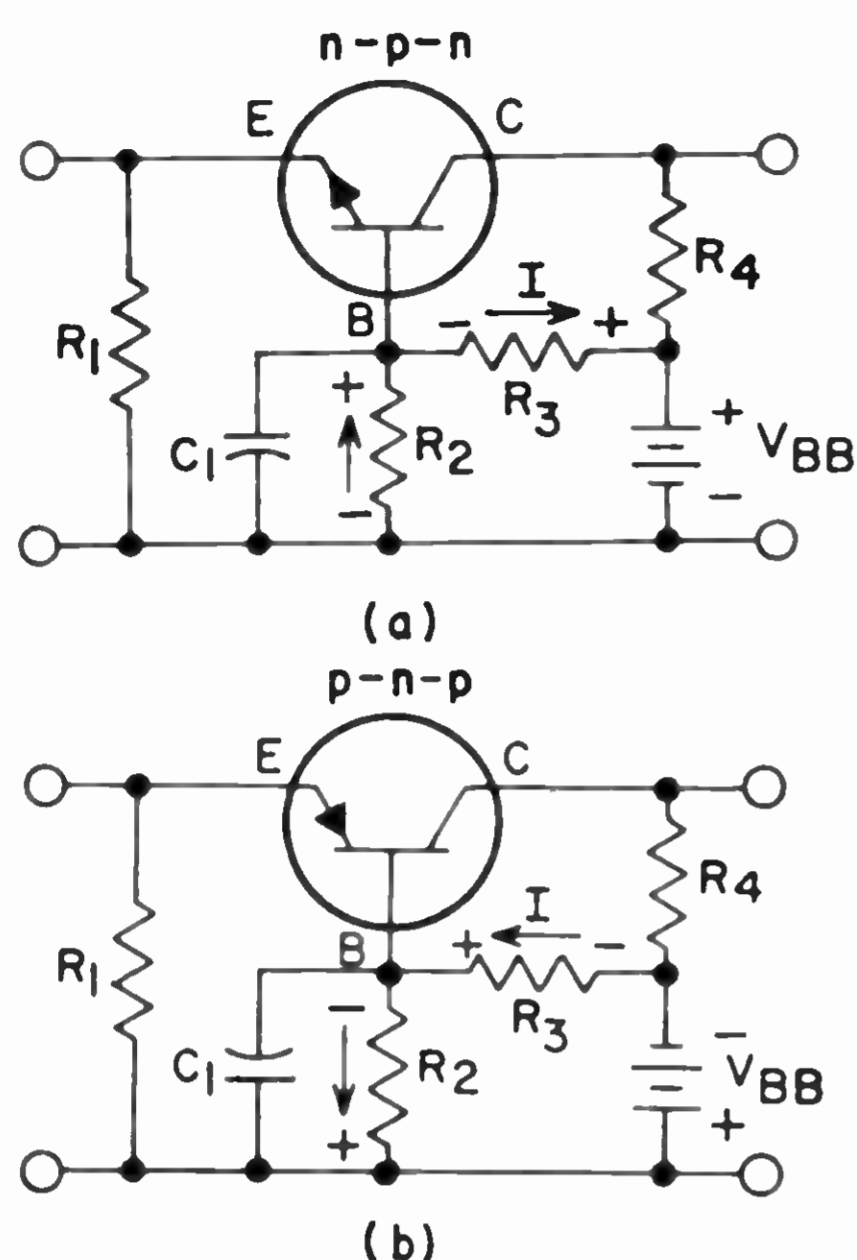


Fig. 29—Biasing network for common-base circuit for (a) *n-p-n* and (b) *p-n-p* transistors.

junction is obtained from the single battery through the voltage-divider network consisting of resistors R_2 and R_3 . (For the *n-p-n* transistor shown in Fig. 29(a) the emitter-base junction is forward-biased because the emitter is negative with respect to the base, and the collector-base junction is reverse-biased because the collector is positive with respect to the base, as shown. For the *p-n-p* transistor shown in Fig. 29(b), the polarity of the battery and of the electrolytic bypass capacitor C_1 is reversed.) The electron current I from the battery and through the voltage divider causes a voltage drop across resistor R_2 which biases the base. The proper amount of current then flows through R_1 so that the correct emitter potential is established to provide forward bias relative to the base. This emitter current establishes the amount of collector current which, in turn, causes a voltage drop across R_4 . Simply stated, the voltage divider consisting of R_2 and R_3 establishes the base potential; the base potential essentially establishes the emitter potential; the emitter poten-

tial and resistor R_1 establish the emitter current; the emitter current establishes the collector current; and the collector current and R_4 establish the collector potential. R_2 is bypassed with capacitor C_1 so that the base is effectively grounded for ac signals.

A single battery can also be used to bias the common-emitter circuit. The simplified arrangement shown in Fig. 30 is commonly called "fixed bias". In this case, both the base and the collector are made positive with respect to the emitter by means of the battery. The base resistance R_B is then selected to provide the desired base current I_B for the transistor (which, in turn, establishes the desired emitter current I_E), by means of the following expression:

$$R_B = \frac{V_{BB} - V_{BE}}{I_B}$$

where V_{BB} is the battery supply voltage and V_{BE} is the base-to-emitter voltage of the transistor.

In the circuit shown, for example, the battery voltage is six volts. The

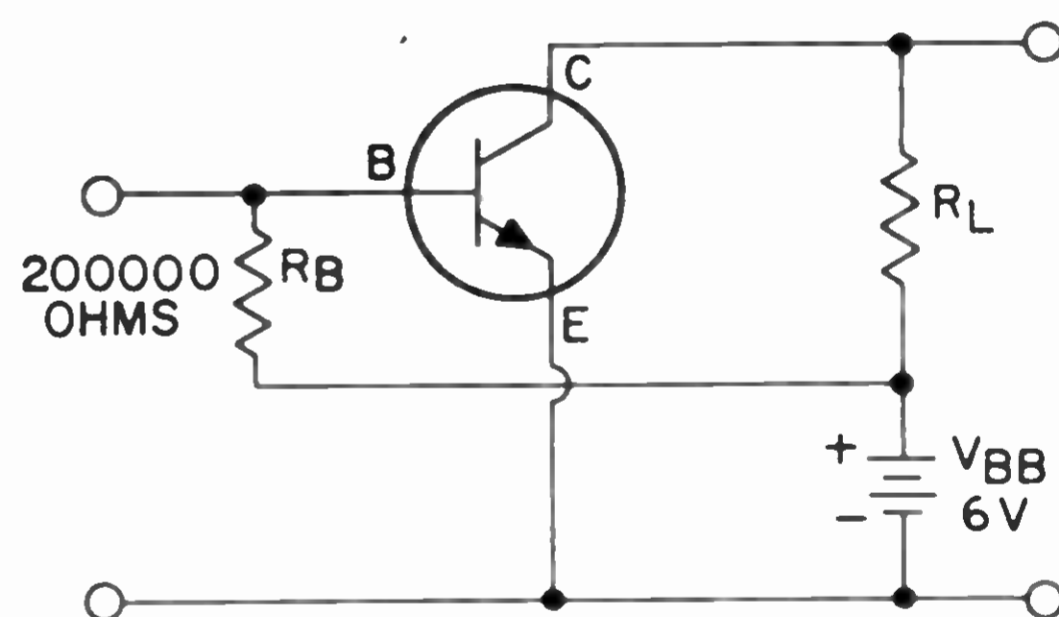


Fig. 30—"Fixed-bias" arrangement for common-emitter circuit.

value of R_B was selected to provide a base current of 27 microamperes, as follows:

$$R_B = \frac{6 - 0.6}{27 \times 10^{-6}} = 200,000 \text{ ohms}$$

The fixed-bias arrangement shown in Fig. 30, however, is not a satisfactory method of biasing the base in a common-emitter circuit. The critical base current in this type of circuit is very difficult to maintain under fixed-bias conditions because of variations between transistors and the sensitivity of these devices

to temperature changes. This problem is partially overcome in the "self-bias" arrangement shown in Fig. 31.

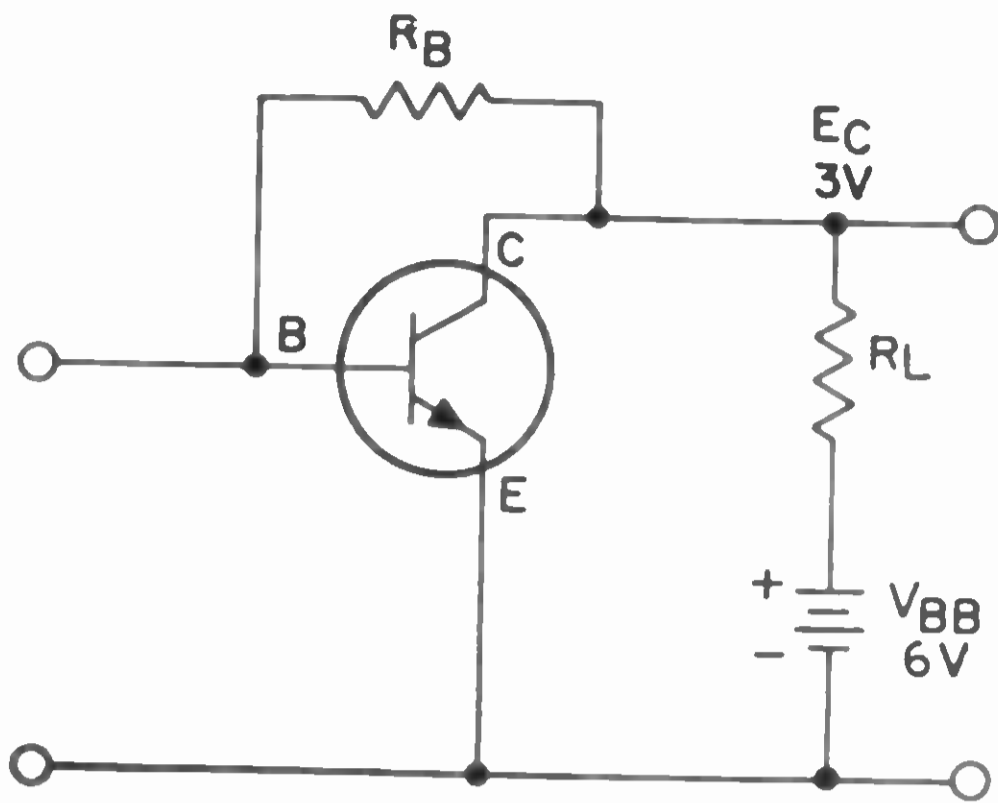


Fig. 31—"Self-bias" arrangement for common-emitter circuit.

In this circuit, the base resistor is tied directly to the collector. This connection helps to stabilize the operating point because an increase or decrease in collector current produces a corresponding decrease or increase in base bias. The value of R_B is then determined as described above, except that the collector voltage V_{CE} is used in place of the supply voltage V_{BB} :

$$R_B = \frac{V_{CE} - V_{BE}}{I_B}$$

$$= \frac{3 - 0.6}{27 \times 10^{-6}} = 90,000 \text{ ohms}$$

The arrangement shown in Fig. 31 overcomes many of the disadvantages of fixed bias, although it reduces the effective gain of the circuit.

In the bias method shown in Fig. 32 the voltage-divider network composed of R_1 and R_2 provides the

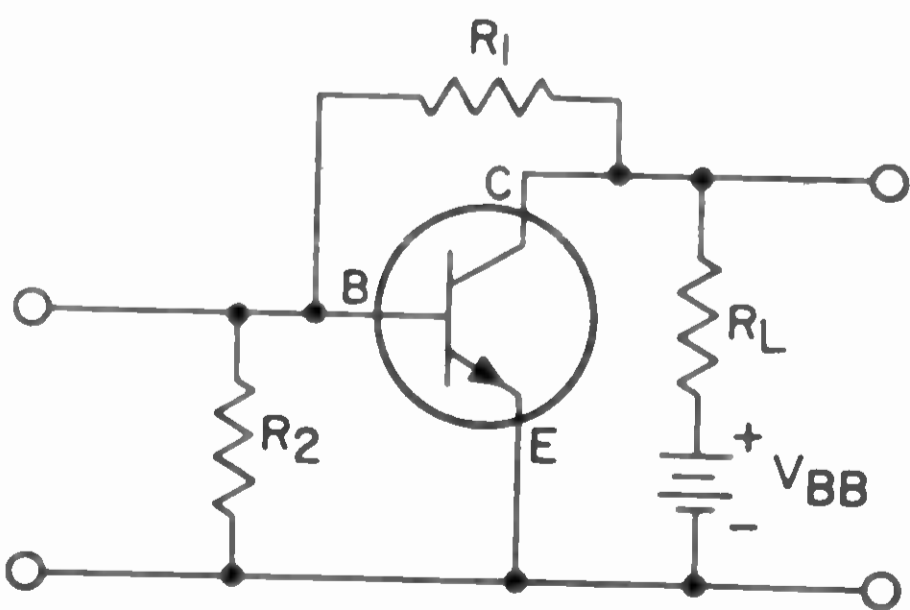


Fig. 32—Bias network using voltage-divider arrangement for increased stability.

required forward bias across the base-emitter junction. The value of

the base bias voltage is determined by the current through the voltage divider. This type of circuit provides less gain than the circuit of Fig. 31, but is commonly used because of its inherent stability.

The common-emitter circuits shown in Figs. 33 and 34 may be used to provide stability and yet minimize loss of gain. In Fig. 33, a resistor

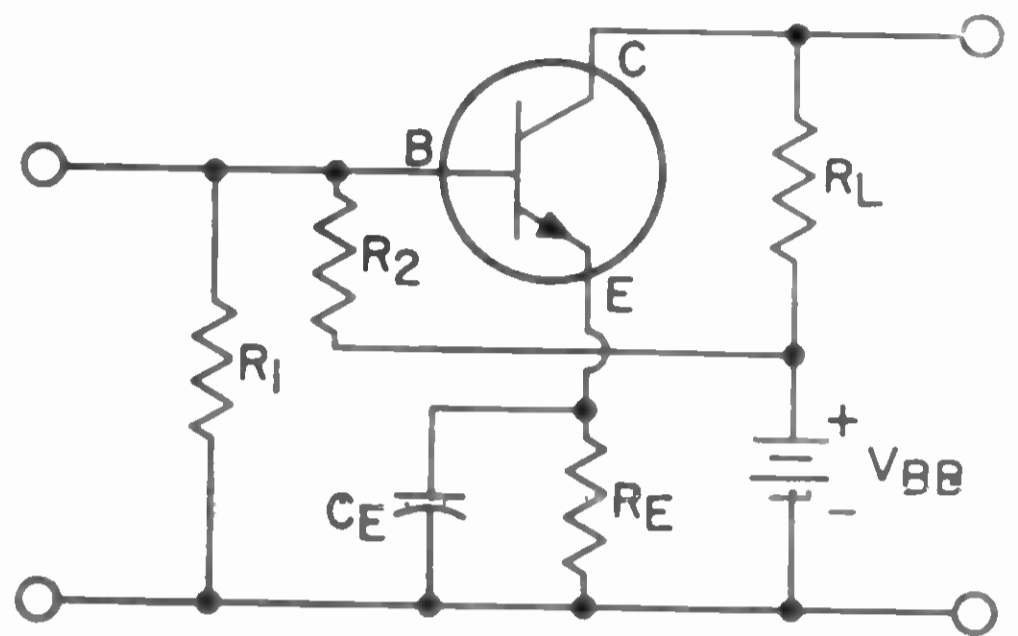


Fig. 33—Bias network using emitter stabilizing resistor.

R_E is added to the emitter circuit, and the base resistor R_2 is returned to the positive terminal of the battery instead of to the collector. The emitter resistor R_E provides additional stability. It is bypassed with capacitor C_E . The value of C_E depends on the lowest frequency to be amplified.

In Fig. 34 the R_2R_3 voltage-divider network is split, and all ac feedback currents through R_3 are shunted to ground (bypassed) by capacitor C_1 .

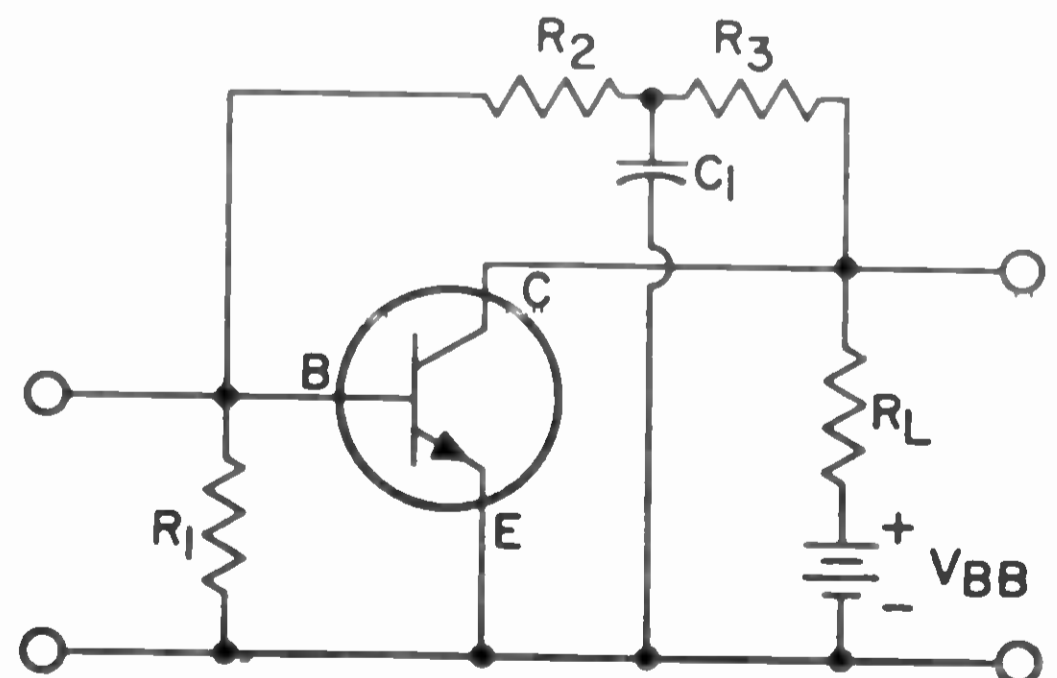


Fig. 34—Bias network using split voltage-divider network.

The value of R_3 is usually larger than the value of R_2 . The total resistance of R_2 and R_3 should equal the resistance of R_1 in Fig. 32.

In practical circuit applications, any combination of the arrangements shown in Figs. 31, 32, 33, and 34 may be used. However, the stability of Figs. 31, 32, and 34 may be

poor unless the voltage drop across the load resistor R_L is at least one-third the value of the supply voltage. The determining factors in the selection of the biasing circuit are usually gain and bias stability (which is discussed later).

In many cases, the bias network may include special elements to compensate for the effects of variations in ambient temperature or in supply voltage. For example, the thermistor (temperature-sensitive resistor) shown in Fig. 35(a) is used to compensate for the rapid increase of collector current with increasing

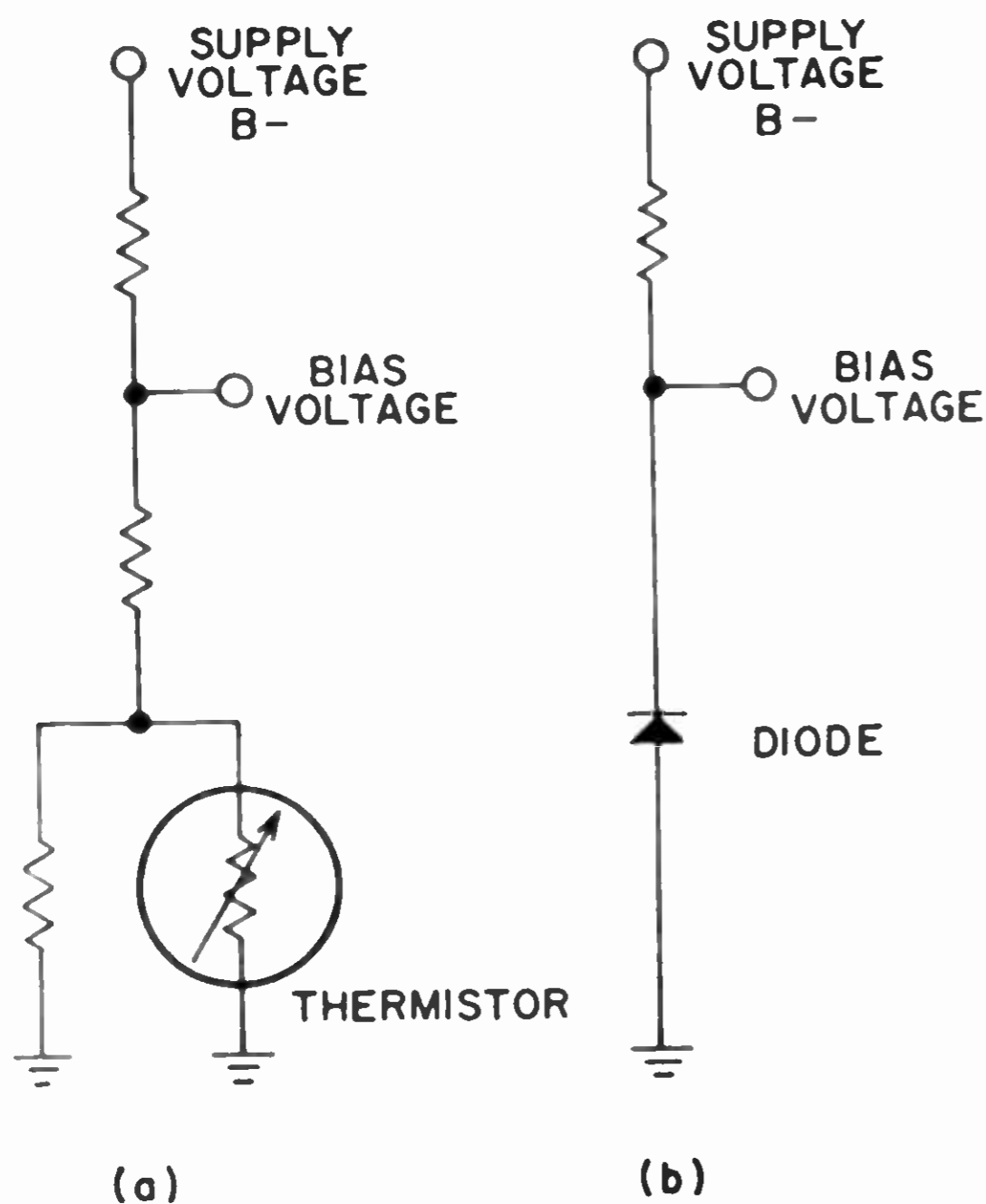


Fig. 35—Bias networks including (a) a thermistor and (b) a voltage-compensating diode.

temperature. Because the thermistor resistance decreases as the temperature increases, the emitter-to-base bias voltage is reduced and the collector current tends to remain constant. The addition of the shunt and series resistances provides most effective compensation over a desired temperature range.

The diode biasing network shown in Fig. 35(b) stabilizes collector current for variations in both temperature and supply voltage. The forward-biased diode current determines a bias voltage which establishes the transistor **idling** current (collector

current under no-signal conditions). As the temperature increases, this bias voltage decreases. Because the transistor characteristic also shifts in the same direction and magnitude, however, the idling current remains essentially independent of temperature. Temperature stabilization with a properly designed diode network is substantially better than that provided by most thermistor bias networks. Any temperature-stabilizing element should be thermally close to the transistor being stabilized.

In addition, the diode bias current varies in direct proportion with changes in supply voltage. The resultant change in bias voltage is small, however, so that the idling current also changes in direct proportion to the supply voltage. Supply-voltage stabilization with a diode biasing network reduces current variation to about one-fifth that obtained when resistor or thermistor bias is used for a germanium transistor and one-fifteenth for a silicon transistor.

The bias networks of Figs. 30 through 34 are generally used in class A circuits. Class B circuits normally employ the bias networks shown in Fig. 35. The bias resistor values for class B circuits are generally much lower than those for class A circuits.

BIAS STABILITY

Because transistor currents tend to increase with temperature, it is necessary in the design of transistor circuits to include a "stability factor" to keep the collector-current variation within tolerable values under the expected high-temperature operating conditions. The bias stability factor SF is expressed as the ratio between a change in steady-state collector current and the corresponding change in steady-state collector-cutoff current.

For a given set of operating voltages, the stability factor can be calculated for a maximum permissible rise in steady-state collector current

from the room-temperature value, as follows:

$$SF = \frac{I_{C_{max}} - I_{C1}}{I_{C_{BO2}} - I_{C_{BO1}}}$$

where I_{C1} and $I_{C_{BO1}}$ are measured at 25°C, $I_{C_{BO2}}$ is measured at the maximum expected ambient (or junction) temperature, and $I_{C_{max}}$ is the maximum permissible collector current for the specified collector-to-emitter voltage at the maximum expected ambient (or junction) temperature (to keep transistor dissipation within ratings).

The calculated values of SF can then be used, together with the appropriate values of beta and r_b' (base-connection resistance), to determine suitable resistance values for the transistor circuit. Fig. 36 shows equations for SF in terms of resistance values for three typical circuit configurations. The maximum value which SF can assume is the value of beta. Although this analysis was originally made for germanium transistors, in which the collector saturation current I_{c0} is relatively large, the same type of analysis may be applied to interchangeability with beta for silicon transistors.

COUPLING

Three basic methods are used to couple transistor stages: transformer, resistance-capacitance, and direct coupling.

The major advantage of transformer coupling is that it permits power to be transferred from one impedance level to another. A transformer-coupled common-emitter n-p-n stage is shown in Fig. 37. The voltage step-down transformer T_1 couples the signal from the collector of the preceding stage to the base of the common-emitter stage. The voltage loss inherent in this transformer is not significant in transistor circuits because, as mentioned previously, the transistor is a current-operated device. Although the voltage is stepped down, the available current is stepped up. The change in base current resulting from the presence of the signal causes an alternating collector current to flow in the primary winding of transformer T_2 , and a power gain is obtained between T_1 and T_2 .

This use of a voltage step-down transformer is similar to that in the output stage of an audio amplifier, where a step-down transformer is

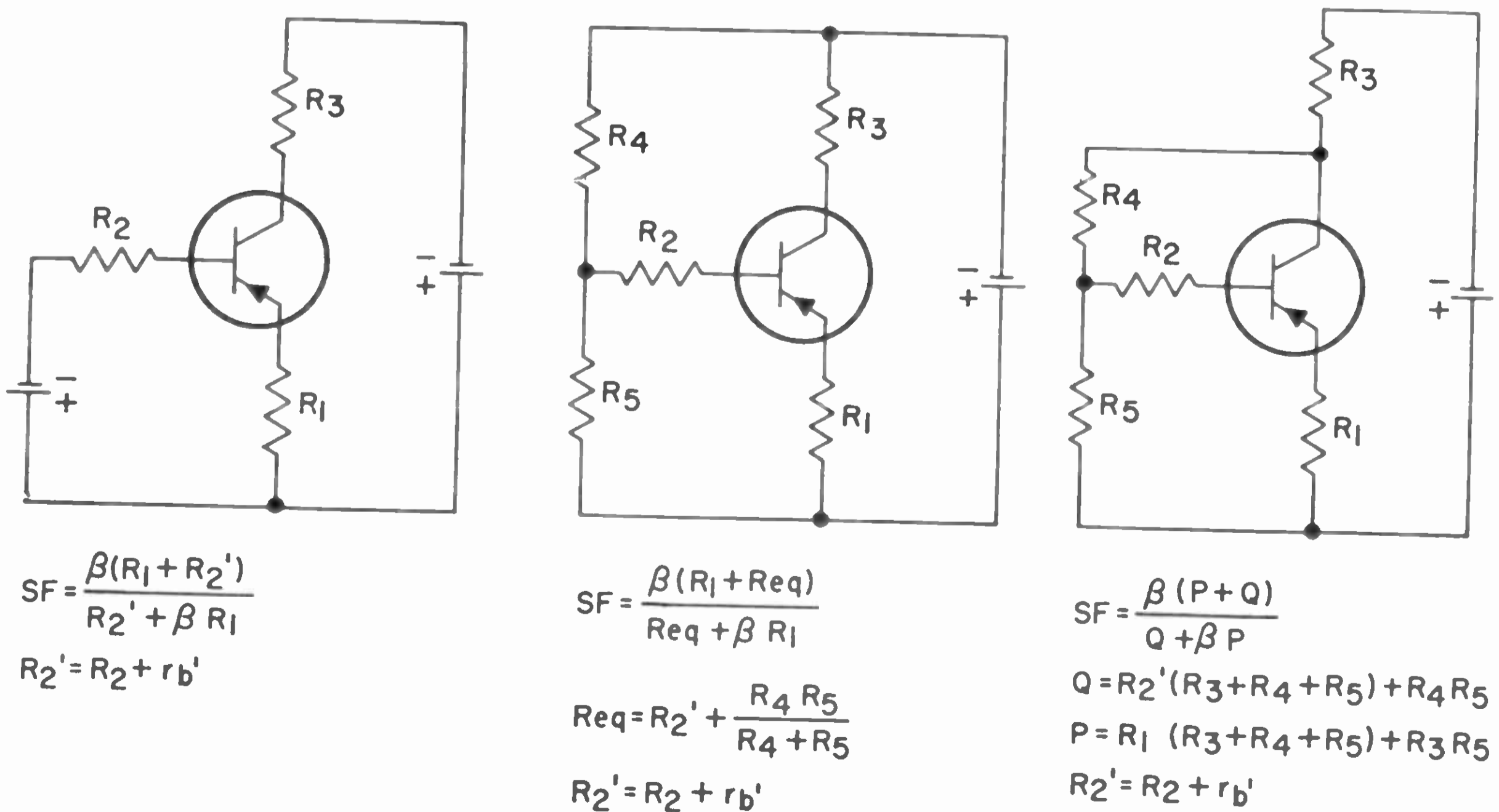


Fig. 36—Bias-stability-factor equations for three typical circuit configurations.

normally used to drive the loudspeaker, which is also a current-operated device.

The voltage-divider network consisting of resistors R_1 and R_2 in Fig. 37 provides bias for the transistor. The voltage divider is bypassed by capacitor C_1 to avoid signal attenuation. The stabilizing emitter resistor R_E permits normal variations of the transistor and circuit elements to be compensated for automatically without adverse effects. This resistor R_E is bypassed by capacitor C_2 . The voltage supply V_{BB} is also bypassed, by capacitor C_3 , to prevent feedback in the event that ac signal voltages are developed across the power supply. Capacitors C_1 and C_2 may normally be replaced by a single capacitor connected between the emitter and the bottom of the secondary winding of transformer T_1 , with little change in performance.

The use of **resistance-capacitance coupling** usually permits some economy of circuit costs and reduction of size, with some accompanying sacrifice of gain. This method of coupling is particularly desirable in low-level, low-noise audio amplifier stages to minimize hum pickup from stray magnetic fields. Use of resistance-capacitance (RC) coupling in battery-operated equipment is usually limited to low-power operation. The frequency response of an RC-coupled stage is normally better than that of a transformer-coupled stage.

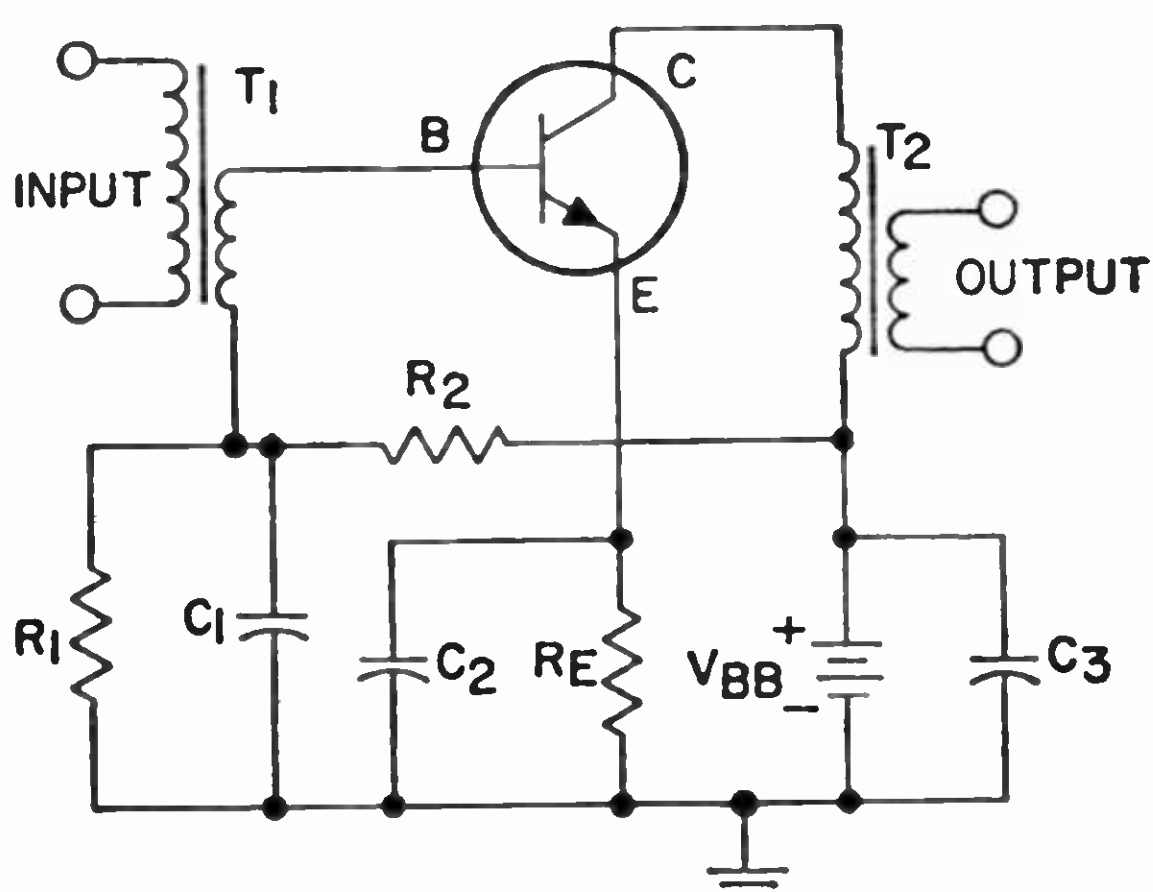


Fig. 37—Transformer-coupled common-emitter stage.

Fig. 38(a) shows a two-stage RC-coupled circuit using n-p-n transistors in the common-emitter configuration. The method of bias is similar to that used in the transformer-coupled circuit of Fig. 37. The major additional components are the collector load resistances R_{L1} and R_{L2} and the coupling capacitor C_c . The value of C_c must be made fairly large, in the order of 2 to 10 microfarads, because of the small input and load resistances involved. (It should be noted that electrolytic capacitors are normally used for coupling in transistor audio circuits. Polarity must be observed, therefore, to obtain proper circuit operation. Occasionally, excessive leakage current through an electrolytic coupling capacitor may adversely affect transistor operating currents.)

Impedance coupling is a modified form of resistance-capacitance coupling in which inductances are used to replace the load resistors. This type of coupling is rarely used except in special applications where supply voltages are low and cost is not a significant factor.

Direct coupling is used primarily when cost is an important factor. (It should be noted that direct-coupled amplifiers are not inherently dc amplifiers, i.e., that they cannot always amplify dc signals. Low-frequency response is usually limited by other factors than the coupling network.) In the direct-coupled amplifier shown in Fig. 38(b), resistor R_3 serves as both the collector load resistor for the first stage and the bias resistor for the second stage. Resistors R_1 and R_2 provide circuit stability similar to that of Fig. 32 because the emitter voltage of transistor Q_2 and the collector voltage of transistor Q_1 are within a few tenths of a volt of each other.

Because so few circuit parts are required in the direct-coupled amplifier, maximum economy can be achieved. However, the number of stages which can be directly coupled is limited. Temperature variation of

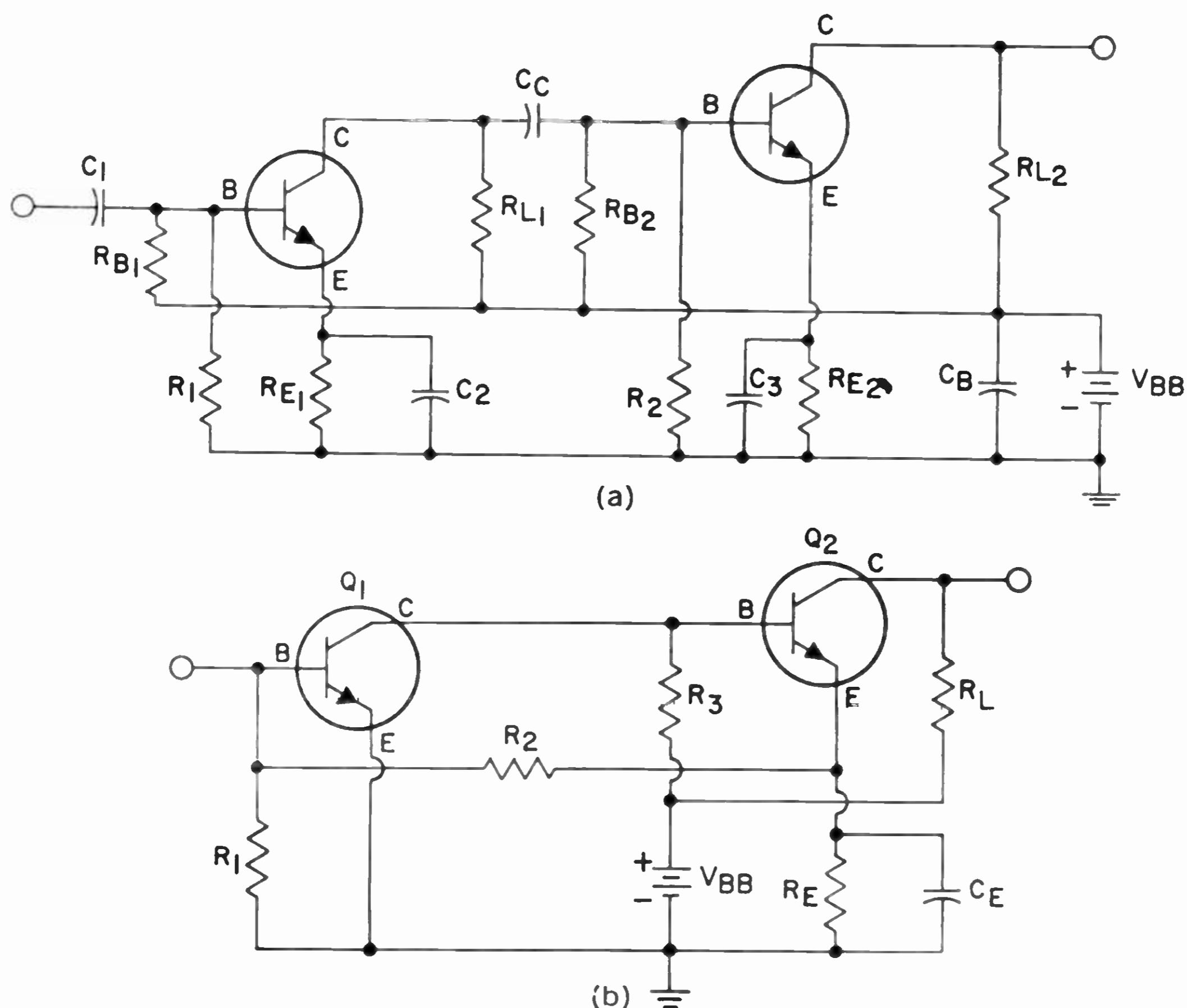


Fig. 38—(a) Two-stage resistance-capacitance-coupled circuit and (b) two-stage direct-coupled circuit.

the bias current in one stage may be amplified by all the stages, and severe temperature instability may result.

HIGH-FREQUENCY OPERATION

At frequencies of 100 MHz or more, the effects of stray capacitances and inductances, ground paths, and feedback coupling have a pronounced effect on the gain and power-output capabilities of transistors. As a result, physical aspects such as layout, type of chassis, shielding, and heat-sink considerations are important in the design of high-frequency amplifiers and oscillators.

In general, high-frequency circuits are constructed on material such as brass or aluminum which is either silver-plated or machined to increase conductivity. The input and output circuits are "compartmentalized" by use of a milling operation. Copper-clad laminated or printed circuit boards facilitate soldering opera-

tions, and have been used satisfactorily at frequencies up to 400 MHz when the entire copper surface was kept intact and used for the ground plane.

Because even a short lead provides a large impedance at high frequencies, it is necessary to keep all high-frequency leads as short as possible. This precaution is especially important for ground connections and for all connections to bypass capacitors and high-frequency filter capacitors. It is recommended that a common ground return be used for each stage, and that short, direct connections be made to the common ground point. The emitter lead especially should be kept as short as possible.

In many cases, problems of oscillation and regenerative feedback are caused by unwanted ground currents (i.e., ground-circuit feedback currents). An effective solution is to isolate the ac signal path from the dc path so that the signal does not pass through the power supply by

way of the power leads. In a multi-stage amplifier, the power leads should enter the circuit at the highest power stage to minimize the amount of signal on the common power path. Lower-frequency oscillations can be minimized by use of a large capacitor across the power-supply terminals. High-quality feed-through capacitors should also be used as the power-lead connections.

Particular care should be taken with the lead dress of the input and output circuits of high-frequency stages so that the possibility of stray coupling is minimized. Unshielded leads connected to shielded components should be dressed close to the chassis. (In high-gain audio amplifiers, these same precautions should be taken to minimize the possibility of self-oscillation.)

Feedback effects may occur in radio or television receivers as a result of coupling between stages through common voltage-supply circuits. Filters find an important use in minimizing such effects. They should be placed in voltage-supply leads to each transistor to provide isolation between stages.

Capacitors used in transistor rf circuits, particularly at high frequencies, should be mica or ceramic. For audio bypassing, electrolytic capacitors are required.

In high-frequency stages having high gain, undesired feedback may occur and produce harmful effects on circuit performance unless shielding is used. The output circuit of each stage is usually shielded from the input of the stage, and each high-frequency stage is usually shielded from other high-frequency stages. It is also desirable to shield separately each unit of the high-frequency stages. For example, each if and rf coil in a superheterodyne receiver may be mounted in a separate shield can. Baffle plates may be mounted on the ganged tuning capacitor to shield each section of the capacitor from the other section.

The shielding precautions required in a circuit depend on the design of

the circuit and the layout of the parts. When the metal case of a transistor is grounded at the socket terminal, the grounding connection should be as short as possible to minimize lead inductance. Many transistors have a separate lead connected to the case and used as a ground lead; where present, these leads are indicated in the outline diagrams.

SWITCHING

Transistor switching applications are generally characterized by large-signal nonlinear operation of the devices. The switching transistor is generally required to operate in either of two states: on or off. In transistor switching circuits, the common-emitter configuration is by far the most widely used.

Typical output characteristics for an n-p-n transistor in the common-emitter configuration are shown in Fig. 39. These characteristics are divided into three regions of operation, i.e., cutoff region, active region, and saturation region.

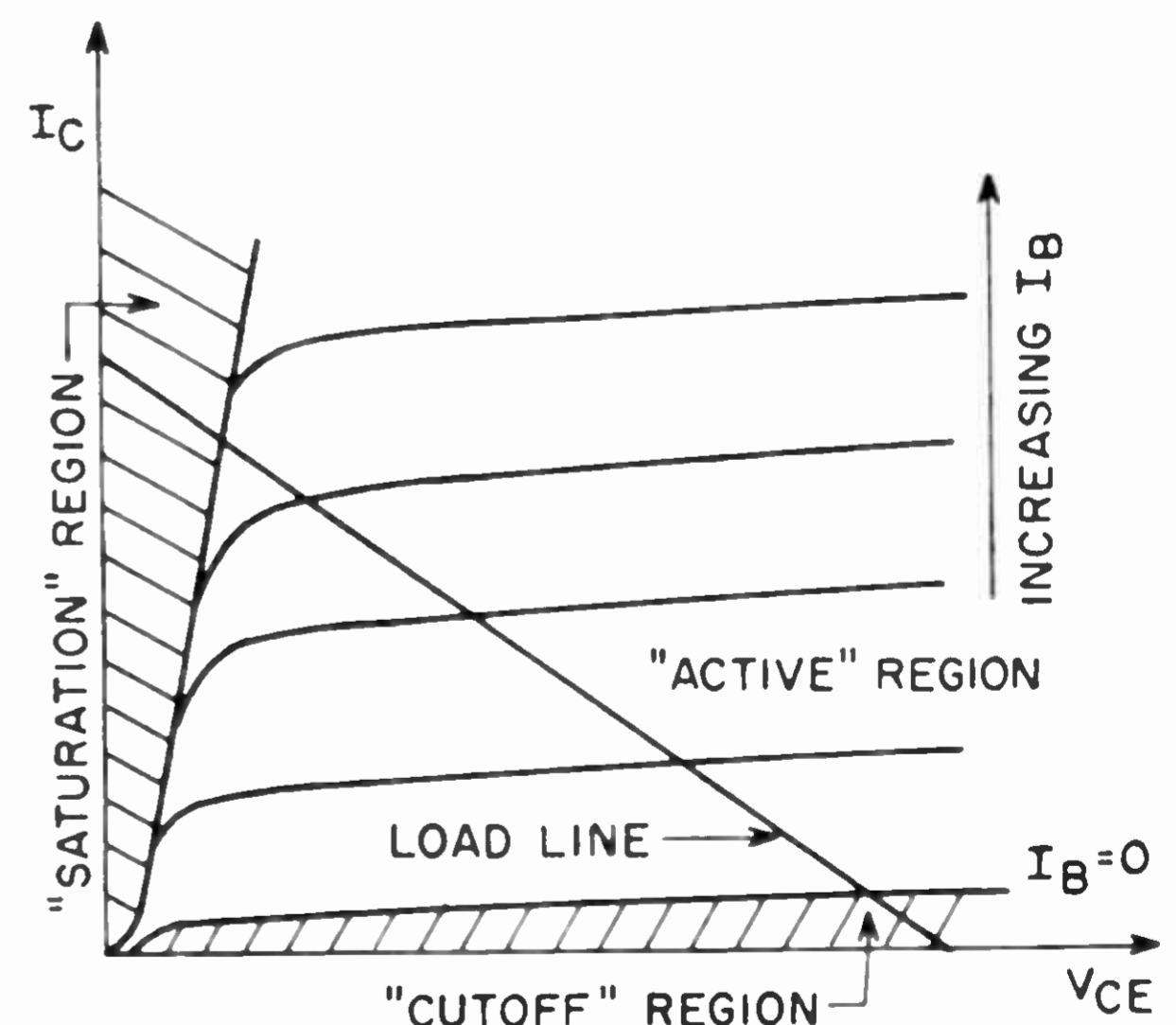


Fig. 39—Typical collector characteristic of an n-p-n transistor showing three principal regions involved in switching.

In the cutoff region, both the emitter-base and collector-base junctions are reverse-biased. Under these conditions, the collector current is very small, and is comparable in magnitude to the leakage current

I_{CEO} , I_{CEV} , or I_{CBO} , depending on the type of base-emitter biasing used.

Fig. 40 is a sketch of the minority-carrier concentration in an n-p-n transistor. For the cutoff condition,

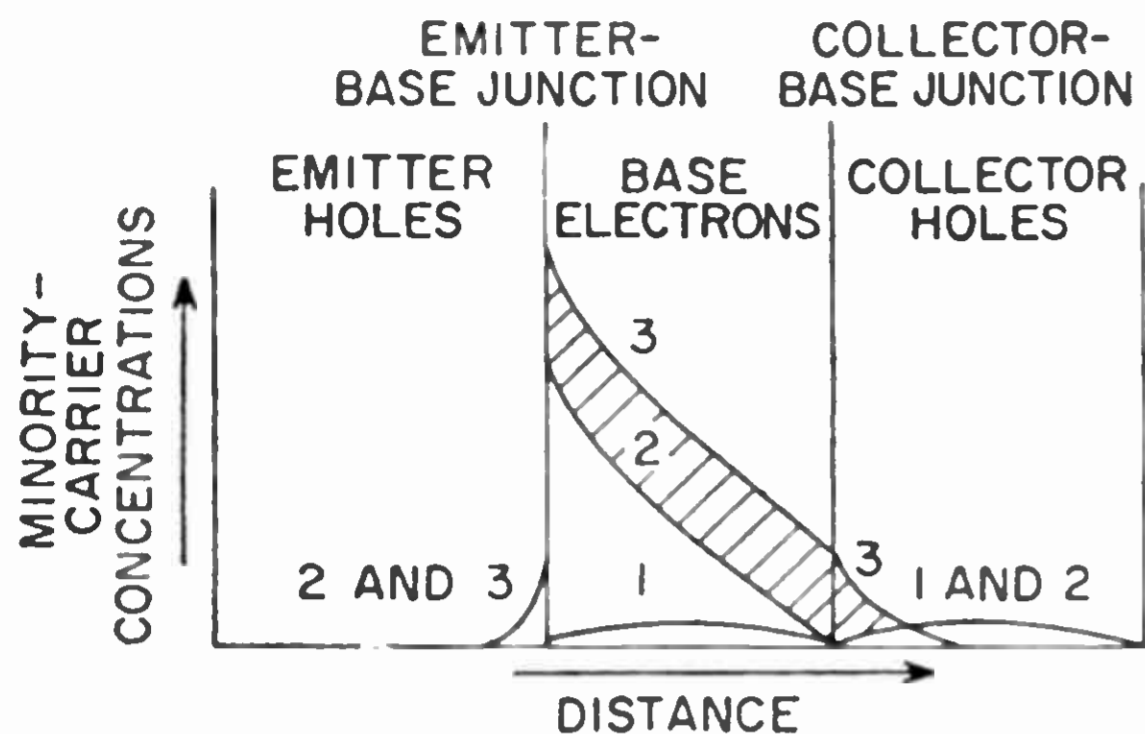


Fig. 40—Minority-carrier concentrations in an n-p-n transistor: (1) in cutoff region, (2) in active region at edge of saturation region, (3) in saturation region.

the concentration is zero at both junctions because both junctions are reverse-biased, as shown by curve 1 in Fig. 40.

In the active region, the emitter-base junction is forward-biased and the collector-base junction is reverse-biased. Switching from the cutoff region to the active region is accomplished along a load line, as indicated in Fig. 39. The speed of transition through the active region is a function of the frequency-response characteristics of the device. The minority-carrier concentration for the active region is shown by curve 2 in Fig. 40.

The remaining region of operation is the saturation region. In this region, the emitter-base and collector-base junctions are both forward-biased. Because the forward voltage drop across the emitter-base junction under this condition [$V_{BE}(\text{sat})$] is greater than that across the collector-base junction, there is a net collector-to-emitter voltage referred to as $V_{CE}(\text{sat})$. It is evident that any series-resistance effects of the emitter and collector also enter into determining $V_{CE}(\text{sat})$. Because the collector is now forward-biased, additional carriers are injected into the base, and some into the collector.

This minority-carrier concentration is shown by curve 3 in Fig. 40.

A basic saturated-transistor switching circuit is shown in Fig. 41. The voltage and current waveforms for this circuit under typical

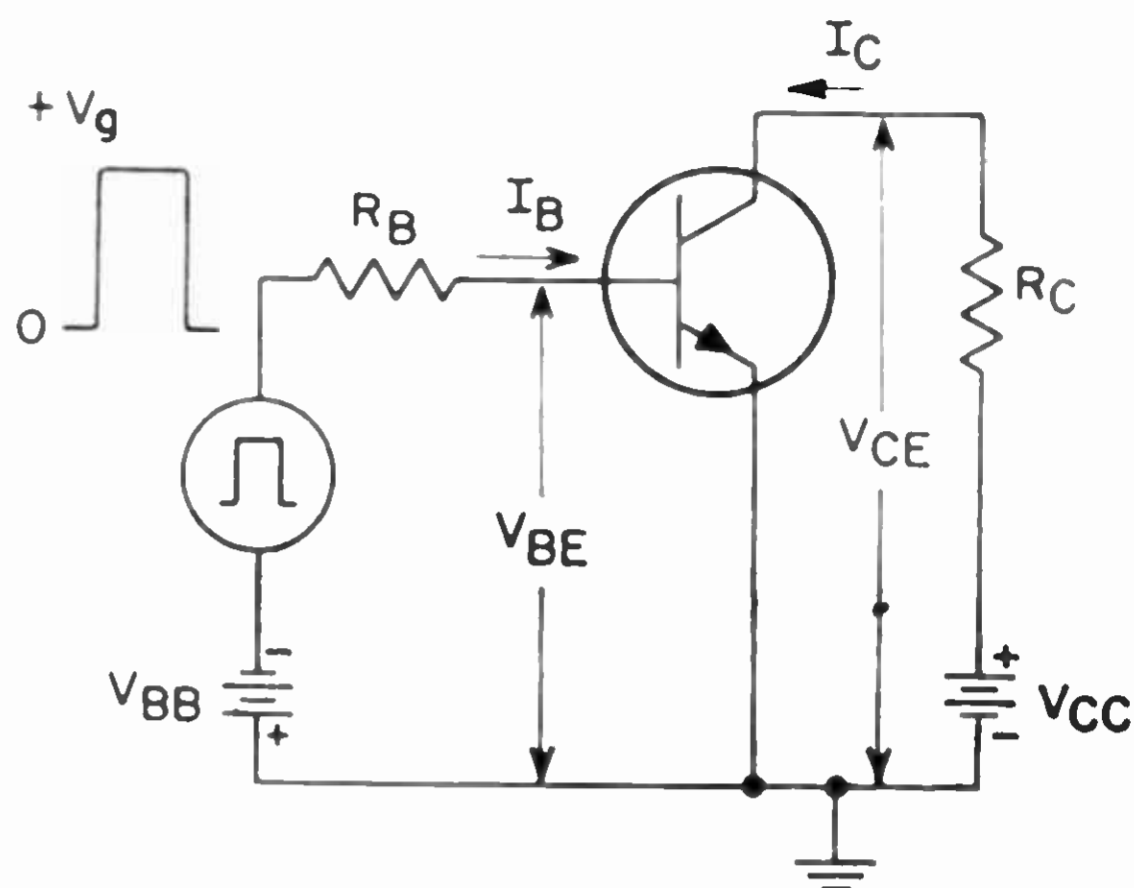


Fig. 41—Basic saturated transistor switching circuit.

base-drive conditions are shown in Fig. 42. Prior to the application of the positive-going input pulse, the emitter-base junction is reverse-biased by a voltage $-V_{BE}(\text{off}) = V_{BB}$. Because the transistor is in the cutoff region, the base current I_B is the reverse leakage current I_{BEV} , which is negligible compared with I_{B1} , and the collector current I_C is the reverse leakage current I_{CEV} , which is negligible compared with V_{CC}/R_C . When the positive-going input pulse V_g is applied, the base current I_B immediately goes positive.

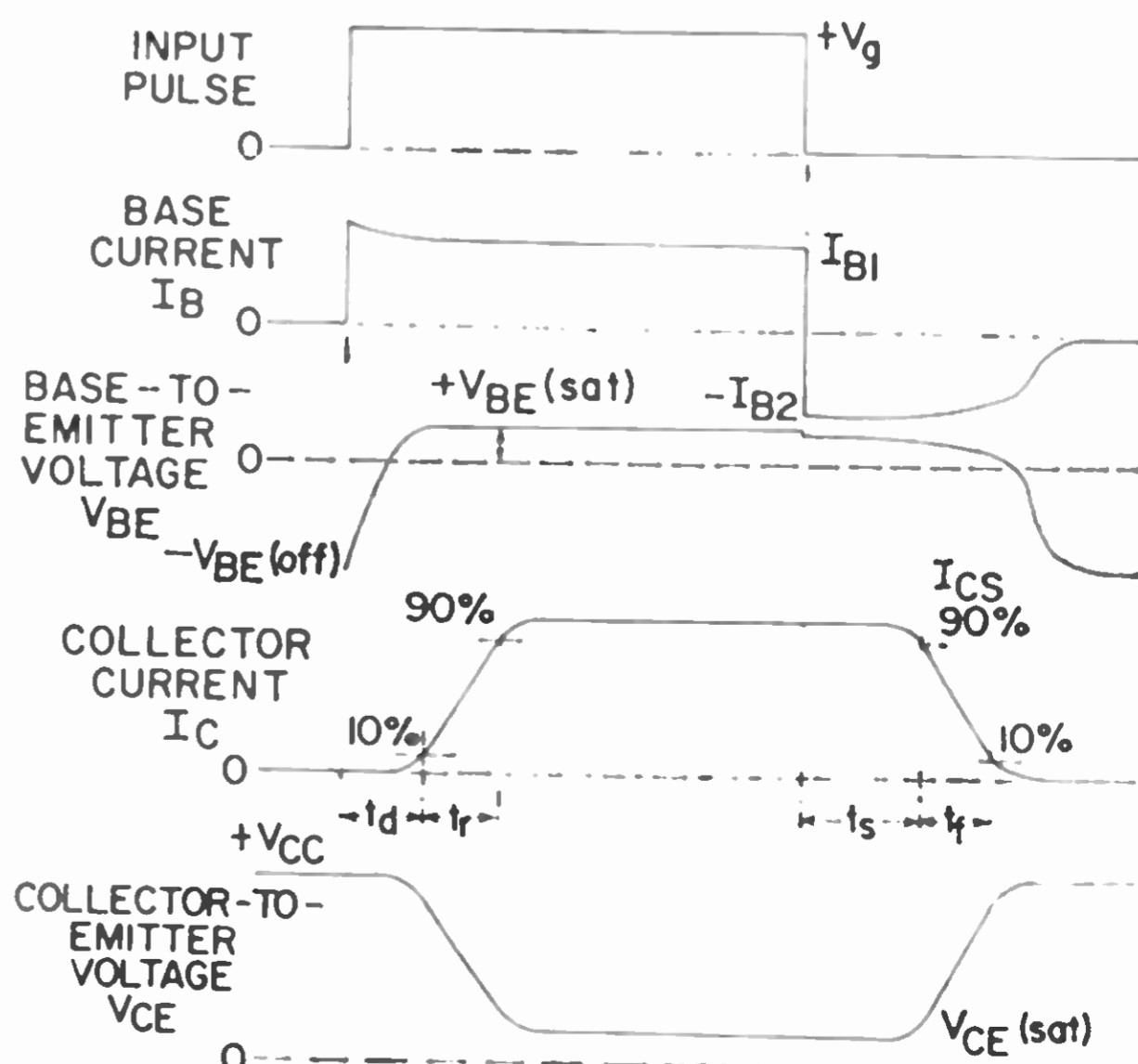


Fig. 42—Voltage and current waveforms for saturated switching circuit shown in Fig. 41.

The collector current, however, does not begin to increase until some time later. This delay in the flow of collector current (t_d) results because the emitter and collector capacitances do not allow the emitter-base junction to become forward-biased instantaneously. These capacitances must be charged from their original negative potential $[-V_{BE}(\text{off})]$ to a forward bias sufficient to cause the transistor to conduct appreciably. After the emitter-base junction is sufficiently forward-biased, there is an additional delay caused by the time required for minority carriers which are injected into the base to diffuse across the base and be collected at the collector. This delay is usually negligible compared with the delay introduced by the capacitive component. The collector and emitter capacitances vary with the collector-base and emitter-base junction voltages, and increase as the voltage V_{BE} goes positive. An accurate determination of total delay time, therefore, requires knowledge of the nonlinear characteristics of these capacitances.

When the collector current I_c begins to increase, the transistor has made the transition from the cutoff region into the active region. The collector current takes a finite time to reach its final value. This time, called rise time (t_r), is determined by the gain-bandwidth product (f_T), the collector-to-emitter capacitance (C_c), and the static forward current-transfer ratio (h_{FE}) of the transistor. At high collector currents and/or low collector voltages, the effect of this capacitance on rise time is negligible, and the rise time of collector current is inversely proportional to f_T . At low currents and/or high voltages, the effect of gain-bandwidth product is negligible, and the rise time of collector current is directly proportional to the product $R_c C_c$. At intermediate currents and voltages, the rise time is proportional to the sum $(\frac{1}{2}\pi f_T) + R_c C_c$. Under any of the above conditions,

the collector current responds exponentially to a step of base current. If a turn-on base current (I_{B1}) is applied to the device, and the product $I_{B1}h_{FE}$ is less than V_{CC}/R_c , the collector current rises exponentially until it reaches the steady-state value $I_{B1}h_{FE}$. If $I_{B1}h_{FE}$ is greater than V_{CC}/R_c , the collector current rises toward the value $I_{B1}h_{FE}$. The transistor becomes saturated when I_c reaches the value I_{CS} ($\approx V_{CC}/R_c$). At this point, I_c is effectively clamped at the value V_{CC}/R_c .

The rise time, therefore, depends on an exponential function of the ratio $I_{CS}/I_{B1} : h_{FE}$. Because the values of h_{FE} , f_T , and C_c are not constant, but vary with collector voltage and current as the transistor is switching, the rise time as well as the delay time is dependent on nonlinear transistor characteristics.

After the collector current of the transistor has reached a steady-state value I_{CS} , the minority-charge distribution is that shown by curve 3 in Fig. 40. When the transistor is turned off by returning the input pulse to zero, the collector current does not change immediately. This delay is caused by the excess charge in the base and collector regions, which tends to maintain the collector current at the I_{CS} value until this charge decays to an amount equal to that in the active region at the edge of saturation (curve 2 in Fig. 40). The time required for this charge to decay is called the storage time (t_s). The rate of charge decay is determined by the minority-carrier lifetime in the base and collector regions, on the amount of reverse "turn-off" base current (I_{B2}), and on the overdrive "turn-on" current (I_{B1}) which determined how deeply the transistor was driven into saturation. (In non-saturated switching, there is no excess charge in the base region, so that storage time is negligible.)

When the stored charge (Q_s) has decayed to the point where it is equal to that at the edge of saturation, the transistor again enters the

active region and the collector current begins to decrease. This fall-time portion of the collector-current characteristic is similar to the rise-time portion because the transistor is again in the active region. The fall time, however, depends on I_{B2} , whereas the rise time was dependent on I_{B1} . Fall time, like rise time, also depends on f_T and C_C .

The approximate values of I_{B1} , I_{B2} , and I_{CS} for the circuit shown in Fig. 41 are given by:

$$I_{B1} = \frac{V_G - V_{BB} - V_{BE}(\text{sat})}{R_B}$$

$$I_{B2} = \frac{V_{BB} + V_{BE}(\text{sat})}{R_B}$$

$$I_{CS} = \frac{V_{CC} - V_{CE}(\text{sat})}{R_C}$$

Switching Characteristics

The electrical characteristics for a switching transistor, in general, differ from that for a linear-amplifier type of transistor in several respects. The static forward current-transfer ratio h_{FE} and the saturation voltages $V_{CE}(\text{sat})$ and $V_{BE}(\text{sat})$ are of fundamental importance in a switching transistor. The static forward current-transfer ratio determines the maximum amount of current amplification that can be achieved in any given circuit, saturated or non-saturated. The saturation voltages are necessary for the proper dc design of saturated circuits. Consequently, h_{FE} is always specified for a switching transistor, generally at two or more values of collector current. $V_{CE}(\text{sat})$ and $V_{BE}(\text{sat})$ are specified at one or more current levels for saturated transistor applications. Control of these three characteristics determines the performance of a given transistor type over a broad range of operating conditions. For non-saturated applications, $V_{CE}(\text{sat})$ and $V_{BE}(\text{sat})$ need not be specified. For such applications, it is important to specify V_{BE} at specific values of col-

lector current and collector-to-emitter voltage in the active region.

Because the collector and emitter capacitances and the gain-bandwidth product influence switching time, these characteristics are specified for most switching transistors. The collector-base and emitter-base junction capacitances are usually measured at some value of reverse bias and are designated C_{ob} and C_{ib} , respectively. The gain-bandwidth product (f_T) of the transistor is the frequency at which the small-signal forward current-transfer ratio (h_{fe}) is unity. Because this characteristic falls off at 6 dB per octave above the corner frequency, f_T is usually controlled by specifying the h_{fe} at a fixed frequency anywhere from $1/2$ to $1/10 f_T$. Because C_{ob} , C_{ib} , and f_T , vary nonlinearly over the operating range, these characteristics are generally more useful as figures of merit than as controls for determining switching speeds. When the switching speeds in a particular application are of major importance, it is preferable to specify the required switching speeds in the desired switching circuit rather than C_{ob} , C_{ib} , and f_T .

The storage time (t_s) of a transistor is dependent on the stored charge (Q_s) and on the driving current employed to switch the transistor between cutoff and saturation. Consequently, either the stored charge or the storage time under heavy overdrive conditions should be specified. Most recent transistor specifications require that storage time be specified.

Because of the dependence of the switching times on current and voltage levels, these times are determined by the voltages and currents employed in circuit operation.

Dissipation, Current, and Voltage Ratings

Up to this point, no mention has been made of dissipation, current, and voltage ratings for a switching transistor. The maximum continuous

ratings for dissipation and current are determined in the same manner as for any other transistor. In a switching application, however, the peak dissipation and current may be permitted to exceed these continuous ratings depending on the pulse duration, on the duty factor, and on the thermal time constant of the transistor.

Voltage ratings for switching transistors are more complicated. In the basic switching circuit shown in Fig. 41, three breakdown voltages must be considered. When the transistor is turned off, the emitter-base junction is reverse-biased by the voltage $V_{BE}(\text{off})$, (i.e., V_{BB}), the collector-base junction by $V_{CC} + V_{BB}$, and the emitter-to-collector junction by $+V_{CC}$. To assure that none of the voltage ratings for the transistor is exceeded under "off" conditions, the following requirements must be met:

The minimum emitter-to-base breakdown voltage $V_{(BR)EBO}$ must be greater than $V_{BE}(\text{off})$.

The minimum collector-to-base breakdown voltage $V_{(BR)CBO}$ must be greater than $V_{CC} + V_{BE}(\text{off})$.

The minimum collector-to-emitter breakdown voltage $V_{(BR)CERL}$ must be greater than V_{CC} .

$V_{(BR)EBO}$ and $V_{(BR)CBO}$ are always specified for a switching transistor. The collector-to-emitter breakdown voltage $V_{(BR)CEO}$ is usually specified under open-base conditions. The breakdown voltage BV_{CERL} (the subscript "RL" indicates a resistive load in the collector circuit) is generally higher than $V_{(BR)CEO}$. The requirement that $V_{(BR)CEO}$ be greater than V_{CC} is overly pessimistic. The requirement that $V_{(BR)CERL}$ be greater than V_{CC} should be used wherever applicable.

Coupled with the breakdown voltages are the collector-to-emitter and base-to-emitter transistor leakage currents. These leakage currents (I_{CEV} and I_{BEV}) are particularly important considerations at high operating temperatures. The subscript

"V" in these symbols indicates that these leakage currents are specified at a given emitter-to-base voltage (either forward or reverse). In the basic circuit of Fig. 41, these currents are determined by the following conditions:

$$\left. \begin{array}{l} I_{CEV} \\ I_{BEV} \end{array} \right\} \begin{array}{l} V_{CE} = V_{CC} \\ V_{BE} = V_{BE}(\text{off}) = -V_{BB} \end{array}$$

In a switching transistor, these leakage currents are usually controlled not only at room temperature, but also at some higher operating temperature near the upper operational limit of the transistor.

Inductive Switching

Most inductive switching circuits can be represented by the basic equivalent circuit shown in Fig. 43.

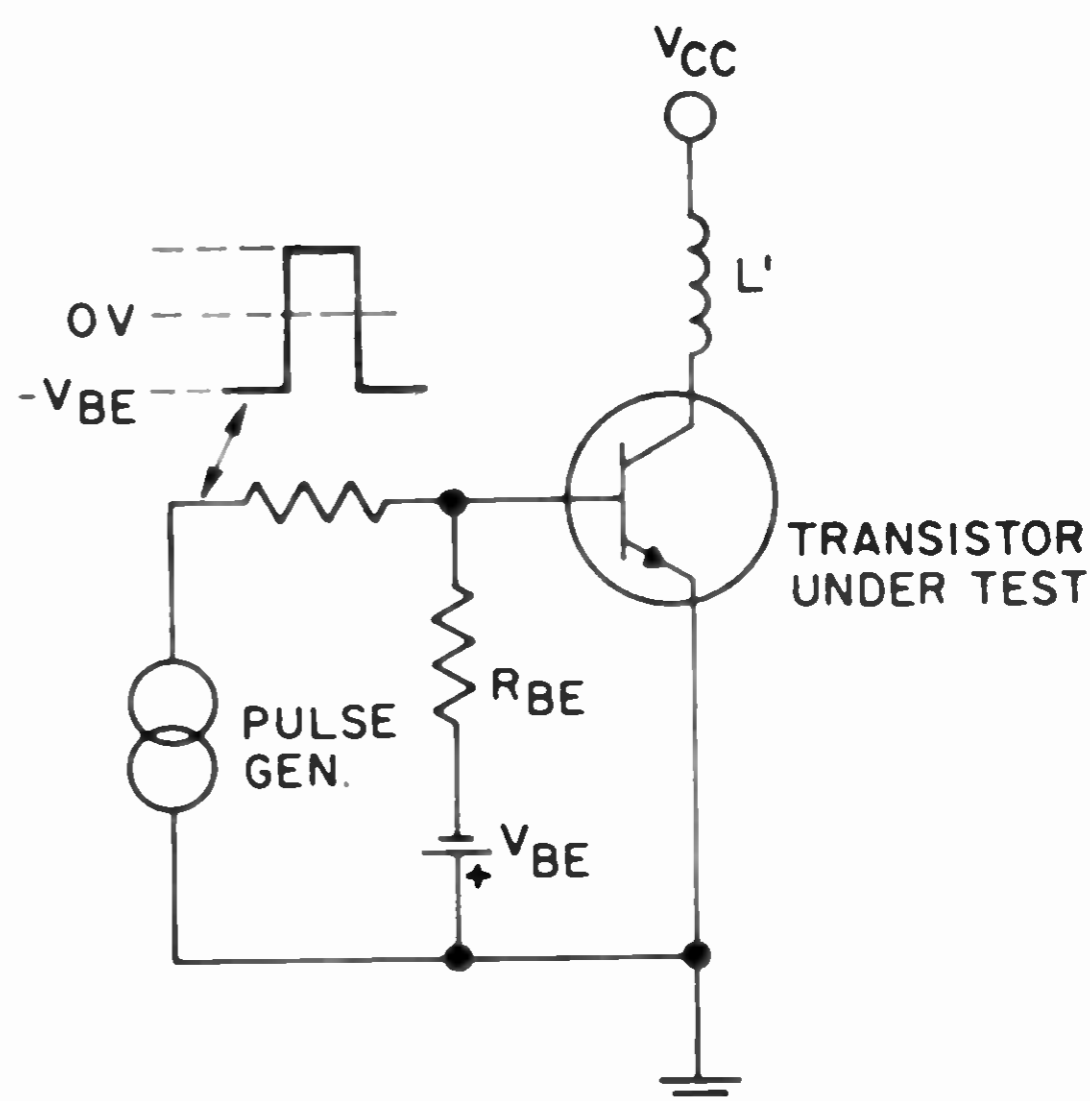


Fig. 43—Basic equivalent circuit for inductive switching circuit.

This type of circuit requires a rapid transfer of energy from the switched inductance to the switching mechanism, which may be a relay, a transistor, a commutating diode, or some other device. Often an accurate calculation of the energy to be dissipated in the switching device is required, particularly if that device is a transistor. If the supply voltage is low compared to the sustaining breakdown voltage of the transistor and if the series resistance of the inductor can be ignored, then the en-

ergy to be dissipated is $\frac{1}{2} LI^2$. This type of rating for a transistor is called "reverse-bias second breakdown." The energy capability of a transistor varies with the load inductance and base-emitter reverse bias. A typical set of ratings which now appear in RCA data sheets is shown on Fig. 44.

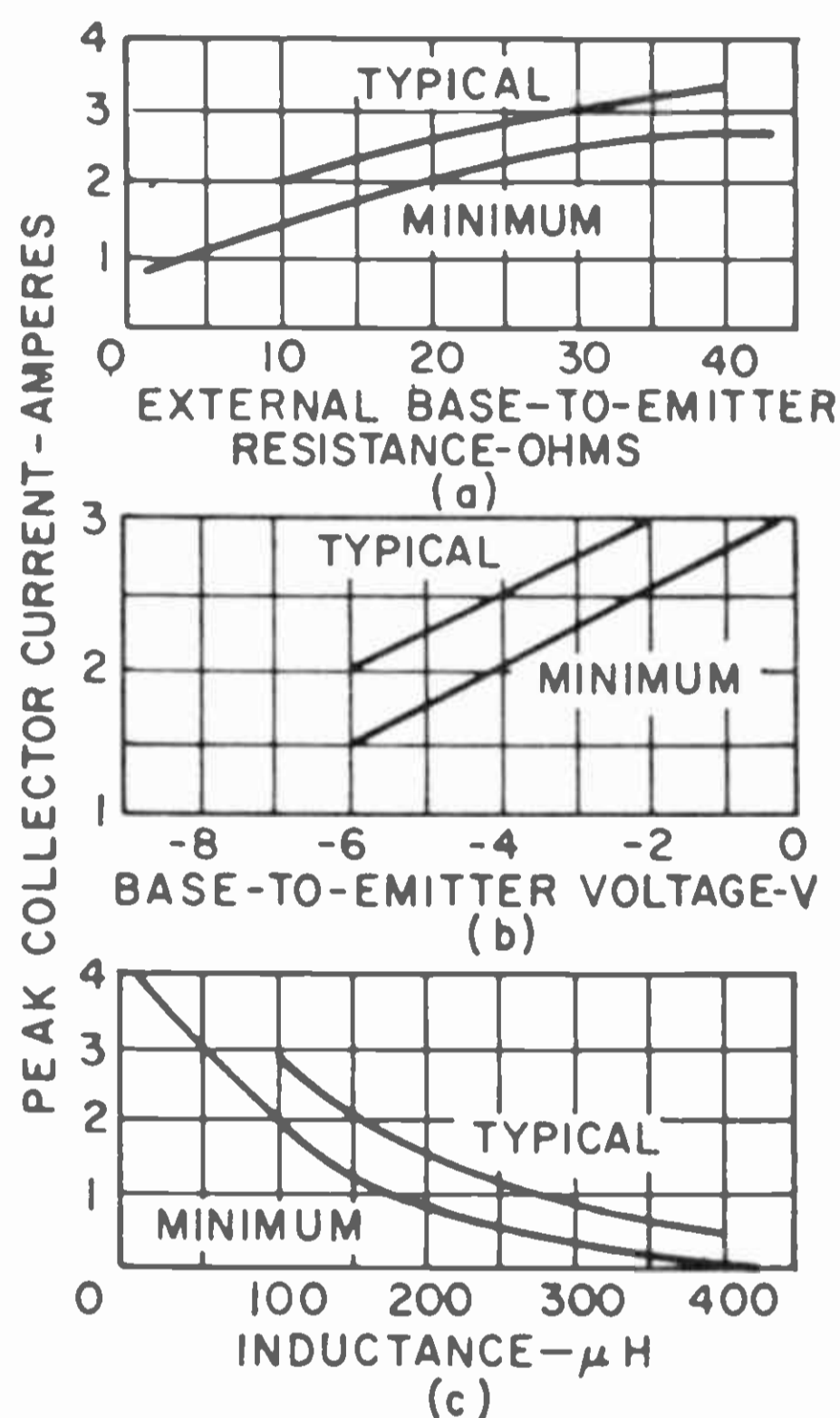


Fig. 44—Typical reverse-bias second-breakdown (E_s/v) rating curves.

TRANSIENT EFFECTS

The generation of static charge in dry weather is harmful to all transistors, and can cause permanent damage or catastrophic failure in the case of high-speed devices. The most obvious precaution against such damage is humidity control in storage and operating areas. In addition, it is desirable that transistors be stored and transported in metal trays rather than in polystyrene foam "snow". During testing and installation, both the equipment and the operator should be grounded, and all power should be turned off when the device is inserted into the

socket. Grounded plates may also be used for stockpiling of transistors prior to or after testing, or for use in testing ovens or on operating life racks. Further protection against static charges can be provided by use of partially conducting floor planes and non-insulating footwear for all personnel.

Environmental temperature also affects performance. Variations of as little as 5 per cent can cause changes of as much as 50 per cent in the saturation current of a transistor. Some test operators can cause marked changes in measurements of saturation current because the heat of their hands affects the transistors they work on. Precautions against temperature effects include air-conditioning systems, use of finger cots in handling of transistors (or use of pliers or "plug-in boards" to eliminate handling), and accurate monitoring and control of temperature near the devices. Prior to testing, it is also desirable to allow sufficient time (about 5 minutes) for a transistor to stabilize if it has been subjected to temperature much higher or lower than normal room temperature (25°C).

Although transient rf fields are not usually of sufficient magnitude to cause permanent damage to transistors, they can interfere with accurate measurement of characteristics at very low signal levels or at high frequencies. For this reason, it is desirable to check for such radiation periodically and to eliminate its causes. In addition, sensitive measurements should be made in shielded screen rooms if possible. Care must also be taken to avoid the exposure of transistors to other ac or magnetic fields.

Many transistor characteristics are sensitive to variations in temperature, and may change enough at high operating temperatures to affect circuit performance. Fig. 45 illustrates the effect of increasing temperature on the common-emitter forward current-transfer ratio (beta), the dc collector-cutoff current, and the in-

put and output impedances. To avoid undesired changes in circuit operation, it is recommended that transistors be located away from heat

sources in equipment, and also that provisions be made for adequate heat dissipation and, if necessary, for temperature compensation.

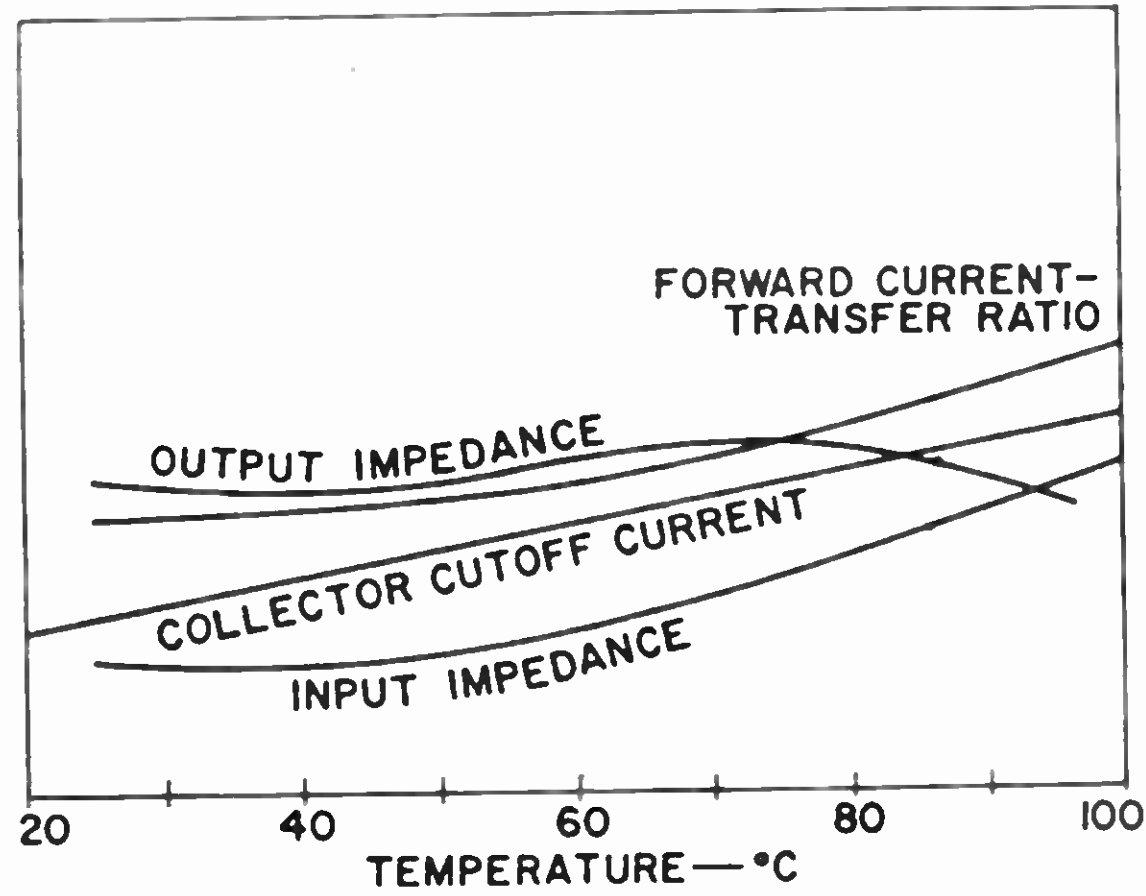


Fig. 45—Variation of transistor characteristics with temperature.

MOS Field-Effect Transistors

Field-effect transistors combine the inherent advantages of solid-state devices (small size, low power consumption, and mechanical ruggedness) with a very high input impedance and a square-law transfer characteristic that is especially desirable for low cross-modulation in rf amplifiers. Unlike the other transistors described in this Manual, which are bipolar devices (i.e., performance depends on the interaction of two types of charge carriers, holes and electrons), field-effect transistors are unipolar devices (i.e., operation is basically a function of only one type of charge carrier, holes in p-channel devices and electrons in n-channel devices).

Early models of field-effect transistors used a reverse-biased semiconductor junction for the control electrode. In MOS (metal-oxide-semiconductor) field-effect transistors, a metal control "gate" is separated from the semiconductor "channel" by an insulating oxide layer. One of the major features of the metal-oxide-semiconductor structure is that the very high input resistance of MOS transistors (unlike that of junction-gate-type field-effect transistors) is not affected by the polarity of the bias on the control (gate) electrode. In addition, the leakage currents associated with the insulated control electrode are relatively unaffected by changes in ambient temperature. Because of their unique properties, MOS field-effect transistors are particularly well

suited for use in such applications as voltage amplifiers, rf amplifiers, and voltage-controlled attenuators.

THEORY OF OPERATION

The operation of field-effect devices can be explained in terms of a charge-control concept. The metal control electrode, which is called a gate, acts as a charge-storage or control element. A charge placed on the gate induces an equal but opposite charge in the semiconductor layer, or channel, located beneath the gate. The charge induced in the channel can then be used to control the conduction between two ohmic contacts, called the source and the drain, made to opposite ends of the channel.

In the junction-gate type of field-effect transistor, a p-n junction is used for the gate or control electrode, as shown in Fig. 46. When this junction is reverse-biased, it functions as a charge-control electrode. Under steady-state condi-

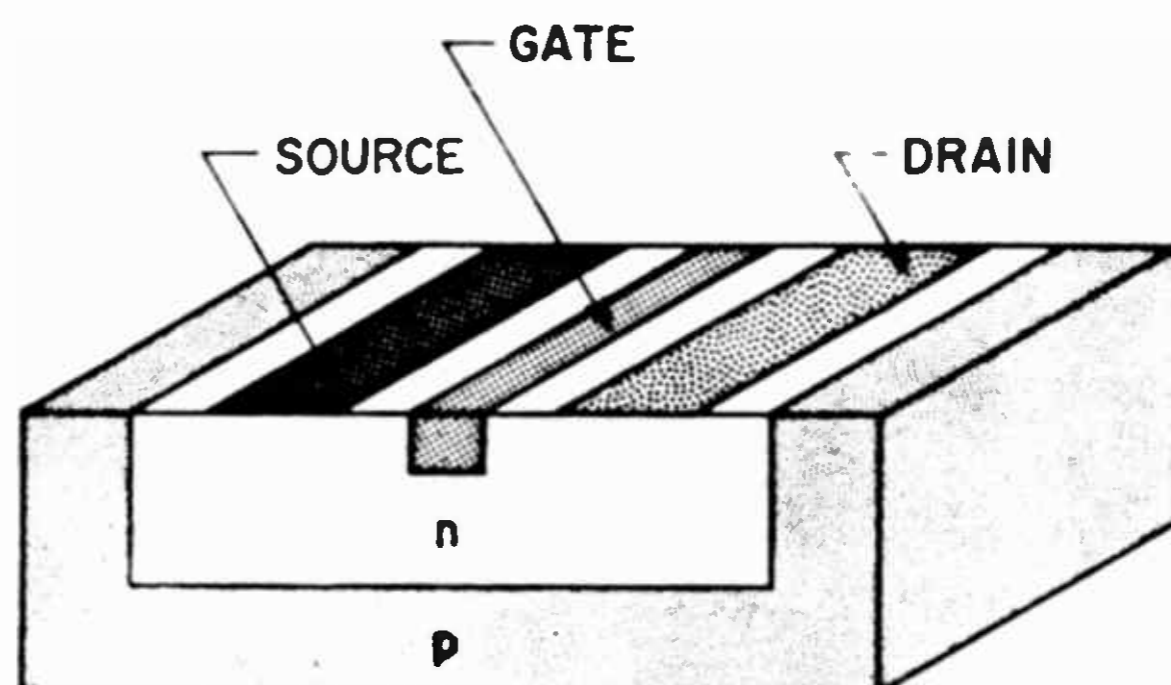


Fig. 46—Structure of p-n junction field-effect transistor.

tions, only leakage currents flow in the gate circuit and thus the device has a high input resistance. When the junction gate is forward-biased, however, the input resistance drops sharply, there is appreciable input current, and power gain decreases significantly.

The MOS type of field-effect transistor uses a metal gate electrode separated from the semiconductor material by an insulator, as shown in Fig. 47. Like the p-n junction, this insulated-gate electrode can deplete the source-to-drain channel of active carriers when suitable bias voltages are applied. However, the insulated-gate electrode can also increase the conductivity of the channel without increasing steady-state input current or reducing power gain.

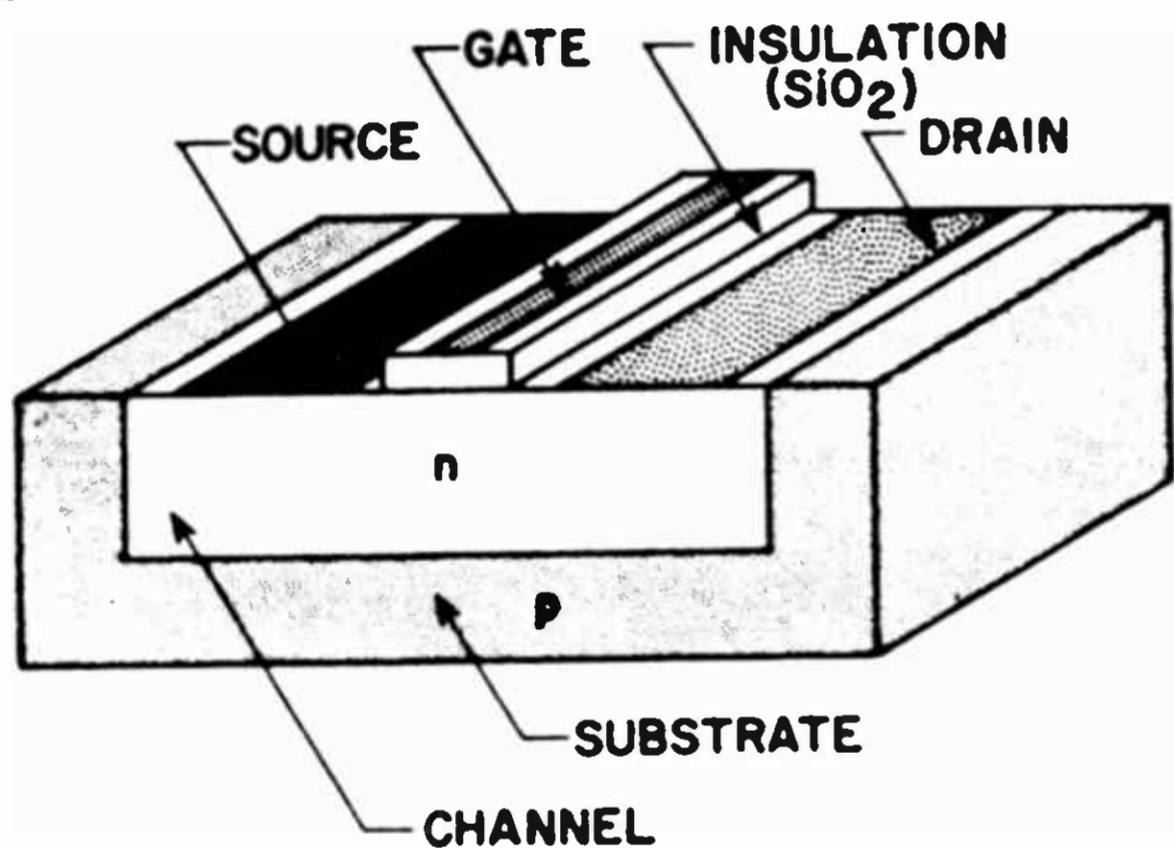


Fig. 47—Structure of an MOS field-effect transistor.

The two basic types of MOS field-effect transistors are the depletion type and the enhancement type. In the depletion type, charge carriers are present in the channel and the channel is conductive when no bias voltage is applied to the gate. A reverse gate voltage is one which depletes this charge and thereby reduces the channel conductivity. A forward gate voltage draws more charge carriers into the channel and thus increases the channel conductivity. In the enhancement type, the gate must be forward-biased to produce active carriers and permit conduction through the channel. No useful channel conductivity exists at either zero or reverse gate bias.

Because MOS transistors can be

made to utilize either electron conduction (n-channel) or hole conduction (p-channel), four distinct types of MOS field-effect transistors are possible. As shown in Fig. 48, the

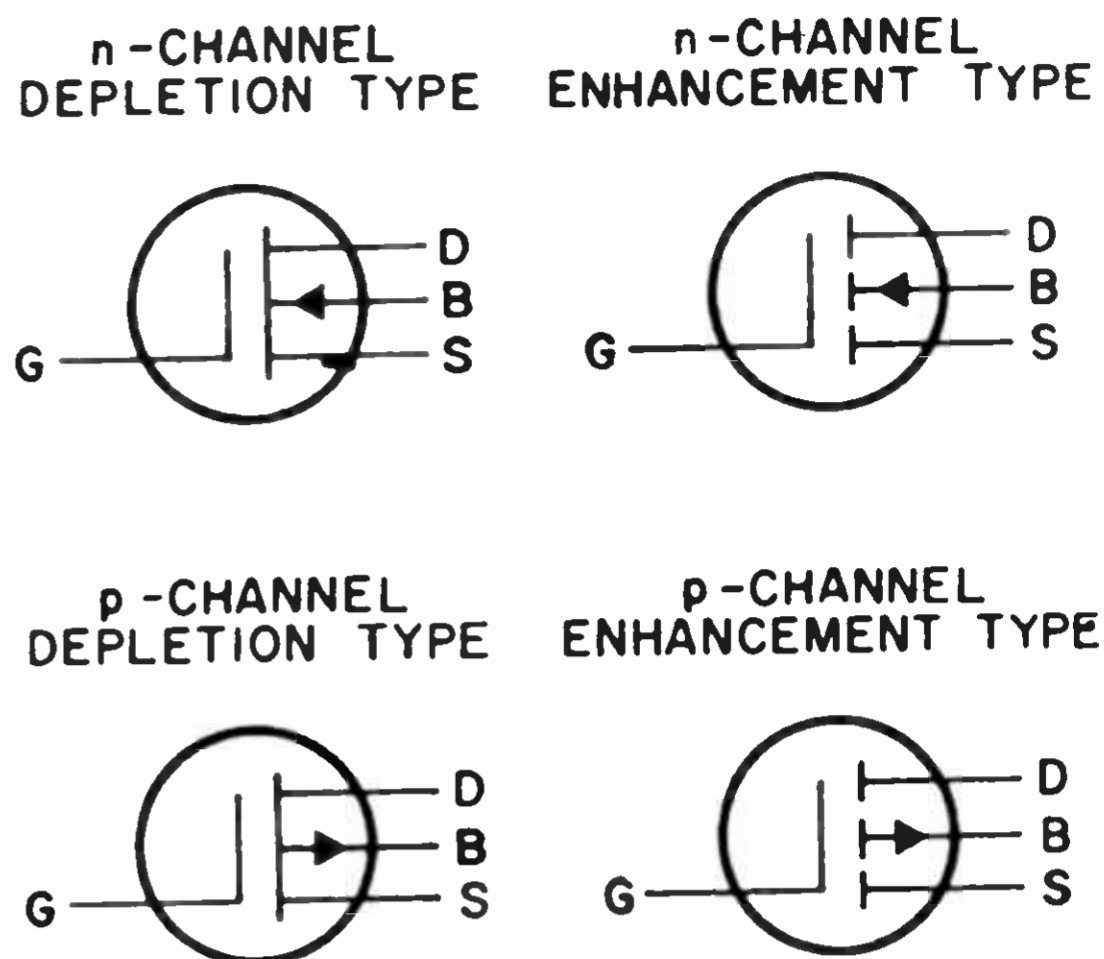


Fig. 48—Schematic symbols for MOS transistors (G = gate, D = drain, B = active bulk, S = source).

schematic symbol for an MOS transistor indicates whether it is n-channel or p-channel, depletion-type or enhancement-type. The direction of the arrowhead in the symbol identifies the n-channel device (arrow pointing toward the channel) or the p-channel device (arrow pointing away from the channel). The channel line itself is made solid to identify the "normally ON" depletion-type, or is interrupted to identify the "normally OFF" enhancement type.

Fig. 49 shows a cross-section view of an n-channel enhancement-type MOS transistor (reversal of n-type and p-type regions would produce a p-channel enhancement-type transistor). This type of transistor is normally non-conducting until a sufficient voltage of the correct

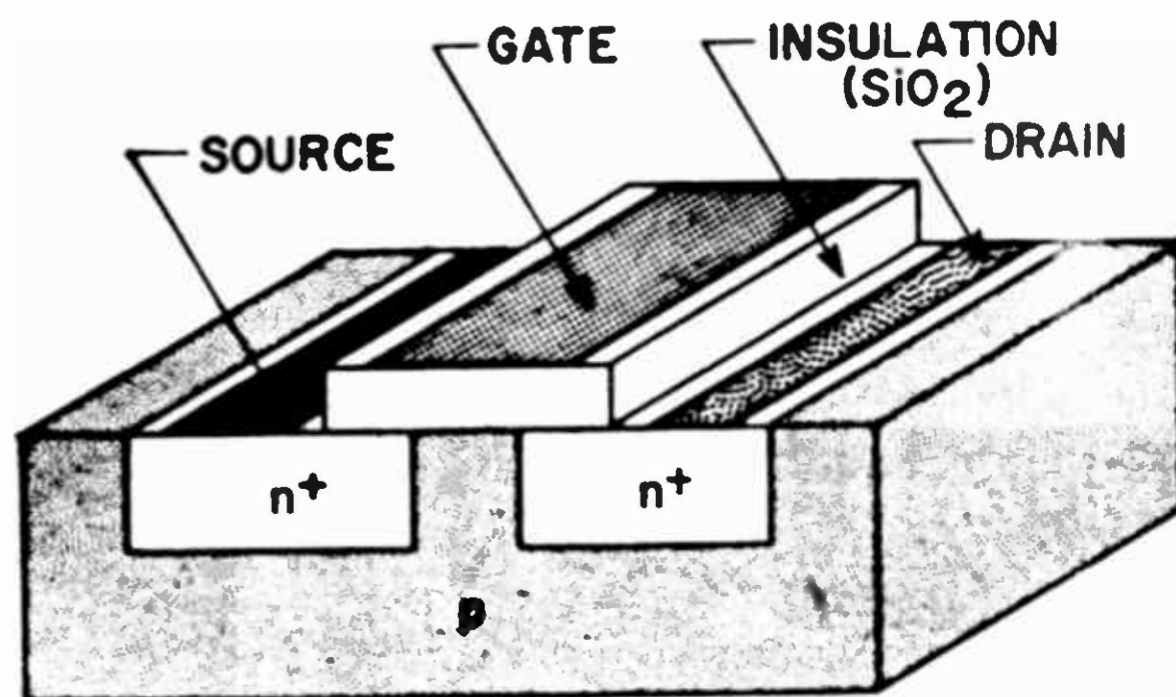


Fig. 49—Structure of n-channel enhancement-type MOS transistor.

polarity is applied to the gate electrode. When a positive bias voltage is applied to the gate of an n-channel enhancement transistor, electrons are drawn into the channel region beneath the gate. If sufficient voltage is applied, this channel region changes from p-type to n-type and provides a conduction path between the n-type source and the n-type drain regions. (In a p-channel enhancement transistor, the application of negative bias voltage draws holes into the region below the gate so that this channel region changes from n-type to p-type and again provides a source-to-drain conduction path.) Effectively, the increase in gate voltage causes the forward transfer characteristic to shift along the gate-voltage axis. Because of this feature, enhancement-type MOS transistors are particularly suitable for switching applications.

In a depletion-type MOS transistor, the channel region between the source and the drain is made of material of the same conductivity type as both the source and drain, as was shown in Fig. 47. This structure can provide substantial drain current even when no gate bias voltage is applied.

In enhancement-type transistors, the gate electrode must cover the entire region between the source and the drain so that the applied gate voltage can induce a conductive channel between them. In depletion-type transistors, however, the gate can be "offset" from the drain region to achieve a substantial reduction in feedback capacitance and an over-all improvement in amplifier circuit stability.

FABRICATION

The fabrication techniques used to produce MOS transistors are similar to those used for modern high-speed silicon bipolar transistors. The starting material for an n-channel transistor is a lightly doped p-type silicon wafer. (Reversal of p-type and n-type materials referred to in

this description produces a p-channel transistor.) After the wafer is polished on one side and oxidized in a furnace, photolithographic techniques are used to etch away the oxide coating and expose bare silicon in the source and drain regions. The source and drain regions are then formed by diffusion in a furnace containing an n-type impurity (such as phosphorus). If the transistor is to be an enhancement-type device, no channel diffusion is required. If a depletion-type transistor is desired, an n-type channel is formed to bridge the space between the diffused source and drain.

The wafer is then oxidized again to cover the bare silicon regions, and a second photolithographic and etching step is performed to remove the oxide in the contact regions. After metal is evaporated over the entire wafer, another photolithographic and etching step removes all metal not needed for the ohmic contacts to the source, drain, and gate. The individual transistor chips are then mechanically separated and mounted on individual headers, connector wires are bonded to the metalized regions, and each unit is hermetically sealed in its case in an inert atmosphere. After testing, the external leads of each device are physically shorted together to prevent electrostatic damage to the gate insulation during branding and shipping.

ELECTRICAL CHARACTERISTICS

The basic current-voltage relationship for a depletion-type MOS transistor operating in the common-source configuration is shown in Fig. 50. At low drain-to-source potentials and with the gate returned to the source ($V_G = 0$), the resistance of the channel is essentially constant and current varies linearly with voltage, as illustrated in region A-B. As the drain current is increased beyond point B, the voltage (IR) drop in the channel produces a progressively greater voltage dif-

ference between the gate and points in the channel successively closer to the drain. As this potential difference between gate and channel increases, the channel is depleted of carriers (becomes "constricted")

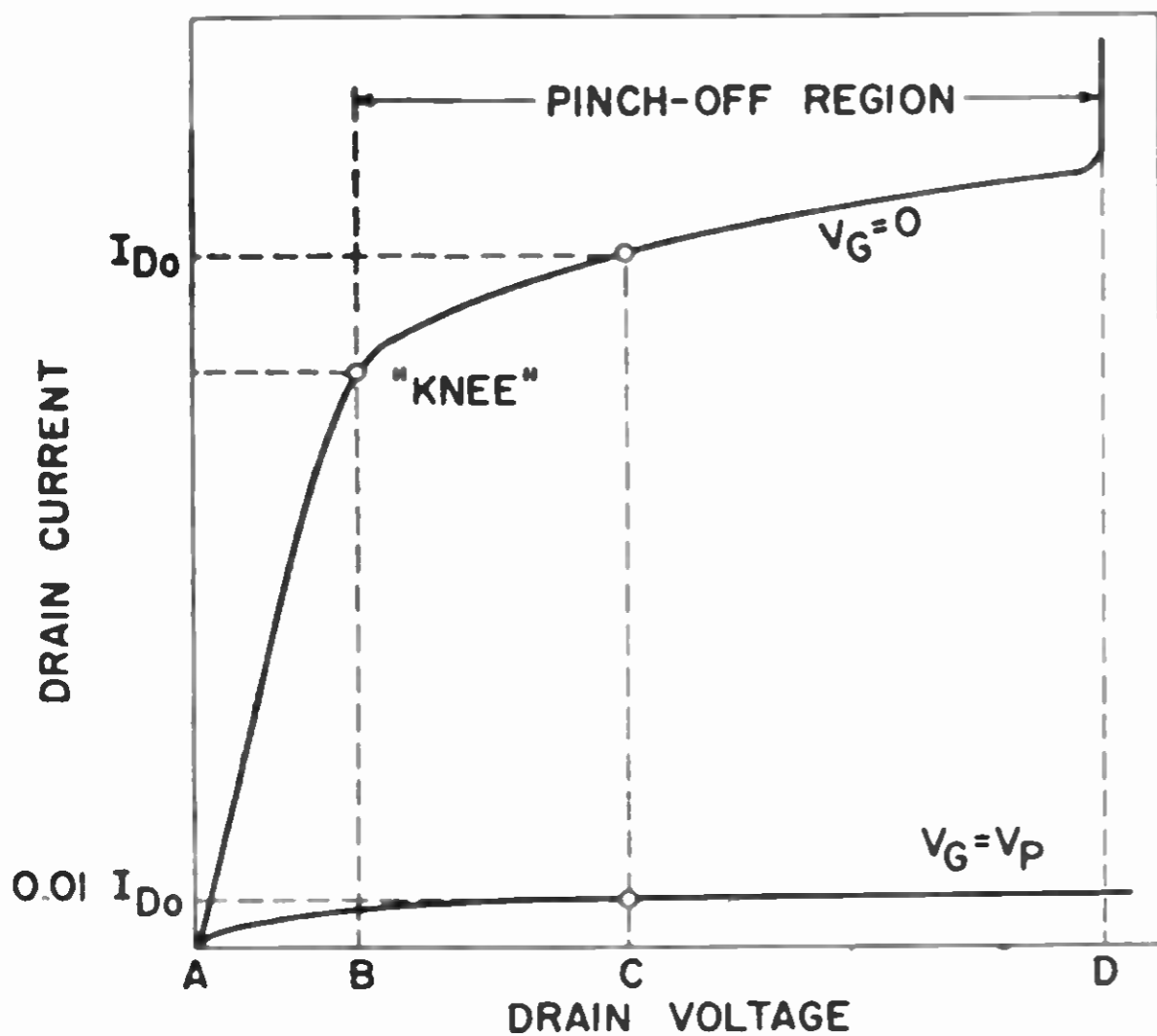


Fig. 50—Basic current-voltage relationship for a depletion-type MOS transistor.

and drain current increases much more slowly with further increases in drain-to-source voltage, as shown in region B-C. Further increases in drain-to-source voltage beyond point C produce no change in drain current until point D is reached. This condition leads to the description of region B-D as the "pinch-off" region. Beyond point D, the transistor enters the "breakdown" region, and the drain current may increase excessively. (The upper curve in Fig. 50 also applies to enhancement-type transistors provided the gate voltage V_G is large enough to produce channel conduction.)

The channel of an MOS transistor may achieve self pinch-off as a result of the intrinsic IR drop alone, or it may be pinched off by a combination of intrinsic IR drop and an external voltage applied to the gate, or by an external gate voltage alone which has the same magnitude as the self pinch-off IR drop V_P . In any case, channel pinch-off occurs when the sum of the intrinsic IR drop and the extrinsic gate voltage reaches V_P . The pinch-off voltage V_P is usually defined as the gate

cutoff voltage $V_G(\text{off})$ that reduces the drain current to between 0.1 and 1 per cent of its zero-gate-voltage value at a specified drain-to-source voltage (which must be the "knee" voltage, point B in Fig. 50 of the zero-gate-voltage output characteristic).

The pinch-off region between points B and D in Fig. 50 is the region in which MOS transistors are especially useful as high-impedance voltage amplifiers. In the ohmic region between points A and B, the linear variation in channel resistance makes the device useful in voltage-controlled resistor applications such as the chopper unit at the input of some dc amplifiers.

Typical output-characteristic curves for n-channel MOS transistors are shown in Fig. 51 (For p-channel

ENHANCEMENT TYPE

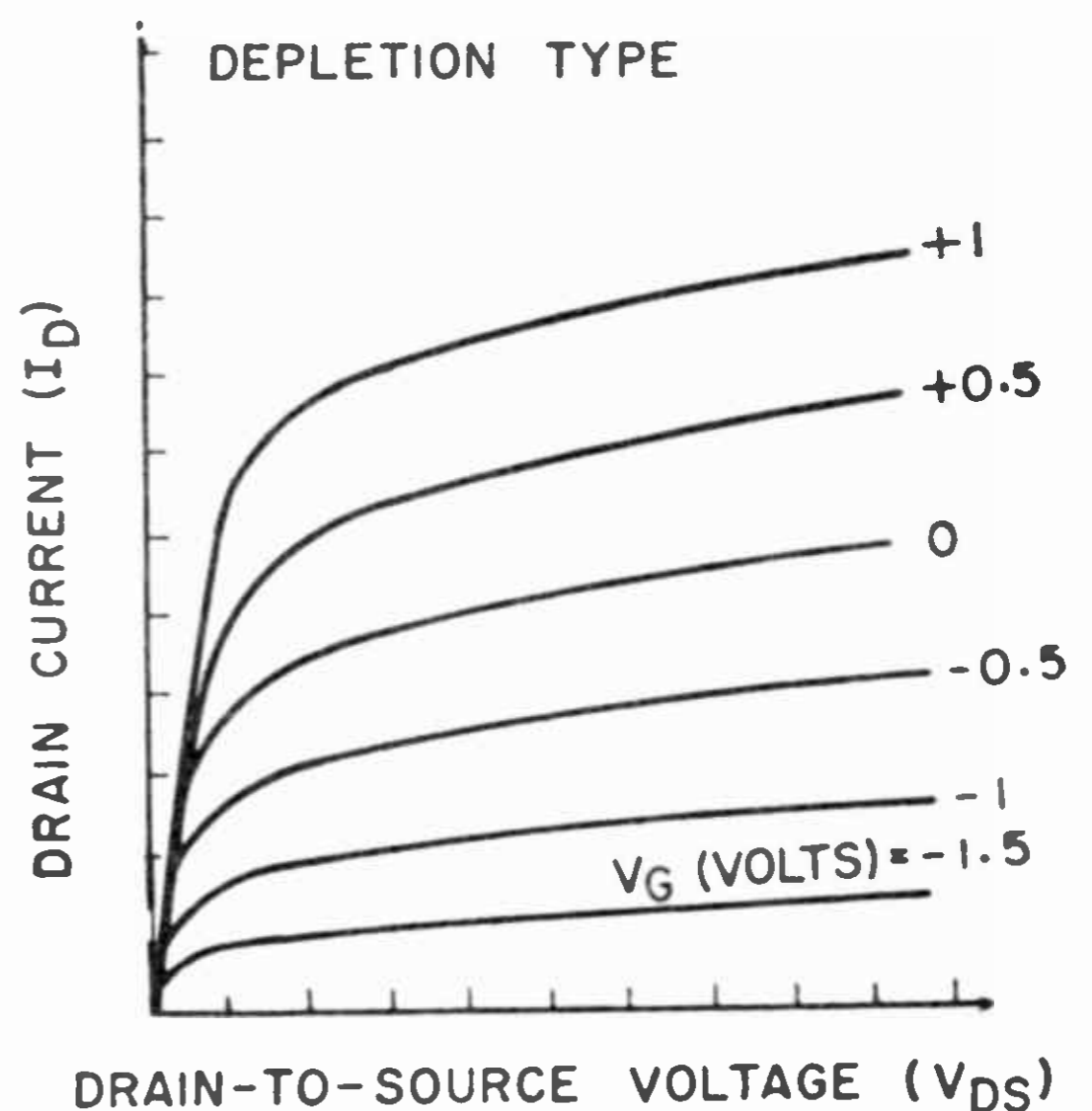
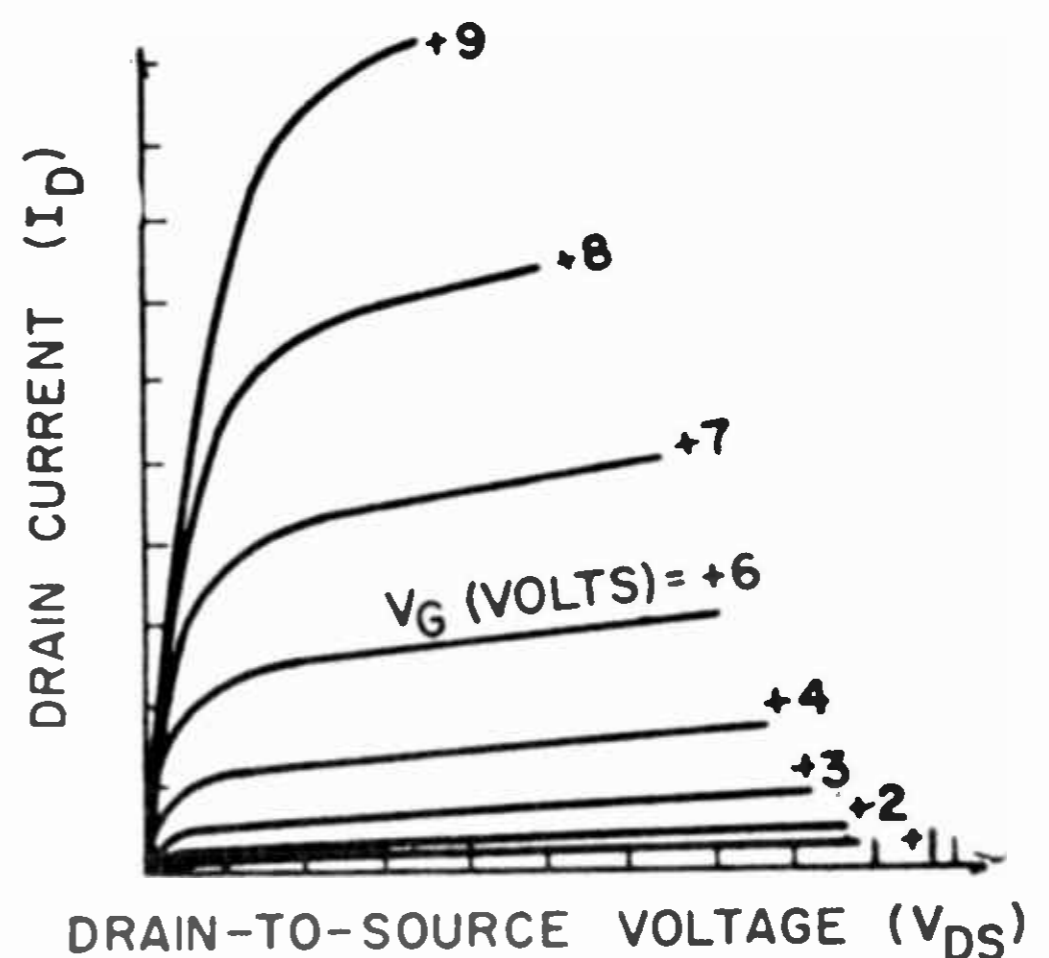


Fig. 51—Typical output-characteristic curves for n-channel MOS transistors.

transistors, the polarity of the voltages and current is reversed.) In the pinch-off region, the dynamic output resistance r_{os} of the transistor may be approximated from the slope of the output-characteristic curve at any given set of conditions.

Typical transfer characteristics for n-channel MOS transistors are shown in Fig. 52. (Again, polarities would be reversed for p-channel devices.) The threshold voltage shown in Fig. 52 is an important parameter for enhancement-type transistors because it provides a desirable region of noise immunity for switching applications.

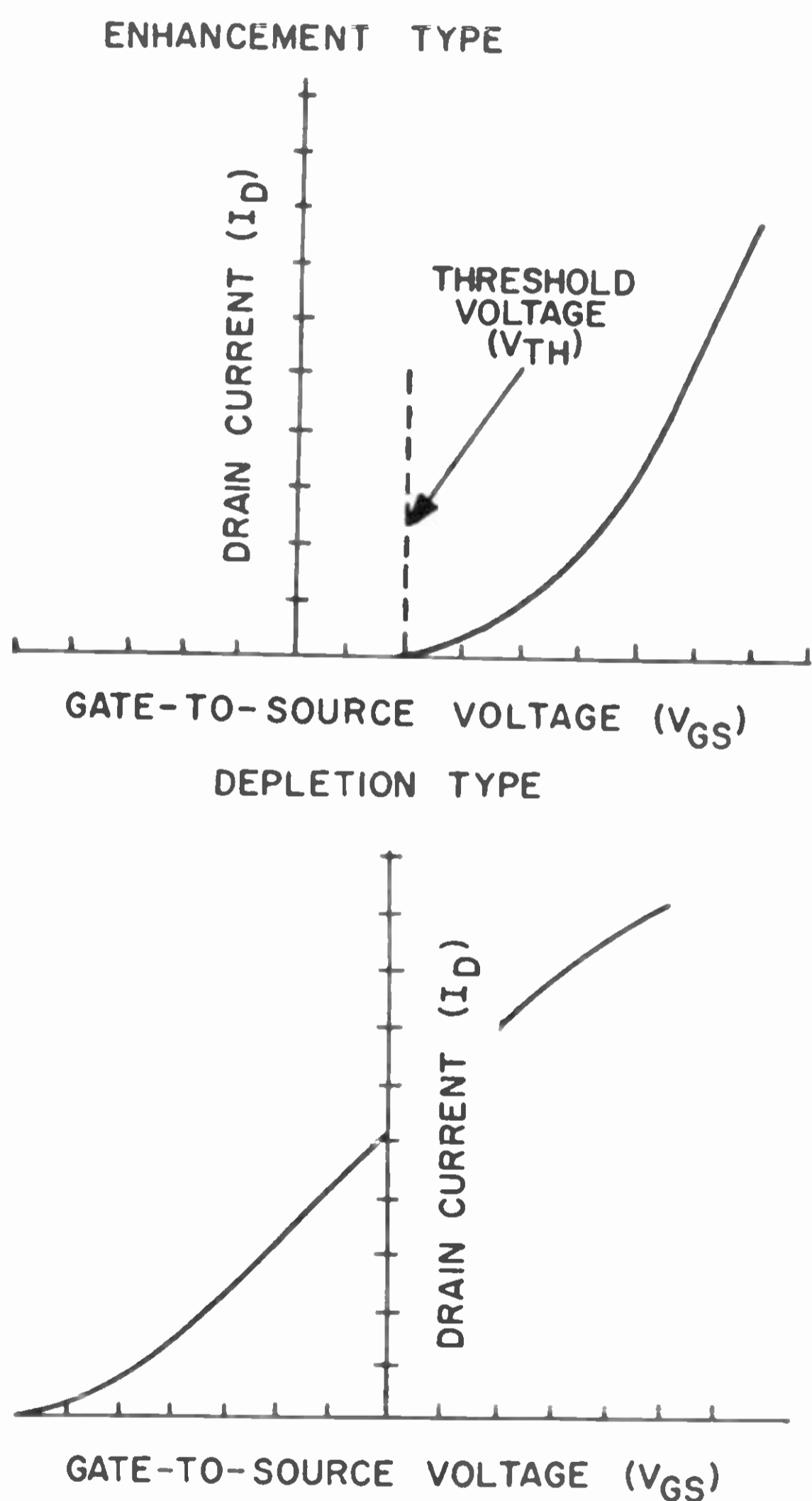


Fig. 52—Typical transfer characteristics for n-channel MOS transistors.

GENERAL CIRCUIT CONFIGURATIONS

There are three basic single-stage amplifier configurations for MOS

transistors: common-source, common-gate, and common-drain. Each of these configurations provides certain advantages in particular applications.

The **common-source** arrangement shown in Fig. 53 is most frequently used. This configuration provides a high input impedance, medium to high output impedance, and voltage gain greater than unity. The input signal is applied between gate and source, and the output signal is taken between drain and source. The voltage gain without feedback, A , for the common-source circuit may be determined as follows:

$$A = \frac{g_{fs} r_{os} R_L}{r_{os} + R_L}$$

where g_{fs} is the gate-to-drain forward transconductance of the transistor, r_{os} is the common-source output resistance, and R_L is the effective load resistance. The addition of an unbypassed source resistor to

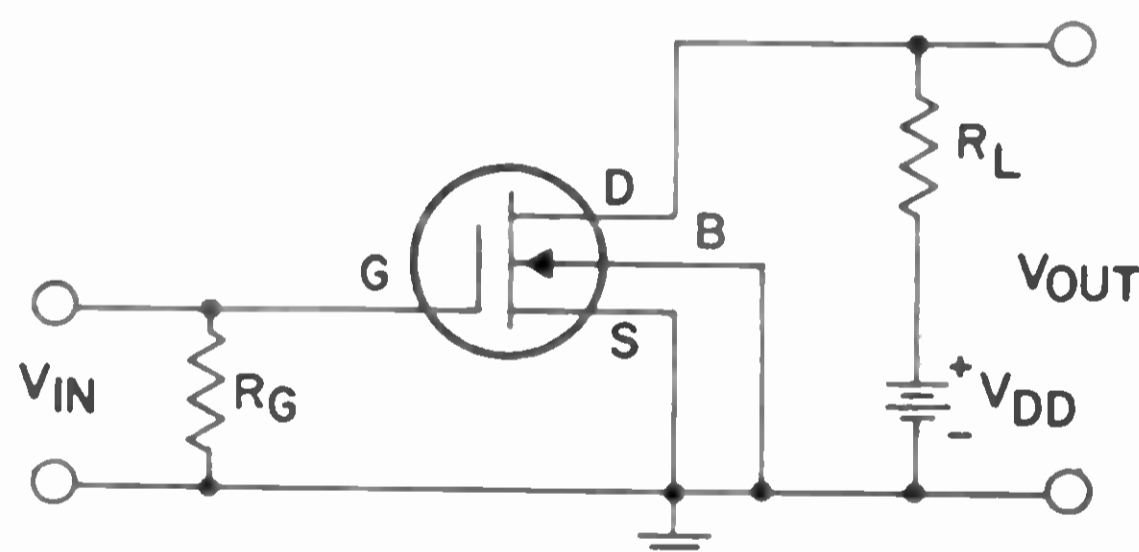


Fig. 53—Basic common-source circuit for MOS field-effect transistors.

the circuit of Fig. 53 produces negative voltage feedback proportional to the output current. The voltage gain with feedback, A' , for a common-source circuit is given by

$$A' = \frac{g_{fs} r_{os} R_L}{r_{os} + (g_{fs} r_{os} + 1) R_s + R_L}$$

where R_s is the total unbypassed source resistance in series with the source terminal. The common-source output impedance with feedback, Z_o , is increased by the unbypassed source resistor as follows:

$$Z_o = r_{os} + (g_{fs} r_{os} + 1) R_s$$

The **common-drain** arrangement, shown in Fig. 54, is also frequently referred to as a **source-follower**. In this configuration, the input impedance is higher than in the common-source configuration, the output impedance is low, there is no polarity reversal between input and output, the voltage gain is always less than unity, and distortion is low. The source-follower is used in applications which require reduced input-circuit capacitance, downward impedance transformation, or increased input-signal-handling capability. The input signal is effectively injected between gate and drain, and the output is taken between source and drain. The circuit inherently has 100-per-cent negative

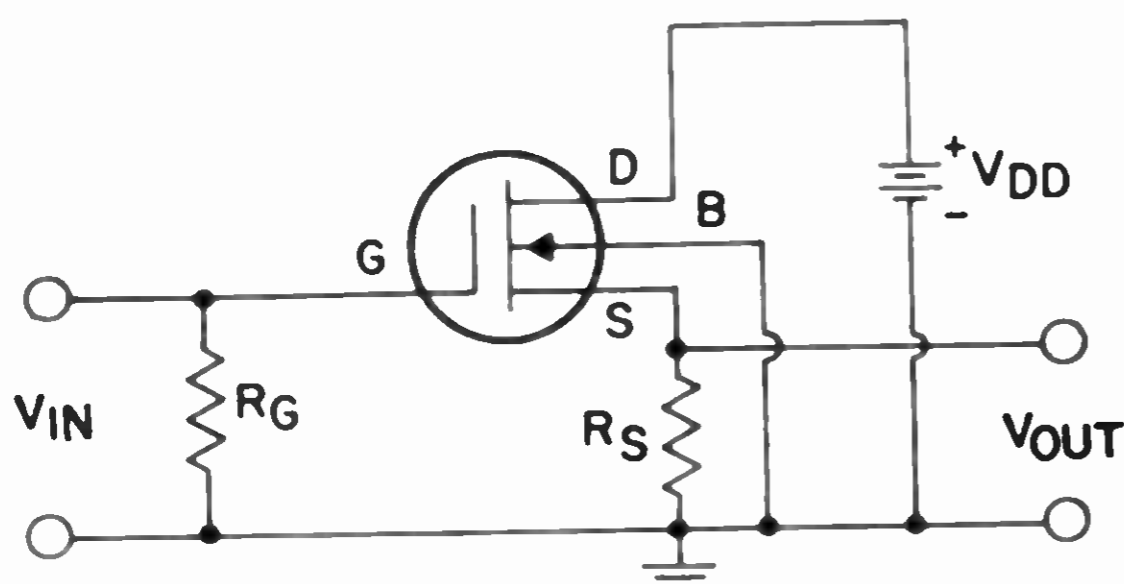


Fig. 54—Basic common-drain (or source-follower) circuit for MOS transistors.

voltage feedback; its gain A' is given by

$$A' = \frac{R_s}{\frac{\mu + 1}{\mu} R_s + \frac{1}{g_{fs}}}$$

Because the amplification factor (μ) of an MOS transistor is usually much greater than unity, the equation for gain in the source-follower can be simplified as follows:

$$A' = \frac{g_{fs} R_s}{1 + g_{fs} R_s}$$

For example, if it is assumed that the gate-to-drain forward transconductance g_{fs} is 2000 micromhos (2×10^{-3} mho) and the unbypassed source resistance R_s is 500 ohms, the stage gain A' is 0.5. If the same source resistance is used with a transistor having a transconductance

of 10,000 micromhos (1×10^{-2} mho), the stage gain increases to 0.83.

When the resistor R_G is returned to ground, as shown in Fig. 54, the input resistance R_i of the source-follower is equal to R_G . If R_G is returned to the source terminal, however, the effective input resistance R_i' is given by

$$R_i' = \frac{R_G}{1 - A'}$$

where A' is the voltage amplification of the stage with feedback. For example, if R_G is one megohm and A' is 0.5, the effective resistance R_i' is two megohms.

If the load is resistive, the effective input capacitance C_i' of the source-follower is reduced by the inherent voltage feedback and is given by

$$C_i' = c_{gd} + (1 - A') c_{gs}$$

where c_{gd} and c_{gs} are the intrinsic gate-to-drain and gate-to-source capacitances, respectively, of the MOS transistor. For example, if a typical MOS transistor having a c_{gd} of 0.3 picofarad and a c_{gs} of 5 picofarads is used, and if A' is equal to 0.5, then C_i' is reduced to 2.8 picofarads.

The effective output resistance R_o' of the source-follower stage is given by

$$R_o' = \frac{r_{os} R_s}{(g_{fs} r_{os} + 1) R_s + r_{os}}$$

where r_{os} is the transistor common-source output resistance in ohms. For example, if a unit having a gate-to-drain forward transconductance g_{fs} of 2000 micromhos and a common-source output resistance r_{os} of 7500 ohms is used in a source-follower stage with an unbypassed source resistance R_s of 500 ohms, the effective output resistance R_o' of the source-follower stage is 241 ohms.

The source-follower output capacitance C_o' may be expressed as follows:

$$C_o' = c_{ds} + c_{gs} \left(\frac{1 - A'}{A'} \right)$$

where c_{ds} and c_{gs} are the intrinsic drain-to-source and gate-to-source capacitances, respectively, of the MOS transistor. If A' is equal to 0.5 (as assumed for the sample input-circuit calculations), C_o' is reduced to the sum of c_{ds} and c_{gs} .

The common-gate circuit, shown in Fig. 55, is used to transform from a low input impedance to a high output impedance. The input impedance of this configuration has approximately the same value as the output impedance of the source-follower circuit. The common-gate circuit is also a desirable configuration

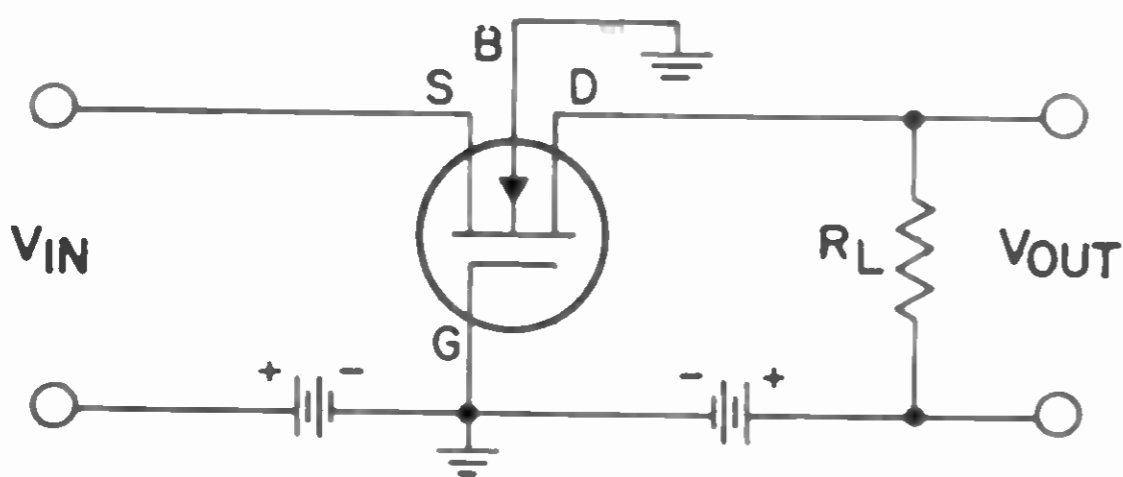


Fig. 55—Basic common-gate circuit for MOS transistors.

for high-frequency applications because its relatively low voltage gain makes neutralization unnecessary in most cases. The common-gate voltage gain, A , is given by

$$A = \frac{(g_{fs} r_{os} + 1) R_L}{(g_{fs} r_{os} + 1) R_G + r_{os} + R_L}$$

where R_G is the resistance of the input-signal source. For a typical

MOS transistor ($g_{fs} = 2000$ micromhos, $r_{os} = 7500$ ohms) and with $R_L = 2000$ ohms and $R_G = 500$ ohms, the common-gate voltage gain is 1.8. If the value of R_G is doubled, the voltage gain is reduced to 1.25.

HANDLING CONSIDERATIONS

Performance of MOS transistors depends on the relative perfection of the insulating layer between the control electrode (gate) and the active channel. If this layer is punctured by inadvertent application of excess voltage to the external gate connection, the damage is irreversible. If the damaged area is small enough, the additional leakage may not be noticed in most applications. However, greater damage may degrade the device to the leakage levels associated with junction-gate-type field-effect transistors. It is very important, therefore, that appropriate precautions be taken to insure that MOS transistor gate-voltage ratings are not exceeded. Special handling considerations for these devices are discussed in the section on Testing and Mounting.

Thyristors

The term **thyristor** is the generic name for semiconductor devices that have characteristics similar to those of thyratron tubes. Basically, this group includes bistable semiconductor devices that have two or more junctions (three or more semiconductor layers) and that can be switched between conducting states (from OFF to ON or from ON to OFF) within at least one quadrant of the principal voltage-current characteristic. Reverse-blocking triode thyristors, commonly called silicon controlled rectifiers (SCR's), and bidirectional triode thyristors, usually referred to as triacs, have three electrodes and are switched between states by a current pulse applied to the gate terminal. The bidirectional trigger diode, commonly called a diac, has only two electrodes. This device has no gate electrode but may be switched from an OFF state to an ON state for either polarity of applied voltage. The discussions in this section deal primarily with the SCR and the triac, their operation, electrical characteristics, and ratings. A brief description is also given of the operation of the diac and its chief function in triac phase-control circuits.

SILICON CONTROLLED RECTIFIERS

A silicon controlled rectifier (SCR) is basically a four-layer p-n-p-n device that has three electrodes (a cathode, an anode, and a control electrode called the gate). Fig. 56 shows the junction diagram, principal voltage-current characteristic, and schematic symbol for an SCR.

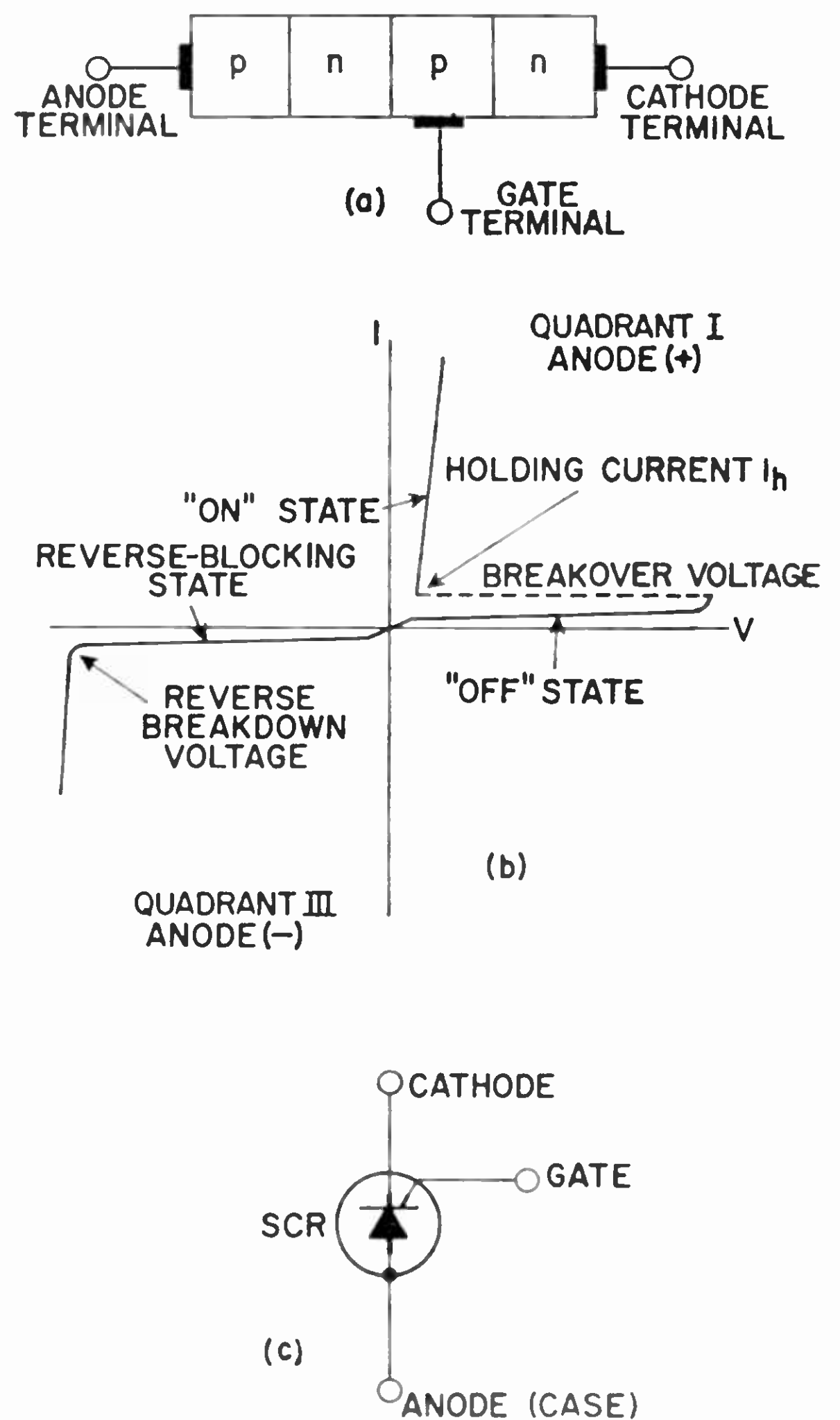


Fig. 56—(a) Junction diagram, (b) principal voltage-current characteristic, and (c) schematic symbol for an SCR thyristor.

Fig. 56(b) shows that under forward-bias conditions (anode positive with respect to cathode) the SCR has two states. At low values of forward bias, the SCR exhibits a very high impedance; in this forward-blocking or OFF state, a small forward current, called the forward OFF-state current, flows through the device. As the forward bias is increased, however, a voltage point is reached at which the forward cur-

rent increases rapidly and the SCR switches to the ON state. This value of voltage is called the breakover voltage. When the SCR is in the ON state, the forward current is limited primarily by the impedance of the external circuit.

Under reverse bias (anode negative with respect to cathode), the SCR exhibits a very high internal impedance, and only a small amount of current, called the reverse blocking current, flows through the device. This current remains very small and the device remains in this OFF state unless the reverse voltage exceeds the reverse-breakdown-voltage limitation. At this point, the reverse current increases rapidly, and the SCR undergoes thermal runaway, a condition that normally causes irreversible damage to the device. The value of reverse breakdown voltage differs for individual SCR types, but is approximately 100 volts greater than the forward breakover voltage for most types. Under forward-bias conditions, the breakover voltage of the SCR can be controlled or varied by application of a current pulse to the gate electrode, as shown in Fig. 57. As the amplitude of the gate current pulse is increased, the breakover voltage for the SCR decreases until the curve closely resembles that of a rectifier. In normal operation, the SCR is operated with critical values well below the breakover voltage and is made to switch on by gate signals of sufficient magnitude to assure that

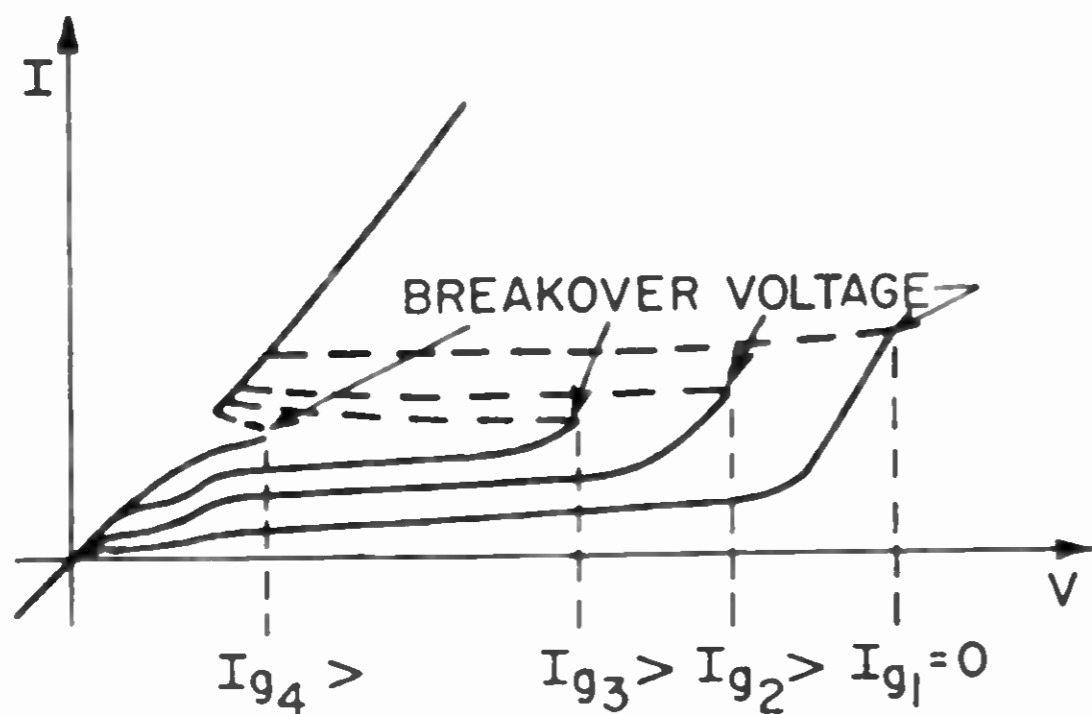


Fig. 57—Curves showing the forward-voltage characteristics of a thyristor for different values of gate current.

the device is switched to the ON state at the instant desired.

After the SCR is triggered by the gate signal, the current through the device is independent of the gate voltage or gate current. The SCR remains in the ON state until the principal current is reduced to a level below that required to sustain conduction.

Construction details of a typical SCR pellet are shown in Fig. 58.

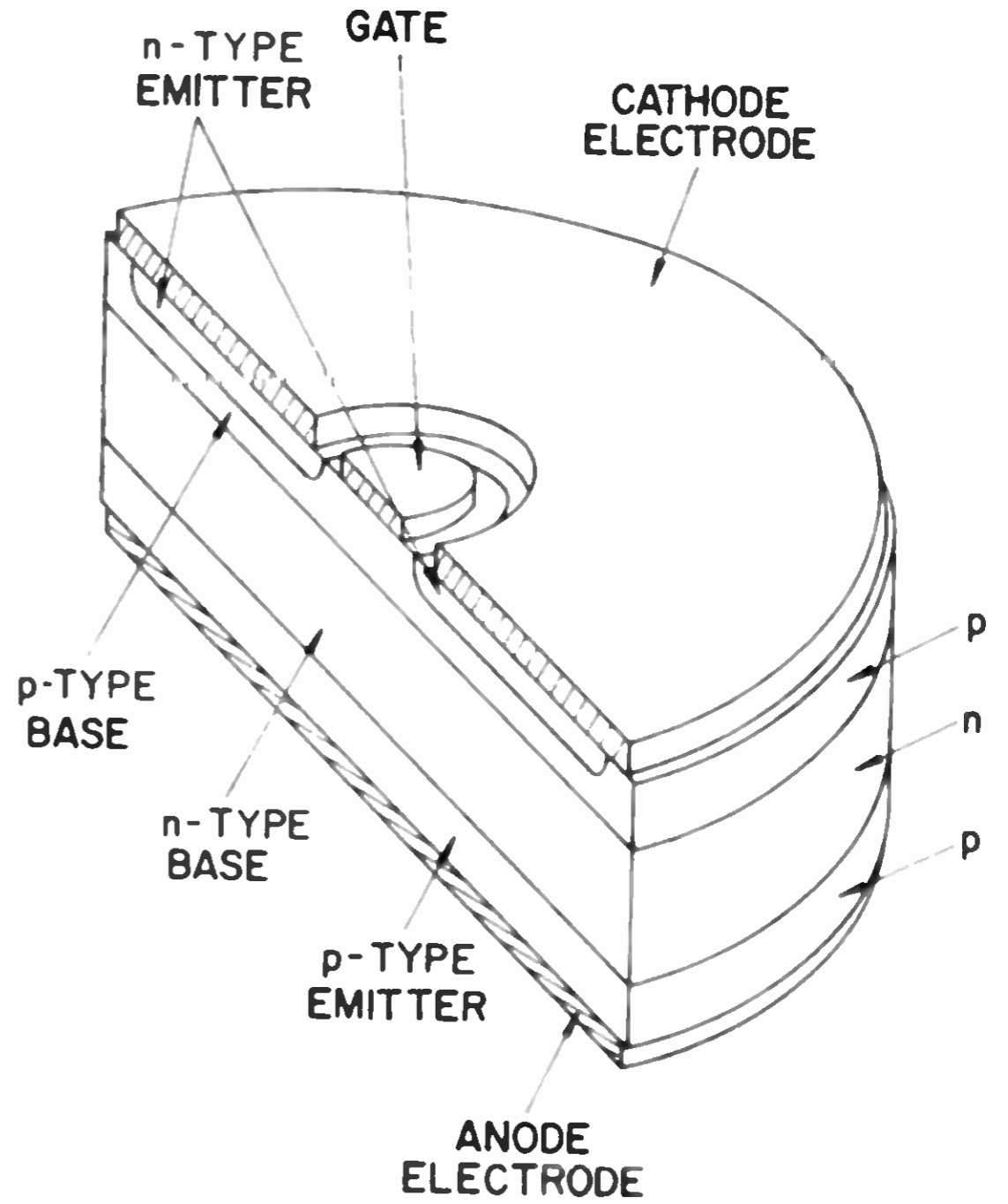


Fig. 58—Cross-section of a typical SCR pellet.

The shorted-emitter construction used in RCA SCR's can be recognized by the metallic cathode electrode in direct contact with the p-type base layer around the periphery of the pellet. The gate, at the center of the pellet, also makes direct metallic contact to the p-type base so that the portion of this layer under the n-type emitter acts as an ohmic path for current flow between gate and cathode. Because this ohmic path is in parallel with the n-type emitter junction, current preferentially takes the ohmic path until the IR drop in this path reaches the junction threshold voltage of about 0.8 volt. When the gate voltage exceeds this value, the junction current increases rapidly, and injection of electrons by the n-type emitter reaches a level high enough to turn on the device.

In addition to providing a precisely controlled gate current, the shorted-emitter construction also improves the high-temperature and dv/dt (maximum allowable rate of rise of OFF-state voltage) capabilities of the device.

The center-gate construction of the SCR pellet provides fast turn-on and high di/dt capabilities. In an SCR, conduction is initiated in the cathode region immediately adjacent to the gate contact and must then propagate to the more remote regions of the cathode. Switching losses are influenced by the rate of propagation of conduction and the distance conduction must propagate from the gate. With a central gate, all regions of the cathode are in close proximity to the initially conducting region so that propagation distance is significantly decreased; as a result, switching losses are minimized.

TRIACS

Fig. 59 shows the junction diagram, voltage-current characteristic, and schematic symbol for a triac. The triac, like the SCR, has three electrodes; they are designated as main terminal No.1, main terminal No.2, and the gate. As shown in Fig. 59(b), the triac exhibits the same forward-blocking, forward-conducting voltage-current characteristic of the SCR, but for either polarity of voltage applied to the main terminals. Under forward bias (main terminal No.2 positive with respect to main terminal No.1) or reverse bias (main terminal No.2 negative with respect to main terminal No.1), the triac exhibits first a forward-blocking (OFF) state, then a forward-conducting (ON) state. The point at which the device switches states is the breakover voltage. Again like the SCR, the breakover voltage of the triac can be controlled or varied by application of a positive or negative current pulse to the gate electrode. As the amplitude of the current pulse is

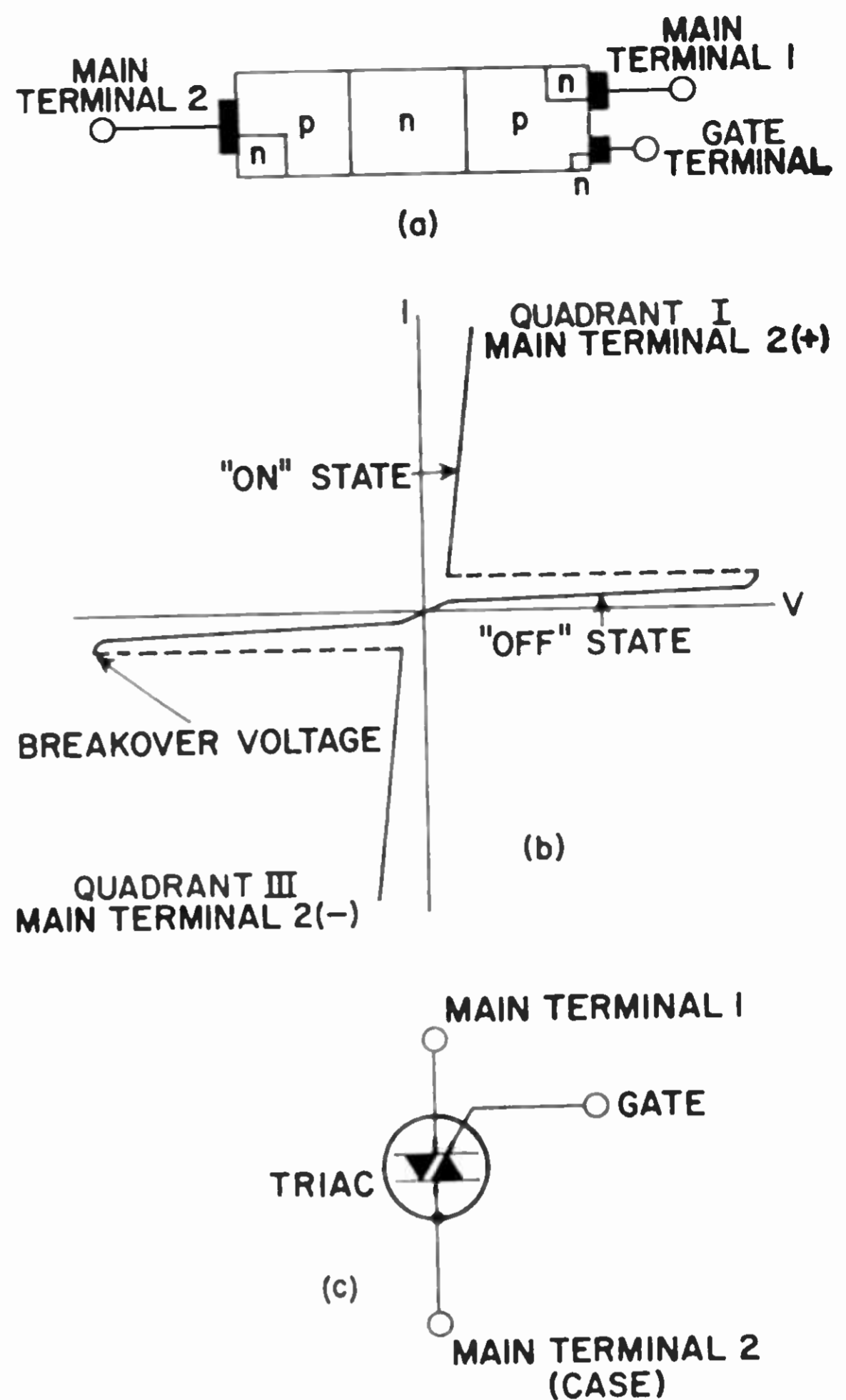


Fig. 59—(a) Junction diagram, (b) principal voltage-current characteristic, and (c) schematic symbol for a triac thyristor.

increased, the breakover point of the triac is decreased. The triac can therefore be considered as two SCR's connected in parallel and oriented in opposite directions, as shown in Fig. 60.

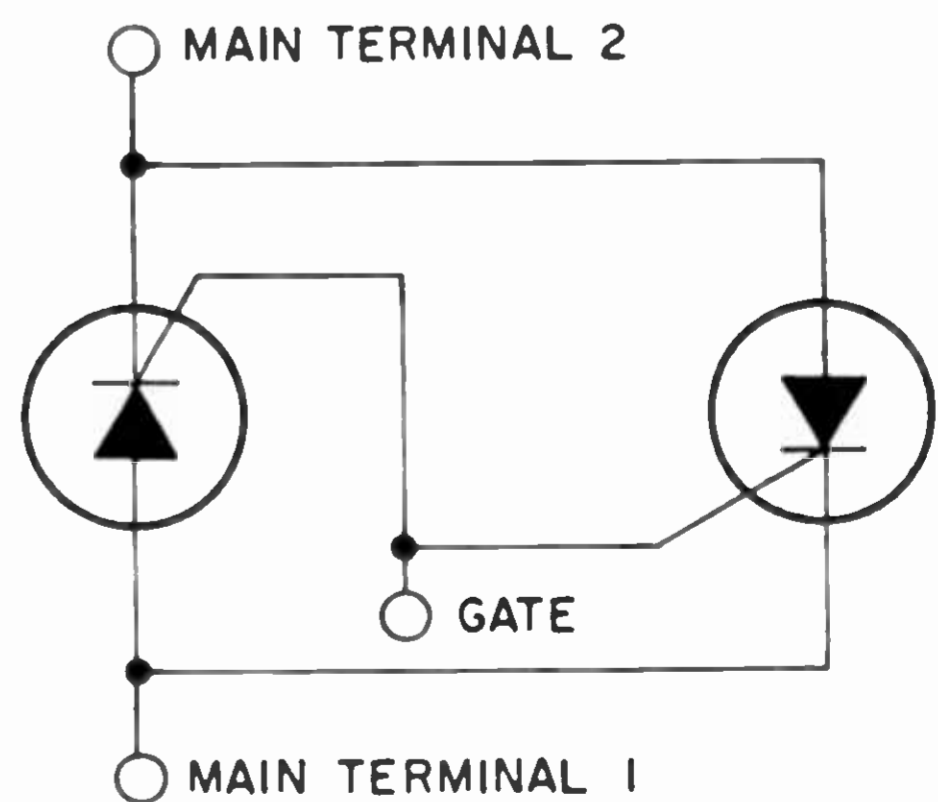


Fig. 60—A triac equivalent circuit: two SCR's in parallel and oriented in opposite directions.

Construction of a typical RCA triac pellet is shown in Fig. 61. In

this device, the main-terminal-No. 1 electrode makes ohmic contact to a p-type emitter as well as to an n-type emitter. Similarly, the main-terminal-No. 2 electrode also makes ohmic contact to both types of emitters, but the p-type emitter of the main-terminal-No. 2 side is located opposite the n-type emitter of the main-terminal-No. 1 side, and the main-terminal-No. 2 n-type emitter is opposite the main-terminal-No. 1 p-type emitter. The net result is two four-layer switches in parallel, but oriented in opposite directions, in one silicon pellet. This type of construction makes it possible for a triac either to block or to conduct current in either direction between main terminal No. 1 and main terminal No. 2.

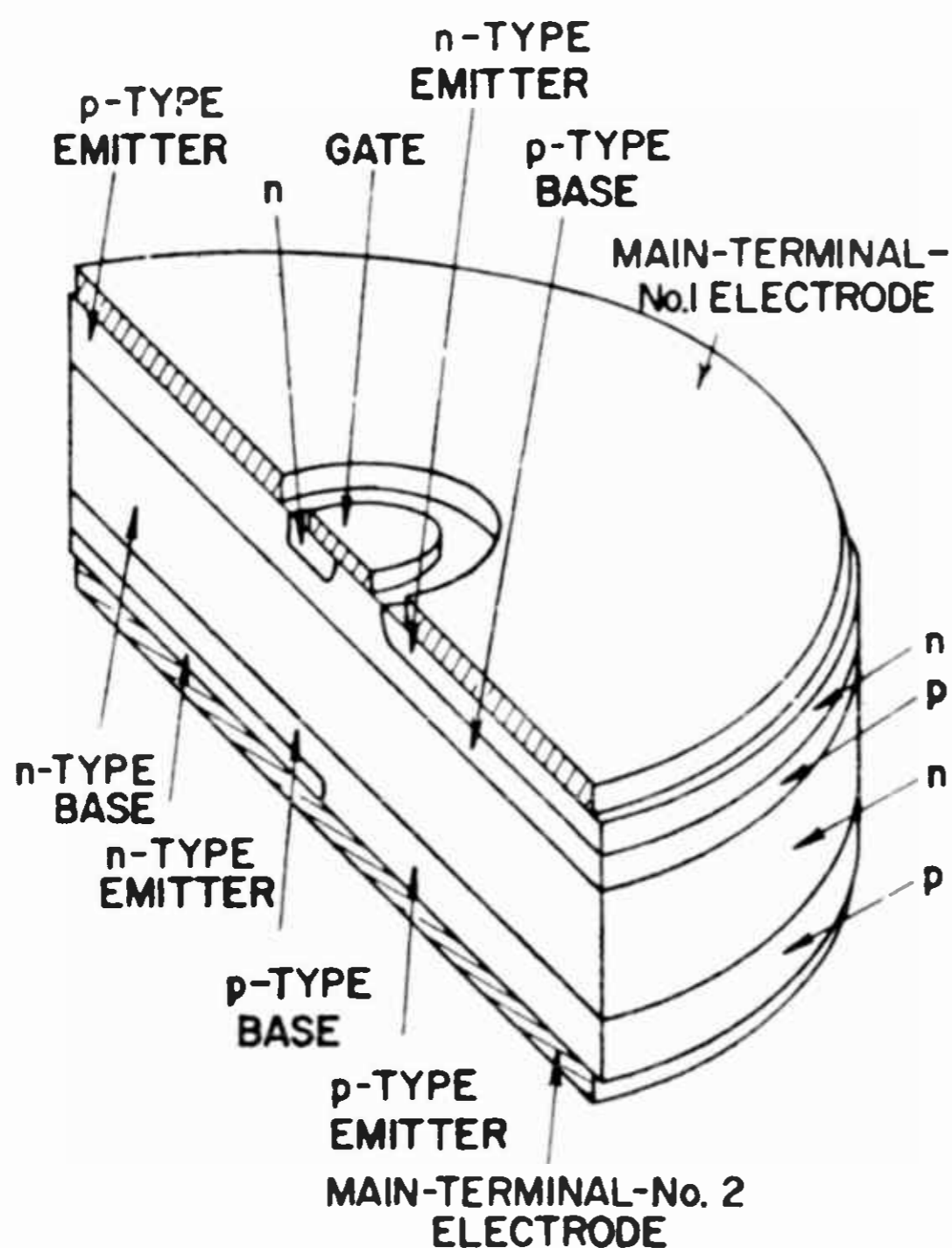


Fig. 61—Cross-section of a typical triac pellet.

DIACS

A diac is a two-electrode, three-layer bidirectional avalanche diode which can be switched from the OFF state to the ON state for either polarity of applied voltage. Fig. 62 shows the junction diagram, voltage-current characteristic, and schematic symbol for a diac.

This three-layer trigger diode is similar in construction to a bipolar

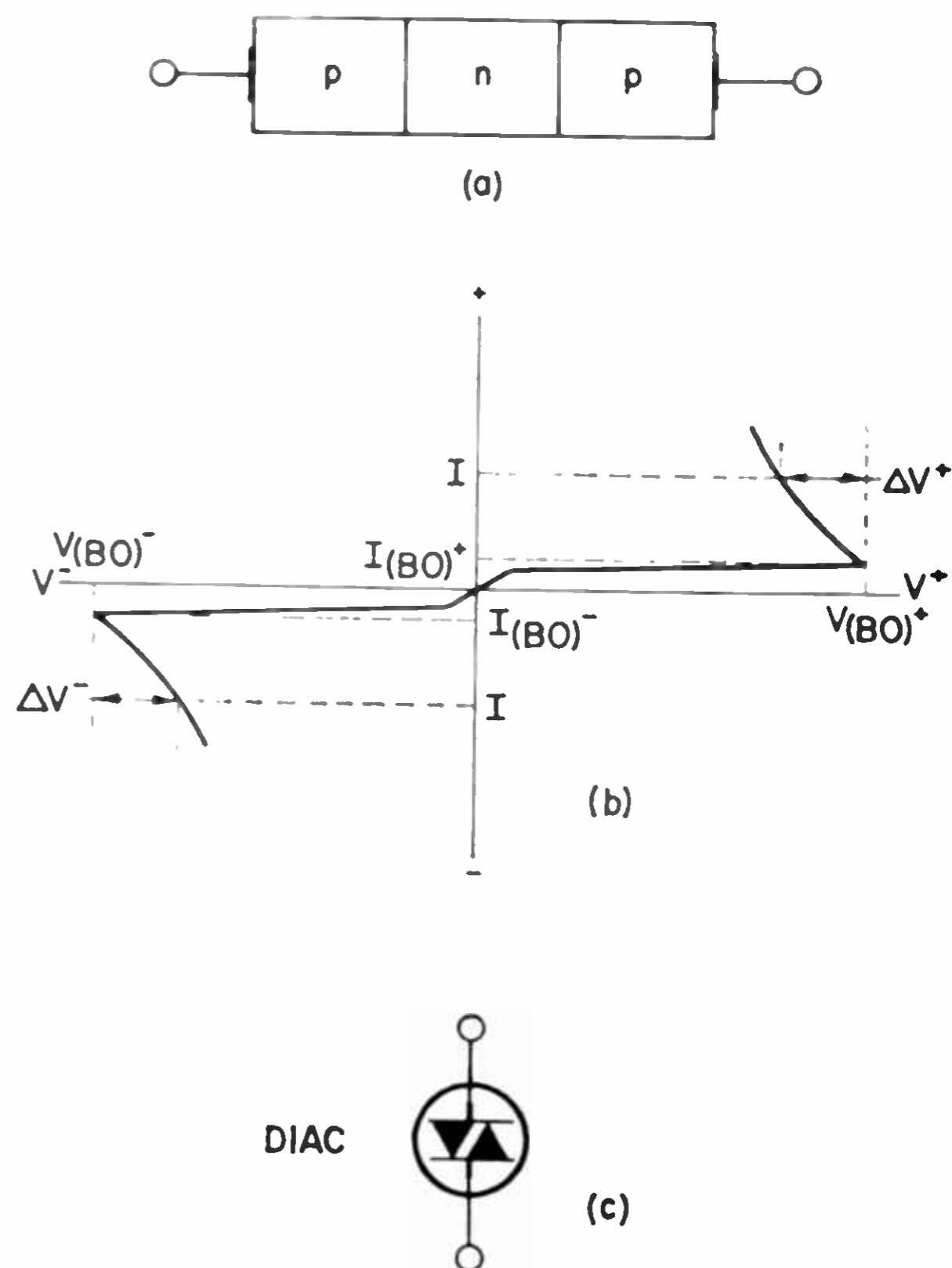


Fig. 62—(a) Junction diagram, (b) voltage-current characteristic, and (c) schematic symbol for a diac.

transistor. A diac differs from a bipolar transistor in that the doping concentrations at the two junctions are approximately the same and there is no contact made to the base layer. The equal doping levels result in a symmetrical bidirectional switching characteristic, as shown in Fig. 62(b). When an increasing positive or negative voltage is applied across the terminals of the diac, a minimum (leakage) current $I_{(BO)}$ flows through the device until the voltage reaches the breakover point $V_{(BO)}$. The reverse-biased junction then undergoes avalanche breakdown and, beyond this point, the device exhibits a negative-resistance characteristic, i.e., current through the device increases substantially with decreasing voltage.

Diacs are primarily used as triggering devices in triac phase-control circuits used for light dimming, universal motor-speed control, heat control, and similar applications. Fig. 63 shows the general circuit diagram for a diac/triac phase-control circuit. The magnitude and

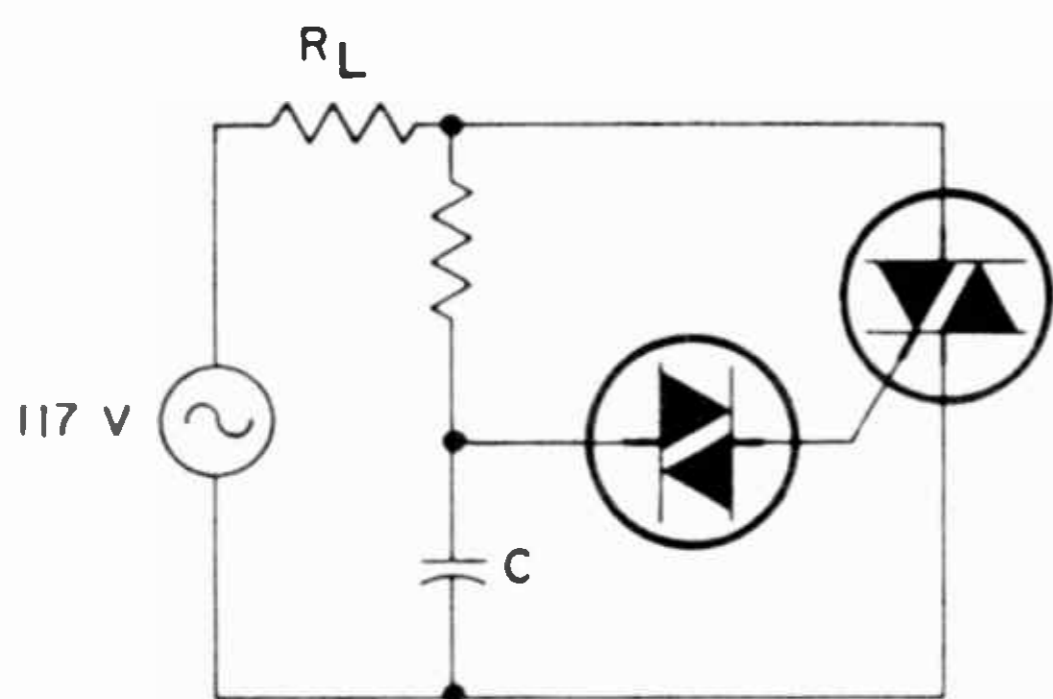


Fig. 63—General circuit diagram for a diac/triac phase-control circuit.

duration of the current pulse applied to the gate of the triac are determined by the value of phase-shift capacitance C , the change in voltage across and the dynamic impedance of the diac, and the triac gate impedance. The interaction of all circuit impedances and the phase-shift capacitance can best be represented by the curve of peak current as a function of the capacitance shown in Fig. 64.

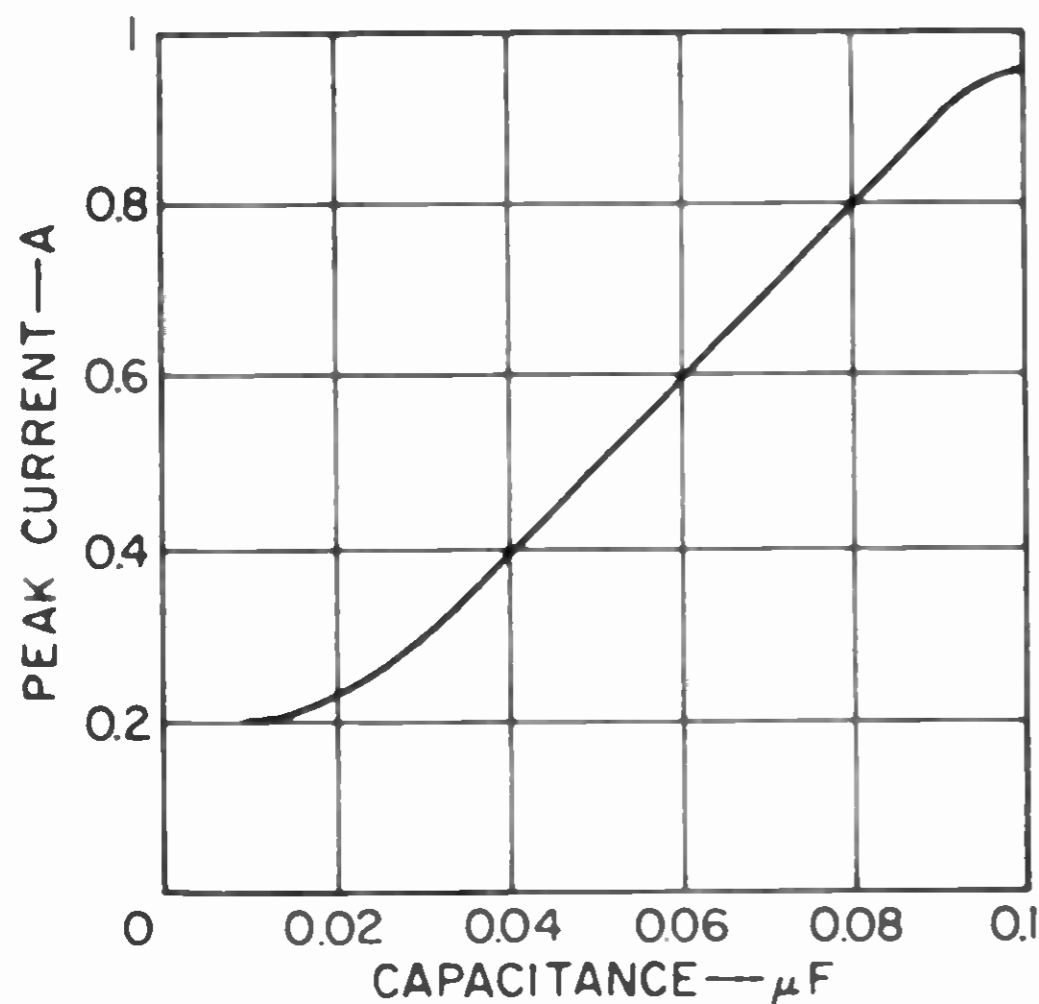


Fig. 64—Peak current as a function of capacitance in a triac.

SCR AND TRIAC GATE CHARACTERISTICS

Silicon controlled rectifiers and triacs are ideal for switching applications. When the working voltage of the thyristor is below the breakover point, the device is essentially an open switch; above the breakover voltage, the thyristor

switches to the ON state and is effectively a closed switch. The break-over voltage can be varied or controlled by injections of a signal at the gate terminal.

The manufacturer's specifications indicate the magnitude of gate current and voltage required to turn on these devices. Gate characteristics, however, vary from device to device even among devices within the same family. For this reason, manufacturer's specifications on gating characteristics provide a range of values in the form of characteristic diagrams. A diagram such as that shown in Fig. 65 is given to define the limits of gate currents and voltages that may be used to trigger any given device of a specific family. The boundary lines of maximum and minimum gate impedance on this characteristic diagram represent the loci of all possible triggering points for thyristors in this family. The curve OA represents the gate characteristic of a specific device that is triggered within the shaded area.

The magnitude of gate current and voltage required to trigger a thyristor varies inversely with junction temperature. As the junction temperature increases, the level of gate signal required to trigger the thyristor becomes smaller. Worst-case triggering conditions occur, therefore, at

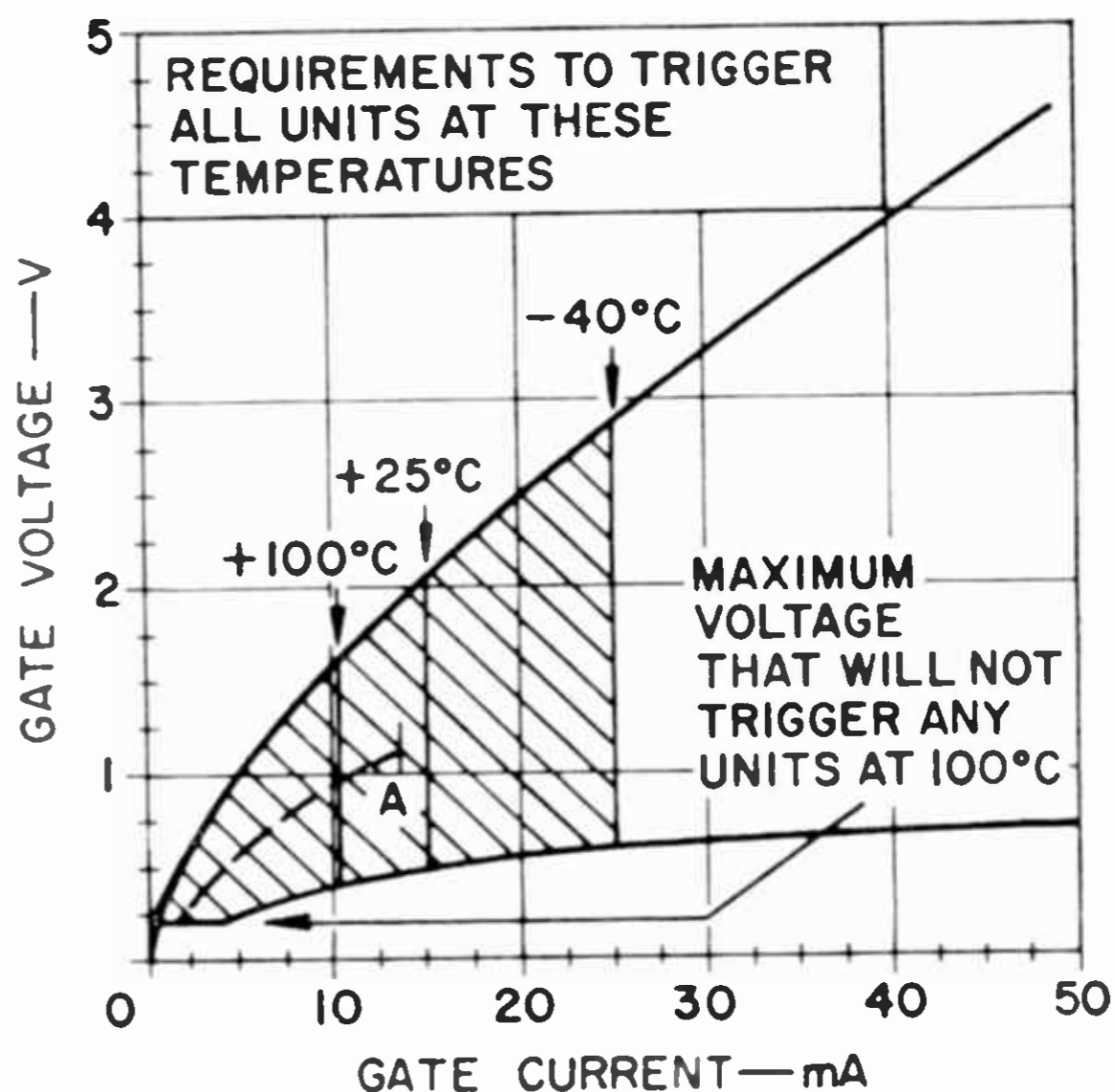


Fig. 65—Gate-characteristics curves for a typical RCA SCR.

the minimum operating junction temperature.

The gate nontrigger voltage V_{gnt} is the maximum dc gate voltage that may be applied between gate and cathode of the thyristor for which the device can maintain its rated blocking voltage. This voltage is usually specified at the rated operating temperature (100°C) of the thyristor. Noise signals in the gate circuit should be maintained below this level to prevent unwanted triggering of the thyristor.

When very precise triggering of a thyristor is desired, the thyristor gate must be overdriven by a pulse of current much larger than the dc gate current required to trigger the device. The use of a large current pulse reduces variations in turn-on time, minimizes the effect of temperature variations on triggering characteristics, and makes possible very short switching times.

The coaxial gate structure and the "shorted-emitter" construction techniques used in RCA thyristors have greatly extended the range of limiting gate characteristics. As a result, the gate-dissipation ratings of RCA thyristors are compatible with the power-handling capabilities of other elements of these devices. Advantage can be taken of the higher peak-power capability of the gate to improve dynamic performance, increase di/dt capability (maximum allowable rate of rise of ON-state current), minimize interpulse jitter, and reduce switching losses. This higher peak-power capability also allows greater interchangeability of thyristors in high-performance applications.

The forward gate characteristics for thyristors, shown in Fig. 66, indicate the maximum allowable pulse widths for various peak values of gate input power. The pulse width is determined by the relationship that exists between gate power input and the increase in the temperature of the thyristor pellet that results from the application of gate power.

The curves shown in Fig. 66(a) are for RCA SCR's that have relatively small current ratings (2N4101, 2N4102, and 40379 families), and the curves shown in Fig. 66(b) are for RCA SCR's that have larger current ratings (2N4103, 2N3873, and 2N3899 families). Because

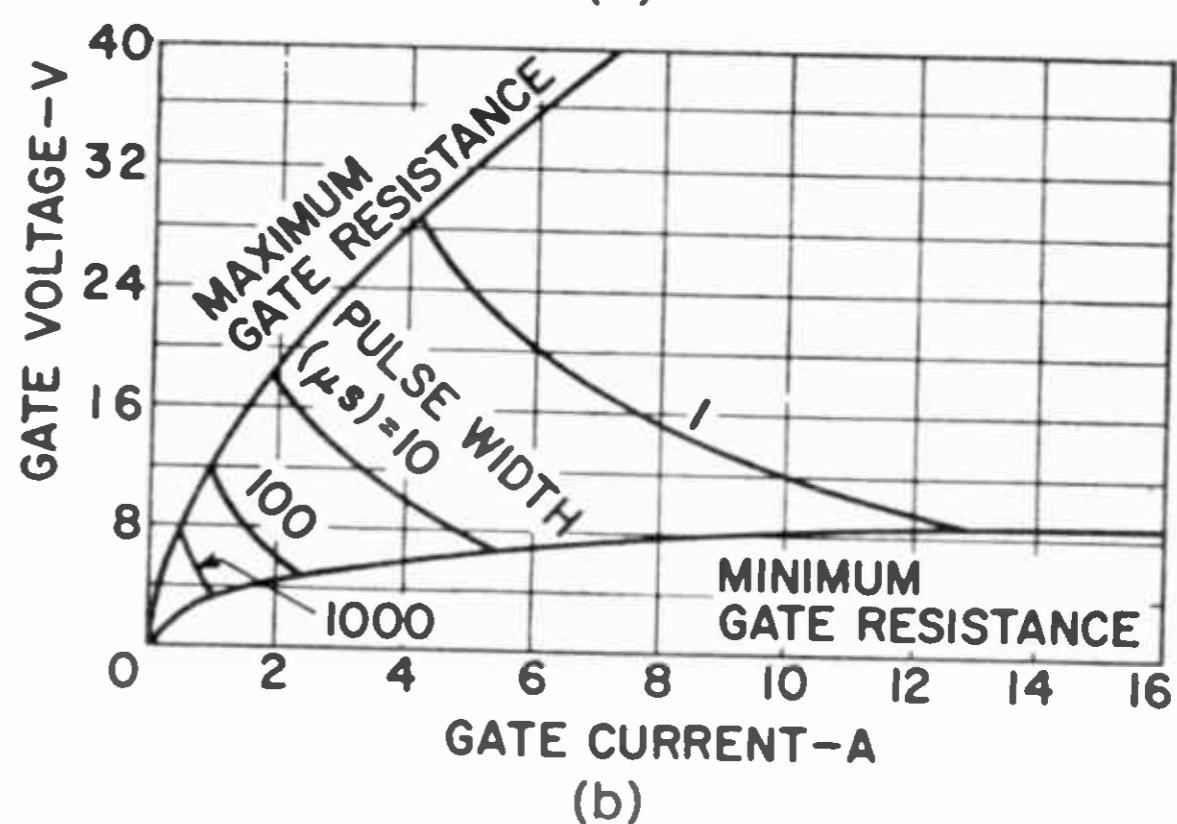
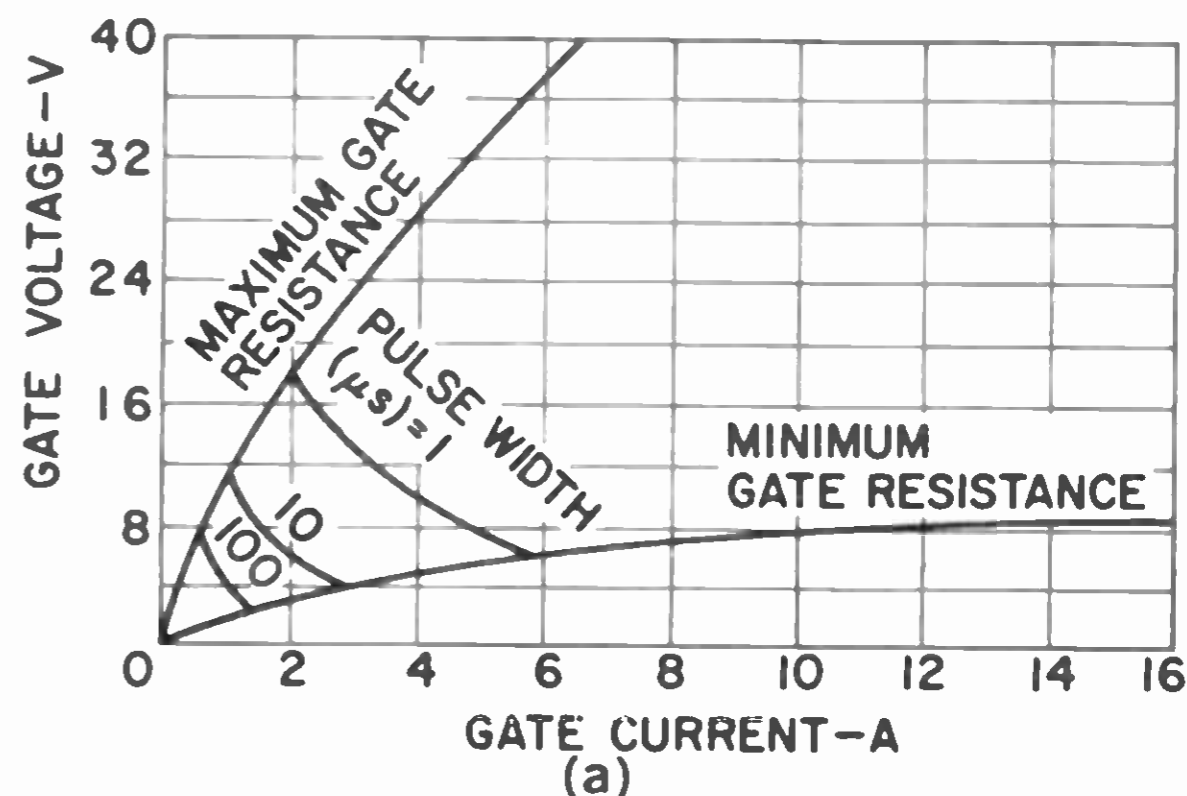
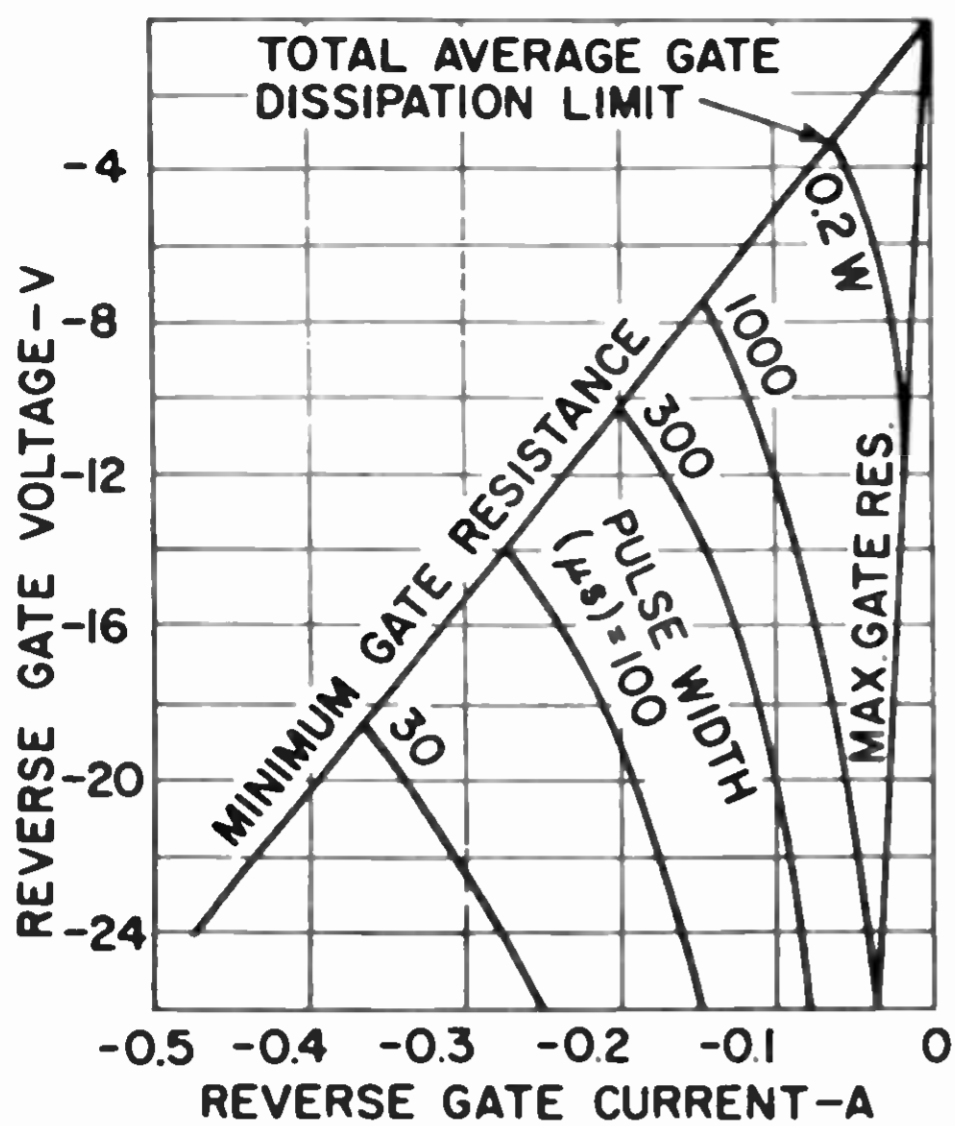


Fig. 66—Forward gate characteristics for pulse triggering of RCA SCR's: (a) low-current types; (b) high-current types.

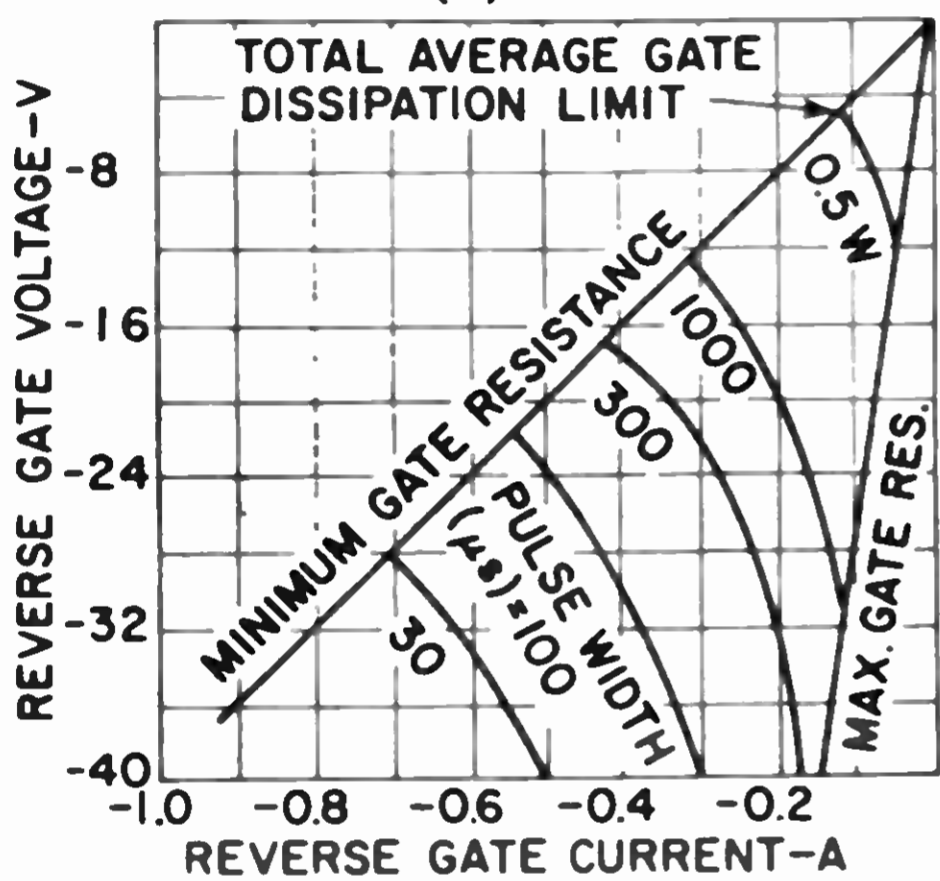
the higher-current thyristors have larger pellets, they also have greater thermal capacities than the smaller-current devices. Wider gate trigger pulses can therefore be used on these devices for the same peak value of gate input power.

Because of the resistive nature of the "shorted-emitter" construction, similar volt-ampere curves can be constructed for reverse gate voltages and currents, with maximum allowable pulse widths for various peak-power values, as shown in Fig. 67. These curves indicate that reverse dissipations do not exceed the maximum allowable power dissipation for the device.

The total average dissipation caused by gate-trigger pulses is the sum of the average forward and re-



(a)



(b)

Fig. 67—Reverse gate characteristics of RCA SCR's: (a) low-current types; (b) high-current types.

verse dissipations. This total dissipation should be less than the Maximum Gate Power Dissipation P_{GM} shown in the published data for the selected SCR. If the average gate dissipation exceeds the maximum published value, as the result of high forward gate-trigger pulses and transient or steady-state reverse gate biasing, the maximum allowable forward-conduction-current rating of the device must be reduced to compensate for the increased rise of junction temperature caused by the increased gate power dissipation.

The triac can be triggered in any of four operating modes, as summarized in Table I. The quadrant designations refer to the operating quadrant on the principal voltage-current characteristics, shown in Fig. 59 (either I or III), and the polarity

symbol represents the gate-to-main-terminal-No. 1 voltage.

Table I—Triac Triggering Modes

Gate-to-Main-Terminal-No. 1 Voltage	Main Terminal No. 2-to-Main Terminal No. 1 Voltage	Operating Quadrant
Positive	Positive	I(+)
Negative	Positive	I(-)
Positive	Negative	III(+)
Negative	Negative	III(-)

The gate-trigger requirements of the triac are different in each operating mode. The I(+) mode (gate positive with respect to main terminal No. 1 and main terminal No. 2 positive with respect to main terminal No. 1), which is comparable to equivalent SCR operation, is usually the most sensitive. The smallest gate current is required to trigger the triac in this mode. The other three operating modes require larger gate-trigger currents. For RCA triacs, the maximum trigger-current rating in the published data is the largest value of gate current that is required to trigger the selected device in any operating mode.

Gate Trigger Circuits

The gate signal used to trigger an SCR or triac must be of sufficient strength to assure sustained forward conduction. Triggering requirements are usually stated in terms of dc voltage and current. Because it is common practice to pulse-fire thyristors, it is also necessary to consider the duration of firing pulse required. A trigger pulse that has an amplitude just equivalent to the dc requirements must be applied for a relatively long period of time (approximately 30 microseconds) to ensure that the gate signal is provided during the full turn-on period of the thyristor. As the amplitude of the gate-triggering signal is increased, the turn-on time of the

thyristor is decreased, and the width of the gate pulse may be reduced. When highly inductive loads are used, the inductance controls the current-rise portion of the turn-on time. For this type of load, the width of the gate pulse must be made long enough to assure that the principal current rises to a value greater than the latching-current level of the device. The latching current of RCA thyristors is always less than twice the holding current.

The application usually determines whether a simple or somewhat sophisticated triggering circuit should be used to trigger a given thyristor. Triggering circuits can be as numerous and as varied as the applications in which they are used; this text discusses the basic types only.

Many applications require that a thyristor be switched full ON or full OFF in a manner similar to the operation of a relay. Although higher currents are handled by the thyristor, only small trigger or gate currents are required from the control circuit or switch. The simplest method of accomplishing this type of triggering is illustrated in Fig. 68.

Each circuit shows a variable resistor in the gate circuit to control the conduction angle of the thyristor.

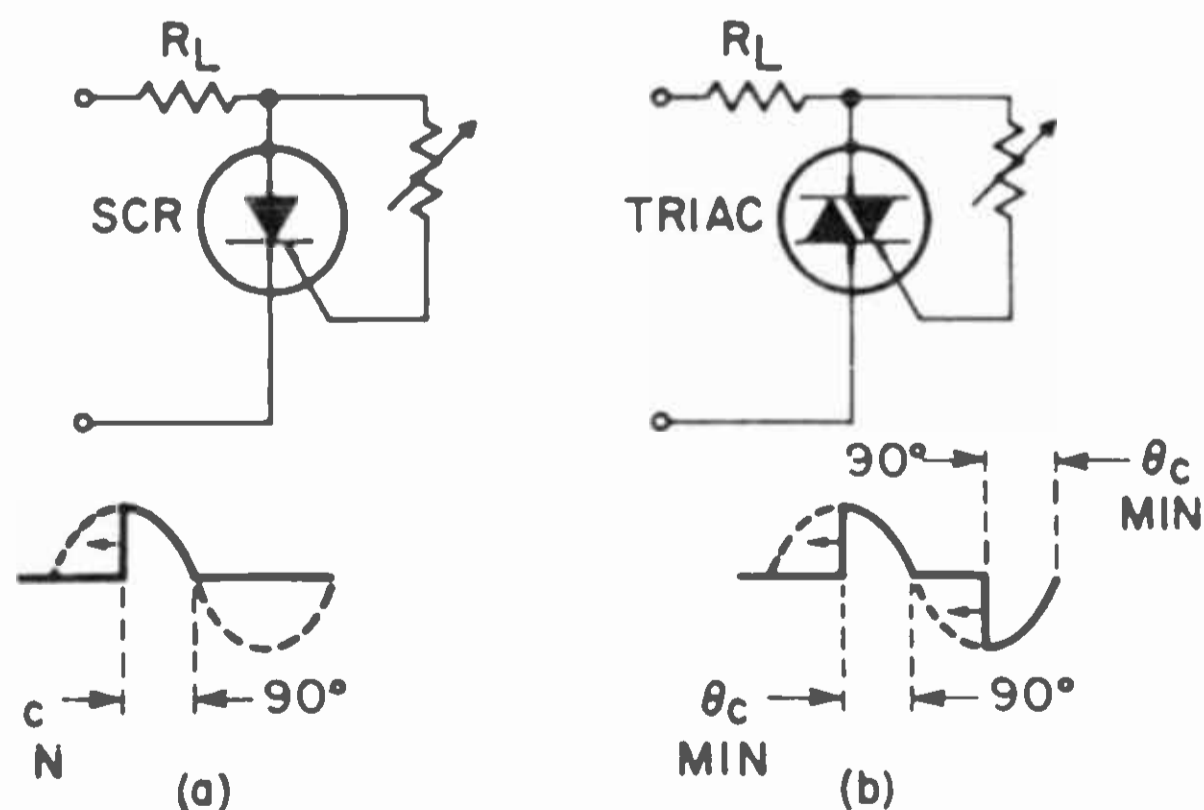


Fig. 68—Degree of control over conduction angles when an ac resistive network is used to trigger SCR's and triacs.

The waveforms indicating the degree of control exercised by the variable resistance are also shown in Fig. 68. With maximum resistance in either circuit, the thyristor is

OFF. As the resistance is reduced in the SCR circuit, a point is reached at which sufficient gate trigger current is provided at the positive peak of the voltage wave (90 degrees) to trigger the SCR ON. The SCR conducts from the 90-degree point to the 180-degree point for a total conduction angle of $(180-90)$, or 90 degrees. In the triac circuit, as the resistance is reduced, the gate current increases until the triac is triggered at both the peak positive (90 degrees) and peak negative (270 degrees) points on the voltage wave. The triac then conducts between 90 degrees and 180 degrees, and between 270 degrees and 360 degrees for a total conduction angle of 180 degrees. The conduction angles of both the SCR and the triac can be increased by further reduction of the resistance in the gate circuits. For the SCR, the firing point is moved back from 90 degrees toward zero for a total conduction angle approaching 180 degrees. The triac firing points can also be moved back from 90 degrees toward zero for the positive half-cycle and from 270 degrees toward 180 degrees for the negative half-cycle to obtain a total conduction angle approaching 360 degrees. The resistor in the gate circuit assures that the gate current decreases to a negligible value after the thyristor is fired.

An easier method of obtaining a phase angle greater than 90 degrees for half-wave operation is to use a resistance-capacitance triggering network. Fig. 69 shows the simplest form of such networks for use with an SCR and a triac. The thyristor is in series with the load and in parallel with the RC network. At the beginning of each half-cycle (positive half-cycle only for the SCR), the thyristor is in the OFF state. As a result, the ac voltage appears across the thyristor and essentially none appears across the load. Because the thyristor is in parallel with the potentiometer and capacitor, the voltage across the thyristor drives current through the

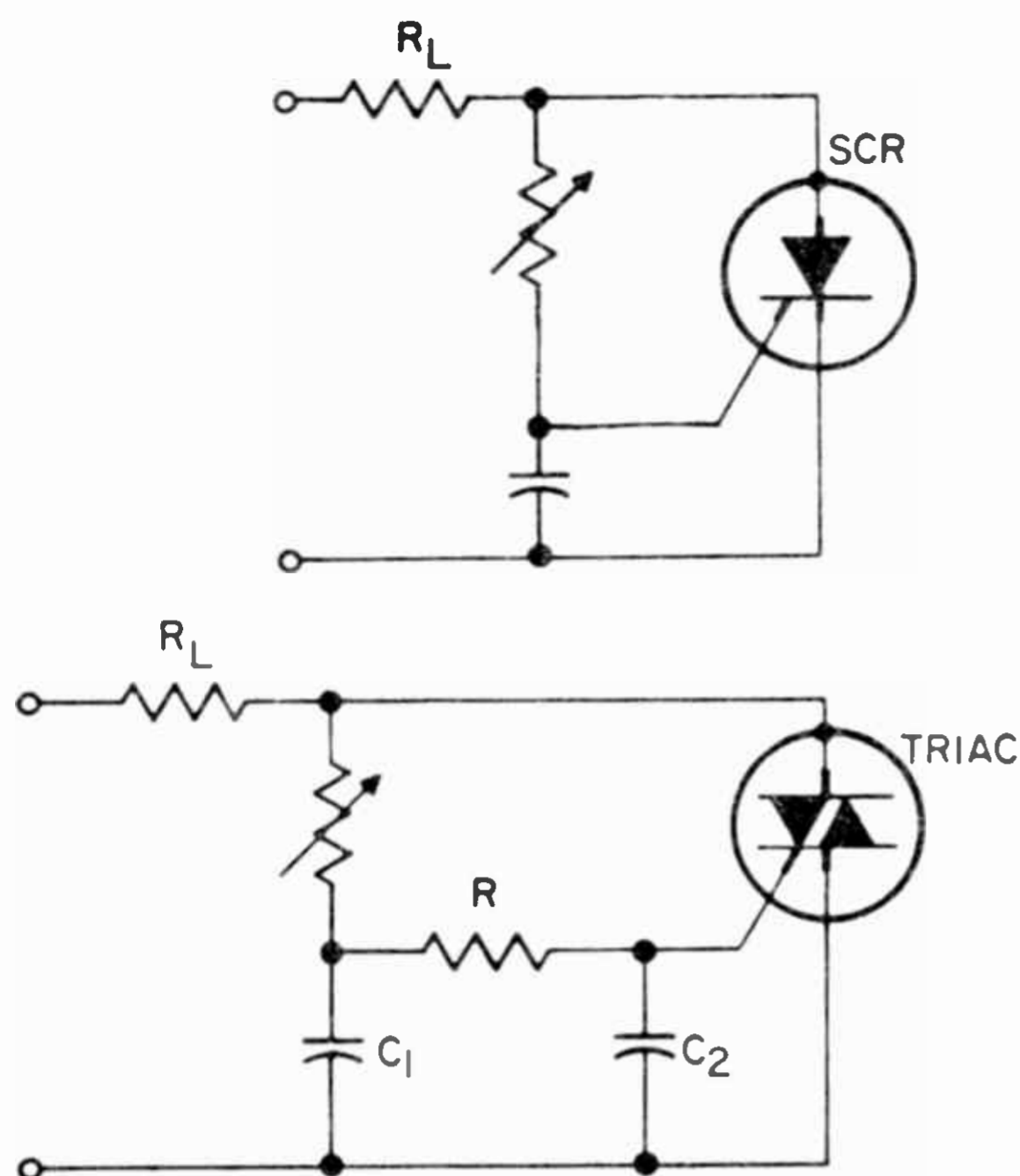


Fig. 69—RC triggering networks used for phase-control triggering of thyristors.

potentiometer and charges the capacitor. When the capacitor voltage reaches the breakover voltage of the thyristor, the capacitor discharges through the gate circuit and turns the thyristor on. At this point, the ac voltage is transferred from the thyristor to the load R_L for the remainder of the half-cycle. If the potentiometer resistance is reduced, the capacitor charges more rapidly, and the breakover voltage is reached earlier in the cycle; as a result, the power applied to the load is increased.

The gate trigger voltage can be more closely controlled in simple resistance or resistance-capacitance circuits by use of a variety of special triggering devices. These triggering devices, including the diac, have a smaller range of characteristics, and are less temperature-sensitive. Basically, a thyristor triggering device exhibits a negative resistance after a critical voltage is reached, so that the gate-current requirement of the thyristor can be obtained as a pulse from the discharge of the phase-shift capacitor. Because the gate pulse need be only microseconds in duration, the gate-pulse energy and the size of the triggering components are relatively small. Triggering circuits of this

type employ elements such as neon bulbs, diacs, unijunction transistors, and two-transistor switches.

Fig. 70 shows a light-dimming circuit in which a diac is used to trigger a triac. The voltage-current

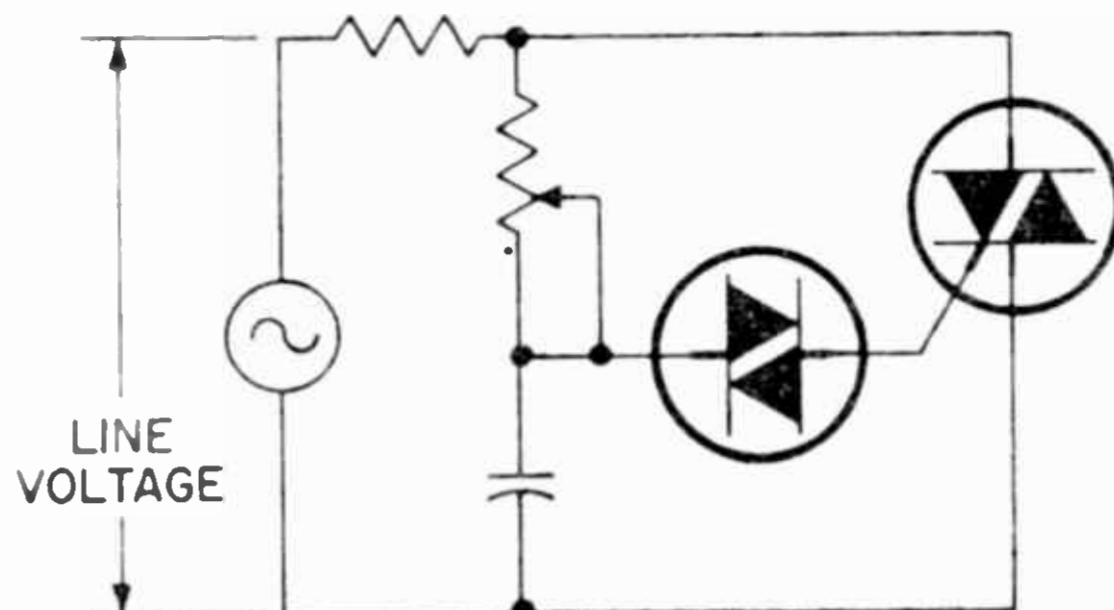


Fig. 70—A light-dimmer circuit in which a diac is used to trigger a triac.

characteristic for the diac in this circuit is shown in Fig. 71. The magnitude and duration of the gate-current pulse are determined

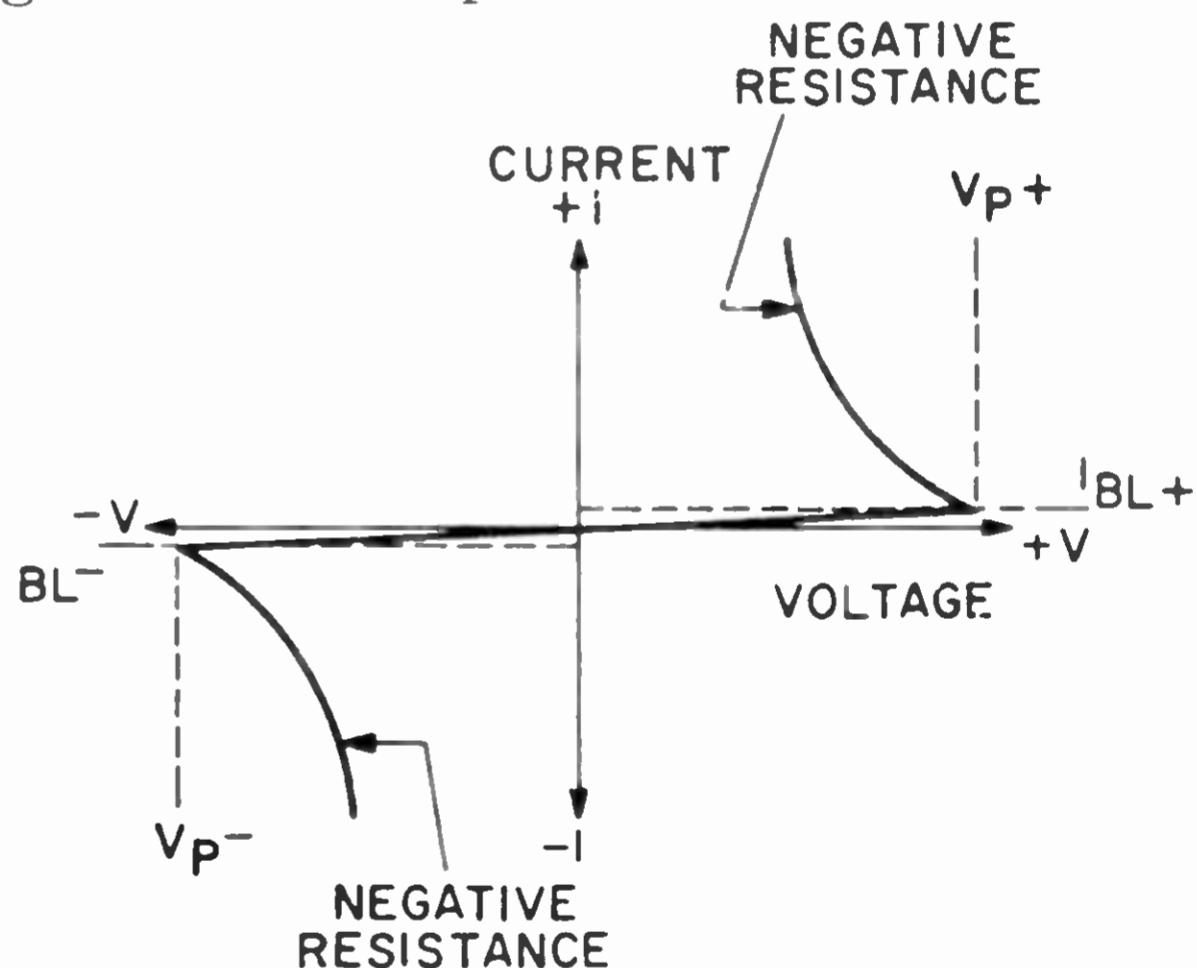


Fig. 71—Voltage-current characteristic for triggering device shown in Fig. 70.

by the interaction of the capacitor C_1 , the diac characteristics, and the impedance of the thyristor gate. Fig. 72 shows the typical shape of the gate-current pulse that is produced.

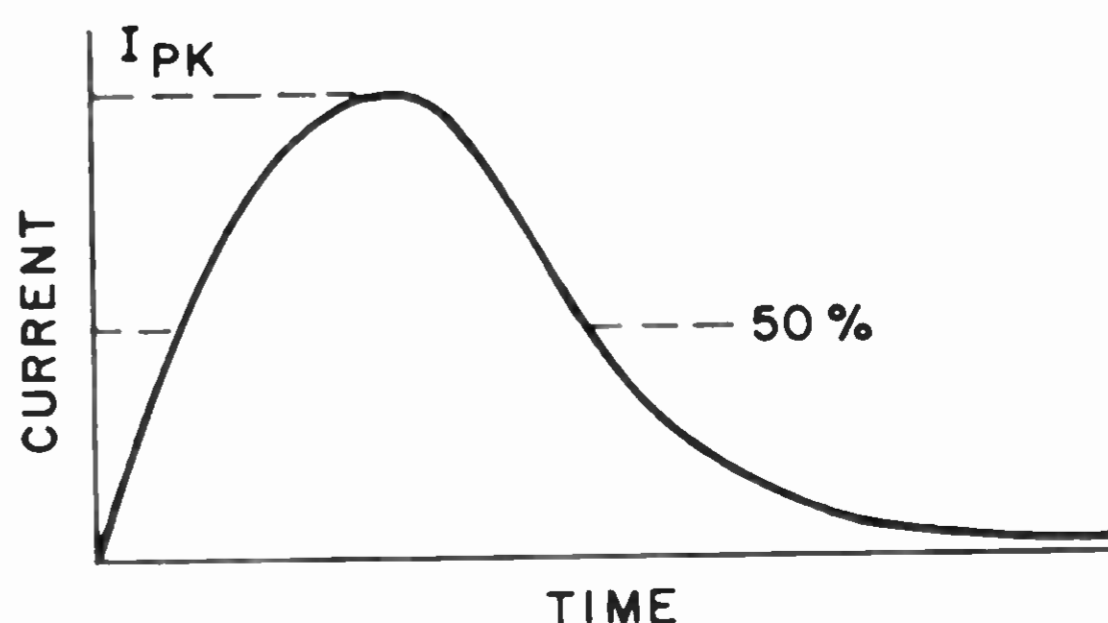


Fig. 72—Typical gate-current waveform for circuit shown in Fig. 70.

SWITCHING CHARACTERISTICS

The ratings of thyristors are based primarily upon the amount of heat generated within the device pellet and the ability of the device package to transfer the internal heat to the external case. For high-frequency applications in which the peak-to-average current ratio is high, or for high-performance applications that require large peak values but narrow current pulses, the energy lost during the turn-on process may be the main cause of heat generation within the thyristor. The switching properties of the device must be known, therefore, to determine power dissipation which may limit the device performance.

When a thyristor is triggered by a gate signal, the turn-on time of the device consists of two stages, a delay time t_d and a rise time t_r , as shown in Fig. 73. The total turn-on time t_{gt} is defined as the time interval between the initiation of the gate signal and the time when the resulting current through the thyristor reaches 90 per cent of its maximum value with a resistive load. The delay time t_d is defined as the time interval between the 10-per-cent point of the leading edge of the gate-trigger voltage and the 10-per-cent point of the

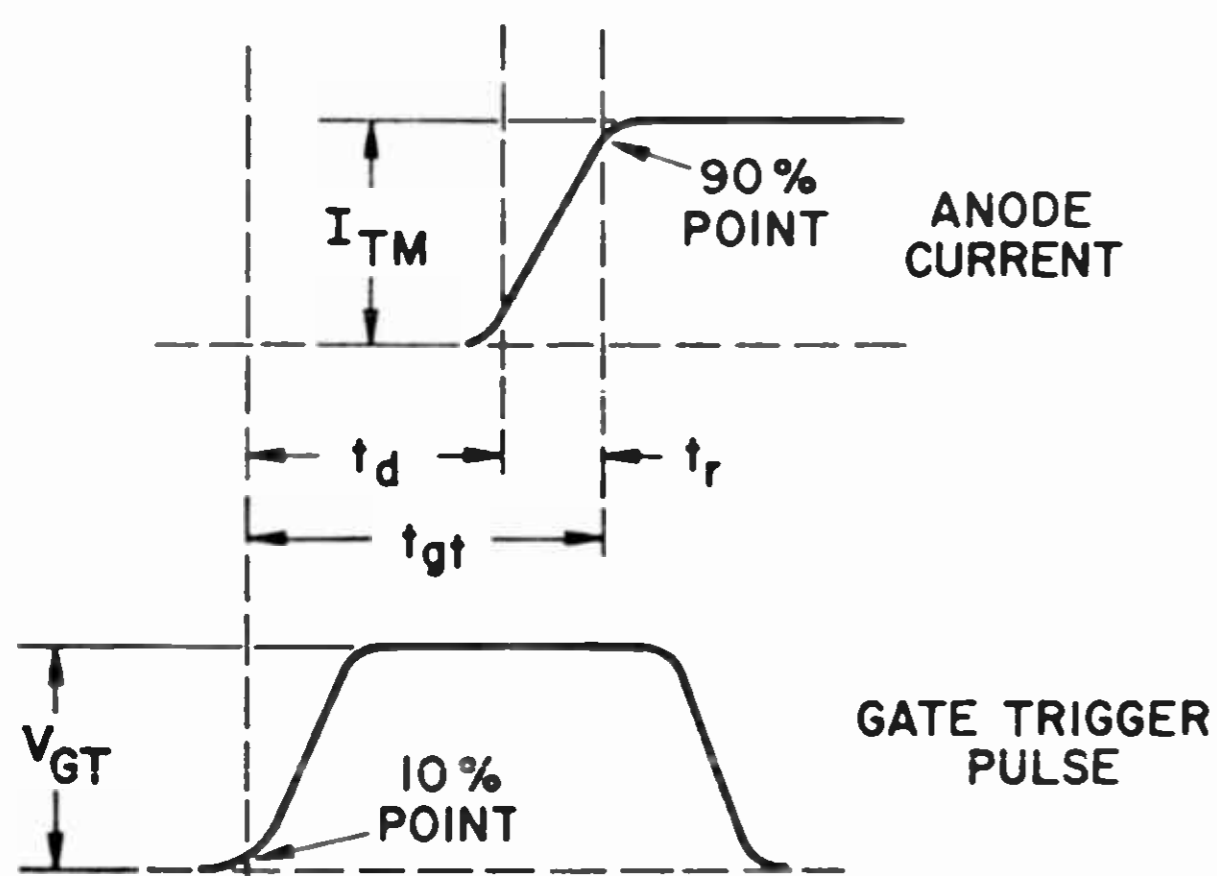


Fig. 73—Gate-current and voltage turn-on waveforms for a thyristor.

resulting current with a resistive load. The rise time t_r is the time interval required for the principal current to rise from 10 to 90 per cent of its maximum value. The total turn-on time, therefore, is the

sum of both the delay and rise times of the thyristor.

Although the turn-on time is affected to some extent by the peak OFF-state voltage and the peak ON-state current level, it is influenced primarily by the magnitude of the gate-trigger current pulse. Fig. 74 shows the variation in turn-on time with gate-trigger current for the RCA-2N3873 SCR.

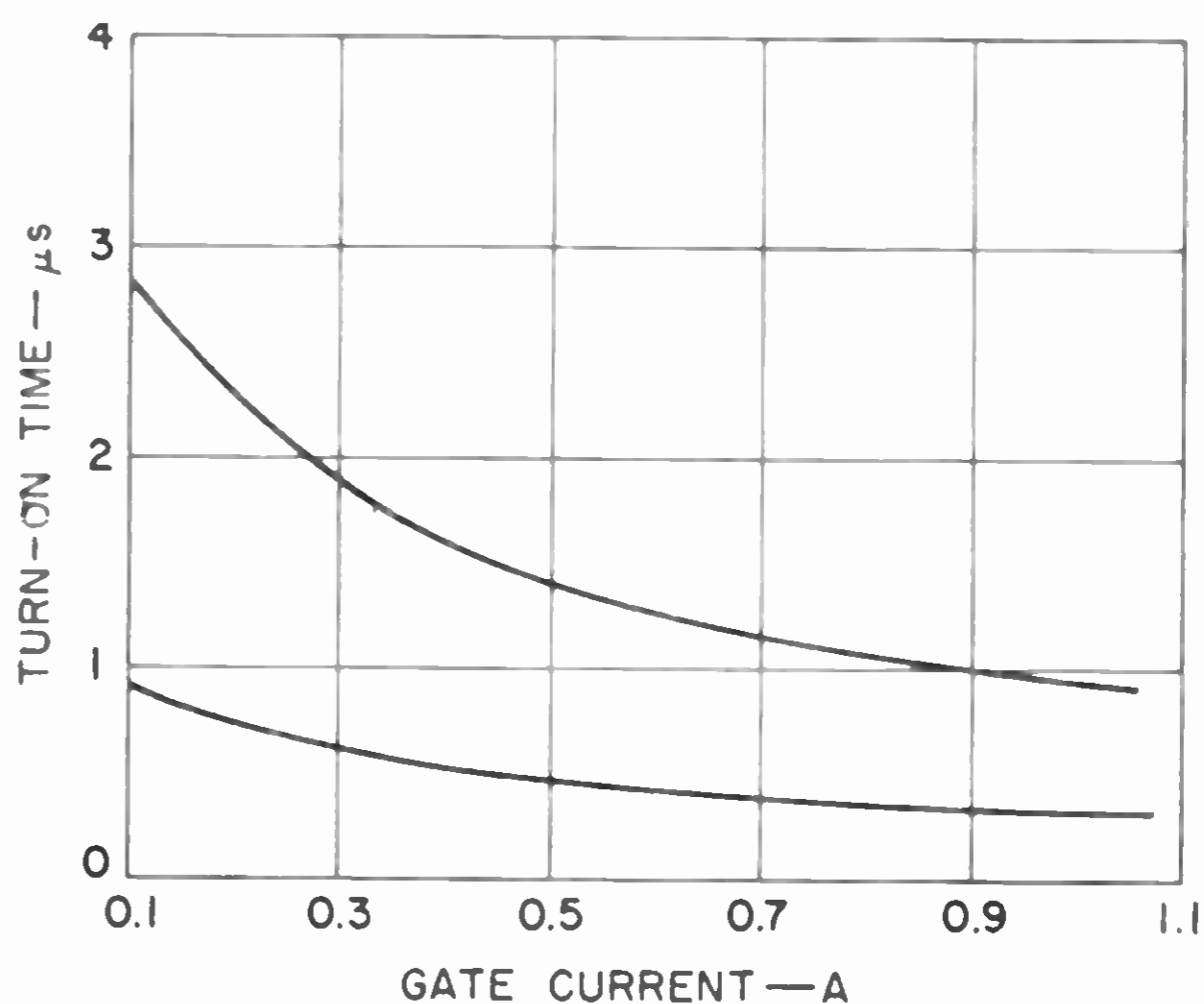


Fig. 74—Range of turn-on time as a function of gate current for the 2N3873 SCR.

To guarantee reliable operation and provide guidance for equipment designers in applications having short conduction periods, the voltage drop across RCA thyristors, at a given instantaneous forward current and at a specified time after turn-on from an OFF-state condition, is given in the published data. The waveshape for the initial ON-state voltage for the RCA-2N3873 SCR is shown in Fig. 75. This initial voltage, together with the time required for reduction of the dynamic forward voltage drop during the spreading time, is an indication of the current-switching capability of the thyristor.

When the entire junction area of a thyristor is not in conduction, the current through that fraction of the pellet area in conduction may result in large instantaneous power losses. These turn-on switching losses are proportional to the current and the voltage from cathode to anode of the device, together with the repetition rate of the gate-trigger pulses. The instantaneous power dissipated in a

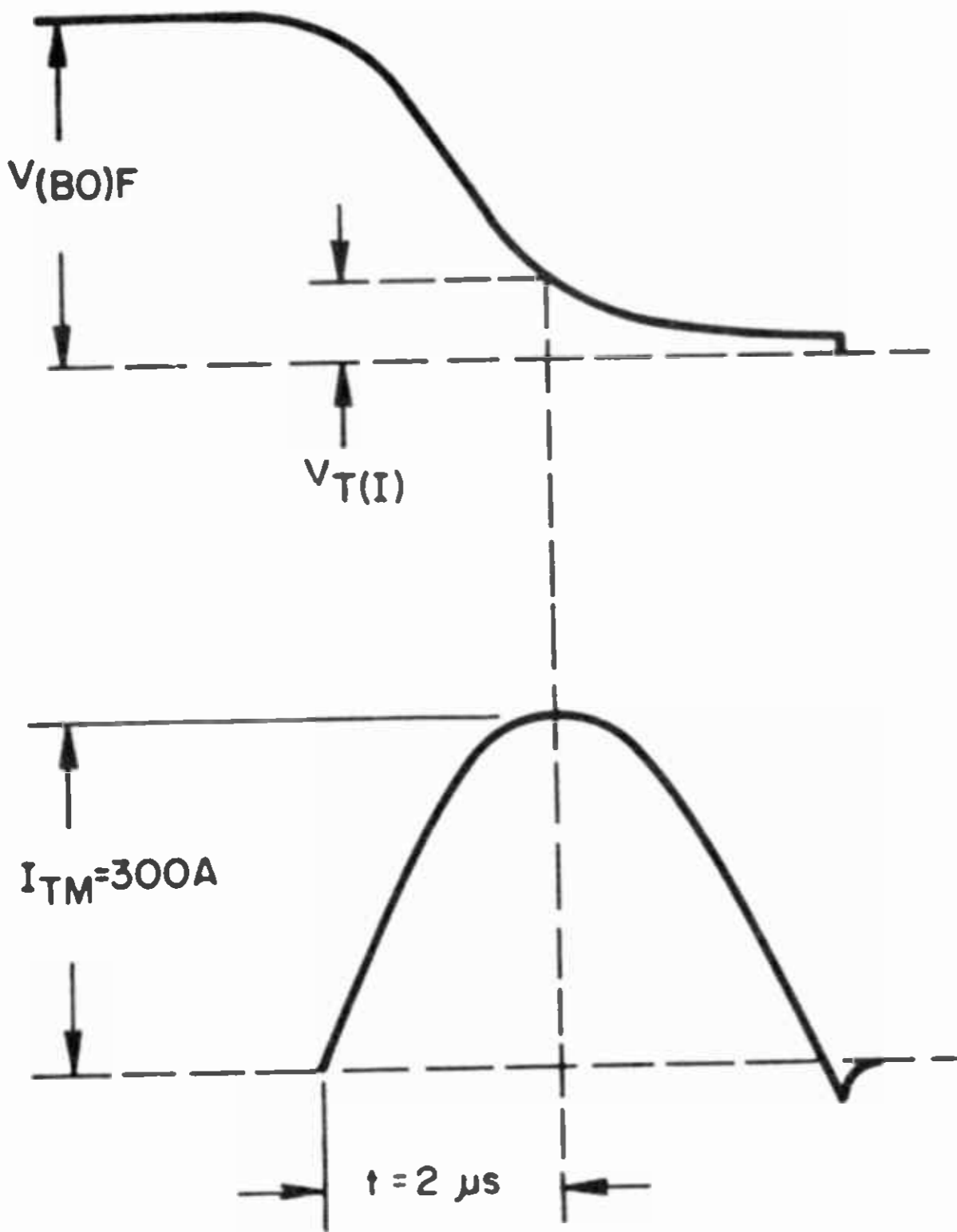


Fig. 75—Initial on-state voltage and current waveforms for the 2N3873 SCR.

thyristor under such conditions is shown in Fig. 76. The curves shown in this figure indicate that the peak

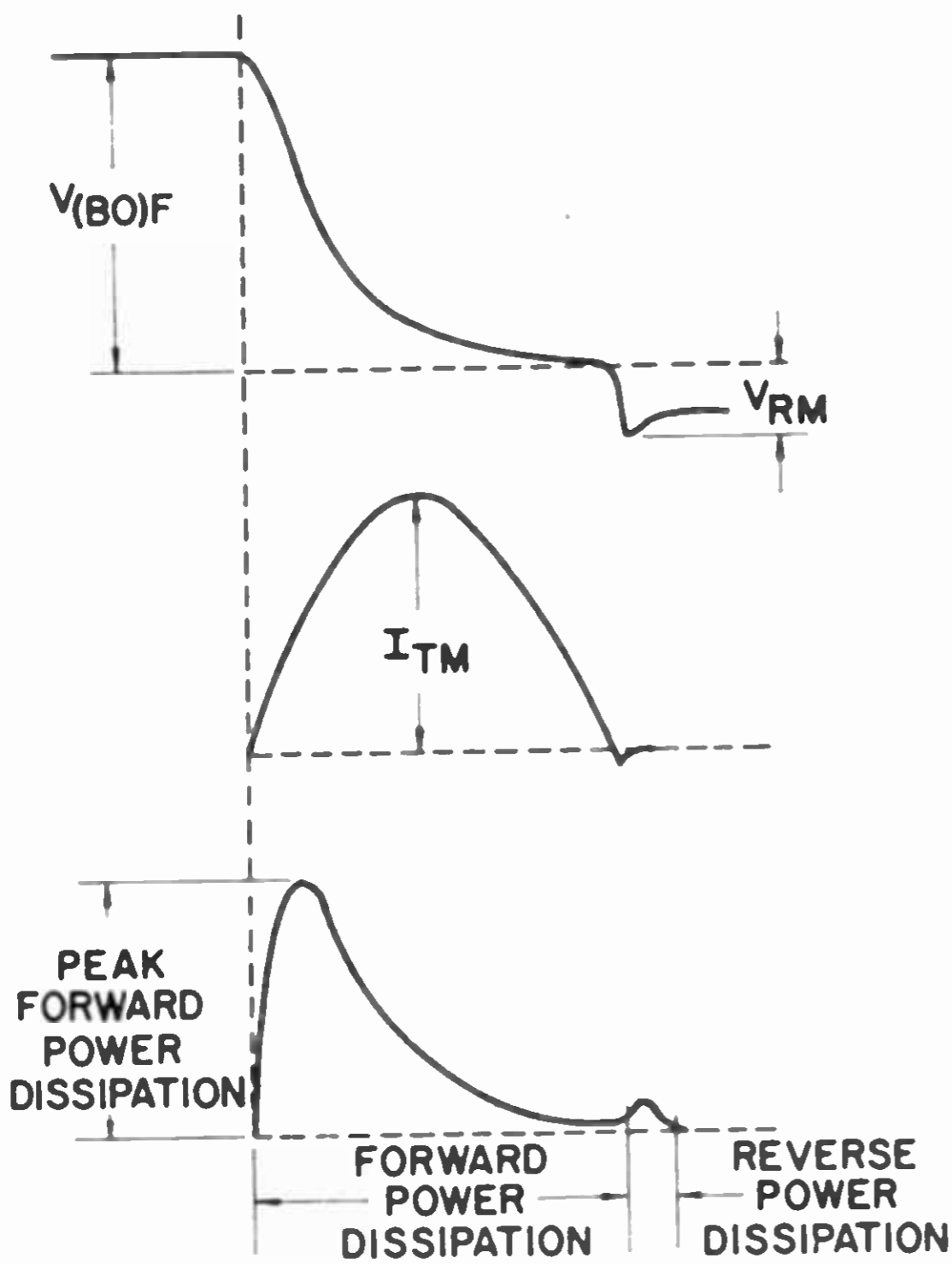


Fig. 76—Instantaneous power dissipation in a thyristor during turn-on.

power dissipation occurs in the short interval immediately after the device starts to conduct, usually in the first microsecond. During this time interval, the peak junction temperature

may exceed the maximum operating temperature given in the manufacturer's data; in this case, the thyristor should not be required to block voltages immediately after the conduction interval. If the thyristor must block voltages immediately following the conduction interval, the junction-temperature rating must not be exceeded.

The turn-off time of an SCR also consists of two stages, a reverse-recovery time and a gate-recovery time, as shown in Fig. 77. When the

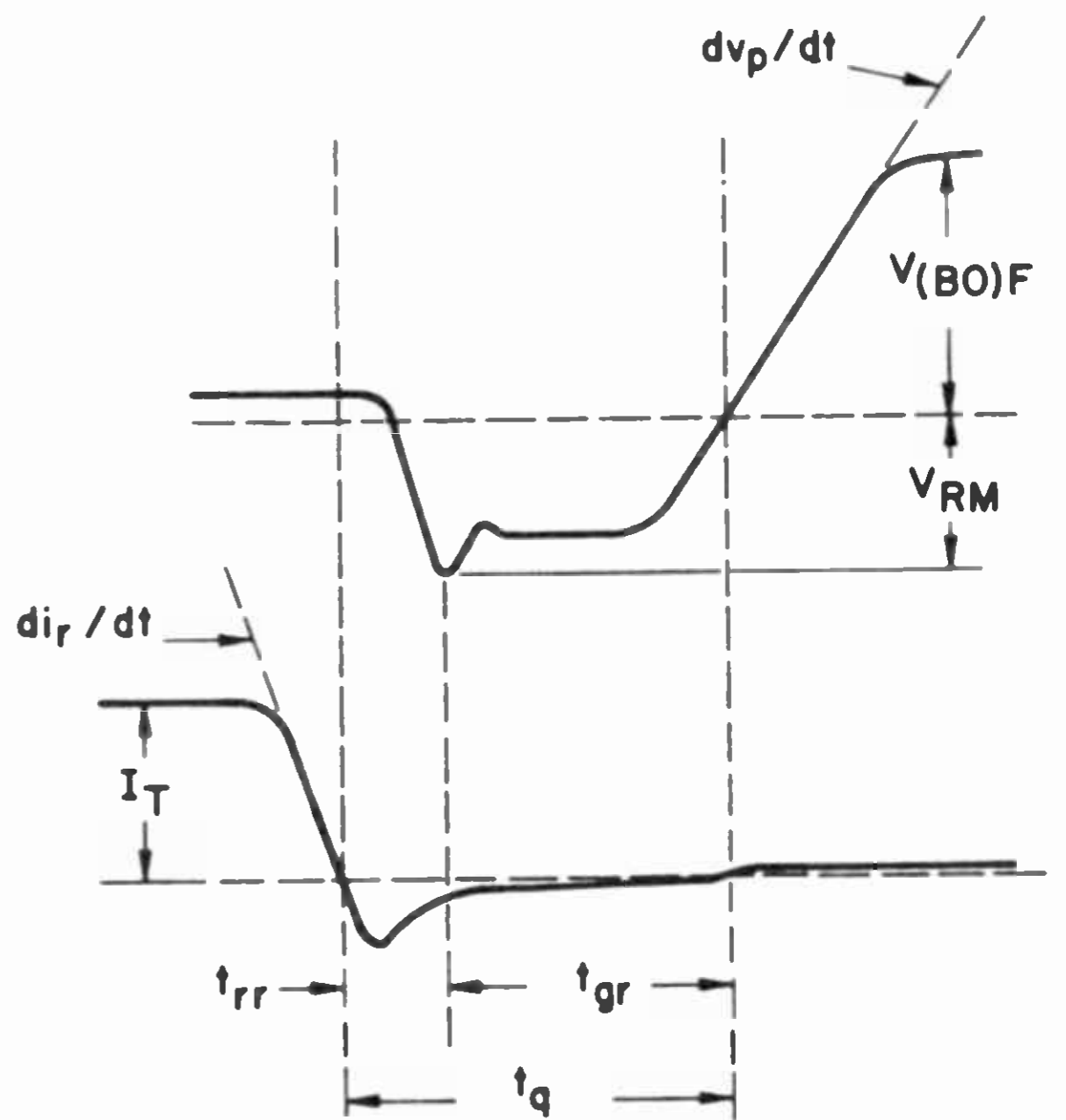


Fig. 77—Circuit-commutated turn-off voltage and current waveforms for a thyristor.

forward current of an SCR is reduced to zero at the end of a conduction period, application of reverse voltage between the anode and cathode terminals causes reverse current to flow in the SCR until the reverse-blocking junction establishes a depletion region. The time interval between the application of reverse voltage and the time that the reverse current passes its peak value to a steady-state level is called the reverse-recovery time t_{rr} . A second recovery period, called the gate-recovery time t_{gr} , must then elapse for the forward-blocking junction to establish a forward-depletion region so that forward-blocking voltage can be re-applied and successfully blocked by the SCR.

The gate-recovery time of an SCR is usually much longer than the reverse-recovery time. The total time from the instant reverse-recovery current begins to flow to the start of the re-applied forward-blocking voltage is referred to as the circuit commutated turn-off time t_g . The turn-off time is dependent upon a number of circuit parameters, including the ON-state current prior to turn-off, the rate of change of current during the forward-to-reverse transition, the reverse-blocking voltage, the rate of change of the re-applied forward voltage, the gate trigger level, the gate bias, and the junction temperature. The junction temperature and the ON-state current, however, have a more significant effect on turn-off time than any of the other factors. Because the turn-off time of an SCR depends upon a number of circuit parameters, the manufacturer's turn-off time specification is meaningful only if these critical parameters are listed and the test circuit used for the measurement is indicated.

Thyristors must be operated within the maximum ratings specified by the manufacturer to assure best results in terms of performance, life, and reliability. These ratings define limiting values, determined on the basis of extensive tests, that represent the best judgment of the manufacturer of the safe operating capability of the device.

VOLTAGE RATINGS

The voltage ratings of thyristors are given for both steady-state and transient operation and for both forward- and reverse-blocking conditions. For SCR's, voltages are considered to be in the forward or positive direction when the anode is positive with respect to the cathode. Negative voltages for SCR's are referred to as reverse-blocking voltages. For triacs, voltages are considered to be positive when main terminal No. 2 is positive with respect to main terminal No. 1. Alter-

natively, this condition may be referred to as operation in the first quadrant.

OFF-State Voltages

The repetitive peak OFF-state voltage V_{DRM} is the maximum value of OFF-state voltage, either transient or steady-state, that the thyristor should be required to block under the stated conditions of temperature and gate-to-cathode resistance. If this voltage is exceeded, the thyristor may switch to the ON state. The circuit designer should insure that the V_{DRM} rating is not exceeded to assure proper operation of the thyristor.

Under relaxed conditions of temperature or gate impedance, or when the blocking capability of the thyristor exceeds the specified rating, it may be found that a thyristor can block voltages far in excess of its repetitive OFF-state voltage rating V_{DRM} . Because the application of an excessive voltage to a thyristor may produce irreversible effects, an absolute upper limit should be imposed on the amount of voltage that may be applied to the main terminals of the device. This voltage rating is referred to as the peak OFF-state voltage V_{DM} . It should be noted that the peak OFF-state voltage has a single rating irrespective of the voltage grade of the thyristor. This rating is a function of the construction of the thyristor and of the surface properties of the pellet; it should not be exceeded under either continuous or transient conditions.

Reverse Voltages (SCR's only)

Reverse voltage ratings are given for SCR's to provide operating guidance in the third quadrant, or reverse-blocking mode. There are two voltage ratings for SCR's in the reverse-blocking mode: repetitive peak reverse voltage (V_{RRM}) and nonrepetitive peak reverse voltage (V_{RSM}).

The repetitive peak reverse voltage is the maximum allowable value of reverse voltage, including all repetitive transient voltages, that may be applied to the SCR. Because reverse power dissipation is small at this voltage, the rise in junction temperature because of this reverse dissipation is very slight and is accounted for in the rating of the SCR.

The nonrepetitive peak reverse voltage is the maximum allowable value of any nonrepetitive transient reverse voltage which may be applied to the SCR. These nonrepetitive transient voltages are allowed to exceed the steady-state ratings, even though the instantaneous power dissipation can be significant. While the transient voltage is applied, the junction temperature may increase, but removal of the transient voltage in a specified time allows the junction temperature to return to its steady-state operating temperature before a thermal runaway occurs.

ON-State Voltages

When a thyristor is in a high-conduction state, the voltage drop across the device is no different in nature from the forward-conduction voltage drop of a semiconductor diode, although the magnitude may be slightly higher. As in diodes, the ON-state voltage-drop characteristic is the major source of power losses in the operation of the thyristor, and the temperatures produced become a limiting feature in the rating of the device.

CURRENT RATINGS

The current ratings for SCR's and triacs define maximum values for normal or repetitive currents and for surge or nonrepetitive currents. These maximum ratings are determined on the basis of the maximum junction-temperature rating, the junction-to-case thermal resistance, the internal power dissipation that results from the current

flow through the thyristor, and the ambient temperature. The effect of these factors in the determination of current ratings is illustrated by the following example.

Fig. 78 shows curves of the maximum average forward power dissipation for the RCA-2N3873 SCR as a

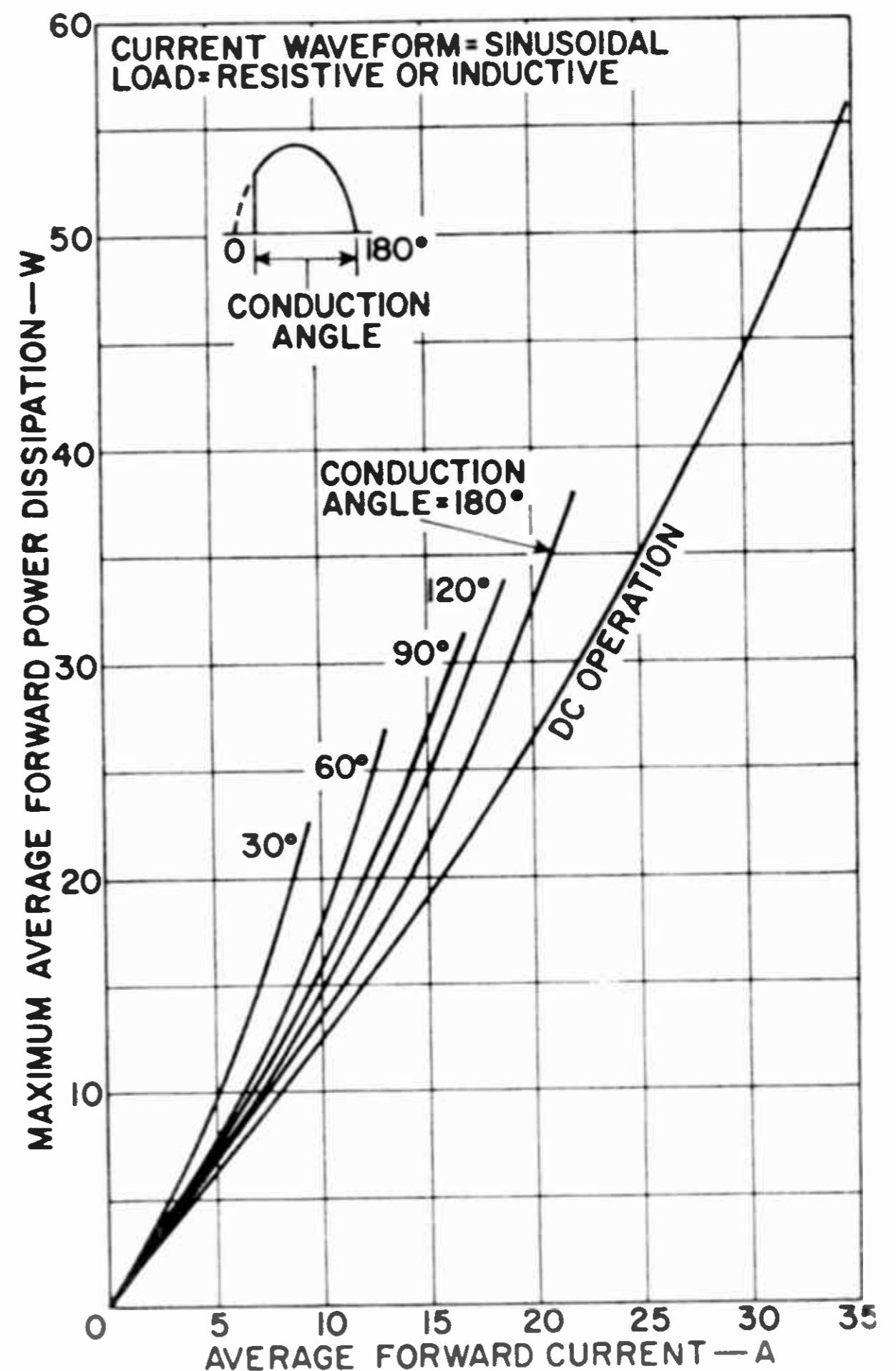


Fig. 78—Power-dissipation rating chart for the 2N3873 SCR.

function of average forward current for dc operation and for various conduction angles. For the 2N3873, the junction-to-case thermal resistance θ_{J-C} is 0.92°C per watt and the maximum operating junction temperature T_J is 100°C . If the maximum case temperature $T_{C(\text{max})}$ is assumed to be 65°C , the maximum average forward power dissipation can be determined as follows:

$$\begin{aligned} P_{\text{AVG}(\text{max})} &= \frac{T_{J(\text{max})} - T_{C(\text{max})}}{\theta_{J-C}} \\ &= \frac{(100 - 65)^{\circ}\text{C}}{0.92^{\circ}\text{C/watt}} \\ &= 38 \text{ watts} \end{aligned}$$

The maximum average forward current rating for the specified conditions can then be determined from the rating curves shown in Fig. 78. For example, if a conduction angle of 180 degrees is assumed, the average forward current rating for a maximum dissipation of 38 watts is found to be 22 amperes.

These calculations assume that the temperature is uniform throughout the pellet and the case. The junction temperature, however, increases and decreases under conditions of transient loading or periodic currents, depending upon the instantaneous power dissipated within the thyristor. The current rating takes these variations into account.

The ON-state current ratings for a thyristor indicate the maximum values of average, rms, and peak (surge) current that should be allowed to flow through the main terminals of the device, under stated conditions, when the thyristor is in the ON state. For heat-sink-mounted thyristors, these maximum ratings are based on the case temperature; for lead-mounted thyristors, the ratings are based on the ambient temperature.

The maximum average ON-state current rating is usually specified for a half-sine-wave current at a particular frequency. Fig. 79 shows curves of the maximum allowable average ON-state current $I_{TF(AVG)}$ for the RCA-2N3873 SCR family as a function of case temperature. Because peak and rms currents may be high for small conduction angles, the curves in Fig. 79 also show maximum allowable average currents as a function of conduction angle. The maximum operating junction temperature for the 2N3873 is 100°C. The rating curves indicate, for a given case temperature, the maximum average ON-state current for which the average temperature of the pellet will not exceed the maximum allowable value. The rating curves may be used for only resistive or inductive loads. When capacitive loads are used, the currents produced

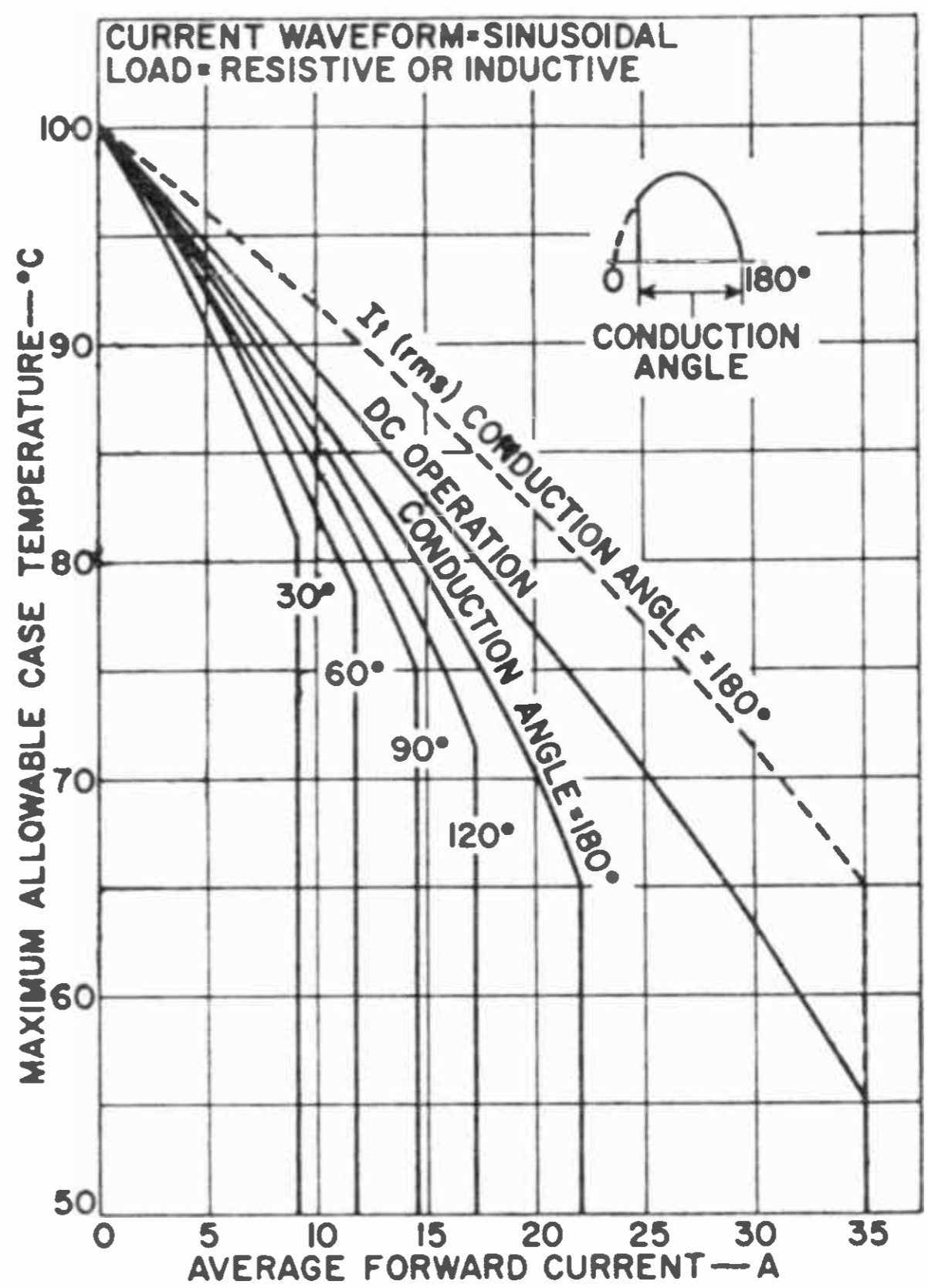


Fig. 79—Current rating chart for the 2N3873 SCR.

by the charge or discharge of the capacitor through the thyristor may be excessively high, and a resistance should be used in series with the capacitor to limit the current to the rating of the thyristor.

The ON-state current rating for a triac is given only in rms values because these devices normally conduct alternating current. Fig. 80 shows an rms ON-state current rating curve

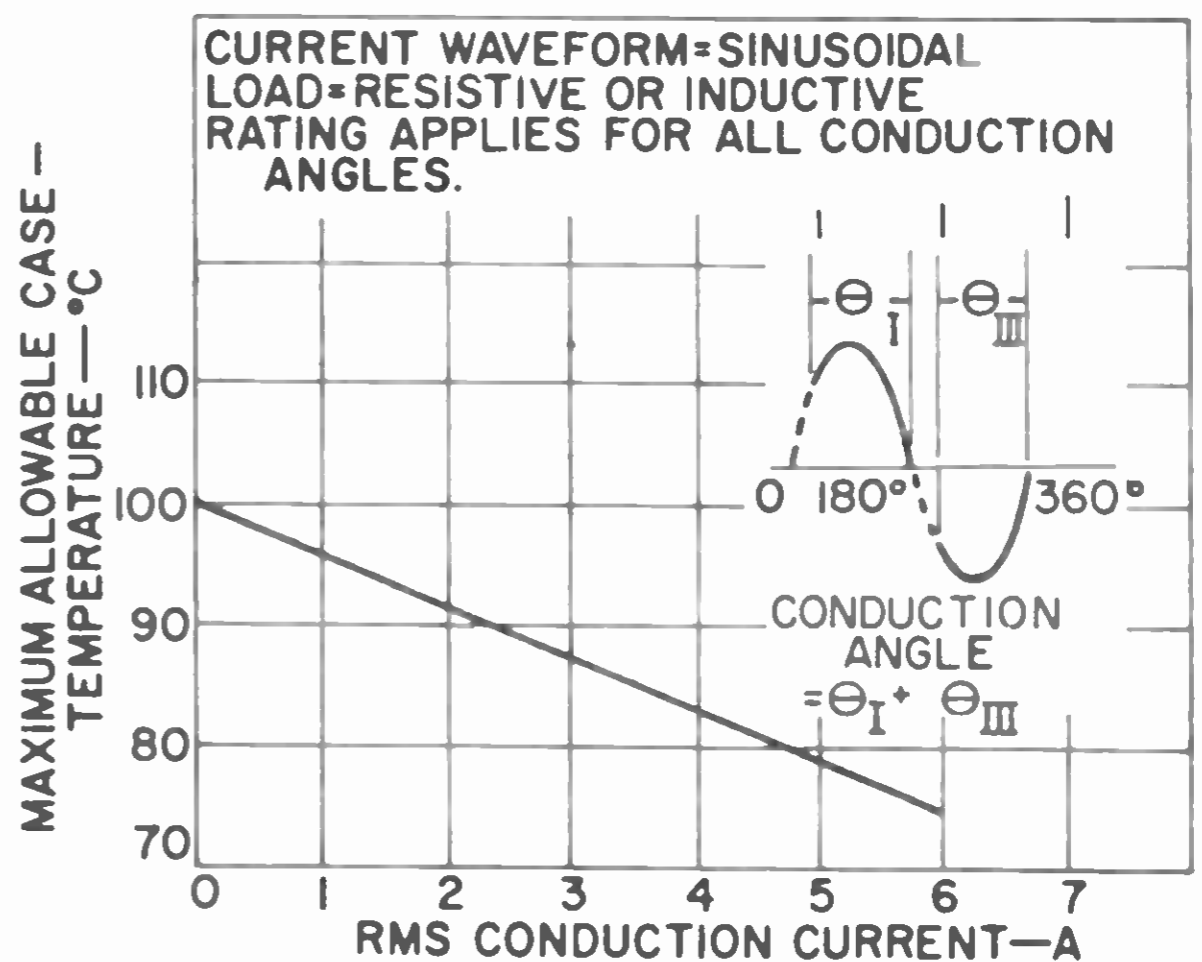


Fig. 80—Current rating curve for a typical RCA triac.

for a typical triac as a function of case temperature. As with the SCR, the triac curve is derated to zero current when the case temperature rises to the maximum operating junction temperature. Triac current ratings are given for full-wave conduction under resistive or inductive loads. Precautions should be taken to limit the peak current to tolerable levels when capacitive loads are used.

The surge ON-state current rating $I_{TF(surge)}$ indicates the maximum peak value of a short-duration current pulse that should be allowed to flow through a thyristor during one ON-state cycle, under stated conditions. This rating is applicable for any rated load condition. During normal operation, the junction temperature of a thyristor may rise to the maximum allowable value; if the surge occurs at this time, the maximum limit is exceeded. For this reason, a thyristor is not rated to block OFF-state voltage immediately following the occurrence of a current surge. Sufficient time must be allowed to permit the junction temperature to return to the normal operating value before gate control is restored to the thyristor. Fig. 81 shows a surge-current rating curve for the 2N3873

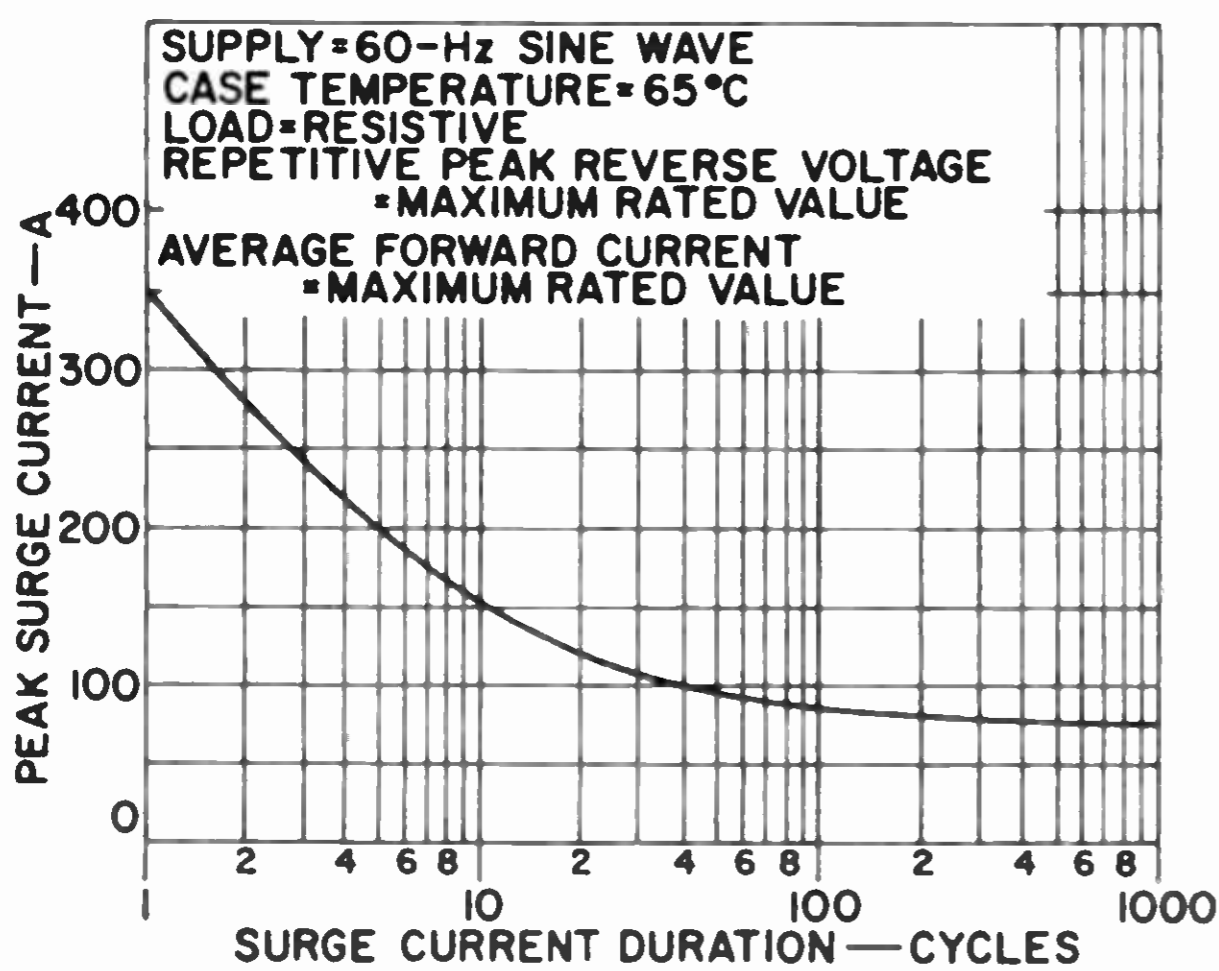


Fig. 81—Surge-current rating curve for the 2N3873 SCR.

SCR. This curve shows peak values of half-sine-wave forward (ON-state) current as a function of overload duration measured in cycles of the 60-Hz current. Fig. 82 shows surge-current rating curves for a typical

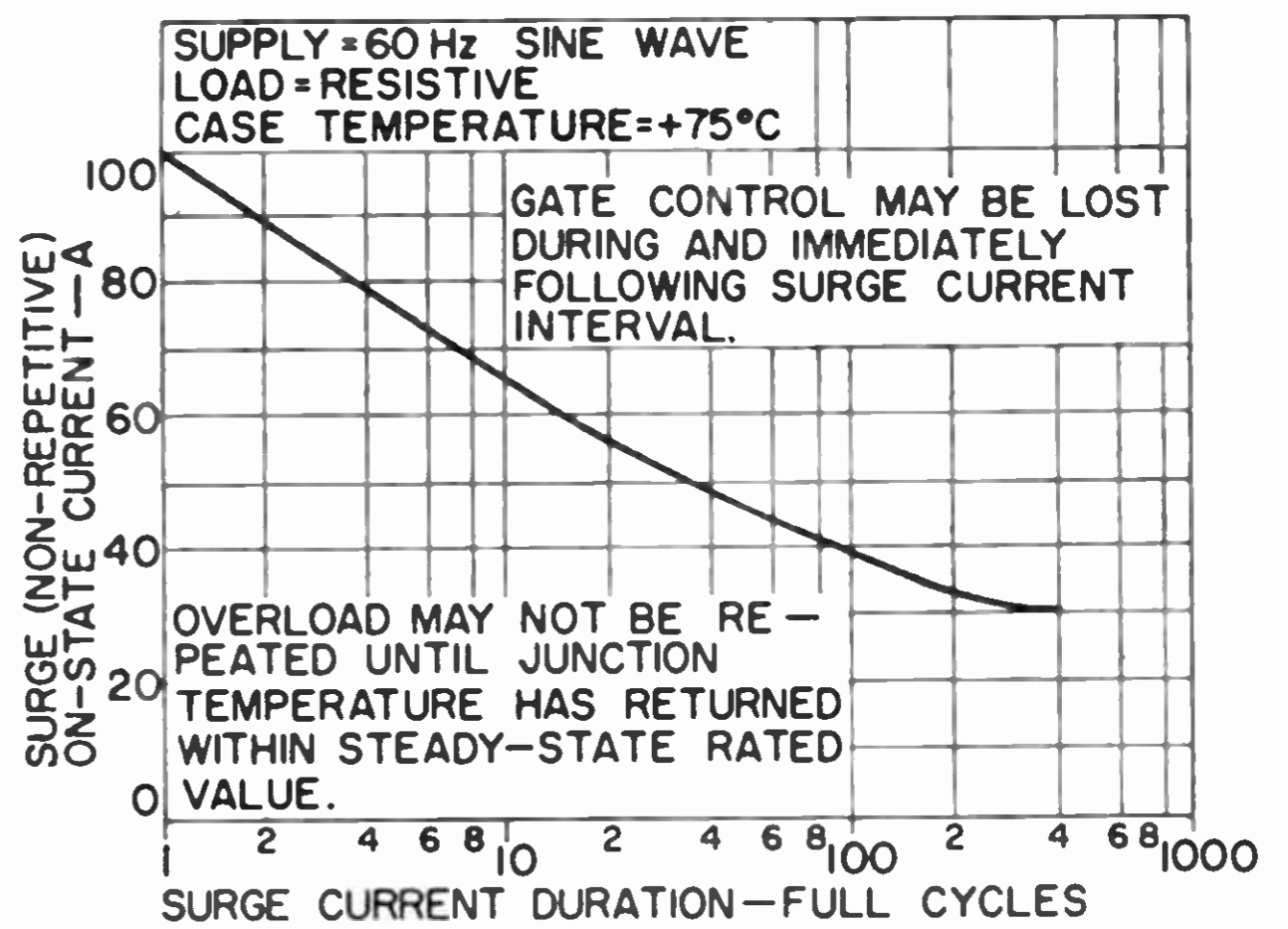


Fig. 82—Surge-current rating chart for a typical triac.

triac. For triacs, the rating curve shows peak values for a full-sine-wave current as a function of the number of cycles of overload duration. Multicycle surge curves are the basis for the selection of circuit breakers and fuses that are used to prevent damage to the thyristor in the event of accidental short-circuit of the device. The number of surges permitted over the life of the thyristor should be limited to prevent device degradation.

CRITICAL RATE OF RISE OF ON-STATE CURRENT (di/dt)

In an SCR or triac, the load current is initially concentrated in the small area of the pellet where load current first begins to flow. This small area effectively limits the amount of current that the device can handle and results in a high voltage drop across the pellet in the first microsecond after the thyristor is triggered. If the rate of rise of current is not maintained within the rating of the thyristor, localized hot spots may occur within the pellet and permanent damage to the device may result. The wave-shape for testing the di/dt capability of the RCA 2N3873 is shown in Fig. 83. The critical rate of rise of ON-state current is dependent upon the size of the cathode area that begins to conduct initially,

and the size of this area is increased for larger values of gate trigger current. For this reason, the di/dt rating is specified for a specific value of gate trigger current.

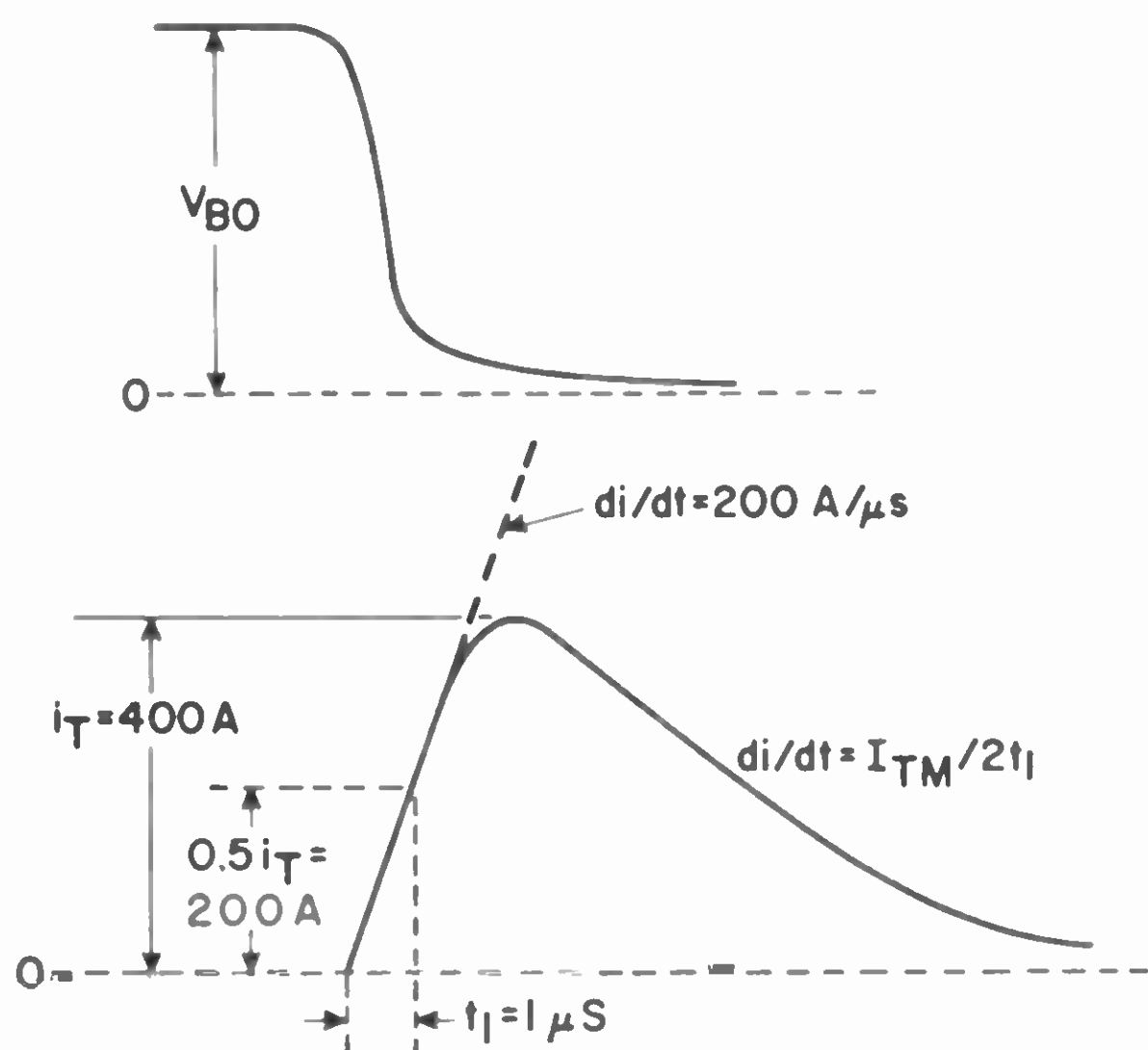


Fig. 83—Voltage and current waveforms used to determine di/dt rating of the 2N3873 SCR.

HOLDING AND LATCHING CURRENTS

After an SCR or triac has been switched to the ON-state condition, a certain minimum value of anode current is required to maintain the thyristor in this low-impedance state. If the anode current is reduced below this critical holding-current value, the thyristor cannot maintain regeneration and reverts to the OFF or high-impedance state. Because the holding current (I_H) is sensitive to changes in temperature (increases as temperature decreases), this rating is specified at room temperature with the gate open.

The latching-current rating of a thyristor specifies a value of anode current, slightly higher than the holding current, which is the minimum amount required to sustain conduction immediately after the thyristor is switched from the OFF state to the ON state and the gate signal is removed. Once the latching current (I_L) is reached, the thyristor remains in the ON, or low-impedance, state until its anode current is decreased below the holding-current value. The latching-current rating is

an important consideration when a thyristor is to be used with an inductive load because the inductance limits the rate of rise of the anode current. Precautions should be taken to insure that, under such conditions, the gate signal is present until the anode current rises to the latching value so that complete turn-on of the thyristor is assured.

CRITICAL RATE OF RISE OF OFF-STATE VOLTAGE (dv/dt)

Because of the internal capacitance of a thyristor, the forward-blocking capability of the device is sensitive to the rate at which the forward voltage is applied. A steep rising voltage impressed across the main terminals of a thyristor causes a capacitive charging current to flow through the device. This charging current ($i = Cdv/dt$) is a function of the rate of rise of the OFF-state voltage.

If the rate of rise of the forward voltage exceeds a critical value, the capacitive charging current may become large enough to trigger the thyristor. The steeper the wavefront of applied forward voltage, the smaller the value of the thyristor breakover voltage becomes.

The use of the shorted-emitter construction in SCR's has resulted in a substantial increase in the dv/dt capability of these devices by providing a shunt path around the gate-to-cathode junction. Typical units can withstand rates of voltage rise up to 200 volts per microsecond under worst-case conditions. The dv/dt capability of a thyristor decreases as the temperature rises and is increased by the addition of an external resistance from gate to reference terminal. The dv/dt rating, therefore, is given for the maximum junction temperature with the gate open, i.e., for worst-case conditions.

TRANSIENT PROTECTION

Voltage transients occur in electrical systems when some disturb-

ance disrupts the normal operation of the system. These disturbances may be produced by various sources (such as lighting surges, energizing transformers, and load switching) and may generate voltages which exceed the rating of the thyristors. In addition, transients generally have a fast rate of rise that is usually greater than the critical value for the rate of rise of the thyristor OFF-state voltage (static dv/dt).

If transient voltages have magnitudes far greater than the device rating, the thyristor may switch from the OFF state to the ON state, and energy is then transferred from the thyristor to the load. Because the internal resistance of the thyristor is high during the OFF state, the transients may cause considerable energy to be dissipated in the thyristor before breakover occurs. In such instances, the transient voltage exceeds the maximum allowable voltage rating, and irreversible damage to the thyristor may occur.

Even if the magnitude of a transient voltage is within the maximum allowable voltage rating of the thyristor, the rate of rise of the transient may exceed the static dv/dt capability of the thyristor and cause the device to switch from the OFF state to the ON state. This condition also results in transfer of energy from the thyristor to the load. In this case, thyristor switching from the OFF state to the ON state does not occur because the maximum allowable voltage is exceeded but, instead, occurs because of the fast rate of rise of OFF-state voltage (dv/dt) and the thyristor capacitance, which result in a turn-on current $i = Cdv/dt$. Thyristor switching produced in this way is free from high-energy dissipation, and turn-on is not destructive provided that the current that results from the energy transfer is within the device capability.

In either case, transient suppression techniques are employed to minimize the effects of turn-on be-

cause of overvoltage or because the thyristor dv/dt capability is exceeded.

One of the obvious solutions to insure that transients do not exceed the maximum allowable voltage rating is to provide a thyristor with a voltage rating greater than the highest transient voltage expected in a system. This technique, however, does not represent an economical solution because, in most cases, the transient magnitude, which is dependent on the source of transient generation, is not easily defined. Transient voltages as high as 2600 volts have resulted from lighting disturbances on a 120-volt residential power line. Usually, the best solution is to specify devices that can withstand voltage from 2 to 3 times the steady-state value. This technique provides a reasonable safety factor. The effects of voltage transients can further be minimized by use of external circuit elements, such as RC snubber networks across the thyristor terminals, as shown in Fig. 84. The rate at which the voltage rises at the thyristor terminal is a function of the load

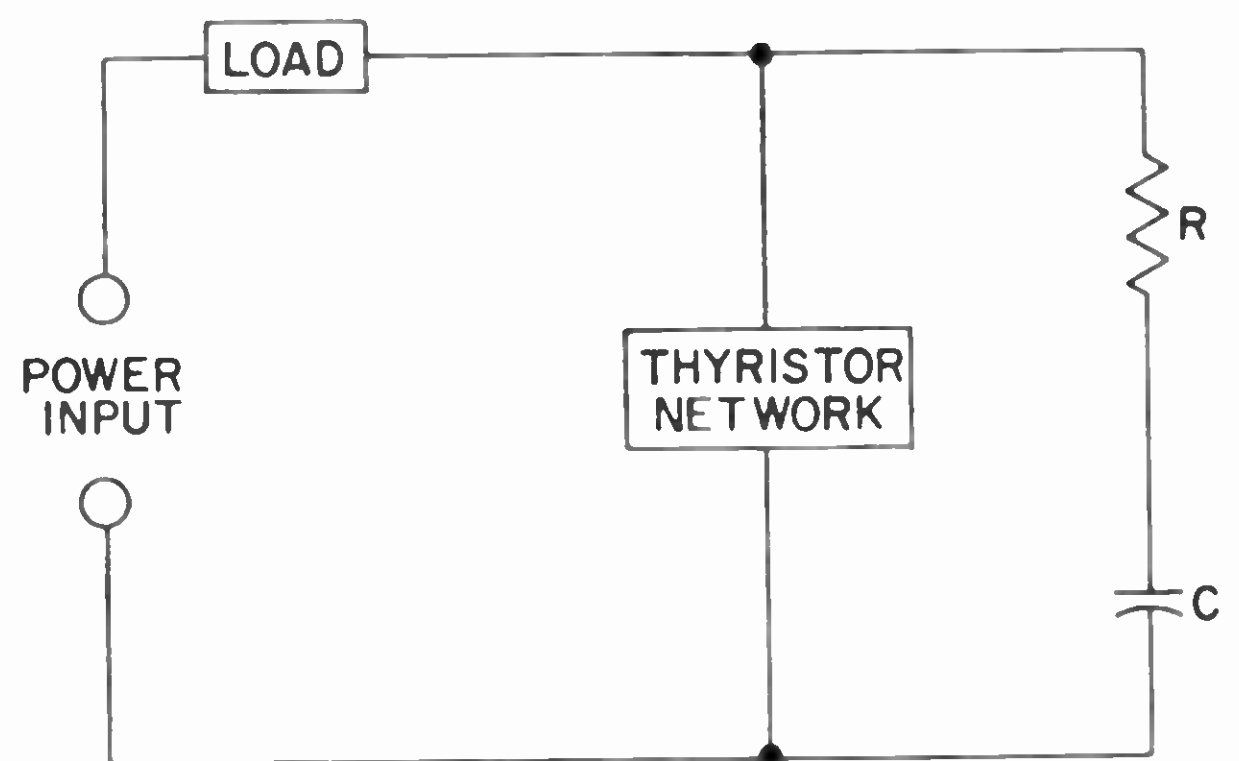


Fig. 84—Minimizing effects of voltage transients in thyristor circuit by means of an RC snubber network.

impedance and the values of the resistor R and the capacitor C in the snubber network. Because the load impedance is usually variable, the preferred approach is to assume a worst-case condition for the load and, through actual transient measurement, to select a value of C that provides the minimum rate of rise

at the thyristor terminals. The snubber resistance should be selected to minimize the capacitor discharge currents during turn-on.

For applications in which it is necessary to minimize false turn-on because of transients, the addition of a coil in series with the load, as shown in Fig. 85, is very effective for suppression of transient rise times at the thyristor terminals. For example, if a transient of

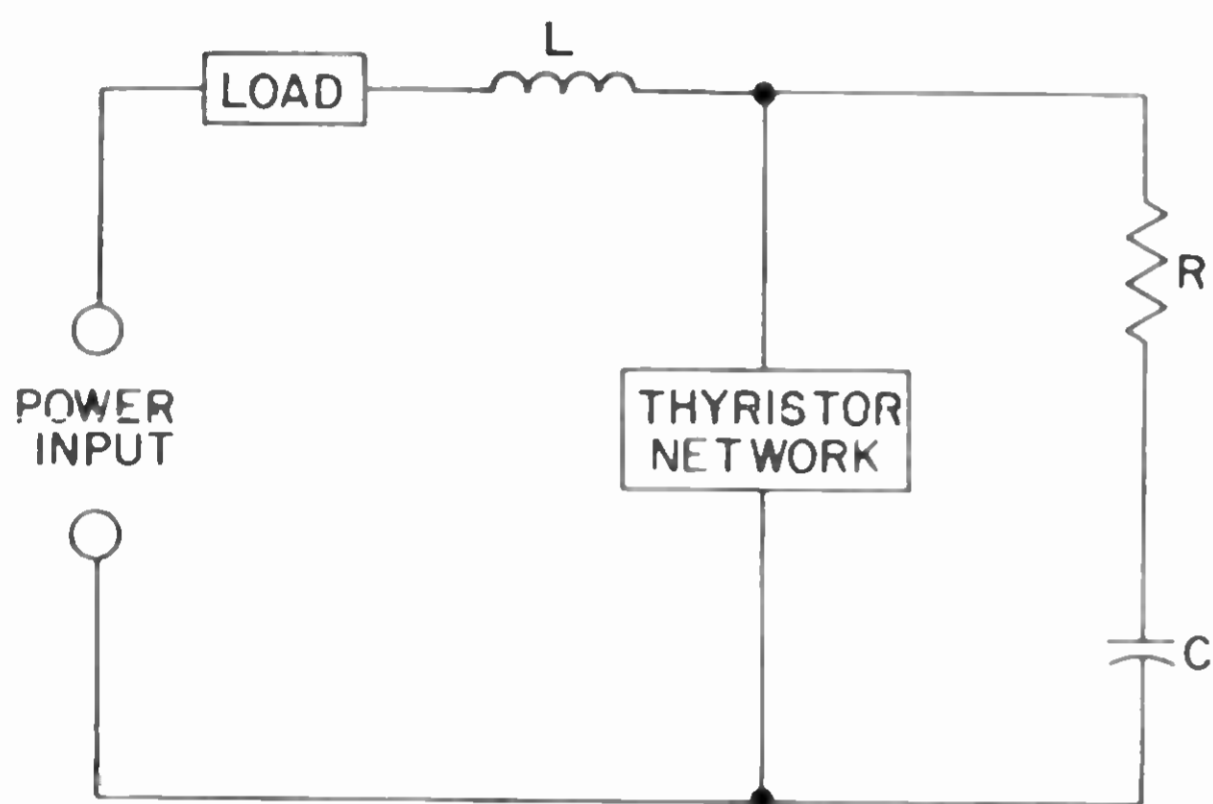


Fig. 85—Suppression of transient rise times at the terminals of a thyristor by means of a coil in series with the load.

infinite rise time is assumed to occur at the input terminals and if the effects of the load impedance are neglected, the rise time of the transient at the thyristor terminals is approximately equal to E_{pk}/\sqrt{LC} . If the value of the added inductor L is 100 microhenries and the value of the snubber capacitor C is 0.1 microfarad, the infinite rate of rise of the transient at the thyristor terminals is reduced by a factor of 3. For a filter network consisting of $L = 100$ microhenries, $C = 22$ microfarads, and $R = 47$ ohms, a 1000-volt-per-microsecond transient that appears at the input terminals is suppressed by a factor of 6 at the thyristor terminals.

RADIO-FREQUENCY INTERFERENCE

The fast switching action of triacs when they turn on into resistive loads causes the current to rise to

the instantaneous value determined by the load in a very short period of time. Triacs switch from the high to the low impedance state within 1 or 2 microseconds; the current must rise from essentially zero to full-load value during this period. This fast switching action produces a current step which is largely composed of higher-harmonic frequencies of several megahertz that have an amplitude varying inversely as the frequency. In phase-control applications, such as light dimming, this current step is produced on each half-cycle of the input voltage. Because the switching occurs many times a second, a noise pulse is generated into frequency-sensitive devices such as AM radios and causes annoying interference. The amplitude of the higher frequencies in the current step is of such low levels that they do not interfere with television or FM radio. In general, the level of radio-frequency interference (RFI) produced by the triac is well below that produced by most ac/dc brush-type electric motors; however, some type of RFI suppression network is usually added anyway.

There are two basic types of radio-frequency interference (RFI) associated with the switching action of triacs. One form, radiated RFI, consists of the high-frequency energy radiated through the air from the equipment. In most cases, this radiated RFI is insignificant unless the radio is located very close to the source of the radiation.

Of more significance is conducted RFI which is carried through the power lines and affects equipment attached to the same power lines. Because the composition of the current waveshape consists of higher frequencies, a simple choke placed in series with the load increases the current rise time and reduces the amplitude of the higher harmonics. To be effective, however, such a choke must be quite large. A more effective filter, and one that has been found adequate for most light-dimming applications is shown

in Fig. 86. The LC filter provides adequate attenuation of the high-frequency harmonics and reduces the noise interference to a low level.

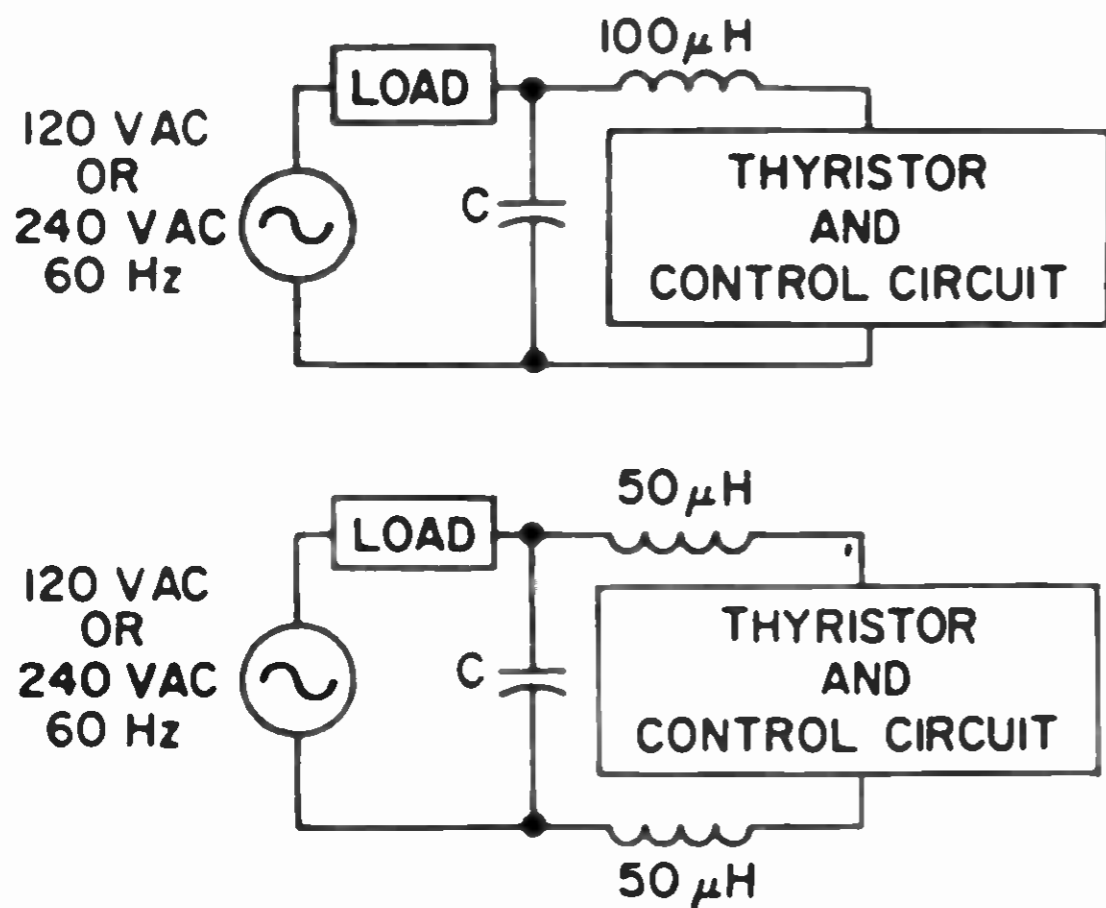


Fig. 86—RFI-suppression networks ($C = 0.1 \mu F$, 200 V at 120 V ac; $0.1 \mu F$, 400 V at 240 V ac).

The capacitor connected across the entire network bypasses high-frequency signals so that they are not

connected to any external circuits through the power lines.

Fig. 87 shows a triac control circuit that includes RFI suppression for the purpose of minimizing high-frequency interference. The values indicated are typical of those used in lamp-dimmer circuits.

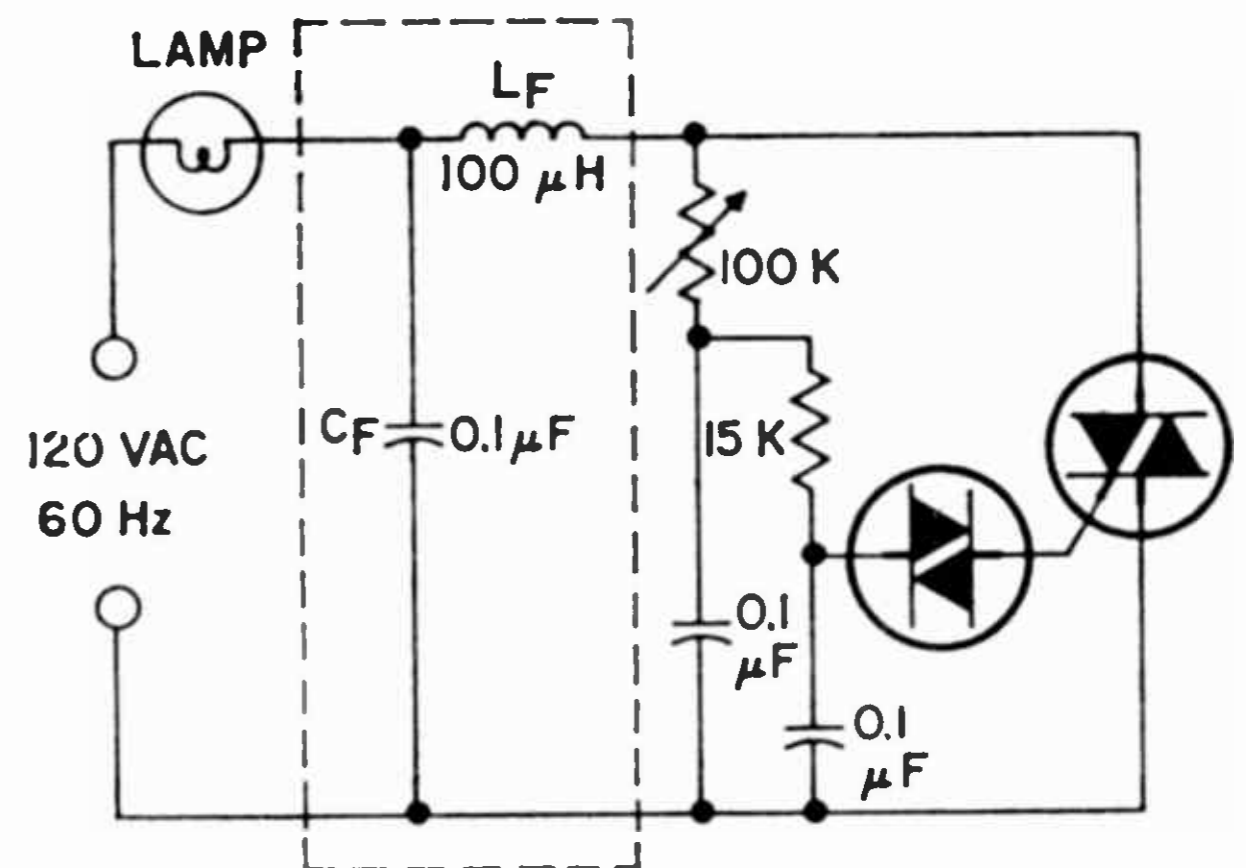


Fig. 87—Lamp-control circuit incorporating RFI suppression.

Silicon Rectifiers

SILICON rectifiers are essentially cells containing a simple p-n junction. As a result, they have low resistance to current flow in one (forward) direction, but high resistance to current flow in the opposite (reverse) direction. They can be operated at ambient temperatures up to 200°C and at current levels as high as hundreds of amperes, with voltage levels greater than 1000 volts. In addition, they can be used in parallel or series arrangements to provide higher current or voltage capabilities.

Because of their high forward-to-reverse current ratios, silicon rectifiers can achieve rectification efficiencies greater than 99 per cent. When properly used, they have excellent life characteristics which are not affected by aging, moisture, or temperature. They are very small and light-weight, and can be made impervious to shock and other severe environmental conditions.

THERMAL CONSIDERATIONS

Although rectifiers can operate at high temperatures, the thermal capacity of a silicon rectifier is quite low, and the junction temperature rises rapidly during high-current operation. Sudden rises in junction temperature caused by either high currents or excessive ambient-temperature conditions can cause failure. (A silicon rectifier is considered to have failed when either the forward voltage drop or the reverse current has increased to a point where the crystal structure or surrounding material breaks down.) Consequently,

temperature effects are very important in the consideration of silicon rectifier characteristics.

REVERSE CHARACTERISTICS

When a reverse-bias voltage is applied to a silicon rectifier, a limited amount of reverse current (usually measured in microamperes, as compared to milliamperes or amperes of forward current) begins to flow. As shown in Fig. 88, this reverse current flow increases slightly as the bias voltage increases, but then tends

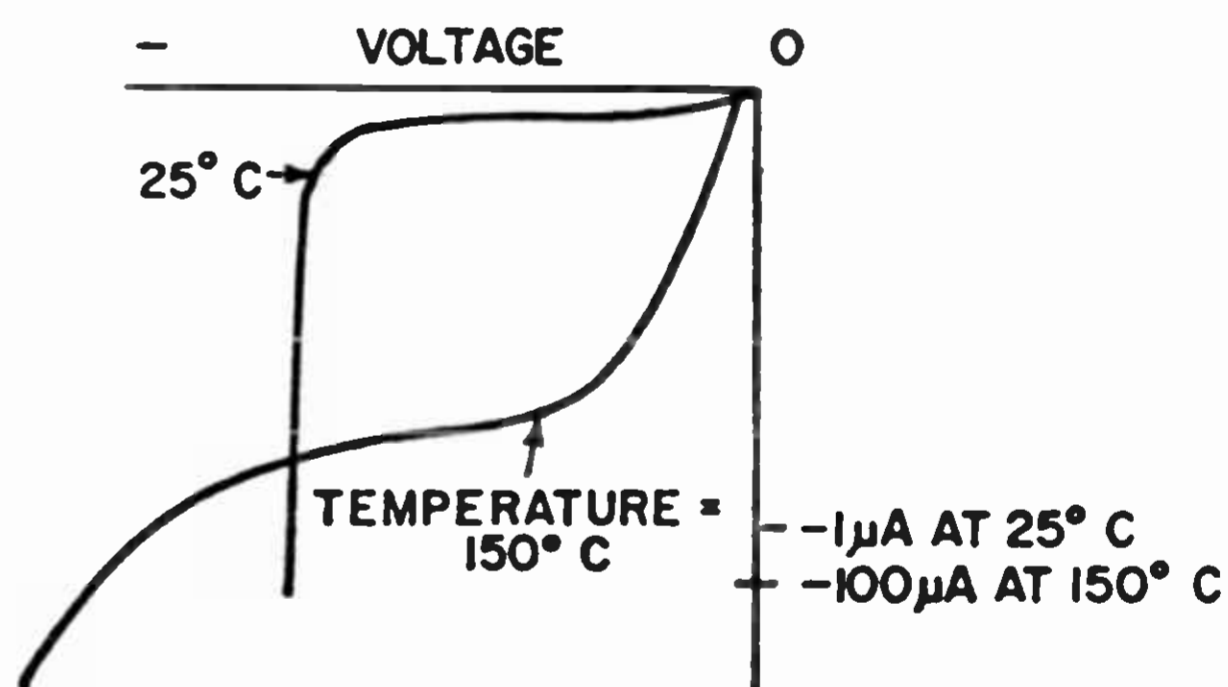


Fig. 88—Typical reverse characteristics in a silicon rectifier.

to remain constant even though the voltage continues to increase significantly. However, an increase in operating temperature increases the reverse current considerably for a given reverse bias.

At a specific reverse voltage (which varies for different types of diodes), a very sharp increase in reverse current occurs. This voltage is called the breakdown or avalanche (or zener) voltage. In many applications, rectifiers can operate safely at the avalanche point. If the reverse voltage is increased beyond this point, however, or if the ambient temperature is raised sufficiently (for ex-

ample, a rise from 25 to 150°C increases the current by a factor of several hundred), "thermal runaway" results and the diode may be destroyed.

FORWARD CHARACTERISTICS

A silicon rectifier usually requires a forward voltage of 0.4 to 0.8 volt (depending upon the temperature and the impurity concentration in the p-type and n-type materials) before significant current flow occurs. As shown in Fig. 89, a slight rise in voltage beyond this point increases the forward current sharply. Because of the small mass of the silicon rectifier, the forward voltage drop must be carefully controlled so that the specified maximum value of dissipation for the device is not exceeded. Otherwise, the diode may be seriously damaged or destroyed.

Fig. 89 shows the effects of an increase in temperature on the forward-current characteristic of a silicon

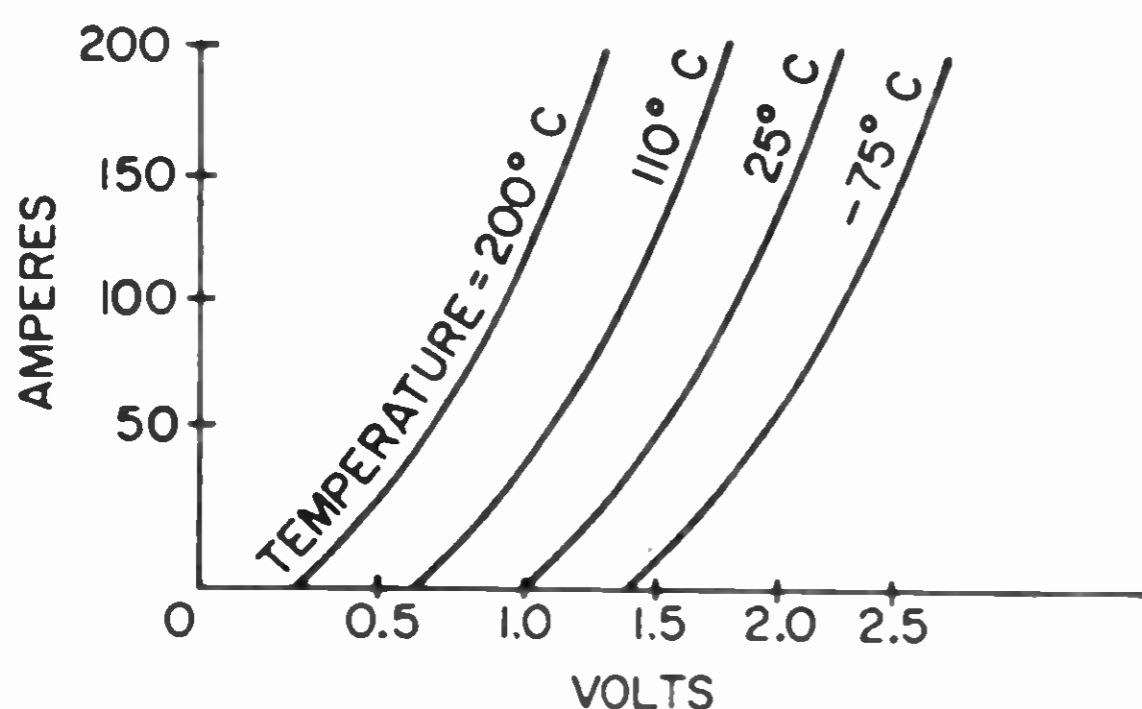


Fig. 89—Typical forward characteristics in a silicon rectifier.

rectifier. In certain applications, close control of ambient temperature is required for satisfactory operation. Close control is not usually required, however, in power circuits.

RATINGS

Ratings for silicon rectifiers are determined by the manufacturer on the basis of extensive reliability testing. One of the most important ratings is the maximum peak reverse voltage (PRV), i.e., the highest amount of reverse voltage which can be applied to a specific rectifier before the avalanche breakdown point

is reached. PRV ratings range from about 50 volts to as high as 1000 volts for some single-junction diodes. As will be discussed later, several junction diodes can be connected in series to obtain the PRV values required for very-high-voltage power-supply applications.

Because the current through a rectifier is normally not dc, current ratings are usually given in terms of average, rms, and peak values. The waveshapes shown in Figs. 90 and 91 help to illustrate the relationships among these ratings. For example, Fig. 90 shows the current variation with time of a sine wave

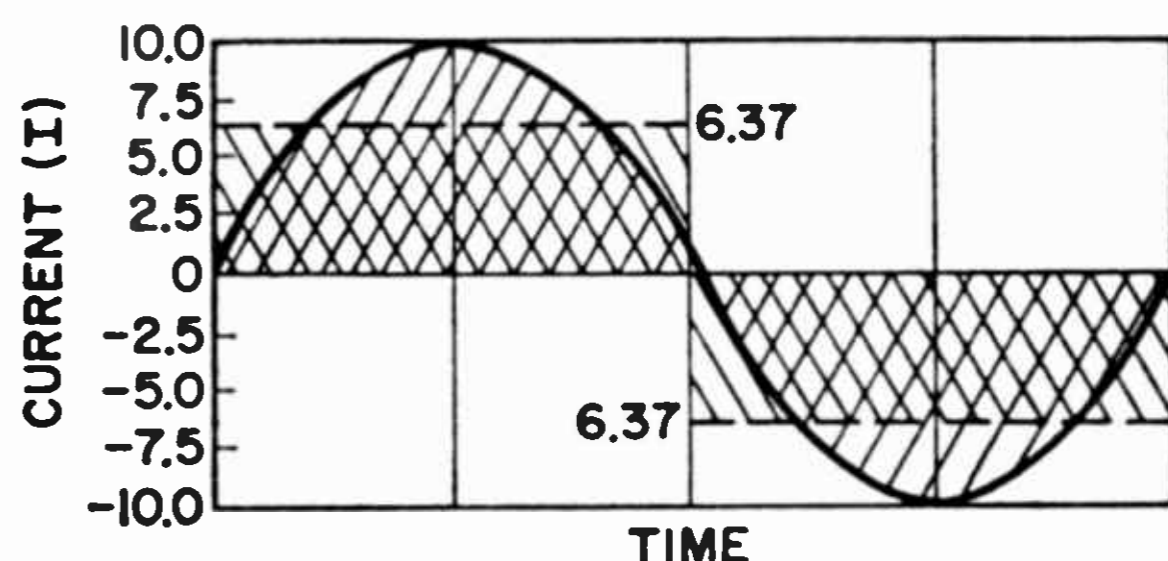


Fig. 90—Variation of current of a sine wave with time.

that has a peak current I_{peak} of 10 amperes. The area under the curve can be translated mathematically into an equivalent rectangle that indicates the average value I_{av} of the sine wave. The relationship between the average and peak values of the total sine-wave current is then given by

$$I_{\text{av}} = 0.637 I_{\text{peak}}$$

or

$$I_{\text{peak}} = 1.57 I_{\text{av}}$$

However, the power P consumed by a device (and thus the heat generated within it) is equal to the square of the current through it times its finite electrical resistance R (i.e., $P = I^2R$). Therefore, the power is proportional to the square of the current rather than to the peak or average value. Fig. 91 shows the square of the current for the sine wave of Fig. 90. A horizontal line drawn through a point halfway up the I^2 curve indicates the average (or mean) of the squares, and the square root of the I^2 value

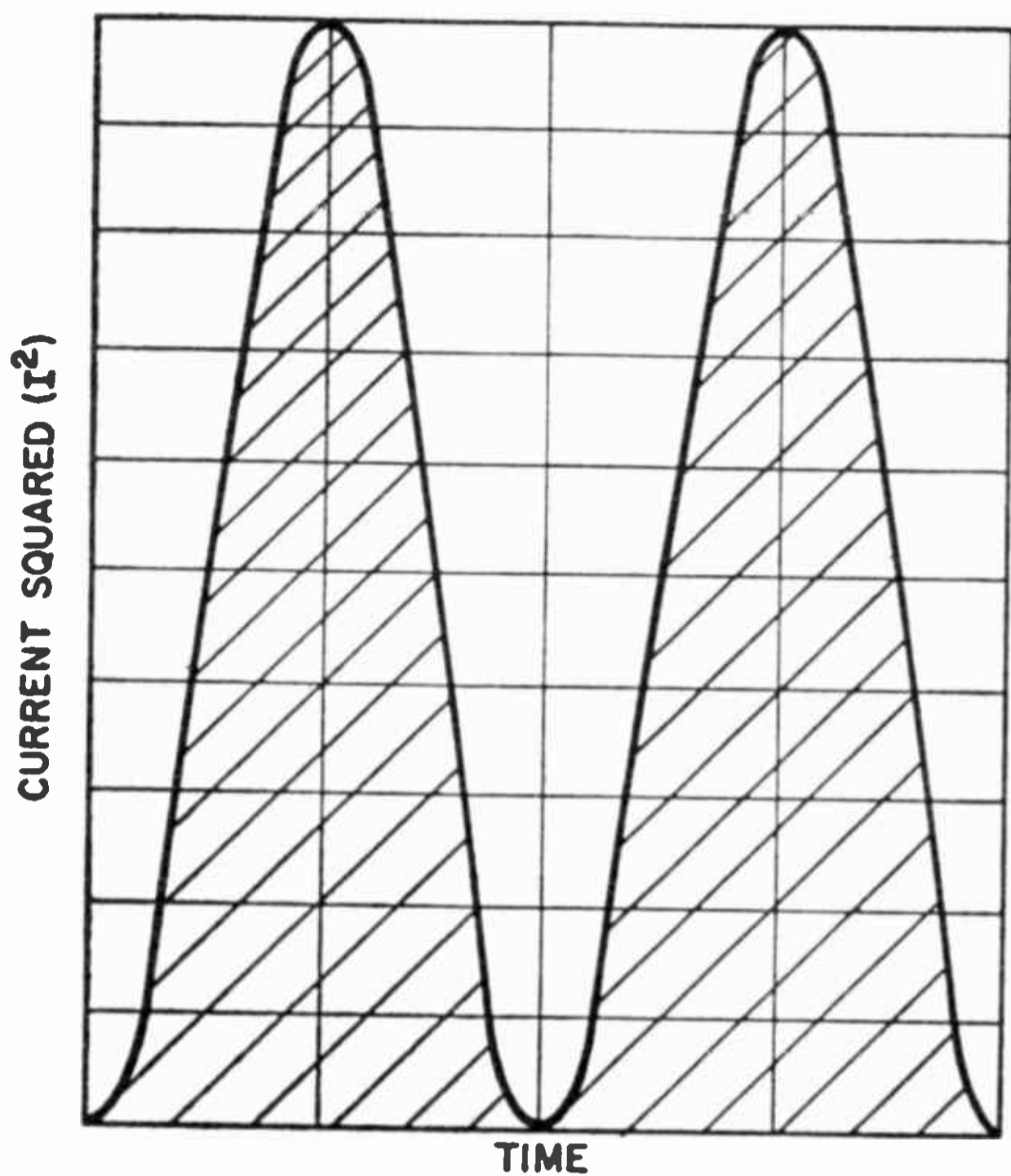


Fig. 91—Variation of the square of sine-wave current with time.

at this point is the root-mean-square (rms) value of the current. The relationship between rms and peak current is given by

$$I_{rms} = 0.707 I_{peak}$$

or

$$I_{peak} = 1.414 I_{rms}$$

Because a single rectifier cell passes current in one direction only, it conducts for only half of each cycle of an ac sine wave. Therefore, the second half of the curves in Figs. 90 and 91 is eliminated. The average current I_{av} then becomes half of the value determined for full-cycle conduction, and the rms current I_{rms} is equal to the square root of half the mean-square value for full-cycle conduction. In terms of half-cycle sine-wave conduction (as in a single-phase half-wave circuit), the relationships of the rectifier currents can be shown as follows:

$$\begin{aligned} I_{peak} &= \pi \times I_{av} = 3.14 I_{av} \\ I_{av} &= (1/\pi) I_{peak} = 0.32 I_{peak} \\ I_{rms} &= (\pi/2) I_{av} = 1.57 I_{av} \\ I_{av} &= (2/\pi) I_{rms} = 0.64 I_{rms} \\ I_{peak} &= 2 I_{rms} \\ I_{rms} &= 0.5 I_{peak} \end{aligned}$$

For different combinations of rectifier cells and different circuit con-

figurations, these relationships are, of course, changed again. Current (and voltage) relationships have been derived for various types of rectifier applications and are given in the section on DC Power Supplies.

Published data for silicon rectifiers usually include maximum ratings for both average and peak forward current. As shown in Fig. 92, the maximum average forward current is the maximum average value of current which is allowed to flow in the forward direction during a full ac cycle at a specified ambient or case temperature. Typical average current outputs range from 0.5 ampere to as high as 100 amperes for single silicon diodes. The peak recurrent forward current is the maximum repetitive instantaneous forward current permitted under stated conditions.

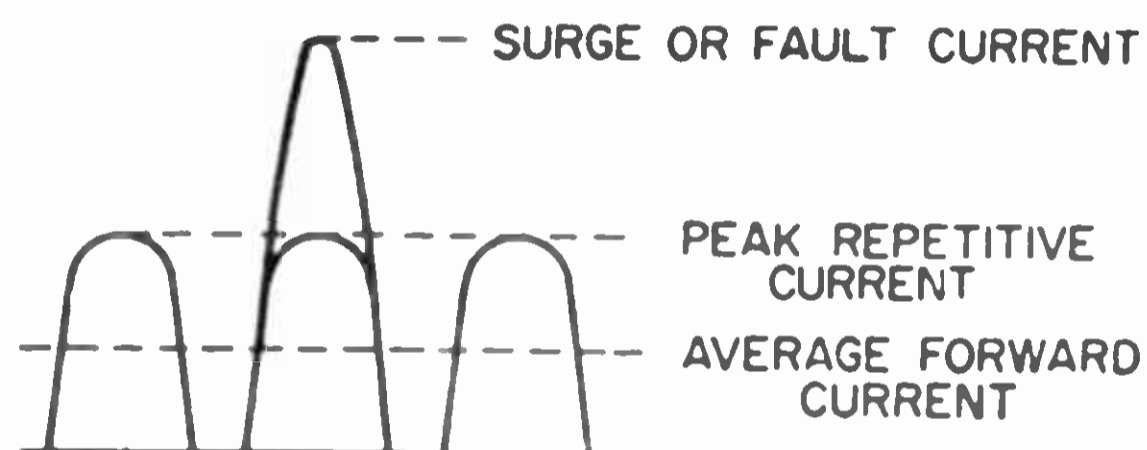


Fig. 92—Representation of rectifier currents.

In addition, ratings are usually given for non-repetitive surge, or fault, current. In rectifier applications, conditions may develop which cause momentary currents that are considerably higher than normal operating current. These increases (current surges) may occur from time to time during normal circuit operation as a result of normal load variations, or they may be caused by abnormal conditions or faults in the circuit. Although a rectifier can usually absorb a limited amount of additional heat without any effects other than a momentary rise in junction temperature, a sufficiently high surge can drive the junction temperature high enough to destroy the rectifier. Surge ratings indicate the amount of current overload or surge that the rectifier can withstand without detrimental effects.

Fig. 93 shows universal surge

rating charts for families of rectifiers having average current ratings up to 40 amperes. The rms currents shown in these charts are incremental values which add to the normal rms forward current during surge periods. The charts indicate maximum current increments that can be safely handled by the rectifiers for given lengths of time. These charts can be used by designers to determine whether circuit modifications are necessary to protect the rectifiers. If the value and duration of expected current surges are greater than the ratings for the rectifier, impedance should be added to capacitive-load circuits or fuses or circuit breakers to variable-load circuits for surge protection.

The fusing requirements for a

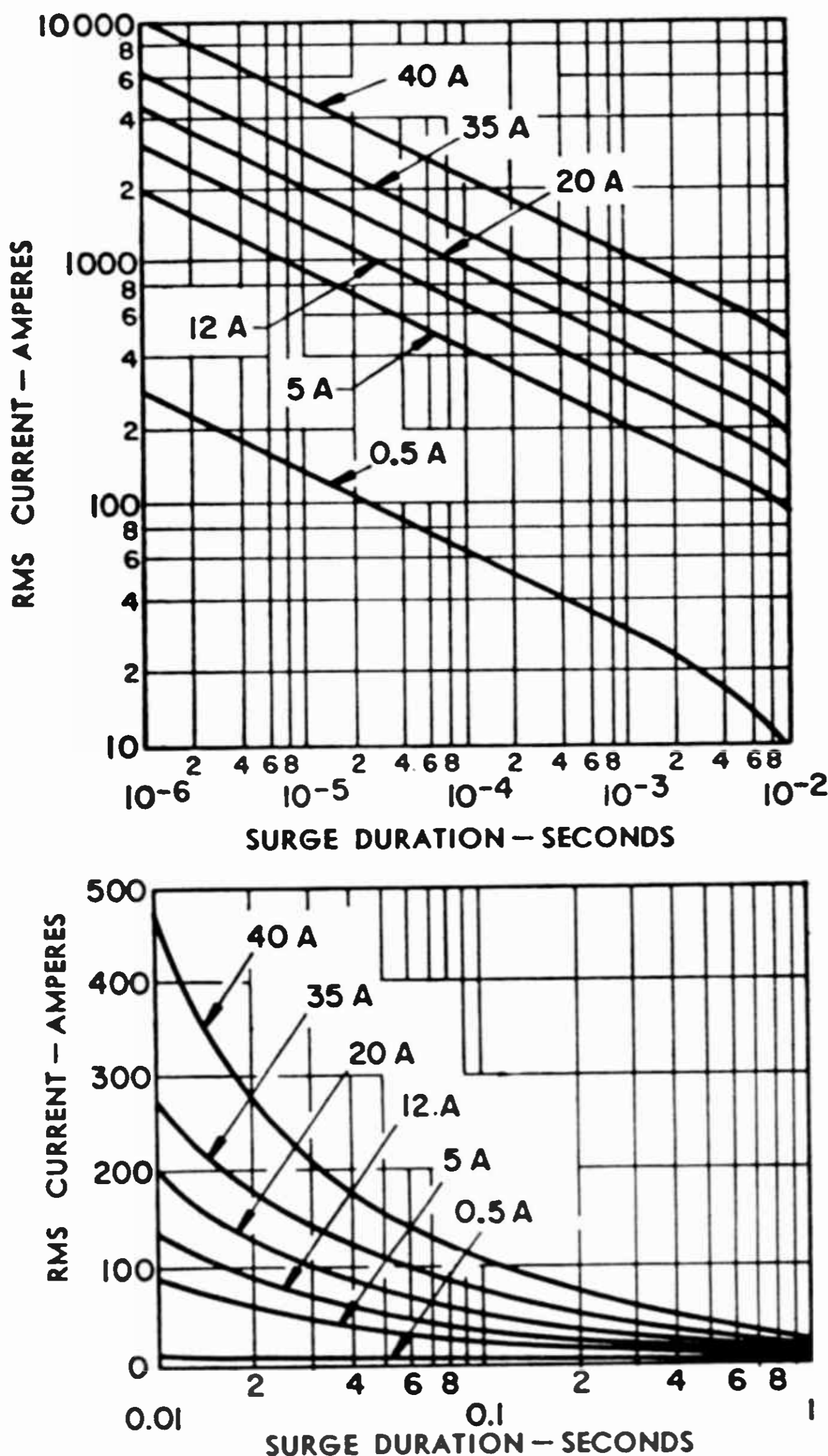


Fig. 93—Universal surge rating charts for RCA rectifiers.

given circuit can be determined by use of a coordination chart such as that shown in Fig. 94. Two characteristics are plotted on the coordination chart initially: (A) the surge rating curve for the rectifier, and

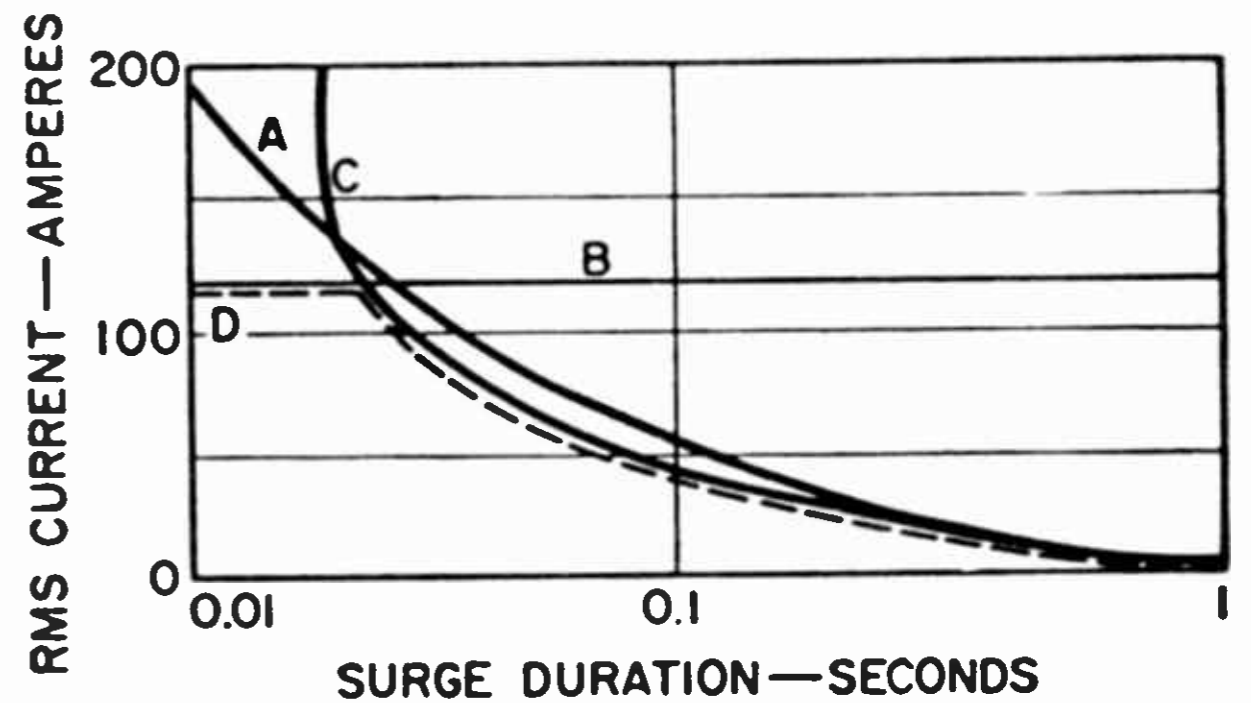


Fig. 94—Typical coordination chart for determining fusing requirements (A = surge-rating chart for 20-ampere rectifier; B = expected surge current in half-wave circuit; C = opening characteristics of protective device; D = resulting surge current in modified circuit).

(B) the maximum surge (fault current) expected in the circuit. In Fig. 94, curve A is the surge rating curve for a 20-ampere rectifier, and curve B is the maximum surge expected to occur in a single-phase half-wave rectifier circuit that has an input voltage of 600 volts and is subject to overload conditions in which the load resistance can decrease to 2 ohms. The maximum rms current which can flow under these conditions is given by

$$I_{rms} = E_{in}/2R_L = 600/4 = 150 \text{ amperes}$$

The incremental portion of this current is determined by subtracting the normal rms current of the 20-ampere rectifier ($I_{rms} = 1.57 I_{av} = 1.57 \times 20 = 31.4$ amperes; $I_{surge} = 150 - 31.4 = 118.6$ amperes). The straight line of curve B is then drawn at an rms value of 118.6 amperes in Fig. 94.

The intersection of curves A and B indicates that the 20-ampere rectifier can safely support an incremental rms surge current of 118.6 amperes for a maximum duration of about 40 milliseconds. Therefore, the circuit must be modified to include a protective element that has an

“opening” characteristic that falls below the rectifier surge rating curve for all times greater than 40 milliseconds. The opening characteristic of such a protective element is shown in Fig. 94 as curve C. Surge current in the modified circuit is then limited by the circuit resistance for periods up to 40 milliseconds and by the protective element for surges of longer duration, as shown by curve D.

Surge currents generally occur when the equipment is first turned on, or when unusual voltage transients are introduced in the ac supply line. Protection against excessive currents of this type can be provided in various ways, as will be discussed later.

Because these maximum current ratings are all affected by thermal variations, ambient-temperature conditions must be considered in the application of silicon rectifiers. Temperature-rating charts are usually provided to show the percentage by which maximum currents must be decreased for operation at temperatures higher than normal room temperature (25°C).

OVERLOAD PROTECTION

In the application of silicon rectifiers, it is necessary to guard against both over-voltage and over-current (surge) conditions. A voltage surge in a rectifier arrangement can be caused by dc switching, reverse recovery transients, transformer switching, inductive-load switching, and various other causes. The effects of such surges can be reduced by the use of a capacitor connected across the input or the output of the rectifier. In addition, the magnitude of the voltage surge can be reduced by changes in the switching elements or the sequence of switching, or by a reduction in the speed of current interruption by the switching elements.

In all applications, a rectifier having a more-than-adequate peak reverse voltage rating should be used. The safety margin for reverse volt-

age usually depends on the application. For a single-phase half-wave application using switching of the transformer primary and having no transient suppression, a rectifier having a peak reverse voltage three or four times the expected working voltage should be used. For a full-wave bridge using load switching and having adequate suppression of transients, a margin of 1.5 to 1 is generally acceptable.

Because of the small size of the silicon rectifier, excessive surge currents are particularly harmful to rectifier operation. Current surges may be caused by short circuits, capacitor inrush, dc overload, or failure of a single cell in a multiple arrangement. In the case of low-power cells, fuses or circuit breakers are often placed in the ac input circuit to the rectifier to interrupt the fault current before it damages the rectifier. When circuit requirements are such that service must be continued in case of failure of an individual diode, a number of cells can be used in parallel, each with its own fuse. Additional fuses should be used in the ac line and in series with the load for protection against dc load faults. In high-power cells, an arrangement of circuit breakers, fuses, and series resistances is often used to reduce the amplitude of the surge current. Fusing requirements can be determined by use of coordination charts for the particular circuits and rectifiers used.

SERIES AND PARALLEL ARRANGEMENTS

Silicon rectifiers can be arranged in series or in parallel to provide higher voltage or current capabilities, respectively, as required for specific applications.

A parallel arrangement of rectifiers can be used when the maximum average forward current required is larger than the maximum current rating of an individual rectifier cell. In such arrangements, however, some means must be provided to assure proper division of current

through the parallel rectifier cells. Parallel rectifier arrangements are not in general use. Designers normally use a polyphase arrangement to provide higher currents, or simply substitute the readily available higher-current rectifier types.

Series arrangements of silicon rectifiers are used when the applied reverse voltage is expected to be greater than the maximum peak reverse voltage rating of a single silicon rectifier (or cell). For example, four rectifiers having a maximum reverse voltage rating of 200 volts each could be connected in series to handle an applied reverse voltage of 800 volts.

In a series arrangement, the most important consideration is that the applied voltage be divided equally across the individual rectifiers. If the instantaneous voltage is not uniformly divided, one of the rectifiers may be subjected to a voltage greater than its specified maximum reverse voltage, and, as a result, may be destroyed. Uniform voltage division can usually be assured by connection of either resistors or capacitors in parallel with individual cells. Shunt

resistors are used in steady-state applications, and shunt capacitors in applications in which transient voltages are expected. Both resistors and capacitors should be used if the circuit is to be exposed to both dc and ac components. When only a few diodes are in series, multiple transformer windings may be used, each winding supplying its own assembly consisting of one series diode. The outputs of the diodes are then connected in series for the desired voltage.

RCA rectifier stacks (CR101, CR201, and CR301 series) are designed to provide equal reverse voltage across the individual rectifier cells in the assembly under both steady-state and transient conditions. The CR101 and CR301 series stacks include an integral resistance-capacitance network to equalize the reverse voltage across the series-connected rectifier cells. The CR201 series stacks use precisely matched rectifier cells for internal voltage equalization. Extended life tests have shown that these rectifier stacks are capable of operating for many thousands of hours without noticeable degradation of performance.

Other Semiconductor Diodes

TUNNEL DIODES

A TUNNEL diode is a small p-n junction device having a very high concentration of impurities in the p-type and n-type semiconductor materials. This high impurity density makes the junction depletion region (or space-charge region) so narrow that electrical charges can transfer across the junction by a quantum-mechanical action called "tunneling". This tunneling effect provides a negative-resistance region on the characteristic curve of the device that makes it possible to achieve amplification, pulse generation, and rf-energy generation.

Characteristics

Typical current-voltage characteristics for a tunnel diode are shown in Fig. 95. Conventional diodes do

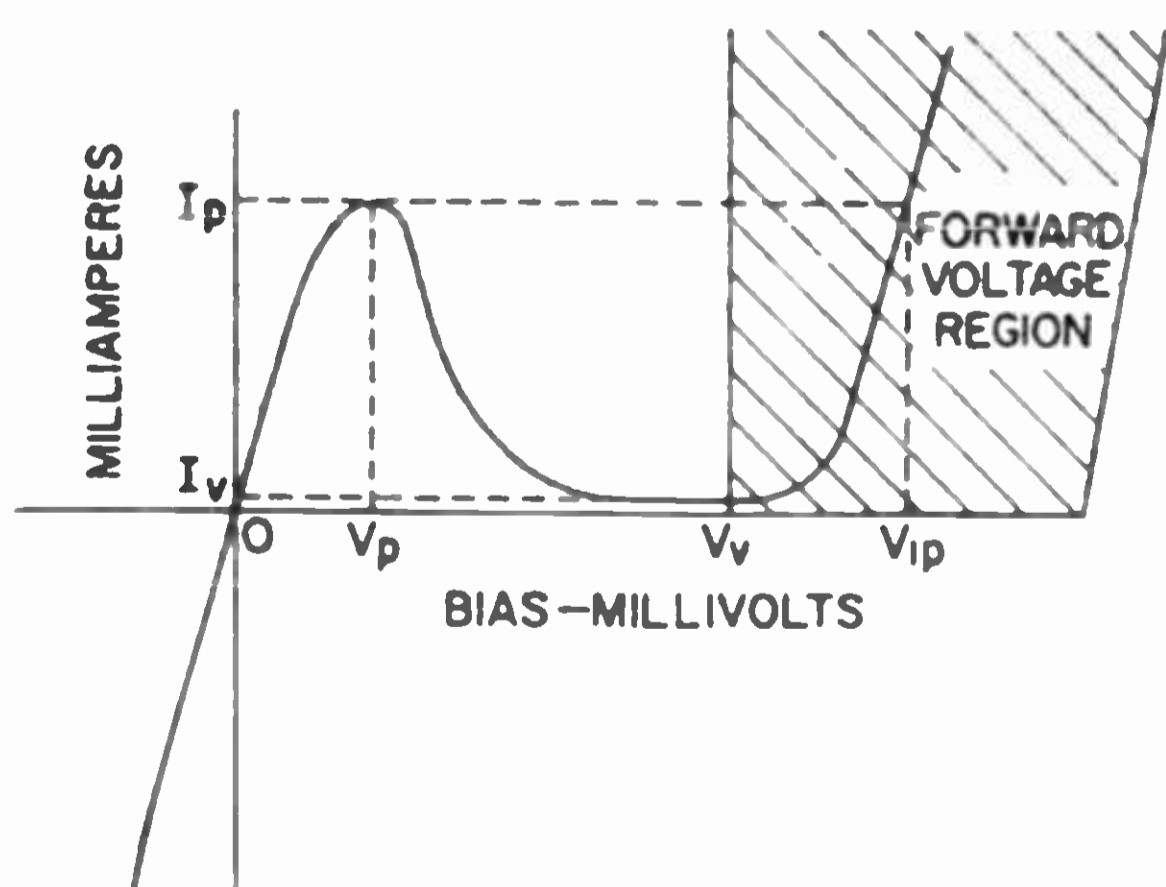


Fig. 95—Typical current-voltage characteristic of a tunnel diode.

not conduct current under conditions of reverse bias until the breakdown voltage is reached; under forward bias they begin to conduct at ap-

proximately 300 millivolts. In tunnel diodes, however, a small reverse bias causes the valence electrons of semiconductor atoms near the junction to "tunnel" across the junction from the p-type region into the n-type region; as a result, the tunnel diode is highly conductive for all reverse biases. Similarly, under conditions of small forward bias, the electrons in the n-type region "tunnel" across the junction to the p-type region and the tunnel-diode current rises rapidly to a sharp maximum peak I_p . At intermediate values of forward bias, the tunnel diode exhibits a negative-resistance characteristic and the current drops to a deep minimum valley point I_v . At higher values of forward bias, the tunnel diode exhibits the diode characteristic associated with conventional semiconductor current flow. The decreasing current with increasing forward bias in the negative-resistance region of the characteristic provides the tunnel diode with its ability to amplify, oscillate, and switch.

Equivalent Circuit

In the equivalent circuit for a tunnel diode shown in Fig. 96, the n-type and p-type regions are shown as

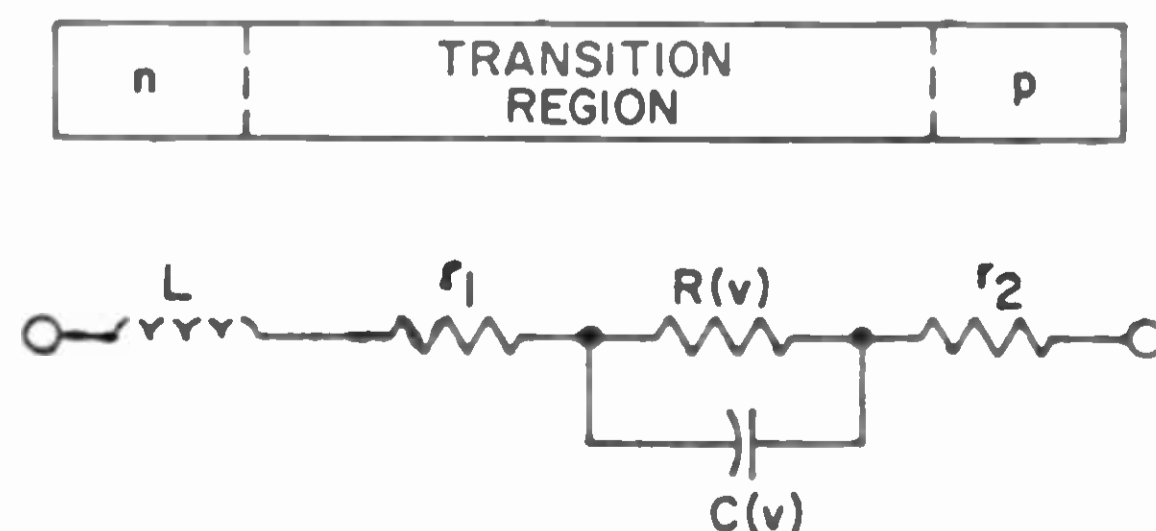


Fig. 96—Equivalent circuit for a tunnel diode.

pure resistances r_1 and r_2 . The transition region is represented as a voltage-sensitive resistance $R(v)$ in parallel with a voltage-sensitive capacitance $C(v)$ because tunneling is a function of both voltage and junction capacitance. This capacitance is similar to that of a parallel-plate capacitor having plates separated by the transition region.

The dashed portion L in Fig. 96 represents an inductance which results from the case and mounting of the tunnel diode. This inductance is unimportant for low-frequency diodes, but becomes increasingly important at high frequencies (above 100 MHz).

Fig. 97 shows the form of the equivalent circuit when the diode is biased so that its operating point is in the negative-resistance region; dynamic characteristics of tunnel diodes are defined with respect to this circuit. L_S represents the total series inductance, and R_S the total series resistance. C_D is the capacitance and $-R_D$ is the negative resistance of the diode. For small signal variations, both the resistance R_D and the capacitance C_D are constant.

The figure of merit F of a tunnel diode is equal to the reciprocal of $2\pi RC$, where R and C are the equivalent values $-R_D$ and C_D , respectively, shown in Fig. 97. This expression has two very useful interpretations:

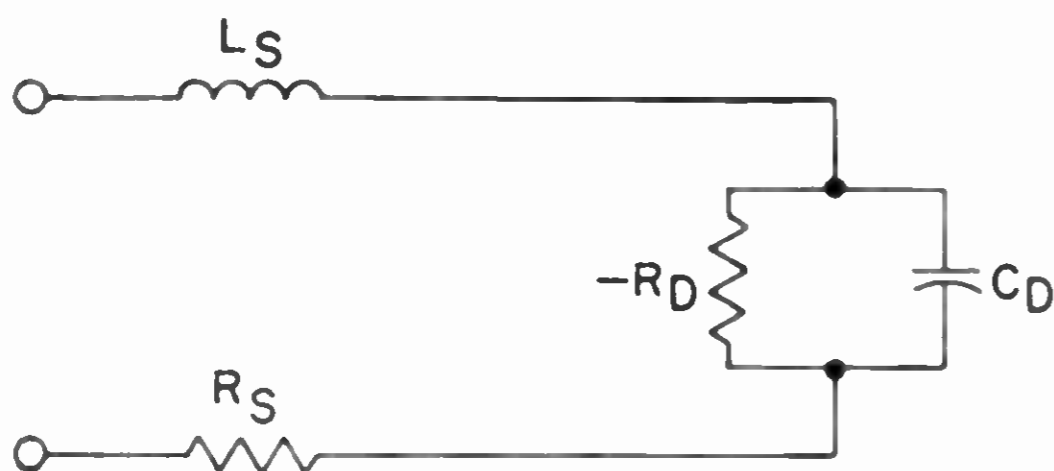


Fig. 97—Equivalent circuit for a tunnel diode biased in the negative-resistance region.

(1) it is the diode gain-bandwidth product for circuits operating in the linear negative-resistance region of the characteristic, and (2) its reciprocal is the diode switching time when the device is used as a logic element.

Operating Point

When the tunnel diode is used in circuits such as amplifiers and oscillators, the operating point must be established in the negative-resistance region. The dc load line, shown as a solid line in Fig. 98, must be very steep so that it intersects the static characteristic curve at only one point A . The ac load line can be either steep with only one intersection B , as in the case of an amplifier, or relatively flat with three intersections C , D , and E , as in the case of an oscillator. The location of the op-

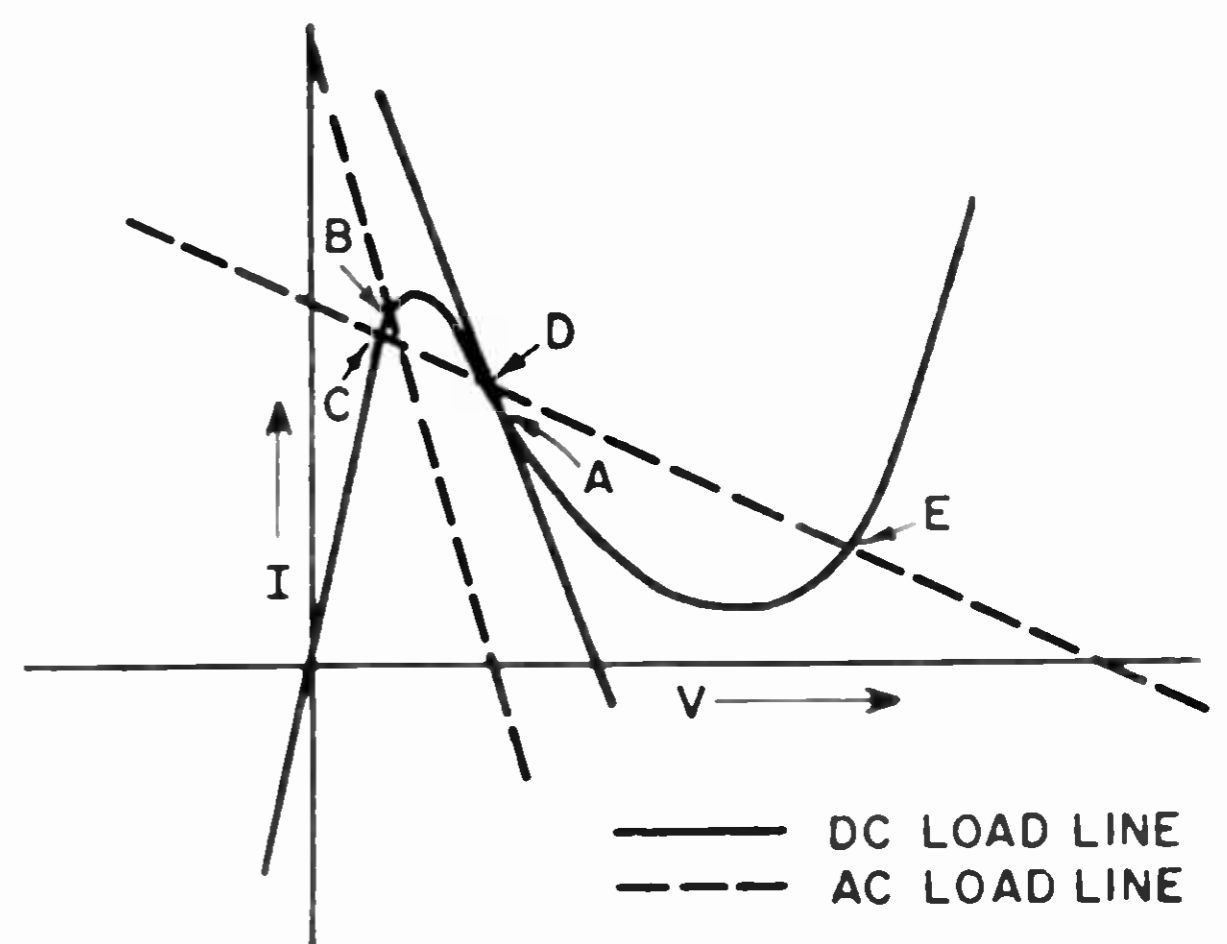


Fig. 98—Typical load lines for tunnel diode circuits.

erating point is determined by the anticipated signal swing, the required signal-to-noise ratio, and the operating temperature of the device. Biasing at the center of the linear portion of the negative-resistance slope permits the greatest signal swing. For high-temperature operation, a higher operating current is chosen; for low noise, the device is operated at the lowest possible bias current.

Radiation and Thermal Considerations

One of the most important features of the tunnel diode is its resistance to nuclear radiation. Experimental results have shown tunnel diodes to be at least ten times more resistant to radiation than transistors. Because the resistivity of tunnel diodes is so low initially, it is not critically affected by radiation until large doses

have been applied. In addition, tunnel diodes are less affected by ionizing radiation because they are relatively insensitive to surface changes produced by such radiation.

In general, the tunnel-diode voltage-current characteristic is relatively independent of temperature. Specific tunnel-diode applications may be affected, however, by the relative temperature dependence of the various circuit components. In such applications, negative feedback or direct (circuit) compensation may be required.

TUNNEL RECTIFIERS

In addition to its negative-resistance properties, the tunnel diode has an efficient rectification characteristic which can be used in many rectifier applications. When a tunnel diode is used in a circuit in such a way that this rectification property is emphasized rather than its negative-resistance characteristic, it is called a tunnel rectifier. In general, the peak current for a tunnel rectifier is less than one milliampere.

The major differences in the current-voltage characteristics of tunnel rectifiers and conventional rectifiers are shown in Fig. 99. In conventional rectifiers, current flow is substantial in the forward direction, but

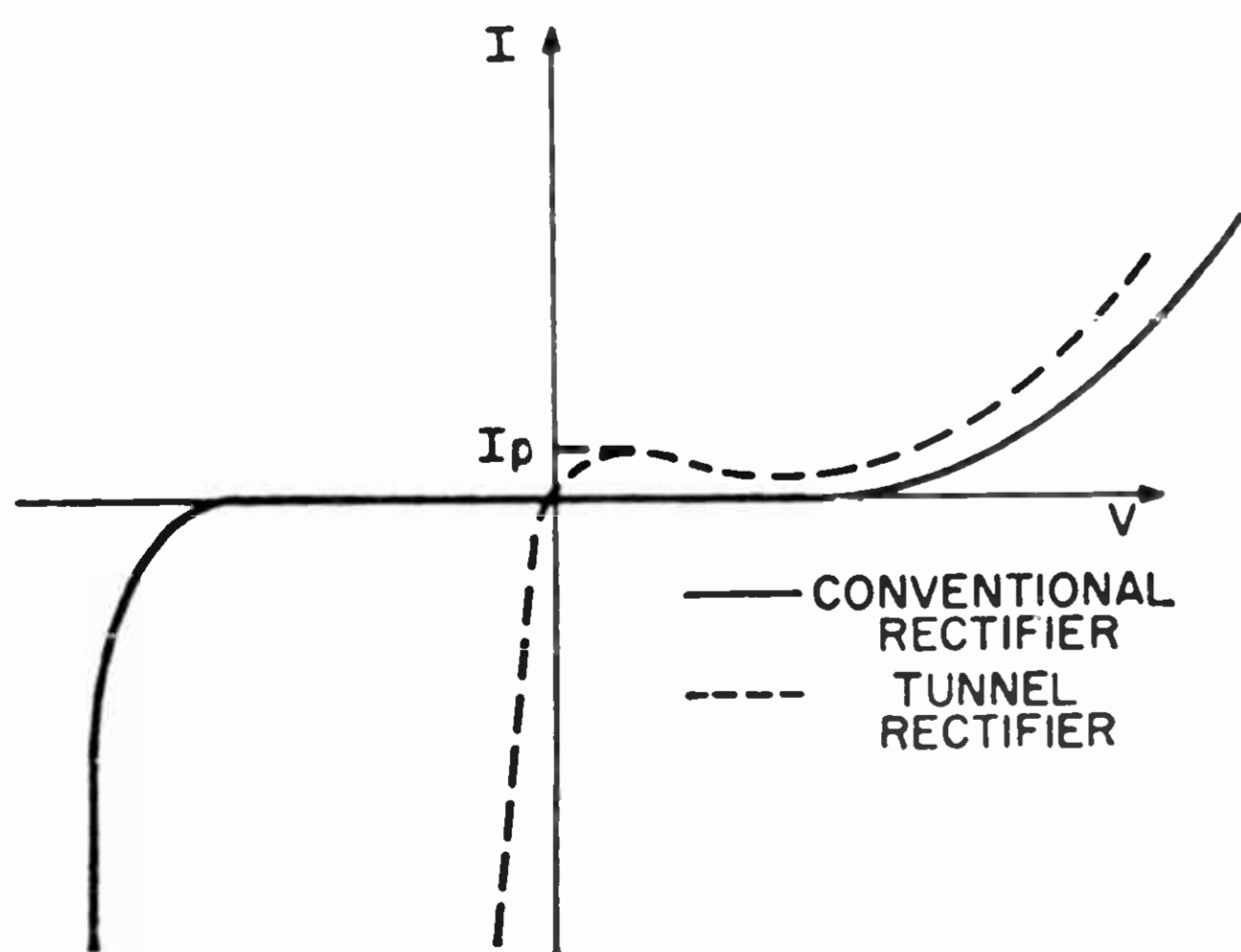


Fig. 99—Current-voltage characteristics of tunnel rectifier and conventional rectifier.

extremely small in the reverse direction (for signal voltages less than the breakdown voltage for the device). In tunnel rectifiers, however,

substantial reverse current flows at very low voltages, while forward current is relatively small. Consequently, tunnel rectifiers can provide rectification at smaller signal voltages than conventional rectifiers, although their polarity requirements are opposite. (For this reason, tunnel rectifiers are sometimes called "back diodes.")

Because of their high-speed capability and superior rectification characteristics, tunnel rectifiers can be used to provide coupling in one direction and isolation in the opposite direction. Fig. 100 shows the use of tunnel rectifiers to provide directional coupling in a tunnel-diode logic circuit.

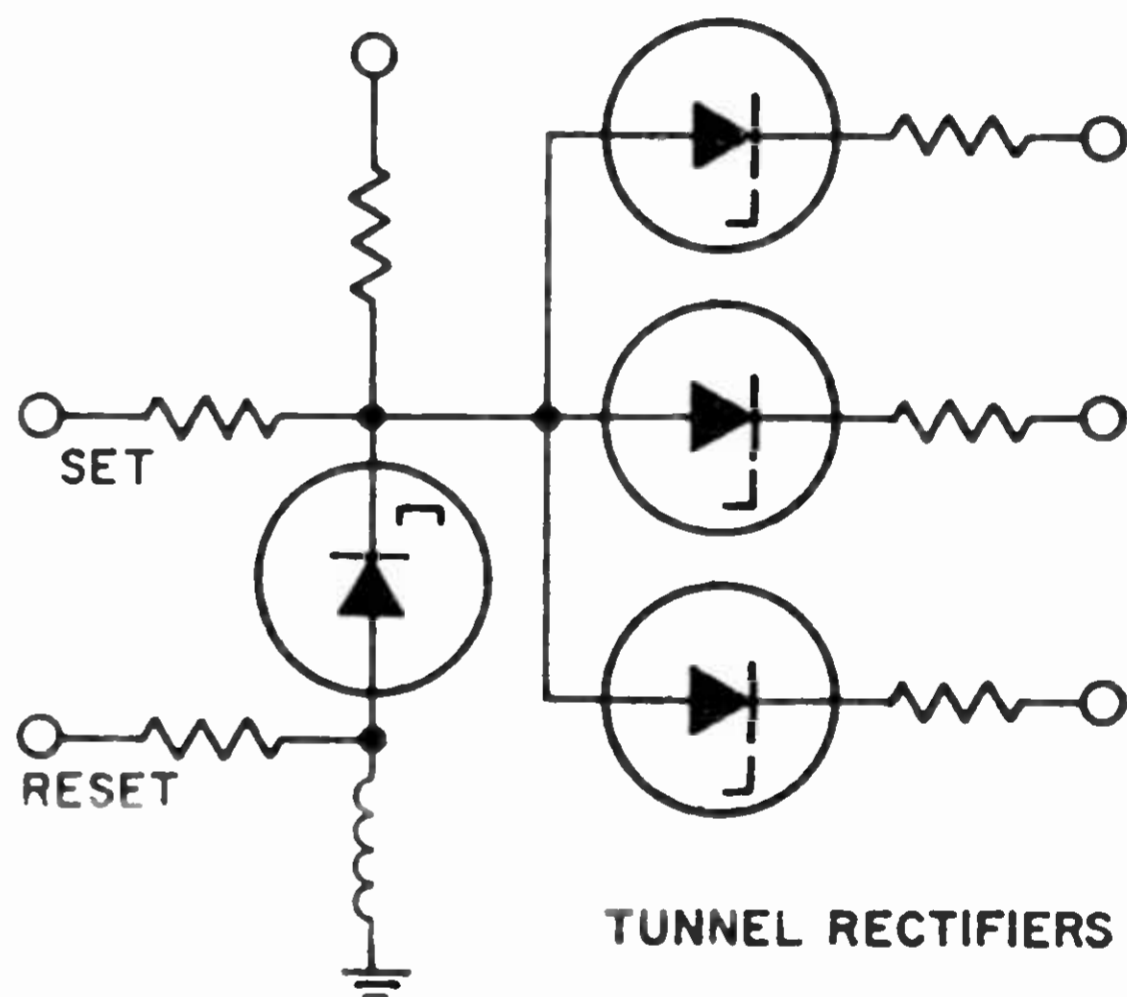


Fig. 100—Logic circuit using a tunnel diode and three tunnel rectifiers.

VARACTOR DIODES

A varactor or variable-reactance diode is a microwave-frequency p-n junction semiconductor device in which the depletion-layer capacitance bears a nonlinear relation to the junction voltage, as shown in Fig. 101(a). When biased in the reverse direction, a varactor diode can be represented by a voltage-sensitive capacitance $C(v)$ in series with a resistance R_s , as shown in Fig. 101(b). This nonlinear capacitance and low series resistance, which permit the device to perform frequency-multiplication, oscillation, and switching functions, result from a very high impurity concentration outside the depletion-layer region and a rela-

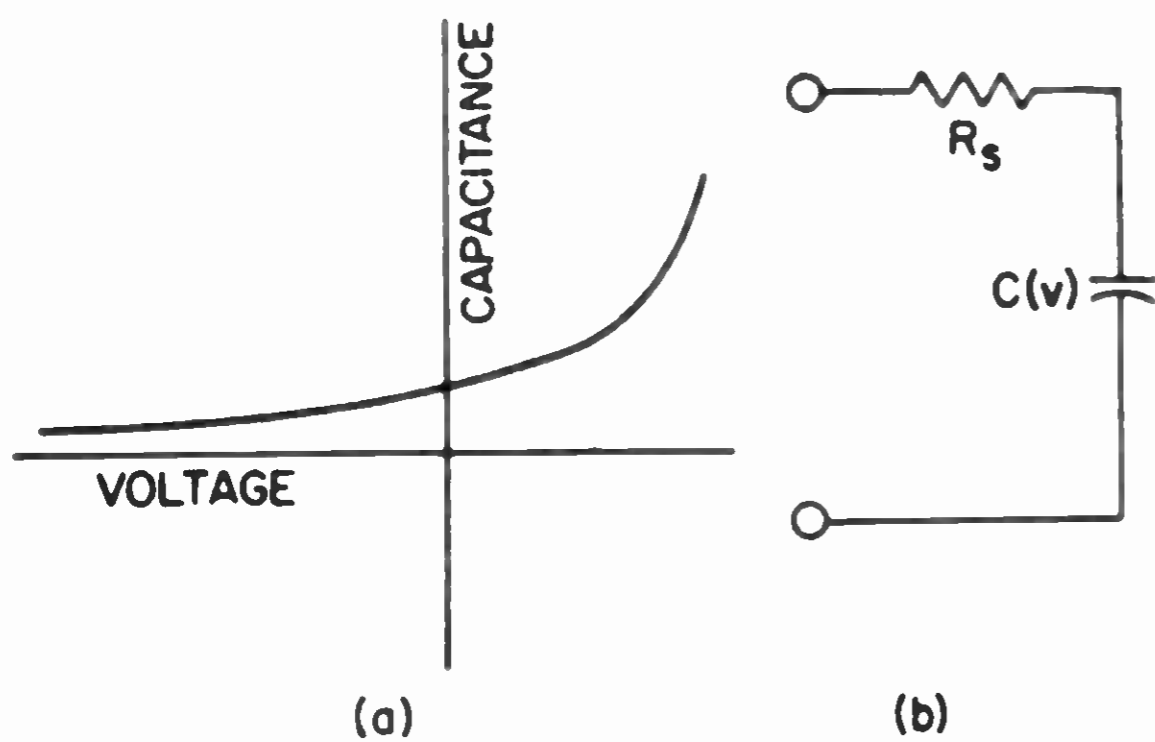


Fig. 101—(a) Capacitance-voltage relation and (b) equivalent circuit for a varactor diode.

tively low concentration at the junction. Very low noise levels are possible in circuits using varactor diodes because the dominant current across the junction is reactive and shot-noise components are absent.

Reactive nonlinearity, without an appreciable series resistance component, enables varactor diodes to generate harmonics with very high efficiency in circuits such as the shunt-type frequency multiplier shown in Fig. 102. The circuit is driven by a sinusoidal voltage source V_s having

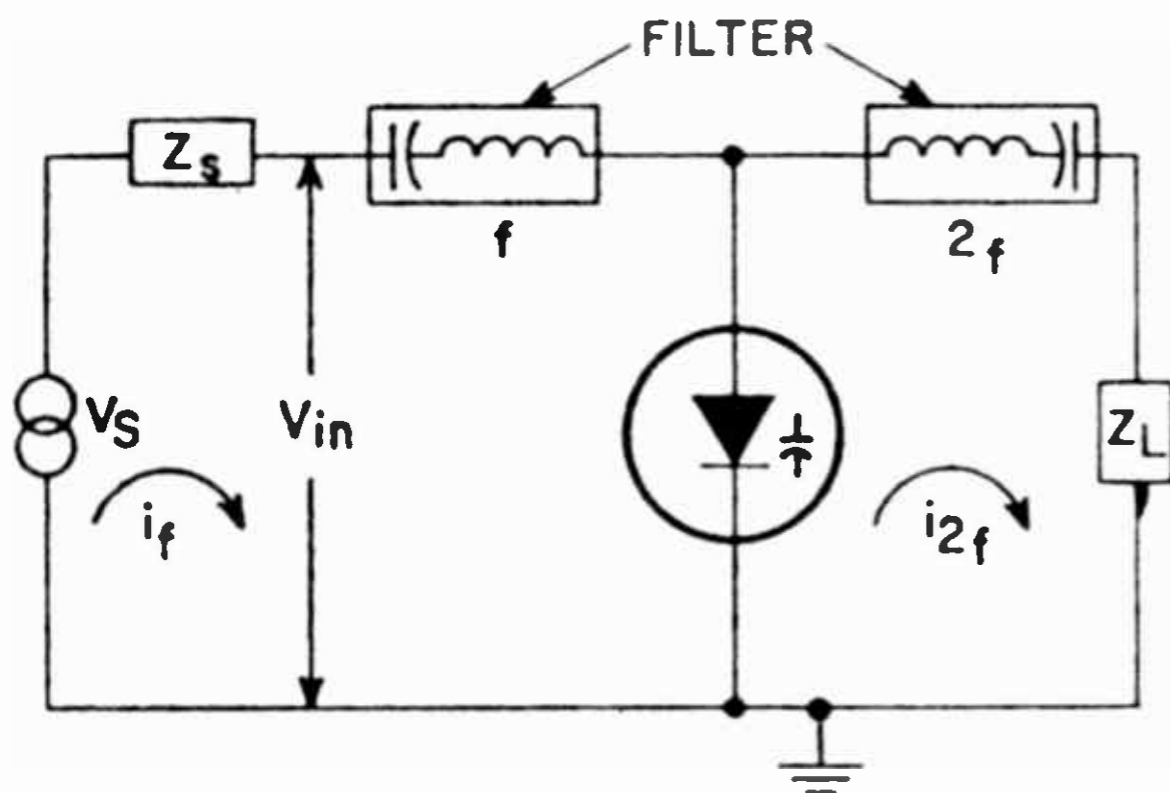


Fig. 102—Varactor-diode frequency multiplier

a fundamental frequency f and an internal impedance Z_s . Because the ideal input filter is an open circuit for all frequencies except the fundamental frequency, only the fundamental component of current i_f can flow in the input loop. A second-harmonic current i_{2f} is generated by the varactor diode and flows toward the load Z_L ; another ideal filter is used in the output loop to block the fundamental-frequency component of the input current.

Varactor diodes can amplify signals when their voltage-dependent capacitance is modulated by an alternating voltage at a different frequency. This alternating voltage supply, which is often referred to as the "pump", adds energy to the signal by changing the diode capacitance in a specific phase relation with the stored signal charge so that potential energy is added to this charge. An "idler" circuit is generally used to provide the proper phase relationship between the signal and the "pump".

VOLTAGE-REFERENCE DIODES

Voltage-reference or zener diodes are silicon rectifiers in which the reverse current remains small until the breakdown voltage is reached and then increases rapidly with little further increase in voltage. The breakdown voltage is a function of the diode material and construction, and can be varied from one volt to several hundred volts for various current and power ratings, depending on the junction area and the method of cooling. A stabilized supply can deliver a constant output (voltage or current) unaffected by temperature, output load, or input voltage, within given limits. The stability provided by voltage-reference diodes makes them useful as stabilizing devices and as reference sources capable of supplying extremely constant current loads.

COMPENSATING DIODES

Excellent stabilization of collector current for variations in both supply voltage and temperature can be obtained by the use of a compensating diode operating in the forward direction in the bias network of amplifier or oscillator circuits. Fig. 103 shows the transfer characteristics of a transistor; Fig. 104 shows the forward characteristics of a compensating diode. In a typical circuit, the diode is biased in the forward direction; the operating point is repre-

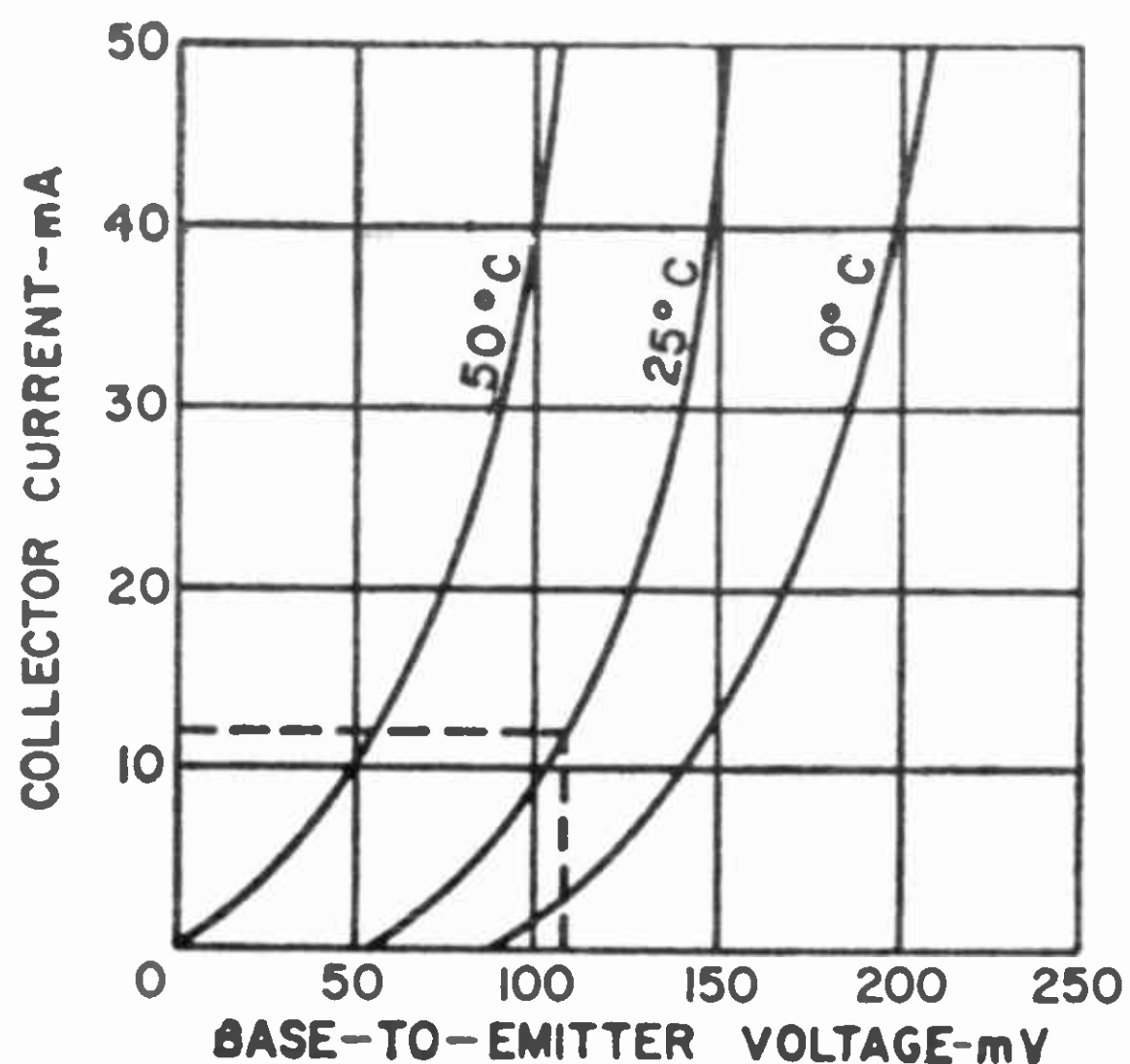
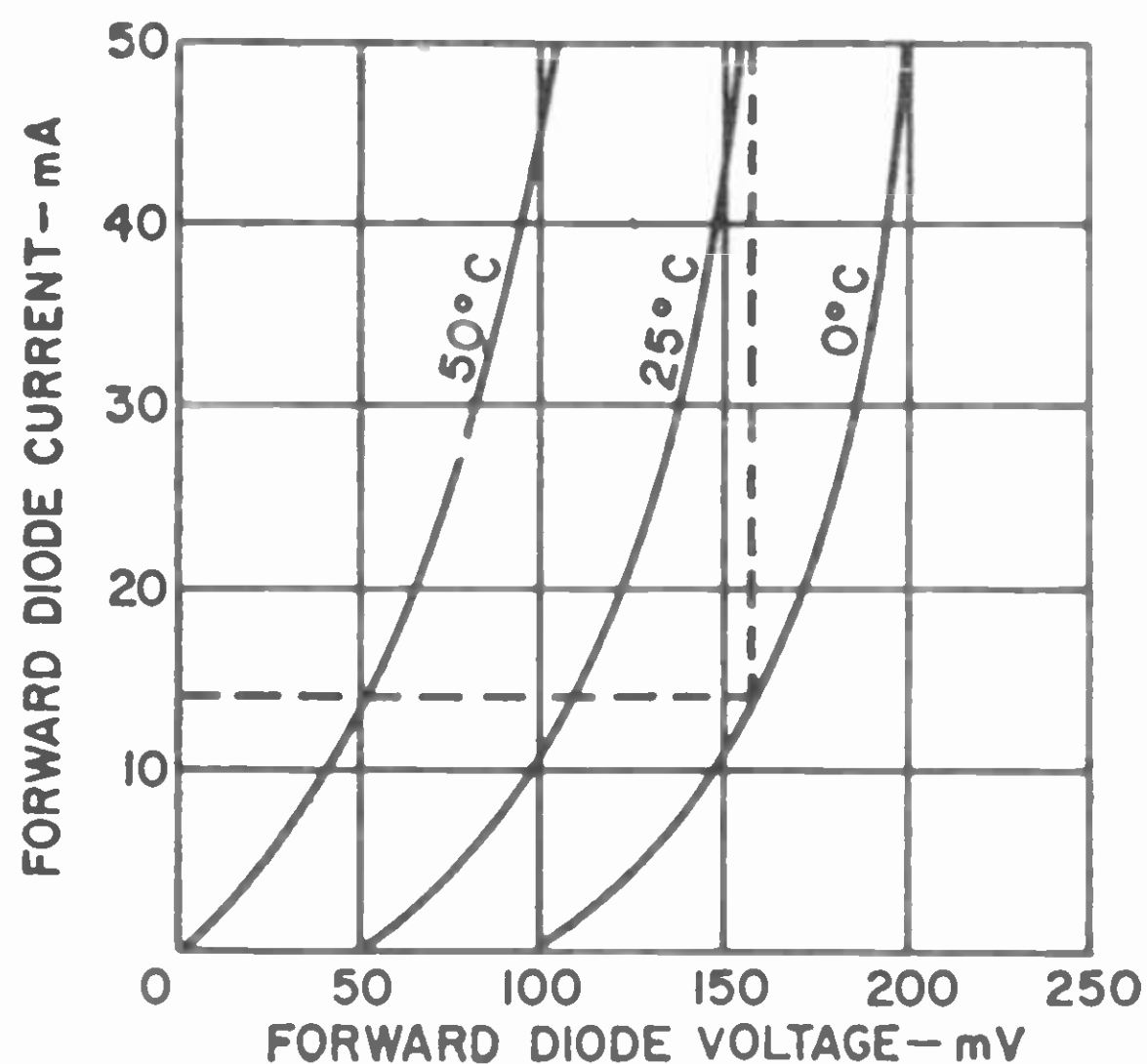


Fig. 103—Transfer characteristics of transistor.

sented on the diode characteristics by the dashed horizontal line. The diode current at this point determines a bias voltage which establishes the transistor idling current. This bias voltage shifts with varying temperature in the same direction and magnitude as the transistor characteristic, and thus provides an idling current that is essentially independent of temperature.

The use of a compensating diode also reduces the variation in transistor idling current as a result of supply-voltage variations. Because the diode current changes in proportion with the supply voltage, the bias voltage to the transistor changes in the same proportion and idling-current changes are minimized. (The



104—Forward characteristics of compensating diode.

use of diode compensation is discussed in more detail under "Biasing" in the section on Bipolar Transistors.

PHOTOCONDUCTIVE CELLS

A photoconductive cell is a diode in which the resistance of the photosensitive material decreases as the intensity of the light striking the material increases. The essential elements of RCA photoconductive cells are shown by the cutaway view in Fig. 105. The photosensitive material, either cadmium sulfide or cadmium-sulfo-selenide, is normally

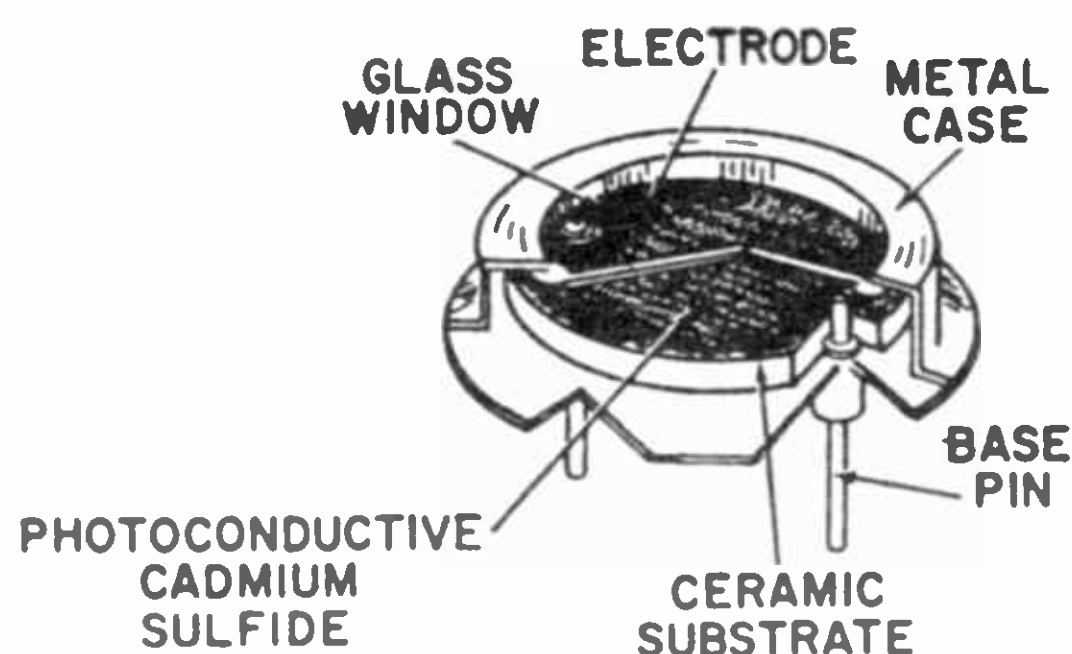


Fig. 105—Cutaway view of a typical photoconductive cell.

deposited in a serpentine pattern on a ceramic substrate and connected at each end by an electrode. After the base pins are attached to the two electrodes, the photosensitive area is protected from moisture by use of a glass window and metal case. In normal operation, the photoconductive cell is connected in series with the supply voltage, and an increase in light flux falling on the cell increases the current of the circuit.

RCA polycrystalline cadmium-sulfide and cadmium-sulfo-selenide photoconductive cells are designed for use in a variety of light-operated control applications. Maximum response for cadmium-sulfide photocells types occurs at approximately 5100 angstroms and for cadmium sulfo-selenide photocells at approximately 6150 angstroms. Typical spectral response characteristics are shown in Fig. 106.

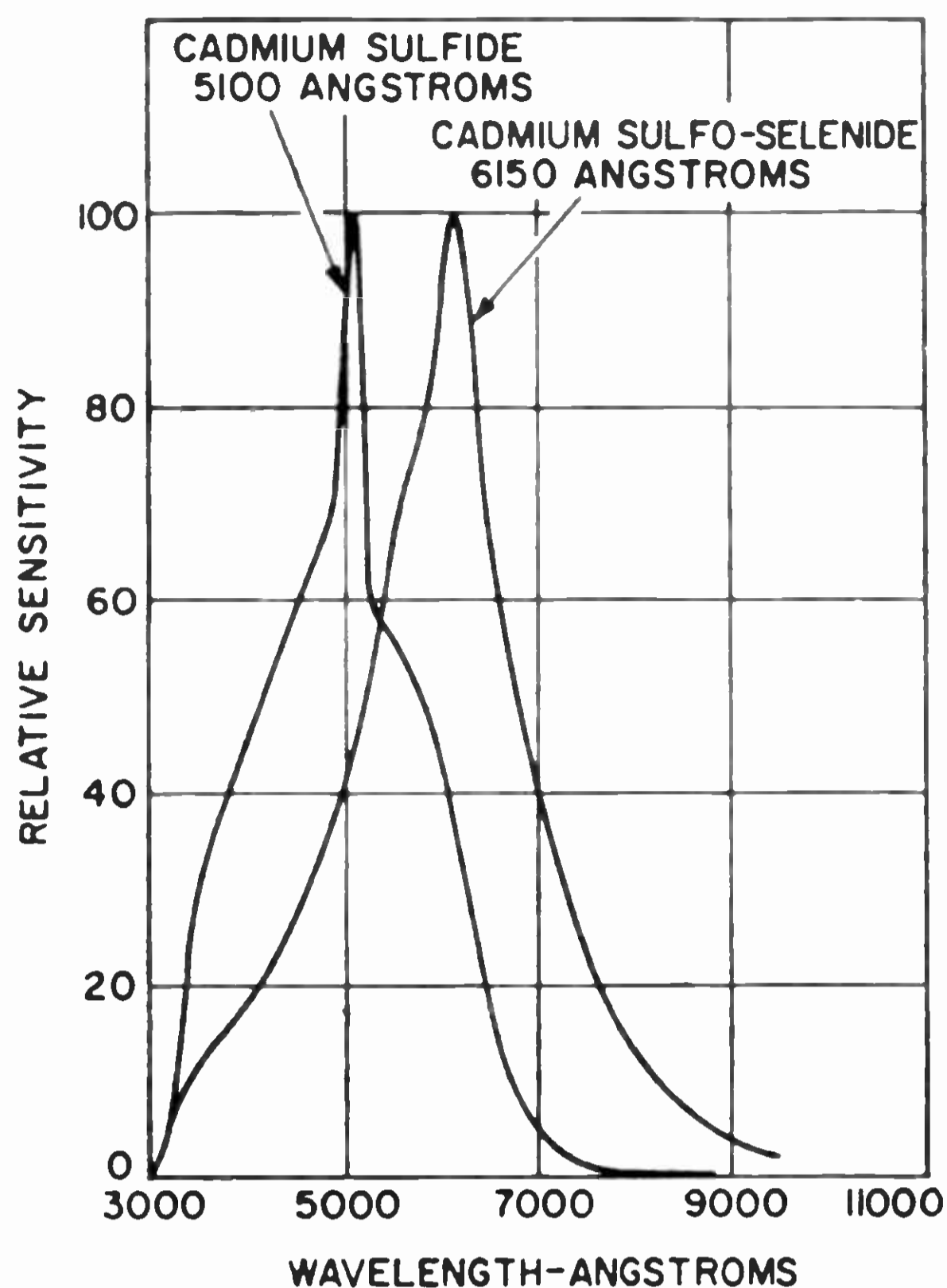


Fig. 106—Typical spectral response characteristics of photoconductive cells.

The 5100-angstrom cadmium-sulfide cells are intended for general-purpose use while the 6150-angstrom cadmium-sulfo-selenide cells are designed for applications in which faster time-response characteristics are required. The 6150-angstrom photocells are about three times faster than their 5100-angstrom counterparts.

Electrical Characteristics

One of the most important characteristics of the photocell is its resistance as a function of illumination. Fig. 107 shows this relationship for a number of RCA photocells. The slopes of these curves vary slowly as a function of illumination and are nearly constant. The dc cell resistance R measured across the terminals may be expressed as follows:

$$R = R_1 L - \gamma$$

where R_1 is the resistance of the cell per unit illumination, L is the illumination in footcandles, and γ is

the slope of the characteristic at a given operating point. The performance of the photocell at a given operating point is defined by specifying R_1 and γ .

For a typical cell, RCA-7163, R_1 and γ are 0.03×10^6 ohms and 0.83, respectively, at an illumination of 1 footcandle. The resistance, or conductance, of the cell is often indirectly expressed in terms of the current drawn through the cell at a given voltage and given light level. When a dc voltage is applied across the cell, the resistance for a given illumination may be computed by means of Ohm's Law. The conductance (1/resistance) of the photoconductive cell does not change rapidly with change in incident illumination, but requires some time to reach its steady-state value.

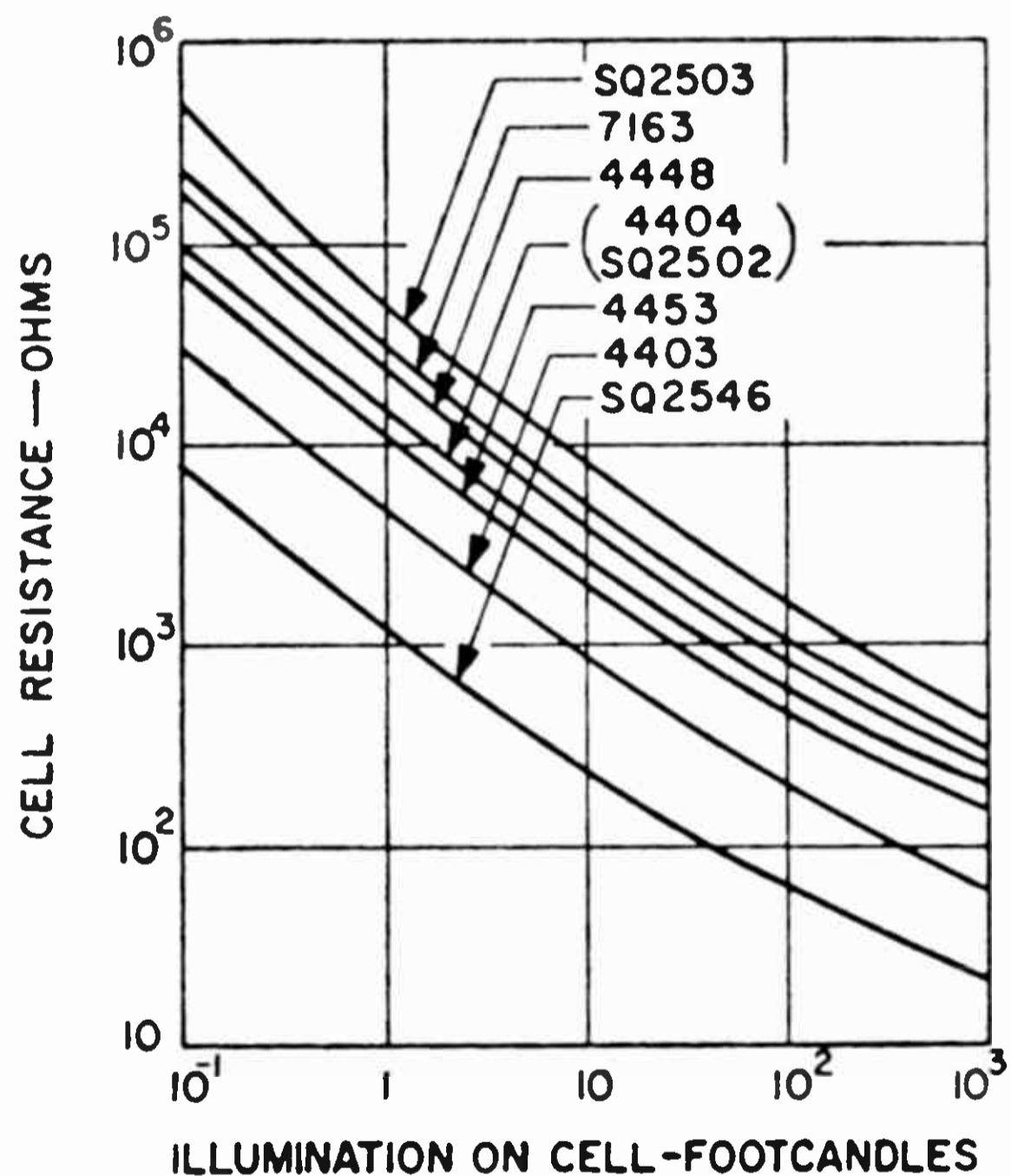


Fig. 107—Effect of illumination on resistance of RCA photocells.

Although the build-up and decay of conductance and current upon the application or removal of illumination is only approximately exponential, the term "time constant" is frequently used to describe the time required for conductance or current to reach 63.2 per cent (rise) or 36.8 per cent (decay) of its maximum value. The rise time constant depends on the previous dark storage of the cell and on the intensity of

the applied illumination. In general, the cell responds more quickly to high illumination levels than to low illumination levels and its rise time is usually longer than its decay time. Typical photocurrent rise curves are shown in Fig. 108.

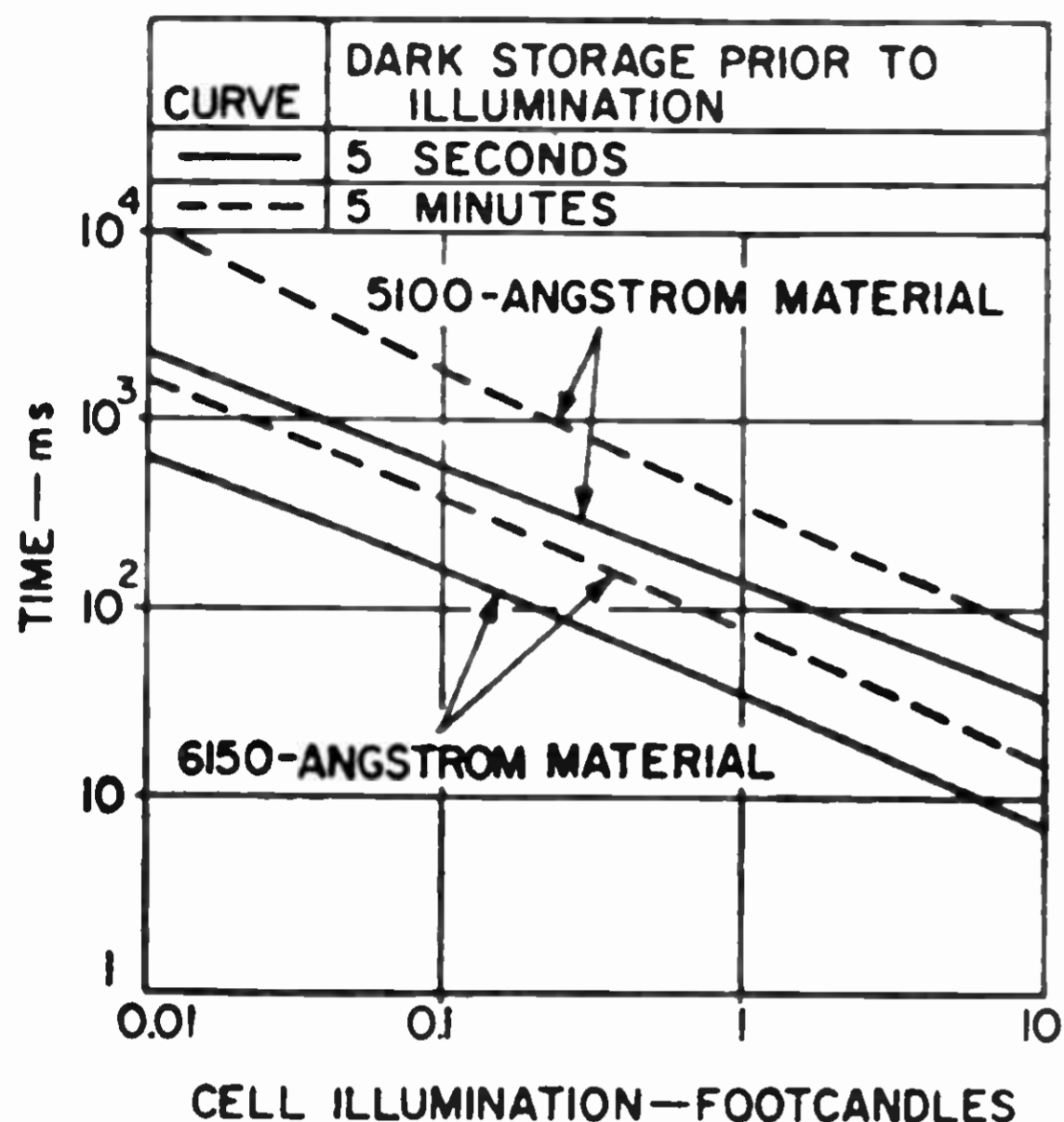


Fig. 108—Typical photocurrent rise characteristics.

In addition to these time effects, there are other time-associated phenomena that take place more slowly. The phenomena can best be described by saying that the cell has some memory of previous light exposure. Long exposure to high light levels tends to make the cell slightly less sensitive and somewhat faster in response whether or not voltage is applied to the cell during exposure. These changes are reversible, and the cell will return to its former condition after a storage period in the dark.

Because of the "memory" of the photocell, it is desirable to "light-precondition" a cell before a measurement of photocurrent is made. A commonly used preconditioning schedule employed in production testing is the exposure of the cell for 16 to 24 hours to daylight fluorescent light of 500 footcandles. Voltage is not applied to the cell during the preconditioning schedule.

Time effects are also related to the application of voltage. For ex-

ample, a cell is slightly less sensitive under ac voltage operation than under dc voltage operation.

In most photocell applications, it is important that the conductance of the cell be substantially less when the cell is in the dark than when it is illuminated. The terms **dark current** and **decay current** are used to describe cell performance under unilluminated conditions. Dark current is that current which passes through the cell under specified conditions of voltage and temperature after the cell has been in the dark for a long period of time. Dark current usually has a very low value. Because of the time effects, it is more convenient to specify the decay current which is observed at a given time interval following the removal of a given level of illumination. For the 7163, at an applied voltage of 50 volts, decay current is below 40 microamperes 10 seconds after the removal of 1 footcandle of illumination. Photocurrent decay curves are shown in Fig. 109.

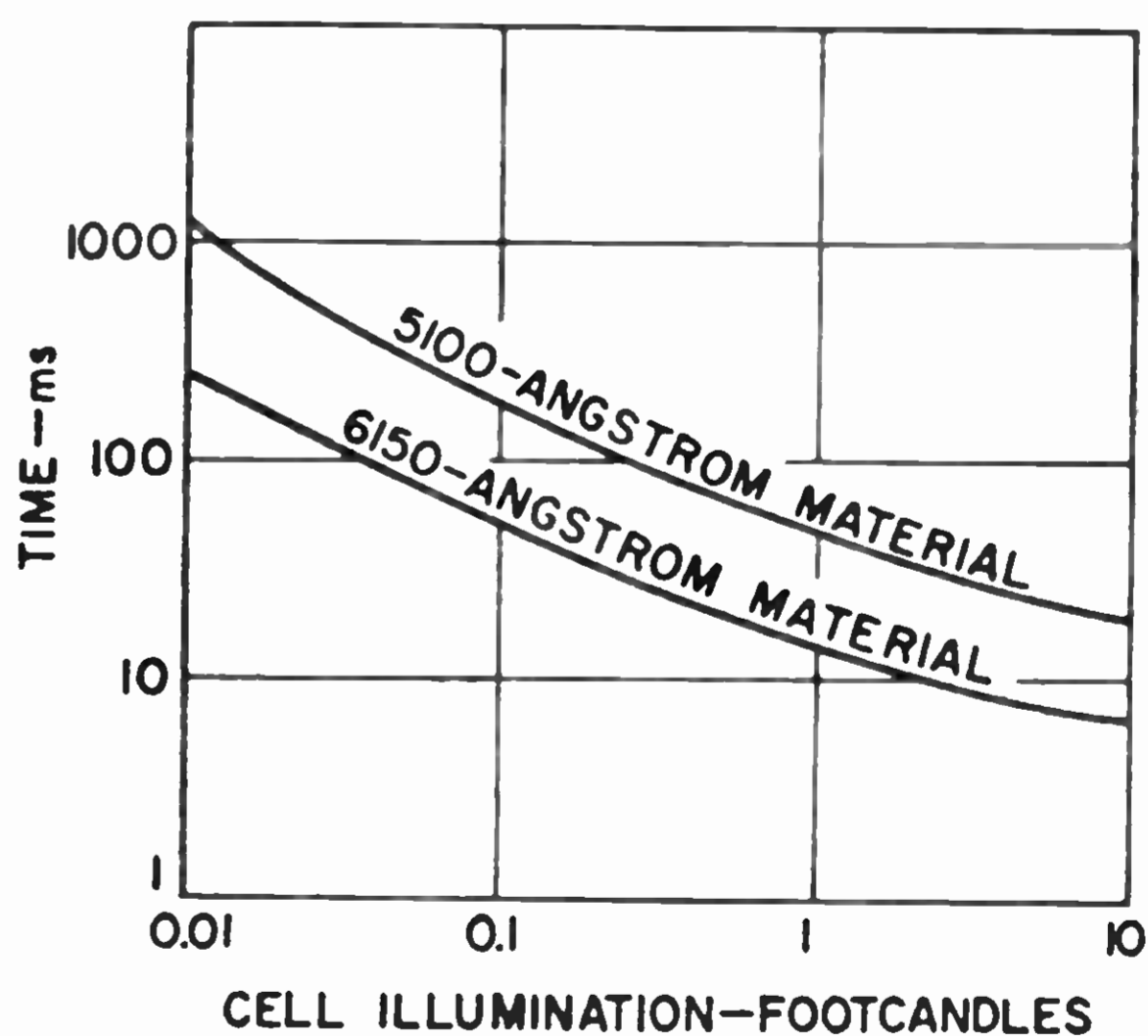


Fig. 109—Typical photocurrent decay characteristics

Peak-to-valley response as a function of square-wave light input for typical cells is shown in Fig. 110. As expected, the frequency response is higher for higher levels of illumination.

The effect of ambient temperature on photocell sensitivity is shown in Fig. 111 for 5100-angstrom material

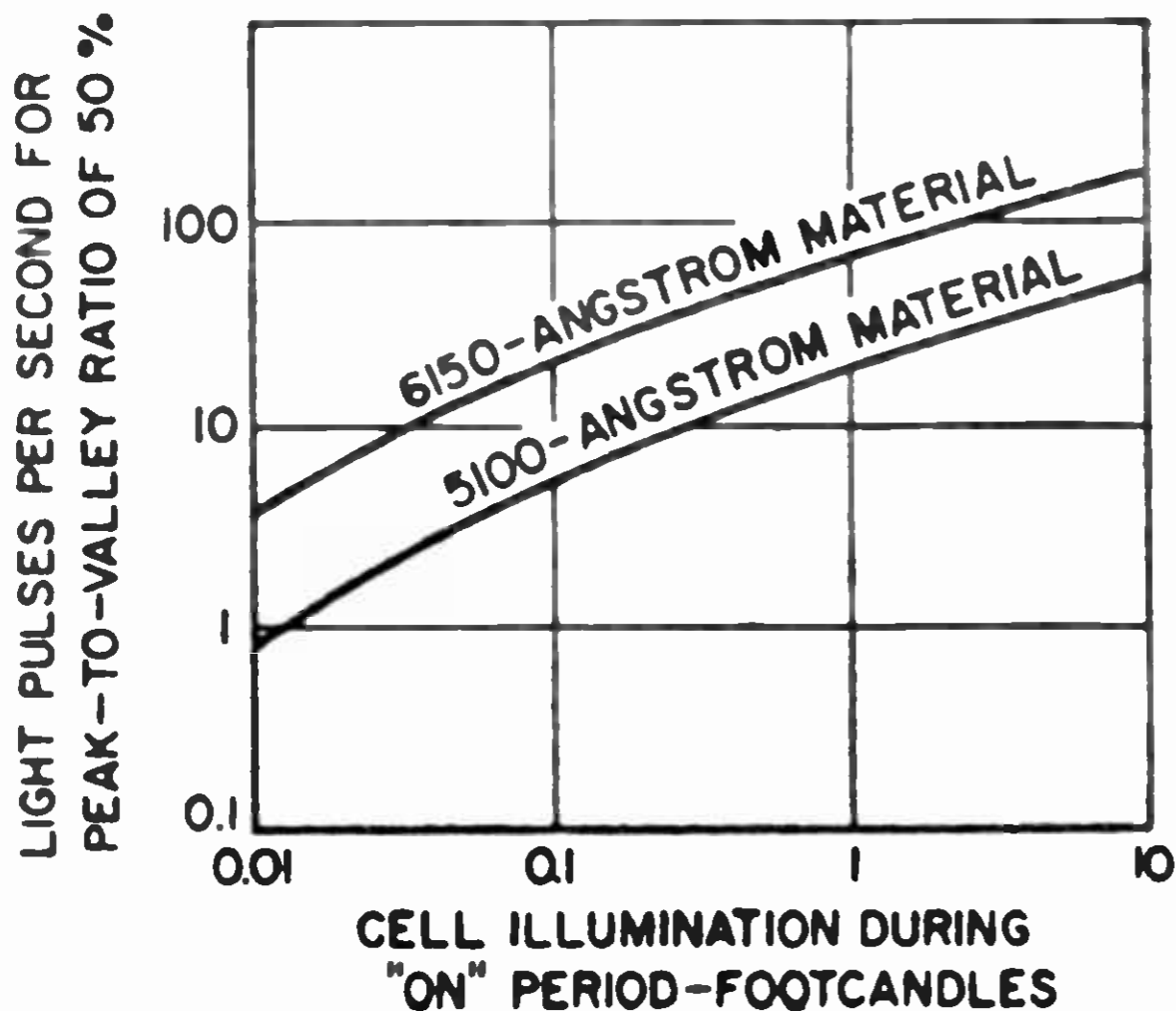


Fig. 110—Typical response characteristics to pulsed light.

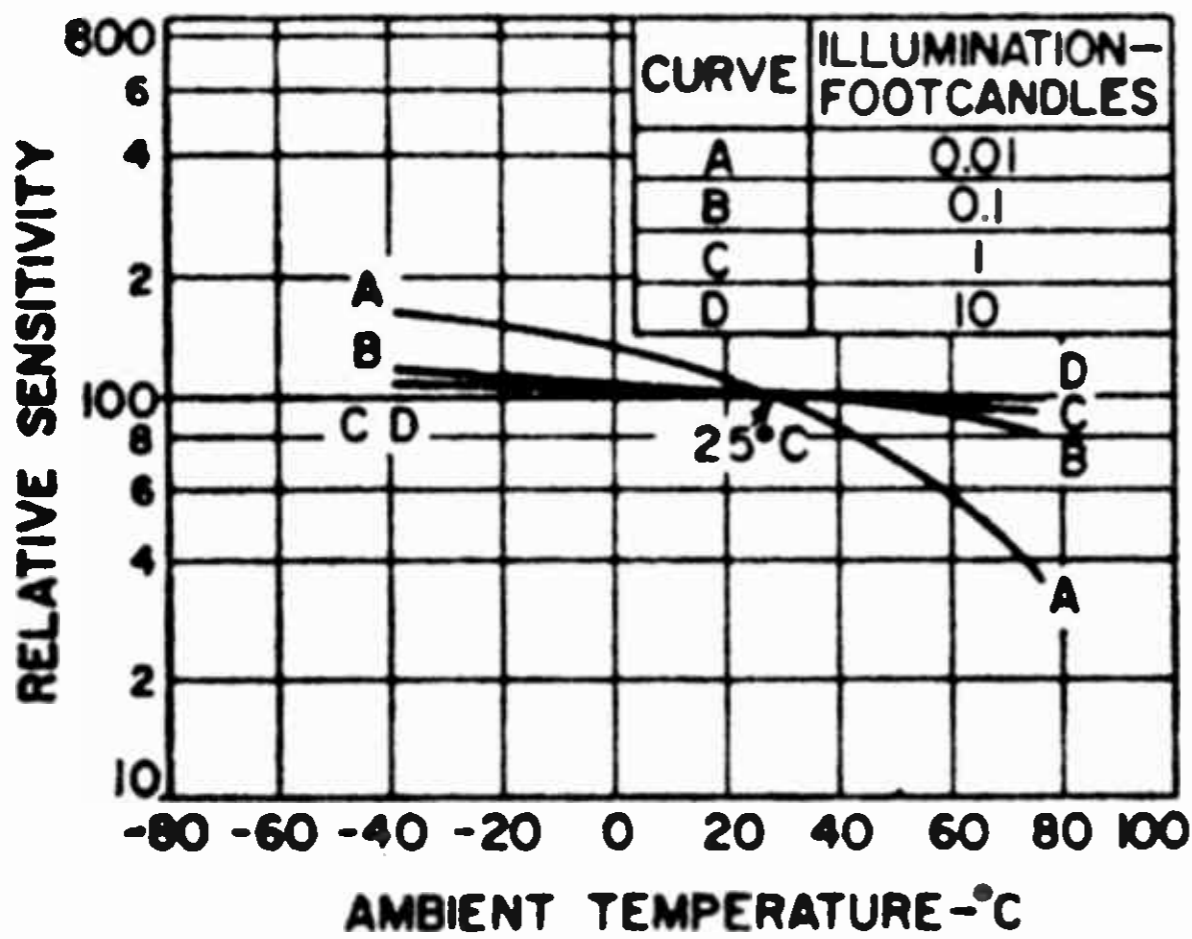


Fig. 111—Typical temperature characteristics of 5100-angstrom photocells.

and in Fig. 112 for 6150-angstrom material.

Power dissipated within the sensitive surface causes a rise in photocell temperature. This rise in

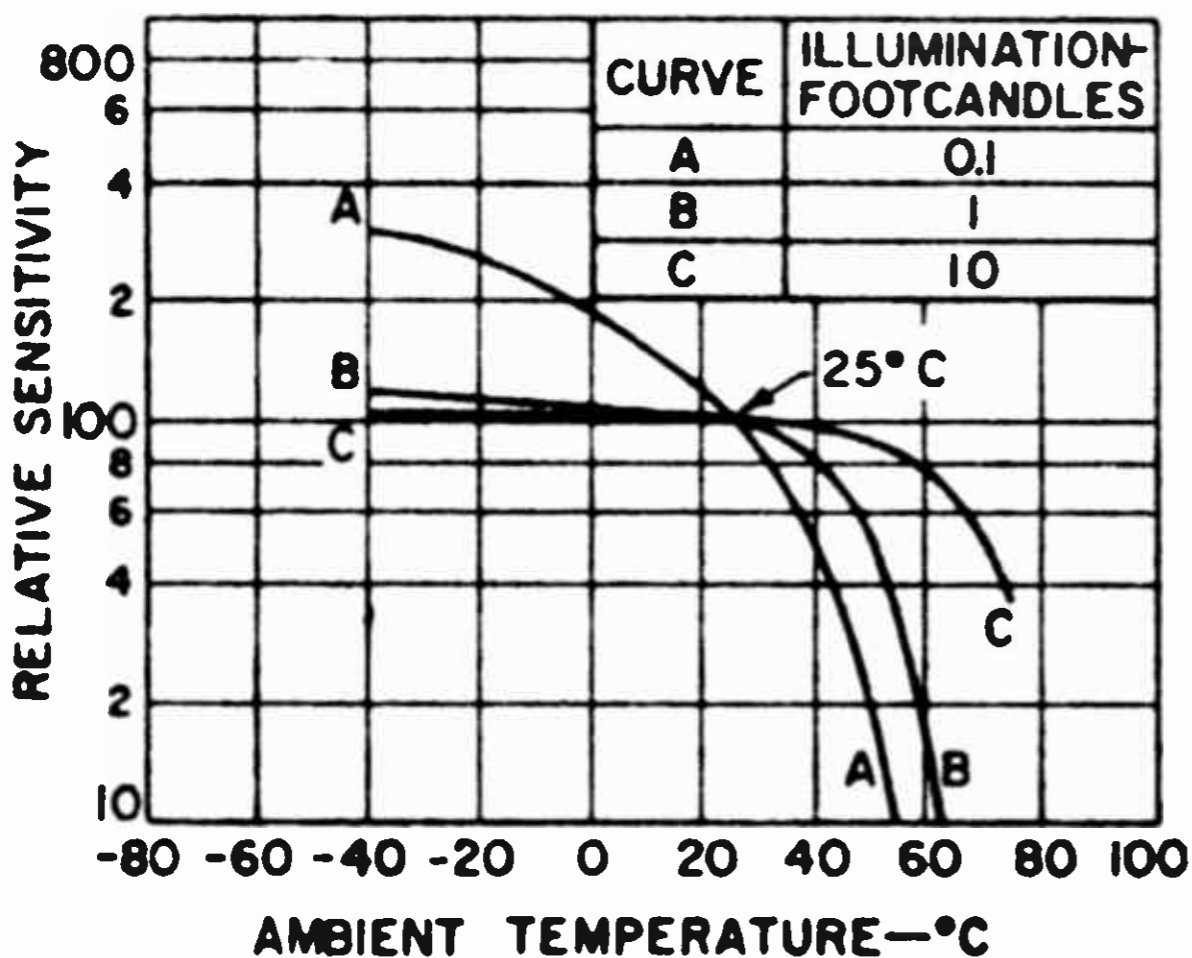


Fig. 112—Typical temperature characteristics of 6150-angstrom photocells.

temperature can be reduced by the use of heat sinks. Table II lists typical case-to-ambient thermal resistance values for the different RCA photocell packages.

Table II—Photocell Thermal-Resistance Values (Case-to-Ambient)

Case	Thermal Resistance °C/W
1"-Diameter	38
Modified TO—8	95
Modified TO—5	170
Modified TO—18	250

LIGHT-EMITTING DIODES

Most p-n junction devices emit some form of radiation when under forward bias; however, the efficiency or ratio of light-energy output to electrical-energy input is usually low, and the radiation is not easily detected. A light-emitting diode is a p-n junction device which is specifically designed to emit radiation in a particular portion of the spectrum when a forward voltage is applied across its p-n junction. The radiation occurs as a result of hole-electron recombination at the junction and within the narrow space-charge region around the junction. Majority carriers combine across the junction, and minority carriers combine with majority carriers within the space-charge region. The wavelength of emitted radiation depends on the energy gap of the substrate material and the energy levels of the impurity dopants.

Fig. 113 shows various crystal materials and the portion of the spectrum in which they emit radiation. Table III lists these materials and indicates those which also provide laser action. With the exception of SiC, the materials fall into three groups: the III-V group and the II-VI group of the periodic table and lead salts. The lead salts emit radiation toward the far-infrared portion of the spectrum, while the

III-V and II-VI groups cover the near-infrared and visible portions of the spectrum. The latter two groups exhibit considerable overlap. Generally, any one diode emits one strong line that has a width in the

order of 300 angstroms. Continuous coverage of the spectrum from the blue to the near-infrared region can be obtained by use of mixed crystals. For example, gallium arsenide phosphide [Ga (As_{1-x} P_x)] emits radiation from the green through infrared (5600 to 9000 angstroms) by variation of the ratio of gallium phosphide to gallium arsenide in the p- and n-type layers. The higher the content of gallium phosphide, the shorter the wavelength. With a 45-per-cent content of gallium phosphide, the peak emission occurs in the red region at 6400 angstroms.

Applications for p-n junction light emitters range from electroluminescent displays to such electronic functions as card reading, character recognition, sensing, electro-optical switching, optical ranging, illumination, metrology, communication, intrusion alarms, control circuits, and warning devices. The non-laser diode appears to have a substantial advantage over the laser in present-day devices for display applications; however, the laser diode has distinct advantages for electronic-function applications.

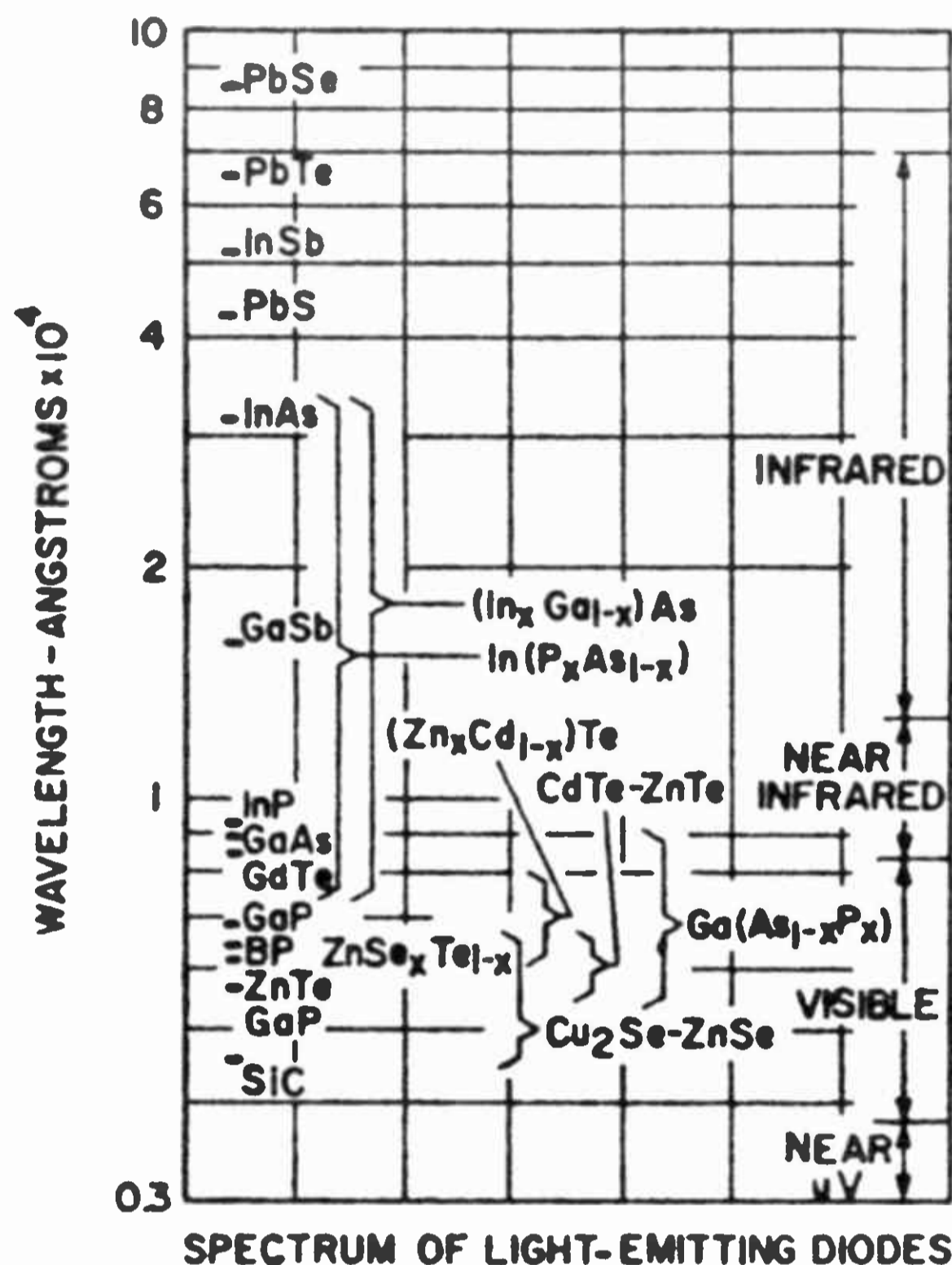


Fig. 113—Chart showing portion of spectrum in which various crystal materials emit radiation.

Table III—Materials for p-n Junction Light-Emitting Diodes

Crystal	Macrometers	Laser Action	Remarks
PbSe	8.5	Yes	direct
PbTe	6.5	Yes	direct
InSb	5.2	Yes	direct
PbS	4.3	Yes	direct
InAs	3.15	Yes	direct
(In _x Ga _{1-x}) As	0.85-3.15	Yes	direct
In (P _x As _{1-x})	0.91-3.15	Yes	direct
GaSb	1.6	No	
InP	0.91	Yes	direct
GaAs	0.90	Yes	direct
Ga (As _{1-x} P _x)	0.55-0.90	Yes	direct
CdTe	0.855	No	homojunction
(Zn _x Cd _{1-x}) Te	0.59-0.83	No	homojunction
CdTe-ZnTe	0.56-0.66	No	heterojunction
BP	0.64	No	indirect
Cu ₂ Se-ZnSe	0.40-0.63	No	heterojunction
Zn (Se _x Te _{1-x})	0.627	No	homojunction
ZnTe	0.62	No	barrier
Ga P	0.565	No	indirect-band gap
	0.68	No	indirect-oxygen line
Si C	0.456	?	-SiC homojunction

Linear System Applications

THIS section discusses the use of semiconductor devices in linear applications, i.e., applications in which the output quantity of a circuit or a portion of a circuit is directly proportional to an input quantity so that a graph representing the relationship of the two quantities is a straight line. Linear applications include communications receivers and transmitters, FM tuners, and TV and hi-fi equipment.

When speech, music, or video information is transmitted from a radio or television station, the station radiates a modulated radio-frequency (rf) carrier. The function of a radio or television receiver is simply to reproduce the modulating wave from the modulated carrier.

As shown in Fig. 114, a superheterodyne radio receiver picks up the transmitted modulated rf signal, amplifies it and converts it to a modulated intermediate-frequency (if) signal, amplifies the modulated if signal, separates the modulating signal from the basic carrier wave, and amplifies the resulting audio signal to a level sufficient to produce the desired volume in a speaker. In addition, the receiver usually includes some means of producing automatic gain control (agc) of the modulated

signal before the audio information is separated from the carrier.

The transmitted rf signal picked up by the radio receiver may contain either amplitude modulation (AM) or frequency modulation (FM). (These modulation techniques are described later under the heading **Detection**.) In either case, amplification prior to the detector stage is performed by tuned amplifier circuits designed for the proper frequency and bandwidth. Frequency conversion is performed by mixer and oscillator circuits or by a single converter stage which performs both mixer and oscillator functions. Separation of the modulating signal is normally accomplished by one or more diodes in a detector or discriminator circuit. Amplification of the audio signal is then performed by one or more audio amplifier stages.

Audio-amplifier systems for phonograph or tape recorders are similar to the stages after detection in a radio receiver. The input to the amplifier is a low-power-level audio signal from the phonograph or magnetic-tape pickup head. This signal is usually amplified through a pre-amplifier stage, one or more low-level (pre-driver or driver) audio stages,

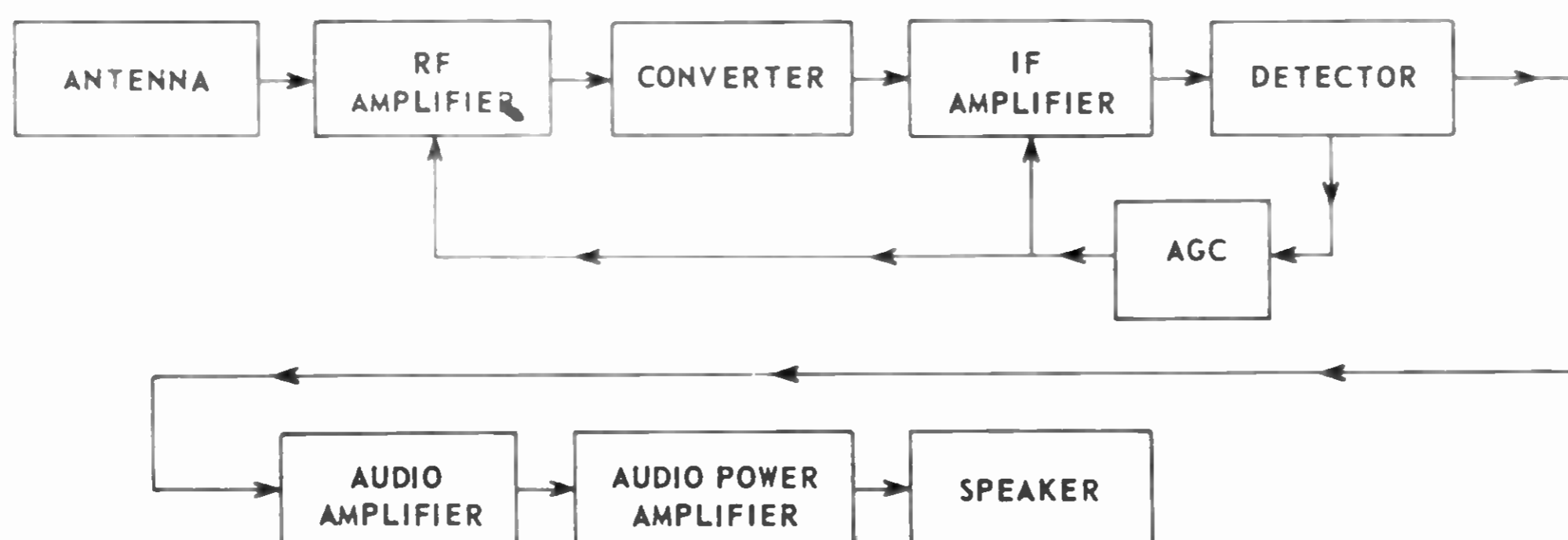


Fig. 114—Simplified block diagram for a broadcast-band receiver.

and an audio power amplifier. The system may also include frequency-selective circuits which act as equalization networks and/or tone controls. Audio amplifiers are discussed in greater detail in a later part of this section.

The operation of a television receiver (shown in block-diagram form in Fig. 115) is more complex than that of a radio receiver, as shown by a comparison of Figs. 114 and 115.

The tuner section of the television receiver selects the proper rf signals for the desired channel frequency, amplifies them, and converts them to a lower intermediate frequency. As in a radio receiver, these functions are accomplished in rf-amplifier, mixer, and local-oscillator stages. The if signal is then amplified in if-amplifier stages which provide the additional gain required to bring the signal level to an amplitude suitable for detection.

After if amplification, the detected signal is separated into sound and picture information. The sound signal is amplified and processed to provide an audio signal which is fed to an audio amplifier system similar to those described above. The picture (video) signal is passed through a

video amplifier stage which conveys beam-intensity information to the television picture tube and thus controls instantaneous "spot" brightness. At the same time, deflection circuits cause the electron beam of the picture tube to move the "spot" across the faceplate horizontally and vertically. Special "sync" signals derived from the video signal assure that the horizontal and vertical scanning are timed so that the picture produced on the receiver exactly duplicates the picture being viewed by the camera or pickup tube.

In a television receiver, the video signal contains a dc component, and therefore the average carrier level varies with signal information. As a result, the agc circuit is designed to provide a control voltage proportional to the peak modulated carrier level rather than the average modulated carrier level. The time constant of the agc detector circuit is made large enough so that the picture content of the composite video signal does not influence the magnitude of the agc voltage. In addition, an electronic switch is often included in the circuit so that it can be operated only during the retrace portion of the scanning cycle. This "gated agc" technique prevents noise peaks from affecting agc operation.

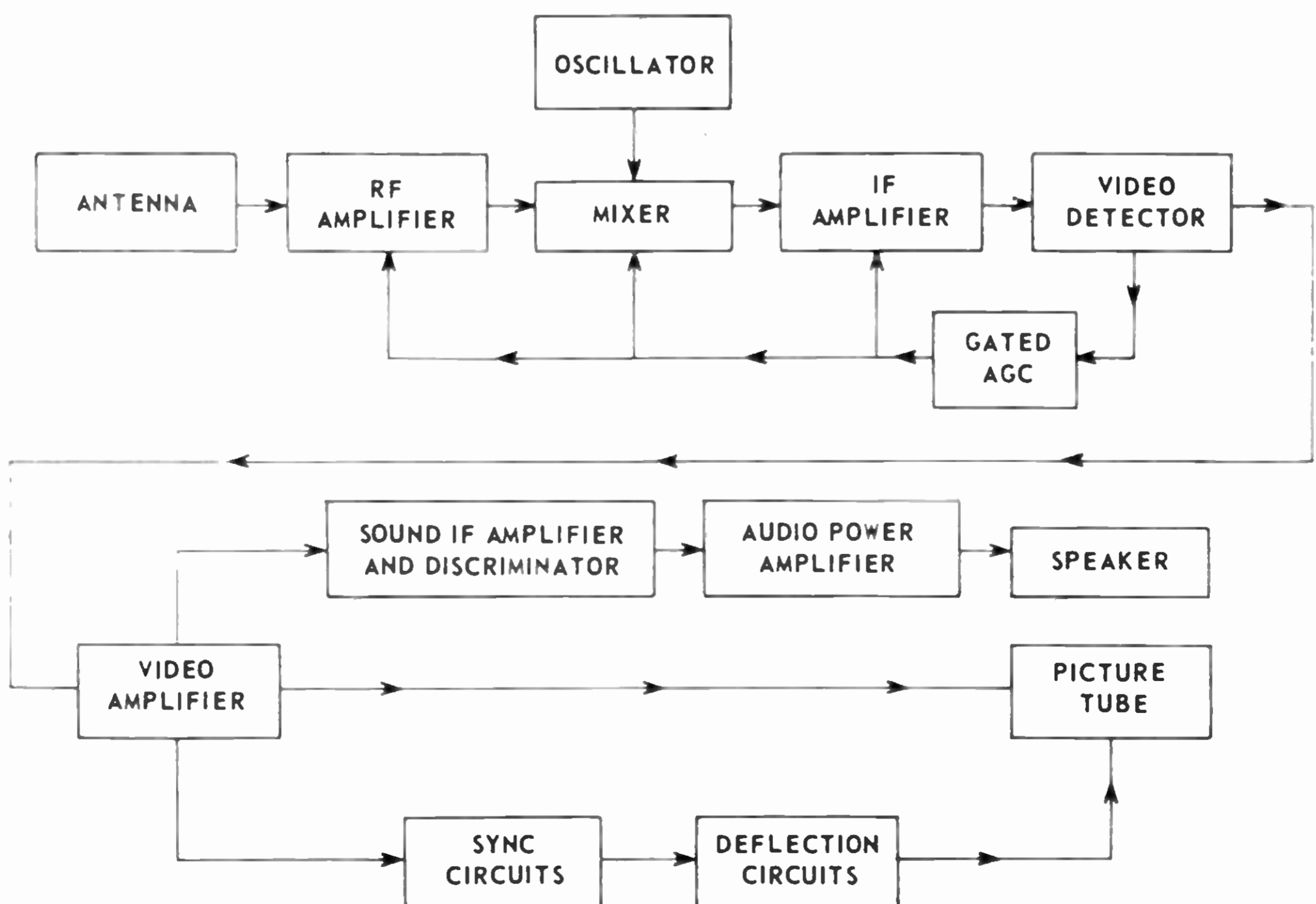


Fig. 115—Simplified block diagram for a television receiver.

DETECTION

The circuit of a radio, television, or communications receiver in which the modulation is separated from the carrier is called the demodulator or detector stage. Transmitted rf signals may be modulated in either of two ways. If the frequency of the carrier remains constant and its amplitude is varied, the carrier is called an amplitude-modulated (AM) signal. If the amplitude remains essentially constant and the frequency is varied, the carrier is called a frequency-modulated (FM) signal.

The effect of **amplitude modulation (AM)** on an rf carrier wave is shown in Fig. 116. The audio-

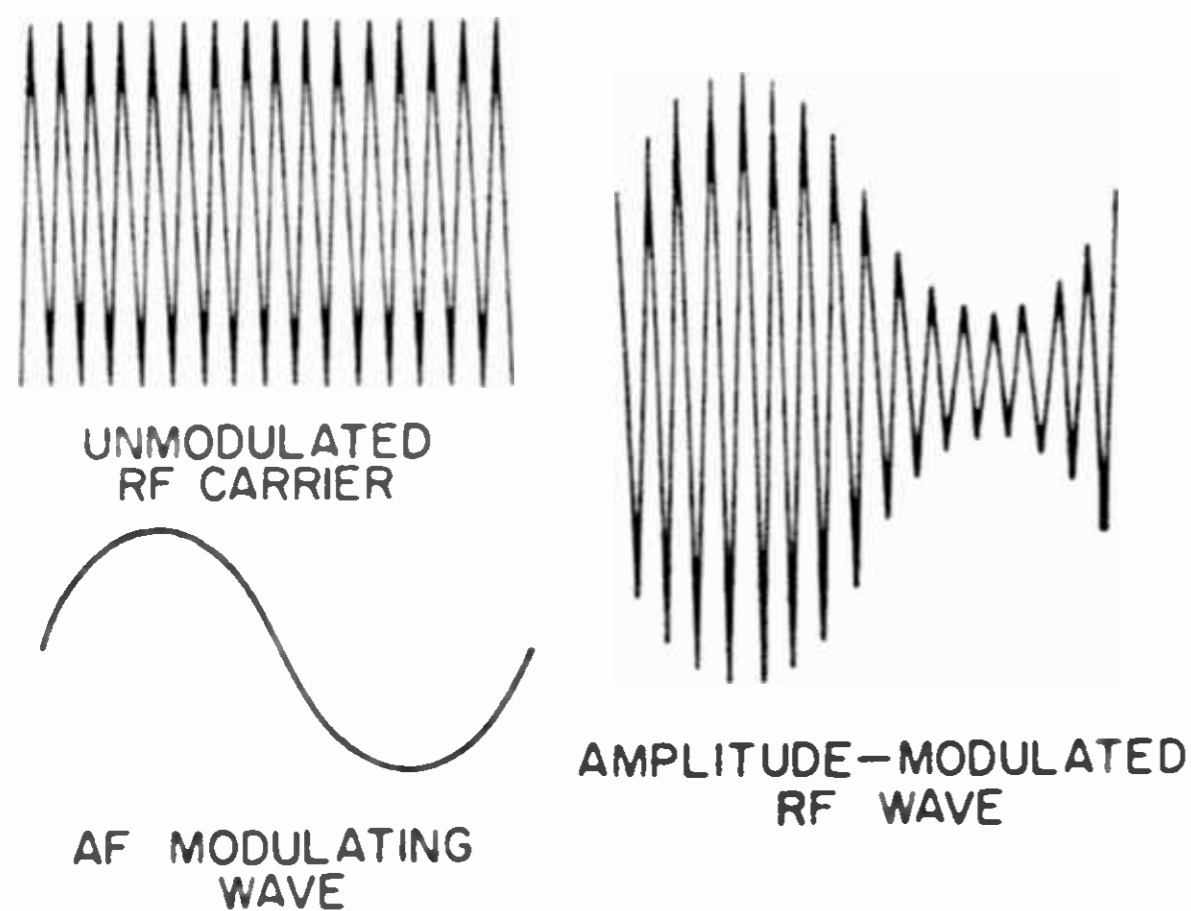


Fig. 116—Waveforms showing effect of amplitude modulation on an rf wave.

frequency (af) modulation can be extracted from the amplitude-modulated carrier by means of a simple **diode detector** circuit such as that shown in Fig. 117. This circuit eliminates alternate half-cycles of the

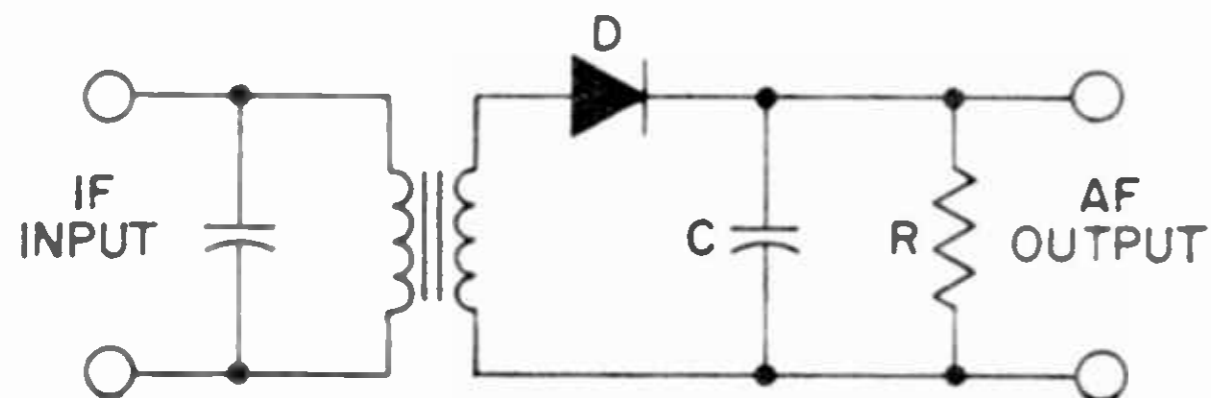
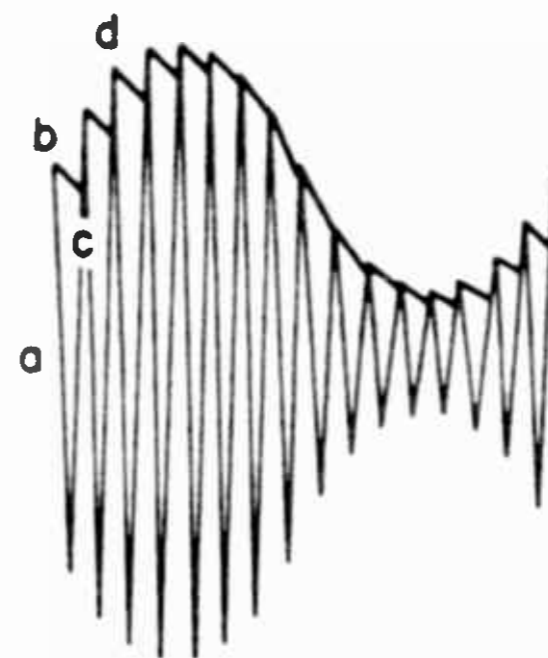


Fig. 117—Basic diode detector circuit.

waveform, and detects the peaks of the remaining half-cycles to produce the output voltage shown in Fig. 118. In this figure, the rf voltage applied to the circuit is shown in light line; the output voltage across the capacitor C is shown in heavy line.

Between points (a) and (b) of



AMPLITUDE-MODULATED
RF WAVE

Fig. 118—Waveform showing modulated rf input (light line) and output voltage (heavy line) of diode-detector circuit of Fig. 117.

Fig. 118, capacitor C charges up to the peak value of the rf voltage. Then, as the applied rf voltage falls away from its peak value, the capacitor holds the cathode of the diode at a potential more positive than the voltage applied to the anode. The capacitor thus temporarily cuts off current through the diode. While the diode current is cut off, the capacitor discharges from (b) to (c) through the diode load resistor R.

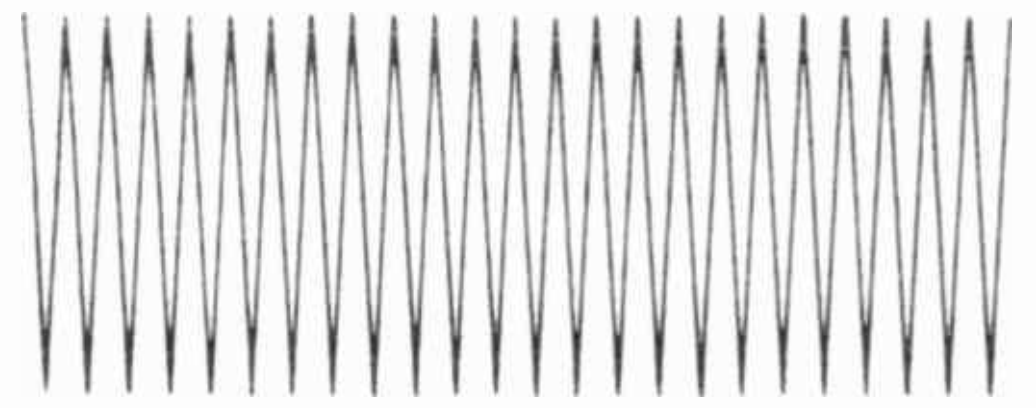
When the rf voltage on the anode rises high enough to exceed the potential at which the capacitor holds the cathode, current flows again and the capacitor charges up to the peak value of the second positive half-cycle at (d). In this way, the voltage across the capacitor follows the peak value of the applied rf voltage and reproduces the af modulating signal. The jaggedness of the curve in Fig. 118, which represents an rf component in the voltage across the capacitor, is exaggerated in the drawing. In an actual circuit, the rf component of the voltage across the capacitor is small. When the voltage across the capacitor is amplified, the output of the amplifier reproduces the speech or music that originated at the transmitting station.

Another way to describe the action of a diode detector is to consider the circuit as a half-wave rectifier. When the signal on the anode swings positive, the diode conducts and the rectified current flows. The dc voltage across the capacitor C varies in ac-

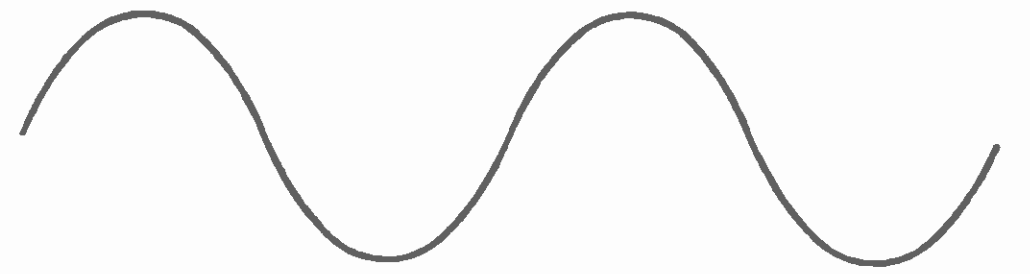
cordance with the rectified amplitude of the carrier and thus reproduces the af signal. Capacitor C should be large enough to smooth out rf or if variations, but should not be so large as to affect the audio variations. (Although two diodes can be connected in a circuit similar to a full-wave rectifier to produce full-wave detection, in practice the advantages of this connection generally do not justify the extra circuit cost and complication.)

In the circuit shown in Fig. 117, it is often desirable to forward-bias the diode almost to the point of conduction to improve performance for weak signal levels. It is also desirable that the resistance of the ac load which follows the detector be considerably larger than the diode load resistor to avoid severe distortion of the audio waveform at high modulation levels.

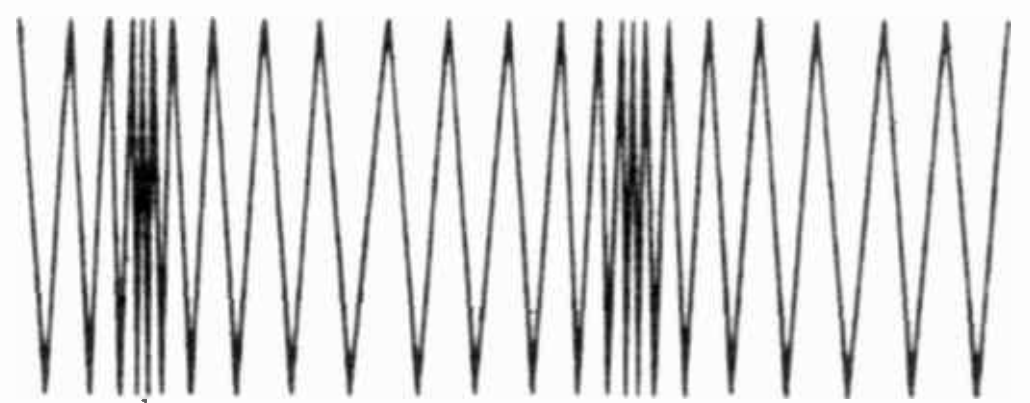
The effect of frequency modulation (FM) on the waveform of an rf carrier wave is shown in Fig. 119. In this type of transmission, the frequency of the rf carrier deviates from the mean value at a rate proportional to the audio-frequency modulation and by an amount (determined in the transmitter) proportional to the amplitude of the af modulating signal. That is, the number of times the carrier frequency deviates above and below the center frequency is a measure of the frequency of the modulating signal; the amount of frequency deviation from the center frequency is a measure of the loudness (amplitude) of the modulating signal. For



UNMODULATED RF CARRIER



AF MODULATING WAVE



FREQUENCY-MODULATED RF WAVE

Fig. 119—Waveforms showing effect of frequency modulation on an rf wave.

this type of modulation, a detector is required to discriminate between deviations above and below the center frequency and to translate these deviations into a voltage having an amplitude that varies at audio frequencies.

The FM detector shown in Fig. 120 is called a **balanced phase-shift discriminator**. In this detector, the mutually coupled tuned circuits in the primary and secondary windings of the transformer T are tuned to the center frequency. A characteristic of a double-tuned transformer is that the voltages in the primary and secondary windings are 90 degrees out of phase at resonance, and that the phase shift changes as the frequency

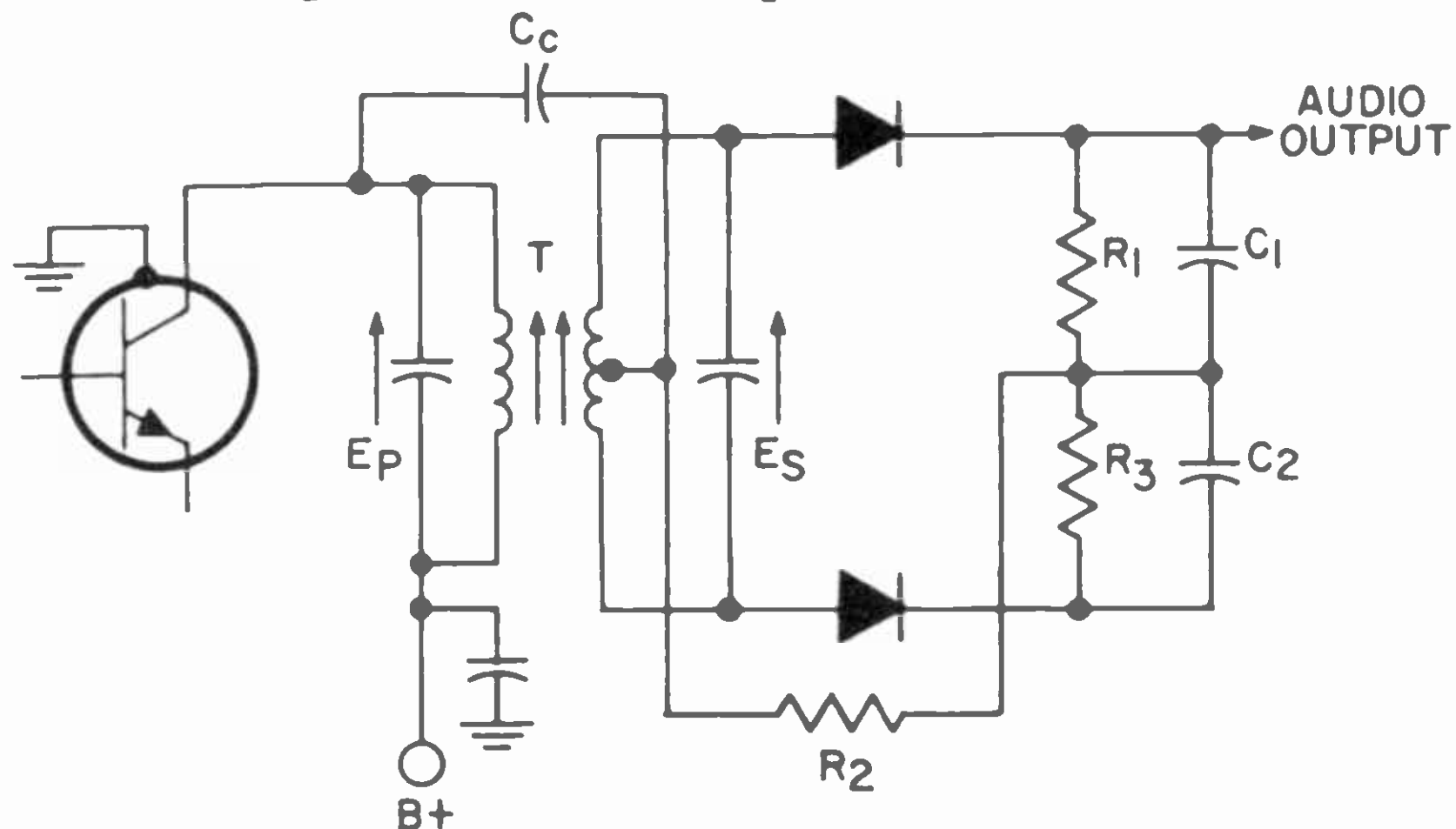


Fig. 120—Balanced phase-shift discriminator circuit.

changes from resonance. Therefore, the signal applied to the diodes and the RC combinations for peak detection also changes with frequency.

Because the secondary winding of the transformer T is center-tapped, the applied primary voltage E_p is added to one-half the secondary voltage E_s through the capacitor C_1 . The addition of these voltages at resonance can be represented by the diagram in Fig. 121; the resultant voltage E_1 is the signal applied to one peak-detector network consisting of

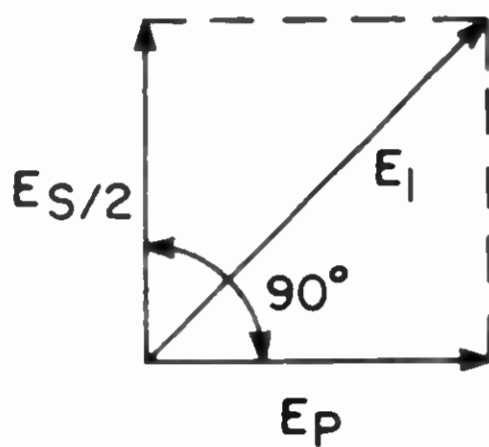


Fig. 121—Diagram illustrating phase shift in double-tuned transformer at resonance.

one diode and its RC load. When the signal frequency decreases (from resonance), the phase shift of $E_s/2$ becomes greater than 90 degrees, as shown at (a) in Fig. 122, and E_1 becomes smaller. When the signal frequency increases (above resonance), the phase shift of $E_s/2$ is less than 90 degrees, as shown at (b), and E_1 becomes larger. The curve

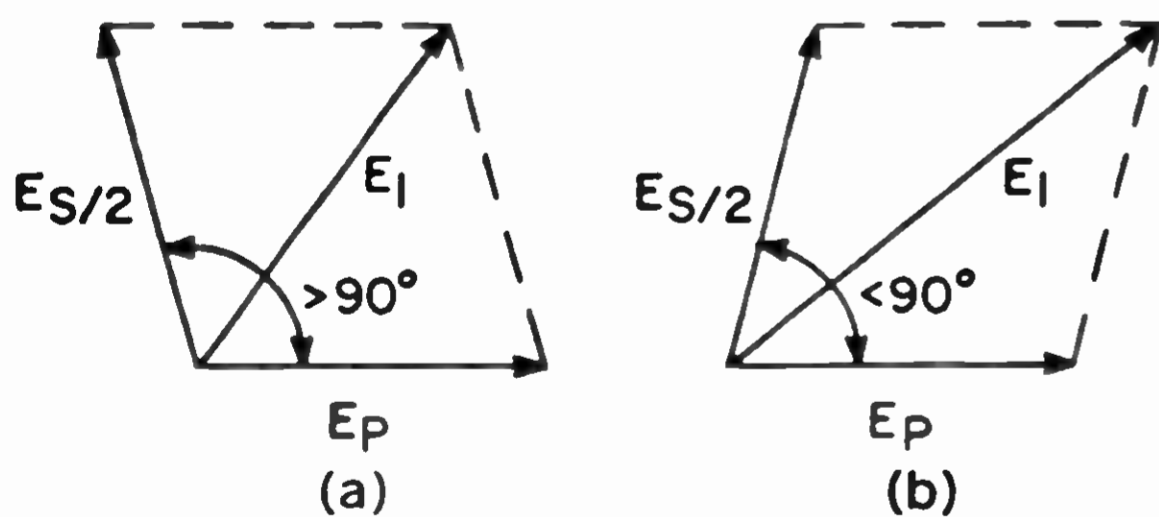


Fig. 122—Diagrams illustrating phase shift in double-tuned transformer (a) below resonance and (b) above resonance.

of E_1 as a function of frequency in Fig. 123 is readily identified as the response curve of an FM detector.

Because the discriminator circuit shown in Fig. 120 uses a push-pull configuration, the diodes conduct on alternate half-cycles of the signal frequency and produce a plus-and-minus output with respect to zero rather than with respect to E_1 . The primary advantage of this arrangement is that there is no output at

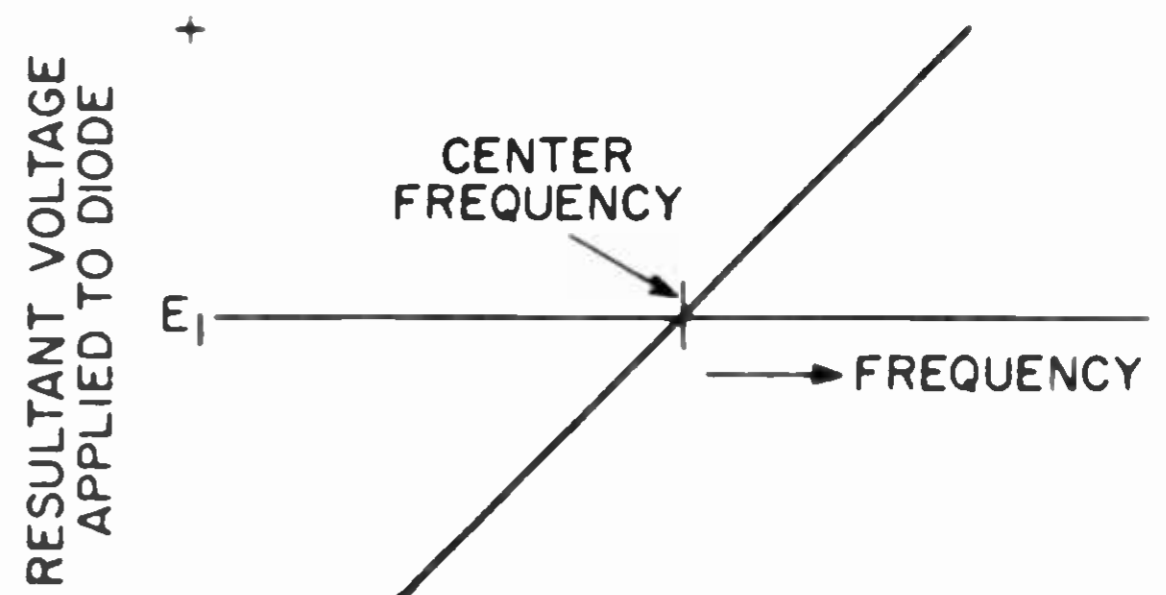


Fig. 123—Diagram showing resultant voltage E_1 in Fig. 121 as a function of frequency.

resonance. When an FM signal is applied to the input, the audio output voltage varies above and below zero as the instantaneous frequency varies above and below resonance. The frequency of this audio voltage is determined by the modulation frequency of the FM signal, and the amplitude of the voltage is proportional to the frequency excursion from resonance. (The resistor R_2 in the circuit provides a dc return for the diodes, and also maintains a load impedance across the primary winding of the transformer.)

One disadvantage of the balanced phase-shift discriminator shown in Fig. 120 is that it detects amplitude modulation (AM) as well as frequency modulation (FM) in the if signal because the circuit is balanced only at the center frequency. At frequencies off resonance, any variation in amplitude of the if signal is reproduced to some extent in the audio output.

The ratio-detector circuit shown in Fig. 124 is a discriminator circuit which has the advantage of being relatively insensitive to amplitude variations in the FM signal. In this circuit, E_p is added to $E_s/2$ through the mutual coupling M_2 (this voltage addition may be made by either mutual or capacitive coupling). Because of the phase-shift relationship of these voltages, the resultant detected signals vary with frequency variations in the same manner as described for the phase-discriminator circuit shown in Fig. 120. However, the diodes in the ratio detector are placed "back-to-back" (in series, rather than in push-pull) so

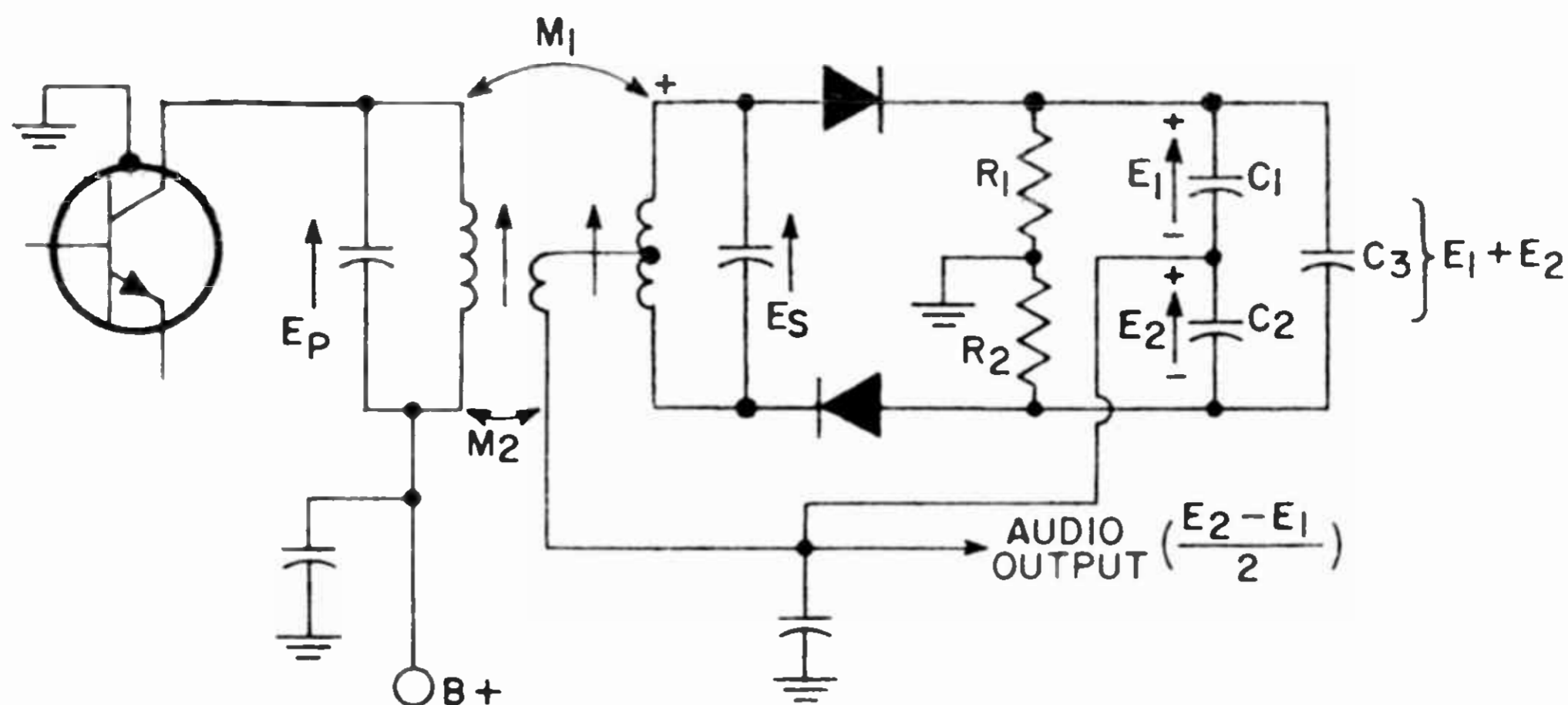


Fig. 124—Ratio-detector circuit.

that both halves of the circuit operate simultaneously during one-half of the signal frequency cycle (and are cut off on the other half-cycle). As a result, the detected voltages E_1 and E_2 are in series, as shown for the instantaneous polarities that occur during the conduction half-cycle. When the audio output is taken between the equal capacitors C_1 and C_2 , therefore, the output voltage is equal to $(E_2 - E_1)/2$ (for equal resistors R_1 and R_2).

The dc circuit of the ratio detector consists of a path through the secondary winding of the transformer, both diodes (which are in series), and resistors R_1 and R_2 . The value of the electrolytic capacitor C_3 is selected so that the time constant of R_1 , R_2 , and C_3 is very long compared to the detected audio signal. As a result, the sum of the detected voltages ($E_1 + E_2$) is a constant and the AM components on the signal frequency are suppressed. This feature of the ratio detector provides improved AM rejection as compared to the phase-shift discriminator circuit shown in Fig. 120.

AMPLIFICATION

The amplifying action of a transistor can be used in various ways in electronic circuits, depending on the results desired. The four recognized classes of amplifier service can be defined for transistor circuits as follows:

A class A amplifier is an amplifier in which the base bias and alternating signal are such that collector current in a transistor flows continuously during the complete electrical cycle of the signal, and even when no signal is present.

A class AB amplifier is an amplifier in which the base bias and alternating signal are such that collector current in a transistor flows for appreciably more than half but less than the entire electrical cycle.

A class B amplifier is an amplifier in which the base is biased to approximately collector-current cutoff, so that collector current is approximately zero when no signal is applied, and so that collector current in a transistor flows for approximately one-half of each cycle when an alternating signal is applied.

A class C amplifier is an amplifier in which the base is biased to such a degree that the collector current in a transistor is zero when no signal is applied, and so that collector current in a transistor flows for appreciably less than one-half of each cycle when an alternating signal is applied.

For radio-frequency (rf) amplifiers which operate into selective tuned circuits, or for other amplifiers in which distortion is not a prime factor, any of the above classes of amplification may be used with either a single transistor or a push-pull stage. For audio-frequency (af) amplifiers in which distortion is an

important factor, single transistors can be used only in class A amplifiers. For class AB or class B audio-amplifier service, a balanced amplifier stage using two transistors is required. A push-pull stage can also be used in class A audio amplifiers to obtain reduced distortion and greater power output. Class C amplifiers cannot be used for audio or AM applications.

Audio Amplifiers

Audio amplifier circuits are used in radio and television receivers, public address systems, sound recorders and reproducers, and similar applications to amplify signals in the frequency range from 20 to 20,000 Hz. Each transistor in an audio amplifier can be considered as either a current amplifier or a power amplifier. The type of circuit configuration selected is dictated by the requirements of the given application. The output power to be supplied, the required sensitivity and frequency response, and the maximum distortion limits, together with the capabilities and limitations of available devices, are the main criteria used to determine the circuit that will provide the desired performance most efficiently and economically.

In addition to the consideration that must be given to the achievement of performance objectives and the selection of the optimum circuit configuration, the circuit designer must also take steps to insure reliable operation of the audio amplifier under varying conditions of signal level, frequency, ambient temperature, load impedance, line voltage, and other factors which may subject the transistors to either transient or steady-state high stress levels. Low-cost, low-power audio systems (such as those used in mobile and TV output stages), in which high operating efficiency is not an important consideration, usually employ a single-ended, class A, transformer-coupled output stage such as that shown in Fig. 125.

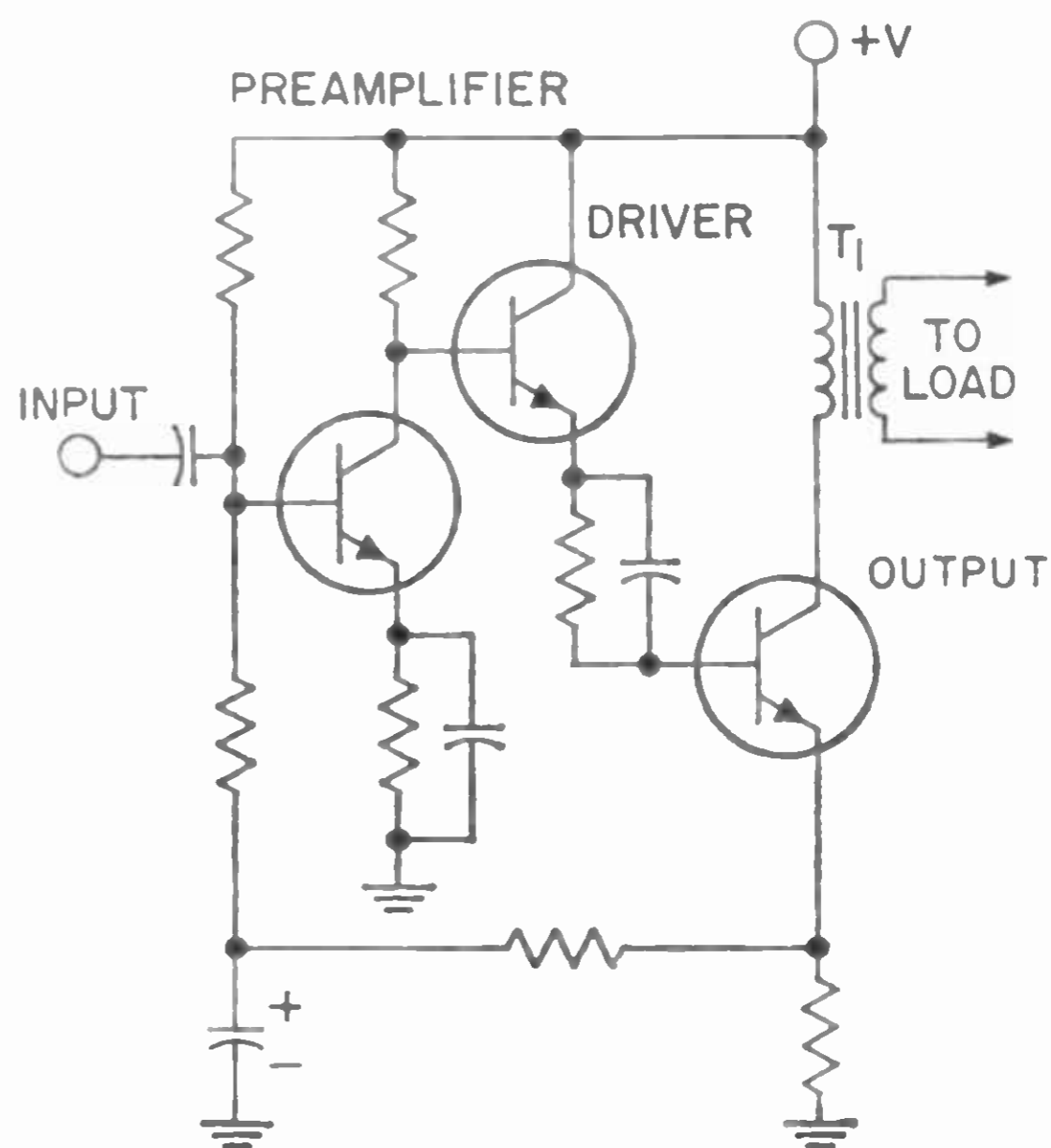


Fig. 125—Typical low-power audio-amplifier circuit.

Simple class A amplifier circuits are normally used in low-level audio stages such as preamplifiers and drivers. Preamplifiers usually follow low-level output transducers such as microphones, hearing-aid and phonograph pickup devices, and recorder-reproducer heads.

One of the important characteristics of a low-level amplifier circuit is its **signal-to-noise ratio**, or **noise figure**. The input circuit of an amplifier inherently contains some thermal noise contributed by the resistive elements in the input device. All resistors generate a predictable quantity of noise power as a result of thermal activity. This power is about 160 dB below one watt for a bandwidth of 10 kHz.

When an input signal is amplified, therefore, the thermal noise generated in the input circuit is also amplified. If the ratio of signal power to noise power (S/N) is the same in the output circuit as in the input circuit, the amplifier is considered to be "noiseless" and is said to have a noise figure of unity, or zero dB.

In practical circuits, however, the ratio of signal power to noise power is inevitably impaired during amplification as a result of the generation of additional noise in the circuit ele-

ments. A measure of the degree of impairment is called the noise figure (NF) of the amplifier, and is expressed as the ratio of signal power to noise power at the input (S_i/N_i) divided by the ratio of signal power to noise power at the output (S_o/N_o), as follows:

$$NF = \frac{S_i/N_i}{S_o/N_o}$$

The noise figure in dB is equal to ten times the logarithm of this power ratio. For example, an amplifier with a one-dB noise figure decreases the signal-to-noise ratio by a factor of 1.26, a 3-dB noise figure by a factor of 2, a 10-dB noise figure by a factor of 10, and a 20-dB noise figure by a factor of 100.

In audio amplifiers, it is desirable that the noise figure be kept low. In general, the lowest value of NF is obtained by use of an emitter current of less than one milliamper and a collector voltage of less than two volts for a signal-source resistance between 300 and 3000 ohms. If the input impedance of the transistor is matched to the impedance of the signal source, the lowest value of NF that can be attained is 3 dB. Generally, the best noise figure is obtained by use of a transistor input impedance approximately 1.5 times the source impedance. However, this condition is often not realizable in practice because many transducers are reactive rather than resistive. In addition, other requirements such as circuit gain, signal-handling capability, and reliability may not permit optimization for noise.

In the simple low-level amplifier stage shown in Fig. 126, resistor R_1 determines the base bias for the transistor. The output signal is developed across the load resistor R_2 . The collector voltage and the emitter current are kept relatively low to reduce the noise figure. If the load impedance across the capacitor C_2 is low

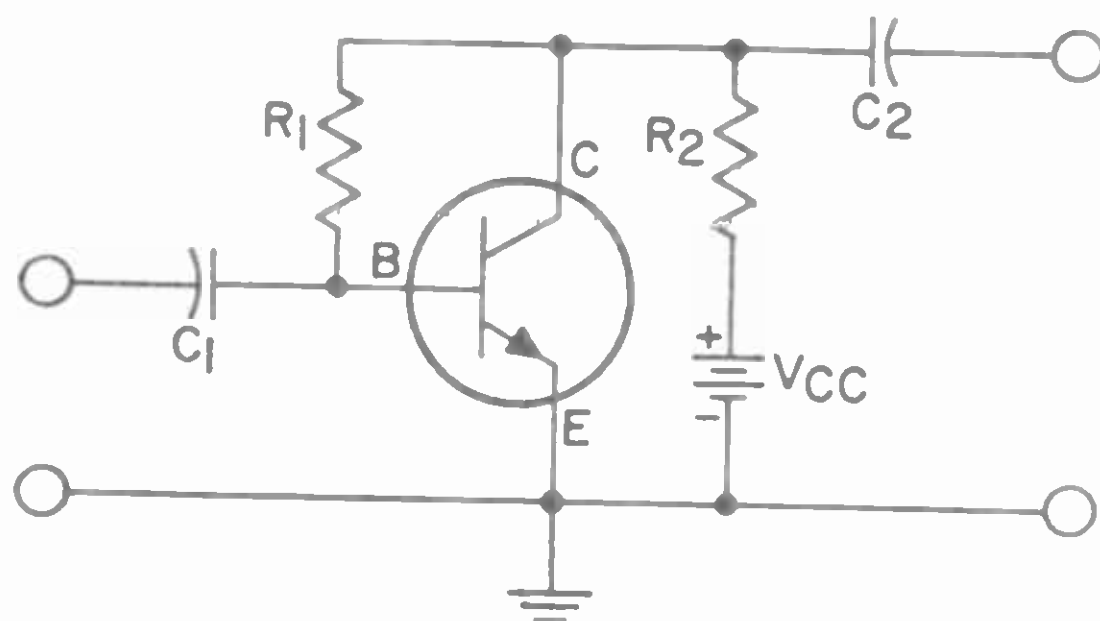


Fig. 126—Simple low-level class A amplifier.

compared to R_2 , very little voltage swing results on the collector. Therefore, ac feedback through R_1 does not cause much reduction in gain.

In many cases, low-level amplifier stages used as preamplifiers include some type of frequency-compensation network to enhance either the low-frequency or the high-frequency components of the input signal. The frequency range and dynamic range* which can be recorded on a phonograph record or on magnetic tape depend on several factors, including the composition, mechanical characteristics, and speed of the record or tape, and the electrical and mechanical characteristics of the recording equipment. To achieve wide frequency and dynamic range, manufacturers of commercial recordings use equipment which introduces a nonuniform relationship between amplitude and frequency. This relationship is known as a "recording characteristic". To assure proper reproduction of a high-fidelity recording, therefore, some part of the reproducing system must have a frequency-response characteristic which is the inverse of the recording characteristic. Most manufacturers of high-fidelity recordings use the RCA "New Orthophonic" (RIAA) characteristic for discs and the NARTB characteristic for magnetic tape.

The simplest type of equalization network is shown in Fig. 127. Because the capacitor C is effectively an open circuit at low frequencies, the low frequencies must be passed

* The dynamic range of an amplifier is a measure of its signal-handling capability. The dynamic range expresses in dB the ratio of the maximum usable output signal (generally for a distortion of about 10 per cent) to the minimum usable output signal (generally for a signal-to-noise ratio of about 20 dB). A dynamic range of 40 dB is usually acceptable; a value of 70 dB is exceptional for any audio system.

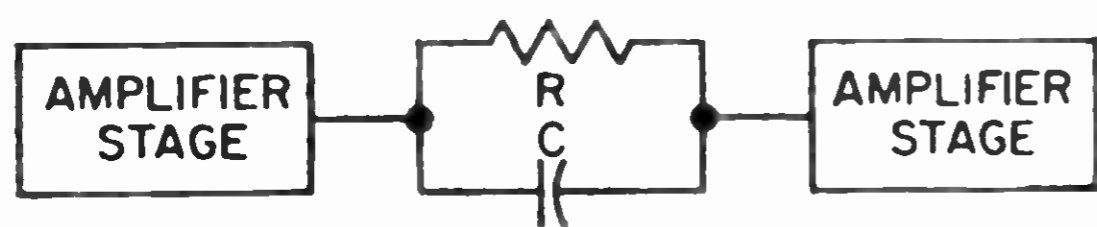


Fig. 127—Simple RC frequency-compensation network.

through the resistor R and are attenuated. The capacitor has a lower reactance at high frequencies, however, and bypasses high-frequency components around R so that they receive negligible attenuation. Thus the network effectively “boosts” the high frequencies. This type of equalization is called “attenuative”.

Some typical preamplifier stages are shown in the **Circuits** section. The location of the frequency-compensation network or “equalizer” in the reproducing system depends on the types of recordings which are to be reproduced and on the pickup devices used. All commercial pickup devices provide very low power levels to a transistor preamplifier stage.

A ceramic high-fidelity phonograph pickup is usually designed to provide proper compensation for the RIAA recording characteristic when the pickup is operated into the load resistance specified by its manufacturer. Usually, a “matching” resistor is inserted in series with the input of the preamplifier transistor. However, this arrangement produces a fairly small signal current which must then be amplified. If the matching resistor is not used, equalization is required, but some improvement can be obtained in dynamic range and gain.

A magnetic high-fidelity phonograph pickup, on the other hand, usually has an essentially flat frequency-response characteristic. Because a pickup of this type merely reproduces the recording characteristic, it must be followed by an equalizer network, as well as by a preamplifier having sufficient gain to satisfy the input requirements of the tone-control amplifier and/or power amplifier. Many designs include both the equalizing and amplifying circuits in a single unit.

A high-fidelity magnetic-tape pick-

up head, like a magnetic phonograph pickup, reproduces the recording characteristic. This type of pickup device, therefore, must also be followed by an equalizing network and preamplifier to provide equalization for the NARTB characteristic.

Feedback networks may also be used for frequency compensation and for reduction of distortion. Basically, a feedback network returns a portion of the output signal to the input circuit of an amplifier. The feedback signal may be returned in phase with the input signal (positive or regenerative feedback) or 180 degrees out of phase with the input signal (negative, inverse, or degenerative feedback). In either case, the feedback can be made proportional to either the output voltage or the output current, and can be applied to either the input voltage or the input current. A negative feedback signal proportional to the output current raises the output impedance of the amplifier; negative feedback proportional to the output voltage reduces the output impedance. A negative feedback signal applied to the input current decreases the input impedance; negative feedback applied to the input voltage increases the input impedance. Opposite effects are produced by positive feedback.

A simple negative or inverse feedback network which provides high-frequency boost is shown in Fig. 128.

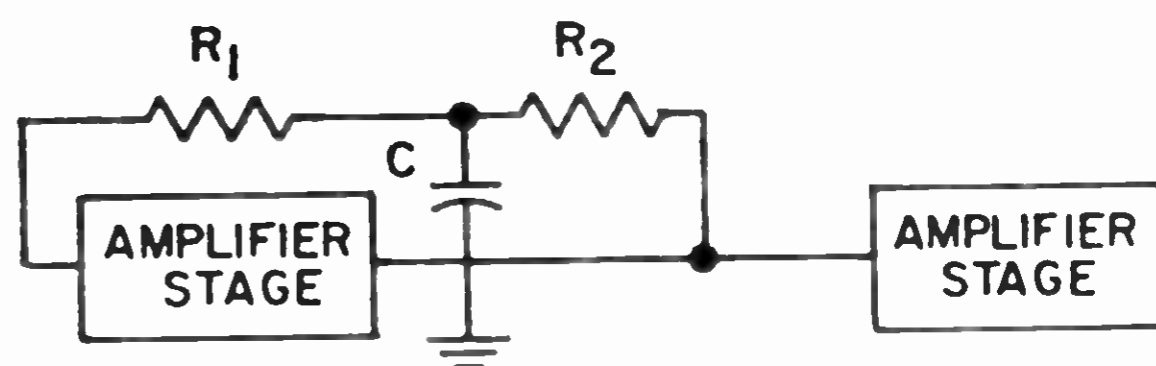


Fig. 128—Negative-feedback frequency-compensation network.

This network provides equalization comparable to that obtained with Fig. 127, but is more suitable for low-level amplifier stages because it does not require the first amplifier stage to provide high-level low frequencies. In addition, the inverse feedback improves the distortion characteristics of the amplifier.

As mentioned previously, it is undesirable to use a high-resistance signal source for a transistor audio amplifier because the extreme impedance mismatch results in high noise figure. High source resistance cannot be avoided, however, if an input device such as a ceramic pickup is used. In such cases, the use of negative feedback to raise the input impedance of the amplifier circuit (to avoid mismatch loss) is no solution because feedback cannot improve the signal-to-noise ratio of the amplifier. A more practical method is to increase the input impedance somewhat by operating the transistor at the lowest practical current level and by using a transistor which has a high forward current-transfer ratio.

Some preamplifier or low-level audio amplifier circuits include variable resistors or potentiometers which function as volume or tone controls. Such circuits should be designed to minimize the flow of dc currents through these controls so that little or no noise will be developed by the movable contact during the life of the circuit. Volume controls and their associated circuits should permit variation of gain from zero to maximum, and should attenuate all frequencies equally for all positions of the variable arm of the control. Several examples of volume controls and tone controls are shown in the Circuits section.

A tone control is a variable filter (or one in which at least one element

is adjustable) by means of which the user may vary the frequency response of an amplifier to suit his own taste. In radio receivers and home amplifiers, the tone control usually consists of a resistance-capacitance network in which the resistance is the variable element.

The simplest form of tone control is a "treble cut" network such as that shown in Fig. 129. As R_1 is made smaller, the capacitor C_2 bypasses more of the high audio frequencies; therefore, the output of

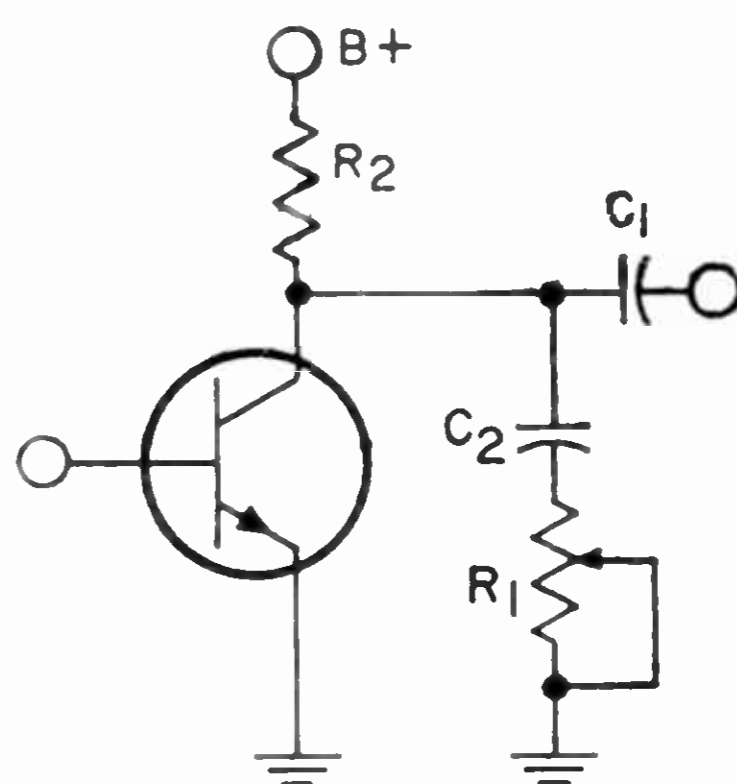


Fig. 129—Simple tone-control network for fixed tone compensation or equalization.

the network is decreased by an amount dependent upon the value of R_1 . The resistance of R_1 should be very large in comparison to the reactance of C_2 at the highest audio frequency.

The tone-control network shown in Fig. 130 has two stages with completely separate bass and treble con-

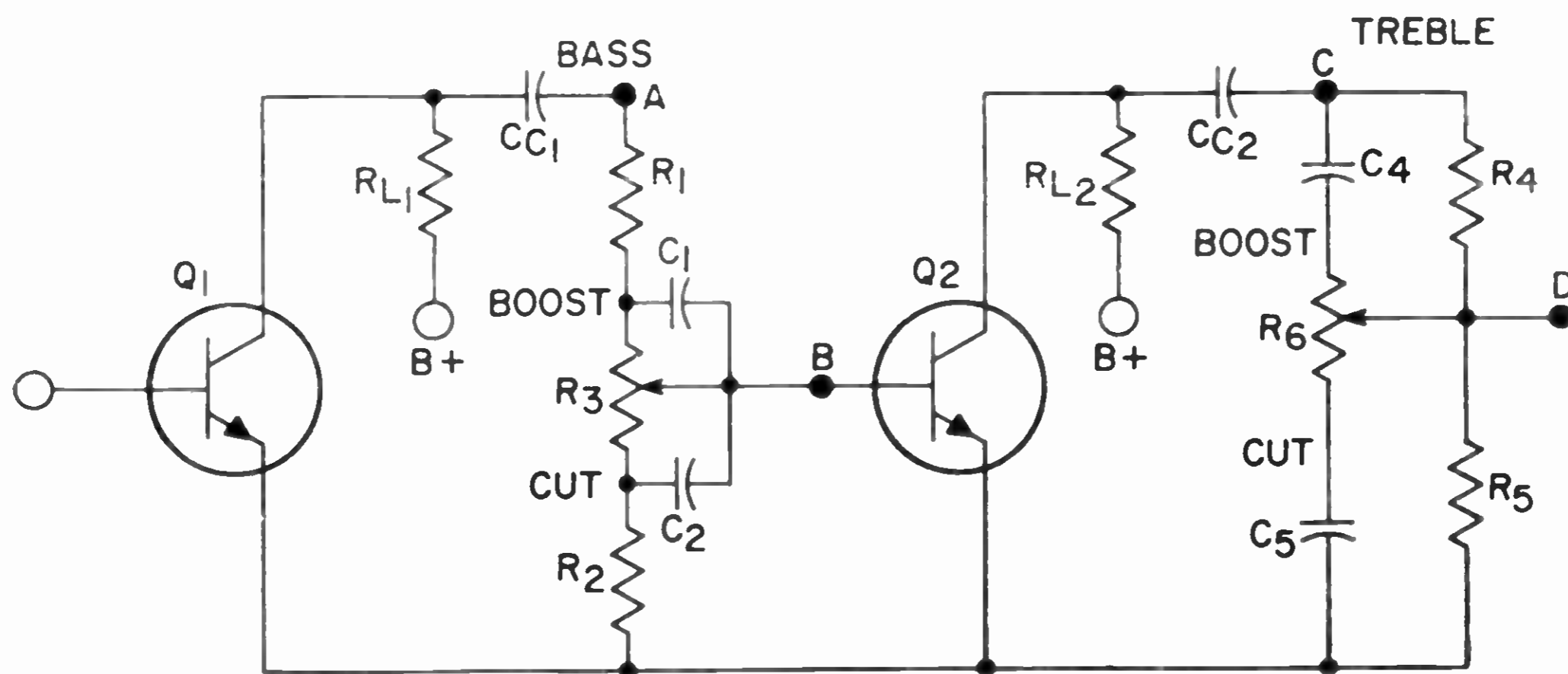


Fig. 130—Two-stage tone-control circuit incorporating separate bass and treble controls.

trols. Fig. 131 shows simplified representations of the bass control when the potentiometer is turned to its extreme variations (labeled BOOST and CUT). At very high frequencies, C_1 and C_2 are effectively short circuits and the network becomes the simple voltage divider R_1 and R_2 . In the bass-boost position, R_3 is inserted in series with R_2 so that there is less attenuation to very low frequencies than to very high frequencies. Therefore, the bass is said to be "boosted". In the bass-cut position, R_3 is inserted in series with R_1 so that there is more attenuation to very low frequencies.

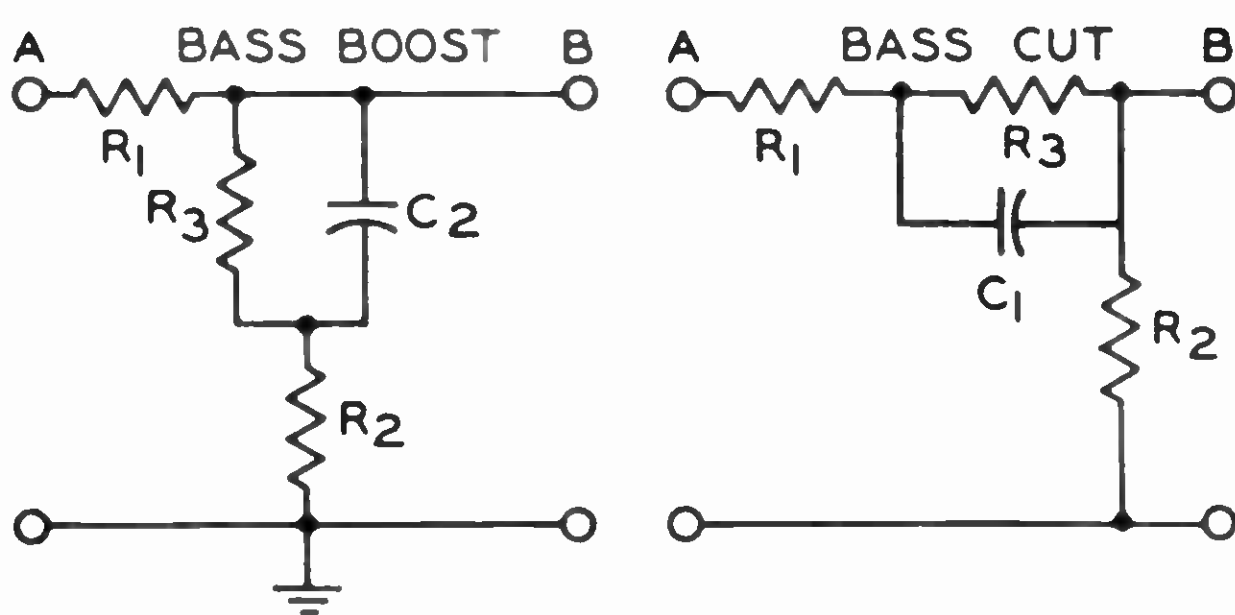


Fig. 131—Simplified representations of bass-control circuit at extreme ends of potentiometer.

Fig. 132 shows extreme positions of the treble control. R_5 is generally much larger than R_4 or R_6 and may be treated as an open circuit in the extreme positions. In both the boost and cut positions, very low frequencies are controlled by the voltage divider R_4 and R_5 . In the boost position,

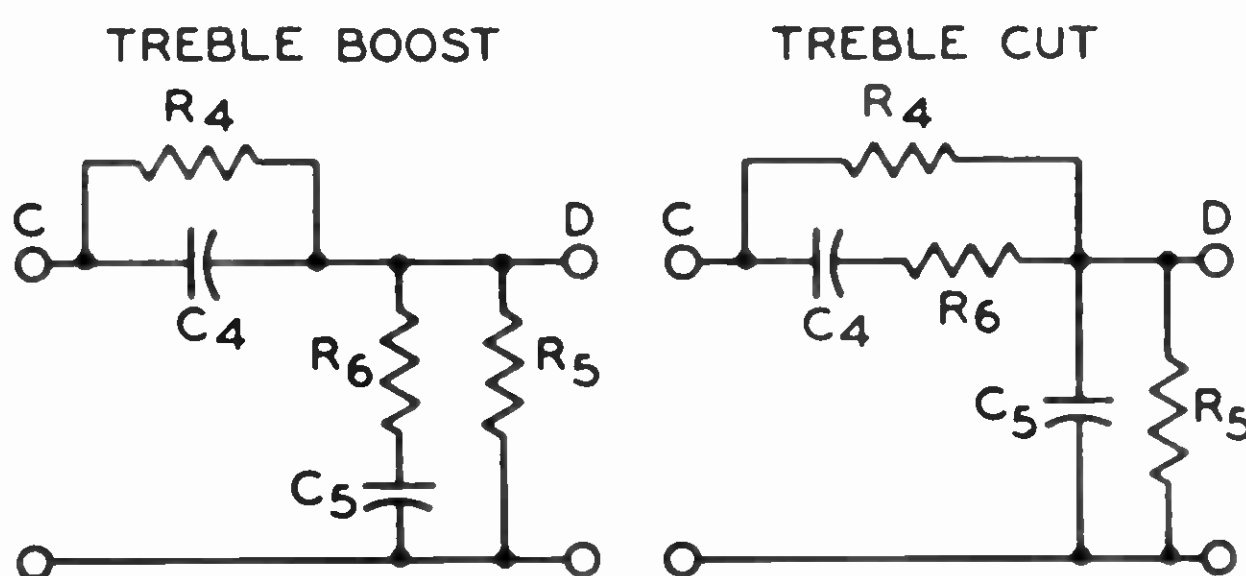


Fig. 132—Simplified representations of treble-control circuit at extreme ends of potentiometer.

R_4 is bypassed by the high frequencies and the voltage-divider point D is placed closer to C. In the cut position, R_5 is bypassed and there is greater attenuation of the high frequencies.

The frequencies at which boost and cut occur in the circuit of Fig. 130 are controlled by the values of C_1 , C_2 , C_3 , and C_5 . Both the output impedance of the driving stage (generally R_{L1}) and the loading of the driven stage affect the response curves and must be considered. This tone-control circuit, like the one in Fig. 129, is attenuative. Feedback tone controls may also be employed.

The location of a tone-control network is of considerable importance. In a typical preamplifier, it may be in the collector circuit of the final low-level stage or in the input circuit of the first stage. If the amplifier incorporates negative feedback, the tone control must be inserted in a part of the amplifier which is external to the feedback loop, or must be made a part of the feedback network. The over-all gain of a well designed tone-control network should be approximately unity. The system dynamic range should be adequate for all frequencies anticipated with the tone controls in any position. The high-frequency gain should not be materially affected as the bass control is varied, nor should the low-frequency gain be sensitive to the treble control.

Driver stages in audio amplifiers are located immediately before the power-output stage. When a single-ended class A output stage is used, the driver stage is similar to a preamplifier stage. When a push-pull output stage in which both transistors are the same type (n-p-n or p-n-p) is used, however, the audio driver must provide two output signals, each 180 degrees out of phase with the other. This phase requirement can be met by use of a tapped-secondary transformer between a single-ended driver stage and the output stage, as shown in Fig. 133. The transformer T_1 provides the required out-of-phase input signals for the two transistors Q_1 and Q_2 in the push-pull output stage.

Transistor audio power amplifiers may be class A single-ended stages,

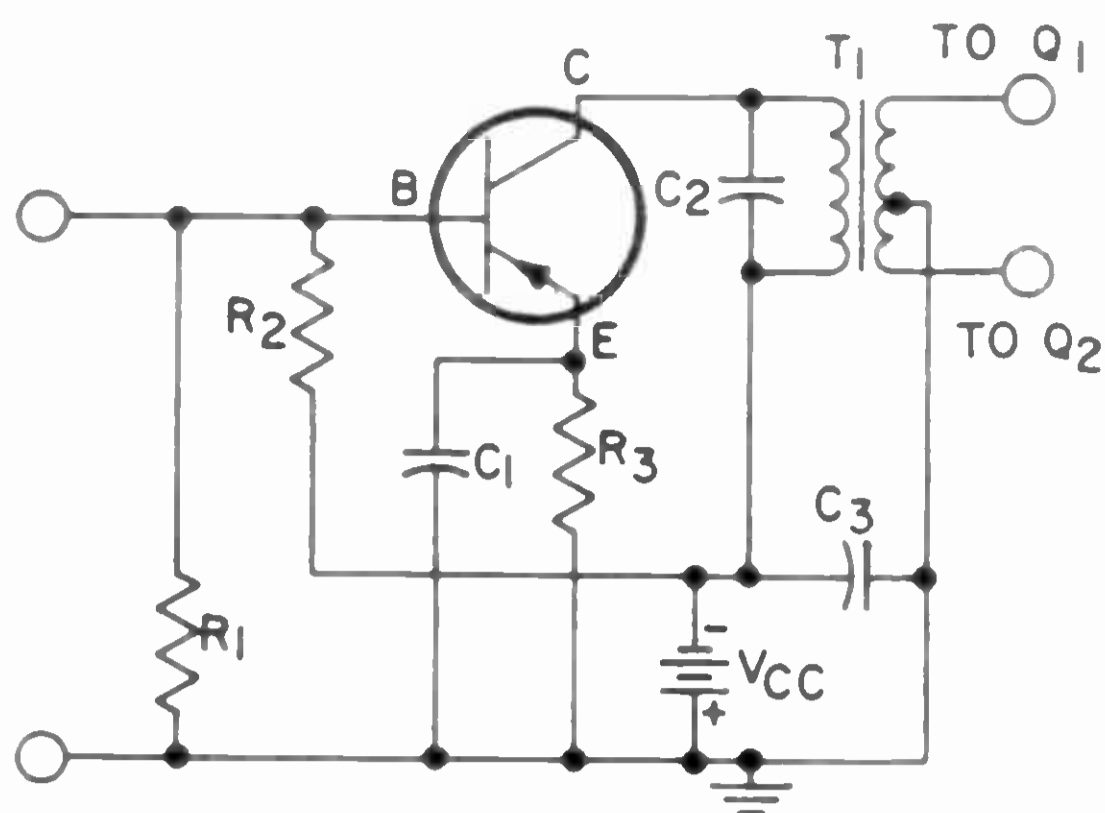


Fig. 133—Driver stage for push-pull output circuit.

or class A, class AB, or class B push-pull stages. A simple class A single-ended power amplifier is shown in Fig. 134. Component values which will provide the desired power output can be calculated from the

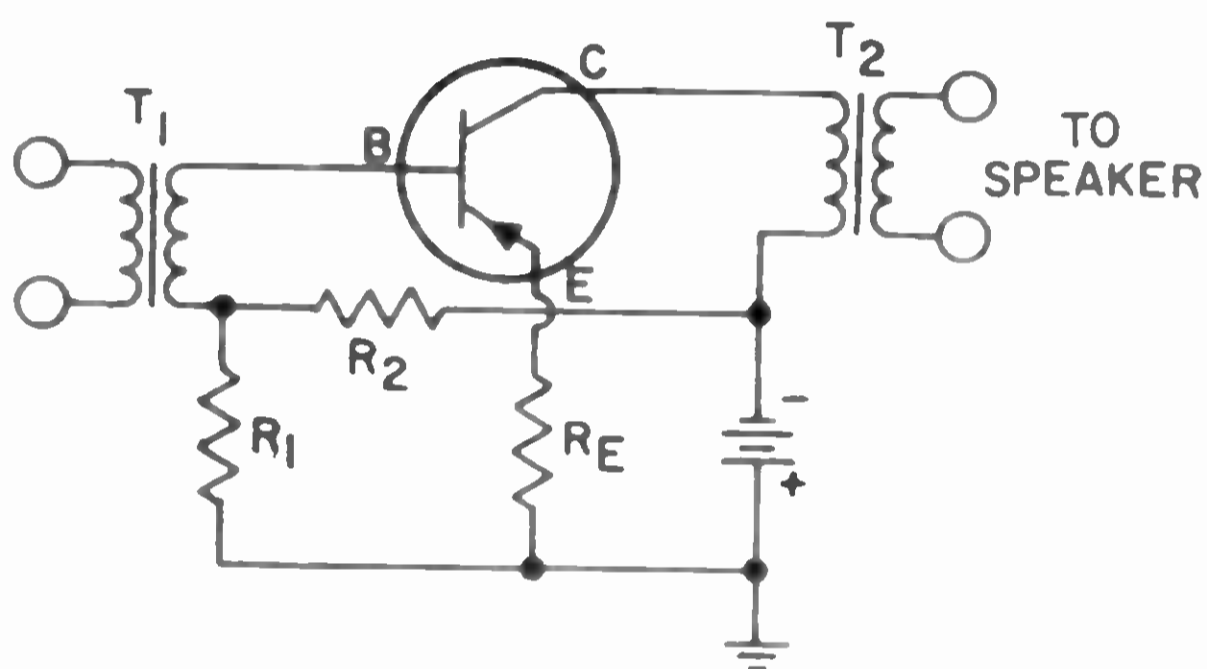


Fig. 134—Class A power-amplifier circuit.

transistor characteristics and the supply voltage. For example, an output of four watts may be desired from a circuit operating with a supply voltage of 14.5 volts (this voltage is normally available in automobiles which have a 12-volt ignition system). If losses are assumed to be negligible, the power output (P_o) is equal to the peak collector voltage (e_c) times the peak collector current (i_c), each divided by the square root of two to obtain rms values. The peak collector current can then be determined as follows:

$$P_o = \frac{e_c}{\sqrt{2}} \times \frac{i_c}{\sqrt{2}}$$

$$i_c = P_o (\sqrt{2}) \times \frac{\sqrt{2}}{e_c}$$

$$= 4 \sqrt{2} \times \frac{\sqrt{2}}{14.5}$$

$$= 0.55, \text{ or approximately } 0.6 \text{ ampere.}$$

In class A service, the dc collector current and the peak collector swing are about the same. Thus, the collector voltage and current are 14.5 volts and 0.6 ampere, respectively.

The voltage drop across the resistor R_E in Fig. 134 usually ranges from 0.3 to 1 volt; a typical value of 0.6 volt can be assumed. The value of R_E must equal the 0.6-volt drop divided by the 0.6-ampere emitter current, or one ohm. (The emitter current is assumed to be nearly equal to the 0.6-ampere collector current.)

The current through resistor R_2 should be about 10 to 20 per cent of the collector current; a typical value is 15 per cent of 0.6, or 90 milliamperes.

The voltage from base to ground is equal to the base-to-emitter voltage (determined from the transistor transfer-characteristics curves for the desired collector or emitter current; normally about 0.4 volt for a germanium power transistor operating at an emitter current of 600 milliamperes) plus the emitter-to-ground voltage (0.6 volt as described above), or one volt. The voltage across R_2 , therefore, is 14.5 minus 1, or 13.5 volts. The value of R_2 must equal 13.5 divided by 90, or about 150 ohms.

Because the voltage drop across the secondary winding of the driver transformer T_1 is negligible, the voltage drop across R_1 is one volt. The current through R_1 equals the current through R_2 (90 milliamperes) minus the base current. If the dc forward current-transfer ratio (beta) of the transistor selected has a typical value of 60, the base current equals the collector current of 600 milliamperes divided by 60, or 10 milliamperes. The current through R_1 is then 90 minus 10, or 80 milliamperes, and the value of R_1 is 1 divided by 80, or about 12 ohms.

The transformer requirements are determined from the ac voltages and currents in the circuit. The peak collector voltage swing that can be used before distortion occurs as a result of clipping of the output volt-

age is about 13 volts. The peak collector current swing available before current cutoff occurs is the dc current of 600 milliamperes. Therefore, the collector load impedance should be 13 volts divided by 600 milliamperes, or about 20 ohms, and the output transformer T_2 should be designed to match a 20-ohm primary impedance to the desired speaker impedance. If a 3.2-ohm speaker is used, for example, the impedance values for T_2 should be 20 ohms to 3.2 ohms.

The total input power to the circuit of Fig. 134 is equal to the voltage required across the secondary winding of the driver transformer T_1 times the current. The driver signal current is equal to the base current (10 milliamperes peak, or 7 milliamperes rms). The peak ac signal voltage is nearly equal to the sum of the base-to-emitter voltage across the transistor (0.4 volt as determined above), plus the voltage across R_E (0.6 volt), plus the peak ac signal voltage across R_1 (10 milliamperes times 12 ohms, or 0.12 volt). The input voltage, therefore, is about one volt peak, or 0.7 volt rms. Thus, the total ac input power required to produce an output of 4 watts is 0.7 volt times 7 milliamperes, or 5 milliwatts, and the input impedance is 0.7 volt divided by 7 milliamperes, or 100 ohms.

Higher power output can be achieved with less distortion in class A service by the use of a push-pull circuit arrangement. One of the disadvantages of a transistor class A amplifier (single-ended or push-pull), however, is that collector current flows at all times. As a result, transistor dissipation is highest when no ac signal is present. This dissipation can be greatly reduced by use of class B push-pull operation. When two transistors are connected in class B push-pull, one transistor amplifies half of the signal, and the other transistor amplifies the other half. These half-signals are then combined in the output circuit to re-

store the original waveform in an amplified state.

Ideally, transistors used in class B push-pull service should be biased to collector cutoff so that no power is dissipated under zero-signal conditions. At low signal inputs, however, the resulting signal would be distorted, as shown in Fig. 135, because of the low forward current-transfer ratio of the transistor at very low currents. This type of distortion, called **cross-over distortion**, can be suppressed by the use of a bias voltage which permits a small collector current flow at zero signal level. Any residual distortion can be further reduced by the use of negative feedback.

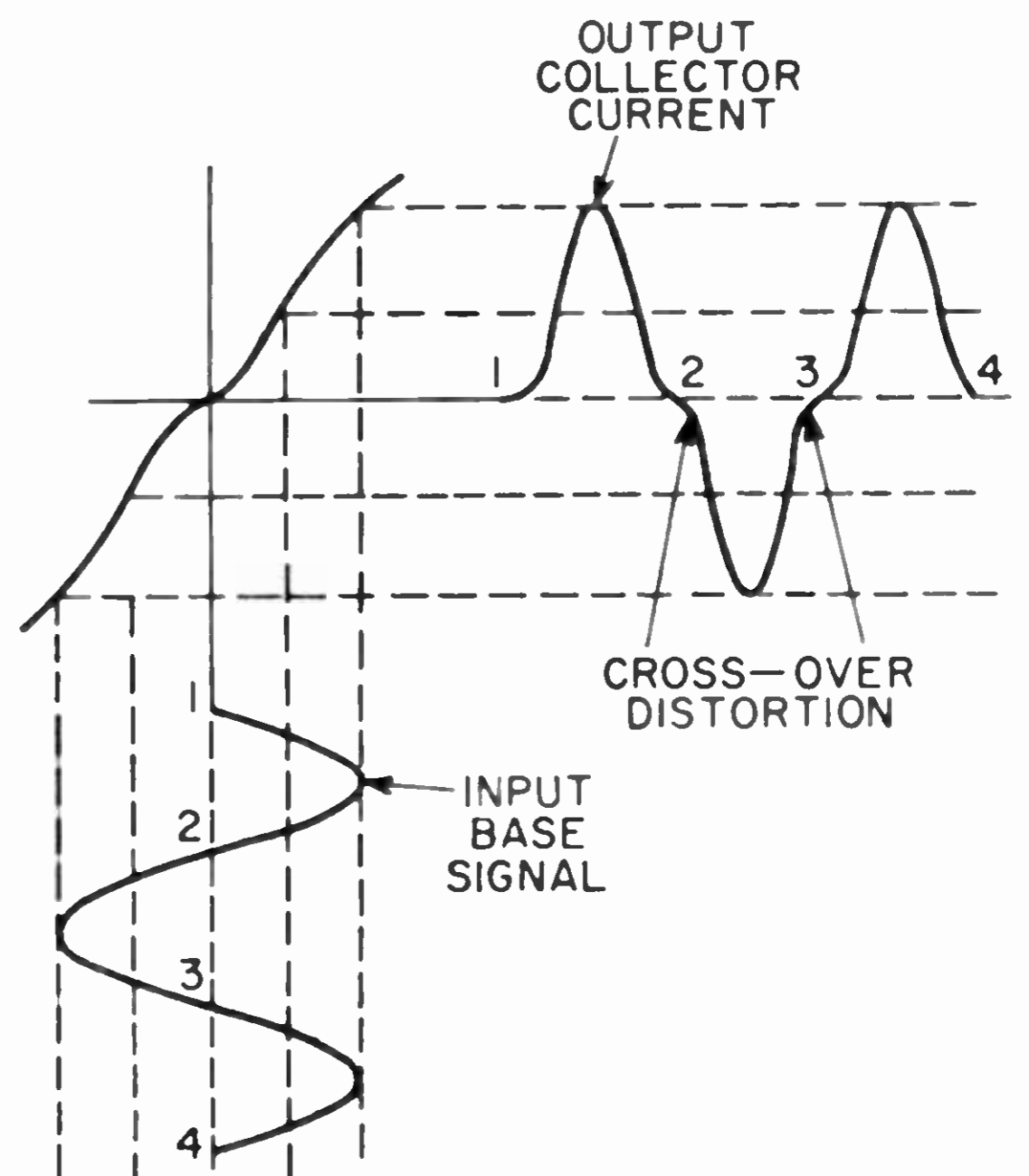


Fig. 135—Waveforms showing cause of cross-over distortion.

A typical class B push-pull audio amplifier is shown in Fig. 136. Resistors R_{E1} and R_{E2} are the emitter stabilizing resistors. Resistors R_1 and R_2 form a voltage-divider network which provides the bias for the transistors. The base-emitter circuit is biased near collector cutoff so that very little collector power is dissipated under no-signal conditions. The characteristics of the bias network must be very carefully chosen so that the bias voltage will be just sufficient to minimize cross-over distortion at low signal levels. Because

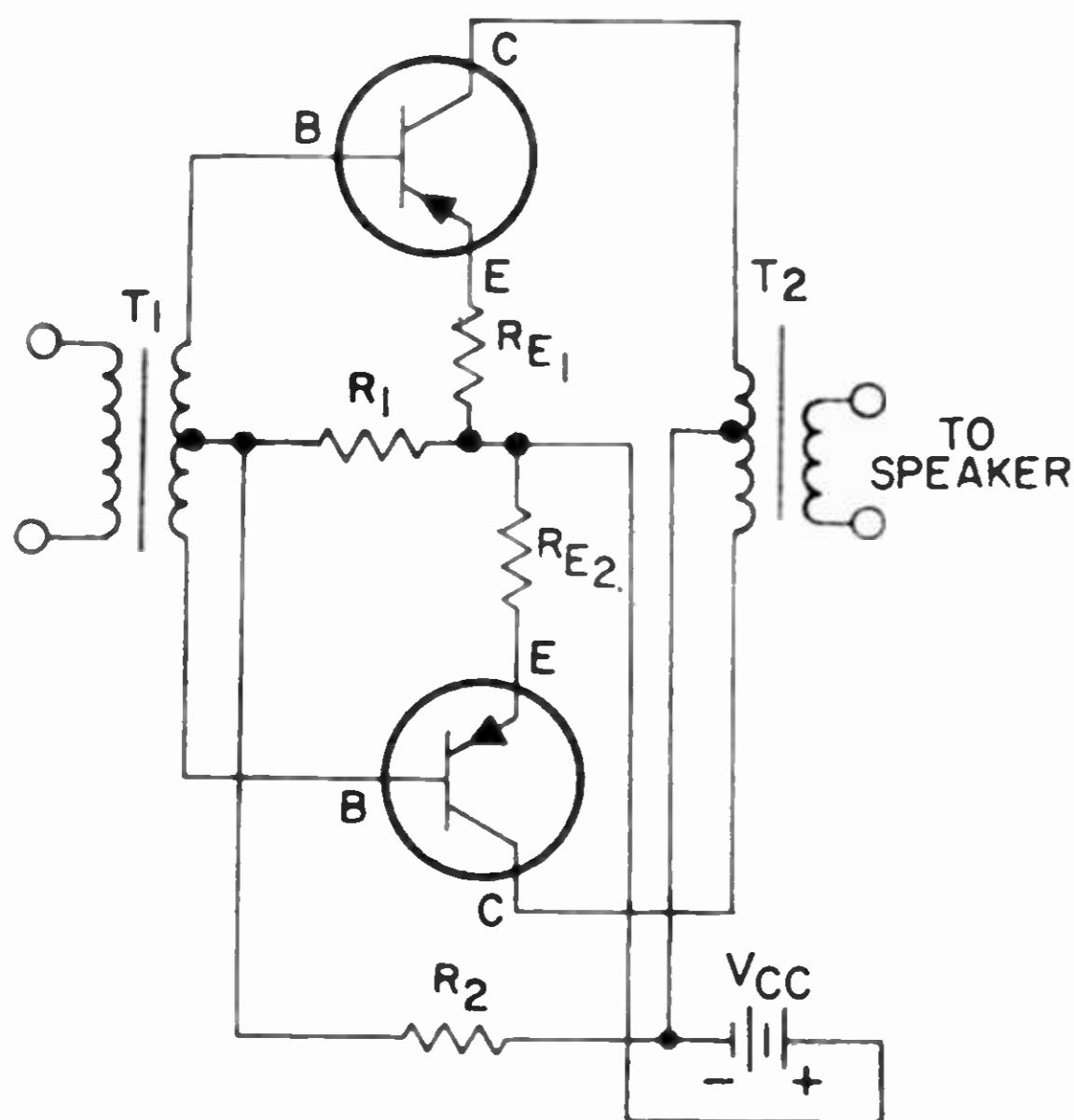


Fig. 136—Class B push-pull audio-amplifier circuit.

the collector current, collector dissipation, and dc operating point of a transistor vary with ambient temperature, a temperature-sensitive resistor (such as a thermistor) or a bias-compensating diode may be used in the biasing network to minimize the effect of temperature variations.

The advantages of class B push-pull operation can be obtained without the need for an output transformer by use of a circuit such as that shown in Fig. 137. In this circuit, the secondary windings of the driver transformer T_1 are phased so that a negative signal from base to emitter of one transistor is accompanied by a positive signal from

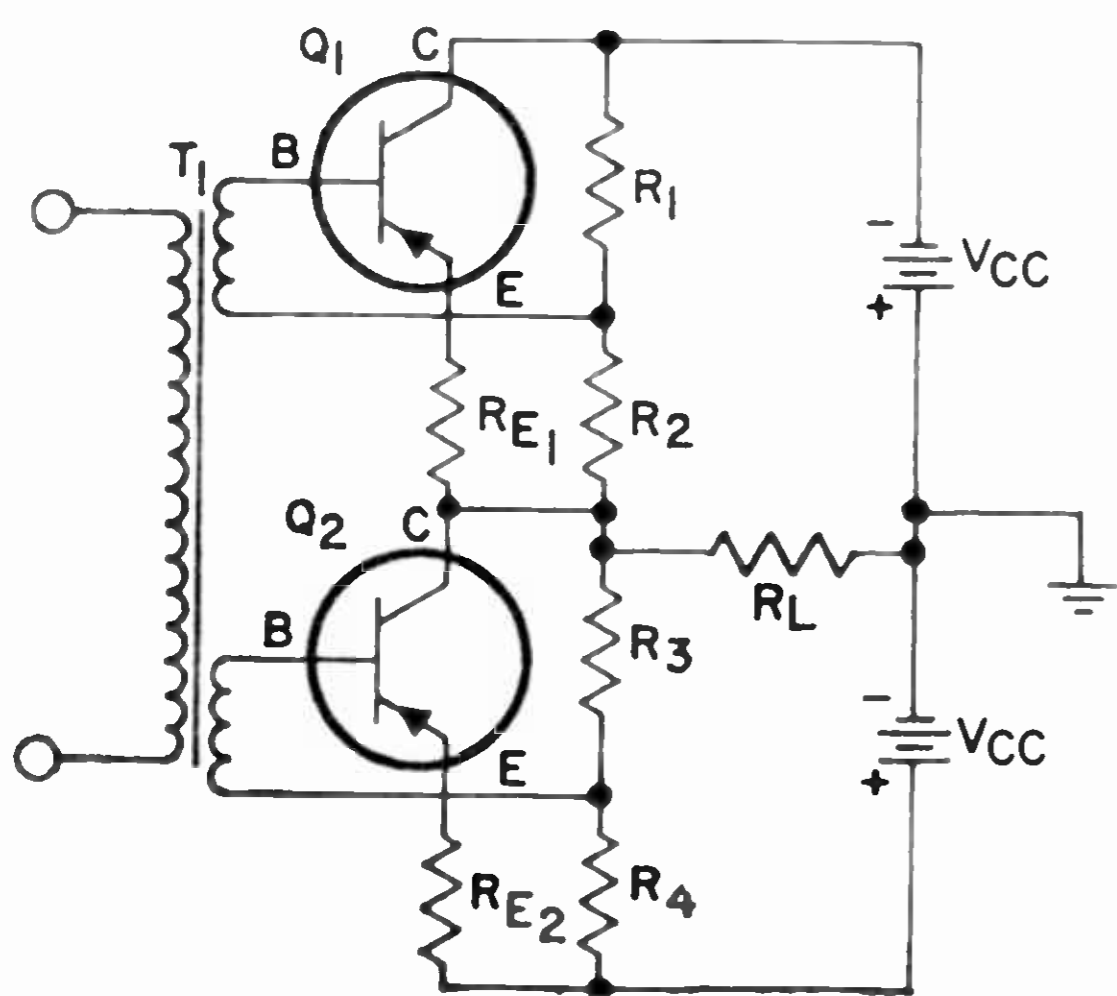


Fig. 137—Single-ended class B circuit.

base to emitter of the other transistor. When a negative signal is applied to the base of transistor Q_1 , for example, Q_1 draws current. This current must flow through the load because the accompanying positive signal on the base of transistor Q_2 cuts Q_2 off. When the signal polarity reverses, transistor Q_1 is cut off, while Q_2 conducts current. The resistive dividers R_1, R_2 and R_3, R_4 provide a dc bias which keeps the transistors slightly above cutoff under no-signal conditions and thus minimizes cross-over distortion. The emitter resistors R_{E1} and R_{E2} help to compensate for differences between transistors and for the effects of ambient-temperature variations.

The secondary windings of any class B driver transformer should be bifilar-wound (i.e., wound together) to obtain tighter coupling and thereby minimize leakage inductance. Otherwise, "ringing" may occur in the cross-over region as a result of the energy stored in the leakage inductance.

Because junction transistors can be made in both p-n-p and n-p-n types, they can be used in **complementary-symmetry** circuits to obtain all the advantages of conventional push-pull amplifiers plus direct coupling. The arrows in Fig. 138 indicate the direction of electron current flow in the terminal leads of p-n-p and n-p-n transistors. When these

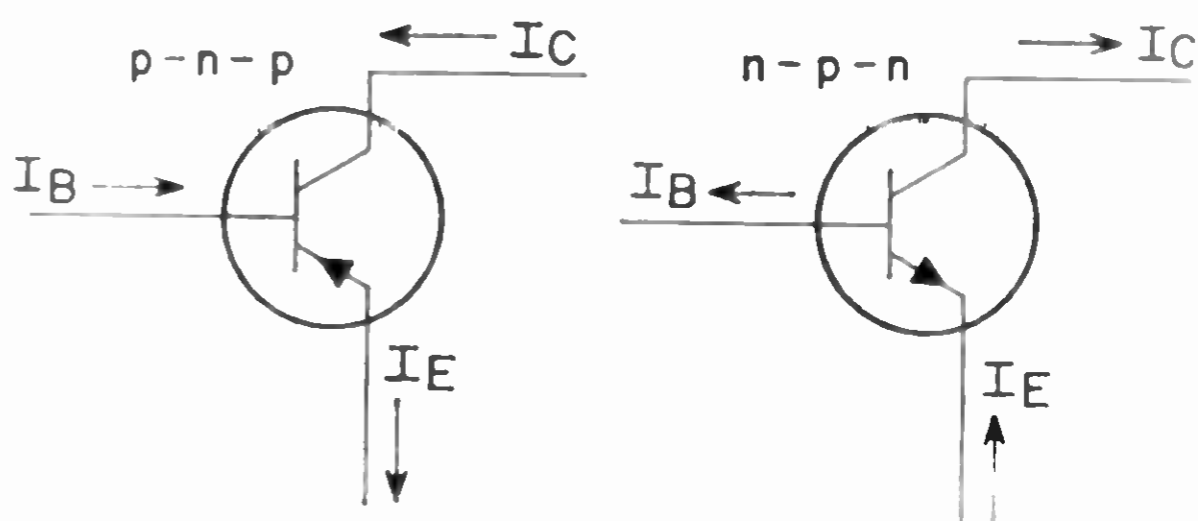


Fig. 138—Electron-current flow in p-n-p and n-p-n transistors.

two transistors are connected in a single stage, as shown in Fig. 139, the steady-state electron current path in the output circuit is completed through the collector-emitter circuits of the transistors. In the circuits of Figs. 137 and 139, essen-

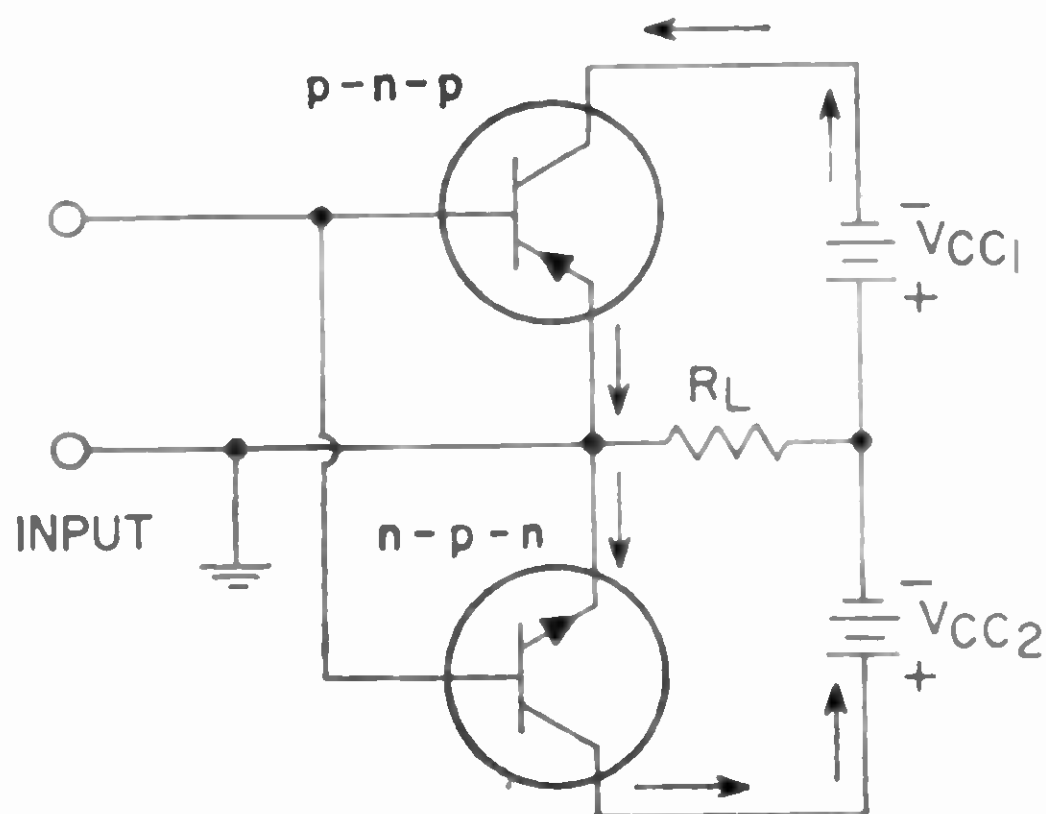


Fig. 139—Basic complementary-symmetry circuit.

tially no steady-state current flows through the load resistor R_L . Therefore, the voice coil of a loudspeaker can be connected directly in place of R_L without excessive speaker cone distortion.

The true complementary amplifier, shown in Fig. 140, is the simplest of all complementary circuits. Its features include a single

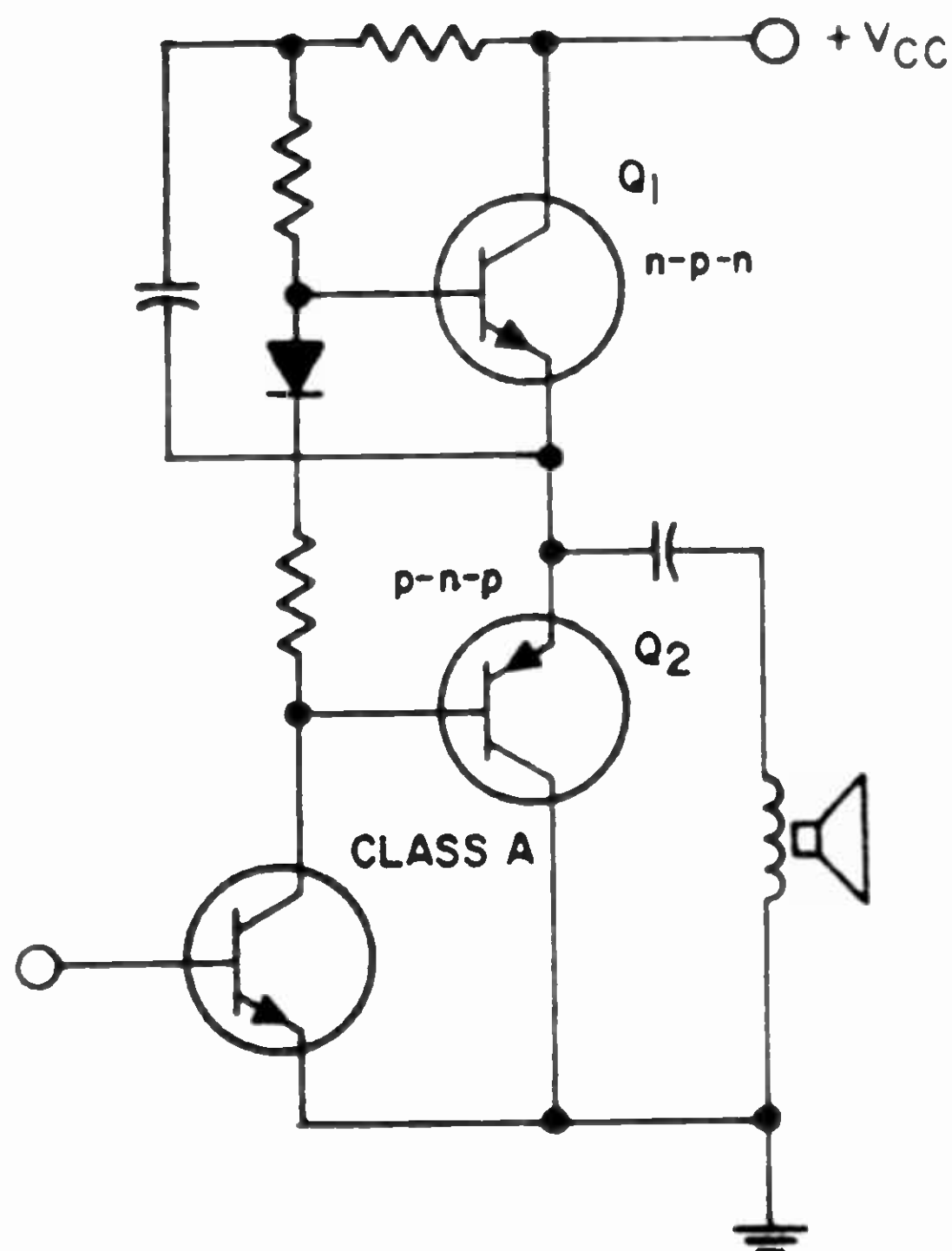


Fig. 140—True-complementary amplifier.

driven stage, a single diode for bias, and the application of turn-off drive to the output devices. Because it requires a class A driver and both p-n-p and n-p-n output devices and has high standby current, the true-complementary design is seldom used for power-output levels in excess of 25 watts rms.

The class A driver stage shown in Fig. 140 requires the use of a large heat sink. The p-n-p power device in the complementary output stage is more expensive and has lower safe-area ratings than its n-p-n equivalent. Because control of base diffusion is more difficult in p-n-p devices, these types are generally 25-per-cent costlier than comparable n-p-n types.

One way to avoid the high cost of power p-n-p transistors is to employ a quasi-complementary circuit such as that shown in Fig. 141. In this type of circuit, a low-current

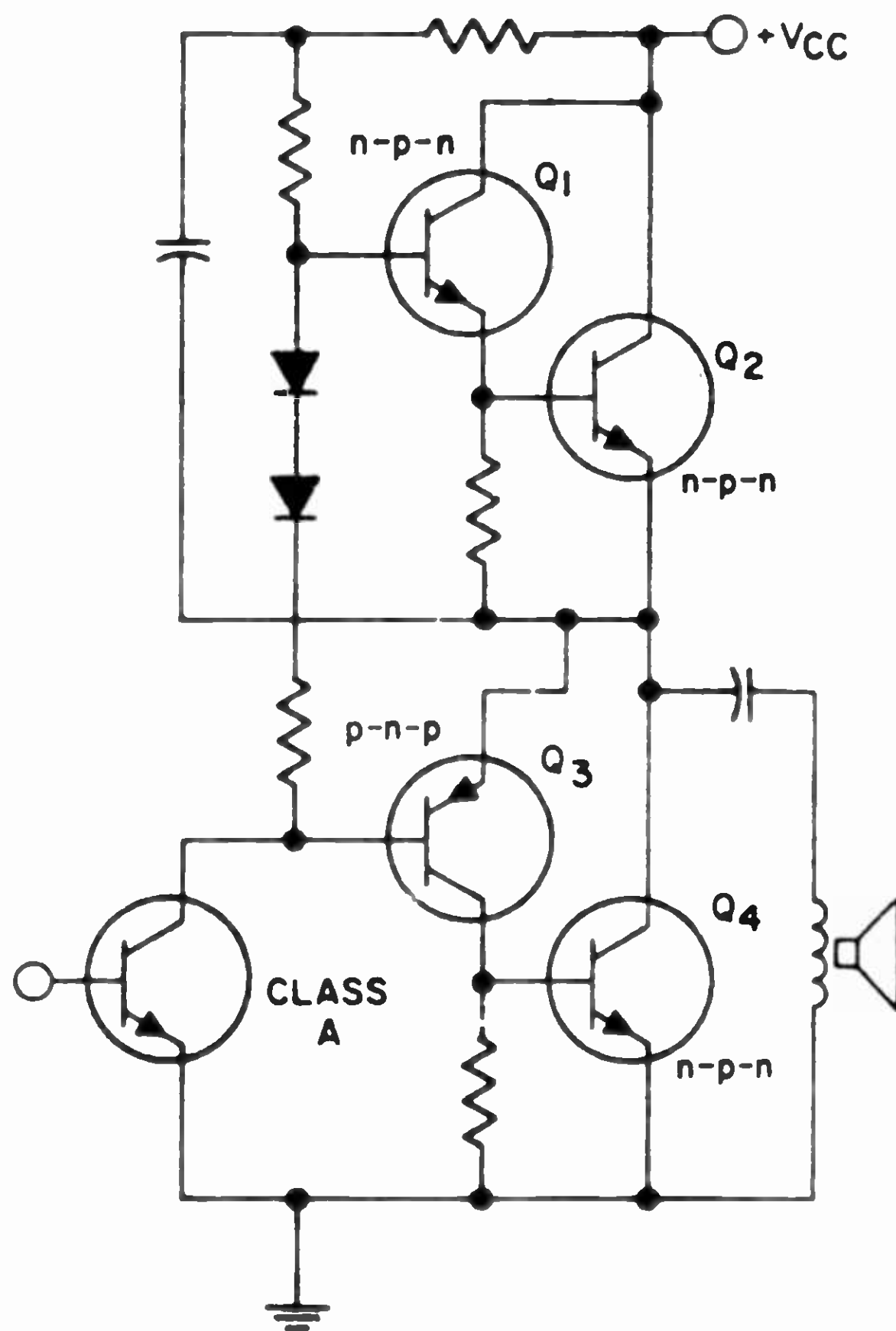


Fig. 141—Quasi-complementary amplifier.

p-n-p transistor is directly coupled to a high-current n-p-n transistor to simulate a high-current transistor, as shown in Fig. 142.

The advantages of quasi-complementary amplifiers include improved safe area for the n-p-n output transistor, lower cost, and the use of class B drivers. The major disadvantages are the need for two driver transistors and two bias diodes, and the absence of turn-off

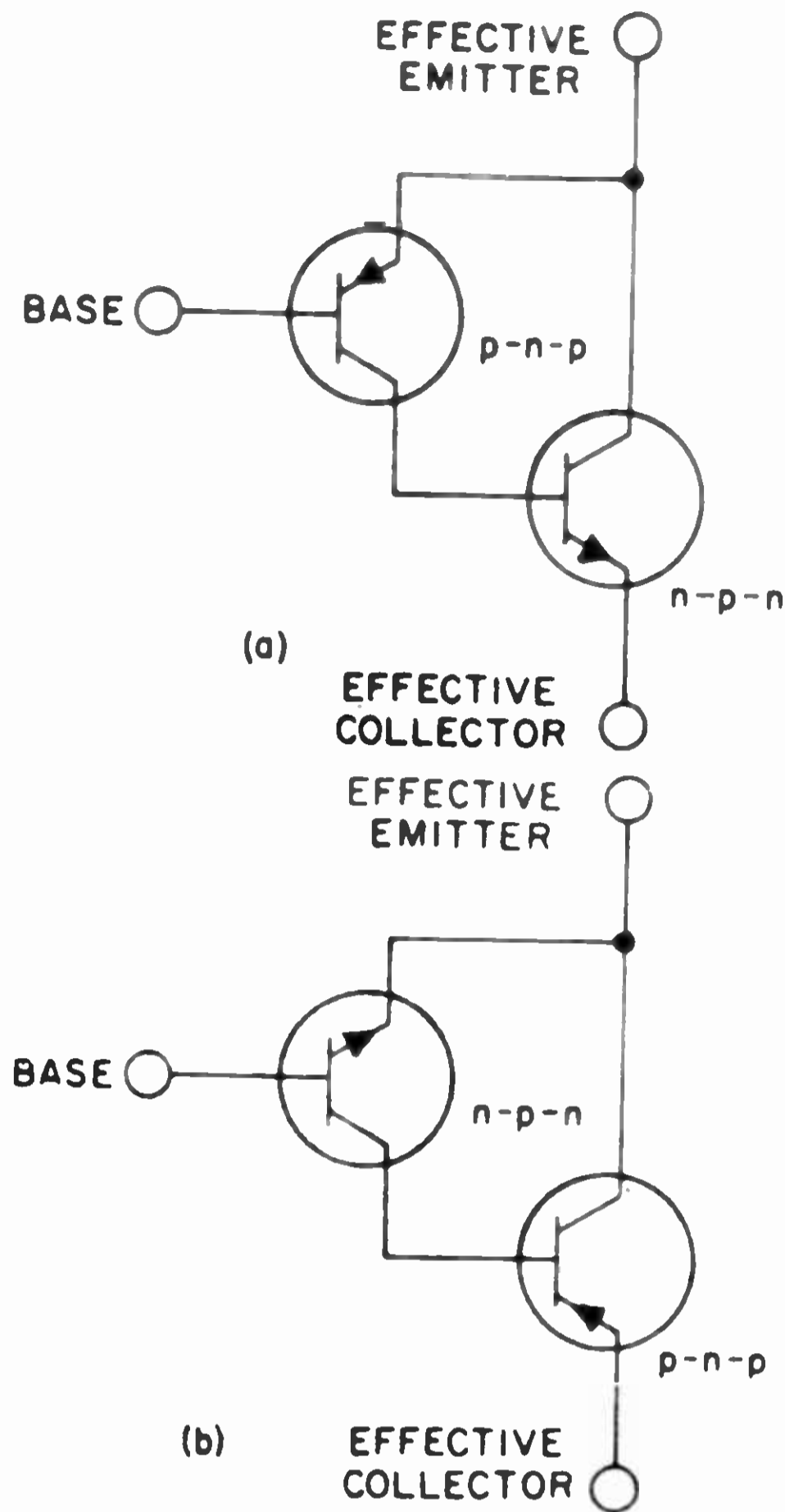


Fig. 142—Connection of two transistors to simulate a high-current transistor.

drive to the output transistors. Because the advantages far outweigh the disadvantages for high-power amplifiers, quasi-complementary circuits are generally used at power levels above 25 watts rms. The high-frequency response of such circuits can be improved by use of bleeder resistors in the base circuits of the output transistors.

In both true-complementary and quasi-complementary circuits, the output devices do not need to be well matched for beta. These circuits are essentially voltage amplifiers used in an emitter-follower configuration that has a voltage gain of nearly unity which varies only slightly with transistor beta. In the higher-power quasi-complementary amplifier, the effect of beta is even less important because a Darlington-connected stage is used. The basic requirement is that a minimum current gain be maintained from minimum to maximum drive.

Several high-fidelity amplifiers are shown in the Circuits section. The performance capabilities of such amplifiers are usually given in terms of frequency response, total harmonic distortion, maximum power output, and noise level. To provide high-fidelity reproduction of audio program material, an amplifier should have a frequency response which does not vary more than 1 dB over the entire audio spectrum. General practice is to design the amplifier so that its frequency response is flat within 1 dB from a frequency well below the lowest to be reproduced to one well above the upper limit of the audible region.

Harmonic distortion and intermodulation distortion produce changes in program material which may have adverse effects on the quality of the reproduced sound. Harmonic distortion causes a change in the character of an individual tone by the introduction of harmonics which were not originally present in the program material. For high-fidelity reproduction, total harmonic distortion (expressed as a percentage of the output power) should not be greater than about 0.5 per cent at the desired listening level.

Intermodulation distortion is a change in the waveform of an individual tone as a result of interaction with another tone present at the same time in the program material. This type of distortion not only alters the character of the modulated tone, but may also result in the generation of spurious signals at frequencies equal to the sum and difference of the interacting frequencies. Intermodulation distortion should be less than 2 per cent at the desired listening level. In general, any amplifier which has low intermodulation distortion will have very low harmonic distortion.

The maximum power output which a high-fidelity amplifier should deliver depends upon a complex relation of several factors, including the size and acoustical characteristics of the listening area, the desired listen-

ing level, and the efficiency of the loudspeaker system.

The noise level and maximum output power determine the range of volume the amplifier is able to reproduce, i.e., the difference (usually expressed in dB) between the loudest and softest sounds in program material. Because the greatest volume range utilized in electrical program material at the present time is about 60 dB, the noise level of a high-fidelity amplifier should be at least 60 dB below the signal level at the desired listening level.

The design of audio equipment for direct operation from the ac power line normally requires the use of either a power transformer or a large voltage-dropping resistor to reduce the 120-volt ac line voltage to a level that is appropriate for transistors. Both of these techniques have disadvantages. The use of a transformer adds cost to the system. The use of a dropping resistor places restrictions on the final packaging of the instrument because the resistor must dissipate power. In addition, low-voltage supplies are usually more expensive to filter than high-voltage supplies.

The use of high-voltage silicon transistors eliminates the need for either a power transformer or a high-power voltage-dropping resistor, and permits the use of economical circuits and components in **line-operated audio equipment**. Several ac/dc circuits using these high-voltage transistors are shown in the Circuits section. The basic class A audio output stage shown in Fig. 143 is essentially of the same design as the class A amplifier discussed previously. Because the supply voltage is much higher, however, the currents are about one-tenth as high and the impedances about 100 times as high.

The use of a voltage-dependent resistor (VDR) as a damping resistor across the primary winding of the output transformer in Fig. 143 protects the output circuit against the destructive effects of transient voltages that can occur under abnormal

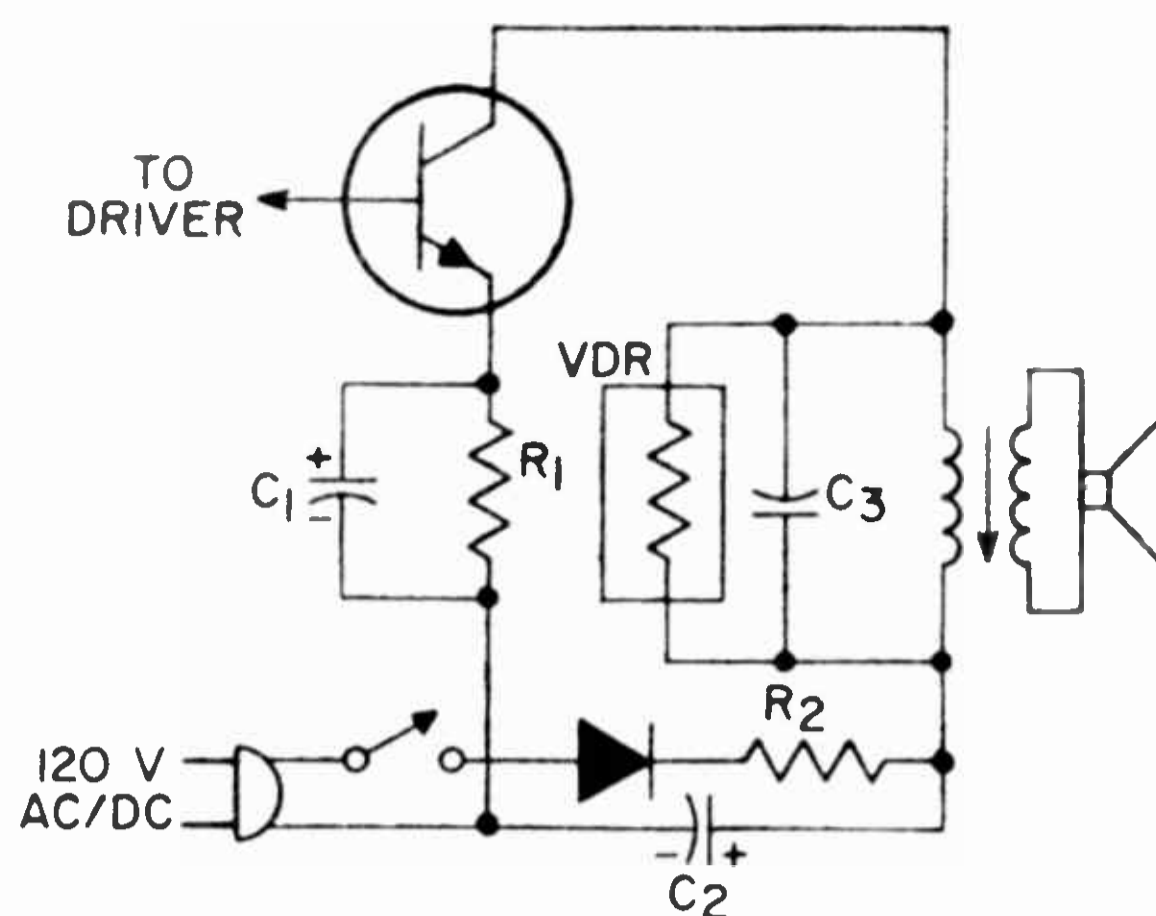


Fig. 143—Basic audio-output stage for line operated equipment.

conditions. If the VDR were not used the peak collector voltage under transient conditions could be as high as five to ten times the supply voltage, or far in excess of the breakdown-voltage rating for the transistor. Because the resistance of the VDR varies directly with voltage, its use limits the transient voltage to safe levels but does not degrade overall circuit performance.

Fig. 144 shows another effective method for protection against transient voltages. In this arrangement,

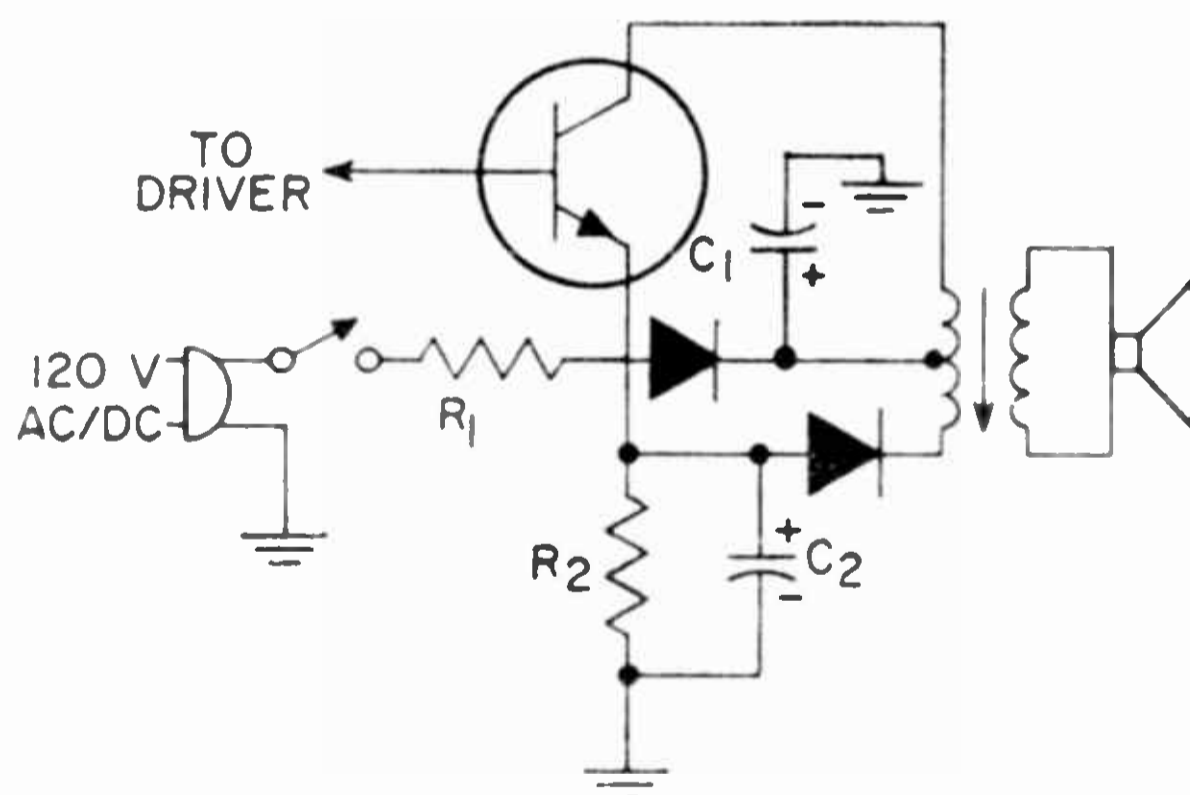


Fig. 144—Alternate method for protection against transient voltages.

the output transformer is replaced by a center-tapped transformer and a silicon rectifier that has a peak-reverse-voltage rating of 300 to 400 volts. The peak voltage across the output is thus limited to a value which does not exceed twice the magnitude of the supply voltage. As the collector voltage approaches a value equal to twice the supply voltage, the voltage at the diode end of the trans-

former becomes sufficiently negative to forward-bias the diode and thus clamp the collector voltage. The required transformer primary impedance is generally about 10,000 ohms center-tapped; in addition, it is recommended that a bifilar winding be used to minimize leakage inductance. Because the arrangement shown in Fig. 144 provides more reliable protection against transients than that of Fig. 143, a higher supply voltage and a higher transformer impedance can be used.

It should be noted that special precautions are required in the construction of circuits for line-voltage operation. Because these circuits operate at high ac and dc voltages, special care must be exercised to assure that no metallic part of the chassis or output transformer is exposed to touch, accidental or otherwise. The circuits should be installed in non-metallic cabinets, or should be properly insulated from metallic cabinets. Insulated knobs should be used for potentiometer shafts and switches.

A **phase inverter** is a type of class A amplifier used when two out-of-phase outputs are required. In the split-load phase-inverter stage shown in Fig. 145, the output current of transistor Q_1 flows through both the collector load resistor R_1 and the emitter load resistor R_3 . When the input signal is negative, the decreased output current causes the collector side of resistor R_1 to become more positive and the emitter side of resistor R_3 to become more negative with respect to ground. When the input signal is positive, the output current increases and opposite voltage polarities are established across resistors R_3 and R_1 . Thus, two output signals are pro-

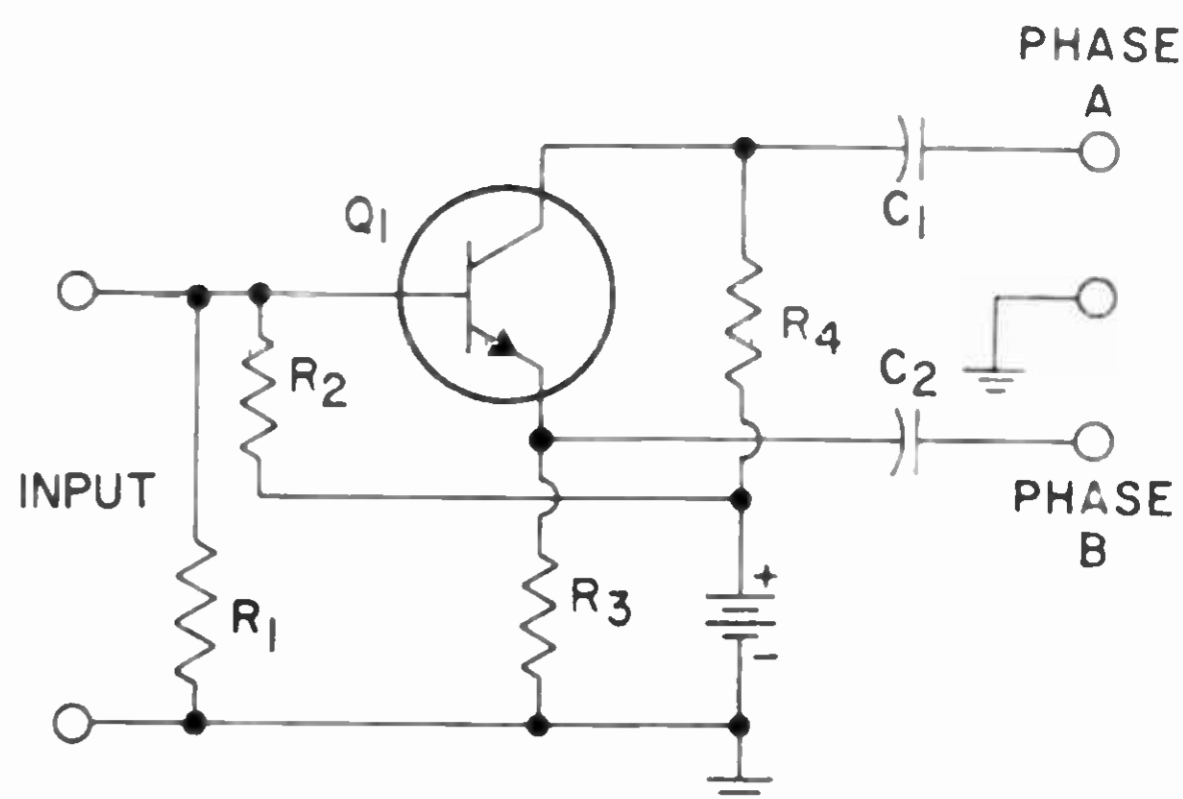


Fig. 145—Split-load phase-inverter stage.

duced which are 180 degrees out of phase with each other. This circuit provides the 180-degree phase relationship only when each load is resistive and constant throughout the entire signal swing. It is not suitable as a driver stage for a class B output stage.

Direct-Coupled Amplifiers

Direct-coupled amplifiers are normally used in transistor circuits to amplify small dc or very-low-frequency ac signals; they can amplify signals having a frequency of zero hertz. The upper frequency limit of such an amplifier may range from a few hundred hertz in general-purpose electrometer applications to several megahertz in other applications. In general, dc amplifiers are used to amplify the output of transducers which produce quantitative information relative to heat, vibration, pressure, speed, and distance. Other applications include the output stages of series-type and shunt-type regulating circuits, chopper-type circuits, differential amplifiers, and pulse amplifiers.

Direct-coupled amplifiers are also used in **chopper-type** circuits to amplify low-level dc signals, as illustrated by the block diagram in Fig. 146. The dc signal modulates an ac

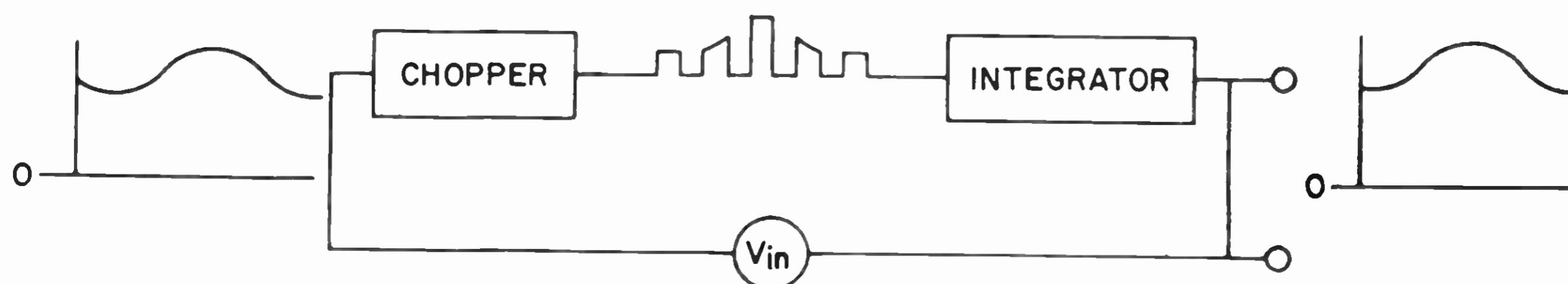


Fig. 146—Block diagram showing action of "chopper" circuit.

carrier wave, usually a square wave, and the modulated wave is then amplified to a convenient level. The series of amplified pulses can then be detected and integrated into the desired dc output signal.

Chopper amplifiers consist of three basic sections. The first section converts the low-level input signal into a modulated ac signal, the second section amplifies this ac signal, and the third section demodulates the amplified signal.

The first section of a chopper amplifier is fundamentally a continuously operated ON-OFF switch. Ideally, this switch would have zero ON resistance, infinite OFF resistance, zero shunt capacitance, and zero switching time. It would also require no driving power and have infinite life. In actual practice, it is possible to achieve satisfactory performance with a switch that does not have these ideal characteristics.

The two basic circuit configurations for chopping are the series chopper and the shunt chopper. The shunt chopper is the more popular of the two because it can be capacitively coupled to an ac amplifier without the need for either a choke or a transformer. The series chopper has the disadvantage that it requires a dc return path for the input current. This path can be provided by an additional resistor at the expense of over-all circuit efficiency.

The basic series chopper circuit using an MOS transistor is shown in Fig. 147. This circuit has the characteristics of a simple L-pad attenuator in which the transistor is the variable series resistor. In the

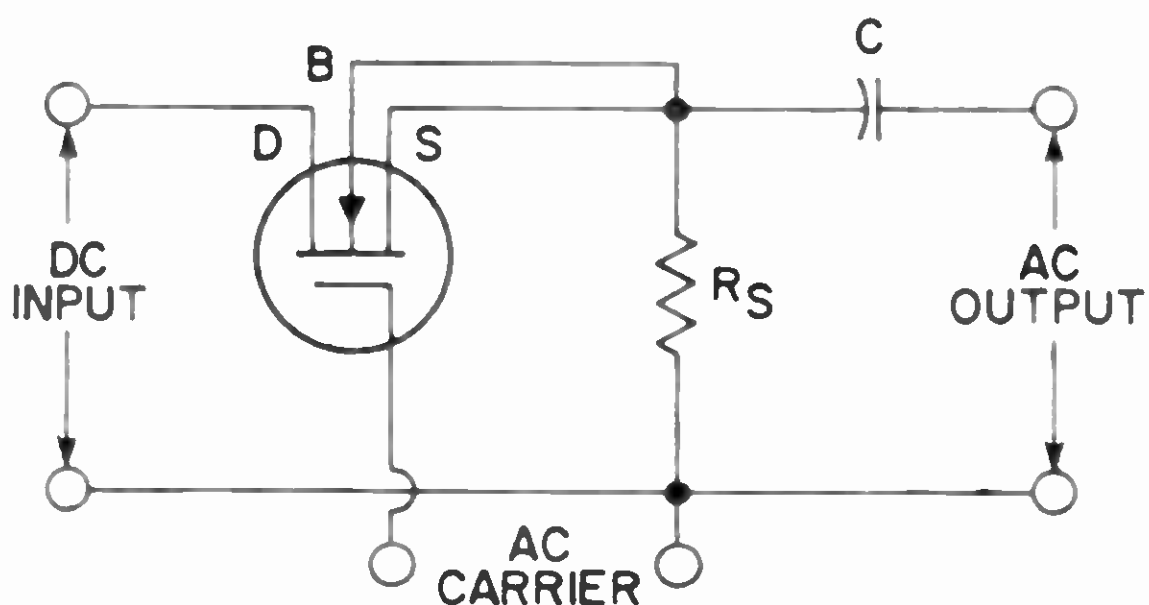


Fig. 147—Basic series chopper circuit using an MOS transistor.

ON condition, the value of the dc return resistance R_S must be large compared to the load resistance R_L to minimize resistive losses; R_L , in turn, must be large compared to the intrinsic drain resistance $r_d(\text{ON})$ so that the voltage V_L across the load approaches the value of the dc input voltage V_G . In the OFF condition, the dc return resistance R_S must be small compared to $r_d(\text{OFF})$. Because of these restrictions, the series chopper is seldom used except when the fixed resistance R_S can be made variable by replacing it with a shunt chopper arranged to be OFF when the series chopper is ON, and vice versa.

Fig. 148 shows a shunt chopper circuit using an MOS transistor. In

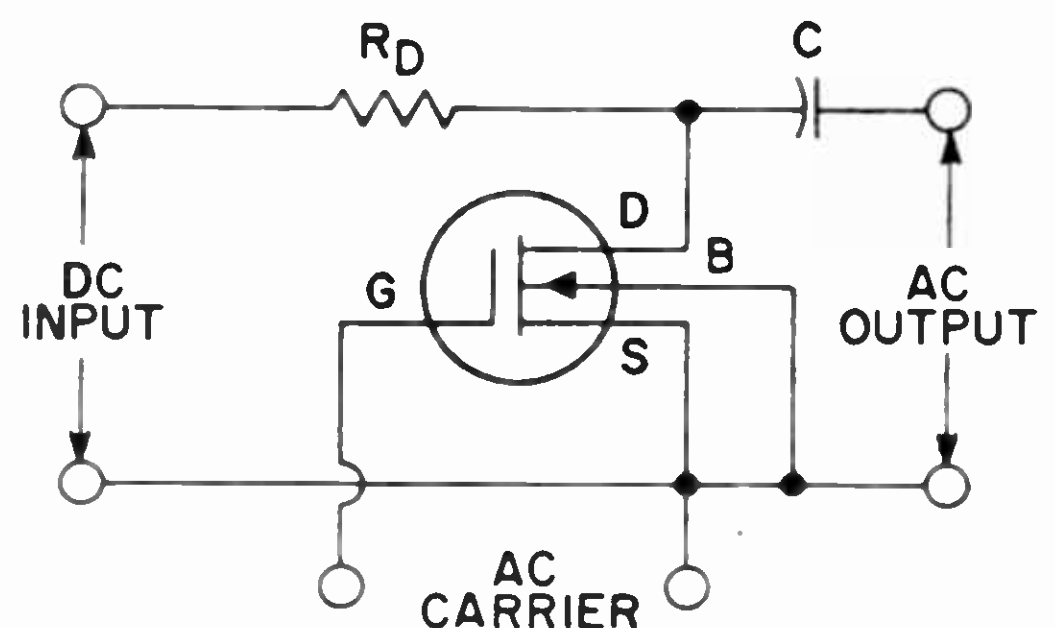


Fig. 148—Basic shunt chopper circuit using an MOS transistor.

this circuit, the intrinsic drain resistance r_d of the transistor must be small compared to the load resistance R_L in the ON condition, but must be large compared to the fixed series resistance R_D in the OFF condition. The requirement for $r_d(\text{ON})$ to have a very small value is minimized if R_L is the high input impedance of an MOS transistor amplifier stage. Because of their high ON-to-OFF resistance ratio, negligible gate-leakage currents, and low feedthrough capacitance, MOS transistors considerably improve the level of solid-state chopper performance.

Differential amplifiers can be used to provide voltage regulation, or to compensate for fluctuations in current due to signal, component, or temperature variations. Typical differential-amplifier circuits, such as

those shown in Fig. 149, may also include an output stage which supplies current to the load resistor R , and the necessary number of direct-

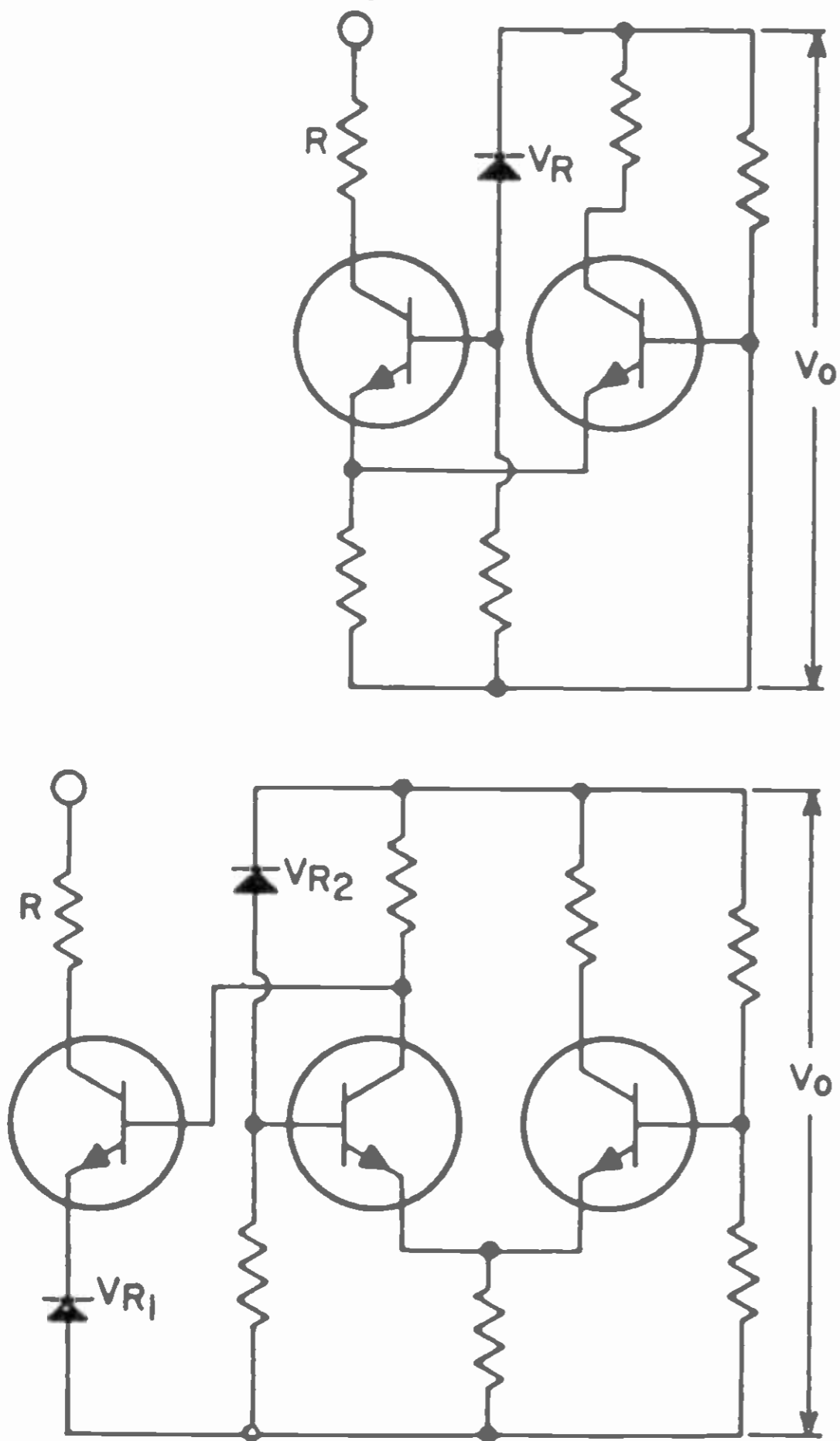


Fig. 149—Typical differential-amplifier circuits.

coupled cascaded stages to provide the required amount of gain for a given condition of line-voltage or load-current regulation. The reference-voltage source V_R is placed in one of the cascaded stages in such a manner that an error or difference signal between V_R and some portion of the output voltage V_o is developed and amplified. Some form of temperature compensation is usually included to insure stability of the direct-coupled amplifier.

MOS-transistor dc amplifiers may take several different forms, including single-ended input to single-ended output, differential input to single-ended output, and differential input to differential output. Normally dc amplifiers require direct coupling of all stages (no coupling capacitors). In some versions of dc amplifiers, this requirement is circumvented by

conversion of the low- or zero-frequency input signal into a modulated ac signal, amplification of this signal by means of capacitor-coupled stages, and then demodulation of the amplified signal to restore it to the original dc form. The necessary modulation may be accomplished by a number of different techniques, including electrically actuated mechanical switches, electronic switches, photo-optical switches, magnetic modulators, and diode bridge modulators. Input devices which function as switches are generally referred to as "choppers" because, as described above, they divide the input signal into segments in the form of square waves or pulses having an amplitude proportional to the amplitude of the input signal.

Single-ended dc amplifiers which do not employ "choppers" have a continuous ohmic current path between the input and the output as the result of direct coupling of all stages (i.e., the omission of all capacitive or inductive forms of coupling). In this configuration, the steady-state voltage at the output of one stage appears at the input of the next stage. In a typical cascade arrangement using MOS field-effect transistors, the signal progresses from the drain of the first unit to the gate of the next and so on to the last stage, as shown in Fig. 150.

In general, the ideal MOS transistor for use in a single-ended dc amplifier circuit has an optimum zero-signal operating point which is obtained at a gate voltage having the same magnitude as the optimum drain voltage and also the same polarity. Because enhancement-type MOS transistors automatically meet the latter requirement and can be designed to meet the former requirement, they are generally the logical choice for most direct-coupled circuits. If other device considerations (such as gain, input impedance, temperature coefficient, or noise) require the use of depletion-type transistors, such transistors can be

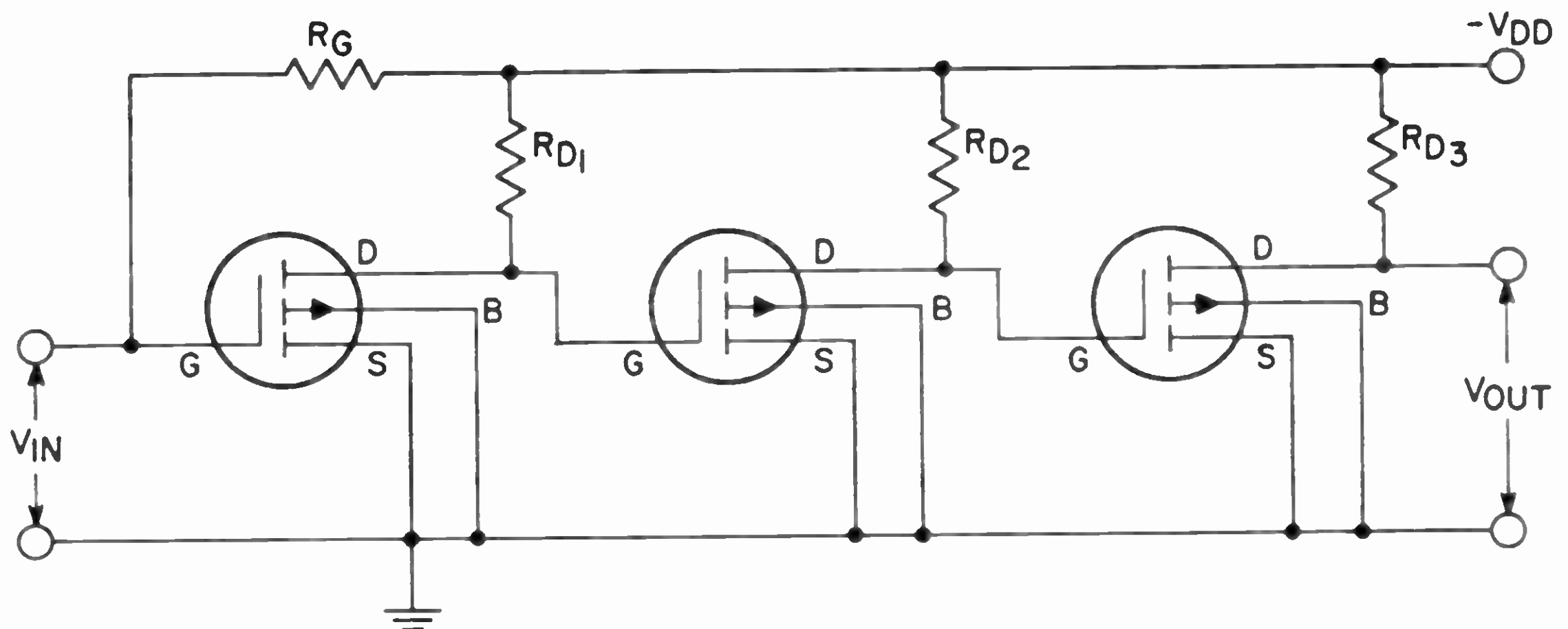


Fig. 150—Typical single-ended dc amplifier using p-channel enhancement-type MOS transistors.

direct-coupled by the use of level shifting, as shown in Fig. 151. In this circuit configuration, the source terminal is generally placed at a potential equal to or greater than the drain-to-source voltage of the preceding stage. In the arrangement of Fig. 151, the gate is at a net zero voltage or is reverse-biased relative to the source.

Although MOS transistors are not optimized for direct-coupled applications, they can be used in such circuits because they have low gate leakage current (typically fractions of a picoampere), total input capacitance of about 5 picofarads, and an appreciable value of forward transconductance. In addition, tight production control limits the spread of drain current between individual transistors to a variation of approximately two to one for a high degree of interchangeability.

For a fixed value of supply voltage, there are only three ways to increase the stage voltage gain A in a single-ended amplifier: (1) use of a transistor having a higher ratio of gate-to-drain forward transconductance g_{fs} to drain current I_D ; (2) use of a higher value of load resistance R_L (if R_L is less than the common-source output resistance r_{os}); and (3) use of a transistor having a higher value of r_{os} . The load resistance R_L can only be increased to the point where the product of I_D and R_L is equal to approximately one-half the supply voltage. In general, the ratio of transconductance to drain current increases as drain current is decreased by negative gate bias. As a result, the stage voltage gain may be increased and power consumption decreased at the same time.

The increased voltage gain of an MOS transistor at reduced values of

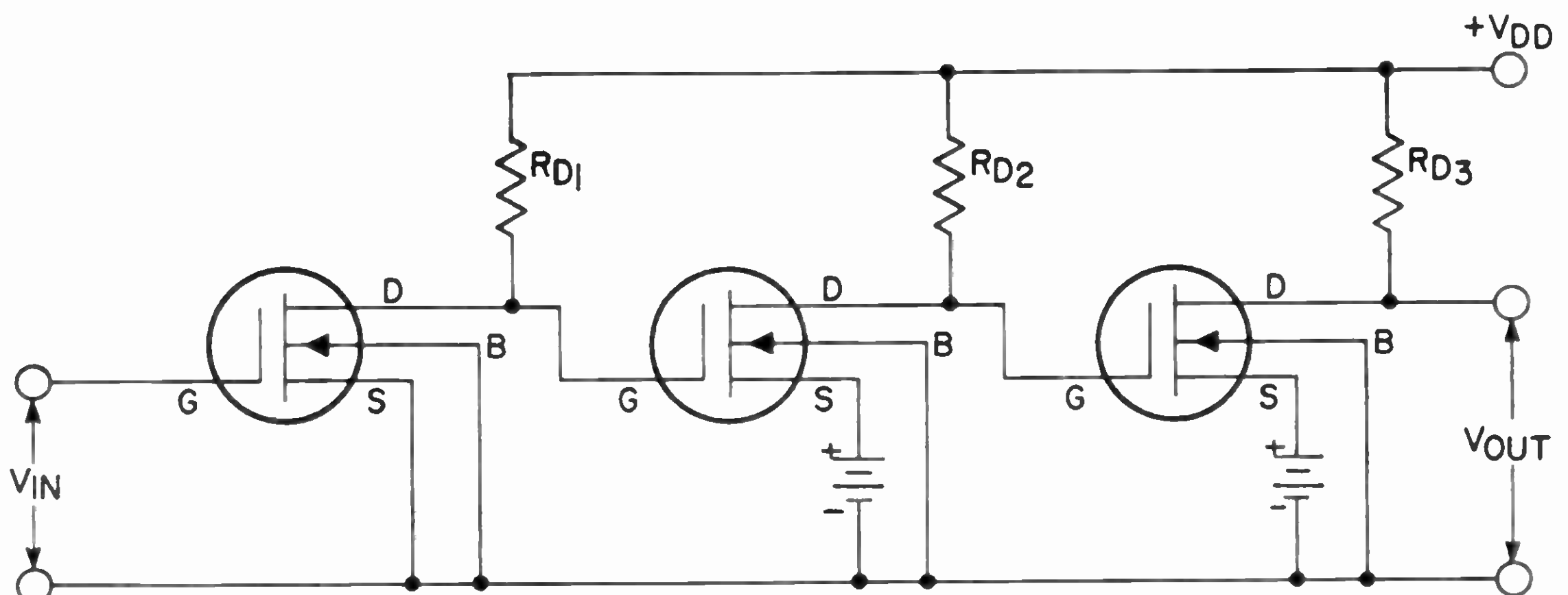


Fig. 151—DC amplifier circuit in which n-channel depletion-type MOS transistors are direct-coupled by use of level shifting.

drain current may be accompanied by a relatively large drift in the operating point if there are wide excursions in ambient temperature. Many field-effect transistors have a point on their forward-transfer characteristic which is relatively insensitive to temperature variations. If this point does not coincide with the operating point which provides the desired voltage gain, a design compromise is required. As shown in Fig. 152, the zero-temperature-coefficient point may be identified by measurement of the forward-transfer characteristic at different ambient temperatures.

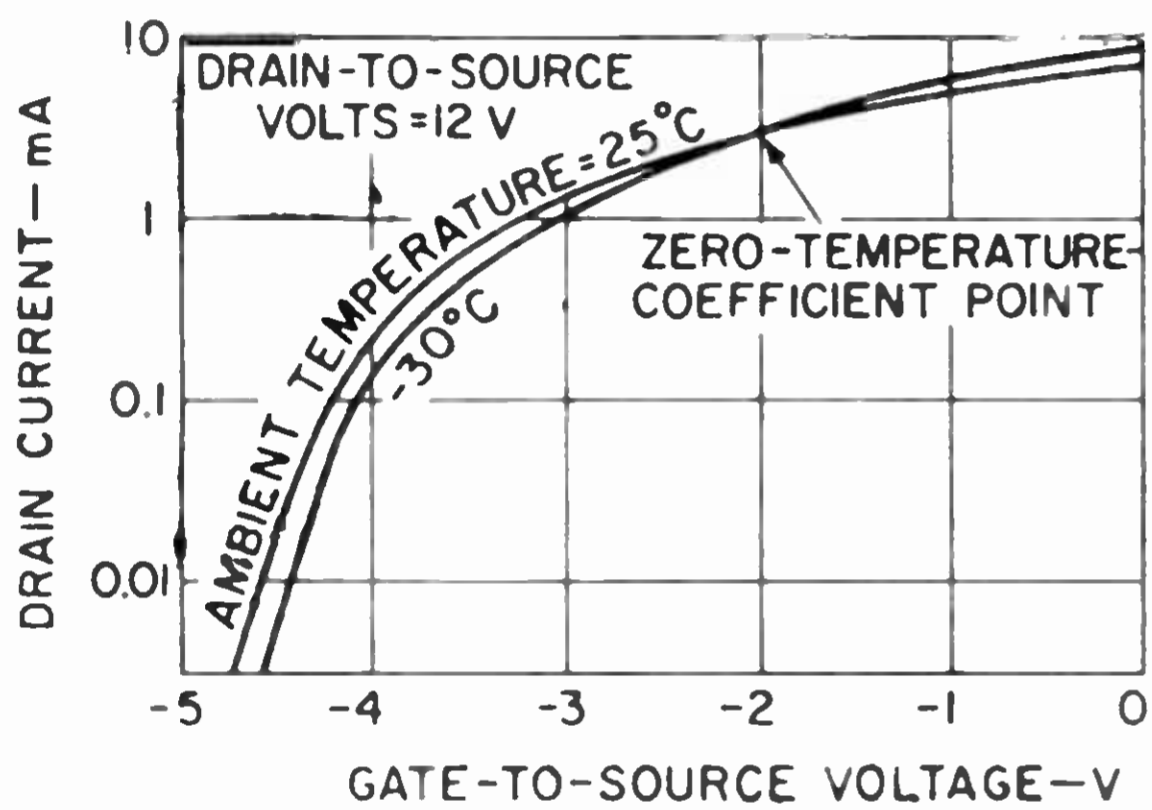


Fig. 152—Forward-transfer characteristics of MOS transistor at 25°C and -30°C.

Voltage-Controlled Attenuators

Because the drain current-voltage characteristic of MOS transistors remains linear at low drain-to-source voltages, these devices can be used as low-distortion voltage-controlled attenuators. The principal advantages of MOS transistors in this application are negligible gate-power requirements and large dynamic range.

Fig. 153 shows drain resistance as a function of gate-to-source voltage for a typical n-channel depletion-type insulated-gate transistor. Transistors having higher pinch-off voltages accept correspondingly greater peak signal-voltage swings before wave-shape distortion occurs. However, the higher-pinch-off-voltage transistors require higher gate-voltage excursions to cover the resistance range from minimum to

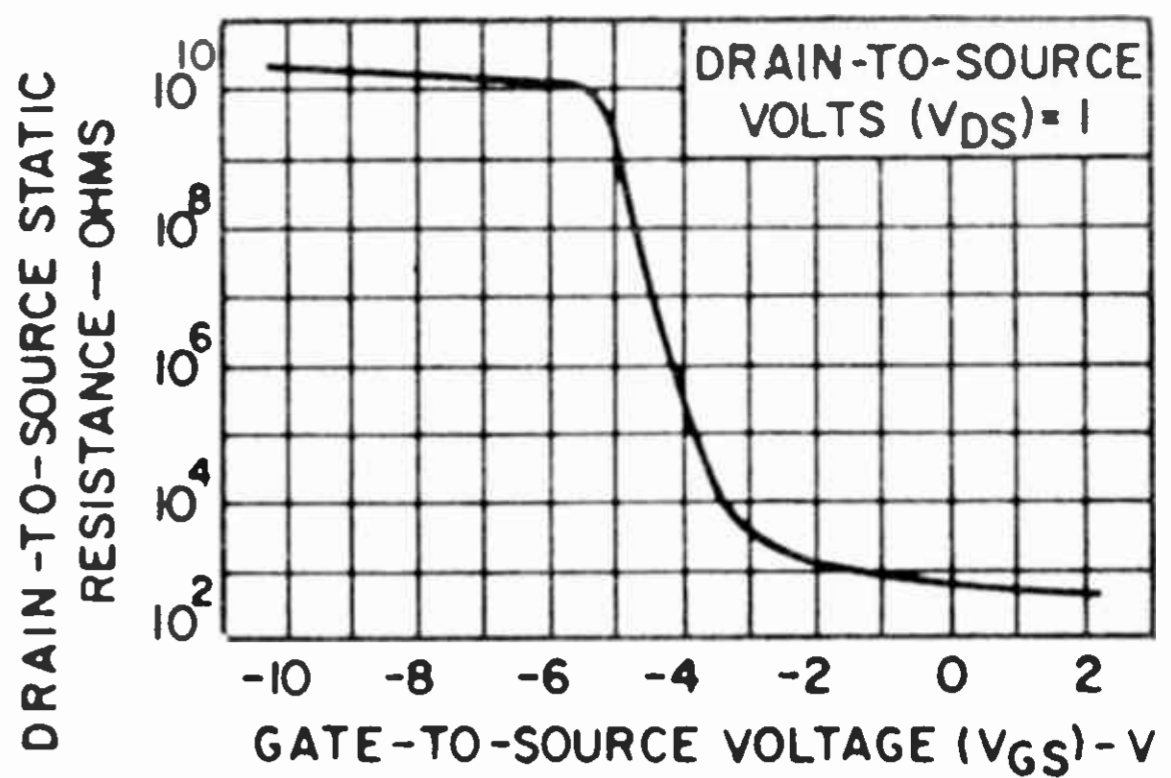


Fig. 153—Drain resistance as a function of gate voltage for typical n-channel depletion-type MOS transistor.

maximum. A typical n-channel MOS transistor produces total harmonic distortion of less than two per cent in a 100-millivolt 400-Hz sine wave. Fig. 154 shows an attenuator circuit using an MOS transistor and the output signal of the circuit as a function of gate-to-source voltage.

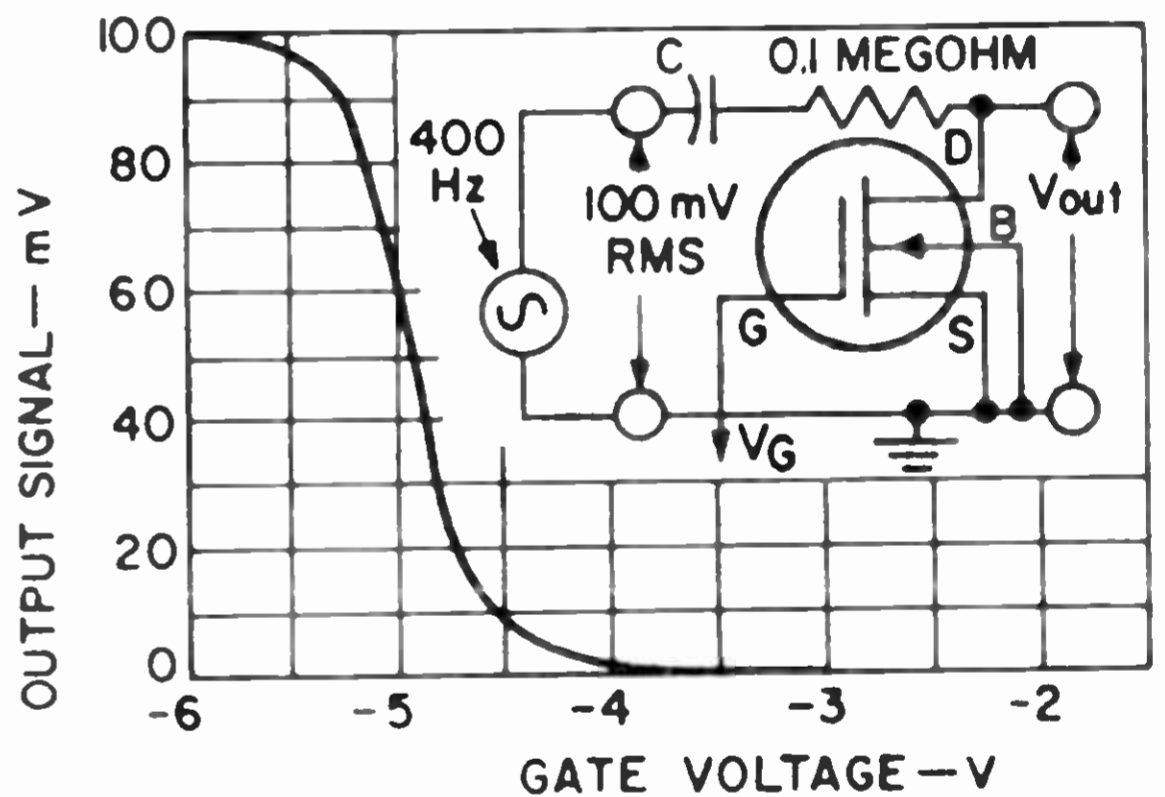


Fig. 154—Output signal as a function of gate voltage for MOS transistor in circuit shown.

Figs. 155 to 157 show several possible attenuator circuit configurations which use MOS transistors as voltage-variable resistors. The circuit in Fig. 155 is desirable for use

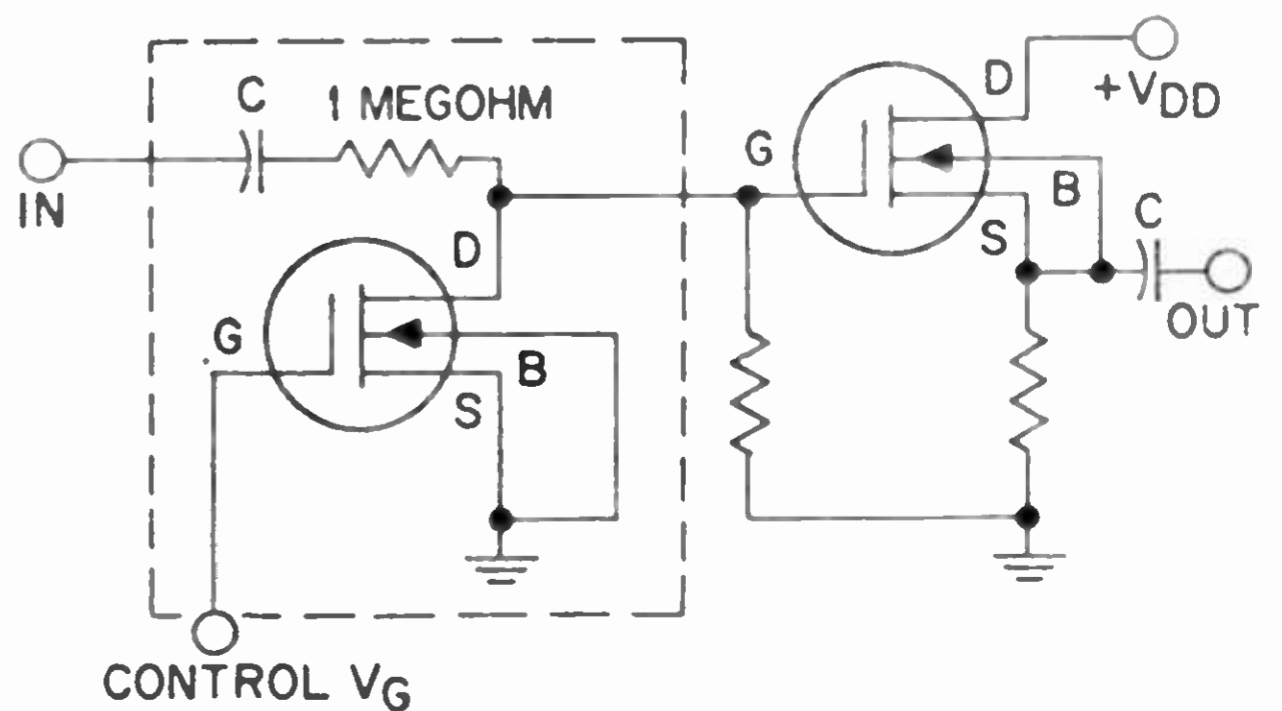


Fig. 155—Attenuator circuit in which MOS transistor serves as variable-resistive element in low side.

at high signal levels because at such levels the thermal noise of the one-megohm series resistor does not degrade the signal-to-noise ratio of the system to an objectionable degree. This circuit is a simple L-pad configuration in which the transistor serves as the variable-resistive element in the low side of the attenuator. The maximum attenuation obtainable is generally between 60 and 70 dB; minimum attenuation is 1 to 2 dB. This circuit must be followed by a high-impedance load such as a common-source amplifier stage.

The circuit shown in Fig. 156 is the inverse of that in Fig. 155; i.e., the transistor serves as the variable-resistive element in the high side of the attenuator. Maximum attenuation in this circuit is also between 60 and 70 dB; minimum attenuation is between 1 and 6 dB. This circuit is

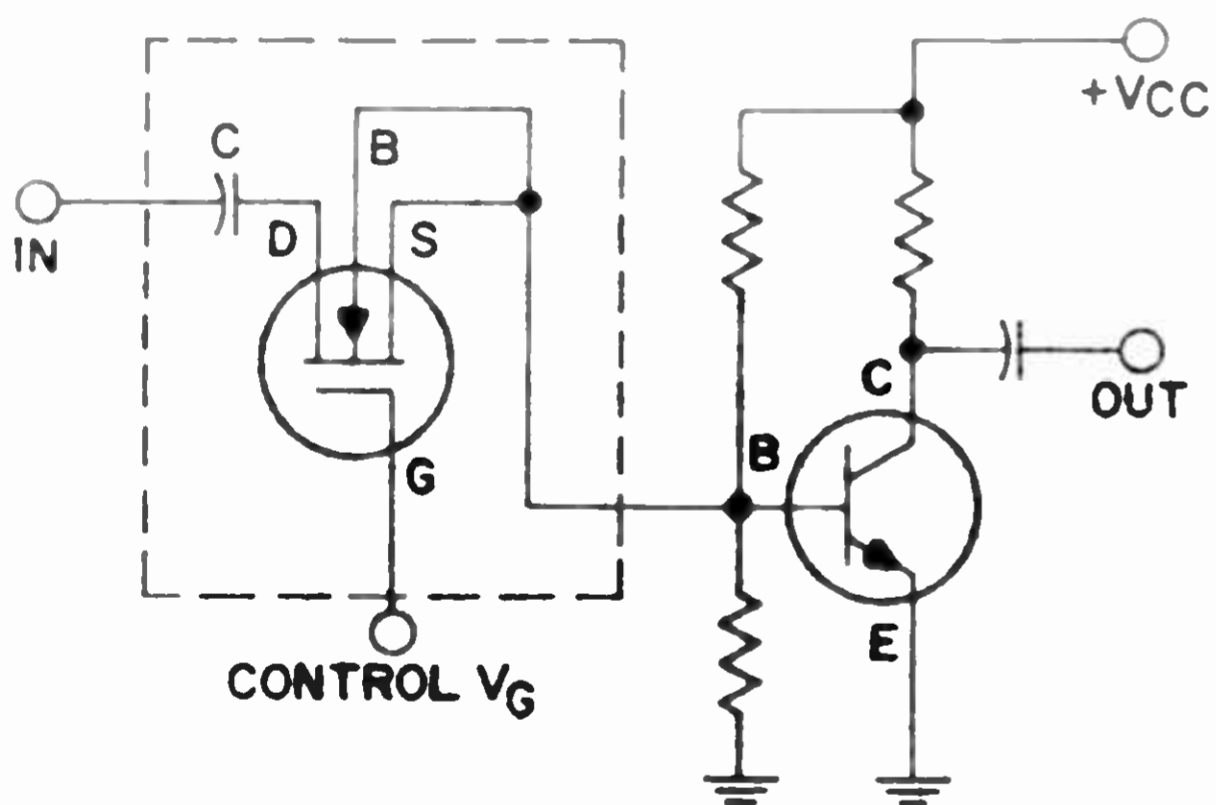


Fig. 156—Attenuator circuit in which MOS transistor serves as variable-resistive element in high side.

usually followed by a low-impedance load such as a common-emitter bipolar transistor amplifier stage.

Fig. 157 shows a method which controls both arms of an L-pad attenuator simultaneously. In this circuit, a p-channel enhancement-type MOS transistor is used in the upper arm and an n-channel depletion-type MOS transistor is used in the lower arm. When negative voltage is applied to the gates, the resistance of the n-channel unit increases at the same time that the resistance of the p-channel unit decreases. When the gate control is at zero volts, the drain resistance of Q_2 is about 500

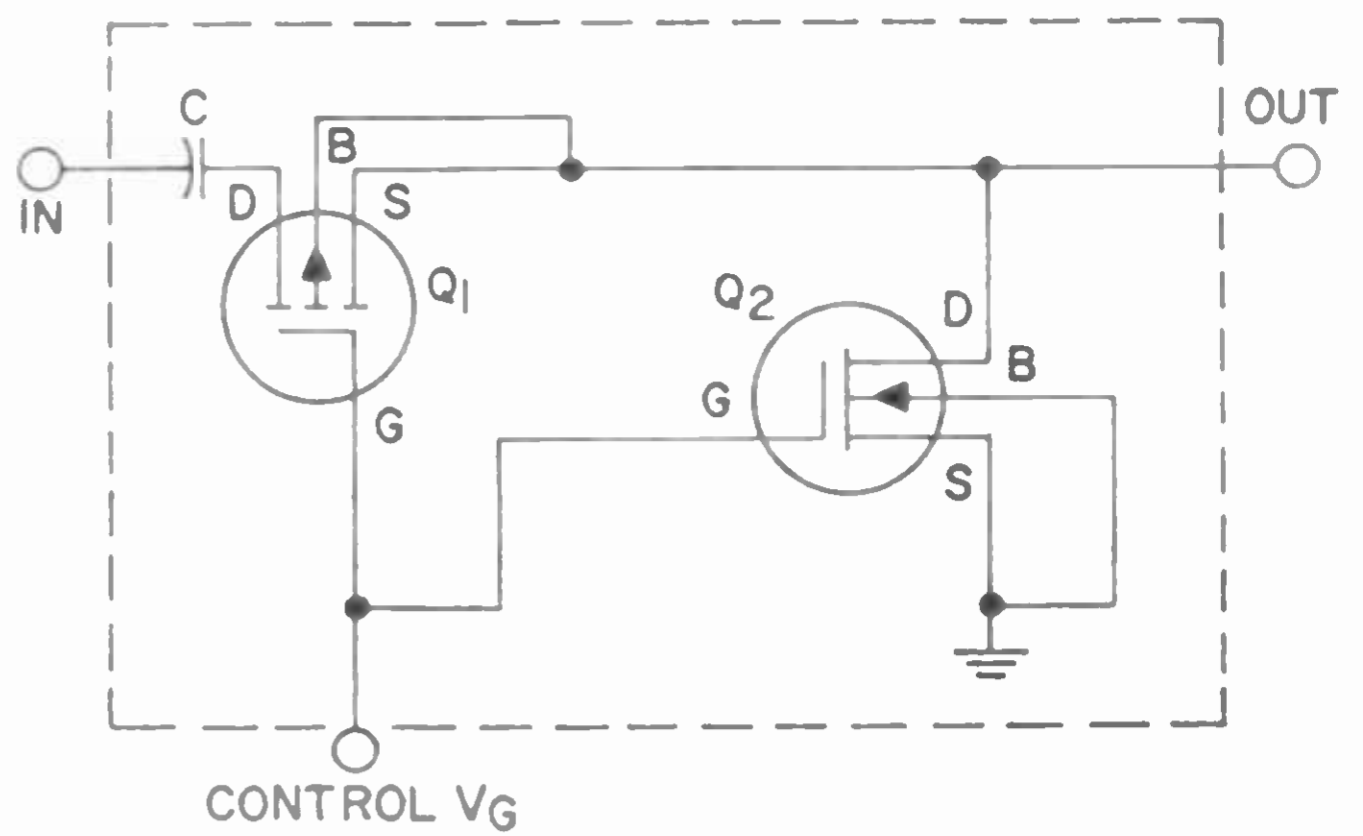


Fig. 157—L-pad attenuator circuit using two MOS transistors.

ohms and that of Q_1 is about 10 megohms. Under these conditions, a maximum attenuation of approximately 86 dB is obtained. When the gate control is at -6 volts, the drain resistance of Q_2 is about 10 megohms and that of Q_1 is about 500 ohms. Under these conditions, the attenuation is essentially zero. This circuit must work into a high-impedance load.

The following design considerations are important for effective use of MOS field-effect transistors as linear attenuators:

(a) The gate(s) must be adequately decoupled to prevent the introduction of unwanted signals.

(b) The transistor attenuator must be inserted at a point in the system where the signal level is as high as the transistor can accept without excessive distortion.

(c) In ac systems, the direct-current flow through the transistor must be minimized by the use of suitable blocking capacitors.

(d) In ac systems, proper layout must be used to minimize stray shunt capacitance.

(e) In ac systems, the effects of the capacitive elements of the transistor must be considered.

Tuned Amplifiers

In radio-frequency (rf) and intermediate-frequency (if) amplifiers, the bandwidth of frequencies to be amplified is usually only a small percentage of the center frequency. Tuned amplifiers are used

in these applications to select the desired bandwidth of frequencies and to suppress unwanted frequencies. The selectivity of the amplifier is obtained by means of tuned interstage coupling networks.

The properties of tuned amplifiers depend upon the characteristics of resonant circuits. A simple parallel resonant circuit (sometimes called a "tank" because it stores energy) is shown in Fig. 158. For practical purposes, the resonant frequency of such a circuit may be considered independent of the resistance R , provided R is small compared to the inductive reactance X_L . The resonant frequency f_r is then given by

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

For any given resonant frequency, the product of L and C is a constant; at low frequencies LC is large; at high frequencies it is small.

The Q (selectivity) of a parallel resonant circuit alone is the ratio of

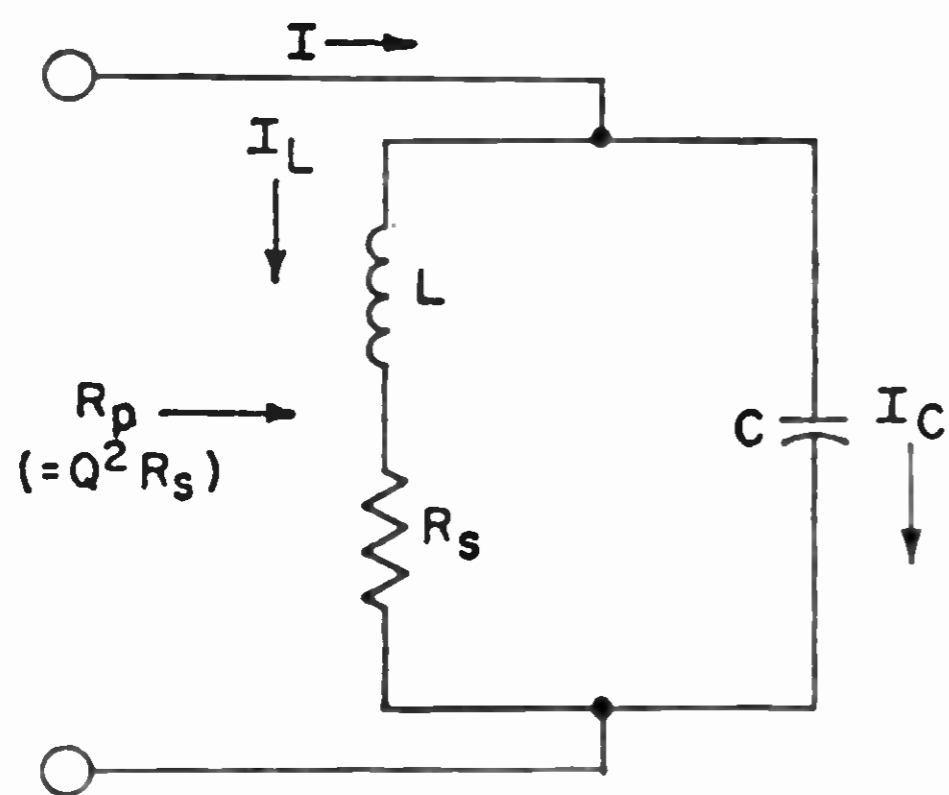


Fig. 158—Simple parallel resonant circuit.

the current in the tank (I_L or I_C) to the current in the line (I). This unloaded Q , or Q_0 , may be expressed in various ways, for example:

$$Q_0 = \frac{I_C}{I} = \frac{X_L}{R_s} = \frac{R_p}{X_C}$$

where X_L is the inductive reactance ($= 2\pi fL$), X_C is the capacitive reactance ($= 1/[2\pi fC]$), and R_p is the total impedance of the parallel resonant circuit (tank) at resonance. The Q varies inversely with the resistance of the inductor R_s . The lower the resistance, the higher the Q and the

greater the difference between the tank impedance at frequencies off resonance compared to the tank impedance at the resonant frequency.

The Q of a tuned interstage coupling network also depends upon the impedances of the preceding and following stages. The output impedance of a transistor can be considered as consisting of a resistance R_o in parallel with a capacitance C_o , as shown in Fig. 159. Similarly, the input impedance can be considered as consisting of a resistance R_i in parallel with a capacitance C_i . Because the

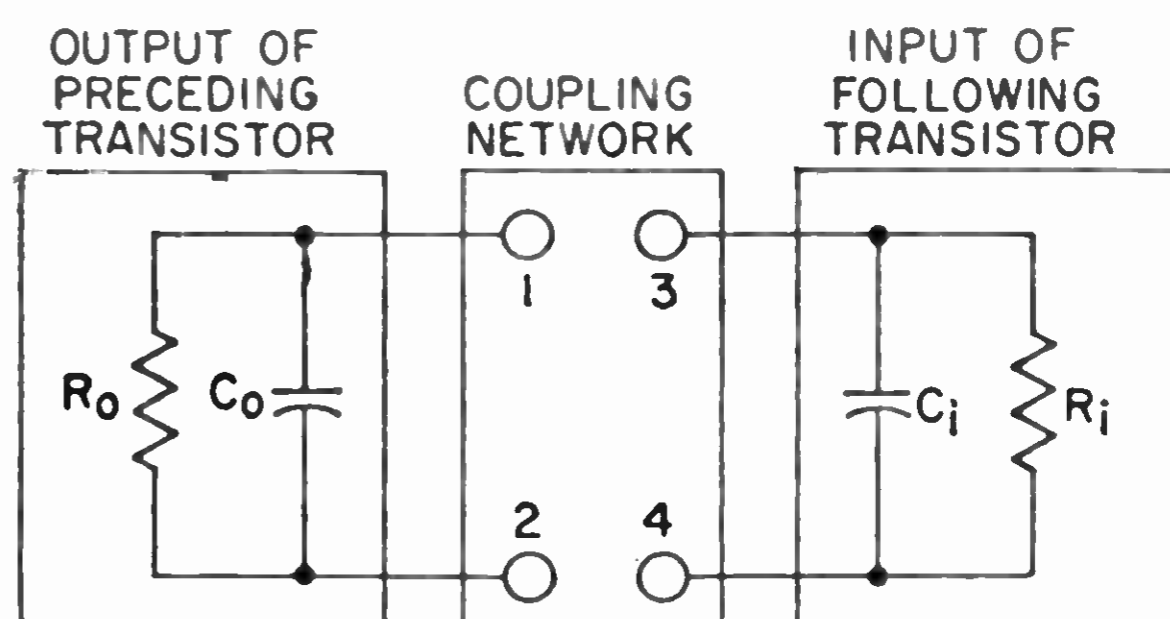


Fig. 159—Equivalent output and input circuits of transistors connected by a coupling network.

tuned circuit is shunted by both the output impedance of the preceding transistor and the input impedance of the following transistor, the effective selectivity of the circuit is the loaded Q (or Q_L) based upon the total impedance of the coupled network, as follows:

$$Q_L = \frac{\left\{ \begin{array}{l} \text{total loading on} \\ \text{coil at resonance} \end{array} \right\}}{X_L \text{ or } X_C}$$

The capacitances C_o and C_i in Fig. 159 are usually considered as part of the coupling network. For example, if the required capacitance between terminals 1 and 2 of the coupling network is calculated to be 500 picofarads and the value of C_o is 10 picofarads, a capacitor of 490 picofarads is used between terminals 1 and 2 so that the total capacitance is 500 picofarads. The same method is used to allow for the capacitance C_i at terminals 3 and 4.

When a tuned resonant circuit in the primary winding of a trans-

former is coupled to the nonresonant secondary winding of the transformer, as shown in Fig. 160(a), the effect of the input impedance of the following stage on the Q of the tuned circuit can be determined by considering the values reflected (or referred) to the primary circuit by transformer action. The reflected resistance r_i is equal to the resistance R_i in the secondary circuit times the square of the effective turns ratio between the primary and secondary windings of the transformer T :

$$r_i = R_i (N_1/N_2)^2$$

where N_1/N_2 represents the electrical turns ratio between the primary winding and the secondary winding of T . If there is capacitance in the secondary circuit (C_s), it is reflected to the primary circuit as a capacitance C_{sp} , and is given by

$$C_{sp} = C_p \div (N_1/N_2)^2$$

The loaded Q , or Q_L , is then calculated on the basis of the inductance L_p , the total shunt resistance (R_o plus r_i plus the tuned-circuit impedance $Z_t = Q_o X_c = Q_o X_L$), and the total capacitance ($C_p + C_{sp}$) in the tuned circuit.

Fig. 160(b) shows a coupling network which consists of a single-tuned circuit using mutual inductive coupling. The capacitance C_t includes the effects of both the output capacitance of the preceding transistor and the input capacitance of the following transistor (referred to the primary of transformer T_1). The bandwidth of a single-tuned transformer is determined by the half-power points on the resonance curve (-3 dB or 0.707 down from the maximum). Under these conditions, the band pass Δf is equal to the ratio of the center or resonant frequency f_r divided by the loaded (effective) Q of the circuit, as follows:

$$\Delta f = f_r/Q_L$$

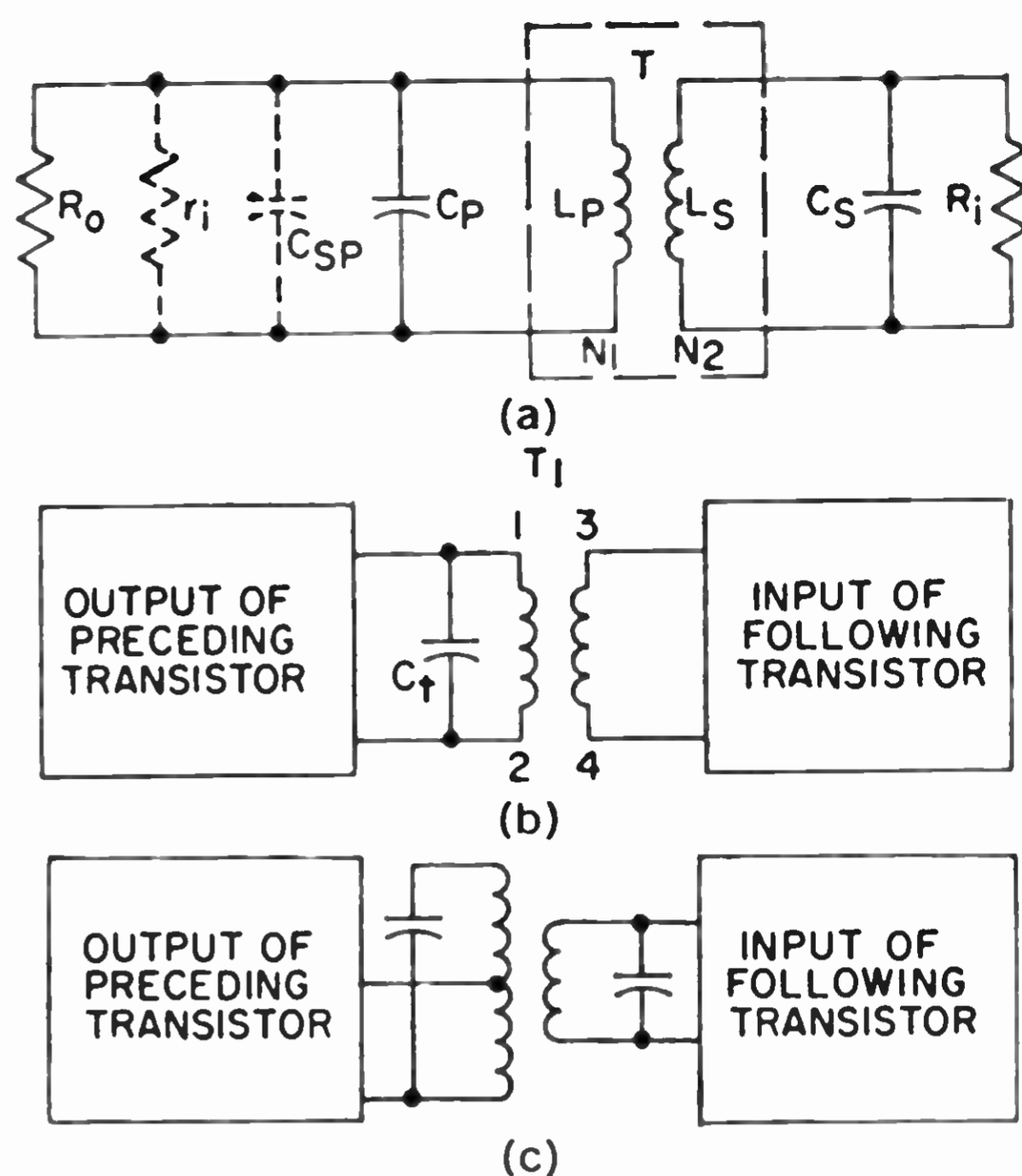


Fig. 160—Equivalent circuits for transformer-coupling networks: (a) having tuned primary winding; (b) using inductive coupling; (c) using tap on primary winding.

The inherent internal feedback in transistors can cause instability and oscillation as the gain of an amplifier stage is increased (i.e., as the load and source impedances are increased from zero to matched conditions). At low radio frequencies, therefore, where the potential gain of transistors is high, it is often desirable to keep the transistor load impedance low. Relatively high capacitance values in the tuned collector circuit can then be avoided by use of a tap on the primary winding of the coupling transformer, as shown in Fig. 160(c). At higher frequencies, the gain potential of the transistor decreases, and impedance matching is permissible. However, lead inductance becomes significant at higher frequencies, particularly in the emitter circuit. All lead lengths should be kept short, therefore, and especially the emitter lead, which not only degrades performance but is also a mutual coupling to the output circuit.

External feedback circuits are often used in tuned coupling networks to counteract the effects of the internal transistor feedback and thus provide more gain or more stable performance. If the external feedback circuit cancels the effects

of both the resistive and the reactive internal feedback, the amplifier is considered to be **unilateralized**. If the external circuit cancels the effect of only the reactive internal feedback, the amplifier is considered to be **neutralized**.

A typical tuned amplifier using neutralization is shown in Fig. 161. The input signal to the transistor is an if carrier (e.g., 455 kHz) amplitude-modulated by an audio signal. Capacitor C_1 and the primary winding of transformer T_1 form a parallel-tuned circuit resonant at 455 kHz. Transformer T_1 couples the signal power from the previous stage to the base of the transistor. Resistors R_1 and R_3 provide forward bias to the transistor. Capacitor C_3 provides a low-impedance path for the 455-kHz signal from the input tuned circuit to the emitter. Resistor R_2 , which is bypassed for 455 kHz by capacitor C_4 , is the emitter dc stabilizing resistor. The amplified signal from the transistor is developed across the parallel resonant circuit (tuned to 455 kHz) formed by capacitor C_6 and the primary winding of transformer T_2 , and is coupled by T_2 to the crystal-diode second detector CR_1 .

Because of the phase reversal inherent in the common-emitter con-

figuration, reactive feedback in the transistor due to the internal capacitance between the collector and the base is 180 degrees out of phase with the input. In the external feedback loop, therefore, current at the intermediate frequency is taken from the secondary winding of the single-tuned output transformer and applied to the base of the transistor through the feedback (neutralizing) capacitor C_5 . Because this current is 180 degrees out of phase with the collector current, it cancels the reactive feedback in the transistor and thus improves the gain of the circuit.

The rectified output of the crystal diode CR_1 is filtered by capacitor C_7 and resistor R_4 so that the voltage across capacitor C_7 consists of an audio signal and a dc voltage (positive with respect to ground for the arrangement shown in Fig. 161) that is directly proportional to the amplitude of the if carrier. This dc voltage is fed back to the base of the transistor through the resistor R_1 to provide automatic gain control. Resistor R_1 and capacitor C_2 form an audio decoupling network to prevent audio feedback to the base of the transistor.

Neutralization, output selectivity, and input and output matching are prime considerations in the

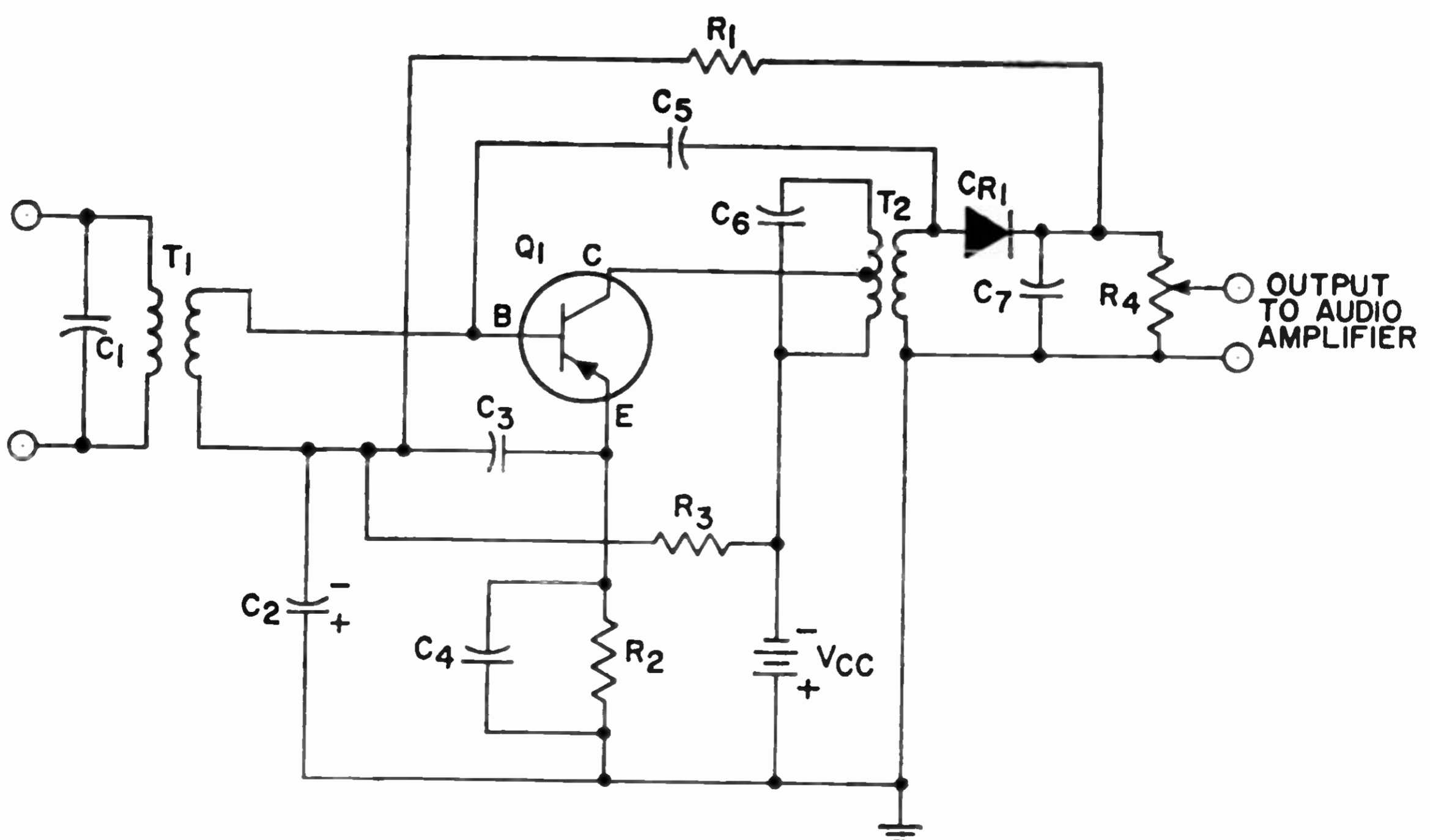


Fig. 161—Neutralized if-amplifier and second-detector circuit.

design of MOS rf circuits. The last two areas are filter-design problems to which there are numerous solutions. The neutralization requirement can also be satisfied in many ways. Some of the more popular circuit techniques are shown in Fig. 162.

In the circuit of Fig. 162(a), capacitor C_f represents the internal feedback capacitance of the MOS transistor amplifier A. An inverted output signal from the secondary of the transformer is fed back through a neutralization capacitance C_n . This feedback signal cancels the signal fed back through the internal path C_f .

The circuits in Fig. 162(b), (c), and (d) are best explained by bridge-type circuit models. In Fig. 162(b) the additional capacitors C_n and C_x form a capacitance bridge with C_f and the output (drain) capacitance C_D . Thus, when the bridge is balanced so that $C_n C_D$ equals $C_x C_f$, zero signal appears at the input for any value of E_o at the output, i.e., the amplifier is neutralized. In Fig. 162(c), a capacitive bridge can be formed by use of the input (gate) capacitance instead of the output capacitance; C_n and C_x are added to form a bridge with C_f and C_G . In the balanced state $C_n C_G$ equals $C_f C_x$ and the amplifier is neutralized. An inductance-capacitance bridge can be formed by inductors L_1 and L_2 in Fig. 162(d). When $L_1 C_D$ equals $L_2 C_f$, the amplifier is neutralized.

A typical neutralized rf amplifier circuit using an n-channel MOS transistor is shown in Fig. 163. The transistor shown is intended for operation at frequencies up to 60 MHz, although it has useful response well beyond this value. Typically, its forward transconductance g_{fs} does not drop 3 dB until approximately 150 MHz. The stage shown in Fig. 163 has a typical power gain of 10 to 18 dB at 60 MHz. Cross-modulation typically is

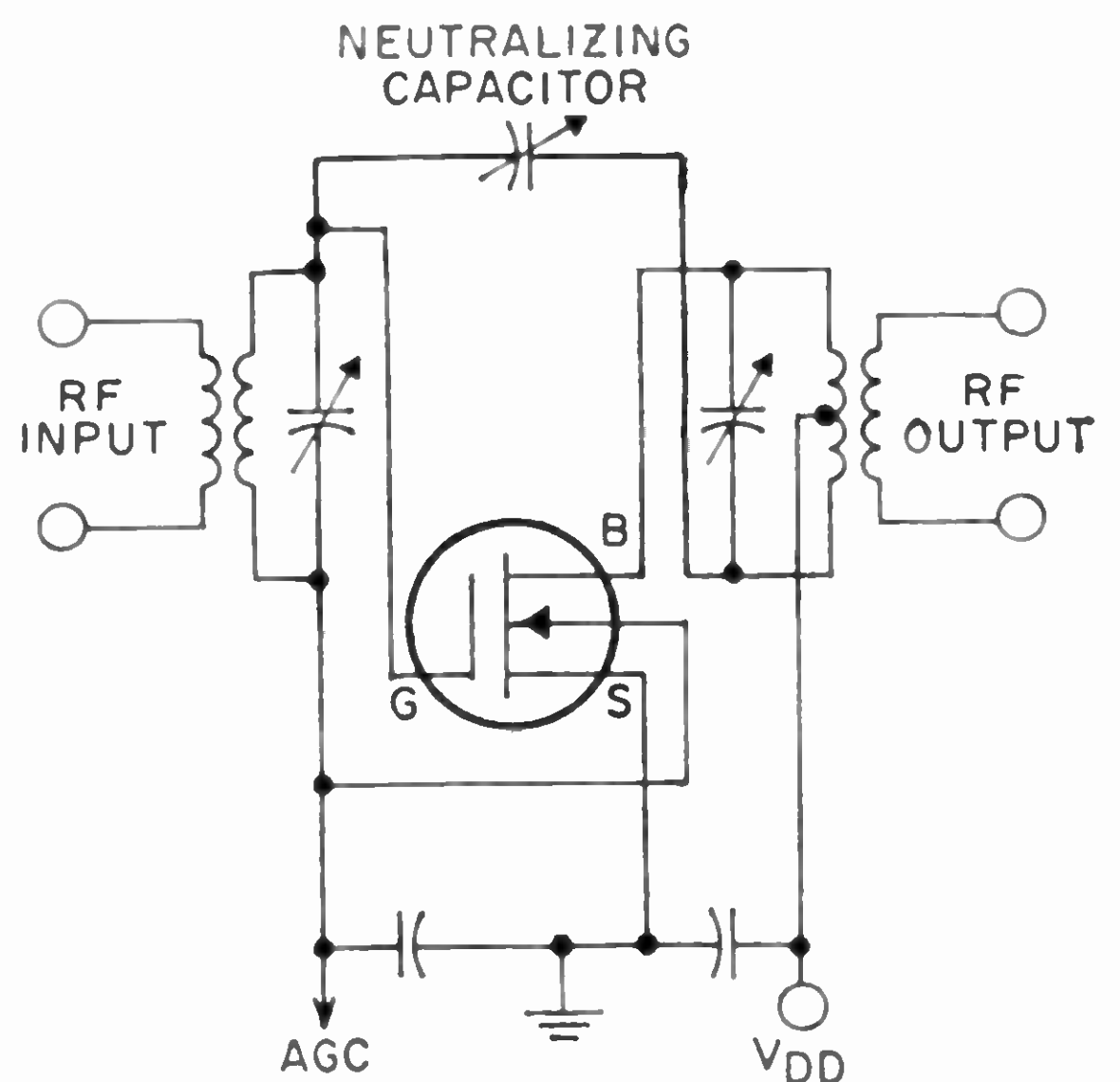


Fig. 163—Typical 60-MHz rf-amplifier stage using MOS transistor.

less than one per cent for interfering signal voltages up to 200 millivolts.

In the design of low-level tuned rf amplifiers, careful consideration must be given to the transistor and

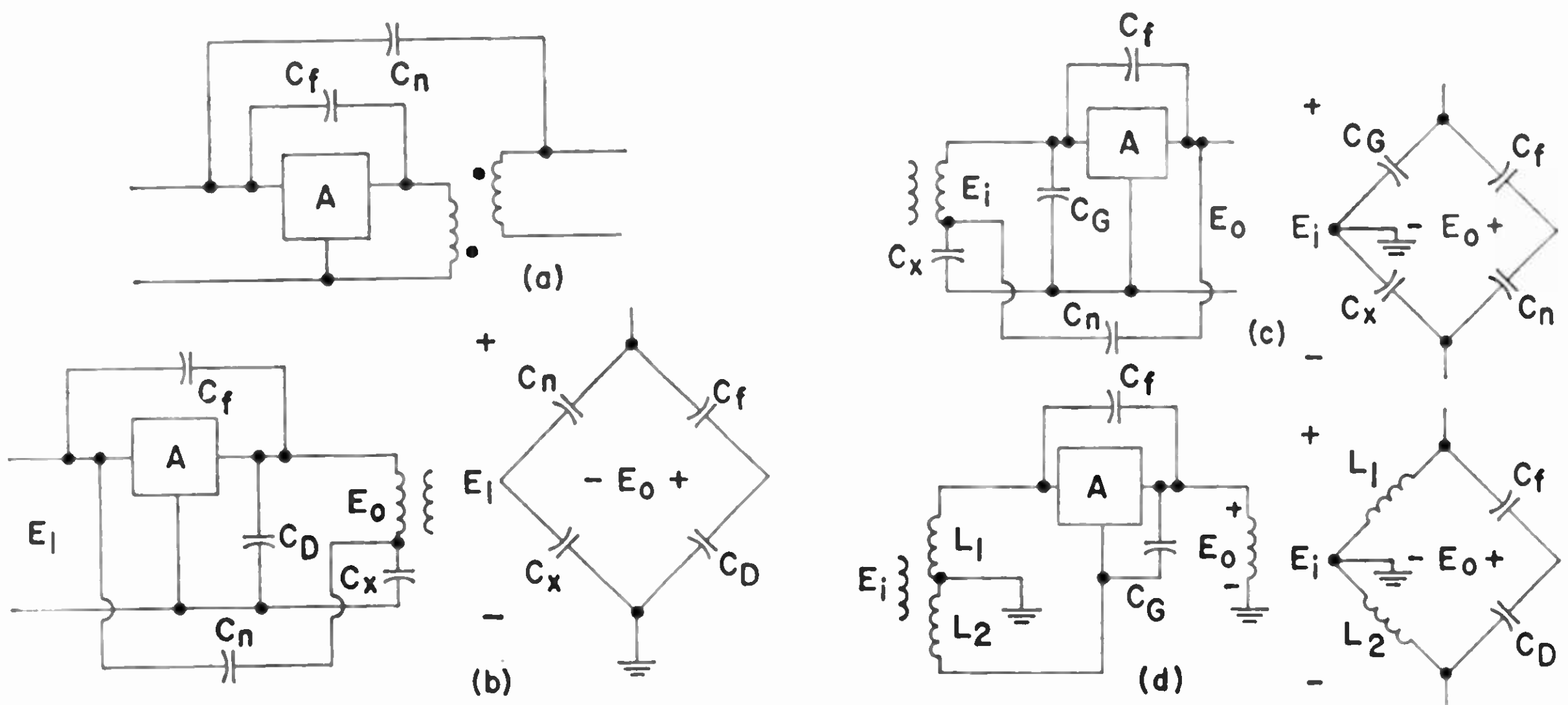


Fig. 162—Some suitable neutralizing techniques for MOS rf circuits.

circuit parameters which control circuit stability, as well as those which maintain adequate power gain. The power gain of an rf transistor must be sufficient to provide a signal that will overcome the noise level of succeeding stages. In addition, if the signals to be amplified are relatively weak, it is important that the transistor and its associated circuit provide low noise figure at the operating frequency. In communication receivers, the noise figure of the rf stage determines the absolute selectivity of the receiver and is, therefore, one of the most important characteristics of the device used in the rf stage.

The relative power-gain capabilities of transistors at high frequencies are indicated by their theoretical maximum frequency of oscillation f_{max} . At this frequency, the unilateralized matched power gain, or maximum available gain MAG, is zero dB. As shown in Fig. 164, the curve of MAG as a function of frequency for a typical rf transistor rises approximately 6 dB per octave below f_{max} .

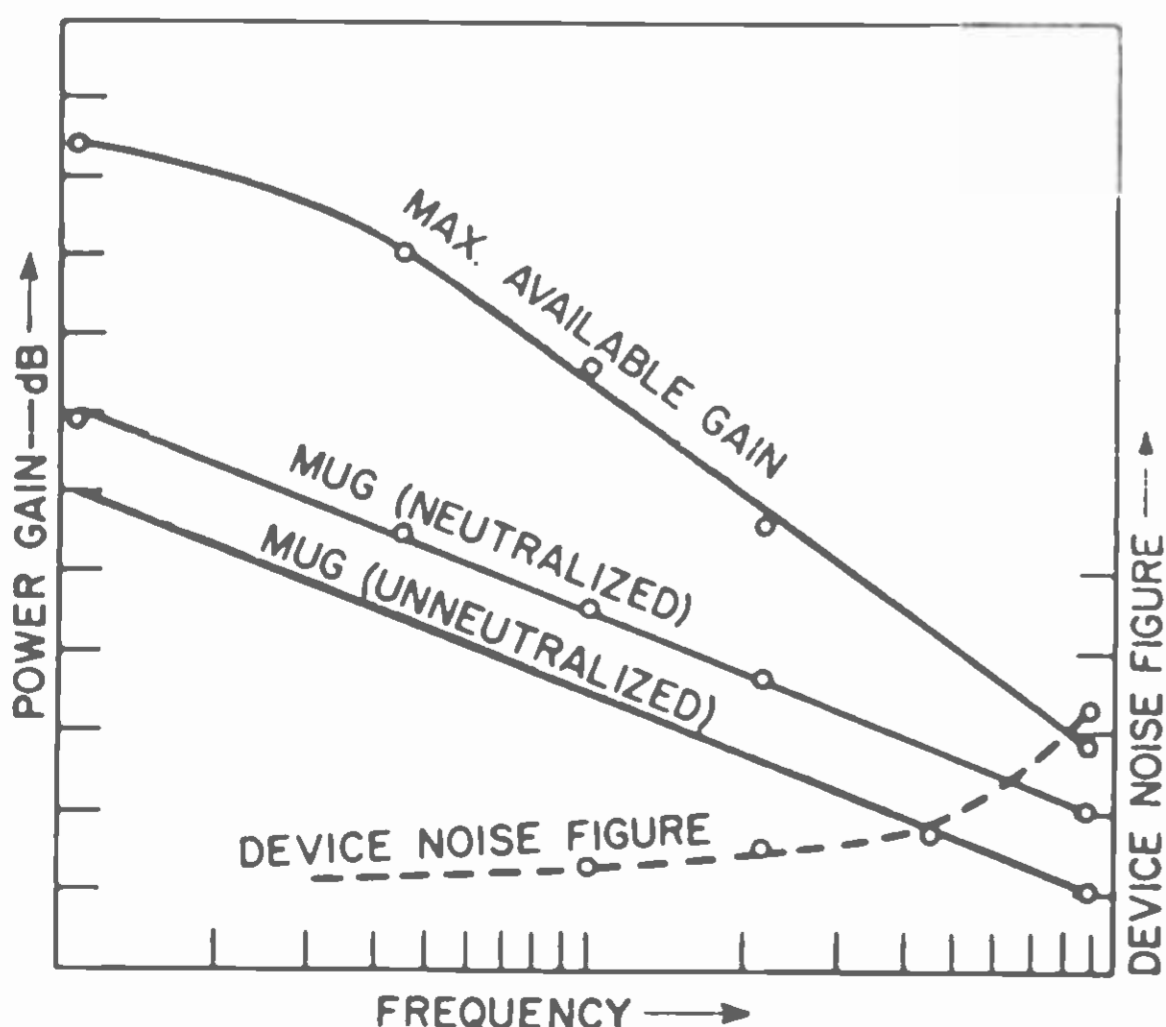
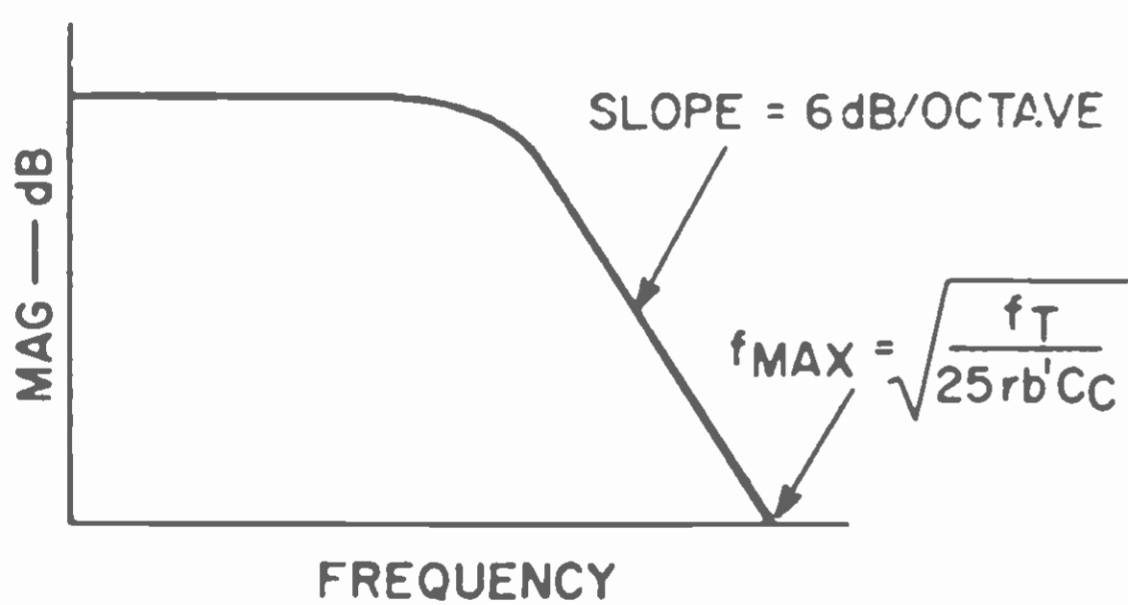


Fig. 164—Maximum available gain MAG, maximum usable gain MUG, and noise figure NF as functions of frequency.

Because most practical rf amplifiers are not individually unilateralized, the power gain that can be obtained is somewhat less than the MAG because of internal feedback in the circuit. This feedback is greater in unneutralized circuits than in neutralized circuits, and therefore gain is lower when neutralization is not used. From a practical consideration, the feedback capacitance which must be considered is the total feedback capacitance between collector and base, including both stray and socket capacitances. In neutralized circuits, stray capacitances, socket capacitance, and the typical value of device capacitance can generally be neutralized. At a given frequency, therefore, the maximum usable power gain MUG of a neutralized circuit depends on the transconductance g_m and the amount of internal feedback capacitance C_r . In unneutralized circuits, however, both socket and stray capacitances are involved in the determination of gain and must be included in the value of C_r . The ratio of g_m to C_r should be high to provide high power gain. Fig. 164 shows typical curves of MAG and MUG (for both the neutralized and the unneutralized case) for a low-level rf transistor used in a common-emitter circuit.

The transistor requirements for high power gain and low noise figure are essentially the same. Published data for transistors intended for low-level rf applications generally indicate a minimum power gain and a maximum noise figure in a circuit typical of the intended use. A curve of noise figure NF as a function of frequency is also shown in Fig. 164. Circuit design factors for lowest noise figure include use of a low-noise transistor, choice of optimum bias current and source resistance, and use of low-loss input circuits. Optimum low-noise bias current for most low-level rf transistors is about 1 milliamperes, or slightly higher in the uhf range. Optimum source resistance is a function of operating frequency and bias current for a given transistor.

Although maximum theoretical power gain cannot be achieved in practical circuits, the gain of MOS transistors at high frequencies closely approximates the theoretical limit except for some losses in the input and output matching circuits.

Power gain is essentially independent of channel width, which is a determining factor in the size of MOS transistors. For example, if the width of the transistor is reduced by one half (and the steady-state drain current is similarly reduced to maintain a constant current density in the device) power gain remains the same because the transconductance, the input conductance, and the output conductance are all reduced by one half. Consequently, the frequency capability of MOS transistors can be increased by a reduction in their size.

The input circuit to the first stage of the amplifier should have as little loss as possible because such loss adds directly to the otherwise attainable noise figure. In other words, if the loss at the input to the first stage is 2 dB, the amplifier noise figure will be 2 dB higher than could be achieved with no loss at the input. To minimize such loss, it is generally desirable that the ratio of unloaded Q (Q_u) to loaded Q (Q_L) of the input circuit be high and that the bias resistors be isolated from the input by chokes or tuned circuits.

In practical rf-amplifier circuits using MOS transistors, the best possible noise figures are obtained when the input impedance of the transistor is slightly mismatched to that of the source. With this technique, noise figures as low as 1.9 dB have been obtained.

Fig. 165 shows the input noise resistance R_N of typical MOS transistors as a function of frequency. In the region where the curves differ, the noise for n-channel MOS units closely resembles "shot noise", i.e., the equivalent noise current I_{eq} increases linearly with direct current, rather than with the square root of the direct current as in the case of

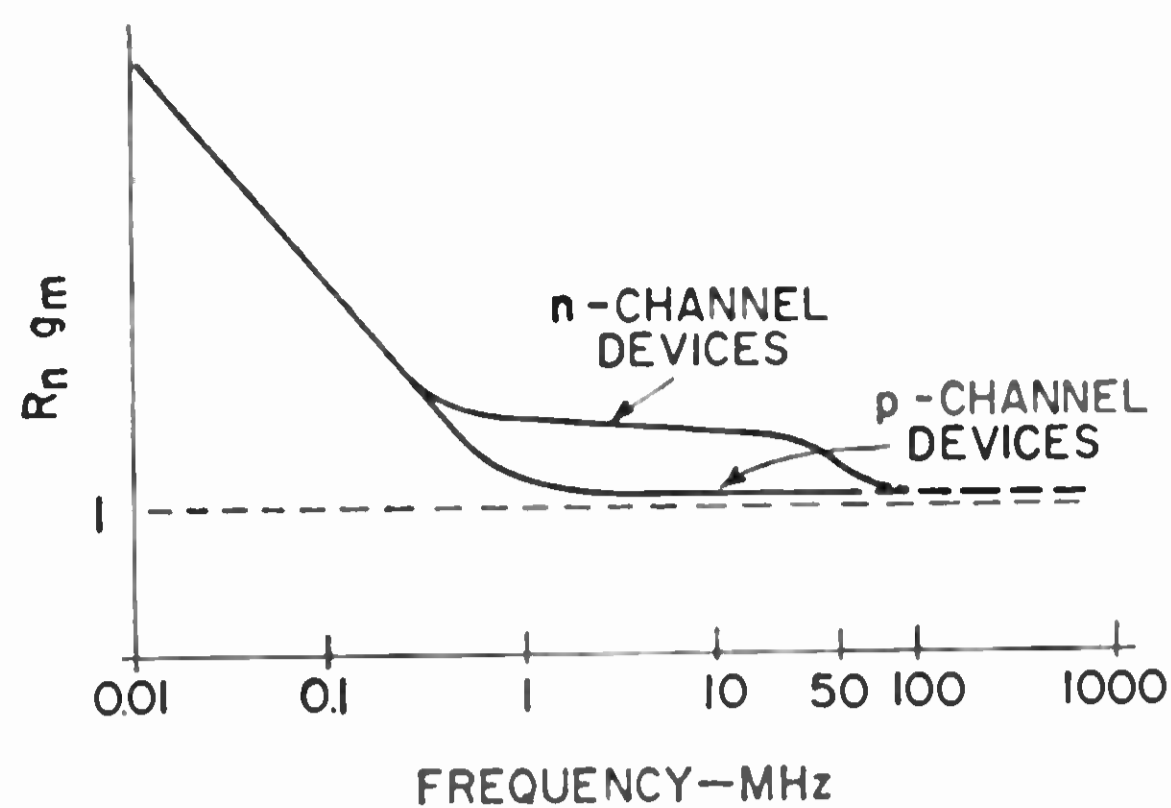


Fig. 165—Input noise resistance R_N of MOS transistors as a function of frequency.

thermal noise. Noise figures of 2 to 4 dB appear practical for MOS transistors operating in the vhf range.

In high-frequency tuned amplifiers, where the input impedance is typically low, mutual inductive coupling may be impracticable because of the small number of turns in the secondary winding. It is extremely difficult in practice to construct a fractional part of a turn. In such cases, capacitance coupling may be used, as shown in Fig. 166. This arrangement, which is also called **capacitive division**, is similar to

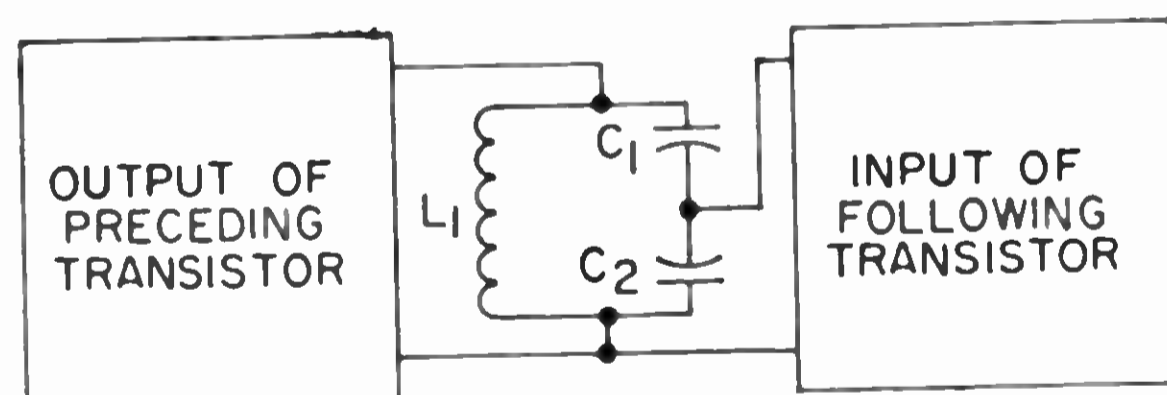


Fig 166—Single-tuned coupling network using capacitive division.

tapping down on a coil at or near resonance. Impedance transformation in this network is determined by the ratio between capacitors C_1 and C_2 . Capacitor C_1 is normally much smaller than C_2 ; thus the capacitive reactance X_{C_1} is normally much larger than X_{C_2} . Provided the input resistance of the following transistor is much greater than X_{C_2} , the effective turns ratio from the top of the coil to the input of the following transistor is $(C_1 + C_2)/C_1$. The total ca-

capitance C_t across the inductance L , is given by

$$C_t = \frac{C_1 C_2}{C_1 + C_2}$$

The resonant frequency f_r is then given by

$$f_r = \frac{1}{2\pi\sqrt{L_1 C_t}}$$

Double-tuned interstage coupling networks are often used in preference to single-tuned networks to provide flatter frequency response within the pass band, a sharper drop in response immediately adjacent to the ends of the pass band, or more attenuation at frequencies far removed from resonance. In synchronous double-tuned networks, both the resonant circuit in the input of the coupling network and the resonant circuit in the output are tuned to the same resonant frequency. In "stagger-tuned" networks, the two resonant circuits are tuned to slightly different resonant frequencies to provide a more rectangular band pass with sharper selectivity at the ends of the pass band. Double-tuned or stagger-tuned networks may use capacitive, inductive, or mutual inductance coupling, or any combination of the three.

Automatic gain control (agc) is often used in rf and if amplifiers in AM radio and television receivers to provide lower gain for strong signals and higher gain for weak signals. (In radio receivers, this gain-compensation network may also be called automatic volume control or avc.) When the signal strength at the antenna changes, the agc circuit modifies the receiver gain so that the output of the last if-amplifier stage remains nearly constant and consequently maintains a nearly constant speaker volume or picture contrast.

The agc circuit usually reduces the rf and if gain for a strong signal by varying the bias on the rf-amplifier and if-amplifier stages when the signal increases. A simple reverse agc circuit is shown in Fig. 167. On each positive half-cycle of the signal volt-

age, when the diode anode is positive with respect to the cathode, the diode passes current. Because of the flow of diode current through R_1 , there is a voltage drop across R_1 which makes the upper end of the resistor negative with respect to ground. This voltage drop across R_1 is applied, through the filter R_2 and C , as reverse

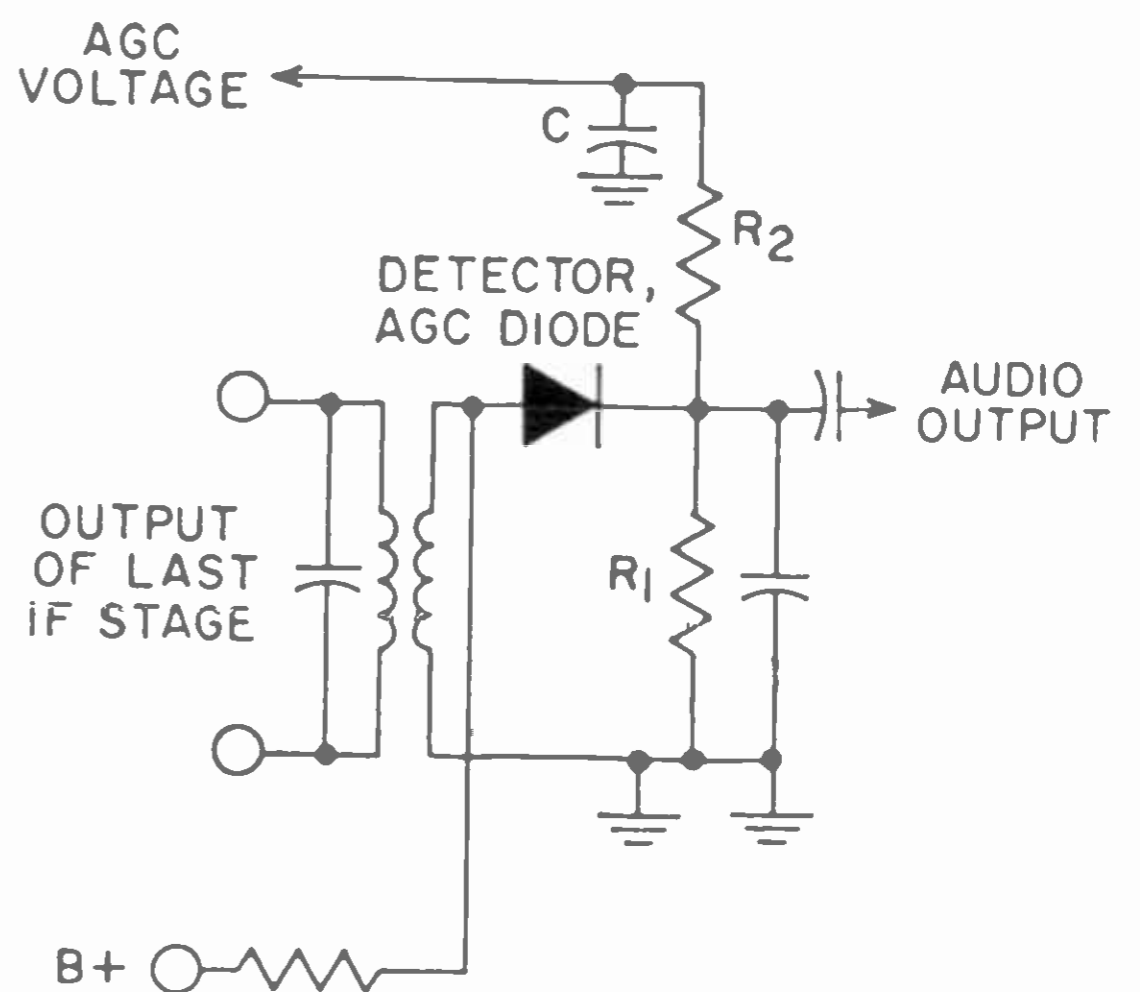


Fig. 167—Simple reverse agc circuit.

bias on the preceding stages. When the signal strength at the antenna increases, therefore, the signal applied to the agc diode increases, the voltage drop across R_1 increases, the reverse bias applied to the rf and if stages increases, and the gain of the rf and if stages is decreased. As a result, the increase in signal strength at the antenna does not produce as much increase in the output of the last if-amplifier stage as it would without agc.

When the signal strength at the antenna decreases from a previous steady value, the agc circuit acts in the opposite direction, applying less reverse bias and thus permitting the rf and if gain to increase.

The filter composed of C and R_2 prevents the agc voltage from varying at an audio frequency. This filter is necessary because the voltage drop across R_1 varies with the modulation of the carrier being received. If agc voltage were taken directly from R_1 without filtering, the audio variations in agc voltage would vary the receiver gain so as to smooth out the modulation of the carrier.

To avoid this effect, the age voltage is taken from the capacitor C. Because of the resistance R_2 in series with C, the capacitor can charge and discharge at only a comparatively slow rate. The age voltage therefore cannot vary at frequencies as high as the audio range, but can vary rapidly at frequencies high enough to compensate for most changes in signal strength.

There are two ways in which automatic gain control can be applied to a transistor. In the reverse age method shown in Fig. 167, age action is obtained by decreasing the collector or emitter current of the transistor, and thus its transconductance and gain. The use of forward age provides improved cross-modulation characteristics and better signal-handling capability than reverse age. For forward age operation, however, the transistor used must be specially designed so that transconductance decreases with increasing emitter current. In such transistors, the current-cutoff characteristics are designed to be more remote than the typical sharp-cutoff characteristics of conventional transistors. (All transistors can be used with reverse age, but only specially designed types with forward age.)

Reverse age is simpler to use, and provides less bandpass shift and tilt with signal-strength variations. The input and output resistances of a transistor increase when reverse age is applied, but the input and output capacitances are not appreciably changed. The change in the loading of tuned circuits is minimal, however, because considerable mismatch already exists and the additional mismatch caused by age has little effect.

In forward age, however, the input and output resistances of the transistor are reduced when the collector or emitter current is increased, and thus the tuned circuits are damped. In addition, the input and output capacitances change drastically, and alter the resonant frequency of the tuned circuits. In a practical circuit, the bandpass shift and tilt caused by

forward age can be compensated to a large extent by the use of passive coupling circuits.

Cross-modulation, an important consideration in the evaluation of transistorized tuner circuits, is produced when an undesired signal within the pass band of the receiver input circuit modulates the carrier of the desired signal. Such distortion occurs when third- and higher-order nonlinearities are present in an rf-amplifier stage. In general, the severity of cross-modulation is independent of both the semiconductor material and the construction of the transistor (provided gain and noise factor are not sacrificed). At low frequencies, cross-modulation is also independent of the amplitude of the desired carrier, but varies as the square of the amplitude of the interfering signal.

To measure cross-modulation distortion, it is necessary to determine the amplitude of the undesired signal which transfers one per cent of its modulation to the desired signal. In most cases, a value of 100 millivolts or more over the complete age range is considered good. The cross-modulation characteristics of MOS transistors are as good as those of bipolar transistors in the high-attenuation region, and are as much as ten times better in the low-attenuation region (when the incoming signal is weak). This low cross-modulation distortion should ultimately lead to extensive use of MOS transistors in the rf stages of all types of communications receivers.

In most rf circuits, the undesirable effects of cross-modulation can be minimized by good selectivity in the antenna and rf interstage coils. Minimum cross-modulation can best be achieved by use of the optimum circuit Q with respect to bandwidth and tracking considerations, which implies minimum loading of the tank circuits.

In rf circuits where selectivity is limited by the low unloaded Q's of the coils being used, improved cross-

modulation can be obtained by mismatching the antenna circuit (that is, selecting the antenna primary-to-secondary turns ratio such that the reflected antenna impedance at the base of the rf amplifier is very low compared to the input impedance). This technique is commonly used in automobile receivers, and causes a slight degradation in noise figure. At high frequencies, such as in television, where low source impedances are difficult to obtain because of lead inductance or the impracticality of putting a tap on a coil having one or two turns, an unbypassed emitter resistor having a low value of resistance (e.g., 22 ohms) may be used to obtain the same effect.

Cross-modulation may occur in the mixer or rf amplifier, or both. Accordingly, it is important to analyze the entire tuner as well as the individual stages. Cross-modulation is also a function of agc. At sensitivity conditions where the rf stage is operating at maximum gain and the interfering signal is far removed from the desired signal, cross-modulation occurs primarily in the rf stage. As the desired signal level increases and agc is applied to the rf stage, the rf transistor gain decreases and provides improved cross-modulation. If the interfering signal is close to the desired signal, it is the rf gain at the undesired signal frequency which determines whether the rf stage or mixer stage is the prime contributor of cross-modulation. For example, it is possible that the rf stage gain (including selectivity of tuned circuits) at the undesired frequency is greater than unity. In this case, the undesired signal at the mixer input is larger than that at the rf input; thus the contribution of the mixer is appreciable. Intermediate and high signal conditions may be analyzed similarly by considering rf agc.

If adequate limiting is employed, cross-modulation does not occur in an FM signal.

Spurious-response characteristics are an important consideration in the evaluation of transistorized FM tuner circuits. Like cross-modulation, spurious response, an effect caused by the mixture of unwanted signals with the desired carrier, can occur in either the rf stage or the mixer. MOS field-effect transistors are especially suitable for use in FM rf-amplifier and mixer stages because of their inherently superior spurious-response rejection properties and signal-handling capabilities.

When spurious response is created in the rf amplifier, it may be removed by improved filtering between the rf amplifier and the mixer. When used as an rf amplifier, the MOS transistor produces an output signal that contains low levels of the harmonics of unwanted signals. As a result, the need for a double-tuned rf interstage transformer is reduced and acceptable performance can usually be achieved with single-tuned circuits in both the antenna and rf interstage sections.

The dynamic-range capability of MOS field-effect transistors is about 25 times greater than that of bipolar transistors. In an actual tuner circuit, this large intrinsic dynamic range is reduced by a factor proportional to the square of the circuit source impedances. The net result is a practical dynamic range for MOS tuner circuits about five times that for bipolar types.

With MOS field-effect transistors, as contrasted with either bipolar transistors or junction-gate field-effect transistors, there is no loading of the input signal, nor drastic change of input capacitance even under extreme overdrive conditions.

In junction-gate field-effect transistors, a large incoming signal can have sufficiently high positive swing to drive the gate into conduction by a momentary forward bias; power is then drawn from the input signal just as if a resistance were placed across the input circuit. In bipolar transistors, there is a gradual change of both input impedance and input

capacitance as a function of large signal excursions. These changes are undesirable because they can result in detuning of tuned circuits and widening of the input selectivity curve.

Fig. 168 shows an FM tuner with an MOS-transistor rf-amplifier stage; the operation of the tuner

loading of the interstage coil and cause some degradation in the selectivity of the front end, they can be tolerated because the antenna coil is not loaded by the gate of the MOS transistor.

The elimination of spurious response is the primary goal in the circuit design shown in Fig. 168.

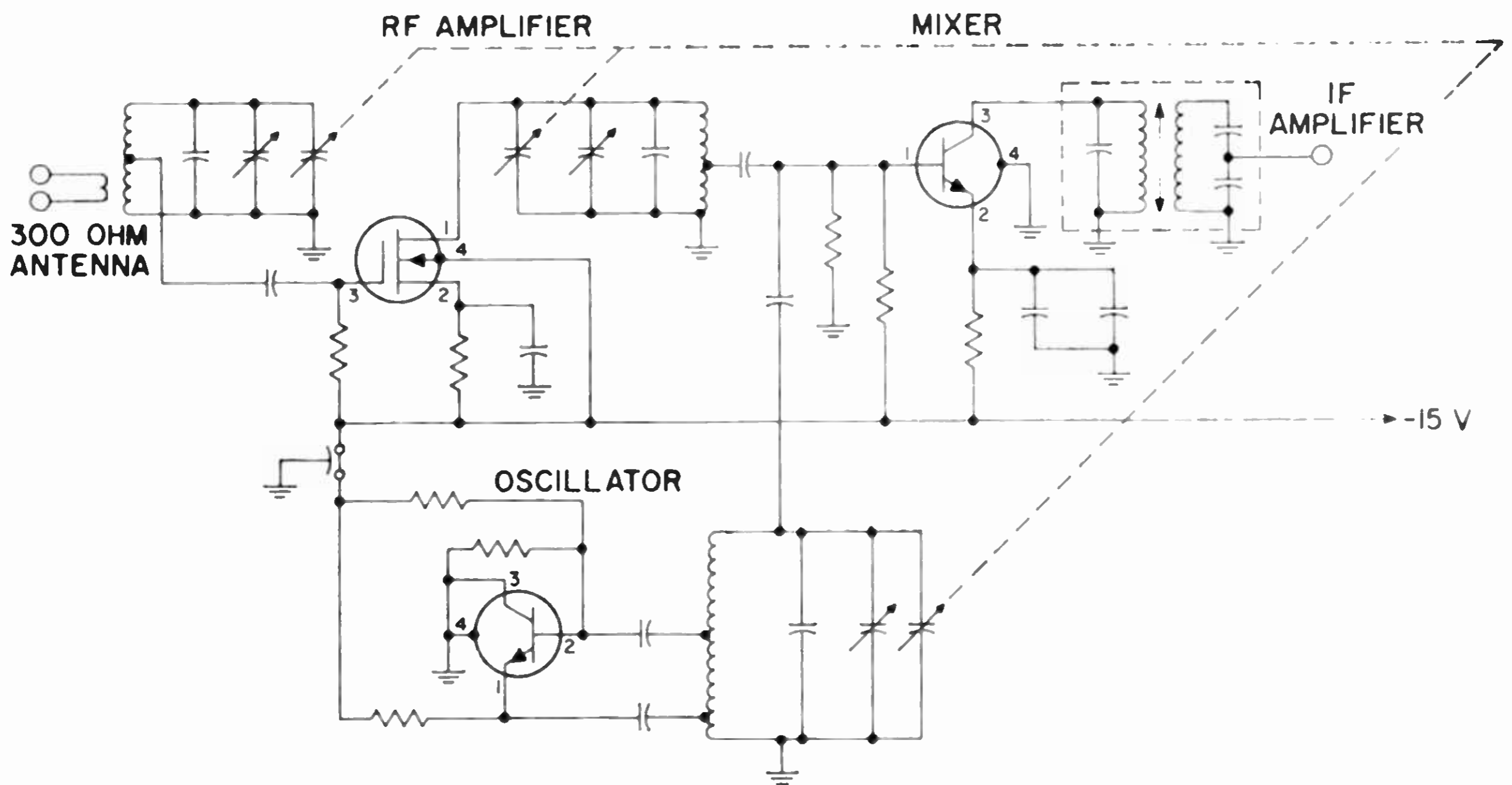


Fig. 168—Typical FM tuner using MOS-transistor rf-amplifier stage.

is described in the **Circuits** section of this Manual. Figs. 169 through 173 show curves that illustrate tuner performance.

Selection of the appropriate source and load impedance for the rf stage is based on the fact that a low spurious response requires the gate of the MOS to be tapped as far down on the antenna coil as gain and noise considerations permit. This arrangement applies the smallest possible voltage swing to the gate and makes optimum use of the available dynamic range.

In addition, achievement of minimum spurious response requires the use of the entire rf interstage coil as the load for the MOS transistor. This interstage coil, which is selected on the basis of a compromise between gain and bandwidth requirements, presents a slight mismatch to the output impedance of the MOS transistor. Although these design compromises result in a slight

Generally, a circuit that has a low spurious response is difficult to reproduce. In some systems, the performance of such a circuit depends on the exact operating points of the transistors used. When the rf-amplifier transistor in Fig. 168 is changed, performance of the tuner remains essentially the same. Fig. 169 shows

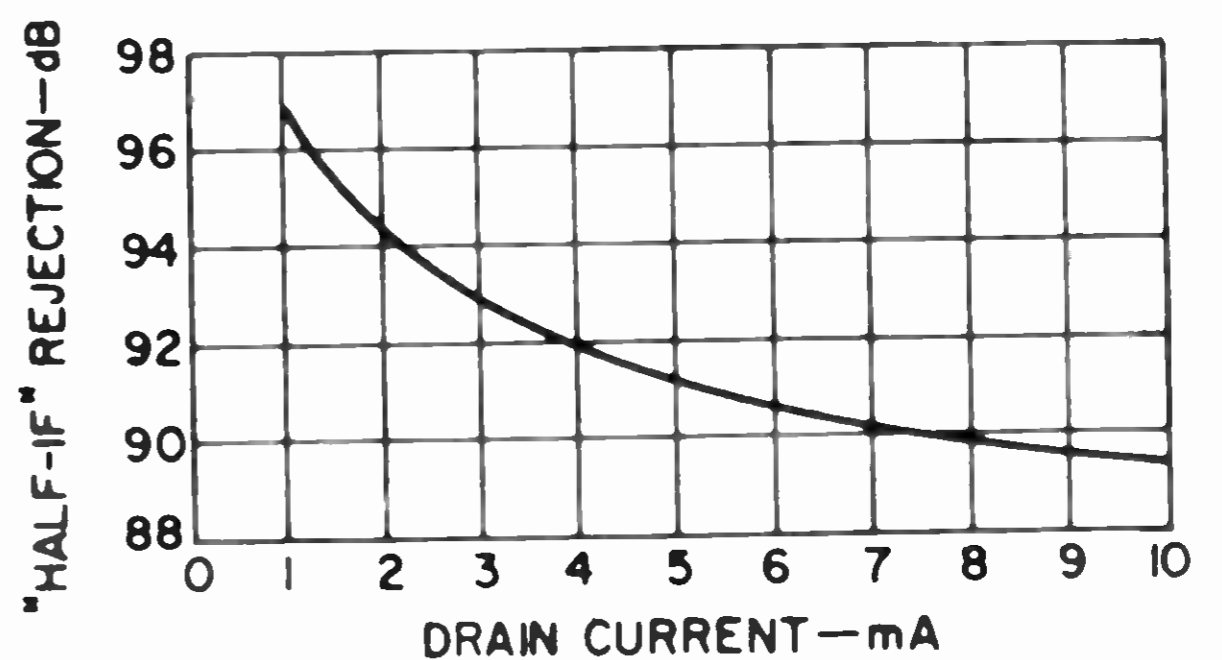


Fig. 169—Half-if rejection as a function of operating point for tuner in Fig. 168.

the change in the rejection of the "half-if" spurious response as a function of drain current for a typical MOS transistor. Fig. 170 shows the variation of 20-dB quieting

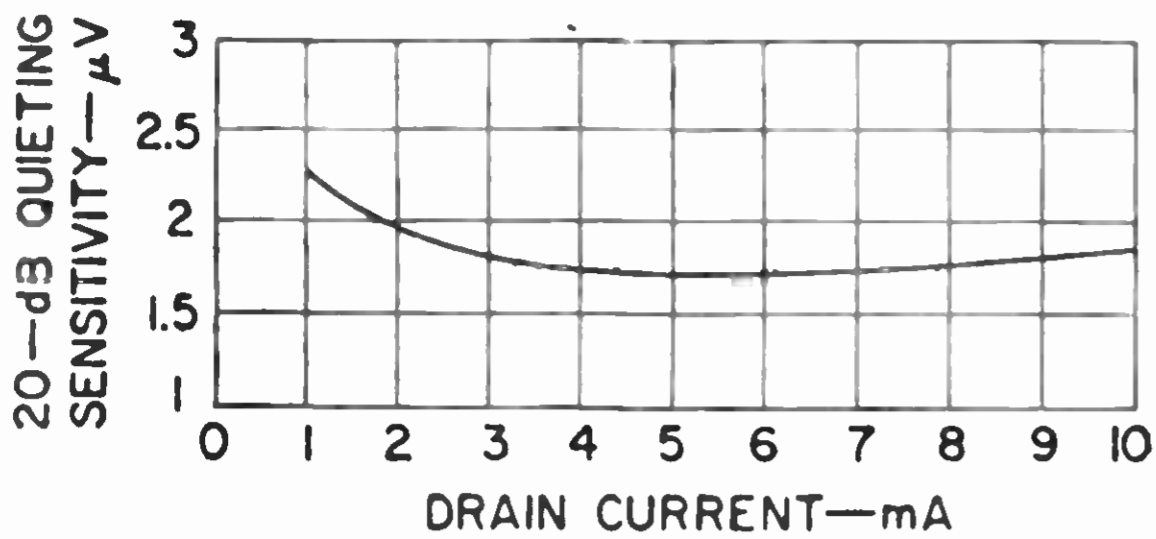


Fig. 170—20-dB quieting sensitivity as a function of operating point for FM tuner shown in Fig. 168.

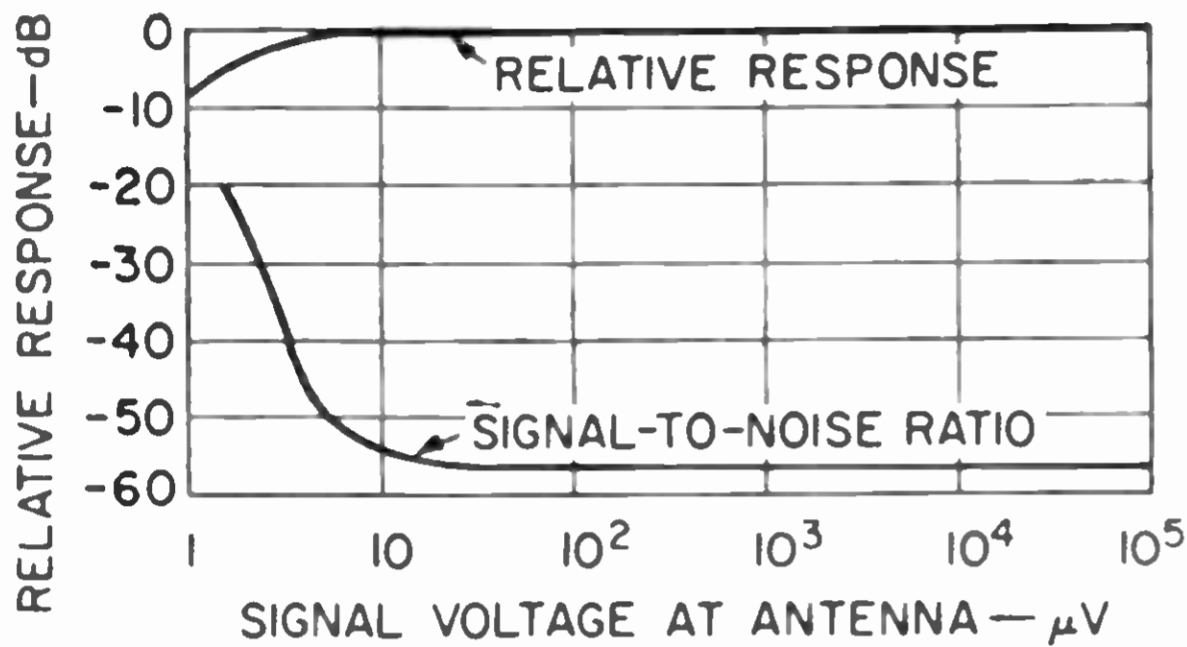


Fig. 171—Relative response as a function of signal voltage measured at antenna terminals.

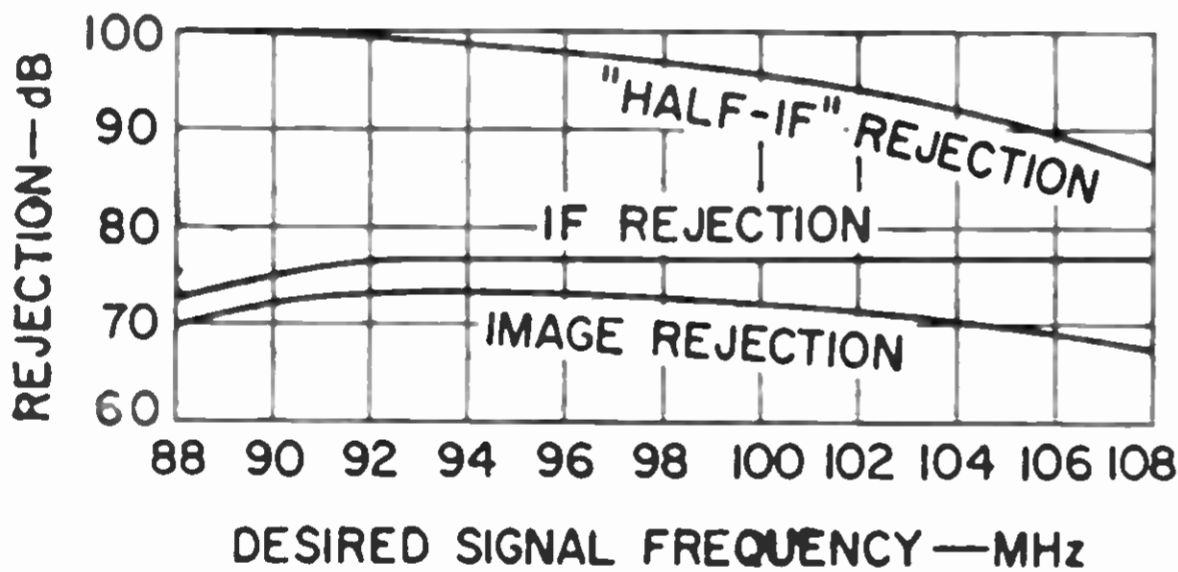


Fig. 172—Spurious-response rejection as a function of frequency.

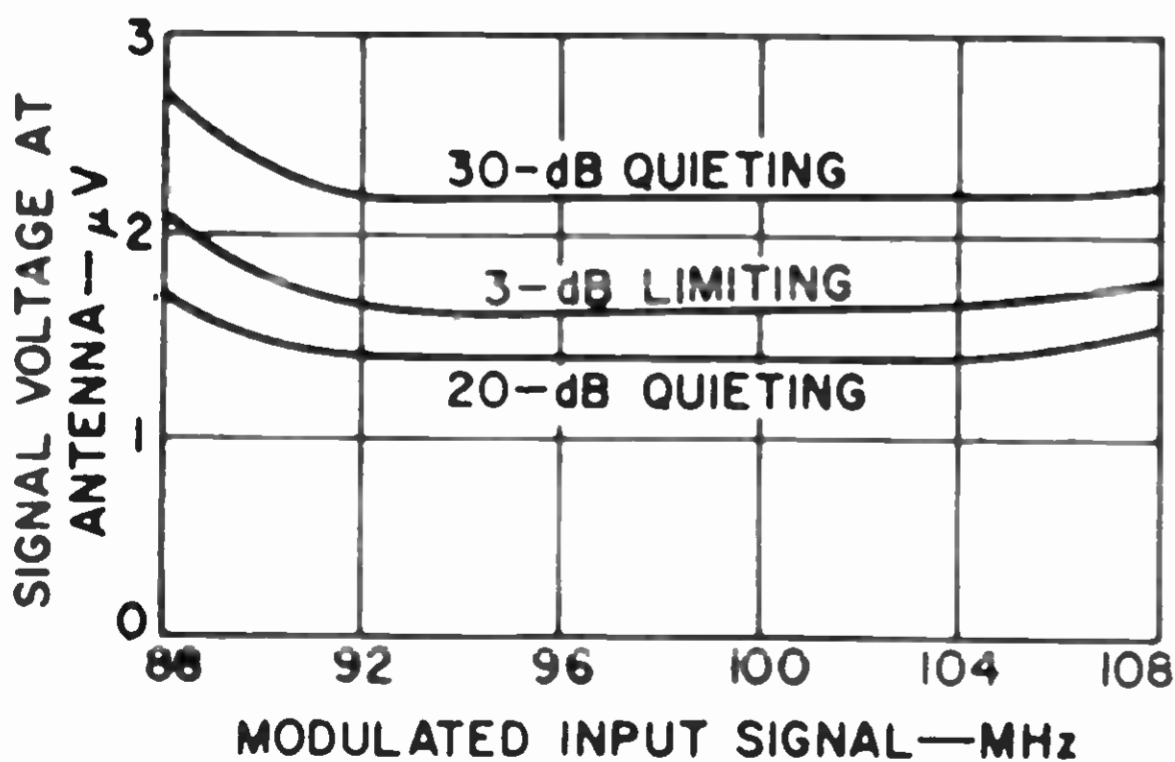


Fig. 173—Sensitivity curves for FM receiver using tuner shown in Fig. 168.

sensitivity as a function of drain current.

Figs. 174 and 175 show FM tuner circuits that use bipolar transistors only. The n-p-n silicon transistors

used are characterized by very low feedback capacitance, low noise, and high useful power gain, and feature a terminal arrangement in which the base and emitter terminals are interchanged to provide maximum isolation between the base and collector terminals. Although this basing configuration does not appreciably change the measured device-feedback capacitance, it does allow reduction of the collector-to-base capacitance due to external circuitry.

Laboratory results indicate that although tuners using three tuned circuits (including the oscillator tank) perform extremely well with regard to gain, noise, and rejection of certain higher-order spurious responses, the addition of another tuned circuit provides truly superior performance with regard to the attenuation of all spurious responses including image and the troublesome "half-if."

Figs. 174 and 175 each show the schematic diagram of a four-coil tuner designed around bipolar transistors. The dc conditions of both circuits are identical. The rf-stage transistor operates in the common-emitter configuration at an emitter current of 1.5 milliamperes. This configuration offers the highest stable gain at FM frequencies; the operating point specified was chosen as a compromise between noise, gain, and spurious response rejection. The mixer transistor operates in a common-emitter configuration at 1.5 milliamperes. The oscillator transistor operates in the common-collector configuration at approximately 2.5 milliamperes and provides approximately 28 millivolts of injection voltage to the mixer base. The common-collector configuration was chosen because it offers the greatest frequency stability with respect to changes in voltage and temperature. Also, if recommended wiring practices are adhered to, the use of the common-collector oscillator minimizes higher-order spurious responses.

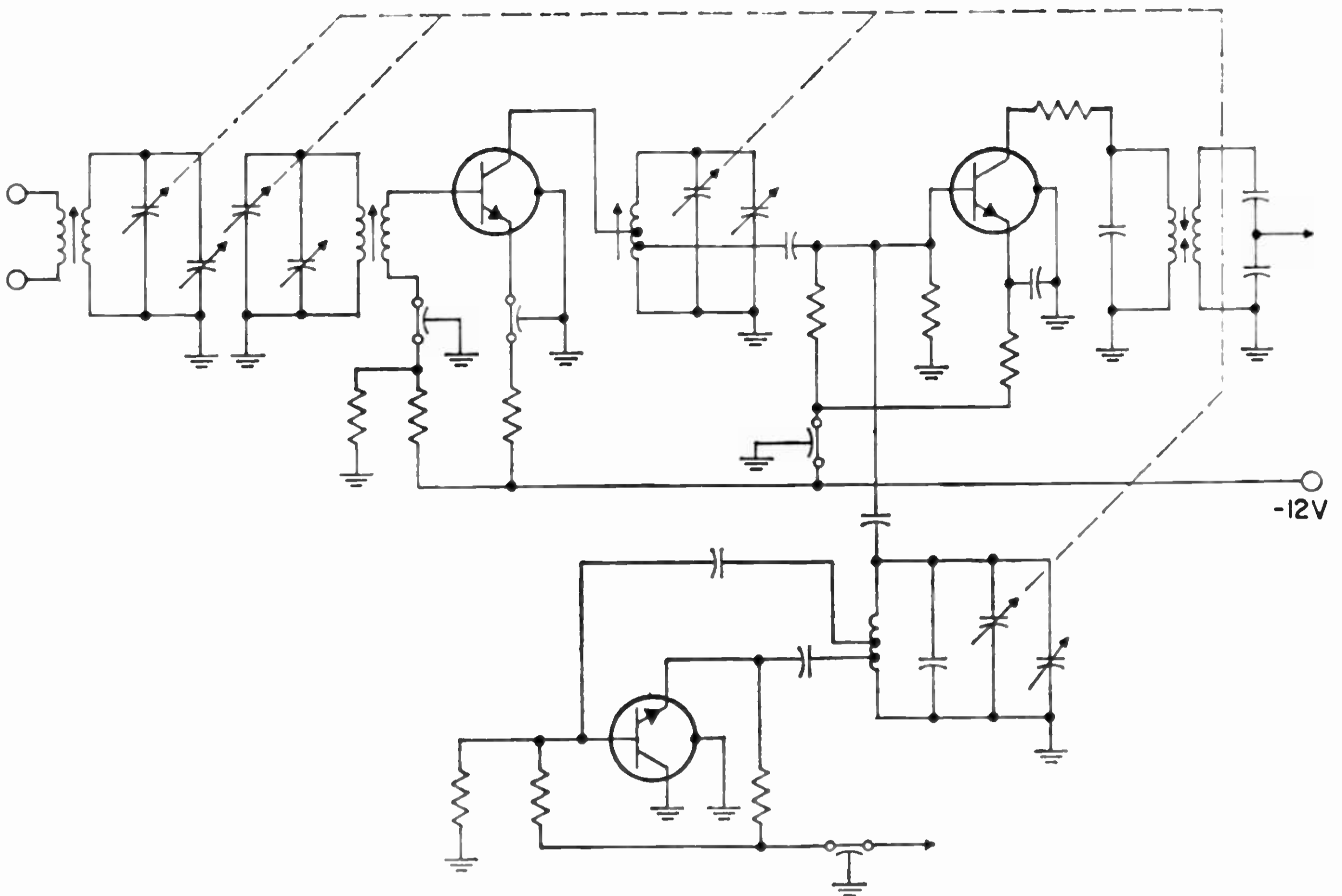


Fig. 174—Four-coil FM tuner with double-tuned antenna transformer.

In Fig. 174 the antenna coil is double-tuned, and thus provides better selectivity characteristics ahead of the rf stage than a single-tuned transformer under the same impedance-matching condition. By using coils with unloaded, mounted Q's of 100, sufficient selectivity is realized so that at signal levels up to 200 millivolts there are no spuri-

ous responses within the FM frequency band. One disadvantage of double-tuned transformers is the coupling loss associated with them. Noise performance is degraded from that obtained when single tuning is employed in the antenna coil by exactly the coupling loss of the double-tuned coil.

Because the IHF (Institute of

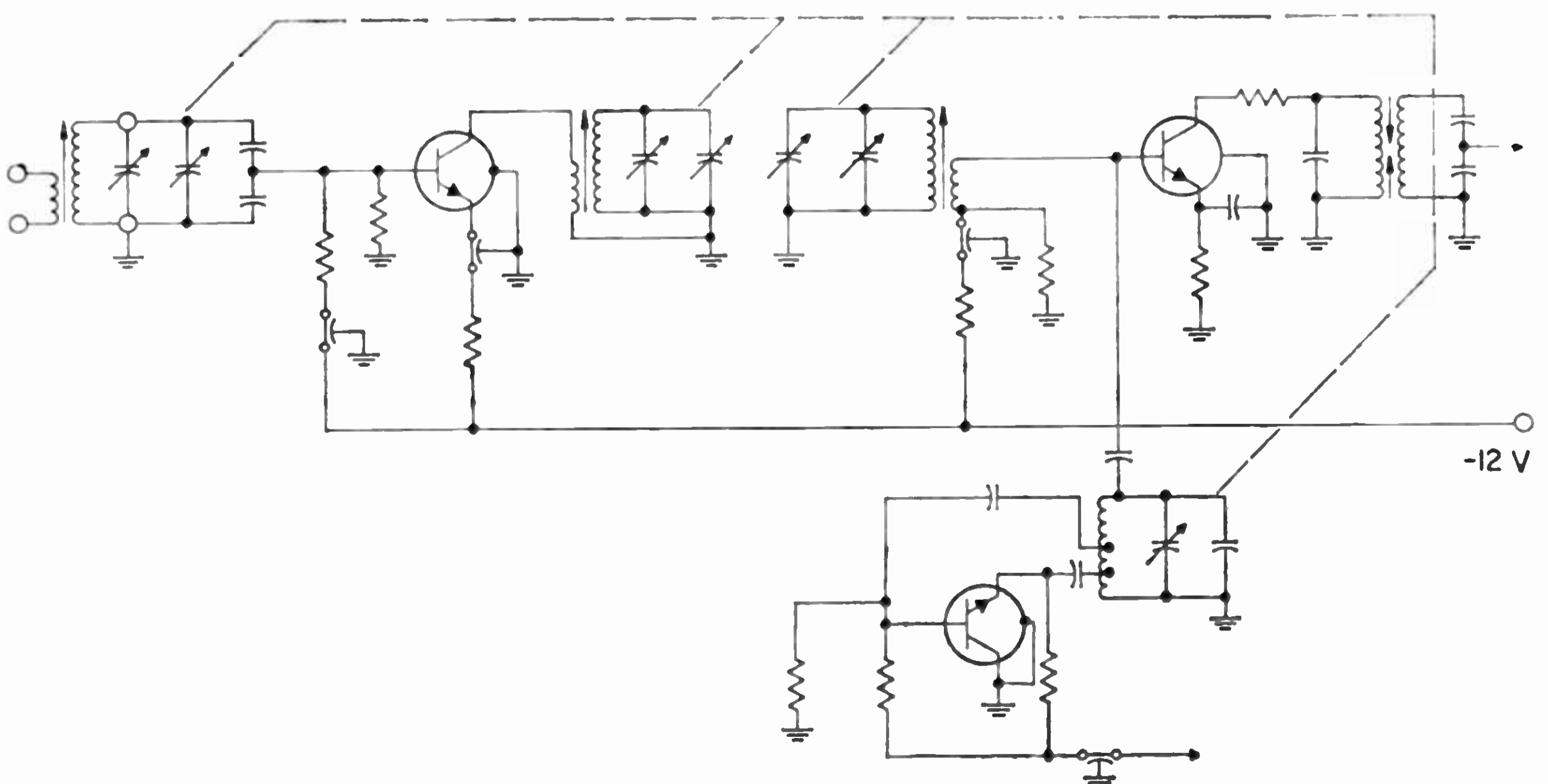


Fig. 175—Four-coil FM tuner with double-tuned rf transformer.

High Fidelity) sensitivity has developed into an important requirement and because a low value of IHF sensitivity is determined in part by noise performance, a circuit, Fig. 175, has been designed that improves the noise performance and yet maintains a high degree of rejection of spurious responses. It is felt that although high selectivity ahead of the rf stage is desirable, it is not essential. Laboratory tests indicate that the mixer is primarily responsible for spurious generation and that it is more important to maintain low drive to the mixer base and to have adequate selectivity ahead of it. Because the over-all gain from antenna to mixer base must be kept low enough for spurious immunity, and sufficiently high (10 to 15 dB) to mask mixer noise, it is clear that all of the available maximum usable gain is not needed. At a sacrifice of some gain, therefore, the selectivity characteristics of the double-tuned rf transformer can be improved by decreasing the coupling. It is assumed that if harmonics are generated in the rf stage, they will be adequately attenuated by the rf transformer. With a single-tuned antenna coil, circuit noise performance is improved for the reasons described.

Neither of the four-coil tuner circuits shown in Figs. 174 and 175 uses a 10.7-MHz if trap because the need for such a trap is eliminated with the use of the inductively tapped transformer.

A choice of first if transformer is offered. One version employs a capacitance-tapped secondary, as shown in Figs. 174 and 175; the other has an inductively tapped secondary. Electrically, both transformers are identical.

A limiter circuit is essentially an if-amplifier stage designed to provide clipping at a desired signal level. Such circuits are used in FM receivers to remove AM components from the if signal prior to FM detection. The limiter stage is normally the last stage prior to detection, and is simi-

lar to preceding if stages. At low input rf signal levels, it amplifies the if signal in the same manner as preceding stages. As the signal level increases, however, a point is reached at which the limiter stage is driven into saturation (i.e., the peak currents and voltages are limited by the supply voltage and load impedances and increases in signal produce very little increase in collector current). At this point, the if signal is "clipped" (or flattened) and further increases in rf signal level produce no further output in if signal to the detector.

Limiter stages may be designed to provide clipping at various input-signal levels. A high-gain FM tuner is usually designed to limit at very low rf input signal levels, and possibly even on noise signals. Additional AM rejection may be obtained by use of a ratio detector for the frequency discriminator.

Wideband (Video) Amplifiers

In television camera chains as well as in ac voltmeters and vertical amplifiers for oscilloscopes, it is necessary for a transistor circuit to amplify signals ranging from very low frequencies (several hertz) to high frequencies (tens of megahertz) with a minimum of frequency and time-delay distortion. In response to these demands, circuit compensation techniques have been developed to minimize the amplitude and time-delay variation as the upper or lower frequency limits of the amplifier are approached.

The need for such compensation is evident when many identical stages of amplification are employed. If ten cascaded stages are used, a variation of 0.3 dB per stage results in a total variation of 3 dB. In an uncompensated amplifier, this total variation occurs two octaves (a frequency ratio of four) prior to the half-power point. Because two octaves are lost from both the high and low frequencies, the bandwidth of ten cascaded uncompensated amplifier stages is

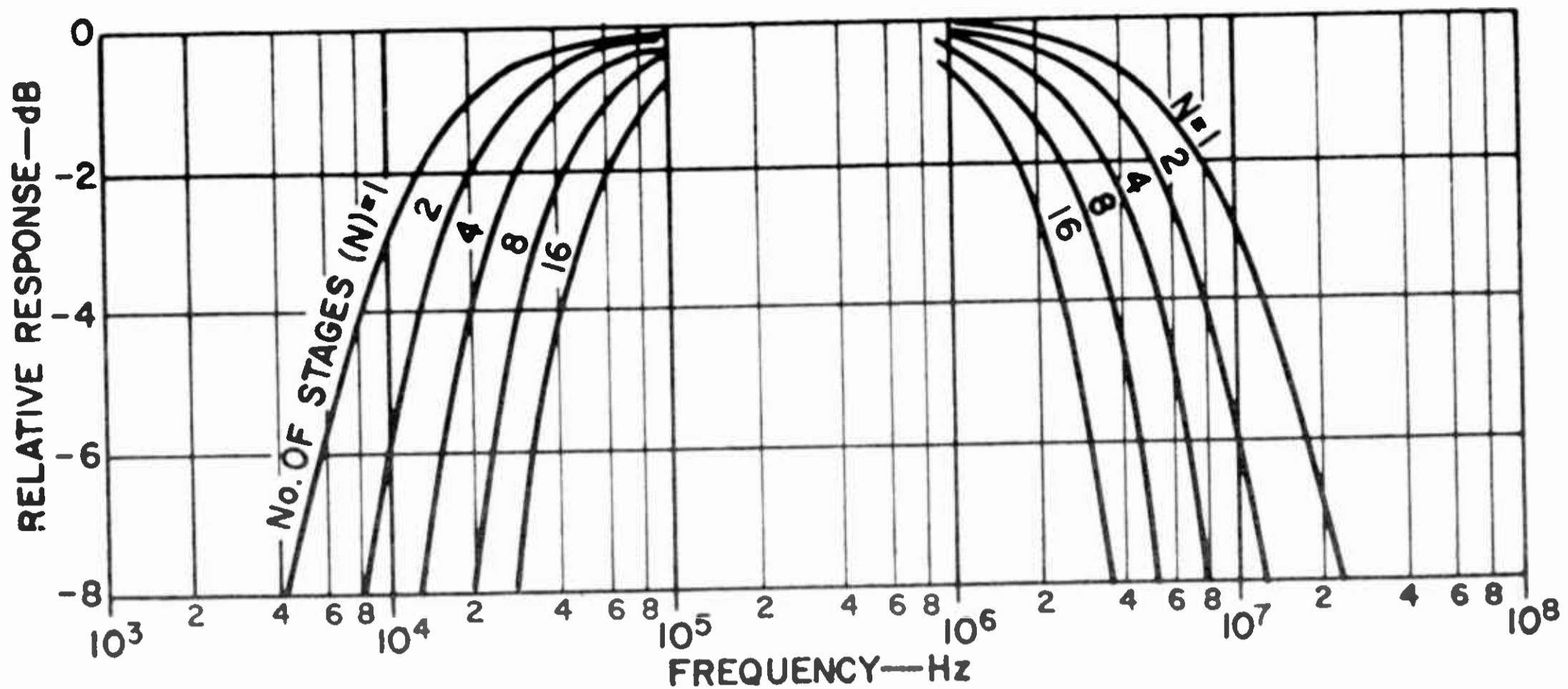


Fig. 176—Amplitude response characteristics of various numbers (N) of identical uncompensated amplifiers.

only one-sixteenth that of a single amplifier stage. Fig. 176 shows the amplitude response characteristics of various numbers of identical uncompensated amplifiers.

In general, the output of an amplifier may be represented by a current generator i_{out} and a load resistance R_L , as shown in Fig. 177(a). Because the signal current is shunted by various capacitances at high frequencies, as shown in Fig. 177(b), there is a loss in gain at these frequencies. If an inductor L is placed in series with the load resistor R_L , as shown in

Fig. 177(c), a low-Q circuit is formed which somewhat suppresses the capacitive loading. This method of gain compensation, called **shunt peaking**, can be very effective for improving high-frequency response. Fig. 177 shows the frequency response for the circuits shown in Figs. 177(a), (b), and (c). If the inductor L shown in Fig. 177(c) is made self-resonant approximately one octave above the 3-dB frequency of the circuit of Fig. 177(b), the amplifier response is extended by about another 30 per cent.

If the stray capacitance C shown

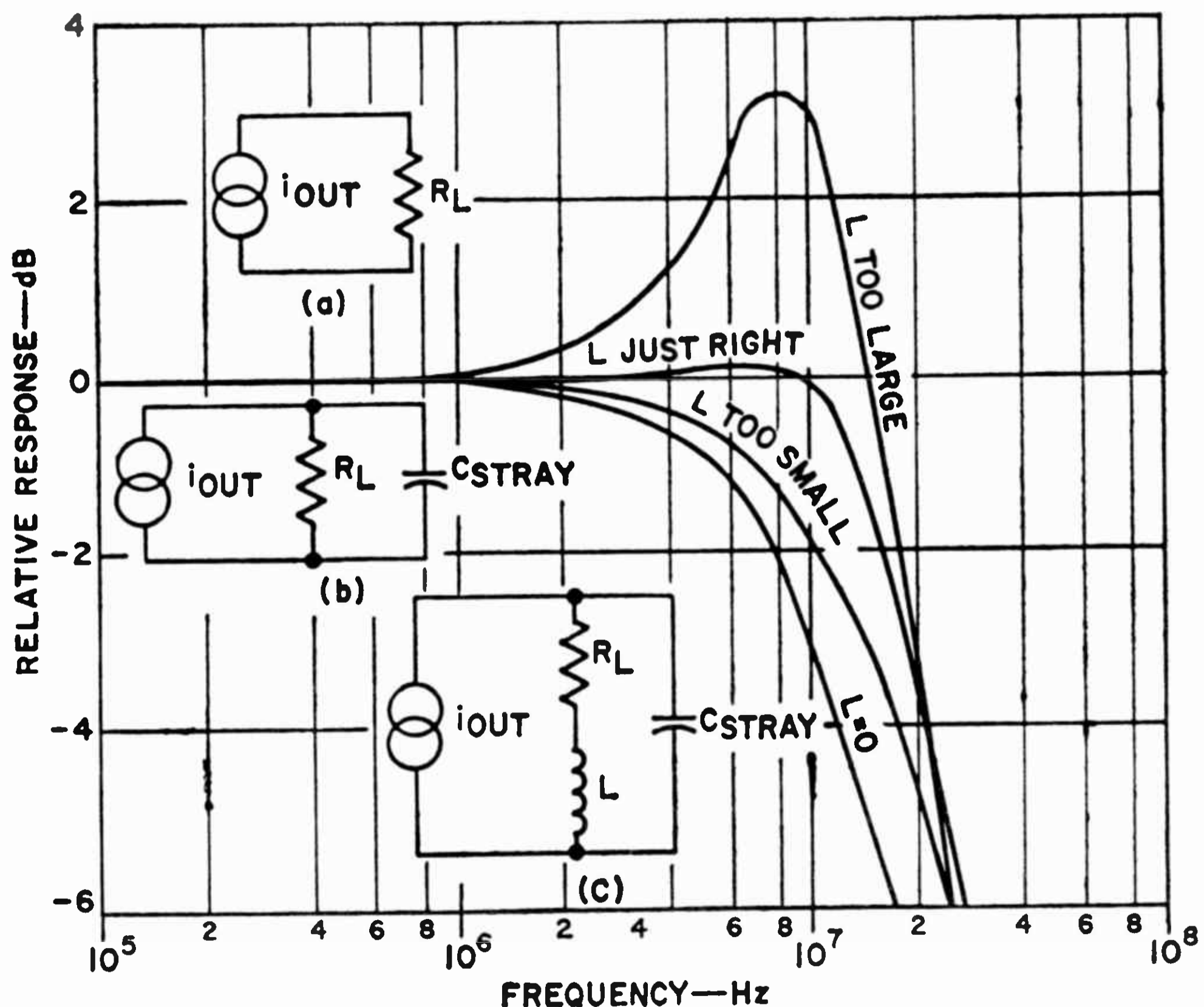


Fig. 177—Equivalent circuits and frequency response of uncompensated and shunt-peaked amplifiers.

in Fig. 177(b) is broken into two parts C' and C'' and an inductor L_1 is placed between them, a heavily damped form of series resonance may be employed for further improvement. This form of compensation, called series peaking, is shown in Fig. 178. If C' and C'' are within

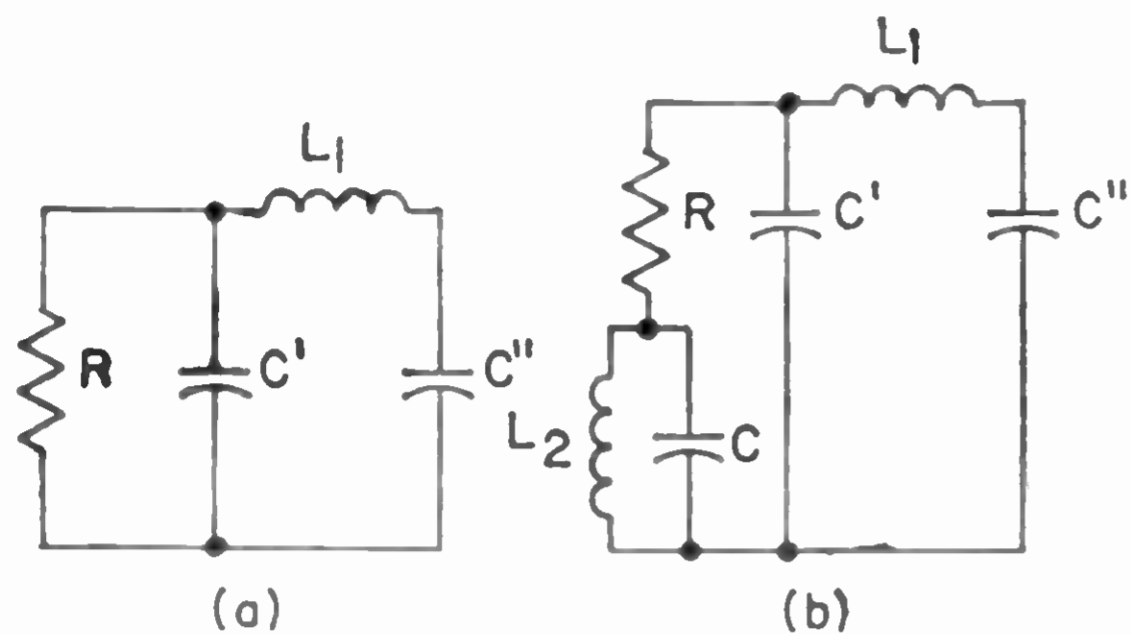


Fig. 178—Circuits using (a) series peaking, and (b) both self-resonant shunt peaking and series peaking.

a factor of two of each other, series peaking produces an appreciable improvement in frequency response as compared to shunt peaking. A more complex form of compensation embodying both self-resonant shunt peaking and series peaking is shown in Fig. 178(b).

The effects of various high-frequency compensation systems can be demonstrated by consideration of an amplifier consisting of three identical stages. If each of the three stages is down 3 dB at 1 MHz, and if a total gain variation of plus 1 dB and minus 3 dB is allowed, the bandwidth of the amplifier is 0.5 MHz without compensation. Shunt peaking raises the bandwidth to 1.3 MHz. Self-resonant shunt peaking raises it to 1.5 MHz. An infinitely complicated system could raise it to 2 MHz. If the distribution of capacitance permits it, series peaking alone can provide a bandwidth of about 2 MHz, while a combination of shunt and series peaking can provide a bandwidth of approximately 2.8 MHz. If the capacitance is perfectly distributed, and if an infinitely complex network of shunt and series peaking is employed, the ultimate capability is about 4 MHz.

The frequency response of a wideband amplifier is influenced greatly

by variations in component values due to temperature effects, variation of transistor parameters with voltage and current (normal large-signal excursions), changes of stray capacitance due to relocated lead wires, or other variations. A change of 20 per cent in any of the critical parameters can cause a change of 0.7 dB in gain per stage over the last half-octave of the response for the most simple case of shunt peaking. As the bandwidth is extended by more complex peaking, a circuit becomes substantially more critical. (Measurement probes generally alter circuit performance because of their capacitance; this effect should be considered during frequency-response measurements.)

In the design of wideband amplifiers using many stages of amplification, it is necessary to consider time-delay variations as well as amplitude variation. When feedback capacitance is a major contributor to response limitation, the more complex compensating networks may produce severe ringing or even sustained oscillation. If feedback capacitance is treated as input capacitance produced by the Miller effect, the added input capacitance C_i' caused by the feedback capacitor C_f is given by

$$C_i' = C_f (1 - VG)$$

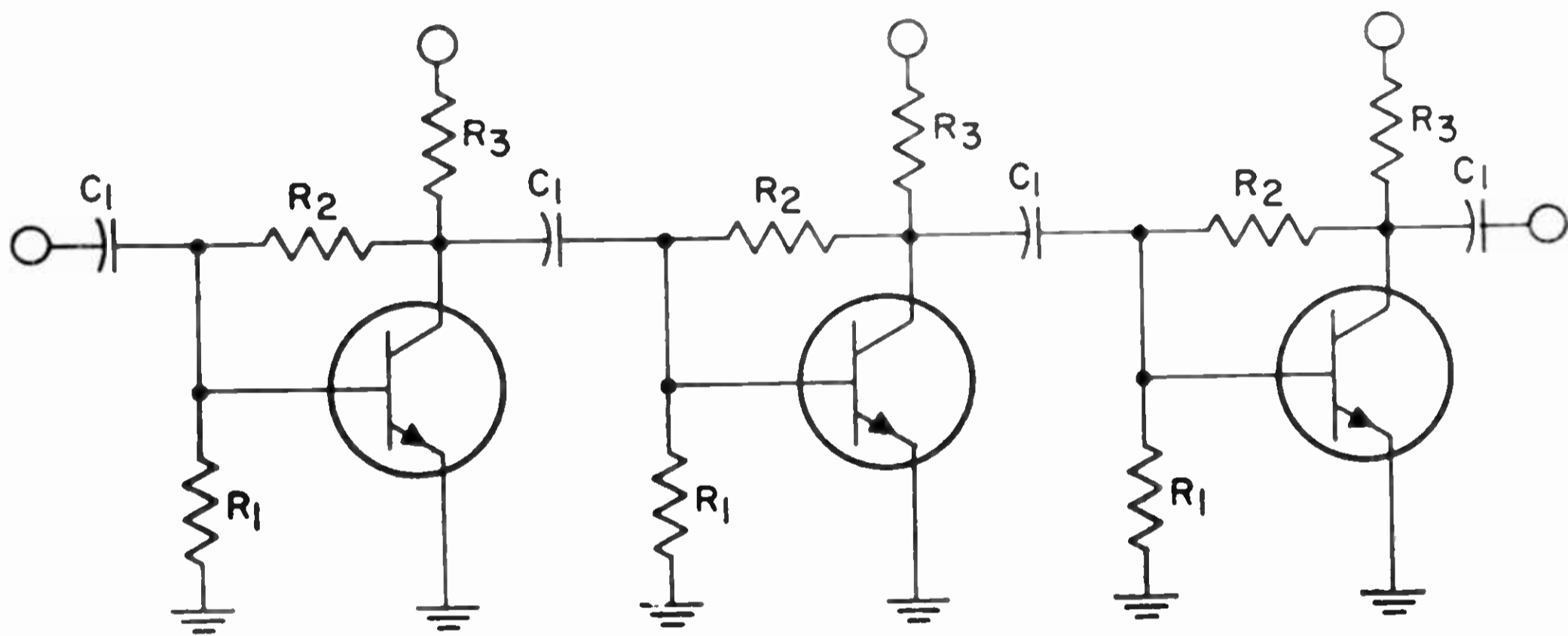
where VG is the input-to-output voltage gain. The gain VG , however, has a phase angle that varies with frequency. The phase angle is 180 degrees at low frequencies, but may lead or lag this value at high frequencies; the magnitude of VG then also varies. In the design of very wideband amplifiers (20 MHz or more), the phase of the transconductance g_m must be considered.

Fig. 179(a) shows three stages of a multistage wideband amplifier. The resistors R_b merely provide a high-impedance bias path for the collectors of the transistors. The ac collector current of each transistor normally flows almost exclusively into the relatively low impedance offered by the base of the next stage

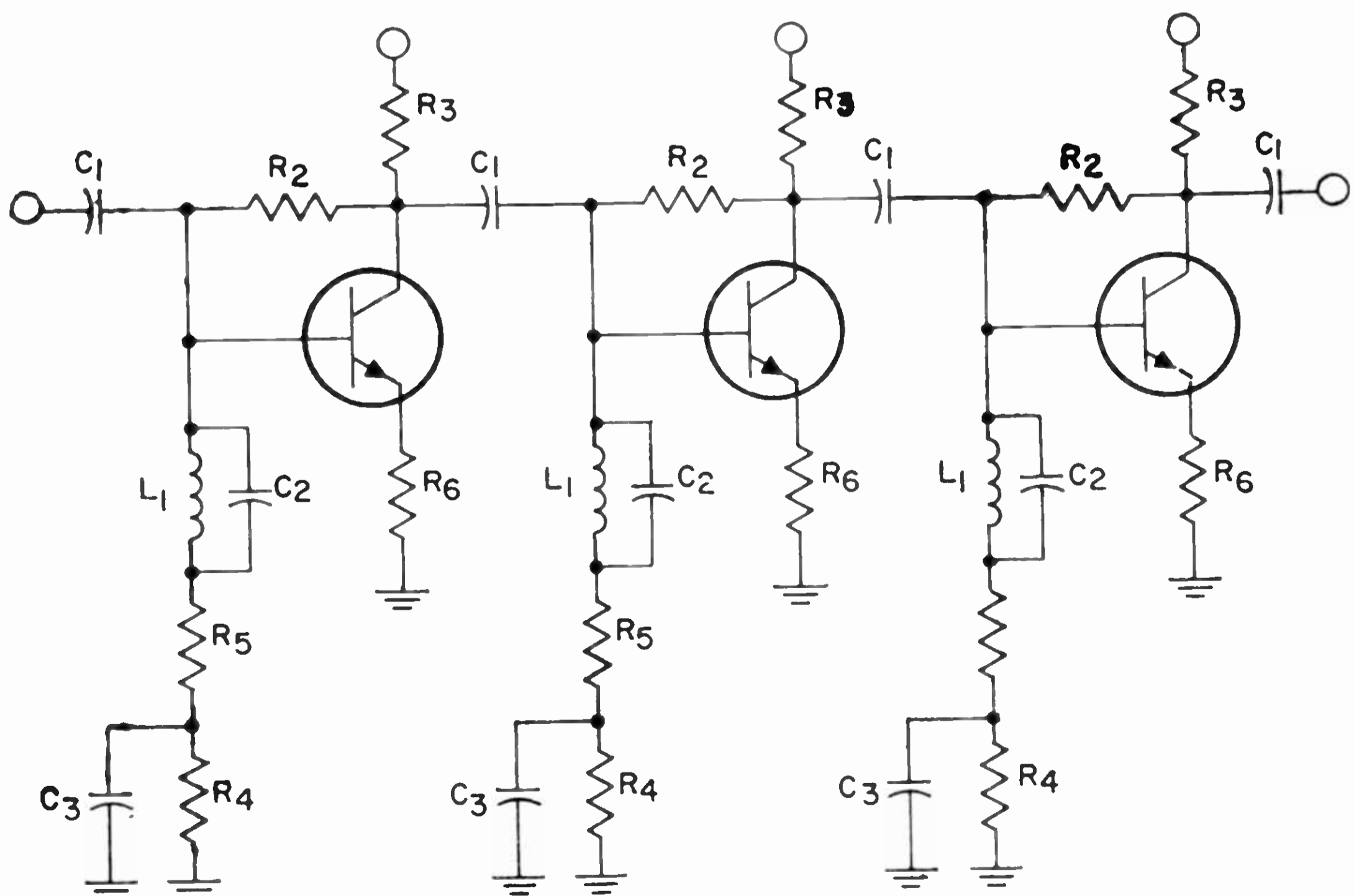
through the coupling capacitor C_1 . The resistive network R_1 and R_2 provides a stable dc bias for the transistor base.

The mid-frequency gain of each stage is approximately equal to the common-emitter current-transfer ratio (beta) of the transistor if the component values are properly chosen. The high-frequency response is limited primarily by the transistor gain-bandwidth product f_T , the transistor feedback capacitance, and sometimes the stray capacitance. The low-frequency response is limited primarily by the value of the coupling capacitor C_1 .

Fig. 179(b) illustrates the use of high-frequency shunt peaking and low-frequency peaking at the expense of stage gain in the three stages of the wideband amplifier to extend the high- and low-frequency response. The emitter resistors R_6 are made as small as possible, yet large enough to mask the variation of transconductance, and thus voltage gain, as a function of signal-current variation. For very small ratios of peak ac collector current to dc collector current, this variation is not substantial. The resistors R_6 also partially mask the effect of the intrinsic base-lead resistance r_b' .



(a)



(b)

Fig. 179—(a) Uncompensated and (b) compensated versions of three stages of a multi-stage wideband amplifier.

The base-bias resistors R_1 of Fig. 179(a) are split into two resistors R_4 and R_5 in Fig. 179(b), with R_4 well bypassed. The mid-frequency gain is then reduced to a value approximating R_5 divided by R_6 . At this point, however, the high-frequency response is increased by the same factor. Shunt peaking is provided by L_1 and C_2 for additional high-frequency improvement.

When the reactance of the bypass capacitor C_3 is large compared to R_5 , the low-frequency gain is increased because the resistor no longer heavily shunts the transistor input. Selection of the proper value for C_3 exactly offsets the loss of low-frequency gain caused by C_1 . When the reactance of C_3 approaches R_4 , however, the low-frequency peaking is no longer effective.

RF Power Amplifiers

One of the most common uses of high-frequency power amplifiers is in radio transmitters. In one section of the transmitter, an rf signal of the desired frequency is developed in an oscillator stage and amplified in one or more rf-amplifier stages. The audio-frequency (af) modulating signal is impressed on the rf carrier in the final rf-power-amplifier stage (high-level modulation), in the rf low-level stage (low-level modulation), or in both. Fig. 180 shows a simplified block diagram of the transmitter portion of a citizens-band transceiver that operates at a frequency of 27 MHz.

Fig. 181 shows the schematic diagram of a linear wideband amplifier designed to operate over the

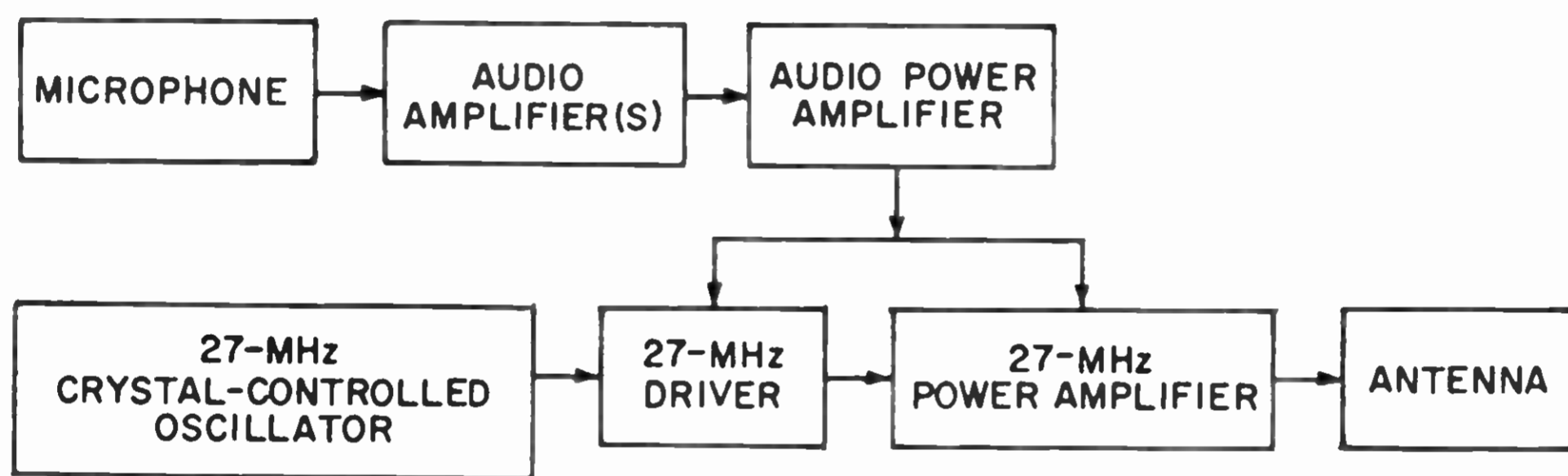


Fig. 180—Simplified block diagram for the transmitter portion of a 27-MHz communications transceiver.

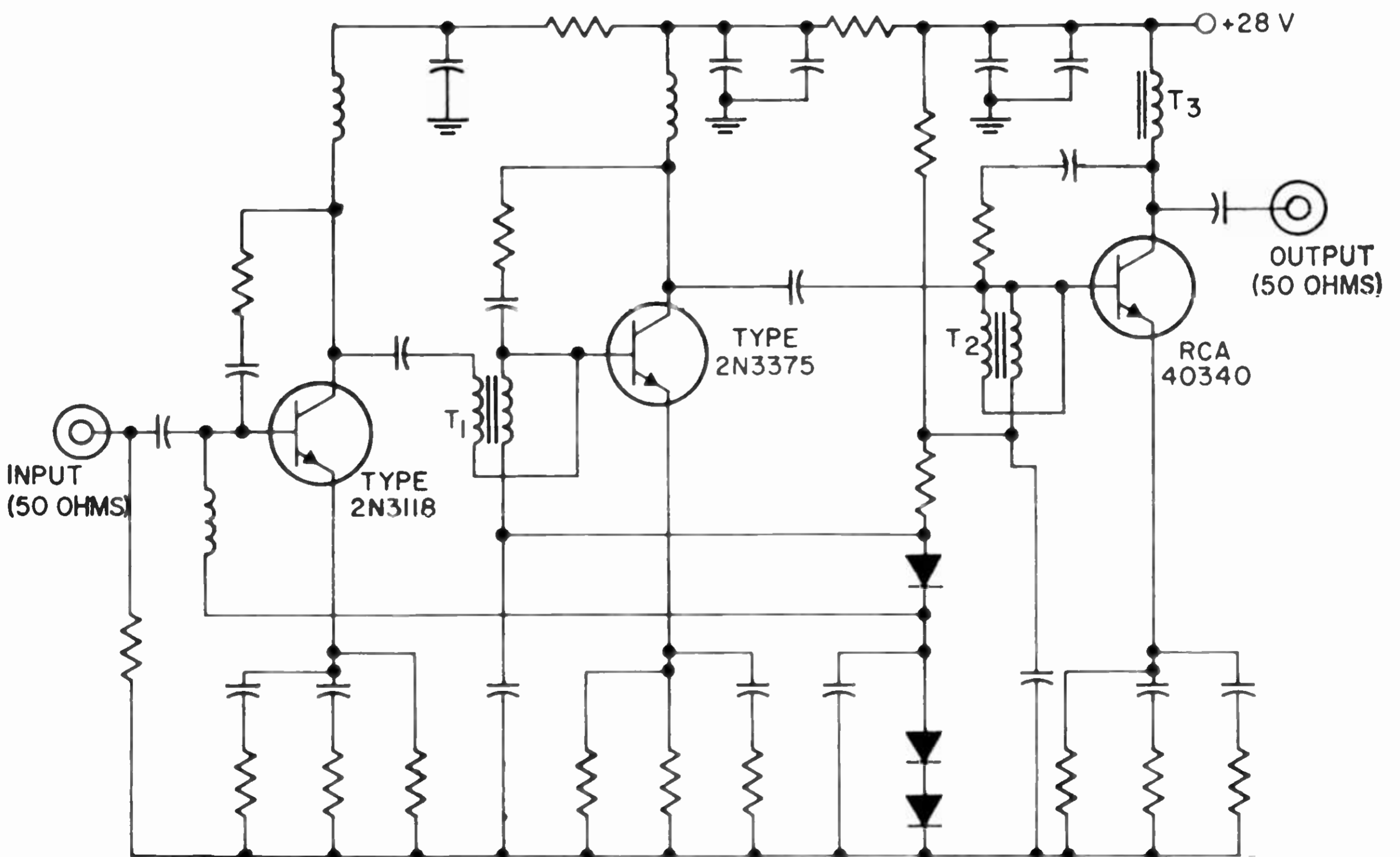


Fig. 181—2-to-30-MHz linear power amplifier.

frequency range from 2 to 30 MHz in a single-sideband transmitter. The main advantages of a single-sideband transmitter are reduced power consumption with respect to the effective transmission, reduced channel width to permit more transmitters to be operated within a given frequency range, and improved signal-to-noise ratio. Most commercially available rf power transistors are normally designed for class C operation. Transistors designed for single-sideband operation, however, are required to operate in the linear mode and, therefore, should have a flat beta curve. Emitter ballast resistors are usually employed with these transistors to assure circuit stability and low distortion.

Most transmitters used in the 30-to-76-MHz communications band are frequency-modulated. Fig. 182 shows the schematic diagram of a wideband rf amplifier using an overlay transistor. With an input drive of 3 watts, an amplifier of this type can provide a minimum power output of 15 watts across the frequency band. The collector efficiency of the amplifier can be greater than 35 per cent.

One of the most obvious applications for broadband transmitters is

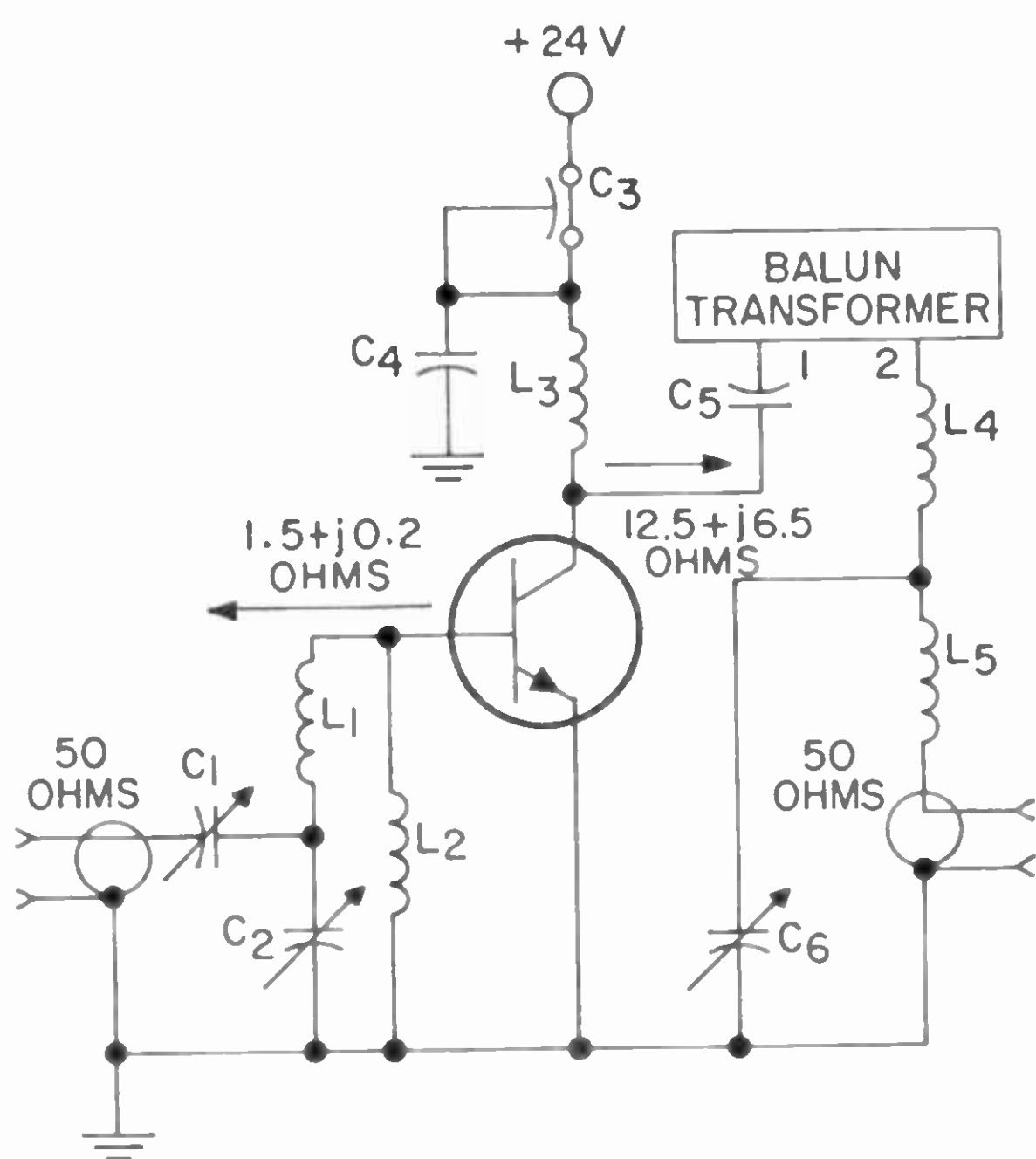


Fig. 182—Wideband (30-to-76-MHz) rf-amplifier circuit.

in the aircraft-radio frequency band. The flight crew must be able to communicate with any airport that they service and to change rapidly from communication to navigational channels. The necessity for broadband performance precludes the use of sharply tuned circuits to reduce the harmonic power in the output signal. Instead, harmonic reduction is achieved by use of low-pass filters.

Fig. 183 shows a broadband amplifier that uses a push-pull output to reduce harmonics. An amplifier of this type can develop a peak envelope power (PEP) output of 40 watts from a 12.5 volt dc supply.

The advent of all-solid-state mobile transmitters is the result mainly of advances in rf power transistor capability. The development of vhf silicon power transistors made possible the design of all-solid-state mobile transmitters for operation in the 25-to-50-MHz frequency band. Initially, the design of such transmitters operating at frequencies as high as 175 MHz required the use of varactor frequency multipliers. Solid-state uhf transmitters really became practical with the introduction of the overlay transistor. Low-voltage versions of overlay transistors led to the design of uhf transmitters that operate directly from a vehicle 12-volt electrical system.

Fig. 184(a) shows a 175-MHz amplifier chain that operates directly from a 12-volt dc supply. An amplifier chain of this type can deliver 12 watts of output power with an input of 125 milliwatts and has an over-all efficiency of 60 per cent. The chain consists of three cascaded stages that provide power outputs of 1, 4, and 12 watts, respectively. For applications such as base stations in which higher output power levels are required, three overlay power transistors can be operated in parallel as shown in Fig. 184(b). In this arrangement, the transistors can supply as much as 35 watts at 175 MHz when driven

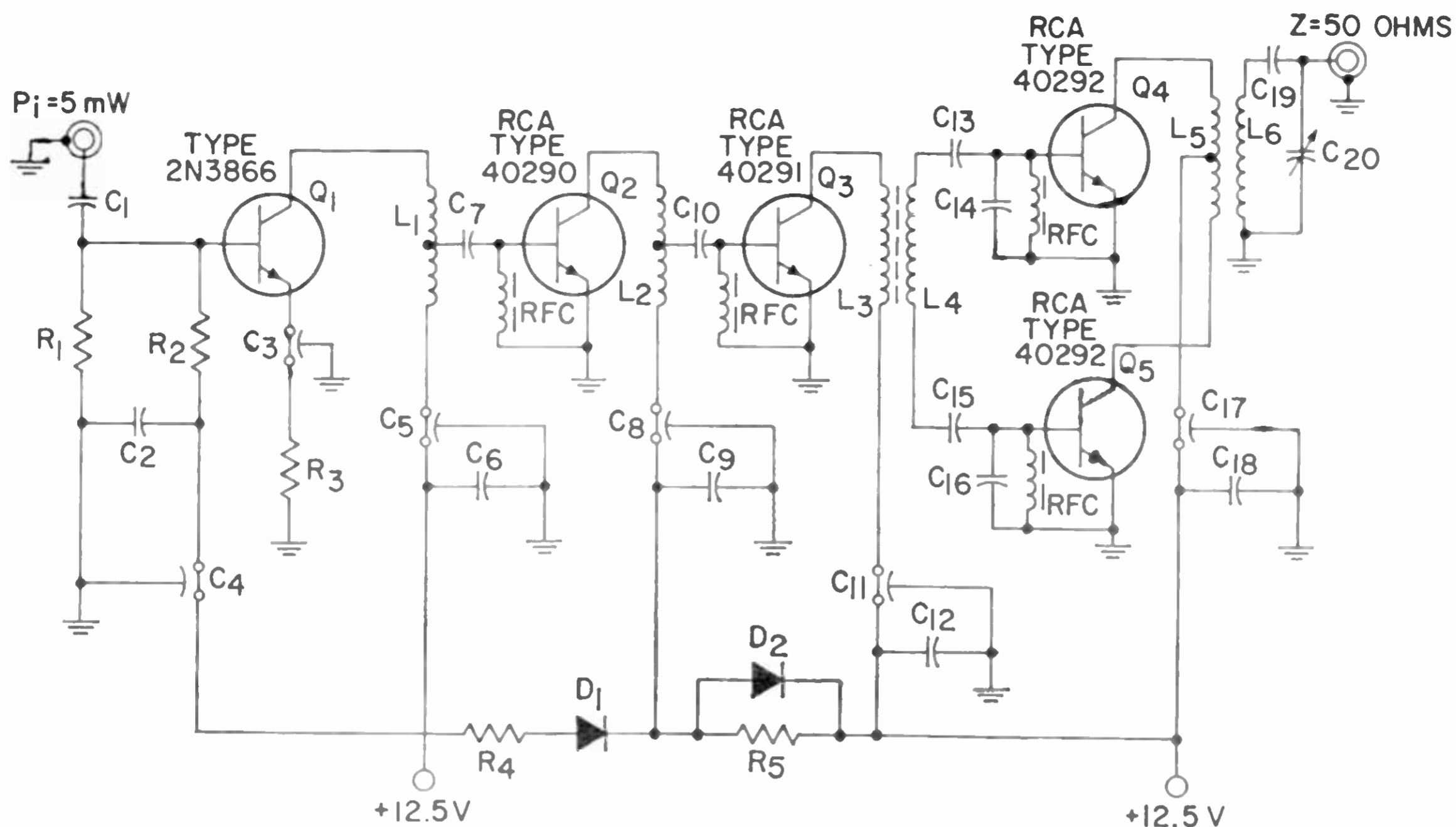


Fig. 183—118-to-136-MHz broadband amplifier.

from the three-stage amplifier chain shown in Fig. 184(a).

The requirements of rf power transistors operated in mobile-radio applications are extremely severe. The transistors must withstand the load-mismatch conditions created by objects near the transmitting antenna or by a break in the transmission line anywhere between zero and one-half wavelength. Under such conditions, the transistors must handle not only the increased dissipation, but also sudden energy surges that can destroy them in just a few microseconds. The development of transmitters that are immune to these failures is a result of a joint effort between semiconductor-device and mobile-radio manufacturers. To avoid excessive junction temperatures, the equipment manufacturer must select transistors of sufficiently low thermal resistance. If a transistor lacks enough dissipation capability, two should be used—even though one could deliver the required rf output power. The use of adequately sized heat sinks is essential to protect devices operated under high-ambient-temperature conditions. Current limiting should also be employed to prevent excessive rise in junction temperature under mismatched load

conditions. As an added precaution, a thermostat can be mounted on the heat sink to reduce the transmitter power in the event that the temperature becomes excessive.

The protection of the devices from “instantaneous” failure is more difficult because the time response of current or voltage limiters is not fast enough. Proper biasing of the emitters of transistors operating from 24-to-28-volt supplies helps to prevent this type of failure. Fig. 185 shows a circuit which has a sufficiently fast response time to protect the power transistors from “instantaneous” failures that result from mismatched-load conditions. This circuit operates on the principle of reflected power. Under matched load conditions, there is no output from the VSWR detector. The control amplifier is saturated, and the gain-controlled rf amplifier operates at maximum gain. The power amplifier, therefore, is operated at maximum power output. If a mismatch occurs, a negative voltage from the VSWR bridge brings the control amplifier out of saturation, which, in turn, reduces the gain in the gain-controlled rf amplifier. Gain is reduced because the base of the rf amplifier becomes more negative with respect to the emitter,

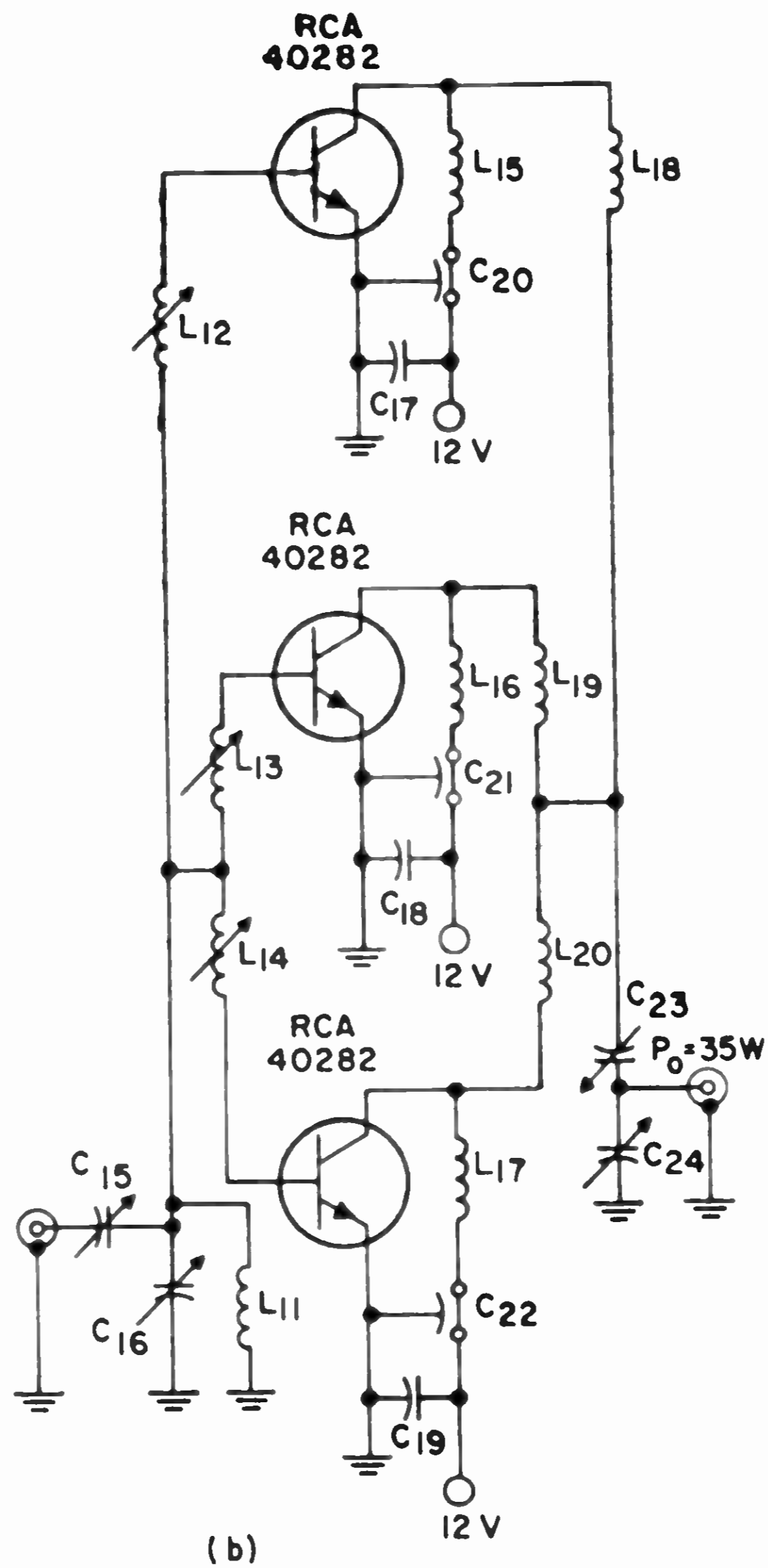
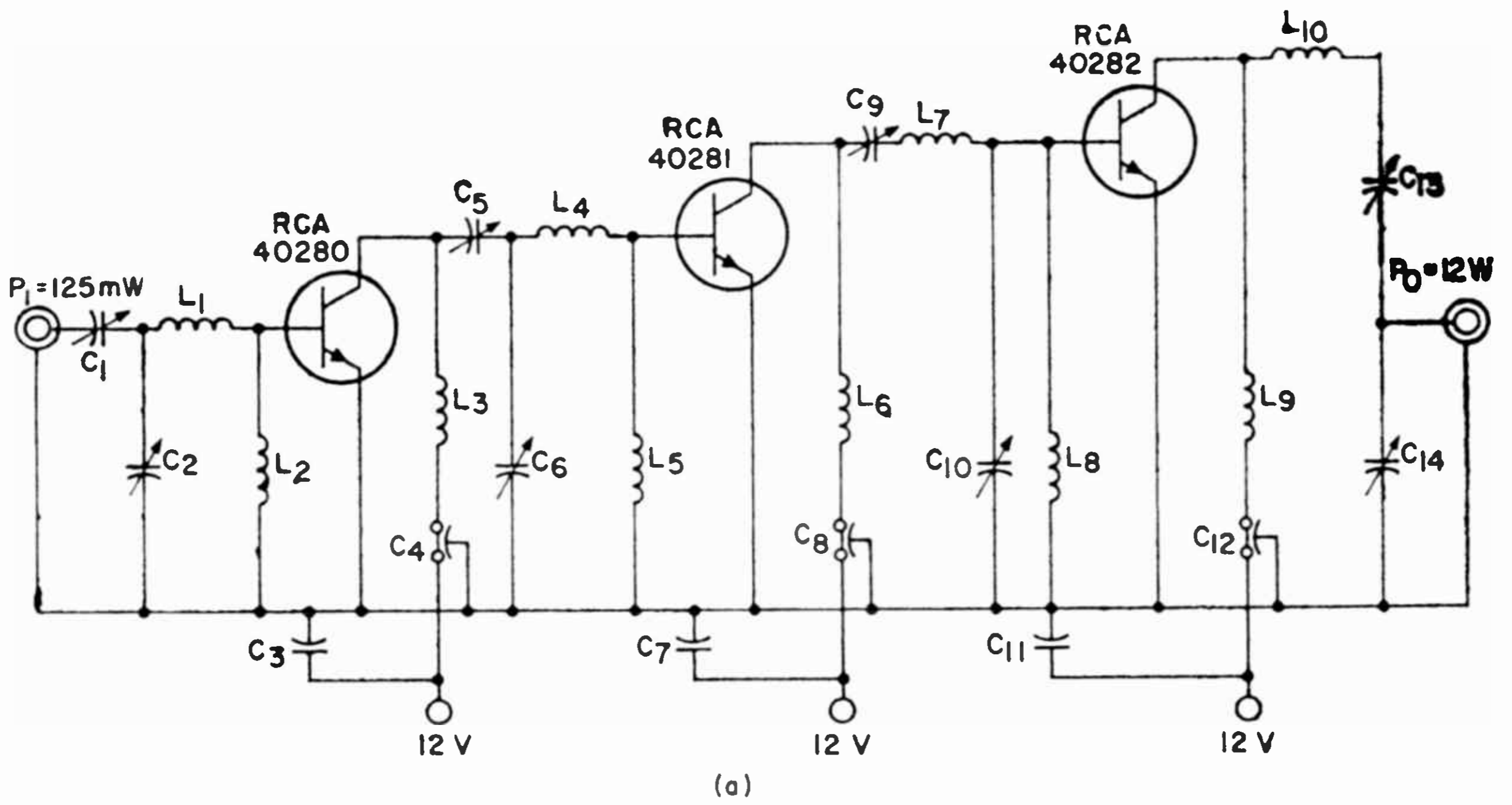


Fig. 184—175-MHz transistor power amplifier: (a) 3-stage input amplifier; (b) output stage.

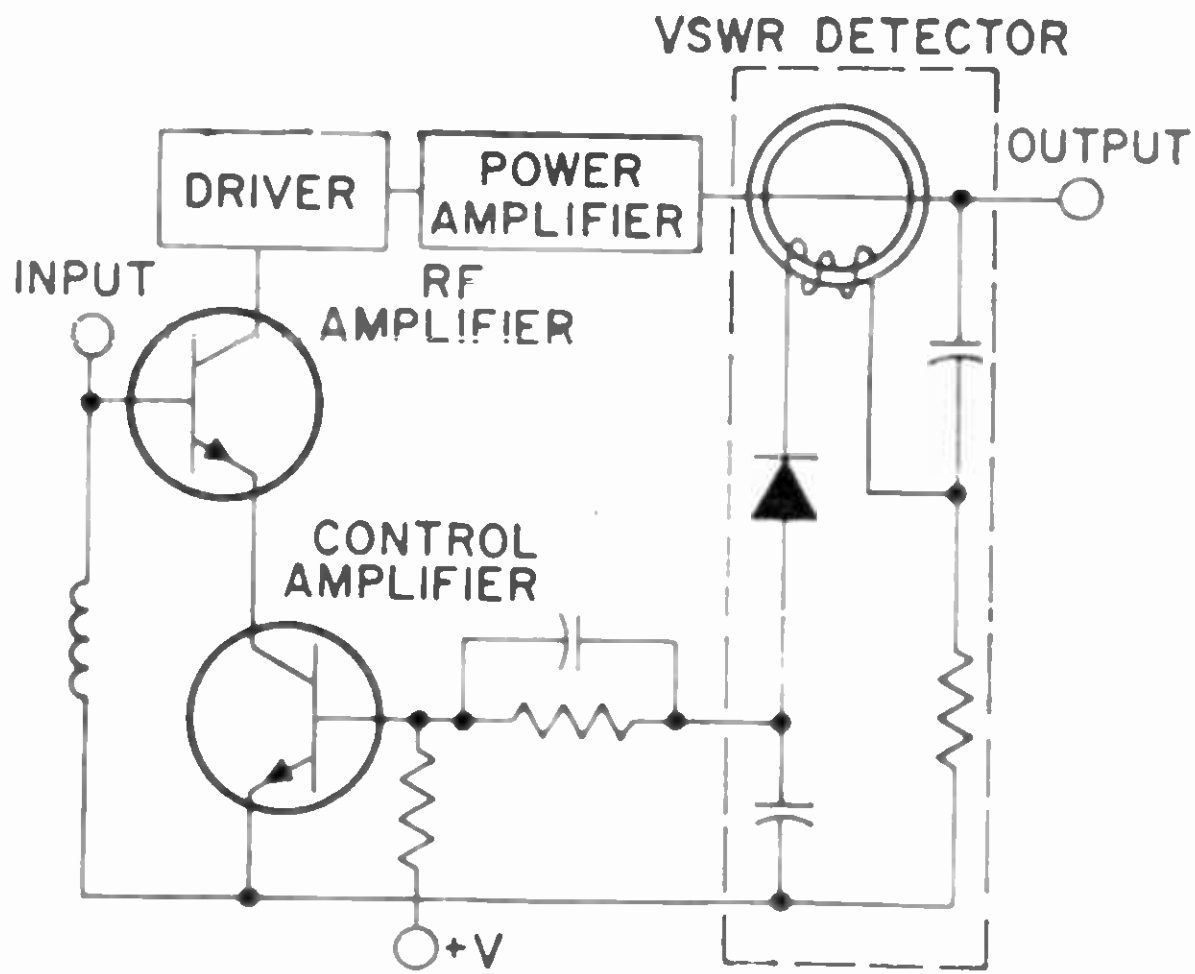


Fig. 185—Load-mismatch protection circuit.

and because the unsaturated control amplifier has a degenerative effect on the rf amplifier. With the reduction in the gain of the gain-controlled rf amplifier, the drive to the power amplifier is decreased to safe levels. Once the load mismatch is removed, the system returns instantaneously to normal operating conditions.

UHF Power Generation

When a transistor is operated in a uhf power amplifier, the objective is usually to obtain as much power output as possible with good collector efficiency, a minimum of harmonic distortion, and reasonable bandwidth. The following transistor requirements are important to the circuit designer:

- (a) maximum collector dissipation;
- (b) maximum peak collector current;
- (c) maximum collector voltage;
- (d) input and output impedance or admittance characteristics;
- (e) high-frequency current-gain figure of merit f_T .

The most important consideration in the design of an rf power amplifier is, of course, the power-dissipation capability of the transistor. The maximum power that can be dissipated before thermal runaway occurs depends to a great extent on how well the heat generated within the transistor is removed. When heat is removed by conduction, the

amount removed is an inverse function of the thermal resistance. A good rf power transistor, therefore, is characterized by a low value of thermal resistance.

An rf transistor must be capable of handling high peak collector currents to provide substantial power output. The maximum peak-collector-current rating is usually limited primarily by the practical consideration that the current amplification factor varies inversely with emitter current at high values of emitter-current density. The maximum peak-collector-current rating, therefore, may be established by the amount of reduction in current gain which can be tolerated at high frequencies.

The maximum collector-voltage rating of an rf power transistor must be sufficiently high to avoid breakdown under conditions of strong reactive loading. The rf transistor must be capable of withstanding high VSWR without collector-junction breakdown.

Under large-signal conditions, the instantaneous values of the input and output impedances or admittances vary considerably over the range of applied signal level and operating frequency. The circuit designer must know the character of the input and output impedances or admittances as a function of both current and frequency if proper coupling networks are to be designed.

The high-frequency current-gain figure of merit (f_T) is essential in determination of the power-gain capability of a particular rf power transistor. The f_T of an rf transistor varies with dc emitter current and usually decreases at very high levels of current. A good rf power transistor should be characterized by a high value of f_T at high levels of dc emitter or collector current.

One of the main factors that restricts the bandwidth of a uhf transistor amplifier is the parasitic inductances of the package. This restriction can be overcome by circuit techniques that compensate for the

inductance, such as the broadband lumped-constant reactive-ladder network used in both input and output circuits in Fig. 186. With an arrangement of this type, parasitic lead inductances are not restrictive provided that the design tradeoff between bandwidth and input reflective power is acceptable.

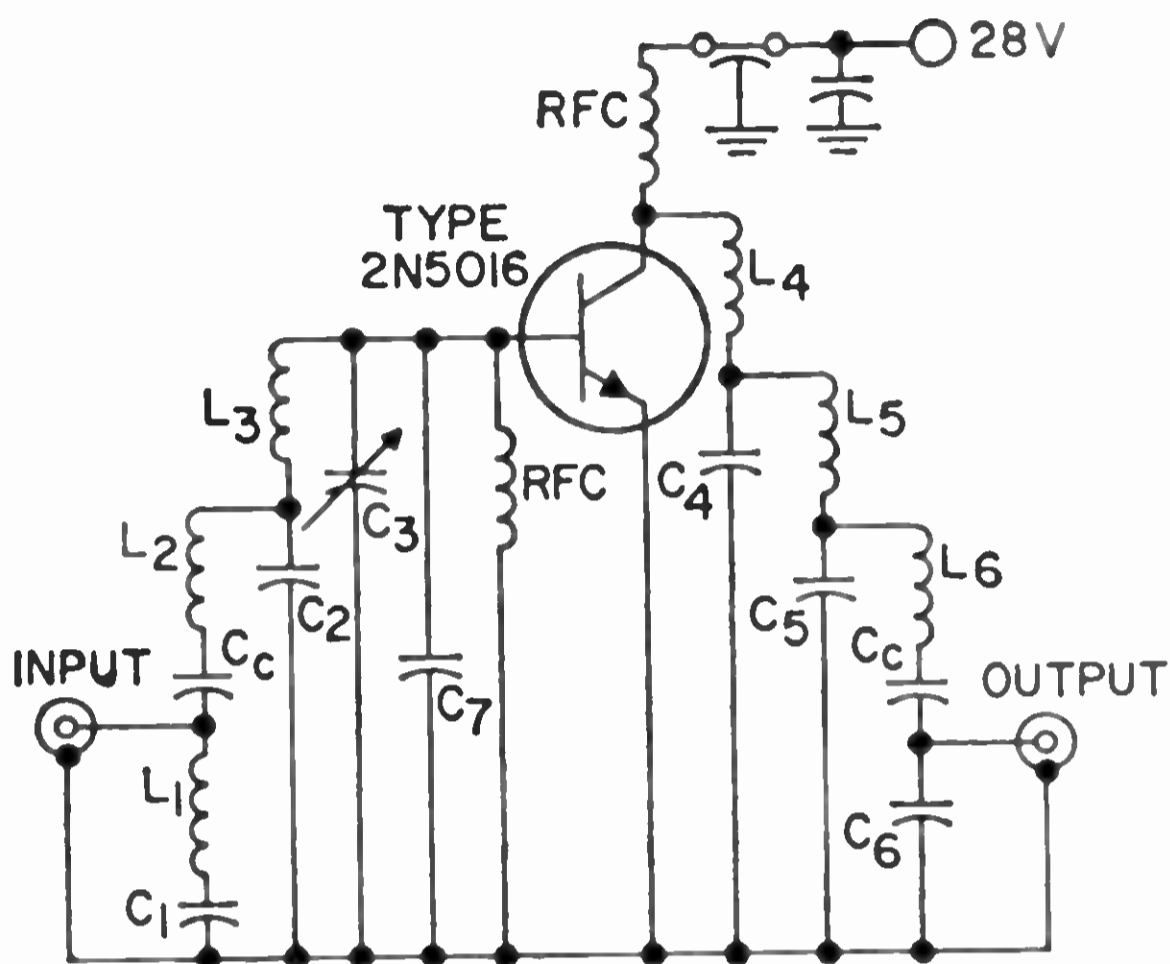


Fig. 186—Lumped-constant 225-to-400 power amplifier.

Microwave Power Applications

A significant breakthrough in solid-state microwave power generation was made by introduction of the RCA overlay transistor. This transistor will deliver 1 watt of output power at 2 GHz in a suitable amplifier. The complete circuit diagram of such an amplifier is shown in Fig. 187, and construction details are given in Fig. 188.

The input section consists of capacitance C_1 and a line section. The output section consists of a line section, capacitance C_3 , and a capacitance C_4 .

A cw power output of 1 watt at a gain of 5 dB can be obtained in this circuit with the grounded-base coaxial transistor operated at a collector voltage of 28 volts. The collector efficiency measured at a power-output level of 1 watt is higher than 35 per cent. The 3-dB bandwidth measured at the same power level is greater than 5 per cent.

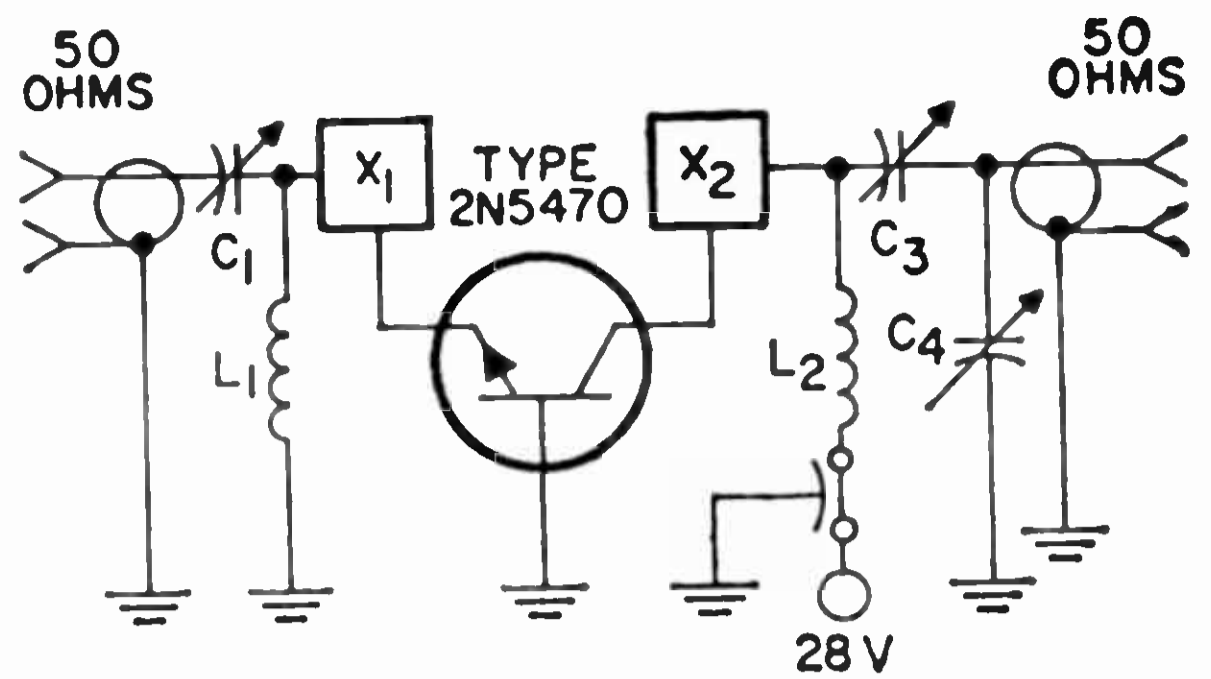


Fig. 187—Typical circuit for 2GHz, coaxial-line power amplifier.

Because tunnel diodes can operate effectively at frequencies above 300 MHz, they are particularly suitable for use in microwave amplifiers and oscillators. In microwave amplifier circuits, tunnel diodes offer low noise, as well as small size and weight, low cost, and low power drain. In addition, bandwidths in excess of an octave can readily be obtained because of the wideband negative-resistance characteristic of tunnel diodes. However, this wideband negative resistance makes stabilization an important problem in the design of microwave tunnel-diode amplifiers.

In microwave oscillator circuits, tunnel diodes can provide useful power outputs at frequencies as high as 5000 MHz. Compared to vacuum-tube microwave oscillators, tunnel-diode oscillators are inexpensive, require only a fraction of a volt dc bias, and are rugged and reliable in severe environments. Compared to transistor-driven varactor frequency-multiplier circuits, they are simple and compact, and afford higher dc-to-rf conversion efficiencies. (More detailed information on microwave tunnel-diode applications, is given in the RCA TUNNEL-DIODE MANUAL TD-30.)

OSCILLATION

Bipolar and field-effect transistor oscillator circuits are similar in many respects to the amplifiers discussed previously, except that a portion of the output power is returned to the input network in phase with the starting power (re-

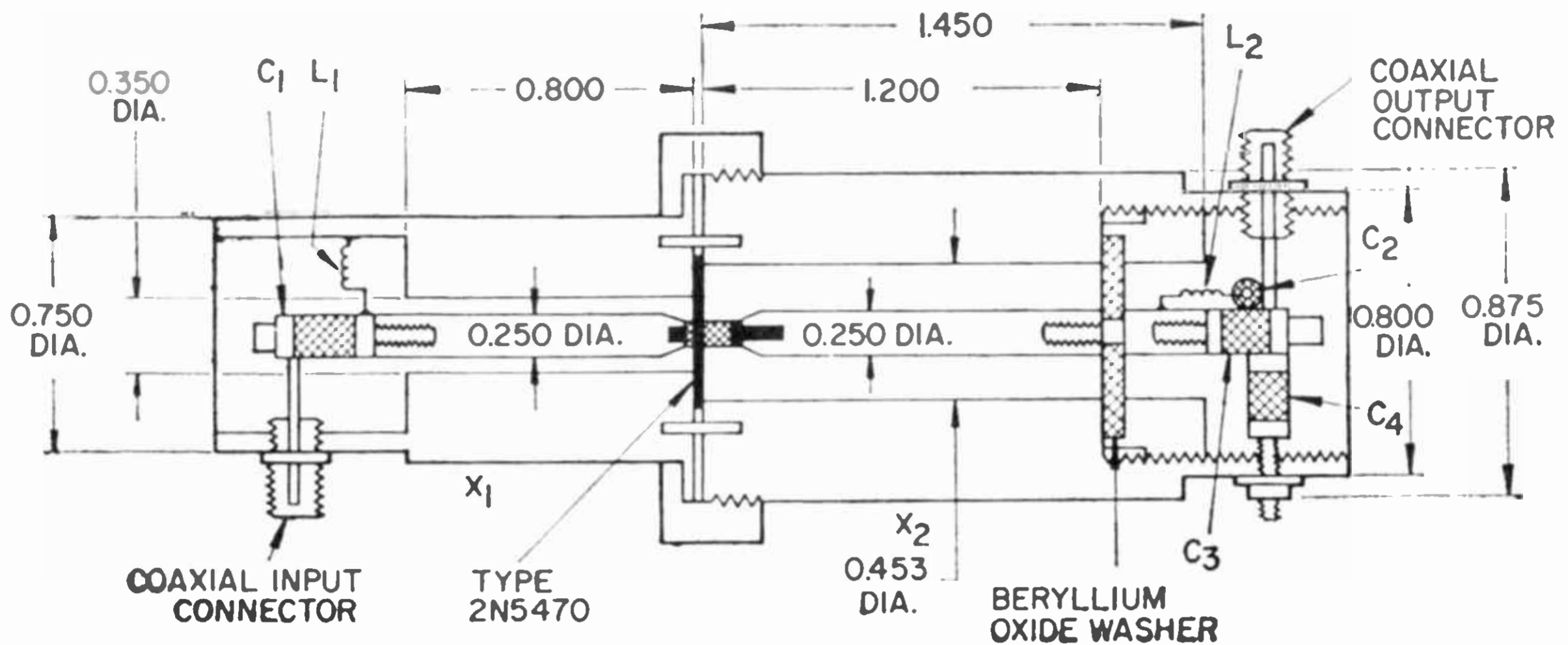


Fig. 188—Constructional details of 2-GHz power amplifier in Fig. 186.

generative or positive feedback) to sustain oscillation. DC bias-voltage requirements for oscillators are similar to those discussed for amplifiers.

The maximum operating frequency of an oscillator circuit is limited by the frequency capability of the transistor used. The maximum frequency of oscillation of a transistor is defined as the frequency at which the power gain is unity. Because some power gain is required in an oscillator circuit to overcome losses in the feedback network, the operating frequency must be some value below the transistor maximum frequency of oscillation.

For sustained oscillation in a transistor oscillator, the power gain of the amplifier network must be equal to or greater than unity. When the amplifier power gain becomes less than unity, oscillations become smaller with time (are “damped”)

until they cease to exist. In practical oscillator circuits, power gains greater than unity are required because the power output is divided between the load and the feedback network, as shown in Fig. 189. The feedback power must be equal to the input power plus the losses in the feedback network to sustain oscillation.

LC Resonant Feedback Oscillators

The frequency-determining elements of an oscillator circuit may consist of an inductance-capacitance (LC) network, a crystal, or a resistance-capacitance (RC) network. An LC tuned circuit may be placed in either the base circuit or the collector circuit of a common-emitter transistor oscillator. In the tuned-base oscillator shown in Fig. 190, one battery is used to provide all the

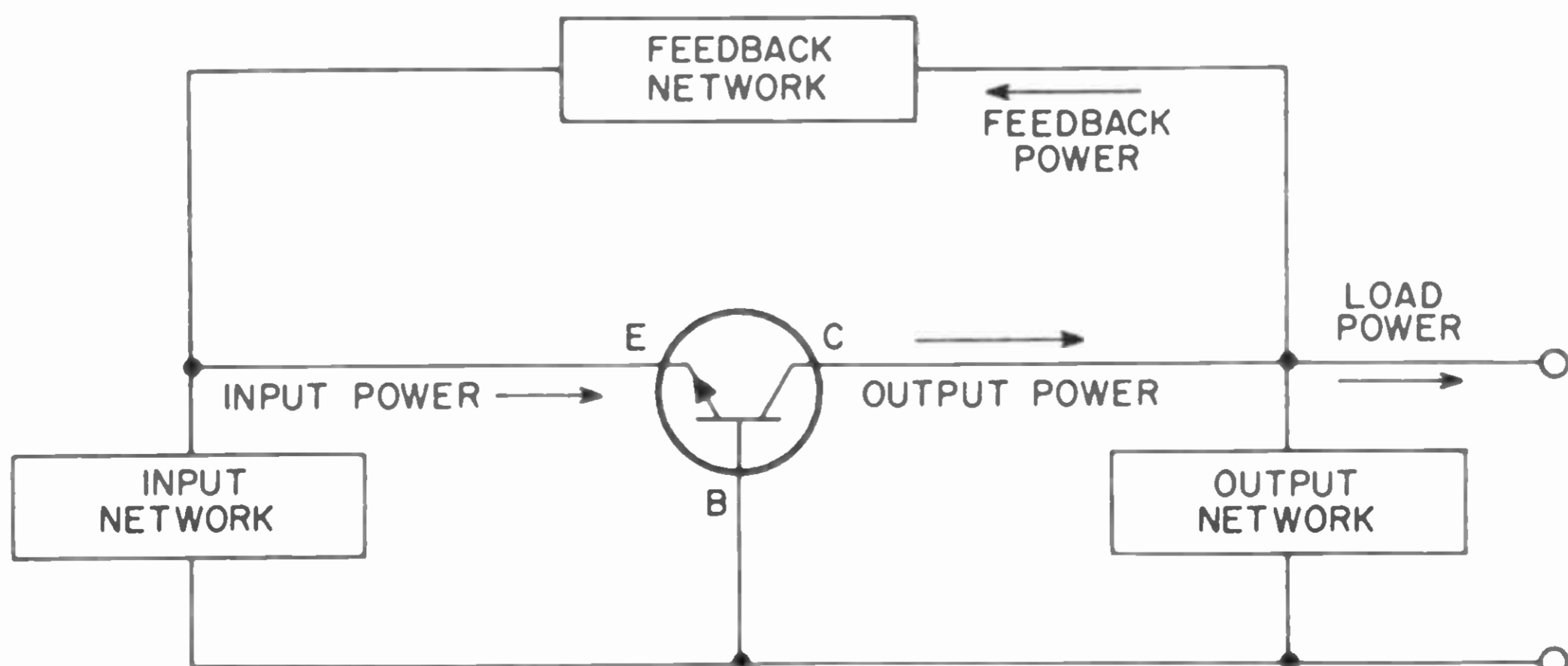


Fig. 189—Block diagram of transistor oscillator showing division of output power.

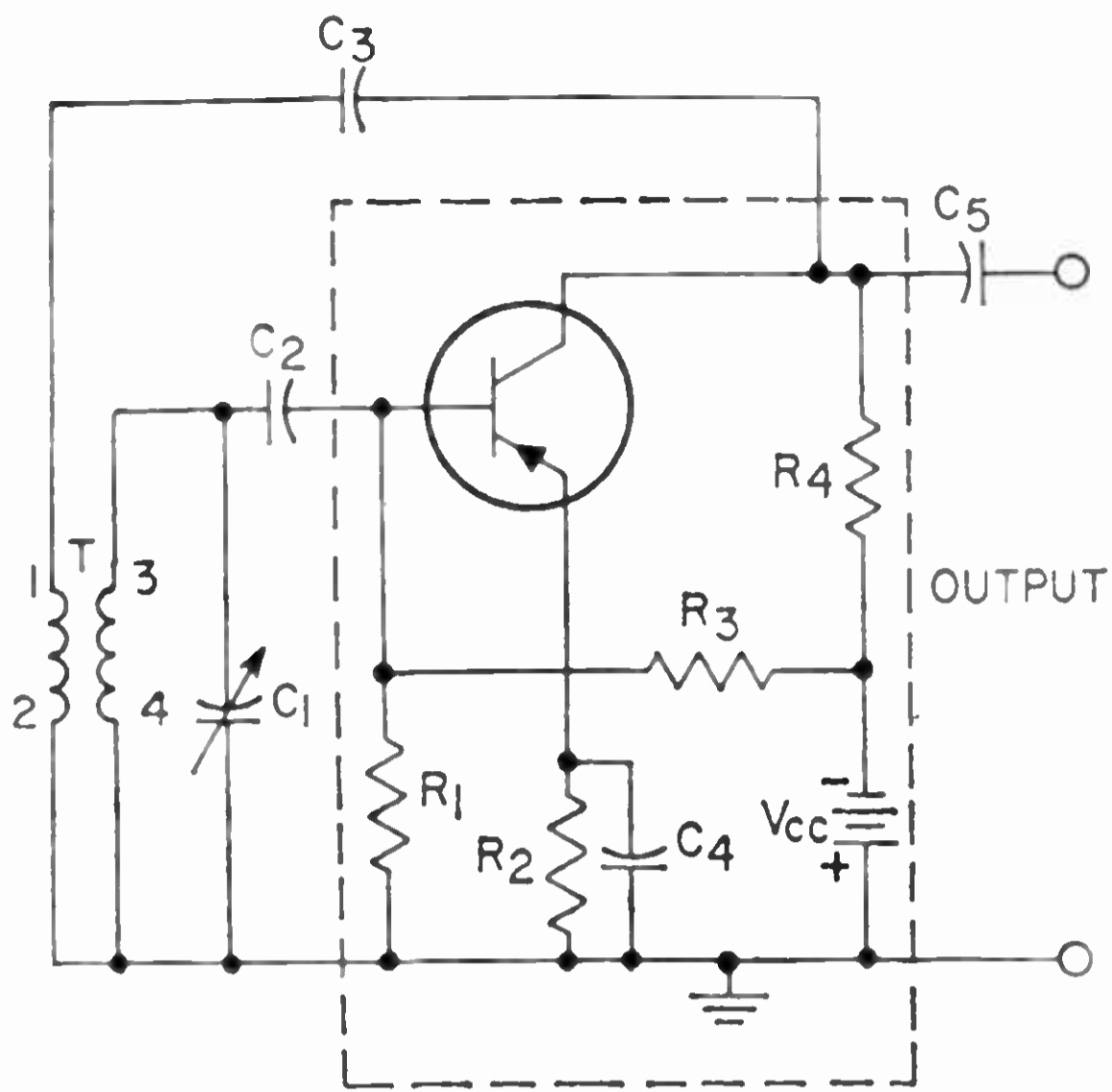


Fig. 190—Tuned-base oscillator.

dc operating voltages for the transistor. Resistors R_1 , R_3 , and R_4 provide the necessary bias conditions. Resistor R_2 is the emitter stabilizing resistor. The components within the dotted lines comprise the transistor amplifier. The collector shunt-feed arrangement prevents dc current flow through the tickler (primary) winding of transformer T. Feedback is accomplished by the mutual inductance between the transformer windings.

The tuned circuit consisting of the secondary winding of transformer T and variable capacitor C_1 is the frequency-determining element of the oscillator. Variable capacitor C_1 permits tuning through a range of frequencies. Capacitor C_2 couples the oscillation signal to the base of the transistor, and also blocks dc. Capacitor C_4 bypasses the ac signal around the emitter resistor R_3 and prevents degeneration. The output signal is coupled from the collector through coupling capacitor C_5 to the load.

A tuned-collector transistor oscillator is shown in Fig. 191. In this circuit, resistors R_1 and R_3 establish the base bias. Resistor R_2 is the emitter stabilizing resistor. Capacitors C_1 and C_2 bypass ac around resistors R_1 and R_2 , respectively. The tuned circuit consists of the primary winding of transformer T and the

variable capacitor C_3 . Regeneration is accomplished by coupling the feedback signal from transformer winding 3-4 to the tickler coil winding 1-2. The secondary winding of the transformer couples the signal output to the load.

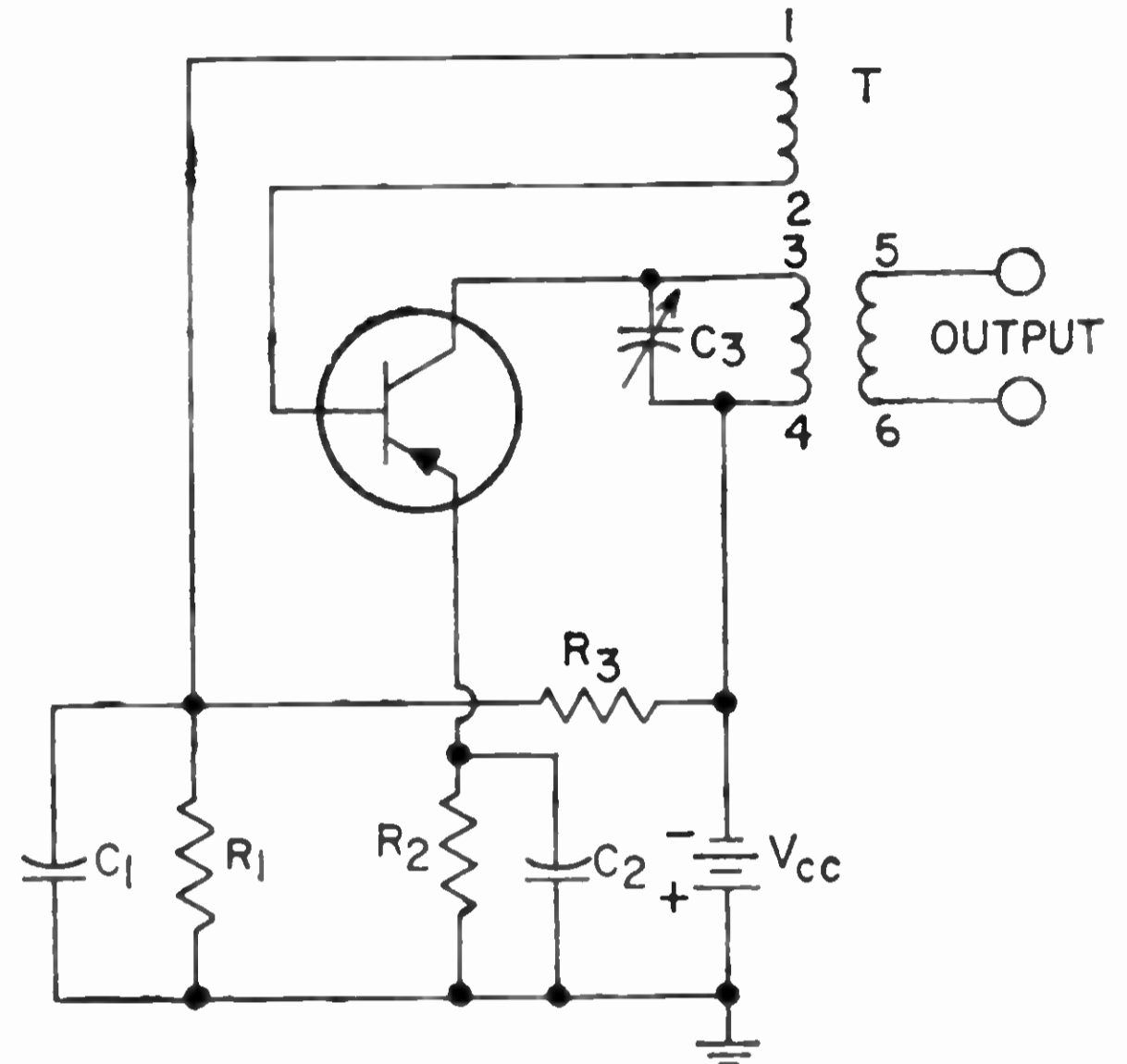


Fig. 191—Tuned-collector oscillator.

Another form of LC resonant feedback oscillator is the Hartley oscillator. This oscillator makes use of split inductance to obtain feedback and may be either shunt or series fed. In the shunt-fed circuit of Fig. 192, R_1 , R_2 , and R_3 are the biasing resistors; the frequency-determining network consists of variable capacitor C_1 in series with the windings of T. The frequency of the oscillator is varied by C_1 ; C_2

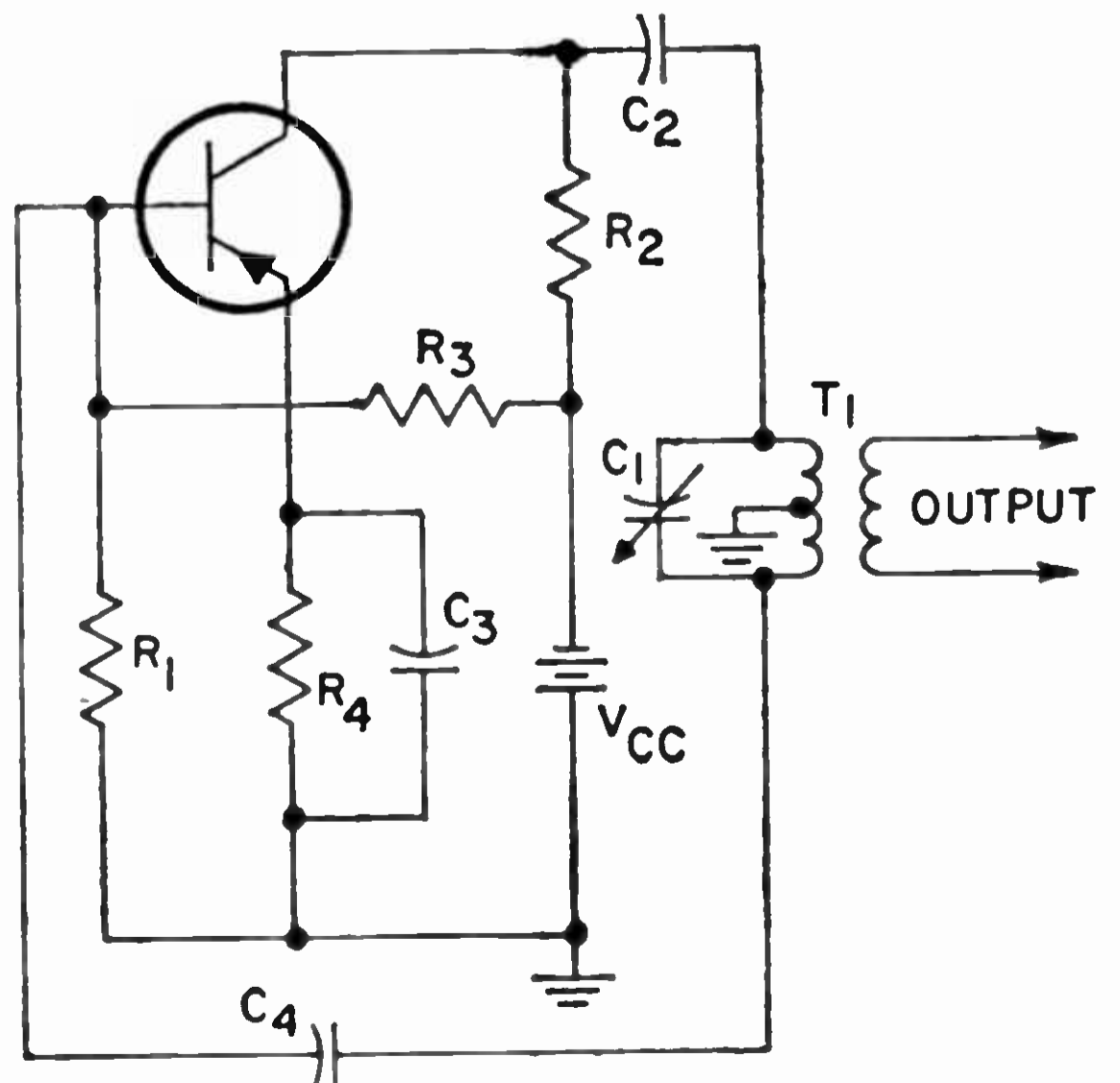


Fig. 192—Shunt-fed Hartley oscillator.

is the dc blocking capacitor and C_3 is an ac bypass capacitor.

The circuit inductance functions in the manner of an auto transformer and provides the regenerative feedback signal obtained from the voltage induced in the lower half of the transformer winding and coupled through C_1 to the transistor base. No dc current flows through the primary of T_1 because the collector is shunt fed through R_2 .

In the series-fed Hartley circuit shown in Fig. 193, the base-emitter circuit is biased through R_1 and R_2 ;

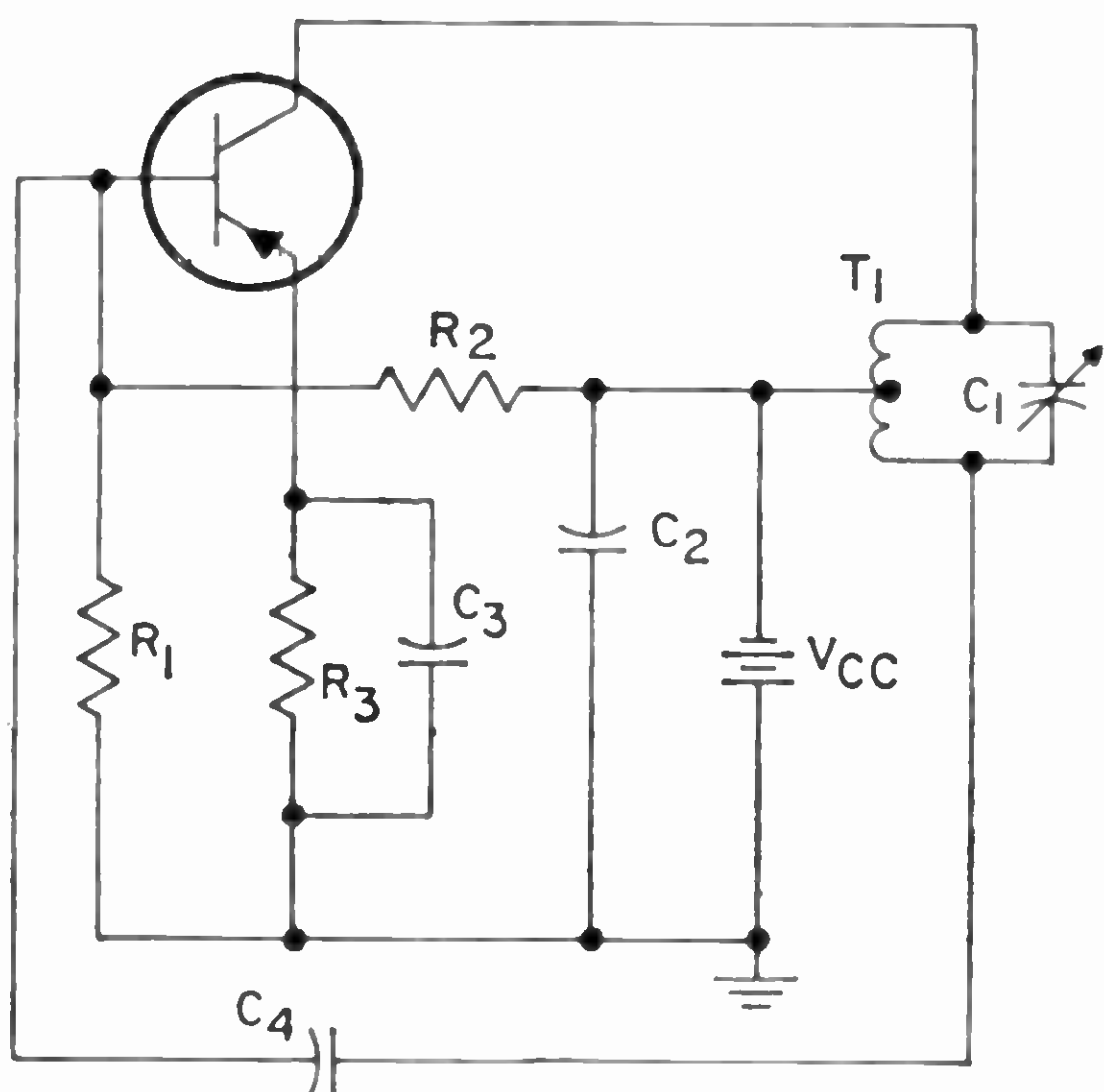


Fig. 193—Series-fed Hartley oscillator.

the collector is biased through the upper half of the transformer windings. Again, as in the shunt-fed circuit, C_3 provides an ac bypass. Feedback in the series-fed Hartley circuit is obtained from the lower-half of the transformer winding and is coupled through C_1 to the base of the transistor. The center-tap of the transformer winding is maintained at ac ground potential by C_2 .

Fig. 194 shows two arrangements of a Hartley oscillator circuit using MOS field-effect transistors. Circuit (a) utilizes a bypassed source resistor to provide proper operating conditions; circuit (b) utilizes a gate-leak resistor and biasing diode. The amount of feedback in either circuit is dependent on the position of the tap on the coil. Too little feedback results in a feedback signal voltage at the gate insufficient

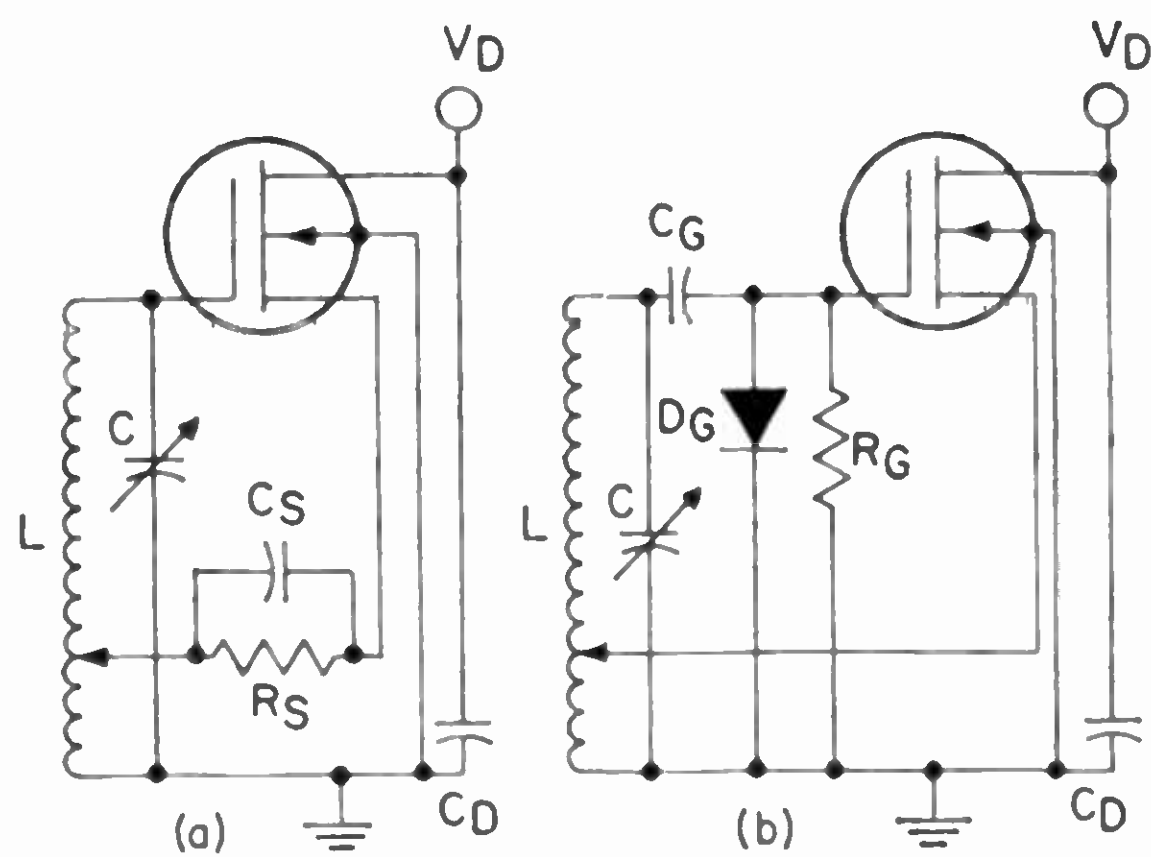


Fig. 194—Hartley oscillator circuits using MOS transistors.

to sustain oscillation; too much feedback causes the impedance between source and drain to become so low that the circuit becomes unstable. Output from these circuits can be obtained through inductive coupling to the coil or through capacitive coupling to the gate.

Another form of LC resonant feedback oscillator is the transistor version of the Colpitts oscillator, shown in Fig. 195. Regenerative feedback is obtained from the tuned circuit consisting of capacitors C_2

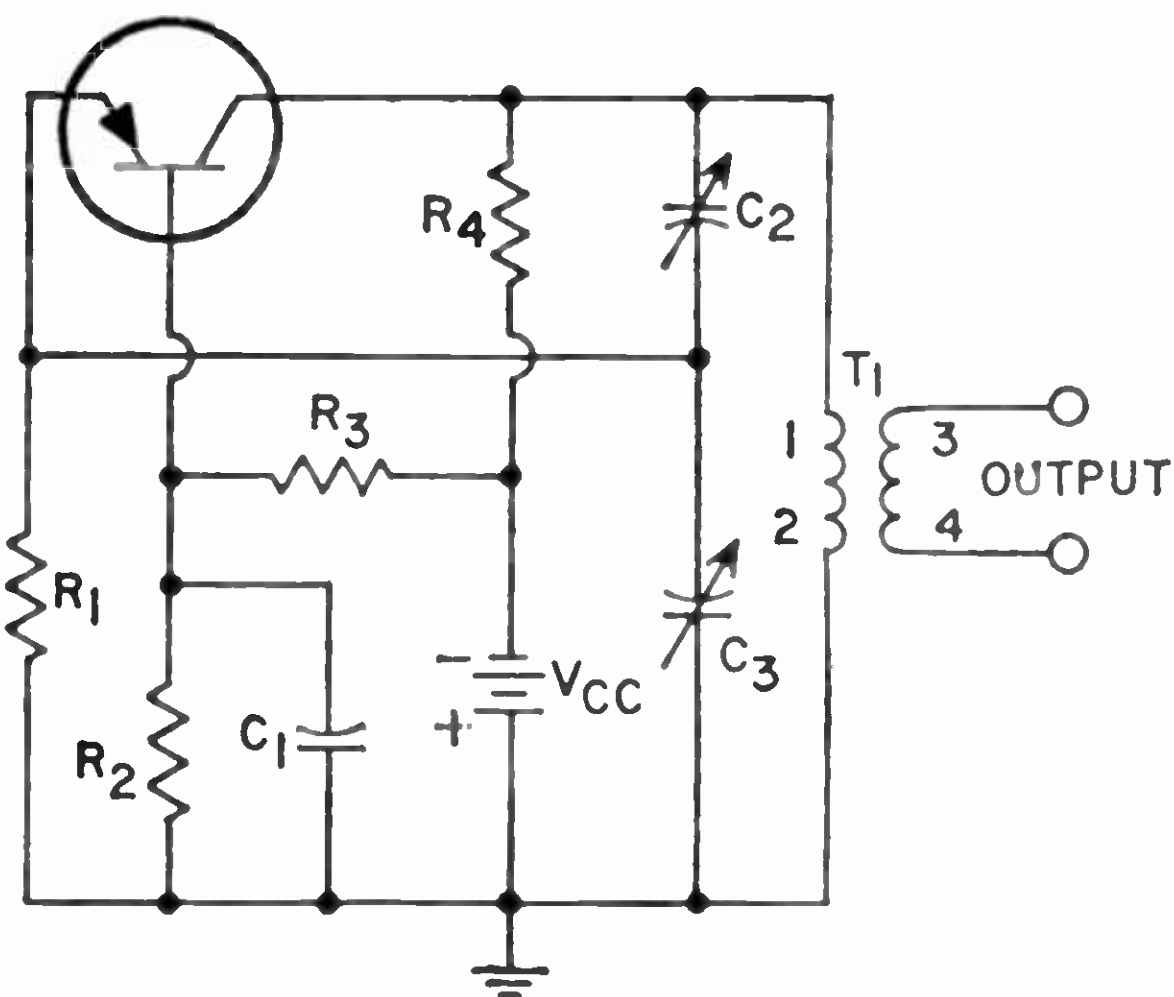


Fig. 195—Transistor Colpitts oscillator.

and C_3 in parallel with the primary winding of the transformer, and is applied to the emitter of the transistor. Base bias is provided by resistors R_2 and R_3 . Resistor R_4 is the collector load resistor. Resistor R_1 develops the emitter input signal and also acts as the emitter stabilizing resistor. Capacitors C_2 and C_3 form a voltage divider; the voltage

developed across C_3 is the feedback voltage. The frequency and the amount of feedback voltage can be controlled by adjustment of either or both capacitors. For minimum feedback loss, the ratio of the capacitive reactance between C_2 and C_3 should be approximately equal to the ratio between the output impedance and the input impedance of the transistor.

Fig. 196 shows the field-effect transistor in use in two forms of the Colpitts oscillator circuit. These circuits are more commonly used in vhf and uhf equipment than the Hartley circuits because of the mechanical difficulty involved in making the tapped coils required at these frequencies by the Hartley circuits.

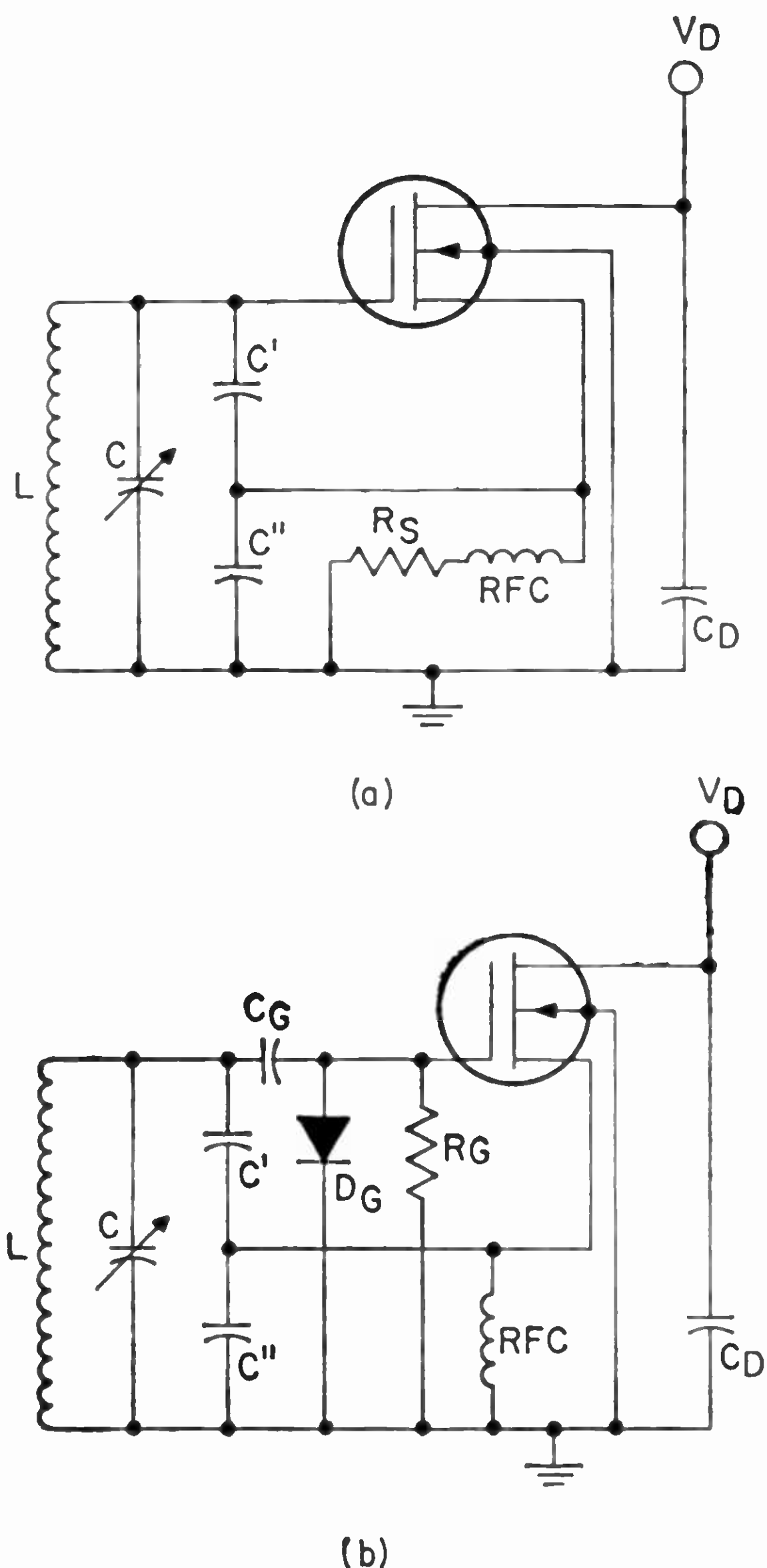


Fig. 196—Colpitts oscillator circuits using MOS transistors.

Feedback is controlled in the Colpitts oscillator by the ratio of the capacitance of C' to C'' .

Fig. 197, the gate-tickler-feedback oscillator circuit, and Fig. 198, the drain-tickler-feedback oscillator

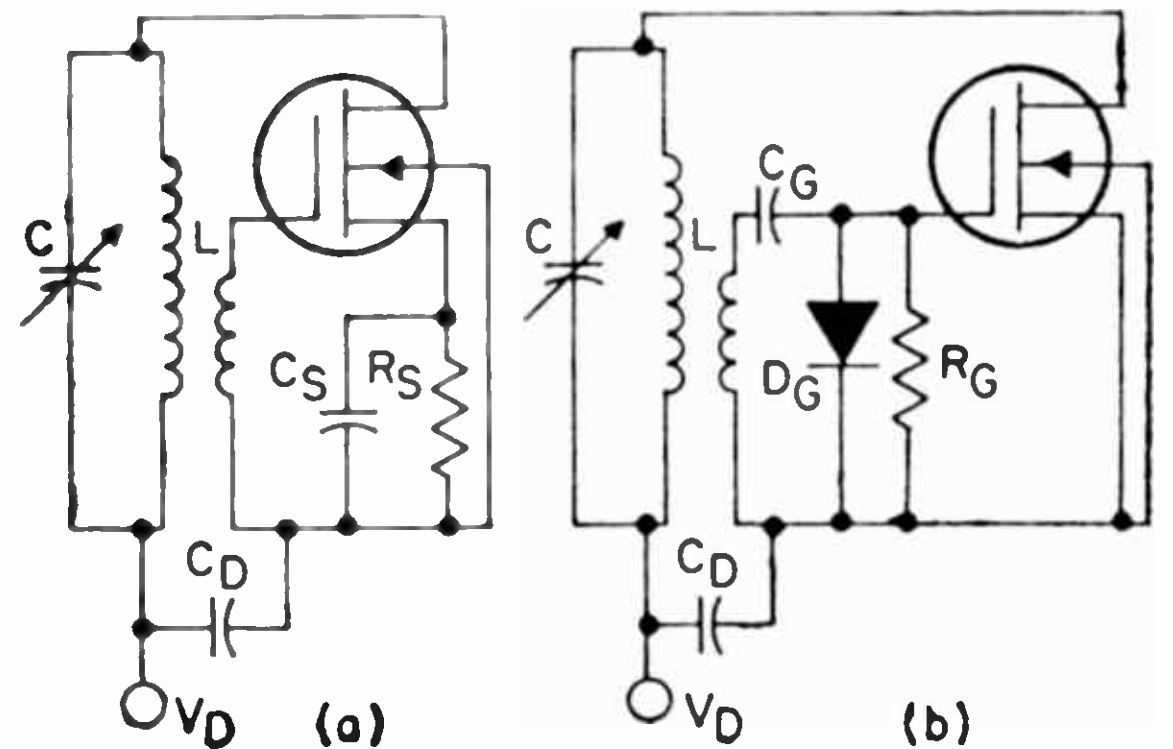


Fig. 197—Gate-tickler-feedback oscillator circuits.

circuit, have no particular advantages over the Hartley and Colpitts circuits except that in some designs it may be more economical to provide a tickler winding than the tapped coil or capacitive divider required in the Hartley or Colpitts circuits, respectively.

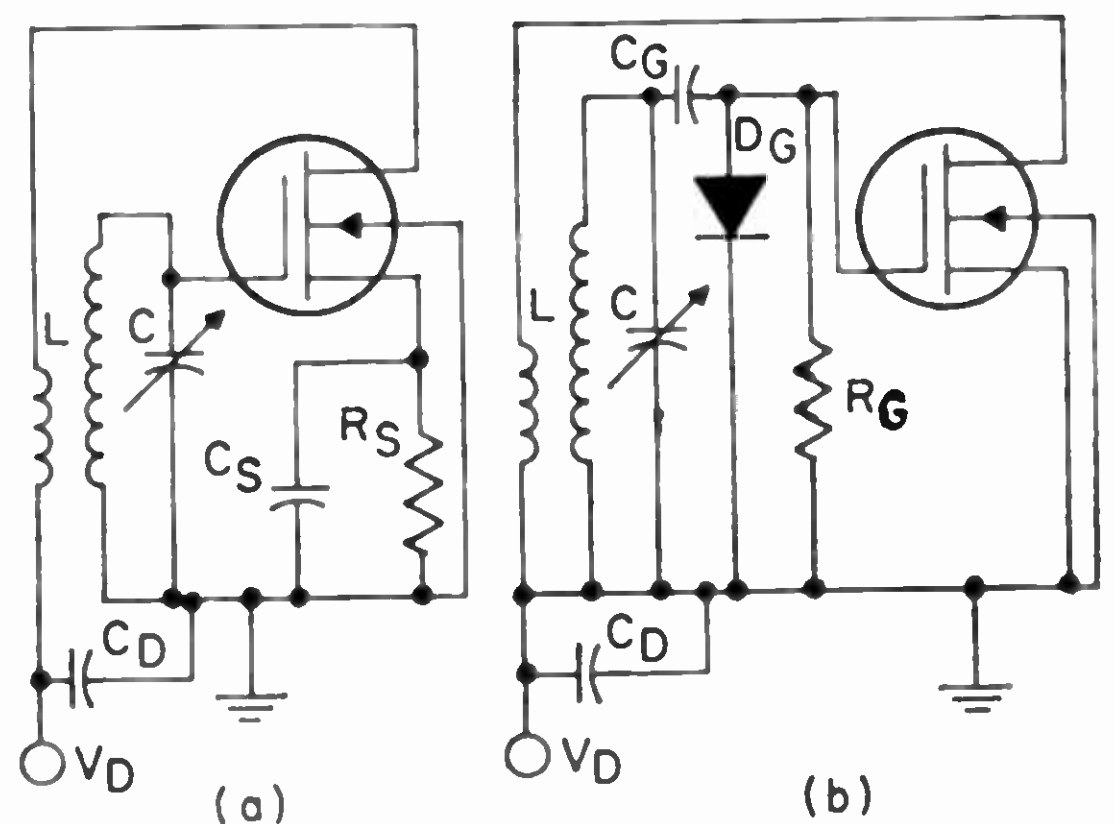


Fig. 198—Drain-tickler-feedback oscillator circuits.

A Clapp oscillator is a modification of the Colpitts circuit shown in Fig. 195 in which a capacitor is added in series with the primary winding of the transformer to improve frequency stability. When the added capacitance is small compared to the series capacitance of C_3 and C_4 , the oscillator frequency is determined by the series LC combination of the transformer primary and the added capacitor.

Crystal Oscillators

A quartz crystal is often used as the frequency-determining element in a transistor oscillator circuit because of its extremely high Q (narrow bandwidth) and good frequency stability over a given temperature range. A quartz crystal may be operated as either a series or parallel resonant circuit. As shown in Fig. 199, the electrical equivalent of the mechanical vibrating characteristic of the crystal can be represented by a resistance R , an inductance L , and a capacitance C_s in series. The lowest impedance of the crystal occurs at the series resonant frequency of C_s and L ; the resonant frequency of the circuit is then determined only by the mechanical vibrating characteristics of the crystal.

The parallel capacitance C_p shown in Fig. 199 represents the electrostatic capacitance between the crystal electrodes. At frequencies above the

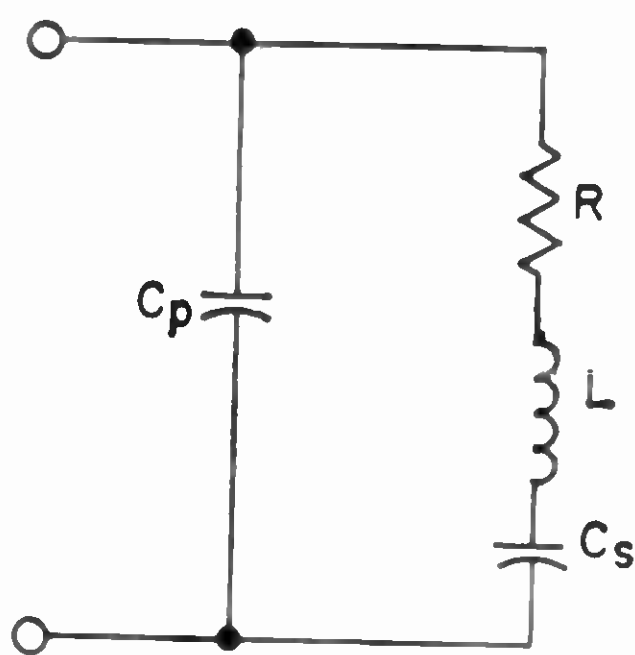


Fig. 199—Equivalent circuit of quartz crystal.

series resonant frequency, the combination of L and C_s has the effect of a net inductance because the inductive reactance of L is greater than the capacitive reactance of C_s . This net inductance forms a parallel resonant circuit with C_p and any circuit capacitance across the crystal. The impedance of the crystal is highest at the parallel resonant frequency; the resonant frequency of the circuit is then determined by both the crystal and externally connected circuit elements.

Increased frequency stability can be obtained in the tuned-collector and tuned-base oscillators discussed

previously if a crystal is used in the feedback path. The oscillation frequency is then fixed by the crystal. At frequencies above and below the series resonant frequency of the crystal, the impedance of the crystal increases and the feedback is reduced. Thus, oscillation is prevented at frequencies other than the series resonant frequency.

The parallel mode of crystal resonance is used in the Pierce oscillator shown in Fig. 200. (If the crystal were replaced by its equivalent circuit, the functioning of the oscillator would be analogous to that of the Colpitts oscillator shown in Fig. 195.) The resistances shown in Fig. 200 provide the proper bias and stabilizing conditions for the common-emitter circuit. Capacitor C_1 is the

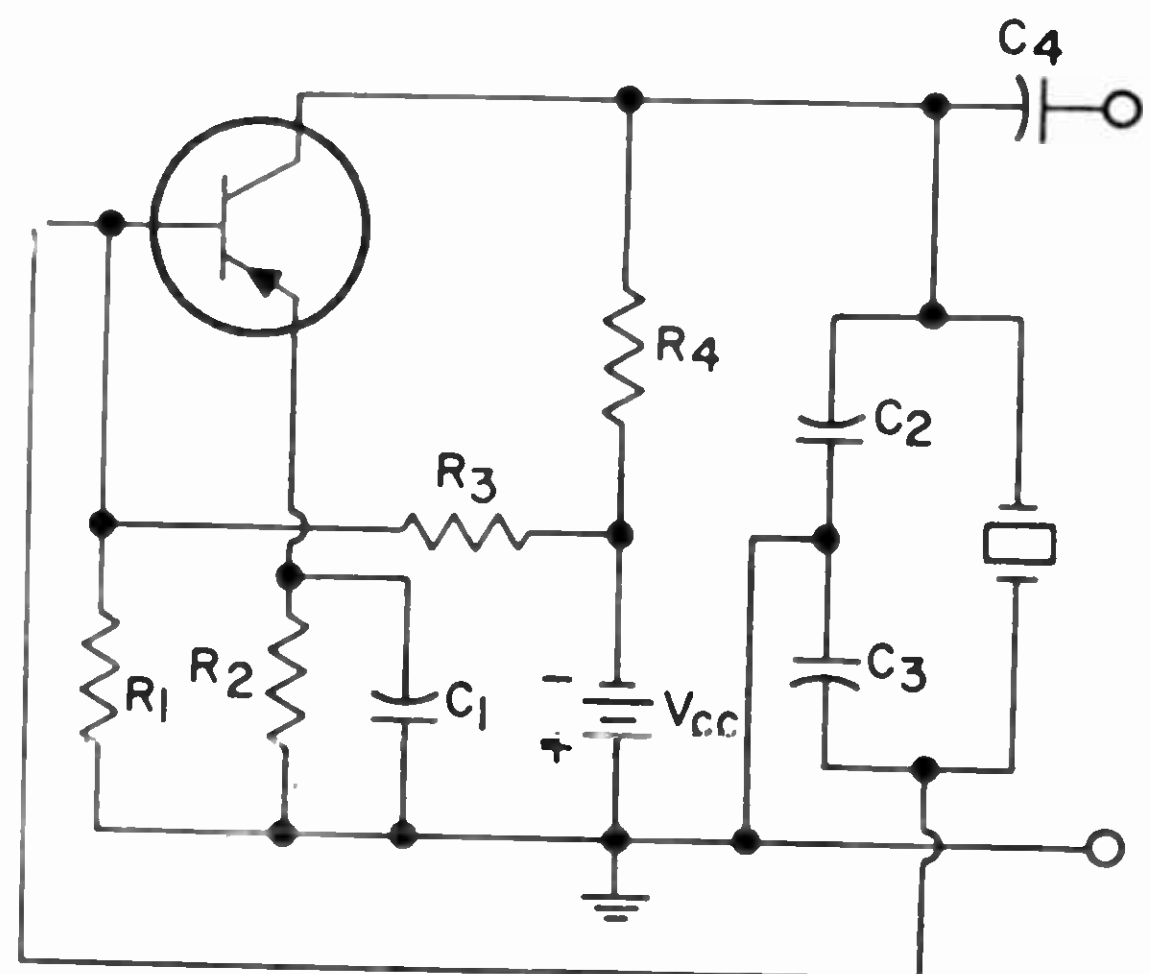


Fig. 200—Pierce-type transistor crystal oscillator.

emitter bypass capacitor. The required 180-degree phase inversion of the feedback signal is accomplished through the arrangement of the voltage-divider network C_2 and C_3 . The connection between the capacitors is grounded so that the voltage developed across C_3 is applied between base and ground and a 180-degree phase reversal is obtained. The oscillating frequency of the circuit is determined by the crystal and the capacitors connected in parallel with it.

The field-effect transistor also operates well in crystal oscillator circuits such as the Pierce-type oscillator shown in Fig. 201. This oscillator is extremely popular because

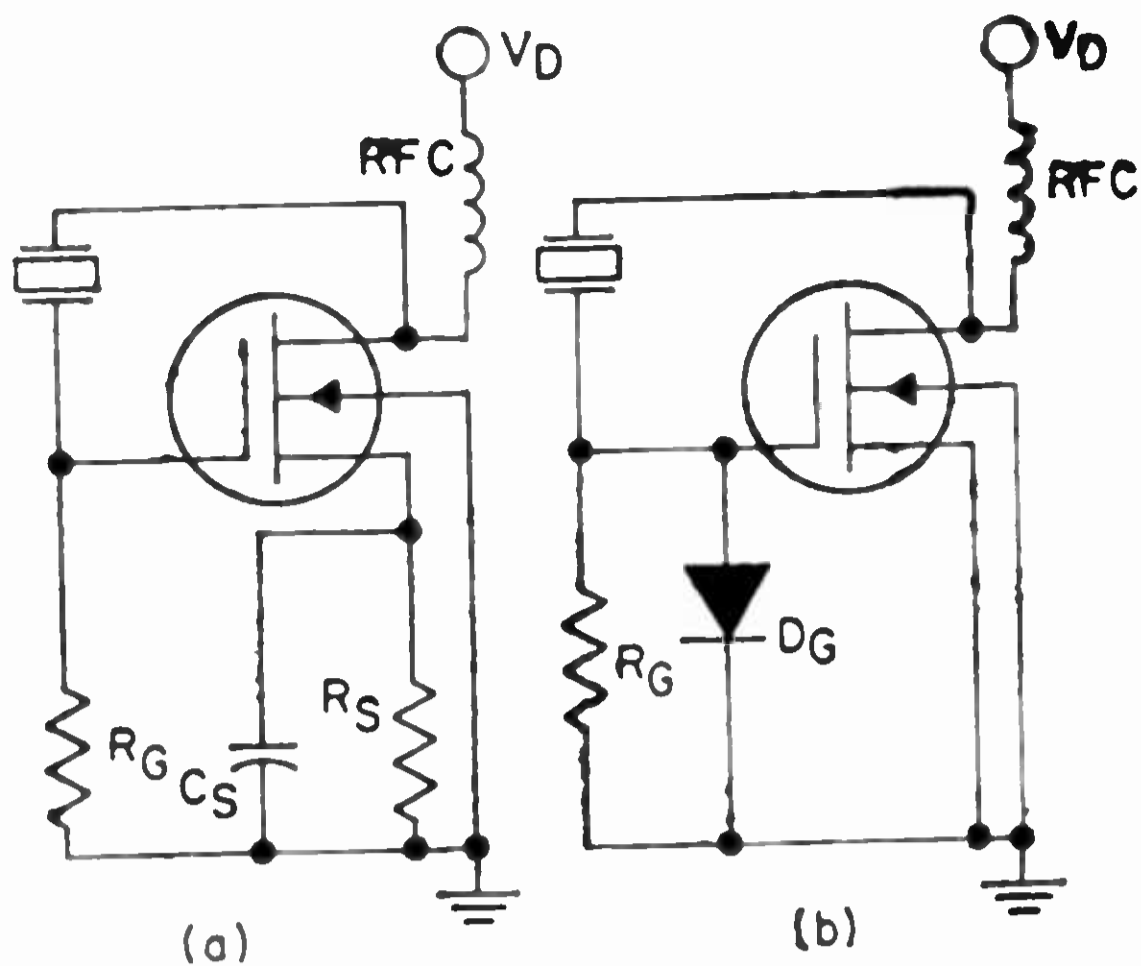


Fig. 201—Pierce-type crystal oscillator circuits using MOS transistors.

of its simplicity and minimum number of components. At frequencies below 2 MHz, a capacitive voltage divider may be required across the crystal. The connection between the voltage-divider capacitors must be grounded so that the voltage developed across the capacitors is reversed in phase by 180 degrees.

It is frequently desirable to operate crystals in communications equipment at their harmonic or overtone frequencies; Fig. 202 shows two circuits designed for this purpose. Additional feedback is obtained for the overtone crystal by the use of a capacitive divider as the tuned-circuit bypass. Most third-overtone crystals operate satisfactorily without this additional feedback, but the extra feedback is required for the 5th and 7th harmonics. The tuned circuit in Figs. 202(a) and 202(b) is not fully bypassed and produces a voltage that aids oscillation. The crystal in both circuits is connected to the junction of the capacitors $C_{d'}$ and $C_{d''}$; the ratio of these capacitors should be approximately 1:3.

The circuit of Fig. 203 operates well with low-frequency quartz bars. The crystal is located in the feedback circuit between the sources of the two field-effect transistors and operates in the series mode. Capacitor C_2 is normally used for precise adjustment of the frequency of the oscillator; a reduction in the capacitance increases the frequency slightly.

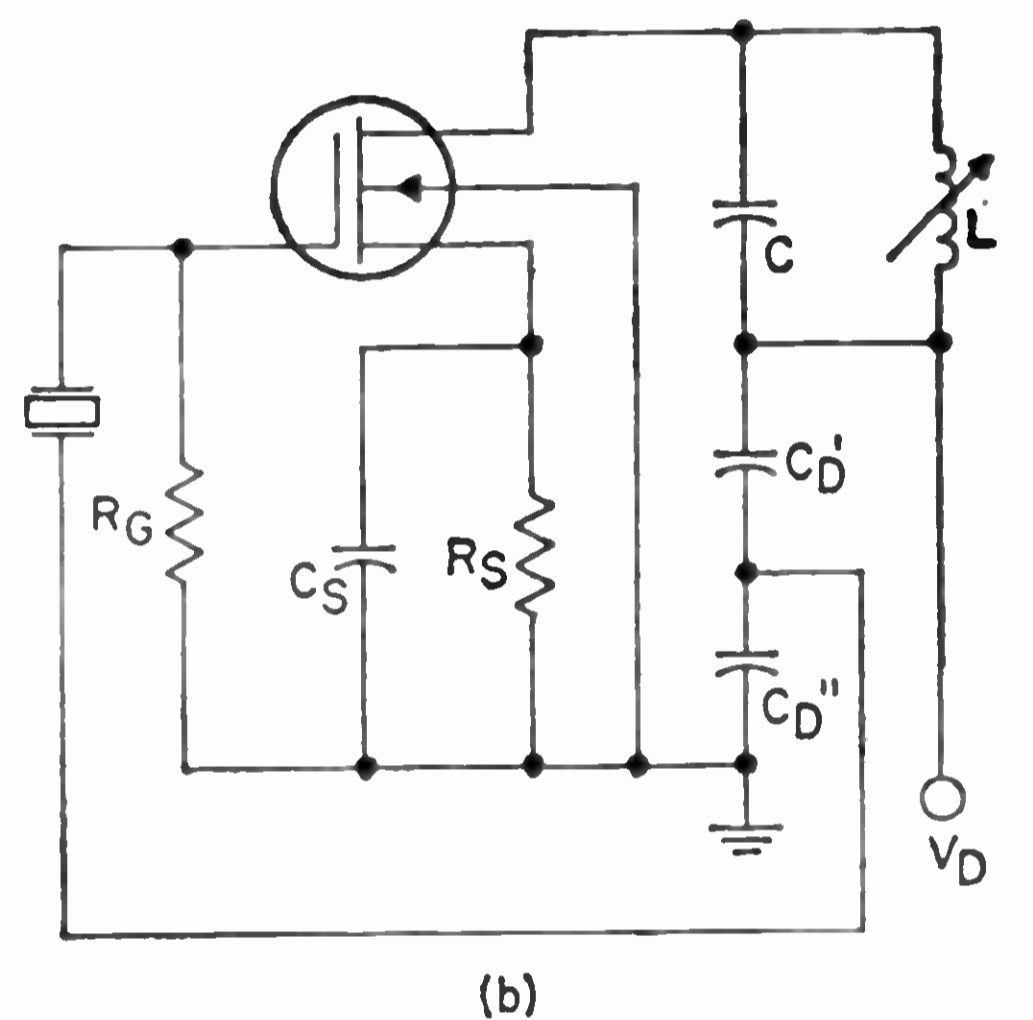
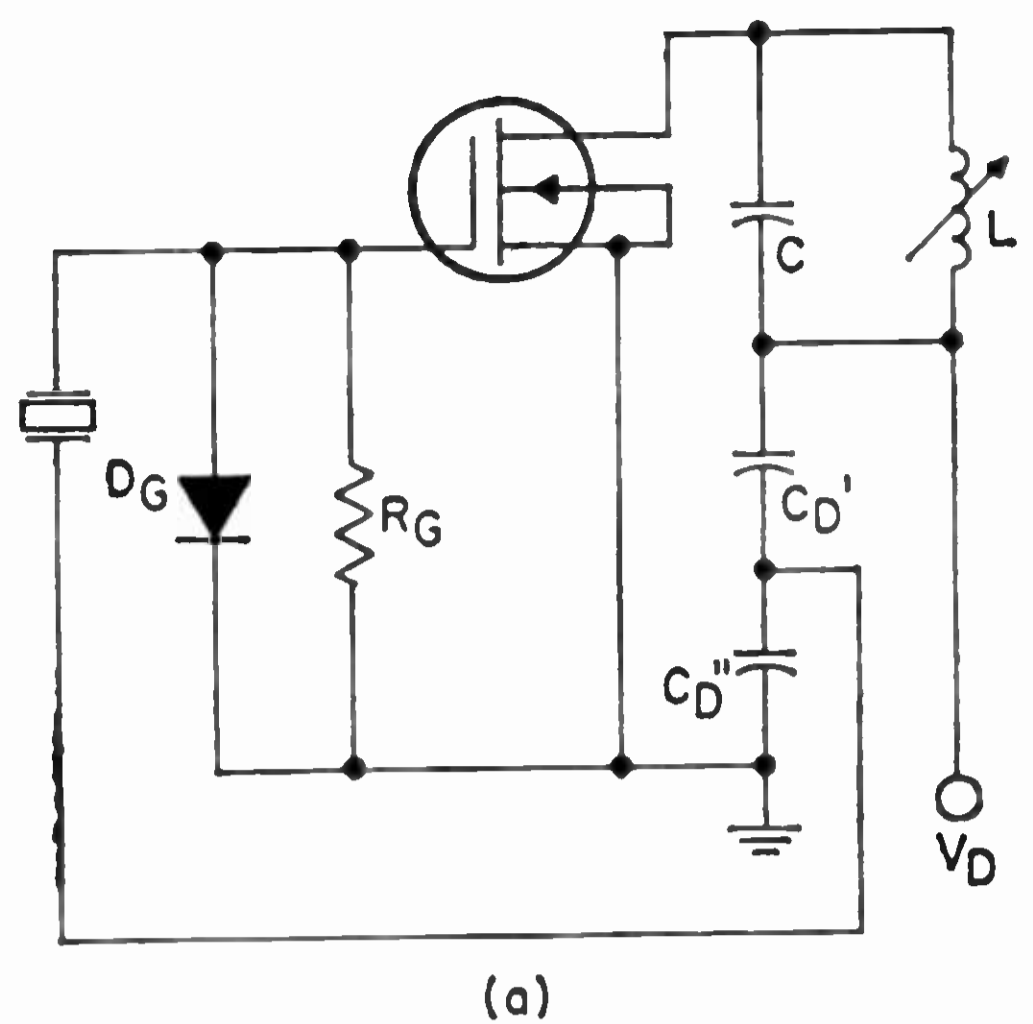


Fig. 202—Crystal oscillator circuits permitting operation at overtone or harmonic frequencies.

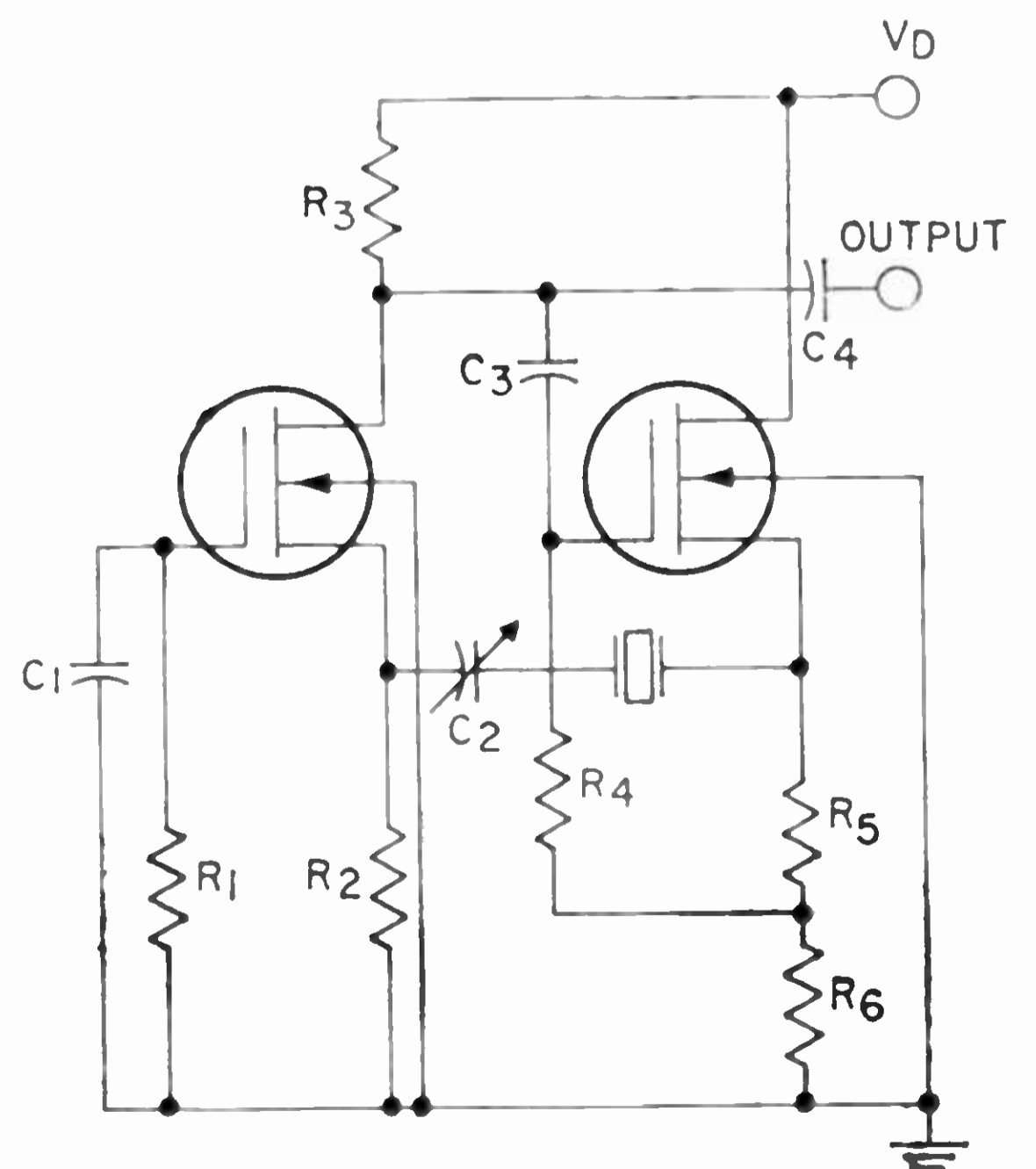


Fig. 203—Low-frequency crystal oscillator circuit using MOS transistors.

RC Feedback Oscillators

A resistance-capacitance (RC) network is sometimes used in place of an inductance-capacitance network in a transistor oscillator. In the phase-shift oscillator shown in Fig. 204, the RC network consists of three sections (C_1R_1 , C_2R_2 , and C_3R_3), each of which contributes a phase shift of 60 degrees at the frequency of oscillation. Because the capacitive reactance of the network increases or decreases at other frequencies, the 180-degree phase shift required for the common-emitter oscillator occurs only at one frequency; thus, the output frequency of the oscillator is fixed. Phase-shift oscillators may be

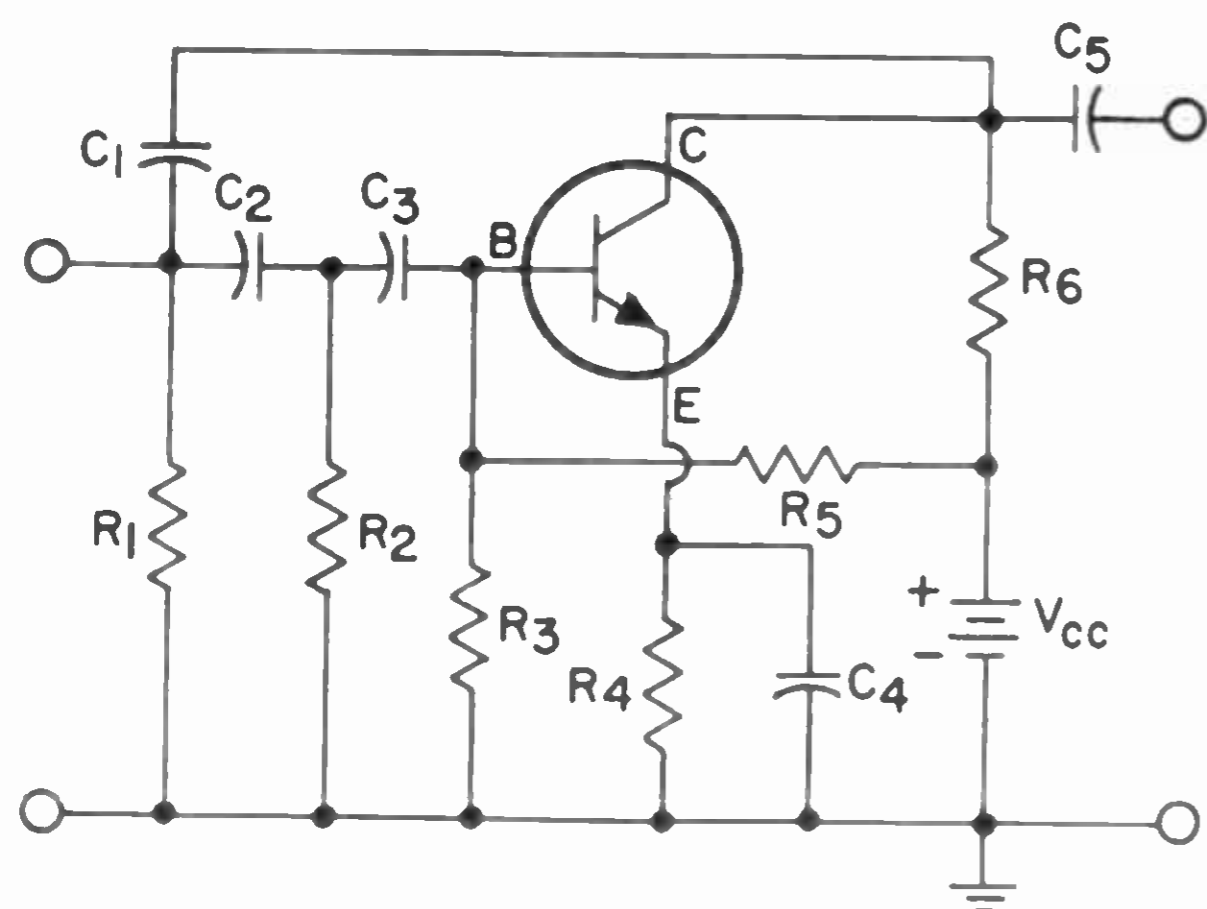


Fig. 204—Transistor RC phase-shift oscillator.

made variable over particular frequency ranges by the use of ganged variable capacitors or resistors in the RC networks. Three or more sections must be used in the phase-shifting networks to reduce feedback losses. The use of more sections contributes to increased stability.

FREQUENCY CONVERSION

Transistors can be used in various types of circuits to change the frequency of an incoming signal. In radio and television receivers, frequency conversion is used to change the frequency of the rf signal to an intermediate frequency. In communications transmitters, frequency mul-

tiplication is often used to raise the frequency of the developed rf signal.

In a radio or television receiver, the oscillating and mixing functions are performed by a nonlinear device such as a diode or a transistor. As shown in the diagram of Fig. 205,

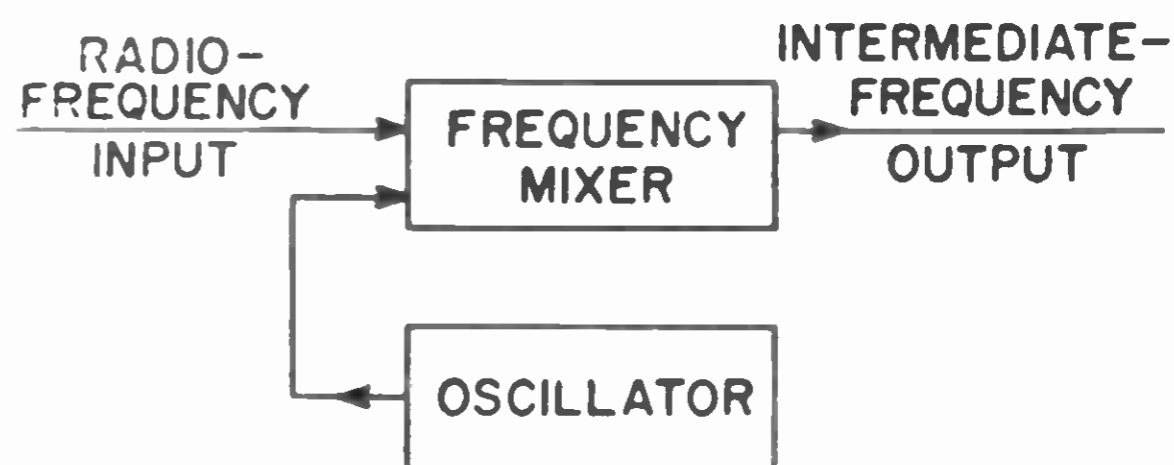


Fig. 205—Block diagram of simple frequency-converter circuit.

two voltages of different frequencies, the rf signal voltage and the voltage generated by the oscillator, are applied to the input of the mixer. These voltages “beat,” or heterodyne, within the mixer transistor to produce a current having, in addition to the frequencies of the input voltages, numerous sum and difference frequencies.

The output circuit of the mixer stage is provided with a tuned circuit which is adjusted to select only one beat frequency, i.e., the frequency equal to the difference between the signal frequency and the oscillator frequency. The selected output frequency is known as the intermediate frequency, or if. The output frequency of the mixer transistor is kept constant for all values of signal frequency by tuning of the oscillator circuit.

In AM broadcast-band receivers, the oscillator and mixer functions are often accomplished by use of a single transistor called an “autodyne converter”. In FM receivers, stable oscillator operation is more readily obtained when a separate transistor is used for the oscillator function. In such a circuit, the oscillator voltage is applied to the mixer by inductive coupling, capacitive coupling, or a combination of the two.

AUTOMATIC FREQUENCY CONTROL

An automatic frequency control (afc) circuit is often used to provide automatic correction of the oscillator frequency of a superheterodyne receiver when, for any reason, it drifts from the frequency which produces the proper if center frequency. This correction is made by adjustment of the frequency of the oscillator. Such a circuit automatically compensates for slight changes in rf carrier or oscillator frequency, as well as for inaccurate manual or push-button tuning.

An afc system requires two sections: a frequency detector and a variable reactance. The detector section may be essentially the same as the FM detector illustrated in Fig. 120. In the afc system, however, the output is a dc control voltage, the magnitude of which is proportional to the amount of frequency shift. This dc control voltage is used to control the bias on a transistor or diode which comprises the variable reactance.

Automatic frequency control is also used in television receivers to keep the horizontal oscillator in step with the horizontal-scanning frequency at the transmitter. A widely used horizontal afc circuit is shown in Fig. 206. This circuit, which is often referred to as a balanced-phase-detector or phase-discriminator circuit, is usually employed to control the frequency of the horizon-

tal-oscillator circuit. The detector diodes supply a dc control voltage to the horizontal-oscillator circuit which counteracts changes in its operating frequency. The magnitude and polarity of the control voltages are determined by phase relationships in the afc circuit.

The horizontal sync pulses obtained from the sync-separator circuit are fed through a phase-inverter or phase-splitter circuit to the two diode detectors. Because of the action of the phase-inverter circuit, the signals applied to the two diode units are equal in amplitude but 180 degrees out of phase. A reference sawtooth voltage obtained from the horizontal output circuit is also applied simultaneously to both units. The diodes are biased so that conduction takes place only during the tips of the sync pulses. Any change in the oscillator frequency alters the phase relationship between the reference sawtooth and the incoming horizontal sync pulses, and thus causes one of the diodes to conduct more heavily than the other so that a correction signal is produced. The system remains unbalanced at all times, therefore, because momentary changes in oscillator frequency are instantaneously corrected by the action of this control voltage. The network between the diodes and the horizontal-oscillator circuit is essentially a low-pass filter which prevents the horizontal sync pulses from affecting the horizontal-oscillator performance.

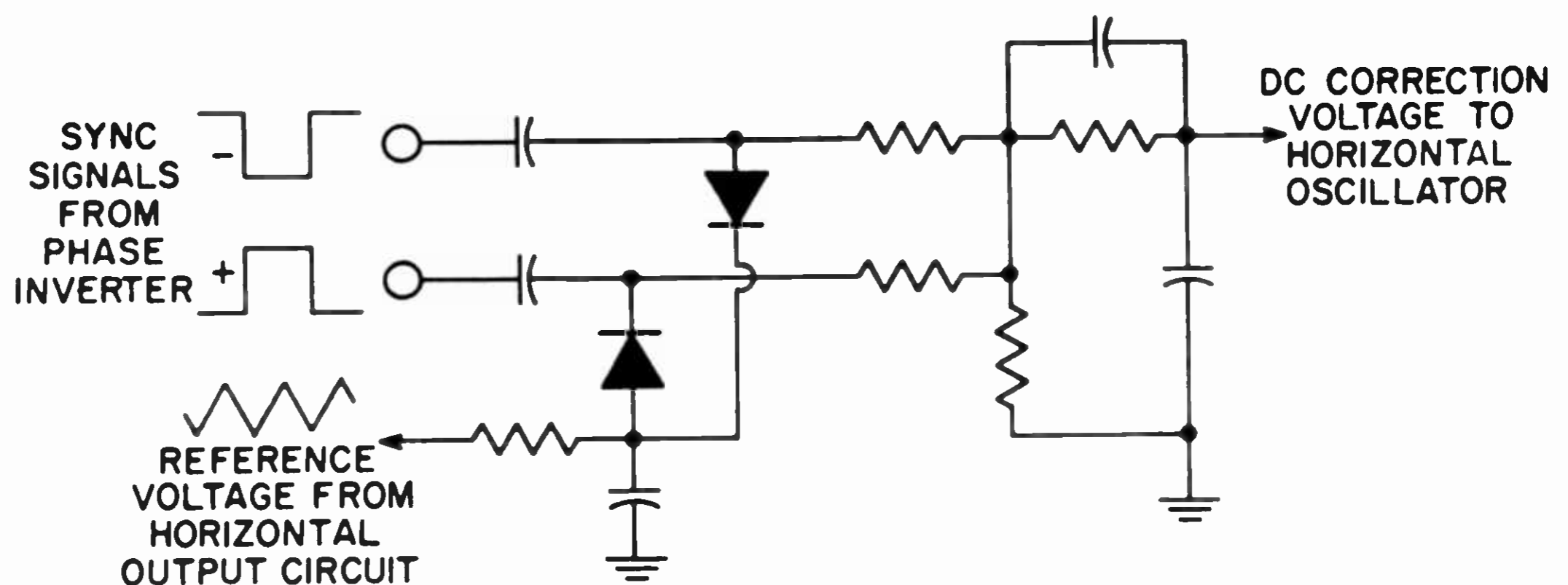


Fig. 206—Balanced-phase-detector or phase-discriminator circuit for horizontal afc.

FREQUENCY MULTIPLICATION

Frequency multipliers are another type of frequency-conversion circuit. Because the output-current waveform of power transistors can be made to contain both fundamental and harmonic frequency components, power output can be obtained at a desired harmonic frequency by use of a special type of output circuit coupled to the collector of the transistor. Transistors can be connected in either the common-base or the common-emitter configuration for frequency multiplication.

The design of transistor frequency-multiplier circuits consists of selection of a suitable transistor and design of filtering and matching networks for optimum circuit performance. The transistor must be capable of power and gain at the fundamental frequency and capable of converting power from the fundamental to a harmonic frequency. At a given input power level, the output power at a desired harmonic frequency is equal to the product of the power gain of the transistor at the drive frequency and the conversion efficiency of the frequency-multiplier circuit. Conversion gain can be obtained only when the power gain of the transistor at the fundamental frequency is larger than the conversion loss of the circuit.

Various types of instabilities can occur in transistor frequency-multiplier circuits, including low-frequency resonances, parametric oscillations, hysteresis, and high-frequency resonances. Low-frequency resonances occur because the gain of the transistor is very high at low frequency compared to that at the

operating frequency. "Hysteresis" refers to discontinuous mode jumps in output power when the input power or frequency is increased or decreased. A tuned circuit used in the output coupling network has a different resonant frequency under strong drive than under weaker driving conditions. It has been found experimentally that hysteresis effect can be minimized, and sometimes eliminated, by use of the common-emitter configuration.

Perhaps the most troublesome instability in transistor frequency-multiplier circuits is high-frequency resonance. Such instability shows up in the form of oscillations at a frequency very close to the output frequency when the input drive power is removed. This effect suggests that the transistor under this condition behaves as a locked oscillator at the fundamental frequency. Common-emitter circuits have been found to be less critical for high-frequency oscillations than common-base circuits. High-frequency resonance is also strongly related to the input drive frequency, and can be eliminated if the input frequency is kept below a certain value. The input frequency at which stable operation can be obtained depends on the method used to ground the emitter of the transistor, and can be increased by use of the shortest possible path from the emitter to ground.

Varactor diodes are also used to provide frequency multiplication. Fig. 102 and associated text given previously in the section on **Other Semiconductor Diodes** define the requirements for this type of application.

TV Deflection and Color Demodulation

For reproduction of a transmitted picture in a television receiver, the face of a cathode-ray tube is scanned with an electron beam while the intensity of the beam is varied to control the emitted light at the phosphor screen. The scanning is synchronized with a scanned image at the TV transmitter, and the black-through-white picture areas of the scanned image are converted into an electrical signal that controls the intensity of the electron beam in the picture tube at the receiver.

SCANNING FUNDAMENTALS

The scanning procedure used in the United States employs horizontal linear scanning in an odd-line interlaced pattern. The standard scanning pattern for television systems includes a total of 525 horizontal scanning lines in a rectangular frame having an aspect ratio of 4 to 3. The frames are repeated at a rate of 30 per second, with two fields interlaced in each frame. The first field in each frame consists of all odd-number scanning lines, and the second field in each frame consists of all even-

number scanning lines. The field repetition rate is thus 60 per second, and the vertical scanning rate is 60 Hz. (For color systems, the vertical scanning rate is 59.94 Hz.)

The geometry of the standard odd-line interlaced scanning pattern is illustrated in Fig. 207. The scanning beam starts at the upper left corner of the frame at point A, and sweeps across the frame with uniform velocity to cover all the picture elements in one horizontal line. At the end of each trace, the beam is rapidly returned to the left side of the frame, as shown by the dashed line, to begin the next horizontal line. The horizontal lines slope downward in the direction of scanning because the vertical deflecting signal simultaneously produces a vertical scanning motion, which is very slow compared with the horizontal scanning speed. The slope of the horizontal line trace from left to right is greater than the slope of the retrace from right to left because the shorter time of the retrace does not allow as much time for vertical deflection of the beam. Thus, the beam is continuously and slowly deflected downward as it scans

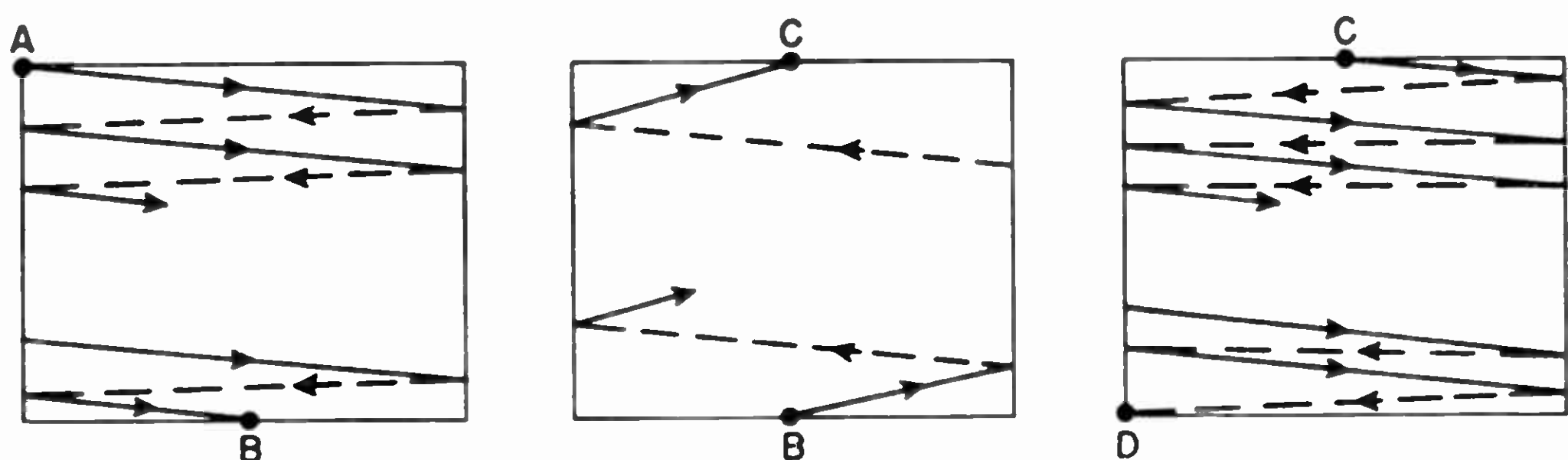


Fig. 207—The odd-line interlaced scanning procedure.

the horizontal lines, and its position is successively lower as the horizontal scanning proceeds.

At the bottom of the field, the vertical retrace begins, and the beam is brought back to the top of the frame to begin the second or even-number field. The vertical "flyback" time is very fast compared to the trace, but is slow compared to the horizontal scanning speed; therefore, some horizontal lines are produced during the vertical flyback.

All odd-number fields begin at point A in Fig. 207 and are the same. All even-number fields begin at point C and are the same. Because the beginning of the even-field scanning at C is on the same horizontal level as A, with a separation of one-half line, and the slope of all lines is the same, the even-number lines in the even fields fall exactly between the odd-number lines in the odd field.

SYNC

In addition to picture information, the composite video signal from the video detector of a television receiver contains timing pulses to assure that the picture is produced on the faceplate of the picture tube at the right instant and in the right location. These pulses, which are called sync pulses, control the horizontal and vertical scanning generators of the receiver.

Fig. 208 shows a portion of the detected video signal. When the picture is bright, the amplitude of the signal is low. Successively deeper grays are represented by higher amplitudes

until, at the "blanking level" shown in the diagram, the amplitude represents a complete absence of light. This "black level" is held constant at a value equal to 75 per cent of the maximum amplitude of the signal during transmission. The remaining 25 per cent of the signal amplitude is used for synchronization information. Portions of the signal in this region (above the black level) cannot produce light.

In the transmission of a television picture, the camera becomes inactive at the conclusion of each horizontal line and no picture information is transmitted while the scanning beam is retracing to the beginning of the next line. The scanning beam of the receiver is maintained at the black level during this retrace interval by means of the blanking pulse shown in Fig. 208. Immediately after the beginning of the blanking period, the signal amplitude rises further above the black level to provide a horizontal-synchronization pulse that initiates the action of the horizontal scanning generator. When the bottom line of the picture is reached, a similar vertical-synchronization pulse initiates the action of the vertical scanning generator to move the scanning spot back to the top of the pattern.

The sync pulses in the composite video signal are separated from the picture information in a **sync-separator** stage, as shown in Figs. 209 and 210. This stage is biased sufficiently beyond cutoff so that current flows and an output signal is produced only at the peak positive swing of the input signal. In the

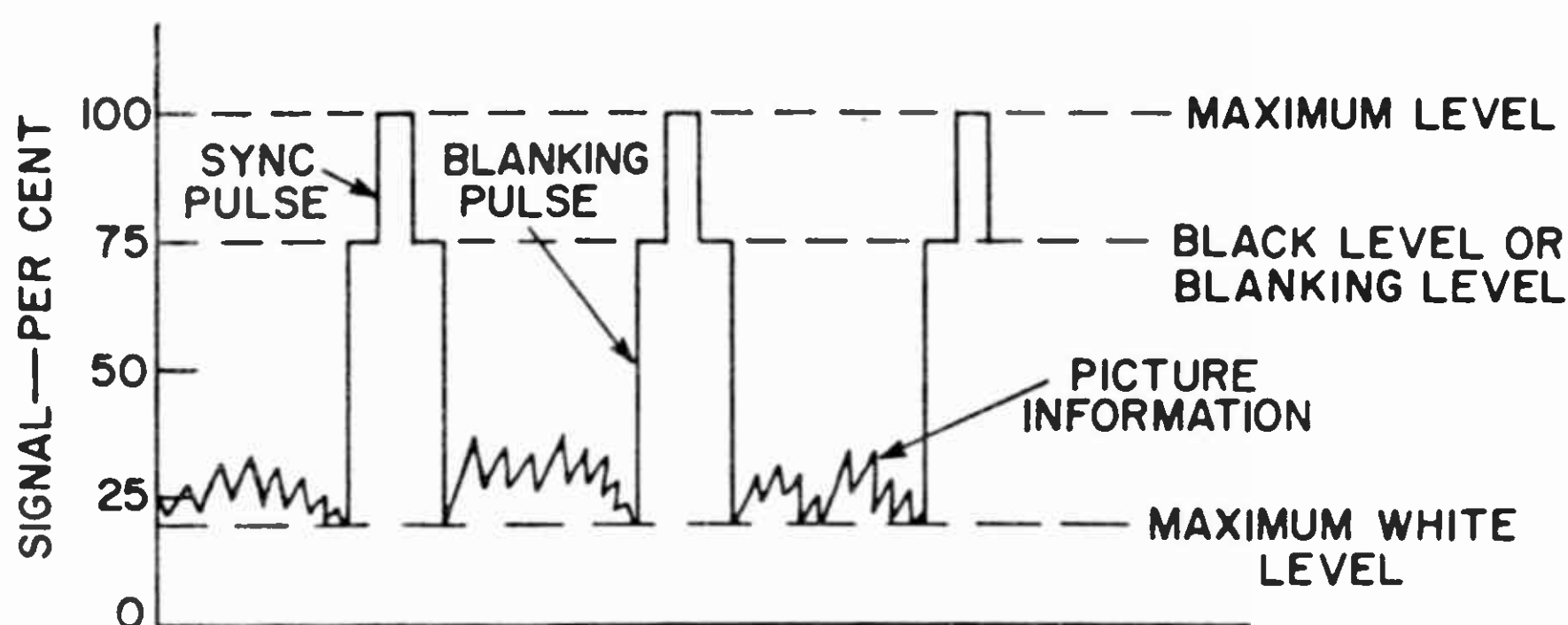


Fig. 208—Detected video signal.

diode circuit of Fig. 209, negative bias for the diode is developed by R and C as a result of the flow of diode current on the positive extreme of signal input. The bias automatically adjusts itself so

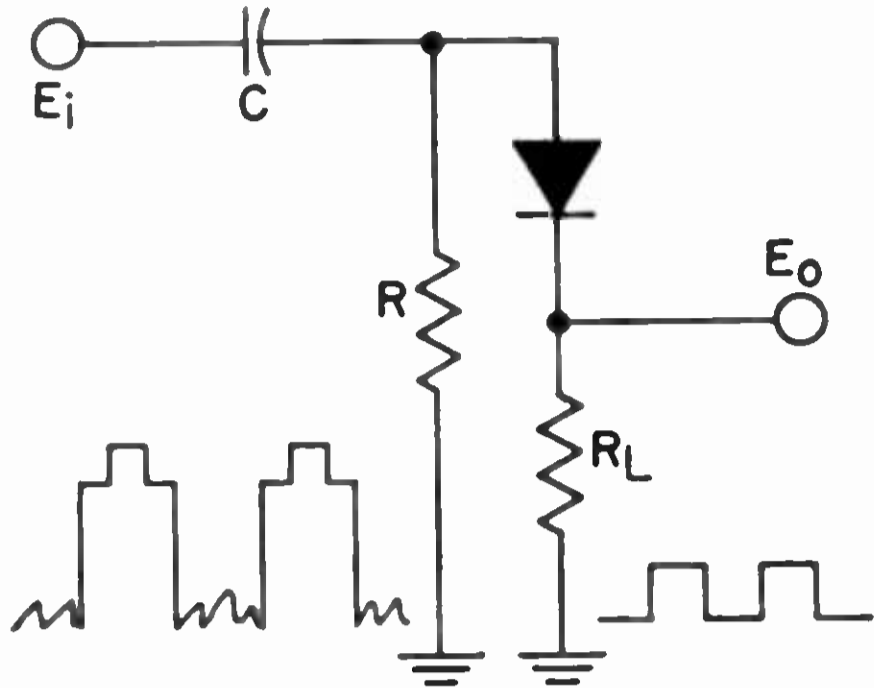


Fig. 209—Diode sync-separator circuit.

that the peak positive swing of the input signal drives the anode of the diode positive and allows the flow of current only for the sync pulse. In the circuit shown in Fig. 210, the base-emitter junction of the transistor functions in the same manner as the diode in Fig. 209, but in addition the pulses are amplified.

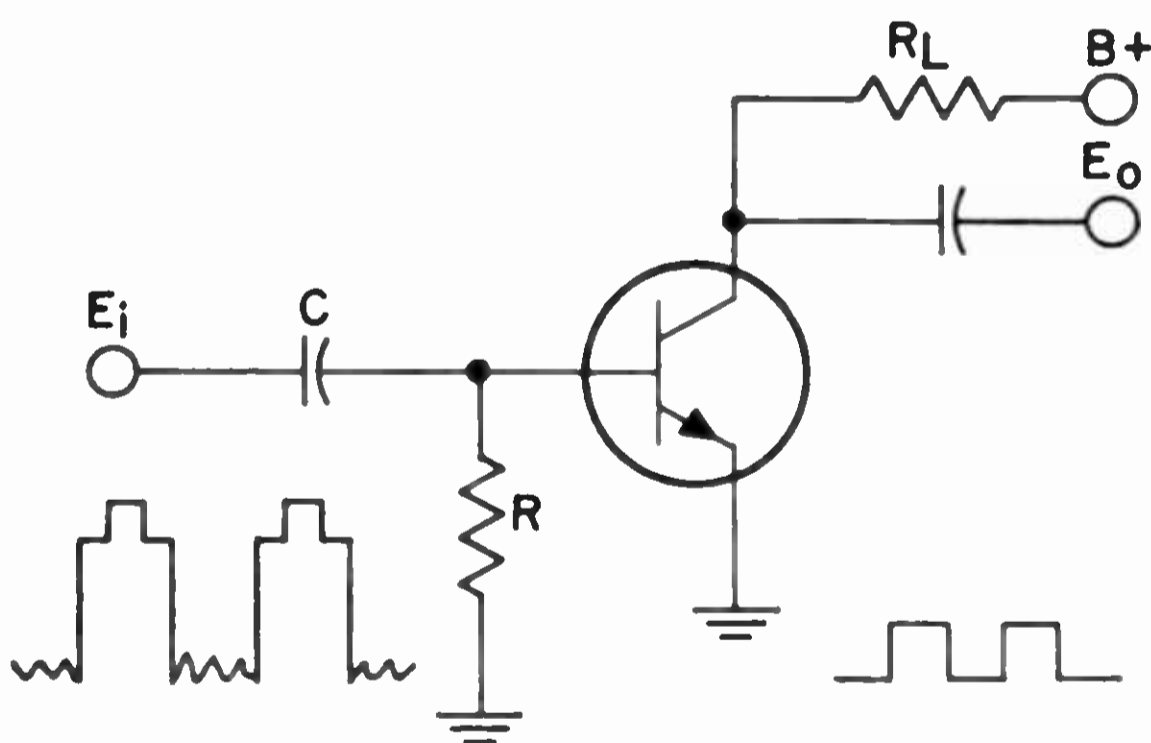


Fig. 210—Transistor sync-separator circuit.

After the synchronizing signals are separated from the composite video signal, it is necessary to filter out the horizontal and vertical sync signals so that each can be applied to its respective deflection generator. This filtering is accomplished by RC circuits designed to filter out all but the desired synchronizing signals. Although the horizontal, vertical, and equalizing pulses are all rectangular pulses of the same amplitude, they differ in frequency and pulse width, as shown in Fig. 211. The horizontal

sync pulses have a repetition rate of 15,750 per second (one for each horizontal line) and a pulse width of 5.1 microseconds. (For color system, the repetition rate of the horizontal sync pulses is 15,734 per second.) The equalizing pulses have a width approximately half the horizontal pulse width, and a repetition rate of 31,500 per second; they occur at half-line intervals, with six pulses immediately preceding and six following the vertical synchronizing pulse. The vertical pulse is repeated at a rate of 60 per second (one for each field), and has a width of approximately 190 microseconds. The serrations in the vertical pulse occur at half-line intervals, dividing the complete pulse into six individual pulses that provide horizontal synchronization during the vertical retrace. (Although the picture is blanked out during the vertical retrace time, it is necessary to keep the horizontal scanning generator synchronized.)

All the pulses described above are produced at the transmitter by the synchronizing-pulse generator; their waveshapes and spacings are held within very close tolerances to provide the required synchronization of receiver and transmitter scanning.

The horizontal sync signals are separated from the total sync in a differentiating circuit that has a short time constant compared to the width of the horizontal pulses. When the total sync signal is applied to the differentiating circuit shown in Fig. 212, the capacitor charges completely very soon after the leading edge of each pulse, and remains charged for a period of time equal to practically the entire pulse width. When the applied voltage is removed at the time corresponding to the trailing edge of each pulse, the capacitor discharges completely within a very short time. As a result, a positive peak of voltage is obtained for each leading edge and a negative peak for the trailing edge of every pulse. One polarity is produced by the charging current for the leading edge of the applied pulse, and the

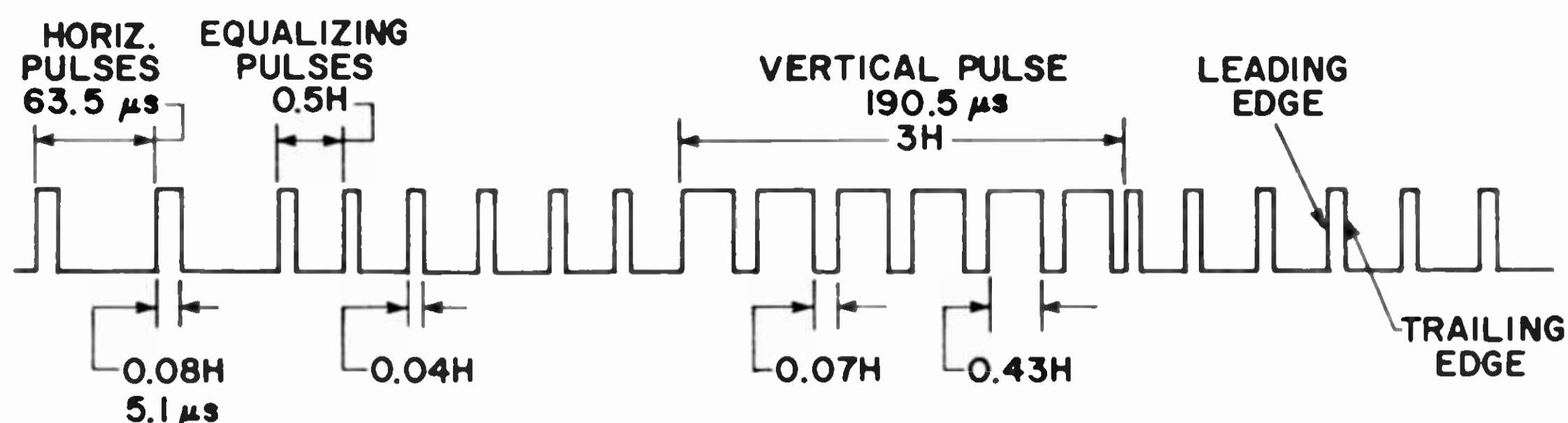


Fig. 211—Waveform of TV synchronizing pulses ($H =$ horizontal line period of $1/15,750$ seconds, or $63.5 \mu s$).

opposite polarity is obtained from the discharge current corresponding to the trailing edge of the pulse.

As mentioned above, the serrations in the vertical pulse are inserted to provide the differentiated output needed to synchronize the horizontal scanning generator during the time of vertical synchronization. During the vertical blanking period, many more voltage peaks are available than are necessary for horizontal synchronization (only one pulse is used for each horizontal line period). The check marks above the differentiated output in Fig. 212 indicate the voltage peaks used to synchronize the horizontal deflection generator for one field. Because the sync system is made sensitive only to positive pulses occurring at approximately the right horizontal timing, the negative sync pulses and alternate differentiated positive pulses produced by the equalizing pulses and the serrated vertical information have no

effect on horizontal timing. It can be seen that although the total sync signal (including vertical synchronizing information) is applied to the circuit of Fig. 212, only horizontal synchronization information appears at the output.

The vertical sync signal is separated from the total sync in an integrating circuit which has a time constant that is long compared with the duration of the 5-microsecond horizontal pulses, but short compared with the 190-microsecond vertical pulse width. Fig. 213 shows the general circuit configuration used, together with the input and output signals for both odd and even fields. The period between horizontal pulses, when no voltage is applied to the RC circuit, is so much longer than the horizontal pulse width that the capacitor has time to discharge almost down to zero. When the vertical pulse is applied, however, the integrated voltage across the capacitor builds

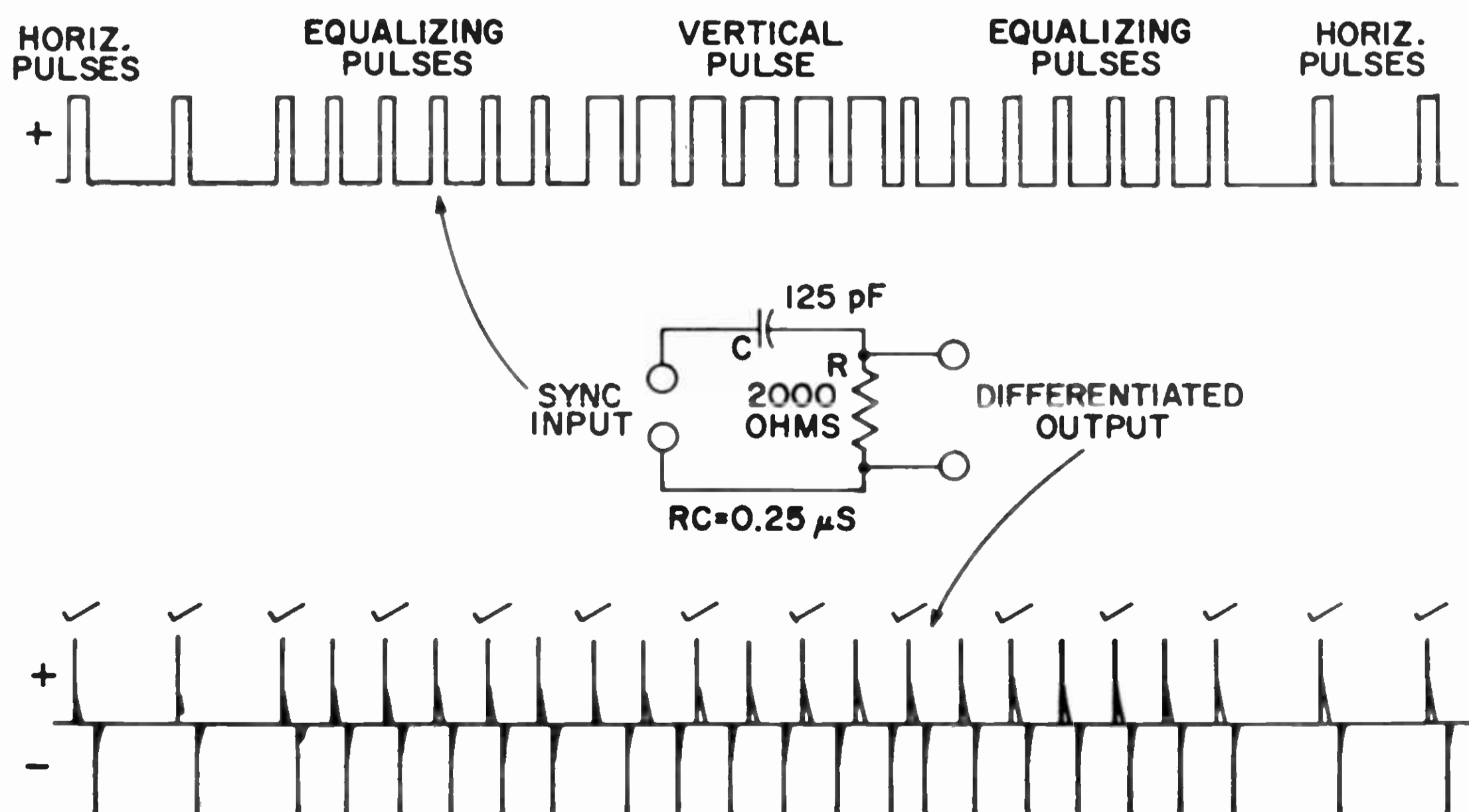


Fig. 212—Separation of the horizontal sync signals from the total sync by a differentiating circuit.

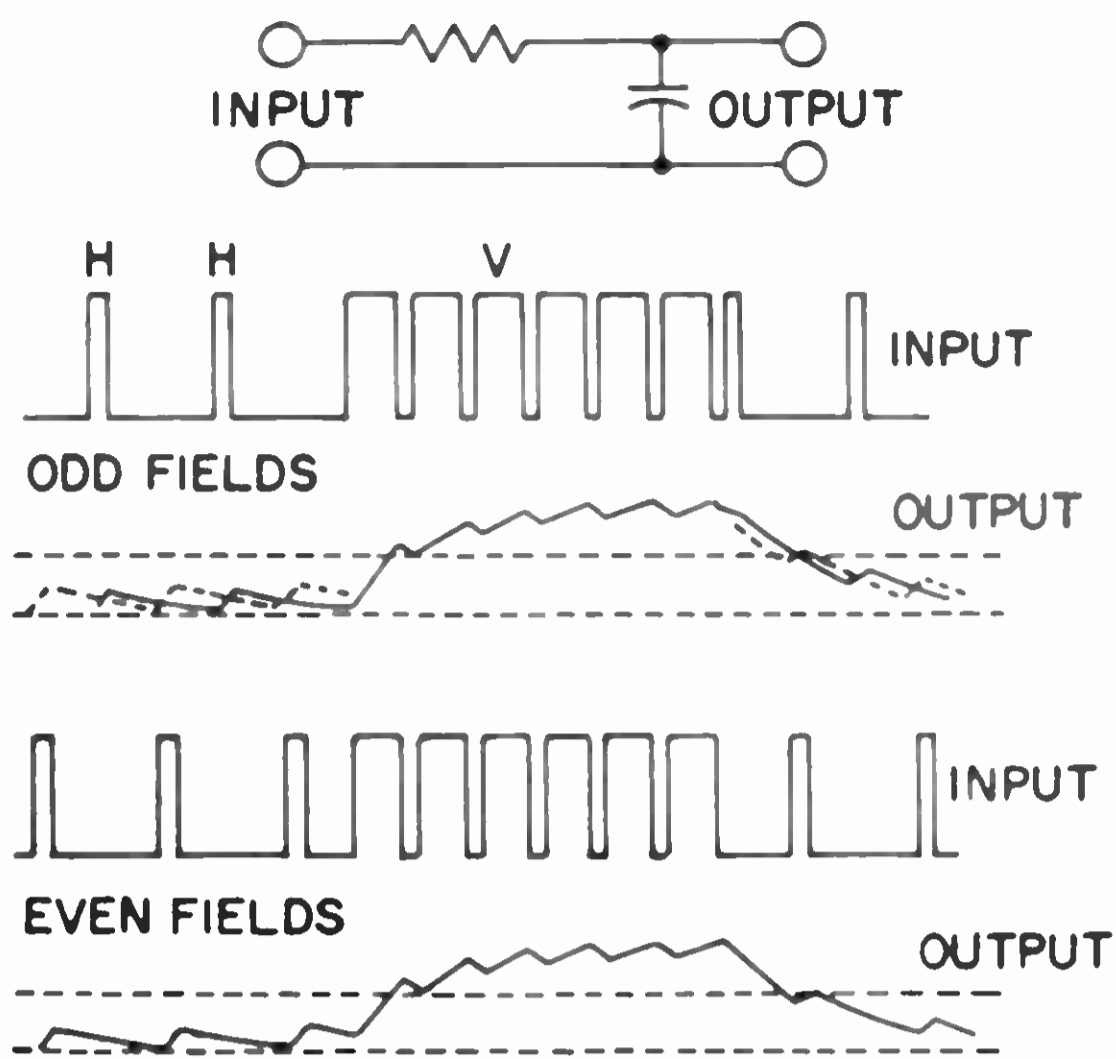


Fig. 213—Separation of vertical sync signals from the total sync for odd and even fields with no equalizing pulses. (Dashed line indicates triggering level for vertical scanning generator.)

up to the value required for triggering the vertical scanning generator. This integrated voltage across the capacitor reaches its maximum amplitude at the end of the vertical pulse, and then declines practically to zero, producing a pulse of the triangular wave shape shown for the complete vertical synchronizing pulse. Although the total sync signal (including horizontal information) is applied to the circuit of Fig. 213, therefore, only vertical synchronization information appears at the output.

The vertical synchronizing pulses are repeated in the total sync signal at the field frequency of 60 per second (59.94 per second in color systems). Therefore, the integrated output voltage across the capacitor of the RC circuit of Fig. 213 can be coupled to the vertical scanning generator to provide vertical synchronization. The six equalizing pulses immediately preceding and following the vertical pulse improve the accuracy of the vertical synchronization for better interlacing. The equalizing pulses that precede the vertical pulses make the average value of applied voltage more nearly the same for even and odd fields, so that the integrated voltage across the capacitor adjusts to practically equal values for the two fields before

the vertical pulse begins. The equalizing pulses that follow the vertical pulse minimize any difference in the trailing edge of the vertical synchronizing signal for even and odd fields.

VERTICAL DEFLECTION

The vertical-deflection circuit in a television receiver is essentially a class A audio amplifier with a complex load line, severe low-frequency requirements (much lower than 60 Hz), and a need for controlled linearity. The equivalent low-frequency response for a 10-per-cent deviation from linearity is 1 Hz. A simple circuit configuration is shown in Fig. 214.

The required performance can be obtained in a vertical-deflection circuit in any of three ways. The amplifier may be designed to provide a flat response down to 1 Hz. This design, however, requires an extremely large output transformer and immense capacitors. Another arrangement is to design the amplifier for fairly good low-frequency response and predistort the generated signal.

The third method is to provide extra gain so that feedback techniques can be used to provide linearity. If loop feedback of 20 or 30 dB is used, transistor gain variations and nonlinearities become fairly insignificant. The feedback automatically provides the necessary "predistortion" to correct low-frequency limi-

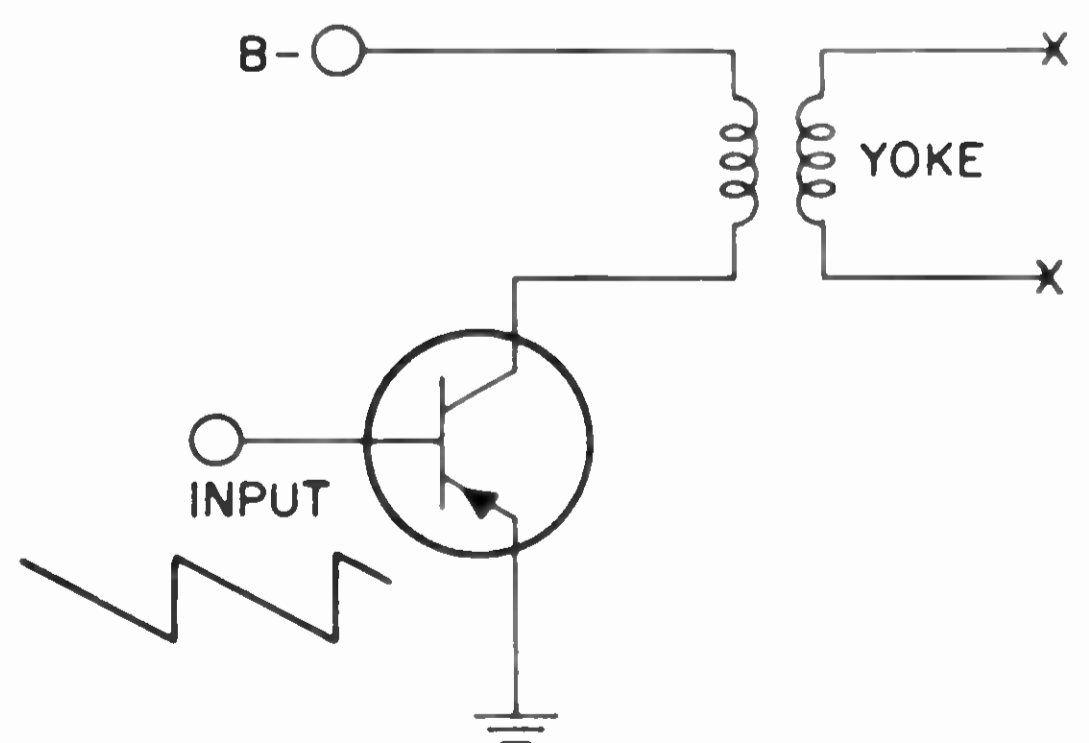


Fig. 214—Simple vertical-deflection circuit. In addition, the coupling of miscellaneous signals (such as power-supply hum or horizontal-deflection signals) in the amplifying loop is suppressed.

Fig. 215 shows a vertical-deflection system that employs bipolar and MOS transistors. A positive pulse fed back from the output circuit triggers the oscillator Q_1 . The high input impedance of the MOS transistor Q_2 , used as a predriver, permits the use of relatively large resistors and small capacitors in the gate-No.1 circuit. Negative sync is injected at gate No. 2. Only 4 to 5 volts of sync at the integrator input provides exceptionally good interlace.

The thermal compensating stage, Q_5 , provides thermal tracking during warmup and also prevents thermal runaway. The peak current of the output stage, Q_4 , is monitored by connection of the base of Q_5 to the emitter side of the emitter resistor of Q_4 . The output voltage developed at the collector of Q_5 is proportional to the peak current of the vertical output stage and is fed back to gate No.1 of the predriver Q_2 by means of the bias-linearity control. If some condition exists which causes the peak current of

the output stage to increase, the thermal-compensating transistor Q_5 conducts more heavily and causes a reduction in the average voltage at its collector. This decreasing voltage changes the bias of the predriver Q_2 . Because the predriver, driver, and output stages are all direct-coupled, the changes in the peak current of the output stage are coupled back to the base of the output stage in such a polarity as to adjust the dc operating conditions of the output stage to compensate for any change in peak current.

There are two linearity potentiometers in the circuit. The first is a bias potentiometer which sets the bias on the predriver and, in turn, on the output unit so that the output unit commences scan from cut-off. The second potentiometer is located in the integrating circuit, which shapes a sawtooth waveform taken from the output and feeds it back to gate No.1 of the predriver to provide the required parabolic correction for good linearity.

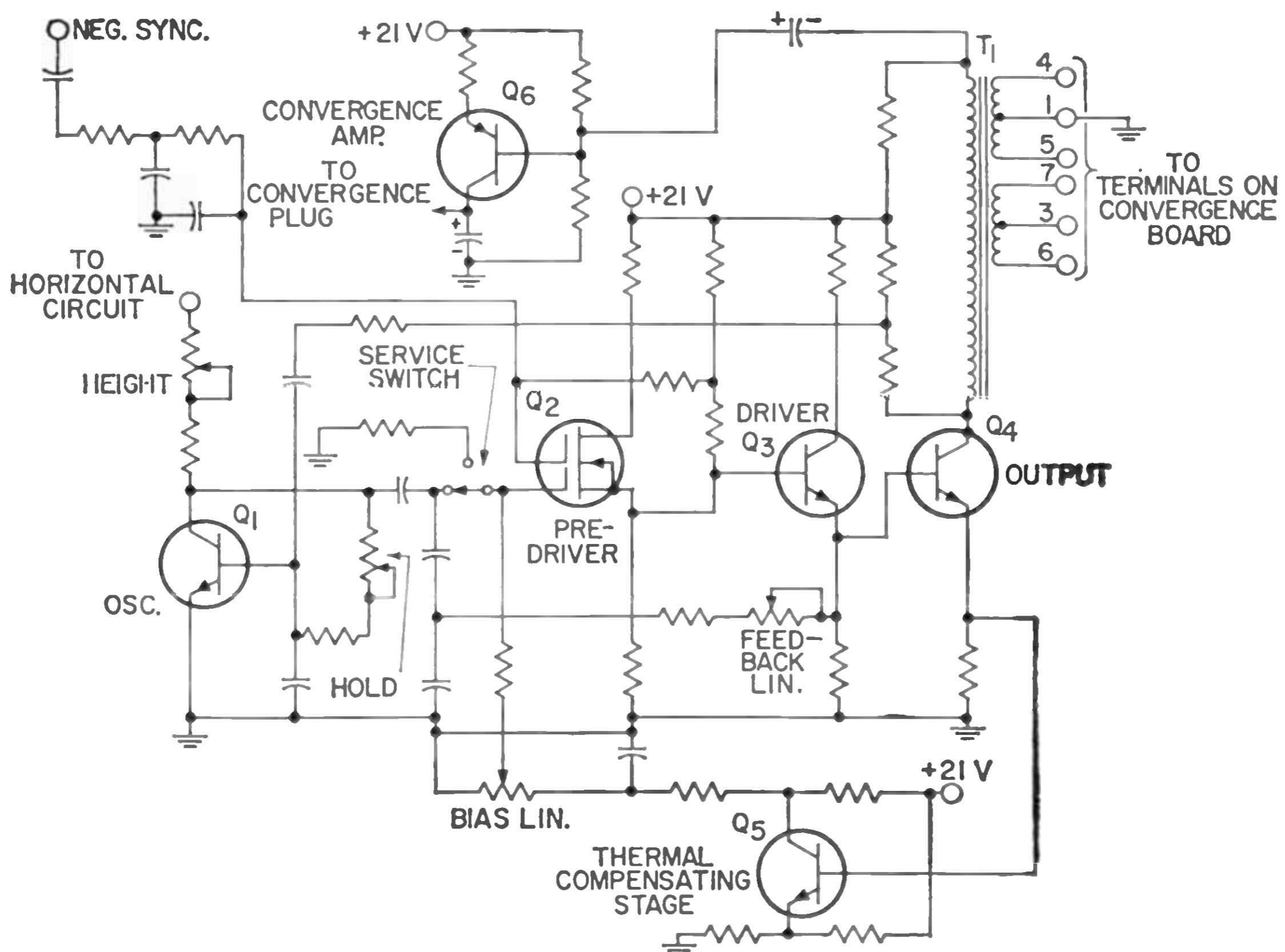


Fig. 215—Vertical-deflection circuit for color TV receiver.

The parabolic sawtooth voltage required for convergence is obtained from the collector of the output transistor Q_4 . This sawtooth voltage is coupled to the base of the convergence amplifier Q_6 and then applied to the convergence board.

For vertical blanking, the negative retrace pulse from the secondary of the vertical output transformer is amplified and inverted by a blanking transistor, and is then applied to the cathodes of the picture tube.

HORIZONTAL DEFLECTION

In the horizontal-deflection stages of a television receiver, a current that varies linearly with time and has a sufficient peak-to-peak amplitude must be passed through the horizontal-deflection-yoke winding to develop a magnetic field adequate to deflect the electron beam of the television picture tube. After the beam is deflected completely across the face of the picture tube, it must be returned very quickly to its starting point. (As explained previously, the beam is extinguished during this retrace by the blanking pulse incorporated in the composite video signal, or in some cases by additional external blanking derived from the horizontal-deflection system.)

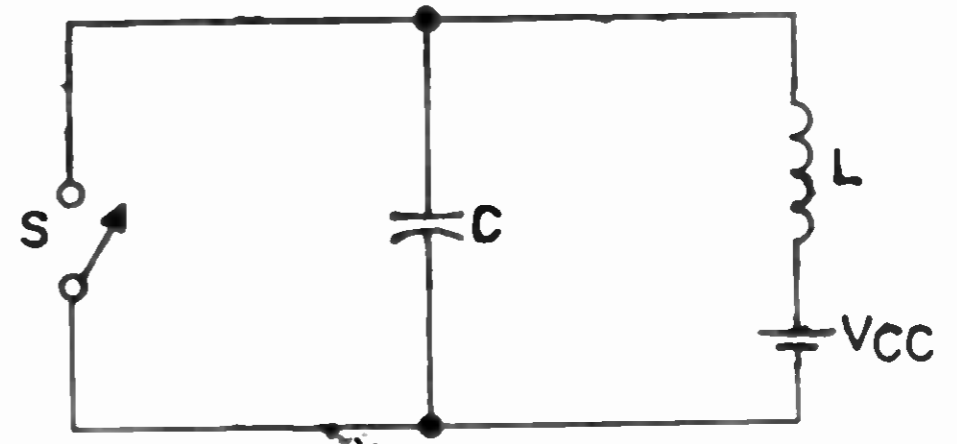
The simplest form of a deflection circuit is shown in Fig. 216(a). In this circuit, the yoke impedance L is assumed to be a perfect inductor. When the switch is closed, the yoke current starts from zero and increases linearly. At any time t , the current i is equal to Et/L , where E is the applied voltage. When the switch is opened at a later time t_1 , the current instantly drops from a value of Et_1/L to zero.

Although the basic circuit of Fig. 216(a) crudely approaches the requirements for deflection, it presents some obvious problems and limitations. The voltage across the switch becomes extremely high, theoretically approaching infinity. In addition, if very little of the total time

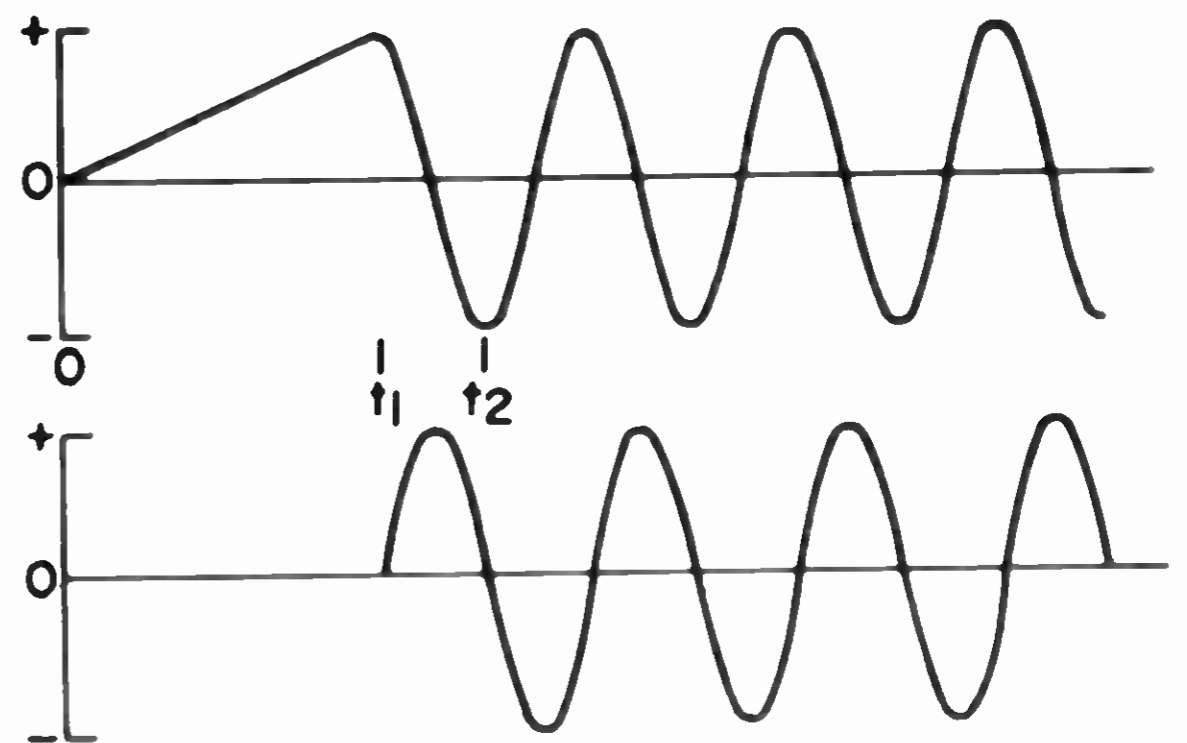
is spent at zero current, the circuit would require a tremendous amount of dc power. Furthermore, the opera-



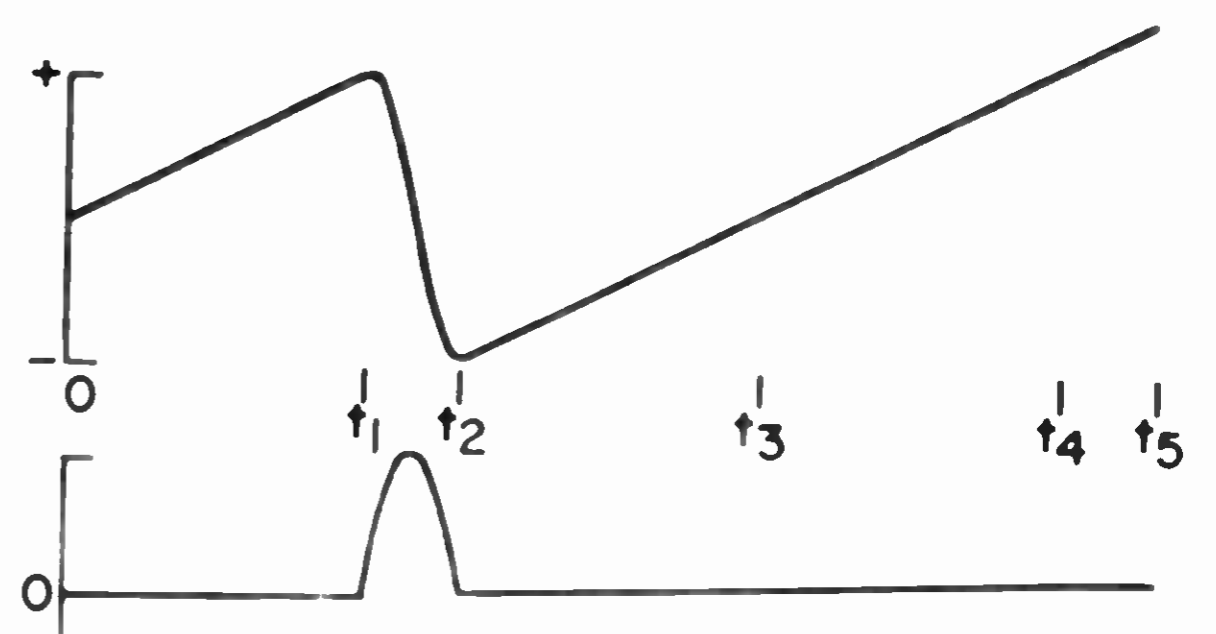
(a) SIMPLE DEFLECTION CIRCUIT



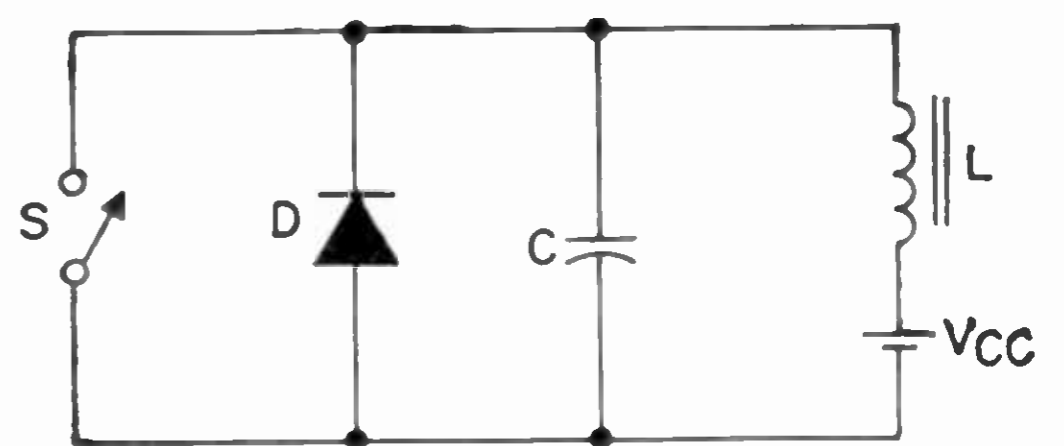
(b) ADDITION OF CAPACITOR



(c) YOKE CURRENT (top) AND SWITCH VOLTAGE (bottom) FOR CIRCUIT (b)



(d) YOKE CURRENT (top) AND SWITCH VOLTAGE (bottom) FOR SWITCH CLOSED AT t_2



(e) ADDITION OF DAMPER DIODE

Fig. 216—Development of horizontal-deflection circuit.

tion of the switch would be rather critical with regard to both its opening and its closing. Finally, because the deflection field would be phased in only one direction, the beam would have to be centered at the extreme left of the screen for zero yoke current.

If a capacitor is placed across the switch, as shown in Fig. 216(b), the yoke current still increases linearly when the switch is closed at time $t = 0$. However, when the switch is opened at time $t = t_1$, a tuned circuit is formed by the parallel combination of L and C . The resulting yoke currents and switch voltages are then as shown in Fig. 216(c). The current is at a maximum when the voltage equals zero, and the voltage is at a maximum when the current equals zero. If it is assumed that there are no losses, the ringing frequency f_{osc} is equal to $1/(2\pi\sqrt{LC})$.

If the switch is closed again at any time the capacitor voltage is not equal to zero, an infinite switch current flows as a result of the capacitive discharge. However, if the switch is closed at the precise moment t_2 that the capacitor voltage equals zero, the capacitor current effortlessly transfers to the switch, and a new transient condition results. Fig. 216(d) shows the yoke-current and switch-voltage waveforms for this new condition.

If the switch is again opened at t_4 , closed at t_5 , and so on, the desired sweep results, the peak switch voltage is finite, and the average supply current is zero. The deflection system is then lossless and efficient and, because the average yoke current is zero, beam decentering is avoided. The only fault of the circuit of Fig. 216(b) is the critical timing of the switch, particularly at time $t = t_2$. However, if the switch is shunted by a damper diode, as shown in Fig. 216(e), the diode acts as a closed switch as soon as the capacitor voltage reverses slightly. The switch may then be closed at any time between t_2 and t_3 .

In horizontal-deflection circuits, the switch can be a transistor, as shown in Fig. 217. Although the transistor is forward-biased prior to t_3 , it is not an effective switch for the reverse collector current; therefore, the damper diode carries most of this current. High voltage is generated by use of the step-up transformer T_1 in parallel with the yoke. This step-up transformer is designed so that its leakage inductance, distributed capacitance, and output stray capacitance complement the yoke inductance and retrace tuning capacitance in such a manner that the peak voltage across the primary winding is reduced and the peak volt-

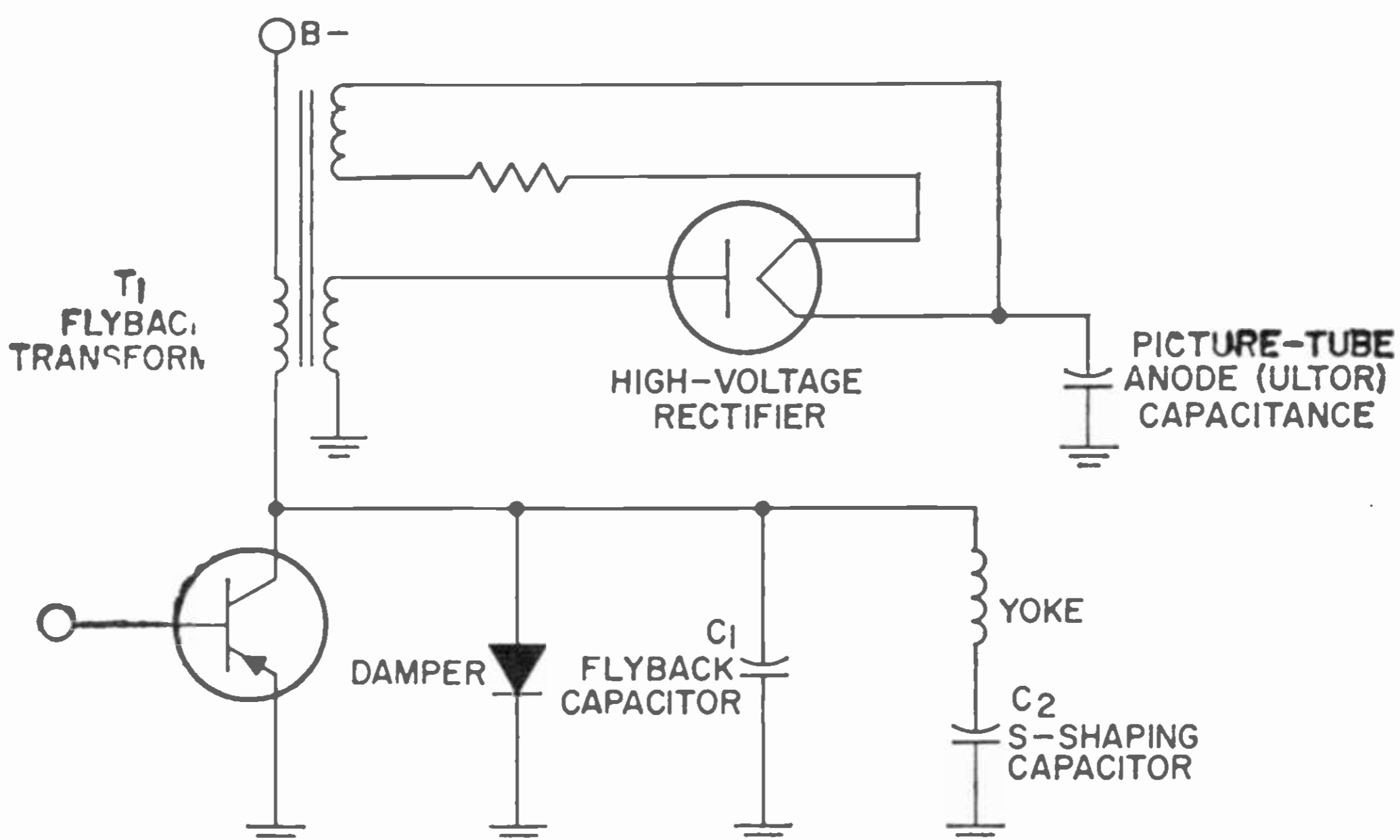


Fig. 217—Simple transistor horizontal-deflection circuit.

age across the secondary winding is increased, as compared to the values that would be obtained in a perfect transformer. This technique, which is referred to as "third-harmonic tuning", yields a voltage ratio of secondary-to-primary peak voltage of approximately 1.7 times the value expected in a perfect transformer.

To provide linearity correction for wide-angle television picture tubes, it is necessary to retard the sweep rate at the beginning and end of scan. Therefore, a suitable capacitor C_2 is placed in series with the yoke, as shown in Fig. 217, so that the direct current required to replenish circuit losses is fed through the flyback-transformer primary. A parabolic waveform is then developed across C_2 (called the S-shaping capacitor) so that the trace voltage across the yoke is less at the ends of the sweep than in the middle of the sweep. (This capacitor actually provides a series resonant circuit tuned to approximately 5 kHz so that an S-shaped current portion of a sine wave re-

sults.) It is desirable to place the S-shaping capacitor and the yoke between the collector and the emitter of the transistor so that the yoke current does not have to flow through the power supply.

The highest anticipated peak voltage across the transistor in Fig. 217 is a function of the dc voltage obtained at high ac line voltage and at the lowest horizontal-oscillator frequency. (At these conditions, of course, the receiver is out of sync.) The tolerance on the inductors and capacitors alters the trace time only slightly and usually may be ignored if a 10-per-cent tolerance is used for the tuning capacitor.

Fig. 218 shows a schematic of a transistorized horizontal-deflection circuit for a color TV receiver. The horizontal output transistor, Q_5 , is a high-voltage silicon transistor. The normal collector-to-emitter pulse voltage across Q_5 includes an ample safety factor that allows for any increased pulse that may result from out-of-sync opera-

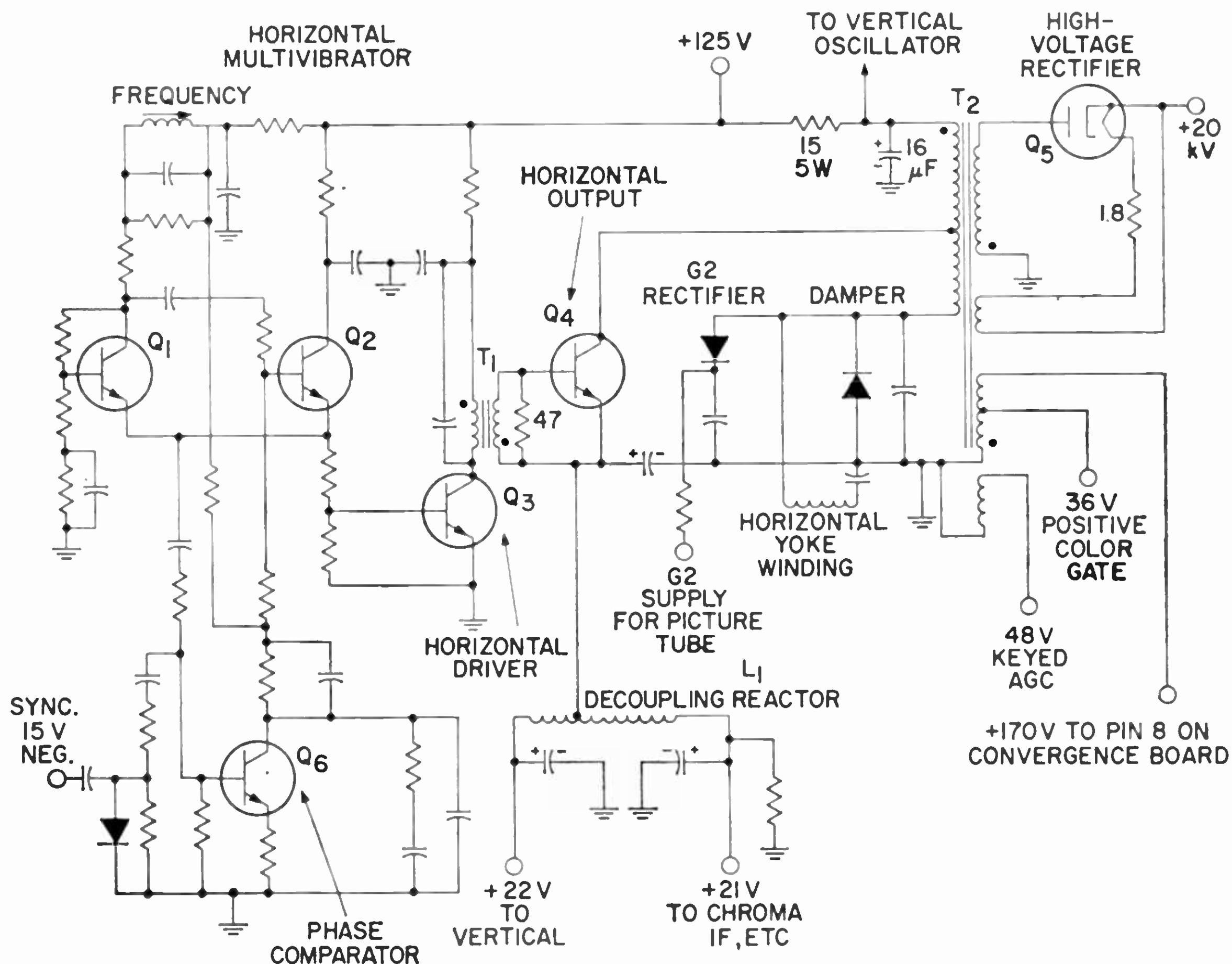


Fig. 218—Horizontal-deflection circuit and high-voltage and low-voltage power supplies.

tion, line surges, and other abnormal conditions.

A unique feature of the horizontal-deflection circuit is the low-voltage supply of approximately 23 volts that is derived from it. This feature makes it possible to eliminate the power transformer in the power supply. The low-voltage power is used to operate all but the high-voltage receiver stages, such as the video-output stage, the audio-output stage, and the horizontal oscillator and driver. The vertical oscillator is supplied from the same point which supplies the horizontal output in such a way that the actual voltage is a function of beam current; this connection compensates for the tendency for picture height to change with brightness settings.

The transistorized deflection circuit achieves commercially acceptable high-voltage regulation without the use of the high-voltage shunt regulator used with tube-type deflection circuits. With a flyback transformer of normal design and a low-voltage power supply with about 3-per-cent regulation, high-voltage regulation from zero beam to full load of 750 microamperes is about 3 kilovolts and is accompanied by a considerable increase in picture width. Improvement of this behavior with brightness changes is achieved by utilizing the accompanying changes of direct current to the deflection circuit in two ways. First, the air gap of the transformer is reduced to permit core saturation to decrease the system inductance as the high-voltage load is increased. When this method is used, regulation is improved to about half that of the normal transformers with no circuit instabilities, but picture-width change is still greater than desired. Second, series resistance is added to the B supply to decrease power input at full load and thereby reduce the change in picture width (at some sacrifice in high-voltage regulation). The net result of both changes is a regulation of about 2.8 kilovolts for the

high voltage, with very little variation in picture size.

A secondary benefit of the inherently good regulation of the transistor deflection system is a reduction in the size of the flyback transformer. The size reduction is accomplished by a reduction in the area of the "window" in the flyback core. A reduction in the size of the high-voltage cage required to maintain adequate isolation of the high-voltage winding from ground is possible because of the smaller flyback transformer.

The transformer-coupled driver stage takes advantage of the high-voltage capability and switching speed of the horizontal driver transistor which is designed primarily for video-output use. A sine-wave stabilized multivibrator type of horizontal oscillator is used. This type of oscillator is especially useful in experimental work with deflection systems because it permits on-time and off-time periods to be easily varied.

The afc phase detector operates on the principle of pulse-width variation of combined sync and reference pulses. In the circuit shown in Fig. 218, timing information is related to the leading edges of the sync pulses, and the retrace process is initiated prior to the leading edge of the sync pulse; performance of the circuit is very satisfactory.

A highly reliable horizontal-deflection system for color-television receivers has been using silicon controlled rectifiers. This system illustrates a new approach to horizontal-circuit design that represents a complete departure from the approaches currently used in commercial television receivers. The switching action required to generate the scan current in the horizontal-yoke windings and the high-voltage pulse used to derive the dc operating voltages for the picture tube is controlled by two SCR's that are used in conjunction with associated fast-recovery diodes to form bipolar switches.

The SCR's used to control the trace current and to provide the commutating action to initiate trace-retrace switching exhibit high voltage- and current-handling capabilities together with the excellent switching characteristics required for reliable operation in deflection-system applications. The switching diodes, (trace and commutating diodes), provide fast recovery times, high reverse-voltage blocking capabilities, and low turn-on voltage drops. These features and the fact that, with the exception of one non-critical triggering pulse, all control voltages, timing, and control polarities are supplied by passive elements within the system (rather than by external drive sources) contribute substantially to the excellent reliability of the SCR deflection system.

Fig. 219 shows the circuit configuration of the complete horizontal-deflection system. The system operates directly from a conventional, unregulated dc power supply of +155 volts, and provides full-screen deflection at angles up to 90 degrees at full beam current. The current and voltage waveforms required for horizontal deflection and

for generation of the high voltage are derived essentially from LC resonant circuits. As a result, fast and abrupt switching transients which would impose strains on the solid-state device are avoided.

A regulator stage is included in the SCR horizontal-deflection circuit to maintain the scan and the high voltage within acceptable limits with variations in the ac line voltage or picture-tube beam current. The system also contains circuits that provide full protection against the effects of arcs in the picture tube or the high-voltage rectifier, and linearity and pincushion correction circuits.

The SCR horizontal-deflection system employs two bidirectional switches, each of which consists of an SCR and a diode in an inverse parallel connection. Fig. 220 shows a simplified schematic of the basic deflection circuit. SCR_T and diode D_T are used to control the current in the yoke winding L_y during the trace interval; SCR_C and diode D_C provide the commutating action required for retrace.

At the beginning of the trace interval, the trace-switch diode con-

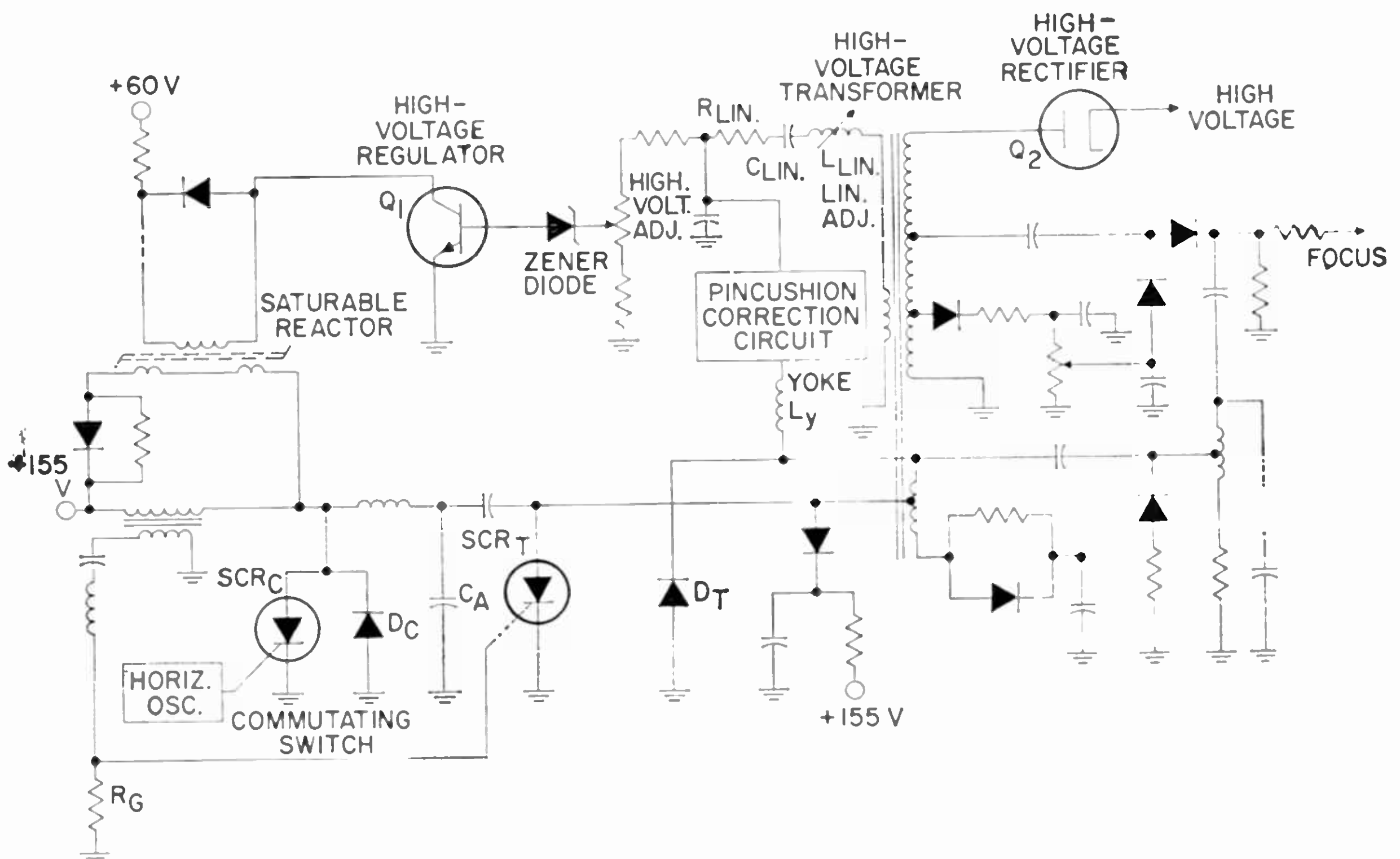


Fig. 219—General circuit configuration of the over-all SCR horizontal-deflection system.

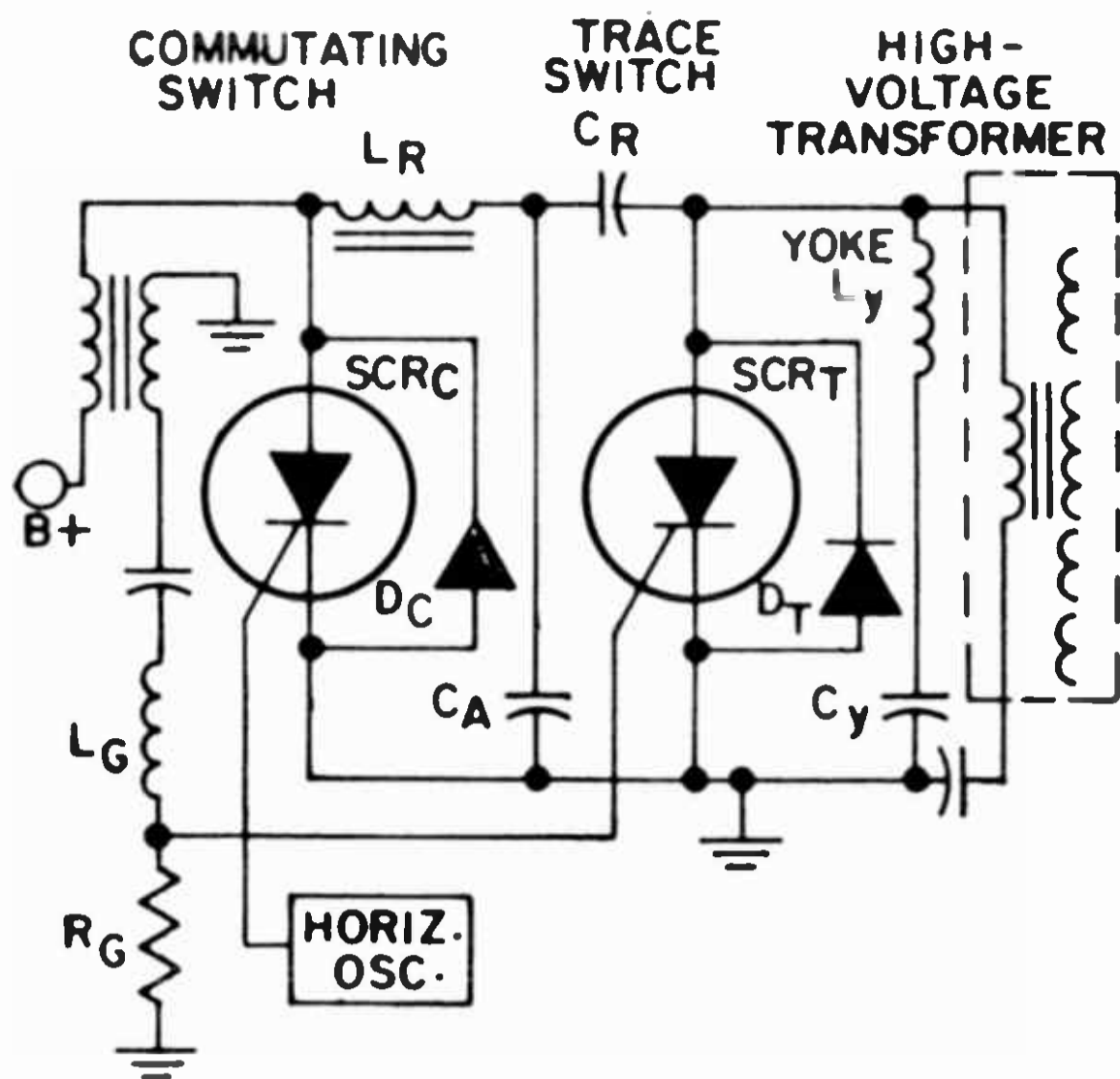


Fig. 220—Basic circuit for generation of the deflection-current waveform in the horizontal-yoke winding.

ducts the yoke current established during previous circuit action. The trace-switch diode conducts a linearly decreasing current until the yoke current reaches zero to produce the first half of the scan current. Before the zero-yoke-current point is reached, the trace-switch SCR is made ready to conduct by application of a positive pulse to its gate electrode. When the yoke current crosses the zero point from negative to positive, the current transfers from the trace-switch diode to the trace-switch SCR. Capacitor C_y then begins to discharge through the trace-switch SCR to supply current to yoke winding L_y during the second half of the trace interval. The voltage across capacitor C_y remains essentially constant throughout the trace-retrace cycle. This constant voltage results in a linearly rising current through the yoke winding to complete the trace period.

Just prior to the end of trace, the commutating-switch SCR is gated on by the horizontal oscillator. Capacitor C_R then discharges a pulse of current through inductor L_R and the trace and commutating SCR's. This current pulse, referred to as the commutating pulse, increases until it exceeds the yoke current and thereby causes the trace diode D_T to turn on. The conduction of diode D_T re-

verse-biases the trace SCR for sufficient time to allow it to turn off. When the commutating pulse declines to a value less than the yoke current, diode D_T opens, and the energy in the yoke winding produces a current that charges the retrace capacitors C_R and C_A during the first half of retrace. This current then rings back into the yoke winding during the second half of retrace. The circuit for the ringing oscillation during the second half of retrace is completed through the commutating-switch diode and allows sufficient time for the commutating-switch SCR to turn off. When the yoke current reaches its peak negative value, the trace-switch diode begins to conduct to start the trace interval.

During the time the commutating switch is closed, the input inductor L_{cc} is connected across the $B+$ supply, and energy is stored in this inductor. This stored energy charges the retrace capacitors C_R and C_A to replenish the energy loss in the circuit.

Fig. 221 shows the current and voltage waveforms applied to the trace and commutating switches as a result of the circuit actions described in the preceding paragraphs.

The SCR horizontal-deflection system offers a number of distinct advantages over the conventional types of systems currently used in commercial television receivers. The following list outlines some of the more significant circuit features of the SCR deflection system and points out the advantage derived from each of them:

1. Critical voltage and current waveforms, and timing cycles are determined by passive components in response to the action of two SCR-diode switches. The stability of the system, therefore, is determined primarily by the passive components. When the passive components are properly adjusted, the system exhibits highly predictable perform-

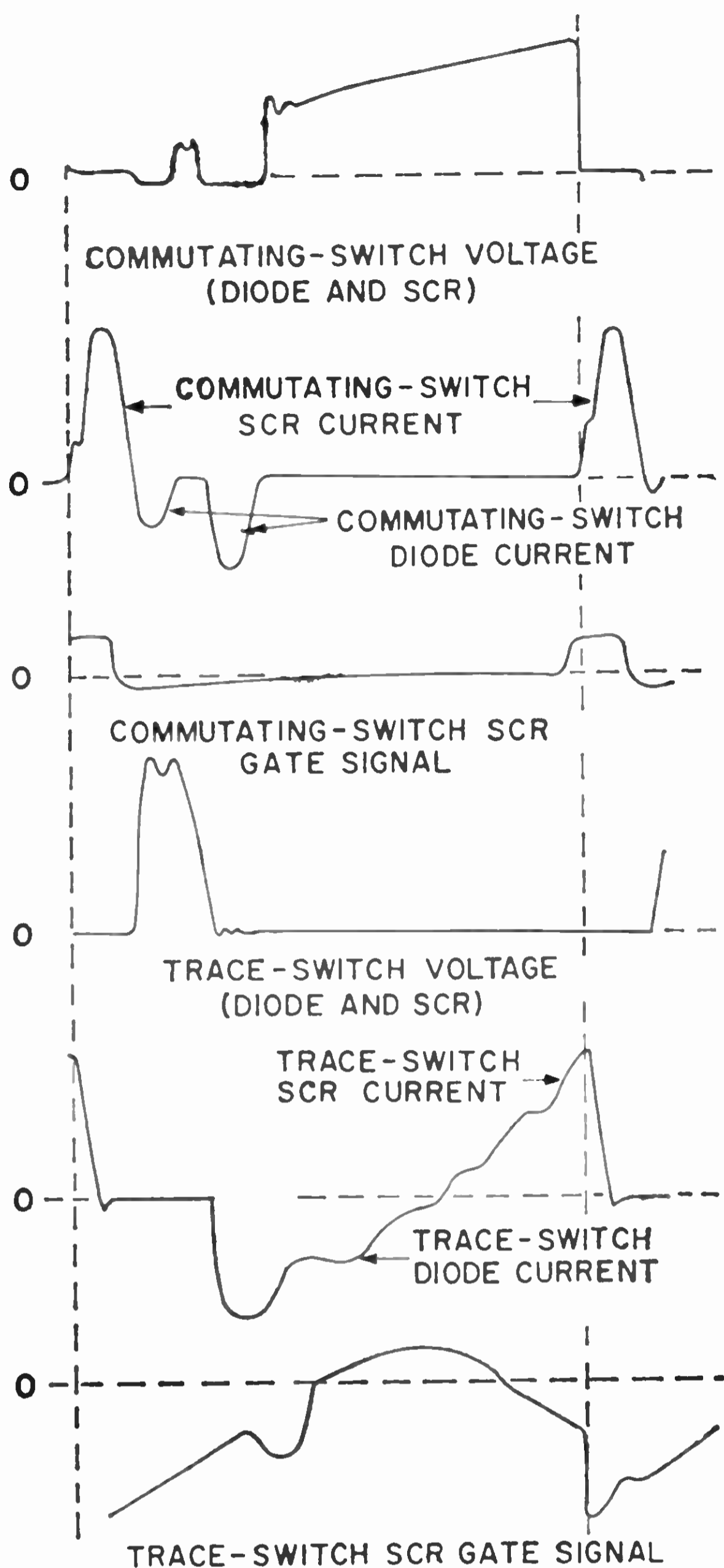


Fig. 221—Voltage and current waveforms applied to the switching SCR's and diodes in the horizontal-deflection system.

ance characteristics and exceptional operational dependability.

2. The only input drive signal required for the SCR deflection system is a low-power pulse which has no stringent accuracy specification in relation to either amplitude or time duration. The deflection system, therefore, can be driven directly from a pulse developed by the horizontal oscillator.

3. This deflection system is unique in that, although it operates from a conventional B+ supply of +155 volts, the flyback pulse is less than 500 volts. This level of voltage stress is substantially less than that

in conventional line-operated systems, and this factor contributes to improved reliability of the switching devices.

4. Regulation in the SCR deflection system is accomplished by control of the energy stored by a reactive element. This technique avoids the use of resistive-load regulating elements required by many other types of systems and, therefore, makes possible higher over-all system efficiency and reduces input-power requirements.

5. All switching occurs at the zero current level through the reverse recovery of high-voltage p-n junctions in the deflection diodes. The diode junctions are not limited in volt-ampere switching capabilities for either normal or abnormal conditions in the circuit.

COLOR DEMODULATION

In the transmission of picture signals for color-television receivers, all the color information is contained in three signals, a luminance (black-and-white) or monochrome signal and two chrominance signals. The luminance signal, which is called the Y signal, contains brightness information only. The voltage response of the Y signal is made similar to the brightness response of the human eye by use of a composite signal that contains definite proportions of the red, green, and blue signals from the color-television camera (30 per cent red, 59 per cent green, and 11 per cent blue). This Y signal, which includes sync and blanking pulses, provides a correct monochrome picture in a conventional black-and-white television receiver.

For the generation of color-television signals, the Y signal is subtracted from the red, green, and blue signals to provide a new set of color-difference signals, which are designated as R-Y, B-Y, and G-Y. All of the original picture information is contained in the Y signal, the R-Y signal, and the B-Y signal.

Therefore, the G-Y signal is not contained in the transmitted signal, but is synthesized in the receiver by proper combinations of the R-Y and B-Y signals.

(Color signals transmitted under present color-television standards are not R-Y and B-Y, but a similar pair of signals designated as I and Q. In the color-television receiver, R-Y and B-Y signals are demodulated directly from the I and Q signals with negligible loss of color quality. For purposes of simplicity, only R-Y and B-Y signals are considered in this explanation. In addition, a 90-degree phase-shift network is shown; the phase-shift angle could be, and often is, some other value.)

Because the luminance signal and the two color-difference signals must be transmitted with a standard 6-MHz channel, the two color signals are combined into one signal at the transmitter and are independently recovered at the receiver by proper detection techniques. A color subcarrier of approximately 3.58 MHz is used for transmitting the color information within the 6-MHz spectrum of the television station. As shown in Fig. 222, the 3.58-MHz subcarrier and one of the color-difference signals are applied directly to a balanced AM modulator. The other color-difference signal is applied directly to a second balanced AM modulator, and the 3.58-MHz subcarrier is applied to this second modulator through a 90-degree phase-shifting network. The

balanced modulators effectively cancel both the individual color-difference signals and the subcarrier signal, and the output contains only the sidebands of the combined chrominance signal.

Recovery of the color information at the receiver involves a process called **synchronous detection**. In this process, two separate detectors are used to recover the separate color information, just as two separate modulators were used to combine the information at the transmitter. The 3.58-MHz subcarrier, which was suppressed during transmission, must be reinserted at the receiver for recovery of the color information. The basis of synchronous detection is the phase relationship of this reinserted 3.58-MHz subcarrier.

For example, the original color information is represented in Fig. 222 by the color-difference signals A and B. At the receiver, the combined color signal is fed to two demodulators A and B, as shown in Fig. 223. At the same time, a 3.58-MHz subcarrier is also fed to the two demodulators, with the same phase relationship that was used in the modulators at the transmitter. This locally generated subcarrier essentially duplicates or replaces the original subcarrier, which was removed at the transmitter.

The local 3.58-MHz oscillator in the color-television receiver is made to function at the proper frequency and phase by means of a synchronizing signal sent out by the transmitter. This synchronizing signal

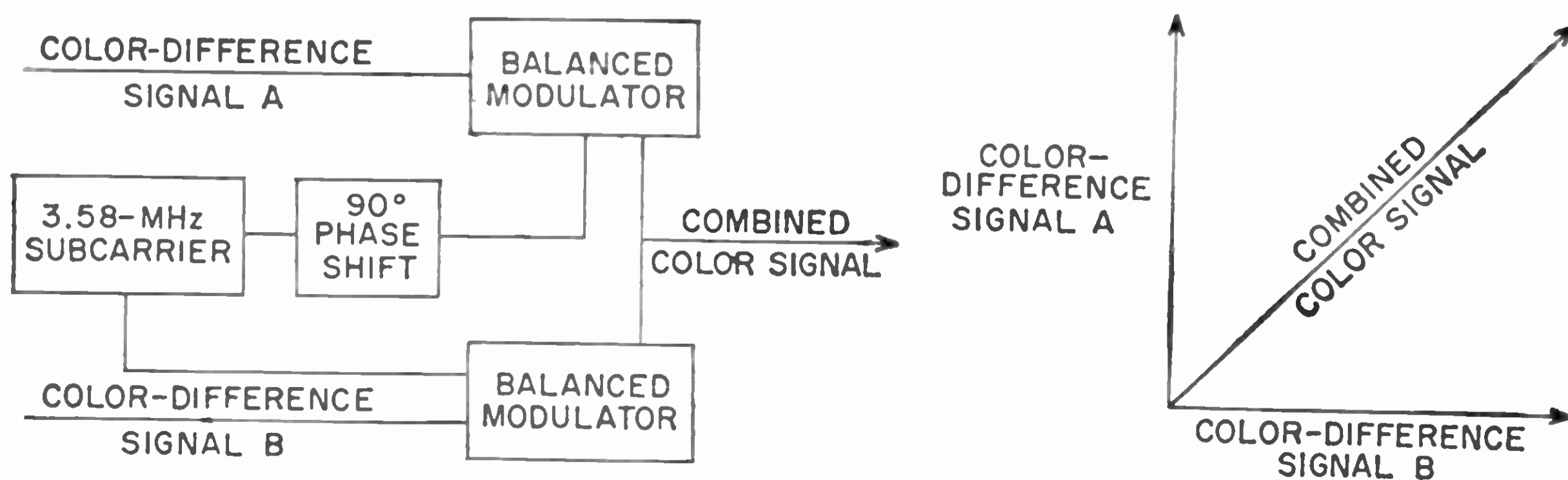


Fig. 222—Formation of combined color signal for transmission.

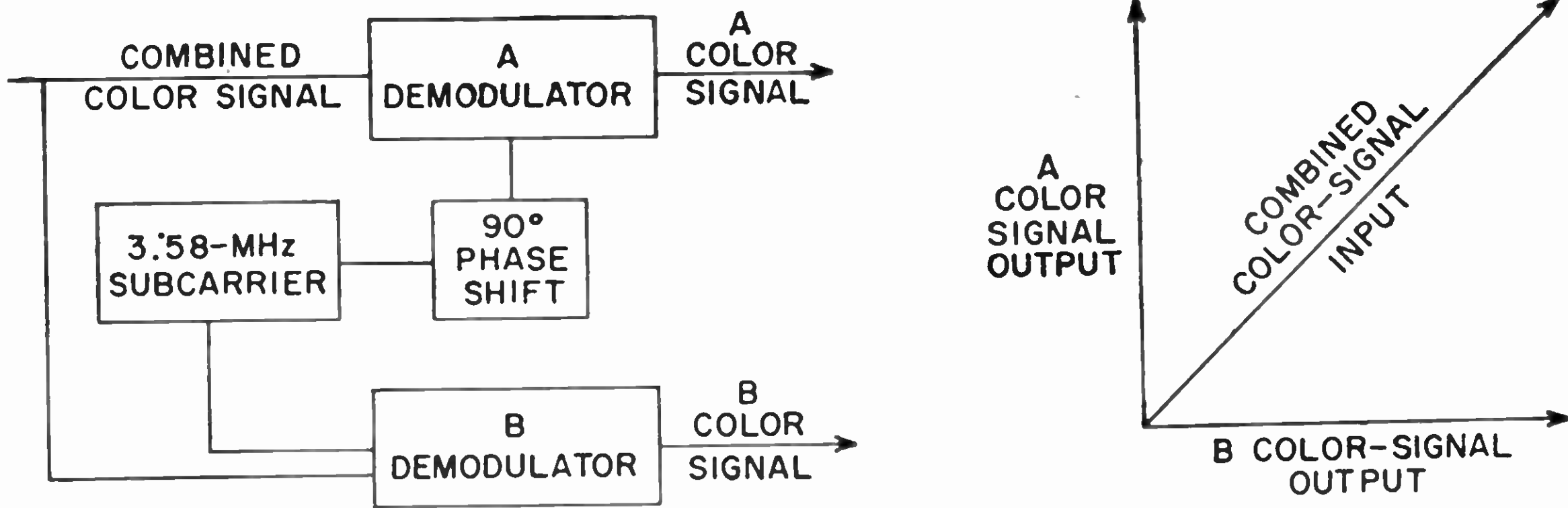


Fig. 223—Separation of combined color signal into two signals at the receiver.

consists of a short burst of 3.58-MHz signals transmitted during the horizontal blanking interval, immediately after the horizontal sync pulse, as shown in Fig. 224.

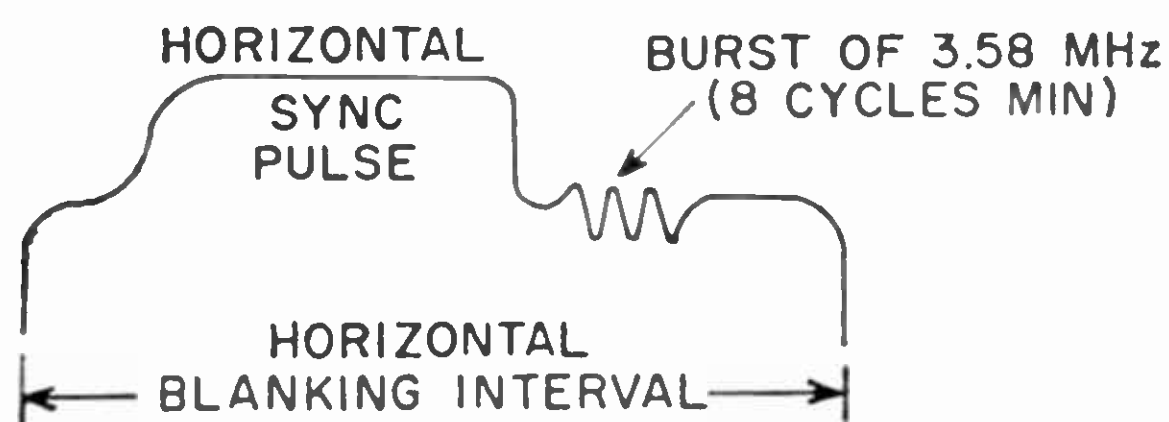


Fig. 224—Waveform for synchronizing signal.

The dual-gate MOS transistor is especially adaptable for use in color demodulator circuits of color TV receivers. Transistors of this type have the necessary high transconductance, good inherent limiting, and more than adequate output to drive the difference amplifiers with their associated matrix. Use of a dual-gate MOS transistor make possible the design of a color-demodulation circuit that is simple, that provides gain, and that minimizes problems in cross-coupling and oscillator limiting. The use of bipolar transistors or diodes causes problems in balancing and oscillator limiting as well as loss of gain. Because the low drain-to-gate capa-

citance of the MOS transistors results in minimum feedback from output to input, there is excellent isolation and resulting device stability.

Fig. 225 shows the complete schematic diagram for the R-Y and B-Y color-demodulator circuits in a receiver. Except for the lower supply voltage and difference in component values, this circuit is identical with that used in tube-type color receivers. The chroma signals are applied to gate No. 2 of demodulators Q_1 and Q_2 . The 3.58-MHz local-oscillator signal is applied, in the appropriate phase, to gate No. 1 of each demodulator. The LR network in the gate-No. 1 input to modulator Q_1 shifts the phase of the 3.58-MHz local-oscillator signal applied to this stage. The phase of the 3.58-MHz continuous-wave signal determines the color-difference signal (B-Y or R-Y) at the output of each demodulator. For highest efficiency and maximum AM rejection of any extraneous 3.58-MHz cw signal modulation, gate No. 1 is normally overdriven by the local-oscillator signal. The low-pass pi filter at the output of each demodulator removes the 3.58-MHz carrier signal and passes the demodulated video information.

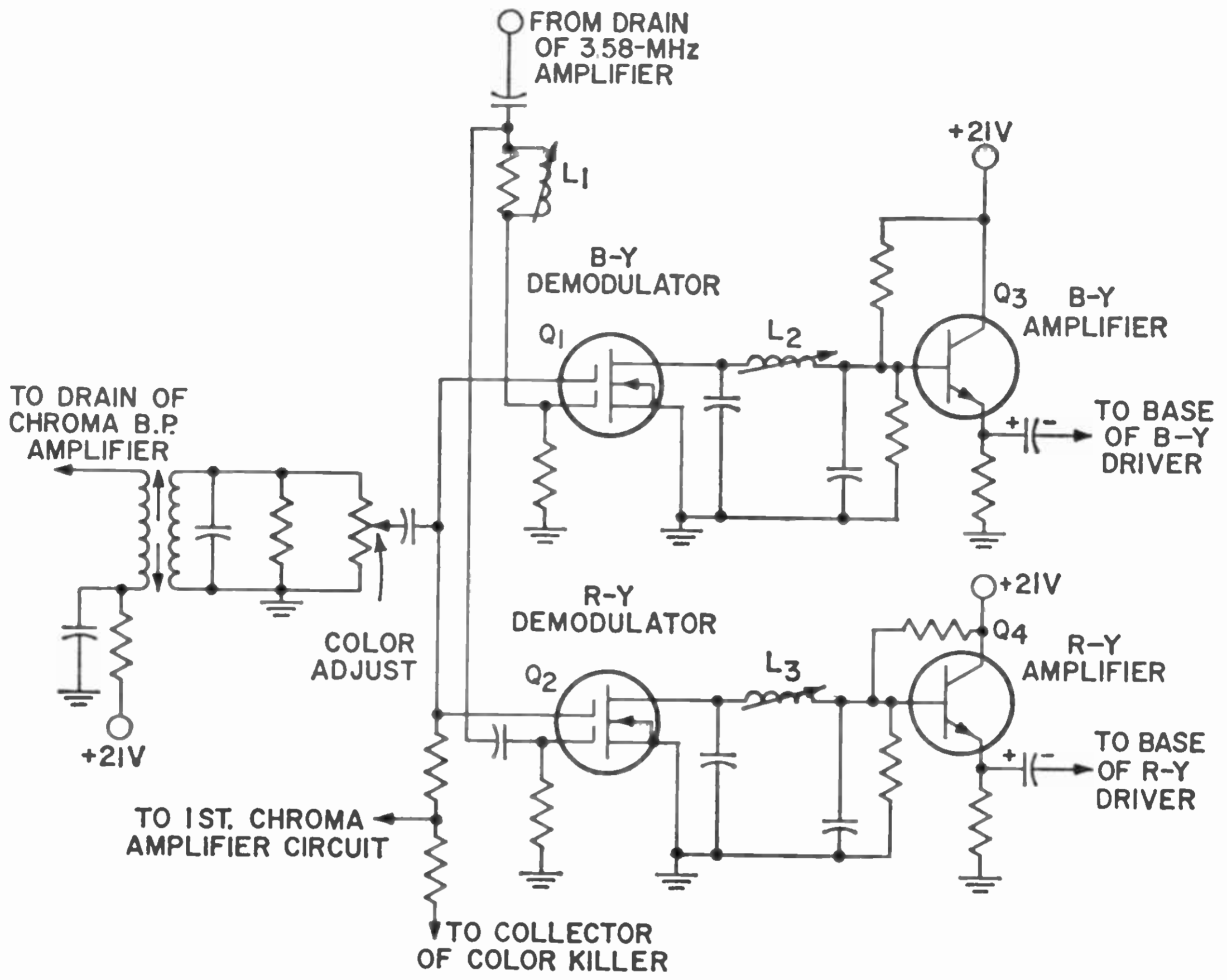


Fig. 225—Color-demodulator circuit.

Power Switching and Control

Transistors have already established themselves in switching applications in radar, television, telemetering, pulse code communications, and computing equipment. More recently, triacs, diacs, and SCR's have been used in these applications and in arc-lamp ballasting circuits, automobile ignition systems, and heat, light, and motor controls. This section describes the circuits used in these applications and discusses special consideration required for their operation.

NONSINUSOIDAL OSCILLATORS

Oscillator circuits which produce nonsinusoidal output waveforms use a regenerative circuit in conjunction with resistance-capacitance (RC) or resistance-inductance (RL) components to produce a switching action. The charge and discharge times of the reactive elements (which are directly proportional to $R \times C$ or L/R) are used to produce sawtooth, square, or pulse output waveforms.

The switching action in a nonsinusoidal oscillator occurs when an externally applied signal causes an instantaneous change in the operating state of the circuit; when this instantaneous change occurs the circuit is said to be triggered. Triggered circuits may be astable, monostable, or bistable.

Astable triggered circuits have no stable state; they operate in the active linear region and produce relaxation-type oscillations. A **monostable** circuit has one stable state

in either of the stable regions (cut-off or saturation); an external pulse "triggers" the transistor to the other stable region, but the circuit then switches back to its original stable state after a period of time determined by the time constants of the circuit elements. A **bistable (flip-flop)** circuit has a stable state in each of the two stable regions. The transistor is triggered from one stable state to the other by an external pulse, and a second trigger pulse is required to switch the circuit back to its original stable state.

The multivibrator circuit shown in Fig. 226 is an example of a monostable circuit. The bias network holds transistor Q_2 in saturation and transistor Q_1 at cutoff during the quiescent or steady-state period. When an input signal is applied through the coupling capacitor C_1 , however, transistor Q_1 begins to conduct. The decreasing collector voltage of Q_1 (coupled to the base of Q_2 through capacitor C_2) causes the base current

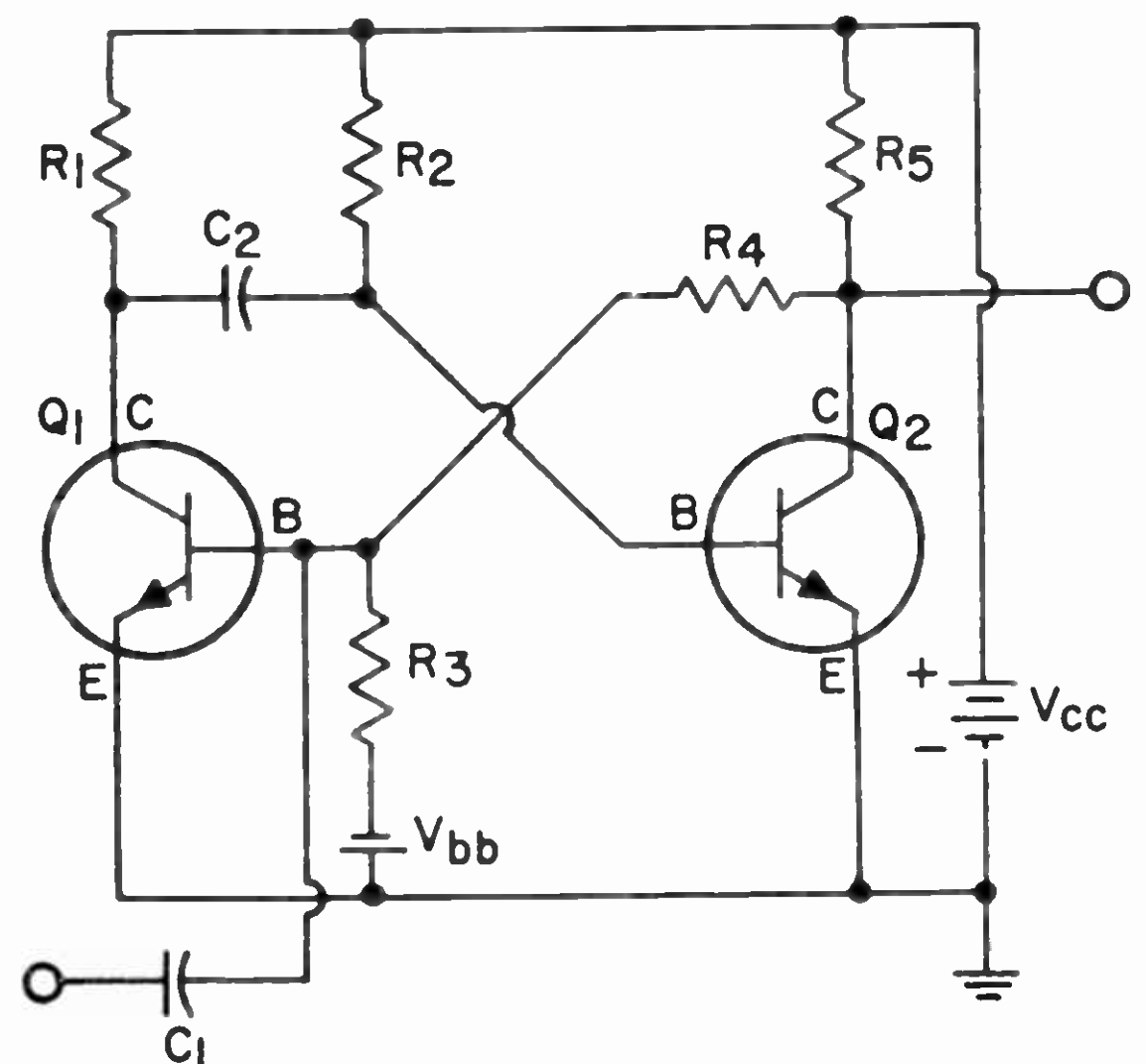


Fig. 226—Monostable multivibrator.

and collector current of Q_2 to decrease. The increasing collector voltage of Q_2 (coupled to the base of Q_1 through resistor R_4) then increases the forward base current of Q_1 . This regeneration rapidly drives transistor Q_1 into saturation and transistor Q_2 into cutoff. The base of transistor Q_2 at this point is at a negative potential almost equal to the magnitude of the battery voltage V_{cc} .

Capacitor C_2 then discharges through resistor R_2 and the low saturation resistance of transistor Q_1 . As the base potential of Q_2 becomes slightly positive, transistor Q_2 again conducts. The decreasing collector potential of Q_2 is coupled to the base of Q_1 and transistor Q_1 is driven into cutoff, while transistor Q_2 becomes saturated. This stable condition is maintained until another pulse triggers the circuit. The duration of the output pulse is primarily determined by the time constant of capacitor C_2 and resistor R_2 during discharge. In other words, the oscillating frequency of the multivibrator is determined by the values of resistance and capacitance in the circuit.

The Eccles-Jordan type multivibrator circuit shown in Fig. 227 is an example of a bistable circuit. The resistive and bias values of this circuit are chosen so that the initial application of dc power causes one transistor to be cut off and the other to be driven into saturation. Because of the feedback arrangement, each transistor is held in its original state by the condition of the other. The application of a positive trigger pulse to the base of the OFF transistor or a negative pulse to the base of the ON transistor switches the conducting state of the circuit. The new condition is then maintained until a second pulse triggers the circuit back to the original condition.

In Fig. 227, two separate inputs are shown. A trigger pulse at input A will change the state of the circuit. An input of the same polarity at input B or an input of opposite polarity at input A will then return the

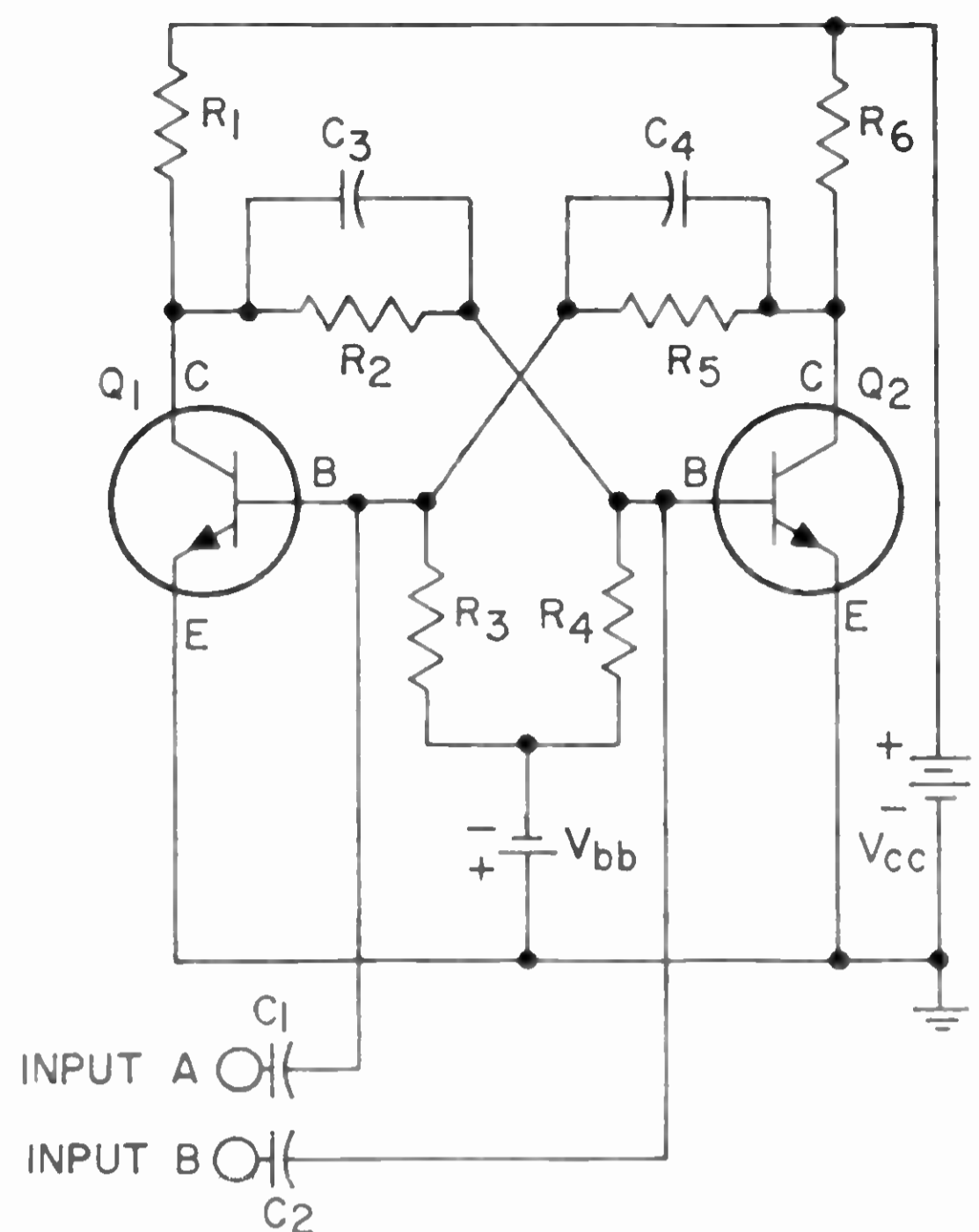


Fig. 227—Eccles-Jordan type bistable multivibrator.

circuit to its original state. (Collector triggering can be accomplished in a similar manner.) The capacitors C_3 and C_4 are used to speed up the regenerative switching action. The output of the circuit is a unit step voltage when one trigger is applied, or a square wave when continuous pulsing of the input is used.

A blocking oscillator is a form of nonsinusoidal oscillator which conducts for a short period of time and is cut off (blocked) for a much longer period. A basic circuit for this type of oscillator is shown in Fig. 228.

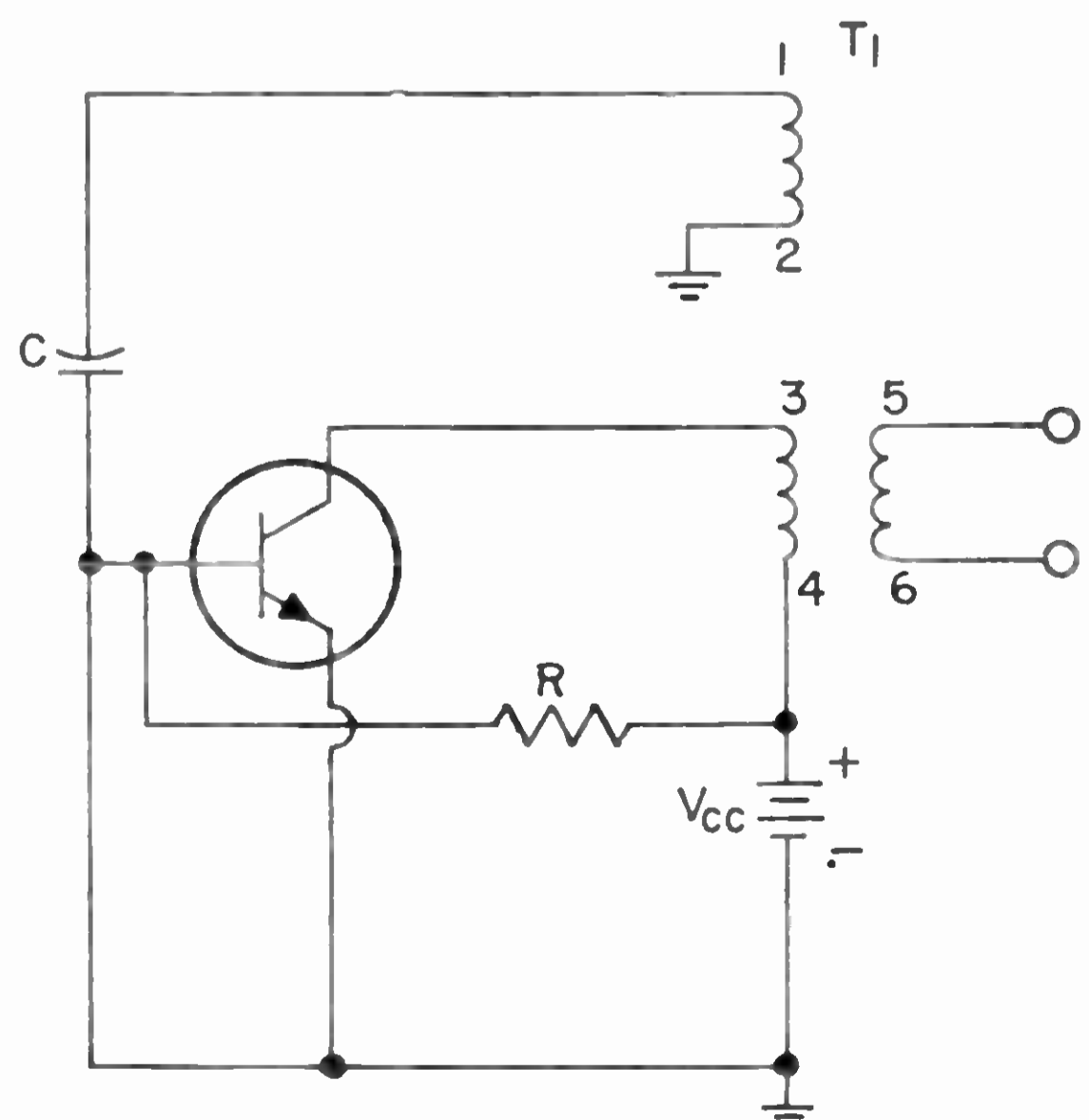


Fig. 228—Basic circuit of blocking oscillator.

Regenerative feedback through the tickler-coil winding 1-2 of transformer T_1 and capacitor C causes current through the transistor to rise rapidly until saturation is reached. The transistor is then cut off until C discharges through resistor R . The output waveform is a pulse, the width of which is primarily determined by winding 1-2. The time between pulses (resting or blocking time) is determined by the time constant of capacitor C and resistor R .

SWITCHING REGULATORS

Fig. 229 shows the basic configuration of a switching type of transistor voltage regulator. In this circuit, the pass transistor is connected in series with the load and is pulse-duration modulated by the signal supplied from the pulse generator or multivibrator. The ON time of the multivibrator is controlled by a dc comparison between a reference voltage and the output. The pulsed output from the series transistor is integrated by the low-pass filter. When the transistor is conducting, current is delivered to the load from the input source. In the OFF condition, the diode conducts and the energy stored in the reactive elements supplies current to the load. If the output voltage tends to decrease below the reference voltage, the duration of the ON-time pulse increases. The pass

transistor then conducts for a longer period of time so that the output voltage increases to the desired level. If the output voltage tends to rise above the reference voltage, the duration of the ON-time pulse decreases. The shorter conduction period of the pass transistor then results in a compensating decrease in output voltage.

When a step-down regulator is required (e.g., 100 volts down to 28 volts), the efficiency of a switching regulator is considerably higher than that of a conventional series regulator. If very precise regulation is required, the switching regulator can be used as a pre-regulator followed by a conventional regulator circuit; this configuration optimizes the advantages of both types of regulators. Over-all efficiency for such a combination circuit is typically about 80 to 85 per cent, as compared to values of 25 to 30 per cent for a conventional series-type step-down regulator. In addition, total power dissipation is reduced from several hundreds of watts to less than 50 watts.

Fig. 230 shows a switching regulator included in the design of a mercury-arc-lamp ballasting system. DC potential is applied to the V_{1S} terminals so that the transistor switch Q_1 (part of the switching regulator) is slightly forward-biased by a small current through R_s (approximately 3 milliamperes). Through positive feedback, Q_1 is immediately saturated by L_2 , which also powers the control circuit. Cur-

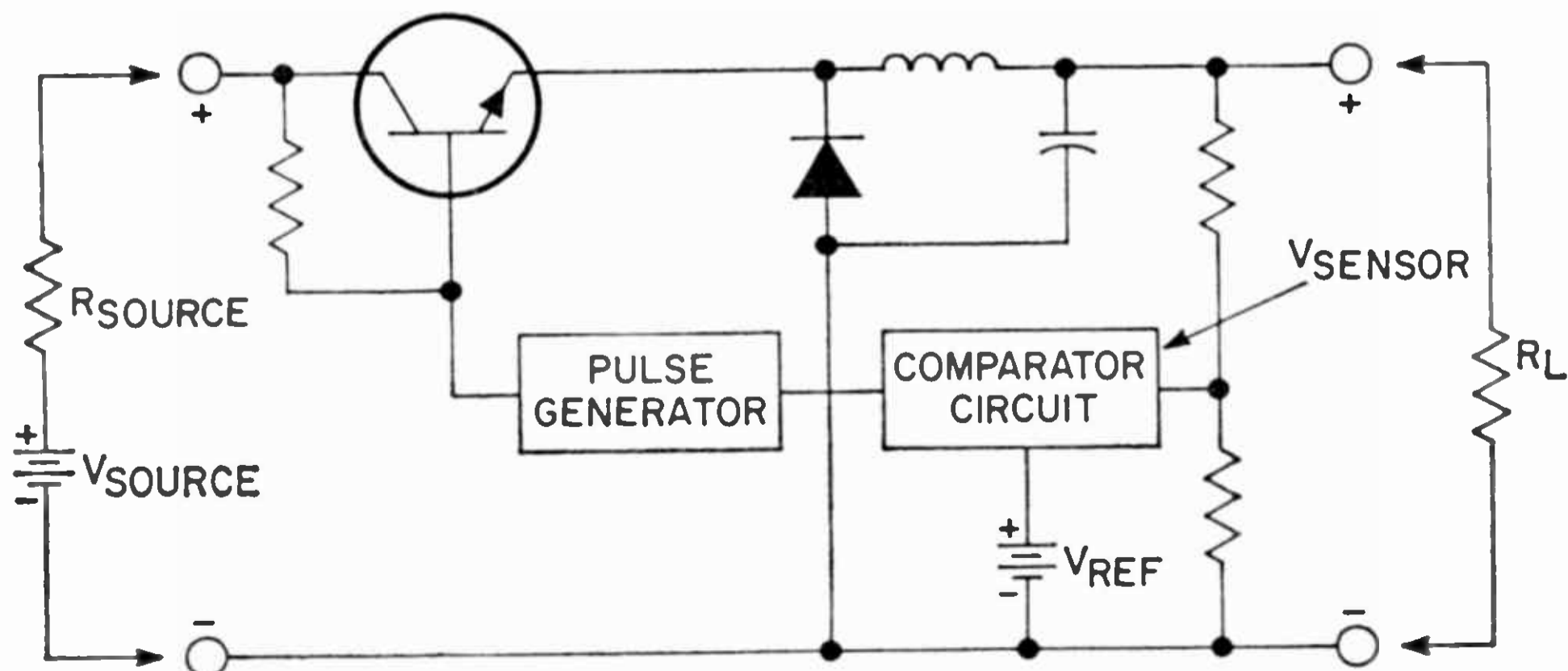


Fig. 229—Basic diagram of switching regulator.

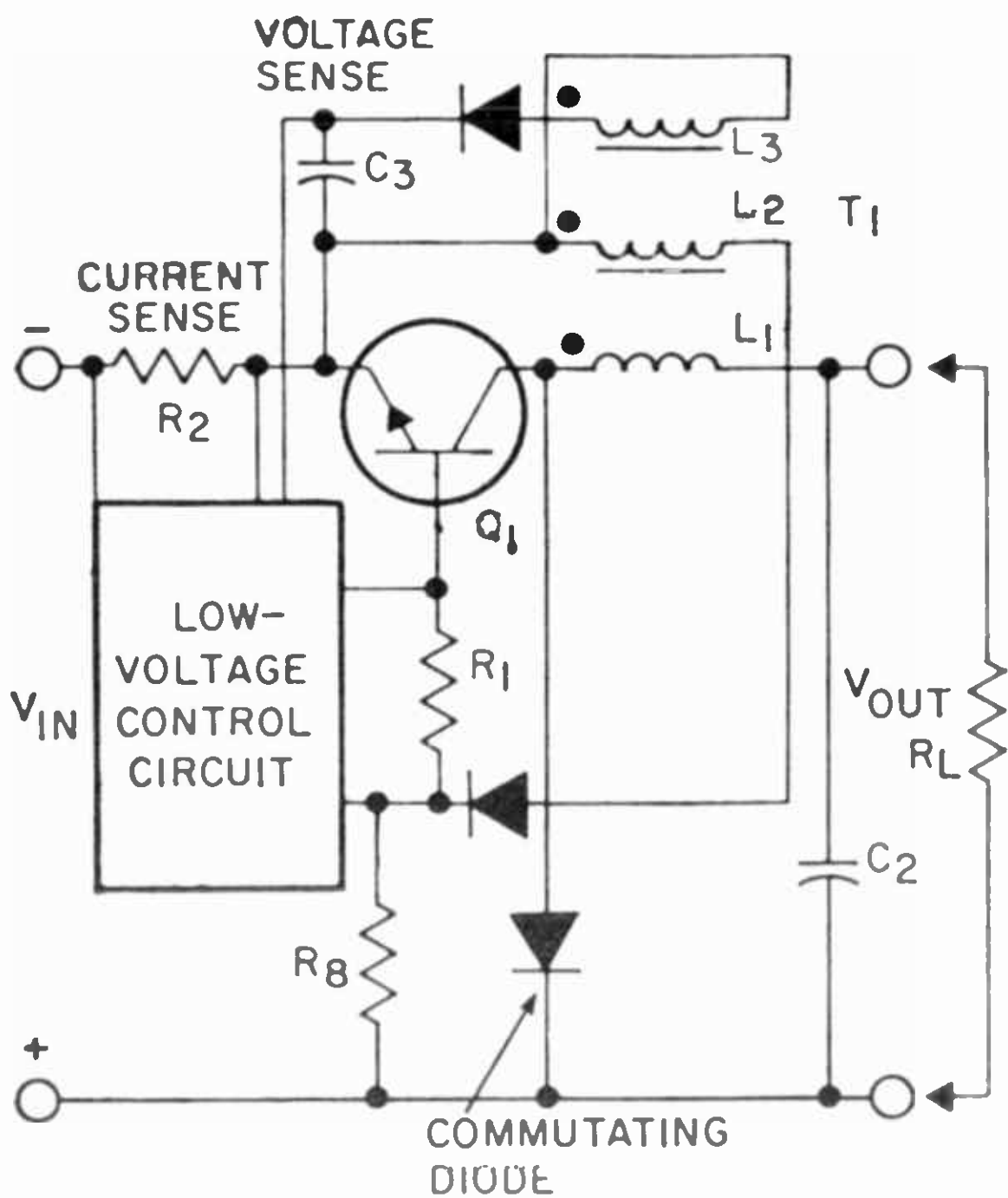


Fig. 230—Switching-regulator design for solid-state mercury-arc-lamp ballasting.

rent rises at a linear rate until the voltage across R_2 causes the control circuit to shunt the base-emitter junction of Q_1 . Q_1 is shut off and held off by L_2 until the current through L_1 is zero. The inductive kickback voltage is clamped by the commutating diode and, therefore, is the same as the output voltage on C_2 . L_3 charges C_3 to a voltage proportional to V_{OUT} . During the next cycle, the control circuit samples a combination of the voltage on C_3 and the current in R_2 . The output waveshapes for the circuit are shown in Fig. 231; performance data are shown in Fig. 232.

The unique feature of this circuit

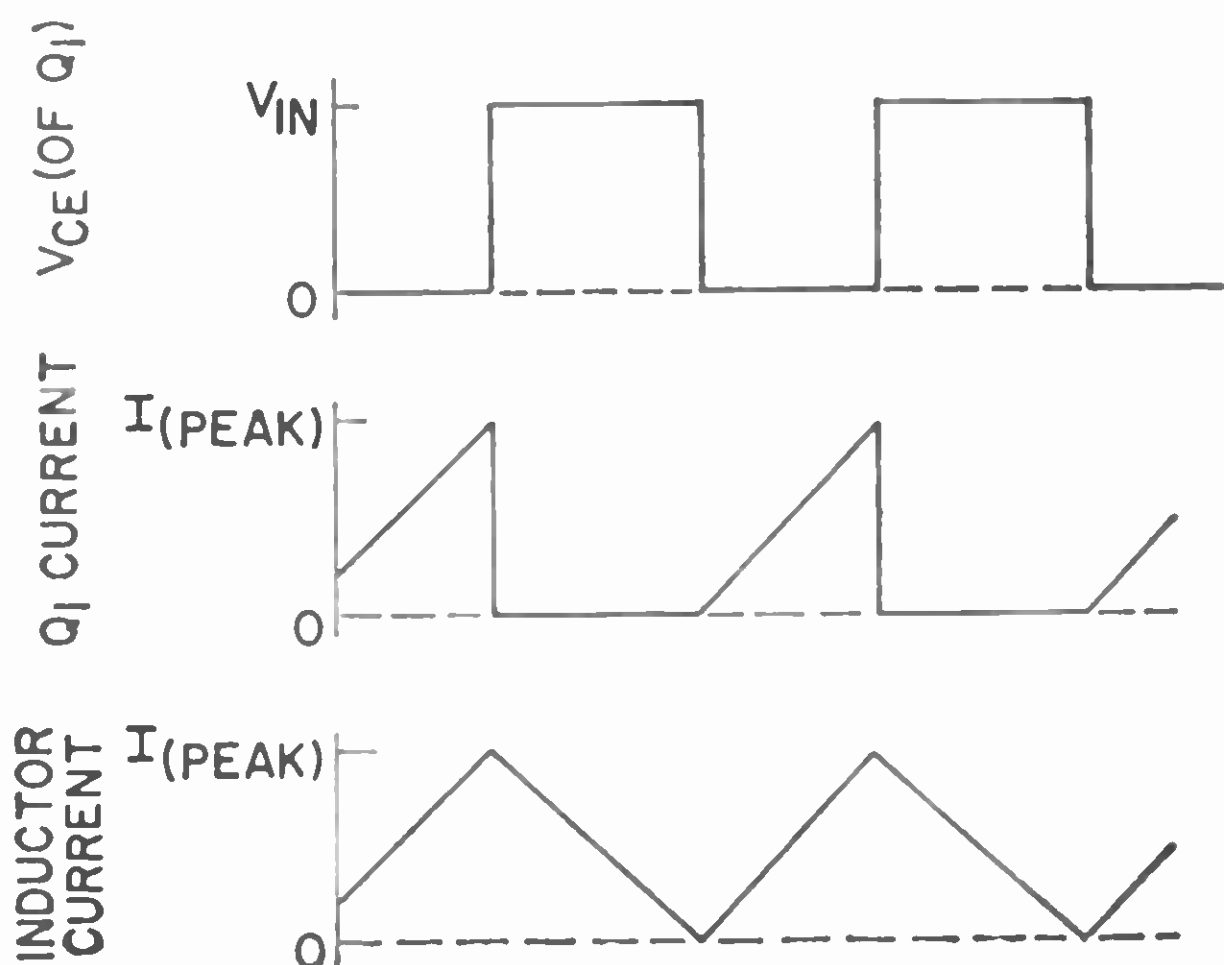


Fig. 231—Output waveshapes for circuit of Fig. 230.

is that only the high-current switching element Q_1 must meet the breakdown-voltage requirement imposed by the high input voltage; with this one exception, all of the control-circuit transistors are of the low-voltage, low-dissipation type. The circuit is able to withstand operation under short-circuit conditions.

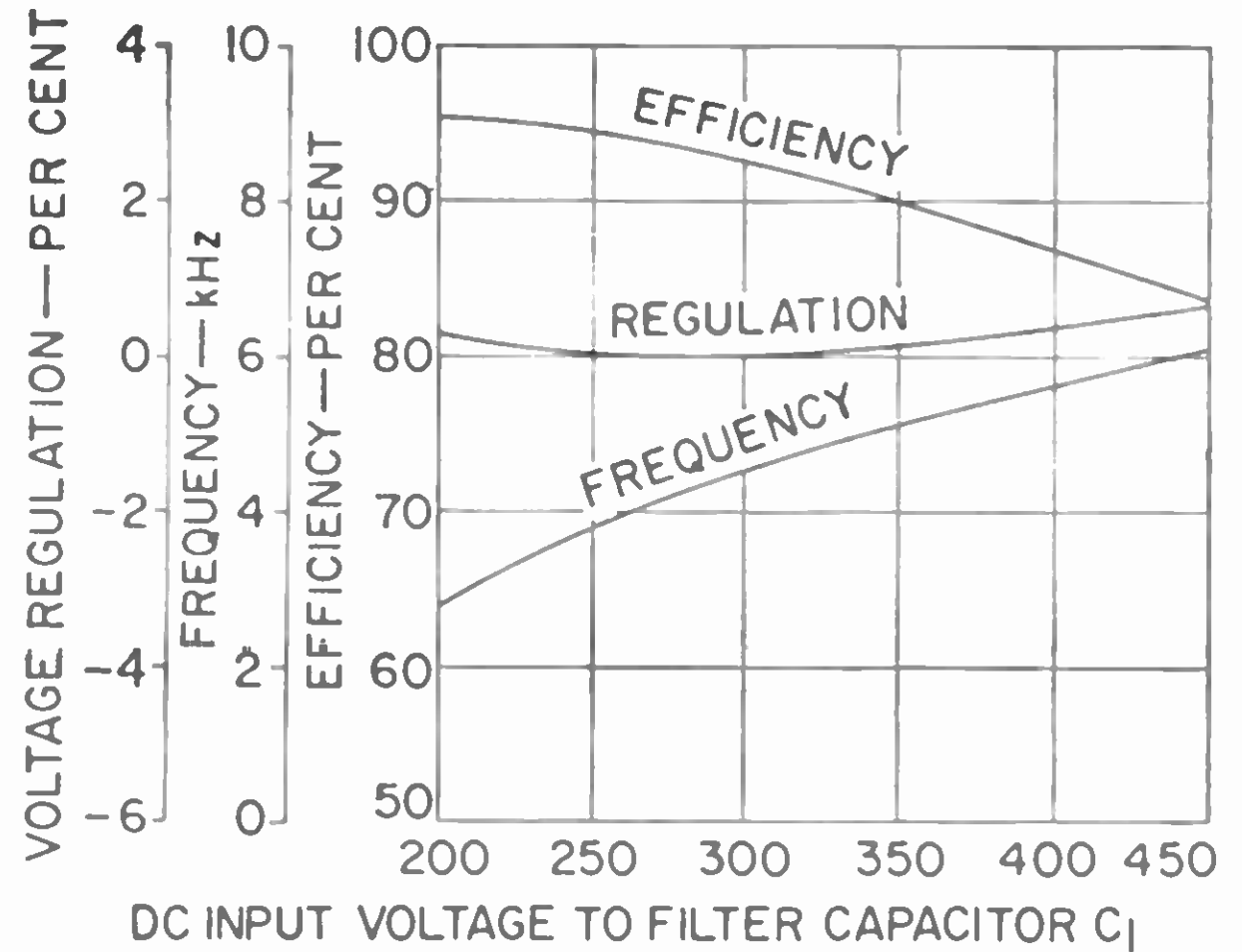


Fig. 232—Performance curves for circuit of Fig. 230.

A 175-watt switching-regulator ballast circuit utilizing the approach just described is shown in Fig. 233. For three-phase operation, no C_1 filter element is necessary provided that the dc input voltage to the switching regulator never drops below 200 volts. An input voltage drop below this level would extinguish the bulb.

Switching-regulator techniques are also utilized in motor-control systems. A servo motor control is shown in Fig. 234.

Switching-mode servo controls afford an efficient means for amplification of directional information. As an alternative to the use of cascaded linear stages to drive a class B push-pull output stage, this switching mode of control allows the active elements of the amplifier to operate in either saturation or cut-off. Because a relatively small length of time is spent in the active region of the devices, where power dissipation is high, the average power dissipation is lower. The efficiency of the over-all system, therefore, is higher. Switching servos are used in stable platforms for guidance and

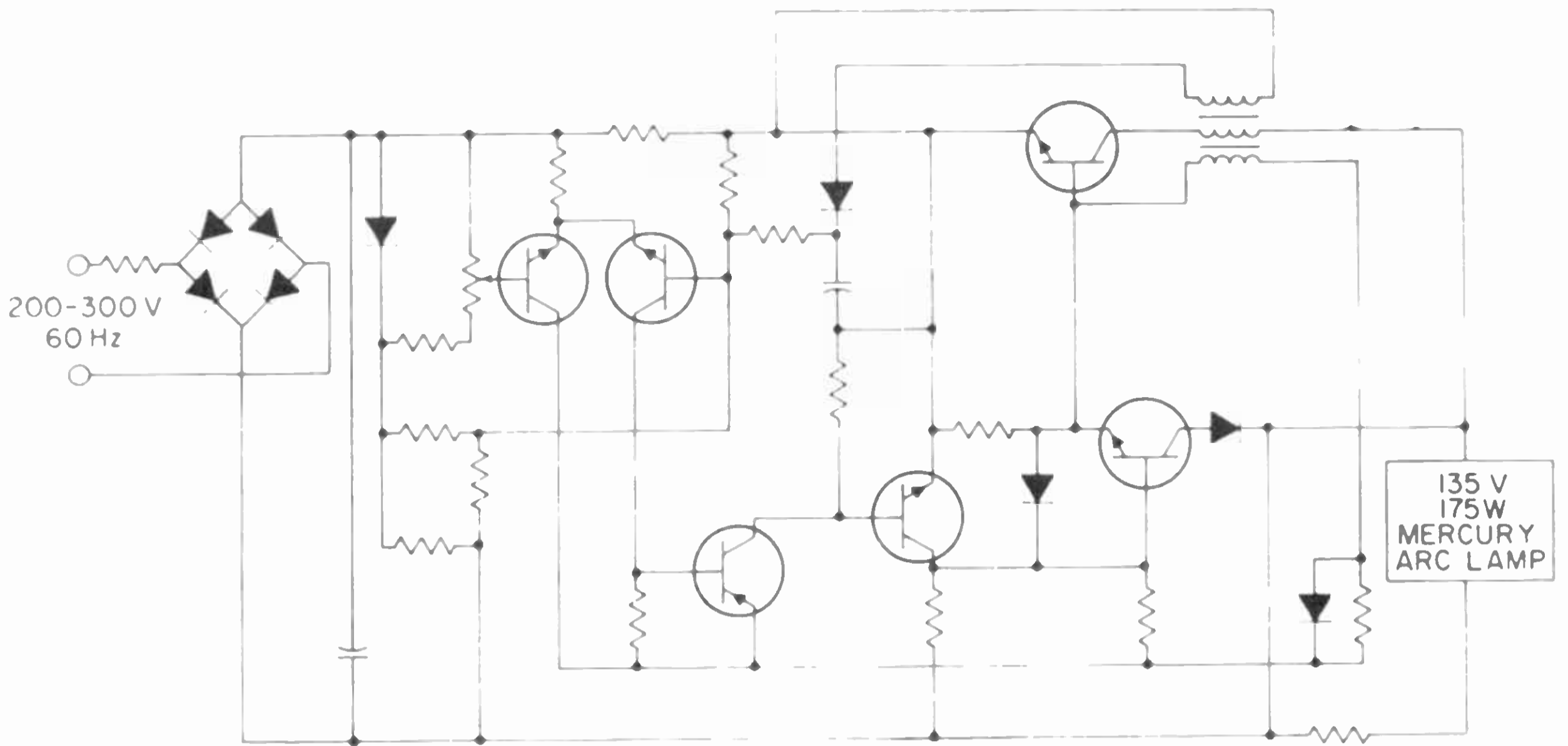


Fig. 233—175-watt switching-regulator ballast.

navigational systems, control of memory access devices in computer and data-processing systems, and other applications in which efficiency is a prime factor.

An ever-expanding application for switching systems is in the ac motor-control field. Sometimes this

application is necessary because the standby power is dc. More generally, however, high-speed inverters or switching circuits are used because the higher-frequency motors are more efficient and weigh less than their lower-frequency counterparts.

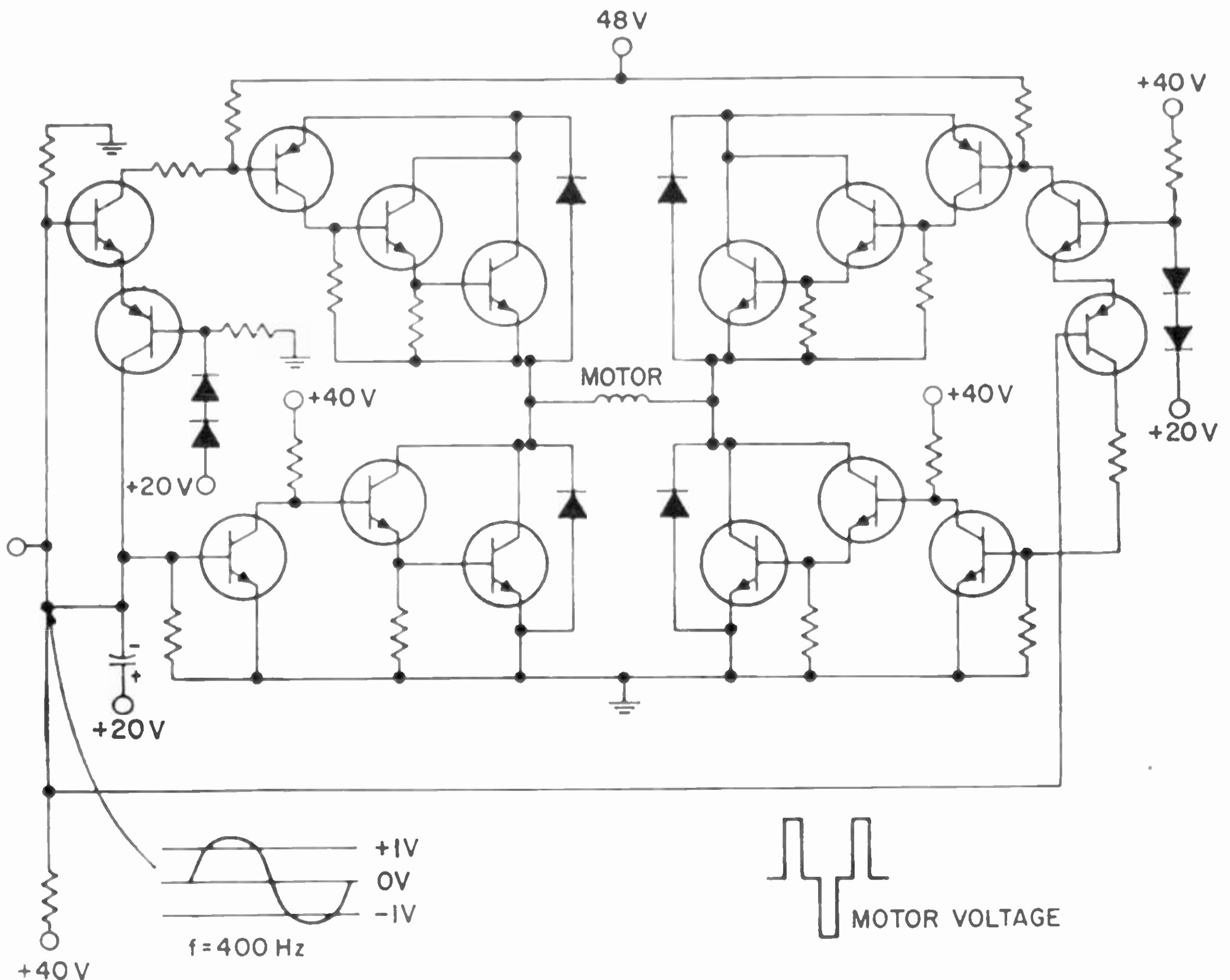


Fig. 234—Pulse-width-modulated servo-motor-driven output stage.

CONVERTERS AND INVERTERS

In many cases, the dc voltage required to operate electronic equipment is different from the available dc supply. The circuit used to convert direct current from one level to another is called a **converter**. Fig. 235 shows two simple converter circuits which can be used in place of the conventional vibrator-type converter in automobile radios. The switching drive to the two transistors is supplied by a separate, small, saturable transformer in the circuit of Fig. 235(a), and by an additional center-tapped drive winding on a single saturable transformer in Fig. 235(b). The characteristic hysteresis loop of the auto-transformer used in the circuit of Fig. 235(b) is shown in Fig. 236. Transformer parameters such as frequency, number of turns, and size and type of core material are determined by the operating requirements for the circuit. Once the transformer has been established, a change in supply voltage results in a change in the operating frequency.

Switching is accomplished as a result of the saturation of the trans-

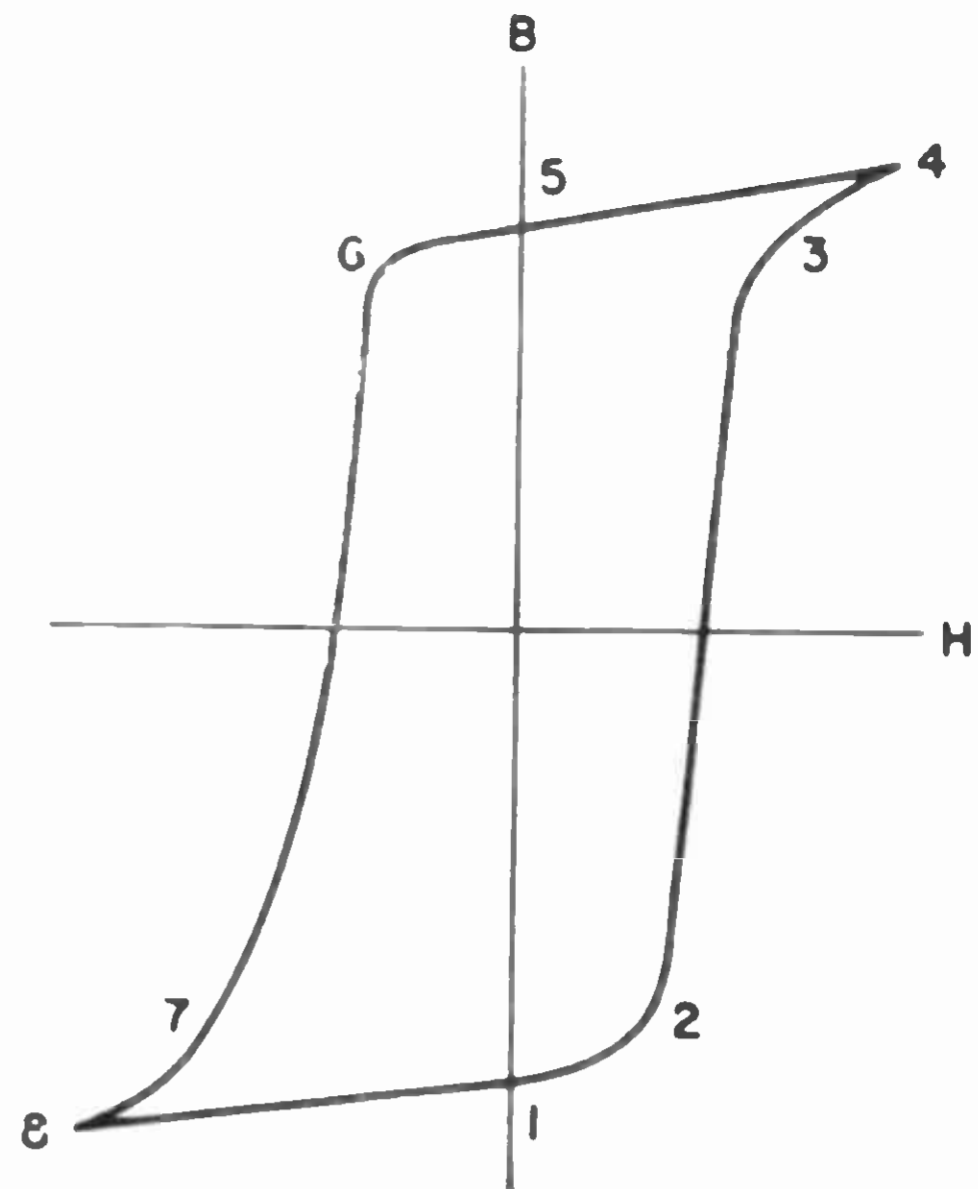


Fig. 236—Characteristic hysteresis loop of auto-transformer used in circuit of Fig. 235(b).

former. When the slope of the hysteresis loop shown in Fig. 236 is small, the magnetizing inductance is small and the magnetizing current increases rapidly. This situation exists as the loop is traversed in a counter-clockwise manner from point 1 to point 2. From point 2 to point 3, the magnetizing current increases very slowly because the magnetizing inductance is high. At point 3, the core is in saturation, and the

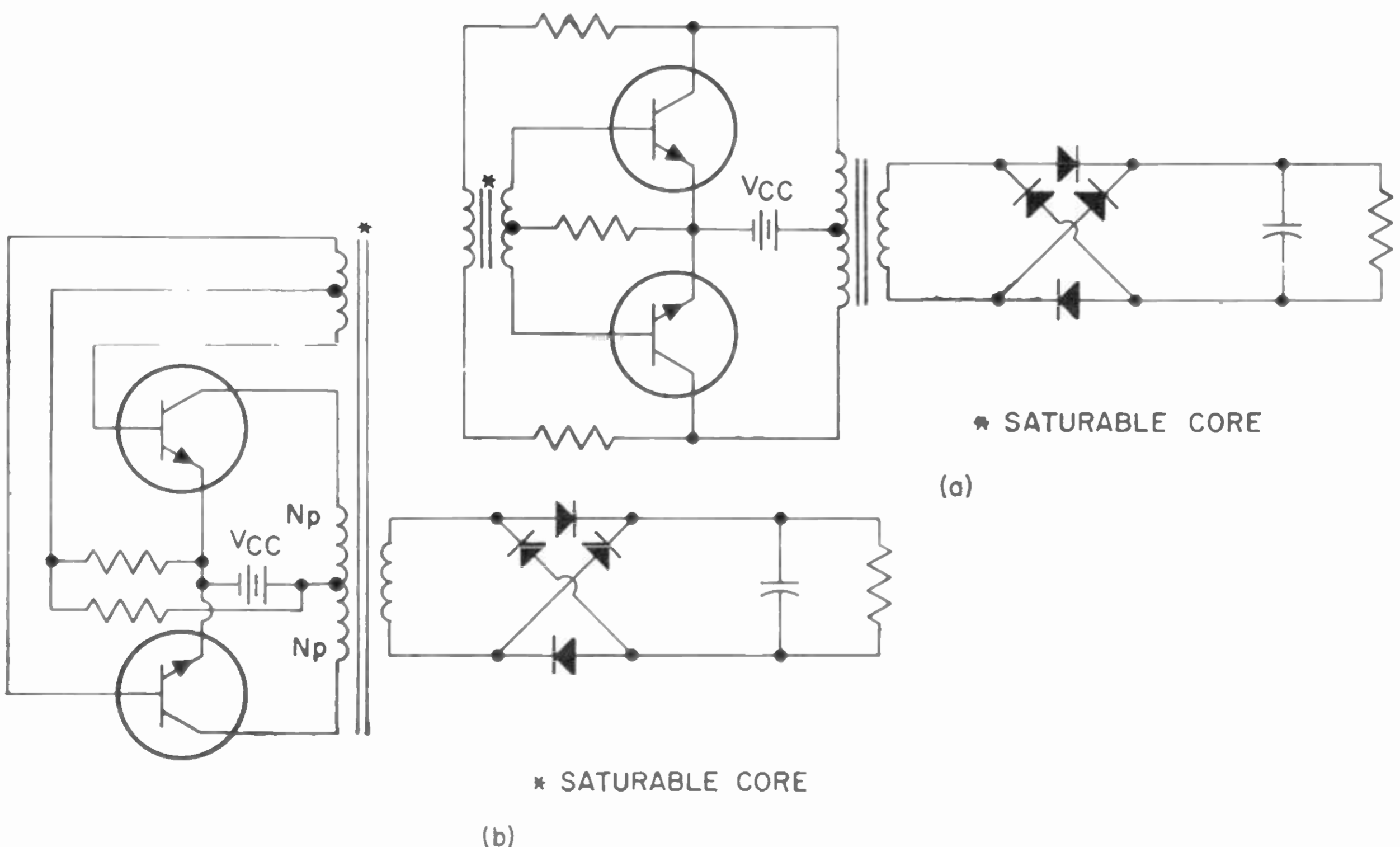


Fig. 235—Simple converter circuits that can be used in place of vibrator-type converters in automobile radios.

magnetizing current again increases rapidly. As the current continues to increase (between points 3 and 4), the ON transistor comes out of saturation. When point 4 has been reached, the voltages across the primary windings of the transformer have dropped to zero, and the battery voltage is applied across the collector-to-emitter terminals of each transistor. The magnetizing current then begins to decay, and voltages of opposite polarity are induced across the transformer. At point 5, the magnetizing current has been reduced to zero, the second transistor is in saturation, and the first transistor has twice the battery voltage across its emitter-to-collector junction. This sequence of events is repeated during each half-cycle of the operation of the circuit, except for a reversal of polarity.

The approximate load line of the converter circuit of Fig. 235(b) is shown in Fig. 237. Many of the important transistor ratings can be

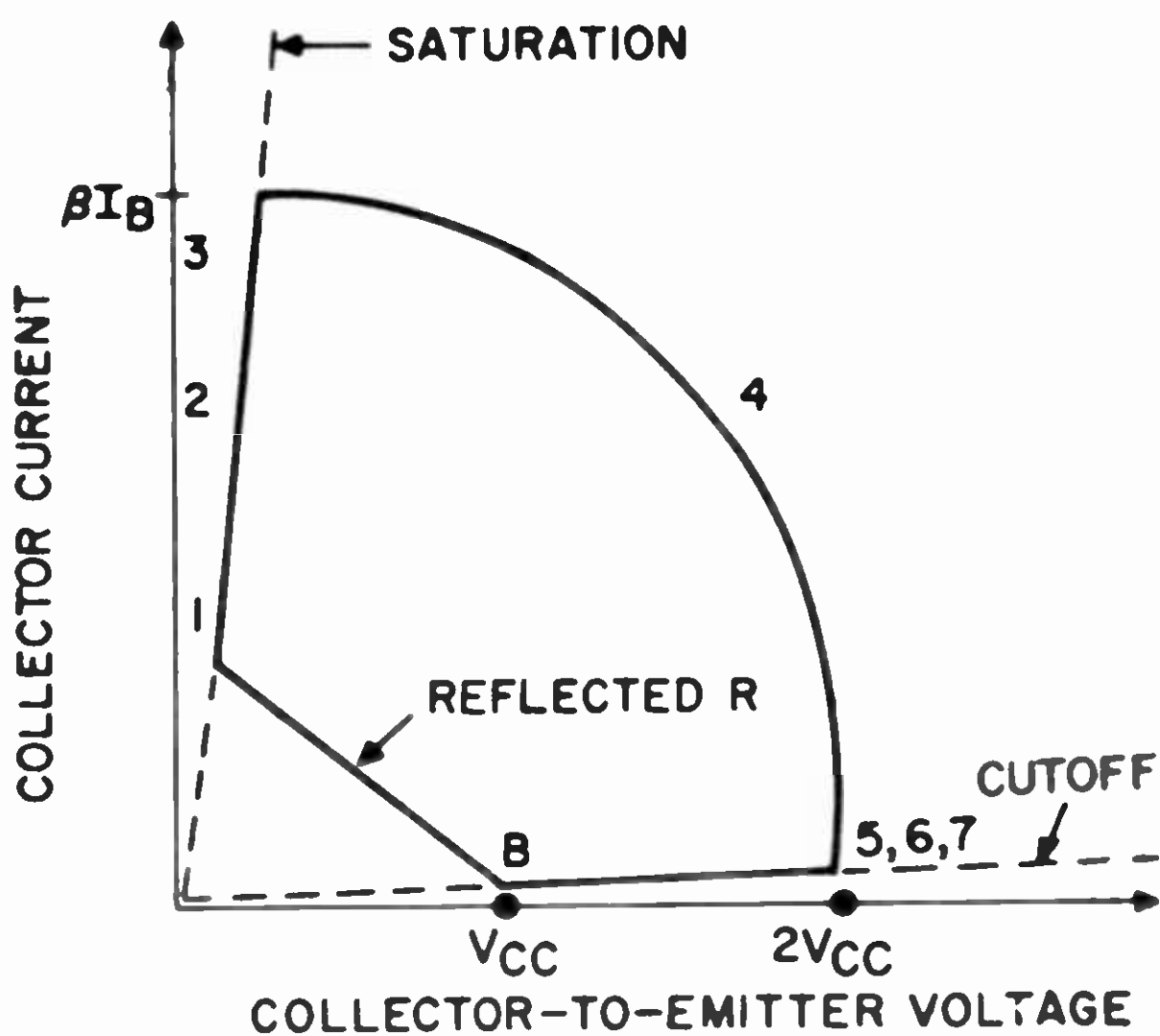


Fig. 237—Approximate load line for converter circuit shown in Fig. 235(b).

determined from this curve. For example, the collector-to-emitter sustaining voltage under reverse-bias conditions, $V_{CEV(sus)}$, is given by

$$V_{CEV(sus)} \geq 2V_{CC} + \Delta V_{CC}$$

where V_{CC} is the collector-supply voltage and ΔV_{CC} is the magnitude of the supply variations or "spikes." The second-breakdown voltage limit $E_{S/B}$ for the transistor is given by

$$E_{S/B} \geq \frac{1}{2} (\beta I_B)^2 L_1$$

where β is the common-emitter forward-current transfer ratio, I_B is the base current, and L_1 is the total series inductance of the transformer and the load reflected to the input. As mentioned previously, the collector-to-emitter saturation voltage $V_{CE(sat)}$ of the transistor should be low.

Fig. 238 shows the basic circuit configuration for a ringing-choke dc-to-dc converter. In this converter,

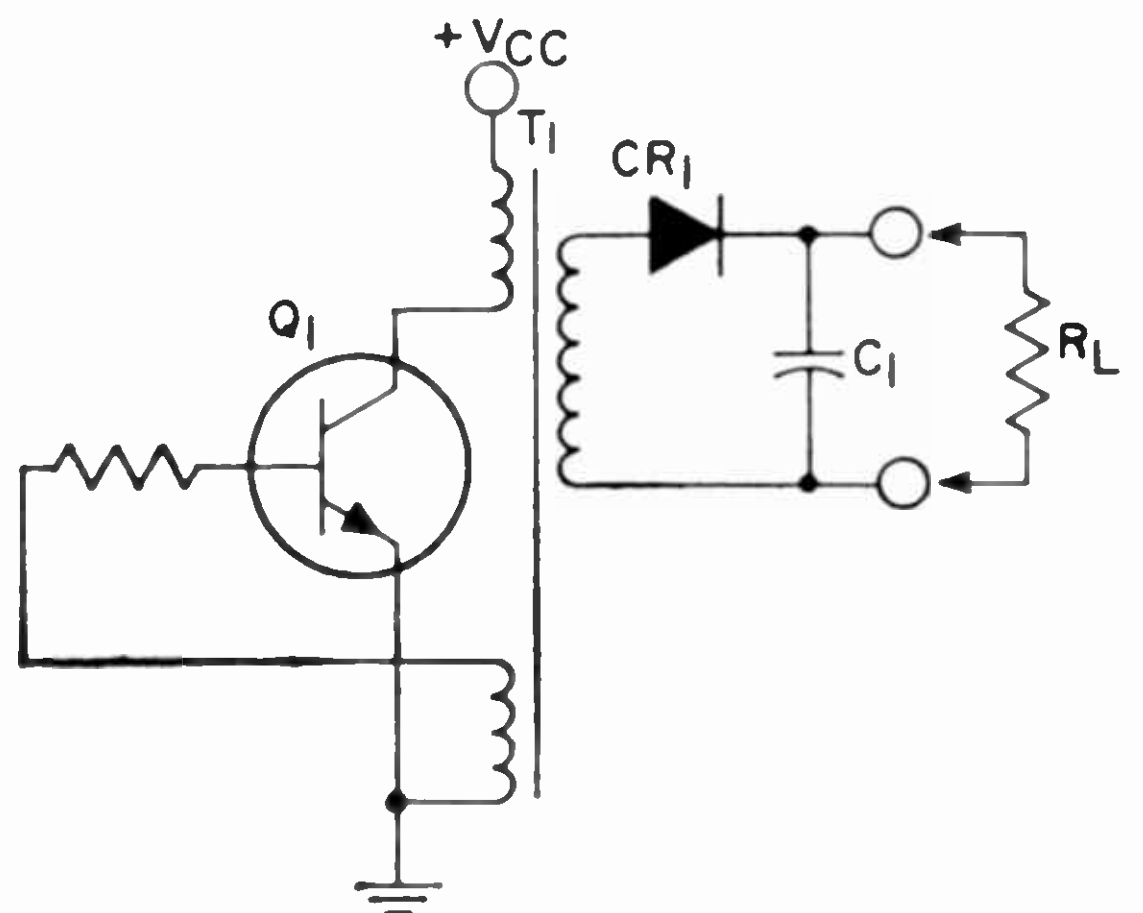


Fig. 238—Basic circuit configuration of a ringing-choke dc-to-dc converter.

a blocking oscillator (chopper circuit) is transformed-coupled to a half-wave-rectifier type of output circuit. The rectifier converts the pulsating oscillator output into a fixed-value dc output voltage.

When the oscillator transistor Q_1 conducts (as a result of either a forward bias or external drive), energy is transferred to the collector inductance presented by the primary winding of transformer T_1 . The voltage induced across the transformer feedback winding connected to the transistor base through resistor R_B increases the conduction of Q_1 until the transistor is driven into saturation. The rectifier diode CR_1 in series with the secondary winding of transformer T_1 is oriented so that no power is delivered to the load circuit during this portion of the oscillator cycle.

With transistor Q_1 in saturation, the collector current through the primary inductance of transformer T_1

risers linearly with time ($-di/dt = E/L$) until the base drive supplied by the transformer feedback winding can no longer maintain Q_1 in saturation. As the current through Q_1 decreases from the saturation level, the voltage induced into the feedback winding decreases, and transistor Q_1 is rapidly driven beyond cutoff. The energy stored in the collector inductance (primary of transformer T_1) is released by the collapsing magnetic field and coupled by the secondary winding of transformer T_1 , through rectifier diode CR_1 , to the load resistance R_L and filter capacitor C_1 . The filter capacitor stores the energy it receives from the collector inductance. When no current is supplied to the load circuit from the oscillator (i.e., during conduction of transistor Q_1), capacitor C_1 supplies current to the load resistance R_L to maintain the output voltage at a relatively constant value. The switching action of rectifier diode CR_1 prevents any decrease of the energy stored by capacitor C_1 because of the negative pulse coupled from the oscillator during the periods that transistor Q_1 conducts.

The operating efficiency of the ringing-choke inverter is low, and the circuit, therefore, is used primarily in low-power applications. In addition, because power is delivered to the output circuit for only a small fraction of the oscillator cycle (i.e., when Q_1 is not conducting), the circuit has a relatively high ripple factor which substantially increases output filtering requirements. This converter, however, provides definite advantages to the system designer in terms of design simplicity and compactness.

In a converter the change in frequency of operation with supply voltage is not usually important because the output voltage is rectified and filtered. In an inverter circuit, however, the frequency may be very important and is generally controlled by adjustment of the supply voltage. Typically, the dc supply voltage

is controlled by means of a voltage regulator inserted ahead of the converter to stabilize the input voltage and a power amplifier following the converter to isolate the converter from the effects of a varying load.

Inverters may be used to drive any equipment which requires an ac supply, such as motors, ac radios, television receivers, or fluorescent lighting. In addition, an inverter can be used to drive electromechanical transducers in ultrasonic equipment, such as ultrasonic cleaners and sonar detection devices.

High-current tunnel diodes are used as low-voltage inverters in circuits having low-impedance dc power sources. They can also be used for efficient inversion of the output of solar cells, thermoelectric generators, or thermionic converters, and as overload detectors in dc and ac power supplies, pulse generators, high-speed switches, and oscillators.

Fig. 239 shows a block diagram

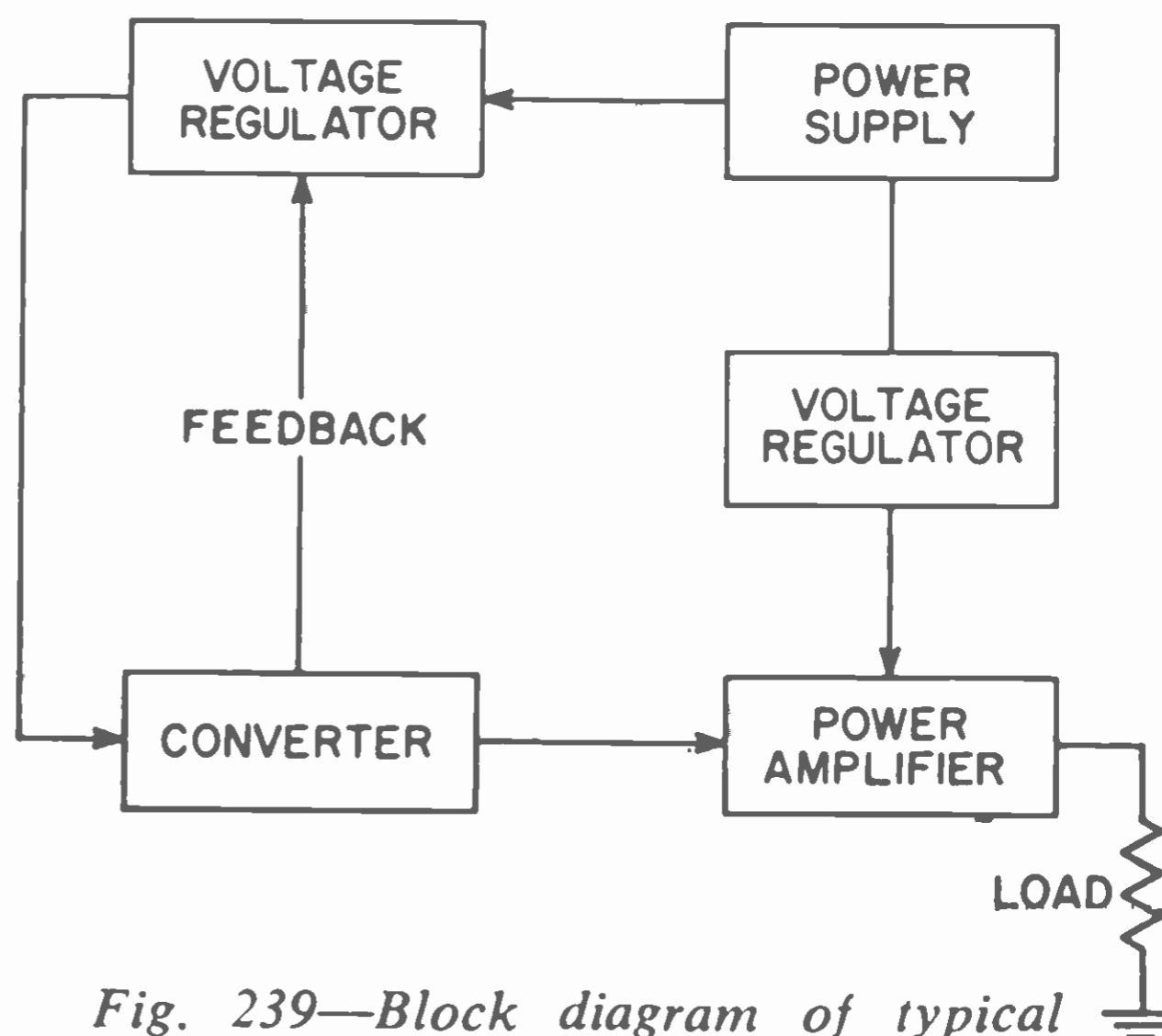


Fig. 239—Block diagram of typical inverter circuit.

of a typical inverter circuit. The output frequency is directly dependent on the induced voltage of the converter transformer. The feedback shown samples this induced voltage and adjusts the output of the voltage regulator to maintain a constant induced voltage in the converter and thus a constant output frequency. If a regulated output voltage is not required, the second voltage regulator is omitted.

Fig. 240 shows a simple complementary inverter circuit using p-channel and n-channel MOS transistors. When the input voltage to the circuit is zero, the n-channel unit is cut off and the p-channel unit is forward-biased by V volts. The

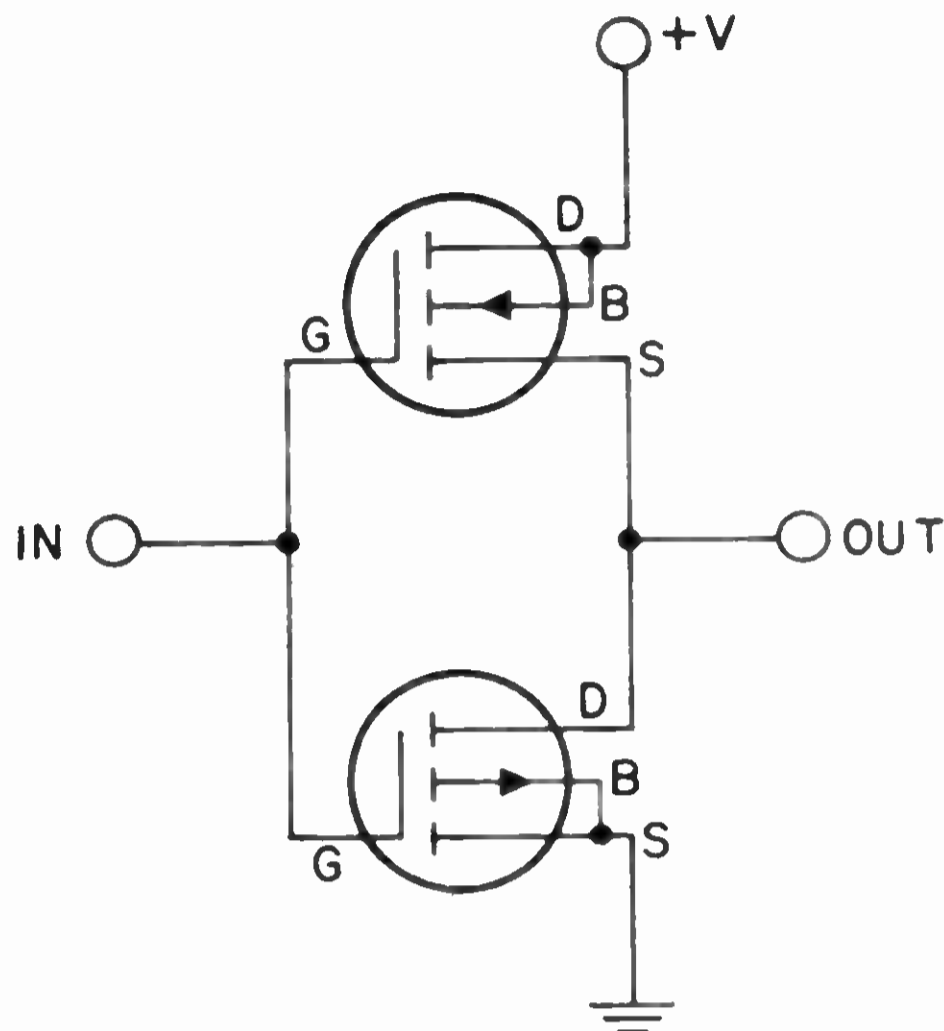


Fig. 240—Complementary inverter circuit using MOS transistors.

p-channel unit is capable of supplying several milliamperes of current. The n-channel unit, however, will draw only its channel leakage current, which is typically a few microamperes. Because the load for the circuit is assumed to be other MOS gates, which have a high input impedance and require negligible driving current, there is no dc load current under these conditions.

When the input voltage is V volts, however, the situation is reversed; the p-channel unit is cut off and the n-channel unit is forward-biased by V volts. The n-channel unit is then capable of drawing a current of several milliamperes. However, because the only source available is the leakage current of the p-channel unit, the current drawn by the n-channel unit is still negligible. In either of its stable states, therefore, the inverter draws only a leakage current from the supply. On any transition, however, the circuit can provide a current of several milliamperes to charge or discharge capacitive loads such as those presented by MOS gates and wiring. Fig. 241 shows in graphical form the operation of the inverter circuit in its two dc states.

The push-pull switching inverter is probably the most widely used type of power-conversion circuit. For inverter applications, the circuit provides a square-wave ac output. When the inverter is used to provide dc-to-dc conversion, the square-wave voltage is usually applied to a full-wave bridge rectifier and filter.

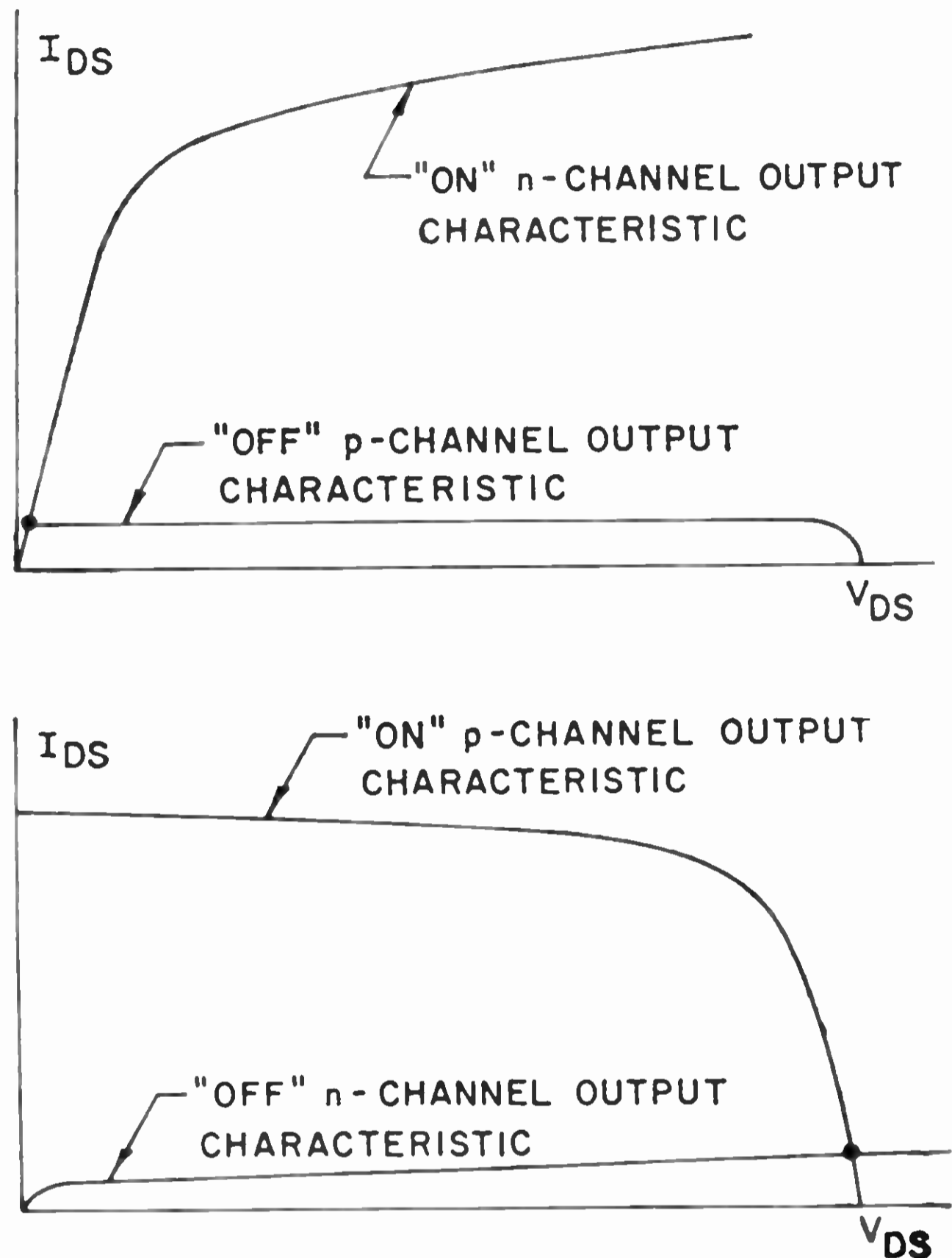


Fig. 241—Characteristics of inverter circuit of Fig. 240 in its two stable states.

Fig. 242 shows the configuration of the push-pull switching inverter. The single saturable transformer controls circuit switching and provides the desired voltage transformation for the square-wave output delivered to the bridge rectifier. The rectifier and filter convert the square-wave voltage in a smooth, fixed-amplitude dc output voltage.

When the voltage V_{CC} is applied to the converter circuit, current tends to flow through both switching transistors Q_1 and Q_2 . It is very unlikely, however, that a perfect balance can be achieved between corresponding active and passive components of the two transistor sections; therefore, the initial flow of current through one

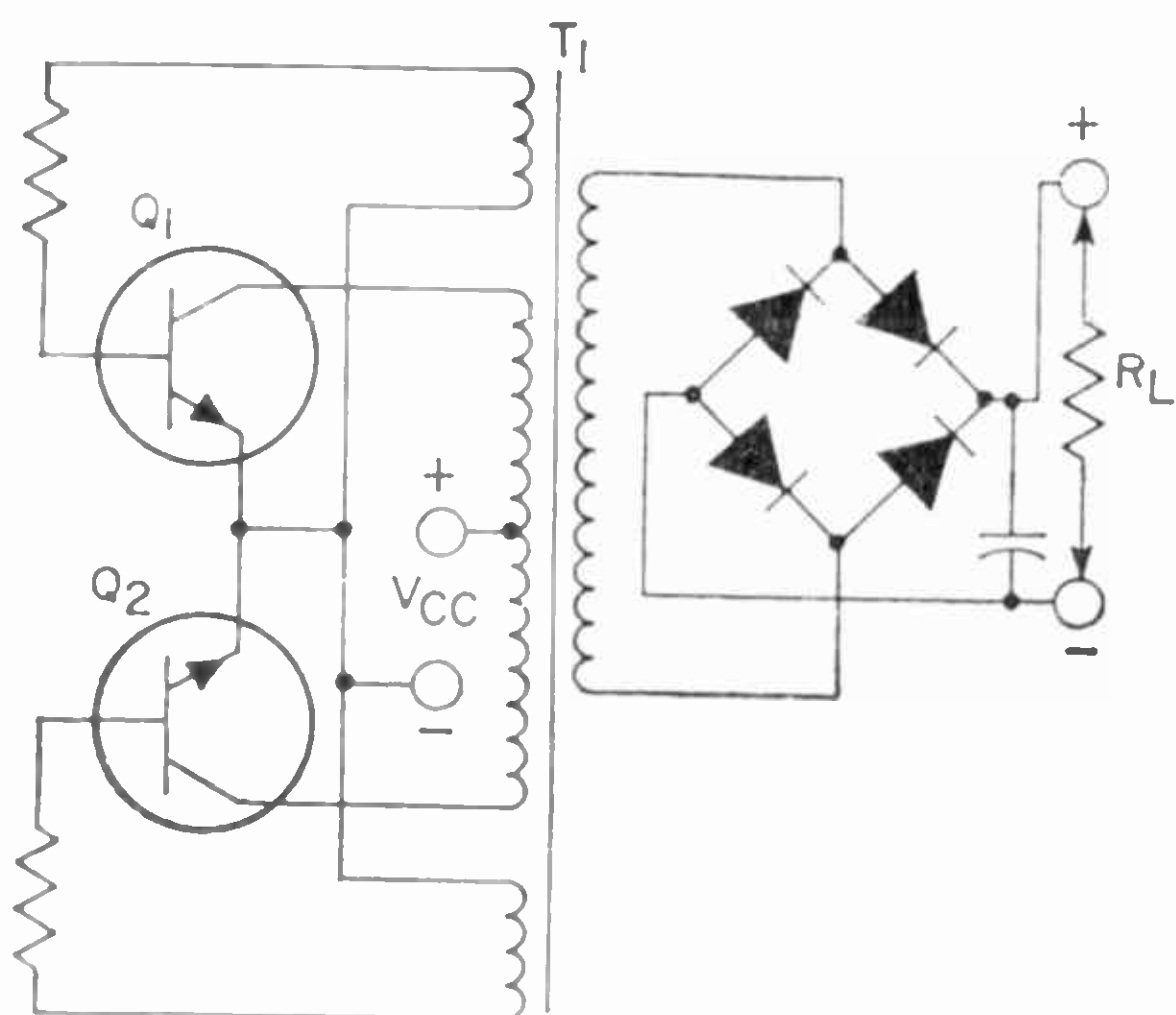


Fig. 242—Basic circuit configuration of a single-transformer push-pull switching converter.

of the transistors is slightly larger than that through the other transistor. If transistor Q_1 is assumed to conduct more heavily initially, the rise in current through its collector inductance causes a voltage to be induced in the feedback windings of transformer T_1 which supply the base drive to transistors Q_1 and Q_2 . The base-drive voltages are in the proper polarity to increase the current through Q_1 and to decrease the current through Q_2 . As a result of regenerative action, the condition of Q_1 is rapidly increased, and Q_2 is quickly driven to cutoff.

The increased current through Q_1 causes the core of the collector inductance to saturate. The inductance no longer impedes the rise in current, and the transistor current increases sharply into the saturation region. For this condition, the magnetic field about the collector inductance is constant, and no voltage is induced in the feedback windings of transformer T_1 . With the cutoff base voltage removed, current is allowed to flow through transistor Q_2 . The increase in current through the collector inductance of this transistor causes voltages to be induced in the feedback windings in the polarity that increases the current through Q_2 and decreases the current through Q_1 . This effect is aided by the collapsing magnetic field about the collector inductance of Q_1 that results from the decrease

in current through this transistor. The feedback voltages produced by this collapsing field quickly drive Q_1 beyond cutoff and further increase the conduction of Q_2 until the core of the collector inductance for this transistor saturates to initiate a new cycle of operation. The square wave of voltage produced by the switching action of transistors Q_1 and Q_2 is coupled by transformer T_1 to the bridge rectifier and filter, which develop a smooth, constant-amplitude dc voltage across the load resistance R_L . The small ripple produced by the square wave greatly simplifies filter requirements.

Push-pull transformer-coupled converters with full-wave rectification provide power to the load continuously and are, therefore, well suited for low-impedance, high-power applications. Although not as economical as the ringing-choke design, the push-pull configuration provides higher efficiency and improved regulation.

In high-power driven inverters, it is not uncommon to use a Darlington connection to increase the current gain. However, this configuration increases the V_{CE} saturation of the output and does not permit a fast turn-off. The circuit shown in Fig. 243 uses two small additional windings and eliminates both problems.

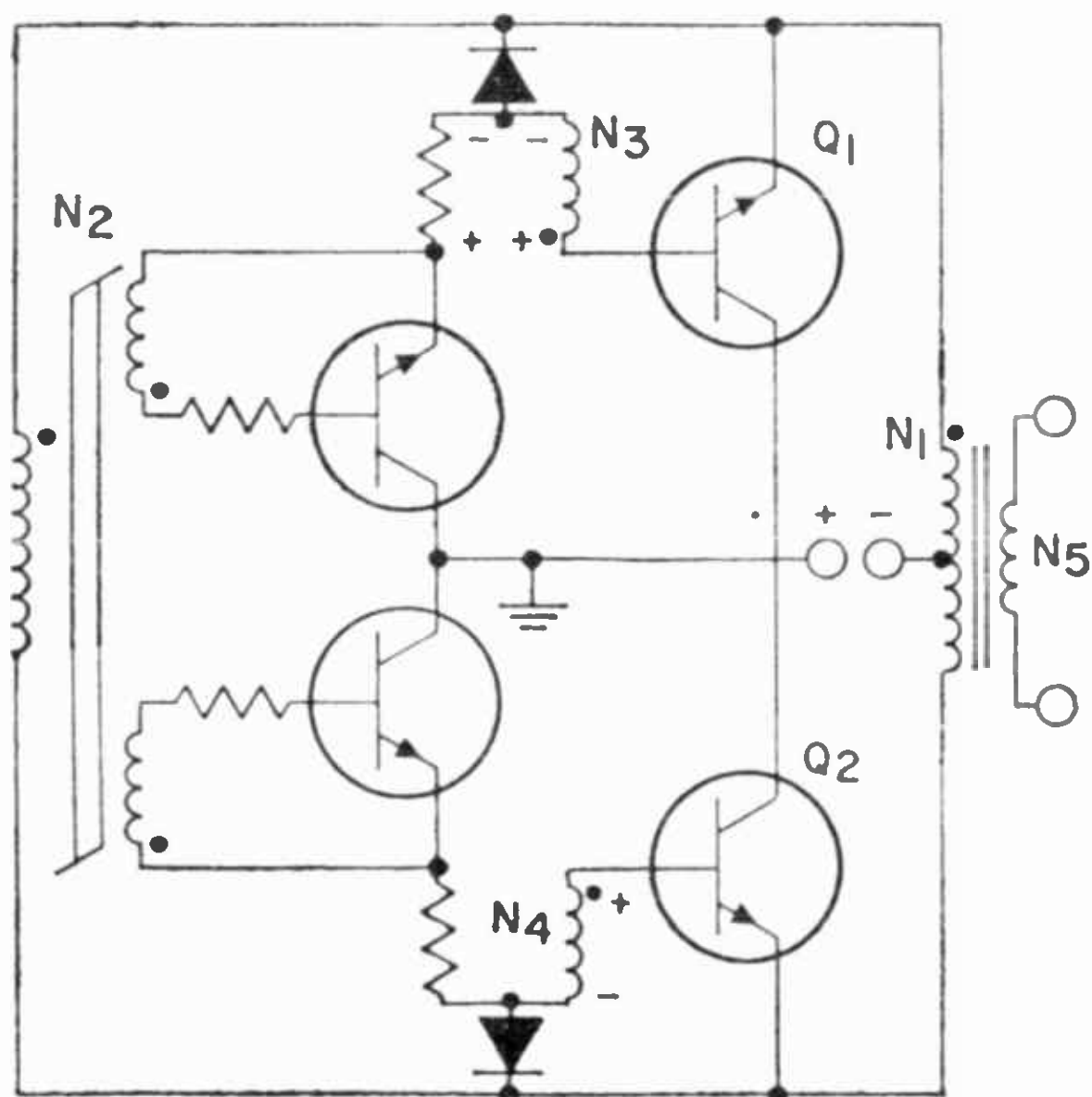


Fig. 243—Boosted Darlington inverter with turn-off drive.

The polarity of N_3 and N_4 is shown for Q_1 ON and Q_2 OFF. N_3 and N_4 are wound on core No. 1 which could be a motor or other magnetic structure. The voltage developed across N_3 allows Q_1 to saturate fully while the voltage across N_4 allows Q_2 to have a reverse bias applied, thus helping the device to turn off. The diodes provide a path for reverse bias when the transistor turns off and blocks voltage while the transistor is on; thus, they allow the driver transistors to control the output units.

Three-phase bridge inverters for induction motors are usually used to convert dc, 60-Hz, or 400-Hz input to a much higher frequency, possibly as high as 10 kHz. Increasing frequency reduces the motor size and increases the horsepower-to-weight ratio, desirable features in military, aviation, and portable industrial power-tool markets. Fig. 244 shows a typical three-phase bridge circuit with gate signals and transformer primary currents.

Fig. 245 shows the schematic diagram of a two-transistor, two-transformer inverter circuit. A saturable base-drive transformer T_2 controls the inverter switching operation. A linearly operating output transformer T_1 transfers the output power to the load. The output transformer T_1 is not allowed to saturate; therefore, the peak collector current through the transistor is determined principally by the value of the load impedance.

Because no two transistors are perfectly matched, one of the transistors in the inverter circuit conducts more rapidly than the other when the power is turned on. This transistor, Q_2 for example, tends toward saturation and causes positive voltages to appear at the dotted ends of the transformers. Thus, there is an effective positive feedback that causes Q_1 to switch off and Q_2 to switch on. The voltage from the collector of Q_1 to the collector of Q_2 is then positive and equal to twice the collector supply

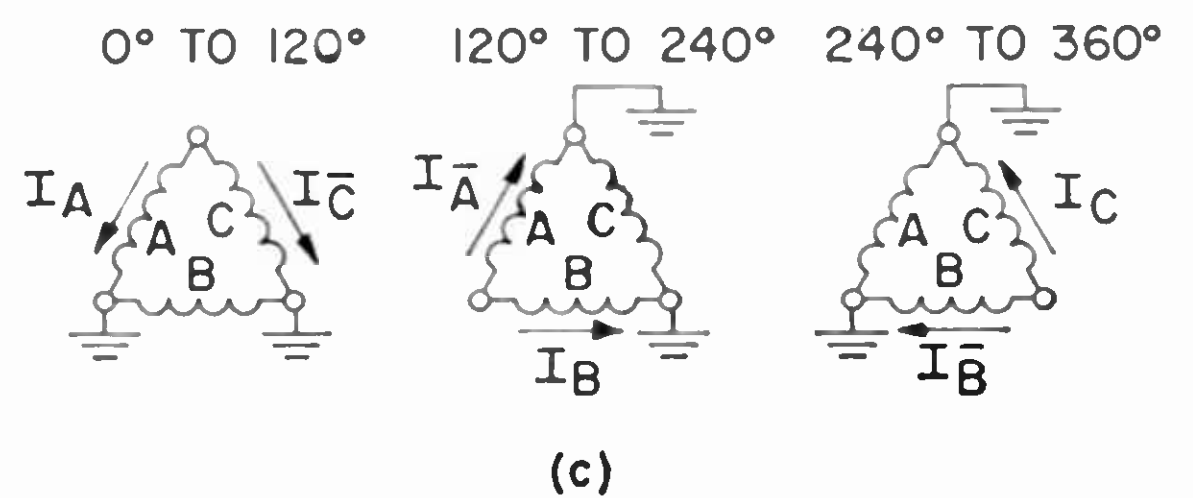
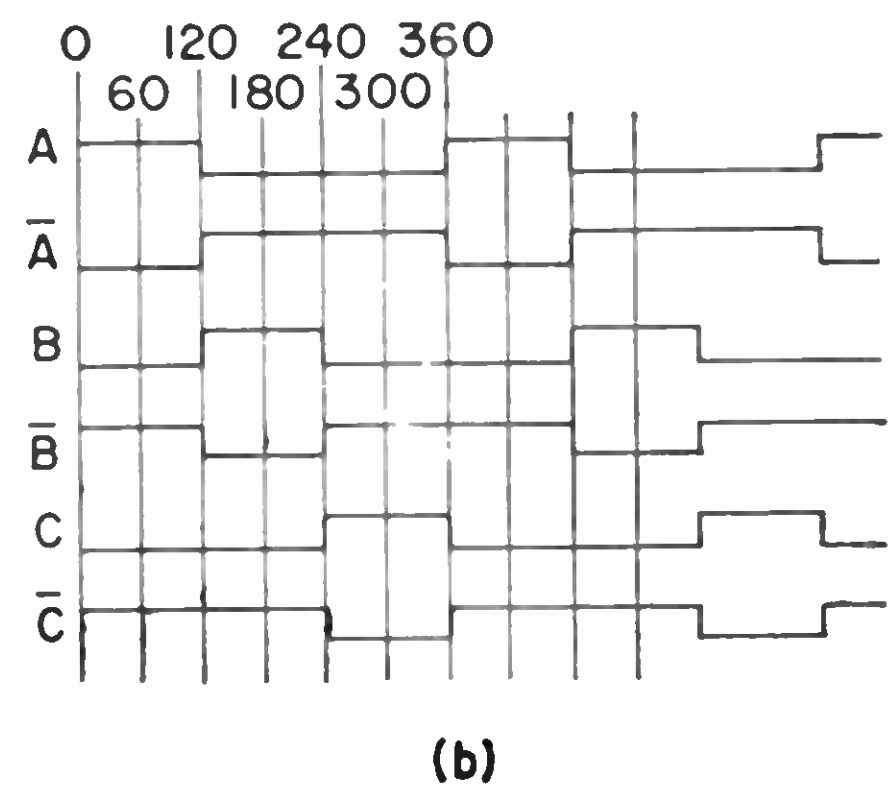
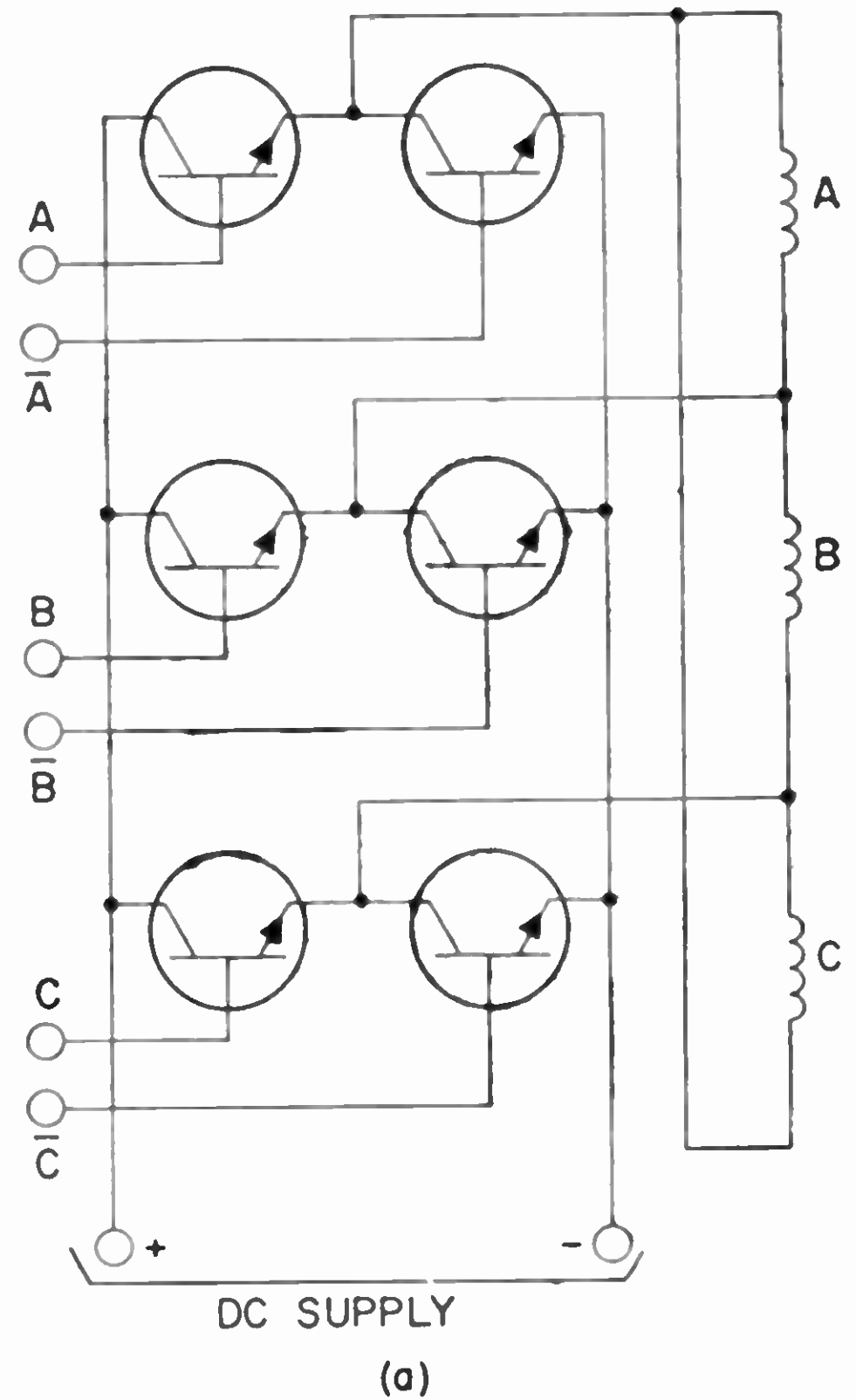


Fig. 244—Three-phase bridge inverter: (a) circuit configuration; (b) gate driving signals; (c) transformer primary current switching.

voltage V_{CC} . The voltage $V_{R_{fb}}$ across the feedback resistor R_{fb} is essentially the product of the resistance R_{fb} and the base current referred to the primary of T_2 . The voltage across T_2 is equal to $2 V_{CC} - V_{R_{fb}}$. At the beginning of the next half-

cycle, the voltage across R_{fb} increases very slowly with the slowly increasing magnetizing current through T_2 . When T_2 reaches its saturation flux density, the magnetizing current increases very

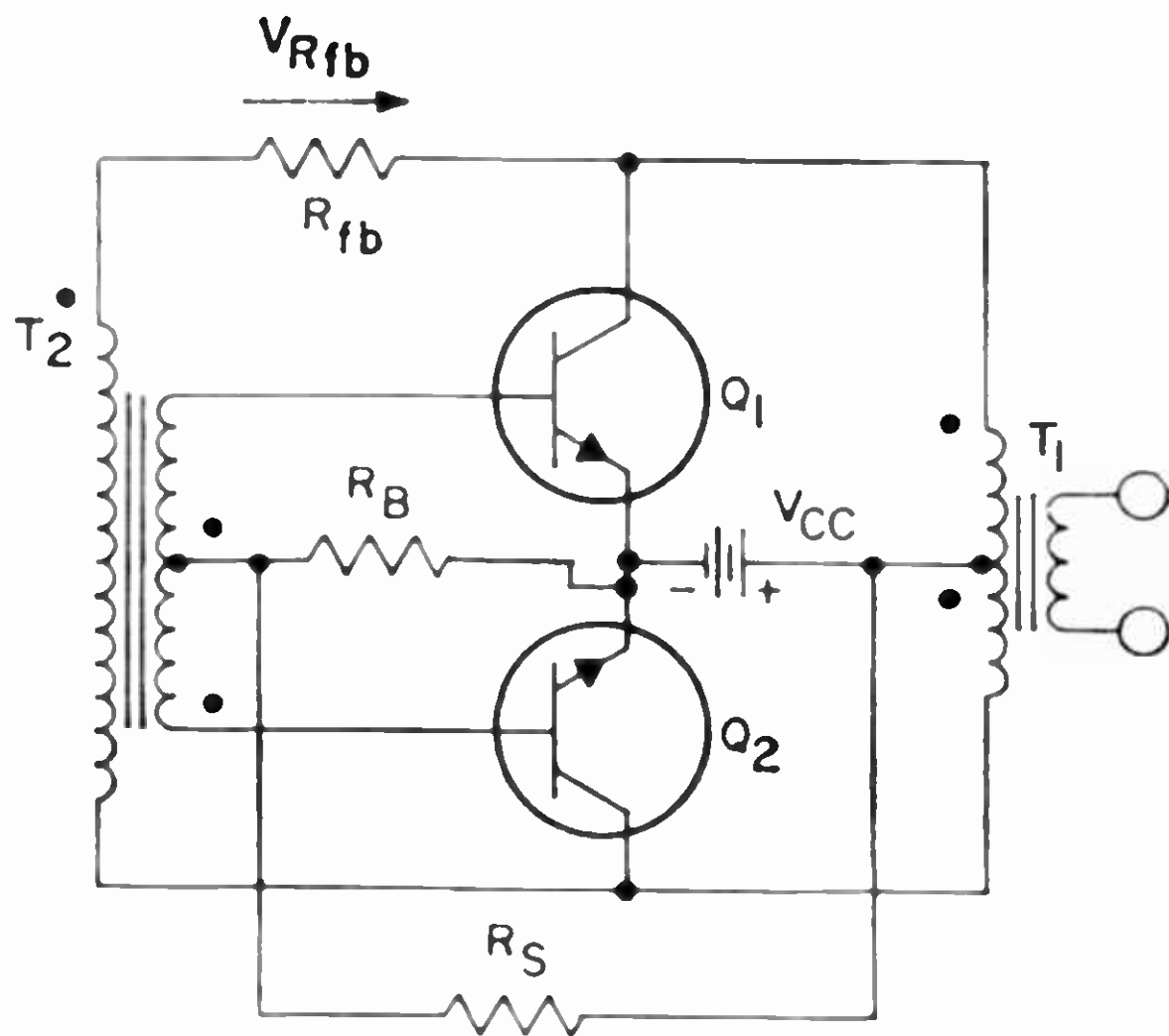


Fig. 245—Two-transistor/two-transformer inverter.

rapidly and causes a rapid increase in V_{Rfb} . As a result, the voltage across T_2 decreases rapidly and Q_2 comes out of saturation. The collector voltage of Q_2 then rises, and regenerative action causes Q_1 and Q_2 to reverse states. As these processes are repeated during succeeding half-cycles, oscillations are sustained.

AUTOMOBILE IGNITION SYSTEM

Fig. 246 shows a simple ignition system that uses an n-p-n transistor; performance curves for the circuit

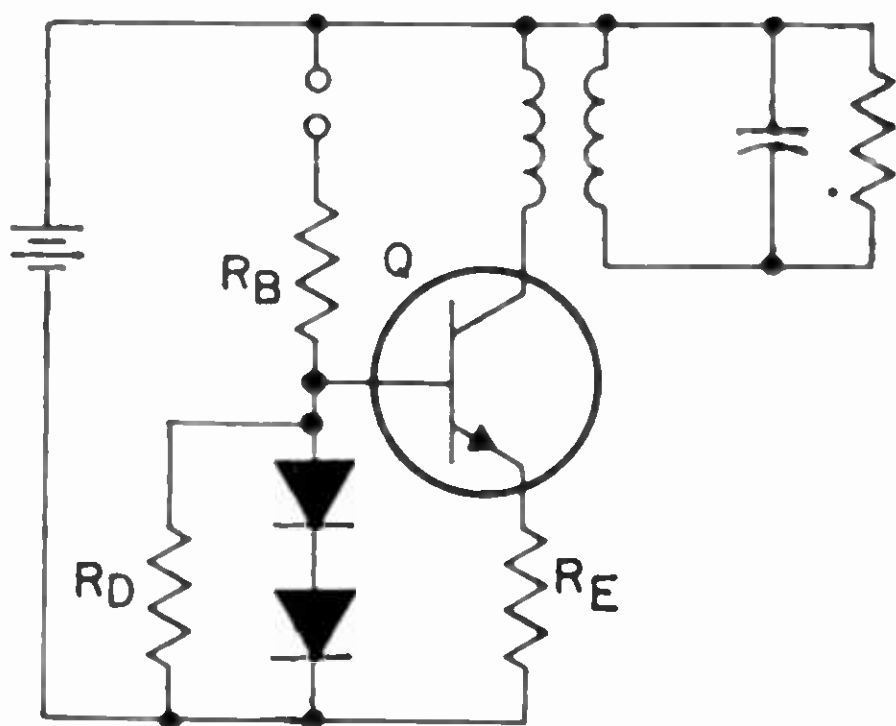


Fig. 246 Solid-state automobile ignition system.

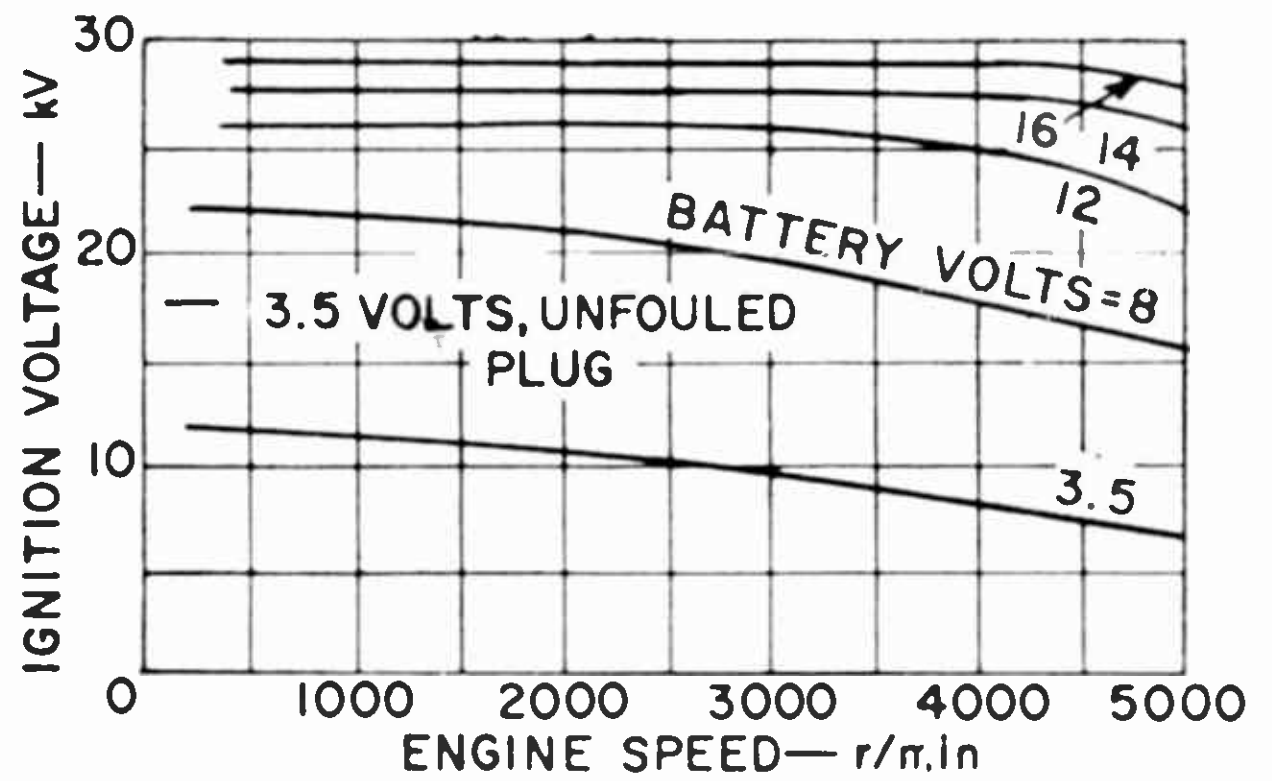


Fig. 247—Ignition voltage as a function of engine speed.

are shown in Fig. 247. The advantages of this circuit include less maintenance of points and spark plugs, better performance at high engine speeds, and easier engine starting.

PULSE MODULATORS

Silicon controlled rectifiers are often used in pulse circuits in which the ratio of peak to average current is large. Typical applications include radar pulse modulators, inverters, and switching regulators. The limiting parameter in such applications often is the time required for forward current to spread over the whole area of the junction. Losses in the SCR are high, and are concentrated in a small region until the entire junction area is in conduction. This concentration produces undesirable high temperatures.

A typical SCR pulse modulator circuit is shown in Fig. 248; basic waveforms for the circuit are shown in Fig. 249. The capacitors of the energy-storage network are charged by the dc supply. The SCR is triggered by pulses from the gate-trigger generator No.1, and the energy-storage network discharges through an inductance and the load (transformer). Fig. 249 shows that the discharge of the storage network ($t_1 - t_2$) is oscillatory; the half-sine-wave shape is characteristic of a single LC-section energy-storage network.

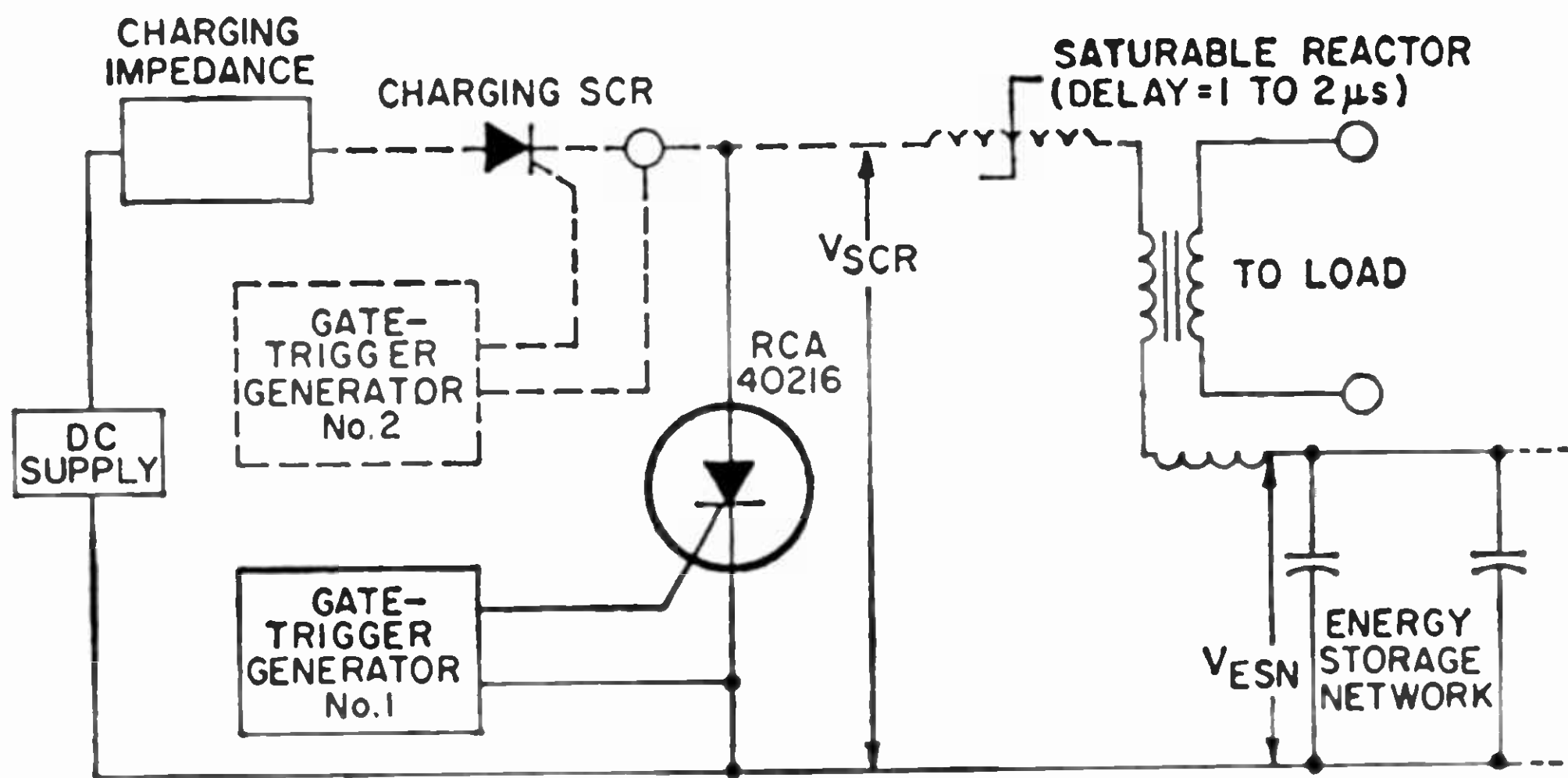


Fig. 248—Basic pulse modulator circuit.

For turn-off, the load is “mismatched” to the discharge-circuit impedance so that a negative voltage is developed on the capacitor at the end of the pulse.

As an example, the rise-time portion of turn-on is defined as the time interval between the 10-percent and 90-percent points on the current wave shape when the SCR is triggered on in a circuit that has rated forward voltage and sufficient

resistance to limit current to rated values. For a 600-volt device, the end of the turn-on interval occurs when the forward voltage drop across the SCR is 60 volts. This value contrasts with the steady-state forward voltage of only 1 or 2 volts under such conditions. An interval many times greater than the turn-on time may be required before the forward voltage drop reduces to the steady-state level.

Thyristors have been widely accepted in power-control applications in industrial systems where high-performance requirements justify the economics of the application. Historically, in the commercial high-volume market, economic considerations have precluded the use of the thyristor. However, with the development of several families of thyristors by RCA designed specifically for mass-production economy and rated for 120- and 240-volt line operation, the use of these devices in controls for many types of small electric motors has been made economically feasible. The controls can be designed to provide good performance, maximum efficiency, and high reliability in compact packaging arrangements.

The simplest form of half-wave power control is shown in Fig. 250. This circuit provides a simple, non-regulating half-wave power control that begins at the 90-degree conduction (peak-voltage) point and

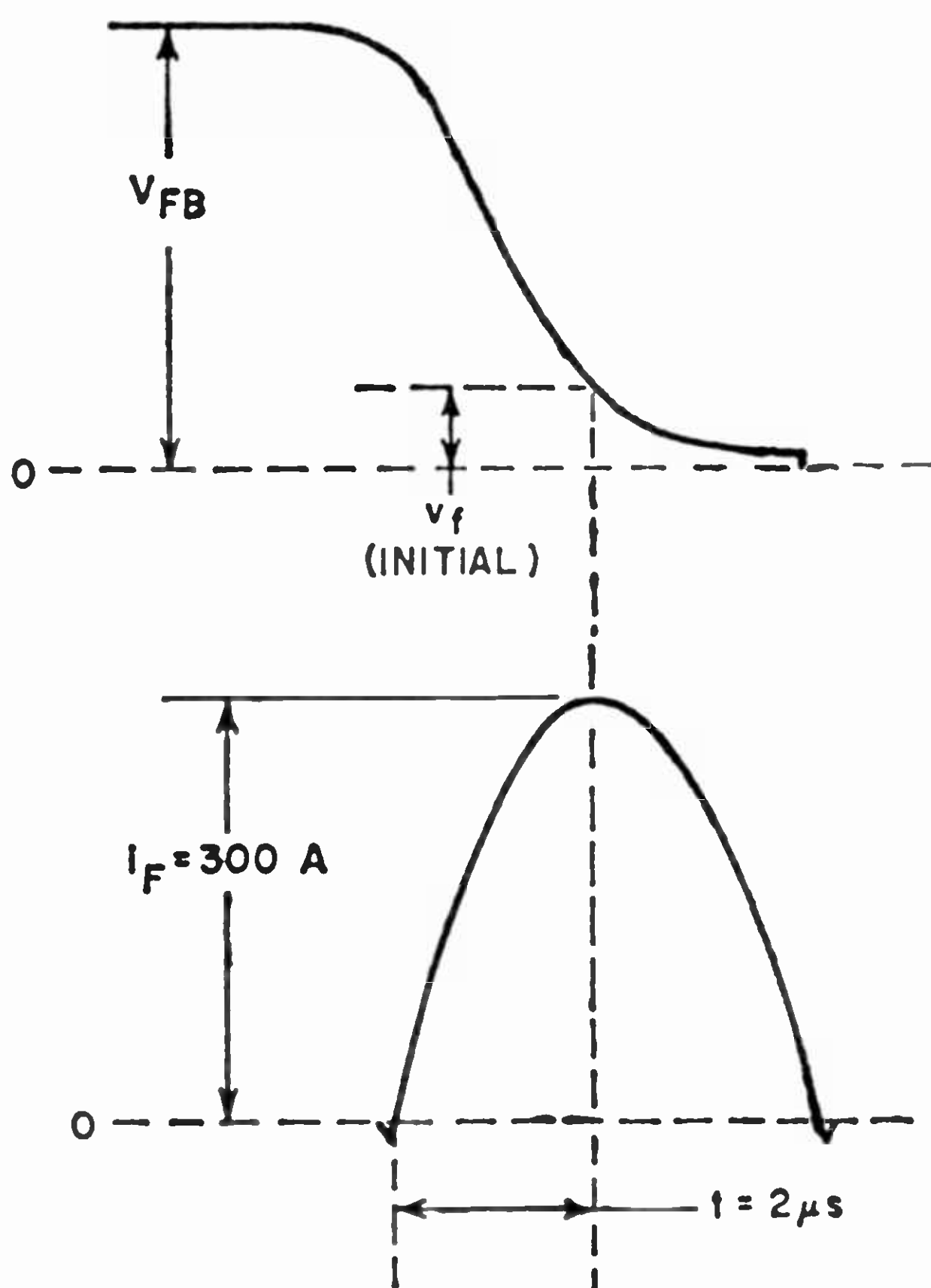


Fig. 249—Turn-on requirements for a pulse-modulator SCR.

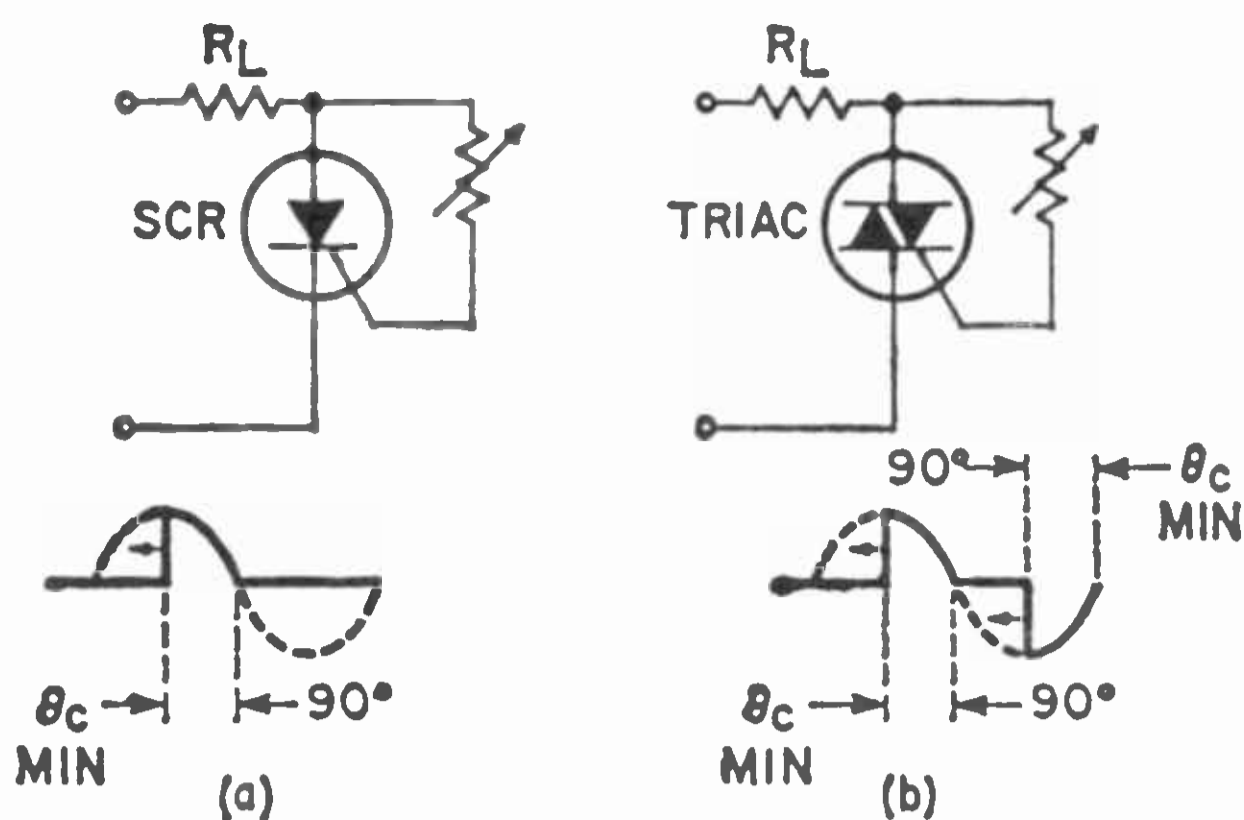


Fig. 250—Degree of control over conduction angles when ac resistive network is used to trigger (a) SCR's and (b) triacs.

may be adjusted to within a few degrees of full conduction (180-degree half-cycle).

The half-wave proportional control shown in Fig. 251 is a non-regulating circuit whose function depends upon an RC delay network for gate phase-lag control. This circuit is better than simple resistance firing circuits because the phase-shifting characteristics of the RC network permit the firing of the SCR beyond the peak of the impressed voltage, resulting in small conduction angles. On the positive half-cycle of the applied voltage, capacitor C is charged through the network R_a and R_b . When the voltage across capacitor C exceeds the gate-firing voltage of the SCR, the SCR is turned on; during the remaining portion of the half-cycle, ac power is applied to the load.

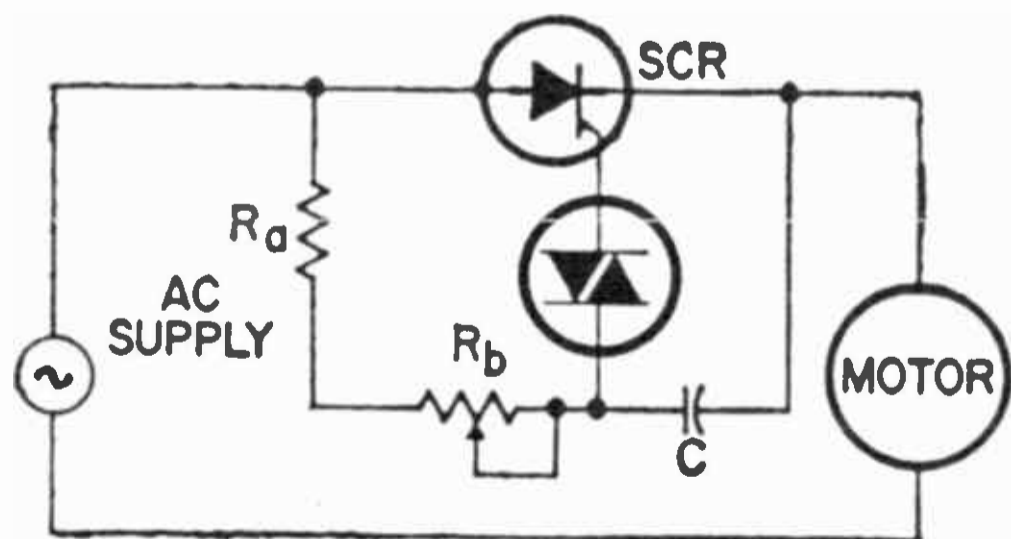


Fig. 251—SCR half-wave proportional power control circuit.

The delay in firing the SCR depends upon the time-constant network (R_a , R_b , C) which produces a gate-firing voltage that is shifted in phase with respect to the supply voltage. The amount of phase shift is adjusted by R_b . With maximum resistance in the circuit, the RC time

constant is longest. This condition results in a large phase shift with a correspondingly small conduction angle. With minimum resistance, the phase shift is small, and essentially the full line voltage is applied to the load.

The control circuit uses the breakdown voltage of a diac as a threshold setting for firing the SCR. The diac is specifically designed for handling the high-current pulses required to trigger SCR's. When the voltage across capacitor C reaches the breakdown voltage of the diac, it fires and C discharges through the diac to its maintaining voltage. At this point, the diac again reverts to its high-impedance state. The discharge of the capacitor from breakdown to maintaining voltage of the diac provides a current pulse of sufficient magnitude to fire the SCR. Once the SCR has fired, the voltage across the phase-shift network reduces to the forward voltage drop of the SCR for the remainder of the half-cycle.

Two SCR's are usually required to provide full-wave power control. Because of the bidirectional switching characteristics of triacs, however, only one of these devices is needed to provide the same type of control. Fig. 252 shows three full-wave power controls that employ thyristors.

In circuits of this type, a rapidly rising off-state voltage can occur across the thyristor when the device changes from a conducting state to a blocking state (commutates). The influence of this dv/dt stress on the operation of the power-control element is described below. Consideration is given only to those circuit applications that utilize a triac as the main power-control element.

The dv/dt stress in a circuit with a resistive load (such as those just described) can be illustrated by consideration of a circuit with a 6-ampere load, i.e., one with a power factor close to unity. The load resistance in this circuit is 20 ohms

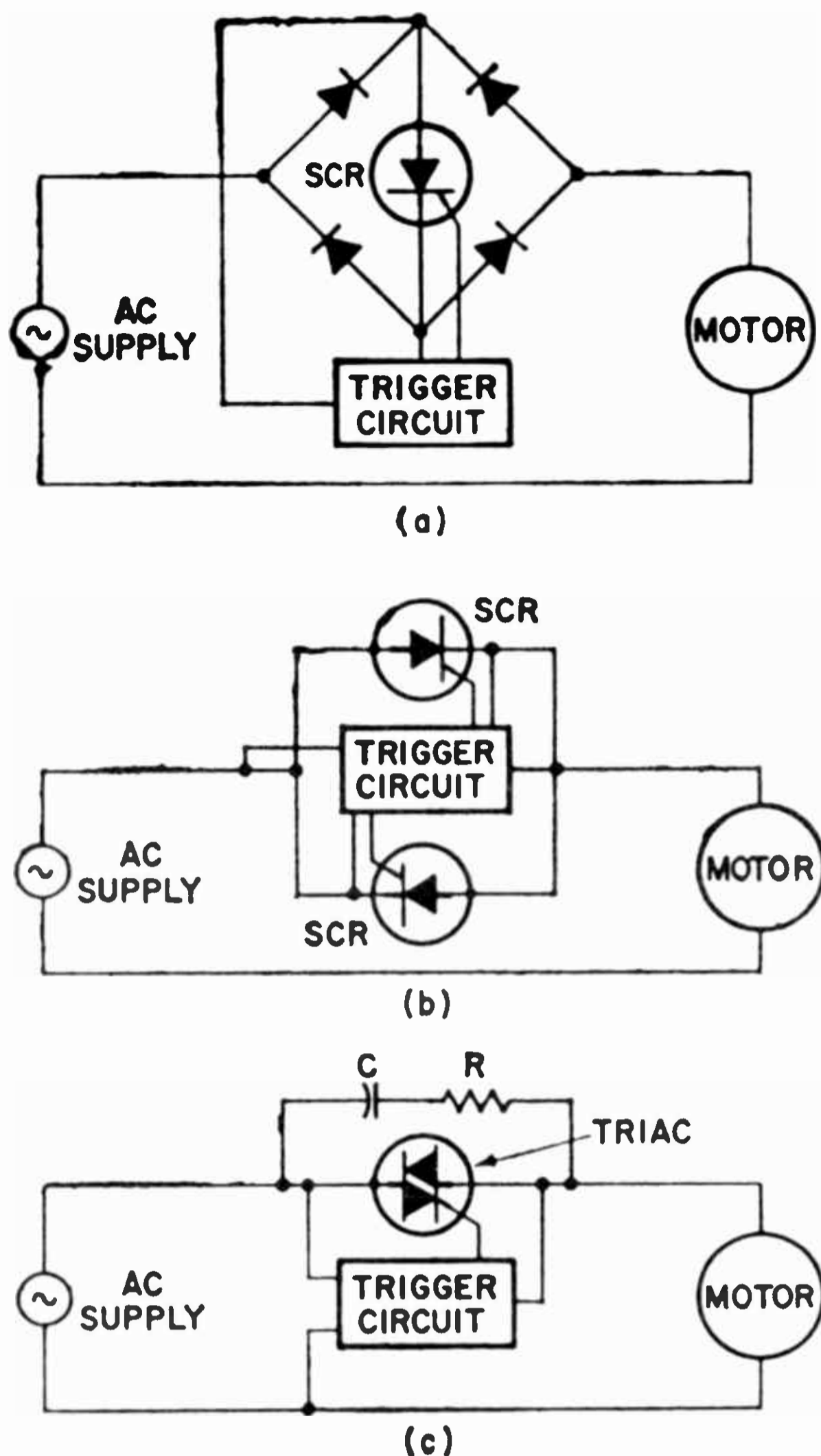


Fig. 252—Full-wave thyristor motor control circuits using (a) bridge rectifier and a single SCR; (b) inverse parallel SCR's; (c) a triac.

for a source voltage of 120 volts. If the total circuit inductance is assumed to be 500 microhenries and the total triac and stray capacitance is 500 picofarads, the circuit factor for the conducting state is 0.99996, lagging. Thus, the load current lags the line voltage by the small phase delay of approximately 25 microseconds. At the time that the triac commutates current, the line voltage is 1.6 volts. At this time, a transient damped oscillation occurs as a result of the interaction of the triac junction capacitance and the circuit inductance. For the circuit parameter values given ($R = 20$ ohms, $L = 500$ microhenries, and $C = 500$ picofarads), the frequency of oscillation is 3.2×10^6 Hz. Calculation of the maximum dv/dt stress across the triac yields a value of 1.97 volts per

microsecond. The voltage at the time of commutation is then 1.6 volts, and the maximum commutating dv/dt becomes 3.15 volts per microsecond.

Thus, it can be seen that a definite dv/dt stress is imposed on the triac even when the load is primarily resistive. Because all resistive circuit configurations have some small inductance associated with them, a commutating dv/dt stress is produced in all resistive circuits. Fig. 253 shows a commutating dv/dt waveshape for a resistive load of 6 amperes in a 120-volt triac control circuit.

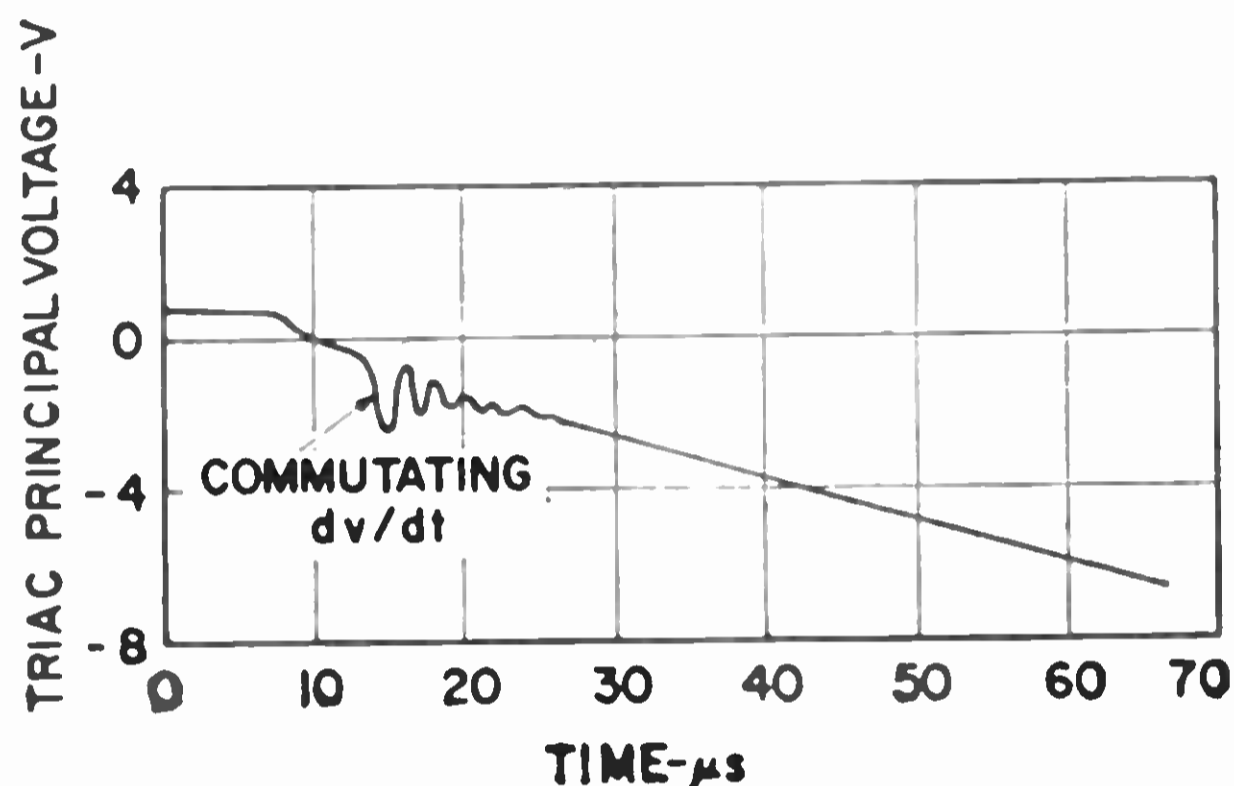


Fig. 253—Triac principal voltage during commutation of a resistive load.

The use of triacs for full-wave ac power control results in either fixed or adjustable power to the load. Fixed load power is achieved by use of the triac as a static on-off switch which applies effectively all of the available line voltage to the load, or by use of the triac in a fixed-phase firing mode which applies only the desired portion of the line voltage to the load. The latter method of operation is but one point of an infinite number of available points which can be attained by variable-phase firing operation.

Fig. 254 shows the current and voltage waveshapes produced when a triac is used to control ac power to a highly inductive load for on-off triac operation; Fig. 255 illustrates the waveshapes for phase-control operation. Because the load is highly inductive ($\omega L \gg R$), the load current lags the line voltage by some phase angle θ . When the current

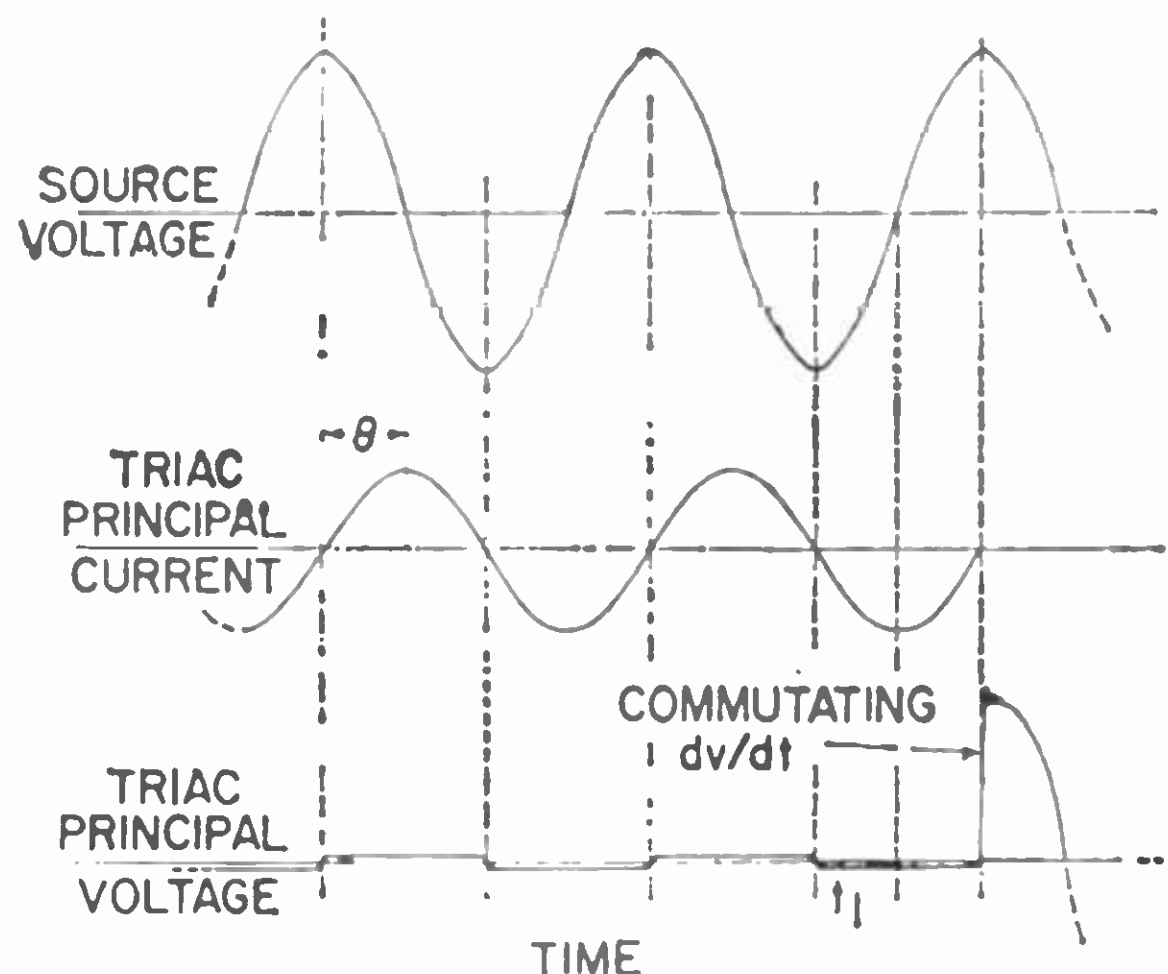


Fig. 254—Principal voltage and current for static-switch triac operation with an inductive load.

through the triac (i.e., the load current) goes to zero (commutates), the triac turns off. In static control operation, the triac is immediately turned on by continuous application, or re-application, of the gate triggering signal; thus, this signal causes the triac to continue conducting for the desired number of successive half-cycles.

As shown in Fig. 254, at time t_1 , the gate is opened and the triac continues to conduct for the remainder of that half-cycle of load current. At the end of the half-cycle, commutation occurs and the triac is subjected to an off-state blocking voltage which has a polarity opposite to the conducted current and a magnitude equal to the value of line voltage at that instant. Because the triac goes from a conducting state to a blocking state in a very short period of time, the rate of rise of off-state voltage is very rapid. This rapidly rising off-state voltage produces a dv/dt across the main power terminals of the triac and can result in the triac going into conduction if the triac is incapable of withstanding the dv/dt .

Fig. 255 shows the waveshapes produced for phase-control operation with an inductive load. The oscillations which are present on the peaks of the voltage waveform are the result of interaction of the cir-

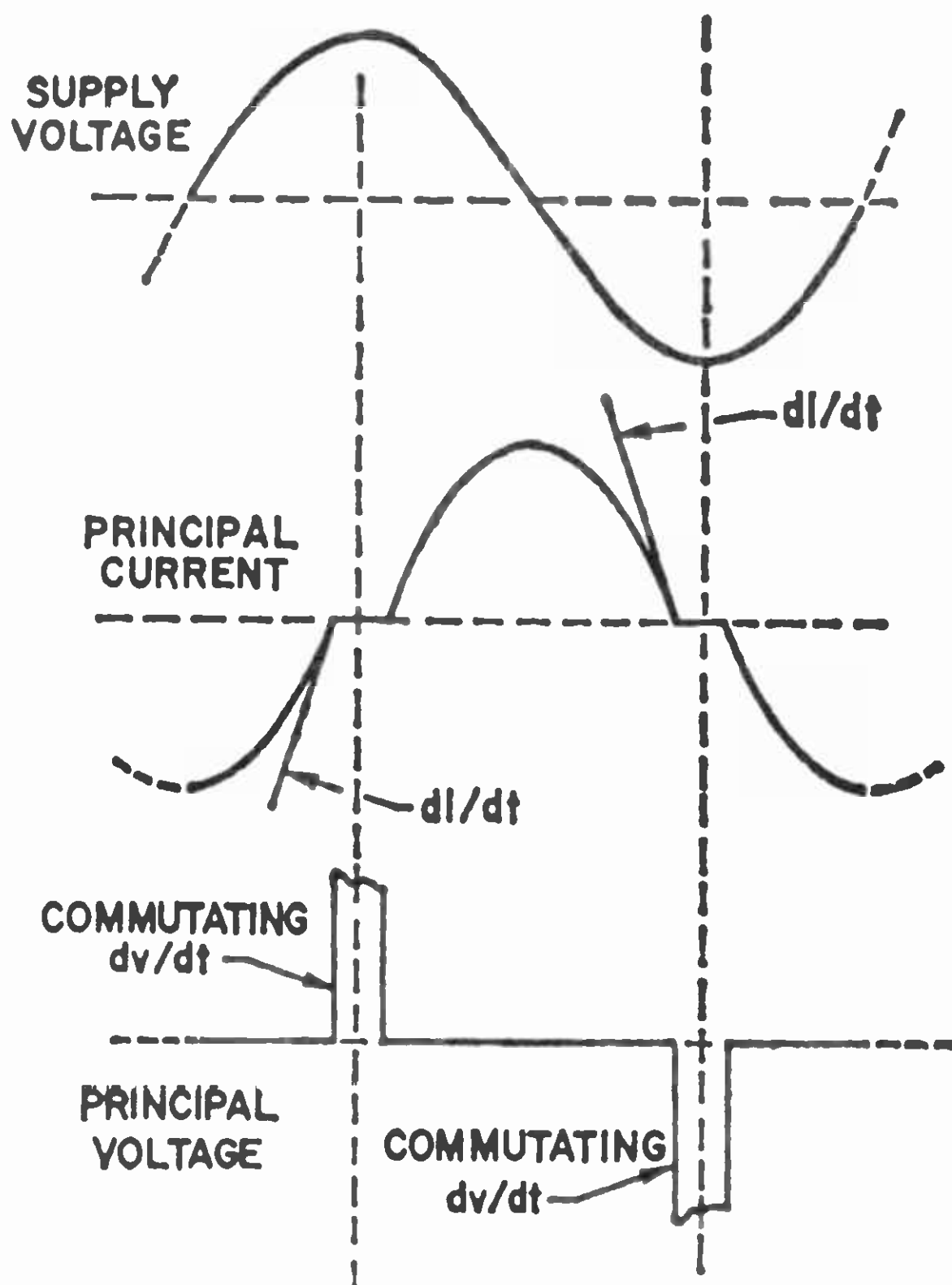


Fig. 255—Principal voltage and current for phase-control triac operation with an inductive load.

this type of operation, the stress caused by the commutating dv/dt is produced each time the current crosses the zero-axis and, therefore, occurs at a frequency equal to twice the line-voltage frequency. If the triac is incapable of sustaining the dv/dt which is produced, it goes into a conducting state and remains in continuous conduction, supplying current to the load. This malfunction is illustrated in Fig. 256.

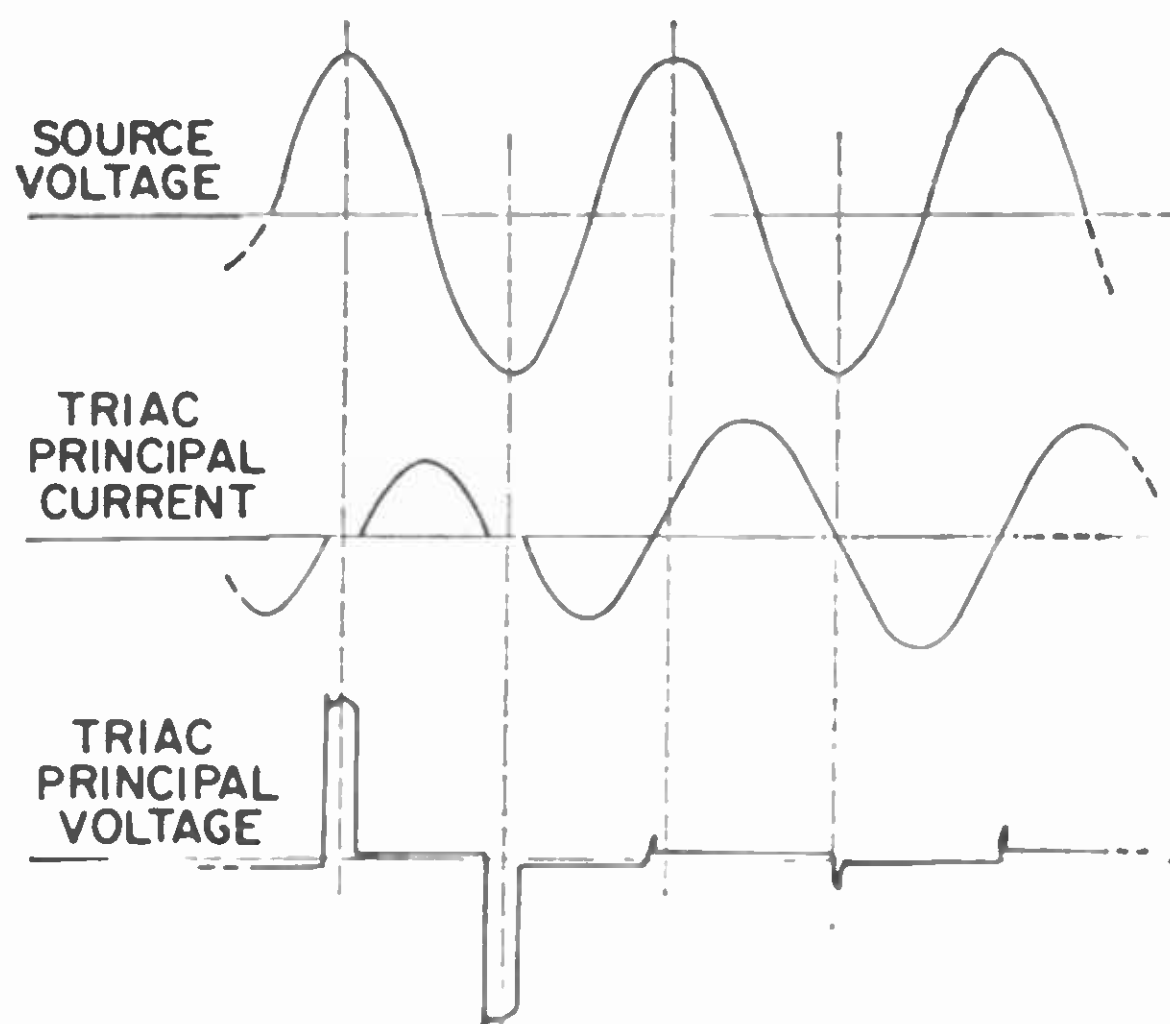


Fig. 256—Principal voltage and current showing malfunction of triac as a result of commutating dv/dt produced by an

Fig. 257(a) shows the circuit diagram of a series connection of voltage source, triac, and load. An equivalent circuit for this series connection is shown in Fig. 257(b). When the triac is in conduction, the triac junction capacitance is shunted by a low-value, nonlinear resistance which minimizes the effect of triac capacitance. However, when the triac

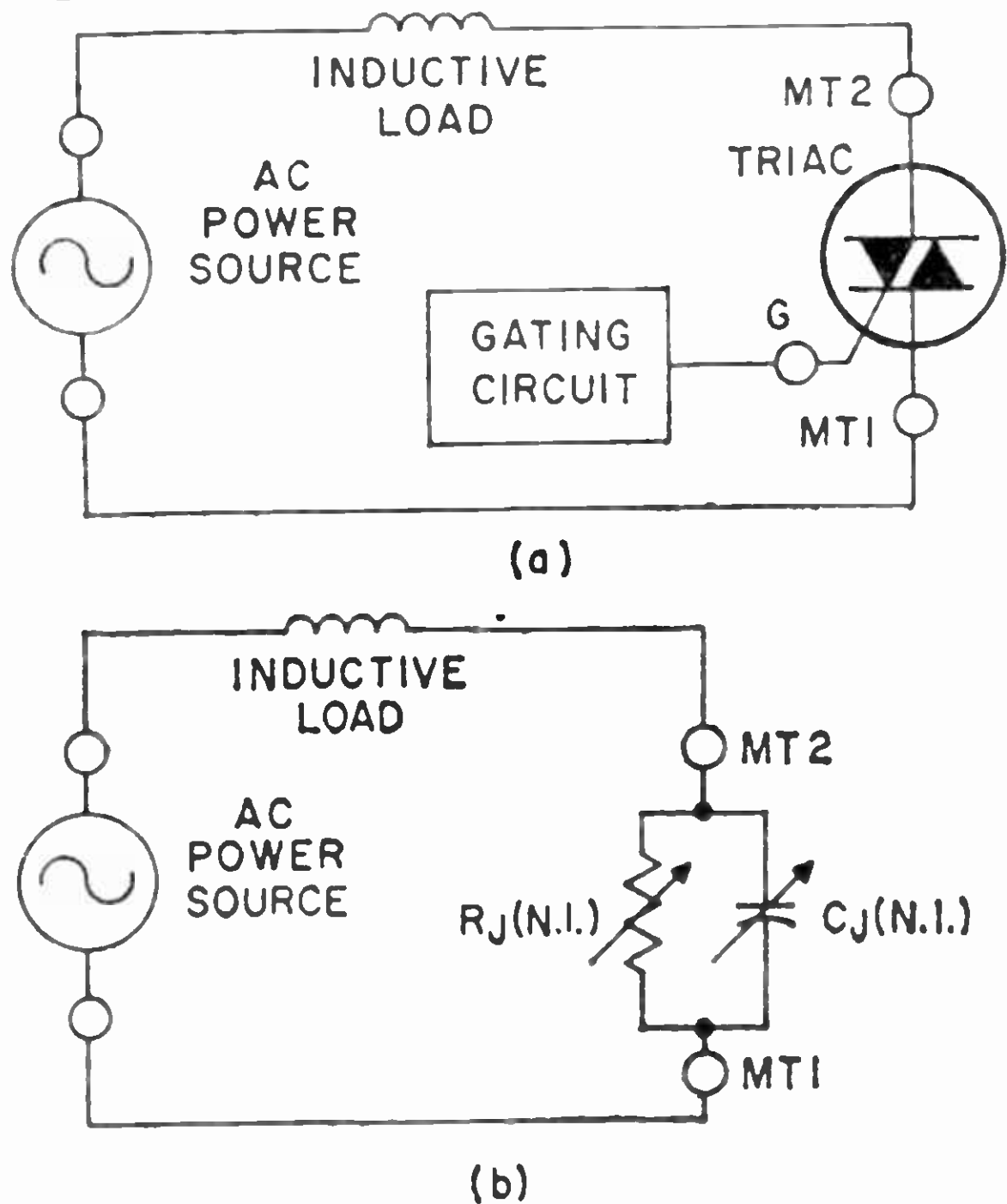


Fig. 257—(a) Series-circuit connection of triac, inductive load, and ac power source; and (b) equivalent circuit.

goes out of conduction, the resistive component becomes very large and the equivalent triac shunting capacitance becomes significant. Because the circuit is basically a series RLC circuit, the voltage waveshape and the rate of rise of voltage across the triac at commutation are determined by the magnitude of source voltage and the circuit inductance, capacitance, and resistance. Thus the rising off-state voltage across the triac can be an overdamped, critically damped, or underdamped oscillation.

Fig. 258 shows a low-current triac in use in a simple, common, proportional-control application; the circuit consists of a single RC time constant and a threshold device. The trigger diac is used as a threshold device to remove the dependence of the trigger circuit on

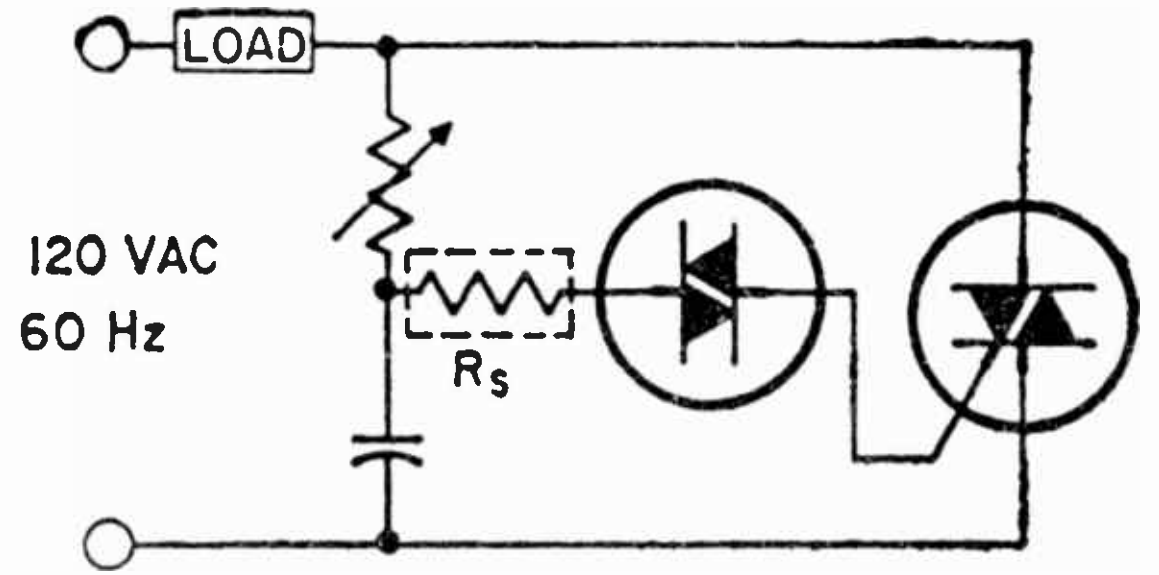


Fig. 258—Simple control circuit using a single time constant.

variations in gate trigger characteristics. The circuit can provide sufficient control for many applications, such as heaters and motor-speed and switching controls. Because of its simplicity, the circuit can be packaged in confined areas where space is at a premium. Electrically, it displays a hysteresis effect and initially turns on for resistive loads with a conduction angle which may be too large; however, it provides maximum power output at the full "on" position of the control potentiometer.

The hysteresis effect produced by a single-time-constant circuit can be reduced by addition of a resistor (R_s) in series with the trigger diac, as shown by the dotted lines in Fig. 258. The series resistor reduces the capacitor discharge time and thus provides reduced time lag because of the diac turn-on-characteristics.

The circuit shown in Fig. 259 uses a double-time-constant control to improve on the performance of the single-time-constant control circuit. This circuit minimizes the hysteresis effect and allows the triac to turn on at small conduction angles. The circuit has the advantages of low hysteresis, bidirectional operation at

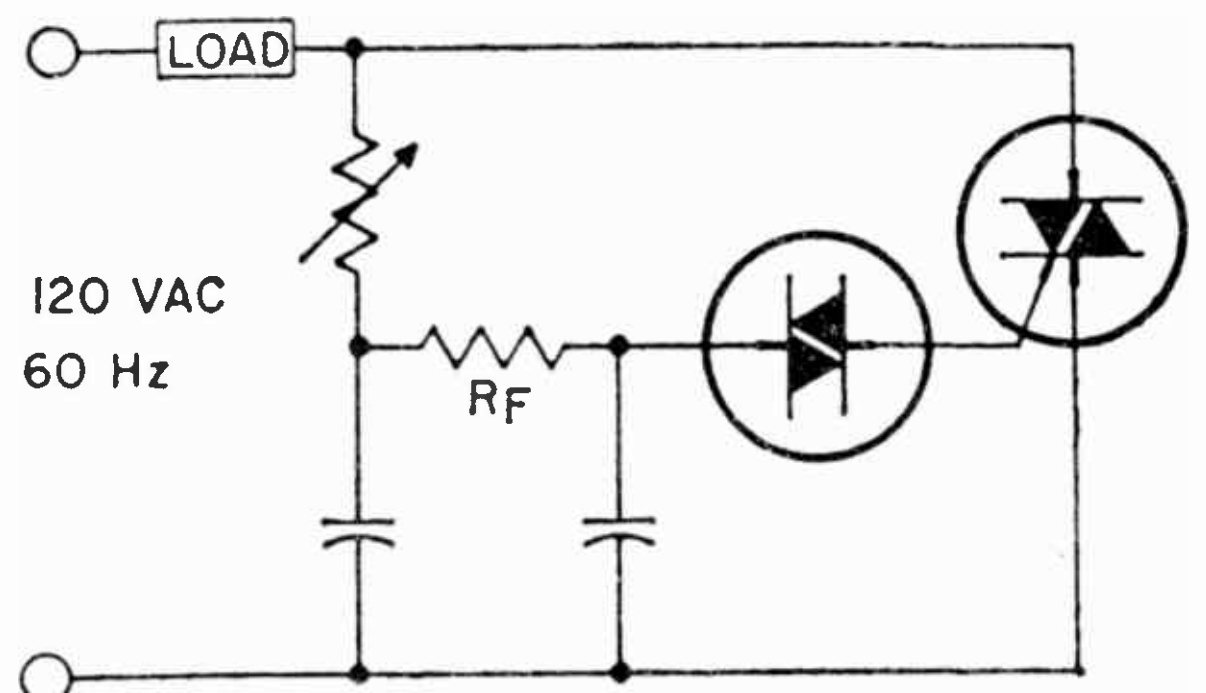


Fig. 259—Control circuit using a double time constant.

small conduction angles, and continuous control up to the maximum conduction angle. In addition, the fixed resistor R_r can be replaced by a trimmer potentiometer for minimum control at low conduction angles.

The circuit shown in Fig. 260 uses a neon bulb as a threshold device rather than the solid-state diac. This circuit has the advantages of low hysteresis, bidirectional operation at small conduction angles, and

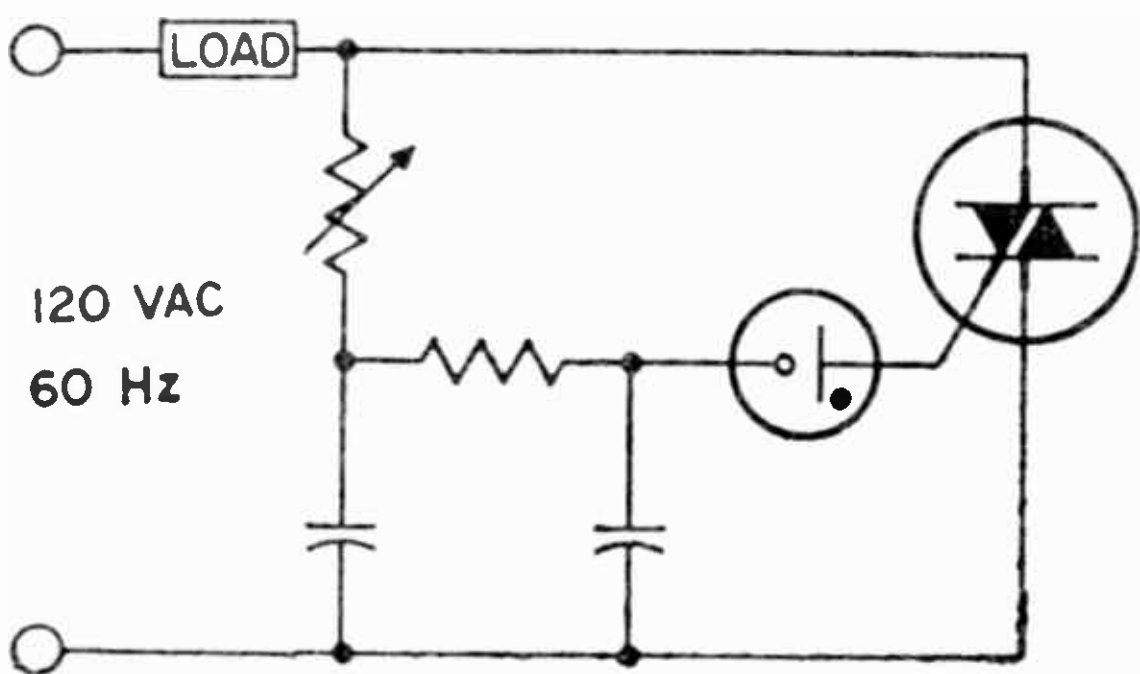


Fig. 260—Control circuit using a neon-bulb threshold device.

continuous control up to the maximum conduction angle. Because the neon-bulb threshold voltage is higher than that of a solid-stage diac, however, full 360-degree control may not be achieved.

Fig. 261 shows a circuit in which an SCR controls the triggering and operation of a triac in an integral-cycle control circuit which is radio-frequency-interference free. A basic SCR gate-trigger or gate-control

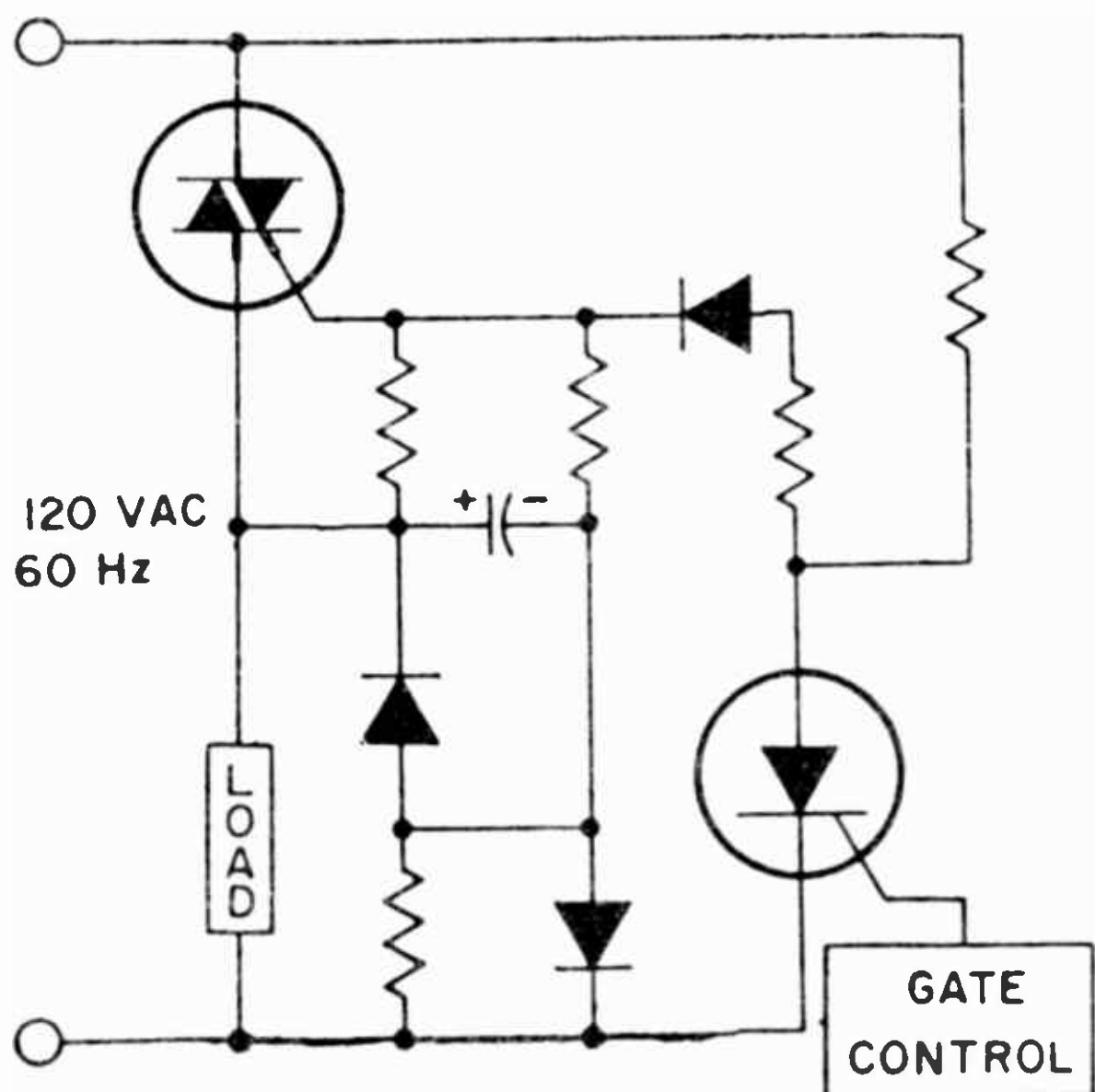


Fig. 261—Integral-cycle control circuit.

circuit can be represented by a voltage source and a series resistance, as shown in Fig. 262. The series resistance should include both the ex-

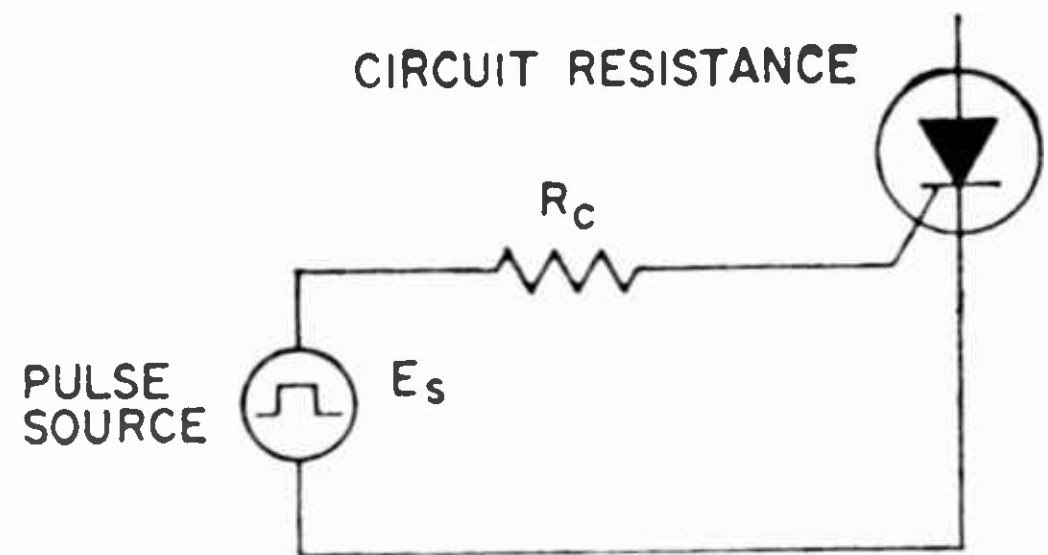


Fig. 262—Equivalent gate trigger circuit.

ternal circuit resistance and the internal generator resistance. With this type of equivalent circuit, the conventional load-line approach to gate trigger-circuit design can be used. With pulse-type triggering, it is assumed initially that the time required to trigger all SCR's of the same type is known, and that the maximum allowable gate trigger pulse widths for specific peak gate power inputs are to be determined. The magnitude of gate trigger current required to turn on an SCR of a given type can be determined from the turn-on characteristics shown in the section on Thyristors.

The triac in Fig. 261 is not triggered as long as the SCR is on. When the SCR is turned off by removal of the gate signal and application of a negative anode potential, the triac is triggered on at the beginning of the next half-cycle. When the triac conducts, the capacitor charges up to the peak supply voltage and retains its charge to trigger the triac on in the next half-cycle. When the triac conducts in the reverse direction, the negative charge on the capacitor is held to a low value so that it does not trigger the triac when the supply voltage reverses. If the SCR is still off, the triac repeats its conduction angle. If the SCR is conducting, the triac does not trigger on, but remains off until the SCR is again turned off. This circuit provides the unique function of integral-cycle switching, i.e., once the triac is triggered on, it completes one full cycle before turning off. This type

of switching eliminates dc components present with half-wave control. The circuit also provides synchronous switching, i.e., the triac turns on at the beginning of the cycle and does not generate RFI.

LIGHT CONTROLS

A simple, inexpensive light-dimmer circuit can be constructed with a diac, a triac, and an RC charge-control network. It is important to remember that a triac in this type of circuit dissipates power at the rate of about one watt per ampere. Therefore, some means of removing heat must be provided to keep the device within its safe operating-temperature range. On a small light-control circuit such as one built into a lamp socket, the lead-in wire serves as an effective heat sink. Attachment of the triac case directly to one of the lead-in wires provides sufficient heat dissipation for operating currents up to 2 amperes (rms). On wall-mounted controls operating up to 6 amperes, the combination of faceplate and wallbox serves as an effective heat sink. For higher-power controls, however, the ordinary faceplate and wallbox do not provide sufficient heat-sink area. In this case, additional area may be obtained by use of a finned face plate that has a cover plate which stands out from the wall so air can circulate freely over the fins.

On wall-mounted controls, it is also important that the triac be electrically isolated from the face plate, but at the same time be in good thermal contact with it. Although the thermal conductivity of most electrical insulators is relatively low when compared with metals, a low-thermal-resistance, electrically isolated bond of triac to faceplate can be obtained if the thickness of the insulator is minimized and the area for heat transfer through the insulator is maximized. Suitable insulating materials are fiber-glass tape, ceramic sheet, mica, and polyimide film. Fig. 263 shows two

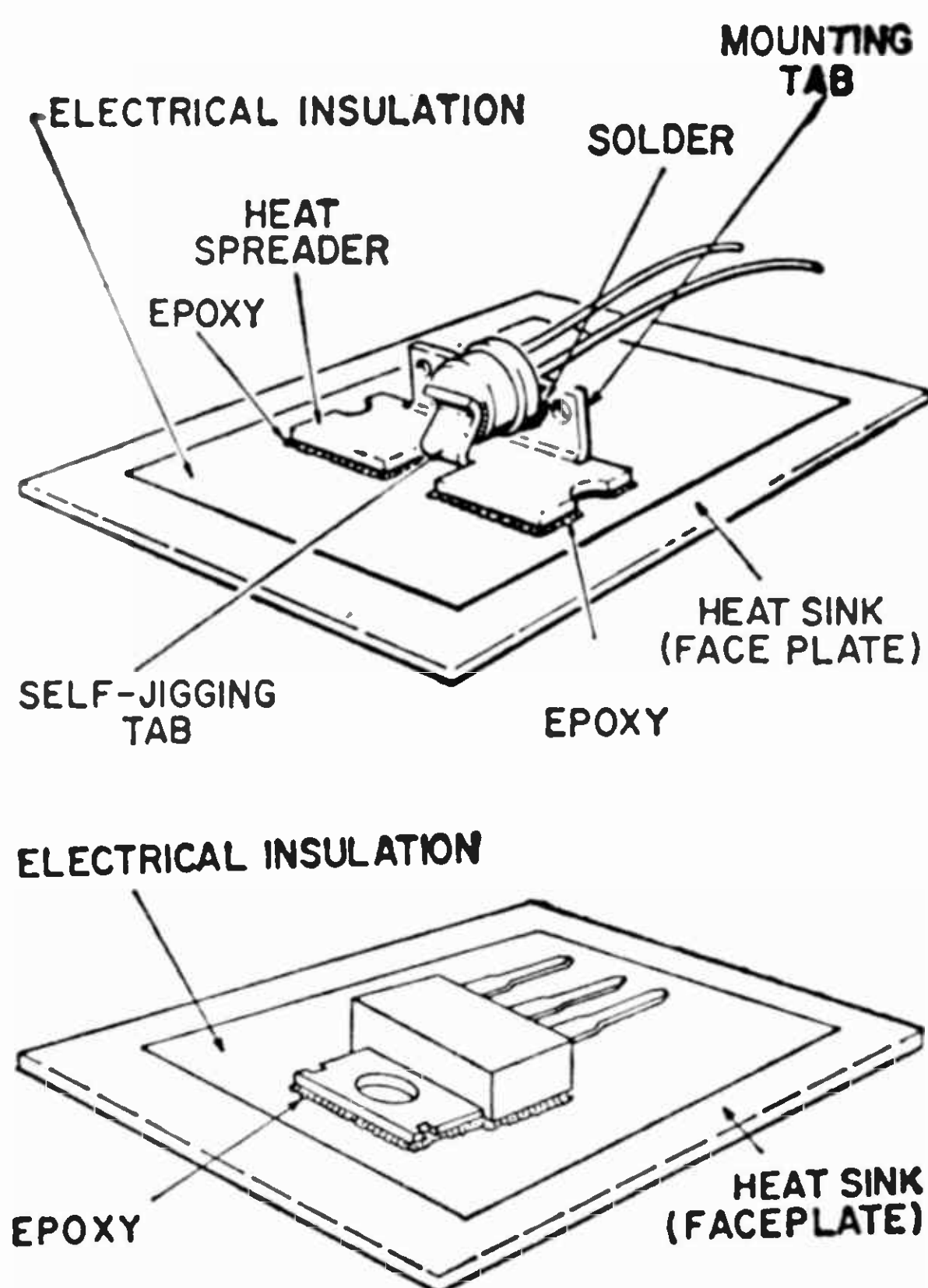


Fig. 263—Examples of isolated mounting of triacs.

examples of isolated mounting for triacs in a TO-5 package and the new plastic package. Electrical insulating tape is first placed over the inside of the faceplate. The triac is then mounted to the insulated faceplate by use of epoxy-resin cement.

Because the light output of an incandescent lamp depends upon the voltage impressed upon the lamp filament, changes in the lamp voltage vary the brightness of the lamp. When ac source voltages are used, a triac can be used in series with an incandescent lamp to vary the voltage to the lamp by changing its conduction angle; i.e., the portion of each half-cycle of ac line voltage in which the triac conducts to provide voltage to the lamp filament. The triac, therefore, is very attractive as a switching element in light-dimming applications.

To switch incandescent-lamp loads reliably, a triac must be able to withstand the inrush current of the lamp load. The inrush current is a result of the difference between the cold and hot resistance of the tungsten

filament. The cold resistance of the tungsten filament is much lower than the hot resistance. The resulting inrush current is approximately 12 times the normal operating current of the lamp.

The simplest circuit that can be used for light-dimming applications is shown in Fig. 264 and uses a diac in series with the gate of a triac to minimize the variations in gate

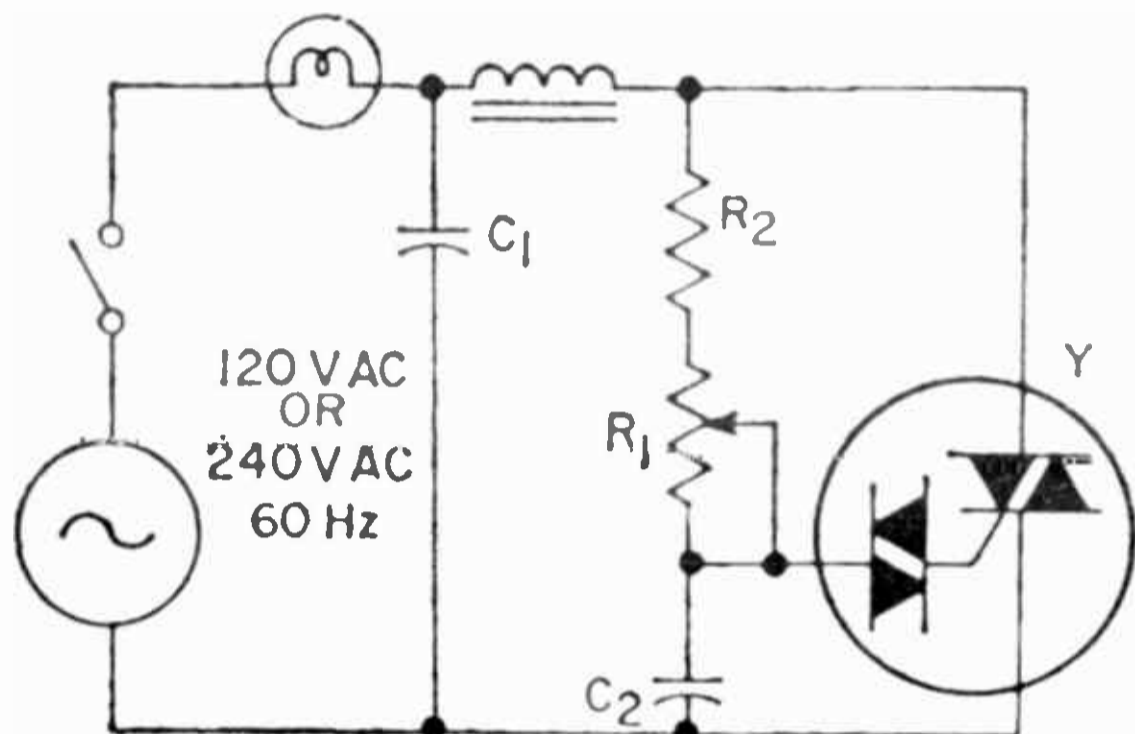


Fig. 264—Single-time-constant light-dimmer circuit.

trigger characteristics. In applications where space is at a premium, the RCA-40431 or RCA-40432, which combine the functions of both triac and diac, may be used. Changes in the resistance in series with the capacitor change the conduction angle of the triac. Because of its simplicity, this circuit can be packaged in confined areas where space is at a premium.

The capacitor in the circuit of Fig. 264 is charged through the control potentiometer and the series resistance. The series resistance is used to protect the potentiometer by limiting the capacitor charging current when the control potentiometer is at its minimum resistance setting. This resistor may be eliminated if the potentiometer can withstand the peak charging current until the triac turns on. The diac conducts when the voltage on the capacitor reaches its breakover voltage. The capacitor then discharges through the diac to produce a current pulse of sufficient amplitude and width to trigger the triac. Because the triac can be triggered with either polarity of gate signal, the same operation oc-

curs on the opposite half-cycle of the applied voltage. The triac, therefore, is triggered and conducts on each half-cycle of the input supply voltage.

The interaction of the RC network and the trigger diode results in a hysteresis effect when the triac is initially triggered at small conduction angles. The hysteresis effect is characterized by a difference in the control potentiometer setting when the triac is first triggered and when the circuit turns off. Fig. 265 shows the interaction between the RC network and the diac to produce the hysteresis effect. The capacitor voltage and the ac line voltage are shown as solid lines. As the resistance in the circuit is decreased from its maximum value, the capacitor voltage reaches a value which fires the diac. This point is designated A on the capacitor-voltage waveshape. When the diac fires, the

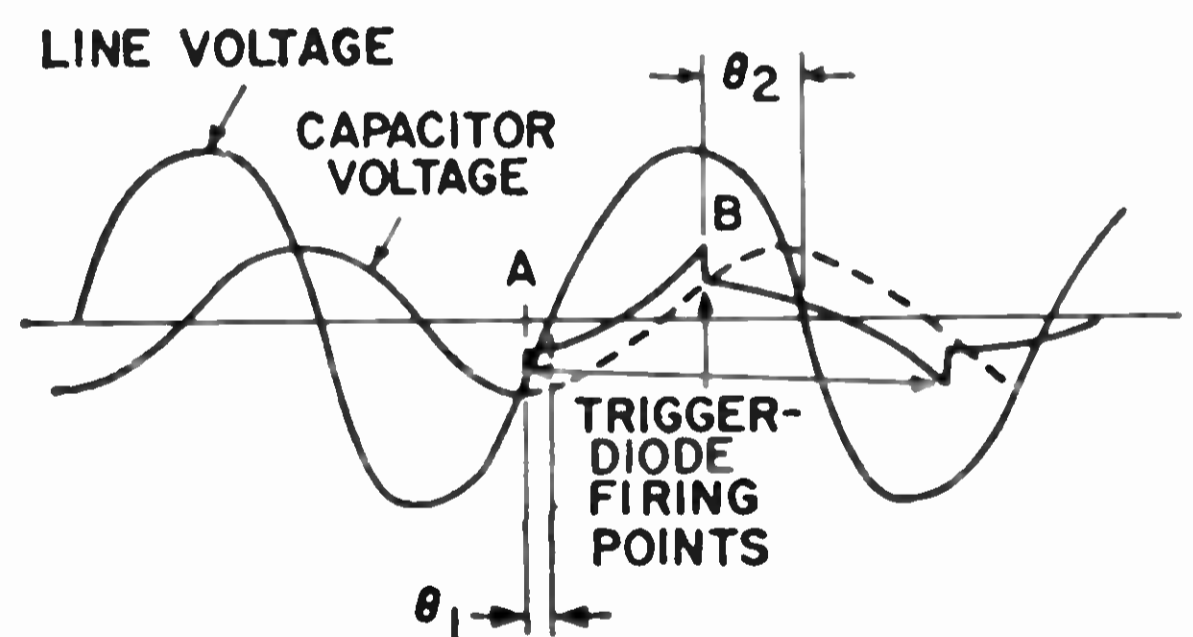


Fig. 265—Waveforms showing interaction of control network and trigger diode.

capacitor discharges and triggers the triac at an initial conduction angle θ_1 . During the forming of the gate trigger pulse, the capacitor voltage drops suddenly. The charge on the capacitor is smaller than when the diac did not conduct. As a result of the different voltage conditions on the capacitor, the break-over voltage of the diac is reached earlier in the next half-cycle. This point is labeled B on the capacitor-voltage waveform. The conduction angle θ_2 corresponding to point B is greater than θ_1 . All succeeding conduction angles are equal to θ_2 in magnitude. When the circuit resistance is increased by a change

in the potentiometer setting, the triac is still triggered, but at a smaller conduction angle. Eventually, the resistance in series with the capacitance becomes so great that the voltage on the capacitor does not reach the breakover voltage of the diac. The circuit then turns off and does not turn on until the circuit resistance is again reduced to allow the diac to be fired. The hysteresis effect makes the voltage load appear much greater than would normally be expected when the circuit is initially turned on.

The double-time-constant circuit in Fig. 266 improves on the performance of the single-time-constant control circuit. This circuit uses an

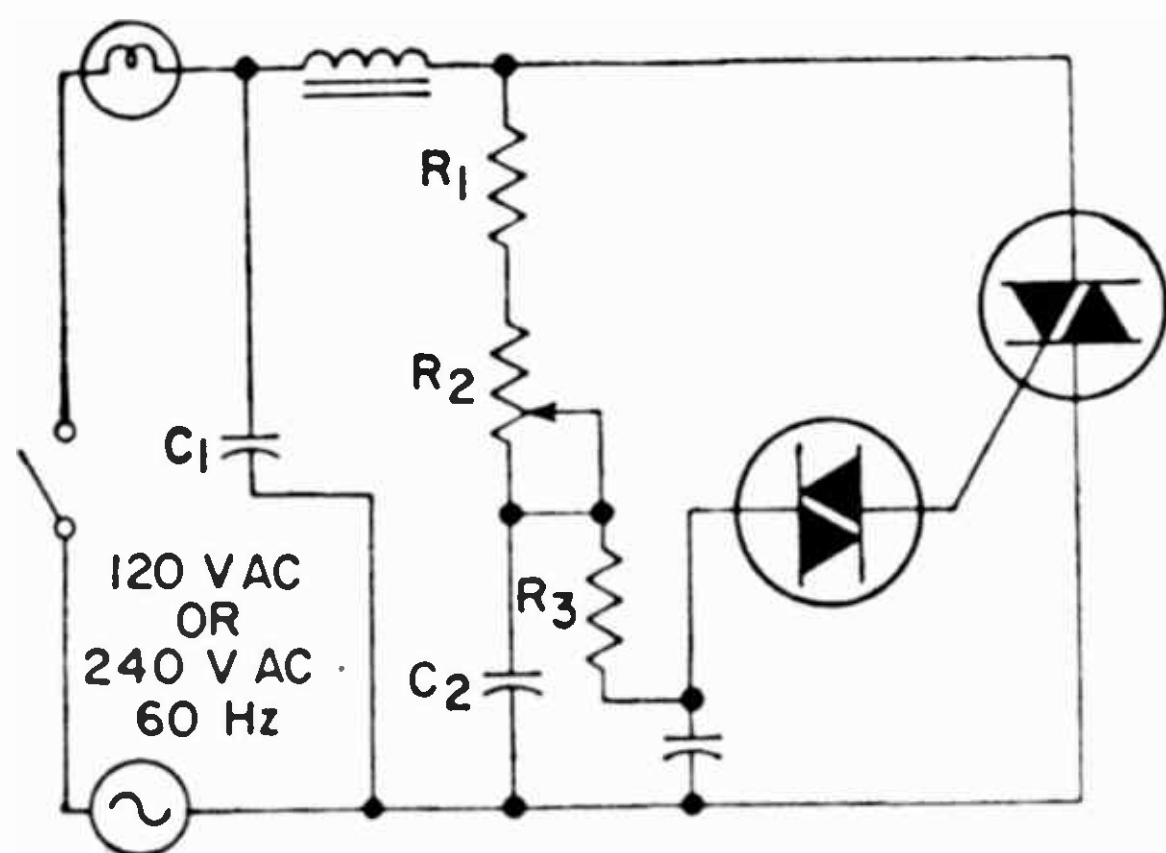


Fig. 266—Double-time-constant light-dimmer circuit.

additional RC network to extend the phase angle so that the triac can be triggered at small conduction angles. The additional RC network also minimizes the hysteresis effect. Fig. 267 shows the voltage waveforms for the ac supply and the trigger capacitor of the circuit of Fig. 266. Because of the voltage drop across R_3 , the input capacitor C_2 charges to a higher voltage than the trigger capacitor C_3 . When the voltage on C_3 reaches the breakover voltage

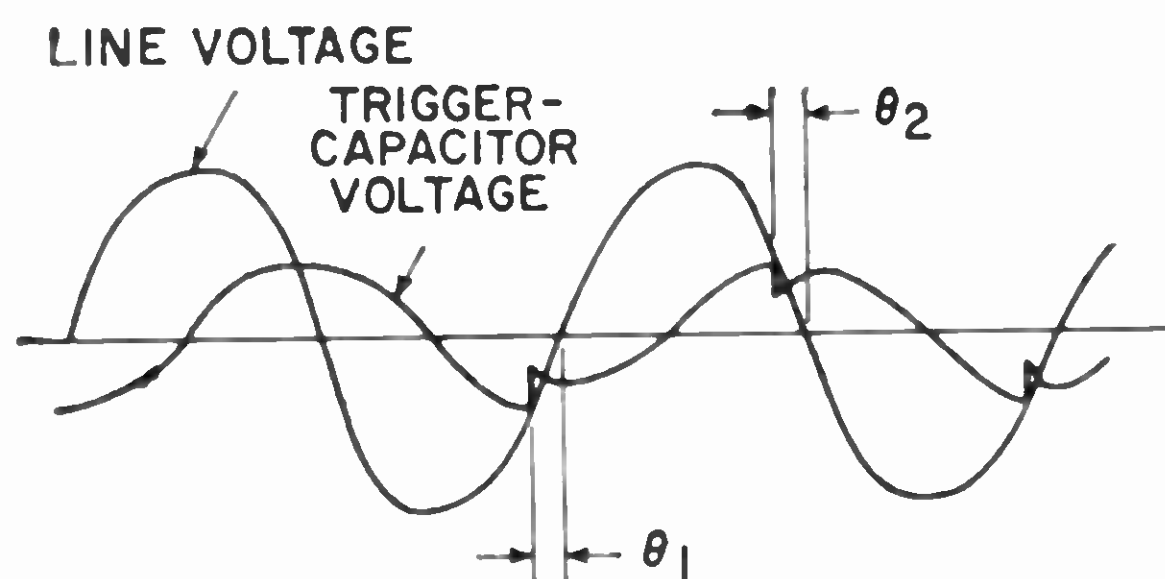


Fig. 267—Voltage waveforms of double-time-constant control circuit.

of the diac, it conducts and causes the capacitor to discharge and produce the gate-current pulse to trigger the triac. After the diac turns off, the charge on C_3 is partially restored by the charge from the input capacitor C_2 . The partial restoration of charge on C_3 results in better circuit performance with a minimum of hysteresis.

For applications requiring a light-activated circuit, such as outdoor or indoor lights, the circuit shown in Fig. 268 can be employed. Although this circuit functions in the

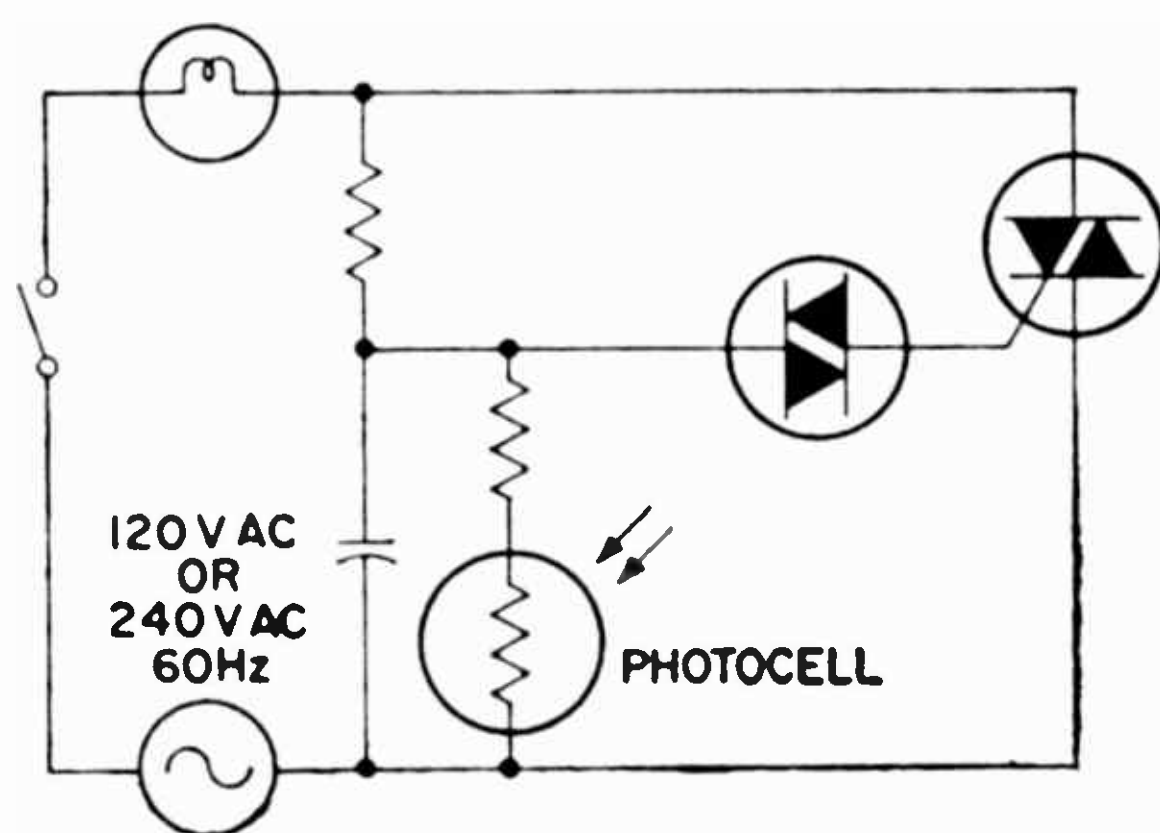


Fig. 268—Light-controlled turn-off circuit.

same manner as the light-dimmer circuit, the photocell controls its operation. When the light impinges on the surface of the photocell, the resistance of the photocell becomes low and prevents the voltage on the trigger capacitor from increasing to the breakover voltage of the trigger diode. The circuit is then inoperative. When the light source is removed, the photocell becomes a high resistance. The voltage on the trigger capacitor then increases to the breakover voltage of the trigger diode and causes the diode to fire. The trigger pulse formed by the capacitor discharge through the trigger diode makes the triac conduct and operates the circuit. The triac continues to be triggered on each half-cycle and supplies power to the load as long as the resistance of the photocell is high. When light again impinges on the surface of the photocell and reduces its resistance, the voltage on the capacitor can no longer reach the break-

over voltage of the trigger diode, and the circuit turns off.

For applications requiring operation when light impinges on the surface of the photocell, the circuit of Fig. 269 is recommended. In this circuit, low resistance of the photocell allows the triac to be triggered on. When light is removed from the photocell, the increased resistance of the photocell prevents the triac from being triggered and renders the circuit inoperative.

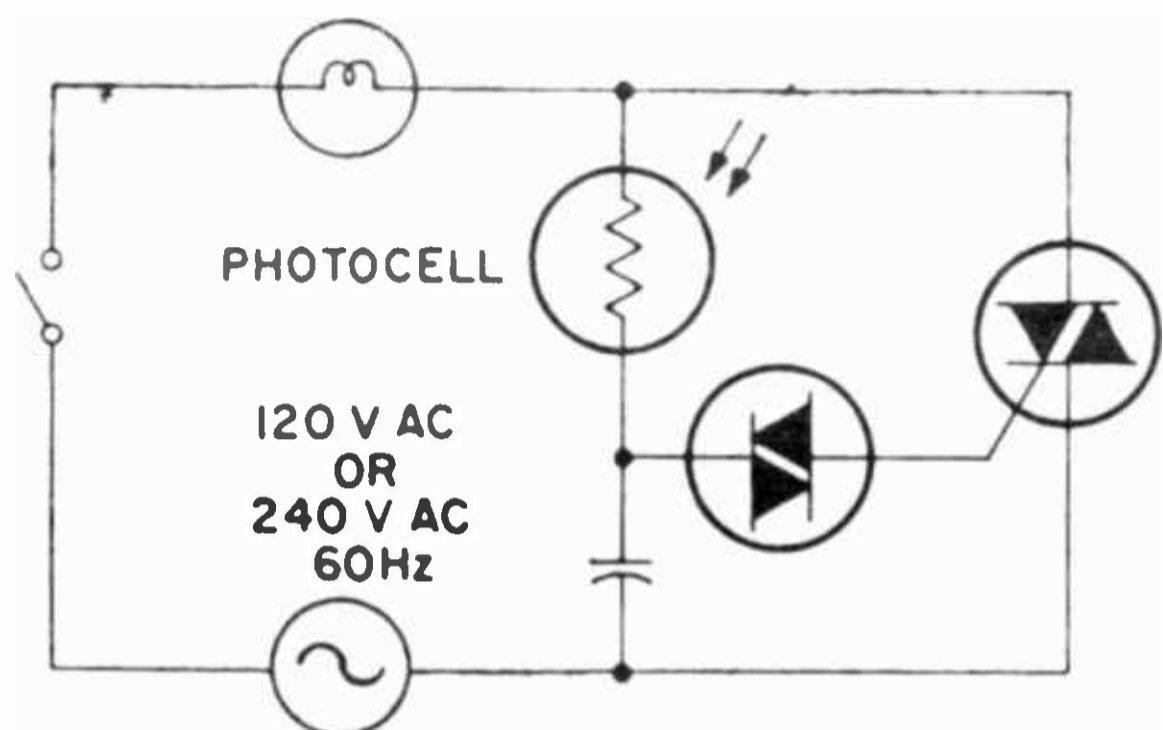


Fig. 269—Light-controlled turn-on circuit.

HEAT CONTROLS

There are three general categories of solid-state control circuits for electric heating elements: on-off control, phase control, and proportional control using integral-cycle synchronous switching. Phase-control circuits such as those used for light dimming are very effective and efficient for electric heat control except for the problem of radio-frequency interference (RFI). In higher-power applications, the RFI is of such magnitude that suppression circuits to minimize the interference become quite bulky and expensive.

An on-off circuit for the control of resistance-heating elements is shown in Fig. 270. The circuit also provides synchronous switching close to the beginning of the zero-voltage crossing of the input voltage to minimize RFI. The thermistor controls the operation of the two-transistor regenerative switch, which, in turn, controls the operation of the triac. When the temperature being controlled is low, the resistance of

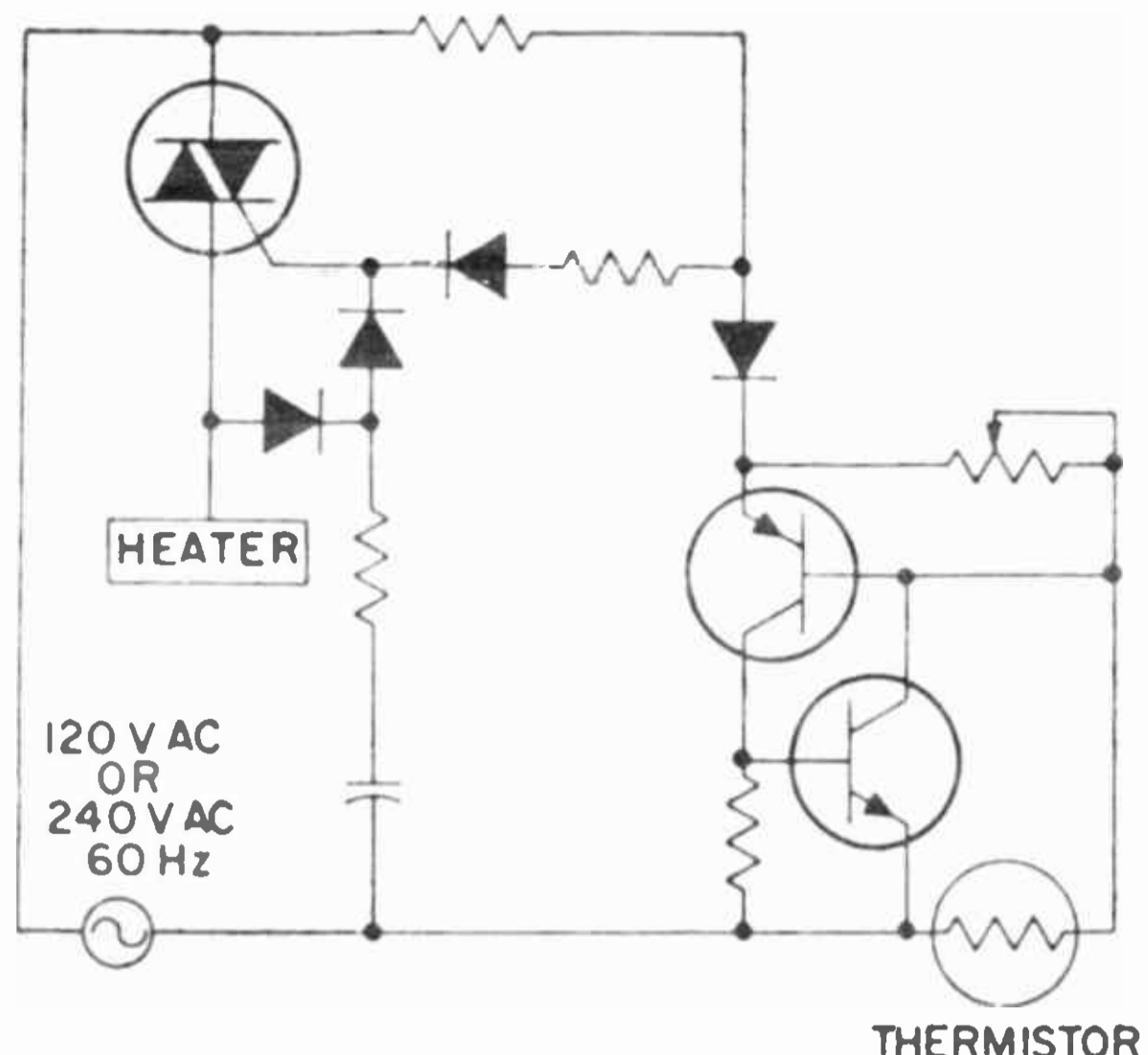


Fig. 270—Synchronous switching on-off heat controller.

the thermistor is high and the regenerative switch is OFF. The triac is then triggered directly from the line on positive half-cycles of the input voltage. When the triac triggers and applies voltage to the load, the capacitor is charged to the peak value of the input voltage. The capacitor discharges through the triac gate to trigger the triac on the opposite half-cycle. The diode-resistor-capacitor “slaving” network triggers the triac on negative half-cycles of the ac input voltage after it is triggered on the positive half-cycle to provide integral cycles of ac power to the load.

When the temperature being controlled reaches the desired value, as determined by the thermistor, the transistor regenerative switch conducts at the beginning of the positive input-voltage cycle to shunt the trigger current away from the triac gate. The triac does not conduct as long as the resistance of the thermistor is low enough to make the transistor regenerative switch turn on before the triac can be triggered.

On-off controls have only two levels of power input to the load. The heating coils are either energized to full power or are at zero power. Because of thermal time constants, on-off controls produce a cyclic action which alternates between thermal overshoots and undershoots with poor resolution.

This disadvantage is overcome and RFI is minimized by use of the concept of integral-cycle proportional control with synchronous switching. In this system, a time base is selected and the on-time of the triac is varied within the time base. The ratio of the on-to-off time of the triac within this time interval depends upon the power required to the heating elements to maintain the desired temperature. Fig. 271 shows the on-off ratio of the triac. Within the time period, the on-time varies by an integral number of cycles from full ON to a single cycle of input voltage.

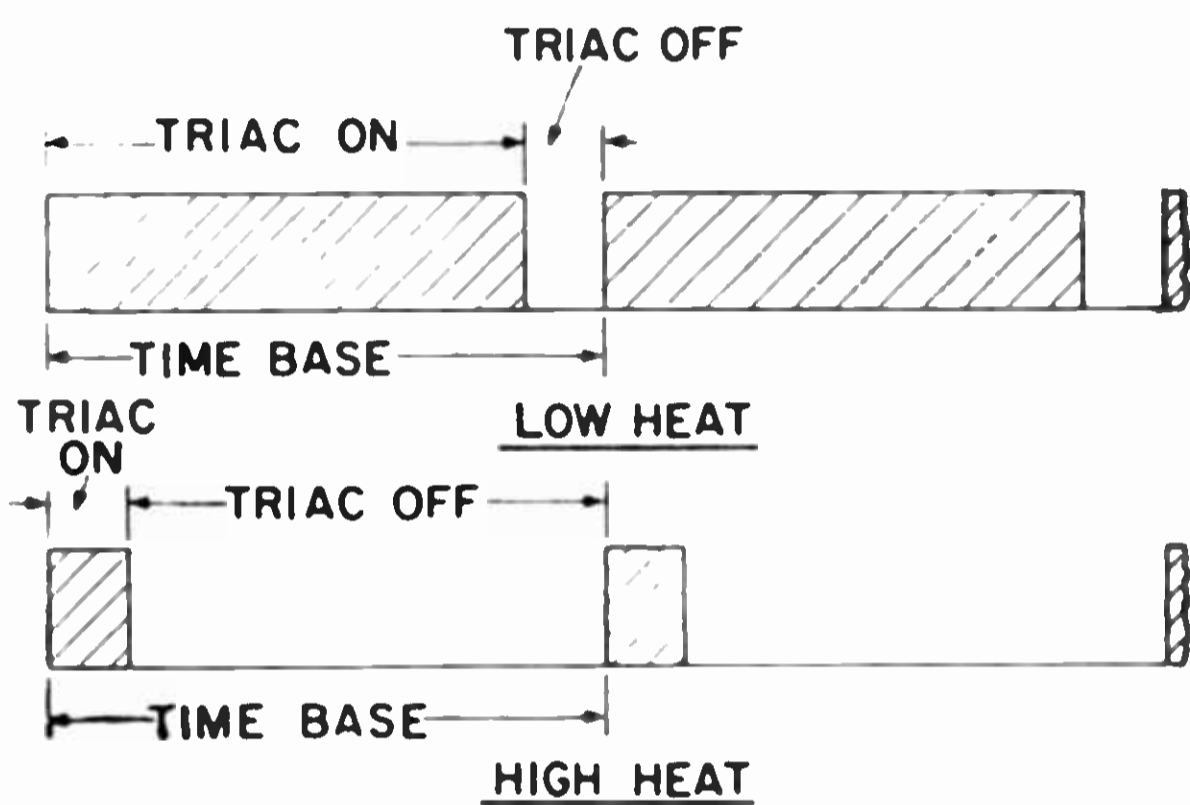


Fig. 271—Triac duty cycle.

One method of achieving integral-cycle proportional control is to use a fixed-frequency sawtooth generator signal which is summed with a dc control signal. The sawtooth generator establishes the period or time base of the system. The dc control signal is obtained from the output of the temperature-sensing network. The principle is illustrated in Fig. 272. As the sawtooth voltage increases, a level is reached which turns on power to the heating elements. As the temperature at the sensor changes, the dc level shifts accordingly and changes the length of time that the power is applied to the heating elements within the established time.

When the demand for heat is high, the dc control signal is high and high power is supplied continuously to the heating elements. When the demand for heat is completely satis-

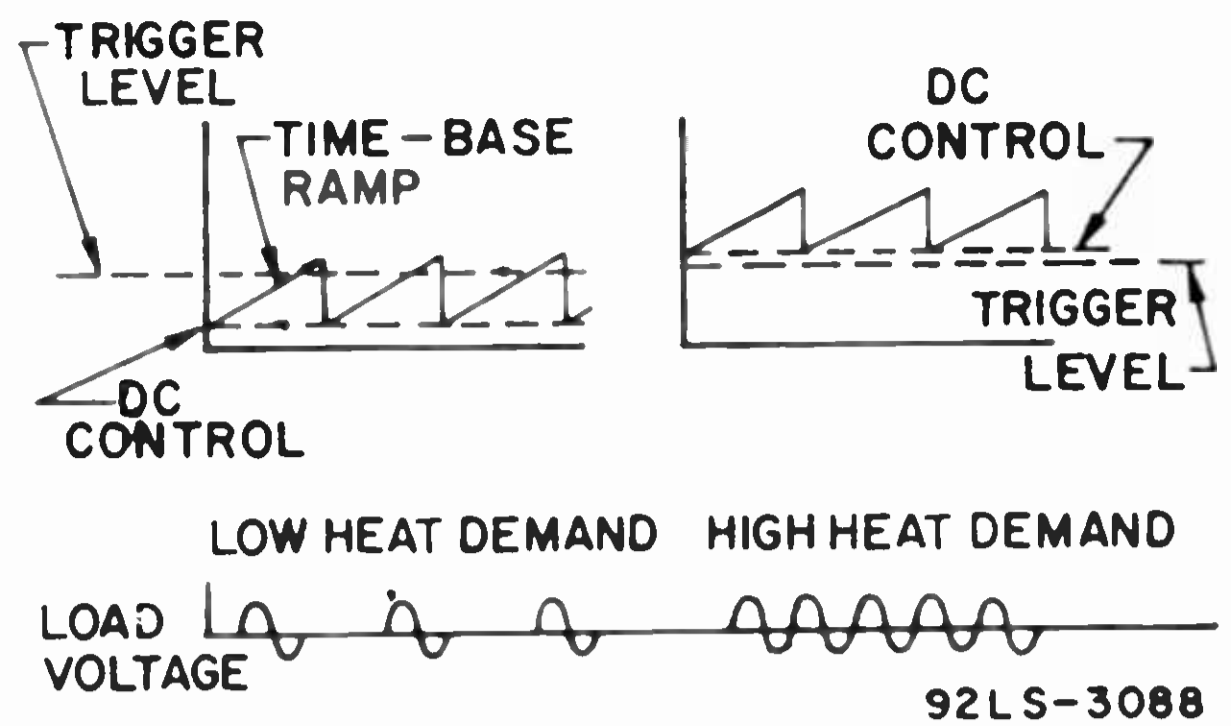


Fig. 272—Proportional-controller wave-shapes.

fied, the dc control signal is low and low power is supplied to the heating elements. Usually a system using this principle operates continuously somewhere between full ON and full OFF to satisfy the demand for heat.

A proportional integral-cycle heat-control system is shown in Fig. 273. The ramp voltage is generated by charging of capacitor C through resistor R. The length of the ramp is determined by the voltage magnitude required to trigger the regenerative switch consisting of Q_1 and Q_2 . The temperature sensor consisting of Q_3 and Q_4 , together with the controlling thermistor R_{11} , establishes a voltage level at the base of Q_3 which depends upon the resistance value of the thermistor. Q_3 and Q_1 form a bistable multivibrator. The state of the multivibrator depends upon the base bias of Q_3 . When Q_3 is conducting, Q_1 is cut off. The pulse generator is energized and generates pulses to trigger the triac. The output of the pulse generator is synchronized to the line voltage on the negative half-cycle by D_2 and R_3 and on the positive half-cycle by D_1 and R_3 . The pulses are, therefore, generated at the zero-voltage crossings and trigger the triacs into conduction at only these points.

MOTOR CONTROLS

Thyristors have been widely accepted in power-control applications in industrial systems. The controls can be designed to provide good per-

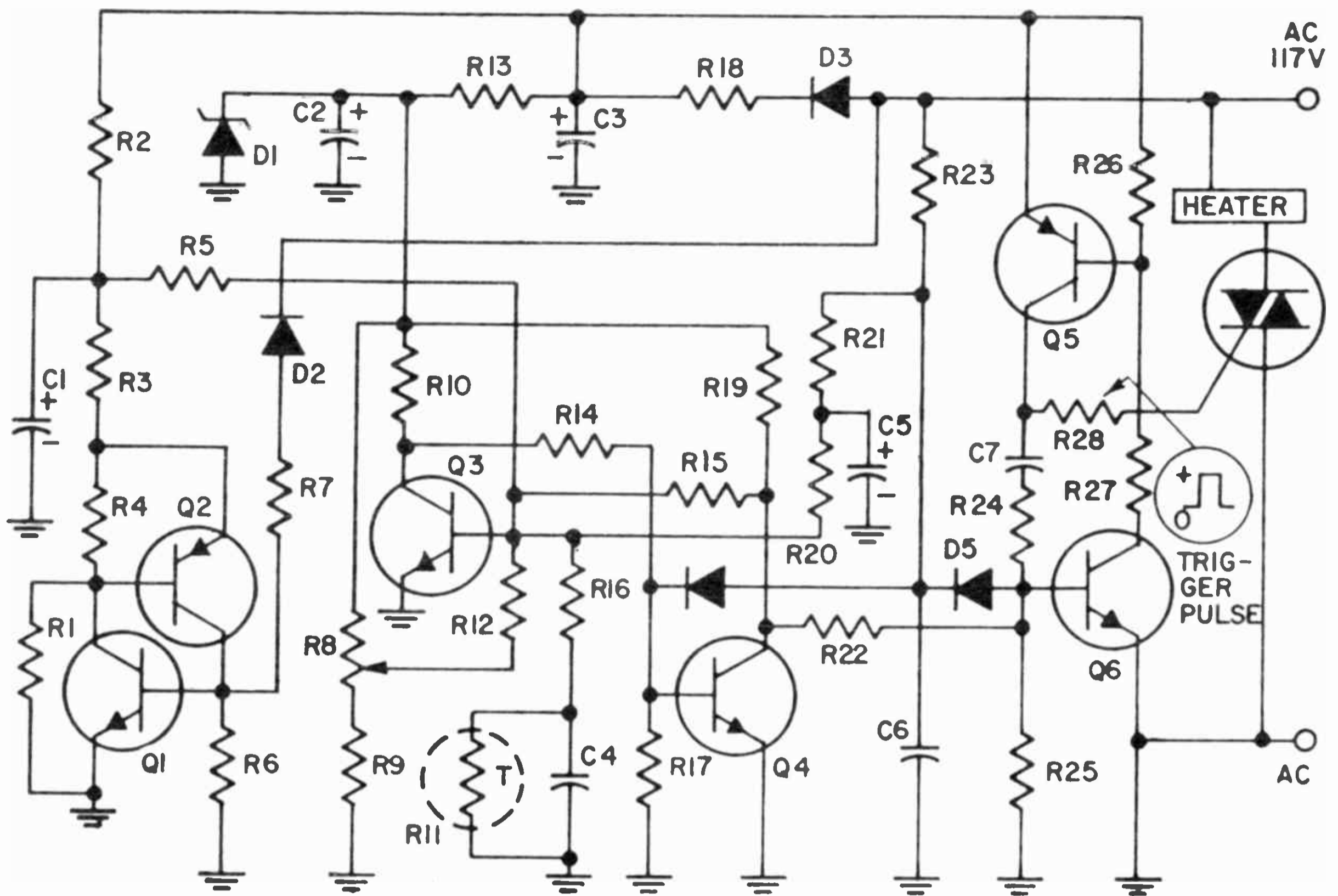


Fig. 273—Proportional integral-cycle heat controller.

formance, maximum efficiency, and high reliability in compact packaging arrangements.

Triacs as well as SCR's can be used very effectively to apply power to motors and perform switching, or any other desired operating condition that can be obtained by a switching action. Because most motors are line-operated, the triac can be used as a direct replacement for electromechanical switches. A very simple triac static switch for control of ac motors is shown in Fig. 274. The low-current switch

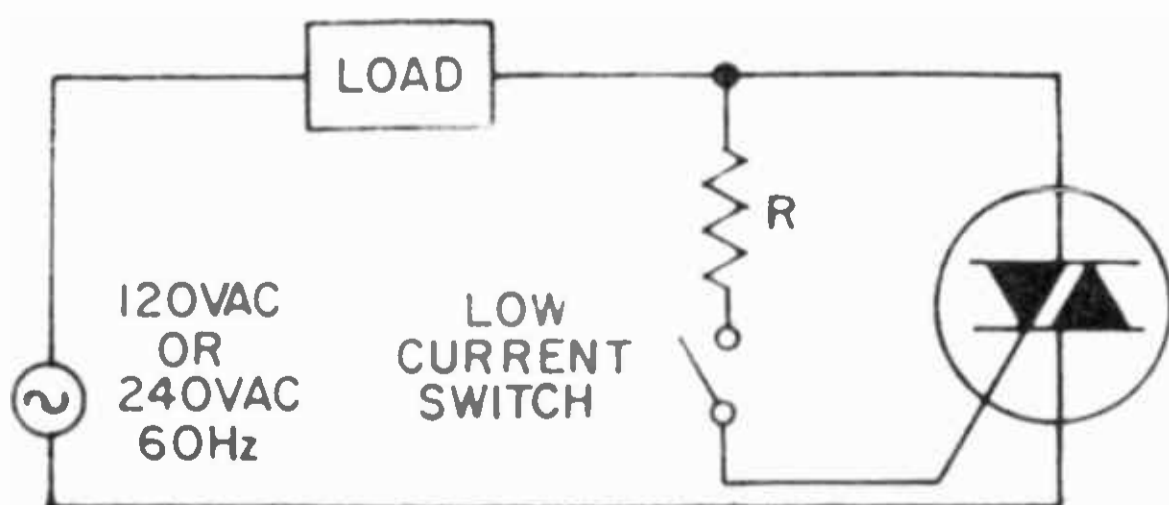


Fig. 274—Simple triac static switch.

controlling the gate trigger current can be any type of transducer, such as a pressure switch, a thermal switch, a photocell, or a magnetic reed relay. This simple type of cir-

cuit allows the motor to be switched directly from the transducer switch without any intermediate power switch or relay.

Triacs can also be used to change the operating characteristics of motors to obtain many different speed and torque curves.

For dc control, the circuit of Fig. 275 can be used. By use of the dc triggering modes, the triac can be directly triggered from transistor

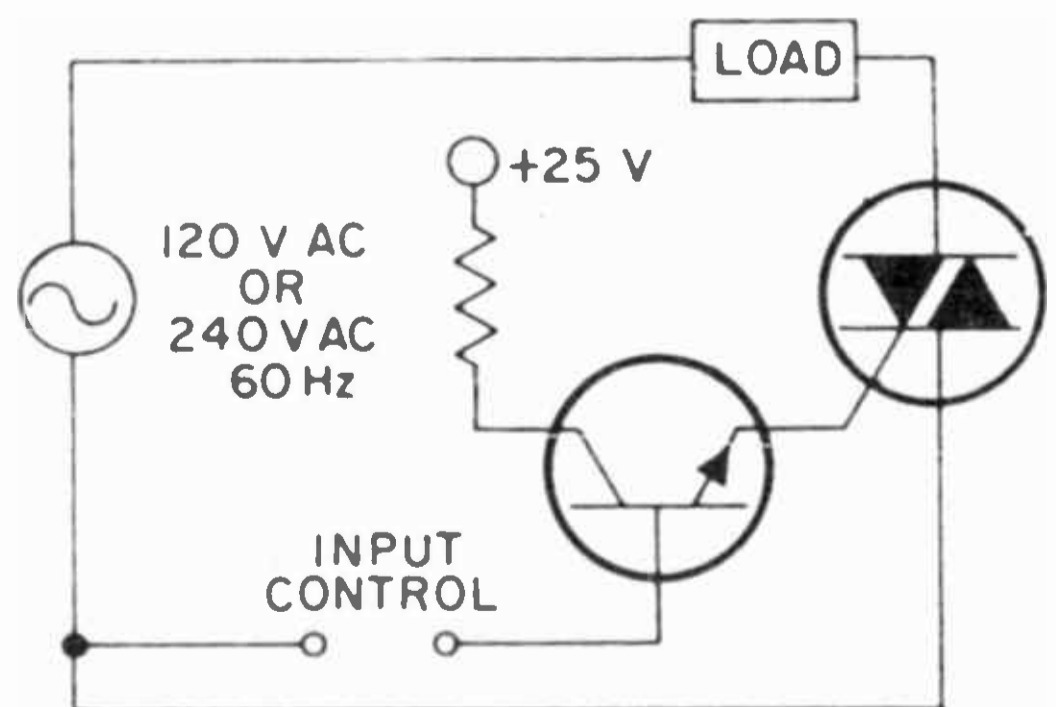


Fig. 275—AC triac switch control from dc input.

cuits by either a pulse or continuous signal. A transistor series-switching regulator approach can also be used to control the armature

current of a dc motor, as shown in Fig. 276. Usually the transistor is full ON or full OFF and the duration of the pulse (or the duty cycle) determines the motor speed. Its typical high-power application is in the drive motors of electric vehicles or submarines.

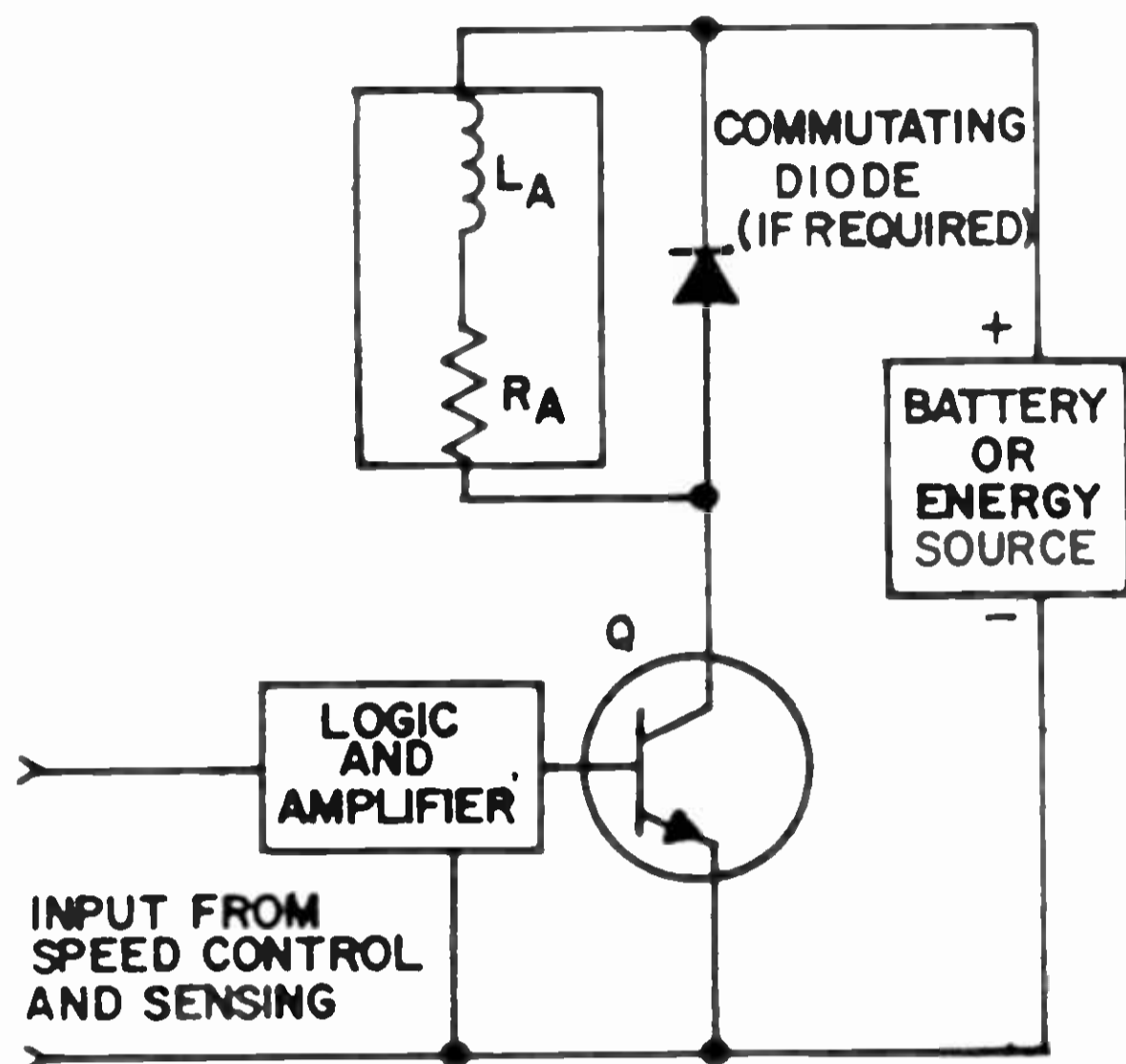


Fig. 276—DC motor armature control.

Many fractional-horsepower motors are series-wound "universal" motors, so named because of their ability to operate directly from either ac or dc power sources. Fig. 277 is a schematic of this type of motor operated from an ac supply. Because most domestic applications today require 60-Hz power, universal motors are usually designed to have

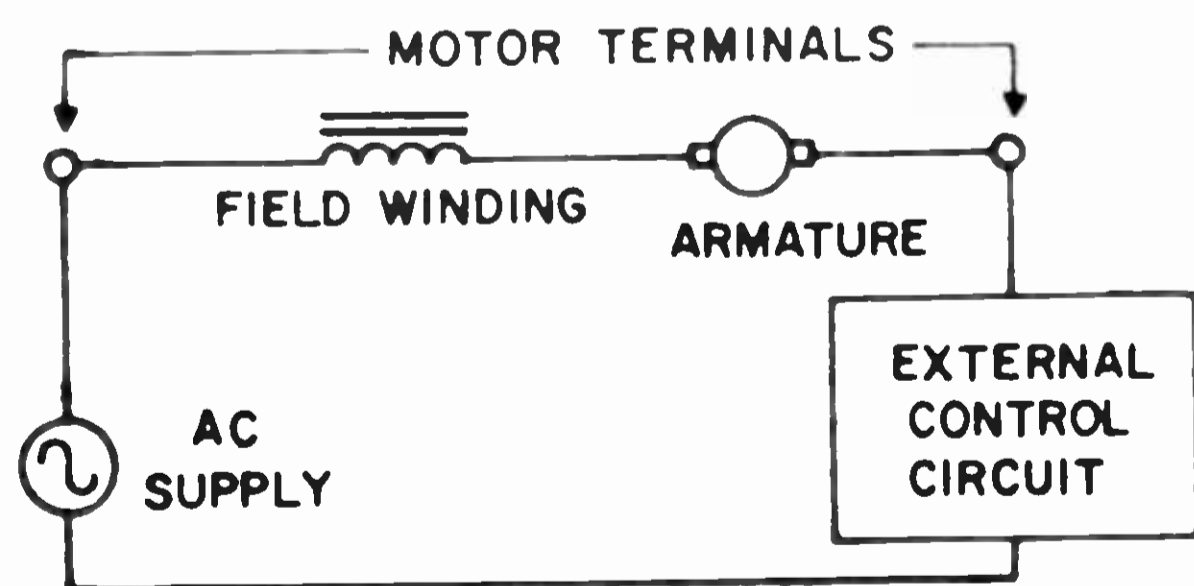


Fig. 277—Series-wound universal motor.

optimum performance characteristics at this frequency. Most universal motors run faster at a given dc voltage than at the same 60-Hz ac voltage.

The field winding of a universal motor, whether distributed or lumped (salient pole), is in series with the armature and external circuit, as shown in Fig. 277. The current

through the field winding produces a magnetic field which cuts across the armature conductors. The action of this field in opposition to the field set up by the armature current subjects the individual conductors to a lateral thrust which results in armature rotation.

AC operation of a universal motor is possible because of the nature of its electrical connections. As the ac source voltage reverses every half-cycle, the magnetic field produced by the field winding reverses its direction simultaneously. Because the armature windings are in series with the field windings through the brushes and commutating segments, the current through the armature winding also reverses. Because both the magnetic field and armature current are reversed, the direction of the lateral thrust on the armature windings remains constant. Typical performance characteristic curves for a universal motor are shown in Fig. 278.

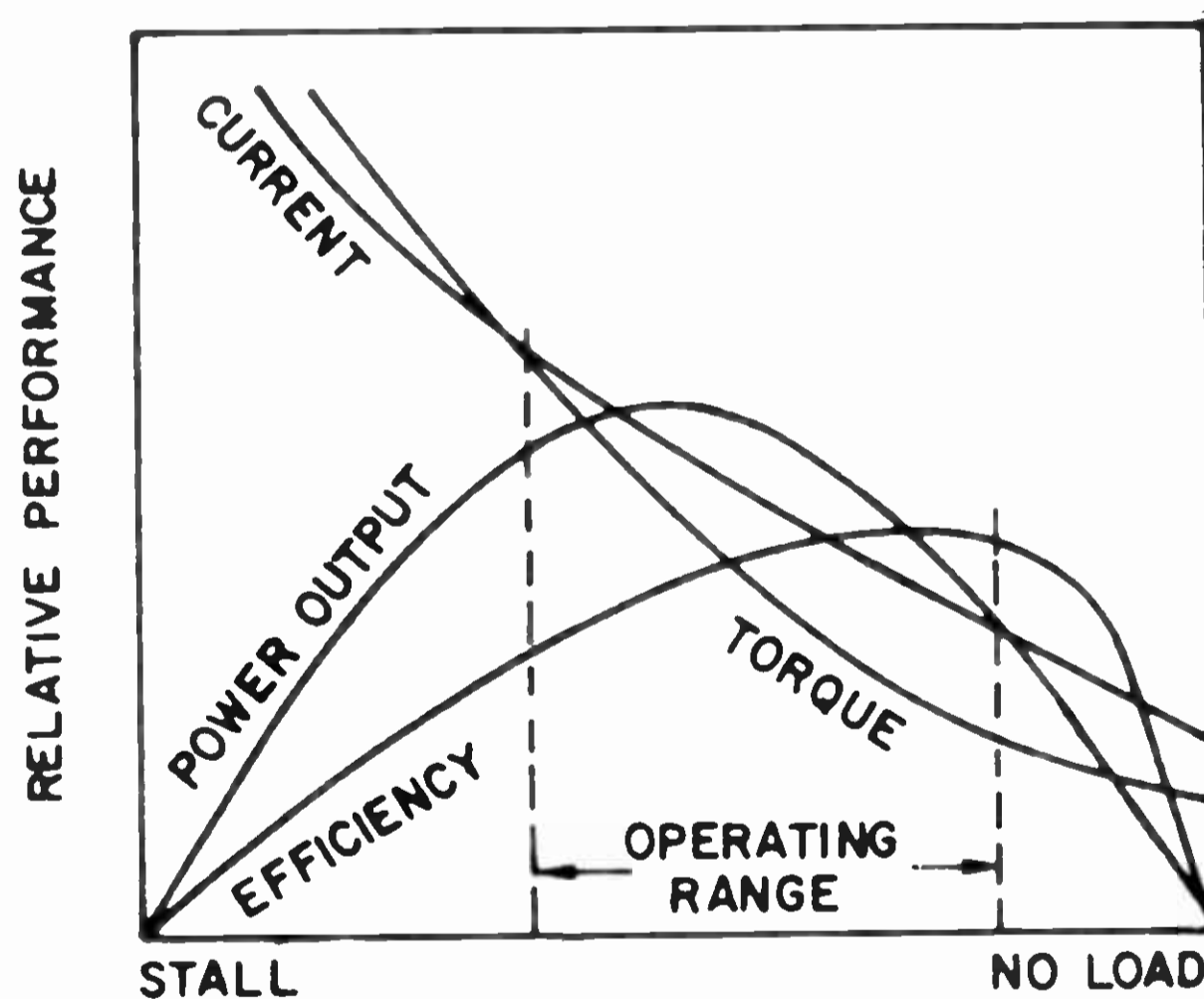


Fig. 278—Typical performance curves for a universal motor.

One of the simplest and most efficient means of varying the impressed voltage to a load on an ac power system is by control of the conduction angle of a thyristor placed in series with the load. Typical curves showing the variation of motor speed with conduction angle for both half-wave and full-wave impressed motor voltages are illustrated in Fig. 279.

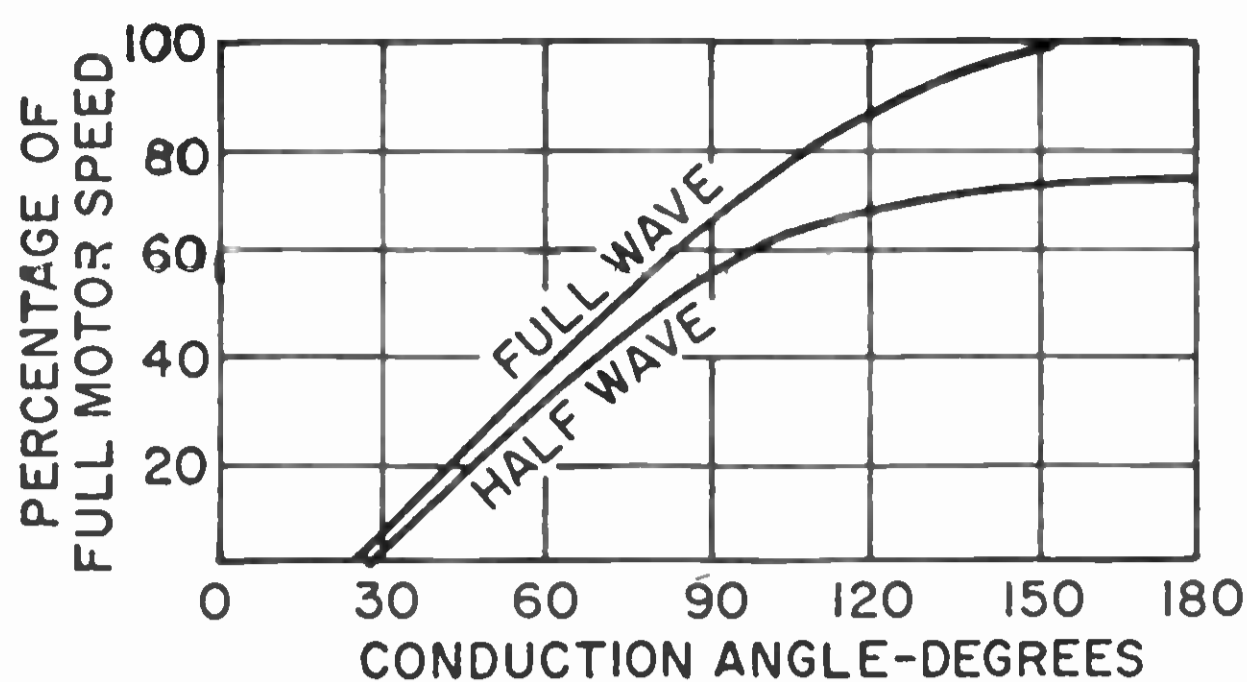


Fig. 279—Typical performance curves for a universal motor with phase-angle control.

Half-Wave Control

There are many good circuits available for half-wave control of universal motors. The circuits are divided into two classes: regulating and non-regulating. Regulation in this instance implies load sensing and compensation of the system to prevent changes in motor speed.

The half-wave proportional control circuit shown in Fig. 280 is a non-regulating circuit that depends upon an RC delay network for gate

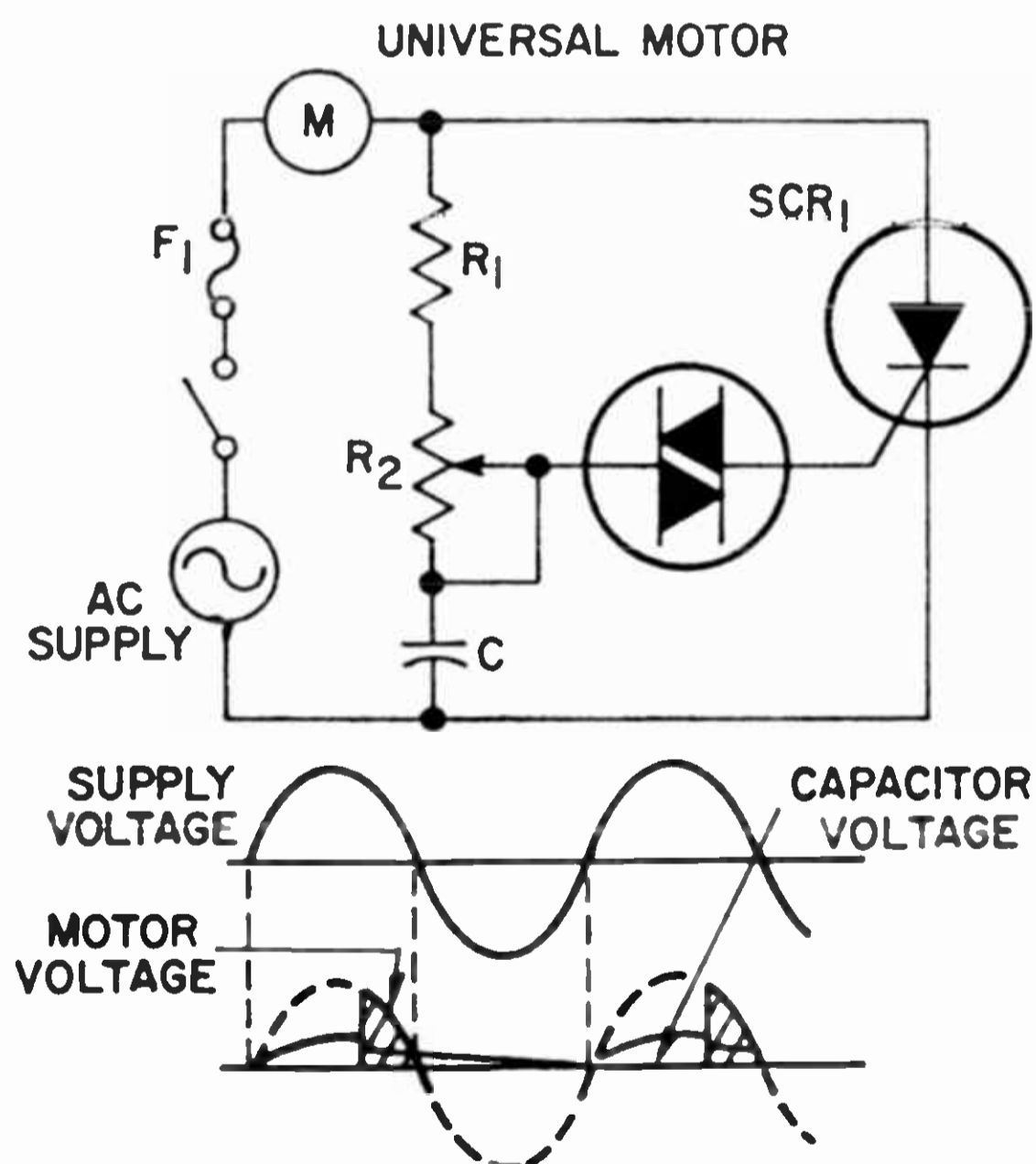


Fig. 280—Half-wave motor control with no regulation.

phase-lag control. This circuit is better than simple resistance firing circuits because the phase-shifting characteristics of the RC network permit the firing of the SCR beyond the peak of the impressed voltage, resulting in small conduction angles and very slow speed.

Fig. 281 shows a fundamental circuit of direct-coupled SCR control with voltage feedback. This circuit is highly effective for speed control of universal motors. The circuit makes use of the counter emf induced in the rotating armature because of the residual magnetism in the motor on the half-cycle when the SCR is blocking.

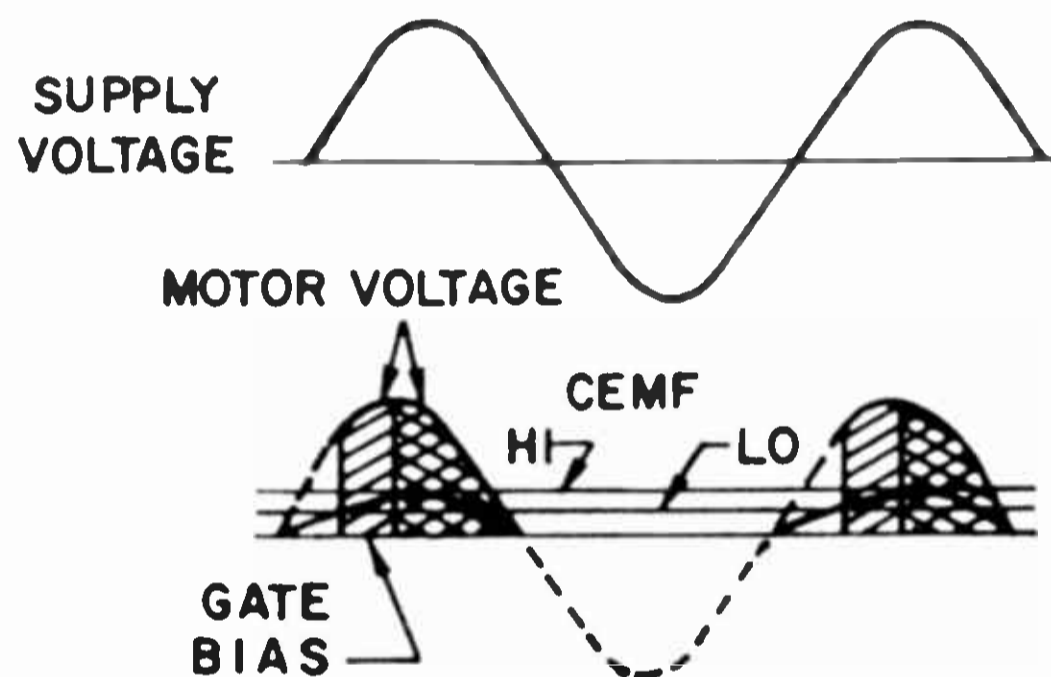
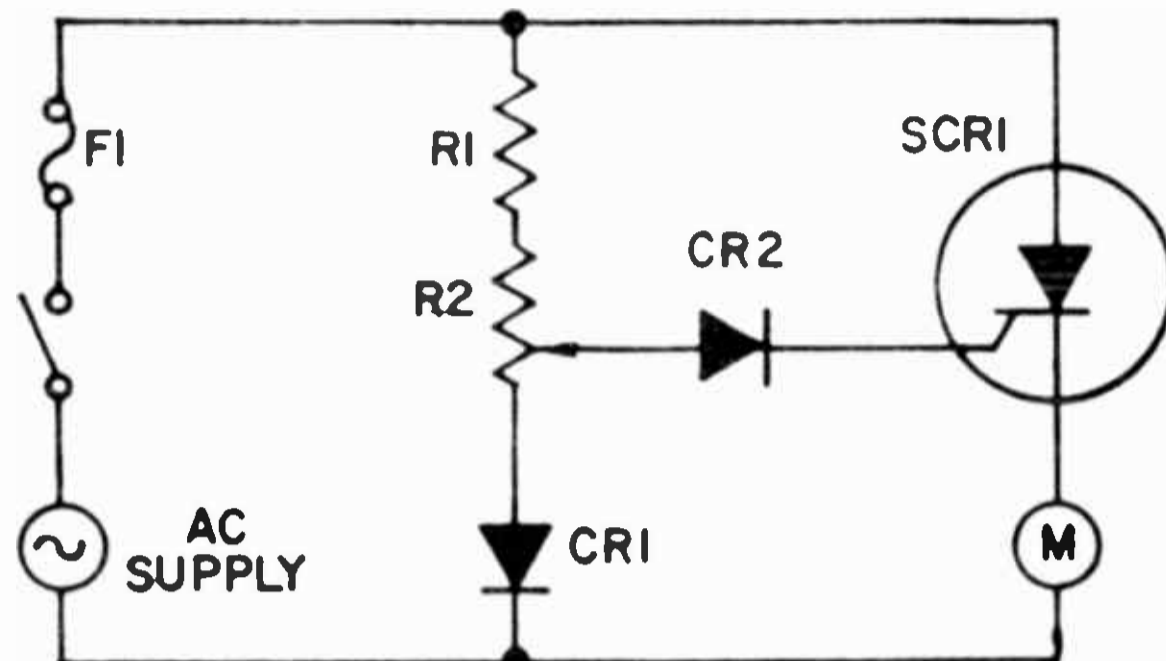


Fig. 281—Half-wave motor control with regulation.

The counter emf is a function of speed and, therefore, can be used as an indication of speed changes as mechanical load varies. The gate-firing circuit is a resistance network consisting of R_1 and R_2 . During the positive half-cycle of the source voltage, a fraction of the voltage is developed at the center-tap of the potentiometer and is compared with the counter emf developed in the rotating armature of the motor. When the bias developed at the gate of the SCR from the potentiometer exceeds the counter emf of the motor, the SCR fires. AC power is then applied to the motor for the remaining portion of the positive half-cycle. Speed control is accomplished by adjustment of potentiometer R_1 . If the SCR is fired early in the cycle, the motor operates at high speed because essen-

tially the full rated line voltage is applied to the motor. If the SCR is fired later in the cycle, the average value of voltage applied to the motor is reduced, and a corresponding reduction in motor speed occurs. On the negative half-cycle, the SCR blocks voltage to the motor. The voltage applied to the gate of the SCR is a sine wave because it is derived from the sine-wave line voltage. The minimum conduction angle occurs at the peak of the sine wave and is restricted to 90 degrees. Increasing conduction angles occur when the gate bias to the SCR is increased to allow firing at voltage values which are less than the peak value.

When a load is applied to the motor, the motor speed decreases and thus reduces the counter emf induced in the rotating armature. With a reduced counter emf, the SCR fires earlier in the cycle and provides increased motor torque to the load. Fig. 281 also shows variations of conduction angle with changes in counter emf. The counter emf appears as a constant voltage at the motor terminals when the SCR is blocking.

Fig. 282 shows the circuit that provides feedback for changing load conditions to minimize changes in motor speed. The feedback is provided by R_7 , which is in series with the motor. A voltage proportional to the peak current through the motor is developed across the resistor. This voltage is stored on capacitor C_2 through diode CR_2 , and is of a polarity that causes the bias on the resistance network of R_3 and R_4 to change in accordance with the load on the motor. With an increasing motor load, the speed tends to decrease. This decrease in motor speed causes more current to flow through the motor armature and field windings. When the current flowing through R_7 increases, the voltage stored on capacitor C_2 increases in the positive direction. This increase in capacitor voltage causes the transistors to conduct earlier in the cycle, to fire the SCR, and to provide a greater portion of the power cycle to the motor. With a decreasing load, the motor current decreases and the voltage stored by capacitor C_2 decreases. The transistors and SCR then conduct later in the cycle. The resultant reduction in the average

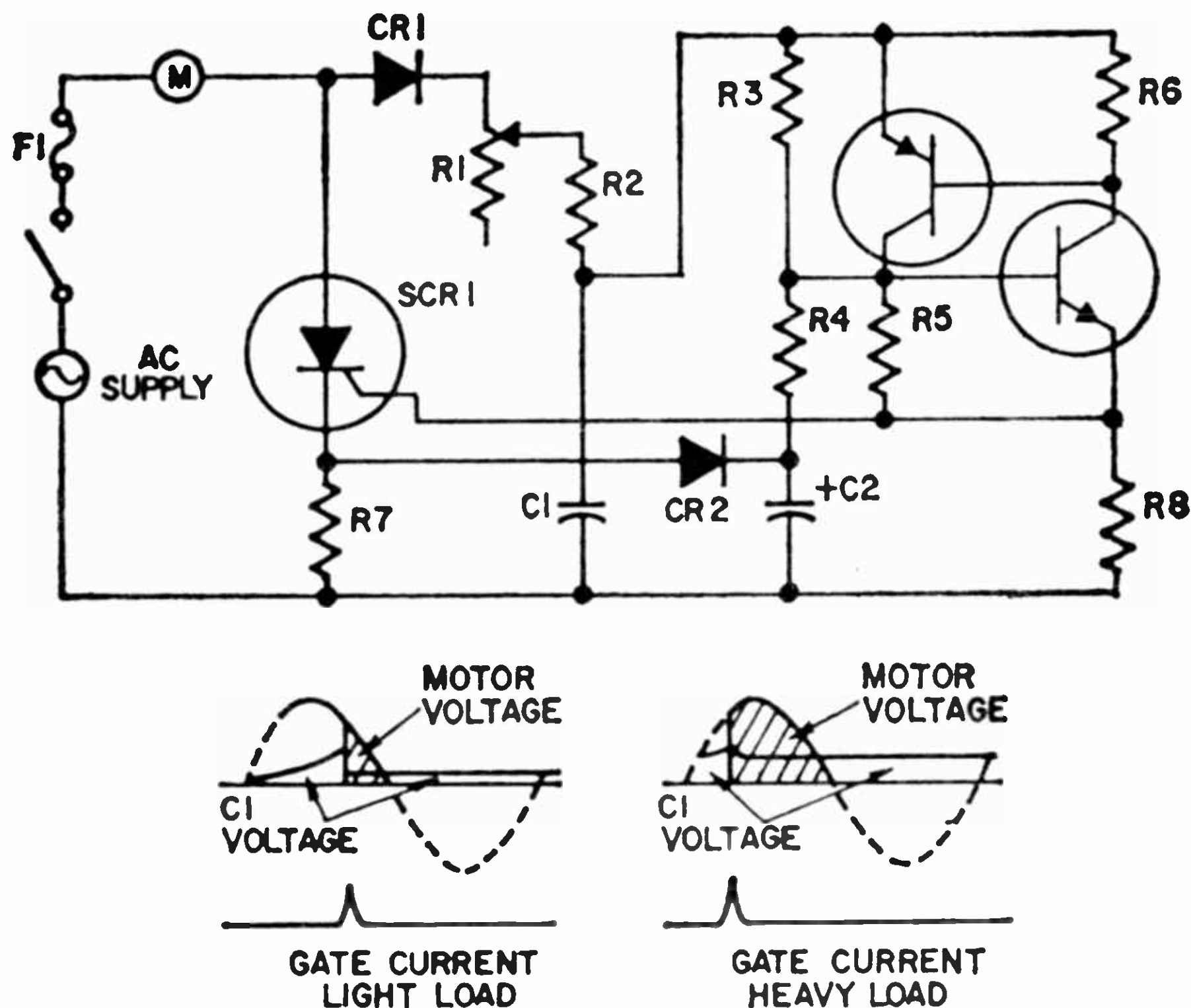


Fig. 282—Half-wave motor control using two-transistor regenerative triggering with regulation.

power supplied to the motor causes a reduced torque to the smaller load. Because motor current is a function of the motor itself, resistor R_r has to be matched with the motor rating to provide optimum feedback for load compensation. Resistor R_r may range from 0.1 ohm for larger-size universal motors to 1.0 ohm for smaller types.

Half-Wave Motor Control Limitations

If a universal motor is operated at low speed under a heavy mechanical load, it may stall and cause heavy current flow through the SCR. For this reason, low-speed heavy-load conditions should be allowed to exist for only a few seconds to prevent possible circuit damage. In any case, fuse ratings should be carefully determined and observed.

Nameplate data for some universal motors are given in developed horsepower to the load. This mechanical designation can be converted into its electrical current equivalent through the following procedure.

Internal motor losses are taken into consideration by assigning a figure of merit. This figure, 0.5, represents motor operation at 50-percent efficiency, and indicates that the power input to the motor is twice the power delivered to the load. With this figure of merit and the input voltage V_{ac} , the rms input current to the motor can be calculated as follows:

$$\text{rms current} = \frac{\text{mechanical horsepower} \times 746}{0.5 V_{ac}}$$

For an input voltage of 120 volts, the rms input current becomes

$$\text{rms current} = \text{horsepower} \times 12.4$$

For an input voltage of 240 volts, the rms input current becomes

$$\text{rms current} = \text{horsepower} \times 6.2$$

The motor-control circuits described above should not be used with universal motors that have calculated rms current exceeding the values given. The circuits will ac-

commodate universal motors with ratings up to $\frac{3}{4}$ horsepower at 120 volts input and up to $1\frac{1}{2}$ horsepower at 240 volts input.

Full-Wave Universal and Induction Motor Controls

Fig. 283 shows a single-time-constant full-wave triac circuit which can be used as a satisfactory proportional speed control for universal motors and with certain types

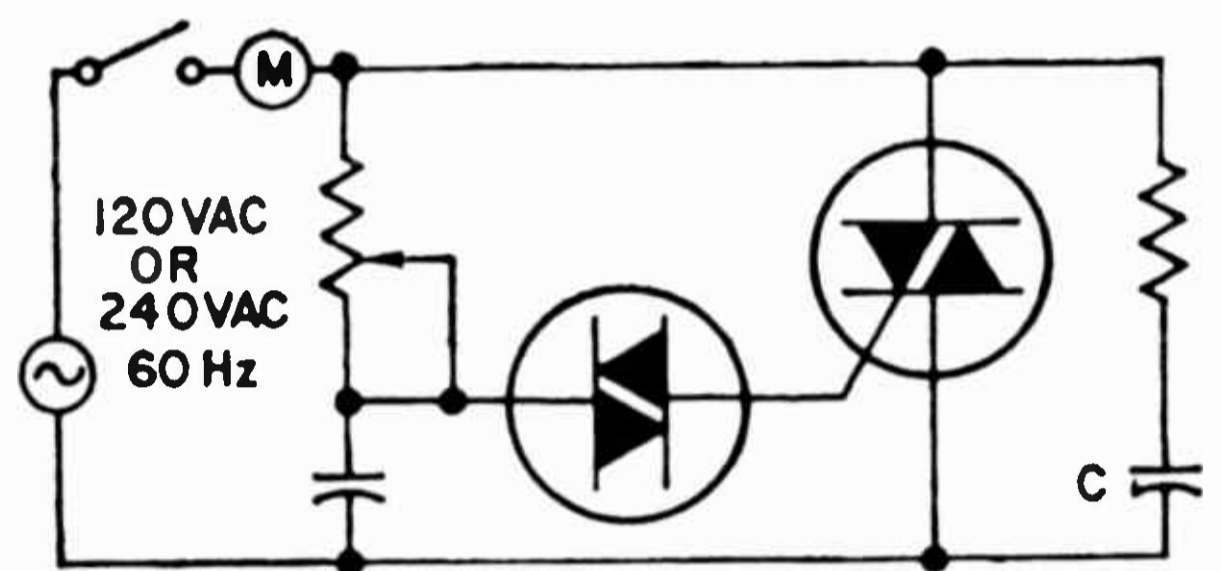


Fig. 283—Induction motor control.

of induction motors, such as shaded pole or permanent split-capacitor motors when the load is fixed. No regulation is provided with this circuit. This type of circuit is best suited to applications which require speed control in the medium to full-power range. It is specifically useful in applications such as fans or blower-motor controls, where a small change in motor speed produces a large change in air velocity. Caution must be exercised if this type of circuit is used with induction motors because the motor may stall suddenly if the speed of the motor is reduced below the drop-out speed for the specific operating condition determined by the conduction angle of the triac. Because the single-time-constant circuit cannot provide speed control of an induction motor load from maximum power to full OFF, but only down to some fraction of the full-power speed, the effects of hysteresis described previously are not present. Speed ratios as high as 3:1 can be obtained from the single-time-constant circuit used with certain types of induction motors. Care must be

taken to avoid continuous low-speed operation of induction motors in which sleeve bearings are used as improper lubrication will result.

Because motors are basically inductive loads and because the triac turns off when the current reduces to zero, the phase difference between the applied voltage and the device current causes the triac to turn off when the source voltage is at a value other than zero. When the triac turns off, the instantaneous value of input voltage is applied directly to the main terminals of the triac. This commutating voltage may have a rate of rise which can re-trigger the triac. The commutating dv/dt can be limited to the capability of the triac by use of an RC network across the device, as shown in Fig. 283. The current and voltage waveshapes for the circuit are shown in Fig. 284 to illustrate the principle of commutating dv/dt .

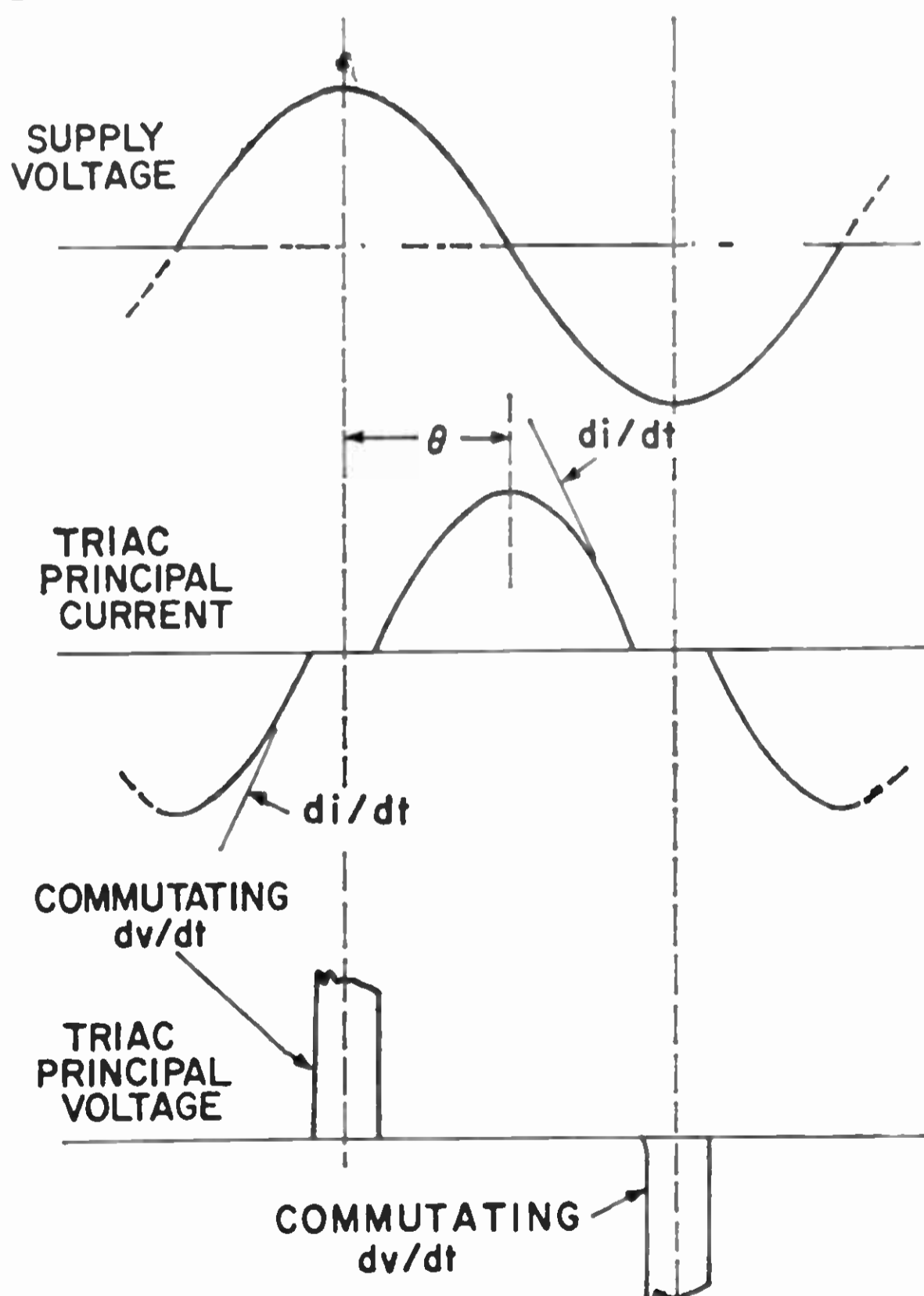


Fig. 284—Waveshapes of commutating dv/dt characteristics.

In applications in which the hysteresis effect can be tolerated or which require speed control primarily in the medium to full-power range, a single-time-constant circuit such as that shown in Fig. 283

for induction motors can also be used for universal motors. However, it is usually desirable to extend the range of speed control from full-power ON to very low conduction angles. The double-time-constant circuit shown in Fig. 285 provides the delay necessary to trigger the triac at very low conduction angles with a minimum of hysteresis, and

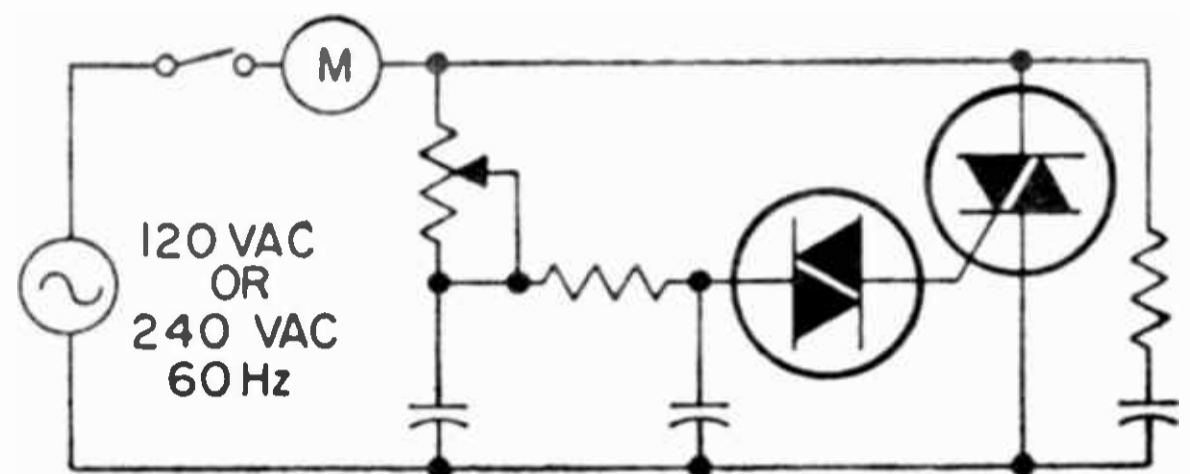


Fig. 285—Double-time-constant motor control.

also provides practically full power to the load at the minimum-resistance position of the control potentiometer. When this type of control circuit is used, an infinite range of motor speeds can be obtained from very low to full-power speeds.

Reversing Motor Control

In many industrial applications, it is necessary to reverse the direction of a motor, either manually or by means of an auxiliary circuit. Fig. 286 shows a circuit which uses two triacs to provide this type of reversing motor control for a split-

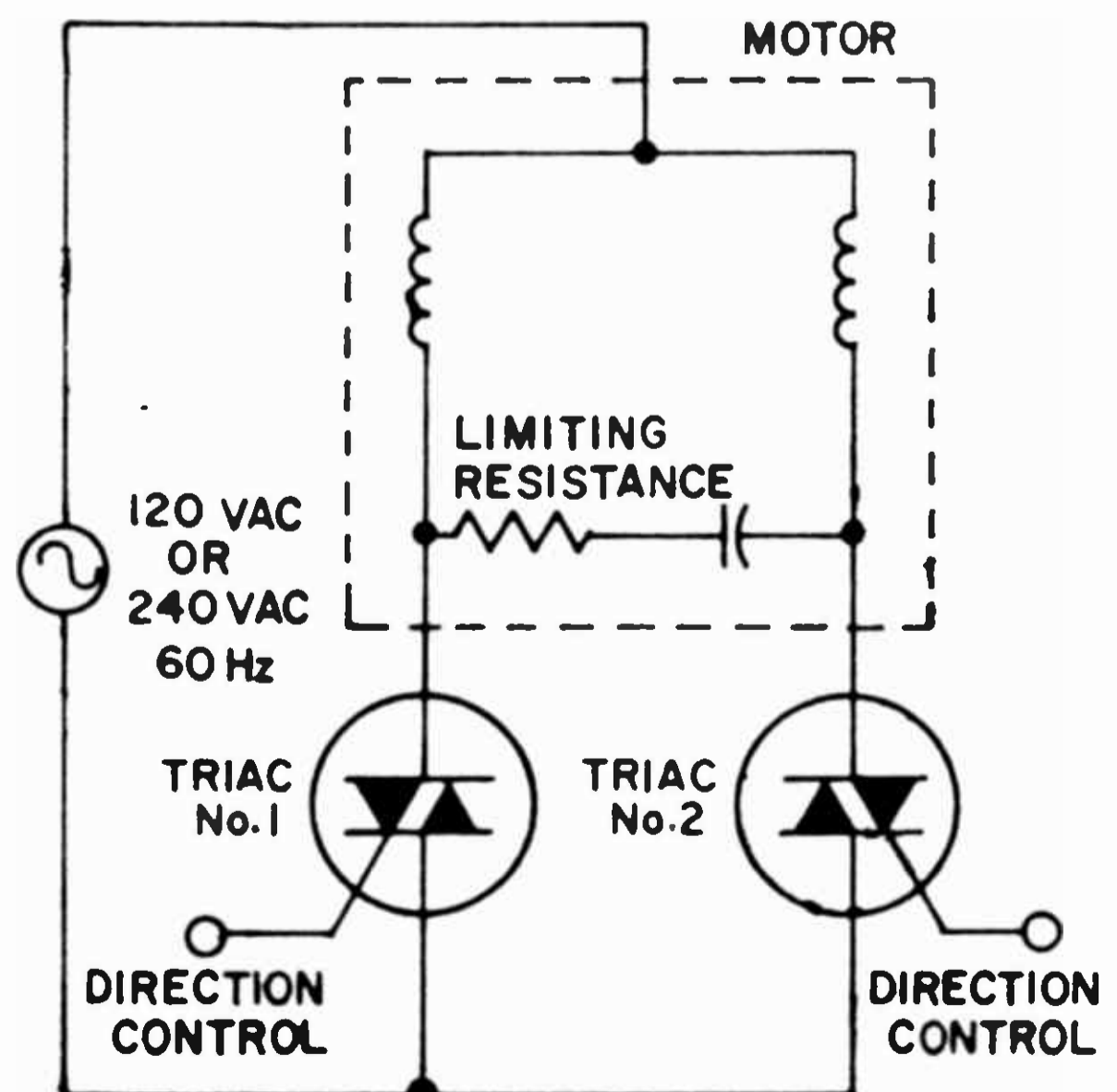


Fig. 286—Reversing motor control.

phase capacitance motor. The reversing switch can be either a manual switch or an electronic switch used with some type of sensor to reverse the direction of the motor. A resistance is added in series with the capacitor to limit capacitor discharge current to a safe value whenever both triacs are conducting simultaneously. If triac No.1 is turned on while triac No.2 is on, a loop current resulting from capacitor discharge will occur and may damage the triacs.

The circuit operates as follows: when triac No.1 is in the off state, motor direction is controlled by triac No.2; when triac No.2 reverts to the off state and triac No.1 turns on, the motor direction is reversed.

The triac motor-reversing circuit can be extended to electronic garage-door systems which use the principle for garage-door direction control. The system contains a transmitter and a receiver and provides remote control of door opening and closing. The block diagram in Fig. 287 shows the functions required for a complete solid-state system. When the garage door is closed, the gate drive to the DOWN triac is disabled by the lower-limit closure and the gate drive to the UP triac is inactive because of the state of the flip-flop. If the transmitter is momentarily keyed, the receiver activates the time-delay monostable multivibrator so that it then changes the flip-flop state and provides continuous gate drive to the UP triac. The door then continues to travel in the UP direction until

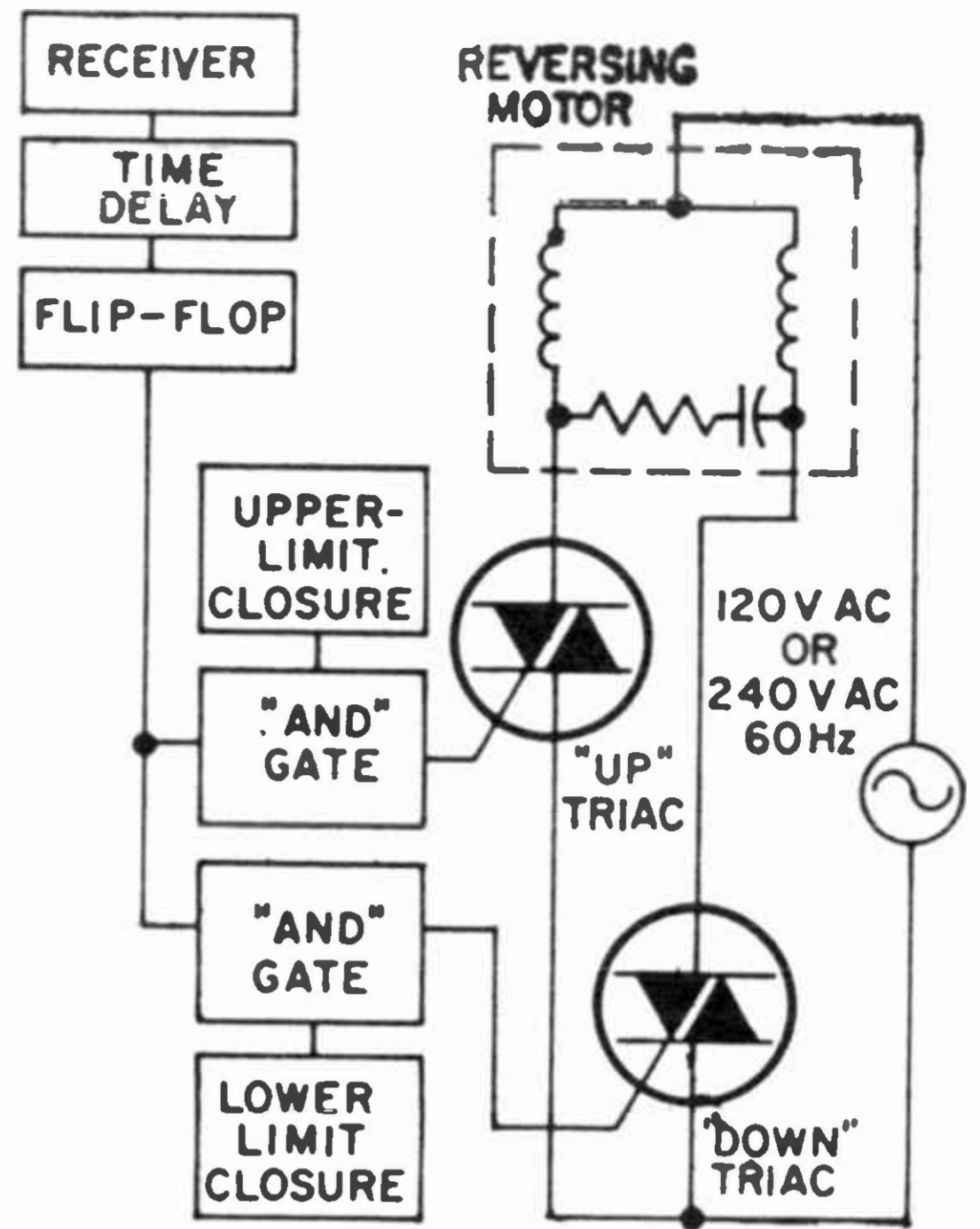


Fig. 287—Block diagram for remote-control solid-state garage-door system.

the upper-limit switch closure disables gate drive to the UP triac. A second keying of the transmitter provides the DOWN triac with gate drive and causes the door to travel in the DOWN direction until the gate drive is disabled by the lower limit closure. The time in which the monostable multivibrator is active should override normal transmitter keying for the purpose of eliminating erroneous firing. A feature of this system is that, during travel, transmitter keying provides motor reversing independent of the upper- or lower-limit closures. Additional features, such as obstacle clearance, manual control, or time delay for overhead garage lights can be included very economically.

Computer Circuits

Basically, a computer system is designed to evaluate information supplied to it in such a way that a predetermined output is obtained for prescribed input conditions. This evaluation is performed in digital computers by switching circuits (also called logic circuits or "gates") which provide a binary output ("1" or "0"). Various types of logic circuits can be combined in large quantity to perform complicated analytical functions at very high speed.

Most computer circuits make use of digital integrated circuits in construction because computer-circuit requirements in terms of tolerances, voltages, types of components, repetitive use of the same circuit, small size, and need for high reliability are consistent with integrated-circuit technology. For this reason, the following section should be considered as demonstrating a possible use of the semiconductor devices included, rather than as describing an application in which these devices are currently, commercially used.

LOGIC CIRCUITS

A switching circuit in which the semiconductor device operates as an effective open or short circuit is called a "gate". Switching circuits are used extensively in computer applications to provide a variety of functions, such as circuit triggering at prescribed intervals, and level and waveshape control. In computer applications, these circuits are called logic circuits. Logic circuits include OR, AND, NOR (NOT-OR), NAND

(NOT-AND), series (clamping), and shunt or inhibitor circuits.

An OR gate has more than one input, but only one output. It provides a prescribed output condition when one or another prescribed input condition exists. When a pulse of the proper polarity is applied at one or more of the inputs to an OR gate, an output pulse of the same polarity is obtained. If the circuit provides phase inversion of the input signal, the OR gate becomes a NOT-OR (NOR) gate. Fig. 288 shows a simple NOR gate that uses diode inputs.

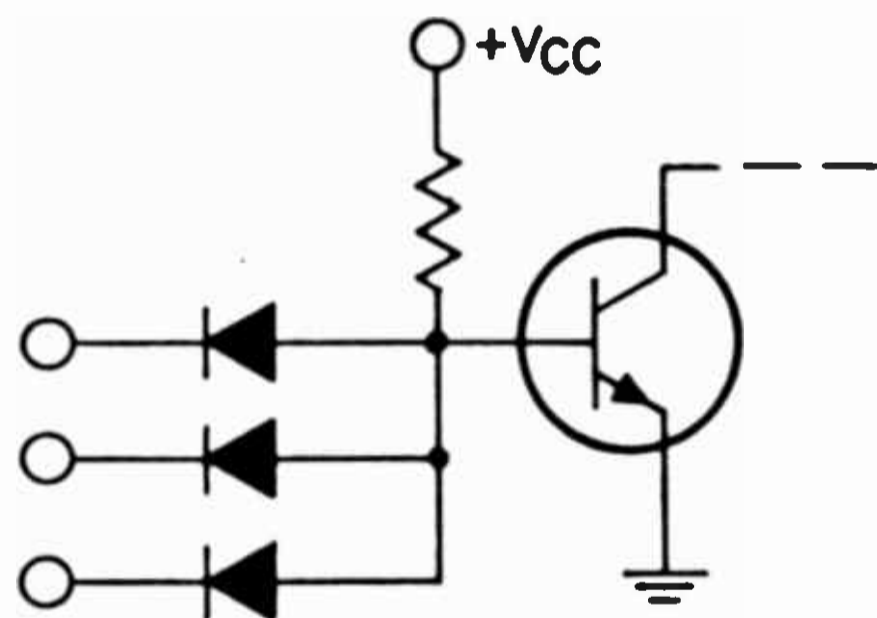


Fig. 288—Simple diode NOR gate.

Fig. 289 shows a transistor NOR gate in which bias is provided by the battery V_{BB} . The bias value is chosen so that the transistor is cut off when all inputs are low and is turned

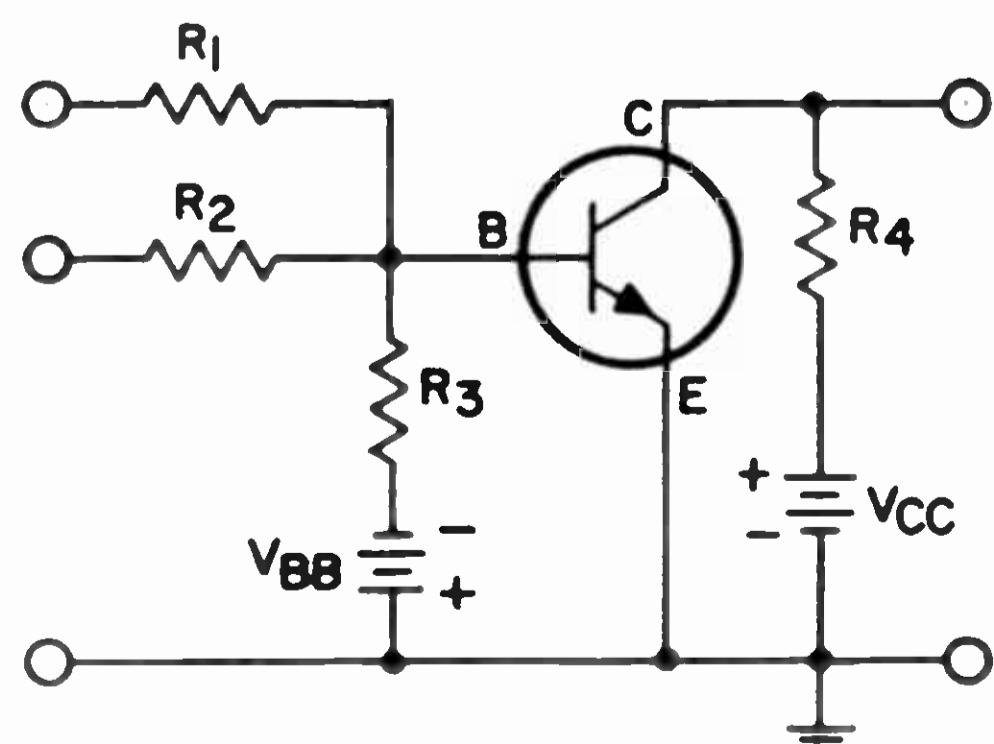


Fig. 289—Simple transistor NOR gate.

on and saturated when either or both of the inputs are high.

An AND gate also has more than one input, but only one output. However, it provides an output only when all the inputs are applied simultaneously. As in the case of the OR gate, the use of a configuration which provides phase inversion provides a NOT-AND (NAND) gate.

The AND-OR gate shown in Fig. 290 illustrates the use of a direct-coupled transistor logic circuit to trigger a bistable multivibrator. The

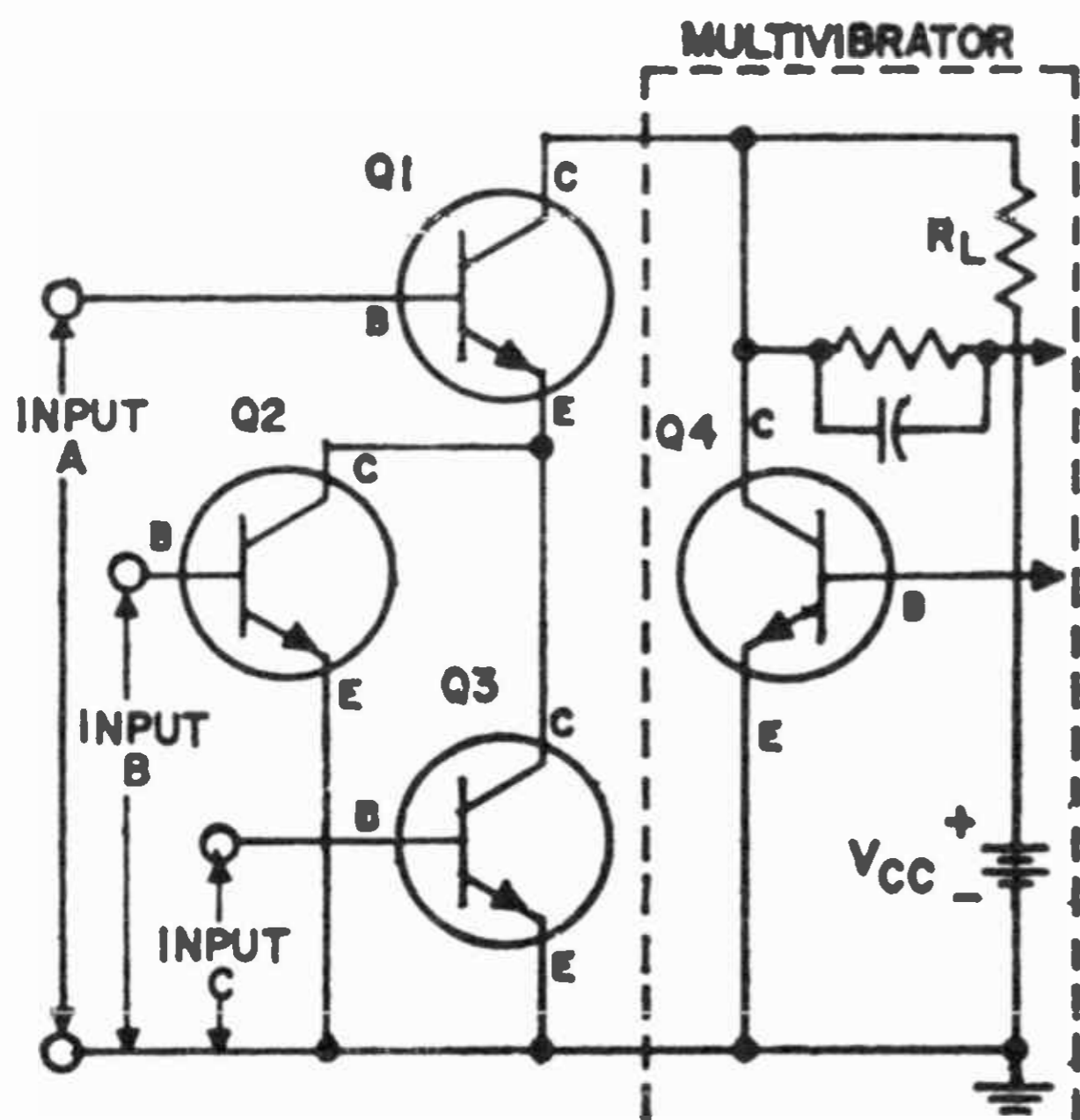


Fig. 290—AND-OR gate or trigger circuit.

over-all gating function, which consists of a NAND function and a NOR function, is performed by transistors Q_1 , Q_2 , and Q_3 . Transistor Q_4 is part of the bistable multivibrator.

Transistors Q_1 and Q_2 are series-connected and form a NAND gate. Similarly, transistors Q_1 and Q_3 are series-connected and form a NAND gate. Transistors Q_2 and Q_3 are parallel-connected and form a NOR gate. Provided all transistors are cut off (quiescent condition), triggering of the bistable multivibrator is accomplished when the prescribed input conditions for either of the NAND gates are met, i.e., when either transistors Q_1 and Q_2 or transistors Q_1 and Q_3 are triggered into conduction.

Gating circuits are also used as amplitude discriminators (limiters),

clippers, and clamping circuits, and as signal-shunting or transmission gates.

Enhancement-type MOS transistors are well suited for digital-type logic-circuit applications because direct-coupled signal inversion is possible without the need for level shifting between stages. An important consideration for MOS logic circuits is the relationship between the saturation voltage $V_D(\text{sat})$ and the threshold voltage V_{TH} of the transistor. For direct coupling, $V_D(\text{sat})$ must be smaller than V_{TH} . It is relatively easy to design enhancement-type MOS transistors which meet this requirement.

Fig. 291 shows a simple NOR logic gate consisting of two MOS transistors and a single load resistor. The inputs X and Y are considered to be LOW if the voltage is less than V_{TH} , and HIGH if the voltage

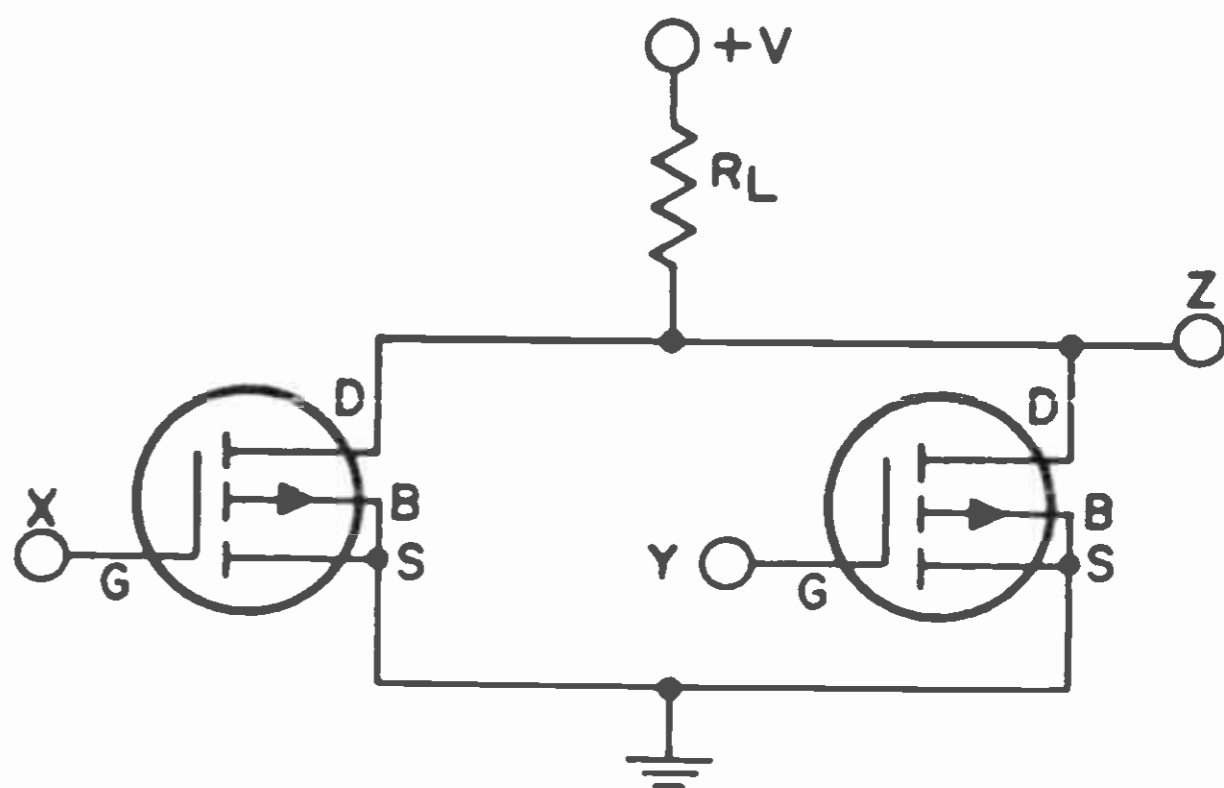


Fig. 291—Simple NOR logic gate using MOS transistors.

is greater than V_{TH} . If both inputs are LOW, both MOS transistors are cut off and the output voltage is HIGH (essentially the supply voltage V) because there is negligible current in the load resistor R_L . If either or both inputs are HIGH, the current produced causes the output voltage to drop to the level of $V_D(\text{sat})$, and the output is LOW. If a binary "1" is assigned to the HIGH level and a binary "0" to the LOW level, the gate performs the NOR function.

As a two-terminal switch, the tunnel diode is particularly suited to computer applications because of its

high speed, small size, and low power consumption. Switching operation is obtained by use of a load line which intersects the diode characteristic in three points, as shown in Fig. 292; however, only points C and E are stable operating points. If the circuit is operated at point C and a

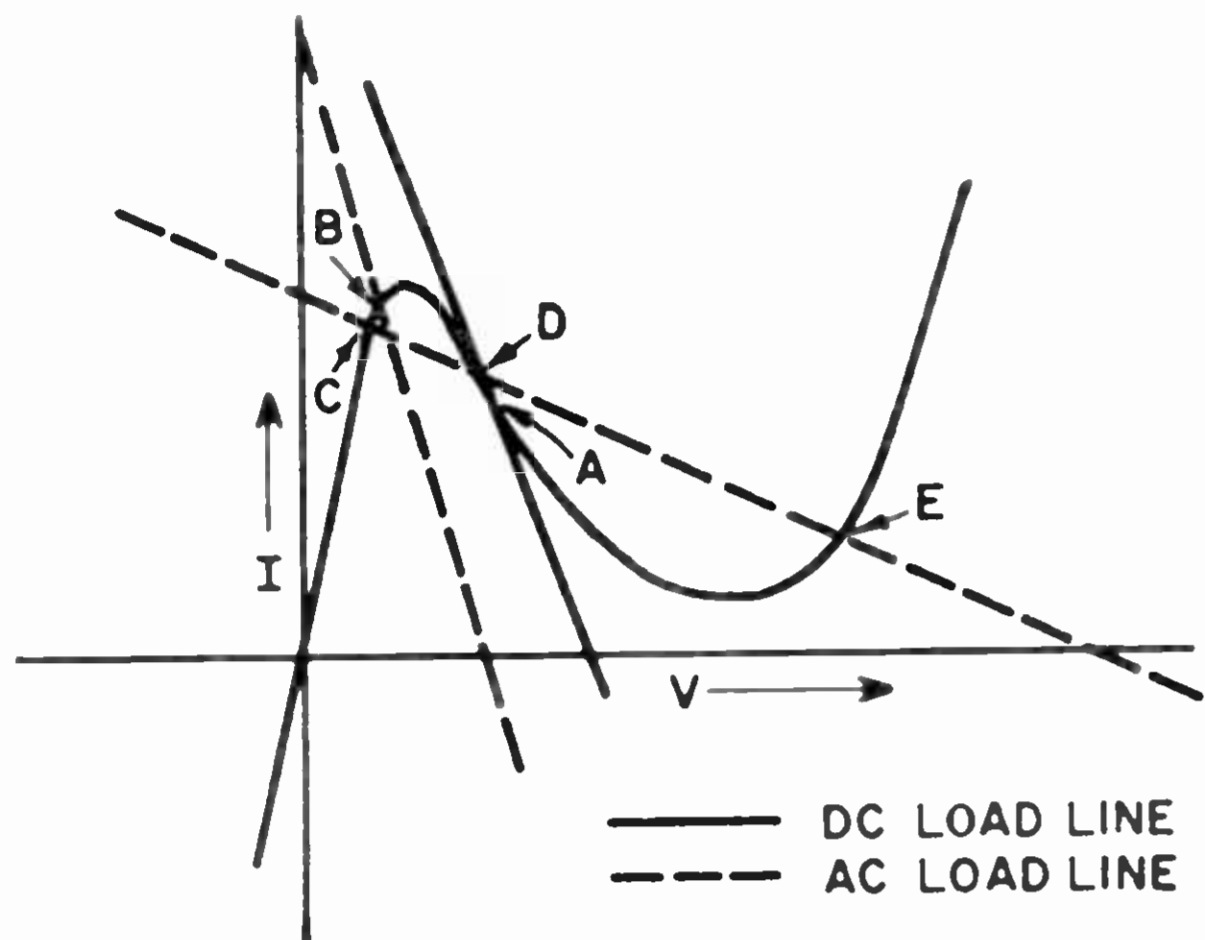


Fig. 292—Typical load lines for tunnel-diode circuits.

positive current step of sufficient amplitude is applied, the operating point switches to point E. Correspondingly, a negative input signal switches the operating point back to point C.

An advantage of the switching mode is its nonsensitivity to the exact linearity of the negative-resistance region of the tunnel-diode characteristics. Slight irregularities in the negative characteristic have negligible effect on the switching action.

In the basic monostable circuit or "gate" shown in Fig. 293(a), the static load line is determined by the resistance R_0 and the voltage V_0 . If R_0 is less than the minimum dynamic negative resistance of the diode, only a single operating point exists. The gate is stable in its low state if V_0 is adjusted so that the operating point is at E. The dynamic load line is determined by the inductive time constant L/R_0 . When the inductive time constant is long compared to the switching time t_s , the current in the circuit is effectively constant.

If a small step of current I_{in} is applied to the diode, the operating point switches to the high-voltage point F along the constant-current path

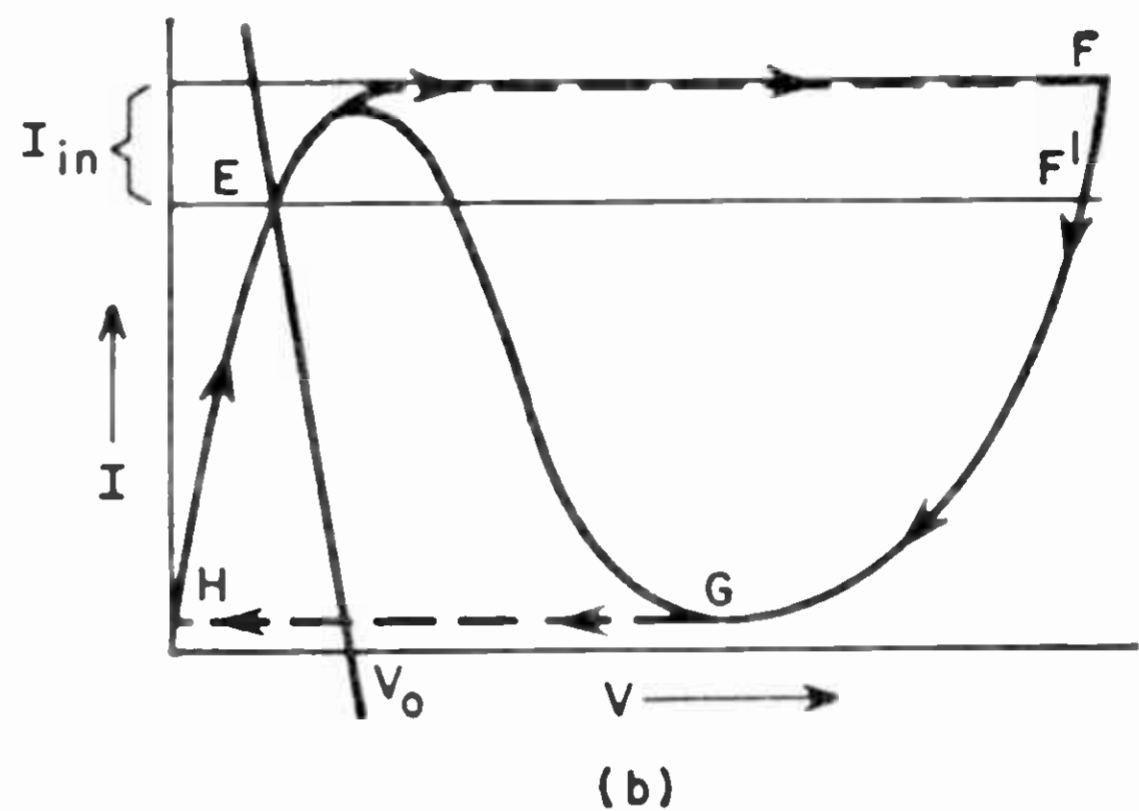
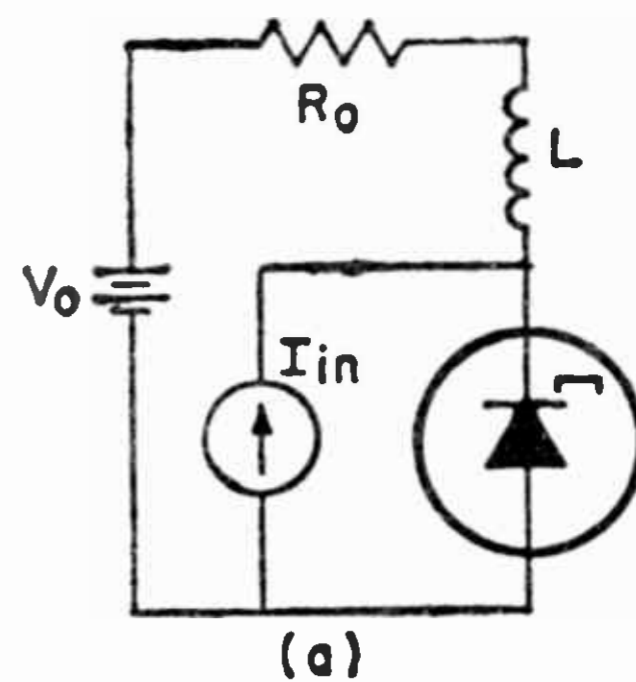


Fig. 293—Basic tunnel-diode logic circuit.

shown by the dashed line in Fig. 293(b). Removal of the input causes the operating point to move to F'. At this point, the energy stored in the inductor L must be dissipated before the circuit can return to its original operating point. As the energy in the inductor decreases, the operating point moves along the diode characteristic to the point of minimum current at G. When this point is reached, switching again occurs along a constant-current path to point H. The cycle of operation is completed by a recovery region in which the energy in the inductor builds up to its original level; during this period the operating point moves up the diode characteristic to the starting point.

Fig. 294(a) shows a simple tunnel-diode logic circuit. If the static operating bias is adjusted so that only one input is required to trigger the diode, an OR function is performed. If all inputs are required to trigger the diode, an AND function is performed. Because the coupling impedance is high compared to the diode impedance, the inputs can be considered as current sources during

the triggering period. Fig. 294(b) shows the biasing for a three-input AND gate. If the operating-point bias is increased slightly, the circuit can be made to trigger on two of its inputs; the logical function performed would then be that of a "majority gate".

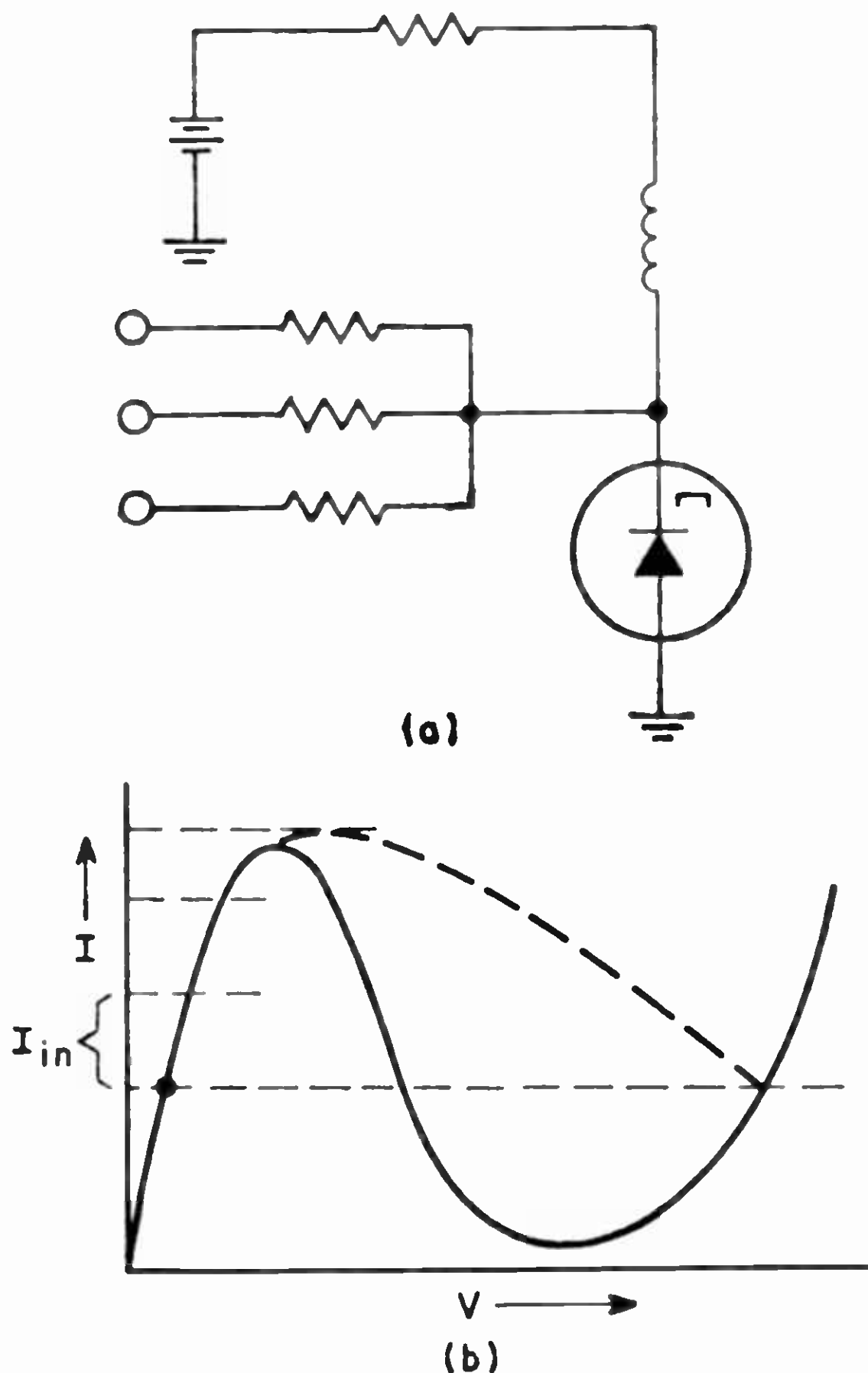


Fig. 294—Tunnel-diode "AND" gate.

Fig. 295 shows a tunnel rectifier in use as a tunnel-diode logic circuit. Because of its high-speed capability and superior rectification character-

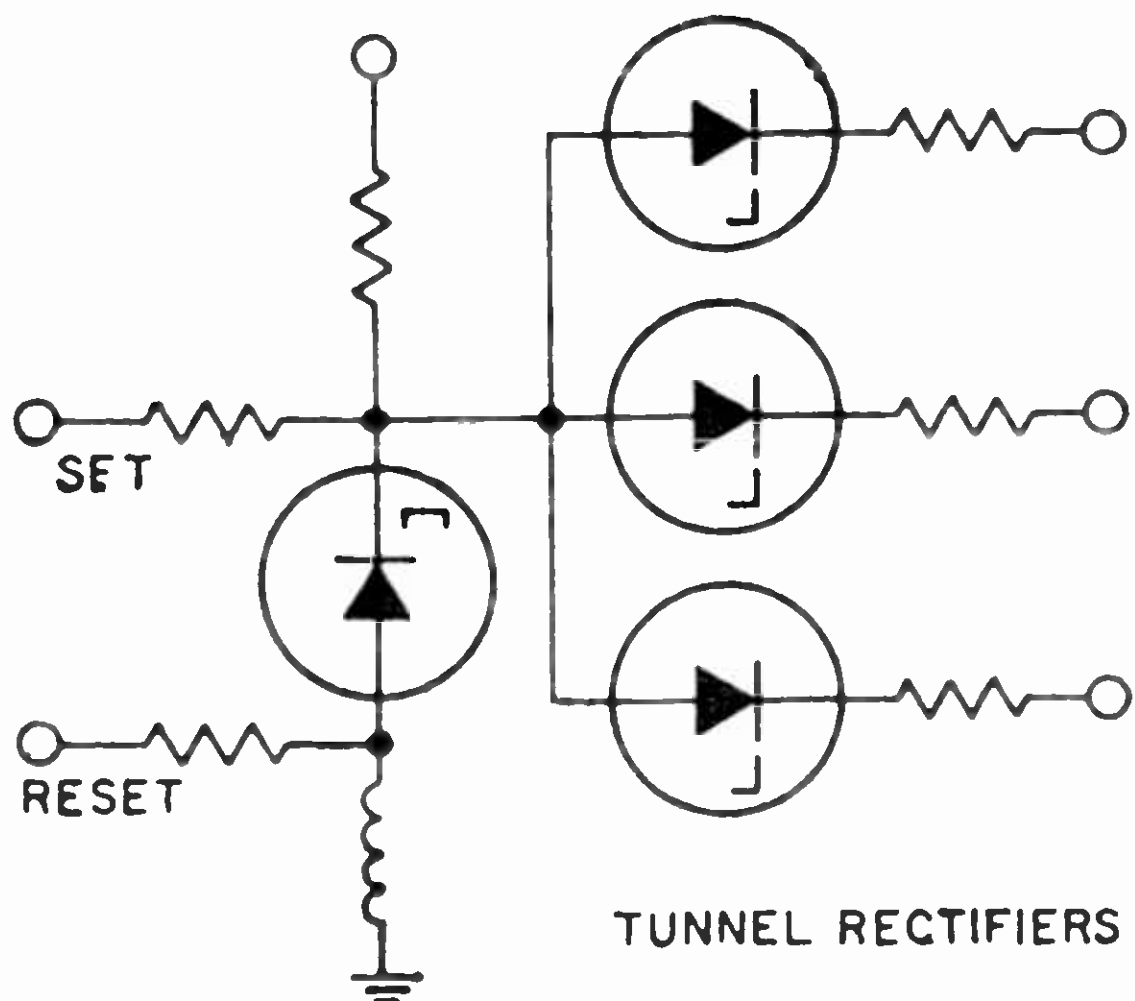


Fig. 295—Logic circuit using a tunnel diode and three tunnel resistors.

istics, the tunnel rectifier can be used to provide the directional coupling required in a logic circuit; it provides coupling in one direction (the ON state) and isolation in the opposite direction (OFF state).

LOGIC SYSTEMS

Propagation delay per stage or per pair of stages is the most important consideration in determining the speed capabilities of a logic system for computer applications. This delay time limits the maximum speed with which information can be processed in a computer. Typical propagation delays ranging from several microseconds to less than 10 nanoseconds can be obtained, depending upon the type of circuit and transistor used. As mentioned at the beginning of this section, integrated circuits are now in general use in computer application. However, the following description applies equally to discrete transistorized and integrated logic systems.

The simplest computer building block is the RTL (resistance-transistor-logic) circuit shown in Fig. 296. This circuit performs a NOR function if positive voltage levels are defined as binary "1" and negative voltages are defined as binary "0". RTL circuits must be designed so that dc stability is obtained under "worst-case" conditions. However, if optimum switching performance is desired, circuits are designed to provide maximum reverse base current for a given fan-in (number of inputs) and fan-out (number of outputs). This approach decreases storage and fall times and thus provides smaller propagation delays per stage, but decreases the fan-out capability of the circuit.

The measurement of propagation delay in RTL circuits is made under "worst-case" conditions, i.e., alternate stages are subjected in turn to maximum and then minimum drive conditions. Maximum drive produces short delay and rise times but long storage and fall times; it occurs

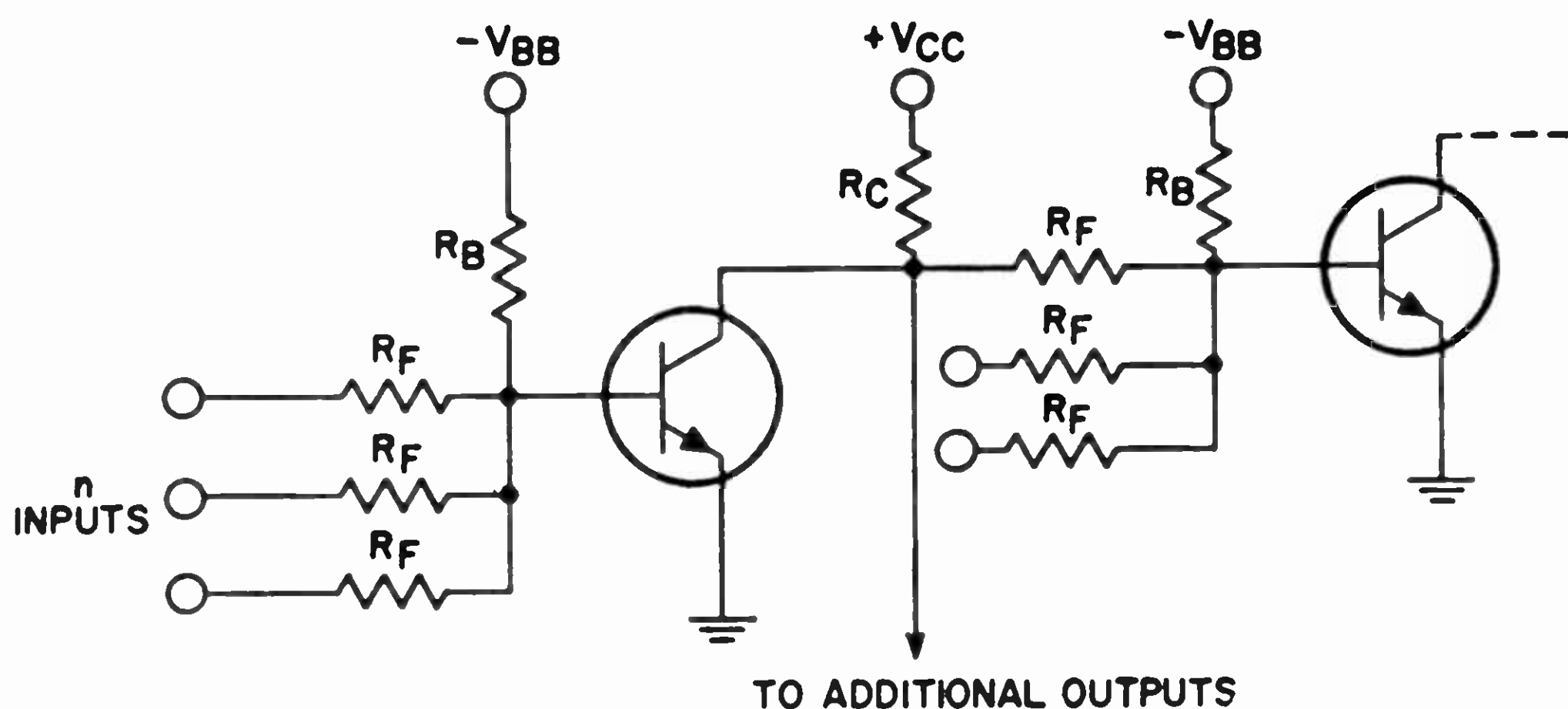


Fig. 296—Simple RTL (resistance-transistor-logic) NOR circuit.

when a given stage is driven by three unloaded stages. Minimum drive produces short storage and fall times but long delay and rise times; it occurs when a given stage is driven at only one input by a fully loaded stage.

A generalized RCTL (resistance-capacitance-transistor-logic) circuit is shown in Fig. 297. This type of logic circuit is characterized by a large number of transistors and is capable of extremely fast operation. The logic function performed by the RCTL arrangement of Fig. 297 is the same as that described for the RTL system shown in Fig. 296.

The high-speed operation of RCTL systems is a result of the use of the "speed-up" capacitor C_F . This capacitor compensates for stored charge in the transistor, and also provides large forward-base-current over-

drive on an instantaneous basis. Therefore, extremely fast transistor switching times can be obtained. However, the maximum repetition rate of the circuit is limited by the value of C_F . Therefore, C_F must be selected just large enough to compensate for the transistor stored charge.

Fig. 298 shows a generalized DTL (diode-transistor-logic) circuit which performs either a NAND or a NOR function depending upon the definition of voltage levels. The DTL circuit is characterized by extremely high speed, a large number of diodes, and relatively few transistors. Such circuits may use a collector clamp voltage, as shown, or may be designed without collector clamping provided all input diodes are reverse-biased when a transistor is to be ON. The latter approach makes pos-

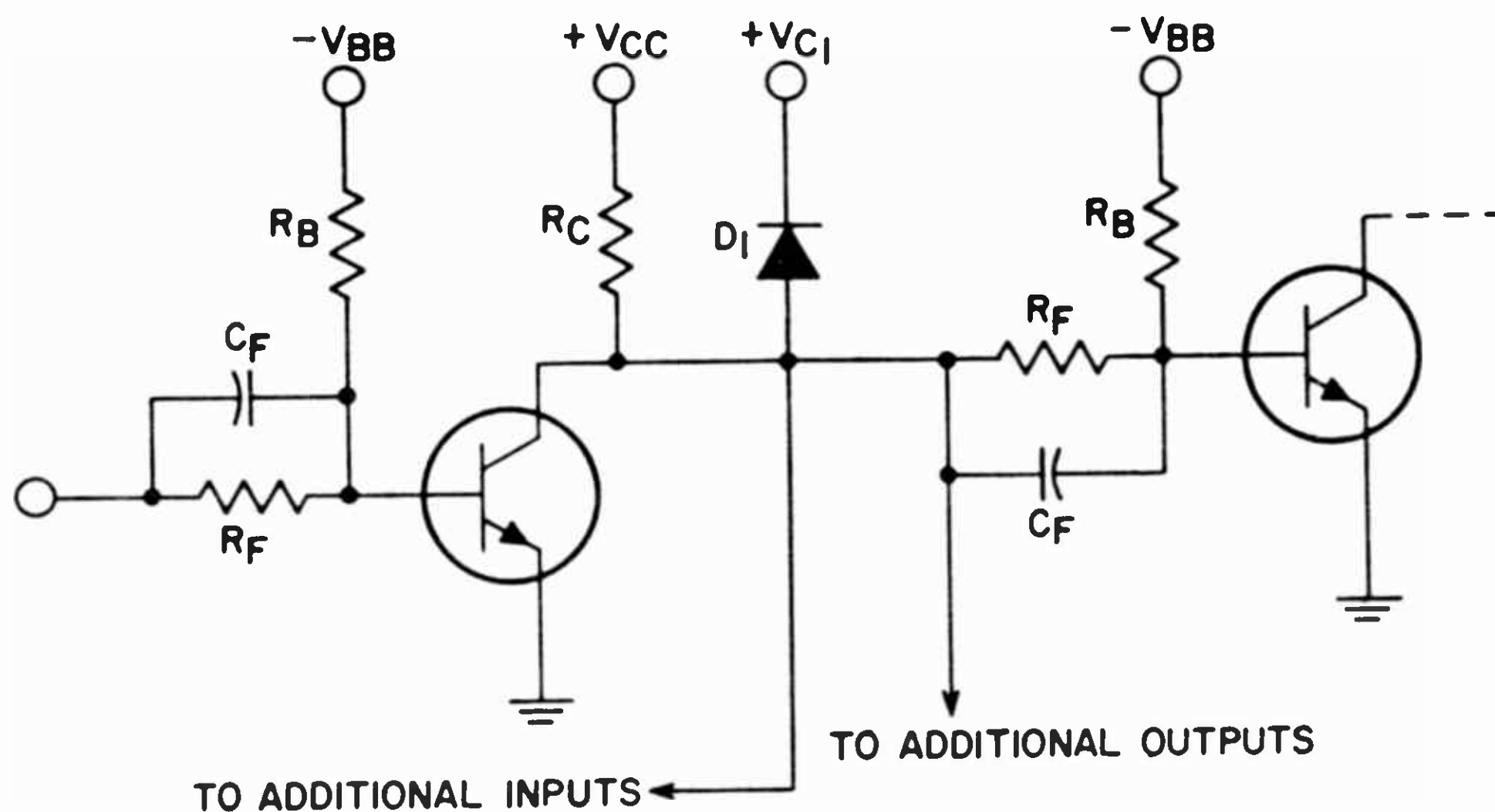


Fig. 297—Generalized RCTL (resistance-capacitance-transistor-logic) NOR circuit.

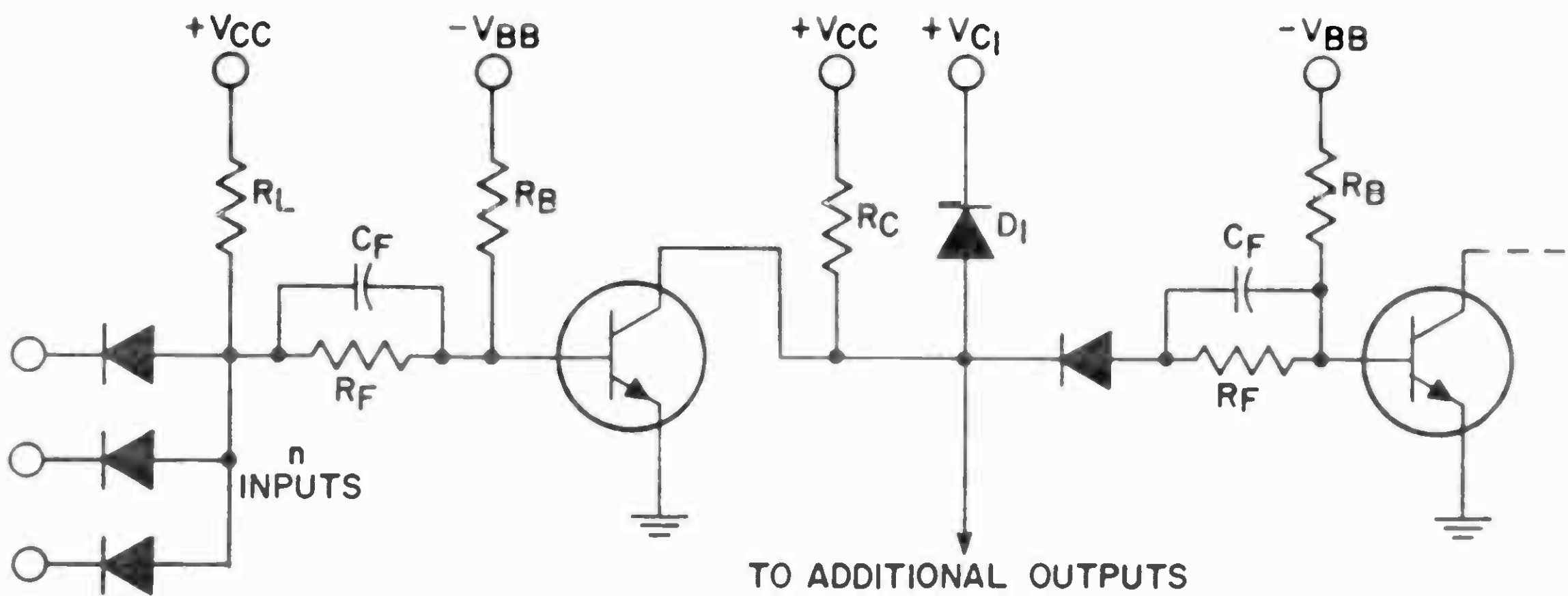


Fig. 298—Generalized DTL (diode-transistor-logic) circuit.

sible larger fan-in and fan-out, but is somewhat slower in speed than the design shown. The DTL system is more economical than the RCTL system because fewer transistors

are required to perform a given logic function.

Figs. 299 and 300 show two approaches to the design of ultra-high-speed, non-saturating logic circuits.

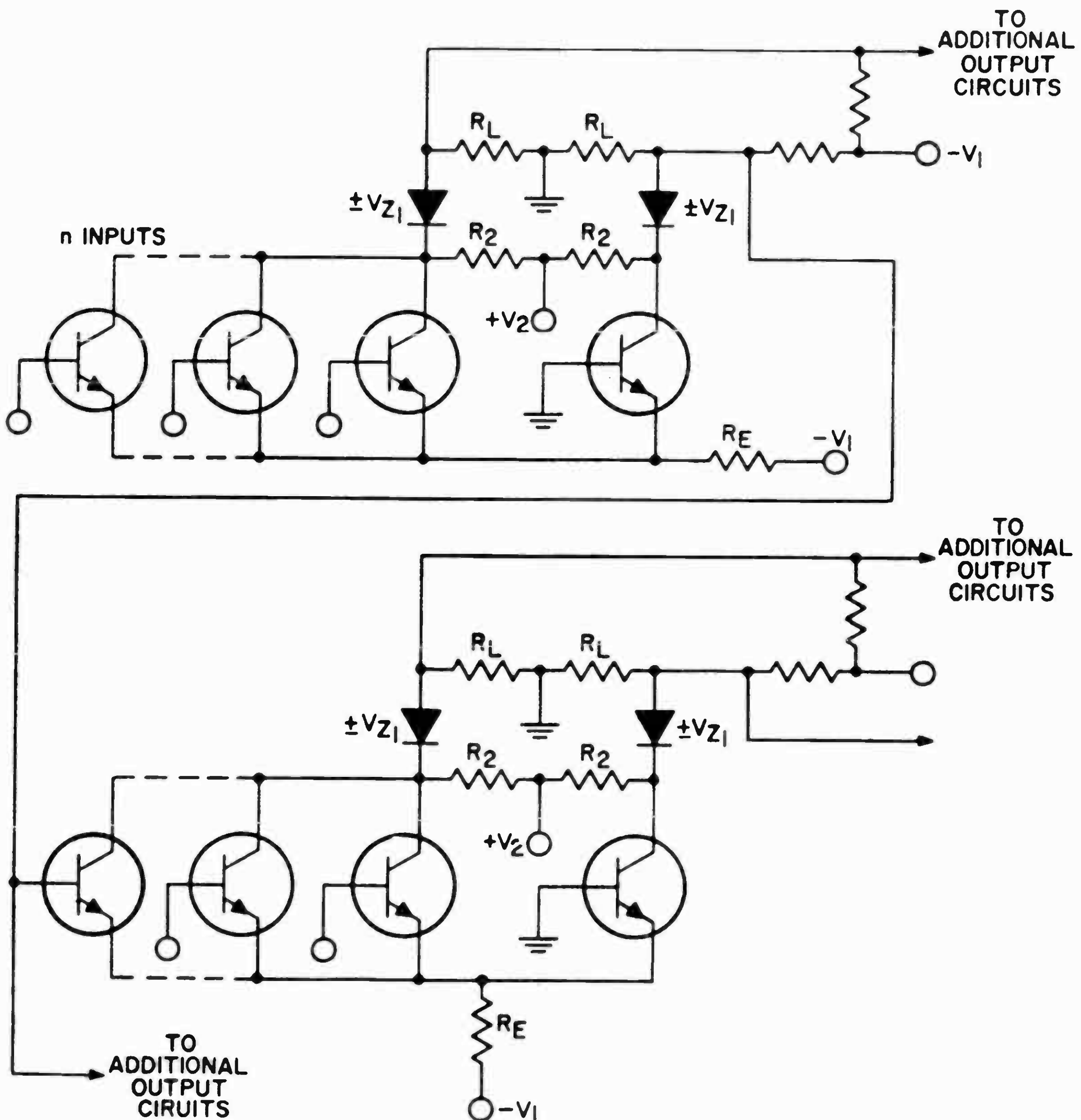


Fig. 299—Generalized current-steering system using reference diodes and transistors.

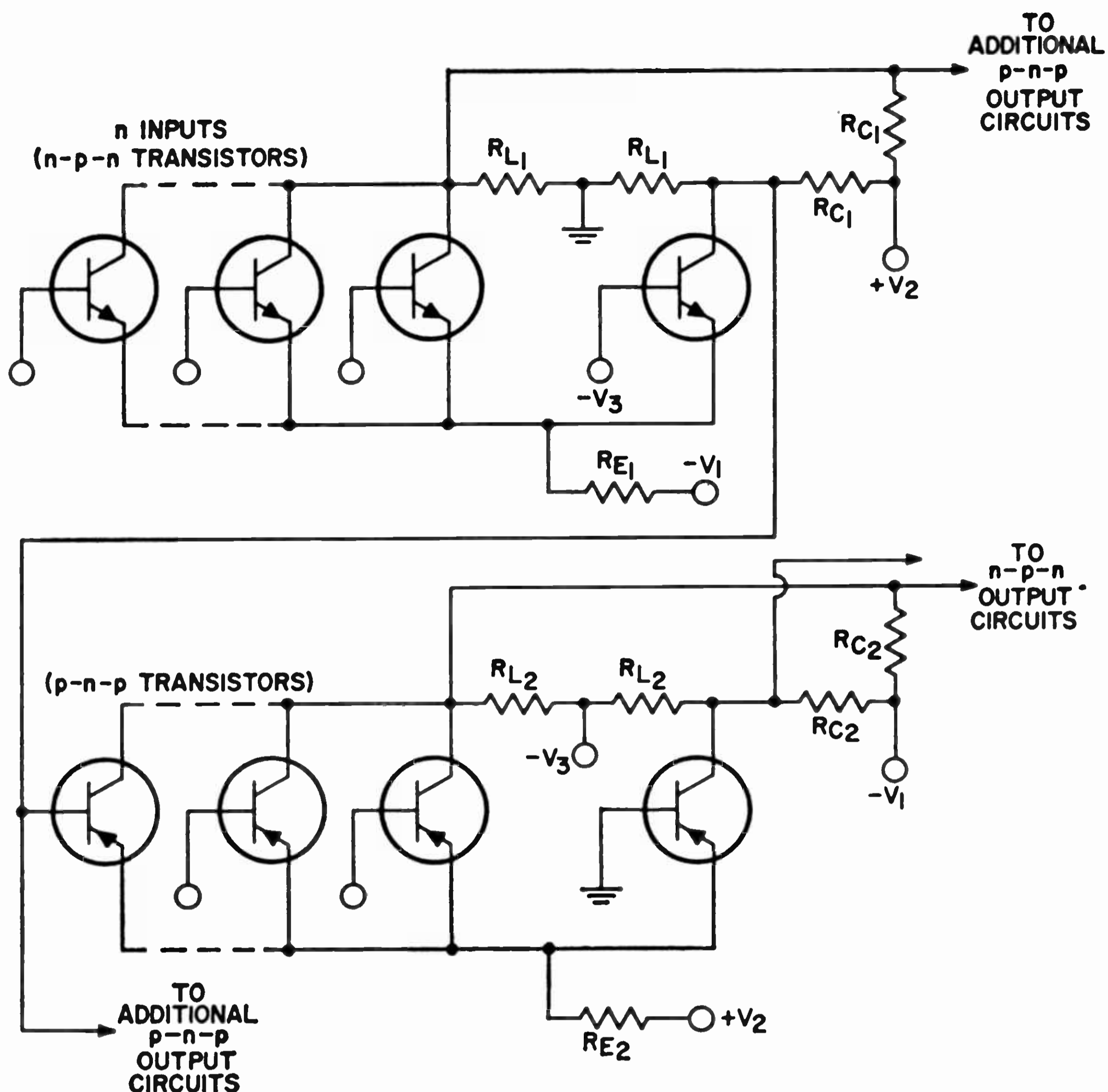


Fig. 300—Generalized circuit for complementary-symmetry current-steering system using only transistors.

The circuit in Fig. 299 is the generalized circuit for a current-steering system using reference diodes and transistors; Fig. 300 shows the generalized circuit for a complementary-symmetry current-steering system using only transistors.

Current-steering logic (CSL) circuits are characterized by a large number of transistors, high power dissipation, and ultra-high-speed operation. The logic function performed by these circuits is somewhat different from those discussed previously. Because of the extra transistors involved, such circuits can perform both a desired function and its inverse. For example, both NAND and AND or NOR and OR functions are directly obtained, the combination depending upon the definition of voltage levels.

The design of current-steering circuits must be optimized to use the smallest load resistor R_L possible because the ultimate speed of the circuit is limited by the time constant of this load resistance and the load capacitance. The complementary-symmetry approach is superior to diode current steering because it is equivalent in speed, provides the same transistor dissipation (and is thus equally reliable), and may be designed with less critical tolerances.

Computer operation requires the use of many flip-flop circuits for temporary storage of data. "Set-reset" flip-flops may be formed readily by use of any of the basic logic blocks described. A binary-counter-type flip-flop is shown in Fig. 301.

The design of the flip-flop circuit

is the same as for the RCTL system except for the trigger gating circuit and the value of C_F . The trigger gating circuit is designed so that a negative pulse at the input turns the ON transistor off. Therefore, the size of the input capacitors must be determined by the maximum stored charge of the transistor and the size of the input voltage swing. The two additional diodes connected from base to emitter of each transistor are used to eliminate time-constant problems at high frequencies. These diodes may be eliminated if high-frequency operation is not required.

The problem of noise control in computer systems increases in importance with the use of ultra-high-speed transistors and circuits. **Noise immunity** is defined as the ability of a given circuit to be relatively immune to a certain amplitude and duration of noise voltage. In computer circuits, there are essentially three sources of noise: (1) capacitive cross-coupling, (2) inductive cross-coupling, and (3) coupling through common impedances. The inductive noise component is generally

the most significant in transistor circuits because relatively low voltages and high currents are present.

To optimize a switching design for noise immunity, it is necessary to determine what noise-voltage amplitude at the input is required to cause a change at the output. Because this amplitude is a function of the transient response of the switching circuit, the pulse width or duration of the noise voltage must also be considered. In the following discussion, it is assumed that the noise voltage is of sufficient duration that effects of the circuit transient response may be neglected (i.e., that the noise-voltage duration is no less than the longest turn-on or turn-off time of the switching circuit).

The DTL circuit shown in Fig. 298 can be used to illustrate the design of a logic circuit for noise immunity. When all inputs are high, a negative noise pulse at any input tends to turn the ON transistor off; a positive noise pulse has no effect. The amplitude of noise required to effect a change is determined by the reverse bias V_R on the input diodes,

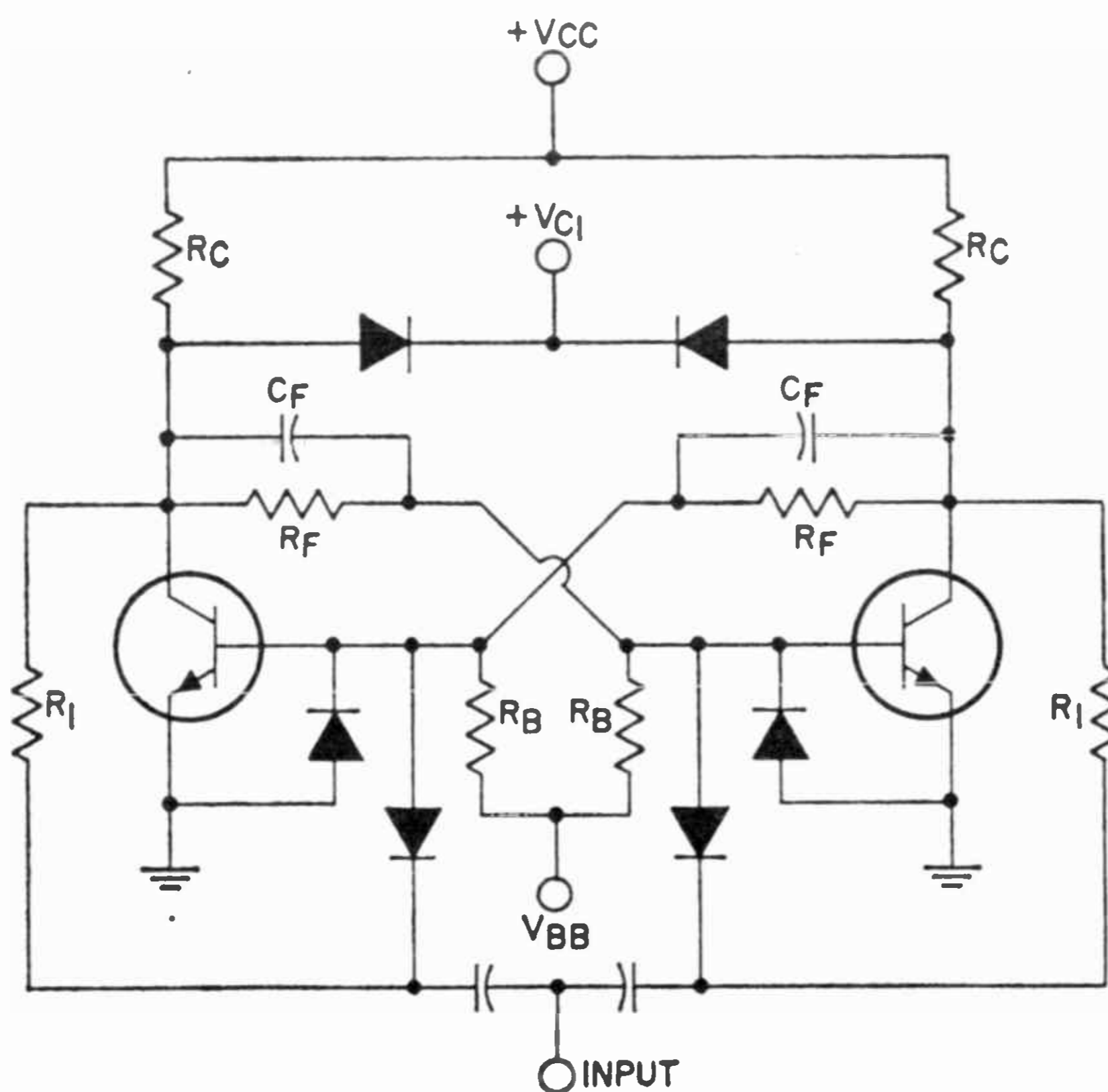


Fig. 301—Binary-counter-type flip-flop circuit.

the amount of forward bias V_F necessary to cause appreciable conduction of an input diode, and the stored charge Q_s of the ON transistor. For the ON condition, therefore, the negative noise-voltage amplitude required to cause a change in the output is given by

$$-V_n = V_R + V_F + (Q_s/C_F)$$

When any one of the inputs is low and the transistor is OFF, only a positive noise pulse at a low input has any effect on the transistor output. The amplitude of the positive noise voltage required to start the transistor turning ON is determined by the amount of reverse bias V_B on the base-to-emitter junction of the transistor, the forward bias V_{BE} required across the base-to-emitter junction to cause appreciable conduction of base current, and the amount of charge necessary to charge the input capacitance C_i at the base through the voltage $V_B + V_{BE}$. For the OFF condition, there-

fore, the positive noise-voltage amplitude required is given by

$$V_n = (V_B + V_{BE}) \left(1 + \frac{C_i}{C_F}\right)$$

A per-cent noise-immunity figure can be defined for a particular circuit as the ratio of the noise voltages determined above to the normal voltage swing of a true input, which is approximately equal to the collector supply voltage. It is desirable to have equal noise immunity for both the ON and OFF conditions because the per-cent noise-immunity figure for the circuit is no better than the lower value.

Because the values V_F , V_{BE} , Q_s , C_F , and C_i are constants for a specific transistor and diode, the values of V_R and V_B may be chosen to obtain a desired noise immunity for a given circuit design. However, circuit noise immunity and fan-out capability are interdependent; if noise immunity is made too large; fan-out capability will suffer. Therefore, a compromise between the two must be made.

DC Power Supplies

DC power supplies convert the output of a prime source, such as a generator, to a form useful to the circuit to be powered. The supply of power usually requires rectification to change ac to dc, filtering to smooth out the ac ripple in the output of the rectifier circuit, and regulation to assure a constant output from the power supply in spite of variations in the input voltage and output load.

RECTIFICATION

The most suitable type of rectifier circuit for a particular application depends on the dc voltage and current requirements, the amount of rectifier "ripple" (undesired fluctuation in the dc output caused by an ac component) that can be tolerated in the circuit, and the type of ac power available. Figs. 302 through 308 show seven basic rectifier configurations. These illustrations include the output-voltage waveforms for the various circuits and the current waveforms for each individual rectifier in the circuits. Filtering of the output of the rectifier circuits is discussed later in this section. Ideally, the voltage waveform should be as flat as possible (i.e., approaching almost pure dc). A flat curve indicates a peak-to-average voltage ratio of one.

The single-phase half-wave circuit shown in Fig. 302 delivers only one pulse of current for each cycle of ac input voltage. As shown by the current waveform, the single rectifier conducts the entire current flow. This type of circuit contains

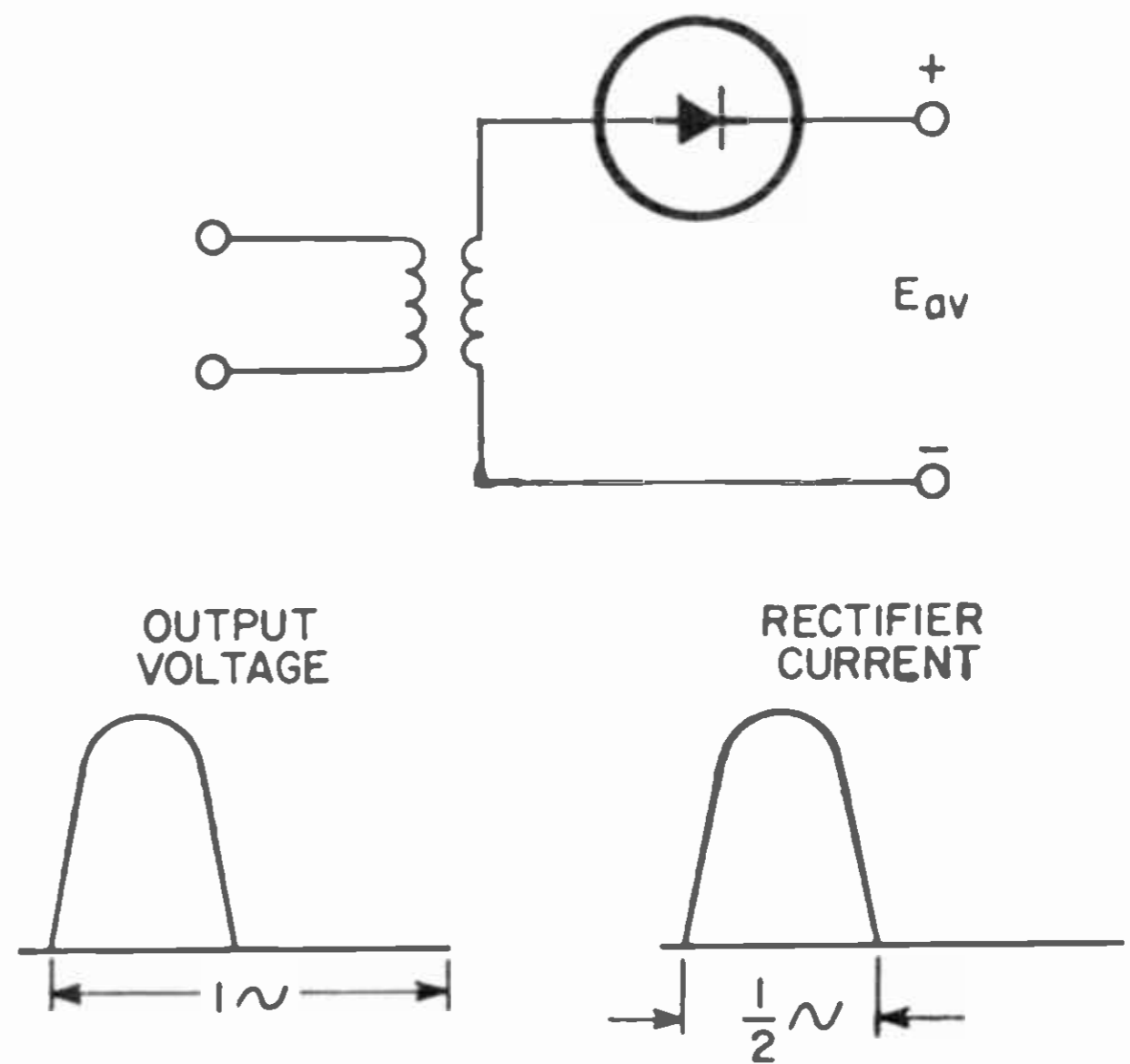


Fig. 302—Single-phase half-wave circuit.

a very high percentage of output ripple.

Fig. 303 shows a single-phase full-wave circuit that operates from a

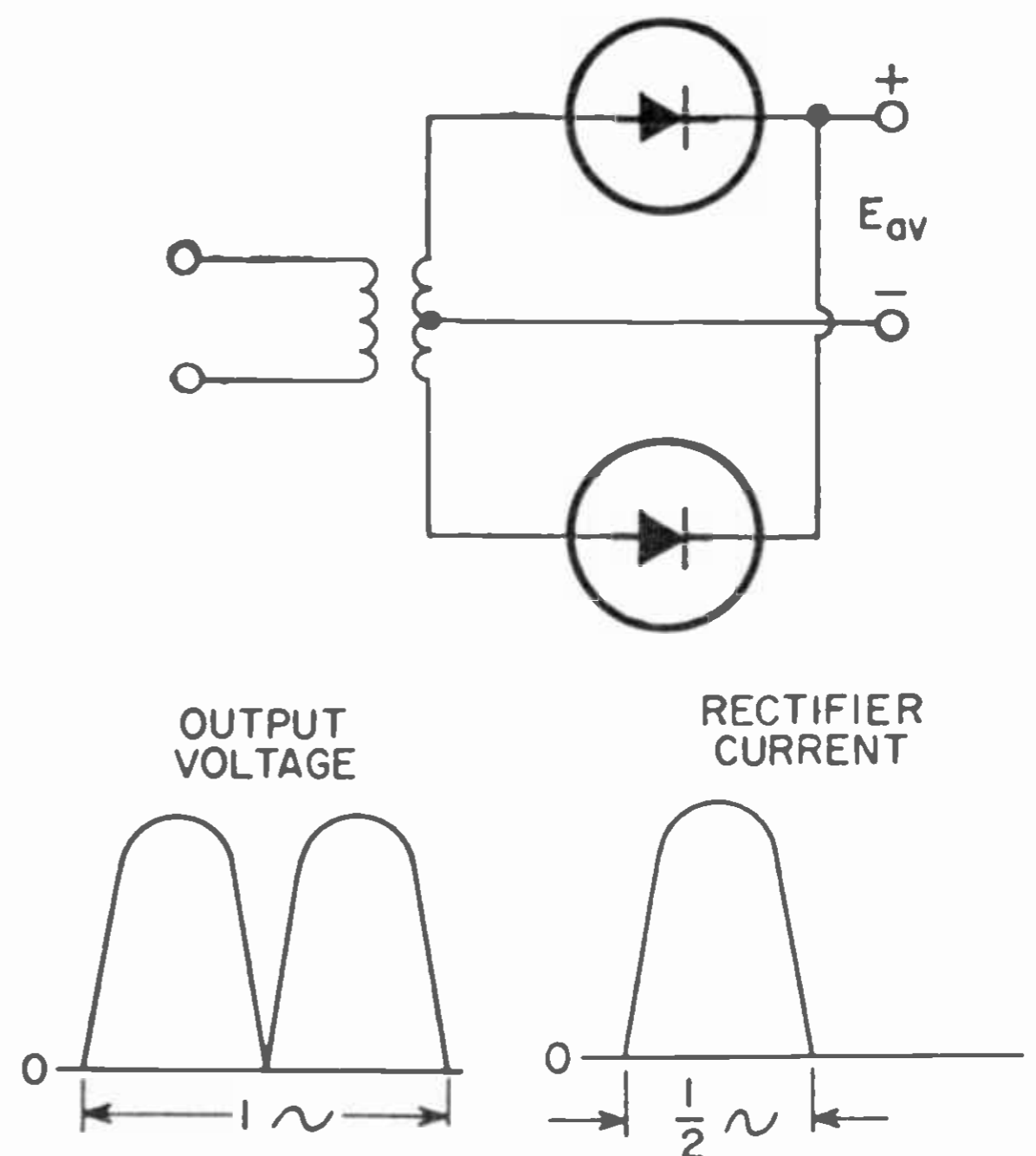


Fig. 303—Single-phase full-wave circuit with center-tapped power transformer.

center-tapped high-voltage transformer winding. This circuit has a lower peak-to-average voltage ratio than the circuit of Fig. 302 and about 65 per cent less ripple. Only 50 per cent of the total current flows through each rectifier. This type of circuit is widely used in television receivers and large audio amplifiers.

The single-phase full-wave bridge circuit shown in Fig. 304 uses four

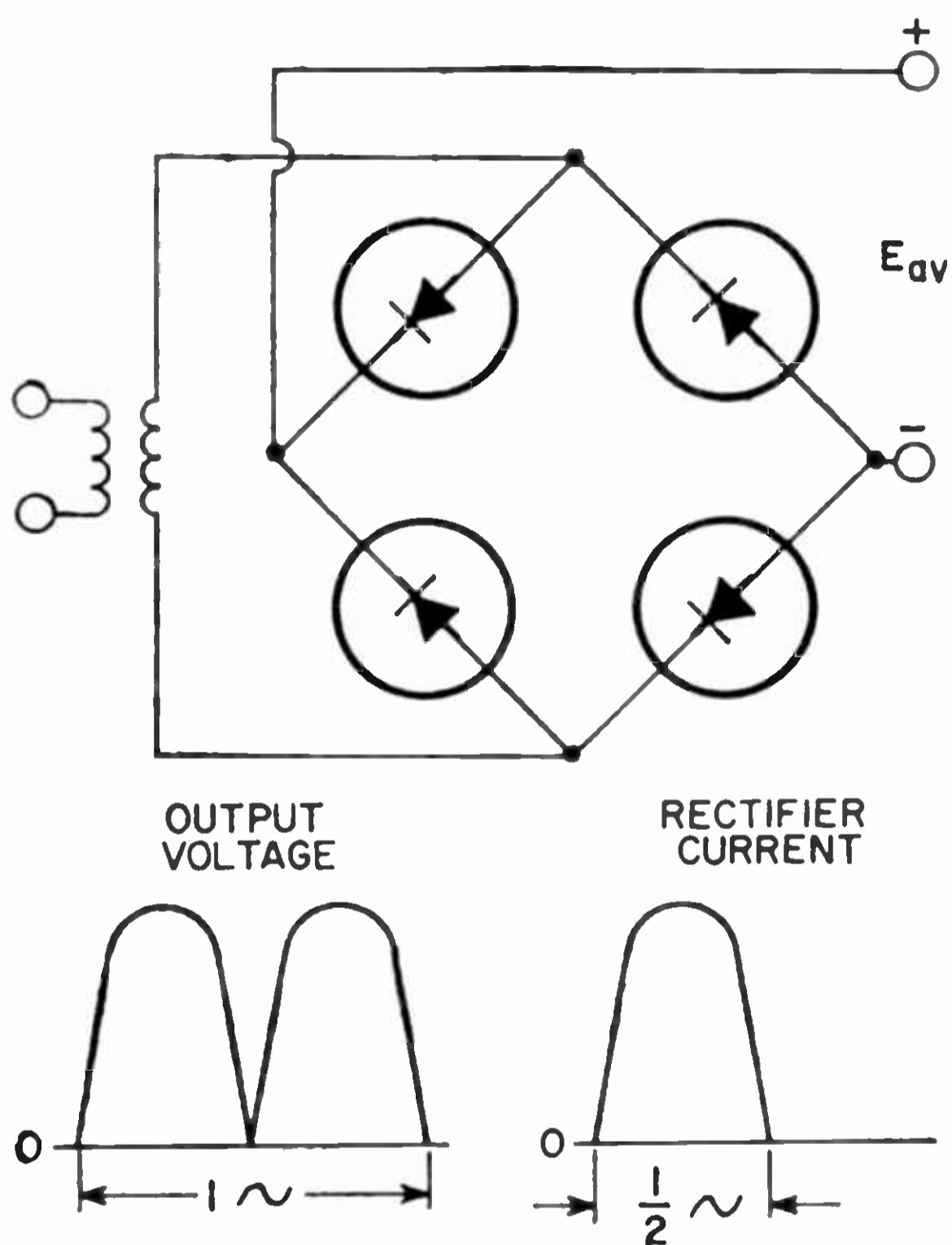


Fig. 304—Single-phase full-wave circuit without center-tapped power transformer (i.e., bridge-rectifier circuit).

rectifiers, and does not require the use of a transformer center-tap. It

can be used to supply twice as much output voltage as the circuit of Fig. 303 for the same transformer voltage, or to expose the individual rectifiers to only half as much peak reverse voltage for the same output voltage. Only 50 per cent of the total current flows through each rectifier. This type of circuit is popular in amateur transmitter use.

The three-phase circuits shown in Figs. 305 through 308 are usually found in heavy industrial equipment such as high-power transmitters. The three-phase Y half-wave circuit shown in Fig. 305 uses three rectifiers. This circuit has considerably less ripple than the circuits discussed above. In addition, only one-third of the total output current flows through each rectifier.

Fig. 306 shows a three-phase full-wave bridge circuit which uses six rectifiers. This circuit delivers twice as much voltage output as the circuit of Fig. 305 for the same transformer conditions. In addition, this circuit, as well as those shown in Figs. 307 and 308, has an extremely small percentage of ripple.

In the six-phase "star" circuit shown in Fig. 307, which also uses six rectifiers, the least amount of the total output current (one-sixth) flows through each output rectifier. The three-phase double-Y and inter-phase transformer circuit shown in

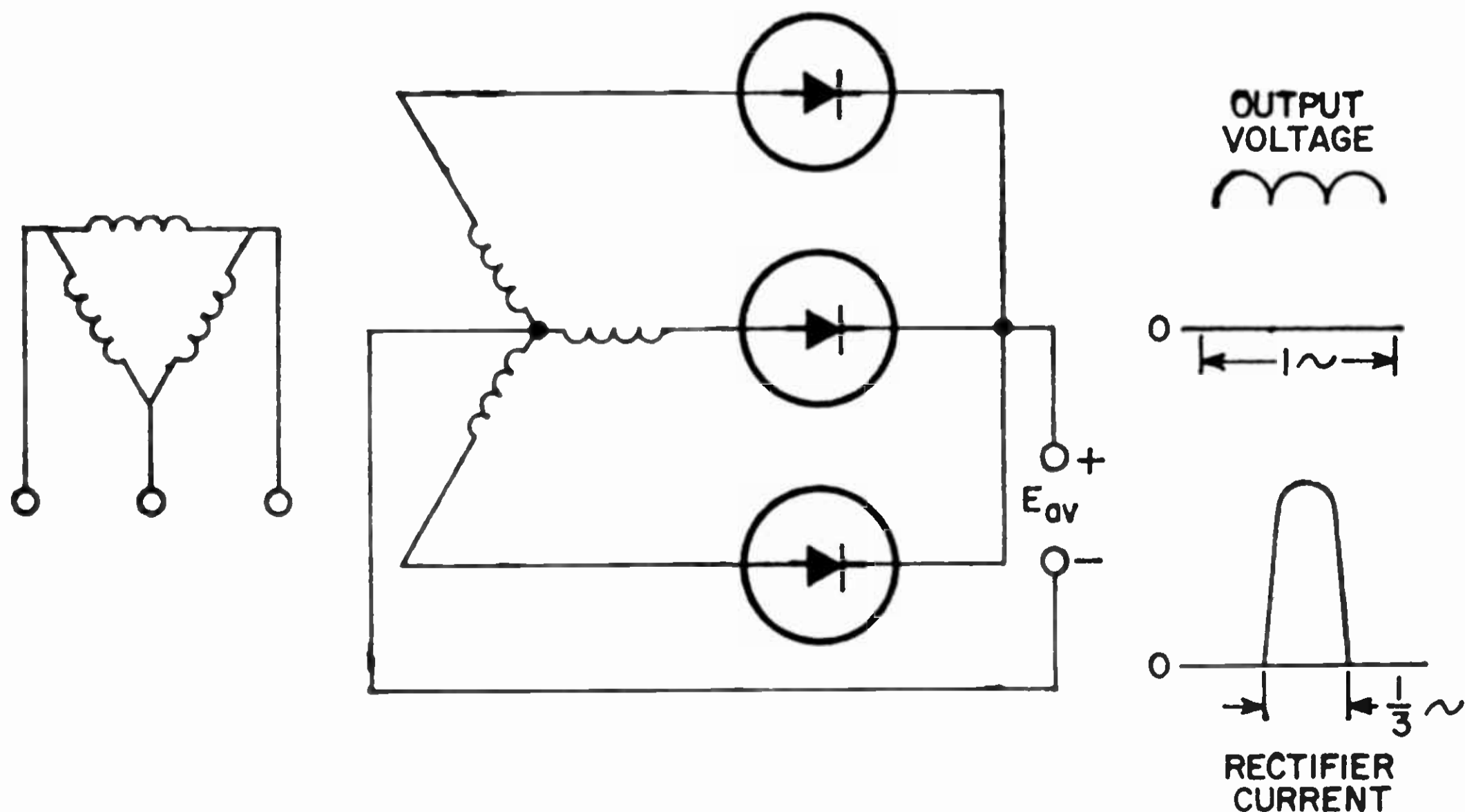


Fig. 305—Three-phase "Y" half-wave circuit.

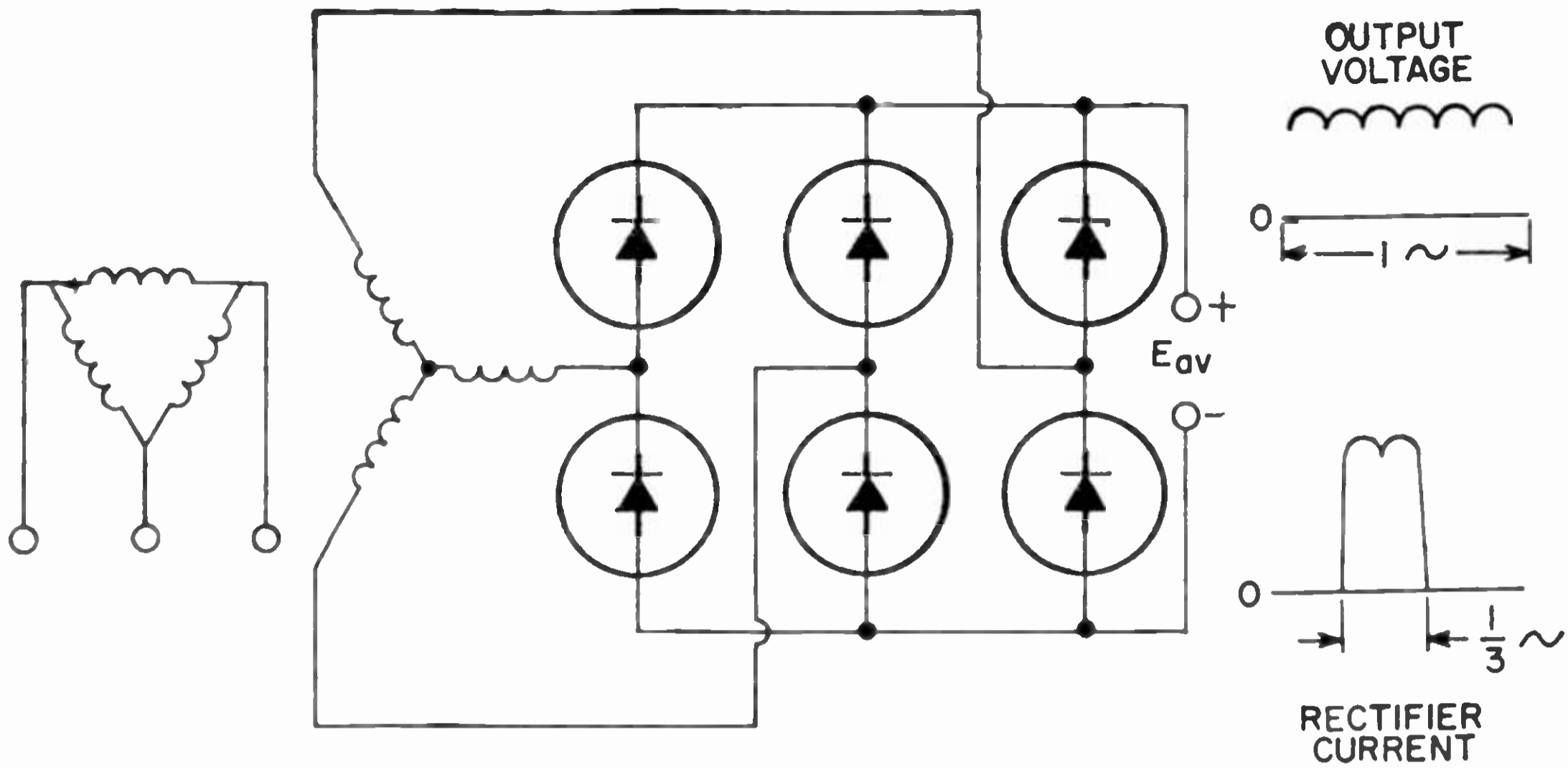


Fig. 306—Three-phase "Y" full-wave circuit.

Fig. 308 uses six half-wave rectifiers in parallel. This arrangement delivers six current pulses per cycle and twice as much output current as the circuit shown in Fig. 305.

Table IV lists voltage and current ratios for the circuits shown in Figs. 302 through 308 for resistive or inductive loads. These ratios apply for sinusoidal ac input voltages. It is

generally recommended that inductive loads rather than resistive loads be used for filtering of rectifier current, except for the circuit of Fig. 302. Current ratios given for inductive loads apply only when a filter choke is used between the output of the rectifier and any capacitor in the filter circuit. Values shown do not take into consideration voltage drops

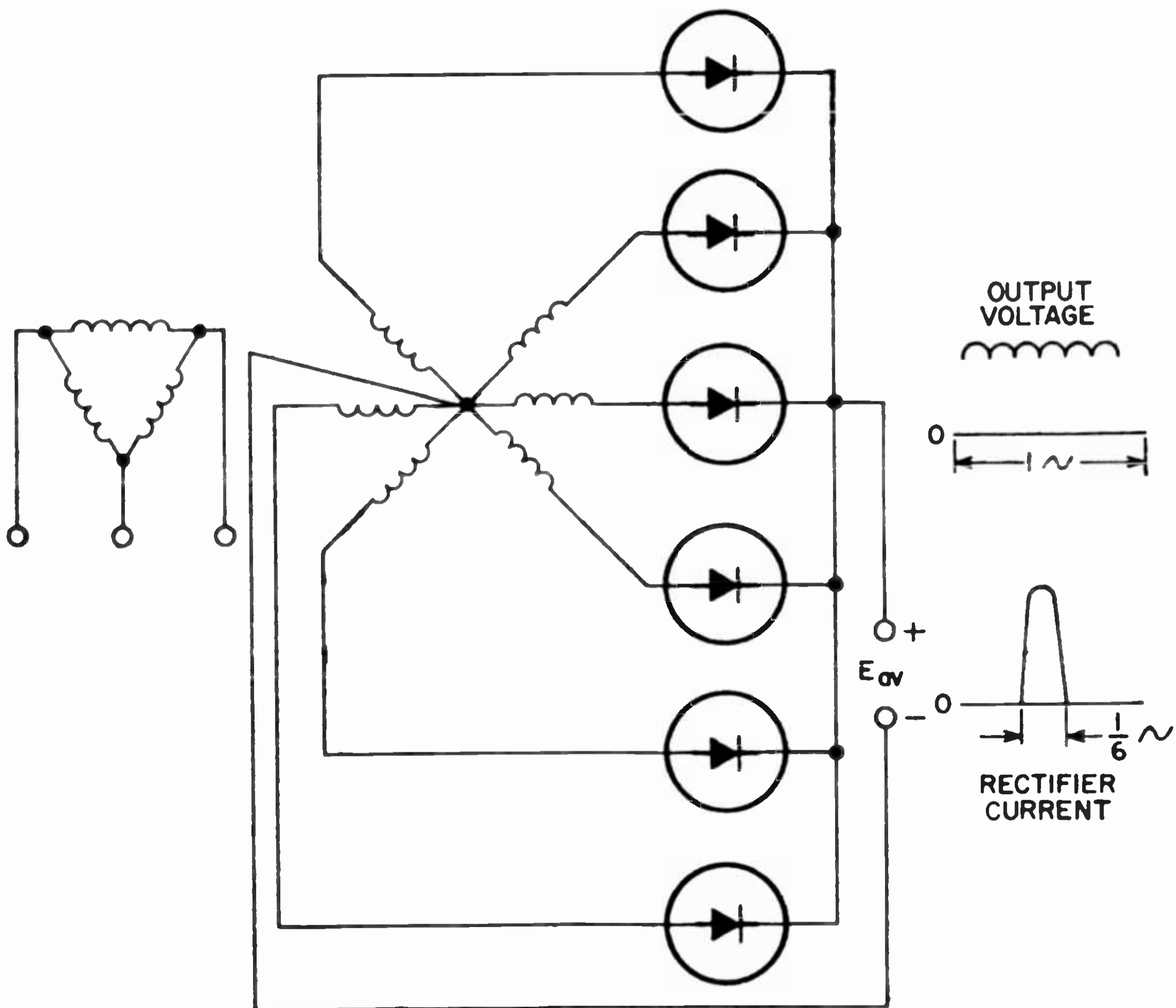


Fig. 307—Six-phase "star" circuit.

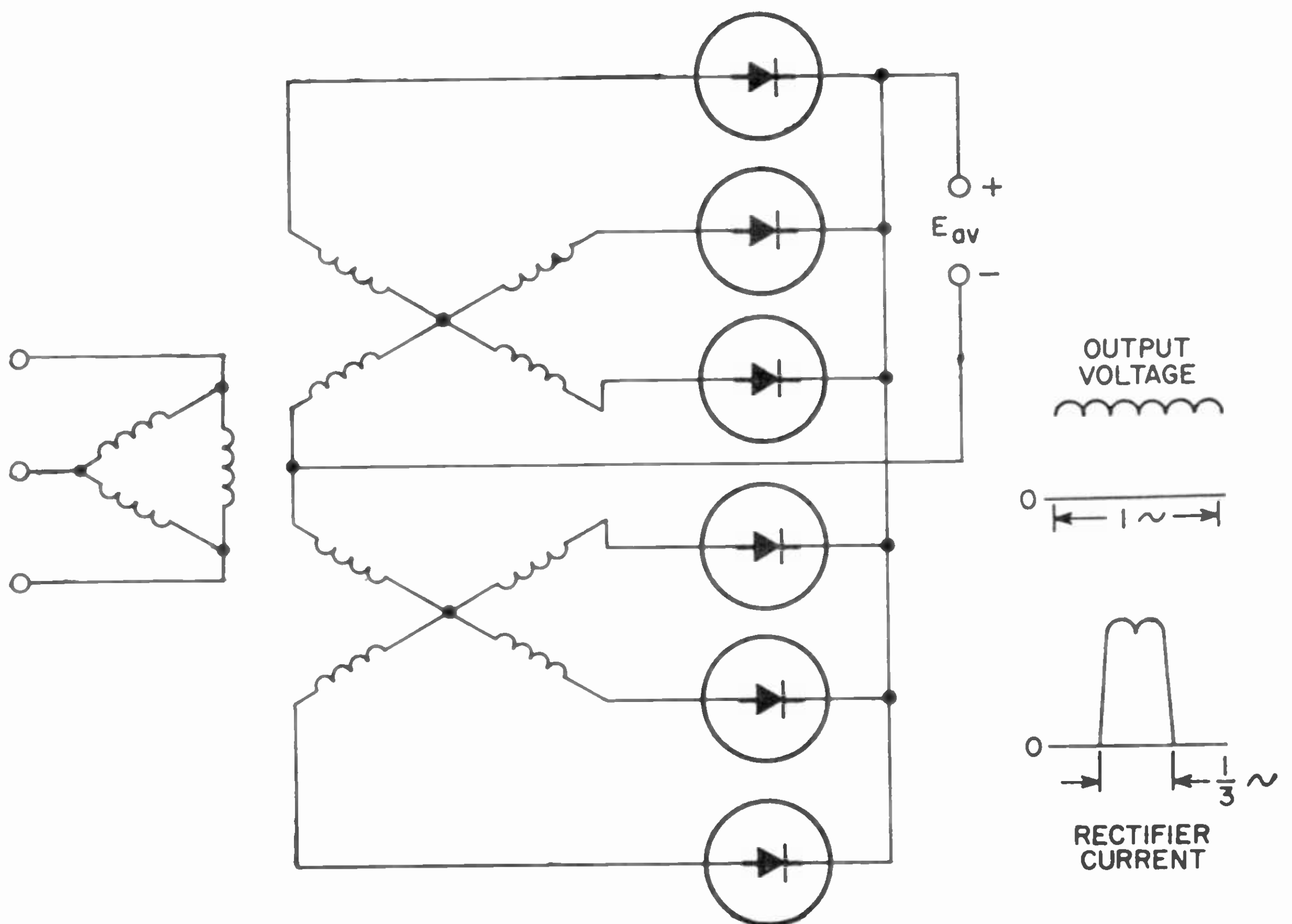


Fig. 308—Three-phase “double-Y” and interphase-transformer circuit.

which occur in the power transformer, the silicon rectifiers, or the filter components under load conditions. When a particular rectifier type has been selected for use in a specific circuit, Table IV can be used to determine the parameters and characteristics of the circuit.

In Table IV, all ratios are shown as functions of either the average output voltage E_{av} or the average dc output current I_{av} , both of which are expressed as unity for each circuit. In practical applications, the magnitudes of these average values will, of course, vary for the different circuit configurations.

FILTERING

Filter circuits are used to smooth out the ac ripple in the output of a rectifier circuit. Filters consist of two basic types, inductive “choke” input and capacitive input. Combinations and variations of these types are often used; some typical filter circuits are shown in Fig. 309.

The simplest of these filtering circuits is the capacitive input type.

This type of filtering is most often used in low-current circuits in which a fairly large amount of ripple can be tolerated. Such circuits are usually single-phase, half-wave or full-wave. In this type of filter, the capacitor charges up to approximately the peak of the input voltage on each half-cycle that a rectifier conducts. The current into the load is then supplied from the capacitor rather than from the power supply until the point in the next half-cycle when the input voltage again equals the voltage across the capacitor. A rectifier circuit that uses a smoothing capacitor and the voltages involved are shown in Fig. 310.

Higher average dc output voltages and currents can be obtained from this type of circuit by the use of larger capacitors. A larger capacitor also tends to reduce the ripple. However, care must be taken that the capacitor is not so large that excessive peak and rms currents cause overheating of the rectifier.

The next simplest filter is the inductive input filter. This filter performs the same function as a capacitive input filter in that it smooths

Table IV—Voltage and Current Ratios for Rectifier Circuits Shown in Figs. 302 Through 308. Fig. 302 Uses a Resistive Load, and Figs. 303 Through 308 an Inductive Load

CIRCUIT RATIOS	Fig. 302	Fig. 303	Fig. 304	Fig. 305	Fig. 306	Fig. 307	Fig. 308
Output Voltage:							
Average $\dots\dots\dots$	E_{av}	E_{av}	E_{av}	E_{av}	E_{av}	E_{av}	E_{av}
Peak ($\times E_{av}$) $\dots\dots$	3.14	1.57	1.57	1.21	1.05	1.05	1.05
RMS ($\times E_{av}$) $\dots\dots$	1.57	1.11	1.11	1.02	1.00	1.00	1.00
Ripple (%) $\dots\dots$	121	48	48	18.3	4.3	4.3	4.3
Input Voltage (RMS):							
Phase ($\times E_{av}$) $\dots\dots$	2.22	1.11*	1.11	0.855 [●]	0.428 [●]	0.74 [●]	0.855 [●]
Line-to-Line ($\times E_{av}$)	2.22	2.22	1.11	1.48	0.74	1.48 [†]	1.71 [‡]
Average Output (Load)							
Current $\dots\dots\dots$	I_{av}	I_{av}	I_{av}	I_{av}	I_{av}	I_{av}	I_{av}
RECTIFIER CELL RATIOS							
Forward Current:							
Average ($\times I_{av}$) \dots	1.00	0.5	0.5	0.333	0.333	0.167	0.167
RMS ($\times I_{av}$):							
resistive load \dots	1.57	0.785	0.785	0.587	0.579	0.409	0.293
inductive load \dots	—	0.707	0.707	0.578	0.578	0.408	0.289
Peak ($\times I_{av}$):							
resistive load \dots	3.14	1.57	1.57	1.21	1.05	1.05	0.525
inductive load \dots	—	1.00	1.00	1.00	1.00	1.00	0.500
Ratio peak to average:							
resistive load \dots	3.14	3.14	3.14	3.63	3.15	6.30	3.15
inductive load \dots	—	2.00	2.00	3.00	3.00	6.00	3.00
Peak Reverse Voltage:							
$\times E_{av}$ $\dots\dots\dots$	3.14	3.14	1.57	2.09	1.05	2.42	2.09
$\times E_{rms}$ $\dots\dots\dots$	1.41	2.82	1.41	2.45	2.45	2.83	2.45

* to center tap ● to neutral † maximum value ‡ maximum value, no load

the load current by storing energy during one part of the cycle and releasing it to the load during another part of the cycle. However, the

inductor acts in a different way by extending the time during which current is drawn from a rectifier. When a smoothing inductor is used

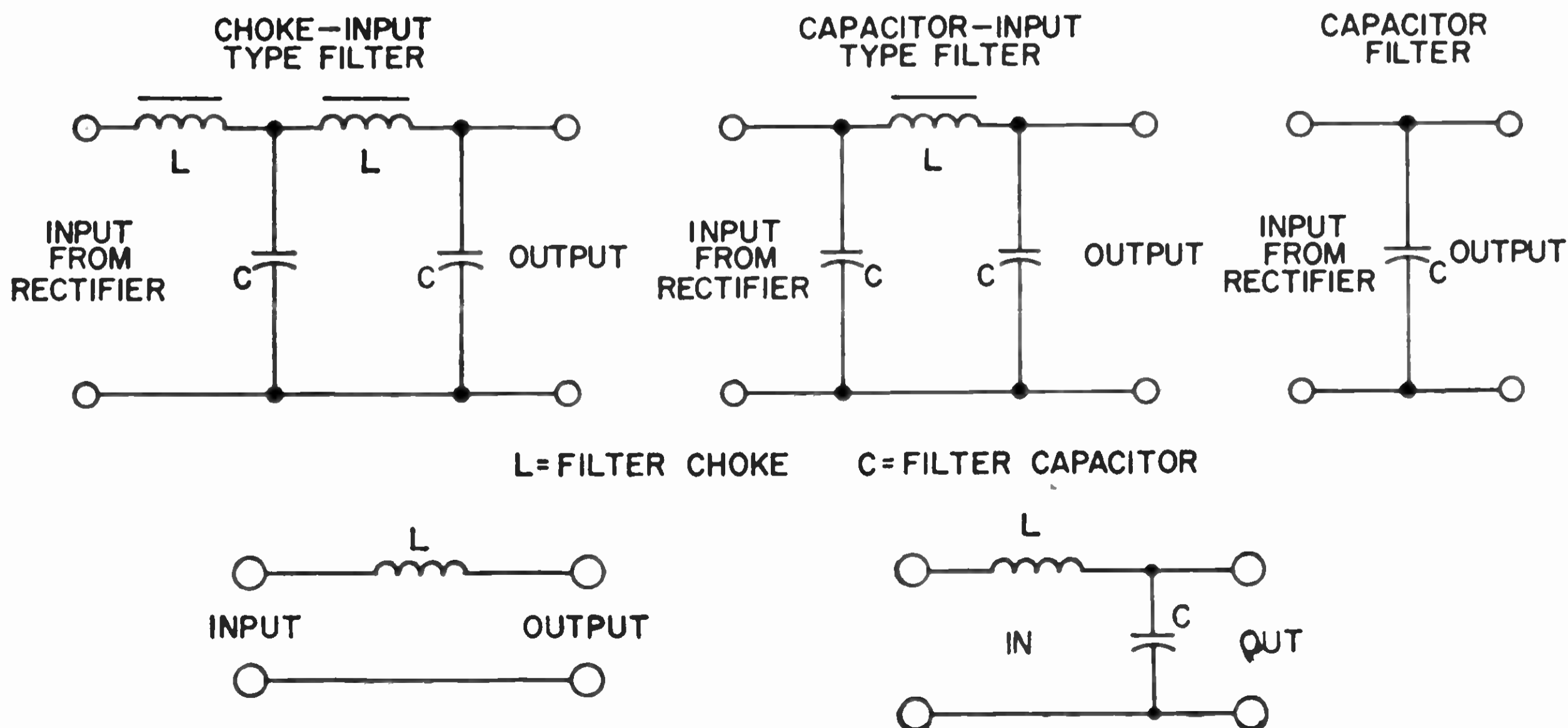


Fig. 309—Typical filter circuits.

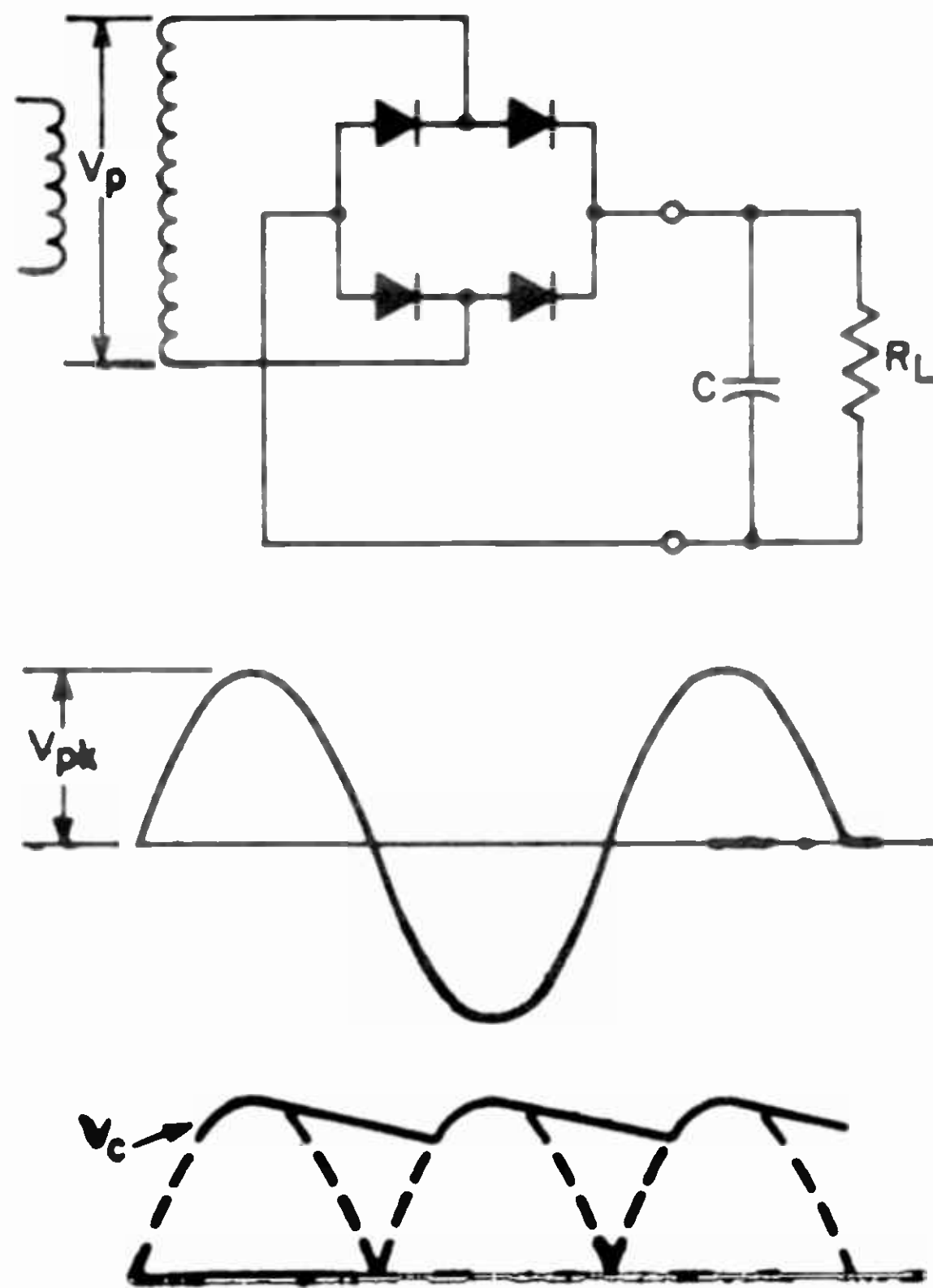


Fig. 310—Bridge-rectifier circuit with capacitor input filter.

in series with a full-wave rectifier circuit, the conduction period of each rectifier may be extended so that conduction does not stop in one rectifier until the other rectifier starts conducting. As a result of this spreading action, any increase in inductance to reduce ripple results in a decrease in the average output voltage and current.

The smoothing capabilities of capacitors and inductors can be combined as shown in the other filters of Fig. 309 to take advantage of the best feature of each. Filters which provide maximum output and minimum ripple and use reasonably small components can thus be designed.

REGULATORS

In the operation of a regulator circuit, the difference between a reference input (e.g., the supply voltage) and some portion of the output voltage (e.g., a feedback signal) is used to supply an actuating error signal to the control elements. The amplified error signal is applied in a manner that tends to

reduce this difference to zero. Regulators are designed to provide a constant output voltage very nearly equal to the desired value in the presence of varying input voltage and output load.

In series regulator circuits such as that shown in Fig. 311, direct-coupled amplifiers are used to amplify an error or difference signal obtained from a comparison between a por-

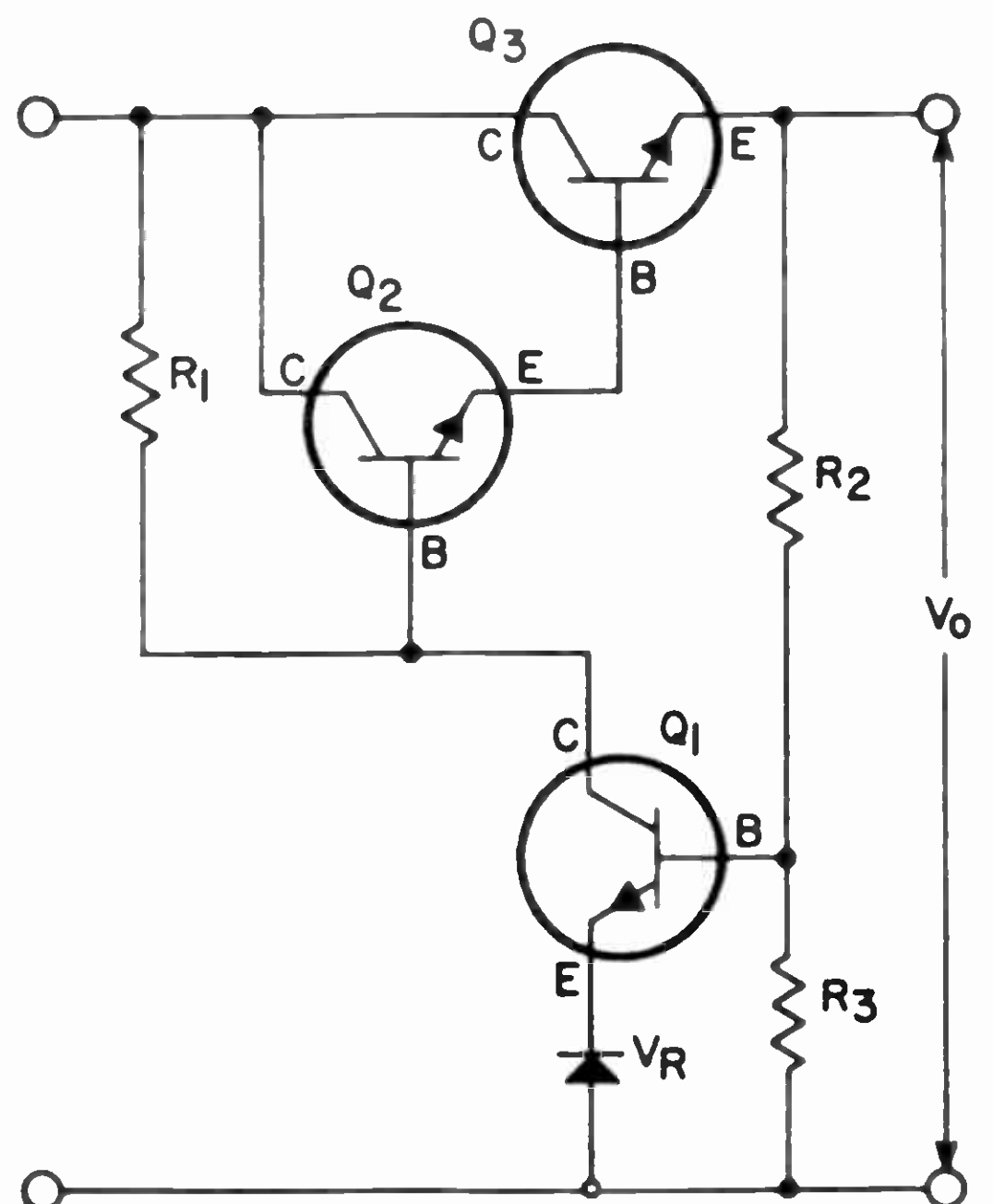
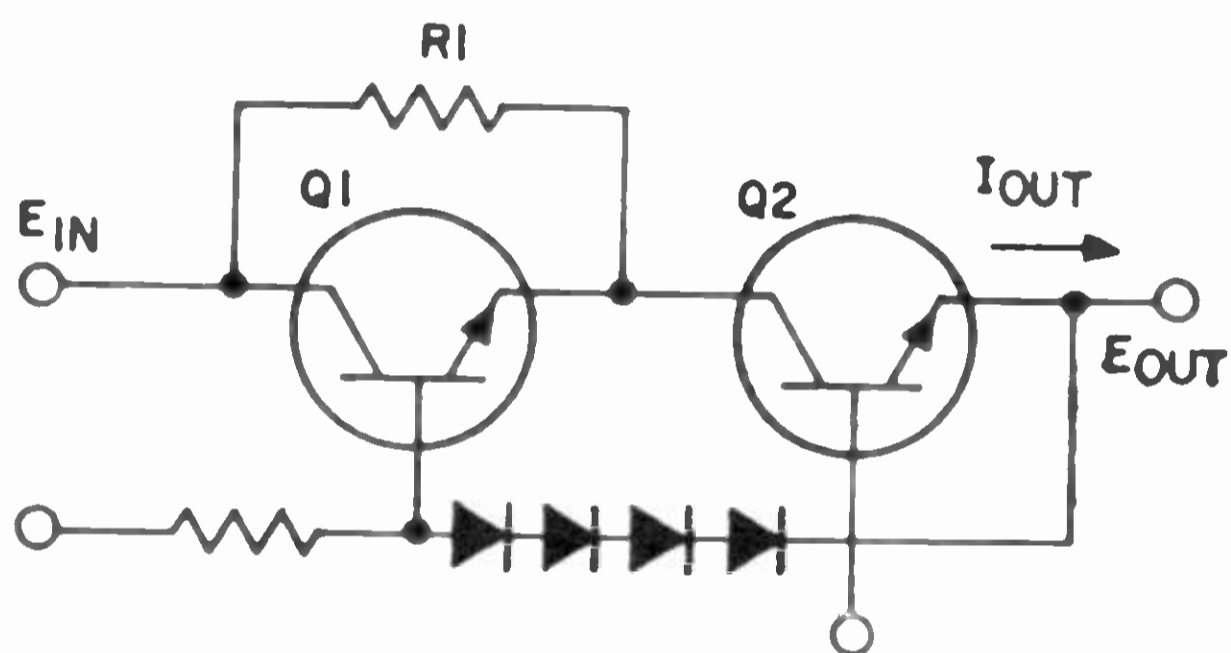


Fig. 311—Typical series regulator circuit.

tion of the output voltage and a reference source. The reference-voltage source V_R is placed in the emitter circuit of the amplifier transistor Q_1 so that the error or difference signal between V_R and some portion of the output voltage V_O is developed and amplified. The amplified error signal forms the input to the regulating element consisting of transistors Q_2 and Q_3 .

In many situations, a device for a high-voltage power supply is available with sufficient voltage capability but insufficient current dissipation or second-breakdown capability. The series-regulator circuit shown in Fig. 312 solves this problem by reducing the dissipation and current requirements in the high-voltage device Q_1 .



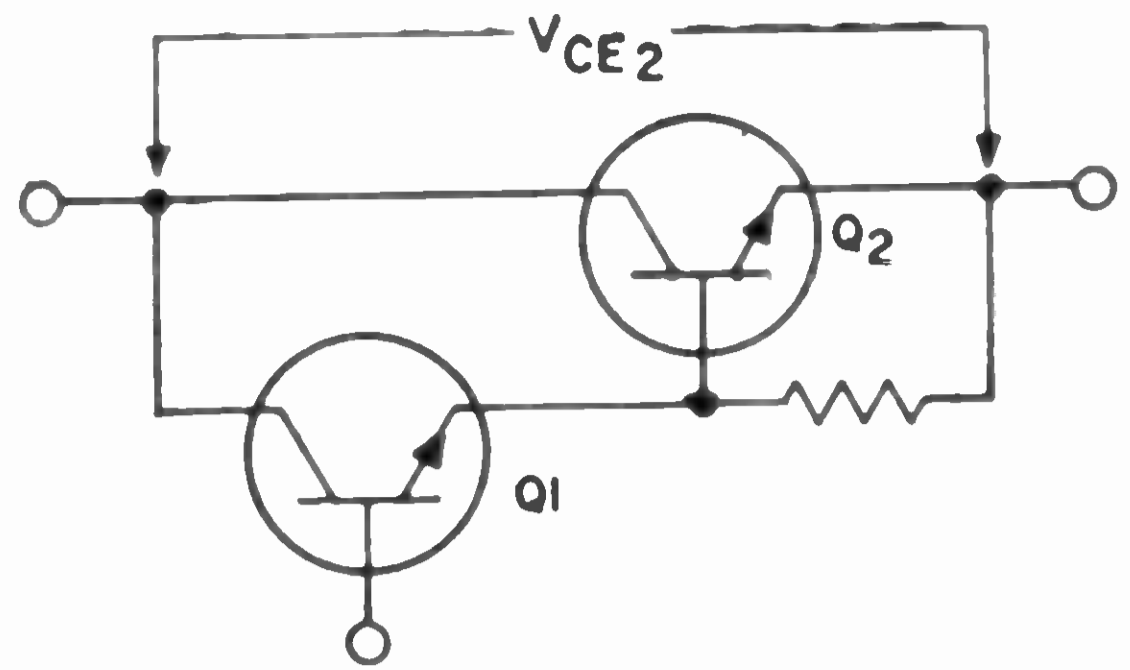
$$P_{Q1 \max} = P_{Q2 \max} = \frac{E_{\max} I_{\max}}{4}$$

$$R_1 = \frac{E_{IN}(\max)}{I_{OUT}(\max)}$$

Fig. 312—Series-regulator circuit using series matching.

In the circuit of Fig. 312, the maximum power dissipated in Q_1 or Q_2 is approximately one-fourth of the power that would be dissipated in a conventional series-pass stage. The balance of the power is dissipated in resistor R_1 .

In many high-current applications including series regulators, a Darlington configuration is utilized to improve the current gain, as shown in Fig. 313. A serious limitation of this method, however, is the high power dissipated in the pass element because this device cannot reach saturation.



$$h_{FE}(\text{TOTAL}) = h_{FE1} + h_{FE2} + h_{FE1} h_{FE2}$$

$$V_{CE2} = V_{CE1} + V_{BE2}$$

Fig. 313—Darlington configuration.

A typical automobile voltage-regulator circuit for an auto with a 12-volt system is shown in Fig. 314. Transistor Q_2 presents a variable resistance in series with the field. If the battery is fully charged and the electrical loading is small (e.g., only from the ignition circuit), the 10-volt zener diode breaks down, turning Q_1 on and Q_2 off (i.e., high resistance). The consequent reduction in field current reduces the armature voltage E_A so that the

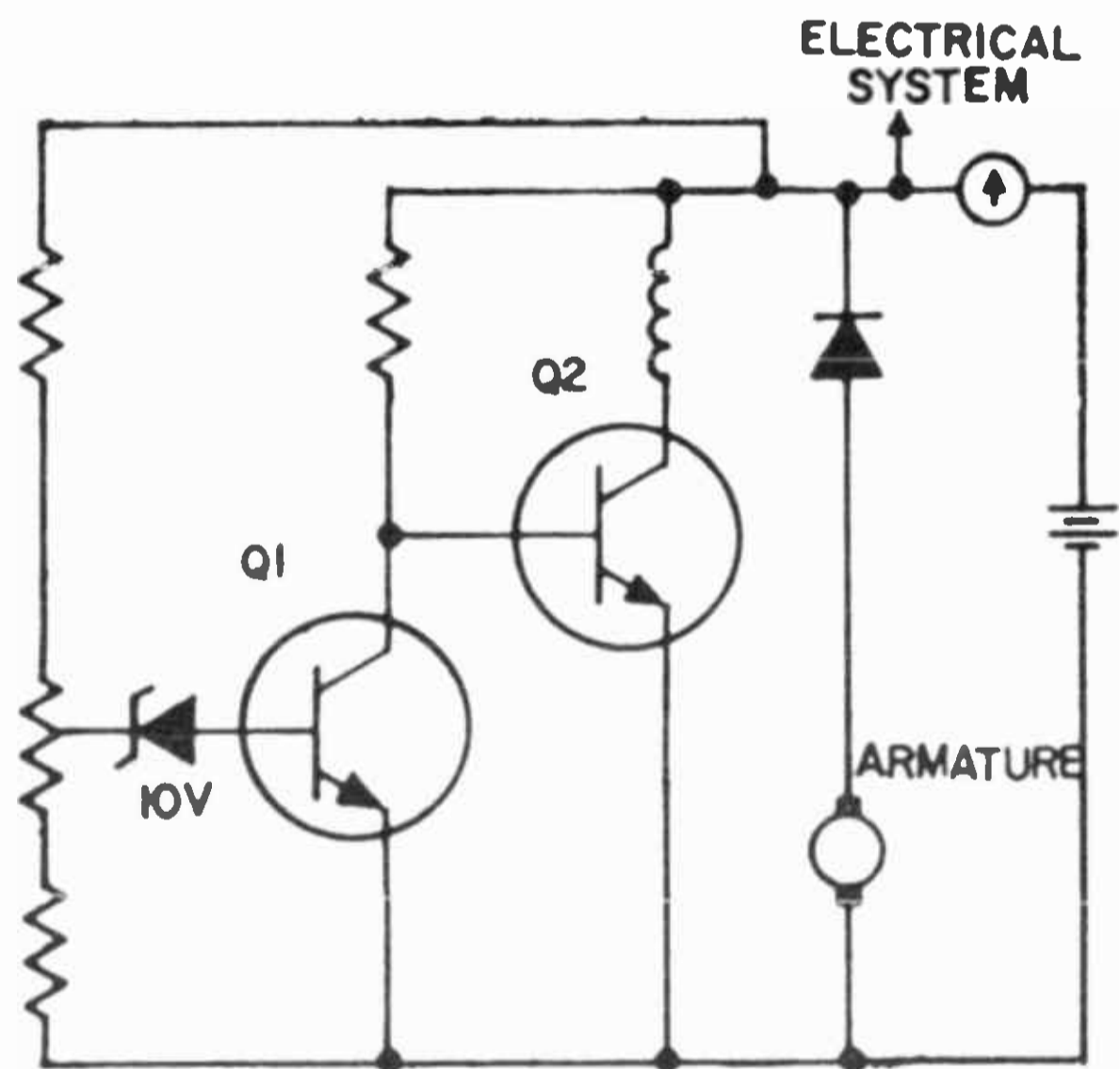


Fig. 314—Typical automobile voltage-regulator circuit.

battery supplies the load current. If the battery requires charging, or if the electrical load is heavy, then the lower terminal voltage is not sufficient to break down the zener. For this condition, Q_1 is off and Q_2 is on full (i.e., driven into saturation). As a result, field current is high, the armature voltage is high, and the alternator supplies current to the load and also charges the bat-

tery. Under normal operation, the transistor may be fully on, fully off, or somewhere in between (i.e., on but in the active region rather than in saturation). The actual transistor operating conditions depend on battery condition and electrical load.

Shunt regulator circuits are not as efficient as series regulator circuits for most applications, but they have the advantage of greater simplicity. In the shunt voltage regulator circuit shown in Fig. 315, the current through the shunt element consisting of transistors Q_1 and Q_2 varies with changes in the load current or the input voltage. This current variation is reflected across the resistance R_1 in series with the load so that the

output voltage V_0 is maintained nearly constant.

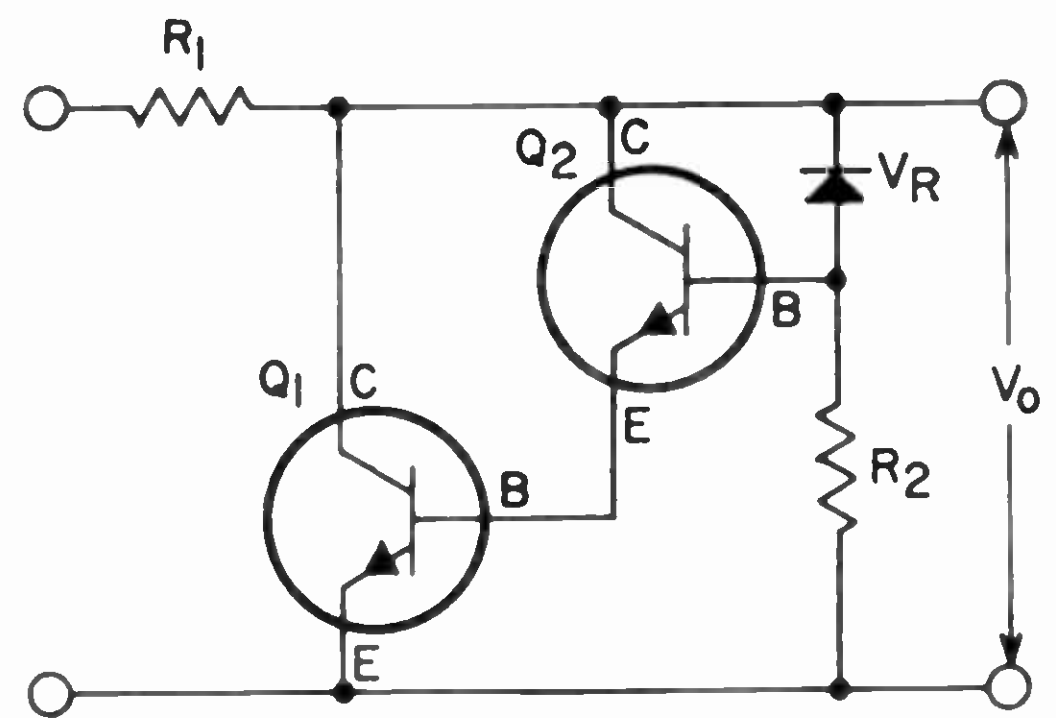


Fig. 315—Typical shunt-regulator circuit.

A third type of regulator, the switching regulator, is discussed in the section on Power Switching and Control under the heading of "Switching Regulators."

Testing and Mounting

This section covers the testing and installation suggestions which are generally applicable to all types of semiconductor devices. Careful observance of these suggestions will help experimenters and technicians to obtain the best results from semiconductor devices and circuits.

TESTING

The ability to determine the condition of semiconductor devices is an important requisite for servicemen, experimenters, and others who are required to operate and maintain electrical equipment that employ such devices. Although thorough, comprehensive evaluations of semiconductor devices are hindered by the limited amount of commercially available test equipment, simple techniques and circuits can be readily devised to provide go/no-go type of indications or to measure significant characteristics of the devices. The following paragraphs outline various test methods, indicate some of the available test equipment, and describe simple test circuits that may be constructed for use in the test and evaluation of different types of semiconductor devices.

Bipolar Transistors

Fig. 316 shows a go/no-go test circuit for bipolar transistors. The connections shown are for an n-p-n transistor. When the base resistor is connected to the negative terminal of the battery, the lamp should go out. For p-n-p transistors, the same results should be obtained with the battery polarities reversed.

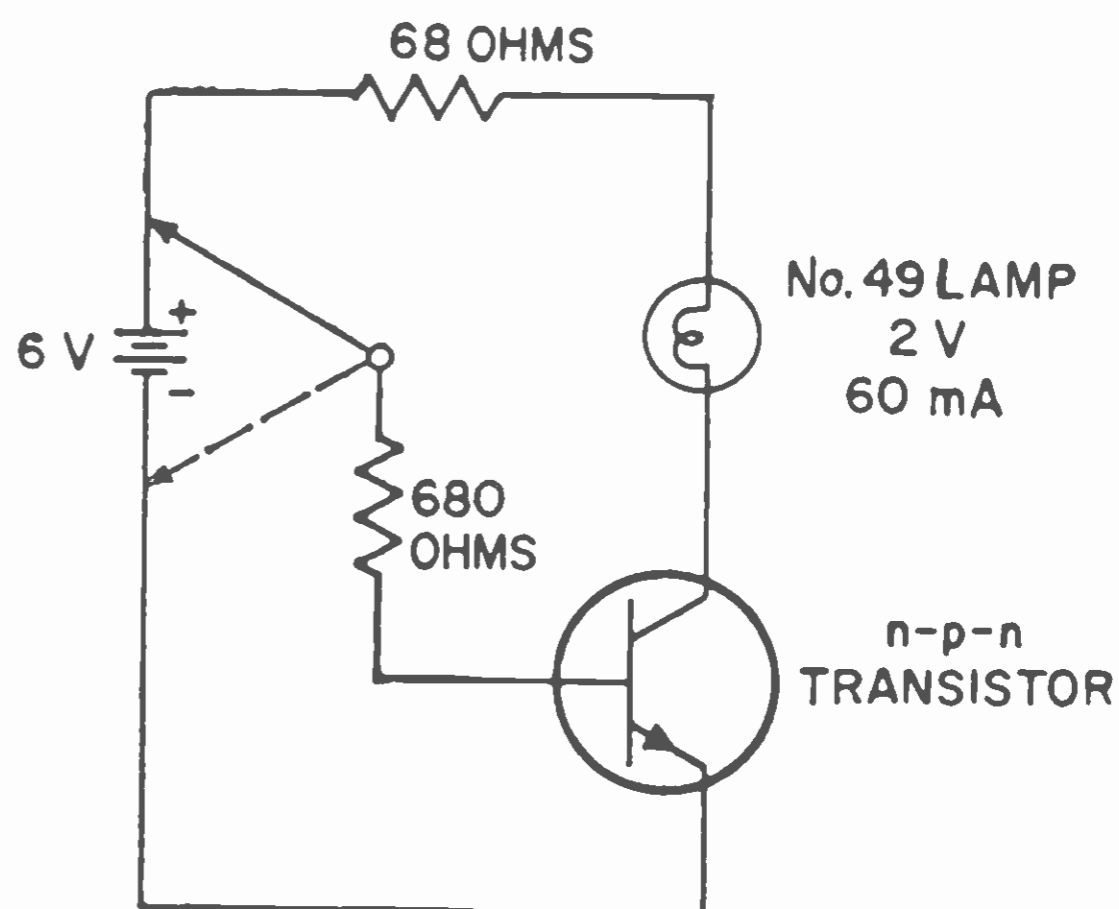


Fig. 316—"Go/no-go" test circuit for bipolar transistors.

A quick check of bipolar transistors can also be made prior to their installation in a circuit by resistance measurement with a conventional ohmmeter. The resistance between any two electrodes should be very high (more than 10,000 ohms) in one direction and considerably lower in the other direction (100 ohms or less between emitter and base or collector and base; about 1000 ohms between emitter and collector). It is very important to limit the voltage applied by the ohmmeter in such tests (particularly between emitter and base) so that the breakdown voltages of the transistor will not be exceeded; otherwise, the transistor may be damaged by excessive currents.

In addition to the test to determine open or shorted elements described above, any comprehensive evaluation of bipolar transistors must include measurements of the two most important transistor characteristics, beta and leakage. Commercial transistor testers are available to perform these measurements. Because there is no efficient substi-

tute way to evaluate these characteristics, a transistor tester is a worthwhile instrument for use in the servicing of equipments that employ bipolar transistors.

The value of a transistor tester for such work, however, depends on its design and how it is used. For accurate measurements of a wide range of transistor types, the tester must incorporate several specific design features. In addition the user must know a few facts about in-circuit and out-of-circuit measurements of transistor characteristics.

Beta Measurements—The beta, or common-emitter forward-current transfer ratio (h_{fe}), of a bipolar transistor expresses the gain characteristics of the device. This characteristic can be determined by use of ac or dc test voltages. Some basic factors that must be considered for transistor beta measurements are as follows:

1. The collector current level has a direct effect upon beta, whether the transistor is tested in or out of circuit. The published data for most transistors denotes the dc beta for specific conditions of dc voltage and temperature. The practical significance this characteristic has to troubleshooting is that a single level of collector current will not provide an adequate beta measurement for all types of transistors. Therefore, a transistor tester which provides for setting the collector current over a wide range of values will be better able to test diverse transistor types, such as small-signal rf and high-power audio transistors.

2. AC beta is a function of frequency. The gain-bandwidth product is the frequency at which the beta is equal to unity, and indicates the approximate useful frequency range of the device. The frequency-cutoff point is the frequency at which the alpha (common-base forward current-transfer ratio) drops to 0.707 times its 1-kHz value. These cutoff points vary widely with transistor types. In many consumer applica-

tions, transistors are now operating at frequencies up to 1,000 MHz. Significant tests of the frequency characteristics require elaborate rf measuring facilities. Consequently, it is not practical to include them in service-type transistor testers. It is apparent that an ac-beta tester which uses only a 60- or 1,000-Hz test signal cannot provide a significant indication of transistor performance at rf, vhf, or uhf frequencies.

3. The transistor beta specified by manufacturers for most transistors is a dc beta. AC beta figures are usually reserved for rf and higher-frequency types. In many of the latter cases, the dc beta is also specified.

4. If a transistor has insufficient current gain, its condition will be disclosed by either a dc- or an ac-beta test. Unlike electron tubes, transistors do not exhibit gain slumps due to materials depletion. In addition, beta does not normally change as the transistor ages. A defective transistor can be readily detected because it will have little or no beta, will give a shorted or open indication, or will have excessive leakage.

5. In-circuit beta readings will be lower than out-of-circuit readings for the same transistor. Variations will depend on the circuit resistance. In most cases, these differences will not be substantial. In some in-circuit tests, however, meaningful beta readings cannot be obtained because of low circuit resistances. The horizontal-deflection output stage of a TV receiver is a good example. In such situations, it will be necessary to test the transistor out of circuit.

6. In most applications, a reference beta figure for an in-circuit or out-of-circuit transistor may not be available for several reasons:

- (a) "Good" transistors of any one type may display a very wide spread in betas and still be acceptable for use in a specific circuit.

- (b) In-circuit beta may be affected by circuit configurations and operating parameters.

(c) The beta figure published by manufacturers is usually the average, or design center, of a very large number of tested devices.

(d) Equipment service notes do not specify reference beta figures for in-circuit measurements for the reasons given above. In spite of these factors, interpretation of beta measurements and their significance is not a guessing game. A defective transistor will have little or no beta, will cause the pointer to slam against the meter stop of the tester, or will make it impossible to calibrate the tester prior to beta measurements. It would appear, then, that discrete beta values have little significance in service work. In most applications, however, a minimum gain characteristic is needed, and it is often necessary to "pair up" transistors for complementary-symmetry circuits in various types of equipment, including audio amplifiers of radio and television receivers.

7. A transistor with a low beta (or excess leakage) may be satisfactory for use in noncritical circuits. It is necessary, therefore, to consider test results in terms of the application. For example, a transistor having a low beta may be satisfactory in some audio-amplifier circuits but not usable in a small-signal rf circuit. A transistor having high leakage may be acceptable in an audio stage but be useless in a high-frequency circuit.

Leakage Measurements—Collector-to-base leakage (I_{CBO}), measured with the emitter open, is the critical leakage of both germanium and silicon transistors. However, these two basic transistor types can display wide differences in their leakage values and in levels of acceptability.

A transistor tester should measure leakage directly in milliamperes or microamperes. Some factors to be considered when interpreting measurement results and levels of I_{CBO} acceptability are as follows:

1. I_{CBO} limits for any particular transistor type are usually speci-

fied in general data or in equipment service notes.

2. A transistor having a given amount of leakage may be usable in some applications and not in others.

3. Silicon transistors generally have much lower leakage than germanium types.

4. I_{CBO} of most small-signal silicon transistors will be less than one microampere.

5. Some acceptable silicon power transistors may have an I_{CBO} as high as 50 microamperes.

6. The I_{CBO} of most germanium transistors will be less than 100 microamperes.

7. Germanium power transistors often have an acceptable I_{CBO} of several milliamperes.

8. Leakage measurements can be made only with the transistor out of the circuit.

Transistor Tester—The beta- and leakage-measurement considerations discussed above indicate that a transistor tester must include several specific features to be a reliable measurement device. The more important considerations are as follows:

1. The capability to measure beta at the collector-current level best suited to the transistor type or its application. This capability should extend to the handling of devices ranging from small-signal rf transistors that have nominal collector currents of a few milliamperes to high-power types that have ratings up to one ampere.

2. The facility to provide beta readings with an accuracy of $\pm 5\%$ both in and out of circuit. (It should be remembered, however, that beta is directly affected by the collector current.)

3. An adjustment which permits leakage currents to be "bucked out" before the beta measurement is made; otherwise, the beta reading may be upset by the leakage current. In the case of high-leakage germanium power transistors, the resultant beta reading may be sig-

nificantly inaccurate. This rule applies to both in-circuit and out-of-circuit tests.

4. Means for calibrating the beta test for each transistor tested.

5. A facility for reading leakage current directly in values as low as one microampere.

The considerations listed above define the primary requirements of a good transistor tester. Other features are desirable, of course, to make the tester completely reliable and easy to use.

All of the necessary and desirable features have been included in the new RCA WT-501A Transistor Tester, a measurement instrument that combines service speed and simplicity with laboratory-measurement qualities. Fig. 317 shows the overall schematic and Fig. 318 shows a photograph of the WT-501A tran-

sistor tester. This tester is designed to measure transistor collector-to-base leakage (I_{CBO}), collector-to-emitter leakage (I_{CEO}), and dc beta. Collector current (I_C) is continuously adjustable up to 1 ampere in four ranges. The WT-501A can also be used for in-circuit beta tests of a transistor.

A 100-microampere meter movement is used in the measuring circuits for the various test functions. Precision resistors are used to insure accurate test results.

An N-P-N/P-N-P switch provides the proper bias polarity to the transistor. Two dual potentiometers provide coarse and fine adjustment of collector current (CAL) and in-circuit zero.

The instrument has two internal 1.5-volt "D"-size batteries. One battery is used in n-p-n tests and the

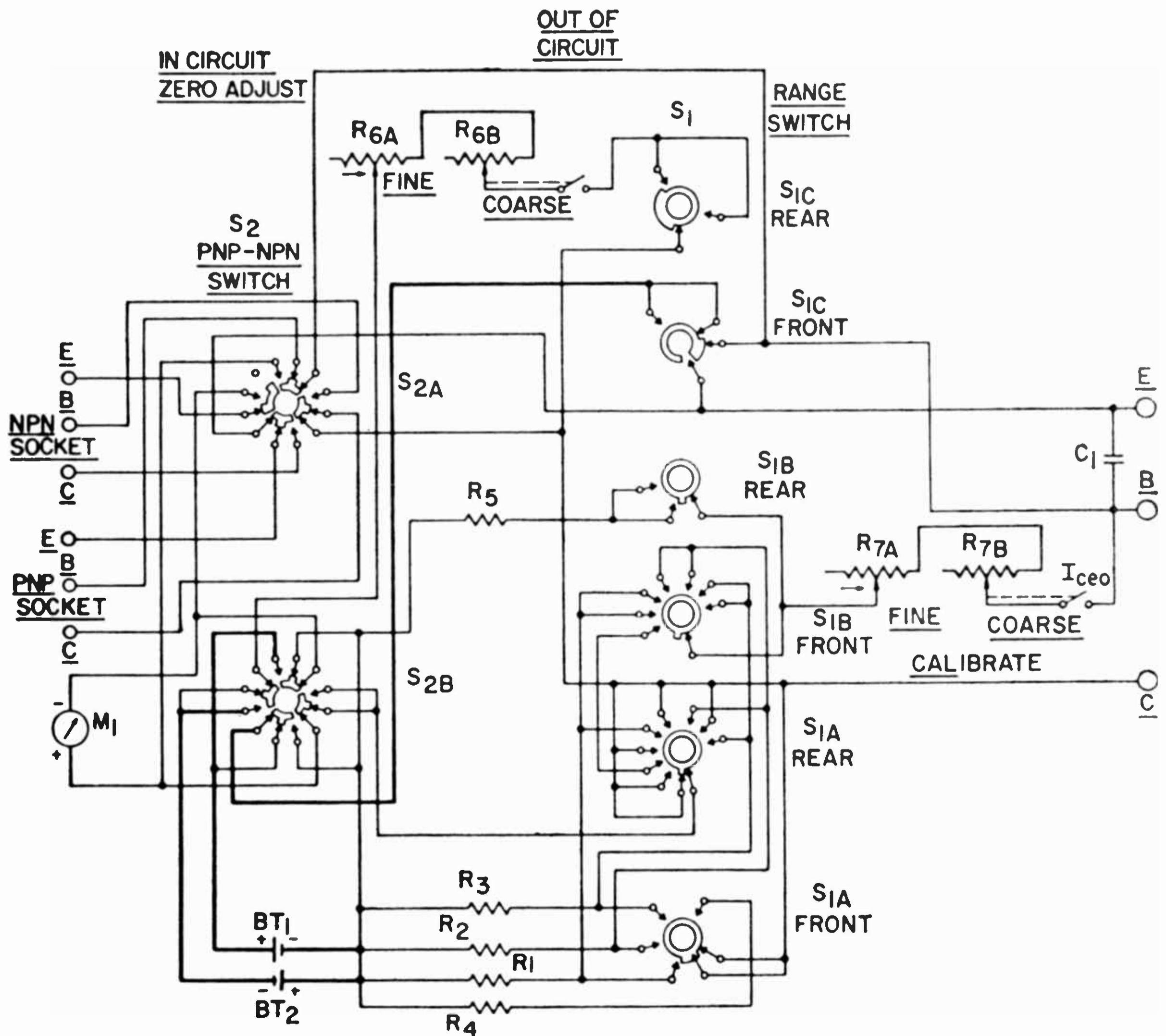


Fig. 317—Circuit diagram for RCA WT-501A transistor tester.



Fig. 318—RCA WT-501A transistor tester.

other is used in p-n-p tests. The batteries are also used during in-circuit tests to provide voltage in reverse polarity to cancel the effect of circuit leakage.

Beta-measuring circuit: A simplified diagram of the dc-beta test circuit is shown in Fig. 319. Resistors R_b and R_c serve both to establish

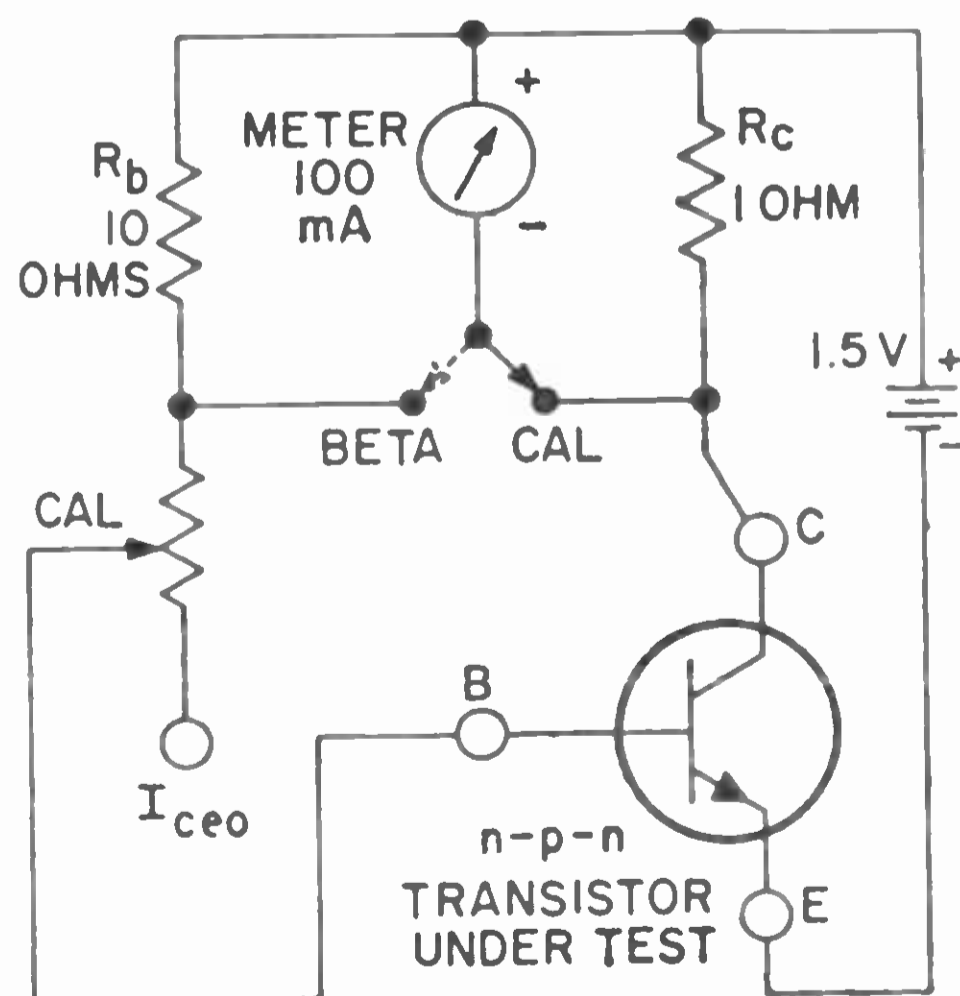


Fig. 319—Simplified beta-measuring circuit for 0-to-100-milliamperere range.

the collector current, and to shunt the meter to the required sensitivity. Values for R_b and R_c are as follows:

Range	R_b	R_c
1 mA	1000 ohms	110 ohms
10 mA	110 ohms	10 ohms
100 mA	10 ohms	1 ohm
1 A	1 ohm	0.1 ohm

When the range switch is set to the CAL function, the meter is in the collector circuit. Collector current is determined by the value of the collector resistor for the particular range, and by the setting of the CAL control.

In the BETA function, the meter is switched to the base circuit. DC beta is defined as the ratio of the steady-state collector current to the base current. Because the collector current is established at a known value by the CAL adjustment, the base-current meter reading can be interpreted in terms of dc beta for the transistor.

I_{CBO} measuring circuit: I_{CBO} is the current flow, or leakage, from the collector to the base with the emitter open. As shown in Fig. 320, 1.5 volts is applied to the collector and base of the transistor, and the

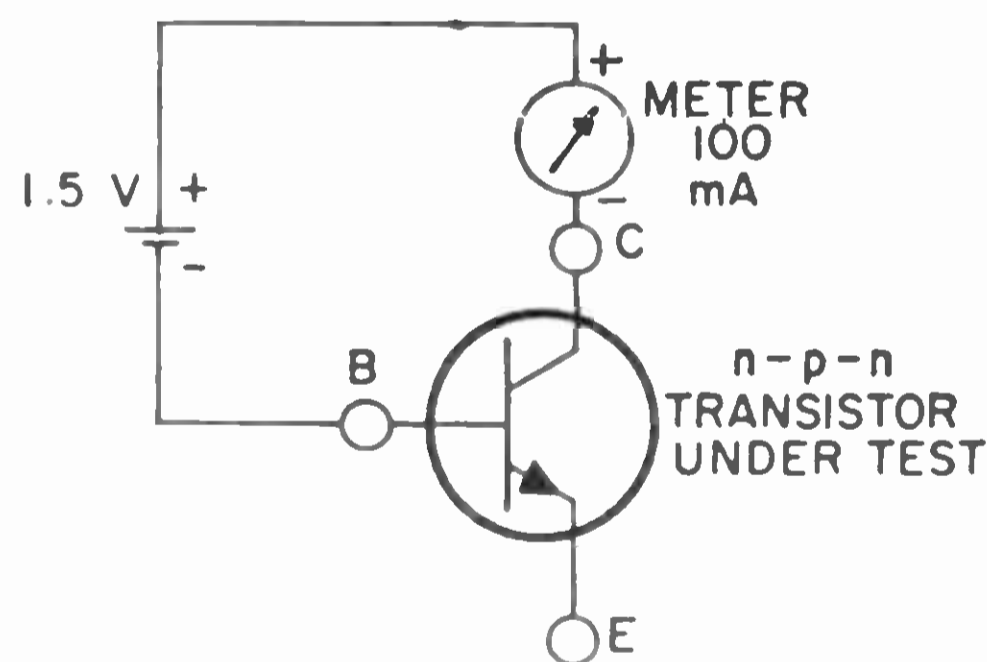


Fig. 320—Simplified I_{CBO} test circuit.

meter is connected in the collector circuit. Collector-to-base leakage is indicated directly in microamperes.

I_{CEO} measuring circuit: I_{CEO} represents the leakage from collector to emitter, with the base open. Fig. 321 shows a simplified diagram of the I_{CEO} test circuit. A voltage of 1.5 volts is applied to the transistor, and the meter is connected in the collector circuit. The resistor shunting the meter reduces the meter sensitivity to 10 milliamperes.

Measurement of I_{CEO} is normally

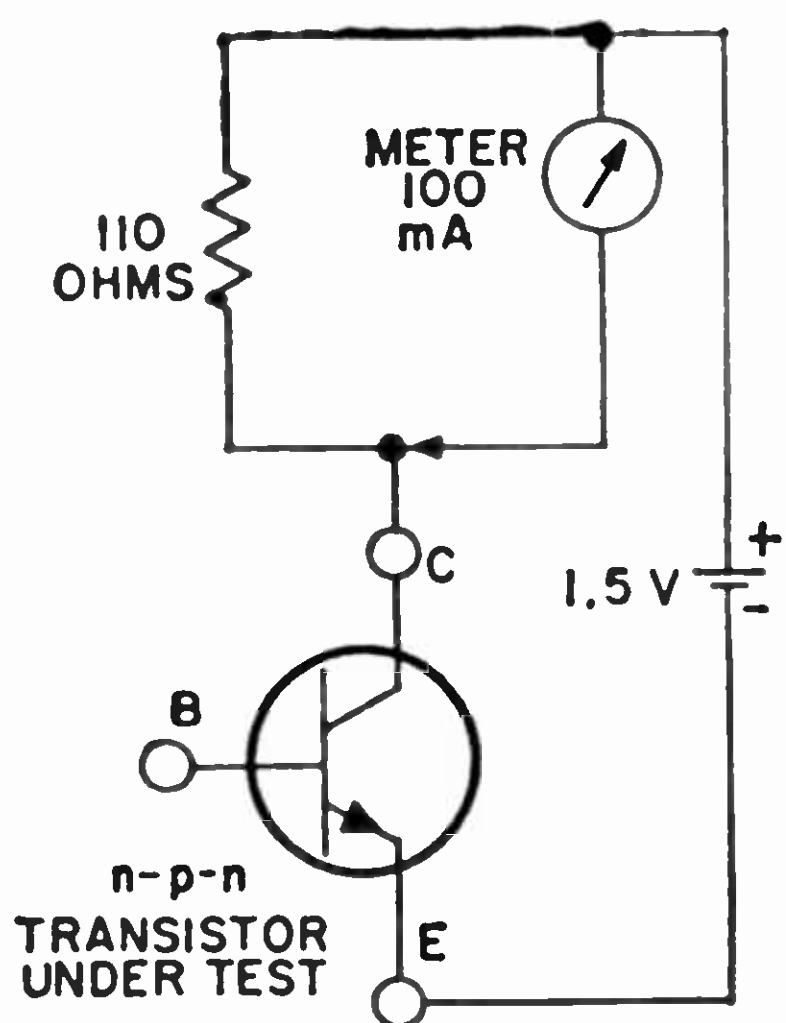


Fig. 321—Simplified I_{CEO} test circuit for 1-milliamperere range.

made on the CAL position of the 1-milliamperere range. If I_{CEO} exceeds 1 milliamperere, however, the range switch can be set to the 10-milliamperere or 100-milliamperere range as necessary. Collector-to-emitter leakage is indicated in milliampereres, depending on the current range that is used.

In-circuit beta test: The test circuit used to measure in-circuit current gain is similar to that used for out-of-circuit beta measurement. As shown in Fig. 322, the IN-CIRCUIT ZERO ADJUST control applies a voltage of reverse polarity

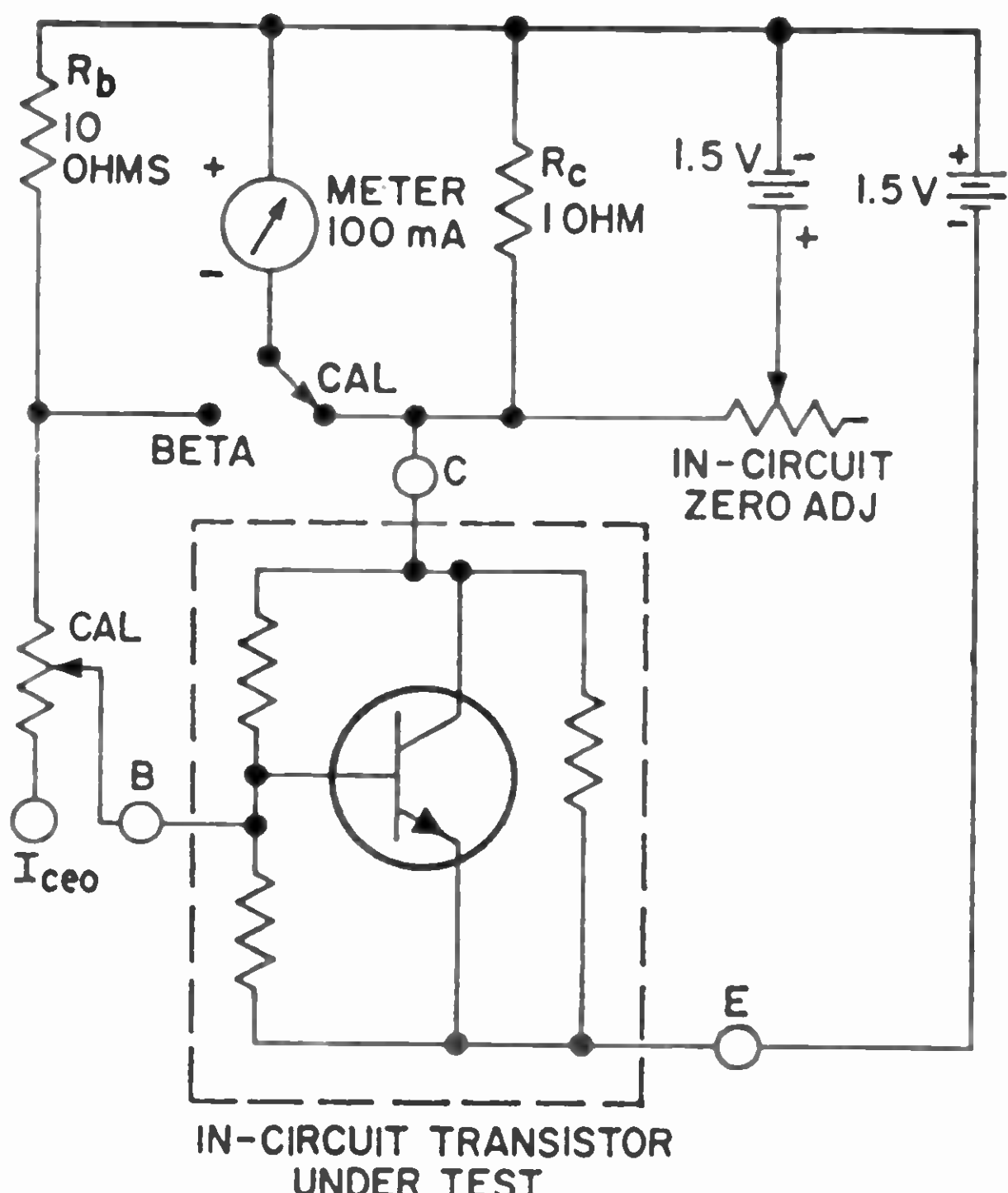


Fig. 322—Simplified in-circuit beta test circuit for 0-to-100-milliamperere range.

to the collector metering circuit. This voltage compensates for the collector-to-emitter leakage through the components in the circuit under test, and permits the meter to be set to zero.

The CAL adjustment and the metering circuit are the same as for out-of-circuit measurement.

The resistance of the measuring circuit is low in value so that no significant loading effect occurs from the circuit being tested.

MOS Transistors

In the servicing of electrical equipment that employs MOS transistors, it is readily determined that the test techniques required to measure the characteristics of these devices are not the same as those used for bipolar transistors. An entirely new set of techniques, aimed specifically at the unique properties of MOS transistors, is required. Simple go/no-go types of test circuits, however, may still be used for detection of open or shorted devices.

The test circuit shown in Fig. 323 can be used to test n-channel deple-

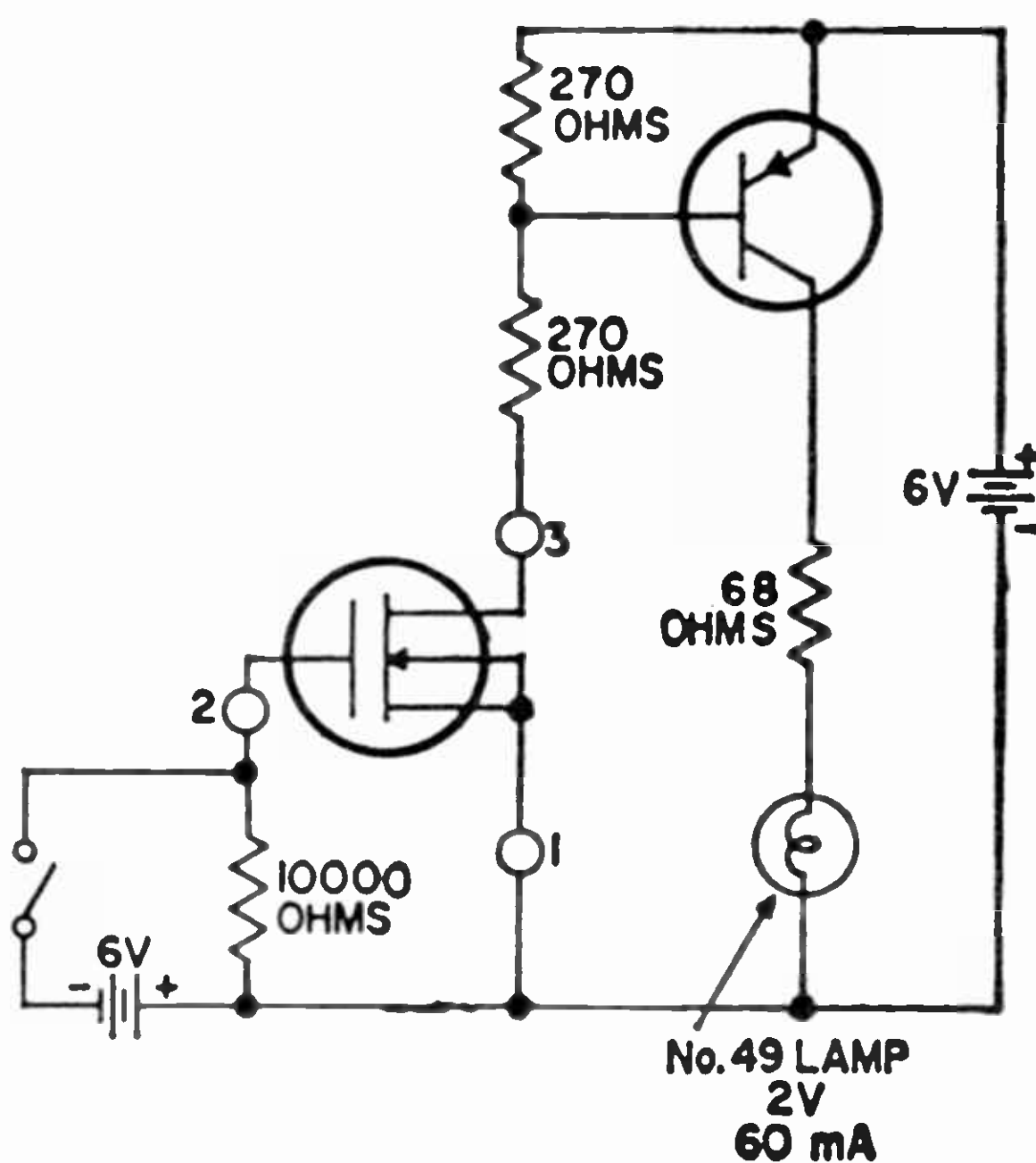


Fig. 323—"Go/no-go" test circuit for MOS transistors.

tion or p-channel enhancement MOS transistors for opens or shorts. The substrate and source of the device

being tested should be connected to terminal No. 1, the gate should be connected to terminal 2, and the drain should be connected to terminal No. 3. If the MOS transistor is a dual-gate type, the gates are tested separately. For n-channel depletion types, if the lamp lights when the switch is open and does not light when the switch is closed, the transistor is good. If the lamp lights with the switch in either position, the transistor is shorted. If the lamp remains off with the switch in either position, the transistor is open. For p-channel enhancement types, the reverse indications are obtained.

A complete, precise determination of the characteristics of MOS transistors, particularly at high frequencies, is best obtained by the combined use of a curve tracer and special measurement circuits. For normal troubleshooting tests of these devices, however, the approximate value of a number of MOS-transistor electrical parameters can be conveniently obtained from a sweep display of the corresponding static characteristics on a curve tracer. A commercial curve tracer, such as the Tektronix 575 or equivalent, is specifically designed to display a complete family of characteristics. Although designed for use with bipolar transistors (current amplifiers), this equipment can be used with MOS transistors (voltage amplifiers) if the base-step generator is modified to provide voltage steps instead of current steps.

This modification involves the connection of a 1000-ohm resistor between the base and emitter terminals of the curve-tracer transistor. Adjustment of the base-step generator to 1 milliampere per step (negative steps for n-channel devices) results in an incremental voltage of 1 volt per step being applied to the gate of the MOS transistor.

When a commercial curve tracer is not available, any low-frequency oscilloscope that has X and Y inputs and a vertical sensitivity of at

least 10 millivolts per division may be adapted to curve tracing by use of the special adapter circuit shown in Fig. 324. Although this method does not result in the complete fam-

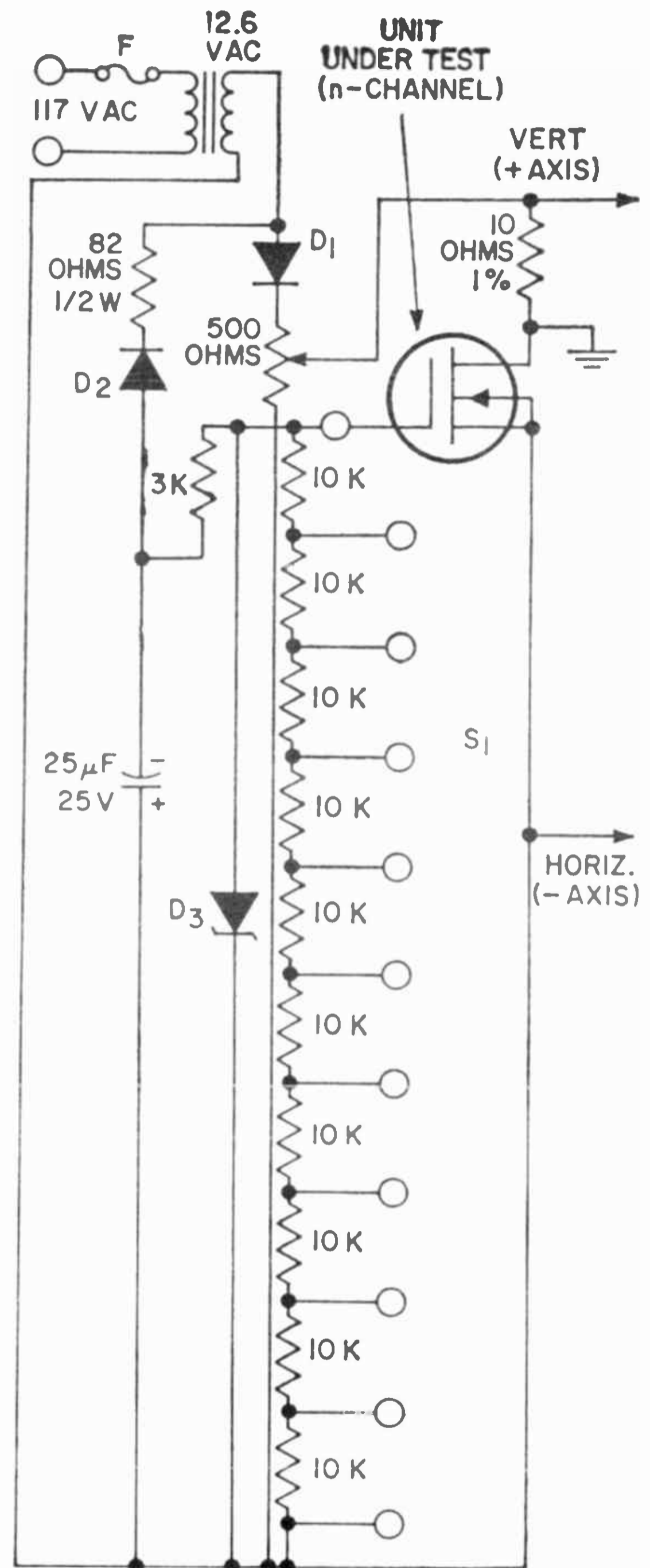
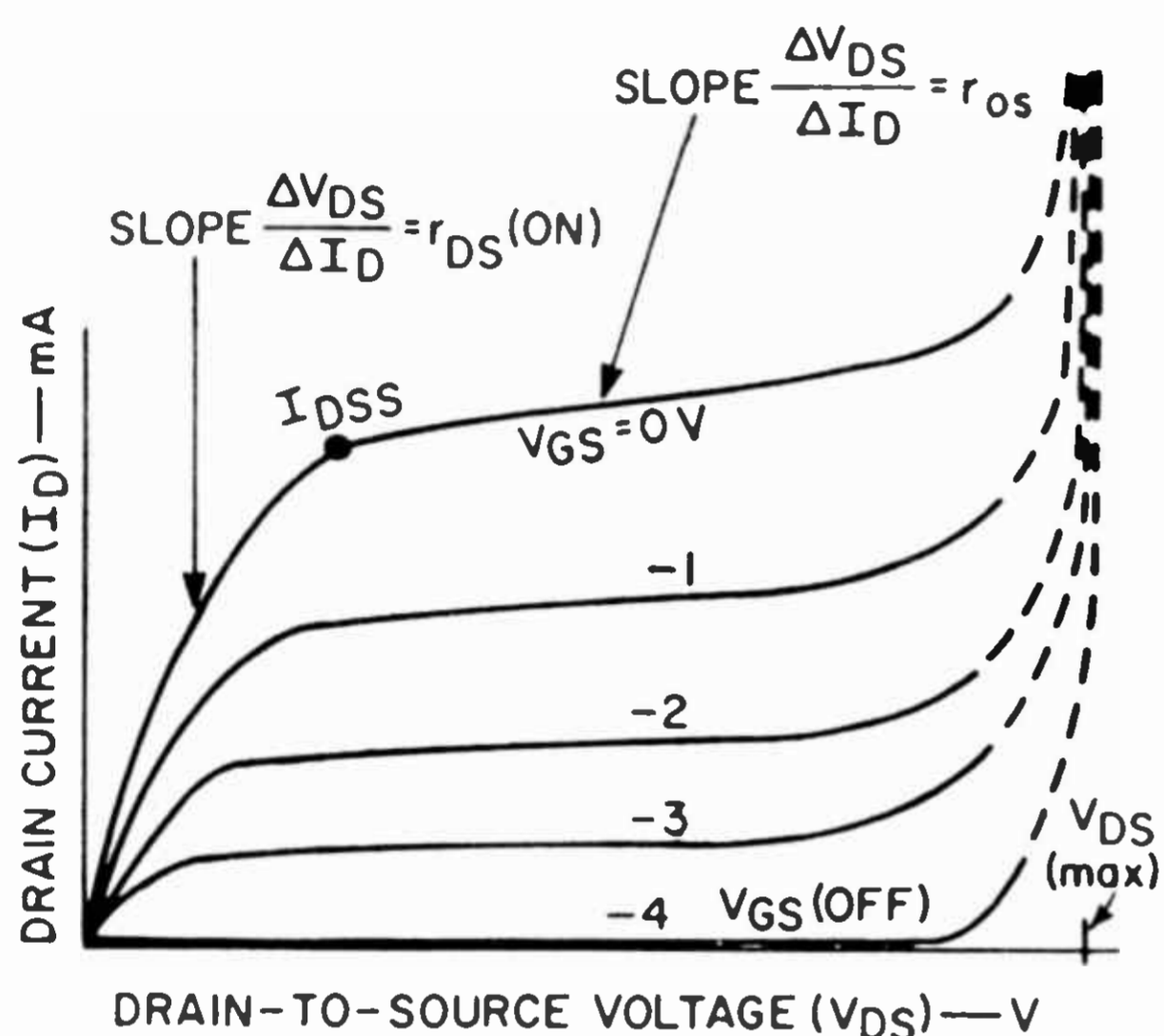


Fig. 324—Adapter circuit for tracing MOS-transistor curves on oscilloscope.

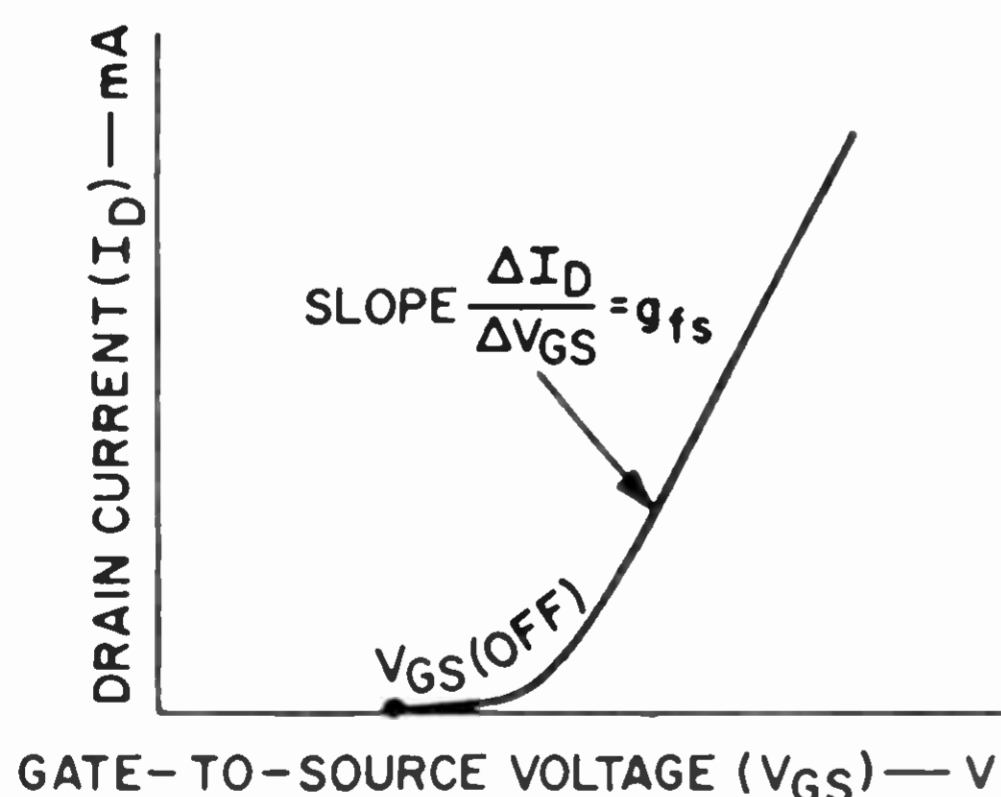
ily of curves being presented on the oscilloscope simultaneously, each curve may be displayed sequentially by turning the gate-bias switch, S_1 , on the adapter. This switch provides 10 different gate voltages from zero to -10 volts in increments of -1 volt per step.

The drain-current/drain-voltage family of curves and the drain-

current/gate-voltage curve obtained by use of the curve-tracer are shown in Fig. 325. Pinch-off voltage V_p (depletion-type MOS transistors) and zero-bias drain current I_{DSS} are read off the curves directly. The drain-to-source ON-resistance r_{ds} , the output resistance r_{os} , and the low-frequency transconductance g_{fs} are calculated from the slope of the curves. Although the maximum drain-to-source voltage V_{DS} appears on the output characteristics, V_{DS} should not be measured by this method because, in some cases, the maximum gate-to-drain voltage rat-



(a)



(b)

Fig. 325—MOS-transistor curves obtained by use of curve tracer.

ing may be exceeded. V_{DS} should therefore be limited in this method to the solid-line portions of the curves shown in Fig. 325(a).

It should be mentioned that personnel handling MOS transistors during testing should ground them-

selves, preferably at the hand or wrist. This precaution eliminates the possibility of large electrostatic voltages being applied to the device. A simple method of grounding oneself is to rest one hand on a grounded part of the test chassis when the transistor is handled.

Silicon Rectifiers

In general, silicon rectifiers and most other types of semiconductor diodes can be adequately tested by resistance measurements with a conventional ohmmeter (For procedures used in the testing of tunnel diodes, refer to RCA Tunnel Diodes, Technical Manual TD-30.) Resistance measurements are taken in both the forward and reverse directions. The ratio of the "reverse" resistance reading to the "forward" resistance reading should be greater than 10 to 1. For the forward-direction measurement, it is important to assure that the forward-voltage rating of the rectifier is greater than the voltage applied by the ohmmeter (the battery voltage of a conventional ohmmeter is 1.5 volts); otherwise, the rectifier may be damaged by excessive current. The front-to-back ratio of rectifiers can also be checked at various current levels with the RCA WT-501A Transistor Tester described in the paragraph on testing of Bipolar Transistors.

There are a number of easily constructed go/no-go types of test circuits that may be used to detect open or shorted rectifiers. Several of these test circuits are shown in the following paragraphs.

Fig. 326 shows a simple "go/no-go" test circuit for silicon rectifiers operating at 120 volts. With the connection shown, the lamp operates at half-power. When the switch is closed, the lamp should brighten if the diode under test is good. If there is no change in brightness when the switch is closed, the lamp was burning at full power with the switch open; in this case, the diode is

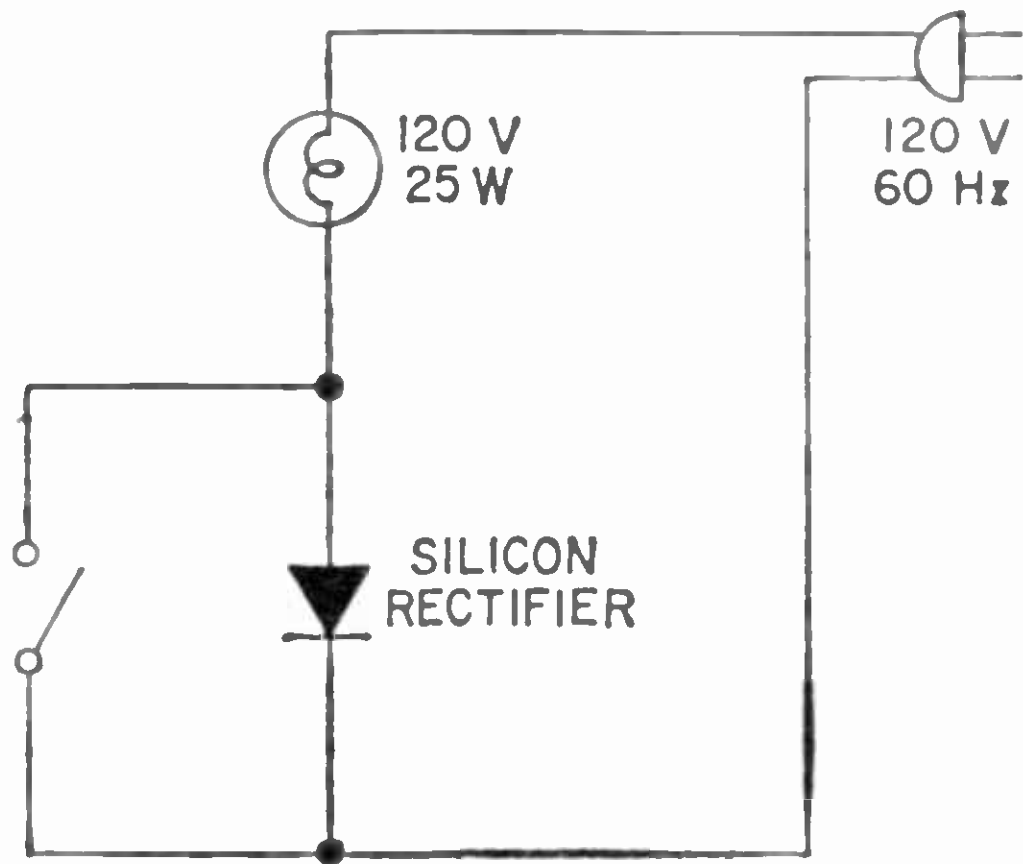


Fig. 326—"Go/no-go" test circuit for high-voltage silicon rectifiers.

shorted. If the lamp is out with the switch open but lights when the switch is closed, the diode is open.

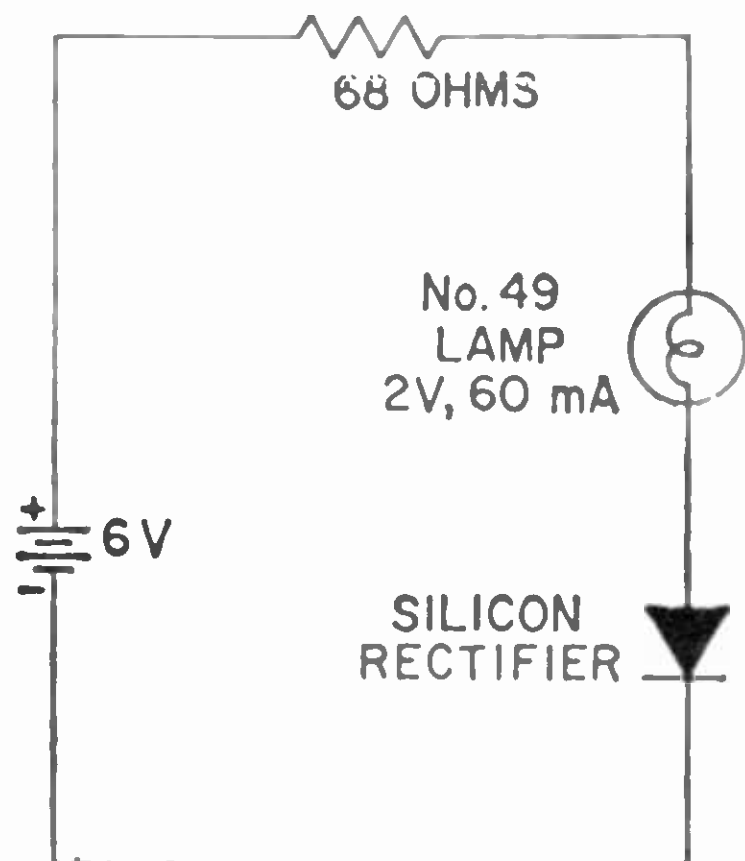


Fig. 327—"Go/no-go" test circuit for low-voltage silicon rectifiers excluding types 1N34A and 1N270.

Fig. 327 shows a "go/no-go" tester for all silicon rectifiers in this Manual that operate at low voltages

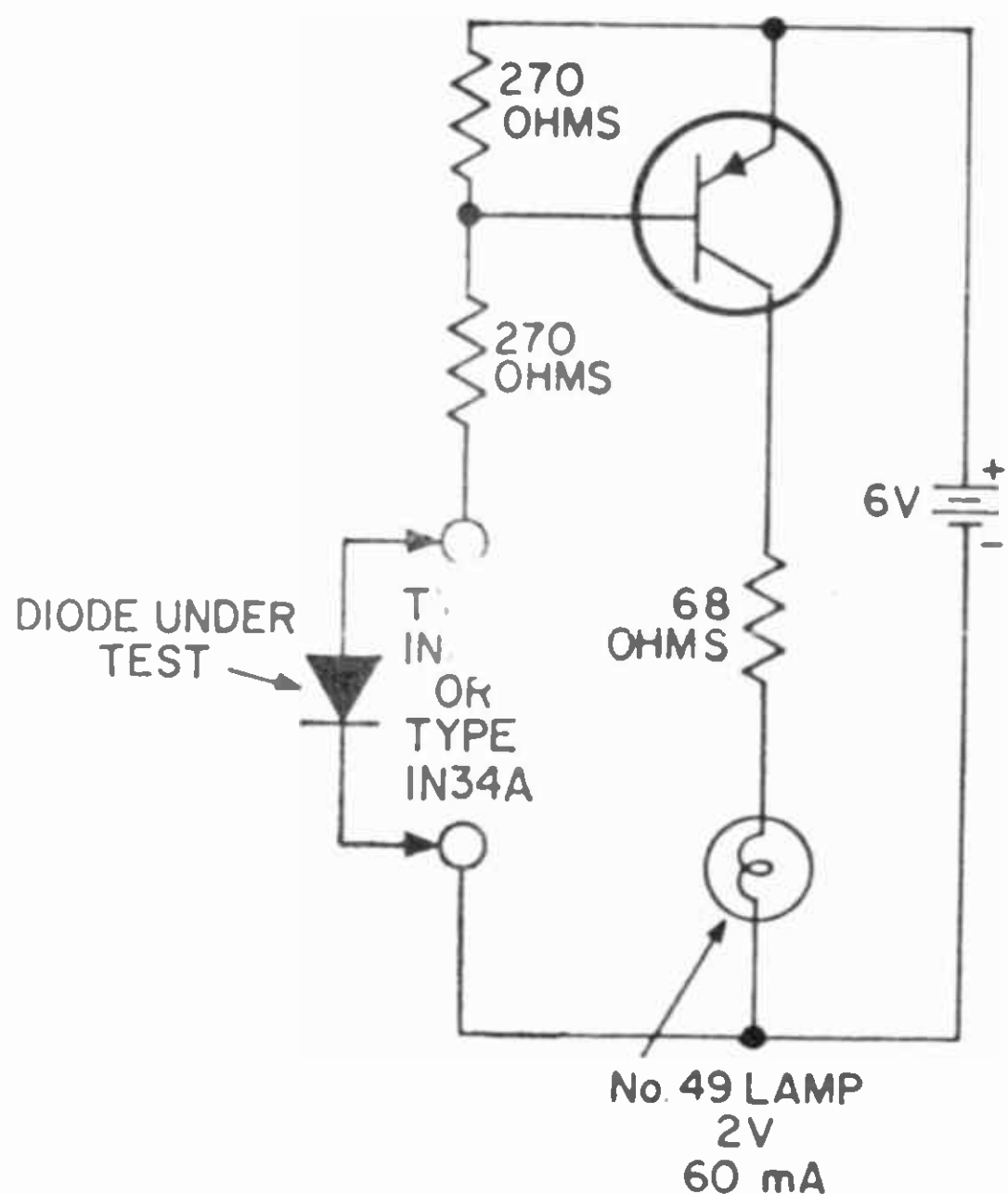


Fig. 328—"Go/no-go" test circuit for silicon rectifier types 1N34A and 1N270.

except the 1N34A and 1N270. The test circuit for these two types is shown in Fig. 328.

With a diode connected as shown in Fig. 327 and with the polarity of the battery as shown, the lamp should light; when the polarity of the battery is reversed, the lamp should not light. If the lamp lights regardless of the polarity of the battery, the diode is shorted; if the lamp does not light with either polarity, the diode is open.

When the anode of a 1N34A or 1N270 diode is connected to terminal No. 1 in Fig. 328, the lamp should light if the diode is good; when the anode is connected to terminal No. 3 the light should go off. If the light remains lit regardless of the connection, the diode is shorted; if the light is off regardless of the connection, the diode is open.

SCR's and Triacs

Similar test procedures and circuits may be used for testing SCR's and triacs. The triac, however, should be tested for operation in all four operating modes. For convenience of illustration, the test circuits described show only SCR's. Triacs tested in these circuits should be connected in one direction and then reversed for each test. In addition, the triacs should be tested for both negative and positive gate signals for each direction in which they are connected.

Fig. 329 shows a go/no-go type of test circuit that can be used to test thyristors that operate directly from the line voltage. When the switch is closed, a current of approximately 20 milliamperes flows through the 25-watt lamp, the 5600-ohm resistor, and the switch; this amount of current is not enough to light the lamp. When the switch is opened, the light should brighten to approximately half maximum brightness. Under these conditions, the SCR should be triggered into operation (shunting the 5600-ohm resistor) on each positive half-cycle of input by the 20-milliamper current

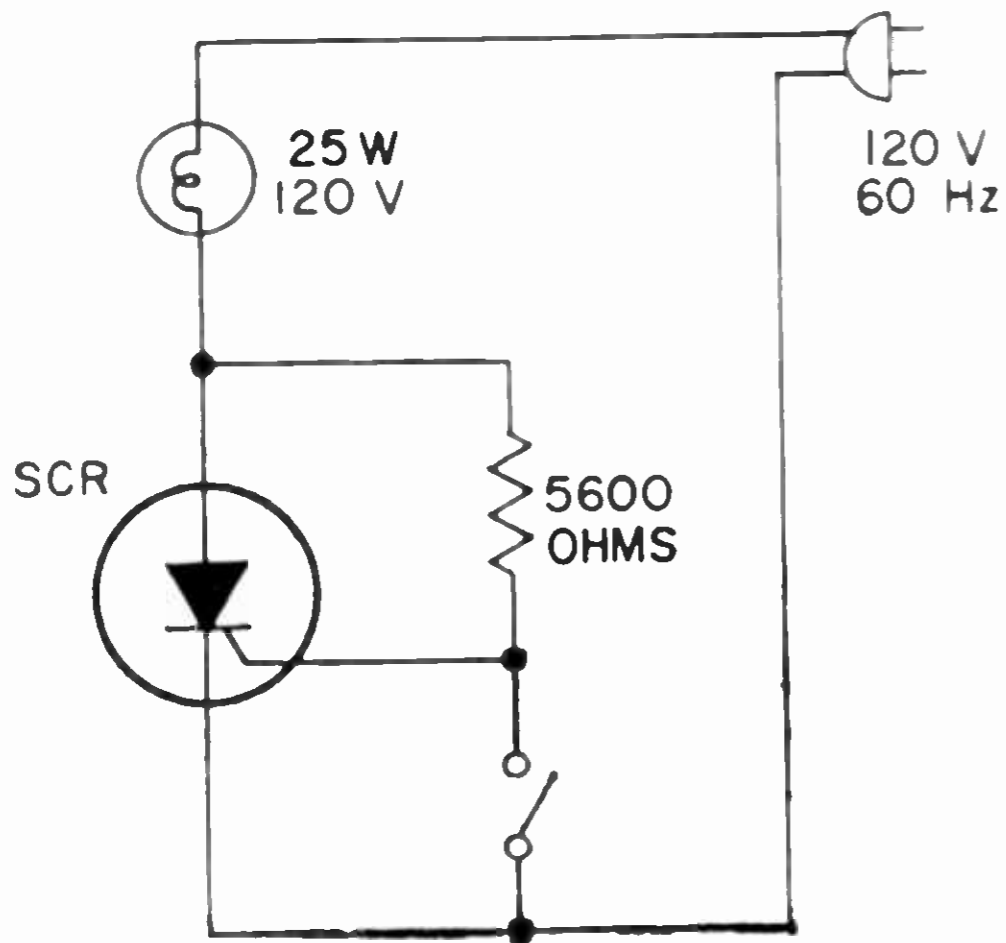


Fig. 329—Simple test circuit for SCR's.

flowing in the gate-cathode circuit. If the lamp lights to full brightness, the SCR is shorted. If the lamp does not brighten regardless of the position of the switch, the SCR is open.

Fig. 330 shows a simple, inexpensive test circuit that may be used to evaluate the OFF-state voltage capabilities of thyristors, and for reverse-blocking (SCR's) and

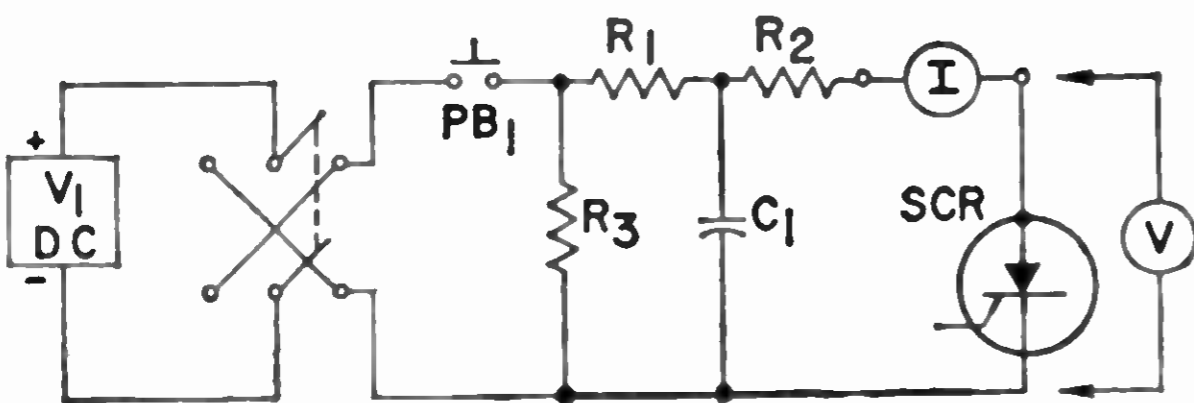


Fig. 330—Test circuit used to determine dc forward- and reverse-voltage-blocking capabilities and leakage current of thyristors.

leakage tests. Resistor R_1 and capacitor C_1 are included in the test circuit to limit the rate of rise of applied voltage to the thyristor under test. Resistor R_2 limits the discharge of capacitor C_1 through the thyristor in the event that the thyristor is turned on during the test. Resistor R_3 provides a discharge path for capacitor C_1 .

Fig. 331 shows a simple test circuit that may be used to determine the holding and latching currents of thyristors. For the holding-current tests, the value of potentiometer R_1 is adjusted to approximately 50 ohms, and the spring-loaded push-button switch PB_1 is momentarily depressed to turn on the thyristor. The value of R_1 is

then gradually increased to the point at which the thyristor turns off.

For the latching-current test, the value of potentiometer R_1 is initially adjusted so that the main-terminal current is less than the holding level. The value of R_1 is then decreased, as push-button switch PB_1 is alternately depressed and released, until the thyristor latches on.

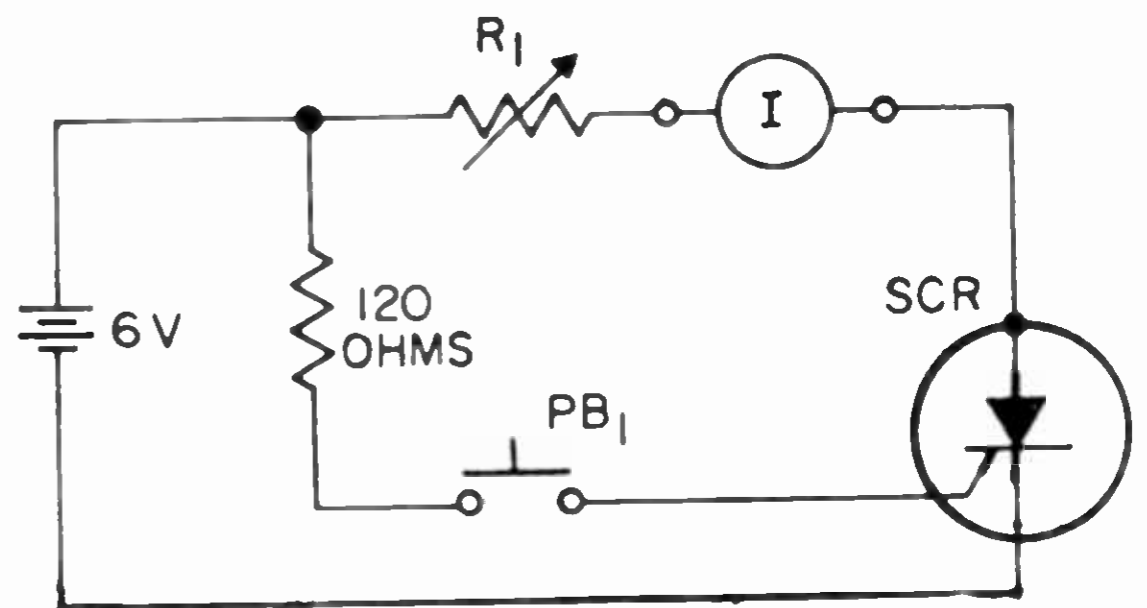
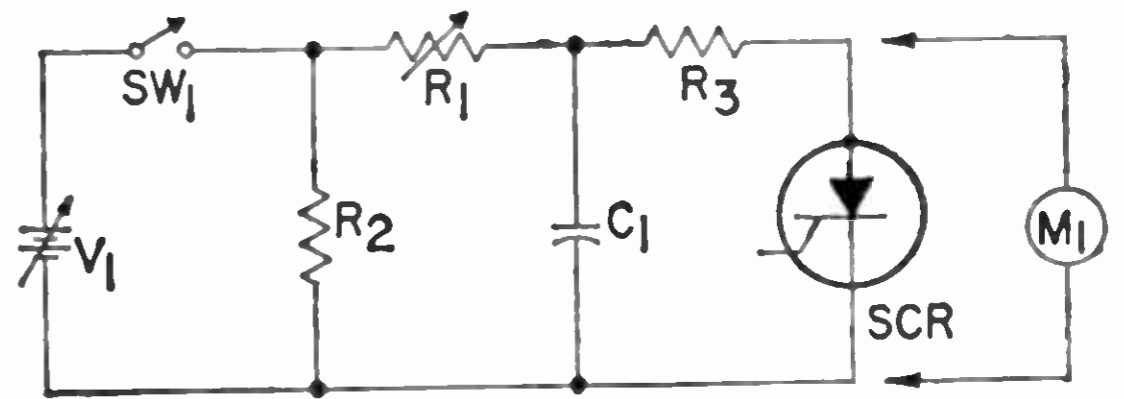
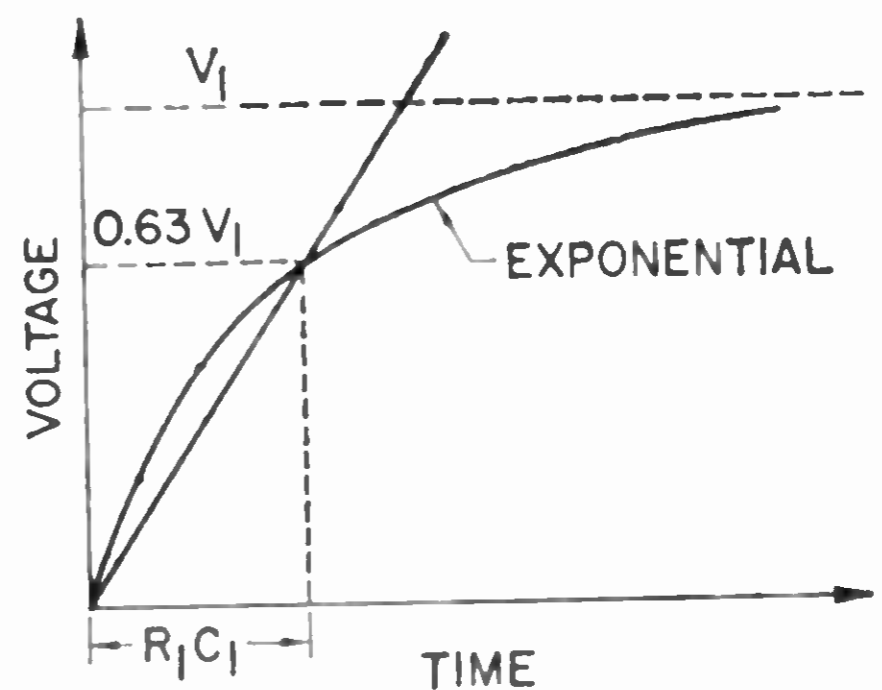


Fig. 331—Test circuit used to determine holding and latching currents of thyristors.

Fig. 332(a) shows a simple test circuit that may be used to determine the dv/dt capability of a thyristor. The curves in Fig. 332(b) define the critical values for linear and exponential rates of increase in



(a)



(b)

Fig. 332—Test circuit and waveforms used to determine dv/dt capability of a thyristor.

reapplied forward OFF-state voltage for an SCR. The critical value for the exponential rate of rise of forward voltage is the rating given in the manufacturer's test specifications. This rating is determined from the following equation:

$$\frac{dv}{dt} = \frac{\text{rated value of thyristor voltage } (V_{BO})}{RC \text{ time constant}} \times 0.632$$

Fig. 333 shows a simple test circuit used to determine turn-on times of thyristors. The value of resistor R_1 is chosen so that the rated value

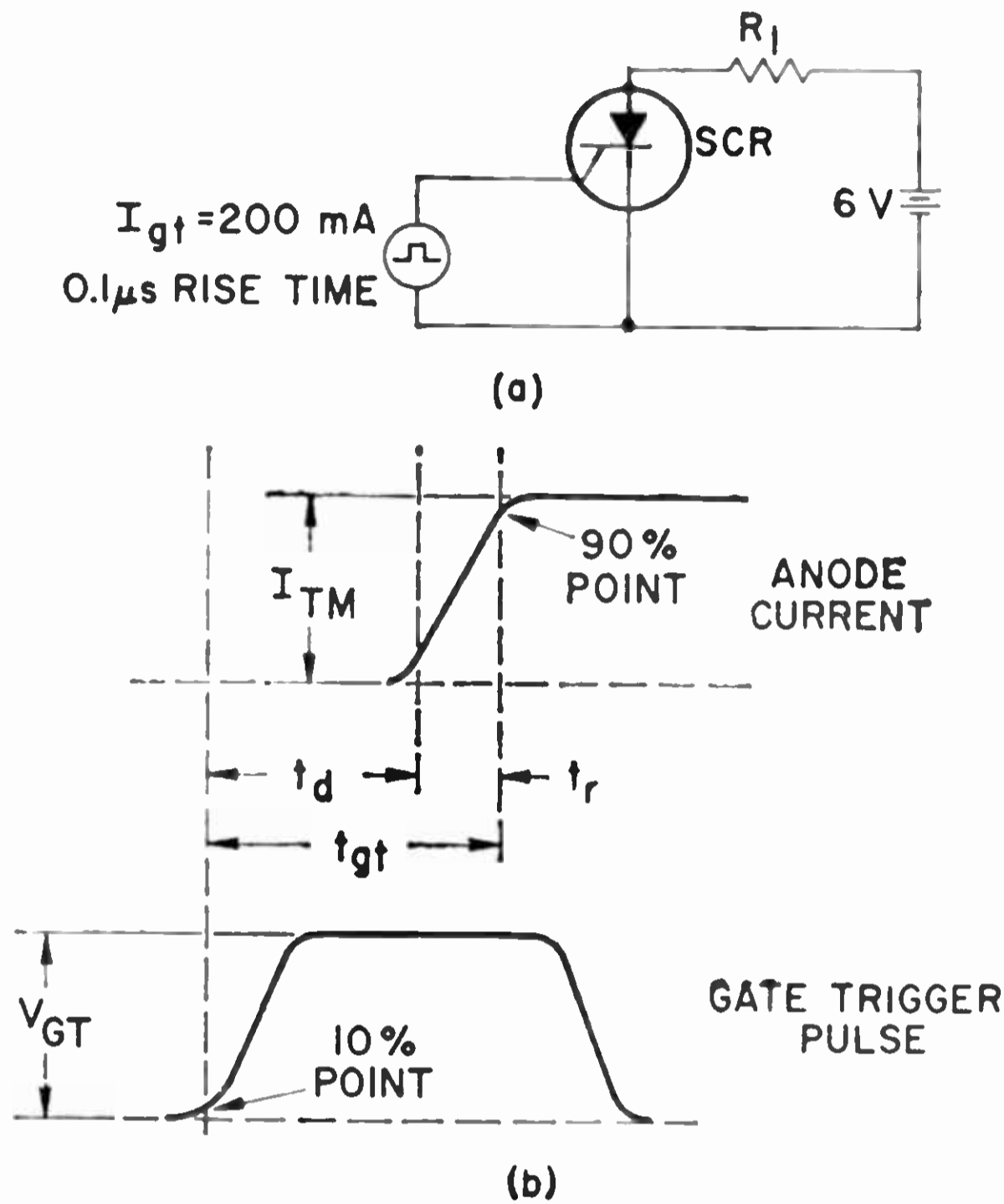


Fig. 333—Test circuit and waveforms used to determine turn-on time of thyristors.

of current flows through the thyristor. Turn-on time is specified by the thyristor manufacturer at the rated blocking voltage. It is defined (for resistive loads) as the time interval between 10 per cent of the gate voltage and the period required for the current to rise to 90 per cent of its maximum value.

Fig. 334 shows a simple test circuit used to measure turn-off time. The circuit subjects the thyristor to current and voltage waveforms similar to those encountered in most typical applications. In the circuit diagram, SCR_1 is the device under test. Initially, both SCR 's are in the OFF-state; push-button switch SW_1 is momentarily closed to start the test. This action turns on SCR_1 and load current flows through this SCR and resistor R_2 . Capacitor C_1 charges through resistor R_3 to the voltage developed across R_2 . If the second push-button switch SW_2 is

then closed, SCR_2 is turned on. SCR_1 is then reverse-biased by the voltage across capacitor C_1 . The discharge of this capacitor causes a short pulse of reverse current to flow through SCR_1 until this device recovers its reverse-blocking capability. At some time t_1 , the anode-to-cathode voltage of SCR_1 passes through zero and starts to build up in a forward direction at a rate dependent upon the time constant of C_1 and R_2 . The peak value of the reverse current during the

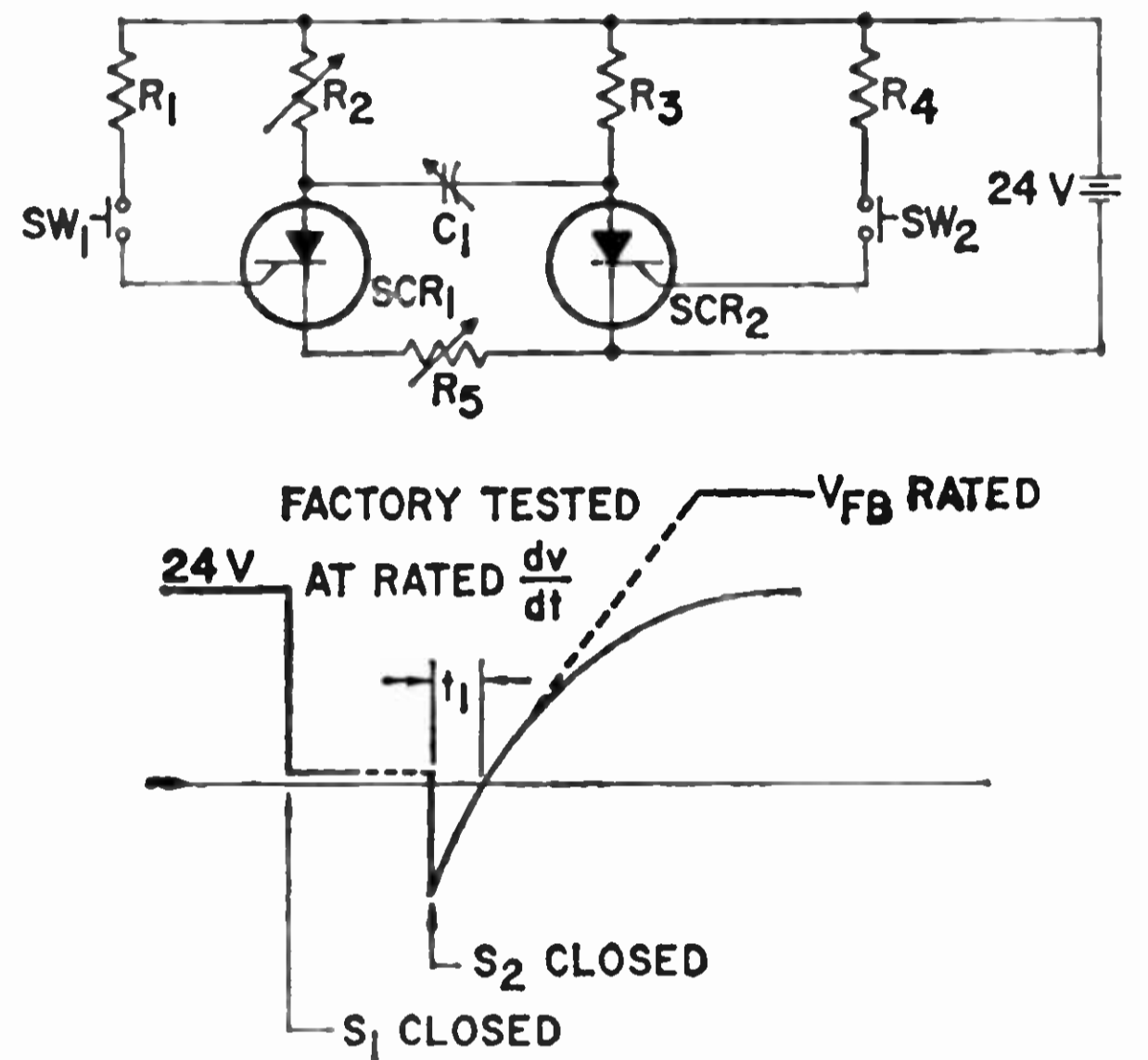


Fig. 334—Test circuit and voltage waveforms used to determine turn-off times of thyristors.

recovery period can be controlled by adjustment of potentiometer R_5 . If the turn-off time of SCR_1 is less than the time t_1 , the device will turn off. The turn-off interval t_1 can be measured by observation of the anode-to-cathode voltage of SCR_1 with a high-speed oscilloscope. A typical waveform is shown in Fig. 334.

The gate voltage and current required to switch a thyristor to its low-impedance state at maximum rated forward anode current can be determined from the circuit shown in Fig. 335. The value of resistor R_2 is chosen so that maximum anode current, as specified in the manufacturer's current rating, flows when the device latches into its low-impedance state. The

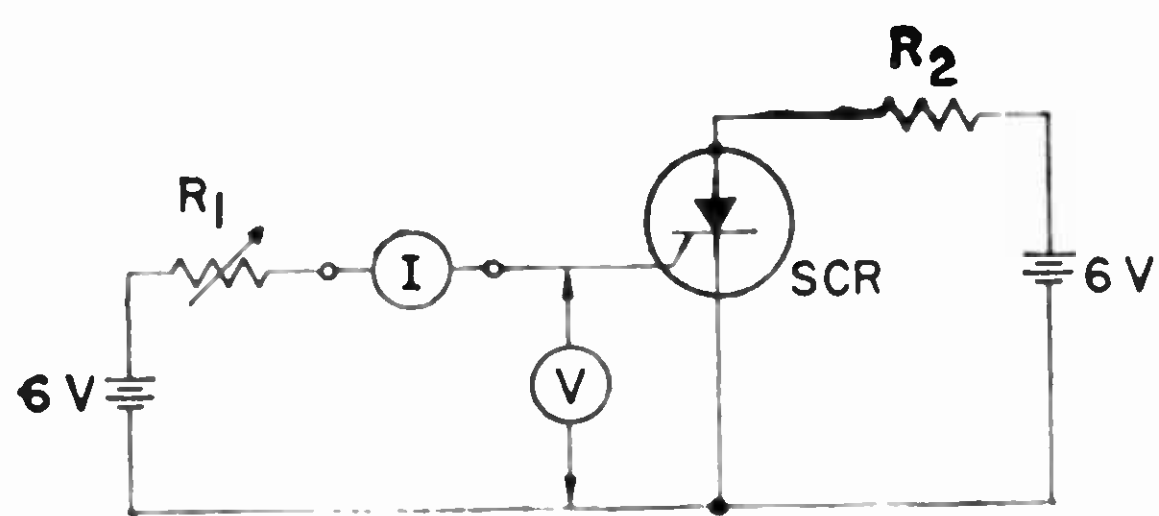


Fig. 335—Test circuit used to determine gate-trigger-pulse requirements of thyristors.

value of resistor R_1 is gradually decreased until the device under test is switched from its high-impedance state to its low-impedance state. The values of gate current and gate voltage immediately prior to switching are the gate voltage and current required to trigger the thyristor.

HEAT-SINK REQUIREMENTS

All semiconductor devices are temperature-sensitive, some to a greater degree than others. As a result, the device temperature or power dissipation must be kept below the maximum specified rating either by limiting the input power requirements to maintain a limited power dissipation or by providing some external means of removing the excess heat generated during normal operation. Generally, low-power semiconductor devices have sufficient mass and heat-dissipation area to conduct away the detrimental heat energy formed at their semiconductor junctions. For higher-power devices, such as power transistors, thyristors, and silicon rectifiers, however, a heat sink must be used.

Under steady-state conditions, the maximum dissipation capability of a semiconductor device that has a heat sink attached depends on the sum of (a) the series thermal resistances from the semiconductor junction to the ambient, (b) the maximum junction temperature, and (c) the ambient temperature at which the device is operated. The total thermal resistance of the de-

vice from junction to ambient θ_{J-A} can be expressed as follows:

$$\theta_{J-A} = \theta_{J-C} + \theta_{C-S} + \theta_{S-A}$$

where θ_{J-C} is the thermal resistance from the semiconductor junction to the case of the device, θ_{C-S} is the thermal resistance between the device case and the surface of the heat sink, and θ_{S-A} is the thermal resistance of the heat sink (from its surface to the ambient air).

The maximum dissipation capability of a semiconductor device $P_D(\max)$ with a heat sink attached is given by

$$P_D(\max) = \frac{T_J(\max) - T(\text{amb})}{\theta_{J-C} + \theta_{J-S} + \theta_{S-A}}$$

where $T_J(\max)$ is the maximum junction temperature obtained from the manufacturer's data and $T(\text{amb})$ is the ambient temperature.

Discrete heat sinks are sold commercially in various size, shapes, colors, and materials. It is also common practice to use the chassis of the unit as a heat sink. In any case, the heat-dissipation capability of the heat sink is based on its thermal resistance θ_{S-A} . The thermal-resistance value of the heat sink should be small enough to obtain a power-dissipation capability, as expressed in the above equation, that exceeds the power-dissipation rating of the semiconductor device. For high-power devices, the interface thermal resistance θ_{C-S} between the semiconductor case and the surface of the heat sink can be maintained at a low value (1 to 2°C per watt) by use of epoxy glue or silicone grease.

Fig. 336 shows a useful nomograph for obtaining the physical dimensions of a heat sink as a function of its thermal resistance. The data in this nomograph pertain to a heat sink that cools by convection and radiation and that is of natural bright finish of copper or aluminum. The heat-sink area is selected from the left-hand column and a line is

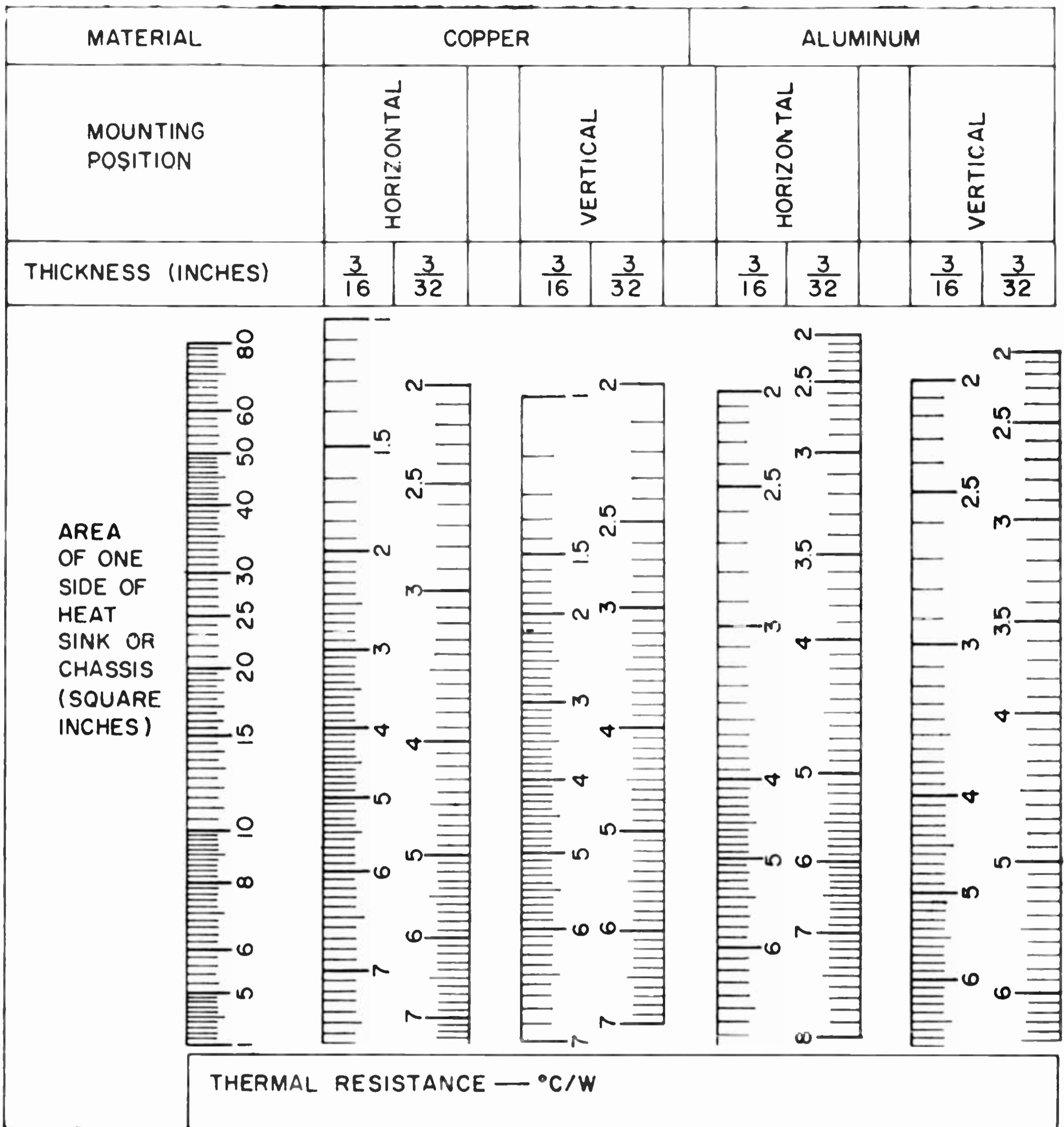


Fig. 336—Thermal resistance as a function of heat-sink dimensions (Nomograph reprinted from *ELECTRONIC DESIGN*, Aug. 16, 1961).

drawn horizontally from this point. The value of thermal resistance θ_{s-A} is read directly from the graph, depending on the type and thickness of the heat-sink material and the mounting position of the heat sink, either horizontal or vertical, with respect to the mounting board.

TRANSISTOR MOUNTING

The collector, base, and emitter terminals of transistors can be connected to associated circuit elements by means of sockets, clips, or solder connections to the leads or pins. If connections are soldered close to the lead or pin seals, care must be taken

to conduct excessive heat away from the seals, otherwise the heat of the soldering operation may crack the glass seals and damage the transistor. When dip soldering is employed in the assembly of printed circuits using transistors, the temperature of the solder should be limited to about 225 to 250°C for a maximum immersion period of 10 seconds. Furthermore, the leads should not be dip-soldered too close to the transistor case. Under no circumstances should the mounting flange of a transistor be soldered to a heat sink because the heat of the soldering operation may permanently damage the transistor.

In some transistors, the collector electrode is connected internally to the metal case to improve heat-dissipation capabilities. More efficient cooling of the collector junction in these transistors can be accomplished by connection of the case to a heat sink. Direct connection of the case to a metal surface is practical only when a grounded-collector circuit is used. For other configurations, the collector is electrically isolated from the chassis or heat sink by means of an insulator that has good thermal conductivity.

For small general-purpose transistors, such as the 2N2102, which use a JEDEC TO-5 package, a good thermal method of isolating the collector from a metal chassis or printed circuit board is by means of a beryllium oxide washer. The use of a zinc-oxide-filled silicone compound between the washer and the chassis, together with a moderate amount of pressure from the top of the transistor, helps to improve thermal dissipation. An alternate method is the use of a fin-type heat sink. Fig. 337 illustrates both types of mounting. Fin-type heat sinks are especially suitable when transistors are mounted in Teflon sockets which

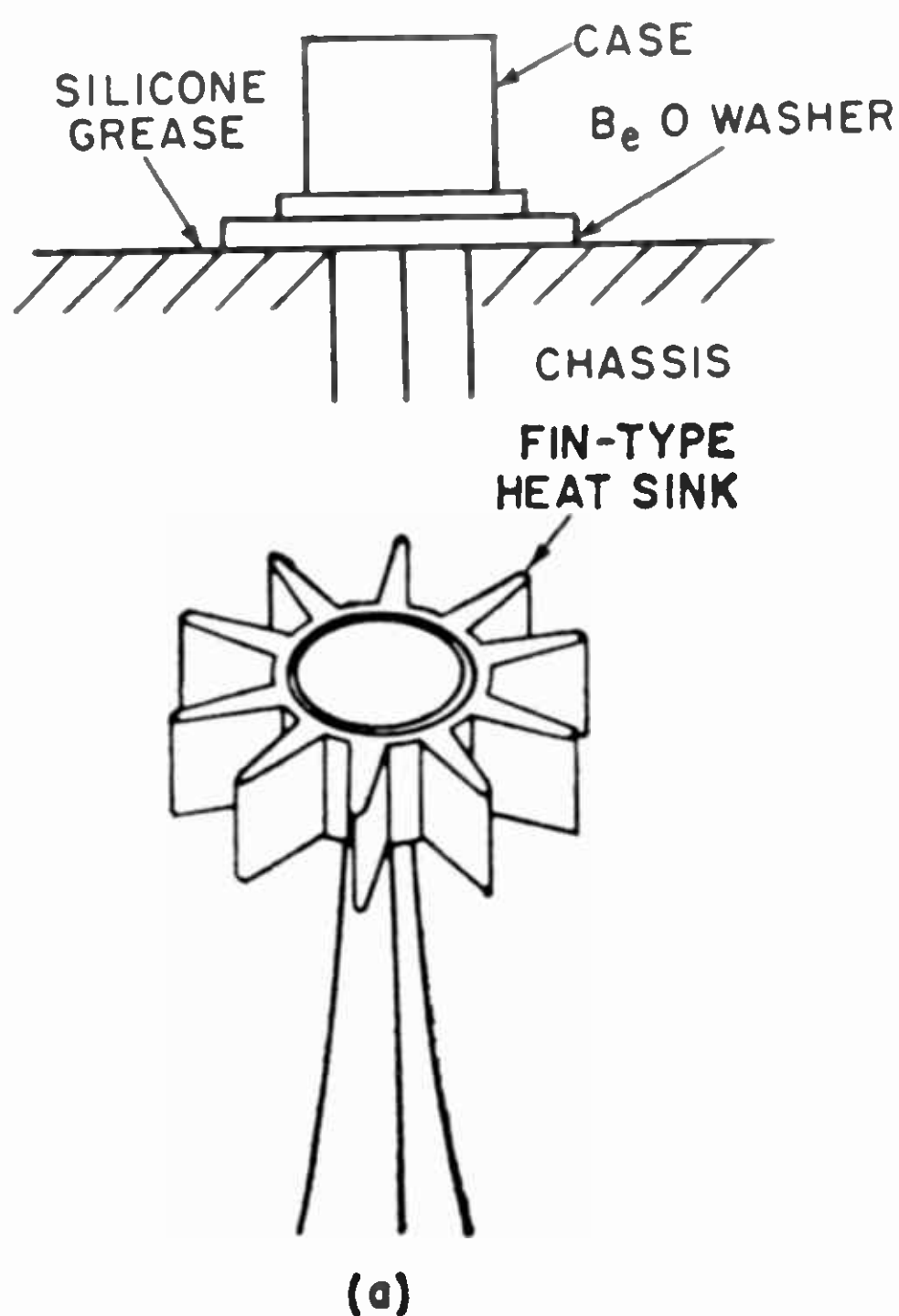


Fig. 337—Suggested mounting arrangements for transistors in JEDEC TO-5 package.

provide no thermal conduction to the chassis or printed circuit board.

For power transistors which use a JEDEC TO-3 package, such as the 2N3055, it is recommended that a 0.002-inch mica insulator or an anodized aluminum insulator having high thermal conductivity be used between the transistor base and the heat sink or chassis. The insulator should extend beyond the mounting clamp, as shown in Fig. 338. It should be drilled or punched to provide both the two mounting holes

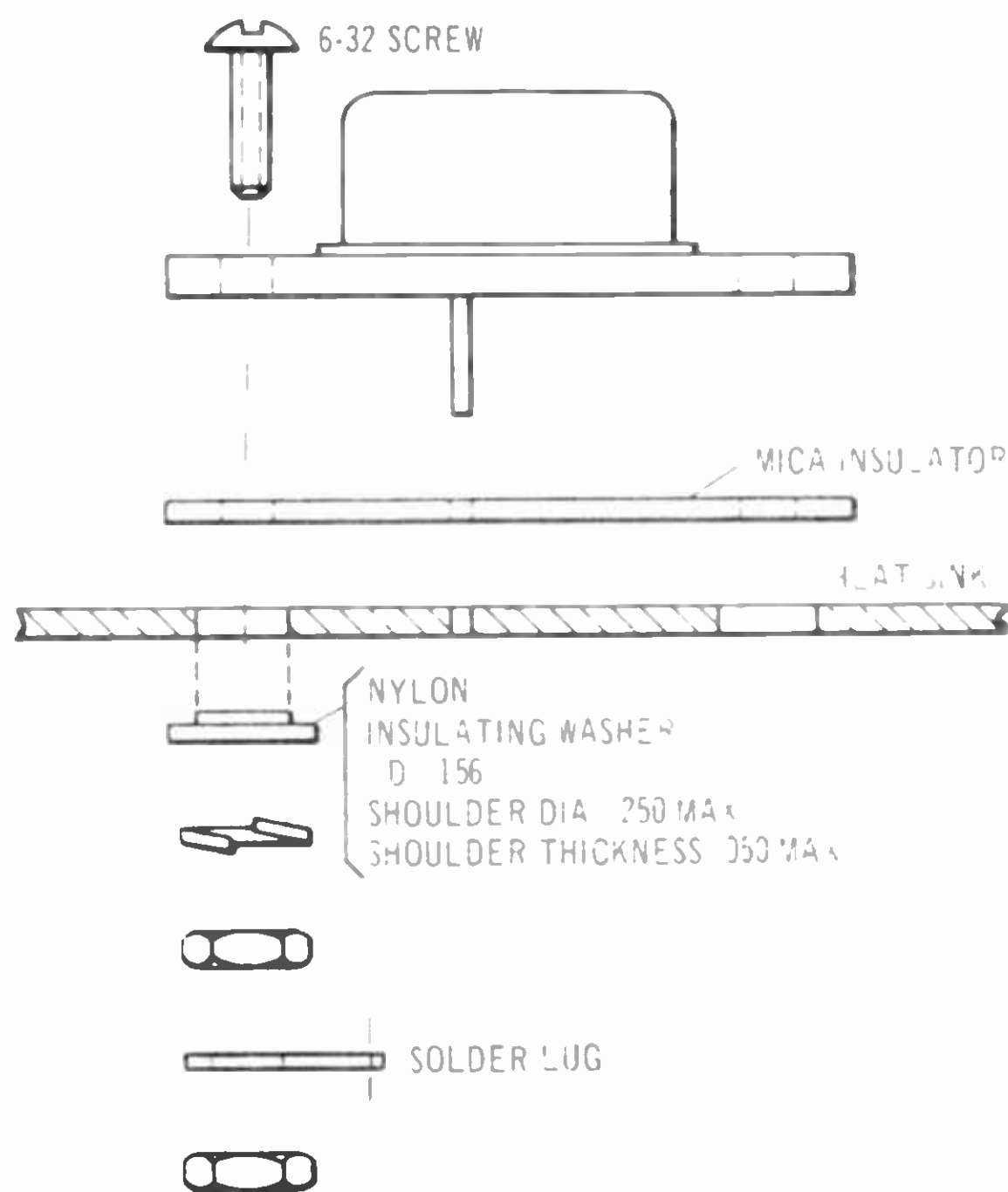


Fig. 338—Suggested mounting arrangement for transistors in JEDEC TO-3 package.

and the clearance holes for the emitter and base pins. Burrs should be removed from both the insulator and the holes in the chassis so that the insulating layer will not be destroyed during mounting. It is also recommended that an insulating washer be used between the mounting screws and the chassis, as shown in Fig. 338, to prevent a short circuit between them.

For large power transistors, such as the 2N2876, which use a double-ended stud package, connection to the chassis or heat sink should be made at the flat surface of the transistor perpendicular to the threaded stud. A large mating surface should be provided to avoid hot spots and

high thermal drop. The hole for the stud should be only as large as necessary for clearance, and should contain no burrs or ridges on its perimeter. As mentioned above, the use of a silicon grease between the heat sink and the transistor improves thermal contact. The transistor can be screwed directly into the heat sink or can be fastened by means of a nut. In either case, care must be taken to avoid the application of too much torque lest the transistor semiconductor junction be damaged. Although the studs are made of relatively soft copper to provide high thermal conductivity, the threads should not be relied upon to provide a mating surface. The actual heat transfer must take place on the underside of the hexagonal part of the package.

RCA transistors are also available in molded silicone plastic packages for medium-power and high-power switching and amplifier applications. Fig. 339 shows the four package designs for plastic-package transistors. The packages shown in Fig. 339(a) and (b) are designed for printed-circuit boards. The packages shown in Fig. 339(c) and (d) are designed for substitution in place of equivalent transistors in TO-3 and TO-66 packages, respectively. For example, the device shown in Fig. 339(c) may be plugged into a TO-3 socket or (as shown in Fig. 340) secured by means of an over-clamp that has mounting holes identical to those for a TO-3 package.

The use of an external resistance in the emitter or collector circuit of

a transistor is an effective deterrent to damage which might be caused by thermal runaway. The minimum value of this resistance for low-level stages may be obtained from the following equation:

$$R_{min} = \frac{E^2}{4 \left(P_0 + \frac{25}{\theta_{J-A}} \right)}$$

where E is the dc collector supply voltage in volts, P₀ is the product of the collector-to-emitter voltage and the collector current at the desired operating point in watts, and θ_{J-A} is the thermal resistance of the transistor and heat sink in degrees centigrade per watt (θ_{J-C} + θ_{C-S} + θ_{S-A}).

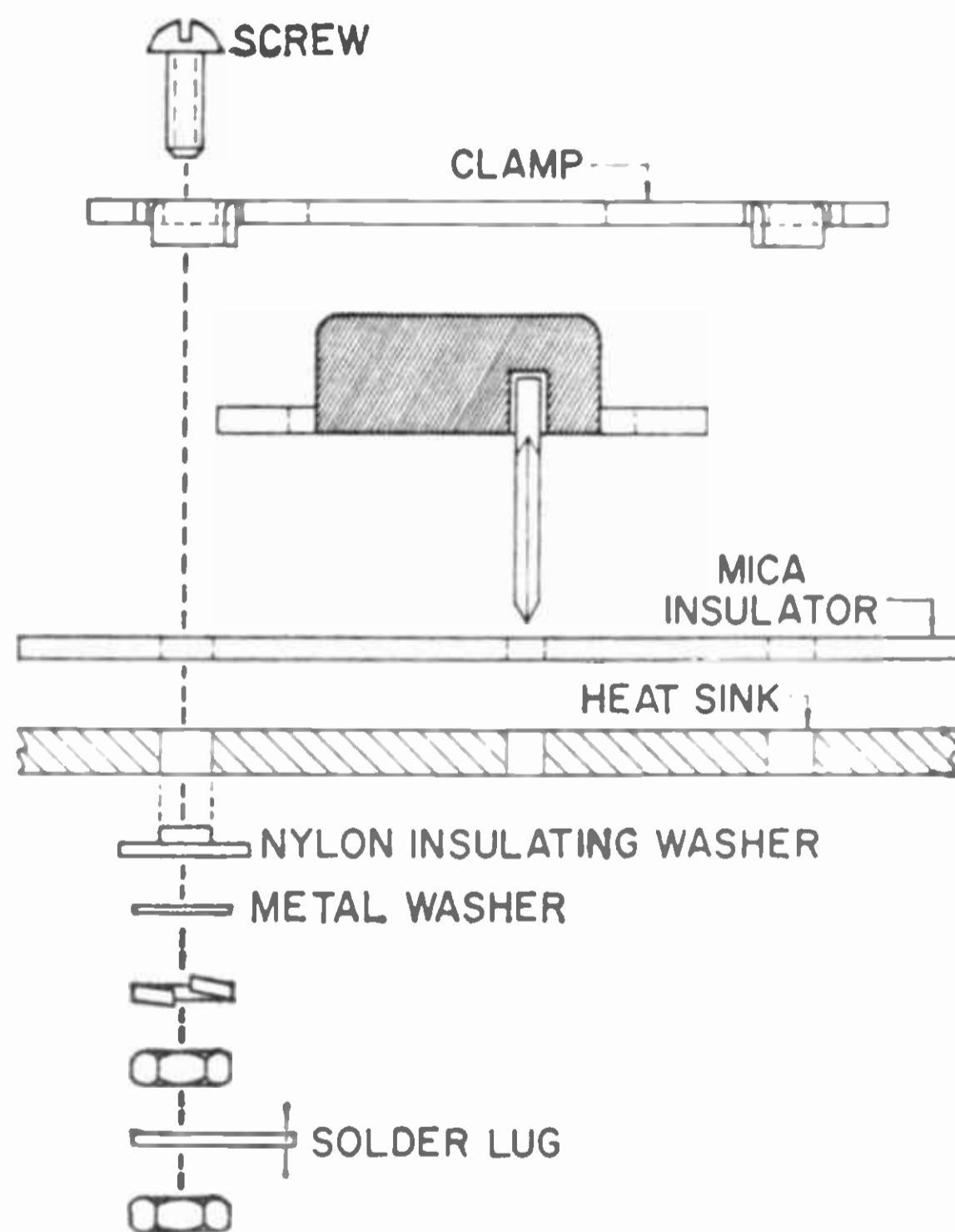


Fig. 340—Suggested mounting for plastic TO-3 package.

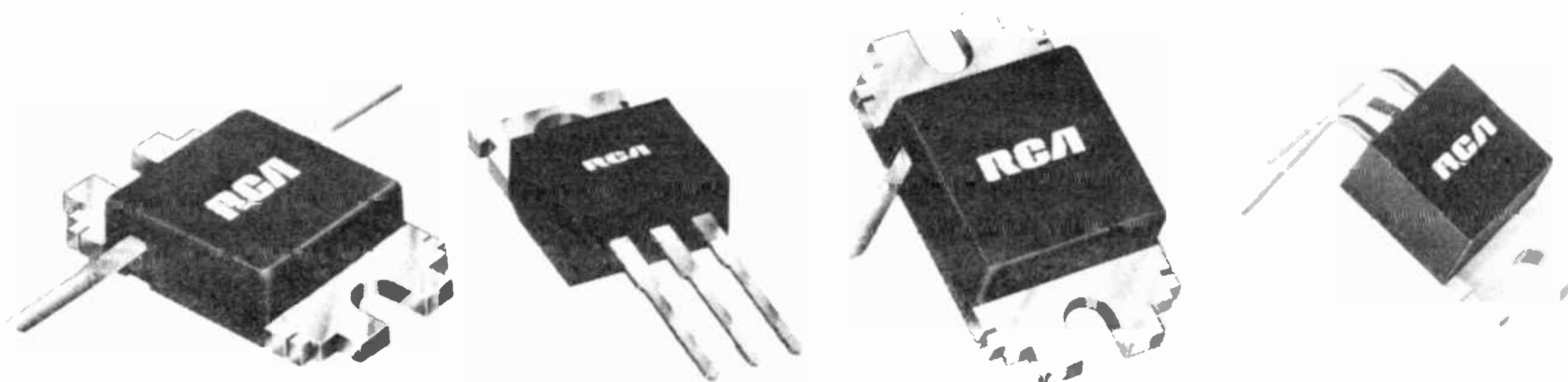


Fig. 339—Four package designs for plastic-package transistors.

THYRISTOR MOUNTING

For most efficient heat sinks, intimate contact should exist between the heat sink and at least one-half of the package base. The package can be mounted on the heat sink mechanically, with glue or epoxy adhesive, or by soldering. The JEDEC TO-48, TO-66, and stud-mounted packages are mounted mechanically. In these cases, silicone grease should be used between the device and the heat sink to eliminate surface voids, prevent insulation build-up due to oxidation, and help conduct heat across the interface. Although glue or epoxy adhesive provides good bonding, a significant amount of resistance may exist at the interface. To minimize this interface resistance, an adhesive material with low thermal resistance, such as Hysol* Epoxy Patch Material No. 6C or Wakefield* Delta Bond No. 152, or their equivalent, should be used.

Fig. 341 shows the special press-fit package used for some SCR's and triacs. Press-fit mounting depends upon an interference fit between the



Fig. 341—Press-fit package.

thyristor case and the heat sink. As the thyristor is forced into the heat-sink hole, metal from the heat sink flows into the knurl voids of the thyristor case. The resulting close contact between the heat sink and thyristor case assures low thermal resistances.

* Products of Hyson Corporation, Olean, New York, and Wakefield Engineering, Inc., Wakefield, Massachusetts, respectively.

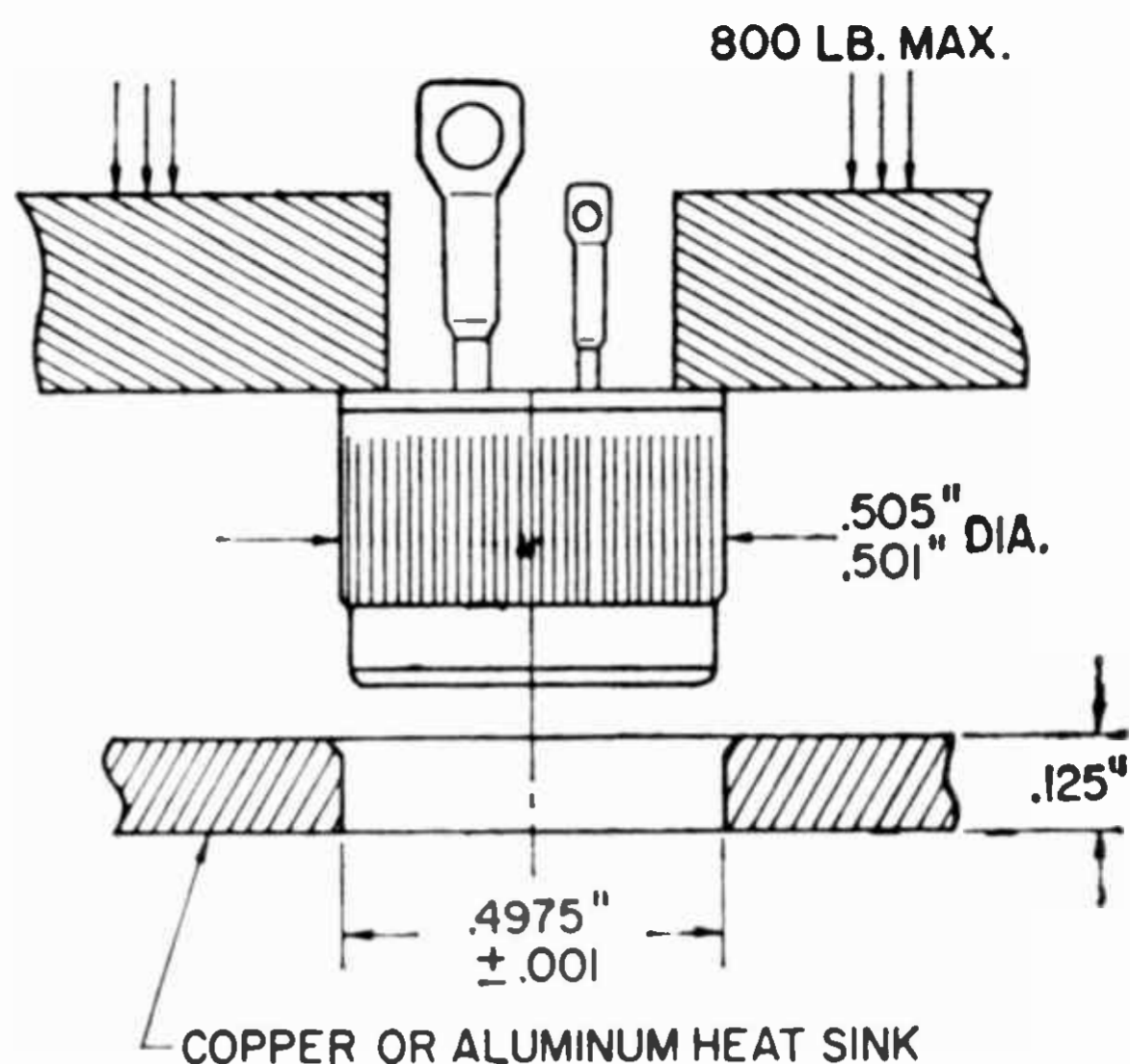


Fig. 342—Suggested mounting arrangement for press-fit types.

A recommended mounting method, shown in Fig. 342, shows press-fit knurl and heat-sink hole dimensions. If these dimensions are maintained, a "worst-case" condition of 0.0085 inch interference fit will allow press-fit insertion below the maximum allowable insertion force of 800 pounds. A slight chamfer in the heat-sink hole will help center and guide the press-fit package properly into the heat sink. The insertion tool should be a hollow shaft having an inner diameter of 0.380 ± 0.010 inch and an outer diameter of 0.500 inch. These dimensions provide sufficient clearance for the leads and assure that no direct force is applied to the glass seal of the thyristor.

The press-fit package is not restricted to a single mounting arrangement; direct soldering and the use of epoxy adhesives have been successfully employed. The press-fit case is tin-plated to facilitate direct soldering to the heat sink. A 60-40 solder should be used, and heat should only be applied long enough to allow the solder to flow freely.

For the JEDEC TO-5, TO-8, and low-profile packages, shown in Fig. 343, soldering of the thyristor to the heat sink is preferable because it is most efficient. Not only is the bond permanent, but the thermal re-



Fig. 343—JEDEC TO-5, TO-8, and low-profile packages.

sistance θ_{c-s} from the thyristor case to the heat sink is easily kept below 1°C per watt under normal soldering conditions. Oven or hot-plate batch-soldering techniques are recommended because of their low cost. The use of a self-jigging arrangement of the thyristor and the heat sink and a 60-40 solder preform is recommended. If each unit is soldered individually with a flame or electric soldering iron, the heat source should be held on the heat sink and the solder on the unit. Heat should be applied only long enough to permit solder to flow freely. Because RCA thyristors are tin-plated, maximum solder wetting is easily obtainable without thyristor overheating.

The special high-conductivity leads on the two-lead TO-5 package permit operation of the thyristor at current levels that would be considered excessive for an ordinary TO-5 package. The special leads can be bent into almost any configuration to fit any mounting requirement; however, they are not intended to take repeated bending and unbending. In particular, repeated bending at the glass should be avoided. The leads are not especially brittle at this point, but the glass has a sharp edge which produces an excessively small radius of curvature in a bend made at the glass. Repeated bending with a small radius of curvature at a fixed point will cause fatigue and breakage in almost any material. For this reason, right-angle bends should be made at least 0.020

inch from the glass. This practice will avoid sharp bends and maintain sufficient electrical isolation between lead connections and header. A safe bend can be assured if the lead is gripped with pliers close to the glass seal and then bent the requisite amount with the fingers, as shown in Fig. 344. When the leads of a number of devices are to

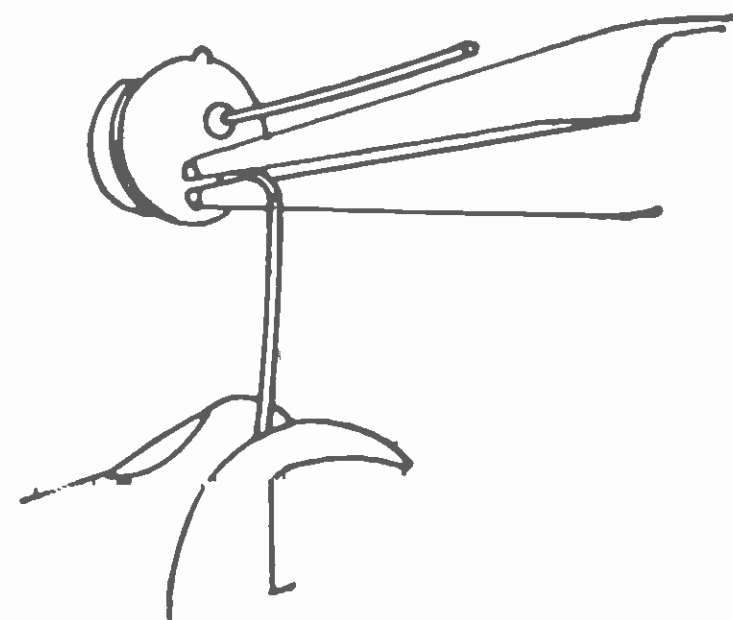


Fig. 344—Method of bending leads on thyristor package.

be bent into a particular configuration, it may be advantageous to use a lead-bending fixture to assure that all leads are bent to the same shape and in the correct place the first time, so that there is no need for repeated bending.

Typical Heat-Sink Configurations

Fig. 345 shows some typical heat-sink configurations that can be used with RCA thyristors in a TO-5 package. The thermal-resistance θ_{s-a} for each of the easily fabricated sinks is given, together with approximate dimensions. The thyristors in the illustrations are soldered to the heat sink; if epoxy is used, an additional thermal resistance θ_{c-s} of 1 to 2°C per watt must be added to the

thermal-resistance values shown. The junction-to-case thermal-resistance value for the particular thyristor being used should be added to the values shown to obtain the over-all junction-to-air thermal resistance of each configuration. In the designs shown, electrical insulation of the heat sink from the chassis or equipment housing may be required.

Chassis-Mounted Heat Sinks

In many applications, it is desirable and practical to use the chassis or equipment housing as the heat sink. In such cases, the thyristor must be electrically insulated from the heat sink, but must still permit heat generated by the device to be efficiently transferred to the chassis or housing. This heat transfer can be achieved by use of the heat-spreader mounting method. In this method, the thyristor is attached to a metal bracket (heat spreader) which is attached to, but electrically insulated from, the chassis. The heat-sink configurations shown in Fig. 345 can serve as heat spreaders, as well as the special clip shown in Fig. 346. (Triacs soldered to this heat spreader are available from RCA as type numbers 40638 and 40639; SCR's on this spreader are available as type numbers 40656 and 40657.)

Electrical insulation may consist of material such as alumina ceramic, polyimide film or tape, fiberglass tape, or epoxy. The metal bracket itself has a low thermal resistance, and spreads the heat out over a larger area than could the thyristor case alone. The larger area in contact with the electrical insulation allows heat to transfer from bracket to chassis through the insulation with relatively low thermal resistance. Typical heat sinks, such as those shown in Fig. 345, provide a much lower thermal resistance when used as heat spreaders than when used as heat sinks.

Heat-spreader dimensions can be varied over a wide range to suit

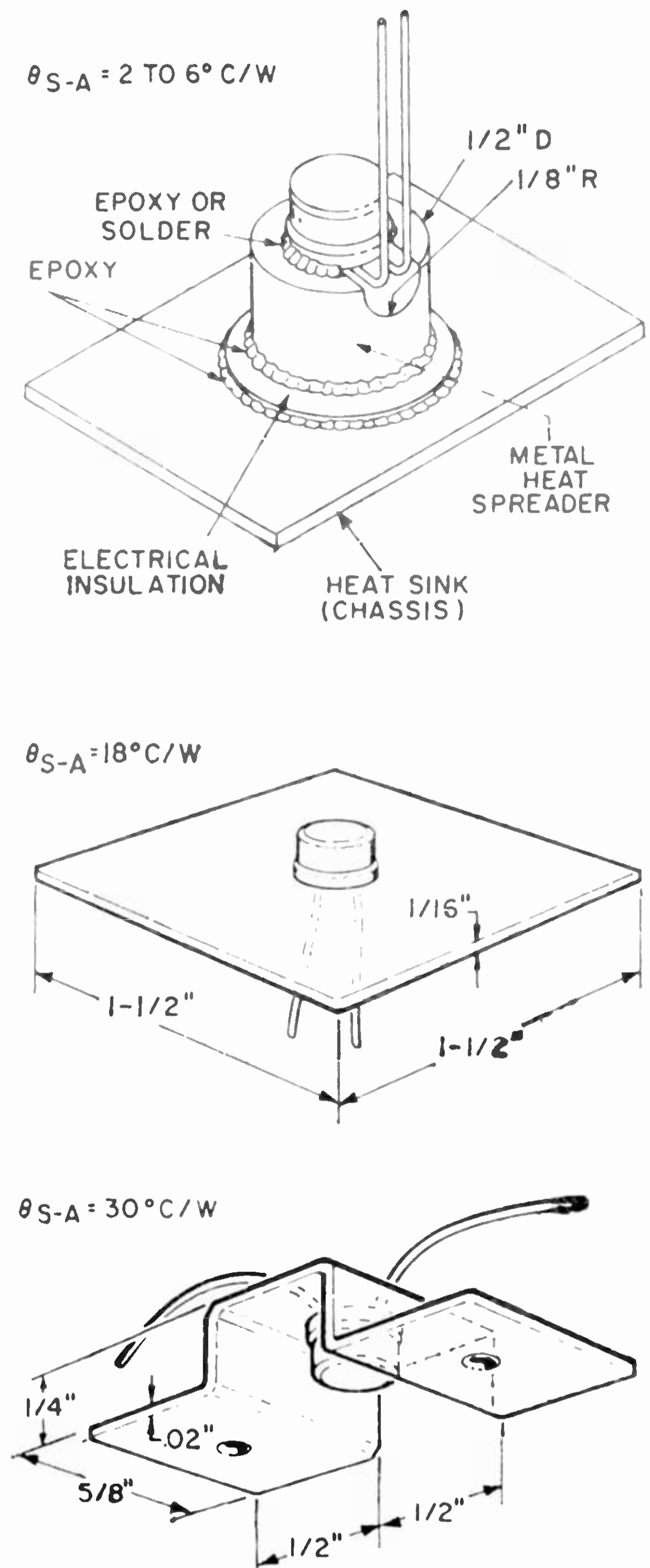


Fig. 345—Typical heat-sink configurations for use with TO-5 package.

particular applications. For example, area or diameter can be increased, or shape changed, as long as the heat-transfer area in contact with the electrical insulation is sufficient. An area of 0.2 square inch or more is usually desirable. The exact thermal resistance of any heat spreader depends on the heat-transfer area, type of metal used, type of insulation used, and whether the thyristor is fastened to the heat

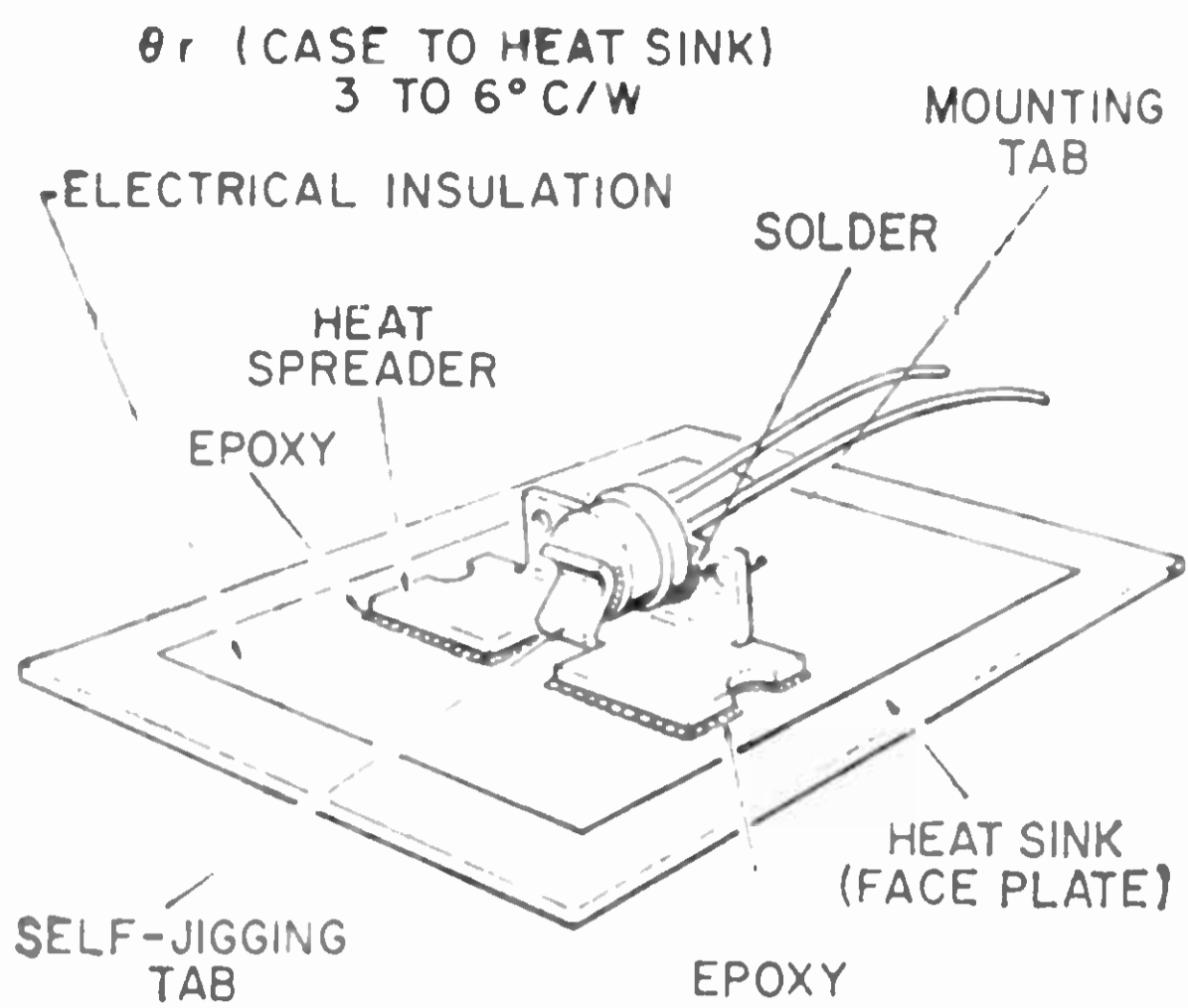


Fig. 346—Self-jigging heat spreader.

spreader with solder or epoxy. Soldered construction yields a thermal resistance about 1°C per watt less than that obtained with epoxy. Alumina or polyimide insulation provides a thermal resistance about 1 to 2°C per watt less than that obtained with thermosetting fiberglass-tape insulation. The heat spreader can be made of any material with suitable thermal conductivity, such as copper, brass, or aluminum. Solderable plating for aluminum is commercially available.

RECTIFIER MOUNTING

The maximum forward-current ratings for RCA silicon rectifiers

apply specifically for operation in free air (natural convection cooling). The average (dc) forward-current and the peak recurrent forward-current capabilities of these rectifiers are substantially higher than those shown in the maximum ratings when the rectifiers are attached to heat sinks.

Rectifiers used for low-power applications normally do not require an external heat sink to dissipate the heat generated at their p-n junctions. Most rectifiers in this category are packaged in the same small case used for the JEDEC TO-1 package. For medium-current (1- to 2-ampere) high-voltage applications, the rectifier is packaged in a flange-case, axial-lead JEDEC DO-1 case. For higher-current applications, the DO-4 and DO-5 packages are used. These package configurations are shown in Fig. 347.

Fig. 348 shows two suggested methods for attaching the flange-case, axial-lead package to a heat sink. The flange of the rectifier may also be soldered directly to the heat sink, provided the flange temperature during soldering does not exceed 253°C for a maximum period of 10 seconds. Permanent damage to the rectifier may result if these limits are exceeded.

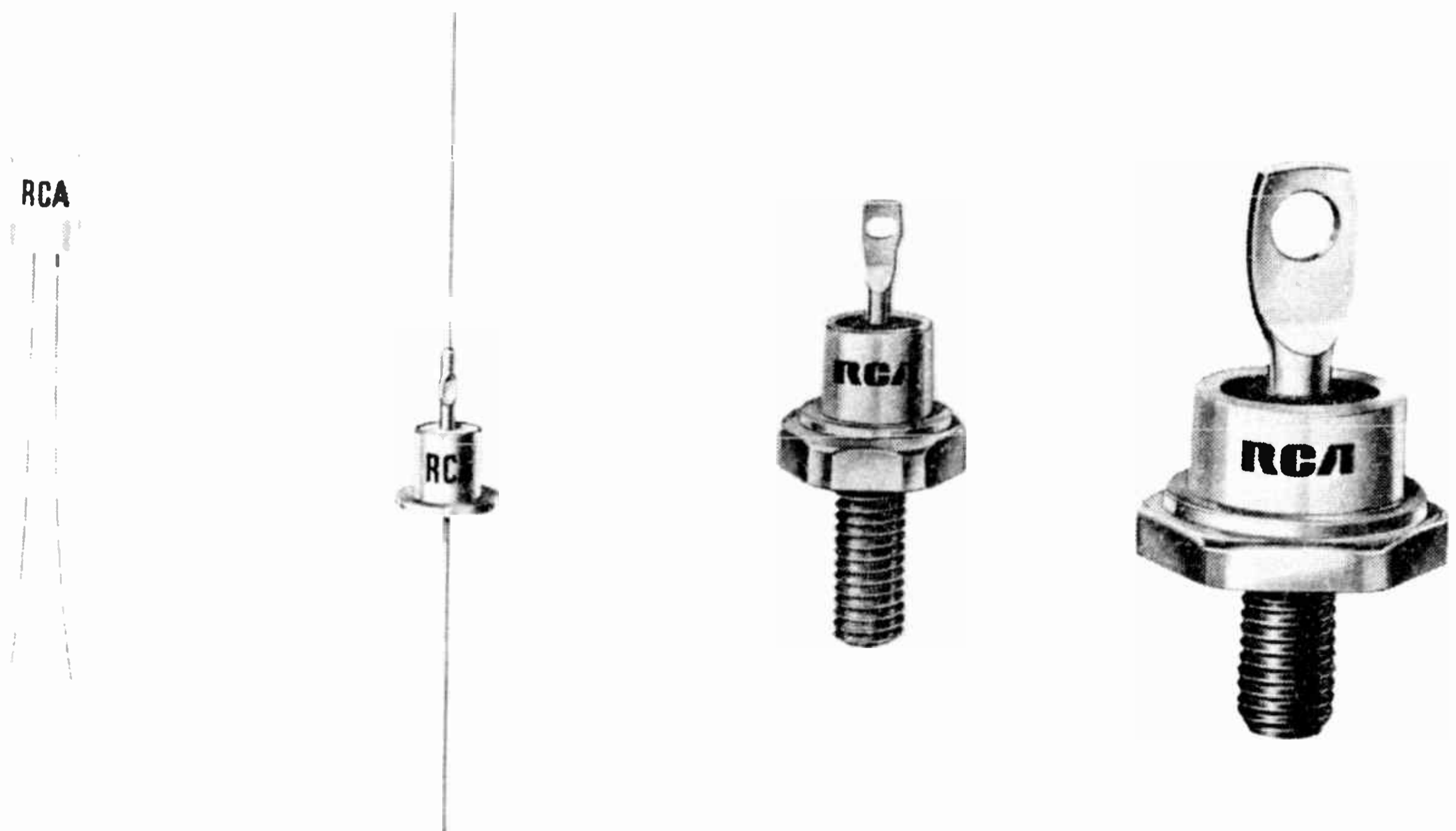


Fig. 347—Various package designs for RCA silicon rectifiers.

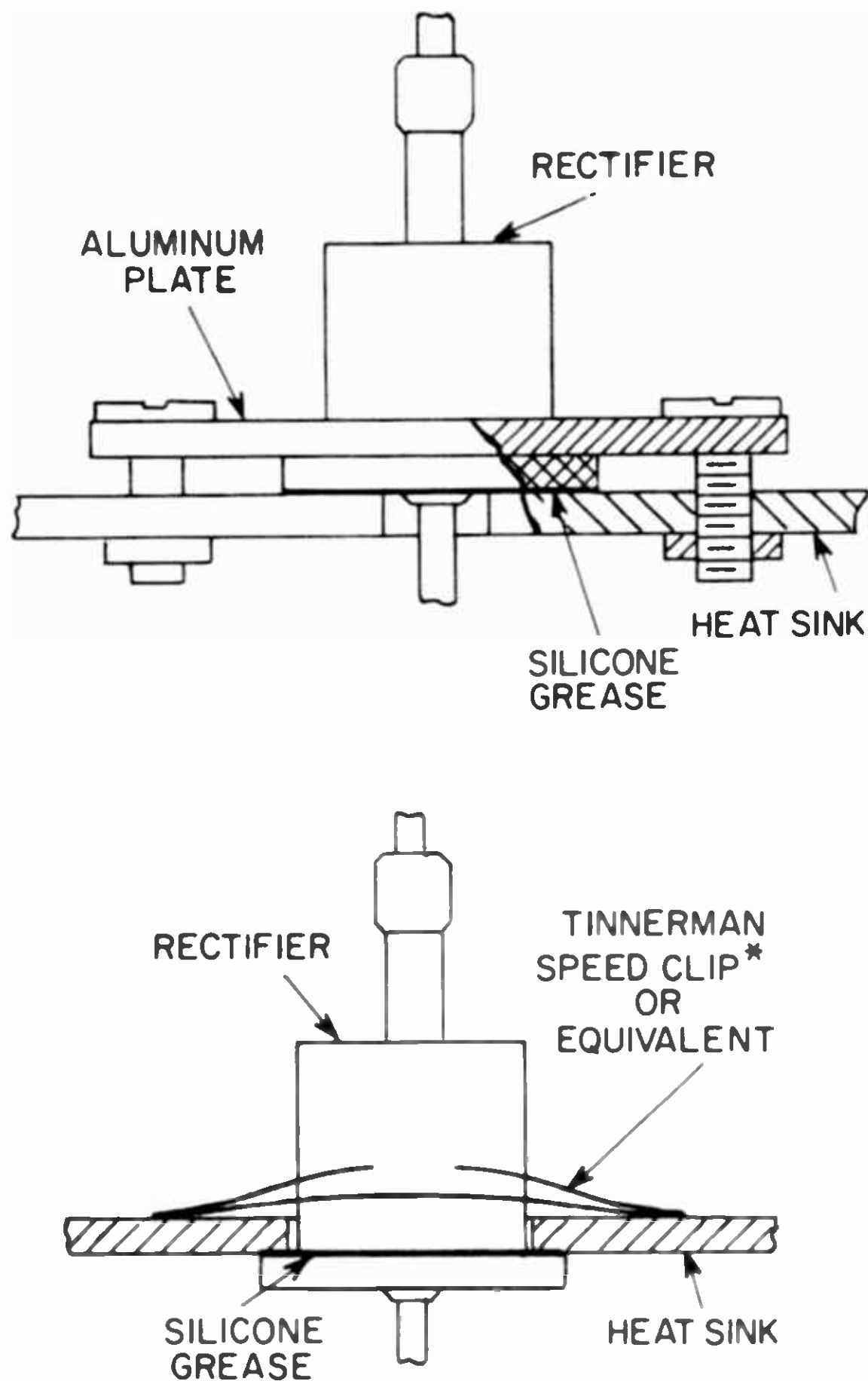


Fig. 348—Suggested methods for attaching rectifier types 1N2858A through 1N2864A to heat sink.

The flexible leads of some RCA rectifiers are usually soldered to the circuit elements. It is desirable in all installations to provide some slack or an expansion elbow in each lead to prevent excessive tension on the leads. Manual soldering should be performed carefully and quickly to avoid damage to the rectifier by excessive heating. To minimize heating the rectifier junction during manual soldering, it is desirable to grip the flexible lead being soldered between the case and the soldering point with a pair of pliers.

When dip soldering is used in the assembly of printed circuits, the temperature of the solder should not exceed 255°C for a maximum immersion period of 10 seconds. The leads should not be dip-soldered beyond points, "A" and "B" indicated in Fig. 349.

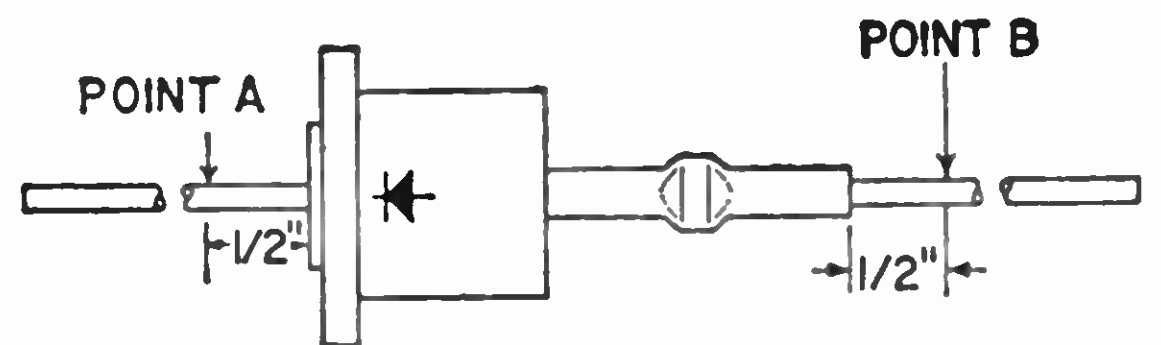


Fig. 349—Diagram showing areas beyond which dip-soldering should not extend.

Fig. 350 shows the suggested mounting of the higher-current-type DO-4 and DO-5 packages. Mounting components of the type shown are furnished with each rectifier. With these mounting components, the increase in thermal resistance θ_{c-s} from the rectifier case to the heat-sink surface is approximately 3°C per watt.

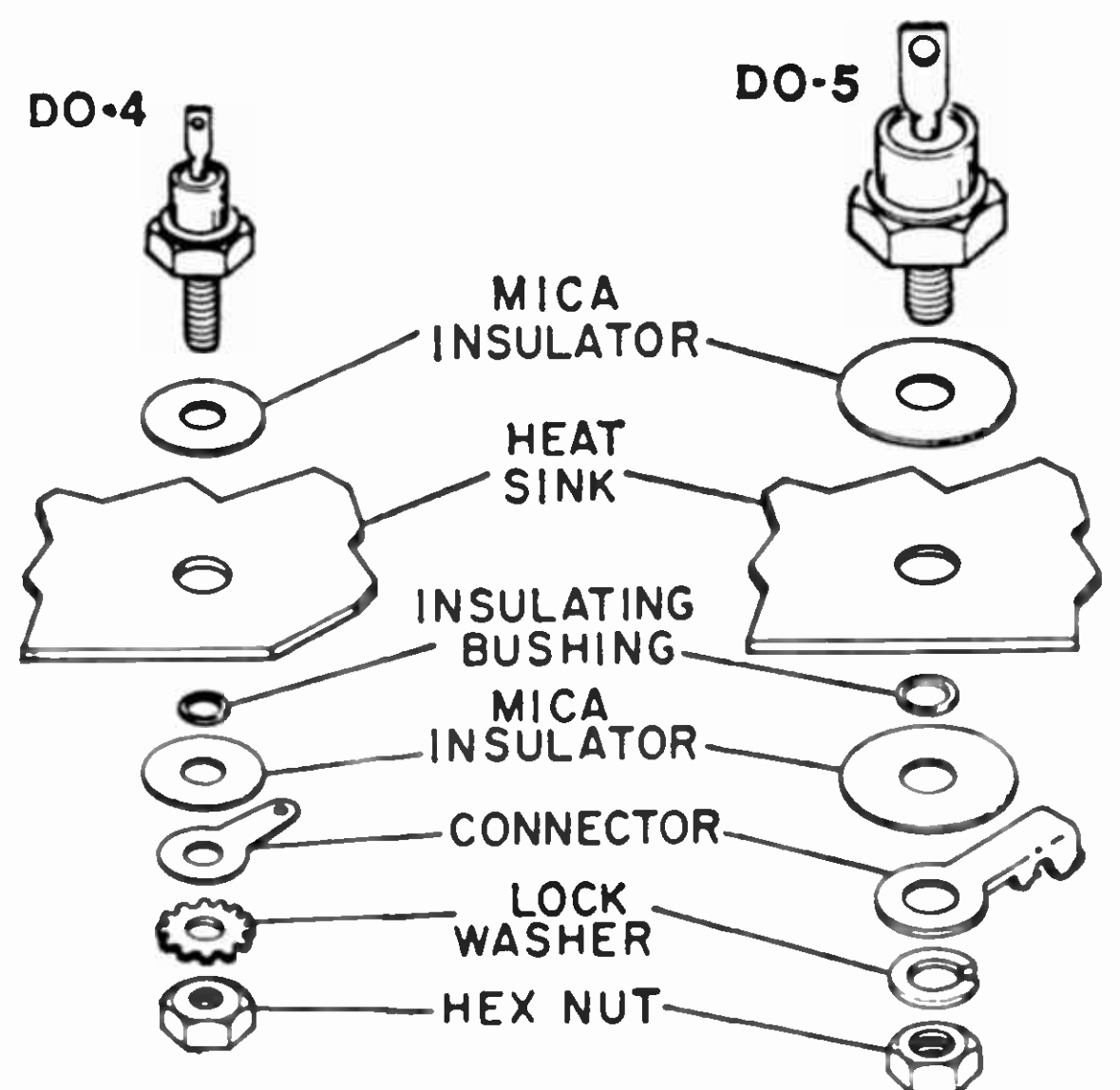


Fig. 350—Suggested mounting arrangements for DO-4 and DO-5 packages.

Symbols

Although semiconductor-device symbols have not yet been standardized throughout the industry, many symbols have become fairly well established by common usage. The symbols used in this Manual are listed and defined in this section.

GENERAL SEMICONDUCTOR SYMBOLS

df	duty factor
η (eta)	efficiency
NF	noise figure
T	temperature
T_A	ambient temperature
T_C	case temperature
T_J	junction temperature
T_{MF}	mounting-flange temperature
T_S	soldering temperature
T_{STG}	storage temperature
θ	thermal resistance
θ_{J-A}	thermal resistance, junction-to-ambient
θ_{J-C}	thermal resistance, junction-to-case
θ_{J-HS}	thermal resistance, junction-to-heat sink
θ_{J-MF}	thermal resistance, junction-to-mounting-flange
t	time
t_d	delay time
$t_d + t_r$	turn-on time
t_f	fall time
t_p	pulse time
t_r	rise time
t_s	storage time
$t_s + t_f$	turn-off time
τ (tau)	time constant
τ_s	saturation stored-charge time constant

TRANSISTOR SYMBOLS

$C_{b'e}$	collector-to-base feedback capacitance
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C_c	collector-to-case capacitance
C_{cb}	collector-to-base feedback capacitance
C_{ibo}	input capacitance, open circuit (common base)
C_{ieo}	input capacitance, open circuit (common emitter)
CM	cross modulation
C_{obo}	output capacitance, open circuit (common base)
C_{oeo}	output capacitance, open circuit (common emitter)
$E_{S/b}$	second-breakdown energy
f_c	cutoff frequency
f_{hfb}	small-signal forward-current transfer-ratio cutoff frequency, short-circuit (common base)
f_{hfe}	small-signal forward-current transfer-ratio cutoff frequency, short-circuit (common emitter)
f_T	gain-bandwidth product (frequency at which small-signal forward-current transfer ratio, common emitter, extrapolates to unity)
g_{me}	small-signal transconductance (common emitter)
G_{PB}	large-signal average power gain (common base)
G_{pb}	small-signal average power gain (common base)

G_{PE}	large-signal average power gain (common emitter)	I_{CES}	collector-cutoff current, base short-circuited to emitter
G_{pe}	small-signal average power gain (common emitter)	I_{CEV}	collector-cutoff current, specified voltage between base and emitter
h_{FB}	static forward-current transfer ratio (common base)	I_{CEX}	collector-cutoff current, specified circuit between base and emitter
h_{fb}	small-signal forward-current transfer ratio, short circuit (common base)	I_{CS}	switching current (at minimum h_{FE} per specification)
h_{FE}	static forward-current transfer ratio (common emitter)	I_E	emitter current
h_{fe}	small-signal forward-current transfer ratio, short circuit (common emitter)	I_{EBO}	emitter-cutoff current, collector open
h_{ib}	small-signal input impedance, short circuit (common base)	$I_{S/b}$	second-breakdown collector current
h_{IE}	static input resistance (common emitter)	MAG	maximum available amplifier gain
h_{ie}	small-signal input impedance, short circuit (common emitter)	MAG _c	maximum available conversion gain
h_{ob}	small-signal output impedance, open circuit (common base)	MUG	maximum usable amplifier gain
h_{oe}	small-signal output impedance, open circuit (common emitter)	P_{BE}	total dc or average power input to base (common emitter)
h_{rb}	small-signal reverse-voltage transfer ratio, open circuit (common base)	p_{BE}	total instantaneous power input to base (common emitter)
h_{re}	small-signal reverse-voltage transfer ratio, open circuit (common emitter)	P_{CB}	total dc or average power input to collector (common base)
I_B	base current	p_{CB}	total instantaneous power input to collector (common base)
I_{B1}	turn-on current	P_{CE}	total dc or average power input to collector (common emitter)
I_{B2}	turn-off current	p_{CE}	total instantaneous power input to collector (common emitter)
I_C	collector current	P_{EB}	total dc or average power input to emitter (common base)
i_c	collector current, instantaneous value	p_{EB}	total instantaneous power input to emitter (common base)
I_{CB}	collector-cutoff current	P_{IB}	large-signal input power (common base)
I_{CBO}	collector-cutoff current, emitter open	P_{ib}	small-signal input power (common base)
I_{CEO}	collector-cutoff current, base open	P_{IE}	large-signal input power (common emitter)
I_{CER}	collector-cutoff current, specified resistance between base and emitter	P_{ic}	small-signal input power (common emitter)

P_{OB}	large-signal output power (common base)		
P_{ob}	small-signal output power (common base)		
P_{OE}	large-signal output power (common emitter)		
P_{oe}	small-signal output power (common emitter)		
Q_b	stored base charge		
r_{bb}'	intrinsic base spreading resistance		
$r_b'C_c$	collector - to - base time constant		
$r_{CE}(\text{sat})$	collector-to-emitter saturation resistance		
$Re(h_{ie})$	real part of small-signal input impedance, short circuit (common emitter)		
R_G	generator resistance		
R_{i_e}	input resistance (common emitter)		
R_L	load resistance		
R_{o_e}	output resistance (common emitter)		
R_s	source resistance		
τ (thermal)	thermal time constant		
V_{BB}	base-supply voltage		
V_{BC}	base-to-collector voltage		
V_{BE}	base-to-emitter voltage		
$V_{BE}(\text{sat})$	base-to-emitter saturation voltage		
$V_{(BR)CBO}$	collector-to-base breakdown voltage, emitter open		
$V_{(BR)CEO}$	collector - to - emitter breakdown voltage, base open		
$V_{(BR)CER}$	collector - to - emitter breakdown voltage, specified resistance between base and emitter		
$V_{(BR)CES}$	collector - to - emitter breakdown voltage, base short-circuited to emitter		
$V_{(BR)CEV}$	collector - to - emitter breakdown voltage, specified voltage between base and emitter		
$V_{(BR)EBO}$	emitter-to-base breakdown voltage, collector open		
V_{CB}	collector-to-base voltage		
$V_{CB}(\text{fl})$	dc open-circuit voltage between collector and		base (floating potential), emitter biased with respect to base
		$V_{CE}(\text{fl})$	dc open-circuit voltage between collector and emitter (floating potential), base biased with respect to emitter
		V_{CBO}	collector-to-base voltage (emitter open)
		V_{CBV}	collector-to-base voltage, specified voltage between emitter and base
		V_{CC}	collector-supply voltage
		V_{CE}	collector-to-emitter voltage
		V_{CEO}	collector-to-emitter voltage, base open
		V_{CER}	collector-to-emitter voltage, specified resistance between base and emitter
		V_{CES}	collector-to-emitter voltage, base short-circuited to emitter
		V_{CEV}	collector-to-emitter voltage, specified voltage between base and emitter
		$V_{CE}(\text{sat})$	collector-to-emitter saturation voltage
		V_{EB}	emitter-to-base voltage
		$V_{EB}(\text{fl})$	dc open-circuit voltage between emitter and base (floating potential), collector biased with respect to base
		V_{EBO}	emitter-to-base voltage, collector open
		V_{EE}	emitter-supply voltage
		V_{RT}	reach-through voltage
		V_G	voltage gain
		$1/Y_{22}(\text{real})$	real part of short-circuit output impedance
		Y_{fe}	forward transconductance
		Y_{ie}	input admittance
		Y_{oe}	output admittance
		Y_{re}	reverse transconductance
MOS FIELD-EFFECT TRANSISTOR SYMBOLS			
		A	voltage amplification ($= Y_{fs}/Y_{os} + Y_L$)
		B_{os}	$= C_{ds}$
		c_c	intrinsic channel capacitance

C_{ds}	drain-to-source capacitance (includes approximately 1-pF drain-to-case and interlead capacitance)	$r_{i_{ss}}$	input resistance
C_{gd}	gate-to-drain capacitance (includes 0.1-pF interlead capacitance)	$r_{o_{ss}}$	output resistance
C_{gs}	gate-to-source interlead and case capacitance	V_{DB}	drain-to-substrate voltage
$C_{i_{ss}}$	small-signal input capacitance, short circuit	V_{DG}	drain-to-gate voltage
$C_{o_{ss}}$	small-signal output capacitance, short circuit	V_{DG1}	drain-to-gate No. 1 voltage
$C_{r_{ss}}$	small-signal reverse transfer capacitance, short circuit	V_{DG2}	drain-to-gate No. 2 voltage
e_n	equivalent input noise voltage	V_{DS}	drain-to-source voltage
g_c	forward conversion conductance	V_{G1S}	gate No. 1-to-source voltage
g_{fs}	forward transconductance	$V_{G1S(off)}$	gate No. 1-to-source cutoff voltage
$g_{fs}(c)$	forward conversion transconductance	V_{G2S}	gate No. 2-to-source voltage
$g_{fs}(off)$	cutoff forward transconductance	$V_{G2S(off)}$	gate No. 2-to-source cutoff voltage
g_{is}	input conductance	V_{GB}	dc gate-to-substrate voltage
g_{os}	output conductance	V_{GB}	peak gate-to-substrate voltage
G_{ps}	power gain	V_{GS}	dc gate-to-source voltage
$G_{ps(c)}$	conversion power gain	V_{GS}	peak gate-to-source voltage
I_D	dc drain current	$V_{GS(OFF)}$	gate-to-source cutoff voltage
$I_{DS(OFF)}$	drain-to-source OFF current	V_o	offset voltage
I_{DSS}	zero-bias drain current	Y_{fs}	forward transadmittance $\approx g_{fs}$
I_{G1SS}	gate No. 1 leakage current	Y_{os}	output admittance = $g_{os} + jB_{os}$, $B_{os} = \omega C_{ds}$
I_{G2SS}	gate No. 2 leakage current	Y_L	load admittance = $g_L + jB_L$
I_{GSS}	gate leakage current	$\angle \theta$	phase angle of forward transadmittance
NF	spot noise figure (generator resistance $R_G = 1$ megohm)		
r_c	effective gate series resistance	SCR SYMBOLS	
r_d	active channel resistance	Critical dv/dt	critical rate of applied forward voltage
r_d'	unmodulated channel resistance	di _T /dt	rate of change of on-state current
$r_{DS(ON)}$	drain-to-source ON resistance	I_{DOM}	peak off-state current (open gate)
$R_{DS(off)}$	drain-to-source cutoff resistance	I_{GT}	average trigger current
r_{gd}	gate-to-drain leakage resistance	i_{HO}	instantaneous holding current
r_{gs}	gate-to-source leakage resistance	I_{RRDM}	repetitive peak reverse current (open gate)
		i_T	instantaneous on-state current
		$I_{T(AV)}$	average on-state current
		$I_{T(RMS)}$	rms on-state current
		I_{TSM}	surge (non-repetitive) on-state current

$[I_{TS(RMS)}]^{2t}$	rms surge (non-repetitive) on-state current
$P_{G(AV)}$	average on-state or off-state gate power dissipation
P_{GM}	peak on-state or off-state gate power dissipation
R_L	load resistance
t_{gt}	gate controlled turn-on time
t_q	circuit commutated turn-off time
V_{DROM}	repetitive peak off-state voltage (open gate)
V_{DSOM}	non-repetitive peak forward voltage (open gate)
$V_{F(BOOD)}$	instantaneous forward breakover voltage (open gate)
V_{GT}	average trigger voltage
V_{RRROM}	repetitive peak reverse voltage (open gate)
V_{RSOM}	non-repetitive peak reverse voltage (open gate)
V_T	instantaneous on-state voltage

TRIAC SYMBOLS

Commutating dv/dt	critical rate of applied commutating voltage
Critical dv/dt	critical rate-of-rise of off-state voltage
I_{DROM}	peak off-state current
I_{GT}	dc gate-trigger current
I_{GTM}	peak gate-trigger current
I_{HO}	dc holding current
i_T	instantaneous on-state current
$I_{T(RMS)}$	rms on-state current
I_{TSM}	peak surge (non-repetitive) on-state current
$P_{G(AV)}$	average gate power dissipation
P_{GM}	peak gate power dissipation
R_L	load resistance
t_{gt}	gate-controlled turn-on time
V_D	instantaneous off-state voltage
V_{DROM}	repetitive peak off-state voltage
V_{GT}	dc gate-trigger voltage
V_T	instantaneous on-state voltage

RECTIFIER SYMBOLS

C_S	shunt capacitance
I_{FAV}	average forward current
$i_{FM(rep)}$	peak recurrent forward current
$i_{FM(surge)}$	peak surge forward current
I_{RM}	maximum reverse current
V_{FM}	maximum dc forward voltage drop
$V_M(block)$	maximum dc blocking voltage
V_{RM}	peak reverse voltage
$V_{RM(non-rep)}$	non-repetitive (transient) peak reverse voltage
$V_{RM(rep)}$	repetitive peak reverse voltage
V_{RMS}	rms supply voltage

TUNNEL-DIODE SYMBOLS

C_j	junction capacitance
C_p	case capacitance
C_{tv}	valley-point terminal capacitance
f_c	characteristic frequency (figure of merit)
f_{max}	maximum frequency of oscillation
f_r	resistive cutoff frequency
g_j	junction resistance
I_i	inflection-point current
I_p	peak-point current
I_p/C_{tv}	speed index
I_v	valley-point current
L	series inductance
L_{ex}	excess series inductance
r_j	junction resistance
r_s	series resistance
t_{sw}	characteristic switching time
V_i	inflection-point voltage
V_p	peak-point voltage
V_{pp}	projected-peak-point voltage
V_v	valley-point voltage
Y_t	terminal admittance

Static (DC) Parameters

Inflection point—the point on the forward current-voltage characteristic at which the slope of the characteristic reaches its most negative value

Peak point—the point on the forward current-voltage characteristic corresponding to the lowest positive (forward) voltage at which $dI/dV = 0$

Projected peak point—the point on the forward current characteristic where the current is equal to the peak-point current and where the voltage is greater than the valley-point voltage

Valley point—the point on the forward current-voltage characteristic corresponding to the second lowest positive (forward) voltage at which $dI/dV = 0$

RCA MILITARY-SPECIFICATION TYPES

TYPE	MIL-S-19500/	TYPE	MIL-S-19500/
Transistors			
JAN-2N220	1	JAN-TX2N1485	180
JAN-2N384	27	JAN-2N1486	180
JAN-2N388	65	JAN-TX2N1486	180
JAN-2N398A	174	JAN-2N1487	208
JAN-2N404	20	JAN-2N1488	208
JAN-2N404A	20	JAN-2N1489	208
JAN-2N918	301	JAN-2N140	208
JAN-TX2N918	301	JAN-2N1493	247
JAN-2N1183	143	JAN-2N1853	171
JAN-2N1183A	143	JAN-2N1854	172
JAN-2N1183B	143	JAN-2N2015	248
JAN-2N1184	143	JAN-2N2016	248
JAN-2N1184A	143	JAN-2N2708	302
JAN-2N1184B	143	JAN-2N2857	343
JAN-2N1224	189	JAN-TX2N2857	343
JAN-2N1225	189	JAN-2N3375	341
JAN-2N1302	126	JAN-TX2N3375	341
JAN-2N1303	126	JAN-2N3439	368
JAN-2N1304	126	JAN-2N3440	368
JAN-2N1305	126	JAN-2N3441	369
JAN-2N1306	126	JAN-2N3442	370
JAN-2N1307	126	JAN-2N3553	341
JAN-2N1308	126	JAN-TX2N3553	341
JAN-2N1309	126	JAN-2N4440	341
JAN-2N1479	207	JAN-TX2N4440	341
JAN-2N1480	207		
JAN-2N1481	207	Rectifiers	
JAN-2N1482	207	JAN-1N249B	134
JAN-2N1483	180	JAN-1N250B	134
JAN-TX2N1483	180	JAN-1N1184	297
JAN-2N1484	180	JAN-1N1186	297
JAN-TX2N1484	180	JAN-1N1188	297
JAN-2N1485	180	JAN-1N1190	297
		JAN-1N1198A	134
		JAN-1N2135A	134

Copies of specification sheets may be obtained by directing requests to *Specifications Division, Naval Supply Depot, 5801 Tabor Avenue, Philadelphia 20, Pa., Attn: CDS*

Selection Charts

The accompanying charts classify RCA semiconductor devices by function, by material, and by performance level. These charts are particularly useful for an initial selection of suitable devices for a specific application. More complete data on these devices, given in the Technical

Data section, should then be consulted to determine the most suitable type. Data charts for rectifiers, other semiconductor diodes, and photoconductive devices are given at the end of the Technical Data section.

TRANSISTORS

Audio-Frequency Applications— Linear Operations

SMALL SIGNAL—CLASS A

Silicon n-p-n

Dissipations up to 5 W

2N697	2N2897	40398
2N699	2N3053	40399
2N718A	2N3241A	40400
2N720A	2N3242A	40450
2N1613	2N4074	40451
2N1711	2N5183	40452
2N1893	40084	40453
2N2102	40231	40454
2N2270	40232	40455
2N2405	40233	40456
2N2895	40234	40458
2N2896	40397	40459

Germanium p-n-p

Dissipations up to 165 mW

2N104	2N405	40329
2N109	2N406	40359
2N175	2N591	40395
2N215	2N1613	40490
2N217	2N1614	
2N220	2N2953	

Germanium n-p-n

Dissipations up to 20 mW

2N1010

POWER—CLASS A, AB, B

Silicon n-p-n

Dissipations up to 5 W

2N697	2N4074	40397
2N699	40084	40398
2N1479‡	40309	40399
2N1480‡	40311	40400
2N1481‡	40314	40407
2N1482‡	40315	40408
2N1613	40317	40450
2N1700‡	40320	40451
2N1711	40321	40452
2N1893	40323	40453
2N2102	40326	40454
2N2270	40327	40455
2N2405	40354	40456
2N2895	40355	40539
2N2896	40360	40611
2N2897	40361	40616
2N3053	40366●	40625
2N3241A	40367●	40628
2N3242A	40385●	40635

‡ Hometaxial base type.
● High-reliability type.

Dissipations above 5 W to 29 W

2N1483‡	40250V1	40374*
2N1484‡	40310	40375*
2N1485‡	40312	40389*
2N1486‡	40316	40390*
2N1701‡	40324	40392
2N3054‡	40346	40409*
2N3439	40347‡	40412
2N3440	40347V1*‡	40422
2N3441‡	40347V2‡	40423*
2N4063	40348‡	40424
2N4064	40348V1*‡	40425*
2N4296	40348V2‡	40426
2N4297	40349‡	40427*
2N4298	40349V1*‡	40491
2N4299	40349V2‡	40544
2N5320	40368●	40546
2N5321	40372*	40547
40250‡	40373*	40594

Dissipations above 29 W to 100 W

2N1487‡	2N5240‡	40364
2N1488‡	2N5293*‡	40369‡●
2N1489‡	2N5294‡	40464
2N1490‡	2N5295*‡	40466
2N1702‡	2N5296‡	40513*‡
2N3263	2N5297*‡	40514‡
2N3264	2N5298‡	40542‡
2N3583	2N5490*‡	40543‡
2N3584	2N5491‡	40613
2N3585	2N5492*‡	40618
2N3878	2N5493‡	40621
2N3879	2N5494*‡	40622
2N4240	2N5495‡	40624
2N4347‡	2N5496*‡	40627
2N5034‡	2N5497‡	40629
2N5035*‡	40313	40630
2N5036‡	40318	40631
2N5037*‡	40322	40632
2N5239‡	40328	40633

Dissipation above 100 W to 150 W

2N2015	2N3772‡	2N5579‡
2N2016	2N3773‡	2N5580‡
2N2338‡	2N4348‡	40251‡
2N3055‡	2N5575‡	40325
2N3265	2N5576‡	40363
2N3266	2N5577‡	40411‡
2N3442‡	2N5578‡	40636
2N3771‡		

Silicon p-n-p

Dissipation to 10 W

2N4036	2N5322	40410
2N4037	40319	40537
2N4314	40362	40538
2N5323	40391*	40595
2N5415	40394*	40634
2N5416	40406	

Germanium n-p-n

Dissipation to 300 mW

2N647	2N649	40396
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Germanium p-n-p

Dissipation to 30 W

2N176	2N1184B	40050
2N270	2N1905	40051
2N351	2N1906	40253
2N376	2N2147	40254
2N407	2N2148	40396
2N408	2N2869/	40421
2N1183	2N301	40462
2N1183A	2N2870/	40612
2N1183B	2N301A	40623
2N1184	40022	40626
2N1184A		

HIGH-VOLTAGE

Germanium p-n-p

2N3730	2N3732	40439
2N3731	2N4346	40440

Silicon n-p-n

2N2016	2N4063	40349‡
2N2102	2N4064	40349V1*‡
2N2405	2N4068	40349V2‡
2N3263	2N4069	40354
2N3264	2N4240	40355
2N3265	2N4296	40366●
2N3266	2N4297	40373*
2N3439	2N4298	40374*
2N3440	2N4299	40375*
2N3441‡	2N4347‡	40385●
2N3442‡	2N4348‡	40390*
2N3583	2N4390	40422
2N3584	2N5184	40423*
2N3585	2N5185	40424
2N3773	2N5239‡	40425*
2N3878	2N5240‡	40426
2N3879	40346	40427*

* For printed-circuit-board applications.

‡ Hometaxial base type.

● High-reliability type.

**Radio-Frequency Applications—
Linear and Class C Operation**

SMALL SIGNAL

**MOS FET Silicon N-Channel-Single
Insulated Gate**

3N128	3N152	40468A
3N139	3N154	40559
3N142	40467A	40559A
3N143	40468	

**MOS FET Silicon N-Channel-Dual
Insulated Gate**

3N140	40600	40603
3N141	40601	40604
3N159	40602	40673

Silicon n-p-n

f_T to 700 MHz (Typ.)

2N2102	2N2897	2N5189●
2N2270	2N3053	40084
2N2405	2N5181	40354
2N2895	2N5182	40355
2N2896	2N5188●	40637

f_T to 1200 MHz (Min.)

2N917	40235	40414
2N918	40236	40472
2N2708	40237	40473
2N2857	40238	40474
2N3478	40239	40475
2N3600	40240	40476
2N3839	40242	40477
2N3932	40243	40478
2N3933	40244	40479
2N4259	40245	40480
2N4934	40246	40481
2N4935	40294●	40482
2N4936	40295●	40517
2N5109	40296●	40518
2N5179	40405	40519
2N5180	40413	

Germanium p-n-p

f_T to 132 MHz (Typ.)

2N140	2N1178	2N1527
2N274	2N1179	2N1631
2N370	2N1180	2N1632
2N372	2N1224	2N1637
2N384	2N1225	2N1638
2N409	2N1226	2N1639
2N410	2N1395	40261
2N411	2N1396	40262
2N412	2N1397	40487
2N1023	2N1524	40488
2N1066	2N1525	40489
2N1177	2N1526	

POWER—"OVERLAY" CONSTRUCTION

Silicon n-p-n

2N1491	2N4933	40290
2N1492	2N5016	40291
2N1493	2N5070	40292
2N2631	2N5071	40305●
2N2876	2N5090	40306●
2N3118	2N5102	40307●
2N3229	2N5108	40340
2N3375	2N5470	40341
2N3553	40080	40405
2N3632	40081	40446
2N3733	40082	40577●
2N3866	40279●	40578●
2N4012	40280	40581
2N4427	40281	40582
2N4440	40282	40608
2N4932		

**SWITCHING AND PULSE
APPLICATIONS
Computer and Power**

**COMPUTER—LOW LEVEL, MEDIUM-SPEED
LOGIC SWITCHING**

Silicon n-p-n

f_T to 175 MHz (Min.)

2N697	2N2897	2N5202
2N699	2N3053	2N5320
2N718A	2N3241A	2N5321
2N720A	2N3242A	40084
2N1613	2N3262	40375*
2N1711	2N3263	40389*
2N1893	2N3264	40392
2N2102	2N3265	40450
2N2270	2N3266	40451
2N2405	2N3878	40458
2N2895	2N3879	40459
2N2896	2N5183	

Silicon p-n-p

f_T to 60 MHz (Min.)

2N4036	2N5322	40391*
2N4037	2N5323	40394*
2N4314		

HIGH-SPEED LOGIC SWITCHING

Silicon n-p-n

f_T to 600 MHz (Min.)

2N706	2N2369A	2N3261
2N706A	2N2475	2N5186
2N709	2N3011	2N5187
2N834	2N3119	

* For printed-circuit-board applications.
● High-reliability type.

HIGH-VOLTAGE SWITCHING

Silicon p-n-p

f_T to 600 MHz (Min.)

2N2476	2N3512	2N5189 [●]
2N2477	2N5188 [●]	2N5262
2N3261		

Germanium p-n-p

2N398	2N398A	2N398B
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LOW- AND MEDIUM-SPEED SWITCHING

Germanium p-n-p

f_T to 50 MHz (Min.)

2N396	2N1300	2N1309
2N404	2N1301	2N1384
2N404A	2N1303	2N1683
2N414	2N1305	2N1853
2N581	2N1307	2N1854
2N582		

Germanium n-p-n

f_T to 15 MHz (Min.)

2N388	2N1091	2N1308
2N388A	2N1302	2N1605
2N585	2N1304	2N1605A
2N1090	2N1306	

CHOPPER AND MULTIPLEX SERVICE

MOS FET Silicon N-Channel-Single Insulated Gate

3N138	3N153
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POWER—LOW SPEED SWITCHING

Silicon n-p-n

Dissipations to 8.75 W

2N697	2N3053	40349‡
2N699	2N3262	40349V1*‡
2N718A	40250V1*	40360
2N720A	40309	40361
2N1479‡	40311	40366 [●]
2N1480‡	40314	40367 [●]
2N1481‡	40315	40372*
2N1482‡	40317	40374*
2N1613	40320	40375*
2N1700‡	40321	40385
2N1711	40323	40389*
2N1893	40326	40390*
2N2102	40327	40392
2N2270	40346V1*	40407
2N2405	40347*	40408
2N2895	40347V1*‡	40409*
2N2896	40348‡	40412V1*
2N2897	40348V1*‡	

Dissipations above 8.75 W to 50 W

2N1483‡	2N4298	40312
2N1484‡	2N4299	40313
2N1485‡	2N5293*‡	40316
2N1486‡	2N5294‡	40318
2N1701‡	2N5295*‡	40322
2N3054‡	2N5296‡	40324
2N3439	2N5297*‡	40328
2N3440	2N5298‡	40346
2N3441‡	2N5490*‡	40346V2
2N3583	2N5491‡	40347V2‡
2N3584	2N5492*‡	40348V2‡
2N3585	2N5493‡	40349V2‡
2N3878	2N5494*‡	40364
2N3879	2N5495‡	40368 [●]
2N4063	2N5496*‡	40412
2N4064	2N5497‡	40412V2
2N4240	40250‡	40464
2N4296	40310	40466
2N4297		

Dissipations above 50 W to 150 W

2N1487‡	2N3442‡	2N5576‡
2N1488‡	2N3771‡	2N5577‡
2N1489‡	2N3772‡	2N5578‡
2N1490‡	2N3773‡	2N5579‡
2N1702‡	2N4347‡	2N5580‡
2N2015	2N4348‡	40251‡
2N2016	2N5034‡	40325
2N2338‡	2N5035*‡	40363
2N3055‡	2N5036‡	40369‡ [●]
2N3263	2N5037*‡	40411‡
2N3264	2N5039‡	40513*‡
2N3265	2N5240‡	40514‡
2N3266	2N5575‡	

Silicon p-n-p

Dissipations to 7 W

40319	40391*	40406
40362	40394*	40410*

Germanium p-n-p

Dissipation to 30 W

2N586	2N1183	2N1184
2N1905	2N1183A	2N1184A
2N1906	2N1183B	2N1184B

* For printed-circuit-board applications.
‡ Hometaxial base type.
● High-reliability type.

HIGH-VOLTAGE SWITCHING

Silicon n-p-n

Collector-to-Emitter Voltage to 350 V (max.)

2N3439	2N4069	40349V1*‡
2N3440	2N4240	40349V2‡
2N3441‡	2N4347‡	40354
2N3442‡	2N4348‡	40373*
2N3583	2N4390	40374*
2N3584	2N5239‡	40385●
2N3585	2N5240‡	40390*
2N3773	40346	40412
2N4063	40346V1*	40412V1*
2N4064	40346V2	40412V2
2N4068	40349‡	

Silicon p-n-p

Collector-to-Emitter Sustaining Voltage to -300 V (max.)

2N5415 2N5416

* For printed-circuit-board applications.
‡ Hometaxial base type.
● High-reliability type.

THYRISTORS

TRIACS

2N5441	40485	40533
2N5442	40486	40534
2N5444	40502	40535
2N5445	40503	40536
2N5567	40509	40575
2N5568	40510	40576
2N5569	40511	40638
2N5570	40512	40639
2N5571	40525	40660
2N5572	40526	40661
2N5573	40527	40662
2N5574	40528	40663
40429	40529	40664
40430	40530	40667
40431	40531	40668
40432	40532	40669

DIACS

1N5411	40583
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SILICON CONTROLLED RECTIFIERS

2N681	2N3228	40378
2N682	2N3525	40379
2N683	2N3528	40504
2N684	2N3529	40505
2N685	2N3668	40506
2N686	2N3669	40507
2N687	2N3670	40508
2N688	2N3870	40553
2N689	2N3871	40554
2N690	2N3872	40555
2N1842A	2N3873	40640
2N1843A	2N3896	40641
2N1844A	2N3897	40654
2N1845A	2N3898	40655
2N1846A	2N3899	40656
2N1847A	2N4101	40657
2N1848A	2N4102	40658
2N1849A	2N4103	40659
2N1850A	40216	

DIODES

TUNNEL DIODES

40561	40566	40571
40562	40567	40572
40563	40568	40573
40564	40569	40574
40565	40570	

DAMPER DIODES

1N4785	40442
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COMPENSATING DIODES

1N2326	40428
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RECTIFIERS

SILICON RECTIFIERS—LOW POWER

1N536	1N3194	1N445B
1N537	1N3195	1N5211
1N538	1N3196	1N5212
1N539	1N3253	1N5213
1N540	1N3254	1N5214
1N547	1N3255	1N5215
1N1095	1N3256	1N5216
1N1763A	1N3563	1N5217
1N1764A	1N3754	1N5218
1N2858A	1N3755	40265
1N2859A	1N3756	40266
1N2860A	1N440B	40267
1N2861A	1N441B	40495
1N2862A	1N442B	40642
1N2863A	1N443B	40643
1N2864A	1N444B	40644
1N3193		

SILICON RECTIFIER STACKS

CR101	CR301	CR323
CR102	CR302	CR324
CR103	CR303	CR325
CR104	CR304	CR331
CR105	CR305	CR332
CR106	CR306	CR333
CR107	CR307	CR334
CR108	CR311	CR335
CR109	CR312	CR341
CR110	CR313	CR342
CR201	CR314	CR343
CR203	CR315	CR344
CR204	CR316	CR351
CR206	CR317	CR352
CR208	CR321	CR353
CR210	CR322	CR354
CR212		

SILICON RECTIFIERS—HIGH POWER

1N248C	1N1203A	40108
1N249C	1N1204A	40109
1N250C	1N1205A	40110
1N1183A	1N1206A	40111
1N1184A	1N1341B	40112
1N1186A	1N1342B	40113
1N1187A	1N1344B	40114
1N1188A	1N1345B	40115
1N1189A	1N1346B	40208
1N1190A	1N1347B	40209
1N1195A	1N1348B	40210
1N1196A	1N1612	40211
1N1197A	1N1613	40212
1N1198A	1N1614	40213
1N1199A	1N1615	40214
1N1200A	1N1616	40259 [•]
1N1202A		

SILICON RECTIFIER BRIDGES

Single-Phase Operation

CR401	CR404	CR407
CR402	CR405	CR408
CR403	CR406	CR409

Three-Phase Operation

CR501	CR503	CR505
CR502	CR504	CR506

Plug-In Types

CR273/ 8008	CR274/ 872A	CR275/ 866A/ 3B28/ 3B25
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PHOTOCELLS

Broad-Area Cadmium-Sulfide Types (5100A°)

4403	SQ2502	SQ2521	SQ2534	SQ2544	SQ2546
4404	SQ2503	SQ2526	SQ2535	SQ2544V1	SQ2554
4448	SQ2508	SQ2527	SQ2536	SQ2545	SQ2555
4453	SQ2519	SQ2529	SQ2543	SQ2545V1	SQ2556
7163	SQ2520				

Technical Data

This section contains detailed technical data for all current RCA transistors, thyristors, and compensating, damper, and emitting diodes. Tabular data for RCA discontinued transistors and for silicon rectifiers, tunnel diodes, and photocells are given at the end of the section. Outline drawings and information on mounting hardware for all RCA semiconductor devices are given later in the Manual (see Table of Contents). For Key: Basing Diagrams, see inside back cover.

Devices are listed in this section according to the numerical-alphabetical-numerical sequence of their type designations. Unless otherwise specified, voltages and currents are dc values, and values are obtained at an ambient temperature of 25°C.

Maximum device ratings shown are based on the Absolute Maximum system, and are limiting values of operating and environmental conditions which should not be exceeded by any device of a specified type under any conditions of operation. Effective use of these ratings requires close control of supply-voltage variations, component variations,

equipment-control adjustment, load variations, signal variations, and environmental conditions.

Voltage ratings are established with reference to a specified electrode (e.g., collector-to-emitter voltage), and indicate the maximum potential which can be placed across the two given electrodes before crystal breakdown occurs. These ratings may be specified with the third electrode open, or with specific bias voltages or external resistances.

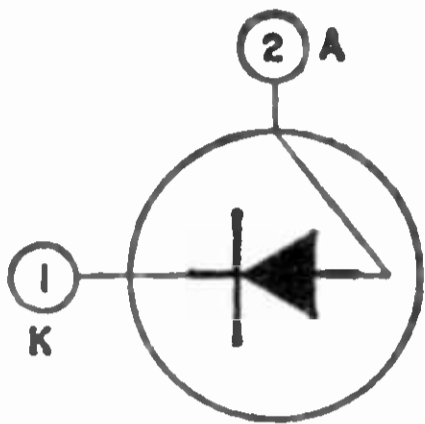
Characteristic curves represent the characteristics of an average device. Individual devices may have characteristics that range above or below the values given in the curves. Although some curves are extended beyond the maximum ratings of the devices, this extension has been made for convenience in calculations only; no device should be operated outside of its maximum ratings.

In choosing semiconductor devices for use in new electronic equipment, the designer should refer to the Selection Charts in the pages immediately preceding this section.

Refer to Charts of Rectifier Data	1N248C
Refer to Charts of Rectifier Data	1N249C
Refer to Charts of Rectifier Data	1N250C
Refer to Charts of Rectifier Data	1N440B
Refer to Charts of Rectifier Data	1N441B
Refer to Charts of Rectifier Data	1N442B
Refer to Charts of Rectifier Data	1N443B
Refer to Charts of Rectifier Data	1N444B
Refer to Charts of Rectifier Data	1N445B

1N536	Refer to Charts of Rectifier Data
1N537	Refer to Charts of Rectifier Data
1N538	Refer to Charts of Rectifier Data
1N539	Refer to Charts of Rectifier Data
1N540	Refer to Charts of Rectifier Data
1N547	Refer to Charts of Rectifier Data
1N1095	Refer to Charts of Rectifier Data
1N1183A	Refer to Charts of Rectifier Data
1N1184A	Refer to Charts of Rectifier Data
1N1186A	Refer to Charts of Rectifier Data
1N1187A	Refer to Charts of Rectifier Data
1N1188A	Refer to Charts of Rectifier Data
1N1189A	Refer to Charts of Rectifier Data
1N1190A	Refer to Charts of Rectifier Data
1N1195A	Refer to Charts of Rectifier Data
1N1196A	Refer to Charts of Rectifier Data
1N1197A	Refer to Charts of Rectifier Data
1N1198A	Refer to Charts of Rectifier Data
1N1199A	Refer to Charts of Rectifier Data
1N1200A	Refer to Charts of Rectifier Data
1N1202A	Refer to Charts of Rectifier Data
1N1203A	Refer to Charts of Rectifier Data
1N1204A	Refer to Charts of Rectifier Data
1N1205A	Refer to Charts of Rectifier Data
1N1206A	Refer to Charts of Rectifier Data
1N1341B	Refer to Charts of Rectifier Data
1N1342B	Refer to Charts of Rectifier Data
1N1344B	Refer to Charts of Rectifier Data
1N1345B	Refer to Charts of Rectifier Data
1N1346B	Refer to Charts of Rectifier Data
1N1347B	Refer to Charts of Rectifier Data
1N1348B	Refer to Charts of Rectifier Data

Refer to Charts of Rectifier Data	1N1612
Refer to Charts of Rectifier Data	1N1613
Refer to Charts of Rectifier Data	1N1614
Refer to Charts of Rectifier Data	1N1615
Refer to Charts of Rectifier Data	1N1616
Refer to Charts of Rectifier Data	1N1763A
Refer to Charts of Rectifier Data	1N1764A



COMPENSATING DIODE

1N2326

Ge alloy-junction type used in temperature- and voltage-compensation applications. Similar to JEDEC TO-1 (2-lead), Outline No.41.

MAXIMUM RATINGS

Reverse Voltage	V_{RM}	-1	V
Peak Recurrent Current	$i_{FM}(rep)$	200	mA
DC Forward Current	I_{FM}	100	mA
Temperature Range:			
Operating (T_A) and Storage (T_{STG})		-65 to 85	°C
Lead-Soldering Temperature (10 s max)	T_L	255	°C

CHARACTERISTICS

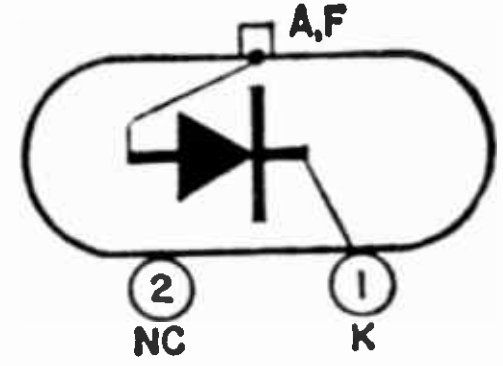
DC Forward Voltage Drop:		<i>min</i>	<i>typ</i>	<i>max</i>	
$I_{FAV} = 2$ mA	V_{FAV}	120	135	150	mV
$I_{FAV} = 100$ mA	V_{FAV}	240	260	280	mV

Refer to Charts of Rectifier Data	1N2858A
Refer to Charts of Rectifier Data	1N2859A
Refer to Charts of Rectifier Data	1N2860A
Refer to Charts of Rectifier Data	1N2861A
Refer to Charts of Rectifier Data	1N2862A
Refer to Charts of Rectifier Data	1N2863A
Refer to Charts of Rectifier Data	1N2864A
Refer to Charts of Rectifier Data	1N3193
Refer to Charts of Rectifier Data	1N3194
Refer to Charts of Rectifier Data	1N3195
Refer to Charts of Rectifier Data	1N3196
Refer to Charts of Rectifier Data	1N3253
Refer to Charts of Rectifier Data	1N3254
Refer to Charts of Rectifier Data	1N3255
Refer to Charts of Rectifier Data	1N3256
Refer to Charts of Rectifier Data	1N3563

1N3754	Refer to Charts of Rectifier Data
1N3755	Refer to Charts of Rectifier Data
1N3756	Refer to Charts of Rectifier Data

1N4785 DAMPER DIODE

Ge diffused-junction type used in transistorized 114-degree, 18-kilovolt horizontal-deflection systems in television receivers with types 2N3730, 2N3731, and 2N3732. JEDEC TO-3, Outline No.2.



MAXIMUM RATINGS

Peak Reverse Voltage	V_{RM}	320	V
Continuous Reverse Voltage	V_{RM}	60	V
Peak Forward Current	i_{FM}	10	A
Average Forward Current	I_{FM}	7	A
Temperature Range:			
Operating (T_J) and Storage (T_{STG})		-65 to 85	°C
Pin-Soldering Temperature	T_P	230	°C

CHARACTERISTICS

Peak Reverse Voltage ($I_R = 1$ mA)	V_{RM}	320 min	V
Reverse Current, Static ($V_R = 10$ V)	I_R	150 max	μA
Forward Voltage Drop, Static ($I_F = 7$ A)	V_F	0.77 max	V

1N5411 DIAC

Si all-diffused three-layer trigger diode type used for triac phase-control circuits for lamp dimming, universal-motor speed, and heat controls. JEDEC DO-26, Outline No.66.



MAXIMUM RATINGS

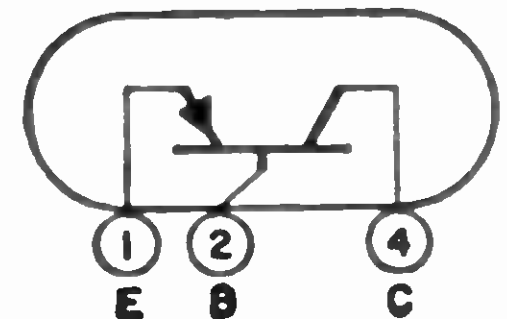
Peak Pulse Current, Forward or Reverse ($t_p = 30 \mu s$, $df = 0.004$)		2	A
Device Dissipation (T_c up to 75°C)		0.5	W
Temperature Range:			
Operating (Junction)	T_J (opr)	-40 to 100	°C
Storage	T_{STG}	-40 to 150	°C
Lead-Soldering Temperature (10 s max)	T_L	255	°C

CHARACTERISTICS (At case temperature = 25°C)

Breakover Voltage, Forward or Reverse	$V_{(BO)}$	29 to 35	V
Breakover-Voltage Symmetry	$ +V_{(BO)} - -V_{(BO)} $	± 3	V
Breakback Voltage Change, Forward or Reverse (I_{BO} (forward or reverse) = 10 mA)	ΔV	5 min	V
Peak Breakover Current	$I_{(BO)}$	50 max	μA

2N104 TRANSISTOR

Ge p-n-p alloy-junction type used in low-power audio-frequency service. JEDEC TO-40, Outline No.16.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-30	V
Collector Current	I_C	-50	mA
Transistor Dissipation:			
$T_A = 25^\circ C$	P_T	150	mW
Temperature Range:			
Operating (Ambient)	T_A (opr)	-65 to 70	°C

CHARACTERISTICS

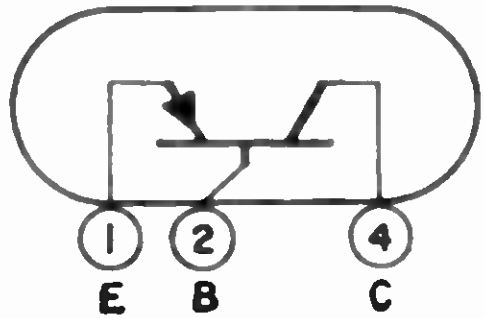
Collector-to-Base Breakdown Voltage ($I_C = -20 \mu A$, $I_E = 0$)	$V_{(BR)CBO}$	-30 min	V
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CHARACTERISTICS (cont'd)

Collector-Cutoff Current ($V_{CB} = -12\text{ V}$, $I_E = 0$)	I_{CBO}	-10 max	μA
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = -6\text{ V}$, $I_C = -1\text{ mA}$)	h_{fe}	44 min	
Small-Signal Forward-Current Transfer Ratio Cutoff Frequency	f_{hfb}	0.7	MHz
Output Capacitance	C_{obo}	40	pF
Power Gain	G_{pe}	32.4	dB
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	0.4	$^{\circ}\text{C}/\text{mW}$

Refer to Chart of Discontinued Transistors

2N105



TRANSISTOR

2N109

Ge p-n-p alloy-junction type used in low-power, small-signal and large-signal audio applications in consumer-product equipment. JEDEC TO-40, Outline No.16.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-35	V
Collector-to-Emitter Voltage	V_{CEO}	-25	V
Emitter-to-Base Voltage	V_{EBO}	-12	V
Collector Current	I_C	-150	mA
Transistor Dissipation:			
$T_A = 25^{\circ}\text{C}$	P_T	165	mW
T_A above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 71	$^{\circ}\text{C}$
Storage	T_{STG}	-65 to 85	$^{\circ}\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	255	$^{\circ}\text{C}$

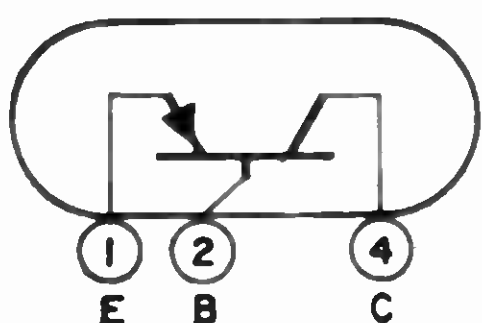
CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = -50\ \mu\text{A}$, $I_E = 0$)	$V_{(BR)CBO}$	-35 min	V
Collector-to-Emitter Breakdown Voltage ($I_C = -1\ \text{mA}$, $I_E = 0$)	$V_{(BR)CEO}$	-25 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -7\ \mu\text{A}$, $I_C = 0$)	$V_{(BR)EBO}$	-12 min	V
Collector-to-Emitter Saturation Voltage ($I_C = -50\ \text{mA}$, $I_E = -5\ \text{mA}$)	$V_{CE}(\text{sat})$	-0.15 max	V
Base-to-Emitter Voltage ($V_{CE} = -1\ \text{V}$, $I_C = -50\ \text{mA}$)	V_{BE}	0.2 to 0.4	V
Collector-Cutoff Current ($V_{CB} = -30\ \text{V}$, $I_E = 0$)	I_{CBO}	-14 max	μA
Emitter-Cutoff Current ($V_{EB} = -12\ \text{V}$, $I_C = 0$)	I_{EBO}	-7 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = -1\ \text{V}$, $I_C = -50\ \text{mA}$)	h_{FE}	75 min	
Power Gain Δ ($f = 0.001\ \text{MHz}$)	G_{pe}	33	dB
Total Harmonic Distortion Δ ($P_{oe} = 0.16\ \text{W}$)	THD	10 max	$\%$
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = -6\ \text{V}$, $I_E = -1\ \text{mA}$, $f = 1\ \text{kHz}$)	h_{fe}	50 to 150	
Small-Signal Input Impedance ($V_{CE} = -6\ \text{V}$, $I_E = -1\ \text{mA}$, $f = 1\ \text{kHz}$)	h_{ie}	1000 to 4000	Ω
Output Capacitance ($V_{CB} = -6\ \text{V}$, $I_C = -1\ \text{mA}$, $f = 0.5\ \text{MHz}$)	C_{obo}	20 to 60	pF

Δ This characteristic does not apply to type 2N217.

Refer to Chart of Discontinued Transistors

2N139



TRANSISTOR

2N140

Ge p-n-p alloy-junction type used primarily in converter and mixer-oscillator service in AM battery-operated portable radio receivers and automobile radio receivers operating from either a 6-volt or a 12-volt supply. JEDEC TO-40, Outline No.16.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CB0}	-16	V
Collector Current	I_C	-15	mA
Transistor Dissipation: $T_A = 25^\circ\text{C}$	P_T	80	mW
Temperature Range: Operating (Ambient)	$T_A(\text{opr})$	-65 to 71	$^\circ\text{C}$

CHARACTERISTICS

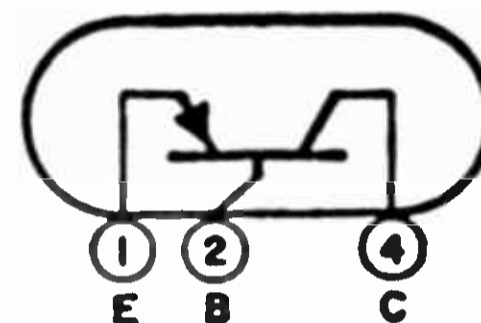
Collector-Cutoff Current ($V_{CB} = -12\text{ V}, I_E = 0$)	I_{CBO}	-6 max	
Static Forward-Current Transfer Ratio ($V_{CE} = -9\text{ V}, I_C = -0.6\text{ mA}$)	h_{FE}	75 min	MHz
Gain-Bandwidth Product	f_T	10	mV
Oscillator Injection Voltage ($f = 1\text{ MHz}$)		100 max	pF
Output Capacitance	C_{ob0}	9.5	dB
Power Gain ($f = 1\text{ MHz}$)	G_{pe}	32	μA

2N173 Refer to Chart of Discontinued Transistors

2N174 Refer to Chart of Discontinued Transistors

2N175 TRANSISTOR

Ge p-n-p alloy-junction type used in small-signal af amplifier applications in hearing aids, microphone preamplifiers, recorders, and other low-power applications. JEDEC TO-40, Outline No.16.



MAXIMUM RATINGS

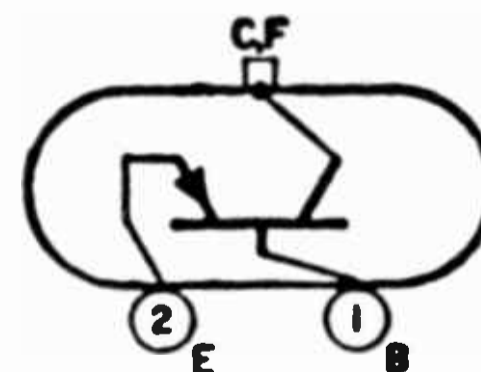
Collector-to-Base Voltage	V_{CB0}	-10	V
Collector Current	I_C	-2	mA
Transistor Dissipation: $T_A = 25^\circ\text{C}$	P_T	50	mW
Temperature Range: Operating (Ambient)	$T_A(\text{opr})$	-65 to 50	$^\circ\text{C}$

CHARACTERISTICS

Collector-Cutoff Current ($V_{CB} = -25\text{ V}, I_E = 0$)	I_{CBO}	-12 max	μA
Small-Signal Forward-Current Transfer-Ratio Cutoff Frequency ($V_{CB} = -4\text{ V}, I_C = -0.5\text{ mA}$)	f_{hfb}	0.85	MHz
Power Gain	G_{pe}	43	dB

2N176 POWER TRANSISTOR

Ge p-n-p alloy-junction type used in large-signal af amplifiers in class A power-output stages and class B push-pull amplifier stages in automobile radio receivers. JEDEC TO-3, Outline No.2.



MAXIMUM RATINGS

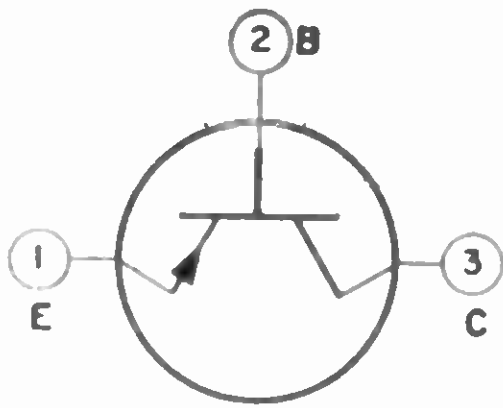
Collector-to-Base Voltage	V_{CB0}	-40	V
Collector Current	I_C	-3	A
Transistor Dissipation: $T_{MF} = 80^\circ\text{C}$	P_T	10	W
Temperature Range: Operating (Mounting Flange)	$T_{MF}(\text{opr})$	-65 to 90	$^\circ\text{C}$

CHARACTERISTICS (At mounting-flange temperature = 25°C)

Collector-Cutoff Current ($V_{CB} = -30\text{ V}, I_E = 0$)	I_{CBO}	-3 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = -2\text{ V}, I_C = -0.5\text{ A}$)	h_{FE}	63 min	
Power Gain ($f = 0.001\text{ MHz}$)	G_{pe}	35.5	dB
Total Harmonic Distortion ($P_{oe} = 2\text{ W}$)		2 max	%
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	1 max	$^\circ\text{C/W}$

Refer to Chart of Discontinued Transistors

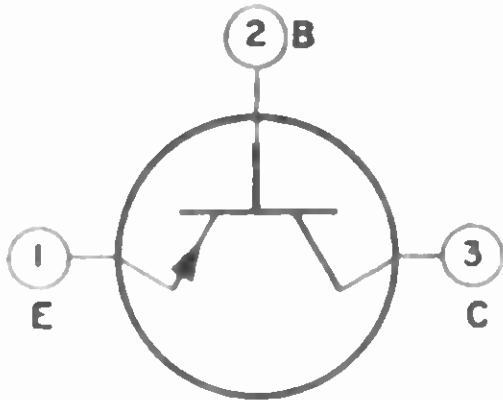
2N206



TRANSISTOR

2N215

Ge p-n-p alloy-junction type used in low-power audio-frequency amplifier applications. JEDEC TO-1, Outline No.1. This type is electrically identical with type 2N104.



TRANSISTOR

2N217

Ge p-n-p alloy-junction type used in low-power, small-signal and large-signal audio applications in consumer-product equipment. JEDEC TO-1, Outline No.1. This type is electrically identical with type 2N109 except for the following items:

CHARACTERISTICS

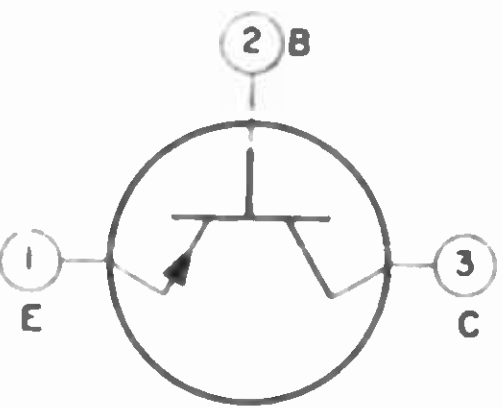
Collector-Cutoff Current ($V_{CB} = -30\text{ V}$, $I_E = 0$)	I_{CBO}	-7	μA
Static Forward-Current Transfer Ratio ($V_{CE} = -1\text{ V}$, $I_C = -50\text{ mA}$)	h_{FE}	65 to 120	

Refer to Chart of Discontinued Transistors

2N218

Refer to Chart of Discontinued Transistors

2N219



TRANSISTOR

2N220

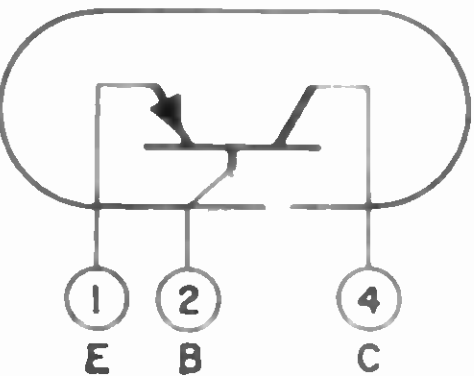
Ge p-n-p alloy-junction type used in small-signal af amplifier applications in hearing aids, microphone pre-amplifiers, recorders, and other low-power applications. JEDEC TO-1, Outline No.1. This type is electrically identical with type 2N175.

Refer to Chart of Discontinued Transistors

2N247

Refer to Chart of Discontinued Transistors

2N269



TRANSISTOR

2N270

Ge p-n-p alloy-junction type used in large-signal applications in class A driver stages and af amplifiers, and class B push-pull line- and battery-operated af amplifiers. Similar to JEDEC TO-7 (3-lead type), Outline No.9.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-25	V
Emitter-to-Base Voltage	V_{EBO}	-12	V
Collector Current	I_C	-150	mA
Emitter Current	I_E	150	mA
Transistor Dissipation:			
T_A up to 25°C	P_T	250	mW
T_A above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Ambient)	T_A (opr)	71	°C
Storage	T_{STG}	-65 to 85	°C
Lead-Soldering Temperature (10 s max)	T_L	230	°C

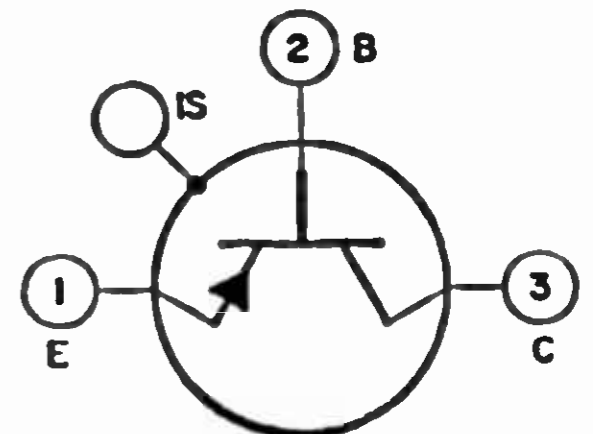
CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = -0.016$ mA, $I_E = 0$)	$V_{(BR)CBO}$	-30 min	V
Collector-to-Emitter Breakdown Voltage ($V_{EB} = -5$ V, $I_C = -0.016$)	$V_{(BR)CEX}$	25 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.012$ mA, $I_C = 0$)	$V_{(BR)EBO}$	-12 min	V
Collector-Cutoff Current ($V_{CB} = -30$ V, $I_E = 0$)	I_{CBO}	-16 max	μ A
Emitter-Cutoff Current ($V_{EB} = -12$ V, $I_C = 0$)	I_{EBO}	-12 max	μ A
Static Forward-Current Transfer Ratio ($V_{CE} = -1$ V, $I_C = -150$ mA)	h_{FE}	50 to 140	
Gain-Bandwidth Product ($V_{CE} = -12$ V, $I_C = -2$ mA)	f_T	1	MHz
Intrinsic Base-Spreading Resistance ($V_{CE} = -12$ V, $I_C = -2$ mA)	r_{bb}'	150 max	Ω
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	0.24 max	$^{\circ}$ C/W

2N274

TRANSISTOR

Ge p-n-p alloy drift-field type used in rf and if amplifier, oscillator, mixer, and converter circuits, and in low-level video-amplifier circuits in industrial and military equipment. JEDEC TO-44, Outline No.17.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-40	V
Collector-to-Emitter Voltage ($V_{BE} = 0.5$ V)	V_{CEV}	-40	V
Emitter-to-Base Voltage	V_{EBO}	-0.5	mA
Collector Current	I_C	-10	mA
Emitter Current	I_E	10	mA
Transistor Dissipation:			
T_A up to 25° C	P_T	120	mW
T_A above 25° C	P_T	See curve page 300	
$T_A = 25^{\circ}$ C (with heat sink)	P_T	240	mW
T_A above 25° C (with heat sink)	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 100	$^{\circ}$ C
Storage	T_{STG}	-65 to 100	$^{\circ}$ C

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = -50$ μ A, $I_E = 0$)	$V_{(BR)CBO}$	-40 min	V
Collector-to-Base Reach-Through Voltage ($V_{EB} = -0.5$ V)	V_{RT}	-40 min	V
Collector-Cutoff Current ($V_{CB} = -12$ V, $I_E = 0$)	I_{CBO}	-12 max	μ A
Emitter-Cutoff Current ($V_{EB} = -0.5$ V, $I_C = 0$)	I_{EBO}	-12 max	μ A
Small-Signal Forward-Current Transfer Ratio ($f = 1$ kHz, $V_{CE} = -12$ V, $I_E = 1.5$ mA)	h_{fe}	20 to 175	
Small-Signal Forward-Current Transfer-Ratio Cutoff Frequency ($V_{CB} = -12$ V, $I_E = 1.5$ mA)	f_{hfb}	30	MHz
Output Capacitance ($V_{CB} = -12$ V, $I_E = 0$)	C_{obo}	3 max	pF
Input Resistance:			
$V_{CE} = -12$ V, $I_E = 1.5$ mA, $f = 12.5$ MHz	R_{ie}	150	Ω
$V_{CE} = -12$ V, $I_E = 1.5$ mA, $f = 1.5$ MHz	R_{ie}	1350	Ω
Output Resistance:			
$V_{CE} = -12$ V, $I_E = 1.5$ mA, $f = 12.5$ MHz	R_{oe}	4000	Ω
$V_{CE} = -12$ V, $I_E = 1.5$ mA, $f = 1.5$ MHz	R_{oe}	70000	Ω
Power Gain:			
$V_{CE} = -12$ V, $I_E = 1.5$ mA, $f = 12.5$ MHz	G_{pe}	17 to 27	dB
$V_{CE} = -12$ V, $I_E = 1.5$ mA, $f = 1.5$ MHz	G_{pe}	40 to 50	dB
Thermal Resistance, Junction-to-Case	θ_{J-C}	0.31 max	$^{\circ}$ C/mW
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	0.62 max	$^{\circ}$ C/mW

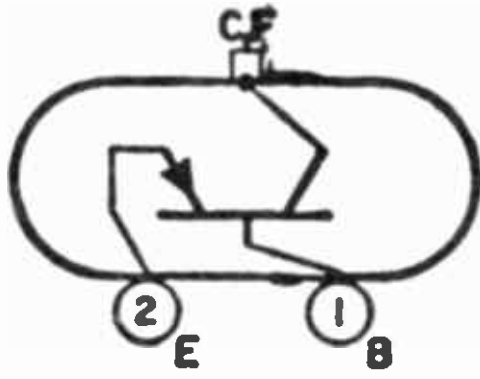
- 2N277** Refer to Chart of Discontinued Transistors
- 2N278** Refer to Chart of Discontinued Transistors
- 2N301** Refer to Chart of Discontinued Transistors
- 2N301A** Refer to Chart of Discontinued Transistors
- 2N307** Refer to Chart of Discontinued Transistors

Refer to Chart of Discontinued Transistors

2N331

POWER TRANSISTOR

2N351



Ge p-n-p alloy-junction type used in large-signal af amplifiers in class A power-output stages and class B push-pull amplifier stages in automobile radio receivers. JEDEC TO-3, Outline No.2. This type is identical with type 2N176 except for the following items:

CHARACTERISTICS

Static Forward-Current Transfer Ratio ($V_{CE} = -2 V$, $I_c = -0.7 A$)	h_{FE}	65	
Power Gain ($f = 0.001 MHz$)	G_{pe}	33.5	dB
Total Harmonic Distortion ($P_{oe} = 4 W$)	THD	5 max	%

Refer to Chart of Discontinued Transistors

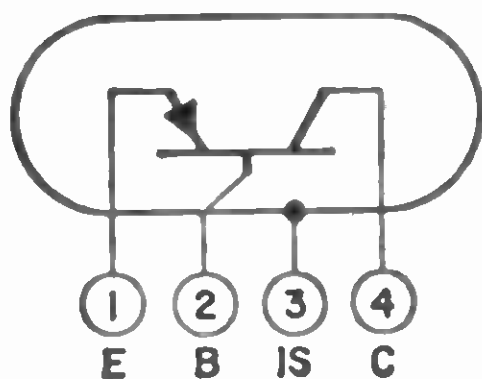
2N356

Refer to Chart of Discontinued Transistors

2N357

Refer to Chart of Discontinued Transistors

2N358



TRANSISTOR

2N370

Ge p-n-p alloy-junction drift-field type used in rf-amplifier service in AM broadcast-band portable radio receivers and short-wave receivers. JEDEC TO-7, Outline No.9.

MAXIMUM RATINGS

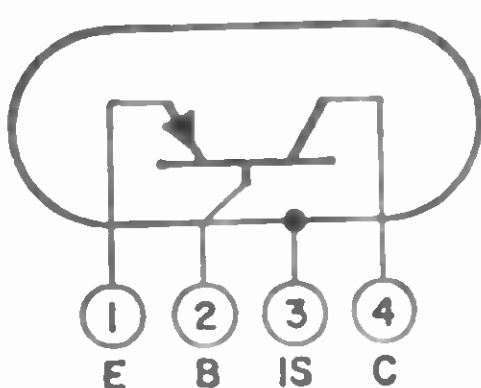
Collector-to-Base Voltage	V_{CBO}	-24	V
Emitter-to-Base Voltage	V_{EBO}	-0.5	V
Collector Current	I_C	-10	mA
Transistor Dissipation: $T_A = 25^\circ C$	P_T	80	mW
Temperature Range: Operating (Ambient)	$T_A (opr)$	-65 to 71	$^\circ C$

CHARACTERISTICS

Collector-Cutoff Current	I_{CBO}	-20 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = -12 V$, $I_c = -1 mA$)	h_{FE}	60 min	
Gain-Bandwidth Product	f_T	30	MHz
Output Capacitance*	C_{obo}	1.7	pF
Power Gain* ($f = 1.5 MHz$)	G_{pe}	31	dB

Refer to Chart of Discontinued Transistors

2N371



TRANSISTOR

2N372

Ge p-n-p alloy-junction drift-field type for use as an rf mixer in AM broadcast-band portable radio receivers and short-wave receivers. JEDEC TO-7, Outline No.9. This type is identical with type 2N370.

Refer to Chart of Discontinued Transistors

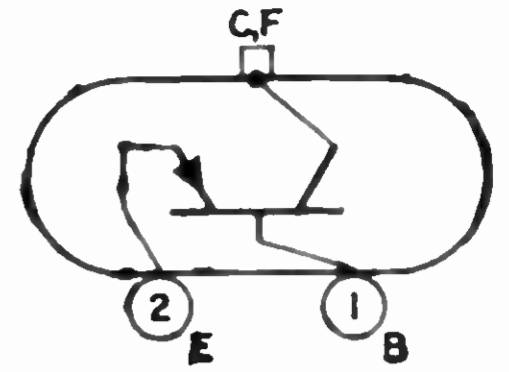
2N373

Refer to Chart of Discontinued Transistors

2N374

2N376 POWER TRANSISTOR

Ge p-n-p alloy-junction type used in large-signal af amplifiers in class A power-output stages and class B push-pull amplifier stages in automobile radio receivers. JEDEC TO-3, Outline No.2. This type is identical with type 2N176 except for the following items:

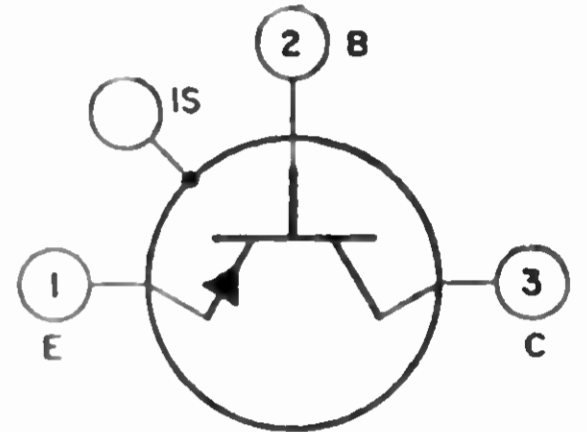


CHARACTERISTICS

Static Forward-Current Transfer Ratio ($V_{CE} = -2\text{ V}$, $I_C = -0.7\text{ A}$)	h_{FE}	78 min	
Power Gain ($f = 0.001\text{ MHz}$)	G_{pe}	35	dB
Total Harmonic Distortion ($P_{oe} = 4\text{ W}$)	THD	5 max	%

2N384 TRANSISTOR

Ge p-n-p alloy-junction drift-field type used in rf and if amplifier, oscillator, mixer, and converter circuits, and low-level video-amplifier circuits in industrial and military equipment. JEDEC TO-44, Outline No.17.



MAXIMUM RATINGS

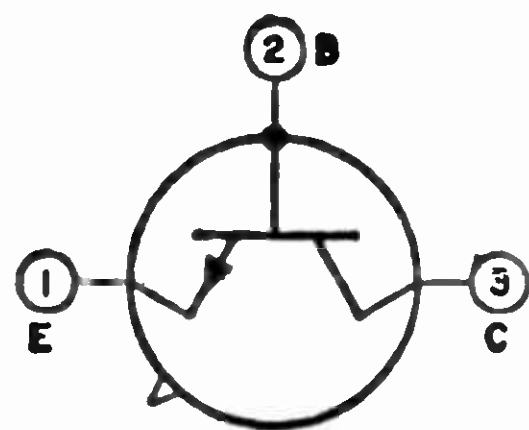
Collector-to-Base Voltage	V_{CBO}	-40	V
Collector-to-Emitter Voltage ($V_{BE} = 0.5\text{ V}$)	V_{CEV}	-40	V
Emitter-to-Base Voltage	V_{EBO}	-0.5	V
Collector Current	I_C	-10	mA
Emitter Current	I_E	10	mA
Transistor Dissipation:			
T_A up to 25°C	P_T	120	mW
T_A above 25°C	P_T	See curve page 300	
$T_C = 25^\circ\text{C}$ (with heat sink)	P_T	240	mW
T_C above 25°C (with heat sink)	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 100	$^\circ\text{C}$
Storage	T_{STG}	-65 to 100	$^\circ\text{C}$

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = -50\ \mu\text{A}$, $I_E = 0$)	$V_{(BR)CBO}$	-40 min	V
Collector-to-Base Reach-Through ($V_{EB} = -0.5\text{ V}$)	V_{RT}	-40 min	V
Collector-Cutoff Current ($V_{CB} = -12\text{ V}$, $I_E = 0$)	I_{CBO}	-12 max	μA
Emitter-Cutoff Current ($V_{EB} = -0.5\text{ V}$, $I_C = 0$)	I_{EBO}	-12 max	μA
Small-Signal Forward-Current Transfer Ratio ($V_{CB} = -12\text{ V}$, $I_E = 1.5\text{ mA}$, $f = 1\text{ kHz}$)	h_{re}	20 to 175	
Small-Signal Forward-Current Transfer Ratio Cutoff Frequency ($V_{CB} = -12\text{ V}$, $I_E = 1.5\text{ mA}$)	f_{hfb}	100	MHz
Input Resistance:			
$V_{CE} = -12\text{ V}$, $I_E = 1.5\text{ mA}$, $f = 50\text{ MHz}$	R_{ie}	30	Ω
$V_{CE} = -12\text{ V}$, $I_E = 1.5\text{ mA}$, $f = 12.5\text{ MHz}$	R_{ie}	250	Ω
Output Resistance:			
$V_{CE} = -12\text{ V}$, $I_E = 1.5\text{ mA}$, $f = 50\text{ MHz}$	R_{oe}	5000	Ω
$V_{CE} = -12\text{ V}$, $I_E = 1.5\text{ mA}$, $f = 12.5\text{ MHz}$	R_{oe}	16000	Ω
Output Capacitance ($V_{CB} = -12\text{ V}$, $I_E = 0$)	C_{obo}	3 max	pF
Power Gain:			
$V_{CB} = -12\text{ V}$, $I_E = 1.5\text{ mA}$, $f = 50\text{ MHz}$	G_{pe}	15 to 21	dB
$V_{CE} = -12\text{ V}$, $I_E = 1.5\text{ mA}$, $f = 12.5\text{ MHz}$	G_{pe}	24 to 32	dB
Thermal Resistance, Junction-to-Case	θ_{J-C}	0.31 max	$^\circ\text{C/mW}$
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	0.62 max	$^\circ\text{C/mW}$

TYPICAL OPERATION IN VIDEO-AMPLIFIER CIRCUIT

DC Collector-to-Emitter Voltage	V_{CE}	-12	V
DC Emitter Current	I_E	5.8	mA
Source Impedance	R_S	150	Ω
Capacitive Load		16	pF
Frequency Response		20 Hz to 10 MHz	
Pulse-Rise Time	t_r	0.035	μs
Voltage Gain		26	dB
Maximum Peak-to-Peak Output Voltage		20	V



COMPUTER TRANSISTORS

2N388 2N388A

Ge n-p-n alloy-junction types used in switching applications in data-processing equipment. JEDEC TO-5, Outline No.5.

MAXIMUM RATINGS

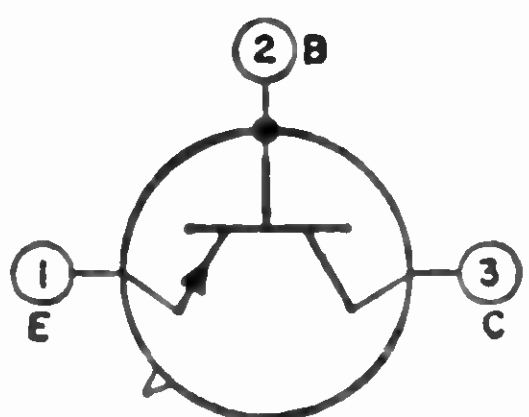
	2N388	2N388A		
Collector-to-Base Voltage	V_{CBO}	25	40	V
Collector-to-Emitter Voltage:				
$V_{BE} = -0.5$ V	V_{CEV}	—	40	V
$R_{BE} = 10000$ Ω	V_{CER}	20	20	V
Emitter-to-Base Voltage	V_{EBO}	15	15	V
Collector Current	I_C	200	200	mA
Transistor Dissipation:				
T_A up to 25°C	P_T	150	150	mW
T_A above 25°C	P_T	See curve page 300		
Temperature Range:				
Operating (Junction)	T_J (opr)	-65 to 100 °C		
Storage	T_{STG}	-65 to 100 °C		
Lead-Soldering Temperature (10 s max)	T_L	235	235	°C

CHARACTERISTICS

	2N388	2N388A		
Base-to-Emitter Voltage:				
$I_B = 10$ mA, $I_C = 200$ mA	V_{BE}	1.5	1.5 max	V
$I_B = 4$ mA, $I_C = 100$ mA	V_{BE}	0.8	0.8 max	V
Collector-Cutoff Current:				
$V_{CE} = 20$ V, $R_{BE} = 10000$ Ω	I_{CER}	50	50 max	μA
$V_{CE} = 40$ V, $V_{BE} = -0.5$ V	I_{CEV}	—	50 max	μA
$V_{CB} = 40$ V, $I_E = 0$	I_{CBO}	—	40 max	μA
$V_{CB} = 25$ V, $I_E = 0$	I_{CBO}	10	10 max	μA
$V_{CB} = 1$ V, $I_E = 0$	I_{CBO}	5	5 max	μA
Emitter-Cutoff Current:				
$V_{EB} = 15$ V, $I_C = 0$	I_{EBO}	10	10 max	μA
$V_{EB} = 1$ V, $I_C = 0$	I_{EBO}	5	5 max	μA
Static Forward-Current Transfer Ratio:				
$V_{CE} = 0.75$ V, $I_C = 200$ mA	h_{FE}	30	30 min	
$V_{CE} = 0.5$ V, $I_C = 30$ mA	h_{FE}	60 to 180		
Small-Signal Forward-Current Transfer-Ratio				
Cutoff Frequency ($V_{CB} = 6$ V, $I_C = 1$ mA) ..	f_{hfb}	5	5 min	MHz
Output Capacitance ($V_{CB} = 6$ V, $I_C = 1$ mA) ..	C_{obo}	20	20 max	pF
Turn-On Time ($V_{CC} = 20$ V, $I_{B1} = 10$ mA, $I_{B2} = -10$ mA, $I_C = 0.2$ A, $R_C = 100$ Ω)	$t_d + t_r$	1	1 max	μs
Storage Time ($V_{CC} = 20$ V, $I_{B1} = 10$ mA, $I_{B2} = -10$ mA, $I_C = 0.2$ A, $R_C = 100$ Ω)	t_s	0.7	0.7 max	μs
Fall Time ($V_{CC} = 20$ V, $I_{B1} = 10$ mA, $I_{B2} = -10$ mA, $I_C = 0.2$ A, $R_C = 100$ Ω)	t_f	0.7	0.7 max	μs

Refer to Chart of Discontinued Transistors

2N395



COMPUTER TRANSISTOR

2N396

Ge p-n-p alloy-junction type used in switching applications in data-processing equipment. JEDEC TO-5, Outline No.5.

MAXIMUM RATINGS

Collector-to-Emitter Voltage	V_{CER}	-20	V
$R_{BE} = 10000$ Ω			
Transistor Dissipation	P_T	See curve page 300	
T_A above 25°C			

CHARACTERISTICS

Collector-to-Emitter Saturation Voltage	$V_{CE}(\text{sat})$	-0.2	V
($I_B = -3.3$ mA, $I_C = -50$ mA)			
Collector-to-Emitter Reach-Through Voltage	V_{RT}	-20	V
Collector-Cutoff Current	I_{CBO}	-6	μA
($V_{CB} = -20$ V, $I_E = 0$, $T_A = 25^\circ C$)			

CHARACTERISTICS (cont'd)

Static Forward-Current Transfer Ratio:

$V_{CE} = -1 \text{ V}, I_C = -10 \text{ mA}, T_A = 25^\circ\text{C}$	h_{FE}	30 to 150	
$V_{CE} = -0.35 \text{ V}, I_C = -200 \text{ mA}, T_A = 25^\circ\text{C}$	h_{FE}	15	
Small-Signal Forward-Current Transfer Ratio			
Cutoff Frequency ($V_{CB} = -5 \text{ V}, I_E = 1 \text{ mA}$)	f_{hfb}	5	MHz

2N396A Refer to Chart of Discontinued Transistors

2N397 Refer to Chart of Discontinued Transistors

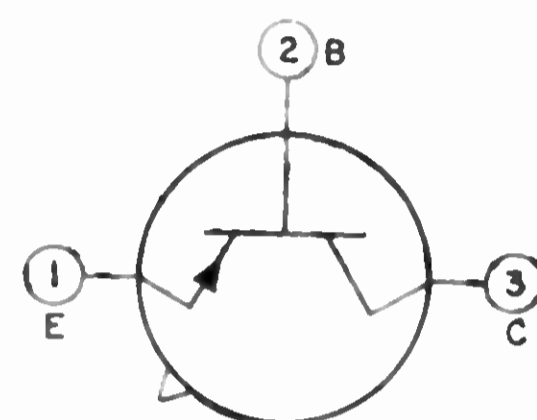
2N398

2N398A

TRANSISTORS

2N398B

Ge p-n-p alloy-junction types used for direct "on-off" control of high-voltage, low-power devices such as neon indicators, relays, incandescent-lamp indicators, indicator counters of electronic computers, and similar applications in critical industrial and military equipment. Designed to meet MIL specifications, including mechanical, environmental, and life tests. JEDEC TO-5, Outline No.5.

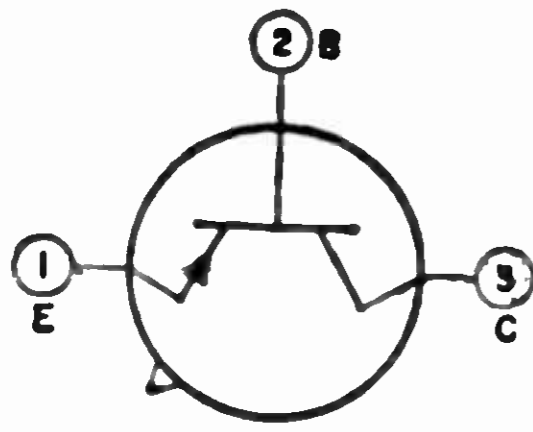


MAXIMUM RATINGS

		2N398	2N398A	2N398B	
Collector-to-Base Voltage	V_{CB0}	-105	-105	-105	V
Collector-to-Emitter ($R_{BE} = 0$)	V_{CES}	-105	-105	-105	V
Emitter-to-Base Voltage	V_{EBO}	-50	-50	-75	V
Collector Current	I_C	-100	-200	-200	mA
Emitter Current	I_E	100	200	200	mA
Transistor Dissipation:					
T_A up to 25°C	P_T	50	150	250	mW
T_A above 25°C	P_T		See curve page 300		
Temperature Range:					
Operating (Ambient)	T_A (opr)	-65 to 55	-65 to 100		$^\circ\text{C}$
Storage	T_{STG}	-65 to 85	-65 to 100		$^\circ\text{C}$
Lead-Soldering Temperature:					
10 seconds max	T_L	230	—	250	$^\circ\text{C}$
3 seconds max	T_L	—	250	—	$^\circ\text{C}$

CHARACTERISTICS

Collector-to-Base Breakdown Voltage:					
$I_C = -0.025 \text{ mA}, I_E = 0$	$V_{(BR)CBO}$	—	—	-105 min	V
$I_C = -0.05 \text{ mA}, I_E = 0$	$V_{(BR)CBO}$	-105	-105	— min	V
Emitter-to-Base Breakdown Voltage					
($I_E = -0.05 \text{ mA}, I_C = 0$)	$V_{(BR)EBO}$	-50	-50	-75 min	V
Collector-to-Emitter Reach-Through					
Voltage	V_{RT}	-105	-105	-105 min	V
Base-to-Emitter Saturation Voltage					
($I_C = -5 \text{ mA}, I_B = -0.25 \text{ mA}$)	$V_{BE(sat)}$	-0.4	-0.4	-0.3 max	V
Collector-to-Emitter Saturation Voltage					
($I_C = -5 \text{ mA}, I_B = -0.25 \text{ mA}$)	$V_{CE(sat)}$	-0.35	-0.35	-0.25 max	V
Collector-Cutoff Current:					
$V_{CE} = -105 \text{ V}, R_{BE} = 0, T_A = 25^\circ\text{C}$	I_{CES}	-600	-600	-300 max	μA
$V_{CE} = -55 \text{ V}, R_{BE} = 10 \text{ k}\Omega, T_A = 25^\circ\text{C}$	I_{CER}	—	—	-300 max	μA
$V_{CB} = -2.5 \text{ V}, I_E = 0, T_A = 25^\circ\text{C}$	I_{CBO}	-14	-14	-6 max	μA
$V_{CB} = -105 \text{ V}, I_E = 0, T_A = 25^\circ\text{C}$	I_{CBO}	-50	-50	-25 max	μA
$V_{CB} = -105 \text{ V}, I_E = 0, T_A = 71^\circ\text{C}$	I_{CBO}	—	—	-300 max	μA
Emitter-Cutoff Current:					
$V_{EB} = -2.5 \text{ V}, I_C = 0$	I_{EBO}	—	—	-6 max	μA
$V_{EB} = -50 \text{ V}, I_C = 0$	I_{EBO}	-50	-50	— max	μA
$V_{EB} = -75 \text{ V}, I_C = 0$	I_{EBO}	—	—	-50 max	μA
Static Forward-Current Transfer Ratio:					
$V_{CE} = -0.25 \text{ V}, I_C = -5 \text{ mA}$	h_{FE}	—	—	20 min	
$V_{CE} = -0.35 \text{ V}, I_C = -5 \text{ mA}$	h_{FE}	20	20	— min	
Small-Signal Forward-Current Transfer					
Ratio ($V_{CE} = -6 \text{ V}, I_C = -1 \text{ mA},$ $f = 1 \text{ kHz}$)	h_{fe}	—	20	40 min	
Small-Signal Forward-Current Transfer-					
Ratio Cutoff Frequency ($V_{CB} = -6 \text{ V},$ $I_E = 1 \text{ mA}$)	f_{hfb}	—	—	1 max	MHz
Thermal Resistance, Junction-to-					
Ambient	θ_{J-A}	—	0.5	0.3 max	$^\circ\text{C/W}$



COMPUTER TRANSISTORS

2N404
2N404A

Ge p-n-p alloy-junction types used in switching applications in data-processing equipment. JEDEC TO-5, Outline No.5.

MAXIMUM RATINGS

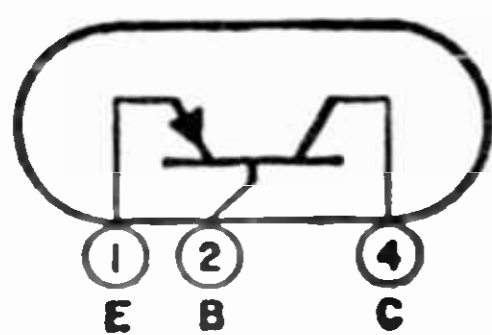
		2N404	2N404A	
Collector-to-Base Voltage	V _{CB0}	-25	-40	V
Collector-to-Emitter Voltage (V _{BE} = 1 V)	V _{CEV}	-24	-35	V
Emitter-to-Base Voltage	V _{EBO}	-12	-25	V
Collector Current	I _C	-100	-150	mA
Emitter Current	I _E	100	150	mA
Transistor Dissipation:				
T _A up to 25°C	P _T	150	150	mW
T _A above 25°C	P _T	See curve page 300		
Temperature Range:				
Operating (Ambient)	T _A (opr)	-65 to 85	-65 to 100	°C
Storage	T _{STG}	-65 to 100	-65 to 100	°C
Lead-Soldering Temperature (10 s max)	T _L	255	255	°C

CHARACTERISTICS

Collector-to-Base Breakdown Voltage (I _C = -0.02 mA, I _E = 0)	V _{(BR)CBO}	-25	-40 min	V
Emitter-to-Base Breakdown Voltage (I _E = -0.02 mA, I _C = 0)	V _{(BR)EBO}	-12	-25 min	V
Base-to-Emitter Saturation Voltage:				
I _C = -12 mA, I _B = -0.4 mA	V _{BE} (sat)	-0.35	-0.35 max	V
I _C = -24 mA, I _B = -1 mA	V _{BE} (sat)	-0.4	-0.4 max	V
Collector-to-Emitter Saturation Voltage:				
I _C = -12 mA, I _B = -0.4 mA	V _{CE} (sat)	-0.15	-0.15 max	V
I _C = -24 mA, I _B = -1 mA	V _{CE} (sat)	-0.2	-0.2 max	V
Collector-Cutoff Current:				
V _{CB} = -12 V, I _E = 0, T _A = 25°C	I _{CBO}	-5	-5 max	μA
V _{CB} = -12 V, I _E = 0, T _A = 80°C	I _{CBO}	-90*	-90 max	μA
Static Forward-Current Transfer Ratio:				
V _{CE} = -0.2 V, I _C = -24 mA	h _{FE}	24	24 min	
V _{CE} = -0.15 V, I _C = -12 mA	h _{FE}	30	30 min	
Small-Signal Forward-Current Transfer-Ratio Cutoff Frequency (V _{CB} = -6 V, I _C = -1 mA)	f _{hfb}	4	4 min	MHz
Output Capacitance:				
V _{CB} = -6 V, I _C = 0	C _{ob0}	20	- max	pF
V _{CB} = -6 V, I _E = 1 mA, f = 2 MHz	C _{ob0}	-	20 max	pF
Stored Base Charge (I _C = -10 mA, I _B = -1 mA)	Q _s	1400	1400 max	pC

• For higher dissipation values in switching applications, see RCA Application Note AN-181.

* This value does not apply to type 2N581.



TRANSISTOR

2N405

Ge p-n-p alloy-junction type used in low-power class A af-amplifier applications in battery-operated portable radio-receivers. JEDEC TO-40, Outline No.16.

MAXIMUM RATINGS

Collector-to-Base Voltage	V _{CB0}	-20	V
Collector Current	I _C	-35	mA
Emitter Current	I _E	35	mA
Transistor Dissipation:			
T _A = 25°C	P _T	150	mW
Temperature Range:			
Operating (Ambient)	T _A (opr)	-65 to 71	°C

CHARACTERISTICS

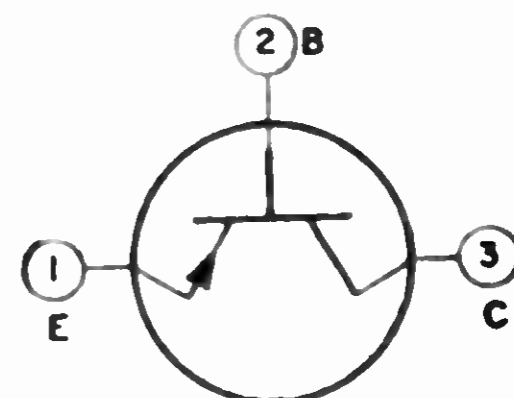
Collector-Cutoff Current	I _{CBO}	-14 max	μA
Static Forward-Current Transfer Ratio (V _{CE} = -6 V, I _E = 1 mA)	h _{FE}	35 min	
Small-Signal Forward-Current Transfer-Ratio Cutoff Frequency (V _{CB} = -6 V, I _C = -1 mA)	f _{hfb}	650	kHz

CHARACTERISTICS (cont'd)

Output Capacitance	C_{obo}	40	pF
Power Gain	G_{pe}	43	dB

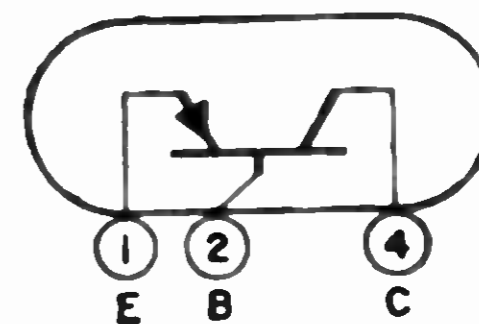
2N406 TRANSISTOR

Ge p-n-p alloy-junction type used in low-power class A af-amplifier applications in battery-operated portable radio receivers. JEDEC TO-1, Outline No.1. This type is electrically identical with type 2N405.



2N407 TRANSISTOR

Ge p-n-p alloy-junction type used in class A amplifiers and class B push-pull output stages of battery-operated radio receivers and af amplifiers. JEDEC TO-40, Outline No.16.



MAXIMUM RATINGS

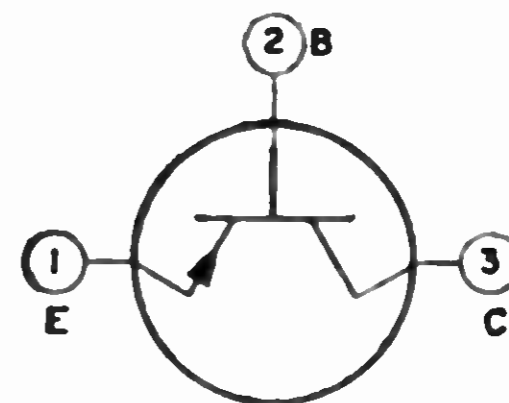
Collector-to-Base Voltage	V_{CBO}	-20	V
Collector Current	I_C	-70	mA
Emitter Current	I_E	70	mA
Transistor Dissipation: $T_A = 25^\circ C$	P_T	150	mW
Temperature Range: Operating (Ambient)	$T_A (opr)$	-65 to 71	$^\circ C$

CHARACTERISTICS

Collector-Cutoff Current ($V_{CB} = -12 V, I_E = 0$)	I_{CBO}	-14 max	μA
Emitter-Cutoff Current ($V_{EB} = -2.5 V, I_C = 0$)	I_{EBO}	-14 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = -1 V,$ $I_C = -50 mA$)	h_{FE}	65	
Power Gain ($f = 0.001 MHz$)	G_{pe}	33	dB
Total Harmonic Distortion ($P_{oe} = 0.16 W$)	THD	10 max	%

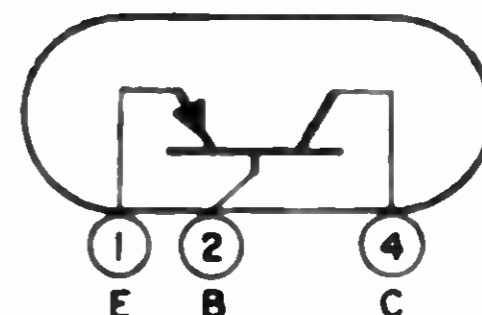
2N408 TRANSISTOR

Ge p-n-p alloy-junction type used in class A amplifiers and class B push-pull output stages of battery-operated radio receivers and af amplifiers. JEDEC TO-1, Outline No.1. This type is electrically identical with type 2N407.



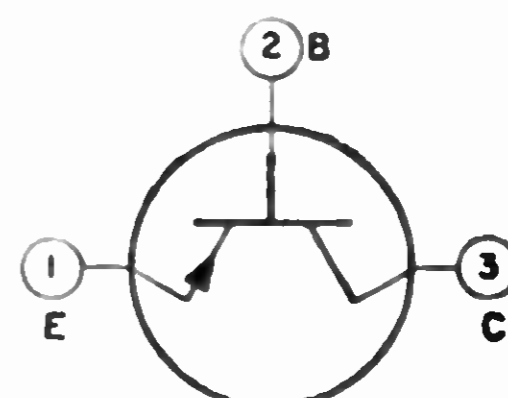
2N409 TRANSISTOR

Ge p-n-p alloy-junction type used in 455-kHz if-amplifier service in battery-operated portable radio receivers and automobile radio receivers. JEDEC TO-40, Outline No.16. This type is electrically identical with type 2N410.



2N410 TRANSISTOR

Ge p-n-p alloy-junction type used in 455-kHz if-amplifier service in battery-operated portable radio receivers and automobile radio receivers. JEDEC TO-1, Outline No.1.



MAXIMUM RATINGS

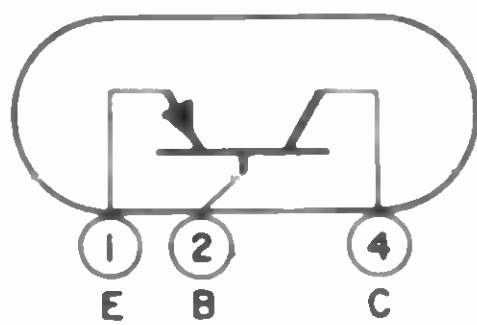
Collector-to-Base Voltage	V_{CB0}	-13	V
Collector Current	I_C	-15	mA
Transistor Dissipation:			
$T_A = 25^\circ\text{C}$	P_T	80	mW
Temperature Range:			
Operating (Ambient)	$T_A(\text{opr})$	-65 to 71	$^\circ\text{C}$

CHARACTERISTICS

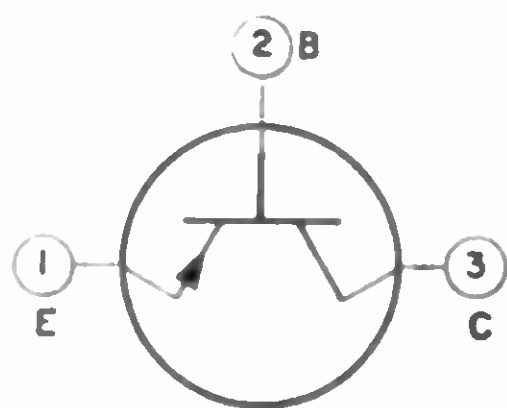
Collector-to-Base Breakdown Voltage ($I_C = -10 \mu\text{A}$, $I_E = 0$)	$V_{(BR)CB0}$	-13 min	V
Collector-Cutoff Current ($V_{CB} = -13 \text{ V}$, $I_E = 0$)	I_{CBO}	-10 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = -9 \text{ V}$, $I_C = -1 \text{ mA}$)	h_{FE}	48	
Small-Signal Forward-Current Transfer-Ratio Cutoff Frequency	f_{hfb}	6.7	MHz
Output Capacitance	C_{obo}	9.5	pF
Power Gain ($f = 0.455 \text{ MHz}$)	G_{pe}	38.8	dB

TRANSISTOR

2N411



Ge p-n-p alloy-junction type intended for converter and mixer-oscillator applications in battery-operated portable radio receivers. JEDEC TO-40, Outline No.16. This type is electrically identical with type 2N412.



TRANSISTOR

2N412

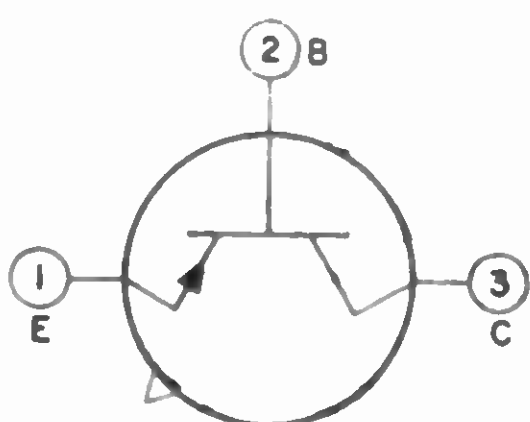
Ge p-n-p alloy-junction type used in converter and mixer-oscillator applications in battery-operated portable radio receivers. JEDEC TO-1, Outline No.1.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CB0}	-13	V
Collector Current	I_C	-15	mA
Transistor Dissipation:			
$T_A = 25^\circ\text{C}$	P_T	80	mW
Temperature Range:			
Operating (Ambient)	$T_A(\text{opr})$	-65 to 71	$^\circ\text{C}$

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = -10 \mu\text{A}$, $I_E = 0$)	$V_{(BR)CB0}$	-13 min	V
Collector-Cutoff Current ($V_{CB} = -13 \text{ V}$, $I_E = 0$)	I_{CBO}	-10 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = -9 \text{ V}$, $I_C = -0.6 \text{ mA}$)	h_{FE}	75	
Small-Signal Forward-Current Transfer-Ratio Cutoff Frequency ($V_{CB} = -9 \text{ V}$, $I_E = 0.6 \text{ mA}$)	f_{hfb}	10	MHz
Oscillator Injection Voltage ($f = 1 \text{ MHz}$)		100	mV
Output Capacitance	C_{obo}	9.5	pF
Power Gain ($f = 1 \text{ MHz}$)	G_{pe}	32	dB



COMPUTER TRANSISTOR

2N414

Ge p-n-p alloy-junction type used in switching applications in data-processing equipment. JEDEC TO-5, Outline No.5.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CB0}	-30	V
Collector-to-Emitter Voltage:			
$V_{BE} = 1 \text{ V}$	V_{CEV}	-20	V
Base open	V_{CEO}	-15	V

MAXIMUM RATINGS (cont'd)

Emitter-to-Base Voltage	V_{EBO}	-20	mA
Peak Collector Current	i_c	-400	mA
Collector Current	I_c	-200	mA
Transistor Dissipation:			
T_A up to 25°C	P_T	150	mW
T_A above 25°C	P_T	See curve page	300
$T_A = 55^\circ C$	P_T	75	mW
Ambient-Temperature Range:			
Operating (T_A) and Storage (T_{STG})		-65 to 85	°C
Lead-Soldering Temperature (10 s max)	T_L	240	°C

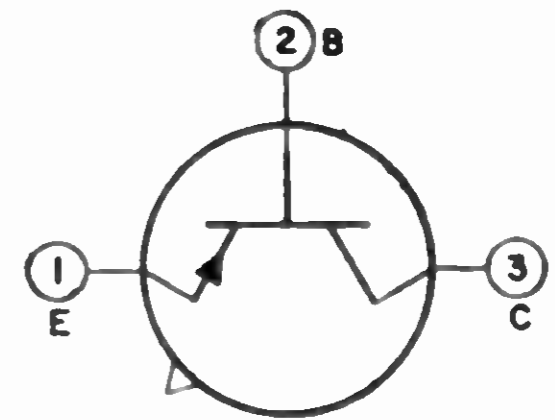
CHARACTERISTICS

Collector-Cutoff Current ($V_{CB} = -12$ V, $I_E = 0$)	I_{CBO}	-5 max	μA
Emitter-Cutoff Current ($V_{EB} = -12$ V, $I_c = 0$)	I_{EBO}	-5 max	μA
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = -6$ V, $I_E = 1$ mA, $f = 1$ kHz)	h_{fe}	80	
Small-Signal Forward-Current Transfer-Ratio Cutoff Frequency ($V_{CB} = -6$ V, $I_E = 1$ mA)	f_{hfb}	8	MHz
Output Capacitance ($V_{CB} = -6$ V, $I_c = -1$ mA)	C_{obo}	11	pF
Small-Signal Short-Circuit Input Impedance ($V_{CB} = -6$ V, $I_E = 1$ mA, $f = 1$ kHz)	h_{ib}	30	Ω
Small-Signal Open-Circuit Reverse-Voltage Transfer Ratio ($V_{CB} = -6$ V, $I_E = 0$, $f = 1$ kHz)	h_{rb}	0.5×10^{-4}	
Noise Figure ($V_{CE} = -6$ V, $I_E = 1$ mA, $f = 1.5$ MHz)	NF	6	dB
Power Gain ($V_{CE} = -6$ V, $I_E = 1$ mA, $f = 1.5$ MHz)	$G_{p\phi}$	16	dB

- 2N441** Refer to Chart of Discontinued Transistors
- 2N442** Refer to Chart of Discontinued Transistors
- 2N443** Refer to Chart of Discontinued Transistors
- 2N456** Refer to Chart of Discontinued Transistors
- 2N457** Refer to Chart of Discontinued Transistors
- 2N497** Refer to Chart of Discontinued Transistors
- 2N544** Refer to Chart of Discontinued Transistors
- 2N561** Refer to Chart of Discontinued Transistors
- 2N578** Refer to Chart of Discontinued Transistors
- 2N579** Refer to Chart of Discontinued Transistors
- 2N580** Refer to Chart of Discontinued Transistors

2N581 COMPUTER TRANSISTOR

Ge p-n-p alloy-junction type used in switching applications in data-processing equipment. JEDEC TO-5, Outline No.5. This type is identical with type 2N404 except for the following items:



MAXIMUM RATINGS

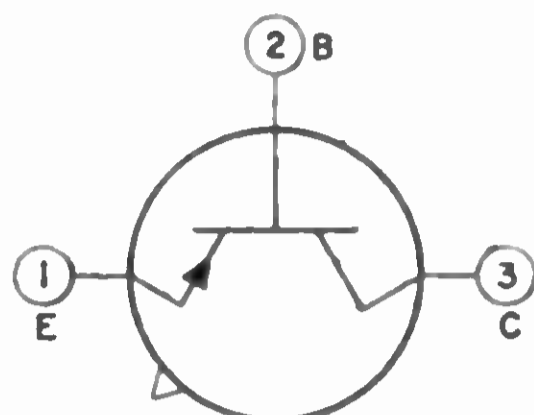
Collector-to-Base Voltage	V_{CBO}	-18	V
Collector-to-Emitter Voltage ($V_{BE} = 1$ V)	V_{CEV}	-15	V
Emitter-to-Base Voltage	V_{EBO}	-10	V

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_c = -0.02$ mA, $I_E = 0$)	$V_{(BR)CBO}$	-18 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -0.02$ mA, $I_c = 0$)	$V_{(BR)EBO}$	-10 min	V
Base-to-Emitter Saturation Voltage ($I_c = -20$ mA, $I_B = -1$ mA)	$V_{BE(sat)}$	-0.5 max	V

CHARACTERISTICS (cont'd)

Collector-to-Emitter Saturation Voltage ($I_c = -20$ mA, $I_B = -1$ mA)	$V_{CE(sat)}$	-0.2 min	V
Collector-Cutoff Current ($V_{CB} = -12$ V, $I_E = 0$, $T_A = 25^\circ\text{C}$)	I_{CBO}	-10 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = -0.3$ V, $I_c = -20$ mA)	h_{FE}	20 min	
Stored Base Charge ($I_c = -20$ mA, $I_B = -2$ mA)	Q_s	2400 max	pC



COMPUTER TRANSISTOR 2N582

Ge p-n-p alloy-junction type used in switching applications in data-processing equipment. JEDEC TO-5, Outline No.5. This type is identical with type 2N404 except for the following items:

MAXIMUM RATINGS

Collector-to-Emitter Voltage ($V_{BE} = 1$ V)	V_{CEV}	-14	V
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CHARACTERISTICS

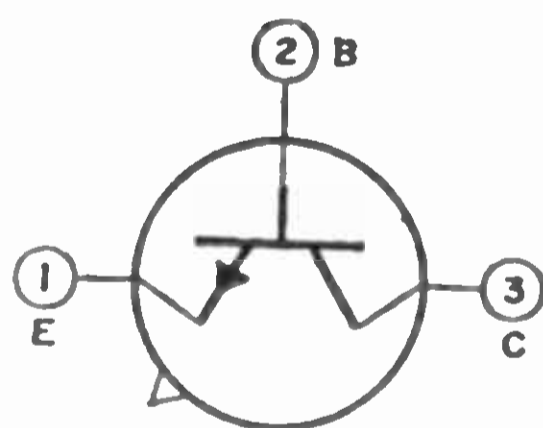
Collector-to-Emitter Saturation Voltage: $I_c = -24$ mA, $I_B = -0.6$ mA	$V_{CE(sat)}$	-0.2 max	V
$I_c = -100$ mA, $I_B = -5$ mA	$V_{CE(sat)}$	-0.3 max	V
Base-to-Emitter Saturation Voltage: $I_c = -24$ mA, $I_B = -0.6$ mA	$V_{BE(sat)}$	-0.4 max	V
$I_c = -100$ mA, $I_B = -5$ mA	$V_{BE(sat)}$	-0.8 max	V
Static Forward-Current Transfer Ratio: $V_{CE} = -0.2$ V, $I_c = -24$ mA	h_{FE}	40 min	
$V_{CE} = -0.3$ V, $I_c = -100$ mA	h_{FE}	20 min	
Small-Signal Forward-Current Transfer Ratio Cutoff Frequency ($V_{CB} = -6$ V, $I_c = -1$ mA)	f_{hfb}	14 min	MHz
Stored Base Charge ($I_c = -24$ mA, $I_B = -1.2$ mA)	Q_s	1200 max	pC

Refer to Chart of Discontinued Transistors

2N583

Refer to Chart of Discontinued Transistors

2N584



COMPUTER TRANSISTOR 2N585

Ge n-p-n alloy-junction type used in switching applications in data-processing equipment. JEDEC TO-5, Outline No.5.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	25	V
Collector-to-Emitter Voltage: $V_{BE} = -1$ V	V_{CEV}	24	V
Base open	V_{CEO}	15	V
Emitter-to-Base Voltage	V_{EBO}	20	V
Collector Current	I_C	200	mA
Emitter Current	I_E	-200	mA
Transistor Dissipation: T_A up to 25°C	P_T	120	mW
T_A above 25°C	P_T	See curve page 300	
Temperature Range: Operating (Ambient)	T_A (opr)	71	$^\circ\text{C}$
Storage	T_{STG}	-65 to 85	$^\circ\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	255	$^\circ\text{C}$

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_c = 25$ μA , $I_E = 0$)	$V_{(BR)CBO}$	25 min	V
Collector-to-Emitter Breakdown Voltage ($I_c = 600$ μA , $I_B = 0$)	$V_{(BR)CEO}$	15 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -25$ μA , $I_c = 0$)	$V_{(BR)EBO}$	20 min	V
Collector-to-Emitter Saturation Voltage ($I_c = 20$ mA, $I_B = 1$ mA)	$V_{CE(sat)}$	0.2 max	V

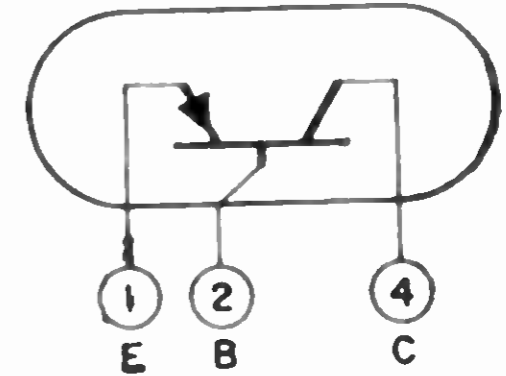
CHARACTERISTICS (cont'd)

Base-to-Emitter Saturation Voltage ($I_C = 20 \text{ mA}$, $I_B = 1 \text{ mA}$)	$V_{BE}(\text{sat})$	0.45 max	V
Collector-Cutoff Current: $V_{CB} = 0.25 \text{ V}$, $I_E = 0$	I_{CBO}	6 max	μA
$V_{CB} = 12 \text{ V}$, $I_E = 0$	I_{CBO}	8 max	μA
Emitter-Cutoff Current ($V_{BE} = 5 \text{ V}$, $I_C = 0$)	I_{EBO}	5 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 0.2 \text{ V}$, $I_C = 20 \text{ mA}$)	h_{FE}	20 min	
Small-Signal Forward-Current Transfer Ratio Cutoff Frequency ($V_{CB} = 6 \text{ V}$, $I_E = -1 \text{ mA}$)	f_{hfb}	3 min	MHz
Output Capacitance ($V_{CB} = 6 \text{ V}$, $I_E = 0$)	C_{obo}	25 max	pF
Stored Base Charge ($I_C = 20 \text{ mA}$, $I_B = 2 \text{ mA}$)	Q_s	3000 max	pC

2N586

TRANSISTOR

Ge p-n-p alloy-junction type used in low-speed switching applications in industrial and military equipment. It can also be used in large-signal class A and class B push-pull af amplifiers. Similar to JEDEC TO-7 (3-lead type), Outline No.9.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-45	V
Emitter-to-Base Voltage	V_{EBO}	-12	V
Collector Current	I_C	-250	mA
Emitter Current	I_E	250	mA
Transistor Dissipation: T_A up to 25°C	P_T	250	mW
$T_A = 55^\circ\text{C}$	P_T	125	mW
$T_A = 71^\circ\text{C}$	P_T	60	mW
Ambient-Temperature Range: Operating (T_A) and Storage (T_{STG})	T_L	-65 to 85	$^\circ\text{C}$
Lead-Soldering Temperature (10 s max)		255	$^\circ\text{C}$

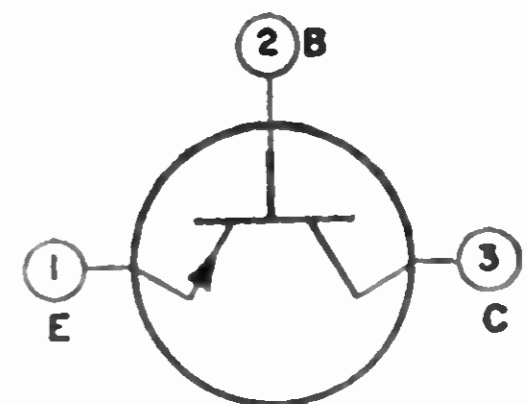
CHARACTERISTICS

Collector-to-Emitter Breakdown Voltage: $I_C = -50 \mu\text{A}$, $V_{BE} = 0$	$V_{(BR)CES}$	-45 min	V
$I_C = -1 \text{ mA}$, $I_B = 0$	$V_{(BR)CEO}$	-25 min	V
Collector-to-Emitter Reach-Through Voltage ($V_{BE} = -1 \text{ V}$, $I_E = 0$)	V_{RT}	-45 min	V
Collector-to-Emitter Saturation Voltage ($I_C = -250 \text{ mA}$, $I_B = -25 \text{ mA}$)	$V_{CE}(\text{sat})$	-0.5 max	V
Base-to-Emitter Voltage ($I_C = -250 \text{ mA}$, $I_B = -7 \text{ mA}$)	V_{BE}	-1 max	V
Collector-Cutoff Current ($V_{CB} = -45 \text{ V}$, $I_E = 0$)	I_{CBO}	-16 max	μA
Emitter-Cutoff Current ($V_{BE} = -12 \text{ V}$, $I_C = 0$)	I_{EBO}	-12 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = -0.5 \text{ V}$, $I_C = -250 \text{ mA}$)	h_{FE}	35 min	

2N591

TRANSISTOR

Ge p-n-p alloy-junction type used in large-signal af driver applications in class A stages of automobile radio receivers. JEDEC TO-1, Outline No.1.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-32	V
Collector-to-Emitter Voltage	V_{CEO}	-32	V
Collector Current	I_C	-40	mA
Transistor Dissipation: T_A up to 55°C	P_T	85	mW
T_C up to 55°C	P_T	200	mW
T_A or T_C above 55°C	P_T	See curve page 300	
Temperature Range: Operating (Ambient)	$T_A(\text{opr})$	71	$^\circ\text{C}$
Storage	T_{STG}	-65 to 85	$^\circ\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	255	$^\circ\text{C}$

CHARACTERISTICS

Collector-Cutoff Current ($V_{CB} = -10 \text{ V}$, $I_E = 0$)	I_{CBO}	-7 max	μA
Emitter-Cutoff Current ($V_{EB} = -1 \text{ V}$, $I_C = 0$)	I_{EBO}	-20 max	μA

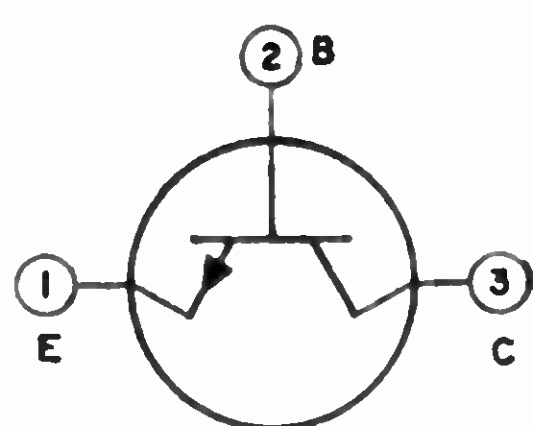
CHARACTERISTICS (cont'd)

Collector-to-Base Breakdown Voltage ($I_C = -0.05 \text{ mA}$, $I_E = 0$)	$V_{(BR)CBO}$	-32 min	V
Collector-to-Emitter Breakdown Voltage ($I_C = -0.3 \text{ mA}$, $I_B = 0$)	$V_{(BR)CEX}$	-32 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.05 \text{ mA}$, $I_C = 0$)	$V_{(BR)EBO}$	-12 min	V
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = -12 \text{ V}$, $I_C = -2 \text{ V}$, $f = 1 \text{ kHz}$)	h_{fe}	40 to 120	
Thermal Resistance:			
Junction-to-Ambient	θ_{J-A}	353 max	$^{\circ}\text{C/W}$
Junction-to-Case	θ_{J-C}	150 max	$^{\circ}\text{C/W}$

- Refer to Chart of Discontinued Transistors **2N640**
- Refer to Chart of Discontinued Transistors **2N641**
- Refer to Chart of Discontinued Transistors **2N642**
- Refer to Chart of Discontinued Transistors **2N643**
- Refer to Chart of Discontinued Transistors **2N644**
- Refer to Chart of Discontinued Transistors **2N645**

TRANSISTOR

2N647



Ge n-p-n alloy-junction type used in large-signal af-amplifier applications in battery-operated portable radio receivers and phonographs. N-P-N construction permits complementary push-pull operation with a matching p-n-p type, such as the 2N217. JEDEC TO-1, Outline No.1.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	25	V
Collector-to-Emitter Voltage	V_{CEO}	25	V
Emitter-to-Base Voltage	V_{EBO}	12	V
Collector Current	I_C	100	mA
Emitter Current	I_E	-100	mA
Transistor Dissipation:			
T_A up to 25°C	P_T	100	mW
T_A above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Ambient)	$T_A(\text{opr})$	-65 to 71	$^{\circ}\text{C}$
Storage	T_{STG}	-65 to 85	$^{\circ}\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	255	$^{\circ}\text{C}$

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = 0.05 \text{ mA}$, $I_E = 0$)	$V_{(BR)CBO}$	25 min	V
Collector-to-Emitter Breakdown Voltage ($V_{EB} = 5 \text{ V}$, $I_C = 0.014 \text{ mA}$)	$V_{(BR)CEV}$	25 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.014 \text{ mA}$, $I_C = 0$)	$V_{(BR)EBO}$	12 min	V
Collector-Cutoff Current ($V_{CB} = 25 \text{ V}$, $I_E = 0$)	I_{CBO}	14 max	μA
Emitter-Cutoff Current ($V_{EB} = 12 \text{ V}$, $I_C = 0$)	I_{EBO}	14 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 1 \text{ V}$, $I_C = 50 \text{ mA}$)	h_{FE}	50 to 150	
Gain Bandwidth Product ($V_{CE} = 6 \text{ V}$, $I_C = 2 \text{ mA}$) ...	f_T	2	MHz
Intrinsic Base-Spreading Resistance ($V_{CE} = 6 \text{ V}$, $I_C = 2 \text{ mA}$)	$r_{bb'}$	350 max	Ω

TYPICAL OPERATION IN CLASS B COMPLEMENTARY-SYMMETRY CIRCUIT

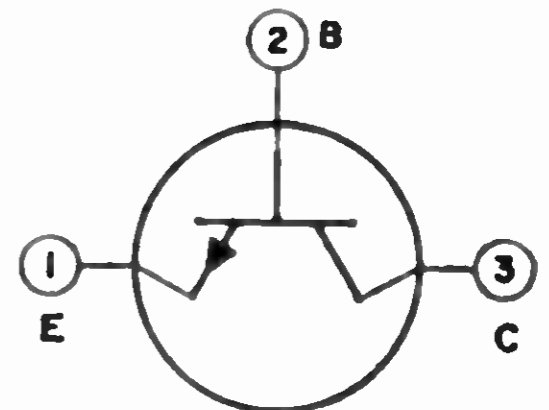
DC Collector-Supply Voltage	V_{CC}	6	V
DC Collector-to-Emitter Voltage for driver stage	V_{CE}	2.3	V
Zero-Signal DC Base-to-Emitter Voltage for output stage	V_{BE}	0.14	V
Peak Collector Current for each transistor in output stage	$i_C(\text{peak})$	70	mA
Zero-Signal DC Collector Current for each transistor (driver and output stage)	I_C	1.5	mA

TYPICAL OPERATION (cont'd)

Signal Frequency		1	kHz
Input Resistance	R_s	1100	Ω
Load Resistance	R_L	45	Ω
Power Gain		54	dB
Total Harmonic Distortion		10	%
Power Output (input = 20 mV)	P_{OEB}	100	mW

2N649 TRANSISTOR

Ge n-p-n alloy-junction type used in large-signal af-amplifier applications in battery-operated portable radio receivers and phonographs. N-P-N construction permits complementary push-pull operation with a matching p-n-p type, such as the 2N408. JEDEC TO-1, Outline No.1.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	20	V
Collector-to-Emitter Voltage	V_{CEO}	18	V
Emitter-to-Base Voltage	V_{EBO}	2.5	V
Collector Current	I_C	100	mA
Emitter Current	I_E	-100	mA
Transistor Dissipation:			
T_A up to 25°C	P_T	100	mW
T_A above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Ambient)	T_A (opr)	-65 to 71	°C
Storage	T_{STG}	-65 to 85	°C
Lead-Soldering Temperature (10 s max)	T_L	255	°C

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = 0.05$ mA, $I_E = 0$)	$V_{(BR)CBO}$	20 min	V
Collector-to-Emitter Breakdown Voltage ($V_{EB} = 2$ V, $I_C = 0.05$ mA)	$V_{(BR)CEV}$	18 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.014$ mA, $I_C = 0$)	$V_{(BR)EBO}$	2.5 min	V
Collector-Cutoff Current ($V_{CB} = 12$ V, $I_E = 0$)	I_{CBO}	14 max	μ A
Emitter-Cutoff Current ($V_{EB} = 2.5$ V, $I_C = 0$)	I_{EBO}	14 max	μ A
Static Forward-Current Transfer Ratio ($V_{CE} = 1$ V, $I_C = 50$ mA)	h_{FE}	50 to 150	
Gain-Bandwidth Product ($V_{CE} = 6$ V, $I_C = 2$ mA) ...	f_T	2	MHz
Intrinsic Base-Spreading Resistance ($V_{CE} = 6$ V, $I_C = 2$ mA)	$r_{bb'}$	350 max	Ω

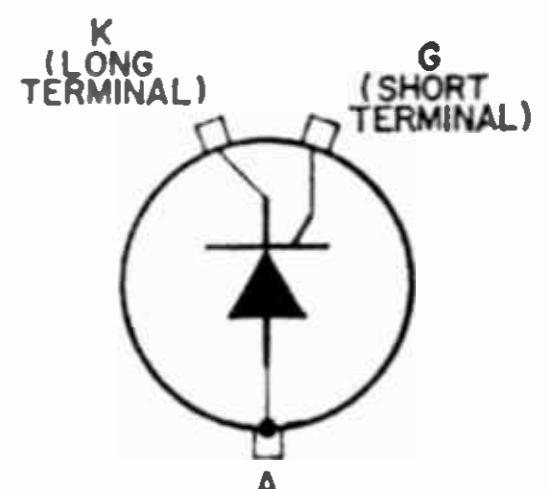
TYPICAL OPERATION IN CLASS B COMPLEMENTARY-SYMMETRY CIRCUIT

DC Collector Supply Voltage	V_{CC}	6	V
DC Collector-to-Emitter Voltage for driver stage	V_{CE}	2.3	V
Zero-Signal DC Base-to-Emitter Voltage for output stage	V_{BE}	0.14	V
Peak Collector Current for each transistor in output stage	i_C (peak)	70	mA
Zero-Signal DC Collector Current for each transistor (driver and output stage)	I_C	1.5	mA
Signal Frequency		1	kHz
Input Resistance	R_s	1100	Ω
Load Resistance	R_L	45	Ω
Power Gain		54	dB
Total Harmonic Distortion ($P_{oe} = 100$ mW)		10 max	%
Power Output (input = 20 mV)	P_{OEB}	100	mW

2N656 Refer to Chart of Discontinued Transistors

2N681-2N690 SILICON CONTROLLED RECTIFIERS

Si all-diffused three-junction types for use in power-control and power-switching applications. JEDEC TO-48, Outline No.20. See Mounting Hardware for desired mounting arrangement.

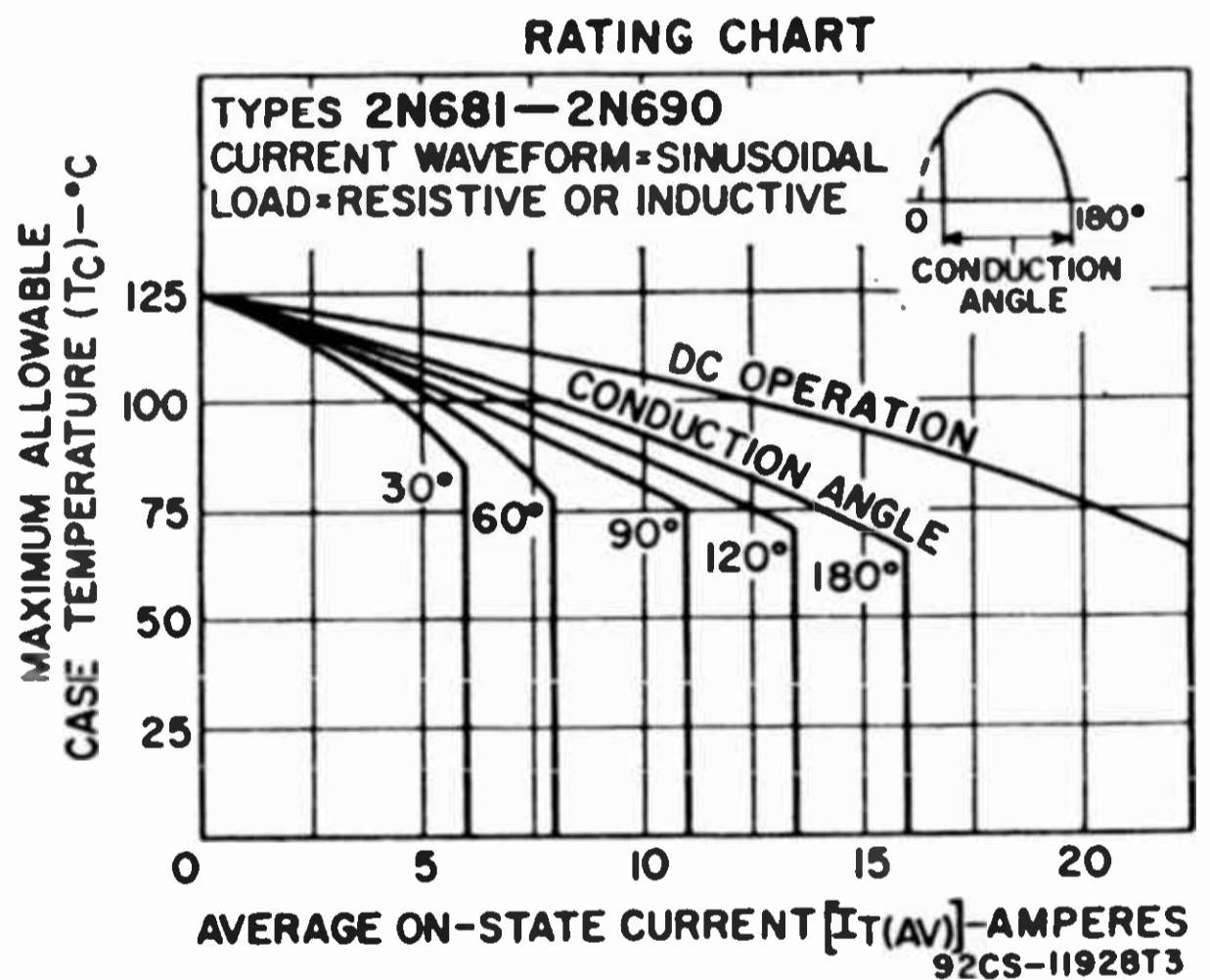
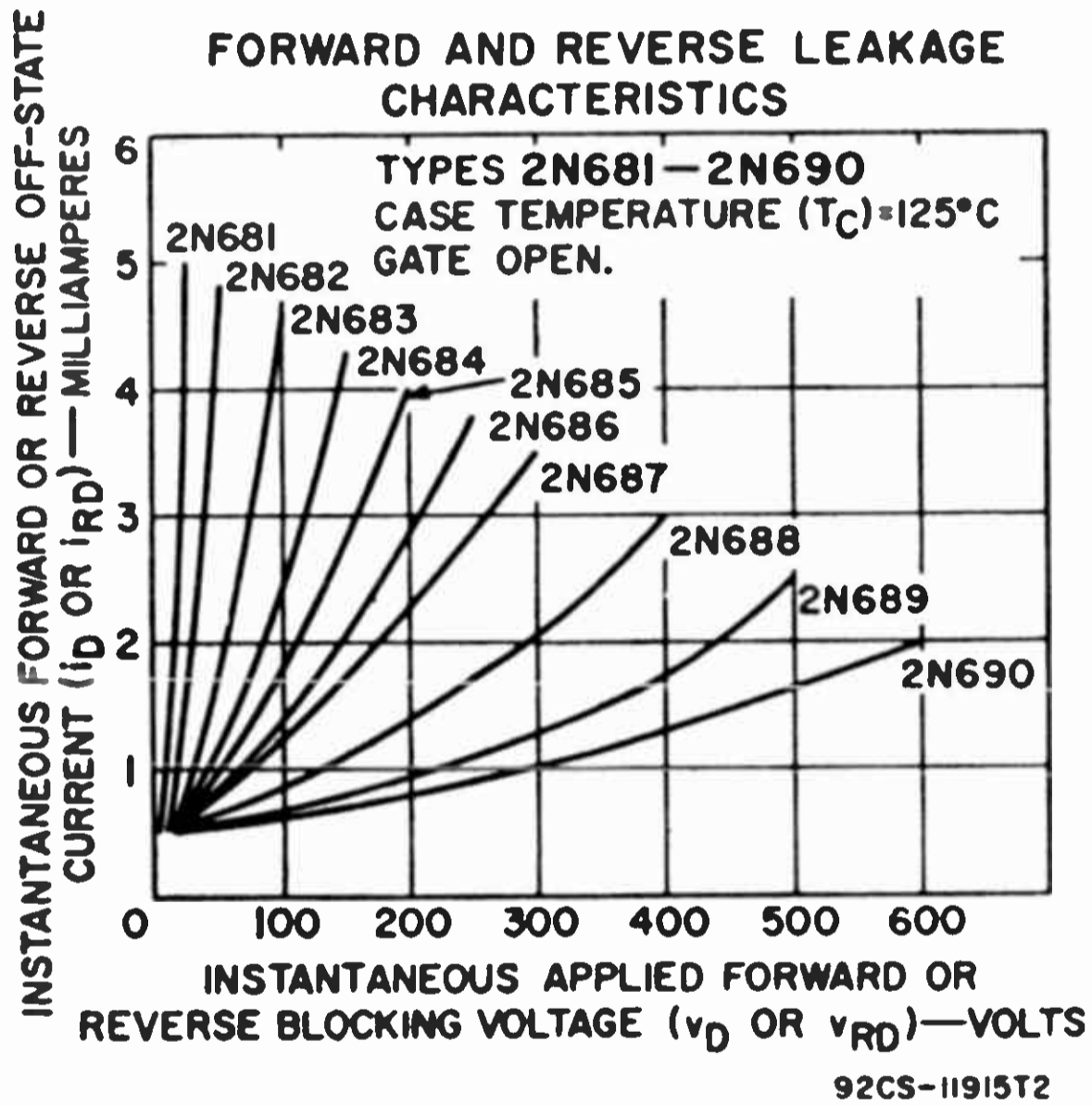


MAXIMUM RATINGS (For sinusoidal ac supply voltage at f = 50 to 400 Hz with resistive or inductive load)

	2N681	2N682	2N683	2N684	2N685	2N686	2N687	2N688	2N689	2N690	
V _{RSOM}	35	75	150	225	300	350	400	500	600	720	V
V _{RROM}	25	50	100	150	200	250	300	400	500	600	V
V _{DROM}	600										V
I _{T(AV)}	16 (conduction angle = 180°, T _c = 65°C)										A
I _{T(RMS)}	25										A
I _{TSM}	150 (1 cycle applied voltage)										A
P _{GM}	5										W
P _{G(AV)}	0.5										W
I _{GTM}	2										A
V _{GTM}	10, 5										V
T _{stg}	-65 to 150										°C
T _c	-65 to 125										°C

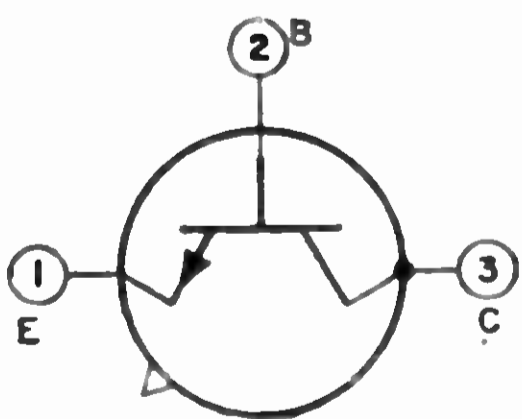
CHARACTERISTICS (At maximum electrical rating at T_c = 125°C)

	2N681	2N682	2N683	2N684	2N685	2N686	2N687	2N688	2N689	2N690	
V _{F(BO)O} (min)	25	50	100	150	200	250	300	400	500	600	V
I _{DOM} (max)	6.5	6.5	6.5	6.5	6	5.5	5	4	3	2.5	mA
I _{RROM} (max)	6.5	6.5	6.5	6.5	6	5.5	5	4	3	2.5	mA
V _T (max) ..	0.86 (on-state current = 25 A, T _c = 65°C)										V
I _{GT} (max) ..	25										mA
V _{GT} (max)	3 (-65 to 125°C)										V
V _{GT} (min)	0.25										V
i _{HO}	15										mA
θ _{J-C}	2										°C/W



Refer to Chart of Discontinued Transistors

2N696



COMPUTER TRANSISTOR

2N697

Si n-p-n planar triple-diffused-base type used in switching applications in data-processing equipment. JEDEC TO-5, Outline No.5.

MAXIMUM RATINGS

Collector-to-Base Voltage	V _{CBO}	60	V
Collector-to-Emitter Voltage:			
R _{BE} ≤ 10 Ω	V _{CER}	40	V
Emitter-to-Base Voltage	V _{EBO}	5	V
Collector Current	I _C	500	mA
Transistor Dissipation:			
T _A up to 25°C	P _T	0.6	W
T _c up to 25°C	P _T	2	W
T _A or T _c above 25°C	P _T	See curve page 300	
Temperature Range:			
Operating (T _A and T _c)	T (opr)	-65 to 175	°C
Storage	T _{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T _L	300	°C

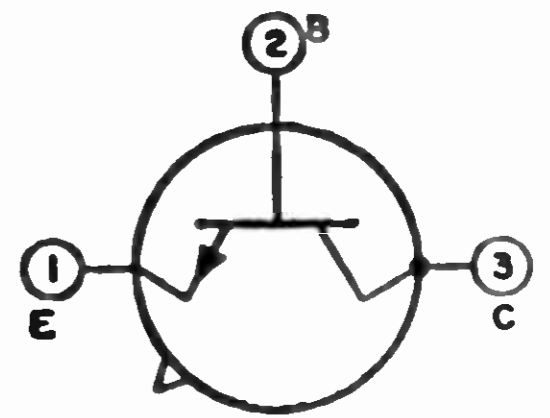
CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = 0.1 \text{ mA}$, $I_E = 0$)	$V_{(BR)CBO}$	60 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.1 \text{ mA}$, $I_C = 0$)	$V_{(BR)EBO}$	5 min	V
Collector-to-Emitter Sustaining Voltage ($I_C = 100 \text{ mA}$, $t_p \leq 12 \text{ ms}$, $df \leq 2\%$, $R_{BE} = 10 \Omega$)	$V_{CE(SUS)}$	40 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 150 \text{ mA}$, $I_B = 15 \text{ mA}$)	$V_{CE(sat)}$	1.5 max	V
Base-to-Emitter Saturation Voltage ($I_C = 150 \text{ mA}$, $I_B = 15 \text{ mA}$)	$V_{BE(sat)}$	1.3 max	V
Collector-Cutoff Current: $V_{CB} = 30 \text{ V}$, $I_E = 0$, $T_A = 25^\circ\text{C}$	I_{CBO}	1 max	μA
$V_{CB} = 30 \text{ V}$, $I_E = 0$, $T_A = 150^\circ\text{C}$	I_{CBO}	100 max	μA
Pulsed Static Forward-Current Transfer Ratio ($V_{CE} = 10 \text{ V}$, $I_C = 150 \text{ mA}$, $t_p \leq 12 \text{ ms}$, $df \leq 2\%$)	h_{FE}	40 to 120	
Small-Signal Forward-Current Transfer Ratio ($f = 20 \text{ MHz}$, $V_{CE} = 10 \text{ V}$, $I_C = 50 \text{ mA}$)	h_{fe}	2.5 min	
Gain-Bandwidth Product	f_T	100 MHz	
Output Capacitance ($V_{CB} = 10 \text{ V}$, $I_E = 0$)	C_{obo}	35 max	pF

2N699

TRANSISTOR

Si n-p-n planar triple-diffused-base type used in small-signal and medium-power applications in rf amplifier, mixer, oscillator and converter service and in power applications in small-signal af amplifiers and switching circuits in industrial and military equipment. JEDEC TO-5, Outline No.5.



MAXIMUM RATINGS

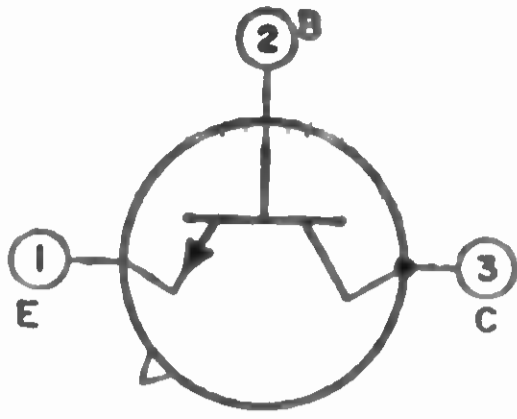
Collector-to-Base Voltage	V_{CBO}	120	V
Collector-to-Emitter Voltage ($R_{BE} \leq 10 \Omega$)	V_{CE}	80	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Transistor Dissipation:			
T_A up to 25°C	P_T	0.6	W
T_c up to 25°C	P_T	2	W
T_A or T_c above 25°C	P_T	See curve page	300
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 175	$^\circ\text{C}$
Storage	T_{STG}	-65 to 200	$^\circ\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	255	$^\circ\text{C}$

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = 0.1 \text{ mA}$, $I_E = 0$)	$V_{(BR)CBO}$	120 min	V
Collector-to-Emitter Sustaining Voltage ($R_{BE} = 10 \Omega$, $I_C = 100 \text{ mA}$, $t_p \leq 300 \mu\text{s}$, $df \leq 2\%$)	$V_{CE(SUS)}$	80 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 150 \text{ mA}$, $I_B = 15 \text{ mA}$, $t_p \leq 300 \mu\text{s}$, $df \leq 2\%$)	$V_{CE(sat)}$	5 max	V
Base-to-Emitter Saturation Voltage ($I_C = 150 \text{ mA}$, $I_B = 15 \text{ mA}$, $t_p \leq 300 \mu\text{s}$, $df \leq 2\%$)	$V_{BE(sat)}$	1.3 max	V
Collector-Cutoff Current ($V_{CB} = 60 \text{ V}$, $I_E = 0$)	I_{CBO}	2 max	μA
Emitter-Cutoff Current ($V_{EB} = 2 \text{ V}$, $I_C = 0$)	I_{EBO}	100 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 10 \text{ V}$, $I_C = 150 \text{ mA}$, $t_p \leq 300 \mu\text{s}$, $df \leq 2\%$)	h_{FE}	40 to 120	
Small-Signal Forward-Current Transfer Ratio:			
$V_{CE} = 5 \text{ V}$, $I_C = 1 \text{ mA}$, $f = 1 \text{ kHz}$	h_{fe}	35 to 100	
$V_{CE} = 10 \text{ V}$, $I_C = 5 \text{ mA}$, $f = 1 \text{ kHz}$	h_{fe}	45 min	
$V_{CE} = 10 \text{ V}$, $I_C = 50 \text{ mA}$, $f = 20 \text{ MHz}$	h_{fe}	2.5 min	
Gain-Bandwidth Product	f_T	50 min	MHz
Output Capacitance ($V_{CB} = 10 \text{ V}$, $I_E = 0$)	C_{obo}	20 max	pF
Small-Signal Short-Circuit Impedance:			
$V_{CE} = 5 \text{ V}$, $I_C = 1 \text{ mA}$, $f = 1 \text{ kHz}$	h_{ib}	30 max	Ω
$V_{CE} = 10 \text{ V}$, $I_C = 5 \text{ mA}$, $f = 1 \text{ kHz}$	h_{ib}	10 max	Ω
Voltage-Feedback Ratio:			
$V_{CE} = 5 \text{ V}$, $I_C = 1 \text{ mA}$, $f = 1 \text{ kHz}$	h_{rb}	2.5×10^{-4} max	
$V_{CE} = 10 \text{ V}$, $I_C = 5 \text{ mA}$, $f = 1 \text{ kHz}$	h_{rb}	3×10^{-4} max	
Output Conductance:			
$V_{CE} = 5 \text{ V}$, $I_C = 1 \text{ mA}$, $f = 1 \text{ kHz}$	h_{ob}	0.5 max	μmho
$V_{CE} = 10 \text{ V}$, $I_C = 5 \text{ mA}$, $f = 1 \text{ kHz}$	h_{ob}	1 max	μmho
Thermal Resistance, Junction-to-Case	θ_{J-C}	75 max	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	250 max	$^\circ\text{C/W}$

2N705

Refer to Chart of Discontinued Transistors



COMPUTER TRANSISTORS

2N706
2N706A

Si n-p-n epitaxial planar types used in high-speed switching applications in data-processing equipment. JEDEC TO-18, Outline No.12.

MAXIMUM RATINGS

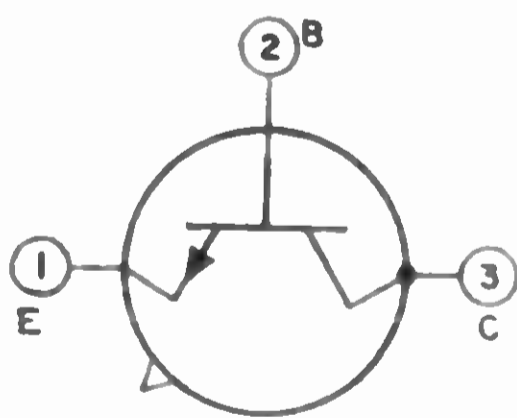
		2N706	2N706A	
Collector-to-Base Voltage	V_{CBO}	25	25	V
Collector-to-Emitter Voltage ($R_{BE} = 10 \Omega$)	V_{CER}	20	20	V
Emitter-to-Base Voltage	V_{EBO}	3	5	V
Collector Current	I_C	—	50	A
Transistor Dissipation:				
T_A up to 25°C	P_T	0.3	0.3	W
T_c (with heat sink) up to 25°C	P_T	1	1	W
T_A or T_c (with heat sink) above 25°C	P_T	See curve page 300		
Temperature Range:				
Operating (Junction)	T_J (opr)	175	175	°C
Storage	T_{STG}	-65 to 175		°C
Lead-Soldering Temperature (10 s max)	T_L	255		°C

CHARACTERISTICS

Collector-to-Emitter Saturation Voltage: ($I_C = 10 \text{ mA}$, $I_B = 1 \text{ mA}$)	$V_{CE}(\text{sat})$	0.6	0.6 max	V
Base-to-Emitter Saturation Voltage: ($I_C = 10 \text{ mA}$, $I_B = 1 \text{ mA}$)	$V_{BE}(\text{sat})$	0.9	0.9 max	V
Collector-Cutoff Current:				
$V_{CB} = 15 \text{ V}$, $I_E = 0$, $T_A = 25^\circ\text{C}$	I_{CBO}	0.5	0.5 max	μA
$V_{CB} = 15 \text{ V}$, $I_E = 0$, $T_A = 150^\circ\text{C}$	I_{CBO}	30	30 max	μA
Static Forward-Current Transfer Ratio:				
$V_{CE} = 1 \text{ V}$, $I_C = 10 \text{ mA}$	h_{FE}	—	20 to 60	
$V_{CE} = 1 \text{ V}$, $I_C = 10 \text{ mA}$, $t_p \leq 12 \text{ ms}$, $df \leq 2\%$	h_{FE}	20	— min	
Small-Signal Forward-Current Transfer Ratio:				
$V_{CE} = 15 \text{ V}$, $I_C = 10 \text{ mA}$, $f = 100 \text{ MHz}$	h_{fe}	2	— min	
$V_{CE} = 10 \text{ V}$, $I_C = 10 \text{ mA}$, $f = 100 \text{ MHz}$	h_{fe}	—	2 min	
Output Capacitance ($V_{CB} = 10 \text{ V}$, $I_E = 0$)	C_{obo}	6	— max	pF
Turn-On Time ($V_{CC} = 3 \text{ V}$, $I_C = 10 \text{ mA}$, $I_{B1} = 3 \text{ mA}$, $I_{B2} = -1 \text{ mA}$, $R_L = 270 \Omega$)	$t_d + t_r$	—	40 max	ns
Turn-Off Time ($V_{CC} = 3 \text{ V}$, $I_C = 10 \text{ mA}$, $I_{B1} = 3 \text{ mA}$, $I_{B2} = -1 \text{ mA}$, $R_L = 270 \Omega$)	$t_s + t_f$	—	75 max	ns
Storage Time ($V_{CC} = 10 \text{ V}$, $I_{B1} = 10 \text{ mA}$, $I_{B2} = -10 \text{ mA}$, $R_L = 1000 \Omega$)	t_s	60	25 max	ns

Refer to Chart of Discontinued Transistors

2N708



COMPUTER TRANSISTOR

2N709

Si n-p-n epitaxial planar type used in switching applications in data-processing equipment. JEDEC TO-18, Outline No.12. This type is identical with type 2N2475 except for the following items:

CHARACTERISTICS

Collector-to-Emitter Saturation Voltage ($I_C = 3 \text{ mA}$, $I_B = 0.15 \text{ mA}$)	$V_{CE}(\text{sat})$	0.3 max	V
Base-to-Emitter Saturation Voltage ($I_C = 3 \text{ mA}$, $I_B = 0.15 \text{ mA}$)	$V_{BE}(\text{sat})$	0.7 to 0.85	V
Static Forward-Current Transfer Ratio:			
$I_C = 10 \text{ mA}$, $V_{CE} = 0.5 \text{ V}$, $T_A = 25^\circ\text{C}$	h_{FE}	20 to 120	
$I_C = 30 \text{ mA}$, $V_{CE} = 1 \text{ V}$, $T_A = 25^\circ\text{C}$	h_{FE}	15 min	
$I_C = 10 \text{ mA}$, $V_{CE} = 0.5 \text{ V}$, $T_A = -55^\circ\text{C}$	h_{FE}	10 min	
Small-Signal Forward-Current Transfer Ratio ($I_C = 5 \text{ mA}$, $V_{CE} = 4 \text{ V}$, $f = 100 \text{ MHz}$)	h_{fe}	6 min	
Input Capacitance ($V_{EB} = 0.5 \text{ V}$, $I_C = 0$, $f = 140 \text{ kHz}$)	C_{ibo}	2 max	pF
Output Capacitance ($V_{CB} = 5 \text{ V}$, $I_E = 0$, $f = 140 \text{ kHz}$)	C_{obo}	3 max	pF
Turn-On Time ($I_C = 10 \text{ mA}$, $I_{B1} = 2 \text{ mA}$, $I_{B2} = -1 \text{ mA}$, $V_{CC} = 1 \text{ V}$)	$t_d + t_r$	15 max	ns
Turn-Off Time ($I_C = 10 \text{ mA}$, $I_{B1} = 2 \text{ mA}$, $I_{B2} = -1 \text{ mA}$, $V_{CC} = 1 \text{ V}$)	$t_s + t_f$	15 max	ns

Refer to Chart of Discontinued Transistors

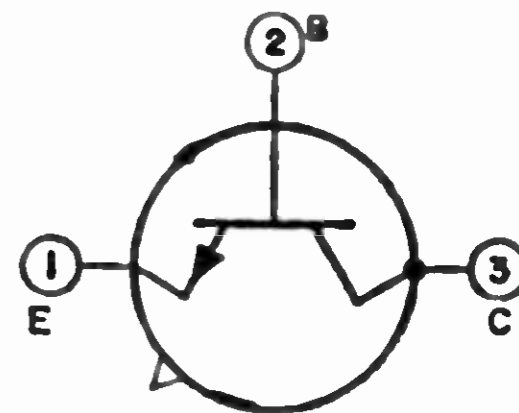
2N710

2N711

Refer to Chart of Discontinued Transistors

2N718A COMPUTER TRANSISTOR

Si n-p-n planar triple-diffused-junction type used primarily for small-signal and switching applications in data-processing equipment. JEDEC TO-18, Outline No.12.



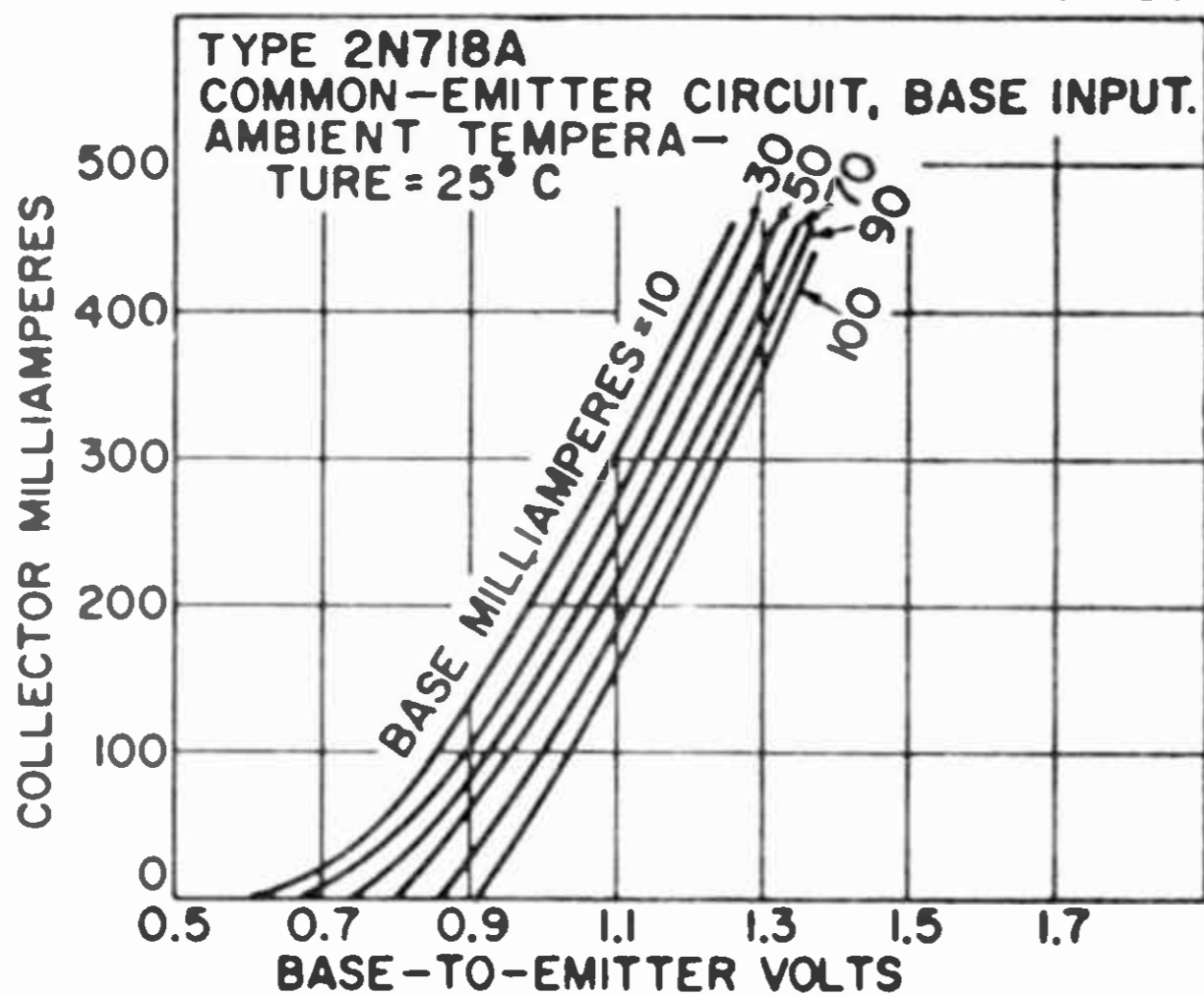
MAXIMUM RATINGS

Collector-to-Base Voltage	V _{CB0}	75	V
Collector-to-Emitter Voltage:			
Base open	V _{CE0}	32	V
R _{BE} ≤ 10 Ω	V _{CER}	50	V
Emitter-to-Base Voltage	V _{EBO}	7	V
Transistor Dissipation:			
T _A up to 25°C	P _T	0.5	W
T _C up to 25°C	P _T	1.8	W
T _A or T _C above 25°C	P _T	See curve page 300	
Temperature Range:			
Operating (Junction)	T _J (opr)	-65 to 200	°C
Storage	T _{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T _L	300	°C

CHARACTERISTICS

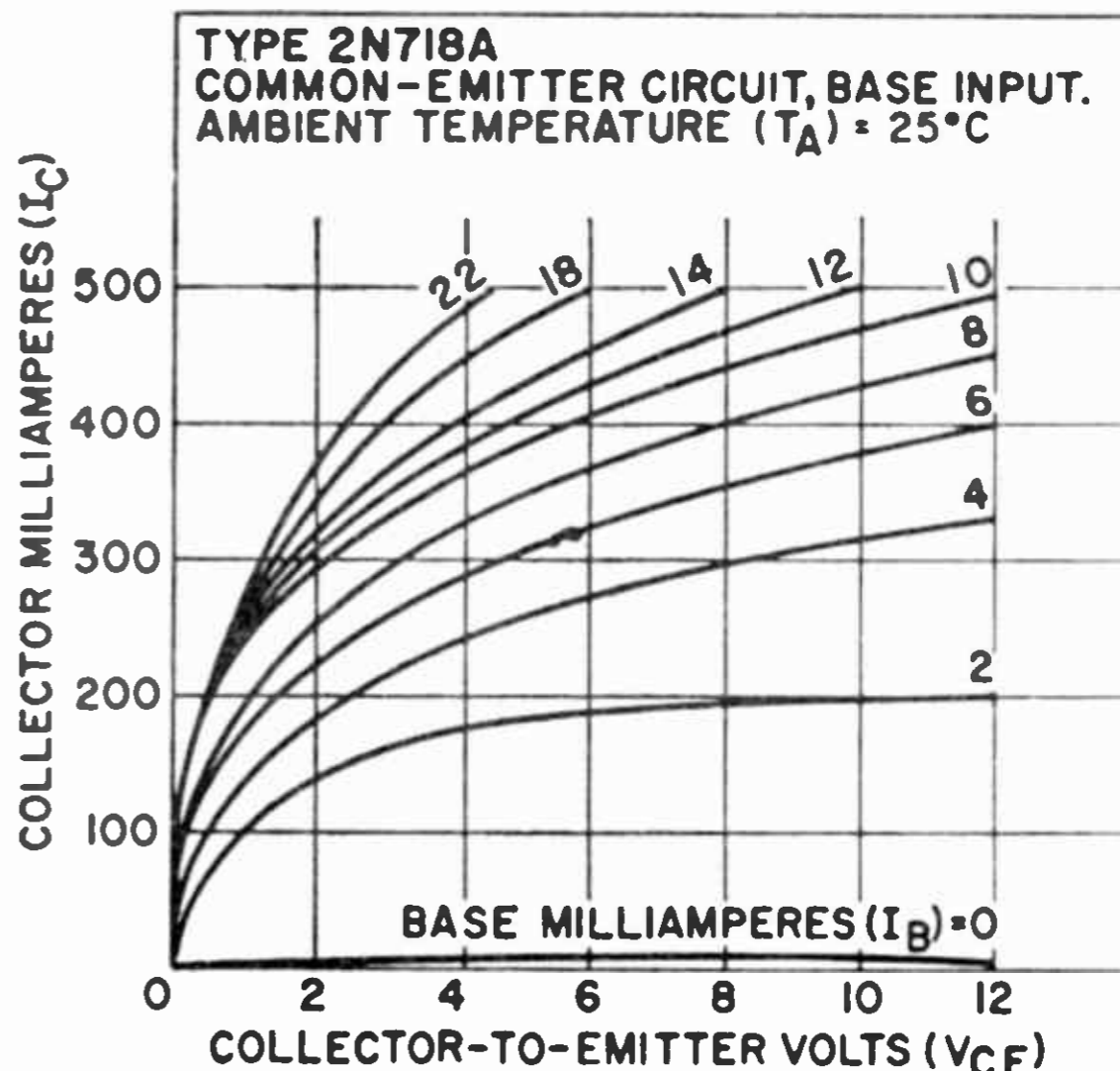
Collector-to-Base Breakdown Voltage (I _C = 0.1 mA, I _E = 0)	V _{(BR)CBO}	75 min	V
Emitter-to-Base Breakdown Voltage (I _E = 0.1 mA, I _C = 0)	V _{(BR)EBO}	7 min	V
Collector-to-Emitter Sustaining Voltage (I _C = 100 mA, I _B = 0, R _{BE} = 10 Ω, t _p ≤ 300 μs, df ≤ 2%)	V _{CER(SUS)}	50 min	V
Collector-to-Emitter Saturation Voltage (I _C = 150 mA, I _B = 15 mA, t _p ≤ 300 μs, df ≤ 2%)	V _{CE(sat)}	1.5 max	V
Base-to-Emitter Saturation Voltage (I _C = 150 mA, I _B = 15 mA, t _p ≤ 300 μs, df ≤ 2%)	V _{BE(sat)}	1.3 max	V
Collector-Cutoff Current:			
V _{CB} = 60 V, I _E = 0, T _A = 25°C	I _{CBO}	0.01 max	μA
V _{CB} = 60 V, I _E = 0, T _A = 150°C	I _{CBO}	10 max	μA
Emitter-Cutoff Current (V _{EB} = 5 V, I _C = 0)	I _{EBO}	0.01 max	μA
Pulsed Static Forward-Current Transfer Ratio:			
V _{CE} = 10 V, I _C = 150 mA, t _p ≤ 300 μs, df ≤ 2%	h _{FE} (pulsed)	40 to 120	
V _{CE} = 10 V, I _C = 10 mA, t _p ≤ 300 μs, df ≤ 2%	h _{FE} (pulsed)	35 min	
V _{CE} = 10 V, I _C = 10 mA, T _A = -55°C, t _p ≤ 300 μs, df ≤ 2%	h _{FE} (pulsed)	20 min	
Static Forward-Current Transfer Ratio (V _{CE} = 10 V, I _C = 0.1 mA)	h _{FE}	20 min	
Small-Signal Forward-Current Transfer Ratio:			
V _{CE} = 5 V, I _C = 1 mA, f = 1 kHz	h _{fe}	30 to 100	
V _{CE} = 10 V, I _C = 5 mA, f = 1 kHz	h _{fe}	35 to 150	
V _{CE} = 10 V, I _C = 50 mA, f = 20 MHz	h _{fe}	3 min	
Input Capacitance (V _{EB} = 0.5 V, I _C = 0)	C _{ibo}	80 max	pF
Output Capacitance (V _{CB} = 10 V, I _E = 0)	C _{obo}	25 max	pF

TYPICAL TRANSFER CHARACTERISTICS



92CS-11185T

TYPICAL COLLECTOR CHARACTERISTICS

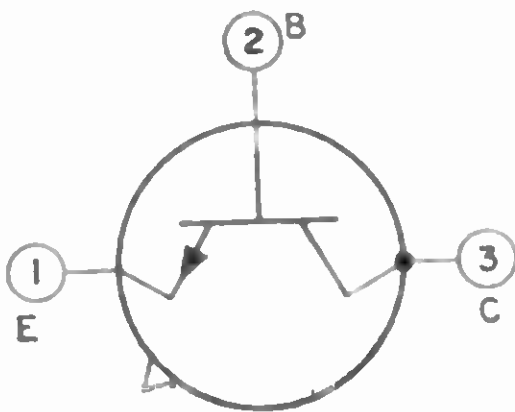


92CS-11189T

CHARACTERISTICS (cont'd)

Input Resistance:			
$V_{CE} = 5\text{ V}, I_C = 1\text{ mA}, f = 1\text{ kHz}$	h_{ib}	24 to 34	Ω
$V_{CE} = 10\text{ V}, I_C = 5\text{ mA}, f = 1\text{ kHz}$	h_{ib}	4 to 8	Ω
Voltage-Feedback Ratio:			
$V_{CE} = 5\text{ V}, I_C = 1\text{ mA}, f = 1\text{ kHz}$	h_{rb}	3×10^{-4} max	
$V_{CE} = 10\text{ V}, I_C = 5\text{ mA}, f = 1\text{ kHz}$	h_{rb}	3×10^{-4} max	
Output Conductance:			
$V_{CE} = 5\text{ V}, I_C = 1\text{ mA}, f = 1\text{ kHz}$	h_{ob}	0.5 max	μmhos
$V_{CE} = 10\text{ V}, I_C = 5\text{ mA}, f = 1\text{ kHz}$	h_{ob}	1 max	μmhos
Noise Figure ($V_{CE} = 10\text{ V}, I_C = 0.3\text{ mA}, f = 1\text{ kHz}$)		NF	12 max
Thermal Resistance, Junction-to-Case		θ_{J-C}	97 max
Thermal Resistance, Junction-to-Ambient		θ_{J-A}	350 max

COMPUTER TRANSISTOR 2N720A



Si n-p-n planar triple-diffused-junction type used primarily in small-signal and switching applications in data-processing equipment. JEDEC TO-18, Outline No.12. For collector and transfer curves, refer to type 2N718A.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	120	V
Collector-to-Emitter Voltage:			
$R_{BE} \leq 10\ \Omega$	V_{CER}	100	V
Base open	V_{CEO}	80	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Transistor Dissipation:			
T_A up to 25°C	P_T	0.5	W
T_C up to 25°C	P_T	1.8	W
T_A or T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 200	$^\circ\text{C}$
Storage	T_{STG}	-65 to 200	$^\circ\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	300	$^\circ\text{C}$

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = 0.1\text{ mA}, I_E = 0$)	$V_{(BR)CBO}$	120 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.1\text{ mA}, I_C = 0$)	$V_{(BR)EBO}$	7 min	V
Collector-to-Emitter Sustaining Voltage:			
$I_C = 100\text{ mA}, I_B = 0, t_p \leq 300\ \mu\text{s}, df \leq 2\%$	$V_{CEO(\text{sus})}$	80 min	V
$I_C = 100\text{ mA}, I_B = 0, R_{BE} = 10\ \Omega, t_p \leq 300\ \mu\text{s}, df \leq 2\%$	$V_{CER(\text{sus})}$	100 min	V
Collector-to-Emitter Saturation Voltage:			
$I_C = 150\text{ mA}, I_B = 15\text{ mA}, t_p \leq 300\ \mu\text{s}, df \leq 2\%$	$V_{CE(\text{sat})}$	5 max	V
$I_C = 50\text{ mA}, I_B = 5\text{ mA}$	$V_{CE(\text{sat})}$	1.2 max	V
Base-to-Emitter Saturation Voltage:			
$I_C = 150\text{ mA}, I_B = 15\text{ mA}, t_p \leq 300\ \mu\text{s}, df \leq 2\%$	$V_{BE(\text{sat})}$	1.3 max	V
$I_C = 50\text{ mA}, I_B = 15\text{ mA}$	$V_{BE(\text{sat})}$	0.9 max	V
Collector-Cutoff Current:			
$V_{CB} = 90\text{ V}, I_E = 0, T_A = 25^\circ\text{C}$	I_{CBO}	0.01 max	μA
$V_{CB} = 90\text{ V}, I_E = 0, T_A = 150^\circ\text{C}$	I_{CBO}	15 max	μA
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}, I_C = 0$)	I_{EBO}	0.01 max	μA
Pulsed Static Forward-Current Transfer Ratio:			
$V_{CE} = 10\text{ V}, I_C = 150\text{ mA}, t_p \leq 300\ \mu\text{s}, df \leq 2\%$	$h_{FE}(\text{pulsed})$	40 to 120	
$V_{CE} = 10\text{ V}, I_C = 10\text{ mA}, t_p \leq 300\ \mu\text{s}, df \leq 2\%$	$h_{FE}(\text{pulsed})$	35 min	
$V_{CE} = 10\text{ V}, I_C = 10\text{ mA}, T_A = -55^\circ\text{C}, t_p \leq 300\ \mu\text{s}, df \leq 2\%$	$h_{FE}(\text{pulsed})$	20 min	
Static Forward-Current Transfer Ratio ($V_{CE} = 10\text{ V}, I_C = 0.1\text{ mA}$)	h_{FE}	20 min	
Small-Signal Forward-Current Transfer Ratio:			
$V_{CE} = 5\text{ V}, I_C = 1\text{ mA}, f = 1\text{ kHz}$	h_{fe}	30 to 100	
$V_{CE} = 10\text{ V}, I_C = 5\text{ mA}, f = 1\text{ kHz}$	h_{fe}	45 min	
$V_{CE} = 10\text{ V}, I_C = 50\text{ mA}, f = 20\text{ MHz}$	h_{fe}	2.5 min	
Input Capacitance ($V_{EB} = 0.5\text{ V}, I_C = 0$)	C_{ibo}	85 max	pF
Output Capacitance ($V_{CBO} = 10\text{ V}, I_E = 0$)	C_{obo}	15 max	pF
Input Resistance:			
$V_{CE} = 5\text{ V}, I_C = 1\text{ mA}, f = 1\text{ kHz}$	h_{ib}	20 to 30	Ω
$V_{CE} = 10\text{ V}, I_C = 5\text{ mA}, f = 1\text{ kHz}$	h_{ib}	4 to 8	Ω
Voltage-Feedback Ratio:			
$V_{CE} = 5\text{ V}, I_C = 1\text{ mA}, f = 1\text{ kHz}$	h_{rb}	1.25×10^{-4} max	
$V_{CE} = 10\text{ V}, I_C = 5\text{ mA}, f = 1\text{ kHz}$	h_{rb}	1.5×10^{-4} max	

CHARACTERISTICS (cont'd)

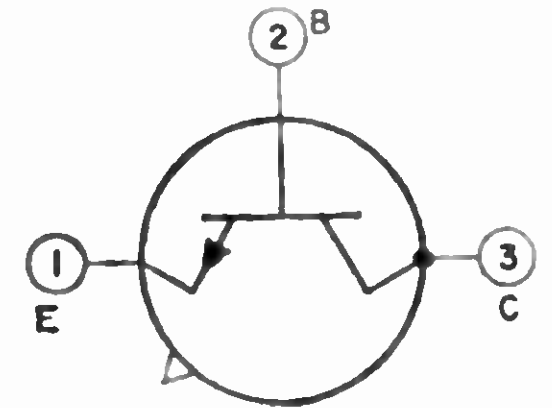
Output Conductance:

$V_{CE} = 5 \text{ V}, I_C = 1 \text{ mA}, f = 1 \text{ kHz}$	h_{ob}	0.5 max	μhos
$V_{CE} = 10 \text{ V}, I_C = 5 \text{ mA}, f = 1 \text{ kHz}$	h_{ob}	0.5 max	μhos
Thermal Resistance, Junction-to-Case	Θ_{J-C}	97 max	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Ambient	Θ_{J-A}	350 max	$^{\circ}\text{C/W}$

- 2N794** Refer to Chart of Discontinued Transistors
- 2N795** Refer to Chart of Discontinued Transistors
- 2N796** Refer to Chart of Discontinued Transistors
- 2N828** Refer to Chart of Discontinued Transistors

2N834 COMPUTER TRANSISTOR

Si n-p-n epitaxial planar type used in high-speed switching applications in equipment requiring high reliability and high packing densities. JEDEC TO-18, Outline No.12.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CB0}	40	V
Collector-to-Emitter Voltage ($R_{BE} = 0$)	V_{CES}	30	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	200	mA
Transistor Dissipation:			
T_A up to 25°C	P_T	0.3	W
T_c up to 25°C	P_T	1	W
T_A or T_c above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	175	$^{\circ}\text{C}$
Storage	T_{STG}	-65 to 175	$^{\circ}\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	240	$^{\circ}\text{C}$

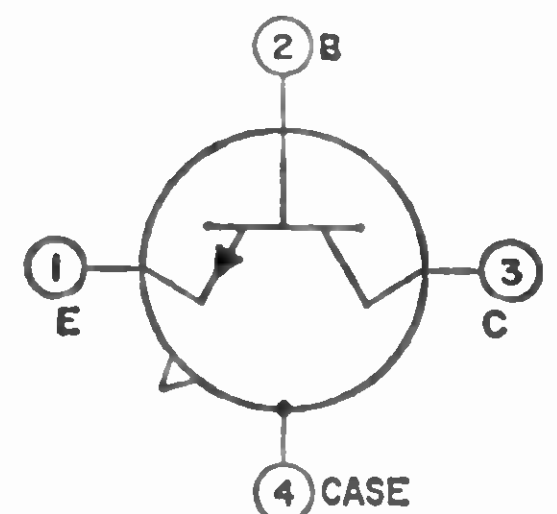
CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = 0.1 \text{ mA}, I_E = 0$)	$V_{(BR)CBO}$	40 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.1 \text{ mA}, I_C = 0$)	$V_{(BR)EBO}$	5 min	V
Collector-to-Emitter Saturation Voltage:			
$I_C = 10 \text{ mA}, I_B = 1 \text{ mA}$	$V_{CE(\text{sat})}$	0.25 max	V
$I_C = 50 \text{ mA}, I_B = 5 \text{ mA}$	$V_{CE(\text{sat})}$	0.4 max	V
Base-to-Emitter Saturation Voltage ($I_C = 10 \text{ mA}, I_B = 1 \text{ mA}$)	$V_{BE(\text{sat})}$	0.9 max	
Collector-Cutoff Current:			
$V_{CB} = 20 \text{ V}, I_E = 0, T_A = 25^{\circ}\text{C}$	I_{CBO}	0.5 max	μA
$V_{CB} = 20 \text{ V}, I_E = 0, T_A = 150^{\circ}\text{C}$	I_{CBO}	30 max	μA
$V_{CE} = 30 \text{ V}, R_{BE} = 0, T_A = 25^{\circ}\text{C}$	I_{CES}	10 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 1 \text{ V}, I_C = 10 \text{ mA}$)	h_{FE}	25 min	
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 15 \text{ V}, I_C = 10 \text{ mA}, f = 100 \text{ MHz}$)	h_{fe}	3.5 min	
Output Capacitance ($V_{CB} = 10 \text{ V}, I_E = 0, f = 100 \text{ kHz}$)	C_{ob0}	4 max	pF
Gain-Bandwidth Product ($V_{CE} = 15 \text{ V}, I_C = 10 \text{ mA}, f = 100 \text{ MHz}$)	f_T	350 min	MHz
Storage Time ($V_{CC} = 10 \text{ V}, I_{B1} = 10 \text{ mA}, I_{B2} = -10 \text{ mA}, I_C = 10 \text{ mA}$)			
Turn-On Time ($V_{CC} = 0$ to $3.5 \text{ V}, I_C = 10 \text{ mA}$)	$t_s + t_r$	25 max	ns
Turn-off Time ($V_{CC} = 0$ to $3.5 \text{ V}, I_C = 10 \text{ mA}$)	$t_s + t_f$	35 max	ns
		75 max	ns

- 2N914** Refer to Chart of Discontinued Transistors

2N917 TRANSISTOR

Si n-p-n epitaxial planar type used in low-noise amplifier, oscillator, and converter applications at vhf frequencies. JEDEC TO-72, Outline No.28.



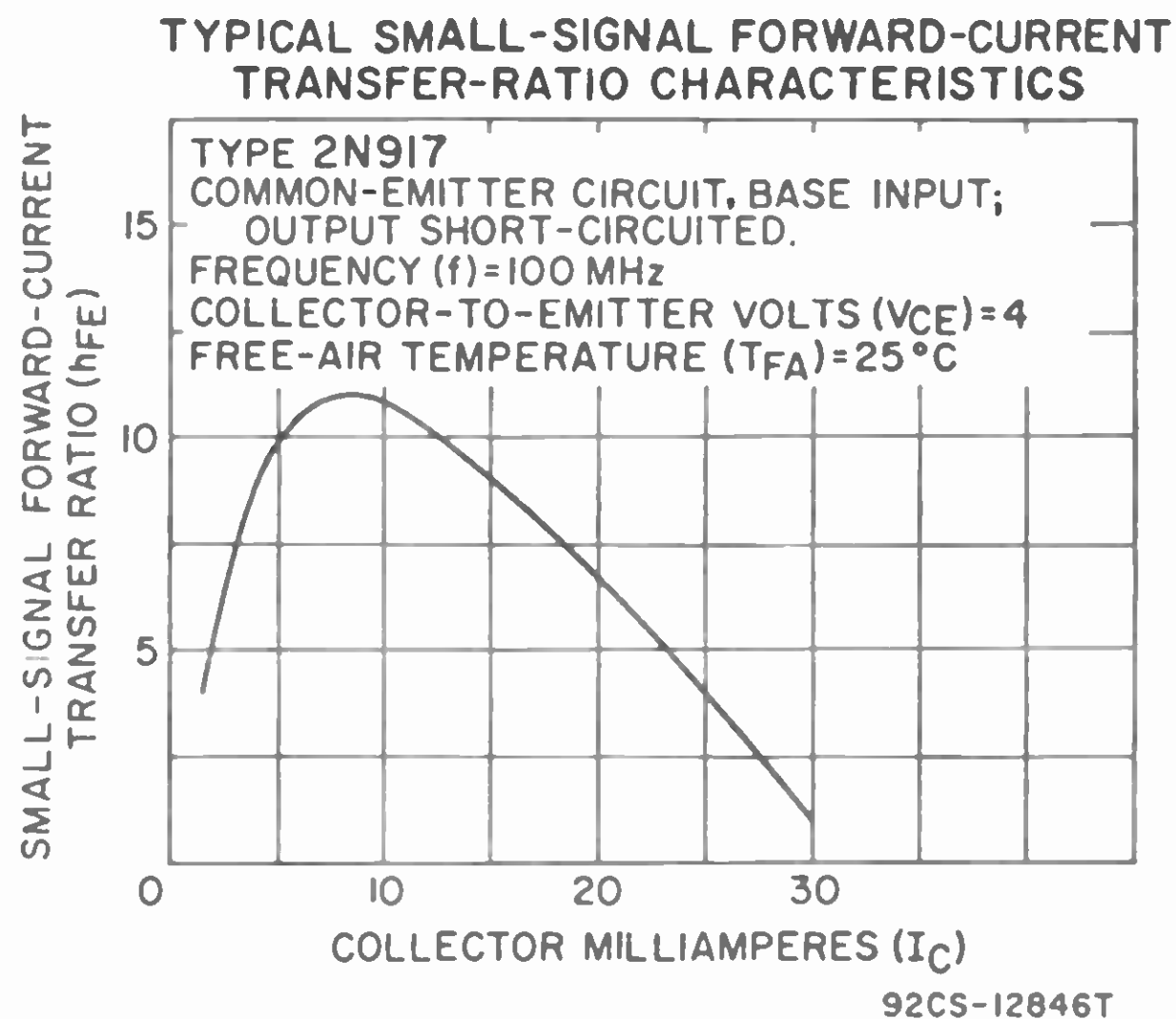
MAXIMUM RATINGS

Collector-to-Base Voltage	V _{CB0}	30	V
Collector-to-Emitter Voltage	V _{CE0}	15	C
Emitter-to-Base Voltage	V _{EB0}	3	V
Collector Current	I _C	Limited by power dissipation	
Transistor Dissipation:			
T _A up to 25°C	P _T	200	mW
T _C up to 25°C	P _T	300	mW
T _A or T _C above 25°C	P _T	See curve page 300	
Temperature Range:			
Operating (Junction)	T _J	-65 to 200	°C
Storage	T _{STG}	-65 to 200	°C
Lead-Soldering Temperature (60 s max)	T _L	300	°C

CHARACTERISTICS

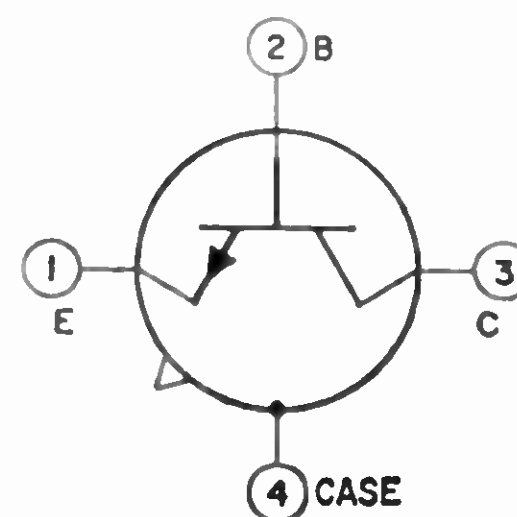
Collector-to-Base Breakdown Voltage (I _C = 0.001 mA, I _E = 0)	V _{(BR)CBO}	30 min	V
Emitter-to-Base Breakdown Voltage (I _E = 0.01 mA, I _C = 0)	V _{(BR)EBO}	3 min	V
Collector-to-Emitter Sustaining Voltage (I _C = 3 mA, I _B = 0, t _p = 300 μs, df = 1%)	V _{CE0(SUS)}	15 min	V
Collector-to-Emitter Saturation Voltage (I _C = 3 mA, I _B = 0.15 mA)	V _{CE(sat)}	0.5 max	V
Base-to-Emitter Saturation Voltage (I _C = 3 mA, I _B = 0.15 mA)	V _{BE(sat)}	0.87 max	V
Collector-Cutoff Current:			
V _{CB} = 15 V, I _E = 0, T _A = 25°C	I _{CBO}	0.001 max	μA
V _{CB} = 15 V, I _E = 0, T _A = 150°C	I _{CBO}	0.1 max	μA
Static Forward-Current Transfer Ratio (V _{CE} = 1 V, I _C = 3 mA)	h _{FE}	20 to 200	
Small-Signal Forward-Current Transfer Ratio* (V _{CE} = 10 V, I _C = 4 mA, f = 100 MHz)	h _{fe}	5 min	
Input Capacitance† (V _{EB} = 0.5 V, I _C = 0, f = 0.1 to 1 MHz)	C _{ibo}	1.6 max	pF
Output Capacitance† (V _{CB} = 10 V, I _E = 0, f = 0.1 to 1 MHz)	C _{obo}	1.7 max	pF
Collector-to-Base Time Constant* (V _{CB} = 10 V, I _C = 4 mA, f = 40 MHz)	r _b 'C _c	75 max	ps
Small-Signal Power Gain, Unneutralized Amplifier Circuit* (V _{CE} = 10 V, I _C = 5 mA, f = 200 MHz)			
G _{pe}		9 min	dB
Power Output in Oscillator Circuit† (V _{CB} = 15 V, I _C = 8 mA, f = 500 MHz)			
P _{oe}		10 min	mW
Noise Figure† (V _{CE} = 6 V, I _C = 1 mA, R _G = 400 Ω, f = 60 MHz)	NF	6 max	dB

* Fourth lead (case) grounded.
 † Fourth lead (case) floating.



2N918 TRANSISTOR

Si n-p-n epitaxial planar type used in low-noise amplifier, oscillator, and converter applications at vhf frequencies. JEDEC TO-72, Outline No.28. This type is identical with type 2N3600 except for the following items:



MAXIMUM RATINGS

Collector Current	I_c	50	mA
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CHARACTERISTICS

Small-Signal Forward-Current Transfer Ratio* ($f = 100$ MHz, $V_{CE} = 10$ V, $I_C = 4$ mA)	h_{fe}	6 min	
Input Capacitance ($f = 0.1$ to 1 MHz, $V_{EB} = 0.5$ V, $I_C = 0$)	C_{ibo}	2 max	pF
Output Capacitance:■ $V_{CB} = 10$ V, $I_E = 0$, $f = 0.1$ to 1 MHz	C_{obo}	1.7 max	pF
$V_{CB} = 0$, $I_E = 0$, $f = 0.1$ to 1 MHz	C_{obo}	3 max	pF
Collector-to-Base Time Constant* ($f = 40$ MHz, $V_{CB} = 6$ V, $I_C = 2$ mA)	$r_b'C_c$	15	ps
Small-Signal Power Gain:*			
Unneutralized Amplifier Circuit ($V_{CE} = 10$ V, $I_C = 5$ mA, $f = 200$ MHz)	G_{pe}	13	dB
Neutralized Amplifier Circuit ($V_{CE} = 12$ V, $I_C = 6$ mA, $f = 200$ MHz)	G_{pe}	15 min	dB
Power Output, Oscillator Circuit† ($V_{CB} = 10$ V, $I_E = 12$ mA, $f = 500$ MHz)	P_{oe}	18 typ	dB
Noise Figure* ($V_{CE} = 6$ V, $I_C = 1$ mA, $R_G = 400 \Omega$, $f = 60$ MHz)	NF	30 min	mW
		6 max	dB

* Fourth lead (case) grounded.

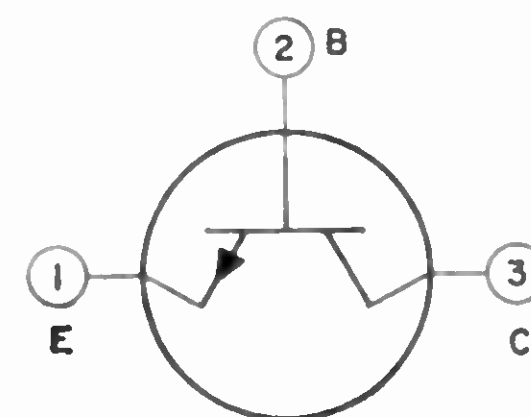
■ Three-terminal measurement of the collector-to-base capacitance with the case and emitter leads connected to the guard terminal.

† Fourth lead (case) floating.

2N955	Refer to Chart of Discontinued Transistors
2N955A	Refer to Chart of Discontinued Transistors
2N960	Refer to Chart of Discontinued Transistors
2N961	Refer to Chart of Discontinued Transistors
2N962	Refer to Chart of Discontinued Transistors
2N963	Refer to Chart of Discontinued Transistors
2N964	Refer to Chart of Discontinued Transistors
2N965	Refer to Chart of Discontinued Transistors
2N966	Refer to Chart of Discontinued Transistors
2N967	Refer to Chart of Discontinued Transistors

2N1010 TRANSISTOR

Ge n-p-n alloy-junction type used in small-signal low-noise af amplifier applications such as high-fidelity amplifiers, tape-recorder amplifiers, microphone pre-amplifiers, and hearing aids. JEDEC TO-1, Outline No.1.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	10	V
Collector Current	I_C	2	mA

MAXIMUM RATINGS (cont'd)

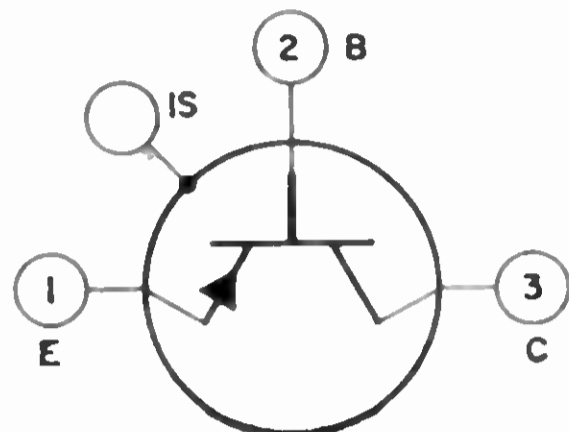
Transistor Dissipation:			
$T_A = 25^\circ\text{C}$	P_T	20	mW
Temperature Range:			
Operating (Ambient)	$T_A(\text{opr})$	-65 to 55	$^\circ\text{C}$

CHARACTERISTICS

Collector-Cutoff Current ($V_{CB} = 10\text{ V}, I_E = 0$)	I_{CBO}	10 max	μA
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 3.5\text{ V}, I_E = -0.3\text{ mA}, f = 1\text{ kHz}$)	h_{fe}	35	
Small-Signal Forward-Current Transfer-Ratio Cutoff Frequency ($V_{CB} = 3.5\text{ V}, I_C = 0.3\text{ mA}$)	f_{hfb}	2	MHz

Refer to Chart of Discontinued Transistors

2N1014



TRANSISTOR

2N1023

Ge p-n-p alloy-junction drift-field type used in rf and if amplifier, oscillator, mixer, and converter circuits, military equipment. JEDEC TO-44, Outline No.17.

MAXIMUM RATINGS

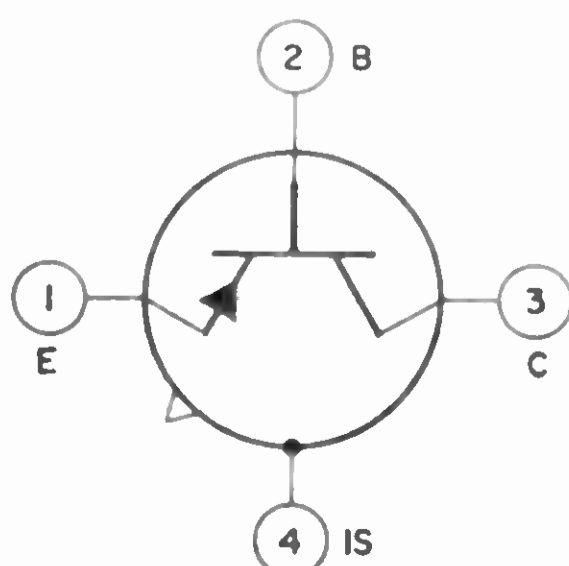
Collector-to-Base Voltage	V_{CBO}	-40	V
Collector-to-Emitter Voltage ($V_{BE} = 0.5\text{ V}$)	V_{CEV}	-40	V
Emitter-to-Base Voltage	V_{EBO}	-0.5	V
Collector Current	I_C	-10	mA
Emitter Current	I_E	10	mA
Transistor Dissipation:			
T_A up to 25°C	P_T	120	mW
T_A above 25°C	P_T	See curve page 300	
T_C up to 25°C (with heat sink)	P_T	240	mW
T_C above 25°C (with heat sink)	P_T	See curve page 300	
Temperature Range:			
Operating (T_A) and Storage (T_{STG})		-65 to 100	$^\circ\text{C}$

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = -50\ \mu\text{A}, I_E = 0$)	$V_{(BR)CBO}$	-40 min	V
Collector-to-Base Reach-Through Voltage ($V_{EB} = -0.5$)	V_{RT}	-40 min	V
Collector-Cutoff Current ($V_{CB} = -12\text{ V}, I_E = 0$)	I_{CBO}	-12 max	μA
Emitter-Cutoff Current ($V_{EB} = -0.5\text{ V}, I_C = 0$)	I_{EBO}	-12 max	μA
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = -12\text{ V}, I_E = 1.5\text{ mA}, f = 1\text{ kHz}$)	h_{fe}	20 to 175	
Small-Signal Forward-Current Transfer Ratio Cutoff Frequency ($V_{CB} = -12\text{ V}, I_E = 1.5\text{ mA}$)	f_{hfb}	120	MHz
Output Capacitance ($V_{CB} = -12\text{ V}, I_E = 0$)	C_{obo}	3 max	pF
Input Resistance (ac output circuit shorted):			
$V_{CB} = -12\text{ V}, I_E = 1.5\text{ mA}, f = 50\text{ MHz}$	R_{ie}	25	Ω
$V_{CE} = -12\text{ V}, I_E = 1.5\text{ mA}, f = 30\text{ MHz}$	R_{ie}	100	Ω
Output Resistance (ac input circuit shorted):			
$V_{CB} = -12\text{ V}, I_E = 1.5\text{ mA}, f = 50\text{ MHz}$	R_{oe}	8000	Ω
$V_{CE} = -12\text{ V}, I_E = 1.5\text{ mA}, f = 30\text{ MHz}$	R_{oe}	8000	Ω
Power Gain, Single-Tuned Unilateral Circuit):			
$V_{CB} = -12\text{ V}, I_E = 1.5\text{ mA}, f = 50\text{ MHz}$	G_{pe}	18 to 24	dB
$V_{CE} = -12\text{ V}, I_E = 1.5\text{ mA}, f = 30\text{ MHz}$	G_{pe}	20 to 26	dB
Thermal Resistance, Junction-to-Case	θ_{J-C}	0.31 max	$^\circ\text{C}/\text{mW}$
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	0.62 max	$^\circ\text{C}/\text{mW}$

TYPICAL OPERATION IN POWER-SWITCHING CIRCUIT

DC Collector-to-Emitter Voltage	V_{CE}	-12	V
DC Emitter Current	I_E	5.8	mA
Source Impedance	R_S	150	Ω
Capacitive Load		16	pF
Frequency Response		20 Hz to 11 MHz	
Pulse Rise Time	t_r	0.032	μs
Voltage Gain		26	dB
Maximum Peak-to-Peak Output Voltage		20	V



TRANSISTOR

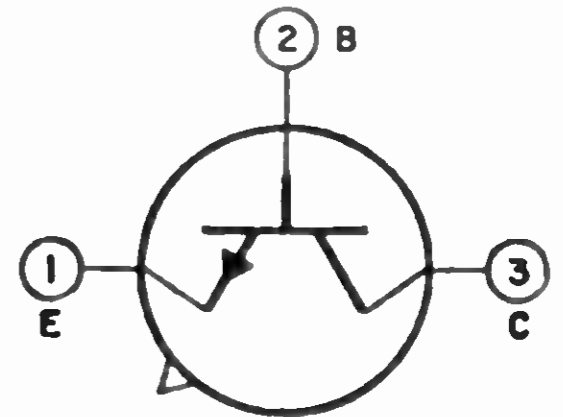
2N1066

Ge p-n-p alloy-junction drift-field type used in rf and if amplifier, oscillator, mixer, and converter circuits, and low-level video-amplifier circuits in industrial and military equipment. JEDEC TO-33, Outline No.13. This type is electrically identical with type 2N1023.

2N1067	Refer to Chart of Discontinued Transistors
2N1068	Refer to Chart of Discontinued Transistors
2N1069	Refer to Chart of Discontinued Transistors
2N1070	Refer to Chart of Discontinued Transistors

2N1090 COMPUTER TRANSISTOR

Ge n-p-n alloy-junction type used in high-current medium-speed switching circuits in electronic computers. JEDEC TO-5, Outline No.5.



MAXIMUM RATINGS

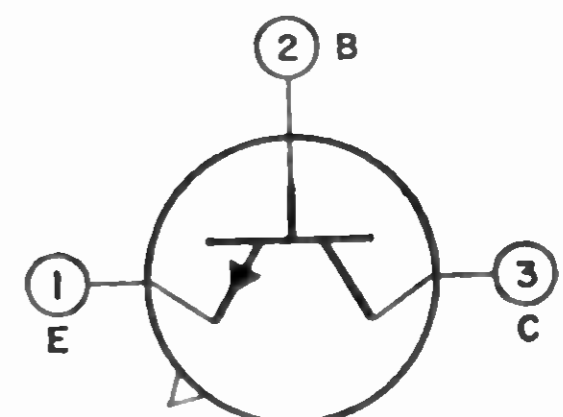
Collector-to-Base Voltage	V_{CBO}	25	V
Collector-to-Emitter Voltage:			
$V_{BE} = -1$ V	V_{CEV}	18	V
Base open	V_{CEO}	15	V
Emitter-to-Base Voltage	V_{EBO}	20	V
Collector Current	I_C	400	mA
Emitter Current	I_E	-400	mA
Transistor Dissipation:			
T_A up to 25°C	P_T	120	mW
T_A above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Ambient)	T_A (opr)	85	°C
Storage	T_{STG}	-65 to 85	°C
Lead-Soldering Temperature (10s max)	T_L	255	°C

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = 25 \mu A$, $I_E = 0$)	$V_{(BR)CBO}$	25 min	V
Collector-to-Emitter Breakdown Voltage ($I_C = 600 \mu A$, $I_B = 0$)	$V_{(BR)CEO}$	15 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 25 \mu A$, $I_C = 0$)	$V_{(BR)EBO}$	20 min	V
Base-to-Emitter Saturation Voltage:			
$I_C = 20$ mA, $I_B = 0.67$ mA	$V_{BE}(\text{sat})$	0.4 max	V
$I_C = 200$ mA, $I_B = 10$ mA	$V_{BE}(\text{sat})$	1.5 max	V
Collector-to-Emitter Saturation Voltage:			
$I_C = 20$ mA, $I_B = 0.67$ mA	$V_{CE}(\text{sat})$	0.2 max	V
$I_C = 200$ mA, $I_B = 10$ mA	$V_{CE}(\text{sat})$	0.3 max	V
Collector-Cutoff Current ($V_{CB} = 12$ V, $I_E = 0$)	I_{CBO}	8 max	μA
Emitter-Cutoff Current ($V_{BE} = 5$ V, $I_C = 0$)	I_{EBO}	5 max	μA
Static Forward-Current Transfer Ratio:			
$V_{CE} = 0.2$ V, $I_C = 20$ mA	h_{FE}	30 min	
$V_{CE} = 0.3$ V, $I_C = 200$ mA	h_{FE}	20 min	
Small-Signal Forward-Current Transfer-Ratio			
Cutoff Frequency ($V_{CB} = 6$ V, $I_E = -1$ mA)	f_{hfb}	5 min	MHz
Output Capacitance ($V_{CB} = 6$ V, $I_E = 0$)	C_{obo}	25 max	pF
Stored Base Charge ($I_C = 20$ mA, $I_B = 1.33$ mA)	Q_s	1600 max	pC

2N1091 COMPUTER TRANSISTOR

Ge n-p-n alloy-junction type used in high-current medium-speed switching circuits in electronic computers. JEDEC TO-5, Outline No.5. This type is identical with type 2N1090 except for the following items:



MAXIMUM RATINGS

Collector-to-Emitter Voltage:			
$V_{BE} = -1$ V	V_{CEV}	15	V
Base open	V_{CEO}	12	V

CHARACTERISTICS

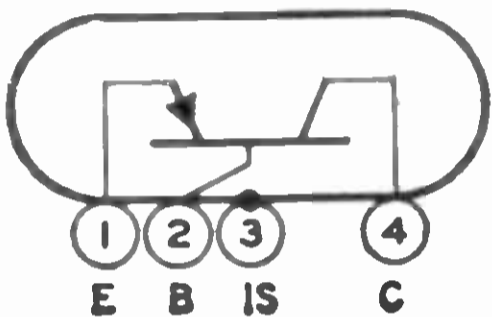
Collector-to-Emitter Breakdown Voltage ($I_C = 600 \mu A$, $I_B = 0$)	$V_{(BR)CEO}$	12 min	V
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CHARACTERISTICS (cont'd)

Base-to-Emitter Saturation Voltage:

$I_C = 20 \text{ mA}, I_B = 0.5 \text{ mA}$	$V_{BE(sat)}$	0.35 max	V
$I_C = 200 \text{ mA}, I_B = 6.7 \text{ mA}$	$V_{BE(sat)}$	1.1 max	V
Collector-to-Emitter Saturation Voltage:			
$I_C = 20 \text{ mA}, I_B = 0.5 \text{ mA}$	$V_{CE(sat)}$	0.2 max	V
$I_C = 200 \text{ mA}, I_B = 6.7 \text{ mA}$	$V_{CE(sat)}$	0.3 max	V
Static Forward-Current Transfer Ratio:			
$V_{CE} = 0.2 \text{ V}, I_C = 20 \text{ mA}$	h_{FE}	40 min	
$V_{CE} = 0.3 \text{ V}, I_C = 200 \text{ mA}$	h_{FE}	30 min	
Small-Signal Forward-Current Transfer Ratio			
Cutoff Frequency ($V_{CB} = 6 \text{ V}, I_E = -1 \text{ mA}$)	f_{hfb}	10 min	MHz
Stored Base Charge ($I_C = 20 \text{ mA}, I_B = 1 \text{ mA}$)	Q_s	1000 max	pC

- Refer to Chart of Discontinued Transistors **2N1092**
- Refer to Chart of Discontinued Transistors **2N1099**
- Refer to Chart of Discontinued Transistors **2N1100**
- Refer to Chart of Discontinued Transistors **2N1169**
- Refer to Chart of Discontinued Transistors **2N1170**



TRANSISTOR

2N1177

Ge p-n-p alloy-junction drift-field type used in radio-frequency amplifier applications in FM and AM/FM radio receivers. JEDEC TO-45, Outline No.18.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-30	V
Collector Current	I_C	-10	mA
Transistor Dissipation:			
$T_A = 25^\circ\text{C}$	P_T	80	mW
Temperature Range:			
Operating (Ambient)	$T_A(\text{opr})$	-65 to 71	$^\circ\text{C}$

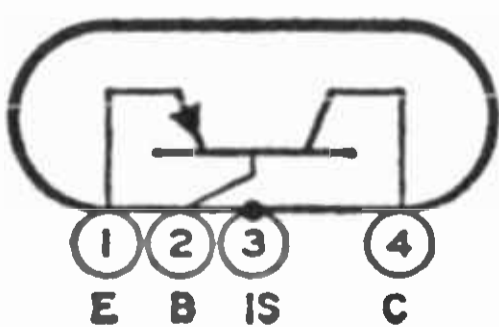
CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($V_{BE} = 0.5 \text{ V}, I_C = -50 \mu\text{A}$)	$V_{(BR)CBO}$	-30 min	V
Collector-Cutoff Current ($V_{CB} = -12 \text{ V}, I_E = 0$)	I_{CBO}	-12 max	μA
Small-Signal Forward-Current Transfer Ratio			
($V_{CE} = -12 \text{ V}, I_C = -1 \text{ mA}, f = 1 \text{ kHz}$)	h_{fe}	100 min	
Small-Signal Forward-Current Transfer-Ratio			
Cutoff Frequency	f_{hfb}	140	MHz
Output Capacitance	C_{ob0}	2	pF
Power Gain ($f = 100 \text{ MHz}$)	G_{pe}	14	dB

TRANSISTOR

2N1178

Ge p-n-p alloy-junction drift-field type used in radio-frequency oscillator applications in FM and AM/FM radio receivers. JEDEC TO-45, Outline No.18. This type is identical with type 2N1177 except for the following item:



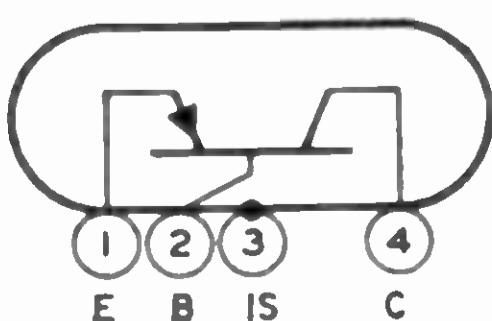
CHARACTERISTICS

Small-Signal Forward-Current Transfer Ratio			
($V_{CE} = -12 \text{ V}, I_C = -1 \text{ mA}, f = 1 \text{ kHz}$)	h_{fe}	40 min	

TRANSISTOR

2N1179

Ge p-n-p alloy-junction drift-field type used in radio-frequency mixer applications in FM and AM/FM radio receivers. JEDEC TO-45, Outline No.18. This type is identical with type 2N1177 except for the following items:



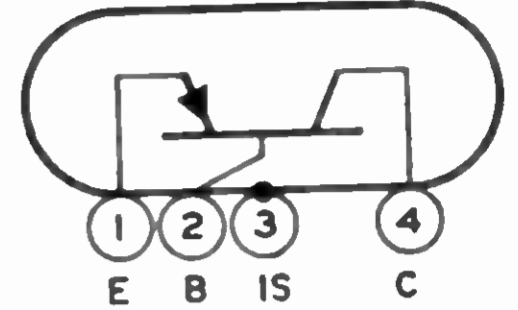
CHARACTERISTICS

Small-Signal Forward-Current Transfer Ratio

($V_{CE} = -12$ V, $I_C = -1$ mA, $f = 1$ kHz)	h_{re}	80 min	
Oscillator Injection Voltage ($f = 100$ MHz)		125 max	mV
Power Gain ($f = 100$ MHz)	G_{pe}	17	dB

2N1180**TRANSISTOR**

Ge p-n-p alloy-junction drift-field type used in intermediate-frequency amplifier applications in FM and AM/FM radio receivers. JEDEC TO-45, Outline No.18. This type is identical with type 2N1177 except for the following items:

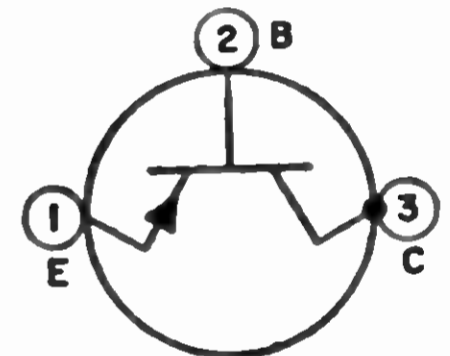
**CHARACTERISTICS**

Small-Signal Forward-Current Transfer Ratio

($V_{CE} = -12$ V, $I_C = -1$ mA, $f = 1$ kHz)	h_{re}	80 min	
Small-Signal Forward-Current Transfer Ratio Cutoff Frequency ($V_{CB} = -12$ V, $I_C = -1$ mA)	f_{hrb}	100	MHz
Power Gain ($f = 10.7$ MHz)	G_{pe}	35	dB

2N1183**2N1183A****POWER TRANSISTORS****2N1183B**

Ge p-n-p alloy-junction types intended for use in intermediate-power switching and low-frequency amplifier applications in industrial and military equipment. JEDEC TO-8, Outline No.10. See Mounting Hardware for desired mounting arrangement.

**MAXIMUM RATINGS**

		2N1183	2N1183A	2N1183B	
Collector-to-Base Voltage	V_{CBO}	-45	-60	-80	V
Collector-to-Emitter Voltage:					
$V_{BE} = 1.2$ V	V_{CEV}	-45	-60	-80	V
$R_{BE} = 0$	V_{CES}	-35	-50	-60	V
Base open	V_{CEO}	-20	-30	-40	V
Emitter-to-Base Voltage	V_{EBO}	-20	-20	-20	V
Collector Current	I_C	-3	-3	-3	A
Emitter Current	I_E	3.5	3.5	3.5	A
Base Current	I_B	-0.5	-0.5	-0.5	A
Transistor Dissipation:					
T_A up to 25°C	P_T	1	1	1	W
T_A above 25°C	P_T	See curve page 300			
T_C up to 25°C (with heat sink)	P_T	7.5	7.5	7.5	W
T_C above 25°C (with heat sink)	P_T	See curve page 300			
Temperature Range:					
Operating (Ambient)	T_A (opr)	-65 to 100			°C
Storage	T_{STG}	-65 to 100			°C

CHARACTERISTICS (At mounting-flange temperature = 25°C.)

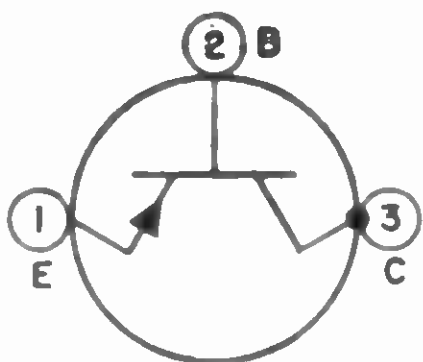
Collector-to-Emitter Voltage:					
$I_C = -50$ mA, $R_{BE} = 0$	V_{CES}	-35 min	-50 min	-60 min	V
$V_{BE} = 1.2$ V, $I_C = -250$ mA	V_{CEV}	-45 min	-60 min	-80 min	V
$I_C = -50$ mA, $I_B = 0$	V_{CEO}	-20 min	-30 min	-40 min	V
Emitter-to-Base Voltage:					
($V_{CE} = -2$ V, $I_C = -400$ mA)	V_{EB}	1.5 max	1.5 max	1.5 max	V
Collector-Cutoff Current:					
$V_{CB} = -1.5$ V, $I_E = 0$	I_{CBO}	-30 max	-30 max	-30 max	μA
$V_{CB} = -45$ V, $I_E = 0$	I_{CBO}	-250 max	—	—	μA
$V_{CB} = -60$ V, $I_E = 0$	I_{CBO}	—	-250 max	—	μA
$V_{CB} = -80$ V, $I_E = 0$	I_{CBO}	—	—	-250 max	μA
Emitter-Cutoff Current ($V_{EB} = -20$ V, $I_C = 0$)	I_{EBO}	-100 max	-100 max	-100 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = -2$ V, $I_C = -400$ mA)	h_{FE}	20 to 60	20 to 60	20 to 60	

CHARACTERISTICS (cont'd)

		2N1183	2N1183A	2N1183B	
Small-Signal Forward-Current Transfer-Ratio Cutoff Frequency ($V_{CB} = -6$ V, $I_B = 1$ mA)	$h_{f\beta}$	0.5 min	0.5 min	0.5 min	MHz
Collector Saturation Resistance ($I_C = -400$ mA, $I_B = -40$ mA)		1.25 max	1.25 max	1.25 max	Ω
Thermal Resistance, Junction-to-Case	θ_{J-C}	10 max	10 max	10 max	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	75 max	75 max	75 max	$^{\circ}\text{C}/\text{W}$

POWER TRANSISTORS

**2N1184
2N1184A
2N1184B**



Ge p-n-p alloy-junction type intended for use in intermediate-power switching and low-frequency amplifier applications in industrial and military equipment. JEDEC TO-8, Outline No.10. See **Mounting Hardware** for desired mounting arrangement. These types are identical with types 2N1183, 2N1183A and 2N1183B, respectively, except for the following item:

CHARACTERISTICS (At mounting-flange temperature = 25°C)

		2N1184	2N1184A	2N1184B
Static Forward-Current Transfer Ratio ($V_{CE} = -2$ V, $I_C = -400$ mA)	h_{FE}	40 to 120	40 to 120	40 to 120

Refer to Chart of Discontinued Transistors

2N1213

Refer to Chart of Discontinued Transistors

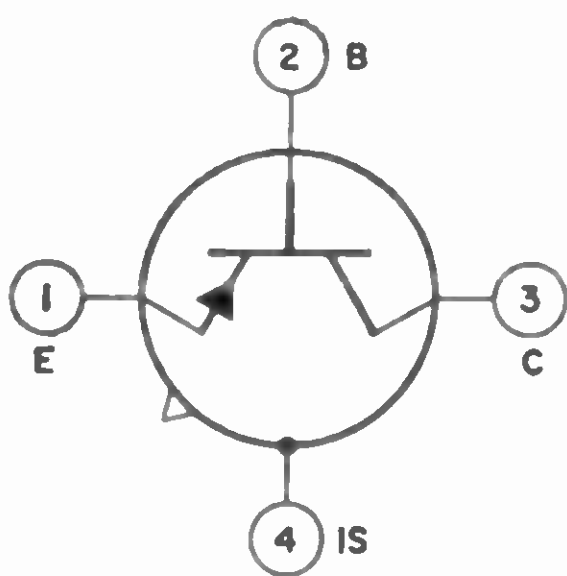
2N1214

Refer to Chart of Discontinued Transistors

2N1215

Refer to Chart of Discontinued Transistors

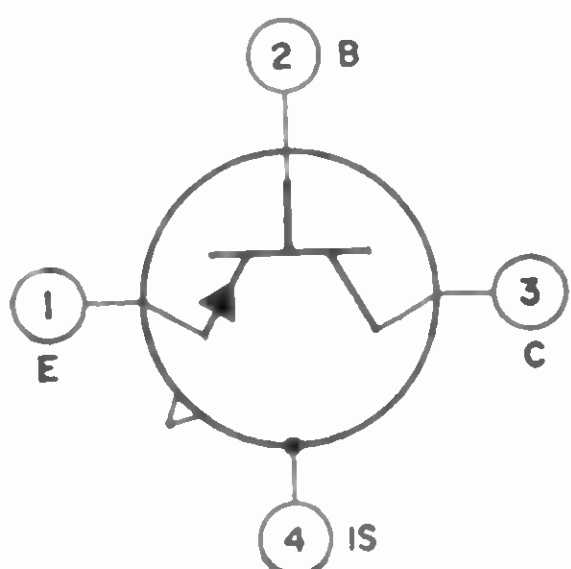
2N1216



TRANSISTOR

2N1224

Ge p-n-p alloy-junction drift-field type used in rf and if amplifier, oscillator, mixer, and converter circuits, and low-level video-amplifier circuits in industrial and military equipment. JEDEC TO-33, Outline No.13. This type is electrically identical with type 2N274.



TRANSISTOR

2N1225

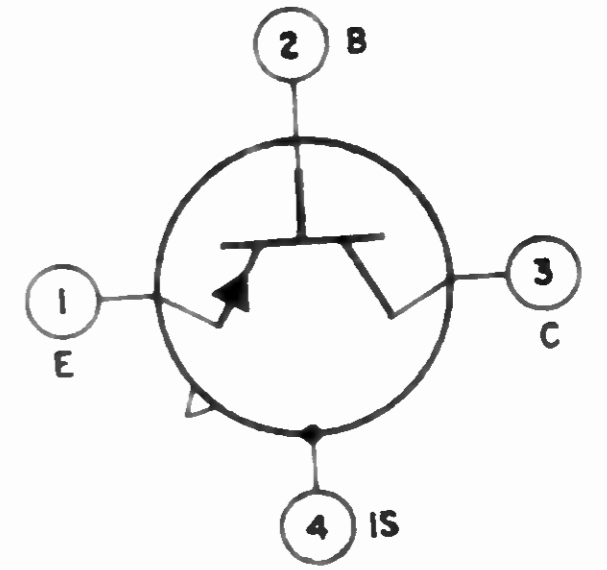
Ge p-n-p alloy-junction drift-field type used in rf and if amplifier, oscillator, mixer, and converter circuits, and low-level video-amplifier circuits in industrial and military equipment. JEDEC TO-33, Outline No.13. This type is electrically identical with type 2N384. For collector-characteristics curves and video-amplifier circuit, refer to type 2N274.

refer to type 2N274.

2N1226

TRANSISTOR

Ge p-n-p alloy-junction drift-field type used in rf and if amplifier, oscillator, mixer, and converter circuits, and low-level video-amplifier circuits in industrial and military equipment. JEDEC TO-33, Outline No.13. This type is identical with type 2N274 except for the following items:



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-60	V
Collector-to-Emitter Voltage ($V_{BE} = 0.5$ V)	V_{CEV}	-60	V

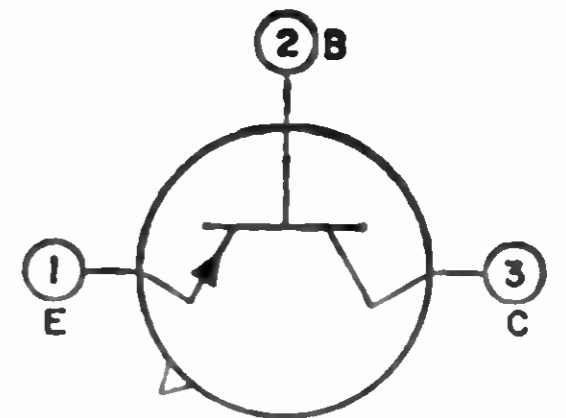
CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = -50 \mu A$, $I_E = 0$)	$V_{(BR)CBO}$	-60 min	V
Collector-to-Emitter Reach-Through Voltage ($V_{EB} = -0.5$ V)	V_{RT}	-60 min	V

2N1300

COMPUTER TRANSISTOR

Ge p-n-p diffused-junction type used in computer applications in commercial and military data-processing equipment. JEDEC TO-5, Outline No.5.

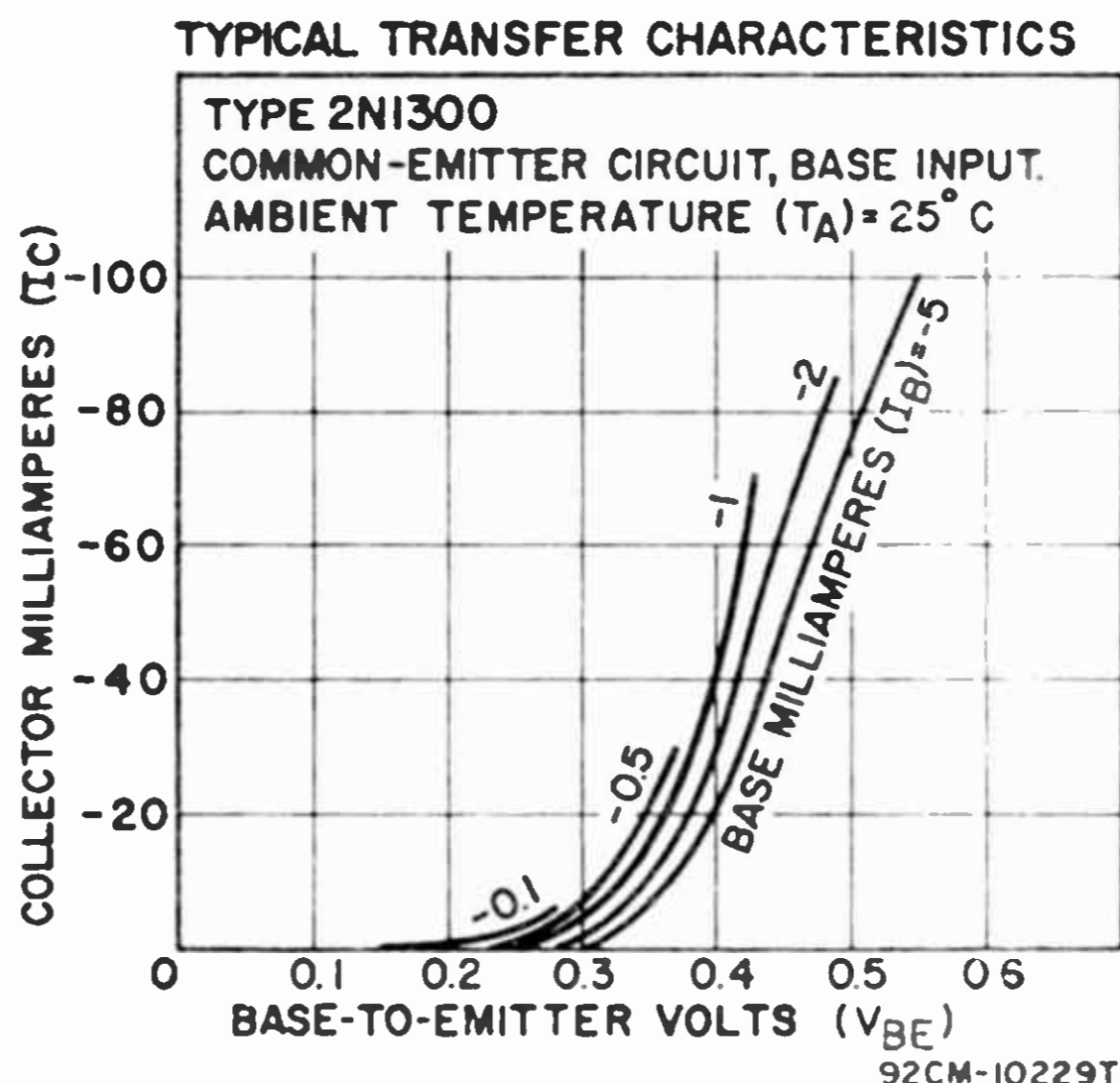


MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-13	V
Collector-to-Emitter Voltage	V_{CEO}	-12	V
Emitter-to-Base Voltage*	V_{EBO}	-1	V
Collector Current	I_C	-100	mA
Emitter Current	I_E	100	mA
Transistor Dissipation:			
$T_A = 25^\circ C$	P_T	150	mW
$T_A = 55^\circ C$	P_T	75	mW
$T_A = 71^\circ C$	P_T	35	mW
Ambient-Temperature Range:			
Operating (T_A) and Storage (T_{STG})		-65 to 85	$^\circ C$
Lead-Soldering Temperature (10 s max)	T_L	225	$^\circ C$

CHARACTERISTICS

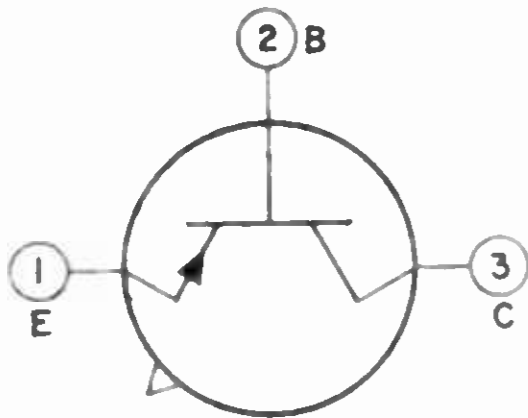
Collector-to-Base Breakdown Voltage ($I_C = -0.02$ mA, $I_E = 0$)	$V_{(BR)CBO}$	-13 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.1$ mA, $I_C = 0$)	$V_{(BR)EBO}$	-1 min	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CERL}$	-12	V
Base-to-Emitter Voltage ($I_C = -10$ mA, $I_B = -0.33$ mA)	V_{BE}	-0.4 max	V



CHARACTERISTICS (cont'd)

Collector-Cutoff Current ($V_{CB} = -6\text{ V}$, $I_E = 0$)	I_{CBO}	-3 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = -0.3\text{ V}$, $I_C = -10\text{ mA}$)	h_{FE}	30 min	
Gain-Bandwidth Product ($V_{CE} = -3\text{ V}$, $I_C = -10\text{ mA}$)	f_T	25 min	MHz
Output Capacitance ($V_{CB} = -6\text{ V}$, $I_E = 0$)	C_{ob}	12 max	pF
Thermal Time Constant	τ (thermal)	10	ms
Total Stored Charge ($I_C = -10\text{ mA}$, $I_B = -1\text{ mA}$)	Q_S	400 max	pC
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	400 max	$^{\circ}\text{C}/\text{W}$

* This rating may be exceeded and the emitter-to-base junction operated in the breakdown condition provided the emitter dissipation is limited to 30 milliwatts at 25°C. For ambient temperatures above 25°C, the dissipation must be reduced by 0.5 milliwatts per °C.



COMPUTER TRANSISTOR 2N1301

Ge p-n-p diffused-junction type used in computer applications in data-processing equipment. JEDEC TO-5, Outline No.5. This type is identical with type 2N1300 except for the following items:

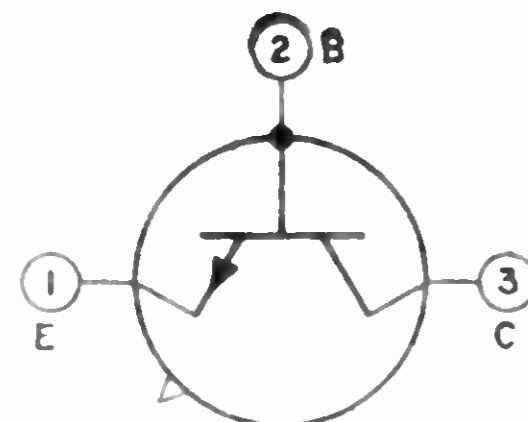
MAXIMUM RATINGS

Emitter-to-Base Voltage*	V_{EBO}	-4	V
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CHARACTERISTICS

Emitter-to-Base Breakdown Voltage ($I_E = 0.1\text{ mA}$, $I_C = 0$)	$V_{(BR)EBO}$	-4 min	V
Base-to-Emitter Voltage ($I_C = -40\text{ mA}$, $I_B = -1\text{ mA}$)	V_{BE}	-0.6 max	V
Static Forward-Current Transfer Ratio: $V_{CE} = -0.3\text{ V}$, $I_C = -10\text{ mA}$	h_{FE}	30 min	
$V_{CE} = -0.5\text{ V}$, $I_C = -40\text{ mA}$	h_{FE}	40 min	
Gain-Bandwidth Product ($V_{CE} = -3\text{ V}$, $I_C = -10\text{ mA}$)	f_T	35 min	MHz
Total Stored Charge: $I_C = -10\text{ mA}$, $I_B = -1\text{ mA}$	Q_S	325 max	pC
$I_C = -40\text{ mA}$, $I_B = -2\text{ mA}$	Q_S	800 max	pC

* This rating may be exceeded and the emitter-to-base junction operated in the breakdown condition provided the emitter dissipation is limited to 30 milliwatts at 25°C. For ambient temperatures above 25°C, reduce the dissipation by 0.5 milliwatts per °C.



COMPUTER TRANSISTOR 2N1302

Ge n-p-n alloy-junction type used in medium-speed switching applications in commercial and military data-processing equipment. The n-p-n construction permits complementary operation with a matching p-n-p type, such as the 2N1303. JEDEC TO-5, Outline No.5.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	25	V
Emitter-to-Base Voltage	V_{EBO}	25	V
Collector Current	I_C	0.3	A
Transistor Dissipation: T_A up to 25°C	P_T	150	mW
T_A above 25°C	P_T	See curve page 300	
Temperature Range: Operating (Junction)	T_J (opr)	-65 to 85	$^{\circ}\text{C}$
Storage	T_{STG}	-65 to 100	$^{\circ}\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	230	$^{\circ}\text{C}$

CHARACTERISTICS

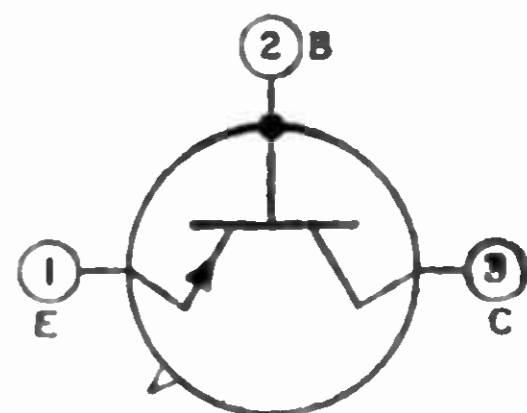
Collector-to-Emitter Saturation Voltage ($I_B = 0.5\text{ mA}$, $I_C = 10\text{ mA}$)	$V_{CE(sat)}$	0.2 max	V
Base-to-Emitter Voltage ($I_B = 0.5\text{ mA}$, $I_C = 10\text{ mA}$) ..	V_{BE}	0.15 to 0.4	V
Collector-to-Emitter Reach-Through Voltage	V_{RT}	25 min	V
Collector-Cutoff Current ($V_{CB} = 25\text{ V}$, $I_E = 0$)	I_{CBO}	6 max	μA
Emitter-Cutoff Current ($V_{EB} = 25\text{ V}$, $I_C = 0$)	I_{EBO}	6 max	μA
Static Forward-Current Transfer Ratio: $V_{CE} = 1\text{ V}$, $I_C = 10\text{ mA}$	h_{FE}	20 min	
$V_{CE} = 0.35\text{ V}$, $I_C = 200\text{ mA}$	h_{FE}	10 min	

CHARACTERISTICS (cont'd)

Small-Signal Forward-Current Transfer-Ratio Cutoff Frequency ($V_{CB} = 5 \text{ V}$, $I_E = -1 \text{ mA}$)	f_{hfb}	3 min	MHz
Output Capacitance ($V_{CB} = 5 \text{ V}$, $I_E = 0$)	C_{obo}	20 max	pF

2N1303 COMPUTER TRANSISTOR

Ge p-n-p alloy-junction type used in medium-speed switching applications in data-processing equipment. The 2N1303 is the p-n-p complement of the n-p-n type 2N1302. JEDEC TO-5, Outline No.5.

**MAXIMUM RATINGS**

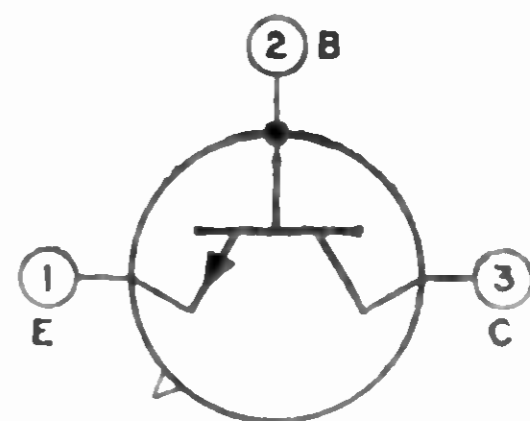
Collector-to-Base Voltage	V_{CBO}	-30	V
Emitter-to-Base Voltage	V_{EBO}	-25	V
Collector Current	I_C	-0.3	A
Transistor Dissipation:			
T_A up to 25°C	P_T	150	mW
T_A above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 85	$^\circ\text{C}$
Storage	T_{STG}	-65 to 100	$^\circ\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	230	$^\circ\text{C}$

CHARACTERISTICS

Collector-to-Emitter Saturation Voltage ($I_B = -0.5 \text{ mA}$, $I_C = -10 \text{ mA}$)	$V_{CE(\text{sat})}$	-0.2 max	V
Base-to-Emitter Voltage ($I_B = -0.5 \text{ mA}$, $I_C = -10 \text{ mA}$)	V_{BE}	-0.15 to -0.4	V
Collector-to-Emitter Reach-Through Voltage	V_{RT}	-25 min	V
Collector-Cutoff Current ($V_{CB} = -25 \text{ V}$, $I_E = 0$)	I_{CBO}	-6 max	μA
Emitter-Cutoff Current ($V_{EB} = -25 \text{ V}$, $I_C = 0$)	I_{EBO}	-6 max	μA
Static Forward-Current Transfer Ratio:			
$V_{CE} = -1 \text{ V}$, $I_C = -10 \text{ mA}$	h_{FE}	20 min	
$V_{CE} = -0.35 \text{ V}$, $I_C = -200 \text{ mA}$	h_{FE}	10 min	
Small-Signal Forward-Current Transfer-Ratio Cutoff Frequency ($V_{CB} = -5 \text{ V}$, $I_E = 1 \text{ mA}$)	f_{hfb}	3 min	MHz
Output Capacitance ($V_{CB} = -5 \text{ V}$, $I_E = 0$)	C_{obo}	20 max	pF

2N1304 COMPUTER TRANSISTOR

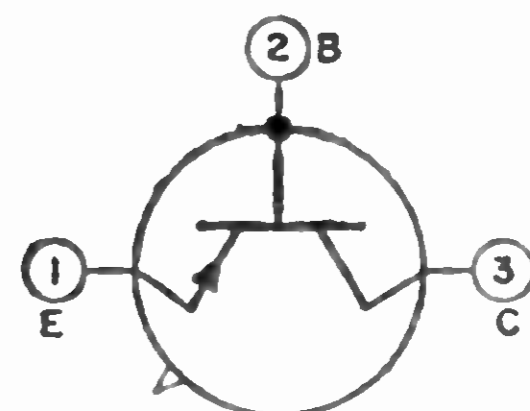
Ge n-p-n alloy-junction type used in medium-speed switching applications in data-processing equipment. The n-p-n construction permits complementary operation with a matching p-n-p type, such as the 2N1305. JEDEC TO-5, Outline No.5. This type is identical with type 2N1302 except for the following items:

**CHARACTERISTICS**

Collector-to-Emitter Saturation Voltage ($I_B = 0.25 \text{ mA}$, $I_C = 10 \text{ mA}$)	$V_{CE(\text{sat})}$	0.2 max	V
Base-to-Emitter Voltage ($I_B = 0.5 \text{ mA}$, $I_C = 10 \text{ mA}$)	V_{BE}	0.15 to 0.35	V
Collector-to-Emitter Reach-Through Voltage	V_{RT}	20 min	V
Static Forward-Current Transfer Ratio:			
$V_{CE} = 1 \text{ V}$, $I_C = 10 \text{ mA}$	h_{FE}	40 to 200	
$V_{CE} = 0.35 \text{ V}$, $I_C = 200 \text{ mA}$	h_{FE}	15 min	
Small-Signal Forward-Current Transfer-Ratio Cutoff Frequency ($V_{CB} = 5 \text{ V}$, $I_E = -1 \text{ mA}$)	f_{hfb}	5 min	MHz

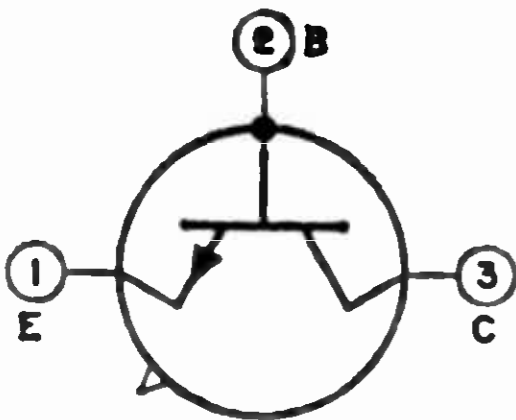
2N1305 COMPUTER TRANSISTOR

Ge p-n-p alloy-junction type used in medium-speed switching applications in data-processing equipment. The 2N1305 is the p-n-p complement of the n-p-n type 2N1304. JEDEC TO-5, Outline No.5. This type is identical with type 2N1303 except for the following items:



CHARACTERISTICS

Collector-to-Emitter Saturation Voltage ($I_B = -25$ mA, $I_C = -10$ mA)	$V_{CE(sat)}$	-0.2 max	V
Base-to-Emitter Voltage ($I_B = -0.5$ mA, $I_C = -10$ mA)	V_{BE}	-0.15 to -0.35	V
Collector-to-Emitter Reach-Through Voltage	V_{RT}	-20 min	V
Static Forward-Current Transfer Ratio:			
$V_{CE} = -1$ V, $I_C = -10$ mA	h_{FE}	40 to 200	
$V_{CE} = -0.35$ V, $I_C = -200$ mA	h_{FE}	15 min	
Small-Signal Forward-Current Transfer-Ratio Cutoff Frequency ($V_{CB} = -5$ V, $I_E = 1$ mA)	f_{hfb}	5 min	MHz



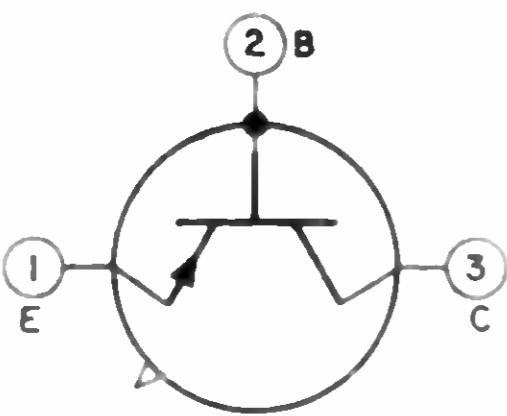
COMPUTER TRANSISTOR

2N1306

Ge n-p-n alloy-junction type used in medium-speed switching applications in data processing equipment. The 2N1306 is the n-p-n complement of the p-n-p type 2N1307. JEDEC TO-5, Outline No.5. This type is identical with type 2N1302 except for the following items:

CHARACTERISTICS

Collector-to-Emitter Saturation Voltage ($I_B = 0.17$ mA, $I_C = 10$ mA)	$V_{CE(sat)}$	0.2 max	V
Base-to-Emitter Voltage ($I_B = 0.5$ mA, $I_C = 10$ mA)	V_{BE}	0.15 to 0.35	V
Collector-to-Emitter Reach-Through Voltage	V_{RT}	15 min	V
Static Forward-Current Transfer Ratio:			
$V_{CE} = 1$ V, $I_C = 10$ mA	h_{FE}	60 to 300	
$V_{CE} = 0.35$ V, $I_C = 200$ mA	h_{FE}	20 min	
Small-Signal Forward-Current Transfer-Ratio Cutoff Frequency ($V_{CB} = 5$ V, $I_E = -1$ mA)	f_{hfb}	10 min	MHz



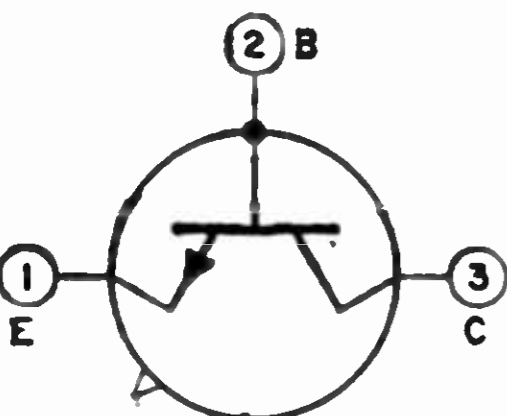
COMPUTER TRANSISTOR

2N1307

Ge p-n-p alloy-junction type used in medium-speed switching applications in data-processing equipment. The 2N1307 is the p-n-p complement of the n-p-n type 2N1306. JEDEC TO-5, Outline No.5. This type is identical with type 2N1303 except for the following items:

CHARACTERISTICS

Collector-to-Emitter Saturation Voltage ($I_B = -0.17$ mA, $I_C = -10$ mA)	$V_{CE(sat)}$	-0.2 max	V
Base-to-Emitter Voltage ($I_B = -0.5$ mA, $I_C = -10$ mA)	V_{BE}	-0.15 to -0.35	V
Collector-to-Emitter Reach-Through Voltage	V_{RT}	-15 min	V
Static Forward-Current Transfer Ratio:			
$V_{CE} = -1$ V, $I_C = -10$ mA	h_{FE}	60 to 300	
$V_{CE} = -0.35$ V, $I_C = -200$ mA	h_{FE}	20 min	
Small-Signal Forward-Current Transfer-Ratio Cutoff Frequency ($V_{CB} = -5$ V, $I_E = 1$ mA)	f_{hfb}	10 min	MHz



COMPUTER TRANSISTOR

2N1308

Ge n-p-n alloy-junction type used in medium-speed switching applications in data processing equipment. The 2N1308 is the n-p-n complement of the p-n-p type 2N1309. JEDEC TO-5, Outline No.5. This type is identical with type 2N1302 except for the following items:

CHARACTERISTICS

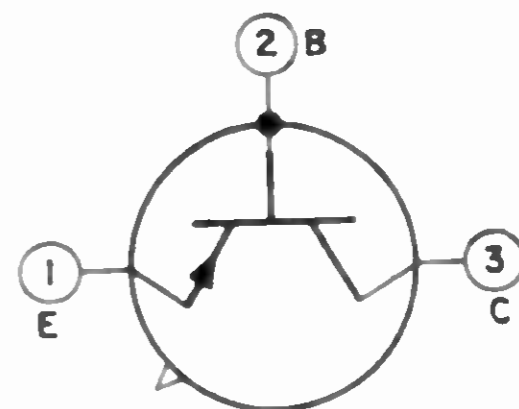
Collector-to-Emitter Saturation Voltage ($I_B = 0.13$ mA, $I_C = 10$ mA)	$V_{CE(sat)}$	0.2 max	V
Base-to-Emitter Voltage ($I_B = 0.5$ mA, $I_C = 10$ mA)	V_{BE}	0.15 to 0.35	V
Collector-to-Emitter Reach-Through Voltage	V_{RT}	15 min	V
Static Forward-Current Transfer Ratio:			
$V_{CE} = 1$ V, $I_C = 10$ mA	h_{FE}	80 min	
$V_{CE} = 0.35$ V, $I_C = 200$ mA	h_{FE}	20 min	

CHARACTERISTICS (cont'd)

Small-Signal Forward-Current Transfer-Ratio Cutoff Frequency ($V_{CB} = 5 \text{ V}$, $I_E = -1 \text{ mA}$) f_{hfb} 15 MHz

2N1309 COMPUTER TRANSISTOR

Ge p-n-p alloy-junction type used in medium-speed switching applications in data-processing equipment. The 2N1309 is the p-n-p complement of the n-p-n type 2N1308. JEDEC TO-5, Outline No.5. This type is identical with type 2N1303 except for the following items:



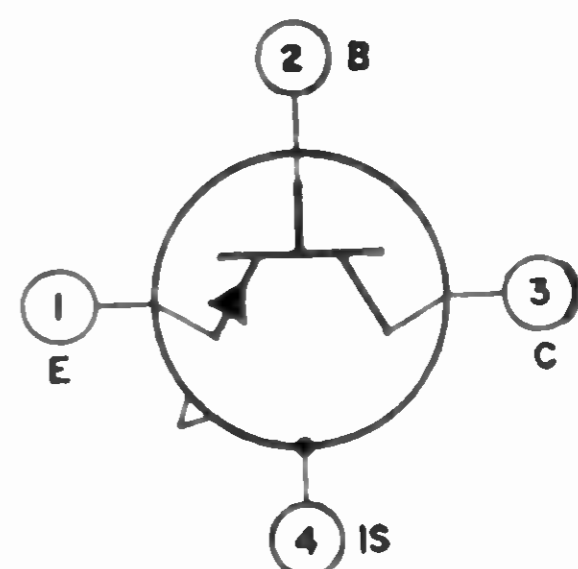
CHARACTERISTICS

Collector-to-Emitter Saturation Voltage ($I_B = -0.13 \text{ mA}$, $I_C = -10 \text{ mA}$)	$V_{CE(sat)}$	-0.2 max	V
Base-to-Emitter Voltage ($I_B = -0.5 \text{ mA}$, $I_C = -10 \text{ mA}$)	V_{BE}	-0.15 to -0.35	V
Collector-to-Emitter Reach-Through Voltage	V_{RT}	-15 min	V
Static Forward-Current Transfer Ratio:			
$V_{CE} = -1 \text{ V}$, $I_C = -10 \text{ mA}$	h_{FE}	80 min	
$V_{CE} = -0.35 \text{ V}$, $I_C = -200 \text{ mA}$	h_{FE}	20 min	
Small-Signal Forward-Current Transfer-Ratio Cutoff Frequency ($V_{CB} = -5 \text{ V}$, $I_E = 1 \text{ mA}$)	f_{hfb}	15 min	MHz

- 2N1319** Refer to Chart of Discontinued Transistors
- 2N1358** Refer to Chart of Discontinued Transistors
- 2N1384** Refer to Chart of Discontinued Transistors

2N1395 TRANSISTOR

Ge p-n-p alloy-junction drift-field type used in rf and if amplifier, oscillator, mixer, and converter circuits, and low-level video-amplifier circuits in industrial and military equipment. JEDEC TO-33, Outline No.13. This type is identical with type 2N274 except for the following item:

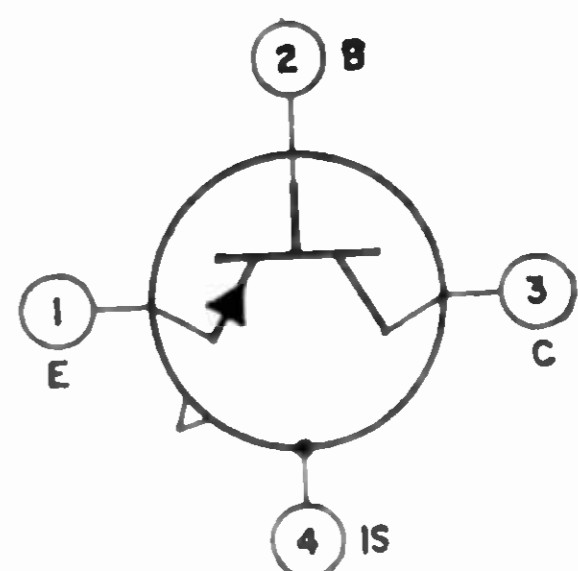


CHARACTERISTICS

Small-Signal Forward-Current Transfer Ratio ($V_{CE} = -12 \text{ V}$, $I_E = 1.5 \text{ mA}$, $f = 1 \text{ kHz}$) h_{fe} 50 to 175

2N1396 TRANSISTOR

Ge p-n-p alloy-junction drift-field type used in rf and if amplifier, oscillator, mixer, and converter circuits, and low-level video-amplifier circuits in industrial and military equipment. JEDEC TO-33, Outline No.13. This type is identical with type 2N384 except for the following item:

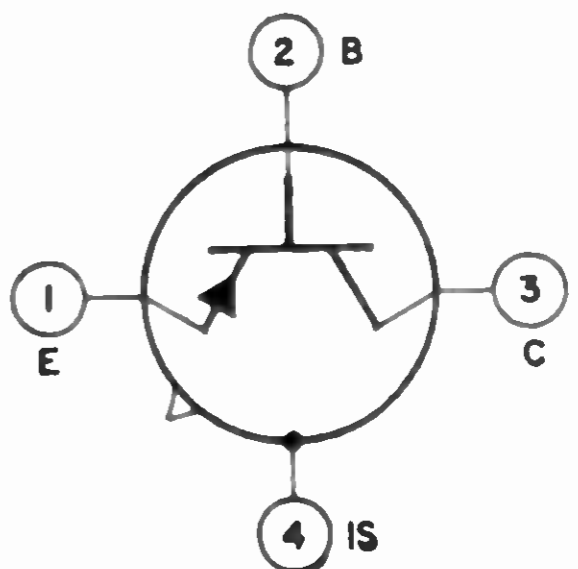


CHARACTERISTICS

Small-Signal Forward-Current Transfer Ratio ($V_{CE} = -12 \text{ V}$, $I_E = 1.5 \text{ mA}$, $f = 1 \text{ kHz}$) h_{fe} 50 to 175

2N1397 TRANSISTOR

Ge p-n-p alloy-junction drift-field type used in rf and if amplifier, oscillator, mixer, and converter circuits, and low-level video-amplifier circuits in industrial and military equipment. JEDEC TO-33, Outline No.13. This type is identical with type 2N1023 except for the following item:



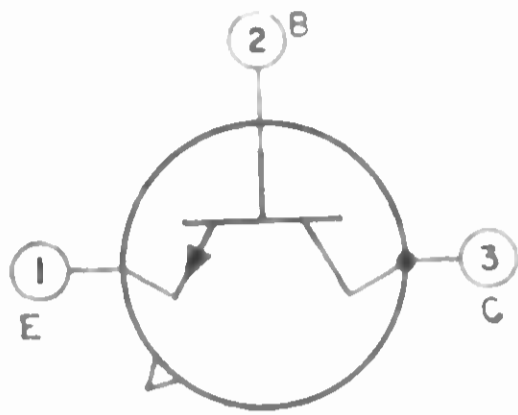
CHARACTERISTICS

Small-Signal Forward-Current Transfer Ratio
 ($V_{CE} = -12\text{ V}$, $I_E = 1.5\text{ mA}$, $f = 1\text{ kHz}$) h_{fe} 50 to 175

- Refer to Chart of Discontinued Transistors **2N1412**
- Refer to Chart of Discontinued Transistors **2N1425**
- Refer to Chart of Discontinued Transistors **2N1426**
- Refer to Chart of Discontinued Transistors **2N1450**

POWER TRANSISTOR

2N1479



Si n-p-n diffused-junction type used in power switching circuits such as dc-to-dc converters, inverters, choppers, solenoid and relay controls; in oscillators, regulators, and pulse amplifier circuits; and as class A and class B push-pull audio and servo amplifiers in industrial and military equipment. JEDEC TO-5, Outline No.5.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	60	V
Collector-to-Emitter Voltage: $V_{BE} = -1.5\text{ V}$	V_{CEV}	60	V
Base open (sustaining voltage)	$V_{CEO}(\text{sus})$	40	V
Emitter-to-Base Voltage	V_{EBO}	12	V
Collector Current	I_C	1.5	A
Emitter Current	I_E	-1.75	A
Base Current	I_B	1	A
Transistor Dissipation: T_C up to 25°C	P_T	5	W
T_C above 25°C	P_T	See curve page 300	
Temperature Range: Operating (T_C) and Storage (T_{STG})		-65 to 200	$^\circ\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	255	$^\circ\text{C}$

CHARACTERISTICS (At case temperature = 25°C)

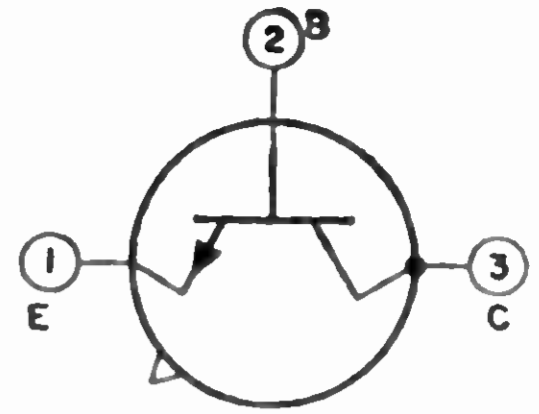
Collector-to-Emitter Sustaining Voltage ($I_C = 50\text{ mA}$, $I_B = 0$)	$V_{CEO}(\text{sus})$	40 min	V
Collector-to-Emitter Voltage ($V_{BE} = -1.5$, $I_C = 0.25\text{ mA}$)	V_{CEV}	60 min	V
Base-to-Emitter Voltage ($V_{CE} = 4\text{ V}$, $I_C = 200\text{ mA}$) ...	V_{BE}	3 max	V
Collector-Cutoff Current: $V_{CB} = 30\text{ V}$, $I_E = 0$, $T_C = 25^\circ\text{C}$	I_{CBO}	10 max	μA
$V_{CB} = 30\text{ V}$, $I_E = 0$, $T_C = 150^\circ\text{C}$	I_{CBO}	500 max	μA
Emitter-Cutoff Current ($V_{EB} = 12\text{ V}$, $I_C = 0$)	I_{EBO}	10 max	μA
Collector-to-Emitter Saturation Resistance ($I_C = 200\text{ mA}$, $I_B = 20\text{ mA}$)	$r_{CE}(\text{sat})$	7 max	Ω
Static Forward-Current Transfer Ratio ($V_{CE} = 4\text{ V}$, $I_C = 200\text{ mA}$)	h_{FE}	20 to 60	
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 4\text{ V}$, $I_C = 5\text{ mA}$, $f = 1\text{ kHz}$)	h_{fe}	50	
Small-Signal Forward-Current Transfer-Ratio Cutoff Frequency ($V_{CB} = 28\text{ V}$, $I_C = 5\text{ mA}$)	f_{hfb}	50 max	kHz
Gain-Bandwidth Product	f_T	1.5	MHz
Output Capacitance ($V_{CB} = 40\text{ V}$, $I_C = 0$, $f = 1\text{ kHz}$)	C_{ob0}	150	pF
Thermal Time Constant	$\tau(\text{thermal})$	10	ms
Thermal Resistance, Junction-to-Case	θ_{J-C}	35 max	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	200 max	$^\circ\text{C/W}$

**TYPICAL OPERATION IN POWER-SWITCHING CIRCUIT
 (At case temperature = 25°C)**

DC Supply Voltage	V_{CC}	12	V
DC Base-Bias Voltage		-8.5	V
Generator Resistance	R_G	50	Ω
"On" DC Collector Current	I_C	200	mA
"Turn-On" Base Current	I_{B1}	20	mA
"Turn-Off" Base Current	I_{B2}	-8.5	mA
Delay Time	t_d	0.2	μs
Rise Time	t_r	1	μs
Storage Time	t_s	0.6	μs
Fall Time	t_f	1	μs

2N1480 POWER TRANSISTOR

Si n-p-n diffused-junction type used in power switching circuits such as dc-to-dc converters, inverters, choppers, solenoid and relay controls; in oscillators, regulators, and pulse amplifier circuits; and as class A and class B push-pull audio and servo amplifiers in industrial and military equipment. JEDEC TO-5, Outline No.5. This type is identical with type 2N1479 except for the following items:



MAXIMUM RATINGS

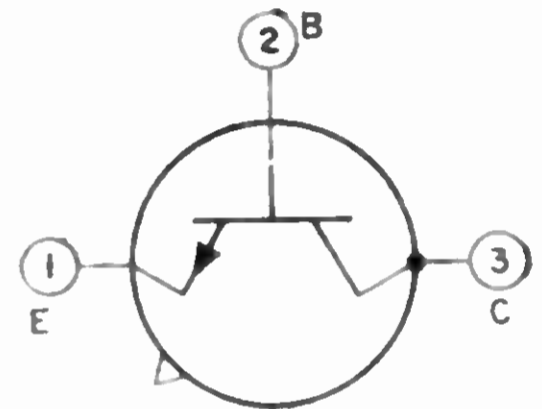
Collector-to-Base Voltage	V_{CB0}	100	V
Collector-to-Emitter Voltage: $V_{BE} = -1.5$ V	V_{CEV}	100	V
Base open (sustaining voltage)	$V_{CEO(sus)}$	55	V

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_C = 50$ mA, $I_B = 0$)	$V_{CEO(sus)}$	55 min	V
Collector-to-Emitter Voltage ($V_{BE} = -1.5$ V, $I_C = 0.25$ mA)	V_{CEV}	100 min	V

2N1481 POWER TRANSISTOR

Si n-p-n diffused-junction type used in power switching circuits such as dc-to-dc converters, inverters, choppers, solenoid and relay controls; in oscillators, regulators, and pulse amplifier circuits; and as class A and class B push-pull audio and servo amplifiers in industrial and military equipment. JEDEC TO-5, Outline No.5. This type is identical with type 2N1479 except for the following items:

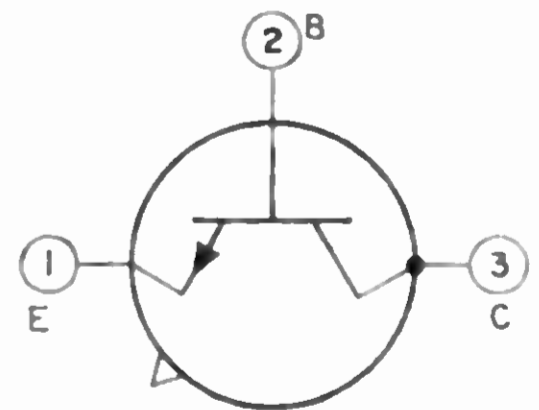


CHARACTERISTICS (At case temperature = 25°C)

Static Forward-Current Transfer Ratio ($V_{CE} = 4$ V, $I_C = 200$ mA)	h_{FE}	35 to 100	
Collector-to-Emitter Saturation Resistance ($I_C = 200$ mA, $I_B = 10$ mA)	$r_{CE(sat)}$	7 max	Ω

2N1482 POWER TRANSISTOR

Si n-p-n diffused-junction type used in power switching circuits such as dc-to-dc converters, inverters, choppers, solenoid and relay controls; in oscillators, regulators, and pulse amplifier circuits; and as class A and class B push-pull audio and servo amplifiers in industrial and military equipment. JEDEC TO-5, Outline No.5. This type is identical with type 2N1479 except for the following items:



MAXIMUM RATINGS

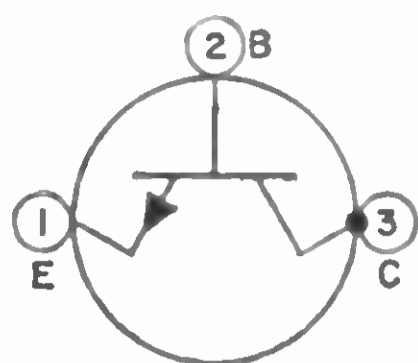
Collector-to-Base Voltage	V_{CB0}	100	V
Collector-to-Emitter Voltage: $V_{BE} = -1.5$ V	V_{CEV}	100	V
Base open (sustaining voltage)	$V_{CEO(sus)}$	55	V

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_C = 50$ mA, $I_B = 0$)	$V_{CEO(sus)}$	55 min	V
Collector-to-Emitter Voltage ($V_{BE} = -1.5$ V, $I_C = 0.25$ mA)	V_{CEV}	100 min	V
Static Forward-Current Transfer Ratio ($V_{CE} = 4$ V, $I_C = 200$ mA)	h_{FE}	35 to 100	
Collector-to-Emitter Saturation Resistance ($I_C = 200$ mA, $I_B = 10$ mA)	$r_{CE(sat)}$	7 max	Ω

POWER TRANSISTOR

2N1483



Si n-p-n diffused-junction type used in dc-to-dc converters, inverters, choppers, dc and servo amplifiers, relay- and solenoid-actuating circuits in industrial and military equipment. JEDEC TO-8, Outline No.10. See Mounting Hardware for desired mounting arrangement.

MAXIMUM RATINGS

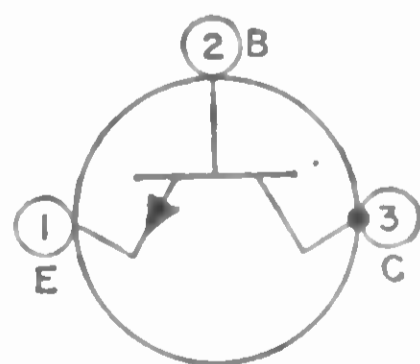
Collector-to-Base Voltage	V_{CBO}	60	V
Collector-to-Emitter Voltage:			
$V_{BE} = -1.5$ V	V_{CEV}	60	V
Base open (sustaining voltage)	$V_{CEO(sus)}$	40	V
Emitter-to-Base Voltage	V_{EBO}	12	V
Collector Current	I_C	3	A
Emitter Current	I_E	-3.5	A
Base Current	I_B	1.5	A
Transistor Dissipation:			
T_c up to 25°C	P_T	25	W
T_c above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (T_c) and Storage (T_{STG})		-65 to 200	°C
Pin-Soldering Temperature (10 s max)	T_P	235	°C

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_C = 100$ mA, $I_B = 0$)	$V_{CEO(sus)}$	40 min	V
Collector-to-Emitter Voltage ($V_{BE} = -1.5$ V, $I_C = 0.25$ mA)	V_{CEV}	60 min	V
Base-to-Emitter Voltage ($V_{CE} = 4$ V, $I_C = 750$ mA)	V_{BE}	3.5 max	V
Collector-Cutoff Current:			
$V_{CB} = 30$ V, $I_E = 0$, $T_A = 25^\circ C$	I_{CBO}	15 max	μA
$V_{CB} = 30$ V, $I_E = 0$, $T_A = 150^\circ C$	I_{CBO}	750 max	μA
Emitter-Cutoff Current ($V_{EB} = 12$ V, $I_C = 0$)	I_{EBO}	15 max	μA
Collector-to-Emitter Saturation Resistance ($I_C = 750$ mA, $I_B = 75$ mA)	$r_{CE(sat)}$	2.67 max	Ω
Static Forward-Current Transfer Ratio ($V_{CE} = 4$ V, $I_C = 750$ mA)	h_{FE}	20 to 60	
Small-Signal Forward-Current Transfer-Ratio Cutoff Frequency ($V_{CB} = 28$ V, $I_C = 5$ mA)	f_{hfb}	1.25	MHz
Output Capacitance ($V_{CB} = 40$ V, $I_E = 0$)	C_{obo}	175	pF
Thermal Time Constant	τ (thermal)	10	ms
Thermal Resistance, Junction-to-Case	θ_{J-C}	7 max	°C/W
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	100 max	°C/W

POWER TRANSISTOR

2N1484



Si n-p-n diffused-junction type used in dc-to-dc converters, inverters, choppers, dc and servo amplifiers, relay- and solenoid-actuating circuits in industrial and military equipment. JEDEC TO-8, Outline No.10. See Mounting Hardware for desired mounting arrangement. This type is identical with type 2N1483 except for the

following items:

MAXIMUM RATINGS

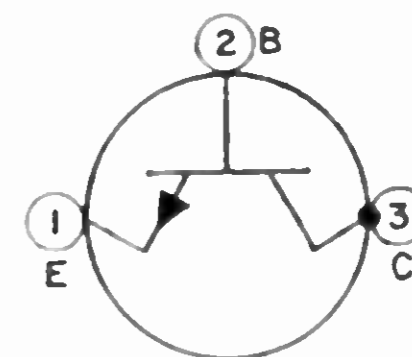
Collector-to-Base Voltage	V_{CBO}	100	V
Collector-to-Emitter Voltage:			
$V_{BE} = -1.5$ V	V_{CEV}	100	V
Base open (sustaining voltage)	$V_{CEO(sus)}$	55	V

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_C = 100$ mA, $I_B = 0$)	$V_{CEO(sus)}$	55 min	V
Collector-to-Emitter Voltage ($V_{BE} = -1.5$ V, $I_C = 0.25$ mA)	V_{CEV}	100 min	V

2N1485 POWER TRANSISTOR

Si n-p-n diffused-junction type used in dc-to-dc converters, inverters, choppers, dc and servo amplifiers, relay- and solenoid-actuating circuits in industrial and military equipment. JEDEC TO-8, Outline No.10. See **Mounting Hardware** for desired mounting arrangement. This type is identical with type 2N1483 except for the following items:

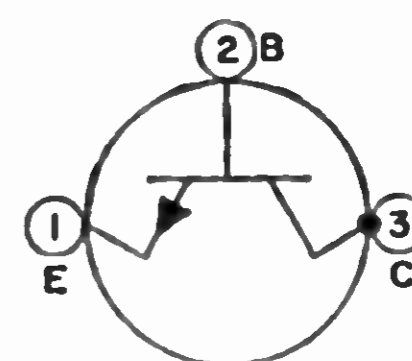


CHARACTERISTICS (At case temperature = 25°C)

Base-to-Emitter Voltage ($V_{CE} = 4\text{ V}$, $I_C = 750\text{ mA}$)	V_{BE}	2.5 max	V
Static Forward-Current Transfer Ratio ($V_{CE} = 4\text{ V}$, $I_C = 750\text{ mA}$)	h_{FE}	35 to 100	
Collector-to-Emitter Saturation Resistance ($I_C = 750\text{ mA}$, $I_B = 40\text{ mA}$)	$r_{CE(sat)}$	1 max	Ω

2N1486 POWER TRANSISTOR

Si n-p-n diffused-junction type used in dc-to-dc converters, inverters, choppers, dc and servo amplifiers, relay- and solenoid-actuating circuits in industrial and military equipment. JEDEC TO-8, Outline No.10. See **Mounting Hardware** for desired mounting arrangement. This type is identical with type 2N1483 except for the following items:



MAXIMUM RATINGS

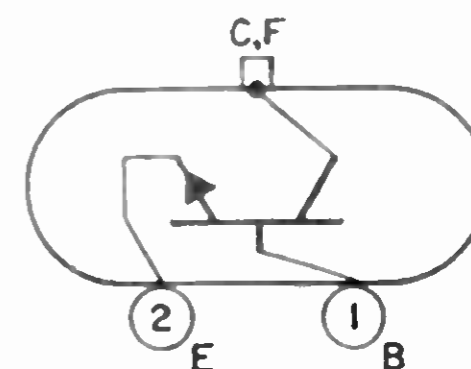
Collector-to-Base Voltage	V_{CBO}	100	V
Collector-to-Emitter Voltage: $V_{BE} = -1.5\text{ V}$	V_{CEV}	100	V
Base open (sustaining voltage)	$V_{CEO(sus)}$	55	V

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CEO(sus)}$	55 min	V
Collector-to-Emitter Voltage ($V_{BE} = -1.5\text{ V}$, $I_C = 0.25\text{ mA}$)	V_{CEV}	100 min	V
Base-to-Emitter Voltage ($V_{CE} = 4\text{ V}$, $I_C = 750\text{ mA}$)	V_{BE}	2.5 max	V
Static Forward-Current Transfer Ratio ($V_{CE} = 4\text{ V}$, $I_C = 750\text{ mA}$)	h_{FE}	35 to 100	
Collector-to-Emitter Saturation Resistance ($I_C = 750\text{ mA}$, $I_B = 40\text{ mA}$)	$r_{CE(sat)}$	1 max	Ω

2N1487 POWER TRANSISTOR

Si n-p-n diffused-junction type used in dc-to-dc converters, inverters, choppers, voltage and current regulators, dc and servo amplifiers, relay- and solenoid-actuating circuits. JEDEC TO-3, Outline No.2. See **Mounting Hardware** for desired mounting arrangement.



MAXIMUM RATINGS

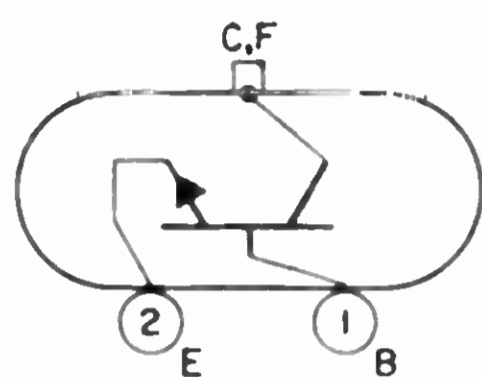
Collector-to-Base Voltage	V_{CBO}	60	V
Collector-to-Emitter Voltage: $V_{BE} = -1.5\text{ V}$	V_{CEV}	60	V
Base open (sustaining voltage)	$V_{CEO(sus)}$	40	V
Emitter-to-Base Voltage	V_{EBO}	10	V
Collector Current	I_C	6	A
Emitter Current	I_E	-8	A
Base Current	I_B	3	A
Transistor Dissipation: T_{MF} at 25°C	P_T	75	W
T_{MF} above 25°C	P_T	See curve page 300	
Temperature Range: Operating (T_{MF}) and Storage (T_{STG})		-65 to 200	°C

CHARACTERISTICS (At mounting-flange temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_C = 100$ mA, $I_B = 0$)	$V_{CE0(sus)}$	40 min	V
Collector-to-Emitter Voltage ($V_{BE} = -1.5$ V, $I_C = 0.5$ mA)	V_{CEV}	60 min	V
Base-to-Emitter Saturation Voltage ($V_{CE} = 4$ V, $I_C = 1.5$ A)	V_{BE}	3.5 max	V
Collector-Cutoff Current: $V_{CB} = 30$ V, $I_E = 0$, $T_A = 25^\circ\text{C}$	I_{CBO}	25 max	μA
$V_{CB} = 30$ V, $I_E = 0$, $T_A = 150^\circ\text{C}$	I_{CBO}	1000 max	μA
Emitter-Cutoff Current ($V_{EB} = 10$ V, $I_C = 0$)	I_{EBO}	25 max	μA
Collector-to-Emitter Saturation Resistance ($I_C = 1.5$ A, $I_B = 300$ mA)	$r_{CE(sat)}$	2 max	Ω
Static Forward-Current Transfer Ratio ($V_{CE} = 4$ V, $I_C = 1.5$ A)	h_{FE}	15 to 45	
Small-Signal Forward-Current Transfer-Ratio Cutoff Frequency ($V_{CB} = 12$ V, $I_C = 100$ mA)	f_{hfb}	1	MHz
Output Capacitance ($V_{CB} = 40$ V, $I_E = 0$)	C_{obo}	200	pF
Thermal Time Constant	$\tau(\text{thermal})$	12	ms
Thermal Resistance, Junction-to-Mounting Flange	Θ_{J-MF}	2.33 max	$^\circ\text{C/W}$

POWER TRANSISTOR

2N1488



Si n-p-n diffused-junction type used in dc-to-dc converters, inverters, choppers, voltage and current regulators, dc and servo amplifiers, relay- and solenoid-actuating circuits. JEDEC TO-3, Outline No.2. See Mounting Hardware for desired mounting arrangement. This type is identical with type 2N1487 except for the

following items:

MAXIMUM RATINGS

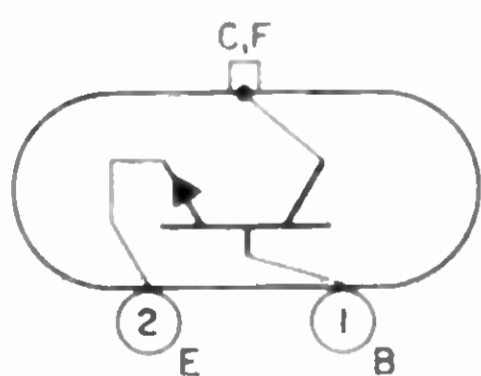
Collector-to-Base Voltage	V_{CBO}	100	V
Collector-to-Emitter Voltage: $V_{BE} = -1.5$ V	V_{CEV}	100	V
Base open (sustaining voltage)	$V_{CE0(sus)}$	55	V

CHARACTERISTICS (At mounting-flange temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_C = 100$ mA, $I_B = 0$)	$V_{CE0(sus)}$	55 min	V
Collector-to-Emitter Voltage ($V_{BE} = -1.5$ V, $I_C = 0.5$ mA)	V_{CEV}	100 min	V

POWER TRANSISTOR

2N1489



Si n-p-n diffused-junction type used in dc-to-dc converters, inverters, choppers, voltage and current regulators, dc and servo amplifiers, relay- and solenoid-actuating circuits. JEDEC TO-3, Outline No.2. See Mounting Hardware for desired mounting arrangement. This type is identical with type 2N1487 except for the following

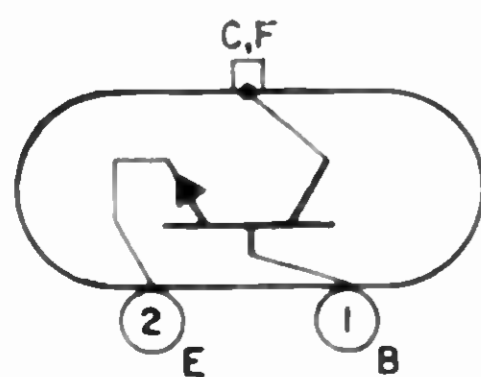
items:

CHARACTERISTICS (At mounting-flange temperature = 25°C)

Base-to-Emitter Voltage ($V_{CE} = 4$ V, $I_C = 1.5$ A)	V_{BE}	2.5 max	V
Static Forward-Current Transfer Ratio ($V_{CE} = 4$ V, $I_C = 1.5$ A)	h_{FE}	25 to 75	
Collector-to-Emitter Saturation Resistance ($I_C = 1.5$ A, $I_B = 100$ mA)	$r_{CE(sat)}$	0.67 max	Ω

POWER TRANSISTOR

2N1490



Si n-p-n diffused-junction type used in dc-to-dc converters, inverters, choppers, voltage and current regulators, dc and servo amplifiers, relay- and solenoid-actuating circuits. JEDEC TO-3, Outline No.2. See Mounting Hardware for desired mounting arrangement. This type is identical with type 2N1487 except for the following

items:

MAXIMUM RATINGS

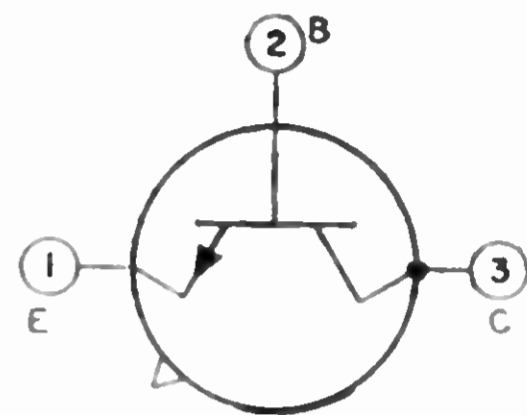
Collector-to-Base Voltage	V_{CBO}	100	V
Collector-to-Emitter Voltage:			
$V_{BE} = -1.5$ V	V_{CEV}	100	V
Base open (sustaining voltage)	$V_{CEO(sus)}$	55	V

CHARACTERISTICS (At mounting-flange temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($V_C = 100$ mA, $I_B = 0$)	$V_{CEO(sus)}$	55 min	V
Collector-to-Emitter Voltage ($V_{BE} = -1.5$ V, $I_C = 0.5$ mA)	V_{CEV}	100 min	V
Base-to-Emitter Voltage ($V_{CE} = 4$ V, $I_C = 1.5$ A) ...	V_{BE}	2.5 max	V
Static Forward-Current Transfer Ratio ($V_{CE} = 4$ V, $I_C = 1.5$ A)	h_{FE}	25 to 75	
Collector-to-Emitter Saturation Resistance ($I_C = 1.5$ A, $I_B = 100$ mA)	$r_{CE(sat)}$	0.67 max	Ω

2N1491**TRANSISTOR**

Si n-p-n triple-diffused type used in vhf applications for rf-amplifier, video-amplifier, oscillator, and mixer circuits in industrial and military equipment. JEDEC TO-39, Outline No.15.

**MAXIMUM RATINGS**

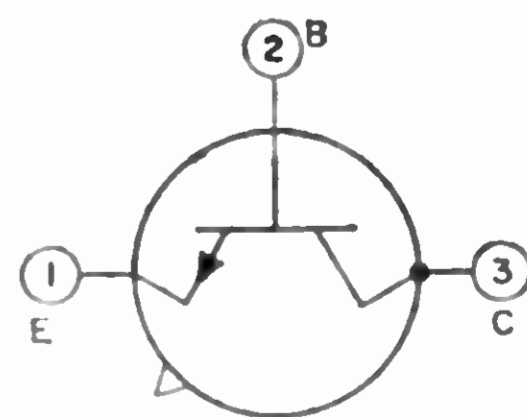
Collector-to-Base Voltage	V_{CBO}	30	V
Collector-to-Emitter Voltage ($V_{BE} = -0.5$ V)	V_{CEV}	30	V
Emitter-to-Base Voltage	V_{EBO}	1	V
Collector Current	I_C	100	mA
Base Current	I_B	20	mA
Emitter Current	I_E	-100	mA
Transistor Dissipation:			
T_c up to 25°C	P_T	3	W
T_c above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (T_c) and Storage (T_{STG})		-65 to 175	°C
Lead-Soldering Temperature (10 s max)	T_L	255	°C

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = 0.1$ mA, $I_E = 0$)	$V_{(BR)CBO}$	30 min	V
Emitter-to-Base Floating Potential ($V_{CB} = 30$ V, $I_E = 0$)	$V_{EB(f)}$	0.5 max	V
Collector-Cutoff Current ($V_{CB} = 12$ V, $I_E = 0$)	I_{CBO}	10 max	μA
Emitter-Cutoff Current ($V_{EB} = 1$ V, $I_C = 0$)	I_{EBO}	100 max	μA
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 20$ V, $I_C = 15$ mA, $f = 1$ kHz)	h_{fe}	15 to 200	
Gain-Bandwidth Product ($V_{CB} = 30$ V, $I_C = 15$ mA) ...	f_T	300	MHz
Output Capacitance ($V_{CB} = 30$ V, $I_E = 0$, $f = 0.15$ MHz)	C_{ob0}	5 max	pF
Small-Signal Power Gain ($V_{CB} = 15$ V, $I_E = -15$ mA, $P_{oe} = 10$ mW, $f = 70$ MHz)	G_{pe}	13 min	dB
Thermal Resistance, Junction-to-Case	θ_{J-C}	50	°C/W

2N1492**TRANSISTOR**

Si n-p-n triple-diffused type used in vhf applications for rf-amplifier, video-amplifier, oscillator, and mixer circuits in industrial and military equipment. JEDEC TO-39, Outline No.15. This type is identical with type 2N1491 except for the following items:

**MAXIMUM RATINGS**

Collector-to-Base Voltage	V_{CBO}	60	V
Collector-to-Emitter Voltage ($V_{BE} = -0.5$ V)	V_{CEV}	60	V
Emitter-to-Base Voltage	V_{EBO}	2	V

CHARACTERISTICS

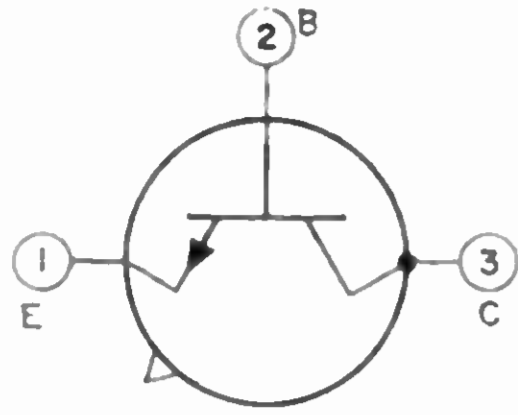
Collector-to-Base Breakdown Voltage ($I_C = 0.1$ mA, $I_E = 0$)	$V_{(BR)CBO}$	60 min	V
Emitter-to-Base Floating Potential ($V_{CB} = 60$ V, $I_E = 0$)	$V_{EB(f)}$	0.5 max	V

CHARACTERISTICS (cont'd)

Emitter-Cutoff Current ($V_{EB} = 2 \text{ V}, I_C = 0$)	I_{EBO}	100 max	μA
Small-Signal Power Gain ($V_{CB} = 30 \text{ V}, I_E = -15 \text{ mA}, P_{oe} = 100 \text{ mW}, f = 70 \text{ MHz}$)	G_{pe}	13 min	dB

TRANSISTOR

2N1493



Si n-p-n triple-diffused type used in vhf applications for rf-amplifier, video-amplifier, oscillator, and mixer circuits in industrial and military equipment. JEDEC TO-39, Outline No.15. This type is identical with type 2N1491 except for the following items:

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	100	V
Collector-to-Emitter Voltage ($V_{BE} = -0.5 \text{ V}$)	V_{CEV}	100	V
Emitter-to-Base Voltage	V_{EBO}	4.5	V

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = 0.1 \text{ mA}, I_E = 0$)	$V_{(BR)CBO}$	100 min	V
Emitter-to-Base Floating Potential ($V_{CB} = 100 \text{ V}, I_E = 0$)	$V_{EB}(f)$	0.5 max	V
Emitter-Cutoff Current ($V_{EB} = 4.5 \text{ V}, I_C = 0$)	I_{EBO}	100 max	μA
Small-Signal Power Gain ($V_{CB} = 50 \text{ V}, I_E = -25 \text{ mA}, P_{oe} = 500 \text{ mW}, f = 70 \text{ MHz}$)	G_{pe}	10 min	dB

Refer to Chart of Discontinued Transistors

2N1511

Refer to Chart of Discontinued Transistors

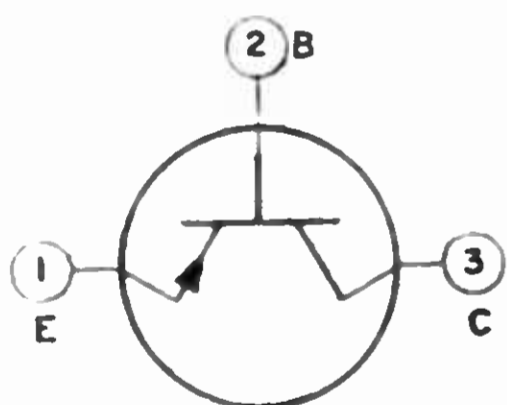
2N1512

Refer to Chart of Discontinued Transistors

2N1513

Refer to Chart of Discontinued Transistors

2N1514



TRANSISTOR

2N1524

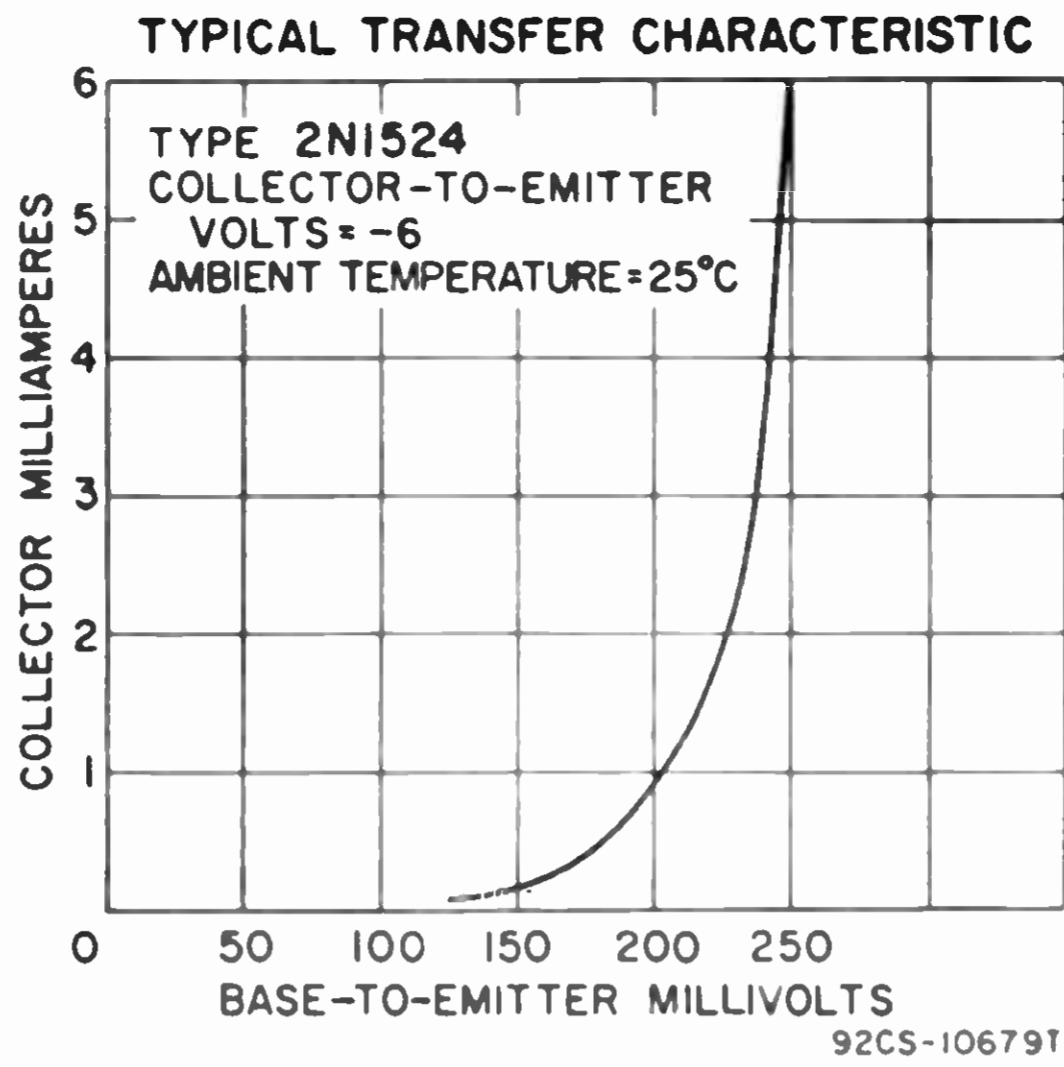
Ge p-n-p drift-field type used in 455-kHz if-amplifier service in battery-operated portable radio receivers and automobile radio receivers operating from either a 6-volt or a 12-volt supply. JEDEC TO-1, Outline No.1.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-24	V
Emitter-to-Base Voltage	V_{EBO}	-0.5	V
Collector Current	I_C	-10	mA
Emitter Current	I_E	10	mA
Transistor Dissipation:			
$T_A = 25^\circ\text{C}$	P_T	80	mW
$T_A = 55^\circ\text{C}$	P_T	50	mW
$T_A = 71^\circ\text{C}$	P_T	35	mW
Temperature Range:			
Operating (Ambient)	$T_A(\text{opr})$	-65 to 71	$^\circ\text{C}$
Storage	T_{STG}	-65 to 85	$^\circ\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	255	$^\circ\text{C}$

CHARACTERISTICS

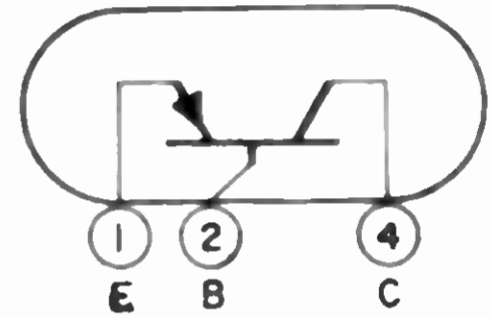
Collector-to-Base Breakdown Voltage ($V_{EB} = -0.5 \text{ V}, I_C = -50 \mu\text{A}$)	$V_{(BR)CBV}$	-24 min	V
Collector-Cutoff Current ($V_{CB} = -12 \text{ V}, I_E = 0$)	I_{CBO}	-16 max	μA
Emitter-Cutoff Current ($V_{EB} = -0.5 \text{ V}, I_C = 0$)	I_{EBO}	-16 max	μA
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = -12 \text{ V}, I_E = -1 \text{ mA}, f = 1 \text{ kHz}$)	h_{fe}	60	
Collector-to-Base Feedback Capacitance ($V_{CE} = -8.5 \text{ V}, I_E = 1 \text{ mA}$)	C_{cb}	2.1	pF
Maximum Available Amplifier Gain Δ ($V_{CE} = -8.5 \text{ V}, I_E = 1 \text{ mA}, f = 455 \text{ kHz}$)	MAG*	52.4	dB
Maximum Usable Amplifier Gain, Unneutralized Δ ($V_{CE} = -8.5 \text{ V}, I_E = 1 \text{ mA}, f = 455 \text{ kHz}$)	MUG	30	dB
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	0.4	$^\circ\text{C}/\text{mW}$



▲ This characteristic does not apply to type 2N1526.
 * Measured in a single-tuned unilateralized circuit matched to the generator and load impedances for maximum transfer of power (transformer insertion losses not included).

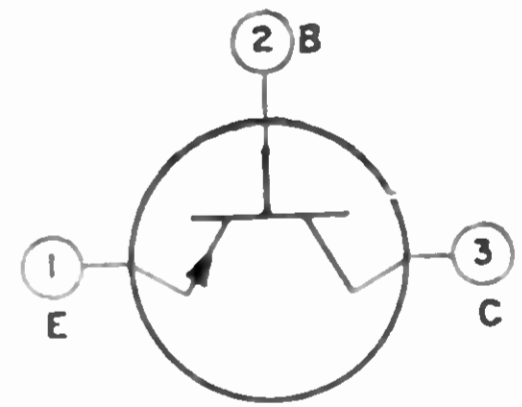
2N1525 TRANSISTOR

Ge p-n-p drift-field type used in 455-kHz if-amplifier service in battery-operated portable radio receivers and automobile radio receivers operating from either a 6-volt or a 12-volt supply. JEDEC TO-40, Outline No.16. This type is electrically identical with type 2N1524.



2N1526 TRANSISTOR

Ge p-n-p drift-field type used in mixer and oscillator applications in battery-operated portable radio receivers and automobile radio receivers operating from either a 6-volt or a 12-volt supply. JEDEC TO-1, Outline No.1. This type is identical with type 2N1524 except for the following items:

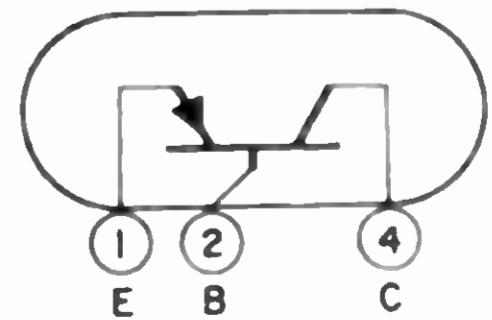


CHARACTERISTICS

Small-Signal Forward-Current Transfer Ratio ($V_{CE} = -12\text{ V}$, $I_E = 1\text{ mA}$, $f = 1\text{ kHz}$)	h_{fe}	130	
Maximum Available Conversion Power Gain ($V_{CE} = -8\text{ V}$, $I_E = 0.65\text{ mA}$, $f = 1.5\text{ MHz}$)	MAG _c	46.1	dB
Maximum Usable Conversion Power Gain ($V_{CE} = -8\text{ V}$, $I_E = 0.65\text{ mA}$, $f = 1.5\text{ MHz}$)	MUG _c	34.5	dB
Base-to-Emitter Oscillator-Injection Voltage ($V_{CE} = -8\text{ V}$, $I_E = 0.65\text{ mA}$)		100	mV (rms)

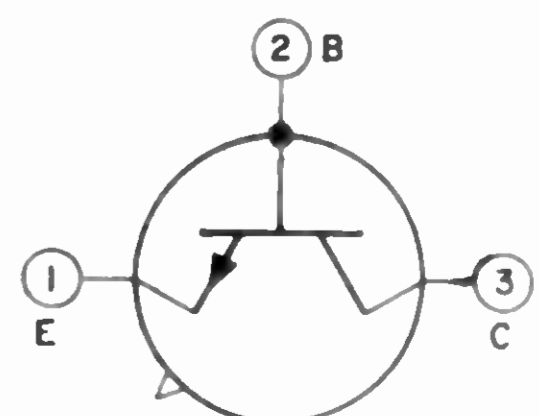
2N1527 TRANSISTOR

Ge p-n-p drift-field type used in mixer and oscillator applications in battery-operated portable radio receivers and automobile radio receivers operating from either a 6-volt or a 12-volt supply. JEDEC TO-40, Outline No.16. This type is electrically identical with type 2N1526.



2N1605 2N1605A COMPUTER TRANSISTORS

Ge n-p-n alloy-junction types used in medium-speed switching applications in data-processing equipment.



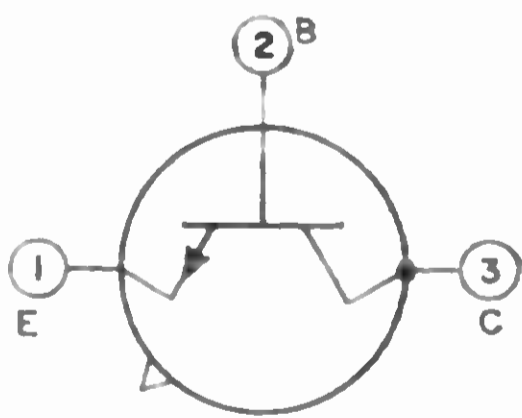
The n-p-n construction permits complementary operation with a matching p-n-p type such as the 2N404. JEDEC TO-5, Outline No.5.

MAXIMUM RATINGS

		2N1605	2N1605A	
Collector-to-Base Voltage	V _{CB0}	25	40	V
Collector-to-Emitter Voltage (V _{BE} = -1 V) ...	V _{C_{EV}}	24	40	V
Emitter-to-Base Voltage	V _{EBO}	12	12	V
Collector Current	I _C	100	100	mA
Emitter Current	I _E	-100	-100	mA
Transistor Dissipation:				
T _A up to 25°C	P _T	150	200	mW
T _A above 25°C	P _T	See curve page 300		
Temperature Range:				
Operating (Junction)	T _J (opr)	100	100	°C
Storage	T _{STG}	-65 to 100 °C		
Lead-Soldering Temperature (10 s max)	T _L	235	235	°C

CHARACTERISTICS

Collector-to-Base Breakdown Voltage:				
I _C = 0.02 mA, I _E = 0	V _{(BR)CBO}	25	- min	V
I _C = 0.01 mA, I _E = 0	V _{(BR)CBO}	-	40 min	V
Emitter-to-Base Breakdown Voltage (I _E = 0.02 mA, I _C = 0)	V _{(BR)EBO}	12	12 min	V
Collector-to-Emitter Saturation Voltage:				
I _C = 12 mA, I _B = 0.4 mA	V _{CE(sat)}	0.15	0.15 max	V
I _C = 24 mA, I _B = 1 mA	V _{CE(sat)}	0.2	0.2 max	V
Base-to-Emitter Voltage:				
I _C = 12 mA, I _B = 0.4 mA	V _{BE}	0.35	0.35 max	V
I _C = 24 mA, I _B = 1 mA	V _{BE}	0.4	0.4 max	V
Emitter Floating Potential (11-MΩ min volt- meter between emitter and base):				
V _{CB} = 24 V	V _{EB(fl)}	1	- max	V
V _{CB} = 40 V	V _{EB(fl)}	-	1 max	V
Collector-Cutoff Current:				
V _{CB} = 12 V, I _E = 0, T _A = 25°C	I _{CBO}	5	- max	μA
V _{CB} = 12 V, I _E = 0, T _A = 80°C	I _{CBO}	125	125 max	μA
V _{CB} = 40 V, I _E = 0, T _A = 25°C	I _{CBO}	-	10 max	μA
Emitter-Cutoff Current (V _{EB} = 2.5 V, I _C = 0)	I _{EBO}	2.5	2.5 max	μA
Static Forward-Current Transfer Ratio:				
V _{CE} = 0.15 V, I _C = 12 mA	h _{FE}	30	30 min	
V _{CE} = 0.2 V, I _C = 24 mA	h _{FE}	24	24 min	
V _{CE} = 0.25 V, I _C = 20 mA	h _{FE}	40	40 min	
Small-Signal Forward-Current Transfer-Ratio				
Cutoff Frequency (V _{CB} = 6 V, I _E = 1 mA)	f _{hftb}	4	4 min	MHz
Total Stored Charge (V _{CC} = 5.25 V, I _C = 10 mA, I _B = 1 mA)	Q _S	1400	1400 max	pC
Output Capacitance (V _{CB} = 6 V, I _E = 1 mA, f = 2 MHz)	C _{obo}	20	20 max	pF



TRANSISTOR

2N1613

Si n-p-n planar type used in small-signal and medium-power applications in industrial and military equipment. JEDEC TO-5, Outline No.5. This type is identical with type 2N2102 except for the following items:

MAXIMUM RATINGS

Collector-to-Base Voltage	V _{CB0}	75	V
Collector-to-Emitter Voltage (R _{BE} ≤ 10 Ω)	V _{CER}	50	V
Transistor Dissipation:			
T _A up to 25°C	P _T	0.8	W
T _c up to 25°C	P _T	3	W
Lead-Soldering Temperature (10 s max)	T _L	265	°C

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Base Breakdown Voltage (I _C = 0.1 mA, I _E = 0)	V _{(BR)CBO}	75 min	V
Collector-to-Emitter Sustaining Voltage (I _C = 100 mA, R _{BE} = 10 Ω, t _p = 300 μs, df = 1.8%)	V _{CER(sus)}	50 min	V
Collector-to-Emitter Saturation Voltage (I _C = 150 mA, I _B = 15 mA, t _p = 300 μs, df = 1.8%)	V _{CE(sat)}	1.5 max	V
Base-to-Emitter Saturation Voltage (I _C = 150 mA, I _B = 15 mA, t _p = 300 μs, df = 1.8%)	V _{BE(sat)}	1.3 max	V

CHARACTERISTICS (cont'd)

Collector-Cutoff Current:

$V_{CB} = 60\text{ V}, I_E = 0, T_A = 25^\circ\text{C}$
 $V_{CB} = 60\text{ V}, I_E = 0, T_A = 150^\circ\text{C}$

Emitter-Cutoff Current ($V_{EB} = 5\text{ V}, I_C = 0$)

Static Forward-Current Transfer Ratio:

$V_{CE} = 10\text{ V}, I_C = 0.1\text{ mA}, T_A = 25^\circ\text{C}$
 $V_{CE} = 10\text{ V}, I_C = 150\text{ mA}, T_A = 25^\circ\text{C}, t_p = 300\ \mu\text{s},$
 $df = 1.8\%$
 $V_{CE} = 10\text{ V}, I_C = 10\text{ mA}, T_A = -55^\circ\text{C}, t_p = 300\ \mu\text{s},$
 $df = 1.8\%$

Small-Signal Forward-Current Transfer Ratio:

$V_{CE} = 5\text{ V}, I_C = 1\text{ mA}, f = 1\text{ kHz}$
 $V_{CE} = 10\text{ V}, I_C = 50\text{ mA}, f = 20\text{ MHz}$

Output Capacitance ($V_{CB} = 10\text{ V}, I_E = 0$)

**Noise Figure ($V_{CE} = 10\text{ V}, I_C = 0.3\text{ mA}, f = 1\text{ kHz},$
 $R_G = 510\ \Omega,$ circuit bandwidth = 1 Hz)**

Thermal Resistance, Junction-to-Case

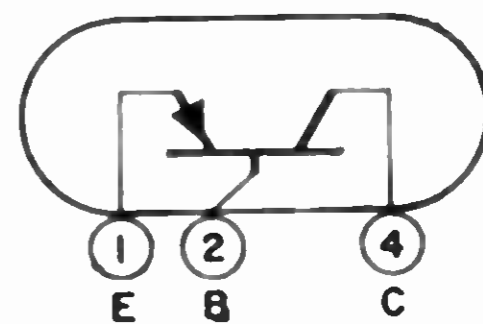
Thermal Resistance, Junction-to-Ambient

I_{CBO}	0.01 max	μA
I_{CBO}	10 max	μA
I_{EBO}	0.01 max	μA
h_{FE}	20 min	
h_{FE}	40 to 120	
h_{FE}	20 min	
h_{fe}	30 to 100	
h_{fe}	3 min	
C_{obo}	25 max	pF
NF	12 max	dB
θ_{J-C}	58.3 max	$^\circ\text{C/W}$
θ_{J-A}	219 max	$^\circ\text{C/W}$

2N1631

TRANSISTOR

Ge p-n-p drift-field type used in rf-amplifier applications in battery-operated AM radio receivers. JEDEC TO-40, Outline No.16.



MAXIMUM RATINGS

Collector-to-Base Voltage
 Collector Current
 Transistor Dissipation:
 $T_A = 25^\circ\text{C}$
 Temperature Range:
 Operating (Ambient)

V_{CBO}	-34	V
I_C	-10	mA
P_T	80	mW
$T_A(\text{opr})$	-65 to 71	$^\circ\text{C}$

CHARACTERISTICS

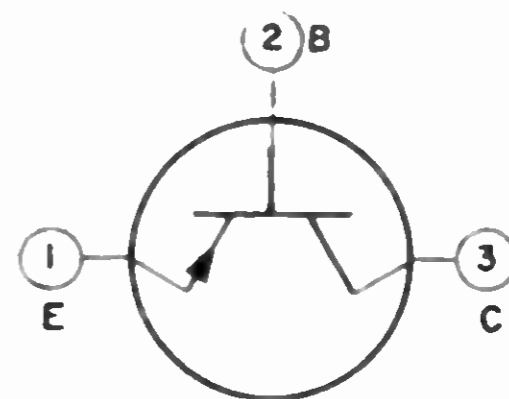
Collector-to-Base Breakdown Voltage ($I_C = -50\ \mu\text{A},$
 $I_E = 0$)
 Collector-Cutoff Current ($V_{CB} = -12\text{ V}, I_E = 0$)
 Small-Signal Forward-Current Transfer Ratio
 ($V_{CE} = -12\text{ V}, I_C = -1\text{ mA}, f = 1\text{ kHz}$)
 Small-Signal Forward-Current Transfer-Ratio Cutoff
 Frequency ($V_{CB} = -12\text{ V}, I_E = 1\text{ mA}$)
 Output Capacitance
 Power Gain ($f = 1.5\text{ MHz}$)
 Thermal Resistance, Junction-to-Ambient

$V_{(BR)CBO}$	-34 min	V
I_{CBO}	-16 max	μA
h_{fe}	80 min	
f_{hfb}	45	MHz
C_{obo}	2	pF
G_{pe}	47.7	dB
θ_{J-A}	0.4 max	$^\circ\text{C/W}$

2N1632

TRANSISTOR

Ge p-n-p drift-field type used in rf-amplifier applications in battery-operated AM radio receivers. JEDEC TO-1, Outline No.1.



MAXIMUM RATINGS

Collector-to-Base Voltage
 Emitter-to-Base Voltage
 Collector Current
 Emitter Current
 Transistor Dissipation:
 $T_A = 25^\circ\text{C}$
 $T_A = 55^\circ\text{C}$
 $T_A = 71^\circ\text{C}$
 Temperature Range:
 Operating (Ambient)
 Storage
 Lead-Soldering Temperature (10 s max)

V_{CBO}	-34	V
V_{EBO}	-0.5	V
I_C	-10	mA
I_E	10	mA
P_T	80	mW
P_T	50	mW
P_T	35	mW
$T_A(\text{opr})$	-65 to 71	$^\circ\text{C}$
T_{STG}	-65 to 85	$^\circ\text{C}$
T_L	255	$^\circ\text{C}$

CHARACTERISTICS

Collector-to-Base Breakdown Voltage
 ($I_C = -0.05\text{ mA}, I_E = 0$)
 Collector-Cutoff Current ($V_{CB} = -12\text{ V}, I_E = 0$)
 Emitter-Cutoff Current ($V_{EB} = -0.5\text{ V}, I_C = 0.05\text{ mA}$)

$V_{(BR)CBO}$	-34 min	V
I_{CBO}	-16 max	μA
I_{EBO}	-16 max	μA

CHARACTERISTICS (cont'd)

Small-Signal Forward-Current Transfer Ratio ($V_{CE} = -12V, I_E = 1 \text{ mA}, f = 1 \text{ kHz}$)	h_{fe}	40 to 170	
Collector-to-Base Feedback Capacitance ($V_{CE} = -8.5 \text{ V}, I_E = 1 \text{ mA}$)	C_{cb}	2.1	pF
Maximum Available Amplifier Gain* ($V_{CE} = -8.5 \text{ V}, I_E = 1 \text{ mA}, f = 1 \text{ kHz}$)	MAG	44.3	dB
Maximum Usable Amplifier Gain, Unneutralized ($V_{CE} = -8.5 \text{ V}, I_E = 1 \text{ mA}, f = 1.5 \text{ kHz}$)	MUG	25.5	dB

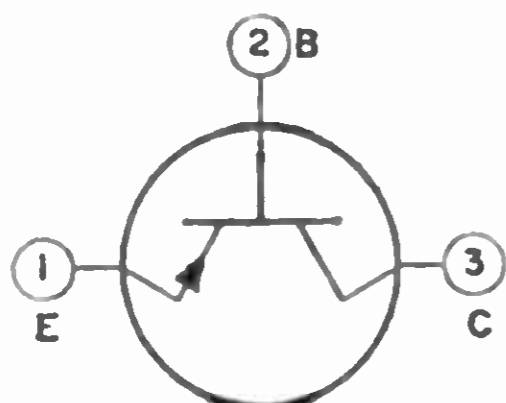
* Measured in a single-tuned unilateralized circuit matched to the generator and load impedances for maximum transfer of power (transformer insertion losses not included).

Refer to Chart of Discontinued Transistors **2N1633**

Refer to Chart of Discontinued Transistors **2N1634**

Refer to Chart of Discontinued Transistors **2N1635**

Refer to Chart of Discontinued Transistors **2N1636**



TRANSISTOR

2N1637

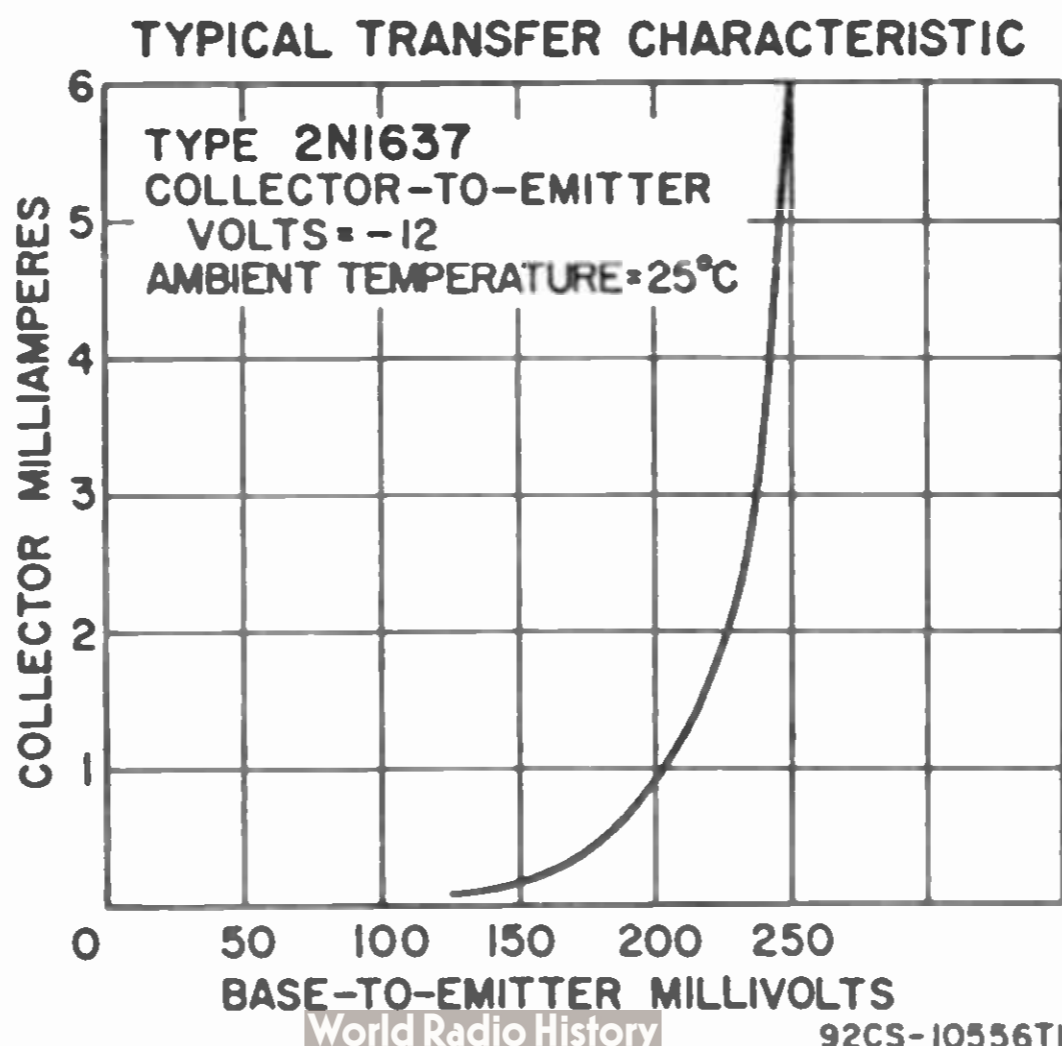
Ge p-n-p drift-field type used in rf-amplifier applications in AM automobile radio receivers. JEDEC TO-1, Outline No.1.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-34	V
Emitter-to-Base Voltage	V_{EBO}	-1.5	V
Collector Current	I_C	-10	mA
Emitter Current	I_E	10	mA
Transistor Dissipation:			
$T_A = 25^\circ\text{C}$	P_T	80	mW
$T_A = 55^\circ\text{C}$	P_T	50	mW
$T_A = 71^\circ\text{C}$	P_T	35	mW
Temperature Range:			
Operating (Ambient)	$T_A(\text{opr})$	-65 to 71	$^\circ\text{C}$
Storage	T_{STG}	-65 to 85	$^\circ\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	255	$^\circ\text{C}$

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = -50 \mu\text{A}, I_E = 0$)	$V_{(BR)CBO}$	-34 min	V
Collector-Cutoff Current ($V_{CB} = -12 \text{ V}, I_E = 0$)	I_{CBO}	-12 max	μA
Emitter-Cutoff Current ($V_{EB} = -1.5 \text{ V}, I_C = 0$)	I_{EBO}	-15 max	μA
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = -12 \text{ V}, I_C = -1 \text{ mA}, f = 1 \text{ kHz}$)	h_{fe}	80	
Collector-to-Base Feedback Capacitance ($V_{CE} = -12 \text{ V}, I_C = -1 \text{ mA}$)	C_{cb}	2	pF
Maximum Available Amplifier Gain* ($V_{CE} = -11 \text{ V}, I_E = 1 \text{ mA}, f = 1.5 \text{ MHz}$)	MAG	47.7	dB



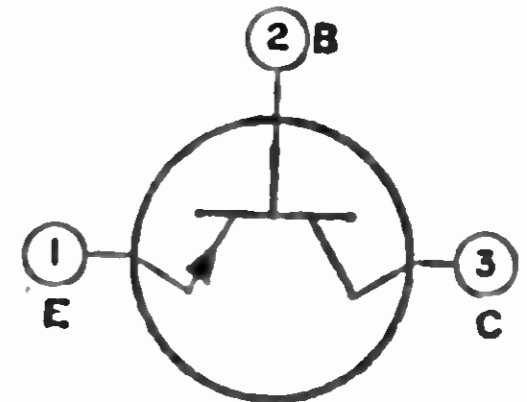
CHARACTERISTICS (cont'd)

Maximum Usable Amplifier Gain, Unneutralized ($V_{CE} = -11$ V, $I_E = 1$ mA, $f = 1.5$ MHz)	MUG	25.6	dB
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	0.4 max	$^{\circ}\text{C}/\text{mW}$

* Measured in a single-tuned unilateralized circuit matched to the generator and load impedances for maximum transfer of power (transformer insertion losses not included).

2N1638 TRANSISTOR

Ge p-n-p drift-field type used in if-amplifier applications in AM automobile radio receivers. JEDEC TO-1, Outline No.1. This type is identical with type 2N1637 except for the following items:



CHARACTERISTICS

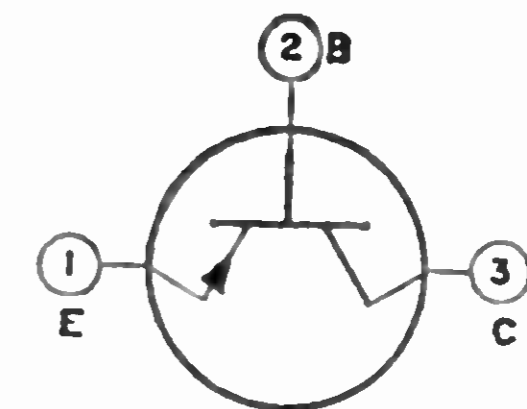
Collector-Cutoff Current ($V_{CB} = -12$ V, $I_C = 0$)	I_{CBO}	-12 max	μA
Emitter-Cutoff Current ($V_{EB} = -0.5$ V, $I_C = 0$)	I_{EBO}	-12 max	μA
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = -12$ V, $I_C = -1$ mA, $f = 1$ kHz)	h_{fe}	75	
Maximum Available Amplifier Gain Δ * ($V_{CE} = -11$ V, $I_E = 2$ mA, $f = 262.5$ kHz)	MAG	61.5	dB
Maximum Usable Amplifier Gain, Unneutralized Δ ($V_{CE} = -11$ V, $I_E = 2$ mA, $f = 262.5$ kHz)	MUG	36.6	dB
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	0.4 max	$^{\circ}\text{C}/\text{mW}$

Δ This characteristic does not apply to type 2N1639.

* Measured in a single-tuned unilateralized circuit matched to the generator and load impedances for maximum transfer of power (transformer insertion losses not included).

2N1639 TRANSISTOR

Ge p-n-p drift-field type used in converter, mixer, and oscillator applications in AM automobile radio receivers. JEDEC TO-1, Outline No.1. This type is identical with type 2N1637 except for the following items:

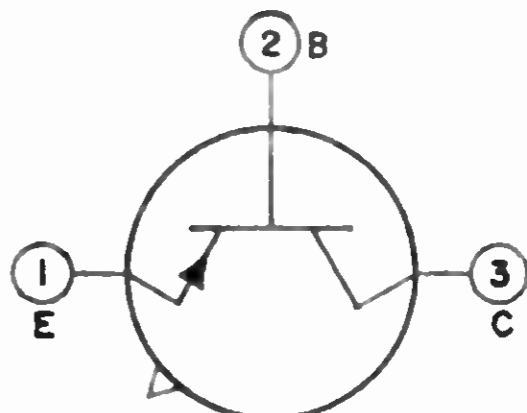


CHARACTERISTICS

Small-Signal Forward-Current Transfer Ratio ($V_{CE} = -12$ V, $I_C = -1$ mA, $f = 1$ kHz)	h_{fe}	75	
Maximum Usable Conversion Power Gain ($V_{CE} = -11$ V, $I_E = 0.25$ mA, $f = 1.5$ MHz)	MUG _c	37	dB
Base-to-Emitter Oscillator-Injection Voltage (RMS) ($V_{CE} = -11$ V, $I_E = 0.25$ mA)		100 mV(rms)	

2N1683 COMPUTER TRANSISTOR

Ge p-n-p diffused-junction type used in computer applications in data-processing equipment. JEDEC TO-5, Outline No.5. This type is identical with type 2N1300 except for the following items:



MAXIMUM RATINGS

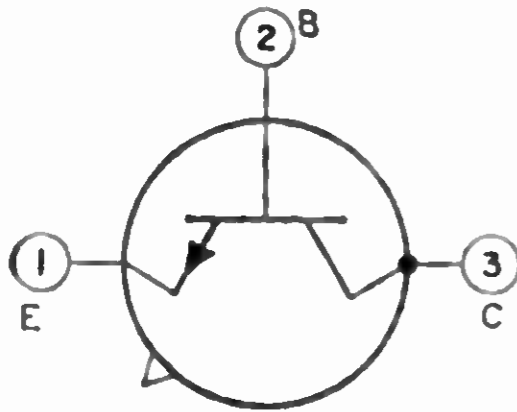
Emitter-to-Base Voltage*	V_{EBO}	-4	V
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CHARACTERISTICS

Emitter-to-Base Breakdown Voltage ($I_E = -0.1$ mA, $I_C = 0$)	$V_{(BR)EBO}$	-4 min	V
Base-to-Emitter Voltage ($I_C = -40$ mA, $I_B = -1$ mA)	V_{BE}	-0.6 max	V
Static Forward-Current Transfer Ratio: $V_{CE} = -0.3$ V, $I_C = -10$ mA	h_{FE}	50 min; 75 typ	
$V_{CE} = -0.5$ V, $I_C = -40$ mA	h_{FE}	50 min; 85 typ	
Gain-Bandwidth Product ($V_{CE} = -3$ V, $I_C = -10$ mA)	f_T	50 min	MHz
Total Stored Charge: $I_C = -10$ mA, $I_B = -0.4$ mA	Q_S	160 max	pC
$I_C = -40$ mA, $I_B = -1.6$ mA	Q_S	410 max	pC

* This rating may be exceeded and the emitter-to-base junction operated in the breakdown condition provided the emitter dissipation is limited to 30 milliwatts at 25°C. For ambient temperatures above 25°C, reduce the dissipation by 0.5 milliwatts per °C.

POWER TRANSISTOR 2N1700



Si n-p-n diffused-junction type used in power-switching circuits such as dc-to-dc converters, inverters, choppers, solenoid and relay controls; in oscillators, regulators, and pulse-amplifier circuits; and as class A and class B push-pull audio and servo amplifiers in industrial and military equipment. JEDEC TO-5, Outline No.5. For typical operation in a power-switching circuit, refer to type 2N1479.

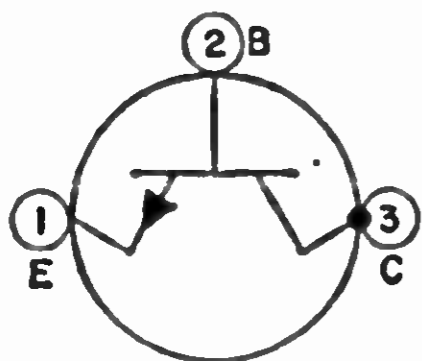
MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	60	V
Collector-to-Emitter Voltage:			
$V_{BE} = -1.5$ V	V_{CEV}	60	V
Base open (sustaining voltage)	$V_{CEO(sus)}$	40	V
Emitter-to-Base Voltage	V_{EBO}	6	V
Collector Current	I_C	1	A
Base Current	I_B	0.75	A
Transistor Dissipation:			
T_c up to 25°C	P_T	5	W
T_c above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	255	°C

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_C = 50$ mA, $I_B = 0$)	$V_{CEO(sus)}$	40 min	V
Collector-to-Emitter Voltage ($V_{BE} = -1.5$ V, $I_C = 0.5$ mA)	V_{CEV}	60 min	V
Base-to-Emitter Voltage ($V_{CE} = 4$ V, $I_C = 100$ mA) ...	V_{BE}	2 max	V
Collector-Cutoff Current:			
$V_{CB} = 30$ V, $I_E = 0$, $T_c = 25^\circ\text{C}$	I_{CBO}	75 max	μA
$V_{CB} = 30$ V, $I_E = 0$, $T_c = 150^\circ\text{C}$	I_{CBO}	1000 max	μA
Emitter-Cutoff Current ($V_{EB} = 6$ V, $I_C = 0$)	I_{EBO}	25 max	μA
Collector-to-Emitter Saturation Resistance ($I_C = 100$ mA, $I_B = 10$ mA)	$r_{CE(sat)}$	10 max	Ω
Static Forward-Current Transfer Ratio ($V_{CE} = 4$ V, $I_C = 100$ mA)	h_{FE}	20 to 80	
Thermal Resistance, Junction-to-Case	θ_{J-C}	35 max	°C/W
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	200 max	°C/W

POWER TRANSISTOR 2N1701



Si n-p-n diffused-junction type used in power-switching applications such as dc-to-dc converter, inverter, chopper, solenoid and relay control circuits; in oscillator, regulator, and pulse-amplifier circuits; and as class A and class B push-pull audio and servo amplifiers in industrial and military equipment. JEDEC TO-8, Outline No.10. See Mounting Hardware for desired mounting arrangement.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	60	V
Collector-to-Emitter Voltage:			
$V_{BE} = -1.5$ V	V_{CEV}	60	V
Base open (sustaining voltage)	$V_{CEO(sus)}$	40	V
Emitter-to-Base Voltage	V_{EBO}	6	V
Collector Current	I_C	2.5	A
Base Current	I_B	1	A

MAXIMUM RATINGS (cont'd)

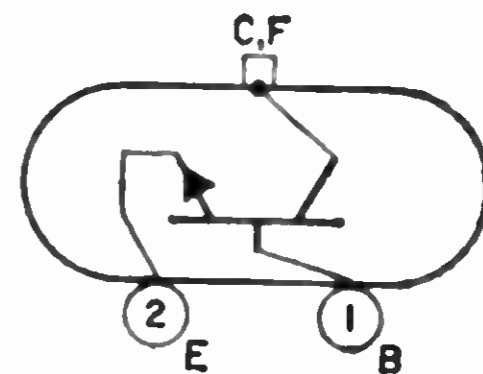
Transistor Dissipation:			
T_c up to 25°C	P_T	25	W
T_c above 25°C	P_T	See curve	page 300
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	235	°C

CHARACTERISTICS

Collector-to-Emitter Sustaining Voltage ($I_c = 100$ mA, $I_B = 0$)	V_{CEO} (sus)	40 min	V
Collector-to-Emitter Voltage ($V_{BE} = -1.5$, $I_c = 0.75$ mA)	V_{CEV}	60 min	V
Collector-to-Emitter Saturation Voltage: ($I_c = 2.5$ A, $I_B = 1$ A)	V_{CE} (sat)	12.5 max	V
Base-to-Emitter Voltage ($V_{CE} = 4$ V, $I_c = 300$ mA)	V_{BE}	3 max	V
Collector-Cutoff Current:			
$V_{CB} = 30$ V, $I_E = 0$, $T_c = 25^\circ\text{C}$	I_{CBO}	100 max	μA
$V_{CB} = 30$ V, $I_E = 0$, $T_c = 150^\circ\text{C}$	I_{CBO}	1500 max	μA
Emitter-Cutoff Current ($V_{EB} = -6$ V, $I_c = 0$)	I_{EBO}	50 max	μA
Collector-to-Emitter Saturation Resistance ($I_c = 300$ mA, $I_B = 30$ mA)	r_{CE} (sat)	5 max	Ω
Static Forward-Current Transfer Ratio:			
$V_{CE} = 4$ V, $I_c = 300$ mA	h_{FE}	20 to 80	
$V_{CE} = 20$ V, $I_c = 2.5$ A	h_{FE}	5 min	
Thermal Resistance, Junction-to-Case	Θ_{J-C}	7 max	°C/W
Thermal Resistance, Junction-to-Ambient	Θ_{J-A}	100 max	°C/W

2N1702 POWER TRANSISTOR

Si n-p-n diffused-junction type used in power-switching applications such as dc-to-dc converter, inverter, chopper, and relay control circuits; in voltage and current regulator circuits; and in dc and servo amplifier circuits. Similar to JEDEC TO-3, Outline No.3. See Mounting Hardware for desired mounting arrangement.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	60	V
Collector-to-Emitter Voltage:			
$V_{BE} = -1.5$ V	V_{CEV}	60	V
Base open (sustaining voltage)	V_{CEO} (sus)	40	V
Emitter-to-Base Voltage	V_{EBO}	6	V
Collector Current	I_C	5	A
Base Current	I_B	2.5	A
Transistor Dissipation:			
T_c up to 25°C	P_T	75	W
T_c above 25°C	P_T	See curve	page 300
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C

CHARACTERISTICS

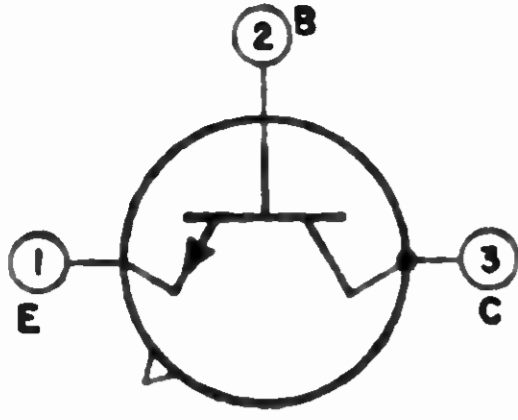
Collector-to-Emitter Sustaining Voltage ($I_c = 100$ mA, $I_B = 0$)	V_{CEO} (sus)	40 min	V
Collector-to-Emitter Voltage ($V_{BE} = -1.5$ V, $I_c = 1$ mA)	V_{CEV}	60 min	V
Base-to-Emitter Voltage ($V_{CE} = 4$ V, $I_c = 800$ mA)	V_{BE}	4 max	V
Collector-Cutoff Current:			
$V_{CB} = 30$ V, $I_E = 0$, $T_c = 25^\circ\text{C}$	I_{CBO}	200	μA
$V_{CB} = 30$ V, $I_E = 0$, $T_c = 150^\circ\text{C}$	I_{CBO}	2000	μA
Emitter-Cutoff Current ($V_{EB} = 6$ V, $I_c = 0$)	I_{EBO}	100	μA
Collector-to-Emitter Saturation Resistance ($I_c = 800$ mA, $I_B = 80$ mA)	r_{CE} (sat)	4 max	Ω
Static Forward-Current Transfer Ratio ($V_{CE} = 4$ V, $I_c = 800$ mA)	h_{FE}	15 to 60	
Thermal Resistance, Junction-to-Case	Θ_{J-C}	2.33 max	°C/W

2N1708

Refer to Chart of Discontinued Transistors

TRANSISTOR

2N1711



Si n-p-n triple-diffused planar type used in a wide variety of small-signal and medium-power applications in military and industrial equipment. It features exceptionally low noise characteristics. JEDEC TO-5, Outline No.5.

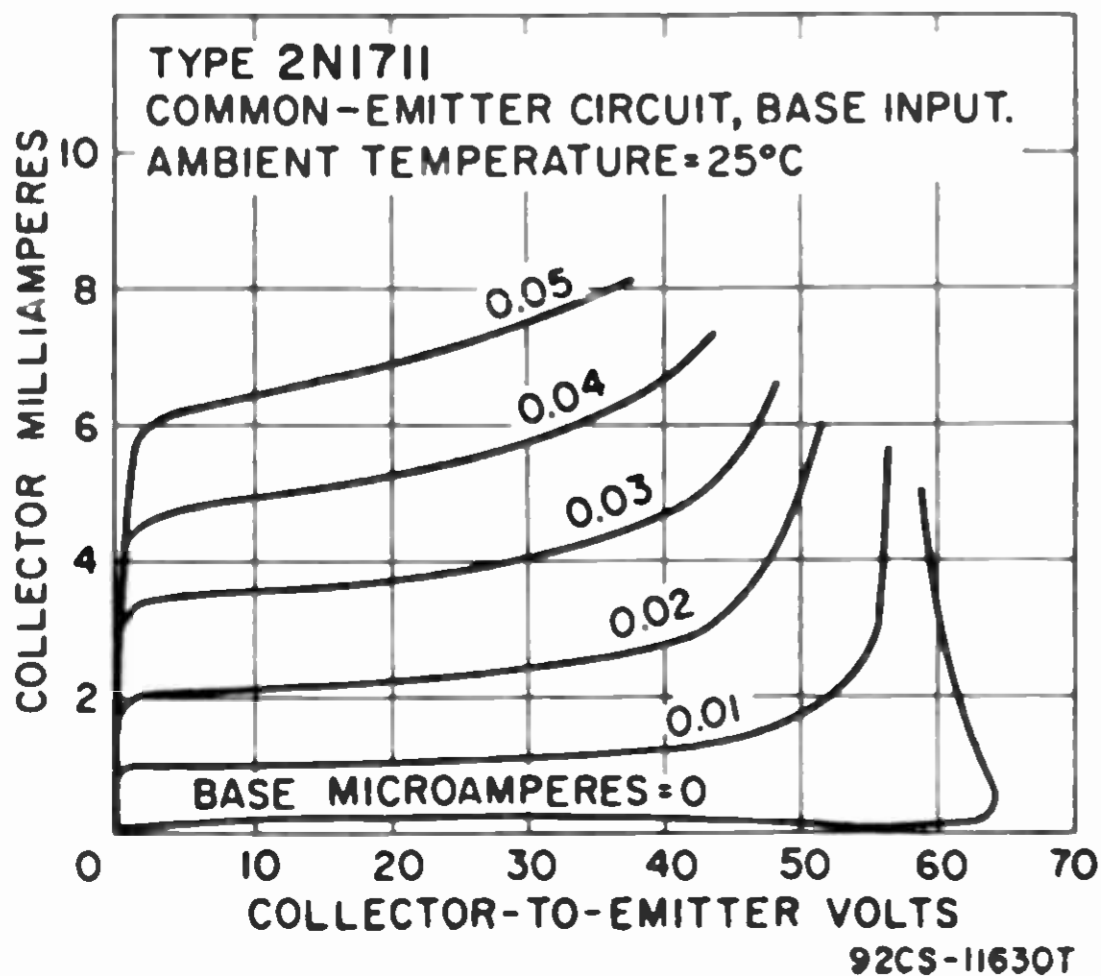
MAXIMUM RATINGS

Collector-to-Base Voltage	V _{CB0}	75	V
Collector-to-Emitter Voltage (R _{BE} ≤ 10 Ω)	V _{CER}	50	V
Emitter-to-Base Voltage	V _{EBO}	7	V
Collector Current	I _C	1	A
Transistor Dissipation:			
T _A up to 25°C	P _T	0.8	W
T _C up to 25°C	P _T	3	W
T _A or T _C above 25°C	P _T	See curve page 300	
Temperature Range:			
Operating (Junction)	T _J (opr)	-65 to 200	°C
Storage	T _{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T _L	300	°C

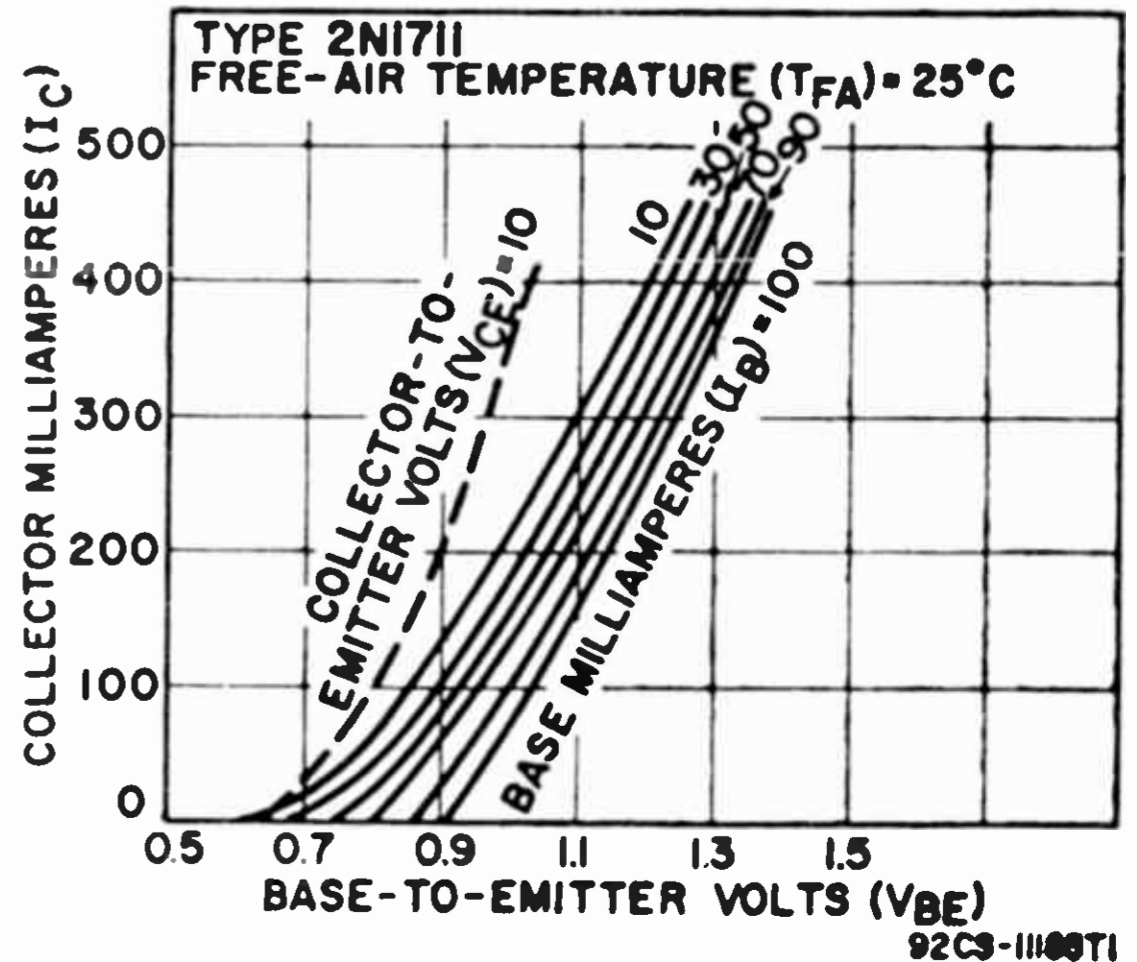
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Base Breakdown Voltage (I _C = 0.1 mA, I _E = 0)	V _{(BR)CBO}	75 min	V
Emitter-to-Base Breakdown Voltage (I _E = 0.1 mA, I _C = 0)	V _{(BR)EBO}	7 min	V
Collector-to-Emitter Reach-Through Voltage (V _{BE} (fl) = -1.5 V, I _C = 0.1 mA)	V _{RT}	75 min	V
Collector-to-Emitter Sustaining Voltage (R _{BE} = 10 Ω, I _C = 100 mA, t _p = 300 μs, df = 1.8%)	V _{CER(sus)}	50 min	V
Collector-to-Emitter Saturation Voltage (I _C = 150 mA, I _B = 15 mA)	V _{CE(sat)}	1.5 max	V
Base-to-Emitter Voltage Saturation Voltage (I _C = 150 mA, I _B = 15 mA)	V _{BE(sat)}	1.3 max	V
Collector-Cutoff Current:			
V _{CB} = 60 V, I _E = 0, T _A = 25°C	I _{CBO}	0.01 max	μA
V _{CB} = 60 V, I _E = 0, T _A = 150°C	I _{CBO}	10 max	μA
Emitter-Cutoff Current (V _{EB} = 5 V, I _C = 0)	I _{EBO}	0.005 max	μA
Pulsed Static Forward-Current Transfer Ratio:			
V _{CE} = 10 V, I _C = 10 mA, t _p = 300 μs, df = 1.8%	h _{FE} (pulsed)	75 min	
V _{CE} = 10 V, I _C = 150 mA, t _p = 300 μs, df = 1.8%	h _{FE} (pulsed)	100 to 300	
V _{CE} = 10 V, I _C = 500 mA, t _p = 300 μs, df = 1.8% ..	h _{FE} (pulsed)	40 min	
Static Forward-Current Transfer Ratio:			
V _{CE} = 10 V, I _C = 0.01 mA, T _C = 25°C	h _{FE}	20 min	
V _{CE} = 10 V, I _C = 0.1 mA, T _C = 25°C	h _{FE}	35 min	
V _{CE} = 10 V, I _C = 10 mA, T _C = -55°C	h _{FE}	35 min	
Small-Signal Forward-Current Transfer Ratio:			
V _{CE} = 5 V, I _C = 1 mA, f = 1 kHz	h _{fe}	50 to 200	
V _{CE} = 10 V, I _C = 5 mA, f = 1 kHz	h _{fe}	70 to 300	
V _{CE} = 10 V, I _C = 50 mA, f = 20 MHz	h _{fe}	3.5 min	
Input Capacitance (V _{EB} = 0.5 V, I _C = 0)	C _{ibo}	80 max	pF
Output Capacitance (V _{CB} = 10 V, I _E = 0)	C _{obo}	25 max	pF

TYPICAL COLLECTOR CHARACTERISTICS



TYPICAL TRANSFER CHARACTERISTICS



CHARACTERISTICS (cont'd)

Noise Figure ($V_{CE} = 10\text{ V}$, $I_C = 0.3\text{ mA}$, $R_G = 50\Omega$, $f = 1\text{ kHz}$, circuit bandwidth = 1 Hz)	NF	8 max	dB
Input Resistance ($V_{CB} = 10\text{ V}$, $I_C = 5\text{ mA}$, $f = 1\text{ kHz}$)	h_{ib}	4 to 8	Ω
Voltage-Feedback Ratio ($V_{CB} = 10\text{ V}$, $I_C = 5\text{ mA}$, $f = 1\text{ kHz}$)	h_{rb}	5×10^{-4} max	
Output Conductance ($V_{CB} = 10\text{ V}$, $I_C = 5\text{ mA}$, $f = 1\text{ kHz}$)	h_{ob}	0.1 to 1	μmho
Thermal Resistance, Junction-to-Case	Θ_{J-C}	58.3 max	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Ambient	Θ_{J-A}	219 max	$^{\circ}\text{C/W}$

2N1768

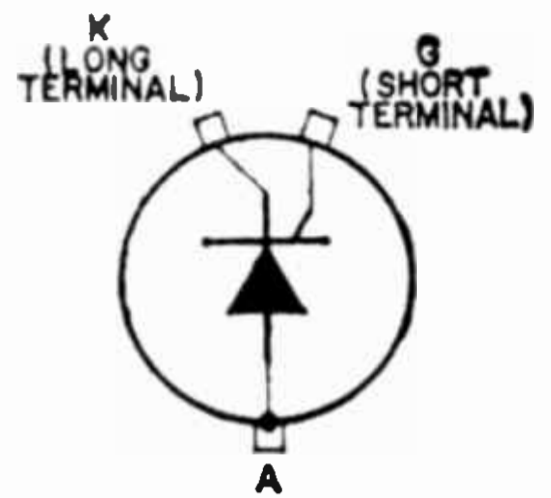
Refer to Chart of Discontinued Transistors

2N1769

Refer to Chart of Discontinued Transistors

2N1842A- 2N1850A SILICON CONTROLLED RECTIFIERS

Si all-diffused three-junction types for use in power-control and power-switching applications. JEDEC TO-48, Outline No.20. See Mounting Hardware for desired mounting arrangement.



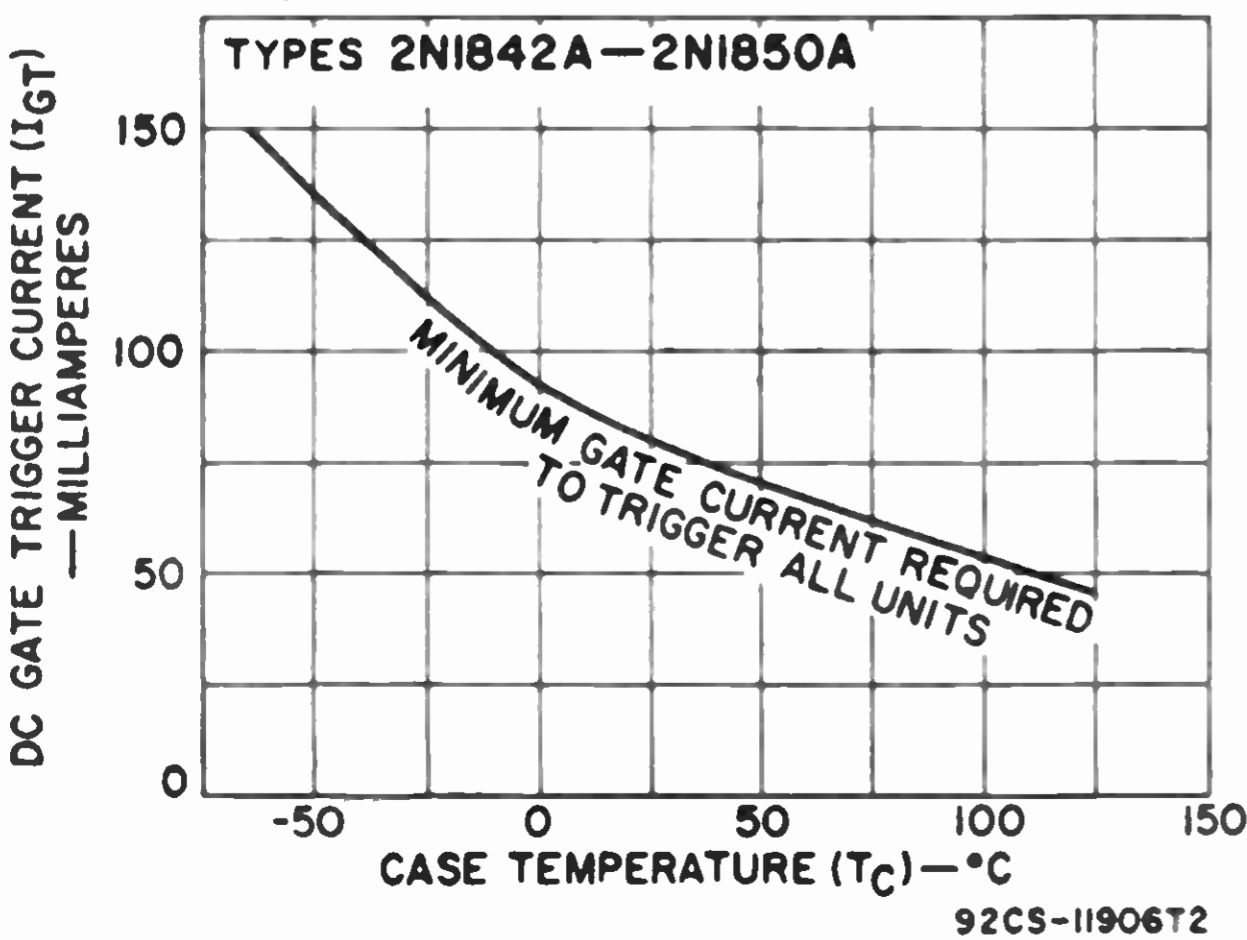
MAXIMUM RATINGS (For sinusoidal ac supply voltage at $f = 50$ to 400 Hz with resistive or inductive load)

	2N1842A	2N1843A	2N1844A	2N1845A	2N1846A	2N1847A	2N1848A	2N1849A	2N1850A	
V_{RSOM}	35	75	150	225	300	350	400	500	600	V
V_{RROM}	25	50	100	150	200	250	300	400	500	V
V_{DROM}					600					V
$I_{T(AV)}$	10 (conduction angle = 180° , $T_c = 80^{\circ}\text{C}$)									V
$I_{T(RMS)}$	16									A
I_{TSM}	125 (1 cycle of voltage)									A
P_{GM}	5									W
$P_{G(AV)}$	0.5									W
I_{GTM}	2									A
V_{GTM}	10, 5									V
T_{stg}	-65 to 125									$^{\circ}\text{C}$
T_c	-65 to 125									$^{\circ}\text{C}$

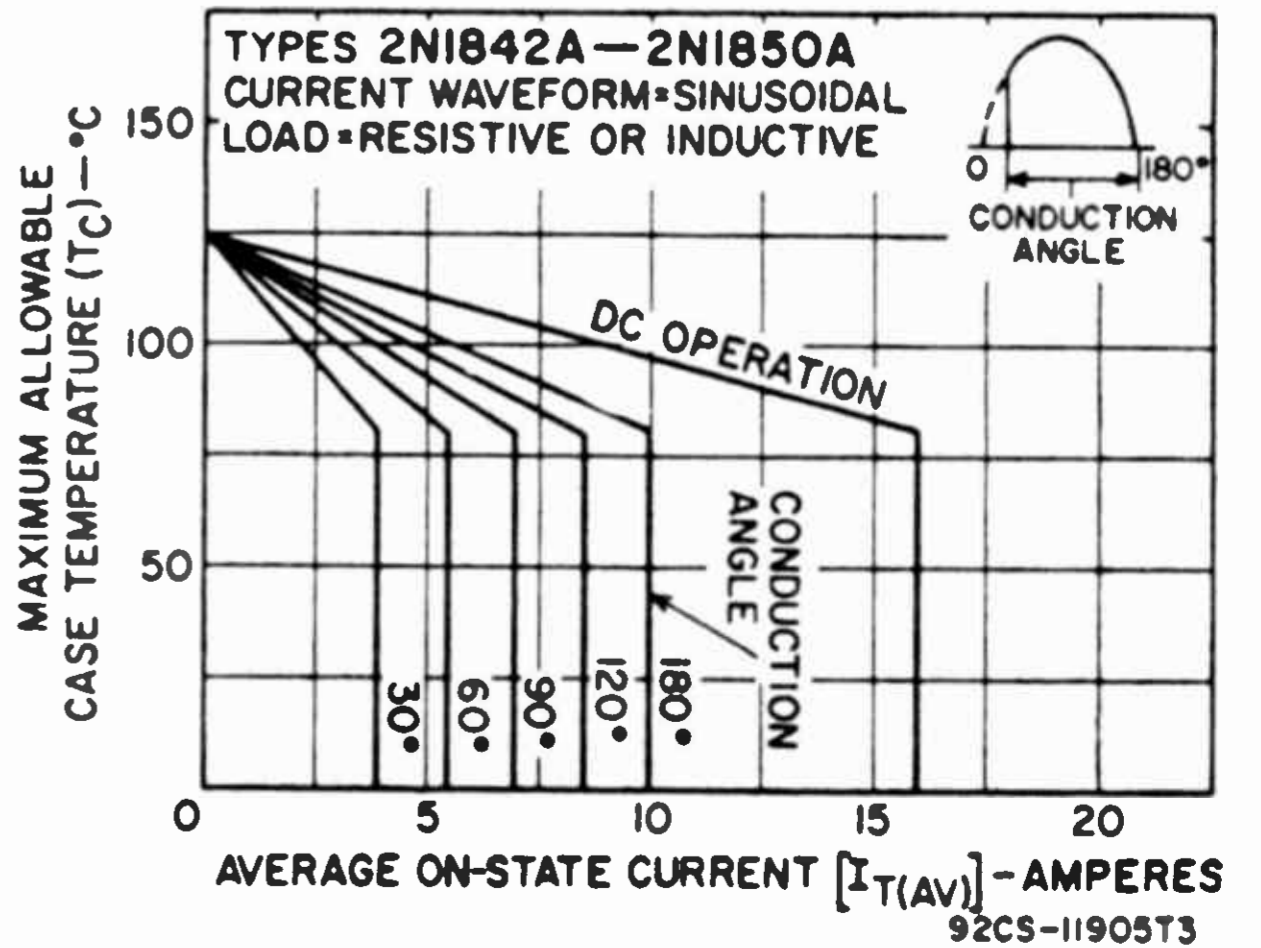
CHARACTERISTICS (At maximum electrical rating at $T_c = 125^{\circ}\text{C}$)

	2N1842A	2N1843A	2N1844A	2N1845A	2N1846A	2N1847A	2N1848A	2N1849A	2N1850A	
$V_{F(BO)O}$ (min)	25	50	100	150	200	250	300	400	500	V
I_{DOM} (max)	22.5	19	12.5	6.5	6	5.5	5	4	3	mA
I_{RROM} (max)	22.5	19	12.5	6.5	6	5.5	5	4	3	mA
V_T	1.2 ($T_c = 80^{\circ}\text{C}$)									V
I_{GT}	45									mA
V_{GT} (max)	3.5 ($T_c = -40^{\circ}\text{C}$)									V
V_{GT} (max)	3.7 ($T_c = -65^{\circ}\text{C}$)									V
V_{GT} (min)	0.25									V
V_{GT} (min)	0.3 ($T_c = 100^{\circ}\text{C}$)									V

GATE TRIGGER CURRENT CHARACTERISTICS

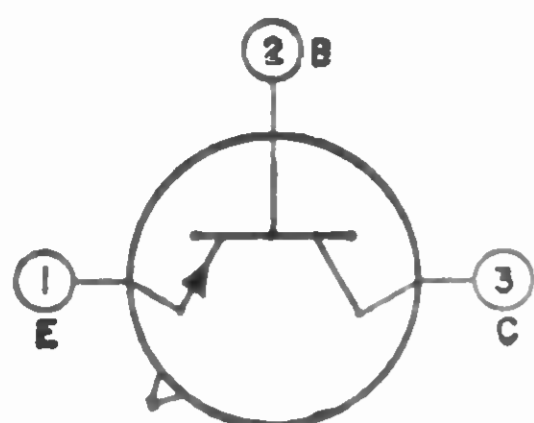


RATING CHART



CHARACTERISTICS (cont'd)

	2N1842A	2N1843A	2N1844A	2N1845A	2N1846A	2N1847A	2N1848A	2N1849A	2N1850A	
i_{HO}					8					mA
θ_{J-C}					2					°C/W



COMPUTER TRANSISTOR 2N1853

Ge p-n-p diffused-junction type used in switching applications in military and commercial data-processing equipment. JEDEC TO-5, Outline No.5.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-18	V
Collector-to-Emitter Voltage	V_{CEO}	-6	V
Emitter-to-Base Voltage*	V_{EBO}	-2	V
Collector Current	I_C	-100	mA
Transistor Dissipation:†			
T_A up to 25°C	P_T	150	mW
T_A above 25°C	P_T	See curve page 300	
Emitter-to-Base Dissipation (Under breakdown conditions with reverse bias)	P_T	25	mW
Ambient-Temperature Range:			
Operating (T_A) and Storage (T_{STG})	T_L	-55 to 85	°C
Lead-Soldering Temperature (10 s max)		235	°C

CHARACTERISTICS

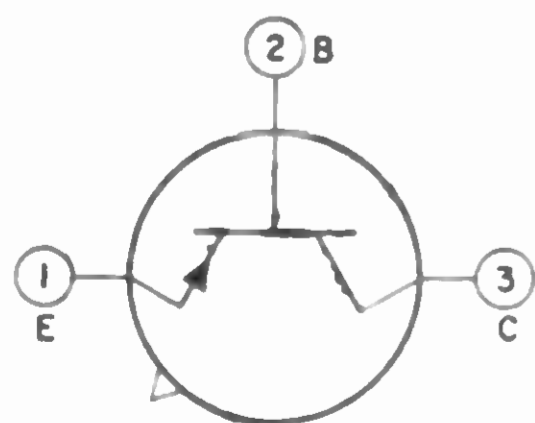
Collector-to-Base Breakdown Voltage ($I_C = -0.025$ mA, $I_E = 0$)	$V_{(BR)CBO}$	-18 min	V
Collector-to-Emitter Breakdown Voltage ($V_{BE} = 0.15$ V, $I_C = -0.025$ mA)	$V_{(BR)CEV}$	-18 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -0.1$ mA, $I_C = 0$)	$V_{(BR)EBO}$	-2 min	V
Collector-to-Emitter Saturation Voltage ($I_C = -6$ mA, $I_B = -0.2$ mA)	$V_{CE(sat)}$	-0.2 max	V
Base-to-Emitter Voltage ($I_C = -6$ mA, $I_B = -0.2$ mA)	V_{BE}	-0.4 max	V
Collector-Cutoff Current:			
$V_{CB} = -15$ V, $I_E = 0$, $T_A = 25^\circ\text{C}$	I_{CBO}	-4.2 max	µA
$V_{CB} = -18$ V, $I_E = 0$, $T_A = 60^\circ\text{C}$	I_{CBO}^\blacksquare	-35 max	µA
Emitter-Cutoff Current ($V_{EB} = -2$ V, $I_C = 0$)	I_{EBO}	-100 max	µA
Static Forward-Current Transfer Ratio:			
$V_{CE} = -1$ V, $I_B = -0.2$ mA	h_{FE}	30 to 400	
$V_{CE} = -0.4$ V, $I_C = -6$ mA	h_{FE}	30 min	
Storage Time $^\blacksquare$ ($V_{CC} = -15$ V, $R_G = 100$ Ω)	t_s	0.8 max	µS
Turn-On Time $^\blacksquare$ ($V_{CC} = -15$ V, $R_G = 100$ Ω)	$t_d + t_r$	0.8 max	µS
Turn-Off Time $^\blacksquare$ ($V_{CC} = -15$ V, $R_G = 100$ Ω)	$t_s + t_f$	0.9 max	µS

* This rating may be exceeded and the emitter-to-base junction operated in the breakdown condition provided the emitter-to-base dissipation is limited to 25 milliwatts at 25°C. For ambient temperatures above 25°C, reduce the dissipation.

† For higher dissipation values in switching applications under transient operating conditions, the maximum dissipation can be computed by utilization of the method described in RCA Application Note "Transistor Dissipation Ratings for Pulse and Switching Service" (AN-181).

■ This characteristic applies only to type 2N1853.

COMPUTER TRANSISTOR 2N1854



Ge p-n-p diffused-junction type used in switching applications in military and commercial data-processing equipment. JEDEC TO-5, Outline No.5. This type is identical with type 2N1853 except for the following items:

CHARACTERISTICS

Collector-to-Emitter Breakdown Voltage ($V_{BE} = 0.2$ V, $I_C = -0.025$ mA)	$V_{(BR)CEV}$	-18 min	V
Collector-to-Emitter Saturation Voltage:			
$I_C = -20$ mA, $I_B = -0.66$ mA	$V_{CE(sat)}$	-0.25 max	V
$I_C = -20$ mA, $I_B = -0.5$ mA	$V_{CE(sat)}$	-0.3	V
$I_C = -80$ mA, $I_B = -2.7$ mA	$V_{CE(sat)}$	-0.7 max	V

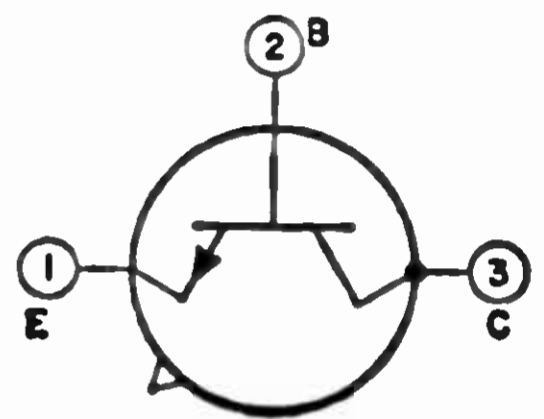
CHARACTERISTICS (cont'd)

Base-to-Emitter Voltage ($I_C = -20$ mA, $I_B = -0.5$ mA)	V_{BE}	-0.8 max	V
Collector-to-Emitter Latching Voltage ($V_{CC} = -18$ V, $R_{BE} = 1$ k Ω , $R_L = 178$ Ω)	V_{CERL}	-17 min	V
Collector-Cutoff Current: $V_{CB} = -15$ V, $I_E = 0$, $T_A = 65^\circ\text{C}$	I_{CBO}	-40 max	μA
Static Forward-Current Transfer Ratio: $V_{CE} = -1$ V, $I_C = -50$ mA	h_{FE}	400 max	
$V_{CE} = -0.5$ V, $I_C = -20$ mA	h_{FE}	40 min	
$V_{CE} = -0.75$ V, $I_C = -100$ mA	h_{FE}	25 min	
Gain-Bandwidth Product ($V_{CE} = -1$ V, $I_C = -10$ mA, $h_{re} = 5$)	f_T	40 min	MHz
Output Capacitance ($V_{CB} = -10$ V, $I_E = 0$, $f = 140$ kHz)	C_{obo}	12 max	pF
Charge Storage Time: $I_C = -20$ mA, $I_{B1} = -1.5$ mA, $V_{CC} = -15$ V, $R_L = 750$ Ω	t_{Q_s}	60 max	ns
$I_C = -80$ mA, $I_{B1} = -4.5$ mA, $V_{CC} = -15$ V, $R_L = 750$ Ω	t_{Q_s}	80 max	ns

2N1893

TRANSISTOR

Si n-p-n triple-diffused planar type used in small-signal and medium-power applications in industrial and military equipment. JEDEC TO-5, Outline No.5. This type is identical with type 2N2405 except for the following items:

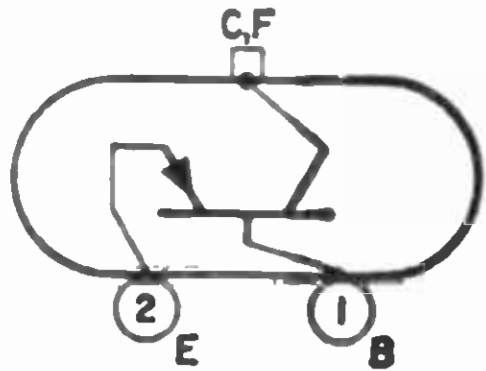


MAXIMUM RATINGS

Collector-to-Emitter Voltage: $R_{BE} \leq 10$ Ω	V_{CER}	100	V
Base open	V_{CEO}	80	V
Collector Current	I_C	0.5	A
Transistor Dissipation: T_A up to 25°C	P_T	0.8	W
T_C up to 25°C	P_T	3	W
T_A or T_C above 25°C	P_T	See curve page 300	
Temperature Range: Operating (Junction)	T_J (opr)	-65 to 200	$^\circ\text{C}$
Storage	T_{STG}	-65 to 200	$^\circ\text{C}$

CHARACTERISTICS

Collector-to-Emitter Sustaining Voltage: $I_C = 30$ mA, $I_B = 0$, $t_p = 300$ μs , $df = 1.8\%$	$V_{CEO}(\text{sus})$	80 min	V
$I_C = 100$ mA, $R_{BE} = 10$ Ω , $t_p = 300$ μs , $df = 1.8\%$...	$V_{CER}(\text{sus})$	100 min	V
Collector-to-Emitter Saturation Voltage: $I_C = 150$ mA, $I_B = 15$ mA	$V_{CE}(\text{sat})$	5 max	V
$I_C = 50$ mA, $I_B = 5$ mA	$V_{CE}(\text{sat})$	1.2 max	V
Base-to-Emitter Saturation Voltage ($I_C = 150$ mA, $I_B = 15$ mA)	$V_{BE}(\text{sat})$	1.3 max	V
Collector-Cutoff Current ($V_{CB} = 90$ V, $I_E = 0$, $T_C = 150^\circ\text{C}$)	I_{CBO}	15 max	μA
Small-Signal Forward-Current Transfer Ratio: $V_{CE} = 5$ V, $I_C = 1$ mA, $f = 1$ kHz	h_{fe}	30 to 100	
$V_{CE} = 10$ V, $I_C = 50$ mA, $f = 20$ MHz	h_{fe}	2.5 min	
Static Forward-Current Transfer Ratio ($V_{CE} = 10$ V, $I_C = 0.1$ mA)	h_{FE}	20 min	
Pulsed Static Forward-Current Transfer Ratio ($V_{CE} = 10$ V, $I_C = 150$ mA, $t_p = 300$ μs , $df = 1.8\%$) ..	h_{FE} (pulsed)	40 to 120	
Gain-Bandwidth Product	f_T	50 min	MHz
Input Capacitance ($V_{EB} = 0.5$ V, $I_C = 0$)	C_{ibo}	85 max	pF
Input Resistance ($V_{CB} = 5$ V, $I_C = 1$ mA, $f = 1$ kHz)	h_{ib}	20 to 30	Ω
Voltage-Feedback Ratio: $V_{CB} = 5$ V, $I_C = 1$ mA, $f = 1$ kHz	h_{rb}	1.25×10^{-4} max	
$V_{CB} = 10$ V, $I_C = 5$ mA, $f = 1$ kHz	h_{rb}	1.5×10^{-4} max	
Thermal Resistance, Junction-to-Case	θ_{J-C}	58.3 max	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	219 max	$^\circ\text{C/W}$



POWER TRANSISTOR

2N1905

Ge p-n-p drift-field type intended for use in power-switching circuits, dc-to-dc converters, inverters, ultrasonic oscillators, and large-signal wide-band linear amplifiers. Similar to JEDEC TO-3, Outline No.4.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-100	V
Collector-to-Emitter Voltage	V_{CEO}	-50	V
Emitter-to-Base Voltage	V_{EBO}	-1.5*	V
Collector Current	I_C	-6	A
Emitter Current	I_E	6	A
Base Current	I_B	-1	A
Transistor Dissipation:			
T_{MF} up to 55°C	P_T	30	W
T_{MF} above 55°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 100	°C
Storage	T_{STG}	-65 to 100	°C
Pin-Soldering Temperature (10 s max)	T_P	255	°C

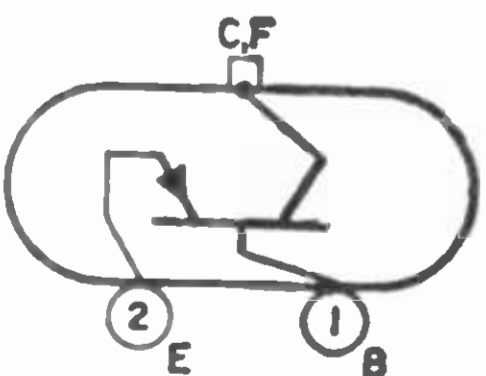
CHARACTERISTICS (At mounting-flange temperature = 25°C)

Collector-to-Base Breakdown Voltage ($I_C = -10$ mA, $I_E = 0$)	$V_{(BR)CBO}$	-100 min	V
Collector-to-Emitter Breakdown Voltage ($I_C = -100$ mA, $I_B = 0$)	$V_{(BR)CEO}$	-50 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 5$ mA, $I_C = 0$)	$V_{(BR)EBO}$	-1.5 min	V
Collector-to-Emitter Saturation Voltage ($I_C = -5$ A, $I_B = 0.25$ A)	$V_{CE(sat)}$	-1 max	V
Base-to-Emitter Voltage ($V_{CE} = -2$ V, $I_C = -1$ A) ...	V_{BE}	-0.38 typ; -0.5 max	V
Collector-Cutoff Current ($V_{CB} = 40$ V, $I_E = 0$)	I_{CBO}	-1 max	mA
Emitter-Cutoff Current ($V_{EB} = -0.5$ V, $I_C = 0$)	I_{EBO}	-1 max	mA
Static Forward-Current Transfer Ratio:			
$V_{CE} = -2$ V, $I_C = -5$ A	h_{FE}	30 min	
$V_{CE} = -2$ V, $I_C = -1$ A	h_{FE}	50 to 150	
Collector-Cutoff Saturation Current ($V_{CB} = -0.5$ V, $I_E = 0$)	$I_{CBO(sat)}$	-100	μ A
Gain-Bandwidth Product ($V_{CE} = -5$ V, $I_C = -0.5$ A)	f_T	2 min	MHz
Thermal Resistance, Junction-to-Case	θ_{J-C}	1.5 max	°C/W

* This value may be exceeded provided that the power dissipated in the emitter under breakdown conditions is limited to 5 watts.

POWER TRANSISTOR

2N1906



Ge p-n-p drift-field type used in power-switching circuits, dc-to-dc converters, inverters, ultrasonic oscillators, and large-signal wide-band linear amplifiers. Similar to JEDEC TO-3, Outline No.4. This type is identical with type 2N1905 except for the following items.

MAXIMUM RATINGS

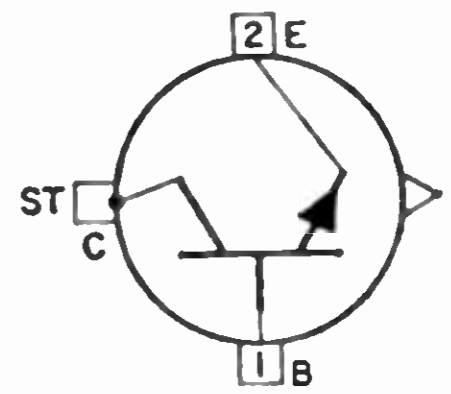
Collector-to-Base Voltage	V_{CBO}	-130	V
Collector-to-Emitter Voltage	V_{CEO}	-60	V

CHARACTERISTICS (At mounting-flange temperature = 25°C)

Collector-to-Emitter Saturation Voltage ($I_C = -5$ A, $I_B = -0.25$ A)	$V_{CE(sat)}$	-0.5 max	V
Base-to-Emitter Voltage:			
$V_{CE} = -2$ V, $I_C = -1$ A	V_{BE}	-0.5 max	V
$V_{CE} = -2$ V, $I_C = -5$ A	V_{BE}	-0.9 max	V
Static Forward-Current Transfer Ratio:			
$V_{CE} = -2$ V, $I_C = -5$ A	h_{FE}	75 max	
$V_{CE} = -2$ V, $I_C = -1$ A	h_{FE}	75 to 250	
Gain Bandwidth Product ($V_{CE} = -5$ V, $I_C = -0.5$ A)	f_T	3 min	MHz

2N2015 POWER TRANSISTOR

Si n-p-n diffused-junction type used in dc-to-dc converter, inverter, chopper, relay-control, oscillator, regulator, pulse-amplifier circuits; and class A and class B push-pull amplifiers for af and servo amplifier applications. JEDEC TO-36, Outline No.14. See Mounting Hardware for desired mounting arrangement.



MAXIMUM RATINGS

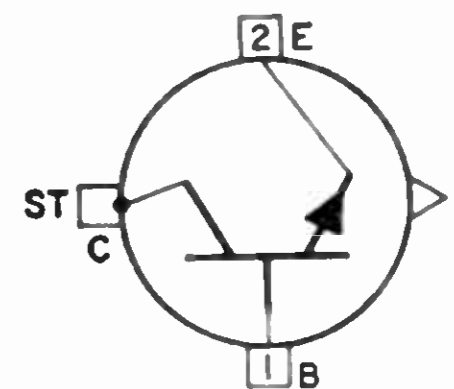
Collector-to-Base Voltage	V_{CB0}	100	V
Collector-to-Emitter Voltage	V_{CE0}	50	V
Emitter-to-Base Voltage	V_{EB0}	10	V
Collector Current	I_C	10	A
Emitter Current	I_E	-13	A
Base Current	I_B	6	A
Transistor Dissipation:			
T_c up to 25°C	P_T	150	W
T_c above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (T_c) and Storage (T_{STG})		-65 to 200	°C
Lug-Soldering Temperature (10 s max)	$T(lug)$	235	°C

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Voltage ($V_{BE} = -1.5$ V, $I_C = 2$ mA)	V_{CEV}	100 min	V
Collector-to-Emitter Sustaining Voltage ($I_C = 200$ mA, $I_B = 0$)	$V_{CE0(sus)}$	50 min	V
Collector-to-Emitter Voltage ($I_C = 5$ A, $I_B = 0.5$ A)	$V_{CE(sat)}$	1.25 max	V
Base-to-Emitter Voltage ($V_{CE} = 4$ V, $I_C = 5$ A)	V_{BE}	2.2 max	V
Collector-Cutoff Current:			
$V_{CE} = 40$ V, $I_B = 0$	I_{CE0}	0.2 max	mA
$V_{CE} = 100$ V, $V_{BE} = -1.5$ V	I_{CEV}	2 max	mA
$V_{CE} = 30$ V, $V_{BE} = -1.5$ V, $T_c = 150^\circ\text{C}$	I_{CEV}	2 max	mA
Emitter-Cutoff Current ($V_{EB} = 10$ V, $I_C = 0$)	I_{EBO}	0.05 max	mA
Static Forward-Current Transfer Ratio:			
$V_{CE} = 4$ V, $I_C = 5$ A	h_{FE}	15 to 50	
$V_{CE} = 4$ V, $I_C = 10$ A	h_{FE}	7.5 min	
Small-Signal Forward-Current Transfer Ratio			
($V_{CE} = 4$ V, $I_C = 1$ A, $f = 1$ kHz)	h_{fe}	12 to 60	
Small-Signal Forward-Current Transfer-Ratio Cutoff			
Frequency ($V_{CE} = 4$ V, $I_C = 5$ A)	f_{hfe}	12 min	kHz
Collector-to-Emitter Saturation Resistance			
($I_C = 5$ A, $I_B = 0.5$ A)	$r_{CE(sat)}$	0.25 max	Ω
Output Capacitance ($V_{CB} = 40$ V, $I_C = 50$ μA , $f = 1$ MHz)			
	C_{ob0}	400 max	pF
Thermal Resistance, Junction-to-Case			
	θ_{J-C}	1.17 max	°C/W

2N2016 POWER TRANSISTOR

Si n-p-n diffused-junction type used in dc-to-dc converter, inverter, chopper, relay-control, oscillator, regulator, and pulse-amplifier circuits; and class A and class B push-pull amplifiers for af and servo amplifier applications. JEDEC TO-36, Outline No.14. See Mounting Hardware for desired mounting arrangement. This type is identical with type 2N2015 except for the following items:



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CB0}	130	V
Collector-to-Emitter Voltage	V_{CE0}	65	V

CHARACTERISTICS (At case temperature = 25°C)

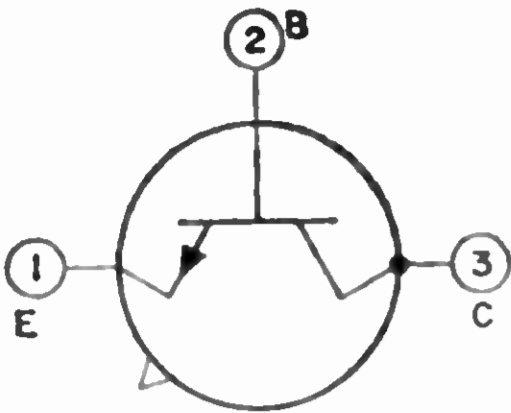
Collector-to-Emitter Voltage ($V_{BE} = -1.5$ V, $I_C = 2$ mA)	V_{CEV}	130 min	V
Collector-to-Emitter Sustaining Voltage ($I_C = 200$ mA, $I_B = 0$)	$V_{CE0(sus)}$	65 min	V

CHARACTERISTICS (cont'd)

Collector-Cutoff Current ($V_{CE} = 130 \text{ V}$,
 $V_{BE} = -1.5 \text{ V}$) I_{CEV} 2 max mA

TRANSISTOR

2N2102



Si n-p-n triple-diffused planar type used in small-signal and medium-power applications in industrial and military equipment. This type features exceptionally low-noise low-leakage characteristics, high switching speed, and high pulse h_{FE} . JEDEC TO-5, Outline No.5.

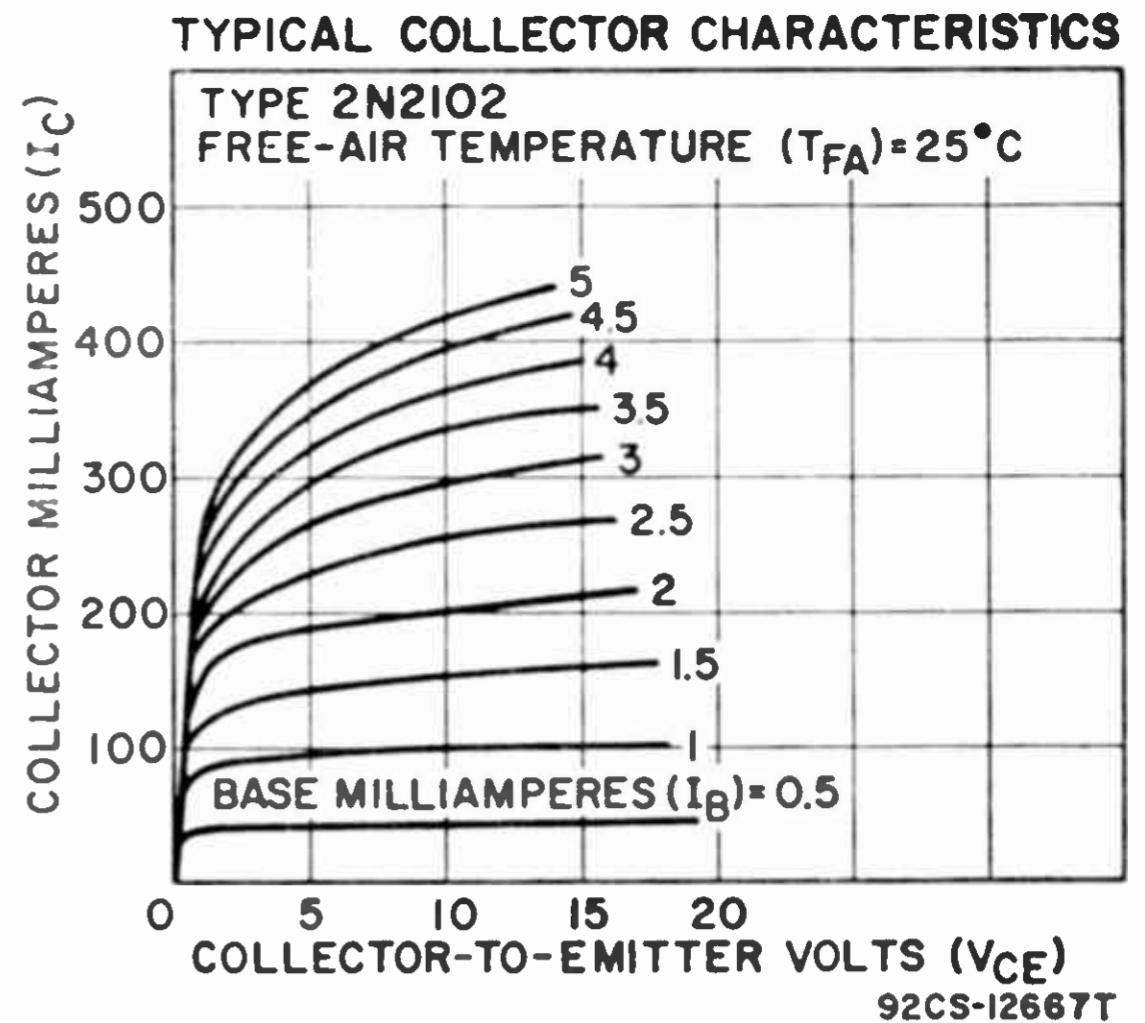
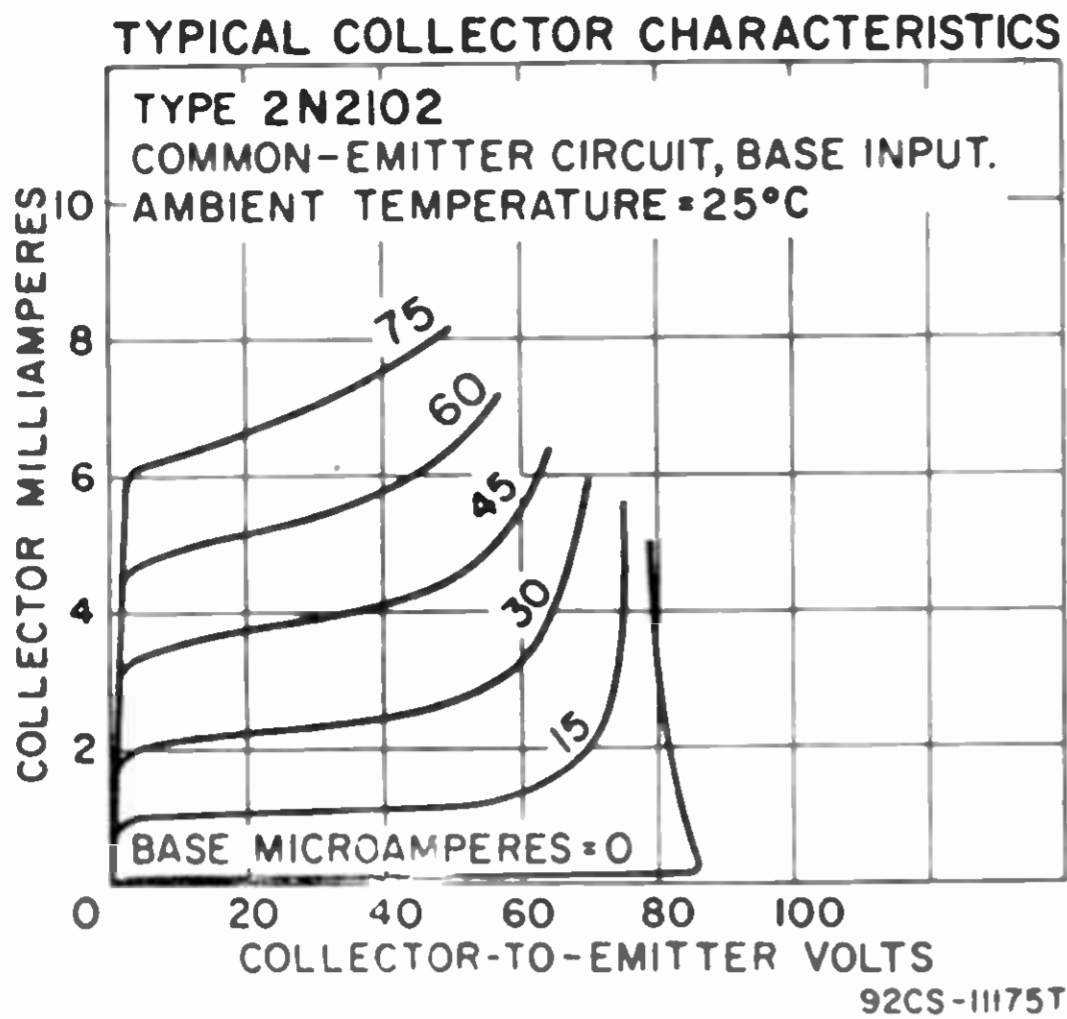
MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	120	V
Collector-to-Emitter Voltage: $R_{BE} \leq 10 \Omega$	V_{CER}	80	V
Base open	V_{CEO}	65*	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Collector Current	I_C	1	A
Transistor Dissipation: T_A up to 25°C	P_T	1	W
T_C up to 25°C	P_T	5	W
T_A or T_C above 25°C	P_T	See curve page 300	
Temperature Range: Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 300	°C
Lead-Soldering Temperature (10 s max)	T_L	300	°C

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Base Breakdown Voltage ($I_C = 0.1 \text{ mA}$, $I_E = 0$)	$V_{(BR)CBO}$	120 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.1 \text{ mA}$, $I_C = 0$)	$V_{(BR)EBO}$	7 min	V
Collector-to-Emitter Sustaining Voltage: $I_C = 100 \text{ mA}$, $R_{BE} = 10 \Omega$, $t_p = 300 \mu s$, $df = 1.8\%$	$V_{CER(SUS)}$	80 min	V
$I_C = 100 \text{ mA}$, $I_B = 0$, $t_p = 300 \mu s$, $df = 1.8\%$	$V_{CEO(SUS)}$	65* min	V
Collector-to-Emitter Saturation Voltage ($I_C = 150 \text{ mA}$, $I_B = 15 \text{ mA}$, $t_p = 300 \mu s$, $df = 1.8\%$)	$V_{CE(sat)}$	0.5 max	V
Base-to-Emitter Saturation Voltage ($I_C = 150 \text{ mA}$, $I_B = 15 \text{ mA}$, $t_p = 300 \mu s$, $df = 1.8\%$)	$V_{BE(sat)}$	1.1 max	V
Collector-Cutoff Current: $V_{CB} = 60 \text{ V}$, $I_E = 0$, $T_A = 25^\circ C$	I_{CBO}	0.002 max	μA
$V_{CB} = 60 \text{ V}$, $I_E = 0$, $T_A = 150^\circ C$	I_{CBO}	2 max	μA
Emitter-Cutoff Current ($V_{EB} = 5 \text{ V}$, $I_C = 0$)	I_{EBO}	0.005 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 10 \text{ V}$, $I_C = 0.01 \text{ mA}$, $T_C = 25^\circ C$)	h_{FE}	10* min	
Pulsed Static Forward-Current Transfer Ratio $V_{CE} = 10 \text{ V}$, $I_C = 150 \text{ mA}$, $T_C = 25^\circ C$, $t_p = 300 \mu s$, $df = 1.8\%$	$h_{FE}(\text{pulsed})$	40 to 120	
$V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$, $T_C = 25^\circ C$, $t_p = 300 \mu s$, $df = 1.8\%$	$h_{FE}(\text{pulsed})$	10* min	
$V_{CE} = 10 \text{ V}$, $I_C = 10 \text{ mA}$, $T_C = -55^\circ C$, $t_p = 300 \mu s$, $df = 1.8\%$	$h_{FE}(\text{pulsed})$	20 min	
Small-Signal Forward-Current Transfer Ratio: $V_{CE} = 5 \text{ V}$, $I_C = 1 \text{ mA}$, $f = 1 \text{ kHz}$	h_{fe}	40 to 125	
$V_{CE} = 10 \text{ V}$, $I_C = 5 \text{ mA}$, $f = 1 \text{ kHz}$	h_{fe}	45 to 190	
$V_{CE} = 10 \text{ V}$, $I_C = 50 \text{ mA}$, $f = 20 \text{ MHz}$	h_{fe}	6 min	
Input Capacitance ($V_{EB} = 0.5 \text{ V}$, $I_C = 0$)	C_{ibo}	80 max	pF
Output Capacitance ($V_{CB} = 10 \text{ V}$, $I_C = 0$)	C_{obo}	15 max	pF
Input Resistance: $V_{CB} = 5 \text{ V}$, $I_C = 1 \text{ mA}$, $f = 1 \text{ kHz}$	h_{ib}	24 to 34	Ω
$V_{CB} = 10 \text{ V}$, $I_C = 5 \text{ mA}$, $f = 1 \text{ kHz}$	h_{ib}	4 to 8	Ω
Small-Signal Reverse-Voltage (Feedback) Transfer Ratio: $V_{CB} = 5 \text{ V}$, $I_C = 1 \text{ mA}$, $f = 1 \text{ kHz}$	h_{rb}	3×10^{-4} max	
$V_{CB} = 10 \text{ V}$, $I_C = 5 \text{ mA}$, $f = 1 \text{ kHz}$	h_{rb}	3×10^{-4} max	
Output Conductance: $V_{CB} = 5 \text{ V}$, $I_C = 1 \text{ mA}$, $f = 1 \text{ kHz}$	h_{ob}	0.1 to 0.5	μmho
$V_{CB} = 10 \text{ V}$, $I_C = 5 \text{ mA}$, $f = 1 \text{ kHz}$	h_{ob}	0.1 to 1	μmho
Noise Figure ($V_{CE} = 10 \text{ V}$, $I_C = 0.3 \text{ mA}$, $f = 1 \text{ kHz}$, $R_G = 510 \Omega$, circuit bandwidth = 1 Hz)	NF	6 max	dB
Thermal Resistance, Junction-to-Case	θ_{J-C}	35 max	°C/W
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	175 max	°C/W

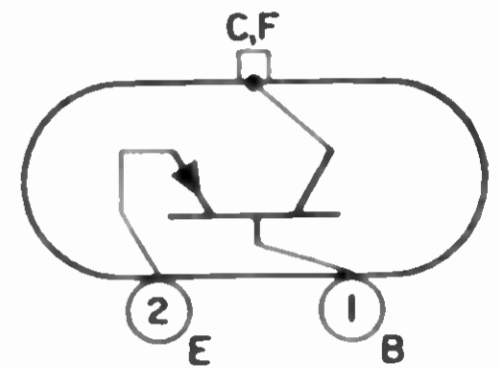
* This value applies only to type 2N2102.



2N2147

POWER TRANSISTOR

Ge p-n-p drift-field type used in high-fidelity amplifiers where wide frequency range and low distortion are required. JEDEC TO-3, Outline No.2.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-75	V
Collector-to-Emitter Voltage	V_{CEO}	-50	V
Emitter-to-Base Voltage*	V_{EBO}	-1.5	V
Collector Current	I_C	-5	A
Emitter Current	I_E	5	A
Base Current	I_B	-1	A
Transistor Dissipation:			
T_{MF} up to 81°C	P_T	12.5	W
T_{MF} above 81°C	P_T	Derate linearly 0.66	W/°C
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 100	°C
Storage	T_{STG}	-65 to 100	°C
Pin-Soldering Temperature (10 s max)	T_P	255	°C

* This rating may be exceeded provided the combined dissipation in the emitter and collector does not exceed the maximum dissipation rating for the device.

CHARACTERISTICS (At mounting-flange temperature = 25°C)

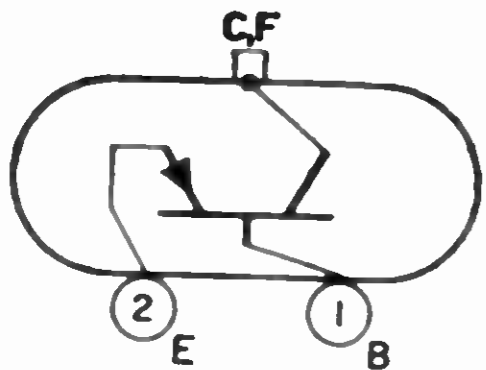
Collector-to-Base Breakdown Voltage ($I_C = -10$ mA, $I_E = 0$, $t_p = 300 \mu s$, $df = 0.01\%$)	$V_{(BR)CBO}$	-75 min	V
Collector-to-Emitter Sustaining Voltage ($I_C = -100$ mA, $I_B = 0$)	$V_{CEO(sus)}$	-50 min	V
Collector-to-Emitter Saturation Voltage ($I_B = -250$ mA, $I_C = -5$ A)	$V_{CE(sat)}$	-0.6 max	V
Base-to-Emitter Voltage:			
$V_{CE} = -10$ V, $I_C = -50$ mA	V_{BE}	-0.2 to -0.27	V
$V_{CE} = -2$ V, $I_C = 1$ A	V_{BE}	-0.5 max	V
Collector-Cutoff Current ($V_{CB} = -40$ V, $I_E = 0$)	I_{CBO}	-1 max	mA
Collector-Cutoff Saturation Current ($V_{CB} = -0.5$ V, $I_E = 0$)	$I_{CBO(sat)}$	-70 max	μA
Emitter-Cutoff Current ($V_{EB} = -1.5$ V, $I_C = 0$)	I_{EBO}	-2.5 max	mA
Static Forward-Current Transfer Ratio			
$V_{CE} = -2$ V, $I_C = -1$ A	h_{FE}	100 to 300	
$V_{CE} = -2$ V, $I_C = -4$ A	h_{FE}	75 min	
Gain-Bandwidth Product ($V_{CE} = -5$ V, $I_C = -500$ mA)	f_T	3 min; 4 typ	MHz
Thermal Resistance, Junction-to-Case	θ_{J-C}	1.5 max	°C/W

TYPICAL OPERATION IN "SINGLE-ENDED PUSH-PULL" CLASS B AF-AMPLIFIER CIRCUIT (At mounting-flange temperature = 25°C)

DC Collector Supply Voltage	V_{CC}	-22	V
Zero-Signal DC Collector Current	I_C	-0.035	A
Zero-Signal Base-Bias Voltage		-0.24	V
Peak Collector Current	$i_C(\text{peak})$	-3.5	A
Maximum-Signal DC Collector Current	$I_C(\text{max})$	-1.1	A
Input Impedance of Stage (per base)		75	Ω

TYPICAL OPERATION (cont'd)

Load Impedance (speaker voice-coil)	R_L	4	Ω
Maximum Collector Dissipation (per transistor) under worst-case conditions		12.5	W
EIA Music Power Output Rating		45	W
Power Gain		33	dB
Maximum-Signal Power Output	P_{OEB}	25	W
Total Harmonic Distortion at Maximum-Signal Power Output		5	%



POWER TRANSISTOR

2N2148

Ge p-n-p drift-field type used in high-fidelity amplifiers where wide frequency range and low distortion are required. JEDEC TO-3, Outline No.2. This type is identical with type 2N2147 except for the following items:

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-60	V
Collector-to-Emitter Voltage	V_{CEO}	-40	V

CHARACTERISTICS (At mounting-flange temperature = 25°C)

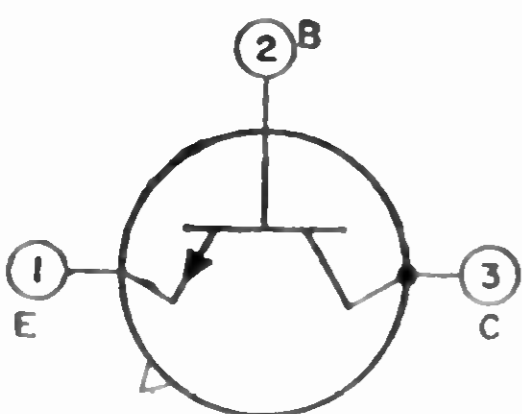
Collector-to-Base Breakdown Voltage ($I_C = -10$ mA, $I_E = 0$)	$V_{(BR)CBO}$	-60 min	V
Collector-to-Emitter Sustaining Voltage ($I_C = -100$ mA, $I_B = 0$)	$V_{CEO(sus)}$	-40 min	V
Collector-to-Emitter Saturation Voltage ($I_C = -5$ mA, $I_B = -250$ mA)	$V_{CE(sat)}$	-0.75 max	V
Base-to-Emitter Voltage ($V_{CE} = -10$ V, $I_C = -50$ mA)	V_{BE}	-0.21 to -0.28	V
Collector-Cutoff Saturation Current ($V_{CB} = -0.5$ V, $I_E = 0$)	$I_{CBO(sat)}$	-100 max	μA
Emitter-Cutoff Current ($V_{EB} = -1.5$ V, $I_C = 0$)	I_{EBO}	-10 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = -2$ V, $I_C = -1$ A)	h_{FE}	60 min	
Gain-Bandwidth Product ($V_{CE} = -5$ V, $I_C = -500$ mA)	f_T	3 min; 4 typ	MHz

Refer to Chart of Discontinued Transistors

2N2205

Refer to Chart of Discontinued Transistors

2N2206



TRANSISTOR

2N2270

Si n-p-n triple-diffused planar type used in rf-amplifiers, mixers, oscillators, and converters, and in af small-signal and power amplifiers. JEDEC TO-5, Outline No.5.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	60	V
Collector-to-Emitter Voltage: $R_{BE} \leq 10 \Omega$	V_{CER}	60	V
Base open	V_{CEO}	45	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Collector Current	I_C	1	A
Transistor Dissipation: T_A up to 25°C	P_T	1	W
T_C up to 25°C	P_T	5	W
T_A or T_C above 25°C	P_T	See curve page 300	
Temperature Range: Operating (Junction)	$T_J(opr)$	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	255	°C

CHARACTERISTICS (At case temperature = 25°C)

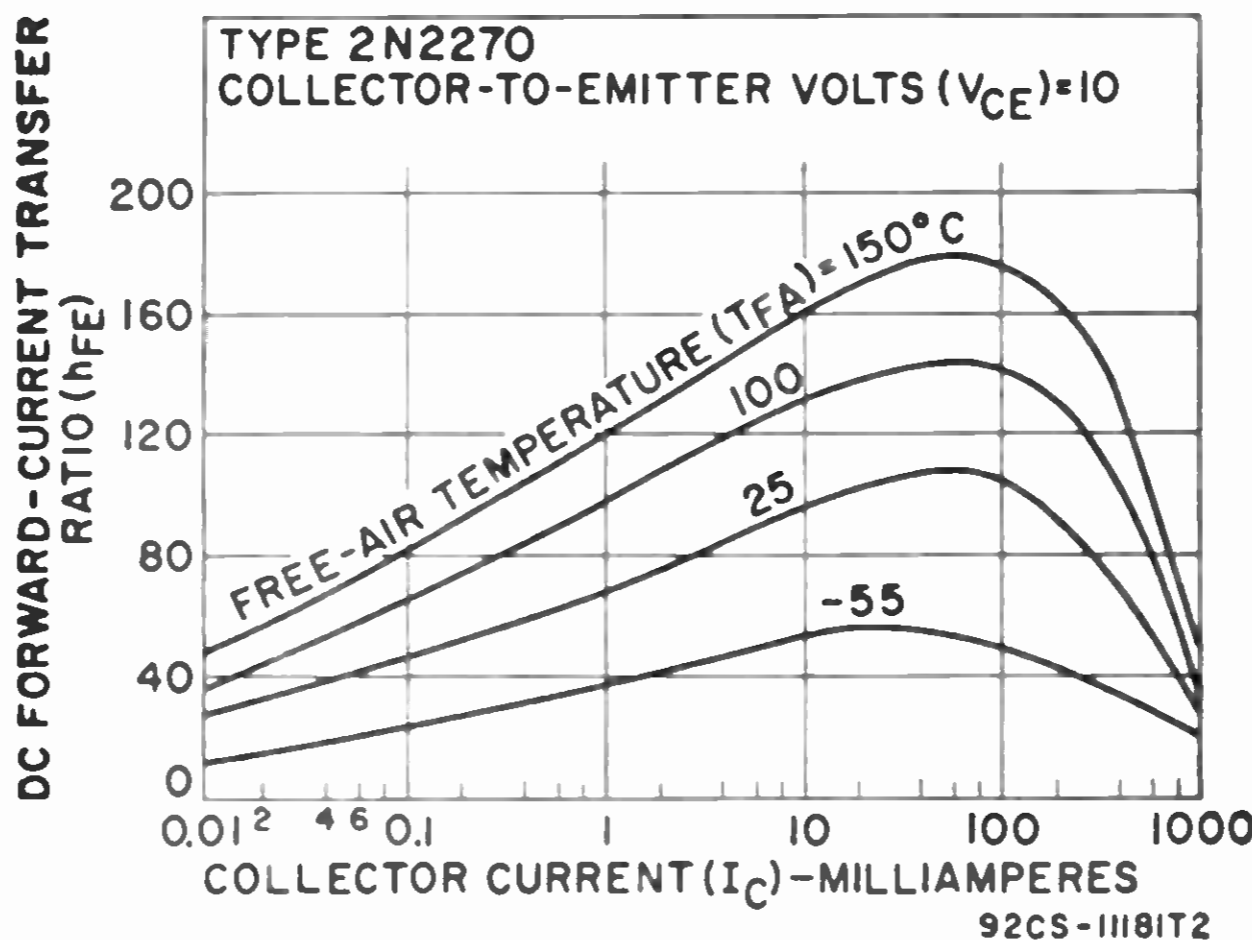
Collector-to-Base Breakdown Voltage ($I_C = 0.1$ mA, $I_E = 0$)	$V_{(BR)CBO}$	60 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.1$ mA, $I_C = 0$)	$V_{(BR)EBO}$	7 min	V

CHARACTERISTICS (cont'd)

Collector-to-Emitter Sustaining Voltage:

$I_C = 100\text{ mA}$, $t_p = 300\ \mu\text{s}$, $df = 1.8\%$	$V_{CEO}\text{ (SUS)}$	45 min	V
$I_C = 100\text{ mA}$, $R_{BE} = 10\ \Omega$, $t_p = 300\ \mu\text{s}$, $df = 1.8\%$...	$V_{CER}\text{ (SUS)}$	60 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 150\text{ mA}$, $I_B = 15\text{ mA}$)	$V_{CE}\text{ (sat)}$	0.9 max	V
Base-to-Emitter Saturation Voltage ($I_C = 150\text{ mA}$, $I_B = 15\text{ mA}$)	$V_{BE}\text{ (sat)}$	1.2 max	V
Collector-Cutoff Current: $V_{CB} = 60\text{ V}$, $I_E = 0$, $T_C = 25^\circ\text{C}$	I_{CBO}	0.1 max	μA
$V_{CB} = 60\text{ V}$, $I_E = 0$, $T_C = 150^\circ\text{C}$	I_{CBO}	50 max	μA
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$, $I_C = 0$)	I_{EBO}	0.1 max	μA
Pulsed Static Forward-Current Transfer Ratio: ($V_{CE} = 10\text{ V}$, $I_C = 150\text{ mA}$, $t_p = 300\ \mu\text{s}$, $df = 1.8\%$)	$h_{FE}\text{ (pulsed)}$	50 to 200	
Static Forward-Current Transfer Ratio ($V_{CE} = 10\text{ V}$, $I_C = 1\text{ mA}$)	h_{FE}	35 min	
Small-Signal Forward-Current Transfer Ratio: $V_{CE} = 10\text{ V}$, $I_C = 5\text{ mA}$, $f = 1\text{ kHz}$	h_{fe}	30 to 180	
$V_{CE} = 10\text{ V}$, $I_C = 50\text{ mA}$, $f = 20\text{ MHz}$	h_{fe}	3 min	
Input Capacitance ($V_{EB} = 0.5\text{ V}$, $I_C = 0$)	C_{ibo}	80 max	pF
Output Capacitance ($V_{CB} = 10\text{ V}$, $I_E = 0$)	C_{obo}	15 max	pF
Thermal Resistance, Junction-to-Case	θ_{J-C}	35 max	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	175 max	$^\circ\text{C/W}$

TYPICAL DC FORWARD-CURRENT TRANSFER-RATIO CHARACTERISTICS



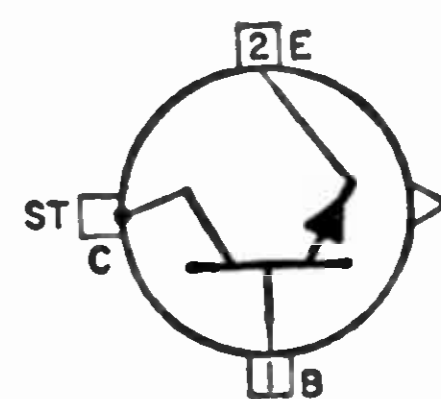
2N2273

Refer to Chart of Discontinued Transistors

2N2338

POWER TRANSISTOR

Si n-p-n diffused-junction type used in dc-to-dc converters, inverters, choppers, and relay-control circuits; in oscillators and voltage- and current-regulator circuits; and in dc and servo-amplifier circuits. JEDEC TO-36, Outline No.14. See Mounting Hardware for desired mounting arrangement.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	60	V
Collector-to-Emitter Voltage: $V_{BE} = -1.5\text{ V}$	V_{CEV}	60	V
Base open	V_{CEO}	40	V
Emitter-to-Base Voltage	V_{EBO}	6	V
Collector Current	I_C	7.5	A
Base Current	I_B	5	A
Transistor Dissipation: T_C up to 25°C	P_T	150	W
T_C above 25°C	P_T	See curve page 300	
Temperature Range: Operating (Junction)	$T_J\text{ (opr)}$	-65 to 200	$^\circ\text{C}$
Storage	T_{STG}	-65 to 200	$^\circ\text{C}$
Lug-Soldering Temperature (10 s max)	$T\text{ (lug)}$	235	$^\circ\text{C}$

CHARACTERISTICS

Collector-to-Emitter Voltage ($V_{BE} = -1.5\text{ V}$, $I_C = 2\text{ mA}$)	V_{CEV}	60 min	V
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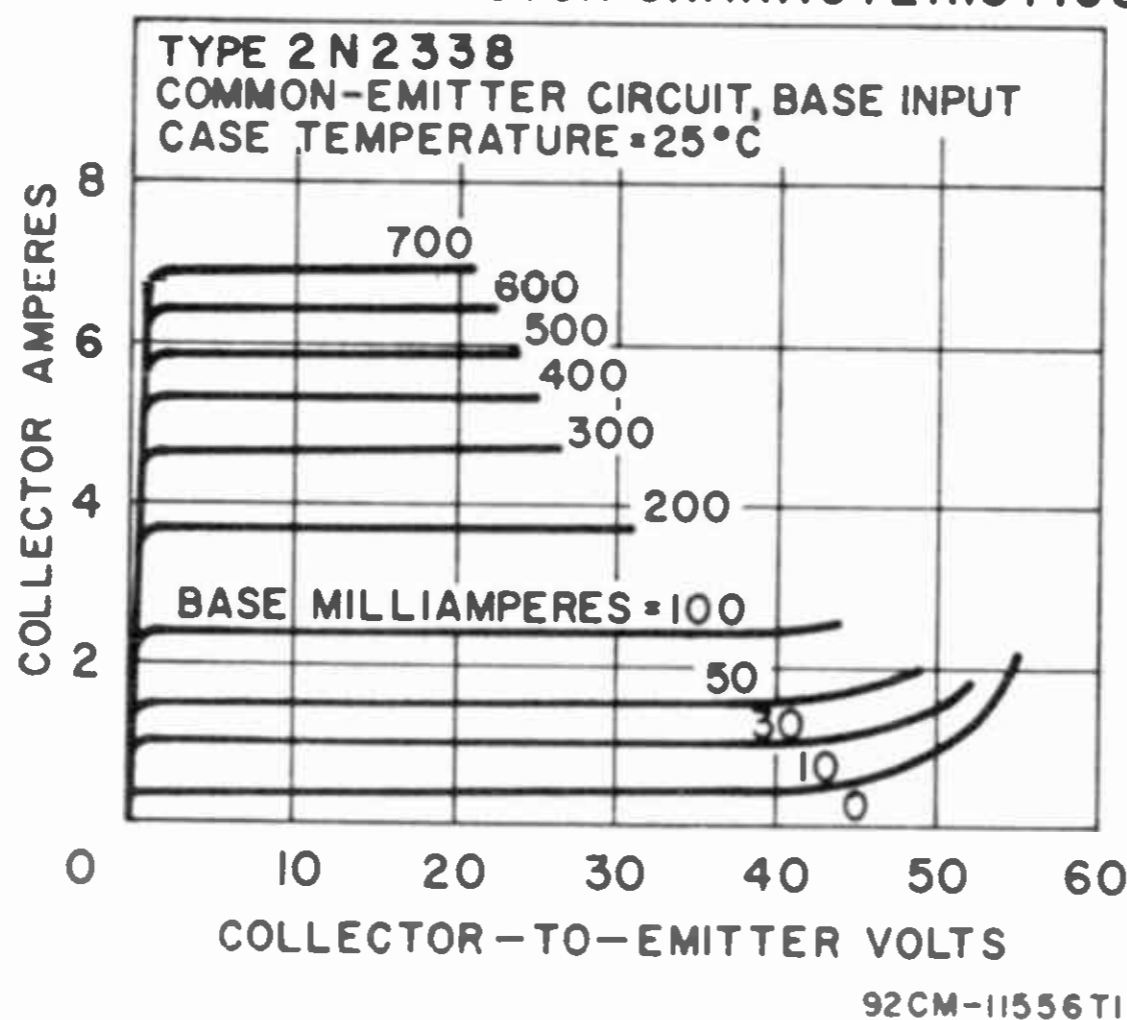
CHARACTERISTICS (cont'd)

Collector-to-Emitter Sustaining Voltage ($I_C = 200 \text{ mA}$, $I_B = 0$)	$V_{CE0}(\text{sus})$	40 min	V
Collector-to-Emitter Saturation Voltage: $I_C = 6 \text{ A}$, $I_B = 1 \text{ A}$	$V_{CE}(\text{sat})$	3.5 max	V
$I_C = 3 \text{ A}$, $I_B = 0.3 \text{ A}$	$V_{CE}(\text{sat})$	1.5 max	V
Base-to-Emitter Saturation Voltage ($V_{CE} = 4 \text{ V}$, $I_C = 3 \text{ A}$)	V_{BE}	3 max	V
Collector-Cutoff Current: $V_{CB} = 30 \text{ V}$, $I_E = 0$, $T_C = 25^\circ\text{C}$	I_{CBO}	0.2 max	mA
$V_{CB} = 30 \text{ V}$, $I_E = 0$, $T_C = 150^\circ\text{C}$	I_{CBO}	3 max	mA
$V_{CE} = 30 \text{ V}$, $I_B = 0$	I_{CEO}	5 max	mA
$V_{CE} = 60 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 25^\circ\text{C}$	I_{CEV}	2 max	mA
$V_{CE} = 30 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 200^\circ\text{C}$	I_{CEV}	50 max	mA
Emitter-Cutoff Current ($V_{EB} = 6 \text{ V}$, $I_C = 0$)	I_{EBO}	0.1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 4 \text{ V}$, $I_C = 3 \text{ A}$)	h_{FE}	15 to 60	
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 4 \text{ V}$, $I_C = 0.5 \text{ A}$, $f = 1 \text{ kHz}$)	h_{fe}	12 to 72	
Output Capacitance ($V_{CB} = 40 \text{ V}$, $I_E = 0$, $f = 0.1 \text{ MHz}$)	C_{obo}	600 max	pF
Small-Signal Forward-Current Transfer-Ratio Cutoff Frequency ($V_{CE} = 4 \text{ V}$, $I_C = 5 \text{ A}$)	f_{hfe}	0.015 min	MHz
Collector-to-Emitter Saturation Resistance ($I_C = 3 \text{ A}$, $I_B = 0.3 \text{ A}$)	$r_{CE}(\text{sat})$	0.5 max	Ω
Thermal Time Constant	$\tau(\text{thermal})$	30	ms
Thermal Resistance, Junction-to-Case	Θ_{J-C}	1.17 max	$^\circ\text{C/W}$

TYPICAL OPERATION IN PULSE-RESPONSE TEST CIRCUIT

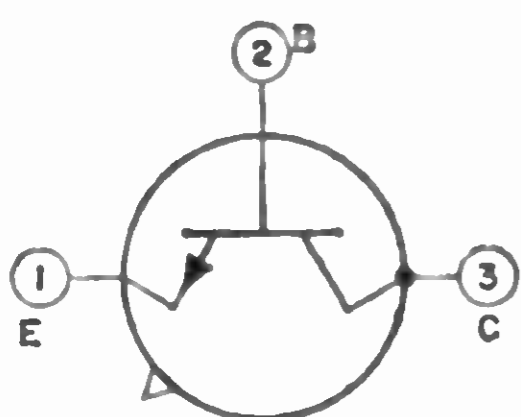
DC Collector Supply Voltage	V_{CC}	24	V
DC Base-Bias Voltage		-6	V
On DC Collector Current	I_C	10	A
Turn-On DC Base Current	I_{B1}	2	A
Base-Circuit Resistance	R_{B1}, R_{B2}	10	Ω
Collector-Circuit Resistance	R_C	2	Ω
Turn-On Time	$t_d + t_r$	4	μs
Turn-Off Time	$t_s + t_f$	7	μs

TYPICAL COLLECTOR CHARACTERISTICS



Refer to Chart of Discontinued Transistors

2N2339



COMPUTER TRANSISTOR

2N2369A

Si n-p-n planar epitaxial type used for high-speed saturated switching in logic applications. JEDEC TO-18, Outline No.12.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CB0}	40	V
Collector-to-Emitter Voltage	V_{CE0}	15	V
Emitter-to-Base Voltage	V_{EB0}	4.5	V
Collector Current	I_C	0.2	A

MAXIMUM RATINGS (cont'd)

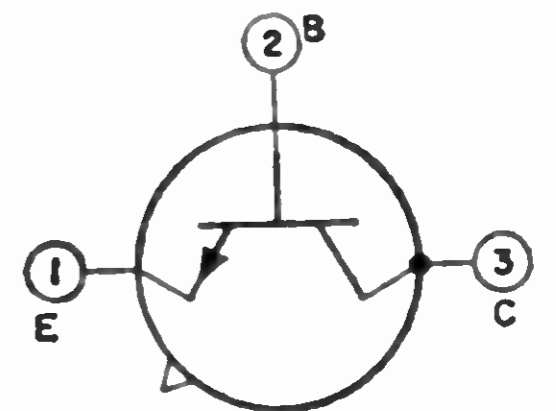
Transistor Dissipation:			
T_A up to 25°C	P_T	0.36	W
T_C up to 25°C	P_T	1.2	W
T_A or T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (60 s max)	T_L	300	°C

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = 0.01$ mA, $I_E = 0$)	$V_{(BR)CBO}$	40 min	V
Collector-to-Emitter Breakdown Voltage ($I_C = 0.01$ mA, $V_{EB} = 0$)	$V_{(BR)CES}$	40 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.01$ mA, $I_C = 0$)	$V_{(BR)EBO}$	4.5 min	V
Collector-to-Emitter Sustaining Voltage ($I_C = 10$ mA, $I_B = 0$, $t_p = 300$ μ s, $df = 2\%$)	V_{CEO} (sus)	15 min	V
Collector-to-Emitter Saturation Voltage:			
$I_C = 10$ mA, $I_B = 1$ mA, $T_A = 25^\circ$ C	V_{CE} (sat)	0.2 max	V
$I_C = 10$ mA, $I_B = 1$ mA, $T_A = 125^\circ$ C	V_{CE} (sat)	0.3 max	V
$I_C = 30$ mA, $I_B = 3$ mA	V_{CE} (sat)	0.25 max	V
$I_C = 100$ mA, $I_B = 10$ mA, $T_A = 25^\circ$ C	V_{CE} (sat)	0.5 max	V
Base-to-Emitter Saturation Voltage:			
$I_C = 10$ mA, $I_B = 1$ mA, $T_A = 25^\circ$ C	V_{BE} (sat)	0.7 to 0.85	V
$I_C = 10$ mA, $I_B = 1$ mA, $T_A = 125^\circ$ C	V_{BE} (sat)	0.59 min	V
$I_C = 10$ mA, $I_B = 1$ mA, $T_A = -55^\circ$ C	V_{BE} (sat)	1.02 max	V
$I_C = 30$ mA, $I_B = 3$ mA	V_{BE} (sat)	1.15 max	V
$I_C = 100$ mA, $I_B = 10$ mA, $T_A = 25^\circ$ C	V_{BE} (sat)	1.6 max	V
Collector-Cutoff Current ($V_{CB} = 20$ V, $I_E = 0$, $T_A = 150^\circ$ C)	I_{CBO}	30 max	μ A
Collector-Cutoff Current ($V_{CE} = 20$ V, $V_{EB} = 0$)	I_{CES}	0.4 max	μ A
Pulsed Static Forward-Current Transfer Ratio:			
$V_{CE} = 1$ V, $I_C = 10$ mA, $T_A = 25^\circ$ C, $t_p = 300$ μ s, $df = 2\%$	h_{FE} (pulsed)	120 max	
$V_{CE} = 0.35$ V, $I_C = 10$ mA, $t_p = 300$ μ s, $df = 2\%$	h_{FE} (pulsed)	40 min	
$V_{CE} = 0.4$ V, $I_C = 30$ mA, $t_p = 300$ μ s, $df = 2\%$	h_{FE} (pulsed)	30 min	
$V_{CE} = 0.35$ V, $I_C = 10$ mA, $T_A = -55^\circ$ C, $t_p = 300$ μ s, $df = 2\%$	h_{FE} (pulsed)	20 min	
$V_{CE} = 1$ V, $I_C = 100$ mA, $T_A = 25^\circ$ C, $t_p = 300$ μ s, $df = 2\%$	h_{FE} (pulsed)	20 min	
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 10$ V, $I_C = 10$ mA, $f = 100$ MHz)	h_{fe}	5 min	
Output Capacitance ($V_{CB} = 5$ V, $I_E = 0$, $f = 0.14$ MHz)	C_{obo}	4 max	pF
Storage Time ($V_{CC} = 10$ V, $I_C = 10$ mA, $I_{B1} = 10$ mA, $I_{B2} = -10$ mA)	t_s	13 max	ns
Turn-On Time ($V_{CC} = 3$ V, $I_C = 10$ mA, $I_{B1} = 3$ mA, V_{BE} (off) = -3 V)	$t_d + t_r$	12 max	ns
Turn-Off Time ($V_{CC} = 3$ V, $I_C = 10$ mA, $I_{B1} = 3$ mA, $I_{B2} = -1.5$ mA)	$t_s + t_f$	18 max	ns

2N2405 POWER TRANSISTOR

Si n-p-n triple-diffused planar type used in small-signal and medium power applications in industrial and military equipment. JEDEC TO-5, Outline No.5.



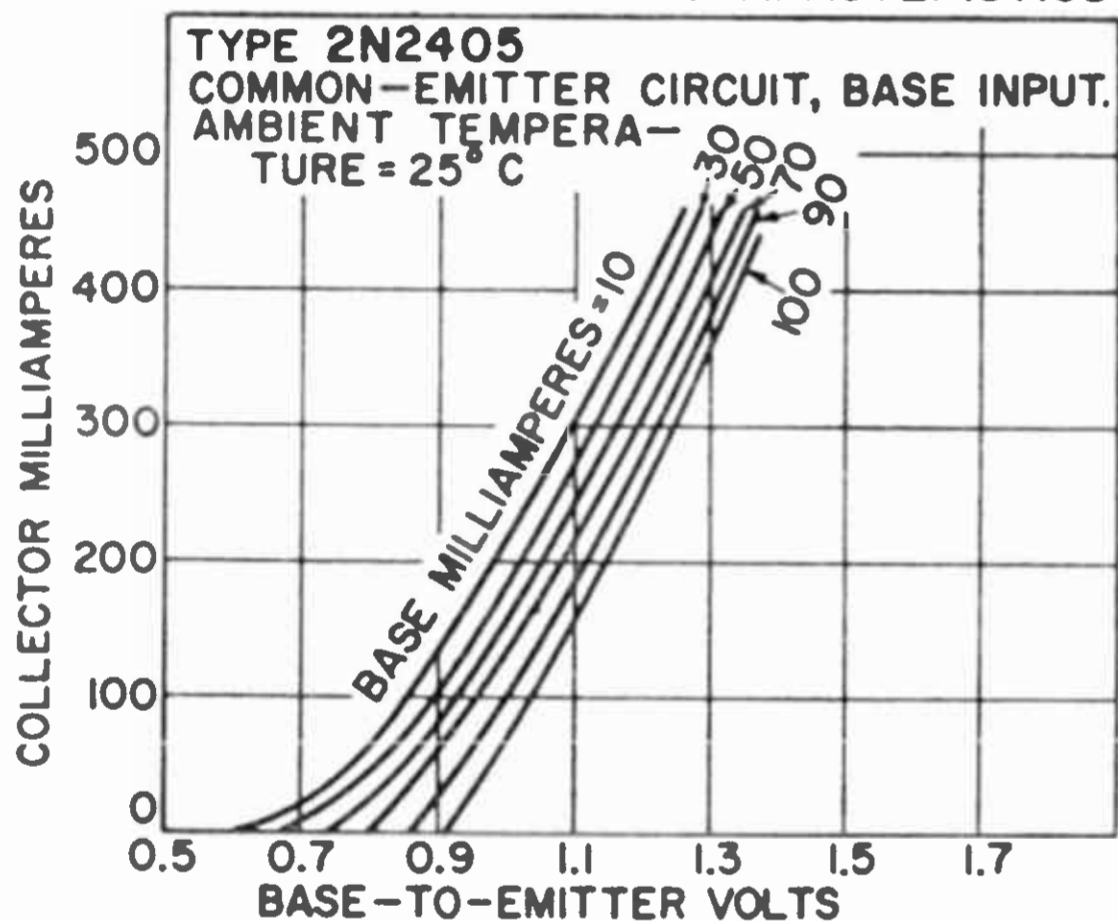
MAXIMUM RATINGS

Collector-to-Base Voltage:			
$V_{BE} = -1.5$ V	V_{CBV}^*	120	V
Emitter open	V_{CBO}	120	V
Collector-to-Emitter Voltage:			
$R_{BE} \leq 500$	V_{CER}^*	120	V
$R_{BE} \leq 10$	V_{CER}	140	V
Base open	V_{CEO}	90	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Collector Current	I_C	1	A
Transistor Dissipation:			
T_A up to 25°C	P_T	1	W
T_C up to 25°C	P_T	5	W
T_A or T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (T_J) and Storage (T_{STG})		-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	255	°C

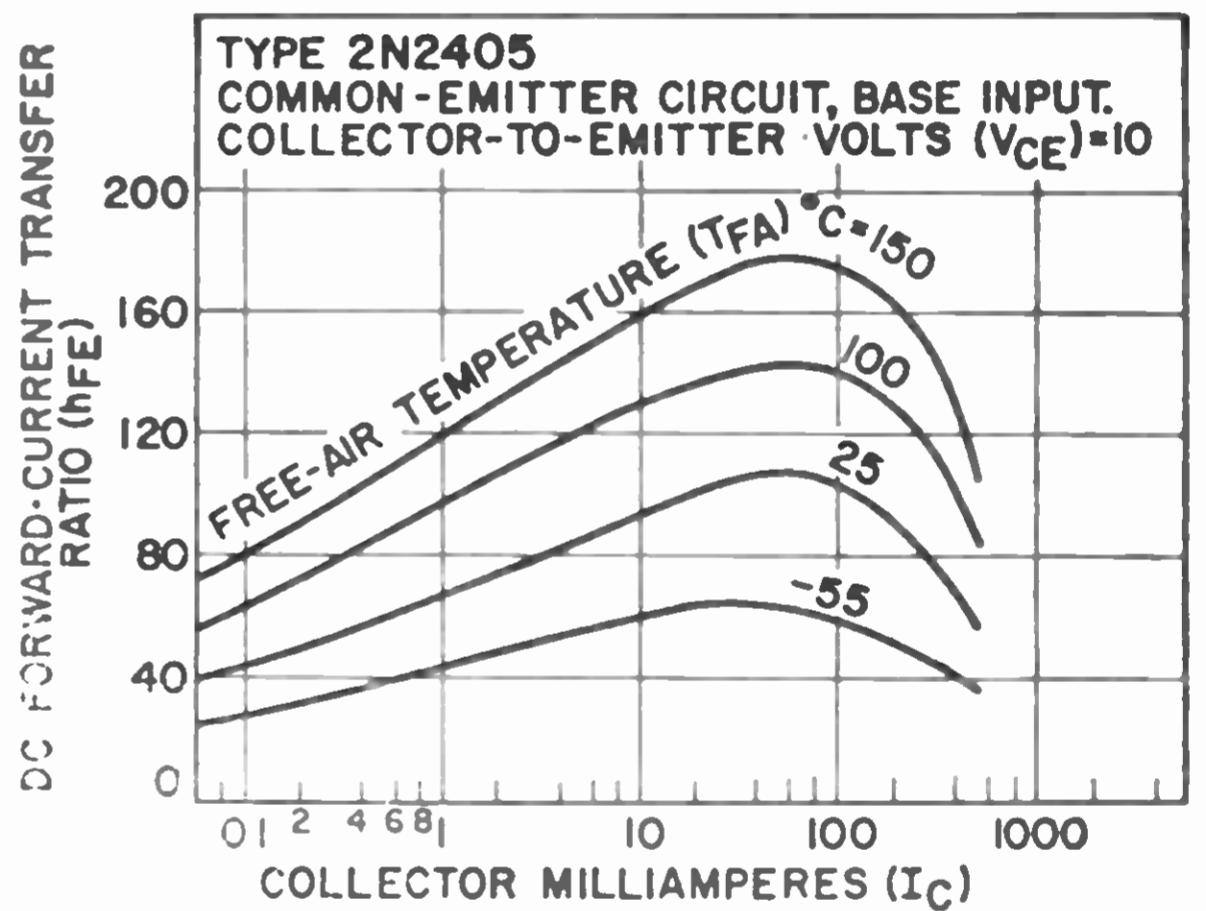
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Base Breakdown Voltage ($I_C = 0.1$ mA, $I_E = 0$)	$V_{(BR)CBO}$	120 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.01$ mA, $I_C = 0$)	$V_{(BR)EBQ}$	7 min	V
Collector-to-Emitter Sustaining Voltage:			
$I_C = 100$ mA, $I_B = 0$, $t_p = 300$ μ s, $df = 1.8\%$	$V_{CEO(SUS)}$	90 min	V
$I_C = 30$ mA, $I_B = 0$, $t_p = 300$ μ s, $df = 1.8\%$	$V_{CEO(SUS)}$	90 min	V
$I_C = 100$ mA, $R_{BE} = 10$ Ω , $t_p = 300$ μ s, $df = 1.8\%$	$V_{CER(SUS)}$	140 min	V
$I_C = 100$ mA, $R_{BE} = 500$ Ω , $t_p = 300$ μ s, $df = 1.8\%$..	$V_{CER(SUS)}$	120 min	V
Collector-to-Emitter Saturation Voltage:			
$I_C = 150$ mA, $I_B = 15$ mA	$V_{CE(sat)}$	0.5 max	V
$I_C = 50$ mA, $I_B = 5$ mA	$V_{CE(sat)}$	0.2 max	V
Base-to-Emitter Saturation Voltage:			
$I_C = 150$ mA, $I_B = 15$ mA	$V_{BE(sat)}$	1.1 max	V
$I_C = 50$ mA, $I_B = 5$ mA	$V_{BE(sat)}$	0.9 max	V
Collector-Cutoff Current:			
$V_{CB} = 90$ V, $I_E = 0$, $T_C = 25^\circ C$	I_{CBO}	0.01 max	μA
$V_{CB} = 90$ V, $I_E = 0$, $T_C = 150^\circ C$	I_{CBO}	10 max	μA
Emitter-Cutoff Current ($V_{EB} = 5$ V, $I_C = 0$)	I_{EBO}	0.01 max	μA
Small-Signal Forward-Current Transfer Ratio:			
$V_{CE} = 5$ V, $I_C = 5$ mA, $f = 1$ kHz	h_{fe}	50 to 275	
$V_{CE} = 10$ V, $I_C = 50$ mA, $f = 20$ MHz	h_{fe}	6 min	
Pulsed Static Forward-Current Transfer Ratio:			
$V_{CE} = 10$ V, $I_C = 500$ mA, $T_A = 25^\circ C$, $t_p = 300$ μ s, $df = 1.8\%$	$h_{FE(pulsed)}$	25 min	
$V_{CE} = 10$ V, $I_C = 150$ mA, $T_A = 25^\circ C$, $t_p = 300$ μ s, $df = 1.8\%$	$h_{FE(pulsed)}$	60 to 200	

TYPICAL TRANSFER CHARACTERISTICS



TYPICAL DC FORWARD-CURRENT TRANSFER-RATIO CHARACTERISTICS

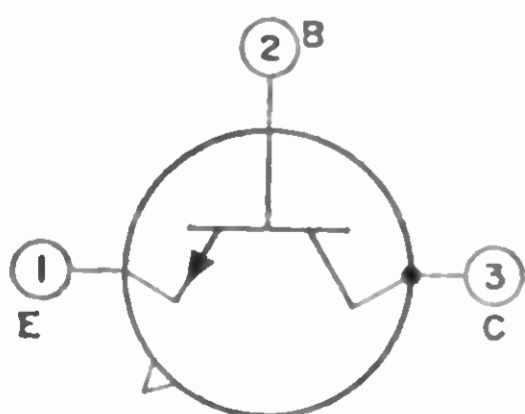


Static Forward-Current Transfer Ratio:			
$V_{CE} = 10$ V, $I_C = 10$ mA, $T_A = 25^\circ C$	h_{FE}	35 min	
$V_{CE} = 10$ V, $I_C = 10$ mA, $T_A = -55^\circ C$	h_{FE}	20 min	
Input Capacitance ($V_{EB} = 0.5$ V, $I_C = 0$)	C_{ibo}	80 max	pF
Output Capacitance ($V_{CB} = 10$ V, $I_E = 0$)	C_{obo}	15 max	pF
Thermal Resistance, Junction-to-Case	θ_{J-C}	35 max	$^\circ C/W$
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	175 max	$^\circ C/W$

* This value does not apply to type 2N1893.

COMPUTER TRANSISTOR

2N2475



Si n-p-n epitaxial planar type used in very-high-speed switching applications in logic circuits in military and commercial data-processing equipment. Similar to JEDEC TO-18, Outline No.12, except has minimum case height of 0.100 inch.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	15	V
Collector-to-Emitter Voltage	V_{CEO}	6	V
Emitter-to-Base Voltage	V_{EBO}	4	V
Collector Current	I_C	Limited by power dissipation	
Transistor Dissipation:			
T_A up to $25^\circ C$	P_T	0.3	W
T_C up to $100^\circ C$	P_T	0.5	W
T_A above $25^\circ C$ or T_C above $100^\circ C$	P_T	See curve page 300	

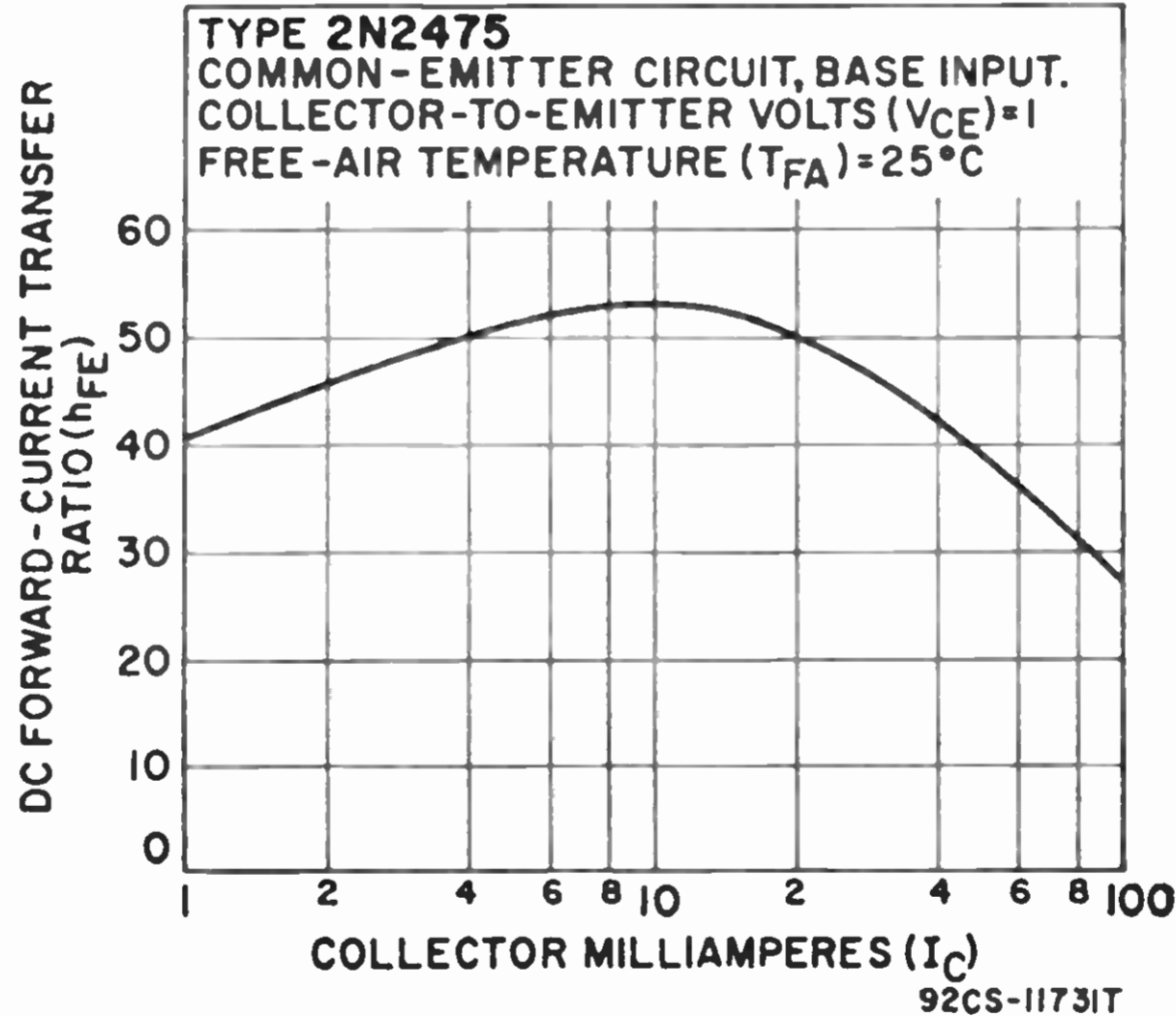
MAXIMUM RATINGS (cont'd)

Temperature Range:			
Operating (Junction)	T _J (opr)	-65 to 200	°C
Storage	T _{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T _L	300	°C

CHARACTERISTICS

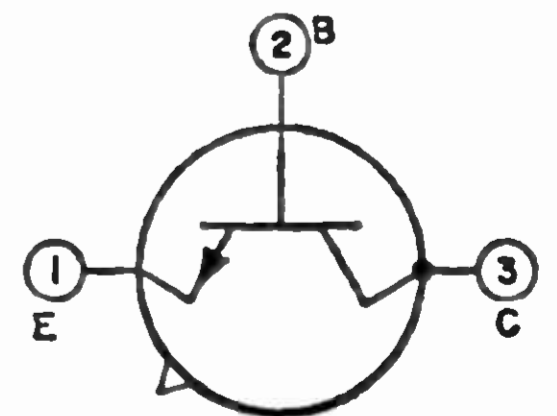
Collector-to-Base Breakdown Voltage (I _C = 10 μA, I _E = 0)	V _{(BR)CBO}	15 min	V
Emitter-to-Base Breakdown Voltage (I _E = 10 μA, I _C = 0)	V _{(BR)EBO}	4 min	V
Collector-to-Emitter Sustaining Voltage (I _C = 10 mA, I _B = 0, t _p ≥ 300 ns, df ≤ 2%)	V _{CEO} (sus)	6 min	V
Collector-to-Emitter Saturation Voltage (I _C = 20 mA, I _B = 0.66 mA)	V _{CE} (sat)	0.4 max	V
Base-to-Emitter Saturation Voltage (I _C = 20 mA, I _B = 0.66 mA)	V _{BE} (sat)	0.8 to 1	V
Collector-Cutoff Current:			
V _{CB} = 5 V, I _E = 0, T _A = 25°C	I _{CBO}	0.05 max	μA
V _{CB} = 5 V, I _E = 0, T _A = 150°C	I _{CBO}	5 max	μA
Static Forward-Current Transfer Ratio:			
V _{CE} = 0.5 V, I _C = 50 mA, T _A = 25°C	h _{FE}	20 min	
V _{CE} = 0.4 V, I _C = 20 mA, T _A = -55°C	h _{FE}	15 min	
V _{CE} = 0.4 V, I _C = 20 mA, T _A = 25°C	h _{FE}	30 to 150	
V _{CE} = 0.3 V, I _C = 1 mA, T _A = 25°C	h _{FE}	20 min	
Small-Signal Forward-Current Transfer Ratio (V _{CE} = 2 V, I _C = 20 mA, f = 100 MHz)	h _{fe}	6 min	
Input Capacitance (V _{EB} = 0.5 V, I _C = 0, f = 0.14 MHz)	C _{iBo}	3 max	pF
Output Capacitance (V _{CB} = 5 V, I _E = 0, f = 0.14 MHz)	C _{oBo}	2.5 max	pF
Storage Time (I _C = 5 mA, I _{B1} = 5 mA, I _{B2} = 5 mA, V _{CC} = 3 V)	t _s	6 max	ns
Turn-On Time (I _C = 20 mA, I _{B1} = 1 mA, I _{B2} = -1 mA, V _{CC} = 1.8 V)	t _d + t _r	20 max	ns
Turn-Off Time (I _C = 20 mA, I _{B1} = 1 mA, I _{B2} = -1 mA, V _{CC} = 1.8 V)	t _s + t _f	15 max	ns

TYPICAL DC FORWARD-CURRENT TRANSFER-RATIO CHARACTERISTIC



2N2476 COMPUTER TRANSISTOR

Si n-p-n double-diffused epitaxial planar type used in core-driving and line-driving applications where high switching speeds at high current are primary design requirements. JEDEC TO-5, Outline No.5.



MAXIMUM RATINGS

Collector-to-Base Voltage	V _{CBO}	60	V
Collector-to-Emitter Voltage	V _{CEO}	20	V
Emitter-to-Base Voltage	V _{EBO}	5	V
Collector Current	I _C	Limited by power dissipation	
Transistor Dissipation:			
T _A up to 25°C	P _T	0.6	W
T _C up to 25°C	P _T	2	W
T _A or T _C above 25°C	P _T	See curve page 300	

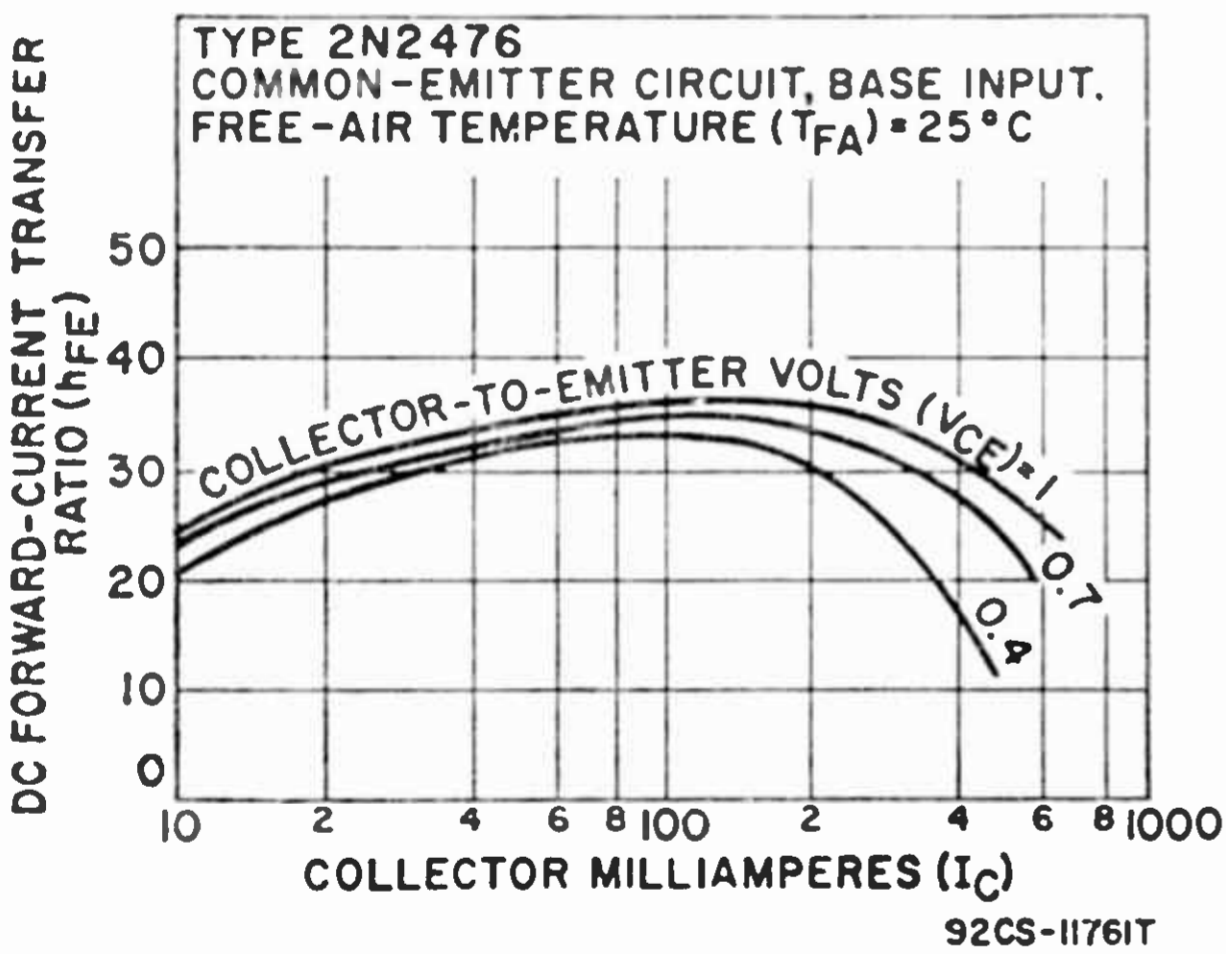
MAXIMUM RATINGS (cont'd)

Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	200	°C

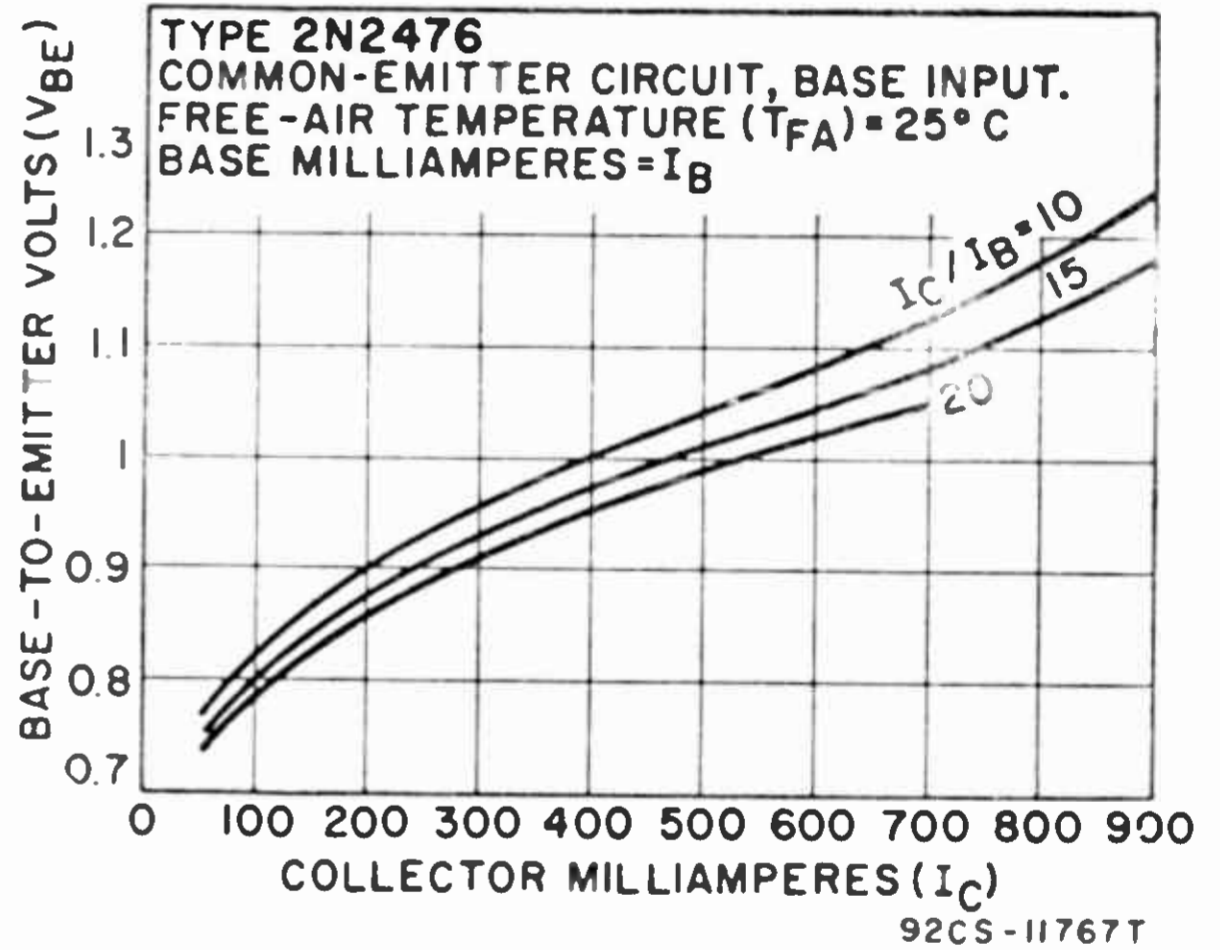
CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = 10 \mu A$, $I_E = 0$)	$V_{(BR)CBO}$	60 min	V
Collector-to-Emitter Breakdown Voltage ($I_C = 50 \text{ mA}$, $I_B = 0$, $t_p \leq 400 \mu s$, $df = 3\%$)	$V_{(BR)CEO}$	20 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.1 \text{ mA}$, $I_C = 0$)	$V_{(BR)EBO}$	5 min	V
Collector-to-Emitter Saturation Voltage $I_C = 150 \text{ mA}$, $I_B = 7.5 \text{ mA}$	$V_{CE(sat)}$	0.4 max	V
$I_C = 500 \text{ mA}$, $I_B = 50 \text{ mA}$	$V_{CE(sat)}$	0.75 max	V
Base-to-Emitter Voltage ($I_C = 150 \text{ mA}$, $I_B = 7.5 \text{ mA}$)	V_{BE}	1 max	V
Collector-Cutoff Current: $V_{CB} = 30 \text{ V}$, $I_E = 0$, $T_A = 25^\circ C$	I_{CBO}	0.2 max	μA
$V_{CB} = 30 \text{ V}$, $I_E = 0$, $T_A = 150^\circ C$	I_{CBO}	200 max	μA
Emitter-Cutoff Current ($V_{EB} = 5 \text{ V}$, $I_C = 0$)	I_{EBO}	100 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 0.4 \text{ V}$, $I_C = 150 \text{ mA}$)	h_{FE}	20 min	
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 10 \text{ V}$, $I_C = 50 \text{ mA}$, $f = 100 \text{ MHz}$)	h_{fe}	2.5 min	
Output Capacitance ($V_{CB} = 10 \text{ V}$, $I_E = 0$, $f = 0.14 \text{ MHz}$)	C_{ob0}	10 max	pF
Storage Time ($V_{CC} = 6.4 \text{ V}$, $R_C = 40 \Omega$, $I_{B1} = 15 \text{ mA}$, $I_{B2} = -15 \text{ mA}$, $I_C = 150 \text{ mA}$)	t_s	25 max	ns
Turn-On Time ($V_{CC} = 6.4 \text{ V}$, $I_{B1} = 15 \text{ mA}$, $I_{B2} = -15 \text{ mA}$, $I_C = 150 \text{ mA}$)	$t_d + t_r$	25 max	ns
Turn-Off Time ($V_{CC} = 6.4 \text{ V}$, $I_{B1} = 15 \text{ mA}$, $I_{B2} = -15 \text{ mA}$, $I_C = 150 \text{ mA}$)	$t_s + t_f$	45 max	ns

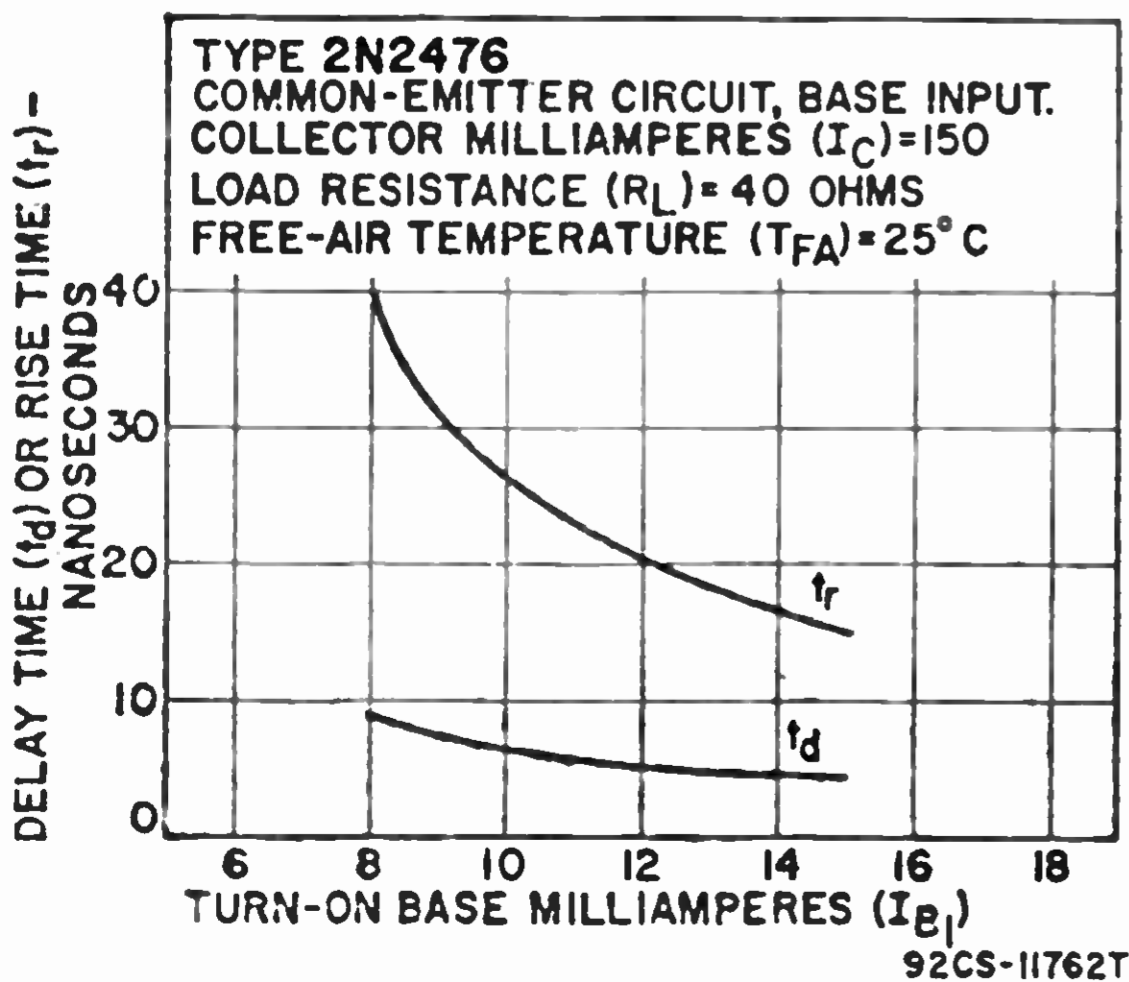
TYPICAL DC FORWARD-CURRENT TRANSFER-RATIO CHARACTERISTICS



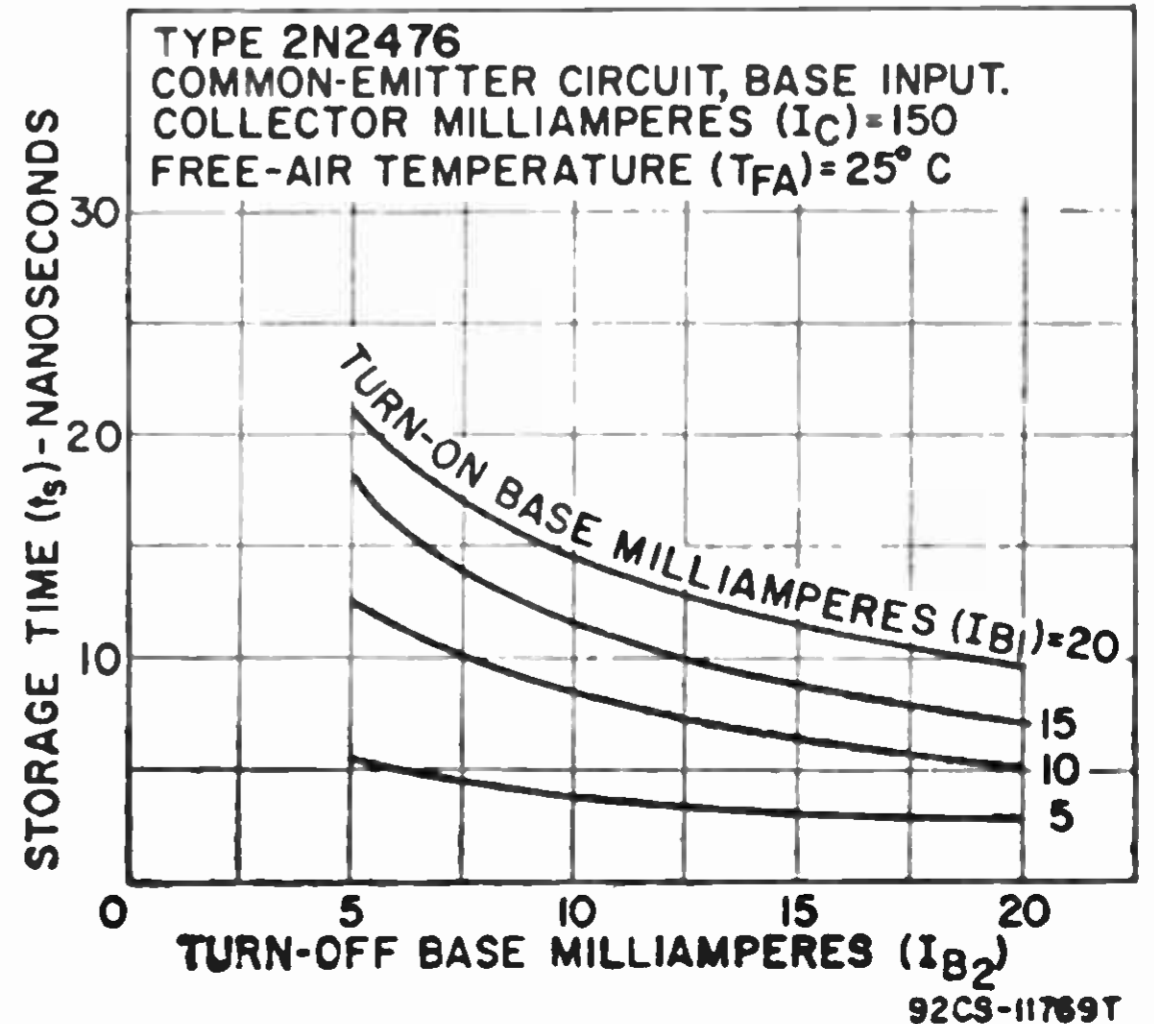
TYPICAL TRANSFER CHARACTERISTICS



TYPICAL DELAY-TIME AND RISE-TIME CHARACTERISTICS

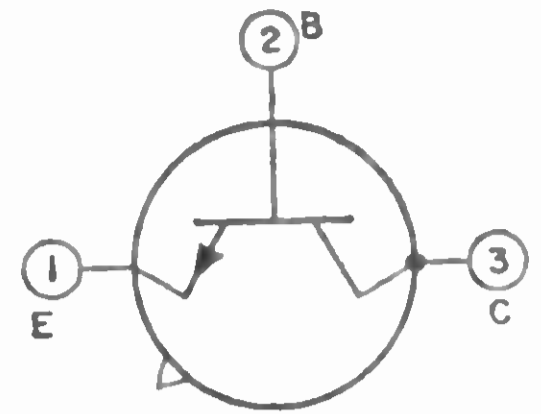


TYPICAL STORAGE-TIME CHARACTERISTICS



2N2477 COMPUTER TRANSISTOR

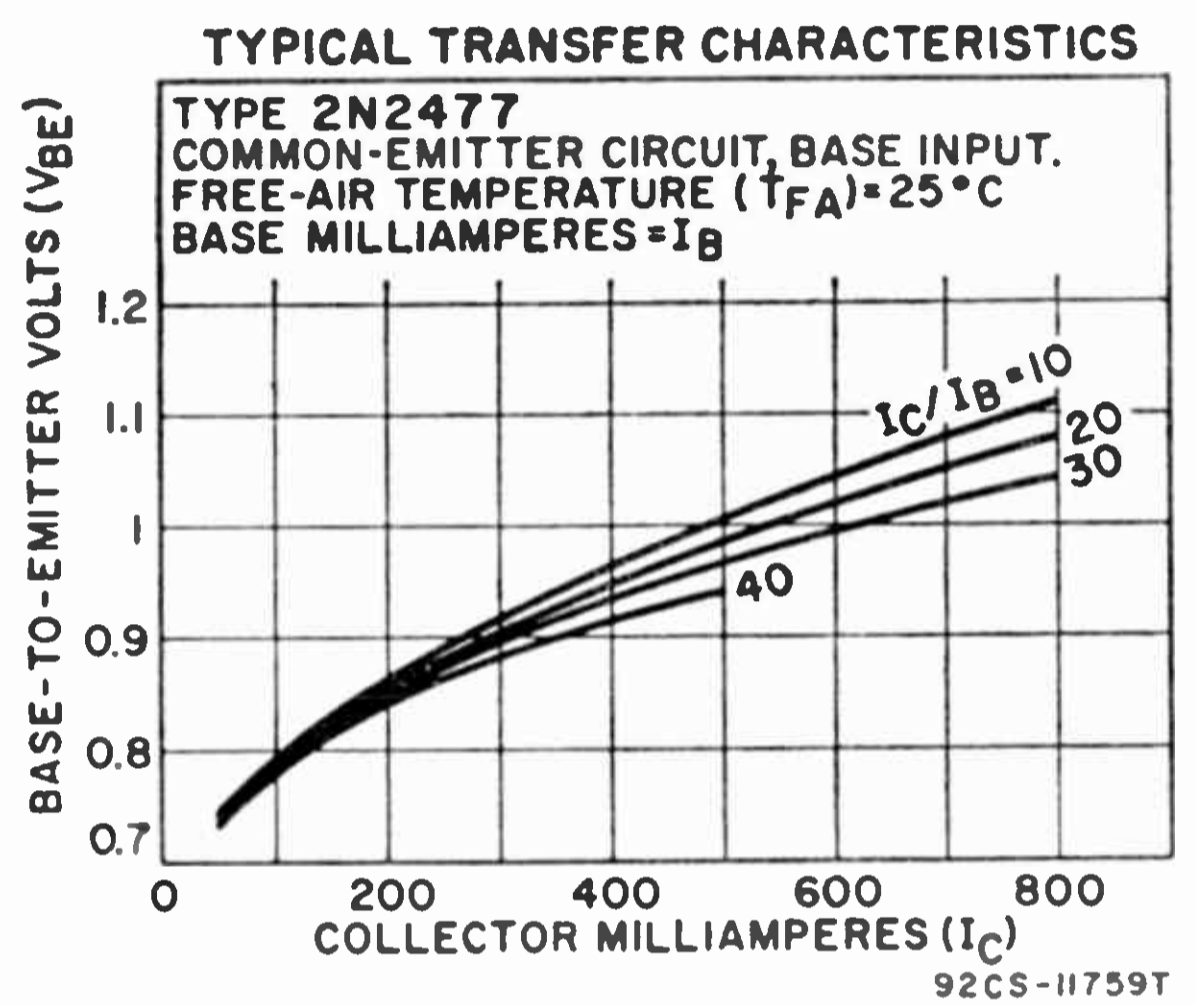
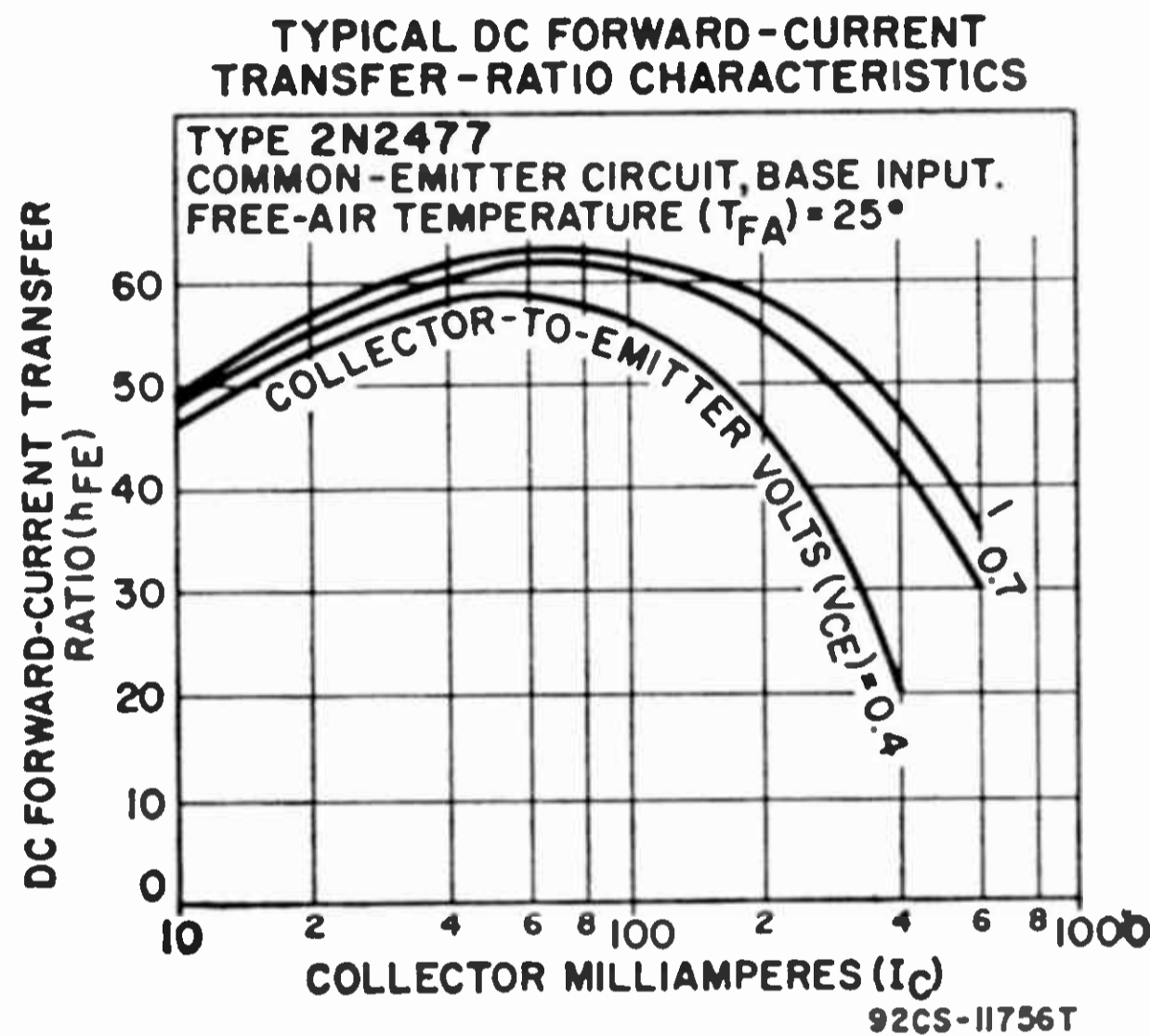
Si n-p-n double-diffused epitaxial planar type used in core-driving and line-driving applications where high switching speeds at high current are primary design requirements. JEDEC TO-5, Outline No.5. This type is identical with type 2N2476 except for its switching characteristics and the following items:



CHARACTERISTICS

Collector-to-Emitter Saturation Voltage:

$I_C = 150 \text{ mA}, I_B = 3.75 \text{ mA}$	$V_{CE(sat)}$	0.4 max	V
$I_C = 500 \text{ mA}, I_B = 50 \text{ mA}$	$V_{CE(sat)}$	0.65 max	V
Base-to-Emitter Voltage ($I_C = 150 \text{ mA}, I_B = 3.75 \text{ mA}$)	V_{BE}	0.95 max	V
Static Forward-Current Transfer Ratio ($V_{CE} = 0.4 \text{ V}, I_C = 150 \text{ mA}$)	h_{FE}	40 min	

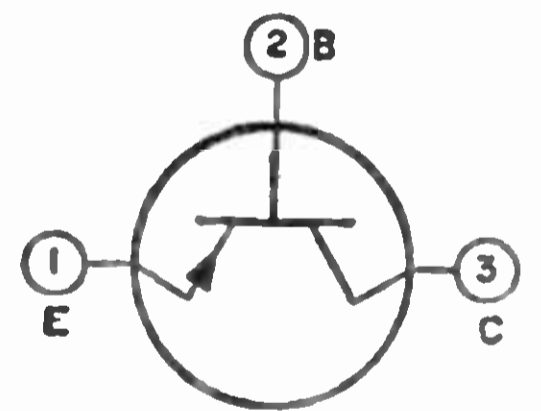


2N2482

Refer to Chart of Discontinued Transistors

2N2613 TRANSISTOR

Ge p-n-p alloy-junction type used in small-signal and low-power audio frequency applications. It is a low-noise type for use in input and low-level stages. JEDEC TO-1, Outline No.1.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-30	V
Collector-to-Emitter Voltage ($R_{BE} = 10 \text{ k}\Omega$)	V_{CER}	-25	V
Emitter-to-Base Voltage	V_{EBO}	-25	V
Collector Current	I_C	-50	mA
Emitter Current	I_E	50	mA
Transistor Dissipation:			
T_A up to 55°C	P_T	120	mW
T_A above 55°C	P_T	See curve page 300	
Temperature Range:*			
Operating (Junction)	$T_J(\text{opr})$	100	$^\circ\text{C}$
Storage	T_{STG}	-65 to 100	$^\circ\text{C}$

Lead-Soldering Temperature (10 s max)

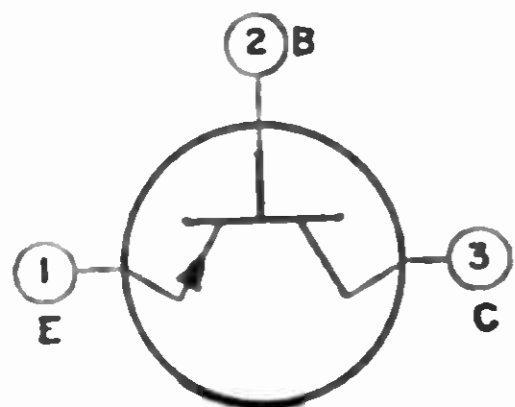
* This type should not be connected into or disconnected from circuits with the power on because high transient current may cause permanent damage to the transistor.

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($V_{BE} = 2 \text{ V}, I_C = -0.05 \text{ mA}$)	$V_{(BR)CBV}$	-30 min	V
Collector-to-Emitter Breakdown Voltage ($R_{BE} = 10000 \Omega, I_C = -1 \text{ mA}$)	$V_{(BR)CER}$	-25 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -0.05 \text{ mA}, I_C = 0$)	$V_{(BR)EBO}$	-25 min	V

CHARACTERISTICS (cont'd)

Collector-Cutoff Current ($V_{CB} = -20\text{ V}, I_E = 0$)	I_{CBO}	-5 max	μA
Emitter-Cutoff Current ($V_{EB} = -20\text{ V}, I_C = 0$)	I_{EBO}	-7.5 max	μA
Intrinsic Base-Spreading Resistance ($V_{CE} = -4\text{ V}, I_C = -0.5\text{ mA}, f = 20\text{ MHz}$)	$r_{bb'}$	300	Ω
Collector-to-Base Feedback Capacitance ($V_{CE} = -4.5\text{ V}, I_C = -0.5\text{ mA}$)	$C_{b'c}$	10	pF
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = -4\text{ V}, I_C = -0.5\text{ mA}, f = 1\text{ kHz}$)	h_{fe}	120 to 300	
Small-Signal Forward-Current Transfer-Ratio Cutoff Frequency ($V_{CE} = -6\text{ V}, I_C = -1\text{ mA}$)	f_{hfb}	4 min	MHz
RMS Noise Input Current (Equivalent) ($V_{CE} = -4.5\text{ V}, I_C = -0.5\text{ mA}, R_{BE} = 50000\ \Omega,$ $f = 20\text{ to }20000\text{ Hz}$)		0.001 max	μA
Noise Figure (Circuit bandwidth = 1.1 kHz, $V_{CE} = -4.5\text{ V}, I_C = -0.5\text{ mA}, R_G = 1000\ \Omega,$ $f = 1\text{ kHz}$)	NF	4 max	dB



TRANSISTOR

2N2614

Ge p-n-p alloy-junction type used in small-signal and low-power audio frequency applications. JEDEC TO-1, Outline No.1.

MAXIMUM RATINGS

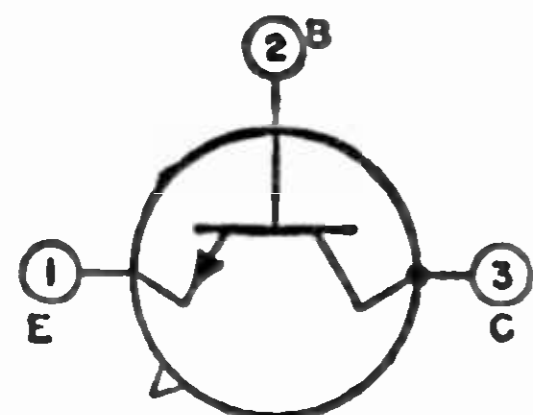
Collector-to-Base Voltage	V_{CBO}	-40	V
Collector-to-Emitter Voltage ($R_{BE} = 10\text{ k}\Omega$)	V_{CER}	-35	V
Emitter-to-Base Voltage	V_{EBO}	-25	V
Collector Current	I_C	-50	mA
Emitter Current	I_E	50	mA
Transistor Dissipation:			
T_A up to 55°C	P_T	120	mW
T_C up to 55°C	P_T	300	mW
T_A or T_C above 55°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 100	°C
Storage	T_{STG}	-65 to 100	°C
Lead-Soldering Temperature (10 s max)	T_L	255	°C

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = -0.05\text{ mA}, V_{BE} = 2\text{ V}$)	$V_{(BR)CBV}$	-40 min	V
Collector-to-Emitter Breakdown Voltage ($I_C = -1\text{ mA}, R_{BE} = 10\text{ k}\Omega$)	$V_{(BR)CER}$	-35 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -0.05\text{ mA}, I_C = 0$)	$V_{(BR)EBO}$	-25 min	V
Collector-Cutoff Current ($V_{CB} = -20\text{ V}, I_E = 0$) ...	I_{CBO}	-5 max	μA
Emitter-Cutoff Current ($V_{EB} = -20\text{ V}, I_C = 0$)	I_{EBO}	-7.5 max	μA
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = -6\text{ V}, I_C = -1\text{ mA}, f = 1\text{ kHz}$)	h_{fe}	100 to 250	
Small-Signal Forward-Current Transfer-Ratio Cutoff Frequency ($V_{CE} = -6\text{ V}, I_C = -1\text{ mA}$)	f_{hfe}	4 min	MHz
Collector-to-Base Feedback Capacitance ($V_{CE} = -6\text{ V}, I_C = -1\text{ mA}$)	$C_{b'c}$	12 max	pF
Intrinsic Base-Spreading Resistance ($V_{CE} = -6\text{ V}, I_C = -1\text{ mA}, f = 20\text{ MHz}$)	$r_{bb'}$	300	Ω

POWER TRANSISTOR

2N2631



Si n-p-n triple-diffused planar type used in large-signal vhf applications such as AM, FM, and cw service at frequencies up to 150 MHz in industrial and military equipment. JEDEC TO-39, Outline No.15. This type is identical with type 2N2876 except for the following items:

MAXIMUM RATINGS

Collector Current	I_C	1.5	A
Transistor Dissipation:			
T_C up to 25°C	P_T	8.75	W
Lead-Soldering Temperature (10 s max)	T_L	230	°C

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Saturation Voltage ($I_C = 1.5\text{ A}, I_B = 0.3\text{ A}$)	$V_{CE}(\text{sat})$	1 max	V
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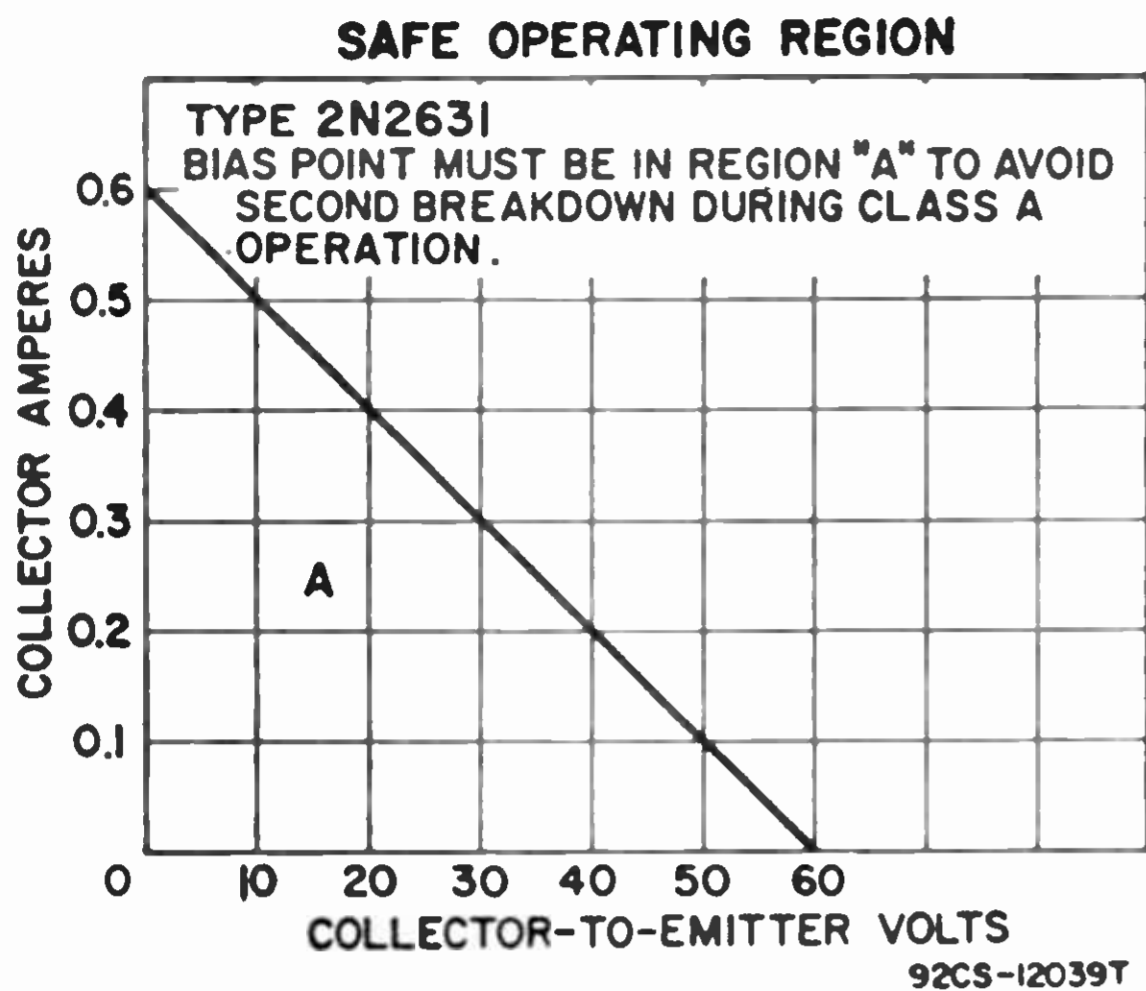
CHARACTERISTICS (cont'd)

RF Power Output, Unneutralized
 ($V_{CE} = 28 \text{ V}$, $I_C = 0.375 \text{ A}$, $P_{IE} = 1 \text{ W}$,
 $f = 50 \text{ MHz}$)

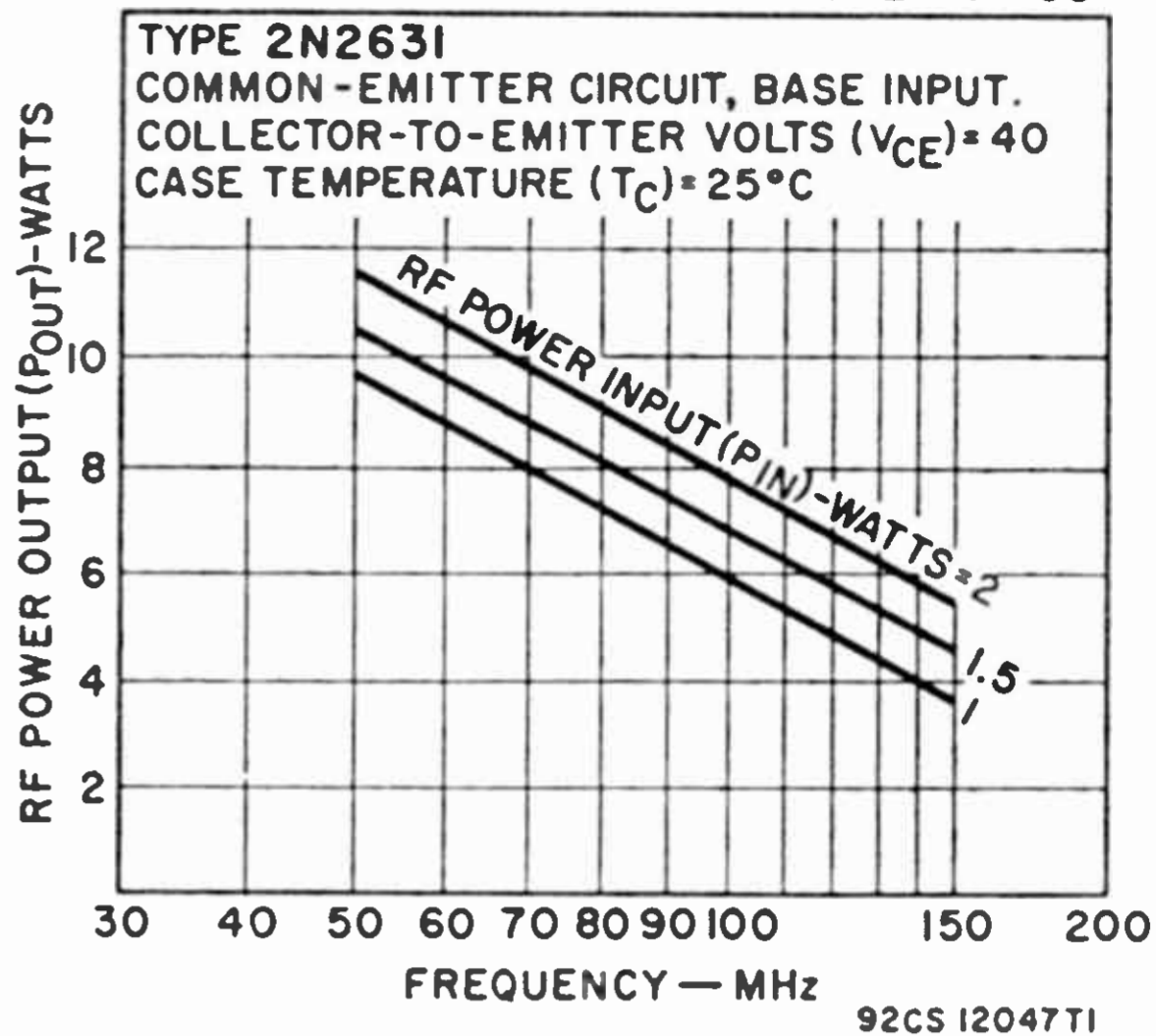
P_{OE}

7.5 min

W



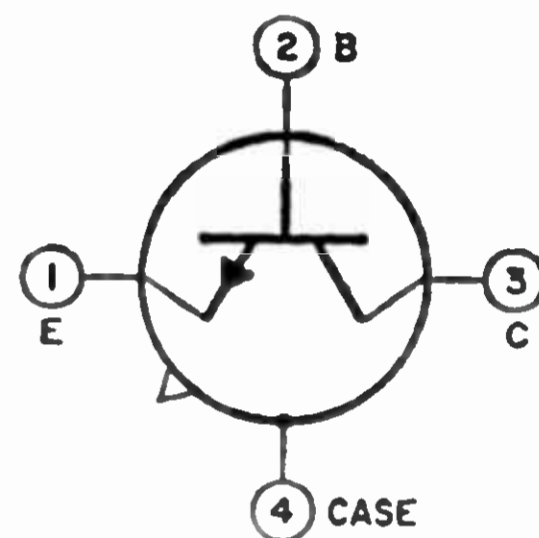
TYPICAL OPERATION CHARACTERISTICS



2N2708

TRANSISTOR

Si n-p-n double-diffused epitaxial planar type used in rf amplifiers, mixers, and oscillator circuits for vhf and uhf applications (200 to 500 MHz). JEDEC TO-72, Outline No.28.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	35	V
Collector-to-Emitter Voltage	V_{CEO}	20	V
Emitter-to-Base Voltage	V_{EBO}	3	V
Collector Current	I_C	Limited by power dissipation	
Transistor Dissipation:			
T_A up to 25°C	P_T	0.2	W
T_C up to 25°C	P_T	0.3	W
T_A or T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	265	°C

CHARACTERISTICS

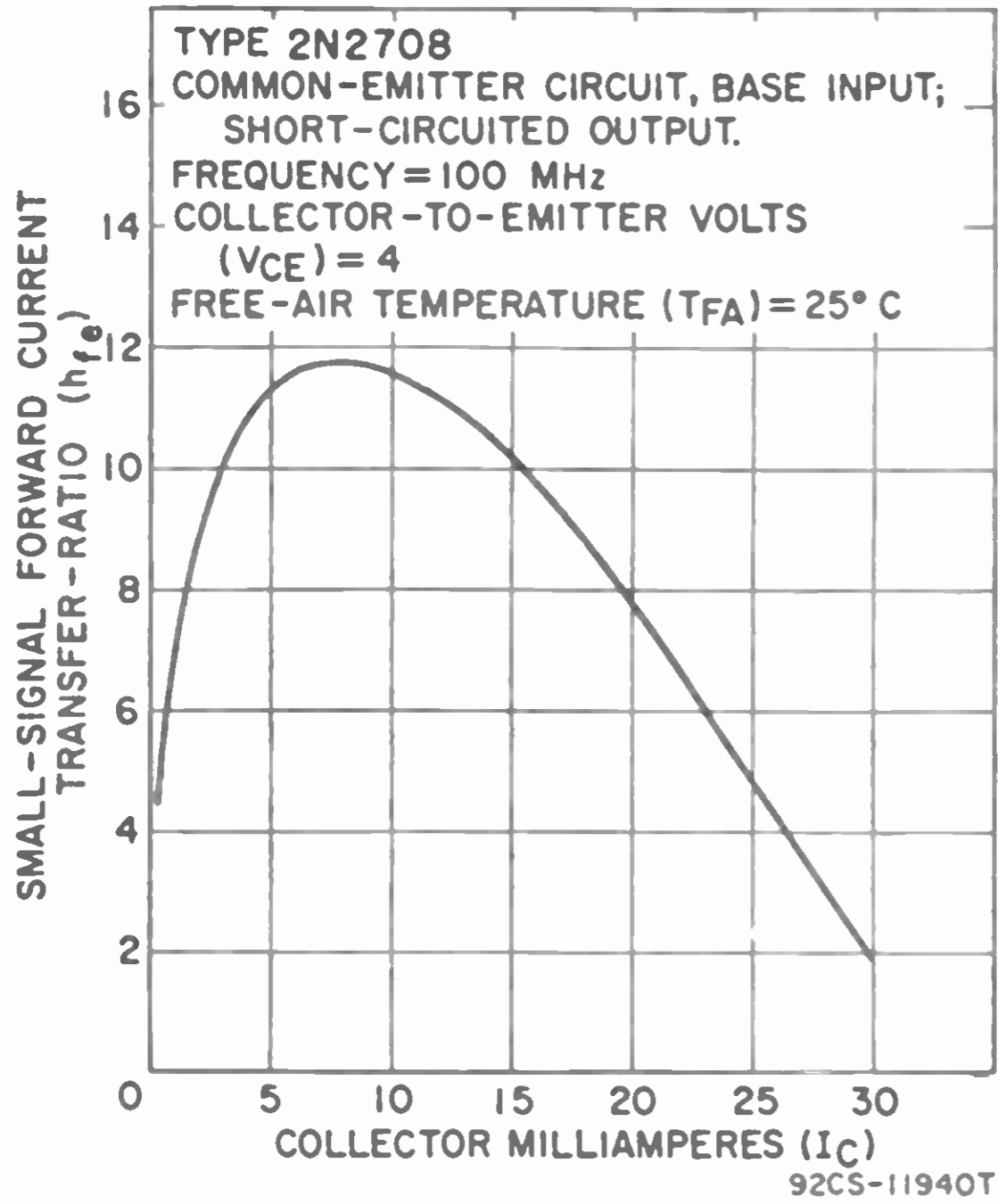
Collector-to-Base Breakdown Voltage ($I_C = 1 \mu\text{A}$, $I_E = 0$)	$V_{(BR)CBO}$	35 min	V
Collector-to-Emitter Breakdown Voltage ($I_C = 3 \text{ mA}$, $I_B = 0$, $t_p = 300 \mu\text{s}$, $df = 1\%$)	$V_{(BR)CEO(SUS)}$	20 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 10 \mu\text{A}$, $I_C = 0$)	$V_{(BR)EBO}$	3 min	V
Collector-Cutoff Current:			
$V_{CB} = 15 \text{ V}$, $I_E = 0$, $T_A = 25^\circ\text{C}$	I_{CBO}	0.01 max	μA
$V_{CB} = 15 \text{ V}$, $I_E = 0$, $T_A = 150^\circ\text{C}$	I_{CBO}	1 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 2 \text{ V}$, $I_C = 2 \text{ mA}$)	h_{FE}	30 to 200	
Small-Signal Forward-Current Transfer Ratio:			
$V_{CE} = 15 \text{ V}$, $I_C = 2 \text{ mA}$, $f = 1 \text{ kHz}$	h_{fe}	30 to 180	
$V_{CE} = 15 \text{ V}$, $I_C = 2 \text{ mA}$, $f = 100 \text{ MHz}$	h_{fe}	7 to 12	
Input Capacitance ($V_{EB} = 0.5 \text{ V}$, $I_C = 0$, $f = 0.14 \text{ MHz}$)	C_{ibo}	1.4	pF
Output Capacitance ($V_{CB} = 15 \text{ V}$, $I_E = 0$, $f = 0.14 \text{ MHz}$)	C_{obo}	1.5 max	pF
Collector-to-Base Time Constant ($V_{CB} = 1.5 \text{ V}$, $I_C = 2 \text{ mA}$, $f = 31.9 \text{ MHz}$)	$r_b'C_c$	9 to 33	ps
Small-Signal Common-Emitter Power Gain:			
(In neutralized amplifier)			
$V_{CE} = 15 \text{ V}$, $I_C = 2 \text{ mA}$, $f = 200 \text{ MHz}$	G_{pe}	15 to 22	dB
(In unneutralized amplifier)			
$V_{CE} = 15 \text{ V}$, $I_C = 2 \text{ mA}$, $f = 200 \text{ MHz}$	G_{pe}	12	dB
Small-Signal Transconductance ($V_{CE} = 15 \text{ V}$, $I_C = 2 \text{ mA}$, $f = 200 \text{ MHz}$)	g_{me}	25	mmhos

CHARACTERISTICS (cont'd)

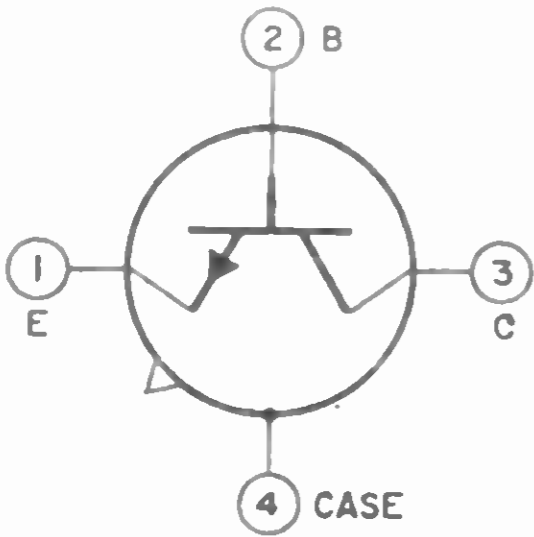
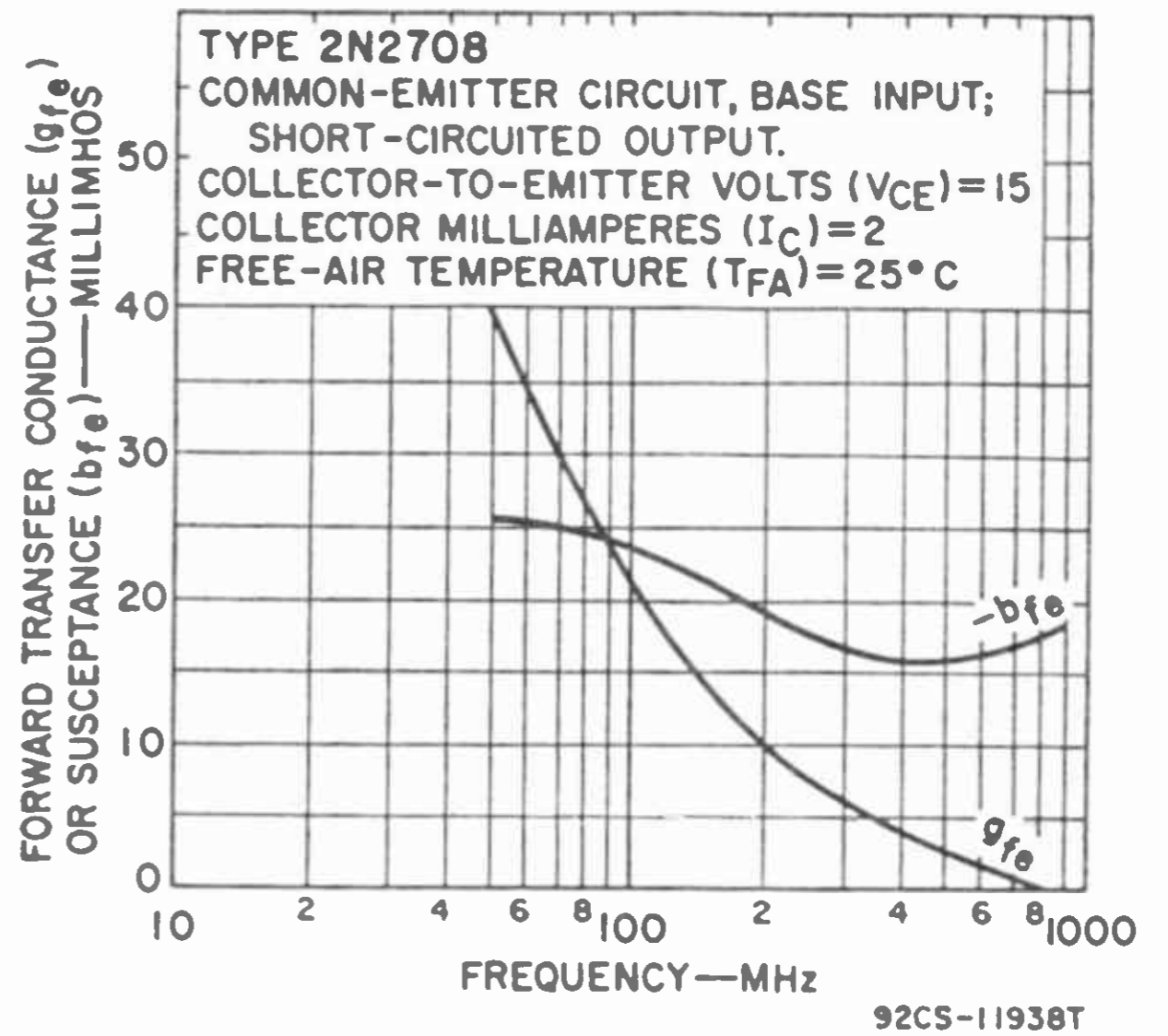
Noise Figure:

$V_{CE} = 15\text{ V}, I_C = 2\text{ mA}, R_s = 50\ \Omega,$ $f = 200\text{ MHz}$	NF	7.5 max	dB
$V_{CE} = 6\text{ V}, I_C = 1\text{ mA}, R_s = 400\ \Omega,$ $f = 60\text{ MHz}$	NF	3.5	dB

TYPICAL SMALL-SIGNAL FORWARD-CURRENT TRANSFER-RATIO CHARACTERISTIC



TYPICAL SMALL-SIGNAL FORWARD TRANSFER CONDUCTANCE AND SUSCEPTANCE CHARACTERISTICS



UHF TRANSISTOR

2N2857

Si n-p-n double-diffused epitaxial planar type used in low-noise amplifier, oscillator, and converter applications at frequencies up to 500 MHz in a common-emitter circuit, and up to 1200 MHz in a common-base circuit. JEDEC TO-72, Outline No.28.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	30	V
Collector-to-Emitter Voltage	V_{CEO}	15	V
Emitter-to-Base Voltage	V_{EBO}	2.5	V
Collector Current	I_C	40	mA
Transistor Dissipation:			
T_A up to 25°C	P_T	200	mW
T_C up to 25°C	P_T	300	mW
T_A or T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	265	°C

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = 0.001\text{ mA}, I_E = 0$)	$V_{(BR)CBO}$	30 min	V
Collector-to-Emitter Breakdown Voltage ($I_C = 3\text{ mA}, I_B = 0$)	$V_{(BR)CEO}$	15 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.01\text{ mA}, I_C = 0$)	$V_{(BR)EBO}$	2.5 min	V
Collector-Cutoff Current ($V_{CB} = 15\text{ V}, I_E = 0$)	I_{CBO}	0.01 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 1\text{ V}, I_C = 3\text{ mA}$)	h_{FE}	30 to 150	
Small-Signal Forward-Current Transfer Ratio:†			
$V_{CB} = 6\text{ V}, I_C = 5\text{ mA}, f = 100\text{ MHz}$	h_{fe}	10 to 19	
$V_{CE} = 6\text{ V}, I_C = 2\text{ mA}, f = 1\text{ kHz}$	h_{fe}	50 to 220	
Collector-to-Base Feedback Capacitance■ ($V_{CB} = 10\text{ V}, I_E = 0, f = 0.1\text{ to }1\text{ MHz}$)	C_{cb}	1 max	pF
Input Capacitance* ($V_{EB} = 0.5\text{ V}, I_C = 0,$ $f = 0.1\text{ to }1\text{ MHz}$)	C_{ibo}	1.4	pF

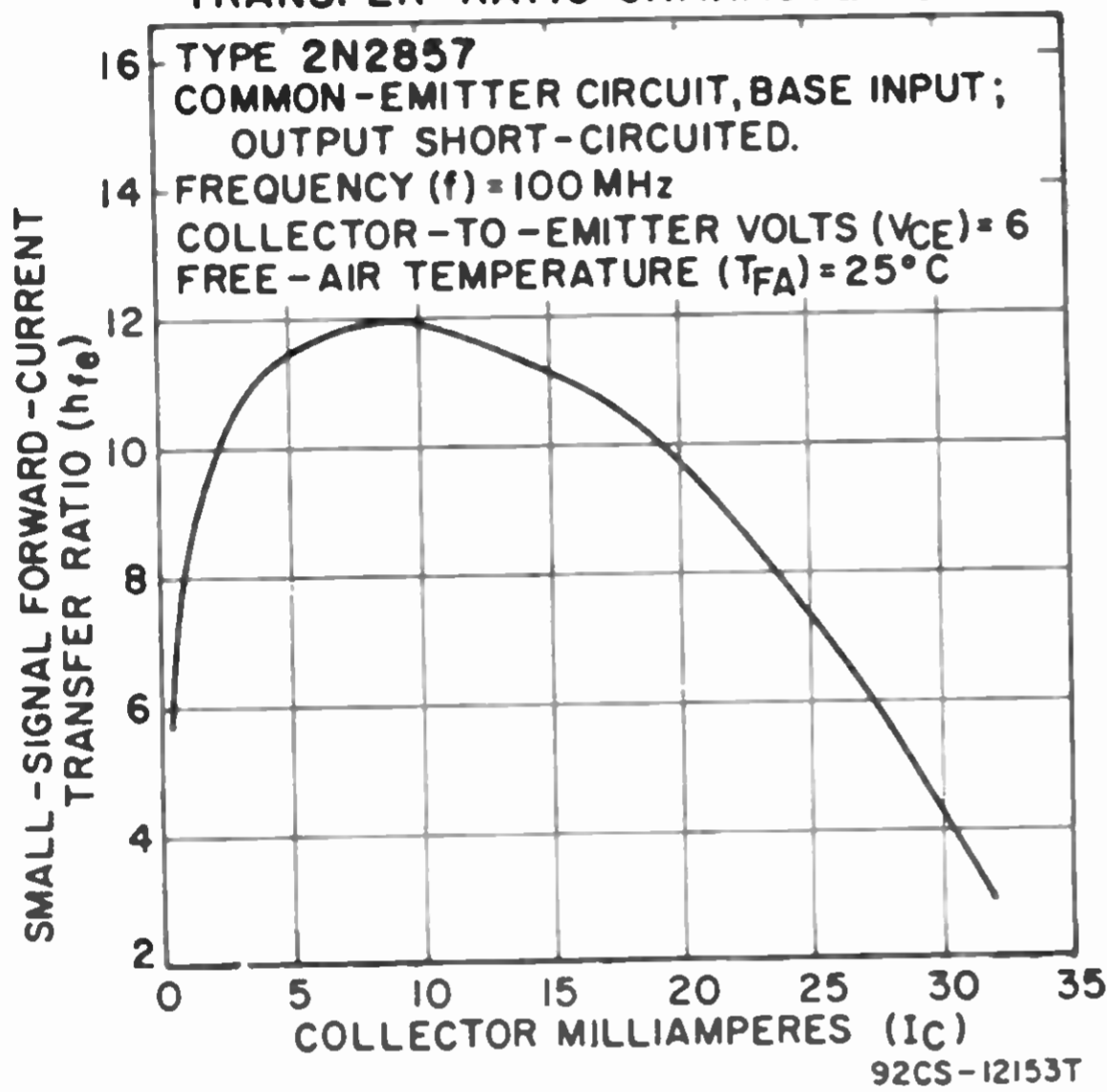
CHARACTERISTICS (cont'd)

Output Capacitance:

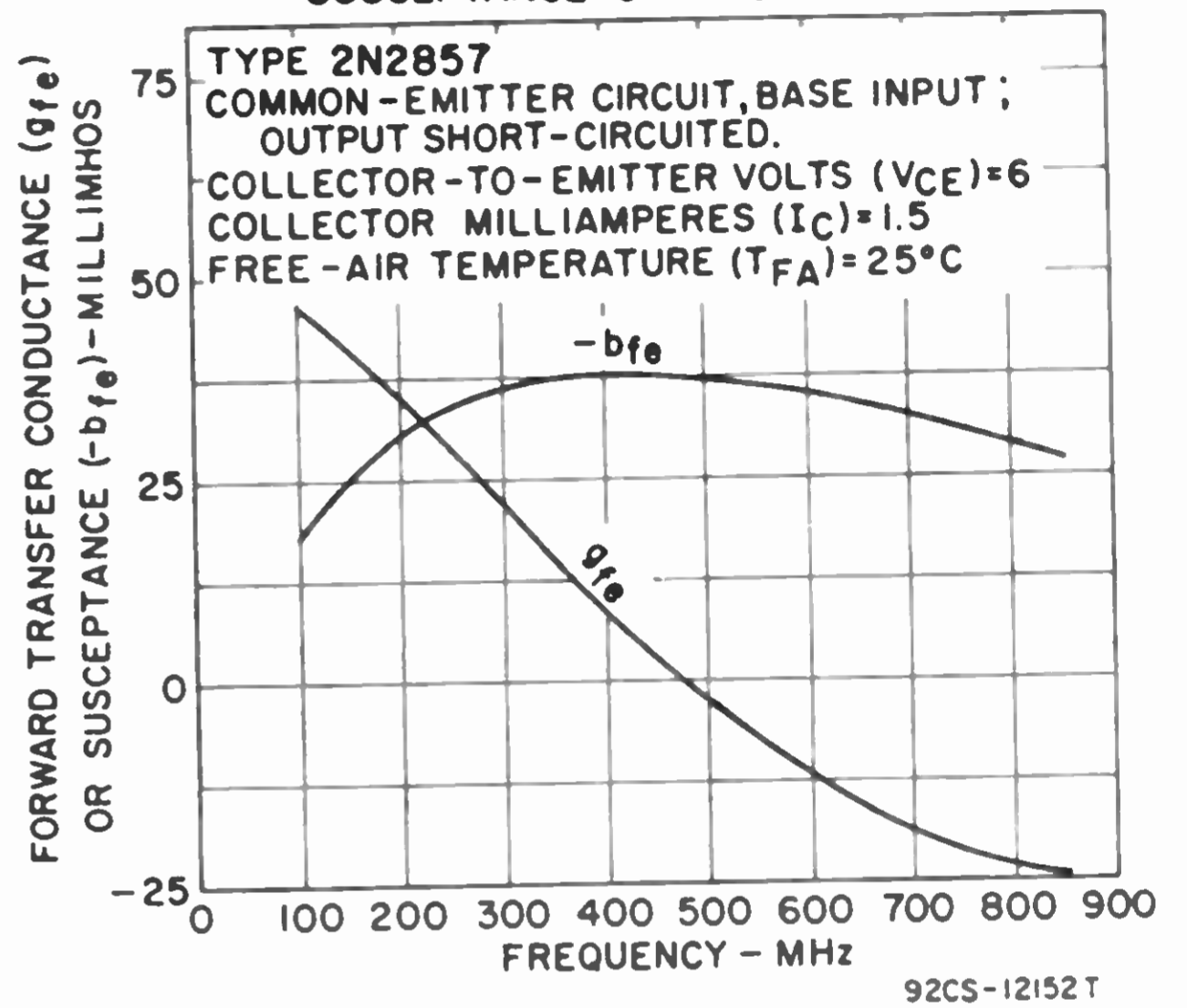
$V_{CB} = 10\text{ V}, I_E = 0, f = 0.14\text{ MHz}$	C_{obo}	1.3† max	pF
$V_{CB} = 10\text{ V}, I_E = 0, f = 0.14\text{ MHz}$	C_{obo}	1.8* max	pF
Collector-to-Base Time Constant† ($V_{CB} = 6\text{ V}, I_C = 2, f = 31.9\text{ MHz}$)	$r_b' C_c$	4 to 15	ps
Small-Signal Power Gain, Neutralized Amplifier† ($V_{CE} = 6\text{ V}, I_C = 1.5\text{ mA}, f = 450\text{ MHz}$)	G_{pe}	12.5 to 19	dB
Power Output, Oscillator Circuit* ($V_{CB} = 10\text{ V}, I_E = -12\text{ mA}, f = 500\text{ MHz}$)	P_{oe}	30 min	mW
Noise Figure:† $V_{CE} = 6\text{ V}, I_C = 1.5\text{ mA}, R_G = 50\ \Omega, f = 450\text{ MHz}$	NF	4.5 max	dB
$V_{CE} = 6\text{ V}, I_C = 1\text{ mA}, R_G = 400\ \Omega, f = 60\text{ MHz}$..	NF	2.2	dB

- * Fourth lead (case) not connected †Fourth lead (case) grounded
- Three-terminal measurement: Lead No. 1 (emitter) and lead No. 4 (case) connected to guard terminal.

TYPICAL SMALL-SIGNAL FORWARD-CURRENT TRANSFER-RATIO CHARACTERISTIC



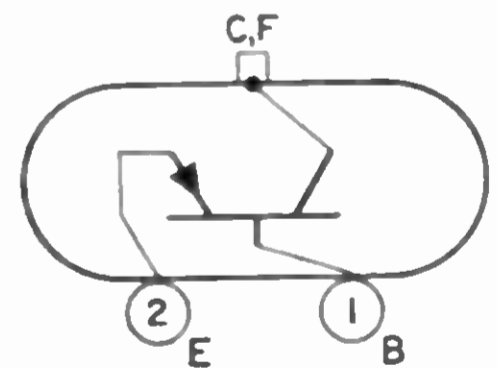
TYPICAL SMALL-SIGNAL FORWARD TRANSFER CONDUCTANCE AND SUSCEPTANCE CHARACTERISTICS



**2N2869 /
2N301**

POWER TRANSISTOR

Ge p-n-p alloy-junction type used in class A and class B af output-amplifier stages of automobile radio receivers and mobile communications equipment. JEDEC TO-3, Outline No.2.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-60	V
Collector-to-Emitter Voltage	V_{CEO}	-50	V
Emitter-to-Base Voltage	V_{EBO}	-10	V
Collector Current	I_C	-10	A
Emitter Current	I_E	10	A
Base Current	I_B	-3	A
Transistor Dissipation:			
T_{MF} up to 55°C	P_T	30	W
T_{MF} above 55°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 100	°C
Storage	T_{STG}	-65 to 100	°C
Pin-Soldering Temperature (10 s max)	T_P	255	°C

CHARACTERISTICS (At mounting-flange temperature = 25°C)

Collector-to-Base Breakdown Voltage ($I_C = 0.005\text{ A}, I_E = 0$)	$V_{(BR)CBO}$	-60 min	V
Collector-to-Emitter Breakdown Voltage ($I_C = -0.6\text{ A}, I_B = 0$)	$V_{(BR)CEO}$	-50 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -2\text{ mA}, I_C = 0$)	$V_{(BR)EBO}$	-10 min	V

CHARACTERISTICS (cont'd)

Collector-to-Emitter Saturation Voltage ($I_c = -5$ A, $I_B = -0.5$ A)	$V_{CE(sat)}$	-0.75 max	V
Base-to-Emitter Voltage ($V_{CE} = -2$ V, $I_c = -1$ A) ...	V_{BE}	-0.5 max	V
Collector-Cutoff Current: $V_{CB} = -30$ V, $I_E = 0$	I_{CBO}	-0.5 max	mA
$V_{CB} = -0.5$ V, $I_E = 0$	$I_{CBO(sat)}$	-0.1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = -2$ V, $I_c = -1$ A)	h_{FE}	50 to 165	
Gain-Bandwidth Product ($V_{CE} = -2$ V, $I_c = -1$ A) ...	f_T	200 min	kHz

TYPICAL OPERATION IN CLASS A POWER-AMPLIFIER CIRCUIT

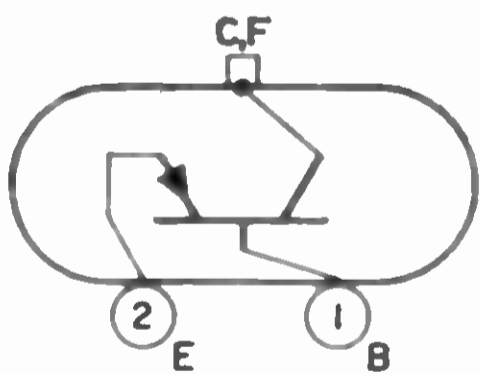
DC Collector-Supply Voltage	V_{CC}	-14.4	V
DC Collector-to-Emitter Voltage	V_{CE}	-12.2	V
DC Base-to-Emitter Voltage	V_{BE}	-0.35	V
Zero-Signal Collector Current	I_c	-0.9	A
Load Impedance	R_L	15	Ω
Signal Frequency	f	400	Hz
Signal-Source Impedance	R_s	10	Ω
Power Gain		38	dB
Total Harmonic Distortion (at a power output of 5 W)		5	%
Zero-Signal Collector Dissipation		11	W
Maximum-Signal Power Output	P_{OE}	5	W
Circuit Efficiency (at a power output of 5 W)	η	45	%

TYPICAL OPERATION IN "SINGLE-ENDED PUSH-PULL" CLASS B AF-AMPLIFIER CIRCUIT

DC Collector Supply Voltage	V_{CC}	-14.4	V
Zero-Signal DC Collector Current (per transistor) ...	I_c	-0.05	A
Zero-Signal Base-Bias Voltage		-0.13	V
Peak Collector Current (per transistor)	$i_c(\text{peak})$	-2	A
Maximum-Signal DC Collector Current (per transistor)	$I_c(\text{max})$	-0.64	A
Signal Frequency	f	400	Hz
Input Impedance of Stage (per base)	R_s	10	Ω
Load Impedance (per collector)	R_L	6	Ω
Power Gain		30	dB
Circuit Efficiency (at a power output of 12 W)	η	67	%
Maximum-Signal Power Output	P_{OE}	12	W
Total Harmonic Distortion (at maximum-signal power output of 12 W)		5	%
Maximum Collector Dissipation (per transistor at a power output of 12 W)		3	W

POWER TRANSISTOR

**2N2870/
2N301A**



Ge p-n-p alloy-junction type used in class A and class B af output-amplifier stages of automobile radio receivers and mobile communications equipment. JEDEC TO-3, Outline No.2. This type is identical with type 2N2869/2N301 except for the following items:

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-80	V
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CHARACTERISTICS

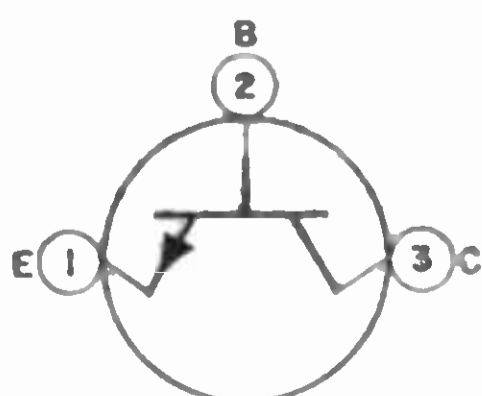
Collector-to-Base Breakdown Voltage ($I_c = -0.005$ A, $I_E = 0$)	$V_{(BR)CBO}$	-80 min	V
Collector-to-Emitter Saturation Voltage ($I_c = -5$ A, $I_B = -0.5$ A)	$V_{CE(sat)}$	-0.5 max	V

Refer to Chart of Discontinued Transistors

2N2873

POWER TRANSISTOR

2N2876



Si n-p-n triple-diffused planar type used in large-signal vhf applications such as AM, FM, and cw service at frequencies up to 150 MHz in industrial and military equipment. JEDEC TO-60, Outline No.23. See **Mounting Hardware** for desired mounting arrangement.

MAXIMUM RATINGS

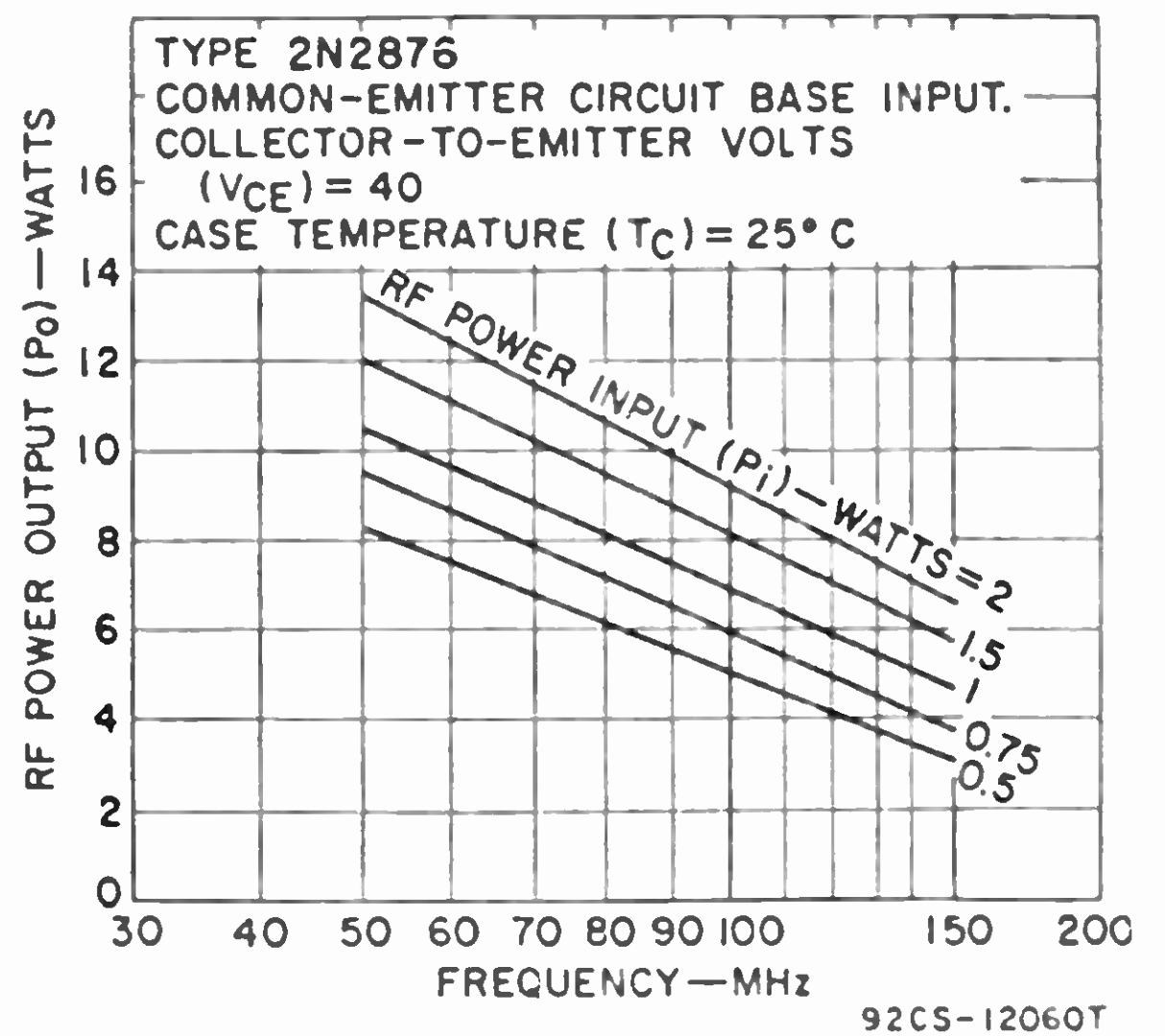
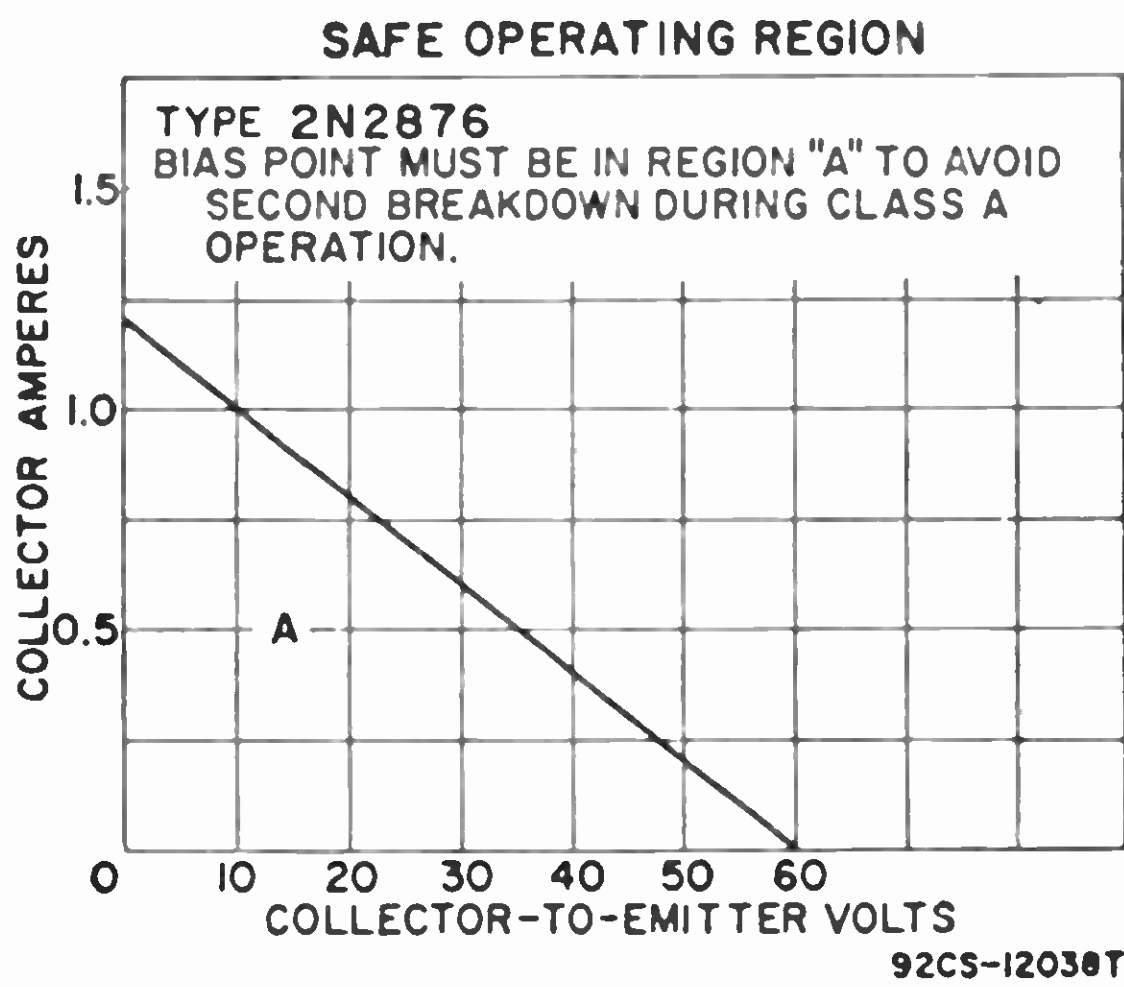
Collector-to-Base Voltage	V_{CBO}	80	V
Collector-to-Emitter Voltage:			
$V_{BE} = -1.5$ V	V_{CEV}	80	V
Base open	V_{CEO}	60	V
Emitter-to-Base Voltage	V_{EBO}	4	V
Collector Current	I_C	2.5	A
Transistor Dissipation:			
T_C up to 25°C	P_T	17.5	W
T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	230	°C

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Base Breakdown Voltage ($I_C = 0.5$ mA, $I_E = 0$)	$V_{(BR)CBO}$	80 min	V
Collector-to-Emitter Breakdown Voltage:			
$I_C = 0.5$ A, $I_B = 0$, $t_p \leq 5 \mu s$, $df \leq 1\%$	$V_{(BR)CEO}$ (sus)	60 min	V
$V_{BE} = -1.5$ V, $I_C = 0.1$ mA	$V_{(BR)CEV}$	80 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.1$ mA, $I_C = 0$)	$V_{(BR)EBO}$	4 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 2.5$ A, $I_B = 0.5$ A)	V_{CE} (sat)	1 max	V
Collector-Cutoff Current ($V_{CB} = 30$ V, $I_E = 0$)	I_{CBO}	0.1 max	μA
Intrinsic Base-Spreading Resistance ($V_{CE} = 28$ V, $I_C = 0.25$ A, $f = 400$ MHz)	$r_{bb'}$	6	Ω
RF Power Output, Unneutralized:			
$V_{CE} = 28$ V, $I_C = 0.5$ A, $P_{IE} = 2$ W, $f = 50$ MHz ...	P_{OE}	10 min	W
$V_{CE} = 28$ V, $I_C = 0.275$ A, $P_{IE} = 1$ W, $f = 150$ MHz	P_{OE}	3 min	W
Gain-Bandwidth Product ($V_{CE} = 28$ V, $I_C = 250$ mA)	f_T	200	MHz
Collector-to-Case Capacitance	C_c	6 max	pF
Output Capacitance ($V_{CB} = 30$ V, $I_E = 0$, $f = 0.14$ MHz)	C_{obo}	20 max*	pF

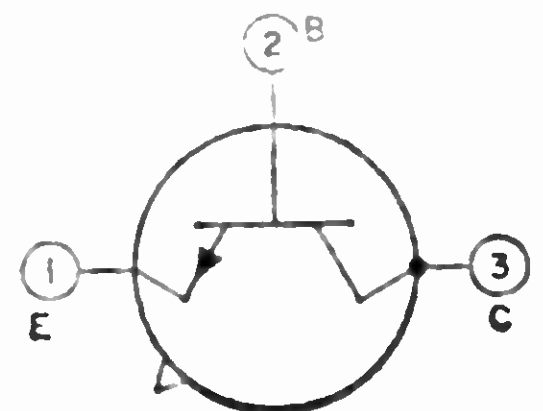
* This value applies only to type 2N2876.

TYPICAL OPERATION CHARACTERISTICS



2N2895 TRANSISTOR

Si n-p-n triple-diffused planar type used in a wide variety of small-signal and low-to-medium-power applications in military and industrial equipment. JEDEC TO-18, Outline No.12. For transfer-characteristics curves, refer to type 2N2102.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	120	V
Collector-to-Emitter Voltage:			
$R_{BE} \leq 10 \Omega$	V_{CER}	80	V
Base open	V_{CEO}	65	V

MAXIMUM RATINGS (cont'd)

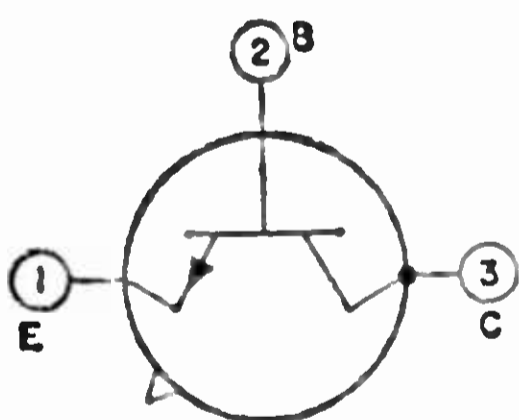
Emitter-to-Base Voltage	V_{EB0}	7	V
Collector Current	I_C	1	A
Transistor Dissipation:			
T_A up to 25°C	P_T	0.5	W
T_C up to 25°C	P_T	1.8	W
T_A or T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	255	°C

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Base Breakdown Voltage ($I_C = 0.1$ mA, $I_E = 0$)	$V_{(BR)CBO}$	120 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.1$ mA, $I_C = 0$)	$V_{(BR)EBO}$	7 min	V
Collector-to-Emitter Sustaining Voltage:			
$I_C = 100$ mA, $I_B = 0$, $t_p = 300$ μ s, $df = 1.8\%$	V_{CEO} (sus)	65 min	V
$I_C = 100$ mA, $I_B = 0$, $R_{BE} = 10$ Ω , $t_p = 300$ μ s, $df = 1.8\%$	V_{CEr} (sus)	80 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 150$ mA, $I_B = 15$ mA, $t_p = 300$ μ s, $df = 1.8\%$)	V_{CE} (sat)	0.6 max	V
Base-to-Emitter Saturation Voltage ($I_C = 150$ mA, $I_B = 15$ mA, $t_p = 300$ μ s, $df = 1.8\%$)	V_{BE} (sat)	1.2 max	V
Collector-Cutoff Current:			
$V_{CB} = 60$ V, $I_E = 0$, $T_C = 25^\circ$ C	I_{CBO}	0.002 max	μ A
$V_{CB} = 60$ V, $I_E = 0$, $T_C = 150^\circ$ C	I_{CBO}	2 max	μ A
Emitter-Cutoff Current ($V_{EB} = 5$ V, $I_C = 0$)	I_{EBO}	0.002 max	μ A
Pulsed Static Forward-Current Transfer Ratio:			
$V_{CE} = 10$ V, $I_C = 150$ mA, $t_p = 300$ μ s, $df = 1.8\%$	h_{FE} (pulsed)	40 to 120	
$V_{CE} = 10$ V, $I_C = 500$ mA, $t_p = 300$ μ s, $df = 1.8\%$	h_{FE} (pulsed)	25 min	
Static Forward-Current Transfer Ratio:			
$V_{CE} = 10$ V, $I_C = 0.01$ mA	h_{FE}	20 min	
$V_{CE} = 10$ V, $I_C = 10$ mA	h_{FE}	35 min	
$V_{CE} = 10$ V, $I_C = 10$ mA, $T_C = -55^\circ$ C	h_{FE}	20 min	
Small-Signal Forward-Current Transfer Ratio:			
$V_{CE} = 5$ V, $I_C = 5$ mA, $f = 1$ kHz	h_{fe}	50 to 200	
$V_{CE} = 10$ V, $I_C = 50$ mA, $f = 20$ MHz	h_{fe}	6 min	
Input Capacitance ($V_{EB} = 0.5$ V, $I_C = 0$, $f = 0.14$ MHz)	C_{ibo}	80 max	pF
Output Capacitance ($V_{CB} = 10$ V, $I_E = 0$, $f = 0.14$ MHz)	C_{obo}	15 max	pF
Noise Figure ($V_{CE} = 10$ V, $I_C = 0.3$ mA, $f = 1$ kHz, $R_G = 510$ Ω , circuit bandwidth = 1 Hz)	NF	8 max	dB
Thermal Resistance, Junction-to-Case	θ_{J-C}	97 max	°C/W
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	350 max	°C/W

TRANSISTOR

2N2896



Si n-p-n triple-diffused planar type used in a wide variety of small-signal and low-to-medium-power applications in military and industrial equipment. JEDEC TO-18, Outline No. 12. For transfer-characteristics curves, refer to type 2N2102.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	140	V
Collector-to-Emitter Voltage:			
$R_{BE} = 10$ Ω	V_{CER}	140	V
Base open	V_{CEO}	90	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Collector Current	I_C	1	A
Transistor Dissipation:			
T_A up to 25°C	P_T	0.5	W
T_C up to 25°C	P_T	1.8	W
T_A or T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	255	°C

CHARACTERISTICS (At case temperature = 25°C)

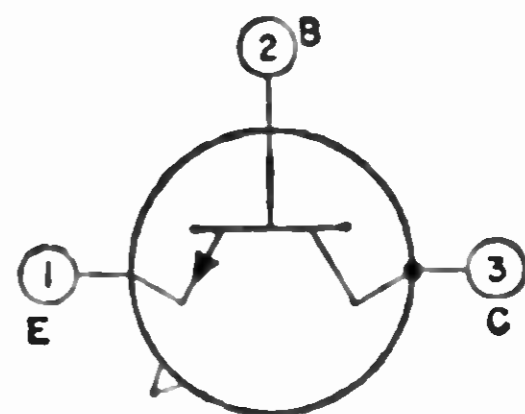
Collector-to-Base Breakdown Voltage ($I_C = 0.1$ mA, $I_E = 0$)	$V_{(BR)CBO}$	140 min	V
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MAXIMUM RATINGS (cont'd)

Emitter-to-Base Breakdown Voltage ($I_E = 0.1$ mA, $I_C = 0$)	$V_{(BR)EBO}$	7 min	V
Collector-to-Emitter Sustaining Voltage: $I_C = 100$ mA, $I_B = 0$, $t_p = 300$ μ s, $df = 1.8\%$	$V_{CEO(sus)}$	90 min	V
$I_C = 100$ mA, $I_B = 0$, $R_{BE} = 10$ Ω , $t_p = 300$ μ s, $df = 1.8\%$	$V_{CER(sus)}$	140 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 150$ mA, $I_B = 15$ mA, $t_p = 300$ μ s, $df = 1.8\%$)	$V_{CE(sat)}$	0.6 max	V
Base-to-Emitter Saturation Voltage ($I_C = 150$ mA, $I_B = 15$ mA, $t_p = 300$ μ s, $df = 1.8\%$)	$V_{BE(sat)}$	1.2 max	V
Collector-Cutoff Current: $V_{CB} = 90$ V, $I_E = 0$, $T_c = 25^\circ\text{C}$	I_{CBO}	0.01 max	μA
$V_{CB} = 90$ V, $I_E = 0$, $T_c = 150^\circ\text{C}$	I_{CBO}	10 max	μA
Emitter-Cutoff Current ($V_{EB} = 5$ V, $I_C = 0$)	I_{EBO}	0.01 max	μA
Pulsed Static Forward-Current Transfer Ratio ($V_{CE} = 10$ V, $I_C = 150$ mA, $t_p = 300$ μ s, $df = 1.8\%$)	$h_{FE(\text{pulsed})}$	60 to 200	
Static Forward-Current Transfer Ratio: $V_{CE} = 10$ V, $I_C = 1$ mA	h_{FE}	35 min	
$V_{CE} = 10$ V, $I_C = 10$ mA, $T_c = 55^\circ\text{C}$	h_{FE}	20 min	
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 10$ V, $I_C = 50$ mA, $f = 20$ MHz)	h_{fe}	6 min	
Output Capacitance ($V_{CB} = 10$ V, $I_E = 0$, $f = 0.14$ MHz)	C_{obo}	15 max	pF
Thermal Resistance, Junction-to-Case	Θ_{J-C}	97 max	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	Θ_{J-A}	350 max	$^\circ\text{C/W}$

2N2897**TRANSISTOR**

Si n-p-n triple-diffused planar type used in a wide variety of small-signal and low-to-medium-power applications in military and industrial equipment. JEDEC TO-18, Outline No.12.

**MAXIMUM RATINGS**

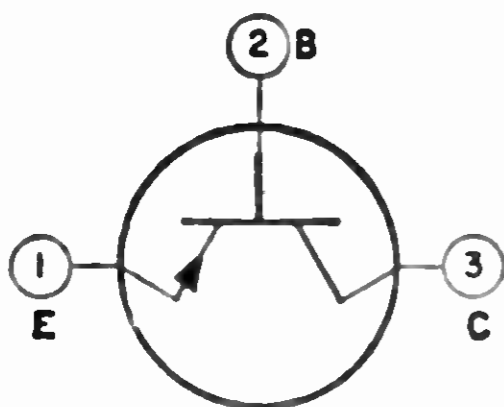
Collector-to-Base Voltage	V_{CBO}	60	V
Collector-to-Emitter Voltage: $R_{BE} = 10$ Ω	V_{CER}	60	V
Base open	V_{CEO}	45	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Collector Current	I_C	1	A
Transistor Dissipation: T_A up to 25°C	P_T	0.5	W
T_c up to 25°C	P_T	1.8	W
T_A or T_c above 25°C	P_T	See curve page 300	
Temperature Range: Operating (Junction)	$T_J(\text{opr})$	-65 to 200	$^\circ\text{C}$
Storage	T_{STG}	-65 to 200	$^\circ\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	255	$^\circ\text{C}$

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Base Breakdown Voltage ($I_C = 0.1$ mA, $I_E = 0$)	$V_{(BR)CBO}$	60 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.1$ mA, $I_C = 0$)	$V_{(BR)EBO}$	7 min	V
Collector-to-Emitter Sustaining Voltage: $I_C = 100$ mA, $I_B = 0$, $t_p = 300$ μ s, $df = 1.8\%$	$V_{CEO(sus)}$	45 min	V
$I_C = 100$ mA, $I_B = 0$, $R_{BE} = 10$ Ω , $t_p = 300$ μ s, $df = 1.8\%$	$V_{CER(sus)}$	60 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 150$ mA, $I_B = 15$ mA, $t_p = 300$ μ s, $df = 1.8\%$)	$V_{CE(sat)}$	1 max	V
Base-to-Emitter Saturation Voltage ($I_C = 150$ mA, $I_B = 15$ mA, $t_p = 300$ μ s, $df = 1.8\%$)	$V_{BE(sat)}$	1.3 max	V
Collector-Cutoff Current: $V_{CB} = 60$ V, $I_E = 0$, $T_A = 25^\circ\text{C}$	I_{CBO}	0.05 max	μA
$V_{CB} = 60$ V, $I_E = 0$, $T_A = 150^\circ\text{C}$	I_{CBO}	50 max	μA
Emitter-Cutoff Current ($V_{EB} = 5$ V, $I_C = 0$)	I_{EBO}	0.05 max	μA
Pulsed Static Forward-Current Transfer Ratio ($V_{CE} = 10$ V, $I_C = 150$ mA, $t_p = 300$ μ s, $df = 1.8\%$)	$h_{FE(\text{pulsed})}$	50 to 200	
Static Forward-Current Transfer Ratio ($V_{CE} = 10$ V, $I_C = 0.1$ mA)	h_{FE}	35 min	
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 10$ V, $I_C = 50$ mA, $f = 20$ MHz)	h_{fe}	5 min	
Output Capacitance ($V_{CB} = 10$ V, $I_E = 0$, $f = 0.14$ MHz)	C_{obo}	15 max	pF

CHARACTERISTICS (cont'd)

Thermal Resistance, Junction-to-Case	θ_{J-C}	97 max	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	350 max	$^{\circ}\text{C/W}$
Refer to Chart of Discontinued Transistors		2N2898	
Refer to Chart of Discontinued Transistors		2N2899	
Refer to Chart of Discontinued Transistors		2N2900	
Refer to Chart of Discontinued Transistors		2N2938	



TRANSISTOR

2N2953

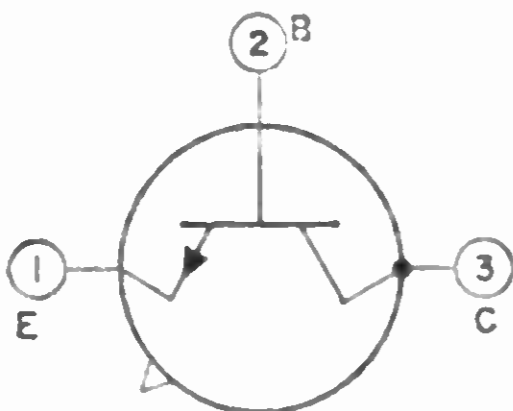
Ge p-n-p alloy-junction type used in af-driver amplifier applications in consumer and industrial equipment. JEDEC TO-1, Outline No.1.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CB0}	-30	V
Collector-to-Emitter Voltage ($R_{BE} = 10\text{ k}\Omega$)	V_{CER}	-25	V
Emitter-to-Base Voltage	V_{EBO}	25	V
Collector Current	I_C	-0.15	A
Emitter Current	I_E	0.15	A
Transistor Dissipation:			
T_A up to 55°C	P_T	120	mW
T_C up to 55°C (in an infinite heat sink)	P_T	300	mW
T_C up to 55°C (with practical heat sink, $\theta = 50^{\circ}\text{C/W}$)	P_T	225	mW
T_A or T_C (with practical heat sink) above 55°C ...	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 100	$^{\circ}\text{C}$
Storage	T_{STG}	-65 to 100	$^{\circ}\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	255	$^{\circ}\text{C}$

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = -0.05\text{ A}$, $V_{EB} = -2\text{ V}$)	$V_{(BR)CBV}$	-30 min	V
Collector-to-Emitter Breakdown Voltage ($I_C = -1\text{ mA}$, $R_{BE} = 10\text{ k}\Omega$)	$V_{(BR)CER}$	-25 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -0.05\text{ mA}$, $I_C = 0$)	$V_{(BR)EBO}$	-25 min	V
Collector-Cutoff Current ($V_{CB} = -20\text{ V}$, $I_E = 0$)	I_{CBO}	-5 max	μA
Emitter-Cutoff Current ($V_{EB} = -20\text{ V}$, $I_C = 0$)	I_{EBO}	-7.5 max	μA
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = -10\text{ V}$, $I_C = -10\text{ mA}$, $f = 1\text{ kHz}$)	h_{fe}	200 min	
Small-Signal Forward-Current Transfer-Ratio Cutoff Frequency ($V_{CE} = -12\text{ V}$, $I_C = -1\text{ mA}$)	f_{hfb}	10	MHz
Intrinsic Base-Spreading Resistance ($V_{CE} = -10\text{ V}$, $I_C = -10\text{ mA}$, $f = 20\text{ MHz}$)	$r_{bb'}$	300	Ω
Collector-to-Base Feedback Capacitance ($V_{CE} = -12\text{ V}$, $I_C = -1\text{ mA}$)	$c_{b'c}$	6.5	pF



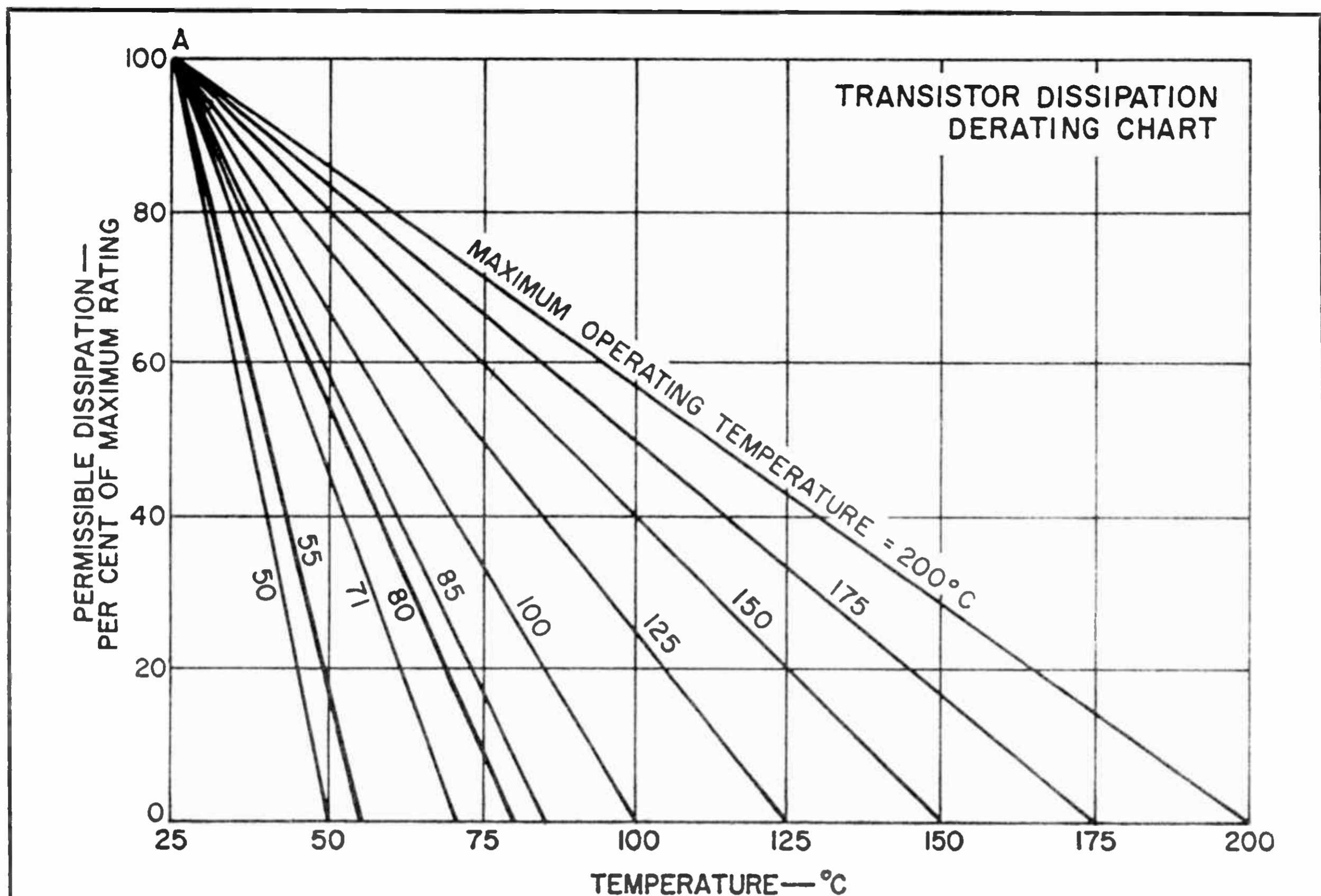
COMPUTER TRANSISTOR

2N3011

Si n-p-n epitaxial planar type used for high-speed saturated switching in logic applications. JEDEC TO-18, Outline No.12.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CB0}	30	V
Collector-to-Emitter Voltage	V_{CEO}	12	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	0.2	A
Transistor Dissipation:			
T_A up to 25°C	P_T	0.36	W
T_C up to 25°C	P_T	1.2	W
T_A or T_C above 25°C	P_T	See curve page 300	



For many transistors, the maximum value of dissipation is specified for ambient, case, or mounting-flange temperatures up to 25°C, and must be reduced linearly for higher temperatures. For such types, the chart above can be used to determine maximum permissible dissipation values at particular temperature conditions above 25°C. (This chart cannot be assumed to apply to types other than those for which it is specified in the data section.) The curves show the permissible percentage of the maximum dissipation ratings as a function of ambient or case temperature. Individual curves are plotted for maximum operating temperatures of 50, 55, 71, 80, 85, 100, 125, 150, 175, and 200°C. If the maximum operating temperature of a transistor is some other value, a new curve can be drawn from point A in the figure to the desired temperature value on the abscissa.

To use the chart, it is necessary to know the maximum dissipation rating and the maximum operating temperature for a given transistor.

The calculation involves only two steps:

1. A vertical line is drawn at the desired operating temperature value on the abscissa to intersect the curve representing the maximum operating temperature for the transistor.

2. A horizontal line drawn from this intersection point to the ordinate establishes the permissible percentage of the maximum dissipation at the given temperature.

The following example illustrates the calculation of the maximum permissible dissipation for transistor type 2N1487 at a case temperature of 100°C. This type has a maximum dissipation rating of 75 watts at a case temperature of 25°C, and a maximum permissible case-temperature rating of 200°C.

1. A perpendicular line is drawn from the 100-degree point on the abscissa to the 200-degree curve.

2. Projection of this point to the ordinate shows a percentage of 57.5.

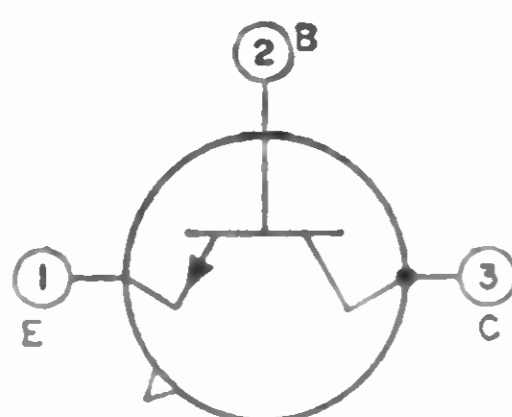
Therefore, the maximum permissible dissipation for the 2N1487 at a case temperature of 100°C is 0.575 times 75, or approximately 43 watts.

MAXIMUM RATINGS (cont'd)

Temperature Range:			
Operating (Junction)	T _J (opr)	−65 to 200	°C
Storage	T _{STG}	−65 to 200	°C
Lead-Soldering Temperature (60 s max)	T _L	300	°C

CHARACTERISTICS

Collector-to-Base Breakdown Voltage (I _C = 0.01 mA, I _E = 0)	V _{(BR)CBO}	30 min	V
Collector-to-Emitter Breakdown Voltage (I _C = 0.01 mA, V _{EB} = 0)	V _{(BR)CES}	30 min	V
Emitter-to-Base Breakdown Voltage (I _E = 0.1 mA, I _C = 0)	V _{(BR)EBO}	5 min	V
Collector-to-Emitter Sustaining Voltage (I _C = 10 mA, I _B = 0, t _p = 300 μs, df = 2%)	V _{CEO(SUS)}	12 min	V
Collector-to-Emitter Saturation Voltage:			
I _C = 10 mA, I _B = 1 mA, T _A = 25°C	V _{CE(sat)}	0.2 max	V
I _C = 10 mA, I _B = 1 mA, T _A = 85°C	V _{CE(sat)}	0.3 max	V
I _C = 100 mA, I _B = 10 mA, T _A = 25°C	V _{CE(sat)}	0.5 max	V
I _C = 30 mA, I _B = 3 mA, t _p = 300 μs, df = 2%, T _A = 25°C	V _{CE(sat)pulsed}	0.25 max	V
Base-to-Emitter Saturation Voltage:			
I _C = 10 mA, I _B = 1 mA	V _{BE(sat)}	0.72 to 0.87	V
I _C = 30 mA, I _B = 3 mA, T _A = 25°C	V _{BE(sat)}	1.15 max	V
I _C = 100 mA, I _B = 10 mA	V _{BE(sat)}	1.6 max	V
Collector-Cutoff Current:			
V _{CE} = 20 V, V _{EB} = 0, T _A = 85°C	I _{CES}	10 max	μA
V _{CE} = 20 V, V _{EB} = 0, T _A = 25°C	I _{CES}	0.4 max	μA
Pulsed Static Forward-Current Transfer Ratio:			
V _{CE} = 0.35 V, I _C = 10 mA, t _p = 300 μs, df = 2%	h _{FE(pulsed)}	30 to 120	
V _{CE} = 0.4 V, I _C = 30 mA, t _p = 300 μs, df = 2%	h _{FE(pulsed)}	25 min	
V _{CE} = 1 V, I _C = 100 mA, t _p = 300 μs, df = 2%	h _{FE(pulsed)}	12 min	
Small-Signal Forward-Current Transfer Ratio (V _{CE} = 10 V, I _C = 20 mA, f = 100 MHz)	h _{FE}	4 min	
Output Capacitance (V _{CB} = 5 V, I _E = 0, f = 0.14 MHz)	C _{obo}	4 max	pF
Storage Time (V _{CC} = 10 V, I _C = 10 mA, I _{B1} = 10 mA, I _{B2} = −10 mA)	t _s	13 max	ns
Turn-On Time (V _{CC} = 2 V, I _C = 10 mA, I _{B1} = 3 mA, V _{BE} (off) = 0 V)	t _d + t _r	15 max	ns
Turn-Off Time (V _{CC} = 2 V, I _C = 30 mA, I _{B1} = 3 mA, I _{B2} = −3 mA)	t _s + t _r	20 max	ns



POWER TRANSISTOR

2N3053

Si n-p-n triple-diffused planar type used in a wide variety of small signal, medium-power applications (up to 20 MHz) in commercial and industrial equipment. JEDEC TO-5, Outline No.5.

MAXIMUM RATINGS

Collector-to-Base Voltage	V _{CBO}	60	V
Collector-to-Emitter Sustaining Voltage:			
V _{BE} = −1.5 V	V _{CEV(SUS)}	60	V
R _{FE} = 10 Ω	V _{CER(SUS)}	50	V
Base open	V _{CEO(SUS)}	40	V
Emitter-to-Base Voltage	V _{EBO}	5	V
Collector Current	I _C	0.7	A
Transistor Dissipation:			
T _A up to 25°C	P _T	1	W
T _C up to 25°C	P _T	5	W
T _A or T _C above 25°C	P _T	See curve page 300	
Temperature Range:			
Operating (T _A -T _C) and Storage (T _{STG})		−65 to 200	°C
Lead-Soldering Temperature (10 s max)	T _L	255	°C

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Base Breakdown Voltage (I _C = 0.1 mA, I _E = 0)	V _{(BR)CBO}	60 min	V
Emitter-to-Base Breakdown Voltage (I _E = 0.1 mA, I _C = 0)	V _{(BR)EBO}	5 min	V

CHARACTERISTICS (cont'd)

Collector-to-Emitter Sustaining Voltage:

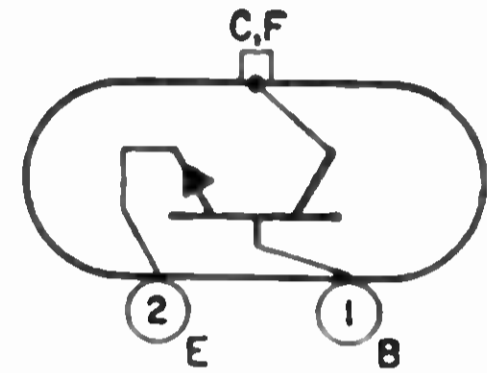
$I_C = 100 \text{ mA}$, $R_{BE} = 10 \Omega$, $t_p = 300 \mu\text{s}$, $df = 1.8\%$	$V_{CE(sus)}$	50 min	V
$I_C = 100 \text{ mA}$, $I_B = 0$, $t_p = 300 \mu\text{s}$, $df = 1.8\%$	$V_{CE(sus)}$	40 min	V
Base-to-Emitter Saturation Voltage ($I_C = 150 \text{ mA}$, $I_B = 15 \text{ mA}$)	$V_{BE(sat)}$	1.7 max	V
Collector-to-Emitter Saturation Voltage ($I_C = 150 \text{ mA}$, $I_B = 15 \text{ mA}$)	$V_{CE(sat)}$	1.4 max	V
Collector-Cutoff Current ($V_{CB} = 30 \text{ V}$, $I_E = 0$)	I_{CBO}	0.25 max	μA
Emitter-Cutoff Current ($V_{EB} = 4 \text{ V}$, $I_C = 0$)	I_{EBO}	0.25 max	μA
Pulsed Static Forward-Current Transfer Ratio ($V_{CE} = 10 \text{ V}$, $I_C = 150 \text{ mA}$, $t_p = 300 \mu\text{s}$, $df = 1.8\%$)	$h_{FE(pulsed)}$	50 to 250	
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 10 \text{ V}$, $I_C = 50 \text{ mA}$, $f = 20 \text{ MHz}$)	h_{fe}	5 min	
Input Capacitance ($V_{EB} = 0.5 \text{ V}$, $I_C = 0$)	C_{ibo}	80 max	pF
Output Capacitance ($V_{CB} = 10 \text{ V}$, $I_E = 0$)	C_{obo}	15 max	pF
Thermal Resistance, Junction-to-Case	θ_{J-C}	35* max	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	175• max	$^\circ\text{C/W}$

* This value does not apply to type 40389.

• This value does not apply to type 40392.

2N3054 POWER TRANSISTOR

Si n-p-n diffused-junction type used in power-switching circuits, series- and shunt-regulator driver and output stages, and high-fidelity amplifiers in commercial and industrial equipment. JEDEC TO-66, Outline No.25. See Mounting Hardware for desired mounting arrangement.

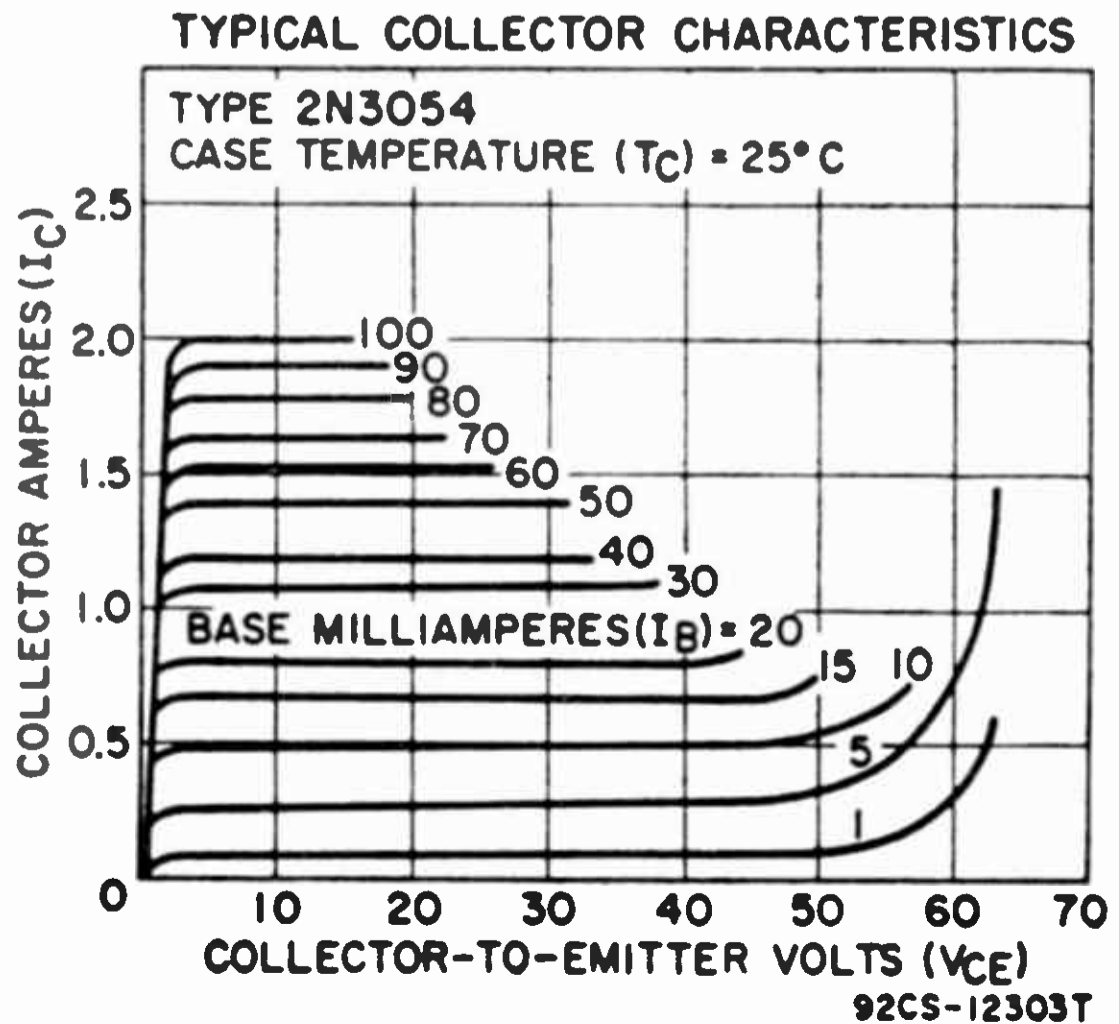
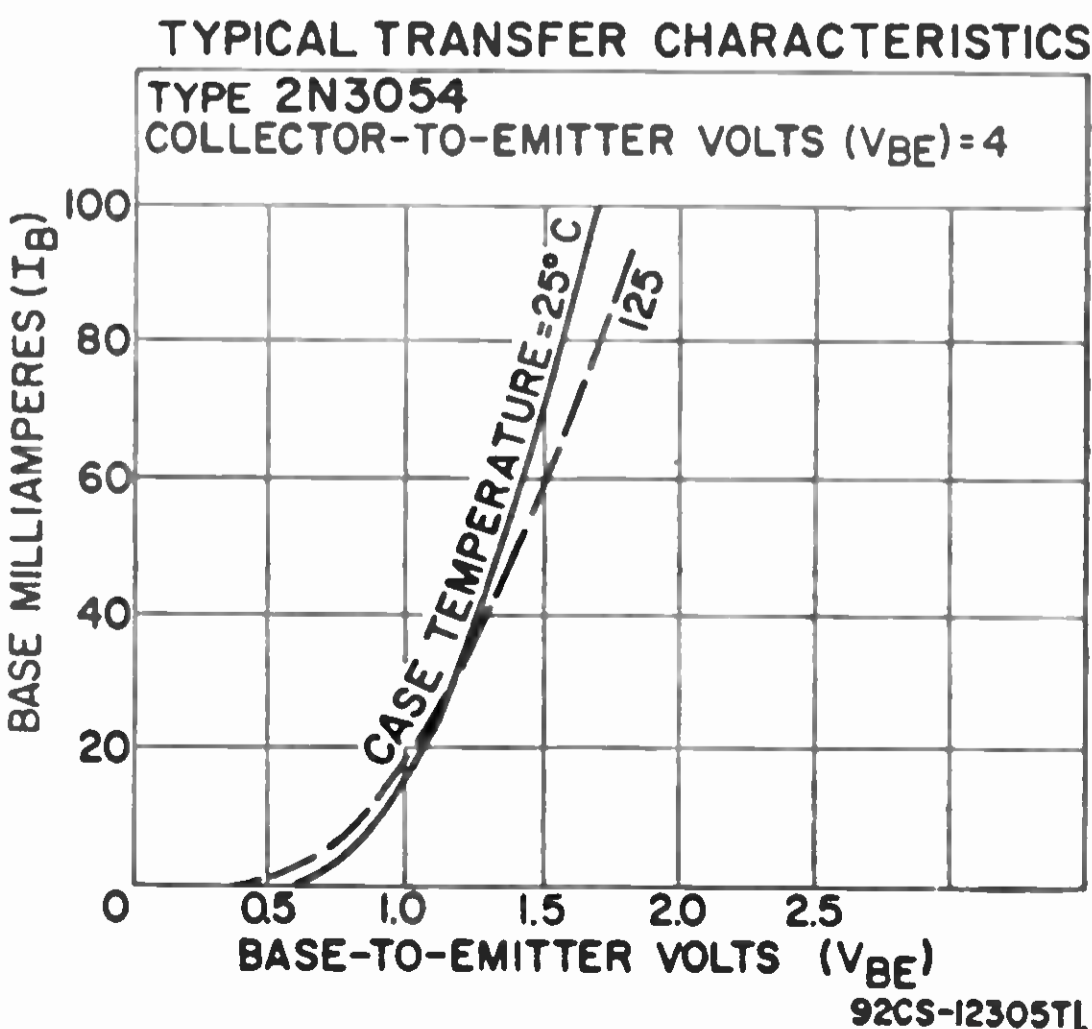


MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	90	V
Collector-to-Emitter Sustaining Voltage: $V_{BE} = -1.5 \text{ V}$	$V_{CEV(sus)}$	90	V
$R_{BE} = 100 \Omega$	$V_{CER(sus)}$	60	V
Base open	$V_{CEO(sus)}$	55	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Collector Current	I_C	4	A
Base Current	I_B	2	A
Transistor Dissipation: T_C up to 25°C	P_T	29	W
T_C above 25°C	P_T	See curve page 300	
Temperature Range: Operating (T_C) and Storage (T_{STG})	T_P	-65 to 200	$^\circ\text{C}$
Pin-Soldering Temperature (10 s max)	T_P	235	$^\circ\text{C}$

CHARACTERISTICS (At case temperature = 25°C)

Emitter-to-Base Breakdown Voltage ($I_E = 1 \text{ mA}$, $I_C = 0$)	$V_{(BR)EBO}$	7 min	V
Collector-to-Emitter Sustaining Voltage: $I_C = 100 \text{ mA}$, $R_{BE} = 100 \Omega$	$V_{CER(sus)}$	60 min	V
$I_C = 100 \text{ mA}$, $I_B = 0$	$V_{CEO(sus)}$	55 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 500 \text{ mA}$, $I_B = 50 \text{ mA}$)	$V_{CE(sat)}$	1 max	V



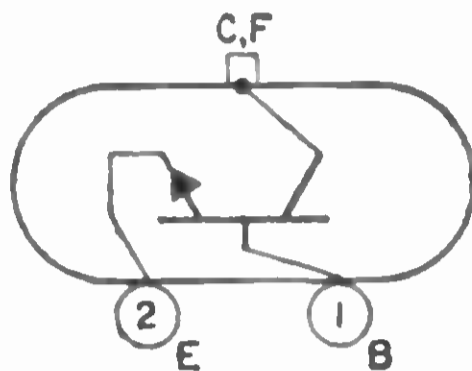
CHARACTERISTICS (cont'd)

Base-to-Emitter Voltage ($V_{CE} = 4 \text{ V}$, $I_C = 500 \text{ mA}$) ...	V_{BE}	1.7 max	V
Collector-Cutoff Current:			
$V_{CE} = 90 \text{ V}$, $V_{BE} = -1.5 \text{ V}$	I_{CEV}	1 max	mA
$V_{CE} = 30 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 150^\circ\text{C}$	I_{CEV}	5 max	mA
Emitter-Cutoff Current ($V_{EB} = 7 \text{ V}$, $I_C = 0$)	I_{EBO}	1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 4 \text{ V}$, $I_C = 500 \text{ mA}$)	h_{FE}	25 to 100	
Thermal Resistance, Junction-to-Case	θ_{J-C}	6* max	$^\circ\text{C/W}$

* This value applies only to type 2N3054.

POWER TRANSISTOR

2N3055



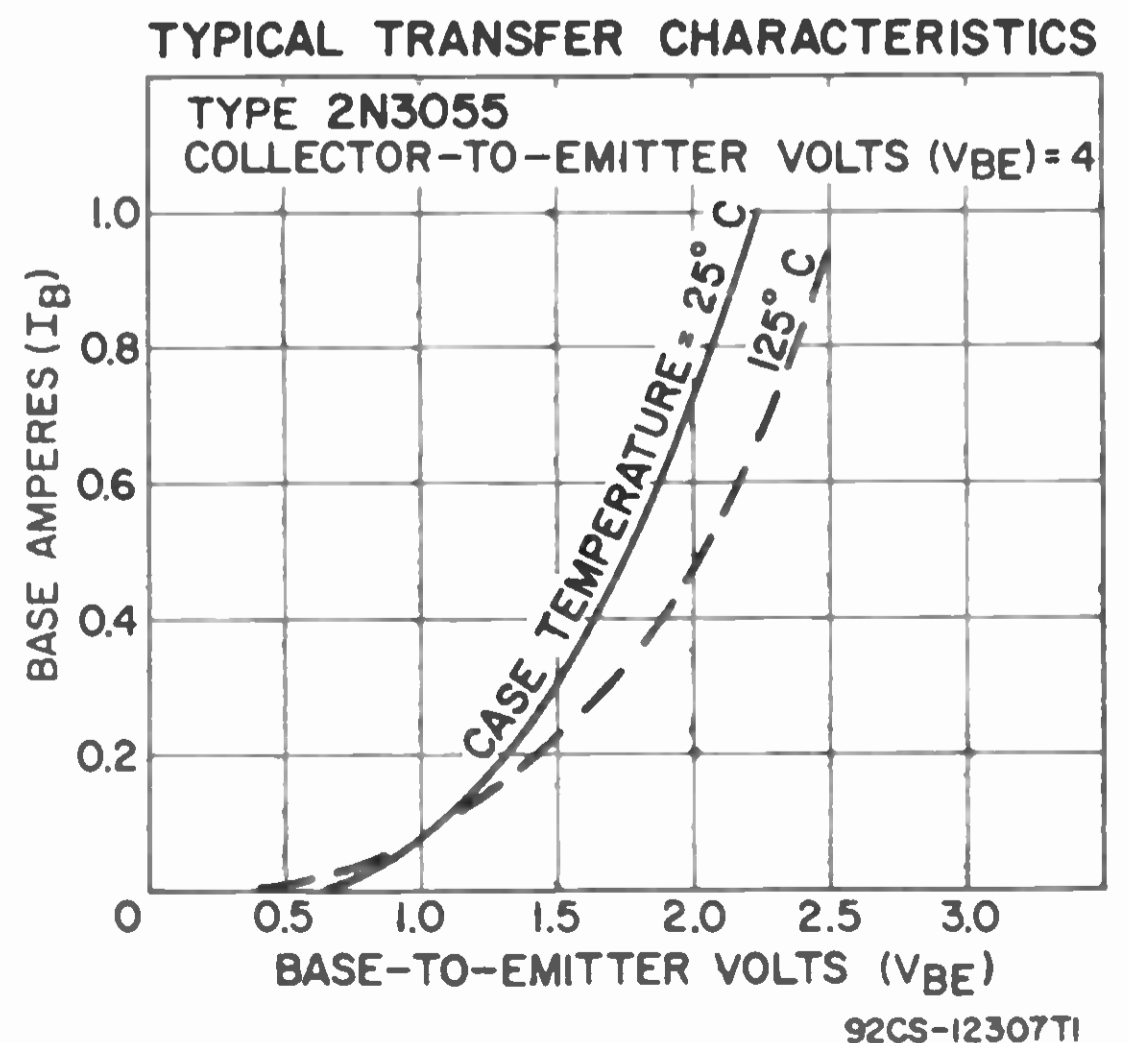
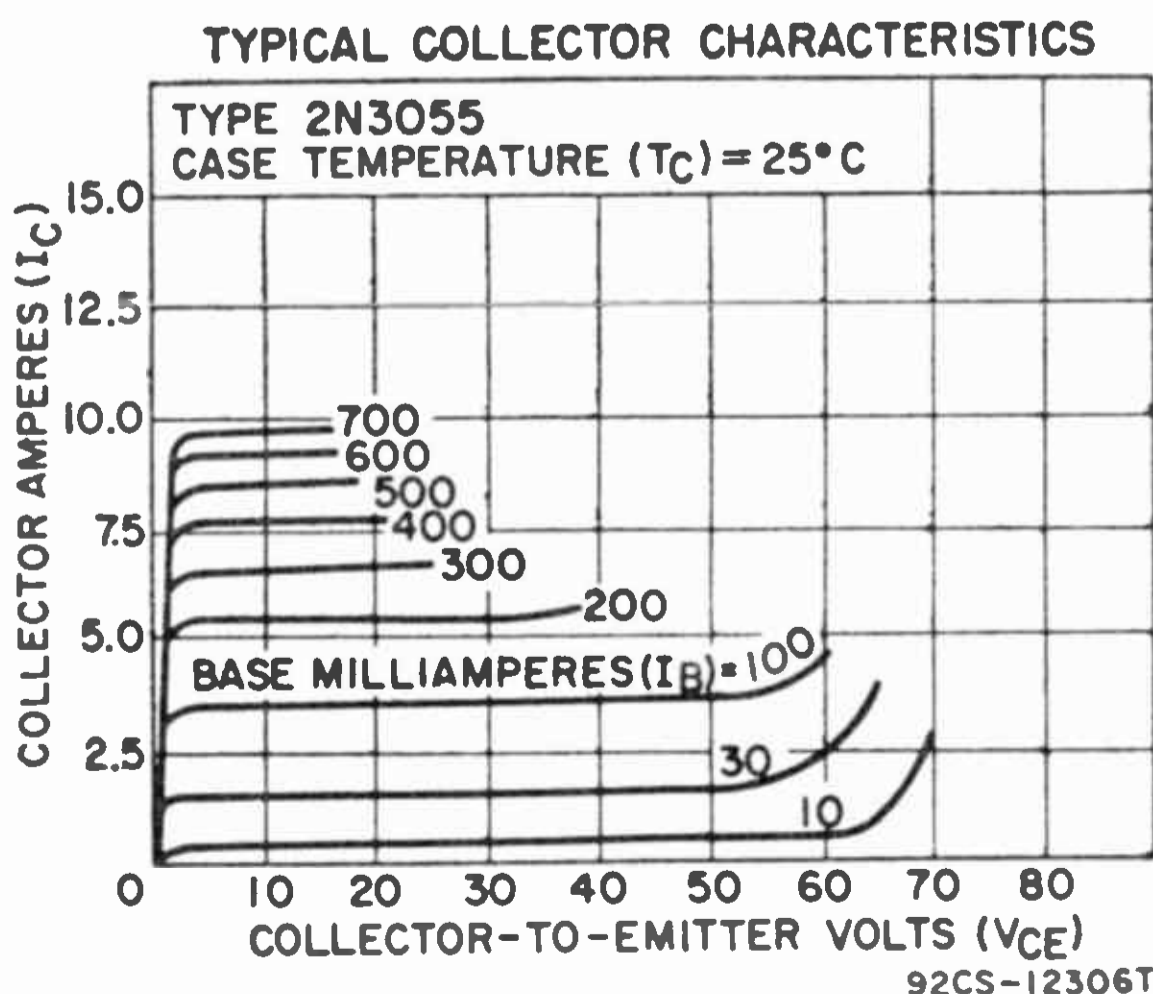
Si n-p-n diffused-junction type used in power-switching circuits, series- and shunt-regulator driver and output stages, and high-fidelity amplifiers in commercial and industrial equipment. JEDEC TO-3, Outline No.2. See Mounting Hardware for desired mounting arrangement.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	100	V
Collector-to-Emitter Sustaining Voltage:			
$V_{BE} = -1.5 \text{ V}$	$V_{CEV}(\text{SUS})$	100	V
$R_{BE} = 100 \Omega$	$V_{CER}(\text{SUS})$	70	V
Base open	$V_{CEO}(\text{SUS})$	60	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Collector Current	I_C	15	A
Base Current	I_B	7	A
Transistor Dissipation:			
T_C up to 25°C	P_T	115	W
T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (T_C) and Storage (T_{STG})		-65 to 200	$^\circ\text{C}$
Pin-Soldering Temperature (10 s max)	T_P	235	$^\circ\text{C}$

CHARACTERISTICS (At case temperature = 25°C)

Emitter-to-Base Breakdown Voltage ($I_E = 5 \text{ mA}$, $I_C = 0$)	$V_{(BR)EBO}$	7 min	V
Collector-to-Emitter Sustaining Voltage:			
$I_C = 200 \text{ mA}$, $R_{BE} = 100 \Omega$	$V_{CER}(\text{SUS})$	70 min	V
$I_C = 200 \text{ mA}$, $I_B = 0$	$V_{CEO}(\text{SUS})$	60 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 4 \text{ A}$, $I_B = 400 \text{ mA}$)	$V_{CE}(\text{sat})$	1.1 max	V
Base-to-Emitter Voltage ($V_{CE} = 4 \text{ V}$, $I_C = 4 \text{ A}$, $t_p = 300 \mu\text{s}$, $df = 1.8\%$)	V_{BE}	1.8 max	V
Collector-Cutoff Current:			
$V_{CE} = 100 \text{ V}$, $V_{BE} = -1.5 \text{ V}$	I_{CEV}	5	mA
$V_{CE} = 60 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 150^\circ\text{C}$	I_{CEV}	10	mA
Emitter-Cutoff Current ($V_{EB} = 7 \text{ V}$, $I_C = 0$)	I_{EBO}	5 max	mA
Pulsed Static Forward-Current Transfer Ratio ($V_{CE} = 4 \text{ V}$, $I_C = 4 \text{ A}$, $t_p = 300 \mu\text{s}$, $df = 1.8\%$) ...	$h_{FE}(\text{pulsed})$	20 to 70	



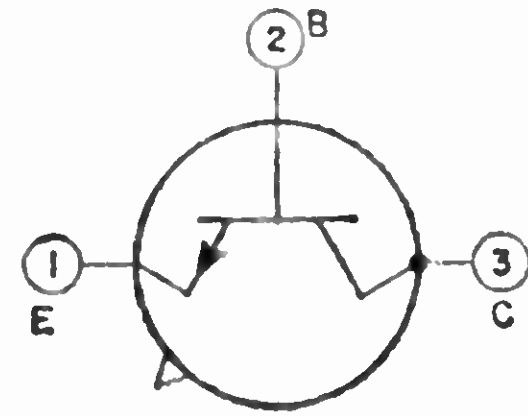
CHARACTERISTICS (cont'd)

Power Rating Test

$(V_{CE} = 39\text{ V, } I_C = 3\text{ A, } t = 1\text{ s})$		115	W
Thermal Resistance, Junction-to-Case	θ_{J-C}	1.5	$^{\circ}\text{C/W}$

2N3118 TRANSISTOR

Si n-p-n triple-diffused planar type for large-signal vhf class C and small-signal vhf class A amplifier applications in industrial and military communications equipment JEDEC TO-5, Outline No.5.



MAXIMUM RATINGS

Collector-to-Emitter Voltage:

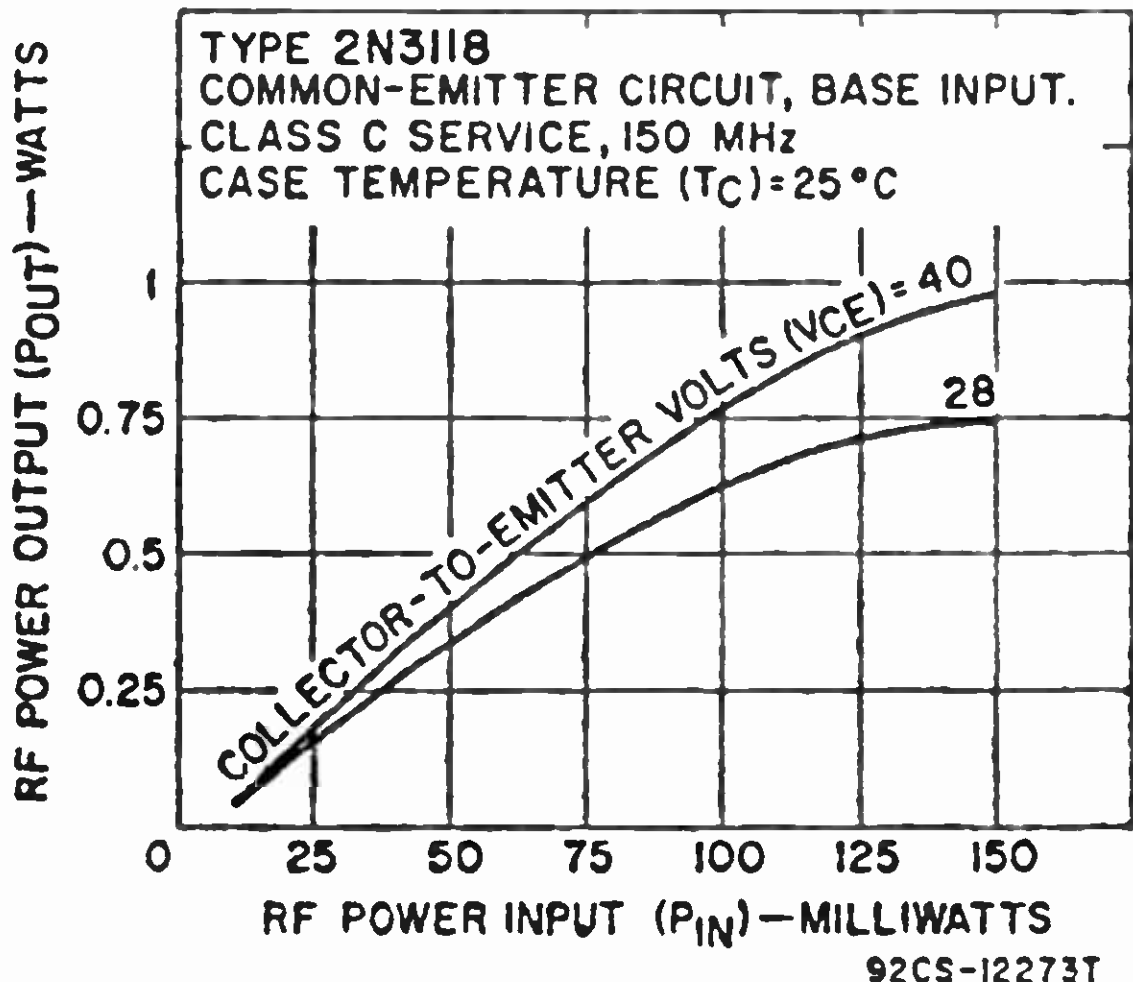
$V_{BE} = -1.5\text{ V}$	V_{CEV}	85	V
Base open	V_{CEO}	60	V
Emitter-to-Base Voltage	V_{EBO}	4	V
Collector Current	I_C	0.5	A
Transistor Dissipation:			
T_A up to 25°C	P_T	1	W
T_C up to 25°C	P_T	4	W
T_A or T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	$^{\circ}\text{C}$
Storage	T_{STG}	-65 to 200	$^{\circ}\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	255	$^{\circ}\text{C}$

CHARACTERISTICS (At case temperature = 25°C)

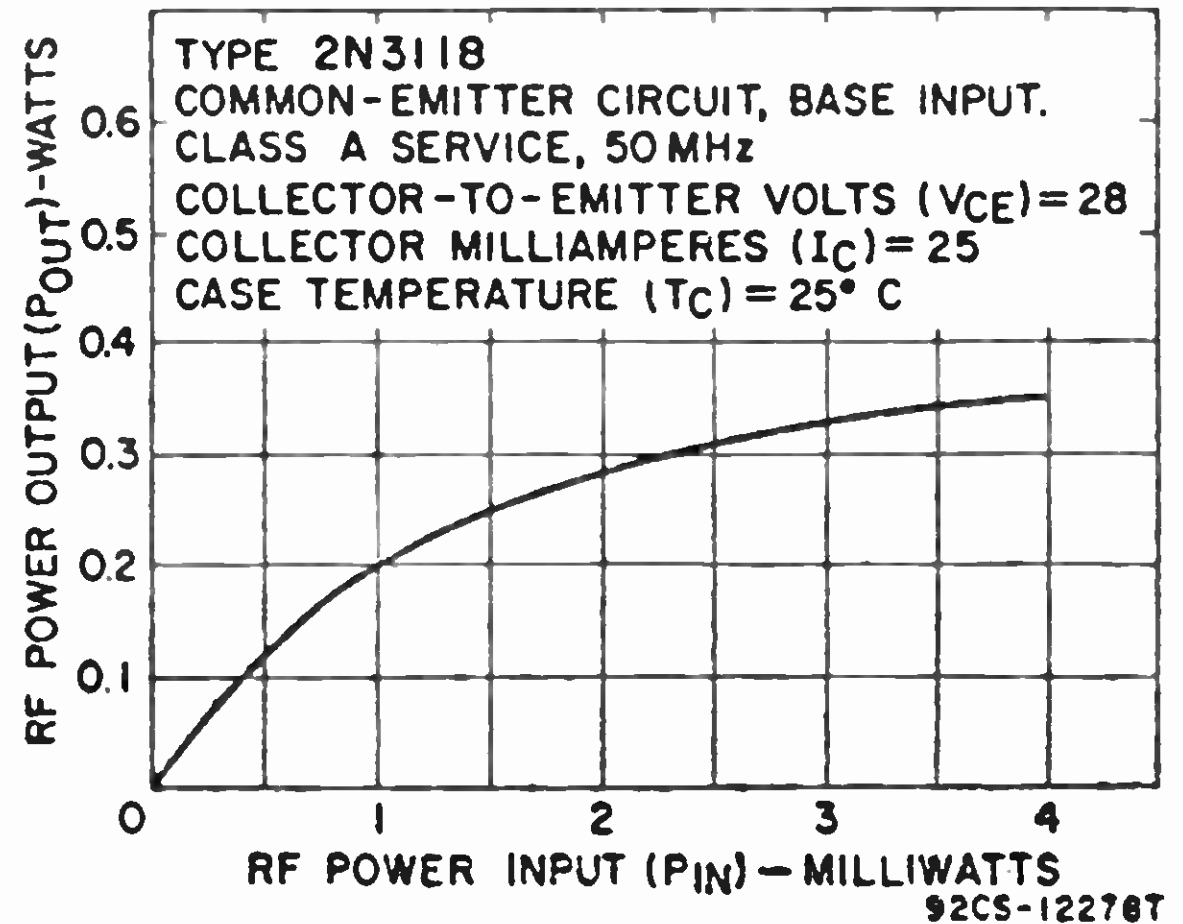
Collector-to-Emitter Breakdown Voltage:

$V_{BE} = -1.5\text{ V, } I_C = 0.1\text{ mA}$	$V_{(BR)CEV}$	85 min	V
$I_C = 10\text{ mA, } I_B = 0, t_p = 300\ \mu\text{s, } df = 1.8\%$	$V_{(BR)CEO}$ (SUS)	60 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.1\text{ mA, } I_C = 0$)	$V_{(BR)EBO}$	4 min	V
Collector-Cutoff Current:			
$V_{CB} = 30\text{ V, } I_E = 0, T_A = 25^{\circ}\text{C}$	I_{CBO}	0.1 max	μA
$V_{CB} = 30\text{ V, } I_E = 0, T_A = 150^{\circ}\text{C}$	I_{CBO}	100 max	μA
Small-Signal Short-Circuit Input Impedance, Real Part ($V_{CE} = 28\text{ V, } I_C = 25\text{ mA, } f = 50\text{ MHz}$)			
	R_e (h_{ie})	25 to 75	Ω
Small-Signal Short-Circuit Output Impedance, Real Part ($V_{CE} = 28\text{ V, } I_C = 25\text{ mA, } f = 50\text{ MHz}$)			
	$\frac{1}{Y_{22}}$ (real)	500 to 1000	Ω
Pulsed Static Forward-Current Transfer Ratio ($V_{CE} = 28\text{ V, } I_C = 25\text{ mA, } t_p = 300\ \mu\text{s, } df \leq 1.8\%$)			
	h_{FE} (pulsed)	50 to 275	
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 28\text{ V, } I_C = 25\text{ mA, } f = 50\text{ MHz}$)			
	h_{FE}	5 min	
$r_{bb'}$ $cb'e$ Product ($V_{CB} = 28\text{ V, } I_C = 25\text{ mA, } f = 50\text{ MHz}$)			
	$r_{bb'}$ $cb'e$	60 max	ps
Power Gain, Class A Service (with heat sink) ($V_{CE} = 28\text{ V, } I_C = 25\text{ mA, } P_{oe} = 0.2\text{ W, } f = 50\text{ MHz}$)			
	G_{pe}	18 min	dB
Collector-to-Base Feedback Capacitance ($V_{CB} = 28\text{ V, } I_C = 0, f = 1\text{ MHz}$)			
	$C_{b'e}$	6 max	pF

TYPICAL LARGE-SIGNAL CLASS C RF POWER-OUTPUT CHARACTERISTICS



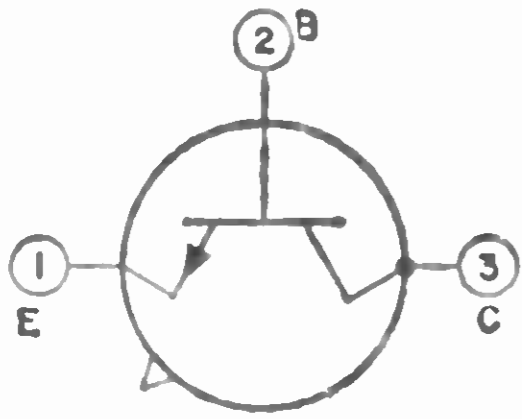
TYPICAL CLASS A RF POWER-OUTPUT CHARACTERISTIC



CHARACTERISTICS (cont'd)

Power Output, Class C Oscillator Service (with heat sink):

$V_{CE} = 28\text{ V}, P_{ie} = 0.1\text{ W}, f = 50\text{ MHz}$	P_{oe}	1 min	W
$V_{CE} = 28\text{ V}, P_{ie} = 0.1\text{ W}, f = 150\text{ MHz}$	P_{oe}	0.4 min	W



TRANSISTOR

2N3119

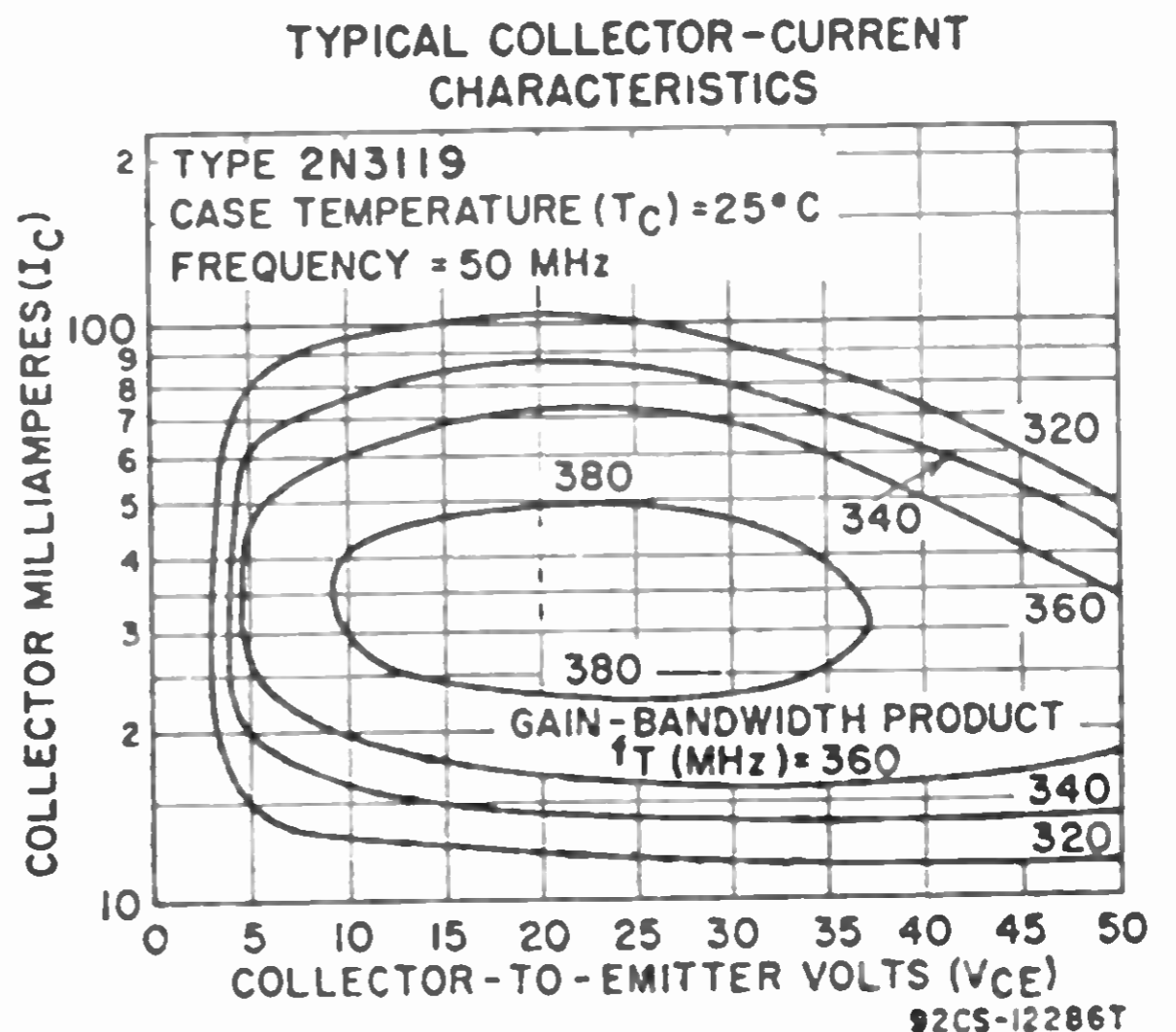
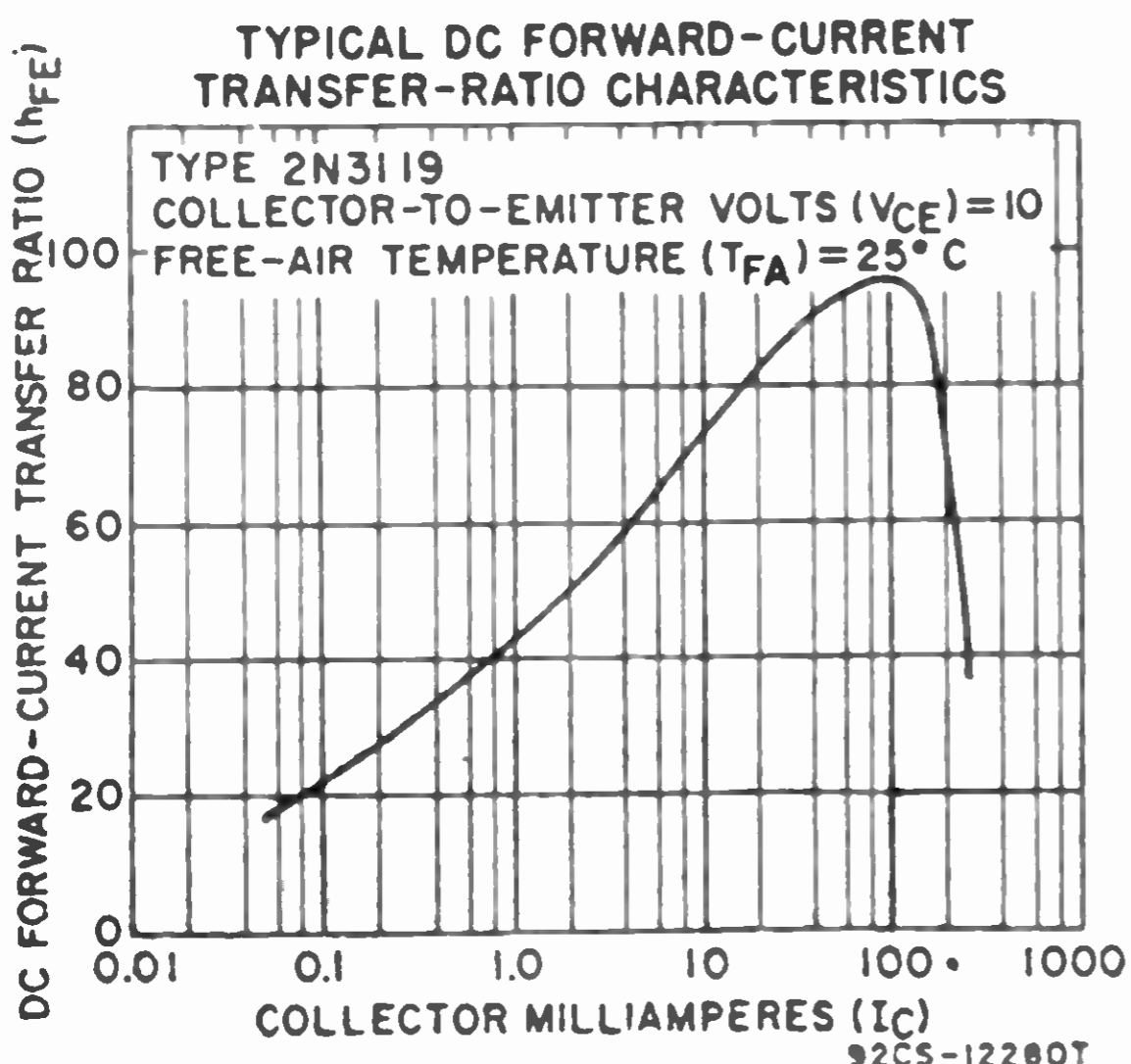
Si n-p-n triple-diffused planar type used in high-voltage, high-frequency pulse-amplifier and high-voltage saturated-switching applications in industrial and military equipment. JEDEC TO-5, Outline No.5.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	100	V
Collector-to-Emitter Voltage:			
$V_{BE} = -1.5\text{ V}$	V_{CEV}	100	V
Base open	V_{CEO}	80	V
Emitter-to-Base Voltage	V_{EBO}	4	V
Collector Current	I_C	0.5	A
Transistor Dissipation:			
T_A up to 25°C	P_T	1	W
T_C up to 25°C	P_T	4	W
T_A or T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	$^\circ\text{C}$
Storage	T_{STG}	-65 to 200	$^\circ\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	255	$^\circ\text{C}$

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Base Breakdown Voltage ($I_C = 0.1\text{ mA}, I_E = 0$)	$V_{(BR)CBO}$	100 min	V
Collector-to-Emitter Breakdown Voltage:			
$V_{BE} = -1.5\text{ V}, I_C = 0.1\text{ mA}$	$V_{(BR)CEV}$	100 min	V
$I_C = 10\text{ mA}, I_B = 0, t_p = 300\text{ }\mu\text{s}, df = 1.8\%$	$V_{(BR)CEO}(\text{sus})$	80 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.1\text{ mA}, I_C = 0$)	$V_{(BR)EBO}$	4 min	V
Base-to-Emitter Saturation Voltage ($I_C = 100\text{ mA}, I_B = 10\text{ mA}$)	$V_{BE}(\text{sat})$	1.1 max	V
Collector-to-Emitter Saturation Voltage ($I_C = 100\text{ mA}, I_B = 10\text{ mA}$)	$V_{CE}(\text{sat})$	0.5 max	V
Collector-Cutoff Current:			
$V_{CB} = 60\text{ V}, I_E = 0, T_A = 25^\circ\text{C}$	I_{CBO}	50 max	nA
$V_{CB} = 60\text{ V}, I_E = 0, T_A = 150^\circ\text{C}$	I_{CBO}	50 max	μA
Emitter-Cutoff Current ($V_{BE} = -3\text{ V}, I_C = 0, T_A = 25^\circ\text{C}$)	I_{EBO}	100 max	nA
Static Forward-Current Transfer Ratio ($V_{CE} = 10\text{ V}, I_C = 10\text{ mA}$)	h_{FE}	40 min	
Pulsed Static Forward-Current Transfer Ratio:			
$V_{CE} = 10\text{ V}, I_C = 100\text{ mA}, t_p = 300\text{ }\mu\text{s}, df = 1.8\%$..	$h_{FE}(\text{pulsed})$	50 to 200	
$V_{CE} = 10\text{ V}, I_C = 250\text{ mA}, t_p = 300\text{ }\mu\text{s}, df = 1.8\%$..	$h_{FE}(\text{pulsed})$	20 min	



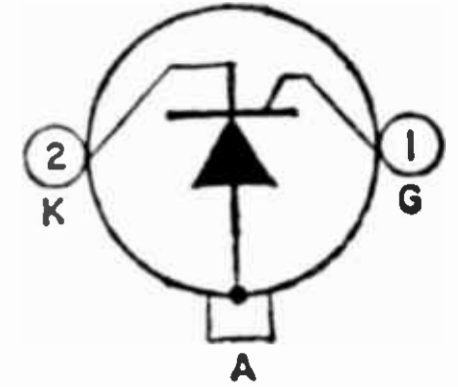
CHARACTERISTICS (cont'd)

Gain-Bandwidth Product ($V_{CE} = 28 \text{ V}$, $I_C = 25 \text{ mA}$, $f = 50 \text{ MHz}$)	f_T	250 min	MHz
Collector-to-Base Feedback Capacitance ($V_{CB} = 28 \text{ V}$, $I_C = 0$, $f = 1 \text{ MHz}$)	$C_{b'c}$	6 max	pF
Pulsed-Amplifier Rise Time ($V_{CC} = 80 \text{ V}$, $I_C = 10 \text{ mA}$)		20 max	ns
Saturated Switch Turn-On Time ($V_{CC} = 28 \text{ V}$, $I_C = 100 \text{ mA}$, $I_{B1} = 10 \text{ mA}$)	$t_d + t_r$	40 max	ns
Saturated Switch Turn-Off Time ($V_{CC} = 28 \text{ V}$, $I_C = 100 \text{ mA}$, $I_{B2} = -10 \text{ mA}$)	$t_s + t_r$	700 max	ns

2N3228

SILICON CONTROLLED RECTIFIER

Si all-diffused three-junction types for use in power-control and power-switching applications. JEDEC TO-66, Outline No.25. See Mounting Hardware for desired mounting arrangement.



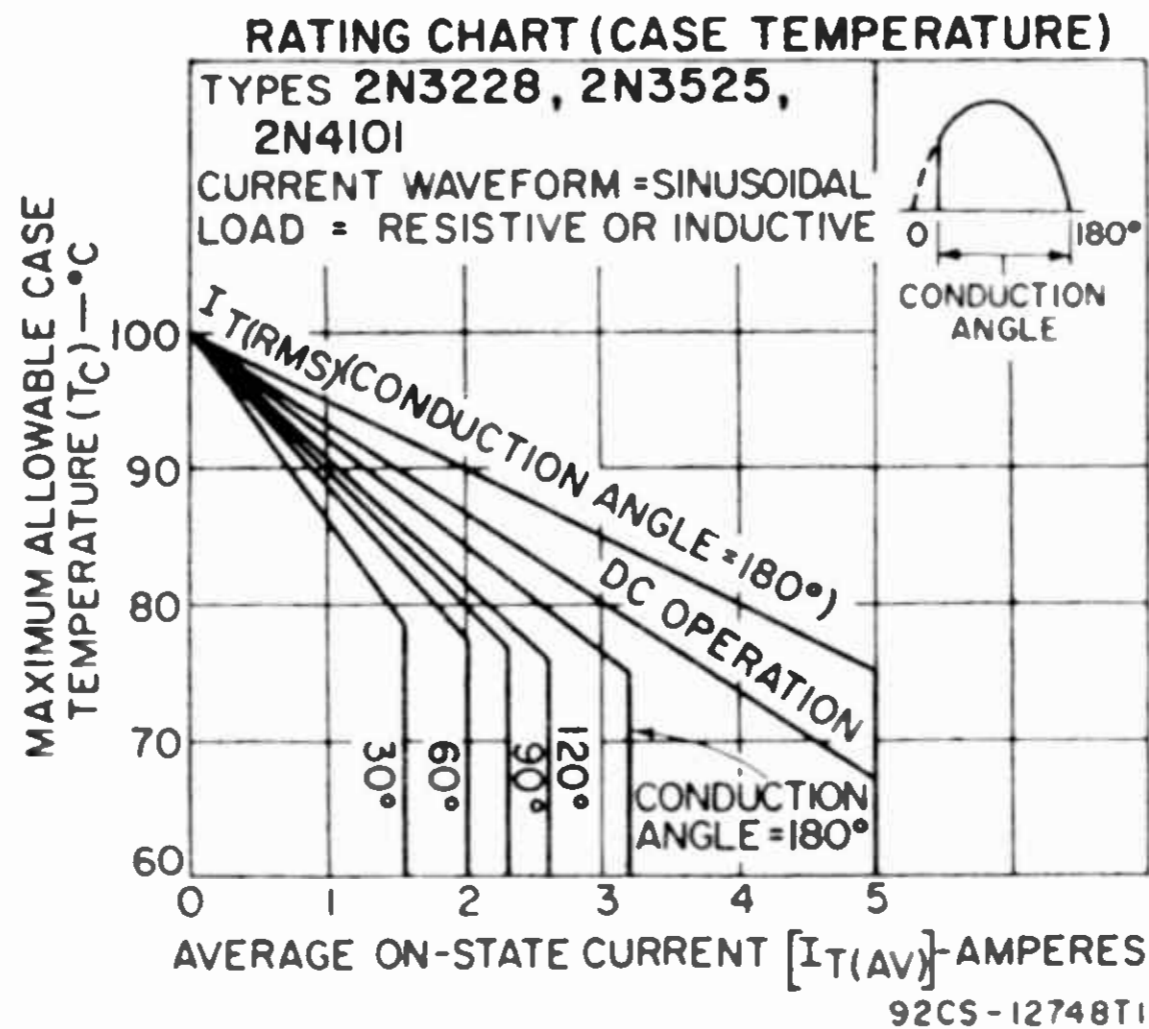
MAXIMUM RATINGS (For sinusoidal ac supply voltage at $f = 50$ to 400 Hz with resistive or inductive load)

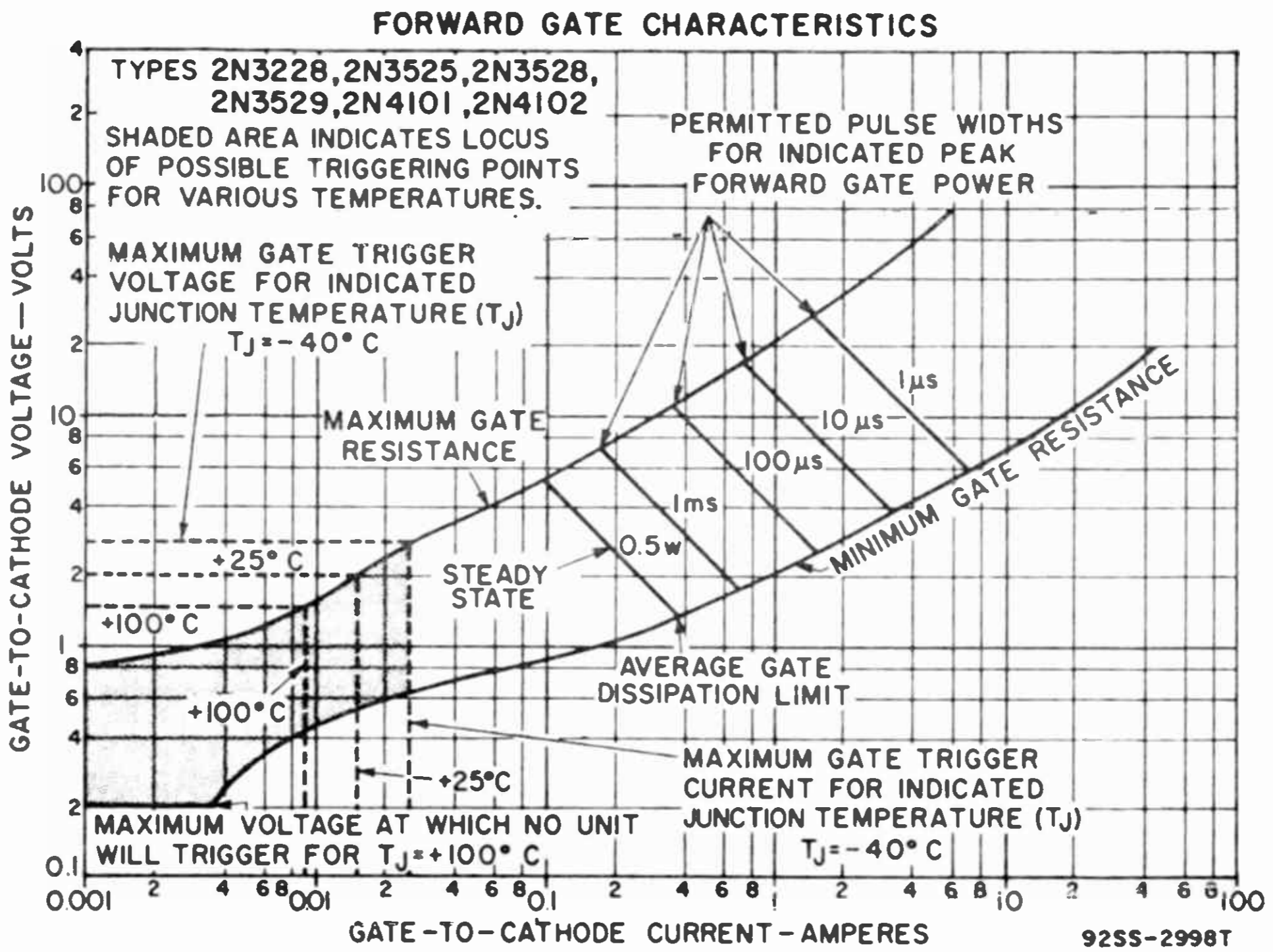
V_{RSOM}	330	V
V_{RROM}	200	V
V_{DROM}	600	V
$I_{T(AV)}$ (conduction angle = 180° , $T_c = 75^\circ\text{C}$)	3.2	A
$I_{T(RMS)}$	5	A
I_{TSM} (1 cycle of principal voltage)	60	A
$[I_{TSM(RMS)}]^2 t$ (1 to 8.3 ms)	15	A^2s
di_T/dt ($V_D = V_{F(BOD)}$, $I_{GT} = 200 \text{ mA}$, $t_r = 0.5 \mu\text{s}$)	200	$\text{A}/\mu\text{s}$
$P_{G(AV)}$	0.5	W
P_{GM} (peak, forward, or reverse for $10 \mu\text{s}$)	13	W
T_{STG}	-40 to 125	$^\circ\text{C}$
T_c	-40 to 125	$^\circ\text{C}$

CHARACTERISTICS (At maximum electrical ratings at $T_c = 25^\circ\text{C}$)

$V_{F(BOD)}$ ($T_c = 100^\circ\text{C}$)	200 min	V
I_{DOM} ($V_{DO} = V_{F(BOD)}$ min value, $T_c = 100^\circ\text{C}$)	0.1 typ; 1.5 max	mA
I_{RROM} ($V_{RO} = V_{RSOM}$, $T_c = 100^\circ\text{C}$)	0.05 typ; 0.75 max	mA
V_T (on-state current = 30 A)	2.15 typ; 2.8 max	V
I_{GT}	8 typ; 15 max	mA (dc)
V_{GT}	1.2 typ; 2 max	V (dc)
i_{HO}	10 typ; 20 max	mA
Critical dv/dt ($V_D = V_{F(BOD)}$ min value, exponential rise, $T_c = 100^\circ\text{C}$)	10 min; 200 typ	$\text{V}/\mu\text{s}$
t_{gt} ($V_D = V_{F(BOD)}$ min value, $i_T = 4.5$, $I_{GT} = 200 \text{ mA}$, $t_r = 0.1 \mu\text{s}$)	0.75 min; 1.5 typ	μs
t_{q1} ($i_T = 2 \text{ A}$, pulse width = $50 \mu\text{s}$, $dv_D/dt = 20 \text{ V}/\mu\text{s}$, $di_T/dt = 30 \text{ A}/\mu\text{s}$, $I_{GT} = 200 \text{ mA}$, $T_c = 75^\circ\text{C}$)	15 typ; 50 max	μs
θ_{J-C}^*	4 max	$^\circ\text{C}/\text{W}$

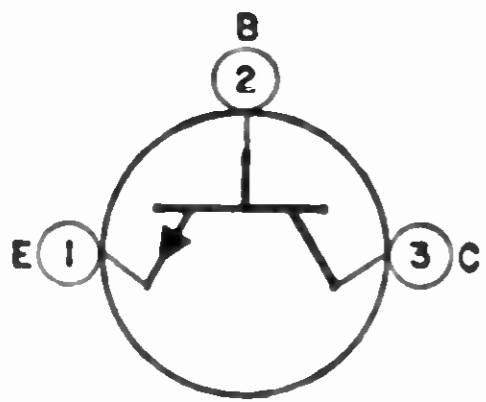
* This characteristic does not apply to types 2N3528, 2N3529, and 2N4102.





TRANSISTOR

2N3229



Si n-p-n triple-diffused planar type used in large-signal, high-power AM, FM, and cw applications at vhf frequencies in industrial and military, communications equipment. JEDEC TO-60, Outline No.23. See Mounting Hardware for desired mounting arrangement.

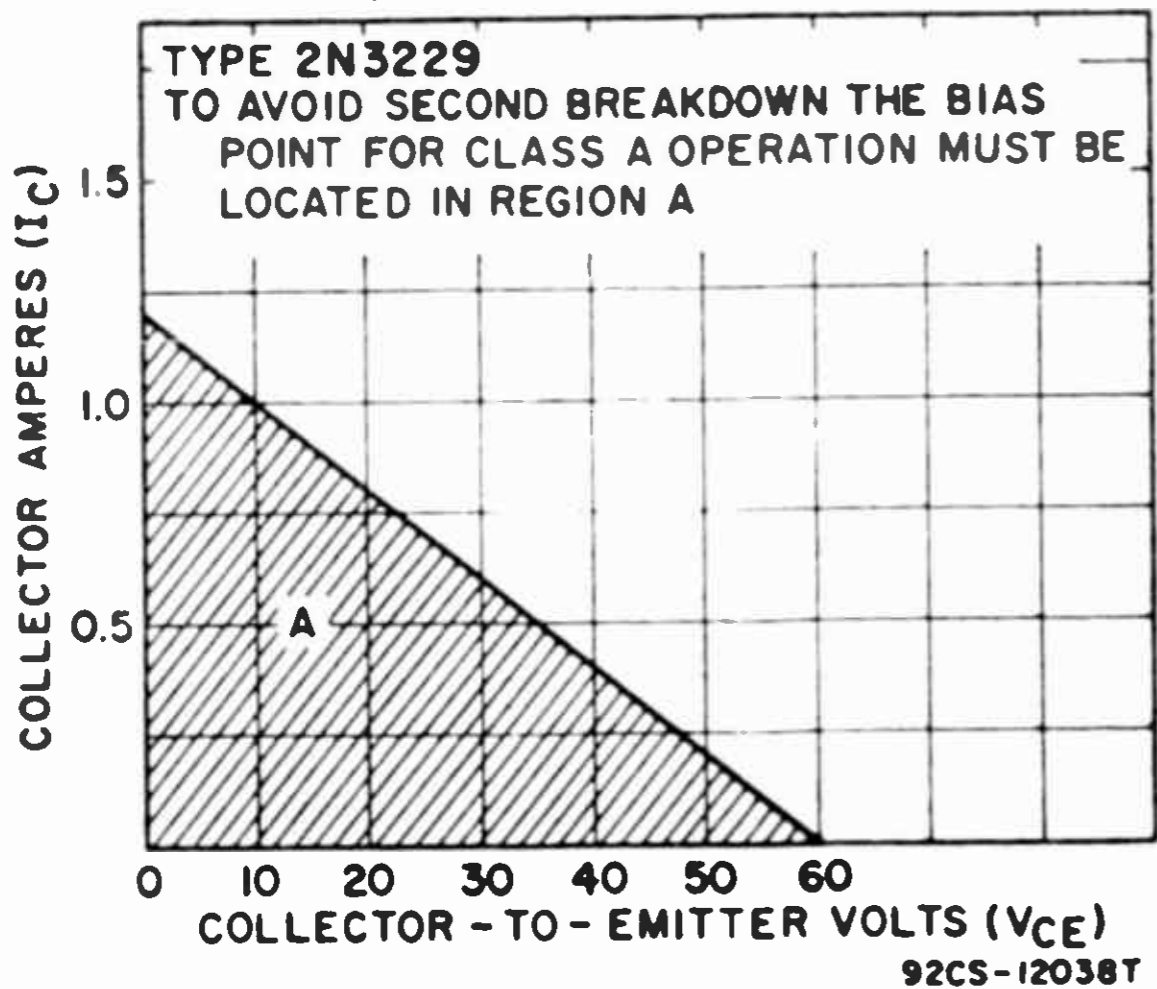
MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	105	V
Collector-to-Emitter Voltage:			
$V_{BE} = -1.5$ V	V_{CEV}	105	V
Base open	V_{CEO}	60	V
Emitter-to-Base Voltage	V_{EBO}	4	V
Collector Current	I_C	2.5	A
Transistor Dissipation:			
T_c up to 25°C	P_T	17.5	W
T_c above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	230	°C

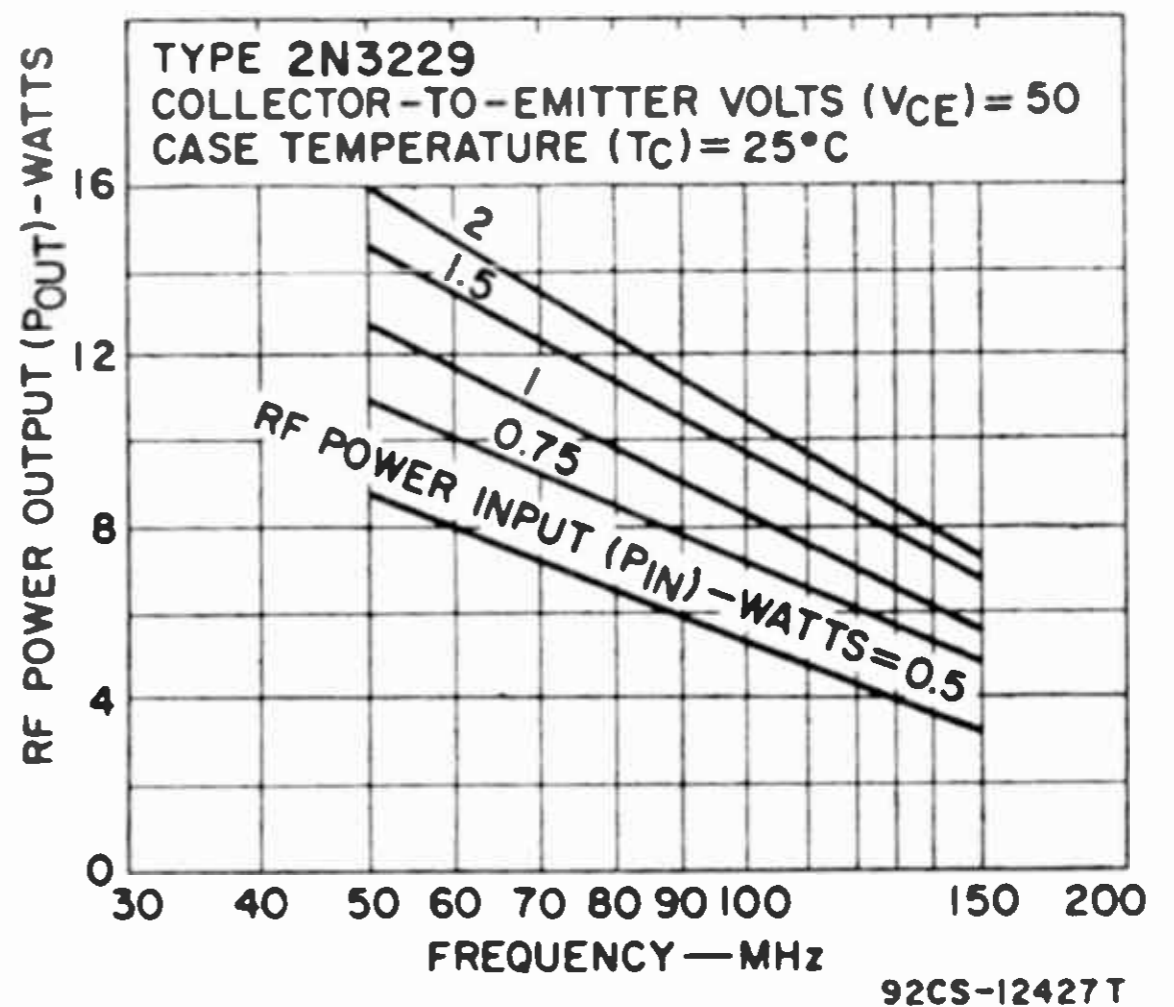
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Base Breakdown Voltage ($I_C = 0.5$ mA, $I_E = 0$)	$V_{(BR)CBO}$	105 min	V
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SAFE OPERATING REGION



TYPICAL OPERATION CHARACTERISTICS



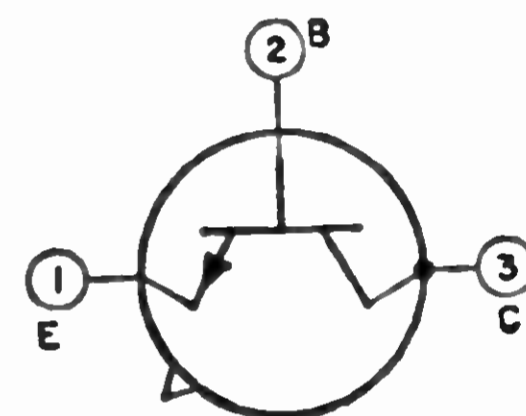
CHARACTERISTICS (cont'd)

Collector-to-Emitter Breakdown Voltage: $V_{BE} = -1.5 \text{ V}, I_C = 0.1 \text{ mA}$	$V_{(BR)CEV}$	105 min	V
$I_C = 500 \text{ mA}, I_B = 0, t_p \leq 5 \mu\text{s}, df \leq 1\%$	$V_{(BR)CEO(sus)}$	60 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.1 \text{ mA}, I_C = 0$)	$V_{(BR)EBO}$	4 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 2.5 \text{ A}, I_B = 500 \text{ mA}$)	$V_{CE(sat)}$	1 max	V
Collector-Cutoff Current ($V_{CB} = 30 \text{ V}, I_E = 0$)	I_{CBO}	0.1 max	μA
Intrinsic Base-Spreading Resistance ($V_{CE} = 28 \text{ V}, I_C = 250 \text{ mA}, f = 400 \text{ MHz}$)	$r_{bb'}$	6	Ω
Gain-Bandwidth Product ($V_{CE} = 28 \text{ V}, I_C = 250 \text{ mA}$)	f_T	200	MHz
Collector-to-Base Feedback Capacitance ($V_{CB} = 30 \text{ V}, I_E = 0, f = 140 \text{ kHz}$)	C_{obo}	20 max	pF
Collector-to-Case Capacitance	C_c	6 max	pF
RF Power Output, Unneutralized: $V_{CC} = 50 \text{ V}, I_C = 500 \text{ mA}, P_{IE} = 2 \text{ W}, f = 50 \text{ MHz}$	P_{OE}	15 min	W
$V_{CC} = 50 \text{ V}, I_C = 250 \text{ mA}, P_{IE} = 1 \text{ W}, f = 150 \text{ MHz}$	P_{OIE}	5 min	W

- 2N3230** Refer to Chart of Discontinued Transistors
- 2N3231** Refer to Chart of Discontinued Transistors
- 2N3241** Refer to Chart of Discontinued Transistors

2N3241A TRANSISTOR

Si n-p-n epitaxial planar type used in high-voltage, high-current audio and video amplifier and switching service in commercial, industrial, and computer equipment. JEDEC TO-104, Outline No.32.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	30	V
Collector-to-Emitter Voltage: $V_{BE} = -1 \text{ V}$	V_{CEV}	25	V
Base open	V_{CEO}	25	V
Emitter-to-Base Voltage	V_{EBO}	7.5	V
Collector Current	I_C	Limited by dissipation	
Transistor Dissipation: T_c up to 75°C	P_T	2	W
T_c above 75°C	P_T	See curve page 300	
T_A up to 25°C	P_T	0.5	W
T_A above 25°C	P_T	See curve page 300	
Temperature Range: Operating (Junction)	T_J (opr)	-65 to 175	$^\circ\text{C}$
Storage	T_{STG}	-65 to 175	$^\circ\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	265	$^\circ\text{C}$

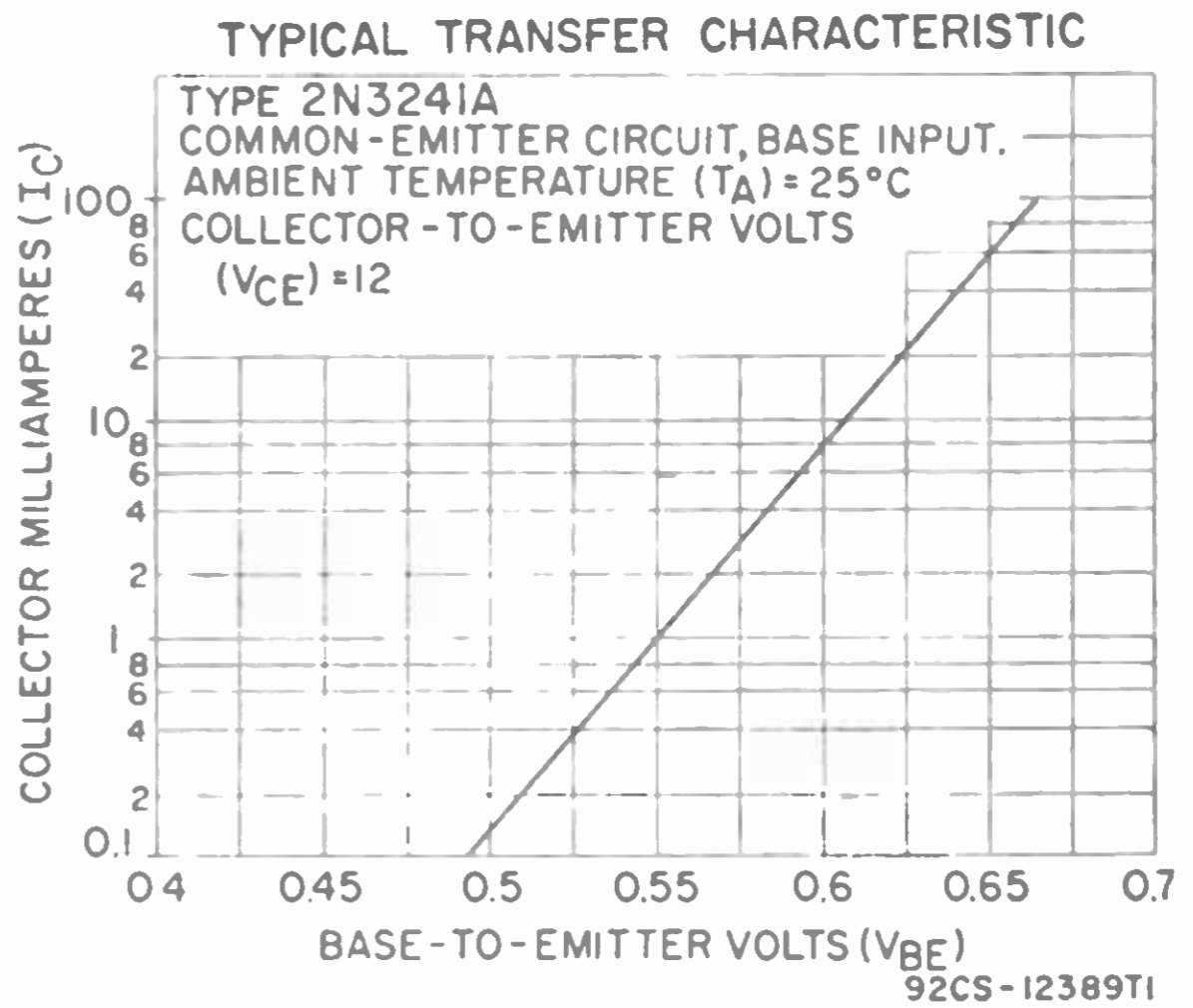
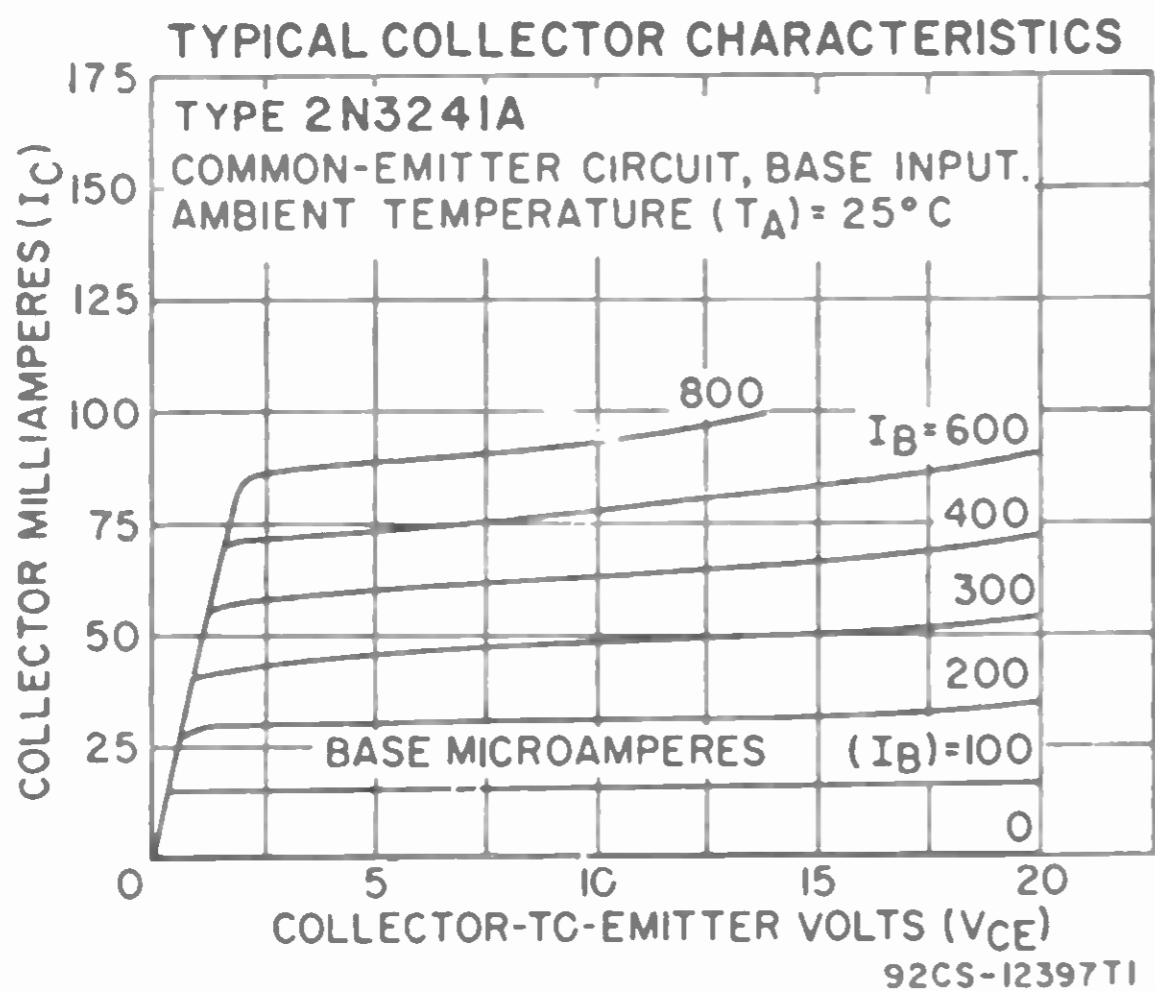
CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = 0.05 \text{ mA}, I_E = 0$)	$V_{(BR)CBO}$	30 min	V
Collector-to-Emitter Breakdown Voltage: $I_C = 10 \text{ mA}, I_B = 0$	$V_{(BR)CBO}$	25 min	V
$V_{BE} = -1 \text{ V}, I_C = 0.01 \text{ mA}$	$V_{(BR)CEV}$	25 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.05 \text{ mA}, I_C = 0$)	$V_{(BR)EBO}$	7.5 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 200 \text{ mA}, I_B = 10 \text{ mA}$)	$V_{CE(sat)}$	0.22 typ; 0.25 max	V
Base-to-Emitter Saturation Voltage ($I_C = 200 \text{ mA}, I_B = 10 \text{ mA}$)	$V_{BE(sat)}$	0.88 typ; 1.25 max	V
Collector-Cutoff Current: $V_{CB} = 25 \text{ V}, I_E = 0$	I_{CBO}	100 max	nA
$V_{CB} = 25 \text{ V}, I_E = 0, T_A = 150^\circ\text{C}$	I_{CBO}	10 max	μA
Emitter-Cutoff Current ($V_{BE} = 2.5 \text{ V}, I_C = 0$)	I_{EBO}	100 max	nA
Static Forward-Current Transfer Ratio ($V_{CE} = 10 \text{ V}, I_C = 10 \text{ mA}$)	h_{FE}	100 to 200	
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 12 \text{ V}, I_C = 10 \text{ mA}, f = 1 \text{ kHz}$)	h_{fe}	100 to 250	
Magnitude of Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 12 \text{ V}, I_C = 1 \text{ mA}, f = 100 \text{ MHz}$)	$ h_{fe} $	0.5 min; 1 typ	
Gain-Bandwidth Product ($V_{CE} = 10 \text{ V}, I_C = 10 \text{ mA}, f = 50 \text{ MHz}$)	f_T	175	MHz

CHARACTERISTICS (cont'd)

Collector-to-Base Feedback Capacitance* ($V_{CB} = 6 \text{ V}$, $I_E = 0$, $f = 1 \text{ MHz}$)	C_{cb}	20 max	pF
Intrinsic Base-Spreading Resistance ($V_{CE} = 6 \text{ V}$, $I_C = 1 \text{ mA}$, $f = 100 \text{ MHz}$)	$r_{bb'}$	20	Ω
Noise Figure: $V_{CE} = 6 \text{ V}$, $I_C = 0.1 \text{ mA}$, $f = 10 \text{ kHz}$, $R_G = 1000 \Omega$, circuit bandwidth = 1 Hz	NF	2.5	dB
$V_{CE} = 6 \text{ V}$, $I_C = 0.5 \text{ mA}$, $f = 1 \text{ kHz}$, $R_G = 1000 \Omega$, circuit bandwidth = 1 Hz	NF	8 typ; 10 max	dB
Small-Signal Input Impedance ($V_{CE} = 12 \text{ V}$, $I_C = 10 \text{ mA}$, $f = 1 \text{ kHz}$)	h_{ie}	200 to 1000	Ω
Small-Signal Output Admittance ($V_{CE} = 12 \text{ V}$, $I_C = 10 \text{ mA}$, $f = 1 \text{ kHz}$)	h_{oe}	30 to 350	μmhos
Thermal Resistance, Junction-to-Case	θ_{J-C}	50 max	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	300 max	$^{\circ}\text{C/W}$

* Emitter terminal guarded.

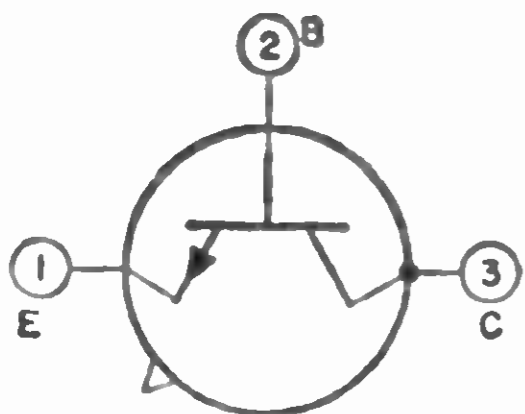


Refer to Chart of Discontinued Transistors

2N3242

TRANSISTOR

2N3242A



Si n-p-n epitaxial planar type used in high-voltage, high-current audio and video amplifier and switching service in commercial, industrial, and computer equipment. JEDEC TO-104, Outline No.32. For collector-characteristics and transfer-characteristics curves, refer to type 2N3241A.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	40	V
Collector-to-Emitter Voltage: $V_{BE} = -1 \text{ V}$ Base open	V_{CEV} V_{CEO}	40 40	V V
Emitter-to-Base Voltage	V_{EBO}	8	V
Collector Current	I_C	Limited by dissipation	
Transistor Dissipation: Tc up to 75°C Tc above 75°C T _A up to 25°C T _A above 25°C	P_T P_T P_T P_T	2 See curve page 300 0.5 See curve page 300	W W W W
Temperature Range: Operating (Junction) Storage	T_J (opr) T_{STG}	-65 to 175 -65 to 175	$^{\circ}\text{C}$ $^{\circ}\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	265	$^{\circ}\text{C}$

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = 0.1 \text{ mA}$, $I_E = 0$)	$V_{(BR)CBO}$	40 min	V
Collector-to-Emitter Breakdown Voltage: $I_C = 10 \text{ mA}$, $I_B = 0$ $V_{BE} = -1 \text{ V}$, $I_C = 0.01 \text{ mA}$	$V_{(BR)CEO}$ $V_{(BR)CEV}$	40 min 40 min	V V
Emitter-to-Base Breakdown Voltage ($I_E = 0.05 \text{ mA}$, $I_C = 0$)	$V_{(BR)EBO}$	8 min	V

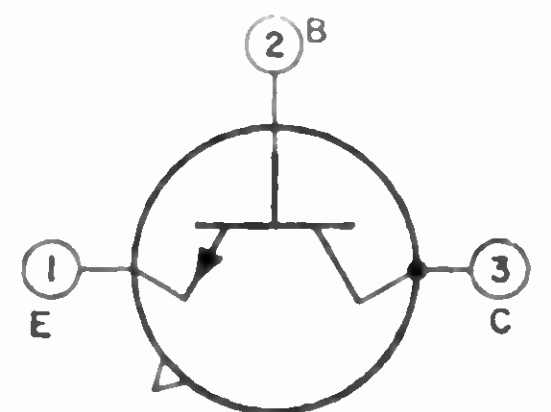
CHARACTERISTICS (cont'd)

Collector-to-Emitter Saturation Voltage ($I_C = 300 \text{ mA}$, $I_B = 15 \text{ mA}$)	$V_{CE(sat)}$	0.24 typ; 0.3 max	V
Base-to-Emitter Saturation Voltage ($I_C = 300 \text{ mA}$, $I_B = 15 \text{ mA}$)	$V_{BE(sat)}$	0.93 typ; 1.5 max	V
Collector-Cutoff Current:			
$V_{CB} = 25 \text{ V}$, $I_E = 0$	I_{CBO}	10 max	nA
$V_{CB} = 25 \text{ V}$, $I_E = 0$, $T_A = 150^\circ\text{C}$	I_{CBO}	1 max	μA
Emitter-Cutoff Current ($V_{BE} = 2.5 \text{ V}$, $I_C = 0$)	I_{EBO}	10 max	nA
Static Forward-Current Transfer Ratio ($V_{CE} = 10 \text{ V}$, $I_C = 10 \text{ mA}$)	h_{FE}	125 to 300	
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 12 \text{ V}$, $I_C = 10 \text{ mA}$, $f = 1 \text{ kHz}$)	h_{fe}	125 to 375	
Magnitude of Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 6 \text{ V}$, $I_C = 1 \text{ mA}$, $f = 100 \text{ MHz}$)	$ h_{fe} $	0.5 min; 1 typ	
Gain-Bandwidth Product ($V_{CE} = 10 \text{ V}$, $I_C = 10 \text{ mA}$, $f = 50 \text{ MHz}$)	f_t	175	MHz
Collector-to-Base Feedback Capacitance* ($V_{CB} = 6 \text{ V}$, $I_E = 0$, $f = 1 \text{ MHz}$)	C_{cb}	20 max	pF
Intrinsic Base-Spreading Resistance ($V_{CE} = 6 \text{ V}$, $I_C = 1 \text{ mA}$, $f = 100 \text{ MHz}$)	$r_{bb'}$	20	Ω
Noise Figure:			
$V_{CE} = 6 \text{ V}$, $I_C = 0.1 \text{ mA}$, $f = 10 \text{ kHz}$, $R_G = 1000 \Omega$, circuit bandwidth = 1 Hz	NF	2	dB
$V_{CE} = 6 \text{ V}$, $I_C = 0.5 \text{ mA}$, $f = 1 \text{ kHz}$, $R_G = 1000 \Omega$, circuit bandwidth = 1 Hz	NF	4 typ; 6 max	dB
Small-Signal Input Impedance ($V_{CE} = 12 \text{ V}$, $I_C = 10 \text{ mA}$, $f = 1 \text{ kHz}$)	h_{ie}	250 to 1500	Ω
Small-Signal Output Admittance ($V_{CE} = 12 \text{ V}$, $I_C = 10 \text{ mA}$, $f = 1 \text{ kHz}$)	h_{oe}	30 to 350	μmhos
Thermal Resistance, Junction-to-Case	θ_{J-C}	50 max	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	300 max	$^\circ\text{C}/\text{W}$

* Emitter terminal guarded.

2N3261 COMPUTER TRANSISTOR

Si n-p-n epitaxial planar type used in high-speed switching applications in military and commercial data-processing equipment such as digital-logic circuits, terminated-line-driver service, and as a high-speed-memory driver. JEDEC TO-52, Outline No.21.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	40	V
Collector-to-Emitter Voltage	V_{CEO}	15	V
Emitter-to-Base Voltage	V_{EBO}	6	V
Collector Current	I_C	500	mA
Transistor Dissipation:			
T_A up to 25°C	P_T	0.3	W
T_C up to 25°C	P_T	1	W
T_A or T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (T_A - T_C)	T_{STG}	-65 to 175	$^\circ\text{C}$
Storage	T_L	-65 to 200	$^\circ\text{C}$
Lead-Soldering Temperature (10 s max)		230	$^\circ\text{C}$

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = 0.01 \text{ mA}$, $I_E = 0$)	$V_{(BR)CBO}$	40 min	V
Collector-to-Emitter Breakdown Voltage ($I_C = 10 \text{ mA}$, $I_B = 0$, $t_p = 100 \mu\text{s}$, $df \leq 2\%$)	$V_{(BR)CEO}$	15 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.01 \text{ mA}$, $I_C = 0$)	$V_{(BR)EBO}$	6 min	V
Base-to-Emitter Saturation Voltage ($I_C = 100 \text{ mA}$, $I_B = 10 \text{ mA}$)	$V_{BE(sat)}$	0.8 to 1.1	V
Collector-to-Emitter Saturation Voltage ($I_C = 100 \text{ mA}$, $I_B = 10 \text{ mA}$, $t_p = 100 \mu\text{s}$, $df \leq 2\%$)	$V_{CE(sat)}$	0.35 max	V
Base-Cutoff Current ($V_{CE} = 15 \text{ V}$, $V_{BE} = 0$)	I_{BEV}	-25 max	nA
Collector-Cutoff Current:			
$V_{CE} = 15 \text{ V}$, $V_{EB} = 0$, $T_A = 15^\circ\text{C}$	I_{CEV}	25 max	nA
$V_{CE} = 15 \text{ V}$, $V_{EB} = 0$, $T_A = 150^\circ\text{C}$	I_{CEV}	25 max	μA
Static Forward-Current Transfer Ratio:			
$V_{CE} = 1 \text{ V}$, $I_C = 10 \text{ mA}$, $T_A = 25^\circ\text{C}$	h_{FE}	40 to 150	
$V_{CE} = 1 \text{ V}$, $I_C = 10 \text{ mA}$, $T_A = -55^\circ\text{C}$	h_{FE}	20 min	

CHARACTERISTICS (cont'd)

Pulsed Static Forward-Current Transfer Ratio:

$V_{CE} = 1\text{ V}$, $I_C = 100\text{ mA}$, $t_p = 300\ \mu\text{s}$, $df \leq 2\%$...
 $V_{CE} = 1\text{ V}$, $I_C = 200\text{ mA}$, $t_p = 300\ \mu\text{s}$, $df \leq 2\%$...

$h_{FE}(\text{pulsed})$ 30 min
 $h_{FE}(\text{pulsed})$ 20 min

Small-Signal Forward-Current Transfer Ratio:

$V_{CE} = 1\text{ V}$, $I_C = 100\text{ mA}$, $f = 100\text{ MHz}$
 $V_{CE} = 10\text{ V}$, $I_C = 10\text{ mA}$, $f = 100\text{ MHz}$

h_{fe} 3 min
 h_{fe} 6 min

Input Capacitance ($V_{EB} = 0.5\text{ V}$, $I_C = 0$, $f = 1\text{ MHz}$)

C_{ibo}

4 max pF

Output Capacitance ($V_{CB} = 5\text{ V}$, $I_E = 0$, $f = 1\text{ MHz}$)

C_{obo}

3.5 max pF

Delay Time ($V_{CC} = 6\text{ V}$, $V_{BE}(\text{off}) = -4\text{ V}$,

$I_{B1} = 10\text{ mA}$, $I_{CS} = 100\text{ mA}$, $I_{B2} = -10\text{ mA}$)

t_d

6 max ns

Rise Time ($V_{CC} = 6\text{ V}$, $V_{BE}(\text{off}) = -4\text{ V}$, $I_{B1} = 10\text{ mA}$,

$I_{CS} = 100\text{ mA}$, $I_{B2} = -10\text{ mA}$)

t_r

7 max ns

Fall Time ($V_{CC} = 6\text{ V}$, $I_{B1} = 10\text{ mA}$,

$I_{CS} = 100\text{ mA}$, $I_{B2} = -10\text{ mA}$)

t_f

6 max ns

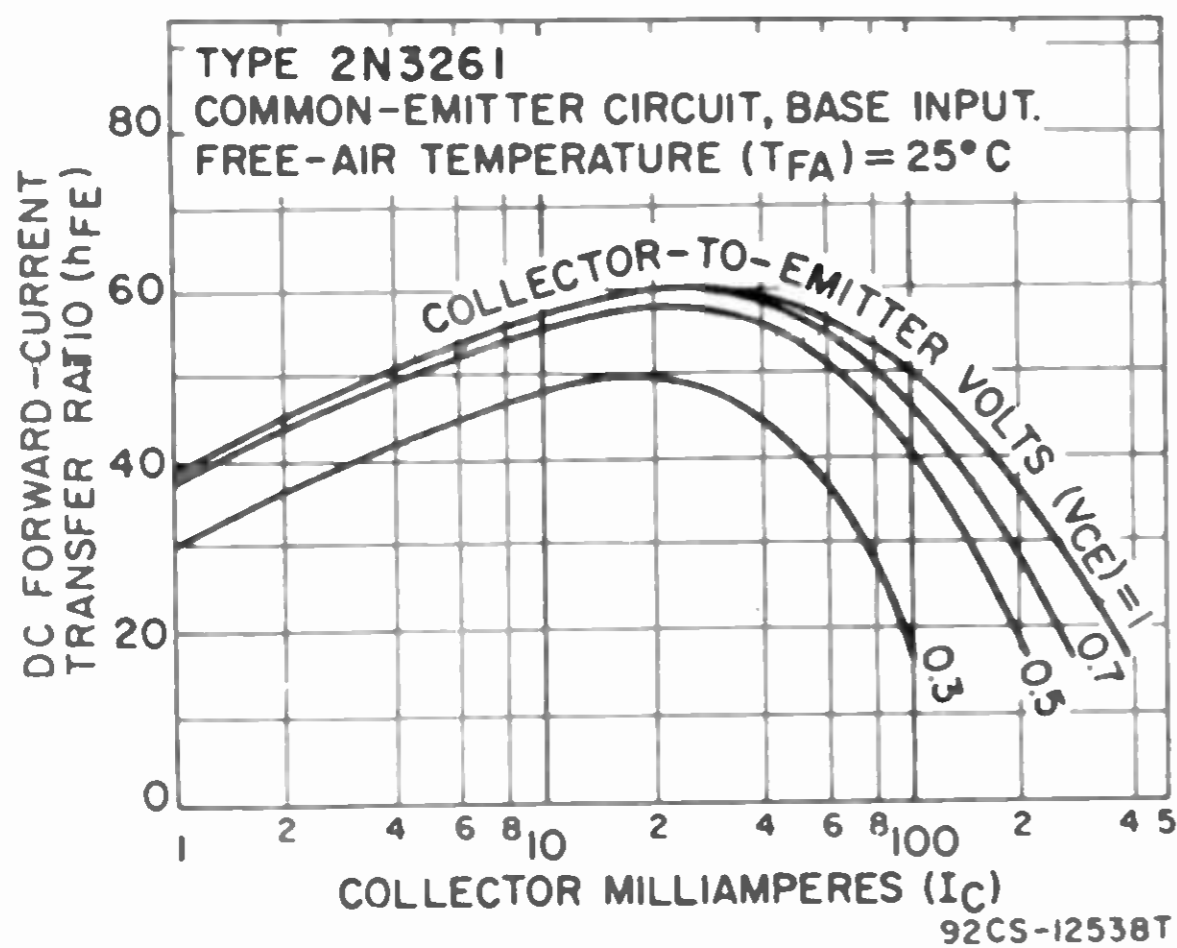
Storage Time ($V_{CC} = 6\text{ V}$, $I_{B1} = 10\text{ mA}$,

$I_{CS} = 100\text{ mA}$, $I_{B2} = -10\text{ mA}$)

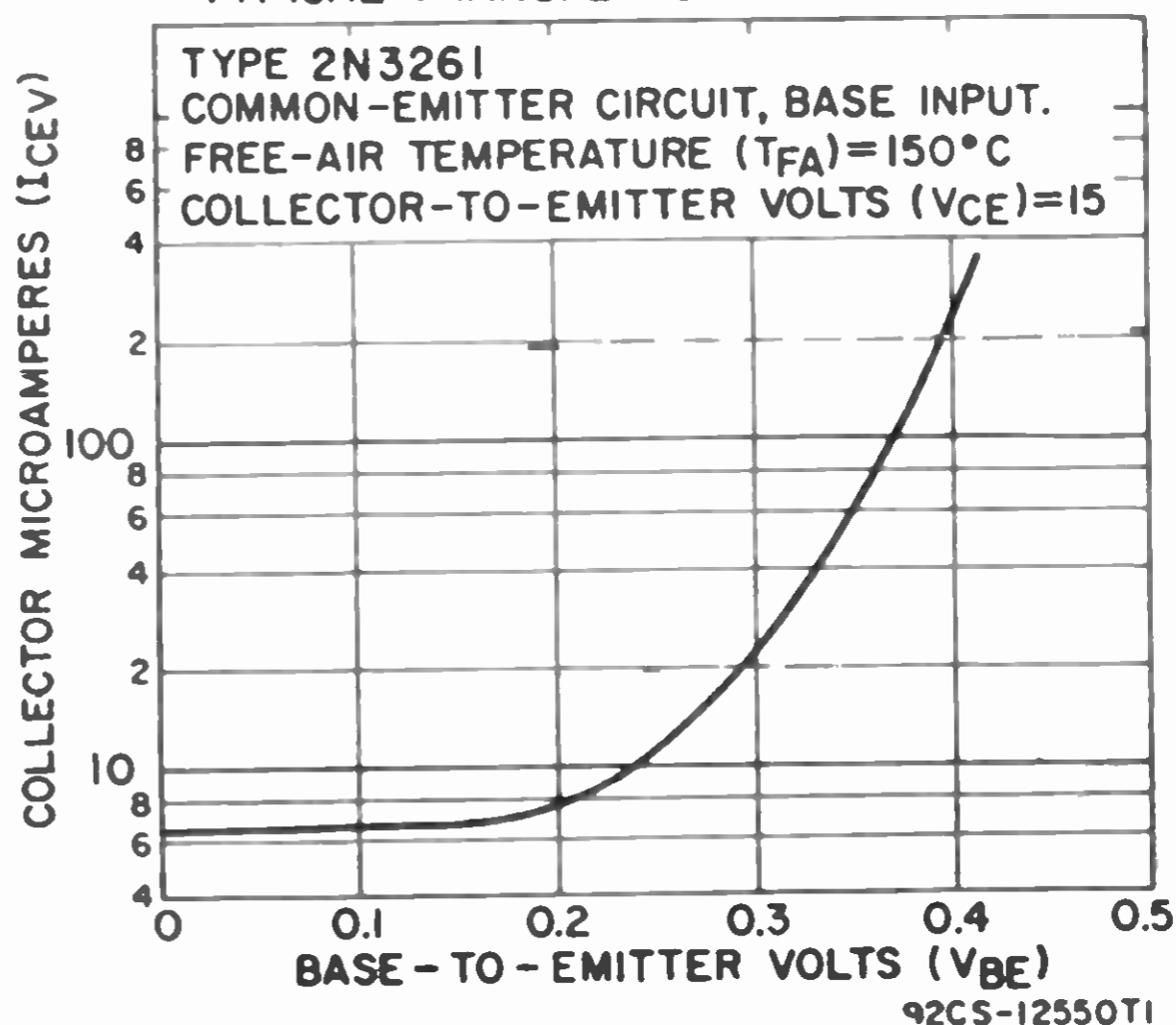
t_s

10 max ns

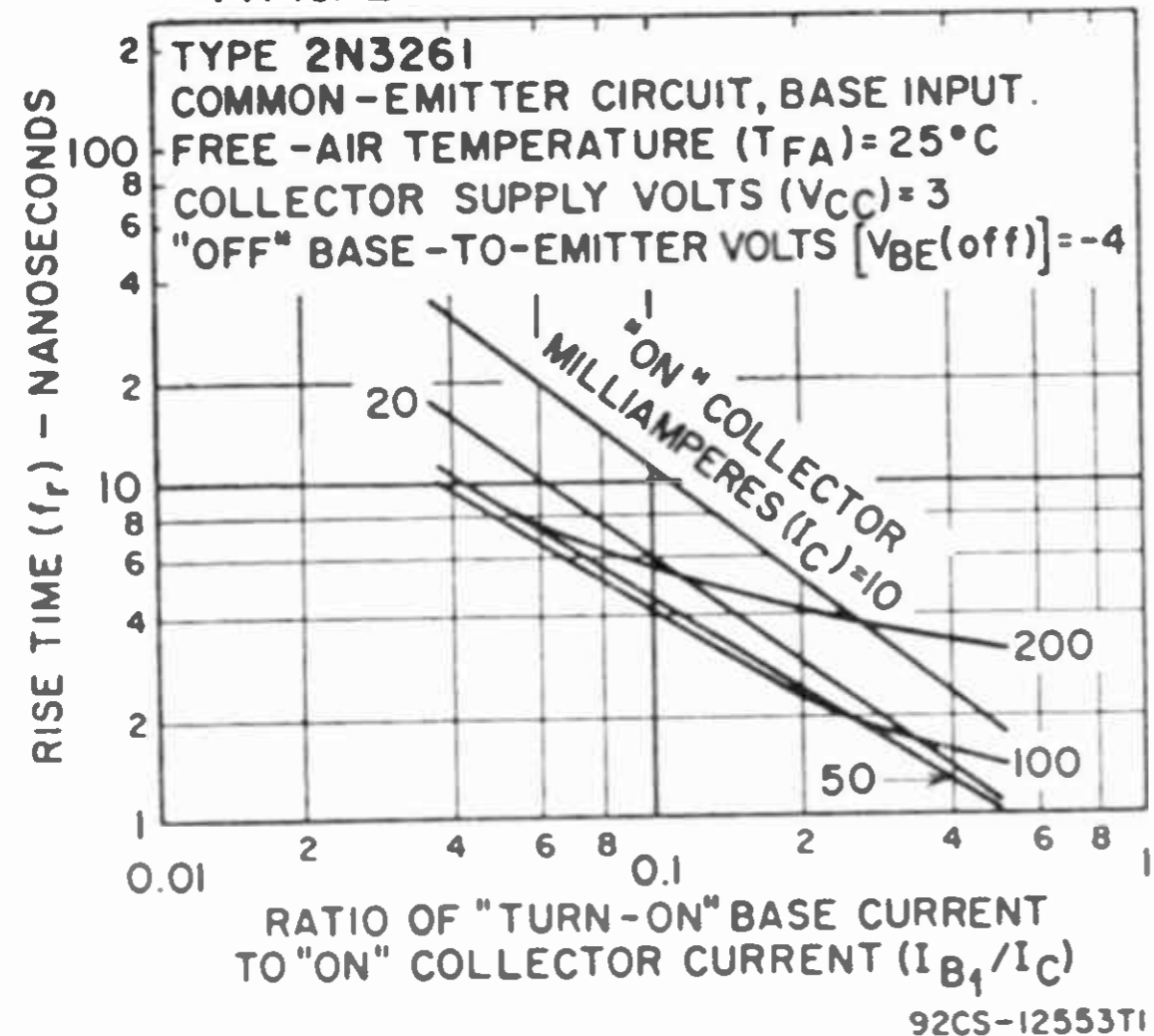
TYPICAL DC FORWARD-CURRENT TRANSFER-RATIO CHARACTERISTICS



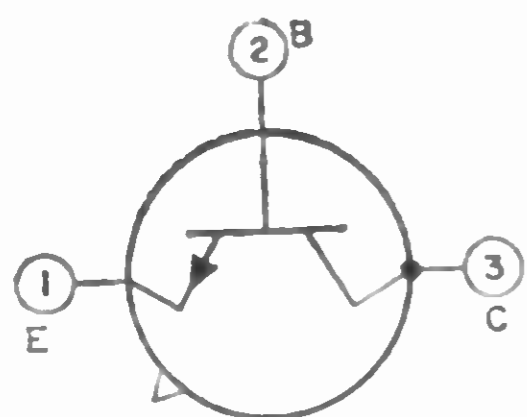
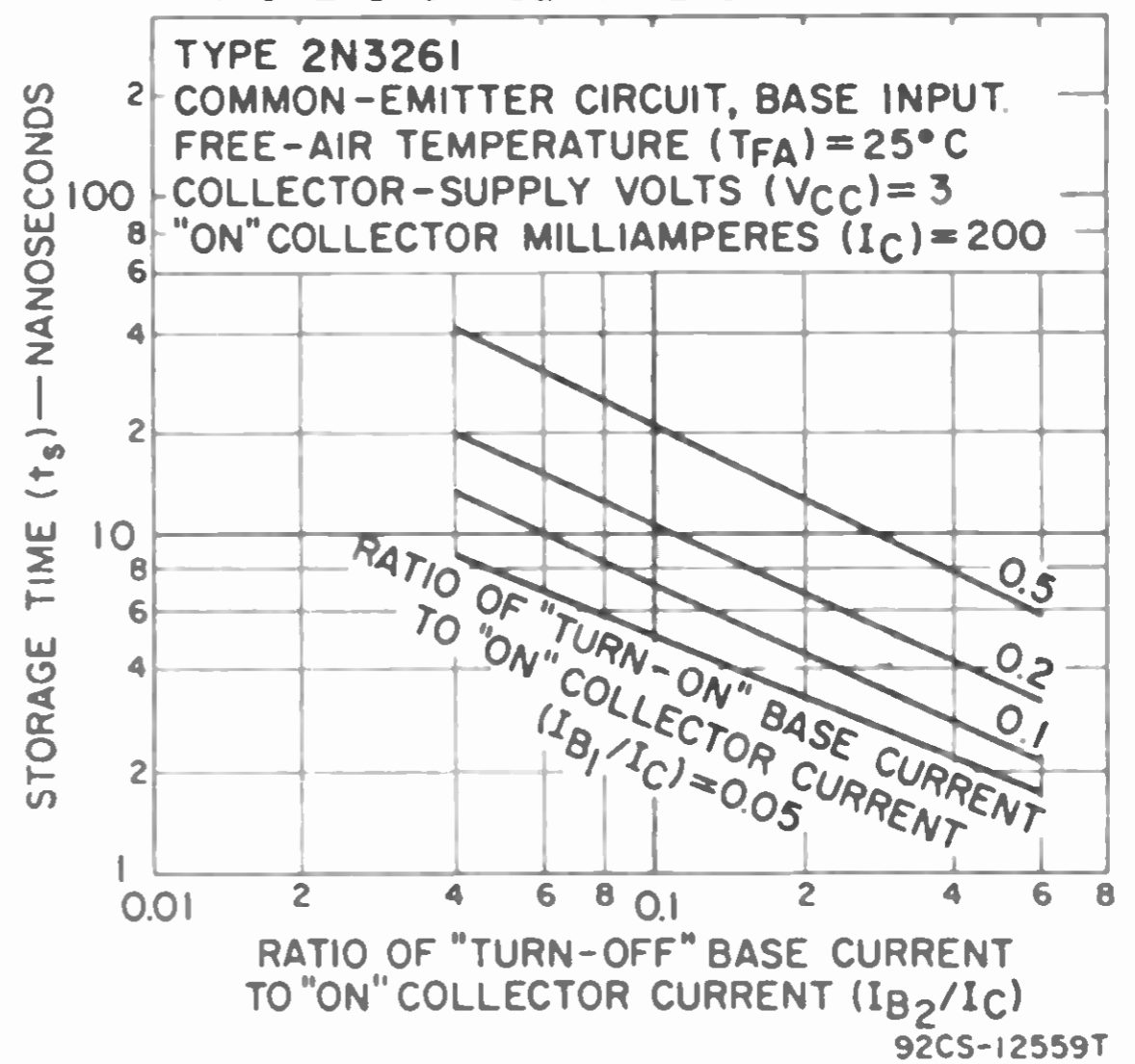
TYPICAL TRANSFER CHARACTERISTICS



TYPICAL RISE-TIME CHARACTERISTICS



TYPICAL STORAGE-TIME CHARACTERISTICS



TRANSISTOR

2N3262

Si n-p-n triple-diffused planar type used in high-voltage, high-frequency pulse-amplifier and high-voltage saturated-switching applications in industrial and military equipment. JEDEC TO-39, Outline No.15.

MAXIMUM RATINGS

Collector-to-Base Voltage
 Collector-to-Emitter Voltage:
 $V_{BE} = -1.5\text{ V}$
 Base open (sustaining voltage)

V_{CBO} 100 V
 V_{CEV} 100 V
 $V_{CEO}(\text{sus})$ 80 V

MAXIMUM RATINGS (cont'd)

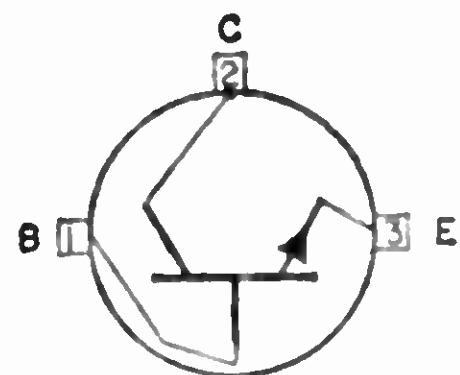
Emitter-to-Base Voltage	V_{EBO}	4	V
Collector Current	I_C	1.5	A
Transistor Dissipation:			
T_A up to 25°C	P_T	1	W
T_C up to 25°C	P_T	8.75	W
T_A or T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (T_A - T_C) and Storage (T_{STG})		-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	230	°C

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Breakdown Voltage ($V_{BE} = -1.5$ V, $I_C = 0.25$ mA)	$V_{(BR)CEV}$	100 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.1$ mA, $I_C = 0$)	$V_{(BR)EBO}$	4 min	V
Collector-to-Emitter Sustaining Voltage:			
$I_C = 500$ mA, $R_{BE} = 10 \Omega$, $t_p = 15 \mu s$, $df = 1.5\%$	$V_{CE(sus)}$	90 min	V
$I_C = 500$ mA, $I_B = 0$, $t_p = 15 \mu s$, $df = 1.5\%$	$V_{CE0(sus)}$	80 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 1$ A, $I_B = 100$ mA)	$V_{CE(sat)}$	0.6 max	V
Base-to-Emitter Saturation Voltage ($I_C = 1$ A, $I_B = 100$ mA)	$V_{BE(sat)}$	1.4 max	V
Collector-Cutoff Current ($V_{CB} = 30$ V, $I_E = 0$, $T_A = 25^\circ C$)	I_{CBO}	0.1 max	μA
Emitter-Cutoff Current ($V_{EB} = 3$ V, $I_C = 0$)	I_{EBO}	100 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 4$ V, $I_C = 500$ mA)	h_{FE}	40 min	
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 28$ V, $I_C = 100$ mA, $f = 50$ MHz)	h_{fe}	3 min	
Collector-to-Base Feedback Capacitance ($V_{CB} = 28$ V, $I_C = 0$, $f = 1$ MHz)	$C_{b'c}$	20 max	pF
Pulse-Amplifier Rise Time ($V_{CC} = 80$ V, $I_C = 25$ mA)	t_r	20 max	ns
Turn-On Time, Saturated Switch ($V_{CE} = 28$ V, $I_C = 1$ A, $I_{B1} = 100$ mA, $I_{B2} = -100$ mA)	$t_d + t_r$	40 max	ns
Turn-On Time, Saturated Swith ($V_{CE} = 28$ V, $I_C = 1$ A, $I_{B1} = 100$ mA, $I_{B2} = -100$ mA)	$t_s + t_r$	750 max	ns

2N3263 POWER TRANSISTOR

Si n-p-n epitaxial type used in high-power, high-speed, and high-current applications such as switching circuits, amplifiers, and power oscillators in aerospace, military, and industrial applications. Outline No.29.



MAXIMUM RATINGS

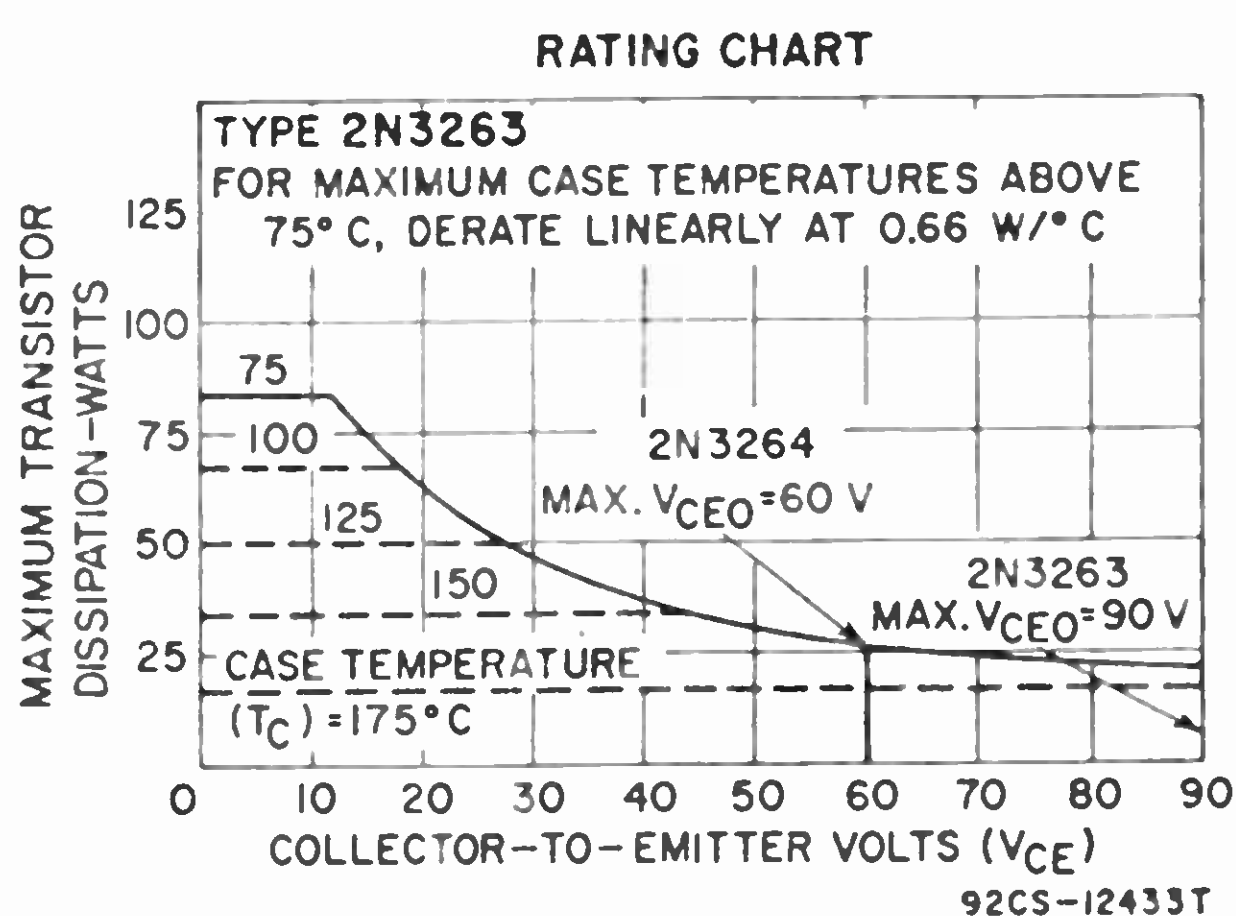
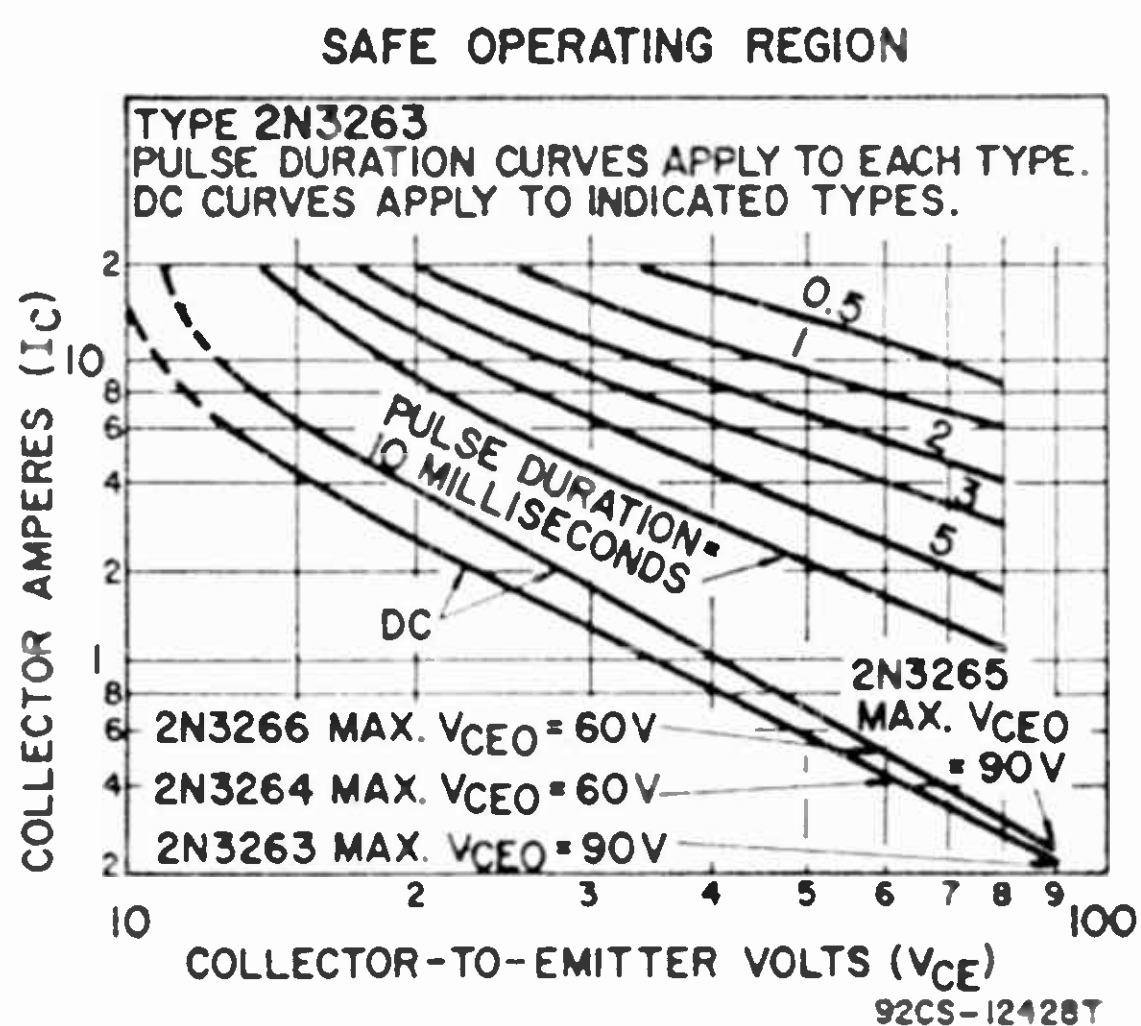
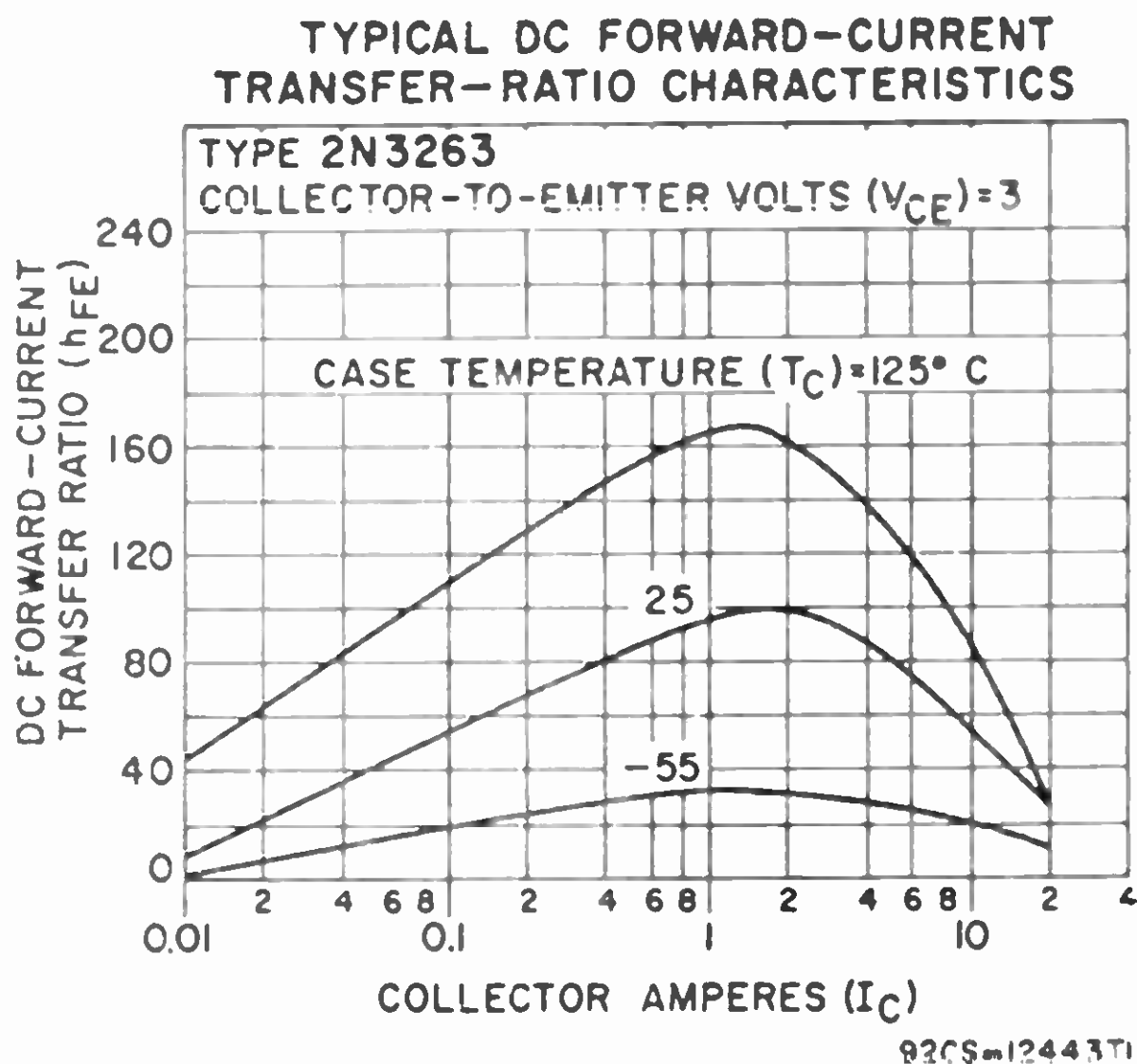
Collector-to-Base Voltage	V_{CBO}	150	V
Collector-to-Emitter Voltage:			
$V_{BE} = -1.5$ V	V_{CEV}	150	V
$R_{BE} \leq 50 \Omega$	$V_{CE(sus)}$	110	V
Base open (sustaining voltage)	$V_{CE0(sus)}$	90	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Collector Current	I_C	25	A
Base Current	I_B	10	A
Transistor Dissipation	P_T	See Rating Chart	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage:			
$I_C = 0.2$ A, $I_B = 0$	$V_{CE0(sus)}$	90 min	V
$I_C = 0.2$ A, $R_{BE} \leq 50 \Omega$	$V_{CE(sus)}$	110 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 15$ A, $I_B = 1.2$ A, $t_p \leq 350 \mu s$, $df \leq 2\%$)	$V_{CE(sat)}$	0.75 max	V
Base-to-Emitter Saturation Voltage ($I_C = 15$ A, $I_B = 1.5$ A, $t_p \leq 350 \mu s$, $df \leq 2\%$)	$V_{BE(sat)}$	1.6 max	V
Emitter-to-Base Voltage ($I_E = 0.02$ A, $I_C = 0$)	V_{EBO}	7 min	V
Collector-Cutoff Current:			
$V_{CE} = 150$ V, $V_{BE} = -1.5$ V, $T_C = 25^\circ C$	I_{CEV}	20 max	mA
$V_{CB} = 80$ V, $I_E = 0$, $T_C = 25^\circ C$	I_{CBO}	4 max	mA
$V_{CB} = 80$ V, $I_E = 0$, $T_C = 125^\circ C$	I_{CBO}	4 max	mA
Emitter-Cutoff Current:			
$V_{EB} = 5$ V, $I_C = 0$, $T_C = 25^\circ C$	I_{EBO}	5 max	mA
$V_{EB} = 5$ V, $I_C = 0$, $T_C = 125^\circ C$	I_{EBO}	5 max	mA

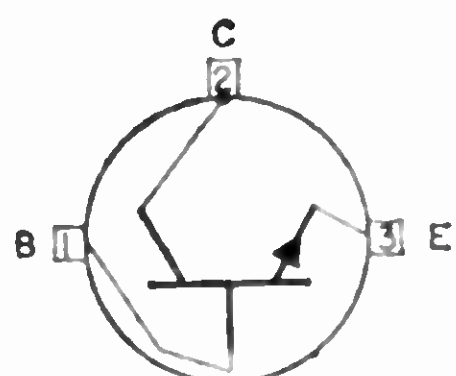
CHARACTERISTICS (cont'd)

Pulsed Static Forward-Current Transfer Ratio:			
($V_{CE} = 3 \text{ V}$, $I_C = 5 \text{ A}$, $t_p \leq 350 \mu\text{s}$, $df \leq 2\%$)	$h_{FE}(\text{pulsed})$	40 min	
($V_{CE} = 3 \text{ V}$, $I_C = 15 \text{ A}$, $t_p \leq 350 \mu\text{s}$, $df \leq 2\%$)	$h_{FE}(\text{pulsed})$	25 to 75	
($V_{CE} = 4 \text{ V}$, $I_C = 20 \text{ A}$, $t_p \leq 350 \mu\text{s}$, $df \leq 2\%$)	$h_{FE}(\text{pulsed})$	20 min	
Collector-to-Base Feedback Capacitance ($V_{CB} = 10 \text{ V}$, $I_E = 0$, $f = 1 \text{ MHz}$)	$c_{b'c}$	900 max	pF
Turn-On Time, Saturated Switch ($V_{CC} = 30 \text{ V}$, $I_C = 15 \text{ A}$, $I_{B1} = 1.2 \text{ A}$, $I_{B2} = -1.2 \text{ A}$)	$t_d + t_r$	0.5 max	μs
Fall Time, Saturated Switch ($V_{CC} = 30 \text{ V}$, $I_C = 15 \text{ A}$, $I_{B1} = 1.2 \text{ A}$, $I_{B2} = -1.2 \text{ A}$)	t_f	0.5 max	μs
Storage Time, Saturated Switch ($V_{CC} = 30 \text{ V}$, $I_C = 15 \text{ A}$, $I_{B1} = 1.2 \text{ A}$, $I_{B2} = -1.2 \text{ A}$)	t_s	1.5 max	μs
Gain-Bandwidth Product ($V_{CE} = 10 \text{ V}$, $I_C = 3 \text{ A}$, $f = 5 \text{ MHz}$)	f_T	20 min	MHz
Second-Breakdown Current, Safe Operating Region ($V_{CE} = 75 \text{ V}$)	$I_{S/b}$	350 min	mA
Second-Breakdown Energy, Safe Operating Region ($V_{BE} = -6 \text{ V}$, $I_C = 10 \text{ A}$, $R_{BE} = 20 \Omega$, $L = 40 \mu\text{H}$)	$E_{S/b}$	2 min	mJ
Thermal Resistance, Junction-to-Case	Θ_{J-C}	1.5 max	$^\circ\text{C}/\text{W}$



POWER TRANSISTOR

2N3264



to type 2N3263.

Si n-p-n epitaxial type used in high-power, high-speed, and high-current applications, such as switching circuits, amplifiers, and power oscillators in aerospace, military, and industrial applications. Outline No.29. For curves of safe operating region, transfer characteristics, and static forward-current transfer ratio, refer

MAXIMUM RATINGS

Collector-to-Base Voltage	V _{CBO}	120	V
Collector-to-Emitter Voltage:			
V _{BE} = -1.5 V	V _{CEV}	120	V
R _{BE} = 50 Ω	V _{CER(SUS)}	80	V
Base open (sustaining voltage)	V _{CEO(SUS)}	60	V
Emitter-to-Base Voltage	V _{EBO}	7	V
Collector Current	I _C	25	A
Base Current	I _B	10	A
Transistor Dissipation	See Rating Chart for type 2N3263		
Temperature Range:			
Operating (Junction)	T _J (opr)	-65 to 200	°C
Storage	T _{STG}	-65 to 200	°C

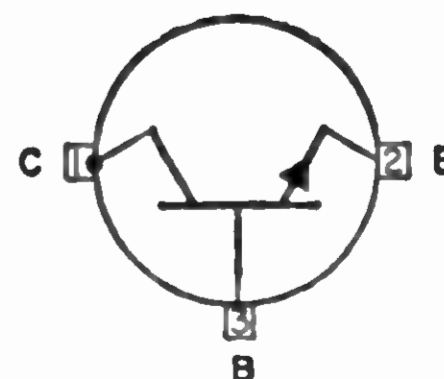
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage:			
I _C = 0.2 A, I _B = 0	V _{CEO(SUS)}	60 min	V
I _C = 0.2 A, R _{BE} ≤ 50 Ω	V _{CER(SUS)}	80 min	V
Collector-to-Emitter Saturation Voltage (I _C = 15 A, I _B = 1.2 A, t _p ≤ 350 μs, df ≤ 2%)	V _{CE(sat)}	1.2 max	V
Base-to-Emitter Saturation Voltage (I _C = 15 A, I _B = 1.5 A, t _p ≤ 350 μs, df ≤ 2%)	V _{BE(sat)}	1.8 max	V
Emitter-to-Base Voltage (I _E = 0.02 A, I _C = 0)	V _{EBO}	7 min	V
Collector-Cutoff Current:			
V _{CE} = 120 V, V _{BE} = -1.5 V, T _C = 25°C	I _{CEV}	20 max	mA
V _{CB} = 60 V, I _E = 0, T _C = 25°C	I _{CBO}	10 max	mA
V _{CB} = 60 V, I _E = 0, T _C = 125°C	I _{CBO}	10 max	mA
Emitter-Cutoff Current:			
V _{EB} = 5 V, I _C = 0, T _C = 25°C	I _{EBO}	15 max	mA
V _{EB} = 5 V, I _C = 0, T _C = 125°C	I _{EBO}	15 max	mA
Pulsed Static Forward-Current Transfer Ratio:			
V _{CE} = 3 V, I _C = 5 A, t _p ≤ 350 μs, df ≤ 2%	h _{FE} (pulsed)	35 min	
V _{CE} = 3 V, I _C = 15 A, t _p ≤ 350 μs, df ≤ 2%	h _{FE} (pulsed)	20 to 80	
V _{CE} = 4 V, I _C = 20 A, t _p ≤ 350 μs, df ≤ 2%	h _{FE} (pulsed)	15 min	
Collector-to-Base Feedback Capacitance (V _{CB} = 10 V, I _E = 0, f = 1 MHz)	c _{b'c}	900 max	pF
Turn-On Time, Saturated Switch (V _{CC} = 30 V, I _C = 15 A, I _{B1} = 1.2 A, I _{B2} = -1.2 A)	t _d + t _r	0.5 max	μs
Fall Time, Saturated Switch (V _{CC} = 30 V, I _C = 15 A, I _{B1} = 1.2 A, I _{B2} = -1.2 A)	t _f	0.5 max	μs
Storage Time, Saturated Switch (V _{CC} = 30 V, I _C = 15 A, I _{B1} = 1.2 A, I _{B2} = -1.2 A)	t _s	1.5 max	μs
Gain-Bandwidth Product (V _{CE} = 10 V, I _C = 3 A, f = 5 MHz)	f _T	20 min	MHz
Second-Breakdown Current, Safe Operating Region (V _{CE} = 75 V)	I _{S/b}	700 min	mA
Second-Breakdown Energy, Safe Operating Region (V _{BE} = 6 V, I _C = 10 A, R _{BE} = 20 Ω, L = 40 μH)	E _{S/b}	2 min	mJ
Thermal Resistance, Junction-to-Case	θ _{J-C}	1.5 max	°C/W

2N3265

POWER TRANSISTOR

Si n-p-n epitaxial type used in high-power, high-speed, and high-current applications such as switching circuits, amplifiers, and power oscillators in aerospace, military, and industrial applications. JEDEC TO-63, Outline No.24. See Mounting Hardware for desired mounting arrangement. This type is identical with type 2N3263 except for the following items:

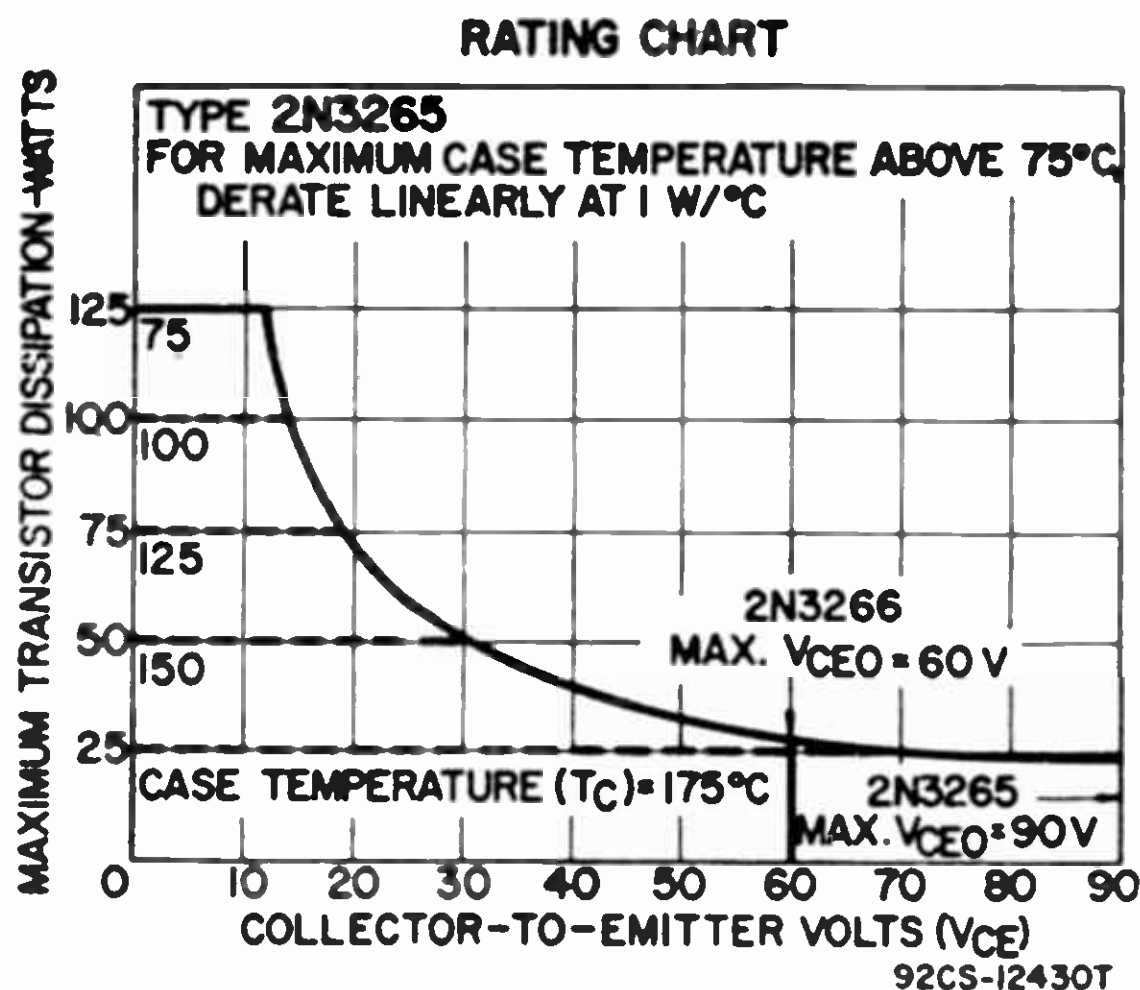


MAXIMUM RATINGS

Transistor Dissipation	P _T	See Rating Chart
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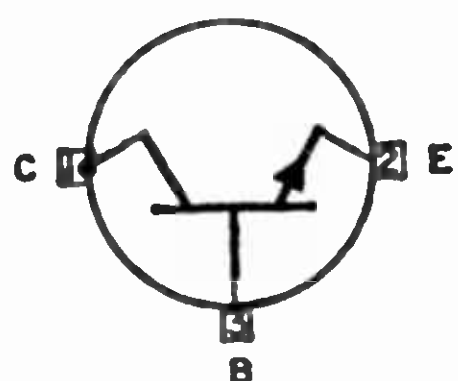
CHARACTERISTICS (At case temperature = 25°C)

Thermal Resistance, Junction-to-Case	θ _{J-C}	1 max °C/W
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POWER TRANSISTOR

2N3266



Si n-p-n epitaxial type used in high-power, high-speed, and high-current applications such as switching circuits, amplifiers, and power oscillators in aerospace, military, and industrial applications. JEDEC TO-63, Outline No.24. See Mounting Hardware for desired mounting arrangement. For curves of safe operating

region, transfer characteristics, and static forward-current transfer ratio, refer to type 2N3263. This type is identical with type 2N3264 except for the following items:

MAXIMUM RATINGS

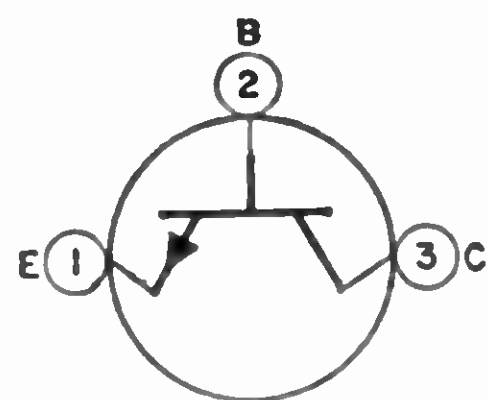
Transistor Dissipation See Rating Chart for Type 2N3265

CHARACTERISTICS (At case temperature = 25°C)

Thermal Resistance, Junction-to-Case θ_{J-C} 1 max °C/W

TRANSISTOR

2N3375



Si n-p-n "overlay" epitaxial planar type used in large-signal, high-power vhf-uhf applications for industrial and military communications equipment in class A, B, or C amplifier, frequency-multiplier, or oscillator operation. JEDEC TO-60, Outline No.23. See Mounting Hardware for desired mounting arrangement.

MAXIMUM RATING

Collector-to-Base Voltage	V _{CBO}	65	V
Collector-to-Emitter Voltage:			
V _{BE} = -1.5 V	V _{CEV}	65	V
Base open	V _{CEO}	40	V
Emitter-to-Base Voltage	V _{EB0}	4	V
Collector Current	I _C	1.5	A
Base Current	I _B	0.2	A
Transistor Dissipation:			
T _c up to 25°C	P _T	11.6	W
T _c above 25°C	P _T	See curve page 300	
Temperature Range:			
Operating (Junction)	T _J	-65 to 200	°C
Storage	T _{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T _L	230	°C

CHARACTERISTICS (At case temperature = 25°C)

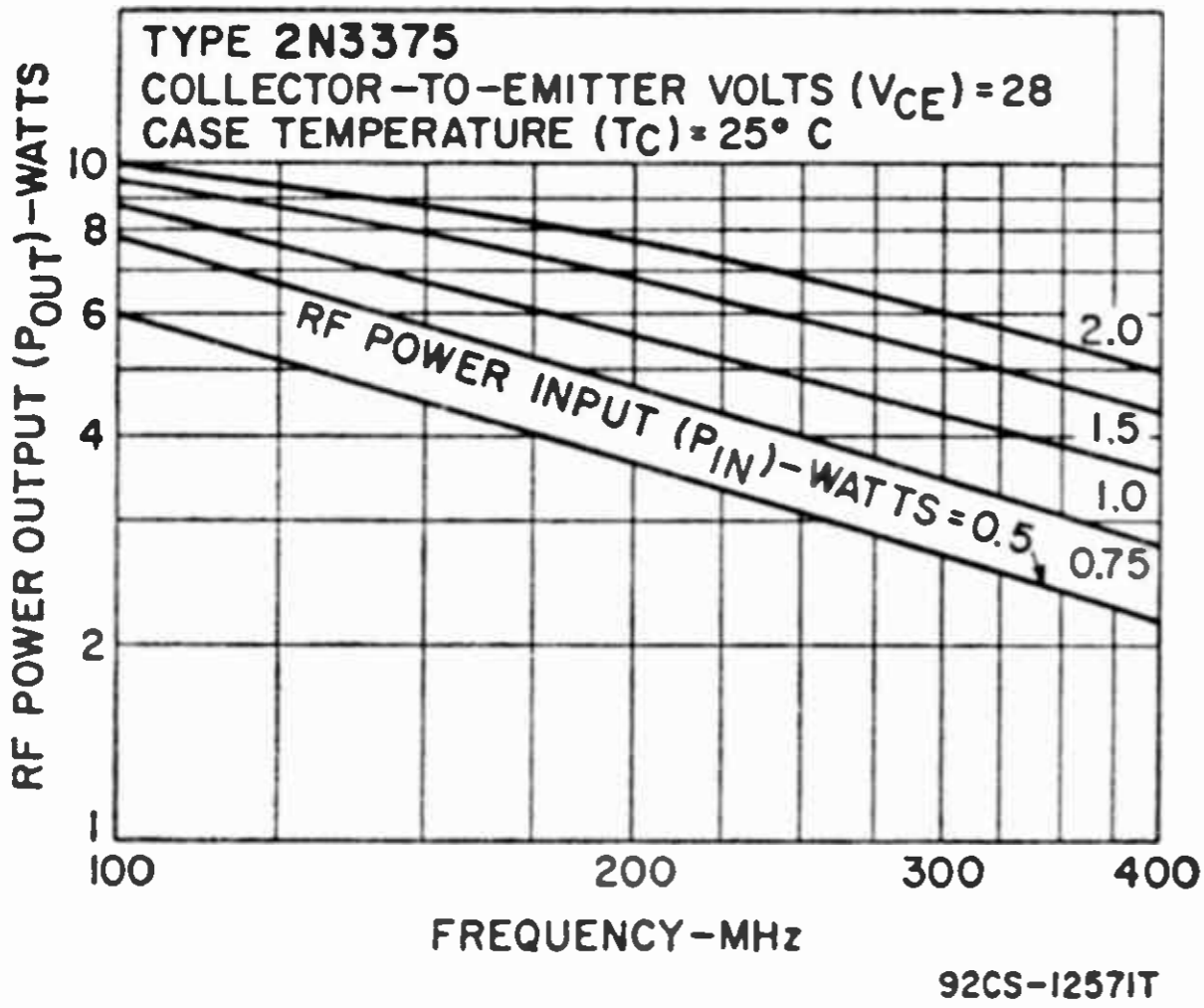
Collector-to-Base Breakdown Voltage			
I _C = 0.1 mA, I _E = 0)	V _{(BR)CBO}	65 min	V
Collector-to-Emitter Breakdown Voltage:			
I _C = 0 to 0.2 A, I _B = 0, pulsed through an inductor			
L = 25 mH, df = 50%	V _{(BR)CEO}	40▲ min	V
I _C = 0 to 0.2 A, V _{BE} = -1.5 V, pulsed through an			
inductor L = 25 mH, df = 50%	V _{(BR)CEV}	65▲ min	V

CHARACTERISTICS (cont'd)

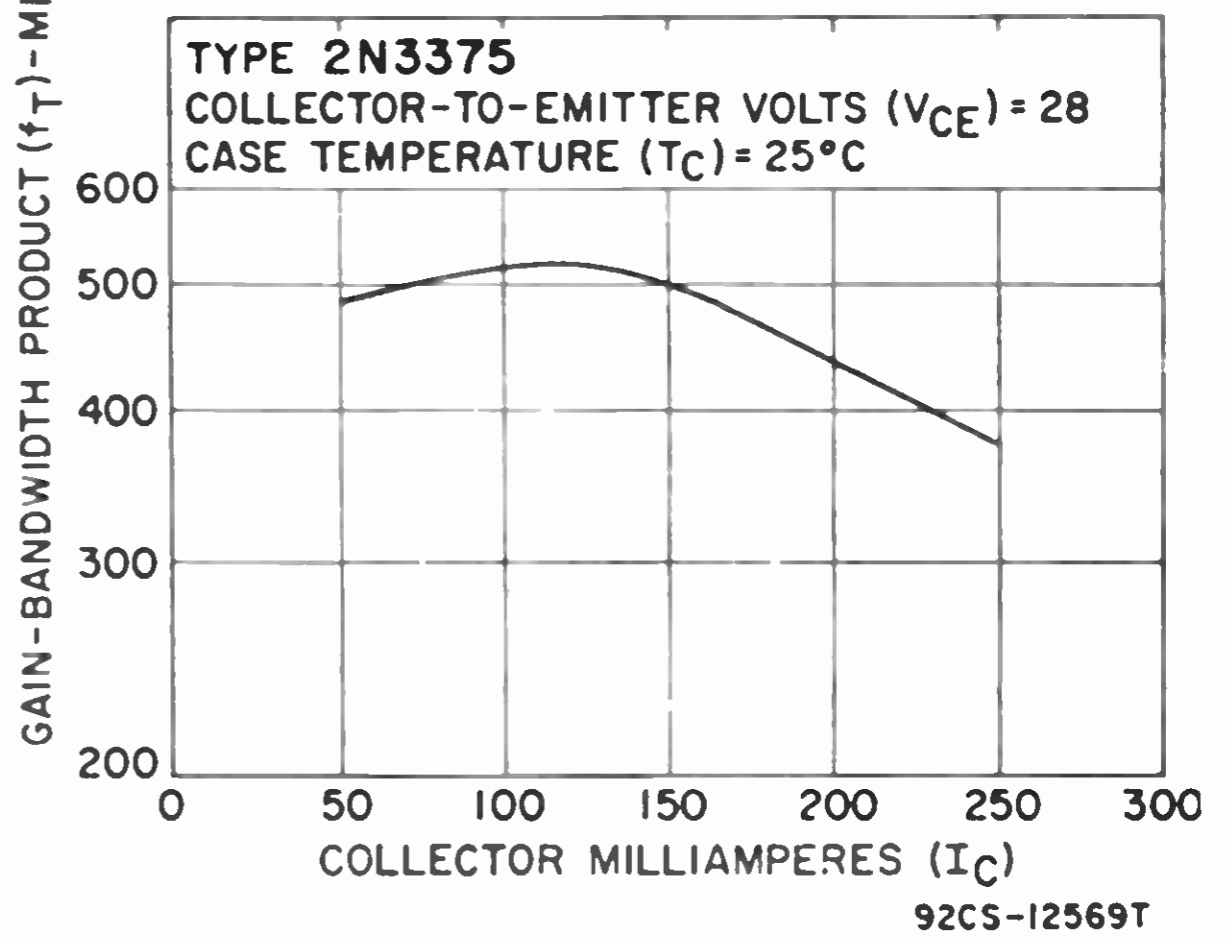
Emitter-to-Base Breakdown Voltage ($I_E = 0.1 \text{ mA}, I_C = 0$)	$V_{(BR)EBO}$	4 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 500 \text{ mA}, I_B = 100 \text{ mA}$)	$V_{CE(sat)}$	1 max	V
Collector-Cutoff Current ($V_{CE} = 30 \text{ V}, I = 0$)	I_{CEO}	0.1 max	mA
RF Power Output: Unneutralized Amplifier			
$V_{CE} = 28 \text{ V}, P_{IE} = 1 \text{ W}, f = 100 \text{ MHz}$	P_{OE}	7.5● min	W
$V_{CE} = 28 \text{ V}, P_{IE} = 1 \text{ W}, f = 400 \text{ MHz}$	P_{OE}	3* min	W
Oscillator $V_{CE} = 28 \text{ V}, f = 500 \text{ MHz}$	P_{OE}	2.5■	W
Collector-to-Case Capacitance	C_c	6 max	pF
Collector-to-Base Feedback Capacitance ($V_{CB} = 30 \text{ V}, I_E = 0, f = 1 \text{ MHz}$)	C_{cb}	10 max	pF
Gain-Bandwidth Product ($V_{CE} = 28 \text{ V}, I_C = 150 \text{ mA}$)	f_T	500	MHz
Intrinsic Base-Spreading Resistance ($V_{CE} = 28 \text{ V}, I_C = 250 \text{ mA}, f = 400 \text{ MHz}$)	$r_{bb'}$	10	Ω

- ▲ Measured at a current where the breakdown voltage is a minimum.
- For conditions given, minimum efficiency = 65 per cent.
- * For conditions given, minimum efficiency = 40 per cent.
- For conditions given, typical efficiency = 40 per cent.

TYPICAL OPERATION CHARACTERISTICS



TYPICAL SMALL-SIGNAL OPERATION CHARACTERISTIC

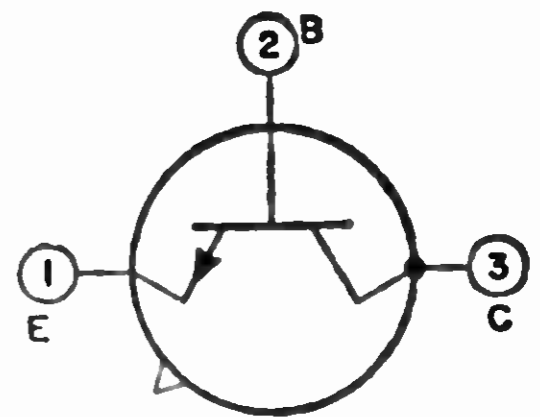


2N3435

Refer to Chart of Discontinued Transistors

2N3439 TRANSISTOR

Si n-p-n triple-diffused type used in high-speed-switching and linear-amplifier applications, such as high-voltage differential and operational amplifiers, high-voltage inverters, and series regulators for industrial and military applications. JEDEC TO-5, Outline No.5.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	450	V
Collector-to-Emitter Sustaining Voltage	$V_{CEO(sus)}$	350	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Collector Current	I_C	1	A
Base Current	I_B	0.5	A
Transistor Dissipation:			
T_A up to 50°C	P_T	1●	W
T_C up to 25°C	P_T	10	W
T_A above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	255	°C

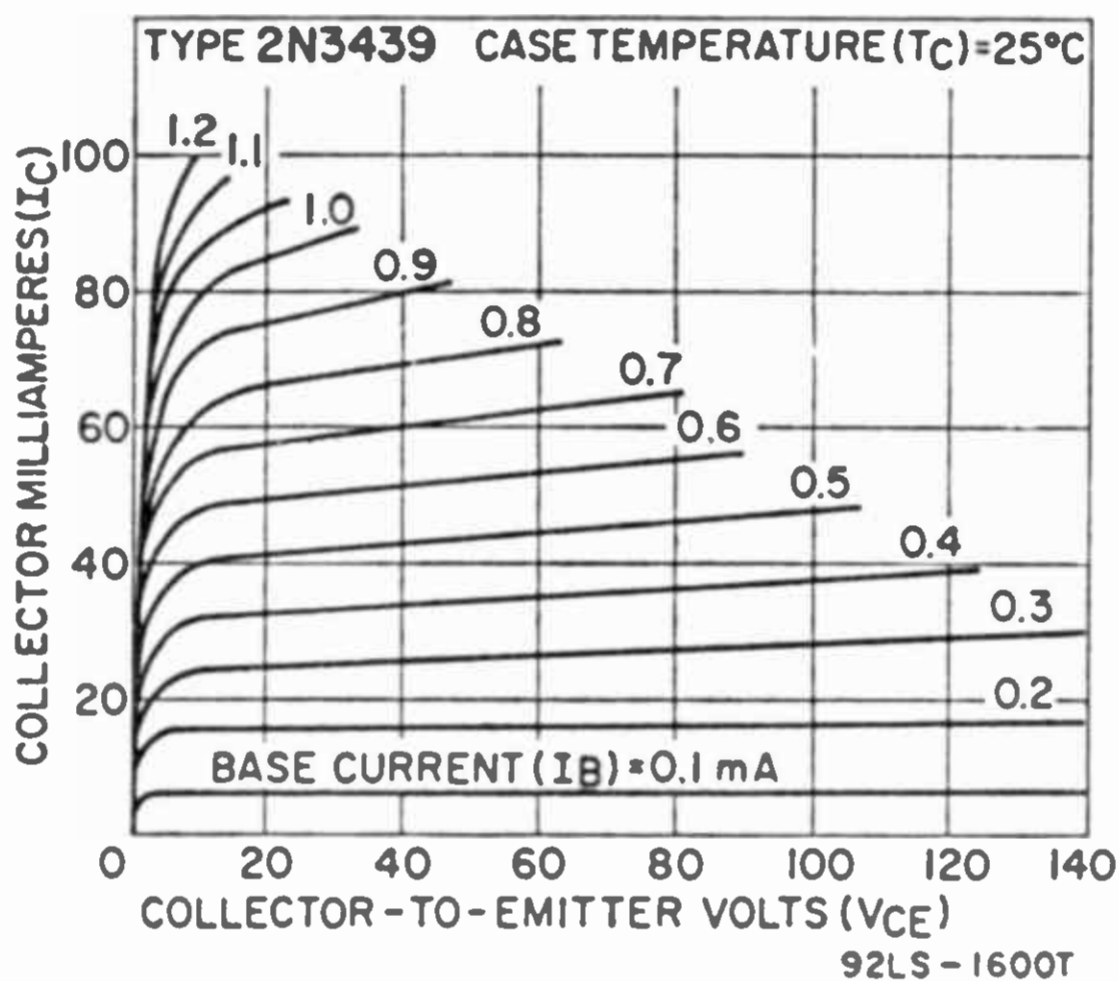
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_C = 50$ mA, $I_B = 0$)	$V_{CE0(sus)}$	350 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 50$ mA, $I_B = 4$ mA)	$V_{CE(sat)}$	0.5 max	V
Base-to-Emitter Saturation Voltage ($I_C = 50$ mA, $I_B = 4$ mA)	$V_{BE(sat)}$	1.3 max	V
Collector-Cutoff Current:			
$V_{CE} = 300$ V, $I_B = 0$	I_{CEO}	20 max	μ A
$V_{CE} = 450$ V, $V_{BE} = -1.5$ V	I_{CEV}	500 max	μ A
Emitter-Cutoff Current ($V_{EB} = 6$ V, $I_C = 0$)	I_{EBO}	20 max	μ A
Static Forward-Current Transfer Ratio:			
$V_{CE} = 10$ V, $I_C = 20$ mA	h_{FE}	40 to 160	
$V_{CE} = 10$ V, $I_C = 2$ mA	h_{FE}	30* min	
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 10$ V, $I_C = 10$ mA, $f = 5$ MHz)	h_{fe}	3 min	
Second-Breakdown Current, Safe Operating Region ($V_{CE} = 200$ V)	$I_{S/b}$	50 min	mA
Output Capacitance ($V_{CB} = 10$ V, $I_E = 0$, $f = 1$ MHz)	C_{obo}	10 max	pF
Thermal Resistance, Junction-to-Case	θ_{J-C}	17.5 max	$^{\circ}$ C/W

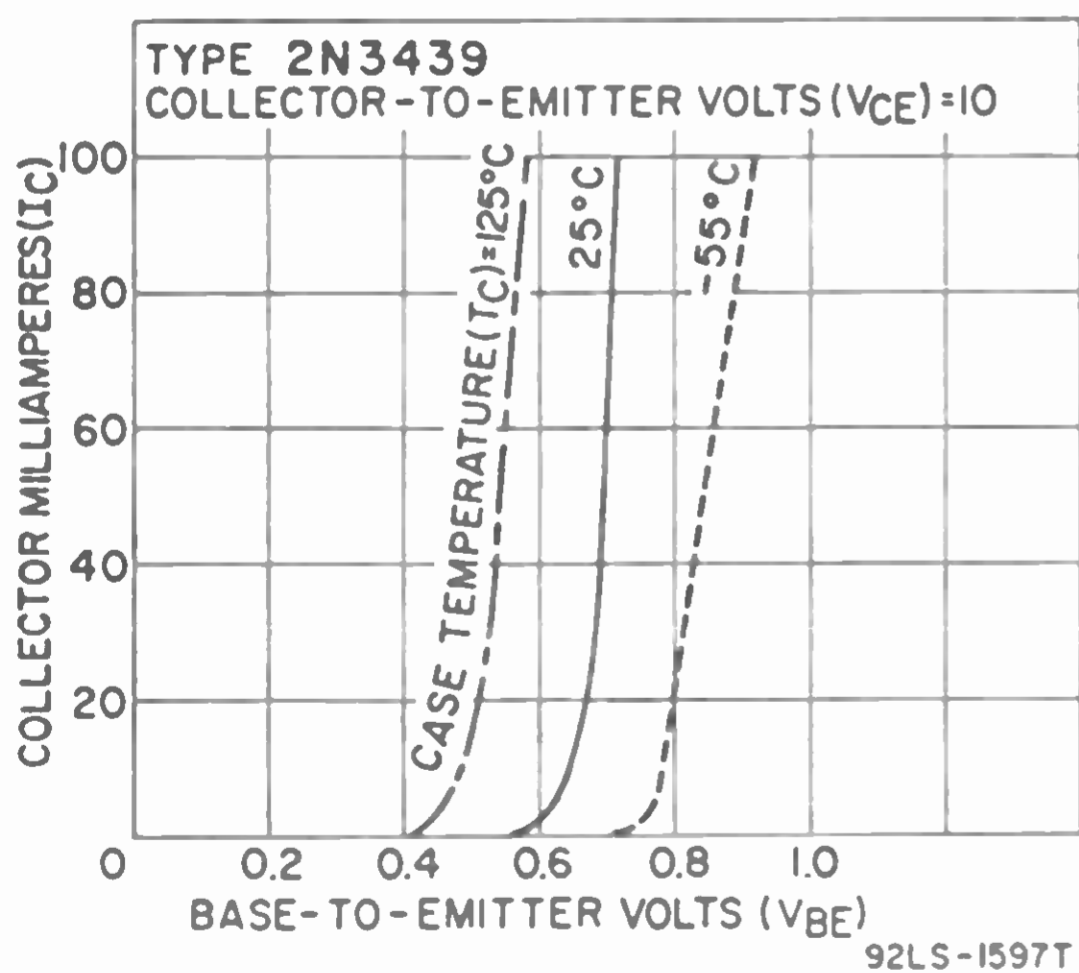
* This value does not apply to type 2N3440.

• This value does not apply to types 2N4063 and 2N4064.

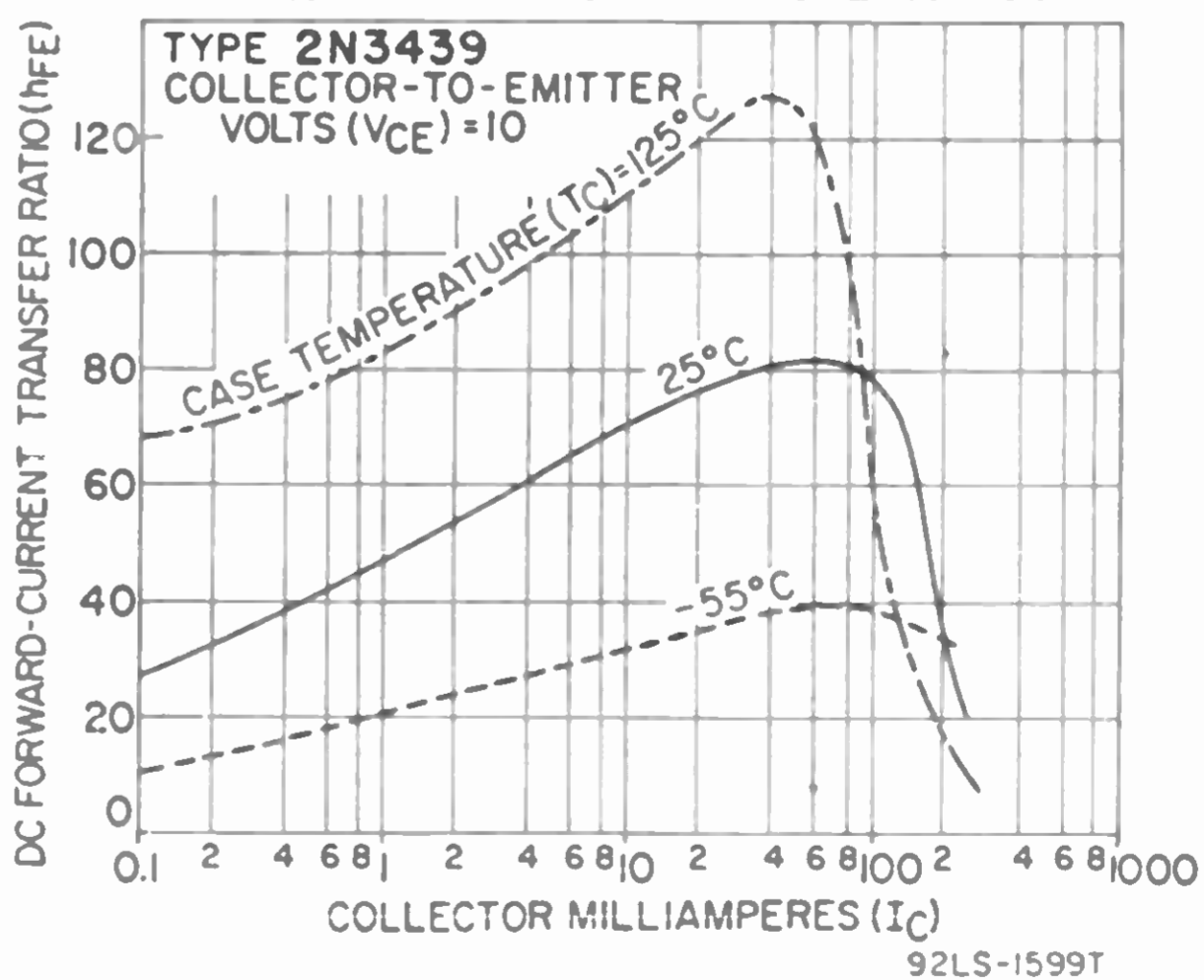
TYPICAL COLLECTOR CHARACTERISTICS



TYPICAL TRANSFER CHARACTERISTICS

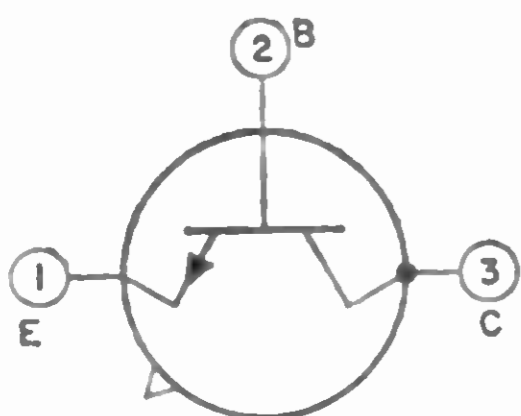


TYPICAL DC FORWARD-CURRENT TRANSFER-RATIO CHARACTERISTICS



TRANSISTOR

2N3440



Si n-p-n triple-diffused type used in high-speed-switching and linear-amplifier applications such as high-voltage differential and operational amplifiers, high-voltage inverters, and series regulators for industrial and military applications. JEDEC TO-5, Outline No.5. This type is identical with type 2N3439

except for the following items:

MAXIMUM RATINGS

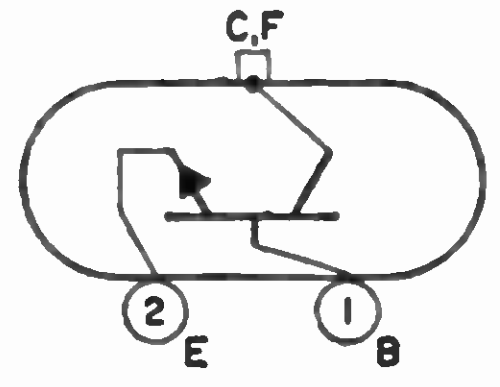
Collector-to-Base Voltage	V_{CBO}	300	V
Collector-to-Emitter Voltage:			
$V_{BE} = -1.5$ V	V_{CEV}	300	V
Base open (sustaining voltage)	$V_{CEO(sus)}$	250	V

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_C = 50$ mA, $I_B = 0$)	$V_{CEO(sus)}$	250	V
Collector-Cutoff Current:			
$V_{CE} = 200$ V, $I_B = 0$	I_{CEO}	50 max	μA
$V_{CE} = 300$ V, $V_{BE} = -1.5$ V	I_{CEV}	500 max	μA

2N3441 POWER TRANSISTOR

Si n-p-n diffused type for high-voltage applications in power-switching circuits, series- and shunt-regulator driver and output stages, and in dc-to-dc converters in military, industrial, and commercial equipment. This type features a base comprised of a homogeneous-resistivity silicon material. JEDEC TO-66, Outline No.25. See Mounting Hardware for desired mounting arrangement.



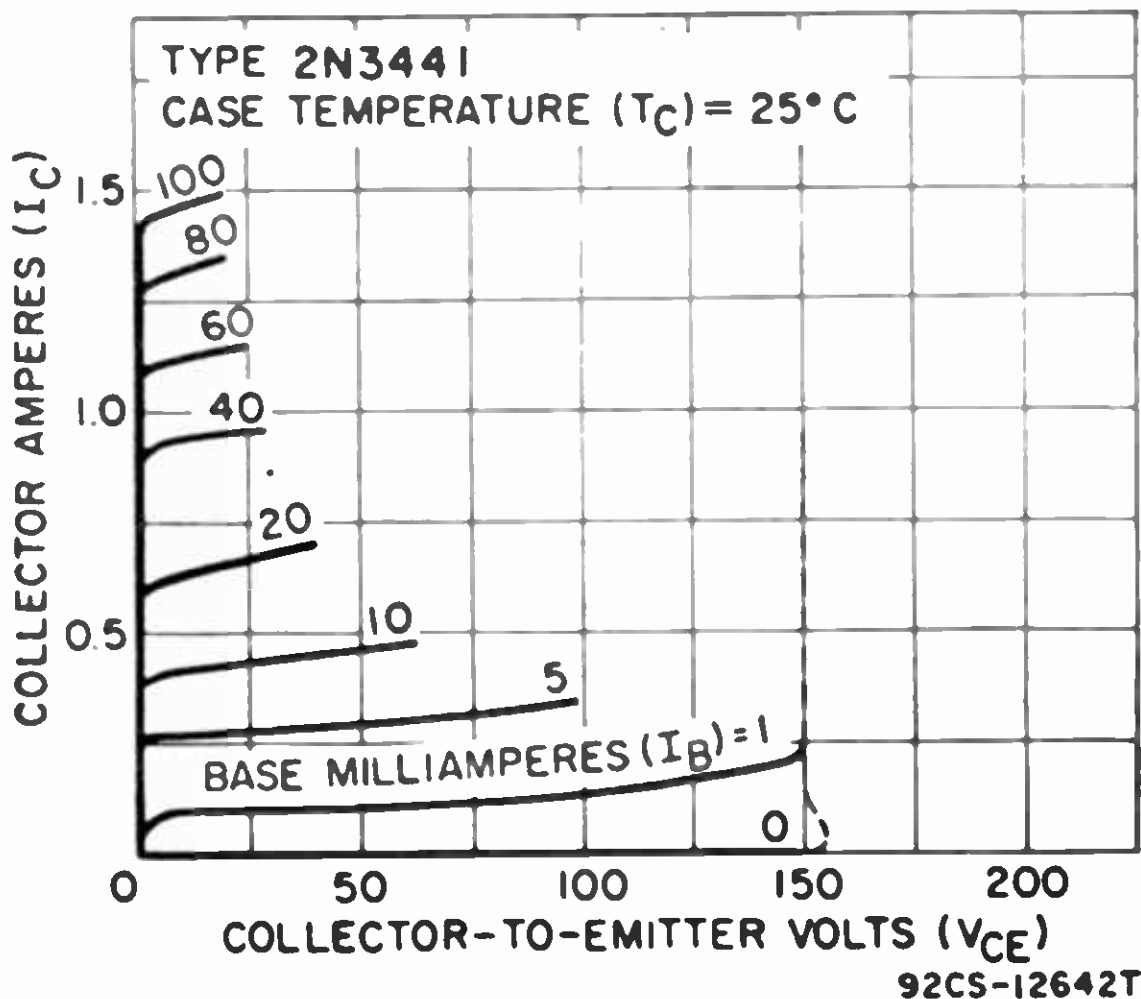
MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	160	V
Collector-to-Emitter Voltage:			
$V_{BE} = -1.5$ V	V_{CEV}	160	V
Base open (sustaining voltage)	$V_{CEO(sus)}$	140	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Collector Current	I_C	3	A
Peak Collector Current	i_C	4	A
Base Current	I_B	2	A
Transistor Dissipation:			
T_C up to 25°C	P_T	25	W
T_A up to 25°C	P_T	5.8	W
T_A or T_C above 25°C	P_T	See curve page	300
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Pin-Soldering Temperature (10 s max)	T_P	255	°C

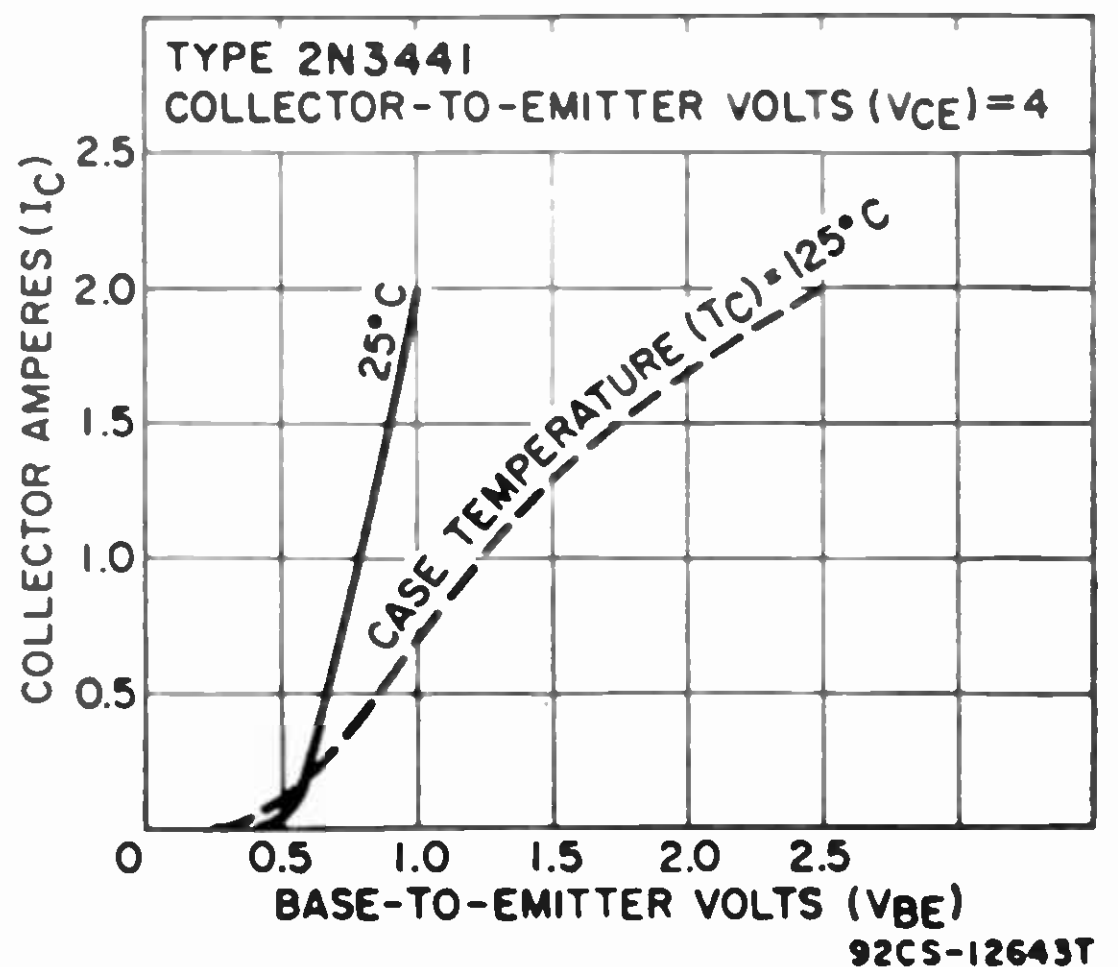
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage:			
$I_C = 0.1$ to 2 A, $I_B = 0$	$V_{CEO(sus)}$	140 min	V
$I_C = 0.1$ to 1 A, $V_{BE} = -1.5$ V	$V_{CEV(sus)}$	160 min	V
$I_C = 0.1$ to 1 A, $R_{BE} = 100$ Ω	$V_{CEV(sus)}$	150* min	V
Collector-to-Emitter Saturation Voltage ($I_C = 0.5$ A, $I_B = 50$ mA)	$V_{CE(sat)}$	1 max	V
Base-to-Emitter Voltage ($V_{CE} = 4$ V, $I_C = 0.5$ A)	V_{BE}	1.7 max	V
Collector-Cutoff Current:			
$V_{CE} = 140$ V, $V_{BE} = -1.5$ V, $T_C = 25^\circ C$	I_{CEO}	1 max	mA
$V_{CE} = 140$ V, $V_{BE} = -1.5$ V, $T_C = 150^\circ C$	I_{CEO}	5 max	mA
Emitter-Cutoff Current ($V_{EB} = 7$ V, $I_C = 0$)	I_{EBO}	1 max	mA

TYPICAL COLLECTOR CHARACTERISTICS



TYPICAL TRANSFER CHARACTERISTICS



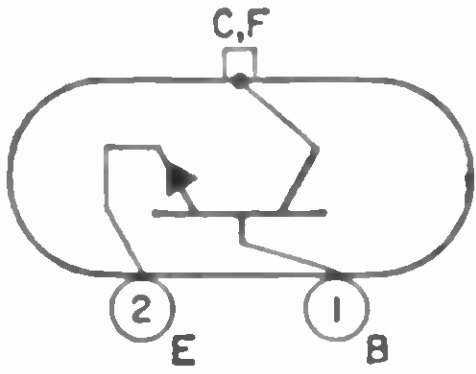
CHARACTERISTICS (cont'd)

Static Forward-Current Transfer Ratio ($V_{CE} = 4 \text{ V}$, $I_C = 0.5 \text{ A}$)	h_{FE}	20 to 80	
Power Rating Test: $V_{CE} = 32.5 \text{ V}$, $I_C = 0.9 \text{ A}$, $t = 1 \text{ s}$		29	W
$V_{CE} = 120 \text{ V}$, $I = 0.24 \text{ A}$, $t = 1 \text{ s}$		29	W
Thermal Resistance, Junction-to-Case	θ_{J-C}	7● max	$^{\circ}\text{C/W}$

* This value does not apply to type 2N3442.
● This value does not apply to type 40373.

POWER TRANSISTOR 2N3442

Si n-p-n diffused type for high-voltage applications in power-switching circuits, series- and shunt-regulator driver and output stages, and in dc-to-dc converters in military, industrial, and commercial equipment. This type features a base comprised of a homogeneous-resistivity silicon material. JEDEC TO-3, Outline No.2. See Mounting Hardware for desired mounting arrangement. This type is identical with type 2N3441 except for the following items:



No.2. See Mounting Hardware for desired mounting arrangement. This type is identical with type 2N3441 except for the following items:

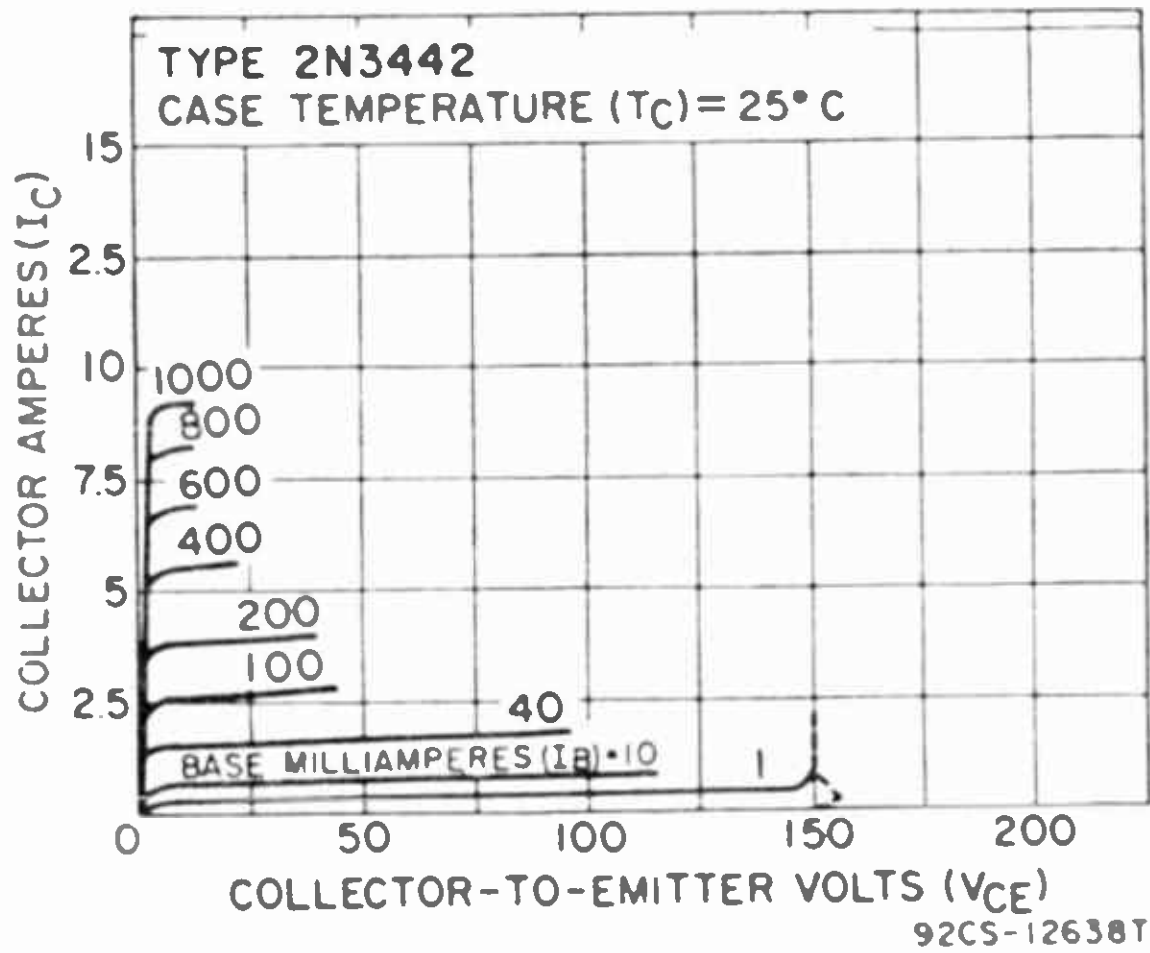
MAXIMUM RATINGS

Collector Current	I_C	10	A
Base Current	I_B	7	A
Transistor Dissipation:			
T_c up to 25°C	P_T	117	W
T_c up to 25°C	P_T	See curve page 300	

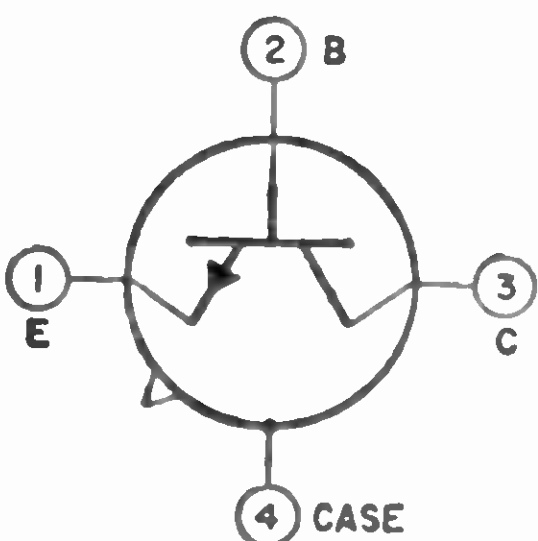
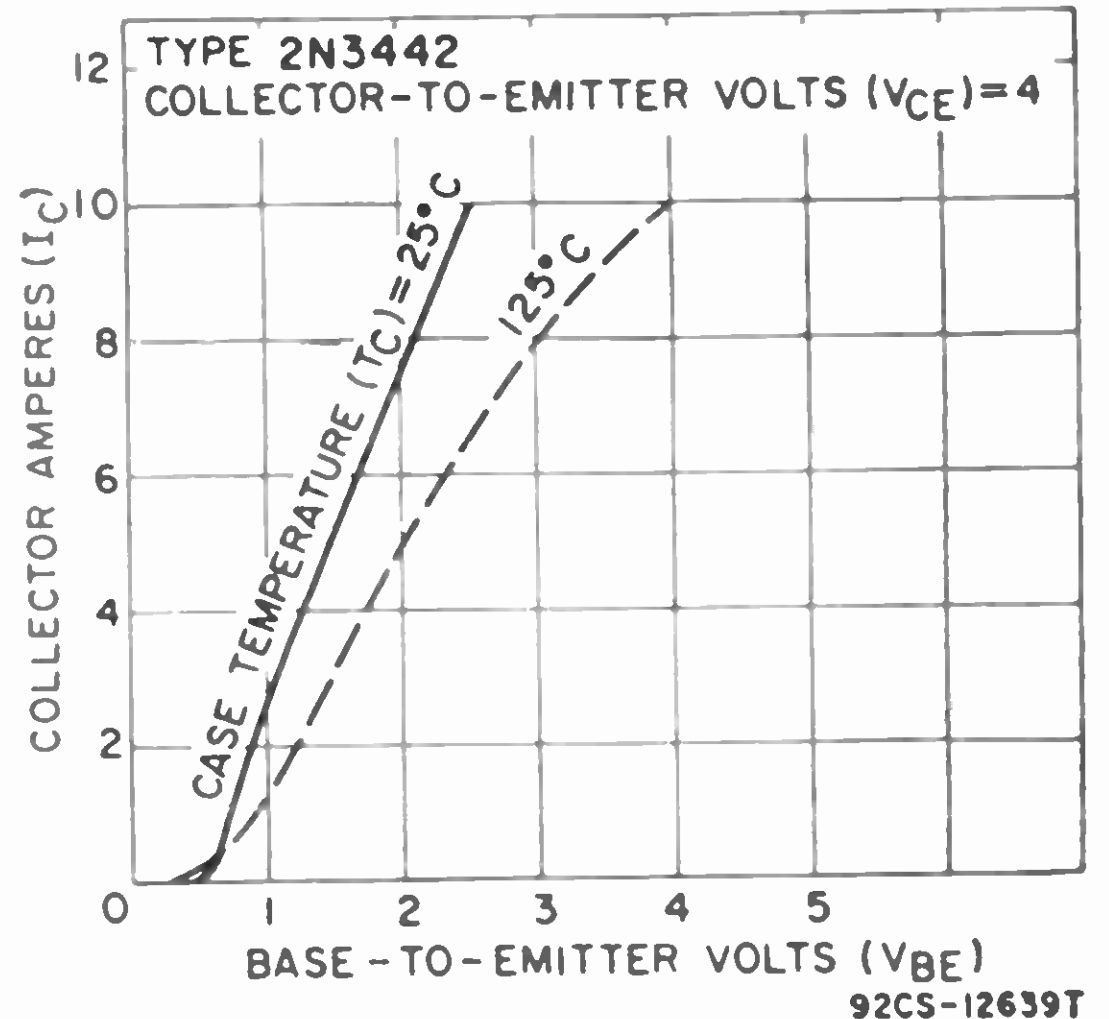
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage: $I_C = 0.2$ to 3 A , $I_B = 0$	$V_{CE0}(\text{sus})$	140 min	V
$I_C = 0.1$ to 1.5 A , $V_{BE} = -1.5 \text{ V}$	$V_{CEV}(\text{sus})$	160 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 3 \text{ A}$, $I_B = 300 \text{ mA}$)	$V_{CE}(\text{sat})$	1 max	V
Base-to-Emitter Voltage ($V_{CE} = 4 \text{ V}$, $I_C = 3 \text{ A}$)	V_{BE}	1.7 max	V
Collector-Cutoff Current: $V_{CE} = 140 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_c = 150^{\circ}\text{C}$	I_{CEV}	10 max	mA
$V_{CB} = 140 \text{ V}$, $I_E = 0$	I_{CEV}	1	mA
Emitter-Cutoff Current ($V_{EB} = 7 \text{ V}$, $I_C = 0$)	I_{EBO}	5 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 4 \text{ V}$, $I_C = 3 \text{ A}$)	h_{FE}	20 to 70	
Power Rating Test ($V_{CE} = 78 \text{ V}$, $I_C = 1.5 \text{ A}$, $t = 1 \text{ s}$)		117	W
Thermal Resistance, Junction-to-Case	θ_{J-C}	1.5 max	$^{\circ}\text{C/W}$

TYPICAL COLLECTOR CHARACTERISTICS



TYPICAL TRANSFER CHARACTERISTICS



TRANSISTOR 2N3478

Si n-p-n epitaxial planar type for vhf-uhf applications at frequencies up to 470 MHz in industrial and commercial equipment. JEDEC TO-104, Outline No.31.

MAXIMUM RATINGS

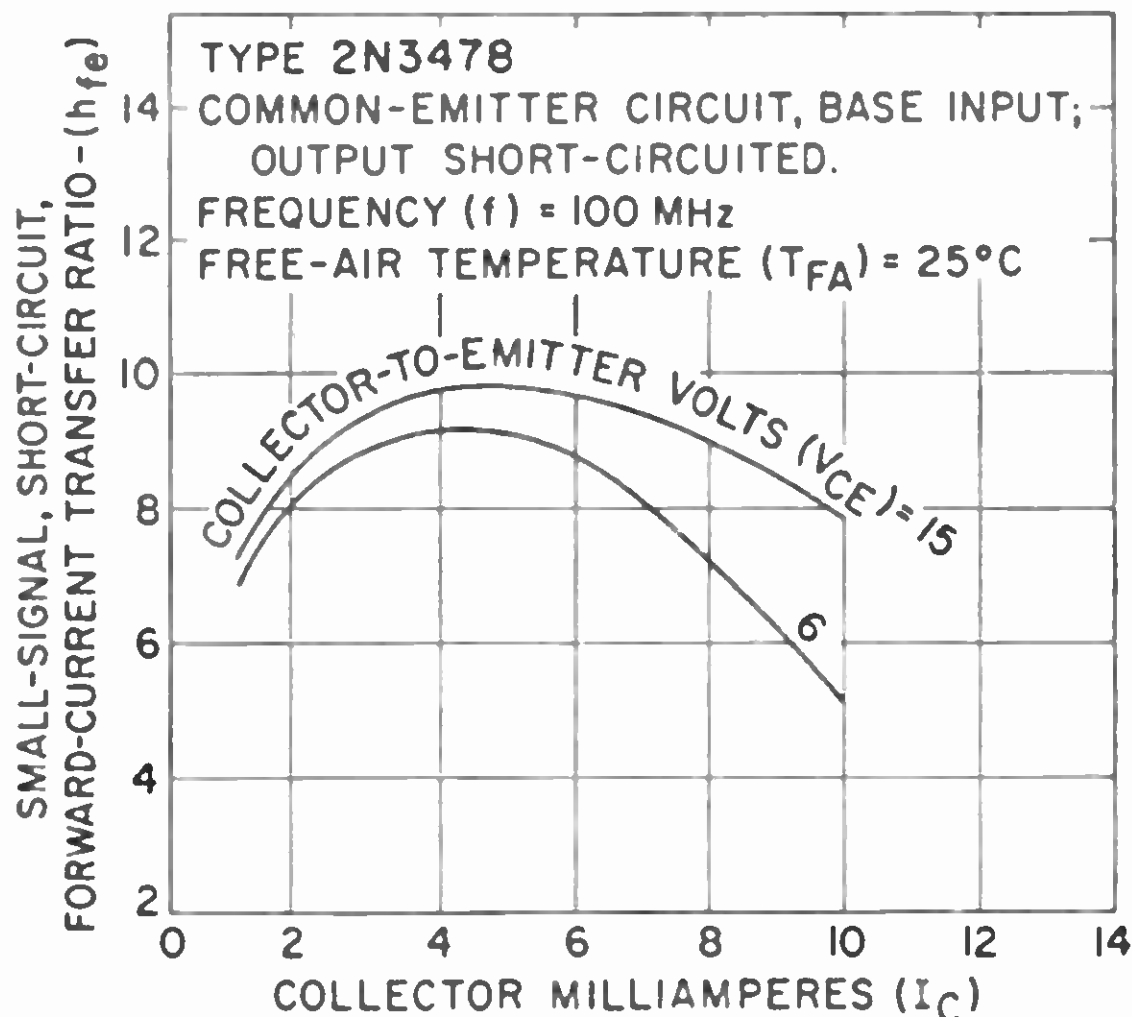
Collector-to-Base Voltage	V _{CB0}	30	V
Collector-to-Emitter Voltage	V _{CE0}	15	V
Emitter-to-Base Voltage	V _{EBO}	2	V
Collector Current	I _C	Limited by power dissipation	
Transistor Dissipation:			
T _A up to 25°C	P _T	200	mW
T _A above 25°C	P _T	See curve page 300	
Temperature Range:			
Operating (Junction)	T _J (opr)	-65 to 200	°C
Storage	T _{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T _L	265	°C

CHARACTERISTICS

Collector-to-Base Breakdown Voltage (I _C = 0.001 mA, I _E = 0)	V _{(BR)CBO}	30 min	V
Collector-to-Emitter Breakdown Voltage (I _C = 0.001 mA, I _B = 0)	V _{(BR)CEO}	15 min	V
Emitter-to-Base Breakdown Voltage (I _E = 0.001 mA, I _C = 0)	V _{(BR)EBO}	2 min	V
Collector-Cutoff Current (V _{CB} = 1 V, I _E = 0)	I _{CBO}	0.02 max	μA
Static Forward-Current Transfer Ratio (V _{CE} = 8 V, I _C = 2 mA)	h _{FE}	25 to 150	
Small-Signal Forward-Current Transfer Ratio* (V _{CE} = 8 V, I _C = 2 mA, f = 100 MHz)	h _{fe}	7.5 to 16	
Collector-to-Base Feedback Capacitance (V _{CB} = 8 V, I _E = 0, f = 0.1 to 1 MHz)	C _{cb}	0.7 max	pF
Small-Signal Power Gain:			
Unneutralized Amplifier Circuit*			
V _{CE} = 8 V, I _C = 2 mA, f = 200 MHz	G _{pe}	11.5 to 17	dB
Neutralized Amplifier Circuit			
R _S = 50 Ω, I _C = 1.5 mA, V _{CE} = 6 V, f = 470 MHz	G _{pe}	12	dB
Noise Figure*			
UHF—R _S = 50 Ω, V _{CE} = 6 V, I _C = 1.5 mA, f = 470 MHz	NF	5	dB
VHF—V _{CE} = 8 V, I _C = 2 mA, f = 200 MHz	NF	4.5 max	dB

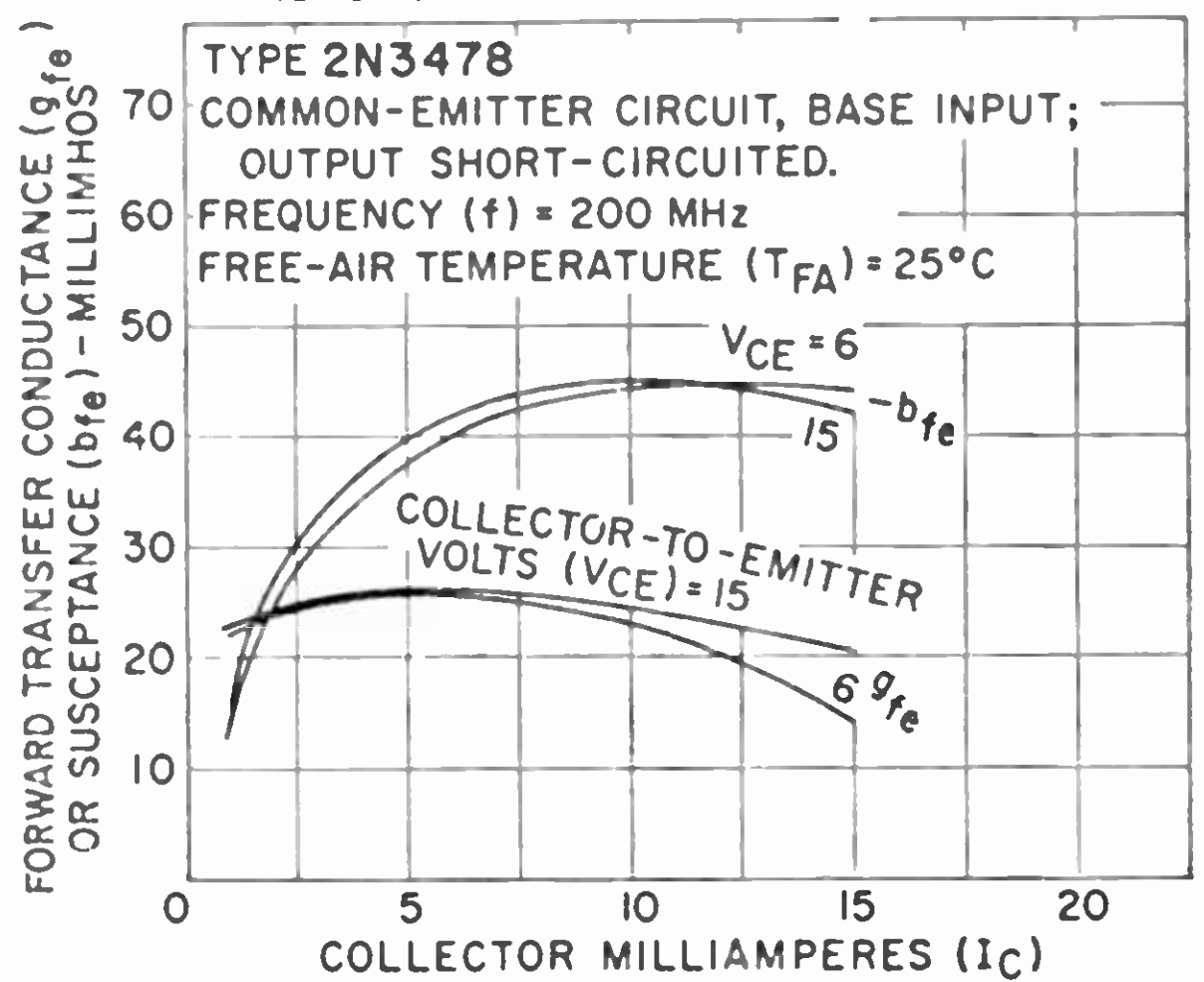
* Lead 4 (case) grounded.

TYPICAL SMALL-SIGNAL FORWARD-CURRENT TRANSFER-RATIO CHARACTERISTICS



92CS-12756T1

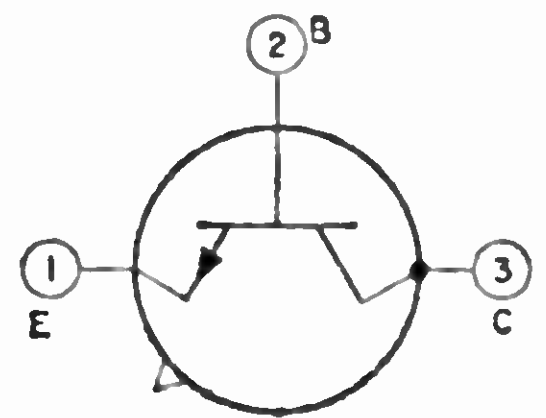
TYPICAL FORWARD TRANSFER CONDUCTANCE AND SUSCEPTANCE CHARACTERISTICS



92CS-12759T

2N3512 COMPUTER TRANSISTOR

Si n-p-n double-diffused epitaxial planar type used for core-driver and line-driver service in high-performance computers and in other critical applications requiring considerable output power. JEDEC TO-5, Outline No.5.



MAXIMUM RATINGS

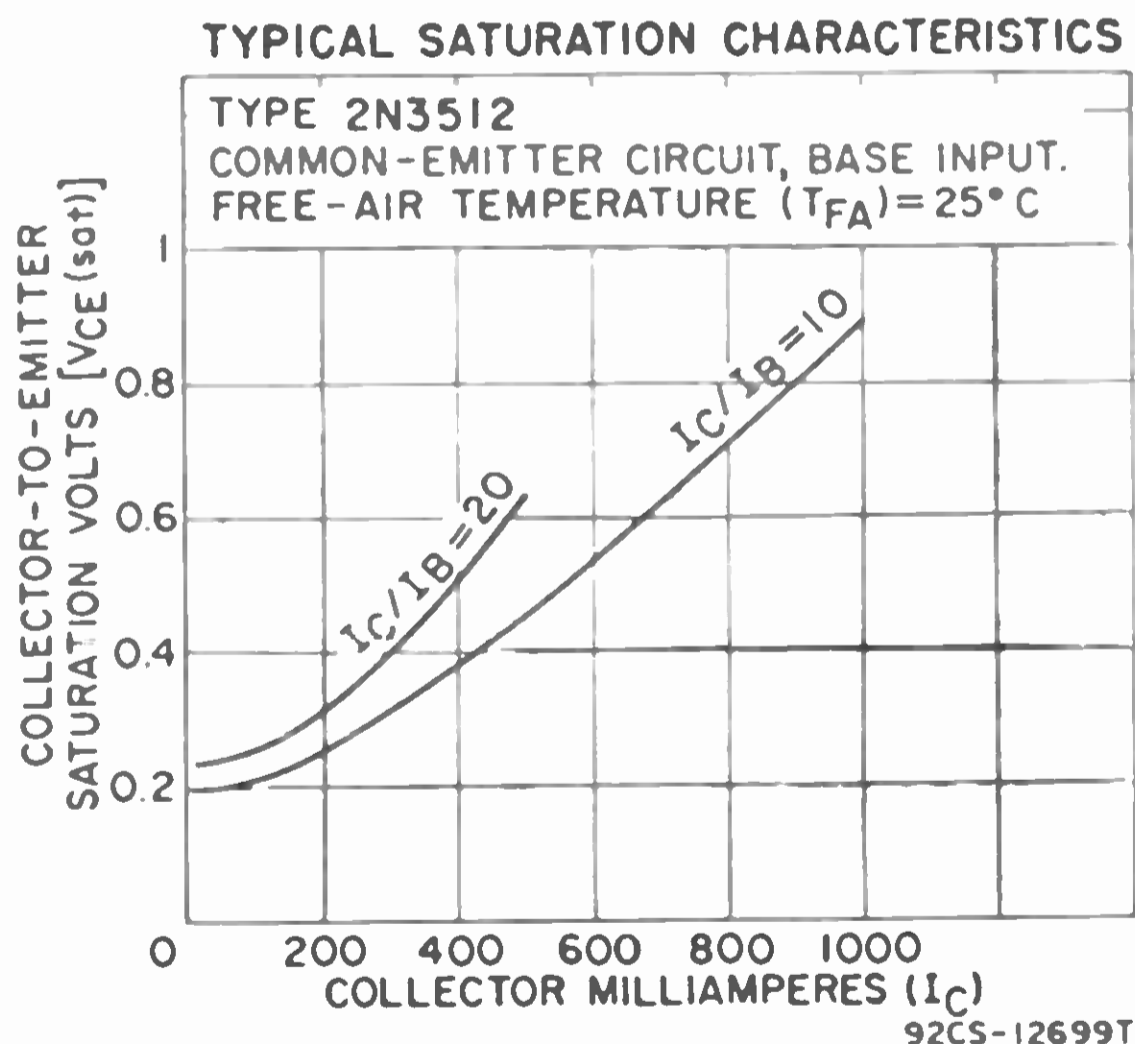
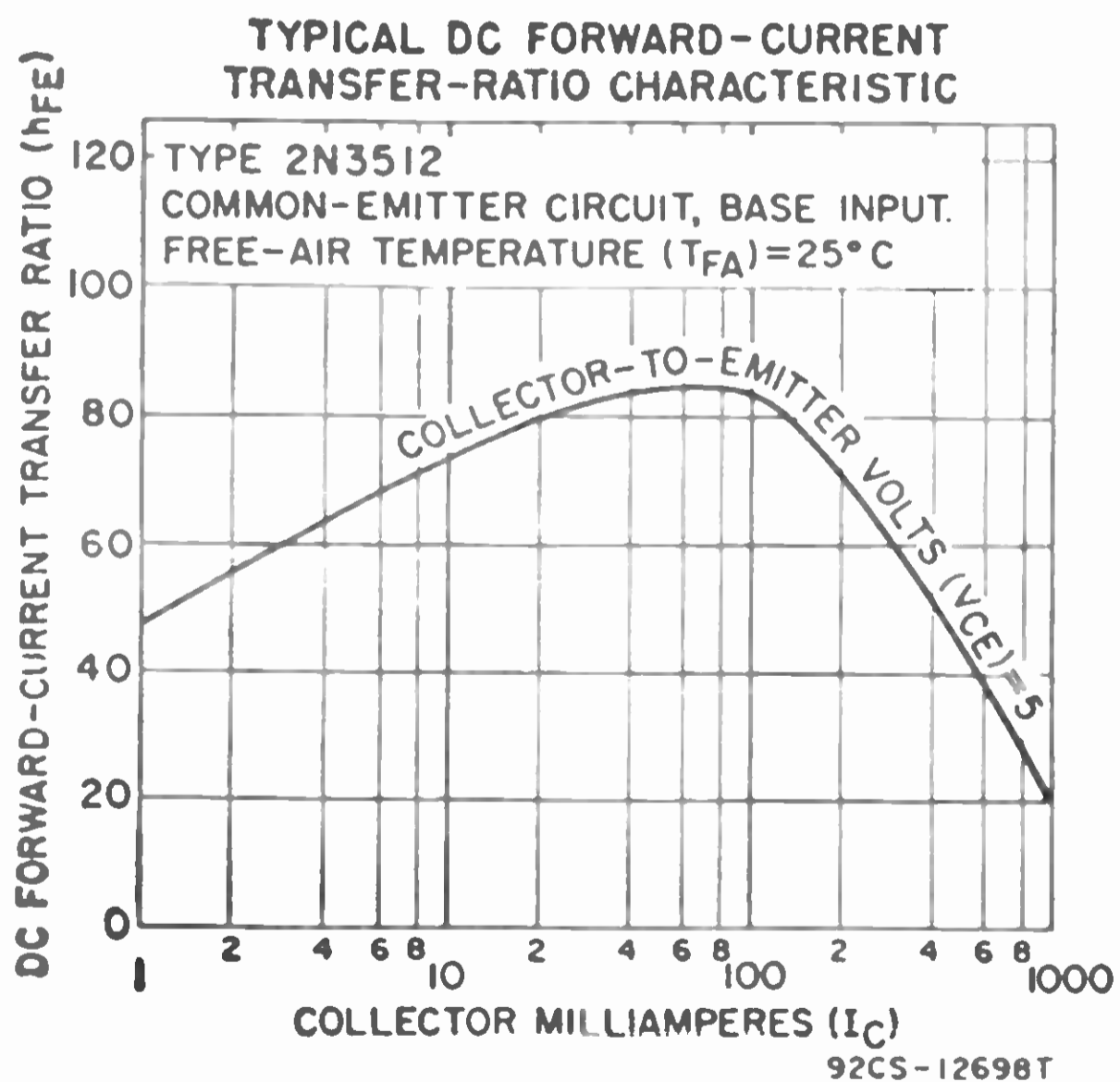
Collector-to-Base Voltage	V _{CB0}	60	V
Collector-to-Emitter Voltage	V _{CE0}	35	V
Emitter-to-Base Voltage	V _{EBO}	5	V

MAXIMUM RATINGS (cont'd)

Collector Current	I _C	Limited by power dissipation	
Transistor Dissipation:			
T _A up to 25°C	P _T	0.8	W
T _C up to 25°C (with heat sink)	P _T	4	W
T _A or T _C (with heat sink) above 25°C	P _T	See curve page 300	
Temperature Range:			
Operating (Junction)	T _J (opr)	-65 to 200	°C
Storage	T _{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T _L	230	°C

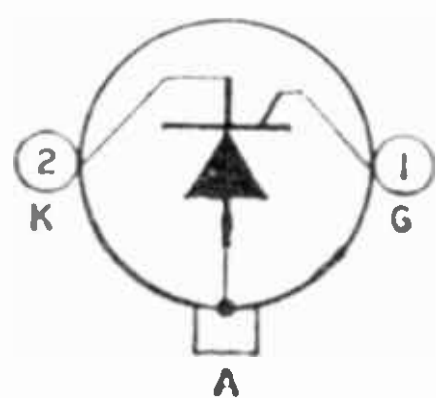
CHARACTERISTICS

Collector-to-Base Breakdown Voltage (I _C = 0.01 mA, I _E = 0)	V _{(BR)CBO}	60 min	V
Collector-to-Emitter Breakdown Voltage (I _C = 50 mA, I _B = 0)	V _{(BR)CEO}	35 min	V
Emitter-to-Base Breakdown Voltage (I _E = 0.1 mA, I _C = 0)	V _{(BR)EBO}	5 min	V
Collector-to-Emitter Saturation Voltage:			
I _C = 150 mA, I _B = 7.5 mA	V _{CE(sat)}	0.4 max	V
I _C = 500 mA, I _B = 50 mA, t _p = 400 μs, df ≤ 3% ...	V _{CE(sat)} (pulsed)	1 max	V
Base-to-Emitter Voltage (I _C = 150 mA, I _B = 7.5 mA)	V _{BE}	1 max	V
Base-Cutoff Current (V _{CE} = 30 V, V _{BE} = -0.3 V) ...	I _{BEV}	0.5 max	μA
Collector-Cutoff Current:			
V _{CE} = 30 V, V _{BE} = -0.3 V, T _A = 25°C	I _{CEV}	0.5 max	μA
V _{CE} = 30 V, V _{BE} = -0.3 V, T _A = 100°C	I _{CEV}	100 max	μA
Pulsed Static Forward-Current Transfer Ratio (V _{CE} = 1 V, I _C = 0.5 A, t _p = 400 μs, df ≤ 3%)	h _{FE} (pulsed)	10 min	
Small-Signal Forward-Current Transfer Ratio (V _{CE} = 10 V, I _C = 50 mA, f = 100 MHz)	h _{FE}	2.5 min	
Output Capacitance (V _{CB} = 10 V, I _E = 0, f = 0.14 MHz)	C _{obo}	10 max	pF
Storage Time (V _{CC} = 6.4 V, V _{BB} = 15.9 V, I _C = 150 mA, I _B = 15 mA)	t _s	30 max	ns
Turn-On Time (V _{CC} = 6.4 V, I _C = 150 mA, I _{B1} = 15 mA, I _{B2} = -15 mA)	t _d + t _r	30 max	ns
Turn-Off Time (V _{CC} = 6.4 V, V _{BB} = 15.9 V, I _C = 150 mA, I _{B2} = -15 mA, I _{B1} = 15 mA)	t _s + t _r	45 max	ns



SILICON CONTROLLED RECTIFIER

2N3525



Si all-diffused three-junction type for use in power-control and power-switching applications. See Mounting Hardware for desired mounting arrangement. JEDEC TO-66, Outline No.25. This type is identical with type 2N3228 except for the following items:

MAXIMUM RATINGS (For sinusoidal ac supply voltage at $f = 50$ to 400 Hz with resistive or inductive load)

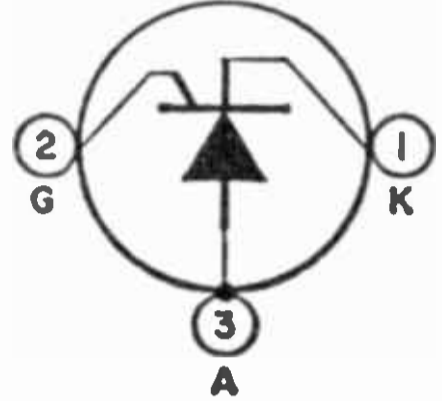
V_{RSOM}	660	V
V_{RROM}	400	V
V_{DROM}	600	V

CHARACTERISTICS (At maximum electrical ratings at $T_c = 25^\circ\text{C}$)

$V_{F(BO)O}$ ($T_c = 100^\circ\text{C}$)	400 min	V
I_{DOM} ($V_{DO} = V_{F(BO)O}$)	0.2 typ; 3 max	mA
I_{RROM} ($V_{RO} = V_{RROM}$, $T_c = 100^\circ\text{C}$)	0.1 typ; 1.5 max	mA

2N3528
2N3529

SILICON
CONTROLLED RECTIFIERS



Si all-diffused three-junction types for use in power-control and power-switching applications. JEDEC TO-8, Outline No.10. These types are identical with type 2N3228 except for the following items:

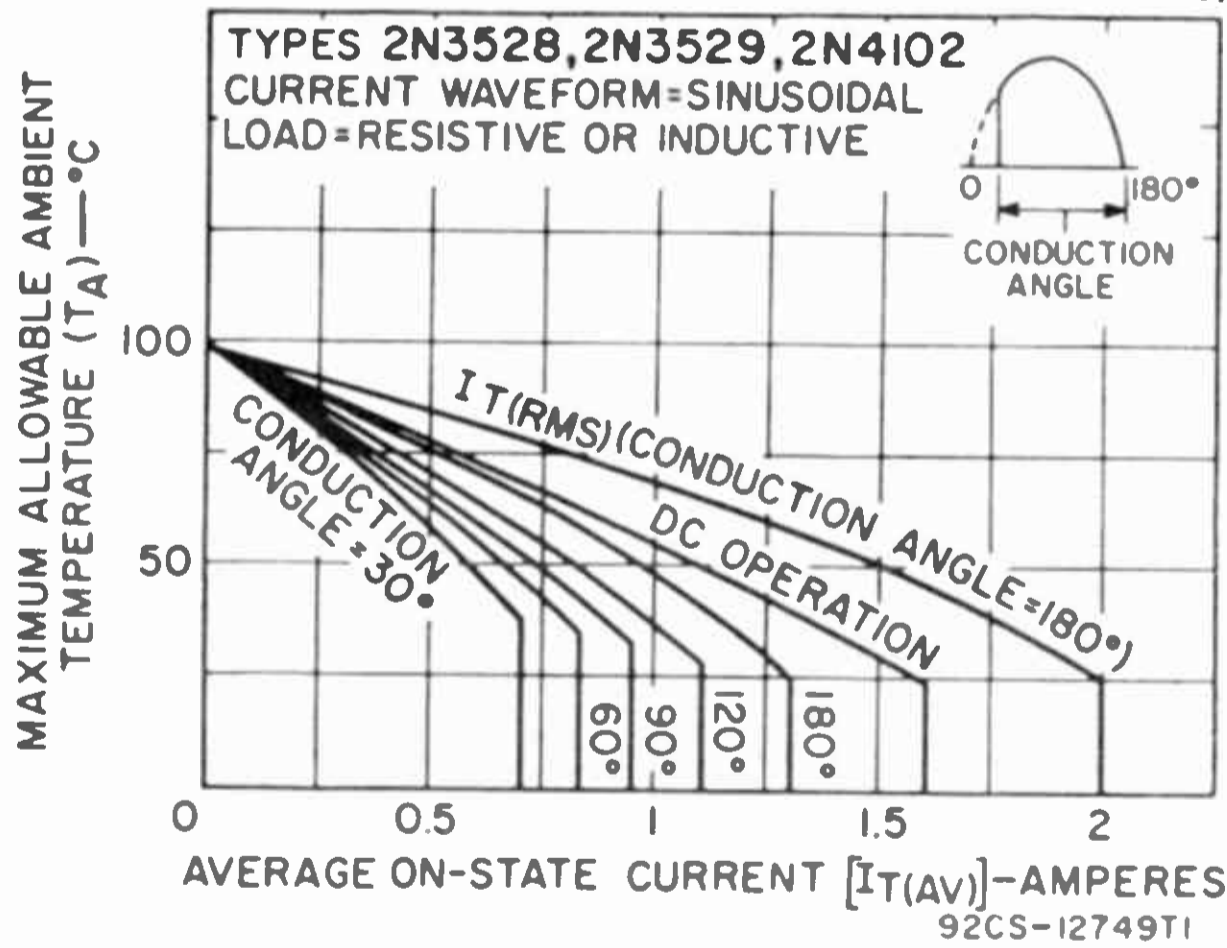
MAXIMUM RATINGS (For sinusoidal ac supply voltage at $f = 50$ to 400 Hz with resistive or inductive load)

	2N3528	2N3529	
V_{RSOM}	_____	660	V
V_{RROM}	_____	400	V
V_{DROM}	_____	600	V
$I_{T(AV)}$ (conduction angle = 180° , $T_A = 25^\circ\text{C}$) ...	_____	1.3	A
$I_{T(RMS)}$ ($T_A = 25^\circ\text{C}$)	_____	2	A

CHARACTERISTICS (At maximum electrical ratings at $T_c = 25^\circ\text{C}$)

$V_{F(BO)O}$ ($T_c = 100^\circ\text{C}$)	_____	400 min	V
I_{DOM} ($V_{DO} = V_{F(BO)O}$, $T_c = 100^\circ\text{C}$)	_____	0.2 typ; 3 max	mA
I_{RROM} ($V_{RO} = V_{RSOM}$, $T_c = 100^\circ\text{C}$)	_____	0.1 typ; 1.5 max	mA
θ_{J-A}	_____	40 max	$^\circ\text{C/W}$

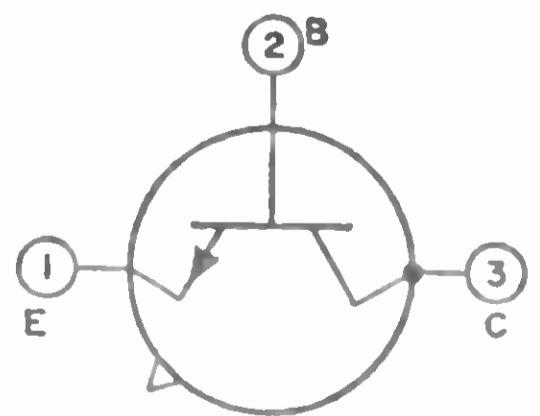
RATING CHART (AMBIENT TEMPERATURE)



2N3553

TRANSISTOR

Si n-p-n "overlay" epitaxial planar type used in class A, B, and C amplifiers, frequency multipliers, or oscillators in vhf-uhf applications for industrial and military communications. JEDEC TO-39, Outline No.15.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	65	V
Collector-to-Emitter Voltage:			
$V_{BE} = -1.5$ V	V_{CEV}	65	V
Base open	V_{CEO}	40	V

MAXIMUM RATINGS (cont'd)

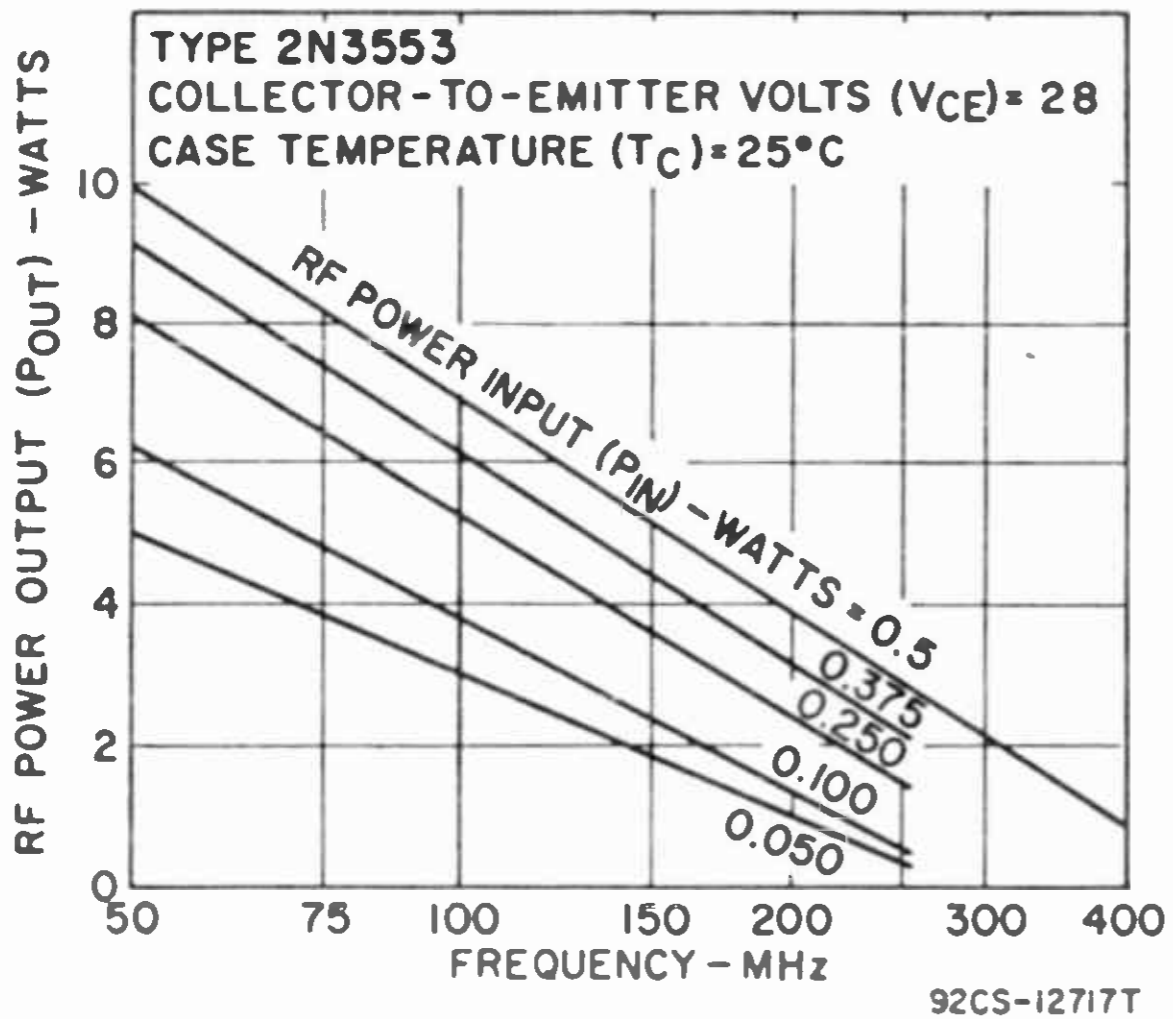
Emitter-to-Base Voltage	V_{EBO}	4	V
Collector Current	I_C	0.33	A
Peak Collector Current	i_C	1	A
Transistor Dissipation:			
T_C up to 25°C	P_T	7	W
T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	230	°C

CHARACTERISTICS (At case temperature = 25°C)

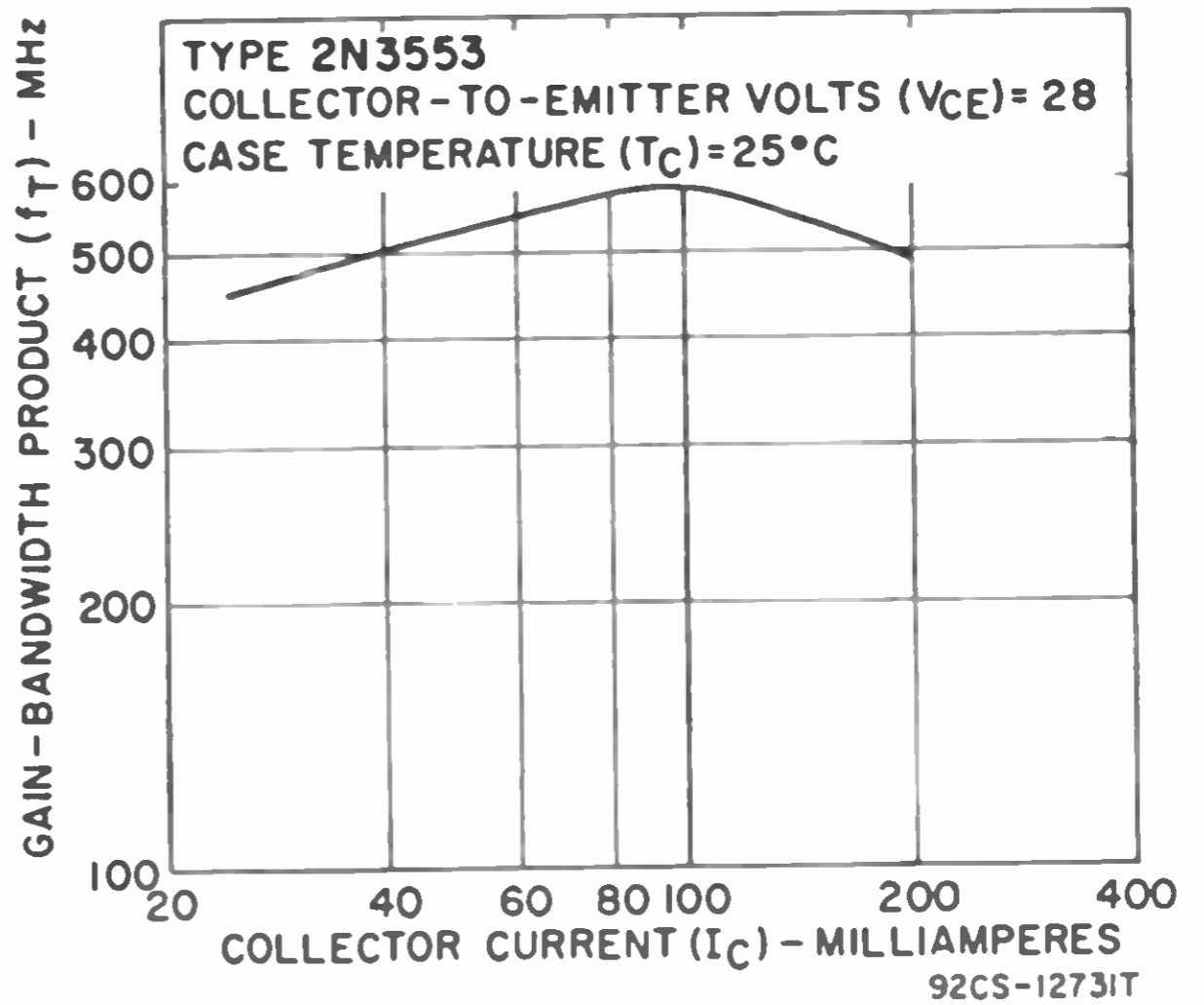
Collector-to-Base Breakdown Voltage ($I_C = 0.3$ mA, $I_E = 0$)	$V_{(BR)CBO}$	65 min	V
Collector-to-Emitter Breakdown Voltage: $I_C = 0$ to 0.2 A, $I_B = 0$, pulsed through an inductor $L = 25$ mH, $df = 50\%$	$V_{(BR)CEO}$	40 min	V
$I_C = 0$ to 0.2 A, $V_{BE} = -1.5$ V, pulsed through an inductor $L = 25$ mH, $df = 50\%$	$V_{(BR)CEV}$	65 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.1$ mA, $I_C = 0$)	$V_{(BR)EBO}$	4 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 250$ mA, $I_B = 50$ mA)	$V_{CE(sat)}$	1 max	V
Collector-Cutoff Current ($V_{CE} = 30$ V, $I_B = 0$)	I_{CEO}	0.1 max	mA
Intrinsic Base-Spreading Resistance ($V_{CE} = 28$ V, $I_C = 100$ mA, $f = 100$ MHz)	r_{bb}	12	Ω
Gain-Bandwidth Product ($V_{CE} = 28$ V, $I_C = 100$ mA)	f_T	500	MHz
Output Capacitance ($V_{CB} = 30$ V, $I_E = 0$, $f = 1$ MHz)	C_{ob0}	10 max	pF
RF Power Output: Unneutralized Amplifier— $V_{CC} = 28$ V, $P_{IE} = 0.25$ W, R_G and $R_L = 50$ Ω , $f = 175$ MHz	P_{OE}	2.5* min	W
Oscillator— $V_{CC} = 28$ V, $f = 500$ MHz	P_{OE}	1.5†	W

* For conditions given, minimum efficiency = 50 per cent.
† For conditions given, typical efficiency = 30 per cent.

TYPICAL OPERATION CHARACTERISTICS

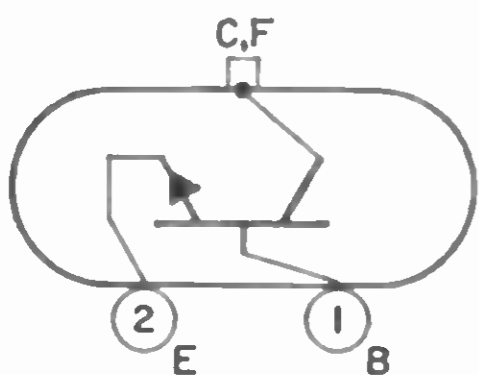


TYPICAL SMALL-SIGNAL OPERATION CHARACTERISTIC



TRANSISTOR

2N3583



Si n-p-n triple-diffused type used in high-speed-switching and linear-amplifier applications such as high-voltage operational amplifiers, high-voltage switches, switching regulators, converters, inverters, deflection and high-fidelity amplifiers in military, industrial and commercial equipment. JEDEC TO-66, Outline No.25.

See Mounting Hardware for desired mounting arrangement.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	250	V
Collector-to-Emitter Sustaining Voltage	$V_{CEO(sus)}$	175	V
Emitter-to-Base Voltage	V_{EBO}	6	V
Collector Current	I_C	2	A

MAXIMUM RATINGS (cont'd)

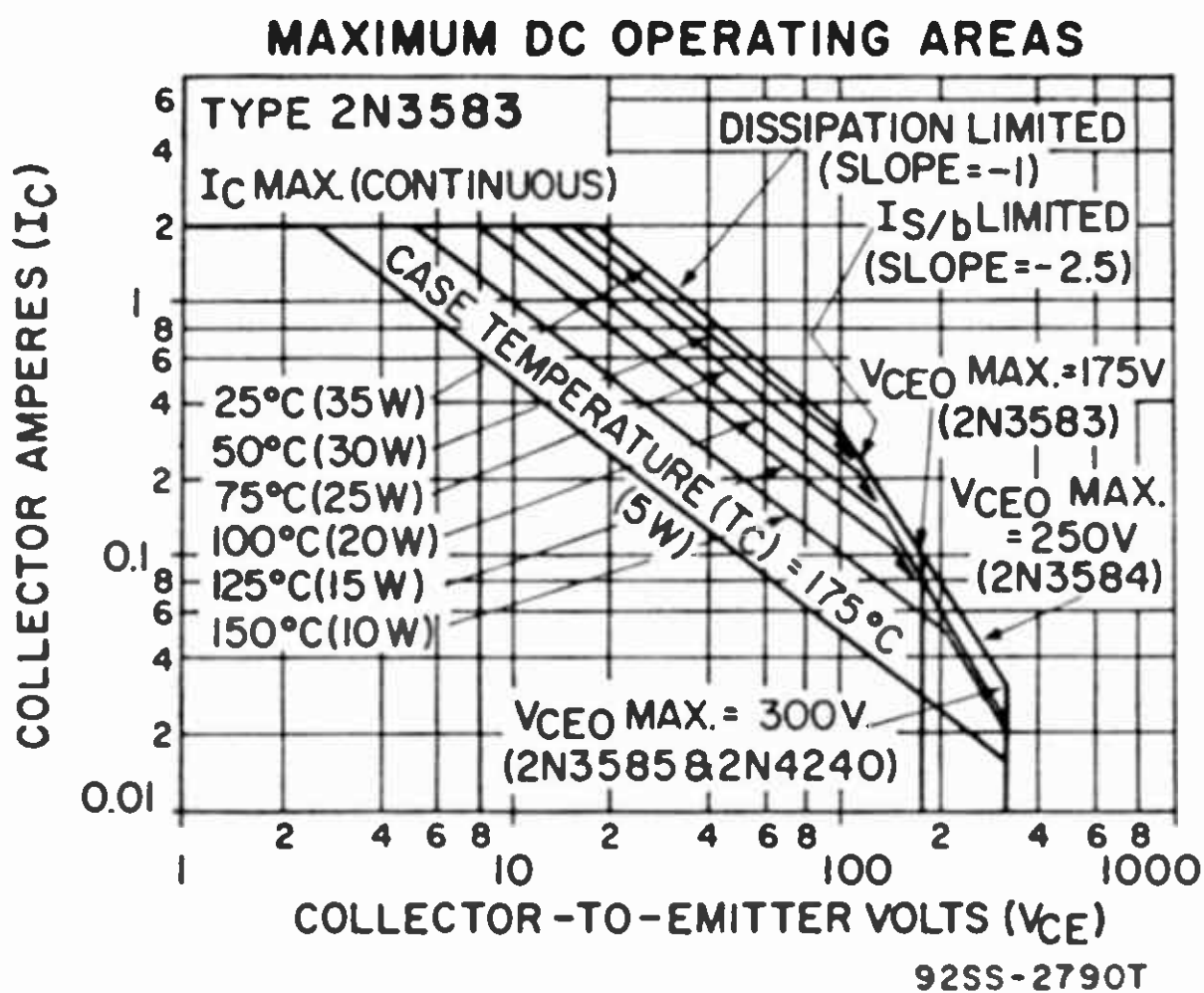
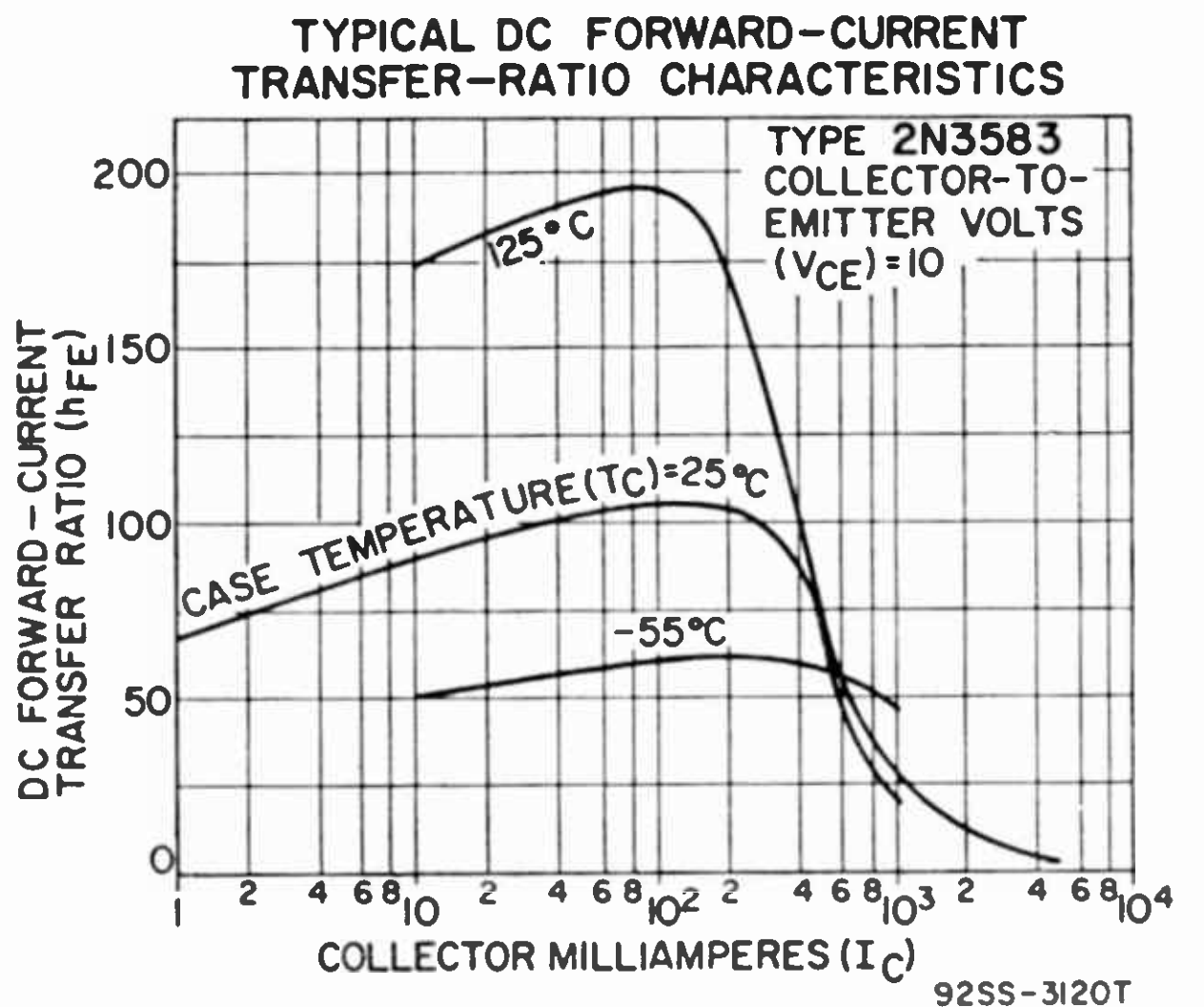
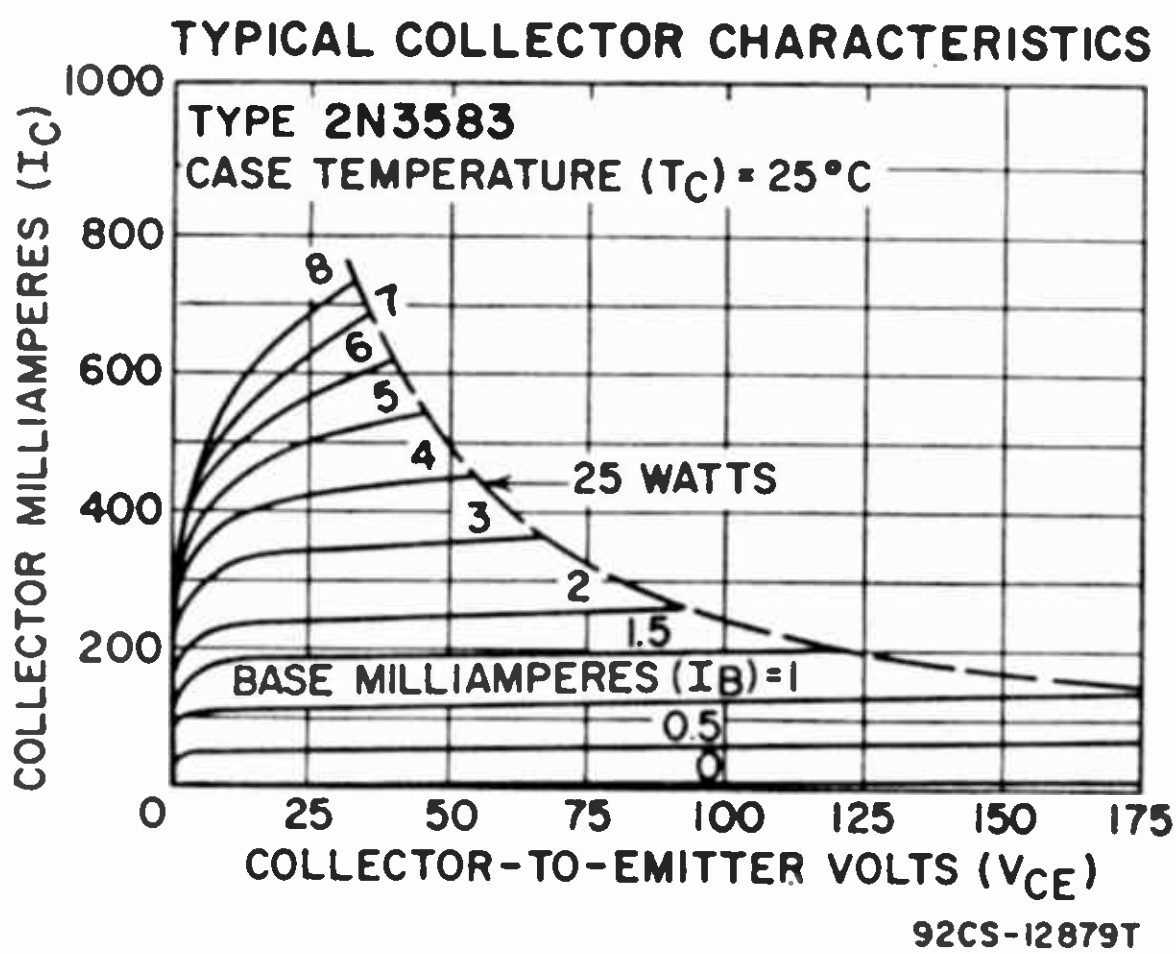
Peak Collector Current	I_C	5	A
Base Current	I_B	1	A
Transistor Dissipation	P_T	See Chart, Maximum DC Operating Areas	
Operating Temperature Range	$T_C(opr)$	-65 to 200	$^{\circ}C$
Pin-Soldering Temperature (10 s max)	T_P	255	$^{\circ}C$

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage:

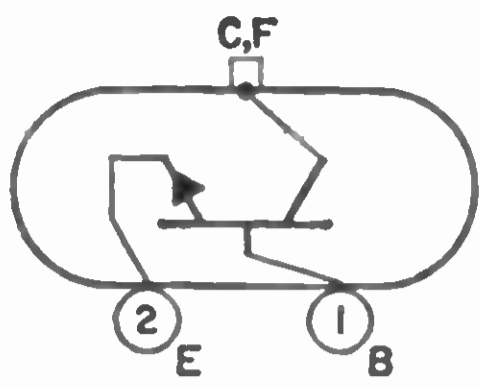
$I_C = 200$ mA, $I_B = 0$	$V_{CE0}(sus)$	175 min	V
$R_{BE} = 50 \Omega$, $I_C = 200$ mA	$V_{CER}(sus)$	250 min	V
Base-to-Emitter Voltage ($I_C = 1$ A, $V_{CE} = 10$ V)	V_{BE}	1.4 max	V
Collector-Cutoff Current:			
$V_{CE} = 150$ V, $I_B = 0$, $T_C = 25^{\circ}C$	I_{CEO}	10 max	mA
$V_{BE} = -1.5$ V, $V_{CE} = 225$ V, $T_C = 25^{\circ}C$	I_{CEV}	1 max	mA
$V_{BE} = -1.5$ V, $V_{CE} = 225$ V, $T_C = 150^{\circ}C$	I_{CEV}	3 max	mA
Emitter-Cutoff Current ($V_{EB} = 6$ V, $I_C = 0$)	I_{EBO}	5 max	mA
Static Forward-Current Transfer Ratio:			
$V_{CE} = 10$ V, $I_C = 100$ mA	h_{FE}	40 min	
$V_{CE} = 10$ V, $I_C = 1$ A	h_{FE}	10 min	
Small-Signal Forward-Current Transfer Ratio			
($V_{CE} = 10$ V, $I_C = 200$ mA, $f = 5$ MHz)	h_{fe}	3 min	
Second-Breakdown Collector Current (Base forward-biased from zero up, $V_{CE} = 100$ V)	$I_{s/b}$	350 min	mA
Second-Breakdown Energy (Base reverse-biased, $R_{BE} = 20 \Omega$, $L = 100 \mu H$, $V_{BE} = -4$ V)	$E_{s/b}$	50 min	μJ
Output Capacitance ($V_{CB} = 10$ V, $I_E = 0$, $f = 1$ MHz)	C_{obo}	120 max	pF
Thermal Resistance, Junction-to-Case ($I_C = 500$ mA)	θ_{J-C}	5* max	$^{\circ}C/W$
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	70 max	$^{\circ}C/W$

* This values does not apply to type 40374.



TRANSISTOR

2N3584



Si n-p-n triple-diffused type used in high-speed-switching and linear-amplifier applications such as high-voltage operational amplifiers, high-voltage switches, switching regulators, converters, inverters, deflection and high-fidelity amplifiers in military, industrial and commercial equipment. JEDEC TO-66, Outline No.25.

See Mounting Hardware for desired mounting arrangement. For Maximum DC Operating Areas Chart, refer to type 2N3583.

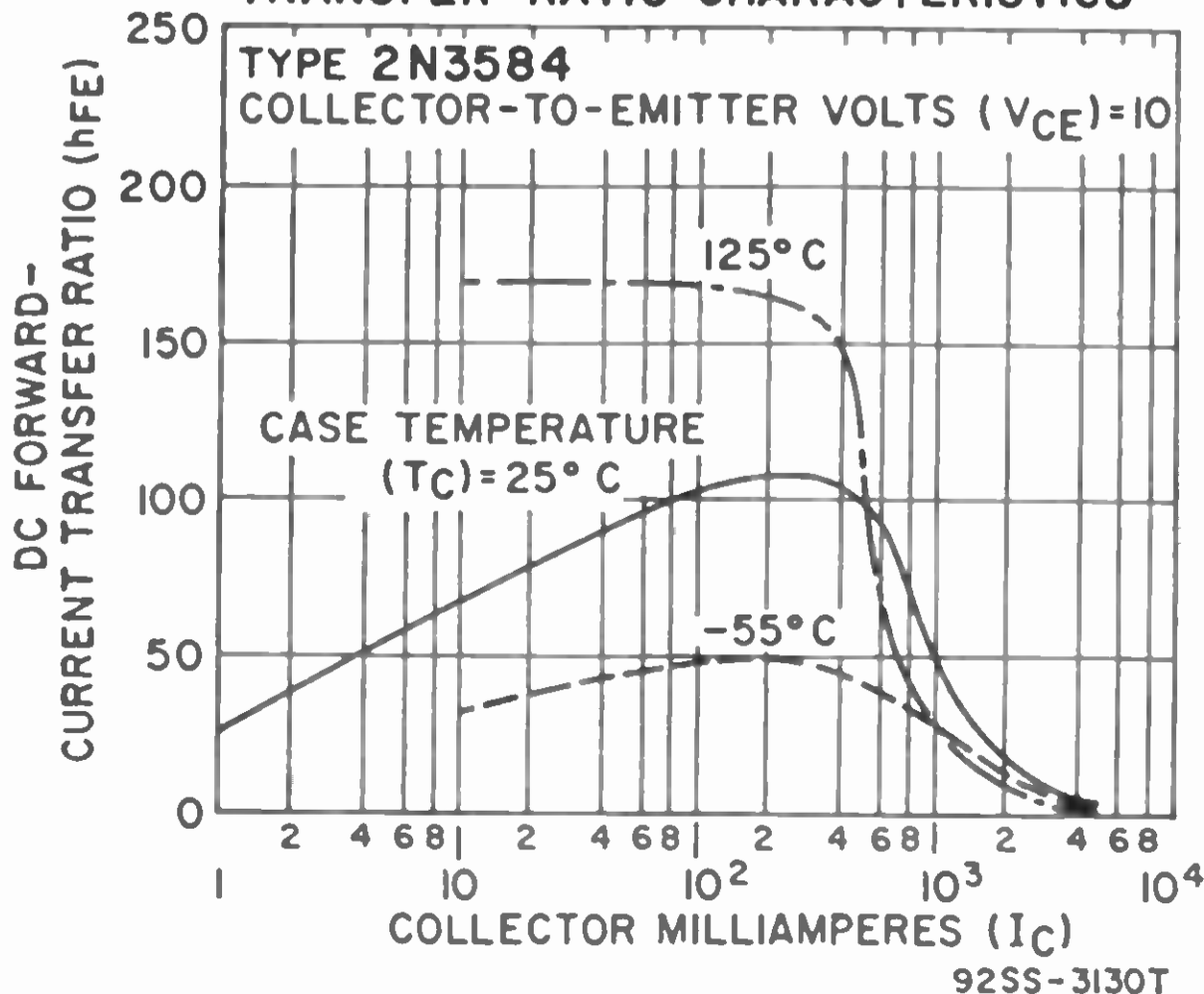
MAXIMUM RATINGS

Table with 4 columns: Parameter, Value, Unit, and Notes. Rows include Collector-to-Base Voltage (375 V), Collector-to-Emitter Sustaining Voltage (250 V), Emitter-to-Base Voltage (6 V), Collector Current (2 A), Peak Collector Current (5 A), Base Current (1 A), Transistor Dissipation (See Chart), Operating Temperature (-65 to 200 °C), and Pin-Soldering Temperature (255 °C).

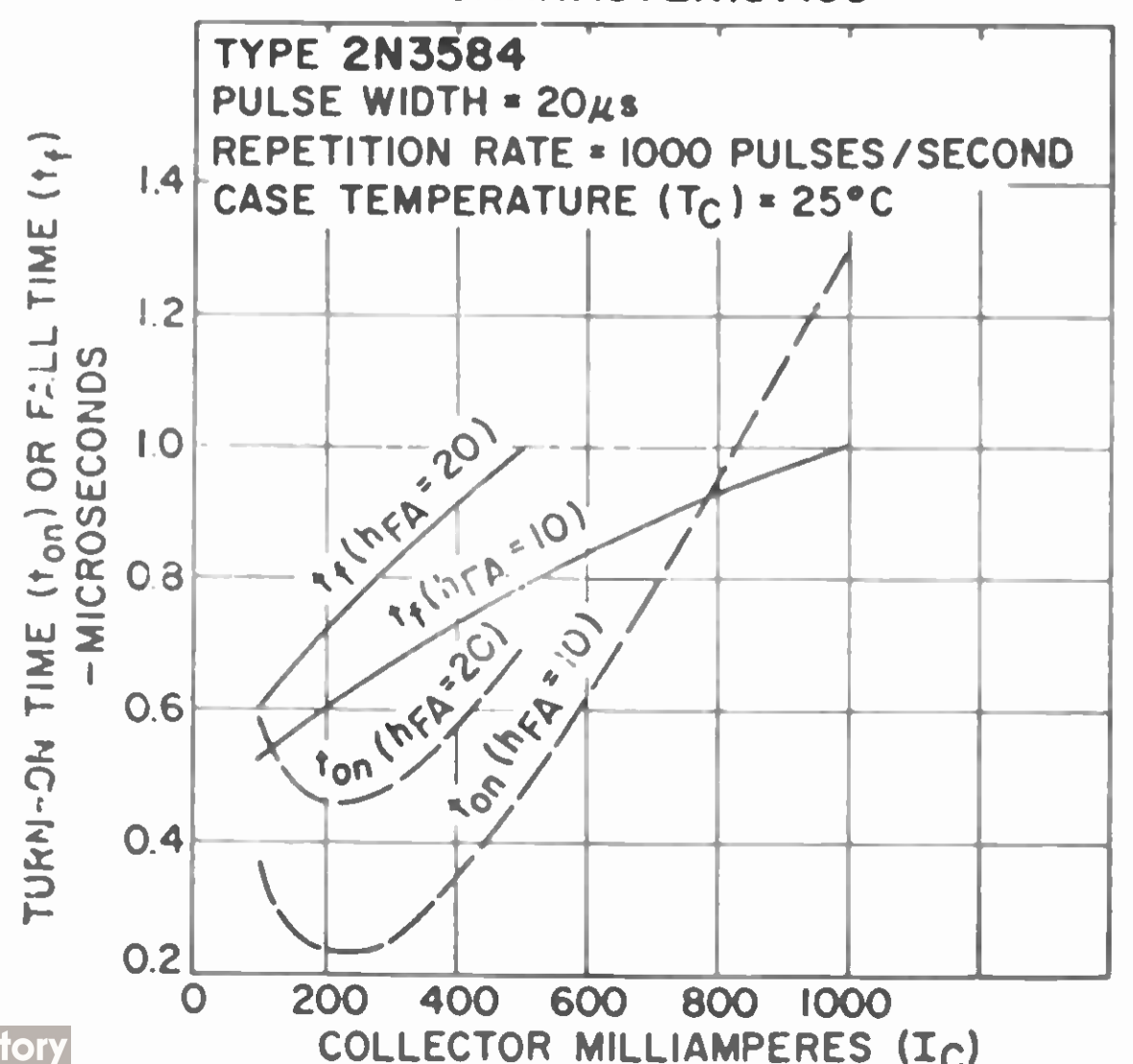
CHARACTERISTICS (At case temperature = 25°C)

Table with 4 columns: Characteristic, Test Conditions, Value, and Unit. Rows include Collector-to-Emitter Sustaining Voltage, Base-to-Emitter Voltage, Collector-to-Emitter Saturation Voltage, Collector-Cutoff Current, Emitter-Cutoff Current, Static Forward-Current Transfer Ratio, Small-Signal Forward-Current Transfer Ratio, Second-Breakdown Collector Current, Second-Breakdown Energy, Output Capacitance, Turn-On Time, and Storage Time.

TYPICAL DC FORWARD-CURRENT TRANSFER-RATIO CHARACTERISTICS



TYPICAL TURN-ON TIME AND FALL-TIME CHARACTERISTICS

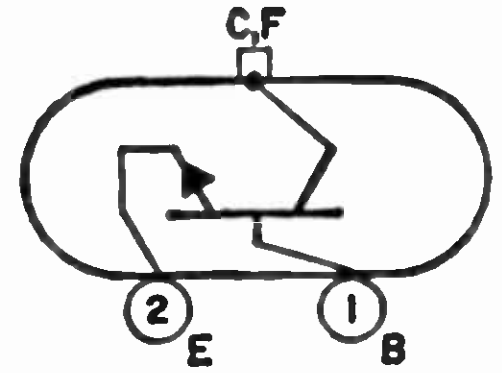


CHARACTERISTICS (cont'd)

Fall Time ($V_{CC} = 30\text{ V}, I_C = 1\text{ A}, I_B = 100\text{ mA}$) ...	t_f	3 max	μs
Thermal Resistance, Junction-to-Case ($I_C = 500\text{ mA}$)	θ_{J-C}	5 max	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient ($I_C = 500\text{ mA}$)	θ_{J-A}	70 max	$^{\circ}\text{C}/\text{W}$

2N3585 TRANSISTOR

Si n-p-n triple-diffused type used in high-speed-switching and linear-amplifier applications such as high-voltage operational amplifiers, high-voltage switches, switching regulators, converters, inverters, deflection and high-fidelity amplifiers in military, industrial and commercial equipment. JEDEC TO-66, Outline No.25.



See Mounting Hardware for desired mounting arrangement. This type is identical with type 2N3584 except for the following items:

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CB0}	500	V
Collector-to-Emitter Sustaining Voltage	$V_{CE0(sus)}$	300	V

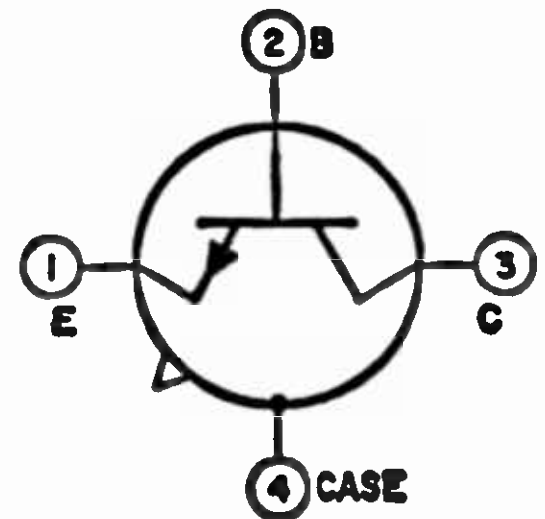
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage: $I_C = 200\text{ mA}, I_B = 0$	$V_{CE0(sus)}$	300 min	V
$R_{BE} = 50\ \Omega, I_C = 200\text{ mA}$	$V_{CER(sus)}$	400 min	V
Collector-Cutoff Current: ($V_{BE} = -1.5\text{ V}, V_{CE} = 400\text{ V}, T_C = 25^{\circ}\text{C}$)	I_{CEV}	1 max	mA
Turn-On Time, Saturated Switch ($V_{CC} = 30\text{ V}, I_C = 1\text{ A}, I_B = 100\text{ mA}$)	$t_d + t_r$	2* max	μs

* This value does not apply to type 2N4240.

2N3600 TRANSISTOR

Si n-p-n epitaxial planar type used in low-noise amplifier, oscillator, and converter applications at vhf frequencies in military, communications, and industrial equipment. JEDEC TO-72, Outline No.28.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CB0}	30	V
Collector-to-Emitter Voltage	V_{CE0}	15	V
Emitter-to-Base Voltage	V_{EB0}	3	V
Collector Current	I_C	Limited by power dissipation	
Transistor Dissipation:			
T_A up to 25°C	P_T	200	mW
T_C up to 25°C (with heat sink)	P_T	300	mW
T_A or T_C (with heat sink) above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 200	$^{\circ}\text{C}$
Storage	T_{STG}	-65 to 200	$^{\circ}\text{C}$
Lead-Soldering Temperature (60 s max)	T_L	300	$^{\circ}\text{C}$

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = 0.001\text{ mA}, I_E = 0$)	$V_{(BR)CBO}$	30 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.01\text{ mA}, I_C = 0$)	$V_{(BR)EBO}$	3 min	V
Collector-to-Emitter Sustaining Voltage ($I_C = 3\text{ mA}, I_B = 0$)	$V_{(BR)CE0(sus)}$	15 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 10\text{ mA}, I_B = 1\text{ mA}$)	$V_{CE(sat)}$	0.4 max	V
Base-to-Emitter Saturation Voltage ($I_C = 10\text{ mA}, I_B = 1\text{ mA}$)	$V_{BE(sat)}$	1 max	V
Collector-Cutoff Current:			
$V_{CB} = 15\text{ V}, I_E = 0, T_A = 25^{\circ}\text{C}$	I_{CBO}	0.01 max	μA
$V_{CB} = 15\text{ V}, I_E = 0, T_A = 150^{\circ}\text{C}$	I_{CBO}	1 max	μA

CHARACTERISTICS (cont'd)

Static Forward-Current Transfer Ratio ($V_{CE} = 1$ V, $I_C = 3$ mA)	h_{FE}	20 to 150 Δ	
Small-Signal Forward-Current Transfer Ratio:* $V_{CE} = 6$ V, $I_C = 5$ mA, $f = 100$ MHz	h_{fe}	8.5 to 15 Δ	
$V_{CE} = 6$ V, $I_C = 2$ mA, $f = 1$ kHz	h_{re}	40 to 200 Δ	
Input Capacitance† ($V_{EB} = 0.5$ V, $I_C = 0$, $f = 0.1$ to 1 MHz)	C_{ibo}	1.4	pF
Output Capacitance† ($V_{CB} = 10$ V, $I_E = 0$, $f = 0.1$ to 1 MHz)	C_{obo}	1.7 max	pF
Collector-to-Base Feedback Capacitance \blacksquare ($V_{CB} = 10$ V, $I_E = 0$, $f = 0.1$ to 1 MHz)	C_{cb}	1 max Δ	pF
Collector-to-Base Time Constant* ($V_{CB} = 6$ V, $I_C = 5$ mA, $f = 31.9$ MHz)	$r_{b'c}$	4 to 15	ps
Small-Signal Power Gain, Amplifier Circuit, Neutralized* ($V_{CE} = 6$ V, $I_C = 5$ mA, $f = 200$ MHz)	G_{pe}	17 to 24 Δ	dB
Power Output, Oscillator Circuit† ($V_{CB} = 10$ V, $I_E = 12$ mA, $f = 500$ MHz)	P_{oe}	20 min	mW
Noise Figure:* $V_{CE} = 6$ V, $I_C = 1.5$ mA, $f = 200$ MHz	NF	4.5 max Δ	dB
$V_{CE} = 6$ V, $I_C = 1$ mA, $f = 60$ MHz	NF	3	dB

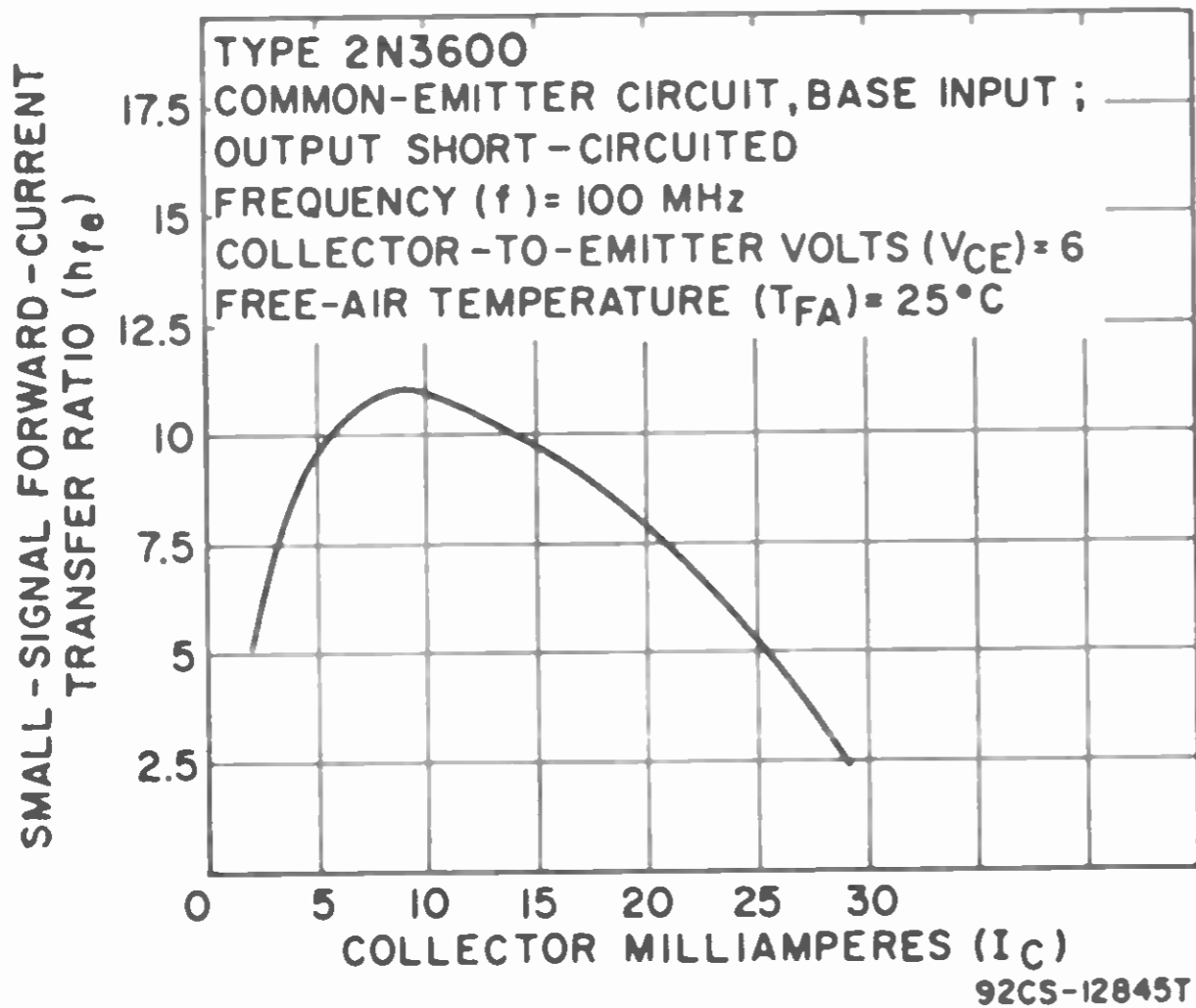
* Lead 4 (case) grounded.

† Lead 4 (case) floating.

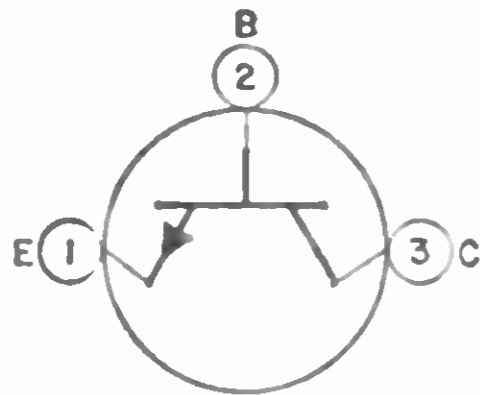
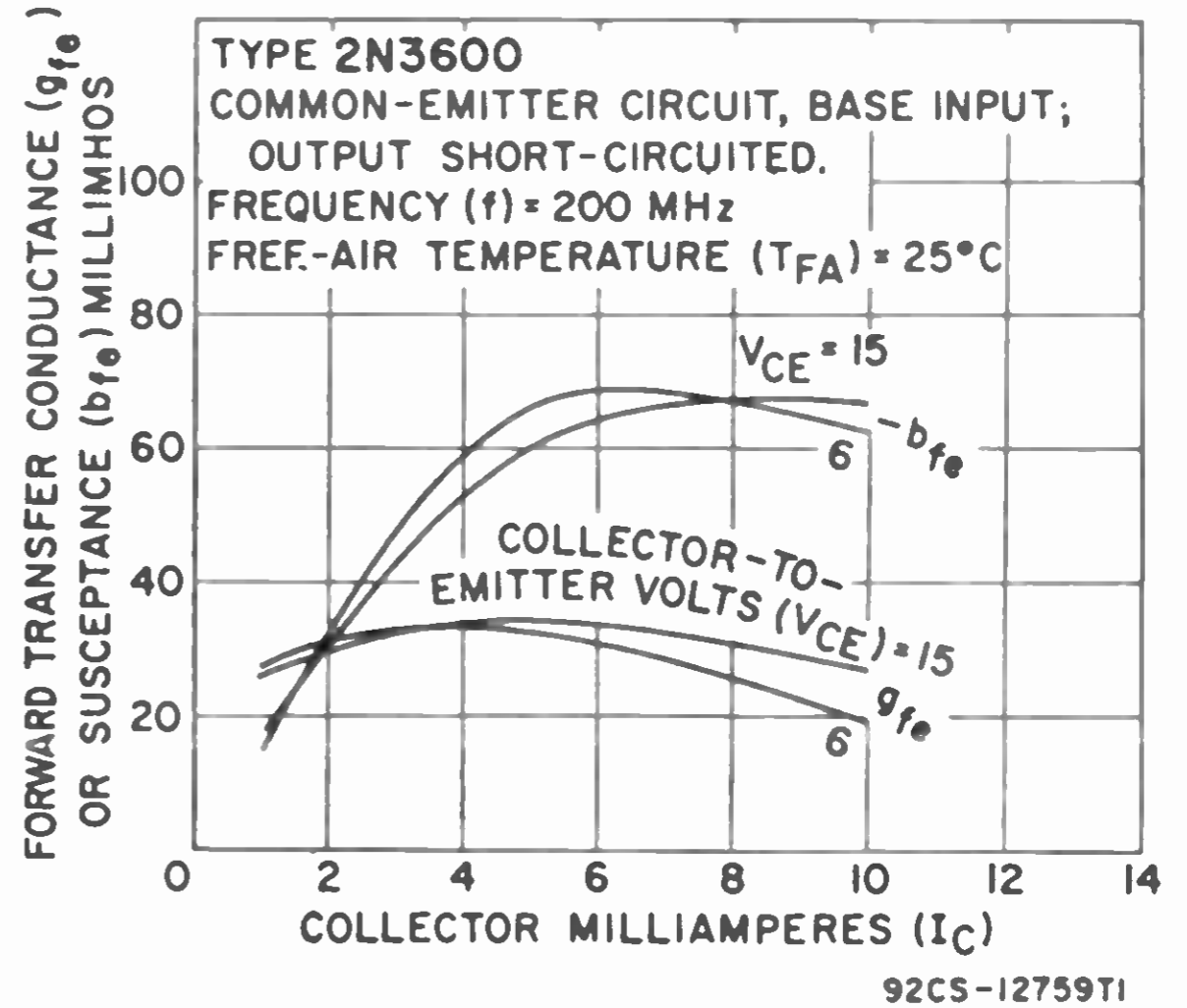
Δ This value does not apply to type 2N918.

\blacksquare Three-terminal measurement of the collector-to-base capacitance with the case and emitter leads connected to the guard terminal.

TYPICAL SMALL-SIGNAL FORWARD-CURRENT TRANSFER-RATIO CHARACTERISTIC



TYPICAL FORWARD TRANSFER CONDUCTANCE AND SUSCEPTANCE CHARACTERISTICS



TRANSISTOR

2N3632

Si n-p-n "overlay" epitaxial planar type used in class A, B, and C amplifiers, frequency multipliers, or oscillators in vhf-uhf applications for industrial and military communications. JEDEC TO-60, Outline No.23. See Mounting Hardware for desired mounting arrangement.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	65	V
Collector-to-Emitter Voltage: $V_{BE} = -1.5$ V	V_{CEV}	65	V
Base open	V_{CEO}	40	V
Emitter-to-Base Voltage	V_{EBO}	4	V
Collector Current	I_C	3	A
Peak Collector Current	ic	1	A
Transistor Dissipation: T_c up to 25°C	P_T	23	W
T_c above 25°C	P_T	See curve page 300	
Temperature Range: Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	230	°C

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Base Breakdown Voltage ($I_C = 0.5$ mA, $I_E = 0$)	$V_{(BR)CBO}$	65 min	V
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CHARACTERISTICS (cont'd)

Collector-to-Emitter Breakdown Voltage:

$I_C = 0$ to 0.2 A, $I_B = 0$, pulsed through an inductor

$L = 25$ mH, $df = 50\%$

$V_{(BR)CEO}$	40 min	V
---------------	--------	---

$I_C = 0$ to 0.2 A, $V_{BE} = -1.5$ V, pulsed

through an inductor $L = 25$ mH, $df = 50\%$...

$V_{(BR)CEV}$	65 min	V
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Emitter-to-Base Breakdown Voltage

($I_E = 0.25$ mA, $I_C = 0$)

$V_{(BR)EBO}$	4 min	V
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Collector-to-Emitter Saturation Voltage

($I_C = 0.5$ A, $I_B = 0.1$ A)

$V_{CE(sat)}$	1 max	V
---------------	-------	---

Collector-Cutoff Current ($V_{CE} = 30$ V, $I_B = 0$)

I_{CEO}	0.25 max	mA
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Collector-to-Case

C_c	6 max	pF
-------	-------	----

Gain-Bandwidth Product ($V_{CE} = 28$ V, $I_C = 150$ mA)

f_T	400	MHz
-------	-----	-----

Output Capacitance ($V_{CB} = 30$ V, $I_E = 0$,

$f = 1$ MHz)

C_{obo}	20 max	pF
-----------	--------	----

RF Power Output, Unneutralized:

$V_{CC} = 28$ V, $P_{IE} = 3.5$ W, R_G and $R_L = 50$ Ω ,

$f = 175$ MHz

P_{OE}	13.5* min	W
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$V_{CC} = 28$ V, $P_{IE} = 3$ W, R_G and $R_L = 50$ Ω ,

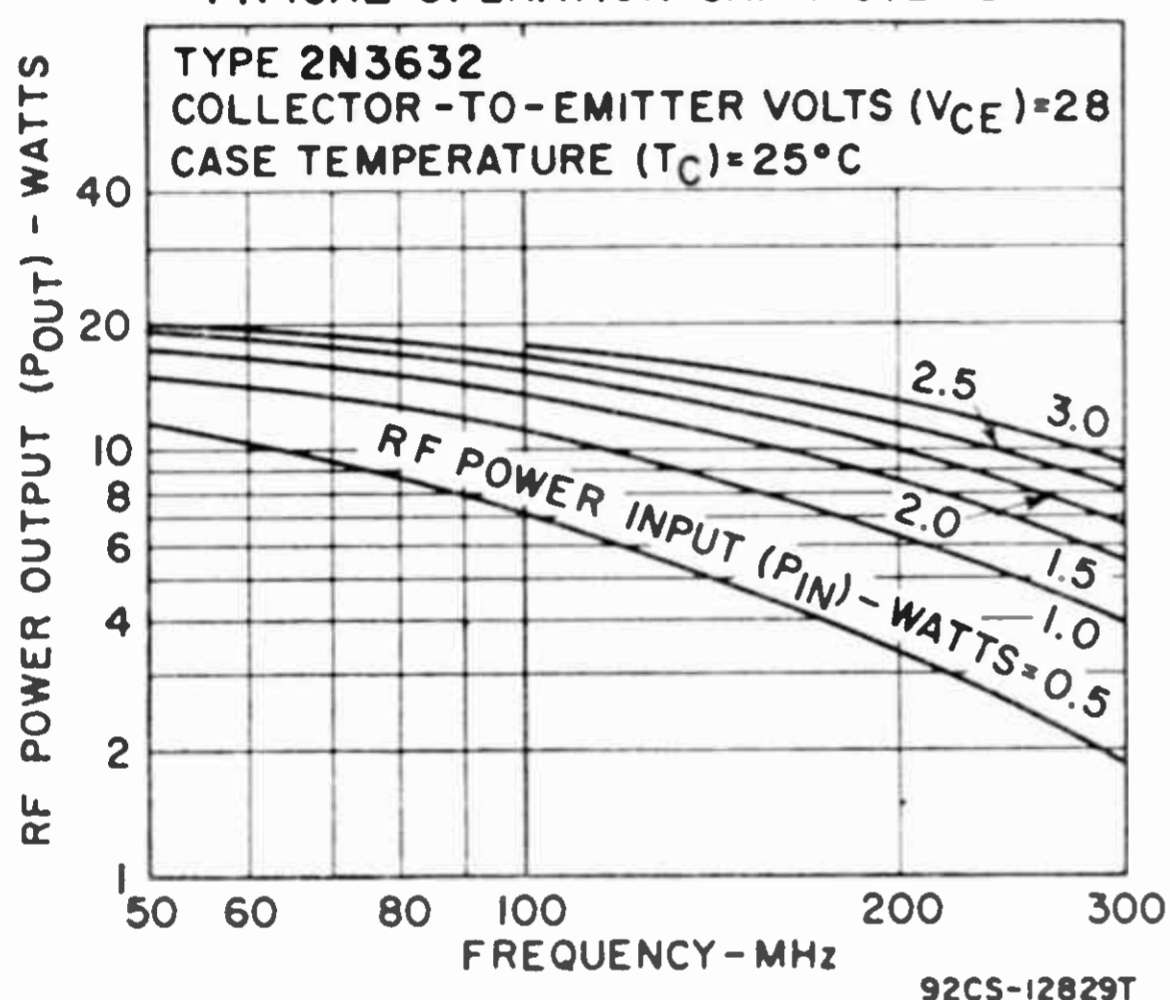
$f = 260$ MHz

P_{OE}	10†	W
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* For conditions given, minimum efficiency = 70 per cent.

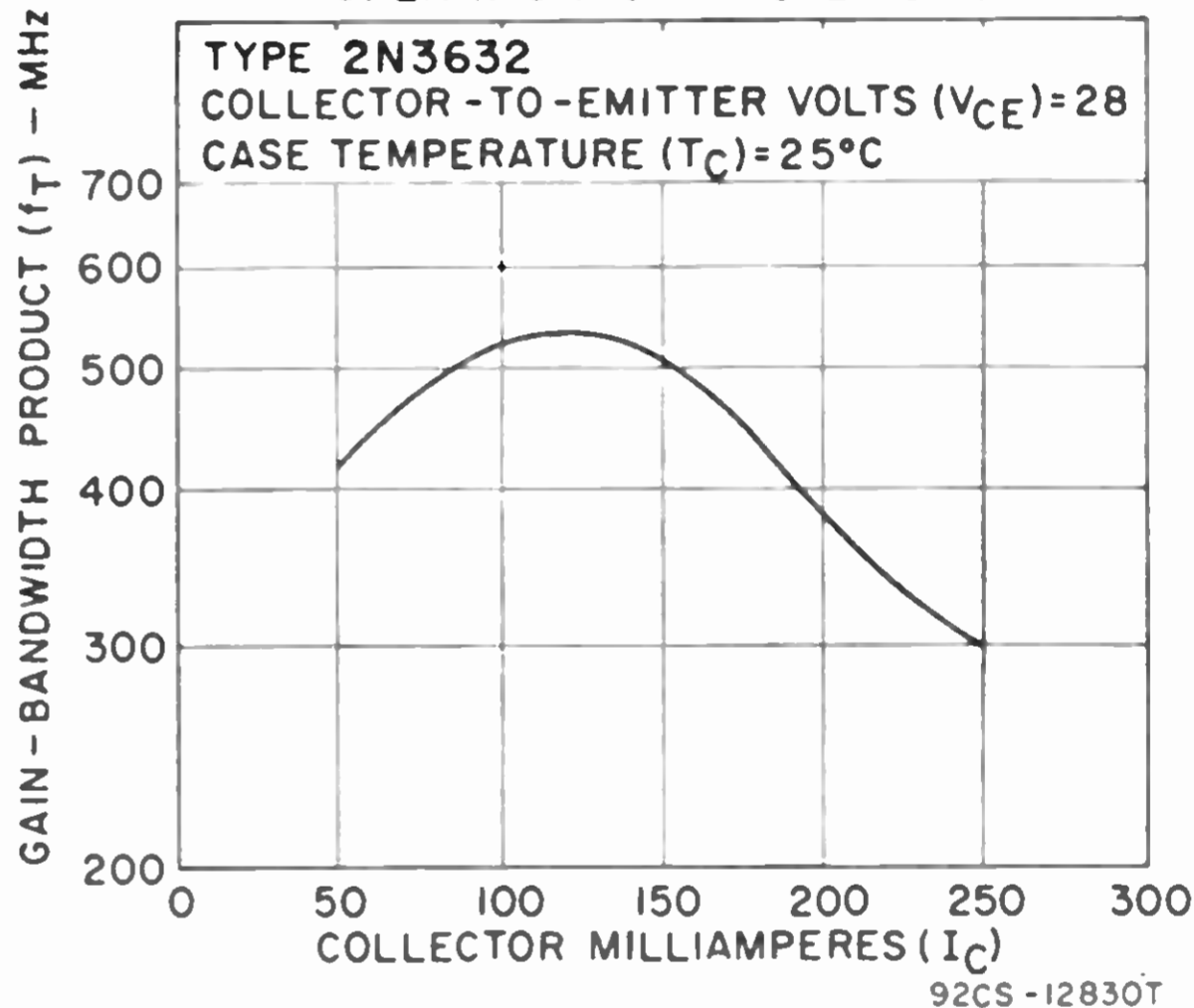
† For conditions given, minimum efficiency = 60 per cent.

TYPICAL OPERATION CHARACTERISTICS



92CS-12829T

TYPICAL SMALL-SIGNAL OPERATION CHARACTERISTIC

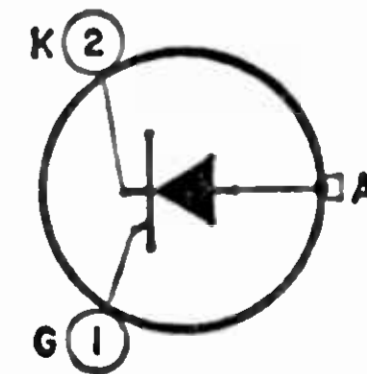


92CS-12830T

2N3668-
2N3670

SILICON
CONTROLLED RECTIFIERS

Si all-diffused three-junction types for use in power-control and power-switching applications. JEDEC TO-3, Outline No.2. See Mounting Hardware for desired mounting arrangement.



MAXIMUM RATINGS (For sinusoidal ac supply voltage at $f = 50$ to 400 Hz with resistive or inductive load)

	2N3668	2N3669	2N3670	
V_{RSOM}	150	330	660	V
V_{RRM}	100	200	400	V
V_{DRM}	600	600	600	V
$I_{T(AV)}$ (conduction angle = 180°, $T_C = 80^\circ C$)	8			A
$I_{T(RMS)}$	12.5			A
I_{TSM} (1 cycle of principle voltage)	200			A
Critical di/dt	200			A/ μs
$[I_{TSM}]^{2t}$ (1 to 8.3 ms)	165			A ² s
P_{GM} (peak, forward, or reverse for 10 μs)	40			W
$P_{G(AV)}$	0.5			W

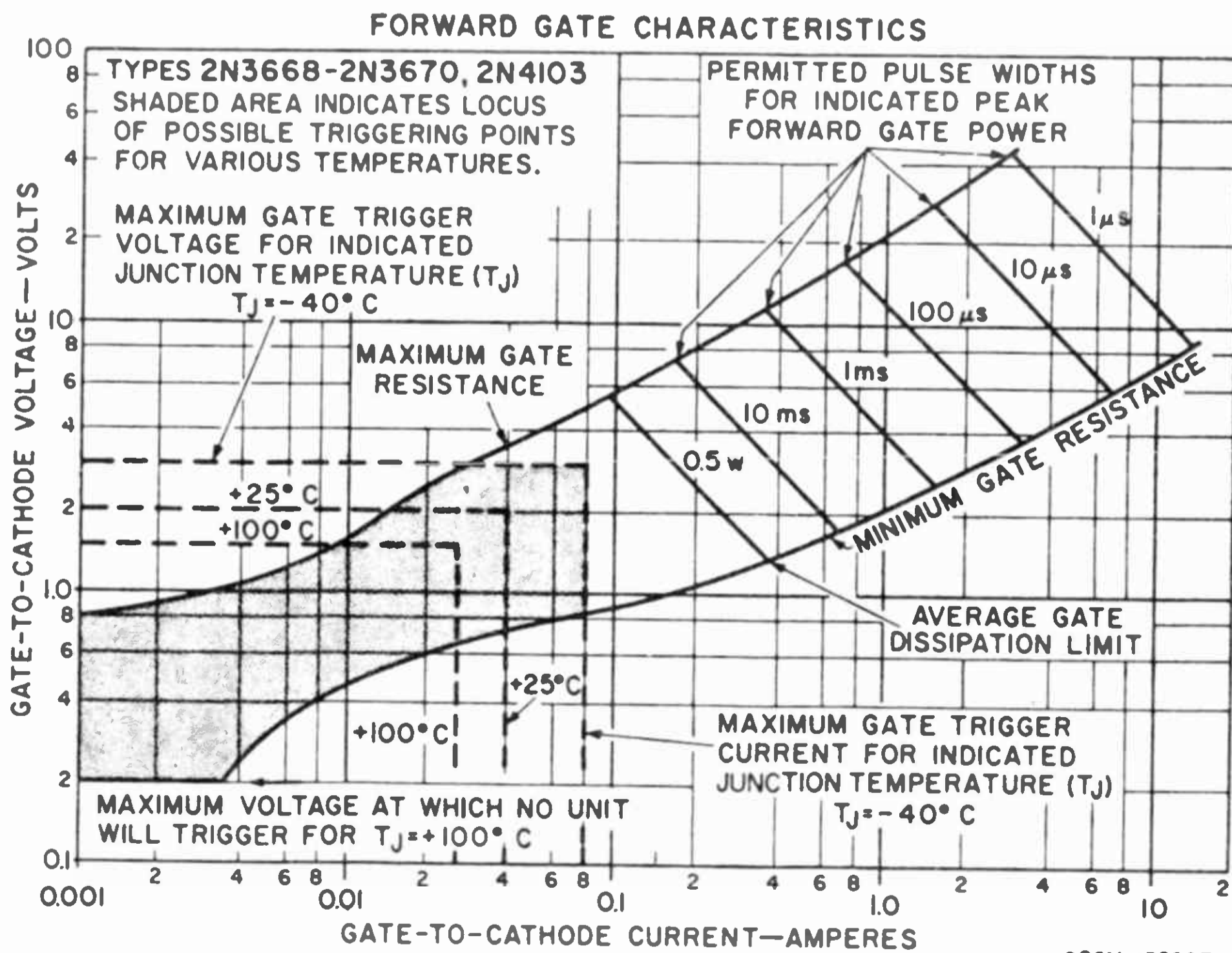
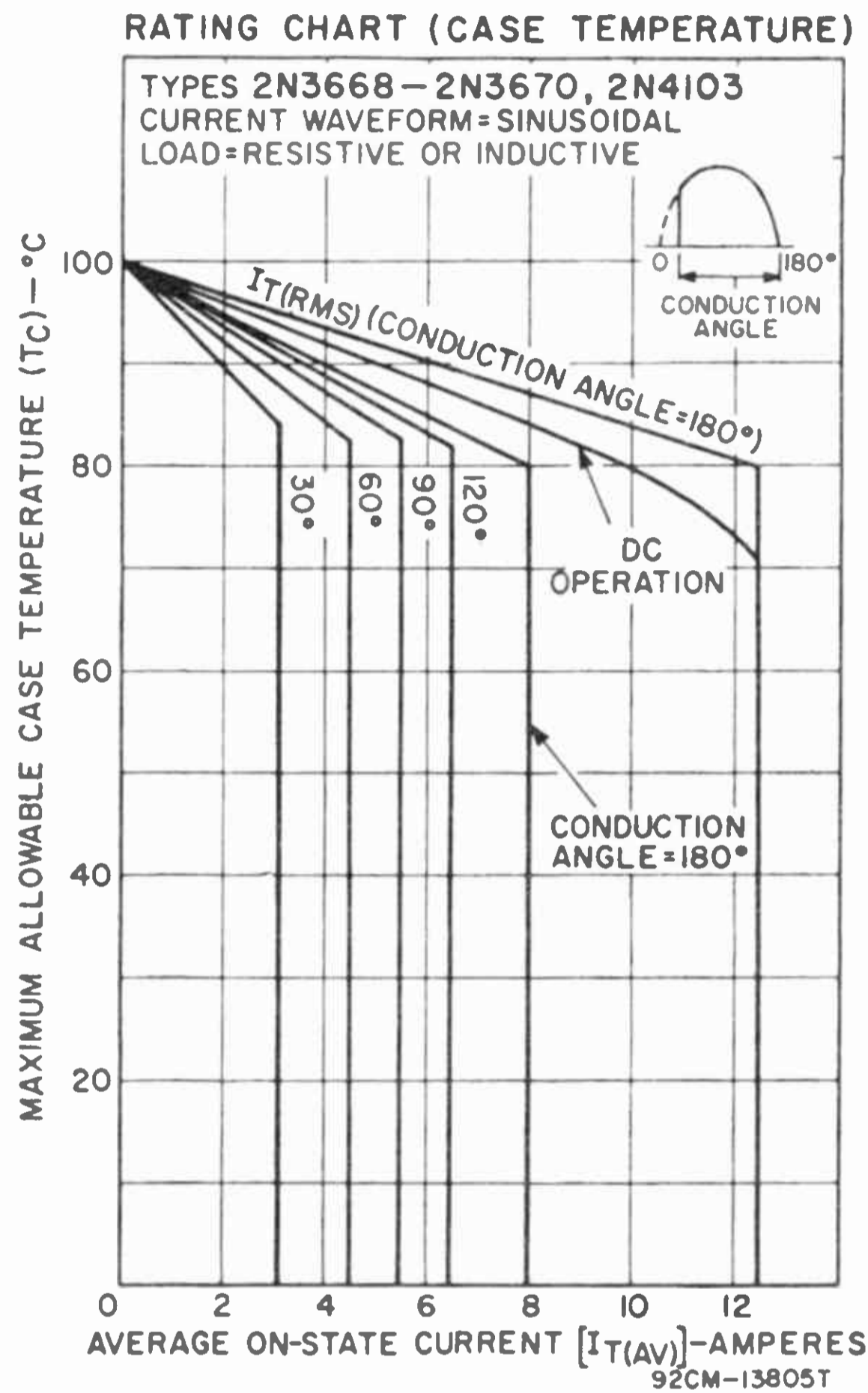
MAXIMUM RATINGS (cont'd)

2N3668 2N3669 2N3670

T_{stg} _____ -40 to 125 _____ °C
 T_c _____ -40 to 100 _____ °C

CHARACTERISTICS (At maximum electrical rating at $T_c = 25^\circ C$)

$V_{F(B0)0}$ ($T_c = 100^\circ C$) 100 min 200 min 400 min V
 0.2 typ 0.25 typ 0.3 typ mA

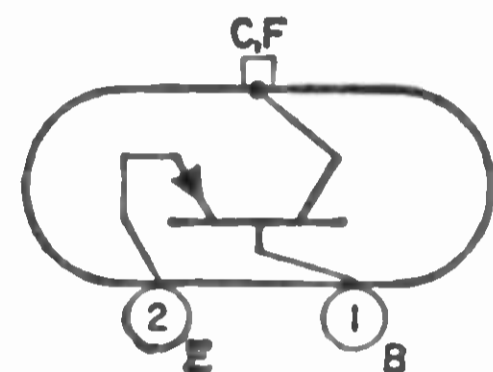


CHARACTERISTICS (cont'd)

	2N3668	2N3669	2N3670	
I_{DOM} ($T_C = 100^\circ C, V_{D0} = V_{F(B0)0}$ min value)	2 max	2.5 max	3 max	mA
I_{RR0M} ($V_{R0} = V_{RR0M}$)	0.05 typ	0.1 typ	0.2 typ	mA
V_T (on-state current = 25 A)	1 max			1.25 max
I_{GT}	1.5 typ; 1.8 max			V
V_{GT}	1 min, 20 typ, 40 max			mA (dc)
i_{HO}	1.5 typ; 2 max			V (dc)
Critical dv/dt ($V_D = V_{F(B0)0}$ min value, exponential rise, $T_C = 100^\circ C$)	0.5 to 50			mA
	10 min; 100 typ			V/ μs
	2N3668	2N3669	2N3670	
t_{gt} ($V_D = V_{F(B0)0}$ min value, $i_T = 8$ A, $I_{GT} = 200$ mA, $t_r = 0.1 \mu s$)	0.75 min; 1.25 typ			μs
t_4 ($i_T = 8$ A, 50 μs pulse width, $dv_D/dt = 20$ V/ μs , $di_R/dt = 30$ A/ μs , $I_{GT} = 200$ mA, $T_C = 80^\circ C$)	20 typ; 50 max			μs
θ_{J-C}	1.7 max			$^\circ C/W$

2N3730 POWER TRANSISTOR

Ge p-n-p diffused-collector graded-base type used in 114-degree 18-kV TV deflection systems as a vertical-deflection output amplifier. This type, together with types 2N3731 (horizontal output), 2N3732 (horizontal driver), and 1N4785 (damper) make up a complete transistor/damper-diode complement. JEDEC TO-3, Outline No.2.



MAXIMUM RATINGS

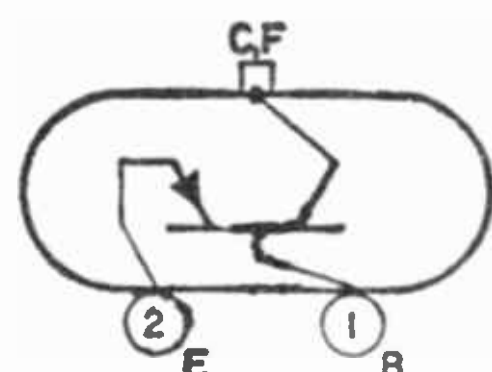
Collector-to-Base Voltage:			
Peak	V_{CB0}	-200	V
Continuous	V_{CB0}	-60	V
Emitter-to-Base Voltage	V_{EB0}	-0.5	V
Collector Current	I_C	-3	A
Base Current	I_B	± 0.5	A
Transistor Dissipation:			
T_{MF} up to $55^\circ C$	P_T	10	W
T_{MF} above $55^\circ C$	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 85	$^\circ C$
Storage	T_{STG}	-65 to 85	$^\circ C$
Pin-Soldering Temperature (10 s max)	T_P	230	$^\circ C$

CHARACTERISTICS

Collector-to-Emitter Breakdown Voltage ($I_C = 5$ mA, $V_{EB} = 0$)	$V_{(BR)CES}$	-200 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -100$ mA, $I_C = 0$)	$V_{(BR)EBO}$	-0.5 min	V
Collector-to-Emitter Saturation Voltage:			
$I_C = -0.7$ A, $I_B = -0.02$ A	$V_{CE(sat)}$	-2 max	V
$I_C = -0.05$ A, $I_B = -0.005$ A	$V_{CE(sat)}$	-1 max	V
Base-to-Emitter Voltage ($I_C = -0.7$ A, $I_B = -0.02$ A)	V_{BE}	0.5 typ	V
Collector-Cutoff Current ($V_{CB} = -10$ V, $I_E = 0$)	I_{CB0}	-200 max	$^\circ C/W$
Thermal Resistance, Junction-to-Case	θ_{J-C}	1.5 max	μA

2N3731 POWER TRANSISTOR

Ge p-n-p diffused-collector graded-base type used in 114-degree 18-kV TV deflection systems as a horizontal output amplifier. This type, together with types 2N3730 (vertical output), 2N3732 (horizontal driver), and 1N4785 (damper) make up a complete transistor/damper-diode complement. JEDEC TO-3, Outline No.2.



MAXIMUM RATINGS

Collector-to-Base Voltage:		
Peak	VCBO	-320 V
Continuous	VCBO	-60 V
Emitter-to-Base Voltage	VEBO	-2 V
Collector Current	IC	-10 A
Base Current	IB	+4, -1 A
Transistor Dissipation:		
T _{MF} up to 55°C	P _T	5 W
T _{MF} above 55°C	P _T	See curve page 300
Temperature Range:		
Operating (Junction)	T _J (opr)	-65 to 85 °C
Storage	T _{STG}	-65 to 85 °C
Pin-Soldering Temperature (10 s max)	T _P	230 °C

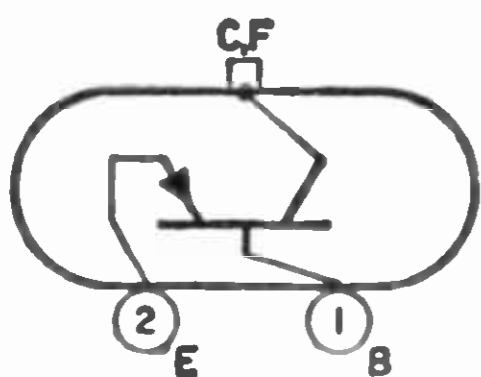
CHARACTERISTICS

Collector-to-Emitter Breakdown Voltage (I _C = -0.025 A, V _{EB} = 0)	V _{(BR)CES}	-320 min	V
Emitter-to-Base Breakdown Voltage (I _E = 100 mA, I _C = 0)	V _{(BR)EBO}	-2 min	V
Collector-to-Emitter Saturation Voltage:			
I _C = -6 A, I _B = -0.4 A	V _{CE(sat)}	-1.5 max	V
I _C = -3 A, I _B = -0.2 A	V _{CE(sat)}	-1.5 [▲] max	V
Base-to-Emitter Voltage (I _C = -6 A, I _B = -0.4 A)			
	V _{BE}	-0.8	μA
Collector-Cutoff Current (V _{CB} = -10 V, I _E = 0)	ICBO	-200 max	
Turn-off Time	t _s + t _f	1.2 max	μs
Thermal Resistance, Junction-to-Case	θ _{J-C}	1.5 max	°C/W

▲ This value does not apply to type 40439.

POWER TRANSISTOR

2N3732



Ge p-n-p diffused-collector graded-base type used in 114-degree 18-kV TV deflection systems as a horizontal driver. This type, together with types 2N3730 (vertical output), 2N3731 (horizontal output), and 1N4785 (damper) make up a complete transistor/damper-diode complement. JEDEC TO-3, Outline No.2.

MAXIMUM RATINGS

Collector-to-Base Voltage:		
Peak	VCBO	-100 V
Continuous	VCBO	-60 V
Emitter-to-Base Voltage	VEBO	-0.5 V
Collector Current	IC	-3 A
Base Current	IB	±0.5 A
Transistor Dissipation:		
T _{MF} up to 55°C	P _T	3 W
T _{MF} above 55°C	P _T	See curve page 300
Temperature Range:		
Operating (Junction)	T _J (opr)	-65 to 85 °C
Storage	T _{STG}	-65 to 85 °C
Pin-Soldering Temperature (10 s max)	T _P	230 °C

CHARACTERISTICS

Collector-to-Emitter Breakdown Voltage (I _C = 5 A, V _{EB} = 0)	V _{(BR)CES}	-100 min	V
Emitter-to-Base Breakdown Voltage (I _E = -100 mA, I _C = 0)	V _{(BR)EBO}	-0.5 min	V
Collector-to-Emitter Saturation Voltage (I _C = -0.7 A, I _B = -0.02 A)	V _{CE(sat)}	-2 max	V
Base-to-Emitter Voltage (I _C = -0.7 A, I _B = -0.02 A)			
	V _{BE}	0.5	V
Collector-Cutoff Current (V _{CB} = -10 V, I _E = 0)	ICBO	-200 max	μA
Thermal Resistance, Junction-to-Case	θ _{J-C}	1.5 max	°C/W

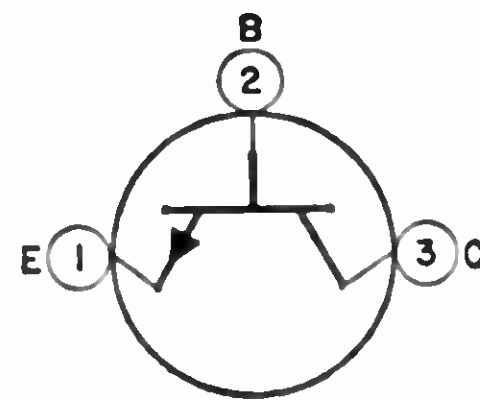
TYPICAL OPERATION IN HORIZONTAL-DEFLECTION AND HIGH-VOLTAGE CIRCUIT

DC Supply Voltage	45	V
Average Supply Current	0.55	A
Input Power:		
Oscillator and driver circuits	1.5	W
Output Circuit:		
At beam current = 0	18	W
At beam current = 200 μA	22	W
DC High-Voltage Output:		
At beam current = 0	18	kV
At beam current = 200 μA	17	kV
Yoke Current (peak-to-peak)	10	A
Peak Yoke Energy	2.5	mJ
Retrace Time	11.5	μs

2N3733

TRANSISTOR

Si n-p-n "overlay" epitaxial planar type used in large-signal, high-power vhf-uhf applications in military and industrial communications equipment. Intended for class A, B, C amplifier, frequency-multiplier, or oscillator service. JEDEC TO-60, Outline No.23. See **Mounting Hardware** for desired mounting arrangement.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	65	V
Collector-to-Emitter Voltage:			
$V_{BE} = -1.5\text{ V}$	V_{CEV}	65	V
Base open	V_{CEO}	40	V
Emitter-to-Base Voltage	V_{EBO}	4	V
Peak Collector Current	i_C	3	A
Transistor Dissipation:			
T_C up to 25°C	P_T	23	W
T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Pin-Soldering Temperature (10 s max)	T_P	230	°C

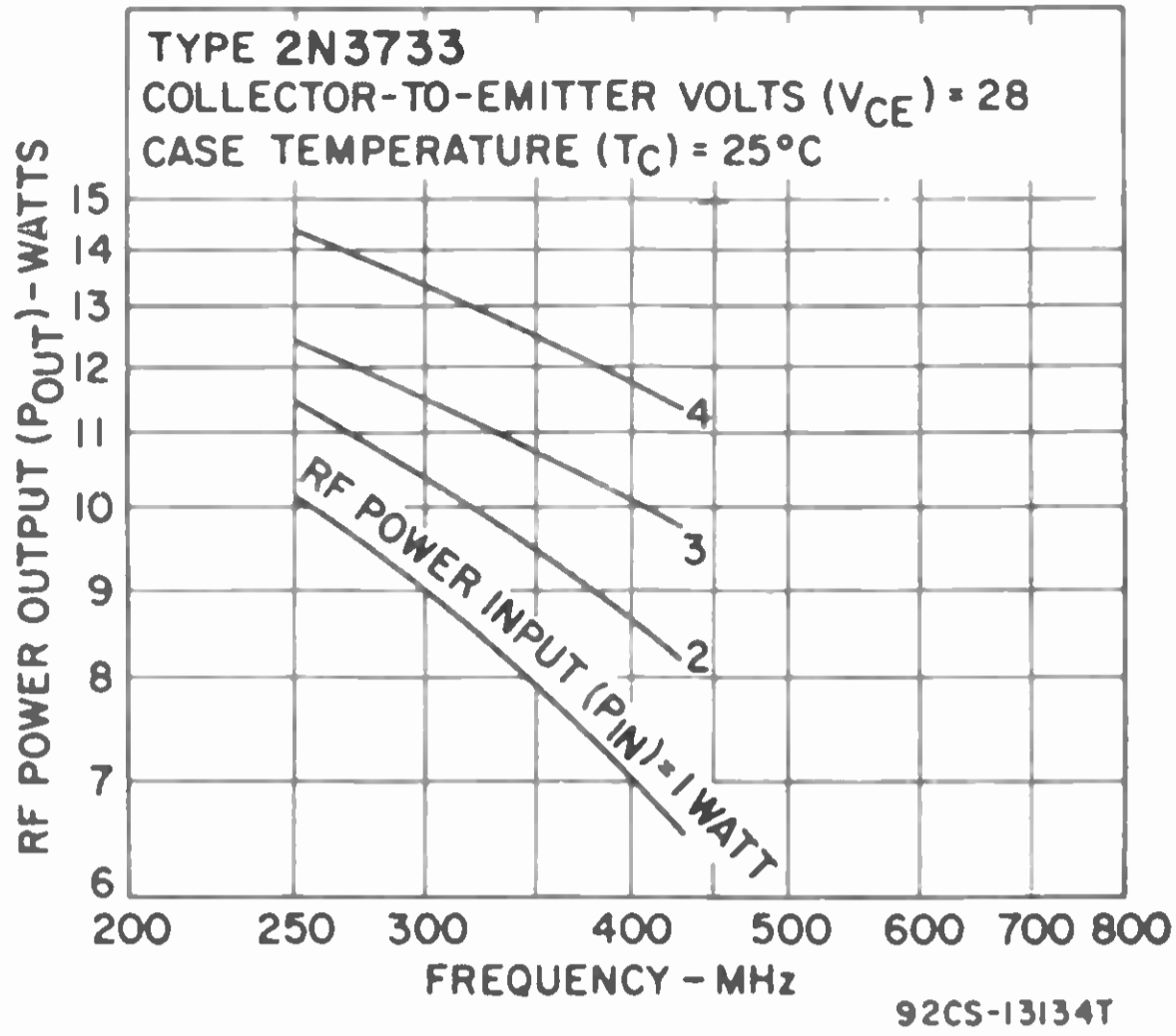
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Base Breakdown Voltage ($I_C = 0.5\text{ mA}$, $I_E = 0$)	$V_{(BR)CBO}$	65 min	V
Collector-to-Emitter Breakdown Voltage:			
$I_C = 0$ to 200 mA, $V_{BE} = -1.5\text{ V}$, pulsed through an inductor $L = 25\text{ mH}$, $df = 50\%$	$V_{(BR)CEV}$	65 min	V
$I_C = 0$ to 200 mA, $I_B = 0$, pulsed through an inductor $L = 25\text{ mH}$, $df = 50\%$	$V_{(BR)CEO}$	40 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.25\text{ mA}$, $I_C = 0$)	$V_{(BR)EBO}$	4 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 0.5\text{ A}$, $I_B = 100\text{ mA}$)	$V_{CE(sat)}$	1 max	V
Collector-Cutoff Current ($V_{CE} = 30\text{ V}$, $I_B = 0$)	I_{CEO}	0.25 max	mA
Intrinsic Base-Spreading Resistance ($V_{CE} = 28\text{ V}$, $I_C = 250\text{ mA}$, $f = 200\text{ MHz}$)	r_{bb}'	6.5	Ω
Gain-Bandwidth Product ($V_{CE} = 28\text{ V}$, $I_C = 150\text{ mA}$)	f_T	400	MHz
Collector-to-Case Capacitance	C_c	6 max	pF
Output Capacitance ($V_{CB} = 30\text{ V}$, $I_E = 0$, $f = 1\text{ MHz}$)	C_{obo}	20 max	pF
RF Power Output Amplifier, Unneutralized:			
$V_{CE} = 28\text{ V}$, $P_{IE} = 4\text{ W}$, R_G and $R_L = 50\ \Omega$, $f = 260\text{ MHz}$	P_{OE}	14.5*	W
$V_{CE} = 28\text{ V}$, $P_{IE} = 4\text{ W}$, R_G and $R_L = 50\ \Omega$, $f = 400\text{ MHz}$	P_{OE}	10 \dagger min	W

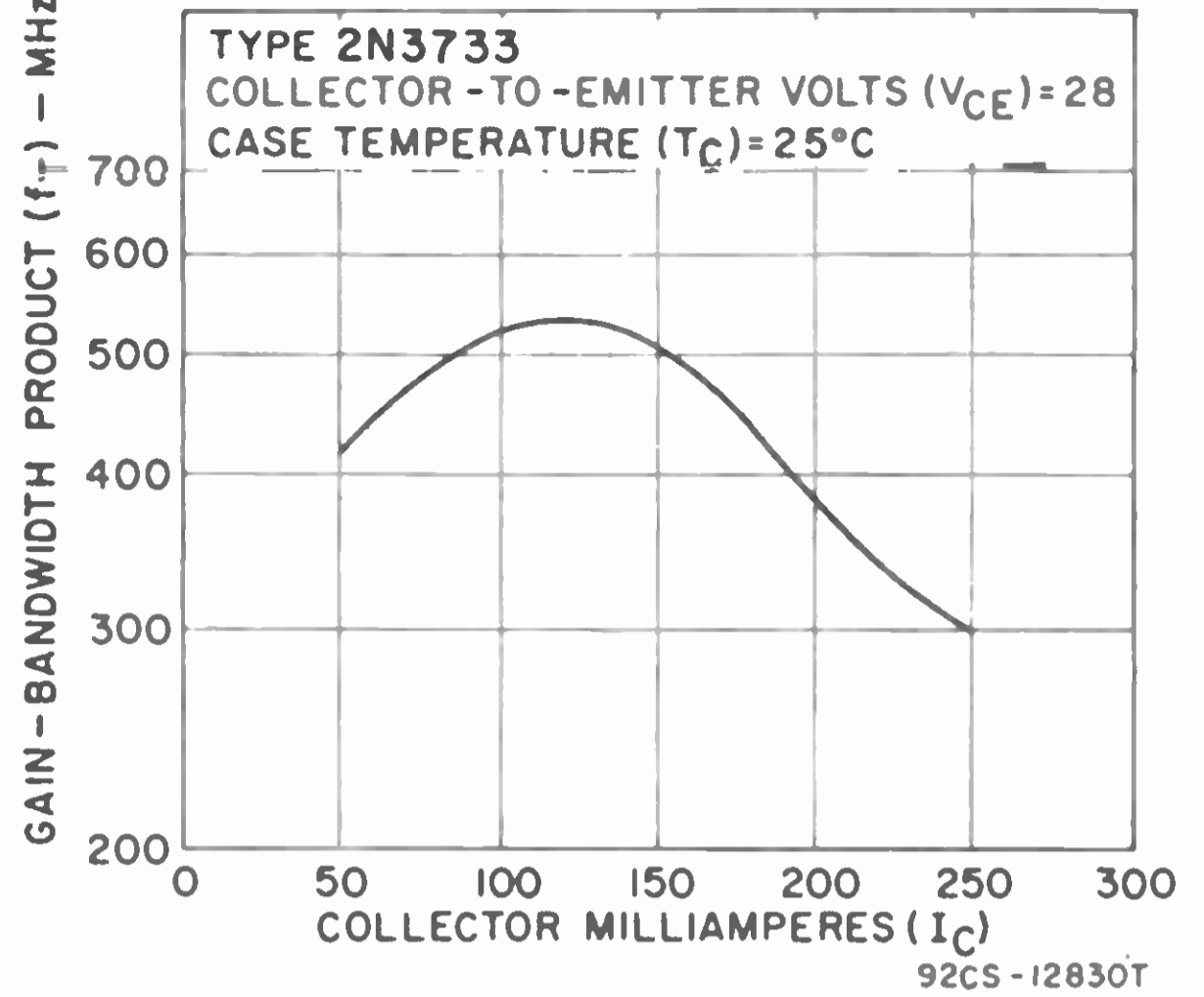
* For conditions given, minimum efficiency = 60 per cent.

\dagger For conditions given, minimum efficiency = 45 per cent.

TYPICAL OPERATION CHARACTERISTICS

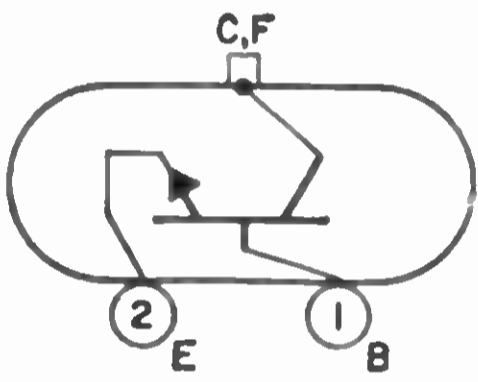


TYPICAL SMALL-SIGNAL OPERATION CHARACTERISTIC



POWER TRANSISTOR

2N3771



Si n-p-n type with high collector-current rating (30 A max) for intermediate- and high-power applications such as public-address amplifiers, power supplies, and low-speed switching regulators and inverters. This type features a base comprised of a homogeneous-resistivity silicon material. JEDEC TO-3, Outline No.2. See

Mounting Hardware for desired mounting arrangement.

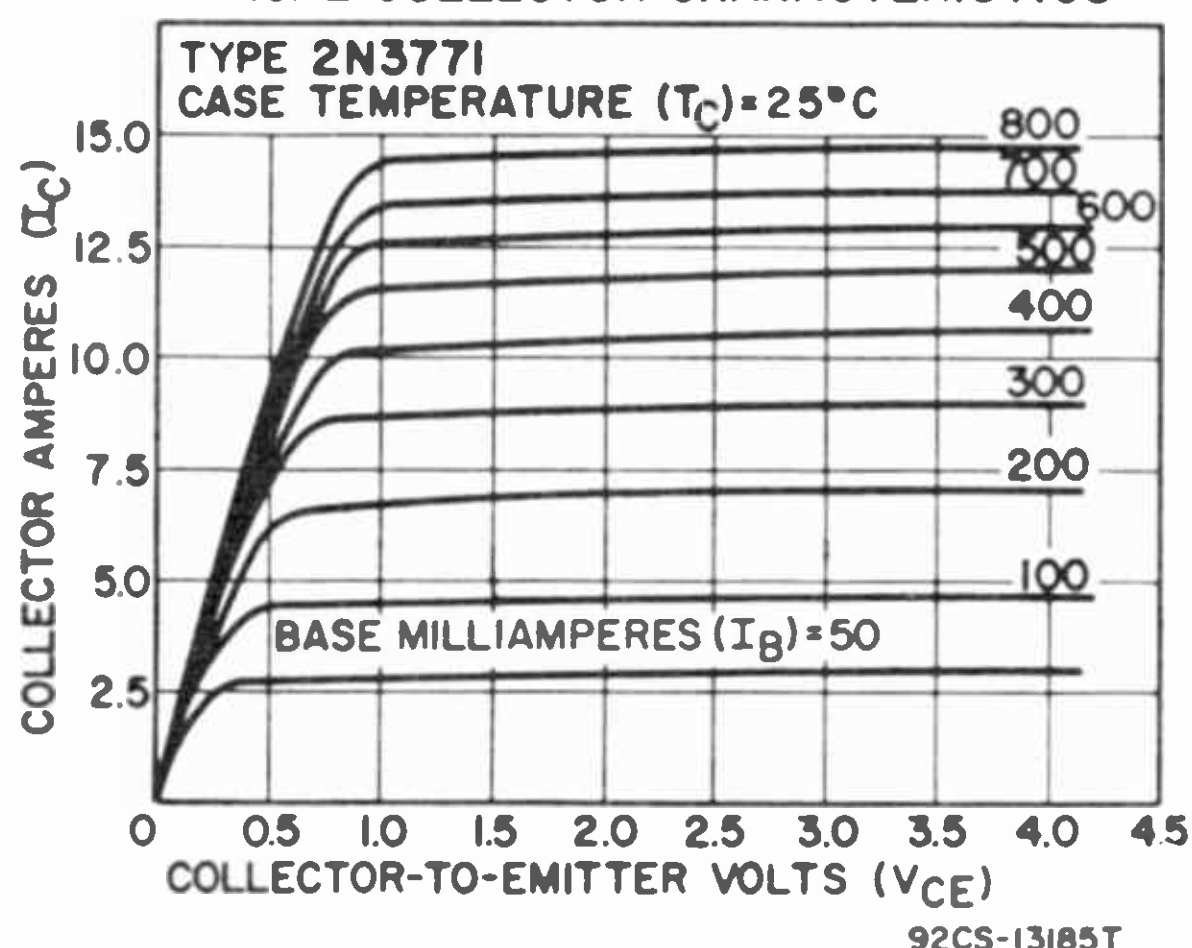
MAXIMUM RATINGS

Collector-to-Base Voltage	V _{CBO}	50	V
Collector-to-Emitter Voltage:			
V _{BE} = -1.5 V, R _{BE} = 100 Ω	V _{CEV}	50	V
Base open	V _{CEO}	40	V
Emitter-to-Base Voltage	V _{EBO}	5	V
Collector Current	I _C	30	A
Peak Collector Current	i _c	30	V
Base Current	I _B	7.5	V
Transistor Dissipation:			
T _c up to 25°C	P _T	150	W
T _c above 25°C	P _T	See curve page 300	
Temperature Range:			
Operating (Junction)	T _J (opr)	-65 to 200	°C
Storage	T _{STG}	-65 to 200	°C
Pin-Soldering Temperature (10 s max)	T _P	230	°C

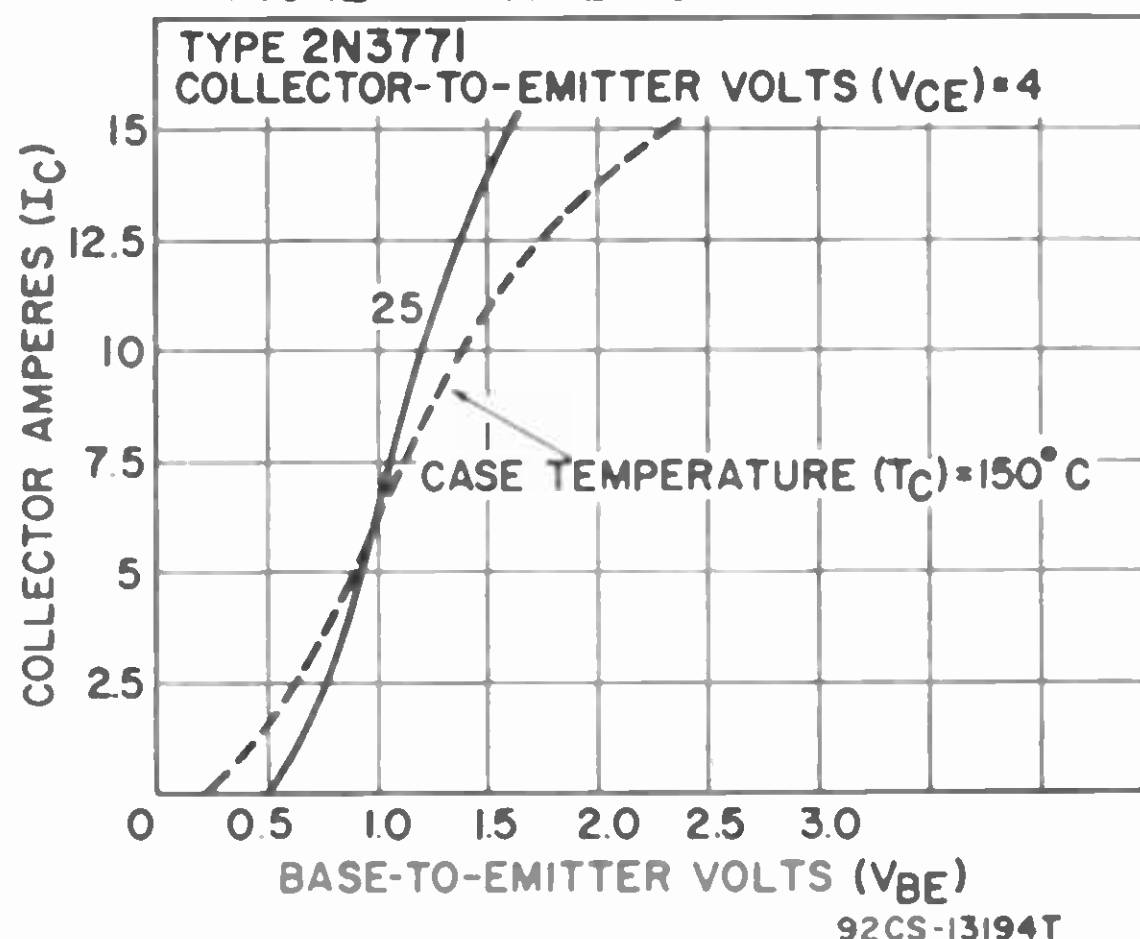
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage:			
R _{BE} = 100 Ω, I _C = 0.2 A	V _{CEV} (sus)	45	V
V _{EB} = -1.5 V, I _C = 0.2 A	V _{CEV} (sus)	50	V
V _{BE} = -1.5 V, I _C = 0.3 A, R _{BE} = 100 Ω	V _{CEV} (sus)	50 min	V
I _C = 0.2 A, I _B = 0	V _{CEO} (sus)	40 min	V
Collector-to-Emitter Saturation Voltage (I _B = 1.5 A, I _C = 15 A, t _p = 300 μs, f = 60 Hz)	V _{CE} (sat)	2 max	V
Base-to-Emitter Voltage (V _{CE} = 4 V, I _C = 15 A, t _p = 300 μs, f = 60 Hz)	V _{BE}	2.7 max	V
Collector-Cutoff Current:			
V _{CB} = 50 V, I _E = 0, T _c = 25°C	I _{CBO}	2 max	mA
V _{CB} = 30 V, I _E = 0, T _c = 150°C	I _{CBO}	10 max	mA
V _{CE} = 50 V, V _{BE} = -1.5 V, T _c = 25°C	I _{CEV}	2 max	mA
V _{CE} = 30 V, V _{BE} = -1.5 V, T _c = 150°C	I _{CEV}	10 max	mA
V _{CE} = 30 V, I _B = 0, T _c = 25°C	I _{CEO}	10 max	mA
Emitter-Cutoff Current (V _{EB} = 5 V, I _C = 0)	I _{EBO}	5 max	mA
Pulsed Static Forward-Current Transfer Ratio (V _{CE} = 4 V, I _C = 15 A, t _p = 300 μs, f = 60 Hz)	h _{FE} (pulsed)	15 to 60	
Gain-Bandwidth Product (V _{CE} = 4 V, I _C = 1 A)	f _T	800	kHz
Power Rating Test (V _{CE} = 33.5 V, I _C = 4.5 A, t = 1 s)		150	W
Thermal Resistance, Junction-to-Case	θ _{J-C}	1.17 max	°C/W

TYPICAL COLLECTOR CHARACTERISTICS

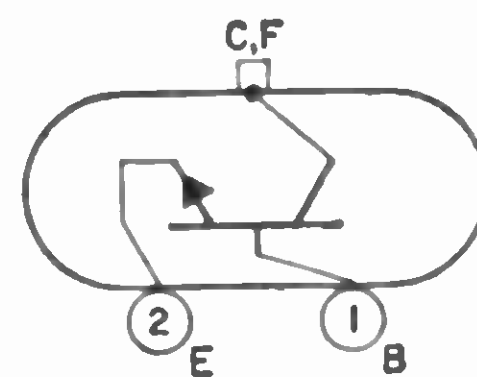


TYPICAL TRANSFER CHARACTERISTICS



2N3772 POWER TRANSISTOR

Si n-p-n type with high collector-current rating (30 A max) for intermediate- and high-power applications such as public-address amplifiers, power supplies, and low-speed switching regulators and inverters. This type features a base comprised of a homogeneous-resistivity silicon material. JEDEC TO-3, Outline No.2. See Mounting Hardware for desired mounting arrangement.

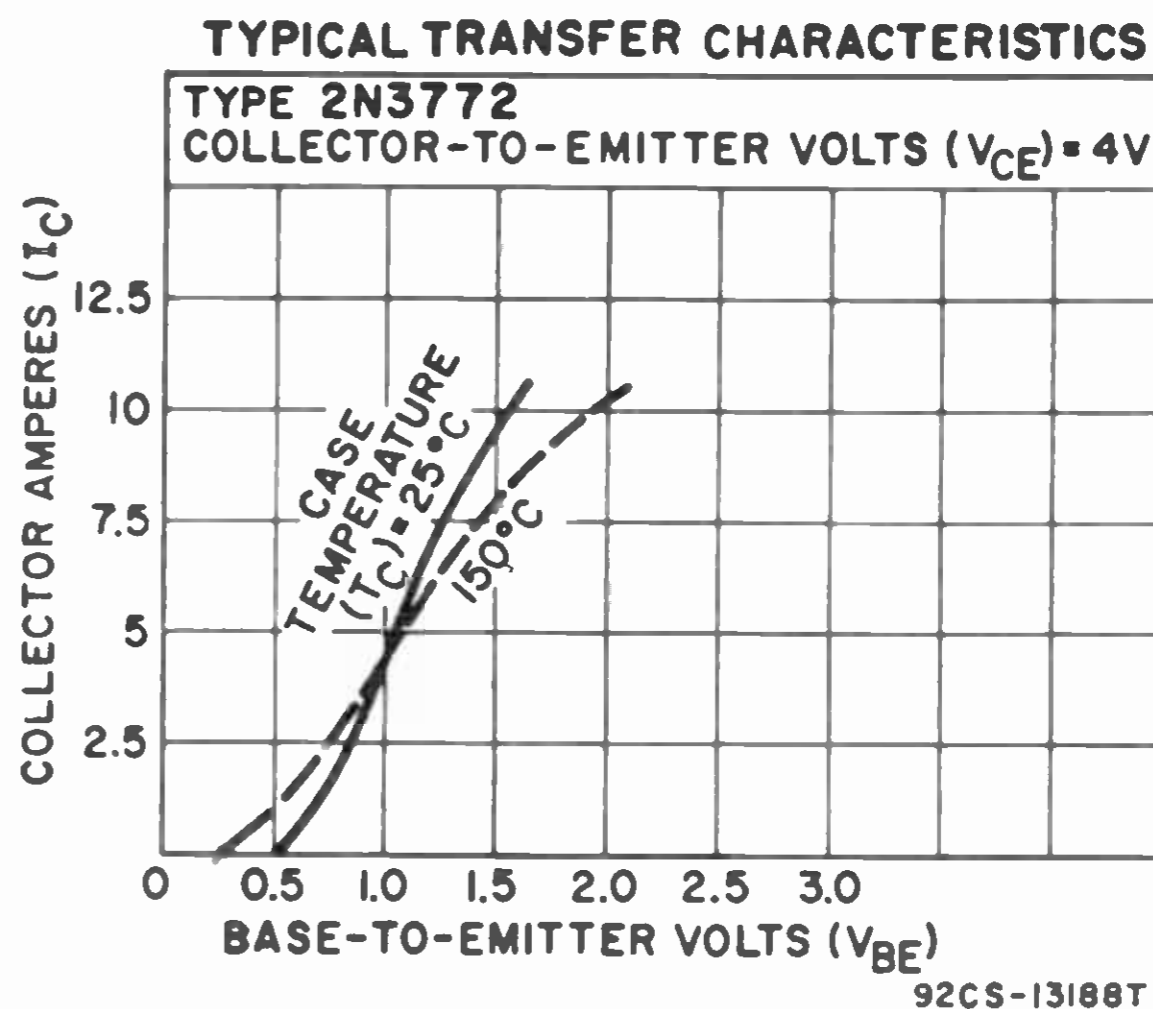
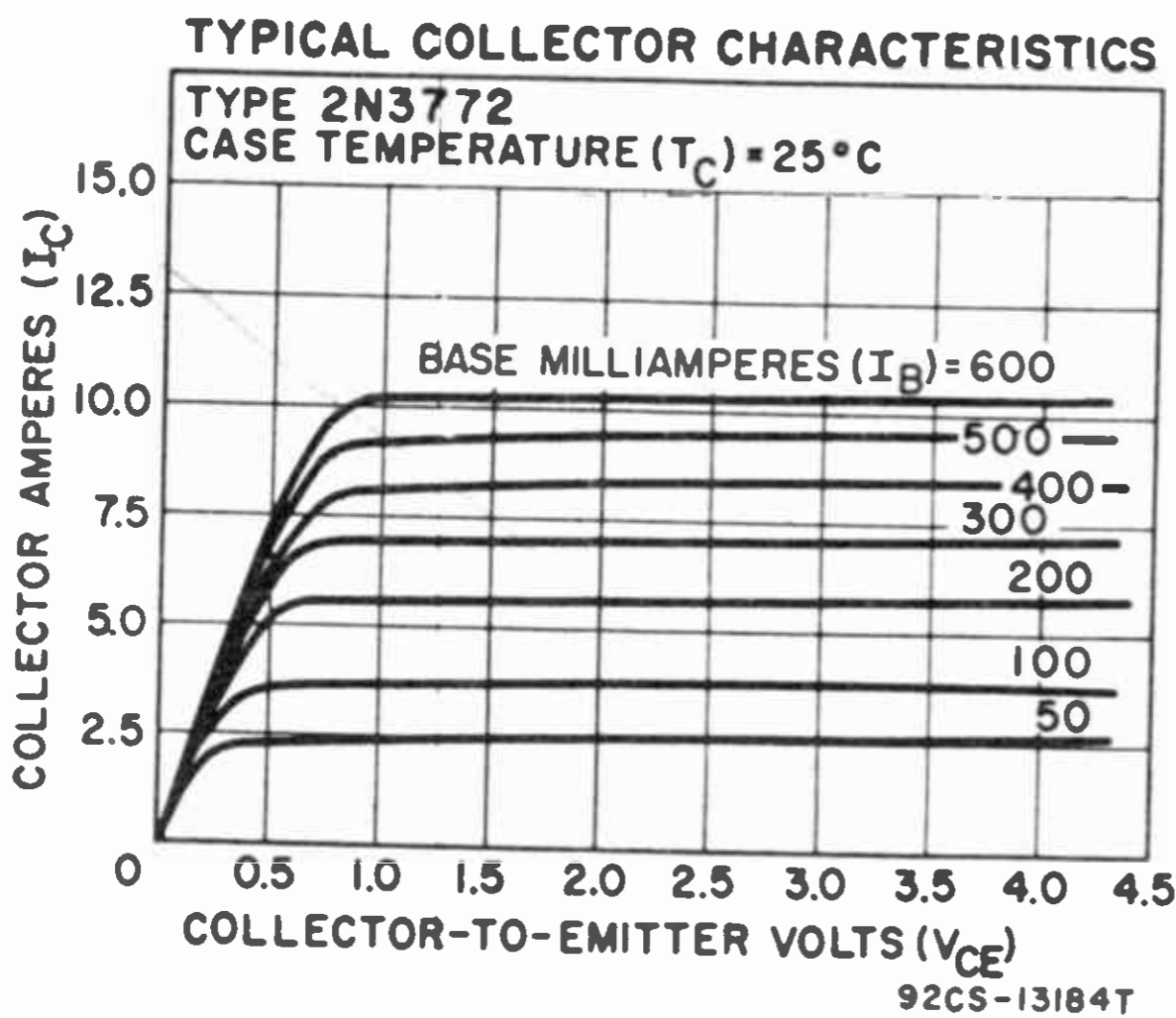


MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	100	V
Collector-to-Emitter Voltage: $V_{BE} = -1.5 \text{ V}$	V_{CEV}	90	V
Base open	V_{CEO}	60	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Collector Current	I_C	20	A
Peak Collector Current	i_C	30	A
Base Current	I_B	5	A
Transistor Dissipation: Tc up to 25°C	P_T	150	W
Tc above 25°C	P_T	See curve page 300	
Temperature Range: Operating (Junction)	$T_J(\text{opr})$	-65 to 200	$^\circ\text{C}$
Storage	T_{STG}	-65 to 200	$^\circ\text{C}$
Pin-Soldering Temperature (10 s max)	T_P	230	$^\circ\text{C}$

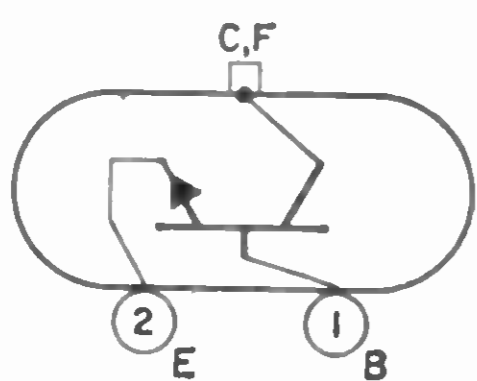
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage: $V_{BE} = -1.5 \text{ V}$, $I_C = 0.3 \text{ A}$, $R_{BE} = 100 \ \Omega$	$V_{CEV}(\text{sus})$	90 min	V
$V_{EB} = -1.5 \text{ V}$, $I_C = 0.2 \text{ A}$	$V_{CEV}(\text{sus})$	80	V
$R_{BE} = 100 \ \Omega$, $I_C = 0.2 \text{ A}$	$V_{CER}(\text{sus})$	45	V
$I_C = 0.2 \text{ A}$, $I_B = 0$	$V_{CEO}(\text{sus})$	60 min	V
Collector-to-Emitter Saturation Voltage ($I_B = 1 \text{ A}$, $I_C = 10 \text{ A}$, $t_p = 300 \ \mu\text{s}$, $f = 60 \text{ Hz}$)	$V_{CE}(\text{sat})$	1.4 max	V
Base-to-Emitter Voltage ($V_{CE} = 4 \text{ V}$, $I_C = 10 \text{ A}$, $t_p = 300 \ \mu\text{s}$, $f = 60 \text{ Hz}$)	V_{BE}	2.2 max	V
Collector-Cutoff Current: $V_{CB} = 100 \text{ V}$, $I_E = 0$, $T_C = 25^\circ\text{C}$	I_{CBO}	5 max	mA
$V_{CB} = 30 \text{ V}$, $I_E = 0$, $T_C = 150^\circ\text{C}$	I_{CBO}	10 max	mA
$V_{CE} = 100 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 25^\circ\text{C}$	I_{CEV}	5 max	mA
$V_{CE} = 30 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 150^\circ\text{C}$	I_{CEV}	10 max	mA
$V_{CE} = 50 \text{ V}$, $I_B = 0$, $T_C = 25^\circ\text{C}$	I_{CEO}	10 max	mA
Emitter-Cutoff Current ($V_{EB} = 7 \text{ V}$, $I_C = 0$)	I_{EBO}	5 max	mA
Pulsed Static Forward-Current Transfer Ratio ($V_{CE} = 4 \text{ V}$, $I_C = 10 \text{ A}$, $t_p = 300 \ \mu\text{s}$, $f = 60 \text{ Hz}$)	$h_{FE}(\text{pulsed})$	15 to 60	
Gain-Bandwidth Product ($V_{CE} = 4 \text{ V}$, $I_C = 1 \text{ A}$)	f_T	800	kHz
Power Rating Test ($V_{CE} = 33.5 \text{ V}$, $I_C = 4.5 \text{ A}$, $t = 1 \text{ s}$)		150	W
Thermal Resistance, Junction-to-Case	θ_{J-C}	1.17 max	$^\circ\text{C/W}$



POWER TRANSISTOR

2N3773



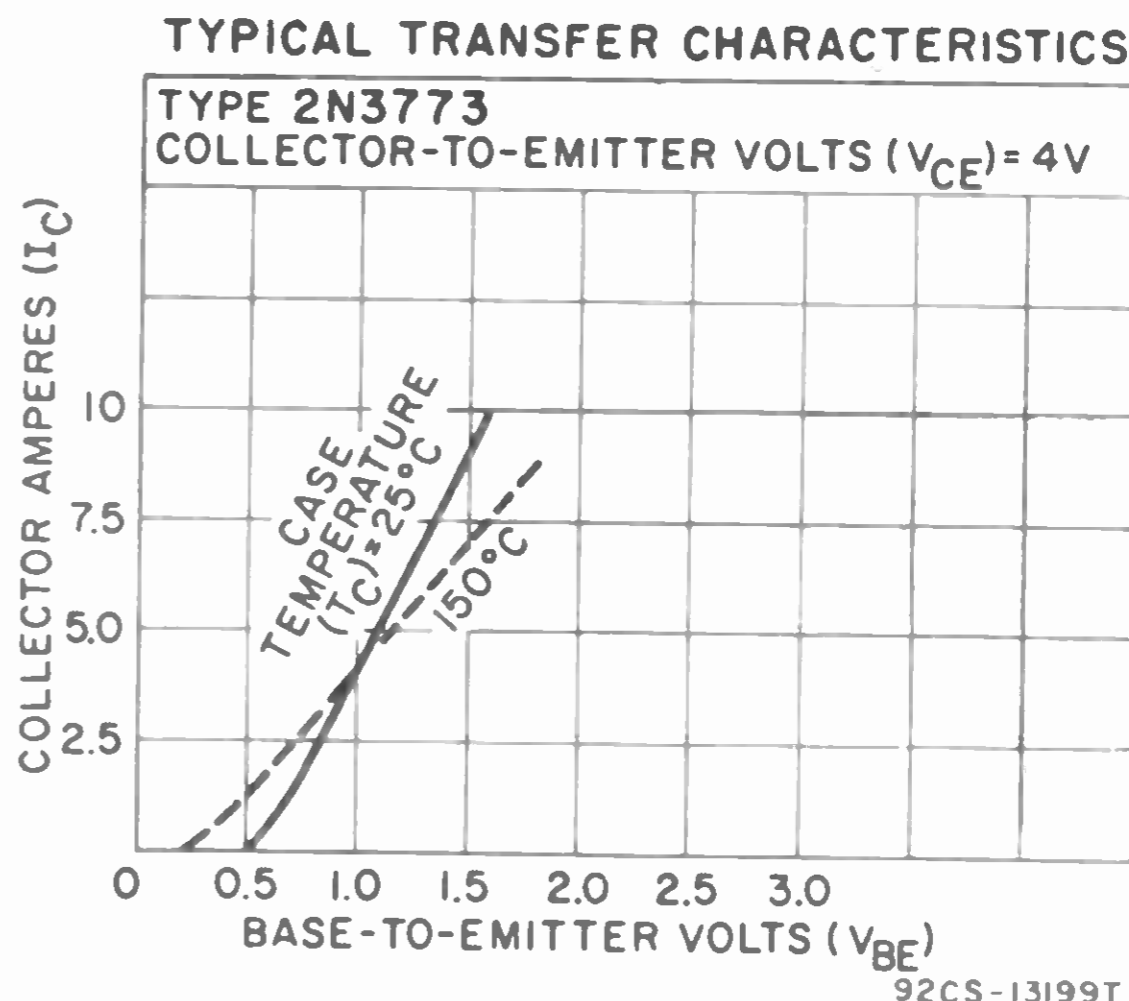
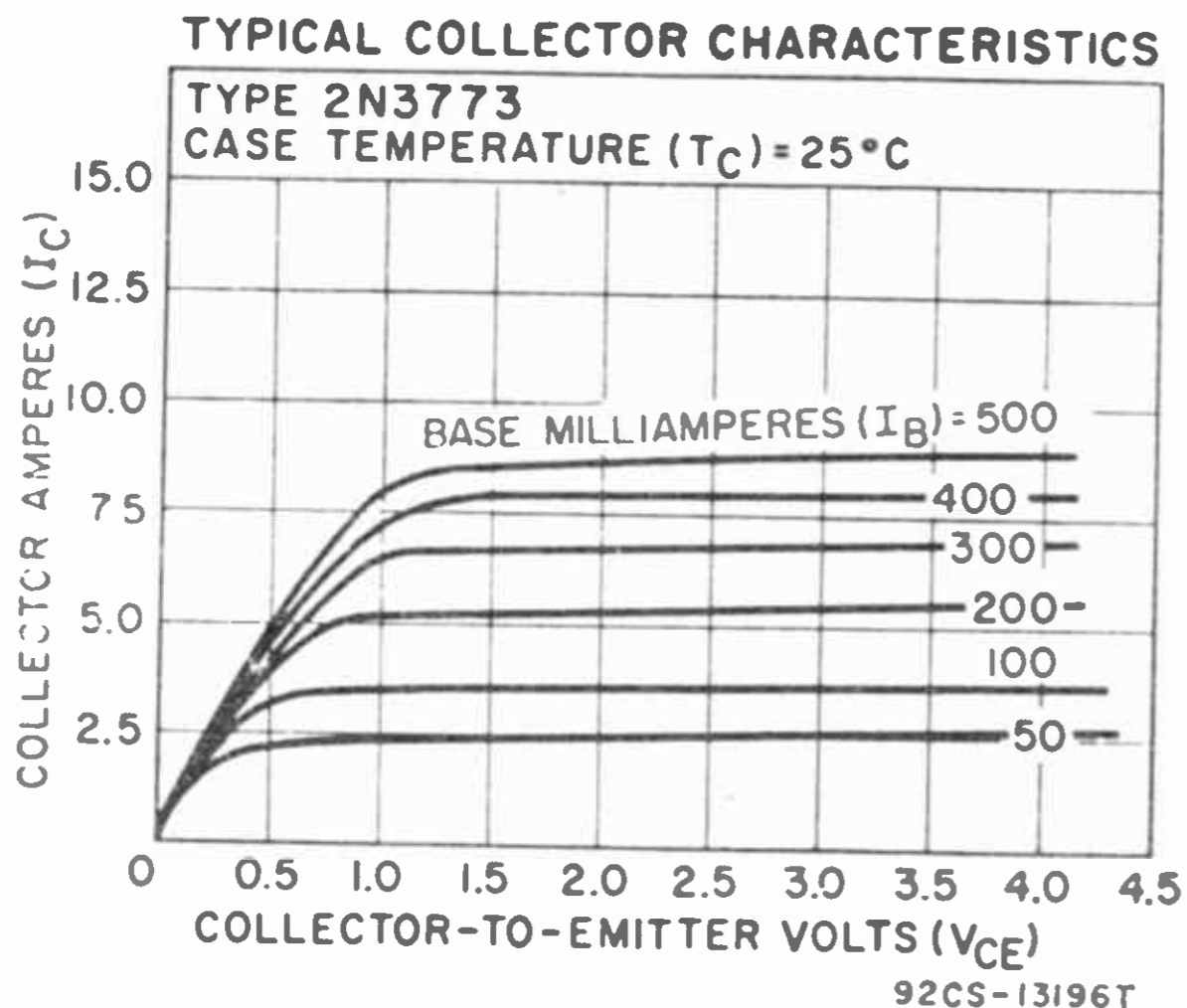
Si n-p-n type with high collector-current rating (30 A max) for intermediate- and high-power applications such as public-address amplifiers, power supplies, and low-speed switching regulators and inverters. This type features a base comprised of a homogeneous-resistivity silicon material. JEDEC TO-3, Outline No.2. See Mounting Hardware for desired mounting arrangement.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	160	V
Collector-to-Emitter Voltage: $V_{EE} = -1.5$ V	V_{CEV}	160	V
Base open	V_{CEO}	140	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Collector Current	I_C	16	A
Peak Collector Current	i_C	30	A
Base Current	I_B	4	A
Transistor Dissipation:			
T_C up to 25°C	P_T	150	W
T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Pin-Soldering Temperature (10 s max)	T_P	230	°C

CHARACTERISTICS (At case temperature = 25°C)

Emitter-to-Base Breakdown Voltage ($I_E = 5$ mA, $I_C = 0$)	$V_{(BR)EBO}$	7 max	V
Collector-to-Emitter Sustaining Voltage: $V_{BE} = -1.5$ V, $I_C = 0.1$ to 1.5 A	V_{CEV} (sus)	160 min	V
$I_C = 0.2$ to 3 A, $I_B = 0$	V_{CEO} (sus)	140 min	V



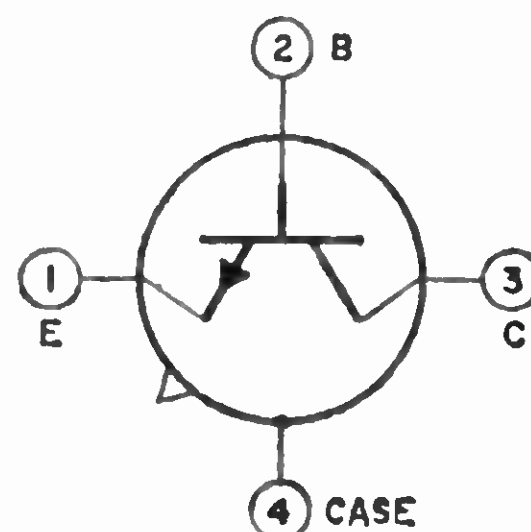
CHARACTERISTICS (cont'd)

Collector-to-Emitter Saturation Voltage ($I_B = 0.8$ A, $I_C = 8$ A, $t_p = 300$ μ s, $f = 60$ Hz)	$V_{CE(sat)}$	1.4 max	V
Base-to-Emitter Voltage ($V_{CE} = 4$ V, $I_C = 8$ A, $t_p = 300$ μ s, $f = 60$ Hz)	V_{BE}	2.2 max	V
Collector-Cutoff Current: $V_{CE} = 140$ V, $V_{BE} = -1.5$ V, $T_C = 25^\circ$ C	I_{CEV}	2 max	mA
$V_{CE} = 140$ V, $I_B = 0$, $T_C = 150^\circ$ C	I_{CEV}	10 max	mA
$V_{CE} = 120$ V, $I_B = 0$, $T_C = 25^\circ$ C	I_{CEO}	2 max	mA
Emitter-Cutoff Current ($V_{EB} = 7$ V, $I_C = 0$)	I_{EBO}	5 max	mA
Pulsed Static Forward-Current Transfer Ratio ($V_{CE} = 4$ V, $I_C = 8$ A, $t_p = 300$ μ s, $f = 60$ Hz)	h_{FE} (pulsed)	15 to 60	
Power Rating Test ($V_{CE} = 100$ V, $I_C = 1.5$ A, $t = 1$ s)		150	W
Thermal Resistance, Junction-to-Case	θ_{J-C}	1.17 max	$^\circ$ C/W

2N3839

UHF TRANSISTOR

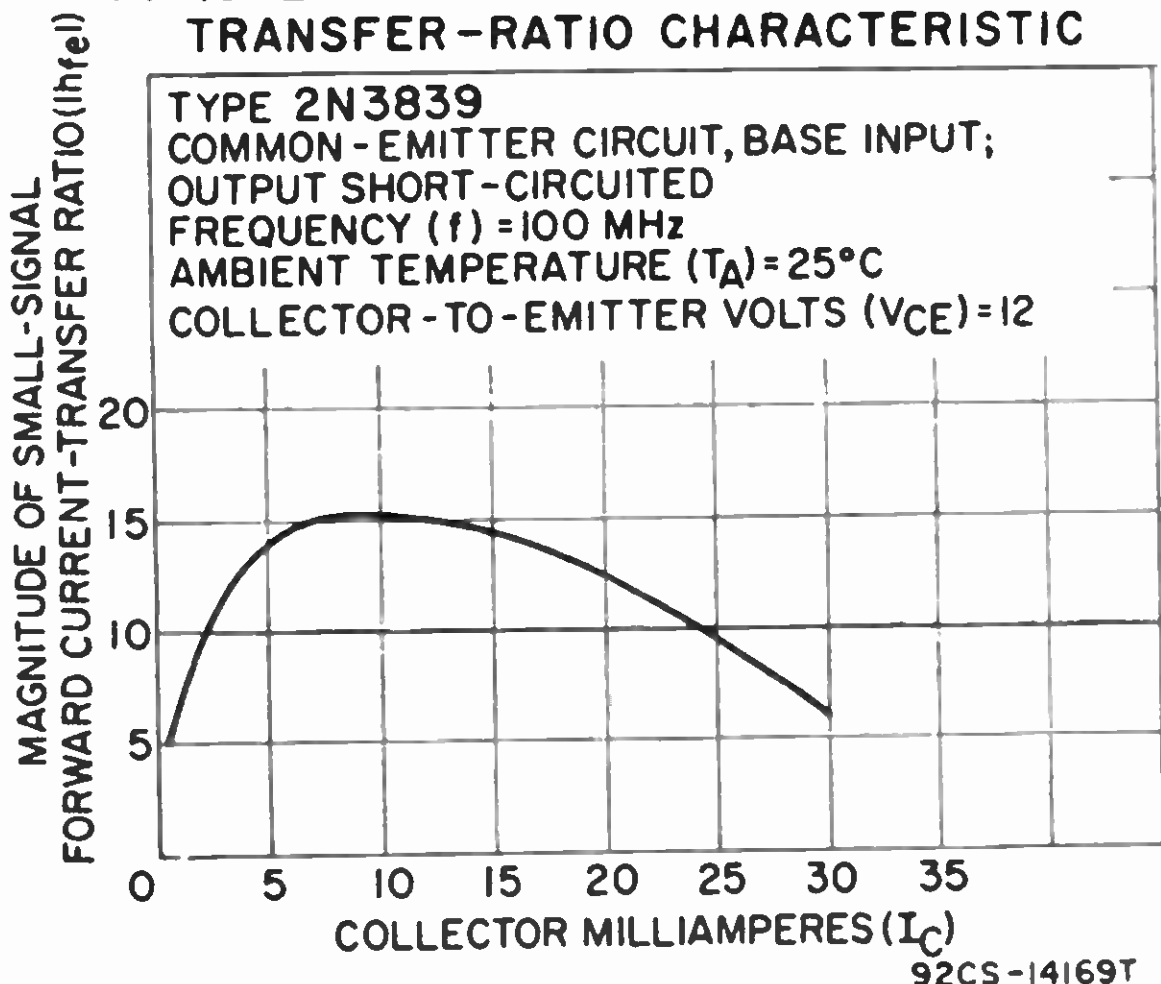
Si n-p-n double-diffused epitaxial planar type used in low-noise amplifier, oscillator, and converter applications at frequencies up to 500 MHz in a common-emitter circuit and 1200 MHz in a common-base circuit. JEDEC TO-72, Outline No.28. For maximum ratings, refer to type 2N2857.



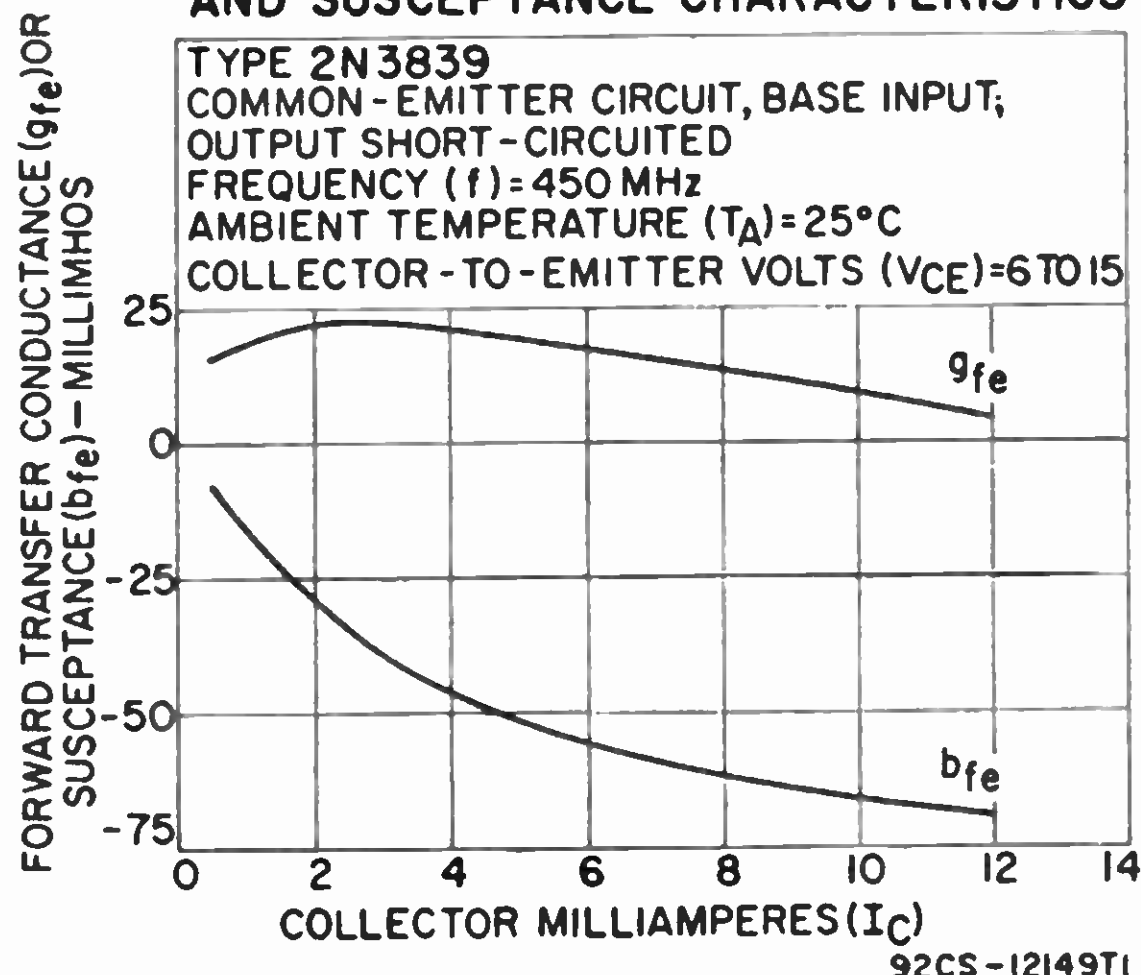
CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = 0.001$ mA, $I_E = 0$)	$V_{(BR)CBO}$	30 min	V
Collector-to-Emitter Breakdown Voltage ($I_C = 3$ mA, $I_B = 0$)	$V_{(BR)CEO}$	15 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -0.01$ mA, $I_C = 0$)	$V_{(BR)EBO}$	2.5 min	V
Collector-Cutoff Current: $V_{CB} = 15$ V, $I_E = 0$	I_{CBO}	10 max	μ A
$V_{CB} = 15$ V, $I_E = 0$, $T_A = 150^\circ$ C	I_{CBO}	1 max	μ A
Static Forward-Current Transfer Ratio ($V_{CE} = 1$ V, $I_C = 3$ mA)	h_{FE}	30 to 150	
Small-Signal Forward-Current Transfer Ratio*: $V_{CE} = 6$ V, $I_C = 2$ mA, $f = 0.001$ MHz	h_{fe}	50 to 220	
$V_{CE} = 6$ V, $I_C = 5$ mA, $f = 100$ MHz	h_{fe}	10 to 20	
Feedback Capacitance* ($V_{CB} = 10$ V, $I_E = 0$, $f = 0.1$ to 1 MHz)	C_{cb}	0.6 typ; 1 max	pF
Input Capacitance ($V_{EB} = 0.5$ V, $I_C = 0$, $f = 0.1$ to 1 MHz)	C_{ibo}	1.4	pF
Collector-to-Base Time Constant* ($V_{CB} = 6$ V, $I_E = -2$ mA, $f = 31.9$ MHz)	$r_b'c_c$	1 to 15	ps
Small-Signal Power Gain* ($V_{CE} = 6$ V, $I_C = 1.5$ mA, $f = 450$ MHz)	G_{pe}	12.5 to 19	dB
Power Output* ($V_{CB} = 10$ V, $I_E = -12$ mA, $f \cong 500$ MHz)	P_{oe}	30 min	mW

TYPICAL SMALL-SIGNAL FORWARD-CURRENT TRANSFER-RATIO CHARACTERISTIC



TYPICAL FORWARD TRANSFER CONDUCTANCE AND SUSCEPTANCE CHARACTERISTICS



CHARACTERISTICS (cont'd)

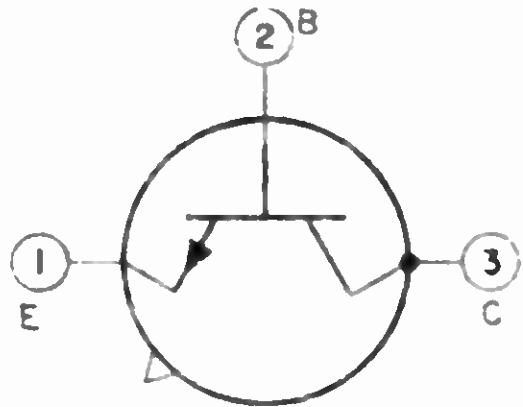
Noise Figure* :

UHF Measured ($V_{CE} = 6 \text{ V}$, $I_C = 1.5 \text{ mA}$, $f = 450 \text{ MHz}$, $R_G = 50 \Omega$)	NF	3.9 max	dB
UHF Device ($V_{CE} = 6 \text{ V}$, $I_C = 1.5 \text{ mA}$, $f = 450 \text{ MHz}$, $R_G = 50 \Omega$)	NF	3.4 max	dB
VHF Measured ($V_{CE} = 6 \text{ V}$, $I_C = 1 \text{ mA}$, $f = 60 \text{ MHz}$, $R_G = 400 \Omega$)	NF	2	dB

- * Lead No. 4 (case) not connected.
- Three-terminal measurement with emitter and case connected to guard terminal.
- Lead No. 4 (case) grounded.

TRANSISTOR

2N3866



Si n-p-n "overlay" epitaxial planar type for vhf-uhf applications in class A, B, and C amplifiers, frequency multipliers, and oscillators in military and industrial communications equipment. JEDEC TO-39, Outline No.15.

MAXIMUM RATINGS

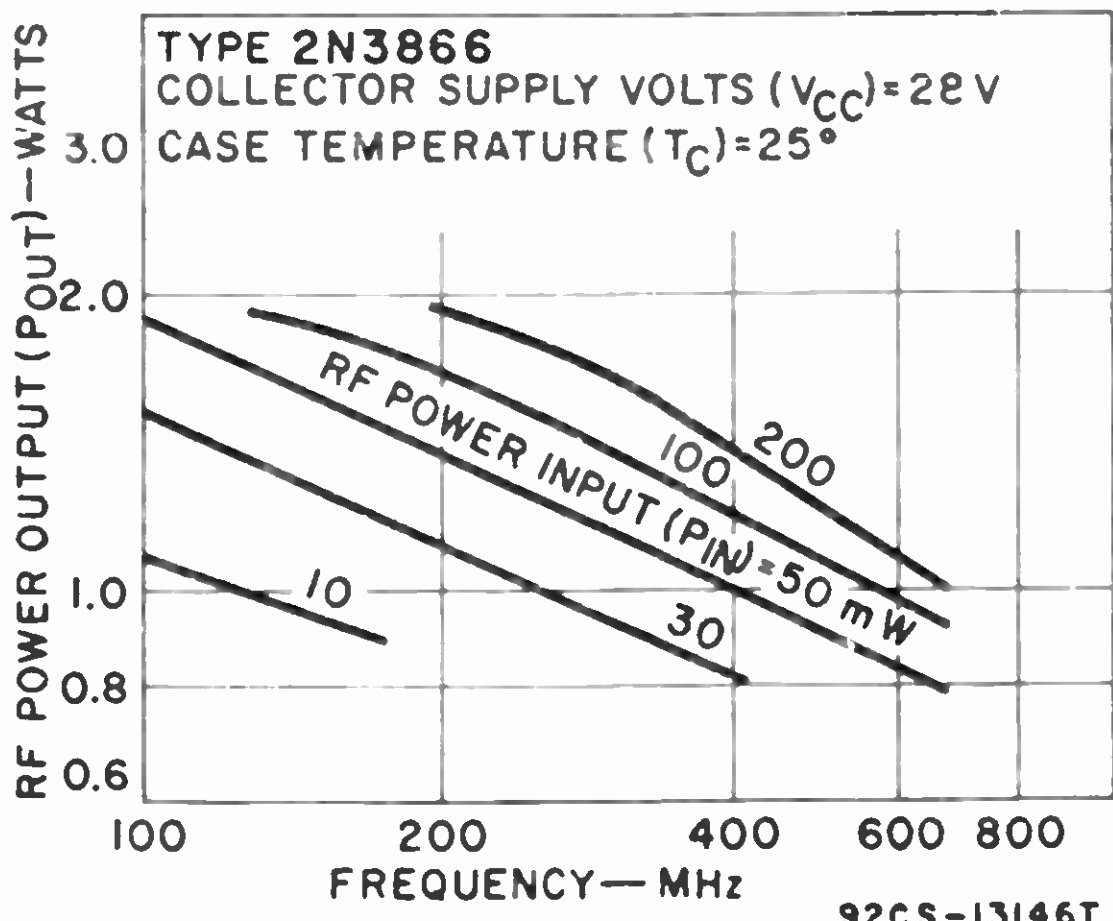
Collector-to-Base Voltage	V_{CBO}	55	V
Collector-to-Emitter Voltage: $R_{BE} = 10 \Omega$	V_{CER}	55	V
Base open	V_{CEO}	30	V
Emitter-to-Base Voltage	V_{EBO}	3.5	V
Collector Current	I_C	0.4	A
Transistor Dissipation: T_C up to 25°C	P_T	5	W
T_C above 25°C	P_T	See curve page 300	
Temperature Range: Operating (Junction)	$T_J(\text{opr})$	-65 to 200	$^\circ\text{C}$
Storage	T_{STG}	-65 to 200	$^\circ\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	230	$^\circ\text{C}$

CHARACTERISTICS (At case temperature = 25°C)

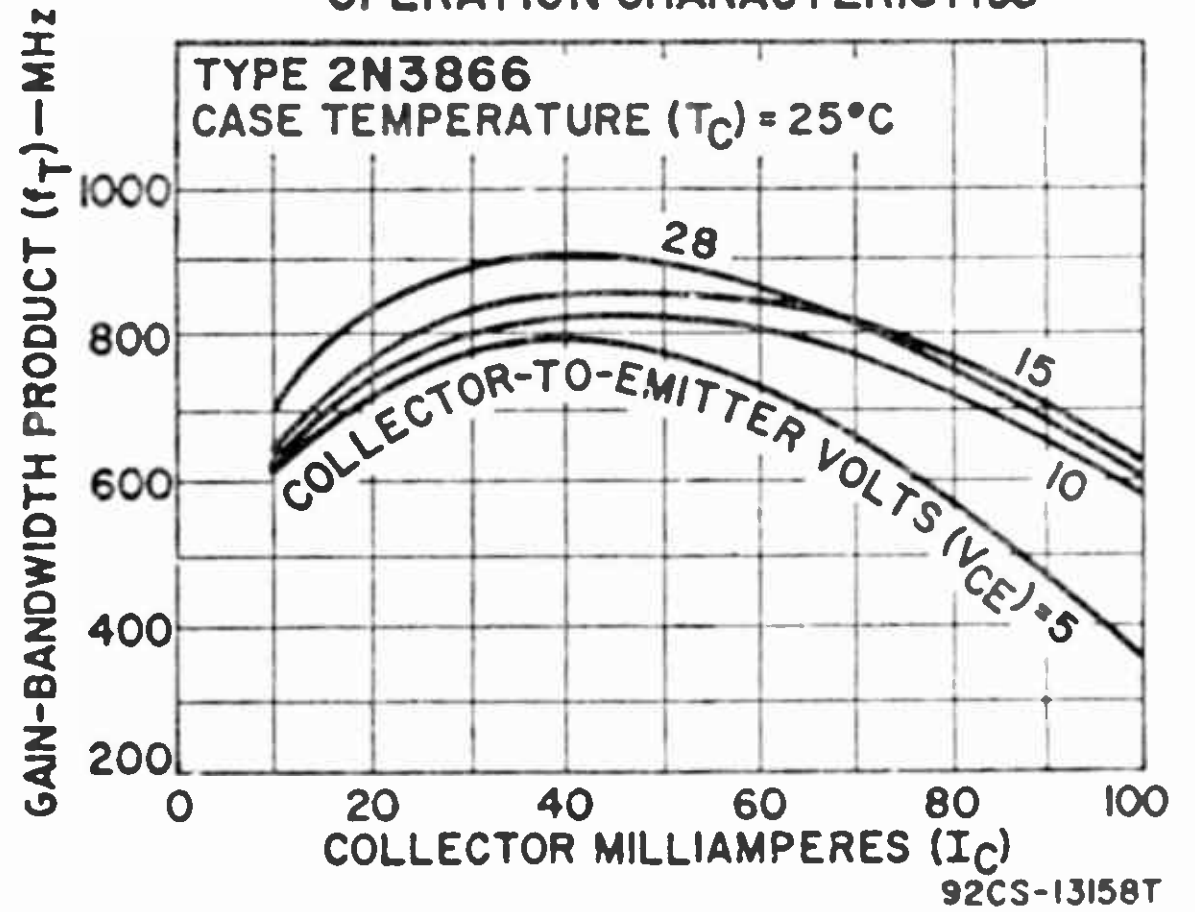
Collector-to-Base Breakdown Voltage ($I_C = 0.1 \text{ mA}$, $I_E = 0$)	$V_{(BR)CBO}$	55 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.1 \text{ mA}$, $I_C = 0$)	$V_{(BR)EBO}$	3.5 min	V
Collector-to-Emitter Sustaining Voltage: $I_C = 5 \text{ mA}$, $R_{BE} = 10 \Omega$	$V_{CER}(\text{sus})$	55 min	V
$I_C = 5 \text{ mA}$, $I_B = 0$	$V_{CEO}(\text{sus})$	30 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 100 \text{ mA}$, $I_B = 20 \text{ mA}$)	$V_{CE}(\text{sat})$	1 max	V
Collector-Cutoff Current ($V_{CE} = 28 \text{ V}$, $I_B = 0$)	I_{CEO}	20 max	μA
Gain-Bandwidth Product ($V_{CE} = 15 \text{ V}$, $I_C = 25 \text{ mA}$)	ft	800	MHz
Output Capacitance ($V_{CB} = 30 \text{ V}$, $I_E = 0$, $f = 1 \text{ MHz}$)	C_{obo}	3 max	pF
RF Power-Output Class C Amplifier, Unneutralized: $V_{CC} = 28 \text{ V}$, $P_{IE} = 0.05 \text{ W}$, $f = 100 \text{ MHz}$	P_{OE}	1.8*	W
$V_{CC} = 28 \text{ V}$, $P_{IE} = 0.1 \text{ W}$, $f = 250 \text{ MHz}$	P_{OE}	1.5●	W
$V_{CC} = 28 \text{ V}$, $P_{IE} = 0.1 \text{ W}$, $f = 400 \text{ MHz}$	P_{OE}	1† min	W

- * For conditions given, minimum efficiency = 60 per cent.
- For conditions given, minimum efficiency = 50 per cent.
- † For conditions given, minimum efficiency = 45 per cent.

TYPICAL OPERATION CHARACTERISTICS

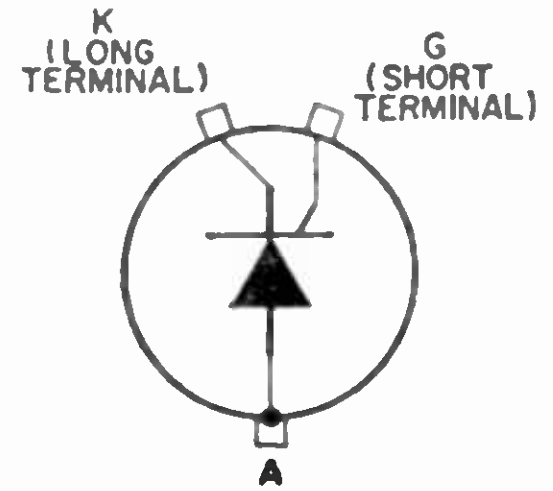


TYPICAL SMALL-SIGNAL OPERATION CHARACTERISTICS



2N3870- 2N3873

SILICON CONTROLLED RECTIFIERS



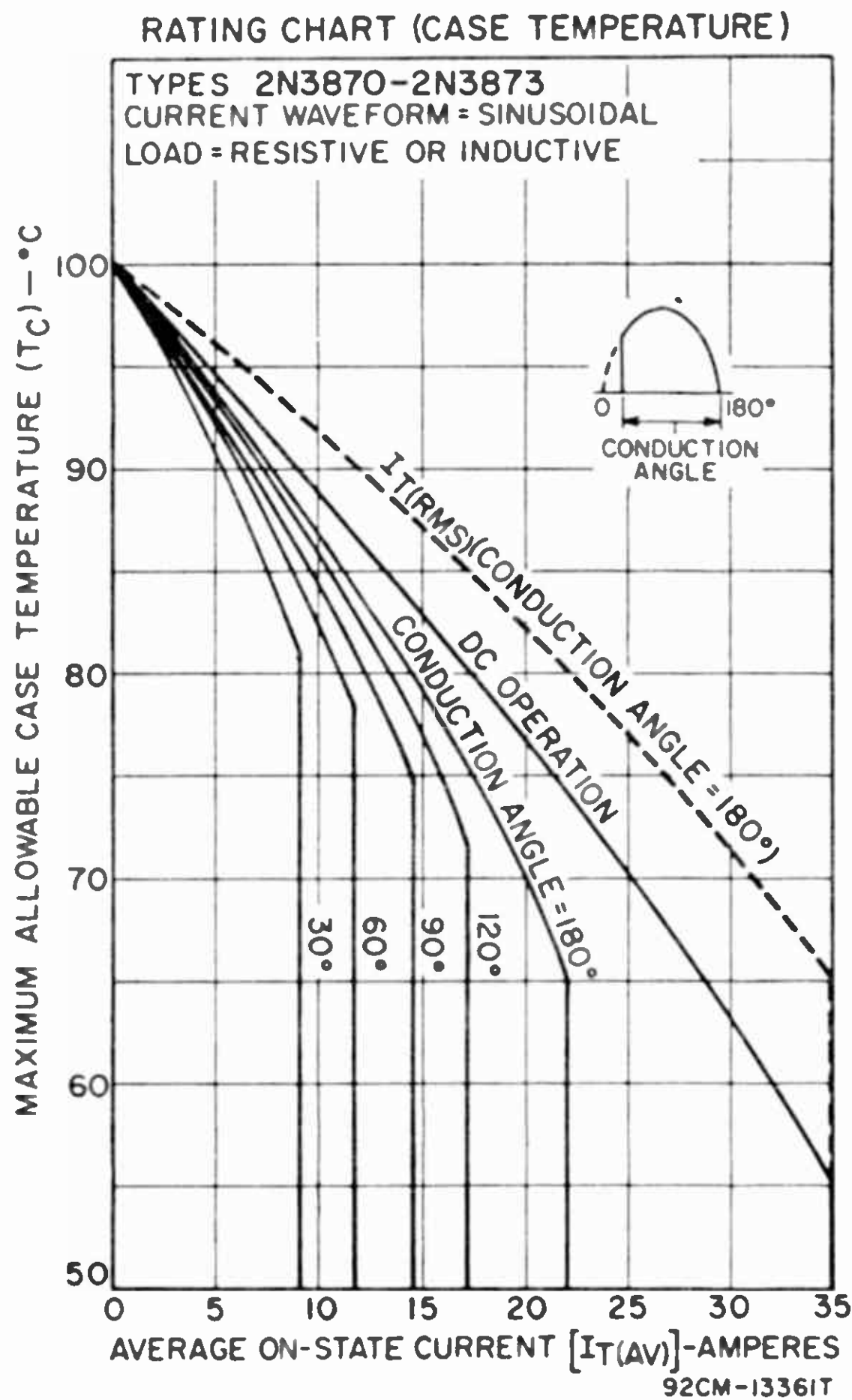
Si all-diffused three-junction types for use in power-control and power-switching applications. Outline No.36. For curve of forward gate characteristics, refer to type 2N3668.

MAXIMUM RATINGS (For sinusoidal ac supply voltage at $f = 50$ to 400 Hz with resistive or inductive load)

	2N3870	2N3871	2N3872	2N3873	
V_{RSOM}	150	330	660	700	V
V_{RROM}	100	200	400	600	V
V_{DROM}	700				V
$I_{T(AV)}$ (conduction angle = 180° , $T_c = 65^\circ C$)	22				A
$I_{T(RMS)}$	35				A
I_{TSM} (1 cycle of principle voltage)	350				A
Critical di/dt	200				A/ μs
P_{GM} (peak, forward, or reverse for $10 \mu s$)	40				W
$P_{G(AV)}$	0.5				W
T_{stg}	-40 to 125				$^\circ C$
T_c	-40 to 100				$^\circ C$

CHARACTERISTICS (At maximum electrical rating at $T_c = 25^\circ C$)

	2N3870	2N3871	2N3872	2N3873	
$V_{F(BOD)}$ ($T_c = 100^\circ C$)	100 min	200 min	400 min	600 min	V
I_{DOM} ($V_D = V_{F(BOD)}$ min value, $T_c = 100^\circ C$)	0.2 typ 2 max	0.25 typ 2.5 max	0.3 typ 3 max	0.35 typ 4 max	mA mA
I_{RROM} ($V_{RD} = V_{F(BOD)}$ min value, $T_c = 100^\circ C$)	3 max				mA
v_T (on-state current = 100 A)	1.7 typ; 2.1 max				V



CHARACTERISTICS (cont'd)

v_T (initial) ($i_T = 300$ A, $t = 2$ μ s, $V_D = V_{F(BO)}$ min value, $I_{GT} = 200$ mA)
 I_{GT}
 V_{GT}
 I_{HO}
Critical dv/dt ($V_D = V_{F(BO)}$ min value, exponential rise, $T_C = 100^\circ$ C)
 t_{gt} ($V_D = V_{F(BO)}$ min value, $i_T = 30$ A, $I_{GT} = 200$ mA, $t_r = 0.1$ μ s)
 t_q ($i_T = 18$ A, 50 μ s pulse width, $dv_D/dt = 20$ V/ μ s, $di_T/dt = 30$ A/ μ s, $I_{GT} = 200$ mA, $T_C = 80^\circ$ C)

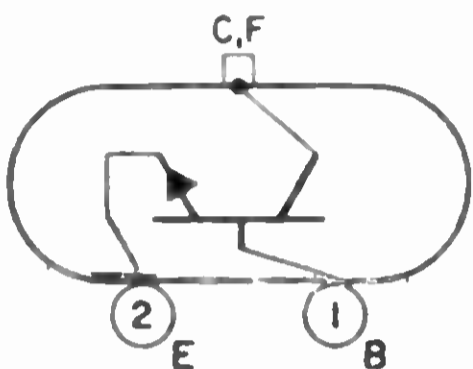
2N3870 2N3871 2N3872 2N3873

_____ 15 typ; 25 max _____	V
_____ 1 min, 25 typ, 40 max _____	mA (dc)
_____ 1.1 typ; 2 max _____	V (dc)
_____ 0.5 to 70 _____	mA
_____ 10 min; 100 typ _____	V (dc)
_____ 0.75 to 2 _____	μ s
_____ 15 to 40 _____	μ s

POWER TRANSISTOR

2N3878

Si n-p-n epitaxial type used in af, rf, and ultrasonic applications such as low-distortion power amplifiers, oscillators, switching regulators, series regulators, converters, and inverters. JEDEC TO-66, Outline No.25. See Mounting Hardware for desired mounting arrangement.



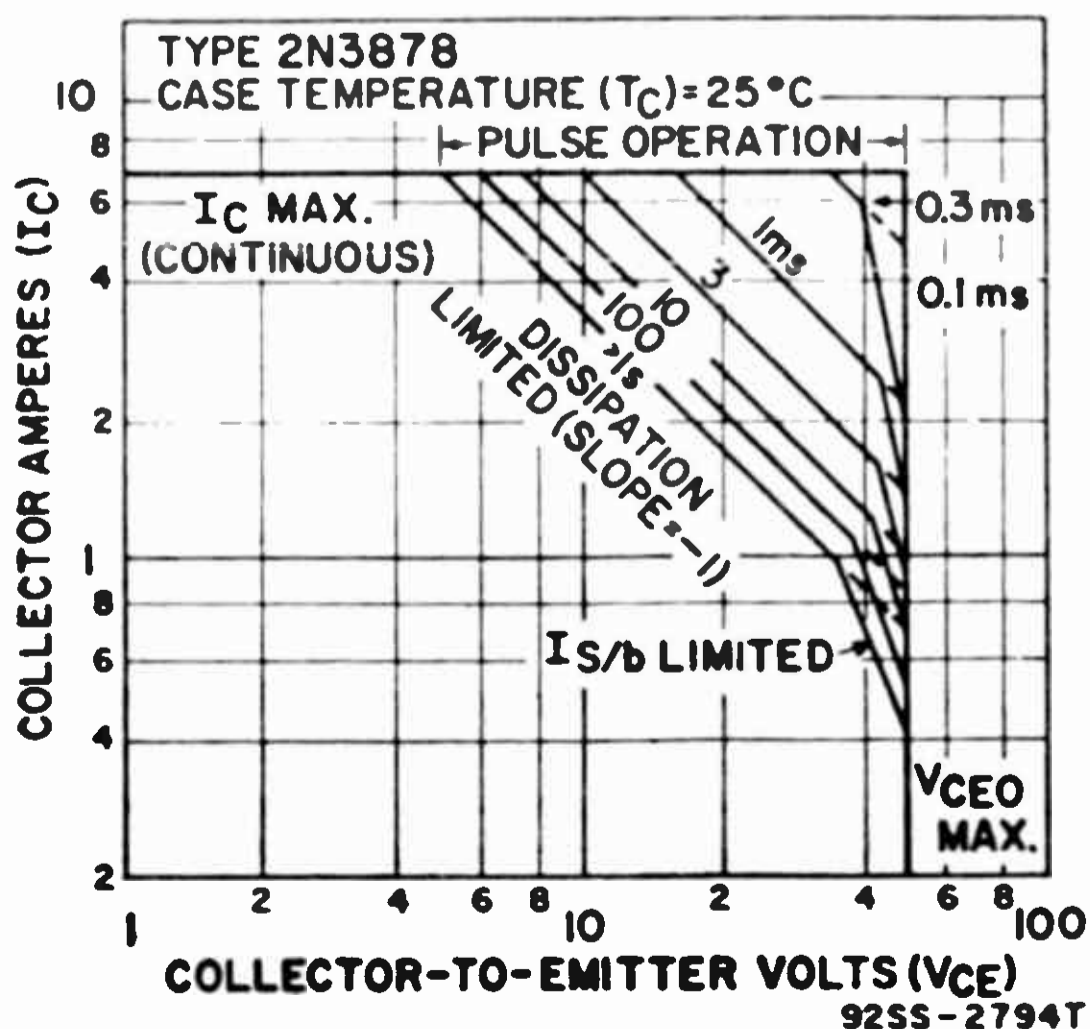
MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	120	V
Collector-to-Emitter Voltage: $R_{BE} = 50$ Ω	$V_{CER(SUS)}$	65	V
Base open (sustaining voltage)	$V_{CEO(SUS)}$	50	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Collector Current	I_C	7	A
Peak Collector Current	i_C	10	A
Base Current	I_B	5	A
Transistor Dissipation: T_c up to 25° C	P_T	35	W
T_c above 25° C	P_T	See curve page 300	
Temperature Range: Operating (Junction)	$T_J(opr)$	-65 to 200	$^\circ$ C
Storage	T_{STG}	-65 to 200	$^\circ$ C
Pin-Soldering Temperature (10 s max)	T_P	255	$^\circ$ C

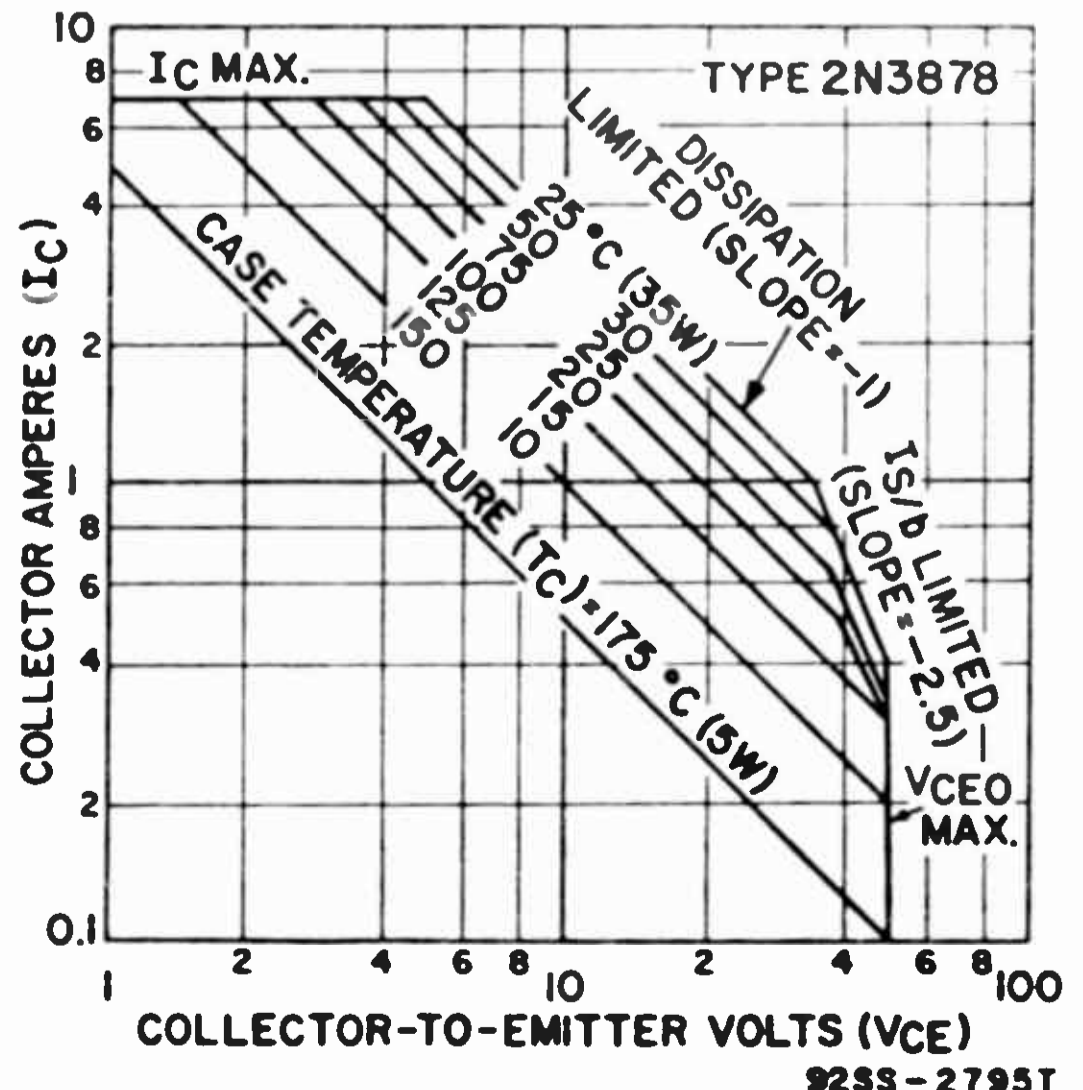
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage: $I_C = 0.2$ A, $I_B = 0$	$V_{CEO(SUS)}$	50 min	V
$I_C = 0.2$ A, $R_{BE} = 50$ Ω	$V_{CER(SUS)}$	65 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 4$ A, $I_B = 0.5$ A)	$V_{CE(sat)}$	2 max	V
Base-to-Emitter Voltage ($V_{CE} = 2$ V, $I_C = 4$ A)	V_{BE}	2.5 max	V
Collector-Cutoff Current: $V_{CE} = 40$ V, $I_B = 0$, $T_C = 25^\circ$ C	I_{CEO}	5 max	mA
$V_{CE} = 100$ V, $V_{BE} = -1.5$ V, $T_C = 25^\circ$ C	I_{CEV}	4 max	mA
$V_{CE} = 100$ V, $V_{BE} = -1.5$ V, $T_C = 150^\circ$ C	I_{CEV}	4 max	mA
Emitter-Cutoff Current ($V_{EB} = 4$ V, $I_C = 0$)	I_{EBO}	4 max	mA

MAXIMUM PULSE OPERATING AREAS



MAXIMUM DC OPERATING AREAS

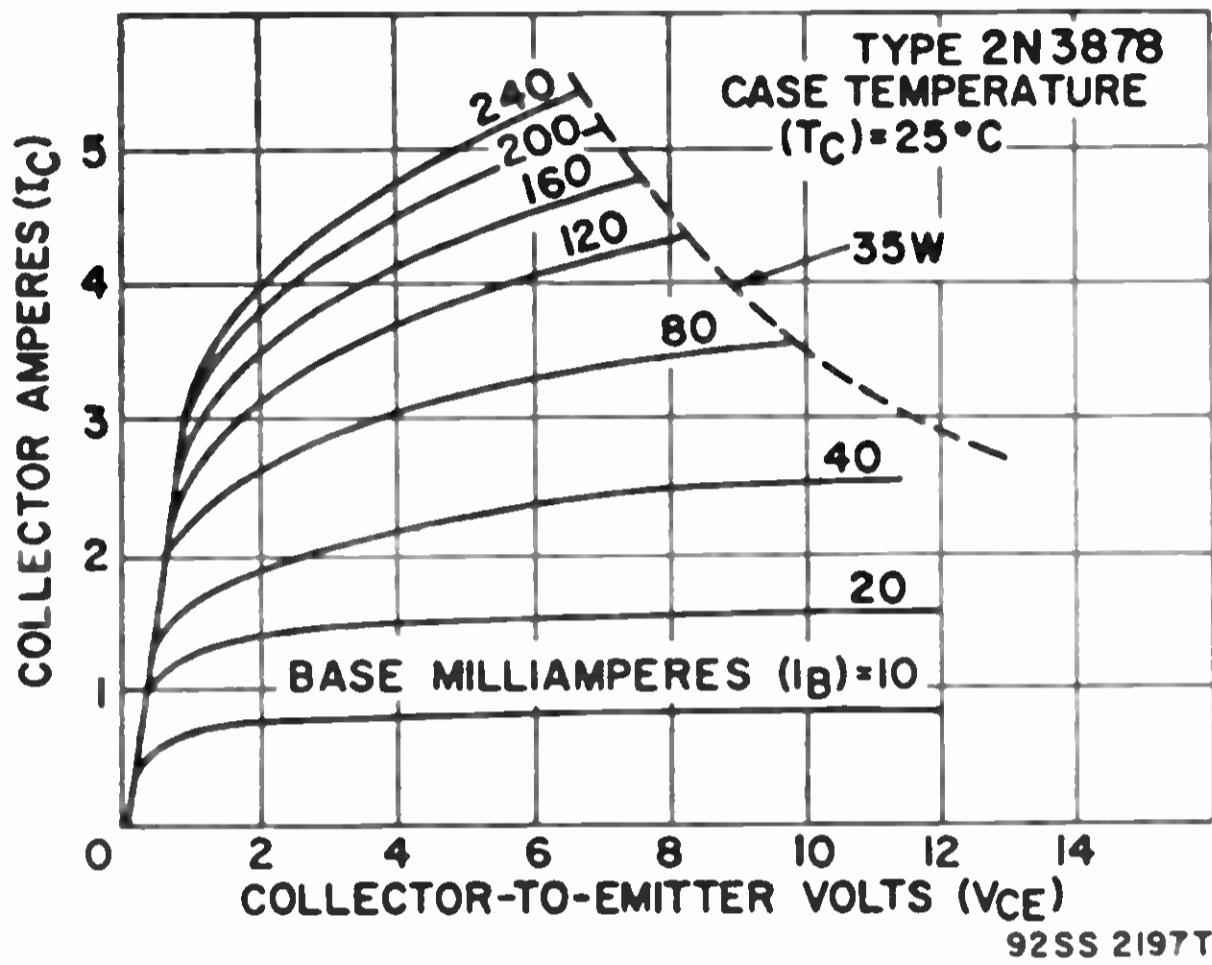


CHARACTERISTICS (cont'd)

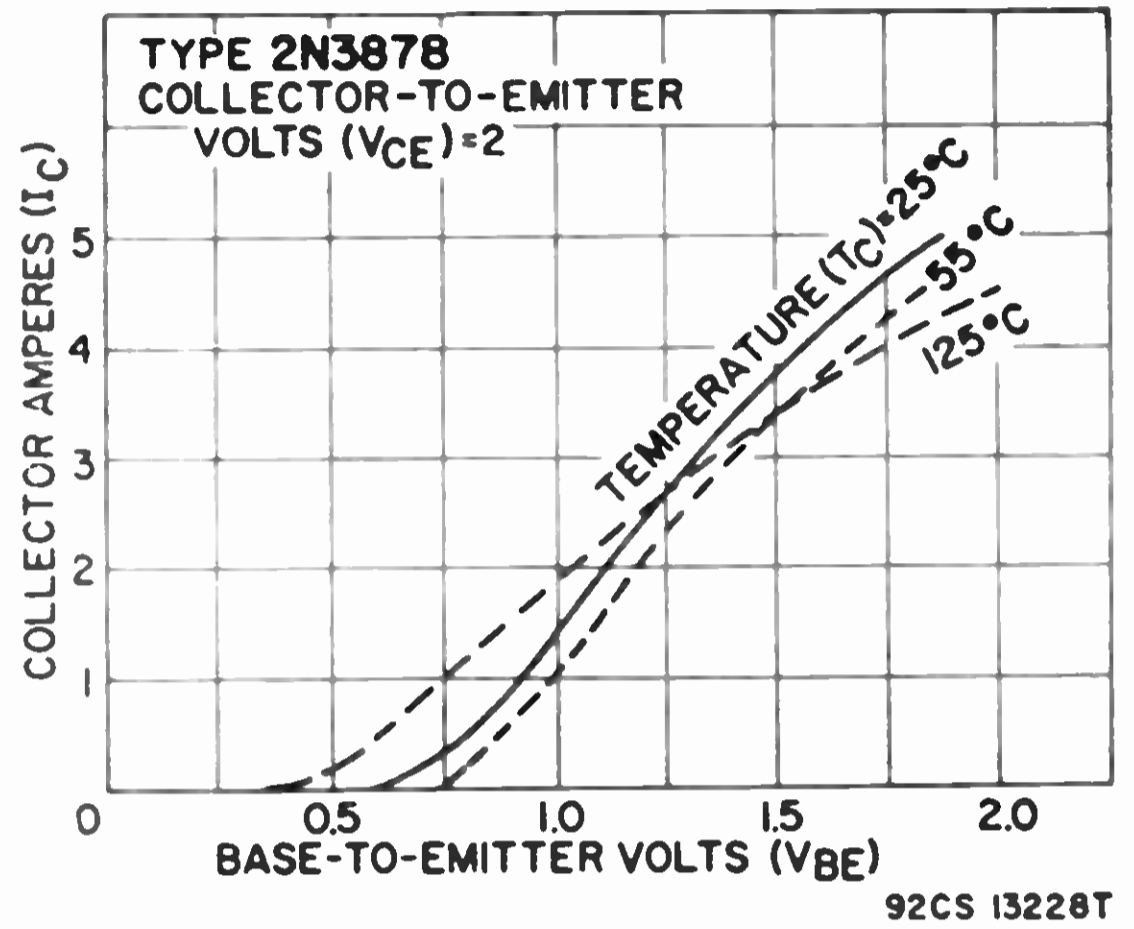
Static Forward-Current Transfer Ratio:

$V_{CE} = 5 \text{ V}, I_C = 0.5 \text{ A}$	h_{FE}	50 to 200	
$V_{CE} = 5 \text{ V}, I_C = 4 \text{ A}$	h_{FE}	20 min	
$V_{CE} = 2 \text{ V}, I_C = 4 \text{ A}$	h_{FE}	8 min	
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 10 \text{ V}, I_C = 0.5 \text{ A}, f = 10 \text{ MHz}$)	h_{fe}	6 min	
Second-Breakdown Collector Current ($V_{CE} = 40 \text{ V}$, base forward-biased)	$I_{S/b}$	750 min	mA
Second-Breakdown Energy ($R_{BE} = 50 \Omega, L = 125 \mu\text{H}$, $V_{BE} = -4 \text{ V}$, base reverse-biased)	$E_{S/b}$	1 min	mJ
Output Capacitance ($V_{CB} = 10 \text{ V}, I_E = 0$, $f = 1 \text{ MHz}$)	C_{obo}	175 max	pF
Thermal Resistance, Junction-to-Case	θ_{J-C}	5 max	$^{\circ}\text{C}/\text{W}$

TYPICAL COLLECTOR CHARACTERISTICS

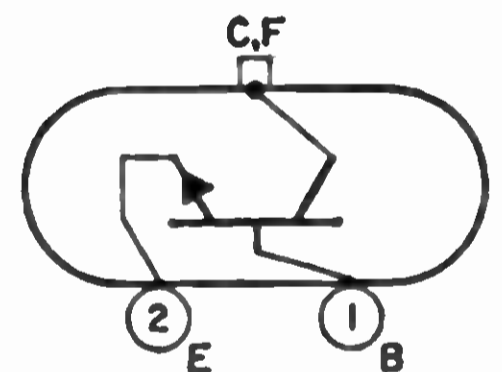


TYPICAL TRANSFER CHARACTERISTICS

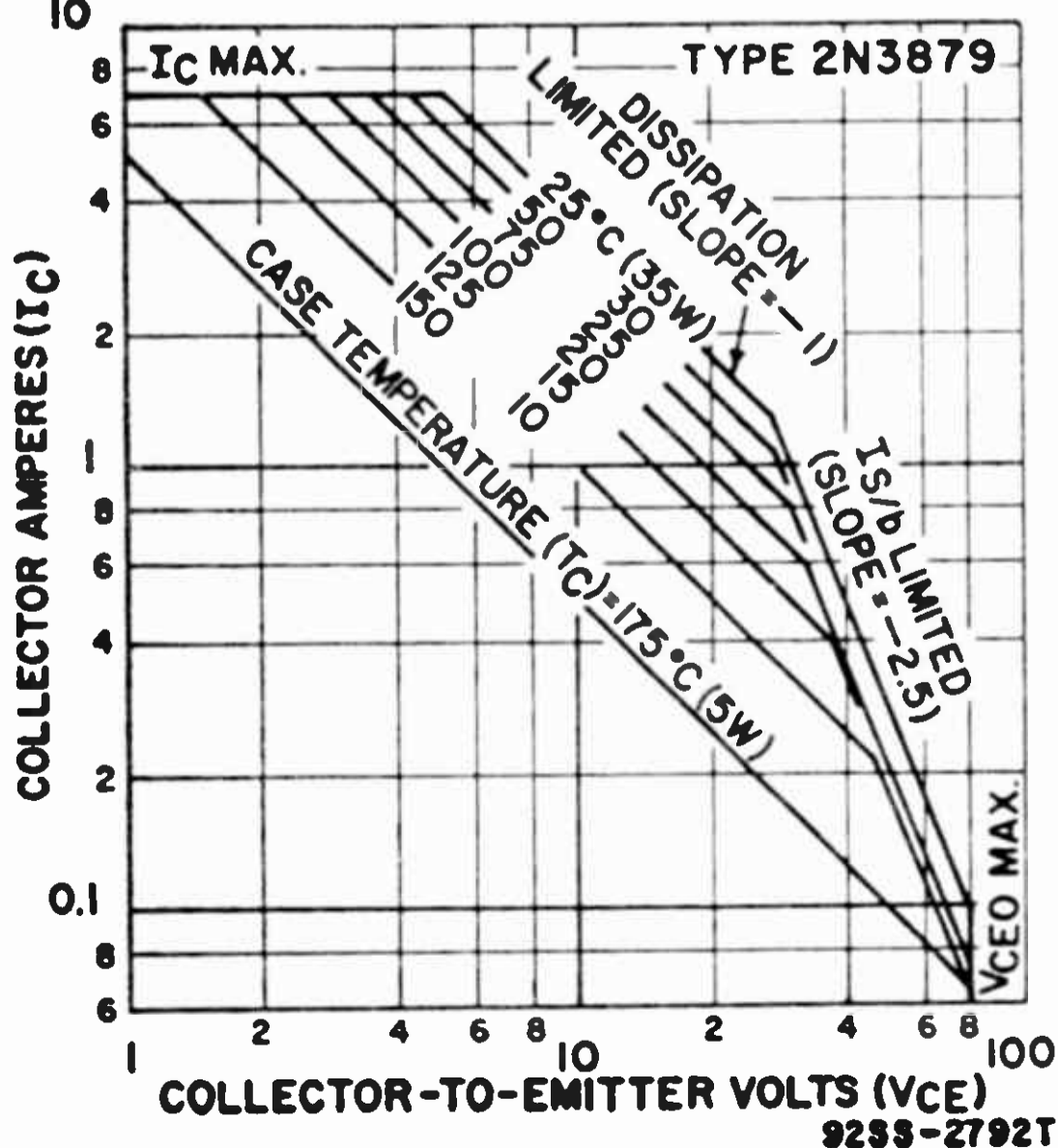


2N3879 POWER TRANSISTOR

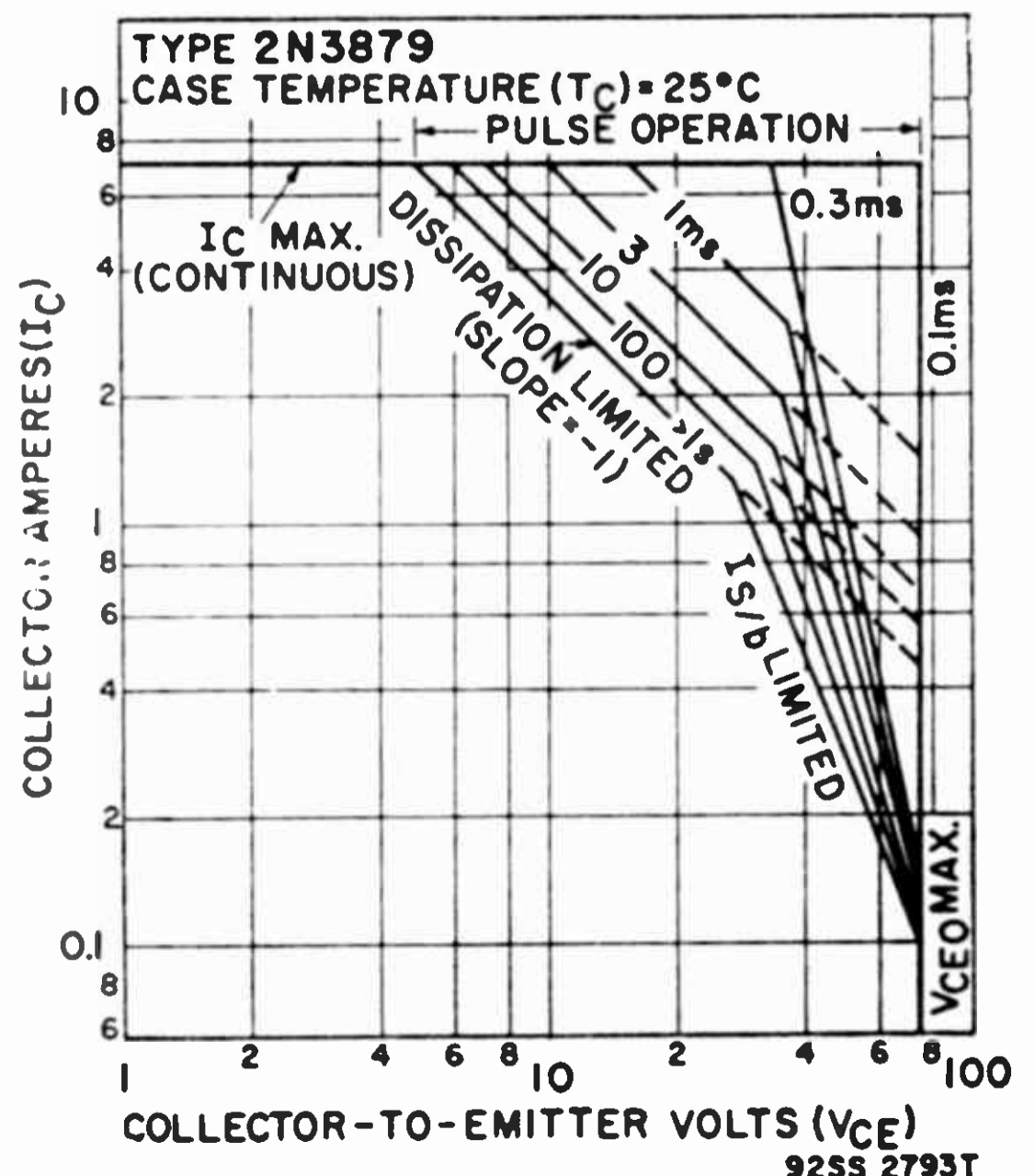
Si n-p-n epitaxial type used in af, rf, and ultrasonic applications such as low-distortion power amplifiers, oscillators, switching regulators, series regulators, converters and inverters. JEDEC TO-66, Outline No.25. See **Mounting Hardware** for desired mounting arrangement. This type is identical with type 2N3878 except for collector-to-emitter voltages of $V_{CER}(sus) = 90 \text{ V}$ and $V_{CEO}(sus) = 75 \text{ V}$, and the following items:



MAXIMUM DC OPERATING AREAS



MAXIMUM PULSE OPERATING AREAS



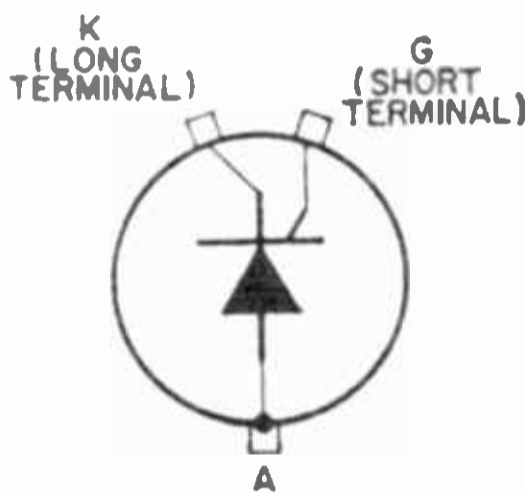
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Saturation Voltage ($I_C = 4\text{ A}, I_B = 0.4\text{ A}$)	$V_{CE(sat)}$	1.2 max	V
Base-to-Emitter Voltage ($V_{CE} = 2\text{ V}, I_C = 4\text{ A}$)	V_{BE}	1.8 max	V
Emitter-Cutoff Current ($V_{EB} = 4\text{ V}, I_C = 0$)	I_{EBO}	2 max	mA
Static Forward-Current Transfer Ratio:			
$V_{CE} = 5\text{ V}, I_C = 0.5\text{ A}$	h_{FE}	40 min	
$V_{CE} = 5\text{ V}, I_C = 4\text{ A}$	h_{FE}	20 to 80	
$V_{CE} = 2\text{ V}, I_C = 4\text{ A}$	h_{FE}	12 min	
Second-Breakdown Collector Current ($V_{CE} = 40\text{ V}$, base forward-biased)	$I_{S/b}$	500 min	mA
Delay Time ($V_{CC} = 30\text{ V}, I_C = 4\text{ A}$, $I_{B1} = 0.4\text{ A}, I_{B2} = -0.4\text{ A}$)	t_d	40 max	ns
Rise Time ($V_{CC} = 30\text{ V}, I_C = 4\text{ A}$, $I_{B1} = 0.4\text{ A}, I_{B2} = -0.4\text{ A}$)	t_r	400 max	ns
Storage Time ($V_{CC} = 30\text{ V}, I_C = 4\text{ A}$, $I_{B1} = 0.4\text{ A}, I_{B2} = -0.4\text{ A}$)	t_s	800 max	ns
Fall Time ($V_{CC} = 30\text{ V}, I_C = 4\text{ A}$, $I_{B1} = 0.4\text{ A}, I_{B2} = -0.4\text{ A}$)	t_f	400 max	ns

**2N3896-
2N3899**

**SILICON
CONTROLLED RECTIFIERS**

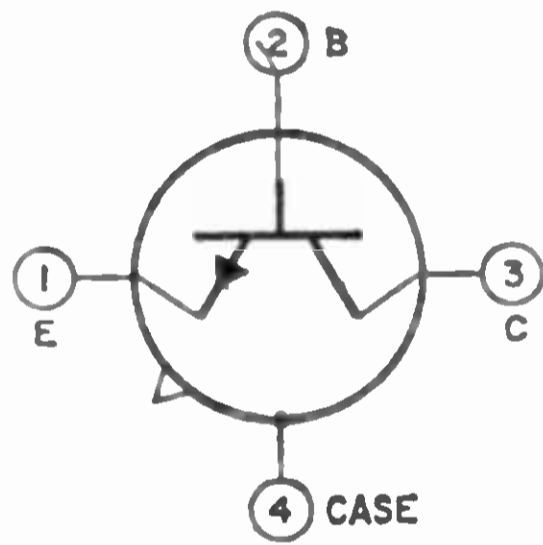
Si all-diffused three-junction types for use in power-control and power-switching applications. Outline No.32. Types 2N3896, 2N3897, 2N3898, and 2N3899 are electrically identical with types 2N3870, 2N3871, 2N3872, and 2N3873, respectively.



TRANSISTOR

2N3932

Si n-p-n epitaxial planar type for general purpose vhf-uhf applications in rf amplifiers. JEDEC TO-104, Outline No.31.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	30	V
Collector-to-Emitter Voltage	V_{CEO}	20	V
Emitter-to-Base Voltage	V_{EBO}	2.5	V
Collector Current	I_C	Limited by power dissipation	
Transistor Dissipation:			
T_A up to 25°C	P_T	200	mW
T_A above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	265	°C

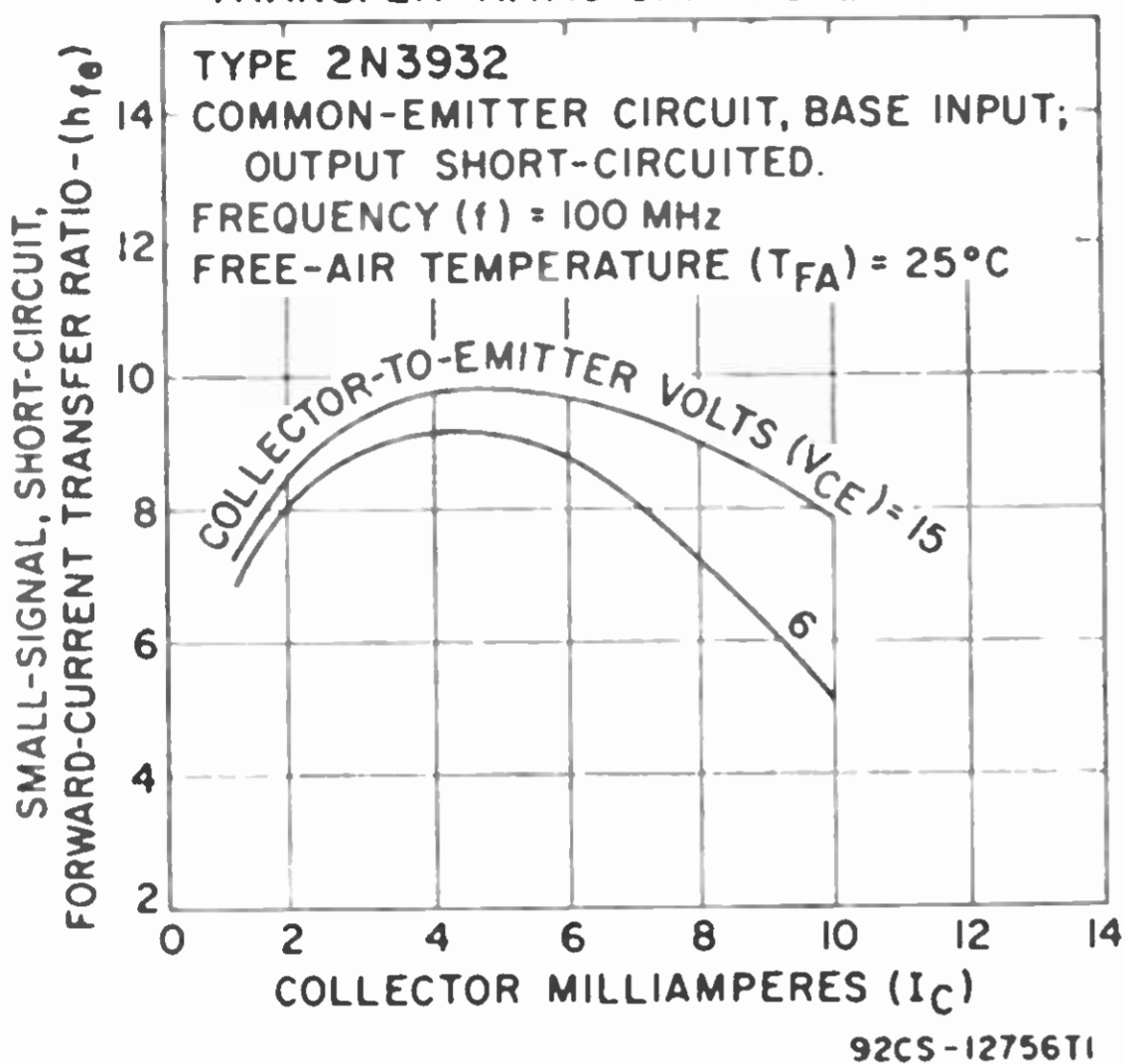
CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = 0.001\text{ mA}$, $I_E = 0$)	$V_{(BR)CBO}$	30 min	V
Collector-to-Emitter Breakdown Voltage ($I_C = 1\text{ mA}$, $I_B = 0$)	$V_{(BR)CEO}$	20 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.001\text{ mA}$, $I_C = 0$)	$V_{(BR)EBO}$	2.5 min	V
Collector-Cutoff Current ($V_{CB} = 15\text{ V}, I_E = 0$)	I_{CBO}	0.01 max	μA
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 8\text{ V}, I_C = 2\text{ mA}, f = 100\text{ MHz}$, lead No. 4 grounded)	h_{fe}	7.5 to 16	
Gain-Bandwidth Product	f_T	750 min	MHz
Collector-to-Base Time Constant ($V_{CB} = 8\text{ V}$, $I_E = 2\text{ mA}, f = 31.9\text{ MHz}$)	$\tau_{b'c}$	1 to 8	ps
Collector-to-Base Feedback Capacitance ($V_{CB} = 8\text{ V}$, $I_E = 0, f = 0.1\text{ to }1\text{ MHz}$, lead Nos. 1 and 4 connected to guard terminal)	C_{cb}	0.55 max	pF

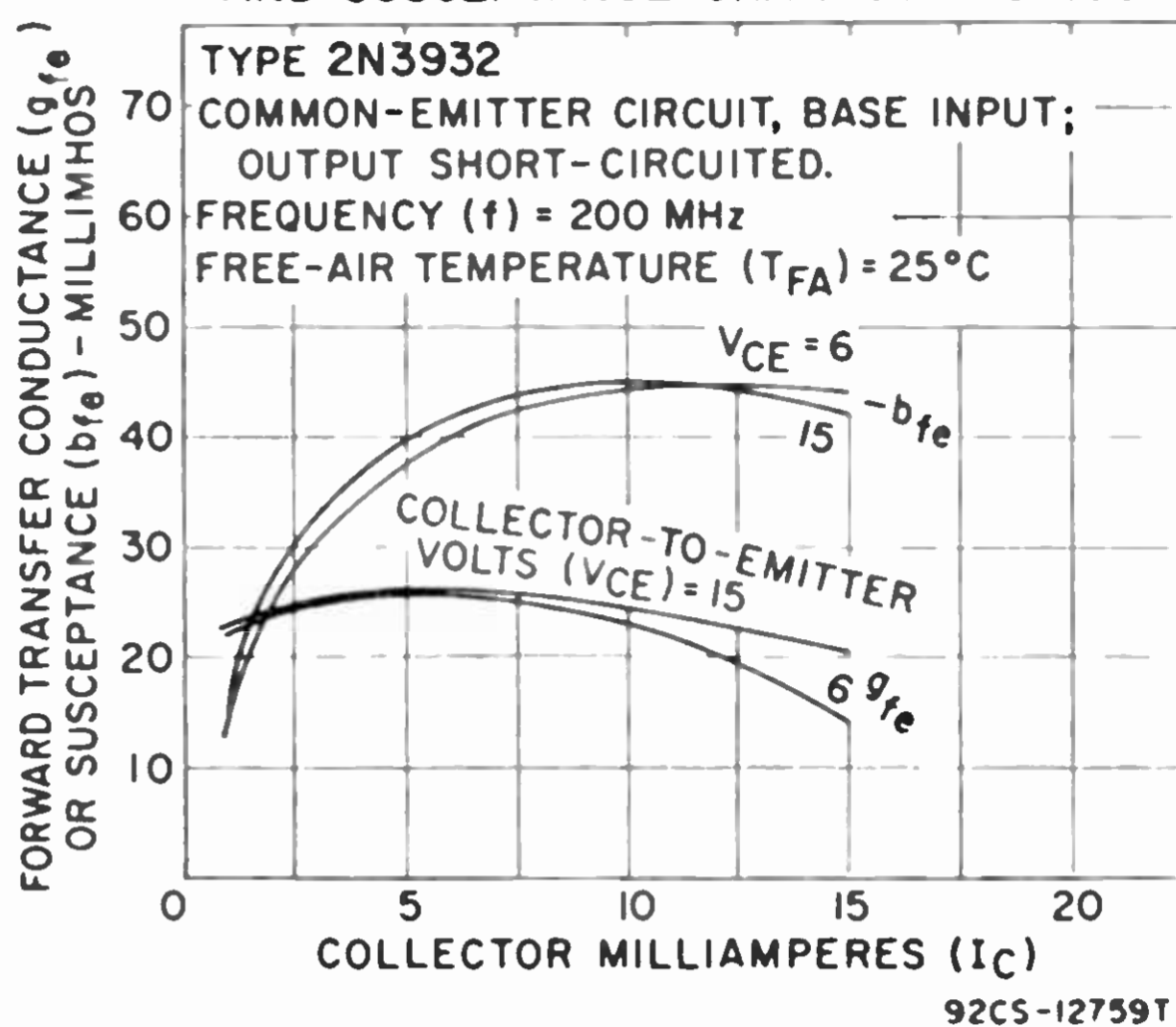
CHARACTERISTICS (cont'd)

Static Forward-Current Transfer Ratio ($V_{CE} = 8\text{ V}$, $I_c = 2\text{ mA}$)	h_{FE}	40 to 150	
Small-Signal Power Gain, Unneutralized Amplifier ($V_{CB} = 8\text{ V}$, $I_c = 2\text{ mA}$, $f = 200\text{ MHz}$, lead No. 4 grounded)	G_{pe}	11.5 to 17	dB
Noise Figure: $V_{CE} = 8\text{ V}$, $I_c = 2\text{ mA}$, $R_s = 200\ \Omega$, $f = 200\text{ MHz}$...	NF	4.5 max	dB
$V_{CE} = 6\text{ V}$, $I_c = 1.5\text{ mA}$, $R_s = 200\ \Omega$, $f = 450\text{ MHz}$	NF	5	dB

TYPICAL SMALL-SIGNAL FORWARD-CURRENT TRANSFER-RATIO CHARACTERISTICS

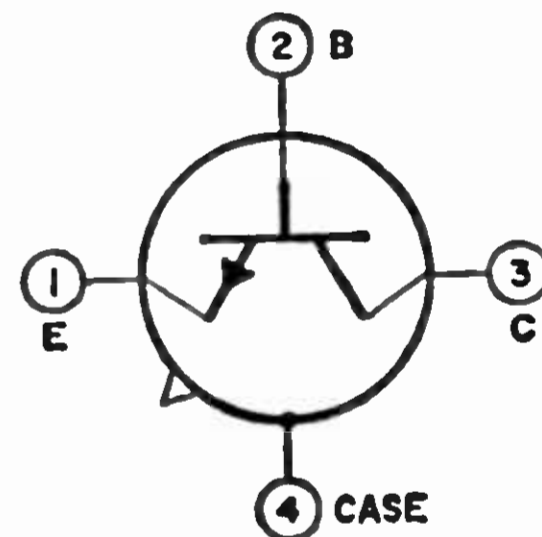


TYPICAL FORWARD TRANSFER CONDUCTANCE AND SUSCEPTANCE CHARACTERISTICS



2N3933 TRANSISTOR

Si n-p-n epitaxial planar type for general purpose vhf and uhf applications in rf amplifiers. JEDEC TO-104, Outline No.31. This type is identical with type 2N3932 except for the following items:



MAXIMUM RATINGS

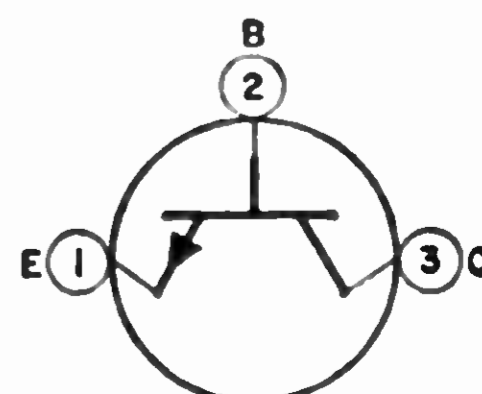
Collector-to-Base Voltage	V_{CBO}	40	V
Collector-to-Emitter Voltage	V_{CEO}	30	V

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_c = 0.001\text{ mA}$, $I_E = 0$)	$V_{(BR)CBO}$	40 min	V
Collector-to-Emitter Breakdown Voltage ($I_c = 1\text{ mA}$, $I_B = 0$)	$V_{(BR)CEO}$	30 min	V
Static Forward-Current Transfer Ratio ($V_{CE} = 8\text{ V}$, $I_c = 2\text{ mA}$)	h_{FE}	60 to 200	
Small-Signal Power Gain, Unneutralized Amplifier ($V_{CB} = 8\text{ V}$, $I_c = 2\text{ mA}$, $f = 200\text{ MHz}$, lead No. 4 grounded)	G_{pe}	14 to 18	
Collector-to-Base Time Constant ($V_{CB} = 8\text{ V}$, $I_E = 2\text{ mA}$, $f = 31.9\text{ MHz}$)	$r_b'c_c$	1 to 6	ps
Noise Figure ($V_{CE} = 8\text{ V}$, $I_c = 2\text{ mA}$, $R_s = 200\ \Omega$, $f = 200\text{ MHz}$)	NF	4 max	dB

2N4012 TRANSISTOR

Si n-p-n "overlay" epitaxial planar type designed to provide high power as a frequency multiplier into the uhf or L-band frequency region in military and industrial communications equipment. JEDEC TO-60, Outline No.23. See Mounting Hardware for desired mounting arrangement.



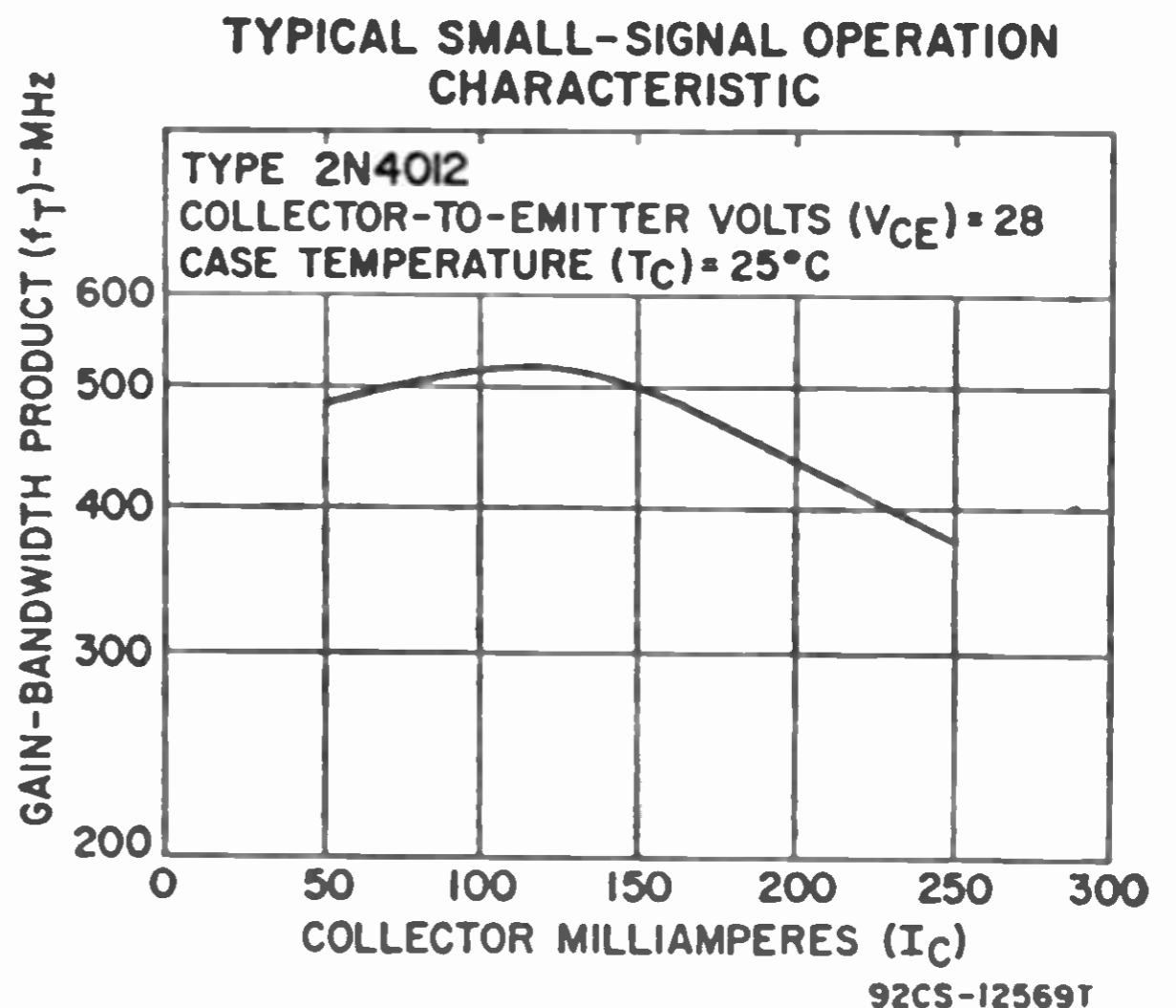
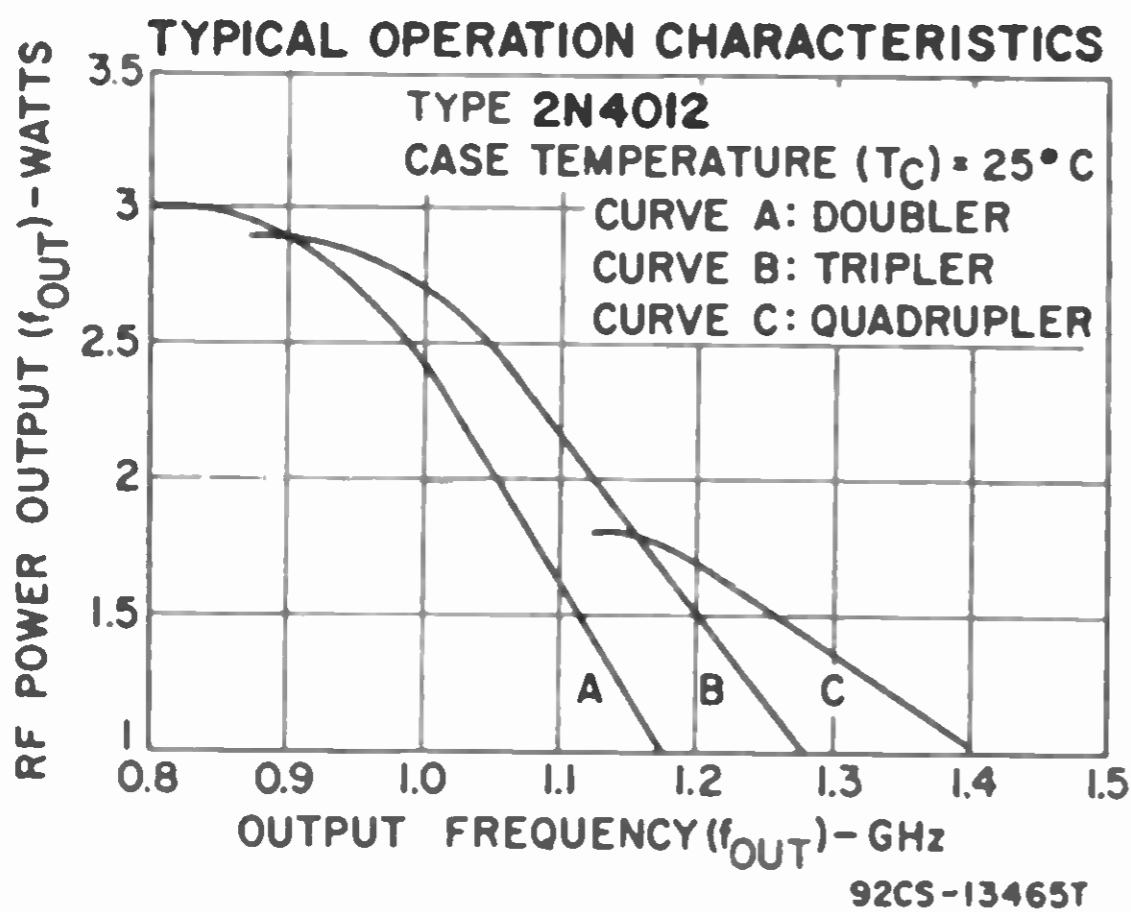
MAXIMUM RATINGS

Collector-to-Base Voltage	V _{CBO}	65	V
Collector-to-Emitter Voltage:			
V _{BE} = -1.5 V	V _{CEV}	65	V
Base open	V _{CEO}	40	V
Emitter-to-Base Voltage	V _{EBO}	4	V
Collector Current	I _C	1.5	A
Transistor Dissipation:			
T _c up to 25°C	P _T	11.6	W
T _c above 25°C	P _T	See curve page 300	
Temperature Range:			
Operating (Junction)	T _J (opr)	-65 to 200	°C
Storage	T _{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T _L	230	°C

CHARACTERISTICS

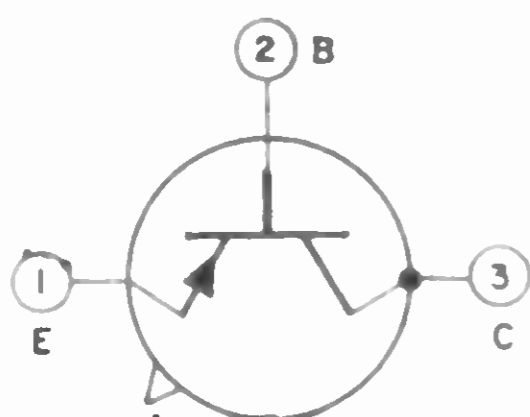
Collector-to-Base Breakdown Voltage (I _C = 0.1 mA, I _E = 0)	V _{(BR)CBO}	65 min	V
Collector-to-Emitter Breakdown Voltage:			
I _C = 0 to 200 mA, pulsed through an inductor	V _{(BR)CEO}	40 min	V
L = 25 mH, df = 50%			
V _{BE} = -1.5 V, I _C = 0 to 200 mA, pulsed through	V _{(BR)CEV}	65 min	V
an inductor L = 25 mH, df = 50%			
Emitter-to-Base Breakdown Voltage (I _E = 0.1 mA, I _C = 0)	V _{(BR)EBO}	4 min	V
Collector-to-Emitter Saturation Voltage (I _C = 500 mA, I _B = 100 mA)	V _{CE} (sat)	1 max	V
Collector-Cutoff Current (V _{CE} = 30 V, I _B = 0)	I _{CEO}	0.1 max	mA
Gain-Bandwidth Product (V _{CE} = 28 V, I _C = 150 mA)	f _T	500	MHz
Output Capacitance (V _{CB} = 30 V, I _E = 0, f = 1 MHz)	C _{obo}	10 max	pF
Collector-to-Base Cutoff Frequency* (V _{CE} = 28 V, I _C = 0)	f _c	25	GHz
RF Power Output, Multiplier:			
Tripler-V _{CE} = 28 V, f = 1002 MHz, P _{IE} = 1 W at 334 MHz	P _{OE}	2.5† min	W
Doubler-V _{CE} = 28 V, f = 800 MHz, P _{IE} = 1 W at 400 MHz	P _{OE}	3■	W

* Cutoff frequency is determined from Q measurement at 210 MHz. The cutoff frequency of the collector-to-base junction of the transistor, f_c = Q x 210 MHz.
 † For conditions given, minimum efficiency = 25 per cent.
 ■ For conditions given, minimum efficiency = 35 per cent.



POWER TRANSISTOR

2N4036



5, Outline No.5.

Si p-n-p double-diffused epitaxial planar type used in a wide variety of small-signal, medium-power, and high-speed saturated switching applications in military, industrial, and commercial equipment. The p-n-p construction permits complementary operation with a matching n-p-n type such as the 2N2102. JEDEC TO-

MAXIMUM RATINGS

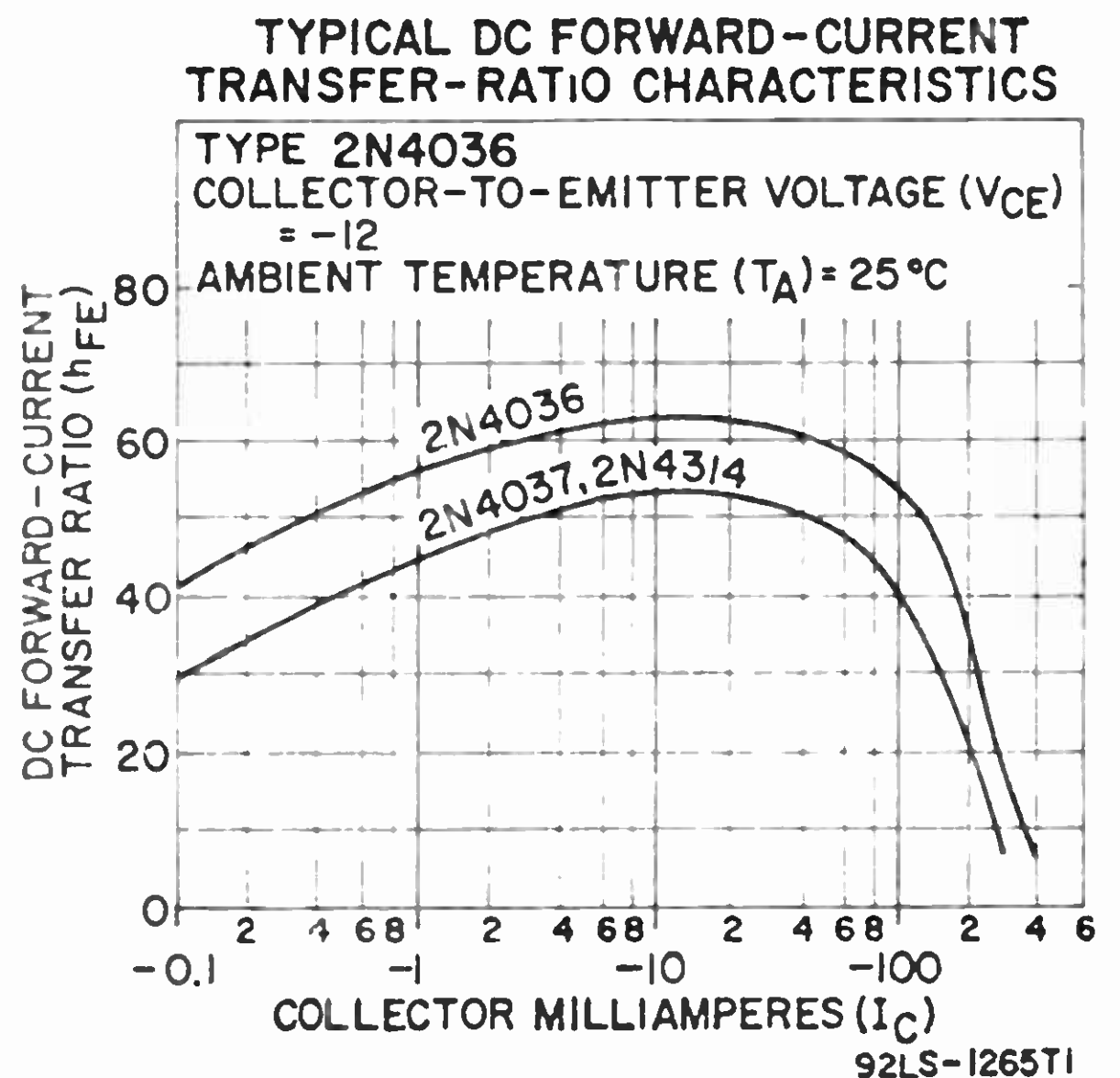
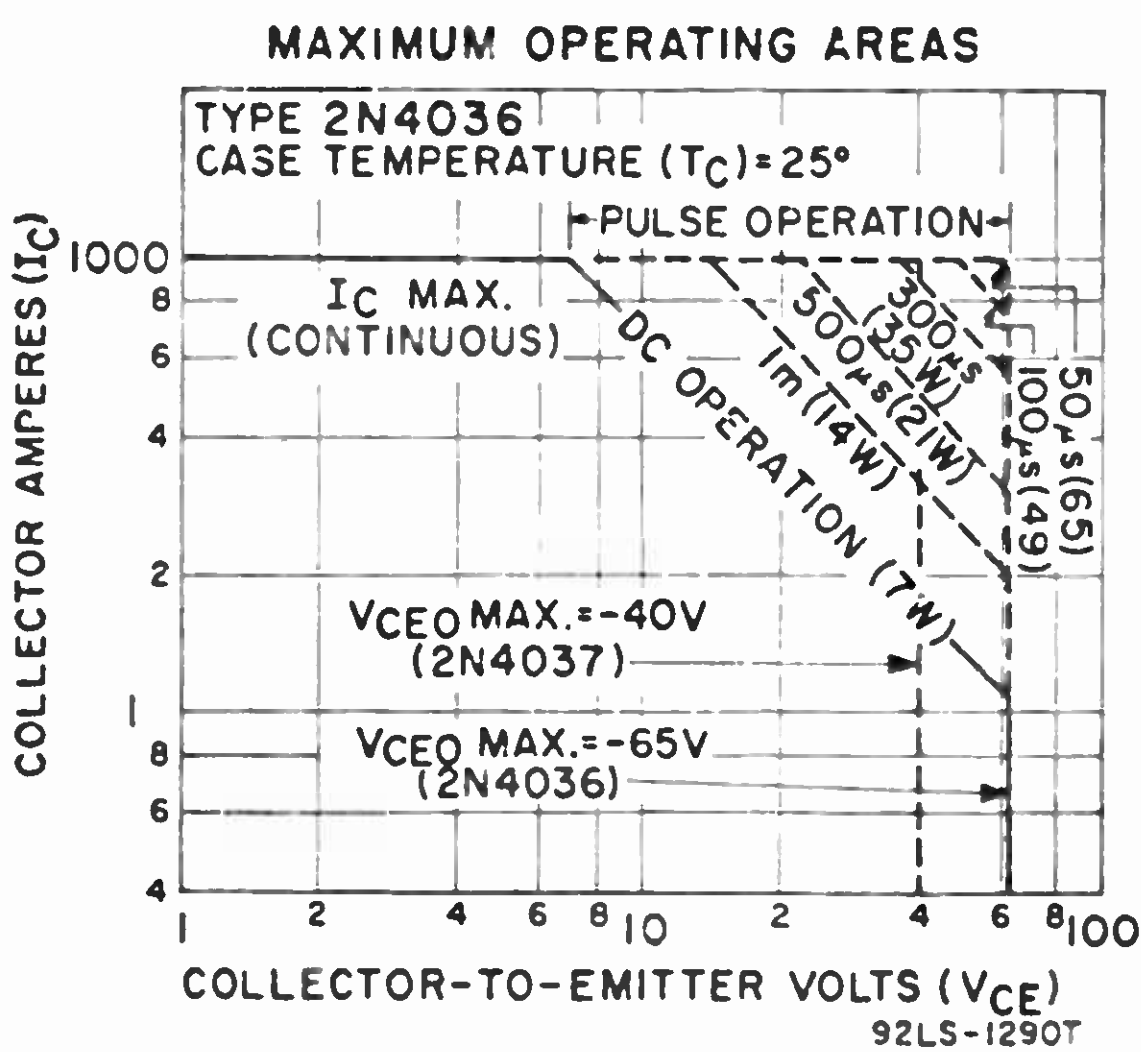
Collector-to-Base Voltage	V_{CBO}	-90	V
Collector-to-Emitter Sustaining Voltage:			
$V_{BE} = 1.5$ V	$V_{CEV(SUS)}$	-85	V
$R_{BE} \leq 200$ Ω	$V_{CER(SUS)}$	-85	V
Base open	$V_{CEO(SUS)}$	-65	V
Emitter-to-Base Voltage	V_{EBO}	-7	V
Collector Current	I_C	-1	A
Base Current	I_B	-0.5	A
Transistor Dissipation:*			
T_A up to 25°C	P_T	1	W
T_C up to 25°C	P_T	7	W
T_A or T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	230	°C

* See curve for maximum pulse operating areas.

CHARACTERISTICS (At case temperature = 25°C)

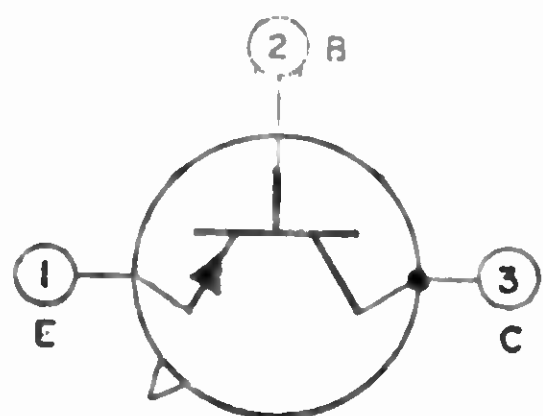
Collector-to-Base Breakdown Voltage ($I_C = 0.1$ mA, $I_E = 0$)	$V_{(BR)CBO}$	-90 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -0.1$ mA, $I_C = 0$)	$V_{(BR)EBO}$	-7 min	V
Collector-to-Emitter Sustaining Voltage:			
$V_{BE} = 1.5$ V, $I_C = -100$ mA	$V_{CEV(SUS)}$	-85 min	V
$R_{BE} \leq 200$ Ω , $I_C = -100$ mA	$V_{CER(SUS)}$	-85 min	V
$I_C = -100$ mA, $I_B = 0$	$V_{CEO(SUS)}$	-65 min	V
Collector-to-Emitter Saturation Voltage ($I_C = -150$ mA, $I_B = -15$ mA)	$V_{CE(sat)}$	-0.65 max	V
Base-to-Emitter Voltage ($V_{CE} = -10$ V, $I_C = -150$ mA)	V_{BE}	-1.1	V
Collector-Cutoff Current:			
$V_{CB} = -60$ V, $I_E = 0$	I_{CBO}	-0.02 max	μ A
$V_{CE} = -30$ V, $I_B = 0$	I_{CEO}	-0.5 max	μ A
Emitter-Cutoff Current ($V_{EB} = -5$ V, $I_C = 0$)	I_{EBO}	-0.02 max	μ A
Static Forward-Current Transfer Ratio ($V_{CE} = -10$ V, $I_C = -0.1$ mA)	h_{FE}	20 min	
Pulsed Static Forward-Current Transfer Ratio:			
$V_{CE} = -10$ V, $I_C = -150$ mA, $t_p = 300$ μ s, $df \leq 2\%$	$h_{FE}(pulsed)$	40 to 140	
$V_{CE} = -10$ V, $I_C = -500$ mA, $t_p = 300$ μ s, $df \leq 2\%$	$h_{FE}(pulsed)$	20 min	
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = -10$ V, $I_C = -50$ mA, $f = 20$ MHz)	h_{fe}	3 min	
Input Capacitance ($V_{EB} = -0.5$ V, $I_C = 0$)	C_{ibo}	90 max	pF
Output Capacitance ($V_{CB} = -10$ V, $I_E = 0$)	C_{obo}	30 max	pF
Saturated Switching Turn-On Time ($V_{CE} = -30$ V, $I_C = -150$ mA, $I_{B1} = -15$ mA, $V_{BB} \approx 4$ V)	$t_d + t_r$	110* max	ns
Saturated Switching Turn-Off Time ($V_{CE} = -30$ V, $I_C = -150$ mA, $I_{B2} = 15$ mA, $V_{BB} \approx 4$ V)	$t_s + t_f$	700* max	ns
Thermal Resistance, Junction-to-Case	θ_{J-C}	25 max	°C/W
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	165 max	°C/W

* This value does not apply to type 2N4314.



POWER TRANSISTOR

2N4037



Si p-n-p double-diffused epitaxial planar type used in a wide variety of small-signal, medium-power applications in military, industrial, and commercial equipment. The p-n-p construction permits complementary operation with a matching n-p-n type such as the 2N3053. JEDEC TO-5, Outline No.5. For maximum operating and transfer-ratio characteristics curves, refer to type 2N4036.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-60	V
Collector-to-Emitter Sustaining Voltage: $V_{BE} = 1.5$ V	$V_{CEV(SUS)}$	-60	V
$R_{BE} \leq 200$ Ω	$V_{CER(SUS)}$	-60	V
Base open	$V_{CEO(SUS)}$	-40	V
Emitter-to-Base Voltage	V_{EBO}	-7	V
Collector Current	I_C	-1	A
Base Current	I_B	-0.5	A
Transistor Dissipation:*			
T_A up to 25°C	P_T	1	W
T_C up to 25°C	P_T	7	W
T_A or T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	230	°C

* See curve for maximum pulse operating areas.

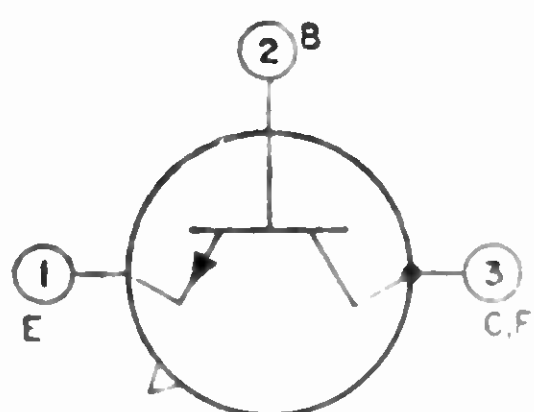
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Base Breakdown Voltage ($I_C = -0.1$ mA, $I_E = 0$)	$V_{(BR)CBO}$	-60 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -0.1$ mA, $I_C = 0$)	$V_{(BR)EBO}$	-7 min	V
Collector-to-Emitter Sustaining Voltage: $V_{BE} = 1.5$ V, $I_C = -100$ mA	$V_{CEV(SUS)}$	-60 min	V
$R_{BE} \leq 200$ Ω , $I_C = -100$ mA	$V_{CER(SUS)}$	-60 min	V
$I_C = -100$ mA, $I_B = 0$	$V_{CEO(SUS)}$	-40 min	V
Collector-to-Emitter Saturation Voltage ($I_C = -150$ mA, $I_B = -15$ mA)	$V_{CE(sat)}$	-1.4 max	V
Collector-Cutoff Current: $V_{CB} = -60$ V, $I_E = 0$	I_{CBO}	-0.25 max	μA
$V_{CE} = -30$ V, $I_B = 0$	I_{CEO}	-5 max	μA
Emitter-Cutoff Current ($V_{EB} = -5$ V, $I_C = 0$)	I_{EBO}	-1 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = -10$ V, $I_C = -1$ mA)	h_{FE}	15 min	
Pulsed Static Forward-Current Transfer Ratio ($V_{CE} = -10$ V, $I_C = -150$ mA, $t_p = 300$ μs , $df \leq 2\%$)	$h_{FE}(pulsed)$	50 to 250	
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = -10$ V, $I_C = -50$ mA, $f = 20$ MHz)	h_{fe}	3 min	
Input Capacitance ($V_{EB} = -0.5$ V, $I_C = 0$)	C_{ibo}	90 max	pF
Output Capacitance ($V_{CB} = -10$ V, $I_E = 0$)	C_{obo}	30 max	pF
Thermal Resistance, Junction-to-Case	θ_{J-C}	25 max	°C/W
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	165 max	°C/W

* This value does not apply to type 40391.

TRANSISTOR

2N4063

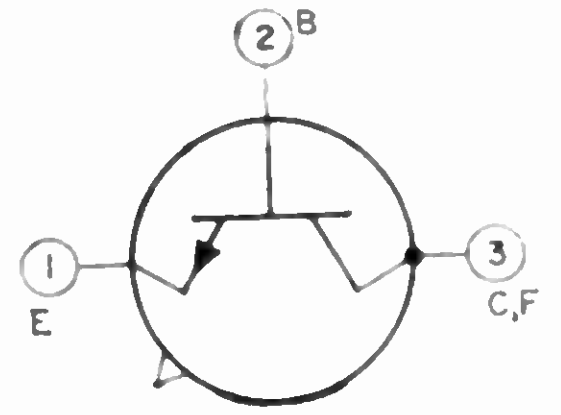


Si n-p-n triple-diffused type used in high-speed-switching and linear-amplifier applications, such as high-voltage differential and operational amplifiers, high-voltage inverters, and series regulators for industrial and military applications. JEDEC TO-5 (with flange), Outline No.6. See Mounting Hardware for desired mounting arrangement. This type is electrically identical with type 2N3439.

This type is electrically identical with type 2N3439.

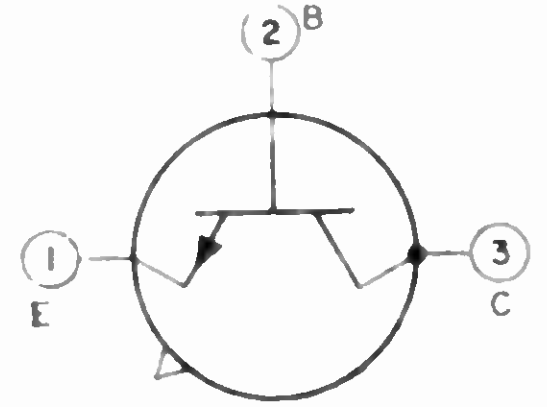
2N4064 TRANSISTOR

Si n-p-n triple diffused type used in high-speed-switching and linear-amplifier applications, such as high-voltage differential and operational amplifiers, high-voltage inverters, and series regulators for industrial and military applications. JEDEC TO-5 (with flange), Outline No.6. See Mounting Hardware for desired mounting arrangement. This type is electrically identical with type 2N3440.



2N4068 TRANSISTOR

Si n-p-n type used in wide-band-amplifier and relay-driver applications in critical industrial equipment such as video amplifiers, television cameras, camera chains, monitors, oscilloscopes, and neon-indicator drivers. JEDEC TO-104, Outline No.32.

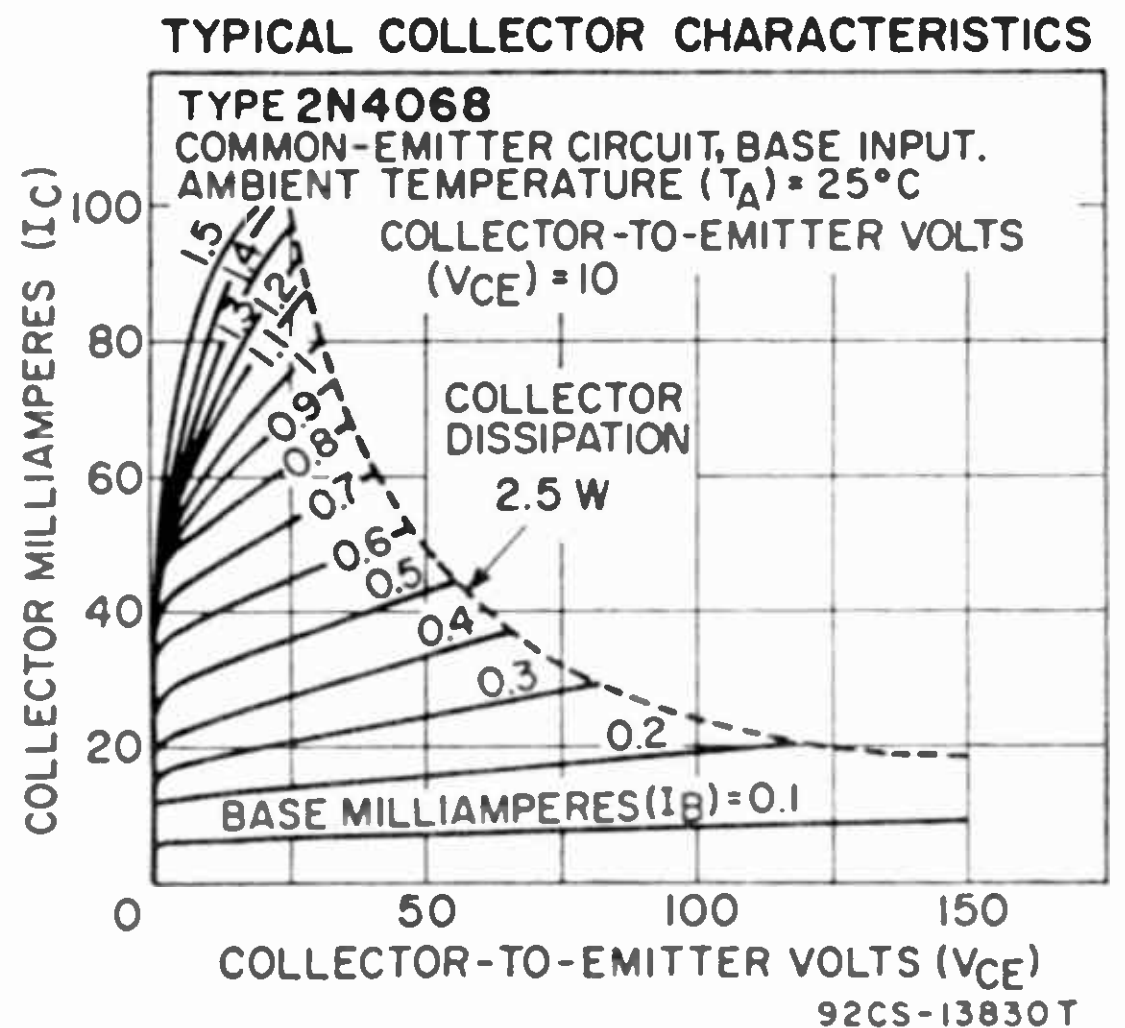
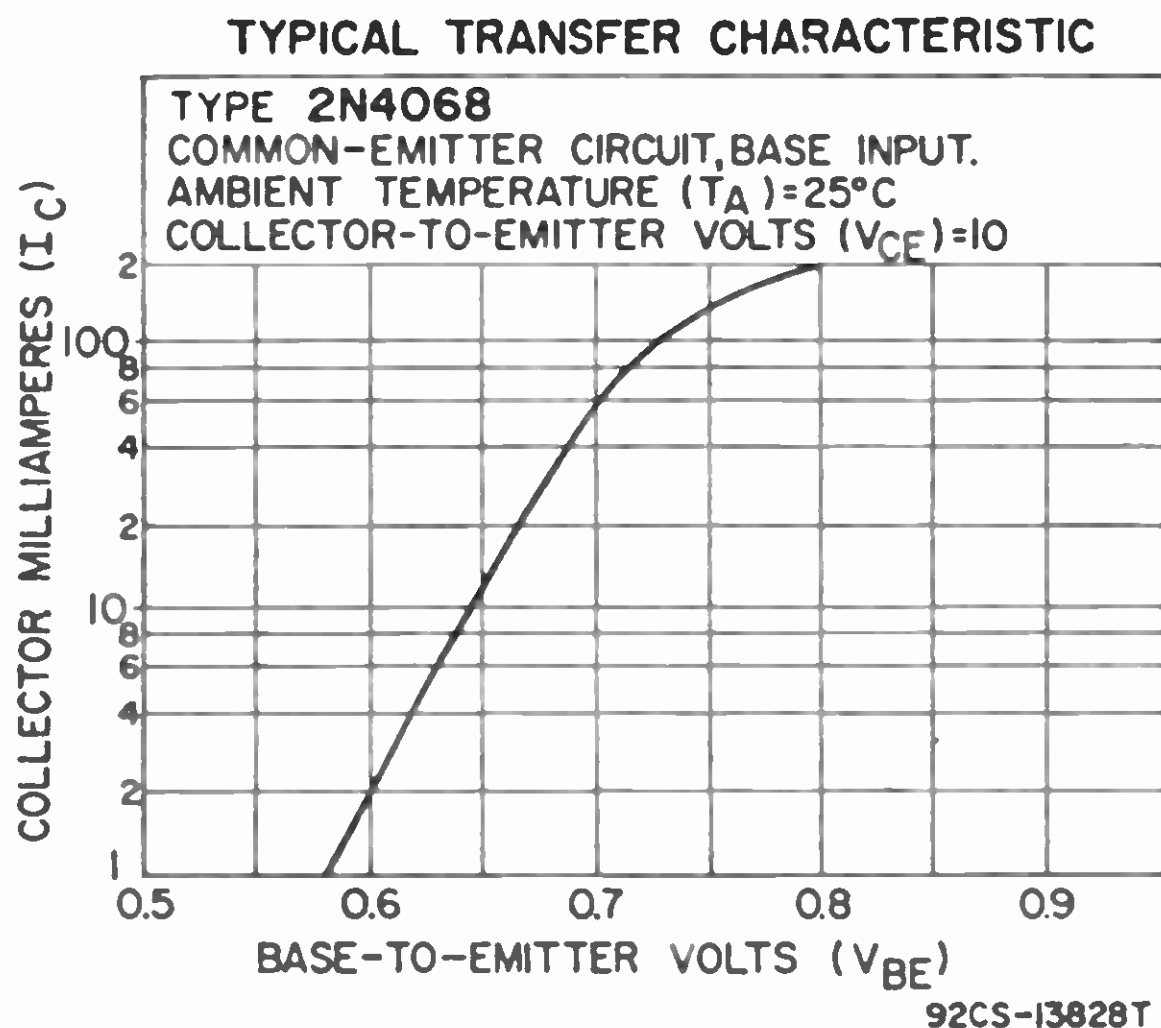


MAXIMUM RATINGS

Collector-to-Emitter Voltage	V_{CE0}	150	V
Emitter-to-Base Voltage	V_{EB0}	5	V
Collector-Current	I_C	200	mA
Transistor Dissipation:			
T_A up to 25°C	P_T	0.5	W
T_A above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 175	°C
Storage	T_{STG}	-65 to 175	°C
Lead-Soldering Temperature (10 s max)	T_L	255	°C

CHARACTERISTICS

Collector-to-Emitter Breakdown Voltage ($I_C = 1$ mA, $I_B = 0$)	$V_{(BR)CE0}$	150 min; 180 typ	V
Emitter-to-Base Breakdown Voltage ($I_E = -10$ μ A, $I_C = 0$)	$V_{(BR)EB0}$	5 min; 7 typ	V
Collector-to-Emitter Saturation Voltage ($I_C = 30$ mA, $I_B = 1$ mA)	$V_{CE(sat)}$	1 typ; 3 max.	V
Base-to-Emitter Saturation Voltage ($I_C = 30$ mA, $I_B = 1$ mA)	$V_{BE(sat)}$	0.68	V
Collector-Cutoff Current ($V_{CB} = 120$ V, $I_E = 0$)	I_{CBO}	5 typ; 50 max	nA
Static Forward-Current Transfer Ratio ($V_{CE} = 10$ V, $I_C = 30$ mA)	h_{FE}	30 min; 70 typ	
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 10$ V, $I_C = 30$ mA, $f = 1$ kHz)	h_{fe}	80	
Gain-Bandwidth Product:			
$V_{CE} = 10$ V, $I_C = 30$ mA, $f = 100$ MHz	f_T	50 min; 100 typ	MHz
$V_{CE} = 140$ V, $I_C = 2$ mA, $f = 100$ MHz	f_T	50 min; 100 typ	MHz



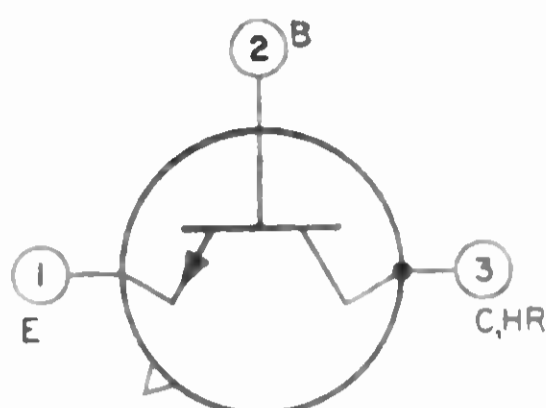
CHARACTERISTICS (cont'd)

Output Capacitance* ($V_{CE} = 10\text{ V}$, $I_C = 0$, $f = 1\text{ MHz}$)	C_{obo}	2.8 typ; 3.5 max	pF
Thermal Resistance, Junction-to-Case	θ_{J-C}	45 typ; 60 max	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	300 max	$^{\circ}\text{C/W}$

* Three-terminal measurement with lead No. 1 (emitter) and lead No. 3 (case) connected to guard terminal.

TRANSISTOR

2N4069



Si n-p-n type used in wide-band-amplifier and relay-driver applications in critical industrial equipment such as video amplifiers, television cameras, camera chains, monitors, oscilloscopes, and neon-indicator drivers. JEDEC TO-104 (with heat radiator), Outline No.33. This type is electrically identical with type 2N4068

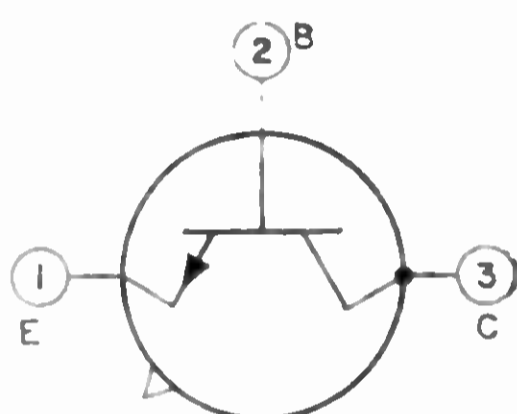
except for the following items:

MAXIMUM RATINGS

Transistor Dissipation:	P_T	1	W
T_A up to 25°C	P_T	See curve page 300	
T_A above 25°C			

CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient	θ_{J-A}	150 max	$^{\circ}\text{C/W}$
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TRANSISTOR

2N4074

Si n-p-n epitaxial planar type used in high-voltage, high-current audio and video amplifier service in commercial and industrial equipment. JEDEC TO-104, Outline No.32.

MAXIMUM RATINGS

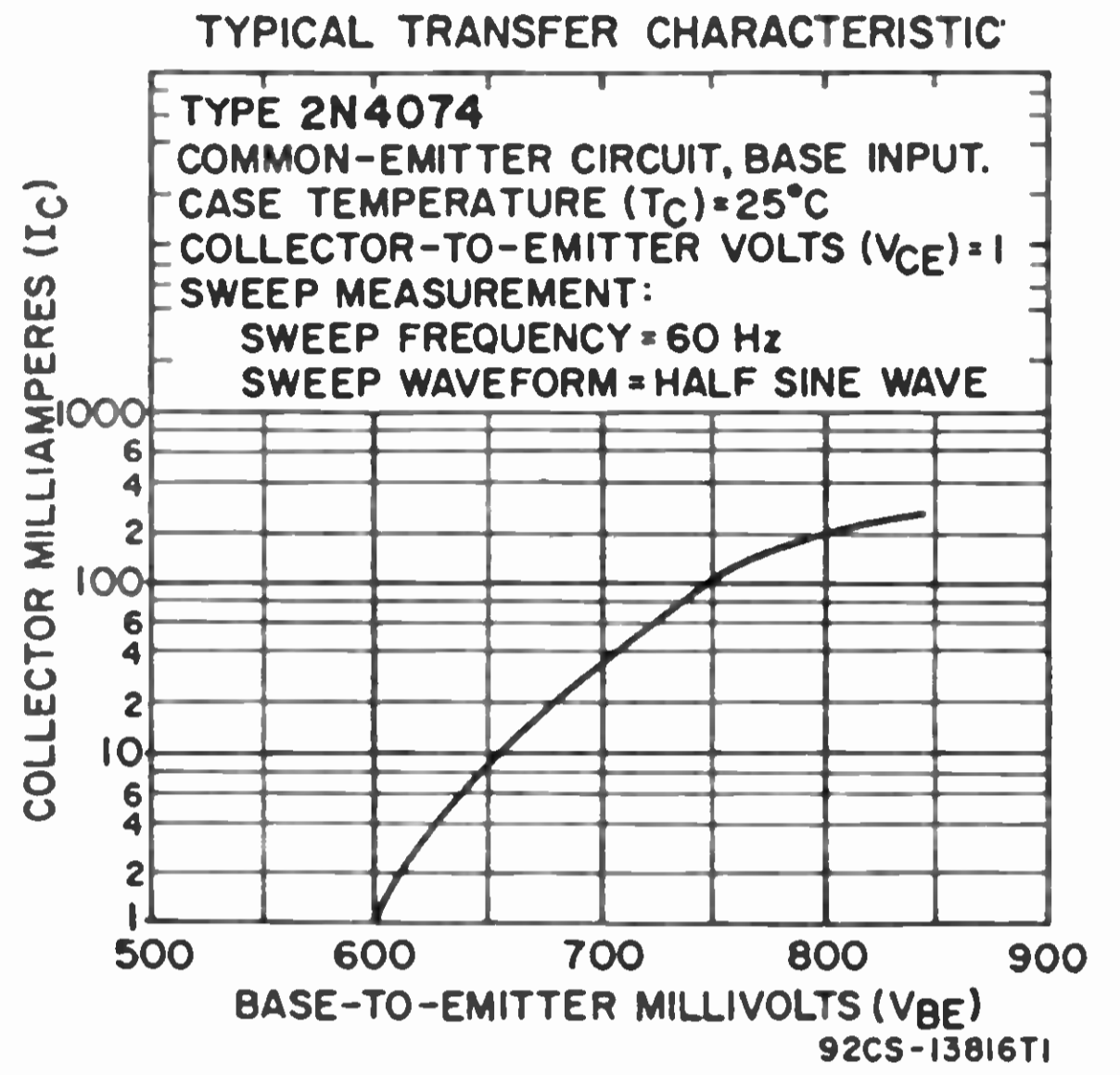
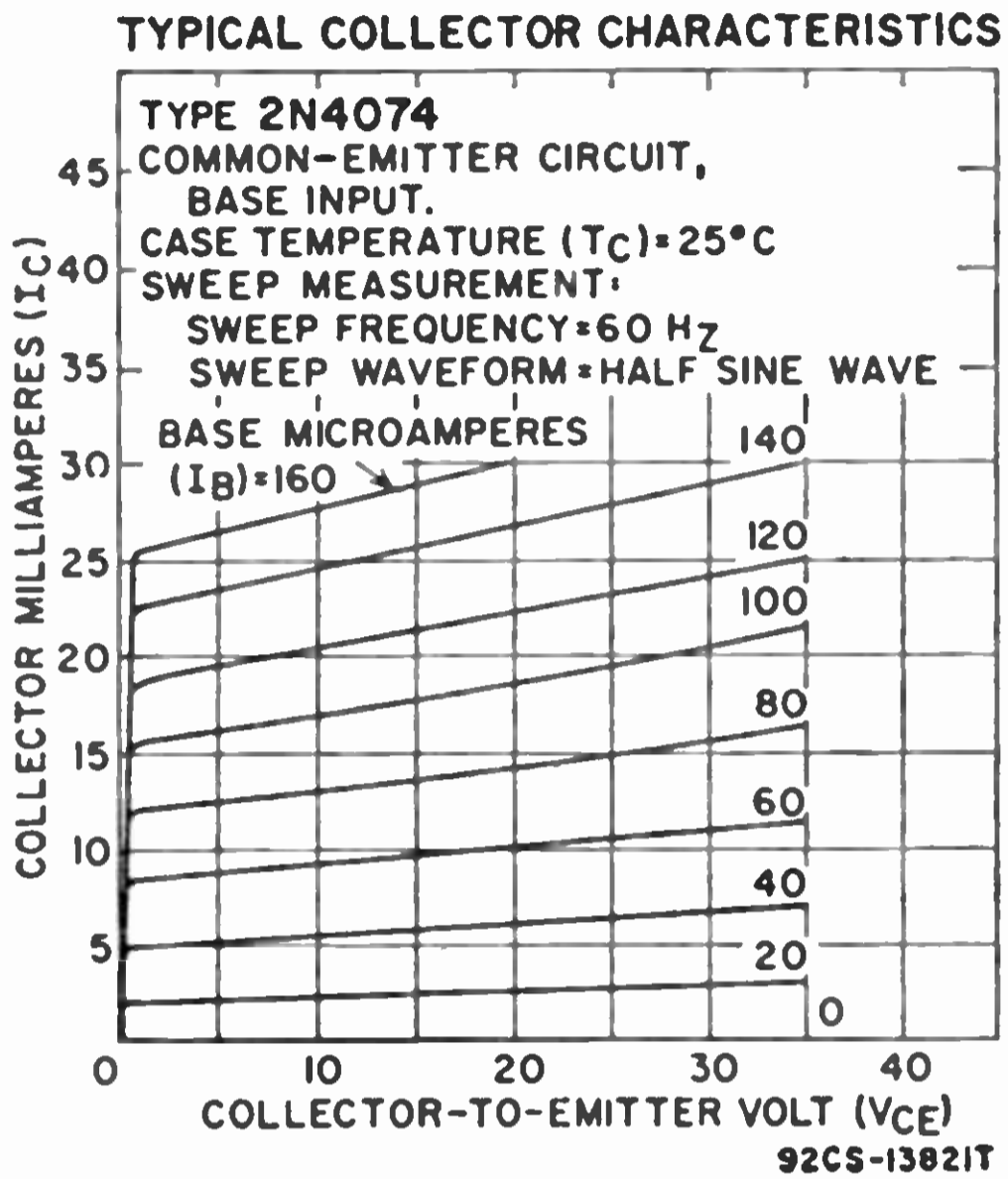
Collector-to-Emitter Voltage:	V_{CEV}	40	V
$V_{BE} = -1\text{ V}$	V_{CEO}	40	V
Base open	V_{EBO}	8	V
Emitter-to-Base Voltage	I_C	300	mA
Collector Current	I_E	-300	mA
Emitter Current	P_T	2	W
Transistor Dissipation:	P_T	See curve page 300	
T_C up to 75°C	P_T	0.5	W
T_C above 75°C	P_T	See curve page 300	
T_A up to 25°C			
T_A above 25°C			
Temperature Range:	$T_J(\text{opr})$	-65 to 175	$^{\circ}\text{C}$
Operating (Junction)	T_{STG}	-65 to 175	$^{\circ}\text{C}$
Storage	T_L	255	$^{\circ}\text{C}$
Lead-Soldering Temperature (10 s max)			

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	40 min	V
($I_C = 10\text{ mA}$, $I_B = 0$)	$V_{(BR)EBO}$	8 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.05\text{ mA}$, $I_C = 0$)	$V_{CE(\text{sat})}$	0.22 typ; 0.3 max	V
Collector-to-Emitter Saturation Voltage ($I_C = 300\text{ mA}$, $I_B = 15\text{ mA}$)	$V_{BE(\text{sat})}$	1 typ; 1.5 max	V
Base-to-Emitter Saturation Voltage ($I_C = 300\text{ mA}$, $I_B = 15\text{ mA}$)	I_{CBO}	10 max	nA
Collector-Cutoff Current:	I_{CBO}	1 max	μA
$V_{CB} = 25\text{ V}$, $I_E = 0$	I_{CEV}	10 max	μA
$V_{CB} = 25\text{ V}$, $I_E = 0$, $T_C = 85^{\circ}\text{C}$	I_{EBO}	10 max	nA
$V_{CE} = 40\text{ V}$, $V_{BE} = 1\text{ V}$	h_{FE}	35 min; 75 typ	
Emitter-Cutoff Current ($V_{BE} = -2.5\text{ V}$, $I_C = 0$)	h_{FE}	75 to 300	
Static Forward-Current Transfer Ratio:	h_{FE}	50 min; 140 typ	
$V_{CE} = 6\text{ V}$, $I_C = 0.5\text{ mA}$			
$V_{CE} = 10\text{ V}$, $I_C = 10\text{ mA}$			
$V_{CE} = 1\text{ V}$, $I_C = 100\text{ mA}$	h_{fe}	75 min; 175 typ	
Small-Signal Forward-Current Transfer Ratio			
($V_{CE} = 12\text{ V}$, $I_C = 10\text{ mA}$, $f = 1\text{ kHz}$)			

CHARACTERISTICS (cont'd)

Gain-Bandwidth Product ($V_{CE} = 6\text{ V}$, $I_C = 1\text{ mA}$, $f = 100\text{ MHz}$)	f_T	50 min; 80 typ	MHz
Intrinsic Base-Spreading Resistance ($V_{CE} = 6\text{ V}$, $I_C = 1\text{ mA}$, $f = 100\text{ MHz}$)	$r_{bb'}$	20 typ; 40 max	Ω
Output Capacitance ($V_{CB} = 6\text{ V}$, $I_E = 0$, $f = 1\text{ MHz}$)	C_{obo}	12 typ; 20 max	pF
Small-Signal Input Impedance ($V_{CE} = 12\text{ V}$, $I_C = 10\text{ mA}$, $f = 1\text{ kHz}$)	h_{ie}	600	Ω
Small-Signal Output Admittance ($V_{CE} = 12\text{ V}$, $I_C = 10\text{ mA}$, $f = 1\text{ kHz}$)	h_{oe}	75	μmhos
Small-Signal Reverse-Voltage Transfer Ratio ($V_{CE} = 12\text{ V}$, $I_C = 10\text{ mA}$, $f = 1\text{ kHz}$)	h_{re}	125×10^{-6}	
Thermal Resistance, Junction-to-Case	θ_{J-C}	50 max	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	300 max	$^{\circ}\text{C/W}$



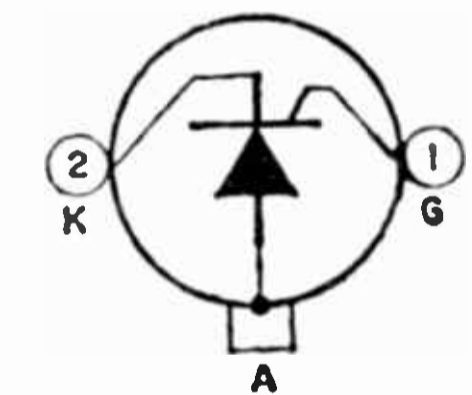
2N4081

Refer to Chart of Discontinued Transistors

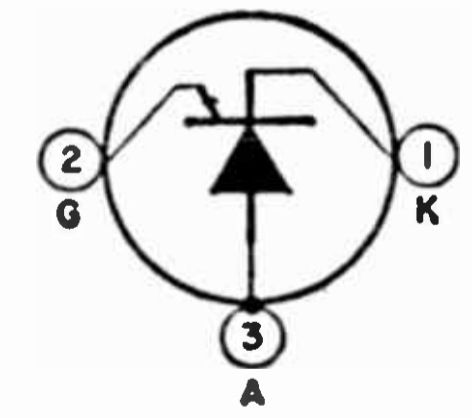
2N4101
2N4102

SILICON CONTROLLED RECTIFIERS

Si all-diffused three-junction types for use in power-control and power-switching applications. 2N4101: JEDEC TO-66, Outline No.25. 2N4102: JEDEC TO-8, Outline No.10. For type 2N4101, see Mounting Hardware for desired mounting arrangement. For rating chart for type 2N4102, refer to type 2N3528. These types are identical with type 2N3228 except for the following items:



2N4101



2N4102

MAXIMUM RATINGS (For sinusoidal ac supply voltage at $f = 50$ to 400 Hz with resistive or inductive load)

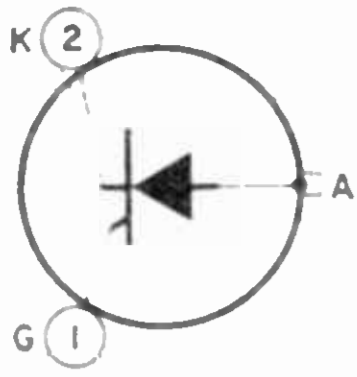
	2N4101		2N4102	
V_{RSOM}	_____	700	_____	V
V_{RROM}	_____	600	_____	V
V_{DROM}	_____	700	_____	V
$I_{T(AV)}$ (conduction angle = 180° , $T_C = 75^{\circ}\text{C}$)	3.2		_____	A
$I_{T(AV)}$ (conduction angle = 180° , $T_A = 25^{\circ}\text{C}$)	_____		1.3	A
$I_{T(RMS)}$ ($T_A = 25^{\circ}\text{C}$)	_____		2	A
$I_{T(RMS)}$ ($T_C = 75^{\circ}\text{C}$)	5		_____	A

CHARACTERISTICS (At maximum electrical ratings at $T_C = 25^{\circ}\text{C}$)

$V_{F(BO)O}$ ($T_C = 100^{\circ}\text{C}$)	_____	600 min	_____	V
I_{DOM} ($V_{DO} = V_{F(BO)O}$, $T_C = 100^{\circ}\text{C}$)	_____	0.4 typ; 4 max	_____	mA
I_{RROM} ($V_{RO} = V_{RSOM}$, $T_C = 100^{\circ}\text{C}$)	_____	0.2 typ; 2 max	_____	mA
θ_{J-A}	_____		40 max	$^{\circ}\text{C/W}$

**SILICON
CONTROLLED RECTIFIER**

2N4103



Si all-diffused three-junction type for use in power-control and power-switching applications. See Mounting Hardware for desired mounting arrangement. JEDEC TO-3, Outline No.2. This type is identical with type 2N3668 except for the following items:

MAXIMUM RATINGS (For sinusoidal ac supply voltage at $f = 50$ to 400 Hz with resistive or inductive load)

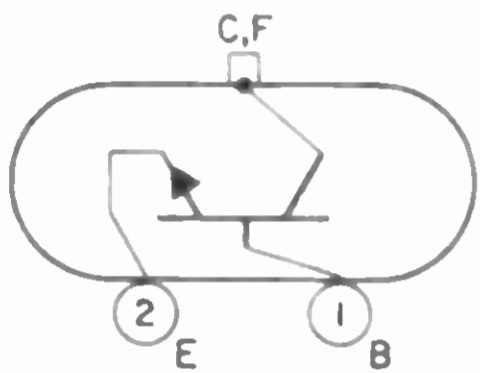
V_{RSOM}	700	V
V_{RROM}	600	V
V_{DROM}	700	V

CHARACTERISTICS (At maximum electrical ratings at $T_c = 25^\circ\text{C}$)

$V_{F(BO)}$ ($T_c = 100^\circ\text{C}$)	600 min	V
I_{DOM} ($V_{DO} = V_{F(BO)}$ min value, $T_c = 100^\circ\text{C}$)	0.35 typ; 4 max	mA
I_{RROM} ($V_{RO} = V_{RROM}$)	0.3 typ; 3 max	mA

TRANSISTOR

2N4240

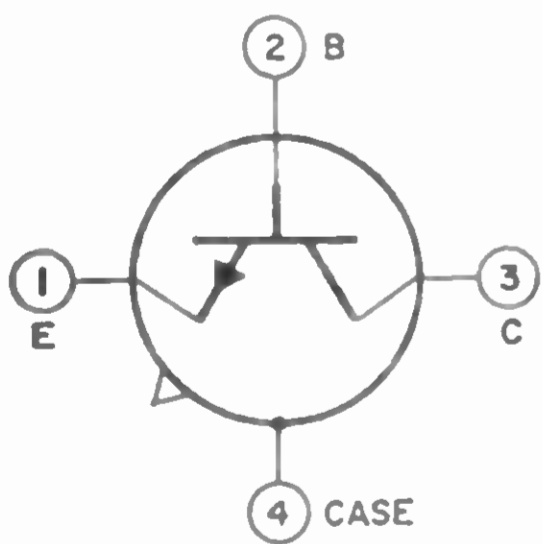


Si n-p-n triple-diffused type used in high voltage, high-speed-switching and linear-amplifier applications such as operational amplifiers, switching regulators, converters, inverters, deflection and high-fidelity amplifiers. JEDEC TO-66, Outline No.25. See Mounting Hardware for desired mounting arrangement. This type

is identical with type 2N3585 except for the following items:

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Saturation Voltage ($I_c = 750$ mA, $I_B = 75$ mA)	$V_{BE(sat)}$	1 max	V
Collector-Cutoff Current: $V_{CE} = 150$ V, $I_B = 0$	I_{CEO}	5 max	mA
$V_{CE} = 400$ V, $V_{BE} = -1.5$ V	I_{CEV}	2 max	mA
$V_{CE} = 300$ V, $V_{BE} = -1.5$ V, $T_c = 150^\circ\text{C}$	I_{CEV}	5 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 10$ V, $I_c = 750$ mA)	h_{FE}	30 to 150	
Second Breakdown Energy ($R_{BE} = 20 \Omega$, $L = 100 \mu\text{H}$, $V_{BE} = -4$ V)	$E_{s/b}$	50 min	μJ



TRANSISTOR

2N4259

Si n-p-n epitaxial planar type used in vhf and uhf applications in industrial and military equipment. JEDEC TO-104, Outline No.31. See Mounting Hardware for desired mounting arrangement.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	40	V
Collector-to-Emitter Voltage	V_{CEO}	30	V
Emitter-to-Base Voltage	V_{EBO}	2.5	V
Collector Current	I_c	Limited by dissipation	
Transistor Dissipation: T_A up to 25°C	P_T	175	mW
T_A above 25°C	P_T	See curve page 300	
Temperature Range: Operating (Junction)	$T_J(\text{opr})$	-65 to 175	$^\circ\text{C}$
Storage	T_{STG}	-65 to 175	$^\circ\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	265	$^\circ\text{C}$

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_c = 0.001$ mA, $I_E = 0$)	$V_{(BR)CBO}$	40 min	V
Collector-to-Emitter Breakdown Voltage ($I_c = 1$ mA)	$V_{(BR)CEO}$	30 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.001$ mA, $I_c = 0$)	$V_{(BR)EBO}$	2.5 min	V

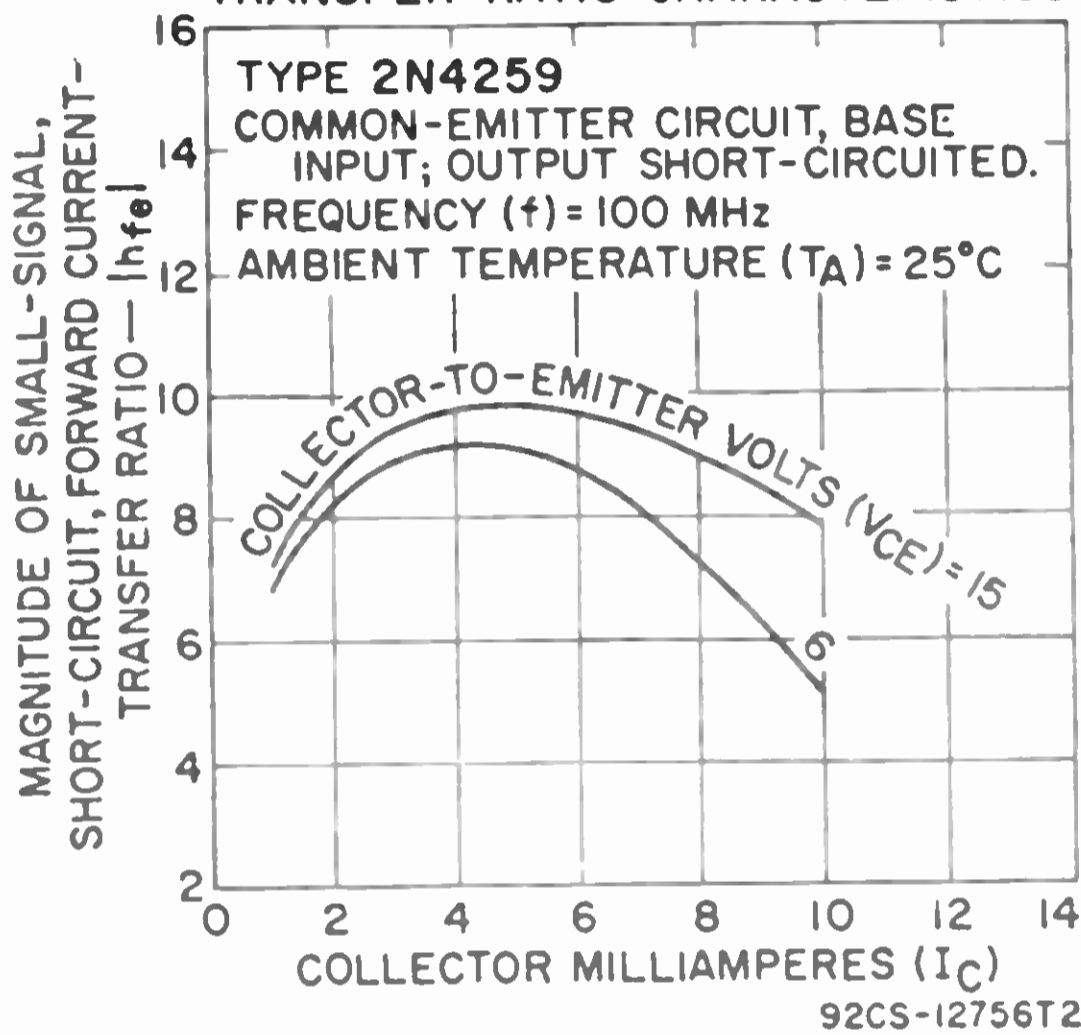
CHARACTERISTICS (cont'd)

Collector-Cutoff Current ($V_{CB} = 15\text{ V}$, $I_E = 0$)	I_{CBO}	0.01 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 8\text{ V}$, $I_C = 2\text{ mA}$)	h_{FE}	60 to 250	
Small-Signal Forward-Current Transfer Ratio: [▲]			
$V_{CE} = 8\text{ V}$, $I_C = 2\text{ mA}$, $f = 0.001\text{ MHz}$	h_{fe}	70 to 280	
$V_{CE} = 8\text{ V}$, $I_C = 2\text{ mA}$, $f = 100\text{ MHz}$	h_{fe}	7.5 to 16	
Collector-to-Base Feedback Capacitance* ($V_{CB} = 8\text{ V}$, $I_E = 0$, $f = 0.1\text{ to }1\text{ MHz}$)	C_{cb}	0.35 typ; 0.55 max	pF
Collector-to-Base Time Constant [▲] ($V_{CB} = 8\text{ V}$, $I_E = 2\text{ mA}$, $f = 31.9\text{ MHz}$)	$\tau_{b'c}$	1 to 8	ps
Small-Signal Power Gain [▲] ($V_{CE} = 8\text{ V}$, $I_C = 1.5\text{ mA}$, $f = 450\text{ MHz}$)	G_{pe}	11.5 to 16.5	dB
Noise Figure [▲] ($V_{CE} = 8\text{ V}$, $I_C = 1.5\text{ mA}$, R_G and $R_L = 50\ \Omega$, $f = 450\text{ MHz}$)	NF	5 max	dB

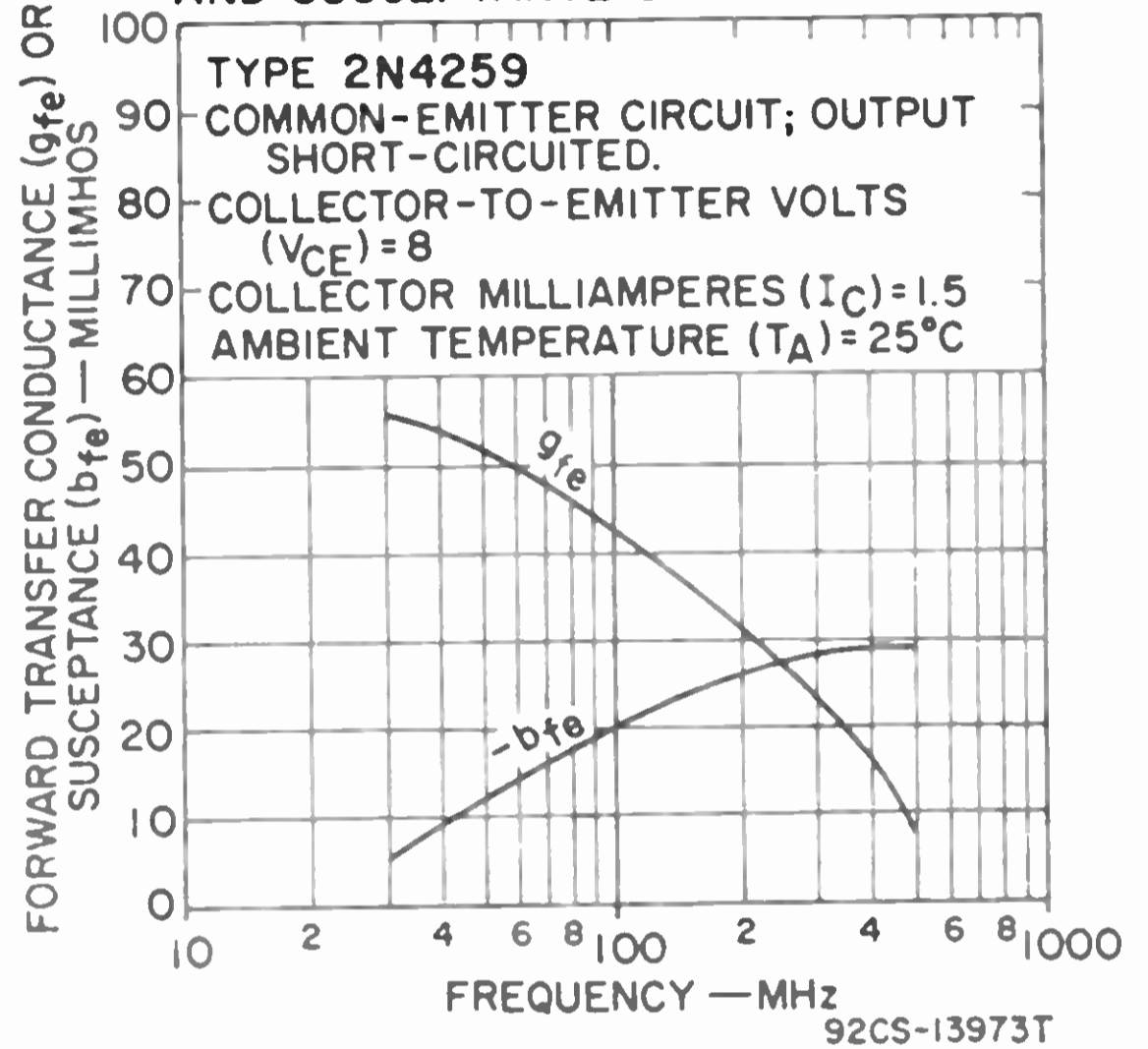
[▲] Lead 4 (case) grounded.

* Three-terminal capacitance measurement with lead No. 1 (emitter) and lead No. 4 (case) connected to guard terminal.

TYPICAL SMALL-SIGNAL FORWARD-CURRENT TRANSFER-RATIO CHARACTERISTICS



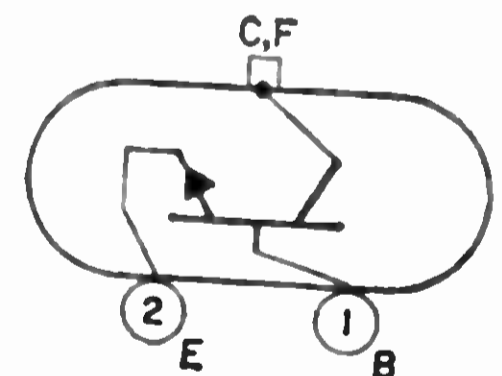
TYPICAL FORWARD TRANSFER CONDUCTANCE AND SUSCEPTANCE CHARACTERISTICS



2N4296

POWER TRANSISTOR

Si n-p-n triple diffused type used in critical amplifier and switching applications in military, industrial and commercial equipment. This type is useful as a power amplifier in line-operated equipment. JEDEC TO-66, Outline No.25. See Mounting Hardware for desired mounting arrangement.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	350	V
Collector-to-Emitter Voltage	V_{CEO}	250	V
Emitter-to-Base Voltage	V_{EBO}	4	V
Collector Current	I_C	1	A
Base Current	I_B	0.25	A
Transistor Dissipation:			
T_{MF} up to 25°C	P_T	20	W
T_{MF} above 25°C	P_T	See curve page 300	
T_A up to 55°C	P_T	2	W
T_A above 55°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 175	$^\circ\text{C}$
Storage	T_{STG}	-65 to 175	$^\circ\text{C}$
Lead-Storage Temperature (10 s max)	T_L	265	$^\circ\text{C}$

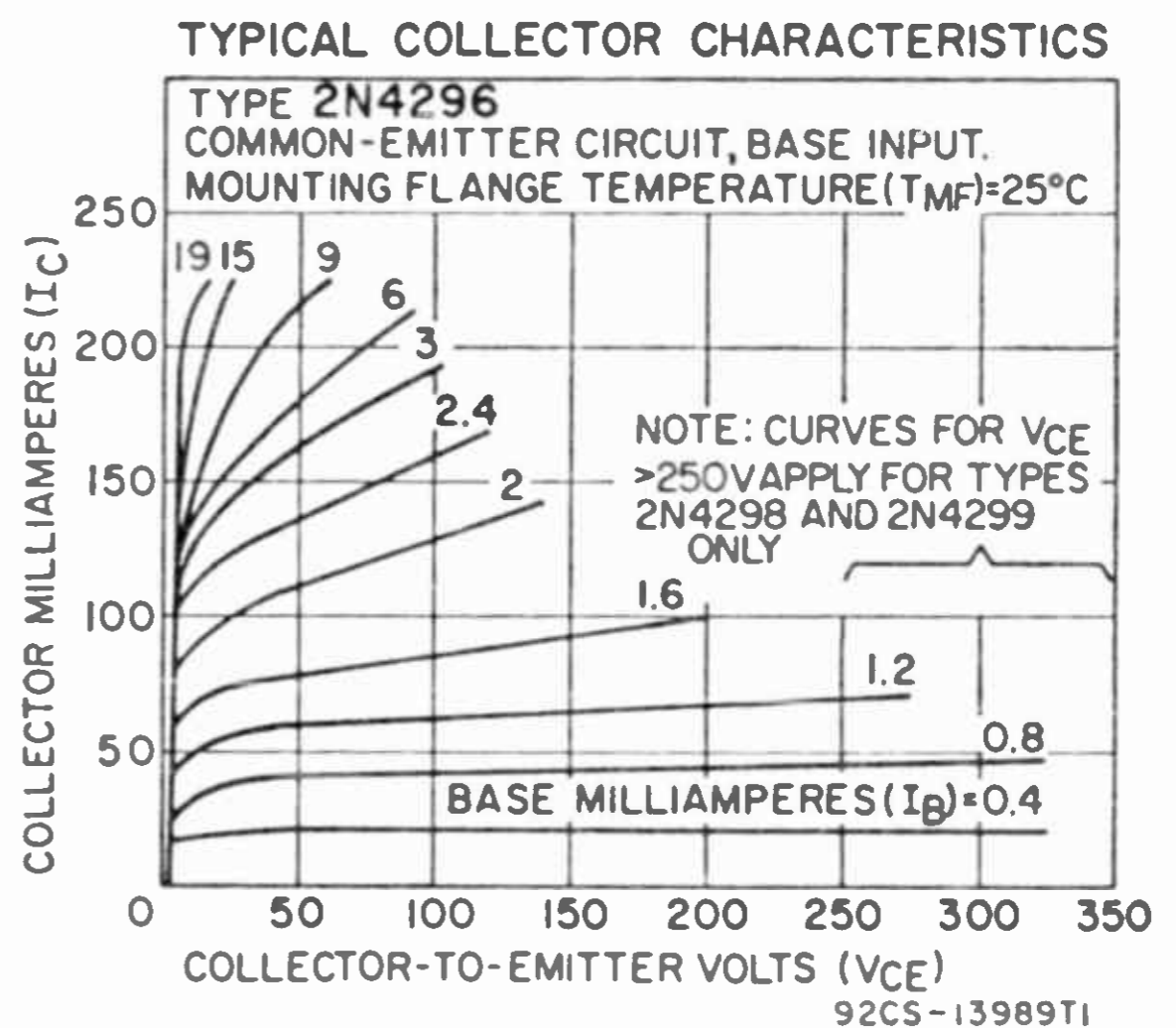
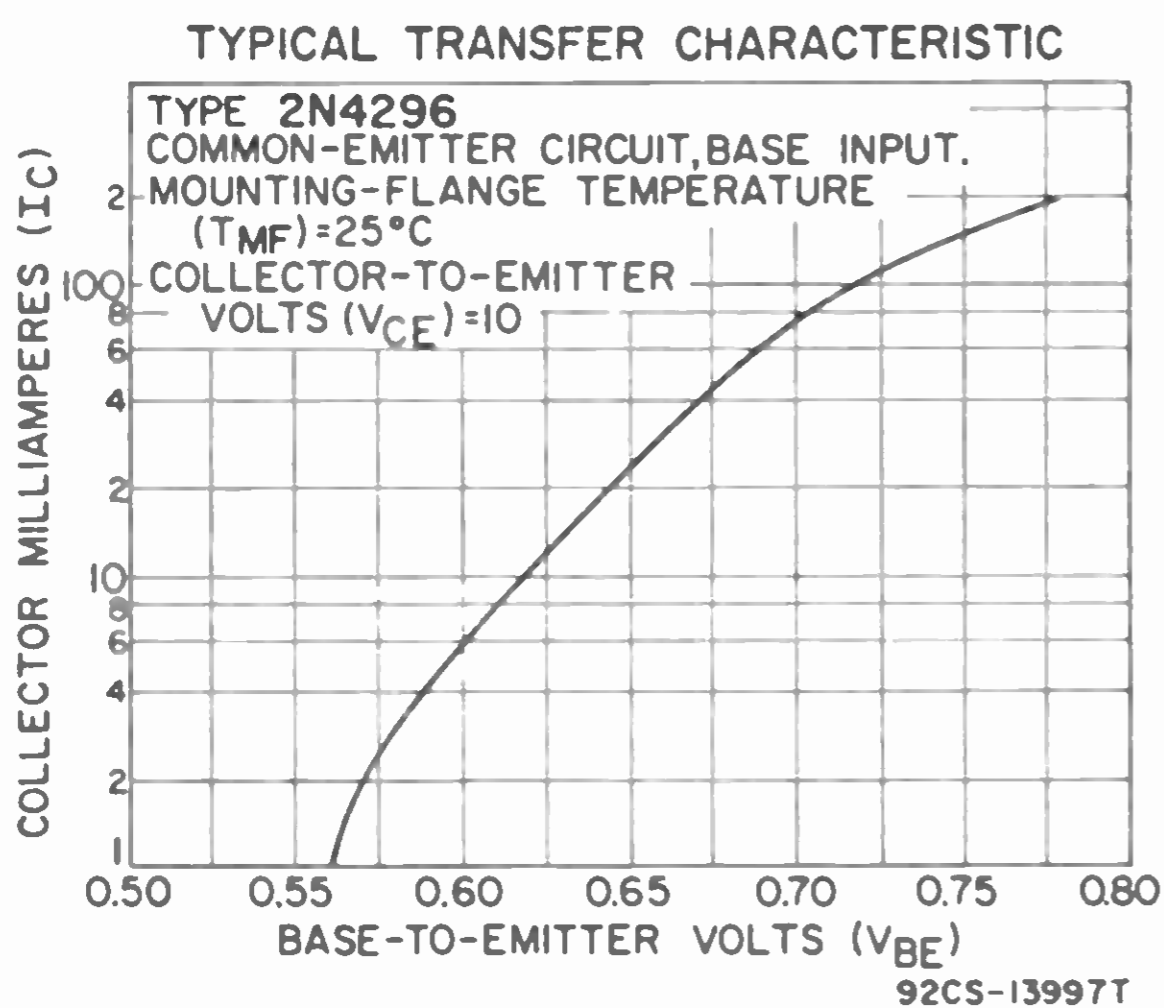
CHARACTERISTICS (At mounting-flange temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_C = 50\text{ mA}$, $I_B = 0$)	$V_{CEO}(\text{sus})$	250 min	V
Collector-to-Emitter Saturation Voltage ($I_B = 5\text{ mA}$, $I_C = 50\text{ mA}$)	$V_{CE}(\text{sat})$	0.9 max	V

CHARACTERISTICS (cont'd)

Base-to-Emitter Saturation Voltage ($I_B = 5 \text{ mA}$, $I_C = 50 \text{ mA}$)	$V_{BE}(\text{sat})$	1.5 max	V
Base-to-Emitter Voltage ($V_{CE} = 10 \text{ V}$, $I_C = 100 \text{ mA}$)	V_{BE}	0.9 max	V
Collector-Cutoff Current: $V_{CB} = 350 \text{ V}$	I_{CBO}	100 max	μA
$V_{CE} = 150 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_{MF} = 135^\circ\text{C}$	I_{CEV}	600 max	μA
Emitter-Cutoff Current ($V_{BE} = -4 \text{ V}$, $I_C = 0$)	I_{EBO}	100 max	μA
Static Forward-Current Transfer Ratio: $V_{CE} = 10 \text{ V}$, $I_C = 5 \text{ mA}$	h_{FE}	35 min	
$V_{CE} = 10 \text{ V}$, $I_C = 50 \text{ mA}$	h_{FE}	50 to 150	
$V_{CE} = 10 \text{ V}$, $I_C = 100 \text{ mA}$	h_{FE}	35 min	
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 10 \text{ V}$, $I_C = 20 \text{ mA}$, $f = 5 \text{ MHz}$)	h_{fe}	4 min; 6 typ	
Second-Breakdown Collector Current ($V_{CE} = 200 \text{ V}$)	$I_{S/b}$	75 min	mA
Collector-to-Base Feedback Capacitance* ($V_{CB} = 100 \text{ V}$, $I_C = 0$, $f = 0.1 \text{ to } 1 \text{ MHz}$)	C_{cb}	3.8 typ; 6 max	pF
Turn-On Time ($V_{BB} = 10 \text{ V}$, $V_{CC} = 100 \text{ V}$, $I_{B1} = 10 \text{ mA}$, $I_{B2} = -10 \text{ mA}$)	$t_d + t_r$	5 typ; 7 max	μs
Turn-Off Time ($V_{BB} = 10 \text{ V}$, $V_{CC} = 100 \text{ V}$, $I_{B1} = 10 \text{ mA}$, $I_{B2} = -10 \text{ mA}$, $I_C = 100 \text{ mA}$)	$t_s + t_f$	7 typ; 10 max	μs
Intrinsic Base-Spreading Resistance ($V_{CE} = 50 \text{ V}$, $I_C = 20 \text{ mA}$)	$r_{bb'}$	15 typ; 25 max	Ω
Thermal Resistance, Junction-to-Case	θ_{J-C}	7.5 max	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	60 max	$^\circ\text{C/W}$

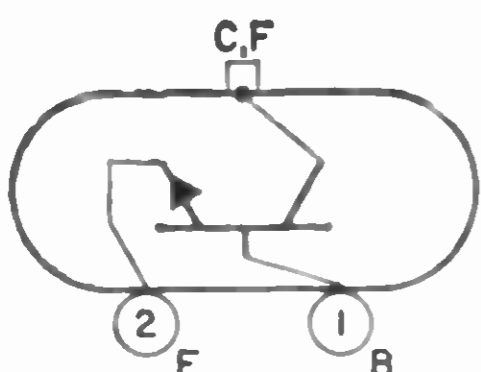
* Three-terminal measurement of the collector-to-base capacitance with lead i (emitter) connected to the guard terminal.



POWER TRANSISTOR

2N4297

Si n-p-n triple diffused type used in critical amplifier and switching applications in military, industrial, and commercial equipment. This type is useful as a power amplifier in line-operated equipment. JEDEC TO-66, Outline No.25. See Mounting Hardware for desired mounting arrangement. This type is identical to type



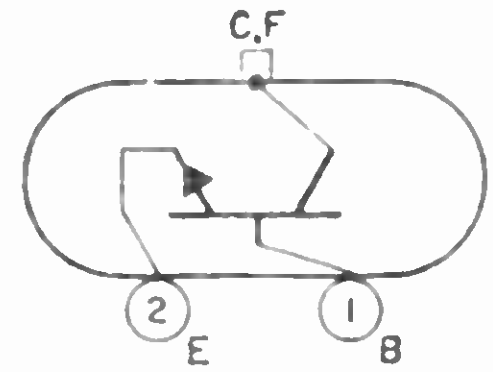
2N4296 except for the following items:

CHARACTERISTICS (At mounting-flange temperature = 25°C)

Collector-to-Emitter Saturation Voltage ($I_B = 5 \text{ mA}$, $I_C = 50 \text{ mA}$)	$V_{CE}(\text{sat})$	0.75 max	V
Static Forward-Current Transfer Ratio: $V_{CE} = 10 \text{ V}$, $I_C = 5 \text{ mA}$	h_{FE}	50 min	
$V_{CE} = 10 \text{ V}$, $I_C = 50 \text{ mA}$	h_{FE}	75 to 300	
$V_{CE} = 10 \text{ V}$, $I_C = 100 \text{ mA}$	h_{FE}	50 min	

2N4298 POWER TRANSISTOR

Si n-p-n triple-diffused type used in critical amplifier and switching applications in military, industrial, and commercial equipment. This type is useful as a power amplifier in line-operated equipment. JEDEC TO-66, Outline No.25. See Mounting Hardware for desired mounting arrangement. This type is identical to type 2N4296 except for the following items:



MAXIMUM RATINGS

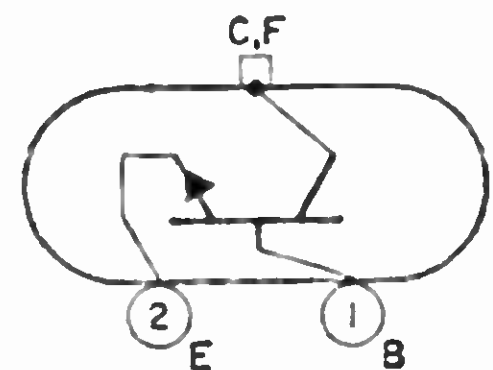
Collector-to-Base Voltage	V_{CB0}	500	V
Collector-to-Emitter Voltage	V_{CE0}	350	V

CHARACTERISTICS (At mounting-flange temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_c = 50$ mA, $I_B = 0$)	V_{CE0} (sus)	350 min	V
Collector-Cutoff Current ($V_{CB} = 500$ V)	I_{CB0}	100 max	μ A
Static Forward-Current Transfer Ratio:			
$V_{CE} = 10$ V, $I_c = 5$ mA	h_{FE}	20 min	
$V_{CE} = 10$ V, $I_c = 50$ mA	h_{FE}	25 to 75	
$V_{CE} = 10$ V, $I_c = 100$ mA	h_{FE}	20 min	

2N4299 POWER TRANSISTOR

Si n-p-n triple-diffused type used in critical amplifier and switching applications in military, industrial and commercial equipment. This type is useful as a power amplifier in line-operated equipment. JEDEC TO-66, Outline No. 25. See Mounting Hardware for desired mounting arrangement. This type is identical to type 2N4298 except for the following items:

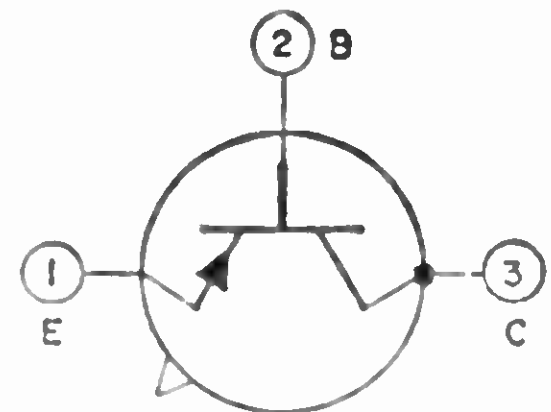


CHARACTERISTICS (At mounting-flange temperature = 25°C)

Collector-to-Emitter Saturation Voltage ($I_B = 5$ mA, $I_c = 50$ mA)	V_{CE} (sat)	0.75 max	V
Static Forward-Current Transfer Ratio:			
$V_{CE} = 10$ V, $I_c = 5$ mA	h_{FE}	35 min	
$V_{CE} = 10$ V, $I_c = 50$ mA	h_{FE}	50 to 150	
$V_{CE} = 10$ V, $I_c = 100$ mA	h_{FE}	35 min	

2N4314 POWER TRANSISTOR

Si p-n-p double-diffused epitaxial planar type used in a wide variety of small-signal, medium-power applications in industrial and commercial applications. JEDEC TO-5, Outline No.5. This type is identical to type 2N4036 except for the following items:

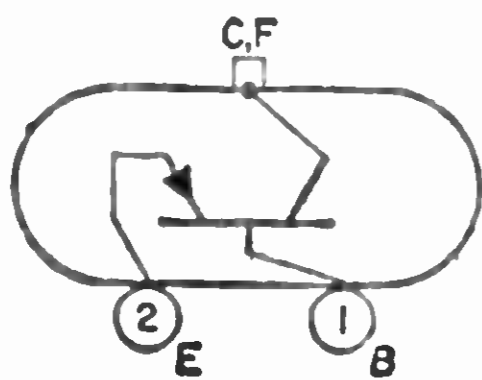


CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Saturation Voltage ($I_c = -150$ mA, $I_B = 15$ mA)	V_{CE} (sat)	-1.4 max	V
Base-to-Emitter Voltage ($V_{CE} = -10$ V, $I_c = -150$ mA)	V_{BE}	-1.5 max	V
Collector-Cutoff Current:			
$V_{CB} = -60$ V, $I_E = 0$	I_{CB0}	-0.25 max	μ A
$V_{CE} = -30$ V, $I_B = 0$	I_{CE0}	-5 max	μ A
Emitter-Cutoff Current ($V_{EB} = -5$ V, $I_c = 0$)	I_{EB0}	-1 max	μ A
Static Forward-Current Transfer Ratio ($V_{CE} = -10$ V, $I_c = -1$ mA)	h_{FE}	15 min	
Pulsed Forward-Current Transfer Ratio ($V_{CE} = -10$ V, $I_c = -150$ mA, $t_p = 300\mu$ s, $df < 2\%$)	h_{FE} (pulsed)	50 to 250	

POWER TRANSISTOR

2N4346



Ge p-n-p diffused-collector graded-base type used as a horizontal-output amplifier in conjunction with types 2N3730 (vertical output), 2N3732 (horizontal driver), and 1N4785 (damper) to provide a complete transistor/damper-diode complement. JEDEC TO-3, Outline No.2.

MAXIMUM RATINGS

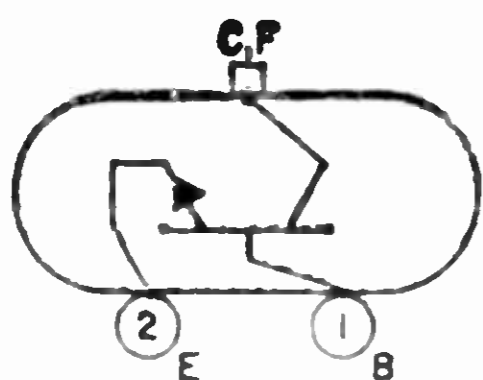
Collector-to-Base Voltage:			
Peak	V_{CBO}	-320	V
Continuous	V_{CBO}	-60	V
Collector Current	I_C	-10	A
Base Current	I_B	+4, -1	A
Transistor Dissipation:			
T_{MF} up to 55°C	P_T	5	W
T_{MF} above 55°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 85	°C
Storage	T_{STG}	-65 to 85	°C
Lead-Soldering Temperature (10 s max)	T_L	230	°C

CHARACTERISTICS

Collector-to-Emitter Breakdown Voltage ($I_C = -0.025$ A, $V_{EB} = 0$)	$V_{(BR)CES}$	-320 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -100$ mA, $I_C = 0$)	$V_{(BR)EBO}$	-2 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 6$ A, $I_B = -0.4$ A)	$V_{CE(sat)}$	-0.75 max	V
Base-to-Emitter Voltage ($I_C = 6$ A, $I_B = -0.4$ A)	V_{BE}	0.8	V
Collector-Cutoff Current ($V_{CB} = -10$ V, $I_E = 0$)	I_{CBO}	-200 max	μ A
Turn-Off Time	$t_s + t_f$	0.75 max	μ s
Thermal Resistance, Junction-to-Case	θ_{J-C}	1.5 max	°C/W

POWER TRANSISTOR

2N4347



Si n-p-n type featuring a base comprised of a homogeneous-resistivity silicon material. This type is used in high-voltage applications in power-switching circuits, audio amplifiers, series and shunt regulators, drivers, and output stages, dc-to-dc converters, inverters, and solenoid (hammer)/relay driver service in military, industrial, and commercial equipment. JEDEC TO-3, Outline No.2. See Mounting Hardware for desired mounting arrangement.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	140	V
Collector-to-Emitter Voltage:			
$V_{BE} = -1.5$ V	V_{CEV}	140	V
Base open	V_{CEO}	120	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Collector Current	I_C	5	A
Peak Collector Current	i_C	10	A
Base Current	I_B	3	A
Transistor Dissipation:			
T_c up to 25°C	P_T	100	W
T_c above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Pin-Soldering Temperature (10 s max)	T_P	255	°C

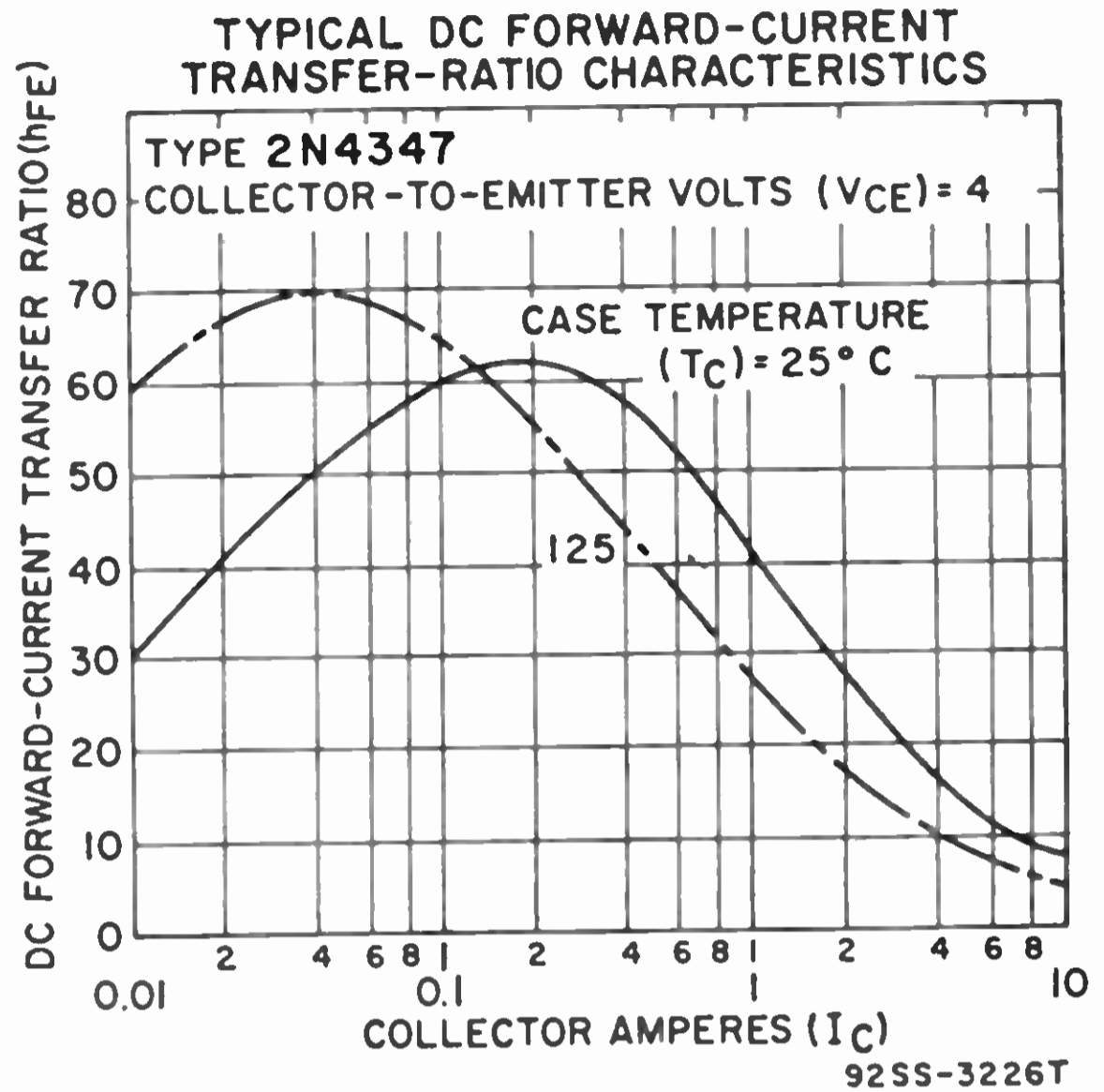
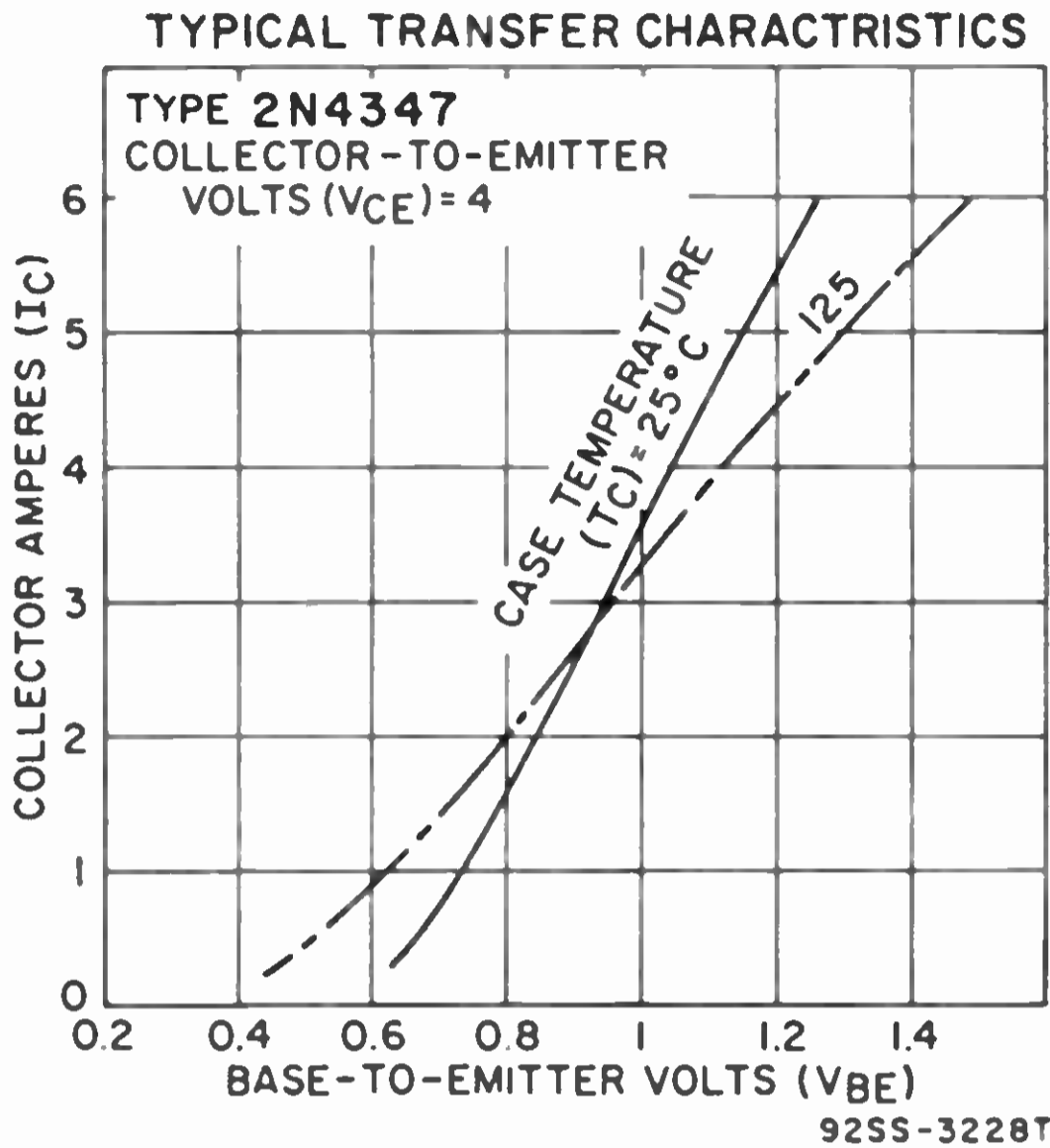
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage:			
$I_C = 0.2$ A to 3 A, $I_B = 0$	$V_{CEO(sus)}$	120 min	V
$V_{BE} = -1.5$ V, $I_C = 0.1$ A to 1.5 A	$V_{CEV(sus)}$	140 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 2$ A, $I_B = 0.2$ A)	$V_{CE(sat)}$	1 max	V
Base-to-Emitter Voltage ($V_{CE} = 4$ V, $I_C = 2$ A)	V_{BE}	2 max	V

CHARACTERISTICS (cont'd)

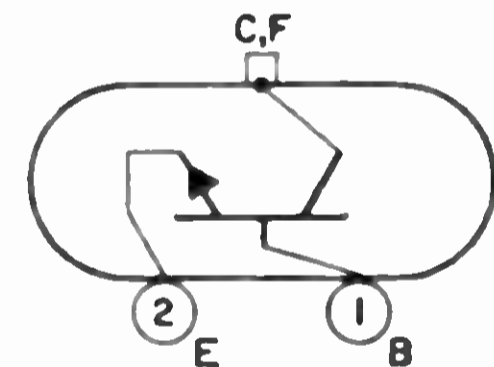
Collector-Cutoff Current:

$V_{CE} = 120\text{ V}, V_{BE} = -1.5\text{ V}$	I_{CEV}	2 max	mA
$V_{CE} = 120\text{ V}, V_{BE} = -1.5\text{ V}, T_C = 150^\circ\text{C}$	I_{CEV}	10 max	mA
Emitter-Cutoff Current ($V_{EB} = 7\text{ V}, I_C = 0$)	I_{EBO}	5 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 4\text{ V}, I_C = 2\text{ A}$)	h_{FE}	20 to 70	
Power Rating Test ($V_{CE} = 67\text{ V}, I_C = 1.5\text{ A}, t = 1\text{ s}$)		100	W
Thermal Resistance, Junction-to-Case	θ_{J-C}	1.75 max	$^\circ\text{C}/\text{W}$



2N4348 POWER TRANSISTOR

Si n-p-n type featuring a base comprised of a homogeneous-resistivity silicon material. This type is used in high-voltage applications in power-switching circuits, audio amplifiers, series and shunt regulators, drivers, and output stages, dc-to-dc converters, inverters, and solenoid (hammer)/relay driver service in military, industrial, and commercial equipment. JEDEC TO-3, Outline No.2. See Mounting Hardware for desired mounting arrangement.



MAXIMUM RATINGS

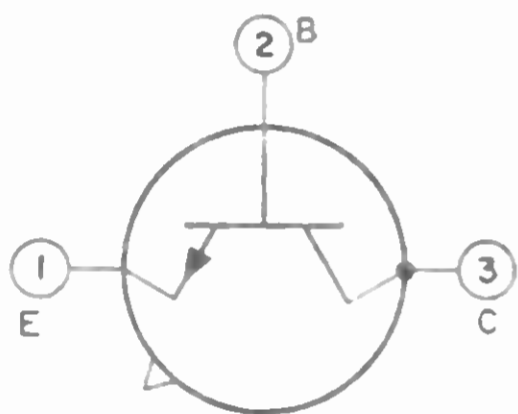
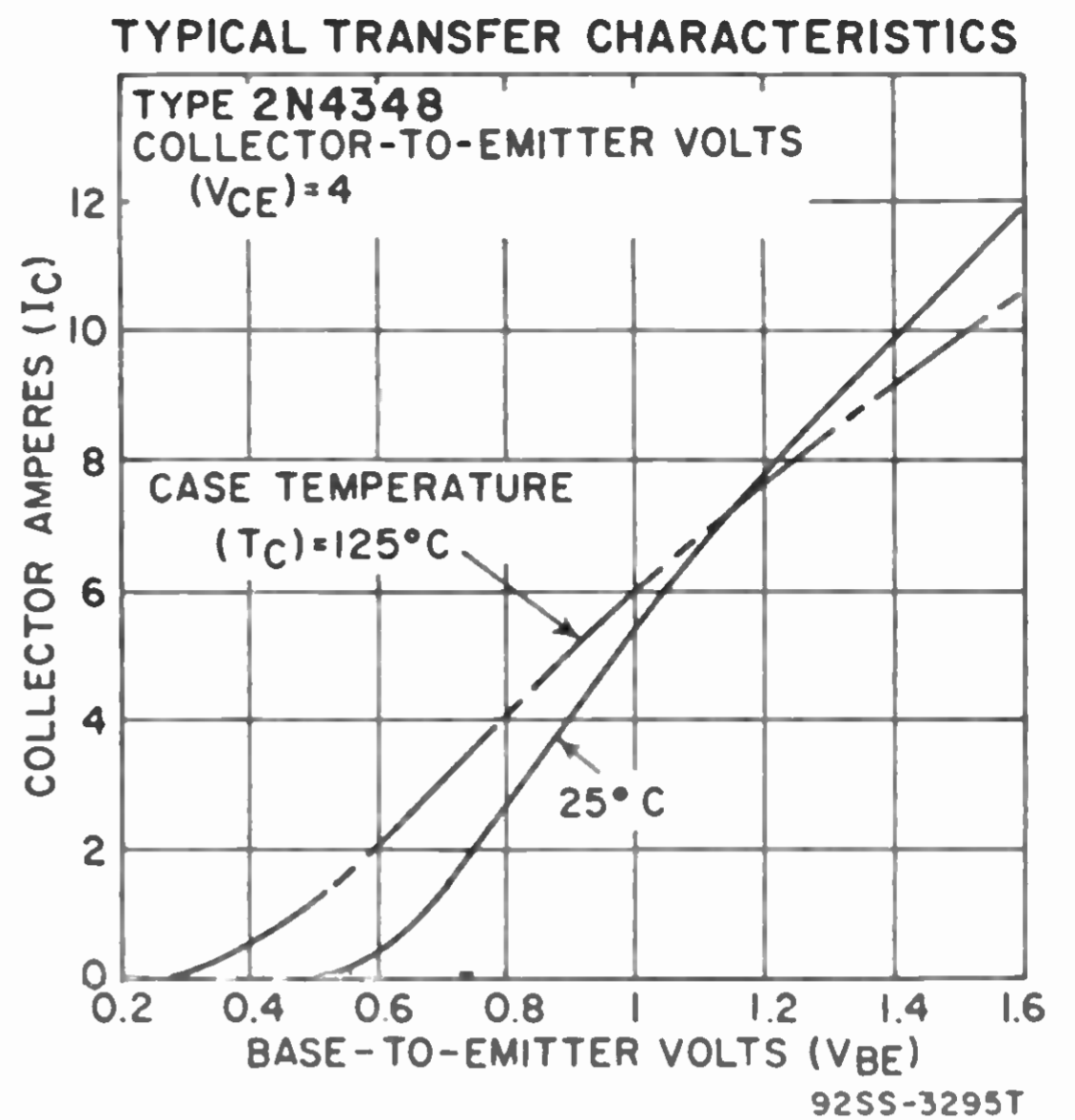
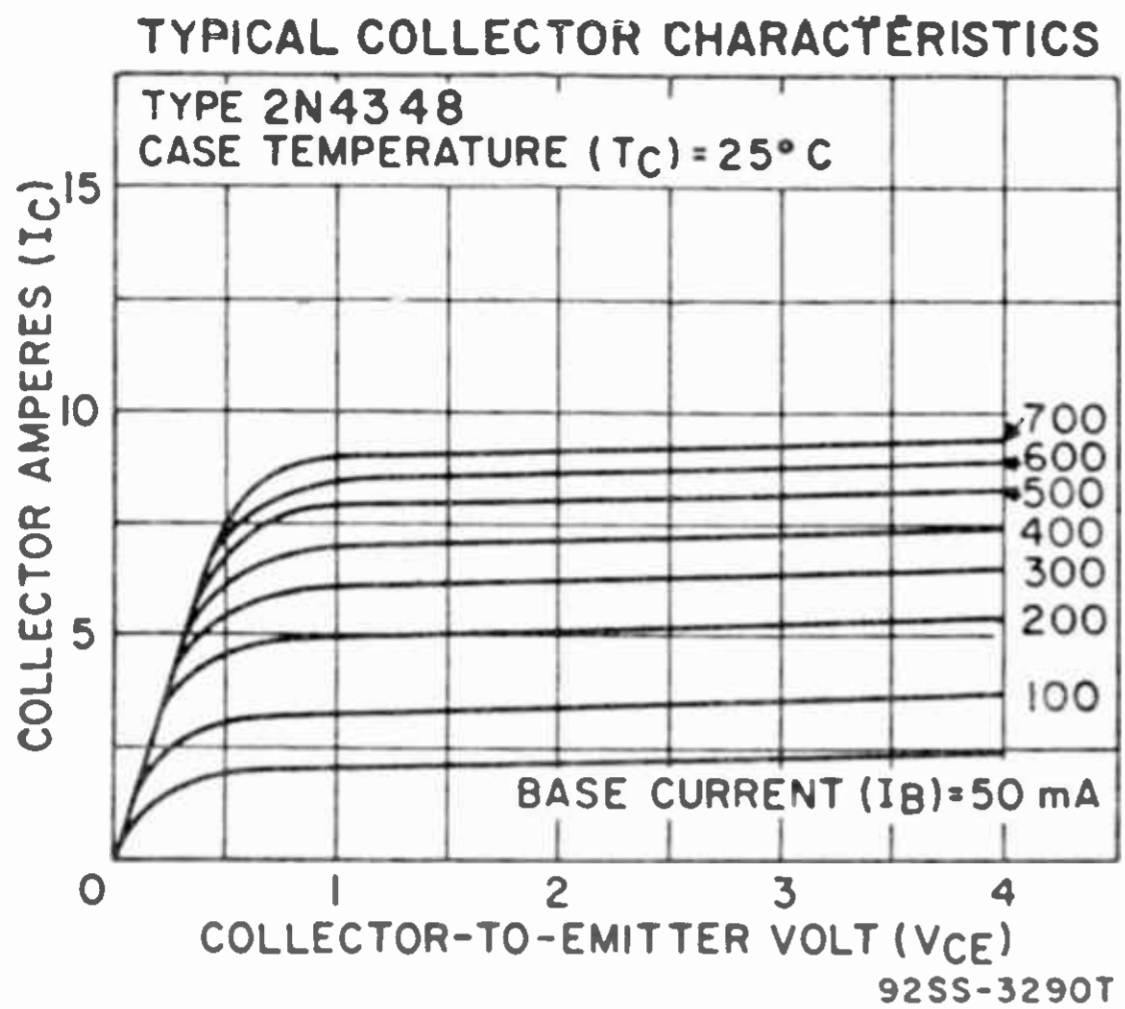
Collector-to-Base Voltage	V_{CBO}	140	V
Collector-to-Emitter Voltage:			
$V_{BE} = -1.5\text{ V}$	V_{CEV}	140	V
Base open	V_{CEO}	120	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Collector Current	I_C	10	A
Peak Collector Current	i_C	30	A
Base Current	I_B	4	A
Transistor Dissipation:			
T_C up to 25°C	P_T	120	W
T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 200	$^\circ\text{C}$
Storage	T_{STG}	-65 to 200	$^\circ\text{C}$
Pin-Soldering Temperature (10 s max)	T_P	230	$^\circ\text{C}$

CHARACTERISTICS (At case temperature = 25°C)

Emitter-to-Base Breakdown Voltage ($I_E = 5\text{ mA}, I_C = 0$)	$V_{(BR)EBO}$	7 min	V
Collector-to-Emitter Sustaining Voltage:			
$V_{BE} = 1.5\text{ V}, I_C = 0.1\text{ A to }1.5\text{ A}$	$V_{CEV}(\text{sus})$	140 min	V
$I_C = 0.2\text{ A to }3\text{ A}, I_B = 0$	$V_{CEO}(\text{sus})$	120 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 5\text{ A}, I_B = 0.5\text{ A}$)	$V_{CE}(\text{sat})$	1 max	V
Base-to-Emitter Voltage ($V_{CE} = 4\text{ V}, I_C = 5\text{ A}$)	V_{BE}	2 max	V
Collector-Cutoff Current:			
$V_{CE} = 120\text{ V}, V_{BE} = -1.5\text{ V}$	I_{CEV}	2 max	mA
$V_{CE} = 120\text{ V}, I_B = 0, T_C = 150^\circ\text{C}$	I_{CEV}	10 max	mA

CHARACTERISTICS (cont'd)

Emitter-Cutoff Current ($V_{EB} = 7\text{ V}, I_C = 0$)	I_{EBO}	5 max	mA
Pulsed Static Forward-Current Transfer Ratio ($V_{CE} = 4\text{ V}, I_C = 5\text{ A}, t_p = 300\ \mu\text{s}, f = 60\text{ Hz}$)	$h_{FE}(\text{pulsed})$	15 to 60	
Power Rating Test ($V_{CE} = 80\text{ V}, I_C = 1.5\text{ A}, t = 1\text{ s}$)		120	W
Thermal Resistance, Junction-to-Case	θ_{J-C}	1.46 max	$^{\circ}\text{C}/\text{W}$



TRANSISTOR

2N4390

Si n-p-n type used for direct "on-off" control of high-voltage, low-power devices such as numerical display tubes and relays, and for other control applications in industrial equipment. JEDEC TO-104, Outline No.32.

MAXIMUM RATINGS

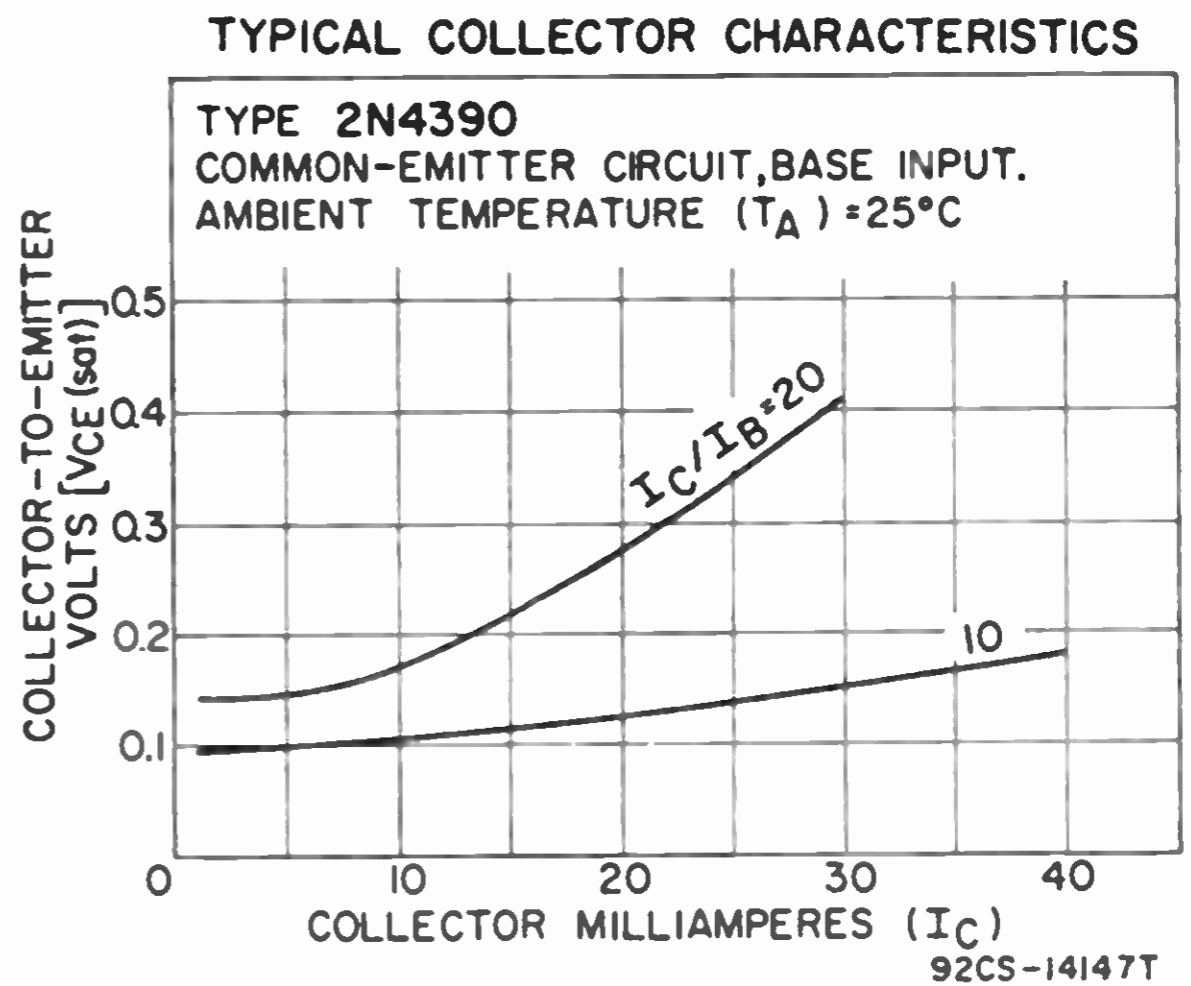
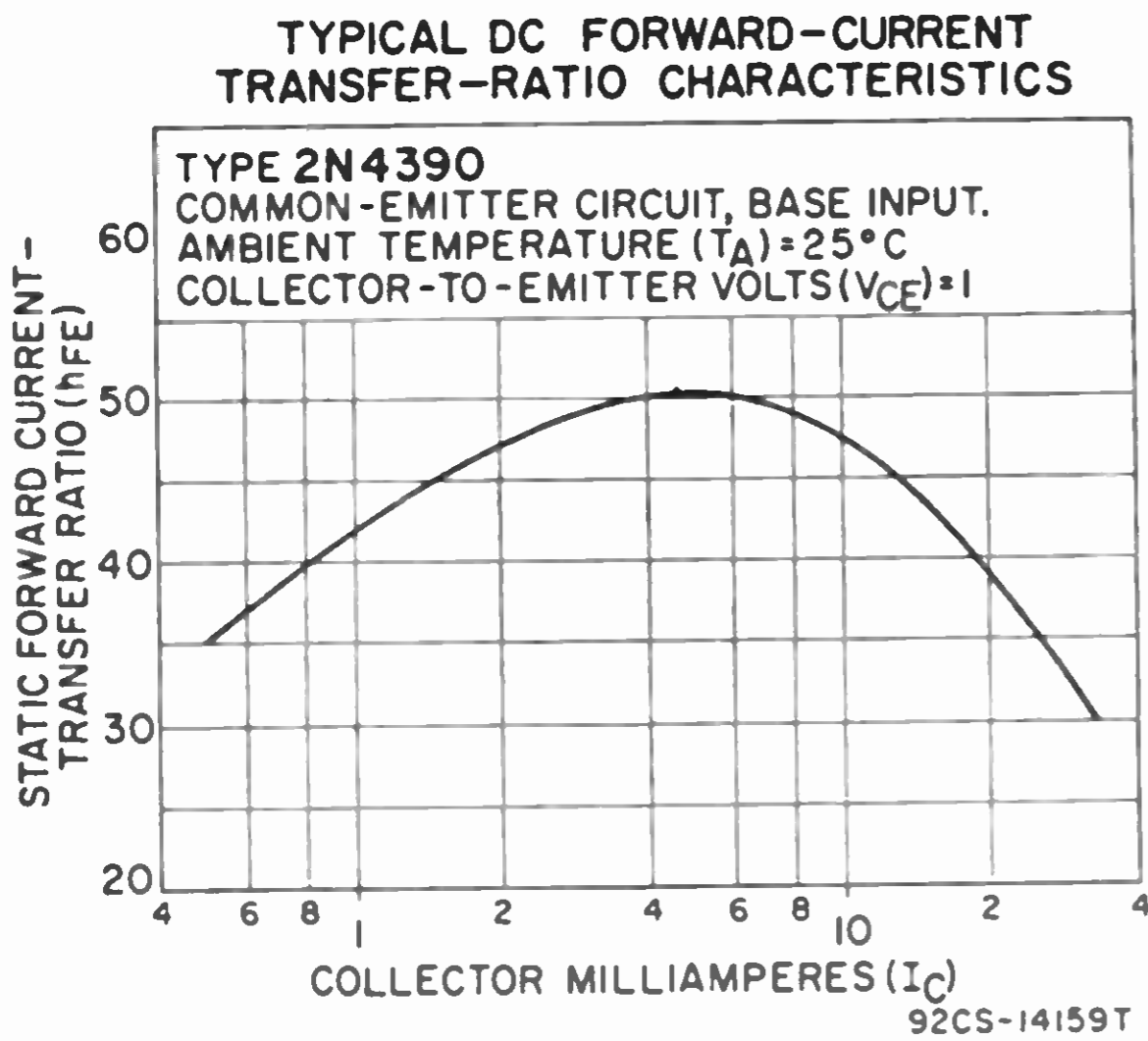
Collector-to-Base Voltage	V_{CBO}	120	V
Emitter-to-Base Voltage	V_{EBO}	6	V
Collector-to-Emitter Voltage	V_{CEO}	120	V
Collector Current	I_C	Limited by dissipation	
Transistor Dissipation:			
T_A up to 25°C	P_T	500	mW
T_A above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (T_A) and Storage (T_{STG})		-65 to 175	$^{\circ}\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	265	$^{\circ}\text{C}$

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = 0.1\text{ mA}, I_E = 0$)	$V_{(BR)CBO}$	120 min	V
Collector-to-Emitter Breakdown Voltage ($I_C = 1\text{ mA}, I_B = 0$)	$V_{(BR)CEO}$	120 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.1\text{ mA}, I_C = 0$)	$V_{(BR)EBO}$	6 min	V
Collector-to-Emitter Saturation Voltage:			
$I_C = 20\text{ mA}, I_B = 2\text{ mA}$	$V_{CE(\text{sat})}$	0.3 max	V
$I_C = 2\text{ mA}, I_B = 0.2\text{ mA}$	$V_{CE(\text{sat})}$	0.2 max	V
Base-to-Emitter Voltage:			
$I_C = 20\text{ mA}, I_B = 2\text{ mA}$	V_{BE}	0.85 max	V
$I_C = 2\text{ mA}, I_B = 0.2\text{ mA}$	V_{BE}	0.75 max	V
Collector-Cutoff Current ($V_{CE} = 70\text{ V}, V_{EB} = 1\text{ V}$)	I_{CEV}	1 max	μA
Base-Cutoff Current ($V_{CE} = 70\text{ V}, V_{EB} = 1\text{ V}$)	I_{BEV}	1 max	μA
Static Forward-Current Transfer Ratio:			
$V_{CE} = 1\text{ V}, I_C = 2\text{ mA}$	h_{FE}	20 min	
$V_{CE} = 1\text{ V}, I_C = 20\text{ mA}$	h_{FE}	20 min	
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 10\text{ V}, I_C = 20\text{ mA}, f = 4\text{ MHz}$)	h_{fe}	12.5 min	
Feedback Capacitance ($V_{CB} = 10\text{ V}, I_E = 0, f = 1\text{ MHz}$)	C_{cb}	6 max	pF
Input Capacitance ($V_{EB} = 0.5\text{ V}, I_E = 0, f = 1\text{ MHz}$)	C_{ibo}	40 max	pF
Delay Time ($V_{CC} = 3.4\text{ V}, V_{BE(\text{off})} = 1.5\text{ V},$ $I_{B1} = 2\text{ mA}, I_{CS} = 20\text{ mA}$)	t_d	150 max	ns
Rise Time ($V_{CC} = 3.4\text{ V}, V_{BE(\text{off})} = 1.5\text{ V},$ $I_{B1} = 2\text{ mA}, I_{CS} = 20\text{ mA}$)	t_r	500 max	ns

CHARACTERISTICS (cont'd)

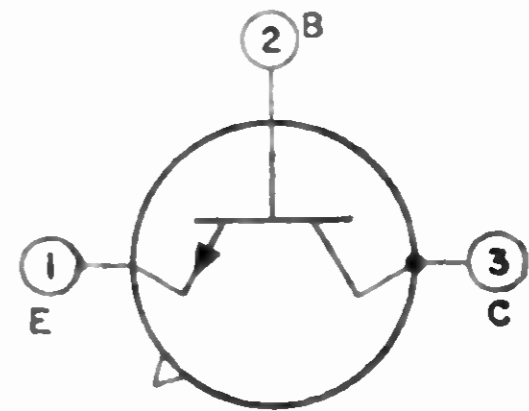
Storage Time ($V_{CC} = 3.4$ V, $I_{B1} = 2$ mA, $I_{CS} = 20$ mA, $I_{B2} = -2$ mA)	t_s	800 max	ns
Fall Time ($V_{CC} = 3.4$ V, $I_{B1} = 2$ mA, $I_{CS} = 20$ mA, $I_{B2} = -2$ mA)	t_f	500 max	ns



- 2N4395** Refer to Chart of Discontinued Transistors
- 2N4396** Refer to Chart of Discontinued Transistors
- 2N4397** Refer to Chart of Discontinued Transistors

2N4427 TRANSISTOR

Si n-p-n "overlay" epitaxial planar type used in class A, B, or C amplifier, frequency-multiplier, or oscillator circuits; it is used in output, driver, or pre-driver stages in vhf and uhf equipment. JEDEC TO-39, Outline No.15.



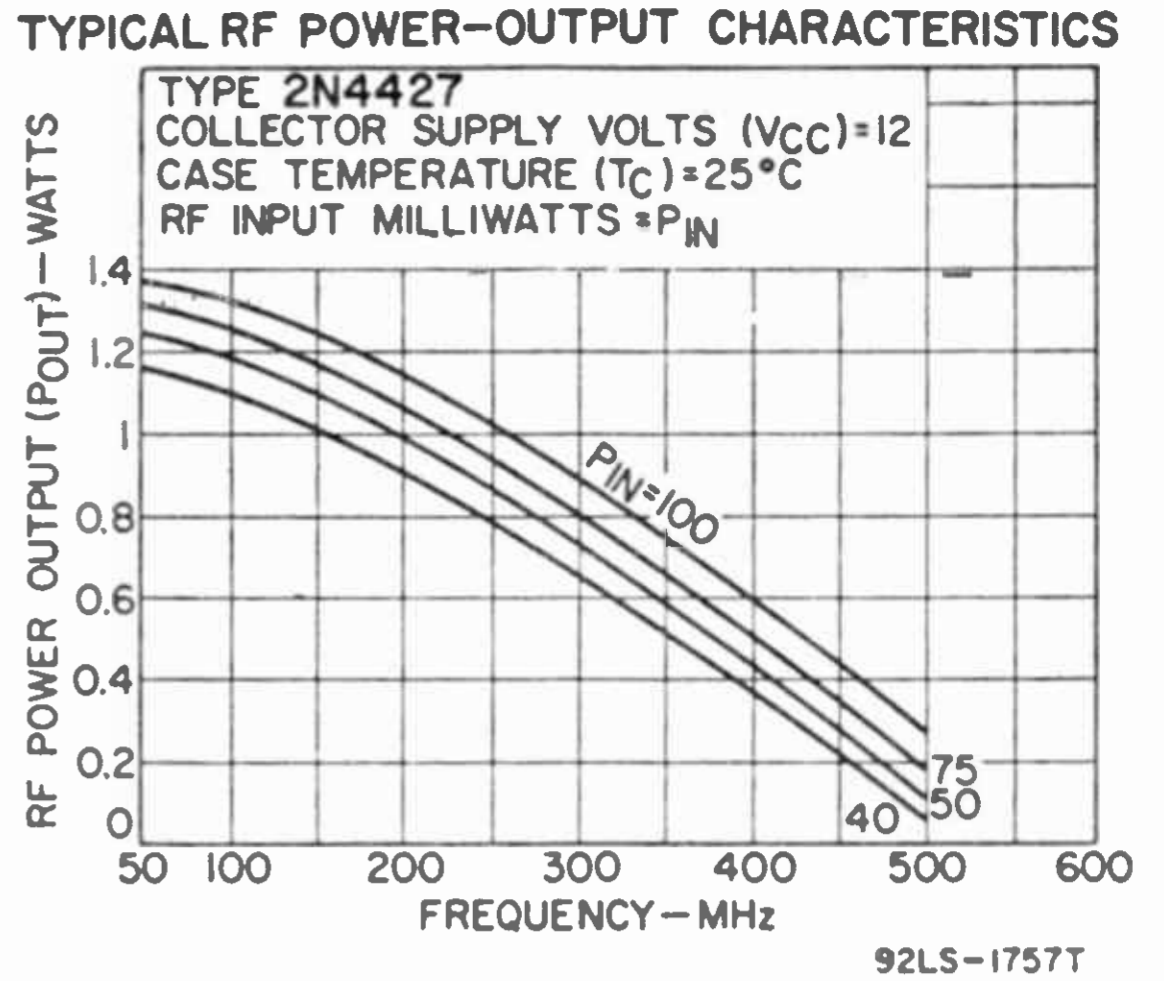
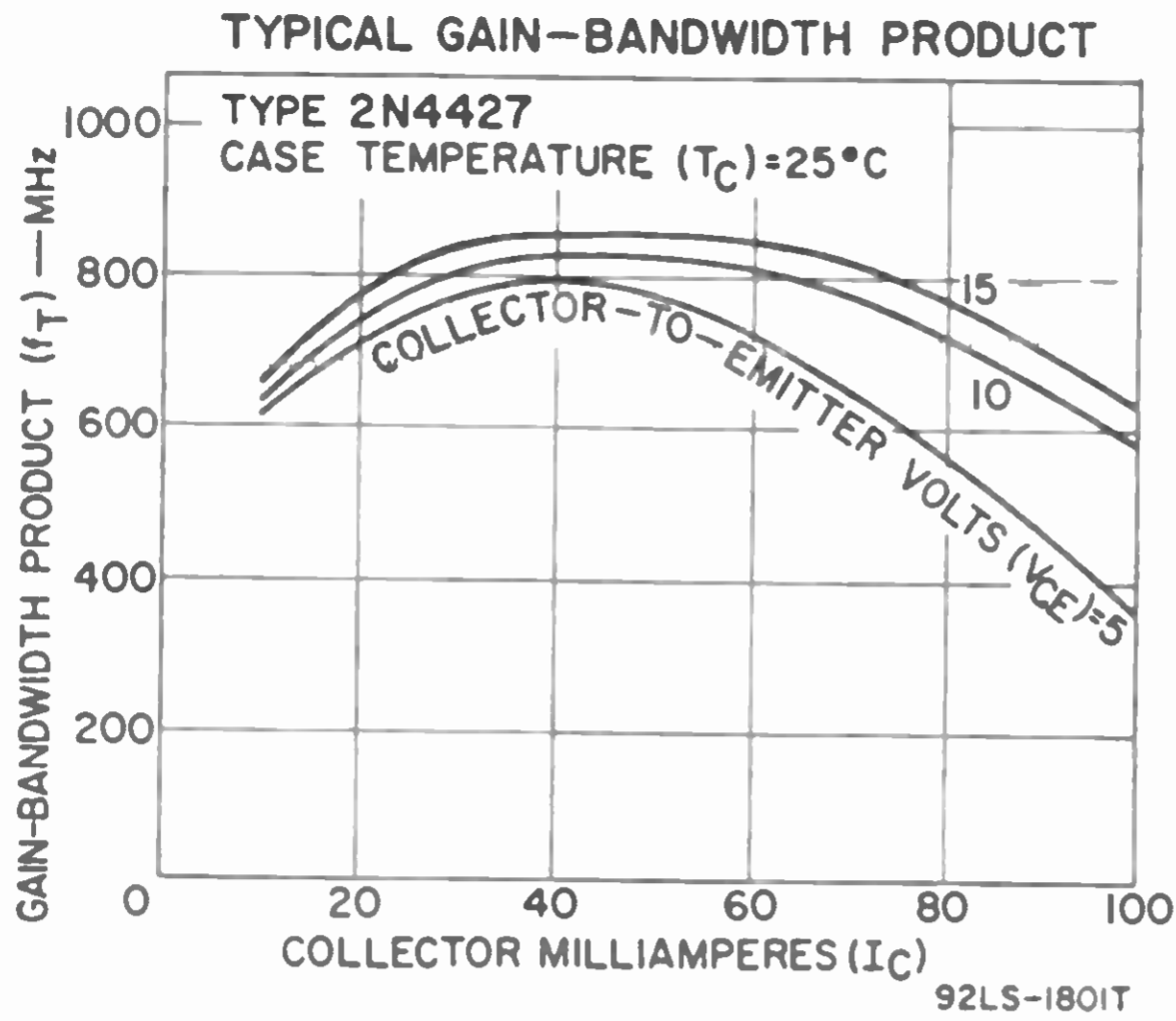
MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	40	V
Collector-to-Emitter Voltage	V_{CEO}	20	V
Emitter-to-Base Voltage	V_{EBO}	2	V
Collector Current	I_C	0.4	A
Transistor Dissipation:			
T_c up to 25°C	P_T	3.5	W
T_c above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	230	°C

CHARACTERISTICS (At case temperature = 25°C)

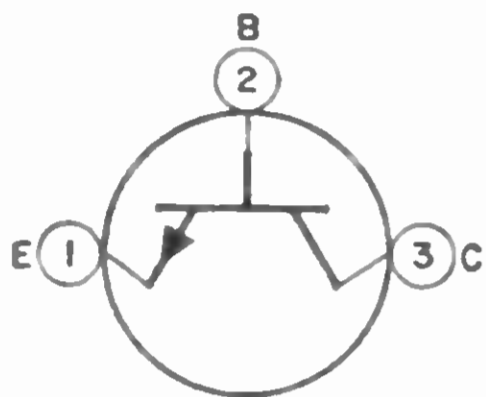
Collector-to-Base Breakdown Voltage ($I_C = 0.1$ mA, $I_E = 0$)	$V_{(BR)CBO}$	40 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.1$ mA, $I_C = 0$)	$V_{(BR)EBO}$	2 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 100$ mA, $I_B = 20$ mA)	$V_{CE(sat)}$	0.5 max	V
Collector-to-Emitter Sustaining Voltage:			
$I_C = 5$ mA, $R_{BE} = 10 \Omega$	$V_{CER(sus)}$	40 min	V
$I_C = 5$ mA, $I_B = 0$	$V_{CEO(sus)}$	20 min	V
Collector-Cutoff Current ($V_{CE} = 12$ V, $I_B = 0$)	I_{CEO}	20 max	μA
Output Capacitance ($V_{CB} = 12$ V, $I_E = 0$, $f = 1$ MHz)	C_{obo}	4 max	pF
RF Power Output, Amplifier, Unneutralized ($V_{CC} = 12$ V, $P_{IE} = 0.1$ W, $f = 175$ MHz, R_G and $R_L = 50 \Omega$)	P_{oB}	1* min	W

* For conditions given, minimum efficiency = 70 per cent.



TRANSISTOR

2N4440



Si n-p-n "overlay" epitaxial planar type used in class A, B, and C amplifiers, frequency multipliers, or oscillators, for military and industrial communications. JEDEC TO-60, Outline No.23. See Mounting Hardware for desired mounting arrangement.

MAXIMUM RATINGS

Collector-to-Emitter Voltage:

$V_{BE} = -1.5$ V Base open

Emitter-to-Base Voltage

Collector Current

Transistor Dissipation:

T_c up to 25°C

T_c above 25°C

Temperature Range:

Operating (Junction)

Storage

Lead-Soldering Temperature (10 s max)

V_{CEV}	65	V
V_{CEO}	40	V
V_{EBO}	4	V
I_C	1.5	A
P_T	11.6	W
P_T	See curve page 300	
T_J (opr)	-65 to 200	$^\circ\text{C}$
T_{STG}	-65 to 200	$^\circ\text{C}$
T_l	230	$^\circ\text{C}$

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Base Breakdown Voltage

($I_C = 0.1$ mA, $I_E = 0$)

Collector-to-Emitter Breakdown Voltage:

$I_B = 0$, $I_C = 0$ to 200 mA, pulsed through

inductor $L = 25$ mH, $df = 50\%$

$V_{BE} = -1.5$ V, $I_C = 0$ to 200 mA, pulsed through

inductor $L = 25$ mH, $df = 50\%$

Emitter-to-Base Breakdown Voltage

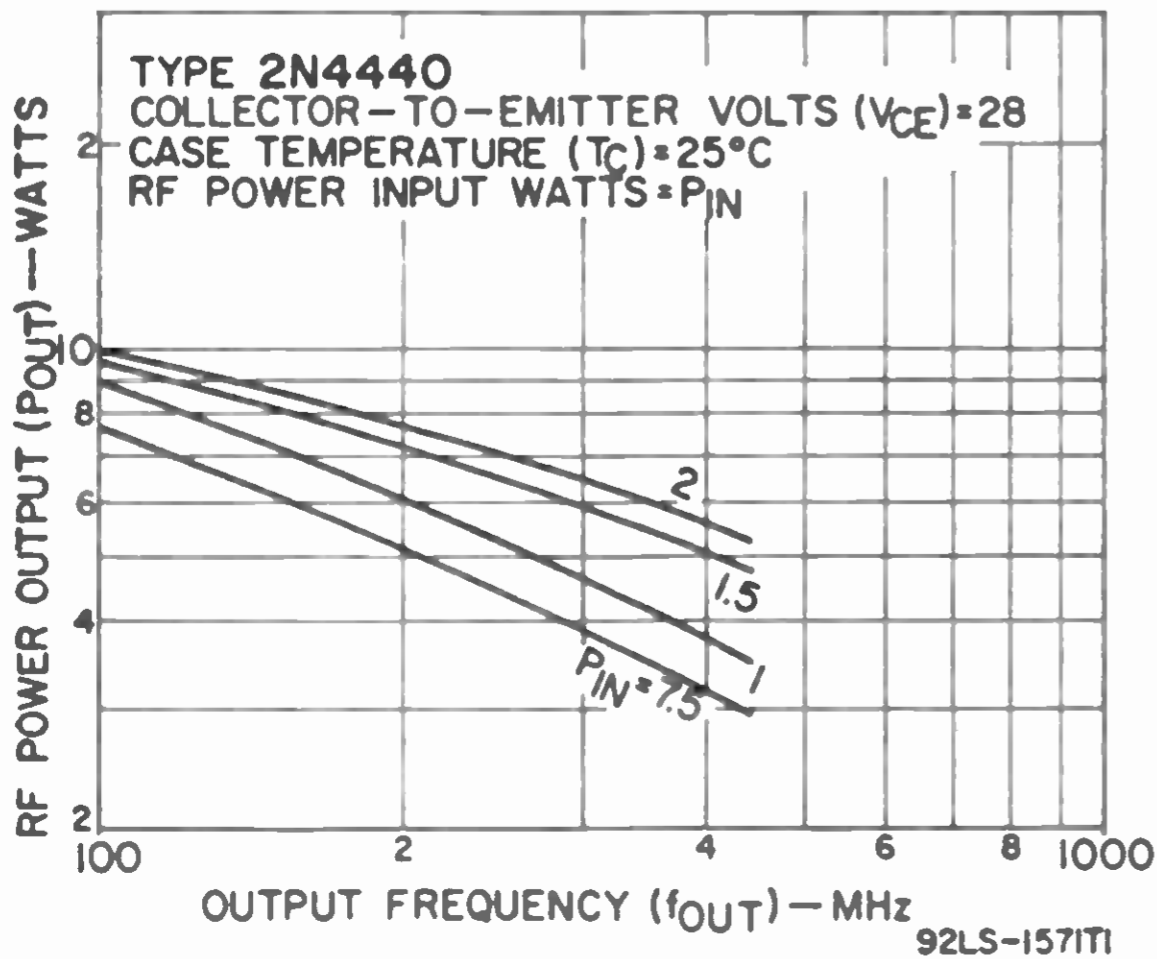
($I_E = 0.1$ mA, $I_C = 0$)

Collector-to-Emitter Saturation Voltage

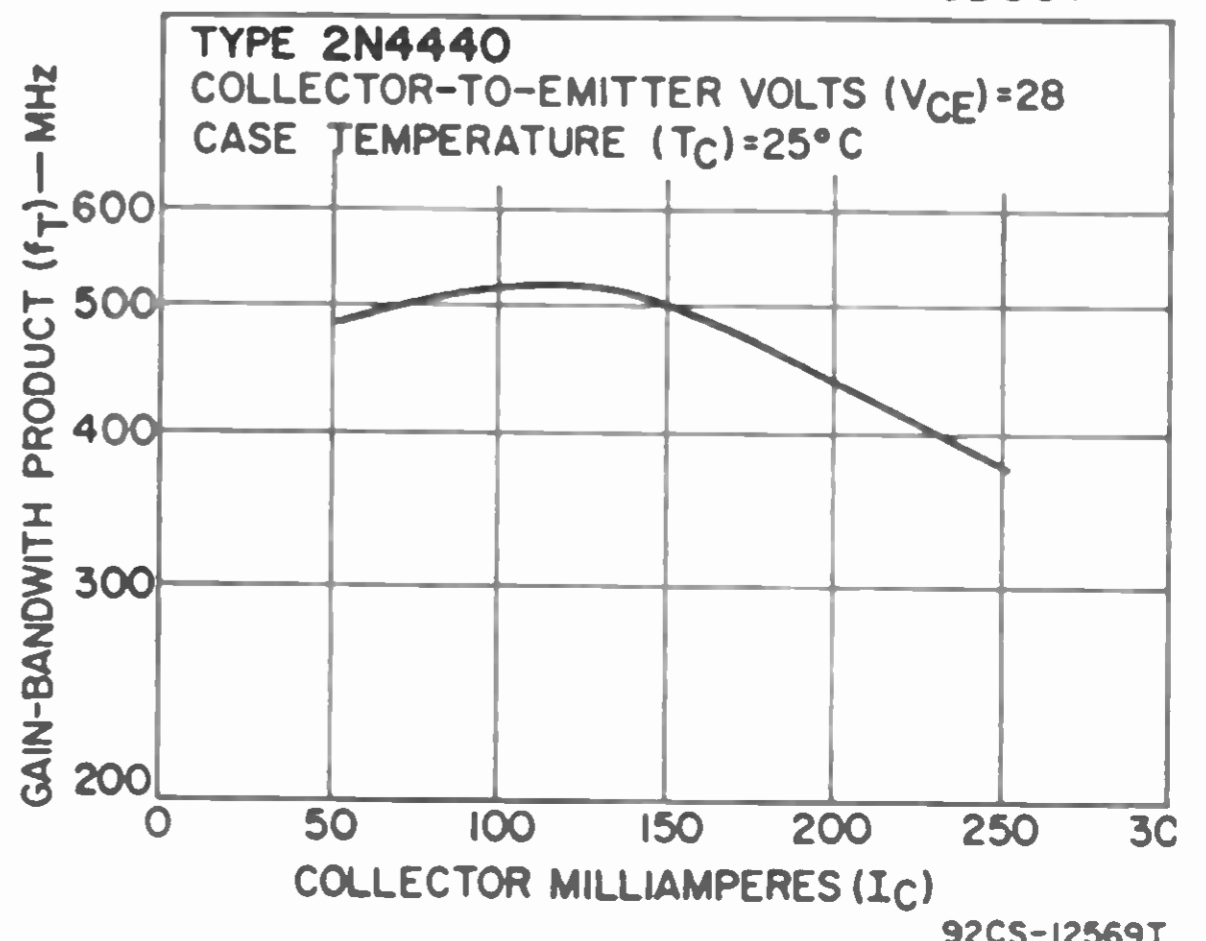
($I_C = 500$ mA, $I_B = 100$ mA)

$V_{(BR)CBO}$	65 min	V
$V_{(BR)CEO}$	40 min	V
$V_{(BR)CEV}$	65 min	V
$V_{(BR)EBO}$	4 min	V
$V_{CE(sat)}$	1 max	V

TYPICAL RF POWER-OUTPUT CHARACTERISTICS



TYPICAL GAIN-BANDWIDTH PRODUCT



CHARACTERISTICS (cont'd)

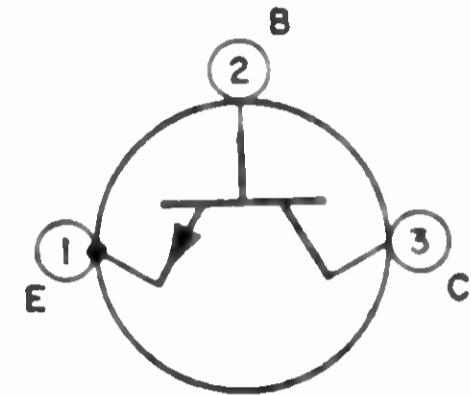
Collector-Cutoff Current ($V_{CE} = 30\text{ V}, I_B = 0$)	I_{CEO}	0.1 max	V
Gain-Bandwidth Product ($V_{CE} = 28\text{ V}, I_C = 150\text{ mA}$) ...	f_T	500	MHz
Output Capacitance ($V_{CB} = 30\text{ V}, I_E = 0, f = 1\text{ MHz}$)	C_{obo}	10 max	pF
Collector-to-Case Capacitance	C_c	6 max	pF
Intrinsic Base-Spreading Resistance ($V_{CE} = 28\text{ V}, I_C = 250\text{ mA}$)	$r_{bb'}$	10	Ω
RF Power Output, Amplifier, Unneutralized: $V_{CE} = 28\text{ V}, P_{IE} = 1.7\text{ W}, R_G$ and $R_L = 50\ \Omega,$ $f = 225\text{ MHz}$	P_{OE}	6.5*	W
$V_{CE} = 28\text{ V}, P_{IE} = 1.7\text{ W}, R_G$ and $R_L = 50\ \Omega,$ $f = 400\text{ MHz}$	P_{OE}	5 min*	W

* For conditions given, minimum efficiency = 55 per cent.
 * For conditions given, minimum efficiency = 45 per cent.

2N4932 *# 29*

TRANSISTOR

Si n-p-n "overlay" epitaxial planar type used in high-power class C rf amplifiers for international vhf mobile and portable communications service. JEDEC TO-60, Outline No.23. See Mounting Hardware for desired mounting arrangement.



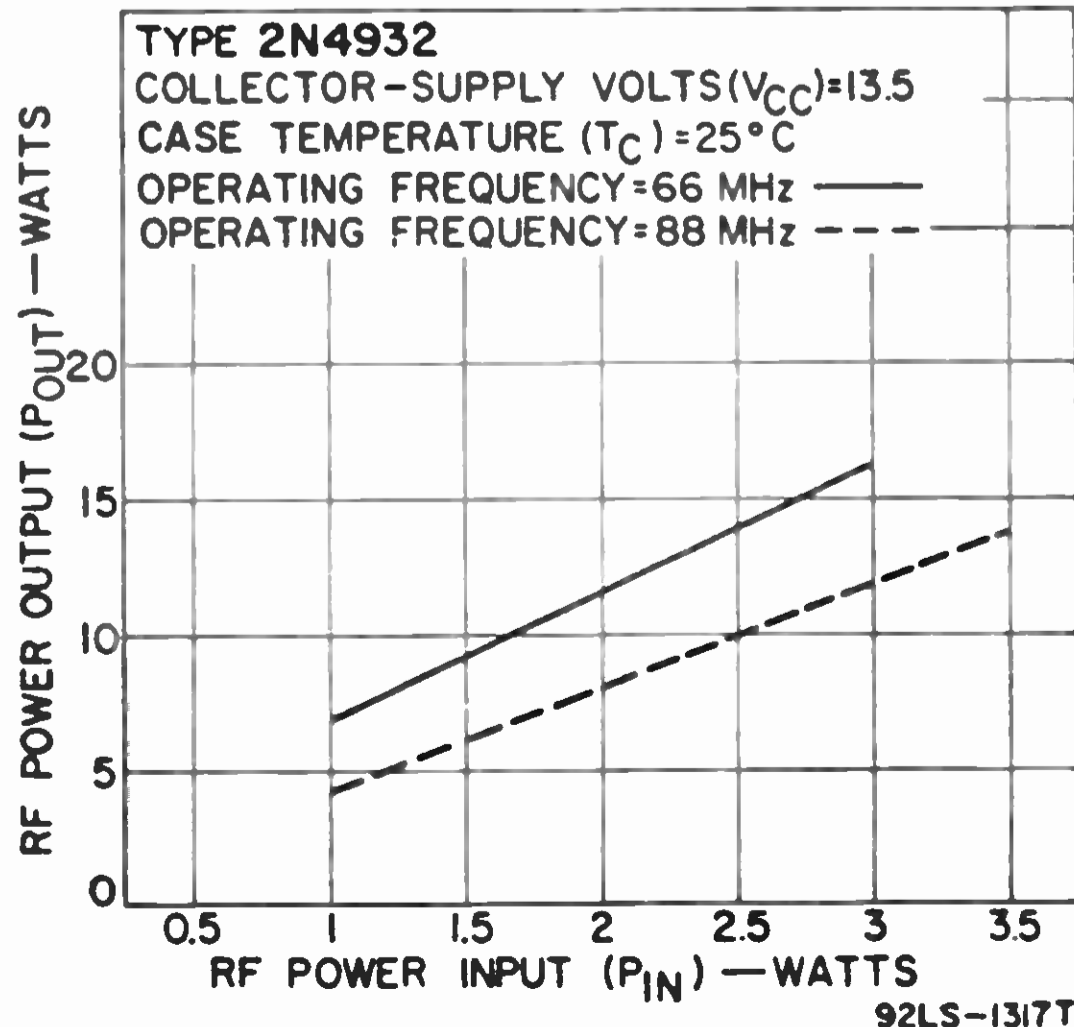
MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	50	V
Collector-to-Emitter Voltage: $V_{BE} = -1.5\text{ V}$	V_{CEV}	50	V
Base open	V_{CEO}	25	V
Emitter-to-Base Voltage	V_{EBO}	4	V
Collector Current	I_C	3.3	A
Peak Collector Current	i_c	10	A
Transistor Dissipation: T_C up to 25°C	P_T	70	W
T_C above 25°C	P_T	See curve page 300	
RF Input Power: At 88 MHz	P_{IE}	3.5	W
Below 88 MHz	P_{IE}	Derate linearly by 0.022 W/MHz to 3 W	
Temperature Range: Operating (Junction)	T_J (opr)	-65 to 200	$^\circ\text{C}$
Storage	T_{STG}	-65 to 200	$^\circ\text{C}$

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Breakdown Voltage: $I_C = 200\text{ mA}$, pulsed through an inductor $L = 25\text{ mH},$ $df = 50\%, I_B = 0$	$V_{(BR)CEO}$ (sus)	25 min	V
$I_C = 200\text{ mA}$, pulsed through an inductor $L = 25\text{ mH},$ $df = 50\%, V_{BE} = -1.5\text{ V}$	$V_{(BR)CEV}$ (sus)	50 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 10\text{ mA},$ $I_C = 0$)	$V_{(BR)EBO}$	4 min	V
Collector-Cutoff Current: $V_{CE} = 15\text{ V}, I_B = 0$	I_{CEO}	1 max	mA
$V_{CB} = 40\text{ V}, I_E = 0$	I_{CBO}	10 max	mA

TYPICAL RF POWER-OUTPUT CHARACTERISTICS



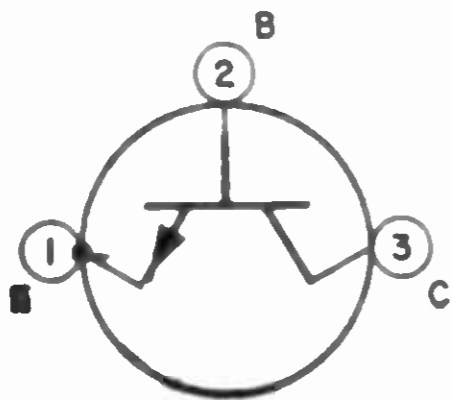
92LS-1317T

CHARACTERISTICS (cont'd)

Output Capacitance ($V_{CB} = 15\text{ V}$, $I_E = 0$)	C_{obo}	120 max	pF
RF Power Output ($V_{CC} = 13.5\text{ V}$, $P_{IE} = 3.5\text{ W}$, $f = 88\text{ MHz}$, R_G and $R_L = 50\ \Omega$)	P_{oB}	12 • min	W

• For conditions given, minimum efficiency = 70 per cent.

TRANSISTOR *29.00* **2N4933**



Si n-p-n "overlay" epitaxial planar type used in high-power class C rf amplifiers for international vhf mobile and portable communications service. JEDEC TO-60, Outline No.23. See **Mounting Hardware** for desired mounting arrangement. This type is identical with type 2N4932 except for the following items:

MAXIMUM RATINGS

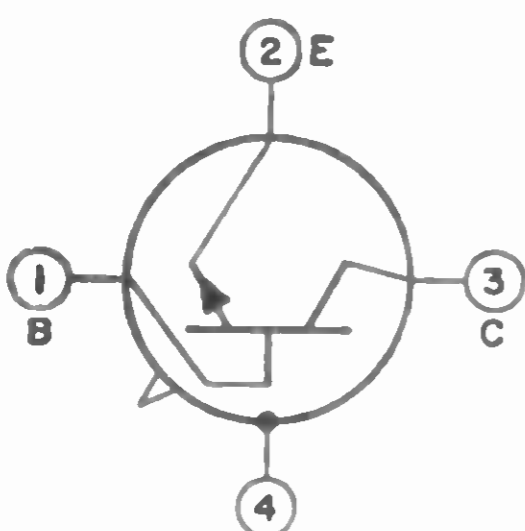
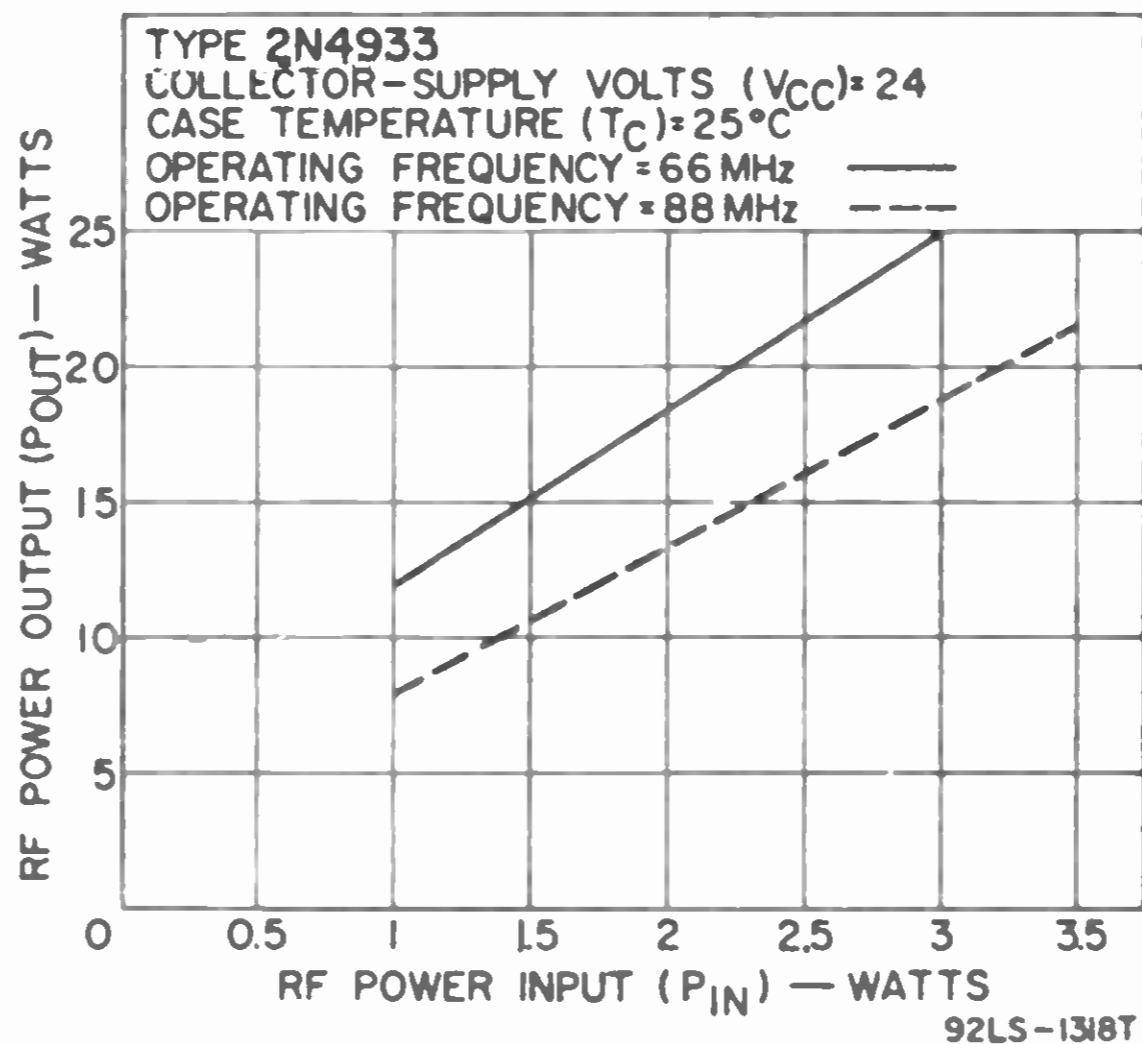
Collector-to-Base Voltage	V_{CBO}	70	V
Collector-to-Emitter Voltage: $V_{BE} = -1.5\text{ V}$	V_{CEV}	70	V
Base open	V_{CEO}	35	V

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Breakdown Voltage: $I_C = 200\text{ mA}$, pulsed through inductor $L = 25\text{ mA}$, $df = 50\%$, $I_b = 0$	$V_{(BR)CEO(SUS)}$	35 min	V
$I_C = 200\text{ mA}$, pulsed through inductor $L = 25\text{ mA}$, $df = 50\%$, $V_{BE} = -1.5\text{ V}$	$V_{(BR)CEV(SUS)}$	70 min	V
Collector-Cutoff Current: $V_{CE} = 30\text{ V}$, $I_B = 0$	I_{CEO}	1 max	mA
$V_{CB} = 50\text{ V}$, $I_E = 0$	I_{CBO}	10 max	mA
Output Capacitance ($V_{CB} = 30\text{ V}$, $I_E = 0$)	C_{obo}	85 max	pF
RF Power Output ($V_{CC} = 24\text{ V}$, $P_{IE} = 3.5\text{ W}$, $f = 88\text{ MHz}$, R_G and $R_L = 50\ \Omega$)	P_{oB}	20 • min	W

• For conditions given, minimum efficiency = 70 per cent.

TYPICAL RF POWER-OUTPUT CHARACTERISTICS



TRANSISTOR **2N4934**

Si n-p-n epitaxial planar type used in vhf-uhf applications at frequencies up to 500 MHz. The terminal arrangement permits shielding between input and output terminals for superior high-frequency performance and greater circuit stability, particularly on printed-circuit boards. JEDEC TO-104, Outline No.31.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CB0}	40	V
Collector-to-Emitter Voltage	V_{CEO}	30	V
Emitter-to-Base Voltage	V_{EBO}	3	V
Collector Current	I_C	Limited by dissipation	
Transistor Dissipation:			
T_A up to 25°C	P_T	200	mW
T_A above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 200	°C
Storage	T_{SIG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	265	°C

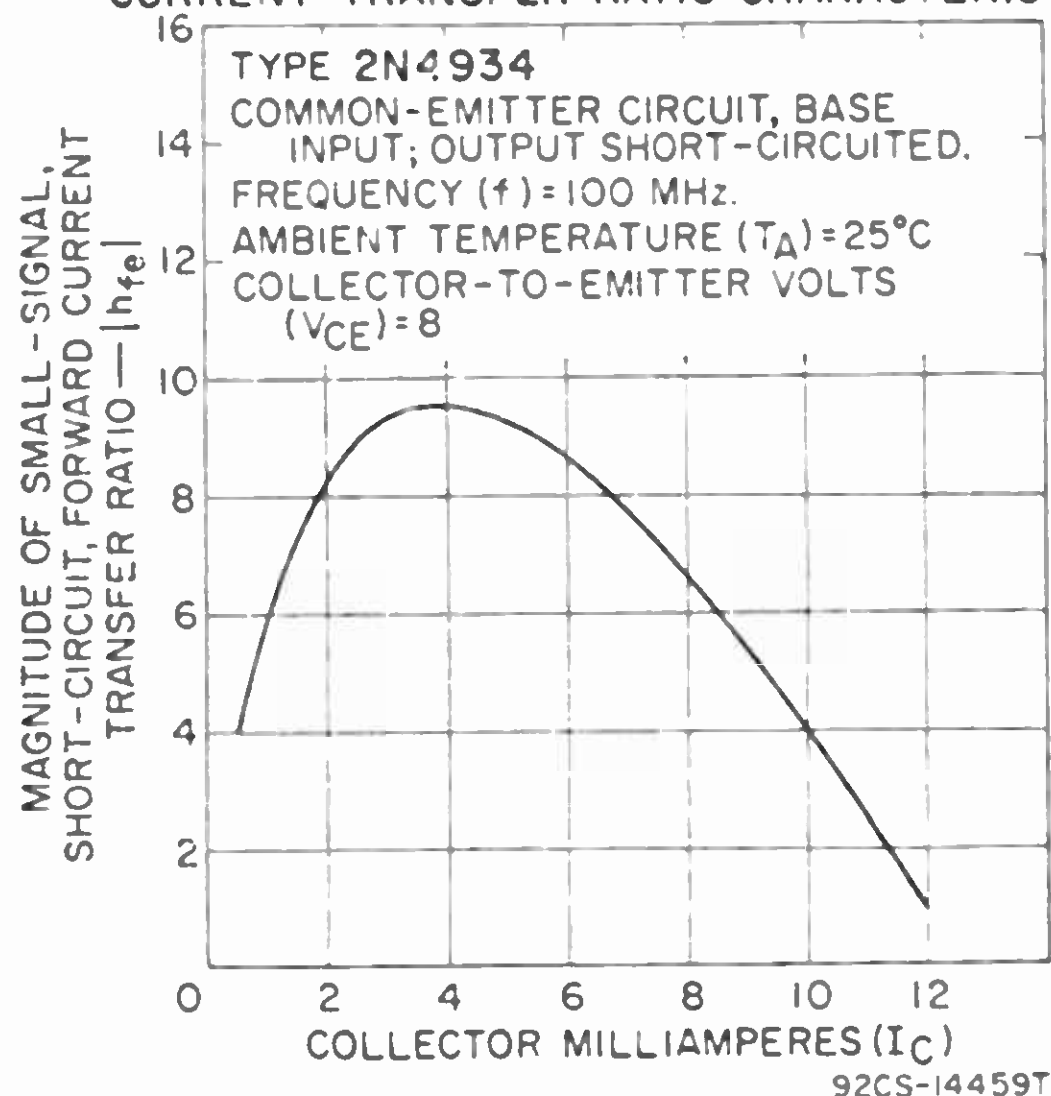
CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = 0.001$ mA, $I_E = 0$)	$V_{(BR)CB0}$	40 min	V
Collector-to-Emitter Breakdown Voltage ($I_C = 1$ mA, $I_B = 0$)	$V_{(BR)CEO}$	30 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -0.001$ mA, $I_C = 0$)	$V_{(BR)EBO}$	3 min	V
Collector-Cutoff Current ($V_{CB} = 15$ V, $I_E = 0$)	I_{CBO}	10 max	nA
Static Forward-Current Transfer Ratio ($V_{CE} = 8$ V, $I_C = 2$ mA)	h_{FE}	40 to 170	
Magnitude of Small-Signal Forward-Current Transfer Ratio:*			
$V_{CE} = 8$ V, $I_C = 2$ mA, $f = 1$ kHz	$ h_{fe} $	45 to 195	
$V_{CE} = 8$ V, $I_C = 2$ mA, $f = 100$ MHz	$ h_{fe} $	7 to 16	
Collector-to-Base Feedback Capacitance* ($V_{CB} = 8$ V, $I_E = 0$, $f = 0.1$ to 1 MHz)	C_{cb}	0.2 typ; 0.25 max	pF
Collector-to-Base Time Constant* ($V_{CB} = 8$ V, $I_E = -2$ mA, $f = 31.9$ MHz)	$r_b'C_c$	1 to 8	ps
Small-Signal Power Gain, Amplifier, Unneutralized* ($V_{CE} = 8$ V, $I_C = 2$ mA, R_G and $R_L = 50$ Ω , $f = 200$ MHz)	G_{pe}	18 to 26	dB
Noise Figure* ($V_{CE} = 8$ V, $I_C = 2$ mA, $R_s = 200$ Ω , R_G and $R_L = 50$ Ω , $f = 200$ MHz)	NF	3.5 max	dB

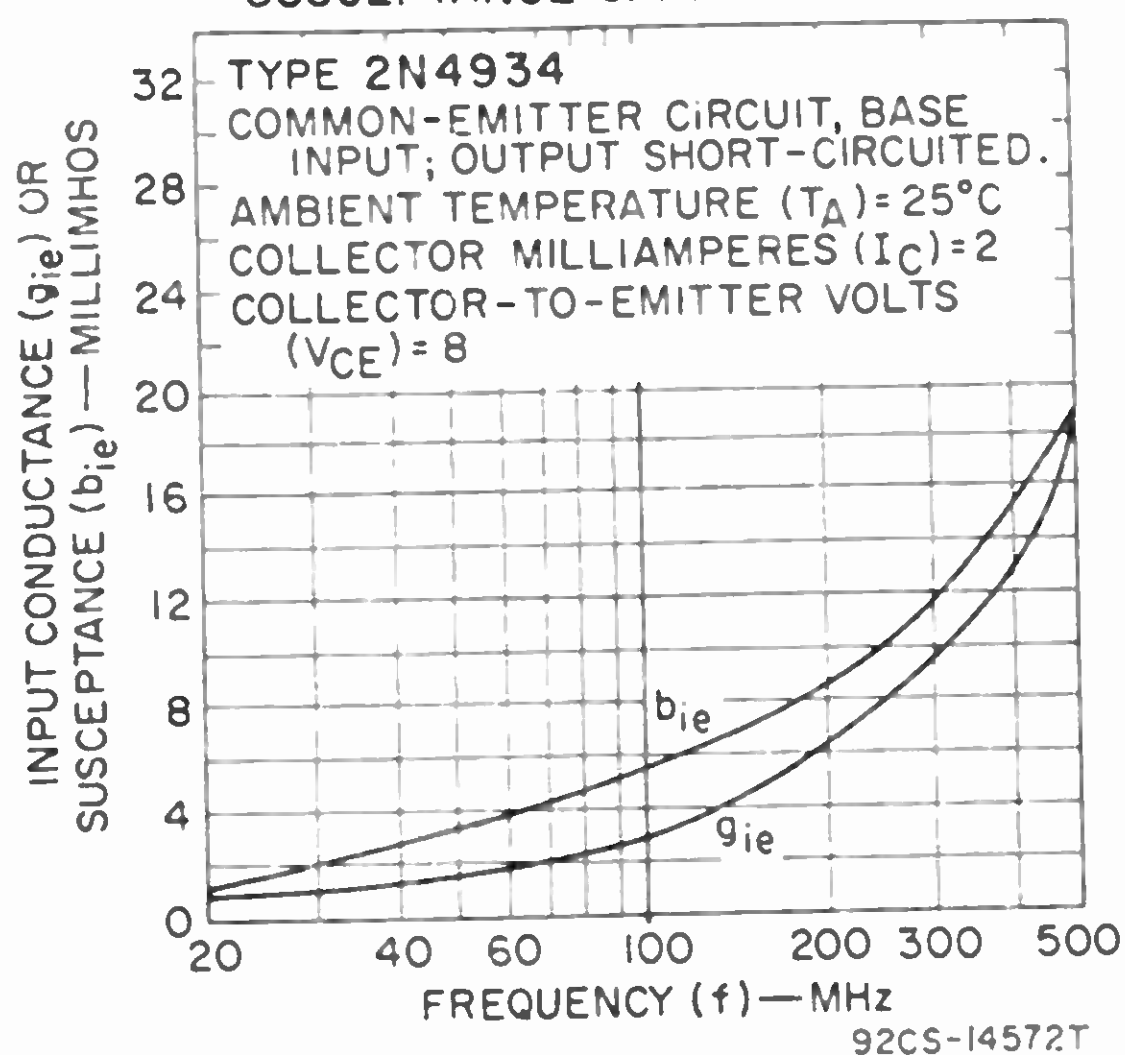
* Lead 4 (case) grounded.

▪ Three-terminal measurement with lead No. 1 (emitter) and lead No. 4 (case) connected to guard terminal

TYPICAL SMALL-SIGNAL FORWARD-CURRENT TRANSFER-RATIO CHARACTERISTIC

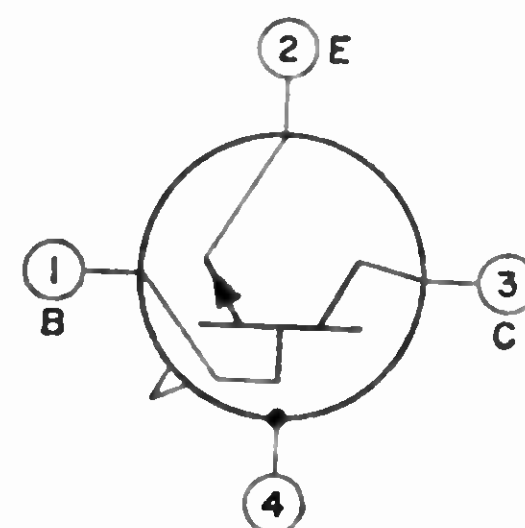


TYPICAL INPUT CONDUCTANCE AND SUSCEPTANCE CHARACTERISTICS



2N4935 TRANSISTOR

Si n-p-n epitaxial planar type used in vhf-uhf applications at frequencies up to 500 MHz. The terminal arrangement permits shielding between input and output terminals for superior high-frequency performance and greater circuit stability, particularly on printed-circuit boards. JEDEC TO-104, Outline No.31. This type is identical with type 2N4934 except for the following items:



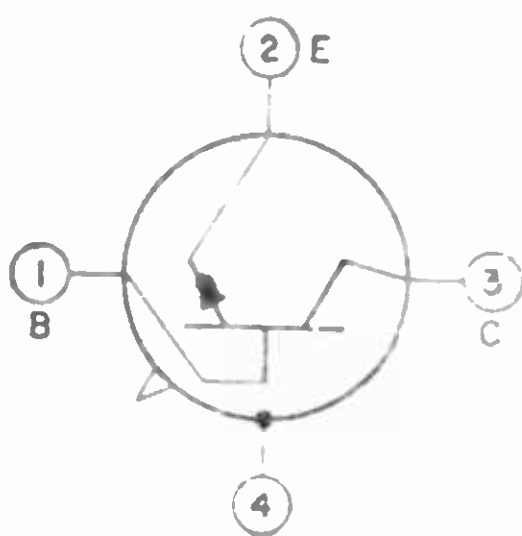
MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	50	V
Collector-to-Emitter Voltage	V_{CEO}	40	V

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = 0.001$ mA, $I_E = 0$)	$V_{(BR)CBO}$	50	V
Collector-to-Emitter Breakdown Voltage ($I_C = 1$ mA, $I_B = 0$)	$V_{(BR)CEO}$	40	V
Static Forward-Current Transfer Ratio ($V_{CE} = 8$ V, $I_C = 2$ mA)	h_{FE}	60 to 200	
Magnitude of Small-Signal Forward-Current Transfer Ratio* ($V_{CE} = 8$ V, $I_C = 2$ mA, $f = 1$ kHz)	$ h_{fe} $	70 to 225	
Collector-to-Base Time Constant* ($V_{CB} = 8$ V, $I_E = -2$ mA, $f = 31.9$ MHz)	$r_b'C_c$	1 to 6	ps
Small-Signal Power Gain, Amplifier, Unneutralized* ($V_{CE} = 8$ V, $I_C = 2$ mA, R_G and $R_L = 50$ Ω , $f = 200$ MHz)	G_{pe}	21 to 28	dB
Noise Figure* ($V_{CE} = 8$ V, $I_C = 2$ mA, $R_s = 200$ Ω , R_G and $R_L = 50$ Ω , $f = 200$ MHz)	NF	3 max	dB

* Lead 4 (case) grounded.



TRANSISTOR

2N4936

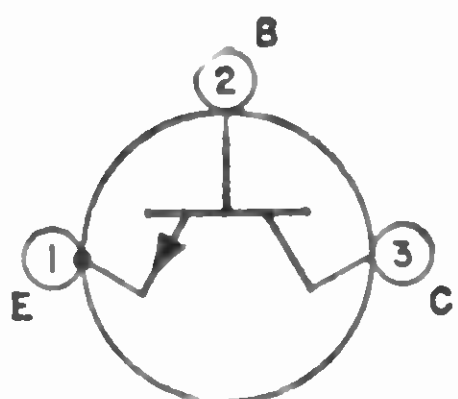
Si n-p-n epitaxial planar type used in vhf-uhf applications at frequencies up to 500 MHz. The terminal arrangement permits shielding between input and output terminals for superior high-frequency performance and greater circuit stability, particularly on printed-circuit boards. JEDEC TO-104, Outline No.31. This type is

identical with type 2N4935 except for the following items:

CHARACTERISTICS

Static Forward-Current Transfer Ratio ($V_{CE} = 8$ V, $I_C = 2$ mA)	h_{FE}	60 to 250	
Magnitude of Small-Signal Forward-Current Transfer Ratio* ($V_{CE} = 8$ V, $I_C = 2$ mA, $f = 1$ kHz)	$ h_{fe} $	70 to 280	
Small-Signal Power Gain, Amplifier, Unneutralized* ($V_{CE} = 8$ V, $I_C = 2$ mA, R_G and $R_L = 50$ Ω , $f = 450$ MHz)	G_{pe}	13 to 18	dB
Small-Signal Power Gain, Amplifier, Neutralized* ($V_{CE} = 8$ V, $I_C = 2$ mA, R_G and $R_L = 50$ Ω , $f = 450$ MHz)	G_{pe}	20	dB
Noise Figure* ($V_{CE} = 8$ V, $I_C = 2$ mA, $R_s = 100$ Ω , R_G and $R_L = 500$ Ω , $f = 450$ MHz)	NF	4.5 max	dB

* Lead 4 (case) grounded.



TRANSISTOR

2N5016

Si n-p-n "overlay" epitaxial planar type used in large-signal high-power class B and C rf amplifiers for military and industrial communications service (200 to 700 MHz). JEDEC TO-60, Outline No.23. See Mounting Hardware for desired mounting arrangement.

MAXIMUM RATINGS

Collector-to-Emitter Voltage:			
$V_{BE} = -1.5$ V	V_{CEV}	65	V
$R_{BE} = 30$ Ω	V_{CER}	40	V
Emitter-to-Base Voltage	V_{EBO}	4	V
Collector Current	I_C	4.5	A
Transistor Dissipation:			
T_c up to 50°C	P_T	30	W
T_c above 50°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Case-Soldering Temperature (10 s max)	T_c	230	°C

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Breakdown Voltage:

$R_{BE} = 30 \Omega$, $I_B = 0$, $I_C = 200 \text{ mA}$,
pulsed through an inductor $L = 25 \text{ mH}$, $df = 50\%$
 $V_{BE} = -1.5 \text{ V}$, $I_C = 200 \text{ mA}$,
pulsed through an inductor $L = 25 \text{ mH}$, $df = 50\%$

Emitter-to-Base Breakdown Voltage ($I_E = 5 \text{ mA}$,
 $I_C = 0$)

Collector-to-Emitter Saturation Voltage

($I_B = 40 \text{ mA}$, $I_C = 2000 \text{ mA}$)

Collector-Cutoff Current ($V_{CE} = 30 \text{ V}$, $I_B = 0$)

Collector-to-Base Capacitance ($V_{CB} = 30 \text{ V}$, $I_E = 0$,
 $f = 1 \text{ MHz}$)

Gain-Bandwidth Product ($V_{CE} = 15 \text{ V}$, $I_C = 500 \text{ mA}$)

RF Power Output, Unneutralized:

$V_{CE} = 28 \text{ V}$, $P_{IE} = 5 \text{ W}$, R_G and $R_L = 50 \Omega$,
 $f = 225 \text{ MHz}$

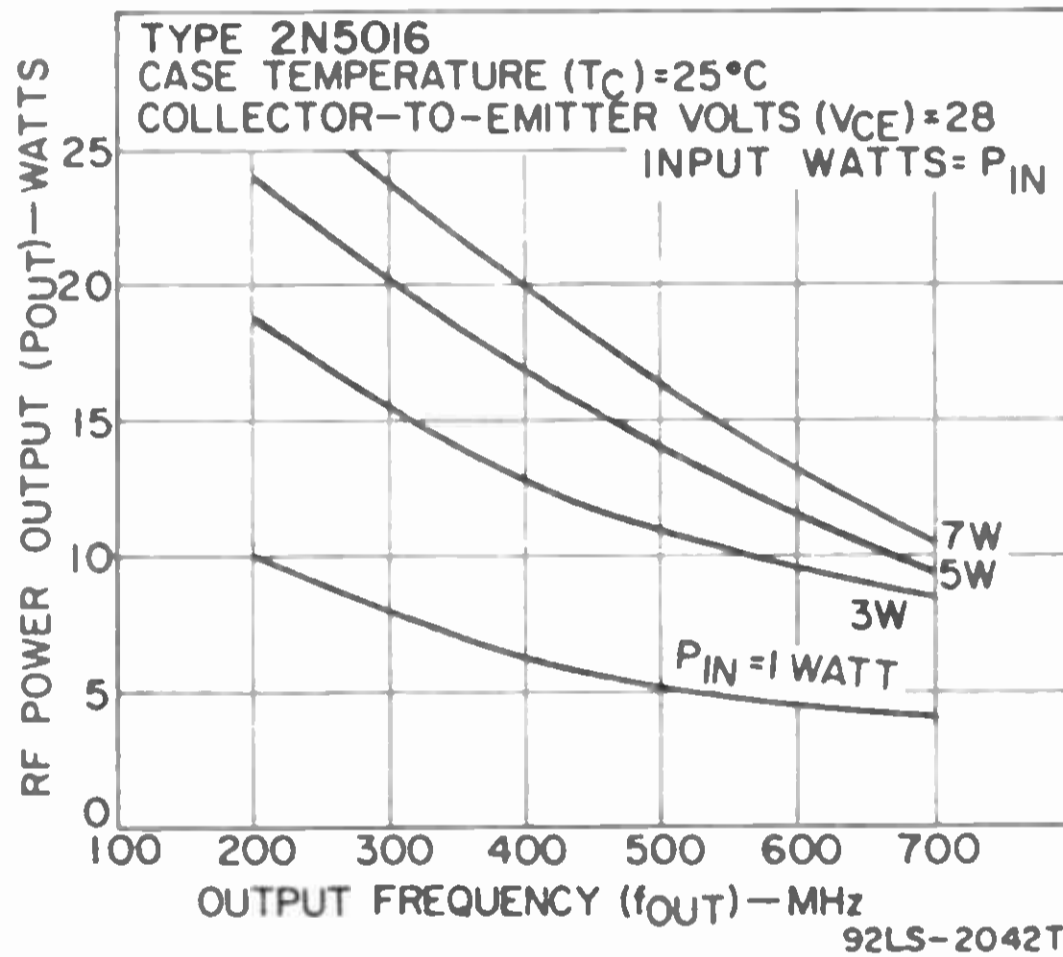
$V_{CE} = 28 \text{ V}$, $P_{IE} = 5 \text{ W}$, R_G and $R_L = 50 \Omega$,
 $f = 400 \text{ MHz}$

Dynamic Input Impedance ($V_{CE} = 28 \text{ V}$, $P_{IE} = 5 \text{ W}$,
 R_G and $R_L = 50 \Omega$, $f = 400 \text{ MHz}$)

$V_{(BR)CER}$	40 min	V
$V_{(BR)CEV(SUS)}$	65 min	V
$V_{(BR)EBO}$	4 min	V
$V_{CE(sat)}$	1 max	V
I_{CEO}	10 max	mA
C_{cb}	25	pF
f_T	600	MHz
P_{OE}	23*	W
P_{OE}	15▪	W
	$2.5 + j5▪$	Ω

- * For conditions given, minimum efficiency = 60 per cent.
- For conditions given, minimum efficiency = 50 per cent.

TYPICAL POWER-OUTPUT CHARACTERISTICS



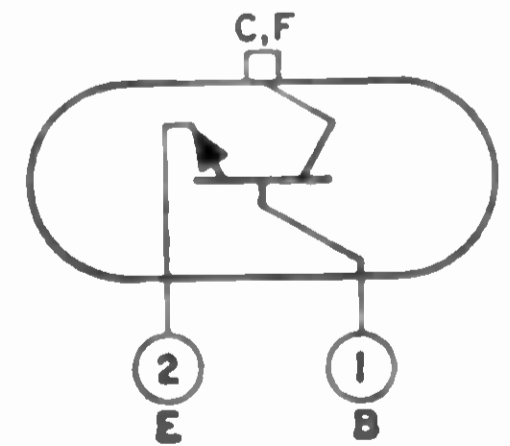
2N5017

Refer to Chart of Discontinued Transistors

2N5034

POWER TRANSISTOR

Si n-p-n type featuring a base comprised of a homogeneous-resistivity silicon material and molded silicone plastic package with vertical leads. This type fits a standard TO-3 socket. It is used in a wide variety of high-power switching and amplifier applications such as series and shunt regulators, drivers, and output stages for high-fidelity amplifiers. Outline No.50. See Mounting Hardware for desired mounting arrangement.



MAXIMUM RATINGS

Collector-to-Base Voltage
Collector-to-Emitter Sustaining Voltage:
 $V_{BE} = -1.5 \text{ V}$
 $R_{BE} = 100 \Omega$
Base open
Emitter-to-Base Voltage
Collector Current
Peak Collector Current
Base Current
Transistor Dissipation:
 T_c up to 25°C
 T_c above 25°C

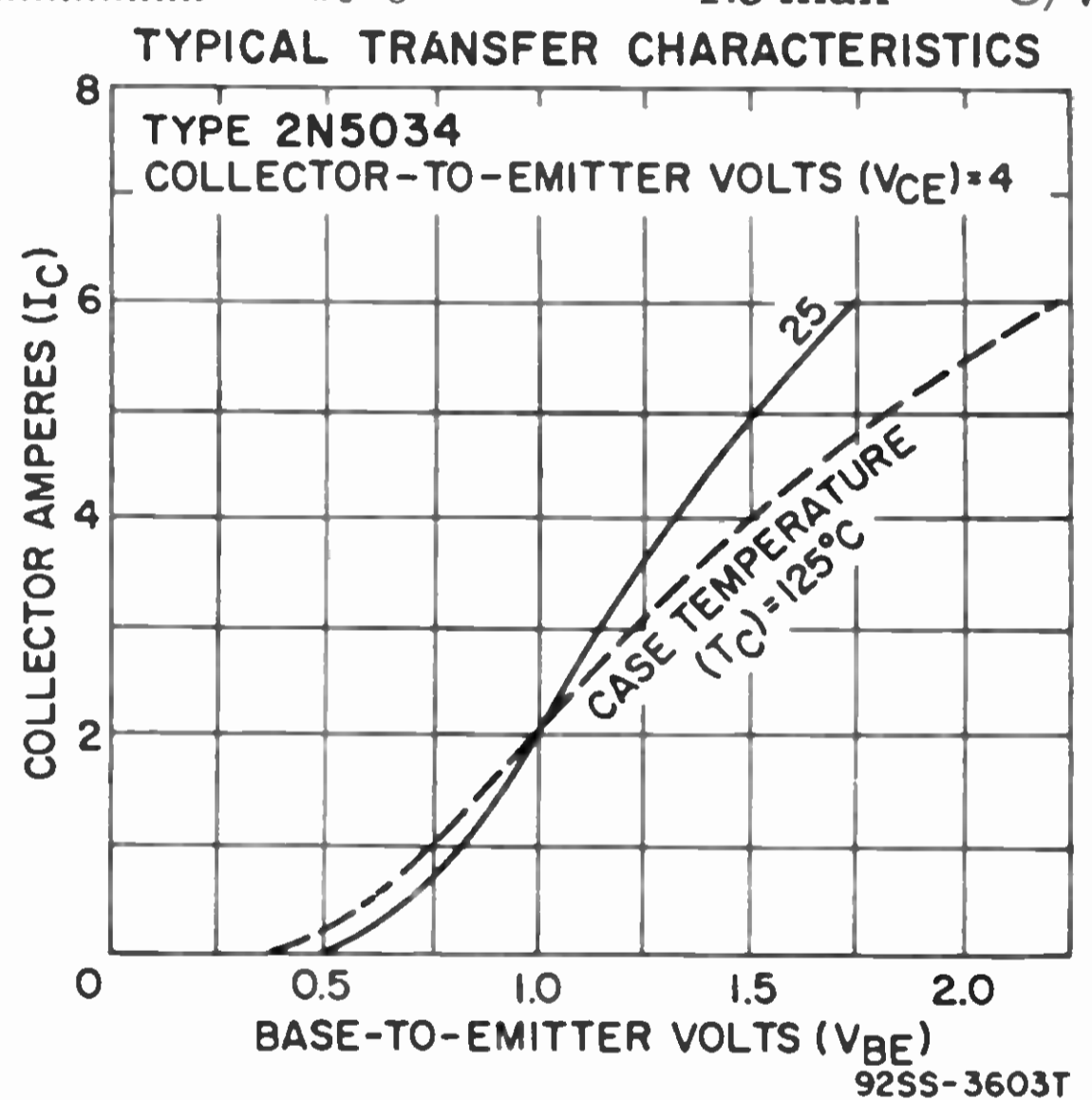
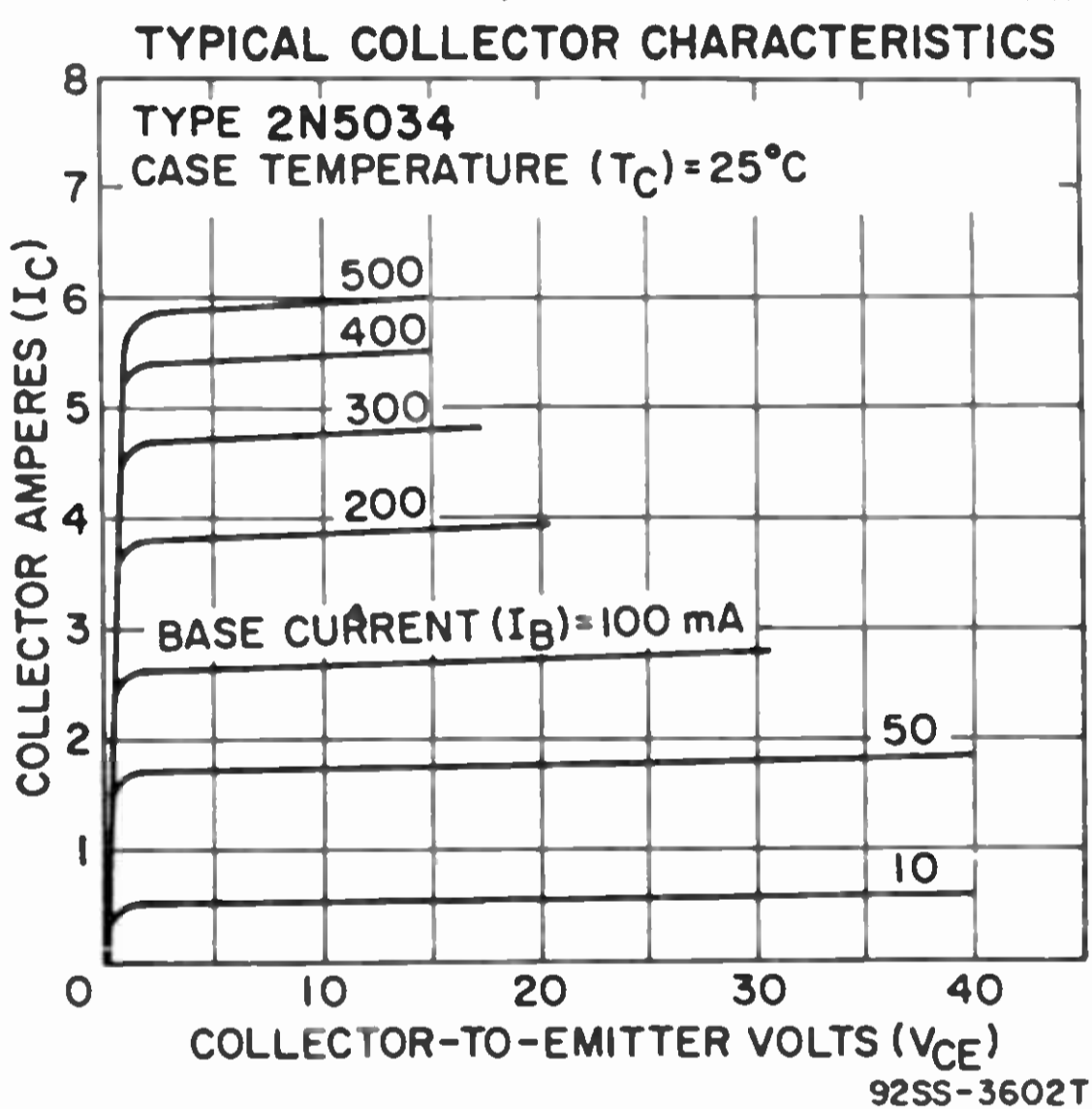
V_{CBO}	55	V
$V_{CEV(SUS)}$	55	V
$V_{CER(SUS)}$	45	V
$V_{CEO(SUS)}$	40	V
V_{EBO}	5	V
I_C	6	A
i_C	12	A
I_B	6	A
P_T	83	W
P_T	See curve page 300	

MAXIMUM RATINGS (cont'd)

Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 150	°C
Storage	T_{STG}	-65 to 150	°C
Lead-Soldering Temperature (10 s max)	T_L	235	°C

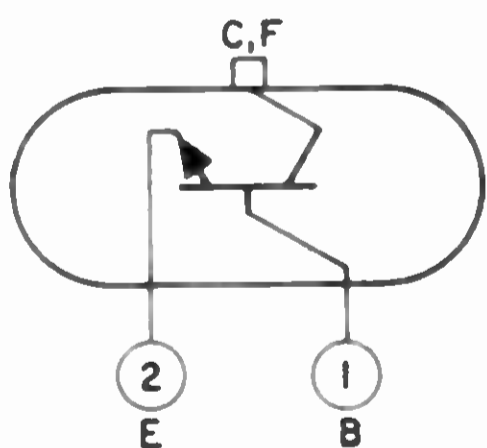
CHARACTERISTICS (At case temperature = 25°C)

Emitter-to-Base Breakdown Voltage ($I_E = 5$ mA, $I_C = 0$)	$V_{(BR)EBO}$	5 min	V
Collector-to-Emitter Sustaining Voltage:			
$I_C = 0.2$ A, $I_B = 0$, $t_p = 300$ μ s, $df = 1.8\%$	$V_{CEO(SUS)}$	40 min	V
$V_{BE} = -1.5$ V, $I_C = 0.1$ A, $t_p = 300$ μ s, $df = 1.8\%$...	$V_{CEV(SUS)}$	55 min	V
$R_{BE} = 100$ Ω , $I_C = 0.2$ A, $t_p = 300$ μ s, $df = 1.8\%$...	$V_{CER(SUS)}$	45 min	V
Base-to-Emitter Voltage ($V_{CE} = 4$ V, $I_C = 2.5$ A, $t_p = 300$ μ s, $df = 1.8\%$)	V_{BE}	1.7 max	V
Collector-to-Emitter Saturation Voltage ($I_C = 2.5$ A, $I_B = 0.25$ A, $t_p = 300$ μ s, $df = 1.8\%$)	$V_{CE(sat)}$	1 max	V
Collector-Cutoff Current:			
$V_{CE} = 35$ V, $R_{BE} = 100$ Ω	I_{CER}	1 max	mA
$V_{CE} = 35$ V, $R_{BE} = 100$ Ω , $T_C = 150^\circ$ C	I_{CER}	5 max	mA
$V_{CE} = 50$ V, $V_{BE} = -1.5$ V	I_{CEV}	1 max	mA
$V_{CE} = 50$ V, $V_{BE} = -1.5$ V, $T_C = 150^\circ$ C	I_{CEV}	5 max	mA
Emitter-Cutoff Current ($V_{EB} = 5$ V, $I_C = 0$)	I_{EBO}	5 max	mA
Pulsed Static Forward-Current Transfer Ratio ($V_{CE} = 4$ V, $I_C = 2.5$ A, $t_p = 300$ μ s, $df = 1.8\%$)	h_{FE} (pulsed)	20 to 70	
Gain-Bandwidth Product ($V_{CE} = 4$ V, $I_C = 0.5$ A)	f_T	0.8 to 2.8	MHz
Thermal Resistance, Junction-to-Case	θ_{J-C}	1.5 max	°C/W



POWER TRANSISTOR

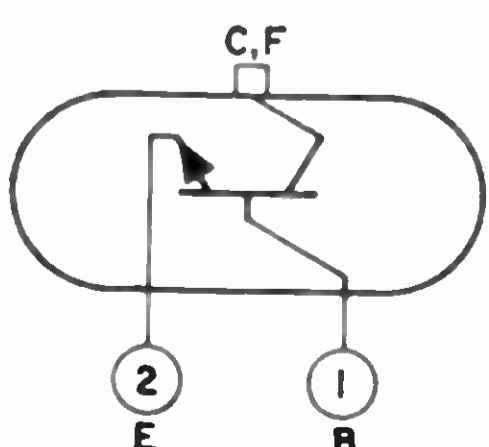
2N5035



Si n-p-n type featuring a base comprised of a homogeneous-resistivity silicon material and molded silicone plastic package having horizontal leads for mounting on printed-circuit boards. It is used in a wide variety of high-power switching and amplifier applications such as series and shunt regulators, drivers, and output stages for high-fidelity amplifiers. Outline No.51. See Mounting Hardware for desired mounting arrangement. This type is electrically identical to type 2N5034.

POWER TRANSISTOR

2N5036



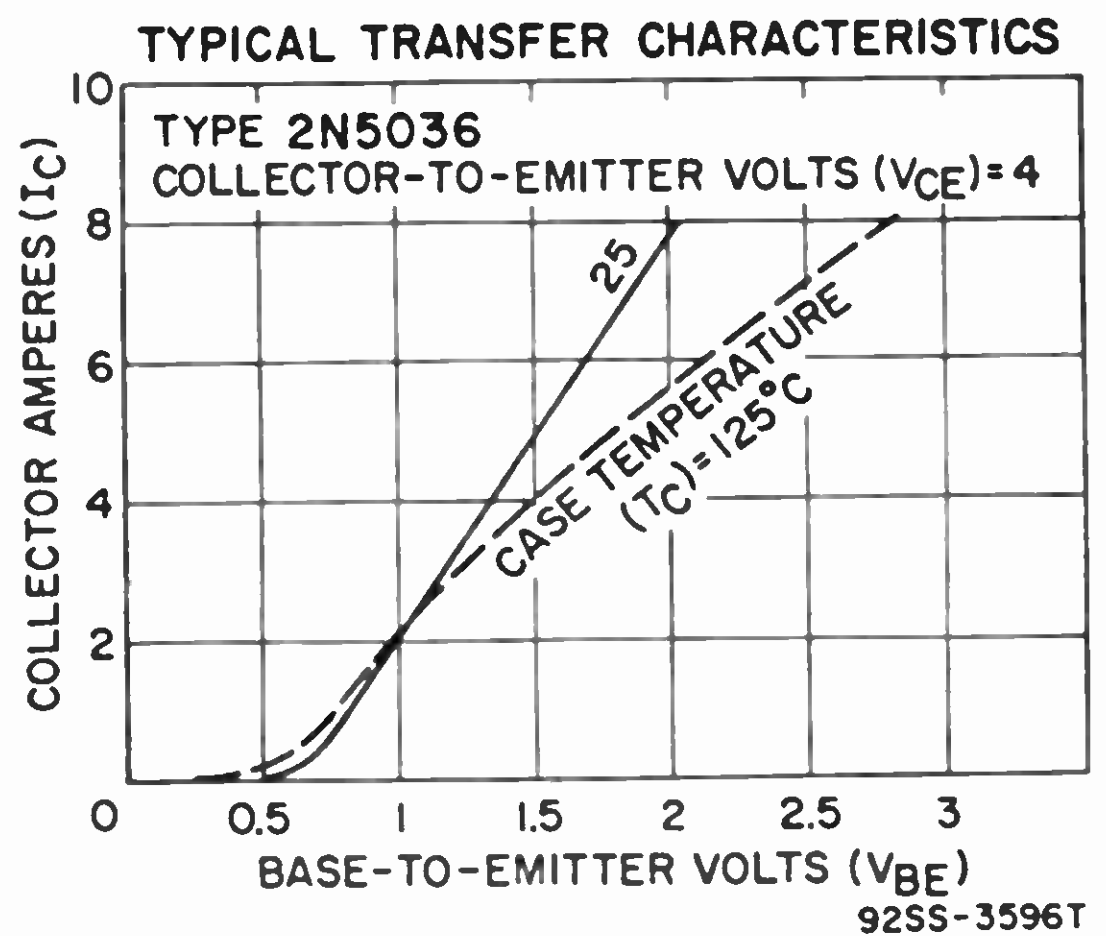
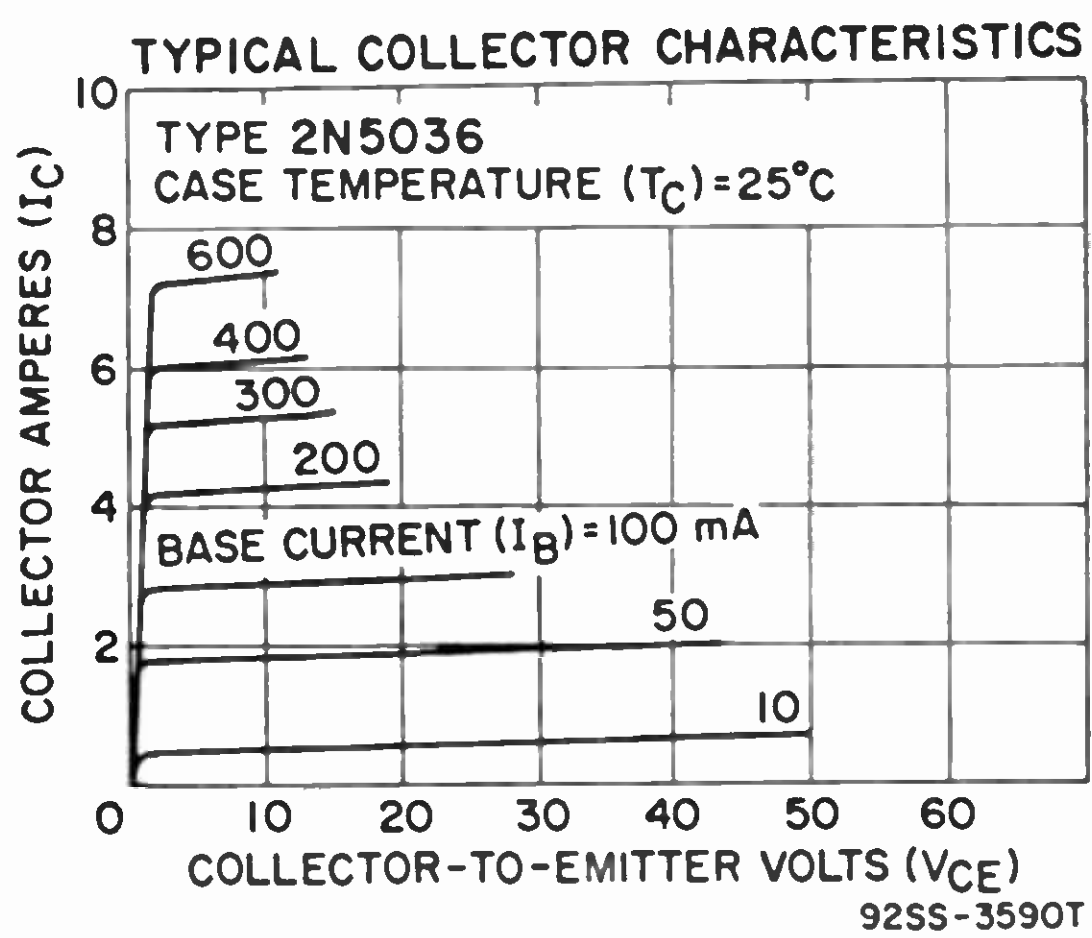
Si n-p-n type featuring a base comprised of a homogeneous-resistivity silicon material and molded silicone plastic package with vertical leads. This type fits a standard TO-3 socket. It is used in a wide variety of high-power switching and amplifier applications such as series and shunt regulators, drivers, and output stages for high-fidelity amplifiers. Outline No.50. See Mounting Hardware for desired mounting arrangement.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	70	V
Collector-to-Emitter Sustaining Voltage:			
$V_{BE} = -1.5$ V	$V_{CEV(SUS)}$	70	V
$R_{BE} = 100$ Ω	$V_{CER(SUS)}$	60	V
Base open	$V_{CEO(SUS)}$	50	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	8	A
Peak Collector Current	i_C	12	A
Base Current	I_B	6	A
Transistor Dissipation:			
T_C up to 25°C	P_T	83	W
T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 150	°C
Storage	T_{STG}	-65 to 150	°C
Lead-Soldering Temperature (10 s max)	T_L	235	°C

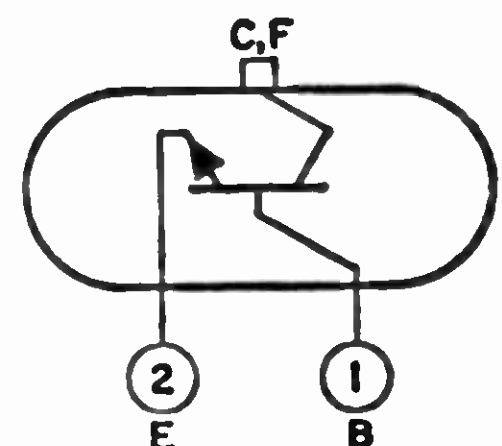
CHARACTERISTICS (At case temperature = 25°C)

Emitter-to-Base Breakdown Voltage ($I_E = 5$ mA, $I_C = 0$)	$V_{(BR)EBO}$	5 min	V
Collector-to-Emitter Sustaining Voltage:			
$I_C = 0.2$ A, $I_B = 0$, $t_p = 300$ μ s, $df = 1.8\%$	$V_{CEO(SUS)}$	50 min	V
$V_{BE} = -1.5$ V, $I_C = 0.1$ A, $t_p = 300$ μ s, $df = 1.8\%$...	$V_{CEV(SUS)}$	70 min	V
$R_{BE} = 100$ Ω , $I_C = 0.2$ A, $t_p = 300$ μ s, $df = 1.8\%$	$V_{CER(SUS)}$	60 min	V
Base-to-Emitter Voltage ($V_{CE} = 4$ V, $I_C = 3$ A, $t_p = 300$ μ s, $df = 1.8\%$)	V_{BE}	1.7 max	V
Collector-to-Emitter Saturation Voltage ($I_C = 3$ A, $t_p = 300$ μ s, $df = 1.8\%$, $I_B = 0.3$ A)	$V_{CE(sat)}$	1 max	V
Collector-Cutoff Current:			
$V_{CE} = 50$ V, $R_{BE} = 100$ Ω	I_{CER}	1 max	mA
$V_{CE} = 50$ V, $R_{BE} = 100$ Ω , $T_C = 150^\circ$ C	I_{CER}	5 max	mA
$V_{CE} = 65$ V, $V_{BE} = -1.5$ V	I_{CEV}	1 max	mA
$V_{CE} = 65$ V, $V_{BE} = -1.5$ V, $T_C = 150^\circ$ C	I_{CEV}	5 max	mA
Emitter-Cutoff Current ($V_{EB} = 5$ V, $I_C = 0$)	I_{EBO}	5 max	mA
Pulsed Static Forward-Current Transfer Ratio ($V_{CE} = 4$ V, $I_C = 3$ A, $t_p = 300$ μ s, $df = 1.8\%$)	$h_{FE}(pulsed)$	20 to 70	
Gain-Bandwidth Product ($V_{CE} = 4$ V, $I_C = 0.5$ A)	f_T	0.8 to 2.8	MHz
Thermal Resistance, Junction-to-Case	θ_{J-C}	1.5 max	°C/W



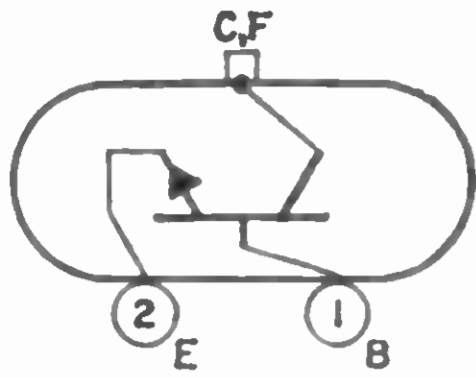
2N5037 POWER TRANSISTOR

Si n-p-n type featuring a base comprised of a homogeneous-resistivity silicon material and molded silicone plastic package having horizontal leads for mounting on printed-circuit boards. It is used in a wide variety of high-power switching and amplifier applications such as series and shunt regulators, drivers, and output stages for high-fidelity amplifiers. Outline No.51. See Mounting Hardware for desired mounting arrangement. This type is electrically identical to type 2N5036.



POWER TRANSISTOR

2N5038



Si n-p-n epitaxial type used for high-current, high-power, high-speed applications in switching and amplifier circuits in industrial and commercial equipment. JEDEC TO-3, Outline No.2. See Mounting Hardware for desired mounting arrangement.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CB0}	150	V
Collector-to-Emitter Sustaining Voltage: $V_{BE} = -1.5$ V, $R_{BE} = 100$ Ω	$V_{CEX(SUS)}$	150	V
$R_{BE} \leq 50$ Ω	$V_{CER(SUS)}$	110	V
Base open	$V_{CEO(SUS)}$	90	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Peak Collector Current	i_c	30	A
Collector Current	I_C	20	A
Base Current	I_B	5	A
Transistor Dissipation:			
T_c up to 25°C, V_{CE} up to 28 V	P_T	140	W
T_c up to 25°C, V_{CE} above 28 V		See curve page 300	
T_c above 25°C, V_{CE} above 28 V		See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Pin-Soldering Temperature (10 s max)	T_P	230	°C

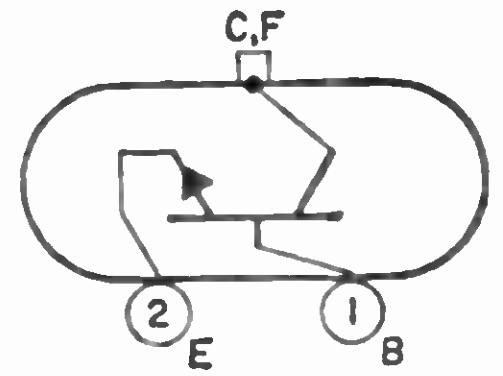
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage: $I_C = 0.2$ A, $I_B = 0$, base open	$V_{CEO(SUS)}$	90 min	V
$V_{BE} = -1.5$ V, $I_C = 0.2$ A, $I_B = 0$, $R_{BE} = 100$ Ω , base-emitter junction reverse biased	$V_{CEX(SUS)}$	150 min	V
$I_C = 0.2$ A, $I_B = 0$, $R_{BE} \leq 50$ Ω	$V_{CER(SUS)}$	110 min	V
Emitter-to-Base Voltage ($I_C = 0$, $i_E = 0.05$ A)	V_{EBO}	7 min	V
Collector-to-Emitter Saturation Voltage: $I_C = 12$ A, $I_B = 1.2$ A, $t_P \leq 350$ μ s, $df = 2\%$	$V_{CE(sat)}$	1 max	V
$I_C = 20$ A, $I_B = 5$ A	$V_{CE(sat)}$	2.5 max	V
Base-to-Emitter Saturation Voltage ($V_{CE} = 5$ V, $I_C = 20$ A, $I_B = 5$ A)	$V_{BE(sat)}$	3.3 max	V
Base-to-Emitter Voltage ($V_{CE} = 5$ V, $I_C = 12$ A, $t_P \leq 350$ μ s, $df = 2\%$)	V_{BE}	1.8 max	V
Collector-Cutoff Current:			
$V_{CE} = 70$ V, $I_B = 0$	I_{CEO}	20 max	mA
$V_{CE} = 140$ V, $V_{BE} = -1.5$ V	I_{CEV}	50 max	mA
$V_{CE} = 100$ V, $V_{BE} = -1.5$ V	I_{CEV}	10 max	mA
$V_{CE} = 100$ V, $V_{BE} = -1.5$ V, $T_c = 150^\circ$ C	I_{CEV}	10 max	mA
Emitter-Cutoff Current:			
$V_{EB} = 5$ V, $I_C = 0$	I_{EBO}	5 max	mA
$V_{EB} = 7$ V, $I_C = 0$	I_{EBO}	50 max	mA
Pulsed Static Forward-Current Transfer Ratio: $V_{CE} = 5$ V, $I_C = 2$ A, $t_P \leq 350$ μ s, $df = 2\%$	$h_{FE}(pulsed)$	50 to 200	
$V_{CE} = 5$ V, $I_C = 12$ A, $t_P \leq 350$ μ s, $df = 2\%$	$h_{FE}(pulsed)$	20 to 100	
Magnitude of Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 10$ V, $I_C = 2$ A, $f = 5$ MHz)	$ h_{FE} $	12 min	
Output Capacitance ($V_{CB} = 10$ V, $I_E = 0$, $f = 1$ MHz)	C_{ob0}	500 max	pF
Second-Breakdown Collector Current: $V_{CE} = 28$ V, base forward-biased, non-repetitive pulse = 1 s	$I_{S/b}$	5 min	A
$V_{CE} = 45$ V, base forward-biased, non-repetitive pulse = 1 s	$I_{S/b}$	0.9 min	A
Second-Breakdown Energy ($V_{BE} = -4$ V, $I_C = 12$ A, $R_B = 20$ Ω , $L = 180$ μ H, base reverse biased)	$E_{S/b}$	13 min	mJ
Gain-Bandwidth Product ($V_{CE} = 10$ V, $I_C = 2$ A, $f = 5$ MHz)	f_T	60 min	MHz
Turn-On-Time ($V_{CC} = 30$ V, $I_C = 12$ A, $I_{B1} = I_{B2} = 1.2$ A)	$t_d + t_r$	0.5 max	μ s
Storage Time ($V_{CC} = 30$ V, $I_C = 12$ A, $I_{B1} = I_{B2} = 1.2$ A)	t_s	1.5 max	μ s
Fall Time ($V_{CC} = 30$ V, $I_C = 12$ A, $I_{B1} = I_{B2} = 1.2$ A)	t_f	0.5 max	μ s
Thermal Resistance, Junction-to-Case ($V_{CE} = 40$ V, $I_C = 0.5$ A)	θ_{J-C}	1.25 max	°C/W

2N5039

POWER TRANSISTOR

Si n-p-n epitaxial type used for high-current, high-power, high-speed applications in switching and amplifier circuits in industrial and commercial equipment. JEDEC TO-3, Outline No.2. See Mounting Hardware for desired mounting arrangement. This type is identical with type 2N5038 except for the following items:



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	120	V
Collector-to-Emitter Sustaining Voltage: $V_{BE} = -1.5$ V, $R_{BE} = 100$ Ω	$V_{CEX(sus)}$	120	V
$R_{BE} \leq 50$ Ω	$V_{CER(sus)}$	95	V
Base open	$V_{CEO(sus)}$	75	V

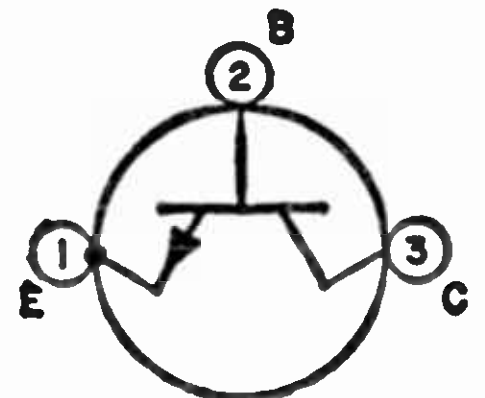
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage: $I_C = 0.2$ A, $I_B = 0$, base open	$V_{CEO(sus)}$	75 min	V
$V_{BE} = -1.5$ V, $I_C = 0.2$ A, $I_B = 0$, $R_{BE} = 100$ Ω , base-emitter junction reverse biased	$V_{CEX(sus)}$	120 min	V
$I_C = 0.2$ A, $I_B = 0$, $R_{BE} \leq 50$ Ω	$V_{CER(sus)}$	95 min	V
Collector-to-Emitter Saturation Voltage: $I_C = 10$ A, $I_B = 1$ A, $t_P \leq 350$ μ s, $df = 2\%$	$V_{CE(sat)}$	1 max	V
$I_C = 20$ A, $I_B = 5$ A	$V_{CE(sat)}$	2.5 max	V
Base-to-Emitter Voltage ($V_{CE} = 5$ V, $I_C = 10$ A, $t_P \leq 350$ μ s, $df = 2\%$)	V_{BE}	1.8 max	V
Collector-Cutoff Current: $V_{CE} = 55$ V, $I_B = 0$	I_{CEO}	20 max	mA
$V_{CE} = 110$ V, $V_{BE} = -1.5$ V	I_{CEV}	50 max	mA
$V_{CE} = 85$ V, $V_{BE} = -1.5$ V	I_{CEV}	10 max	mA
$V_{CE} = 85$ V, $V_{BE} = -1.5$ V	I_{CEV}	10 max	mA
Emitter-Cutoff Current: $V_{EB} = 5$ V, $I_C = 0$	I_{EBO}	15 max	mA
$V_{EB} = 7$ V, $I_C = 0$	I_{EBO}	50 max	mA
Pulsed Static Forward-Current Transfer Ratio $V_{CE} = 5$ V, $I_C = 2$ A, $t_P \leq 350$ μ s, $df = 2\%$	$h_{FE}(pulsed)$	30 to 150	
$V_{CE} = 5$ V, $I_C = 10$ A, $t_P \leq 350$ μ s, $df = 2\%$	$h_{FE}(pulsed)$	20 to 100	
Turn-On-Time ($V_{CC} = 30$ V, $I_C = 10$ A, $I_{B1} = I_{B2} = 1$ A)	$t_d + t_r$	0.5 max	μ s
Storage Time ($V_{CC} = 30$ V, $I_C = 10$ A, $I_{B1} = I_{B2} = 1$ A)	t_s	1.5 max	μ s
Fall Time ($V_{CC} = 30$ V, $I_C = 10$ A, $I_{B1} = I_{B2} = 1$ A)	t_f	0.5 max	μ s

2N5070

TRANSISTOR

Si n-p-n "overlay" epitaxial planar type used in high-power class A or B service in a 2-to-30-MHz single-sideband power amplifier operating from a 28-volt power supply. JEDEC TO-60, Outline No.23. See Mounting Hardware for desired mounting arrangement.



MAXIMUM RATINGS

Collector-to-Emitter Voltage: $V_{BE} = -1.5$ V	V_{CEV}	65	V
$R_{BE} = 5$ Ω	V_{CER}	40	V
Emitter-to-Base Voltage	V_{EBO}	4	V
Collector Current	I_C	3.3	A
Peak Collector Current	i_C	10	A
Transistor Dissipation: T_C up to 25°C	P_T	70	W
T_C above 25°C	P_T	See curve page 300	
Temperature Range: Operating (Junction)	$T_J(opr)$	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	230	°C

CHARACTERISTICS (At case temperature = 25°C)

Emitter-to-Base Breakdown Voltage ($I_E = 10$ mA, $I_C = 0$)	$V_{(BR)EBO}$	4 min	V
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CHARACTERISTICS (cont'd)

Collector-to-Emitter Sustaining Voltage:

$V_{BE} = -1.5 \text{ V}, I_C = 200 \text{ mA}$	$V_{CEV} \text{ (sus)}$	65 min	V
$R_{BE} = 5 \Omega, I_C = 200 \text{ mA}$	$V_{CER} \text{ (sus)}$	40 min	V

Collector-Cutoff Current:

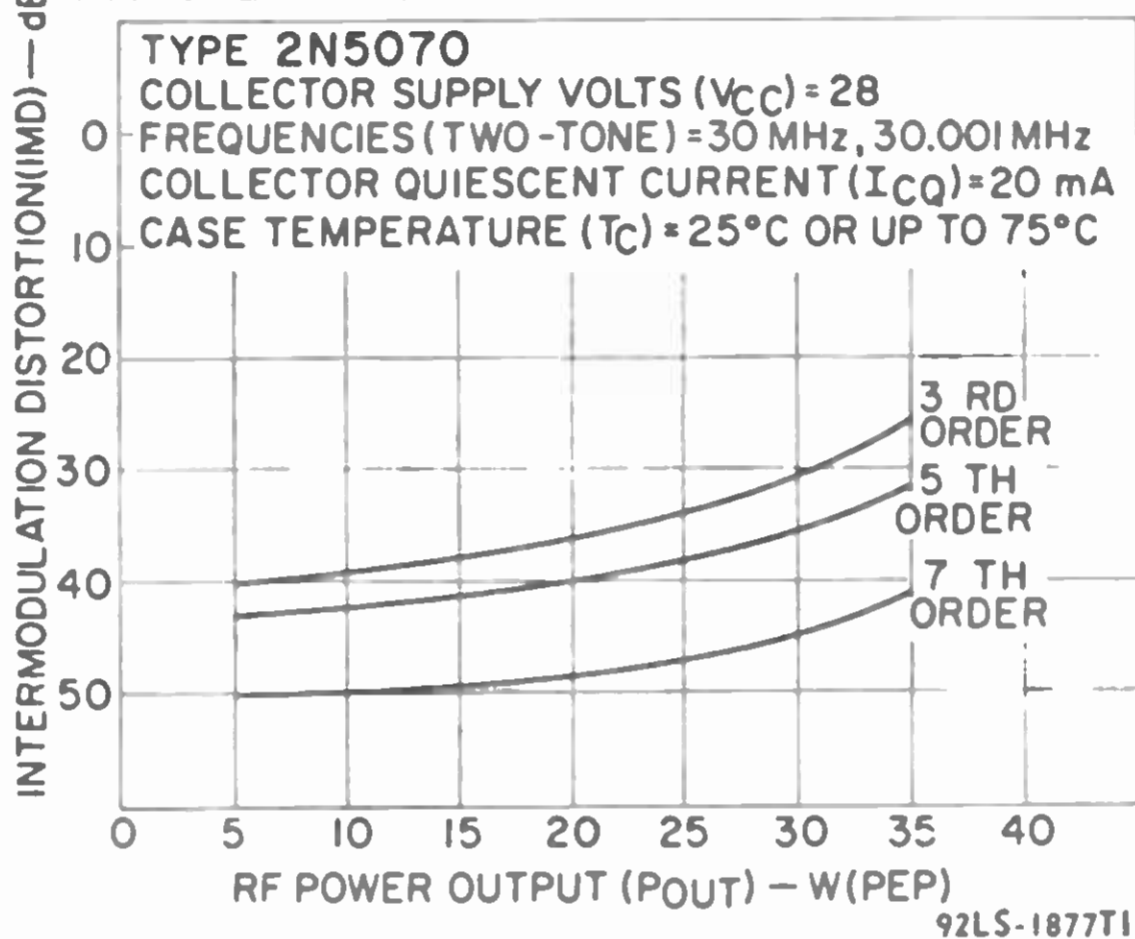
$V_{CE} = 30 \text{ V}, I_B = 0$	I_{CEO}	5 max	mA
$V_{CB} = 30 \text{ V}, I_E = 0$	I_{CBO}	10 max	mA

Output Capacitance ($V_{CB} = 1 \text{ V}, I_E = 0, f = 1 \text{ MHz}$)	C_{obo}	85 max	pF
Thermal Resistance, Junction-to-Case	θ_{J-C}	2.5 max	$^{\circ}\text{C/W}$

TYPICAL OPERATION IN RF-AMPLIFIER CIRCUIT

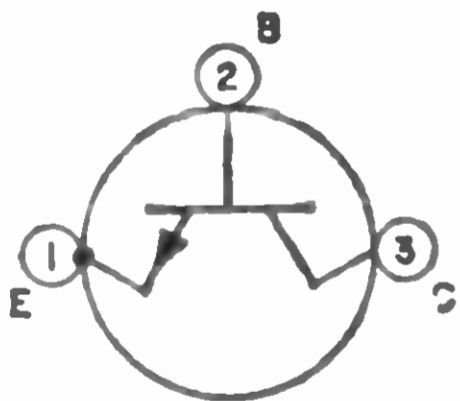
Collector Supply Voltage	28	V
Collector Base Current	20	mA
RF Power Output:		
Average	12.5 min	W
Peak Envelope	25 min	W
Intermodulation Distortion	30 max	dB
Collector Efficiency	40 min	%

TYPICAL RF POWER-OUTPUT CHARACTERISTICS



TRANSISTOR

2N5071



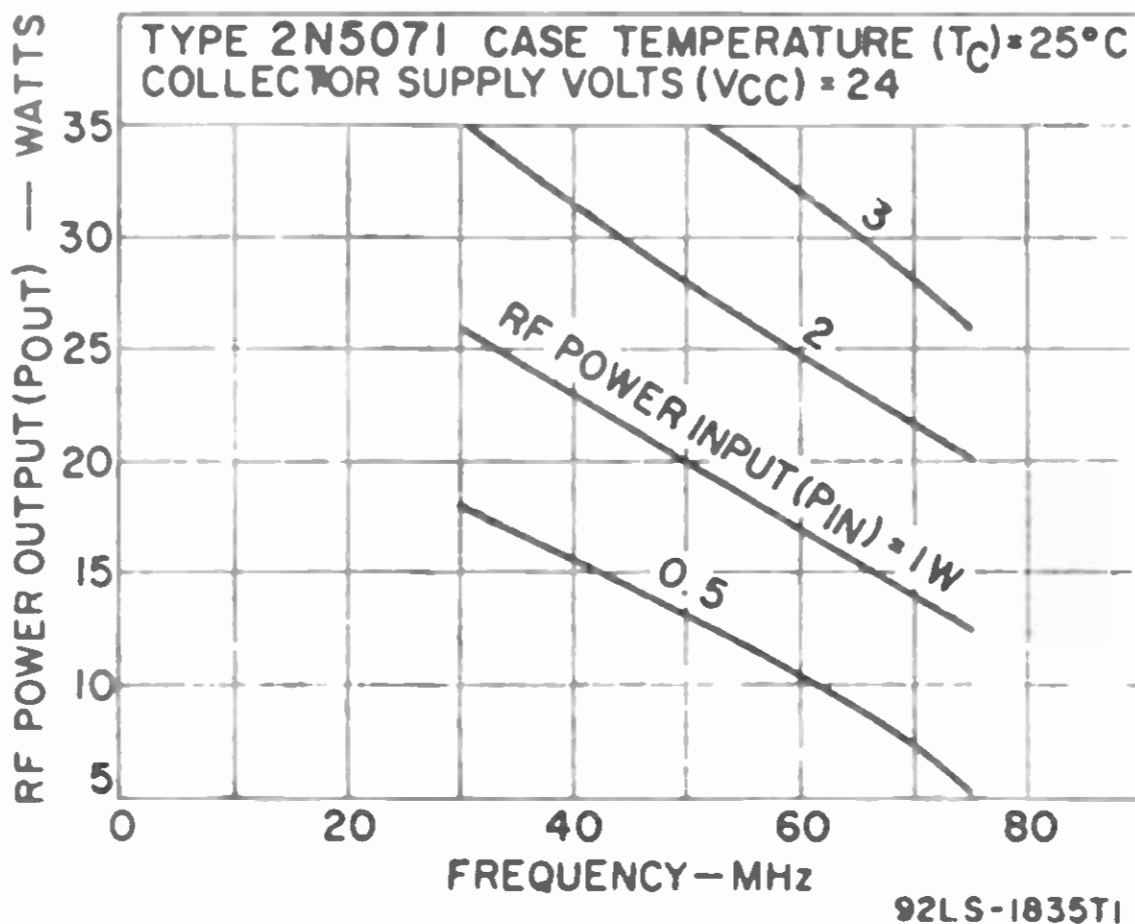
Si n-p-n "overlay" epitaxial planar type used in high-power class A and C rf amplifiers for FM communications with a 24-volt power supply. It is used for narrow-band and wideband applications in the 30-to-76-MHz frequency range. JEDEC TO-60, Outline No.23. See **Mounting Hardware** for desired mounting arrangement.

For maximum ratings, refer to type 2N5070.

CHARACTERISTICS (At case temperature = 25°C)

Emitter-to-Base Breakdown Voltage ($I_E = 10 \text{ mA}, I_C = 0$)	$V_{(BR)EBO}$	4 min	V
Collector-to-Emitter Sustaining Voltage:			
$V_{BE} = -1.5 \text{ V}, I_C = 200 \text{ mA}$	$V_{CEV} \text{ (sus)}$	65 min	V
$R_{BE} = 5 \Omega, I_C = 200 \text{ mA}$	V_{CER}	40 min	V

TYPICAL RF POWER-OUTPUT CHARACTERISTICS



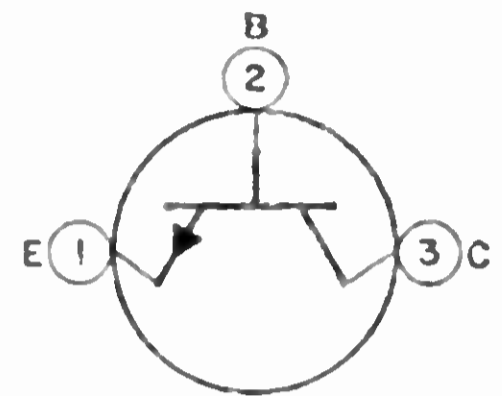
CHARACTERISTICS (cont'd)

Collector-to-Emitter Cutoff Current ($V_{CE} = 30\text{ V}$, $I_B = 0$)	I_{CEO}	5 max	mA
Collector-to-Base Cutoff Current ($V_{CE} = 60\text{ V}$, $I_E = 0$)	I_{CBO}	10 max	mA
Output Capacitance ($V_{CB} = 30\text{ V}$, $I_E = 0$, $f = 1\text{ MHz}$)	C_{obo}	85 max	pF
Power Output:			
Narrowband Amplifier ($V_{CE} = 24\text{ V}$, $P_{IE} = 3\text{ W}$, R_G and $R_L = 50\ \Omega$, $f = 76\text{ MHz}$)	P_{OE}	24• min	W
Wideband Amplifier ($V_{CE} = 24\text{ V}$, $P_{IE} = 3\text{ W}$, R_G and $R_L = 50\ \Omega$, $f = 30$ to 76 MHz)	P_{OE}	15* min	W
Thermal Resistance, Junction-to-Case	θ_{J-C}	2.5	$^{\circ}\text{C}/\text{W}$

- For conditions given, minimum efficiency = 60 per cent.
- * For conditions given, minimum efficiency = 35 per cent.

2N5090 POWER TRANSISTOR

Si n-p-n "overlay" epitaxial planar type used in class A, B, or C amplifier frequency-multiplier, or oscillator circuits; it is used in output, driver, or pre-driver, stages in vhf and uhf equipment. JEDEC TO-60, Outline No.23. See Mounting Hardware for desired mounting arrangement.



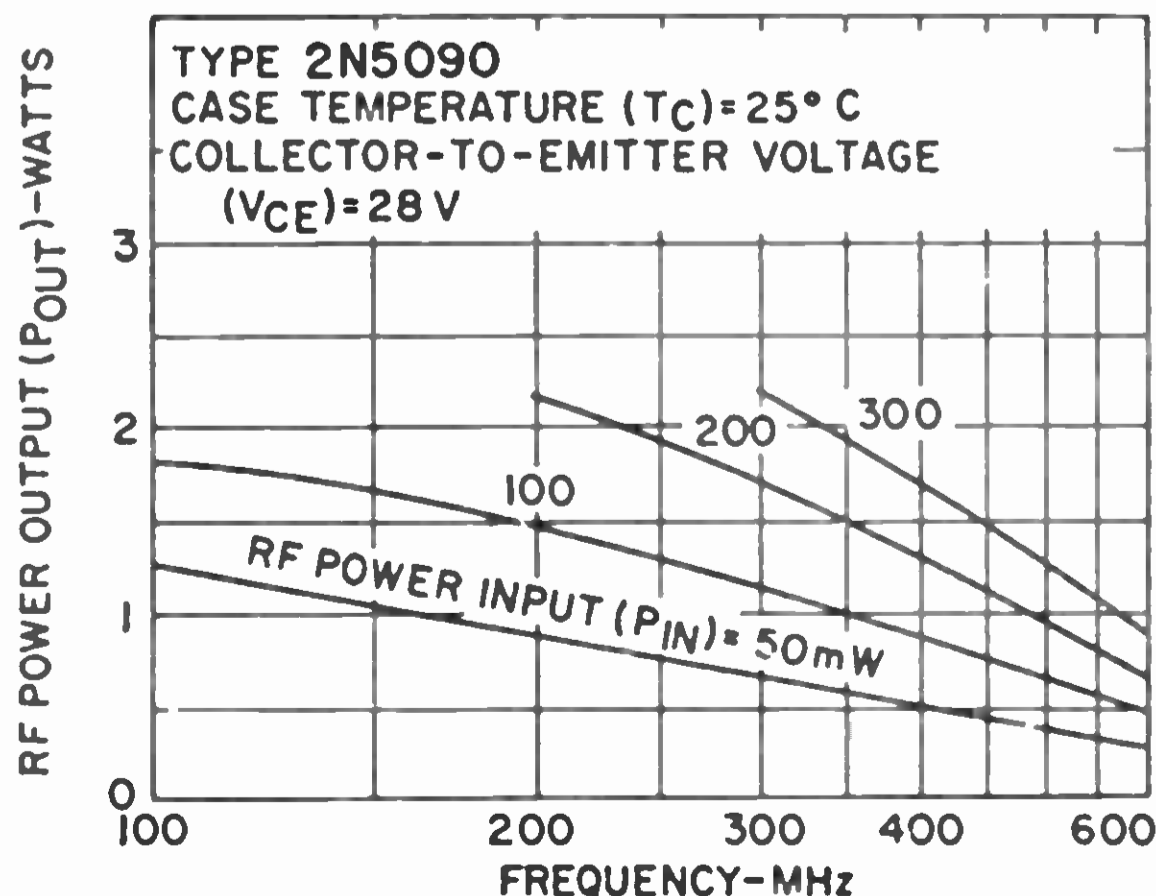
MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	55	V
Collector-to-Emitter Voltage: $R_{BE} = 10\ \Omega$	V_{CER}	55	V
Base open	V_{CEO}	30	V
Emitter-to-Base Voltage	V_{EBO}	3.5	V
Collector Current	I_C	0.4	A
Transistor Dissipation:			
T_C up to 75°C	P_T	5	W
T_C above 75°C	P_T	Derate linearly at $0.04\text{ W}/^{\circ}\text{C}$	
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 200	$^{\circ}\text{C}$
Storage	T_{STG}	-65 to 200	$^{\circ}\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	230	$^{\circ}\text{C}$

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Base Breakdown Voltage ($I_C = 0.1\text{ mA}$, $I_E = 0$)	$V_{(BR)CBO}$	55 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.1\text{ mA}$, $I_C = 0$)	$V_{(BR)EBO}$	3.5 min	V
Collector-to-Emitter Sustaining Voltage:			
$I_C = 5\text{ mA}$, $R_{BE} = 10\ \Omega$, pulsed through inductor $L = 25\text{ mH}$, $df = 50\%$	V_{CEI}	55 min	V
$I_C = 5\text{ mA}$, $I_B = 0$	$V_{CEO(\text{sus})}$	30 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 100\text{ mA}$, $I_B = 20\text{ mA}$)	$V_{CE(\text{sat})}$	1 max	V
Collector-Cutoff Current ($V_{CE} = 28\text{ V}$, $I_B = 0$)	I_{CEO}	20 max	μA
Gain-Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 50\text{ mA}$) ..	ft	500 min	MHz
Collector-to-Base Capacitance ($V_{CB} = 30\text{ V}$, $I_E = 0$, $f = 1\text{ MHz}$)	C_{obo}	3.5 max	pF

TYPICAL RF POWER-OUTPUT CHARACTERISTICS



9255-3618T

CHARACTERISTICS (cont'd)

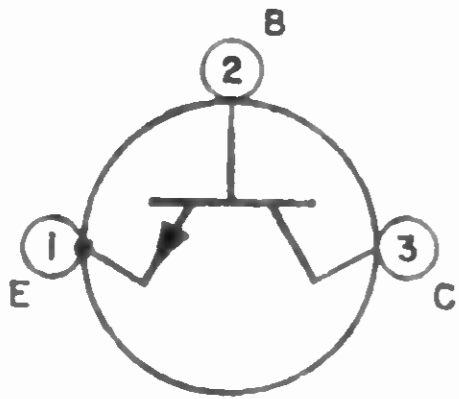
RF Power Output, Amplifier, Unneutralized
 ($V_{CE} = 28 \text{ V}$, $P_{IE} = 0.2 \text{ W}$, $f = 400 \text{ MHz}$,
 R_G and $R_L = 50 \Omega$)

P_{OE} 1.2* min W

* For conditions given, minimum efficiency = 45 per cent.

21.75

TRANSISTOR 2N5102



Si n-p-n "overlay" epitaxial planar type designed to provide high power as a class C rf amplifier for vhf aircraft communications service (108 to 150 MHz) with amplitude modulation and 24-volt power supply. JEDEC TO-60, Outline No.23. See Mounting Hardware for desired mounting arrangement.

MAXIMUM RATINGS

Collector-to-Emitter Voltage:

$V_{BE} = -1.5 \text{ V}$	V_{CEV}	100	V
$R_{BE} = 5 \Omega$	V_{CER}	50	V
Emitter-to-Base Voltage	V_{EBO}	4	V
Collector Current:			
Peak	i_C	10	A
Continuous	I_C	3.3	A
Transistor Dissipation:			
T_C up to 25°C	P_T	70	W
T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 200	$^\circ\text{C}$
Storage	T_{STG}	-65 to 200	$^\circ\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	230	$^\circ\text{C}$

CHARACTERISTICS (At case temperature = 25°C)

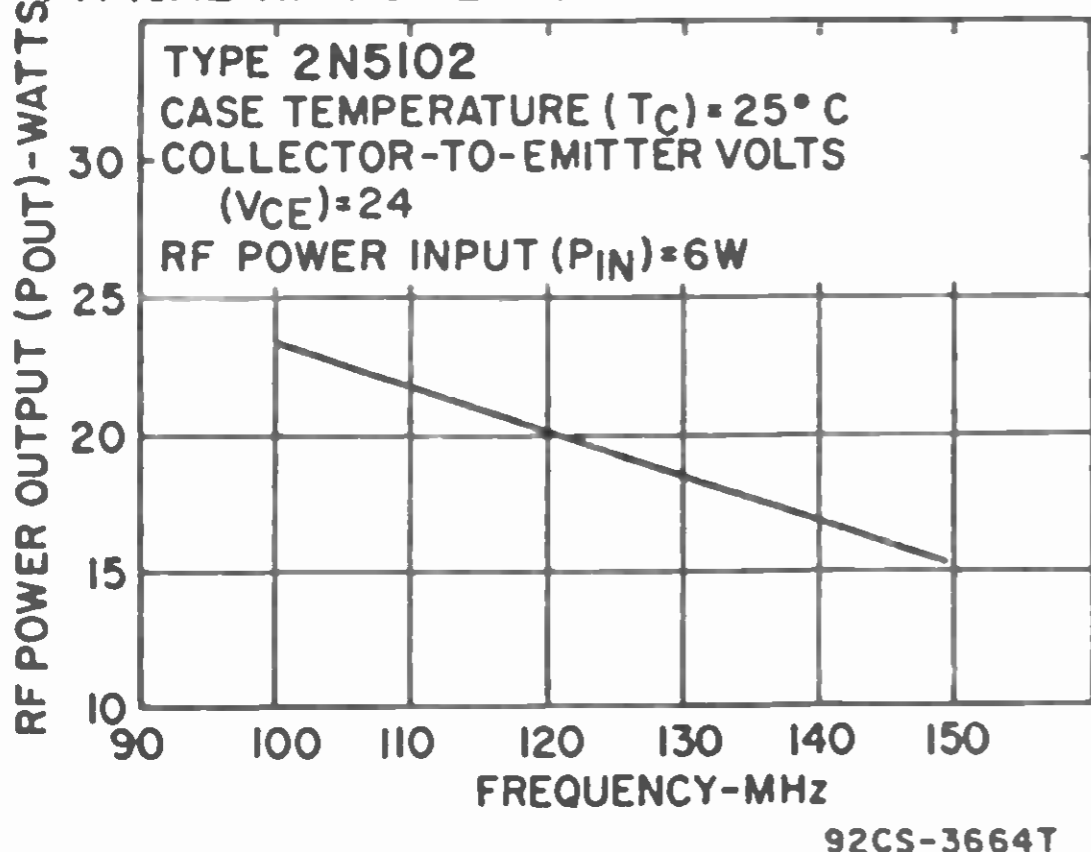
Emitter-to-Base Breakdown Voltage ($I_E = 10 \text{ V}$, $I_C = 0$)	$V_{(BR)EBO}$	4 min	V
Collector-to-Emitter Sustaining Voltage: $V_{BE} = -1.5 \text{ V}$, $I_C = 600 \text{ mA}$, pulsed through an inductor $L = 9 \text{ mH}$, $df = 50\%$	$V_{CEV(\text{SUS})}$	100 min	V
$R_{BE} = 5 \Omega$, $I_C = 200 \text{ mA}$, pulsed through an inductor $L = 9 \text{ mH}$, $df = 50\%$	$V_{CER(\text{SUS})}$	50 min	V
Collector-Cutoff Current ($V_{CE} = 50 \text{ V}$, $R_{BE} = 5 \Omega$) ...	I_{CER}	10 max	mA
Collector-to-Base Capacitance ($V_{CB} = 30 \text{ V}$, $I_C = 0$) ...	C_{cb}	85 max	pF
RF Power Output ($V_{CC} = 24 \text{ V}$, $P_{IE} = 6 \text{ W}$, R_G and $R_L = 50 \Omega$, $f = 136 \text{ MHz}$)	P_{OE}	15* min	W
Modulation [●] ($V_{CE} = 24 \text{ V}$, $f = 118 \text{ MHz}$)		80 min	%
Load Mismatch [■] ($V_{CE} = 24 \text{ V}$, $f = 118 \text{ MHz}$)		will not be damaged	
Dynamic Input Impedance ($V_{CE} = 24 \text{ V}$, $I_C = 1100 \text{ mA}$, $P_{OE} = 6 \text{ W}$, $f = 150 \text{ MHz}$)		1.7 + j2.6	Ω

* Unmodulated carrier.

● Carrier Power, $P_{CAR} = 15 \text{ W}$; V_{CC} modulation = 100%; $M = \frac{\sqrt{2(P_{AM} - P_{CAR})}}{P_{CAR}} \times 100\%$.

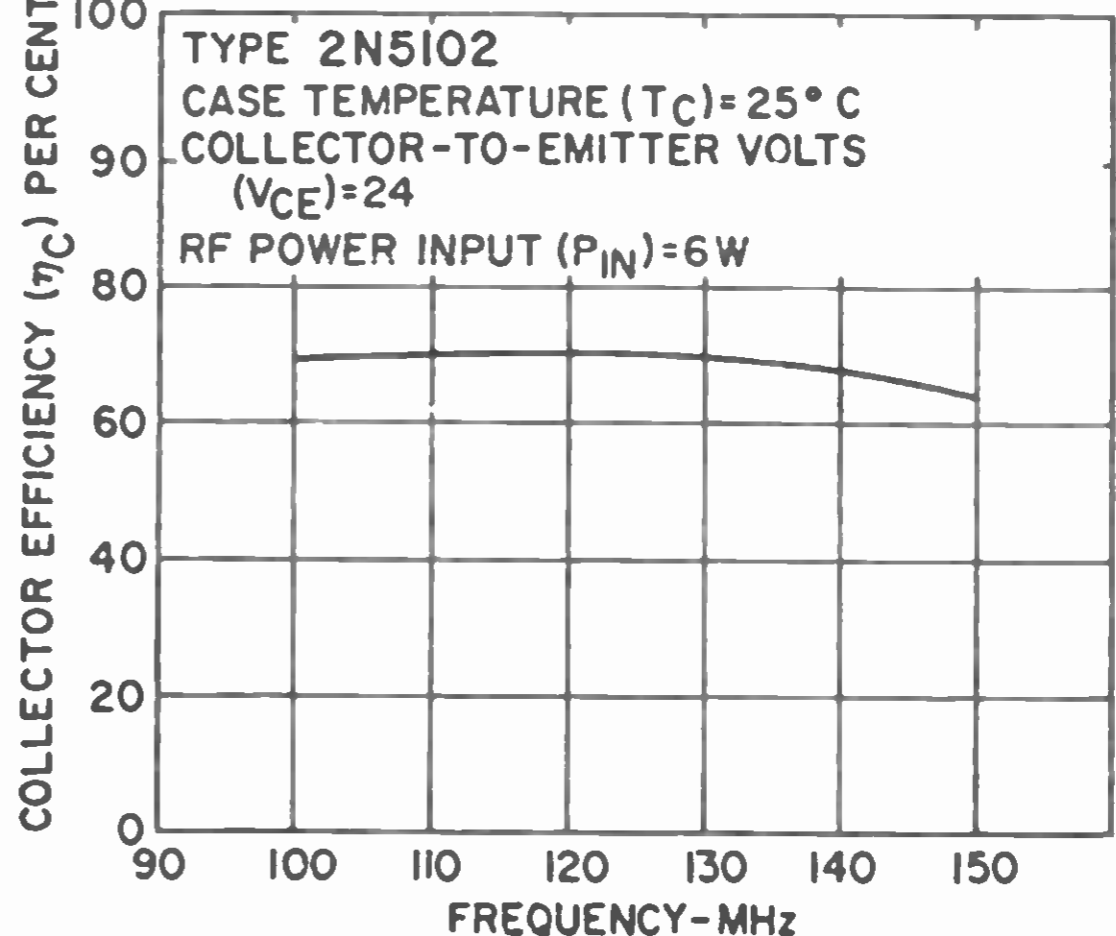
■ Under conditions of footnote (●), the transistor is subjected to all conditions of load mismatch from short circuit to open circuit.

TYPICAL RF POWER-OUTPUT CHARACTERISTIC



92CS-3664T

TYPICAL COLLECTOR CHARACTERISTIC



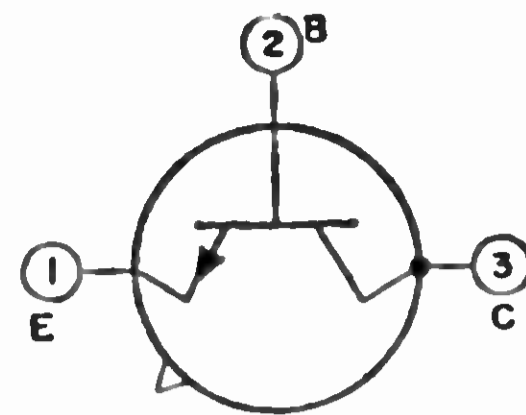
92SS-3666T

10.70

2N5108

TRANSISTOR

Si n-p-n "overlay" epitaxial planar type used as a high-power amplifiers, fundamental-frequency oscillator, and frequency multiplier. It may be used in final, driver, and pre-driver amplifier stages in uhf equipment and as a fundamental-frequency oscillator at 1.68 GHz. JEDEC TO-39, Outline No.15.



MAXIMUM RATINGS

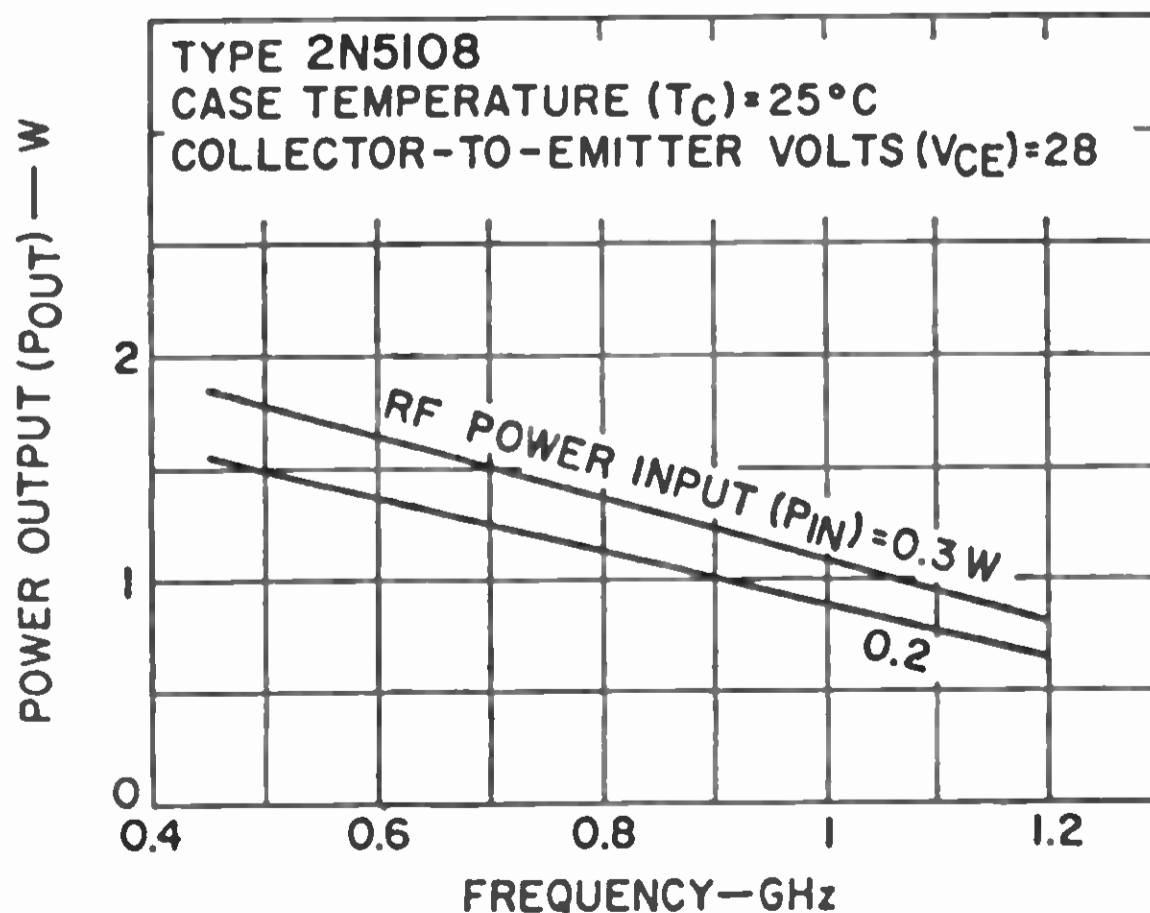
Collector-to-Base Voltage	V_{CBO}	55	V
Collector-to-Emitter Voltage:			
$R_{BE} = 10 \Omega$	V_{CER}	55	V
Base open	V_{CEO}	30	V
Emitter-to-Base Voltage	V_{EBO}	3	V
Collector Current	I_C	0.4	A
Transistor Dissipation:			
T_C up to 25°C	P_T	3.5	W
T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	230	°C

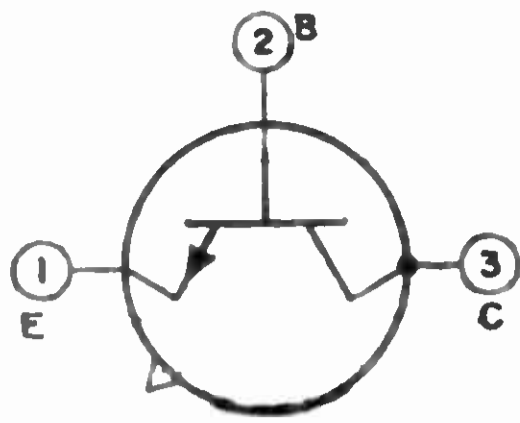
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Base Breakdown Voltage ($I_C = 0.1 \text{ mA}, I_E = 0$)	$V_{(BR)CBO}$	55 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.1 \text{ mA}, I_C = 0$)	$V_{(BR)EBO}$	3 min	V
Collector-to-Emitter Sustaining Voltage ($R_{BE} = 10 \Omega, I_C = 5 \text{ mA}$, pulsed through an inductor $L = 2.5 \text{ mH}$, $df = 50\%$)	$V_{CER(SUS)}$	55 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 100 \text{ mA}, I_B = 10 \text{ mA}$)	$V_{CE(sat)}$	0.5 max	V
Collector-Cutoff Current:			
$V_{CE} = 15 \text{ V}, I_B = 0$	I_{CEO}	20 max	μA
$V_{CE} = 50 \text{ V}$	I_{CES}	1 max	μA
Collector-to-Base Capacitance ($V_{CB} = 30 \text{ V}, I_E = 0$, $f = 1 \text{ MHz}$)	C_{obo}	3 max	pF
Magnitude of Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 15 \text{ V}, I_C = 50 \text{ mA}, f = 200 \text{ MHz}$)	$ h_{fe} $	6 min	
RF Power Output, Common Emitter Amplifier ($V_{CE} = 28 \text{ V}, P_{IE} = 0.316 \text{ W}, f = 1 \text{ GHz}$)	P_{OE}	1* min	W
RF Power Output, Fundamental Frequency Oscillator ($V_{CE} = 20 \text{ V}, V_{EB} = 1.5 \text{ V}, f = 1.68 \text{ GHz}$)	P_{OE}	0.3†	W

* For conditions given, minimum efficiency = 35 per cent.
† For conditions given, minimum efficiency = 15 per cent.

TYPICAL RF POWER-OUTPUT CHARACTERISTICS





TRANSISTOR

2N5109

Si n-p-n "overlay" epitaxial planar type designed to provide large dynamic range, low distortion, and low noise as a wide-band amplifier into the vhf range. JEDEC TO-39, Outline No.15.

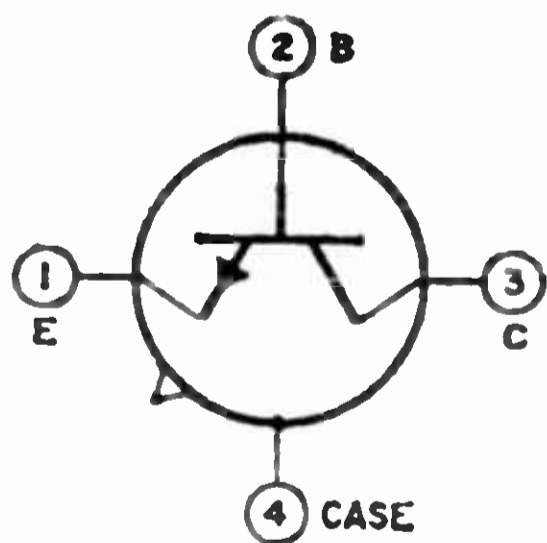
MAXIMUM RATINGS

Collector-to-Base Voltage	V _{CB0}	40	V
Collector-to-Emitter Voltage (R _{BE} = 10 Ω)	V _{CER}	40	V
Emitter-to-Base Voltage	V _{EBO}	3	V
Collector Current	I _C	0.4	A
Transistor Dissipation:			
T _C up to 25°C	P _T	3.5	W
T _C above 25°C	P _T	See curve page 300	
Temperature Range:			
Operating (Junction)	T _J (opr)	-65 to 200	°C
Storage	T _{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T _L	230	°C

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Base Breakdown Voltage (I _C = 0.1 mA, I _E = 0)	V _{(BR)CBO}	40 min	V
Emitter-to-Base Breakdown Voltage (I _E = 0.1 mA, I _C = 0)	V _{(BR)EBO}	3 min	V
Collector-to-Emitter Sustaining Voltage: R _{BE} = 10 Ω, I _C = 5 mA, pulsed through an inductor L = 2.5 mH, df = 50%	V _{CER} (SUS)	40 min	V
I _C = 5 mA, I _B = 0	V _{CEO} (SUS)	20 min	V
Collector-to-Emitter Saturation Voltage (I _C = 100 mA, I _B = 10 mA)	V _{CE} (sat)	0.5 max	V
Collector-Cutoff Current (I _C = 0.1 mA, I _E = 0)	I _{CEO}	20 max	μA
Collector-to-Base Capacitance (V _{CB} = 15 V, I _E = 0, f = 1 MHz)	C _{obo}	3.5 max	pF
Static Forward-Current Transfer Ratio (V _{CB} = 15 V, I _C = 50 mA)	h _{FE}	70 min; 210 typ	
Small-Signal Forward-Current Transfer Ratio:			
V _{CB} = 15 V, I _C = 25 mA	h _{fe}	4.8 min	
V _{CB} = 15 V, I _C = 50 mA	h _{fe}	6 min	
V _{CB} = 15 V, I _C = 100 mA	h _{fe}	4.8 min	
Voltage Gain, Wideband (V _{CB} = 15 V, I _C = 50 mA, f = 50 to 216 MHz)		11 min	dB
Cross Modulation at 54 dBmV• Output (V _{CB} = 15 V, I _C = 50 mA)		-57	dB
Power Gain, Narrowband (V _{CB} = 15 V, I _C = 10 mA, P _{IE} = -10 dB, f = 200 MHz)		11 min	dB
Noise Figure (V _{CB} = 15 V, I _C = 10 mA, f = 200 MHz)	NF	3	dB

● 0 dBmV = 1 millivolt.



TRANSISTOR

2N5179

Si n-p-n double-diffused epitaxial planar type used in low-noise tuned-amplifier and converter applications at vhf frequencies, and as an oscillator up to 500 MHz. JEDEC TO-72, Outline No.28.

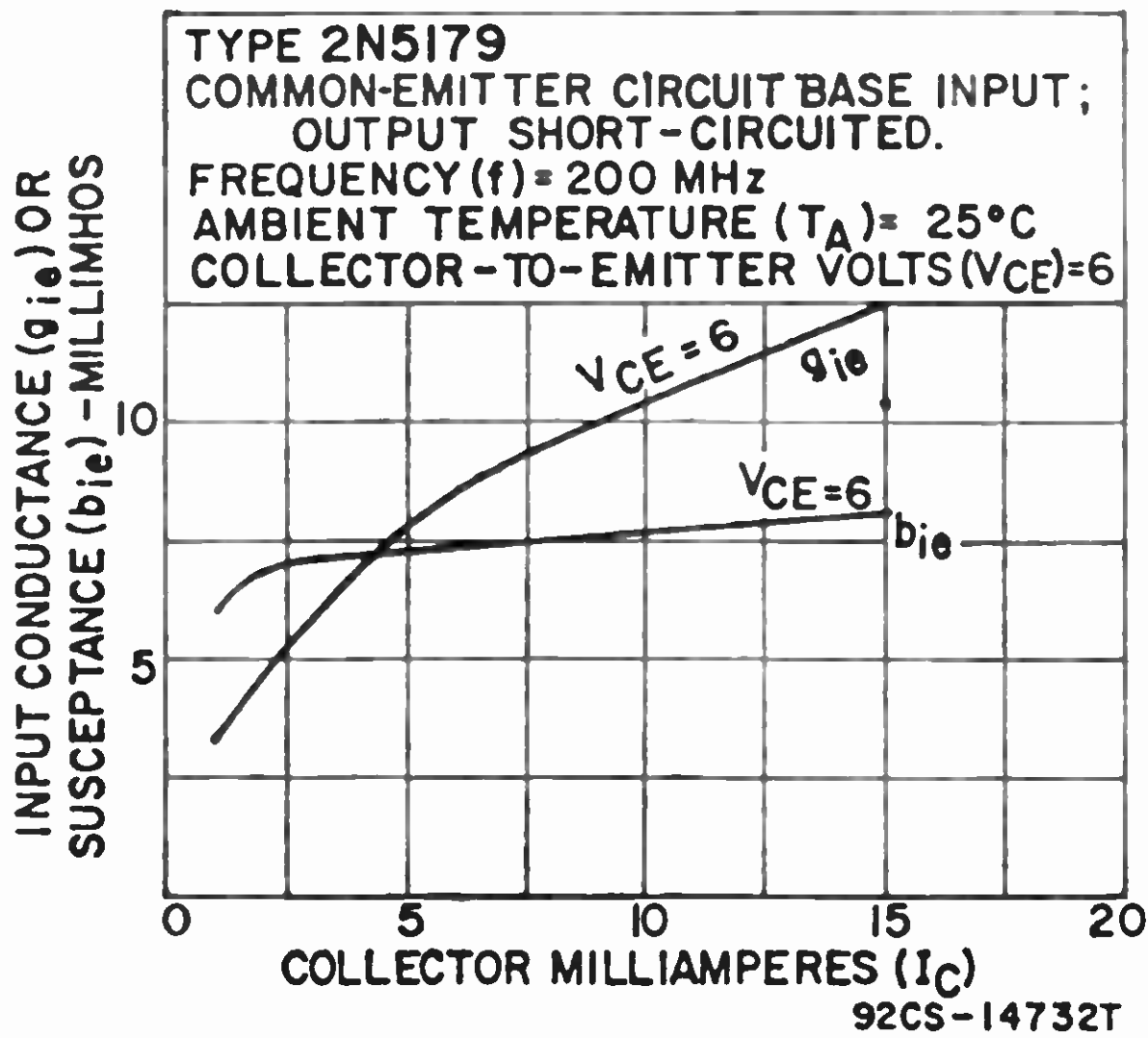
MAXIMUM RATINGS

Collector-to-Base Voltage	V _{CB0}	20	V
Collector-to-Emitter Voltage	V _{CEO}	12	V
Emitter-to-Base Voltage	V _{EBO}	2.5	V
Collector Current	I _C	50	mA
Transistor Dissipation:			
T _C up to 25°C	P _T	300	mW
T _C above 25°C	P _T	Derate at 2	mW/°C
T _A up to 25°C	P _T	200	mW
T _A above 25°C	P _T	Derate at 1.33	mW/°C
Temperature Range:			
Operating (Junction)	T _J (opr)	-65 to 175	°C
Storage	T _{STG}	-65 to 175	°C
Lead-Soldering Temperature (10 s max)	T _L	265	°C

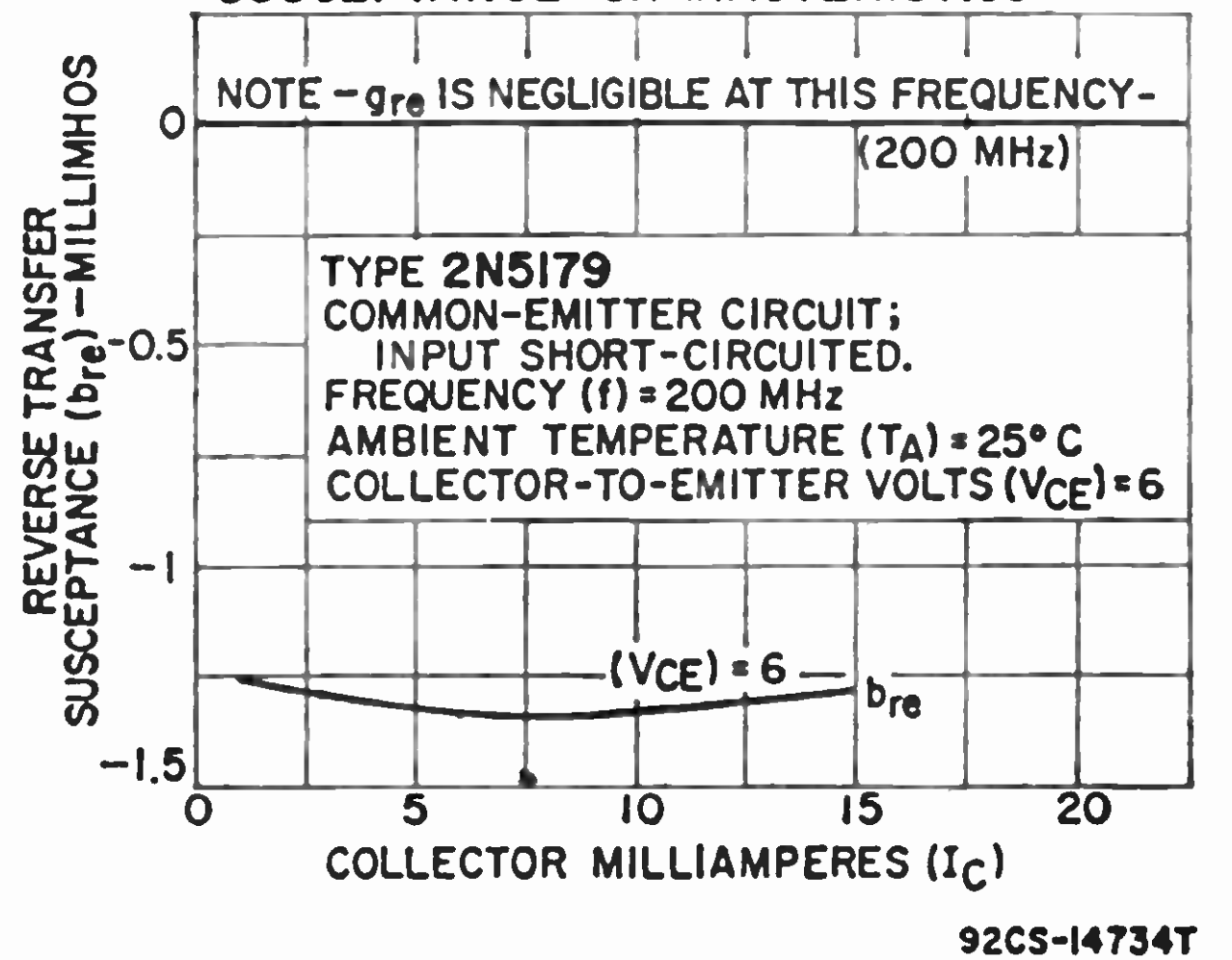
CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = 0.001$ mA, $I_E = 0$)	$V_{(BR)CBO}$	20 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -0.01$ mA, $I_C = 0$)	$V_{(BR)EBO}$	2.5 min	V
Collector-to-Emitter Sustaining Voltage ($I_C = 3$ mA, $I_B = 0$)	$V_{CEO(sus)}$	12 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 10$ mA, $I_B = 1$ mA)	$V_{CE(sat)}$	0.4 max	V
Base-to-Emitter Saturation Voltage ($I_C = 10$ mA, $I_B = 1$ mA)	$V_{BE(sat)}$	1 max	V
Collector-Cutoff Current: $I_C = 15$ mA, $I_E = 0$	I_{CBO}	0.02 max	μ A
$I_C = 15$ mA, $I_E = 0$, $T_A = 150^\circ$ C	I_{CBO}	1 max	μ A
Static Forward-Current Transfer Ratio ($V_{CE} = 1$ V, $I_C = 3$ mA)	h_{FE}	25 to 250	
Magnitude of Small-Signal Forward Current-Transfer Ratio*: $V_{CE} = 6$ V, $I_C = 5$ mA, $f = 100$ MHz	$ h_{fe} $	9 to 20	
$V_{CE} = 6$ V, $I_C = 2$ mA, $f = 1$ kHz	$ h_{fe} $	25 to 300	
Collector-to-Base Feedback Capacitance ^c ($V_{CB} = 10$ V, $I_E = 0$, $f = 0.1$ to 1 MHz)	C_{cb}	0.7 typ; 1 max	pF
Common-Base Input Capacitance ^a ($V_{EB} = 0.5$ V, $I_C = 0$, $f = 0.1$ to 1 MHz)	C_{ibo}	2 max	pF

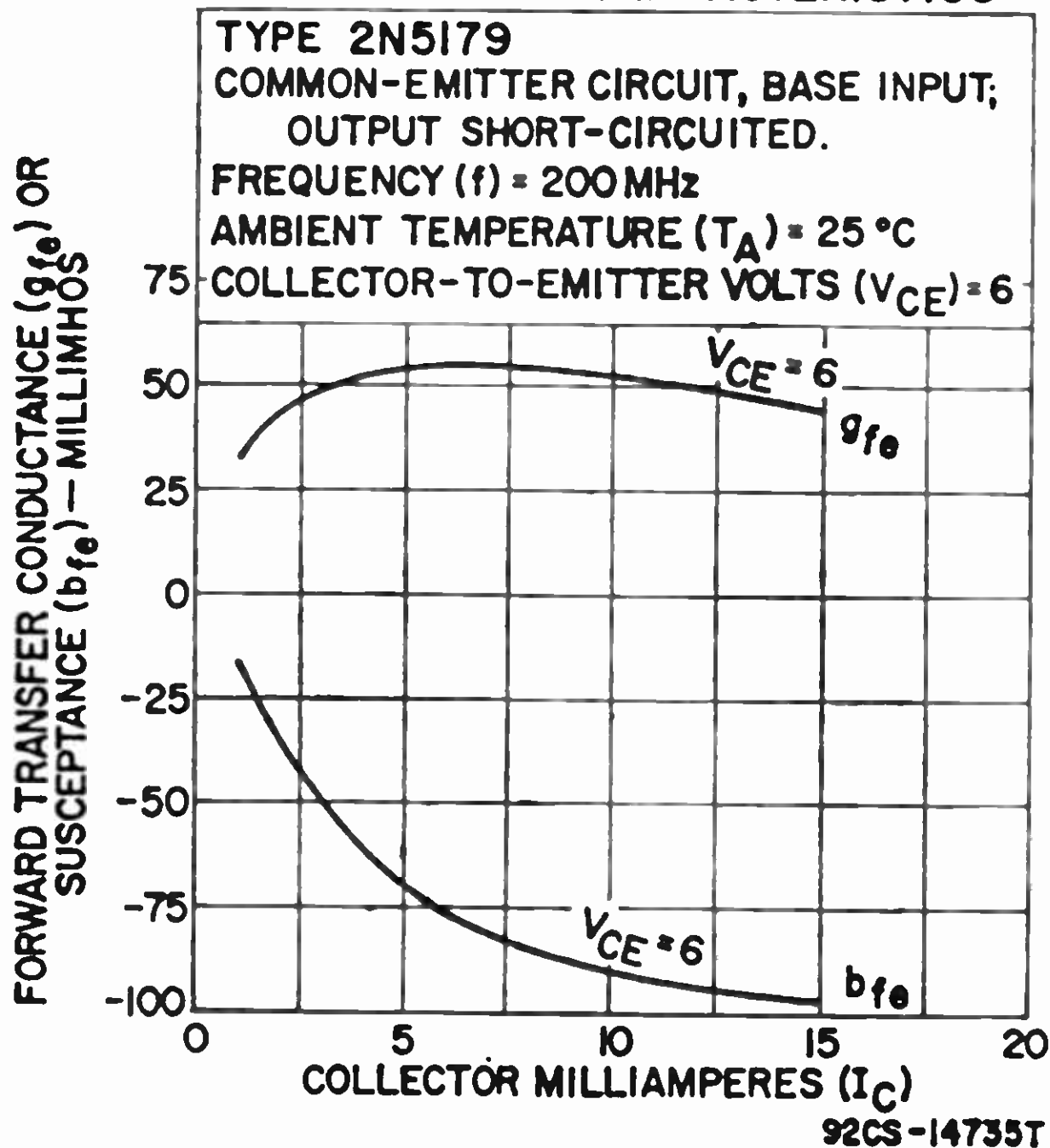
TYPICAL INPUT CONDUCTANCE AND SUSCEPTANCE CHARACTERISTICS



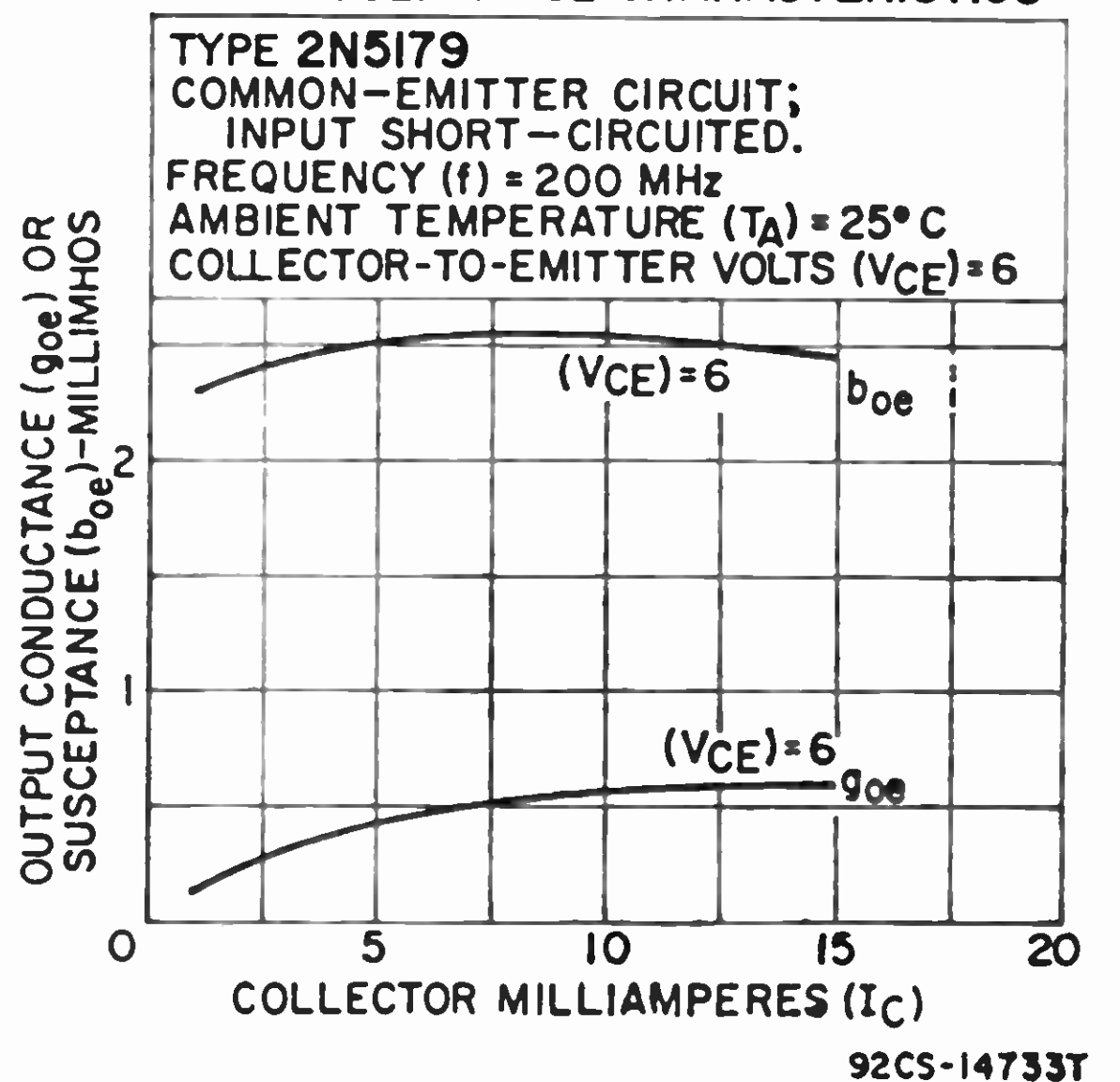
TYPICAL REVERSE TRANSFER SUSCEPTANCE CHARACTERISTICS



TYPICAL FORWARD TRANSFER CONDUCTANCE AND SUSCEPTANCE CHARACTERISTICS



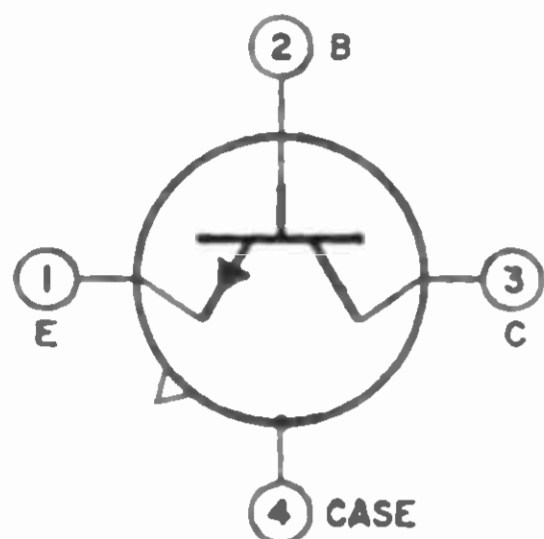
TYPICAL OUTPUT CONDUCTANCE AND SUSCEPTANCE CHARACTERISTICS



CHARACTERISTICS (cont'd)

Collector-to-Base Time Constant* ($V_{CB} = 6\text{ V}$, $I_C = 2\text{ mA}$, $f = 31.9\text{ MHz}$)	$r_b' C_c$	3 to 14	ps
Small-Signal Power Gain, Neutralized Amplifier* ($V_{CE} = 12\text{ V}$, $I_C = 5\text{ mA}$, $R_G = 125\ \Omega$, $f = 200\text{ MHz}$)	G_{pe}	15 min; 21 typ	dB
Power Output, Oscillator Circuit* ($V_{CB} = 10\text{ V}$, $I_E = -12\text{ mA}$, $f > 500\text{ MHz}$)	P_o	20 min	mW
Noise Figure* ($V_{CE} = 6\text{ V}$, $I_C = 1.5\text{ mA}$, $f = 200\text{ MHz}$)	NF	3 typ; 4.5 max	dB

- * Lead No. 4 (case) grounded.
- ‡ Three-terminal measurement of the collector-to-base capacitance: Lead No. 1 (emitter) and lead No. 4 (case) connected to guard terminal.
- Lead No. 4 (case) floating.



TRANSISTOR

2N5180

Si n-p-n epitaxial planar type used as a general-purpose amplifier at vhf frequencies. JEDEC TO-72, Outline No.28.

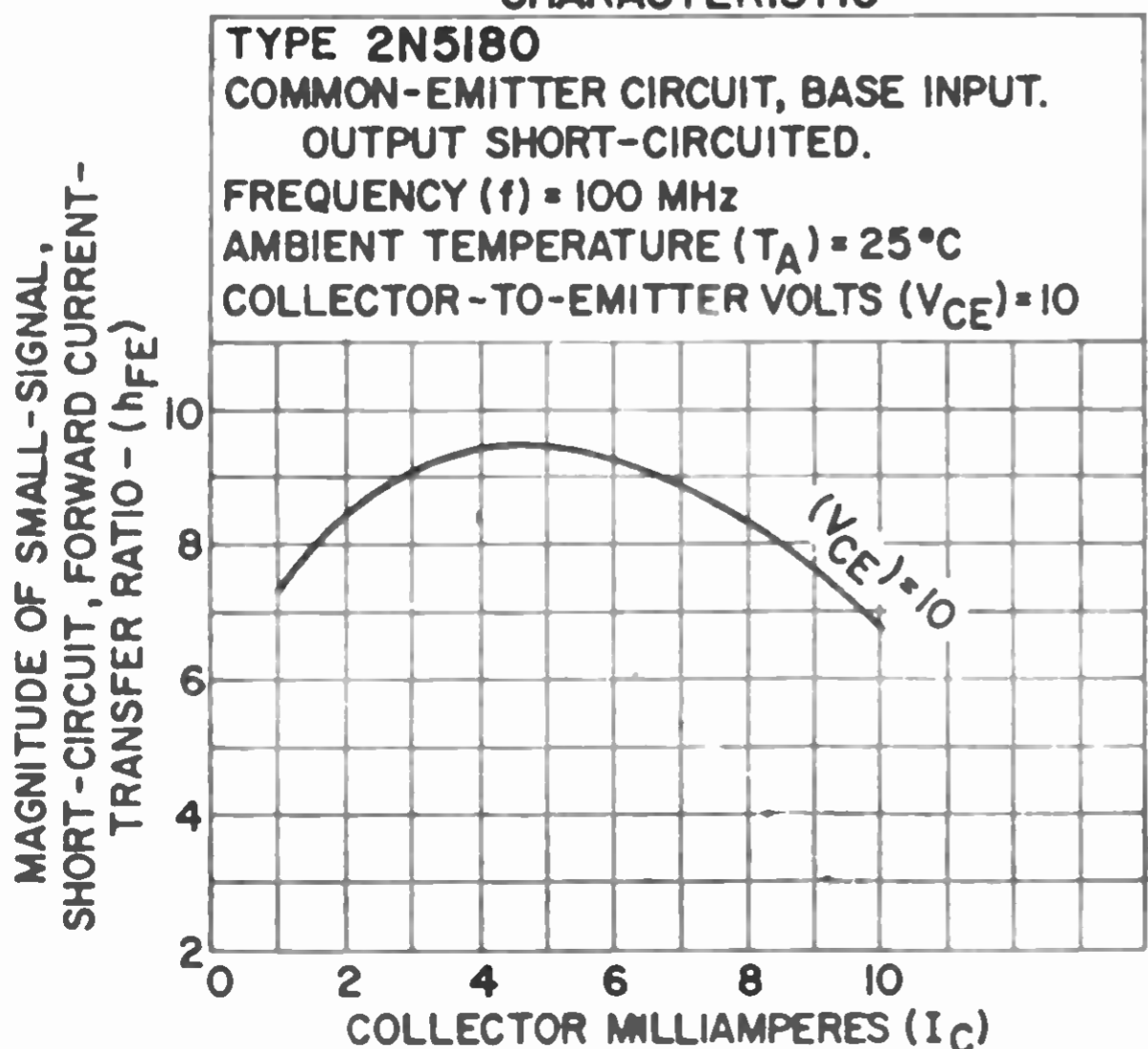
MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	30	V
Collector-to-Emitter Voltage	V_{CEO}	15	V
Emitter-to-Base Voltage	V_{EBO}	2	V
Collector Current	I_C	Limited by dissipation	
Transistor Dissipation:			
T_A up to 25°C	P_T	180	mW
T_A above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 175	$^\circ\text{C}$
Storage	T_{STG}	-65 to 175	$^\circ\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	265	$^\circ\text{C}$

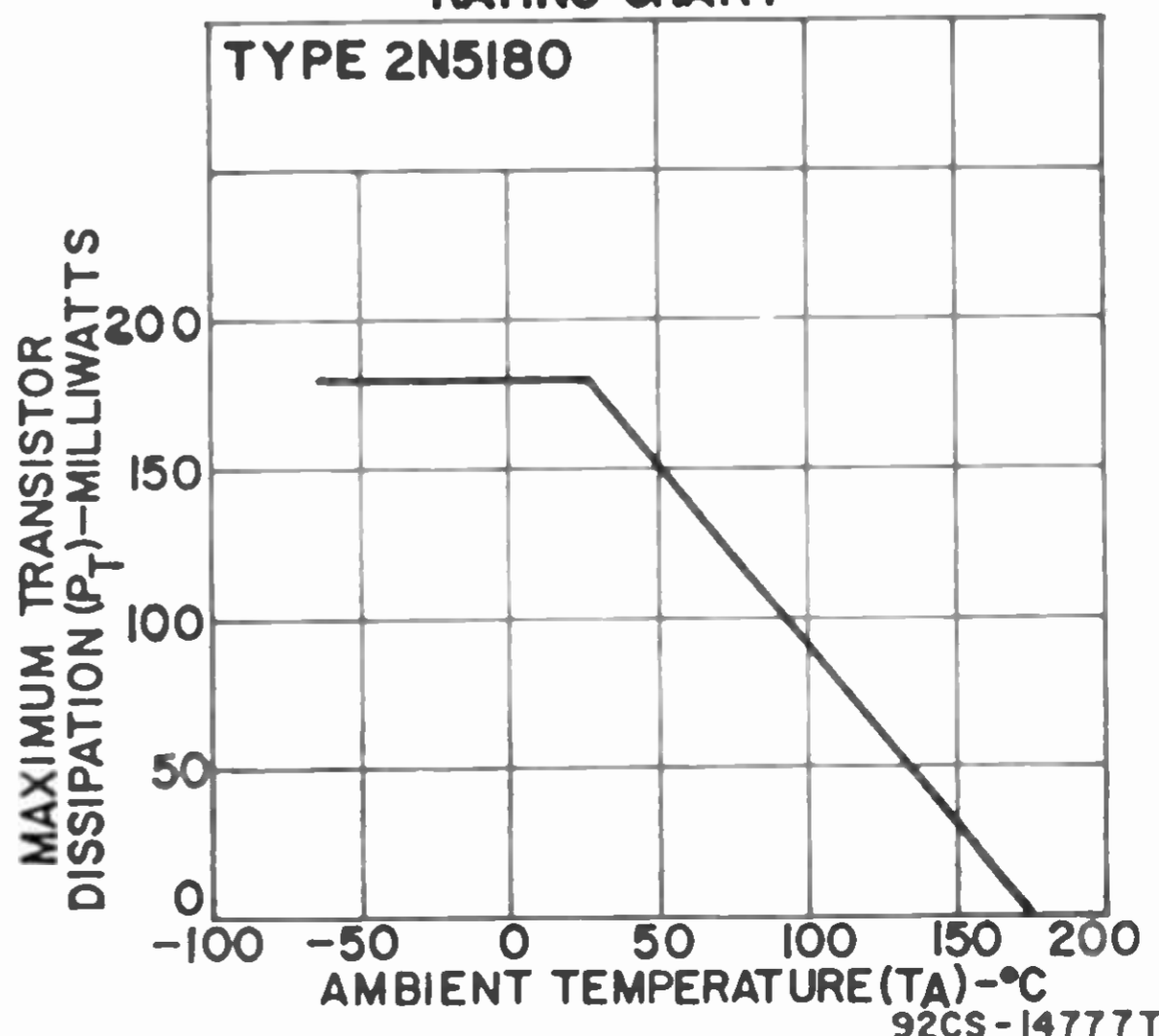
CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = 0.001\text{ mA}$, $I_E = 0$)	$V_{(BR)CBO}$	30 min	V
Collector-to-Emitter Breakdown Voltage ($I_C = 0.001\text{ mA}$)	$V_{(BR)CEO}$	15 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -0.001\text{ mA}$, $I_C = 0$)	$V_{(BR)EBO}$	2 min	V
Collector-Cutoff Current ($V_{CB} = 1\text{ V}$, $I_E = 0$)	I_{CBO}	0.025 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 8\text{ V}$, $I_C = 2\text{ mA}$)	h_{FE}	20 to 200	

TYPICAL SMALL-SIGNAL, SHORT-CIRCUIT FORWARD-CURRENT TRANSFER-RATIO CHARACTERISTIC



RATING CHART



92CS-14785 T

92CS-14777 T

CHARACTERISTICS (cont'd)

Magnitude of Small-Signal Forward-Current Transfer Ratio*

($V_{CE} = 8 \text{ V}$, $I_C = 2 \text{ mA}$, $f = 100 \text{ MHz}$)	$ h_{fe} $	6.5 to 16	
Collector-to-Base Feedback Capacitance† ($V_{CB} = 8 \text{ V}$, $I_E = 0$, $f = 0.1 \text{ to } 1 \text{ MHz}$)	C_{cb}	1 max	pF
Maximum Usable Amplifier Gain, Neutralized* ($V_{CE} = 8 \text{ V}$, $I_C = 2 \text{ mA}$, $f = 200 \text{ MHz}$)	MUG	12 to 19	dB
Noise Figure*: $V_{CE} = 8 \text{ V}$, $I_C = 2 \text{ mA}$, $f = 200 \text{ MHz}$	NF	4.5 max	dB
$V_{CE} = 8 \text{ V}$, $I_C = 1 \text{ mA}$, $R_s = 400 \Omega$, $f = 60 \text{ MHz}$	NF	2.5	dB

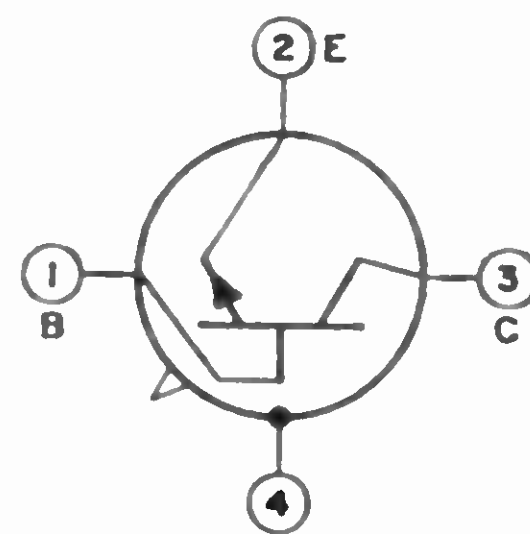
* Fourth lead (case) grounded.

† Three-terminal measurement of the collector-to-base capacitance: Lead No. 1 (emitter and lead No. 4 (case) connected to guard terminal.

2N5181

VHF TRANSISTOR

Si n-p-n type used in rf and if amplifier circuits at frequencies up to 250 MHz. The terminal arrangement permits shielding between input and output terminals for superior high-frequency performance and greater circuit stability, particularly on printed-circuit boards. JEDEC TO-104, Outline No.31.



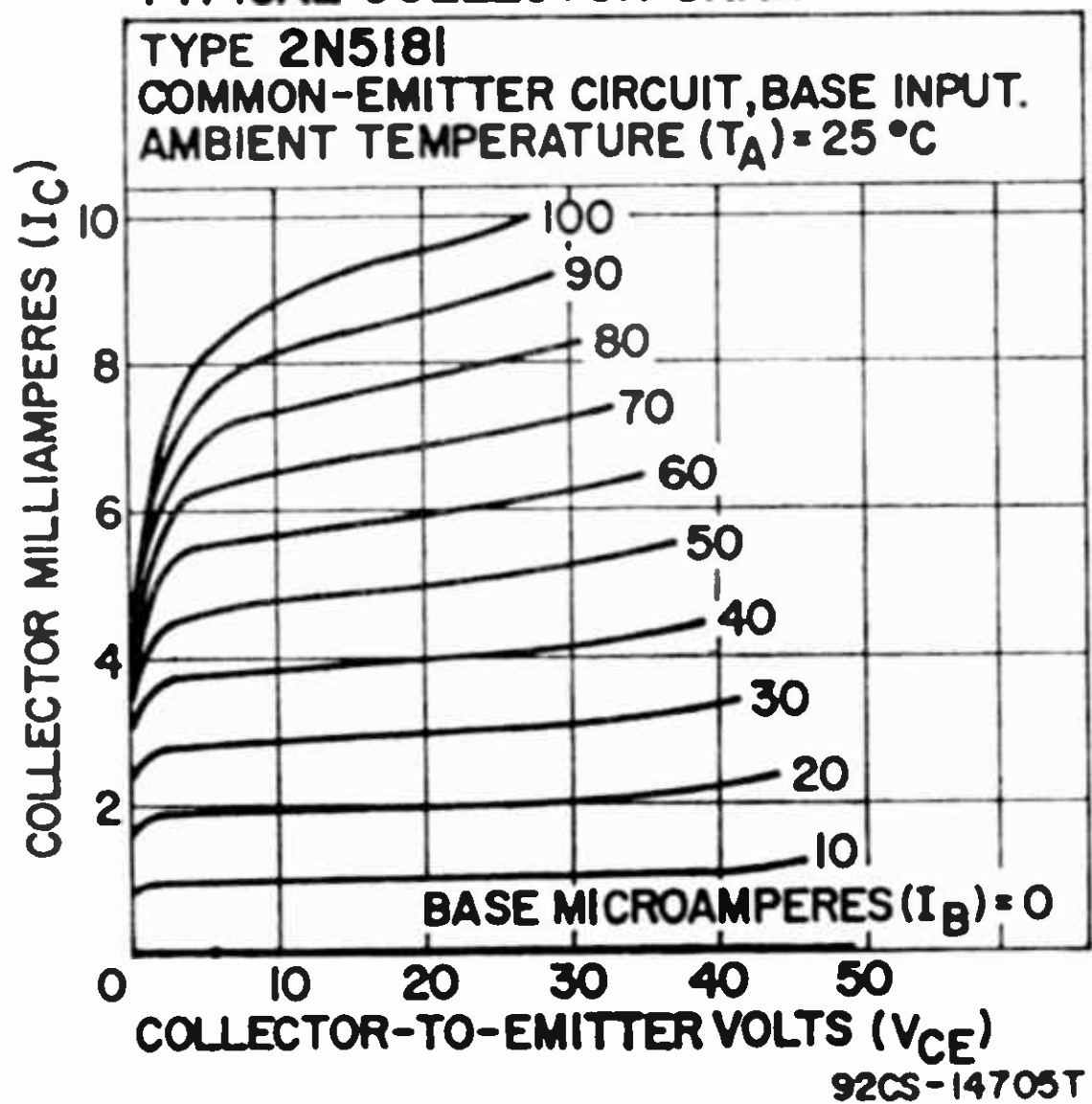
MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	45	V
Emitter-to-Base Voltage	V_{EBO}	3	V
Collector Current	I_C	50	mA
Transistor Dissipation: T_A up to 25°C	P_T	180	mW
T_A above 25°C	P_T	Derate at 1.2	mW/ $^\circ\text{C}$
Temperature Range: Operating (Junction)	$T_J(\text{opr})$	-65 to 175	$^\circ\text{C}$
Storage	T_{STG}	-65 to 175	$^\circ\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	255	$^\circ\text{C}$

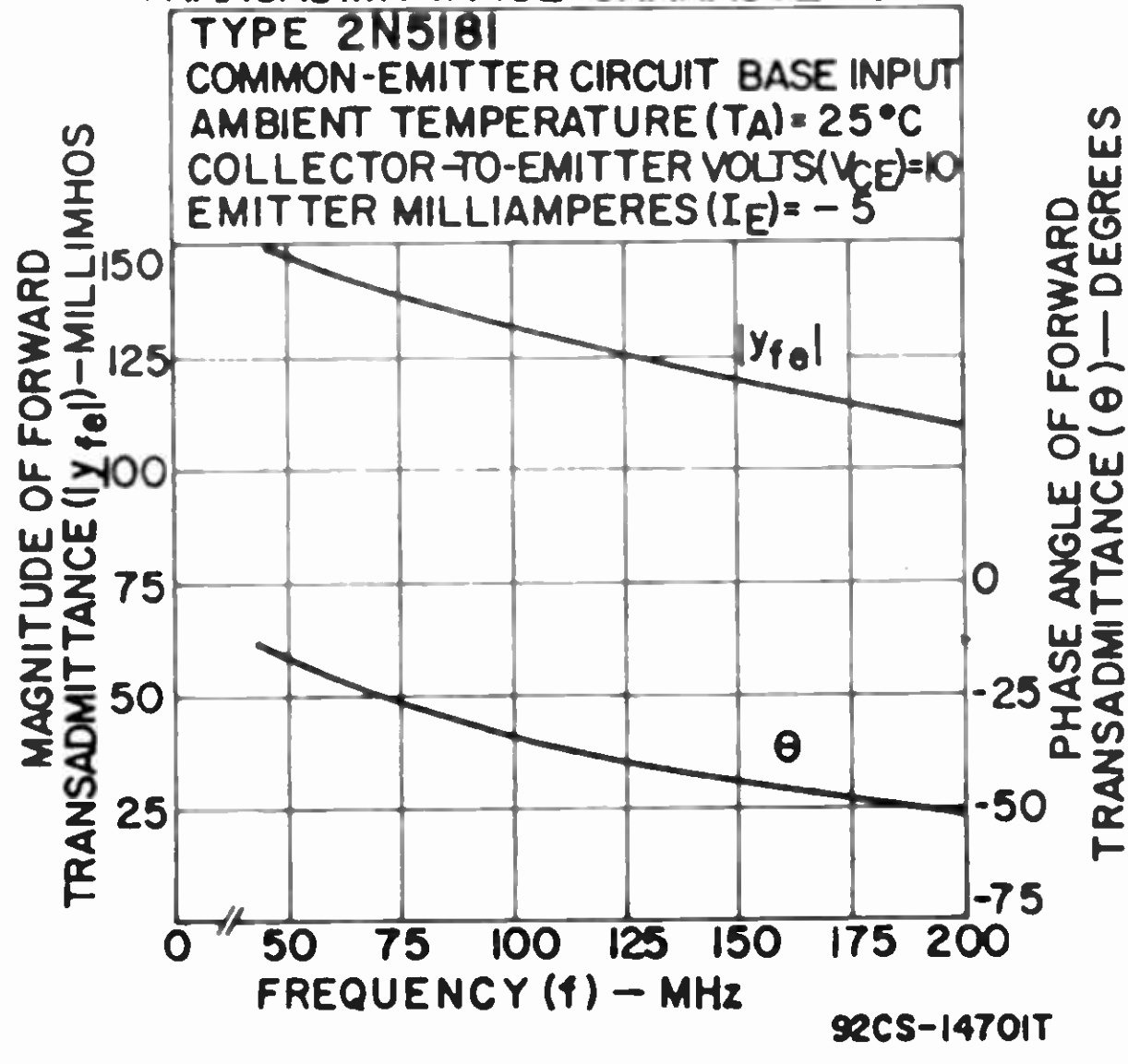
CHARACTERISTICS

Collector-Cutoff Current: $V_{CB} = 1 \text{ V}$, $I_E = 0$	I_{CBO}	0.02 max	μA
$V_{CB} = 45 \text{ V}$, $I_E = 0$	I_{CBO}	1 max	μA
Emitter-Cutoff Current ($V_{EB} = 3 \text{ V}$, $I_C = 0$)	I_{EBO}	1 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 6 \text{ V}$, $I_E = -1 \text{ mA}$)	h_{FE}	27 to 275	
Gain Bandwidth Product ($V_{CE} = 6 \text{ V}$, $I_E = -2 \text{ mA}$, $f = 100 \text{ MHz}$)	f_T	700	MHz
Collector-to-Base Feedback Capacitance ($V_{CE} = 10 \text{ V}$, $I_E = -3 \text{ mA}$, $f = 0.1 \text{ to } 1 \text{ MHz}$)	C_{cb}	0.22 typ; 0.34 max	pF

TYPICAL COLLECTOR CHARACTERISTICS

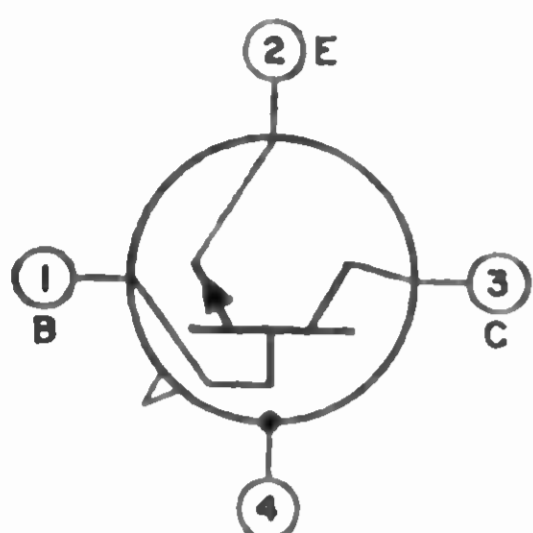


TYPICAL FORWARD TRANSADMITTANCE CHARACTERISTICS



CHARACTERISTICS (cont'd)

Maximum Available Amplifier Gain ($V_{CE} = 10\text{ V}$, $I_E = -2\text{ mA}$, $f = 200\text{ MHz}$)	MAG	29.9	dB
Maximum Usable Amplifier Gain, Unneutralized ($V_{CE} = 10\text{ V}$, $I_E = -2\text{ mA}$, $f = 200\text{ MHz}$)	MUG	20.4	dB
Maximum Usable Amplifier Gain, Neutralized ($V_{CE} = 10\text{ V}$, $I_E = -2\text{ mA}$, $f = 200\text{ MHz}$)	MUG	24.2	dB



VHF TRANSISTOR

2N5182

Si n-p-n type used in rf and if amplifier circuits at frequencies up to 250 MHz. The terminal arrangement permits shielding between input and output terminals for superior high-frequency performance and greater circuit stability, particularly on printed-circuit boards. JEDEC TO-104, Outline No.31. Type 2N5182 is identical to type 2N5181 except for the following items:

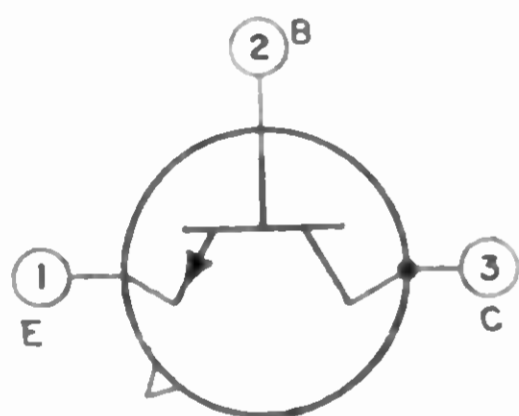
ical to type 2N5181 except for the following items:

MAXIMUM RATINGS

Collector Current	I_C	4	mA
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CHARACTERISTICS

Collector-Cutoff Current: $V_{CB} = 1\text{ V}$, $I_E = 0$	I_{CBO}	0.03 max	μA
$V_{CB} = 35\text{ V}$, $I_E = 0$	I_{CBO}	1	μA
Maximum Available Amplifier Gain ($V_{CE} = 10\text{ V}$, $I_E = -2\text{ mA}$, $f = 200\text{ MHz}$)	MAG	29.5	dB



TRANSISTOR

2N5183

Si n-p-n double-diffused epitaxial planar type used for general-purpose applications in amplifier and computer equipment. JEDEC TO-104, Outline No.32.

MAXIMUM RATINGS

Collector-to-Emitter Voltage	V_{CEO}	18	V
Collector-to-Base Voltage	V_{CBO}	18	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Collector Current	I_C	1	A
Transistor Dissipation:			
T_A up to 25°C	P_T	0.5	W
T_A above 25°C	P_T	Derate at 3.3	mW/ $^\circ\text{C}$
T_C up to 75°C	P_T	2	W
T_C above 75°C	P_T	Derate at 20	mW/ $^\circ\text{C}$
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 175	$^\circ\text{C}$
Storage	T_{STG}	-65 to 175	$^\circ\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	265	$^\circ\text{C}$

CHARACTERISTICS

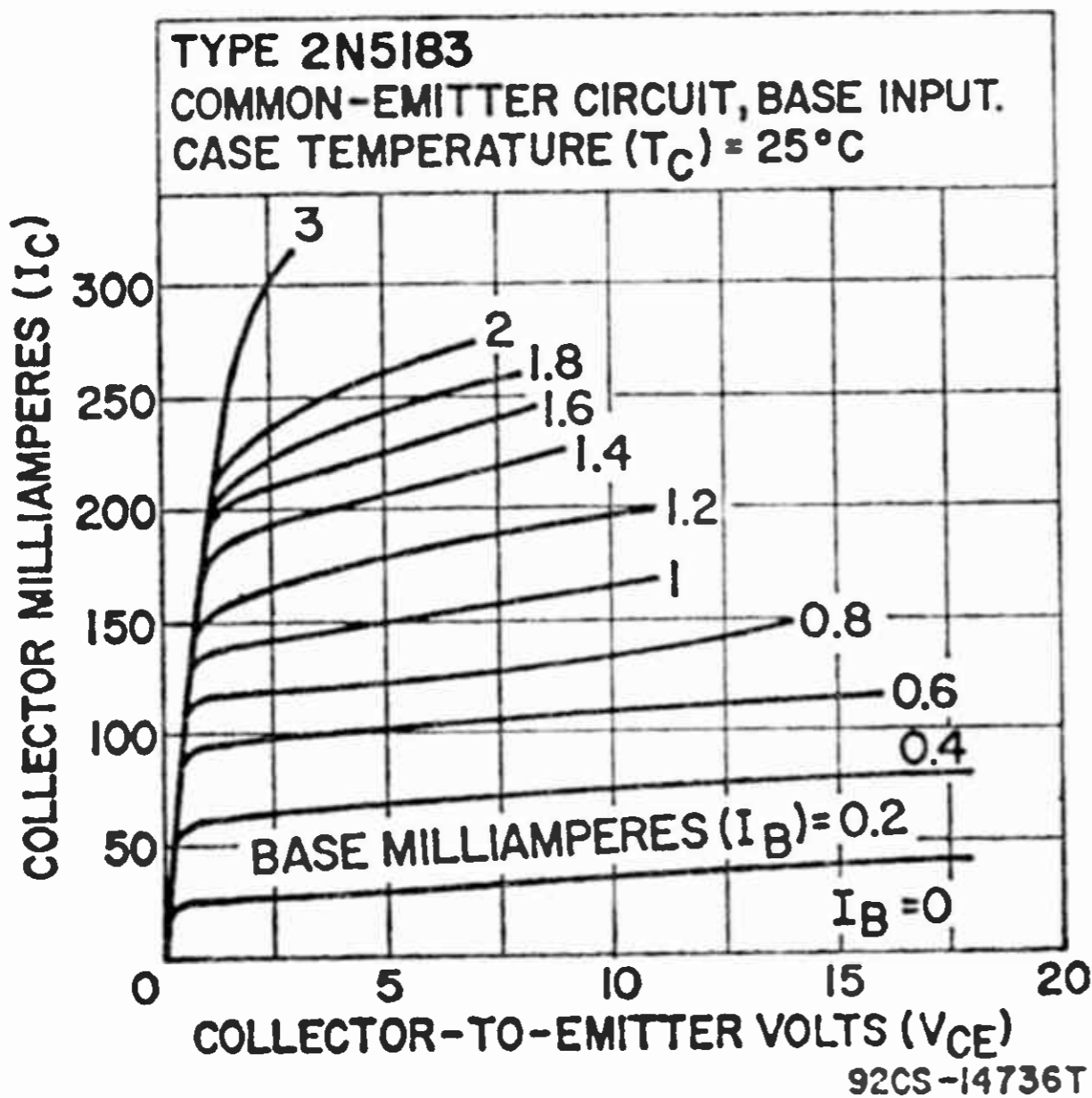
Collector-to-Base Breakdown Voltage ($I_C = 0.1\text{ mA}$)	$V_{(BR)CBO}$	18 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.05\text{ mA}$, $I_C = 0$)	$V_{(BR)EBO}$	7 min	V
Collector-to-Emitter Sustaining Voltage ($I_C = 10\text{ mA}$, $I_B = 0$)	$V_{CEO(\text{sus})}$	18 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 300\text{ mA}$, $I_B = 15\text{ mA}$)	$V_{CE(\text{sat})}$	0.35 typ; 0.5 max	V
Base-to-Emitter Saturation Voltage ($I_C = 300\text{ mA}$, $I_B = 15\text{ mA}$)	$V_{BE(\text{sat})}$	0.05 typ; 1.5 max	V
Collector-Cutoff Current ($V_{CB} = 12\text{ V}$, $I_E = 0$)	I_{CBO}	500 max	nA
Emitter-Cutoff Current ($V_{EB} = 2.5\text{ V}$, $I_C = 0$)	I_{EBO}	500 max	nA
Static Forward-Current Transfer Ratio:			
$V_{CE} = 10\text{ V}$, $I_C = 10\text{ mA}$	h_{FE}	75 to 400	
$V_{CE} = 10\text{ V}$, $I_C = 150\text{ mA}$	h_{FE}	120	
$V_{CE} = 1\text{ V}$, $I_C = 300\text{ mA}$	h_{FE}	40 min; 75 typ	

CHARACTERISTICS (cont'd)

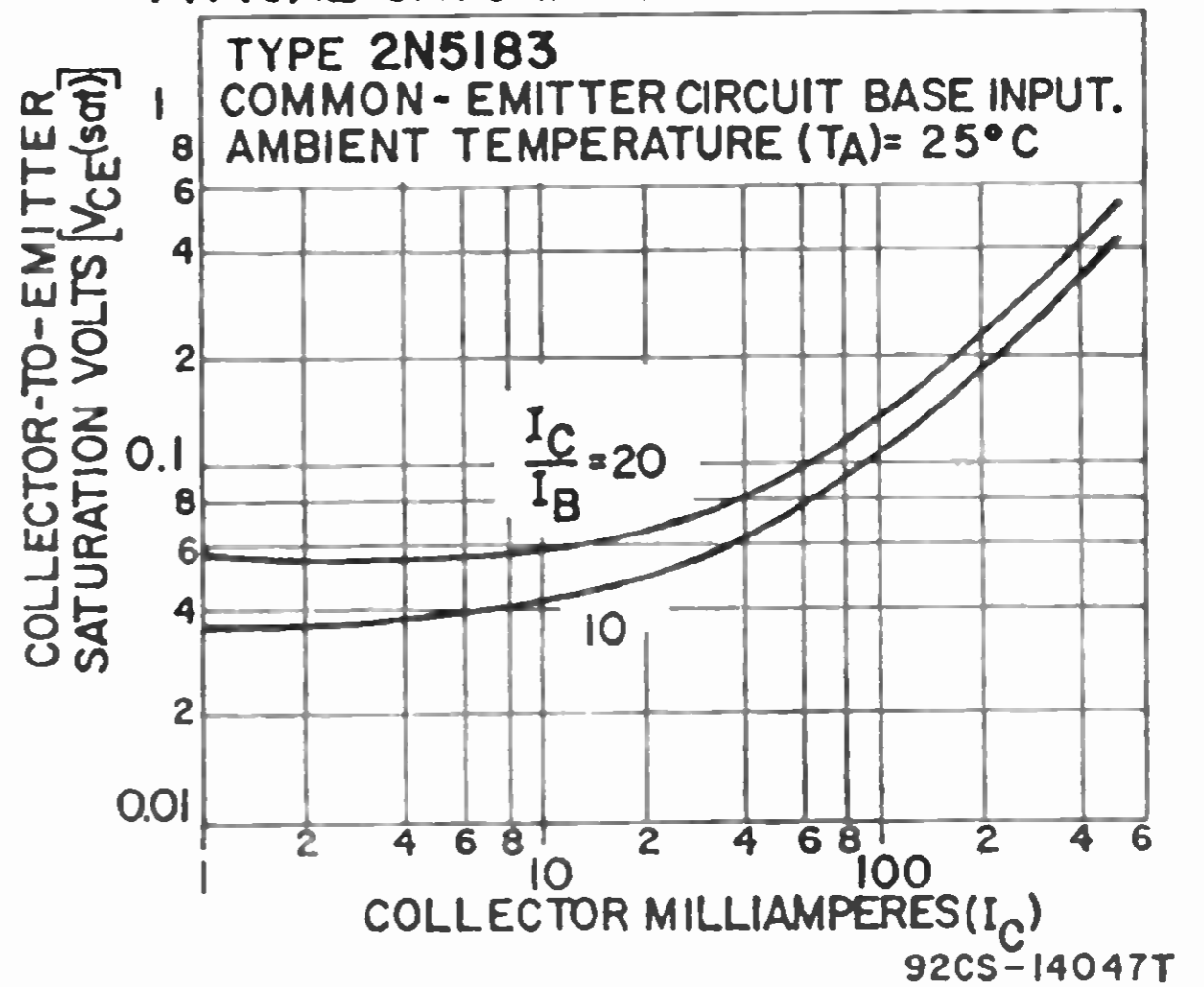
Magnitude of Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 12\text{ V}$, $I_C = 10\text{ mA}$, $f = 1\text{ kHz}$)	$ h_{fe} $	70 min; 175 typ	
Small-Signal Input Impedance ($V_{CE} = 12\text{ V}$, $I_C = 10\text{ mA}$, $f = 1\text{ kHz}$)	h_{ie}	600	Ω
Small-Signal Output Admittance ($V_{CE} = 12\text{ V}$, $I_C = 10\text{ mA}$, $f = 1\text{ kHz}$)	h_{oe}	75	mmho
Small-Signal Reverse-Voltage Transfer Ratio ($V_{CE} = 12\text{ V}$, $I_C = 10\text{ mA}$, $f = 1\text{ kHz}$)	h_{re}	125×10^{-6}	
Collector-to-Base Feedback Capacitance* ($V_{CB} = 6\text{ V}$, $I_E = 0$, $f = 1\text{ MHz}$)	C_{cb}	20 max	pF
Gain-Bandwidth Product ($V_{CE} = 1\text{ V}$, $I_C = 50\text{ MHz}$, $f = 50\text{ MHz}$)	f_T	125 min; 200 typ	MHz
Intrinsic Base-Spreading Resistance ($V_{CE} = 6\text{ V}$, $I_C = 1\text{ mA}$, $f = 100\text{ MHz}$)	$r_{bb'}$	20	Ω
Thermal Resistance, Junction-to-Case	θ_{J-C}	50 max	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	300 max	$^{\circ}\text{C}/\text{W}$

* Three-terminal measurement: Lead No. 1 (emitter) connected to guard terminal.

TYPICAL COLLECTOR CHARACTERISTICS



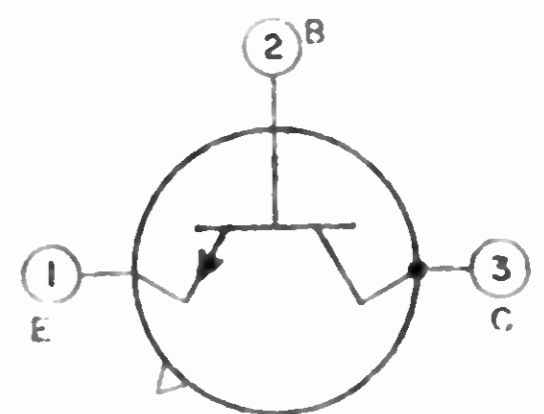
TYPICAL SATURATION CHARACTERISTICS



2N5184

TRANSISTOR

Si n-p-n type used in video-output-amplifier applications in black-and-white television receivers, and control applications in industrial equipment. JEDEC TO-104, Outline No.32.



MAXIMUM RATINGS

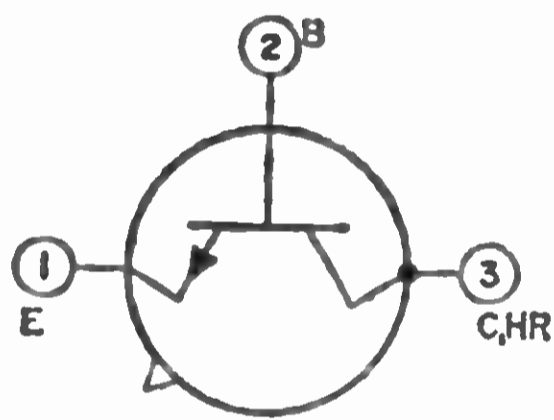
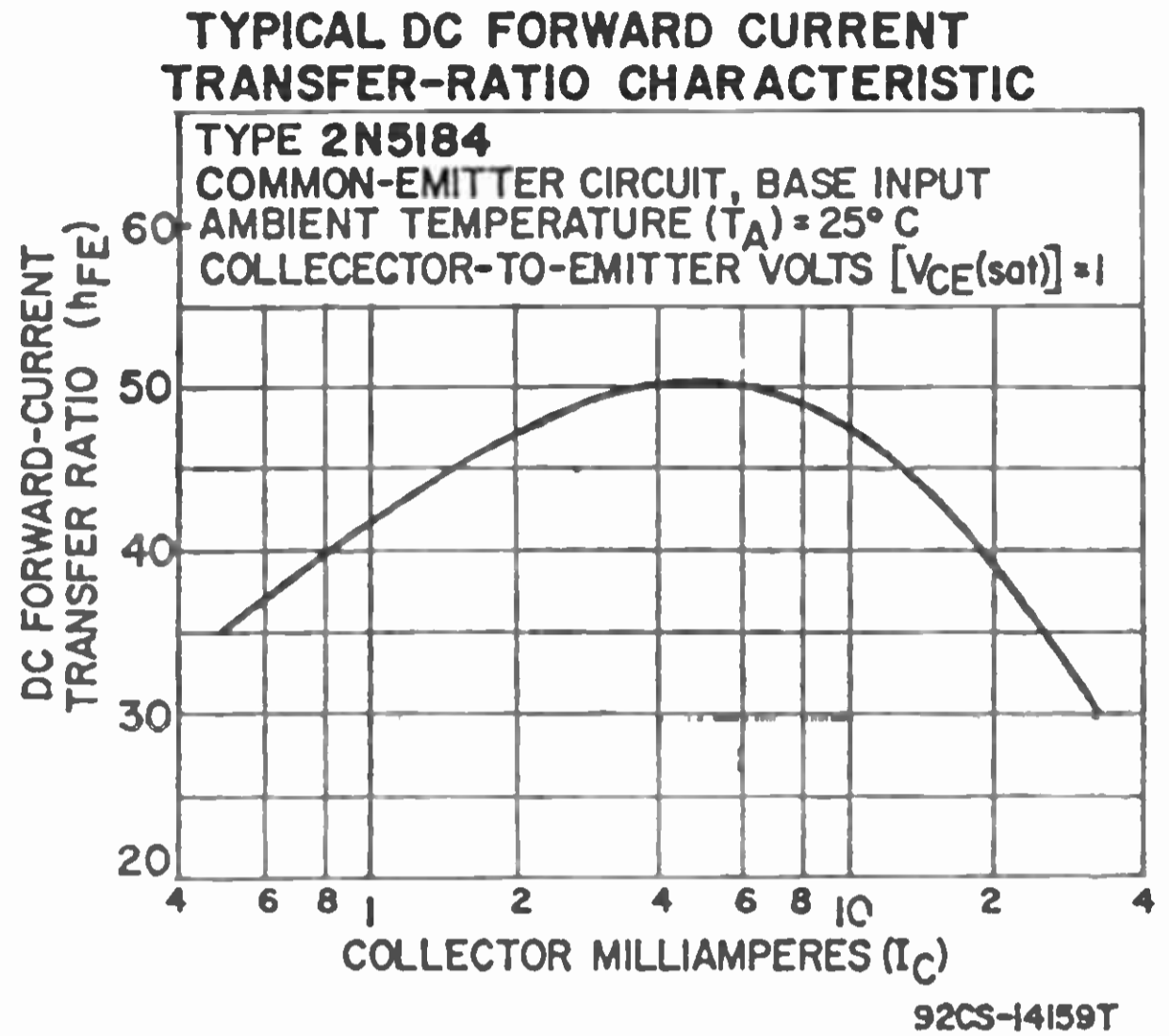
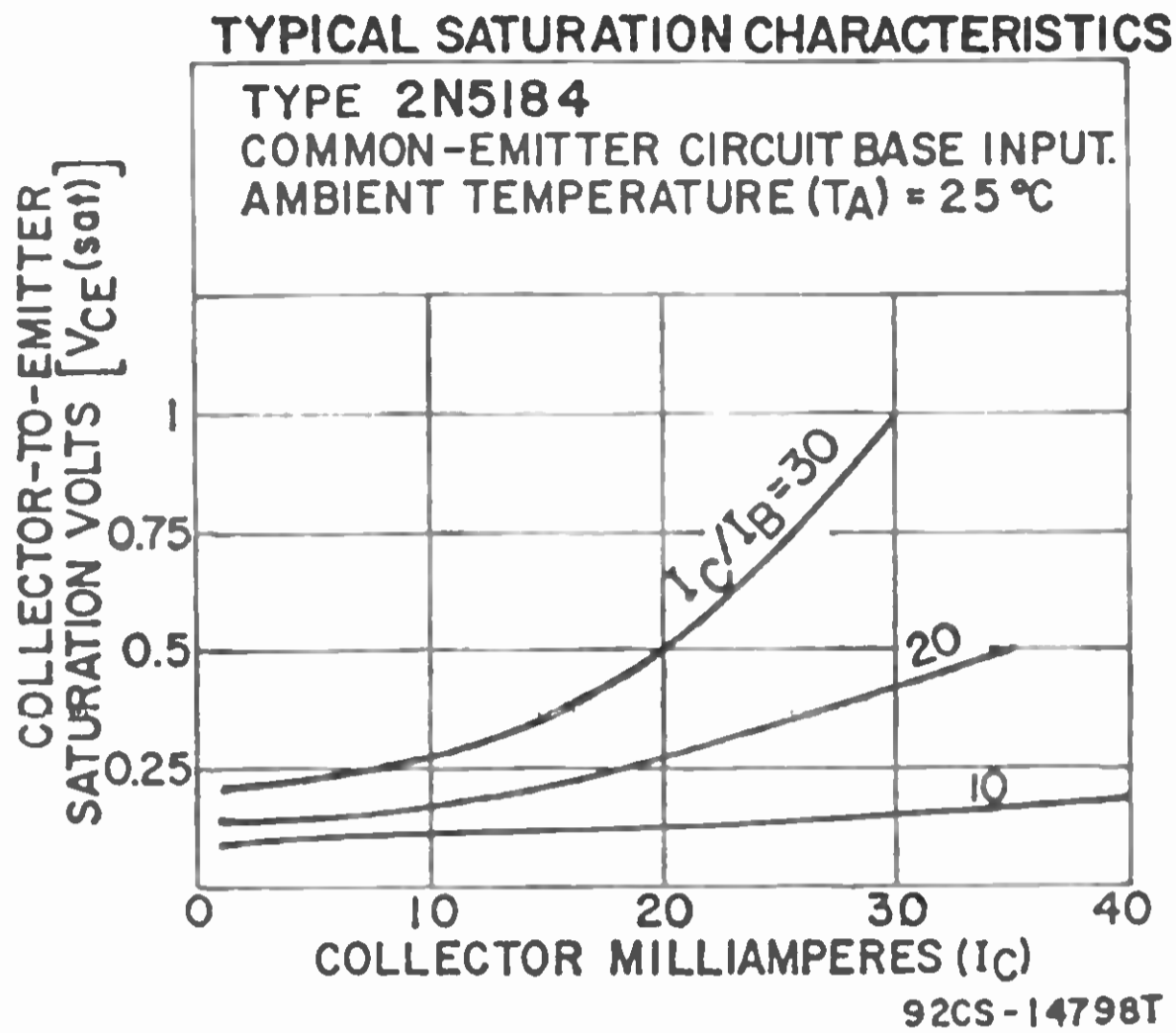
Collector-to-Emitter Voltage	V_{CEO}	120	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	50	mA
Transistor Dissipation:			
T_A up to 25°C	P_T	0.5	W
T_A above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 175	$^{\circ}\text{C}$
Storage	T_{STG}	-65 to 175	$^{\circ}\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	255	$^{\circ}\text{C}$

CHARACTERISTICS

Collector-to-Emitter Breakdown Voltage ($I_C = 1\text{ mA}$, $I_B = 0$)	$V_{(BR)CEO}$	120 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -10\ \mu\text{A}$, $I_C = 0$)	$V_{(BR)EBO}$	5 min; 7 typ	V
Collector-to-Emitter Saturation Voltage ($I_C = 30\text{ mA}$, $I_B = 1\text{ mA}$)	$V_{CE(\text{sat})}$	1 typ; 5 max	V
Collector-Cutoff Current ($V_{CB} = 120\text{ V}$, $I_E = 0$)	I_{CBO}	100 max	nA

CHARACTERISTICS (cont'd)

Static Forward-Current Transfer Ratio ($V_{CE} = 10\text{ V}$, $I_C = 50\text{ mA}$)	h_{FE}	10 min; 55 max	
Collector-to-Base Feedback Capacitance ($V_{CE} = 10\text{ V}$, $I_C = 30\text{ mA}$, $f = 1\text{ MHz}$)	C_{cb}	2.8 typ; 3.5 max	pF
Gain-Bandwidth Product: $V_{CE} = 10\text{ V}$, $I_C = 45\text{ mA}$	f_T	30 min; 100 typ	MHz
$V_{CE} = 120\text{ V}$, $I_C = 2\text{ mA}$	f_T	50 min; 100 typ	MHz
Thermal Resistance, Junction-to-Case	θ_{J-C}	45 typ; 60 max	$^{\circ}\text{C/W}$



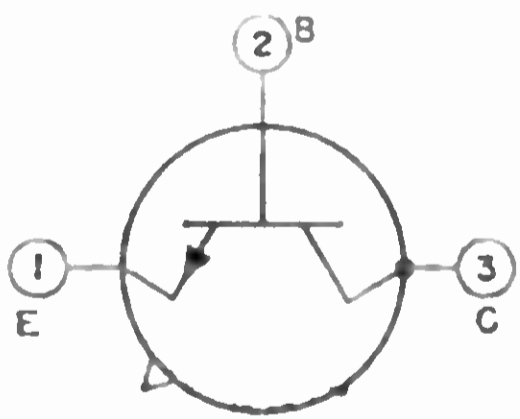
TRANSISTOR

2N5185

Si n-p-n type used in video-output-amplifier applications in black-and-white television receivers, and control applications in industrial equipment. JEDEC TO-104 (with radiator), Outline No.33. This type is identical with type 2N5184 except for the following item:

MAXIMUM RATINGS

Transistor Dissipation: T_A up to 25°C	P_T	1	W
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COMPUTER TRANSISTOR

2N5186

Si n-p-n epitaxial planar type used for switching applications in data-processing equipment and other critical military and industrial equipment. JEDEC TO-52, Outline No.21.

MAXIMUM RATINGS

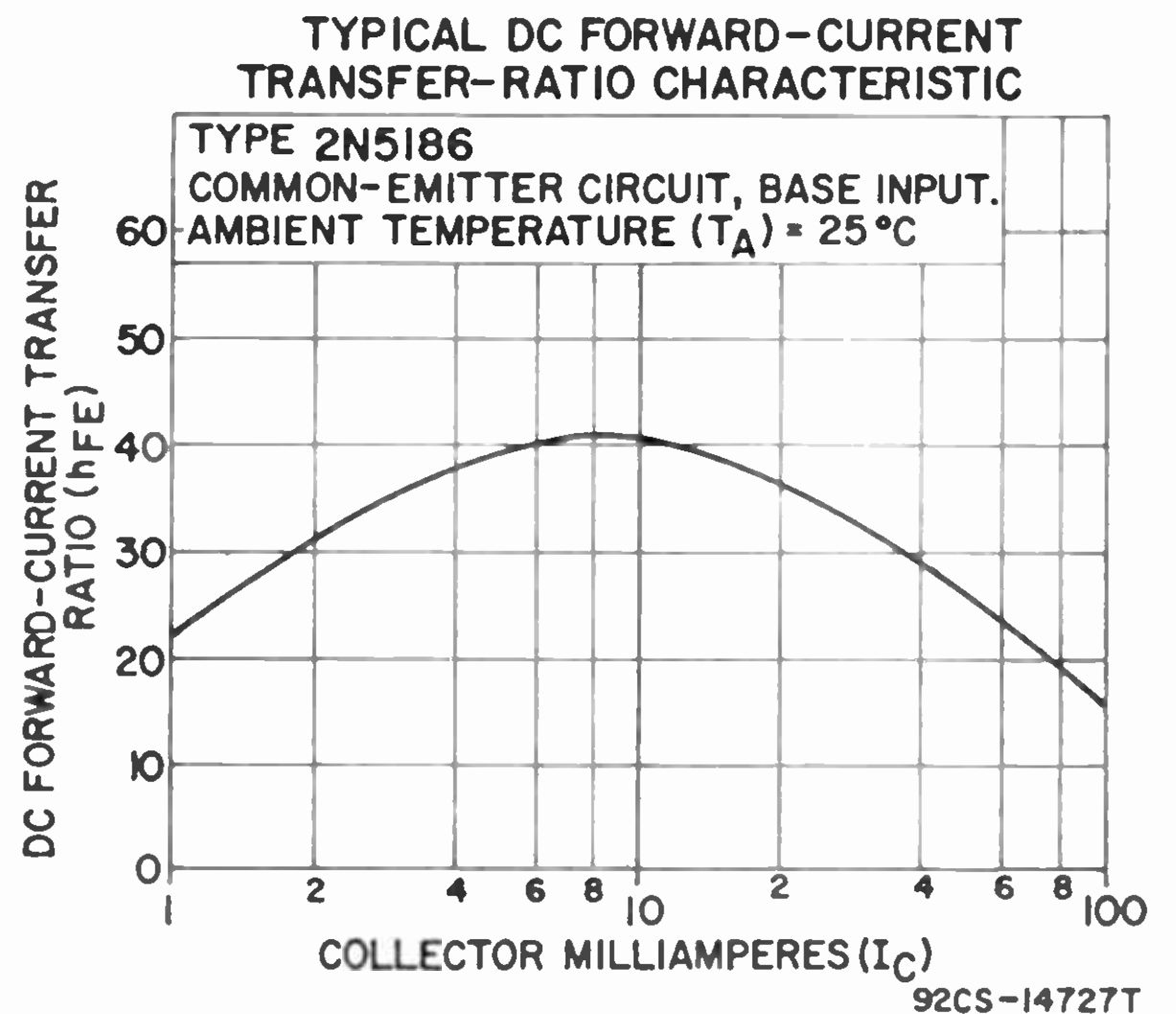
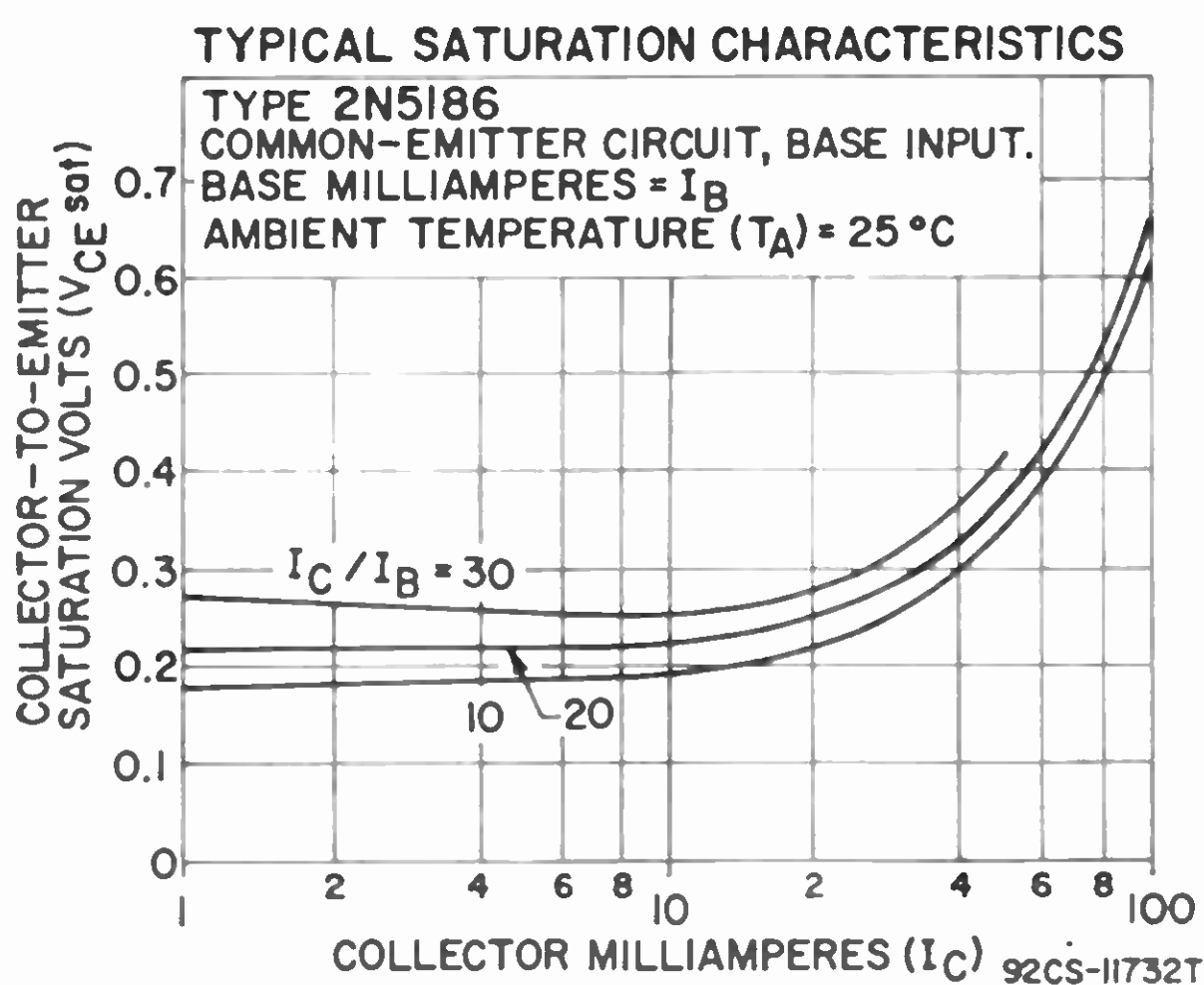
Collector-to-Base Voltage	V_{CBO}	10	V
Emitter-to-Base Voltage	V_{EBO}	3	V
Collector Current	I_C	300	mA
Transistor Dissipation: T_A up to 25°C	P_T	300	mW
T_A above 25°C	P_T	See curve page 300	
T_C up to 100°C	P_T	500	mW
T_C above 100°C	P_T	See curve page 300	
Temperature Range: Operating (Junction)	$T_J(\text{opr})$	-65 to 200	$^{\circ}\text{C}$
Storage	T_{STG}	-65 to 200	$^{\circ}\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	265	$^{\circ}\text{C}$

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = 0.01\text{ mA}$, $I_E = 0$)	$V_{(BR)CBO}$	10 min	V
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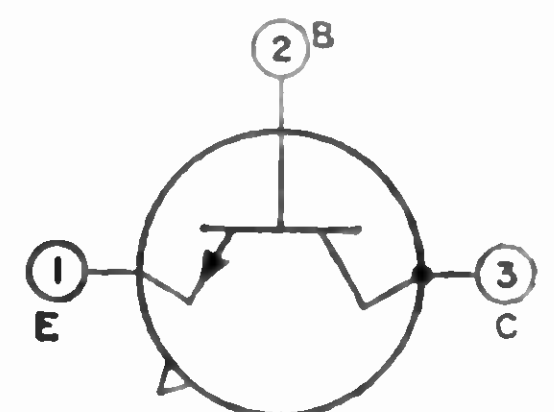
CHARACTERISTICS (cont'd)

Emitter-to-Base Breakdown Voltage ($I_E = -0.01$ mA, $I_C = 0$)	$V_{(BR)EBO}$	3 min	V
Collector-to-Emitter Sustaining Voltage ($I_C = 10$ mA, $I_B = 0$)	$V_{CEO(SUS)}$	6 min; 10 typ	V
Collector-to-Emitter Saturation Voltage ($I_C = 10$ mA, $I_B = 1$ mA)	$V_{CE(sat)}$	0.3 max	V
Base-to-Emitter Saturation Voltage ($I_C = 10$ mA, $I_B = 1$ mA)	$V_{BE(sat)}$	1 max	V
Collector-Cutoff Current: $V_{CB} = 5$ V, $I_E = 0$	I_{CBO}	0.002 typ; 0.05 max	μA
$V_{CB} = 5$ V, $I_E = 0$, $T_A = 150^\circ C$	I_{CBO}	0.9 typ; 5 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 1$ V, $I_C = 10$ mA)	h_{FE}	25 min	
Magnitude of Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 4$ V, $I_C = 10$ mA, $f = 100$ MHz)	$ h_{fe} $	4 min; 6 typ	
Output Capacitance ($V_{CB} = 5$ V, $I_E = 0$, $f = 0.140$ MHz)	C_{obo}	3 max	pF
Input Capacitance ($V_{EB} = 0.5$ V, $I_C = 0$, $f = 0.140$ MHz)	C_{ibo}	3 max	pF
Storage Time ($I_C = 5$ mA, $I_{B1} = -I_{B2} = 5$ mA)	t_s	10 max	ns
Turn-On Time ($I_C = 10$ mA, $I_{B1} = -I_{B2} = 1$ mA)	$t_d + t_r$	25 max	ns
Turn-Off Time ($I_C = 10$ mA, $I_{B1} = -I_{B2} = 1$ mA)	$t_s + t_f$	25 max	ns



2N5187 COMPUTER TRANSISTOR

Si n-p-n epitaxial planar type used for switching applications in data-processing equipment and other critical applications in military and industrial equipment. JEDEC TO-52, Outline No.21.



MAXIMUM RATINGS

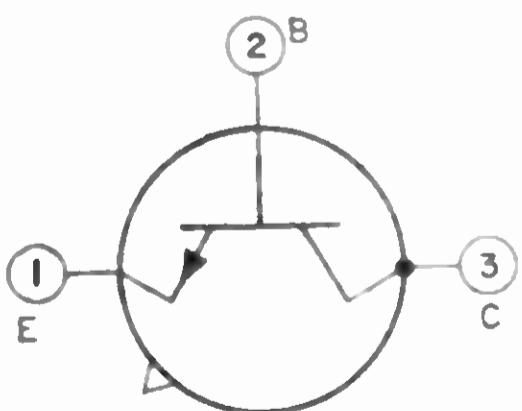
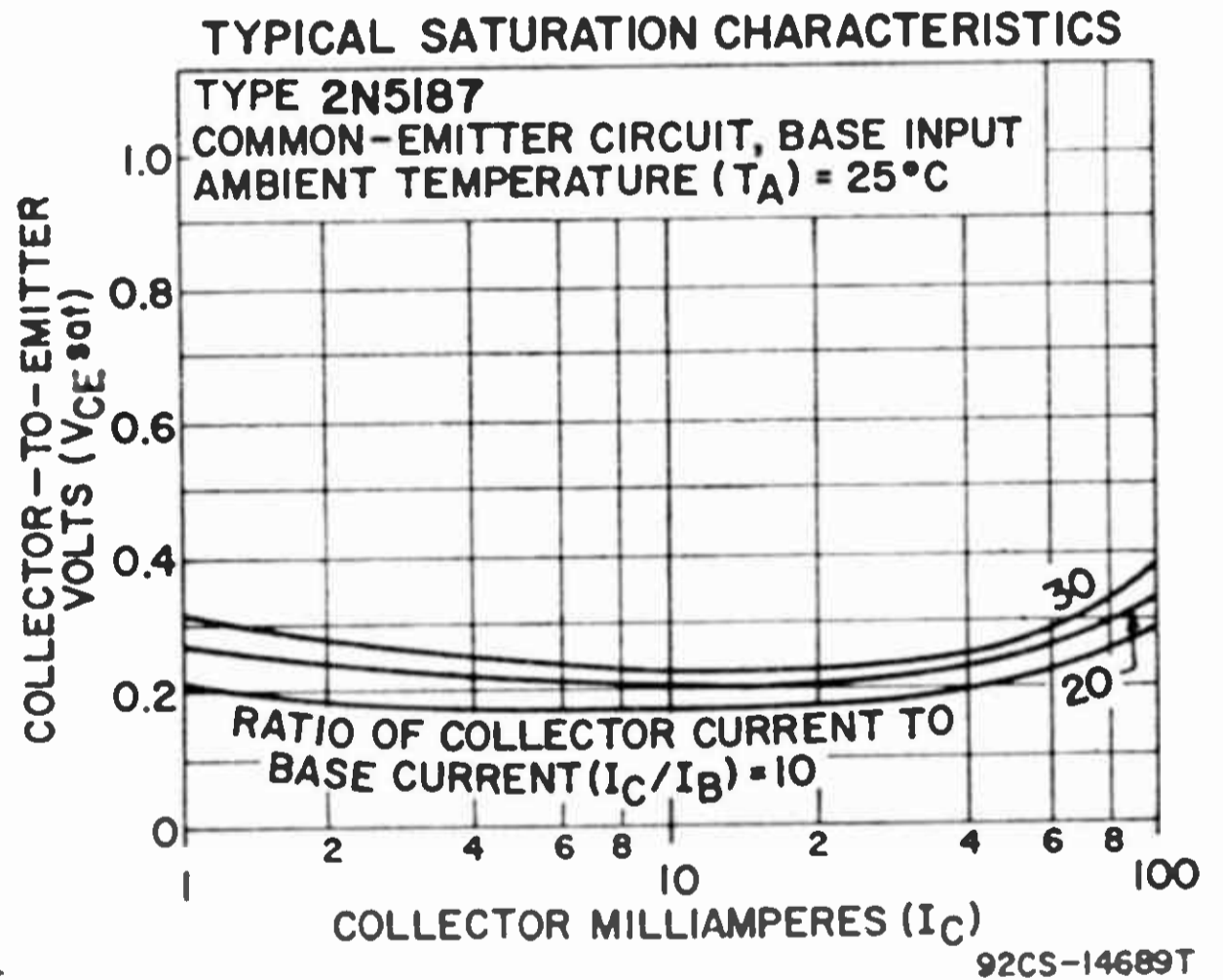
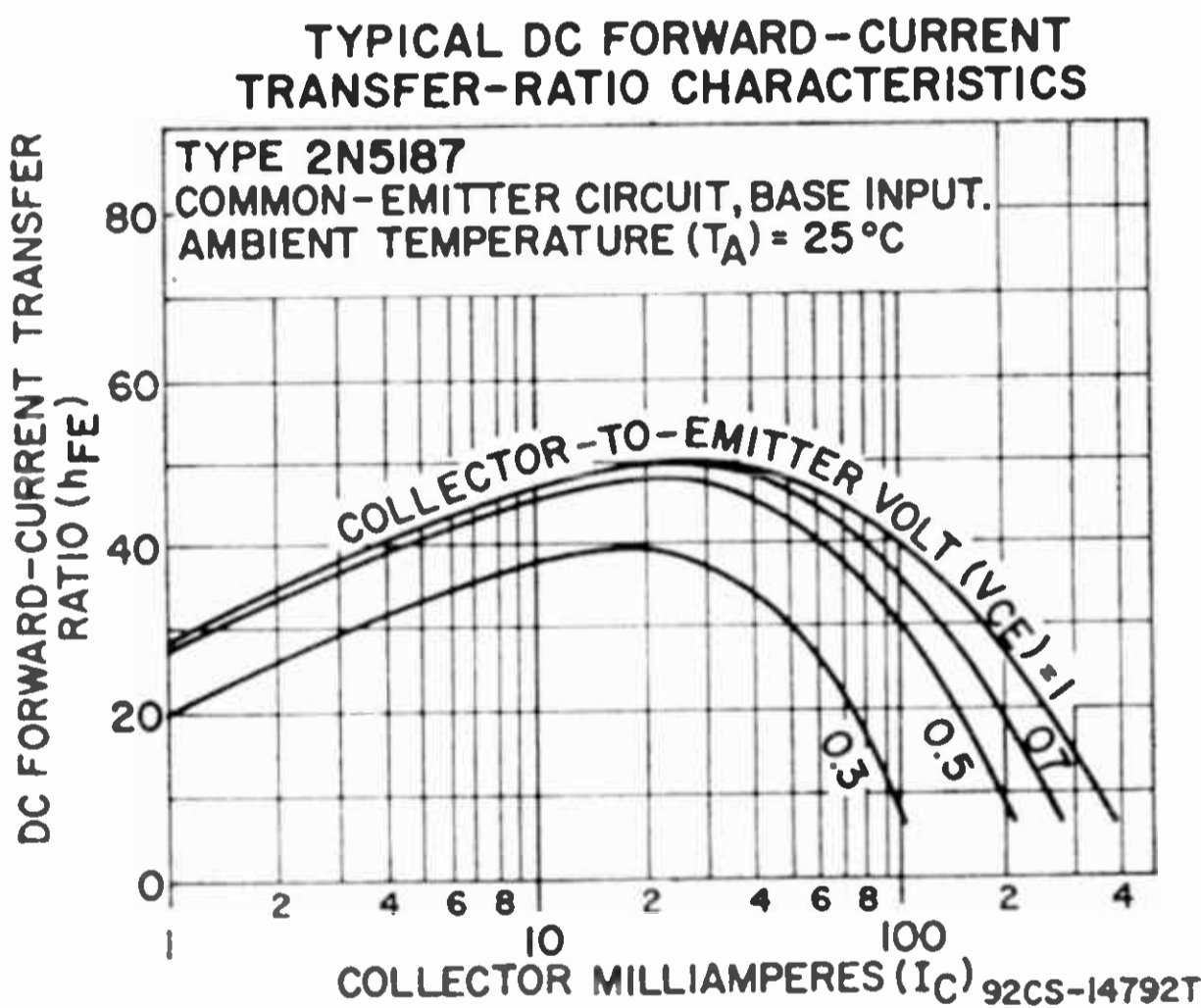
Collector-to-Base Voltage	V_{CBO}	25	V
Collector-to-Emitter Voltage	V_{CEO}	10	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	500	mA
Transistor Dissipation:			
T_c up to $25^\circ C$	P_T	1	W
T_c above $25^\circ C$	P_T	Derate at 5.72	mW/ $^\circ C$
T_A up to $25^\circ C$	P_T	0.3	W
T_A above $25^\circ C$	P_T	Derate at 1.71	mW/ $^\circ C$
Temperature Range:			
Operating	$T(opr)$	-65 to 200	$^\circ C$
Storage	T_{STG}	-65 to 200	$^\circ C$
Lead-Soldering Temperature (10 s max)	T_L	265	$^\circ C$

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = 0.01$ mA, $I_E = 0$)	$V_{(BR)CBO}$	25 min	V
Collector-to-Emitter Breakdown Voltage ($I_C = 10$ mA, $I_B = 0$, $t_P \leq 100 \mu s$, $df \leq 0.02$)	$V_{(BR)CEO}$	10 min	V

CHARACTERISTICS (cont'd)

Emitter-to-Base Breakdown Voltage ($I_E = -0.01$ mA, $I_C = 0$)	$V_{(BR)EBO}$	5 min	V
Collector-to-Emitter Saturation Voltage: $I_C = 100$ mA, $I_B = 10$ mA, $t_P \leq 100$ μ s, $df \leq 0.02$	$V_{CE(sat)}$	0.3 typ; 0.5 max	V
$I_C = 10$ mA, $I_B = 1$ mA	$V_{CE(sat)}$	0.2 typ; 0.25 max	V
Base-to-Emitter Saturation Voltage: $I_C = 100$ mA, $I_B = 10$ mA, $t_P \leq 100$ μ s, $df \leq 0.02$	$V_{BE(sat)}$	0.98 typ; 1.2 max	V
$I_C = 10$ mA, $I_B = 1$ mA	$V_{BE(sat)}$	0.8 typ; 0.85 max	V
Collector-Cutoff Current ($V_{CE} = 20$ V, $V_{EB} = 0$)	I_{CBO}	450 max	nA
Static Forward-Current Transfer Ratio: $V_{CE} = 1$ V, $I_C = 10$ mA	h_{FE}	30 min	
$V_{CE} = 0.4$ V, $I_C = 30$ mA	h_{FE}	25 min	
Magnitude of Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 10$ V, $I_C = 10$ mA, $f = 100$ MHz)	$ h_{fe} $	4 min; 6 typ	
Output Capacitance ($V_{CB} = 5$ V, $I_E = 0$, $f = 0.140$ MHz)	C_{obo}	2.8 typ; 3.5 max	pF
Input Capacitance ($V_{EB} = 0.5$ V, $I_C = 0$, $f = 0.140$ MHz)	C_{ibo}	3 typ; 4 max	pF
Delay Time ($V_{CC} = 6$ V, $V_{BE(off)} = -4$ V, $I_{B1} = 10$ mA, $I_{CS} = 100$ mA, $I_{B2} = -10$ mA)	t_d	6 typ; 8 max	ns
Rise Time ($V_{CC} = 6$ V, $V_{BE(off)} = -4$ V, $I_{B1} = 10$ mA, $I_{CS} = 100$ mA, $I_{B2} = -10$ mA)	t_r	6 typ; 10 max	ns
Storage Time: $V_{CC} = 6$ V, $I_{B1} = 10$ mA, $I_{CS} = 100$ mA, $I_{B2} = -10$ mA	t_s	9 typ; 13 max	ns
$V_{CC} = 10$ V, $I_{B1} = 10$ mA, $I_{CS} = 10$ mA, $I_{B2} = -10$ mA	t_s	9 typ; 13 max	ns
Fall Time ($V_{CC} = 6$ V, $I_{B1} = 10$ mA, $I_{CS} = 100$ mA, $I_B = -10$ mA)	t_f	5 typ; 8 max	ns



COMPUTER TRANSISTOR 2N5188

Si n-p-n double-diffused epitaxial planar type used for core-driver and line-driver service in data-processing equipment and other critical applications in military and industrial equipment. JEDEC TO-39, Outline No.15.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	60	V
Collector-to-Emitter Voltage	V_{CEO}	25	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	Limited by dissipation	
Transistor Dissipation:			
T_C up to 25°C	P_T	4	W
T_C above 25°C	P_T	Derate at 22.8 mW/°C	
T_A up to 25°C	P_T	0.8	W
T_A above 25°C	P_T	Derate at 4.6 mW/°C	

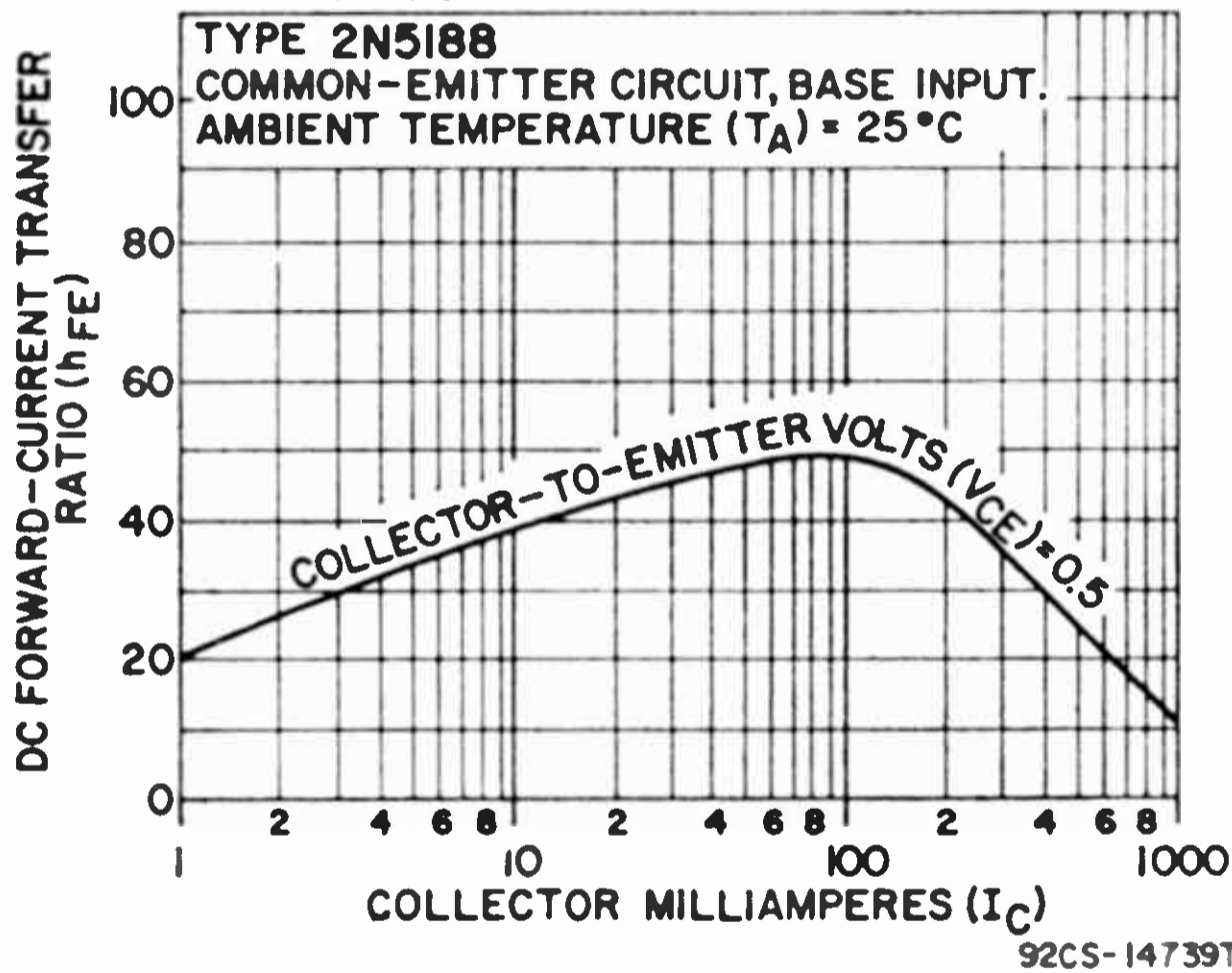
MAXIMUM RATINGS (cont'd)

Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	265	°C

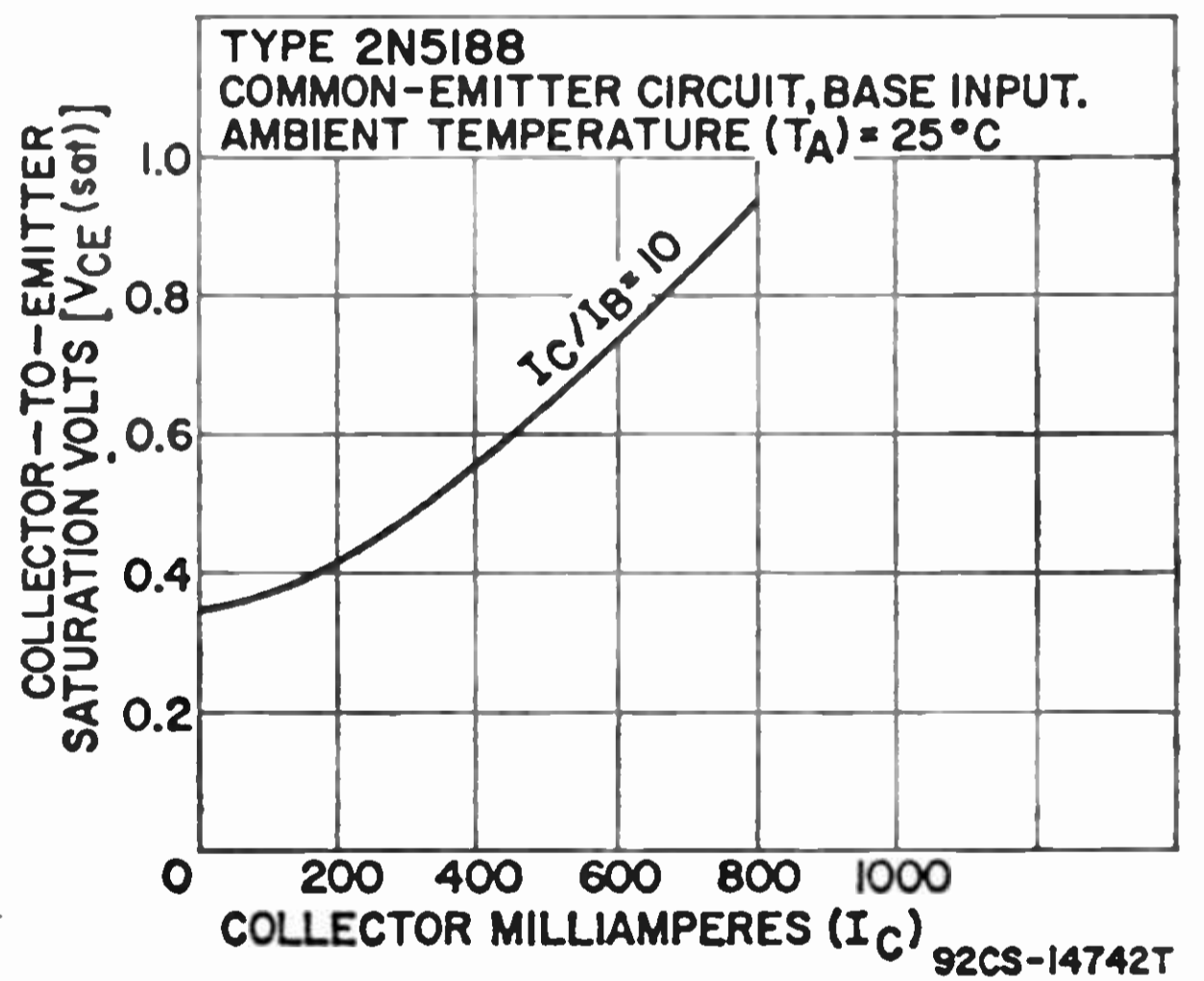
CHARACTERISTICS

Collector-to-Emitter Breakdown Voltage ($I_C = 30$ mA, $I_E = 0$)	$V_{(BR)CEO}$	25 min	V
Collector-to-Base Breakdown Voltage ($I_C = 0.01$ mA, $I_E = 0$)	$V_{(BR)CBO}$	60 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -0.01$ mA, $I_C = 0$)	$V_{(BR)EBO}$	5 min	V
Collector-to-Emitter Saturation Voltage: $I_C = 150$ mA, $I_B = 7.5$ mA	$V_{CE(sat)}$	0.5 max	V
$I_C = 500$ mA, $I_B = 50$ mA, $t_P < 400$ μ s, $df < 0.03$...	$V_{CE(sat)}$	1 max	V
Base-to-Emitter Voltage: $I_C = 150$ mA, $I_B = 7.5$ mA	V_{BE}	1.1 max	V
$I_C = 500$ mA, $I_B = 50$ mA, $t_P < 400$ μ s, $df < 0.03$...	V_{BE}	1.5 max	V
Collector-Cutoff Current ($V_{CB} = 30$ V, $I_E = 0$)	I_{CBO}	0.5 max	μ A
Static Forward-Current Transfer Ratio: $V_{CE} = 1$ V, $I_C = 500$ mA, $t_P < 400$ μ s, $df < 0.03$...	h_{FE} (pulsed)	20 min	
$V_{CE} = 0.5$ V, $I_C = 150$ mA	h_{FE}	25 min	
Magnitude of Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 10$ V, $I_C = 50$ mA, $f = 100$ MHz)	$ h_{fe} $	2.5 min	
Output Capacitance ($V_{CB} = 10$ V, $I_E = 0$, $f = 140$ kHz)	C_{obo}	8 typ; 10 max	pF
Storage Time ($V_{CC} = 6.4$ V, $I_C = 150$ mA, $I_{B1} = I_{B2} = 15$ mA	t_s	35 max	ns
Turn-On Time ($V_{CC} = 6.4$ V, $I_C = 150$ mA, $I_{B1} = I_{B2} = 15$ mA	t_{on}	35 max	ns
Turn-Off Time ($V_{CC} = 6.4$ V, $I_C = 150$ mA, $I_{B1} = I_{B2} = 15$ mA	t_{off}	50 max	ns

TYPICAL DC FORWARD-CURRENT TRANSFER-RATIO CHARACTERISTIC

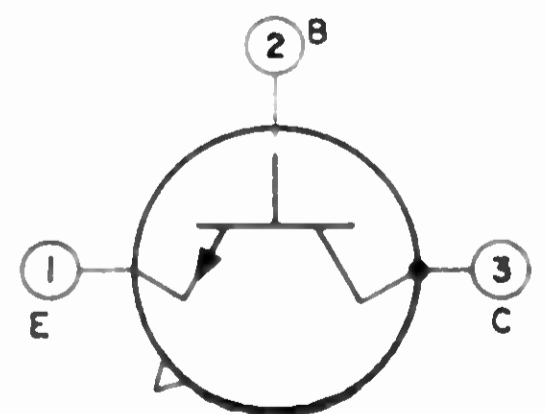


TYPICAL SATURATION CHARACTERISTIC



2N5189 COMPUTER TRANSISTOR

Si n-p-n double-diffused epitaxial planar type used for core-driver and line-driver service in data-processing equipment and other critical applications in military and industrial equipment. Outline No.58.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	60	V
Collector-to-Emitter Voltage	V_{CEO}	35	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	Limited by dissipation	
Transistor Dissipation:			
T_C up to 25°C	P_T	5	W
T_C above 25°C	P_T	Derate at 28.5 mW/°C	
T_A up to 25°C	P_T	1	W
T_A above 25°C	P_T	Derate at 5.7 mW/°C	

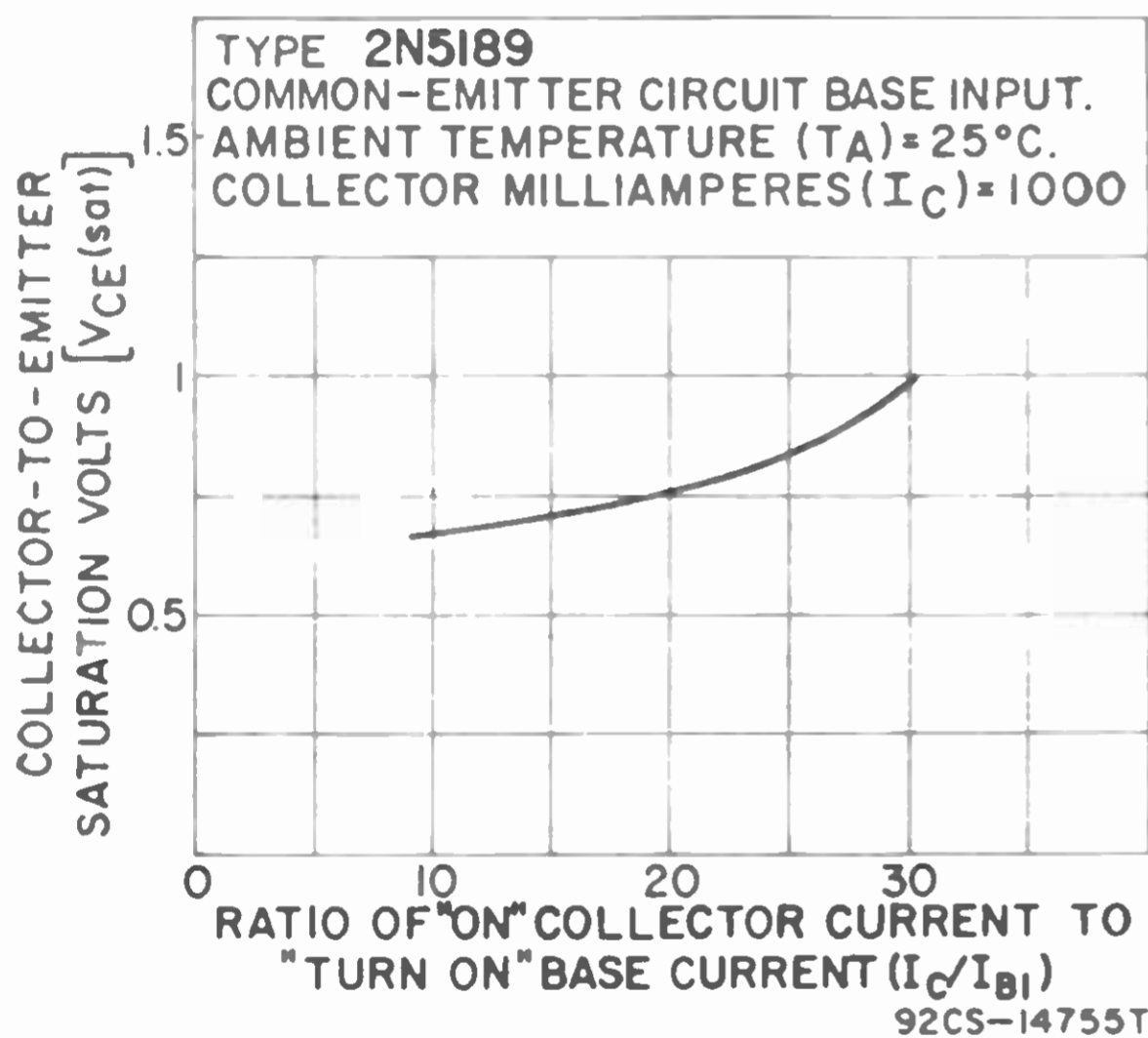
MAXIMUM RATINGS (cont'd)

Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	265	°C

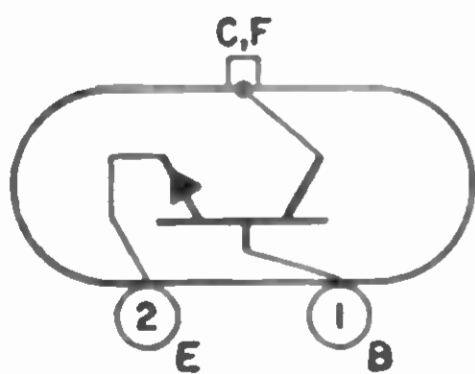
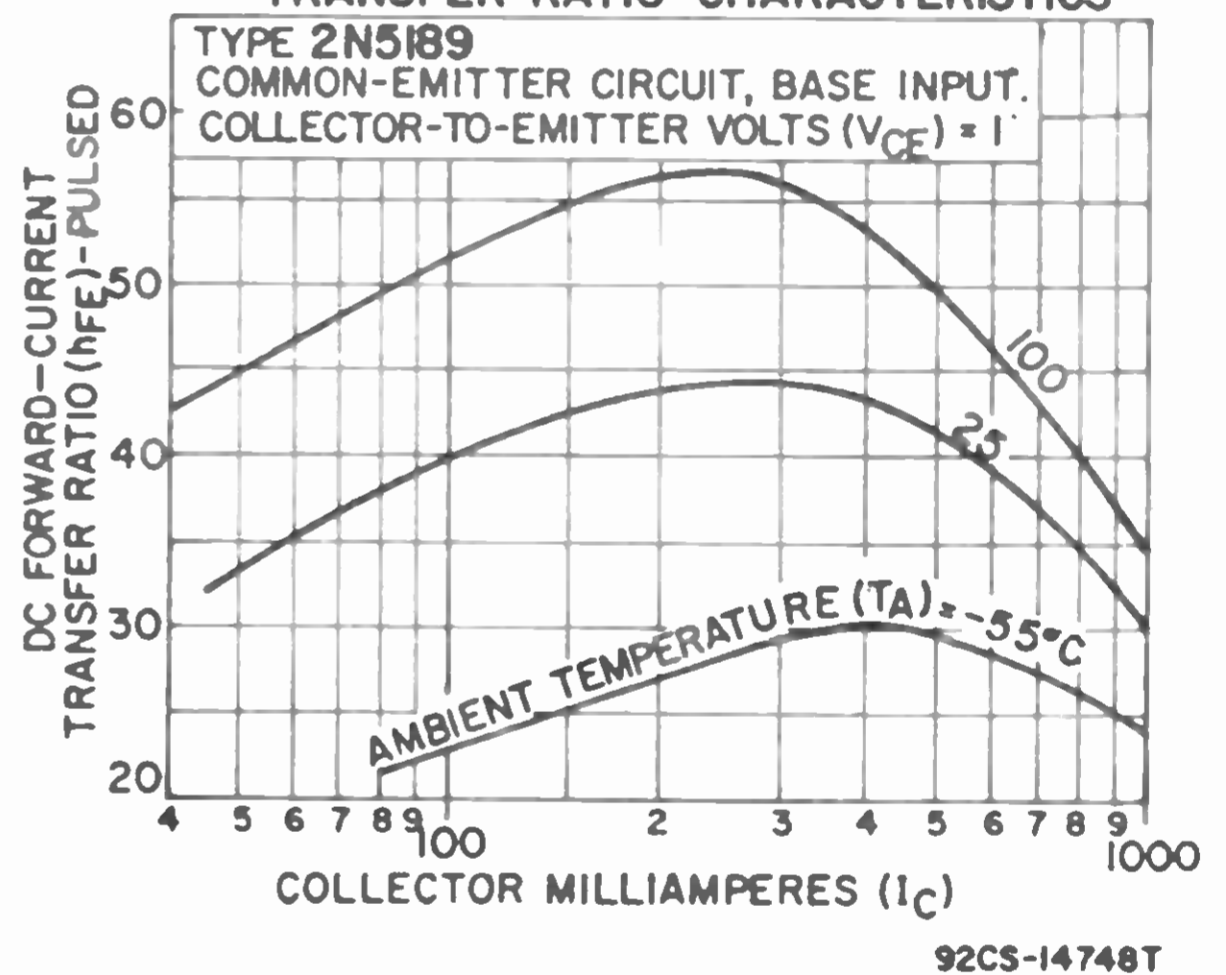
CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = 0.1$ mA)	$V_{(BR)CBO}$	60 min	V
Collector-to-Emitter Breakdown Voltage ($I_C = 10$ mA)	$V_{(BR)CEO}$	35 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -0.1$ mA)	$V_{(BR)EBO}$	5 max	V
Collector-to-Emitter Saturation Voltage ($I_C = 1000$ mA, $I_B = 100$ mA)	$V_{CE(sat)}$	1 max	V
Base-to-Emitter Saturation Voltage ($I_C = 1000$ mA, $I_B = 100$ mA)	$V_{BE(sat)}$	1.5 max	V
Collector-Cutoff Current ($V_{CE} = 30$ V)	I_{CBO}	0.5 max	μA
Static Forward-Current Transfer Ratio:			
$V_{CE} = 1$ V, $I_C = 100$ mA	h_{FE}	30 max	
$V_{CE} = 1$ V, $I_C = 500$ mA	h_{FE}	35 max	
$V_{CE} = 1$ V, $I_C = 500$ mA, $t_P \leq 400$ μs , $df \leq 0.03$	h_{FE} (pulsed)	15 max	
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 10$ V, $I_C = 50$ mA, $f = 100$ MHz)	h_{fe}	2.5 min	
Output Capacitance ($V_{CB} = 10$ V, $I_E = 0$, $f = 0.1$ MHz)	C_{obo}	12 max	pF
Turn-On Time ($I_C = 1000$ mA, $I_{B1} = 100$ mA)	$t_d + t_r$	40 max	ns
Turn-Off Time ($I_C = 1000$ mA, $I_{B1} = 100$ mA, $I_{B2} = -100$ mA)	$t_s + t_r$	70 max	ns

TYPICAL SATURATION CHARACTERISTIC



TYPICAL DC FORWARD-CURRENT TRANSFER-RATIO CHARACTERISTICS



POWER TRANSISTOR

2N5202

Si n-p-n epitaxial type used in high-current, high-speed switching circuits. JEDEC TO-66, Outline No.25.

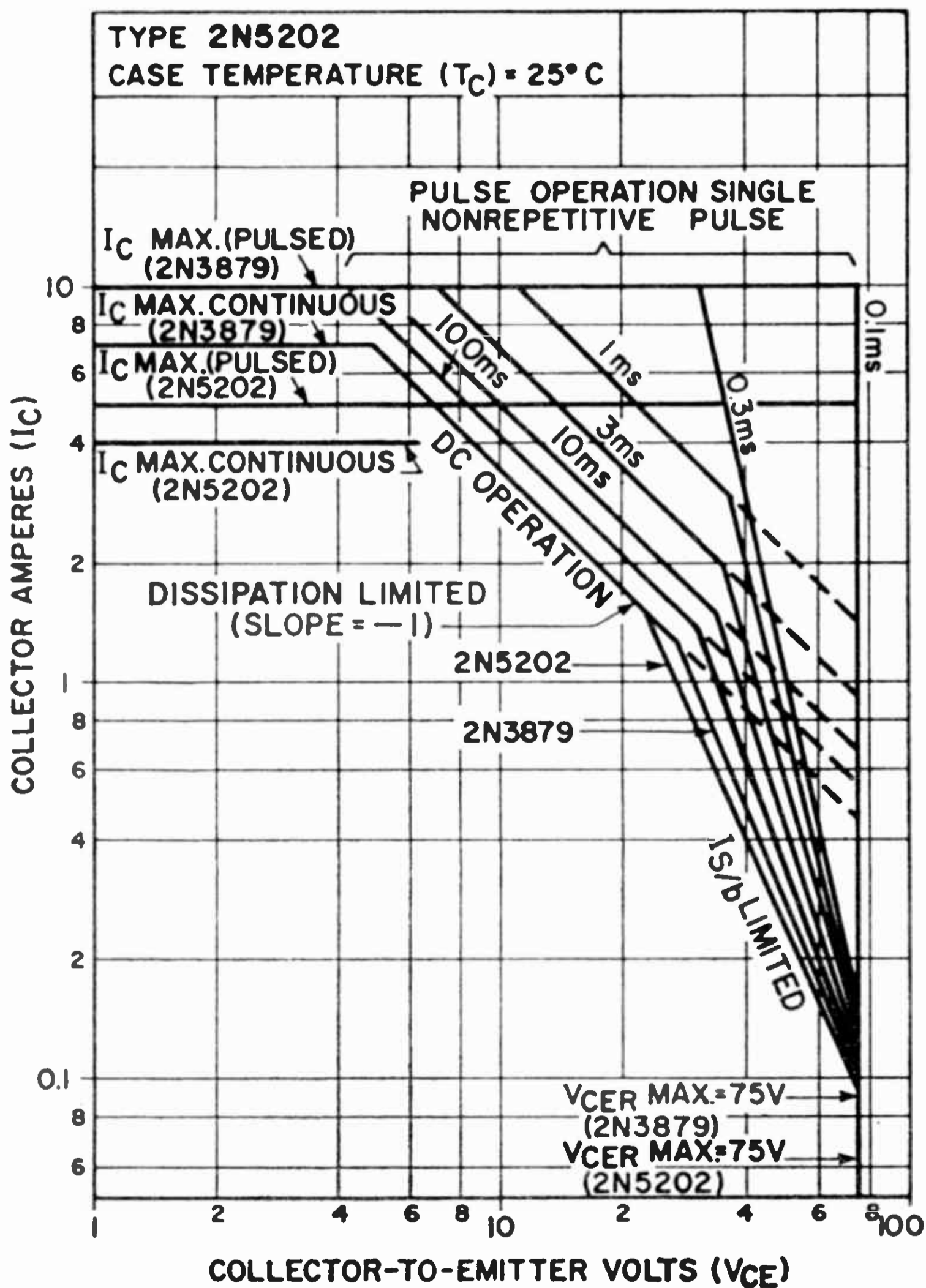
MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	120	V
Collector-to-Emitter Sustaining Voltage: $R_{BE} = 50 \Omega$	$V_{CER(SUS)}$	75	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Collector Current	I_C	4	A
Peak Collector Current	i_C	5	A
Base Current	I_B	2	A
Transistor Dissipation:			
T_c up to 25°C	P_T	35	W
T_c above 25°C		See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Pin-Soldering Temperature (10 s max)	T_P	255	°C

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage: ($I_C = 0.2$ A, $R_{BE} = 50 \Omega$)	$V_{CER(SUS)}$	75 min	V
Base-to-Emitter Voltage ($V_{CE} = 1.2$ V, $I_C = 4$ V)	V_{BE}	1.9 max	V
Collector-to-Emitter Saturation Voltage ($I_C = 4$ A, $I_B = 0.4$ A)	$V_{CE(sat)}$	1.2 max	V
Collector-Cutoff Current: $V_{CE} = 100$ V, $V_{BE} = -1.5$ V	I_{CEV}	10 max	mA
$V_{CE} = 100$ V, $V_{BE} = -1.5$ V, $T_C = 150^\circ\text{C}$	I_{CEV}	10 max	mA
Emitter-Cutoff Current ($V_{EB} = 6$ V, $I_C = 0$)	I_{EBO}	10 max	mA
Output Capacitance ($V_{CB} = 10$ V, $I_E = 0$, $f = 1$ MHz)	C_{obo}	175 max	pF
Second-Breakdown Collector Current ($V_{CE} = 40$ V, non-repetitive pulse = 1 s, base forward-biased) ...	$I_{S/b}$	400 min	mA
Second-Breakdown Energy ($V_{BB} = -4$ V, $R_B = 50 \Omega$, $L = 50 \mu\text{H}$)	$E_{S/b}$	0.4 min	mJ
Static Forward-Current Transfer Ratio ($V_{CE} = 1.2$ V, $I_C = 4$ A)	h_{FE}	10 to 100	ns
Small-Signal, Forward-Current Transfer Ratio ($V_{CE} = 10$ V, $I_C = 0.5$ A, $f = 10$ MHz)	h_{fe}	6 min	
Delay Time ($V_{CC} = 30$ V, $I_C = 4$ A, $I_{B1} = 0.4$ A) ...	t_d	40 max	ns
Rise Time ($V_{CC} = 30$ V, $I_C = 4$ A, $I_{B1} = 0.4$ A) ...	t_r	400 max	ns
Storage Time ($V_{CC} = 30$ V, $I_C = 4$ A, $I_{B2} = -0.4$ A) ...	t_s	800 max	ns
Fall Time ($V_{CC} = 30$ V, $I_C = 4$ A, $I_{B2} = -0.4$ A) ...	t_f	400 max	ns
Thermal Resistance, Junction-to-Case	θ_{J-C}	5 max	$^\circ\text{C/W}$

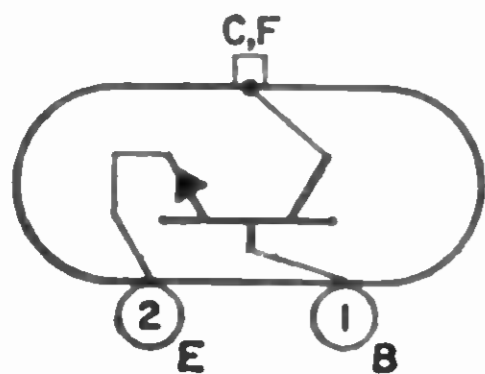
MAXIMUM OPERATING AREAS



9255-3691

POWER TRANSISTOR

2N5239



Si n-p-n multiple epitaxial type used for high-voltage, high-power in linear applications in industrial and commercial service. JEDEC TO-3, Outline No.2. See Mounting Hardware for desired mounting arrangement.

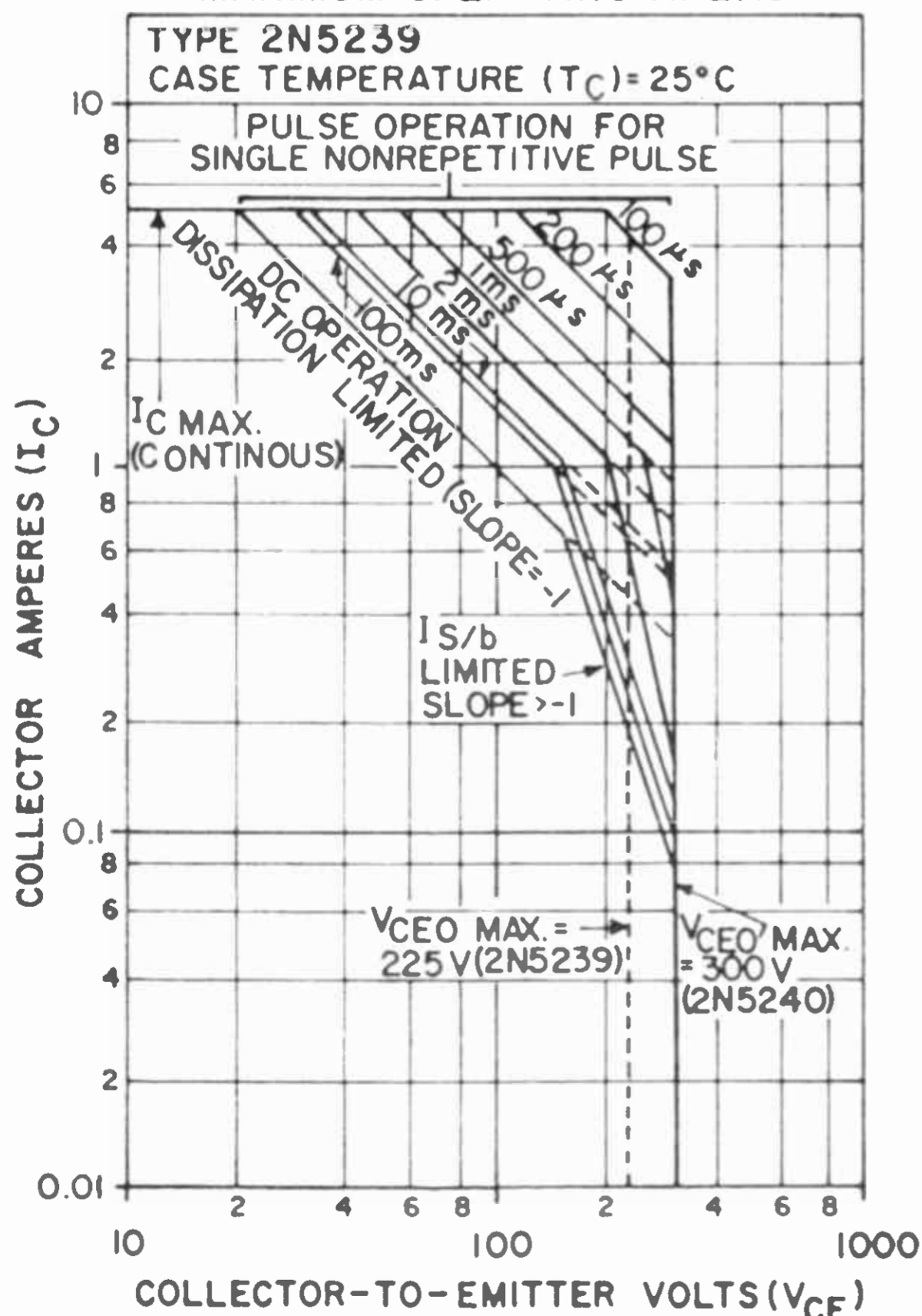
MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	330	V
Collector-to-Emitter Sustaining Voltage:			
$R_{BE} \leq 50\Omega$	$V_{CER(SUS)}$	250	V
Base open	$V_{CEO(SUS)}$	225	V
Emitter-to-Base Voltage	V_{EBO}	6	V
Collector Current	I_C	5	A
Transistor Dissipation:			
T_C up to 25°C and V_{CE} up to 150 V	P_T	100	W
T_C and T_A up to 25°C and V_{CE} above 150 V	P_T	See curve page 300	
T_C and T_A above 25°C and V_{CE} above 150 V	P_T	See Rating Chart	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Pin-Soldering Temperature (10 s max)	T_P	230	°C

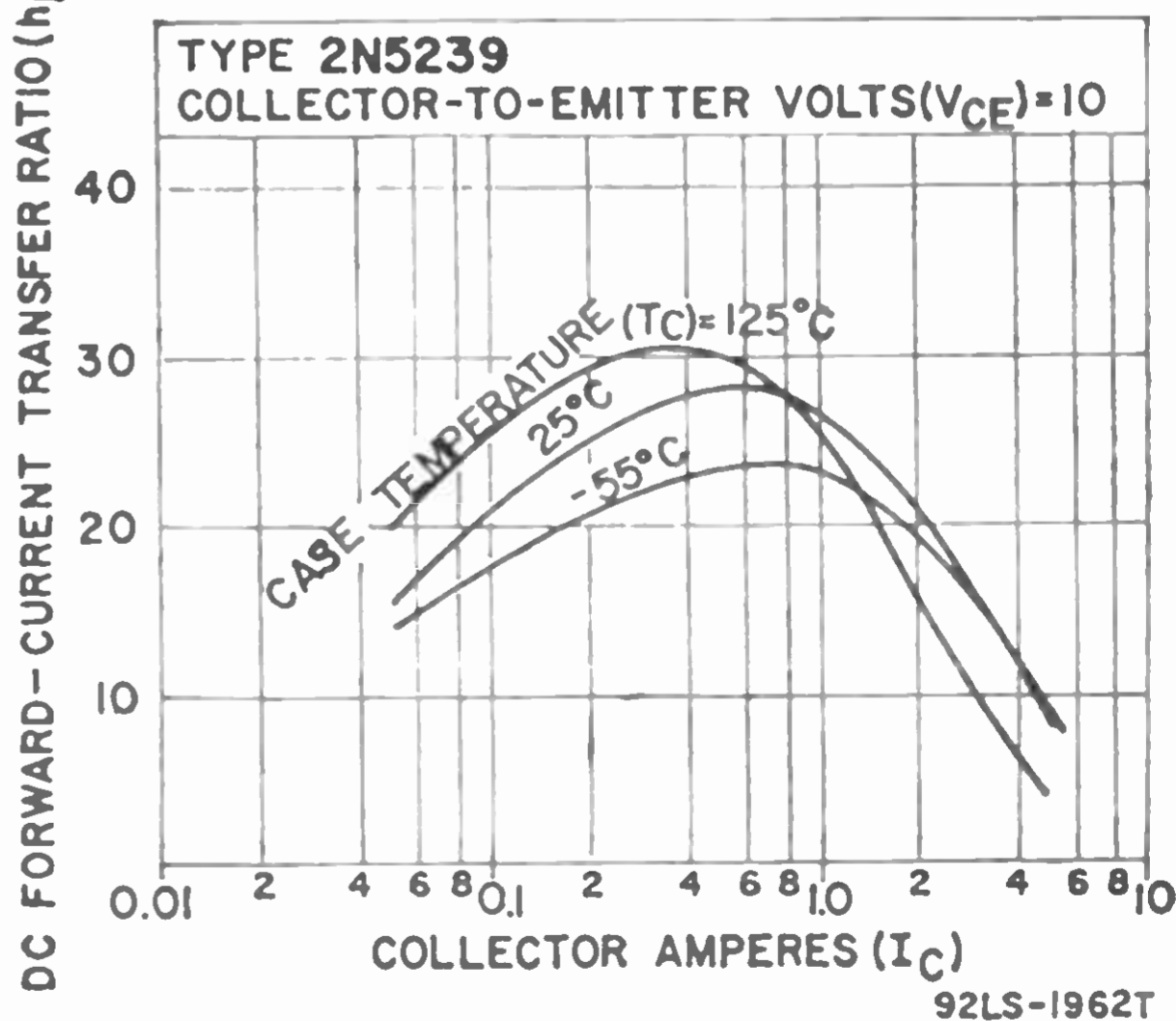
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage:			
$I_C = 0.1 A, I_B = 0$	$V_{CEO(SUS)}$	225 min	V
$I_C = 0.1 A, I_B = 0, R_{BE} = 50 \Omega$	$V_{CER(SUS)}$	250 min	V
Emitter-to-Base Voltage ($I_B = 0.02 A$)	V_{EBO}	6 min	V
Base-to-Emitter Voltage			
($V_{CE} = 10 V, I_C = 2 A, t_P \leq 350 \mu s, df = 2\%$)	V_{BE}	3 max	V
Collector-to-Emitter Saturation Voltage			
($I_C = 2 A, I_B = 0.25 A, t_P \leq 350 \mu s, df = 2\%$)	$V_{CE(sat)}$	2.5 max	V
Collector-Cutoff Current:			
$V_{CE} = 200 V, I_B = 0$	I_{CEO}	5 max	mA
$V_{CE} = 300 V, V_{BE} = -1.5 V$	I_{CEV}	4 max	mA
$V_{CE} = 300 V, V_{BE} = -1.5 V, T_C = 150^\circ C$	I_{CEV}	5 max	mA
Emitter-Cutoff Current ($V_{EB} = 5 V, I_C = 0$)	I_{EBO}	5 max	mA

MAXIMUM OPERATING AREAS



TYPICAL DC FORWARD CURRENT TRANSFER-RATIO CHARACTERISTICS

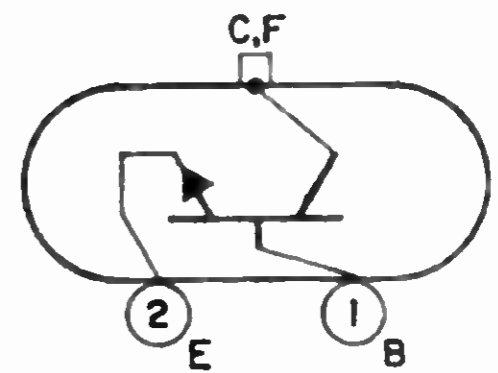


CHARACTERISTICS (cont'd)

Pulsed Static Forward-Current Transfer Ratio:			
$V_{CE} = 10\text{ V}, I_C = 0.4\text{ A}, t_P \leq 350\ \mu\text{s}, df = 2\%$	$h_{FE}(\text{pulsed})$	20 to 80	
$V_{CE} = 10\text{ V}, I_C = 2\text{ A}, t_P \leq 350\ \mu\text{s}, df = 2\%$	$h_{FE}(\text{pulsed})$	20 min	
Output Capacitance ($V_{CB} = 10\text{ V}, I_C = 0, f = 1\text{ MHz}$)	C_{obo}	150 max	pF
Second-Breakdown Collector Current ($V_{CE} = 150\text{ V}$, non-repetitive pulse = 1 s, base forward-biased)	$I_{S/b}$	0.67 min	A
Second-Breakdown Energy ($V_{EB} = 4\text{ V}, I_C = 4\text{ A}, R_B = 50\ \Omega, L = 0.5\text{ mH}$, base reverse-biased)	$E_{S/b}$	4 min	mJ
Gain-Bandwidth Product ($V_{CE} = 10\text{ V}, I_C = 0.2\text{ A}, f = 1\text{ MHz}$)	f_T	5 min	MHz
Thermal Resistance, Junction-to-Case	θ_{J-C}	1.75 max	$^{\circ}\text{C/W}$

2N5240 POWER TRANSISTOR

Si n-p-n multiple epitaxial type used for high-voltage, high-power in linear applications in industrial and commercial service. JEDEC TO-3, Outline No.2. See Mounting Hardware for desired mounting arrangement. This type is identical with type 2N5239 except for the following items:



MAXIMUM RATINGS

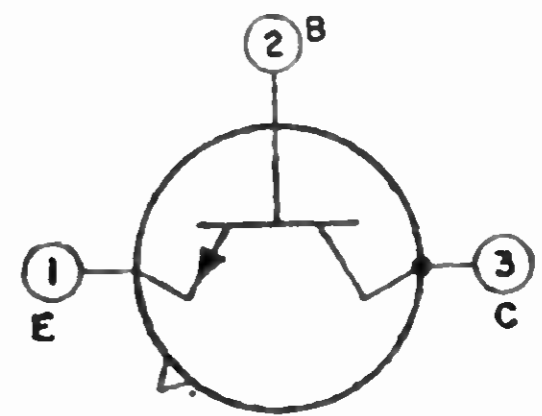
Collector-to-Base Voltage	V_{CBO}	375	V
Collector-to-Emitter Sustaining Voltage: $R_{BE} \leq 50\ \Omega$	$V_{CER}(\text{sus})$	350	V
Base open	$V_{CEO}(\text{sus})$	300	V

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage:			
$I_C = 0.1\text{ A}, I_B = 0$	$V_{CEO}(\text{sus})$	300	V
$I_C = 0.1\text{ A}, I_B = 0, R_{BE} = 50\ \Omega$	$V_{CER}(\text{sus})$	350	V
Collector-Cutoff Current:			
$V_{CE} = 200\text{ V}, I_B = 0$	I_{CEO}	2 max	mA
$V_{CE} = 375\text{ V}, V_{BE} = -1.5\text{ V}$	I_{CEV}	2 max	mA
$V_{CE} = 300\text{ V}, V_{BE} = -1.5\text{ V}, T_C = 150^{\circ}\text{C}$	I_{CEV}	3 max	mA
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}, I_C = 0$)	I_{EBO}	1 max	mA

2N5262 COMPUTER TRANSISTOR

Si n-p-n epitaxial planar type used for high-speed, high-voltage, high-current switching applications for memory driver service in data-processing equipment and other critical industrial applications. Outline No.58.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	75	V
Collector-to-Emitter Voltage	V_{CEO}	50	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	2	A
Peak Collector Current	i_C	3	A
Transistor Dissipation:			
T_C up to 25°C	P_T	5	W
T_C above 25°C	P_T	Derate at 28.5	mW/ $^{\circ}\text{C}$
T_A up to 25°C	P_T	1	W
T_A above 25°C	P_T	Derate at 5.7	mW/ $^{\circ}\text{C}$
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 200	$^{\circ}\text{C}$
Storage	T_{STG}	-65 to 200	$^{\circ}\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	265	$^{\circ}\text{C}$

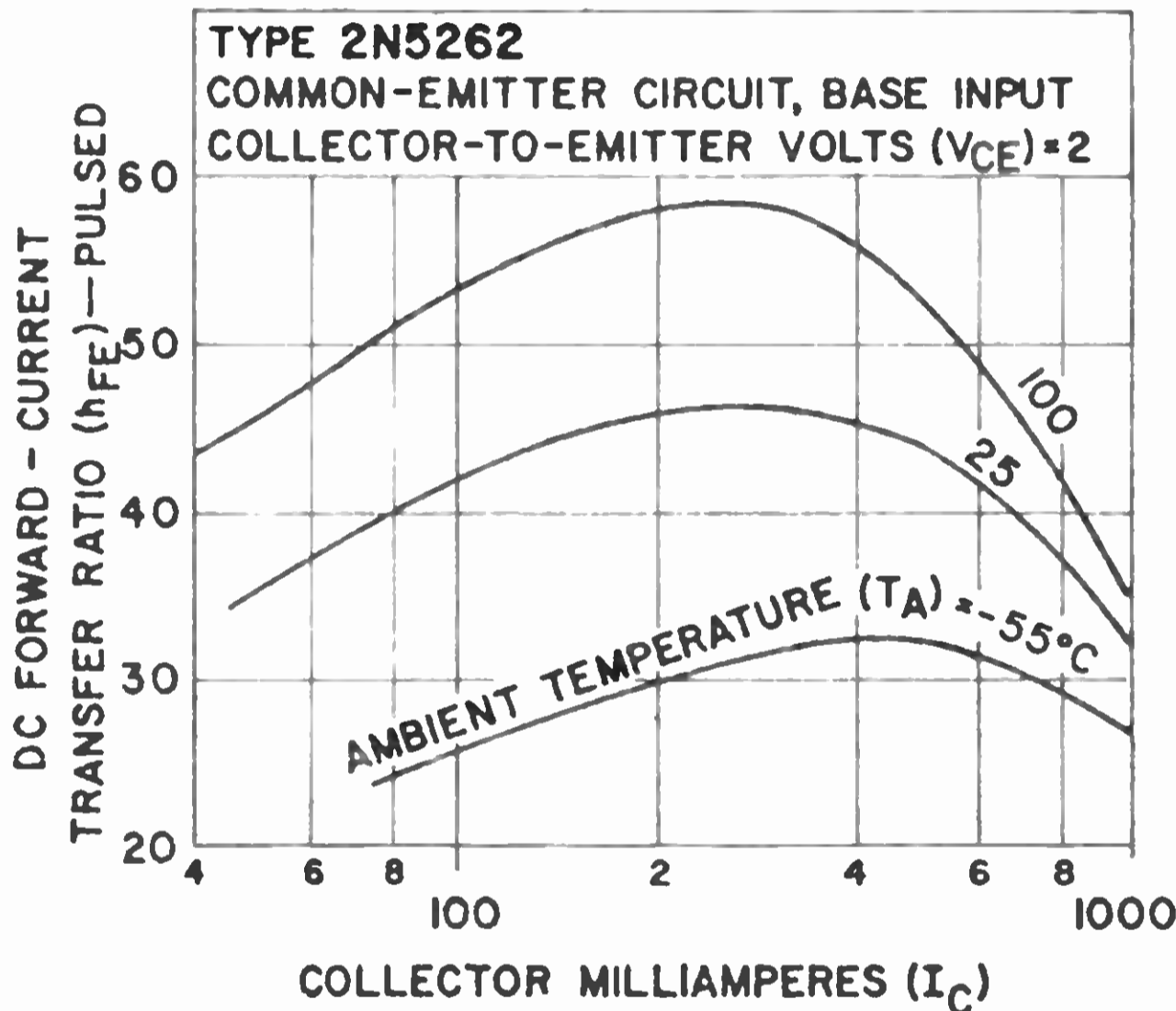
CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = 0.1\text{ mA}$)	$V_{(BR)CBO}$	75 min; 110 typ	V
Collector-to-Emitter Breakdown Voltage ($I_C = 10\text{ mA}$)	$V_{(BR)CEO}$	50 min; 56 typ	V

CHARACTERISTICS (cont'd)

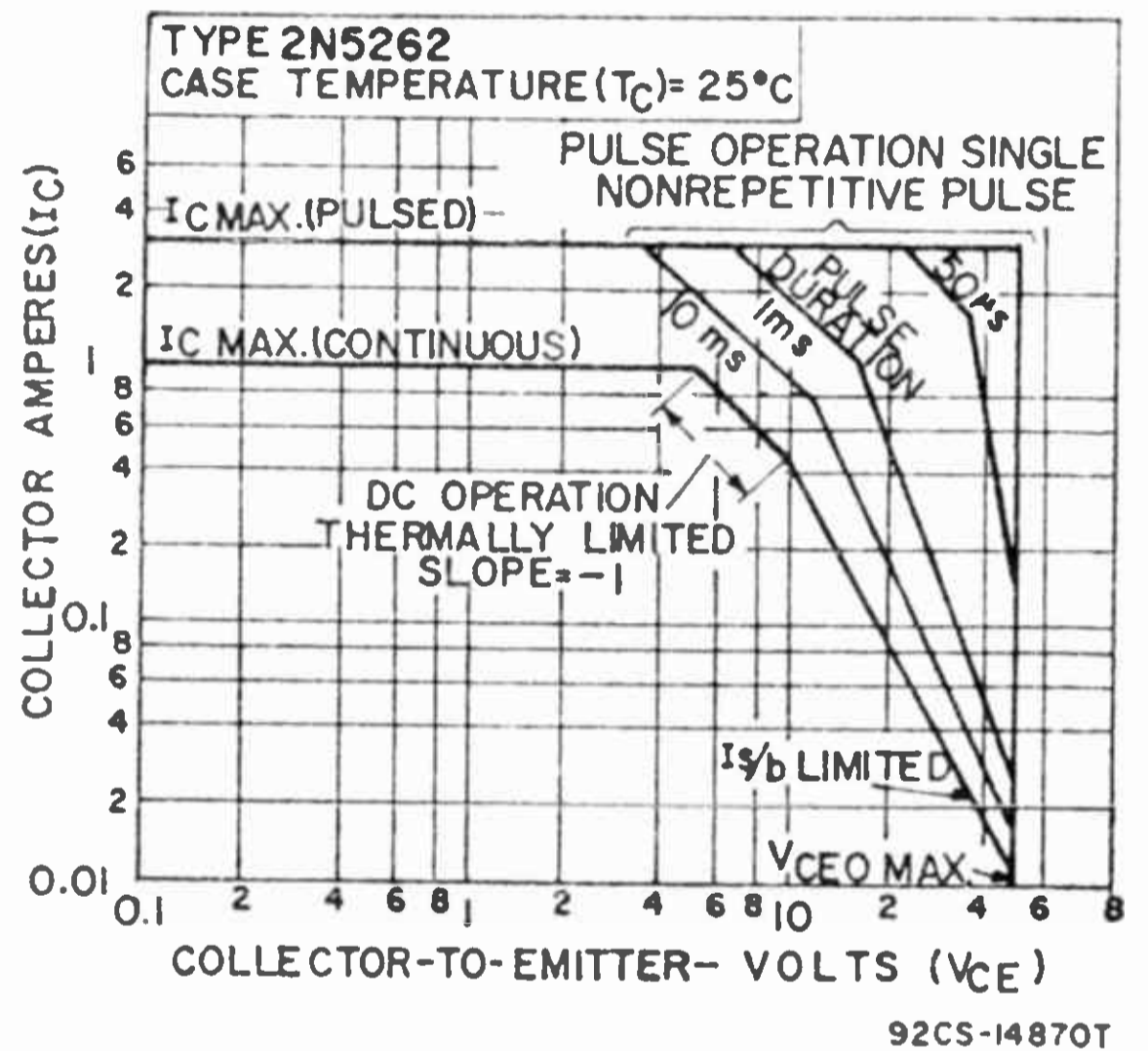
Emitter-to-Base Breakdown Voltage ($I_E = -0.1$ mA)	$V_{(BR)EBO}$	5 min; 8 typ	V
Collector-to-Emitter Saturation Voltage ($I_C = 1000$ mA, $I_B = 100$ mA)	$V_{CE(sat)}$	0.5 typ; 0.8 max	V
Base-to-Emitter Saturation Voltage ($I_C = 1000$ mA, $I_B = 100$ mA)	$V_{BE(sat)}$	1 typ; 1.4 max	V
Collector-Cutoff Current:			
$V_{CE} = 60$ V	I_{CES}	10 max	μA
$V_{CE} = 30$ V	I_{CES}	0.4 typ; 1 max	μA
$V_{CE} = 30$ V, $T_A = 100^\circ C$	I_{CES}	100 max	μA
Static Forward Current Transfer Ratio:			
$V_{CE} = 1$ V, $I_C = 100$ mA	h_{FE}	35 min; 55 typ	
$V_{CE} = 1$ V, $I_C = 500$ mA	h_{FE}	40 min; 65 typ	
$V_{CE} = 1$ V, $I_C = 1000$ mA, $t_P \leq 400$ μs , $df \leq 0.03$	$h_{FE(pulsed)}$	25 min; 45 typ	
Small-Signal Forward Current Transfer Ratio ($V_{CE} = 10$ V, $I_C = 50$ mA, $f = 100$ MHz)	h_{fe}	2.5 min; 3.5 typ	
Output Capacitance ($V_{CB} = 10$ V, $I_E = 0$, $f = 0.1$ to 1 MHz)	C_{obo}	9 typ; 12 max	pF
Turn-On Time ($I_C = 1000$ mA, $I_{B1} = 100$ mA)	$t_d + t_r$	18 min; 30 max	ns
Turn-Off Time ($I_C = 1000$ mA, $I_{B1} = 100$ mA, $I_{B2} = -100$ mA)	$t_s + t_f$	35 typ; 60 max	ns

TYPICAL DC FORWARD CURRENT TRANSFER-RATIO CHARACTERISTICS



92CS-13902T

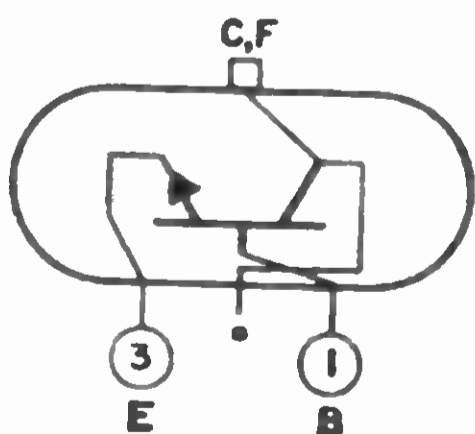
MAXIMUM OPERATING AREAS



92CS-14870T

POWER TRANSISTOR

2N5293



Si n-p-n type featuring a base comprised of a homogeneous-resistivity silicon material and molded silicone plastic package with vertical leads. This type fits a standard TO-66 socket. It is used in a wide variety of medium-power switching and amplifier applications such as series and shunt regulators, and in driver and output stages of high-fidelity amplifiers. Outline No.52. See Mounting Hardware for desired mounting arrangement.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	80	V
Collector-to-Emitter Sustaining Voltage:			
$V_{BE} = -1.5$ V	$V_{CEV(SUS)}$	80	V
$R_{BE} = 100$ Ω	$V_{CER(SUS)}$	75	V
Base open	$V_{CEO(SUS)}$	70	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Collector Current	I_C	4	A
Base Current	I_B	2	A

MAXIMUM RATINGS (cont'd)

Transistor Dissipation:

T_C up to 25°C	P_T	36	W
T_A up to 25°C	P_T	1.8	W
T_C above 25°C	P_T	Derate linearly at 0.288 W/°C	
T_A above 25°C	P_T	Derate linearly at 0.0144 W/°C	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 150	°C
Storage	T_{STG}	-65 to 150	°C
Lead-Soldering Temperature (10 s max)	T_L	235	°C

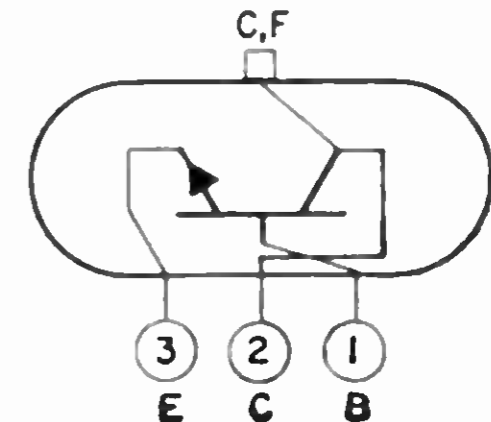
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage:

$I_C = 0.1$ A, $I_B = 0$, $t_P = 300$ μ s, $df = 0.018$	V_{CEO} (sus)	70 min	V
$I_C = 0.1$ A, $t_P = 300$ μ s, $df = 0.018$	V_{CER} (sus)	75 min	V
$V_{BE} = -1.5$ V, $I_C = 0.1$ A, $t_P = 300$ μ s, $df = 0.018$	V_{CEV} (sus)	80 min	V
Base-to-Emitter Voltage ($V_{CE} = 4$ V, $I_C = 0.5$ A, $t_P = 300$ μ s, $df = 0.018$)	V_{BE}	1.1 max	V
Collector-to-Emitter Saturation Voltage ($I_C = 0.5$ A, $I_B = 0.05$ A, $t_P = 300$ μ s, $df = 0.018$)	V_{CE} (sat)	1 max	V
Collector-Cutoff Current:			
$V_{CE} = 65$ V, $V_{BE} = -1.5$ V	I_{CEV}	0.5 max	mA
$V_{CE} = 65$ V, $V_{BE} = -1.5$ V, $T_C = 150^\circ$ C	I_{CEV}	3 max	mA
$V_{CE} = 50$ V, $R_{BE} = 100$ Ω	I_{CER}	0.5 max	mA
$V_{CE} = 50$ V, $R_{BE} = 100$ Ω , $T_C = 150^\circ$ C	I_{CER}	2 max	mA
Emitter-Cutoff Current ($V_{EB} = 7$ V)	I_{EBO}	1 max	mA
Pulsed Static Forward-Current Transfer Ratio			
($V_{CE} = 4$ V, $I_C = 0.5$ A, $t_P = 300$ μ s, $df = 0.018$)	h_{FE} (pulsed)	30 to 120	
Gain-Bandwidth Product ($V_{CE} = 4$ V, $I_C = 0.2$ A)	f_T	0.8 min	MHz
Turn-On Time ($V_{CC} = 30$ V, $I_C = 0.5$ A, $I_{B1} = 0.05$ A)	$t_d + t_r$	5 max	μ s
Turn-Off Time ($V_{CC} = 30$ V, $I_C = 0.5$ A, $I_{B1} = 0.05$ A)	$t_s + t_f$	15 max	μ s
Thermal Resistance, Junction-to-Case	θ_{J-C}	3.5 max	°C/W
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	70 max	°C/W

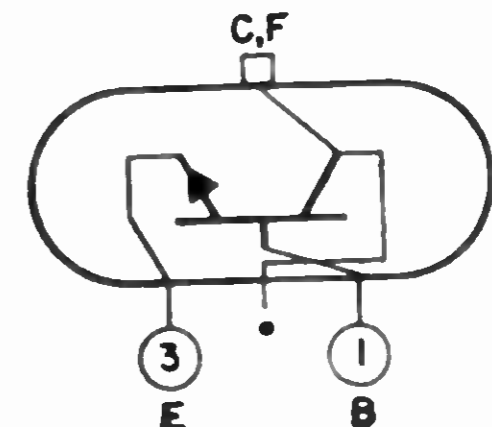
2N5294 POWER TRANSISTOR

Si n-p-n type featuring a base comprised of a homogeneous-resistivity silicon material and molded silicone plastic package having horizontal leads for mounting on printed-circuit boards. It is used in a wide variety of medium-power switching and amplifier applications such as series and shunt regulators, and in driver and output stages of high-fidelity amplifiers. Outline No.53. See Mounting Hardware for desired mounting arrangement. This type is electrically identical to type 2N5293.



2N5295 POWER TRANSISTOR

Si n-p-n type featuring a base comprised of a homogeneous-resistivity silicon material and molded silicone plastic package with vertical leads. This type fits a standard TO-66 socket. It is used in a wide variety of medium-power switching and amplifier applications such as series and shunt regulators, and in driver and output stages of high-fidelity amplifiers. Outline No.52. See Mounting Hardware for desired mounting arrangement.



MAXIMUM RATINGS

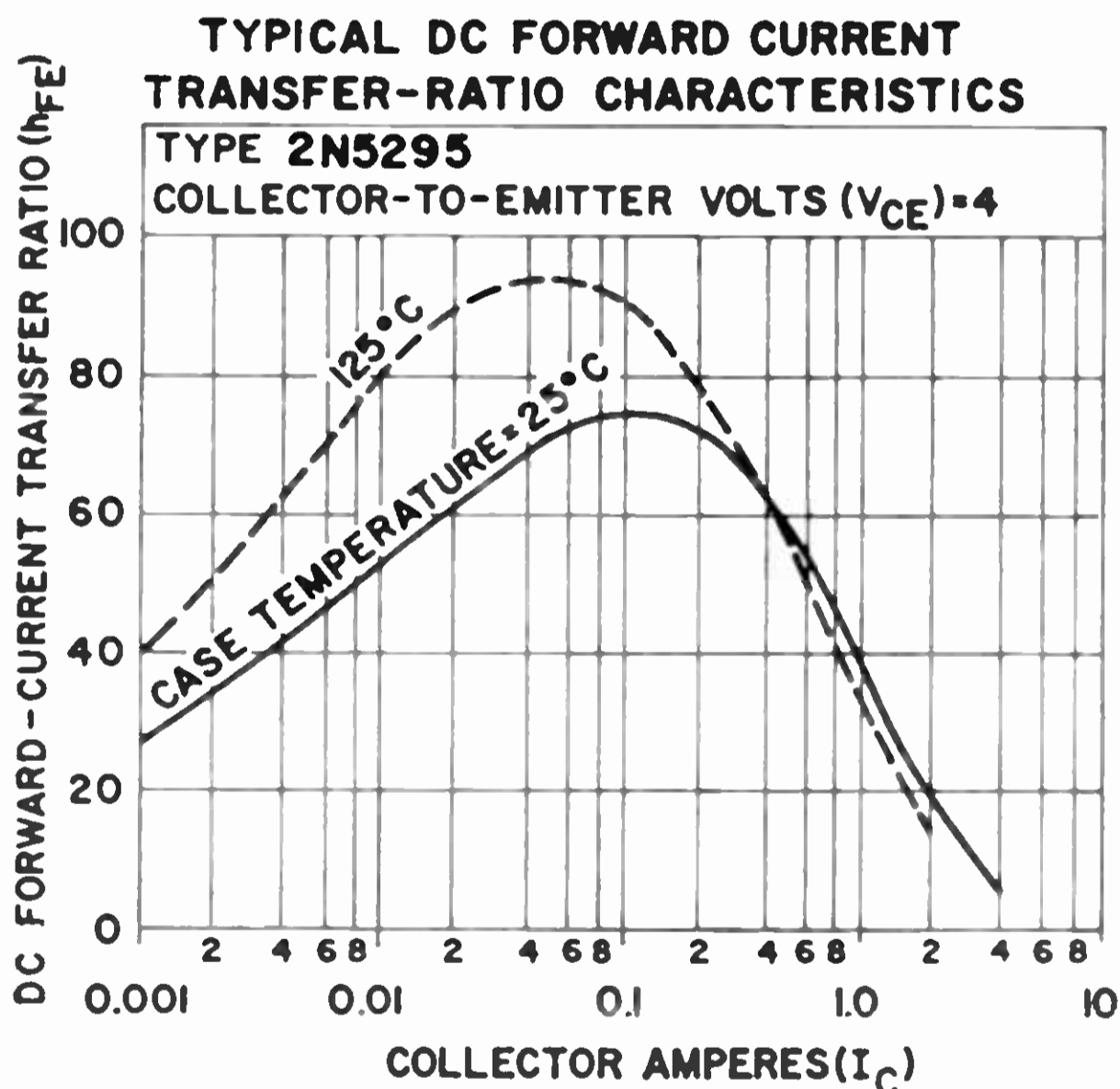
Collector-to-Base Voltage	V_{CBO}	60	V
Collector-to-Emitter Sustaining Voltage:			
$V_{BE} = -1.5$ V	V_{CEV} (sus)	60	V
$R_{BE} = 100$ Ω	V_{CER} (sus)	50	V
Base open	V_{CEO} (sus)	40	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	4	A

CHARACTERISTICS (cont'd)

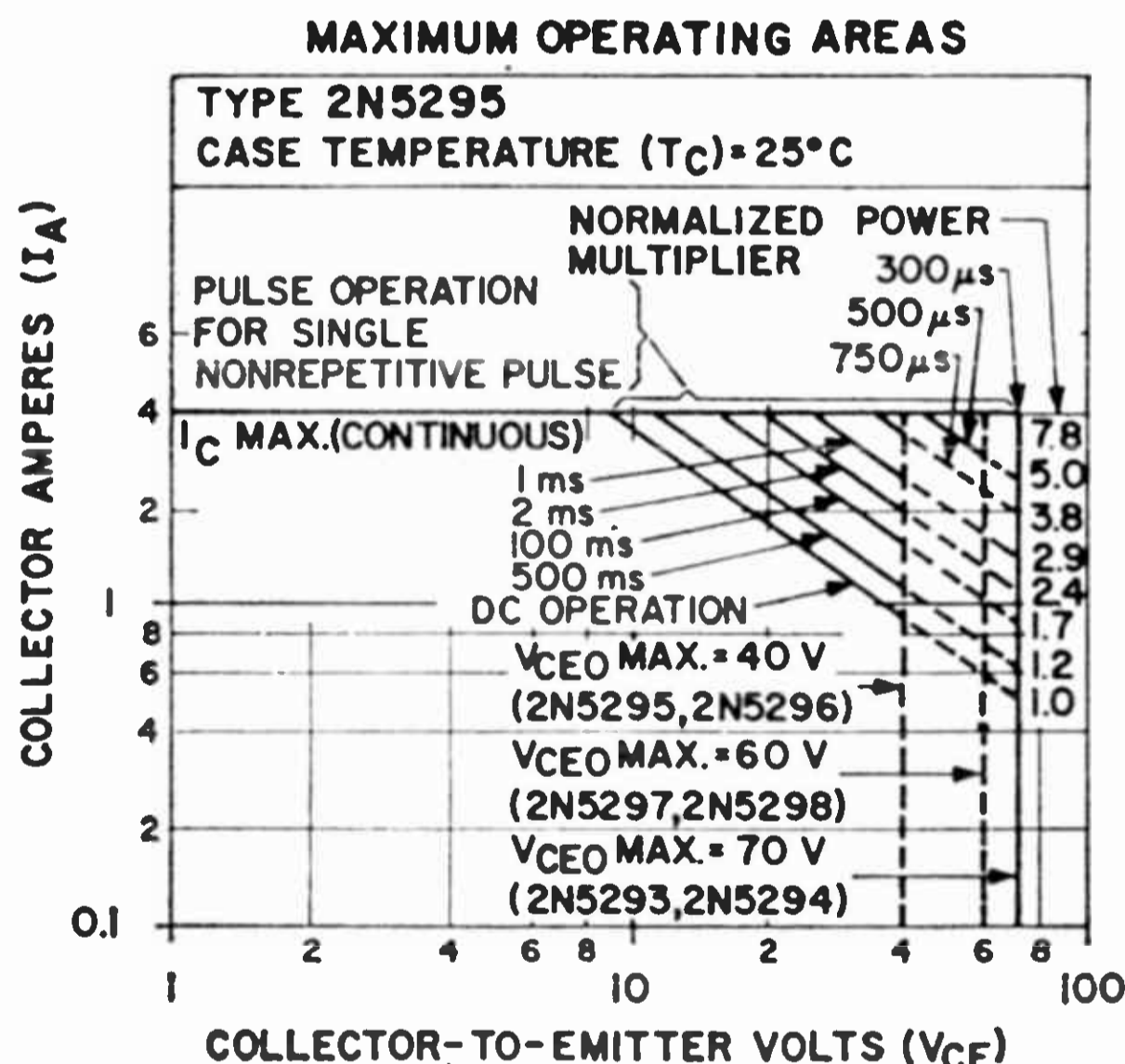
Base Current	I_B	2	A
Transistor Dissipation:			
T_C up to 25°C	P_T	36	W
T_A up to 25°C	P_T	1.8	W
T_C above 25°C	P_T	Derate linearly at 0.288 W/°C	
T_A above 25°C	P_T	Derate linearly at 0.0144 W/°C	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 150	°C
Storage	T_{STG}	-65 to 150	°C
Lead-Soldering Temperature (10 s max)	T_L	235	°C

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage:			
$I_C = 0.1$ A, $I_B = 0$, $t_P = 300$ μ s, $df = 0.018$	V_{CE0} (sus)	40 min	V
$I_C = 0.1$ A, $t_P = 300$ μ s, $df = 0.018$	V_{CER} (sus)	50 min	V
$V_{BE} = -1.5$ V, $I_C = 0.1$ A, $t_P = 300$ μ s, $df = 0.018$	V_{CEV} (sus)	60 min	V
Base-to-Emitter Voltage ($V_{CE} = 4$ V, $I_C = 1$ A, $t_P = 300$ μ s, $df = 0.018$)	V_{BE}	1.3 max	V
Collector-to-Emitter Saturation Voltage ($I_C = 1$ A, $I_B = 0.1$ A, $t_P = 300$ μ s, $df = 0.018$) ...	V_{CE} (sat)	1 max	V
Collector-Cutoff Current:			
$V_{CE} = 35$ V, $V_{BE} = -1.5$ V	I_{CEV}	2 max	mA
$V_{CE} = 35$ V, $V_{BE} = -1.5$ V, $T_C = 150^\circ$ C	I_{CEV}	5 max	mA
Emitter-Cutoff Current ($V_{EB} = 5$ V)	I_{EBO}	1 max	mA
Pulsed Static Forward-Current Transfer Ratio ($V_{CE} = 4$ V, $I_C = 1$ A, $t_P = 300$ μ s, $df = 0.018$) ...	h_{FE} (pulsed)	30 to 120	
Gain-Bandwidth Product ($V_{CE} = 4$ V, $I_C = 0.2$ A)	f_T	0.8 max	MHz
Turn-On Time ($V_{CC} = 30$ V, $I_C = 1$ A, $I_{B1} = 0.1$ A)	$t_d + t_r$	5 max	μ s
Turn-Off Time ($V_{CC} = 30$ V, $I_C = 1$ A, $I_{B2} = -0.1$ A)	$t_s + t_f$	15 max	μ s
Thermal Resistance, Junction-to-Case	θ_{J-C}	3.5 max	°C/W
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	70 max	°C/W



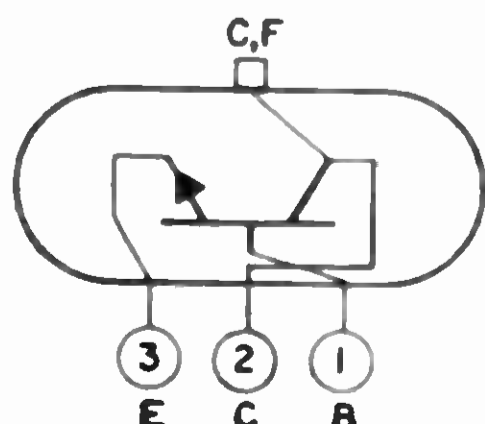
92SS-3732T



92SS-3617T

POWER TRANSISTOR

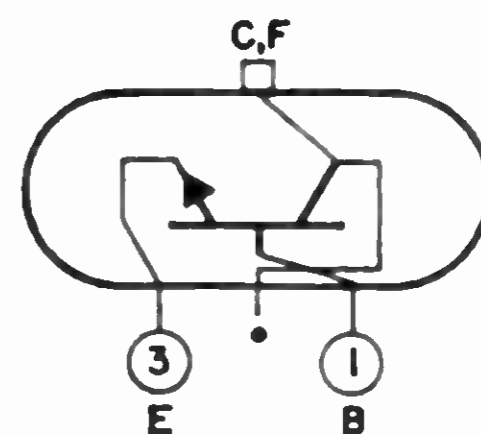
2N5296



Si n-p-n type featuring a base comprised of a homogeneous-resistivity silicon material and molded silicone plastic package having horizontal leads for mounting on printed-circuit boards. It is used in a wide variety of medium-power switching and amplifier applications such as series and shunt regulators, and in driver and output stages of high-fidelity amplifiers. Outline No.53. See Mounting Hardware for desired mounting arrangement. This type is electrically identical to type 2N5295.

2N5297 POWER TRANSISTOR

Si n-p-n type featuring a base comprised of a homogeneous-resistivity silicon material and molded silicone plastic package with vertical leads. This type fits a standard TO-66 socket. It is used in a wide variety of medium-power switching and amplifier applications such as series and shunt regulators, and in driver and output stages of high-fidelity amplifiers. Outline No.52. See Mounting Hardware for desired mounting arrangement.



MAXIMUM RATINGS

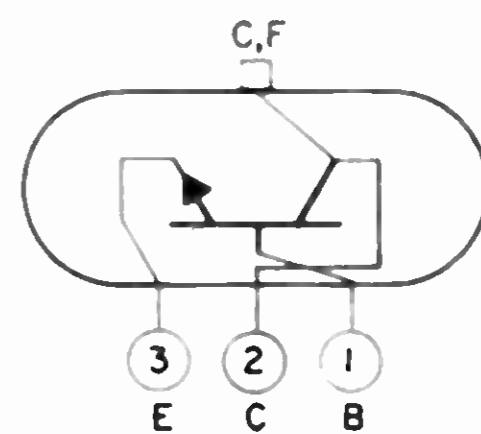
Collector-to-Base Voltage	V_{CBO}	80	V
Collector-to-Emitter Sustaining Voltage: $V_{BE} = -1.5$ V	$V_{CEV(SUS)}$	80	V
$R_{BE} = 100$ Ω	$V_{CER(SUS)}$	70	V
Base open	$V_{CEO(SUS)}$	60	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	4	A
Base Current	I_B	2	A
Transistor Dissipation:			
T_C up to 25°C	P_T	36	W
T_A up to 25°C	P_T	1.8	W
T_C above 25°C	P_T Derate linearly at 0.228	W/°C	
T_A above 25°C	P_T Derate linearly at 0.0144	W/°C	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 150	°C
Storage	T_{STG}	-65 to 150	°C
Lead-Soldering Temperature (10 s max)	T_L	235	°C

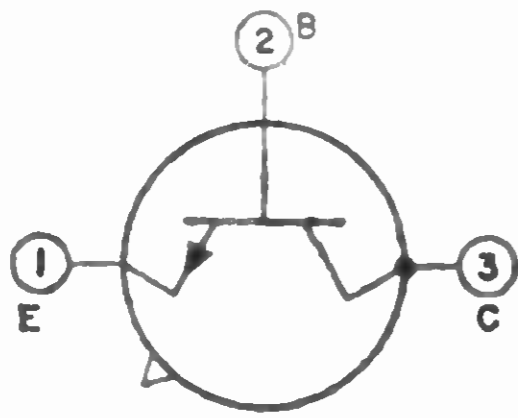
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage: $I_C = 0.1$ A, $I_B = 0$, $t_P = 300$ μ s, $df = 0.018$	$V_{CEO(SUS)}$	60 min	V
$I_C = 0.1$ A, $t_P = 300$ μ s, $df = 0.018$	$V_{CER(SUS)}$	70 min	V
$V_{BE} = -1.5$ V, $I_C = 0.1$ A, $t_P = 300$ μ s, $df = 0.018$	$V_{CEV(SUS)}$	80 min	V
Base-to-Emitter Voltage ($V_{CE} = 4$ V, $I_C = 1.5$ A, $t_P = 300$ μ s, $df = 0.018$)	V_{BE}	1.5 max	V
Collector-to-Emitter Saturation Voltage ($I_C = 1.5$ A, $I_B = 0.15$ A, $t_P = 300$ μ s, $df = 0.018$)	$V_{CE(sat)}$	1 max	V
Collector-Cutoff Current:			
$V_{CE} = 65$ V, $V_{BE} = -1.5$ V	I_{CEV}	0.5 max	mA
$V_{CE} = 65$ V, $V_{BE} = -1.5$ V, $T_C = 150^\circ$ C	I_{CEV}	3 max	mA
$V_{CE} = 50$ V, $R_{BE} = 100$ Ω	I_{CER}	0.5 max	mA
$V_{CE} = 50$ V, $R_{BE} = 100$ Ω , $T_C = 150^\circ$ C	I_{CER}	2 max	mA
Emitter-Cutoff Current ($V_{EB} = 5$ V)	I_{EBO}	1 max	mA
Pulsed-Cutoff Current Transfer Ratio ($V_{CE} = 4$ V, $I_C = 1.5$ A, $t_P = 300$ μ s, $df = 0.018$)	$h_{FE}(pulsed)$	20 to 80	
Gain-Bandwidth Product ($V_{CE} = 4$ V, $I_C = 0.2$ A)	f_T	0.8 min	MHz
Turn-On Time ($V_{CC} = 30$ V, $I_C = 1.5$ A, $I_{B1} = 0.15$ A)	$t_d + t_r$	5 max	μ s
Turn-Off Time ($V_{CC} = 30$ V, $I_C = 1.5$ A, $I_{B2} = -0.15$ A)	$t_s + t_r$	15 max	μ s
Thermal Resistance, Junction-to-Case	θ_{J-C}	3.5 max	°C/W
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	70 max	°C/W

2N5298 POWER TRANSISTOR

Si n-p-n type featuring a base comprised of a homogeneous-resistivity silicon material and molded silicone plastic package having horizontal leads for mounting on printed-circuit boards. It is used in a wide variety of medium-power switching and amplifier applications such as series and shunt regulators, and in driver and output stages of high-fidelity amplifiers. Outline No.53. See Mounting Hardware for desired mounting arrangement. This type is electrically identical to type 2N5297.





POWER TRANSISTOR

2N5320

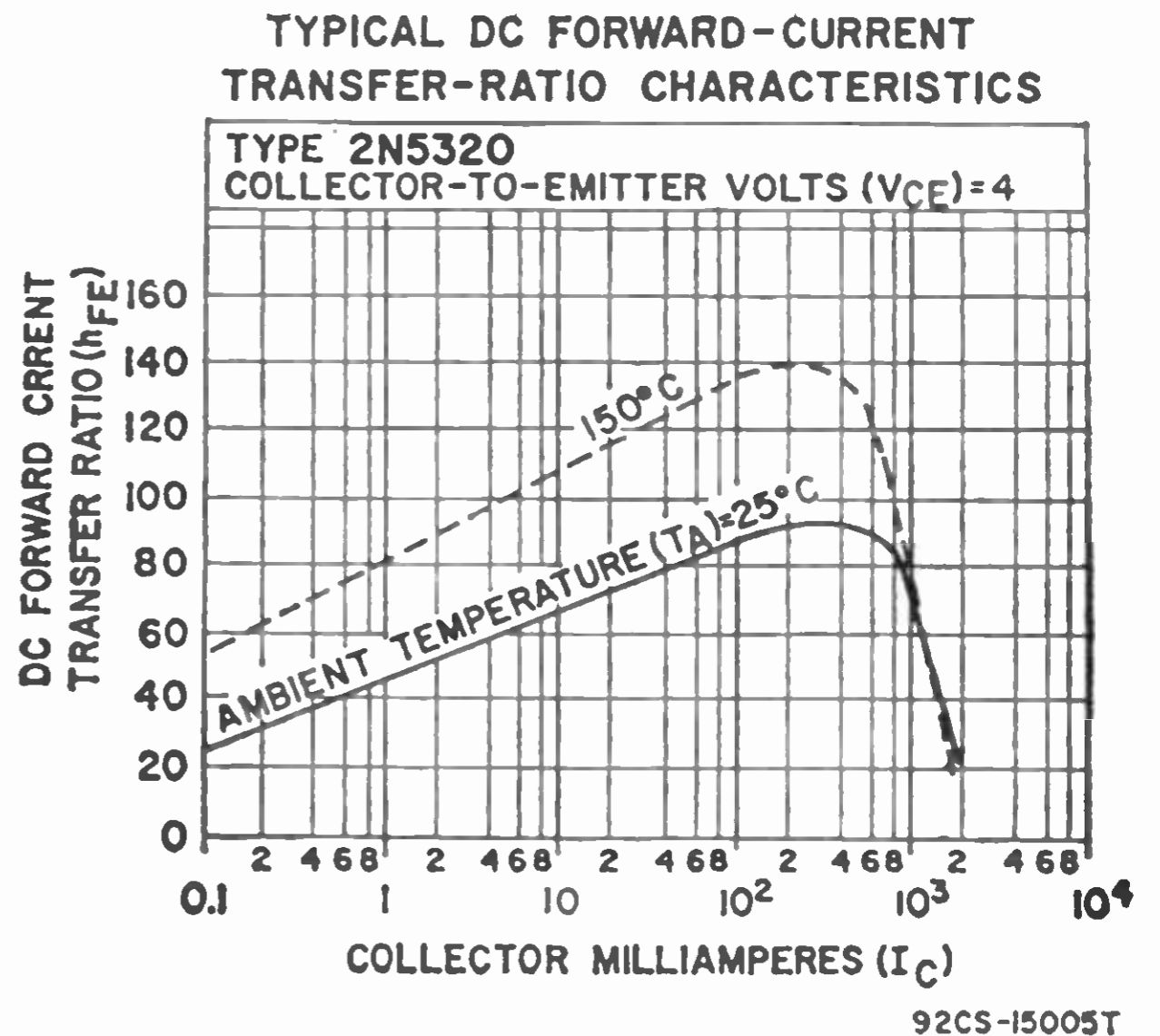
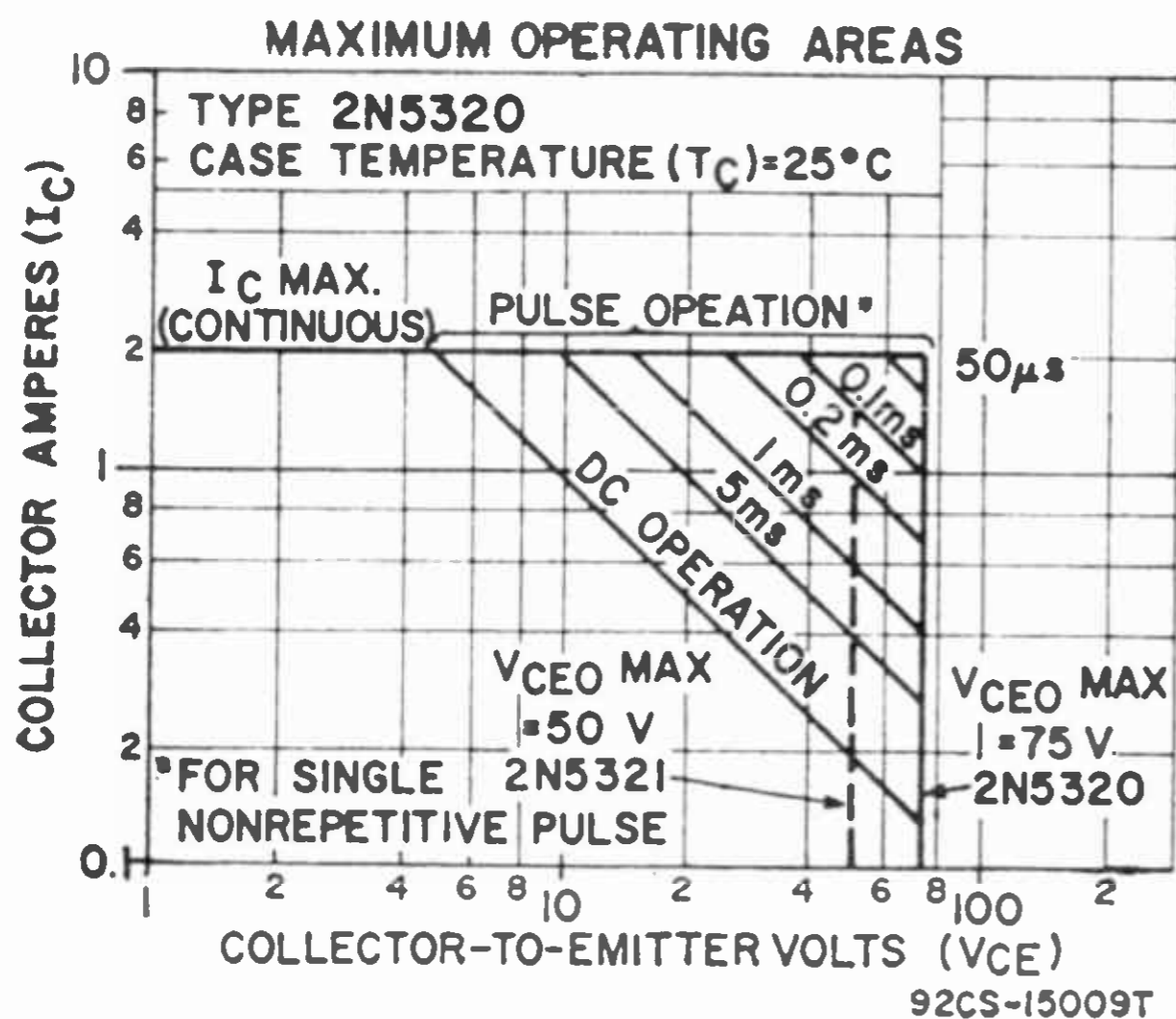
Si n-p-n triple-diffused planar type used for small-signal medium-power applications in military, industrial, and commercial equipment. JEDEC TO-5, Outline No.5.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	100	V
Collector-to-Emitter Sustaining Voltage:			
$V_{BE} = 1.5$ V	$V_{CEV(SUS)}$	100	V
$R_{BE} = 100$ Ω	$V_{CER(SUS)}$	90	V
Base open	$V_{CEO(SUS)}$	75	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Collector Current	I_C	2	A
Base Current	I_B	1	A
Transistor Dissipation:			
T_c up to 25°C	P_T	10	W
T_c above 25°C	P_T	Derate linearly at 0.057 W/°C	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	230	°C

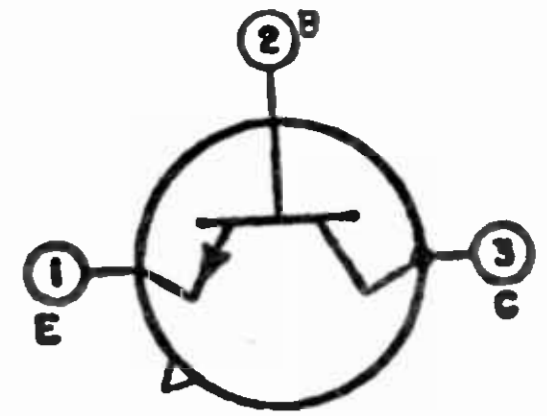
CHARACTERISTICS (At case temperature = 25°C)

Emitter-to-Base Breakdown Voltage ($I_E = 0.1$ mA, $I_C = 0$)	$V_{(BR)EBO}$	7 min	V
Collector-to-Emitter Breakdown Voltage ($V_{BE} = -1.5$ V, $I_C = 0.1$ mA, Base-emitter reverse biased)	$V_{(BR)CEV}$	100 min	V
Collector-to-Emitter Sustaining Voltage: $I_C = 100$ V, $R_{BE} = 100$ Ω	$V_{CER(SUS)}$	90 min	V
$I_C = 100$ V, $I_B = 0$, base open	$V_{CEO(SUS)}$	75 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 500$ mA, $I_B = 50$ mA)	$V_{CE(sat)}$	0.5 max	V
Base-to-Emitter Voltage ($V_{CE} = 4$ V, $I_C = 500$ mA)	V_{BE}	1.1 max	V
Collector-Cutoff Current ($V_{CB} = 80$ V, $I_E = 0$)	I_{CBO}	0.5 max	μ A
Emitter-Cutoff Current ($V_{EB} = 5$ V, $I_C = 0$)	I_{EBO}	0.5 max	μ A
Pulsed Static Forward-Current Transfer Ratio: $V_{CE} = 4$ V, $I_C = 500$ mA, $t_P \leq 300$ μ s, $df \leq 0.02$	$h_{FE}(pulsed)$	30 to 130	
$V_{CE} = 2$ V, $I_C = 1000$ mA, $t_P \leq 300$ μ s, $df \leq 0.02$	$h_{FE}(pulsed)$	10 min	
Gain-Bandwidth Product ($V_{CE} = 4$ V, $I_C = 50$ mA)	f_T	50 min	MHz
Second-Breakdown Collector Current ($V_{CE} = 50$ V, base forward-biased, non-repetitive pulse = 1 s)	$I_{S/b}$	200 min	mA
Turn-On Time ($V_{CE} = 30$ V, $I_C = 500$ mA, $I_B = 50$ mA)	$t_d + t_r$	80 max	ns
Turn-Off Time ($V_{CE} = 30$ V, $I_C = 500$ mA, $I_B = 50$ mA)	$t_s + t_f$	800 max	ns
Thermal Resistance, Junction-to-Case	θ_{J-C}	17.5 max	°C/W
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	150 max	°C/W



2N5321 POWER TRANSISTOR

Si n-p-n triple-diffused planar type used for small-signal medium-power applications in military, industrial, and commercial equipment. JEDEC TO-5, Outline No.5.



MAXIMUM RATINGS

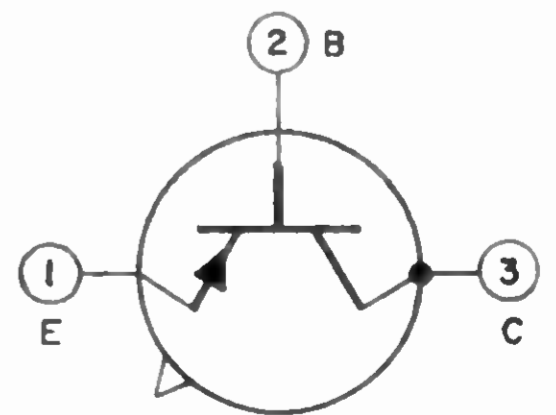
Collector-to-Base Voltage	V_{CBO}	75	V
Collector-to-Emitter Sustaining Voltage:			
$V_{BE} = 1.5$ V	$V_{CEV(sus)}$	75	V
$R_{BE} = 100$ Ω	$V_{CER(sus)}$	65	V
Base open	$V_{CEO(sus)}$	50	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	2	A
Base Current	I_B	1	A
Transistor Dissipation:			
T_c up to 25°C	P_T	10	
T_c above 25°C	P_T	Derate linearly at 0.057 W/°C	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	230	°C

CHARACTERISTICS (At case temperature = 25°C)

Emitter-to-Base Breakdown Voltage ($I_E = 0.1$ mA, $I_C = 0$)	$V_{(BR)EBO}$	5 min	V
Collector-to-Emitter Breakdown Voltage ($V_{BE} = -1.5$ V, $I_C = 0.1$ mA, Base-emitter reverse biased)	$V_{(BR)CEV}$	75 min	V
Collector-to-Emitter Sustaining Voltage:			
$I_C = 100$ mA, $R_{BE} = 100$ Ω	$V_{CER(sus)}$	65 min	V
$I_C = 100$ mA, base open	$V_{CEO(sus)}$	50 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 500$ mA, $I_B = 50$ mA)	$V_{CE(sat)}$	0.8 max	V
Base-to-Emitter Voltage ($V_{CE} = 4$ V, $I_C = 500$ mA) ...	V_{BE}	1.4 max	V
Collector-Cutoff Current ($V_{CB} = 60$ V, $I_E = 0$)	I_{CBO}	5 max	μ A
Emitter-Cutoff Current ($V_{EB} = 4$ V, $I_C = 0$)	I_{EBO}	0.5 max	μ A
Pulsed Static Forward-Current Transfer Ratio ($V_{CE} = 4$ V, $I_C = 500$ mA, $t_P \leq 300$ μ s, $df \leq 0.02$) ...	$h_{FE}(pulsed)$	40 to 250	
Gain-Bandwidth Product ($V_{CE} = 4$ V, $I_C = 50$ mA) ...	f_T	50 min	MHz
Second-Breakdown Collector Current ($V_{CE} = 50$ V, base forward-biased, non-repetitive pulse = 1 s)	$I_{S/b}$	200 min	mA
Turn-On Time ($V_{CE} = 30$ V, $I_C = 500$ mA, $I_B = 50$ mA)	$t_d + t_r$	80 max	ns
Turn-Off Time ($V_{CE} = 30$ V, $I_C = 500$ mA, $I_B = 50$ mA)	$t_s + t_f$	800 max	ns
Thermal Resistance, Junction-to-Case	θ_{J-C}	17.5 max	°C/W
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	150 max	°C/W

2N5322 POWER TRANSISTOR

Si p-n-p double-diffused epitaxial-planar type used for small-signal medium-power applications in military, industrial, and commercial equipment. The p-n-p construction permits complementary operation with a matching n-p-n type such as the 2N5320. JEDEC TO-5, Outline No.5.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-100	V
Collector-to-Emitter Sustaining Voltage:			
$V_{BE} = 1.5$ V	$V_{CEV(sus)}$	-100	V
$R_{BE} = 100$ Ω	$V_{CER(sus)}$	-90	V
Base open	$V_{CEO(sus)}$	-75	V
Emitter-to-Base Voltage	V_{EBO}	-7	V
Collector Current	I_C	-2	A

MAXIMUM RATINGS (cont'd)

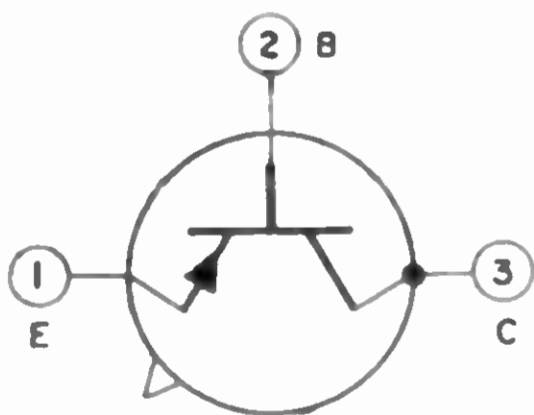
Base Current	I_B	-1	A
Transistor Dissipation:	P_T	10	W
T_c up to 25°C	P_T	Derate linearly at 0.057 W/°C	
T_c above 25°C			
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	230	°C

CHARACTERISTICS (At case temperature = 25°C)

Emitter-to-Base Breakdown Voltage ($I_E = -0.1$ mA, $I_C = 0$)	$V_{(BR)EBO}$	-7 min	V
Collector-to-Emitter Breakdown Voltage ($V_{BE} = 1.5$ V, $I_C = -0.1$ mA, Base-emitter reversed biased)	$V_{(BR)CEV}$	-100 min	V
Collector-to-Emitter Sustaining Voltage: $I_C = -100$ mA, $R_{BE} = 100 \Omega$	$V_{CER}(SUS)$	-90 min	V
$I_C = -100$ mA, $I_B = 0$, base open	$V_{CEO}(SUS)$	-75 min	V
Collector-to-Emitter Saturation Voltage ($I_C = -500$ mA, $I_B = -50$ mA)	$V_{CE}(sat)$	-0.7 min	V
Base-to-Emitter Voltage ($V_{CE} = -4$ V, $I_C = -500$ mA)	V_{BE}	-1.1 max	V
Collector-Cutoff Current ($V_{CB} = -80$ V, $I_E = 0$)	I_{CBO}	-0.5 max	μA
Emitter-Cutoff Current ($V_{EB} = -5$ V, $I_C = 0$)	I_{EBO}	-0.1 max	μA
Pulsed Static Forward-Current Transfer Ratio: $V_{CE} = -4$ V, $I_C = -500$ mA, $t_P \leq 300 \mu s$, $df \leq 0.02$	$h_{FE}(pulsed)$	30 to 130	
$V_{CE} = -2$ V, $I_C = -1000$ mA, $t_P \leq 300 \mu s$, $df \leq 0.02$	$h_{FE}(pulsed)$	10 min	
Gain-Bandwidth Product ($V_{CE} = -4$ V, $I_C = -50$ mA)	f_T	50	MHz
Second-Breakdown Collector Current ($V_{CE} = -35$ V, base forward-biased)	$I_{S/b}$	-285	mA
Turn-On Time ($V_{CE} = -30$ V, $I_C = -500$ mA, $I_B = -50$ mA)	$t_d + t_r$	100 max	ns
Turn-Off Time ($V_{CE} = -30$ V, $V_{BE} = -500$ mA, $I_E = -50$ mA)	$t_s + t_f$	1000 max	ns
Thermal Resistance, Junction-to-Case	θ_{J-C}	17.5 max	°C/W
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	150 max	°C/W

POWER TRANSISTOR

2N5323



Si p-n-p double-diffused epitaxial-planar type used for small-signal medium-power applications in military, industrial, and commercial equipment. The p-n-p construction permits complementary operation with a matching n-p-n type such as the 2N5321. JEDEC TO-5, Outline No.5.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-75	V
Collector-to-Emitter Sustaining Voltage $V_{BE} = 1.5$ V	$V_{(CEV)}(SUS)$	-75	V
$R_{BE} = 100 \Omega$	$V_{(CER)}(SUS)$	-65	V
Base open	$V_{CEO}(SUS)$	-50	V
Emitter-to-Base Voltage	V_{EBO}	-5	V
Collector Current	I_C	-2	A
Base Current	I_B	-1	A
Transistor Dissipation:	P_T	10	W
T_c up to 25°C	P_T	Derate linearly at 0.057 W/°C	
T_c above 25°C			
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	230	°C

CHARACTERISTICS (At case temperature = 25°C)

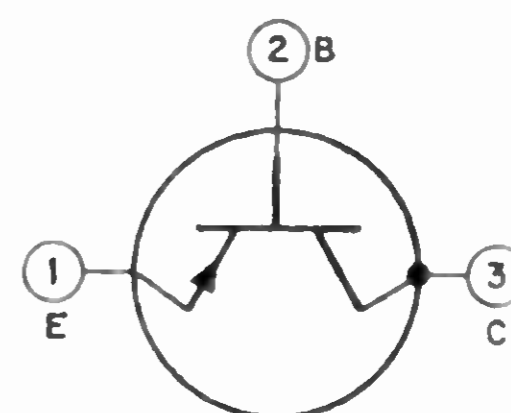
Emitter-to-Base Breakdown Voltage ($I_E = -0.1$ mA, $I_C = 0$)	$V_{(BR)EBO}$	-5 min	V
Collector-to-Emitter Breakdown Voltage ($V_{BE} = 1.5$ V, $I_C = -0.1$ mA, Base-emitter reverse biased)	$V_{(BR)CEV}$	-75 min	V
Collector-to-Emitter Sustaining Voltage $I_C = -100$ mA, $R_{BE} = 100 \Omega$	$V_{CER}(SUS)$	-65 min	V
$I_C = -100$ mA, base open	$V_{CEO}(SUS)$	-50 min	V

CHARACTERISTICS (cont'd)

Collector-to-Emitter Saturation Voltage ($I_C = -500$ mA, $I_B = -50$ mA)	$V_{CE(sat)}$	-1.2 max	V
Base-to-Emitter Voltage ($V_{EB} = -4$ V, $I_C = -500$ mA)	V_{BE}	-1.4 max	V
Collector-Cutoff Current ($V_{CB} = -60$ V, $I_E = 0$)	I_{CBO}	-5 max	μ A
Emitter-Cutoff Current ($V_{EB} = -4$ V, $I_C = 0$)	I_{EBO}	-0.5 max	μ A
Pulsed Static Forward-Current Transfer Ratio ($V_{CE} = -4$ V, $I_C = -500$ mA)	h_{FE} (pulsed)	40 to 250	
Gain-Bandwidth Product ($V_{CE} = -4$ V, $I_C = -500$ mA)	f_T	50 min	MHz
Second-Breakdown Collector Current ($V_{CE} = -35$ V, base forward-biased, non-repetitive pulse = 1 s)	$I_{S/b}$	-285 min	mA
Turn-On Time ($V_{CE} = -30$ V, $I_C = -500$ mA, $I_B = -50$ mA)	$t_d + t_r$	100 max	ns
Turn-Off Time ($V_{CE} = -30$ V, $I_C = -500$ mA, $I_B = -50$ mA)	$t_s + t_r$	1000 max	ns
Thermal Resistance, Junction-to-Case	θ_{J-C}	17.5 max	$^{\circ}$ C/W
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	150 max	$^{\circ}$ C/W

2N5415 POWER TRANSISTOR

Si p-n-p triple-diffused type used for high-speed switching and linear-amplifier applications in military, industrial, and commercial equipment. P-N-P structure permits complementary operation with a matching n-p-n type such as the 2N3440. JEDEC TO-5, Outline No.5.

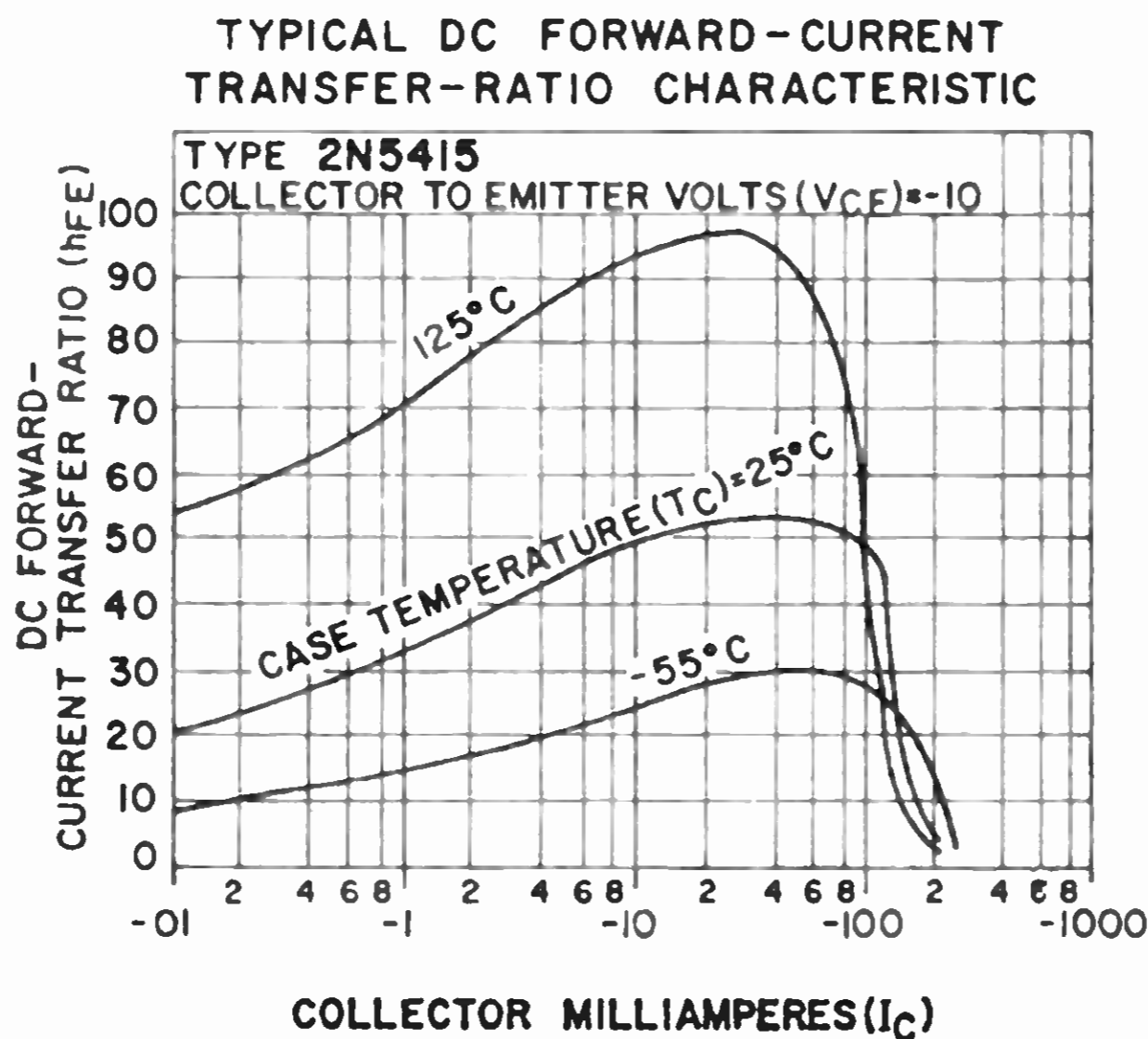


MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage	$V_{CEO(sus)}$	-200	V
Emitter-to-Base Voltage	V_{EBO}	-4	V
Collector Current	I_C	-1	A
Base Current	I_B	-0.5	A
Transistor Dissipation:			
T_C up to 25° C	P_T	10	W
T_C above 25° C		See curve page 300	
T_A up to 50° C	P_T	1	
T_A above 50° C	P_T	Derate linearly at 6.7 mW/ $^{\circ}$ C	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 200	$^{\circ}$ C
Storage	T_{STG}	-65 to 200	$^{\circ}$ C
Lead-Soldering Temperature (10 s max)	T_L	255	$^{\circ}$ C

CHARACTERISTICS (At case temperature = 25° C)

Collector-to-Emitter Sustaining Voltage ($I_C = -50$ mA, $I_B = 0$)	$V_{CEO(sus)}$	-200 min	V
Base-to-Emitter Saturation Voltage ($V_{CB} = -10$ V, $I_C = -50$ V)	$V_{BE(sat)}$	-1.5 max	V

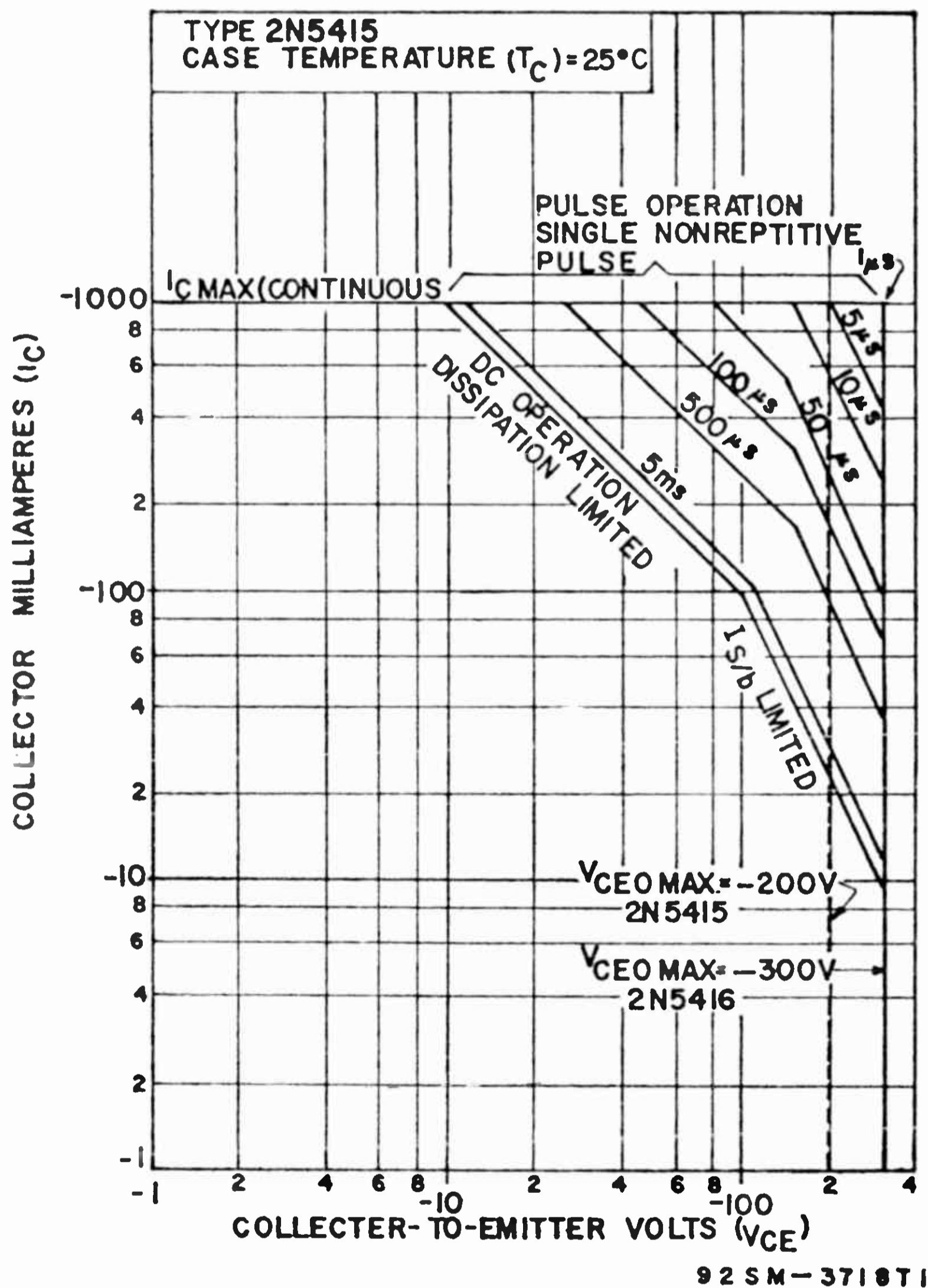


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CHARACTERISTICS (cont'd)

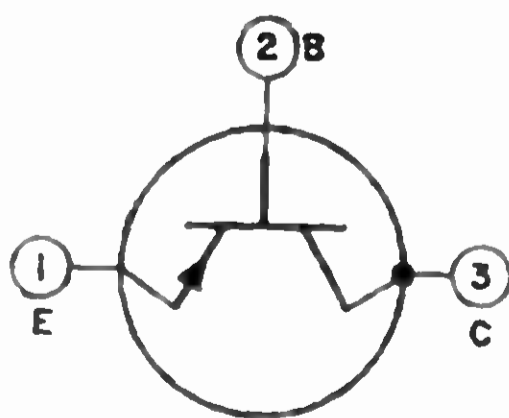
Collector-to-Emitter Saturation Voltage ($I_C = -50$ mA, $I_B = 5$ mA)	$V_{CE(sat)}$	-2.5 max	V
Collector-Cutoff Current: $V_{CE} = -150$ V, $I_B = 0$	I_{CEO}	-50 max	μA
$V_{CE} = -200$ V, $V_{BE} = 1.5$ V	I_{CEV}	-50 max	μA
Emitter-Cutoff Current ($V_{EB} = -4$ V, $I_C = 0$)	I_{EBO}	-20 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = -10$ V, $I_C = -50$ mA)	h_{FE}	30 to 150	
Small-Signal, Forward-Current Transfer Ratio ($V_{CE} = -10$ V, $I_C = -10$ mA, $f =$ MHz)	h_{fe}	3 min	
Output Capacitance ($V_{CB} = -10$ V, $I_E = 0$, $f = 1$ MHz)	C_{obo}	15 max	pF
Second-Breakdown Collector Current ($V_{CE} = -100$ V, base forward-biased)	$I_{s/b}$	-100 min	mA
Thermal Resistance, Junction-to-Case	θ_{J-C}	17.5 max	$^{\circ}C/W$

MAXIMUM OPERATING AREAS



POWER TRANSISTOR

2N5416



Si p-n-p triple-diffused type used for high-speed switching linear-amplifier applications in military, industrial, and commercial equipment. P-N-P structure permits complementary operation with a matching n-p-n type such as the 2N3439. JEDEC TO-5, Outline No.5.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-350	V
Collector-to-Emitter Sustaining Voltage: Base open	$V_{CEO(sus)}$	-300	V
$R_{BE} = 50 \Omega$	$V_{CER(sus)}$	-350	V

MAXIMUM RATINGS (cont'd)

Emitter-to-Base Voltage	V_{EBO}	-6	A
Collector Current	I_C	-1	A
Base Current	I_B	-0.5	W
Transistor Dissipation:			
T_C up to 25°C	P_T	10	W
T_C above 25°C	P_T	See curve page 300	
T_A up to 50°C	P_T	1	°C
T_A above 50°C	P_T	Derate linearly at 6.7 mW/°C	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	255	°C

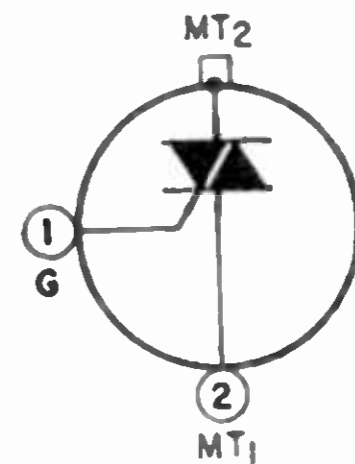
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage:			
Base open	V_{CEO} (sus)	-300 min	V
$R_{BE} = 50 \Omega$	V_{CER} (sus)	-350 min	V
Base-to-Emitter Saturation Voltage ($V_{CE} = 10$ V, $I_C = 50$ mA)	V_{BE} (sat)	-1.5 max	V
Collector-to-Emitter Saturation Voltage ($I_C = -50$ mA, $I_B = 5$ mA)	V_{CE} (sat)	-2 max	V
Collector-Cutoff Current:			
$V_{CE} = -250$ V, $I_B = 0$	I_{CEO}	-50 max	μA
$V_{CE} = -300$ V, $V_{BE} = 1.5$ V	I_{CEV}	-50 max	μA
Emitter-Cutoff Current ($V_{EB} = -6$ V, $I_C = 0$)	I_{EBO}	-20 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = -10$ V, $I_C = 50$ mA)	h_{FE}	30 to 120	
Small-Signal, Forward-Current Transfer Ratio ($V_{CE} = -10$ V, $I_C = -10$ mA, $f = 5$ MHz)	h_{fe}	3 min	
Output Capacitance ($V_{CB} = -10$ V, $I_E = 0$, $f = 1$ MHz)	C_{obo}	15 max	pF
Second-Breakdown Collector Current ($V_{CE} = -100$ V, base forward-biased)	$I_{s/b}$	-100 min	mA
Thermal Resistance, Junction-to-Case	θ_{J-C}	17.5	°C/W

2N5441
2N5442

TRIACS

Si gate-controlled full-wave types used for the control of ac loads in applications such as heating controls, motor controls, arc welding equipment, light dimmers, and power switching systems. See **Mounting Hardware** for desired mounting arrangement. Outline No.36.



MAXIMUM RATINGS (For sinusoidal supply voltage at 50/60 Hz with resistive or inductive load)

	2N5441	2N5442	
	200	400	
V_{DROM}^* ($T_J = -65^\circ C$ to $110^\circ C$)	_____	_____	V
$I_{T(RMS)}$ ($T_C = 70^\circ C$, conduction angle = 360°)	_____	_____	A
I_{TSM} (1 cycle of principal voltage)	_____	_____	A
$I_{GTM}\ddagger$ (1 μs max)	_____	_____	A
$P_{GM}\ddagger$ (10 μs max, $I_{GTM} \leq 4$ A peak)	_____	_____	W
$P_{G(AV)}$	_____	_____	W
T_{STG}	_____	_____	°C
T_C (opr)	_____	_____	°C

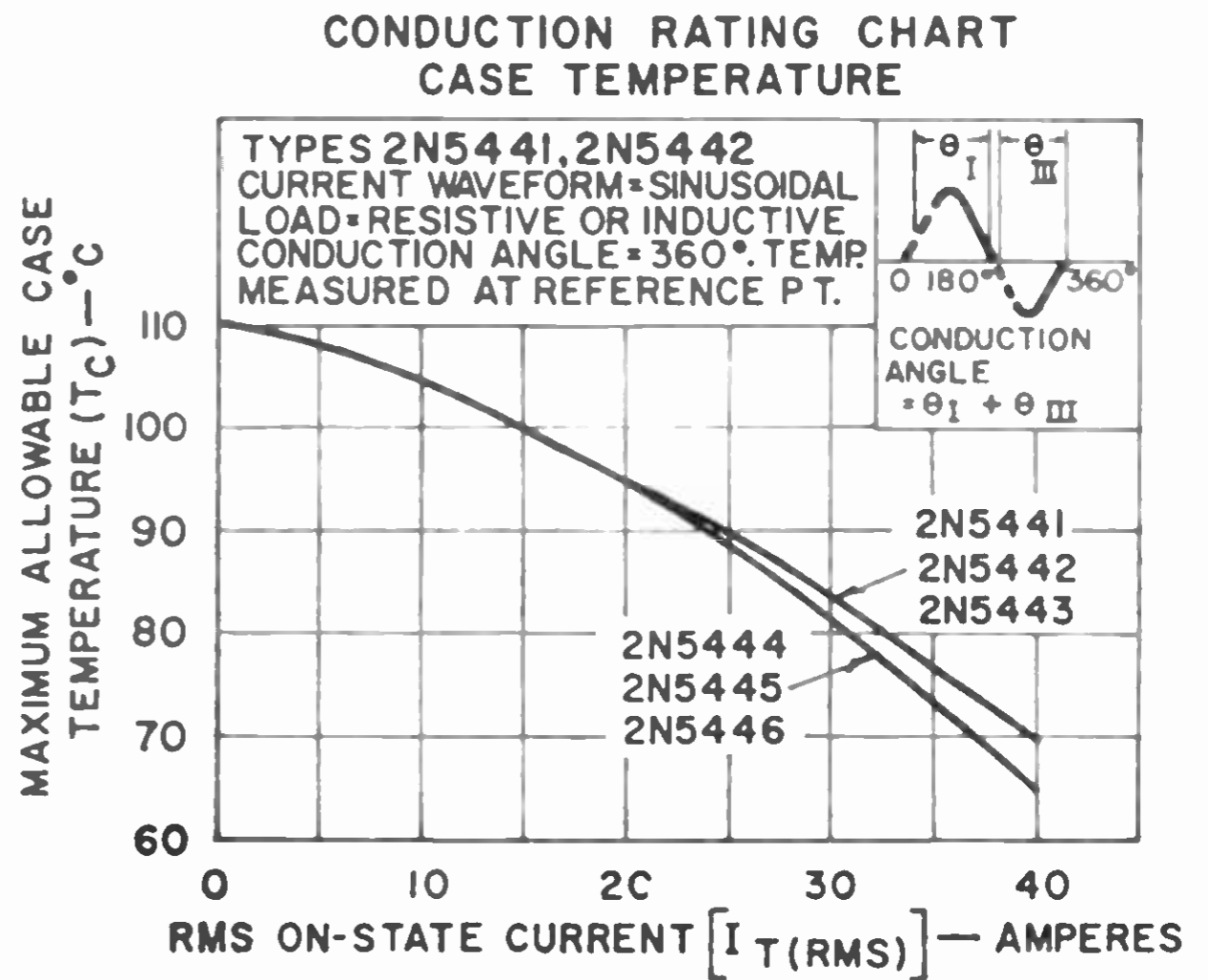
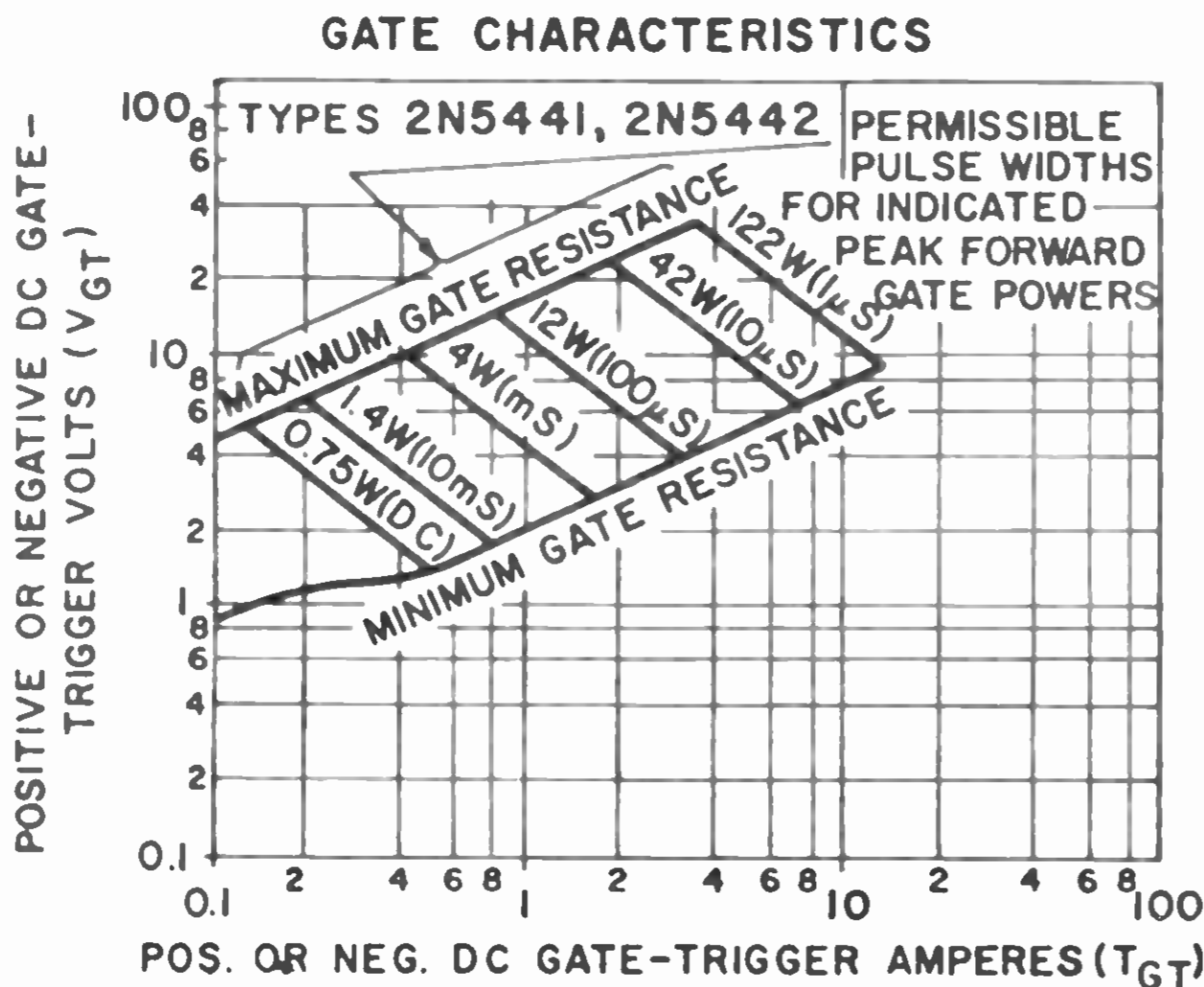
CHARACTERISTICS (At maximum electrical ratings at $T_C = 25^\circ C$)

I_{DROM}^* ($T_J = 110^\circ C$, $V_{DROM} =$ max. rated value)	_____	0.2 typ; 4 max	_____	mA
V_{TM}^* ($i_T = 100$ A peak)	_____	1.7 typ; 2 max	_____	V
I_{HO}^* (initial principal current = 150 mA dc)	_____	25 typ; 60 max	_____	mA
Commutating dv/dt^* ($V_D = V_{DROM}$, $I_{T(RMS)} = 40$ A, commutating $di/dt = 22$ A/ms, gate unenergized at $T_C = 70^\circ C$)	_____	5 min; 30 typ	_____	V/ μs
Critical dv/dt^* ($V_D = V_{DROM}$, exponential voltage rise, $T_C = 110^\circ C$)	50 min; 200 typ	30 min; 150 typ	_____	V/ μs
$I_{GT}\ddagger$ ($V_D = 12$ Vdc, $R_L = 12 \Omega$):				
I ⁺ mode, V_{MT2} positive, V_G positive	_____	15 typ; 50 max	_____	mA
I ⁻ mode, V_{MT2} positive, V_G negative	_____	30 typ; 80 max	_____	mA
III ⁺ mode, V_{MT2} negative, V_G positive	_____	40 typ; 80 max	_____	mA
III ⁻ mode, V_{MT2} negative, V_G negative	_____	20 typ; 50 max	_____	mA

CHARACTERISTICS (cont'd)

$V_{GT}^* \ddagger$ ($V_D = 12 \text{ Vdc}$, $R_L = 12 \Omega$)	2N5441	1.35 typ; 2.5 max	2N5442	V
$V_{GT}^* \ddagger$ ($V_D = V_{DROM}$, $R_L = 125 \Omega$, $T_C = 110^\circ\text{C}$)	-----	0.2 min	-----	V
t_{gt} ($V_D = V_{DROM}$, $I_{GT} = 120 \text{ mA}$, $t_r = 0.1 \mu\text{s}$, $i_r = 60 \text{ A peak}$)	-----	3	-----	μs
θ_{J-C}	-----	0.8 max	-----	$^\circ\text{C/W}$

* For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
 ‡ For either polarity of gate voltage (V_G) with reference to main terminal 1.

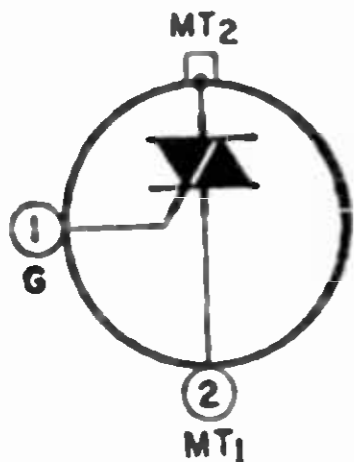


92CS-15198T2

92LS-2255T1

TRIACS

2N5444
2N5445



Si gate-controlled full-wave types used for the control of ac loads in applications such as heating controls, motor controls, arc welding equipment, light dimmers, and power switching systems. See Mounting Hardware for desired mounting arrangement. Outline No.37. Types 2N5444 and 2N5445 are identical with types 2N5441 and 2N5442, respectively, except for the following items:

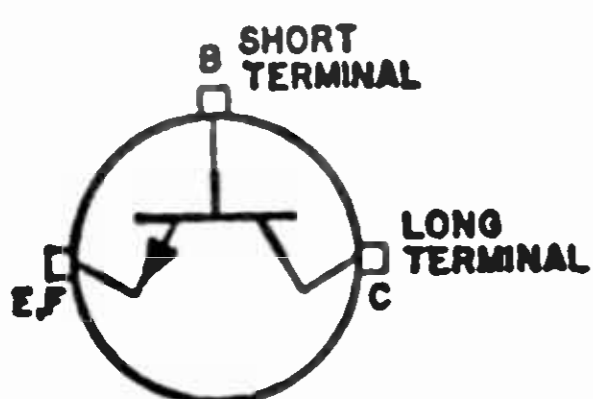
MAXIMUM RATINGS (For sinusoidal supply voltage at 50/60 Hz with resistive or inductive load)

$I_{T(RMS)}$ ($T_C = 65^\circ\text{C}$, conduction angle = 360°)	2N5444	40	2N5445	A
--	--------	----	--------	---

CHARACTERISTICS (At maximum electrical ratings at $T_C = 25^\circ\text{C}$)

Commutating dv/dt^* ($V_D = V_{DROM}$, $I_{T(RMS)} = 40 \text{ A}$, commutating $di/dt = 22 \text{ A/ms}$, gate unenergized at $T_C = 65^\circ\text{C}$)	-----	5 min; 30 typ	-----	$\text{V}/\mu\text{s}$
θ_{J-C}	-----	0.9 max	-----	$^\circ\text{C/W}$

* For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.



RF POWER TRANSISTORS

2N5470

Si n-p-n "overlay" epitaxial planar type used for vhf/microwave power amplifiers, microwave fundamental-frequency oscillators, and frequency multipliers. Outline No.54.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	55	V
Collector-to-Emitter Voltage ($R_{BE} = 10 \Omega$)	V_{CER}	55	V

MAXIMUM RATINGS (cont'd)

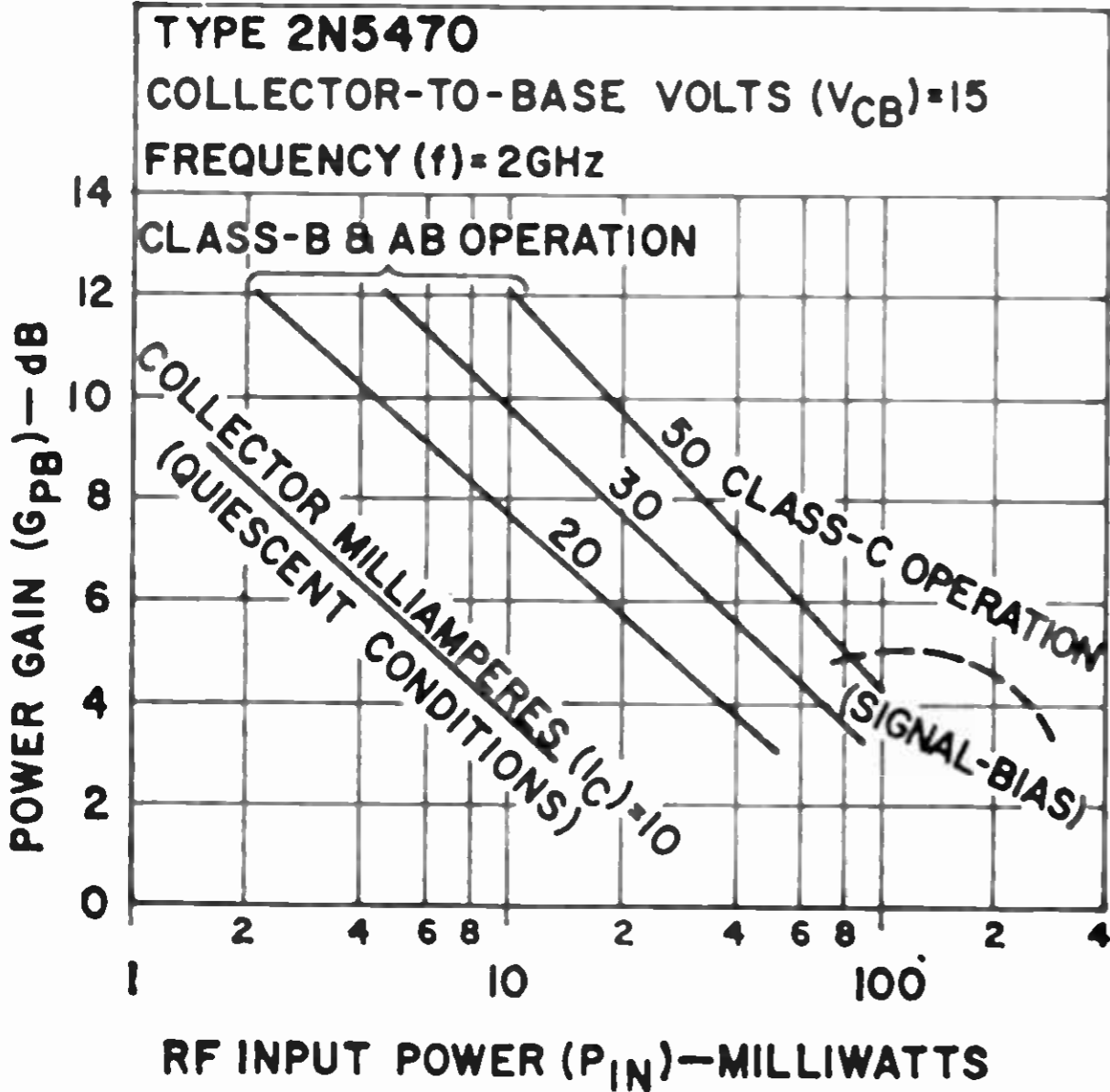
Emitter-to-Base Voltage	V_{EBO}	3.5	V
Peak Collector Current	i_C	0.4	A
Collector Current	I_C	0.2	A
Transistor Dissipation:			
T_C up to 25°C	P_T	3.5	W
T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C

CHARACTERISTICS (At case temperature = 25°C)

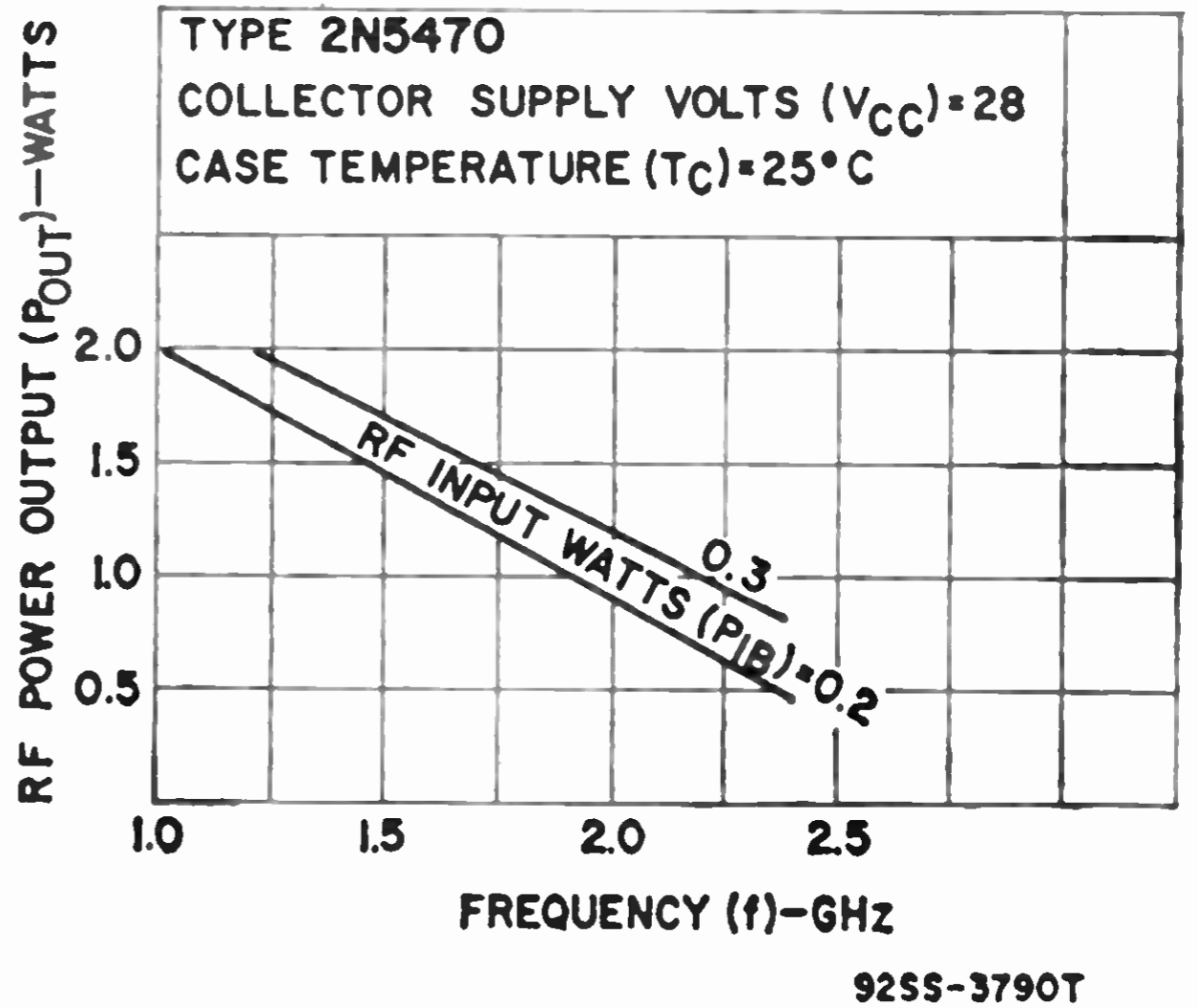
Collector-to-Base Breakdown Voltage ($I_C = 0.1$ mA, $I_E = 0$)	$V_{(BR)CBO}$	55 min	V
Collector-to-Emitter Sustaining Voltage ($I_C = 5$ mA, $R_{BE} = 10 \Omega$)	$V_{CER(SUS)}$	55 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.1$ mA, $I_C = 0$)	$V_{(BR)EBO}$	3.5 min	V
Collector-to-Emitter Saturation Voltage ($I_B = 10$ mA, $I_C = 100$ mA)	$V_{CE(sat)}$	1 max	V
Collector-Cutoff Current ($V_{CE} = 50$ V, $I_B = 0$)	I_{CES}	1 max	mA
Collector-to-Base Capacitance ($V_{CB} = 30$ V, $I_E = 0$, $f = 1$ MHz)	C_{cb}	3 max	pF
RF Power Output:			
Common-Base Amplifier:			
$V_{CB} = 28$ V, $P_{IB} = 0.316$ W, $f = 2$ GHz	P_{OB}^*	1 min	W
$V_{CB} = 28$ V, $P_{IB} = 0.2$ W, $f = 1$ GHz	P_{OB}^{\square}	2	W
Common-Base Oscillator ($V_{CB} = 24$ V, $I_C = 80$ mA)	P_{OB}	0.3	W

* For conditions given, minimum efficiency = 30 per cent.
 ■ For conditions given, typical efficiency = 50 per cent.

TYPICAL POWER-GAIN CHARACTERISTICS



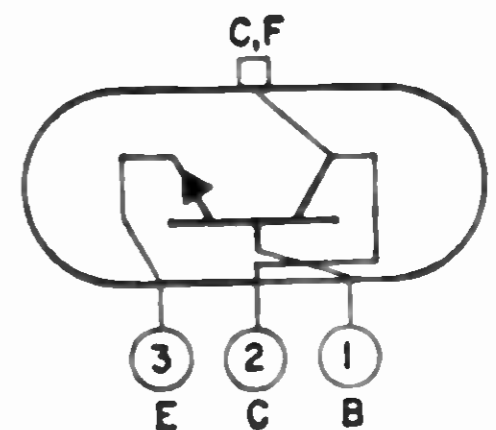
TYPICAL RF POWER OUTPUT CHARACTERISTICS



2N5490

POWER TRANSISTOR

Si n-p-n type featuring a base comprised of a homogeneous-resistivity silicon material and molded silicone plastic package having horizontal leads for mounting on printed-circuit boards. It is used in a wide variety of medium-power switching and amplifier applications in military, industrial, and commercial equipment. Outline No.53. See Mounting Hardware for desired mounting arrangement.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	60	V
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MAXIMUM RATINGS (cont'd)

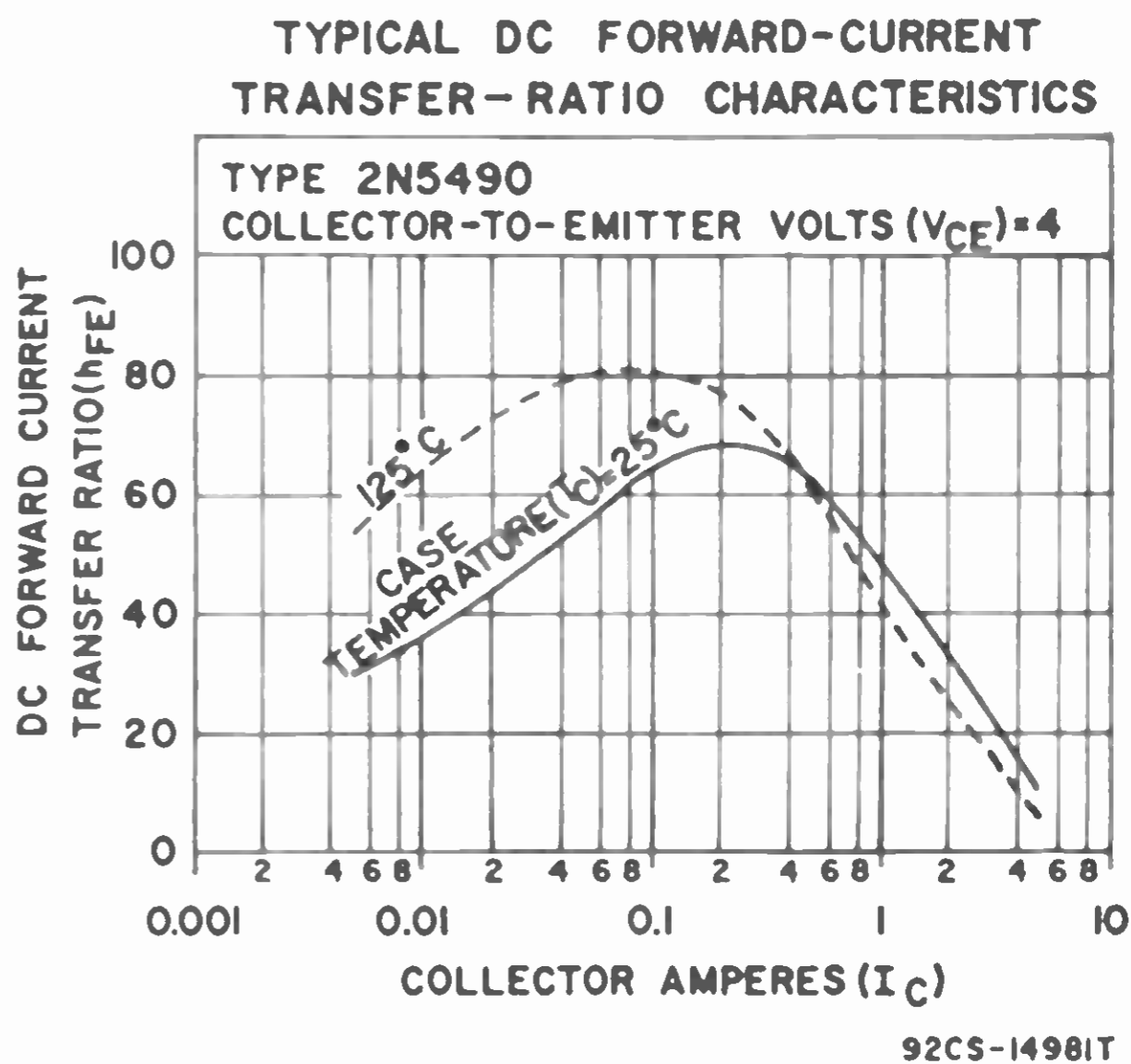
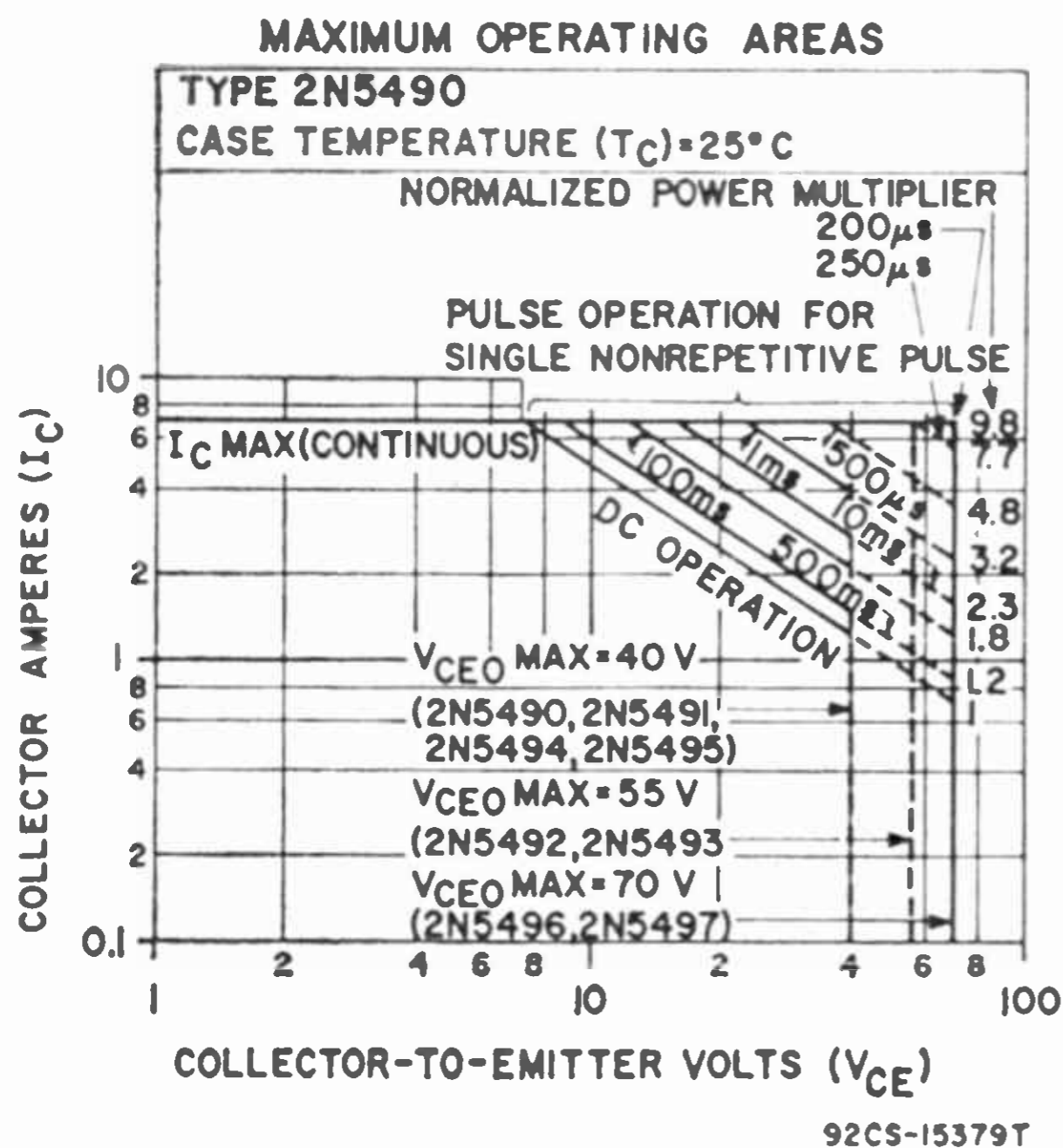
Collector-to-Emitter Sustaining Voltage:

$V_{BE} = -1.5$ V	V_{CEV} (SUS)	60	V
$R_{BE} = 100$ Ω	V_{CER} (SUS)	50	V
Base open	V_{CEO} (SUS)	40	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	7	A
Base Current	I_B	3	A
Transistor Dissipation:			
T_C up to 25°C	P_T	50	W
T_C above 25°C	P_T Derate linearly at 0.4		W/°C
T_A up to 25°C	P_T	1.8	W
T_A above 25°C	P_T Derate linearly at 0.0144		W/°C
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 150	°C
Storage	T_{STG}	-65 to 150	°C
Lead-Soldering Temperature (10 s max)	T_L	235	°C

CHARACTERISTICS (At case temperature = 25°C)

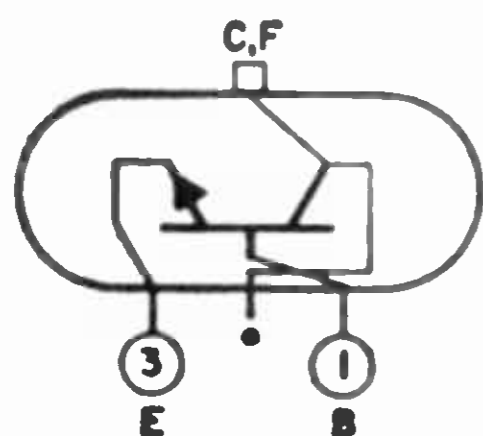
Collector-to-Emitter Sustaining Voltage:

$I_C = 0.1$ A, $I_B = 0$, base open, $t_P = 300$ μ s, $df = 0.018$	V_{CEO} (SUS)	40 min	V
$I_C = 0.1$ A, $R_{BE} = 100$ Ω , $t_P = 300$ μ s, $df = 0.018$...	V_{CER} (SUS)	50 min	V
$V_{BE} = -1.5$ V, $I_C = 0.1$ A, base-emitter junction reverse biased, $t_P = 300$ μ s, $df = 0.018$	V_{CEV}	60 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 2$ A, $I_B = 0.2$ A, $t_P = 300$ μ s, $df = 0.018$) ...	V_{CE} (sat)	1 max	V
Base-to-Emitter Voltage ($V_{CE} = 4$ V, $I_C = 2$ A, $t_P = 300$ μ s, $df = 0.018$)	V_{BE}	1.1 max	V
Collector-Cutoff Current:			
$V_{CE} = 40$ V, $R_{BE} = 100$ Ω	I_{CER}	2 max	mA
$V_{CE} = 40$ V, $R_{BE} = 100$ Ω , $T_C = 150^\circ$ C	I_{CER}	5 max	mA
Emitter-Cutoff Current ($V_{EB} = 5$ V)	I_{EBO}	1 max	mA
Pulsed Static Forward-Current Transfer Ratio ($V_{CE} = 4$ V, $I_C = 2$ A, $t_P = 300$ μ s, $df = 0.018$) ...	h_{FE} (pulsed)	20 to 100	
Gain-Bandwidth Product ($V_{CE} = 4$ V, $I_C = 0.5$ A)	f_T	0.8 min	MHz
Turn-On Time ($V_{CC} = 30$ V, $I_C = 2$ A, $I_B = 0.2$ A)	$t_d + t_r$	5 max	μ s
Turn-Off Time ($V_{CC} = 30$ V, $I_C = 2$ A, $I_B = 0.2$ A)	$t_s + t_f$	15 max	μ s
Thermal Resistance, Junction-to-Case	θ_{J-C}	2.5 max	°C/W
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	70 max	°C/W



POWER TRANSISTOR

2N5491

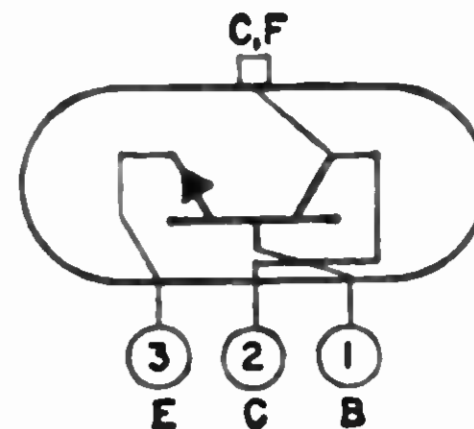


Si n-p-n type featuring a base comprised of a homogeneous-resistivity silicon material and molded silicone plastic package with vertical leads. This type fits a standard TO-66 socket. It is used in a wide variety of medium-power switching and amplifier applications in military, industrial, and commercial equipment.

Outline No.52. See Mounting Hardware for desired mounting arrangement. This type is electrically identical to type 2N5490.

2N5492 POWER TRANSISTOR

Si n-p-n type featuring a base comprised of a homogeneous-resistivity silicon material and molded silicone plastic package having horizontal leads for mounting on printed-circuit boards. It is used in a wide variety of medium-power switching and amplifier applications in military, industrial, and commercial equipment.



Outline No.53. See Mounting Hardware for desired mounting arrangement. For maximum operating area curves, refer to type 2N5490.

MAXIMUM RATINGS

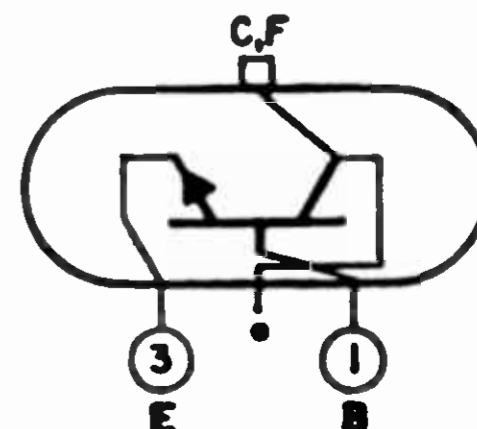
Collector-to-Base Voltage	V_{CBO}	75	V
Collector-to-Emitter Sustaining Voltage: $V_{BE} = -1.5$ V	$V_{CEV(sus)}$	75	V
$R_{BE} = 100 \Omega$	$V_{CER(sus)}$	65	V
Base open	$V_{CEO(sus)}$	55	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	7	A
Base Current	I_B	3	A
Transistor Dissipation:			
T_C up to $25^\circ C$	P_T	50	W
T_C above $25^\circ C$	P_T Derate linearly at 0.4		W/ $^\circ C$
T_A up to $25^\circ C$	P_T	1.8	W
T_A above $25^\circ C$	P_T Derate linearly at 0.0144		W/ $^\circ C$
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 150	$^\circ C$
Storage	T_{STG}	-65 to 150	$^\circ C$
Lead-Soldering Temperature (10 s max)	T_L	235	$^\circ C$

CHARACTERISTICS (At case temperature = $25^\circ C$)

Collector-to-Emitter Sustaining Voltage: $I_C = 0.1$ A, $I_B = 0$, base open, $t_P = 300 \mu s$, $df = 0.018$	$V_{CEO(sus)}$	55 min	V
$I_C = 0.1$ A, $R_{BE} = 100 \Omega$, $t_P = 300 \mu s$, $df = 0.018$... $V_{BE} = -1.5$ V, $I_C = 0.1$ A, base-emitter junction reverse biased, $t_P = 300 \mu s$, $df = 0.018$	$V_{CER(sus)}$	65 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 2.5$ A, $I_B = 0.25$ A, $t_P = 300 \mu s$, $df = 0.018$)	$V_{CE(sat)}$	1 max	V
Base-to-Emitter Voltage ($V_{CE} = 4$ V, $I_C = 2.5$ A, $t_P = 300 \mu s$, $df = 0.018$)	V_{BE}	1.3 max	V
Collector-Cutoff Current: $V_{CE} = 70$ V, $V_{BE} = -1.5$ V, base-emitter reverse biased	I_{CEV}	1 max	mA
$V_{CE} = 70$ V, $V_{BE} = -1.5$ V, $T_C = 150^\circ C$, base-emitter reverse biased	I_{CEV}	5 max	mA
$V_{CE} = 55$ V, $R_{BE} = 100 \Omega$	I_{CER}	0.5 max	mA
$V_{CE} = 55$ V, $R_{BE} = 100 \Omega$, $T_C = 150^\circ C$	I_{CER}	3.5 max	mA
Emitter-Cutoff Current ($V_{EB} = 5$ V)	I_{EBO}	1 max	mA
Pulsed Static Forward-Current Transfer Ratio ($V_{CE} = 4$ V, $I_C = 2.5$ A, $t_P = 300 \mu s$, $df = 0.018$)	$h_{FE}(pulsed)$	20 to 100	
Gain-Bandwidth Product ($V_{CE} = 4$ V, $I_C = 0.5$ A)	f_T	0.8 min	MHz
Turn-On Time ($V_{CC} = 30$ V, $I_C = 2.5$ A, $I_{B1} = 0.25$ A)	$t_d + t_r$	5 max	μs
Turn-Off Time ($V_{CC} = 30$ V, $I_C = 2.5$ A, $I_{B2} = 0.25$ A)	$t_s + t_r$	15 max	μs
Thermal Resistance, Junction-to-Case	θ_{J-C}	2.5 max	$^\circ C/W$
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	70 max	$^\circ C/W$

2N5493 POWER TRANSISTOR

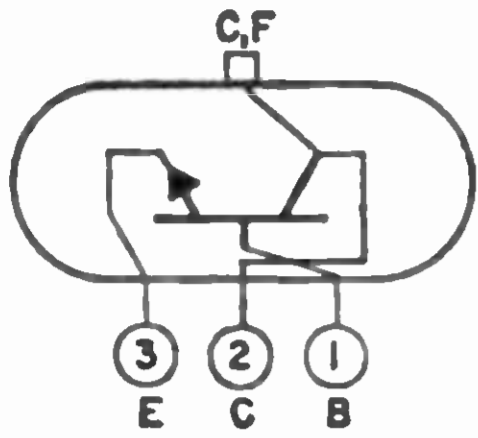
Si n-p-n type featuring a base comprised of a homogeneous-resistivity silicon material and molded silicone plastic package with vertical leads. This type fits a standard TO-66 socket. It is used in a wide variety of medium-power switching and amplifier applications in military, industrial, and commercial equipment.



Outline No.52. See Mounting Hardware for desired mounting arrangement. This type is electrically identical to type 2N5492.

POWER TRANSISTOR

2N5494



Si n-p-n type featuring a base comprised of a homogeneous-resistivity silicon material and molded silicone plastic package having horizontal leads for mounting on printed-circuit boards. It is used in a wide variety of medium-power switching and amplifier applications in military, industrial, and commercial equipment.

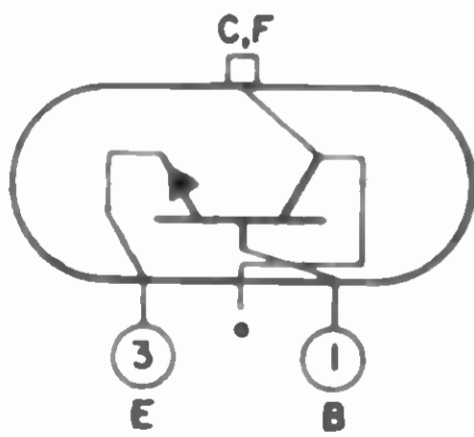
Outline No.53. See Mounting Hardware for desired mounting arrangement. For maximum ratings and maximum operating area curves, refer to type 2N5490.

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage:		
$I_C = 0.1 \text{ A}, I_B = 0, \text{ base open, } t_P = 300 \mu\text{s, df} = 0.018$	$V_{CE0}(\text{sus})$	40 min V
$I_C = 0.1 \text{ A}, R_{BE} = 100 \Omega, t_P = 300 \mu\text{s, df} = 0.018$...	$V_{CEr}(\text{sus})$	50 min V
$V_{BE} = -1.5 \text{ V}, I_C = 0.1 \text{ A}, \text{ base-emitter junction reverse biased}$	$V_{CEV}(\text{sus})$	60 min V
Collector-to-Emitter Saturation Voltage		
$(I_C = 3 \text{ A}, I_B = 0.3 \text{ A}, t_P = 300 \mu\text{s, df} = 0.018)$	$V_{CE}(\text{sat})$	1 max V
Base-to-Emitter Voltage ($V_{CE} = 4 \text{ V}, I_C = 3 \text{ A}, t_P = 300 \mu\text{s, df} = 0.018$)		
	V_{BE}	1.5 max V
Collector-Cutoff Current:		
$V_{CE} = 55 \text{ V}, V_{BE} = -1.5 \text{ V}$	I_{CEV}	1 max mA
$V_{CE} = 55 \text{ V}, V_{BE} = -1.5 \text{ V}, T_C = 150^\circ\text{C}$	I_{CEV}	5 max mA
$V_{CE} = 40 \text{ V}, R_{BE} = 100 \Omega$	I_{CER}	0.5 max mA
$V_{CE} = 40 \text{ V}, R_{BE} = 100 \Omega, T_C = 150^\circ\text{C}$	I_{CER}	3.5 max mA
Emitter-Cutoff Current ($V_{EB} = 5 \text{ V}$)		
	I_{EBO}	1 max mA
Pulsed Static Forward-Current Transfer Ratio		
$(V_{CE} = 4 \text{ V}, I_C = 3 \text{ A}, t_P = 300 \mu\text{s, df} = 0.018)$	$h_{FE}(\text{pulsed})$	20 to 100
Gain-Bandwidth Product ($V_{CE} = 4 \text{ V}, I_C = 0.5 \text{ A}$) ...		
	f_T	0.8 min MHz
Turn-On Time ($V_{CC} = 30 \text{ V}, I_C = 3 \text{ A}, I_{B1} = 0.3 \text{ A}$)		
	$t_d + t_r$	5 max μs
Turn-Off Time ($V_{CC} = 30 \text{ V}, I_C = 3 \text{ A}, I_{B2} = 0.3 \text{ A}$)		
	$t_s + t_f$	15 max μs
Thermal Resistance, Junction-to-Case		
	θ_{J-C}	2.5 max $^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient		
	θ_{J-A}	70 max $^\circ\text{C/W}$

POWER TRANSISTOR

2N5495

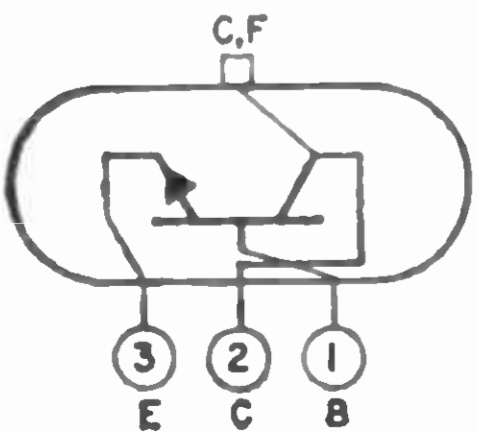


Si n-p-n type featuring a base comprised of a homogeneous-resistivity silicon material and molded silicone plastic package with vertical leads. This type fits a standard TO-66 socket. It is used in a wide variety of medium-power switching and amplifier applications in military, industrial, and commercial equipment.

Outline No.52. See Mounting Hardware for desired mounting arrangement. This type is electrically identical to type 2N5494.

POWER TRANSISTOR

2N5496



Si n-p-n type featuring a base comprised of a homogeneous-resistivity silicon material and molded silicone plastic package having horizontal leads for mounting on printed-circuit boards. It is used in a wide variety of medium-power switching and amplifier applications in military, industrial, and commercial equipment.

Outline No.53. See Mounting Hardware for desired mounting arrangement. For maximum operating area curves, refer to type 2N5490.

MAXIMUM RATINGS

Collector-to-Base Voltage	V _{CBO}	90	V
Collector-to-Emitter Sustaining Voltage:			
V _{BE} = -1.5 V	V _{CEV} (sus)	90	V
R _{BE} = 100 Ω	V _{CER} (sus)	80	V
Base open	V _{CEO} (sus)	70	V
Emitter-to-Base Voltage	V _{EBO}	5	V
Collector Current	I _C	7	A
Base Current	I _B	3	A
Transistor Dissipation:			
T _C up to 25°C	P _T	50	W
T _C above 25°C	P _T	Derate linearly at 0.4	W/°C
T _A up to 25°C	P _T	1.8	W
T _A above 25°C	P _T	Derate linearly at 0.0144	W/°C
Temperature Range:			
Operating (Junction)	T _J (opr)	-65 to 150	°C
Storage	T _{STG}	-65 to 150	°C
Lead-Soldering Temperature (10 s max)	T _L	235	°C

CHARACTERISTICS (At case temperature = 25°C)

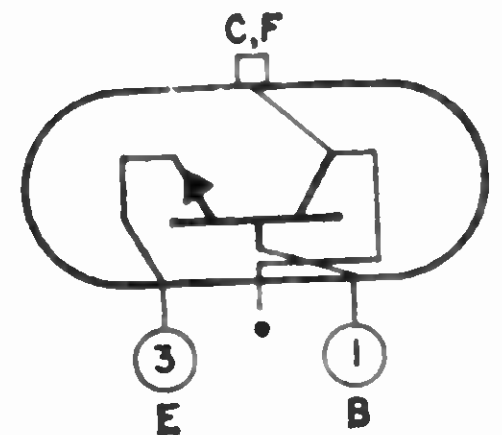
Collector-to-Emitter Sustaining Voltage:			
I _C = 0.1 A, I _B = 0, base open, t _P = 300 μs, df = 0.018	V _{CEO} (sus)	70 min	V
I _C = 0.1 A, R _{BE} = 100 Ω, t _P = 300 μs, df = 0.018 ...	V _{CER} (sus)	80 min	V
V _{BE} = -1.5 V, I _C = 0.1 A, base-emitter junction reverse biased	V _{CEV} (sus)	90 min	V
Collector-to-Emitter Saturation Voltage (I _C = 3.5 A, I _B = 0.35 A, t _P = 300 μs, df = 0.018)	V _{CE} (sat)	1 max	V
Base-to-Emitter Voltage (V _{CE} = 4 V, I _C = 3.5 A, t _P = 300 μs, df = 0.018)	V _{BE}	1.7 max	V
Collector-Cutoff Current:			
V _{CE} = 85 V, V _{BE} = -1.5 V	I _{CEV}	1 max	mA
V _{CE} = 85 V, V _{BE} = -1.5 V, T _C = 150°C	I _{CEV}	5 max	mA
V _{CE} = 70 V, R _{BE} = 100 Ω	I _{CER}	0.5 max	mA
V _{CE} = 70 V, R _{BE} = 100 Ω, T _C = 150°C	I _{CER}	3.5 max	mA
Emitter-Cutoff Current (V _{EB} = 5 V)	I _{EBO}	1 max	mA
Pulsed Static Forward-Current Transfer Ratio (V _{CE} = 4 V, I _C = 3.5 A, t _P = 300 μs, df = 0.018)	h _{FE} (pulsed)	20 to 100	
Gain-Bandwidth Product (V _{CE} = 4 V, I _C = 0.5 A)	f _T	0.8 min	MHz
Turn-On Time (V _{CC} = 30 V, I _C = 3.5 A, I _{B1} = 0.35 A)	t _d + t _r	5 max	μs
Turn-Off Time (V _{CC} = 30 V, I _C = 3.5 A, I _{B2} = 0.35 A)	t _s + t _f	15 max	μs
Thermal Resistance, Junction-to-Case	θ _{J-C}	2.5 max	°C/W
Thermal Resistance, Junction-to-Ambient	θ _{J-A}	70 max	°C/W

2N5497

POWER TRANSISTOR

Si n-p-n type featuring a base comprised of a homogeneous-resistivity silicon material and molded silicone plastic package with vertical leads. This type fits a standard TO-66 socket. It is used in a wide variety of medium-power switching and amplifier applications in military, industrial, and commercial equipment.

Outline No.52. See Mounting Hardware for desired mounting arrangement. This type is electrically identical to type 2N5496.

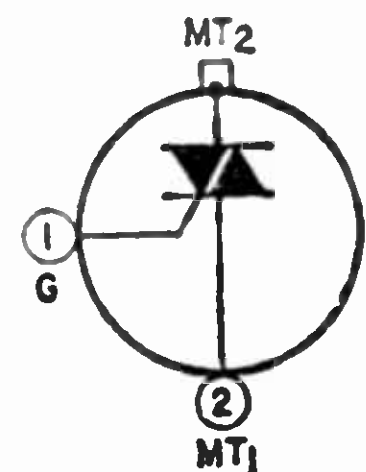


2N5567

TRIACS

2N5568

Si gate-controlled full-wave types used for control of ac loads in applications such as heating controls, motor controls, arc-welding equipment, light dimmers, and power switching systems. See Mounting Hardware for desired mounting arrangement. Outline No.36.



MAXIMUM RATINGS (For sinusoidal supply voltage at 50/60 Hz with resistive or inductive load)

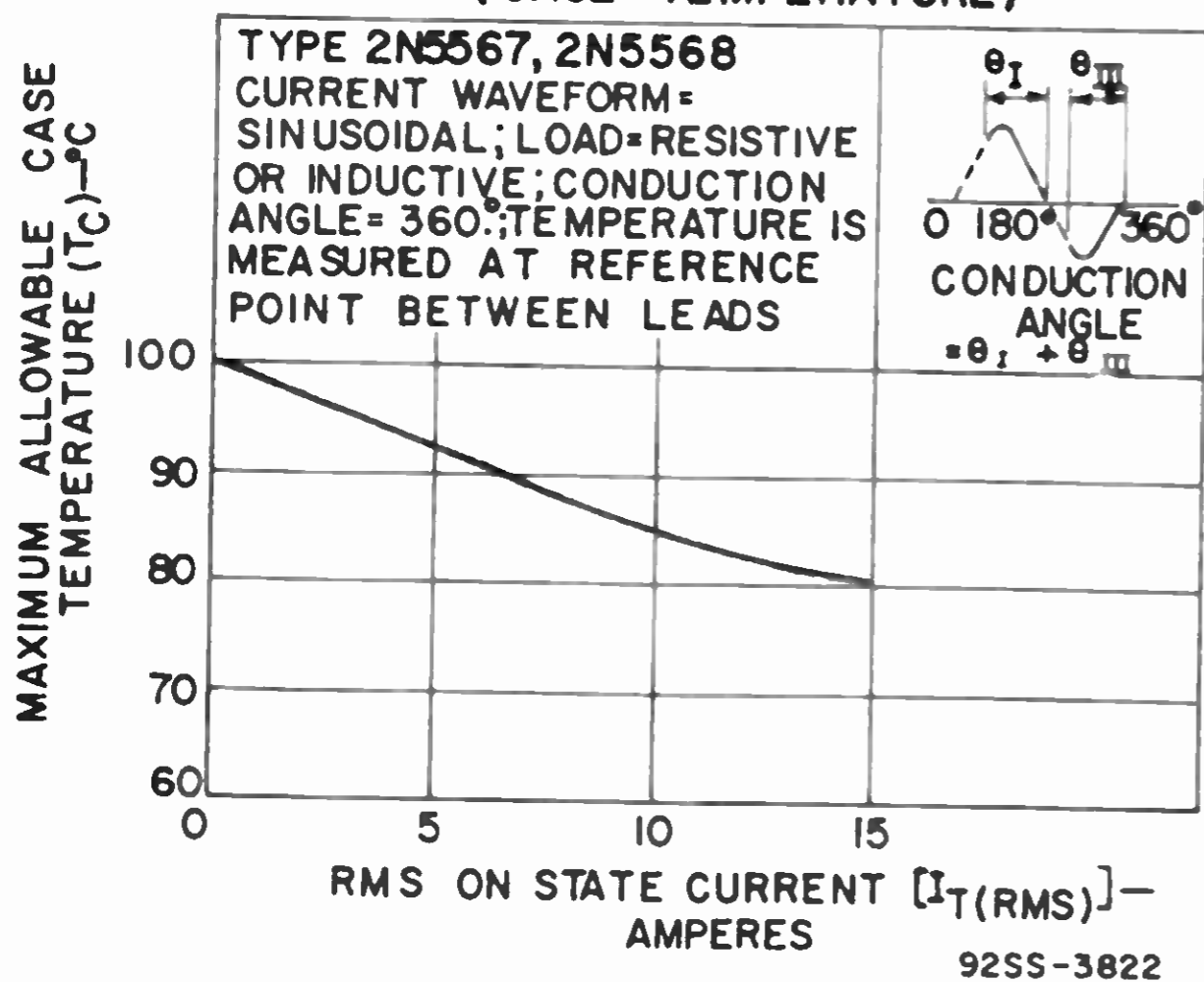
	2N5567 200	2N5568 400	
V _{DROM} * (T _J = -65°C to 100°C)			V
I _{T(RMS)} (T _C = 85°C, conduction angle = 360°)	10		A
I _{TSM} :			
1 cycle of principal voltage at 60 Hz	100		A
1 cycle of principal voltage at 50 Hz	84		A
I _{GT} † (1 μs max)	4		A
P _{GM} † (1 μs max, I _{GT} ≤ 4 A peak)	16		W
P _{G(AV)}	0.5		W
T _{STG}	-65 to 150		°C
T _c (opr)	-65 to 100		°C

CHARACTERISTICS

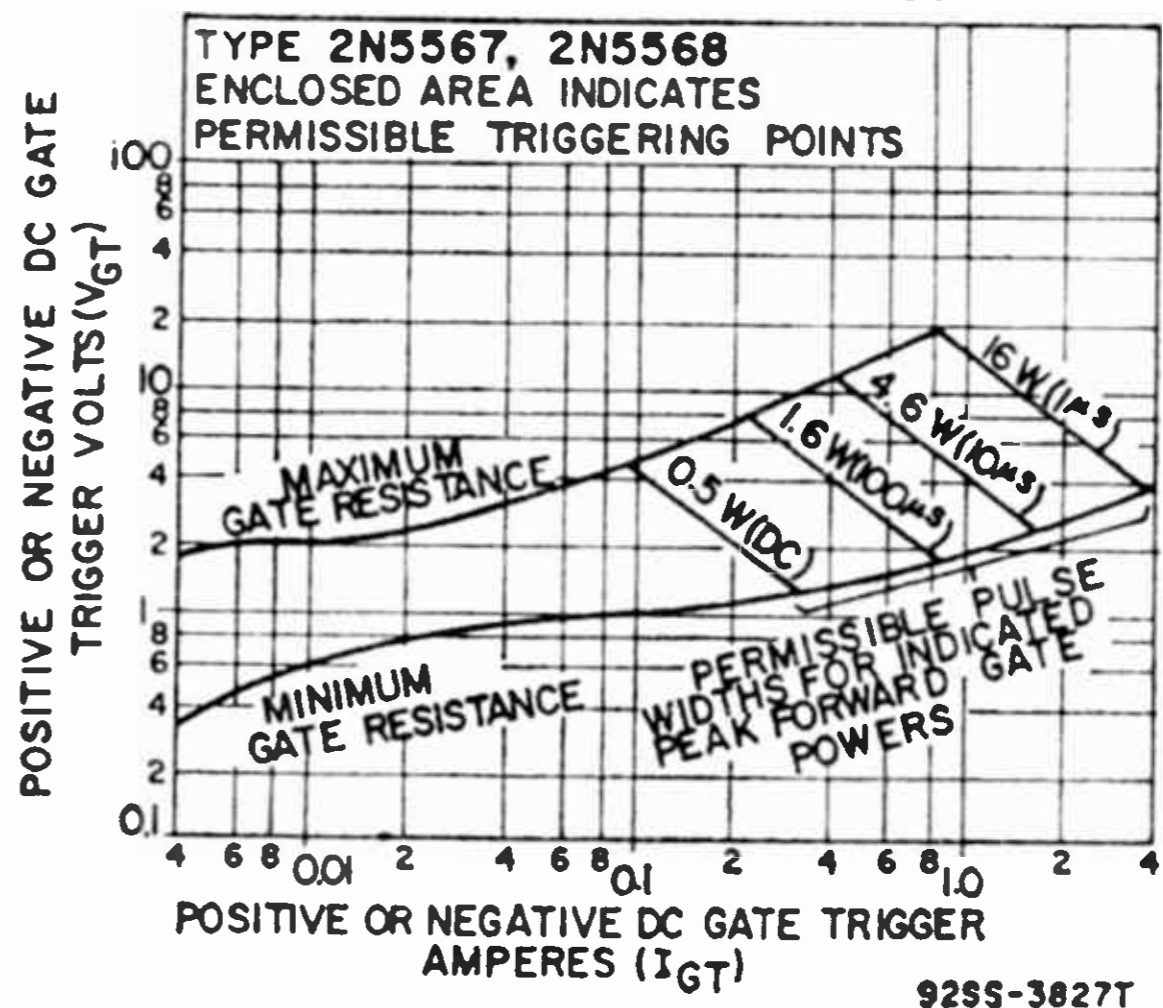
I _{DROM} * (T _J = 100°C, V _{DROM} = max rated value)	0.1 typ; 2 max	mA
V _{TM} * (i _T = 14 A peak, T _C = 25°C)	1.35 typ; 1.65 max	V
I _{HO} * (initial principal current = 500 mAdc):		
T _C = 25°C	15 typ; 30 max	mA
T _C = -65°C	75 typ; 200 max	mA
Commutating dv/dt* (v _D = V _{DROM} , I _{T(RMS)} = 10 A, commutating di/dt = 5.4 A/ms, gate unenergized at T _C = 85°C)	2 min; 5 typ	V/μs
Critical dv/dt* (v _D = V _{DROM} , exponential voltage rise, T _C = 100°C)	30 min; 150 typ; 20 min; 100 typ	V/μs
I _{GT} *‡ (v _D = 12 Vdc, R _L = 12 Ω, T _C = 25°C):		
I+ mode, V _{MT2} positive, V _G positive	10 typ; 25 max	mA
I- mode, V _{MT2} positive, V _G negative	20 typ; 40 max	mA
III+ mode, V _{MT2} negative, V _G positive	20 typ; 40 max	mA
III- mode, V _{MT2} negative, V _G negative	10 typ; 25 max	mA
I _{GT} *‡ (v _D = 12 Vdc, R _L = 12 Ω, T _C = 65°C):		
I+ mode, V _{MT2} positive, V _G positive	45 typ; 100 max	mA
I- mode, V _{MT2} positive, V _G negative	80 typ; 150 max	mA
III+ mode, V _{MT2} negative, V _G positive	80 typ; 150 max	mA
III- mode, V _{MT2} negative, V _G negative	45 typ; 100 max	mA
V _{GT} *‡ (v _D = 12 Vdc, R _L = 12 Ω):		
T _C = 25°C	1 typ; 2.5 max	V
T _C = -65°C	2 typ; 4 max	V
V _{GT} *‡ (v _D = V _{DROM} , R _L = 125 Ω, T _C = 100°C)	0.2 min	V
t _{gt} (v _D = V _{DROM} , I _{GT} = 80 mA, 0.1 μs tr, i _T = 16 A peak, T _C = 25°C)	2.2	μs
θ _{J-C} (steady-state)	1 max	°C/W

* For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
 ‡ For either polarity of gate voltage (V_G) with reference to main terminal 1.

CONDUCTION RATING CHART (CASE TEMPERATURE)



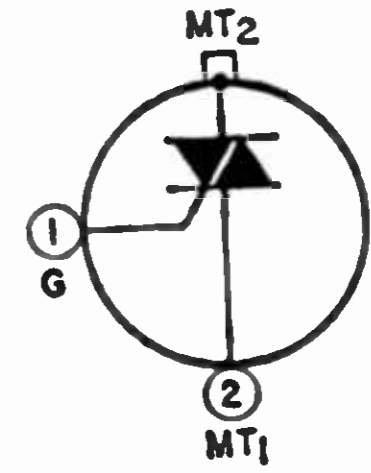
GATE CHARACTERISTICS



2N5569 2N5570

TRIACS

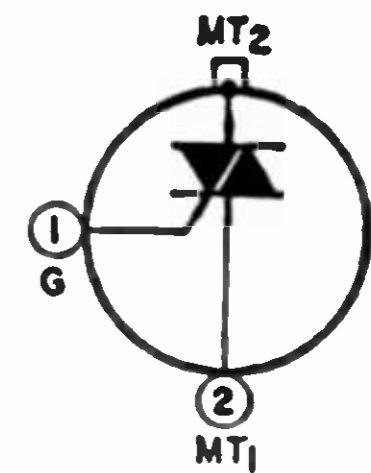
Si gate-controlled full-wave types used for control of ac loads in applications such as heating controls, motor controls, arc-welding equipment, light dimmers, and power switching systems. See **Mounting Hardware** for desired mounting arrangement. **Outline No.37**. Types 2N5569 and 2N5570 are identical with types 2N5567 and 2N5568, respectively.



2N5571 2N5572

TRIACS

Si gate-controlled full-wave types used for control of ac loads in applications such as heating controls, motor controls, arc-welding equipment, light dimmers, and power switching systems. See **Mounting Hardware** for desired mounting arrangement. **Outline No.36**. For gate characteristics curves, refer to types 2N5567 and 2N5568.



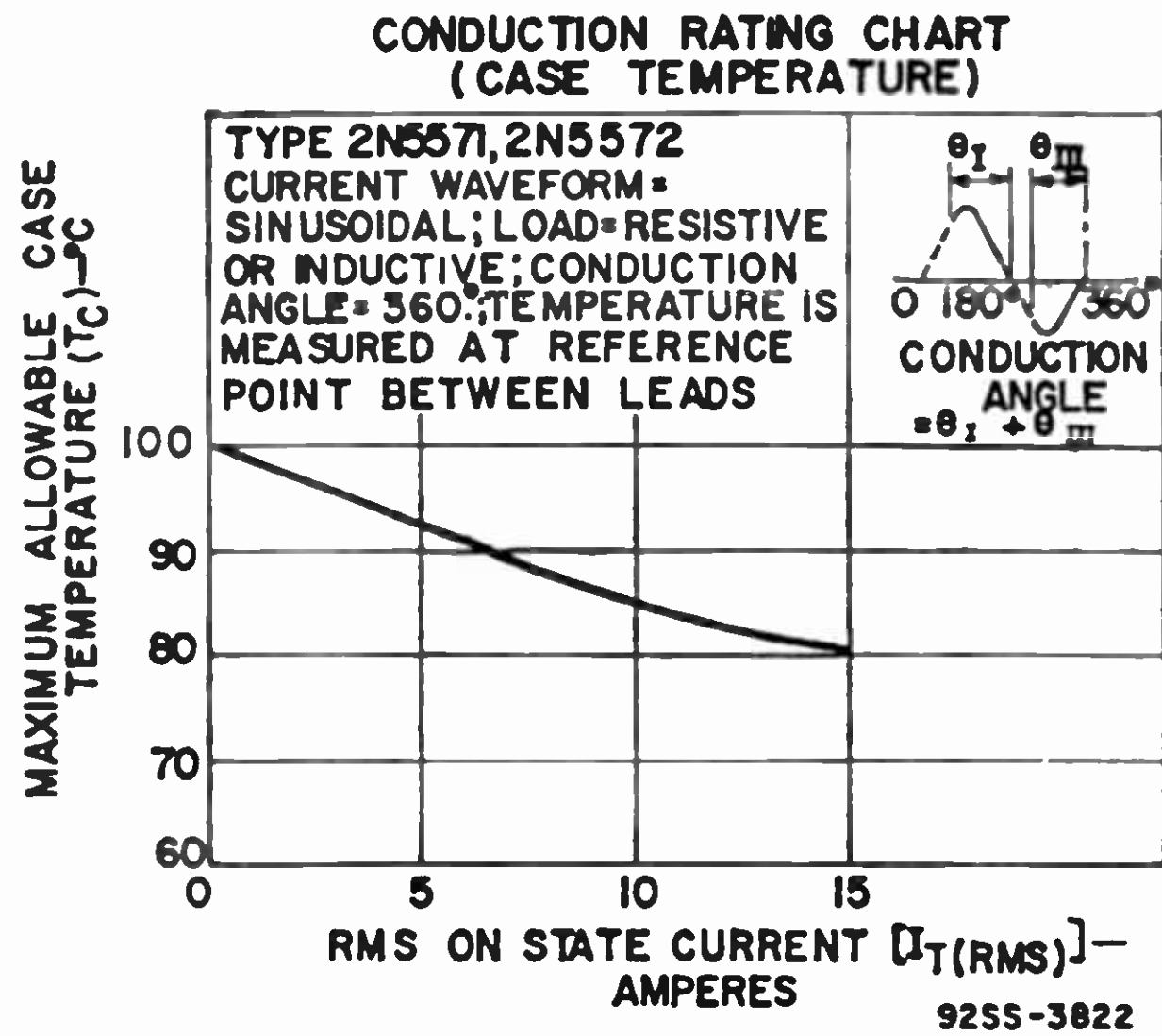
MAXIMUM RATINGS (For sinusoidal supply voltage at 50/60 Hz with resistive or inductive load)

	2N5571	2N5572	
V _{DROM} * (T _J = -65°C to 100°C)	200	400	V
I _{T(RMS)} (T _C = 80°C, conduction angle = 360°)	_____	15	A
I _{TSM} :			
1 cycle of principal voltage at 60 Hz	_____	100	A
1 cycle of principal voltage at 50 Hz	_____	86	A
I _{GT} ‡ (1 μs max)	_____	4	A
P _{GM} ‡ (1 μs max, I _{GT} ≤ 4 A peak)	_____	16	W
P _{G(AV)}	_____	0.5	W
T _{STG}	_____	-65 to 150	°C
T _{C(opr)}	_____	-65 to 150	°C

CHARACTERISTICS

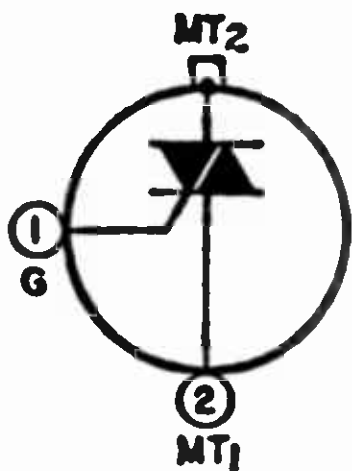
I _{DROM} * (T _J = 100°C, V _{DROM} = max. rated value)	_____	0.2 typ; 2 max	_____	mA
V _{TM} * (i _T = 21 A peak, T _C = 25°C)	_____	1.4 typ; 1.8 max	_____	V
I _{HO} * (initial principal current = 500 mAdc):				
T _C = 25°C	_____	20 typ; 75 max	_____	mA
T _C = -65°C	_____	75 typ; 300 max	_____	mA
Commutating dv/dt* (V _D = V _{DROM} , I _{T(RMS)} = 15 A, commutating di/dt = 8 A/ms, gate unenergized at T _C = 80°C)	_____	2 min; 10 typ	_____	V/μs
Critical dv/dt* (V _D = V _{DROM} , exponential voltage, gate open, T _C = 100°C)	_____	30 min; 150 typ	20 min; 100 typ	V/μs
I _{GT} *‡ (V _D = 12 Vdc, R _L = 12 Ω, T _C = 25°C):				
I ⁺ mode, V _{MT2} positive, V _G positive	_____	20 typ; 50 max	_____	mA
I ⁻ mode, V _{MT2} positive, V _G negative	_____	35 typ; 80 max	_____	mA
III ⁺ mode, V _{MT2} negative, V _G positive	_____	35 typ; 80 max	_____	mA
III ⁻ mode, V _{MT2} negative, V _G negative	_____	20 typ; 50 max	_____	mA
I _{GT} *‡ (V _D = 12 Vdc, R _L = 12 Ω, T _C = -65°C):				
I ⁺ mode, V _{MT2} positive, V _G positive	_____	75 typ; 150 max	_____	mA
I ⁻ mode, V _{MT2} positive, V _G negative	_____	100 typ; 200 max	_____	mA
III ⁺ mode, V _{MT2} negative, V _G positive	_____	100 typ; 200 max	_____	mA
III ⁻ mode, V _{MT2} negative, V _G negative	_____	75 typ; 150 max	_____	mA
V _{GT} *‡:				
V _D = 12 Vdc, R _L = 12 Ω, T _C = 25°C	_____	1 typ; 2.5 max	_____	V
V _D = 12 Vdc, R _L = 12 Ω, T _C = -65°C	_____	2 typ; 4 max	_____	V
V _D = V _{DROM} , R _L = 125 Ω, T _C = 100°C	_____	0.2 min	_____	V
t _{gt} (V _D = V _{DROM} , I _{TG} = 160 mA, t _r = 0.1 μs, i _T = 25 A peak, T _C = 25°C)	_____	3	_____	μs
θ _{J-C} (steady-state)	_____	1 max	_____	°C/W

* For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
‡ For either polarity of gate voltage (V_G) with reference to main terminal 1.



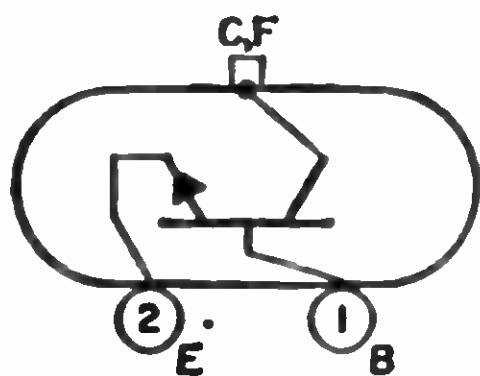
TRIACS

**2N5573
2N5574**



and 2N5572, respectively.

Si gate-controlled full-wave types used for control of ac loads in applications such as heating controls, motor controls, arc-welding equipment, light dimmers, and power switching systems. See Mounting Hardware for desired mounting arrangement. Outline No.37. Types 2N5573 and 2N5574 are identical with types 2N5571 and 2N5572, respectively.



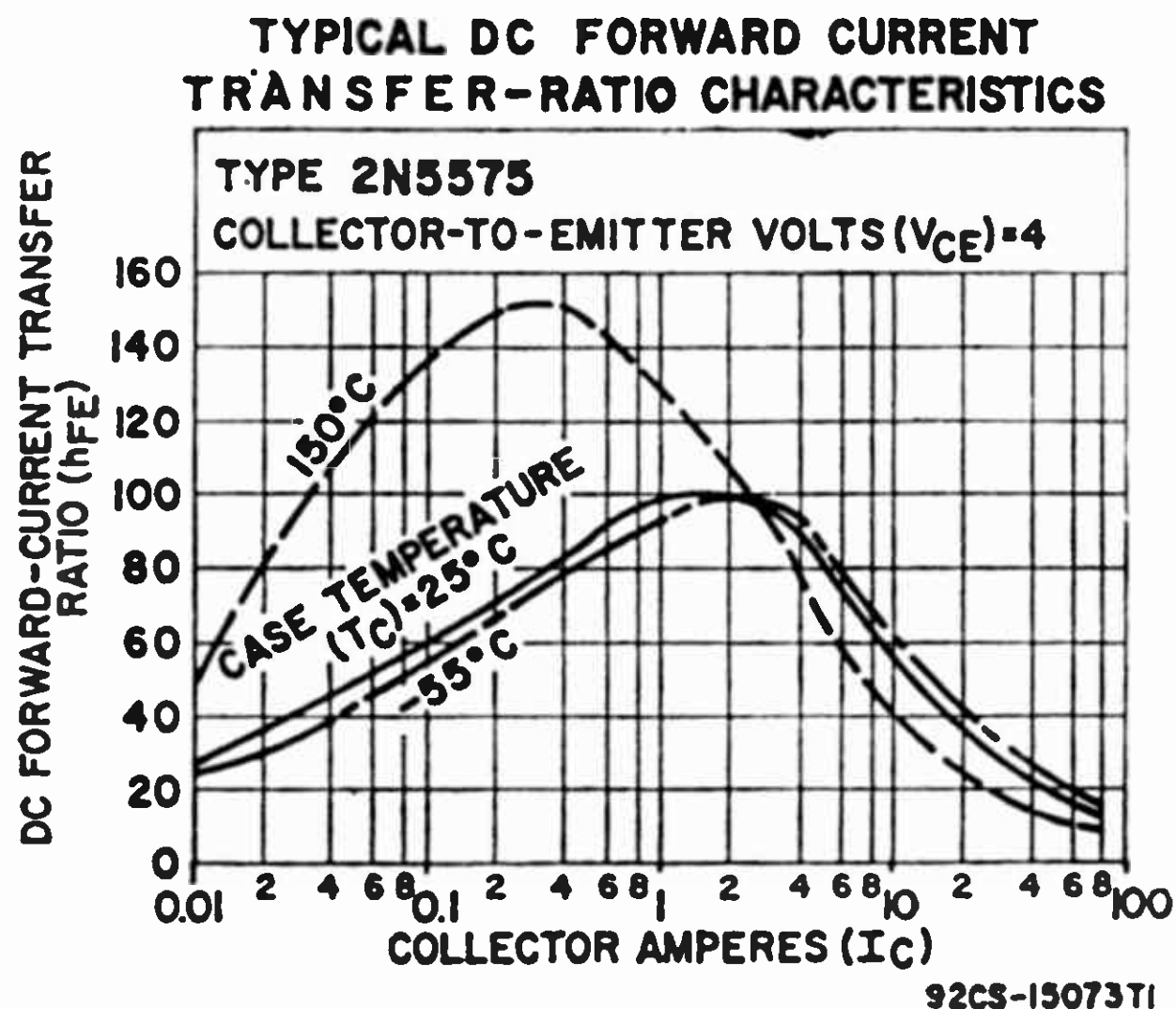
POWER TRANSISTOR

2N5575

Si n-p-n type features a base comprised of a homogeneous-resistivity silicon material. It is used in high-power linear and switching applications in military, industrial, and commercial equipment. Outline No.55.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	70	V
Collector-to-Emitter Sustaining Voltage:			
$R_{BE} = 10 \Omega, V_{BE} = -1.5 V$	$V_{CEX(sus)}$	70	V
Base open	$V_{CEO(sus)}$	50	V

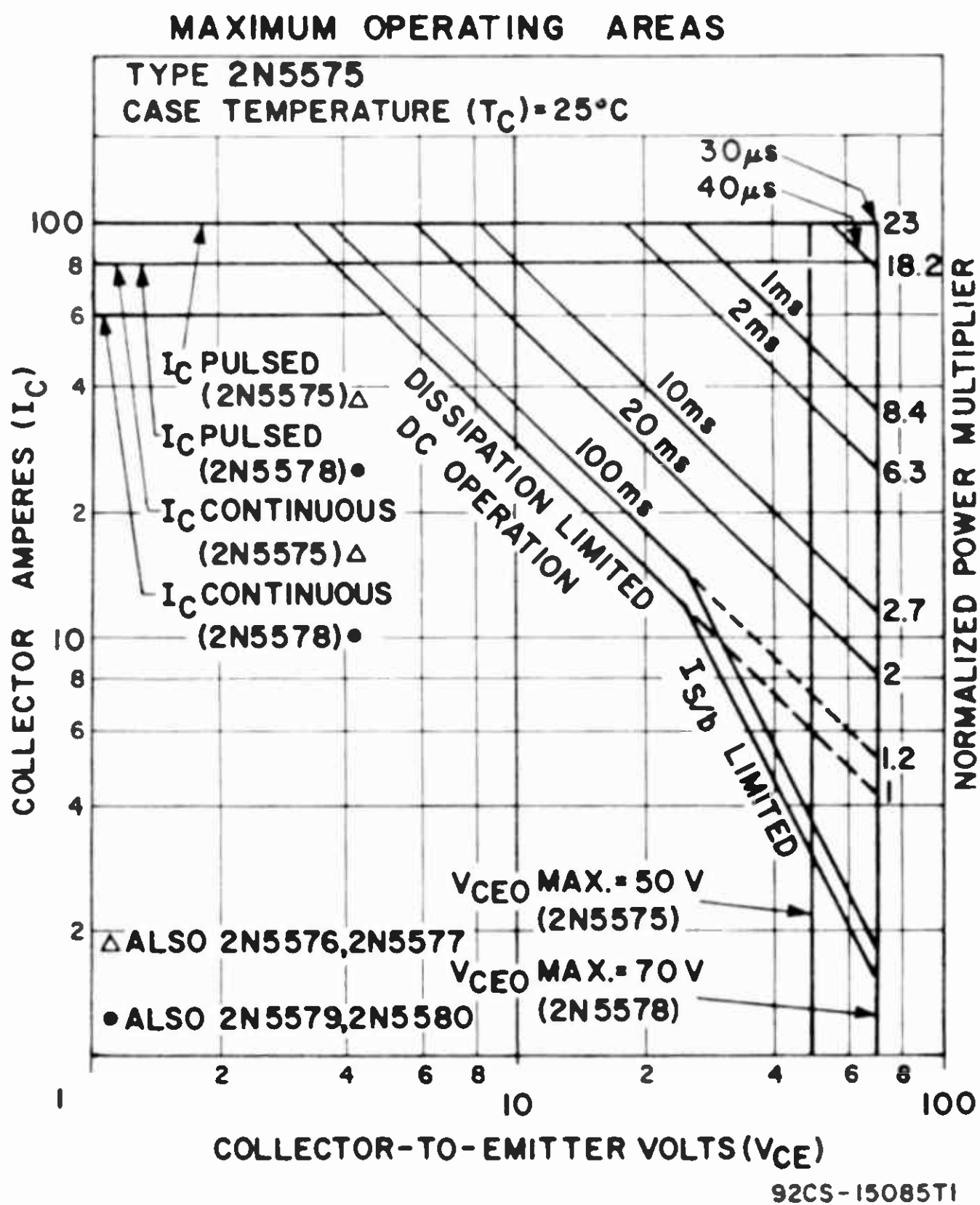


MAXIMUM RATINGS (cont'd)

Emitter-to-Base Voltage	V_{EBO}	8	V
Collector Current	I_C	80	A
Peak Collector Current	i_C	100	A
Base Current	I_B	20	A
Transistor Dissipation:			
T_C up to 25°C, V_{CE} up to 25 V	P_T	300	W
T_C up to 25°C, V_{CE} above 25 V	P_T	See curve page 300	
T_C above 25°C, V_{CE} above 25 V	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 175	°C
Storage	T_{STG}	-65 to 200	°C
Pin-Soldering Temperature (10 s max)	T_P	230	°C

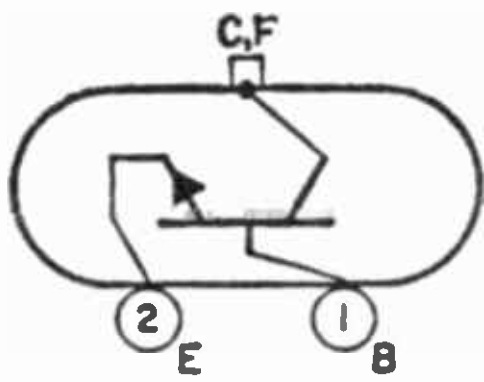
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage:			
$I_C = 0.2$ A	V_{CE0} (sus)	50 min	V
$V_{BE} = -1.5$ V, $I_C = 0.2$ A, $R_{BE} = 10 \Omega$, base-emitter junction reverse biased	V_{CEX} (sus)	70 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 60$ A, $I_B = 6$ A, $t_P \leq 350 \mu s$, $df = 0.02$)	V_{CE} (sat)	2 max	V
Base-to-Emitter Saturation Voltage ($I_C = 60$ A, $I_B = 6$ A, $t_P \leq 350 \mu s$, $df = 0.02$)	V_{BE} (sat)	3 max	V
Base-to-Emitter Voltage ($V_{CE} = 4$ V, $I_C = 60$ A, $t_P \leq 350 \mu s$, $df = 0.02$)	V_{BE}	3 max	V
Collector-Cutoff Current:			
$V_{CE} = 60$ V, $V_{BE} = -1.5$ V, base-emitter junction reverse biased	I_{CEV}	10 max	mA
$V_{CE} = 50$ V, $R_{BE} = 10 \Omega$	I_{CER}	5 max	mA
$V_{CE} = 60$ V, $V_{BE} = -1.5$ V, $T_C = 150^\circ C$, base-emitter junction reverse biased	I_{CEV}	20 max	mA
Emitter-Cutoff Current ($V_{EB} = 8$ V)	I_{EBO}	10 max	mA
Pulsed Static Forward-Current Transfer Ratio			
($V_{CE} = 4$ V, $I_C = 60$ A, $t_P \leq 350 \mu s$, $df = 0.02$)	h_{FE} (pulsed)	10 to 40	
Output Capacitance ($V_{CB} = 10$ V, $I_E = 0$)	C_{obo}	2000 max	pF
Input Capacitance ($V_{EB} = 0.5$ V, $I_C = 0$)	C_{ibo}	4000 max	pF
Gain-Bandwidth Product ($V_{CE} = 4$ V, $I_C = 10$ A) ...	f_T	400 to 2000	kHz
Second-Breakdown Collector Current ($V_{CE} = 25$ V, non-repetitive pulse = 1 s, base forward biased) ...	$I_{S/b}$	12 min	A
Second Breakdown Energy ($V_{BE} = -1.5$ V, $I_C = 7$ A, $R_{BE} = 10 \Omega$, $L = 33$ mH, base reverse biased)	$E_{S/b}$	0.8 min	J
Thermal Resistance, Junction-to-Case	θ_{J-C}	0.5 max	°C/W



POWER TRANSISTOR

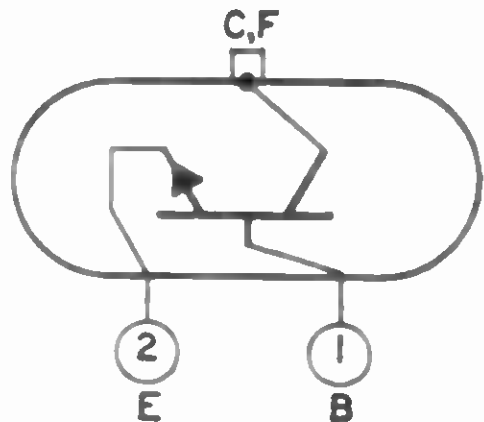
2N5576



Si n-p-n type features a base comprised of a homogeneous silicon material. It is used in high-power linear and switching applications in military, industrial, and commercial equipment. Outline No.56. This type is electrically identical with type 2N5575.

POWER TRANSISTOR

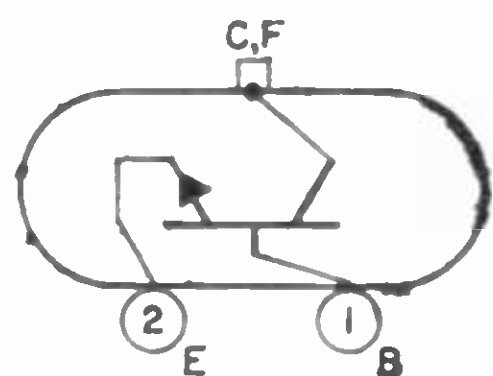
2N5577



Si n-p-n type features a base comprised of a homogeneous silicon material. It is used in high-power linear and switching applications in military, industrial, and commercial equipment. Outline No.57. This type is electrically identical with type 2N5575.

POWER TRANSISTOR

2N5578

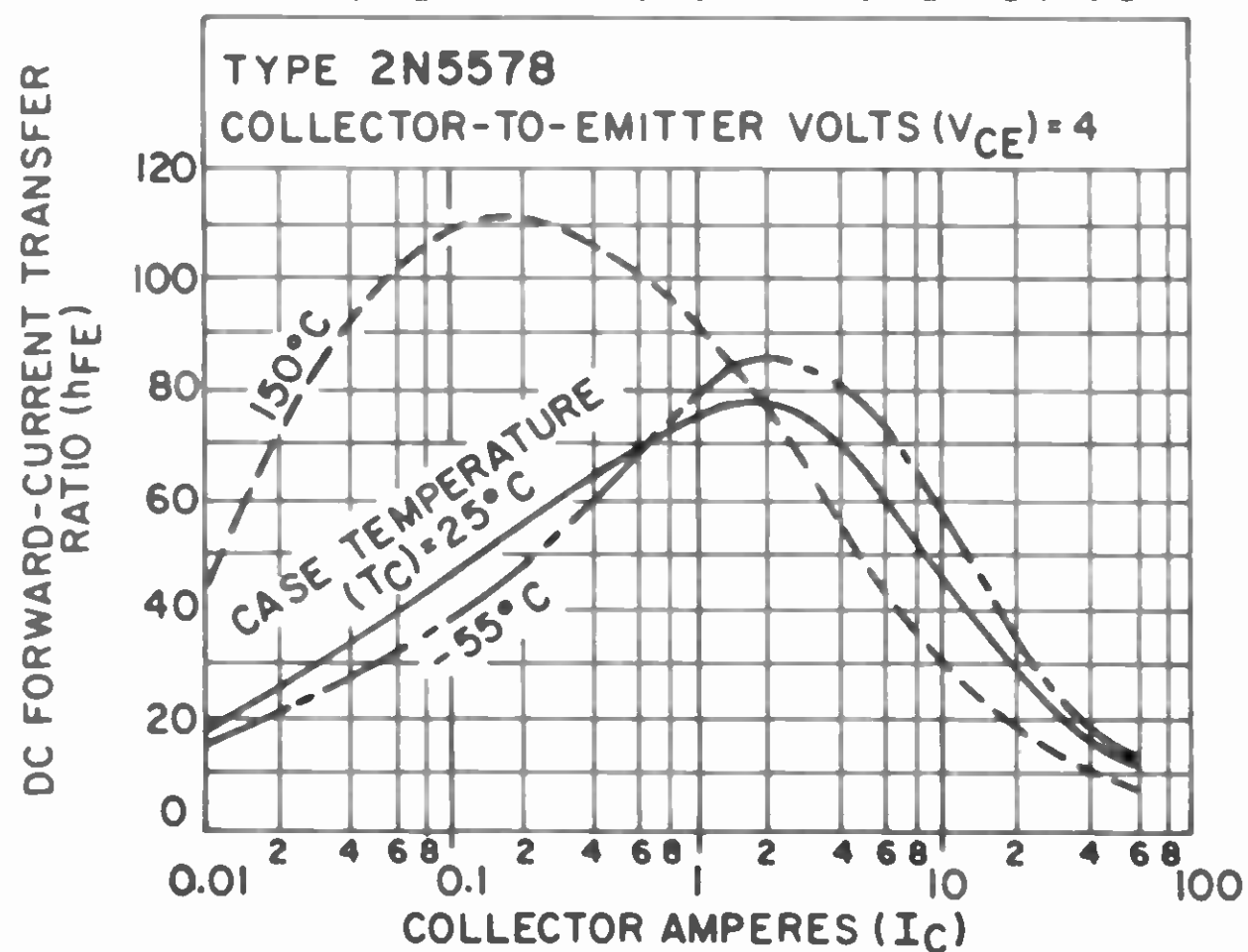


Si n-p-n type features a base comprised of a homogeneous-resistivity silicon material. It is used in high-power linear and switching applications in military, industrial, and commercial equipment. Outline No.55. For maximum operating area curves, refer to type 2N5575.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	90	V
Collector-to-Emitter Sustaining Voltage: $R_{BE} = 10 \Omega, V_{BE} = -1.5 V$	$V_{CEX(sus)}$	90	V
Base open	$V_{CEO(sus)}$	70	V
Emitter-to-Base Voltage	V_{EBO}	8	V
Collector Current	I_C	60	A
Peak Collector Current	i_C	80	A
Base Current	I_B	15	A
Transistor Dissipation:			
T_c up to 25°C, V_{CE} up to 25 V	P_T	300	W
T_c up to 25°C, V_{CE} above 25 V	P_T	See curve page 300	
T_c above 25°C, V_{CE} above 25 V	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 175	°C
Storage	T_{STG}	-65 to 200	°C
Pin-Soldering Temperature (10 s max)	T_P	230	°C

TYPICAL DC FORWARD CURRENT TRANSFER-RATIO CHARACTERISTICS



92CS-15074T1

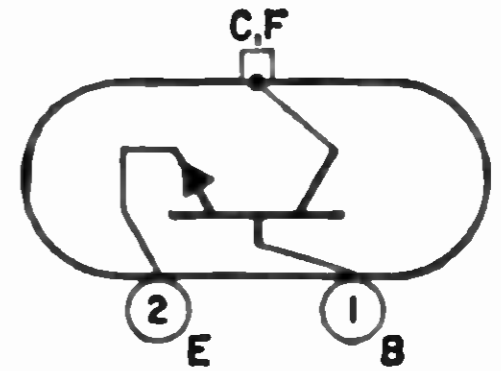
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage: $I_C = 0.2 \text{ A}$	$V_{CEO(sus)}$	70 min	V
$V_{BE} = -1.5 \text{ V}$, $I_C = 0.2 \text{ A}$, $R_{BE} = 10 \Omega$, base-emitter junction reverse biased	$V_{CEX(sus)}$	90 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 40 \text{ A}$, $I_B = 4 \text{ V}$, $t_P \leq 350 \mu\text{s}$, $df = 0.02$)	$V_{CE(sat)}$	1.5 max	V
Base-to-Emitter Saturation Voltage ($I_C = 40 \text{ A}$, $I_B = 4 \text{ V}$, $t_P \leq 350 \mu\text{s}$, $df = 0.02$)	$V_{BE(sat)}$	2.5 max	V
Base-to-Emitter Voltage ($V_{CE} = 4 \text{ V}$, $I_C = 40 \text{ V}$, $t_P \leq 350 \mu\text{s}$, $df = 0.02$)	V_{BE}	2.5 max	V
Collector-Cutoff Current: $V_{CE} = 80 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, base-emitter junction reverse biased	I_{CEV}	10 max	mA
$V_{CE} = 70 \text{ V}$, $R_{BE} = 10 \Omega$	I_{CER}	5 max	mA
$V_{CE} = 80 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_C = 150^\circ\text{C}$, base-emitter junction reverse biased	I_{CEV}	20 max	mA
Emitter-Cutoff Current ($V_{EB} = 8 \text{ V}$)	I_{EBO}	10 max	mA
Pulsed Static Forward-Current Transfer Ratio ($V_{CE} = 4 \text{ V}$, $I_C = 40 \text{ A}$, $t_P \leq 350 \mu\text{s}$, $df = 0.02$)	$h_{FE}(\text{pulsed})$	10 to 40	
Output Capacitance ($V_{CB} = 10 \text{ V}$, $I_E = 0$)	C_{obo}	2000max	pF
Input Capacitance ($V_{EB} = 0.5 \text{ V}$, $I_C = 0$)	C_{ibo}	4000 max	pF
Gain-Bandwidth Product ($V_{CE} = 4 \text{ V}$, $I_C = 10 \text{ A}$)	f_T	400 to 2000	kHz
Second-Breakdown Collector Current ($V_{CE} = 25 \text{ V}$, non-repetitive pulse = 1 s, base forward biased)	$I_{S/b}$	12 min	A
Second Breakdown Energy ($V_{BE} = -1.5 \text{ V}$, $I_C = 7 \text{ A}$, $R_{BE} = 10 \Omega$, $L = 33 \text{ mH}$, base reverse biased)	$E_{S/b}$	0.8 min	J
Thermal Resistance, Junction-to-Case	θ_{J-C}	0.5 max	$^\circ\text{C/W}$

2N5579

POWER TRANSISTOR

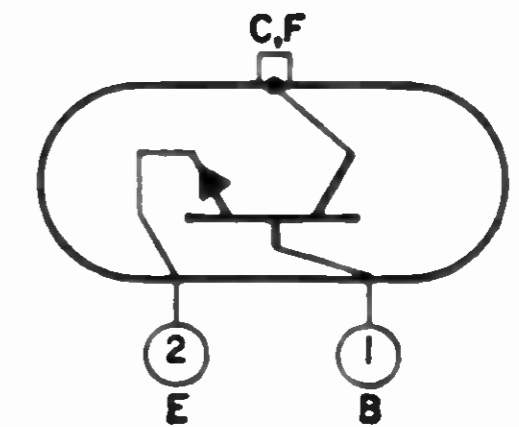
Si n-p-n type features a base comprised of a homogeneous-resistivity silicon material. It is used in high-power linear and switching applications in military, industrial, and commercial equipment. Outline No.56. This type is electrically identical to type 2N5578.



2N5580

POWER TRANSISTOR

Si n-p-n type features a base comprised of a homogeneous-resistivity silicon material. It is used in high-power linear and switching applications in military, industrial, and commercial equipment. Outline No.57. This type is electrically identical to type 2N5578.



3N98

Refer to Chart of Discontinued Transistors

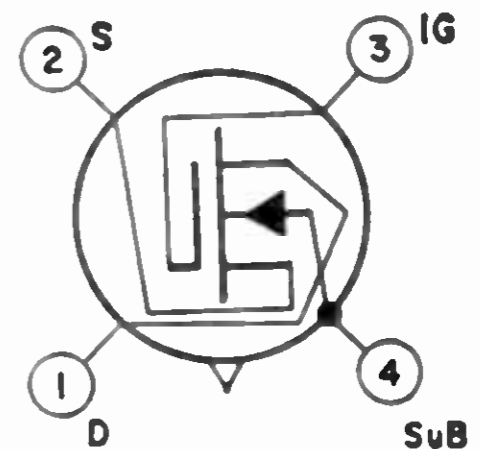
3N99

Refer to Chart of Discontinued Transistors

3N128

FIELD-EFFECT TRANSISTOR

Si insulated-gate field-effect (MOS) n-channel depletion type used in vhf amplifier service in military and industrial applications. JEDEC TO-72, Outline No.28.



MAXIMUM RATINGS

Drain-to-Source Voltage	V_{DS}	20	V
Gate-to-Source Voltage:			
Continuous (dc)	V_{GS}	-8 to 1	V
Peak (ac)	V_{GS}	± 15	V
Drain Current ($t_P \leq 20 \text{ ms}$, $df \leq 0.15$)	$I_D(\text{pulsed})$	50	mA
Transistor Dissipation:			
T_A up to 25°C	P_T	400	mW
T_A above 25°C	P_T	Derate at 2.67	$\text{mW}/^\circ\text{C}$

MAXIMUM RATINGS (cont'd)

Temperature Range:			
Operating	T(opr)	-65 to 175	°C
Storage	T _{STG}	-65 to 175	°C
Lead-Soldering Temperature (10 s max)	T _L	265	°C

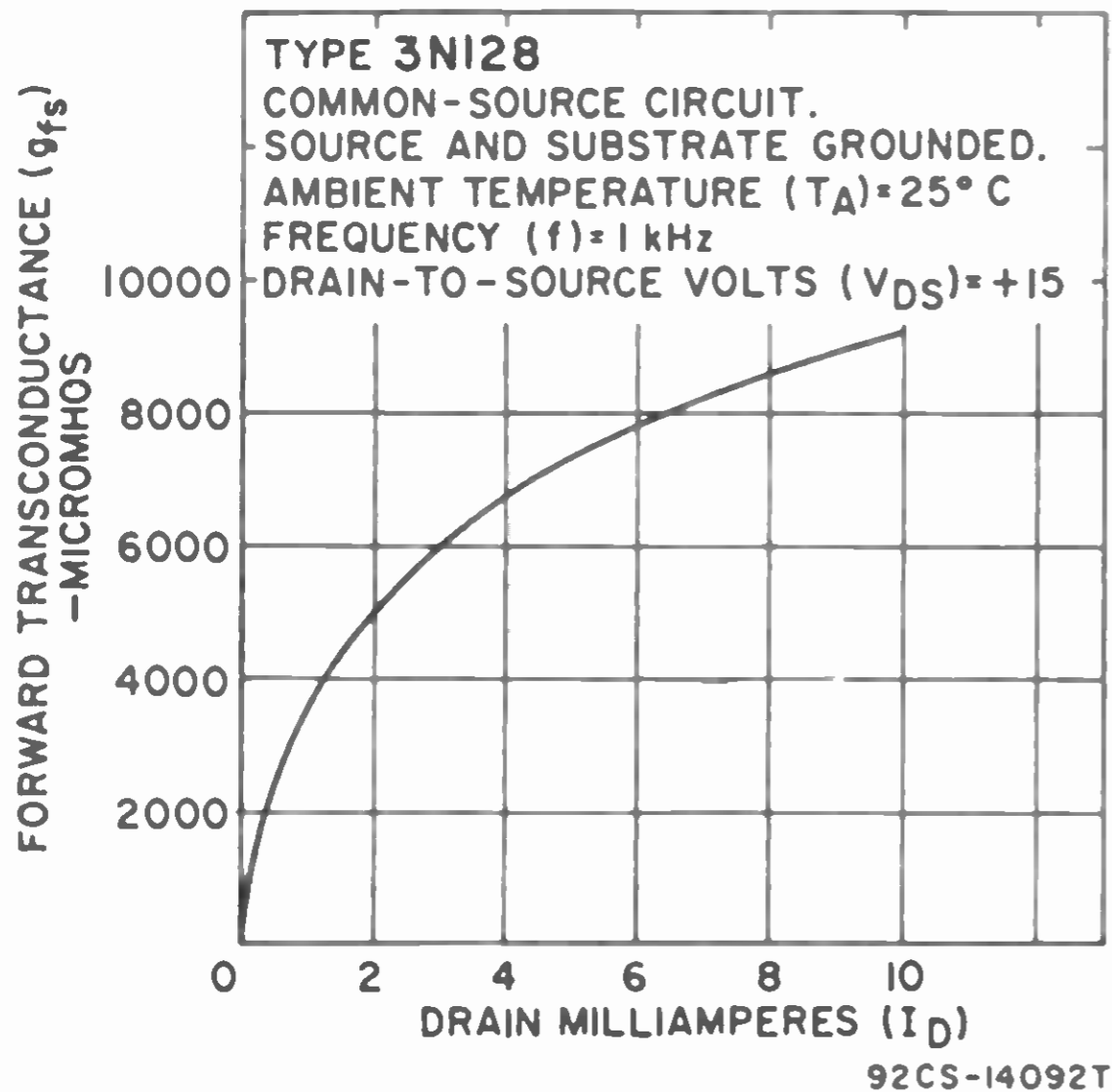
CHARACTERISTICS

Gate Leakage Current:			
V _{GS} = -8 V, V _{DS} = 0	I _{GSS}	0.1 typ; 50 max	pA
V _{GS} = -8 V, V _{DS} = 0, T _A = 125°C	I _{GSS}	5 max	nA
Zero-Bias Drain Current (V _{DS} = 15 V, V _{GS} = 0, t _p = 20 ms (max), df ≤ 0.15)	I _{DSS} (pulsed)	5 to 25	mA
Drain-to-Source Cutoff (V _{DS} = 20 V, V _{GS} = -8 V)	I _D (off)	50 max	μA
Small-Signal Input Capacitance (V _{DS} = 15 V, I _D = 5 mA, f = 0.1 to 1 MHz) ...	C _{iss}	5.5 typ; 7 max	pF
Small-Signal Reverse Transfer Capacitance† (V _{DS} = 15 V, I _D = 5 mA, f = 0.1 to 1 MHz) ...	C _{rss}	0.12 typ; 0.20 max	pF
Small-Signal Output Capacitance (V _{DS} = 15 V, I _D = 5 mA, f = 0.1 to 1 MHz) ...	C _{oss}	1.4	pF
Gate Leakage Resistance (V _{DS} = 0, V _{GS} = -8 V)	R _{GS}	10 ¹⁴	Ω
Drain-to-Source Channel Resistance (V _{DS} = 0, V _{GS} = 0, f = 1 kHz)	r _{DS} (on)	200	Ω
Gate-to-Source Cutoff Voltage (V _{DS} = 15 V, I _D = 50 μA)	V _{GS} (off)	-2 to -8	V
Forward Transconductance:			
V _{DS} = 15 V, V _{GS} = 0, f = 1 kHz	g _{fs}	10000 [▲]	μmhos
V _{DS} = 15 V, I _D = 5 mA, f = 1 kHz	g _{fs}	5000 to 12000	μmhos
Magnitude of Forward Transadmittance (V _{DS} = 15 V, I _D = 5 mA, f = 200 MHz)	Y _{fs}	5000 min; 7500 typ	μmhos
Maximum Available Power Gain (V _{DS} = 15 V, I _D = 5 mA, f = 200 MHz)	MAG	15 min; 20 typ [▲]	dB
Maximum Usable Power Gain, Neutralized (V _{DS} = 15 V, I _D = 5 mA, f = 200 MHz)	MUG	13.5 min; 16 typ [▲]	dB
Noise Figure (V _{DS} = 15 V, I _D = 5 mA, f = 200 MHz)	NF	3.5 typ; 5 max [▲]	dB

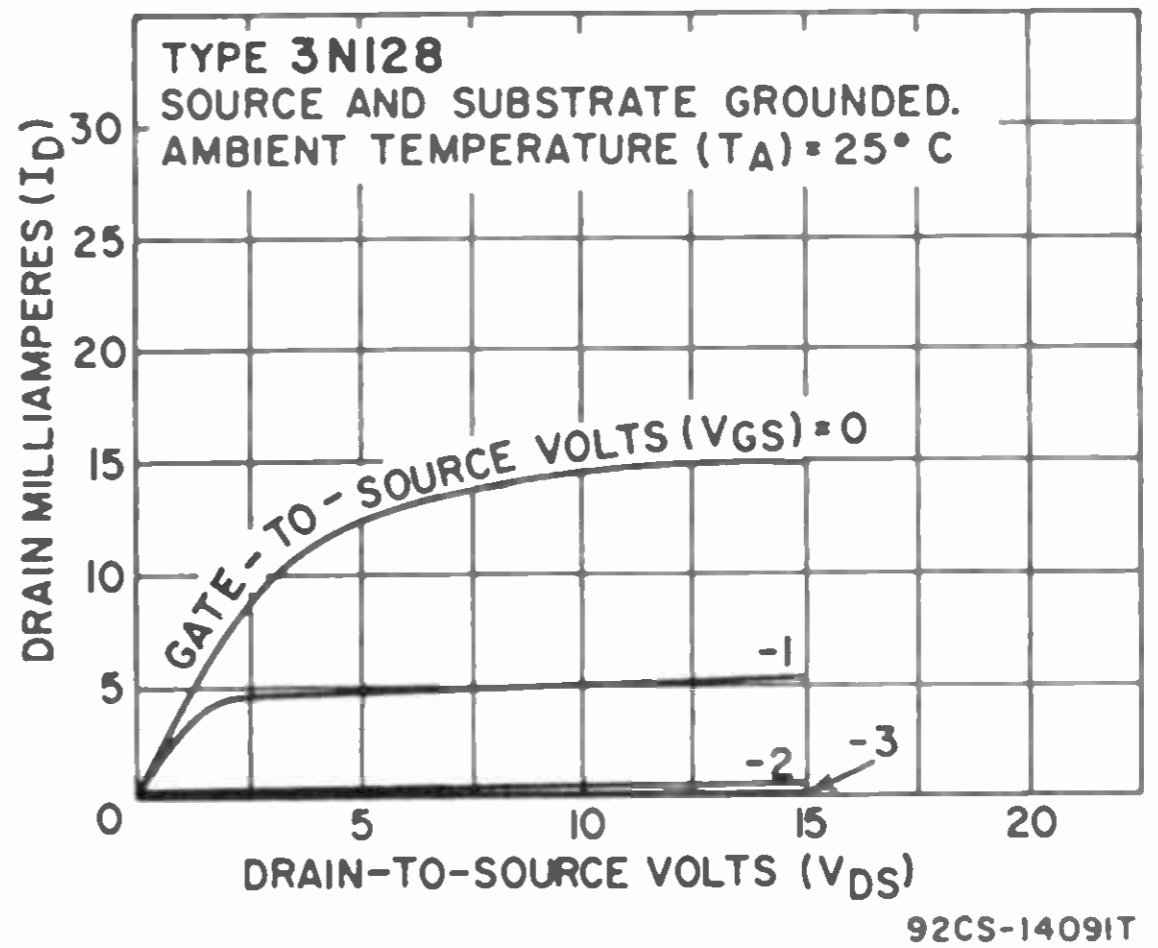
† Three terminal measurement with source returned to guard terminal.

▲ This characteristic does not apply to type 3N143.

TYPICAL FORWARD TRANSCONDUCTANCE CHARACTERISTIC

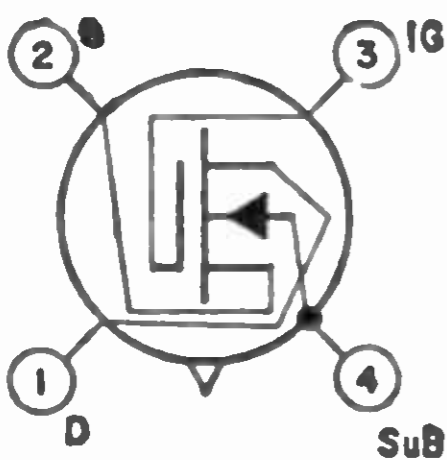


TYPICAL DRAIN CHARACTERISTICS



FIELD-EFFECT TRANSISTOR **3N138**

Si insulated-gate field-effect (MOS) n-channel depletion type used in critical chopper applications and multiplex service up to 60 MHz. The terminal arrangement permits shielding between input and output terminals for superior high-frequency performance and greater circuit stability, particularly on printed-circuit boards.



JEDEC TO-72, Outline No.28.

MAXIMUM RATINGS

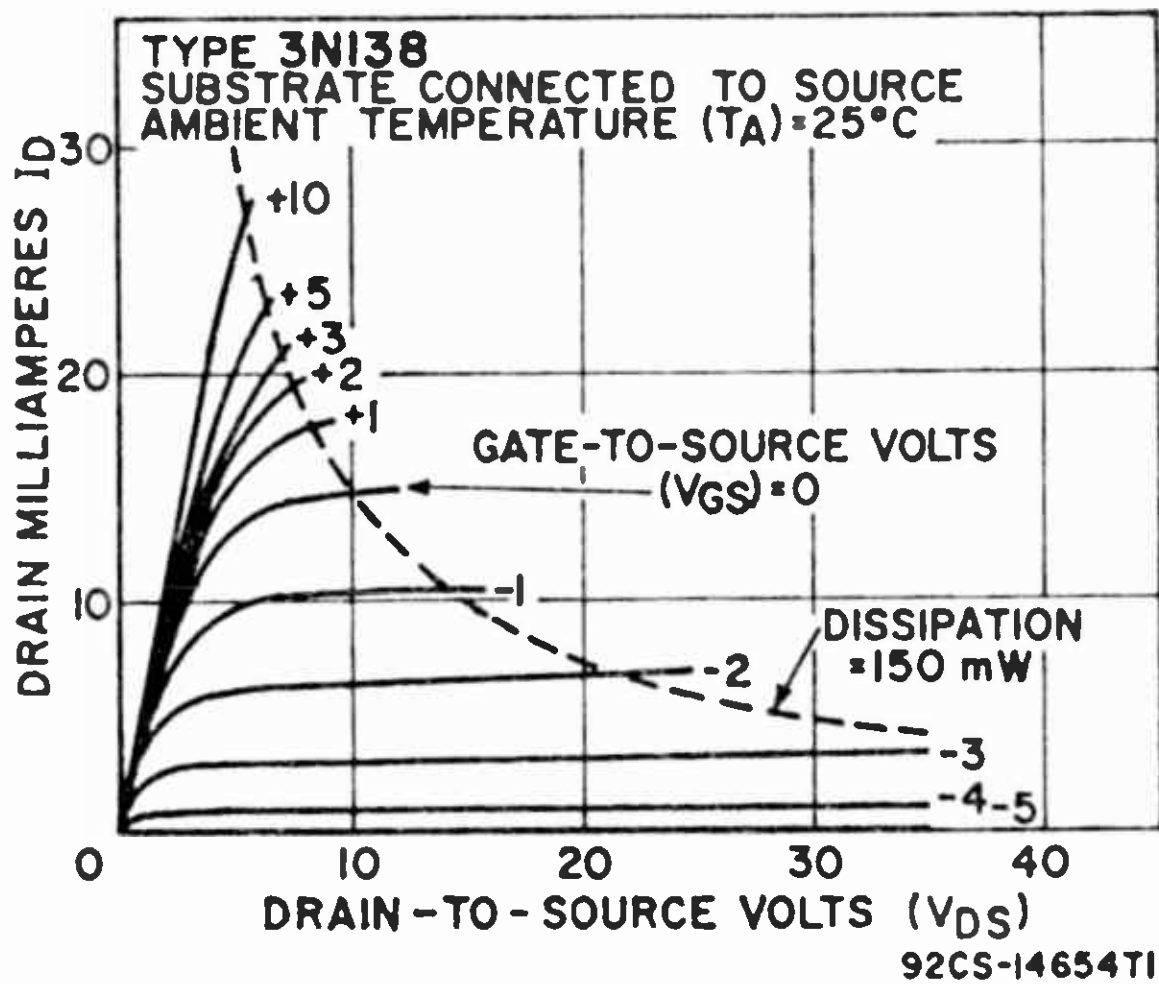
Drain-to-Source Voltage	V_{DS}	35	V
Drain-to-Substrate Voltage	V_{DB}	-0.3 to 35	V
Source-to-Substrate Voltage	V_{SB}	-0.3 to 35	V
Gate-to-Source Voltage:			
Continuous	V_{GS}	± 10	V
Peak	V_{GS}	± 14	V
Peak Voltage, Gate-to-All Other Terminals, V_{GS} , V_{GD} , V_{GB} , non-repetitive		± 45	V
Drain Current ($t_P \leq 20$ ms, $df \leq 0.10$)	I_D (pulsed)	50	mA
Transistor Dissipation (T_A from -65 to 125°C)	P_T	150	mW
Temperature Range:			
Operating	T (opr)	-65 to 125	°C
Storage	T_{STG}	-65 to 150	°C
Lead-Soldering Temperature (10 s max)	T_L	265	°C

CHARACTERISTICS

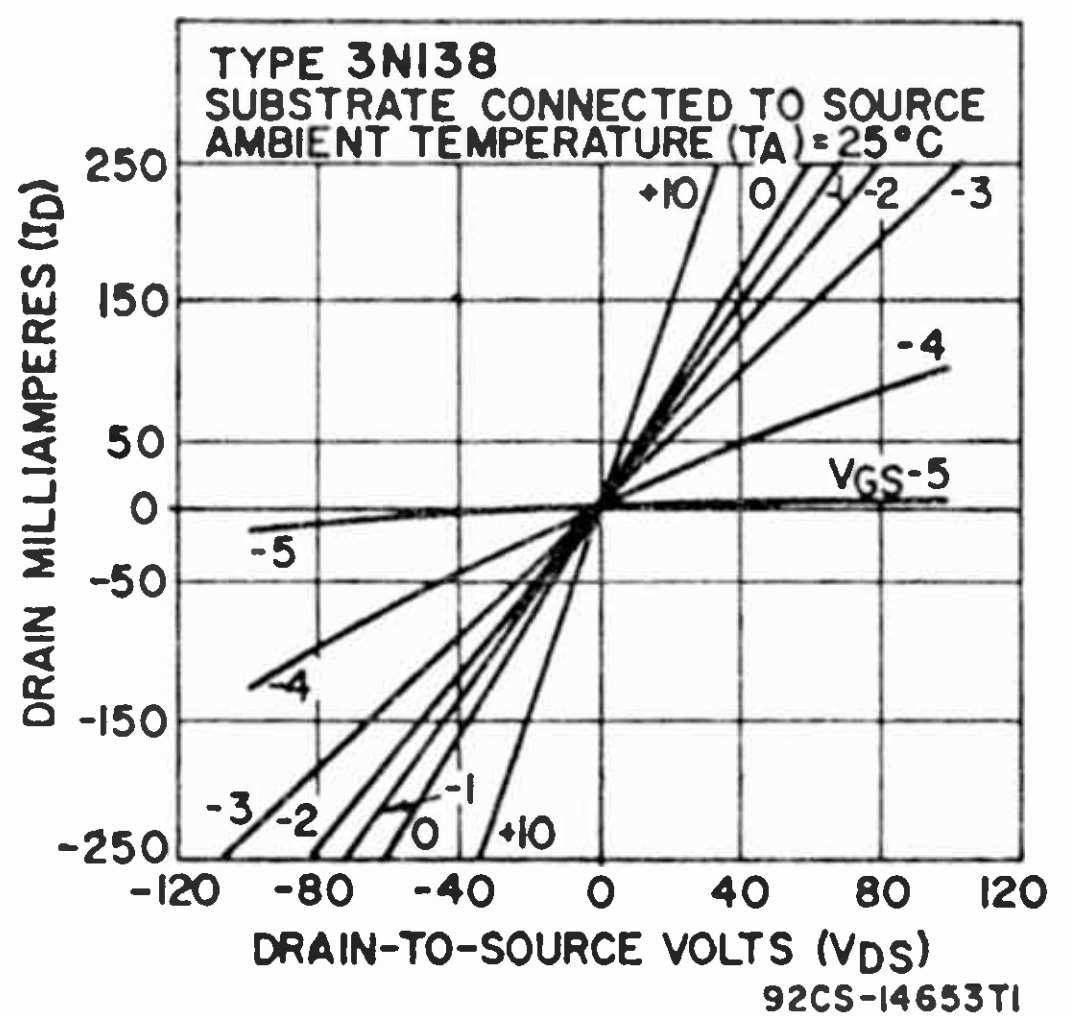
Gate-Leakage Current:			
$V_{GS} = \pm 10$ V, $V_{DS} = 0$	I_{GSS}	0.1 typ; 10 max	pA
$V_{GS} = \pm 10$ V, $V_{DS} = 0$, $T_A = 125^\circ\text{C}$	I_{GSS}	20 typ; 200 max	pA
Drain-to-Source "ON" Resistance:			
$V_{GS} = 0$, $V_{DS} = 0$, $f = 1$ kHz	$r_{DS}(on)$	240 typ; 300 max	Ω
$V_{GS} = 10$ V, $V_{DS} = 0$, $f = 1$ kHz	$r_{DS}(on)$	135	Ω
$V_{GS} = 0$, $V_{DS} = 0$, $f = 1$ kHz, $T_A = 125^\circ\text{C}$	$r_{DS}(on)$	350	Ω
Drain-to-Source "OFF" Resistance ($V_{GS} = -10$ V, $V_{DS} = 1$ V)	$R_{DS}(off)$	2×10^8 min; 10^{10} typ	Ω
Drain-to-Source Cutoff Current:			
$V_{GS} = -10$ V, $V_{DS} = 1$ V	$I_D(off)$	0.01 typ; 0.5 max	nA
$V_{GS} = -10$ V, $V_{DS} = 1$ V, $T_A = 125^\circ\text{C}$	$I_D(off)$	0.01 typ; 0.5 max	μA
Small-Signal, Reverse Transfer Capacitance ($V_{GS} = -10$ V, $V_{DS} = 0$, $f = 1$ MHz)	C_{rss}	0.18 typ; 0.25 max	pF
Small-Signal Input Capacitance ($V_{GS} = -10$ V, $V_{DS} = 0$, $f = 1$ MHz)	C_{iss}	3 typ; 5 max	pF
Zero-Gate Bias Forward Transconductance ($V_{GS} = 0$, $V_{DS} = 12$ V)	g_{fs}	6000	μmhos
Offset Voltage ($V_{GS} = \pm 10$ V, $V_{DS} = 0$)	V_O	0 \ddagger	V

\ddagger In measurements of offset voltage, thermocouple effects and contact potentials in the measurement setup may cause erroneous readings of 1 microvolt or more. These errors may be minimized by the use of solder having a low thermal e.m.f., such as Leeds & Northrup No. 107-1.0.1, or equivalent.

TYPICAL DRAIN CHARACTERISTICS

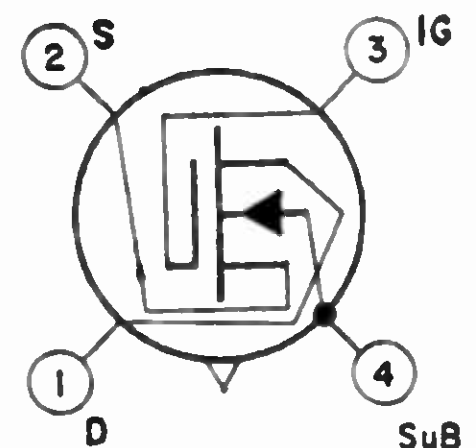


TYPICAL LOW-LEVEL DRAIN CHARACTERISTICS



3N139 FIELD-EFFECT TRANSISTOR

Si insulated-gate field-effect (MOS) n-channel depletion type used in audio, video, and rf amplifier applications. The terminal arrangement permits shielding between input and output terminals for superior high-frequency performance and greater circuit stability, particularly on printed-circuit boards. JEDEC TO-72, Outline No.28.



MAXIMUM RATINGS

Drain-to-Source Voltage	V _{DS}	35	V
Drain-to-Substrate Voltage	V _{DB}	-0.3 to 35	V
Source-to-Substrate Voltage	V _{SB}	-0.3 to 35	V
Gate-to-Source Voltage:			
Continuous	V _{GS}	±10	V
Peak	V _{GS}	±14	V
Peak Voltage, Gate-to-All Other Terminals; V _{GS} , V _{GD} , V _{GB} , non-repetitive		±42	V
Drain Current (t _P ≤ 20 ms, df ≤ 0.10)	I _D (pulsed)	50	mA
Transistor Dissipation (T _A from -65 to 125°C) ...	P _T	150	mW
Temperature Range:			
Operating	T (opr)	-65 to 125	°C
Storage	T _{STG}	-65 to 150	°C
Lead-Soldering Temperature (10 s max)	T _L	265	°C

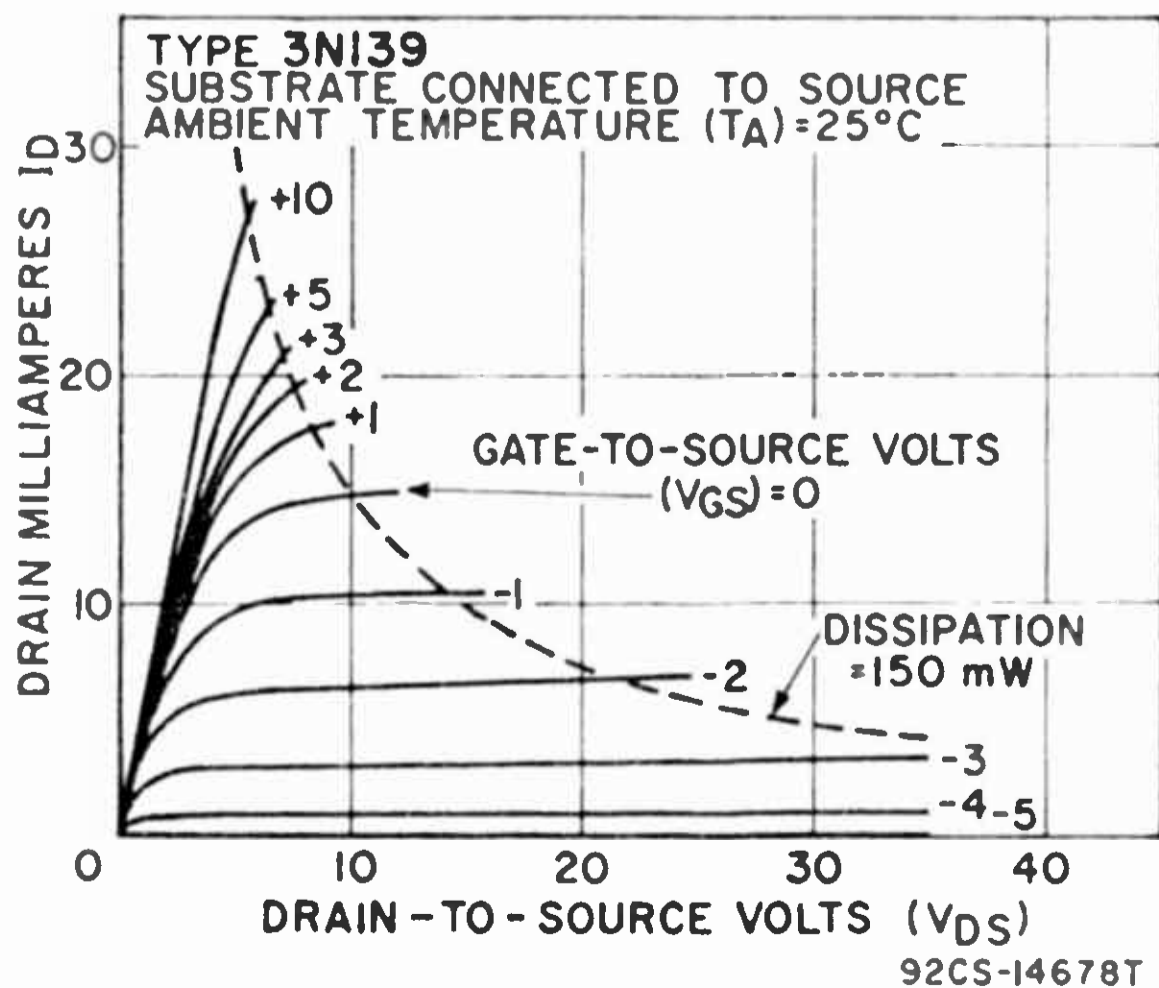
CHARACTERISTICS

Gate Leakage Current:			
V _{GS} = ±10 V, V _{DS} = 0	I _{GSS}	0.1 typ; 1 max	nA
V _{GS} = ±10 V, V _{DS} = 0, T _A = 125°C	I _{GSS}	4 max	nA
Forward Transconductance:			
V _{DS} = 15 V, R _S = 0, f = 1 kHz	g _{fs}	3000 min; 6000 typ	μmhos
V _{DD} = 15 V, R _S = 360 Ω, f = 1 kHz	g _{fs}	3000 to 7500	μmhos
V _{DD} = 15 V, R _S = 360 Ω, f = 1 kHz, T _A = 125°C	g _{fs}	3300	μmhos
Zero-Bias Drain Current (V _{DS} = 15 V, R _S = 0, t _P = 300 μs, df ≤ 0.10)	I _{DSS} (pulsed)	5 to 25	mA
Drain Current:			
V _{DD} = 15 V, R _S = 360 Ω	I _D	3 to 7	mA
V _{DD} = 15 V, R _S = 360 Ω, T _A = 125°C	I _D	3.3	mA
Output Resistance:			
V _{DS} = 15 V, R _S = 0, f = 1 kHz	r _d	5	kΩ
V _{DD} = 15 V, R _S = 360 Ω, f = 1 kHz	r _d	20	kΩ
V _{DD} = 15 V, R _S = 360 Ω, f = 1 kHz, T _A = 125°C	r _d	23	kΩ
Drain-to-Source Cutoff Current:			
V _{DS} = 15 V, V _{GS} = -6 V	I _{DS} (off)	1 typ; 50 max	μA
V _{DS} = 15 V, V _{GS} = -6 V, T _A = 125°C	I _{DS} (off)	2	μA
V _{DS} = 35 V, V _{GS} = -6 V	I _{DS} (off)	75 max	μA
Equivalent Input Noise Voltage:			
V _{DS} = 15 V, R _S = 0, R _G = 0, f = 1 kHz	e _n	0.06	μV√Hz
V _{DD} = 15 V, R _S = 360 Ω, R _G = 0, f = 1 kHz ...	e _n	0.06	μV√Hz
Audio Spot Noise Figure† (V _{DD} = 15 V, R _S = 360 Ω, R _G = 1 MΩ, f = 1 kHz)	NF	0.86	dB
Small-Signal Input Capacitance:			
V _{DS} = 15 V, R _S = 0, f = 1 MHz	C _{iss}	3.3	pF
V _{DD} = 15 V, R _S = 360 Ω, f = 1 MHz	C _{iss}	3 typ; 7 max	pF
Small-Signal Reverse Transfer Capacitance:			
V _{DS} = 15 V, R _S = 0, f = 1 MHz	C _{rss}	0.21	pF
V _{DD} = 15 V, R _S = 360 Ω, f = 1 MHz	C _{rss}	0.19 typ; 0.30 max	pF
Power Gain (V _{DD} = 15 V, R _S = 360 Ω, f = 200 MHz)	G _{ps}	15 min; 17 typ	dB
Noise Figure (V _{DD} = 15 V, R _S = 360 Ω, f = 200 MHz)	NF	4 typ; 6 max	dB

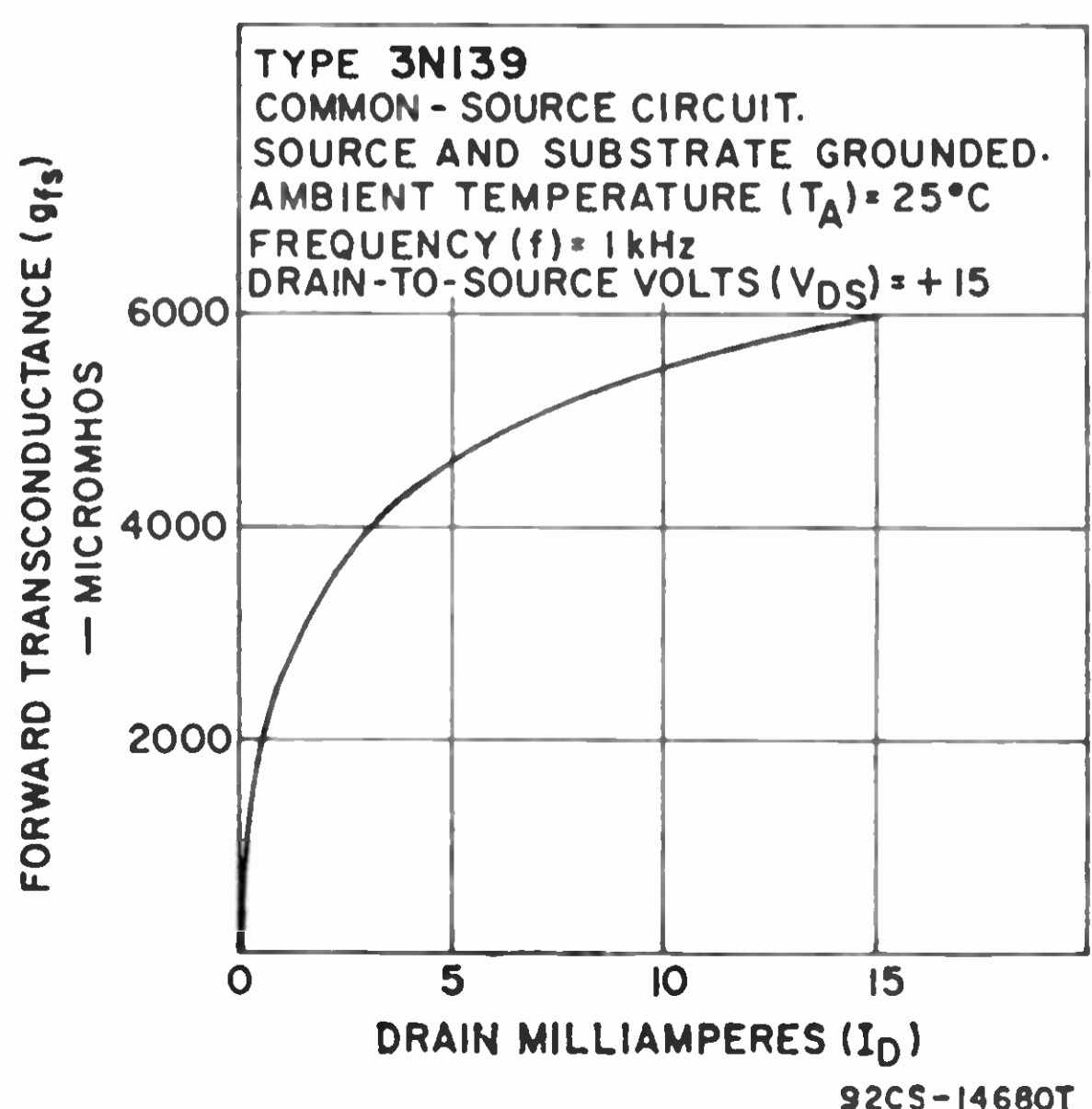
$$\ddagger \text{ Noise Figure} = 10 \log_{10} \left[1 + \frac{e_n^2}{4 KT BW R_g} \right]$$

where: K = 1.38 × 10⁻²³, T = Temperature in °Kelvin, BW = Bandwidth in Hz,
R_g = Generator Resistance

TYPICAL DRAIN CHARACTERISTICS

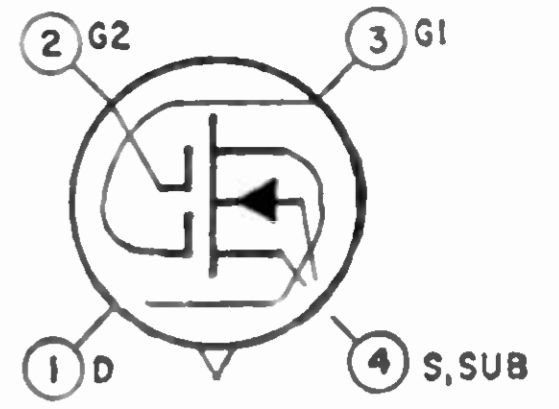


TYPICAL FORWARD TRANSCONDUCTANCE CHARACTERISTICS



3N140 FIELD-EFFECT TRANSISTOR

Si dual insulated-gate field-effect (MOS) n-channel depletion type used in rf amplifier applications at frequencies up to 300 MHz. JEDEC TO-72, Outline No.28.

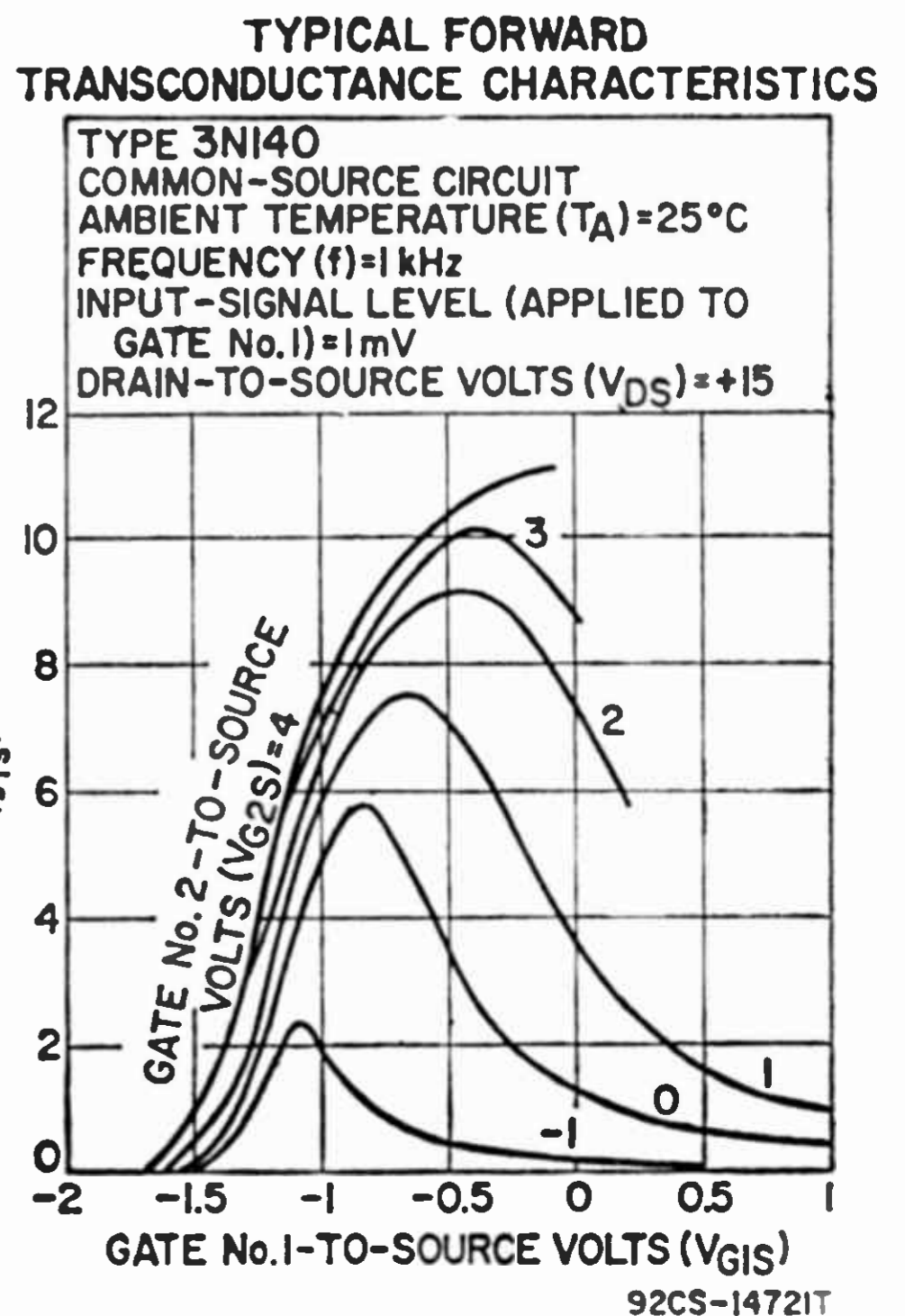
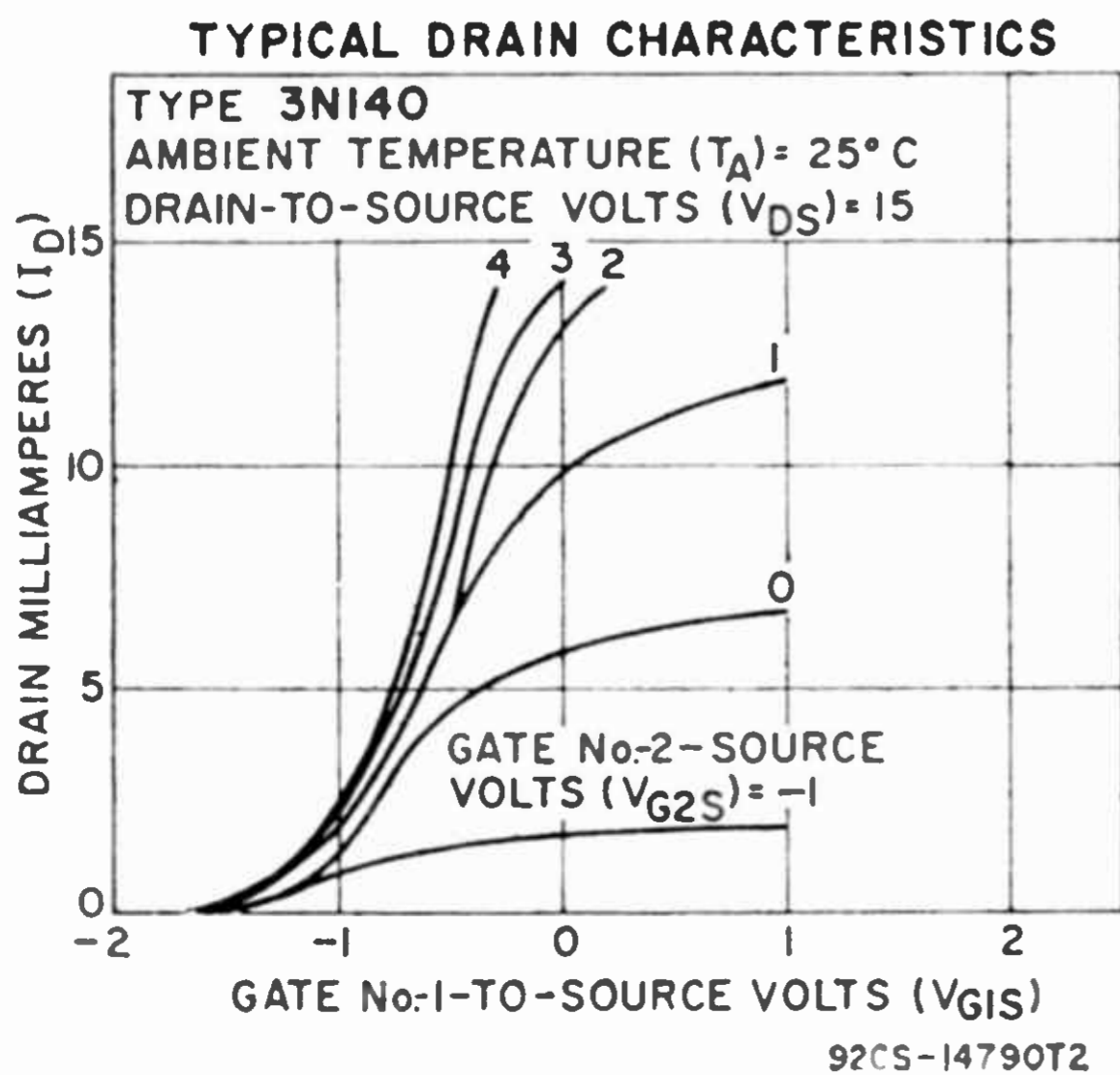


MAXIMUM RATINGS

Drain-to-Source Voltage	V_{DS}	0 to 20	V
Gate-No.1-to-Source Voltage:			
Continuous (dc)	V_{G1S}	-8 to 1	V
Peak (ac)	V_{G1S}	-8 to 20	V
Gate-No.2-to-Source Voltage:			
Continuous (dc)	V_{G2S}	-8 to (0.4 of V_{DS})	V
Peak (ac)	V_{G2S}	-8 to 20	V
Drain-to-Gate-No.1 Voltage	V_{DG1}	20	V
Drain-to-Gate-No.2 Voltage	V_{DG2}	20	V
Drain Current ($t_P \leq 20$ ms, $df \leq 0.15$)	I_D (pulsed)	50	mA
Transistor Dissipation:			
T_A up to 25°C	P_T	400	mW
T_A above 25°C	P_T	Derate linearly at 2.67	mW/°C
Temperature Range:			
Operating	T (opr)	-65 to 175	°C
Storage	T_{STG}	-65 to 175	°C
Lead-Soldering Temperature (10 s max)	T_L	265	°C

CHARACTERISTICS

Gate-No.1-to-Source Cutoff Voltage ($V_{DS} = 16$ V, $V_{G2S} = 4$ V, $I_D = 200$ μ A)	V_{G1S} (off)	-2 typ; -4 max	V
Gate-No.2-to-Source Cutoff Voltage ($V_{DS} = 16$ V, $V_{G1S} = 0$, $I_D = 200$ μ A)	V_{G2S} (off)	-2 typ; -4 max	V
Gate-No.1 Leakage Current:			
$V_{G1S} = -20$ V, $V_{G2S} = 0$, $V_{DS} = 0$	I_{G1SS}	1 max	nA
$V_{G1S} = 1$ V, $V_{G2S} = 0$, $V_{DS} = 0$	I_{G1SS}	1 max	nA
$V_{G1S} = -20$ V, $V_{G2S} = 0$, $V_{DS} = 0$, $T_A = 125^\circ\text{C}$	I_{G1SS}	0.2 max	μ A
Gate-No.2 Leakage Current:			
$V_{G2S} = -20$ V, $V_{G1S} = 0$, $V_{DS} = 0$	I_{G2SS}	1 max	nA
$V_{G2S} = 1$ V, $V_{G1S} = 0$, $V_{DS} = 0$	I_{G2SS}	1 max	nA
$V_{G2S} = -20$ V, $V_{G1S} = 0$, $V_{DS} = 0$, $T_A = 125^\circ\text{C}$	I_{G2SS}	0.2 max	μ A
Zero-Bias Drain Current ($V_{DD} = 14$ V, $V_{G1S} = 0$, $V_{G2S} = 4$ V, $t_P \leq 20$ ms, $df \leq 0.15$)	I_{DSS} (pulsed)	5 to 30	mA
Forward Transconductance, Gate-No.1 to Drain ($V_{DD} = 14$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, $f = 1$ kHz)	g_{fs}	6000 to 18000	μ mhos
Cutoff Forward Transconductance, Gate-No.1 to Drain ($V_{DD} = 14$ V, $V_{G1S} = 0.5$ V, $V_{G2S} = -2$ V, $f = 1$ kHz)	g_{fs} (off) †	100 max	μ mhos
Small-Signal Input Capacitance* ($V_{DS} = 13$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, $f = 1$ MHz)	C_{iss}	3 to 7	pF

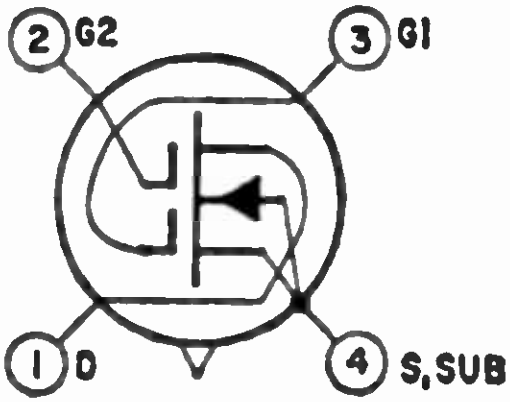


CHARACTERISTICS (cont'd)

Small-Signal Reverse Transfer Capacitance, Drain to Gate-No.1 [▲] ($V_{DS} = 13$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, $f = 1$ MHz)	C_{rss}	0.01 to 0.03	pF
Small-Signal Output Capacitance ($V_{DS} = 13$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, $f = 1$ MHz)	C_{oss}	2.2	pF
Power Gain ($V_{DD} = 15$ V, $R_S = 270$ Ω , $R_G = 50$ Ω , $f = 200$ MHz)	$G_{ps}\ddagger$	16 min; 18 typ	dB
Noise Figure ($V_{DD} = 15$ V, $R_S = 270$ Ω , $R_G = 50$ Ω , $f = 200$ MHz)	NF \ddagger	3.5 typ; 4.5 max	dB

• Capacitance between gate No.1 and all other terminals.
[▲] Three-terminal measurement with gate No.2 and source returned to guard terminal.
 \ddagger This value does not apply to type 3N141.

FIELD-EFFECT TRANSISTOR 3N141

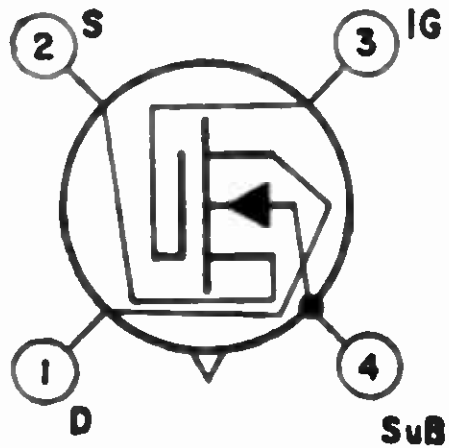


Si dual insulated-gate field-effect (MOS) n-channel depletion type used in mixer applications at frequencies up to 300 MHz. JEDEC TO-72, Outline No.28. This type is identical with type 3N140 except for the following item:

CHARACTERISTICS

Conversion Power Gain ($V_{DD} = 15$ V, $R_S = 120$ Ω , $f_{in} = 200$ MHz, $f_{out} = 30$ MHz, oscillator injection voltage from gate No.2 to source = 2.5 V (rms))	$G_{ps}(c)$	13 min; 17 typ	dB
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FIELD-EFFECT TRANSISTOR 3N142

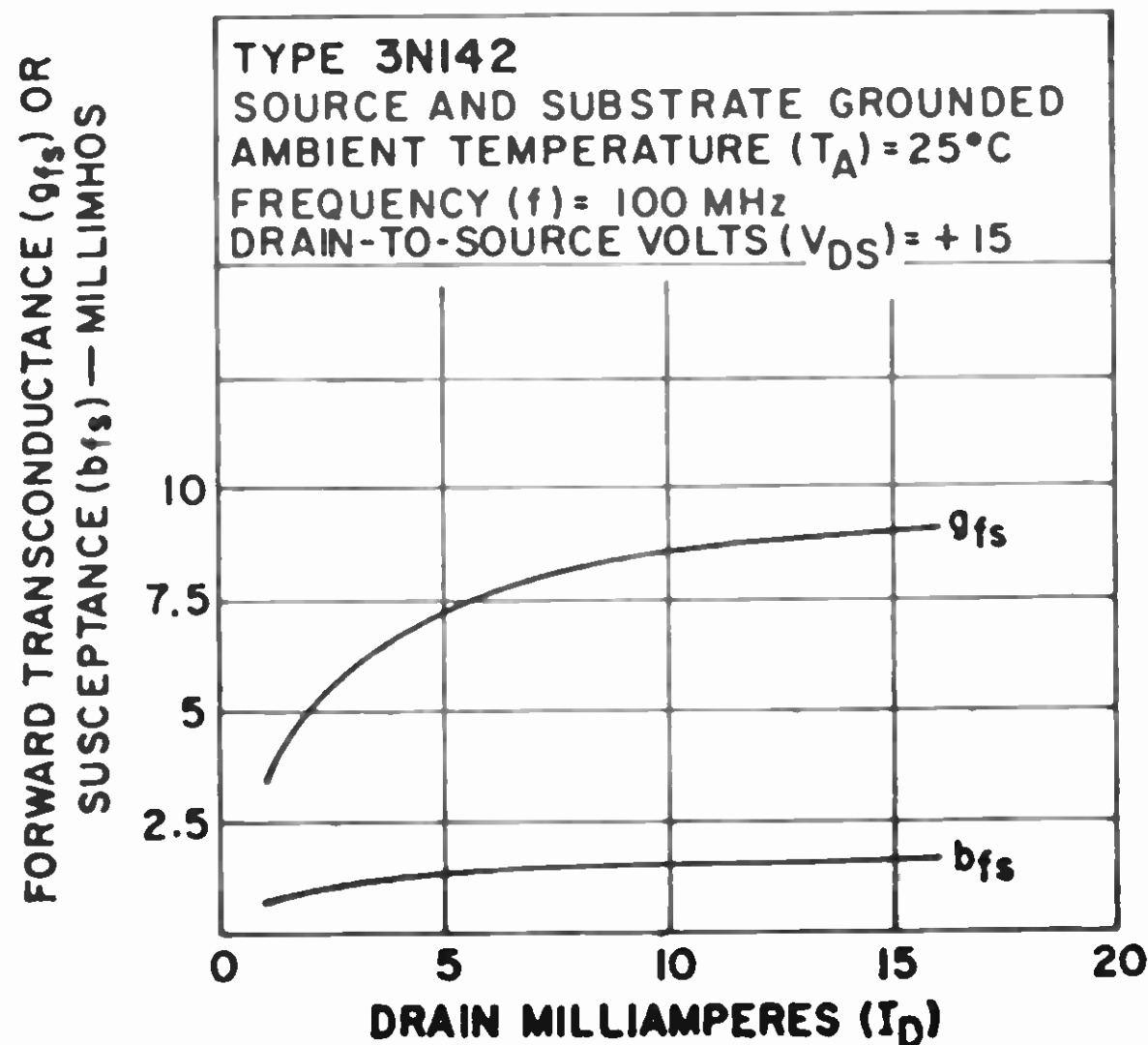


Si insulated-gate field-effect (MOS) n-channel depletion type used in rf-amplifier applications in FM receivers covering the 88-to-108-MHz band, and in general amplifier applications at frequencies up to 175 MHz. JEDEC TO-72, Outline No.28. For typical drain characteristics curve, refer to type 3N128.

MAXIMUM RATINGS

Drain-to-Source Voltage	V_{DS}	20	V
Gate-to-Source Voltage:			
Continuous	V_{GS}	0 to -8	V
Peak	V_{GS}	± 15	V
Drain-to-Gate Voltage	V_{DG}	20	V
Drain Current ($t_P = 20$ ms, $df \leq 0.1$)	I_D (pulsed)	50	mA
Transistor Dissipation:			
T_A up to 85°C	P_T	100	mW
T_A above 85°C	P_T	Derate at 6.67	mW/°C

TYPICAL FORWARD TRANSCONDUCTANCE CHARACTERISTICS



92CS-14154Ti

MAXIMUM RATINGS (cont'd)

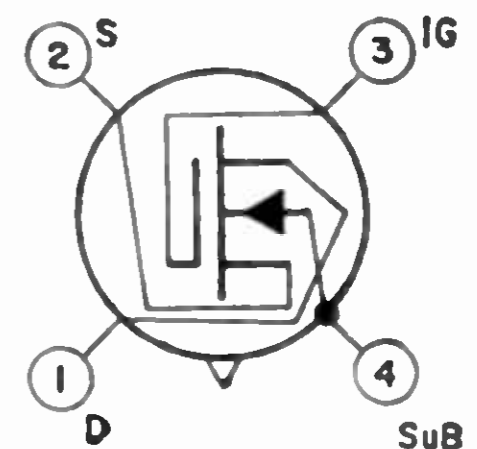
Temperature Range:			
Operating	T _(opr)	-65 to 100	°C
Storage	T _{STG}	-65 to 100	°C
Lead-Soldering Temperature	T _L	265	°C

CHARACTERISTICS

Drain-to-Source Cutoff Current (V _{DS} = 20 V, V _{GS} = -8 V)	I _D (off)	100	μA
Zero-Bias Drain Current (V _{DS} = 15 V, V _{GS} = 0, t _P = 20 ms (max), df ≤ 0.15)	I _{DSS} (pulsed)	5 to 50	mA
Gate Reverse Current: V _{GS} = -8 V, V _{DS} = 0	I _{GSS}	1 max	nA
V _{GS} = -8 V, V _{DS} = 0, T _A = 100°C	I _{GSS}	100 max	nA
Gate-to-Source Cutoff Voltage (V _{DS} = 20 V, I _D = 0.05 mA)	V _{GS} (off)	-2 to -8	V
Small-Signal Reverse Transfer Capacitance, Drain to Gate (V _{DS} = 15 V, I _D = 5 mA, f = 1 MHz)	C _{rSS}	0.12 typ; 0.2 max	pF
Input Resistance (V _{DS} = 15 V, I _D = 5 mA, f = 100 MHz)	r _{iSS}	2 min; 4.5 typ	kΩ
Output Resistance (V _{DS} = 15 V, I _D = 5 mA, f = 100 MHz)	r _{oSS}	2.25 min; 4.2 typ	kΩ
Input Capacitance (V _{DS} = 15 V, I _D = 5 mA, f = 1 MHz)	C _{iSS}	5.5 typ; 10 max	pF
Output Capacitance (V _{DS} = 15 V, I _D = 5 mA, f = 100 MHz)	C _{oSS}	1.4	pF
Forward Transconductance (V _{DS} = 15 V, I _D = 5 mA, f = 100 MHz)	g _{fs}	4 min; 7.5 typ	mmhos
Maximum Available Power Gain (V _{DS} = 15 V, I _D = 5 mA, f = 100 MHz)	MAG	24	dB
Maximum Usable Power Gain, Unneutralized (V _{DS} = 15 V, I _D = 5 mA, f = 100 MHz)	MUG	14	dB
Maximum Usable Power Gain, Neutralized (V _{DS} = 15 V, I _D = 5 mA, f = 100 MHz)	MUG	15 min; 17 typ	dB
Noise Figure (V _{DS} = 15 V, I _D = 5 mA, f = 100 MHz)	NF	4 typ; 5 max	dB

3N143 FIELD-EFFECT TRANSISTOR

Si insulated-gate field-effect (MOS) n-channel depletion type used in vhf mixer and oscillator applications. JEDEC TO-72, Outline No.28. This type is identical with type 3N128 except for the following items:

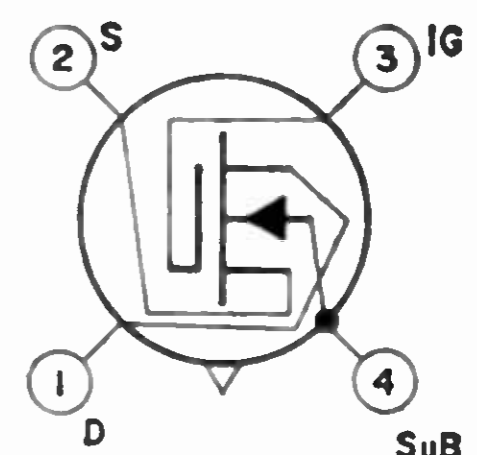


CHARACTERISTICS

Gate Leakage Current: V _{GS} = -8 V, V _{DS} = 0	I _{GSS}	0.1 typ; 1000 max	pA
V _{GS} = -8 V, V _{DS} = 0, T _A = 125°C	I _{GSS}	100 max	nA
Zero-Bias Drain Current (V _{DS} = 15 V, V _{GS} = 0, t _P = 20 ms (max), df ≤ 0.15)	I _{DSS}	10 to 50	mA
Input Conductance (V _{DS} = 15 V, I _D = 5 mA, f = 1 kHz)	g _{is}	10 max	μmhos
Output Conductance (V _{DS} = 15 V, I _D = 5 mA, f = 1 kHz)	g _{os}	1000 max	μmhos
Conversion Power Gain (V _{DS} = 15 V, I _D = 1 mA, f _{in} = 200 MHz, f _{out} = 30 MHz)	G _{PS} (c)	10 min; 13.5 typ	dB

3N152 FIELD-EFFECT TRANSISTOR

Si insulated-gate field-effect (MOS) n-channel depletion type used in low-noise rf applications in military and industrial vhf communications equipment up to 250 MHz. JEDEC TO-72, Outline No.28. For typical forward transconductance curve, refer to type 3N128.



MAXIMUM RATINGS

Drain-to-Source Voltage	V _{DS}	20	V
Gate-to-Source Voltage: Continuous (dc)	V _{GS}	-8 to 1	V
Peak (ac)	V _{GS}	±15	V

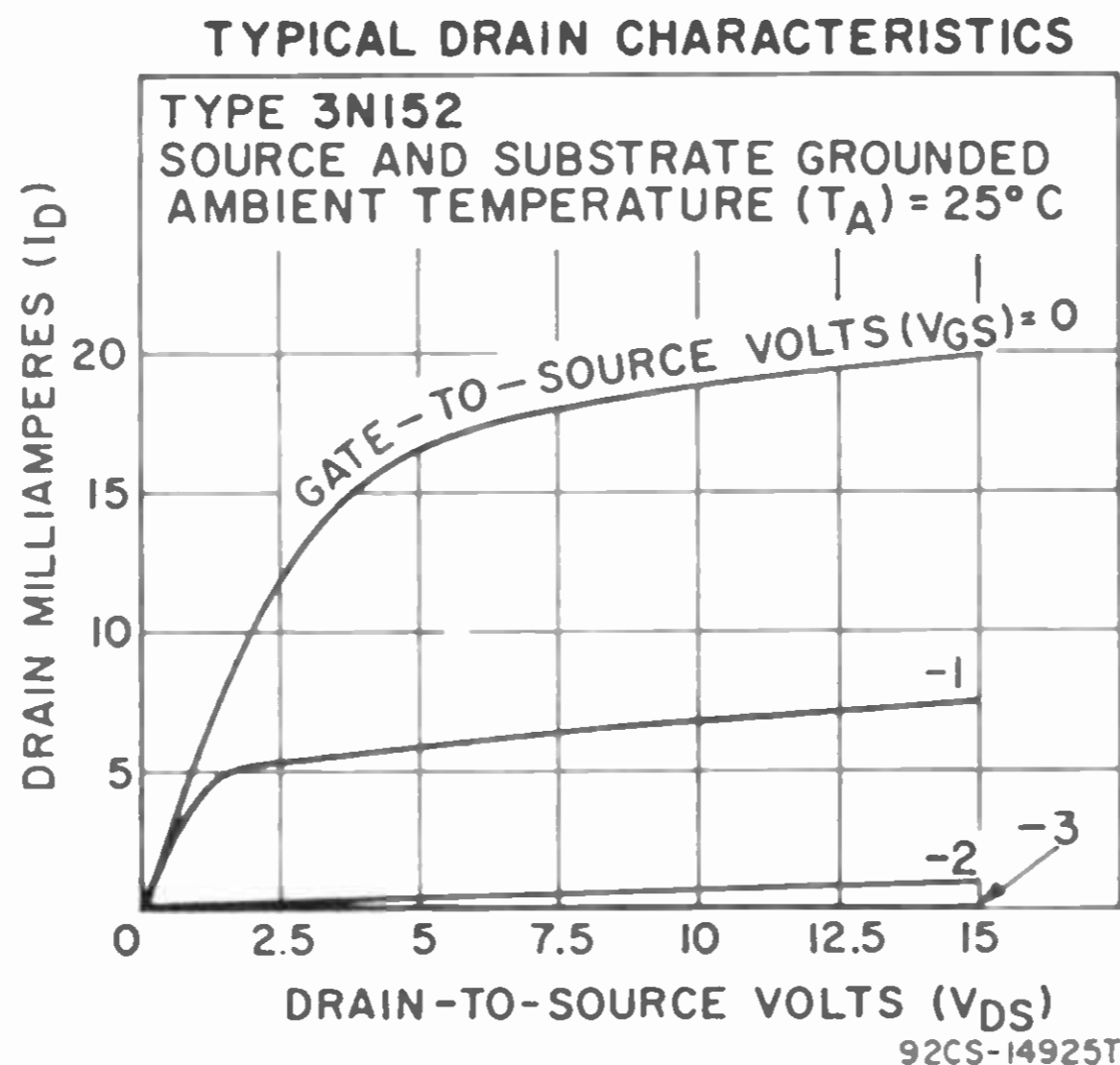
MAXIMUM RATINGS (cont'd)

Drain Current ($t_P \leq 20$ ms, $df \leq 0.15$)	I_D (pulsed)	50	mA
Transistor Dissipation:	P_T	400	mW
T_A up to 25°C	P_T	Derate at 2.67	mW/°C
T_A above 25°C			
Temperature Range:			
Operating	T (opr)	-65 to 175	°C
Storage	T_{STG}	-65 to 175	°C
Lead-Soldering Temperature (10 s max)	T_L	265	°C

CHARACTERISTICS

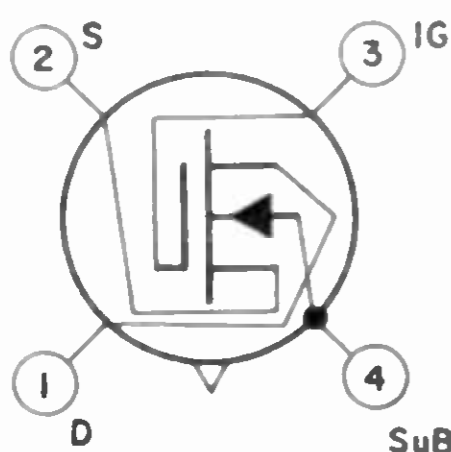
Drain-to-Source Cutoff Current ($V_{DS} = 20$ V, $V_{GS} = -8$ V)	I_D (off)	50 max	μA
Gate Leakage Current:			
$V_{DS} = 0$, $V_{GS} = -8$ V	I_{GSS}	0.0001 to 1	nA
$V_{DS} = 0$, $V_{GS} = -8$ V, $T_A = 85^\circ C$	I_{GSS}	10 max	nA
Zero-Bias Drain Current ($V_{DS} = 15$ V, $V_{GS} = 0$, $t_P \leq 20$ ms, $df \leq 0.15$)	I_{DSS} (pulsed)	10 to 50	mA
Drain-to-Source Channel Resistance ($V_{DS} = 0$, $V_{GS} = 0$, $f = 1$ kHz)	$r_{DS(on)}$	200	Ω
Maximum Available Power Gain ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 200$ MHz)	MAG	16 min; 20 typ	dB
Maximum Usable Gain, Neutralized ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 200$ MHz)	MUG	14.5 min; 16 typ	dB
Small-Signal Input Capacitance ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 0.1$ to 1 MHz)	C_{iss}	5.5 typ; 7 max	pF
Small-Signal Reverse Transfer Capacitance† ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 0.1$ to 1 MHz)	C_{rss}	0.12 typ; 0.2 max	pF
Small-Signal Output Capacitance ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 0.1$ to 1 MHz)	C_{oss}	1.4	pF
Forward Transconductance ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 1$ kHz)	g_{fs}	5000 to 12000	$\mu mhos$
Magnitude of Forward Transadmittance ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 200$ MHz)	$ Y_{fs} $	5000 min	$\mu mhos$
Input Conductance ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 200$ MHz)	g_{is}	450	$\mu mhos$
Output Conductance ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 200$ MHz)	g_{os}	300	$\mu mhos$
Noise Figure ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 200$ MHz)	NF	2.5 typ; 3.5 min	dB

† Three-terminal measurement with source returned to guard terminal.



FIELD-EFFECT TRANSISTOR

3N153



Si dual-insulated gate field-effect (MOS) n-channel depletion type used in critical chopper and multiplex applications up to 60 MHz. The terminal arrangement permits shielding between input and output terminals for superior high-frequency performance and greater circuit stability, particularly on printed-circuit boards.

JEDEC TO-72, Outline No.28.

MAXIMUM RATINGS

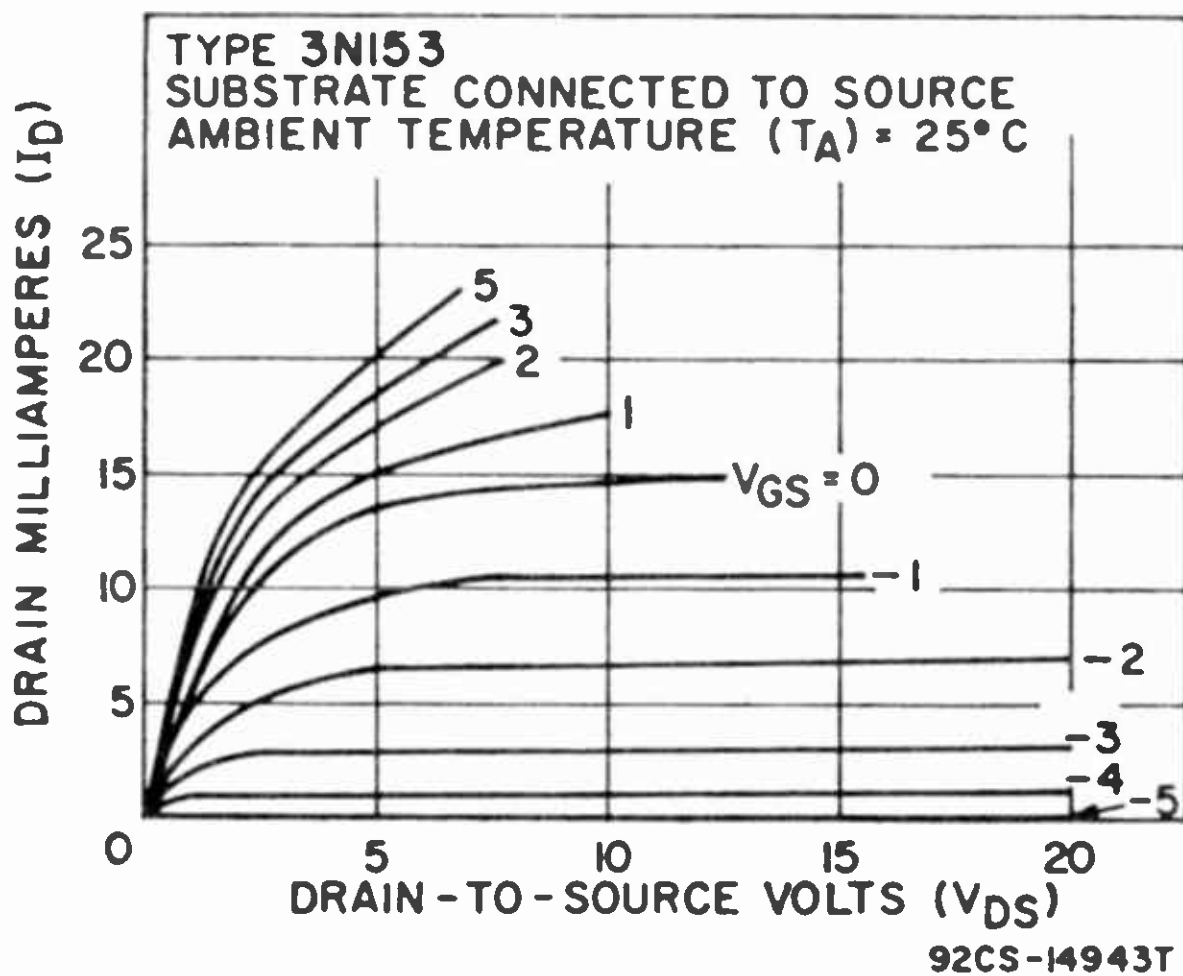
Drain-to-Source Voltage	V_{DS}	20	V
Drain-to-Substrate Voltage	V_{DB}	-0.3 to 20	V
Source-to-Substrate Voltage	V_{SB}	-0.3 to 20	V
DC Gate-to-Source Voltage	V_{GS}	-8 to 6	V
Peak Gate-to-Source Voltage	V_{GS}	± 14	V
Drain Current ($t_P = 20$ ms, $df \leq 0.10$)	I_D (pulsed)	50	mA
Transistor Dissipation:			
T_A up to 25°C	P_T	400	mW
T_A above 25°C	P_T	Derate linearly at 2.67	mW/°C
Temperature Range:			
Operating	T (opr)	-65 to 175	°C
Storage	T_{STG}	-65 to 175	°C
Lead-Soldering Temperature (10 s max)	T_L	265	°C

CHARACTERISTICS

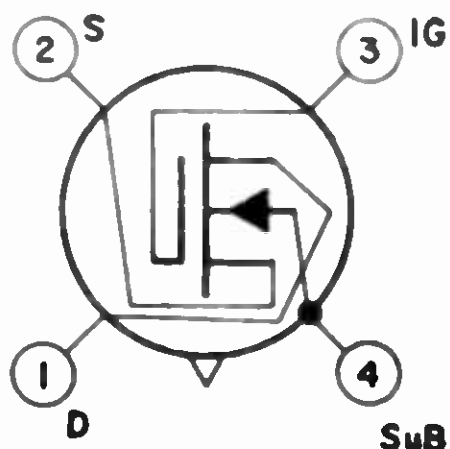
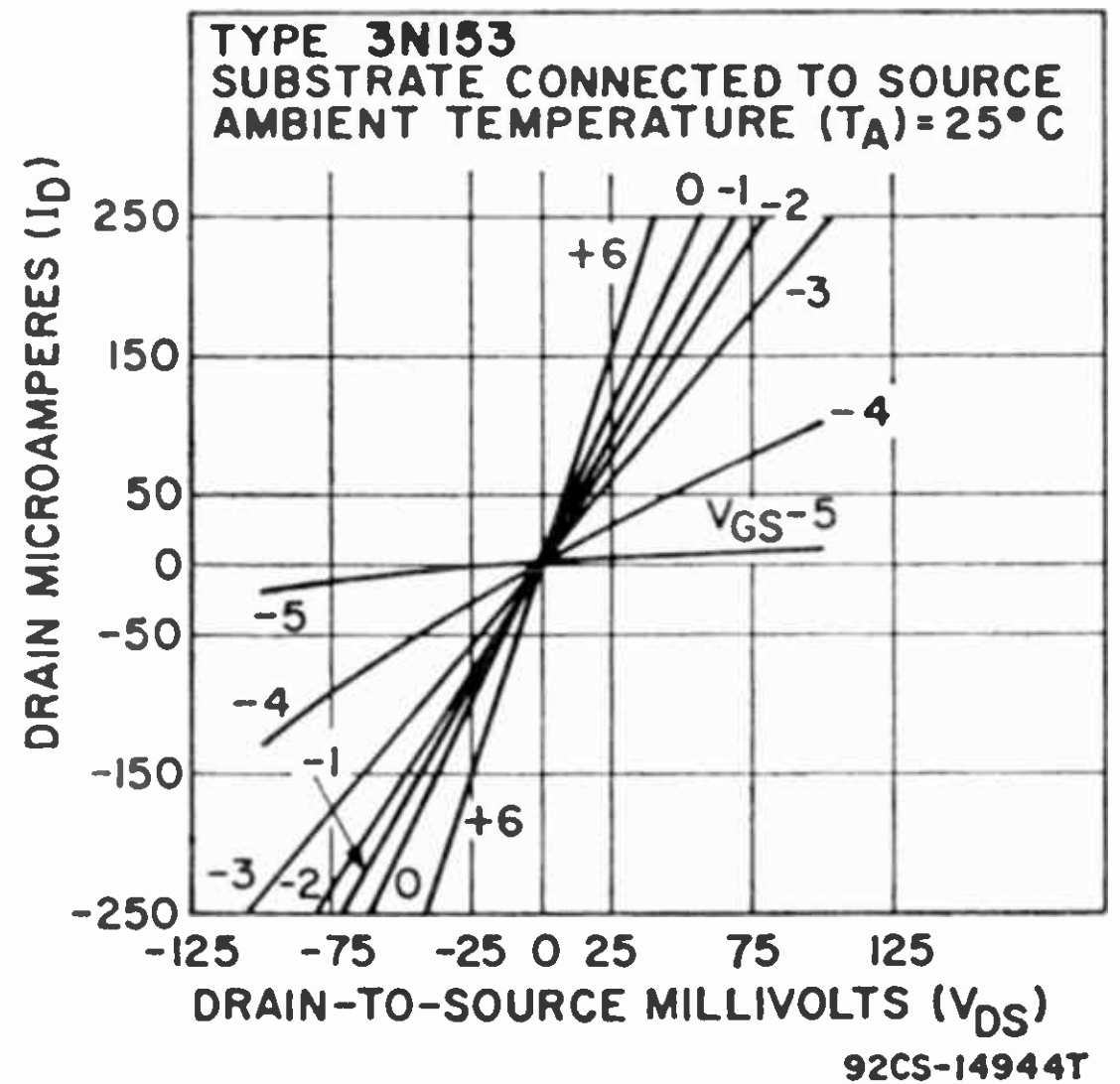
Drain-to-Source Cutoff Current:			
$V_{GS} = -8$ V, $V_{DS} = 1$ V	I_D (off)	0.1 typ; 1 max	nA
$V_{GS} = -8$ V, $V_{DS} = 1$ V, $T_A = 125^\circ\text{C}$	I_D (off)	0.1 typ; 1 max	μA
Gate-Leakage Current:			
$V_{GS} = -8$ to 6 V, $V_{DS} = 0$	I_{GSS}	0.1 typ; 50 max	pA
$V_{GS} = -8$ to 6 V, $V_{DS} = 0$, $T_A = 125^\circ\text{C}$	I_{GSS}	1 max	nA
Static Drain-to-Source "ON" Resistance			
($V_{GS} = 0$, $V_{DS} = 0$)	r_{DS} (on)	200 typ; 300 max	Ω
Drain-to-Source "OFF" Resistance			
($V_{GS} = -8$ V, $V_{DS} = 1$ V)	R_{DS} (off)	10^9 min; 10^{10} typ	Ω
Small-Signal Reverse Transfer Capacitance:			
$V_{GS} = -8$ V, $V_{DS} = 0$, $f = 1$ MHz	C_{rss}	0.34 typ; 0.5 max	pF
$V_{DS} = 15$ V, $I_D = 5$ mA, $f = 1$ MHz	C_{rss}	0.12 typ; 0.2 max	pF
Small-Signal Input Capacitance			
($V_{GS} = -8$ V, $V_{DS} = 0$, $f = 1$ MHz)	C_{iss}	6 typ; 8 max	pF
Small-Signal, Drain-to-Source Capacitance			
($V_{GS} = -8$ V, $V_{DS} = 0$, $f = 1$ MHz)	C_{ds}	3 max	μmhos
Zero-Gate-Bias Forward Transconductance			
($V_{GS} = 0$, $V_{DS} = 15$ V)	g_{fs}	10000	pF
Offset Voltage ($V_{GS} = -8$ to 6 V, $V_{DS} = 0$)	V_O	0†	V

† In measurements of Offset Voltage, thermocouple effects and contact potentials in the measurement setup may cause erroneous readings of 1 microvolt or more. These errors may be minimized by the use of solder having a low thermal e.m.f., such as Leeds & Northrup No. 107-1.0.1., or equivalent.

TYPICAL DRAIN CHARACTERISTICS



TYPICAL LOW-LEVEL DRAIN CHARACTERISTICS



FIELD-EFFECT TRANSISTOR 3N154

Si insulated-gate field-effect (MOS) n-channel depletion type used in vhf amplifier service in military and industrial applications. JEDEC TO-72, Outline No.28. For typical drain characteristics and typical forward transconductance curves, refer to type 3N128.

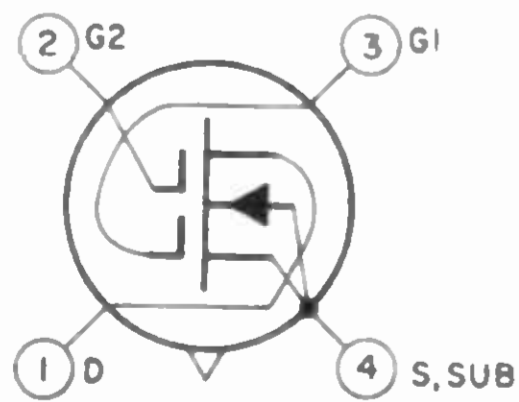
MAXIMUM RATINGS

Drain-to-Source Voltage	V_{DS}	20	V
Gate-to-Source Voltage:			
Continuous (dc)	V_{GS}	-8 to 1	V
Peak (ac)	V_{GS}	± 15	V
Drain-to-Gate Voltage	V_{DG}	20	V
Drain Current ($t_p \leq 20$ ms, $df \leq 0.15$)	I_D (pulsed)	50	mA
Transistor Dissipation:			
T_A up to 25°C	P_T	400	mW
T_A above 25°C	P_T	Derate at 2.67	mW/°C
Temperature Range:			
Operating	T(opr)	-65 to 175	°C
Storage	T_{STG}	-65 to 175	°C
Lead-Soldering Temperature (10 s max)	T_L	265	°C

CHARACTERISTICS

Gate-to-Source Cutoff Voltage ($V_{DS} = 15$ V, $I_D = 50 \mu A$)	V_{GS} (off)	-2 to -8	V
Drain-to-Source Cutoff Current ($V_{DS} = 20$ V, $V_{GS} = -8$ V)	I_D (off)	50 max	μA
Zero-Bias Drain Current ($V_{DS} = 15$ V, $V_{GS} = 0$, $t_p \leq 20$ ms, $df \leq 0.15$)	I_{DSS} (pulsed)	10 to 25	mA
Gate Leakage Current:			
$V_{GS} = -8$ V, $V_{DS} = 0$	I_{GSS}	0.0001 typ; 0.05 max	nA
$V_{GS} = -8$ V, $V_{DS} = 0$, $T_A = 125^\circ C$	I_{GSS}	5 max	nA
$V_{GS} = 1$ V, $V_{DS} = 0$	I_{GSS}	0.0001 typ; 0.05 max	nA
$V_{GS} = 1$ V, $V_{DS} = 0$, $T_A = 125^\circ C$	I_{GSS}	5 max	nA
Magnitude of Forward Transadmittance ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 200$ MHz)	$ Y_{fs} $	5000 min; 7500 typ	$\mu mhos$
Forward Transconductance ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 1$ kHz)	g_{fs}	5000 to 12000	$\mu mhos$
Small-Signal Input Capacitance ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 0.1$ to 1 MHz) ...	C_{iss}	5.5 typ; 7 max	pF
Small-Signal Reverse Transfer Capacitance† ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 0.1$ to 1 MHz) ...	C_{rss}	0.03 to 0.2	pF
Small-Signal Output Capacitance ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 0.1$ to 1 MHz) ...	C_{oss}	1.4	pF
Gate Leakage Current Resistance ($V_{DS} = 0$, $V_{GS} = -8$ V)	R_{GS}	10^{14}	Ω
Drain-to-Source Channel Resistance ($V_{DS} = 0$, $V_{GS} = 0$, $f = 1$ kHz)	$r_{DS}(on)$	200	Ω
Input Conductance ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 200$ MHz)	g_{is}	500	$\mu mhos$
Output Conductance ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 200$ MHz)	g_{os}	275	$\mu mhos$
Maximum Available Power Gain ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 200$ MHz)	MAG	20	dB
Maximum Usable Power Gain, Neutralized ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 200$ MHz)	MUG	13.5 min; 16 typ	dB
Noise Figure ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 200$ MHz)	NF	3.5 typ; 5 max	dB

† Three-terminal measurement with source returned to guard terminal.



FIELD-EFFECT TRANSISTOR 3N159

Si insulated-gate field-effect (MOS) n-channel depletion type used in rf amplifier applications at frequencies up to 300 MHz. JEDEC TO-72, Outline No.28.

MAXIMUM RATINGS

Drain-to-Source Voltage	V_{DS}	0 to 20	V
Gate-No.1-to-Source Voltage:			
Continuous (dc)	V_{G1S}	-8 to 1	V
Peak (ac)	V_{G1S}	-8 to 20	V
Gate-No.2-to-Source Voltage:			
Continuous (dc)	V_{G2S}	-8 to (0.4 V_{DS})	V
Peak (ac)	V_{G2S}	-8 to 20	V
Drain-to-Gate-No.1 Voltage	V_{DG1}	20	V
Drain-to-Gate-No.2 Voltage	V_{DG2}	20	V
Drain Current ($t_p \leq 20$ ms, $df \leq 0.15$)	I_D (pulsed)	50	mA
Transistor Dissipation:			
T_A up to 25°C	P_T	400	mW
T_A above 25°C	P_T	Derate linearly at 2.67	mW/°C

MAXIMUM RATINGS (cont'd)

Temperature Range:			
Operating	T(opr)	-65 to 175	°C
Storage	T _{STG}	-65 to 175	°C
Lead-Soldering Temperature (10 s max)	T _L	265	°C

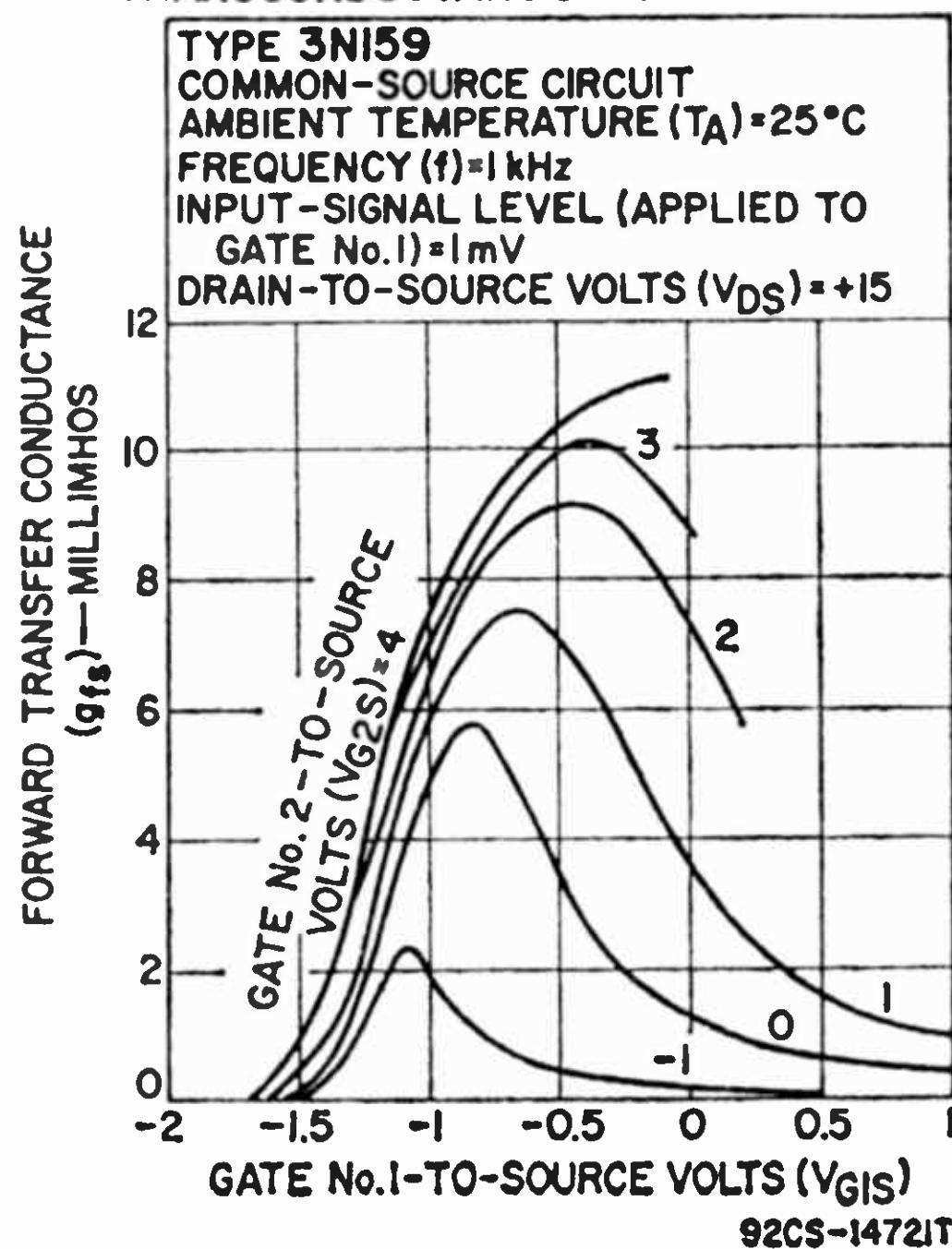
CHARACTERISTICS

Gate-No.1-to-Source Cutoff Voltage (V _{DS} = 16 V, V _{G2S} = 4 V, I _D = 200 μA)	V _{G1S} (off)	-2 typ; -4 max	V
Gate-No.2-to-Source Cutoff Voltage (V _{DS} = 16 V, V _{G1S} = 0, I _D = 200 μA)	V _{G2S} (off)	-2 typ; -4 max	V
Gate-No.1-Leakage Current: V _{G1S} = -20 V, V _{G2S} = 0, V _{DS} = 0	I _{G1SS}	1 max	nA
V _{G1S} = 1 V, V _{G2S} = 0, V _{DS} = 0	I _{G1SS}	1 max	nA
V _{G1S} = -20 V, V _{G2S} = 0, V _{DS} = 0, T _A = 125°C ...	I _{G1SS}	0.2 max	μA
Gate-No.2-Leakage Current: V _{G2S} = -20 V, V _{G1S} = 0, V _{DS} = 0	I _{G2SS}	1 max	nA
V _{G2S} = 1 V, V _{G1S} = 0, V _{DS} = 0	I _{G2SS}	1 max	nA
V _{G2S} = -20 V, V _{G1S} = 0, V _{DS} = 0, T _A = 125°C ...	I _{G2SS}	0.2 max	μA
Zero-Bias Drain Current (V _{DD} = 14 V, V _{G1S} = 0, V _{G2S} = 4 V, t _p ≤ 20 ms, df ≤ 0.15)	I _{DSS} (pulsed)	5 to 30	mA
Forward Transconductance, Gate-No.1 to Drain (V _{DD} = 14 V, V _{G2S} = 4 V, I _D = 10 mA, f = 1 kHz)	g _{fs}	7000 to 18000	μmhos
Cutoff Forward Transconductance, Gate-No.1 to Drain (V _{DD} = 14 V, V _{G1S} = -0.5 V, V _{G2S} = -2 V, f = 1 kHz)	g _{fs} (off)	100 max	μmhos
Small-Signal Input Capacitance‡ (V _{DS} = 13 V, V _{G2S} = 4 V, I _D = 10 mA, f = 1 MHz)	C _{iss}	3 to 7	pF
Small-Signal Reverse Transfer Capacitance, Drain to Gate-No.1 [▲] (V _{DS} = 13 V, V _{G2S} = 4 V, I _D = 10 mA, f = 1 MHz)	C _{rss}	0.01 to 0.03	pF
Small-Signal Output Capacitance (V _{DS} = 13 V, V _{G2S} = 4 V, I _D = 10 mA, f = 1 MHz)	C _{oss}	2.2	pF
Maximum Usable Power Gain (V _{DD} = 15 V, R _S = 270 Ω, R _G = 50 Ω, f = 200 MHz)	MUG	16 to 22	dB
Noise Figure (V _{DD} = 15 V, R _S = 270 Ω, R _G = 50 Ω, f = 200 MHz)	NF	2.5 typ; 3.5 max	dB

‡ Capacitance between gate No.1 and all other terminals.

[▲] Three-terminal measurement with gate No.2 and source returned to guard terminal.

TYPICAL FORWARD TRANSCONDUCTANCE CHARACTERISTICS



3746

3907/2N404

4403

Refer to Chart of Discontinued Transistors

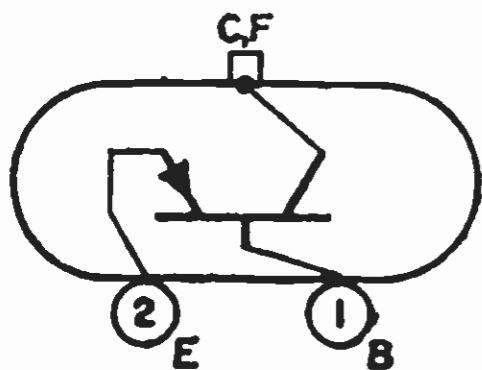
Refer to Chart of Discontinued Transistors

Refer to Chart of Photocells

Refer to Chart of Photocells **4448**

Refer to Chart of Photocells **4453**

Refer to Chart of Photocells **7163**



POWER TRANSISTOR

40022

Ge p-n-p alloy type used in class A and push-pull class B service in high-fidelity af power-amplifier applications. JEDEC TO-3, Outline No.2.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-32	V
Collector-to-Emitter Voltage ($R_{BE} = 30 \Omega$)	V_{CER}	-32	V
Emitter-to-Base Voltage	V_{EBO}	-5	V
Collector Current	I_C	-5	A
Base Current	I_B	-1	A
Transistor Dissipation:			
T_{MF} up to 81°C	P_T	12.5	W
T_{MF} above 81°C	P_T	Derate linearly 0.66 W/°C	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 100	°C
Storage	T_{STG}	-65 to 100	°C
Pin-Soldering Temperature (10 s max)	T_P	255	°C

CHARACTERISTICS (At mounting-flange temperature = 25°C)

Collector-to-Base Breakdown Voltage ($I_C = -0.005 A$, $I_E = 0$)	$V_{(BR)CBO}$	-32 min	V
Collector-to-Emitter Breakdown Voltage ($I_C = -0.2 A$, $R_{BE} = 33 \Omega$)	$V_{(BR)CER}$	-32 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -0.002 A$, $I_C = 0$)	$V_{(BR)EBO}$	-5 min	V
Base-to-Emitter Voltage* ($V_{CB} = -10 V$, $I_C = -0.05 A$)	V_{BE}	-0.18	V
Collector-Cutoff Current ($V_{CB} = -30$, $I_E = 0$)	I_{CBO}	-1 max	mA
Collector-Cutoff Saturation Current ($V_{CB} = -0.5 V$, $I_E = 0$)	$I_{CBO}(sat)$	-0.1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = -2 V$, $I_C = -1 A$)	h_{FE}	38 min; 70 typ	
Gain-Bandwidth Product ($V_{CE} = -5 V$, $I_C = -0.5 A$)	f_T	300	kHz
Thermal Resistance, Junction-to-Case	θ_{J-C}	1.5 max	°C/W

TYPICAL OPERATION IN CLASS B AF-AMPLIFIER CIRCUIT

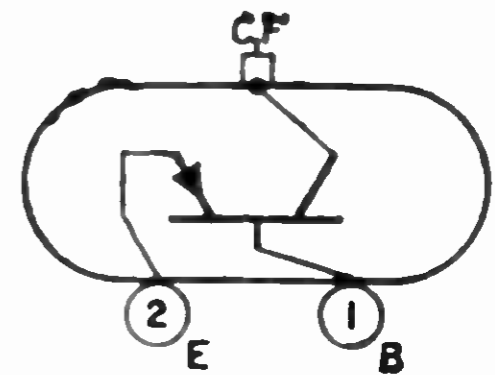
Unless otherwise specified, values are for 2 transistors.

DC Collector-Supply Voltage	V_{CC}	-14	V
Zero-Signal Base-Bias Voltage		-0.18	V
Zero-Signal DC Collector Current	I_C	-0.05	A
Maximum-Signal DC Collector Current	I_C	-0.716	A
Peak Collector Current	$i_C(peak)$	-2.25	A
Input Impedance of Stage (Per base)	R_s	43	Ω
Load Impedance (Speaker voice-coil)	R_L	4	Ω
Maximum Collector Dissipation (Per transistor under worst-case conditions)		5	W
Music Power Output		18	W
Power Gain	G_{PE}	24	dB
Total Harmonic Distortion		5	%
Maximum-Signal Power Output	P_{OE}	10	W

* This characteristic does not apply to type 40254.

40050 POWER TRANSISTOR

Ge p-n-p alloy type for high-fidelity amplifiers and other commercial af amplifier applications. JEDEC TO-3, Outline No.2.



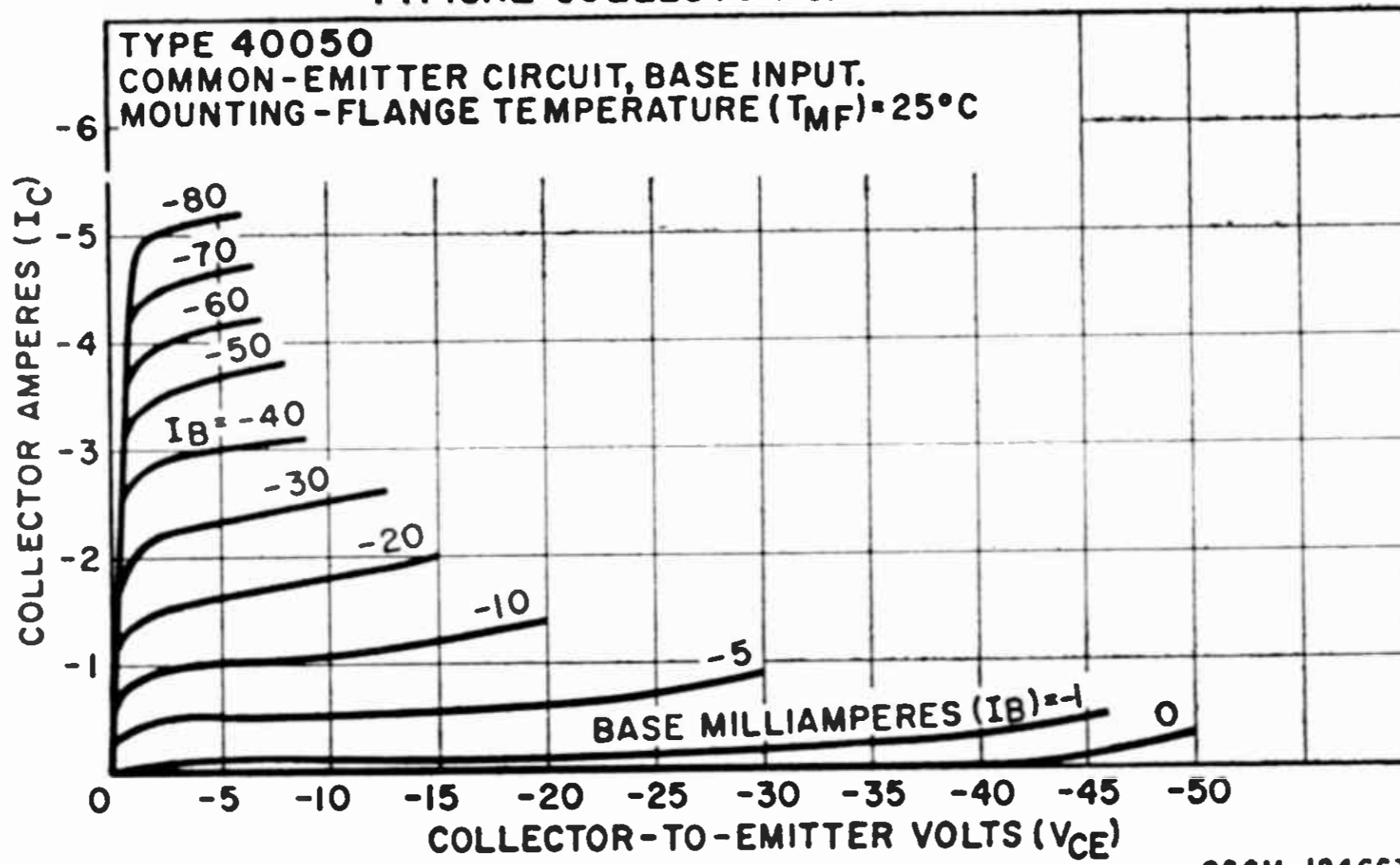
MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-40	V
Collector-to-Emitter Voltage	V_{CEO}	-40	V
Emitter-to-Base Voltage	V_{EBO}	-5	V
Collector Current	I_C	-5	A
Base Current	I_B	-1	A
Transistor Dissipation:			
T_{MF} up to 81°C	P_T	12.5	W
T_{MF} above 81°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 100	°C
Storage	T_{STG}	-65 to 100	°C
Pin-Soldering Temperature (10 s max)	T_P	255	°C

CHARACTERISTICS (At mounting-flange temperature = 25°C)

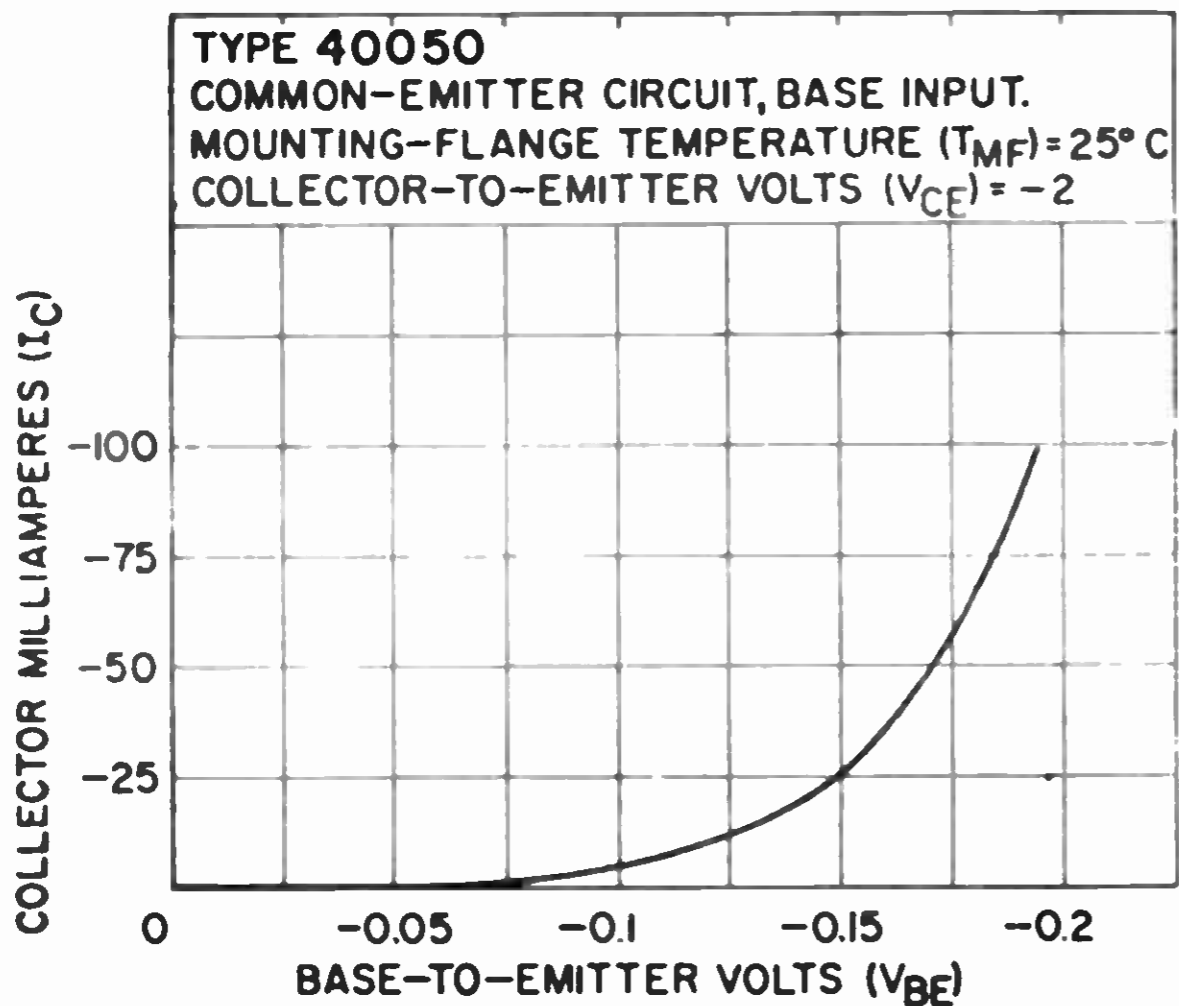
Collector-to-Base Breakdown Voltage ($I_C = -5$ mA, $I_E = 0$)	$V_{(BR)CBO}$	-40 min	V
Collector-to-Emitter Breakdown Voltage ($I_C = -0.6$ A, $R_{BE} = 68 \Omega$)	$V_{(BR)CER}$	-40 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -2$ mA, $I_C = 0$)	$V_{(BR)EBO}$	-5 min	V
Base-to-Emitter Voltage ($V_{CE} = -10$ V, $I_C = -0.5$ A)	V_{BE}	-0.17	V
Collector-Cutoff Current ($V_{CB} = -30$ V, $I_E = 0$)	I_{CBO}	-0.5 max	mA

TYPICAL COLLECTOR CHARACTERISTICS



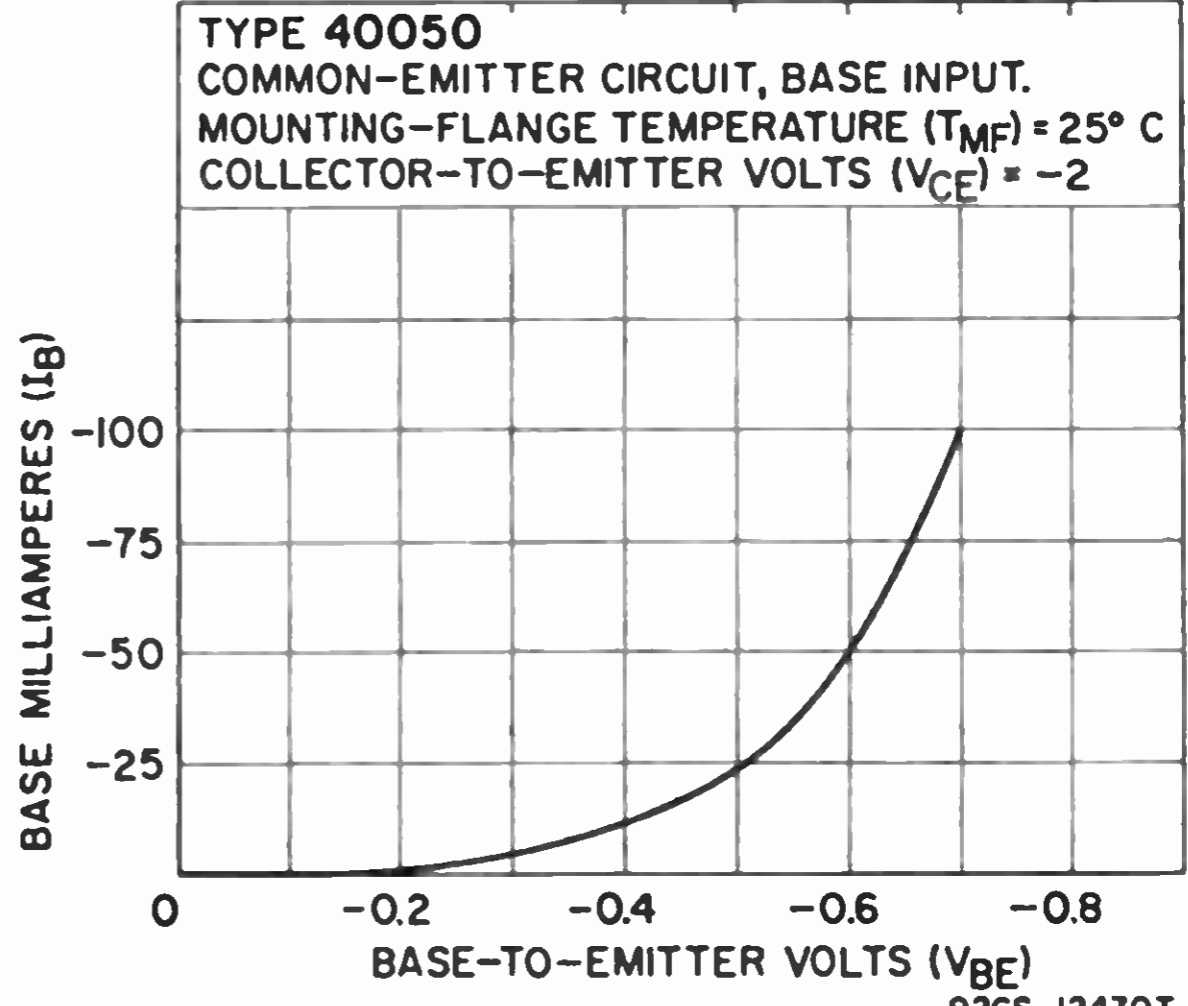
92CM-12466T

TYPICAL TRANSFER CHARACTERISTIC



92CS-12468T

TYPICAL INPUT CHARACTERISTIC



92CS-12470T

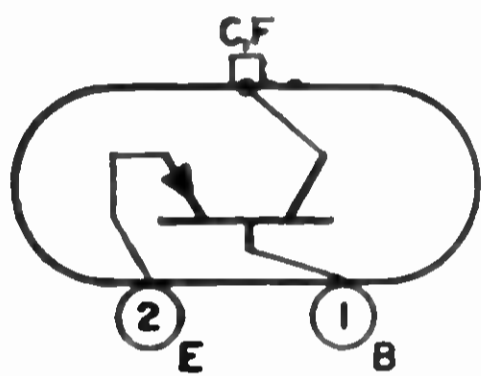
CHARACTERISTICS (cont'd)

Collector-Cutoff Saturation Current ($V_{CB} = -0.5 \text{ V}$, $I_E = 0$)	$I_{CBO}(\text{sat})$	-0.1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = -2 \text{ V}$, $I_C = -1 \text{ A}$)	h_{FE}	50 min	
Gain-Bandwidth Product ($V_{CE} = 5 \text{ V}$, $I_C = -0.5 \text{ A}$)	f_T	500	kHz
Thermal Resistance, Junction-to-Case	Θ_{J-C}	1.5 max	$^{\circ}\text{C}/\text{W}$

TYPICAL OPERATION IN CLASS B AF-AMPLIFIER CIRCUIT

Unless otherwise specified, values are for 2 transistors.

DC Collector-Supply Voltage	V_{CC}	-18	V
Zero-Signal Base-Bias Voltage		-0.17	V
Zero-Signal DC Collector Current	I_C	-0.05	A
Maximum-Signal DC Collector Current	I_C	-0.8	A
Peak Collector Current	$i_C(\text{peak})$	-2.8	A
Input Impedance of Stage (Per base)	R_S	32	Ω
Load Impedance (Speaker voice-coil)	R_L	4	Ω
Maximum Collector Dissipation (Per transistor under worst-case conditions)		7.5	W
Power Gain	G_{PB}	28	dB
Total Harmonic Distortion		5	%
Music Power Output		25	W
Maximum-Signal Power Output	P_{OB}	15	W



POWER TRANSISTOR

40051

Ge p-n-p alloy type for high-fidelity amplifiers and other commercial af amplifier applications. JEDEC TO-3, Outline No.2. This type is identical with type 40050 except for the following items:

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-50	V
Collector-to-Emitter Voltage	V_{CEO}	-50	V

CHARACTERISTICS (At mounting-flange temperature = 25°C)

Collector-to-Base Breakdown Voltage ($I_C = -5 \text{ mA}$, $I_E = 0$)	$V_{(BR)CBO}$	-50 min	V
Collector-to-Emitter Breakdown Voltage ($I_C = -0.6 \text{ A}$, $R_{BE} = 68 \Omega$)	$V_{(BR)CER}$	-50 min	V

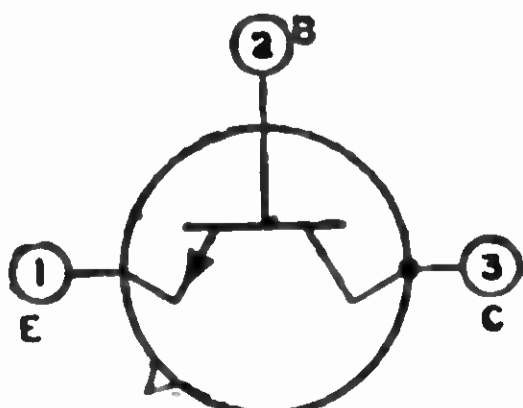
TYPICAL OPERATION IN CLASS B AF-AMPLIFIER CIRCUIT

Unless otherwise specified, values are for 2 transistors.

DC Collector-Supply Voltage	V_{CC}	-22	V
Zero-Signal Base-Bias Voltage		-0.17	V
Zero-Signal DC Collector Current	I_C	-0.05	A
Maximum-Signal DC Collector Current	I_C	-1.1	A
Peak Collector Current	$i_C(\text{peak})$	-3.5	A
Input Impedance of Stage (Per base)	R_S	31	Ω
Load Impedance (Speaker voice-coil)	R_L	4	Ω
Maximum Collector Dissipation (Per transistor under worst-case conditions)		12.5	W
Power Gain	G_{PB}	28	dB
Total Harmonic Distortion		5	%
Music Power Output		45	W
Maximum-Signal Power Output	P_{OB}	25	W

TRANSISTOR

40080



Si n-p-n triple-diffused planar type designed for oscillator applications, in conjunction with transistor types 40081 (driver) and 40082 (power amplifier) in a 5-watt input, 27-MHz citizens-band transmitter. JEDEC TO-39, Outline No.15.

MAXIMUM RATINGS

Table with 4 columns: Parameter, Symbol, Value, Unit. Includes Collector-to-Emitter Voltage (V_CEO), Peak Collector Current (i_c), Transistor Dissipation (P_T), Temperature Range (T_J, T_STG, T_L).

CHARACTERISTICS

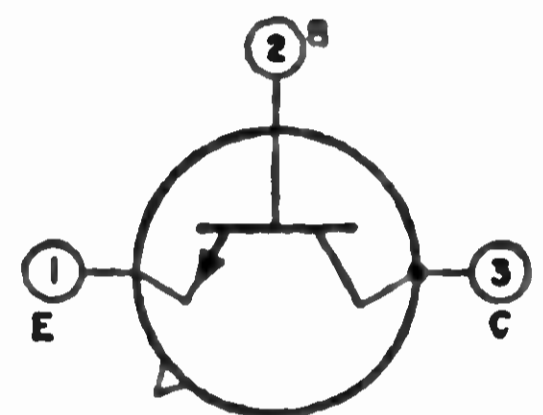
Table with 4 columns: Parameter, Symbol, Value, Unit. Includes Collector-to-Emitter Voltage (I_c = 10 mA), Collector-Cutoff Current (I_CBO), RF Power Output (P_o), Collector-to-Base Capacitance (C_obo), Thermal Resistance (theta_J-A).

TYPICAL OPERATION IN A CITIZENS-BAND TRANSMITTER

Table with 4 columns: Parameter, Symbol, Value, Unit. Includes DC Collector-Supply Voltage (V_cc), DC Collector Current (I_c) for no modulation and 100% modulation.

40081 TRANSISTOR

Si n-p-n triple-diffused planar type designed for driver applications, in conjunction with transistor types 40080 (oscillator) and 40082 (power amplifier), in a 5-watt input, 27-MHz citizens-band transmitter, JEDEC TO-5, Outline No.5.



MAXIMUM RATINGS

Table with 4 columns: Parameter, Symbol, Value, Unit. Includes Collector-to-Emitter Voltage (V_CEV), Emitter-to-Base Voltage (V_EBO), Peak Collector Current (i_c), Transistor Dissipation (P_T), Temperature Range (T_J, T_STG, T_L).

CHARACTERISTICS

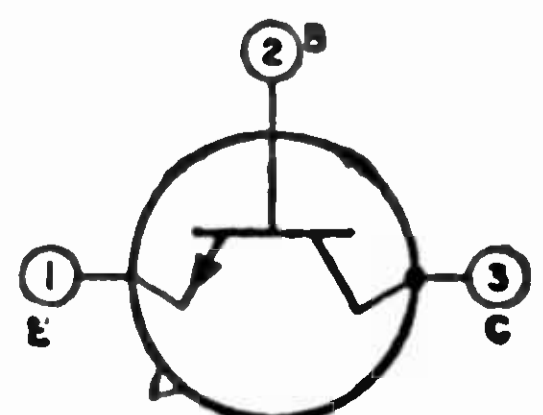
Table with 4 columns: Parameter, Symbol, Value, Unit. Includes Collector-to-Emitter Voltage (V_CEV), Emitter-to-Base Voltage (V_EBO), Collector-Cutoff Current (I_CBO), RF Power Output (P_o), Collector-to-Base Capacitance (C_obo), Thermal Resistance (theta_J-A).

TYPICAL OPERATION IN A CITIZENS-BAND TRANSMITTER

Table with 4 columns: Parameter, Symbol, Value, Unit. Includes DC Collector-Supply Voltage (V_cc), DC Collector Current (I_c) for no modulation and 100% modulation.

40082 POWER TRANSISTOR

Si n-p-n triple-diffused planar type designed for power-amplifier applications, in conjunction with transistor types 40080 (oscillator) and 40081 (driver), in a 5-watt, 27-MHz citizens-band transmitter. JEDEC TO-39, Outline No.15.



MAXIMUM RATINGS

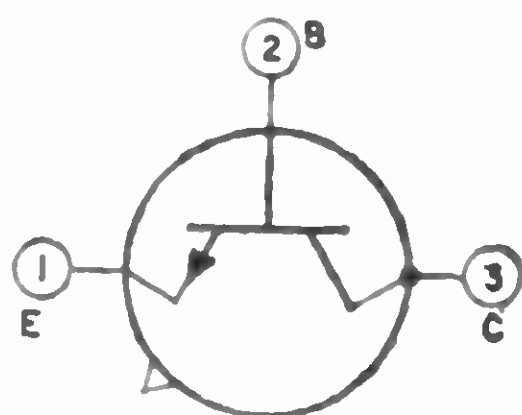
Collector-to-Emitter Voltage ($V_{BE} = -0.5$ V)	V_{CEV}	60	V
Emitter-to-Base Voltage	V_{EBO}	2.5	V
Peak Collector Current	I_C	1.5	A
Transistor Dissipation:			
T_C up to 25°C	P_T	5	W
T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	230	°C

CHARACTERISTICS

Collector-to-Emitter Voltage ($V_{BE} = -0.5$ V, $I_C = 500$ μ A)	V_{CEV}	60 min	V
Emitter-to-Base Voltage ($I_E = 500$ μ A, $I_C = 0$)	V_{EBO}	2.5 min	V
$I_C = 0$)	I_{CBO}	10 max	μ A
Collector-Cutoff Current ($V_{CB} = 15$ V, $I_E = 0$)			
RF Power Output ($V_{CC} = 12$ V, $I_C = 415$ mA max, $P_{IE} = 350$ mW, $f = 27$ MHz)	P_{OE}	3 min	W
Collector-to-Base Capacitance ($V_{CE} = 30$ V, $f = 1$ MHz)	C_{obo}	20 max	pF
Thermal Resistance, Junction-to-Case	θ_{J-C}	35	°C/W

TYPICAL OPERATION IN A CITIZENS-BAND TRANSMITTER

DC Collector-Supply Voltage	V_{CC}	13.8	V
DC Collector Current:			
No modulation	I_C	330	mA
100% modulation	I_C	330	mA
Power Output:			
No modulation (adjusted for legal maximum- power output)	P_{OE}	3.5	W
100% modulation	P_{OB}	4.8	W



TRANSISTOR

40084

Si n-p-n triple-diffused planar type used in a wide variety of small and medium-power applications (up to 20 MHz) in industrial equipment. JEDEC TO-18, Outline No.12.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	60	V
Collector-to-Emitter Voltage:			
$R_{BE} = 10$ Ω	V_{CER}	50	V
Base open	V_{CEO}	40	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	1	A
Transistor Dissipation:			
T_C up to 25°C	P_T	1.8	W
T_A up to 25°C	P_T	0.5	W
T_A or T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	225	°C

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Base Breakdown Voltage ($I_C = 0.1$ mA, $I_E = 0$)	$V_{(BR)CBO}$	60 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.1$ mA, $I_C = 0$)	$V_{(BR)EBO}$	5 min	V
Collector-to-Emitter Sustaining Voltage:			
$I_C = 100$ mA, $R_{BE} = 10$ Ω , $t_p = 300$ μ s, $df = 1.8\%$	$V_{CER}(SUS)$	50 min	V
$I_C = 100$ mA, $I_B = 0$, $t_p = 300$ μ s, $df = 1.8\%$	$V_{CEO}(SUS)$	40 min	V
Base-to-Emitter Saturation Voltage ($I_C = 150$ mA, $I_B = 15$ mA)	$V_{BE}(sat)$	1.7 max	V
Collector-to-Emitter Saturation Voltage ($I_C = 150$ mA, $I_B = 15$ mA)	$V_{CE}(sat)$	1.4 max	V
Collector-Cutoff Current ($V_{CB} = 30$ V, $I_E = 0$)	I_{CBO}	0.25 max	μ A
Emitter-Cutoff Current ($V_{EB} = 4$ V, $I_C = 0$)	I_{EBO}	0.25 max	μ A
Input Capacitance ($V_{EB} = 0.5$ V, $I_C = 0$)	C_{ibo}	80 max	pF
Output Capacitance ($V_{CB} = 10$ V, $I_E = 0$)	C_{obo}	15 max	pF

CHARACTERISTICS (cont'd)

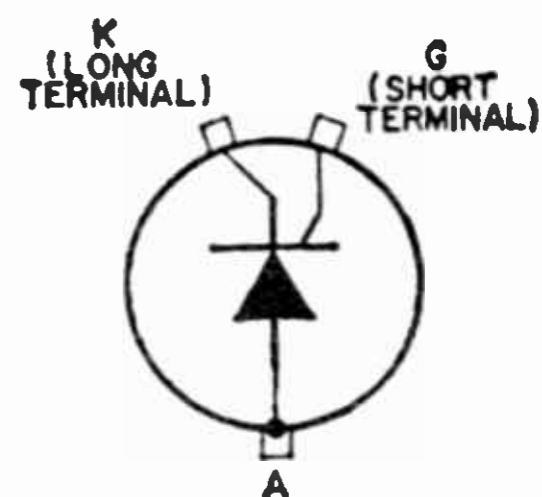
Pulsed Static Forward-Current Transfer Ratio ($V_{CE} = 10\text{ V}$, $I_C = 150\text{ mA}$, $t_p = 300\ \mu\text{s}$, $df = 1.8\%$)	h_{FE}	50 to 250	
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 10\text{ V}$, $I_C = 50\text{ mA}$, $f = 20\text{ MHz}$)	h_{fe}	5 min	
Noise Figure ($R_G = 500\ \Omega$, circuit bandwidth = 15 kHz, $V_{CE} = 10\text{ V}$, $I_C = 0.3\text{ mA}$, $f = 1\text{ kHz}$)	NF	8 max	dB
Thermal Resistance:			
Junction-to-Case	θ_{J-C}	97 max	$^{\circ}\text{C/W}$
Junction-to-Ambient	θ_{J-A}	350 max	$^{\circ}\text{C/W}$

40108	Refer to Charts of Rectifier Data
40109	Refer to Charts of Rectifier Data
40110	Refer to Charts of Rectifier Data
40111	Refer to Charts of Rectifier Data
40112	Refer to Charts of Rectifier Data
40113	Refer to Charts of Rectifier Data
40114	Refer to Charts of Rectifier Data
40115	Refer to Charts of Rectifier Data
40208	Refer to Charts of Rectifier Data
40209	Refer to Charts of Rectifier Data
40210	Refer to Charts of Rectifier Data
40211	Refer to Charts of Rectifier Data
40212	Refer to Charts of Rectifier Data
40213	Refer to Charts of Rectifier Data
40214	Refer to Charts of Rectifier Data

40216

SILICON CONTROLLED RECTIFIER

Si all-diffused three-junction type for use in radar pulse modulators, inverters, switching regulators, and other applications requiring a large ratio of peak to average current. JEDEC TO-48, Outline No.20. See Mounting Hardware for desired mounting arrangement.

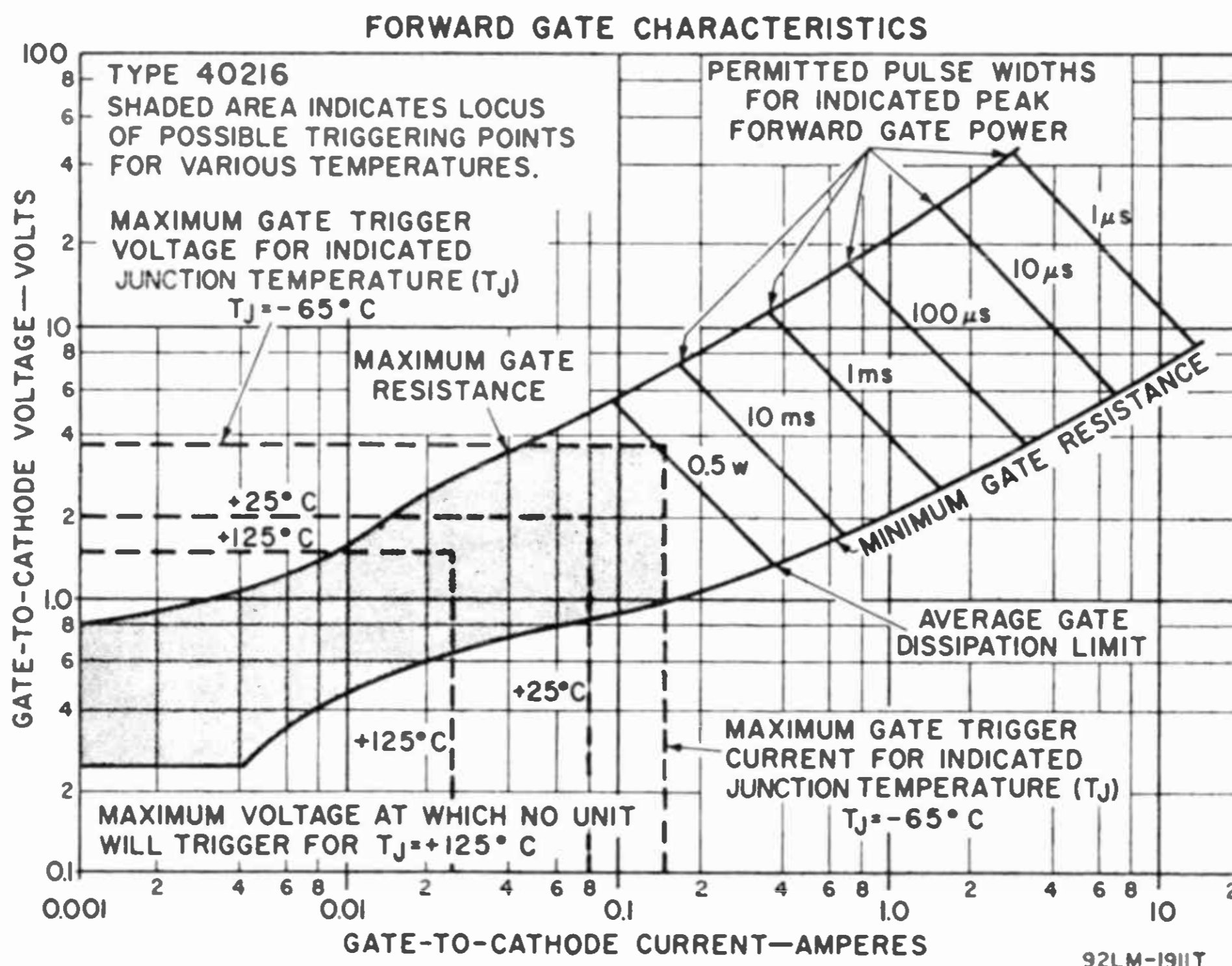
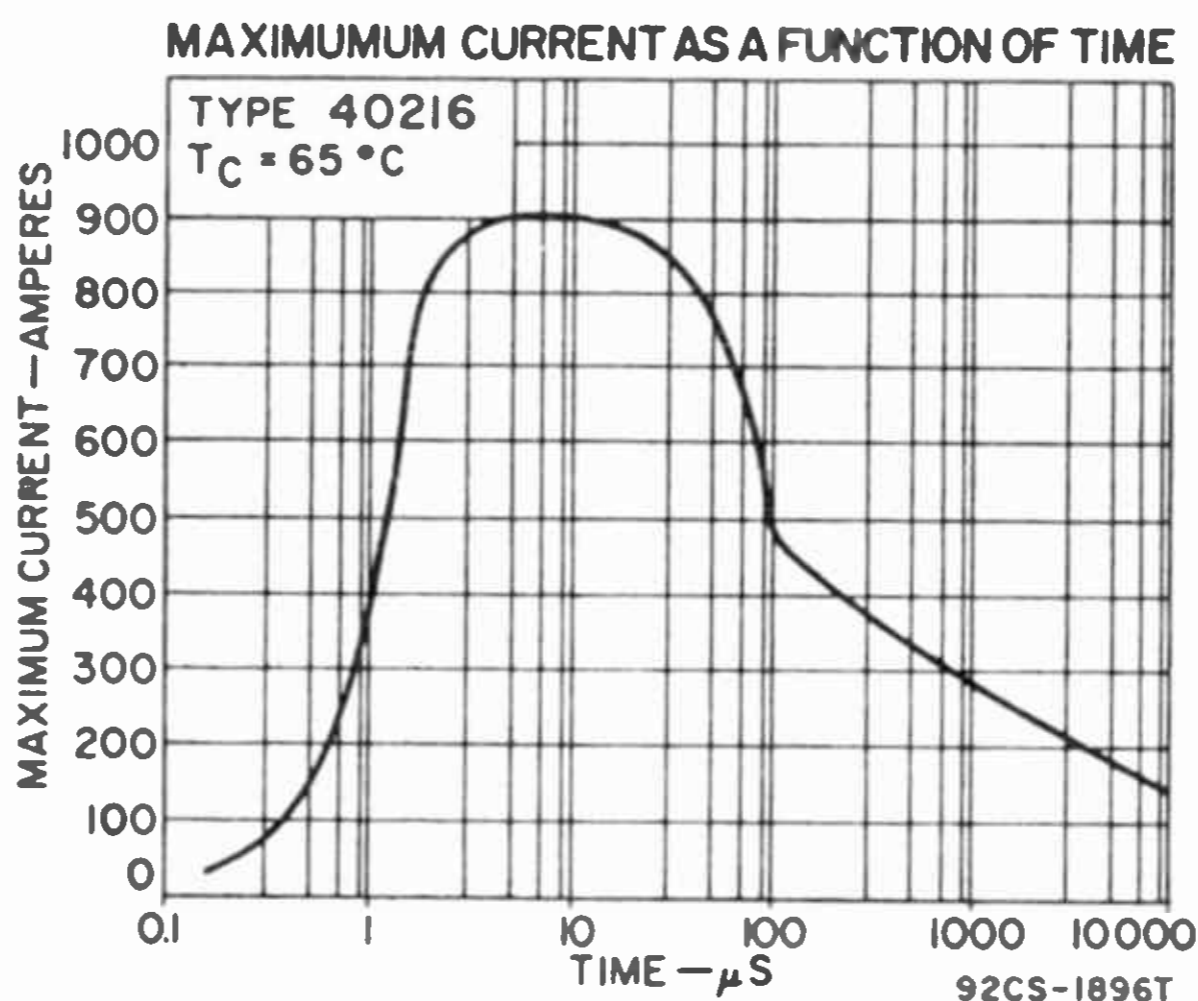


MAXIMUM RATINGS

V_{RSOM}	720	V
V_{RROM}	600	V
V_{DROM}	600	V
$I_{T(RMS)}$ ($T_C = 65^{\circ}\text{C}$)	35	A
I_{TRM}	900	A
P_M ($T_C = 65^{\circ}\text{C}$)	30	W
P_{GM} (peak, forward or reverse, for 10 μs)	40	W
$P_{G(AV)}$	0.5	W
T_{stg}	-65 to 150	$^{\circ}\text{C}$
T_C	-65 to 125	$^{\circ}\text{C}$

CHARACTERISTICS (At maximum electrical rating at $T_c = 25^\circ\text{C}$)

$V_{F(BO)0}$ ($T_c = 125^\circ\text{C}$)	600 min	V
I_{DOM} ($T_c = 125^\circ\text{C}$)	10 max	mA
I_{RROM} ($T_c = 125^\circ\text{C}$)	10 max	mA
I_{GT}	1 min, 25 typ, 80 max	mA (dc)
V_{GT}	1.1 typ; 2 max	V (dc)
i_{HO}	0.5 to 70	mA
Critical dv/dt ($V_D = V_{F(BO)0}$ min value, exponential rise, $T_c = 125^\circ\text{C}$)	20 min; 50 typ	μs
t_{gt} ($V_D = V_{F(BO)0}$ min value, $i_T = 30$ A, $I_{GT} = 200$ mA, $t_r = 0.1 \mu\text{s}$)	1.25	μs
t_q ($i_T = 18$ A, $50 \mu\text{s}$ pulse width, $dv_D/dt = 20$ V/ μs , $di_R/dt = 30$ A/ μs , $I_{GT} = 200$ mA, $T_c = 80^\circ\text{C}$)	15 to 40	μs
θ_{J-C}	2 max	$^\circ\text{C}/\text{W}$



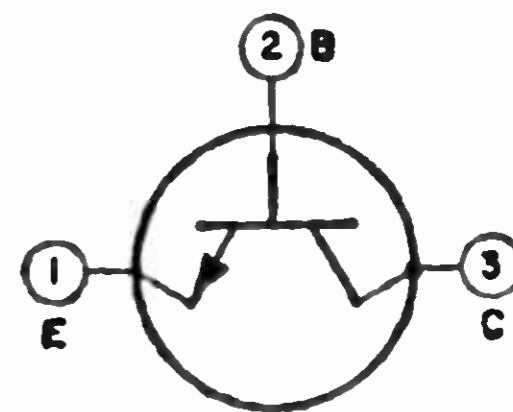
- Refer to Chart of Discontinued Transistors **40217**
- Refer to Chart of Discontinued Transistors **40218**
- Refer to Chart of Discontinued Transistors **40219**
- Refer to Chart of Discontinued Transistors **40220**

40221 Refer to Chart of Discontinued Transistors

40222 Refer to Chart of Discontinued Transistors

40231 TRANSISTOR

Si n-p-n planar type used in low-to-intermediate-signal-level af amplifier circuits, such as preamplifiers, "voltage amplifiers", and driver stages in consumer and industrial equipment. JEDEC TO-104, Outline No.32.



MAXIMUM RATINGS

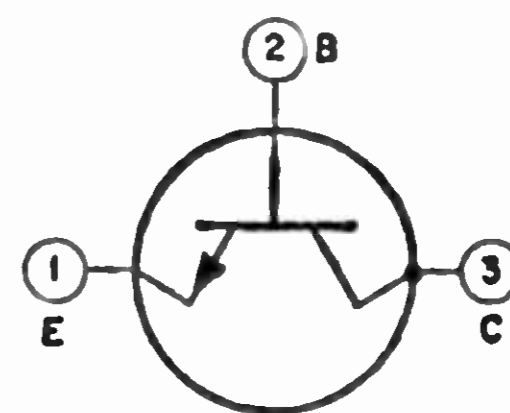
Collector-to-Base Voltage	V_{CB0}	18	V
Collector-to-Emitter Voltage	V_{CE0}	18	V
Emitter-to-Base Voltage	V_{EB0}	5	V
Collector Current	I_C	100	mA
Emitter Current	I_E	-100	mA
Base Current	I_B	25	mA
Transistor Dissipation:			
T_A up to 25°C	P_T	0.5	W
T_A above 25°C	P_T	See curve page 300	
T_C up to 125°C	P_T	1	W
T_C above 125°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 175	°C
Storage	T_{STG}	-65 to 175	°C
Lead-Soldering Temperature (10 s max)	T_L	255	°C

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = 50 \mu A$, $I_E = 0$)	$V_{(BR)CBO}$	18 min	V
Collector-to-Emitter Breakdown Voltage ($I_C = 10 mA$, $I_B = 0$)	$V_{(BR)CEO}$	18 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 50 \mu A$, $I_C = 0$)	$V_{(BR)EBO}$	5 min	V
Collector-Cutoff Current:			
$V_{CB} = 12 V$, $I_E = 0$, $T_A = 25^\circ C$	I_{CBO}	0.5 max	μA
$V_{CB} = 12 V$, $I_E = 0$, $T_A = 85^\circ C$	I_{CBO}	10 max	μA
Emitter-Cutoff Current ($V_{EB} = 2.5 V$, $I_C = 0$)	I_{EBO}	0.5 max	μA
Small-Signal Forward-Current Transfer Ratio			
($I_C = 2 mA$, $V_{CE} = 10 V$, $f = 1 kHz$)	h_{fe}	55 to 180	
Gain-Bandwidth Product ($V_{CE} = 6 V$, $I_C = 1 mA$)	f_T	60	MHz
Intrinsic Base-Spreading Resistance ($V_{CE} = 6 V$, $I_C = 1 mA$, $f = 100 MHz$)			
	$r_{bb'}$	20	Ω
Output Capacitance ($V_{CB} = 6 V$, $I_E = 0$, $f = 1 MHz$)			
	C_{obo}	22	pF
Noise Figure ($R_G = 1000 \Omega$, $V_{CE} = 6 V$, $I_C = 0.1 mA$, circuit bandwidth = 1 Hz, $f = 10 kHz$)			
	NF	2.8	dB
Thermal Resistance, Junction-to-Case			
($T_J = 175^\circ C$)	θ_{J-C}	50 max	°C/W
Thermal Resistance, Junction-to-Ambient			
($T_J = 175^\circ C$)	θ_{J-A}	300 max	°C/W

40232 TRANSISTOR

Si n-p-n planar type used in low-to-intermediate-signal-level af amplifier circuits, such as preamplifiers, "voltage amplifiers", and driver stages in consumer and industrial equipment. JEDEC TO-104, Outline No.32. This type is identical with type 40231 except for the following item:

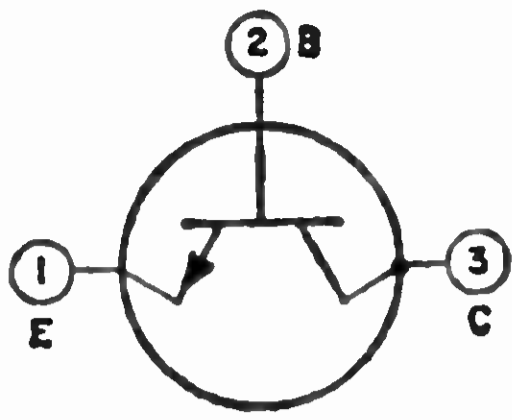


CHARACTERISTICS

Small-Signal Forward-Current Transfer Ratio ($I_C = 2 mA$, $V_{CE} = 10 V$, $f = 1 kHz$)	h_{fe}	90 to 300
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TRANSISTOR

40233



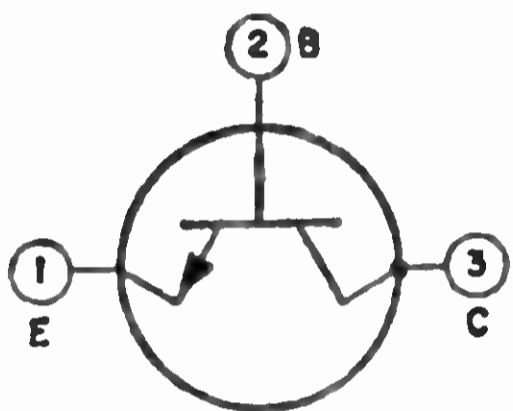
Si n-p-n planar type used in low-to-intermediate-signal-level af amplifier circuits, such as preamplifiers, "voltage amplifiers", and driver stages in consumer and industrial equipment. JEDEC TO-104, Outline No.32. This type is identical with type 40231 except for the following items:

CHARACTERISTICS

Collector-Cutoff Current ($V_{CB} = 12\text{ V}$, $I_E = 0$, $T_A = 25^\circ\text{C}$)	I_{CBO}	0.25 max	μA
Emitter-Cutoff Current ($V_{EB} = 2.5\text{ V}$, $I_C = 0$)	I_{EBO}	0.25 max	μA
Small-Signal Forward-Current Transfer Ratio ($I_C = 2\text{ mA}$, $V_{CE} = 10\text{ V}$, $f = 1\text{ kHz}$)	h_{fe}	90 to 300	
Noise Figure: $R_G = 1000\ \Omega$, $V_{CE} = 6\text{ V}$, $I_C = 0.1\text{ mA}$, circuit bandwidth = 1 Hz, $f = 10\text{ kHz}$	NF	2	dB
$R_G = 1000\ \Omega$, $V_{CE} = 6\text{ V}$, $I_C = 0.5\text{ mA}$, circuit bandwidth = 1 Hz, $f = 1\text{ kHz}$	NF	6 max	dB

TRANSISTOR

40234



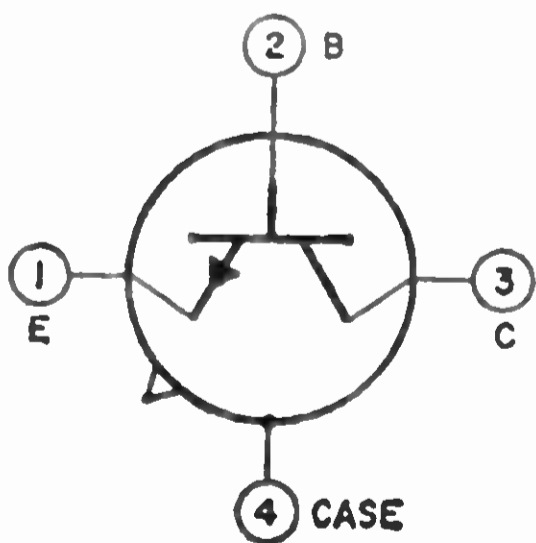
Si n-p-n planar type used in low-to-intermediate-signal-level af amplifier circuits, such as preamplifiers, "voltage amplifiers"; and driver stages in consumer and industrial equipment. JEDEC TO-104, Outline No.32. This type is identical with type 40231 except for the following items:

MAXIMUM RATINGS

Transistor Dissipation: T_A up to 55°C	P_T	0.4	W
T_A above 55°C	P_T	See curve page 300	
T_A up to 125°C	P_T	1	W
T_C above 125°C	P_T	See curve page 300	

CHARACTERISTICS

Collector-to-Emitter Saturation Voltage ($I_C = 50\text{ mA}$, $I_B = 5\text{ mA}$)	$V_{CE(sat)}$	0.2	V
Small-Signal Forward-Current Transfer Ratio ($I_C = 2\text{ mA}$, $V_{CE} = 10\text{ V}$, $f = 1\text{ kHz}$)	h_{fe}	35 to 180	



TRANSISTOR

40235

Si n-p-n type used as rf amplifier in television tuners covering channels 2 through 13. JEDEC TO-104, Outline No.31.

MAXIMUM RATINGS

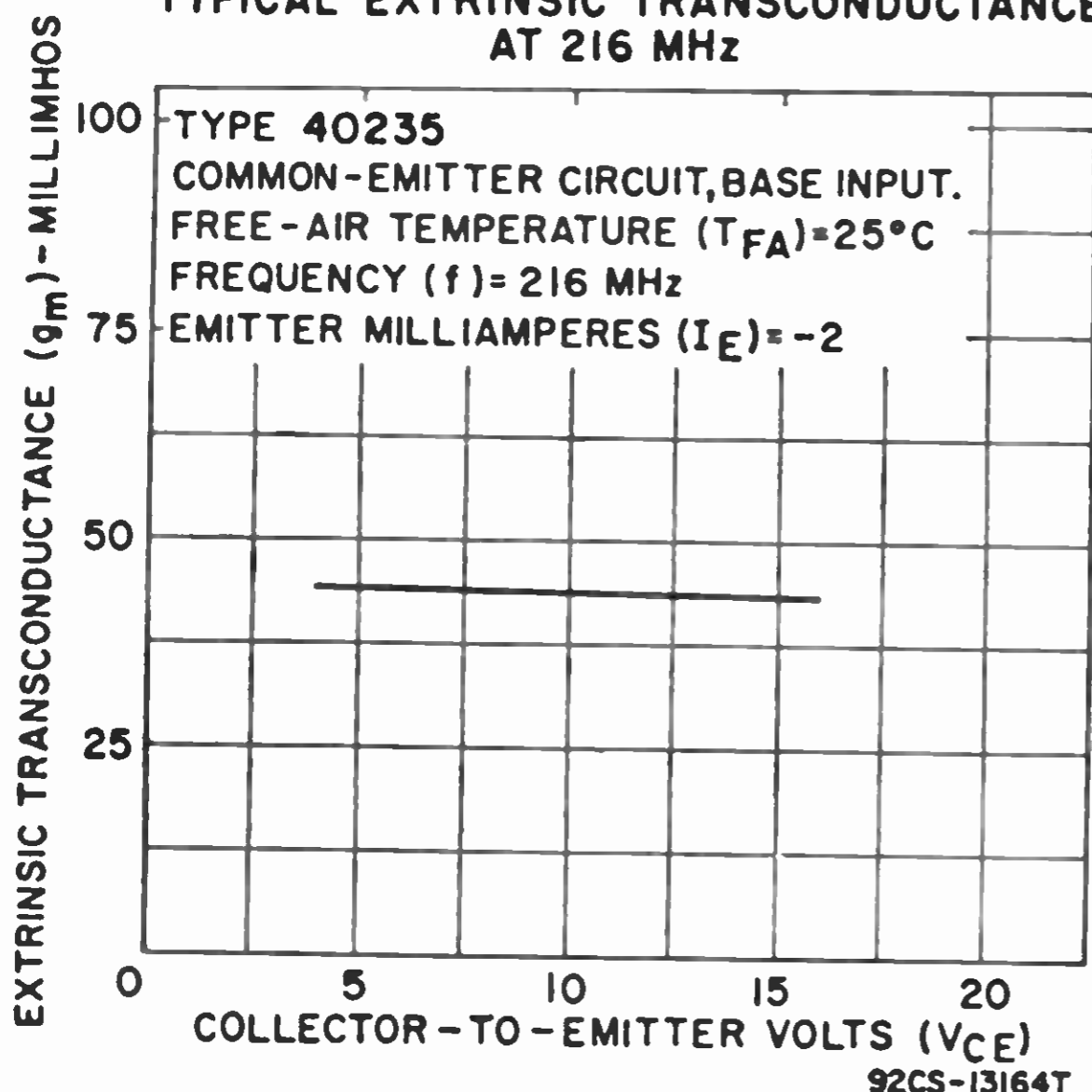
Collector-to-Base Voltage: $V_{EB} = 1\text{ V}$	V_{CBO}	45	V
Emitter open	V_{CBO}	45	V
Emitter-to-Base Voltage	V_{EBO}	4.5	V
Collector Current	I_C	50	mA
Transistor Dissipation: T_A up to 25°C	P_T	180	mW
T_A above 25°C	P_T	See curve page 300	
Temperature Range: Operating (T_A) and Storage (T_{STG})		-65 to 175	$^\circ\text{C}$
Lead Soldering Temperature (10 s max)	T_L	255	$^\circ\text{C}$

CHARACTERISTICS

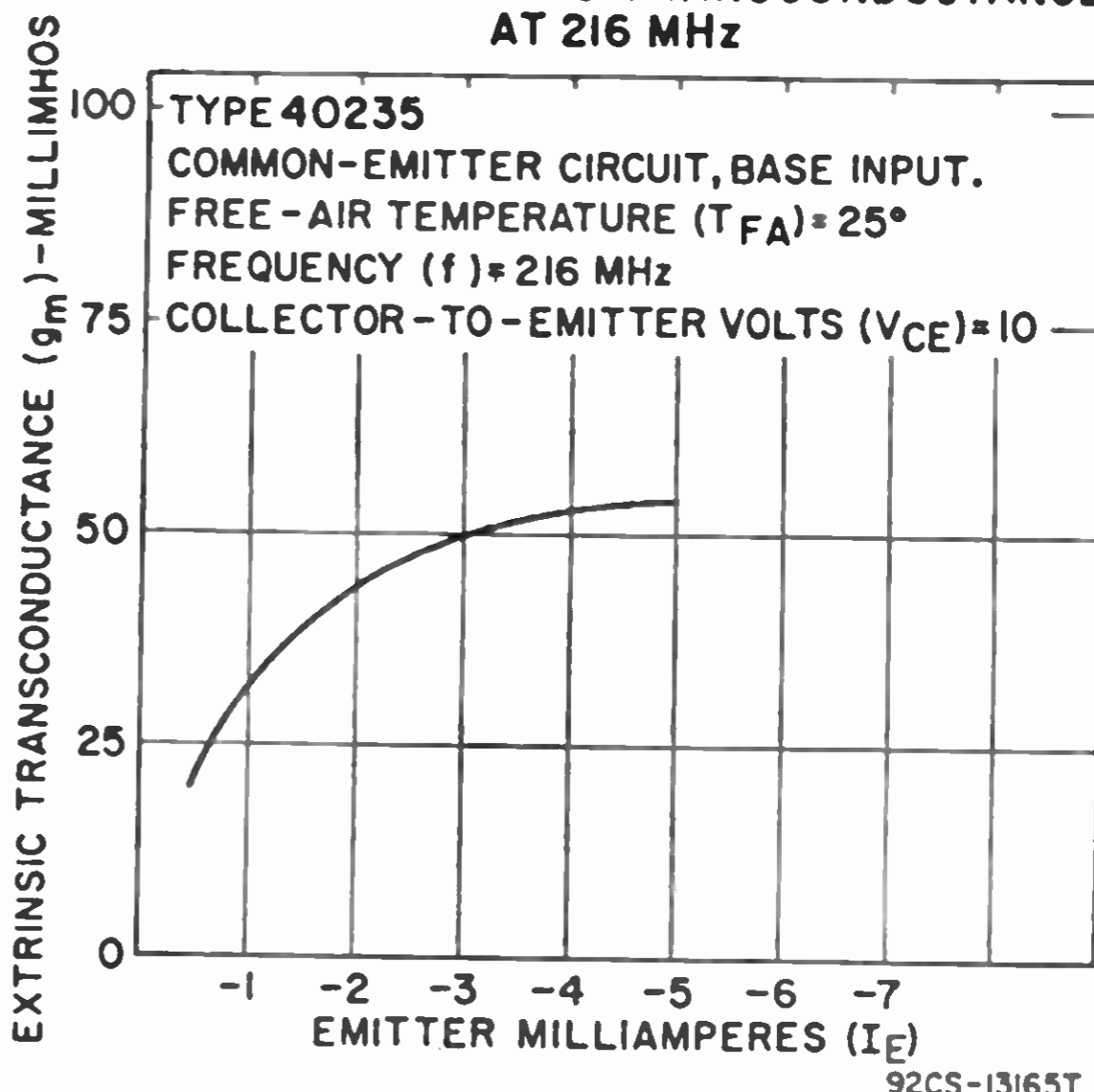
Collector-Cutoff Current:

$V_{CB} = 1 \text{ V}, I_E = 0$	I_{CBO}	0.02 max	μA
$V_{CB} = 35 \text{ V}, I_E = 0$	I_{CBO}	1 max	μA
Emitter-Cutoff Current ($V_{EB} = 4.5 \text{ V}, I_C = 0$)	I_{EBO}	1 max	μA

TYPICAL EXTRINSIC TRANSCONDUCTANCE AT 216 MHz



TYPICAL EXTRINSIC TRANSCONDUCTANCE AT 216 MHz



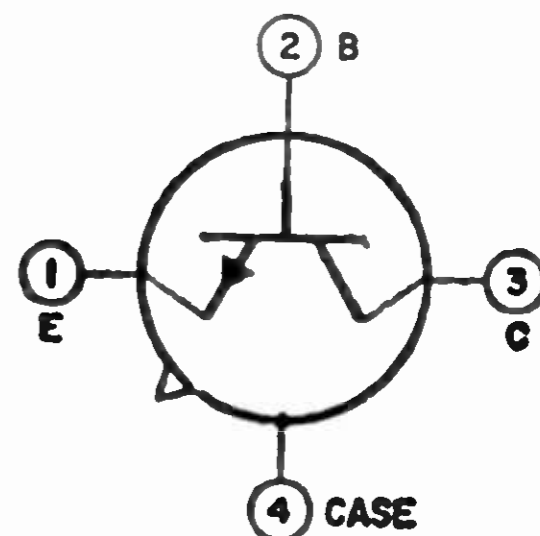
Static Forward-Current Transfer Ratio

($V_{CE} = 6 \text{ V}, I_E = -1 \text{ mA}$)	h_{FE}	40 to 170	
Gain-Bandwidth Product ($V_{CE} = 6 \text{ V}, I_E = -2 \text{ mA}, f = 100 \text{ MHz}$)	f_T	1000	MHz
Collector-to-Base Feedback Capacitance ($V_{CE} = 10 \text{ V}, I_E = -2 \text{ mA}, f = 216 \text{ MHz}$)	C_{cb}	0.65 max	pF
Input Resistance ($V_{CE} = 10 \text{ V}, I_E = -2 \text{ mA}, f = 216 \text{ MHz}$)	R_{i_e}	190	Ω
Output Resistance ($V_{CE} = 10 \text{ V}, I_E = -2 \text{ mA}, f = 216 \text{ MHz}$)	R_{o_e}	8.9	k Ω
Extrinsic Transconductance ($V_{CE} = 10 \text{ V}, I_E = -2 \text{ mA}, f = 216 \text{ MHz}$)	g_m	43.7	mmhos
Noise Figure ($V_{CE} = 10 \text{ V}, I_E = -2 \text{ mA}, R_G \text{ and } R_L = 50 \Omega, f = 216 \text{ MHz}$)	NF	3.3	dB
Maximum Available Amplifier Gain ($V_{CE} = 10 \text{ V}, I_E = -2 \text{ mA}, f = 216 \text{ MHz}$)	MAG	29.1	dB
Maximum Usable Amplifier Gain, Neutralized ($V_{CE} = 10 \text{ V}, I_E = -2 \text{ mA}, R_G \text{ and } R_L = 50 \Omega, f = 216 \text{ MHz}$)	MUG	18.1	dB

40236

TRANSISTOR

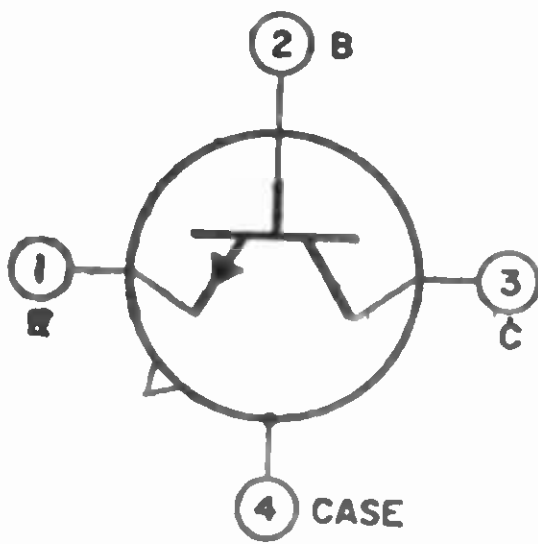
Si n-p-n type used as rf mixer in television tuners covering channels 2 through 13. JEDEC TO -104, Outline No.31. The maximum ratings for this type are identical with type 40235.



CHARACTERISTICS

Collector-Cutoff Current:

$V_{CB} = 1 \text{ V}, I_E = 0$	I_{CBO}	0.02 max	μA
$V_{CB} = 35 \text{ V}, I_E = 0$	I_{CBO}	1 max	μA
Emitter-Cutoff Current ($V_{EB} = 1 \text{ V}, I_C = 0$)	I_{CBO}	1 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 6 \text{ V}, I_E = -1 \text{ mA}$)	h_{FE}	40 to 275	
Gain-Bandwidth Product ($V_{CE} = 6 \text{ V}, I_E = -1 \text{ mA}, f = 100 \text{ MHz}$)	f_T	1000	MHz
Collector-to-Base Feedback Capacitance ($V_{CE} = 12 \text{ V}, I_E = 1.5 \text{ mA}, f = 216 \text{ MHz}$)	C_{cb}	0.65 max	pF
Input Resistance ($V_{CE} = 12 \text{ V}, I_E = -1.5 \text{ mA}, f = 216 \text{ MHz}$)	R_{i_e}	230	Ω
Output Resistance ($V_{CE} = 12 \text{ V}, I_E = -1.5 \text{ mA}, f = 45 \text{ MHz}$)	R_{o_e}	65	k Ω
Maximum Available Conversion Gain ($V_{CE} = 12 \text{ V}, I_E = -1.5 \text{ mA}, f = 216 \text{ to } 45 \text{ MHz}$)	MAG _c	19	dB



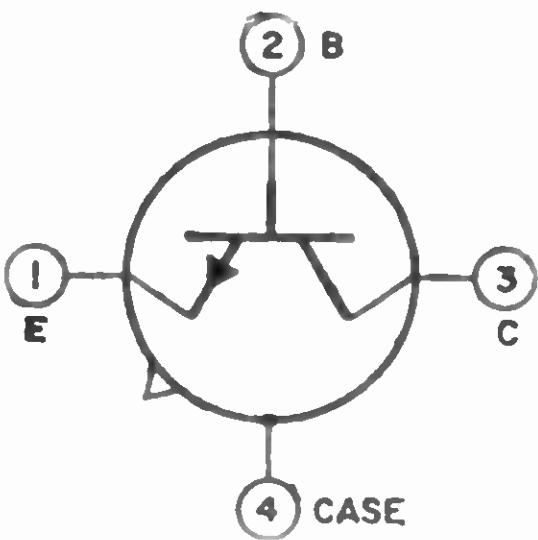
TRANSISTOR

40237

Si n-p-n type used as rf local oscillator in television tuners covering channels 2 through 13. JEDEC TO-104, Outline No.31. The maximum ratings for this type are identical with type 40235.

CHARACTERISTICS

Collector-Cutoff Current: $V_{CB} = 1\text{ V}, I_E = 0$	I_{CBO}	0.02 max	μA
$V_{CB} = 35\text{ V}, I_E = 0$	I_{CBO}	1 max	μA
Emitter-Cutoff Current ($V_{EB} = 1\text{ V}, I_C = 0$)	I_{EBO}	1 max	μA
Collector-to-Base Feedback Capacitance ($V_{CE} = 12\text{ V}, I_E = 1.5\text{ mA}, f = 216\text{ MHz}$)	C_{cb}	0.8 max	pF
Output Capacitance ($V_{CB} = 12\text{ V}, I_C = -2.5\text{ mA},$ $f = 257\text{ MHz}$)	C_{obo}	0.6 max	pF
Static Forward-Current Transfer Ratio ($V_{CE} = 6\text{ V}, I_E = -1\text{ mA}$)	h_{FE}	27 to 275	
Gain-Bandwidth Product ($V_{CE} = 6\text{ V}, I_E = -1\text{ mA},$ $f = 100\text{ MHz}$)	f_T	1000	MHz



TRANSISTOR

40238

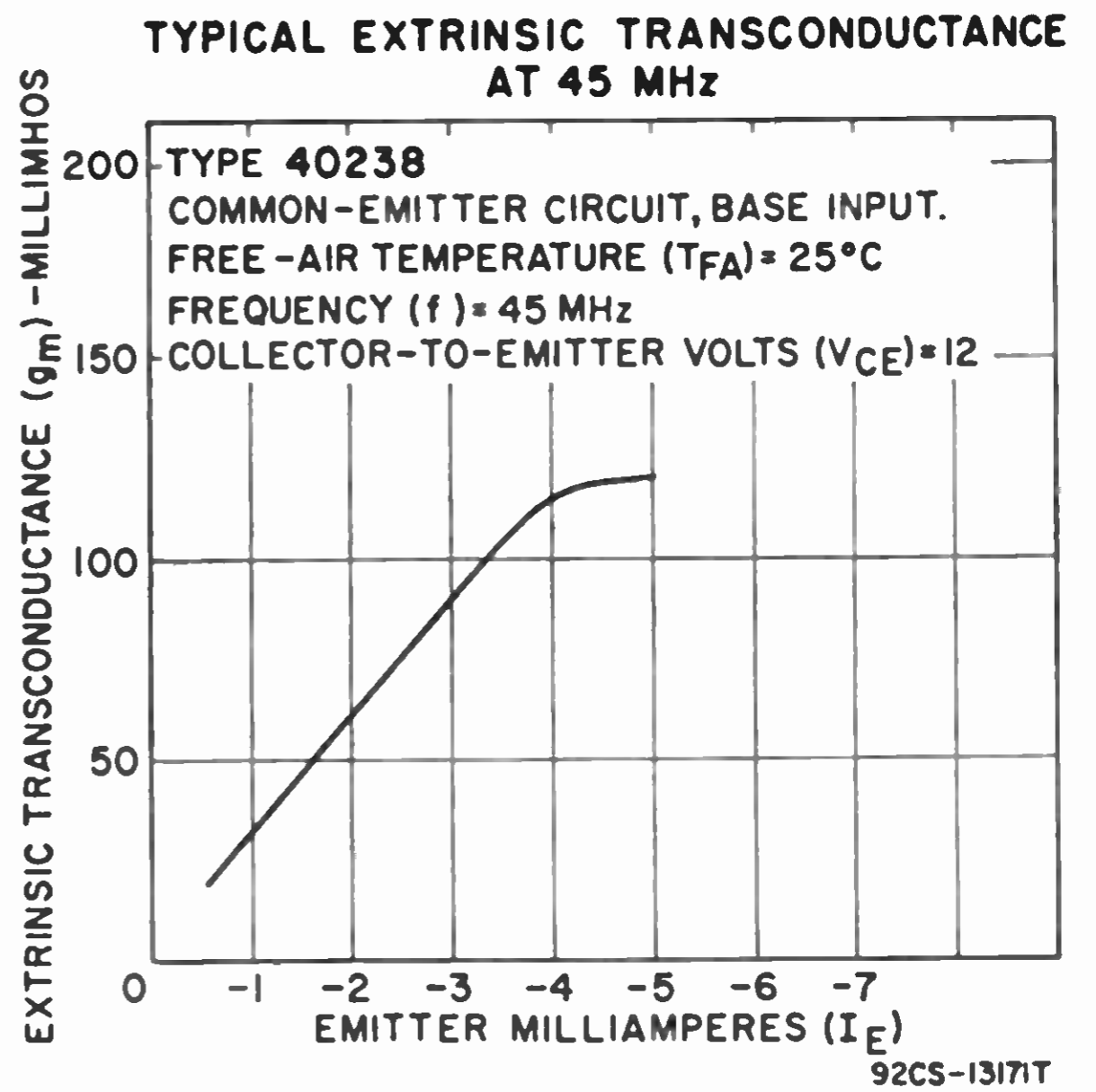
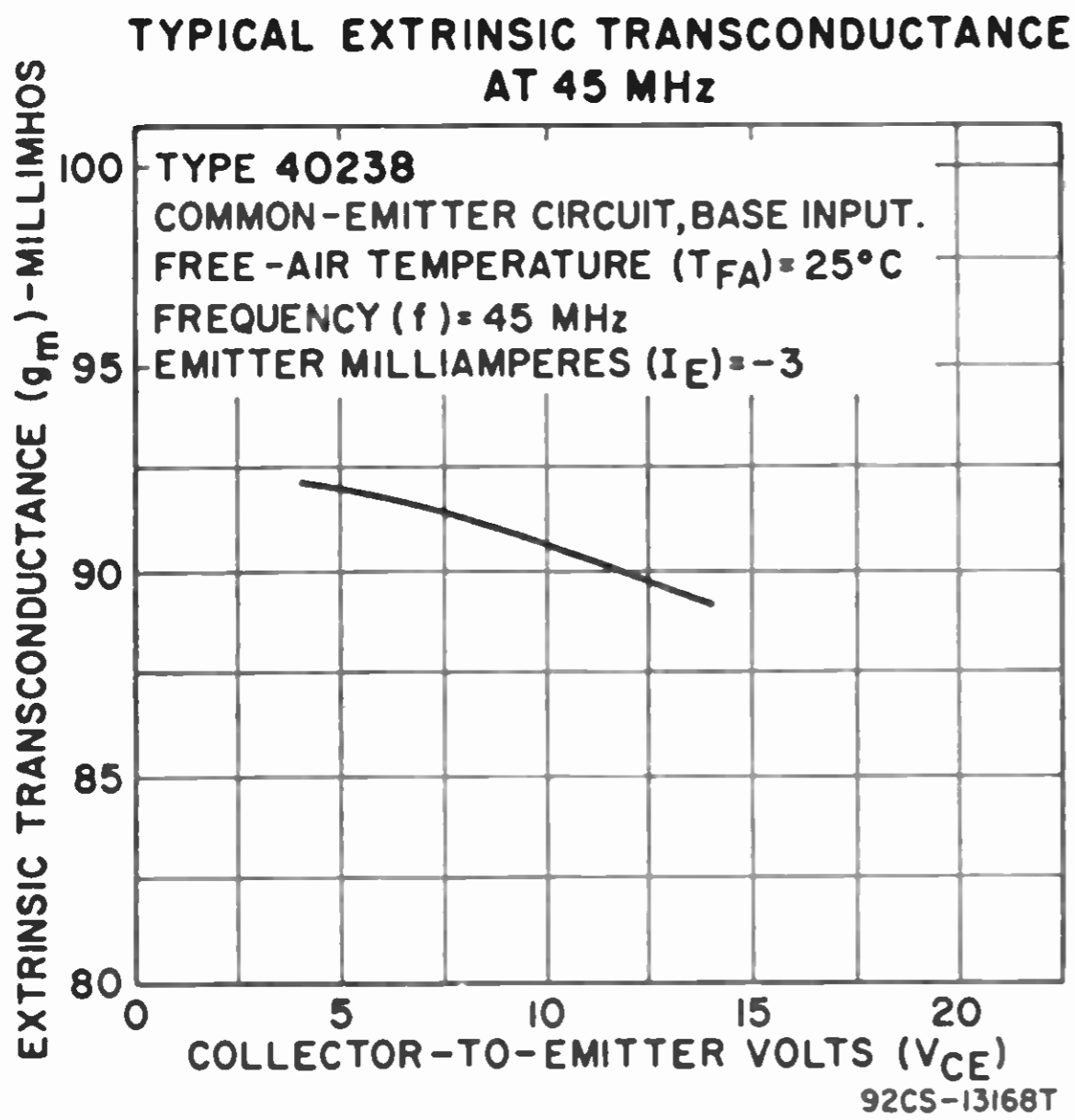
Si n-p-n type used as 45-MHz if amplifier in television receivers. JEDEC TO-104, Outline No.31.

MAXIMUM RATINGS

Collector-to-Base Voltage: $V_{BE} = -1\text{ V}$	V_{CBV}	45	V
Emitter open	V_{CBO}	45	V
Emitter-to-Base Voltage	V_{EBO}	4.5	V
Collector Current	I_C	50	mA
Transistor Dissipation: T_A up to 25°C	P_T	180	mW
T_A above 25°C	P_T	See curve page 300	
Temperature Range: Operating (T_A) and Storage (T_{STG})		-65 to 175	$^\circ\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	255	$^\circ\text{C}$

CHARACTERISTICS

Collector-Cutoff Current: $V_{CB} = 1\text{ V}, I_E = 0$	I_{CBO}	0.02 max	μA
$V_{CB} = 35\text{ V}, I_E = 0$	I_{CBO}	1 max	μA
Emitter-Cutoff Current ($V_{EB} = 1\text{ V}, I_C = 0$)	I_{EBO}	1 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 6\text{ V}, I_E = -1\text{ mA}$)	h_{FE}	40 to 170	
Gain-Bandwidth Product ($V_{CE} = 6\text{ V}, I_E = -2\text{ mA},$ $f = 100\text{ MHz}$)	f_T	800	MHz
Collector-to-Base Feedback Capacitance ($V_{CE} = 12\text{ V}, I_E = -3\text{ mA}, f = 216\text{ MHz}$)	C_{cb}	0.65 max	pF
Input Resistance ($V_{CE} = 12\text{ V}, I_E = -3\text{ mA},$ $f = 45\text{ MHz}$)	$R_{i\theta}$	480	Ω
Output Resistance ($V_{CE} = 12\text{ V}, I_E = -3\text{ mA},$ $f = 45\text{ MHz}$)	$R_{o\theta}$	35	k Ω
Extrinsic Transconductance ($V_{CE} = 12\text{ V}, I_E = -3\text{ mA},$ $f = 45\text{ MHz}$)	g_m	90	mmhos
Maximum Available Amplifier Gain For 1, 2, or 3 Stages ($V_{CE} = 12\text{ V}, I_E = -3\text{ mA}, f = 45\text{ MHz}$) ...	MAG	45.3	dB
Maximum Usable Amplifier Gain, Unneutralized ($V_{CE} = 12\text{ V}, I_E = -3\text{ mA}, f = 45\text{ MHz}$):			
For 1 stage	MUG	22.9	dB
For 2 stages	MUG	20.7	dB
For 3 stages	MUG	19	dB
Maximum Usable Amplifier Gain, Neutralized ($V_{CE} = 12\text{ V}, I_E = -3\text{ mA}, f = 45\text{ MHz}$):			
For 1 stage	MUG	28	dB
For 2 stages	MUG	25.8	dB
For 3 stages	MUG	24.1	dB

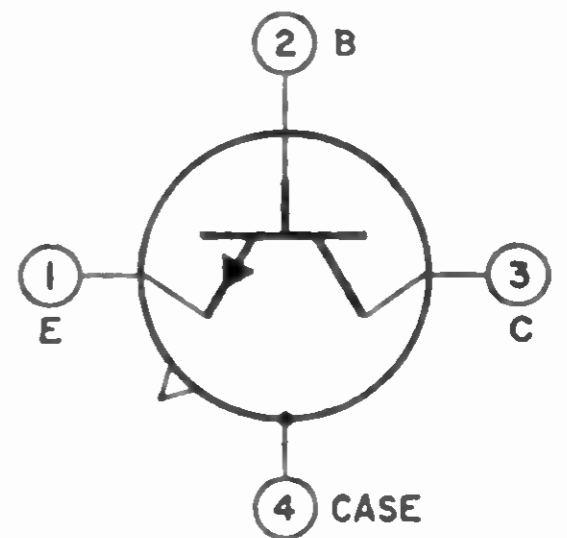


40239 TRANSISTOR

Si n-p-n type used as 45-MHz if amplifier in television receivers. JEDEC TO-104, Outline No.31. This type is identical with type 40238 except for the following item:

CHARACTERISTICS

Static Forward-Current Transfer Ratio (V _{CE} = 6 V, I _E = -1 mA)	h _{FE}	27 to 100
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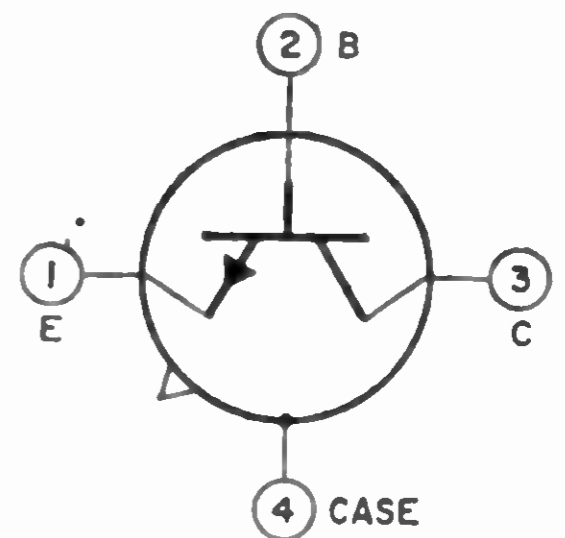


40240 TRANSISTOR

Si n-p-n type used as 45-MHz if amplifier in television receivers. JEDEC TO-104, Outline No.31. This type is identical with type 40238 except for the following item:

CHARACTERISTICS

Static Forward-Current Transfer Ratio (V _{CE} = 6 V, I _E = -1 mA)	h _{FE}	27 to 275
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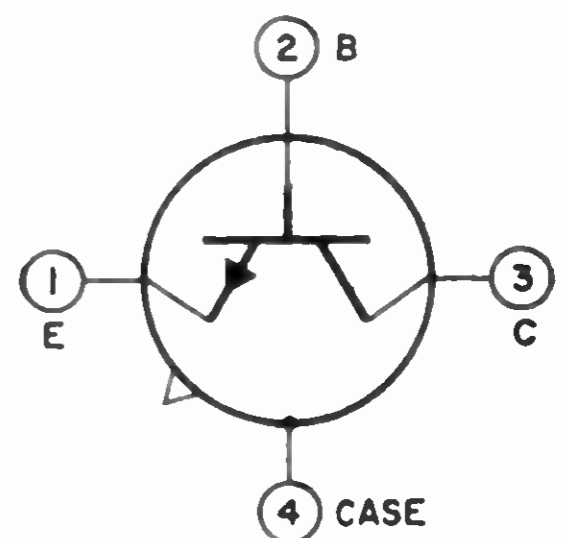


40242 TRANSISTOR

Si n-p-n planar type used in rf-amplifier applications in conjunction with types 40243 (mixer), 40244 (rf oscillator), and 40245 and 40246 (if amplifiers) to make up a "front-end" and if complement for FM and AM/FM receivers. JEDEC TO-104, Outline No.31.

MAXIMUM RATINGS

Collector-to-Base Voltage:			
Emitter open	V _{CB0}	45	V
V _{EB} = -1 V	V _{CE0}	45	V
Collector-to-Emitter Voltage	V _{CBV}	45	V
Emitter-to-Base Voltage	V _{EBO}	4.5	V
Collector Current	I _C	50	mA
Transistor Dissipation:			
T _A up to 25°C	P _T	180	mW
T _A above 25°C	P _T	See curve	page 300



MAXIMUM RATINGS (cont'd)

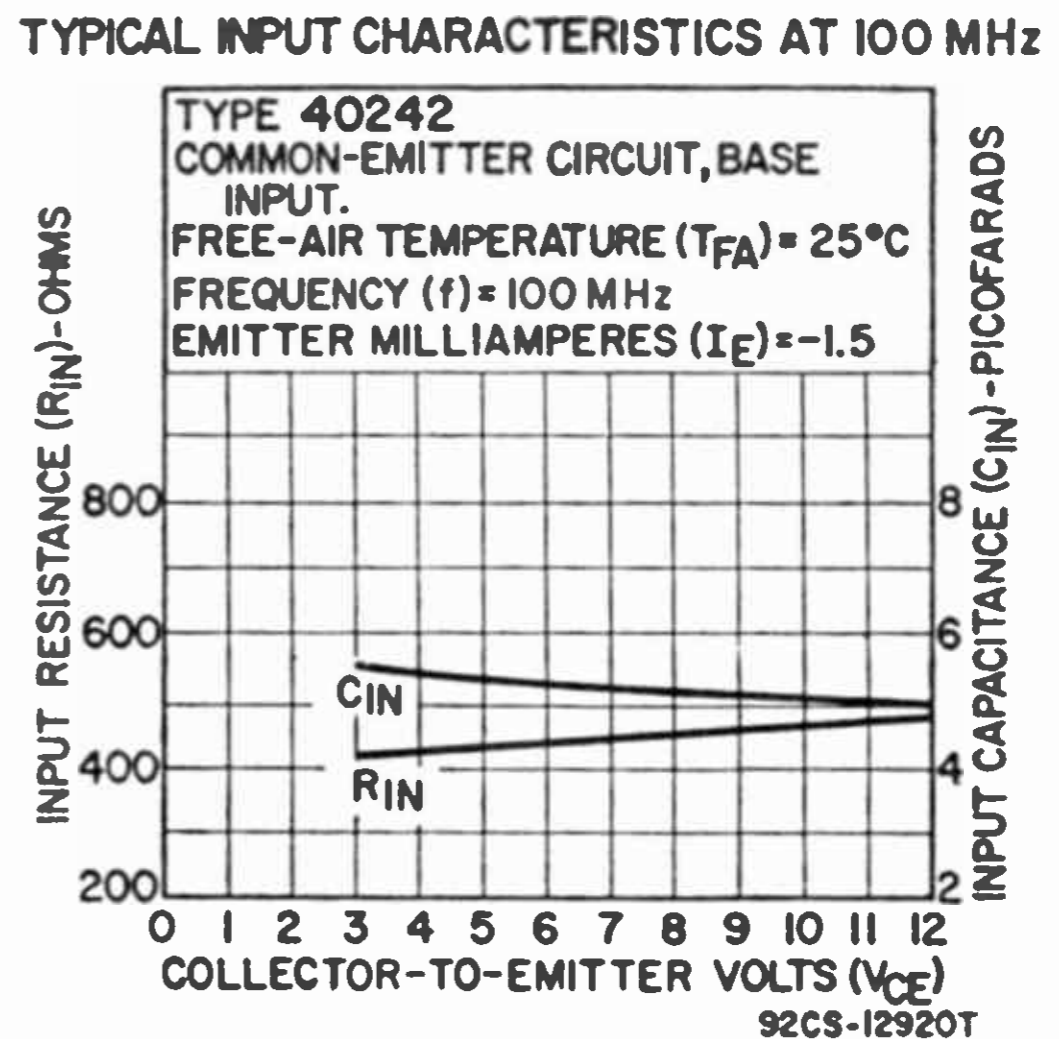
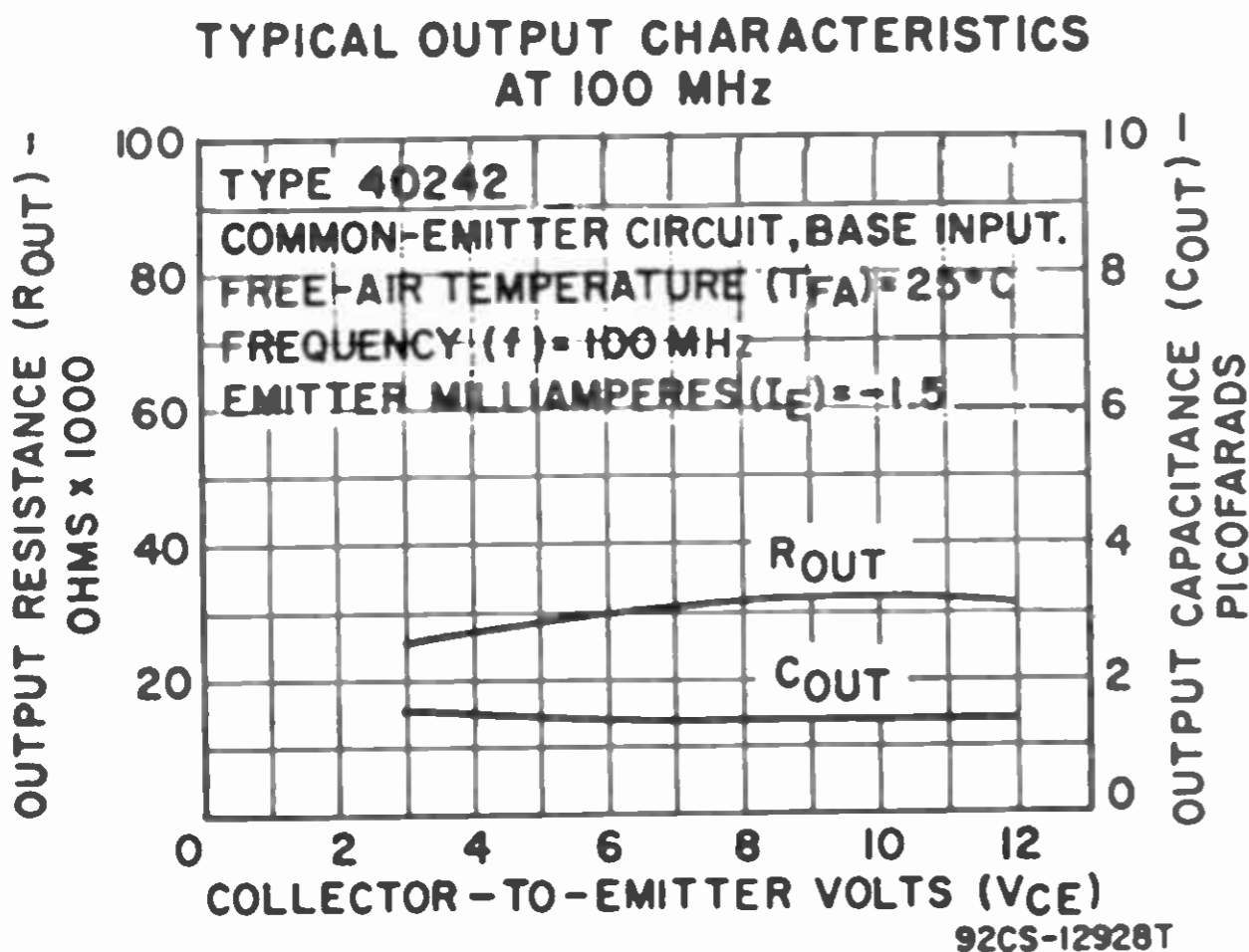
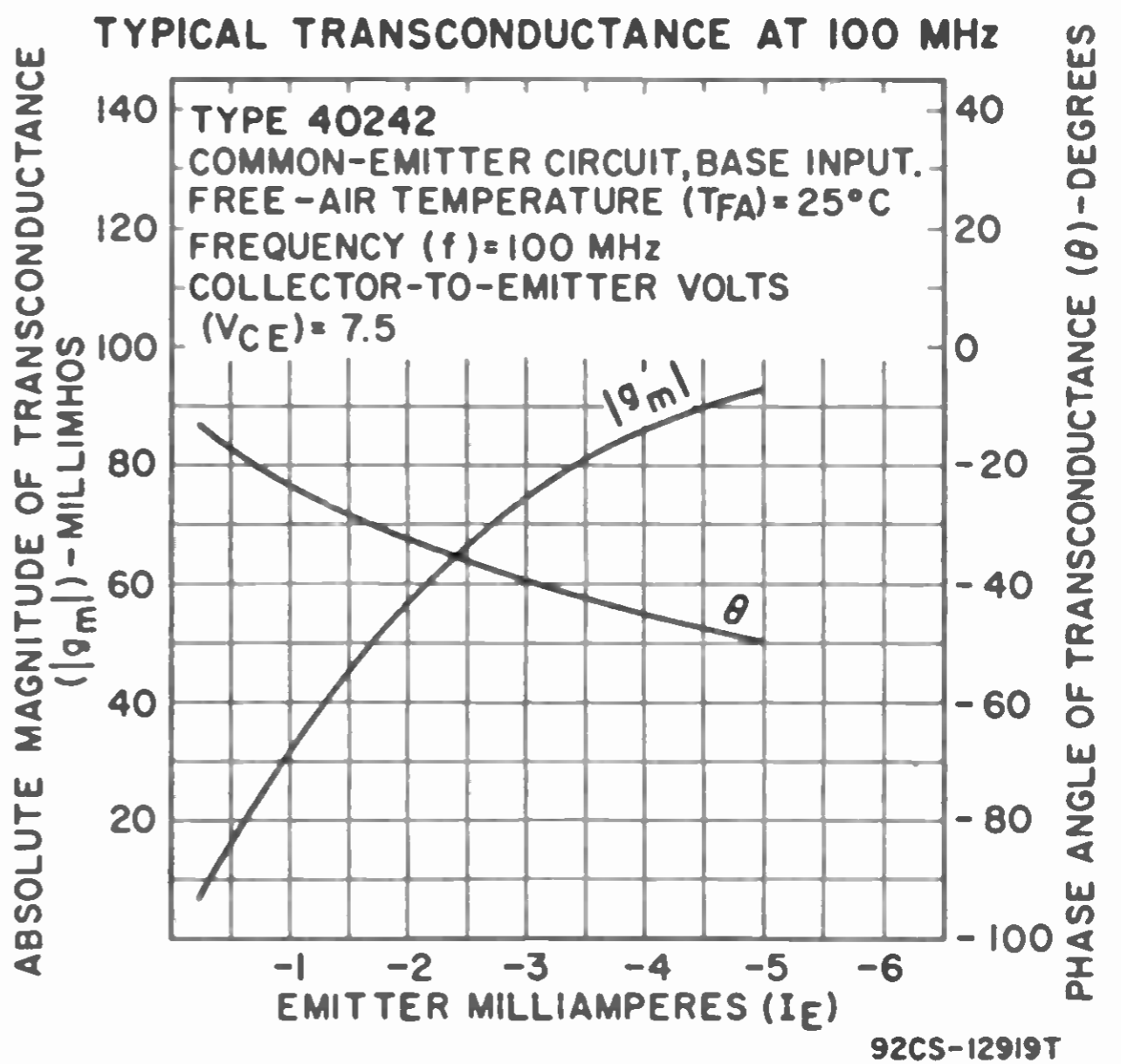
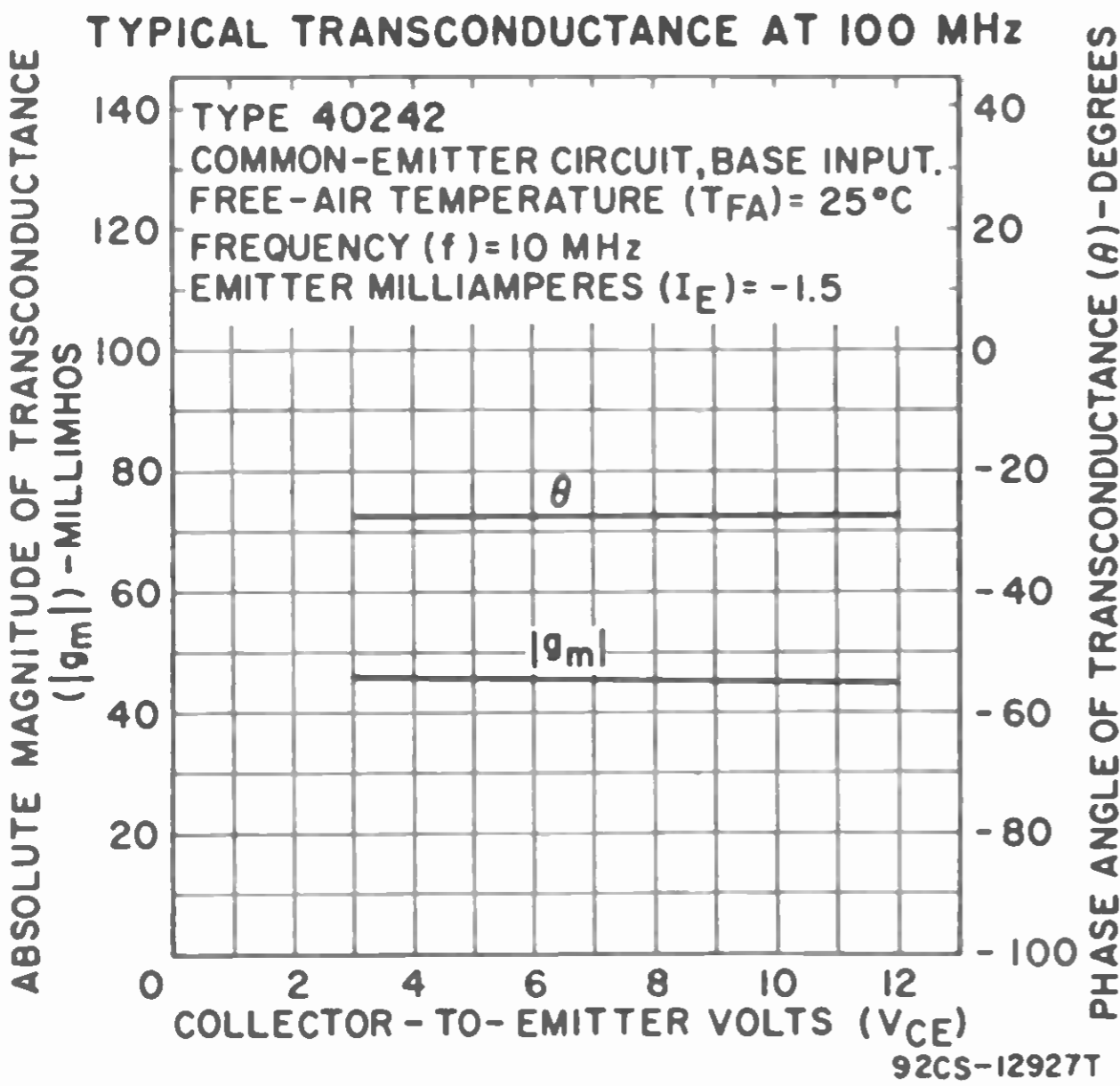
Temperature Range:

Operating (T_A) and Storage (T_{STG})		-65 to 175	°C
Lead-Soldering Temperature (10 s max)	T_L	255	°C

CHARACTERISTICS

Collector-to-Base Breakdown Voltage:

$I_C = 0.001$ mA, $I_E = 0$	$V_{(BR)CBO}$	45 min	V
$V_{EB} = -1$ V, $I_C = 0.001$ mA	$V_{(BR)CBV}$	45 min	V
Collector-to-Emitter Breakdown Voltage ($I_E = 0.5$ mA, $I_B = 0$)	$V_{(BR)CEO}$	45 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -0.001$ mA, $I_C = 0$)	$V_{(BR)EBO}$	4.5 min	V
Collector-Cutoff Current ($V_{CE} = 1$ V, $I_E = 0$)	I_{CBO}	0.02 max	μ A
Emitter-Cutoff Current ($V_{CE} = 1.5$ V, $I_C = 0$)	I_{EBO}	1 max	μ A
Static Forward-Current Transfer Ratio ($V_{CE} = 6$ V, $I_E = -1$ mA)	h_{FE}	40 to 170	
Extrinsic Transconductance ($V_{CE} = 7.5$ V, $I_E = -1.5$ mA, $f = 100$ MHz)	g_m	45	mmhos
Maximum Available Amplifier Gain* ($V_{CE} = 7.5$ V, $I_E = -1.5$ mA, $f = 100$ MHz)	MAG	38.3	dB
Maximum Usable Amplifier Gain*: Neutralized— $V_{CE} = 7.5$ V, $I_E = -1.5$ mA, $f = 100$ MHz	MUG	21.5	dB
Unneutralized— $V_{CC} = 15$ V, $f = 100$ MHz	MUG	16.4	dB
Input Capacitance ($V_{CE} = 7.5$ V, $I_E = -1.5$ mA, $f = 100$ MHz)	C_{ie}	5.2	pF
Feedback Capacitance ($V_{CE} = 8$ V, $I_E = 0$, $f = 1$ MHz)	C_{cb}	0.65 max	pF
Input Resistance ($V_{CE} = 7.5$ V, $I_E = -1.5$ mA, $f = 100$ MHz)	R_{ie}	450	Ω
Output Resistance ($V_{CE} = 7.5$ V, $I_E = -1.5$ mA, $f = 100$ MHz)	R_{oe}	30	k Ω



CHARACTERISTICS (cont'd)

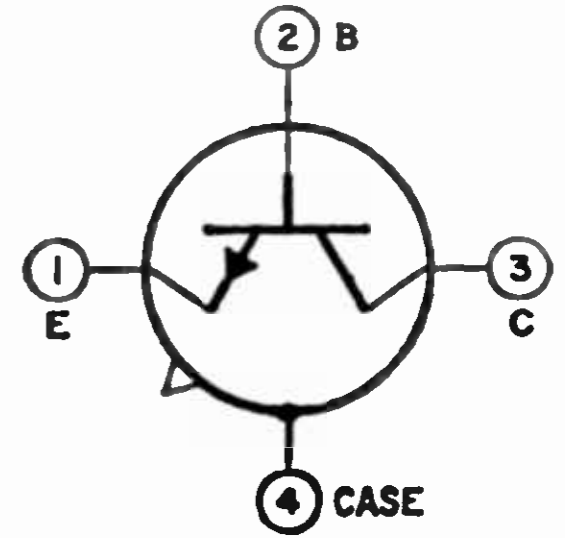
Output Capacitance ($V_{CE} = 7.5 \text{ V}$, $I_E = -1.5 \text{ mA}$, $f = 100 \text{ MHz}$)	C_{oe}	1.35	pF
Noise Figure* ($V_{CC} = 15 \text{ V}$, $R_G = 50 \Omega$, $f = 100 \text{ MHz}$)	NF	2.5	dB

* This characteristic applies only to type 40242.

40243

TRANSISTOR

Si n-p-n planar type used in mixer applications in conjunction with types 40242 (rf amplifier), 40244 (rf oscillator), and 40245 and 40246 (if amplifiers) to make up a "front-end" and if complement for FM and AM/FM receivers. JEDEC TO-104, Outline No.31. This type is identical with type 40242 except for the following items:



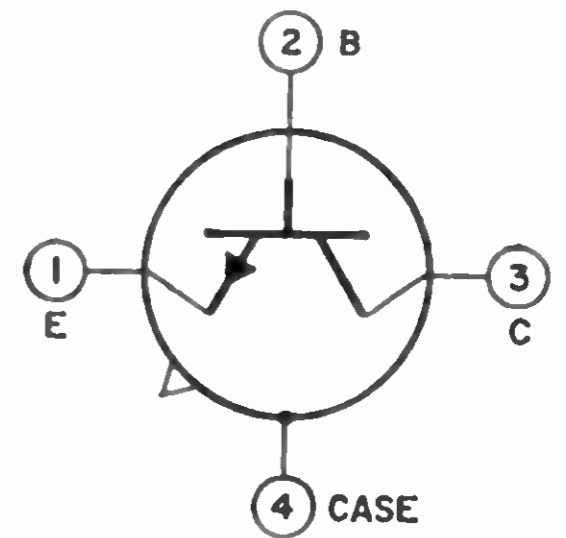
CHARACTERISTICS

Emitter-Cutoff Current ($V_{EB} = 3 \text{ V}$, $I_C = 0$)	I_{EBO}	1 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 6 \text{ V}$, $I_E = -1 \text{ mA}$)	h_{FE}	40 to 170	
Extrinsic Transconductance ($V_{CE} = 7.5 \text{ V}$, $I_E = -1 \text{ mA}$, $f = 100 \text{ MHz}$)	g_m	32	mmhos
Maximum Available Conversion Gain ($V_{CE} = 7.5 \text{ V}$, $I_E = -1 \text{ mA}$, $f = 10.7$ to 100 MHz) ...	MAG_c	37.64	dB
Input Capacitance ($V_{CE} = 7.5 \text{ V}$, $I_E = -1 \text{ mA}$, $f = 100 \text{ MHz}$)	C_{ie}	4.5	pF
Input Resistance ($V_{CE} = 7.5 \text{ V}$, $I_E = -1 \text{ mA}$, $f = 100 \text{ MHz}$)	R_{ie}	650	Ω
Output Resistance ($V_{CE} = 7.5 \text{ V}$, $I_E = -1 \text{ mA}$, $f = 100 \text{ MHz}$)	R_{oe}	30	k Ω
Output Capacitance ($V_{CE} = 7.5 \text{ V}$, $I_E = -1 \text{ mA}$, $f = 100 \text{ MHz}$)	C_{oe}	1.35	pF

40244

TRANSISTOR

Si n-p-n planar type used in rf-oscillator applications in conjunction with types 40242 (rf amplifier), 40243 (mixer), and 40245 and 40246 (if amplifiers) to make up a "front-end" and if complement for FM and AM/FM receivers. JEDEC TO-104, Outline No.31.

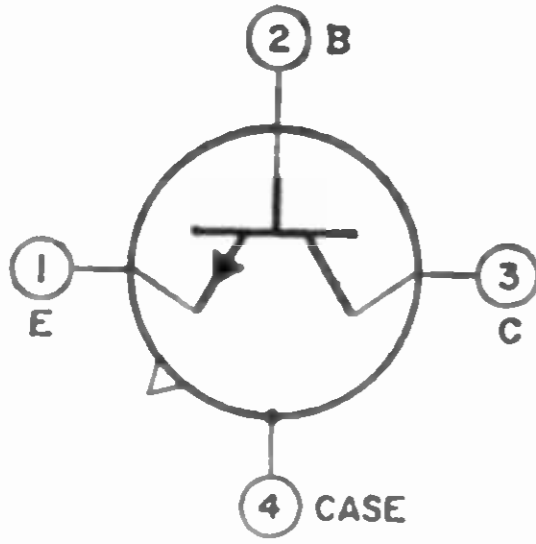


MAXIMUM RATINGS

Collector-to-Base Voltage:			
Emitter open	V_{CBO}	45	V
$V_{EB} = -1 \text{ V}$	V_{CBV}	45	V
Collector-to-Emitter Voltage	V_{CEO}	45	V
Emitter-to-Base Voltage	V_{EBO}	4.5	V
Collector Current	I_C	50	mA
Transistor Dissipation:			
T_A up to 25°C	P_T	180	mW
T_A above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (T_A) and Storage (T_{STG})	T_L	-65 to 175	$^\circ\text{C}$
Lead-Soldering Temperature (10 s max)		255	$^\circ\text{C}$

CHARACTERISTICS

Collector-to-Base Breakdown Voltage:			
$I_C = 0.001 \text{ mA}$, $I_E = 0$	$V_{(BR)CBO}$	45 min	V
$V_{BE} = -1 \text{ V}$, $I_C = 0.001 \text{ mA}$	$V_{(BR)CBV}$	45 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -0.001 \text{ mA}$, $I_C = 0$)	$V_{(BR)EBO}$	3 min	V
Collector-Cutoff Current ($V_{CE} = 1 \text{ V}$, $I_E = 0$)	I_{CBO}	0.02 max	μA
Emitter-Cutoff Current ($V_{EB} = 3 \text{ V}$, $I_C = 0$)	I_{EBO}	1 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 6 \text{ V}$, $I_E = -1 \text{ mA}$)	h_{FE}	27 to 170	
Oscillator Output Voltage, Common Base Circuit ($V_{CC} = 6 \text{ V}$, $R_L = 50 \Omega$, $f = 120 \text{ MHz}$)	V_{ob}	55	mV
Feedback Capacitance ($V_{CE} = 8 \text{ V}$, $I_E = 0$, $f = 1 \text{ MHz}$)	C_{cb}	0.8 max	pF



TRANSISTOR

40245

Si n-p-n planar type used in if-amplifier applications in conjunction with types 40242 (rf amplifier), 40243 (mixer), 40244 (rf oscillator), and 40246 (if amplifier) to make up a "front-end" and if complement for FM and AM/FM receivers. JEDEC TO-104, Outline No.31.

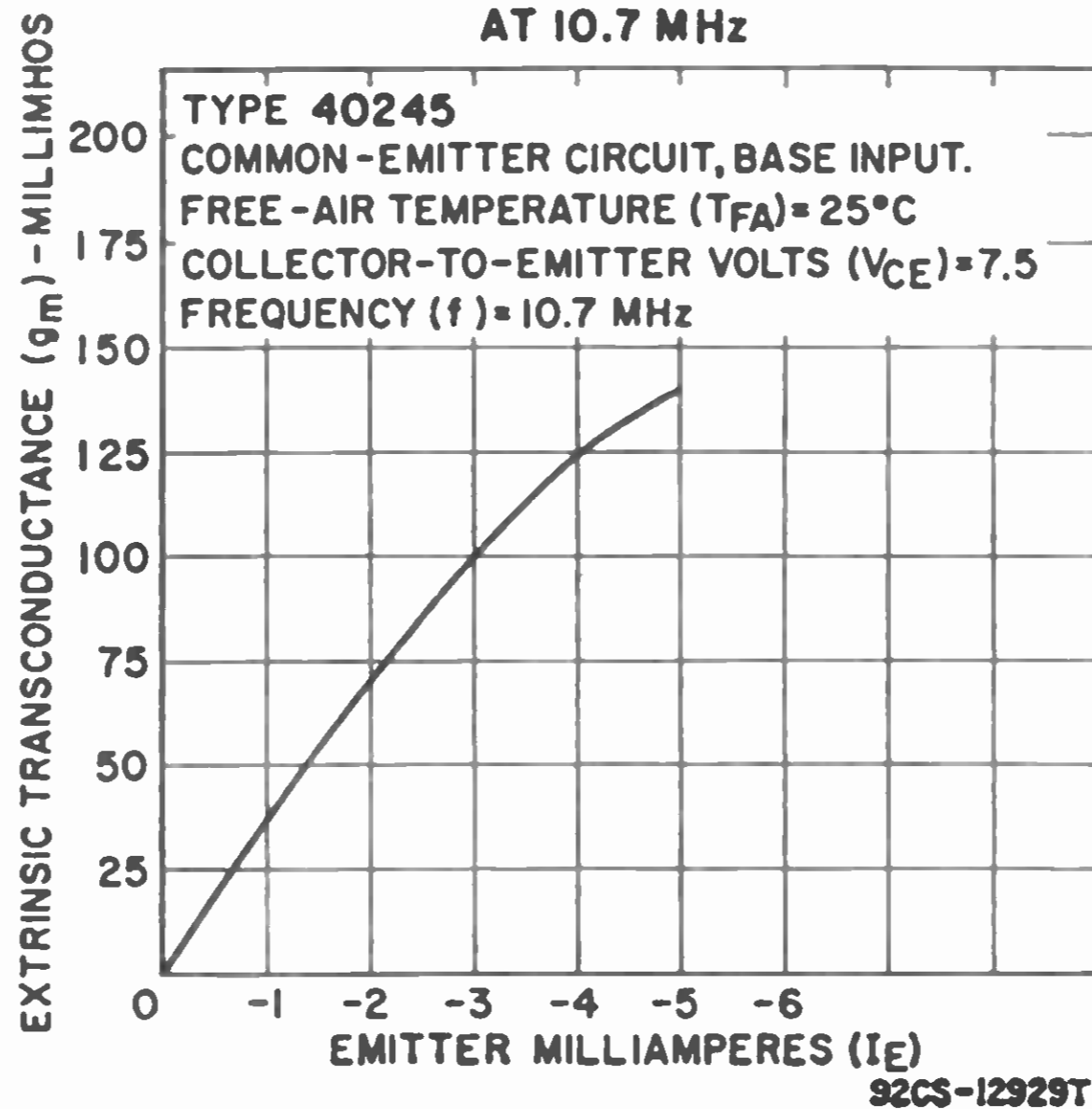
MAXIMUM RATINGS

Collector-to-Base Voltage:			
Emitter open	V_{CB0}	45	V
$V_{EB} = -1$ V	V_{CBV}	45	V
Collector-to-Emitter Voltage			
Emitter-to-Base Voltage	V_{CE0}	45	V
Collector Current	V_{EB0}	4.5	V
Transistor Dissipation:	I_C	50	mA
T_A up to 25°C	P_T	180	mW
T_A above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (T_A) and Storage (T_{STG})	T_L	-65 to 175	°C
Lead-Soldering Temperature (10 s max)		255	°C

CHARACTERISTICS

Collector-to-Base Breakdown Voltage:			
$I_C = 0.001$ mA, $I_E = 0$	$V_{(BR)CB0}$	45 min	V
$V_{BE} = -1$ V, $I_C = 0.001$ mA	$V_{(BR)CBV}$	45 min	V
Emitter-to-Base Breakdown Voltage			
($I_E = -0.001$ mA, $I_C = 0$)	$V_{(BR)EB0}$	3 min	V
Collector-Cutoff Current ($V_{CE} = 1$ V, $I_E = 0$)	I_{CB0}	0.02 max	μ A
Emitter-Cutoff Current ($V_{EB} = 3$ V, $I_C = 0$)	I_{EB0}	1 max	μ A
Static Forward-Current Transfer Ratio			
($V_{CE} = 6$ V, $I_E = -1$ mA)	h_{FE}	70 to 275	
Feedback Capacitance ($V_{CE} = 8$ V, $I_E = 0$, $f = 1$ MHz)			
	C_{cb}	0.65 max	pF
Extrinsic Transconductance ($V_{CE} = 7.5$ V, $I_E = -2$ mA, $f = 10.7$ MHz)			
	g_m	70	mmhos
Maximum Available Amplifier Gain			
($V_{CE} = 7.5$ V, $I_E = -2$ mA, $f = 10.7$ MHz)	MAG	51.4	dB
Maximum Usable Amplifier Gain:			
Neutralized— $V_{CC} = 12$ V, $f = 10.7$ MHz	MUG	33.2	dB
Unneutralized— $V_{CE} = 7.5$ V, $I_E = -2$ mA, $f = 10.7$ MHz	MUG	28.1	dB
Input Capacitance ($V_{CE} = 7.5$ V, $I_E = -2$ mA, $f = 10.7$ MHz)			
	C_{ie}	8.2	pF
Input Resistance ($V_{CE} = 7.5$ V, $I_E = -2$ mA, $f = 10.7$ MHz)			
	R_{ie}	1500	Ω
Output Resistance ($V_{CE} = 7.5$ V, $I_E = -2$ mA, $f = 10.7$ MHz)			
	R_{oe}	80	k Ω
Output Capacitance ($V_{CE} = 7.5$ V, $I_E = -2$ mA, $f = 10.7$ MHz)			
	C_{oe}	1.5	pF

TYPICAL EXTRINSIC TRANSCONDUCTANCE AT 10.7 MHz

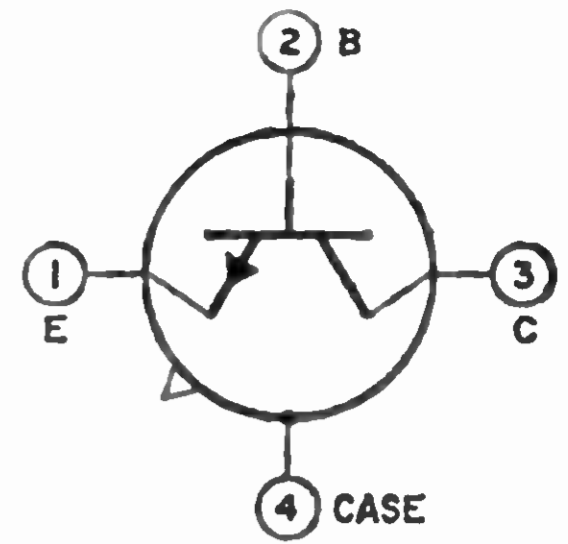


92CS-12929T

40246

TRANSISTOR

Si n-p-n planar type used in if-amplifier applications in conjunction with types 40242 (rf amplifier), 40243 (mixer), 40244 (if oscillator), and 40245 (if amplifier) to make up a "front-end" and if complement for FM and AM/FM receivers. JEDEC TO-104, Outline No.31. This type is identical with type 40245 except for the following items:



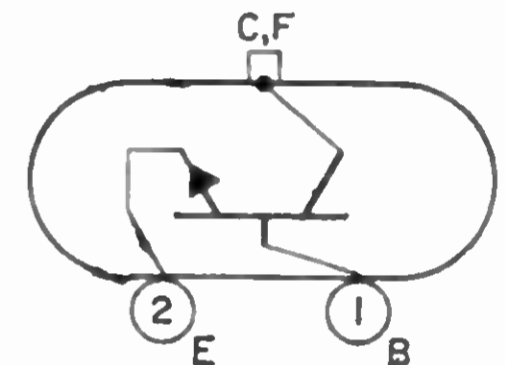
CHARACTERISTICS

Static Forward-Current Transfer Ratio ($V_{CE} = 6\text{ V}$, $I_E = -1\text{ mA}$)	h_{FE}	27 to 90	
Maximum Available Amplifier Gain ($V_{CE} = 7.5\text{ V}$, $I_E = -2\text{ mA}$, $f = 10.7\text{ MHz}$)	MAG	51.2	dB
Input Resistance ($V_{CE} = 7.5\text{ V}$, $I_E = -2\text{ mA}$, $f = 10.7\text{ MHz}$)	R_{ie}	1200	Ω
Output Resistance ($V_{CE} = 7.5\text{ V}$, $I_E = -2\text{ mA}$, $f = 10.7\text{ MHz}$)	R_{oe}	90	k Ω

40250

POWER TRANSISTOR

Si n-p-n diffused-junction type used in audio and inverter circuits in 12-volt mobile radio and portable communications equipment and in a wide variety of intermediate- and high-power applications. JEDEC TO-66, Outline No.25. See Mounting Hardware for desired mounting arrangement.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	50	V
Collector-to-Emitter Voltage: $V_{BE} = -1.5\text{ V}$	V_{CEV}	50	V
Base open	V_{CEO}	40	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	4	A
Base Current	I_B	2	A
Transistor Dissipation: T_c up to 25°C	P_T	29*	W
T_c above 25°C	P_T	See curve page 300	
Temperature Range: Operating (Junction)	$T_J(\text{opr})$	-65 to 200	$^\circ\text{C}$
Storage	T_{STG}	-65 to 200	$^\circ\text{C}$
Pin-Soldering Temperature (10 s max)	T_P	235	$^\circ\text{C}$

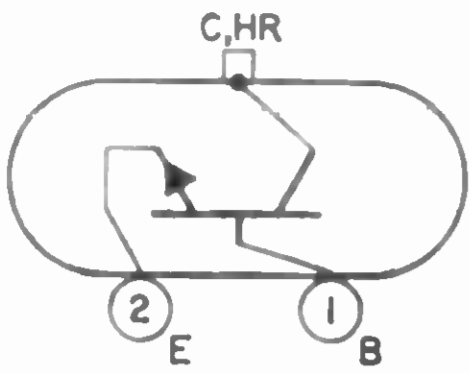
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Base Breakdown Voltage ($I_C = 0.05\text{ A}$, $I_E = 0$)	$V_{(BR)CBO}$	50 min	V
Collector-to-Emitter Breakdown Voltage ($I_C = 0.05\text{ A}$, $V_{BE} = -1.5\text{ V}$)	$V_{(BR)CEV}$	50 min	V
Collector-to-Emitter Sustaining Voltage ($I_C = 0.1\text{ A}$)	$V_{CEO(\text{sus})}$	40 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.005\text{ A}$, $I_C = 0$)	$V_{(BR)EBO}$	5 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 1.5\text{ A}$, $I_B = 0.15\text{ A}$)	$V_{CE(\text{sat})}$	1.5 max	V
Base-to-Emitter Voltage ($V_{CE} = 4\text{ V}$, $I_C = 1.5\text{ A}$)	V_{BE}	2.2 max	V
Collector-Cutoff Current: $V_{CB} = 30\text{ V}$, $I_E = 0$, $T_c = 25^\circ\text{C}$	I_{CBO}	1 max	mA
$V_{CB} = 30\text{ V}$, $I_E = 0$, $T_c = 150^\circ\text{C}$	I_{CBO}	5 max	mA
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$, $I_C = 0$)	I_{EBO}	5 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 4\text{ V}$, $I_C = 1.5\text{ A}$)	h_{FE}	25 to 100	
Thermal Resistance, Junction-to-Case	θ_{J-C}	6* max	$^\circ\text{C/W}$

* This value does not apply to type 40250V1

TRANSISTOR

40250V1



Si n-p-n diffused-junction type used in audio and inverter circuits in 12-volt mobile radio and portable communications equipment and in a wide variety of intermediate- and high-power applications. This type has an attached heat radiator for mounting on printed-circuit-board applications. JEDEC TO-66 (with heat

radiator), Outline No.26. This type is identical with type 40250 except for the following items:

MAXIMUM RATINGS

Transistor Dissipation:

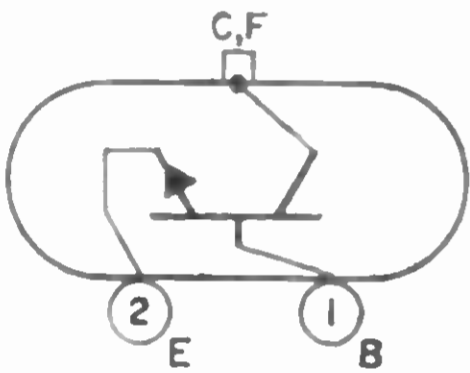
T_A up to 25°C	P_T	5.8	W
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CHARACTERISTICS (At case temperature = 25°C)

Thermal Resistance, Junction-to-Ambient	θ_{J-A}	30 max	°C/W
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TRANSISTOR

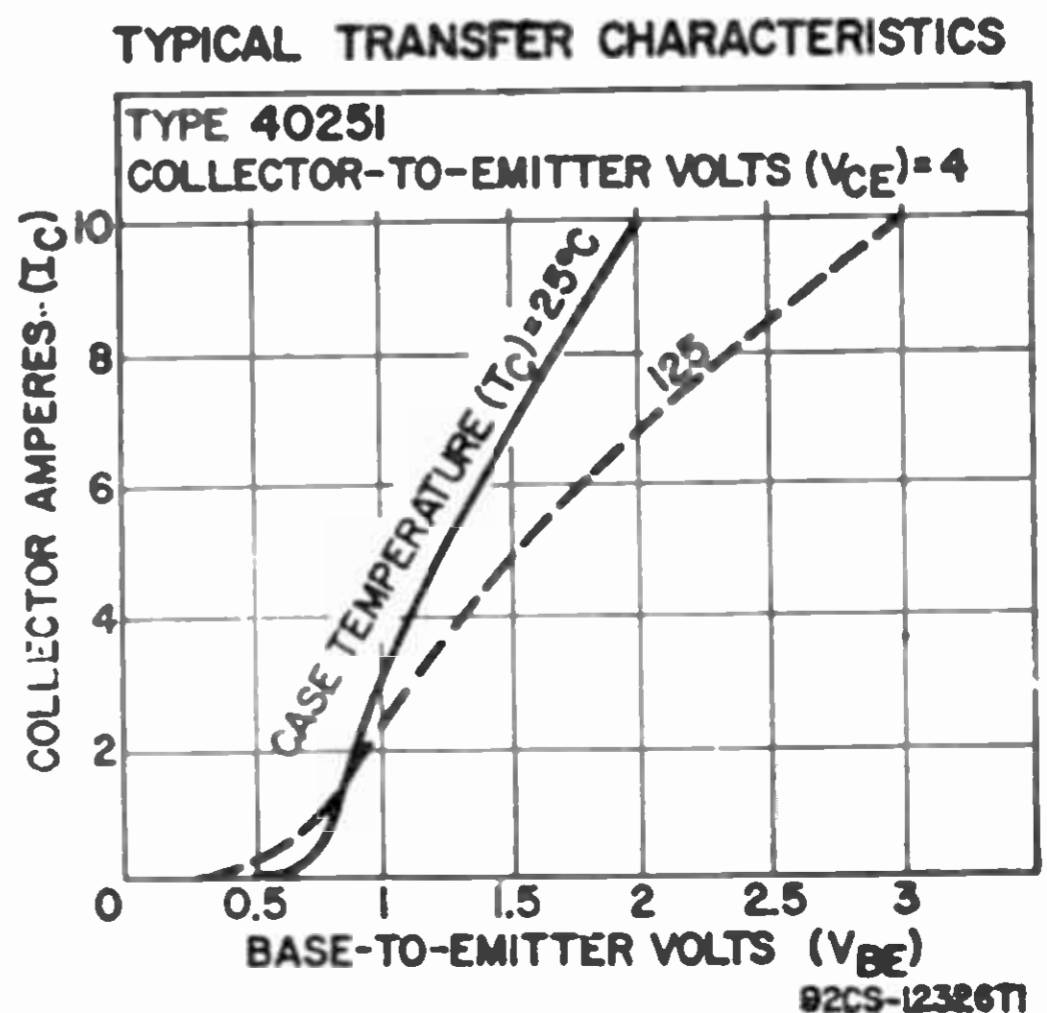
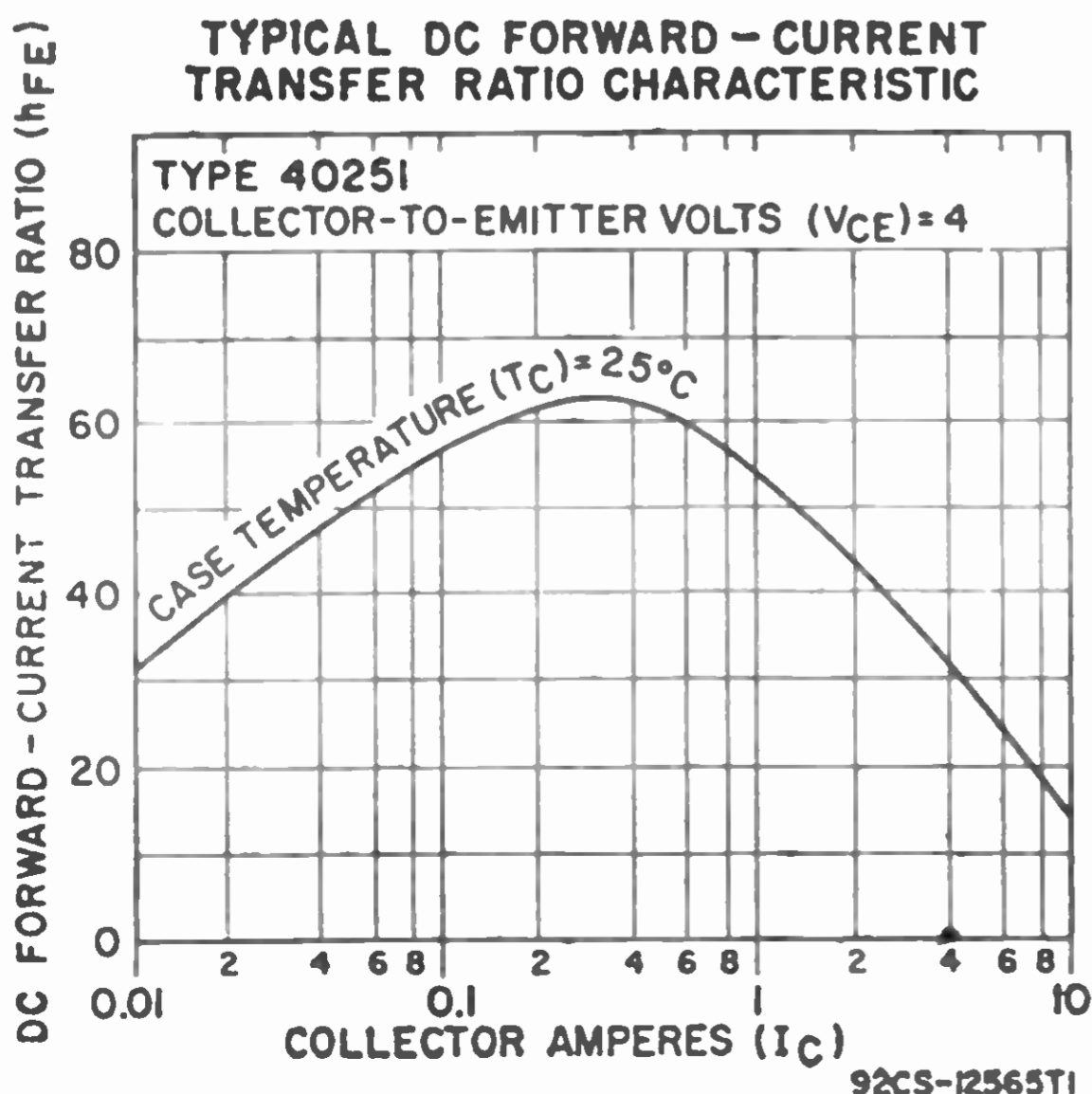
40251



Si n-p-n diffused-junction type used in audio and inverter circuits in 12-volt mobile radio and portable communications equipment and in a wide variety of intermediate- and high-power applications. JEDEC TO-3, Outline No.2. See Mounting Hardware for desired mounting arrangement.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	50	V
Collector-to-Emitter Voltage:			
$V_{BE} = -1.5$ V	V_{CEV}	50	V
Base open	V_{CEO}	40	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	15	A
Base Current	I_B	7	A
Transistor Dissipation:			
T_c up to 25°C	P_T	117	W
T_c above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Pin-Soldering Temperature (10 s max)	T_P	235	°C



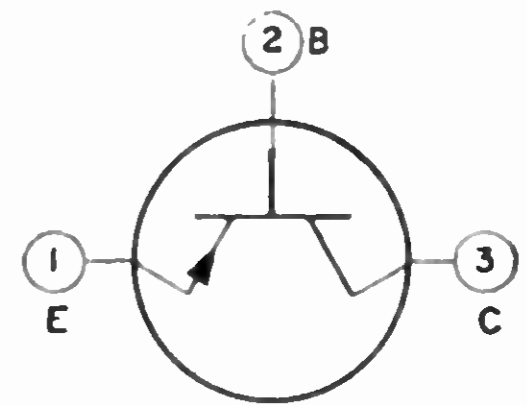
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Base Breakdown Voltage ($I_C = 0.1$ A, $I_E = 0$)	$V_{(BR)CBO}$	50 min	V
Collector-to-Emitter Breakdown Voltage ($I_C = 0.1$ A, $V_{BE} = -1.5$ V)	$V_{(BR)CEV}$	50 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.01$ A, $I_C = 0$)	$V_{(BR)EBO}$	5 min	V
Collector-to-Emitter Sustaining Voltage ($I_C = 0.2$ A)	$V_{CEO(SUS)}$	40 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 8$ A, $I_B = 0.8$ A)	$V_{CE(sat)}$	1.5 max	V
Base-to-Emitter Voltage ($V_{CE} = 4$ V, $I_C = 8$ A)	V_{BE}	2.2 max	V
Collector-Cutoff Current: $V_{CE} = 40$ V, $V_{BE} = -1.5$ V, $T_C = 25^\circ\text{C}$	I_{CEV}	2 max	mA
$V_{CE} = 40$ V, $V_{BE} = -1.5$ V, $T_C = 150^\circ\text{C}$	I_{CEV}	10 max	mA
Emitter-Cutoff Current ($V_{EB} = 5$ V, $I_C = 0$)	I_{EBO}	10 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 4$ V, $I_C = 8$ A)	h_{FE}	15 to 60	
Power Rating Test ($V_{CE} = 39$ V, $I_C = 3$ mA)		1	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Case	θ_{J-C}	1.5 max	$^\circ\text{C/W}$

40253

TRANSISTOR

Ge p-n-p alloy-junction type used in class B audio amplifier applications in consumer product and industrial equipment. JEDEC TO-1, Outline No.1.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-25	V
Collector-to-Emitter Voltage	V_{CEO}	-25	V
Emitter-to-Base Voltage	V_{EBO}	-2.5	V
Collector Current	I_C	-500	mA
Emitter Current	I_E	500	mA
Base Current	I_B	-100	mA
Transistor Dissipation:			
T_A up to 55°C	P_T	125	mW
T_A above 55°C	P_T	See curve page 300	
T_C up to 64°C	P_T	650	mW
T_C above 64°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 90	$^\circ\text{C}$
Storage	T_{STG}	-65 to 90	$^\circ\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	255	$^\circ\text{C}$

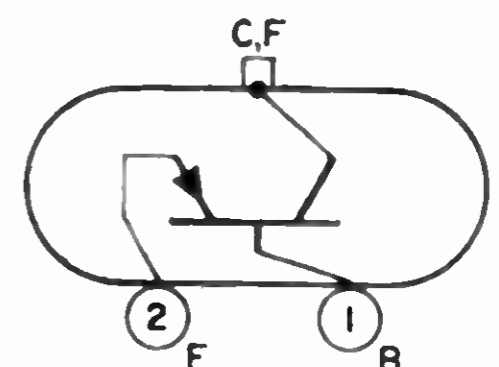
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Base Breakdown Voltage ($I_C = -0.05$ mA, $I_E = 0$)	$V_{(BR)CBO}$	-25 min	V
Collector-to-Emitter Breakdown Voltage ($I_C = -2$ mA, $I_B = 0$)	$V_{(BR)CEO}$	-25 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -0.014$ mA, $I_C = 0$)	$V_{(BR)EBO}$	-2.5 min	V
Collector-to-Emitter Saturation Voltage ($I_C = -400$ mA, $I_B = -20$ mA)	$V_{CE(sat)}$	-0.5	V
Base-to-Emitter Voltage: $V_{CE} = -10$ V, $I_C = -5$ mA	V_{BE}	-0.15	V
$V_{CE} = -1$ V, $I_C = -400$ mA	V_{BE}	-0.45	V
Collector-Cutoff Current ($V_{CB} = -12$ V, $I_E = 0$)	I_{CBO}	-14 max	μA
Emitter-Cutoff Current ($V_{EB} = 2.5$ V, $I_C = 0$)	I_{EBO}	-14 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = -1$ V, $I_C = -400$ mA)	h_{FE}	50 min	$^\circ\text{C/W}$
Gain-Bandwidth Product ($V_{CE} = -6$ V, $I_C = -1$ mA)	f_T	1	MHz
Thermal Resistance, Junction-to-Case ($T_C = 64^\circ\text{C}$)	θ_{J-C}	40 max	

40254

POWER TRANSISTOR

Ge p-n-p alloy type for class A af power-amplifier service in driver- and output-stage applications. JEDEC TO-3, Outline No.2. See Mounting Hardware for desired mounting arrangement. This type is identical with type 40022 except for the following items:



CHARACTERISTICS (At mounting-flange temperature = 25°C)

Collector-Cutoff Current ($V_{CB} = -30$ V, $I_E = 0$)	I_{CBO}	-3 max	mA
Collector-Cutoff Saturation Current ($V_{CB} = -0.5$ V, $I_E = 0$)	$I_{CBO(sat)}$	-0.16 max	mA

TYPICAL OPERATION IN CLASS A AF-AMPLIFIER CIRCUIT

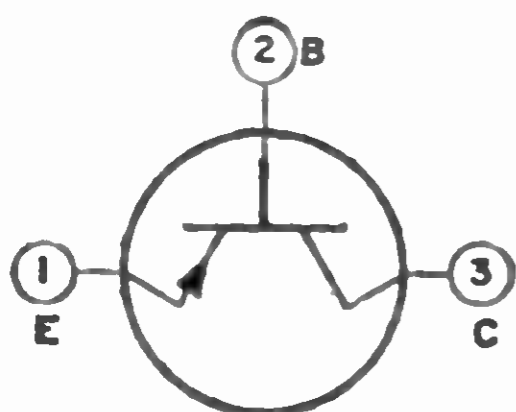
DC Collector-Supply Voltage	V_{CC}	-16	V
DC Collector-to-Emitter Voltage	V_{CE}	-13.2	V
DC Collector Current	I_C	-0.9	A
Peak Collector Current	$i_C(\text{peak})$	-1.8	A
Input Impedance	R_s	15	Ω
Collector Load Impedance	R_L	15	Ω
Maximum Collector Dissipation		12	W
Power Gain	G_{PE}	36	dB
Total Harmonic Distortion ($P_{OEB} = 5$ W)		5	%
Maximum-Signal Power Output	P_{OE}	5	W

Refer to Chart of Discontinued Transistors **40255**

Refer to Chart of Discontinued Transistors **40256**

Refer to Charts of Rectifier Data **40259**

TRANSISTOR 40261



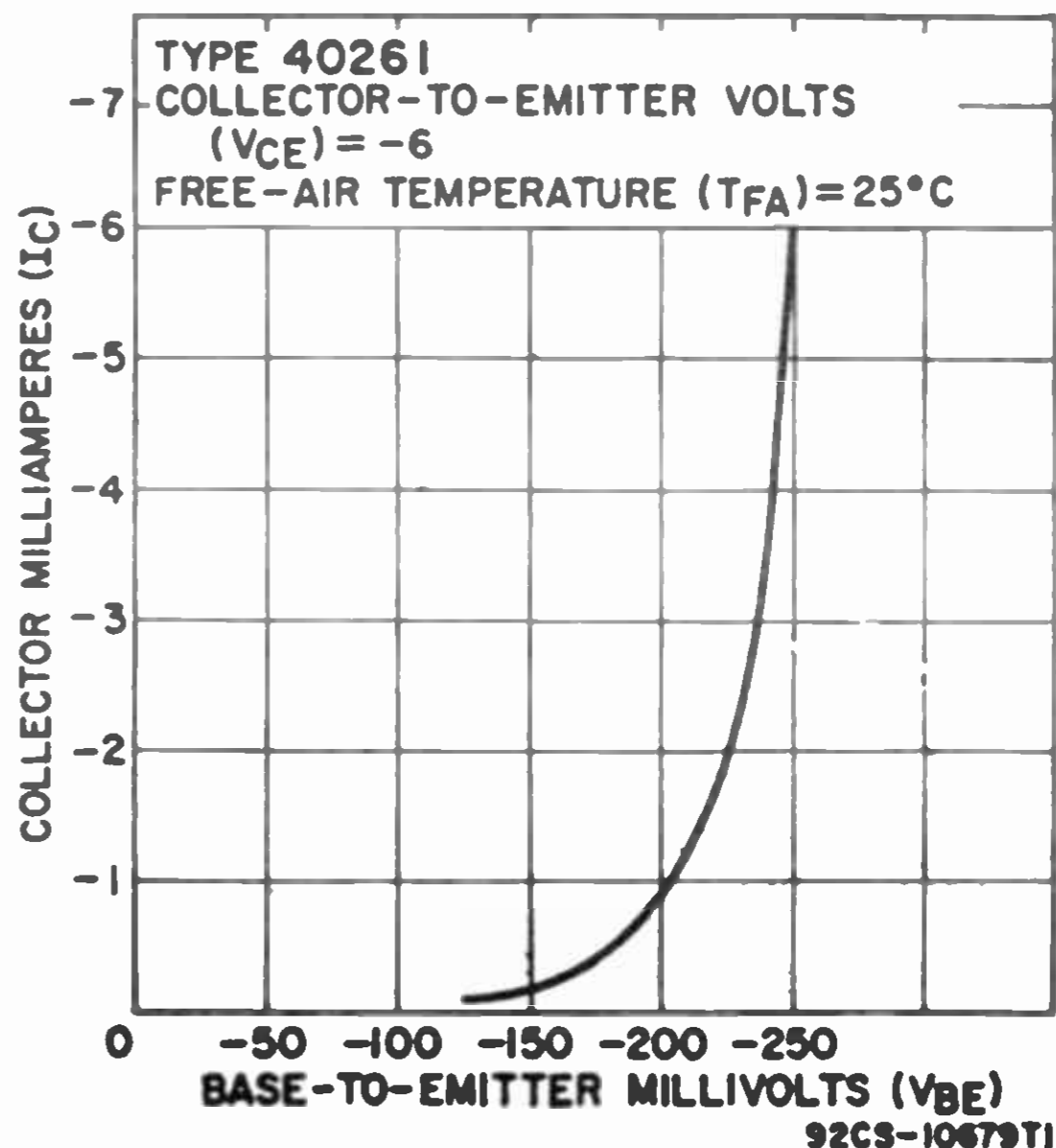
Outline No.1.

Ge p-n-p drift-field type used in converter service in conjunction with types 40262 (if amplifier), 40263 (af amplifier and driver), 40424 (power output), and 40265 (line rectifier) to provide a complement for line-operated AM broadcast-band receivers and phonographs in entertainment equipment. JEDEC TO-1,

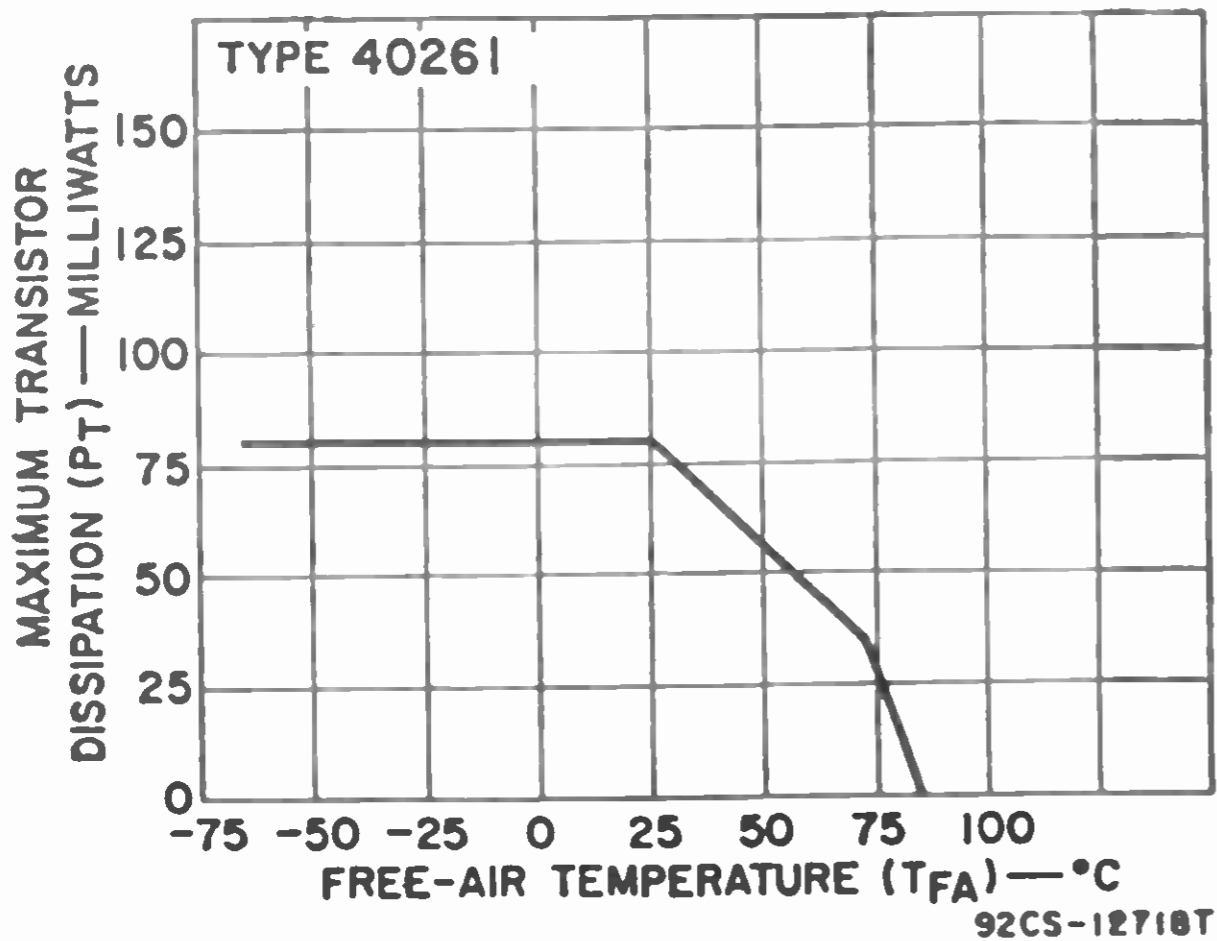
MAXIMUM RATINGS

Collector-to-Base Voltage:			
Emitter open	V_{CBO}	-50	V
$V_{BE} = 0.5$ V, $I_C = -50$ μ A	V_{CBV}	-34	V
Emitter-to-Base Voltage	V_{EBO}	-0.5	V
Collector Current	I_C	-10	mA
Emitter Current	I_E	10	mA
Transistor Dissipation:			
T_A up to 25°C	P_T	80	mW
T_A above 25°C	P_T	See Rating Chart	
Temperature Range:			
Operating (T_A) and Storage (T_{STG})		-65 to 85	°C
Lead-Soldering Temperature (10 s max)	T_L	255	°C

TYPICAL TRANSFER CHARACTERISTIC



RATING CHART



CHARACTERISTICS

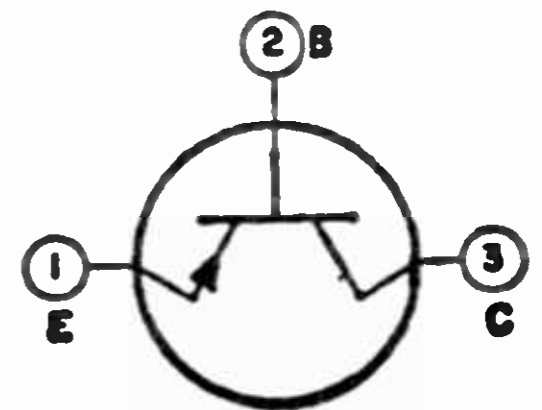
Collector-to-Base Breakdown Voltage:

$I_C = -0.05 \text{ mA}, I_E = 0$	$V_{(BR)CBO}$	-50	V
$V_{BE} = 0.5 \text{ V}, I_C = -0.05 \text{ mA}$	$V_{(BR)CBV}$	-34	V
Emitter-to-Base Breakdown Voltage			
$(I_E = -0.012 \text{ mA}, I_C = 0)$	$V_{(BR)EBO}$	-1.5 min	V
Collector-Cutoff Current ($V_{CB} = -12 \text{ V}, I_E = 0$)	I_{CBO}	-12 max	μA
Emitter-Cutoff Current ($V_{EB} = 0.5 \text{ V}, I_C = 0$)	I_{EBO}	-12 max	μA
Intrinsic Base-Spreading Resistance			
$(V_{CE} = -12 \text{ V}, I_C = -1 \text{ mA}, f = 100 \text{ MHz})$	$r_{bb'}$	25	Ω
Small-Signal Forward-Current Transfer Ratio			
$(V_{CE} = -6 \text{ V}, I_C = -1 \text{ mA}, f = 1 \text{ kHz})$	h_{fe}	27 to 170	
Gain-Bandwidth Product ($V_{CE} = -12 \text{ V}, I_C = -1 \text{ mA}$)	f_T	40	MHz
Collector-to-Base Feedback Capacitance			
$(V_{CB} = -12 \text{ V}, I_E = 0)$	C_{cb}	3.7 max	pF

40262

TRANSISTOR

Ge p-n-p drift-field type used in if-amplifier service in conjunction with types 40261 (converter), 40263 (af amplifier and driver), 40424 (power output), and 40265 (line rectifier) to provide a complement for line-operated AM broadcast-band receivers and phonographs in entertainment equipment. JEDEC TO-1, Outline No.1. This type is identical with type 40261 except for the following items:



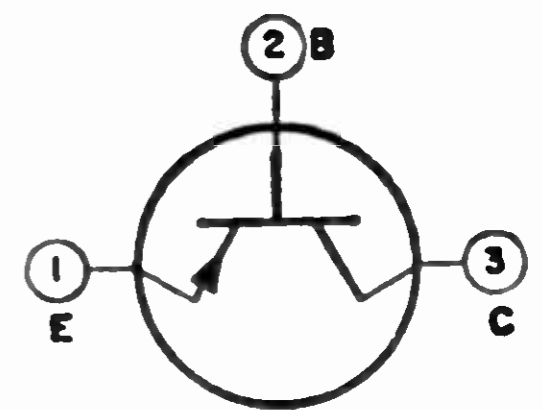
CHARACTERISTICS

Emitter-to-Base Breakdown Voltage			
$(I_E = -0.012 \text{ mA}, I_C = 0)$	$V_{(BR)EBO}$	-0.5 min	V
Small-Signal Forward-Current Transfer Ratio			
$(V_{CE} = -6 \text{ V}, I_C = -1 \text{ mA}, f = 1 \text{ kHz})$	h_{fe}	82 to 350	
Gain-Bandwidth Product ($V_{CE} = -12 \text{ V}, I_C = -1 \text{ mA}$)	f_T	30	MHz
Collector-to-Base Capacitance ($V_{CB} = -12 \text{ V}, I_E = 0$)			
	C_{cb}	3.4 max	pF

40263

TRANSISTOR

Ge p-n-p alloy-junction type used in low-level af-amplifier and driver service in conjunction with types 40261 (converter), 40262 (if amplifier), 40424 (power output), and 40265 (line rectifier) to provide a complement for line-operated AM broadcast-band receivers and phonographs in entertainment equipment. JEDEC TO-1, Outline No.1.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-20	V
Collector-to-Emitter Voltage ($R_{BE} = 10 \text{ k}\Omega$)	V_{CER}	-18	V
Emitter-to-Base Voltage	V_{EBO}	-2.5	V
Collector Current	I_C	-50	mA
Emitter Current	I_E	50	mA
Transistor Dissipation:			
T_A up to 55°C	P_T	120	mW
T_A above 55°C	P_T	See curve page 300	
Temperature Range:			
Operating ($T_A - T_C$) and Storage (T_{STG})		-65 to 100	$^\circ\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	255	$^\circ\text{C}$

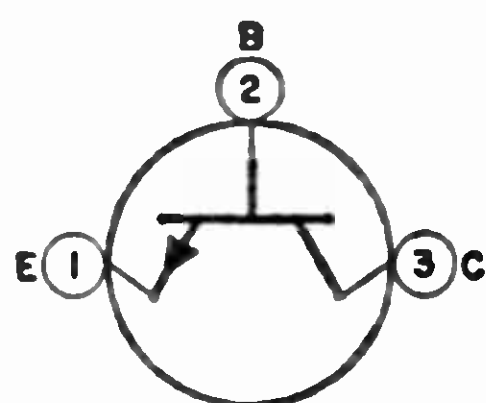
CHARACTERISTICS

Collector-to-Emitter Breakdown Voltage			
$(I_C = -5 \text{ mA}, R_{BE} = 10 \text{ k}\Omega)$	$V_{(BR)CER}$	18 min	V
Emitter-to-Base Breakdown Voltage			
$(I_E = -0.05 \text{ mA}, I_C = 0)$	$V_{(BR)EBO}$	-2.5 min	V
Collector-Cutoff Current ($V_{CB} = -20 \text{ V}, I_E = 0$)	I_{CBO}	-12 max	μA
Emitter-Cutoff Current ($V_{EB} = 2.5 \text{ V}, I_C = 0$)	I_{EBO}	-12 max	μA
Small-Signal Forward-Current Transfer-Ratio Cutoff			
Frequency ($V_{CE} = -6 \text{ V}, I_C = -1 \text{ mA}$)	f_{hfb}	10	MHz
Small-Signal Forward-Current Transfer Ratio			
$(V_{CE} = -6 \text{ V}, I_C = -1 \text{ mA}, f = 1 \text{ kHz})$	h_{fe}	100 to 325	
Intrinsic Base-Spreading Resistance ($V_{CE} = -6 \text{ V}, I_C = -1 \text{ mA}, f = 100 \text{ MHz}$)			
	$r_{bb'}$	200	Ω

Refer to Chart of Discontinued Transistors	40264
Refer to Charts of Rectifier Data	40265
Refer to Charts of Rectifier Data	40266
Refer to Charts of Rectifier Data	40267
Refer to Chart of Discontinued Transistors	40269

TRANSISTOR

40279



Si n-p-n "overlay" epitaxial planar type used in ultra-high-reliability vhf-uhf applications in space, military, and industrial communications equipment. Used in class A, B, and C amplifiers, frequency multipliers, or oscillators. This device is subjected to special preconditioning tests for selection in high-reliability, large-signal, and

high-power applications. JEDEC TO-60, Outline No.23. See Mounting Hardware for desired mounting arrangement.

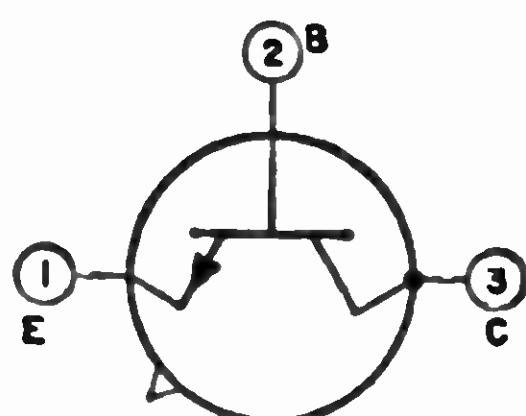
MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	65	V
Collector-to-Emitter Voltage:			
$V_{BE} = -1.5$ V	V_{CEV}	65	V
Base open	V_{CEO}	40	V
Emitter-to-Base Voltage	V_{EBO}	4	V
Collector Current	I_C	1.5	A
Transistor Dissipation:			
T_C up to 25°C	P_T	11.6	W
T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	230	°C

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Base Breakdown Voltage ($I_C = 0.1$ mA, $I_E = 0$)	$V_{(BR)CBO}$	65 min	V
Collector-to-Emitter Breakdown Voltage:			
$I_C = 0$ to 200 mA, $I_B = 0$, pulsed through inductor $L = 25$ mH, $df = 50\%$	$V_{(BR)CEO}$	40 min	V
$V_{BE} = -1.5$ V, $I_C = 0$ to 200 mA, pulsed through inductor $L = 25$ mH, $df = 50\%$	$V_{(BR)CEV}$	65 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.1$ mA, $I_C = 0$)	$V_{(BR)EBO}$	4 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 0.5$ A, $I_B = 0.1$ A)	$V_{CE(\text{sat})}$	1 max	V
Collector-Cutoff Current ($V_{CE} = 30$ V, $I_B = 0$)	I_{CEO}	0.1 max	μ A
Static Forward-Current Transfer Ratio ($V_{CE} = 5$ V, $I_C = 150$ mA)	h_{FE}	10 min	
Output Capacitance ($V_{CB} = 30$ V, $I_E = 0$)	C_{obo}	10 max	pF
RF Power Output, Unneutralized Amplifier:			
$V_{CE} = 28$ V, $P_{IE} = 1$ W, R_G and $R_L = 50$ Ω , $f = 100$ MHz	P_{OE}	7.5* min	W
$V_{CE} = 28$ V, $P_{IE} = 1$ W, R_G and $R_L = 50$ Ω , $f = 400$ MHz	P_{OE}	3† min	W

* For conditions given, minimum efficiency = 65 per cent
 † For conditions given, minimum efficiency = 40 per cent.



TRANSISTOR

40280

Si n-p-n "overlay" epitaxial planar type used in vhf class C amplifier service requiring low supply voltages and high power output in industrial and military communications equipment. JEDEC TO-39, Outline No.15.

MAXIMUM RATINGS

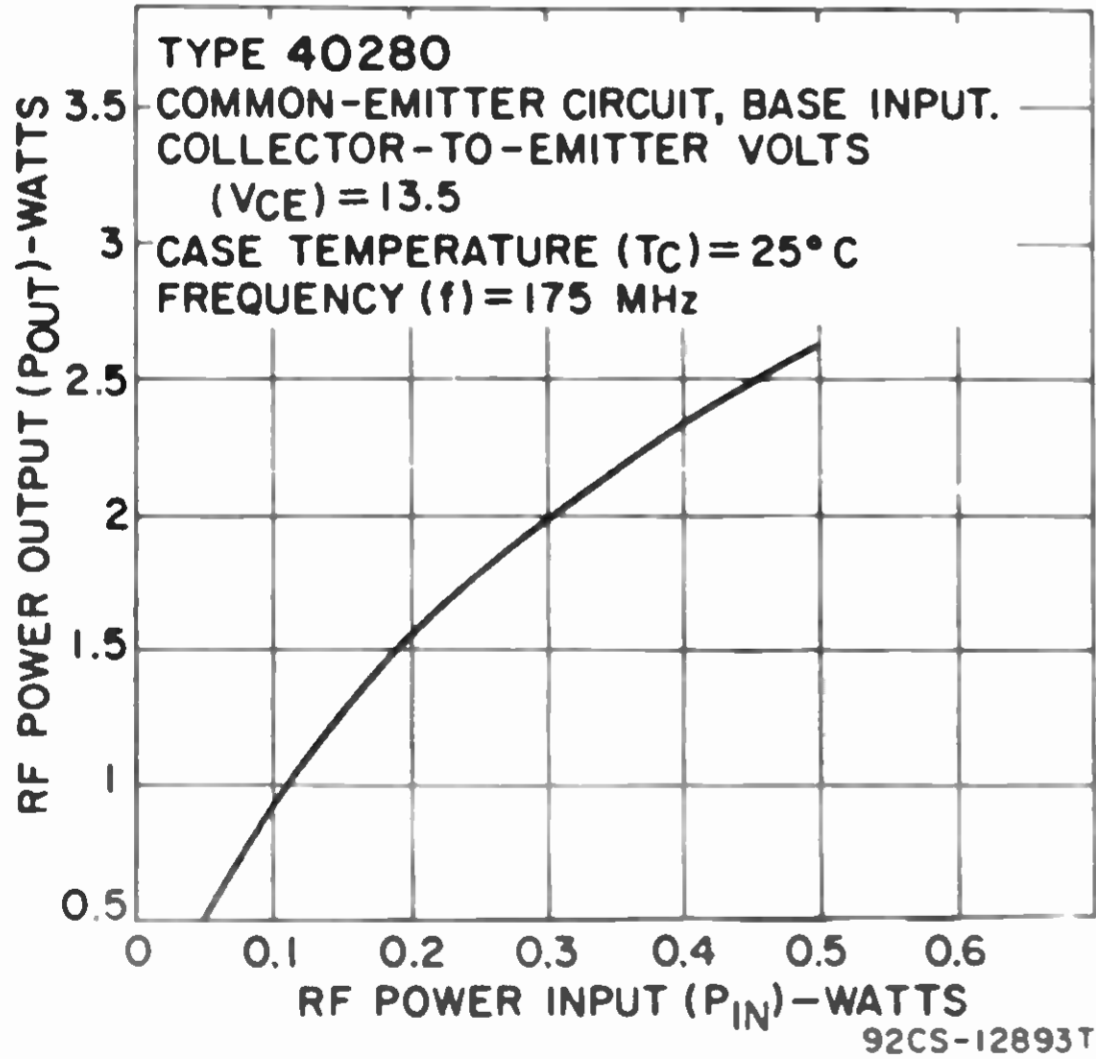
Collector-to-Base Voltage	V_{CBO}	36	V
Collector-to-Emitter Voltage:			
$V_{BE} = -1.5$ V	V_{CEV}	36	V
Base open	V_{CEO}	18	V
Emitter-to-Base Voltage	V_{EBO}	4	V
Collector Current	I_C	0.5	A
Transistor Dissipation:			
T_c up to 25°C	P_T	7	W
T_c above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	230*	°C

CHARACTERISTICS (At case temperature = 25°C)

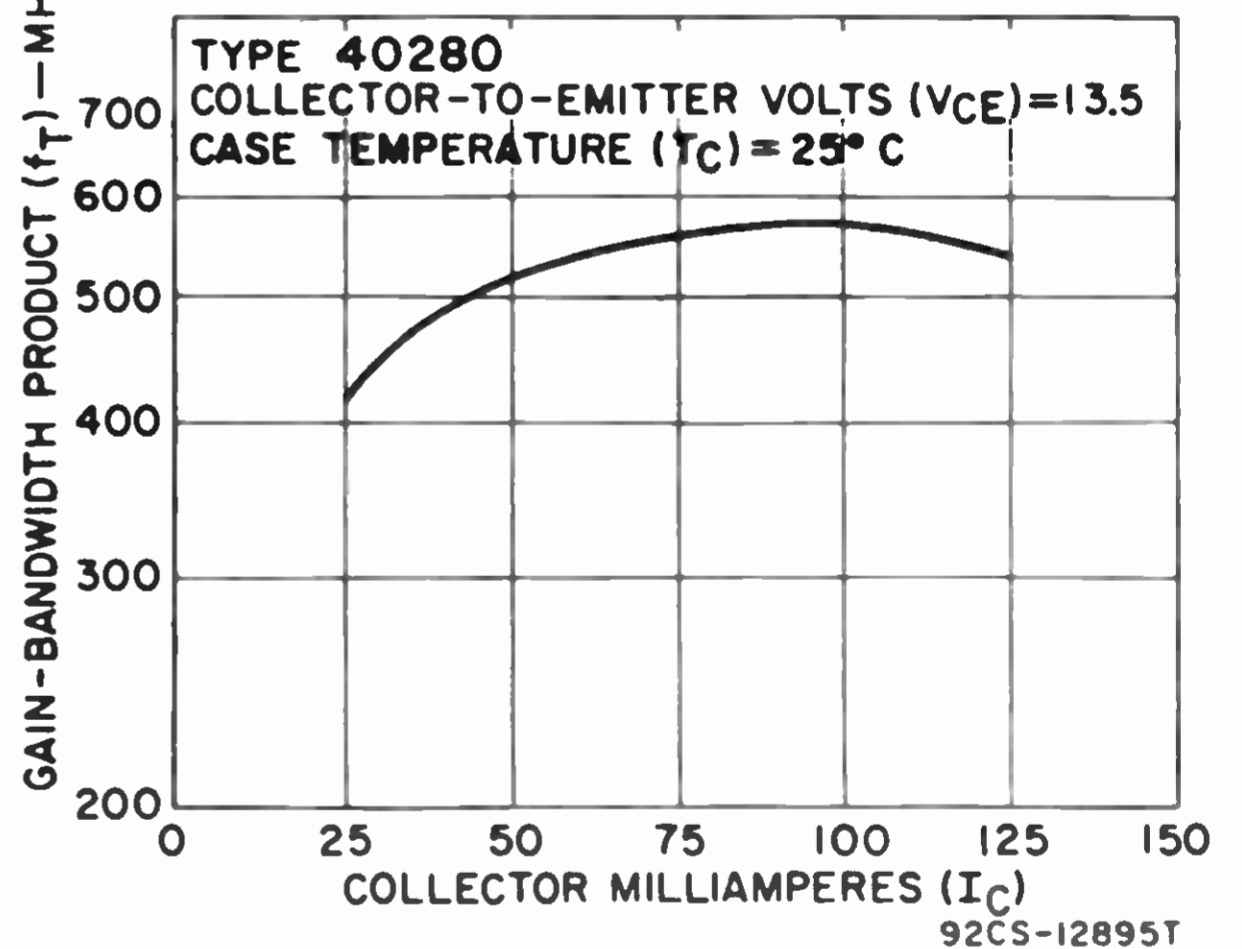
Collector-to-Base Breakdown Voltage ($I_C = 0.25$ mA, $I_E = 0$)	$V_{(BR)CBO}$	36 min	V
Collector-to-Emitter Breakdown Voltage ($I_C = 200$ mA, $I_B = 0$, pulsed through inductor $L = 25$ mH, $df = 50\%$)	$V_{(BR)CEV}$	36 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.1$ mA, $I_C = 0$)	$V_{(BR)EBO}$	4 min	V
Collector-to-Emitter Sustaining Voltage ($I_C = 200$ mA, $I_B = 0$, pulsed through inductor $L = 25$ mH, $df = 50\%$)	V_{CEO} (sus)	18 min	V
Collector-Cutoff Current ($V_{CE} = 15$ V, $I_B = 0$)	I_{CEO}	100 max	μ A
Gain-Bandwidth Product ($V_{CE} = 13.5$ V, $I_C = 100$ mA)	f_T	550	MHz
Output Capacitance ($V_{CB} = 13.5$ V, $I_E = 0$, $f = 1$ MHz)	C_{obo}	15 max	pF
Input Resistance, Real Part ($V_{CE} = 13.5$ V, $I_C = 100$ mA, $f = 175$ MHz)	$R_e(h_{ie})$	10	Ω
Power Output, Class C Amplifier, Unneutralized ($V_{CE} = 13.5$ V, $P_{IE} = 0.125$ W, $f = 175$ MHz, R_G and $R_L = 50 \Omega$)	P_{OE}	1† min	W
Thermal Resistance, Junction-to-Case	θ_{J-C}	25 max	°C/W

* For types 40281 and 40282 this value is maximum Pin-Soldering Temperature.
 † For conditions given, minimum efficiency = 60 per cent.

TYPICAL RF POWER-OUTPUT CHARACTERISTIC



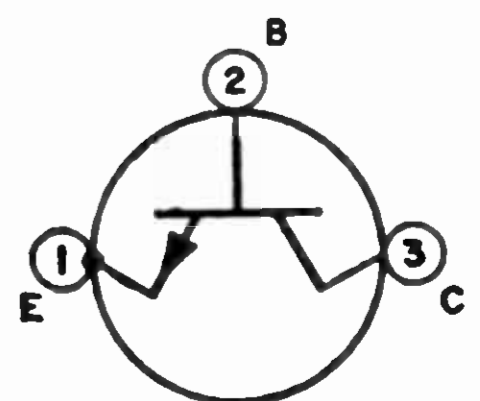
TYPICAL GAIN-BANDWIDTH PRODUCT



40281

TRANSISTOR

Si n-p-n "overlay" epitaxial planar type used in vhf class C amplifier service requiring low supply voltages and high power output in industrial and military communications equipment. JEDEC TO-60, Outline No.23. See **Mounting Hardware** for desired mounting arrangement. This type is identical with type 40280 except for the following items:



MAXIMUM RATINGS

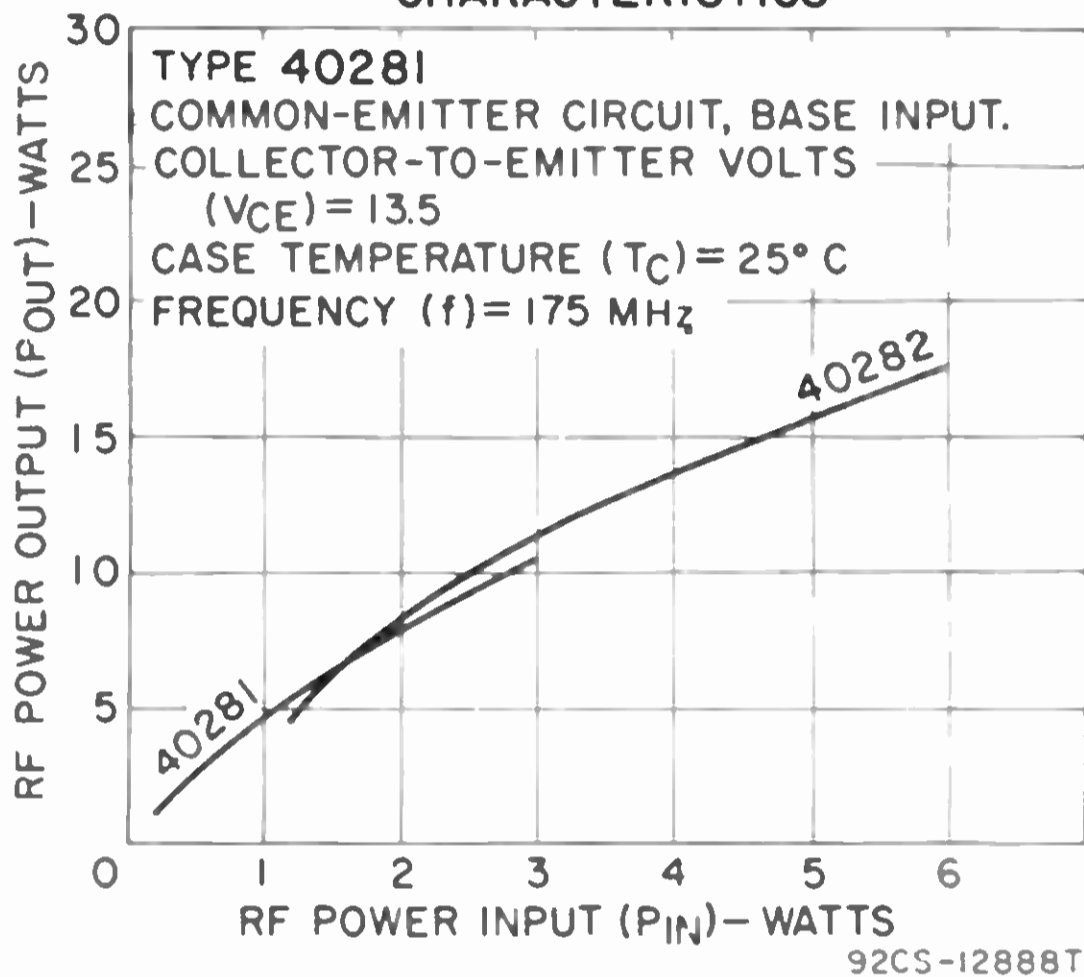
Collector Current	I_C	1	A
Transistor Dissipation: Tc up to 25°C	P_T	11.6	W

CHARACTERISTICS (At case temperature = 25°C)

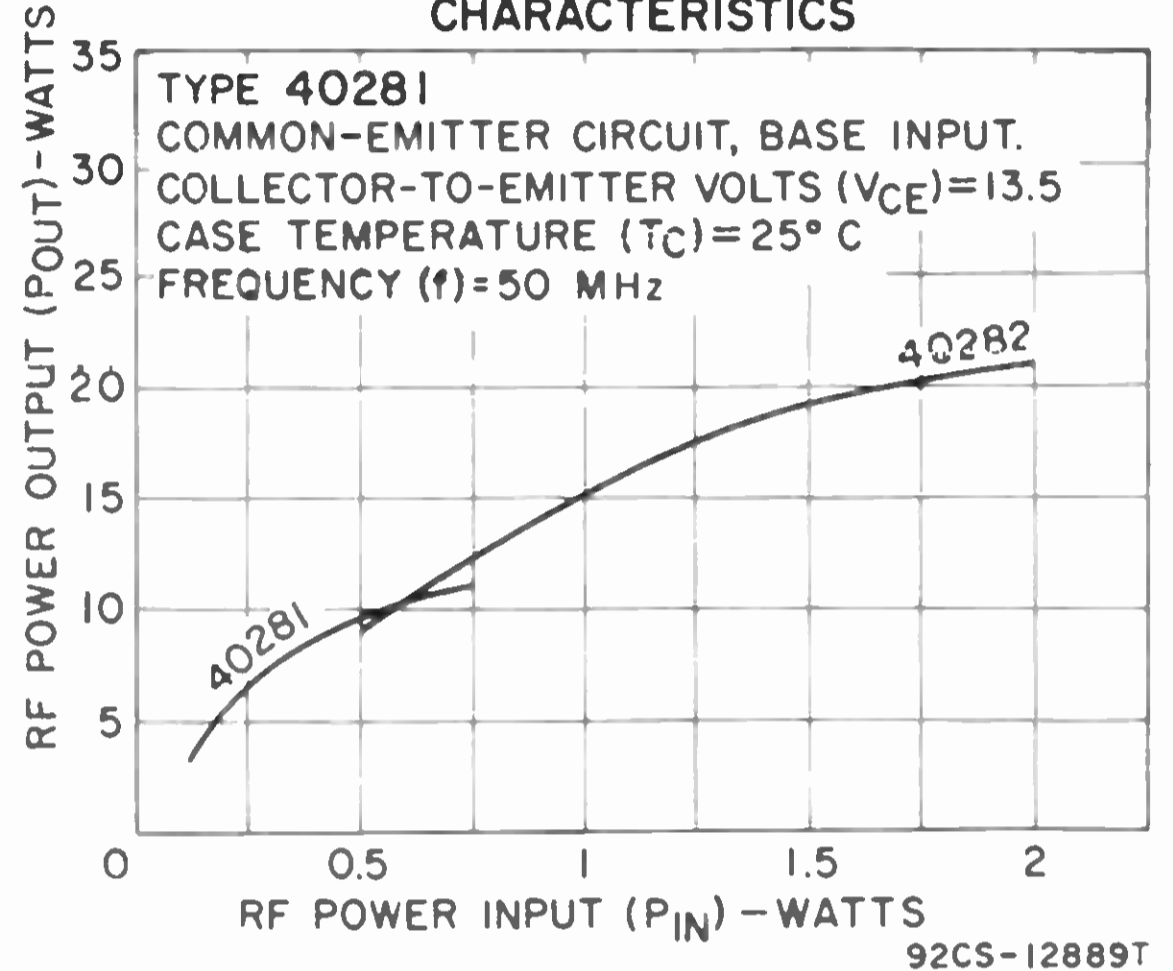
Gain-Bandwidth Product ($V_{CE} = 13.5$ V, $I_C = 400$ mA)	f_T	400	MHz
Output Capacitance ($V_{CB} = 13.5$ V, $I_E = 0$, f = 1 MHz)	C_{obo}	22 max	pF
Collector-to-Case Capacitance	C_c	5 max	pF
Input Resistance, Real Part ($V_{CE} = 13.5$ V, $I_C = 400$ mA, f = 175 MHz)	$R_e(h_{ie})$	7	Ω
Power Output, Class C Amplifier, Unneutralized ($V_{CE} = 13.5$ V, $P_{IE} = 1$ W, f = 175 MHz, R_G and $R_L = 50$ Ω)	P_{OE}	4† min	W
Thermal Resistance, Junction-to-Case	θ_{J-C}	15 max	°C/W

† For conditions given, minimum efficiency = 70 per cent.

TYPICAL RF POWER-OUTPUT CHARACTERISTICS

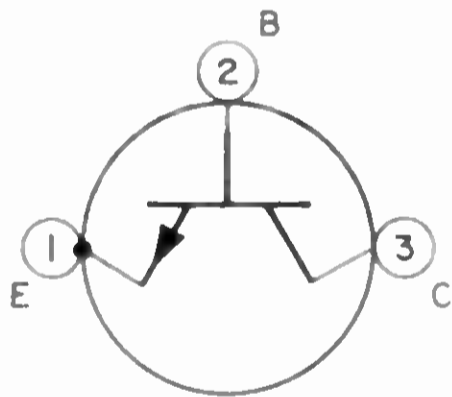


TYPICAL RF POWER-OUTPUT CHARACTERISTICS



TRANSISTOR

40282



Si n-p-n "overlay" epitaxial planar type used in vhf class C amplifier service requiring low supply voltages and high power output in industrial and military communications equipment. JEDEC TO-60, Outline No.23. See **Mounting Hardware** for desired mounting arrangement. This type is identical with type 40280 except for

the following items:

MAXIMUM RATINGS

Collector Current	I_C	2	A
Transistor Dissipation: Tc up to 25°C	P_T	23.2	W

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Base Breakdown Voltage ($I_C = 0.5$ mA, $I_E = 0$)	$V_{(BR)CBO}$	36 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.25$ mA, $I_C = 0$)	$V_{(BR)EBO}$	4 min	V
Collector-Cutoff Current ($V_{CE} = 15$ V, $I_B = 0$)	I_{CEO}	250 max	μA
Gain-Bandwidth Product ($V_{CE} = 13.5$ V, $I_C = 800$ mA)	f_T	350	MHz
Output Capacitance ($V_{CB} = 13.5$ V, $I_E = 0$, f = 1 MHz)	C_{obo}	45 max	pF
Collector-to-Case Capacitance	C_c	5 max	pF
Input Resistance, Real Part ($V_{CE} = 13.5$ V, $I_C = 800$ mA, f = 175 MHz)	$R_e(h_{ie})$	5	Ω
Power Output, Class C Amplifier, Unneutralized ($V_{CE} = 13.5$ V, $P_{IE} = 4$ W, f = 175 MHz, R_G and $R_L = 50$ Ω)	P_{OE}	12† min	W
Thermal Resistance, Junction-to-Case	θ_{J-C}	7.5 max	°C/W

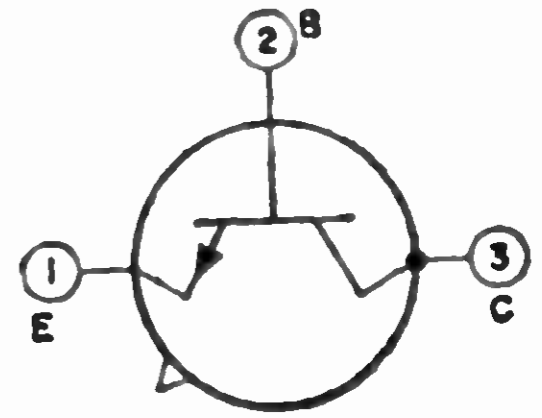
† For conditions given, minimum efficiency = 80 per cent.

40283

Refer to Chart of Discontinued Transistors

40290**TRANSISTOR**

Si n-p-n "overlay" epitaxial planar type used in vhf class C amplifier service requiring low supply voltages and high power output in aircraft, military, and industrial communications equipment. JEDEC TO-39, Outline No.15.

**MAXIMUM RATINGS**

Collector-to-Emitter Voltage:

$V_{BE} = -1.5$ V	V_{CEV}	50	V
$f = 100$ MHz	$V_{CES(RF)}$	90	V
Emitter-to-Base Voltage	V_{EBO}	4	V
Collector Current	I_C	0.5	A
Transistor Dissipation:			
T_c up to 25°C	P_T	7	W
T_c above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 200	$^\circ\text{C}$
Storage	T_{STG}	-65 to 200	$^\circ\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	230*	$^\circ\text{C}$

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Breakdown Voltage:

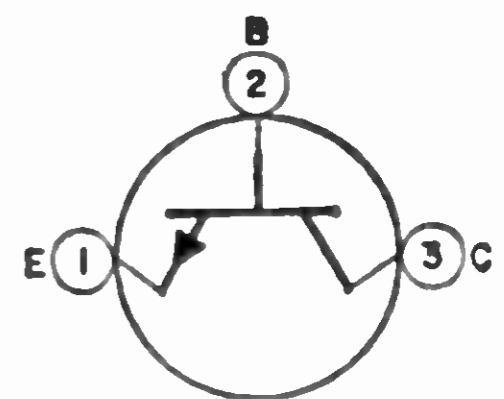
$I_C = 200$ mA, $V_{BE} = -1.5$ V, $R_{BE} = 39$ Ω , pulsed through inductor $L = 25$ mH, $df = 50\%$	$V_{(BR)CEV}$	50 min	V
$I_C = 50$ mA, $V_{BE} = -2$ V, $f \leq 100$ MHz	$V_{(BR)CES(RF)}$	90 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.1$ mA, $I_C = 0$)	$V_{(BR)EBO}$	4 min	V
Collector-Cutoff Current ($V_{CE} = 15$ V, $I_B = 0$)	I_{CEO}	100 max	μA
Gain-Bandwidth Product ($V_{CE} = 12.5$ V, $I_C = 100$ mA)	f_T	500	MHz
Output Capacitance ($V_{CB} = 12.5$ V, $I_E = 0$, $f = 1$ MHz)	C_{obo}	17 max	pF
Input Resistance, Real Part ($V_{CE} = 12.5$ V, $I_C = 100$ mA, $f = 135$ MHz)	$R_e(h_{ie})$	12	Ω
Power Output, Class C Amplifier, Unneutralized ($V_{CE} = 12.5$ V, $P_{IE} = 0.5$ W, $f = 135$ MHz, R_G and $R_L = 50$ Ω)	P_{OE}	2† min	W
Thermal Resistance, Junction-to-Case	θ_{J-C}	25 max	$^\circ\text{C/W}$

* For type 40291 this value is maximum Pin-Soldering Temperature.

† For conditions given, minimum efficiency = 70 per cent.

40291**TRANSISTOR**

Si n-p-n "overlay" epitaxial planar type used in vhf class C amplifier service requiring low supply voltages and high power output in aircraft, military, and industrial communications equipment. JEDEC TO-60, Outline No.23. See Mounting Hardware for desired mounting arrangement. This type is identical with type 40290 except for the following items:

**MAXIMUM RATINGS**

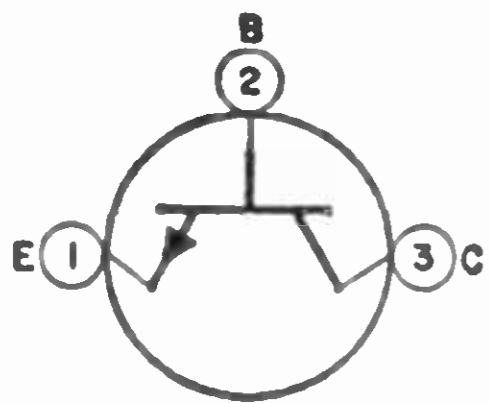
Transistor Dissipation (T_c up to 25°C)	P_T	11.6	W
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CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Case Capacitance	C_c	6 max	pF
Thermal Resistance, Junction-to-Case	θ_{J-C}	15 max	$^\circ\text{C/W}$

TRANSISTOR

40292



Si n-p-n "overlay" epitaxial planar type used in vhf class C amplifier service requiring low supply voltages and high power output in aircraft, military, and industrial communications equipment. JEDEC TO-60, Outline No.23. See Mounting Hardware for desired mounting arrangement.

MAXIMUM RATINGS

Collector-to-Emitter Voltage:

$V_{BE} = -1.5$ V
 $f = 100$ MHz
 Emitter-to-Base Voltage
 Collector Current

Transistor Dissipation:

T_c up to 25°C
 T_c above 25°C

Temperature Range:

Operating (Junction)
 Storage
 Pin-Soldering Temperature (10 s max)

V_{CEV}	50	V
$V_{CES(RF)}$	90	V
V_{EBO}	4	V
I_C	1.25	A
P_T	23.2	W
P_T	See curve page 300	
$T_J(\text{opr})$	-65 to 200	$^\circ\text{C}$
T_{STG}	-65 to 200	$^\circ\text{C}$
T_P	230	$^\circ\text{C}$

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Voltage:

$I_C = 200$ mA, $V_{BE} = -1.5$ V, $R_{BE} = 39 \Omega$,
 pulsed through inductor $L = 25$ mH,
 $df = 50\%$

$I_C = 50$ mA, $V_{BE} = 0$, $f \leq 100$ MHz

Emitter-to-Base Breakdown Voltage
 ($I_E = 0.25$ mA, $I_C = 0$)

Collector-Cutoff Current ($V_{CE} = 15$ V, $I_B = 0$)

Gain-Bandwidth Product ($V_{CE} = 12.5$ V, $I_C = 400$ mA)

Collector-to-Case Capacitance

Output Capacitance ($V_{CB} = 12.5$ V, $I_E = 0$,
 $f = 1$ MHz)

Input Resistance, Real Part ($V_{CE} = 12.5$ V,
 $I_C = 400$ mA, $f = 135$ MHz)

Power Output, Class C Amplifier, Unneutralized
 ($V_{CE} = 12.5$ V, $P_{IE} = 2$ W, $f = 135$ MHz,
 R_G and $R_L = 50 \Omega$)

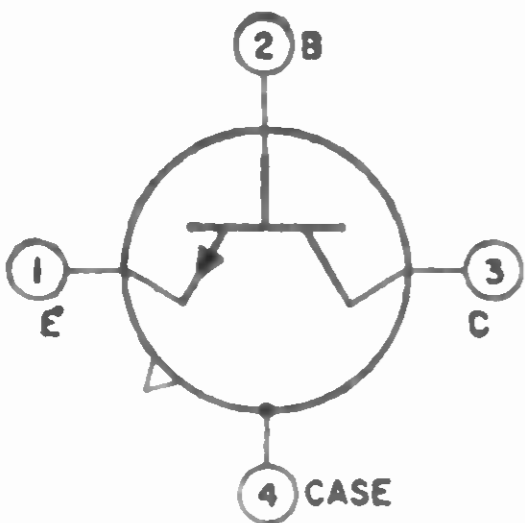
Thermal Resistance, Junction-to-Case

$V_{(BR)CEV}$	50 min	V
$V_{(BR)CES(RF)}$	90 min	V
$V_{(BR)EBO}$	4 min	V
I_{CEO}	250 max	μA
f_T	300	MHz
C_c	6 max	pF
C_{obo}	30 max	pF
$R_e(h_{ie})$	6.5	Ω
P_{oB}	6† min	W
θ_{J-C}	7.5 max	$^\circ\text{C/W}$

† For conditions given, minimum efficiency = 70 per cent.

TRANSISTOR

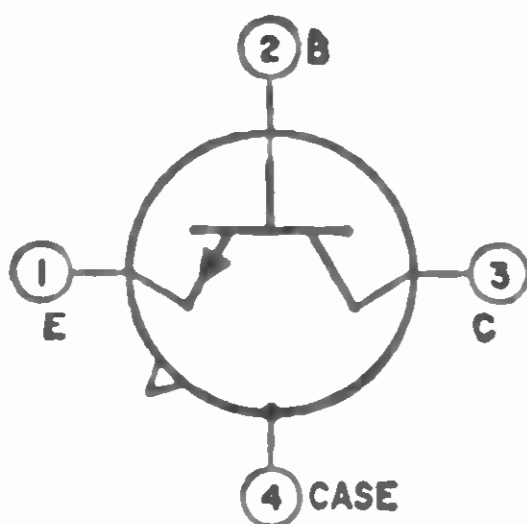
40294



Si n-p-n double-diffused epitaxial planar type used in uhf amplifier, mixer, and oscillator applications. This type is electrically and mechanically identical with type 2N2857, but is specially controlled, processed, and tested for critical aerospace and military applications. JEDEC TO-72, Outline No.28.

TRANSISTOR

40295



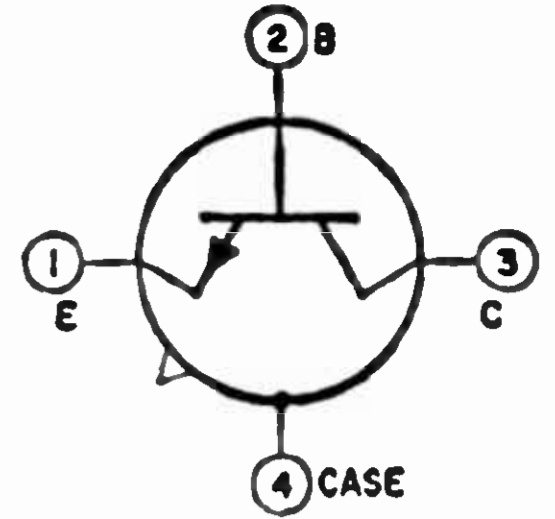
Si n-p-n double-diffused epitaxial planar type used in uhf amplifier, mixer, and oscillator applications. This type is specially controlled, processed, and tested for critical aerospace and military applications. JEDEC TO-72, Outline No.28. This type is identical to type 2N2708 except for the following item:

MAXIMUM RATINGS

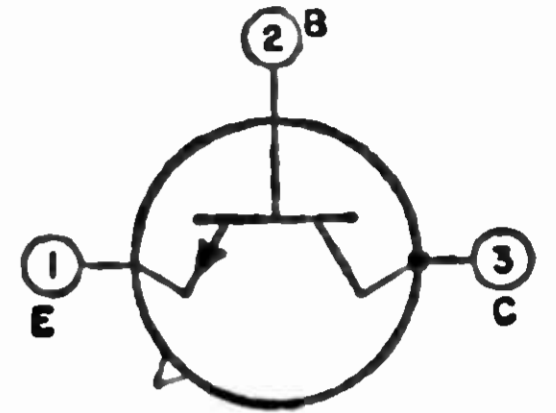
Collector Current	I_C	40	mA
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40296**TRANSISTOR**

Si n-p-n double-diffused epitaxial planar type used in uhf amplifier, mixer, and oscillator applications. This type is electrically and mechanically identical with type 2N2857, but is specially controlled, processed, and tested for critical aerospace and military applications. JEDEC TO-72, Outline No.28.

**40305****TRANSISTOR**

Si n-p-n "overlay" epitaxial planar type subjected to special preconditioning tests for high-reliability, large-signal, high-power vhf-uhf applications in class A, B, and C amplifier, frequency-multiplier, and oscillator circuits in aerospace, industrial and military equipment. JEDEC TO-39, Outline No.15.

**MAXIMUM RATINGS**

Collector-to-Base Voltage	V_{CBO}	65	V
Collector-to-Emitter Voltage:			
$V_{BE} = -1.5$ V	V_{CEV}	65	V
Base open	V_{CEO}	40	V
Emitter-to-Base Voltage	V_{EBO}	4	V
Collector Current	I_C	1	A
Transistor Dissipation:			
T_c up to 25°C	P_T	7	W
T_c above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	230*	°C

CHARACTERISTICS (At case temperature = 25°C)

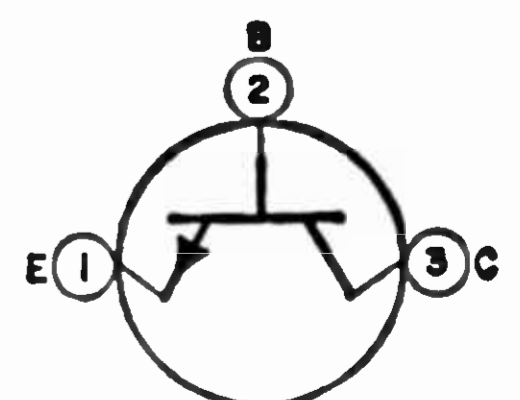
Collector-to-Base Breakdown Voltage ($I_C = 0.3$ mA, $I_E = 0$)	$V_{(BR)CBO}$	65 min	V
Collector-to-Emitter Breakdown Voltage:			
$I_C = 0$ to 200 mA, $I_B = 0$, pulsed through inductor $L = 25$ mH, $df = 50\%$	$V_{(BR)CEO}$	40 min	V
$I_C = 0$ to 200 mA, $V_{BE} = -1.5$ V, pulsed through inductor $L = 25$ mH, $df = 50\%$	$V_{(BR)CEV}$	65 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.1$ mA, $I_C = 0$)	$V_{(BR)EBO}$	4 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 250$ mA, $I_B = 50$ mA)	$V_{CE(sat)}$	1 max	V
Collector-Cutoff Current ($V_{CE} = 30$ V, $I_B = 0$)	I_{CEO}	0.1 max	μ A
Static Forward-Current Transfer Ratio ($V_{CE} = 5$ V, $I_C = 150$ mA)	h_{FE}	10 min	
Output Capacitance ($V_{CB} = 30$ V, $I_E = 0$, $f = 1$ MHz)	C_{ob0}	10 max	pF
RF Power Output, Amplifier, Unneutralized: ($V_{CE} = 28$ V, $P_{IE} = 0.25$ W, $f = 175$ MHz, R_G and $R_L = 50 \Omega$)	P_{OE}	2.5† min	W

* For type 40306 this value is maximum Pin-Soldering Temperature.

† For conditions given, minimum efficiency = 50 per cent.

40306**TRANSISTOR**

Si n-p-n "overlay" epitaxial planar type subjected to special preconditioning tests for high-reliability, large-signal, high-power vhf-uhf applications in class A, B, and C amplifier, frequency-multiplier, and oscillator circuits in aerospace, industrial and military equipment. JEDEC TO-60, Outline No.23. See Mounting Hardware for desired mounting arrangement. This type is identical with type 40305 except for the following items:



MAXIMUM RATINGS

Collector Current	I_C	1.5	A
Transistor Dissipation: T _c up to 25°C	P _T	11.6	W

CHARACTERISTICS (At case temperature = 25°C)

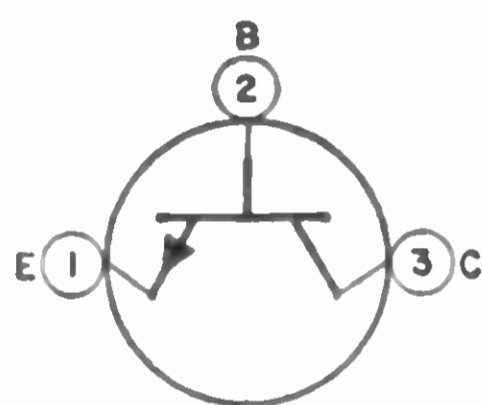
Collector-to-Base Breakdown Voltage ($I_C = 0.1$ mA, $I_E = 0$)	$V_{(BR)CBO}$	65 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 500$ mA, $I_B = 100$ mA)	$V_{CE(sat)}$	1 max	V
RF Power Output, Amplifier, Unneutralized: $V_{CE} = 28$ V, $P_{IE} = 1$ W, $f = 100$ MHz, R_G and $R_L = 50$ Ω	P _{OE}	7.5* min	W
$V_{CE} = 28$ V, $P_{IE} = 1$ W, $f = 400$ MHz, R_G and $R_L = 50$ Ω	P _{OE}	3† min	W

* For conditions given, minimum efficiency = 65 per cent.

† For conditions given, minimum efficiency = 40 per cent.

TRANSISTOR

40307



Si n-p-n "overlay" epitaxial planar type subjected to special preconditioning tests for high-reliability, large-signal, high-power vhf-uhf applications in class A, B, and C amplifier, frequency-multiplier, and oscillator circuits in aerospace, industrial and military equipment. JEDEC TO-60, Outline No.23. See Mounting Hardware

for desired mounting arrangement.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	65	V
Collector-to-Emitter Voltage: $V_{BE} = -1.5$ V	V_{CEV}	65	V
Base open	V_{CEO}	40	V
Emitter-to-Base Voltage	V_{EBO}	4	V
Collector Current	I_C	3	A
Transistor Dissipation: T _c up to 25°C	P _T	23	W
T _c above 25°C	P _T	See curve page 300	
Temperature Range: Operating (Junction)	T _J (opr)	-65 to 200	°C
Storage	T _{STG}	-65 to 200	°C
Pin-Soldering Temperature (10 s max)	T _P	230	°C

CHARACTERISTICS (At case temperature = 25°C)

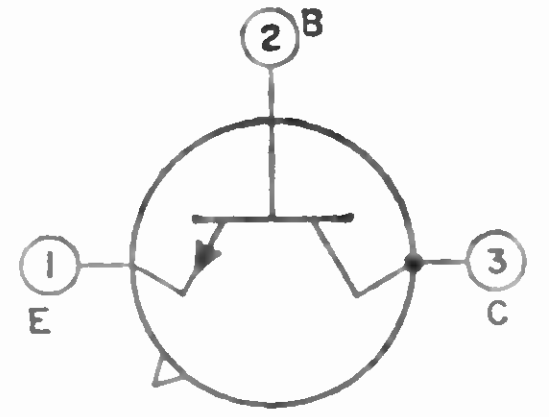
Collector-to-Base Breakdown Voltage ($I_C = 0.5$ mA, $I_E = 0$)	$V_{(BR)CBO}$	65 min	V
Collector-to-Emitter Breakdown Voltage: $I_C = 0$ to 200 mA, $I_B = 0$, pulsed through inductor L = 25 mH, df = 50%	$V_{(BR)CEO}$	40 min	V
$I_C = 0$ to 200 mA, $V_{BE} = -1.5$ V, pulsed through inductor L = 25 mH, df = 50%	$V_{(BR)CEV}$	65 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.25$ mA, $I_C = 0$)	$V_{(BR)EBO}$	4 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 500$ mA, $I_B = 100$ mA)	$V_{CE(sat)}$	1 max	V
Collector-Cutoff Current ($V_{CE} = 30$ V, $I_B = 0$)	I_{CEO}	0.25 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 5$ V, $I_C = 300$ mA)	h_{FE}	10 min	
Output Capacitance ($V_{CB} = 30$ V, $I_E = 0$, $f = 1$ MHz)	C _{ob0}	20 max	pF
RF Power Output, Amplifier, Unneutralized: ($V_{CE} = 28$ V, $P_{IE} = 3.5$ W, $f = 175$ MHz, R_G and $R_L = 50$ Ω)	P _{OE}	13.5† min	W

† For conditions given, minimum efficiency = 70 per cent.

40309

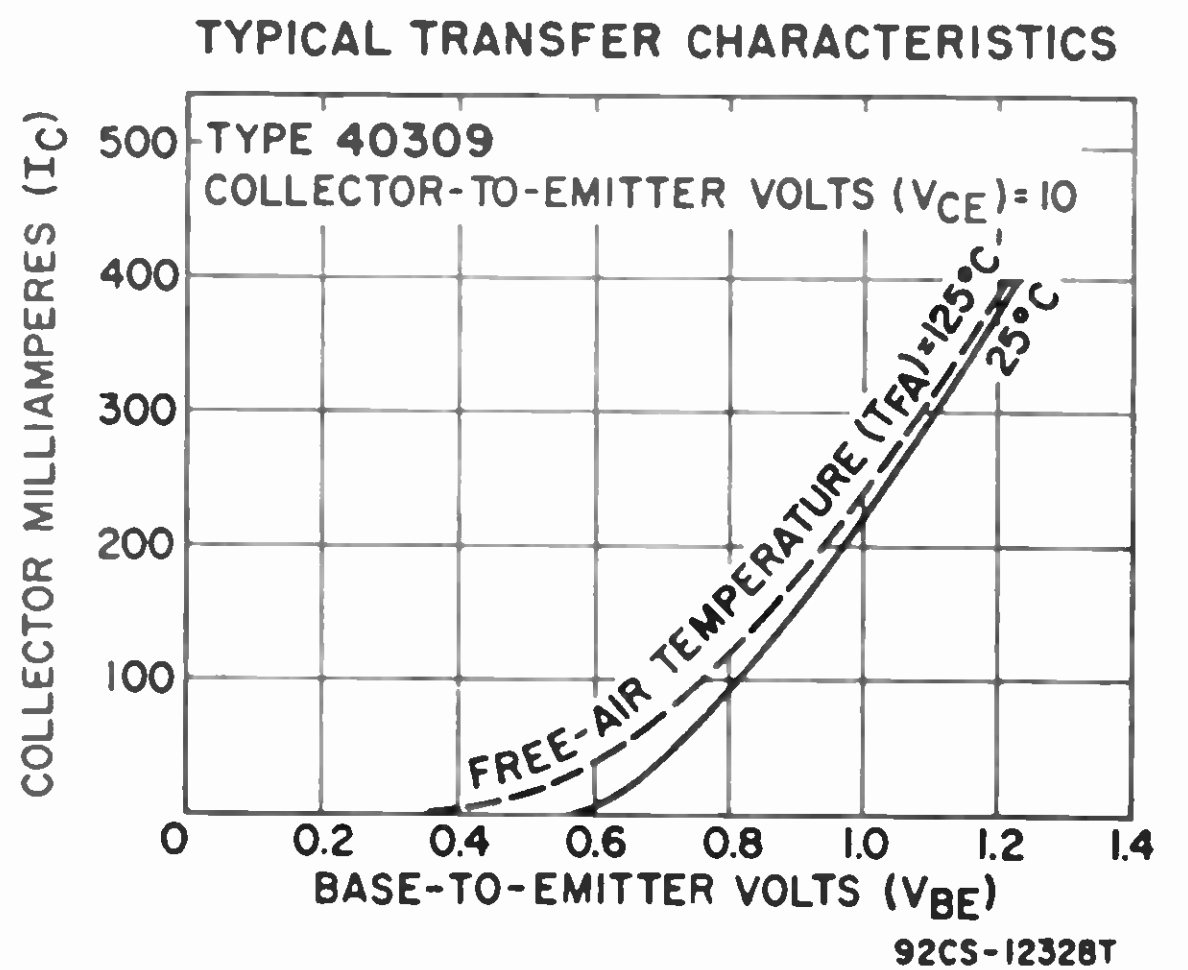
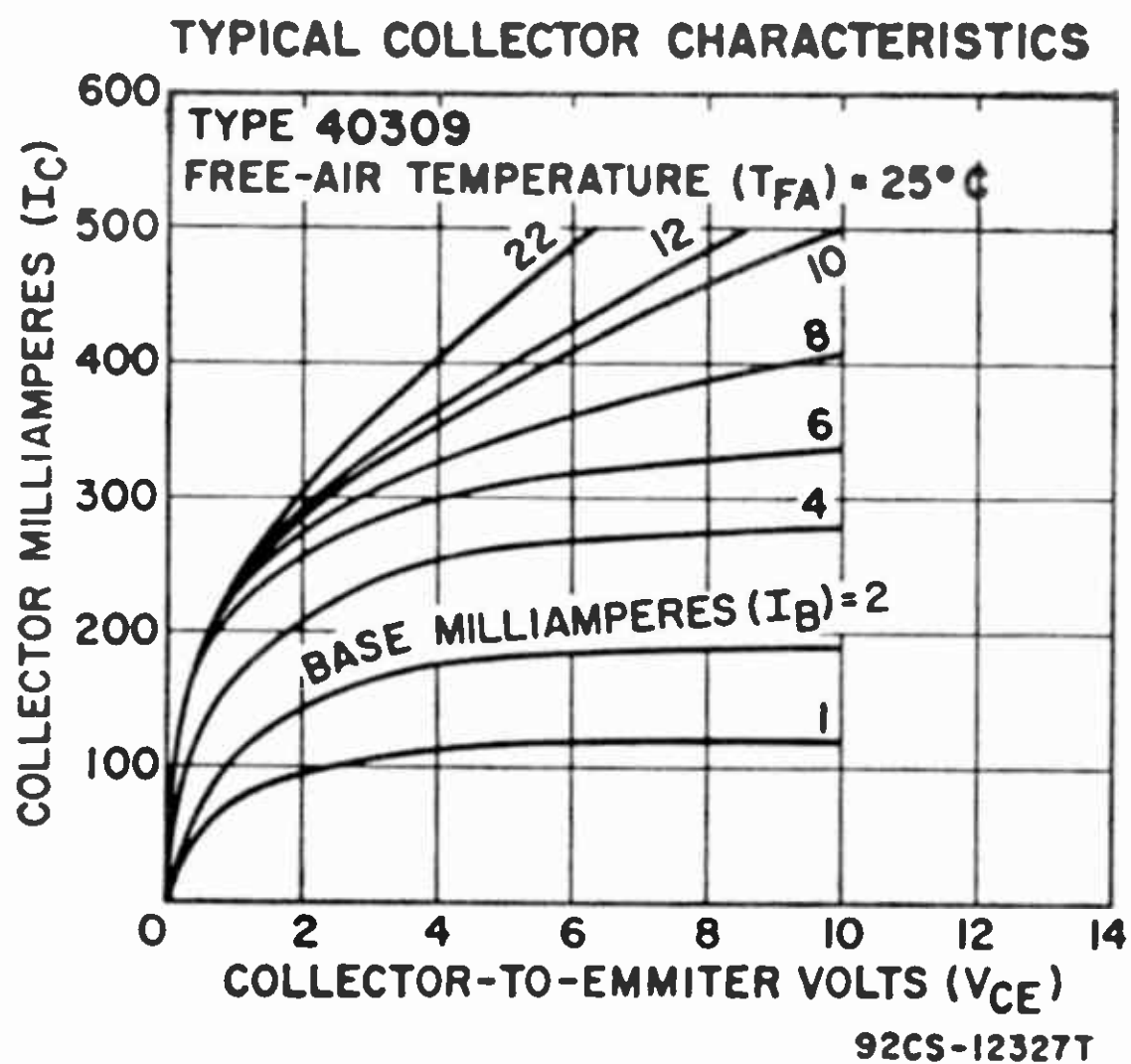
POWER TRANSISTOR

Si n-p-n type used in audio-amplifier driver stages for economical high-quality performance. Designed to assure freedom from second breakdown in the operating region. JEDEC TO-5, Outline No.5.



MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage	$V_{CEO(sus)}$	18	V
Emitter-to-Base Voltage	V_{EBO}	2.5	V
Collector Current	I_C	0.7	A
Base Current	I_B	0.2	A
Transistor Dissipation:			
T_A up to 25°C	P_T	1	W
T_C up to 25°C	P_T	5	W
T_A and T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 200	°C



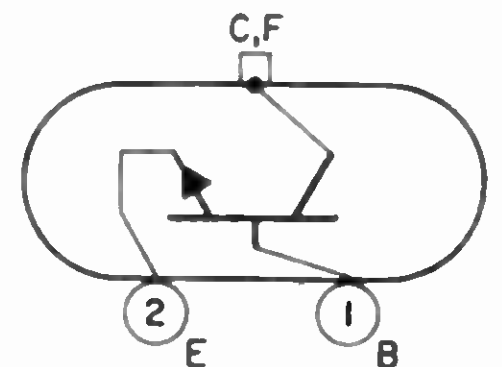
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Breakdown Voltage ($I_C = 100\text{ mA}$, $I_B = 0$, $t_p = 300\ \mu s$, $df \leq 2\%$)	$V_{(BR)CEO}$	18 min	V
Base-to-Emitter Voltage ($V_{CE} = 4\text{ V}$, $I_C = 50\text{ mA}$) ...	V_{BE}	1 max	V
Collector-Cutoff Current:			
$V_{CB} = 15\text{ V}$, $I_E = 0$, $T_C = 25^\circ\text{C}$	I_{CBO}	0.25 max	μA
$V_{CB} = 15\text{ V}$, $I_E = 0$, $T_C = 150^\circ\text{C}$	I_{CBO}	1 max	mA
Emitter-Cutoff Current ($V_{EB} = 2.5\text{ V}$, $I_C = 0$)	I_{EBO}	1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 4\text{ V}$, $I_C = 50\text{ mA}$)	h_{FE}	70 to 350	
Gain-Bandwidth Product ($V_{CE} = 10\text{ V}$, $I_C = 50\text{ mA}$)	f_T	100	MHz
Thermal Resistance, Junction-to-Case	θ_{J-C}	35 max	°C/W
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	175 max	°C/W

40310

POWER TRANSISTOR

Si n-p-n type used in audio-amplifier driver stages for economical high-quality performance. Designed to assure freedom from second breakdown in the operating region. JEDEC TO-66, Outline No.25. See Mounting Hardware for desired mounting arrangement.



MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage	$V_{CEO(sus)}$	35	V
Emitter-to-Base Voltage	V_{EBO}	2.5	V
Collector Current	I_C	4	A
Base Current	I_B	2	A

MAXIMUM RATINGS (cont'd)

Transistor Dissipation:

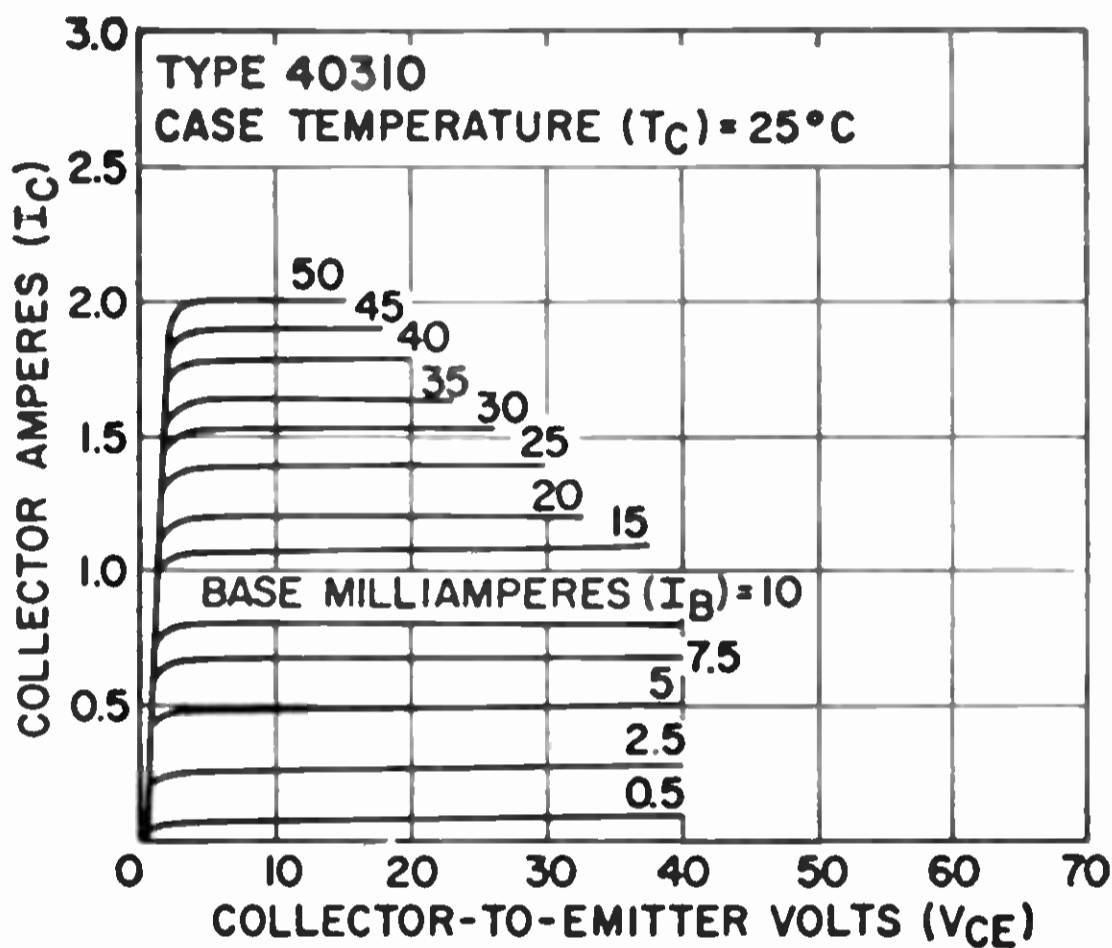
T_c up to 25°C	P_T	29	W
T_c above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Breakdown Voltage

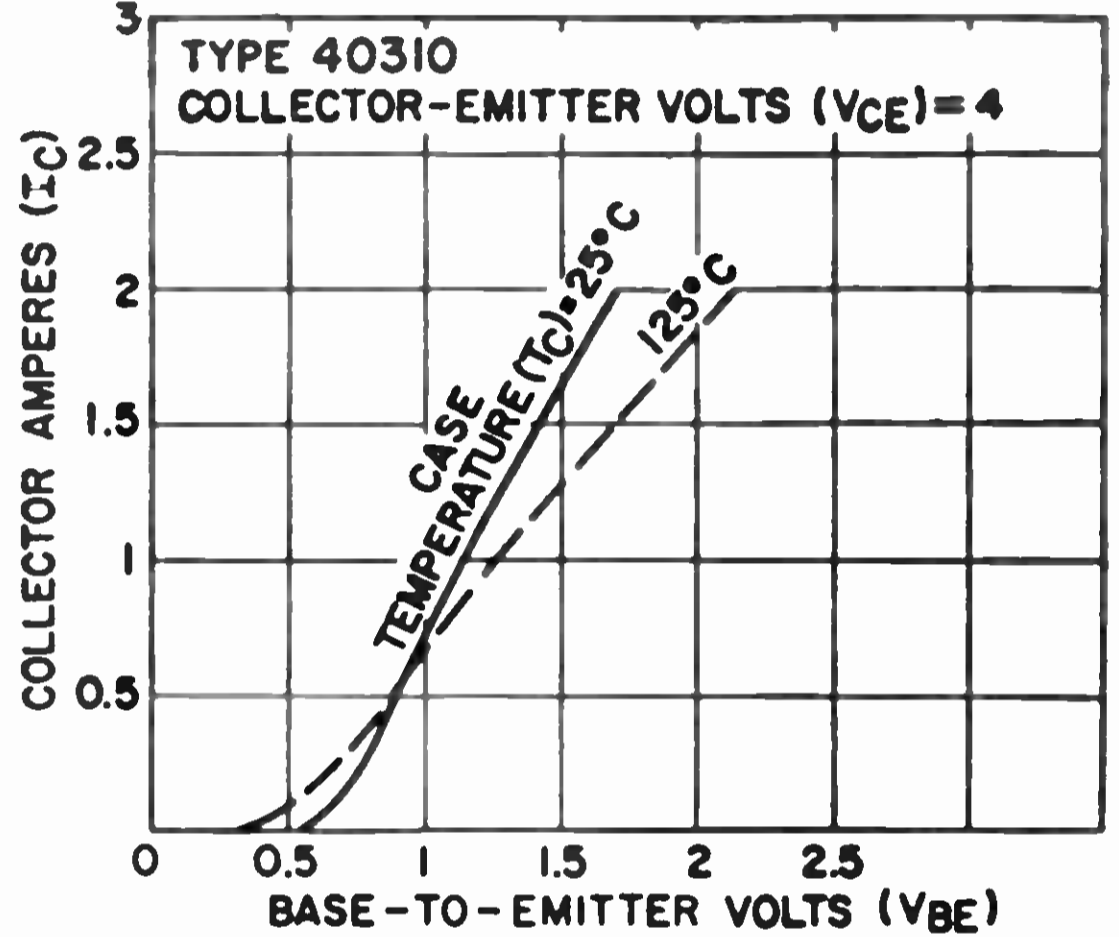
($I_C = 100$ mA, $I_B = 0$)	$V_{(BR)CEO}$	35 min	V
Base-to-Emitter Voltage ($V_{CE} = 2$ V, $I_C = 1$ A)	V_{BE}	1.4 max	V
Collector-Cutoff Current:			
$V_{CB} = 15$ V, $I_E = 0$, $T_c = 25^\circ\text{C}$	I_{CBO}	10 max	μA
$V_{CB} = 15$ V, $I_E = 0$, $T_c = 150^\circ\text{C}$	I_{CBO}	5 max	mA
Emitter-Cutoff Current ($V_{EB} = 2.5$ V, $I_C = 0$)	I_{EBO}	5 max	mA
Static Forward-Current Transfer Ratio			
($V_{CE} = 2$ V, $I_C = 1$ A)	h_{FE}	20 to 120	
Gain-Bandwidth Product ($V_{CE} = 4$ V, $I_C = 500$ mA)	f_T	750	kHz
Thermal Resistance, Junction-to-Case	θ_{J-C}	6 max	°C/W

TYPICAL COLLECTOR CHARACTERISTICS

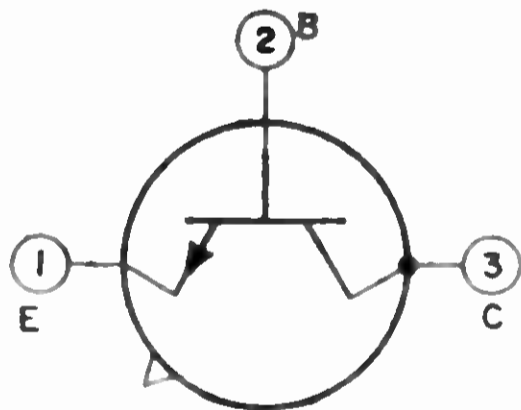


92CS-13004T

TYPICAL TRANSFER CHARACTERISTICS



92CS-12325T



POWER TRANSISTOR

40311

Si n-p-n type used in audio-amplifier driver stages for economical high-quality performance. Designed to assure freedom from second breakdown in the operating region. JEDEC TO-5, Outline No.5.

MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage	V_{CEO} (sus)	30	V
Emitter-to-Base Voltage	V_{EBO}	2.5	V
Collector Current	I_C	0.7	A
Base Current	I_B	0.2	A
Transistor Dissipation:			
T_A up to 25°C	P_T	1	W
T_c up to 25°C	P_T	5	W
T_A and T_c above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C

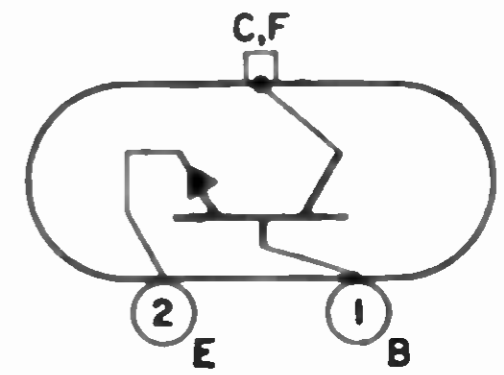
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage

($I_C = 100$ mA, $I_B = 0$, $t_p = 300$ μs , $df \leq 2\%$)	V_{CEO} (sus)	30 min	V
Base-to-Emitter Voltage ($V_{CE} = 4$ V, $I_C = 50$ mA)	V_{BE}	1 max	V
Collector-Cutoff Current:			
$V_{CB} = 15$ V, $I_E = 0$, $T_c = 25^\circ\text{C}$	I_{CBO}	0.25 max	μA
$V_{CB} = 15$ V, $I_E = 0$, $T_c = 150^\circ\text{C}$	I_{CBO}	1 max	mA
Emitter-Cutoff Current ($V_{EB} = 2.5$ V, $I_C = 0$)	I_{EBO}	1 max	mA
Static Forward-Current Transfer Ratio			
($V_{CE} = 4$ V, $I_C = 50$ mA)	h_{FE}	70 to 350	
Gain-Bandwidth Product ($V_{CE} = 10$ V, $I_C = 50$ mA)	f_T	100	MHz
Thermal Resistance, Junction-to-Case	θ_{J-C}	35 max	°C/W
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	175 max	°C/W

40312 POWER TRANSISTOR

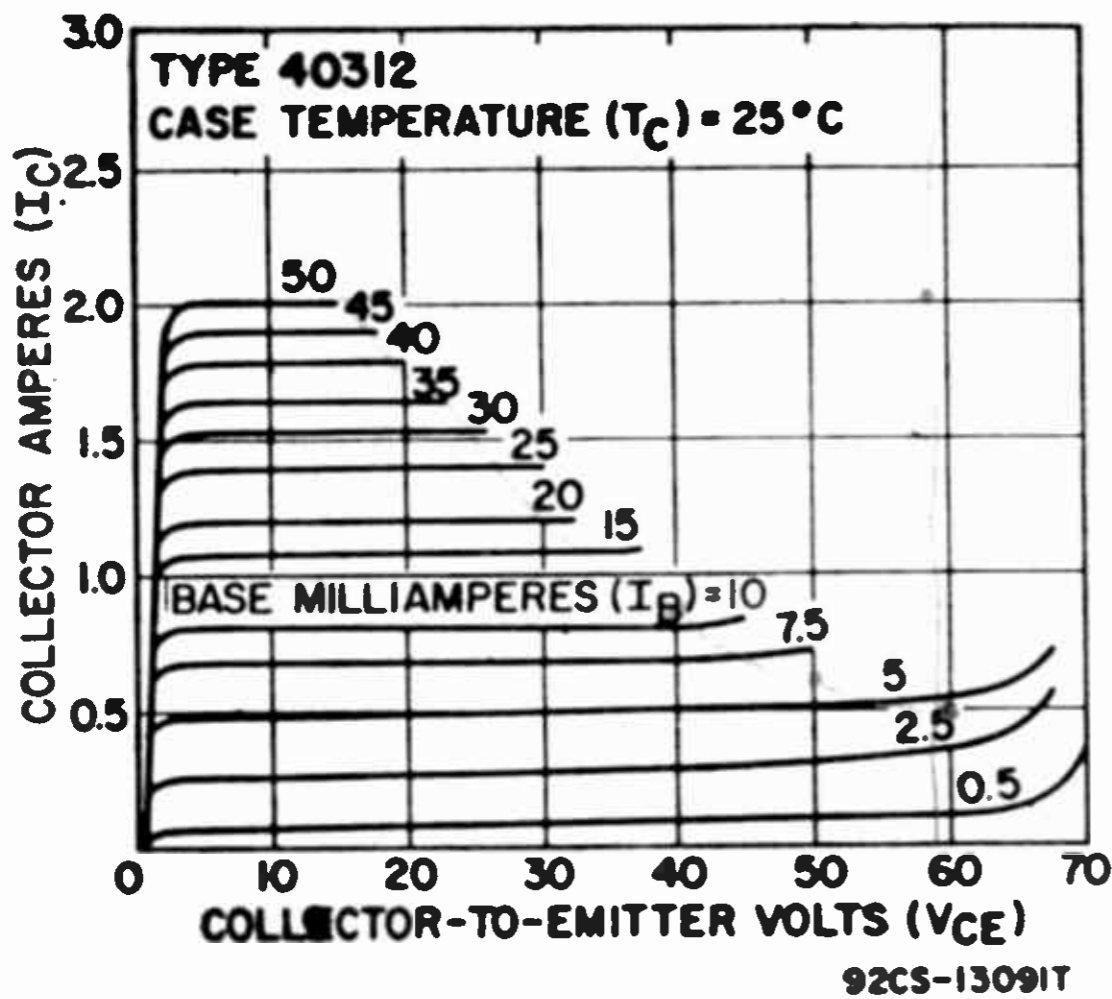
Si n-p-n type used in audio-amplifier output stages for economical high-quality performance. Designed to assure freedom from second breakdown in the operating region. JEDEC TO-66, Outline No.25 See Mounting Hardware for desired mounting arrangement.



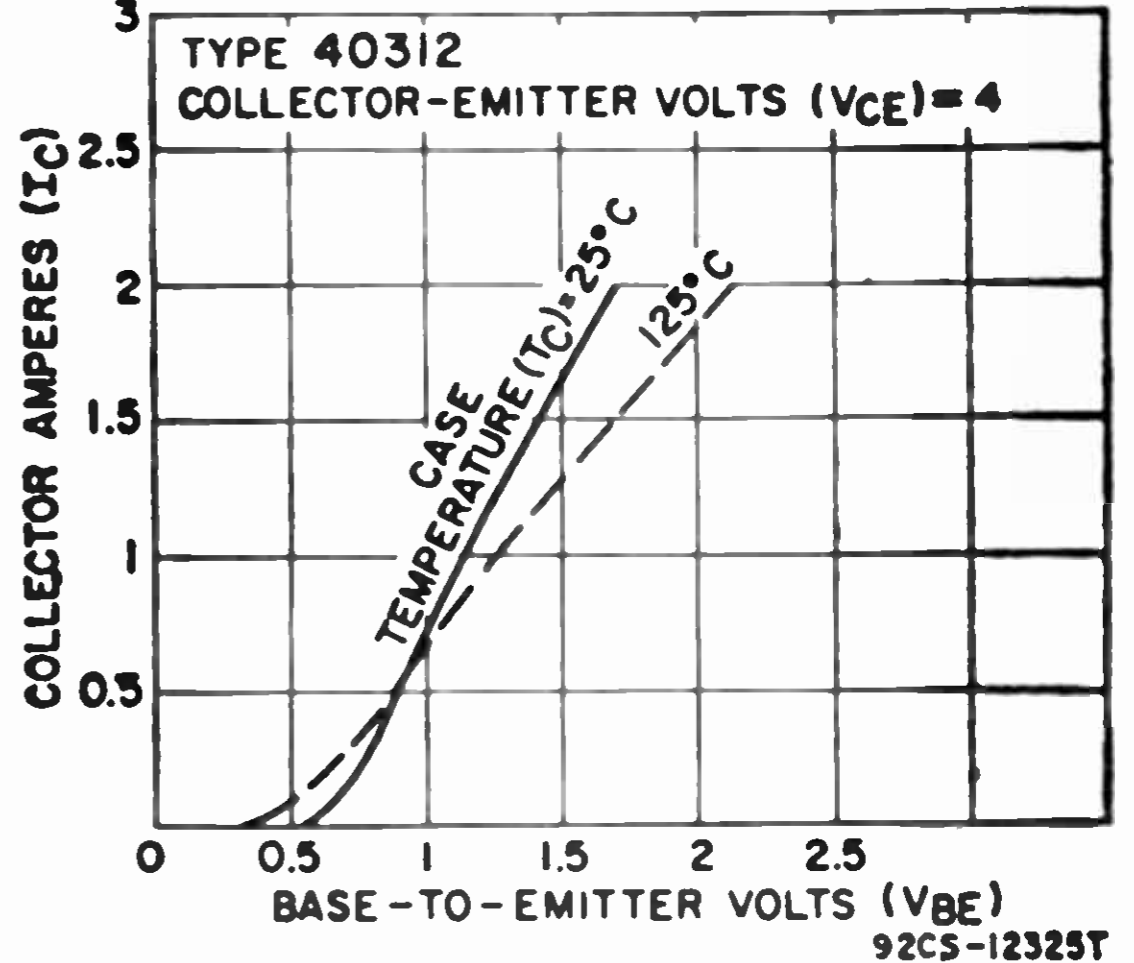
MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage ($R_{BE} = 500 \Omega$)	$V_{CER(SUS)}$	60	V
Emitter-to-Base Voltage	V_{CBO}	2.5	V
Collector Current	I_C	4	A
Base Current	I_B	2	A
Transistor Dissipation:			
T_c up to 25°C	P_T	29	W
T_c above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 200	°C

TYPICAL COLLECTOR CHARACTERISTICS



TYPICAL TRANSFER CHARACTERISTICS

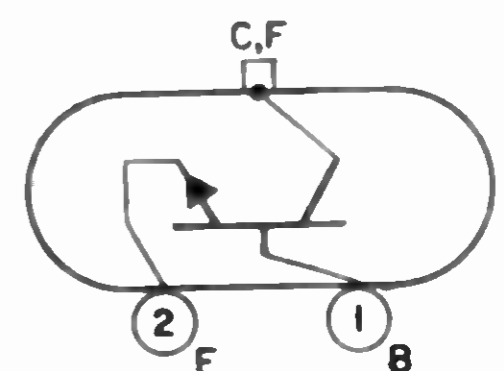


CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_C = 100 \text{ mA}$, $R_{BE} = 500 \Omega$, $t_p = 300 \mu s$, $df = 2\%$)	$V_{CER(SUS)}$	60 min	V
Base-to-Emitter Voltage ($V_{CE} = 2 \text{ V}$, $I_C = 1 \text{ A}$)	V_{BE}	1.4 max	v
Collector-Cutoff Current:			
$V_{CB} = 15 \text{ V}$, $I_E = 0$, $T_c = 25^\circ\text{C}$	I_{CBO}	10 max	μA
$V_{CB} = 15 \text{ V}$, $I_E = 0$, $T_c = 150^\circ\text{C}$	I_{CBO}	5 max	mA
Emitter-Cutoff Current ($V_{EB} = 2.5 \text{ V}$, $I_C = 0$)	I_{EBO}	5 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 2 \text{ V}$, $I_C = 1 \text{ A}$)	h_{FE}	20 to 120	
Gain-Bandwidth Product ($V_{CE} = 4 \text{ V}$, $I_C = 500 \text{ mA}$)	f_T	750	kHz
Thermal Resistance, Junction-to-Case	θ_{J-C}	6 max	°C/W

40313 POWER TRANSISTOR

Si n-p-n high-voltage type for direct 117-volt line operation in audio-amplifier output stages for economical high-quality performance. Designed to assure freedom from second breakdown in the operating region. JEDEC TO-66, Outline No.25. See Mounting Hardware for desired mounting arrangement.



MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage ($R_{BE} = 500 \Omega$)	$V_{CER(SUS)}$	300	V
Emitter-to-Base Voltage	V_{EBO}	2.5	V
Collector Current	I_C	2	A
Base Current	I_B	1	A

MAXIMUM RATINGS (cont'd)

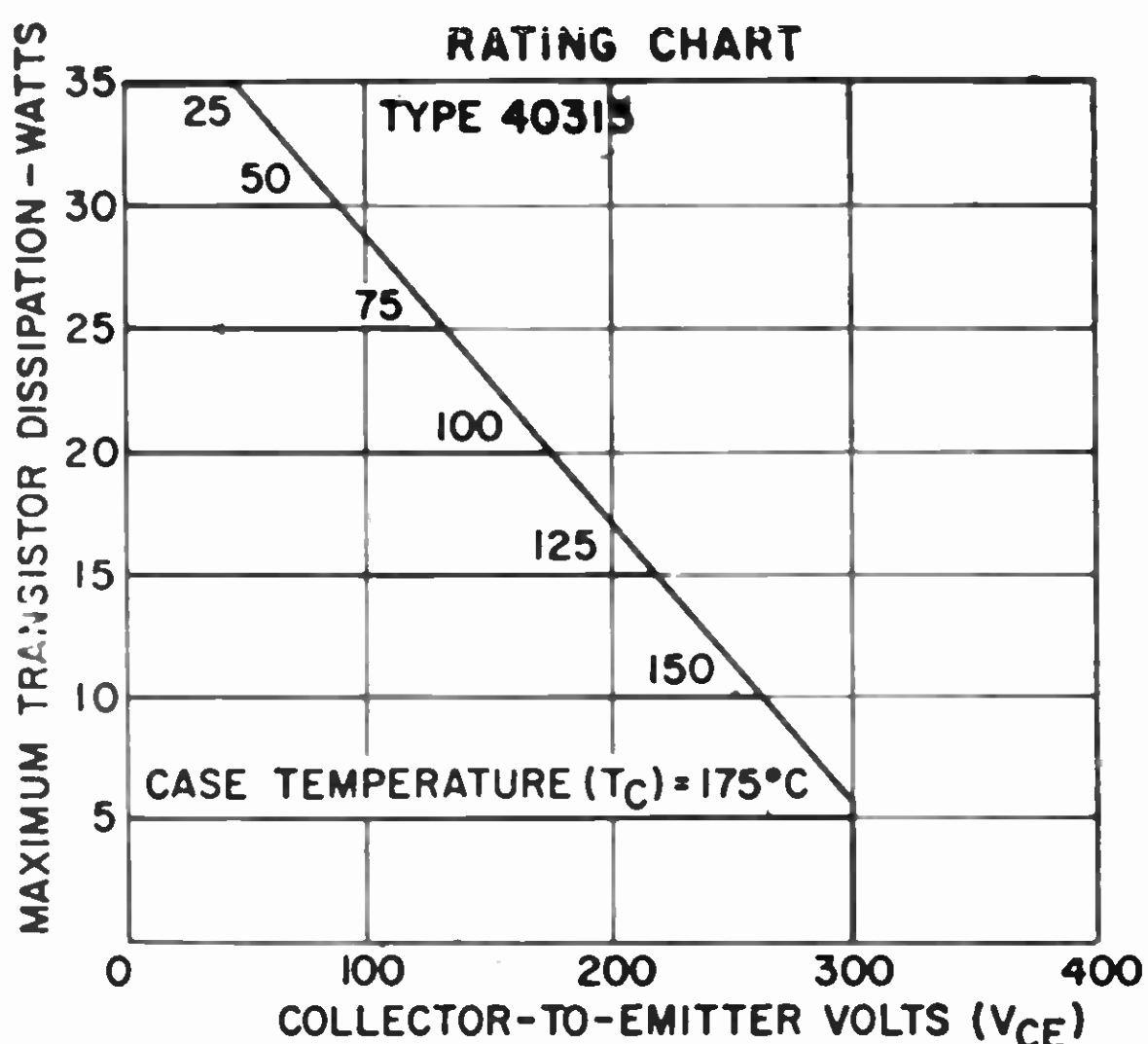
Transistor Dissipation:

T_c up to 25°C	P_T	35	W
T_c above 25°C	P_T	See Rating Chart	W
$T_c = 175^\circ\text{C}$	P_T	5	W
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 200	°C

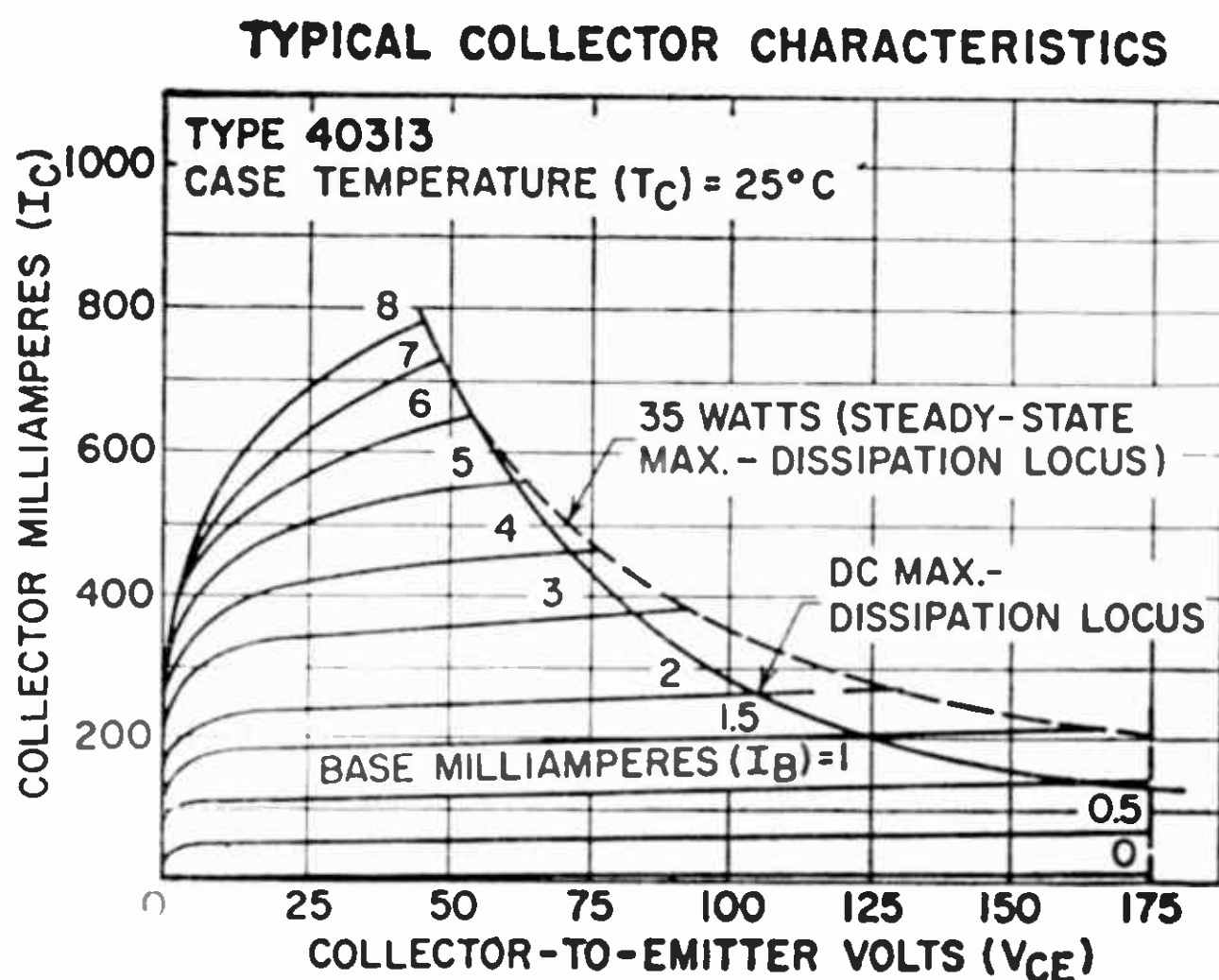
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage

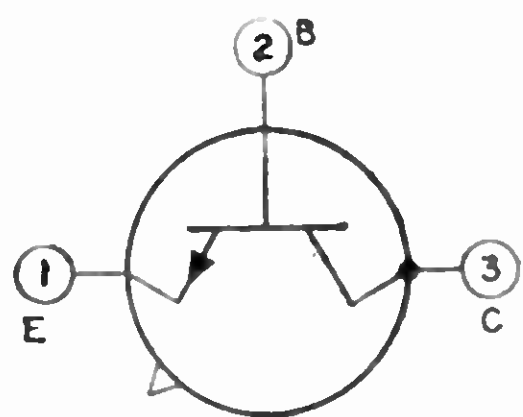
($I_c = 200\text{ mA}$, $R_{BE} = 500\ \Omega$)	$V_{CER(\text{SUS})}$	300 min	V
Base-to-Emitter Voltage ($V_{CE} = 10\text{ V}$, $I_c = 0.1\text{ A}$) ...	V_{BE}	1.5 max	V
Collector-Cutoff Current:			
$V_{CE} = 150\text{ V}$, $I_B = 0$	I_{CEO}	5 max	mA
$V_{CE} = 300\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_c = 25^\circ\text{C}$	I_{CEV}	10 max	mA
$V_{CE} = 300\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_c = 150^\circ\text{C}$	I_{CEV}	10 max	mA
Emitter-Cutoff Current ($V_{EB} = 2.5\text{ V}$, $I_c = 0$)	I_{EBO}	5 max	mA
Static Forward-Current Transfer Ratio:			
$V_{CE} = 10\text{ V}$, $I_c = 100\text{ mA}$	h_{FE}	40 to 250	
$V_{CE} = 10\text{ V}$, $I_c = 500\text{ mA}$	h_{FE}	40 min	
Second-Breakdown Collector Current ($V_{CE} = 150\text{ V}$)	$I_{S/b}$	150 min	mA
Thermal Resistance, Junction-to-Case	Θ_{J-C}	5 max	°C/W



TL 1744T



TL 1745T



POWER TRANSISTOR

40314

Si n-p-n type used in audio-amplifier driver stages for economical high-quality performance. Designed to assure freedom from second breakdown in the operating region. JEDEC TO-5, Outline No.5.

MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage	$V_{CEO(\text{SUS})}$	40	V
Emitter-to-Base Voltage	V_{EBO}	2.5	V
Collector Current	I_c	0.7	A
Base Current	I_B	0.2	A
Transistor Dissipation:			
T_A up to 25°C	P_T	1	W
T_c up to 25°C	P_T	5	W
T_A and T_c above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 200	°C

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_c = 100\text{ mA}$, $I_B = 0$, $t_p = 300\ \mu\text{s}$, $df = 2\%$)	$V_{CEO(\text{SUS})}$	40 min	V
Collector-to-Emitter Saturation Voltage ($I_c = 150\text{ mA}$, $I_B = 15\text{ mA}$)	$V_{CE(\text{sat})}$	1.4 max	V
Base-to-Emitter Voltage ($V_{CE} = 4\text{ V}$, $I_c = 50\text{ mA}$) ...	V_{BE}	1 max	V

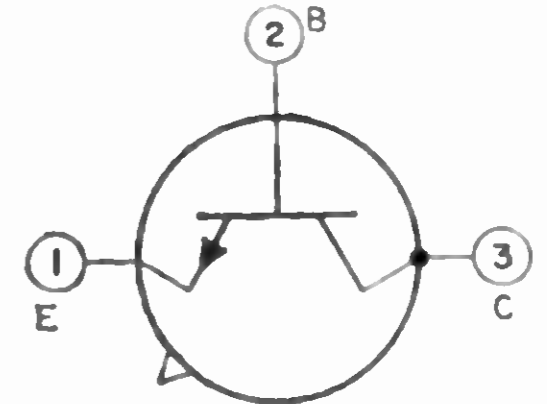
CHARACTERISTICS (cont'd)

Collector-Cutoff Current:

$V_{CB} = 15\text{ V}, I_E = 0, T_C = 25^\circ\text{C}$	I_{CBO}	0.25 max	μA
$V_{CB} = 15\text{ V}, I_E = 0, T_C = 150^\circ\text{C}$	I_{CBO}	1 max	mA
Emitter-Cutoff Current ($V_{EB} = 2.5\text{ V}, I_C = 0$)	I_{EBO}	1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 4\text{ V}, I_C = 50\text{ mA}$)	h_{FE}	35 to 150	
Gain-Bandwidth Product ($V_{CE} = 4\text{ V}, I_C = 50\text{ mA}$)	f_T	100	MHz
Thermal Resistance, Junction-to-Case	θ_{J-C}	35 max	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	175 max	$^\circ\text{C/W}$

40315**POWER TRANSISTOR**

Si n-p-n type used in audio-amplifier inverter and driver stages for economical high-quality performance. Designed to assure freedom from second breakdown in the operating region. JEDEC TO-5, Outline No.5.

**MAXIMUM RATINGS**

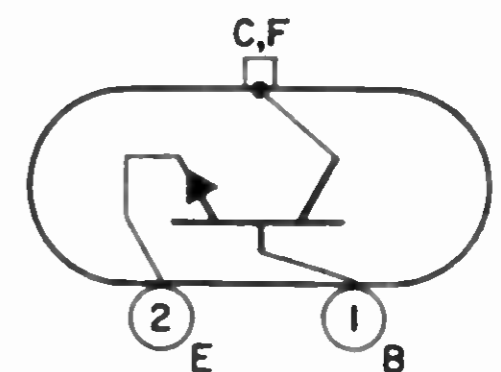
Collector-to-Emitter Sustaining Voltage	$V_{CEO}(\text{sus})$	35	V
Emitter-to-Base Voltage	V_{EBO}	2.5	V
Collector Current	I_C	0.7	A
Base Current	I_B	0.2	A
Transistor Dissipation:			
T_A up to 25°C	P_T	1	W
T_C up to 25°C	P_T	5	W
T_A and T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 200	$^\circ\text{C}$

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Breakdown Voltage ($I_C = 100\text{ mA}, I_B = 0, t_p = 300\ \mu\text{s}, df = 2\%$)	$V_{(BR)CEO}$	35 min	V
Base-to-Emitter Voltage ($V_{CE} = 4\text{ V}, I_C = 50\text{ mA}$)	V_{BE}	1 max	V
Collector-Cutoff Current:			
$V_{CB} = 15\text{ V}, I_E = 0, T_C = 25^\circ\text{C}$	I_{CBO}	0.25 max	μA
$V_{CB} = 15\text{ V}, I_E = 0, T_C = 150^\circ\text{C}$	I_{CBO}	1 max	mA
Emitter-Cutoff Current ($V_{EB} = 2.5\text{ V}, I_C = 0$)	I_{EBO}	1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 4\text{ V}, I_C = 50\text{ mA}$)	h_{FE}	70 to 350	
Gain-Bandwidth Product ($V_{CE} = 10\text{ V}, I_C = 50\text{ mA}$)	f_T	100	MHz
Thermal Resistance, Junction-to-Case	θ_{J-C}	35 max	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	175 max	$^\circ\text{C/W}$

40316**POWER TRANSISTOR**

Si n-p-n type used in audio-amplifier output stages for economical high-quality performance. Designed to assure freedom from second breakdown in the operating region. JEDEC TO-66, Outline No.25. See Mounting Hardware for desired mounting arrangement.

**MAXIMUM RATINGS**

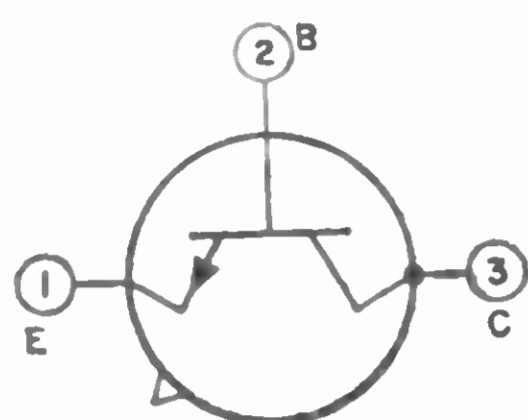
Collector-to-Emitter Sustaining Voltage ($R_{BE} = 500\ \Omega$)	$V_{CER}(\text{sus})$	40	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	4	A
Base Current	I_B	2	A
Transistor Dissipation:			
T_C up to 25°C	P_T	29	W
T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 200	$^\circ\text{C}$

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_C = 100\text{ mA}, R_{BE} = 500\ \Omega$)	$V_{CER}(\text{sus})$	40 min	V
Base-to-Emitter Voltage ($V_{CE} = 2\text{ V}, I_C = 1\text{ A}$)	V_{BE}	1.4 max	V

CHARACTERISTICS (cont'd)

Collector-Cutoff Current: $V_{CB} = 15\text{ V}, I_E = 0, T_C = 25^\circ\text{C}$	I_{CBO}	10 max	μA
$V_{CB} = 15\text{ V}, I_E = 0, T_C = 150^\circ\text{C}$	I_{CBO}	5 max	mA
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}, I_C = 0$)	I_{EBO}	5 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 2\text{ V}, I_C = 1\text{ A}$)	h_{FE}	20 to 120	
Gain-Bandwidth Product ($V_{CE} = 4\text{ V}, I_C = 500\text{ mA}$)	f_T	750	kHz
Thermal Resistance, Junction-to-Case	θ_{J-C}	6 max	$^\circ\text{C/W}$



POWER TRANSISTOR

40317

Si n-p-n type used in audio-amplifier inverter and driver stages for economical high-quality performance. Designed to assure freedom from second breakdown in the operating region. JEDEC TO-5, Outline No.5.

MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage	$V_{CEO(sus)}$	40	V
Emitter-to-Base Voltage	V_{EBO}	2.5	V
Collector Current	I_C	0.7	A
Base Current	I_B	0.2	A
Transistor Dissipation:			
T_A up to 25°C	P_T	1	W
T_C up to 25°C	P_T	5	W
T_A and T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 200	$^\circ\text{C}$

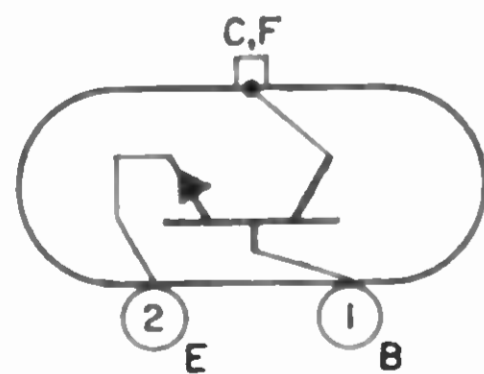
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_C = 100\text{ mA}, I_B = 0, t_p = 300\ \mu\text{s}, df \leq 2\%$)	$V_{CEO(sus)}$	40 min	V
Base-to-Emitter Voltage ($V_{CE} = 4\text{ V}, I_C = 10\text{ mA}$) ...	V_{BE}	1 max	V
Collector-Cutoff Current:			
$V_{CB} = 15\text{ V}, I_E = 0, T_C = 25^\circ\text{C}$	I_{CBO}	0.25 max	μA
$V_{CB} = 15\text{ V}, I_E = 0, T_C = 150^\circ\text{C}$	I_{CBO}	1 max	mA
Emitter-Cutoff Current ($V_{EB} = 2.5\text{ V}, I_C = 0$)	I_{EBO}	1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 4\text{ V}, I_C = 10\text{ mA}$)	h_{FE}	40 to 200	
Thermal Resistance, Junction-to-Case	θ_{J-C}	35 max	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	175 max	$^\circ\text{C/W}$

POWER TRANSISTOR

40318

Si n-p-n high-voltage type for direct 117-volt line operation in audio-amplifier output stages for economical high-quality performance. Designed to assure freedom from second breakdown in the operating region. JEDEC TO-66, Outline No.25. See Mounting Hardware for desired mounting arrangement.



MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage ($R_{BE} = 500\ \Omega$)	$V_{CER(sus)}$	300	V
Emitter-to-Base Voltage	V_{EBO}	6	V
Collector Current	I_C	2	A
Base Current	I_B	1	A
Transistor Dissipation:			
T_C up to 25°C	P_T	35	W
T_C above 25°C	P_T	See Rating Chart	
$T_C = 175^\circ\text{C}$	P_T	5	W
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 200	$^\circ\text{C}$

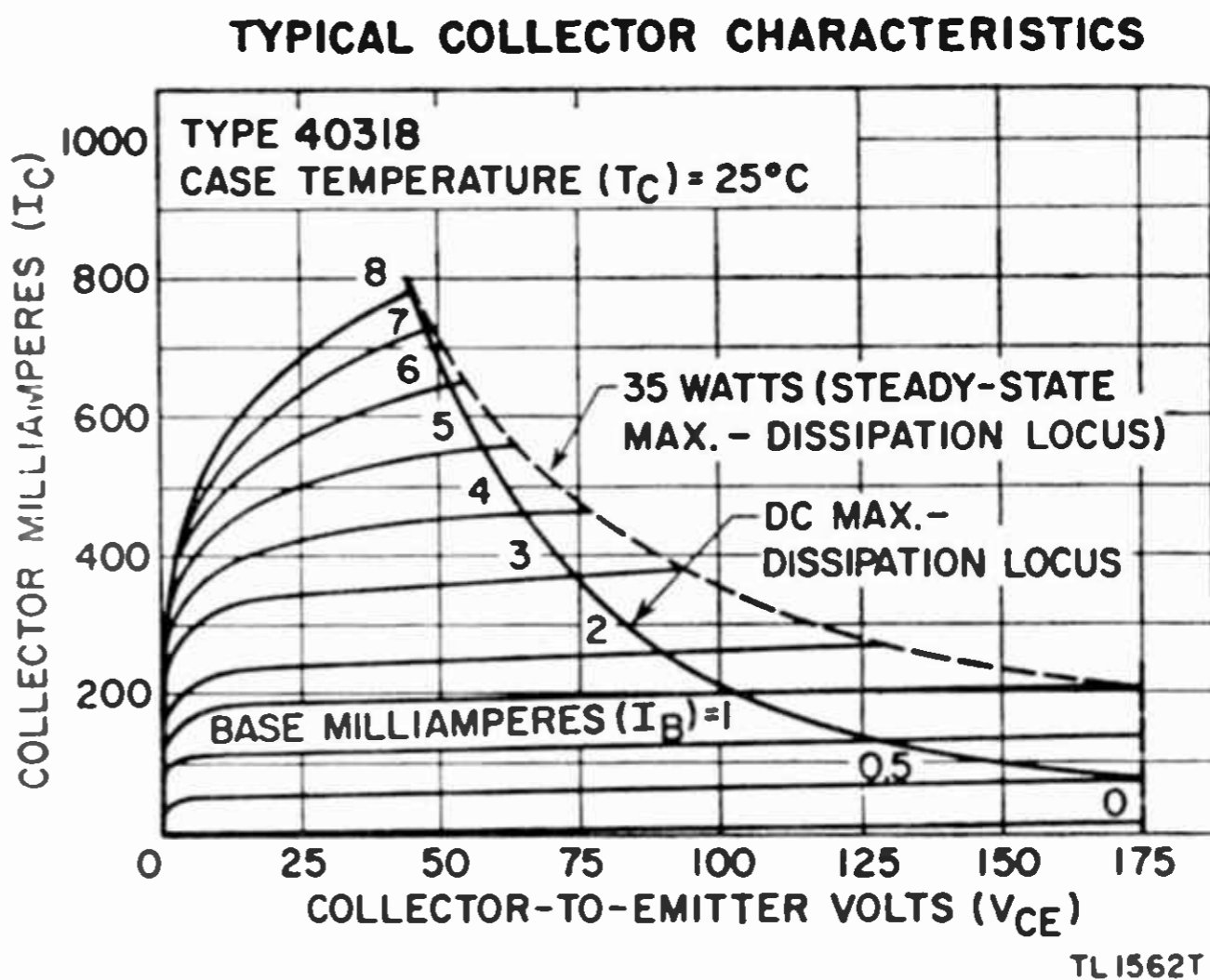
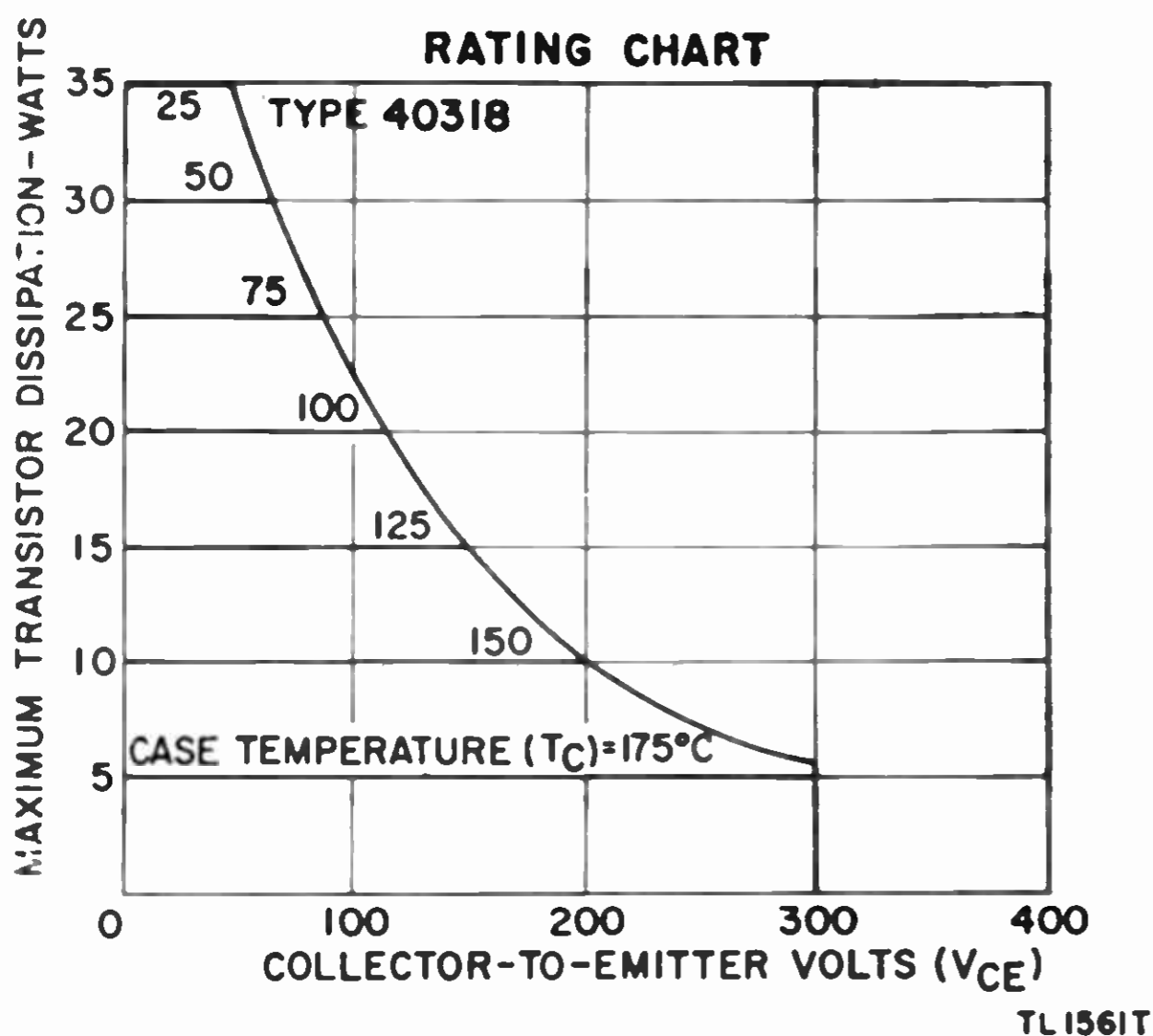
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_C = 200\text{ mA}, R_{BE} = 500\ \Omega$)	$V_{CER(sus)}$	300 min	V
Base-to-Emitter Voltage ($V_{CE} = 10\text{ V}, I_C = 0.5\text{ A}$) ...	V_{BE}	1.5 max	V

CHARACTERISTICS (cont'd)

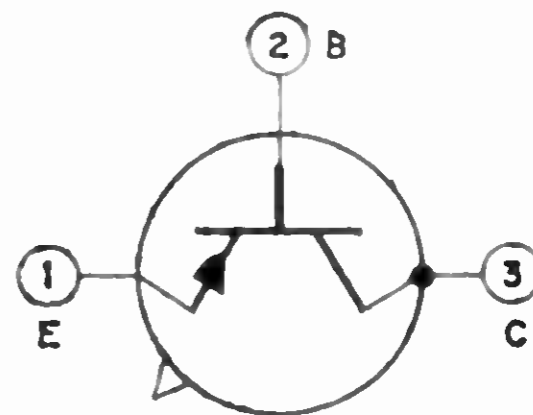
Collector-Cutoff Current:

$V_{CE} = 150 \text{ V}, I_B = 0$	I_{CEO}	5 max	mA
$V_{CE} = 150 \text{ V}, V_{BE} = -1.5 \text{ V}, T_C = 25^\circ\text{C}$	I_{CEV}	5 max	mA
$V_{CE} = 150 \text{ V}, V_{BE} = -1.5 \text{ V}, T_C = 150^\circ\text{C}$	I_{CEV}	10 max	mA
Emitter-Cutoff Current ($V_{EB} = 6 \text{ V}, I_C = 0$)	I_{EBO}	5 max	mA
Static Forward-Current Transfer Ratio:			
$V_{CE} = 10 \text{ V}, I_C = 20 \text{ mA}$	h_{FE}	40 min	
$V_{CE} = 10 \text{ V}, I_C = 500 \text{ mA}$	h_{FE}	50 min	
Second-Breakdown Collector Current ($V_{CB} = 150 \text{ V}$)	$I_{S/b}$	100 min	mA
Second-Breakdown Energy ($V_{EB} = 4 \text{ V}, R_{BE} = 20 \Omega,$ $L = 100 \mu\text{H}$)	$E_{S/b}$	50 min	μJ
Thermal Resistance, Junction-to-Case	θ_{J-C}	5 max	$^\circ\text{C}/\text{W}$



40319 POWER TRANSISTOR

Si p-n-p type used in audio-amplifier driver stages for economical high-quality performance. Designed to assure freedom from second breakdown in the operating region. P-N-P construction permits complementary driver operating with a matching n-p-n type, such as 40314. JEDEC TO-5, Outline No.5.

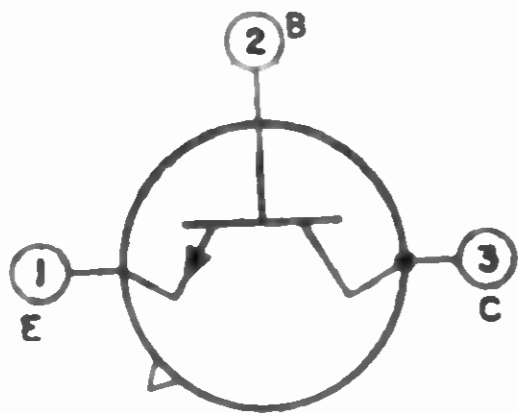
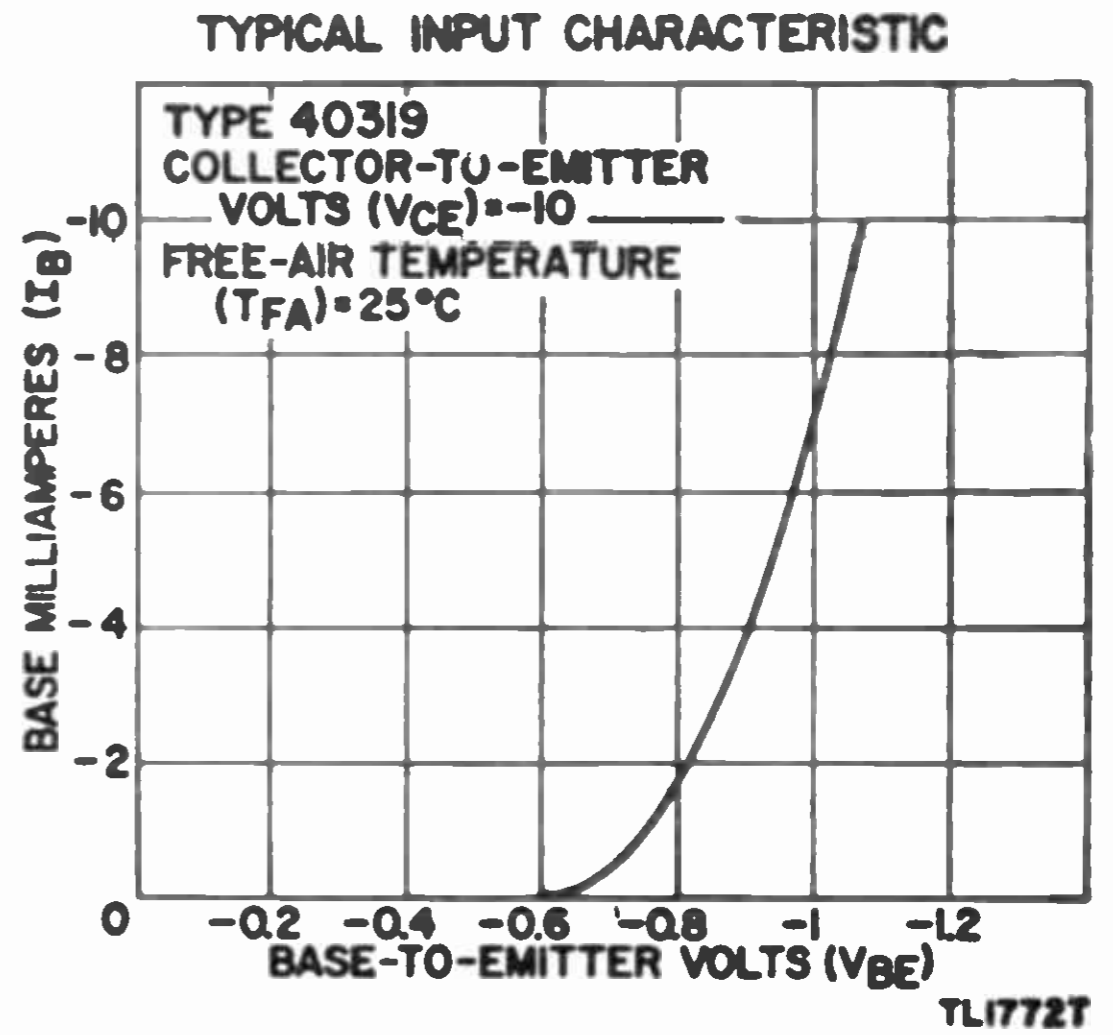
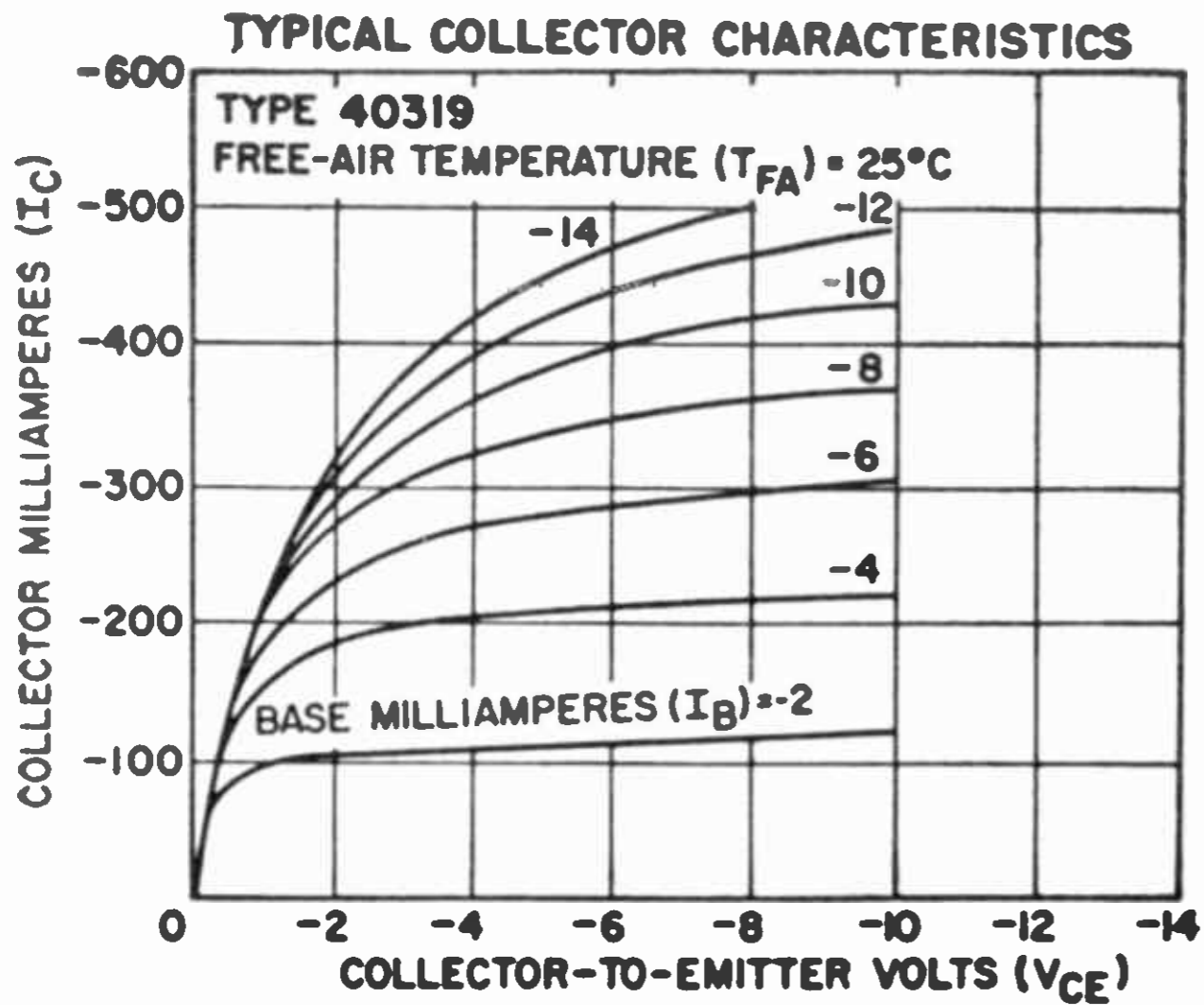


MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage	$V_{CEO(sus)}$	-40	V
Emitter-to-Base Voltage	V_{EBO}	-2.5	V
Collector Current	I_C	-0.7	A
Base Current	I_B	-0.2	A
Transistor Dissipation:			
T_A up to 25°C	P_T	1	W
T_C up to 25°C	P_T	5	W
T_A and T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 200	$^\circ\text{C}$

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_C = -100 \text{ mA}, I_B = 0, t_p = 300 \mu\text{s}, df \leq 2\%$)	$V_{CEO(sus)}$	-40 min	V
Collector-to-Emitter Saturation Voltage ($I_C = -150 \text{ mA}, I_B = -15 \text{ mA}$)	$V_{CE(sat)}$	-1.4 max	V
Base-to-Emitter Voltage ($V_{CE} = -4 \text{ V}, I_C = -50 \text{ mA}$)	V_{BE}	-1 max	V
Collector-Cutoff Current:			
$V_{CB} = -15 \text{ V}, I_E = 0, T_C = 25^\circ\text{C}$	I_{CBO}	-0.25 max	μA
$V_{CB} = -15 \text{ V}, I_E = 0, T_C = 150^\circ\text{C}$	I_{CBO}	-1 max	mA
Emitter-Cutoff Current ($V_{EB} = -2.5 \text{ V}, I_C = 0$)	I_{EBO}	-1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = -4 \text{ V}, I_C = -50 \text{ mA}$)	h_{FE}	35 to 200	
Gain-Bandwidth Product ($V_{CE} = -4 \text{ V}, I_C = -50 \text{ mA}$)	f_T	100	MHz
Thermal Resistance, Junction-to-Case	θ_{J-C}	35 max	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	175 max	$^\circ\text{C}/\text{W}$



POWER TRANSISTOR

40320

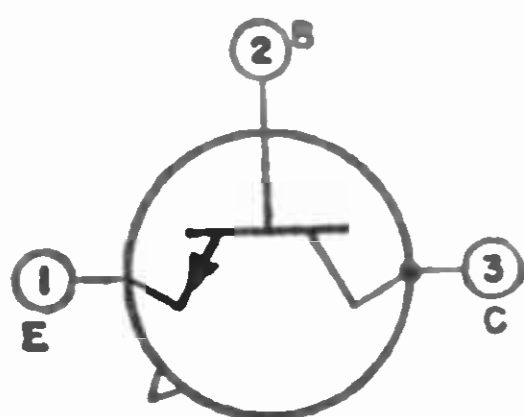
Si n-p-n type used in audio-amplifier and driver stages for economical high-quality performance. Designed to assure freedom from second breakdown in the operating region. JEDEC TO-5, Outline No.5.

MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage	$V_{CE0} (SUS)$	40	V
Emitter-to-Base Voltage	V_{EB0}	2.5	V
Collector Current	I_C	0.7	A
Base Current	I_B	0.2	A
Transistor Dissipation:			
T_A up to 25°C	P_T	1	W
T_C up to 25°C	P_T	5	W
T_A and T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J (opr)$	-65 to 200	°C

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_C = 100\text{ mA}$, $I_B = 0$, $t_p = 300\ \mu s$, $df \leq 2\%$)	$V_{CE0} (SUS)$	40 min	V
Base-to-Emitter Voltage ($V_{CE} = 4\text{ V}$, $I_C = 10\text{ mA}$) ...	V_{BE}	1 max	V
Collector-Cutoff Current:			
$V_{CB} = 15\text{ V}$, $I_E = 0$, $T_C = 25^\circ C$	I_{CBO}	0.25 max	μA
$V_{CB} = 15\text{ V}$, $I_E = 0$, $T_C = 150^\circ C$	I_{CBO}	1 max	mA
Emitter-Cutoff Current ($V_{EB} = 2.5\text{ V}$, $I_C = 0$)	I_{EBO}	1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 4\text{ V}$, $I_C = 10\text{ mA}$)	h_{FE}	40 to 200	
Thermal Resistance, Junction-to-Case	θ_{J-C}	35 max	°C/W



POWER TRANSISTOR

40321

Si n-p-n high-voltage type for direct 117-volt line operation in audio-amplifier driver stages for economical high-quality performance. Designed to assure freedom from second breakdown in the operating region. JEDEC TO-5, Outline No.5.

MAXIMUM RATINGS

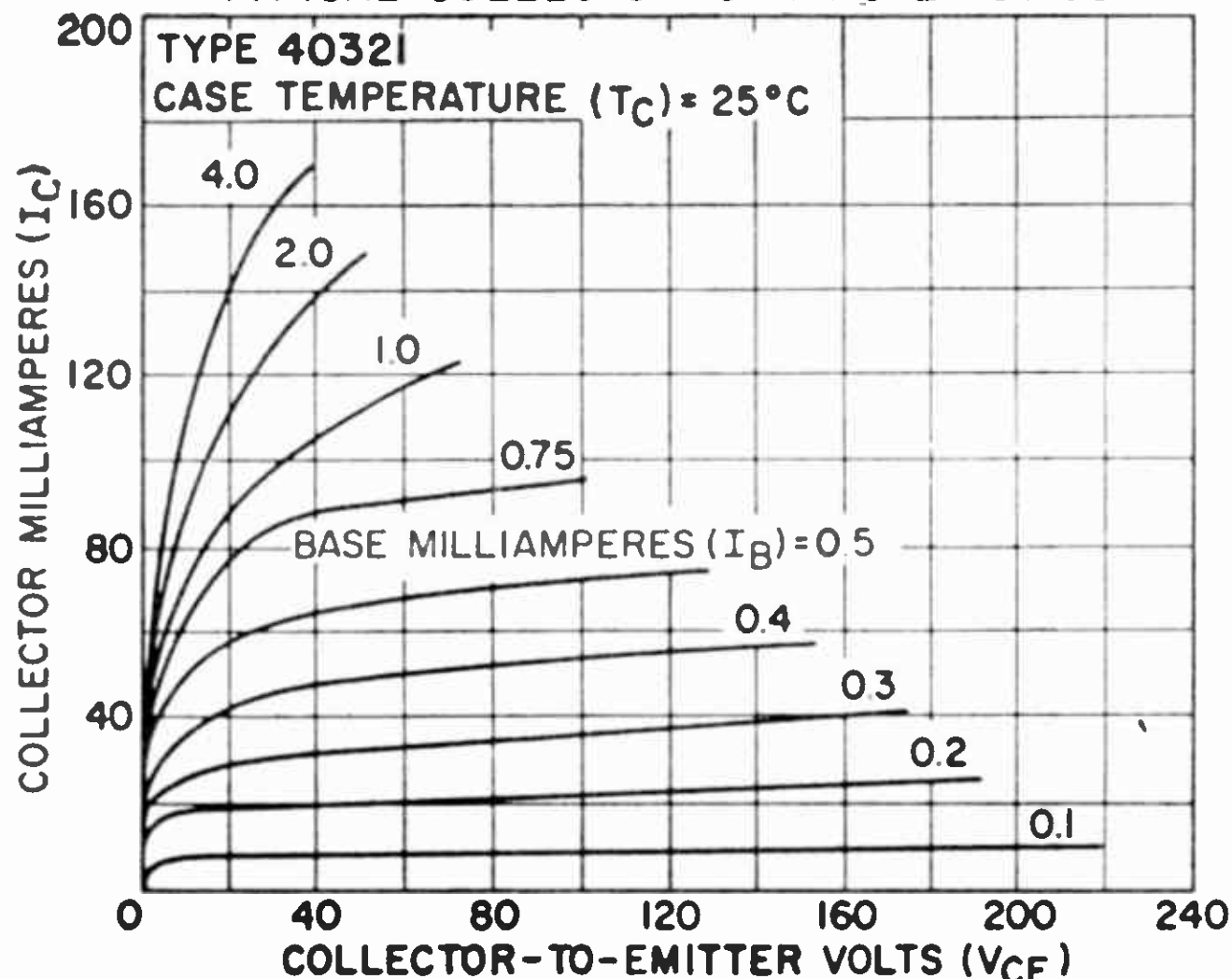
Collector-to-Emitter Sustaining Voltage ($R_{BE} = 1000\ \Omega$)	$V_{CE0} (SUS)$	300	V
Emitter-to-Base Voltage	V_{EB0}	5	V
Collector Current	I_C	1	A
Base Current	I_B	0.5	A

MAXIMUM RATINGS (cont'd)

Transistor Dissipation:

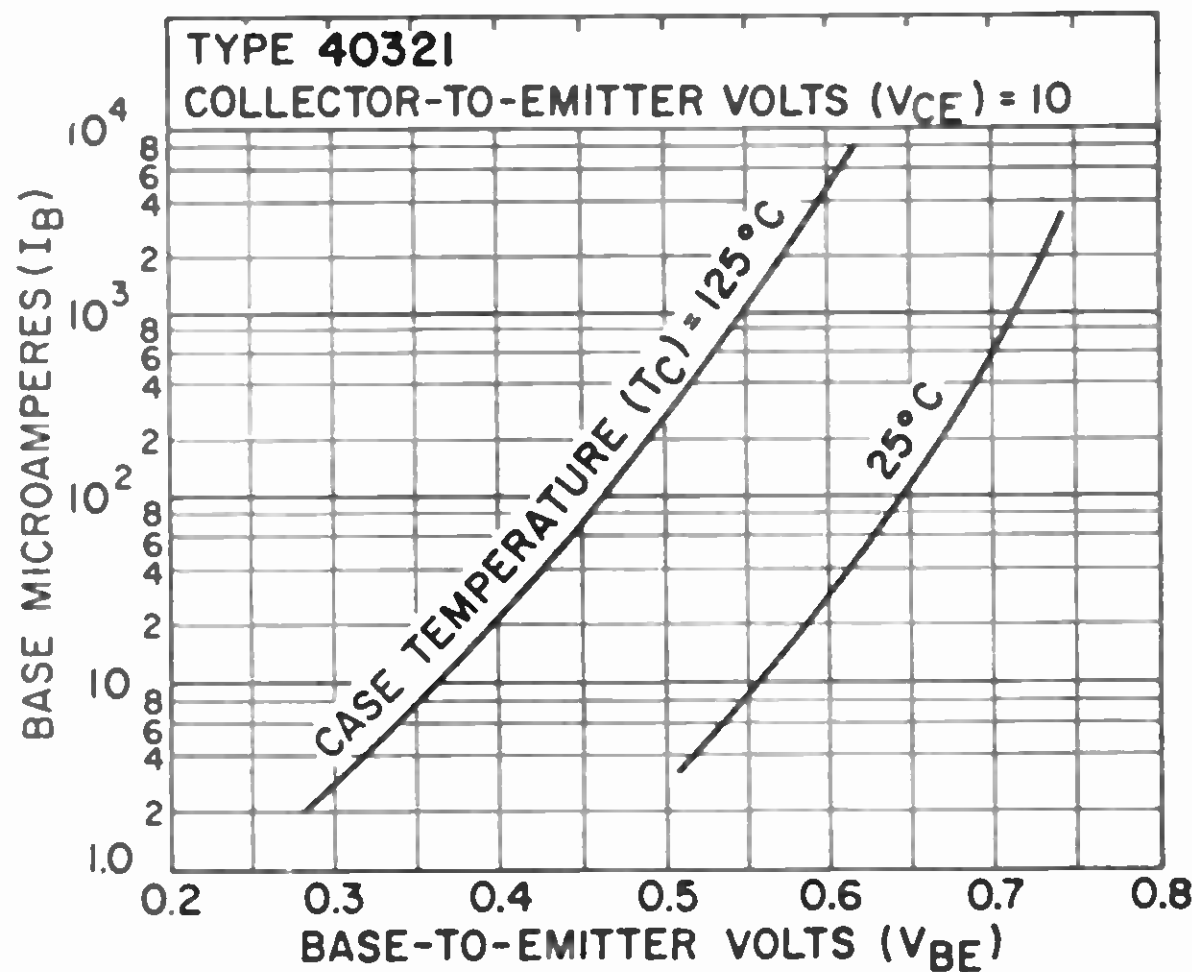
T_A up to 50°C	P_T	1	W
T_C up to 50°C	P_T	5	W
T_A and T_C above 50°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 300	°C

TYPICAL COLLECTOR CHARACTERISTICS



TL 1682T

TYPICAL INPUT CHARACTERISTICS



92CS-12618T

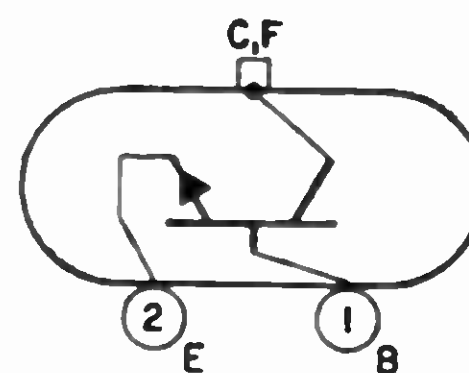
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_C = 50$ mA, $R_{BE} = 1000 \Omega$)	V_{CER} (SUS)	300 min	V
Base-to-Emitter Voltage ($V_{CE} = 10$ V, $I_C = 50$ mA) ...	V_{BE}	2 max	V
Collector-Cutoff Current:			
$V_{CB} = 150$ V, $I_E = 0$, $T_C = 150^\circ\text{C}$	I_{CBO}	100 max	μA
$V_{CE} = 150$ V, $R_{BE} = 1000 \Omega$	I_{CER}	5 max	μA
Emitter-Cutoff Current ($V_{EB} = 5$ V, $I_C = 0$)	I_{EBO}	100 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 10$ V, $I_C = 20$ mA)	h_{FE}	25 to 200	
Thermal Resistance, Junction-to-Case	θ_{J-C}	30 max	°C/W

40322

POWER TRANSISTOR

Si n-p-n high-voltage type for direct 117-volt line operation in audio-amplifier output stages for economical high-quality performance. Designed to assure freedom from second breakdown in the operating region. JEDEC TO-66, Outline No.25. See Mounting Hardware for desired mounting arrangement. For rating chart and collector-characteristics curves, refer to type 40318.



MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage ($R_{BE} = 500 \Omega$)	V_{CER} (SUS)	300	V
Emitter-to-Base Voltage	V_{EBO}	6	V
Collector Current	I_C	2	A
Base Current	I_B	1	A
Transistor Dissipation:			
T_C up to 25°C	P_T	35	W
T_C above 25°C	P_T	See Rating Chart	
$T_C = 175^\circ\text{C}$	P_T	5	W
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C

CHARACTERISTICS (At case temperature = 25°C)

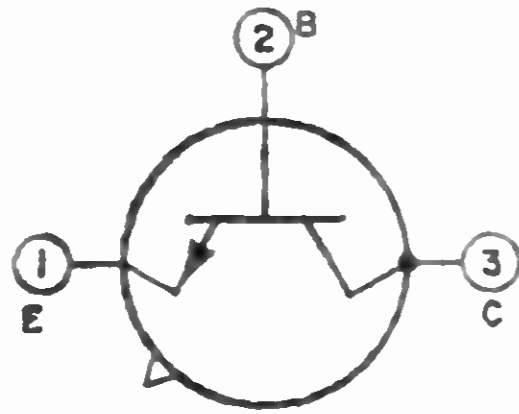
Collector-to-Emitter Sustaining Voltage ($I_C = 200$ mA, $R_{BE} = 200 \Omega$, $L = 5$ mH)	V_{CER} (SUS)	300 min	V
Collector-Cutoff Current:			
$V_{CB} = 150$ V, $I_E = 0$, $T_C = 25^\circ\text{C}$	I_{CEO}	5 max	mA
$V_{CE} = 150$ V, $V_{BE} = -1.5$ V, $T_C = 25^\circ\text{C}$	I_{CEV}	10 max	mA
$V_{CE} = 150$ V, $V_{BE} = -1.5$ V, $T_C = 150^\circ\text{C}$	I_{CEV}	10 max	mA

CHARACTERISTICS (cont'd)

Emitter-Cutoff Current ($V_{EB} = 6\text{ V}$, $I_C = 0$)	I_{EBO}	5 max	mA
Static Forward-Current Transfer Ratio:			
$V_{CE} = 10\text{ V}$, $I_C = 20\text{ mA}$	h_{FE}	40 min	
$V_{CE} = 10\text{ V}$, $I_C = 500\text{ mA}$	h_{FE}	75 min	
Second-Breakdown Collector Current ($V_{CE} = 150\text{ V}$)	$I_{S/b}$	100 min	mA
Second-Breakdown Energy ($V_{EB} = 4\text{ V}$, $R_{BE} = 20\ \Omega$, $L = 100\ \mu\text{H}$)	$E_{S/b}$	50 min	μJ
Thermal Resistance, Junction-to-Case	θ_{J-C}	5 max	$^{\circ}\text{C}/\text{W}$

POWER TRANSISTOR

40323



Si n-p-n type used in audio-amplifier inverter and driver stages for economical high-quality performance. Designed to assure freedom from second breakdown in the operating region. JEDEC TO-5, Outline No.5. For collector-characteristics and transfer-characteristics curves, refer to type 40309.

MAXIMUM RATINGS

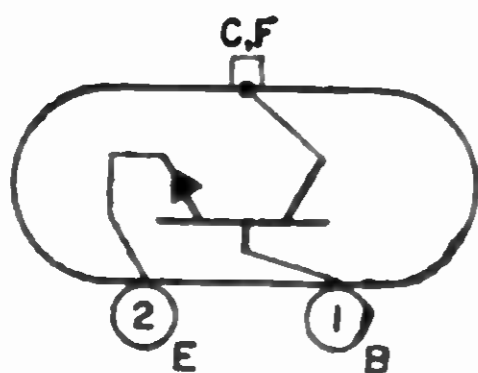
Collector-to-Emitter Sustaining Voltage	$V_{CEO}(\text{sus})$	18	V
Emitter-to-Base Voltage	V_{EBO}	2.5	V
Collector Current	I_C	0.7	A
Base Current	I_B	0.2	A
Transistor Dissipation:			
T_A up to 25°C	P_T	1	W
T_C up to 25°C	P_T	5	W
T_A and T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 200	$^{\circ}\text{C}$

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Breakdown Voltage ($I_C = 100\text{ mA}$, $I_B = 0$, $t_p = 300\ \mu\text{s}$, $df \leq 2\%$)	$V_{(BR)CEO}$	18 min	V
Base-to-Emitter Voltage ($V_{CE} = 4\text{ V}$, $I_C = 50\text{ mA}$) ...	V_{BE}	1 max	V
Collector-Cutoff Current:			
$V_{CB} = 15\text{ V}$, $I_E = 0$, $T_C = 25^{\circ}\text{C}$	I_{CBO}	0.25 max	μA
$V_{CB} = 15\text{ V}$, $I_E = 0$, $T_C = 150^{\circ}\text{C}$	I_{CBO}	1 max	mA
Emitter-Cutoff Current ($V_{EB} = 2.5\text{ V}$, $I_C = 0$)	I_{EBO}	1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 4\text{ V}$, $I_C = 50\text{ mA}$)	h_{FE}	70 to 350	
Gain-Bandwidth Product ($V_{CE} = 10\text{ V}$, $I_C = 50\text{ mA}$)	f_T	100	MHz
Thermal Resistance, Junction-to-Case	θ_{J-C}	35 max	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	175 max	$^{\circ}\text{C}/\text{W}$

POWER TRANSISTOR

40324



Si n-p-n type used in audio-amplifier inverter and driver stages for economical high-quality performance. Designed to assure freedom from second breakdown in the operating region. JEDEC TO-66, Outline No.25. See Mounting Hardware for desired mounting arrangement. For collector-characteristics and transfer-characteristics curves, refer to type 40310.

MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage	$V_{CEO}(\text{sus})$	35	V
Emitter-to-Base Voltage	V_{EBO}	2.5	V
Collector Current	I_C	4	A
Base Current	I_B	2	A
Transistor Dissipation:			
T_C up to 25°C	P_T	29	W
T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 200	$^{\circ}\text{C}$

CHARACTERISTICS (At case temperature = 25°C)

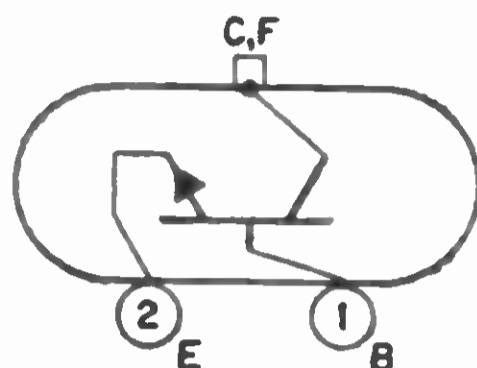
Collector-to-Emitter Breakdown Voltage ($I_C = 100\text{ mA}$, $R_{BE} = 500\ \Omega$)	$V_{(BR)CEO}$	35 min	V
Base-to-Emitter Voltage ($V_{CE} = 2\text{ V}$, $I_C = 1\text{ A}$)	V_{BE}	1.4 max	V

CHARACTERISTICS (cont'd)

Collector-Cutoff Current: V _{CB} = 15 V, I _E = 0, T _C = 25°C	I _{CBO}	10 max	μA
V _{CB} = 15 V, I _E = 0, T _C = 150°C	I _{CBO}	5 max	mA
Emitter-Cutoff Current (V _{EB} = 2.5 V, I _C = 0)	I _{EBO}	5 max	mA
Static Forward-Current Transfer Ratio (V _{CE} = 2 V, I _C = 1 A)	h _{FE}	20 to 120	
Gain-Bandwidth Product (V _{CE} = 4 V, I _C = 500 mA)	f _T	750	kHz
Thermal Resistance, Junction-to-Case	θ _{J-C}	6 max	°C/W

40325 POWER TRANSISTOR

Si n-p-n type used in audio-amplifier output stages for economical high-quality performance. Designed to assure freedom from second breakdown in the operating region. JEDEC TO-3, Outline No.2. See Mounting Hardware for desired mounting arrangement.

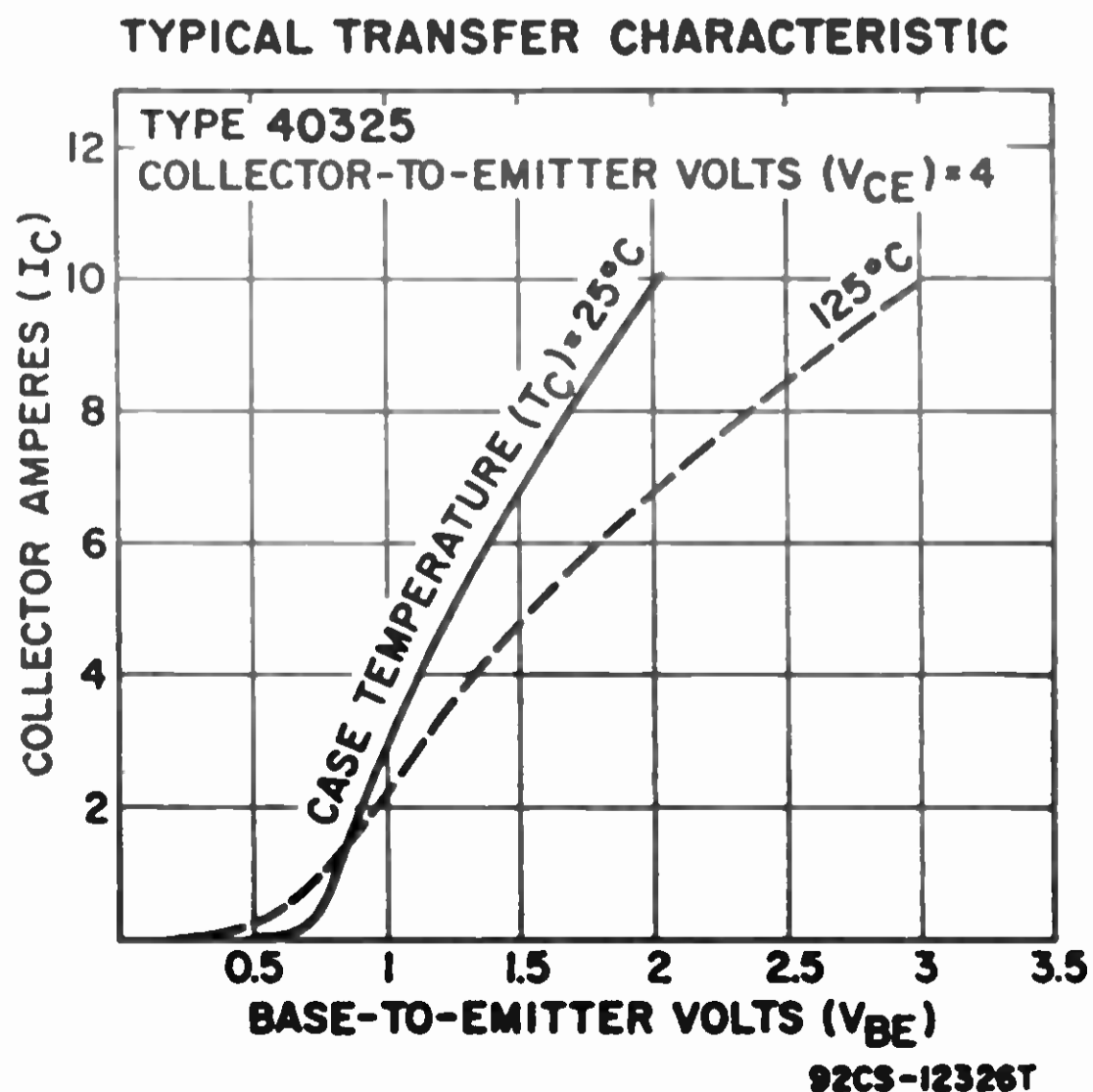
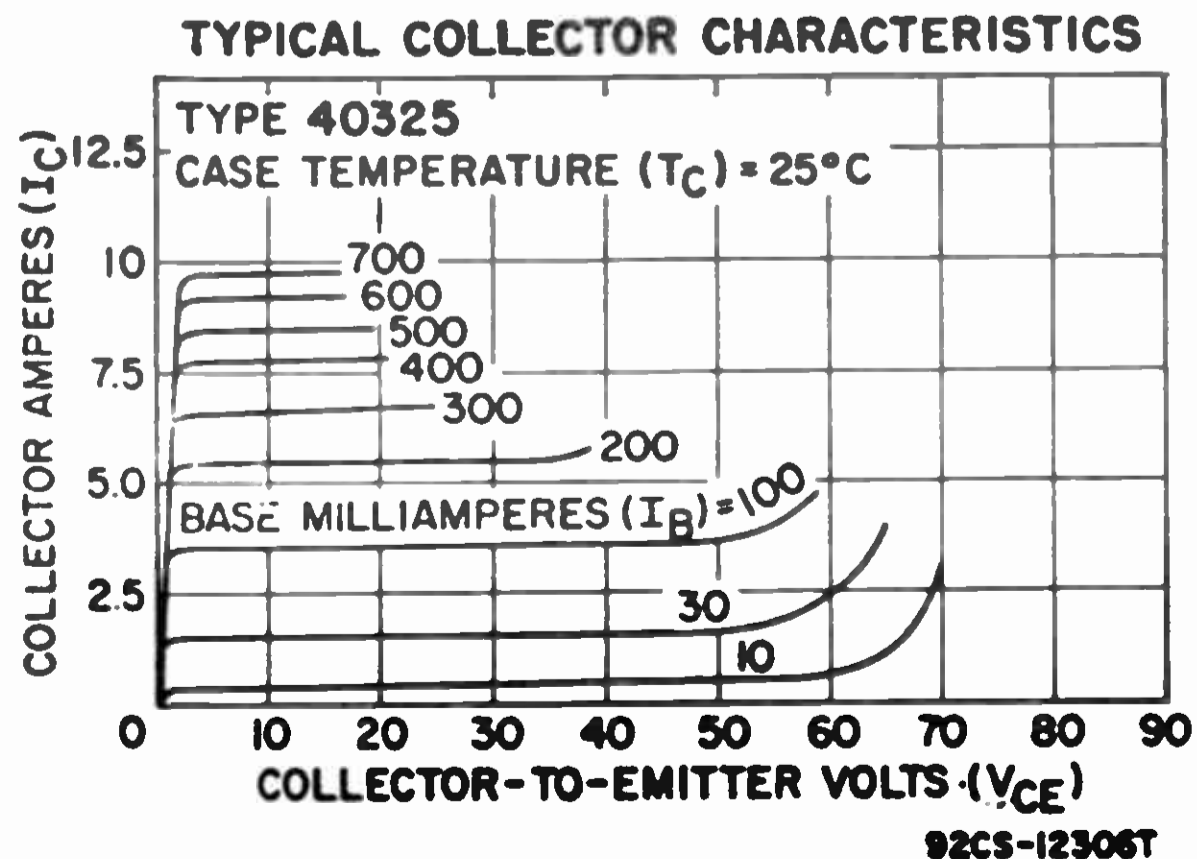


MAXIMUM RATINGS

Collector-to-Base Voltage	V _{CBO}	35	V
Collector-to-Emitter Voltage: V _{BE} = -1.5 V	V _{CEV}	35	V
Base open (sustaining voltage)	V _{CEO (SUS)}	35	V
Emitter-to-Base Voltage	V _{EBO}	5	V
Collector Current	I _C	15	A
Base Current	I _B	7	A
Transistor Dissipation: T _C up to 25°C	P _T	117	W
T _C above 25°C	P _T	See curve page 300	
Temperature Range: Operating (Junction)	T _{J (opr)}	-65 to 200	°C

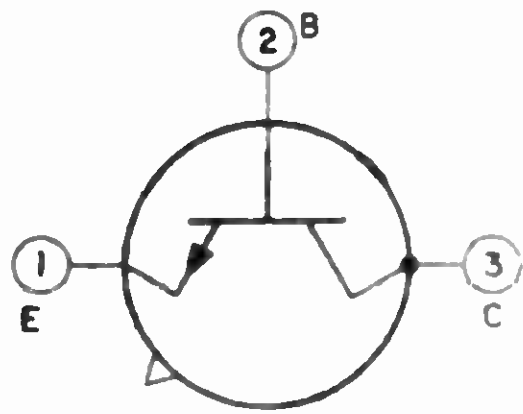
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Breakdown Voltage (I _C = 200 mA, I _B = 0)	V _{(BR)CEO (SUS)}	35 min	V
Collector-to-Base Breakdown Voltage (I _C = 100 mA, I _E = 0)	V _{(BR)CBO}	35 min	V
Collector-to-Emitter Saturation Voltage (I _C = 8 A, I _B = 0.8 A)	V _{CE (sat)}	1.5 max	V
Base-to-Emitter Voltage (V _{CE} = 4 V, I _C = 8 A)	V _{BE}	2 max	V
Collector-Cutoff Current: V _{CB} = 30 V, I _E = 0, T _C = 25°C	I _{CBO}	5 max	
V _{CB} = 30 V, I _E = 0, T _C = 150°C	I _{CBO}	10 max	
Emitter-Cutoff Current (V _{EB} = 5 V, I _C = 0)	I _{EBO}	10 max	°C/W
Static Forward-Current Transfer Ratio (V _{CE} = 4 V, I _C = 8 A)	h _{FE}	12 to 60	mA
Thermal Resistance, Junction-to-Case	θ _{J-C}	1.5 max	mA



POWER TRANSISTOR

40326



Si n-p-n type used in audio-amplifier inverter and driver stages for economical high-quality performance. Designed to assure freedom from second breakdown in the operating region. JEDEC TO-5, Outline No.5. For collector-characteristics curves, refer to type 40309.

MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage	$V_{CEO(sus)}$	40	V
Emitter-to-Base Voltage	V_{EBO}	2.5	V
Collector Current	I_C	0.7	A
Base Current	I_B	0.2	A
Transistor Dissipation:			
T_A up to 25°C	P_T	1	W
T_C up to 25°C	P_T	5	W
T_A and T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 200	°C

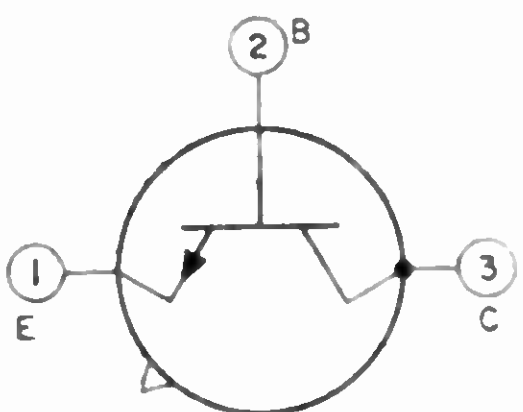
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_C = 100\text{ mA}$, $I_B = 0$, $t_p = 300\ \mu s$, $df \leq 2\%$)	$V_{CEO(sus)}$	40 min	V
Base-to-Emitter Voltage ($V_{CE} = 4\text{ V}$, $I_C = 10\text{ mA}$) ...	V_{BE}	1 max	V
Collector-Cutoff Current:			
$V_{CB} = 15\text{ V}$, $I_E = 0$, $T_C = 25^\circ C$	I_{CBO}	0.25 max	μA
$V_{CB} = 15\text{ V}$, $I_E = 0$, $T_C = 150^\circ C$	I_{CBO}	1 max	mA
Emitter-Cutoff Current ($V_{EB} = 2.5\text{ V}$, $I_C = 0$)	I_{EBO}	1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 4\text{ V}$, $I_C = 10\text{ mA}$)	h_{FE}	40 to 200	
Thermal Resistance, Junction-to-Case	θ_{J-C}	30 max	°C/W

6980270

POWER TRANSISTOR

40327



Si n-p-n high-voltage type used for direct operation from a line source in audio-amplifier driver stages for economical high-quality performance. Designed to assure freedom from second breakdown in the operating region. JEDEC TO-5, Outline No.5. For collector-characteristics and input-characteristics curves, refer to

type 40321.

MAXIMUM RATINGS

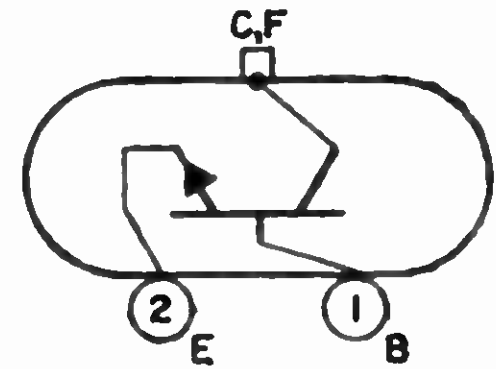
Collector-to-Emitter Sustaining Voltage ($R_{BE} = 1000\ \Omega$)	$V_{CER(sus)}$	300	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	1	A
Base Current	I_B	0.5	A
Transistor Dissipation:			
T_A up to 50°C	P_T	1	W
T_C up to 50°C	P_T	5	W
T_A and T_C above 50°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 200	°C

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_C = 50\text{ mA}$, $R_{BE} = 1000\ \Omega$)	$V_{CER(sus)}$	300 min	V
Base-to-Emitter Voltage ($V_{CE} = 10\text{ V}$, $I_C = 50\text{ mA}$)	V_{BE}	2 max	V
Collector-Cutoff Current:			
$V_{CB} = 150\text{ V}$, $T_C = 150^\circ C$, $I_E = 0$	I_{CBO}	100 max	μA
$V_{CE} = 150\text{ V}$, $R_{BE} = 1000\ \Omega$	I_{CER}	5 max	μA
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$, $I_C = 0$)	I_{EBO}	100 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 10\text{ V}$, $I_C = 20\text{ mA}$)	h_{FE}	40 to 250	
Thermal Resistance, Junction-to-Case	θ_{J-C}	30 max	°C/W

40328 POWER TRANSISTOR

Si n-p-n high-voltage type used for direct operation from a line source in audio-amplifier output stages for economical high-quality performance. Designed to assure freedom from second breakdown in the operating region. JEDEC TO-66, Outline No.25. See **Mounting Hardware** for desired mounting arrangement. For rating chart and collector-characteristics curves, refer to type 40318.



MAXIMUM RATINGS

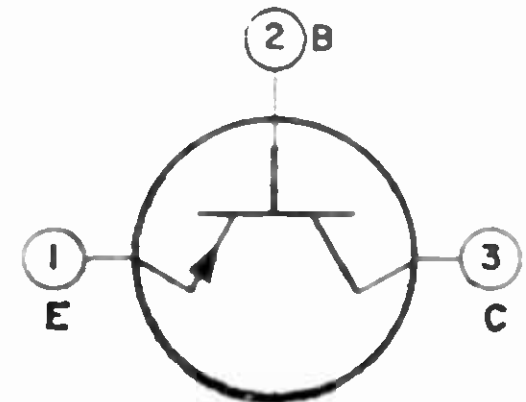
Collector-to-Emitter Sustaining Voltage ($R_{BE} = 500 \Omega$)	$V_{CER(SUS)}$	300	V
Emitter-to-Base Voltage	V_{EBO}	6	V
Collector Current	I_C	2	A
Base Current	I_B	1	A
Transistor Dissipation:			
T_c up to $25^\circ C$	P_T	35	W
T_c above $25^\circ C$	P_T	See Rating Chart	W
$T_c = 175^\circ C$	P_T	5	W
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 200	$^\circ C$

CHARACTERISTICS (At case temperature = $25^\circ C$)

Collector-to-Emitter Sustaining Voltage ($I_C = 200 \text{ mA}$, $R_{BE} = 500 \Omega$)	$V_{CER(SUS)}$	300 min	V
Base-to-Emitter Voltage ($V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$)	V_{BE}	1.5 max	V
Collector-Cutoff Current:			
$V_{CE} = 150 \text{ V}$, $I_B = 0$	I_{CEO}	5 max	mA
$V_{CE} = 150 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_c = 25^\circ C$	I_{CEV}	10 max	mA
$V_{CE} = 150 \text{ V}$, $V_{BE} = -1.5 \text{ V}$, $T_c = 150^\circ C$	I_{CEV}	10 max	mA
Emitter-Cutoff Current ($V_{EB} = 6 \text{ V}$, $I_C = 0$)	I_{EBO}	5 max	mA
Static Forward-Current Transfer Ratio:			
$V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ A}$	h_{FE}	20 min	
$V_{CE} = 10 \text{ V}$, $I_C = 20 \text{ mA}$	h_{FE}	40 min	
Second-Breakdown Collector Current ($V_{CE} = 150 \text{ V}$)	$I_{S/b}$	100 min	mA
Thermal Resistance, Junction-to-Case	θ_{J-C}	5 max	$^\circ C/W$

40329 TRANSISTOR

Ge p-n-p alloy type for low-level, intermediate-level, and class A driver stages in consumer and industrial af-amplifier equipment such as preamplifiers, tone-control stages, and phonograph amplifiers using crystal pickups. JEDEC TO-1, Outline No.1.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-25	V
Collector-to-Emitter Voltage ($R_{BE} \leq 4700 \Omega$)	V_{CER}	-25	V
Emitter-to-Base Voltage	V_{EBO}	-2.5	V
Collector Current	I_C	-100	mA
Emitter Current	I_E	100	mA
Base Current	I_B	-20	mA
Transistor Dissipation:			
T_A up to $55^\circ C$ (With infinite heat sink)	P_T	375	mW
T_A up to $55^\circ C$ (With practical heat sink, $\theta = 50^\circ C/W$)	P_T	265	mW
T_A up to $55^\circ C$ (Without heat sink)	P_T	125	mW
T_A with and without heat sink above $55^\circ C$	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 100	$^\circ C$
Storage	T_{STG}	-65 to 100	$^\circ C$
Lead-Soldering Temperature (10 s max)	T_L	255	$^\circ C$

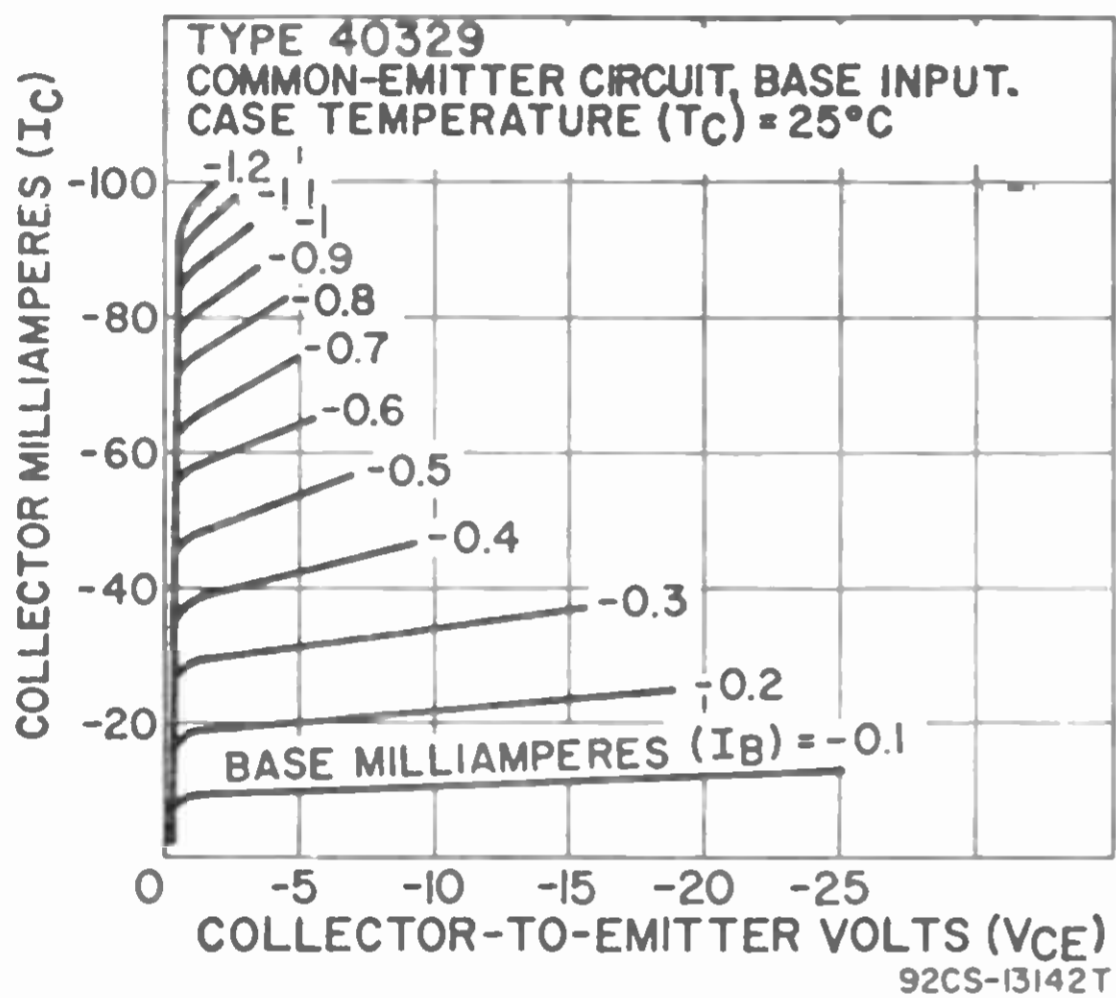
CHARACTERISTICS (At case temperature = $25^\circ C$)

Collector-to-Base Breakdown Voltage ($I_C = -0.05 \text{ mA}$, $I_E = 0$)	$V_{(BR)CBO}$	-25 min	V
Collector-to-Emitter Breakdown Voltage ($R_{BE} = 4700 \Omega$, $I_C = -1 \text{ mA}$)	$V_{(BR)CER}$	-25 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -0.05 \text{ mA}$)	$V_{(BR)EBO}$	-2.5 min	V

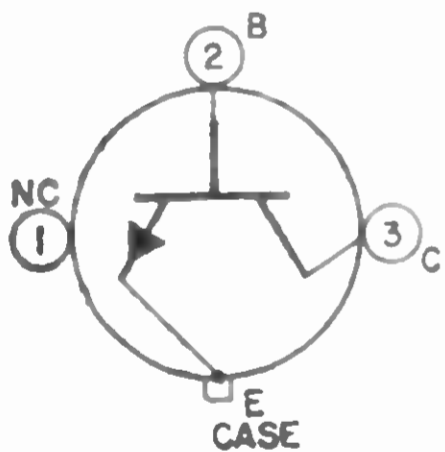
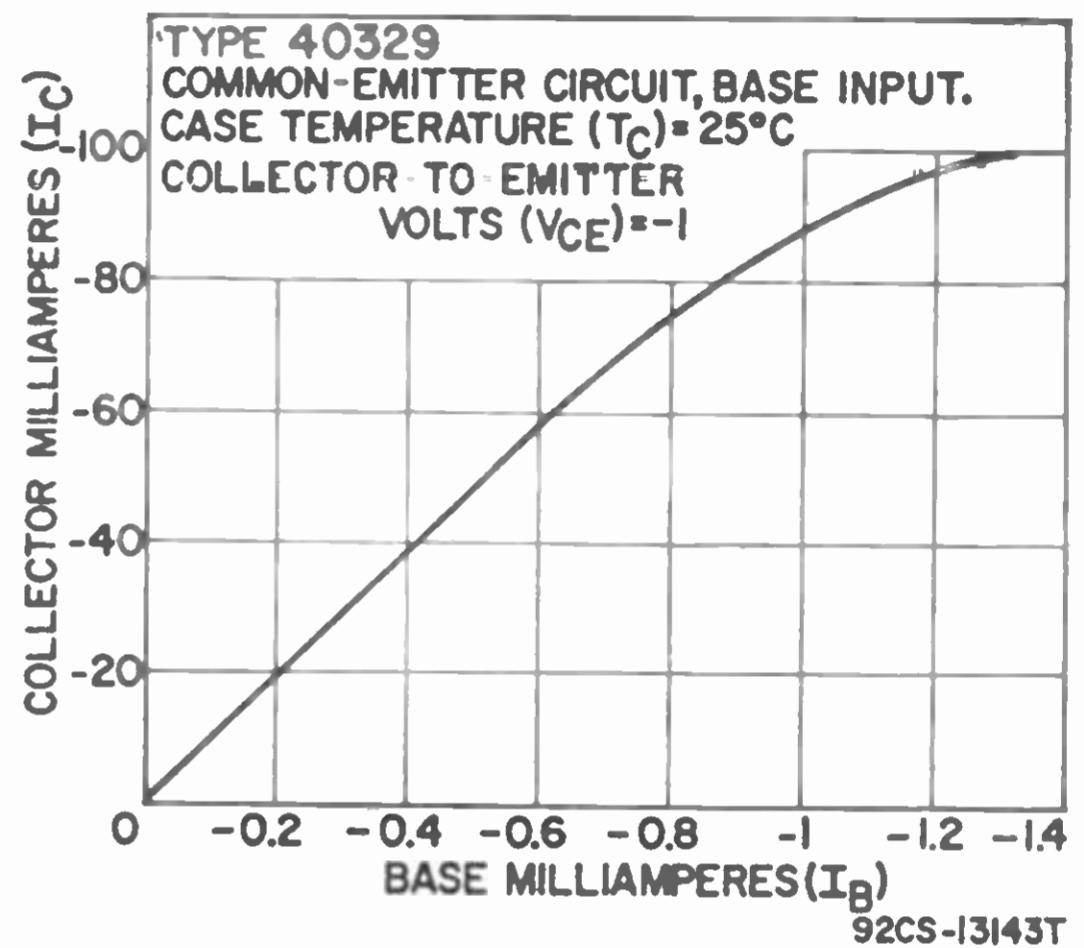
CHARACTERISTICS (cont'd)

Collector-Cutoff Current ($V_{CB} = -12\text{ V}, I_E = 0$)	I_{CBO}	-14 max	μA
Emitter-Cutoff Current ($V_{EB} = -2\text{ V}, I_C = 0$)	I_{EBO}	-14 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = -1\text{ V}, I_C = -25\text{ mA}$)	h_{FE}	50 to 200	
Small-Signal Forward-Current Transfer Ratio: $V_{CE} = -10\text{ V}, I_C = -10\text{ mA}, f = 1\text{ kHz}$	h_{fe}	75 to 300	
$V_{CE} = -1\text{ V}, I_C = -1\text{ mA}, f = 1\text{ kHz}$	h_{fe}	50 to 200	
Small-Signal Forward-Current Transfer Ratio Cutoff Frequency ($V_{CB} = -6\text{ V}, I_C = 1\text{ mA}$)	f_{hfb}	1.5	MHz
Output Capacitance ($V_{CB} = -6\text{ V}, f = 1\text{ kHz}$)	C_{obo}	35	pF
Small-Signal Input Impedance ($V_{CE} = -10\text{ V}, I_C = -10\text{ mA}, f = 1\text{ kHz}$)	h_{ie}	400	Ω
Small-Signal Output Admittance ($V_{CE} = -10\text{ V}, I_C = -10\text{ mA}, f = 1\text{ kHz}$)	h_{oe}	175	μmhos
Small-Signal Reverse Voltage-Transfer Ratio ($V_{CE} = -10\text{ V}, I_C = -10\text{ mA}, f = 1\text{ kHz}$)	h_{re}	300×10^{-6}	
Equivalent RMS Noise Input Current ($V_{CE} = -6\text{ V}, I_C = -0.5\text{ mA}, f = 20\text{ Hz to } 20\text{ kHz}$)		0.02 max	μA
Intrinsic Base-Spreading Resistance ($V_{CE} = -6\text{ V}, I_C = -1\text{ mA}, f = 20\text{ MHz}$)	$r_{bb'}$	100	Ω

TYPICAL COLLECTOR CHARACTERISTICS



TYPICAL TRANSFER CHARACTERISTIC



TRANSISTOR

40340

Si n-p-n "overlay" epitaxial planar type used in high-power class C amplifier applications at frequencies to 100 MHz. JEDEC TO-60, Outline No.23. See Mounting Hardware for desired mounting arrangement.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	60	V
Collector-to-Emitter Voltage: $V_{BE} = -1.5\text{ V}$	V_{CEV}	60	V
Base open	V_{CEO}	25	V
Emitter-to-Base Voltage	V_{EBO}	4	V
Peak Collector Current	$i_c(\text{peak})$	10	A
Continuous Collector Current	I_C	3.3	A
Transistor Dissipation ($T_C = 25^\circ\text{C}$)	P_T	70	W
Temperature Range: Operating (Junction)	$T_J(\text{opr})$	200	$^\circ\text{C}$

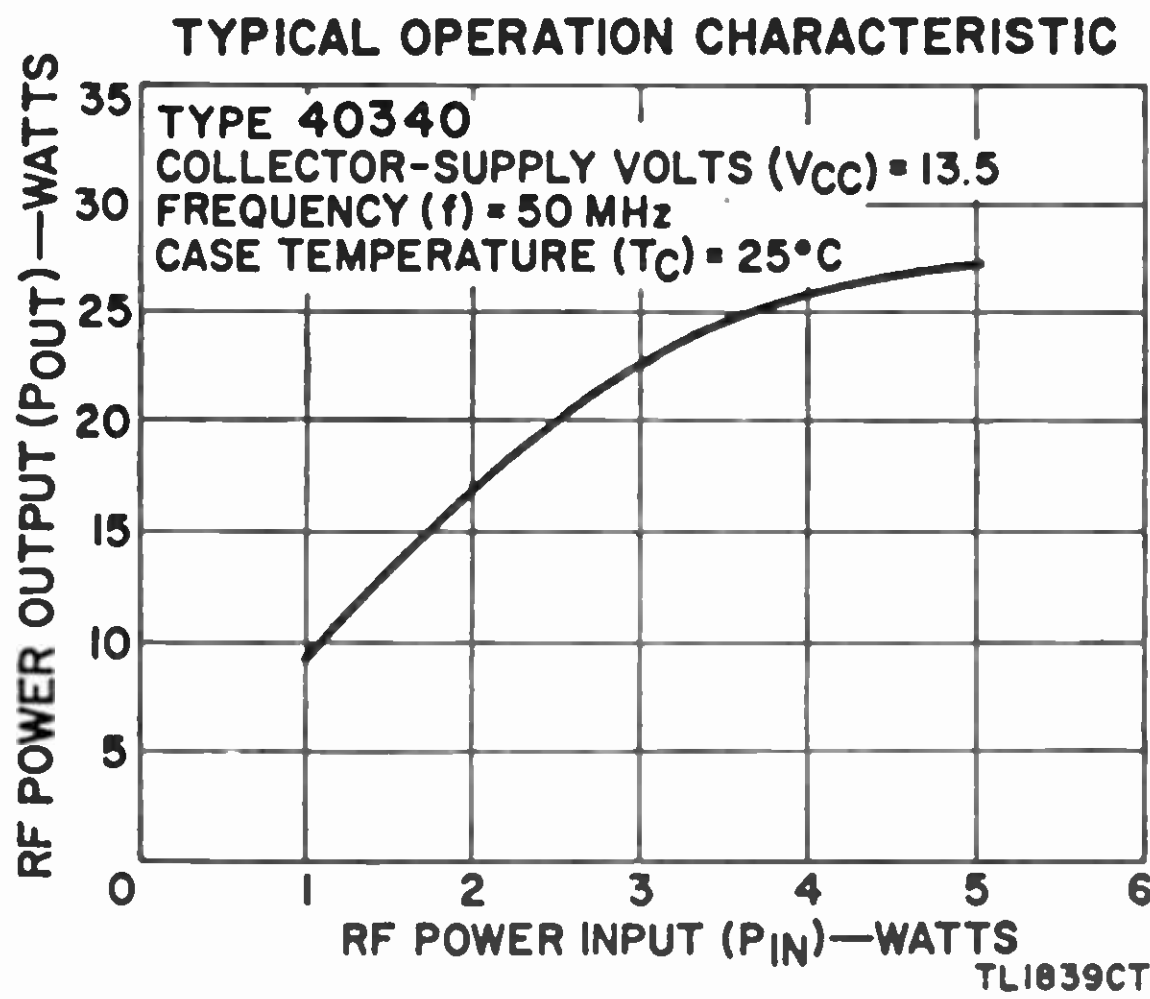
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Breakdown Voltage: $I_C = 200\text{ mA}, V_{BE} = -1.5\text{ V}$, pulsed through an inductor $L = 25\text{ mH}, df = 50\%$	$V_{(BR)CEV}$	60 min	V
$I_C = 200\text{ mA}, I_B = 0$, pulsed through an inductor $L = 25\text{ mH}, df = 50\%$	$V_{(BR)CEO}$	25 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 10\text{ mA}, I_C = 0$)	$V_{(BR)EBO}$	4 min	V
Collector-Cutoff Current: $V_{CE} = 15\text{ V}, I_B = 0$	I_{CEO}	1 max	mA
$V_{CB} = 40\text{ V}, I_E = 0$	I_{CBO}	10 max	mA

MAXIMUM RATINGS (cont'd)

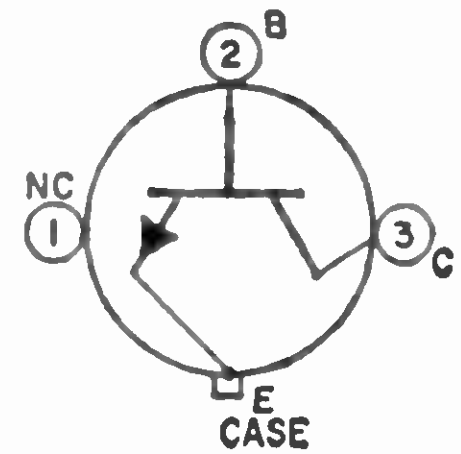
Output Capacitance ($V_{CB} = 15\text{ V}$, $I_E = 0$)	C_{obo}	120 max	pF
RF Power Output ($V_{CE} = 13.5\text{ V}$, $P_{IE} = 5\text{ W}$, $f = 50\text{ MHz}$, R_G and $R_L = 50\ \Omega$)	P_{oE}	25* min	W
Thermal Resistance, Junction-to-Case	θ_{J-C}	2.5 max	$^{\circ}\text{C/W}$

* For conditions given, minimum efficiency = 65 per cent.



40341 TRANSISTOR

Si n-p-n "overlay" epitaxial planar type used in high-power class C amplifier applications at frequencies to 100 MHz. JEDEC TO-60, Outline No.23. See Mounting Hardware for desired mounting arrangement. This type is identical with type 40340 except for the following items:

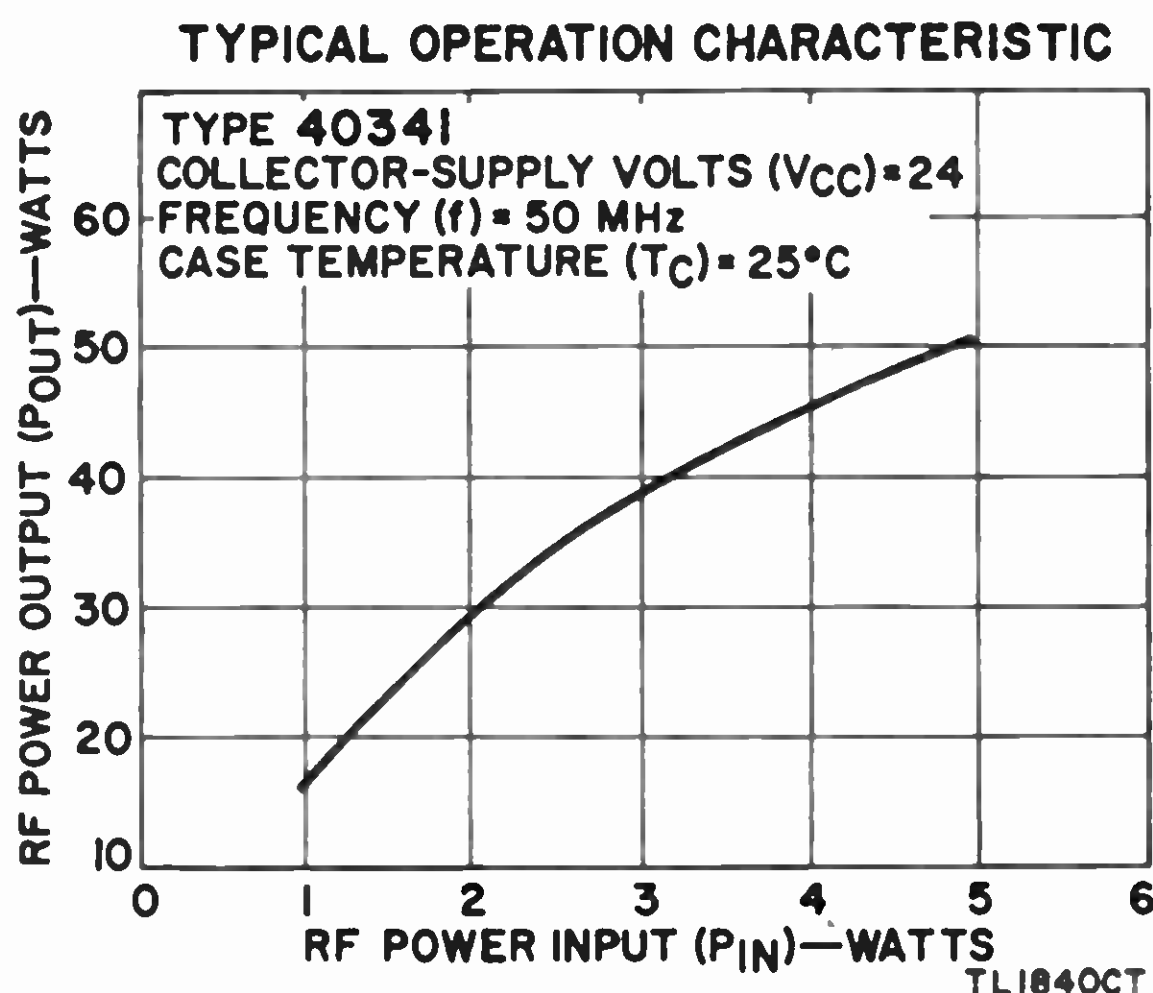


MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	70	V
Collector-to-Emitter Voltage: $V_{BE} = -1.5\text{ V}$	V_{CEV}	70	V
Base open	V_{CEO}	35	V

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Breakdown Voltage: $I_C = 200\text{ mA}$, $V_{BE} = -1.5\text{ V}$, pulsed through an inductor $L = 25\text{ mH}$, $df = 50\%$	$V_{(BR)CEV}$	70 min	V
$I_C = 200\text{ mA}$, $I_B = 0$, pulsed through an inductor $L = 25\text{ mH}$, $df = 50\%$	$V_{(BR)CEO}$	35 min	V
Collector-Cutoff Current: $V_{CE} = 30\text{ V}$, $I_B = 0$	I_{CEO}	1 max	mA
$V_{CB} = 50\text{ V}$, $I_E = 0$	I_{CBO}	10 max	mA



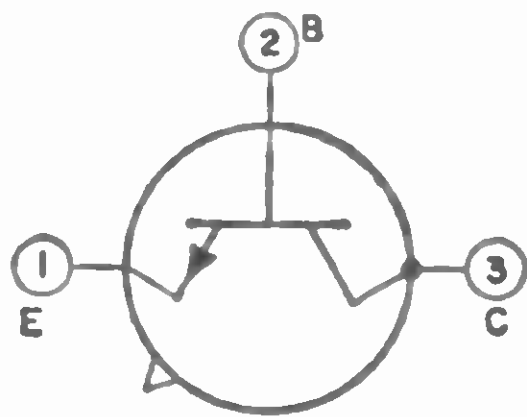
CHARACTERISTICS (cont'd)

Output Capacitance ($V_{CB} = 30\text{ V}$, $I_E = 0$)	C_{obo}	85 max	pF
RF Power Output ($V_{CE} = 24\text{ V}$, $P_{iB} = 3\text{ W}$, $f = 50\text{ MHz}$, R_G and $R_L = 50\ \Omega$)	P_{oB}	30* min	W

* For conditions given, minimum efficiency = 60 per cent.

POWER TRANSISTOR

40346



Si n-p-n triple-diffused planar type used in low-power, high-voltage, general-purpose applications in military, industrial, and commercial equipment. This type is particularly useful in neon-indicator driver circuits and in high-voltage differential and high-voltage operational amplifiers. JEDEC TO-5, Outline No.5.

MAXIMUM RATINGS

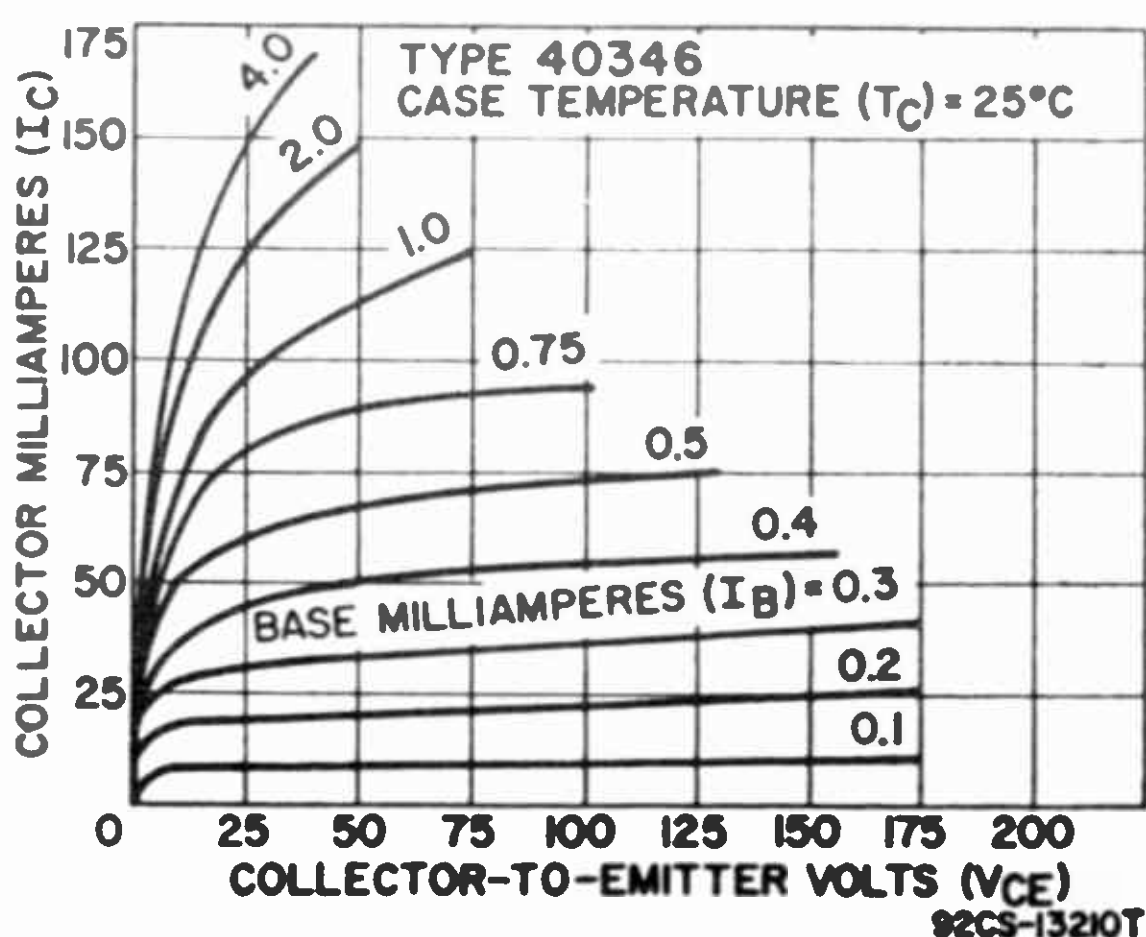
Collector-to-Emitter Voltage ($R_{BE} = 1000\ \Omega$)	$V_{CER(sus)}$	175	V
Collector Current	I_C	1	A
Base Current	I_B	0.5	A
Transistor Dissipation:			
T_A up to 50°C	P_T	1*	W
T_C up to 25°C	P_T	10*	W
T_A and T_C above 50°C	P_T	See curve page 300	
Temperature Range:			
Operating (T_A - T_C)		-65 to 200	$^\circ\text{C}$

CHARACTERISTICS (At case temperature = 25°C)

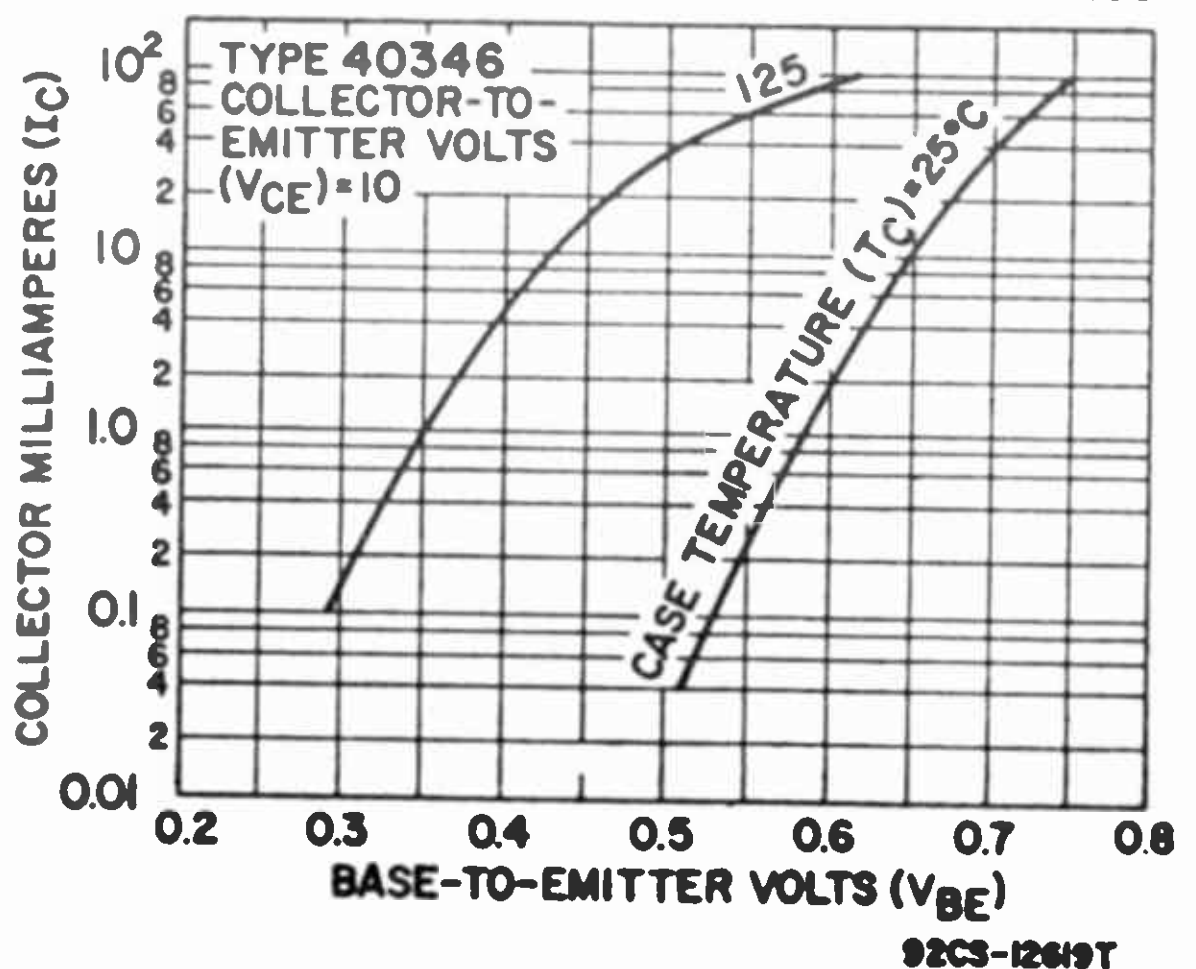
Collector-to-Emitter Sustaining Voltage ($R_{BE} = 1000\ \Omega$, $I_C = 50\text{ mA}$)	$V_{CER(sus)}$	175 min	V
Collector-to-Emitter Saturation Voltage ($I_B = 1\text{ mA}$, $I_C = 10\text{ mA}$)	$V_{CE(sat)}$	0.5 max	V
Base-to-Emitter Voltage ($V_{CB} = 10\text{ V}$, $I_C = 10\text{ mA}$)	V_{BE}	1 max	V
Collector-Cutoff Current:			
$V_{CE} = 100\text{ V}$, $I_B = 0$	I_{CEO}	5 max	μA
$V_{CE} = 200\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 25^\circ\text{C}$	I_{CEV}	10 max	μA
$V_{CE} = 200\text{ V}$, $V_{BE} = -1.5\text{ V}$, $T_C = 150^\circ\text{C}$	I_{CEV}	1 max	mA
Emitter-Cutoff Current ($V_{EB} = 4\text{ V}$, $I_C = 0$)	I_{EBO}	5 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 10\text{ V}$, $I_C = 10\text{ mA}$)	h_{FE}	25 min	
Small-Signal, Forward-Current Transfer Ratio ($V_{CE} = 10\text{ V}$, $I_C = 10\text{ mA}$, $f = 5\text{ MHz}$)	h_{fe}	2 min	
Thermal Resistance, Junction-to-Case	θ_{J-C}	15* max	$^\circ\text{C/W}$

* This value does not apply to type 40346V1.

TYPICAL COLLECTOR CHARACTERISTICS



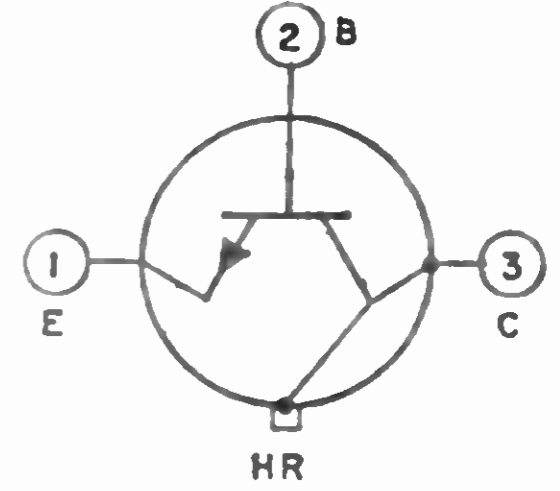
TYPICAL TRANSFER CHARACTERISTICS



40346V1

TRANSISTOR

Si n-p-n triple-diffused type used in high-voltage switching and linear-amplifier applications in military and commercial applications. This type is particularly useful in neon-indicator driver circuits and in differential and operational amplifiers. JEDEC TO-5 (with heat radiator), Outline No.8. This type is identical to type 40346 except for the following items:



MAXIMUM RATINGS

Transistor Dissipation:			
T_A up to 25°C	P_T	4	W

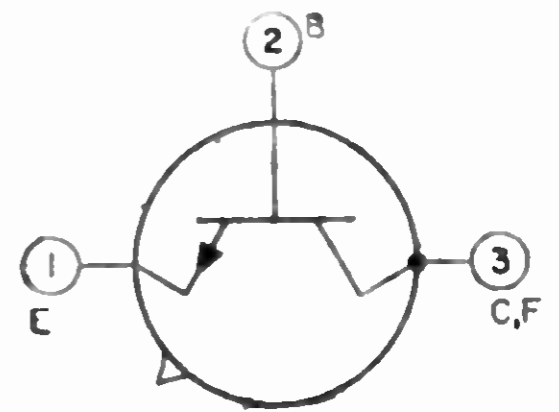
CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient	θ_{J-A}	45 max	°C/W
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40346V2

TRANSISTOR

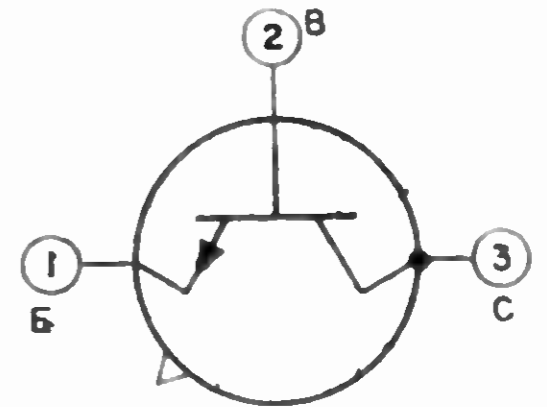
Si n-p-n triple-diffused type used in high-voltage switching and linear-amplifier applications in military and commercial applications. This type is particularly useful in neon-indicator driver circuits and in differential and operational amplifiers. JEDEC TO-5 (with flange), Outline No.6. See Mounting Hardware for desired mounting arrangement. This type is electrically identical with type 40346.



40347

POWER TRANSISTOR

Si n-p-n single-diffused type featuring a base comprised of a homogeneous-resistivity silicon material. This type is used in a wide variety of low- and medium-power applications where medium- and high-voltage power transistors are required, such as switching regulators, converters, inverters, relay controls, oscillators, and pulse and audio amplifiers. JEDEC TO-5, Outline No.5.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	60	V
Collector-to-Emitter Voltage:			
$V_{BE} = -1.5$ V	V_{CEV}	60	V
Base open	V_{CEO}	40	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Collector Current	I_C	1.5	A
Peak Collector Current	i_C	3	A
Base Current	I_B	0.5	A
Transistor Dissipation:			
T_A up to 25°C	P_T	1	W
T_C up to 25°C	P_T	8.75	W
T_A and T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	230	°C

CHARACTERISTICS (At case temperature = 25°C)

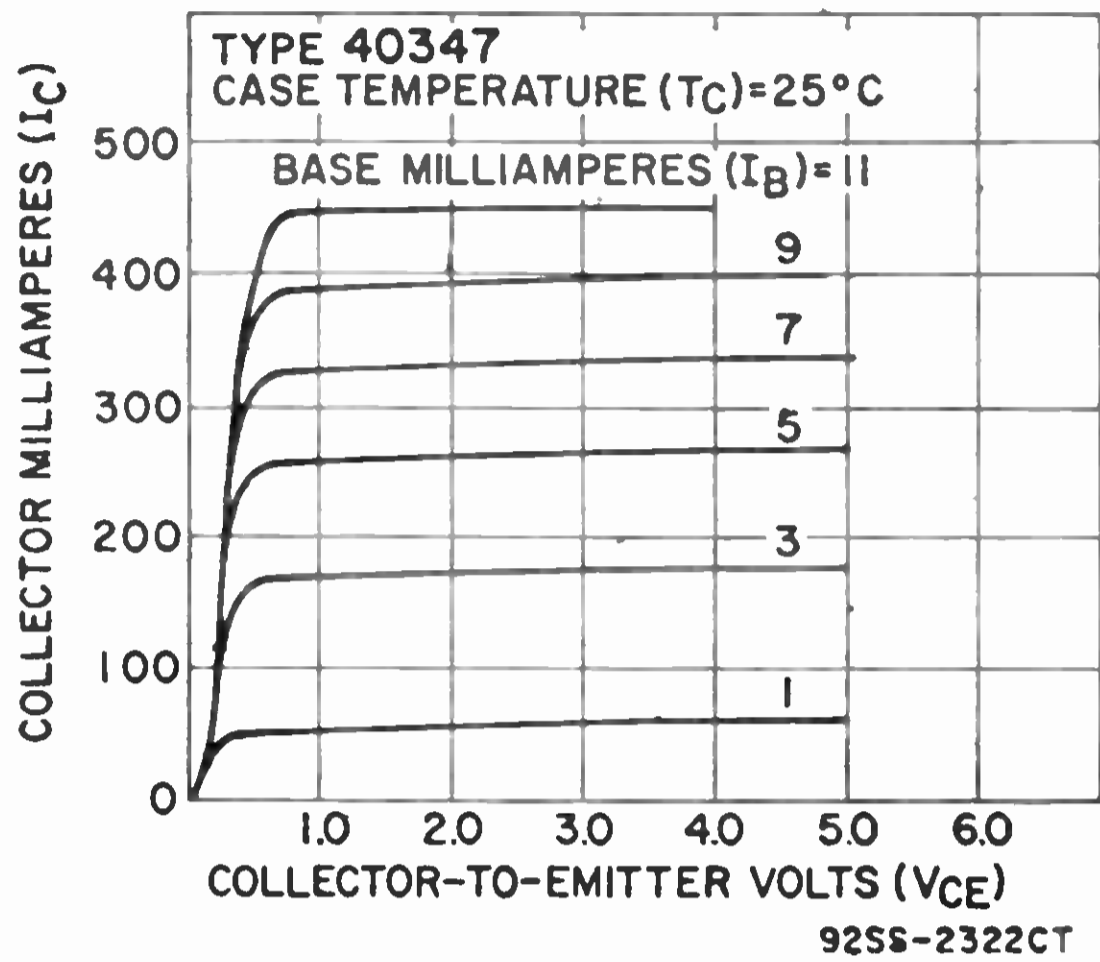
Collector-to-Emitter Sustaining Voltage:			
$V_{BE} = -1.5$ V, $I_C = 50$ mA	V_{CEV} (sus)	60 min	V
$I_C = 50$ mA, $I_B = 0$	V_{CEO} (sus)	40 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 450$ mA, $I_B = 45$ mA)	V_{CE} (sat)	1 max	V
Base-to-Emitter Voltage ($V_{CE} = 4$ V, $I_C = 450$ mA)	V_{BE}	1.5 max	V

CHARACTERISTICS (cont'd)

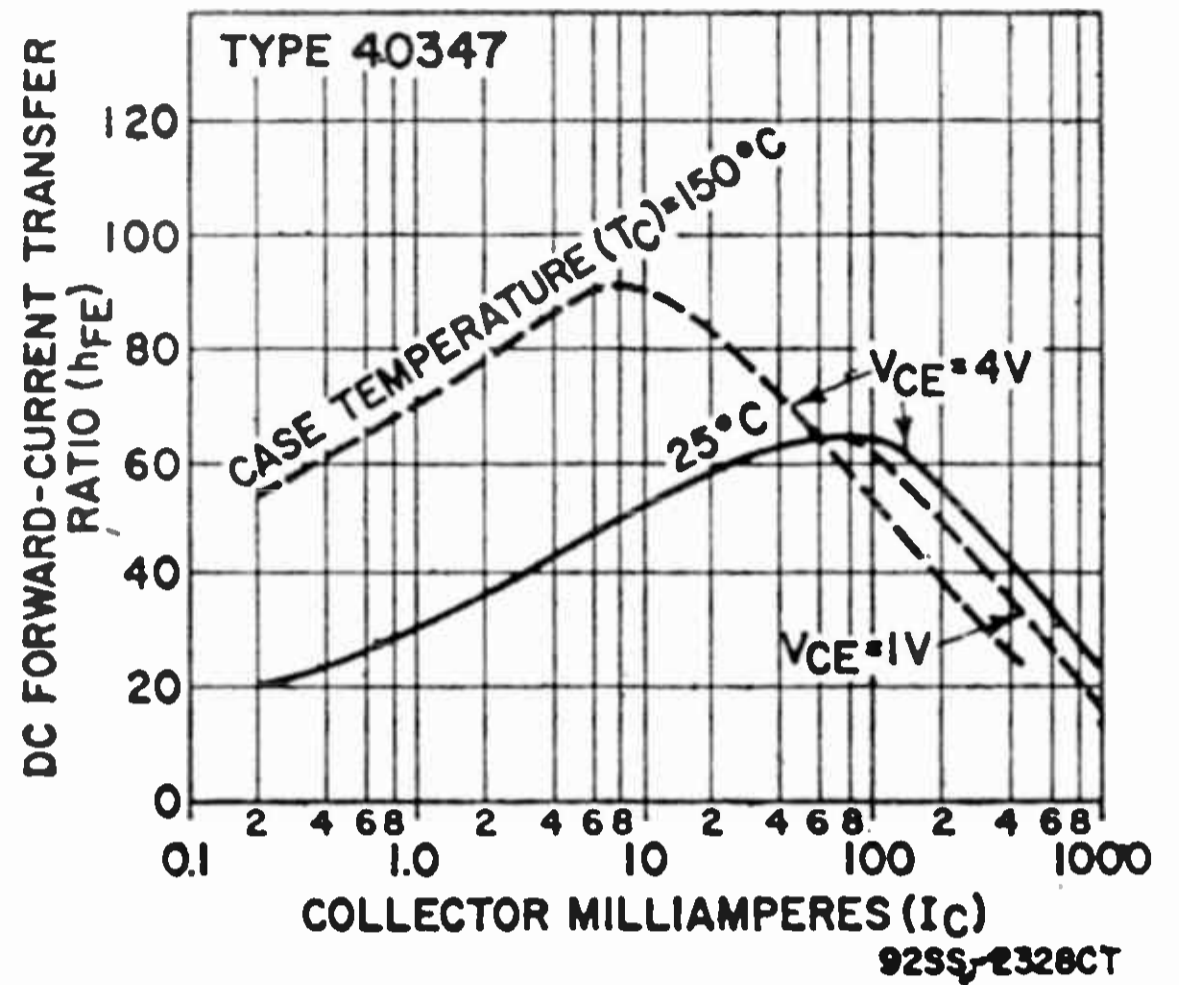
Collector-Cutoff Current:

$V_{CE} = 30\text{ V}, R_{BE} = 1\text{ k}\Omega, T_C = 25^\circ\text{C}$	I_{CER}	1 max	μA
$V_{CE} = 30\text{ V}, R_{BE} = 1\text{ k}\Omega, T_C = 150^\circ\text{C}$	I_{CER}	1 max	mA
Emitter-Cutoff Current ($V_{EB} = 7\text{ V}, I_C = 0$)	I_{EBO}	10 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 4\text{ V}, I_C = 450\text{ mA}$)	h_{FE}	25 to 100	
Thermal Resistance, Junction-to-Case	Θ_{J-C}	20 max	$^\circ\text{C/W}$

TYPICAL COLLECTOR CHARACTERISTICS

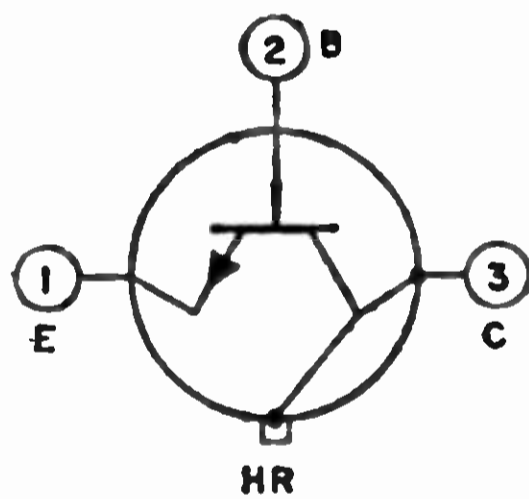


TYPICAL DC FORWARD-CURRENT TRANSFER-RATIO CHARACTERISTICS



POWER TRANSISTOR

40347V1



Si n-p-n single-diffused type featuring a base comprised of a homogeneous-resistivity silicon material. This type has an attached heat radiator for printed-circuit-board use in a wide variety of low- and medium-power applications requiring medium- and high-voltage power transistors for switching regulators, converters, inverters, relay controls, oscillators, and pulse and audio amplifiers. JEDEC TO-5 (with heat radiator), Outline No.8. This type is identical with type 40347 except for the following items:

MAXIMUM RATINGS

Transistor Dissipation:

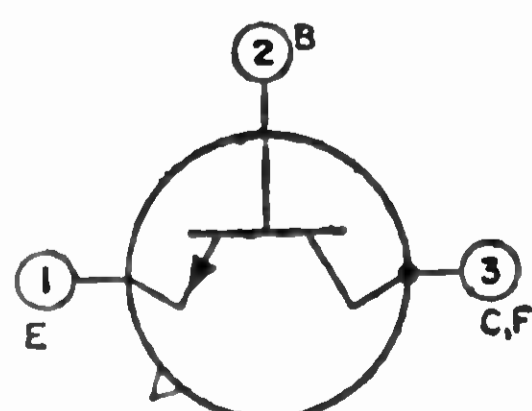
T_A up to 25°C	P_T	4.4	W
T_A above 25°C	P_T	See curve page 300	

CHARACTERISTICS (At case temperature = 25°C)

Thermal Resistance, Junction-to-Ambient	Θ_{J-A}	40 max	$^\circ\text{C/W}$
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POWER TRANSISTOR

40347V2



Si n-p-n single-diffused type featuring a base comprised of a homogeneous-resistivity silicon material. This type is used in a wide variety of low- and medium-power applications requiring medium- and high-voltage power transistors for switching regulators, converters, inverters, relay controls, oscillators, and pulse and audio amplifiers. JEDEC TO-5 (with flange), Outline No.6. See Mounting Hardware for desired mounting arrangement. This type is identical with type 40347 except for the following items:

MAXIMUM RATINGS

Transistor Dissipation:

T_c up to 25°C	P_T	11.7	W
T_c above 25°C	P_T	See curve page 300	

CHARACTERISTICS (At case temperature = 25°C)

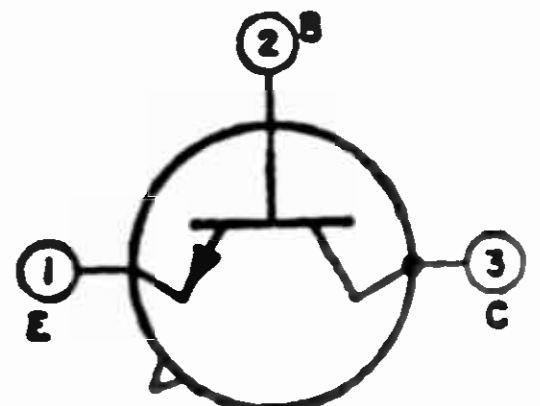
Thermal Resistance, Junction-to-Case	θ_{J-C}	15 max	°C/W
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5000673

40348

POWER TRANSISTOR

Si n-p-n single-diffused type featuring a base comprised of a homogeneous-resistivity silicon material. This type is used in a wide variety of low- and medium-power applications where medium- and high-voltage power transistors are required, such as switching regulators, converters, inverters, relay controls, oscillators, and pulse and audio amplifiers. JEDEC TO-5, Outline No.5.



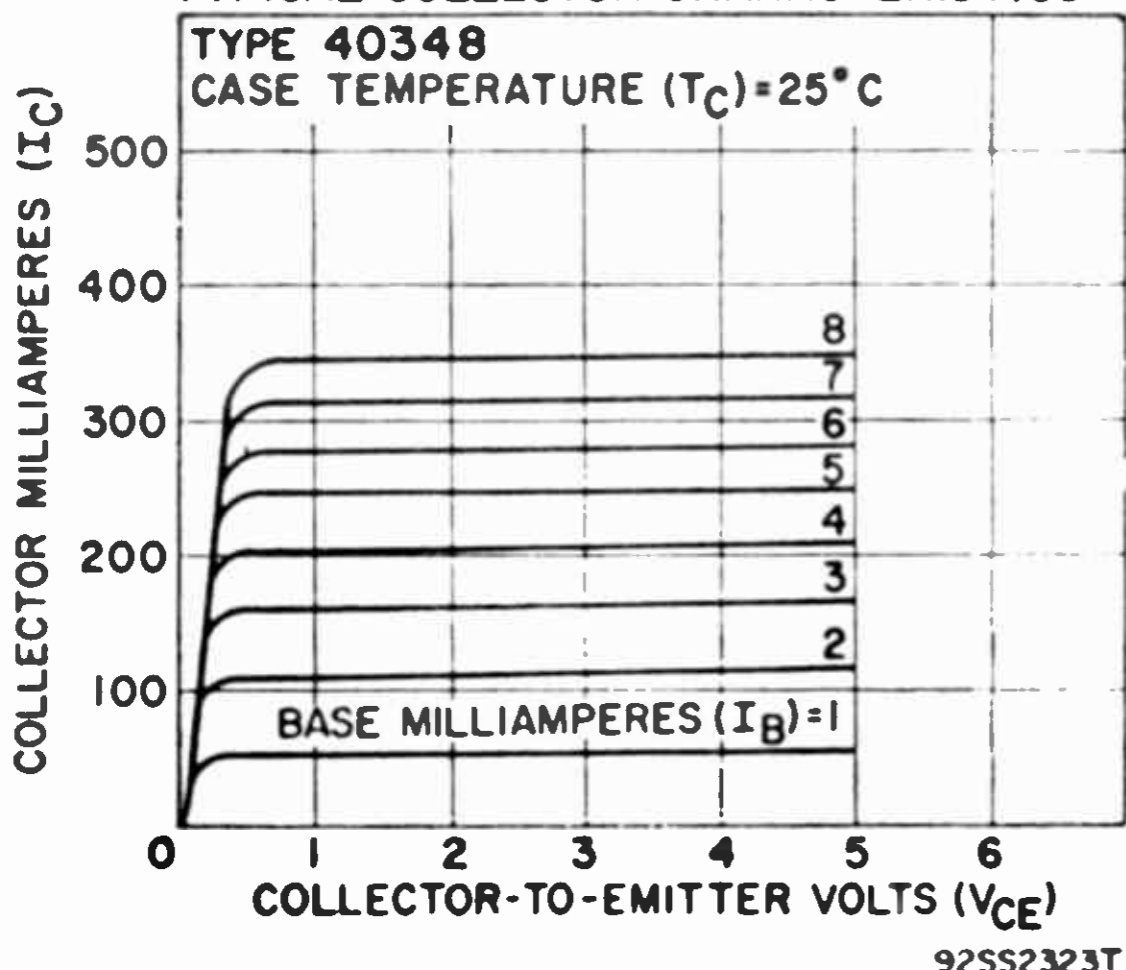
MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	90	V
Collector-to-Emitter Voltage:			
$V_{BE} = -1.5$ V	V_{CEV}	90	V
Base open	V_{CEO}	65	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Peak Collector Current	i_C	3	A
Collector Current	I_C	1.5	A
Base Current	I_B	0.5	A
Transistor Dissipation:			
T_A up to 25°C	P_T	1	W
T_c up to 25°C	P_T	8.75	W
T_A and T_c above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	230	°C

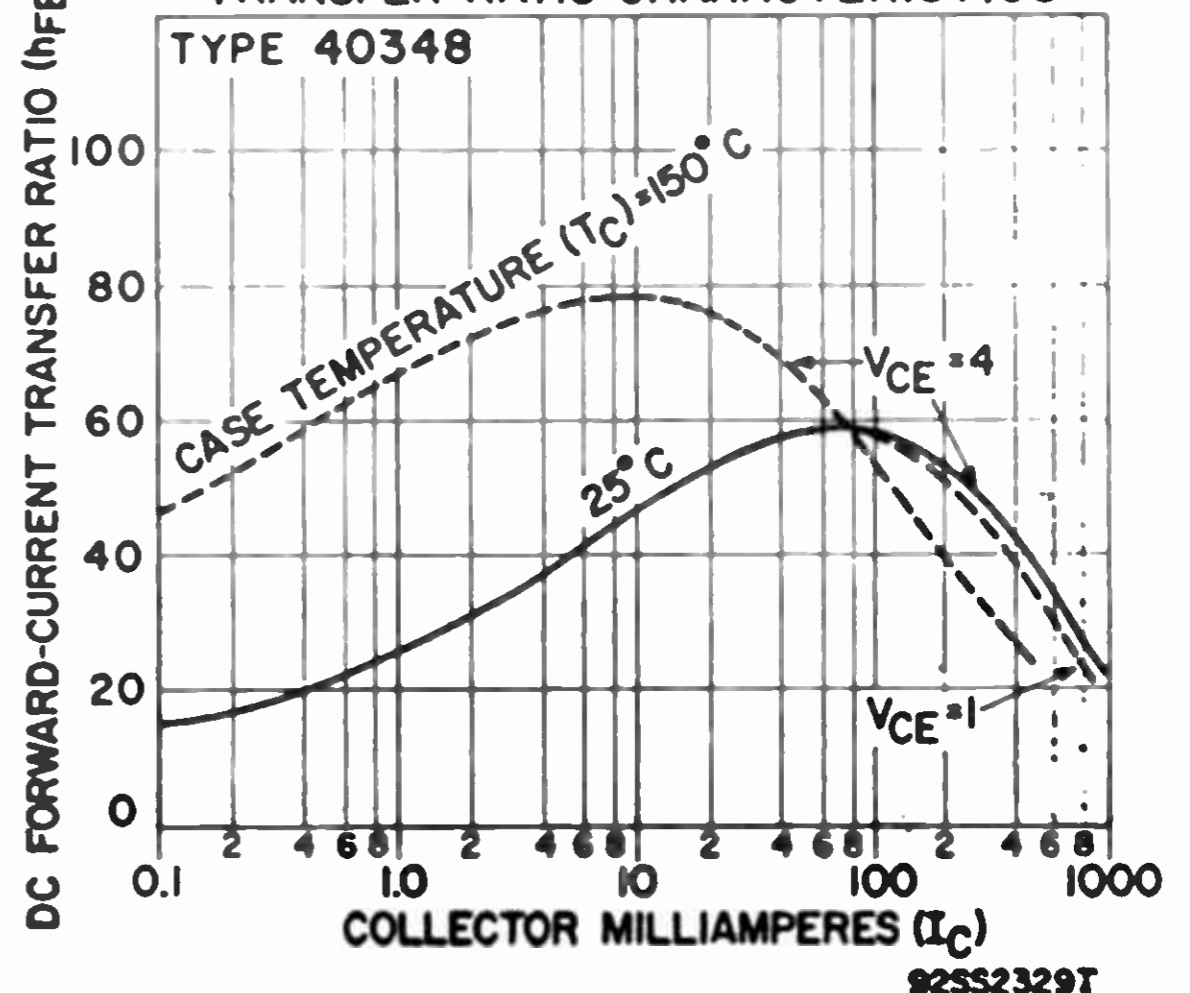
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage:			
$V_{BE} = -1.5$ V, $I_C = 50$ mA	V_{CEV} (sus)	90 min	V
$I_C = 50$ mA, $I_B = 0$	V_{CEO} (sus)	65 min	V
Collector-to-Emitter Saturation Voltage			
($I_C = 300$ mA, $I_B = 30$ mA)	V_{CE} (sat)	0.75 max	V
Base-to-Emitter Voltage ($V_{CE} = 4$ V, $I_C = 300$ mA) ...	V_{BE}	1.3 max	V
Collector-Cutoff Current:			
$V_{CE} = 60$ V, $R_{BE} = 1$ k Ω , $T_c = 25^\circ$ C	I_{CER}	1 max	μ A
$V_{CE} = 60$ V, $R_{BE} = 1$ k Ω , $T_c = 150^\circ$ C	I_{CER}	1 max	mA
Emitter-Cutoff Current ($V_{EB} = 7$ V, $I_C = 0$)	I_{EBO}	10 max	μ A
Static Forward-Current Transfer Ratio:			
$V_{CE} = 4$ V, $I_C = 300$ mA	h_{FE}	30 to 100	
$V_{CE} = 4$ V, $I_C = 1$ A	h_{FE}	10 min	
Thermal Resistance, Junction-to-Case	θ_{J-C}	20 max	°C/W

TYPICAL COLLECTOR CHARACTERISTICS

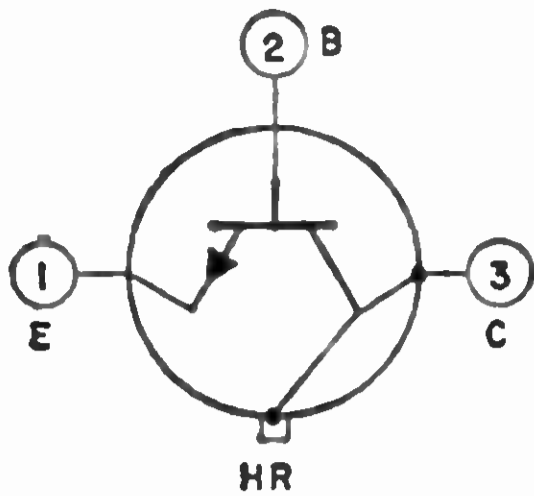


TYPICAL DC FORWARD-CURRENT TRANSFER-RATIO CHARACTERISTICS



POWER TRANSISTOR

40348V1



Si n-p-n single-diffused type featuring a base comprised of a homogeneous-resistivity silicon material. This type has an attached heat radiator for printed-circuit-board use in a wide variety of low- and medium-power applications requiring medium- and high-voltage power transistors for switching regulators, converters, inverters, relay controls, oscillators, and pulse and audio amplifiers. JEDEC TO-5 (with heat radiator), Outline No.8. This type is identical with type 40348 except for the following items:

MAXIMUM RATINGS

Transistor Dissipation:

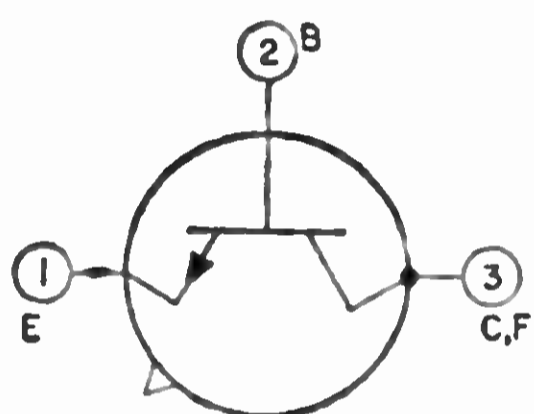
T_A up to 25°C	P_T	4.4	W
T_A above 25°C	P_T	See curve	page 300

CHARACTERISTICS (At case temperature = 25°C)

Thermal Resistance, Junction-to-Ambient	θ_{J-A}	40 max	°C/W
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POWER TRANSISTOR

40348V2



Si n-p-n single-diffused type featuring a base comprised of a homogeneous-resistivity silicon material. This type is used in a wide variety of low -and medium-power applications requiring medium- and high-voltage power transistors for switching regulators, converters, inverters, relay controls, oscillators, and pulse and audio amplifiers. JEDEC TO-5 (with flange), Outline No.6. See Mounting Hardware for desired mounting arrangement. This type is identical with type 40348 except for the following items:

MAXIMUM RATINGS

Transistor Dissipation:

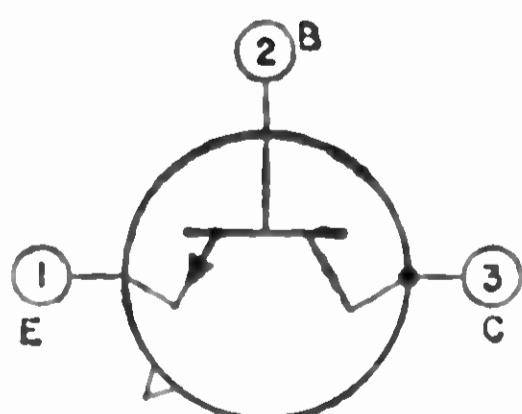
T_c up to 25°C	P_T	11.7	W
T_c above 25°C	P_T	See curve	page 300

CHARACTERISTICS (At mounting-flange temperature = 25°C)

Thermal Resistance, Junction-to-Case	θ_{J-C}	15 max	°C/W
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POWER TRANSISTOR

40349



Si n-p-n single-diffused type featuring a base comprised of a homogeneous-resistivity silicon material. This type is used in a wide variety of low- and medium-power applications where medium- and high-voltage power transistors are required, such as switching regulators, converters, inverters, relay controls, oscillators, and pulse and audio amplifiers. JEDEC TO-5, Outline No.5.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	160	V
Collector-to-Emitter Voltage:			
$V_{BE} = -1.5$ V	V_{CEV}	160	V
Base open	V_{CEO}	140	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Collector Current	I_C	1.5	A
Peak Collector Current	i_C	3	A
Base Current	I_B	0.5	A

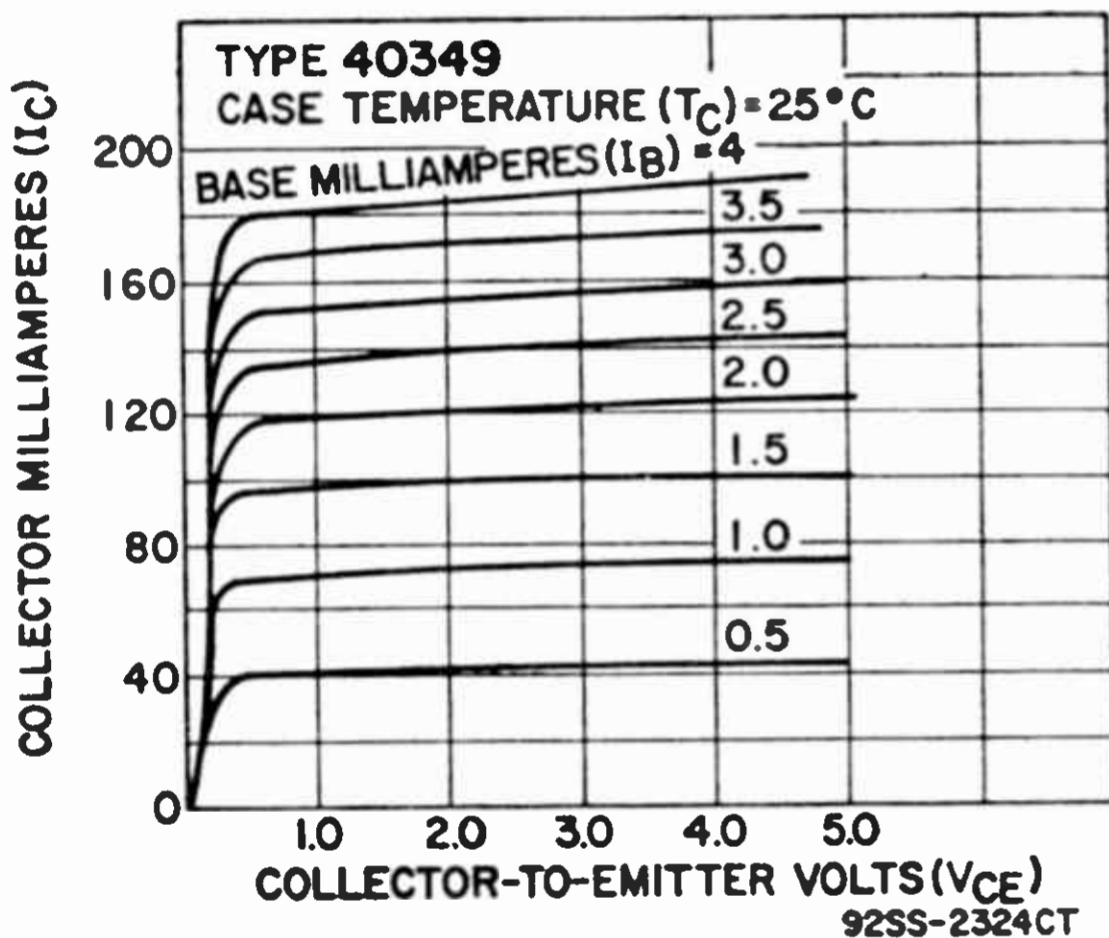
MAXIMUM RATINGS (cont'd)

Transistor Dissipation:			
T_A up to 25°C	P_T	1	W
T_C up to 25°C	P_T	8.75	W
T_A and T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	230	°C

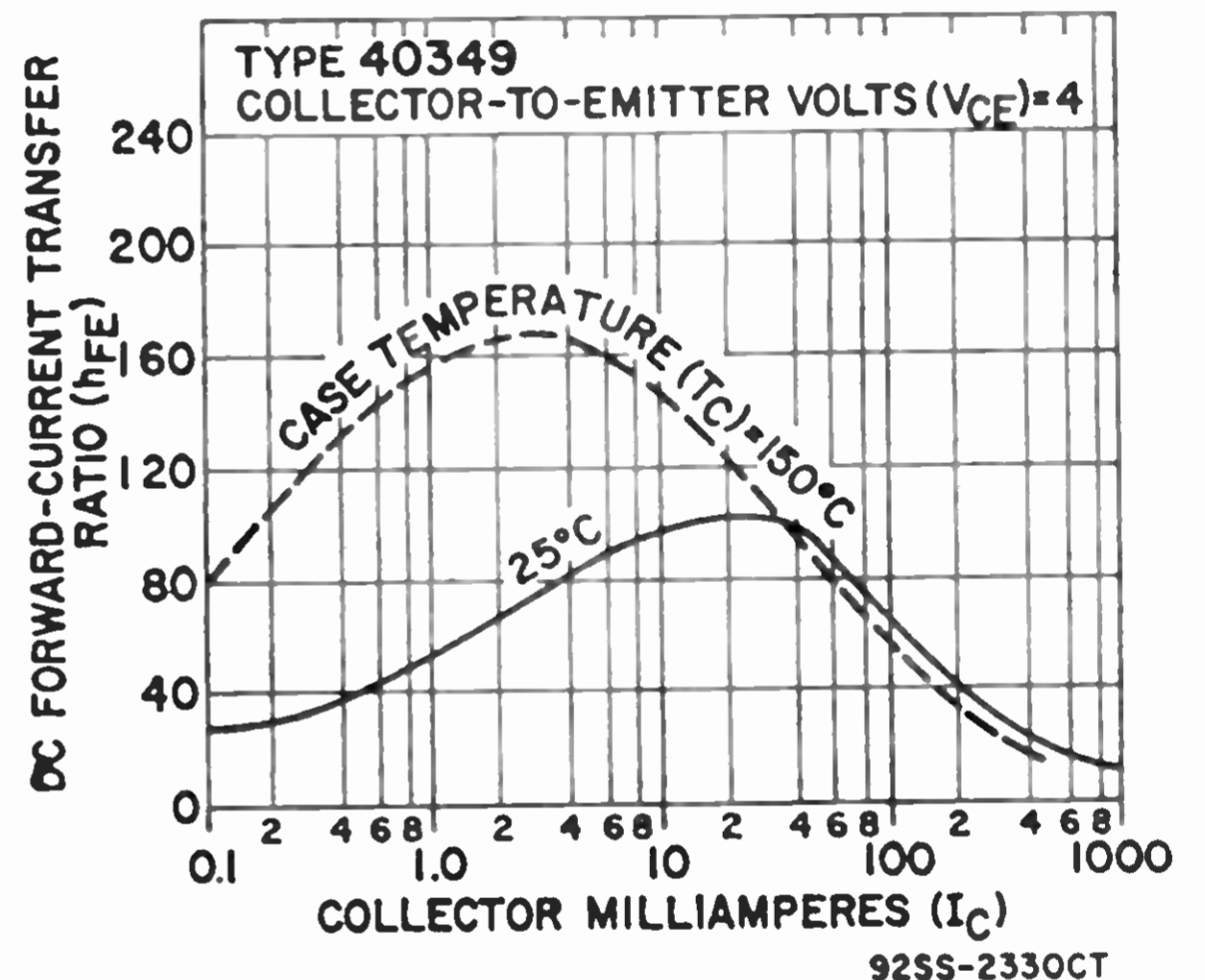
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage:			
$V_{BE} = -1.5$ V, $I_C = 50$ mA, $t_p = 300$ μ s, $df = 1.8\%$	V_{CEV} (sus)	160 min	V
$I_C = 50$ mA, $I_B = 0$, $t_p = 300$ μ s, $df = 1.8\%$	V_{CEO} (sus)	140 min	V
Collector-to-Emitter Saturation Voltage			
($I_C = 150$ mA, $I_B = 15$ mA)	V_{CE} (sat)	0.5 max	V
Base-to-Emitter Voltage ($V_{CE} = 4$ V, $I_C = 150$ mA)	V_{BE}	1.1 max	V
Collector-Cutoff Current:			
$V_{CE} = 90$ V, $R_{BE} = 1$ k Ω , $T_C = 25^\circ$ C	I_{CER}	1 max	μ A
$V_{CE} = 90$ V, $R_{BE} = 1$ k Ω , $T_C = 150^\circ$ C	I_{CEO}	1 max	mA
Emitter-Cutoff Current ($V_{EB} = 7$ V, $I_C = 0$)	I_{EBO}	10 max	μ A
Static Forward-Current Transfer Ratio:			
$V_{CE} = 4$ V, $I_C = 150$ mA	h_{FE}	25 to 100	
$V_{CE} = 4$ V, $I_C = 450$ mA	h_{FE}	10 min	
Thermal Resistance, Junction-to-Case	θ_{J-C}	20 max	°C/W

TYPICAL COLLECTOR CHARACTERISTICS

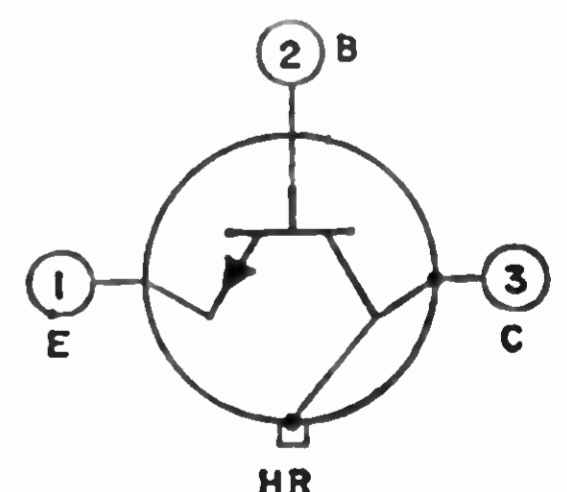


TYPICAL DC FORWARD-CURRENT TRANSFER-RATIO CHARACTERISTICS



40349V1 POWER TRANSISTOR

Si n-p-n single-diffused type featuring a base comprised of a homogeneous-resistivity silicon material. This type has an attached heat radiator for printed-circuit-board use in a wide variety of low- and medium-power applications requiring medium- and high-voltage power transistors for switching regulators, converters, inverters, relay controls, oscillators, and pulse and audio amplifiers. JEDEC TO-5 (with heat radiator), Outline No.8. This type is identical with type 40439 except for the following items:



MAXIMUM RATINGS

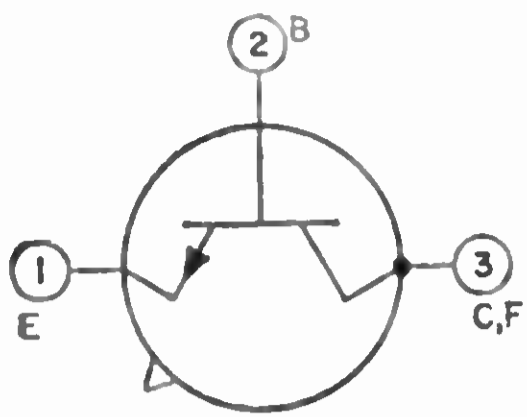
Transistor Dissipation:			
T_A up to 25°C	P_T	4.4	W
T_A above 25°C	P_T	See curve page 300	

CHARACTERISTICS (At case temperature = 25°C)

Thermal Resistance, Junction-to-Ambient	θ_{J-A}	40 max	°C/W
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POWER TRANSISTOR

40349V2



Si n-p-n single-diffused type featuring a base comprised of a homogeneous-resistivity silicon material. This type is used in a wide variety of low- and medium-power applications requiring medium- and high-voltage power transistors for switching regulators, converters, inverters, relay controls, oscillators, and pulse and audio

amplifiers. JEDEC TO-5 (with flange), Outline No.6. See **Mounting Hardware** for desired mounting arrangement. This type is identical with type 40349 except for the following items:

MAXIMUM RATINGS

Transistor Dissipation:			
T _c up to 25°C	P _T	11.7	W
T _c above 25°C	P _T	See curve page 300	

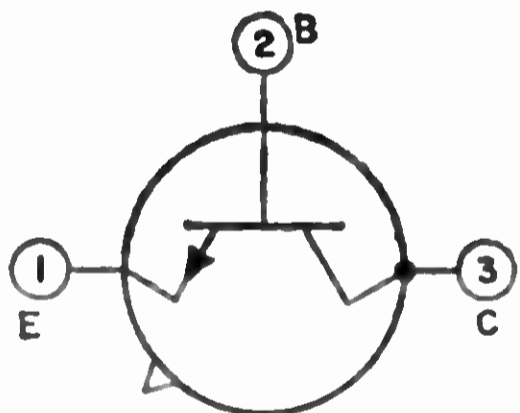
CHARACTERISTICS (At case temperature = 25°C)

Thermal Resistance, Junction-to-Case	θ _{J-c}	15 max	°C/W
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Refer to Chart of Discontinued Transistors **40350**

Refer to Chart of Discontinued Transistors **40351**

Refer to Chart of Discontinued Transistors **40352**



TRANSISTOR

40354

Si n-p-n type used in video-output amplifier stages of black-and-white television receivers. JEDEC TO-104, Outline No.32.

MAXIMUM RATINGS

Collector-to-Emitter Voltage	V _{CEO}	150	V
Emitter-to-Base Voltage	V _{EBO}	5	V
Collector Current	I _C	50	mA
Transistor Dissipation:			
T _A up to 25°C	P _T	0.5	W
T _A above 25°C	P _T	See curve page 300	
Temperature Range:			
Operating (Junction)	T _J (opr)	-65 to 175	°C
Storage	T _{STG}	-65 to 175	°C
Lead-Soldering Temperature (10 s max)	T _L	255	°C

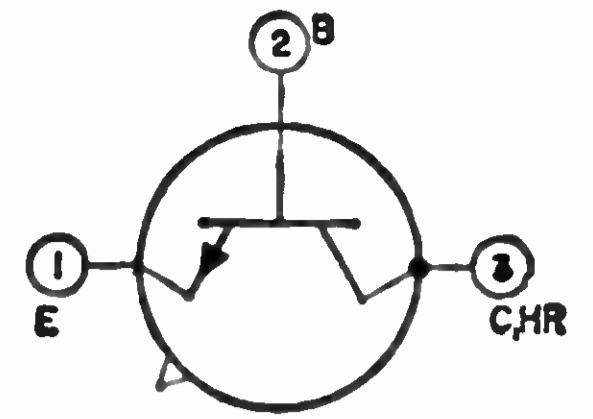
CHARACTERISTICS

Collector-to-Emitter Breakdown Voltage (I _C = 1 mA, I _B = 0)	V _{(BR)CEO}	150 min	V
Emitter-to-Base Breakdown Voltage (I _E = -10 μA, I _C = 0)	V _{(BR)EBO}	5 min	V
Collector-to-Emitter Saturation Voltage (I _C = 30 mA, I _B = 1 mA)	V _{CE} (sat)	5 max	V
Collector-Cutoff Current (V _{CB} = 120 V, I _E = 0)	I _{CBO}	100 max	V
Static Forward-Current Transfer Ratio (V _{CE} = 10 V, I _C = 10 mA)	h _{FE}	55	
Collector-to-Base Feedback Capacitance (V _{CE} = 10 V, I _C = 30 mA)	C _{cb}	3.5 max	pF
Gain-Bandwidth Product:			
V _{CE} = 10 V, I _C = 30 mA	f _T	50 min	MHz
V _{CE} = 140 V, I _C = 2 mA	f _T	50 min	MHz
Thermal Resistance, Junction-to-Case	θ _{J-c}	60 max	°C/W

40355

TRANSISTOR

Si n-p-n type used in video-output amplifier stages of black-and-white television receivers. JEDEC TO-104 (with heat radiator), Outline No.33. This type is identical with type 40354 except for the following item:



MAXIMUM RATINGS

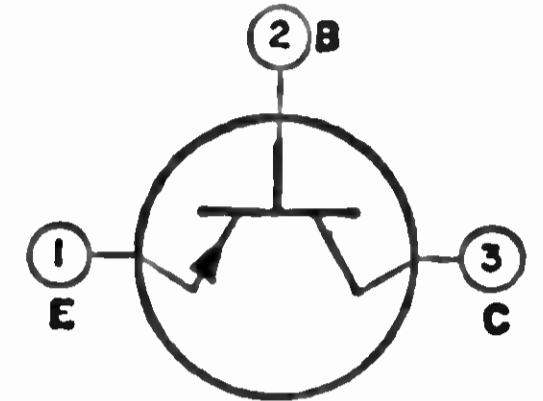
Transistor Dissipation:

T_A up to 25°C	P_T	1	W
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40359

TRANSISTOR

Ge p-n-p alloy-junction type used in af-amplifier applications in consumer product and industrial equipment. JEDEC TO-1, Outline No.1.



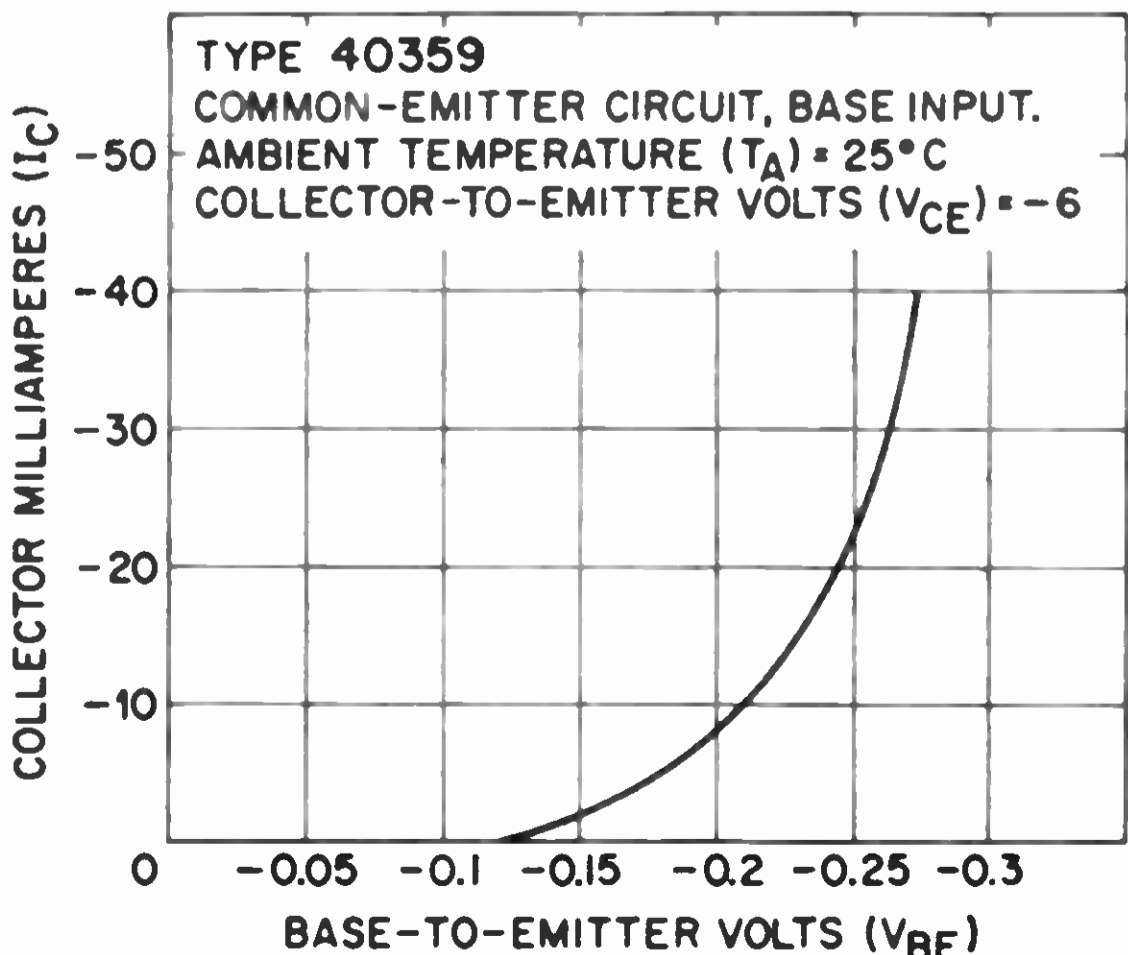
MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CB0}	-20	V
Collector-to-Emitter Voltage ($R_{BE} \leq 10000 \Omega$)	V_{CER}	-18	V
Emitter-to-Base Voltage	V_{EB0}	-2.5	V
Collector Current	I_C	-50	mA
Emitter Current	I_E	50	mA
Transistor Dissipation:			
T_A up to 55°C	P_T	120	mW
T_A above 55°C	P_T	See curve page 300	
Temperature Range:			
Operating	T_A	-65 to 100	°C
Storage	T_{STG}	-65 to 100	°C
Lead-Soldering Temperature (10 s max)	T_L	255	°C

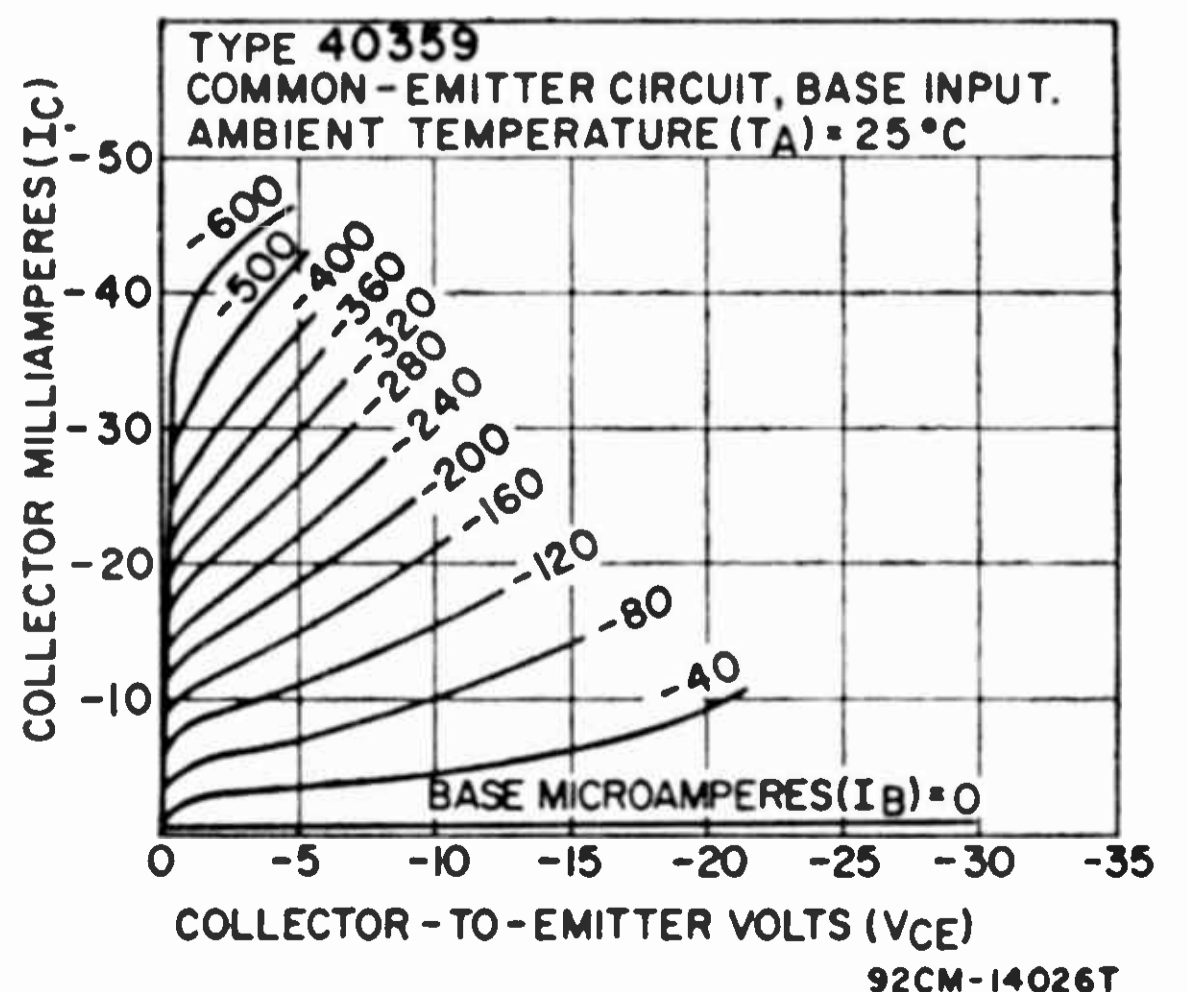
CHARACTERISTICS

Collector-to-Emitter Breakdown Voltage ($R_{BE} = 10 k\Omega$, $I_C = -1 mA$)	$V_{(BR)CER}$	-18 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -0.05 mA$, $I_C = 0$)	$V_{(BR)EBO}$	2.5 min	V
Collector-Cutoff Current ($V_{CB} = -15 V$, $I_E = 0$)	I_{CBO}	-12 max	μA
Emitter-Cutoff Current ($V_{EB} = 2.5 V$, $I_C = 0$)	I_{EBO}	-12 max	μA
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = -6 V$, $I_C = -1 mA$, $f = 1 kHz$)	h_{fe}	40 to 165	
Small-Signal Forward-Current Transfer-Ratio Cutoff Frequency ($V_{CE} = -6 V$, $I_C = -1 mA$)	f_{hfb}	10	MHz
Intrinsic Base-Spreading Resistance ($V_{CE} = -6 V$, $I_C = -1 mA$, $f = 100 MHz$)	$r_{bb'}$	200	Ω

TYPICAL TRANSFER CHARACTERISTIC

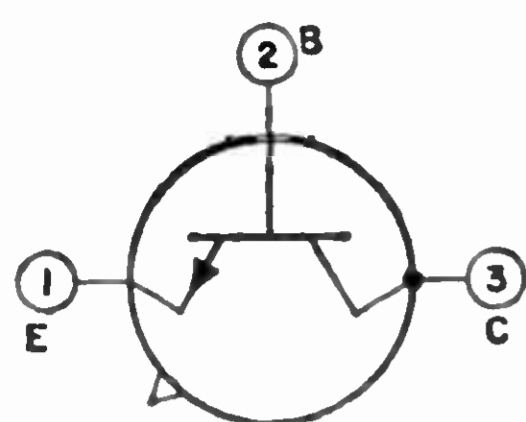


TYPICAL COLLECTOR CHARACTERISTICS



POWER TRANSISTOR

40360



Si n-p-n type used in audio-amplifier inverter and driver stages for economical high-quality performance. Designed to assure freedom from second breakdown in the operating region. JEDEC TO-5, Outline No.5. For collector-characteristics and transfer-characteristics curves, refer to type 40309.

MAXIMUM RATINGS

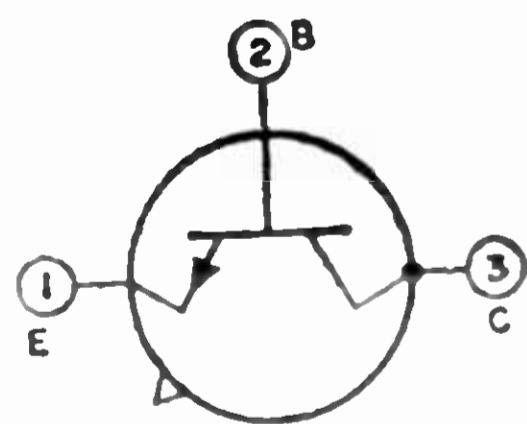
Collector-to-Emitter Sustaining Voltage	$V_{CEO(sus)}$	70	V
Emitter-to-Base Voltage	V_{EBO}	4	V
Collector Current	I_C	0.7	A
Base Current	I_B	0.2	A
Transistor Dissipation:			
T_A up to 25°C	P_T	1	W
T_C up to 25°C	P_T	5	W
T_A and T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 200	°C

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CEO(sus)}$	70 min	V
Collector-to-Emitter Saturation Voltage ($I_B = 15\text{ mA}$, $I_C = 150\text{ mA}$)	$V_{CE(sat)}$	1.4 max	V
Base-to-Emitter Voltage ($V_{CE} = 4\text{ V}$, $I_C = 10\text{ mA}$) ...	V_{BE}	1 max	V
Collector-Cutoff Current:			
$V_{CE} = 60\text{ V}$, $I_B = 0$, $T_C = 25^\circ\text{C}$	I_{CEO}	1 max	μA
$V_{CE} = 60\text{ V}$, $I_B = 0$, $T_C = 150^\circ\text{C}$	I_{CEO}	250 max	μA
Emitter-Cutoff Current ($V_{EB} = 4\text{ V}$, $I_C = 0$)	I_{EBO}	1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 4\text{ V}$, $I_C = 10\text{ mA}$)	h_{FE}	40 to 200	
Gain-Bandwidth Product ($V_{CE} = 4\text{ V}$, $I_C = 50\text{ mA}$)	f_T	100	MHz
Thermal Resistance, Junction-to-Case	θ_{J-C}	35 max	°C/W
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	175 max	°C/W

POWER TRANSISTOR

40361



Si n-p-n type used in audio-amplifier inverter and driver stages for economical high-quality performance. Designed to assure freedom from second breakdown in the operating region. JEDEC TO-5, Outline No.5. For collector-characteristics and transfer-characteristics curves, refer to type 40309.

MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage ($R_{BE} = 200\ \Omega$)	$V_{CER(sus)}$	70	V
Emitter-to-Base Voltage	V_{EBO}	4	V
Collector Current	I_C	0.7	A
Base Current	I_B	0.2	A
Transistor Dissipation:			
T_A up to 25°C	P_T	1	W
T_C up to 25°C	P_T	5	W
T_A and T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 200	°C

CHARACTERISTICS (At case temperature = 25°C)

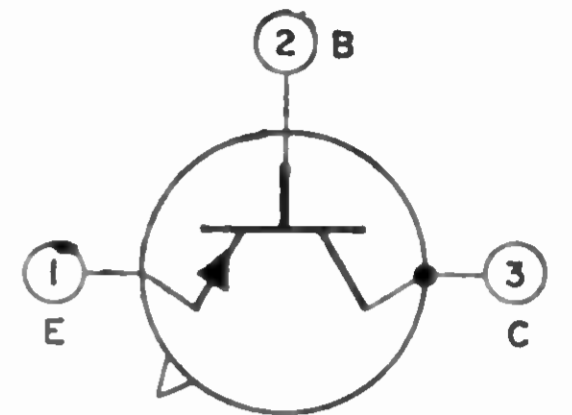
Collector-to-Emitter Sustaining Voltage ($R_{BE} = 200\ \Omega$, $I_C = 100\text{ mA}$)	$V_{CER(sus)}$	70 min	V
Collector-to-Emitter Saturation Voltage ($I_B = 15\text{ mA}$, $I_C = 150\text{ mA}$)	$V_{CE(sat)}$	1.4 max	V
Base-to-Emitter Voltage ($V_{CE} = 4\text{ V}$, $I_C = 50\text{ mA}$) ...	V_{BE}	1 max	V
Collector-Cutoff Current:			
$V_{CE} = 60\text{ V}$, $R_{BE} = 200\ \Omega$, $T_C = 25^\circ\text{C}$	I_{CER}	1 max	μA
$V_{CE} = 60\text{ V}$, $R_{BE} = 200\ \Omega$, $T_C = 150^\circ\text{C}$	I_{CER}	100 max	μA
Emitter-Cutoff Current ($V_{EB} = 4\text{ V}$, $I_C = 0$)	I_{EBO}	1 max	mA

CHARACTERISTICS (cont'd)

Static Forward-Current Transfer Ratio ($V_{CE} = 4\text{ V}$, $I_C = 50\text{ mA}$)	h_{FE}	70 to 350	
Gain-Bandwidth Product ($V_{CE} = 4\text{ V}$, $I_C = 50\text{ mA}$)	f_T	100	MHz
Thermal Resistance, Junction-to-Case	θ_{J-C}	35 max	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	175 max	$^{\circ}\text{C}/\text{W}$

40362 POWER TRANSISTOR

Si p-n-p used in audio-amplifier drive stages for economical high-quality performance. Designed to assure freedom from second breakdown in the operating region. P-N-P structure permits complementary driver operation with a matching n-p-n type such as 40361. JEDEC TO-5, Outline No.5. For collector-characteristics and input-characteristics curves, refer to type 40319.



MAXIMUM RATINGS

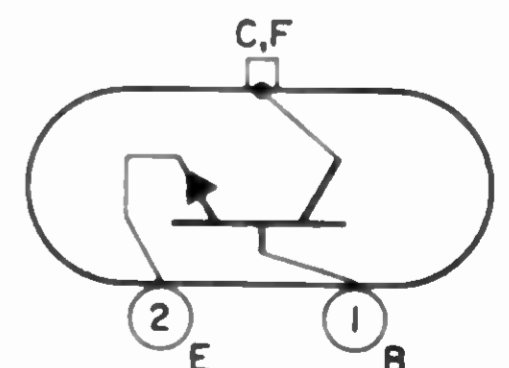
Collector-to-Emitter Sustaining Voltage ($R_{BE} = 200\ \Omega$)	$V_{CER(SUS)}$	-70	V
Emitter-to-Base Voltage	V_{EBO}	-4	V
Collector Current	I_C	-0.7	A
Base Current	I_B	-0.2	A
Transistor Dissipation:			
T_A up to 25°C	P_T	1	W
T_C up to 25°C	P_T	5	W
T_A and T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 200	$^{\circ}\text{C}$

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($R_{BE} = 200\ \Omega$, $I_C = 100\text{ mA}$)	$V_{CER(SUS)}$	-70 min	V
Collector-to-Emitter Saturation Voltage ($I_B = 15\text{ mA}$, $I_C = -150\text{ mA}$)	$V_{CE(sat)}$	-1.4 max	V
Base-to-Emitter Voltage ($V_{CE} = -4\text{ V}$, $I_C = -50\text{ mA}$)	V_{BE}	-1 max	V
Collector-Cutoff Current:			
$V_{CE} = -60\text{ V}$, $R_{BE} = 200\ \Omega$, $T_C = 25^{\circ}\text{C}$	I_{CER}	-1 max	μA
$V_{CE} = -60\text{ V}$, $R_{BE} = 200\ \Omega$, $T_C = 150^{\circ}\text{C}$	I_{CER}	-100 max	μA
Emitter-Cutoff Current ($V_{EB} = -4\text{ V}$, $I_C = 0$)	I_{EBO}	-1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = -4\text{ V}$, $I_C = -50\text{ mA}$)	h_{FE}	35 to 200	
Gain-Bandwidth Product ($V_{CE} = -4\text{ V}$, $I_C = -50\text{ mA}$)	f_T	100	MHz
Thermal Resistance, Junction-to-Case	θ_{J-C}	35 max	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	175 max	$^{\circ}\text{C}/\text{W}$

40363 POWER TRANSISTOR

Si n-p-n type used in audio-amplifier output stages for economical high-quality performance. Designed to assure freedom from second breakdown in the operating region. JEDEC TO-3, Outline No.2. See Mounting Hardware for desired mounting arrangement. For collector-characteristics and transfer-characteristics curves, refer to type 40325.



MAXIMUM RATINGS

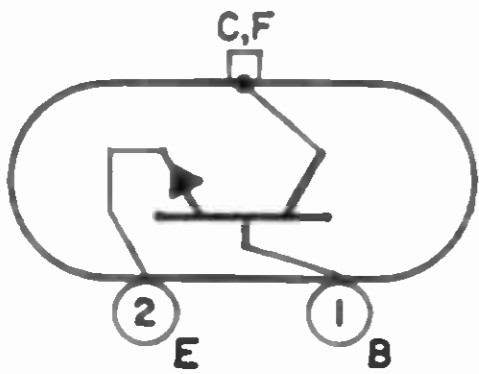
Collector-to-Emitter Sustaining Voltage ($R_{BE} = 200\ \Omega$)	$V_{CER(SUS)}$	70	V
Emitter-to-Base Voltage	V_{EBO}	4	V
Collector Current	I_C	15	A
Base Current	I_B	7	A
Transistor Dissipation:			
T_C up to 25°C	P_T	115	W
T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 200	$^{\circ}\text{C}$

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($R_{BE} = 200 \Omega$, $I_C = 200 \text{ mA}$)	$V_{CER(SUS)}$	70 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 4 \text{ A}$, $I_B = 0.4 \text{ A}$)	$V_{CE(sat)}$	1.1 max	V
Base-to-Emitter Voltage ($V_{CE} = 4 \text{ V}$, $I_C = 4 \text{ A}$)	V_{BE}	1.8 max	V
Collector-Cutoff Current: $V_{CE} = 60 \text{ V}$, $R_{BE} = 200 \Omega$, $T_C = 25^\circ\text{C}$	I_{CER}	0.5 max	mA
$V_{CE} = 60 \text{ V}$, $R_{BE} = 200 \Omega$, $T_C = 150^\circ\text{C}$	I_{CER}	2 max	mA
Emitter-Cutoff Current ($V_{EB} = 4 \text{ V}$, $I_C = 0$)	I_{EBO}	5 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 4 \text{ V}$, $I_C = 4 \text{ A}$)	h_{FE}	20 to 70	
Gain-Bandwidth Product ($V_{CE} = 4 \text{ V}$, $I_C = 3 \text{ A}$)	f_T	700	kHz
Thermal Resistance, Junction-to-Case	θ_{J-C}	1.5 max	$^\circ\text{C/W}$

POWER TRANSISTOR

40364



Si n-p-n type used in audio-amplifier output stages for economical high-quality performance. Designed to assure freedom from second breakdown in the operating region. JEDEC TO-66, Outline No.25. See Mounting Hardware for desired mounting arrangement.

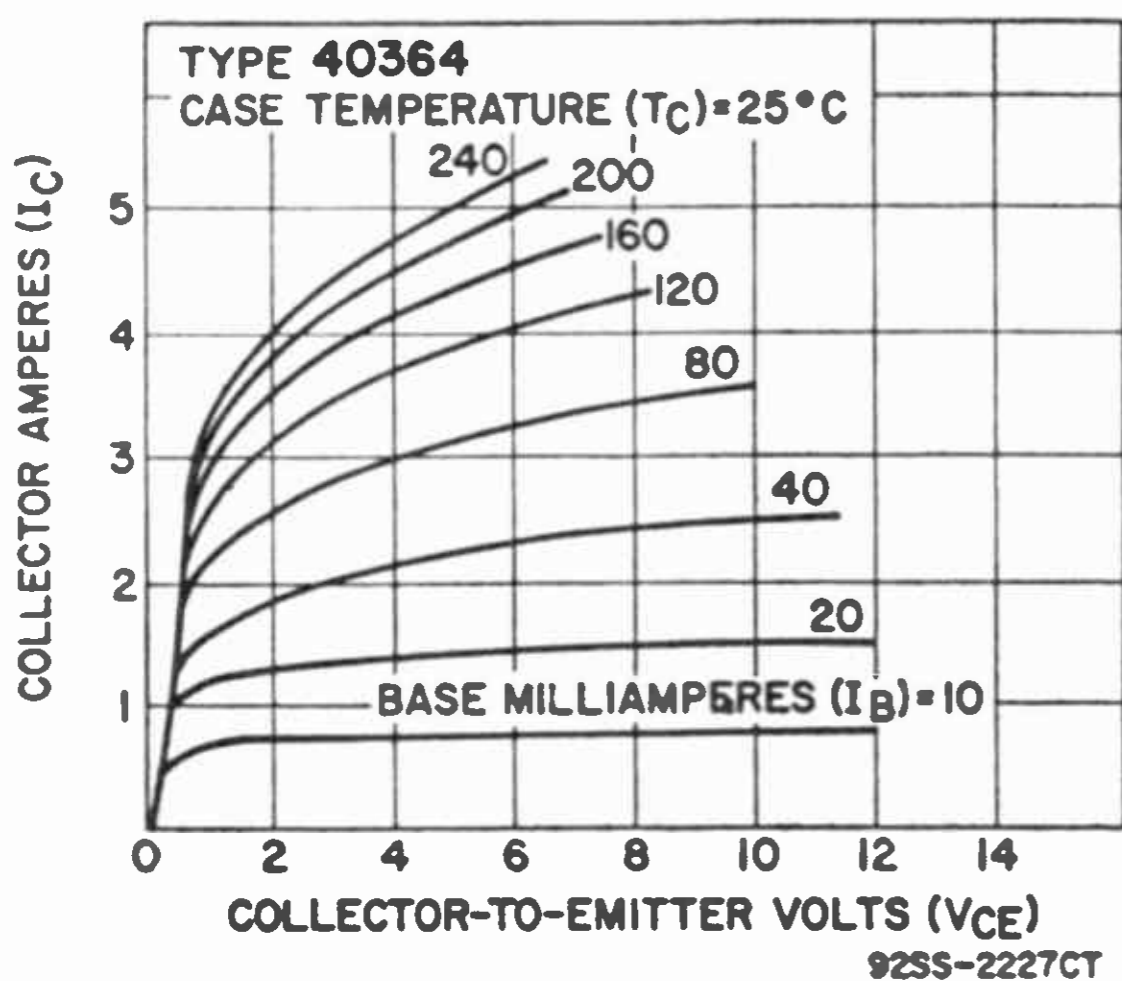
MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage ($R_{BE} = 150 \Omega$)	$V_{CER(SUS)}$	60	V
Emitter-to-Base Voltage	V_{EBO}	4	V
Collector Current	I_C	7	A
Base Current	I_B	5	A
Transistor Dissipation: T_C up to 25°C	P_T	35	W
T_C above 25°C	P_T	See curve page 300	
Temperature Range: Operating (Junction)	$T_J(\text{opr})$	-65 to 200	$^\circ\text{C}$

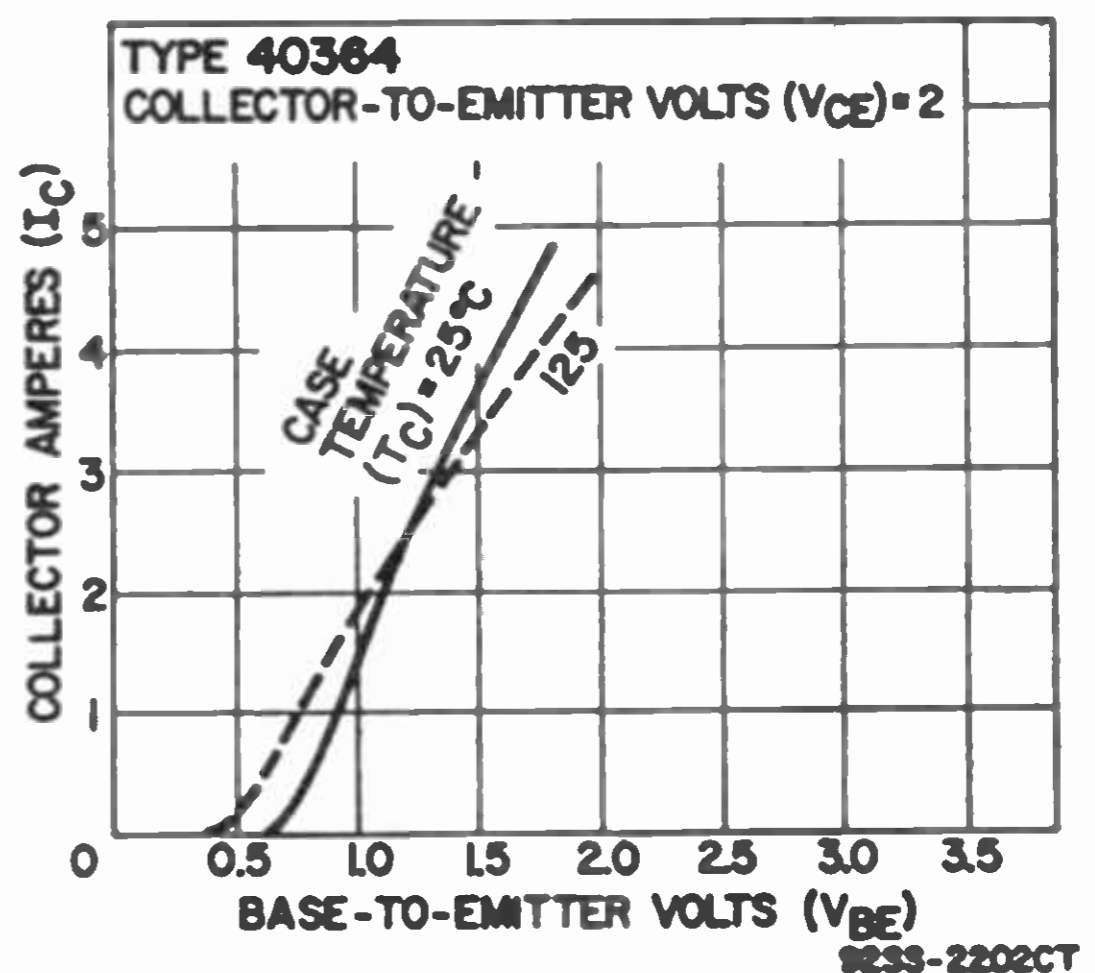
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($R_{BE} = 150 \Omega$, $I_C = 200 \text{ mA}$)	$V_{CER(SUS)}$	60 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 2.5 \text{ A}$, $I_B = 0.25 \text{ A}$)	$V_{CE(sat)}$	2 max	V
Base-to-Emitter Voltage ($V_{CE} = 5 \text{ V}$, $I_C = 2.5 \text{ A}$)	V_{BE}	1.8 max	V
Collector-Cutoff Current: $V_{CE} = 50 \text{ V}$, $R_{BE} = 150 \Omega$, $T_C = 25^\circ\text{C}$	I_{CER}	0.5 max	mA
$V_{CE} = 50 \text{ V}$, $R_{BE} = 150 \Omega$, $T_C = 150^\circ\text{C}$	I_{CER}	2 max	mA
Emitter-Cutoff Current ($V_{EB} = 4 \text{ V}$, $I_C = 0$)	I_{EBO}	5 max	mA
Static Forward-Current Transfer Ratio: $V_{CE} = 5 \text{ V}$, $I_C = 0.5 \text{ A}$	h_{FE}	35 to 175	
$V_{CE} = 5 \text{ V}$, $I_C = 2.5 \text{ A}$	h_{FE}	20 min	
Gain-Bandwidth Product ($V_{CE} = 10 \text{ V}$, $I_C = 2.5 \text{ A}$)	f_T	15	MHz
Second-Breakdown Collector Current ($V_{CE} = 40 \text{ V}$)	$I_{S/b}$	750 min	mA
Thermal Resistance, Junction-to-Case	θ_{J-C}	5 max	$^\circ\text{C/W}$

TYPICAL COLLECTOR CHARACTERISTICS

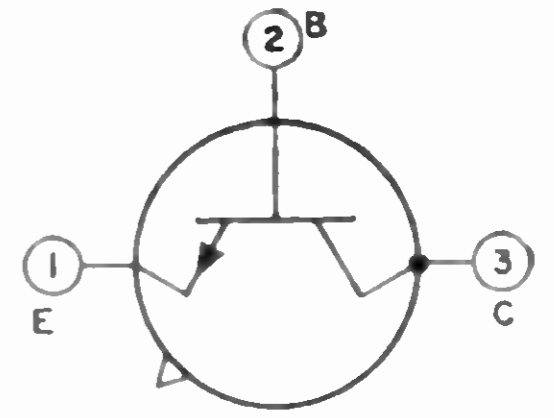


TYPICAL TRANSFER CHARACTERISTICS



40366**POWER TRANSISTOR**

Si n-p-n triple-diffused planar type subjected to special preconditioning tests for high-reliability operation in medium- and high-power switching and amplifier applications in military and industrial equipment. JEDEC TO-5, Outline No.5.

**MAXIMUM RATINGS**

Collector-to-Emitter Voltage:

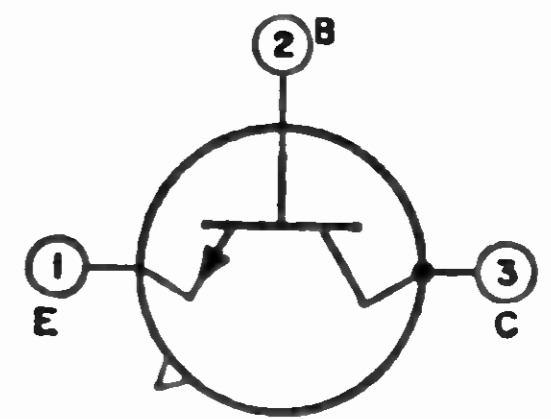
$R_{BE} \leq 10 \Omega$	V_{CER}	80	V
Base open	V_{CEO}	65	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Collector Current	I_C	1	A
Transistor Dissipation:			
T_C up to 25°C	P_T	5	A
T_A above 25°C	P_T	1	A
T_C and T_A above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	$^\circ\text{C}$
Storage	T_{STG}	-65 to 200	$^\circ\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	255	$^\circ\text{C}$

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Base Breakdown Voltage ($V_{EB} = 1.5 \text{ V}$, $I_C = 0.1 \text{ mA}$)	$V_{(BR)CBV}$	120 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.1 \text{ mA}$) ...	$V_{(BR)EBO}$	7 min	V
Collector-to-Emitter Sustaining Voltage:			
$R_{BE} = 10 \Omega$, $I_C = 100 \text{ mA}$, $t_p = 300 \mu\text{s}$, $df = 1.8\%$	$V_{CER(SUS)}$	80 min	V
$I_C = 100 \text{ mA}$, $I_B = 0$, $t_p = 300 \mu\text{s}$, $df = 1.8\%$	$V_{CEO(SUS)}$	65 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 150 \text{ mA}$, $I_B = 15 \text{ mA}$, $t_p = 300 \mu\text{s}$, $df = 1.8\%$)	$V_{CE(sat)}$	0.5 max	V
Base-to-Emitter Saturation Voltage ($I_C = 150 \text{ mA}$, $I_B = 15 \text{ mA}$, $t_p = 300 \mu\text{s}$, $df = 1.8\%$)	$V_{BE(sat)}$	1.1 max	V
Collector-Cutoff Current ($V_{CB} = 60 \text{ V}$, $I_E = 0$)	I_{CBO}	2 max	nA
Emitter-Cutoff Current ($V_{EB} = 5 \text{ V}$, $I_C = 0$)	I_{EBO}	5 max	nA
Static Forward-Current Transfer Ratio:			
$V_{CE} = 10 \text{ V}$, $I_C = 0.01 \text{ mA}$	h_{FE}	10 min	
$V_{CE} = 10 \text{ V}$, $I_C = 0.1 \text{ mA}$	h_{FE}	20 min	
Pulsed Forward-Current Transfer Ratio:			
$V_{CE} = 10 \text{ V}$, $I_C = 150 \text{ mA}$, $t_p = 300 \mu\text{s}$, $df = 1.8\%$...	$h_{FE}(\text{pulsed})$	40 to 120	
$V_{CE} = 10 \text{ V}$, $I_C = 500 \text{ mA}$, $t_p = 300 \mu\text{s}$, $df = 1.8\%$..	$h_{FE}(\text{pulsed})$	25 min	
$V_{CE} = 10 \text{ V}$, $I_C = 1000 \text{ mA}$, $t_p = 300 \mu\text{s}$, $df = 1.8\%$	$h_{FE}(\text{pulsed})$	10 min	

40367**POWER TRANSISTOR**

Si n-p-n single-diffused type featuring a base comprised of a homogeneous-resistivity silicon material. This type is subjected to special preconditioning tests for high-reliability operation in medium- and high-power switching and amplifier applications in military and industrial equipment. JEDEC TO-5, Outline No.5. This type is a high-reliability version of type 2N1482.

**MAXIMUM RATINGS**

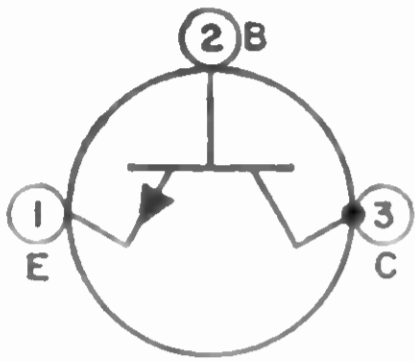
Collector-to-Base Voltage	V_{CBO}	100	V
Collector-to-Emitter Voltage:			
$V_{BE} = -1.5 \text{ V}$	V_{CEV}	100	V
Base open	V_{CEO}	55	V
Emitter-to-Base Voltage	V_{EBO}	12	V
Collector Current	I_C	1.5	A
Base Current	I_B	1	A
Transistor Dissipation:			
T_A up to 25°C	P_T	1	W
T_C up to 25°C	P_T	5	W
T_A or T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	$^\circ\text{C}$
Storage	T_{STG}	-65 to 200	$^\circ\text{C}$
Pin-Soldering Temperature (10 s max)	T_P	255	$^\circ\text{C}$

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Breakdown Voltage ($V_{BE} = -1.5\text{ V}$, $I_C = 0.25\text{ mA}$)	$V_{(BR)CEV}$	100 min	V
Collector-to-Emitter Sustaining Voltage ($I_C = 50\text{ mA}$, $I_B = 0$)	$V_{CEO(SUS)}$	55 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 200\text{ mA}$, $I_B = 10\text{ mA}$)	$V_{CE(sat)}$	1.4 max	V
Base-to-Emitter Voltage ($V_{CE} = 4\text{ V}$, $I_C = 200\text{ mA}$) ...	V_{BE}	3 max	V
Collector-Cutoff Current ($V_{CB} = 30\text{ V}$, $I_E = 0$)	I_{CBO}	4 max	μA
Emitter-Cutoff Current ($V_{EB} = 12\text{ V}$, $I_C = 0$)	I_{EBO}	2 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 4\text{ V}$, $I_C = 200\text{ mA}$)	h_{FE}	35 to 100	

POWER TRANSISTOR

40368



Si n-p-n single-diffused type featuring a base comprised of a homogeneous-resistivity silicon material. This type is subjected to special preconditioning tests for high-reliability operation in medium- and high-power switching and amplifier applications in military and industrial equipment. JEDEC TO-8, Outline No.10. See Mounting

Hardware for desired mounting arrangement. This type is a high-reliability version of type 2N1486.

MAXIMUM RATINGS

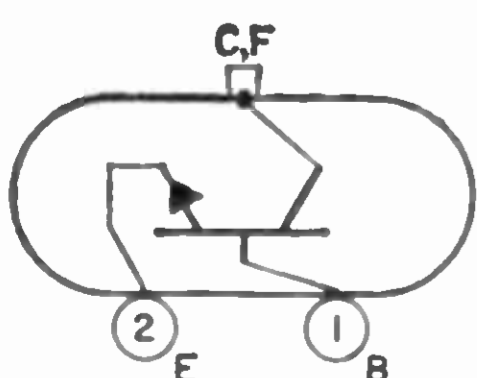
Collector-to-Base Voltage	V_{CBO}	100	V
Collector-to-Emitter Voltage: $V_{BE} = -1.5\text{ V}$	V_{CEV}	100	V
Base open	V_{CEO}	55	V
Emitter-to-Base Voltage	V_{EBO}	12	V
Collector Current	I_C	3	A
Base Current	I_B	1.5	A
Transistor Dissipation: T_c up to 25°C	P_T	25	W
T_c above 25°C	P_T	See curve page 300	
Temperature Range: Operating (Junction)	$T_J(\text{opr})$	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Pin-Soldering Temperature	T_P	235	°C

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Breakdown Voltage ($V_{BE} = -1.5\text{ V}$, $I_C = 0.25\text{ mA}$)	$V_{(BR)CEV}$	100 min	V
Collector-to-Emitter Sustaining Voltage ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CEO(SUS)}$	55 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 750\text{ mA}$, $I_B = 10\text{ mA}$)	$V_{CE(sat)}$	0.75 max	V
Base-to-Emitter Voltage ($V_{CE} = 4\text{ V}$, $I_C = 750\text{ mA}$) ...	V_{BE}	2.5 max	V
Collector-Cutoff Current ($V_{CB} = 30\text{ V}$, $I_E = 0$)	I_{CBO}	9 max	μA
Emitter-Cutoff Current ($V_{EB} = 12\text{ V}$, $I_C = 0$)	I_{EBO}	5 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 4\text{ V}$, $I_C = 750\text{ mA}$)	h_{FE}	35 to 100	

POWER TRANSISTOR

40369



Si n-p-n single-diffused type featuring a base comprised of a homogeneous-resistivity silicon material. This type is subjected to special preconditioning tests for high-reliability operation in medium- and high-power switching and amplifier applications in military and industrial equipment. JEDEC TO-3, Outline No.2. See Mounting

Hardware for desired mounting arrangement. This type is a high-reliability version of type 2N1490.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	100	V
Collector-to-Emitter Voltage:			
$V_{BE} = -1.5$ V	V_{CEV}	100	V
Base open	V_{CEO}	55	V
Emitter-to-Base Voltage	V_{EBO}	10	V
Collector Current	I_C	6	A
Base Current	I_B	3	A
Transistor Dissipation:			
T_C up to 25°C	P_T	75	W
T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Pin-Soldering Temperature (10 s max)	T_P	235	°C

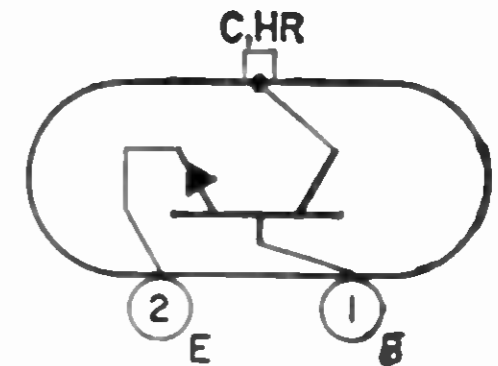
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Breakdown Voltage ($V_{BE} = -1.5$ V, $I_C = 0.25$ mA)	$V_{(BR)CEV}$	100 min	V
Collector-to-Emitter Sustaining Voltage ($I_C = 100$ mA, $I_B = 0$)	$V_{CEO(sus)}$	55 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 1300$ mA, $I_B = 100$ mA)	$V_{CE(sat)}$	1 max	V
Base-to-Emitter Voltage ($V_{CE} = 4$ V, $I_C = 1500$ mA)	V_{BE}	2.5 max	V
Collector-Cutoff Current ($V_{CB} = 30$ V, $I_E = 0$)	I_{CBO}	10 max	μA
Emitter-Cutoff Current ($V_{EB} = 10$ V, $I_C = 0$)	I_{EBO}	6 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 4$ V, $I_C = 1500$ mA)	h_{FE}	25 to 75	

40372

POWER TRANSISTOR

Si n-p-n diffused-junction type featuring a base comprised of a homogeneous-resistivity silicon material. This type has an attached heat radiator for printed-circuit-board use in power-switching circuits, series- and shunt-regulator driver and output stages, and high-fidelity amplifiers in commercial and industrial equipment. JEDEC TO-66 (with heat radiators), Outline No.26. This type is identical with type 2N3054 except for the following items:



MAXIMUM RATINGS

Transistor Dissipation:			
T_A up to 25°C	P_T	5.8	W
T_A above 25°C	P_T	See curve page 300	

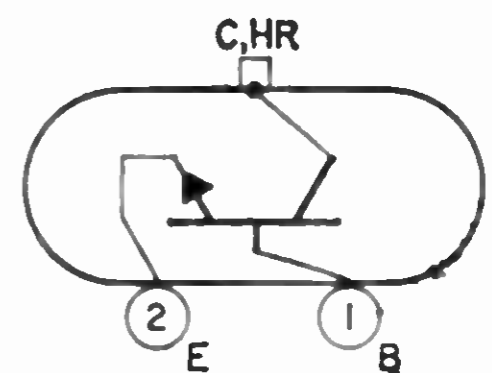
CHARACTERISTICS (At case temperature = 25°C)

Thermal Resistance, Junction-to-Ambient	θ_{J-A}	30 max	°C/W
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40373

POWER TRANSISTOR

Si n-p-n diffused type features a base comprised of a homogeneous-resistivity silicon material. This type has an attached radiator for printed-circuit-board used in high-voltage applications in power-switching circuits, series- and shunt-regulator driver and output stages, and dc-to-dc converters in military, commercial, and industrial equipment. JEDEC TO-66 (with heat radiator), Outline No.26. This type is identical with type 2N3441 except for the following items:



MAXIMUM RATINGS

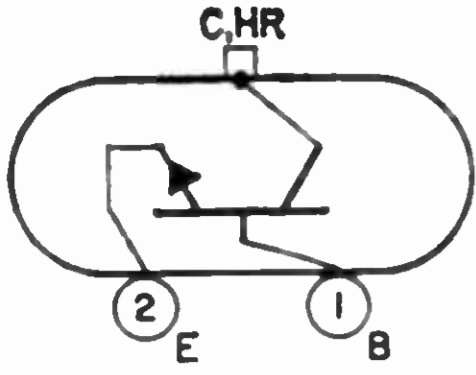
Transistor Dissipation:			
T_A up to 25°C	P_T	5.8	W
T_A above 25°C	P_T	See curve page 300	

CHARACTERISTICS (At case temperature = 25°C)

Thermal Resistance, Junction-to-Ambient	θ_{J-A}	30 max	°C/W
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TRANSISTOR

40374



Si n-p-n triple-diffused type with an attached radiator for printed-circuit-board use in high-speed switching and linear amplifier applications such as high-voltage operational amplifiers, high-voltage switches, switching regulators, converters, inverters, deflection and high-fidelity amplifiers in military, industrial, and commercial equipment. JEDEC TO-66 (with heat radiator), Outline No.26. This type is identical with type 2N3583 except for the following item:

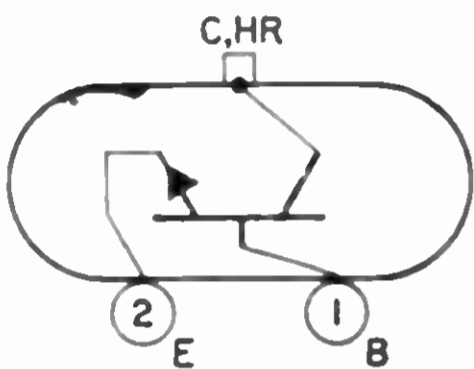
JEDEC TO-66 (with heat radiator), Outline No.26. This type is identical with type 2N3583 except for the following item:

CHARACTERISTICS (At case temperature = 25°C)

Thermal Resistance, Junction-to-Ambient	θ_{J-A}	30 max	°C/W
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POWER TRANSISTOR

40375



Si n-p-n epitaxial type with an attached heat radiator for printed-circuit-board use in audio, ultrasonic, and rf circuits and in low-distortion power amplifiers, oscillators, switching regulators, series regulators, converters, and inverters. JEDEC TO-66 (with heat radiator), Outline No.26. This type is identical with type 2N3878 except for the following items:

2N3878 except for the following items:

MAXIMUM RATINGS

Transistor Dissipation:

T_A up to 25°C	P_T	5.8	W
T_A above 25°C	P_T	See curve page 300	

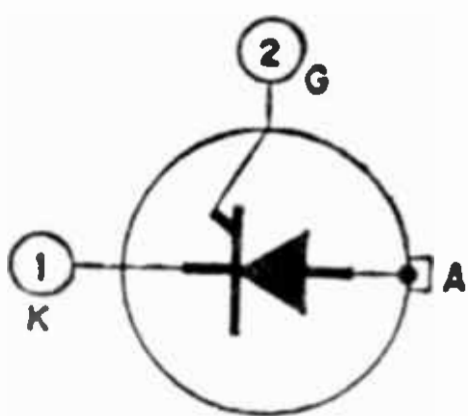
CHARACTERISTICS (At case temperature = 25°C)

Thermal Resistance, Junction-to-Ambient	θ_{J-A}	30 max	°C/W
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SILICON CONTROLLED RECTIFIERS

40378

40379



Si all-diffused three-junction types for use in power-control and power-switching applications. Outline No.35:

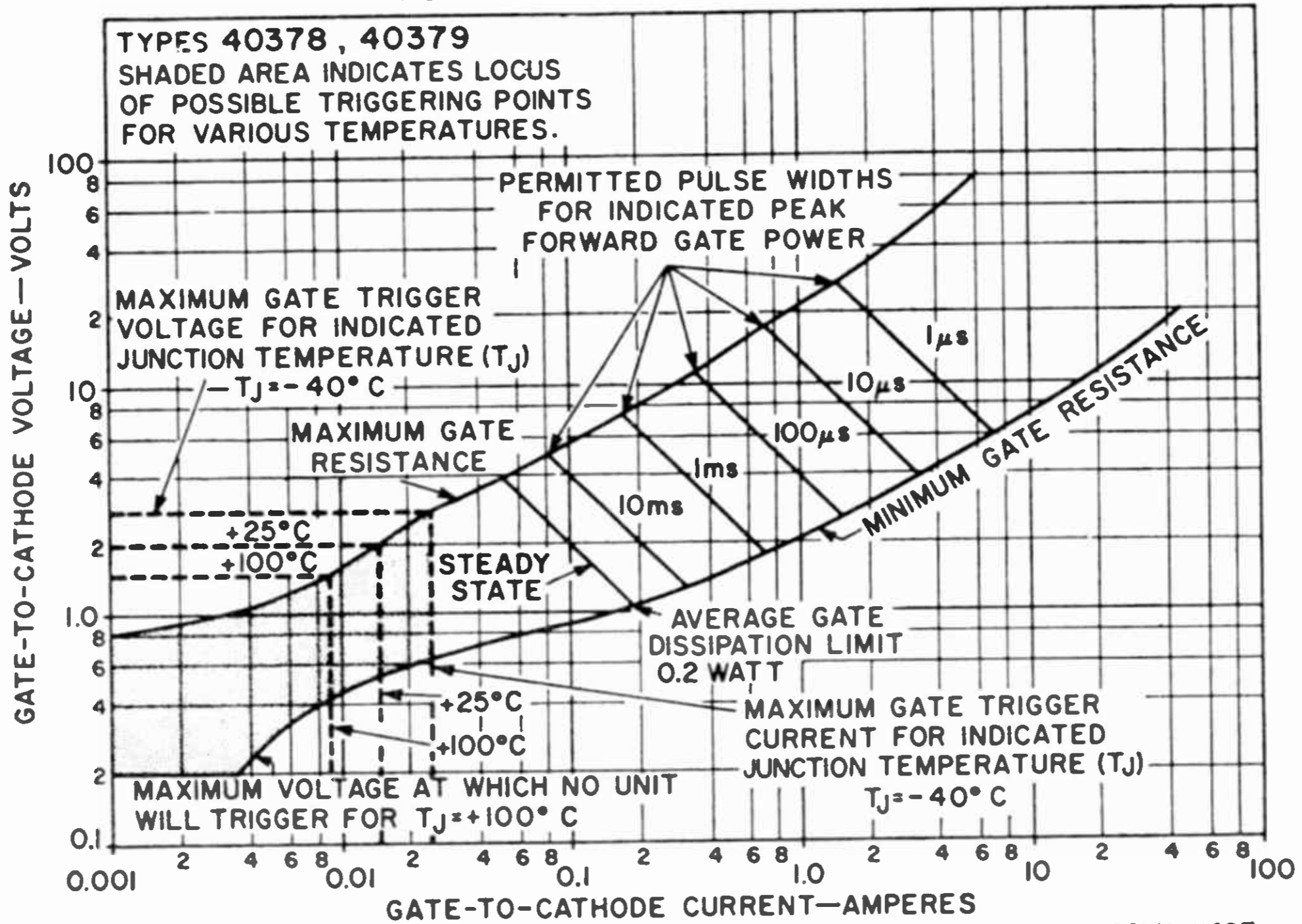
MAXIMUM RATINGS (For sinusoidal ac supply voltage at f = 50 to 400 Hz with resistive or inductive load)

	40378	40379	
V_{RSOM}	330	660	V
V_{RROM}	200	400	V
V_{DROM}	_____	600	V
$I_{T(AV)}$ (conduction angle = 180°, $T_c = 60^\circ C$)	_____	4.5	A
$I_{T(RMS)}$	_____	7	A
I_{TSM} (1 cycle of principle voltage)	_____	80	A
P_{GM} (peak, forward or reverse, for 10 μs)	_____	13	W
$P_{G(AV)}$	_____	0.2	W
T_{stg}	_____	-40 to 150	°C
T_C	_____	-40 to 100	°C

CHARACTERISTICS (At maximum electrical rating at $T_c = 25^\circ\text{C}$)

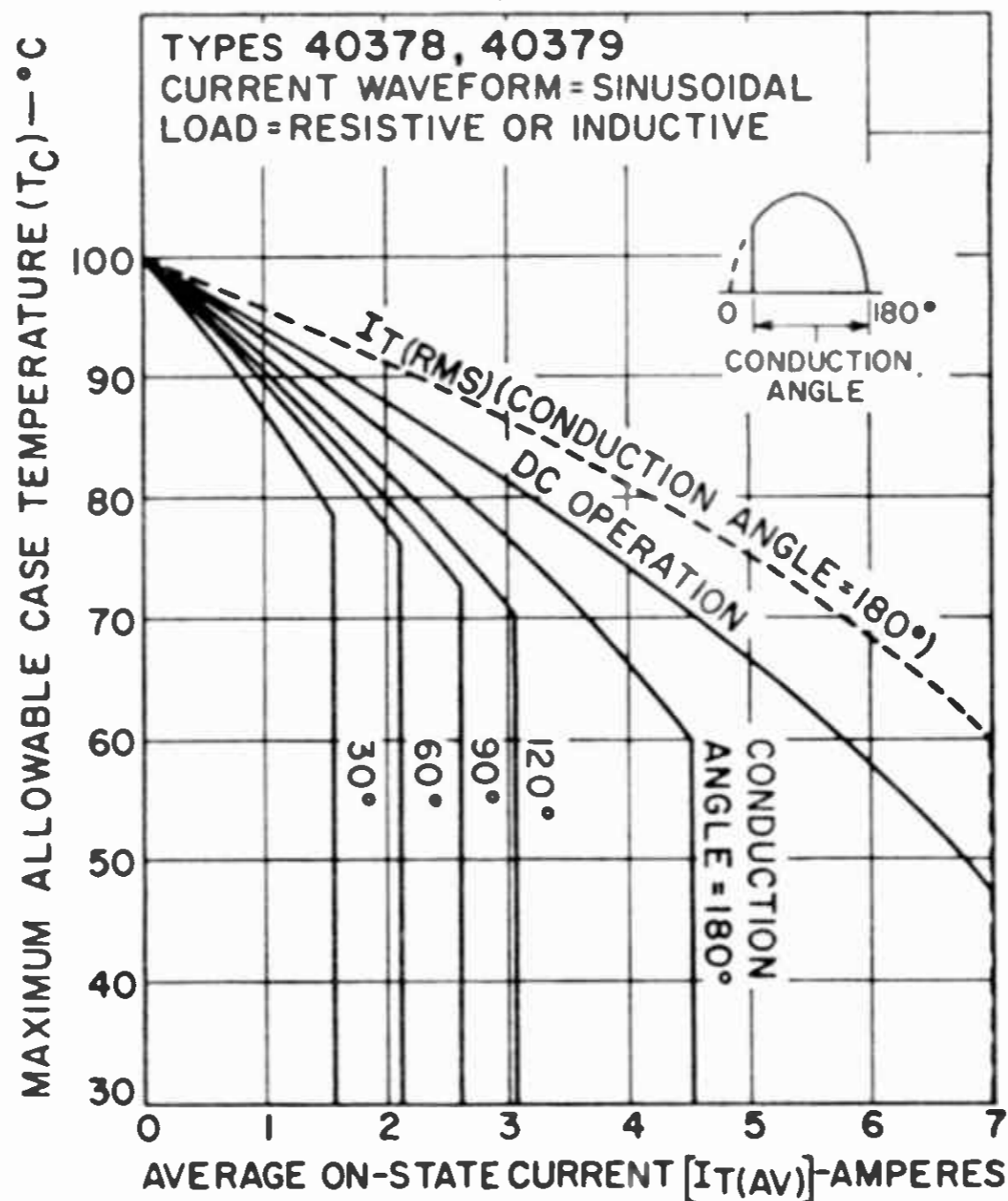
	40378	40379	
$V_{F(BO)O}$ ($T_c = 100^\circ\text{C}$)	200 min	400 min	V
I_{DOM} ($T_c = 100^\circ\text{C}$, $V_D = V_{F(BO)O}$ min value)	0.1 typ	0.2 typ	mA
I_{RRM} ($T_c = 100^\circ\text{C}$, $V_{RO} = V_{RRM}$)	1 max	2 max	mA
V_T (on-state current = 30 A)	0.05 typ	0.1 typ	mA
I_{GT}	0.5 max	1 max	mA
V_{GT}	_____ 1.9 typ; 2.5 max _____	_____ 8 typ; 15 max _____	V (dc)
i_{HO}	_____ 1.2 typ; 2 max _____	_____ 12 _____	V (dc)
Critical dv/dt ($V_D = V_{F(BO)O}$ min value, exponential rise, $T_c = 100^\circ\text{C}$)	10 min	20 min	$V/\mu\text{s}$
θ_{J-C}	200 typ	200 typ	$V/\mu\text{s}$
	_____ 5 max _____		$^\circ\text{C/W}$

FORWARD GATE CHARACTERISTICS



92LM-1148T

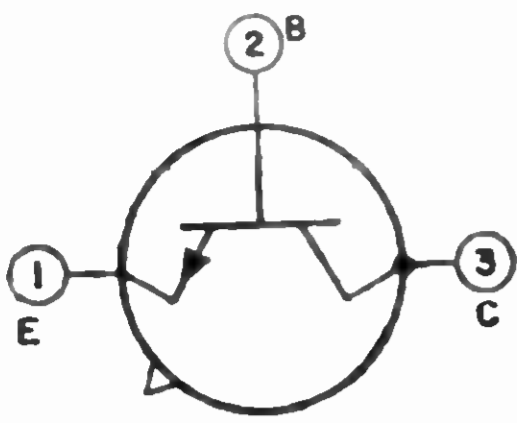
RATING CHART (CASE TEMPERATURE)



92LM-1151T

POWER TRANSISTOR

40385



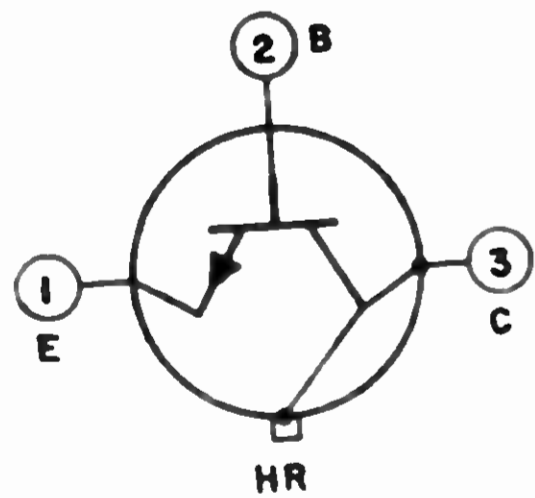
Si n-p-n triple-diffused type subjected to special pre-conditioning and reliability tests for high-reliability operation in high-power switching and amplifier applications in military and industrial equipment. JEDEC TO-5, Outline No.5. This type is a high-reliability version of type 2N3439.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	450	V
Collector-to-Emitter Voltage	V_{CEO}	350	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Collector Current	I_C	1	A
Transistor Dissipation:			
T_A up to 25°C	P_T	1	W
T_C up to 25°C	P_T	5	W
T_A or T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	255	°C

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_C = 50$ mA, $I_B = 0$)	V_{CEO} (sus)	350 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 50$ mA, $I_B = 4$ mA)	V_{CE} (sat)	0.5 max	V
Base-to-Emitter Saturation Voltage ($I_C = 50$ mA, $I_B = 4$ mA)	V_{BE} (sat)	1.3 max	V
Collector-Cutoff Current:			
$V_{CE} = 300$ V, $I_B = 0$	I_{CEO}	20 max	μ A
$V_{CE} = 450$ V, $V_{BE} = -1.5$ V	I_{CEV}	500 max	μ A
Emitter-Cutoff Current ($V_{EB} = 6$ V, $I_C = 0$)	I_{EBO}	20 max	μ A
Static Forward-Current Transfer Ratio:			
$V_{CE} = 10$ V, $I_C = 20$ mA	h_{FE}	40 to 160	
$V_{CE} = 10$ V, $I_C = 2$ mA	h_{FE}	30 min	



POWER TRANSISTOR

40389

Si n-p-n triple-diffused planar type with an attached heat radiator for printed-circuit-board use in a wide variety of small-signal, medium-power applications (up to 20 MHz) in commercial and industrial equipment. JEDEC TO-5 (with heat radiator), Outline No.8. This type is identical with type 2N3053 except for the

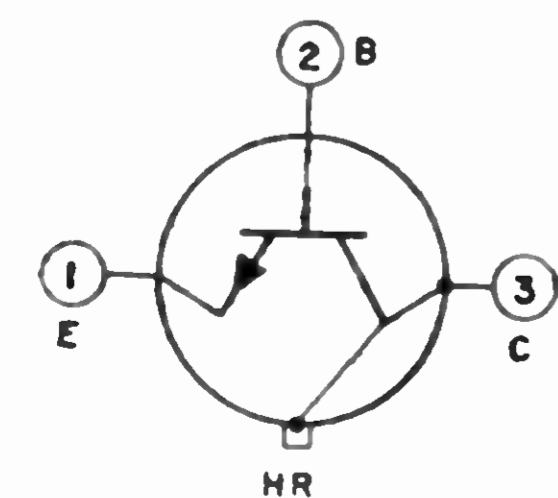
following items:

MAXIMUM RATINGS

Transistor Dissipation:			
T_A up to 25°C	P_T	3.5	W
T_A above 25°C	P_T	See curve page 300	

CHARACTERISTICS (At case temperature = 25°C)

Thermal Resistance, Junction-to-Ambient	θ_{J-A}	50 max	°C/W
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TRANSISTOR

40390

Si n-p-n triple-diffused type with an attached heat radiator for printed-circuit-board use in high-speed switching and linear amplifier applications such as high-voltage differential and operational amplifiers, high-voltage inverters, and series regulators for industrial and military applications. JEDEC TO-5 (with

heat radiator), Outline No.8. This type is identical with type 2N3440 except for the following items:

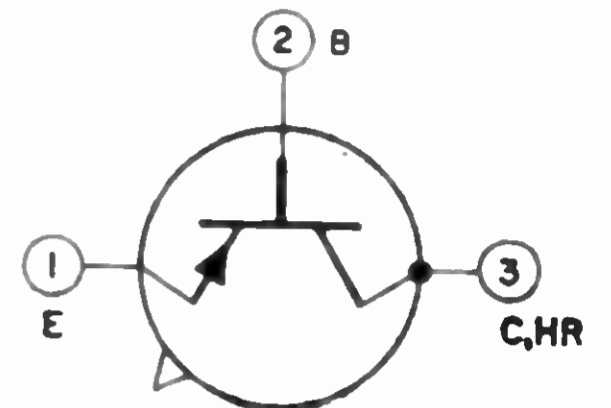
MAXIMUM RATINGS

Transistor Dissipation:

T_A up to 25°C	P_T	3.5	W
T_A above 25°C	P_T	See curve	page 300

40391 POWER TRANSISTOR

Si p-n-p double-diffused epitaxial planar type with an attached heat radiator for printed-circuit-board use in a wide variety of small-signal, medium-power applications in military, industrial, and commercial equipment. JEDEC TO-5 (with heat radiator), Outline No.8. This type is identical with type 2N4037 except for the following items:



MAXIMUM RATINGS

Transistor Dissipation:

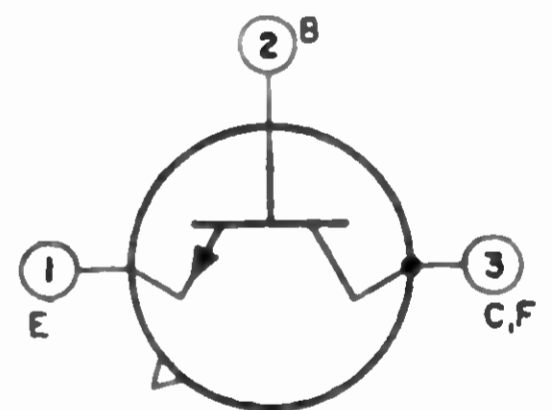
T_A up to 25°C	P_T	3.5	W
T_A above 25°C	P_T	See curve	page 300

CHARACTERISTICS (At case temperature = 25°C)

Thermal Resistance, Junction-to-Ambient	θ_{J-A}	50 max	°C/W
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40392 POWER TRANSISTOR

Si n-p-n triple-diffused planar type features a base comprised of a homogeneous-resistivity silicon material. This type is used in a wide variety of small-signal, medium-power applications at frequencies up to 20 MHz. JEDEC TO-5 (with flange), Outline No.6. See Mounting Hardware for desired mounting arrangement. This type is identical with type 2N3053 except for the following items:



MAXIMUM RATINGS

Transistor Dissipation:

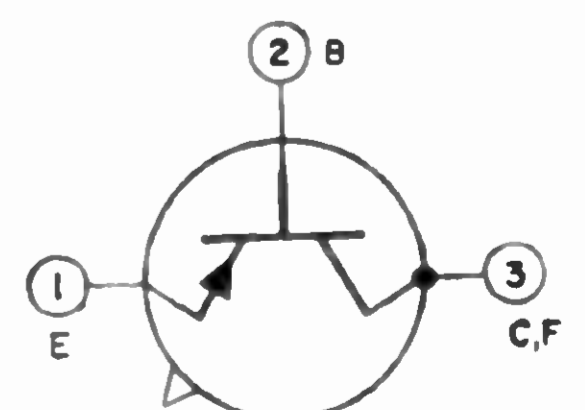
T_c up to 25°C	P_T	7	W
T_c above 25°C	P_T	See curve	page 300

CHARACTERISTICS (At case temperature = 25°C)

Thermal Resistance, Junction-to-Case	θ_{J-C}	25 max	°C/W
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40394 POWER TRANSISTOR

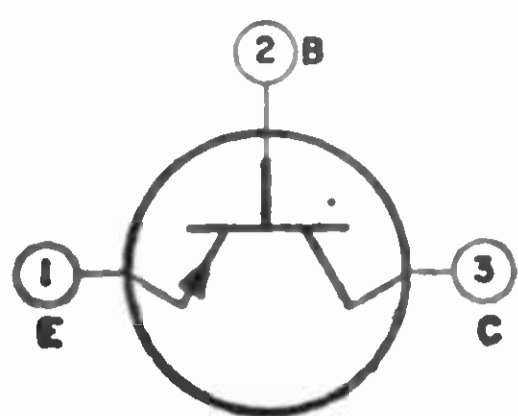
Si p-n-p double-diffused epitaxial planar type used in a wide variety of small-signal, medium-power applications in military, industrial, and commercial equipment. JEDEC TO-5 (with flange), Outline No.6. See Mounting Hardware for desired mounting arrangement. This type is identical with type 2N4037 except for the following items:



MAXIMUM RATINGS

Transistor Dissipation:

T_A up to 25°C	P_T	1	W
T_A above 25°C	P_T	See curve	page 300



TRANSISTOR

40395

Ge p-n-p alloy-junction type used in high-gain low-level audio stages. JEDEC TO-1, Outline No.1.

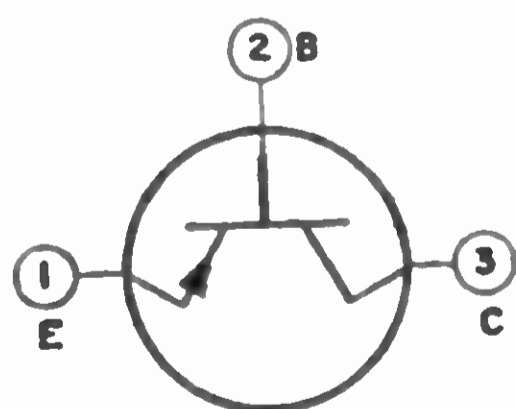
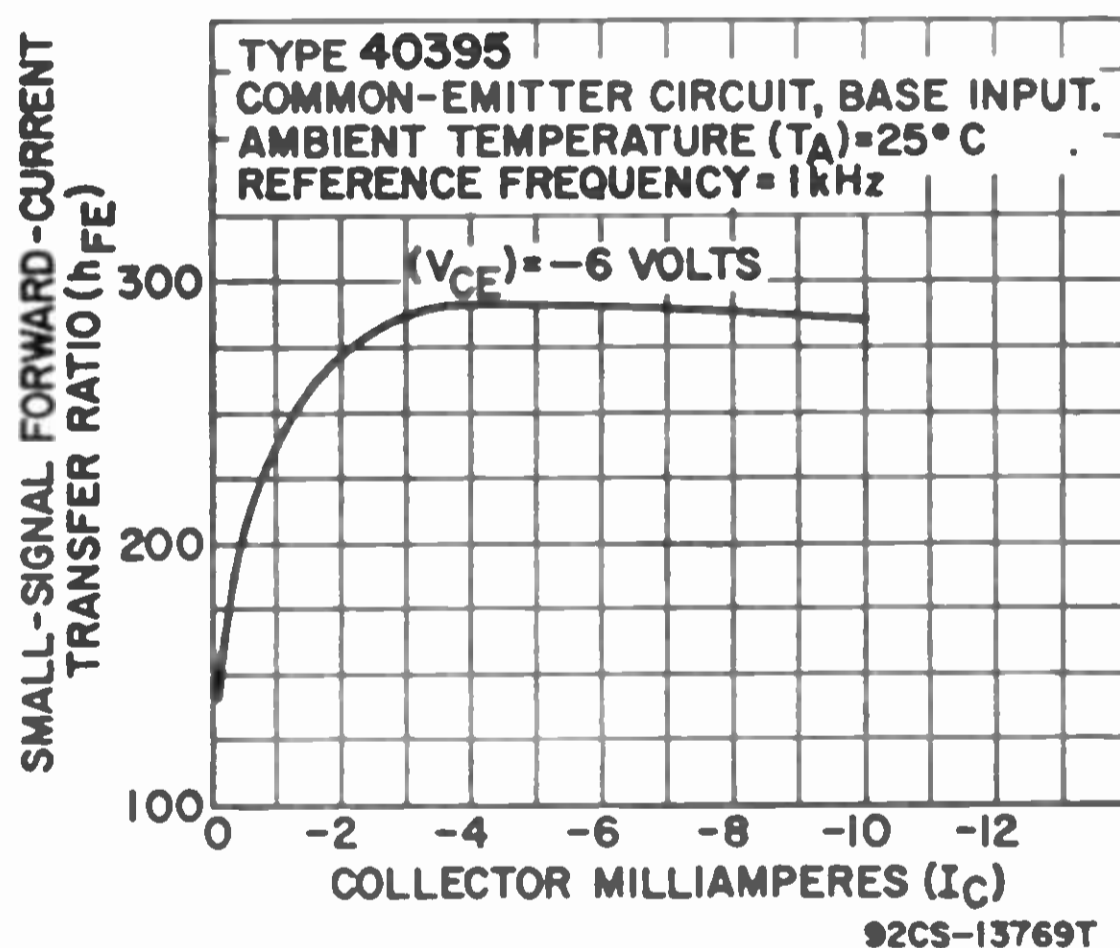
MAXIMUM RATINGS

Collector-to-Base Voltage	V _{CBO}	-20	V
Collector-to-Emitter Voltage (R _{BE} ≤ 4.7 kΩ)	V _{CER}	-18	V
Emitter-to-Base Voltage	V _{EBO}	-20	V
Collector Current	I _C	-50	mA
Transistor Dissipation:			
T _A up to 55°C	P _T	120	mW
T _A above 55°C	P _T	See curve page 300	
Temperature Range:			
Operating (Junction)	T _J (opr)	-65 to 100	°C
Storage	T _{STG}	-65 to 100	°C
Lead-Soldering Temperature (10 s max)	T _L	255	°C

CHARACTERISTICS

Collector-to-Emitter Breakdown Voltage (I _C = -1 mA, I _B = 0, R _{BE} = 10 kΩ)	V _{(BR)CER}	-18 min	V
Collector-Cutoff Current (V _{CB} = -20 V, I _E = 0)	I _{CBO}	-12 max	μA
Emitter-Cutoff Current (V _{EB} = 20 V, I _C = 0)	I _{EBO}	-12 max	μA
Noise Current (V _{CE} = -6 V, I _C = -1 mA, f = 0.05 to 15 kHz)		10 max	nA
Small-Signal Forward-Current Transfer Ratio (V _{CE} = -6 V, I _C = -1 mA)	h _{re}	170 min	
Small-Signal Forward-Current Transfer-Ratio Cutoff Frequency (V _{CE} = -6 V, I _C = -1 mA)	f _{hfb}	10	MHz

TYPICAL SMALL-SIGNAL FORWARD-CURRENT TRANSFER-RATIO CHARACTERISTIC



POWER TRANSISTORS (Matched Pair)

40396

Ge p-n-p and Ge n-p-n types, in separate packages, with matched characteristics for use in complementary symmetry af output-amplifier stages. JEDEC TO-1, Outline No.1.

MAXIMUM RATINGS

		p-n-p	n-p-n	
Collector-to-Base Voltage	V _{CBO}	-18	18	V
Collector-to-Emitter Voltage (R _{BE} ≤ 4.7 kΩ)	V _{CER}	-18	18	V
Emitter-to-Base Voltage	V _{EBO}	-2.5	2.5	V

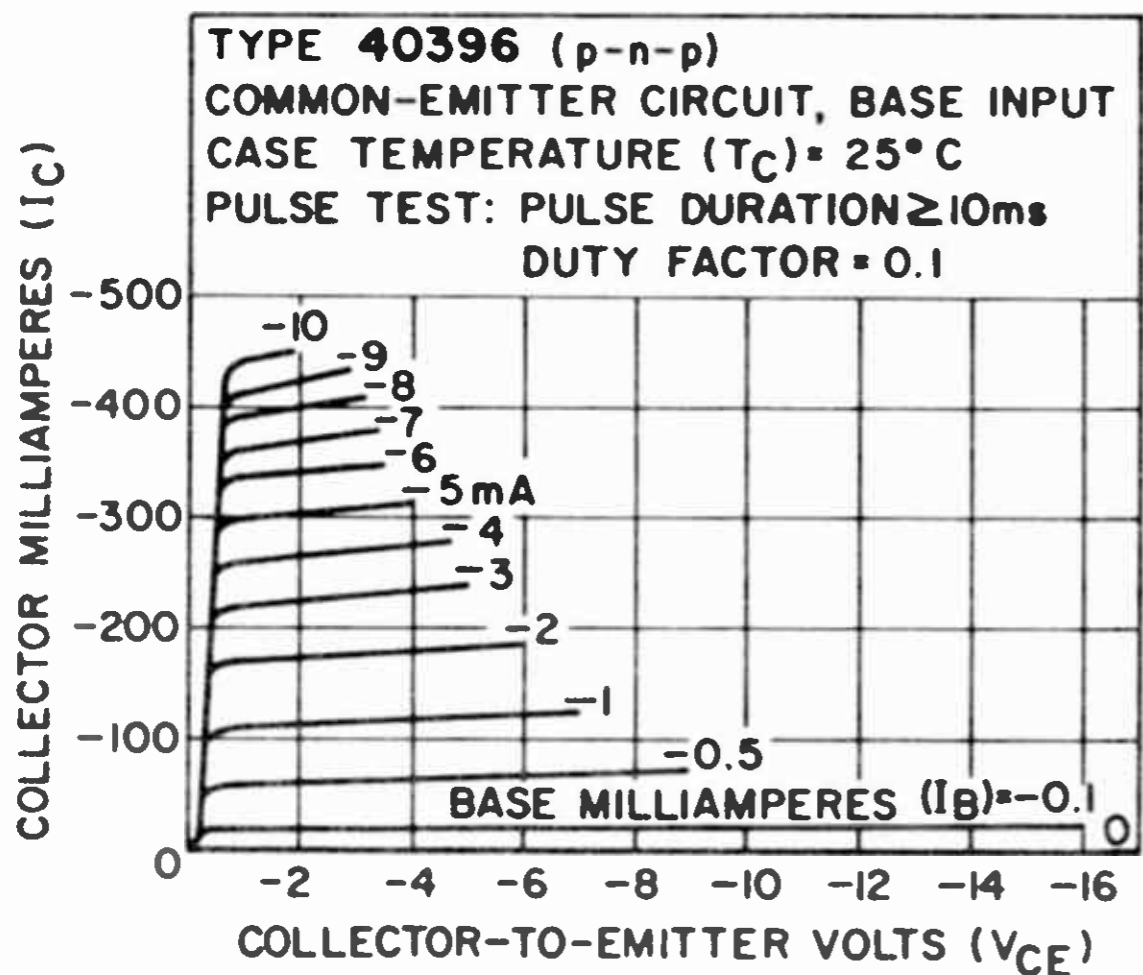
MAXIMUM RATINGS (cont'd)

Collector Current	I_C	<i>p-n-p</i> -500	<i>n-p-n</i> 500	mA
Transistor Dissipation:				
T_C up to 55°C	P_T	300	300	mW
T_C above 55°C	P_T	See curve page 300		
Temperature Range:				
Operating (Junction)	T_J (opr)	-65 to 85		°C
Storage	T_{STG}	-65 to 85		°C
Lead-Soldering Temperature	T_L	255	255	°C

CHARACTERISTICS

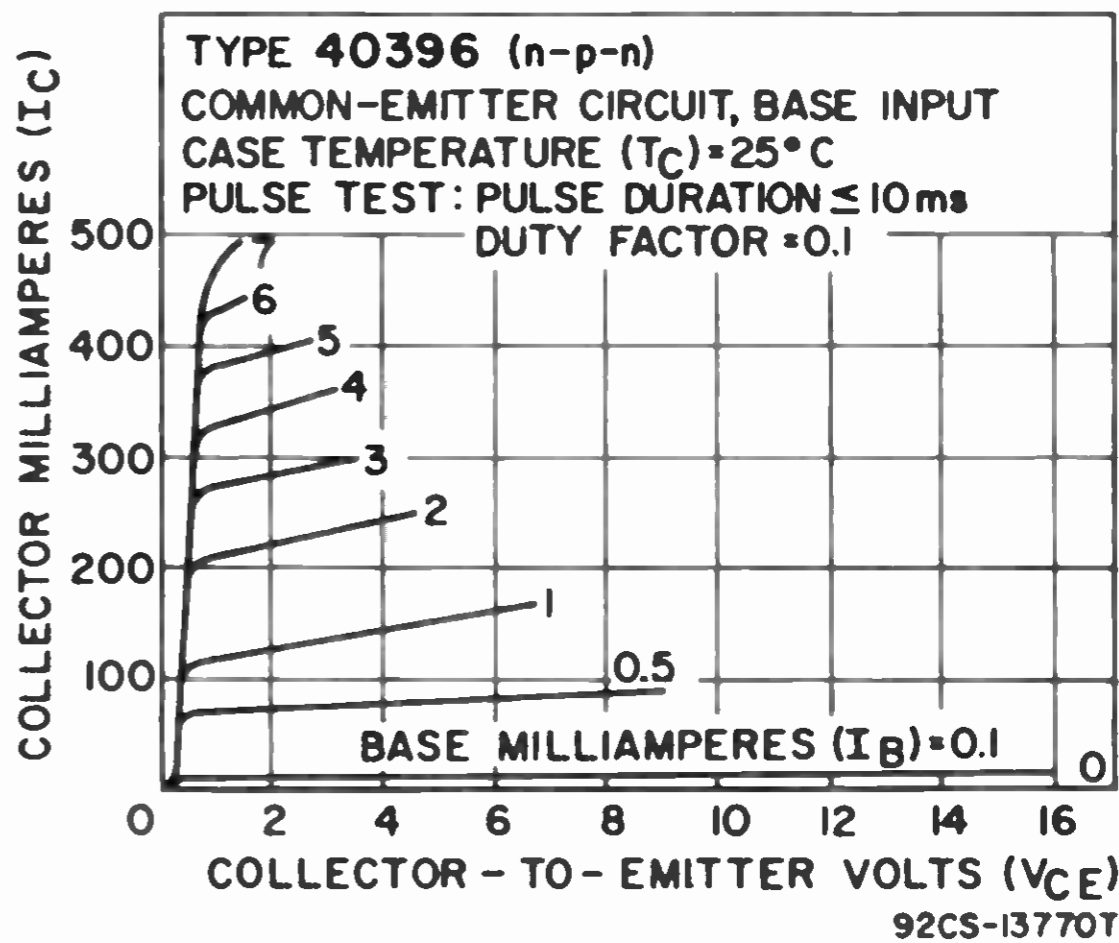
Collector-to-Emitter Breakdown Voltage:				
$I_C = -1$ mA, $R_{BE} = 4.7$ kΩ	$V_{(BR)CER}$	-18 min		V
$I_C = 1$ mA, $R_{BE} = 4.7$ kΩ	$V_{(BR)CER}$		18 min	V
Collector-to-Emitter Saturation Voltage:				
$I_C = -250$ mA, $I_B = -25$ mA	$V_{CE(sat)}$	-0.5 max		V
$I_C = 250$ mA, $I_B = 25$ mA	$V_{CE(sat)}$		0.5 max	V
Collector-Cutoff Current:				
$V_{CB} = -12$ V, $I_E = 0$	I_{CBO}	-14 max		μA
$V_{CB} = 12$ V, $I_E = 0$	I_{CBO}		14 max	μA
Emitter-Cutoff Current:				
$V_{EB} = -2.5$ V, $I_C = 0$	I_{EBO}	-14 max		μA
$V_{EB} = 2.5$ V, $I_C = 0$	I_{EBO}		14 max	μA
Static Forward-Current Transfer Ratio:				
$V_{CE} = -1$ V, $I_C = -50$ mA	h_{FE}	50 min	50 min	
$V_{CE} = 1$ V, $I_C = 50$ mA	h_{FE}			
$V_{CE} = -1$ V, $I_C = -250$ mA	h_{FE}	30 min		
$V_{CE} = 1$ V, $I_C = 250$ mA	h_{FE}		30 min	
Small-Signal Forward-Current Transfer-Ratio				
Cutoff Frequency:				
$V_{CE} = -6$ V, $I_C = -1$ mA	f_{hfb}	1.5		MHz
$V_{CE} = 6$ V, $I_C = 1$ mA	f_{hfb}		2	MHz

TYPICAL COLLECTOR CHARACTERISTICS



92CS-13771T

TYPICAL COLLECTOR CHARACTERISTICS

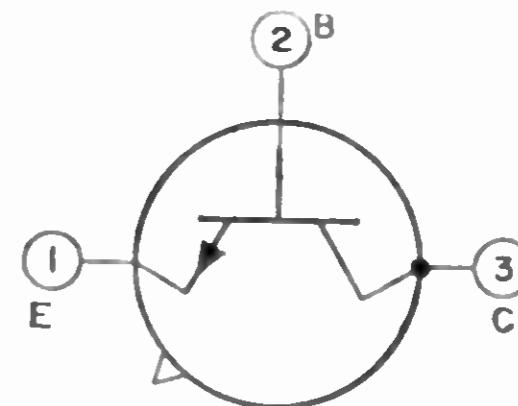


92CS-13770T

40397

TRANSISTOR

Si n-p-n epitaxial planar type used in high-voltage, high-current audio and video amplifier service in commercial and industrial equipment. JEDEC TO-104, Outline No.32.



MAXIMUM RATINGS

Collector-to-Emitter Voltage:			
Base open	V_{CEO}	25	V
$V_{BE} = -1$ V	V_{CEV}	25	V
Emitter-to-Base Voltage	V_{EBO}	7.5	V
Collector Current	I_C	200	mA
Emitter Current	I_E	-200	mA

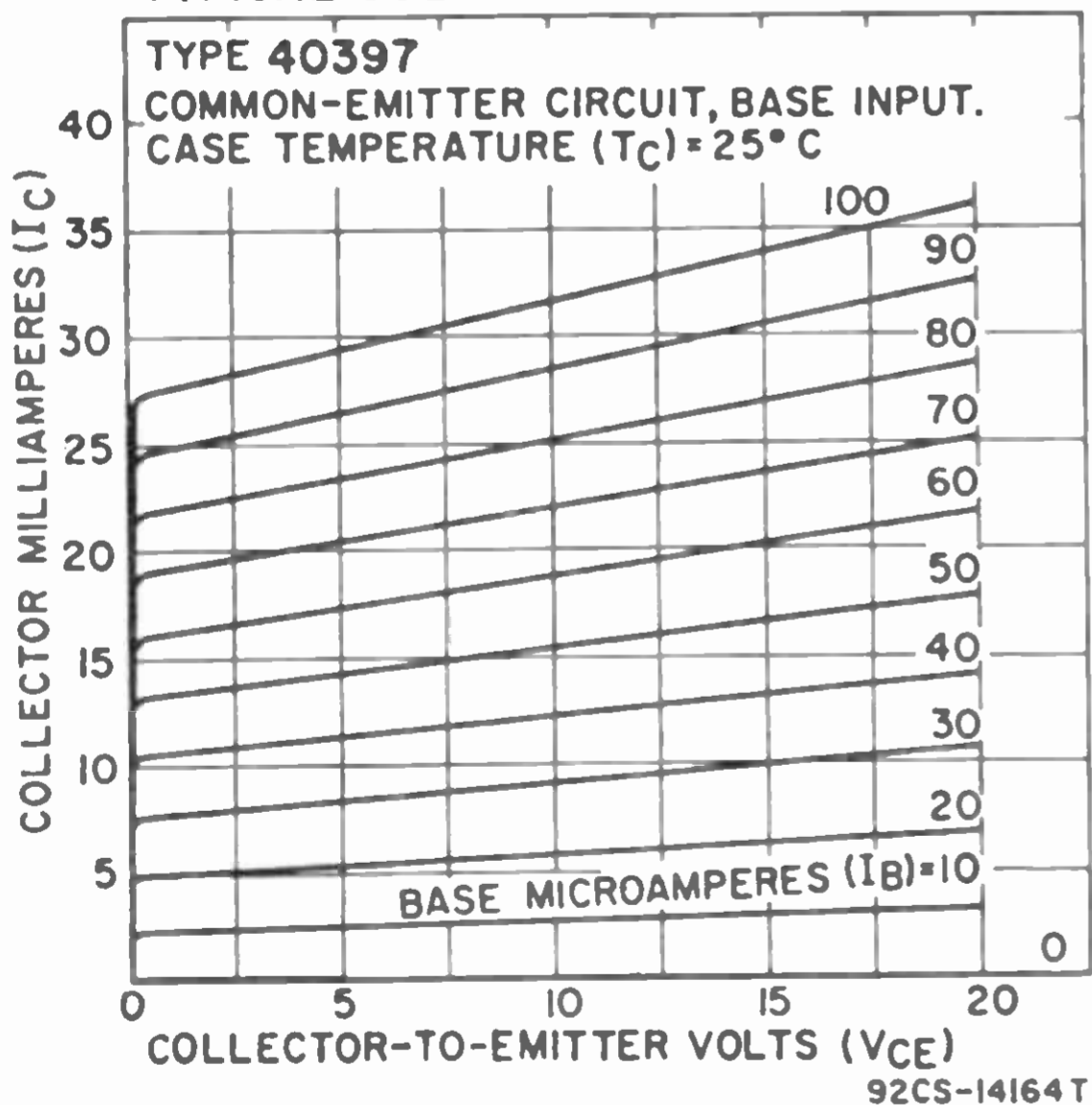
MAXIMUM RATINGS (cont'd)

Base Current	I_B	25	mA
Transistor Dissipation:			
T_A up to 25°C	P_T	0.5	W
T_C up to 75°C	P_T	2	W
T_A or T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 175	°C
Storage	T_{STG}	-65 to 175	°C
Lead-Soldering Temperature (10 s max)	T_L	255	°C

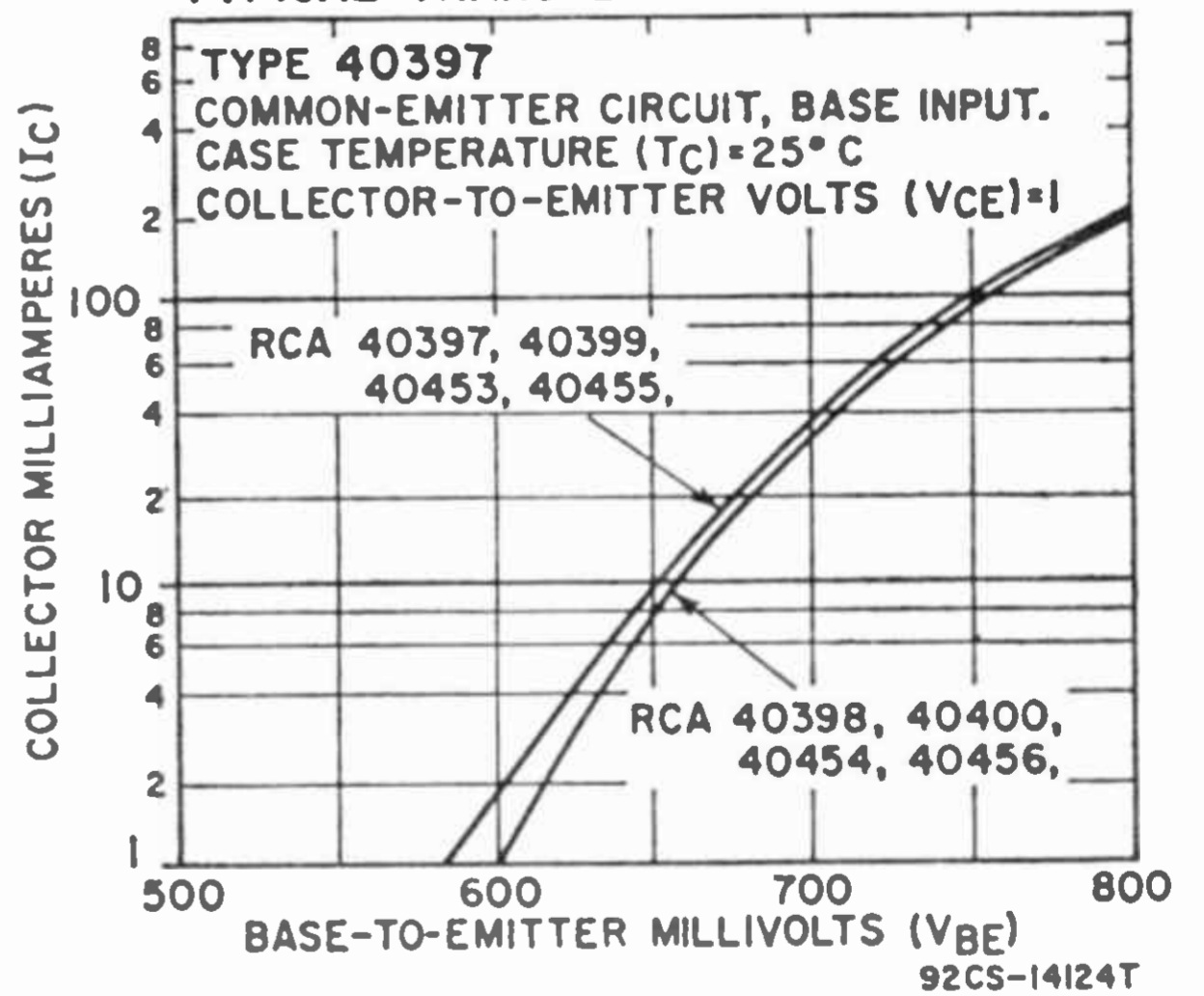
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Breakdown Voltage ($I_C = 10$ mA, $I_B = 0$)	$V_{(BR)CEO}$	25 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.05$ mA, $I_C = 0$)	$V_{(BR)EBO}$	7.5 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 200$ mA, $I_B = 10$ mA)	$V_{CE(\text{sat})}$	0.15 typ; 0.25 max	V
Base-to-Emitter Saturation Voltage ($I_C = 200$ mA, $I_B = 10$ mA)	$V_{BE(\text{sat})}$	0.8 typ; 1.3 max	V
Collector-Cutoff Current:			
$V_{CB} = 25$ V, $I_E = 0$	I_{CBO}	100 max	nA
$V_{CB} = 25$ V, $I_E = 0$, $T_C = 85^\circ\text{C}$	I_{CBO}	5 max	μA
$V_{CE} = 25$ V, $V_{BE} = -1$ V	I_{CEV}	10 max	μA
Emitter-Cutoff Current ($V_{BE} = -2.5$ V, $I_C = 0$)	I_{EBO}	100 max	nA
Static Forward-Current Transfer Ratio:			
$V_{CE} = 6$ V, $I_C = 0.5$ mA	h_{FE}	20 min; 175 typ	
$V_{CE} = 10$ V, $I_C = 10$ mA	h_{FE}	165 to 600	
$V_{CE} = 1$ V, $I_C = 100$ mA	h_{FE}	100 min; 245 typ	
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 12$ V, $I_C = 10$ mA, $f = 1$ kHz)	h_{fe}	165 min; 375 typ	
Gain-Bandwidth Product ($V_{CE} = 6$ V, $I_C = 1$ mA, $f = 100$ MHz)	f_T	50 min; 80 typ	MHz
Intrinsic Base-Spreading Resistance ($V_{CE} = 6$ V, $I_C = 1$ mA, $f = 100$ MHz)	$r_{bb'}$	20 typ; 40 max	Ω
Output Capacitance ($V_{CB} = 6$ V, $I_E = 0$, $f = 1$ MHz)	C_{ob0}	12 typ; 20 max	pF
Small-Signal Input Impedance ($V_{CE} = 12$ V, $I_C = 10$ mA, $f = 1$ kHz)	h_{ie}	1200	Ω
Small-Signal Output Admittance ($V_{CE} = 12$ V, $I_C = 10$ mA, $f = 1$ kHz)	h_{oe}	120	μmhos
Small-Signal Reverse-Voltage Transfer Ratio ($V_{CE} = 12$ V, $I_C = 10$ mA, $f = 1$ kHz)	h_{re}	250×10^{-6}	
Thermal Resistance, Junction-to-Case	θ_{J-C}	50 max	°C/W
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	300 max	°C/W

TYPICAL COLLECTOR CHARACTERISTICS

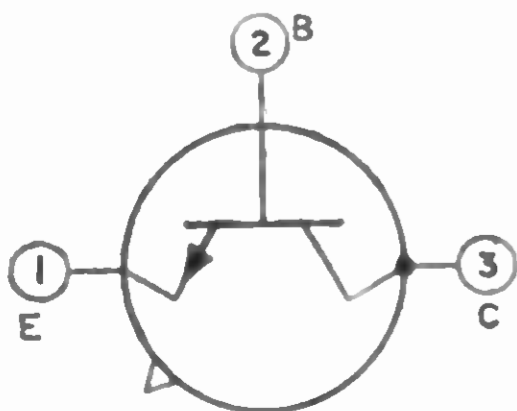


TYPICAL TRANSFER CHARACTERISTICS



TRANSISTOR

40398



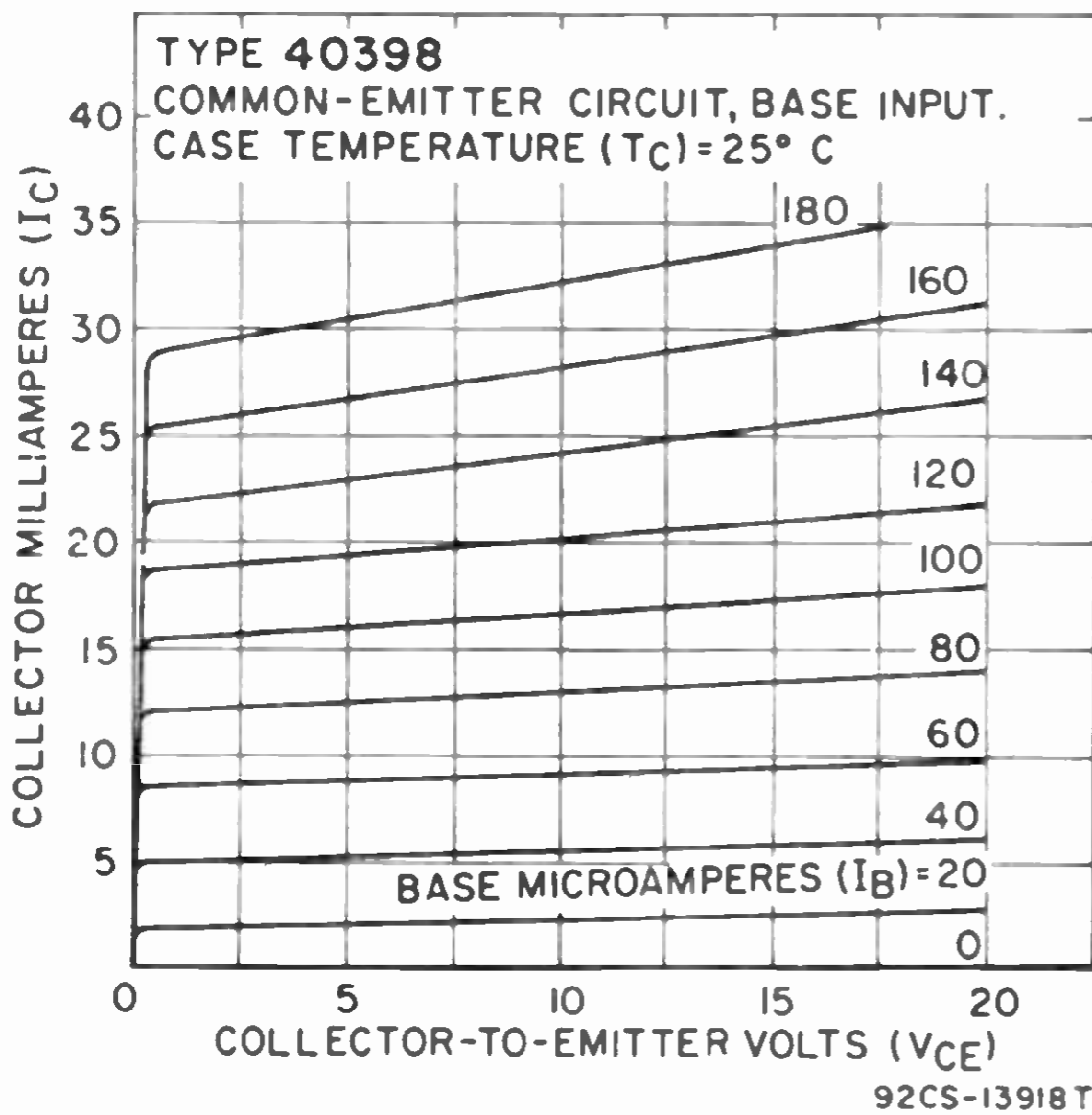
Si n-p-n epitaxial planar type used in high-voltage, high-current audio and video amplifier service in commercial and industrial equipment. JEDEC TO-104, Outline No.32. This type is identical with type 40397 except for the following items:

CHARACTERISTICS (At case temperature = 25°C)

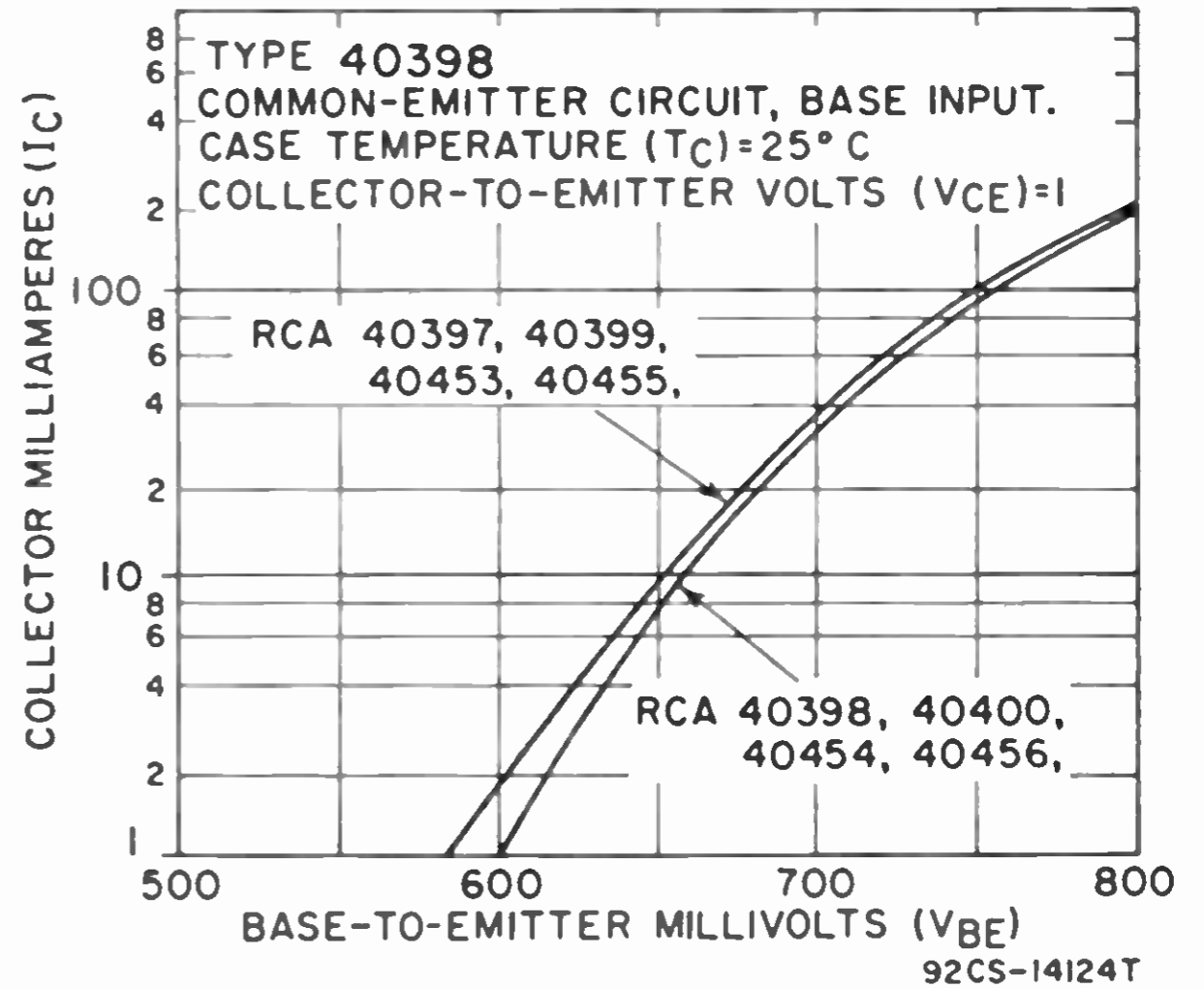
Static Forward-Current Transfer Ratio:

$V_{CE} = 6\text{ V}, I_C = 0.5\text{ mA}$	h_{FE}	20 min; 75 typ
$V_{CE} = 10\text{ V}, I_C = 10\text{ mA}$	h_{FE}	75 to 300
$V_{CE} = 1\text{ V}, I_C = 100\text{ mA}$	h_{FE}	50 min; 140 typ
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 12\text{ V}, I_C = 10\text{ mA}, f = 1\text{ kHz}$)	h_{fe}	75 min; 200 typ
Small-Signal Input Impedance ($V_{CE} = 12\text{ V},$ $I_C = 10\text{ mA}, f = 1\text{ kHz}$)	h_{ie}	600 Ω
Small-Signal Output Admittance ($V_{CE} = 12\text{ V},$ $I_C = 10\text{ mA}, f = 1\text{ kHz}$)	h_{oe}	75 μmhos
Small-Signal Reverse-Voltage Transfer Ratio ($V_{CE} = 12\text{ V}, I_C = 10\text{ mA}, f = 1\text{ kHz}$)	h_{re}	125×10^{-6}

TYPICAL COLLECTOR CHARACTERISTICS



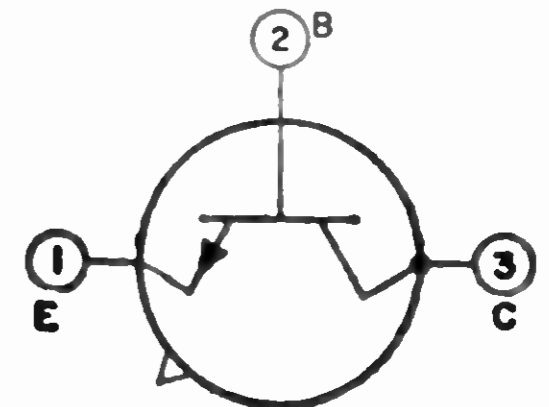
TYPICAL TRANSFER CHARACTERISTICS



40399

TRANSISTOR

Si n-p-n epitaxial planar type used in high-voltage, high-current audio and video amplifier service in commercial and industrial equipment. JEDEC TO-104, Outline No.32.



MAXIMUM RATINGS

Collector-to-Emitter Voltage:

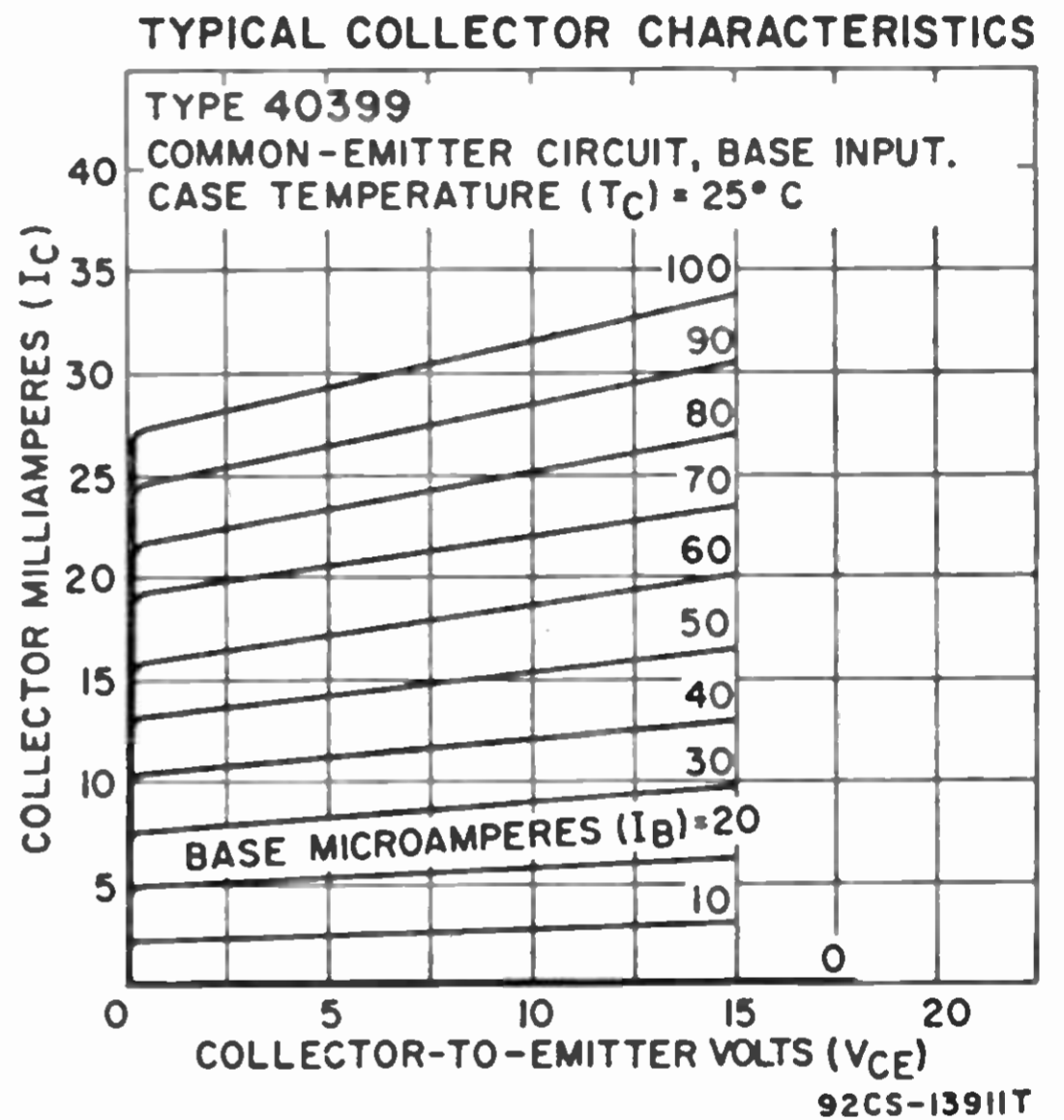
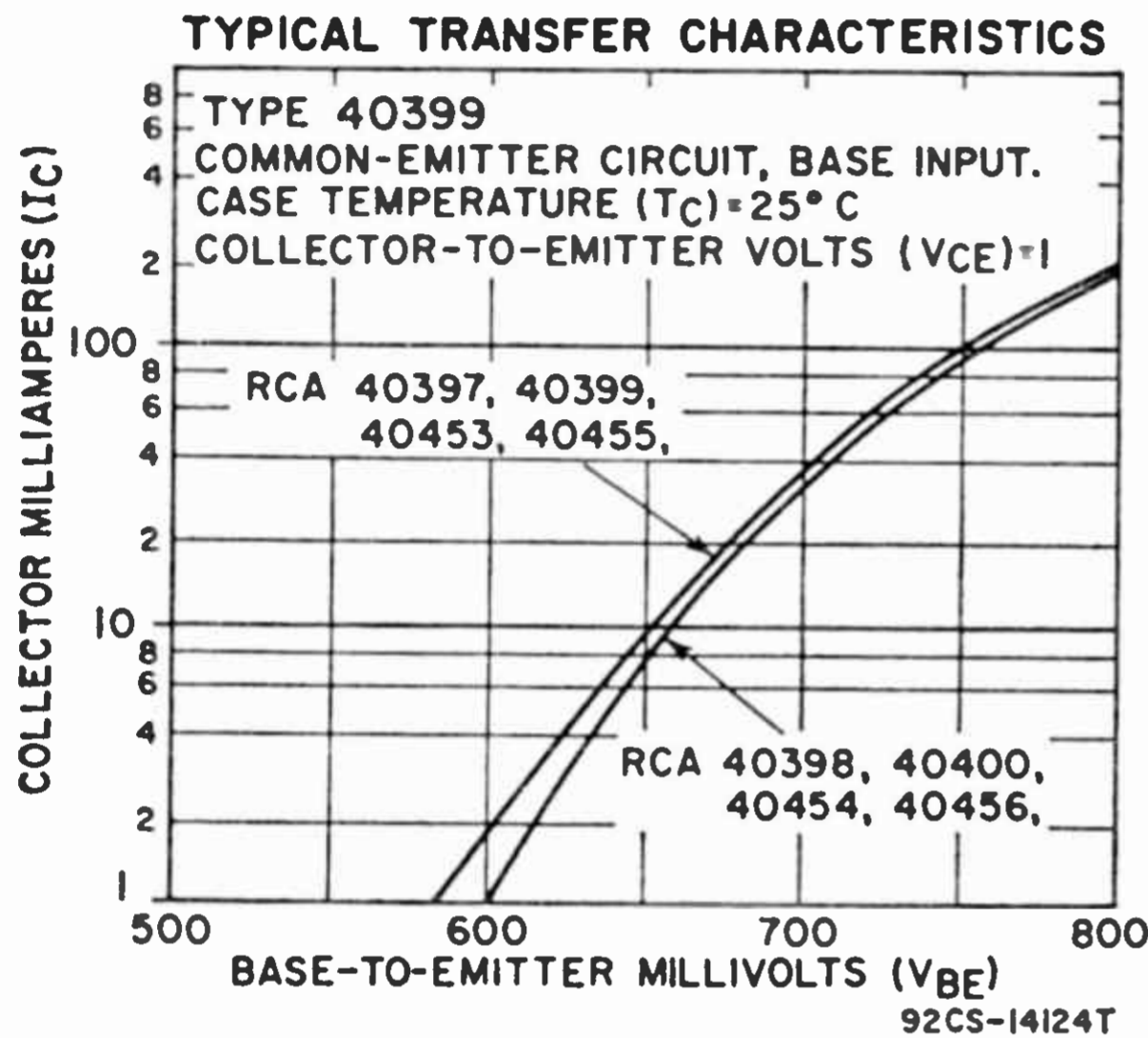
Base open	V_{CEO}	18	V
$V_{BE} = -1\text{ V}$	V_{CEV}	18	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Collector Current	I_C	200	mA
Emitter Current	I_E	-200	mA
Base Current	I_B	25	mA
Transistor Dissipation:			
T_A up to 25°C	P_T	0.5	W
T_C up to 75°C	P_T	2	W
T_A or T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 175	°C
Storage	T_{STG}	-65 to 175	°C
Lead-Soldering Temperature (10 s max)	T_L	255	°C

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Breakdown Voltage ($I_C = 10\text{ mA},$ $I_B = 0$)	$V_{(BR)CEO}$	18 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.05\text{ mA},$ $I_C = 0$)	$V_{(BR)EBO}$	7 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 100\text{ mA},$ $I_B = 5\text{ mA}$)	$V_{CE(\text{sat})}$	0.1 typ; 0.2 max	V
Base-to-Emitter Saturation Voltage ($I_C = 100\text{ mA},$ $I_B = 5\text{ mA}$)	$V_{BE(\text{sat})}$	0.75 typ; 1.3 max	V
Collector-Cutoff Current:			
$V_{CB} = 12\text{ V}, I_E = 0$	I_{CBO}	500 max	nA
$V_{CB} = 12\text{ V}, I_E = 0, T_C = 85^\circ\text{C}$	I_{CBO}	10 max	μA

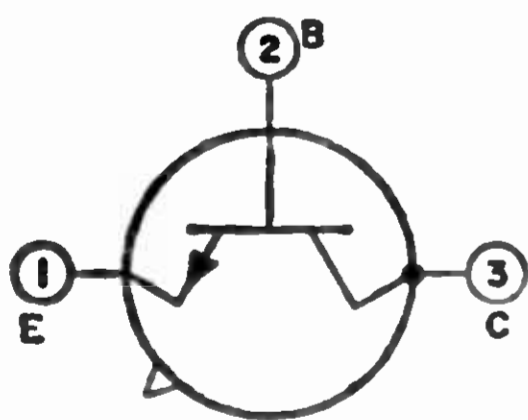
CHARACTERISTICS (cont'd)

Emitter-Cutoff Current ($V_{BE} = -2.5$ V, $I_C = 0$)	I_{EBO}	500 max	nA
Static Forward-Current Transfer Ratio:			
$V_{CE} = 6$ V, $I_C = 0.5$ mA	h_{FE}	175	
$V_{CE} = 10$ V, $I_C = 10$ mA	h_{FE}	165 to 600	
$V_{CE} = 1$ V, $I_C = 100$ mA	h_{FE}	100 min; 245 typ	
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 12$ V, $I_C = 10$ mA, $f = 1$ kHz)	h_{fe}	165 min; 375 typ	
Gain-Bandwidth Product ($V_{CE} = 6$ V, $I_C = 1$ mA, $f = 100$ MHz)	f_T	50 typ; 80 max	MHz
Intrinsic Base-Spreading Resistance ($V_{CE} = 6$ V, $I_C = 1$ mA, $f = 100$ MHz)	$r_{bb'}$	20 typ; 40 max	Ω
Output Capacitance ($V_{CB} = 6$ V, $I_E = 0$, $f = 1$ MHz)	C_{obo}	12 typ; 20 max	pF
Small-Signal Input Impedance ($V_{CE} = 12$ V, $I_C = 10$ mA, $f = 1$ kHz)	h_{ie}	1200	Ω
Small-Signal Output Admittance ($V_{CE} = 12$ V, $I_C = 10$ mA, $f = 1$ kHz)	h_{oe}	120	μ mhos
Small-Signal Reverse-Voltage Transfer Ratio ($V_{CE} = 12$ V, $I_C = 10$ mA, $f = 1$ kHz)	h_{re}	250×10^{-6}	
Thermal Resistance, Junction-to-Case	θ_{J-C}	50 max	$^{\circ}C/W$
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	300 max	$^{\circ}C/W$

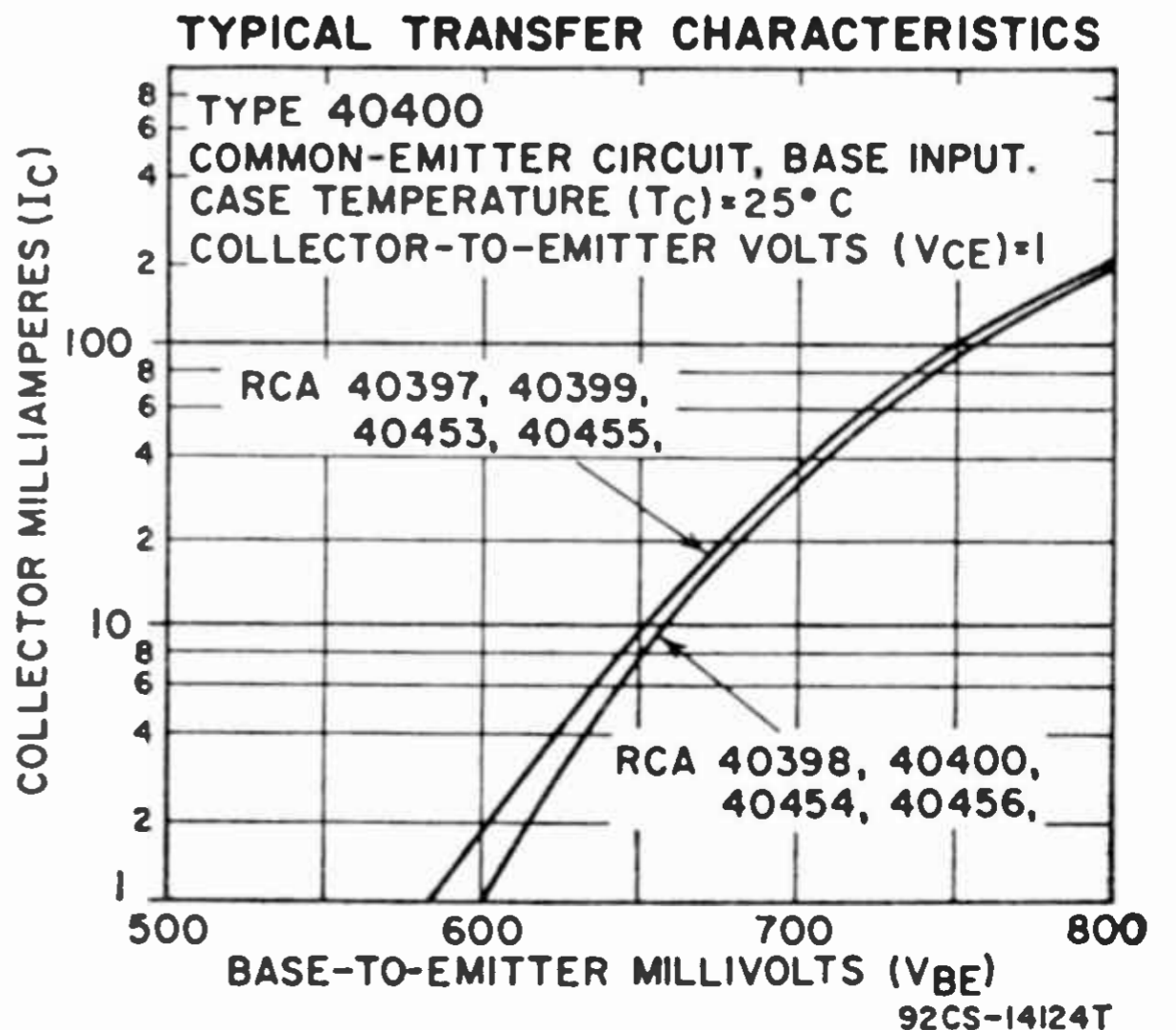
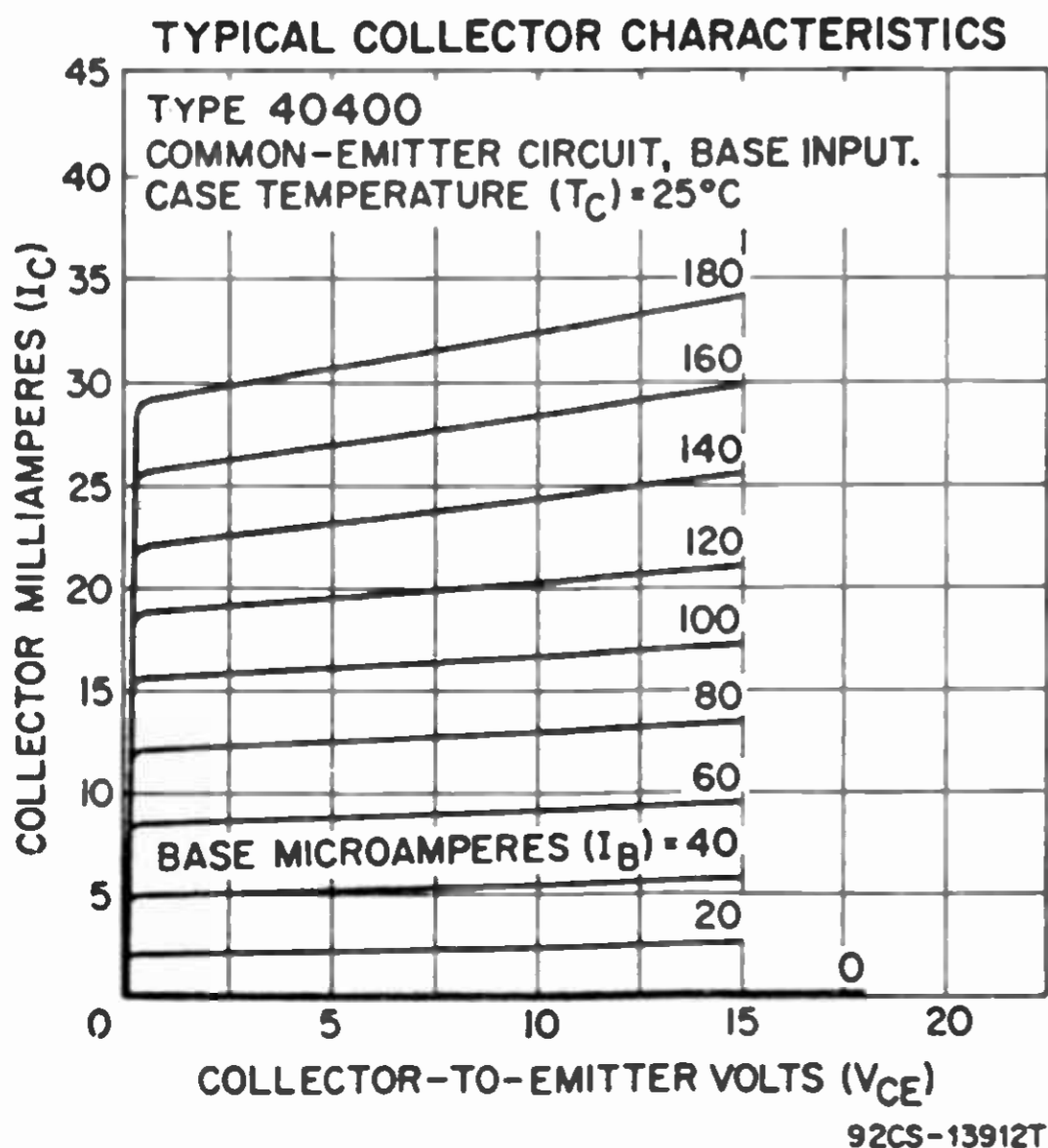


TRANSISTOR

40400



Si n-p-n epitaxial planar type used in high-voltage, high-current audio and video amplifier service in commercial and industrial equipment. JEDEC TO-104, Outline No.32. This type is identical with type 40399 except for the following items:



CHARACTERISTICS (At case temperature = 25°C)

Static Forward-Current Transfer Ratio:

$V_{CE} = 6\text{ V}, I_C = 0.5\text{ mA}$	h_{FE}	75	
$V_{CE} = 10\text{ V}, I_C = 10\text{ mA}$	h_{FE}	75 to 300	
$V_{CE} = 1\text{ V}, I_C = 100\text{ mA}$	h_{FE}	50 min; 140 typ	
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 12\text{ V}, I_C = 10\text{ mA}, f = 1\text{ kHz}$)	h_{fe}	75 min; 200 typ	
Small-Signal Input Impedance ($V_{CE} = 12\text{ V},$ $I_C = 10\text{ mA}, f = 1\text{ kHz}$)	h_{ie}	600	Ω
Small-Signal Output Admittance ($V_{CE} = 12\text{ V},$ $I_C = 10\text{ mA}, f = 1\text{ kHz}$)	h_{oe}	75	μmhos
Small-Signal Reverse-Voltage Transfer Ratio ($V_{CE} = 12\text{ V}, I_C = 10\text{ mA}, f = 1\text{ kHz}$)	h_{re}	125×10^{-6}	

40403

Refer to Chart of Discontinued Transistors

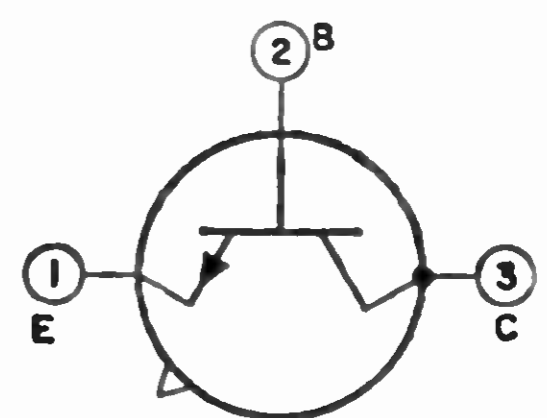
40404

Refer to Chart of Discontinued Transistors

40405

TRANSISTOR

Si n-p-n epitaxial planar type used in class C rf power amplifiers, drivers, and frequency multipliers at frequencies to 400 MHz in battery-operated communications equipment. JEDEC TO-52, Outline No.21.



MAXIMUM RATINGS

Collector-to-Emitter Voltage:

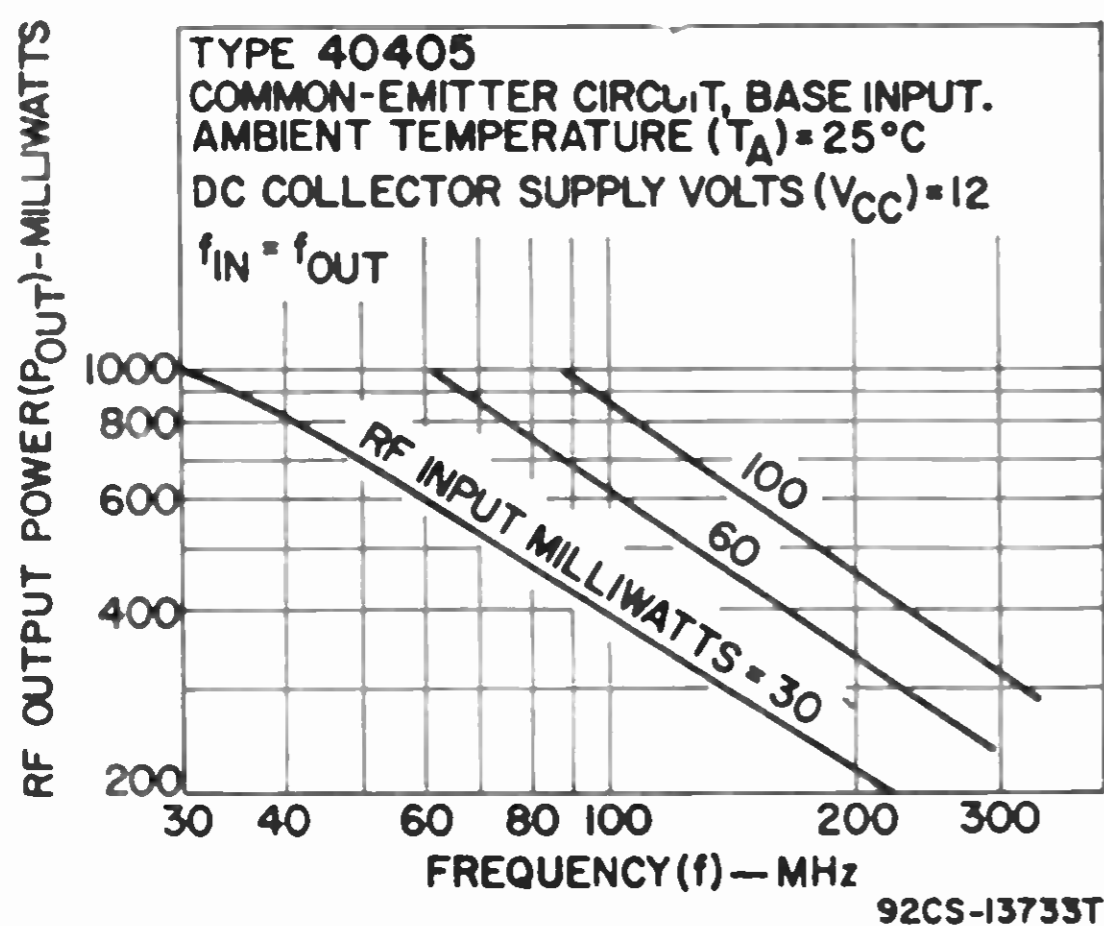
Base open	V_{CEO}	16	V
$V_{BE} = 0$	V_{CES}	40	V
Emitter-to-Base Voltage	V_{EBO}	6	V
Collector Current	I_C	0.5	A
Transistor Dissipation:			
T_A up to 25°C	P_T	0.3	W
T_c up to 25°C	P_T	1	W
T_A and T_c above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (T_A - T_c)	T_{STG}	-65 to 175	°C
Storage	T_L	-65 to 200	°C
Lead-Soldering Temperature (10 s max)		300	°C

CHARACTERISTICS

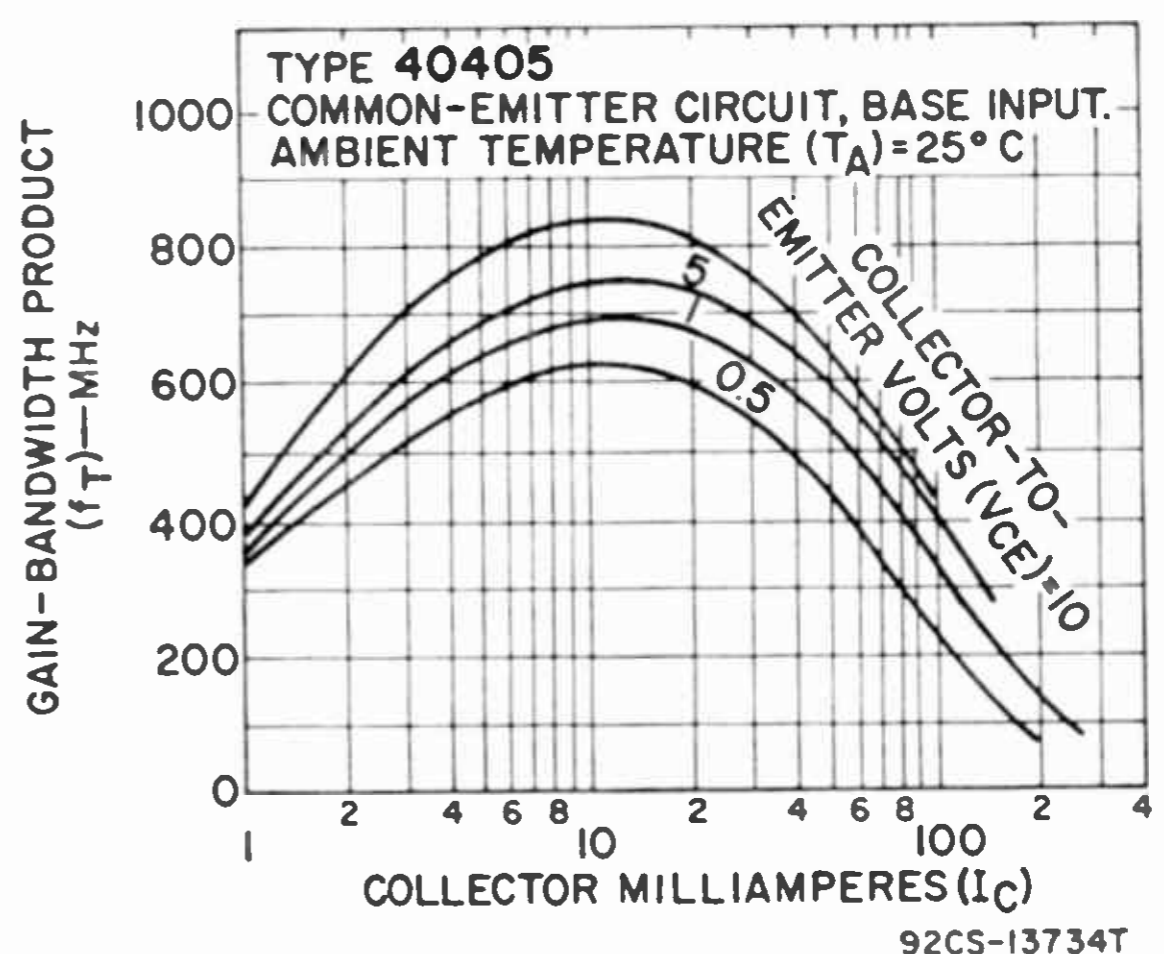
Collector-to-Emitter Breakdown Voltage:

$I_C = 10\text{ mA}, I_B = 0, t_p = 100\ \mu\text{s}, df = 2\%$	$V_{(BR)CEO}$	16 min	V
$I_C = 5\text{ mA}, R_{BE} = 0$	$V_{(BR)CES}$	40 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.01\text{ mA}, I_C = 0$)	$V_{(BR)EBO}$	6 min	V
Collector-Cutoff Current ($V_{CE} = 15\text{ V}, R_{BE} = 0$) ...	I_{CES}	0.4 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 1\text{ V}, I_C = 100\text{ mA}$)	h_{FE}	20 min	
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 1\text{ V}, I_C = 100\text{ mA}, f = 100\text{ MHz}$)	h_{fe}	3 min	

TYPICAL OPERATION CHARACTERISTICS



TYPICAL OPERATION CHARACTERISTICS



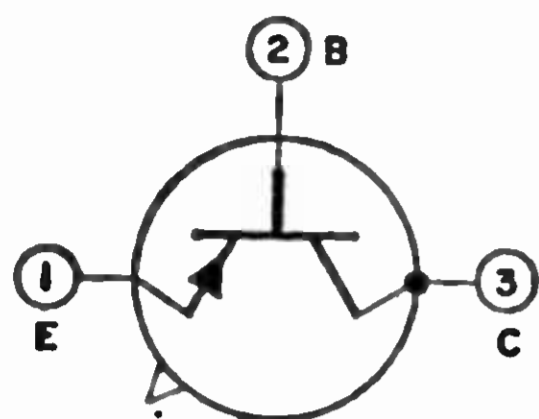
CHARACTERISTICS (cont'd)

Gain Bandwidth Product ($I_C = 100 \text{ mA}$, $V_{CE} = 1 \text{ V}$)	f_T	300 min	MHz
Output Capacitance ($V_{CB} = 5 \text{ V}$, $I_E = 0$, $f = 0.1$ to 1 MHz)	C_{obo}	3.5 max	pF
RF Power Output, Frequency-Doubler ($V_{CC} = 15 \text{ V}$, $P_{ie} \approx 30 \text{ mW}$, $f(in) = 86 \text{ MHz}$, $f(out) = 172 \text{ MHz}$)	P_{oe}	200* min	mW

* For conditions given, minimum efficiency = 35 per cent.

TRANSISTOR

40406



Si p-n-p type used in the input stages in af-amplifier applications in industrial and commercial equipment. JEDEC TO-5, Outline No.5. For collector-characteristics and input-characteristics curves, refer to type 40319.

MAXIMUM RATINGS

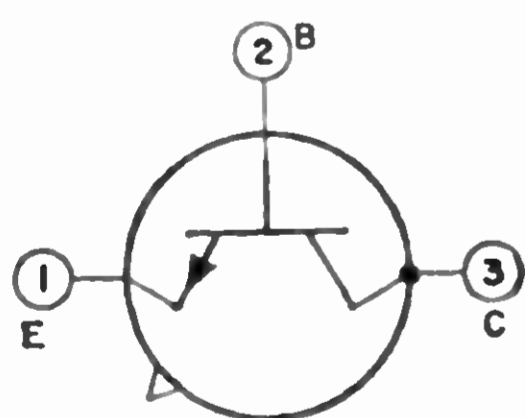
Collector-to-Emitter Sustaining Voltage	$V_{CEO(sus)}$	-50	V
Emitter-to-Base Voltage	V_{EBO}	-4	V
Collector Current	I_C	-0.7	A
Base Current	I_B	-0.2	A
Transistor Dissipation:	P_T	1	W
T_A up to 25°C	P_T	See curve page 300	
T_A above 25°C			
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 200	$^\circ\text{C}$

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_C = -100 \text{ mA}$, $I_B = 0$)	$V_{CEO(sus)}$	-50 min	V
Base-to-Emitter Voltage ($I_C = -0.1 \text{ mA}$)	V_{BE}	-0.8 max	V
Collector-Cutoff Current:			
$V_{CE} = -40 \text{ V}$, $I_B = 0$, $T_C = 25^\circ\text{C}$	I_{CEO}	-1 max	μA
$V_{CE} = -40 \text{ V}$, $I_B = 0$, $T_C = 150^\circ\text{C}$	I_{CEO}	-10 max	μA
Emitter-Cutoff Current ($V_{EB} = -4 \text{ V}$, $I_C = 0$)	I_{EBO}	-1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = -10 \text{ V}$, $I_C = -0.1 \text{ mA}$)	h_{FE}	30 to 200	
Gain-Bandwidth Product ($V_{CE} = -4 \text{ V}$, $I_C = -50 \text{ mA}$)	f_T	100	MHz
Thermal Resistance, Junction-to-Case	θ_{J-C}	35 max	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	175 max	$^\circ\text{C/W}$

TRANSISTOR

40407



Si n-p-n type used in predriver stages in af-amplifier applications in industrial and commercial equipment. This type is recommended for use in a Darlington circuit with a type such as the 40408. JEDEC TO-5, Outline No.5. For collector-characteristics and transfer-characteristics curves, refer to type 40309. This type

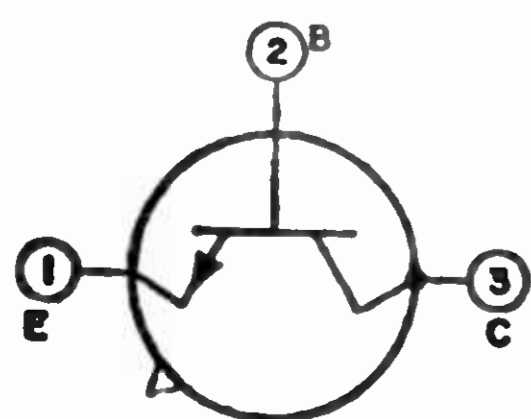
is identical with type 40406 except for reversal of all polarity signs and the following items:

CHARACTERISTICS (At case temperature = 25°C)

Base-to-Emitter Voltage ($V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ mA}$)	V_{BE}	0.8 max	V
Static Forward-Current Transfer Ratio ($V_{CE} = 10 \text{ V}$, $I_C = 1 \text{ mA}$)	h_{FE}	40 to 200	

TRANSISTOR

40408



Si n-p-n type used in predriver stages in af-amplifier applications in industrial and commercial equipment. This type is recommended for use in a Darlington circuit with a type such as the 40407. JEDEC TO-5, Outline No.5. For collector-characteristics and transfer-characteristics curves, refer to type 40309.

MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage	$V_{CEO(SUS)}$	90	V
Emitter-to-Base Voltage	V_{EBO}	4	V
Collector Current	I_C	0.7	A
Base Current	I_B	0.2	A
Transistor Dissipation:			
T_A up to 25°C	P_T	1	W
T_A above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 200	°C

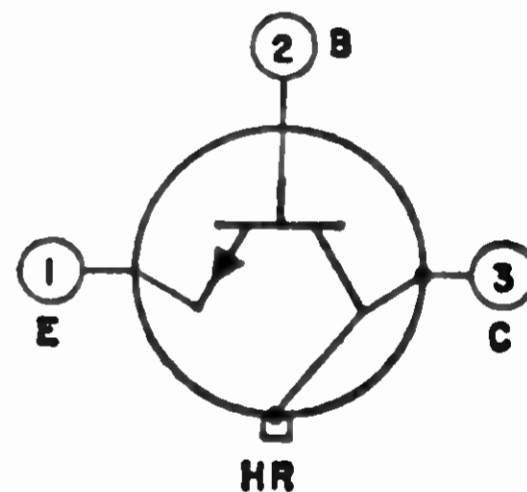
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CEO(SUS)}$	90 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 150\text{ mA}$, $I_B = 15\text{ mA}$)	$V_{CE(sat)}$	1.4 max	V
Base-to-Emitter Voltage ($V_{CE} = 4\text{ V}$, $I_C = 10\text{ mA}$) ...	V_{BE}	1 max	V
Collector-Cutoff Current:			
$V_{CE} = 80\text{ V}$, $I_B = 0$, $T_C = 25^\circ\text{C}$	I_{CEO}	1 max	μA
$V_{CE} = 80\text{ V}$, $I_B = 0$, $T_C = 150^\circ\text{C}$	I_{CEO}	250 max	μA
Emitter-Cutoff Current ($V_{EB} = 4\text{ V}$, $I_C = 0$)	I_{EBO}	1 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 4\text{ V}$, $I_C = 10\text{ mA}$)	h_{FE}	40 to 200	
Gain-Bandwidth Product ($V_{CE} = 4\text{ V}$, $I_C = 50\text{ mA}$) ...	f_T	100	MHz
Thermal Resistance, Junction-to-Case	θ_{J-C}	35 max	°C/W
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	175 max	°C/W

40409

POWER TRANSISTOR

Si n-p-n type used in driver stages in af-amplifier applications in industrial and commercial equipment. This type and type 40410 together form a complementary pair of drivers. In a typical class AB circuit a complementary pair can drive two series-connected 40411 transistors to provide an audio output of 70 watts with a total harmonic distortion of less than 0.25 per cent at 1000 Hz. JEDEC TO-5 (with heat radiator), Outline No.8. For collector-characteristics and transfer-characteristics curves, refer to type 40309.



MAXIMUM RATINGS

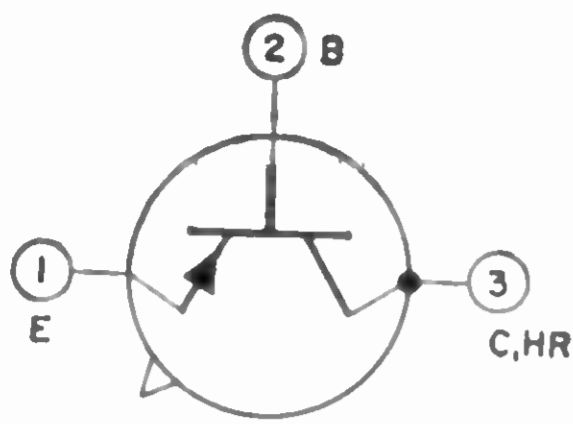
Collector-to-Emitter Sustaining Voltage ($R_{BE} \leq 10\ \Omega$)	$V_{CER(SUS)}$	90	V
Emitter-to-Base Voltage	V_{EBO}	4	V
Collector Current	I_C	0.7	A
Base Current	I_B	0.2	A
Transistor Dissipation:			
T_A up to 50°C	P_T	3	W
T_A above 50°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 200	°C

CHARACTERISTICS

Collector-to-Emitter Sustaining Voltage ($R_{BE} = 100\ \Omega$, $I_C = 100\text{ mA}$)	$V_{CER(SUS)}$	90 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 150\text{ mA}$, $I_B = 15\text{ mA}$)	$V_{CE(sat)}$	1.4 max	V
Base-to-Emitter Voltage ($V_{CE} = 4\text{ V}$, $I_C = 150\text{ mA}$) ..	V_{BE}	1 max	V
Collector-Cutoff Current:			
$V_{CE} = 80\text{ V}$, $R_{BE} = 100\ \Omega$, $T_C = 25^\circ\text{C}$	I_{CER}	1 max	μA
$V_{CE} = 80\text{ V}$, $R_{BE} = 100\ \Omega$, $T_C = 150^\circ\text{C}$	I_{CER}	100 max	μA
Emitter-Cutoff Current ($V_{EB} = 4\text{ V}$, $I_C = 0$)	I_{EBO}	1 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 4\text{ V}$, $I_C = 150\text{ mA}$)	h_{FE}	50 to 250	
Gain-Bandwidth Product ($V_{CE} = 4\text{ V}$, $I_C = 50\text{ mA}$) ...	f_T	100	MHz
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	50 max	°C/W

POWER TRANSISTOR

40410

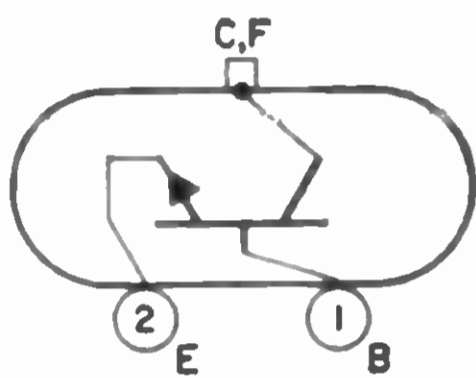


Si p-n-p type used in driver stages in af-amplifier applications in industrial and commercial equipment. This type and type 40409 form a complementary pair of drivers. In a typical class AB circuit a complementary pair can drive two series-connected 40411 transistors to provide an audio output of 70 watts with a total harmonic distortion of less than 0.25 per cent at 1000 Hz. JEDEC TO-5 (with heat radiator), Outline No.8. This type is electrically identical with type 40409 except for the reversal of all polarity signs. For collector-characteristics and input-characteristics curves, refer to type 40319.

harmonic distortion of less than 0.25 per cent at 1000 Hz. JEDEC TO-5 (with heat radiator), Outline No.8. This type is electrically identical with type 40409 except for the reversal of all polarity signs. For collector-characteristics and input-characteristics curves, refer to type 40319.

POWER TRANSISTOR

40411



Si n-p-n type features a base comprised of a homogeneous-resistivity silicon material. This type is used in output stages in af-amplifier applications in industrial and commercial equipment. In a typical class AB circuit, two series-connected 40411 transistors driven by a complementary pair of transistors (40409 and 40410) can provide an audio output of 70 watts with a total harmonic distortion of less than 0.25 per cent at 1000 Hz. JEDEC TO-3, Outline No.2. See Mounting Hardware for desired mounting arrangement.

40410) can provide an audio output of 70 watts with a total harmonic distortion of less than 0.25 per cent at 1000 Hz. JEDEC TO-3, Outline No.2. See Mounting Hardware for desired mounting arrangement.

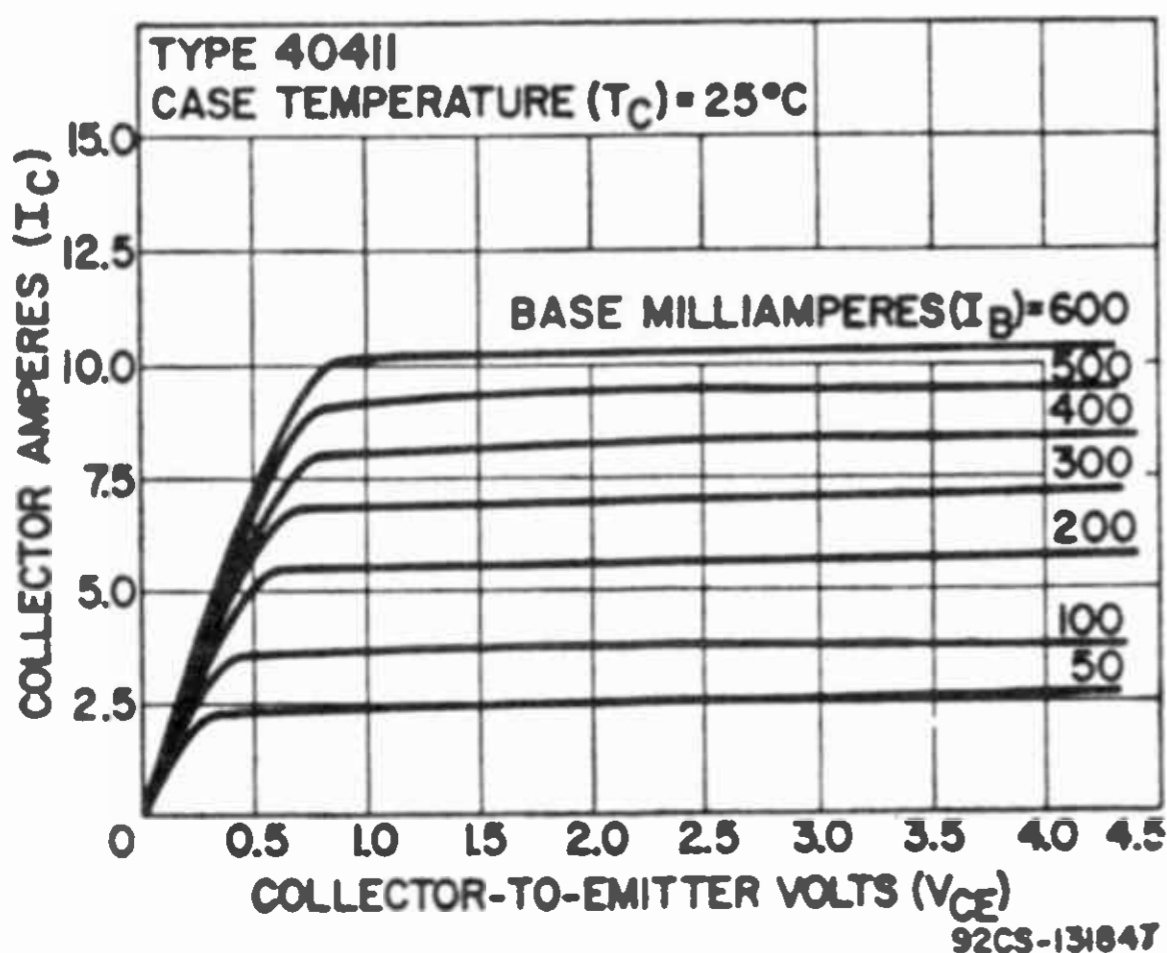
MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage ($R_{BE} \leq 100 \Omega$)	$V_{CER} (SUS)$	90	V
Emitter-to-Base Voltage	V_{EBO}	4	V
Collector Current	I_C	30	A
Base Current	I_B	15	A
Transistor Dissipation:			
T_C up to 25°C	P_T	150	W
T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J (opr)$	-65 to 200	°C

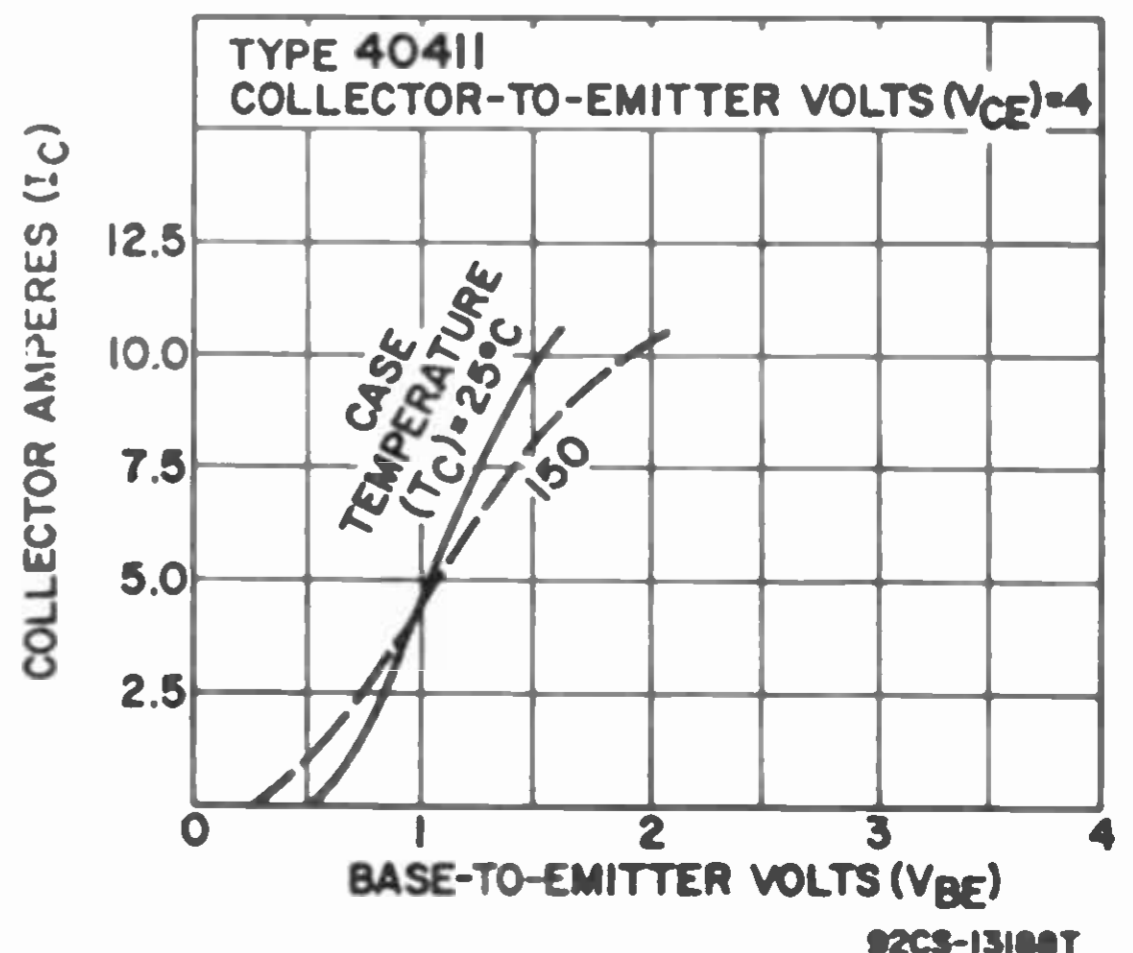
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($R_{BE} = 100 \Omega, I_C = 200 \text{ mA}$)	$V_{CER} (SUS)$	90 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 4 \text{ A}, I_B = 400 \text{ mA}$)	$V_{CE} (sat)$	0.8 max	V
Base-to-Emitter Voltage ($V_{CE} = 4 \text{ V}, I_C = 4 \text{ A}$)	V_{BE}	1.2 max	V

TYPICAL COLLECTOR CHARACTERISTICS



TYPICAL TRANSFER CHARACTERISTICS



CHARACTERISTICS (cont'd)

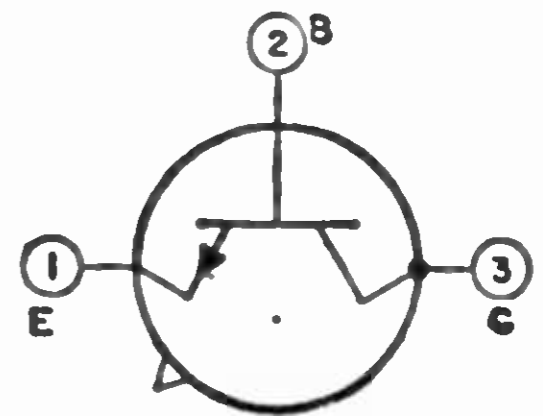
Collector-Cutoff Current:

$V_{CE} = 80\text{ V}, R_{BE} = 100\ \Omega, T_C = 25^\circ\text{C}$	I_{CER}	0.5 max	mA
$V_{CE} = 80\text{ V}, R_{BE} = 100\ \Omega, T_C = 150^\circ\text{C}$	I_{CER}	2 max	mA
Emitter-Cutoff Current ($V_{EB} = 4\text{ V}, I_C = 0$)	I_{EBO}	5 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 4\text{ V}, I_C = 4\text{ A}$)	h_{FE}	35 to 100	
Gain-Bandwidth Product ($V_{CE} = 4\text{ V}, I_C = 4\text{ A}$)	f_T	800	kHz
Power-Rating Test (40 V at 5 A for 1 s max)		200	W
Thermal Resistance, Junction-to-Case	θ_{J-C}	1.17 max	$^\circ\text{C/W}$

40412

TRANSISTOR

Si n-p-n triple-diffused type used in high-voltage switching and linear-amplifier applications in military and commercial applications. This type is particularly useful in neon-indicator driver circuits and in differential and operational amplifiers. JEDEC TO-5, Outline No.5.



MAXIMUM RATINGS

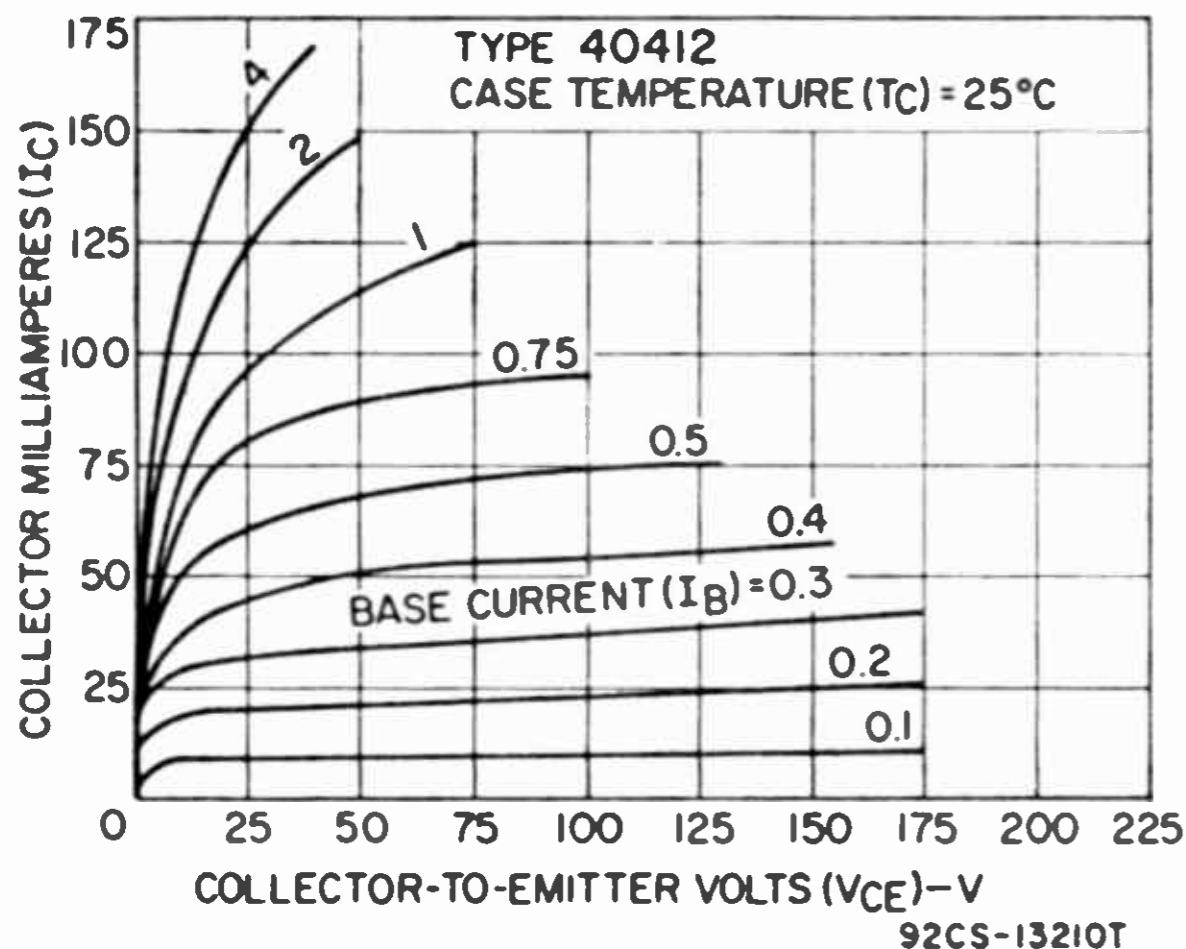
Collector-to-Emitter Sustaining Voltage ($R_{BE} = 10000\ \Omega$)	$V_{CER(SUS)}$	250	V
Collector Current	I_C	1	A
Base Current	I_B	0.5	A
Transistor Dissipation:			
T_C up to 25°C	P_T	10*	W
T_A up to 50°C	P_T	1*	W
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 200	$^\circ\text{C}$

CHARACTERISTICS (At case temperature = 25°C)

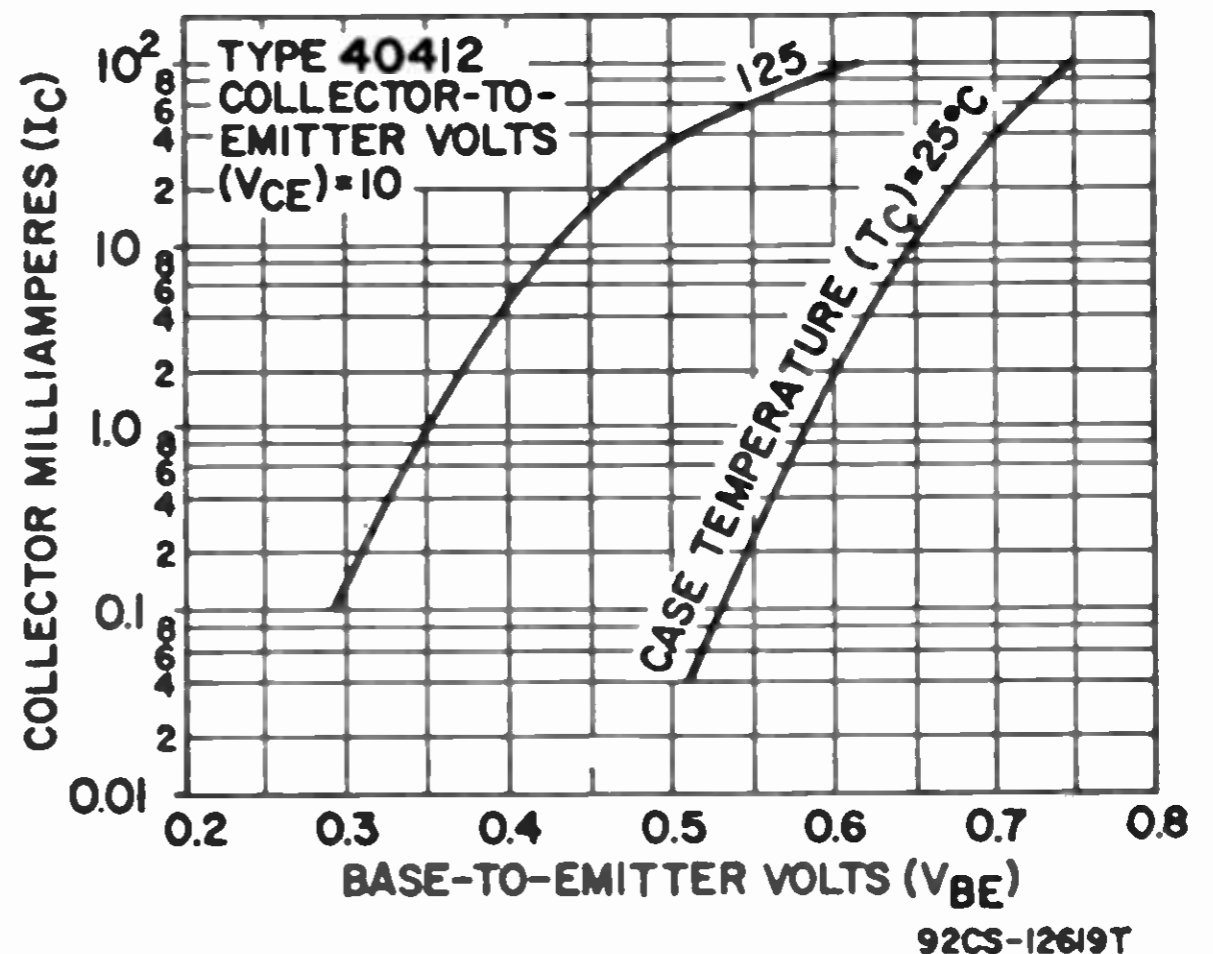
Collector-to-Emitter Sustaining Voltage ($R_{BE} = 10000\ \Omega, I_C = 50\text{ mA}$)	$V_{CER(SUS)}$	250 min	V
Collector-Cutoff Current:			
$R_{BE} = 10000\ \Omega, V_{CE} = 100\text{ V}$	I_{CER}	1 max	mA
$V_{CE} = 150\text{ V}, V_{EB} = 1.5\text{ V}, T_C = 150^\circ\text{C}$	I_{CEV}	2 max	mA
Emitter-Cutoff Current ($V_{EB} = 3\text{ V}, I_C = 0$)	I_{EBO}	100 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 20\text{ V}, I_C = 30\text{ mA}$)	h_{FE}	40 min	
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 10\text{ V}, I_C = 10\text{ mA}, f = 5\text{ MHz}$)	h_{fe}	2 min	
Output Capacitance ($V_{CB} = 10\text{ V}, I_E = 0, f = 1\text{ MHz}$)	C_{obo}	10 max	pF
Second-Breakdown Collector Current ($V_{CE} = 200\text{ V}$)	$I_{s/b}$	50 min	mA
Thermal Resistance, Junction-to-Case	θ_{J-C}	15* max	$^\circ\text{C/W}$

- * This value does not apply to type 40412V1.
- This value applies only for type 40412.

TYPICAL COLLECTOR CHARACTERISTICS

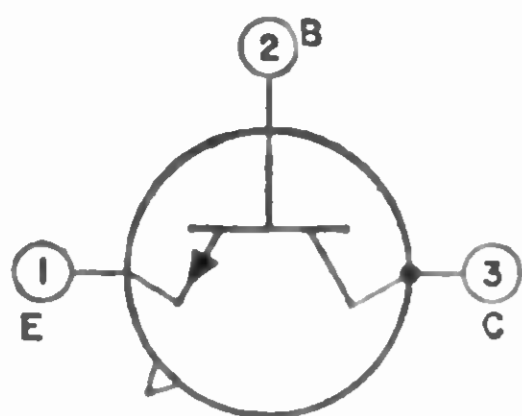


TYPICAL TRANSFER CHARACTERISTICS



TRANSISTOR

40412V1



Si n-p-n triple-diffused type used in high-voltage switching and linear-amplifier applications in military and commercial applications. This type is particularly useful in neon-indicator driver circuits and in differential and operational amplifiers. JEDEC TO-5 (with heat radiator), Outline No.8. This type is electrically identical with type 40412 except for the following items:

tical with type 40412 except for the following items:

MAXIMUM RATINGS

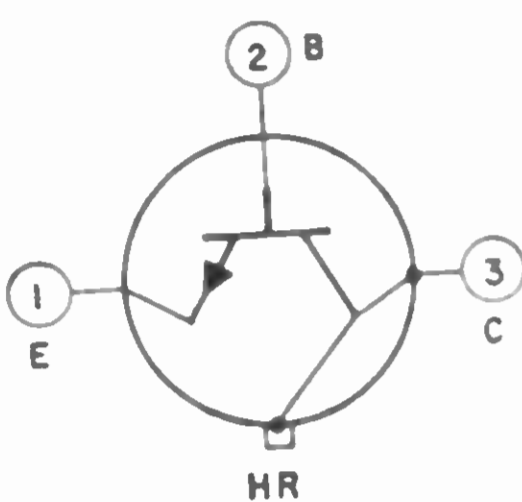
Transistor Dissipation (T_A up to 25°C) P_T 4 W

CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient θ_{J-A} 45 max °C/W

TRANSISTOR

40412V2

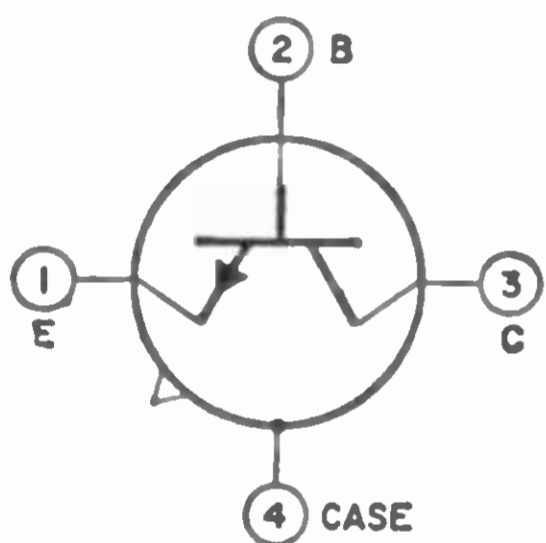


Si n-p-n triple-diffused type used in high-voltage switching and linear-amplifier applications in military and commercial applications. This type is particularly useful in neon-indicator driver circuits and in differential and operational amplifiers. JEDEC TO-5 (with flange), Outline No.6. See Mounting Hardware for desired mounting arrangement. This type is electrically identical with type 40412.

mounting arrangement. This type is electrically identical with type 40412.

TRANSISTOR

40413

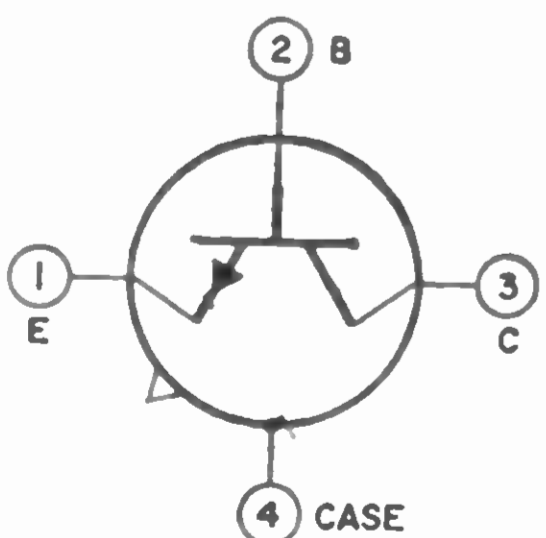


Si n-p-n double-diffused epitaxial planar type used in rf amplifier and mixer applications up to 200 MHz, and in oscillator applications up to 500 MHz. JEDEC TO-72, Outline No.28. This type is electrically and mechanically similar to type 2N2708, but each shipment of type 40413 is accompanied by a certified summary of electrical and environmental tests. For typical characteristics curves, refer to type 2N2857.

summary of electrical and environmental tests. For typical characteristics curves, refer to type 2N2857.

UHF TRANSISTOR

40414

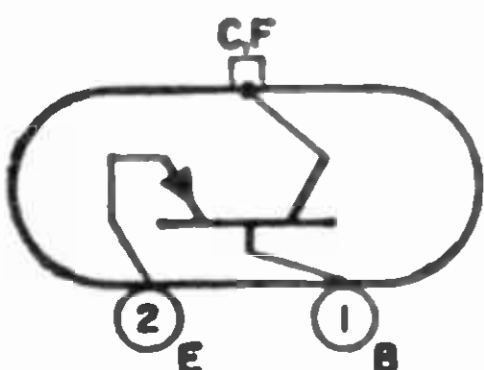


Si n-p-n double-diffused epitaxial planar type used in low-noise amplifier, oscillator, and converter applications at frequencies up to 500 MHz in a common-emitter circuit and 1200 MHz in a common-base circuit. JEDEC TO-72, Outline No.28. This type is electrically and mechanically similar to type 2N2857, but each shipment of type 40414 is accompanied by a certified summary of electrical and environmental tests. For typical characteristics curves, refer to type 2N2857.

of type 40414 is accompanied by a certified summary of electrical and environmental tests. For typical characteristics curves, refer to type 2N2857.

POWER TRANSISTOR

40421



Ge p-n-p' drift-field type used in high-fidelity af amplifier applications. JEDEC TO-3, Outline No.2.

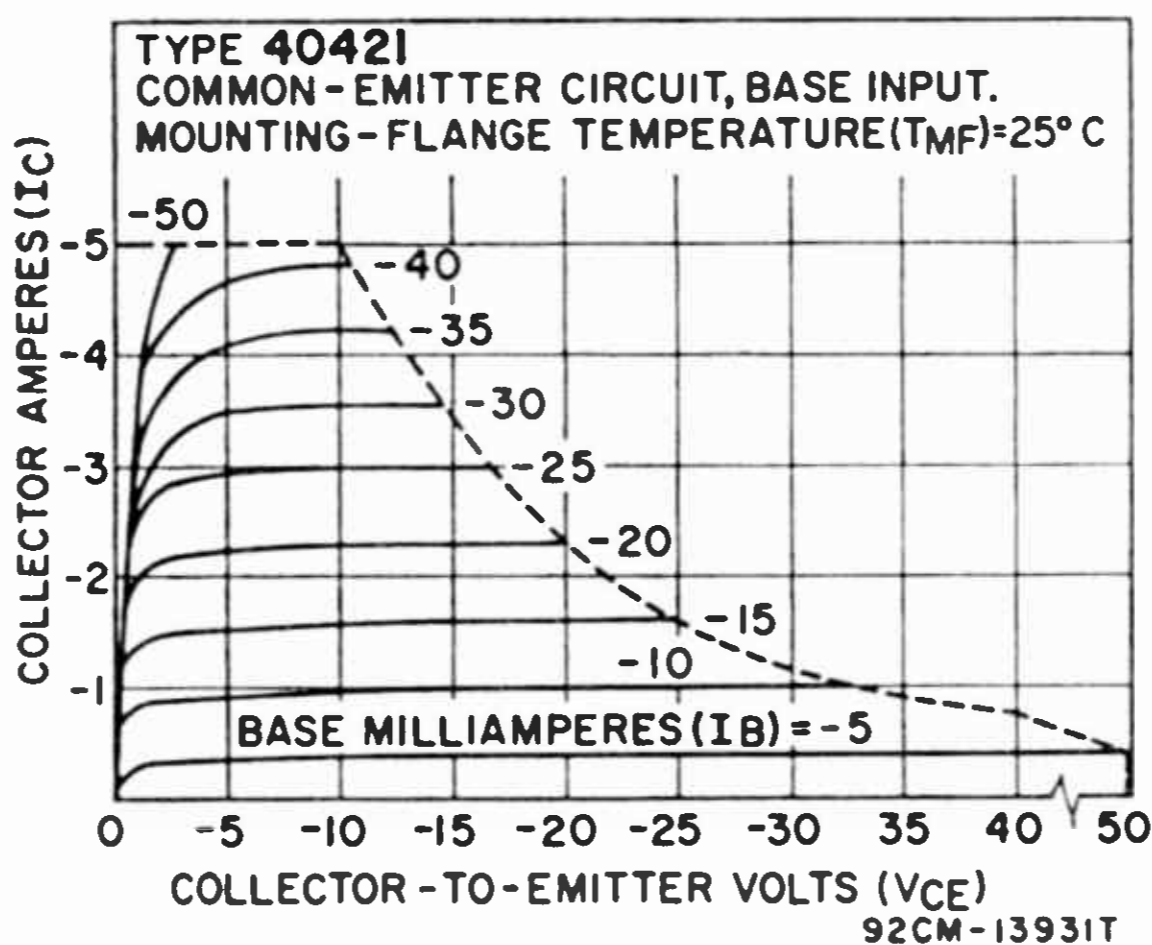
MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-75	V
Collector-to-Emitter Voltage	V_{CEO}	-50	V
Emitter-to-Base Voltage	V_{EBO}	-1.5	V
Collector Current	I_C	-5	A
Base Current	I_B	-1	A
Emitter Current	I_E	5	A
Transistor Dissipation:	P_T	12.5	W
T_{MF} up to 81°C	P_T	See curve page 300	
T_{MF} above 81°C			
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 100	°C
Storage	T_{STG}	-65 to 100	°C
Pin-Soldering Temperature (10 s max)	T_P	255	°C

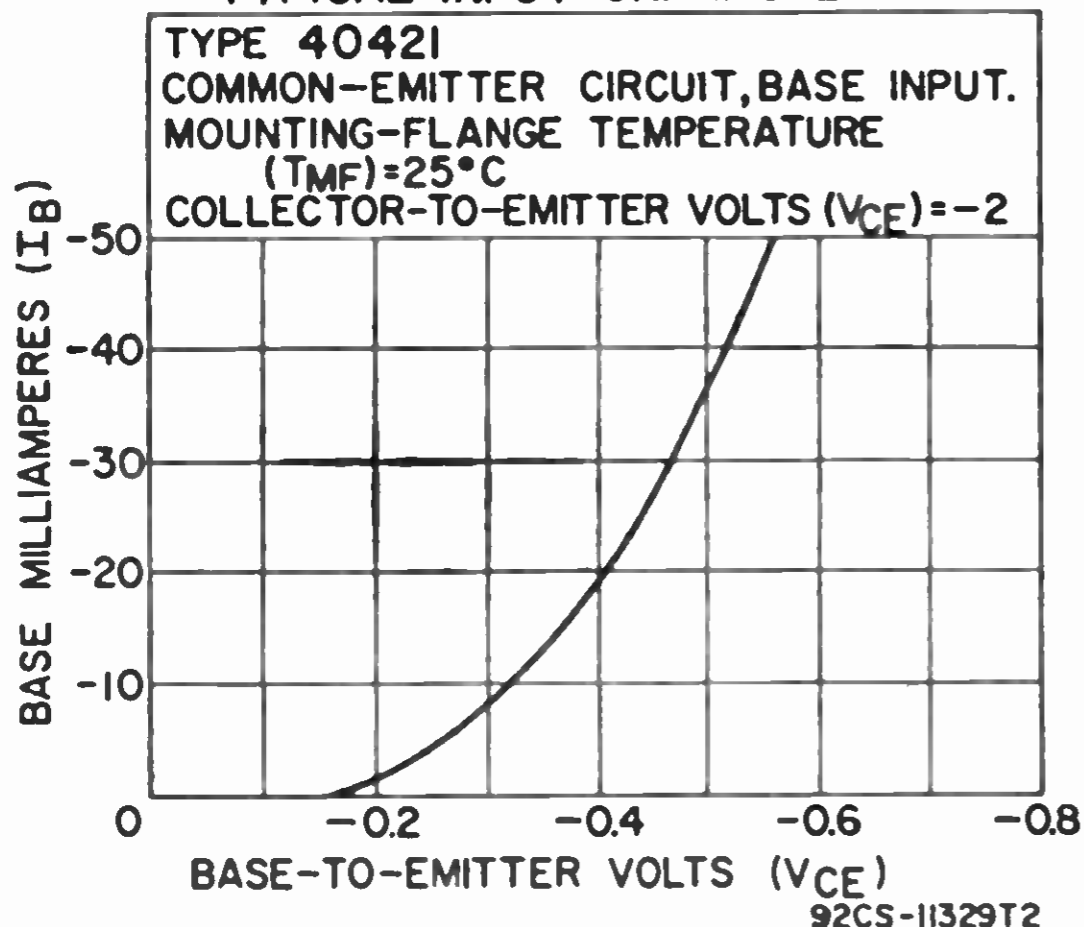
CHARACTERISTICS (At mounting-flange temperature = 25°C)

Collector-to-Base Breakdown Voltage ($I_C = -10$ mA, $I_E = 0$, $t_p \geq 300 \mu s$, $df = 0.01\%$)	$V_{(BR)CBO}$	-75	V
Collector-to-Emitter Sustaining Voltage ($I_C = -100$ mA, $I_B = 0$)	$V_{CEO(SUS)}$	-50	V
Base-to-Emitter Voltage:			
$V_{CE} = -10$ V, $I_C = -50$ mA	V_{BE}	0.21 to 0.28	V
$V_{CE} = -2$ V, $I_C = -1$ mA	V_{BE}	0.5 max	V
Collector-Cutoff Current ($V_{CB} = -40$ V, $I_E = 0$)	I_{CBO}	-1 max	mA
Collector-Cutoff Saturation Current ($V_{CB} = -0.5$ V, $I_E = 0$)	$I_{CBO(sat)}$	-70 max	μA
Emitter-Cutoff Current ($V_{BE} = 1.5$ V, $I_C = 0$)	I_{EBO}	-2.5 max	mA
Static Forward-Current Transfer Ratio:			
$V_{CE} = -2$ V, $I_C = -1000$ V	h_{FE}	62 to 175	
$V_{CE} = -2$ V, $I_C = -4000$ V	h_{FE}	40 min	
Gain-Bandwidth Product ($V_{CE} = -5$ V, $I_C = -500$ mA)	f_T	2 min; 4 typ	MHz
Thermal Resistance, Junction-to-Mounting Flange	θ_{J-MF}	1.5 max	°C/W

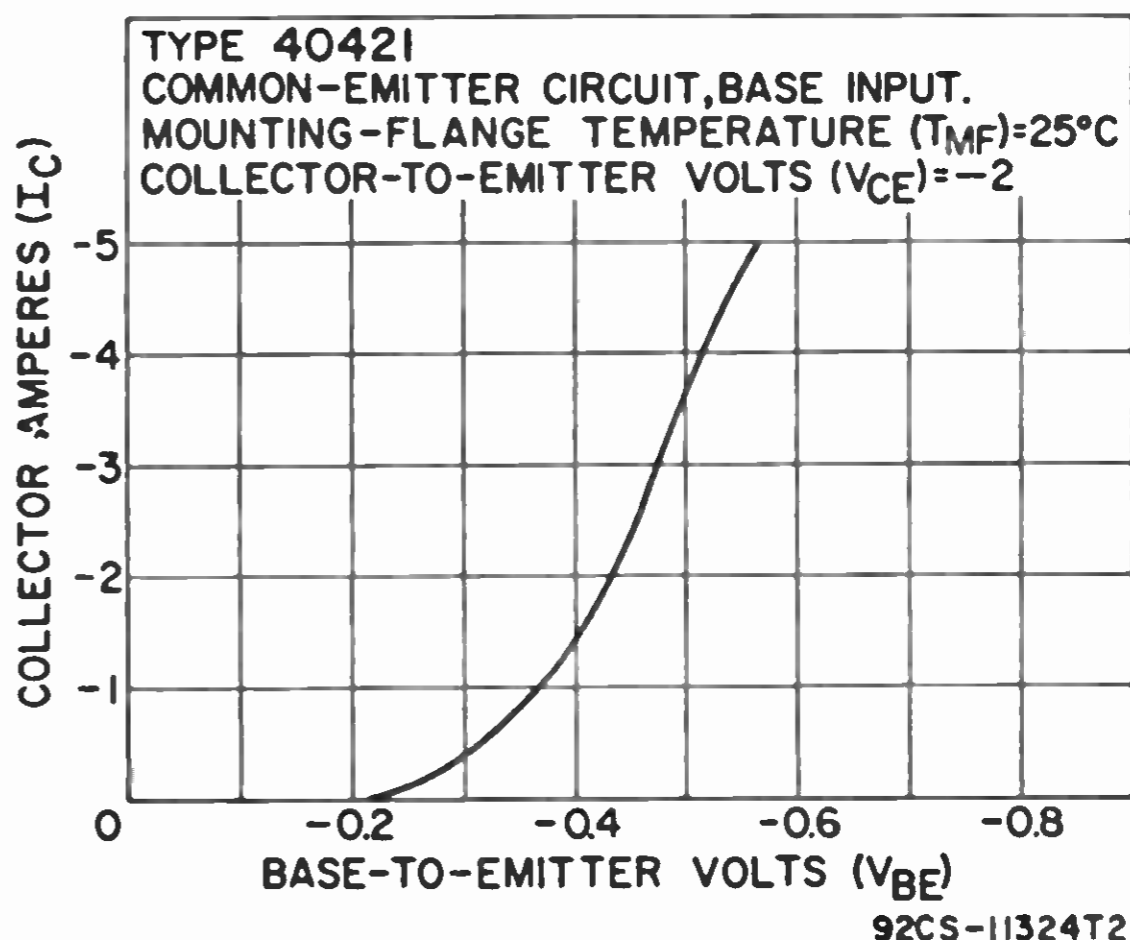
TYPICAL COLLECTOR CHARACTERISTICS



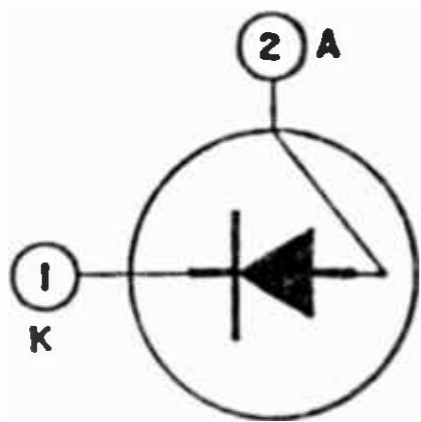
TYPICAL INPUT CHARACTERISTIC



TYPICAL TRANSFER CHARACTERISTIC



Refer to Chart of Discontinued Transistors	40422
Refer to Chart of Discontinued Transistors	40423
Refer to Chart of Discontinued Transistors	40424
Refer to Chart of Discontinued Transistors	40425
Refer to Chart of Discontinued Transistors	40426
Refer to Chart of Discontinued Transistors	40427



COMPENSATING DIODE

40428

Ge alloy-junction type used in temperature- and voltage-compensation applications. Similar to JEDEC TO-1 (2-lead), Outline No.41.

MAXIMUM RATINGS

Reverse Voltage	V_{RM}	-0.5	V
DC Forward Current	I_{FM}	100	mA
Peak Forward Current	$i_F(\max)$	200	mA
Temperature Range:			
Operating (T_A) and Storage (T_{STG})		-65 to 85	°C
Lead-Soldering Temperature (10 s max)	T_L	255	°C

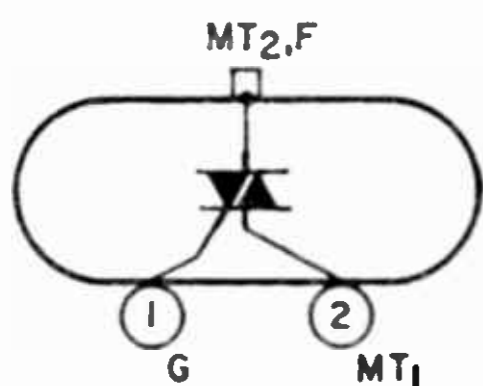
CHARACTERISTICS

DC Forward Voltage Drop:		min	typ	max	
$T_C = 25^\circ C$	V_{FAV}	235	260	285	mV
$T_A = 25^\circ C$	V_{FAV}	225	250	275	mV

TRIACS

40429

40430



Si gate-controlled full-wave types used for the control of ac loads in applications such as heating controls, motor controls, light dimmers, and power switching systems. JEDEC TO-66, Outline No.25. See Mounting Hardware for desired mounting arrangement.

MAXIMUM RATINGS (For sinusoidal ac supply voltage at $f = 50/60$ Hz with resistive or inductive load)

V_{DROM}^* ($T_J = -65^\circ C$ to $100^\circ C$)	40429	40430	
	200	400	V
$I_{T(RMS)}$ ($T_C = 75^\circ C$, conduction angle = 360°)	_____	6	A
$I_{T(RMS)}$ (T_A up to $100^\circ C$, conduction angle = 360°)	See Rating Chart (Ambient Temperature)		
I_{TSM} (1 cycle of principal voltage)	_____	100	A
I_{GTM} (1 μs max)	_____	4	A
P_{GM} (1 μs max, $I_{GTM} \leq 4$ A peak)	_____	16	W
$P_{G(AV)}$	_____	0.2	W
T_{STG}	_____	-65 to 150	°C
T_C	_____	-65 to 100	°C

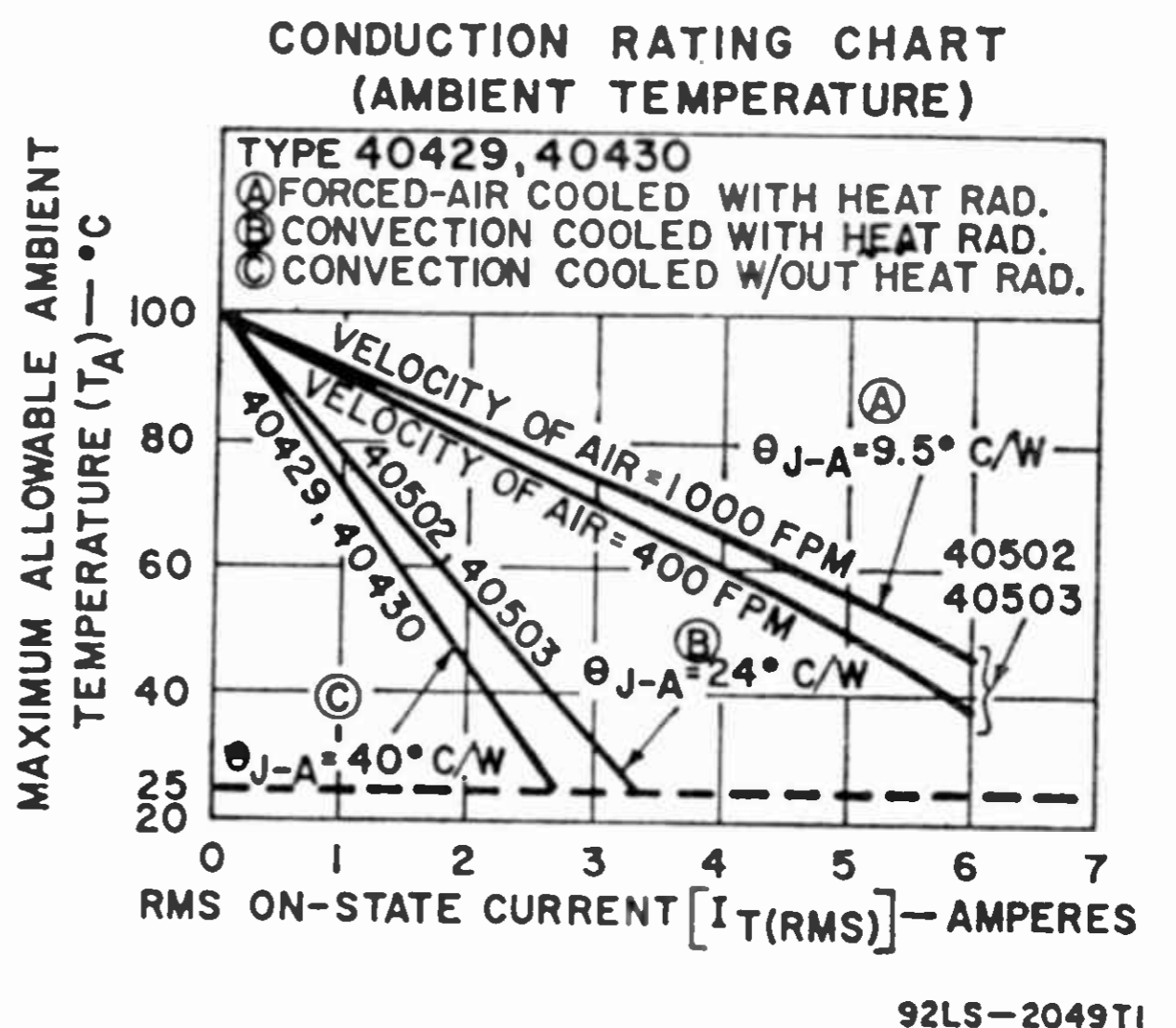
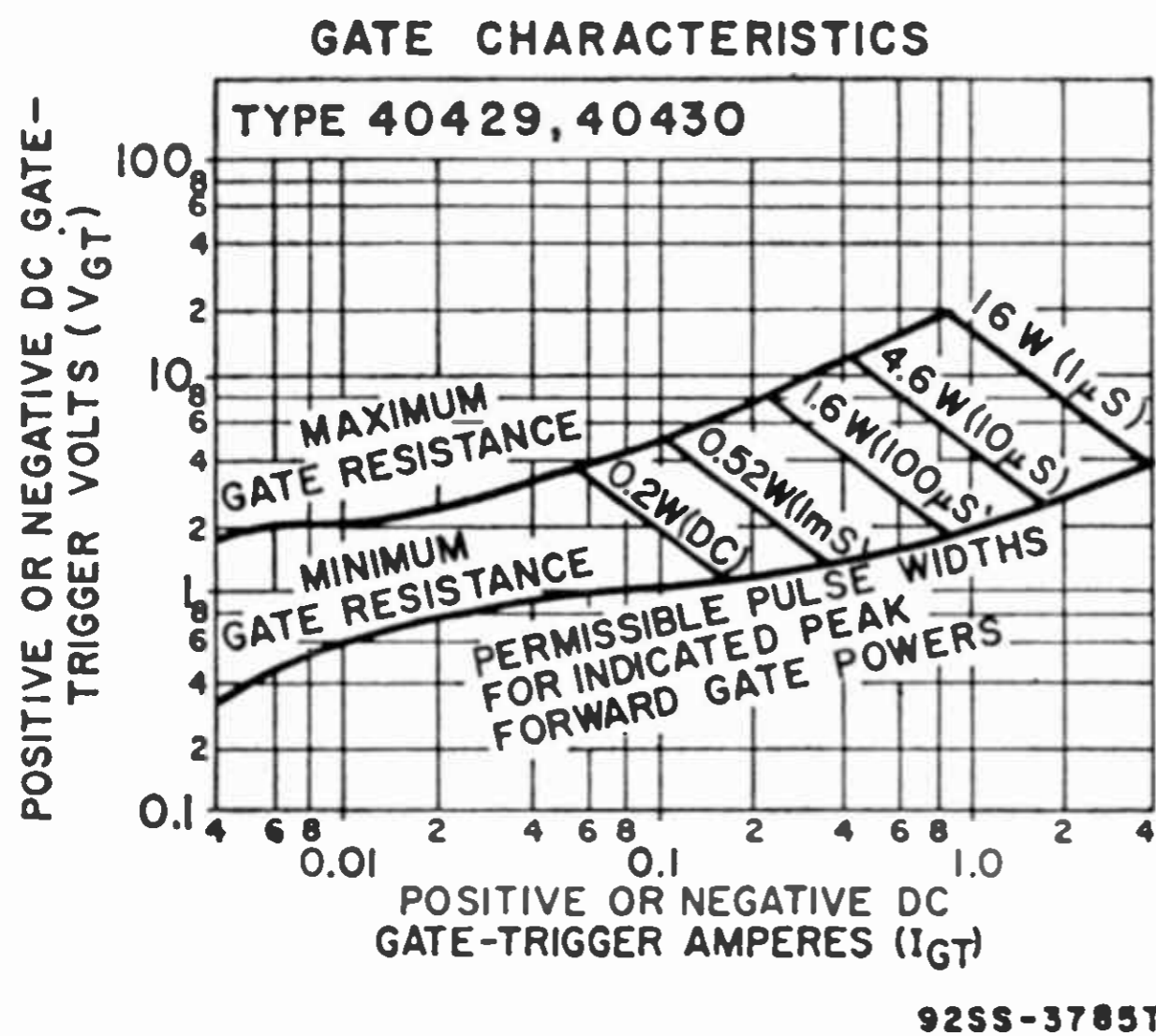
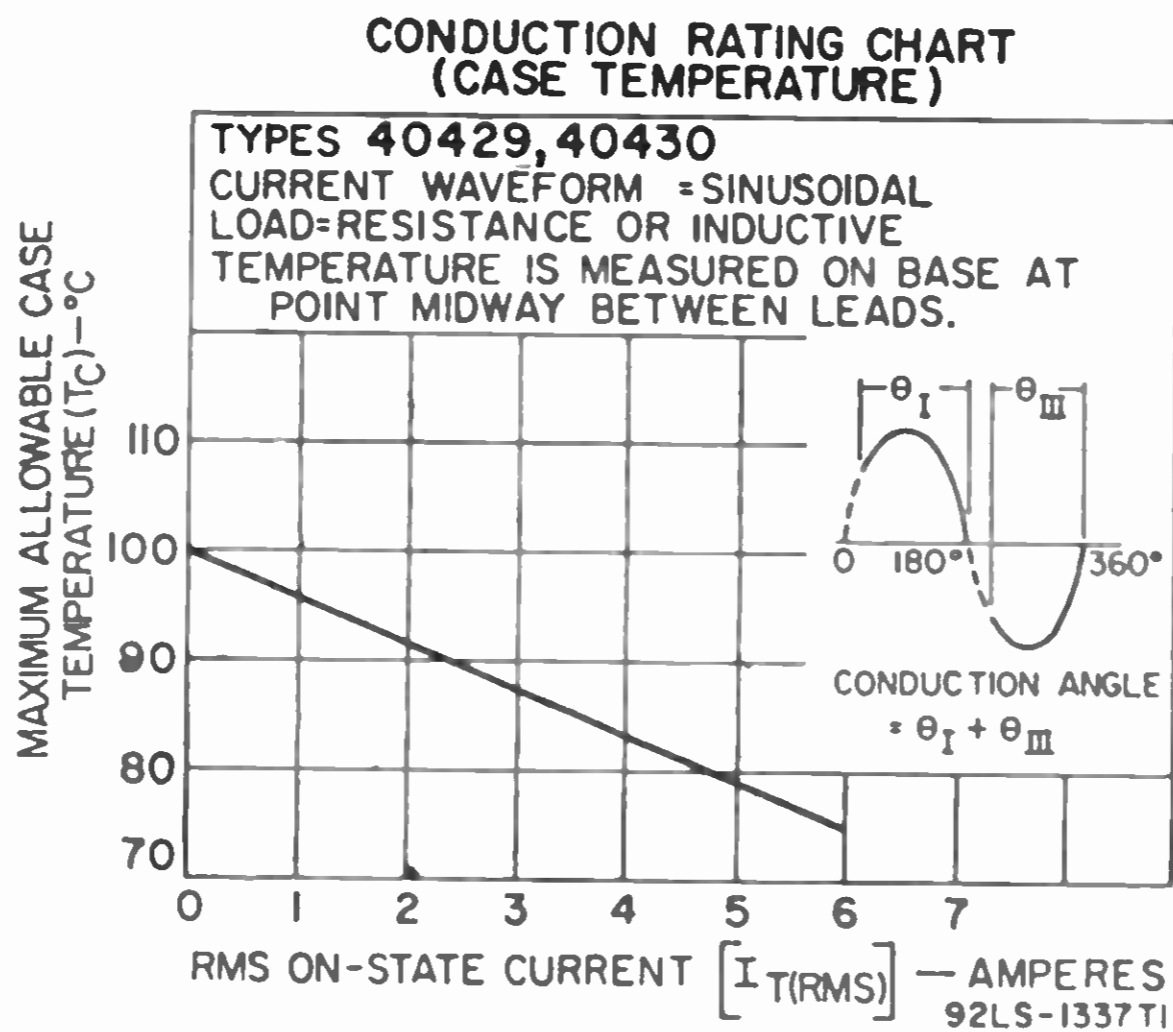
CHARACTERISTICS (At maximum electrical ratings at $T_C = 25^\circ C$)

I_{DROM}^* ($T_J = 100^\circ C$, $V_{DROM} = \max$ rated value)	0.1 typ; 4 max	0.2 typ; 4 max	mA
V_{TM}^* ($i_T = 30$ A peak)	_____	1.8 typ; 2.25	V
I_{HO}^* (initial principal = 150 mA dc)	_____	15 typ; 30 max	mA
Commutating dv/dt^* ($V_D = V_{DROM}$, $I_{T(RMS)} = 6$ A, commutating $di/dt = 3.2$ A/ms, gate unenergized at $T_C = 75^\circ C$)	_____	3 min; 10 typ	V/ μs
Critical dv/dt^* ($V_D = V_{DROM}$, exponential voltage rise, $T_C = 100^\circ C$)	30 min; 150 typ	20 min; 100 max	V/ μs

CHARACTERISTICS (cont'd)

$I_{GT}^* \ddagger$ ($V_D = 12 \text{ Vdc}$, $R_L = 12 \Omega$):			
I ⁺ mode, V_{MT2} positive, V_G positive	_____	15 typ; 25 max	_____ mA
I ⁻ mode, V_{MT2} positive, V_G negative	_____	25 typ; 40 max	_____ mA
III ⁺ mode, V_{MT2} negative, V_G positive	_____	25 typ; 40 max	_____ mA
III ⁻ mode, V_{MT2} negative, V_G negative	_____	15 typ; 40 max	_____ mA
$V_{GT}^* \ddagger$ ($V_D = 12 \text{ Vdc}$, $R_L = 12 \Omega$)	_____	1 typ; 2.2 max	_____ V
$V_{GT}^* \ddagger$ ($V_D = V_{DROM}$, $R_L = 125 \Omega$, $T_c = 100^\circ\text{C}$)	_____	0.2 min	_____ V
t_{gt} ($V_D = V_{DROM}$, $I_{GT} = 80 \text{ mA}$, $t_r = 0.1 \mu\text{s}$, $i_T = 10 \text{ A}$)	_____	2.2	_____ μs
θ_{J-C} (steady-state)	_____	4 max	_____ $^\circ\text{C/W}$
θ_{J-A}	See Rating Chart (Ambient Temperature)		

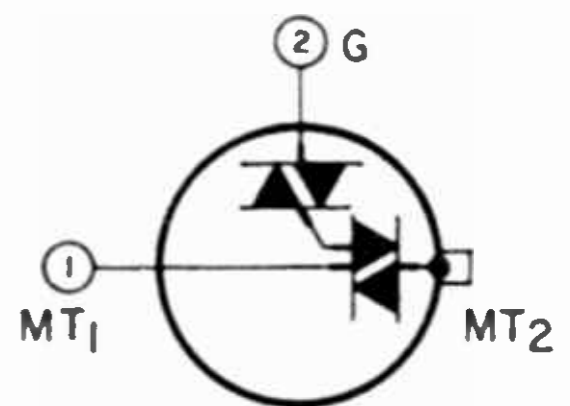
* For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
 † For either polarity of gate voltage (V_G) with reference to main terminal 1.
 • This characteristic does not apply to types 40502 and 40503.



**40431
40432**

TRIACS

Si gate-controlled full-wave types used for phase control of ac loads in applications such as light dimming, universal and induction motor control, and heater control. These devices have integral triggers. JEDEC TO-5 (modified), Outline No.7. See Mounting Hardware for desired mounting arrangement.



MAXIMUM RATINGS (For sinusoidal ac supply voltage at $f = 50$ and 60 Hz with resistive or inductive load)

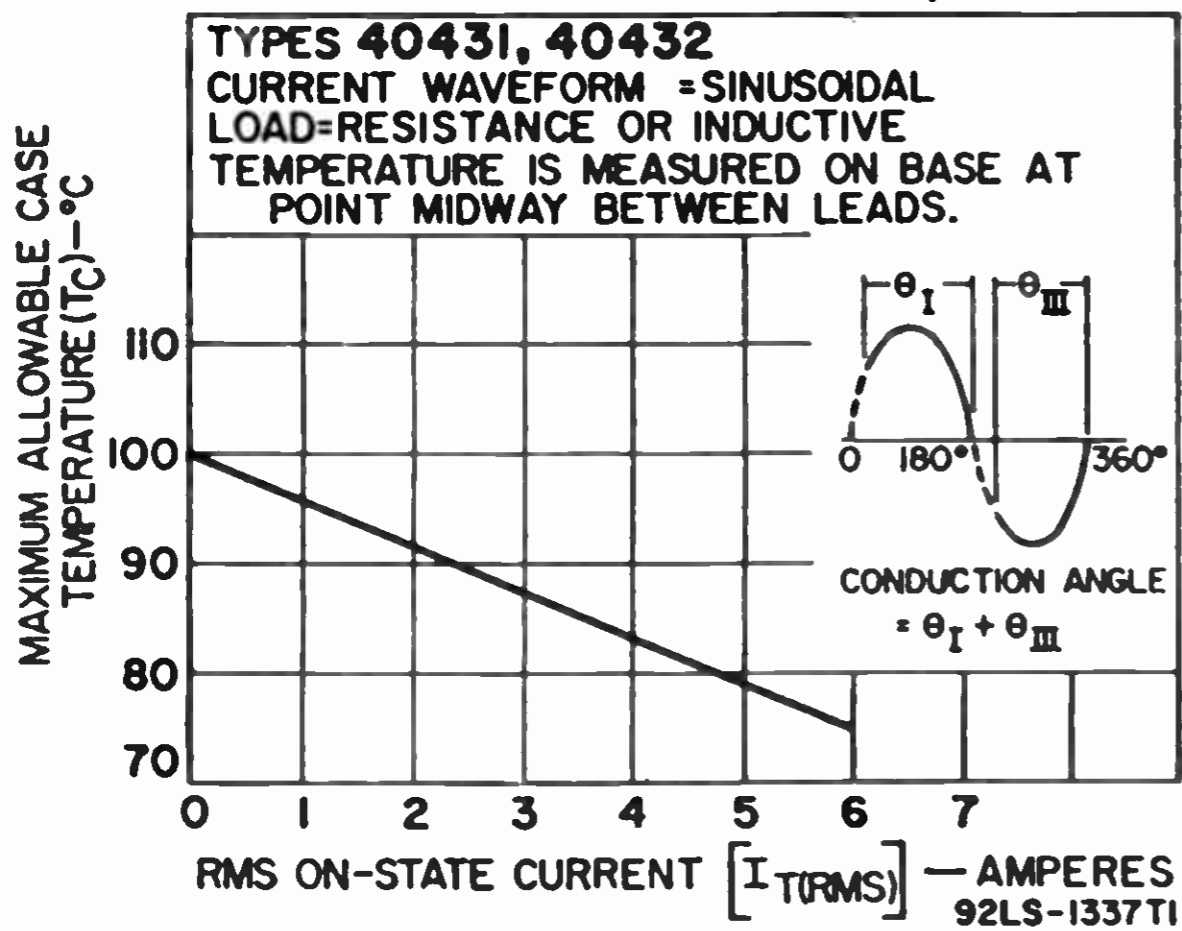
	40431	40432	
V_{DROM} (gate open, $T_J = -40^\circ\text{C}$ to 100°C)	200	400	V
$I_{T(RMS)}$ ($T_C = 75^\circ\text{C}$, conduction angle = 360°) ..	6		A
I_{TSM} (1 cycle of principal voltage)	100		A
I_{GTM} ($2 \mu\text{s}$ max)	1		A
P_{GM} ($2 \mu\text{s}$ max, $I_{GTM} \leq 1$ A peak)	20		W
$P_{G(\Delta V)}$	0.2		W
$T_{stg}^{*\Delta}$	-40 to 150		$^\circ\text{C}$
$T_C^{*\Delta}$	-40 to 100		$^\circ\text{C}$

CHARACTERISTICS (At maximum electrical rating at $T_C = 25^\circ\text{C}$)

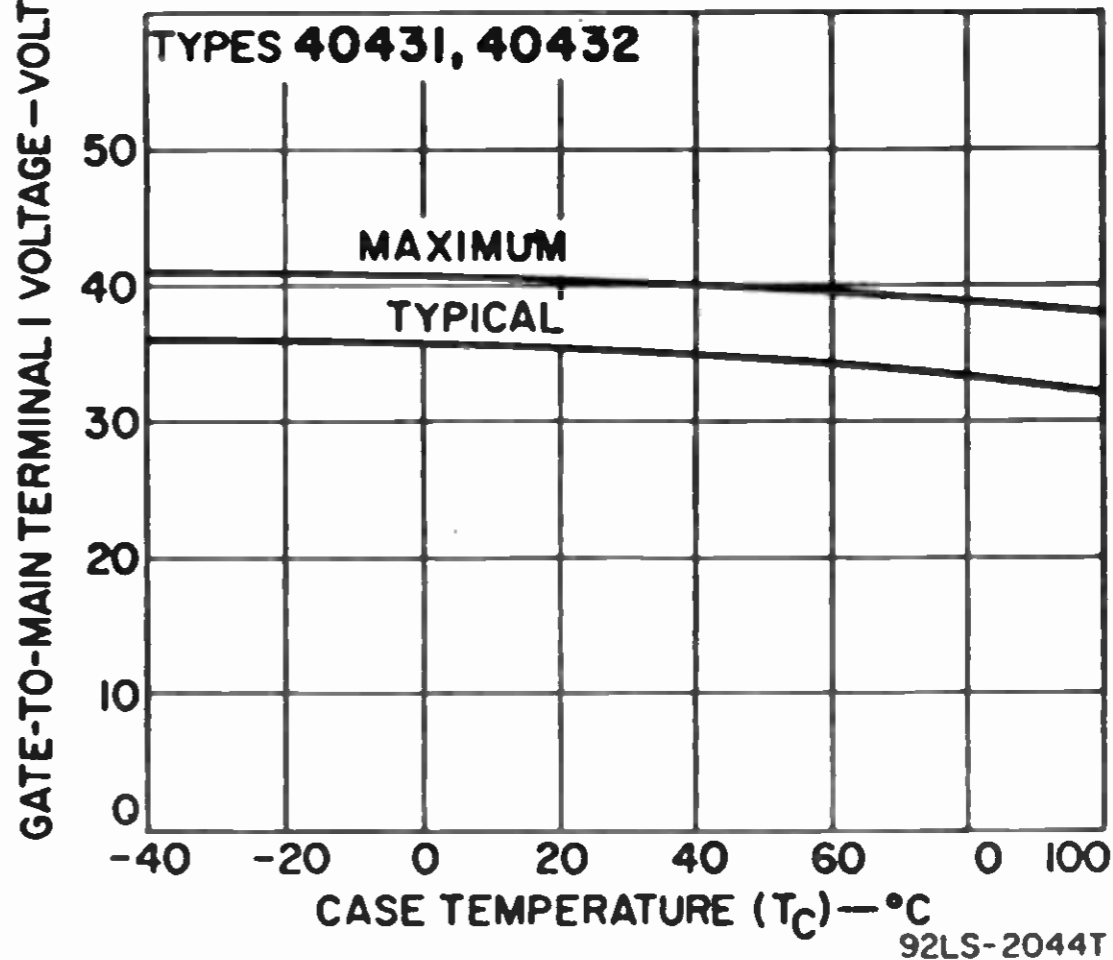
	40431	40432	
I_{DROM} (gate open, $T_J = 100^\circ\text{C}$, $V_{DROM} = \text{max rated value}$)	0.1 typ	0.2 typ	mA
V_T ($i_T = 30$ A)	2 max	4 max	mA
I_{HO} (initial principal current = 150 mA dc)	1.6 typ; 2.25 max		V (peak)
Commutating dv/dt ($V_D = V_{DROM}$, $I_{T(RMS)} = 6$ A, commutating $di/dt = 4$ A/ms, gate open):			
$T_C = 75^\circ\text{C}$	5		V/ μs
$T_C = 50^\circ\text{C}$	8		V/ μs
Critical dv/dt ($V_D = V_{DROM}$, exponential voltage rise, gate open, $T_C = 100^\circ\text{C}$)	30	20	V/ μs
V_{GTM}	20 min, 35 typ, 40 max		V
$ V_{GM}^+ - V_{GM}^- $	± 1 typ; ± 3 max		V
I_{GTM}^\ddagger	40 typ; 200 max		μA
Gate Trigger Capacitance ($V_D = 6$ V dc, $R_L = 12 \Omega$, $T_C = 100^\circ\text{C}$)	0.1 to 2		μF
t_{gt} ($V_D = V_{DROM}$, $I_{GT} = 80$ mA, $t_r = 0.1 \mu\text{s}$, $i_T = 10$ A peak)	2.2		μs

- For either polarity of main-terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
- For either polarity of gate voltage (V_G) with reference to main terminal 1.
- * For information on the reference point of temperature measurement, see section on Outlines.
- ▲ When these devices are soldered directly to the heat sink, a 60-90 solder should be used. Exposure time should be just sufficient to cause the solder to flow freely.

CONDUCTION RATING CHART (CASE TEMPERATURE)

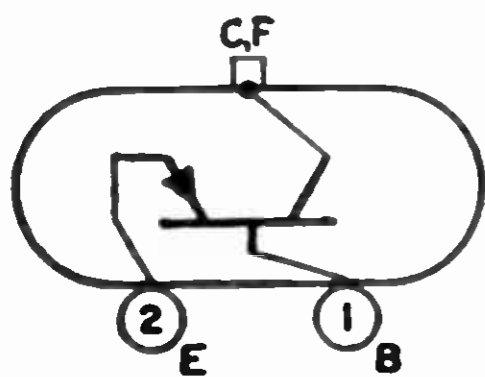


PEAK GATE FIRING VOLTAGE CHARACTERISTICS



POWER TRANSISTOR

40439



Ge p-n-p diffused-collector, graded-base type used in 114-degree 18-kV TV deflection systems as a horizontal-output amplifier. This type, together with types 2N3730 (vertical output), 2N3731 and 40440 (horizontal output), 2N3732 (horizontal driver), and 1N4785 and 40442 (damper), make up a complete transistor/damper-diode

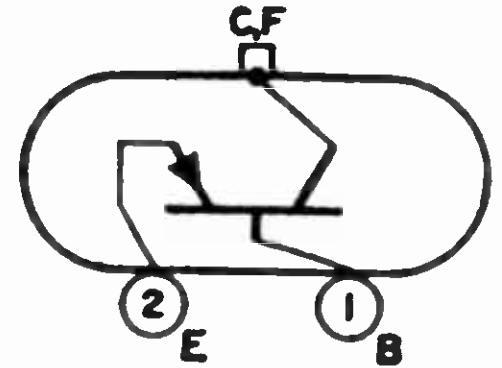
complement. JEDEC TO-3, Outline No.2. This type is identical with type 2N3731 except for the following item:

CHARACTERISTICS

Turn-Off Time	$t_o + t_r$	0.75 max	μs
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40440 POWER TRANSISTOR

Ge p-n-p diffused-collector, graded-base type used in 114-degree 18kV TV deflection systems as a horizontal-output amplifier. This type, together with types 2N3730 (vertical output), 2N3731 and 40439 (horizontal output), 2N3732 (horizontal driver), and 1N4785 and 40442 (damper), make up a complete transistor/damper-diode complement. JEDEC TO-3, Outline No.2. This type is identical with type 2N3731 except for the following items:



This type is identical with type 2N3731 except for the following items:

MAXIMUM RATINGS

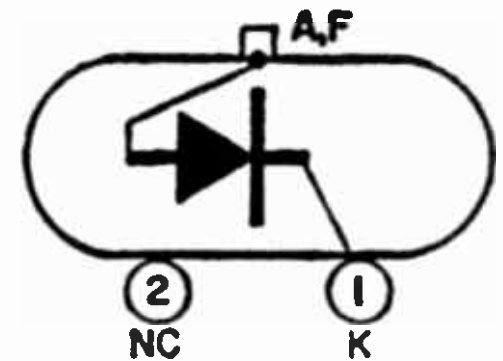
Collector-to-Base Voltage: Peak	V_{CBO}	-200	V
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CHARACTERISTICS

Collector-to-Emitter Breakdown Voltage ($I_c = -0.025 \text{ mA}$, $V_{EB} = 0$)	$V_{(BR)CES}$	-200	V
Collector-to-Emitter Saturation Voltage: $I_c = -6 \text{ A}$, $I_B = -0.4 \text{ A}$	$V_{CE(sat)}$	-0.75 max	V
$I_c = -3 \text{ A}$, $I_B = -0.2 \text{ A}$	$V_{CE(sat)}$	-0.75 max	V
Base-to-Emitter Voltage ($I_c = -6 \text{ A}$, $I_B = -0.4 \text{ A}$) ...	V_{BE}	-1	V

40442 DAMPER DIODE

Ge diffused-junction type used in transistorized 114-degree, 18-kilovolt horizontal-deflection systems in television receivers with types 2N3730, 2N3731, 2N3732, 40439, and 40440 to make up a complete transistor/damper-diode complement. JEDEC TO-3, Outline No.2. This type is identical to type 1N4785 except for the following items:



MAXIMUM RATINGS

Peak Reverse Voltage	V_{RM}	200	V
Continuous Reverse Voltage	V_{RM}	40	V

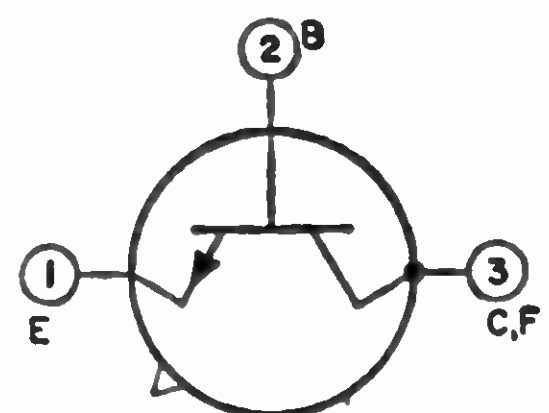
CHARACTERISTICS

Peak Reverse Voltage ($I_R = 1 \text{ mA}$)	V_{RM}	200 min	V
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40444 Refer to Chart of Discontinued Transistors

40446 TRANSISTOR

Si n-p-n triple diffused planar type used in power-amplifier applications, in conjunction with types 40080 (oscillator), 40081 (driver), and 40082 (power amplifier), in a 5-watt-input, 27 - MHz citizens-band transmitter. JEDEC TO-5 (with flange), Outline No.6. See Mounting Hardware for desired mounting arrangement. This type is identical with type 40082 except for the following items:



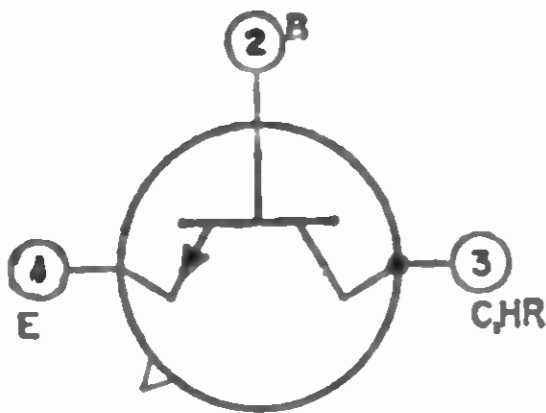
MAXIMUM RATINGS

Transistor Dissipation:

T_c up to 25°C	P_T	10	W
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CHARACTERISTICS (At case temperature = 25°C)

Thermal Resistance, Junction-to-Case	θ_{J-C}	17.5	°C/W
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TRANSISTOR

40450

Si n-p-n epitaxial planar type used in high-voltage, high-current audio and video amplifiers and switching service in commercial, industrial, and computer equipment. JEDEC TO-104, Outline No.33. This type is identical with type 2N3241A except for the following items:

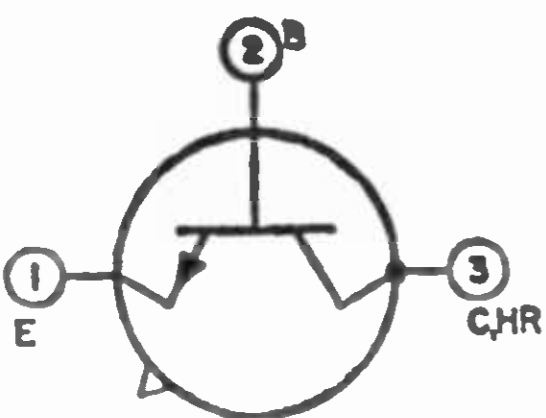
MAXIMUM RATINGS

Transistor Dissipation:

T_A up to 25°C	P_T	1	W
T_A above 25°C	P_T	See curve page 300	

CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient	θ_{J-A}	150 max	°C/W
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TRANSISTOR

40451

Si n-p-n epitaxial planar type used in high-voltage, high-current audio and video amplifier and switching service in commercial, industrial, and computer equipment. JEDEC TO-104 (with heat radiator), Outline No.33. This type is identical with type 2N3242A except for the following items:

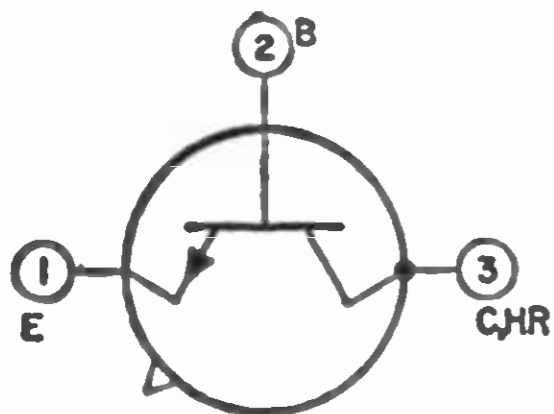
MAXIMUM RATINGS

Transistor Dissipation:

T_A up to 25°C	P_T	1	W
T_A above 25°C	P_T	See curve page 300	

CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient	θ_{J-A}	150 max	°C/W
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TRANSISTOR

40452

Si n-p-n epitaxial planar type used in high-voltage, high-current audio and video amplifier service in commercial and industrial equipment. JEDEC TO-104 (with heat radiator), Outline No.33. This type is identical with type 2N4074 except for the following items:

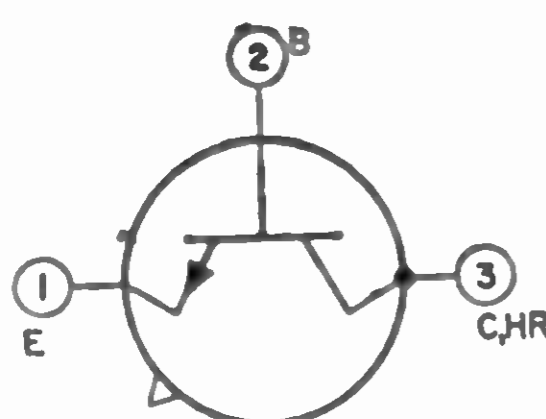
MAXIMUM RATINGS

Transistor Dissipation:

T_A up to 25°C	P_T	1	W
T_A above 25°C	P_T	See curve page 300	

CHARACTERISTICS (At case temperature = 25°C)

Thermal Resistance, Junction-to-Ambient	θ_{J-A}	150 max	°C/W
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TRANSISTOR

40453

Si n-p-n epitaxial planar type used in high-voltage, high-current audio and video amplifier service in commercial and industrial equipment. JEDEC TO-104 (with heat radiator), Outline No.33. This type is identical with type 40397 except for the following items:

MAXIMUM RATINGS

Transistor Dissipation:

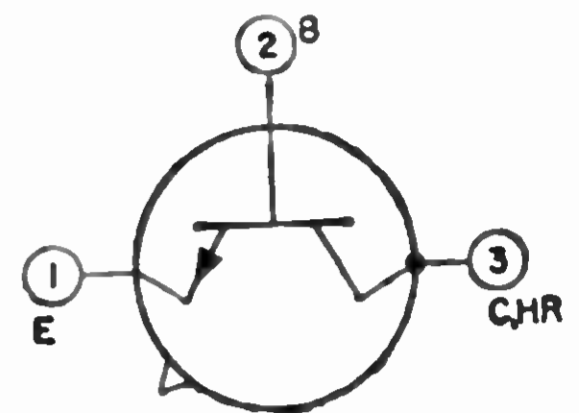
T_A up to 25°C.....	P_T	1	W
T_A above 25°C	P_T	See curve	page 300

CHARACTERISTICS (At case temperature = 25°C)

Thermal Resistance, Junction-to-Ambient	θ_{J-A}	150 max	°C/W
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40454 TRANSISTOR

Si n-p-n epitaxial planar type used in high-voltage, high-current audio and video amplifier service in commercial and industrial equipment. JEDEC TO-104 (with heat radiator), Outline No.33. This type is identical with type 40398 except for the following items:



MAXIMUM RATINGS

Transistor Dissipation:

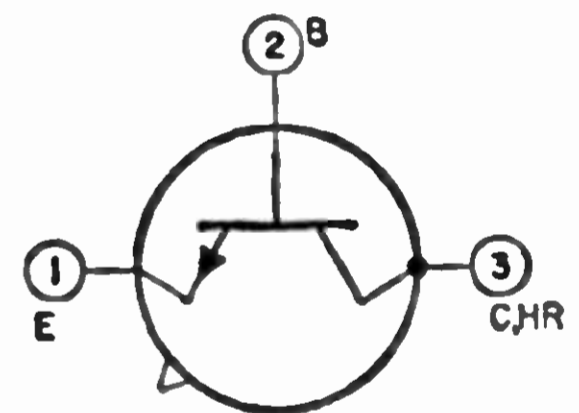
T_A up to 25°C.....	P_T	1	W
T_A above 25°C	P_T	See curve	page 300

CHARACTERISTICS (At case temperature = 25°C)

Thermal Resistance, Junction-to-Ambient	θ_{J-A}	150 max	°C/W
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40455 TRANSISTOR

Si n-p-n epitaxial planar type used in high-voltage, high-current audio and video amplifier service in commercial and industrial equipment. JEDEC TO-104 (with heat radiator), Outline No.33. This type is identical with type 40399 except for the following items:



MAXIMUM RATINGS

Transistor Dissipation:

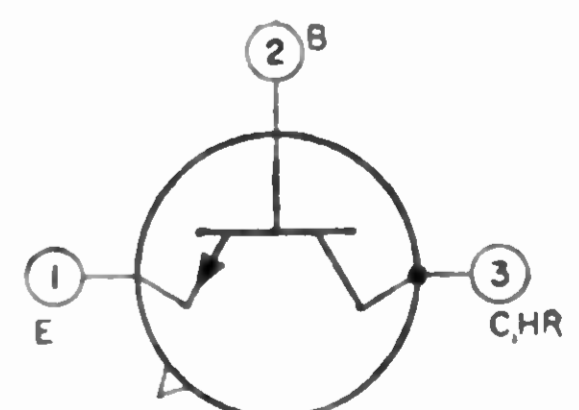
T_A up to 25°C.....	P_T	1	W
T_A above 25°C	P_T	See curve	page 300

CHARACTERISTICS (At case temperature = 25°C)

Thermal Resistance, Junction-to-Ambient	θ_{J-A}	150 max	°C/W
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40456 TRANSISTOR

Si n-p-n epitaxial planar type used in high-voltage, high-current audio and video amplifier service in commercial and industrial equipment. JEDEC TO-104 (with heat radiator), Outline No.33. This type is identical with type 40400 except for the following items:



MAXIMUM RATINGS

Transistor Dissipation:

T_A up to 25°C.....	P_T	1	W
T_A above 25°C	P_T	See curve	page 300

CHARACTERISTICS (At case temperature = 25°C)

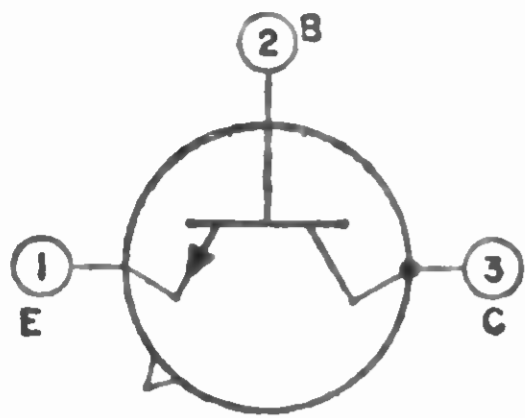
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	150 max	°C/W
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40457

Refer to Chart of Discontinued Transistors

TRANSISTOR

40458



Si n-p-n double-diffused epitaxial planar type used in high-peak-current audio and video amplifier applications in commercial and industrial equipment and high-current switching and driver service in computer equipment. JEDEC TO-104, Outline No.32.

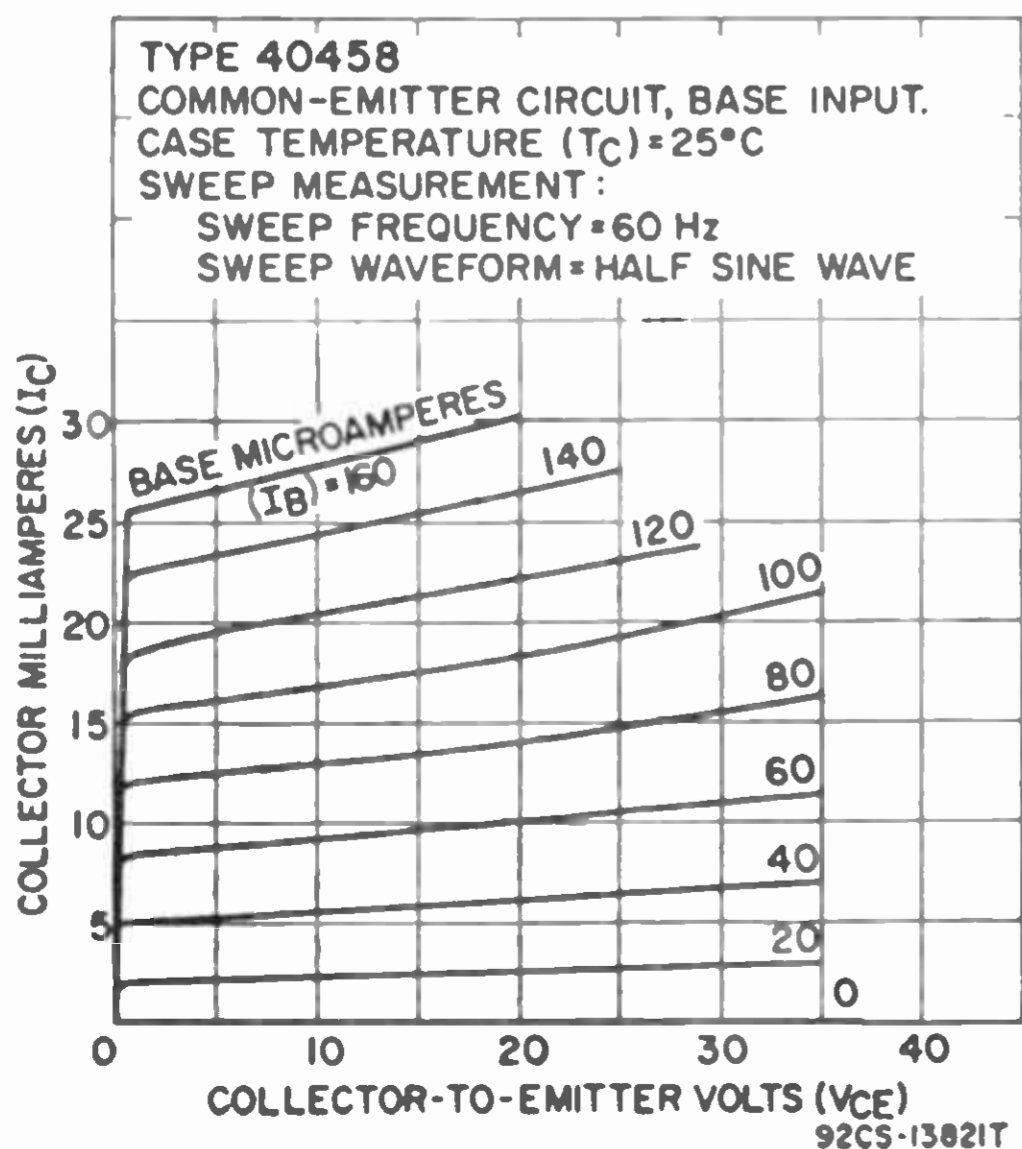
MAXIMUM RATINGS

Collector-to-Base Voltage	V _{CB0}	60	V
Collector-to-Emitter Voltage	V _{CE0}	40	V
Emitter-to-Base Voltage	V _{EB0}	8	V
Collector Current	I _C	1	A
Transistor Dissipation:			
T _A up to 25°C	P _T	0.5	W
T _A above 25°C	P _T	Derate linearly 3.3	mW/°C
T _c up to 75°C	P _T	2	W
T _c above 75°C	P _T	Derate linearly 20	mW/°C
Temperature Range:			
Operating (Junction)	T _J (opr)	-65 to 175	°C
Storage	T _{STG}	-65 to 175	°C
Lead-Soldering Temperature (10 s max)	T _L	265	°C

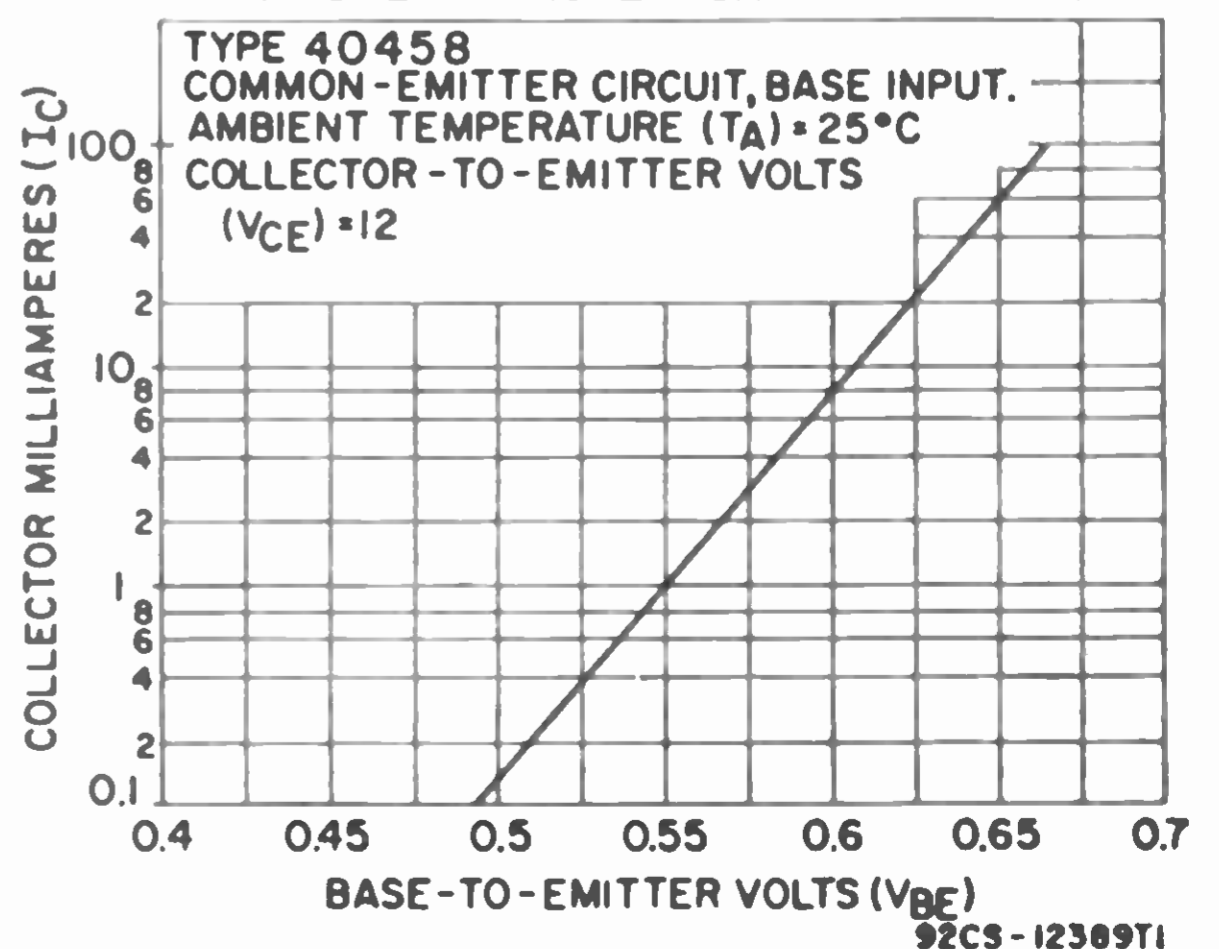
CHARACTERISTICS

Collector-to-Base Breakdown Voltage (I _C = 0.1 mA, I _E = 0)	V _{(BR)CBO}	60 min	V
Emitter-to-Base Breakdown Voltage (I _E = 0.05 mA, I _C = 0)	V _{(BR)EBO}	8 min	V
Collector-to-Emitter Breakdown Voltage (I _C = 100 mA, I _B = 0, t _p = 300 μs, df = 0.018%)	V _{(BR)CEO (sus)}	40 min	V
Collector-to-Emitter Saturation Voltage (I _C = 300 mA, I _B = 15 mA)	V _{CE (sat)}	0.24 typ; 0.3 max	V
Base-to-Emitter Saturation Voltage (I _C = 300 mA, I _B = 15 mA)	V _{BE (sat)}	0.93 typ; 1.5 max	V
Collector-Cutoff Current:			
V _{CB} = 25 V, I _E = 0	I _{CBO}	10 max	nA
V _{CB} = 25 V, I _E = 0, T _A = 85°C	I _{CBO}	1 max	μA
Emitter-Cutoff Current (V _{EB} = 2.5 V, I _C = 0)	I _{EBO}	10 max	nA
Static Forward-Current Transfer Ratio:			
V _{CE} = 10 V, I _C = 10 mA	h _{FE}	100 to 300	
V _{CE} = 10 V, I _C = 150 mA	h _{FE}	150	
V _{CE} = 1 V, I _C = 300 mA	h _{FE}	50 min; 75 typ	
Small-Signal Forward-Current Transfer Ratio			
V _{CE} = 12 V, I _C = 10 mA, f = 1 kHz)	h _{fe}	75 min; 175 typ	
Gain-Bandwidth Product (V _{CE} = 1 V, I _C = 50 mA, f = 50 MHz)	f _T	150 min; 200 typ	MHz
Feedback Capacitance* (V _{CB} = 6 V, I _E = 0, f = 1 MHz)	C _{cb}	20 max	pF
Small-Signal Input Impedance (V _{CE} = 12 V, I _C = 10 mA, f = 1 kHz)	h _{ie}	600	Ω
Small-Signal Output Impedance (V _{CE} = 12 V, I _C = 10 mA, f = 1 kHz)	h _{oe}	75	mmhos

TYPICAL COLLECTOR CHARACTERISTICS



TYPICAL TRANSFER CHARACTERISTIC



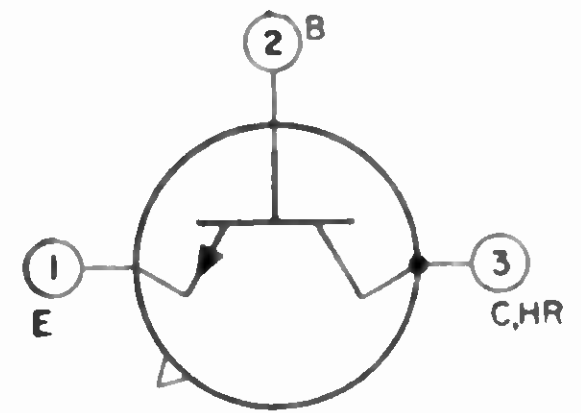
CHARACTERISTICS (cont'd)

Small-Signal Reverse-Voltage Transfer Ratio ($V_{CE} = 12\text{ V}$, $I_C = 10\text{ mA}$, $f = 1\text{ kHz}$)	h_{re}	125×10^{-6}	
Intrinsic Base-Spreading Resistance ($V_{CE} = 6\text{ V}$, $I_C = 1\text{ mA}$, $f = 100\text{ MHz}$)	$r_{bb'}$	20	Ω
Thermal Resistance, Junction-to-Case	θ_{J-C}	50 max	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	300 max	$^{\circ}\text{C}/\text{W}$

* Three-terminal measurement with lead No. 1 (emitter) guarded.

40459 TRANSISTOR

Si n-p-n double-diffused epitaxial planar type used in high-peak-current audio and video amplifier applications in commercial and industrial equipment and high-current switching and driver service in computer equipment. JEDEC TO-104 (with heat radiator), Outline No.33. This type is identical with type 40458 except for the following items:



MAXIMUM RATINGS

Transistor Dissipation:			
T_A up to 25°C	P_T	1	W
T_A above 25°C	P_T	Derate linearly 6.6	$\text{mW}^{\circ}\text{C}$

CHARACTERISTICS

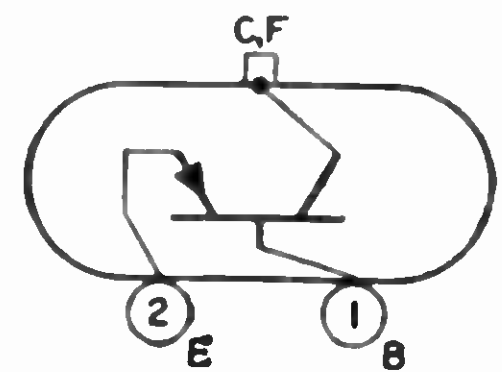
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	150 max	$^{\circ}\text{C}/\text{W}$
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40460 Refer to Chart of Discontinued Transistors

40461 Refer to Chart of Discontinued Transistors

40462 POWER TRANSISTOR

Ge p-n-p alloy-junction type used in high-fidelity class B af amplifier service in push-pull and "single-ended push-pull" circuits. JEDEC TO-3, Outline No.2.



MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	-40	V
Collector-to-Emitter Voltage	V_{CEO}	-40	V
Emitter-to-Base Voltage	V_{EBO}	-5	V
Collector Current	I_C	-5	A
Base Current	I_B	-1	A
Transistor Dissipation:			
T_{MF} up to 81°C	P_T	12.5	W
T_{MF} above 81°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(\text{opr})$	-65 to 100	$^{\circ}\text{C}$
Storage	T_{STG}	-65 to 100	$^{\circ}\text{C}$
Pin-Soldering Temperature (10 s max)	T_P	255	$^{\circ}\text{C}$

CHARACTERISTICS (At mounting-flange temperature = 25°C)

Collector-to-Base Breakdown Voltage ($I_C = -0.005\text{ A}$, $I_E = 0$)	$V_{(BR)CBO}$	-40 min	V
Collector-to-Emitter Breakdown Voltage ($I_C = -0.6\text{ A}$, $R_{BE} = 68\ \Omega$)	$V_{(BR)CER}$	-40 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -2\text{ mA}$, $I_C = 0$)	$V_{(BR)EBO}$	-5 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 5\text{ A}$, $I_B = -0.5\text{ A}$)	$V_{CE(\text{sat})}$	1 max	V
Base-to-Emitter Voltage ($V_{CE} = -10\text{ V}$, $I_C = -0.05\text{ A}$)	V_{BE}	-0.19	V

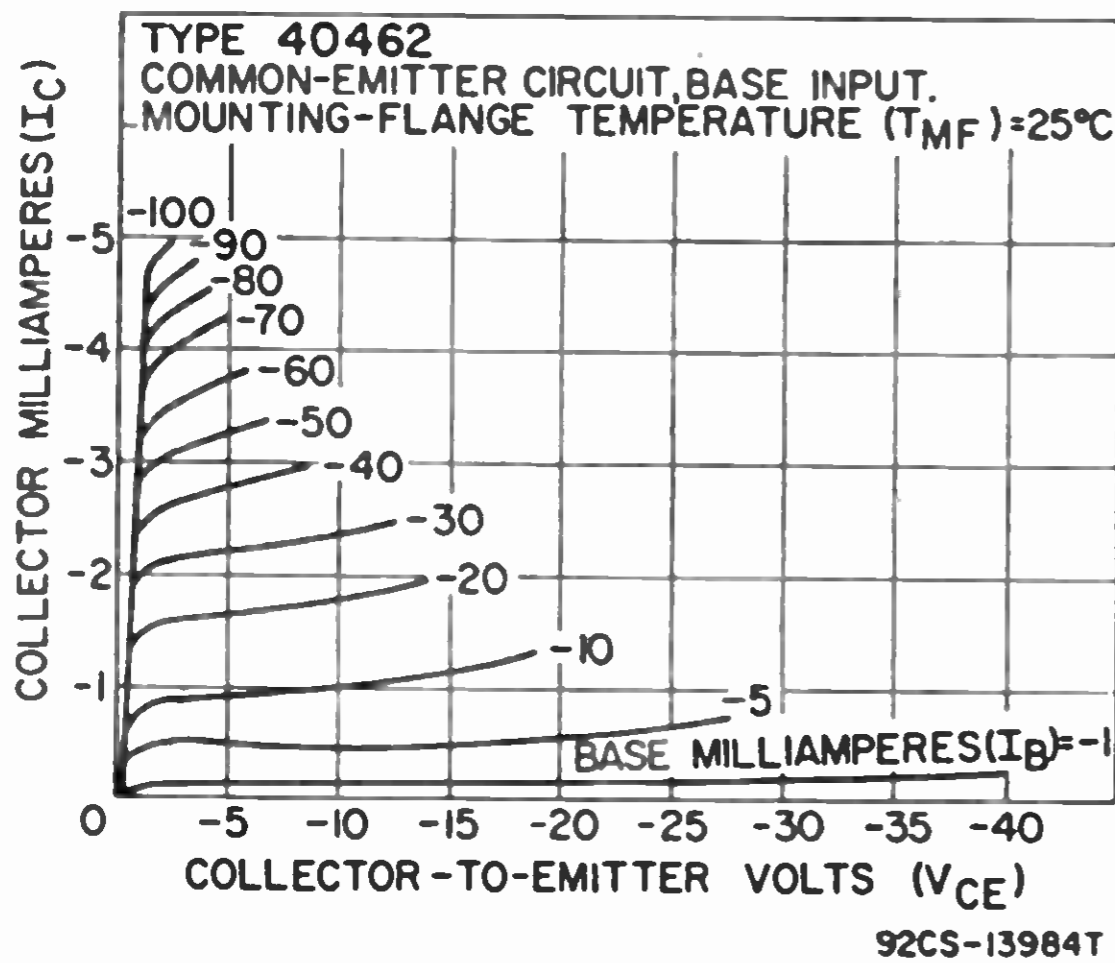
CHARACTERISTICS (cont'd)

Collector-Cutoff Current:			
$V_{CB} = -30\text{ V}, I_E = 0$	I_{CBO}	-0.5 max	mA
$V_{CB} = -0.5\text{ V}, I_E = 0$	$I_{CBO}(\text{sat})$	-0.1 max	mA
Static Forward-Current Transfer Ratio			
($V_{CE} = -2\text{ V}, I_C = -1\text{ A}$)	h_{FE}	50 min; 90 typ	
Gain-Bandwidth Product ($V_{CE} = 5\text{ V}, I_C = -0.5\text{ A}$)	f_T	600	kHz
Thermal Resistance, Junction-to-Case	θ_{J-C}	1.5 max	$^{\circ}\text{C}/\text{W}$

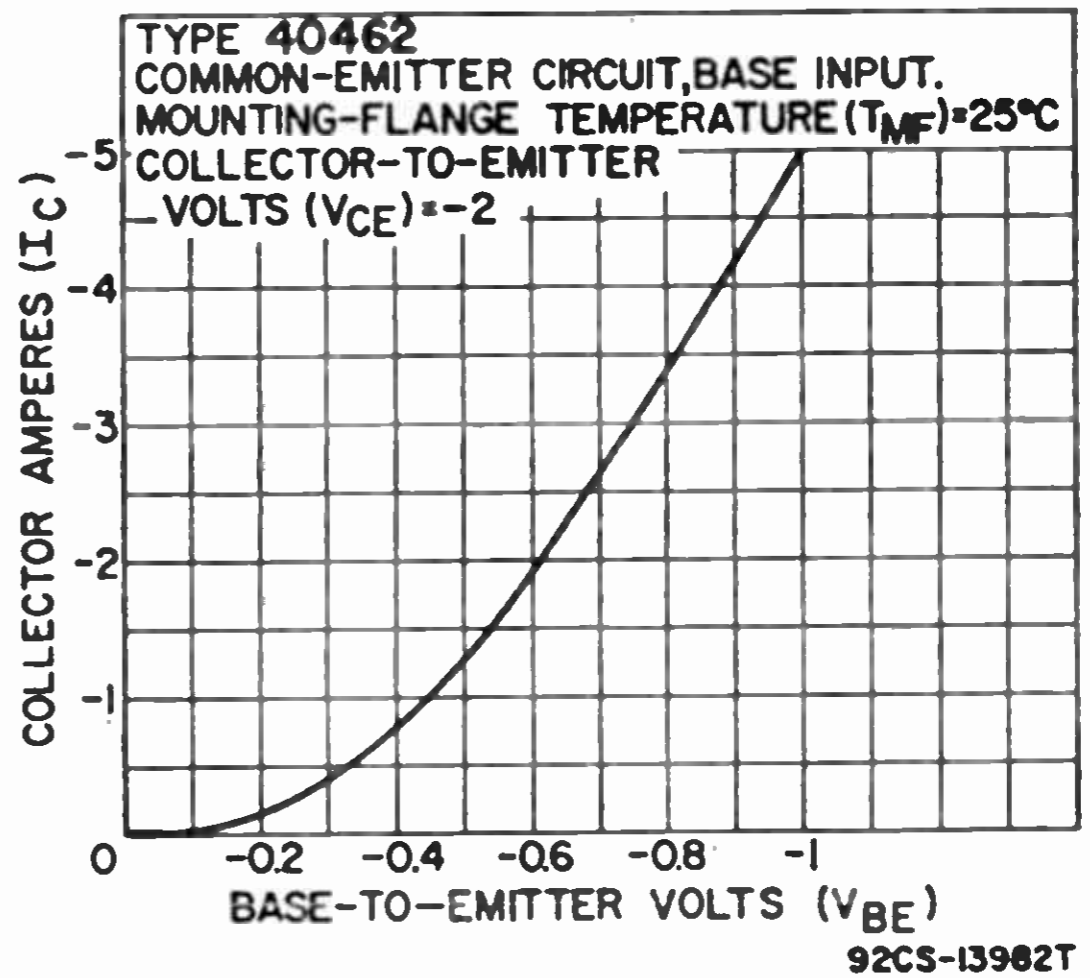
TYPICAL OPERATION IN "SINGLE-ENDED PUSH-PULL" CLASS B AF-AMPLIFIER CIRCUIT (At mounting-flange temperature = 25°C)

DC Collector Supply Voltage	V_{CC}	18	V
Zero-Signal DC Collector Current	I_C	-12	mA
Zero-Signal Base-Bias Voltage		-0.15	V
Peak Collector Current	I_{CM}	-2.8	A
Maximum-Signal DC Collector Current	I_C	-1	A
Input Impedance of Stage (per base)		32	Ω
Load Impedance (speaker voice-coil)	R_L	4	Ω
Maximum Collector Dissipation (per transistor) under worst-case conditions		7.5	W
EIA Music Power-Output Rating		25	W
Power Gain	G_{PE}	25	dB
Maximum-Signal Power Output	P_{OE}	15	W
Total Harmonic Distortion at Maximum-Signal Power Output		5	%

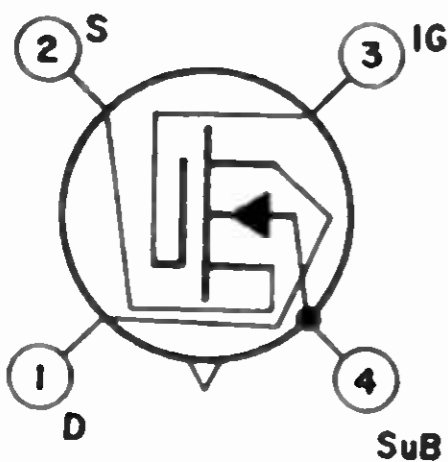
TYPICAL COLLECTOR CHARACTERISTICS



TYPICAL TRANSFER CHARACTERISTIC



- Refer to Chart of Discontinued Transistors **40464**
- Refer to Chart of Discontinued Transistors **40465**
- Refer to Chart of Discontinued Transistors **40466**
- Refer to Chart of Discontinued Transistors **40467**



FIELD-EFFECT TRANSISTOR 40467A

Si insulated-gate field-effect (MOS) n-channel depletion type used in vhf tuners and other vhf amplifier applications in industrial and commercial electronic equipment. JEDEC TO-72, Outline No.28.

MAXIMUM RATINGS

Drain-to-Source Voltage	V_{DS}	20	V
Gate-to-Source Voltage:			
Continuous (dc)	V_{GS}	-8 to 1	V
Peak (ac)	V_{GS}	± 15	V
Drain-to-Gate Voltage	V_{DG}	20	V
Drain Current ($t_P \leq 20\text{ ms}, df \leq 0.15$)	$I_D(\text{pulsed})$	50	mA

MAXIMUM RATINGS (cont'd)

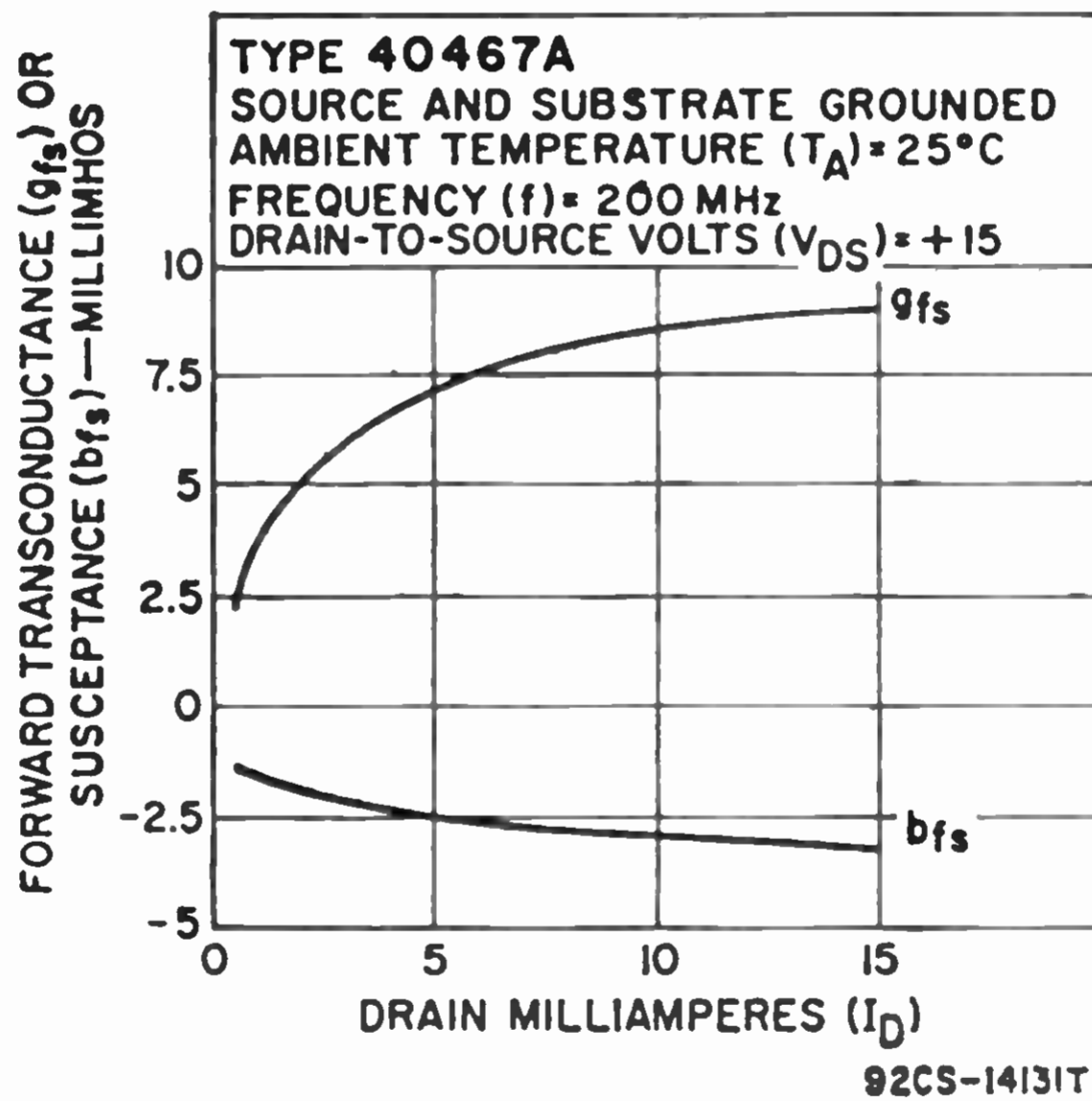
Transistor Dissipation:

T_A up to 25°C	P_T	400	mW
T_A above 25°C	P_T	Derate at 2.67	mW/°C
Temperature Range:			
Operating	T_{opr}	-65 to 175	°C
Storage	T_{stg}	-65 to 175	°C
Lead-Soldering Temperature (10 s max)	T_L	265	°C

CHARACTERISTICS

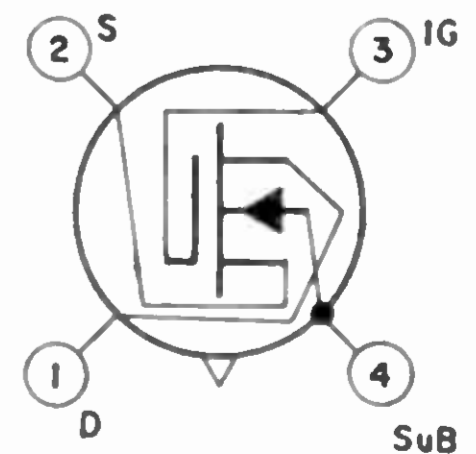
Gate-to-Source Cutoff Voltage ($V_{DS} = 12$ V, $I_D = 0.1$ mA)	$V_{GS}(off)$	-5 typ; -8 max	V
Gate Leakage Current:			
$V_{GS} = 1$ V, $V_{DS} = 0$	I_{GSS}	1 max	nA
$V_{GS} = -8$ V, $V_{DS} = 0$	I_{GSS}	1 max	nA
Zero-Bias Drain Current ($V_{DS} = 15$ V, $V_{GS} = 0$, $t_P \leq 20$ ms, $df \leq 0.15$) ...	$I_{DSS}(pulsed)$	10 to 50	mA
Small-Signal, Forward Transconductance ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 1$ kHz)	g_{fs}	4000 min; 7500 typ	μ mhos
Drain-to-Source Channel Resistance ($V_{DS} = 0$, $I_D = 0$, $f = 1$ kHz)	$r_{DS}(on)$	200	Ω
Input Resistance ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 200$ MHz)	r_{is}	2	k Ω
Output Resistance ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 200$ MHz)	r_{os}	3.6	k Ω
Small-Signal Reverse Transfer Capacitance ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 1$ MHz)	C_{rss}	0.05 to 0.2	pF
Maximum Available Power Gain ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 200$ MHz)	MAG	20	dB
Maximum Usable Power Gain, Unneutralized ($V_{CE} = 15$ V, $I_D = 5$ mA, $f = 200$ MHz)	MUG	12	dB
Maximum Usable Power Gain, Neutralized ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 200$ MHz)	MUG	12 min; 16 typ	dB
Noise Figure ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 200$ MHz)	NF	3.5 typ; 5 max	dB

TYPICAL FORWARD TRANSCONDUCTANCE CHARACTERISTICS



40468 FIELD-EFFECT TRANSISTOR

Si insulated-gate field-effect(MOS) n-channel depletion type used as an rf amplifier in receivers covering the 88-to-108-MHz band and for general amplifier applications at frequencies up to 125 MHz. JEDEC TO-104, Outline No.31. For typical forward transconductance curves, refer to type 3N142.



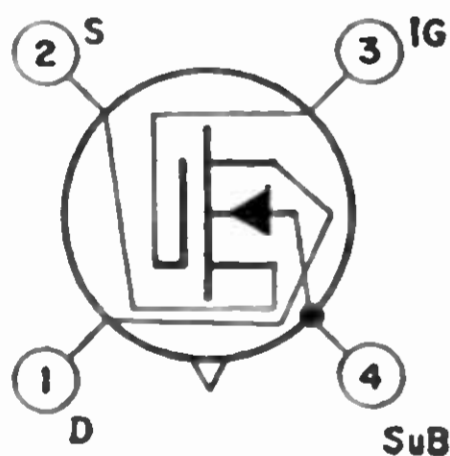
MAXIMUM RATINGS

Drain-to-Source Voltage	V_{DS}	20	V
Gate-to-Source Voltage:			
Continuous	V_{GS}	-8 to 0	V
Peak	V_{GS}	± 15	V

Drain Current	I_D	20	mA
Transistor Dissipation:	P_T	100	mW
T_A up to 100°C	P_T	Derate at 4	mW/°C
T_A above 100°C			
Temperature Range:			
Operating	$T(\text{opr})$	-65 to 125	°C
Storage	T_{STG}	-65 to 125	°C
Lead-Soldering Temperature (10 s max)	T_L	265	°C

CHARACTERISTICS

Gate-to-Source Cutoff Voltage ($V_{DS} = 20$ V, $I_D = 0.05$ mA)	$V_{GS}(\text{off})$	-4 typ; -6 max	V
Gate Reverse Current ($V_{GS} = -8$ V, $V_{DS} = 0$) ...	I_{GSS}	0.2 max	nA
Zero-Gate-Voltage Drain Current ($V_{DS} = 15$ V, $V_{GS} = 0$)	I_{DSS}	5 to 50	mA
Small-Signal Reverse-Transfer Capacitance, Drain-to-Gate ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 1$ MHz)	C_{rss}	0.1 to 0.2	pF
Input Resistance ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 100$ MHz)	r_{iss}	2 min; 4.5 typ	kΩ
Output Resistance ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 100$ MHz)	r_{oss}	2.25 min; 4.2 typ	kΩ
Input Capacitance ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 100$ MHz)	C_{iss}	5.5 typ; 10 max	pF
Output Capacitance ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 100$ MHz)	C_{oss}	1.4	pF
Magnitude of Forward Transadmittance ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 100$ MHz)	$ y_{fs} $	7.5	mmhos
Maximum Available Power Gain ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 100$ MHz)	MAG	24	dB
Maximum Usable Power Gain, Unneutralized ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 100$ MHz)	MUG	14	dB
Maximum Usable Power Gain, Neutralized ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 100$ MHz)	MUG	14 min; 17 typ	dB
Noise Figure ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 100$ MHz)	NF	4 typ; 5 max	dB



FIELD-EFFECT TRANSISTOR 40468A

Si insulated-gate field-effect (MOS) n-channel depletion type used in rf-amplifier applications in FM receivers covering the 88-to-108-MHz band, and in general amplifier applications at frequencies up to 125 MHz. JEDEC TO-72, Outline No.28.

MAXIMUM RATINGS

Drain-to-Source Voltage	V_{DS}	20	V
Gate-to-Source Voltage:			
Continuous	V_{GS}	-8 to 1	V
Peak	V_{GS}	±15	V
Drain-to-Gate Voltage	V_{DG}	20	V
Drain Current ($t_P \leq 20$ ms, $df \leq 0.15$)	$I_D(\text{pulsed})$	25	mA
Transistor Dissipation:			
T_A up to 25°C	P_T	375	mW
T_A above 25°C	P_T	Derate at 2.5	mW/°C
Temperature Range:			
Operating	$T(\text{opr})$	-65 to 175	°C
Storage	T_{STG}	-65 to 175	°C
Lead-Soldering Temperature (10 s max)	T_L	265	°C

CHARACTERISTICS

Drain-to-Source Cutoff Current ($V_{DS} = 12$ V, $V_{GS} = -8$ V)	$I_D(\text{off})$	100 max	μA
Gate Leakage Current:			
$V_{GS} = -8$ V, $V_{DS} = 0$	I_{GSS}	1 max	nA
$V_{GS} = 1$ V, $V_{DS} = 0$	I_{GSS}	1 max	nA
Zero-Bias Drain Current ($V_{DS} = 15$ V, $V_{GS} = 0$, $t_P \leq 20$ ms, $df \leq 0.15$)	$I_{DSS}(\text{pulsed})$	5 to 25	mA
Small-Signal Forward Transconductance ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 1$ kHz)	g_{fs}	7500	μmhos
Small-Signal Reverse-Transfer Capacitance, Drain-to-Gate ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 1$ MHz)	C_{rss}	0.12 typ; 0.2 max	pF

CHARACTERISTICS (cont'd)

Input Capacitance ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 1$ MHz)	C_{iss}	5.5 typ; 10 max	pF
Output Capacitance ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 1$ MHz)	C_{oss}	1.4	pF
Input Resistance ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 100$ MHz)	r_{iss}	2 min; 4.5 typ	k Ω
Output Resistance ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 100$ MHz)	r_{oss}	2.25 min; 4.2 typ	k Ω
Maximum Available Power Gain ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 100$ MHz)	MAG	24	dB
Maximum Usable Power Gain, Unneutralized ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 100$ MHz)	MUG	14	dB
Maximum Usable Power Gain, Neutralized ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 100$ MHz)	MUG	14 min; 17 typ	dB
Noise Figure ($V_{DS} = 15$ V, $I_D = 5$ mA, $f = 100$ MHz)	NF	3.5 typ; 5 max	dB

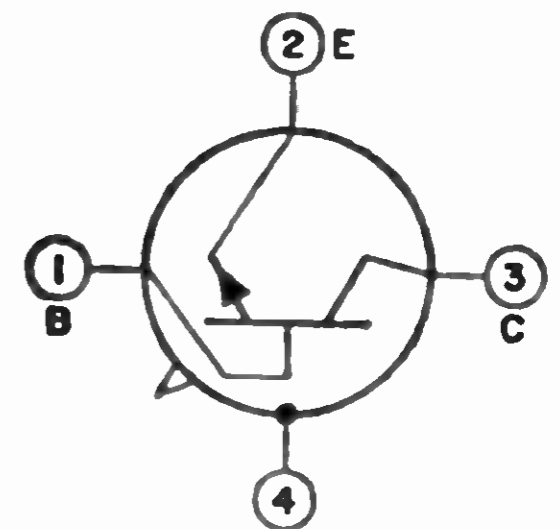
40469 Refer to Chart of Discontinued Transistors

40470 Refer to Chart of Discontinued Transistors

40471 Refer to Chart of Discontinued Transistors

40472**TRANSISTOR**

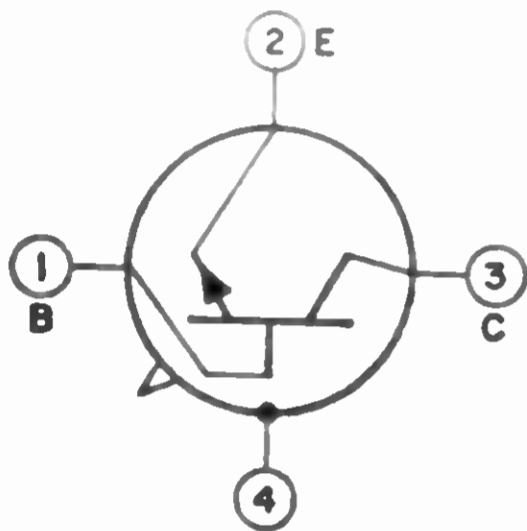
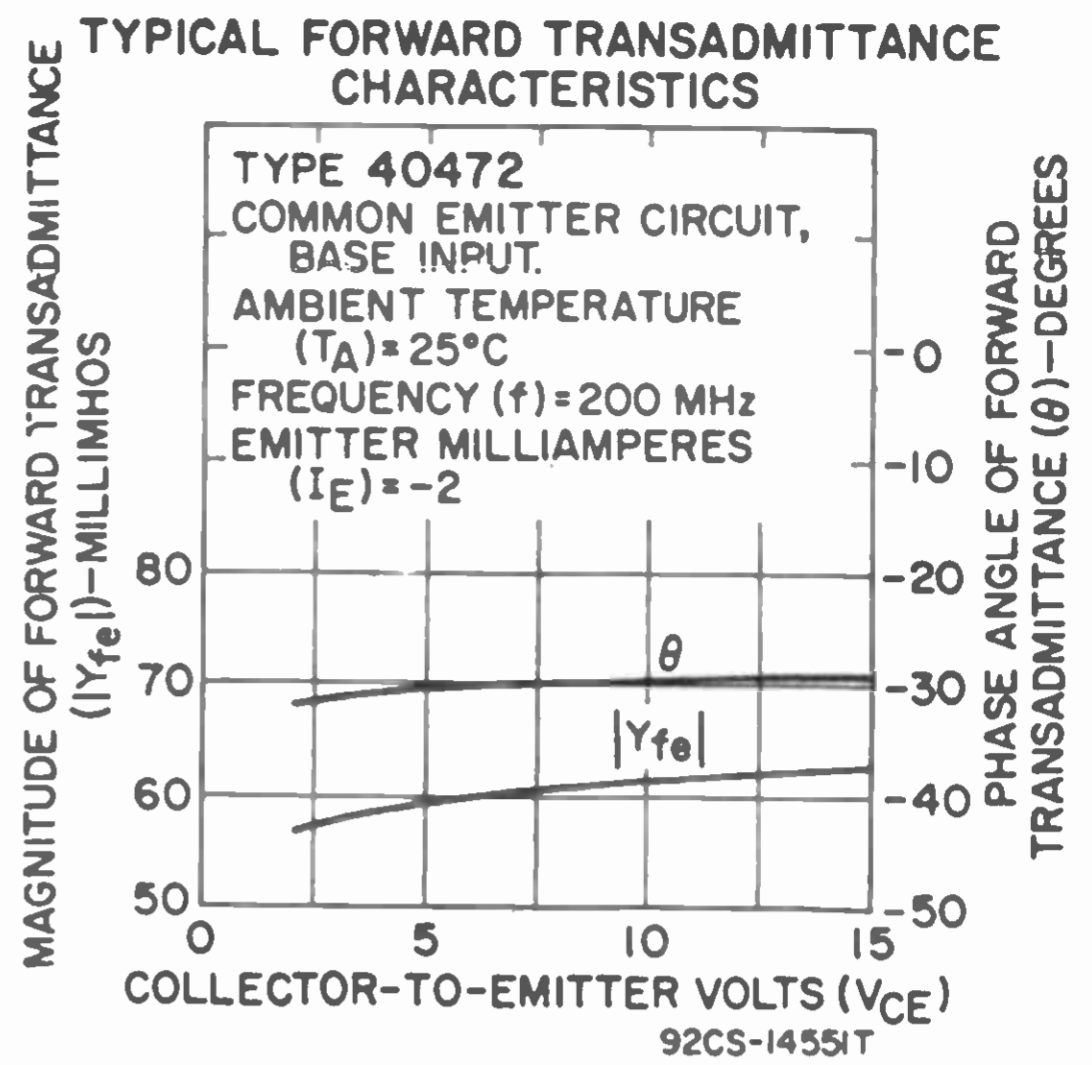
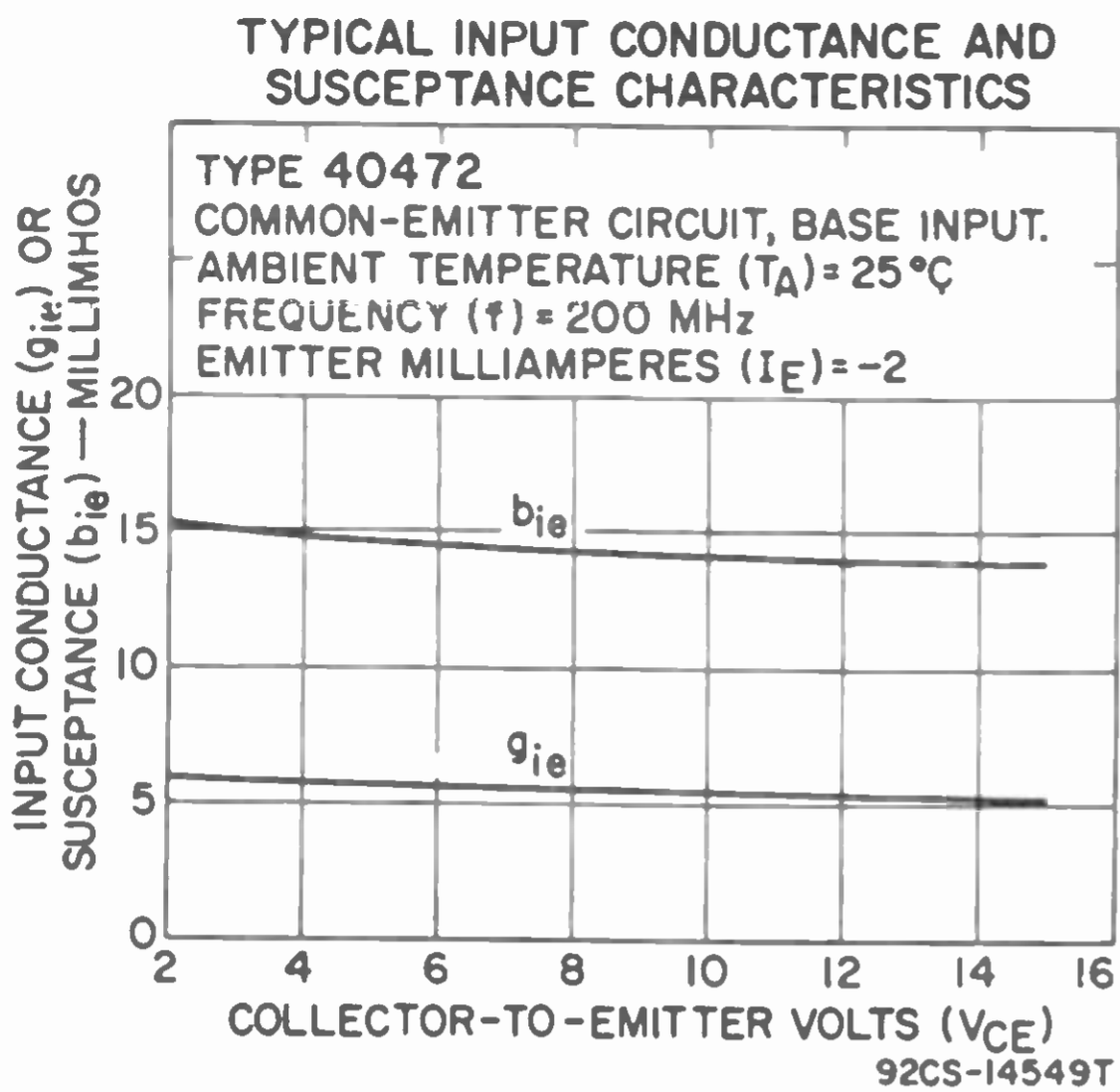
Si n-p-n type used as rf amplifier in television tuners covering channels 2 through 13. The terminal arrangement permits shielding between input and output terminals for superior high-frequency performance and greater circuit stability, particularly on printed-circuit boards. JEDEC TO-104, Outline No.31.

**MAXIMUM RATINGS**

Collector-to-Base Voltage	V_{CBO}	45	V
Emitter-to-Base Voltage	V_{EBO}	3	V
Collector Current	I_C	50	mA
Transistor Dissipation:			
T_A up to 25°C	P_T	180	mW
T_A above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating	T_A	-65 to 175	°C
Storage	T_{STG}	-65 to 175	°C
Lead-Soldering Temperature (10 s max)	T_L	255	°C

CHARACTERISTICS

Collector-Cutoff Current:			
$V_{CB} = 1$ V, $I_E = 0$	I_{CBO}	0.02 max	μ A
$V_{CB} = 45$ V, $I_E = 0$	I_{CBO}	1 max	μ A
Emitter-Cutoff Current ($V_{EB} = 3$ V, $I_C = 0$)	I_{EBO}	1 max	μ A
Static Forward-Current Transfer Ratio ($V_{CE} = 6$ V, $I_E = -1$ mA)	h_{FE}	40 to 170	
Gain-Bandwidth Product ($V_{CE} = 6$ V, $I_E = -2$ mA, $f = 100$ MHz)	f_T	900	MHz
Feedback Capacitance ($V_{CE} = 10$ V, $I_E = -2$ mA, $f = 200$ MHz)	C_{cb}	0.19	pF
Input Resistance ($V_{CE} = 10$ V, $I_E = -2$ mA, $f = 200$ MHz)	R_{ie}	180	Ω
Output Resistance ($V_{CE} = 10$ V, $I_E = -2$ mA, $f = 200$ MHz)	R_{oe}	5.5	k Ω
Magnitude of Forward Transadmittance ($V_{CE} = 10$ V, $I_E = -2$ mA, $f = 200$ MHz)	Y_{fe}	61	mmhos
Noise Figure ($V_{CE} = 10$ V, $I_E = -2$ mA, $R_s = 90$ Ω , $f = 200$ MHz)	NF	3.3	dB
Maximum Available Amplifier Gain ($V_{CE} = 10$ V, $I_E = -2$ mA, $f = 200$ MHz)	MAG	29.6	dB
Maximum Usable Amplifier Gain, Unneutralized ($V_{CE} = 10$ V, $I_E = -2$ mA, $f = 200$ MHz)	MUG	21.8	dB
Maximum Usable Amplifier Gain; Neutralized ($V_{CE} = 10$ V, $I_E = -2$ mA, $f = 200$ MHz)	MUG	26.9	dB



TRANSISTOR

40473

Si n-p-n type used as rf mixer in television tuners covering channels 2 through 13. The terminal arrangement permits shielding between input and output terminals for superior high-frequency performance and greater circuit stability, particularly on printed-circuit boards. JEDEC TO-104, Outline No.31. For maximum ratings, refer to type 40472.

CHARACTERISTICS

Collector-Cutoff Current:

$V_{CB} = 1 \text{ V}, I_E = 0$
 $V_{CB} = 45 \text{ V}, I_E = 0$

Emitter-Cutoff Current ($V_{EB} = 3 \text{ V}, I_C = 0$)

Static Forward-Current Transfer Ratio ($V_{CE} = 6 \text{ V}, I_E = -1 \text{ mA}$)

Gain-Bandwidth Product ($V_{CE} = 6 \text{ V}, I_E = -2 \text{ mA}, f = 100 \text{ MHz}$)

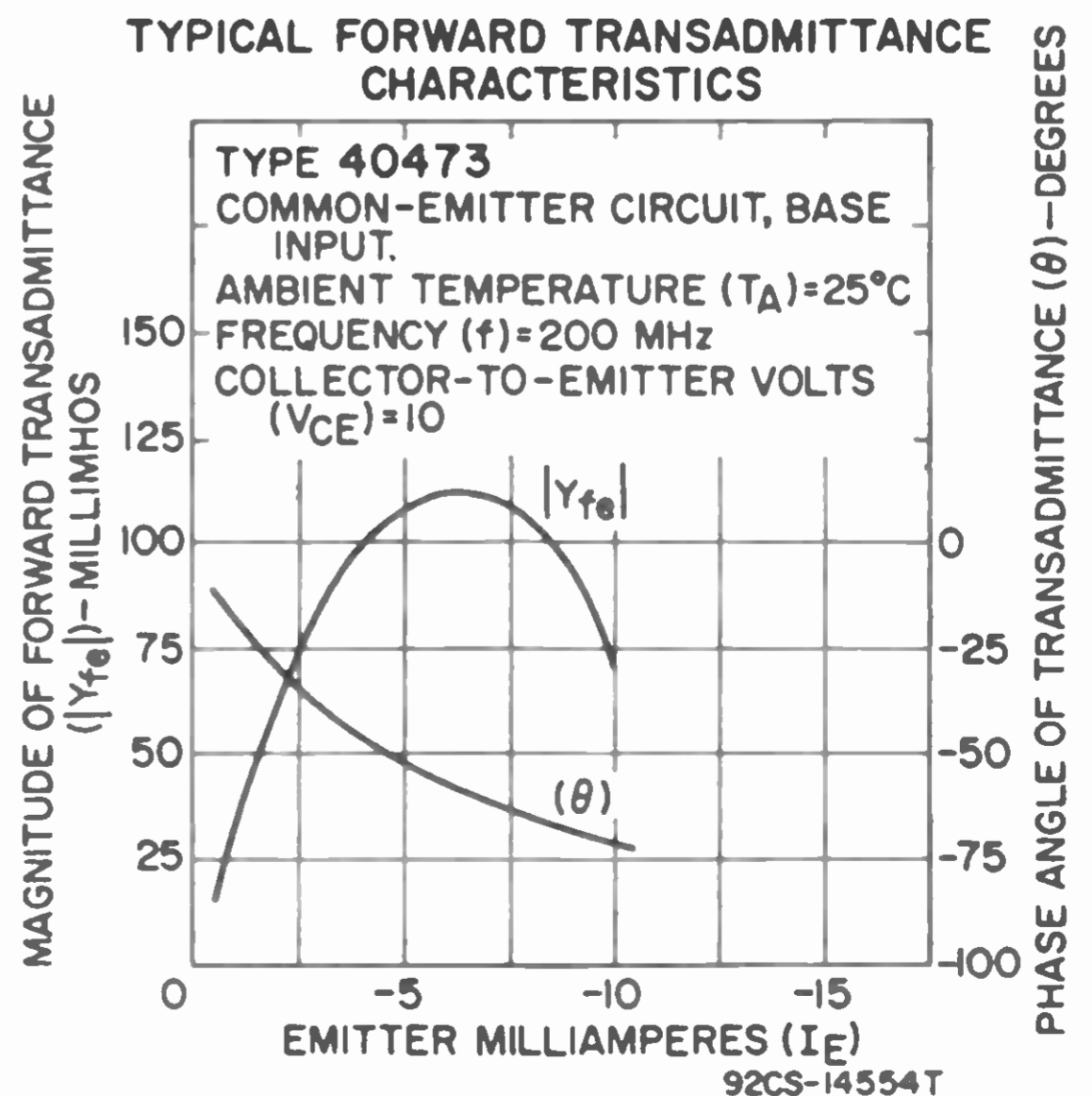
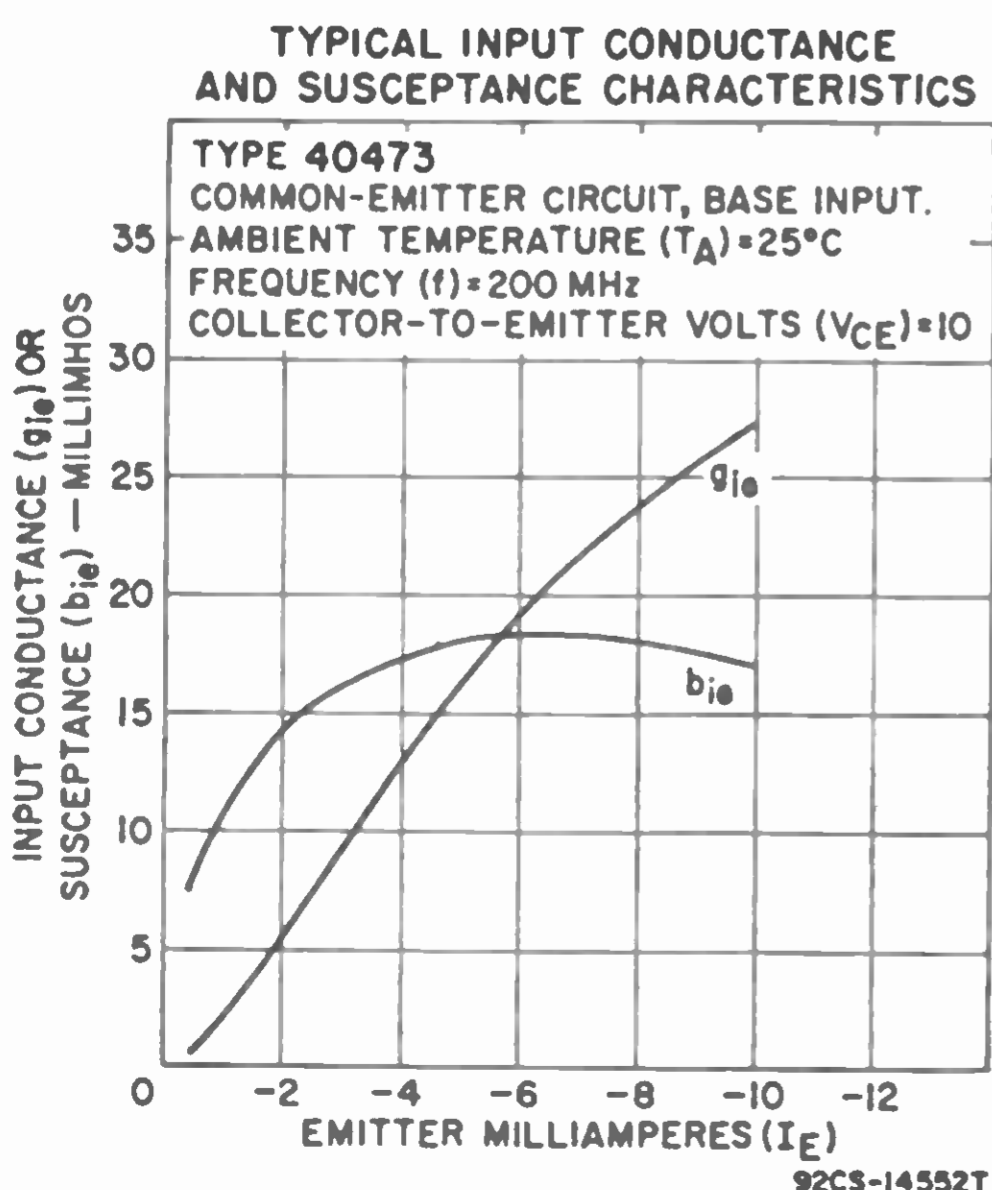
Feedback Capacitance ($V_{CE} = 12 \text{ V}, I_E = -1.5 \text{ mA}, f = 200 \text{ MHz}$)

Input Resistance ($V_{CE} = 12 \text{ V}, I_E = -1.5 \text{ mA}, f = 44 \text{ MHz}$)

Output Resistance ($V_{CE} = 12 \text{ V}, I_E = -1.5 \text{ mA}, f = 44 \text{ MHz}$)

Maximum Available Conversion Gain ($V_{CE} = 12 \text{ V}, I_E = -1.5 \text{ mA}, f = 200 \text{ to } 44 \text{ MHz}$)

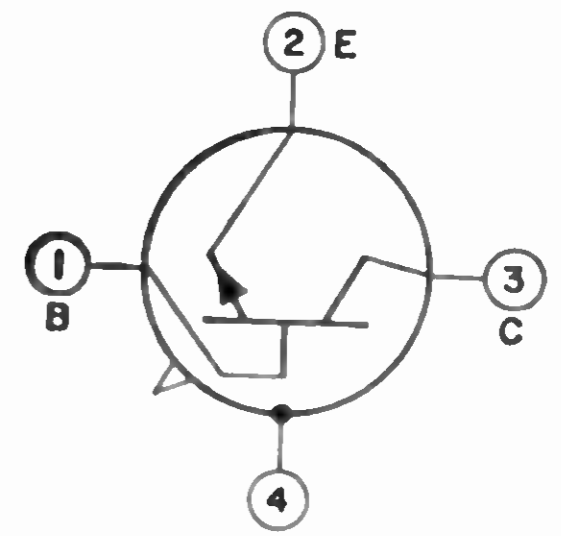
I_{CBO}	0.02 max	μA
I_{CBO}	1 max	μA
I_{EBO}	1 max	μA
h_{FE}	40 to 275	
f_T	900	MHz
C_{cb}	0.19	pF
R_{ie}	270	Ω
R_{oe}	4.6	k Ω
MAG_c	22.7	dB



40474

TRANSISTOR

Si n-p-n type used as rf oscillator in television tuners covering channels 2 through 13. The terminal arrangement permits shielding between input and output terminals for superior high-frequency performance and greater stability, particularly on printed-circuit boards. JEDEC TO-104, Outline No.31. For maximum ratings refer to type 40472.



CHARACTERISTICS

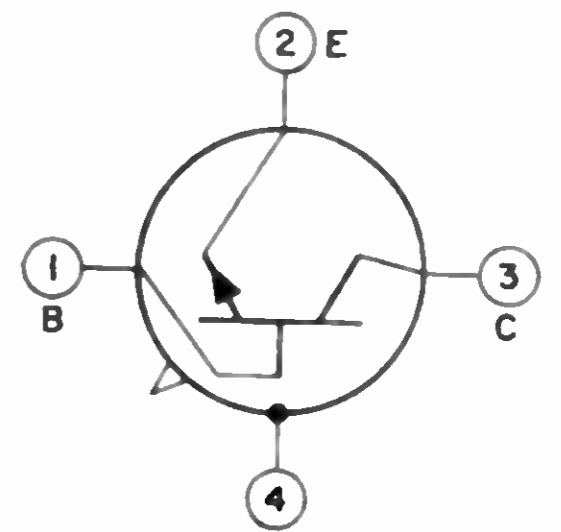
Collector-Cutoff Current:

$V_{CB} = 1\text{ V}, I_E = 0$	I_{CBO}	0.02 max	μA
$V_{CB} = 45\text{ V}, I_E = 0$	I_{CBO}	1 max	μA
Emitter-Cutoff Current ($V_{EB} = 3\text{ V}, I_C = 0$)	I_{EBO}	1 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 6\text{ V}, I_E = -1\text{ mA}$)	h_{FE}	27 to 275	
Gain-Bandwidth Product ($V_{CE} = 6\text{ V}, I_E = -2\text{ mA}, f = 100\text{ MHz}$)	f_T	900	MHz

40475

TRANSISTOR

Si n-p-n type used as 45-MHz if amplifier in television receivers. The terminal arrangement permits shielding between input and output terminals for superior high-frequency performance and greater circuit stability, particularly on printed-circuit boards. JEDEC TO-104, Outline No.31.



MAXIMUM RATINGS

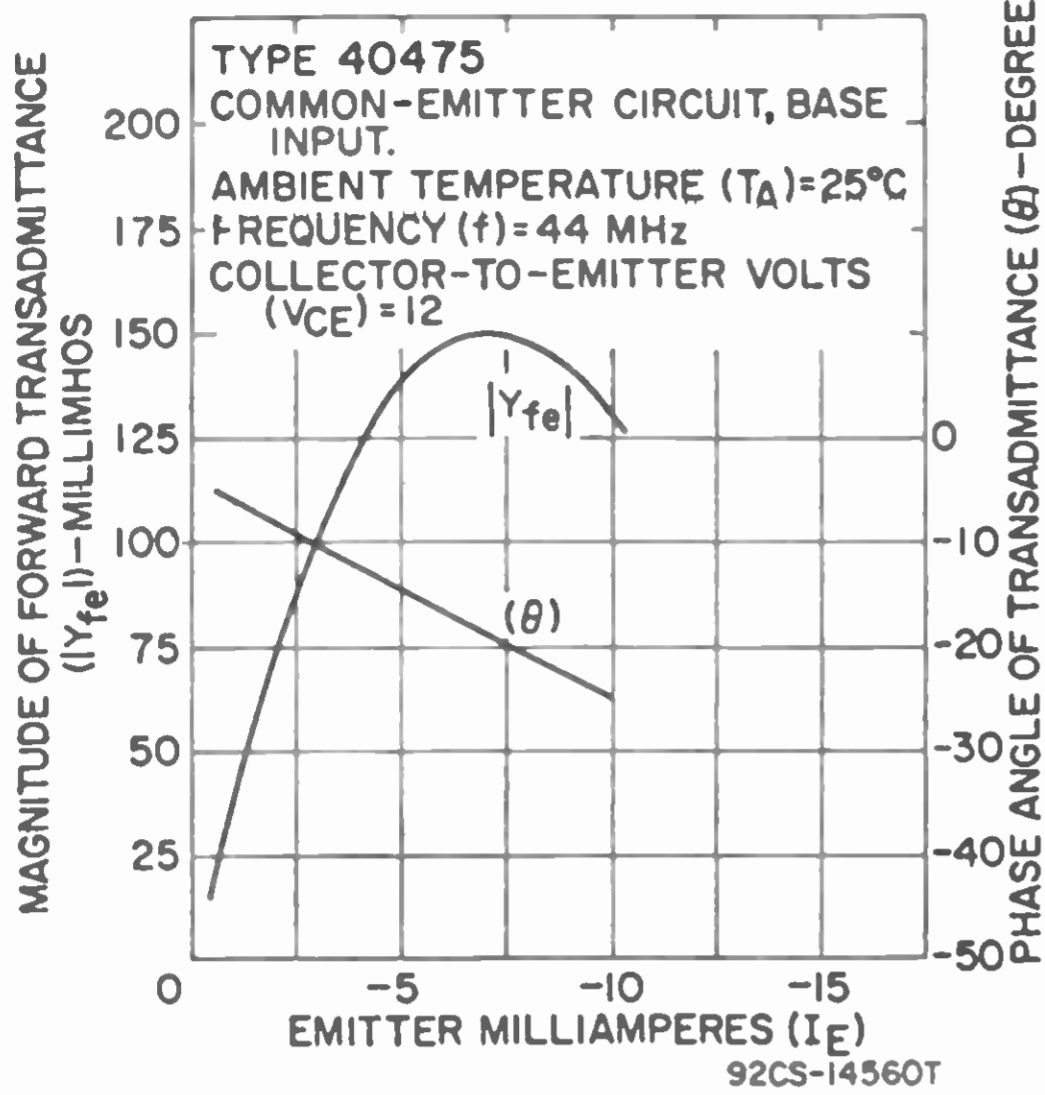
Collector-to-Base Voltage	V_{CBO}	45	V
Emitter-to-Base Voltage	V_{EBO}	3	V
Collector Current	I_C	50	mA
Transistor Dissipation:			
T_A up to 25°C	P_T	180	mW
T_A above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating	T_A	-65 to 175	°C
Storage	T_{STG}	-65 to 175	°C
Lead-Soldering Temperature (10 s max)	T_L	255	°C

CHARACTERISTICS

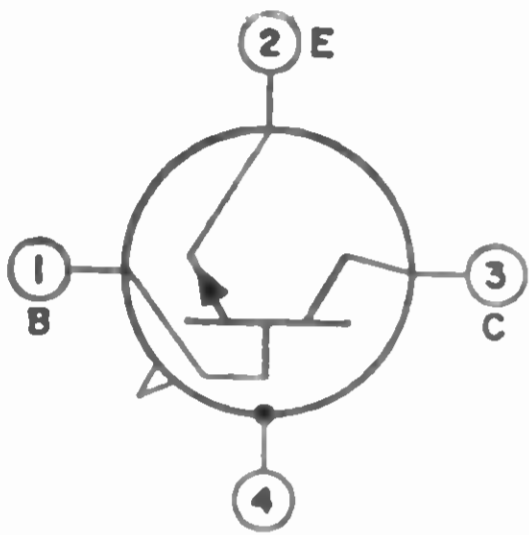
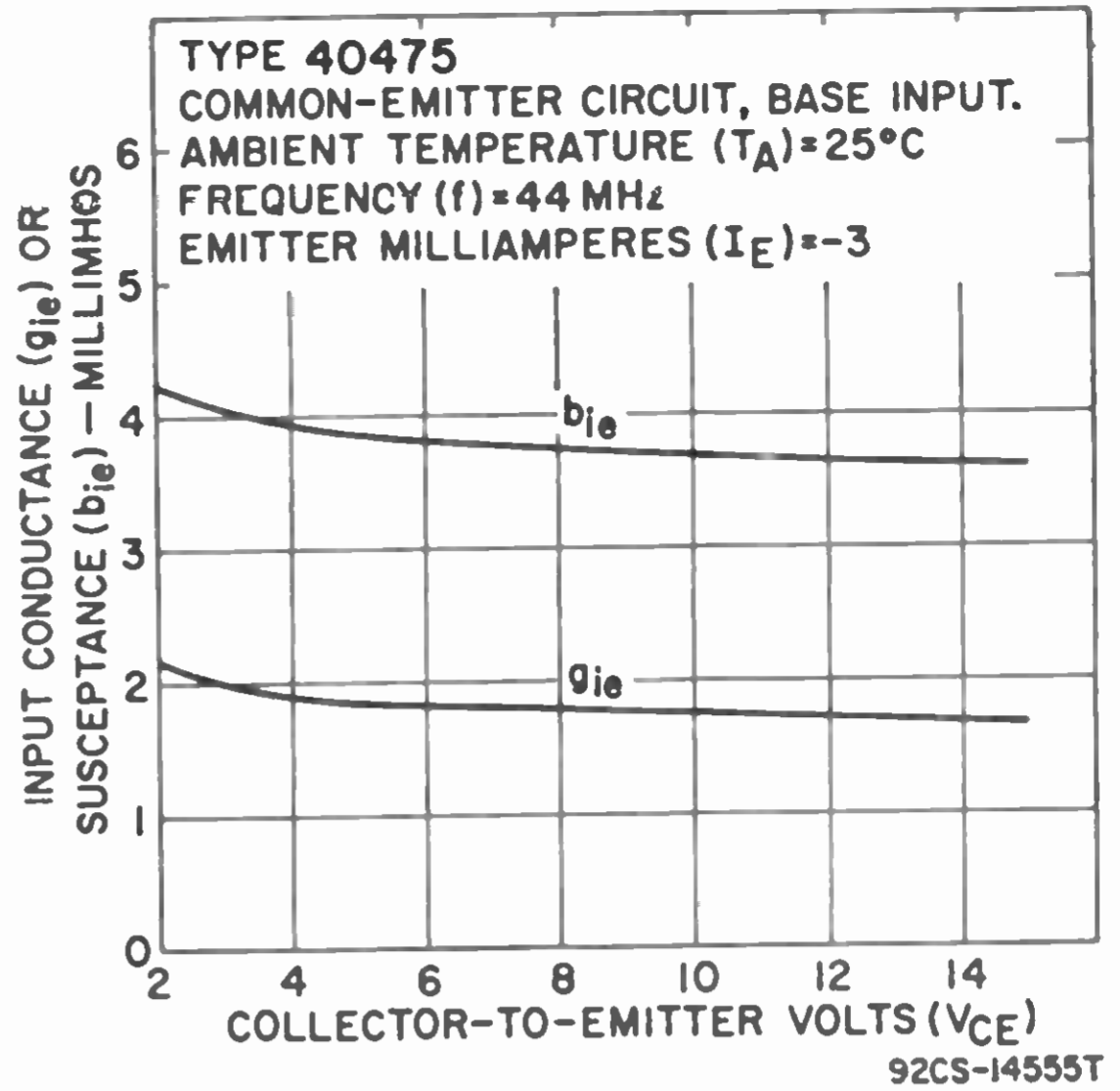
Collector-Cutoff Current:

$V_{CB} = 1\text{ V}, I_E = 0$	I_{CBO}	0.02 max	μA
$V_{CB} = 45\text{ V}, I_E = 0$	I_{CBO}	1 max	μA
Emitter-Cutoff Current ($V_{EB} = 3\text{ V}, I_C = 0$)	I_{EBO}	1 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 6\text{ V}, I_E = 1\text{ mA}$)	h_{FE}	40 to 170	
Gain-Bandwidth Product ($V_{CE} = 6\text{ V}, I_E = -2\text{ mA}, f = 100\text{ MHz}$)	f_T	800	MHz
Feedback Capacitance ($V_{CE} = 12\text{ V}, I_E = -3\text{ mA}, f = 44\text{ MHz}$)	C_{cb}	0.18	pF
Input Resistance ($V_{CE} = 12\text{ V}, I_E = -3\text{ mA}, f = 44\text{ MHz}$)	R_{ie}	575	Ω
Output Resistance ($V_{CE} = 12\text{ V}, I_E = -3\text{ mA}, f = 44\text{ MHz}$)	R_{oe}	25	k Ω
Magnitude of Forward Transadmittance ($V_{CE} = 12\text{ V}, I_E = -3\text{ mA}, f = 44\text{ MHz}$)	$ Y_{fe} $	100	mmhos
Maximum Available Amplifier Gain ($V_{CE} = 12\text{ V}, I_E = -3\text{ mA}, f = 44\text{ MHz}$)	MAG	45.6	dB
Maximum Usable Amplifier Gain Per Stage, Unneutralized ($V_{CE} = 12\text{ V}, I_E = -3\text{ mA}, f = 44\text{ MHz}$):			
For 1 stage	MUG	28.5	dB
For 2 stages	MUG	26.2	dB
For 3 stages	MUG	24.8	dB
Maximum Usable Amplifier Gain Per Stage, Neutralized ($V_{CE} = 12\text{ V}, I_E = -3\text{ mA}, f = 44\text{ MHz}$):			
For 1 stage	MUG	33.5	dB
For 2 stages	MUG	31.3	dB
For 3 stages	MUG	29.5	dB

TYPICAL FORWARD TRANSADMITTANCE CHARACTERISTICS



TYPICAL INPUT CONDUCTANCE AND SUSCEPTANCE CHARACTERISTICS



TRANSISTOR

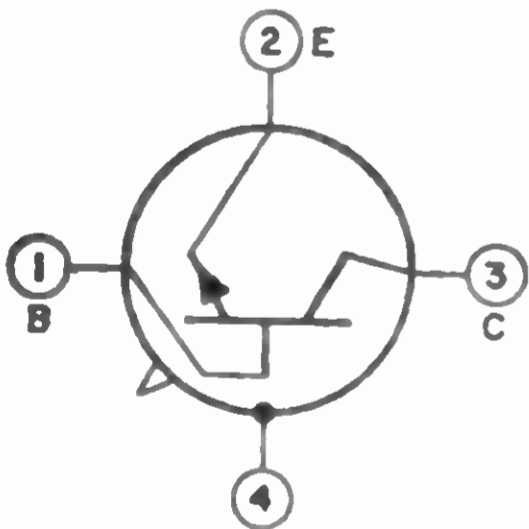
40476

Si n-p-n type used as 45-MHz if amplifier in television receivers. The terminal arrangement permits shielding between input and output terminals for superior high-frequency performance and greater circuit stability, particularly on printed-circuit boards. JEDEC TO-104, Outline No.31. This type is identical with 40475 except

for the following item:

CHARACTERISTICS

Static Forward-Current Transfer Ratio (V _{CE} = 6 V, I _E = -1 mA)	h_{FE}	27 to 100
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TRANSISTOR

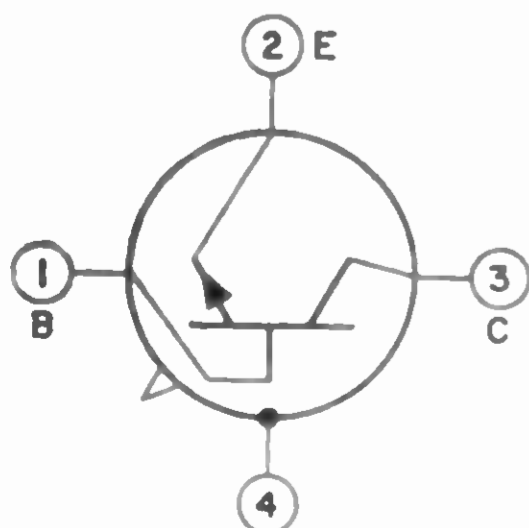
40477

Si n-p-n type used as 45-MHz if amplifier in television receivers. The terminal arrangement permits shielding between input and output terminals for superior high-frequency performance and greater circuit stability, particularly on printed-circuit boards. JEDEC TO-104, Outline No.31. This type is identical with 40475 except

for the following item:

CHARACTERISTICS

Static Forward-Current Transfer Ratio (V _{CE} = 6 V, I _E = -1 mA)	h_{FE}	27 to 275
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TRANSISTOR

40478

Si n-p-n type used in rf - amplifier applications in conjunction with types 40479 (mixer), 40480 (rf oscillator), and 40481 and 40482 (if amplifiers) to make up a "front-end" and if complement for FM and AM/FM receivers. The terminal arrangement permits shielding between input and output terminals for superior high-frequency performance and greater circuit stability, particularly on printed-circuit boards. JEDEC TO-104, Outline No.31.

MAXIMUM RATINGS

Collector-to-Base Voltage:

Emitter open	V_{CBO}	45	V
$V_{EB} = -1$ V	V_{CBV}	45	V
Emitter-to-Base Voltage	V_{EBO}	3	V
Collector Current	I_C	50	mA
Transistor Dissipation:			
T_A up to 25°C	P_T	180	mW
T_A above 25°C	P_T	See curve	page 300
Temperature Range:			
Operating	T_A	-65 to 175	°C
Storage	T_{STG}	-65 to 175	°C
Lead-Soldering Temperature (10 s max)	T_L	255	°C

V_{CBO}	45	V
V_{CBV}	45	V
V_{EBO}	3	V
I_C	50	mA
P_T	180	mW
P_T	See curve	page 300
T_A	-65 to 175	°C
T_{STG}	-65 to 175	°C
T_L	255	°C

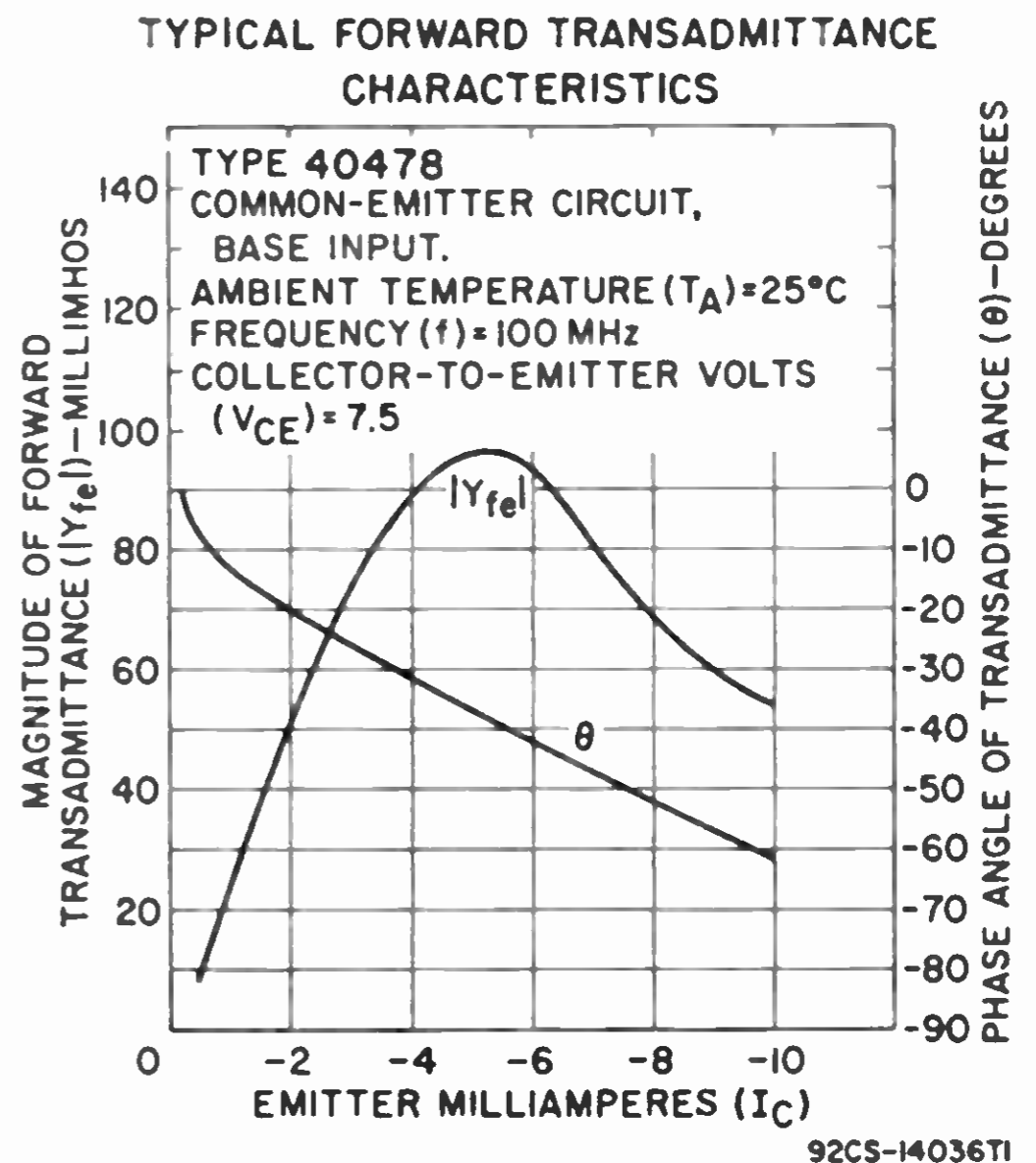
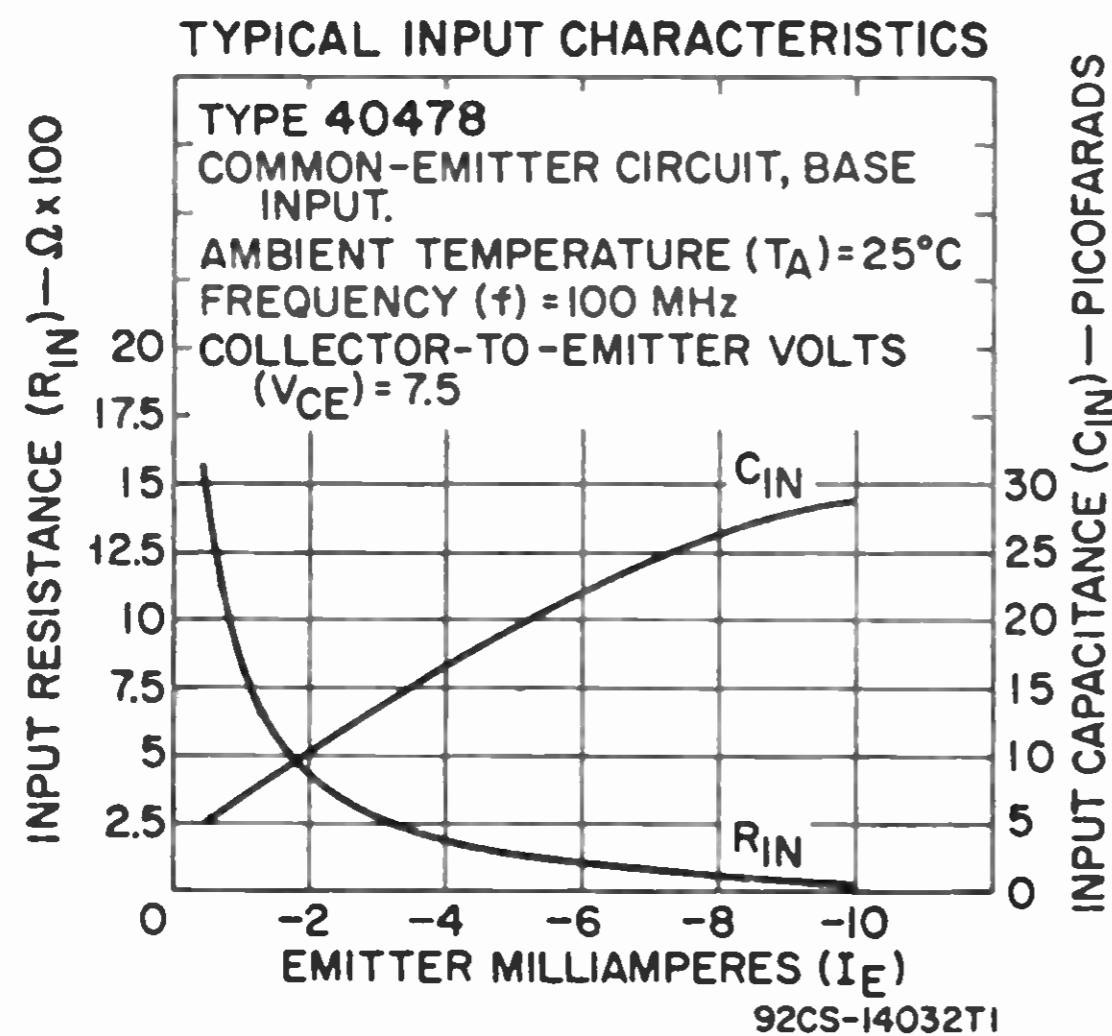
CHARACTERISTICS

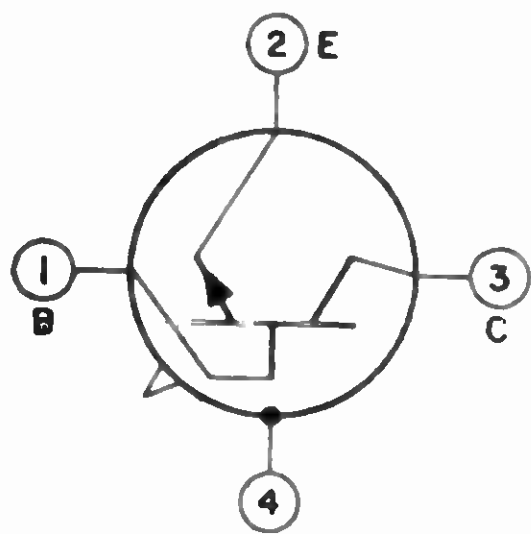
Collector-to-Base Breakdown Voltage:

$I_C = 0.001$ mA	$V_{(BR)CBO}$	45 min	V
$V_{EB} = -1$ V	$V_{(BR)CBV}$	45 min	V
Collector-to-Emitter Breakdown Voltage ($I_E = -0.5$ mA, $I_B = 0$)	$V_{(BR)CEO}$	45 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -0.001$ mA, $I_C = 0$)	$V_{(BR)EBO}$	3 min	V
Collector-Cutoff Current ($V_{CE} = 1$ V, $I_E = 0$)	I_{CBO}	0.02 max	μ A
Emitter-Cutoff Current ($V_{CE} = 3$ V, $I_C = 0$)	I_{EBO}	1 max	μ A
Static Forward-Current Transfer Ratio ($V_{CE} = 6$ V, $I_E = -1$ mA)	h_{FE}	40 to 170	
Gain-Bandwidth Product ($V_{CE} = 7.5$ V, $I_E = -1.5$ mA, $f = 100$ MHz)	f_T	800	MHz
Feedback Capacitance ($V_{CE} = 7.5$ V, $I_E = -1.5$ mA, $f = 100$ MHz)	C_{cb}	0.2	pF
Input Resistance ($V_{CE} = 7.5$ V, $I_E = -1.5$ mA, $f = 100$ MHz)	R_{ie}	550	Ω
Output Resistance ($V_{CE} = 7.5$ V, $I_E = 1.5$ mA, $f = 100$ MHz)	R_{oe}	24	k Ω
Input Capacitance ($V_{CE} = 7.5$ V, $I_E = -1.5$ mA, $f = 100$ MHz)	C_{ie}	8.5	pF
Output Capacitance ($V_{CE} = 7.5$ V, $I_E = -1.5$ mA, $f = 100$ MHz)	C_{oe}	1.4	pF
Magnitude of Forward Transadmittance* ($V_{CE} = 7.5$ V, $I_E = -1.5$ mA, $f = 100$ MHz)	$ Y_{fe} $	38	mmhos
Noise Figure* ($V_{CE} = 7.5$ V, $I_E = -1.5$ mA, $f = 100$ MHz)	NF	2.5	dB
Maximum Available Amplifier Gain* ($V_{CE} = 7.5$ V, $I_E = -1.5$ mA, $f = 100$ MHz)	MAG	37	dB
Maximum Usable Gain*:			
Unneutralized— $V_{CE} = 7.5$ V, $I_E = -1.5$ mA, $f = 100$ MHz	MUG	20	dB
Neutralized— $V_{CE} = 7.5$ V, $I_E = -1.5$ mA, $f = 100$ MHz	MUG	25	dB

$V_{(BR)CBO}$	45 min	V
$V_{(BR)CBV}$	45 min	V
$V_{(BR)CEO}$	45 min	V
$V_{(BR)EBO}$	3 min	V
I_{CBO}	0.02 max	μ A
I_{EBO}	1 max	μ A
h_{FE}	40 to 170	
f_T	800	MHz
C_{cb}	0.2	pF
R_{ie}	550	Ω
R_{oe}	24	k Ω
C_{ie}	8.5	pF
C_{oe}	1.4	pF
$ Y_{fe} $	38	mmhos
NF	2.5	dB
MAG	37	dB
MUG	20	dB
MUG	25	dB

* This characteristic applies only to type 40478.





TRANSISTOR

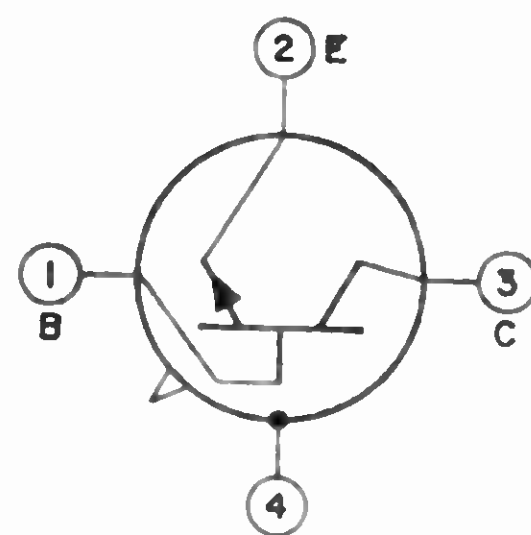
40479

Si n-p-n type used in mixer applications in conjunction with types 40478 (rf amplifier), 40480 (rf oscillator), and 40481 and 40482 (if amplifiers) to make up a "front-end" and if complement for FM and AM/FM receivers. The terminal arrangement permits shielding between input and output terminals for superior high-

frequency performance and greater circuit stability, particularly on printed-circuit boards. JEDEC TO-104, Outline No.31. This type is identical with type 40478 except for the following item:

CHARACTERISTICS

Maximum Available Conversion Gain ($V_{CE} = 7.5$ V, $I_E = -1.5$ mA, $f = 100$ MHz)	MAG _c	35	dB
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TRANSISTOR

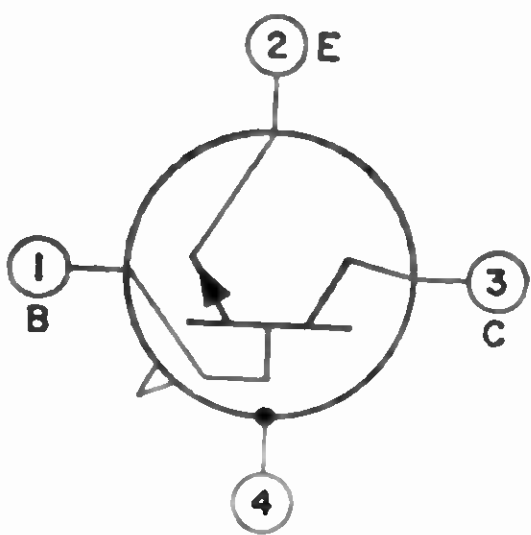
40480

Si n-p-n type used in rf-oscillator applications in conjunction with types 40478 (rf amplifier), 40479 (mixer), and 40481 and 40482 (if amplifiers) to make up a "front-end" and if complement for FM and AM/FM receivers. The terminal arrangement permits shielding between input and output terminals for superior high-

frequency performance and greater circuit stability, particularly on printed-circuit boards. JEDEC TO-104, Outline No.31. For maximum ratings, refer to type 40478.

CHARACTERISTICS

Collector-to-Base Breakdown Voltage: $I_C = 0.001$ mA, $I_E = 0$	$V_{(BR)CBO}$	45 min	V
$V_{EB} = -1$ V	$V_{(BR)CBV}$	45 min	V
Collector-to-Emitter Breakdown Voltage ($I_E = -0.5$ mA, $I_C = 0$)	$V_{(BR)CEO}$	45 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -0.001$ mA, $I_C = 0$)	$V_{(BR)EBO}$	3 min	V
Collector-Cutoff Current ($V_{CE} = 1$ V, $I_E = 0$)	I_{CBO}	0.02 max	μ A
Emitter-Cutoff Current ($V_{CE} = 3$ V, $I_C = 0$)	I_{EBO}	1 max	μ A
Static Forward-Current Transfer Ratio ($V_{CE} = 6$ V, $I_E = -1$ mA)	h_{FE}	27 to 275	



TRANSISTOR

40481

Si n-p-n type used in if-amplifier applications in conjunction with types 40478 (rf amplifier), 40479 mixer, 40480 (rf oscillator), and 40482 (if amplifier) to make up a "front-end" and if complement for FM and AM/FM receivers. The terminal arrangement permits shielding between input and output terminals for superior

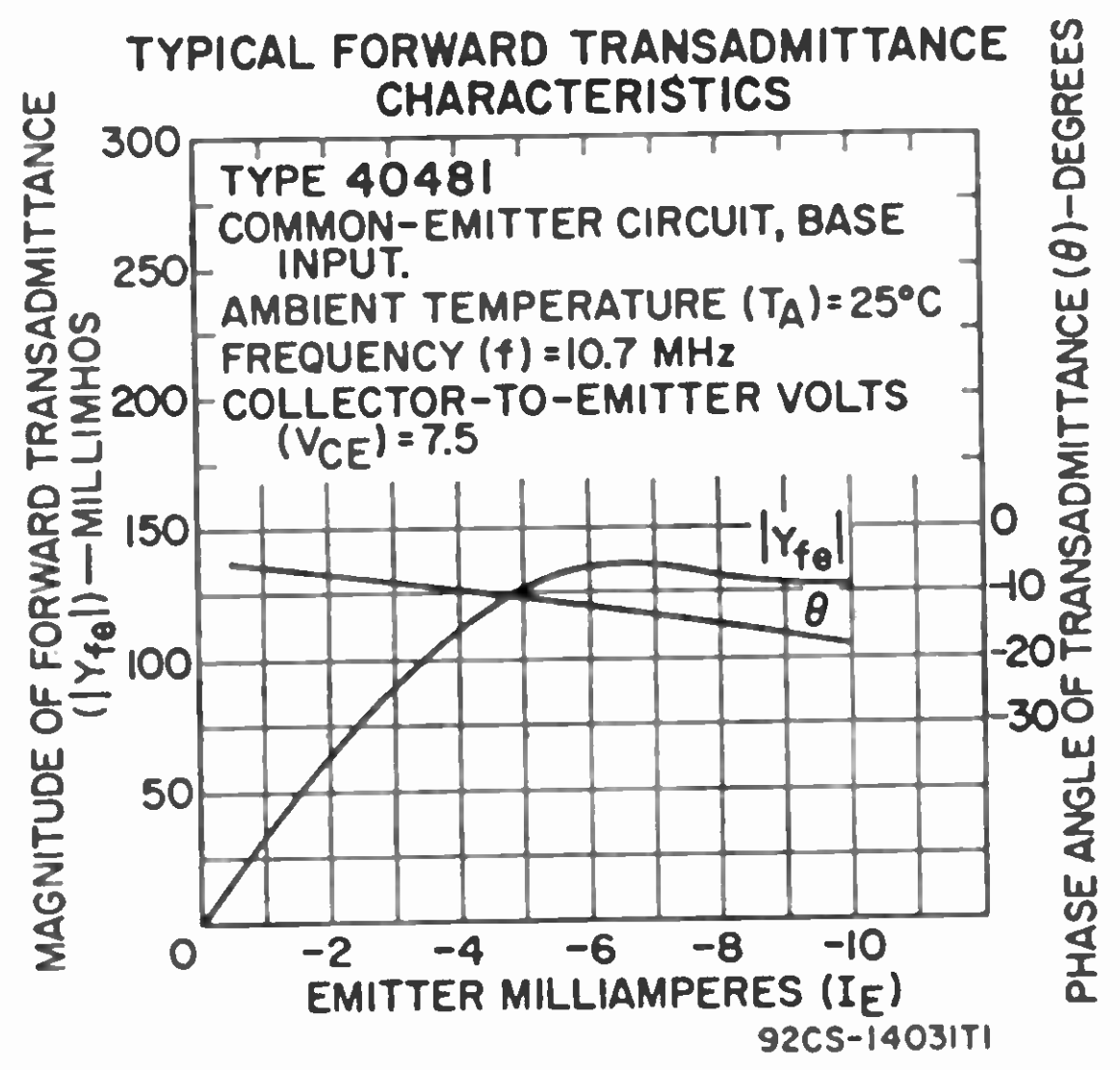
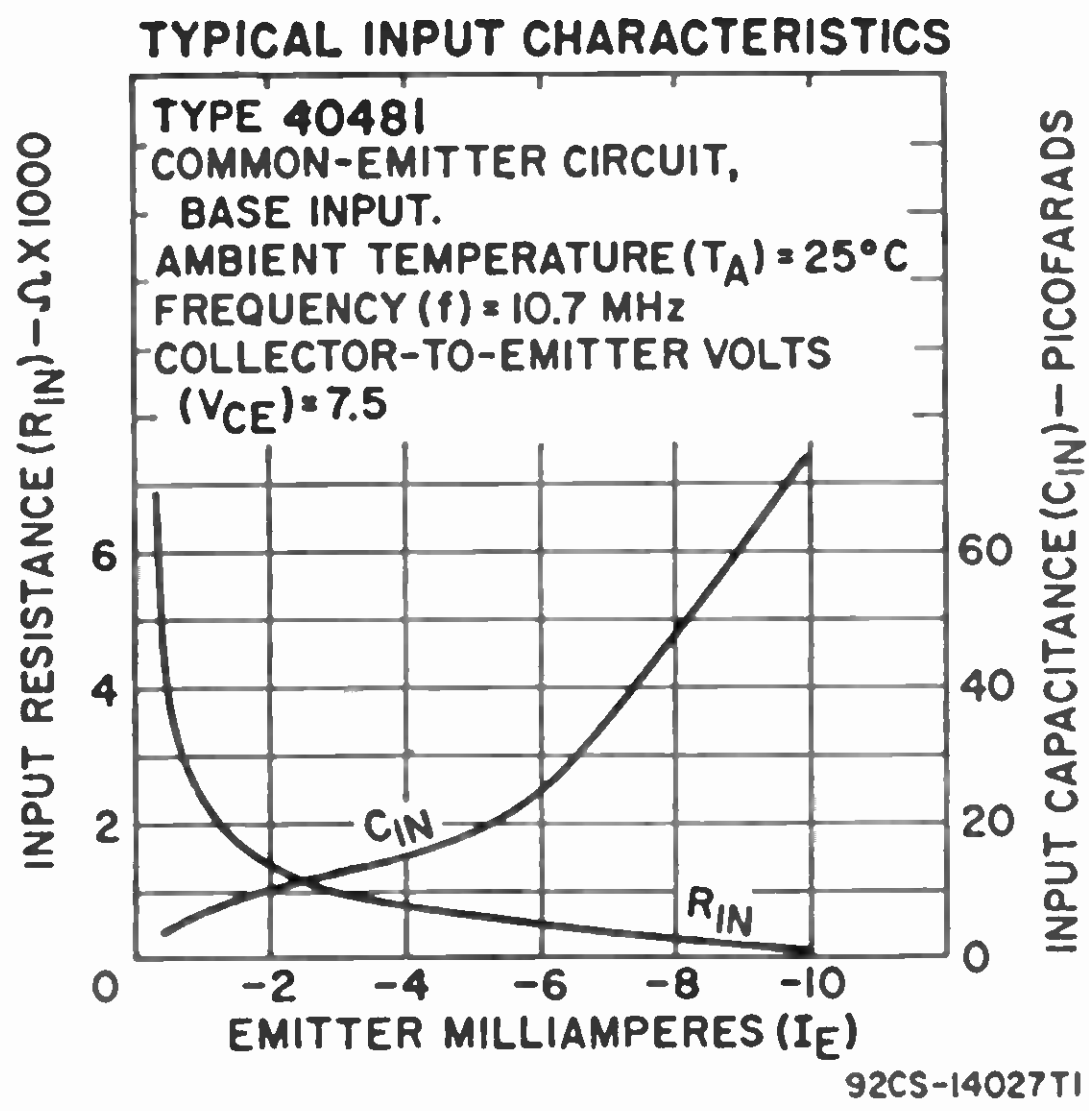
high-frequency performance, and greater circuit stability, particularly on printed-circuit boards. JEDEC TO-104, Outline No.31. For maximum ratings, refer to type 40478.

CHARACTERISTICS

Collector-to-Base Breakdown Voltage: $I_C = 0.001$ mA, $I_E = 0$	$V_{(BR)CBO}$	45 min	V
$V_{EB} = -1$ V	$V_{(BR)CBV}$	45 min	V
Collector-to-Emitter Breakdown Voltage ($I_E = -0.5$ mA, $I_B = 0$)	$V_{(BR)CEO}$	45 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.001$ mA, $I_C = 0$)	$V_{(BR)EBO}$	3 min	V
Collector-Cutoff Current ($V_{CE} = -1$ V, $I_E = 0$)	I_{CBO}	0.02 max	μ A
Emitter-Cutoff Current ($V_{CE} = 3$ V, $I_C = 0$)	I_{EBO}	1 max	μ A

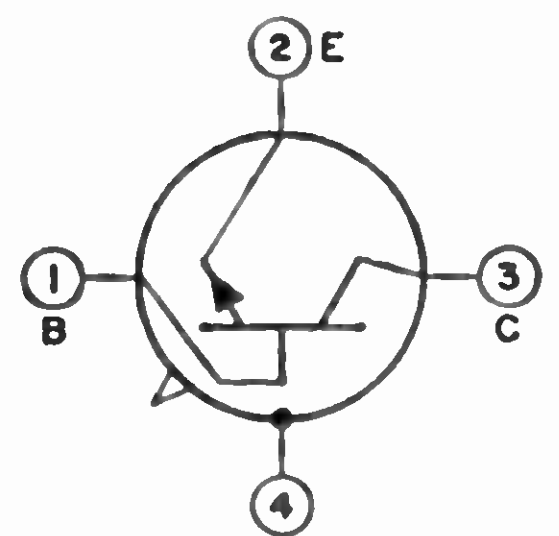
CHARACTERISTICS (cont'd)

Static Forward-Current Transfer Ratio ($V_{CE} = 6\text{ V}$, $I_E = -1\text{ mA}$)	h_{FE}	70 to 275	
Gain-Bandwidth Product ($V_{CE} = 7.5\text{ V}$, $I_E = -2\text{ mA}$, $f = 10.7\text{ MHz}$)	f_T	860	MHz
Feedback Capacitance ($V_{CE} = 7.5\text{ V}$, $I_E = -2\text{ mA}$, $f = 10.7\text{ MHz}$)	C_{cb}	0.2	pF
Input Resistance ($V_{CE} = 7.5\text{ V}$, $I_E = -2\text{ mA}$, $f = 10.7\text{ MHz}$)	R_{i_e}	1500	Ω
Output Resistance ($V_{CE} = 7.5\text{ V}$, $I_E = -2\text{ mA}$, $f = 10.7\text{ MHz}$)	R_{o_e}	85	k Ω
Input Capacitance ($V_{CE} = 7.5\text{ V}$, $I_E = -2\text{ mA}$, $f = 10.7\text{ MHz}$)	C_{i_e}	11	pF
Output Capacitance ($V_{CE} = 7.5\text{ V}$, $I_E = -2\text{ mA}$, $f = 10.7\text{ MHz}$)	C_{o_e}	1.35	pF
Magnitude of Forward Transadmittance ($V_{CE} = 7.5\text{ V}$, $I_E = -2\text{ mA}$, $f = 10.7\text{ MHz}$)	$ Y_{fe} $	64	mmhos
Maximum Available Amplifier Gain ($V_{CE} = 7.5\text{ V}$, $I_E = -2\text{ mA}$, $f = 10.7\text{ MHz}$)	MAG	51	dB
Maximum Usable Gain Per Stage, Unneutralized ($V_{CE} = 7.5\text{ V}$, $I_E = -2\text{ mA}$, $f = 10.7\text{ MHz}$):			
For 1 stage	MUG	32	dB
For 2 stages	MUG	28	dB
For 3 stages	MUG	27.5	dB
For 4 stages	MUG	26	dB
Maximum Usable Gain Per Stage, Neutralized ($V_{CE} = 7.5\text{ V}$, $I_E = -2\text{ mA}$, $f = 10.7\text{ MHz}$):			
For 1 stage	MUG	37	dB
For 2 stages	MUG	35	dB
For 3 stages	MUG	33	dB
For 4 stages	MUG	32	dB



40482 TRANSISTOR

Si n-p-n type used in if-amplifier applications in conjunction with types 40478 (rf amplifier), 40479 (mixer), 40480 (rf oscillator), and 40481 (if amplifier) to make up a "front-end" and if complement for FM and AM/FM receivers. The terminal arrangement permits shielding between input and output terminals for superior high-frequency performance and greater circuit stability, particularly on printed-circuit boards. JEDEC TO-104, Outline No.31. This type is identical to type 40481 except for the following items:

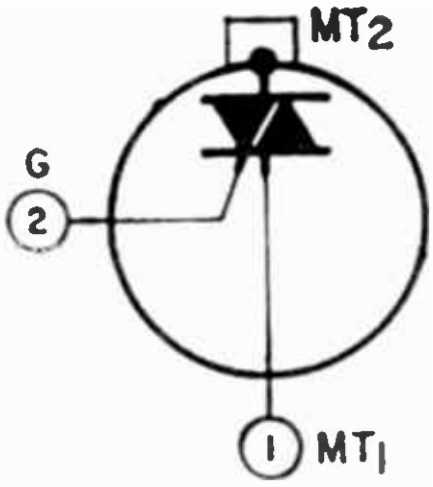


CHARACTERISTICS

Static Forward-Current Transfer Ratio ($V_{CE} = 6\text{ V}$, $I_E = -1\text{ mA}$)	h_{FE}	27 to 90	
Input Resistance ($V_{CE} = 7.5\text{ V}$, $I_E = -2\text{ mA}$, $f = 10.7\text{ MHz}$)	R_{i_e}	1300	Ω
Output Resistance ($V_{CE} = 7.5\text{ V}$, $I_E = -2\text{ mA}$, $f = 10.7\text{ MHz}$)	R_{o_e}	100	k Ω

40485
40486

TRIACS



Si gate-controlled full-wave types used for the control of ac loads in applications such as heating controls, motor controls, light dimmers, and power switching systems. Outline No.7.

MAXIMUM RATINGS (For sinusoidal ac supply voltage at 50/60 Hz with resistive or inductive load)

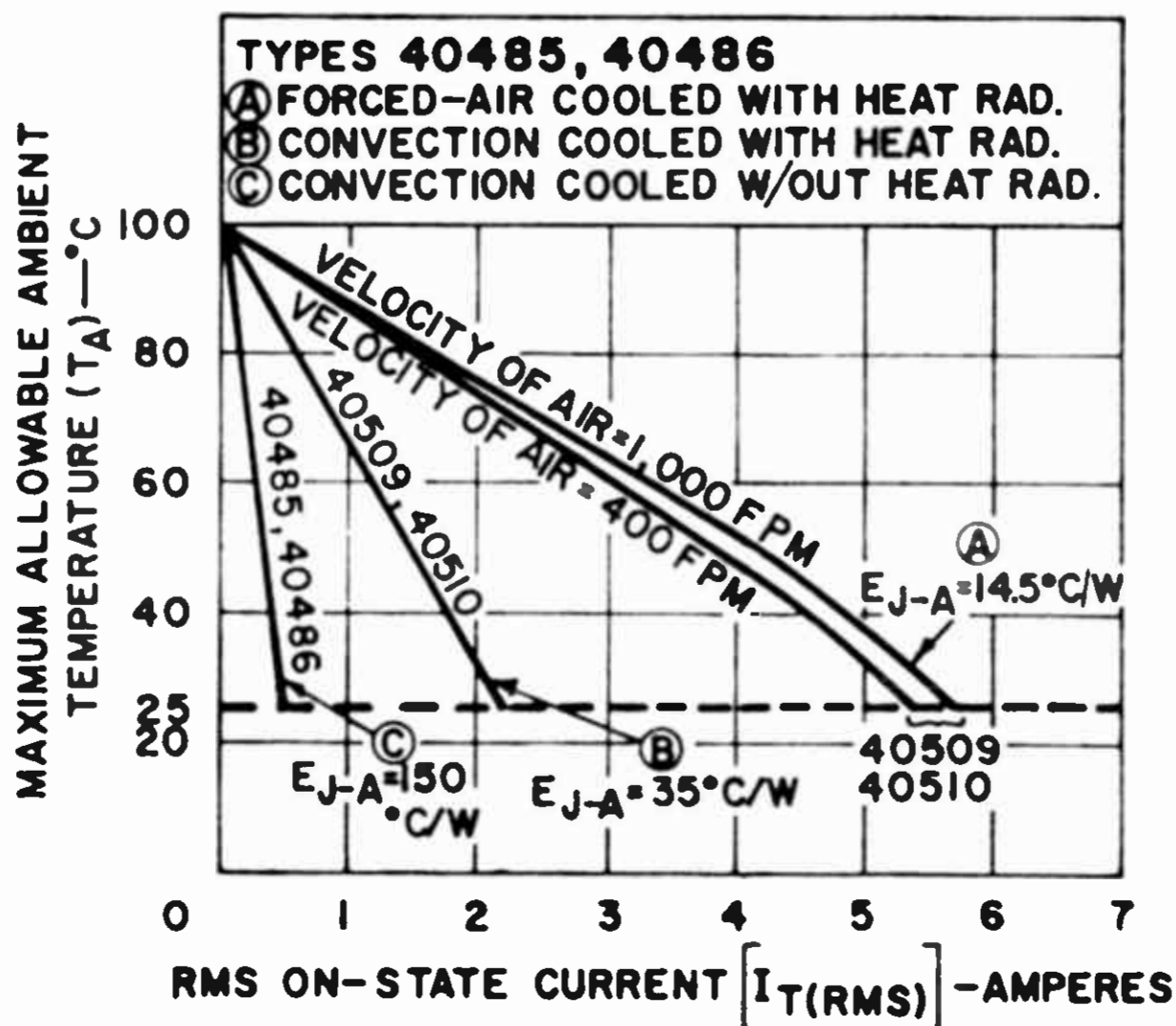
	40485	40486	
V_{DROM}^* ($T_J = -65^\circ\text{C}$ to 100°C)	200	400	V
$I_{T(RMS)}^\Delta$ ($T_C = 75^\circ\text{C}$, conduction angle = 360°)	6		A
$I_{T(RMS)}^\bullet$ (T_A up to 100°C , conduction angle = 360°)	See Rating Chart (Ambient Temperature)		
I_{TSM} (1 cycle of principal voltage)	100		A
I_{GTM} (1 μs max)	4		A
P_{GM} (1 μs max, $I_{GTM} \leq 4$ A peak)	16		W
$P_{G(\Delta V)}$	0.2		W
T_{STG}^\blacksquare	-65 to 150		$^\circ\text{C}$
$T_C(\text{opf})^\blacksquare$	-65 to 100		$^\circ\text{C}$
$T_C(\text{soldering})^\blacksquare$	225		$^\circ\text{C}$

CHARACTERISTICS (At maximum electrical ratings at $T_C = 25^\circ\text{C}$)

I_{DROM} ($T_J = 100^\circ\text{C}$, $V_{DROM} = \text{max rated value}$)	0.1 typ; 4 max	0.2 typ; 4 max	mA
V_{TM} ($i_T = 30$ A peak)	1.6 typ; 2.25 max		V
I_{HO} (initial principal current = 150 mAdc)	15 typ; 30 max		A
Commutating dv/dt ($V_D = V_{DROM}$, $I_{T(RMS)} = 6$ A, commutating $di/dt = 3.2$ A/ms, gate unenergized at $T_C = 75^\circ\text{C}$)	3 min; 10 typ		V/ μs
Critical dv/dt ($V_D = V_{DROM}$, exponential voltage rise, $T_C = 100^\circ\text{C}$)	30 min; 150 typ	20 min; 100 typ	V/ μs
$I_{GT}^*\ddagger$ ($V_D = 12$ Vdc, $R_L = 12 \Omega$):			
I+ mode, V_{MT2} positive, V_G positive	15 typ; 25 max		mA
I- mode, V_{MT2} positive, V_G negative	25 typ; 40 max		mA
III+ mode, V_{MT2} negative, V_G positive	25 typ; 40 max		mA
III- mode, V_{MT2} negative, V_G negative	15 typ; 25 max		mA
$V_{GT}^*\ddagger$ ($V_D = 12$ Vdc, $R_L = 12 \Omega$)	1 typ; 2.2 max		V
$V_{GT}^*\ddagger$ ($V_D = V_{DROM}$, $R_L = 125 \Omega$, $T_C = 100^\circ\text{C}$)	0.2 min		V
t_{gt} ($V_D = V_{DROM}$, $I_{GT} = 80$ mA, $t_r = 0.1 \mu\text{s}$, $i_T = 10$ A)	2.2		μs
$\theta_{J-C}^\blacktriangle$ (steady-state)	4 max		$^\circ\text{C}/\text{W}$

- * For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
- ‡ For either polarity of gate voltage (V_G) with reference to main terminal 1.
- ▲ This characteristic does not apply to types 40509 and 40510.
- This characteristic does not apply to types 40638 and 40639.
- When soldered directly to heat sink, a 60/40 solder should be used. Case heating time should be a minimum . . . sufficient to allow the solder to flow freely.

CONDUCTION RATING CHART (AMBIENT TEMPERATURE)

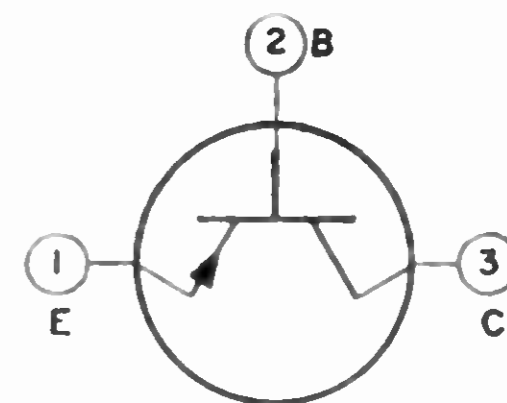


92LS-2052T1

40487

TRANSISTOR

Ge p-n-p drift-field type used in mixer applications in conjunction with types 40488 (oscillator), 40489 (if amplifier), 40490 (af amplifier), 40491 (power amplifier), and 40495 (line rectifier) to provide a complement for AM broadcast-band radio receivers. JEDEC TO-1, Outline No.1.



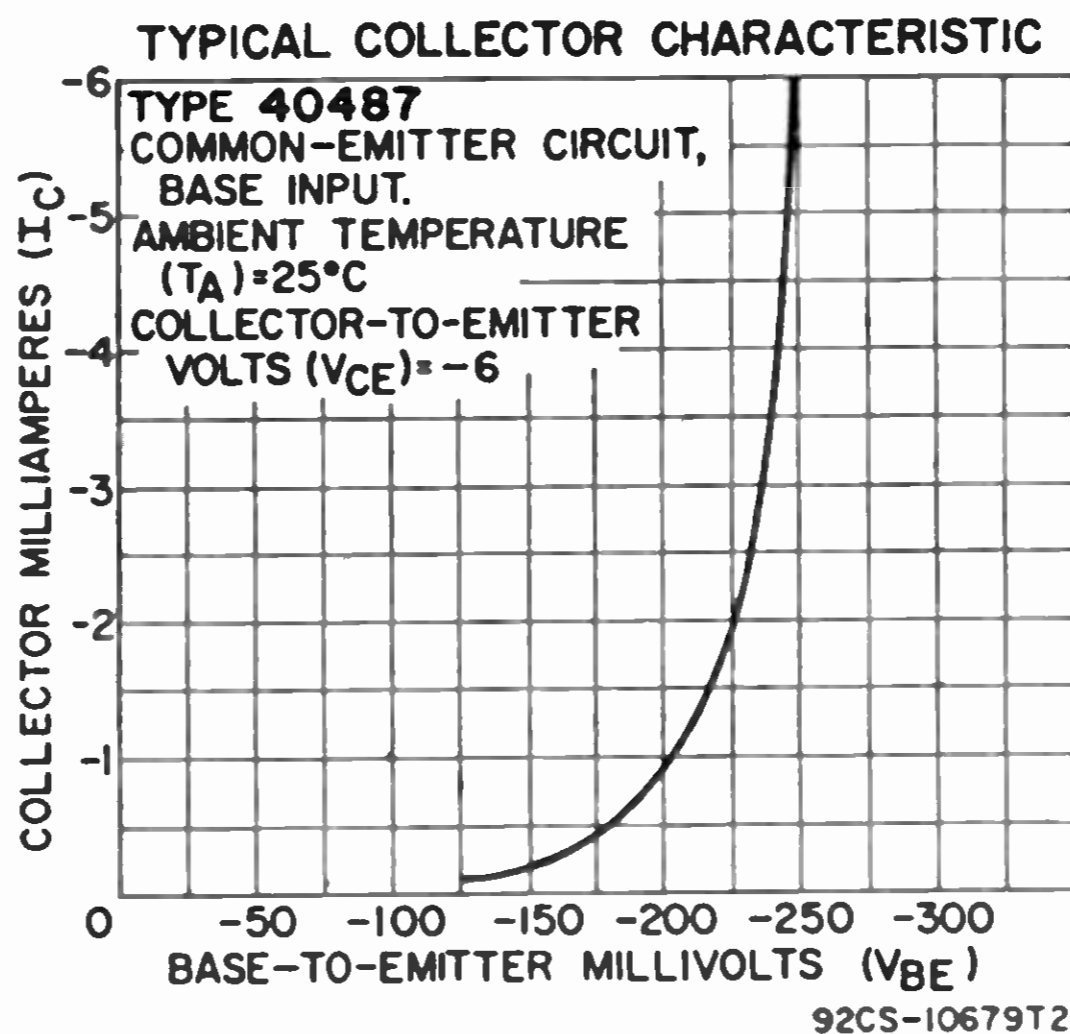
MAXIMUM RATINGS

Collector-to-Base Voltage:				
Emitter open	V_{CB0}	-50	V	
$V_{EB} = -0.5$ V, $I_C = -50$ μ A	V_{CBV}	-34	V	
Emitter-to-Base Voltage	V_{EBO}	-1.5	V	
Collector Current	I_C	-10	mA	
Emitter Current	I_E	10	mA	
Transistor Dissipation:				
T_A up to 25°C	P_T	80	mW	
T_A above 25°C	P_T	See curve page 300		
Temperature Range:				
Operating	T_A	-65 to 85	°C	
Storage	T_{STG}	-65 to 85	°C	
Lead-Soldering Temperature (10 s max)	T_L	255	°C	

CHARACTERISTICS

Collector-to-Base Breakdown Voltage:				
$I_C = -0.05$ mA, $I_E = 0$	$V_{(BR)CBO}$	-50 min	V	
$V_{EB} = -0.5$ V, $I_C = 0.05$ mA	$V_{(BR)CBV}$	-34 min	V	
Emitter-to-Base Breakdown Voltage ($I_E = 0.016$ mA, $I_C = 0$)		$V_{(BR)EBO}$	-1.5 min	V
Collector-Cutoff Current ($V_{CB} = -12$ V, $I_E = 0$)	I_{CBO}	-12 max	μ A	
Emitter-Cutoff Current ($V_{EB} = -1.5$ V, $I_C = 0$)	I_{EBO}	-16 max	μ A	
Small-Signal Forward-Current Transfer Ratio				
($V_{CE} = -6$ V, $I_C = -1$ mA, $f = 1$ kHz)	h_{fe}	40 to 275		
Gain-Bandwidth Product ($V_{CE} = -12$ V, $I_C = -1$ mA)	f_T	40	MHz	
Intrinsic Base-Spreading Resistance ($V_{CE} = -12$ V, $I_C = -1$ mA, $f = 100$ MHz)		$r_{bb'}$	25	Ω
Feedback Capacitance ($V_{CB} = -12$ V, $I_E = 0$)	C_{cb}	3.7 max	pF	
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	390 max	°C/W	

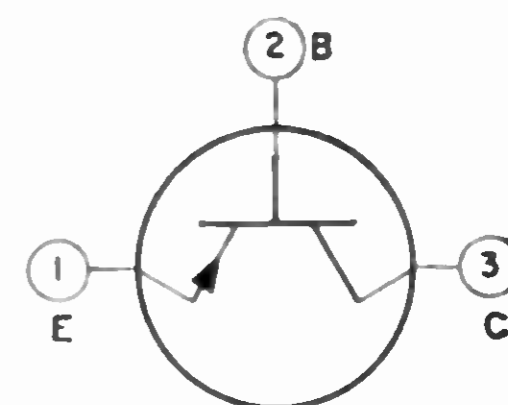
• This value does not apply to type 40488.



40488

TRANSISTOR

Ge p-n-p drift-field type used in oscillator applications in conjunction with types 40487 (mixer), 40489 (if amplifier), 40490 (af amplifier), 40491 (power amplifier), and 40495 (line rectifier) to provide a complement for AM broadcast-band radio receivers. JEDEC TO-1, Outline No.1. This type is identical with type 40487 except for the following items:



MAXIMUM RATINGS

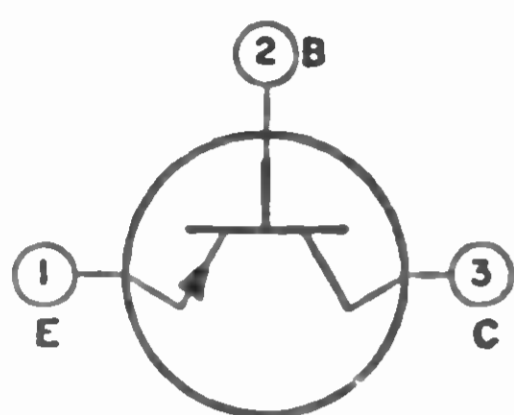
Collector-to-Base Voltage:			
Emitter open	V_{CB0}	-12	V
$V_{EB} = -0.5$ V, $I_C = -50$ μ A	V_{CBV}	-12	V
Emitter-to-Base Voltage	V_{EBO}	-0.5	V

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = -0.05$ mA, $I_C = 0$)	$V_{(BR)CBO}$	-12 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.016$ mA, $I_C = 0$)	$V_{(BR)EBO}$	-0.5 min	V
Emitter-Cutoff Current ($V_{EB} = -0.5$ V, $I_C = 0$)	I_{EBO}	-16 max	μ A
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = -6$ V, $I_C = -1$ mA, $f = 1$ kHz)	h_{fe}	27 to 275	
Gain-Bandwidth Product ($V_{CE} = -12$ V, $I_C = -1$ mA)	f_T	30	MHz

TRANSISTOR

40489



Ge p-n-p drift-field type used in if-amplifier applications in conjunction with types 40487 (mixer), 40488 (oscillator), 40490 (af amplifier), 40491 (power amplifier), and 40495 (line rectifier) to provide a complement for AM broadcast-band radio receivers. JEDEC TO-1, Outline No.1. This type is identical with type 40487

except for the following items:

MAXIMUM RATINGS

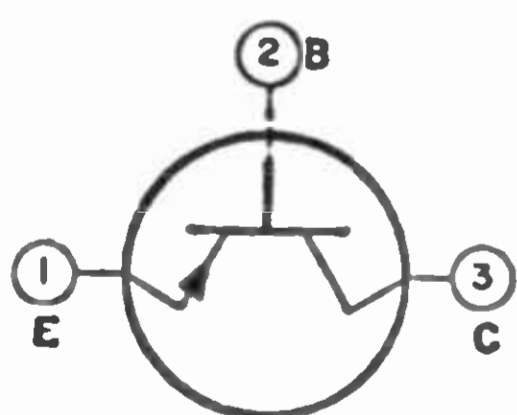
Emitter-to-Base Voltage	V_{EBO}	-0.5	V
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CHARACTERISTICS

Emitter-to-Base Breakdown Voltage ($I_E = 0.016$ mA, $I_C = 0$)	$V_{(BR)EBO}$	-0.5 min	V
Emitter-Cutoff Current ($V_{EB} = -0.5$ V, $I_C = 0$)	I_{EBO}	-16 max	μ A
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = -6$ V, $I_C = -1$ mA, $f = 1$ kHz)	h_{fe}	40 to 350	
Gain-Bandwidth Product ($V_{CE} = -12$ V, $I_C = -1$ mA)	f_T	30	MHz
Feedback Capacitance ($V_{CB} = -12$ V, $I_E = 0$)	C_{cb}	3.4 max	pF

TRANSISTOR

40490



Ge p-n-p alloy-junction type used in af-amplifier and driver stages in conjunction with types 40487 (mixer), 40488 (oscillator), 40489 (if amplifier), 40491 (power amplifier), and 40495 (line rectifier) to provide a complement for AM broadcast-band radio receivers. JEDEC TO-1, Outline No.1.

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CB0}	-20	V
Collector-to-Emitter Voltage ($R_{BE} \leq 10000$ Ω)	V_{CER}	-18	V
Emitter-to-Base Voltage	V_{EBO}	-2.5	V
Collector Current	I_C	-20	mA
Emitter Current	I_E	20	mA
Transistor Dissipation:			
T_A up to 55°C	P_T	0.12	W
T_A above 55°C	P_T	See curve page 300	
Temperature Range:			
Operating	T_A	-65 to 100	°C
Storage	T_{STG}	-65 to 100	°C
Lead-Soldering Temperature (10 s max)	T_L	255	°C

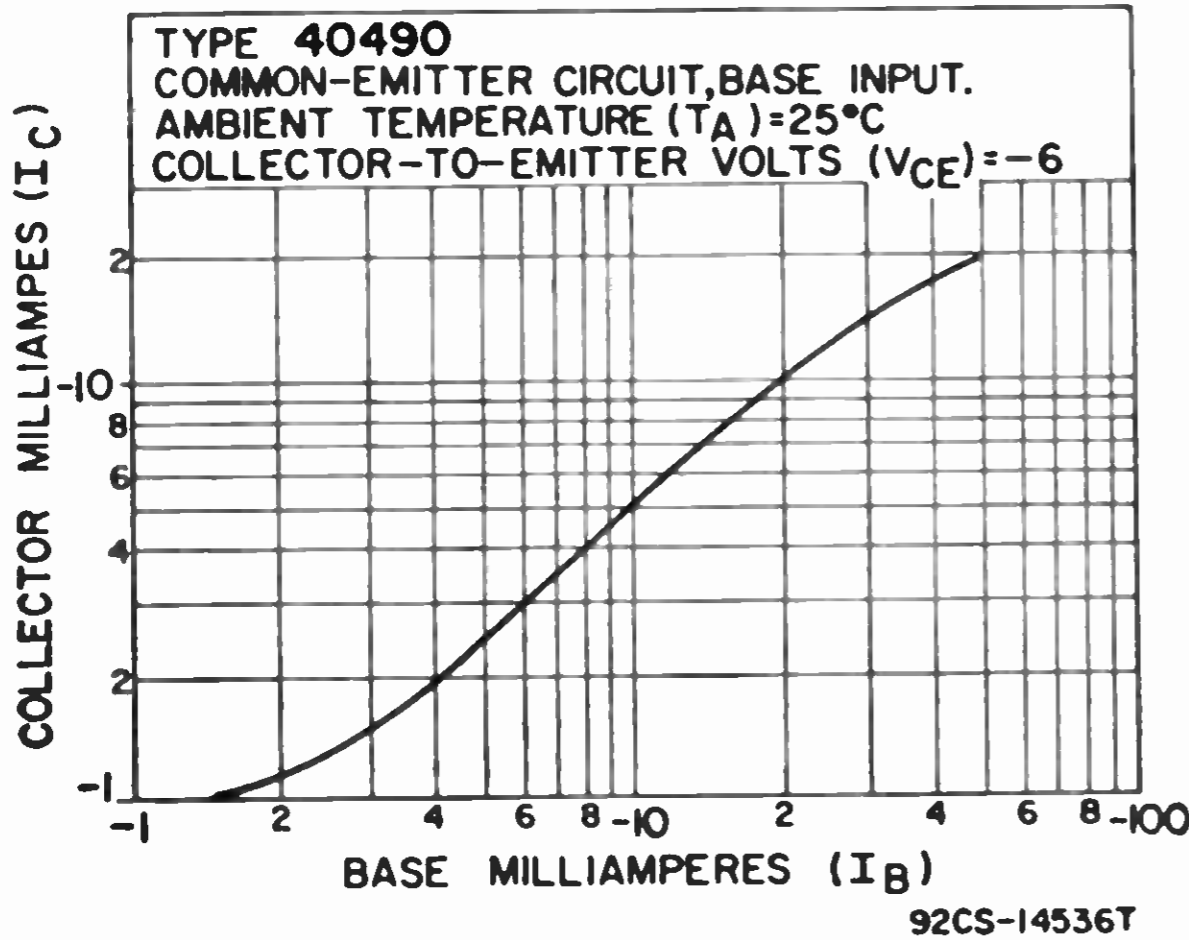
CHARACTERISTICS

Collector-to-Emitter Breakdown Voltage ($R_{BE} = 10$ k Ω , $I_C = -1$ mA)	$V_{(BR)CER}$	-18 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.05$ mA, $I_C = 0$)	$V_{(BR)EBO}$	-2.5 min	V
Collector-Cutoff Current ($V_{CB} = -20$ V, $I_E = 0$)	I_{CB0}	-12 max	μ A
Emitter-Cutoff Current ($V_{EB} = -2.5$ V, $I_C = 0$)	I_{EBO}	-12 max	μ A

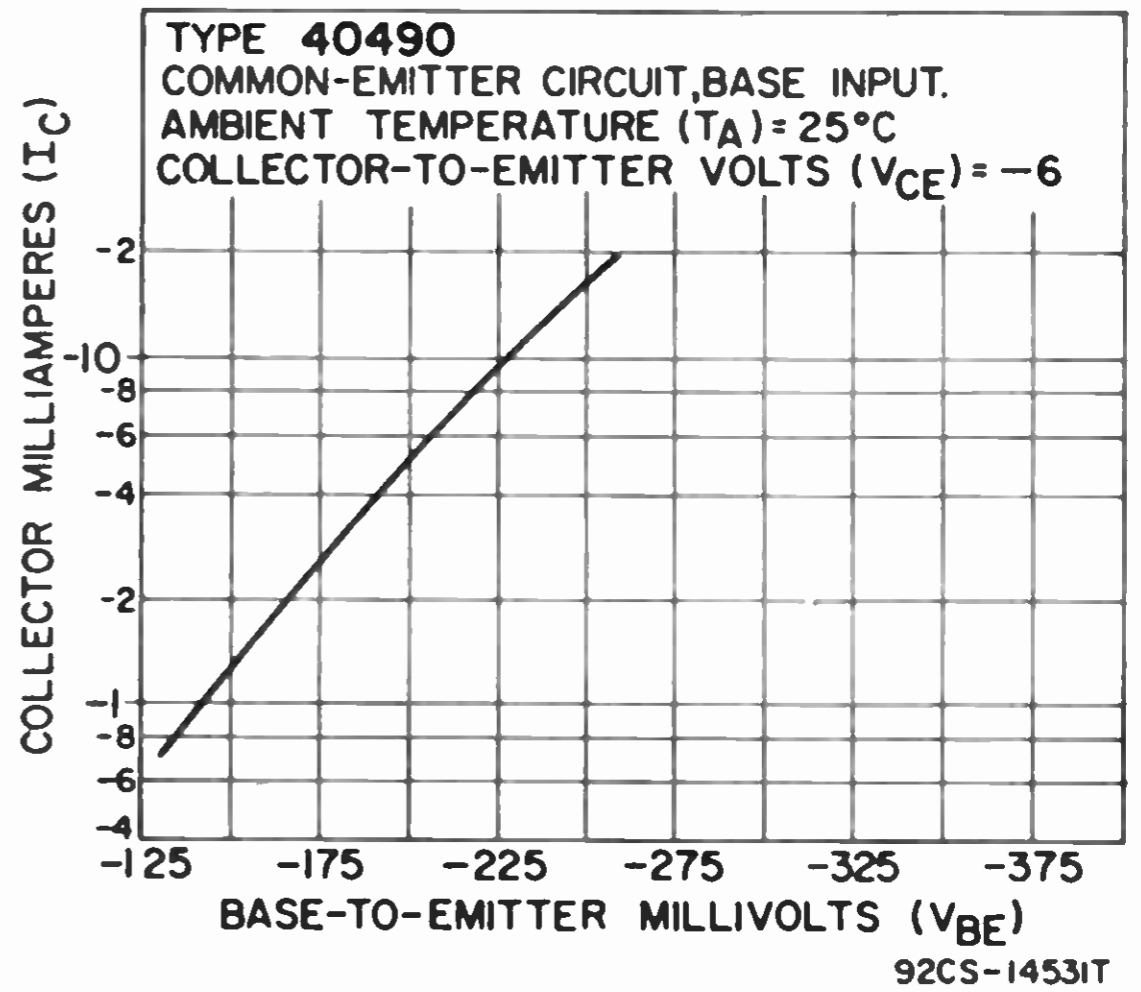
CHARACTERISTICS (cont'd)

Small-Signal Forward-Current Transfer Ratio ($V_{CE} = -6$ V, $I_C = -1$ mA, $f = 1$ kHz)	h_{fe}	170 to 425	
Small-Signal Forward-Current Transfer Ratio Cutoff Frequency ($V_{CE} = -6$ V, $I_C = -1$ mA)	f_{hfb}	10	MHz
Intrinsic Base-Spreading Resistance ($V_{CE} = -6$ V, $I_C = -1$ mA, $f = 100$ MHz)	$r_{bb'}$	200	Ω
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	390 max	$^{\circ}\text{C}/\text{W}$

TYPICAL CURRENT-TRANSFER CHARACTERISTICS

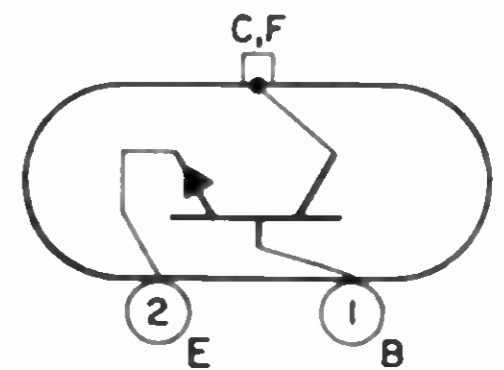


TYPICAL TRANSFER CHARACTERISTIC



40491 POWER TRANSISTOR

Si n-p-n type used in class A af output-amplifier service in conjunction with types 40487 (mixer), 40488 (oscillator) 40489 (if amplifier), 40490 (af amplifier), and 40495 (line rectifier) to provide a complement for AM broadcast-band radio receivers. JEDEC TO-66 (with heat radiator), Outline No.27.

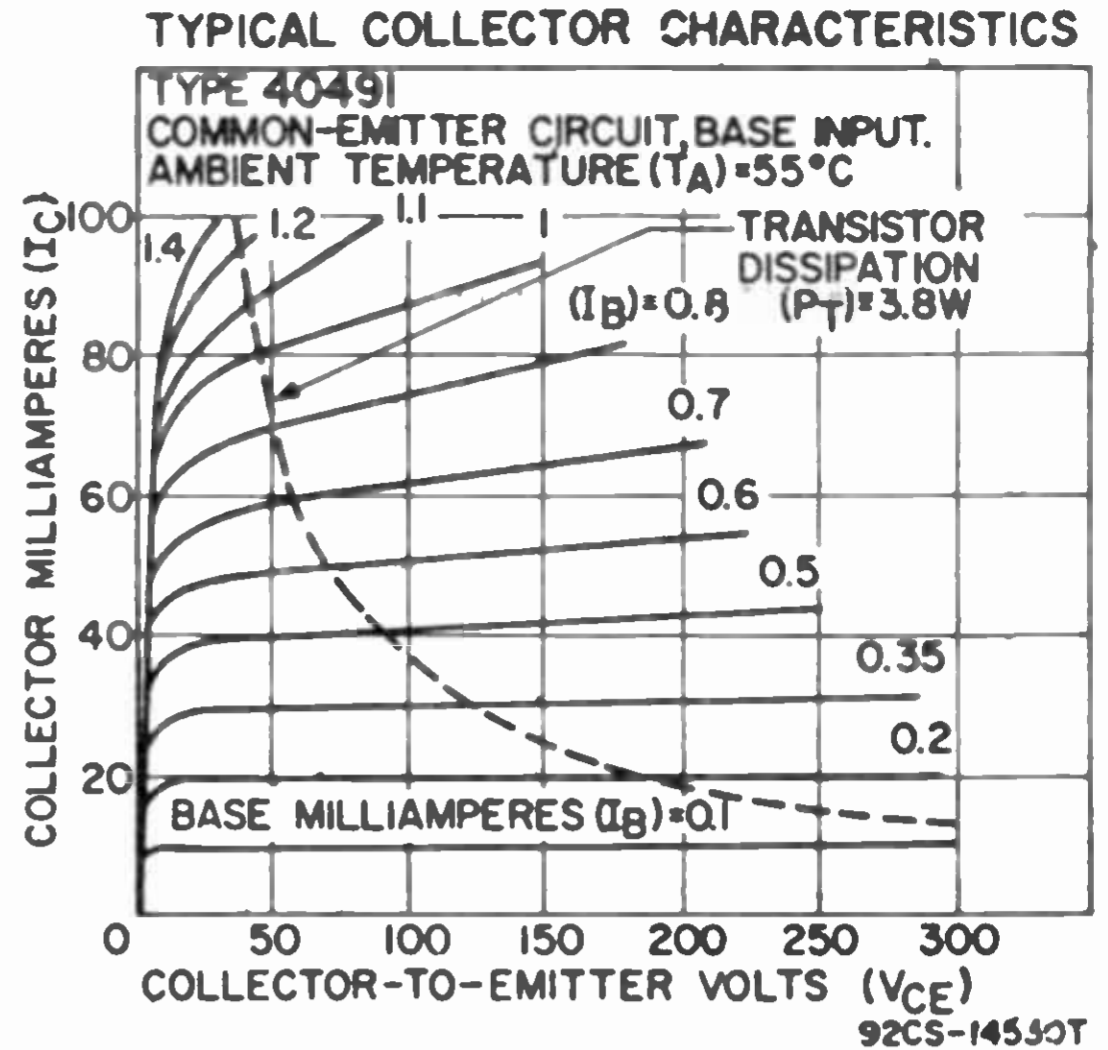
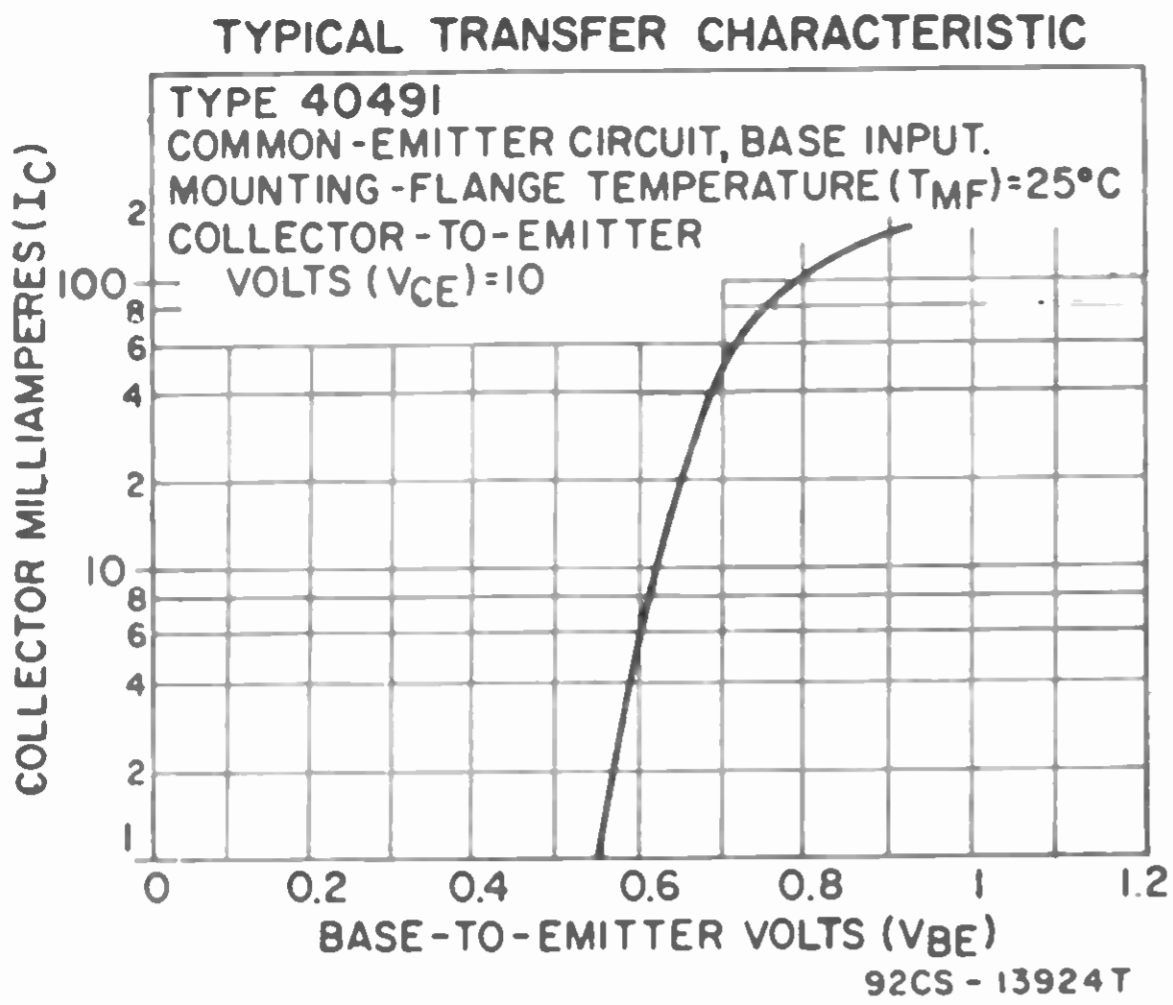


MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	300	V
Collector-to-Emitter Voltage ($I_C = 5$ mA, $I_B = 0$)	V_{CEO}	300	V
Emitter-to-Base Voltage	V_{EBO}	2	V
Collector Current	I_C	150	mA
Emitter Current	I_E	-150	mA
Transistor Dissipation:			
T_A up to 55 $^{\circ}\text{C}$	P_T	3.8	W
T_A above 55 $^{\circ}\text{C}$	P_T	See curve page 300	
Temperature Range:			
Operating	T_A	-65 to 150	$^{\circ}\text{C}$
Storage	T_{STG}	-65 to 150	$^{\circ}\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	255	$^{\circ}\text{C}$

CHARACTERISTICS

Collector-to-Base Breakdown Voltage ($I_C = 0.1$ mA, $I_E = 0$)	$V_{(BR)CBO}$	300 min	V
Collector-to-Emitter Breakdown Voltage ($I_C = 5$ mA, $I_B = 0$)	$V_{(BR)CEO}$	300 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.1$ mA, $I_C = 0$)	$V_{(BR)EBO}$	2 min	V
Collector-Cutoff Current:			
$V_{CE} = 300$ V, $I_E = 0$	I_{CBO}	100 max	μA
$V_{CE} = 300$ V, $I_B = 0$	I_{CEO}	5 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 10$ V, $I_C = 50$ mA)	h_{FE}	30 to 250	
Gain-Bandwidth Product ($V_{CE} = 50$ V, $I_C = 20$ mA) ..	f_T	25	MHz
Intrinsic-Base-Spreading Resistance ($V_{CE} = 50$ V, $I_C = 20$ mA, $f = 100$ MHz)	$r_{bb'}$	20	Ω
Feedback Capacitance ($V_{CB} = 50$ V, $I_E = 0$)	C_{cb}	5	pF
Thermal Resistance, Junction-to-Mounting Flange	θ_{J-FM}	8 typ; 10 max	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	25 max	$^{\circ}\text{C}/\text{W}$



Refer to Chart of Discontinued Transistors

40500

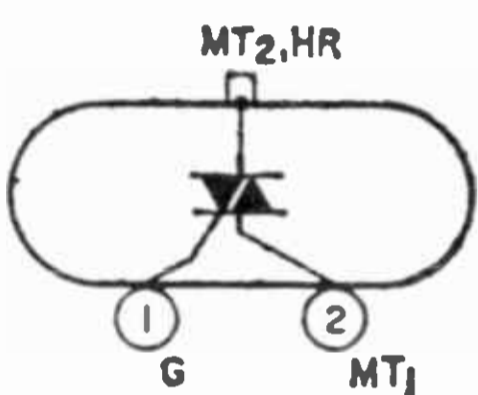
Refer to Chart of Discontinued Transistors

40501

40502

40503

TRIACS



Si gate-controlled full-wave types for the control of ac loads in applications such as heating controls, motor controls, light dimmers, and power switching systems. JEDEC TO-66 (with heat radiator), Outline No.26. Types 40502 and 40503 are identical with types 40429 and 40430, respectively, except for the following items:

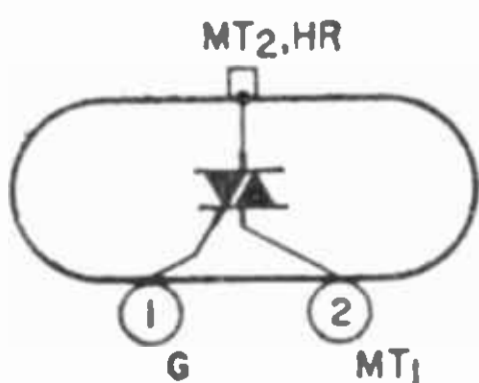
CHARACTERISTICS (At maximum electrical ratings at $T_c = 25^\circ\text{C}$)

	40502	40503	
I_{DROM}^* ($T_J = 100^\circ\text{C}$, $V_{DROM} = \text{max rated value}$)	0.1 typ; 1.2 max	0.2 typ; 1.2 max	mA
Commutating dv/dt^* ($V_D = V_{DROM}$, commutating $di/dt = 3.2 \text{ A/ms}$, $T_c = 75^\circ\text{C}$):			
$I_{T(RMS)}$ and T_A specified by curve A in Rating Chart (Ambient Temperature)	3 min; 10 typ		V/ μs
$I_{T(RMS)}$ and T_A specified by curve B in Rating Chart (Ambient Temperature)	4 min; 12 typ		V/ μs

* For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.

SILICON CONTROLLED RECTIFIERS

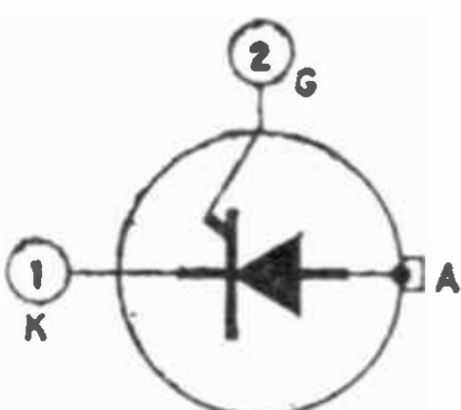
40504-40506



Si all-diffused three-junction types used in power-control and power-switching applications. JEDEC TO-66 (with heat radiator), Outline No.26. Types 40504, 40505, and 40506 are electrically identical with types 2N3228, 2N3525, and 2N4101, respectively.

SILICON CONTROLLED RECTIFIERS

40507-40508

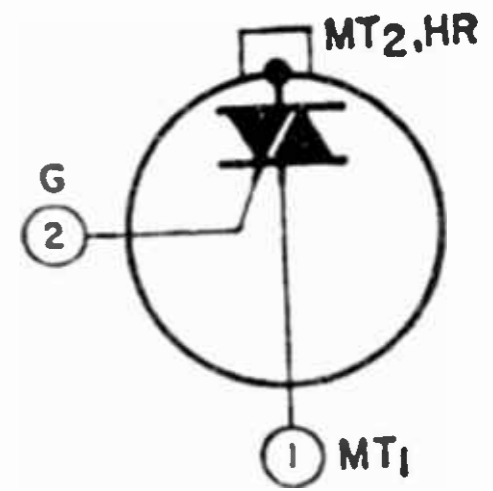


Si all-diffused three-junction types used in power-control and power-switching applications. Outline No.8. Types 40507 and 40508 are electrically identical with types 40378 and 40379, respectively.

**40509
40510**

TRIACS

Si gate-controlled full-wave types used for the control of ac loads in applications such as heating controls, motor controls, light dimmers, and power switching systems. Outline No.8. Types 40509 and 40510 are identical with types 40485 and 40486, respectively, except for the following items:



MAXIMUM RATINGS (For sinusoidal supply voltage at 50/60 Hz with resistive or inductive load)

	40509	40510
$I_{T(RMS)}$ (T_A up to 100°C, conduction angle = 360°)	See Rating Chart (Ambient Temperature)	

CHARACTERISTICS (At maximum electrical ratings at $T_c = 25^\circ C$)

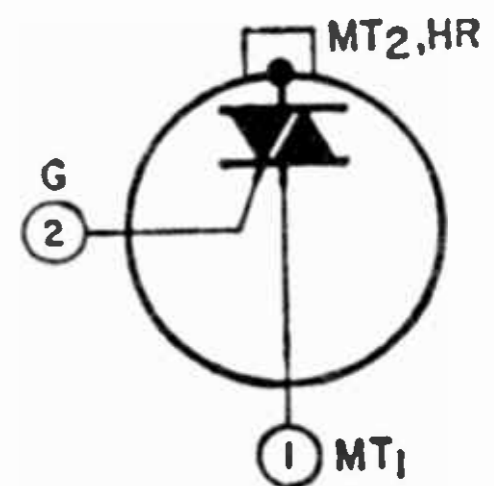
Commutating dv/dt^* ($V_D = V_{DROM}$, commutating $di/dt = 3.2$ A/ms):			
$I_{T(RMS)}$ and T_A specified by curve A in Rating Chart (Ambient Temperature)	_____	3 min; 10 typ _____	_____ V/ μ s
$I_{T(RMS)}$ and T_A specified by curve B in Rating Chart (Ambient Temperature)	_____	4 min; 12 typ _____	_____ V/ μ s
θ_{J-A}	See Rating Chart (Ambient Temperature)		

* For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.

**40511
40512**

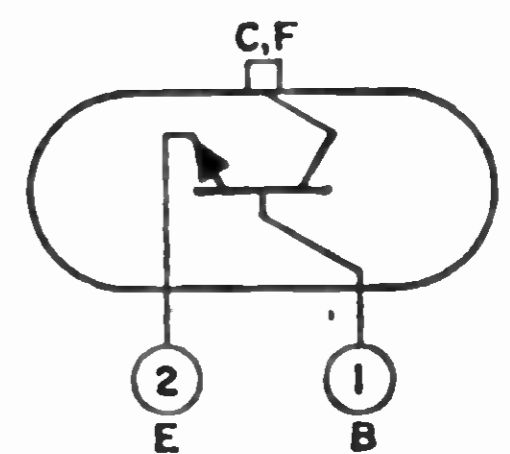
TRIACS

Si gated bidirectional integral-trigger types used for power-control and power-switching applications. Outline No.8. Types 40511 and 40512 are electrically identical with types 40431 and 40432, respectively.



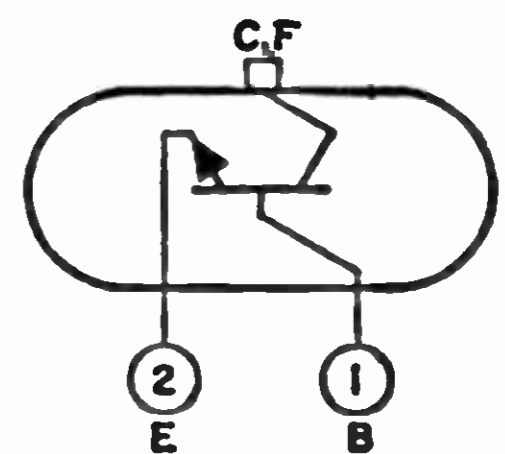
40513 POWER TRANSISTOR

Si n-p-n type featuring a base comprised of a homogeneous-resistivity silicon material and molded silicone plastic package having horizontal leads for mounting on printed-circuit boards. It is used in a wide variety of high-power switching and amplifier applications such as series and shunt regulators, drivers, and output stages for high-fidelity amplifiers. Outline No.51. See Mounting Hardware for desired mounting arrangement. This type is electrically identical with type 40514.



40514 POWER TRANSISTOR

Si n-p-n type featuring a base comprised of a homogeneous-resistivity silicon material and molded silicone plastic package with vertical leads. This type fits a standard TO-3 socket. It is used in a wide variety of high-power switching and amplifier applications such as series and shunt regulators, drivers, and output stages for high-fidelity amplifiers. Outline No.50. See Mounting Hardware for desired mounting arrangement. For collector-characteristics and transfer-characteristics curves, refer to type 2N5034.

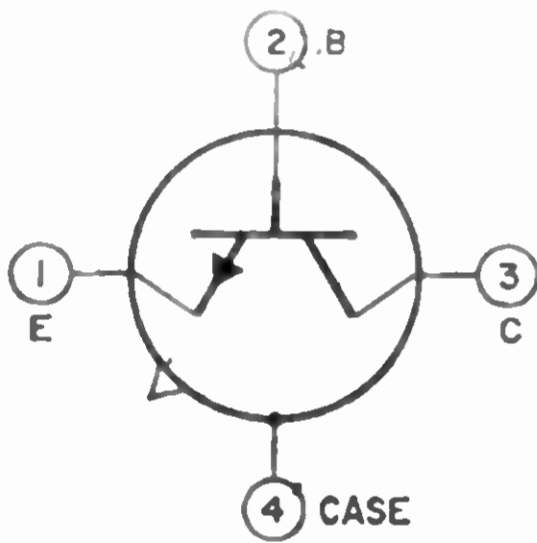


MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage ($R_{BE} = 100 \Omega$)	$V_{CER(SUS)}$	45	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	6	A
Peak Collector Current	i_C	12	A
Base Current	I_B	6	A
Transistor Dissipation:			
T_C up to 25°C	P_T	83	W
T_C above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 150	°C
Storage	T_{STG}	-65 to 150	°C
Lead-Soldering Temperature (10 s max)	T_L	235	°C

CHARACTERISTICS (At case temperature = 25°C)

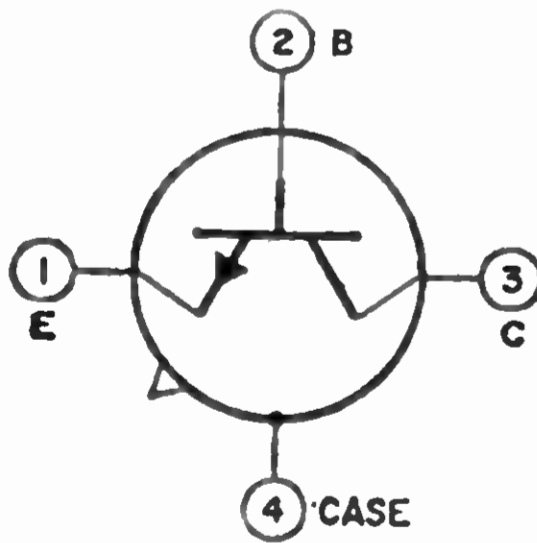
Emitter-to-Base Breakdown Voltage ($I_E = 5 \text{ mA}$)	$V_{(BR)EBO}$	5 min	V
Collector-to-Emitter Sustaining Voltage ($R_{BE} = 100 \Omega$, $I_C = 0.2 \text{ A}$, $t_p = 300 \mu\text{s}$, $df = 1.8\%$)	$V_{CER(SUS)}$	45 min	V
Base-to-Emitter Voltage ($V_{BE} = 4 \text{ V}$, $I_C = 2.5 \text{ A}$, $t_p = 300 \mu\text{s}$, $df = 1.8\%$)	V_{BE}	1.7 max	V
Collector-to-Emitter-to-Saturation Voltage ($I_C = 2.5 \text{ A}$, $t_p = 300 \mu\text{s}$, $df = 1.8\%$, $I_B = 0.25 \text{ A}$)	$V_{CE(sat)}$	1 max	V
Collector-Cutoff Current:			
$V_{CE} = 20 \text{ V}$, $R_{BE} = 100 \Omega$	I_{CER}	2.5 max	mA
$V_{CE} = 20 \text{ V}$, $R_{BE} = 100 \Omega$, $T_C = 150^\circ\text{C}$	I_{CER}	5 max	mA
Emitter-Cutoff Current ($V_{EB} = 5 \text{ V}$, $I_C = 0$)	I_{EBO}	5 max	mA
Pulsed Static Forward-Current Transfer Ratio ($V_{CE} = 4 \text{ V}$, $I_C = 2.5 \text{ A}$, $t_p = 300 \mu\text{s}$, $df = 1.8\%$)	$h_{FE}(\text{pulsed})$	20 to 70	
Gain-Bandwidth Product ($V_{CE} = 4 \text{ V}$, $I_C = 0.5 \text{ A}$)	f_T	0.8 to 2.8	MHz
Thermal Resistance, Junction-to-Case	θ_{J-C}	1.5 max	°C/W



TRANSISTOR

40517

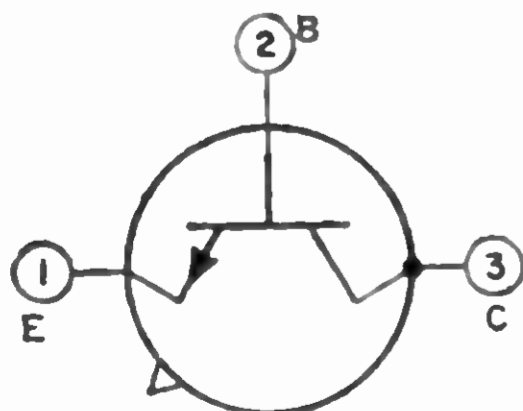
Si n-p-n double-diffused epitaxial planar type used for low-noise amplifier, mixer, and oscillator applications. This type is for use in military applications. It is similar to type 2N3839. JEDEC TO-72, Outline No.28.



UHF TRANSISTOR

40518

Si n-p-n double-diffused epitaxial planar type used for low-noise amplifier, mixer, and oscillator applications. This type is specially preconditioned and tested for high-reliability aerospace and military applications. It is a high-reliability version of type 2N3839. JEDEC TO-72, Outline No.28.



RF TRANSISTOR

40519

Si n-p-n epitaxial planar type used for class C rf-amplifier, driver, and frequency-multiplier service in battery-operated communications equipment. JEDEC TO-52, Outline No.21.

MAXIMUM RATINGS

Collector-to-Emitter Voltage:			
$R_{BE} = 0$	V_{CES}	40	V
Base open	V_{CEO}	16	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	500	mA

MAXIMUM RATINGS (cont'd)

Transistor Dissipation:

T_C up to 25°C	P_T	1	W
T_C above 25°C	P_T	See curve page 300	W
T_A up to 25°C	P_T	0.3	W
T_A above 25°C	P_T	See curve page 300	W
Temperature Range:			
Operating	$T(\text{opr})$	-65 to 200	°C
Storage	T_{STG}	-65 to 175	°C
Lead-Soldering Temperature (10 s max)	T_L	265	°C

CHARACTERISTICS

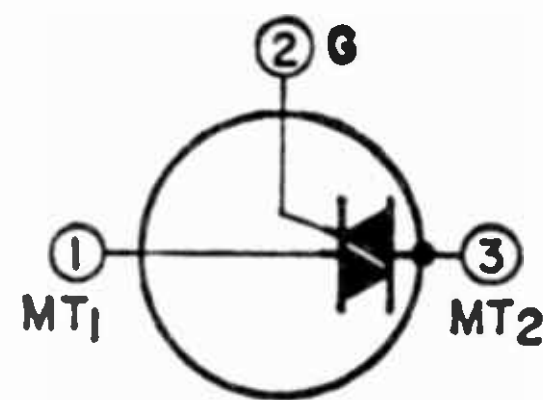
Collector-to-Emitter Breakdown Voltage:

$I_C = 10 \text{ mA}, I_B = 0, t_p = 100 \mu\text{s}, df \leq 0.02$	$V_{(BR)CEO}$	16 min	V
$I_C = 5 \text{ mA}, V_{BE} = 0$	$V_{(BR)CES}$	40 min	V
Emitter-to-Base Breakdown Voltage			
($I_E = -0.01 \text{ mA}, I_C = 0$)	$V_{(BR)EBO}$	5 min	V
Collector-Cutoff Current ($V_{CB} = 20 \text{ V}, V_{BE} = 0,$ $I_E = 0$)			
	I_{CBO}	25 max	nA
Static Forward-Current Transfer Ratio			
($I_C = 50 \text{ mA}, V_{CE} = 1 \text{ V}$)	h_{FE}	20 min	
Magnitude of Small-Signal Forward-Current Transfer			
Ratio ($I_C = 50 \text{ mA}, V_{CE} = 1 \text{ V}, f = 100 \text{ MHz}$)	$ h_{fe} $	3 min	
Output Capacitance ($V_{CB} = 5 \text{ V}, I_E = 0,$ $f = 0.1 \text{ to } 1 \text{ MHz}$)			
	C_{obo}	3.5 max	pF
Power Output, Frequency Doubler			
($P_{io} = 15 \text{ mW}, f(\text{in}) = 86 \text{ MHz}, f(\text{out}) = 172 \text{ MHz}$)	P_{oe}	70 min	mW
Efficiency, Frequency Doubler			
($f(\text{in}) = 86 \text{ MHz}, f(\text{out}) = 172 \text{ MHz}$)	η	20 min	%

40525-
40530

TRIACS

Si gate-controlled full-wave types used for switching from a blocking state to a conducting state for either polarity of applied voltage with positive or negative gate triggering. These types can be controlled with economical transistor circuits for use in low-power phase-control and load-switching applications. JEDEC TO-5 (modified), Outline No.7.

MAXIMUM RATINGS (For sinusoidal ac supply voltage at $f = 50$ and 60 Hz with resistive or inductive load)

	40525	40526	40527	40528	40529	40530	
V_{DROM} (gate open):							
$T_J = -40 \text{ to } 90^\circ\text{C}$	100	200	400	—	—	—	V
$T_J = -40 \text{ to } 100^\circ\text{C}$	—	—	—	100	200	400	V
$I_{T(RMS)}$ (conduction angle = 360°)							
$T_C = 60^\circ\text{C}$	—	2.5	—	—	—	—	A
$T_C = 70^\circ\text{C}$	—	—	—	—	2.5	—	A
$T_A = 25^\circ\text{C}$	—	0.35	—	—	0.4	—	A
I_{TSM} (1 cycle of principal voltage)	—	—	—	25	—	—	A
I_{GTM} (1 μs max)	—	—	—	0.5	—	—	A
P_{GM} (1 μs max)	—	—	—	10	—	—	W
$P_{G(AV)}$:							
$T_A = 25^\circ\text{C}$	—	—	—	0.05	—	—	W
$T_C = 60^\circ\text{C}$	—	—	—	0.15	—	—	W
T_{stg}	—	—	—	-40 to 150	—	—	°C
T_C	—	—	—	-40 to 100	—	—	°C

CHARACTERISTICS (At maximum electrical ratings at $T_C = 25^\circ\text{C}$)

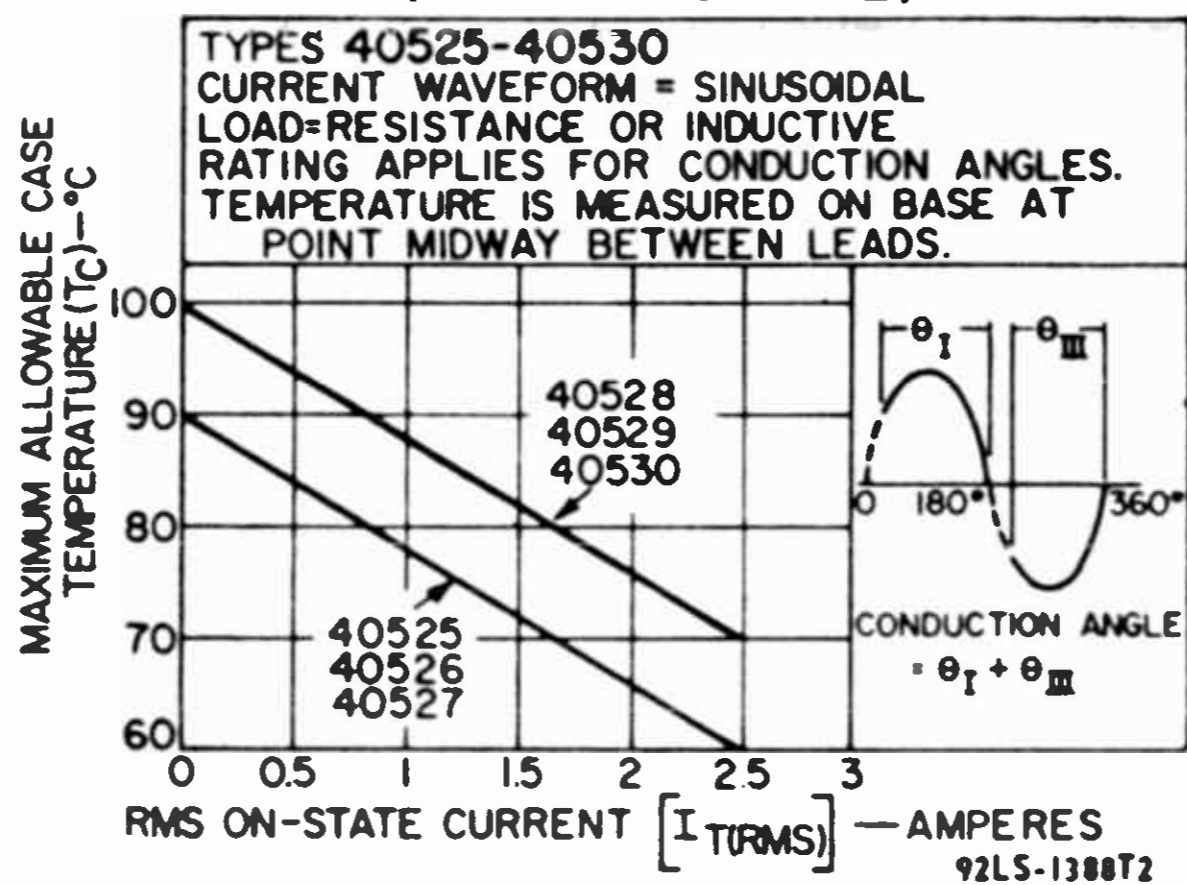
	40525	40526	40527	40528	40529	40530	
I_{DROM} (gate open, $V_{DROM} = \text{max}$ rated value):							
$T_J = 100^\circ\text{C}$	—	—	—	—	—	—	0.2 typ; 0.75 max mA
$T_J = 90^\circ\text{C}$	—	—	—	—	—	—	0.2 typ; 0.75 max mA
V_T ($I_T = 10 \text{ A peak}$)	—	—	—	—	—	—	1.7 typ; 2.2 max V (peak)
I_{HO} (initial principal current = 150 mA dc)	—	—	—	—	—	—	2 typ; 5 max 6.5 typ; 15 max mA (dc)

CHARACTERISTICS (cont'd)

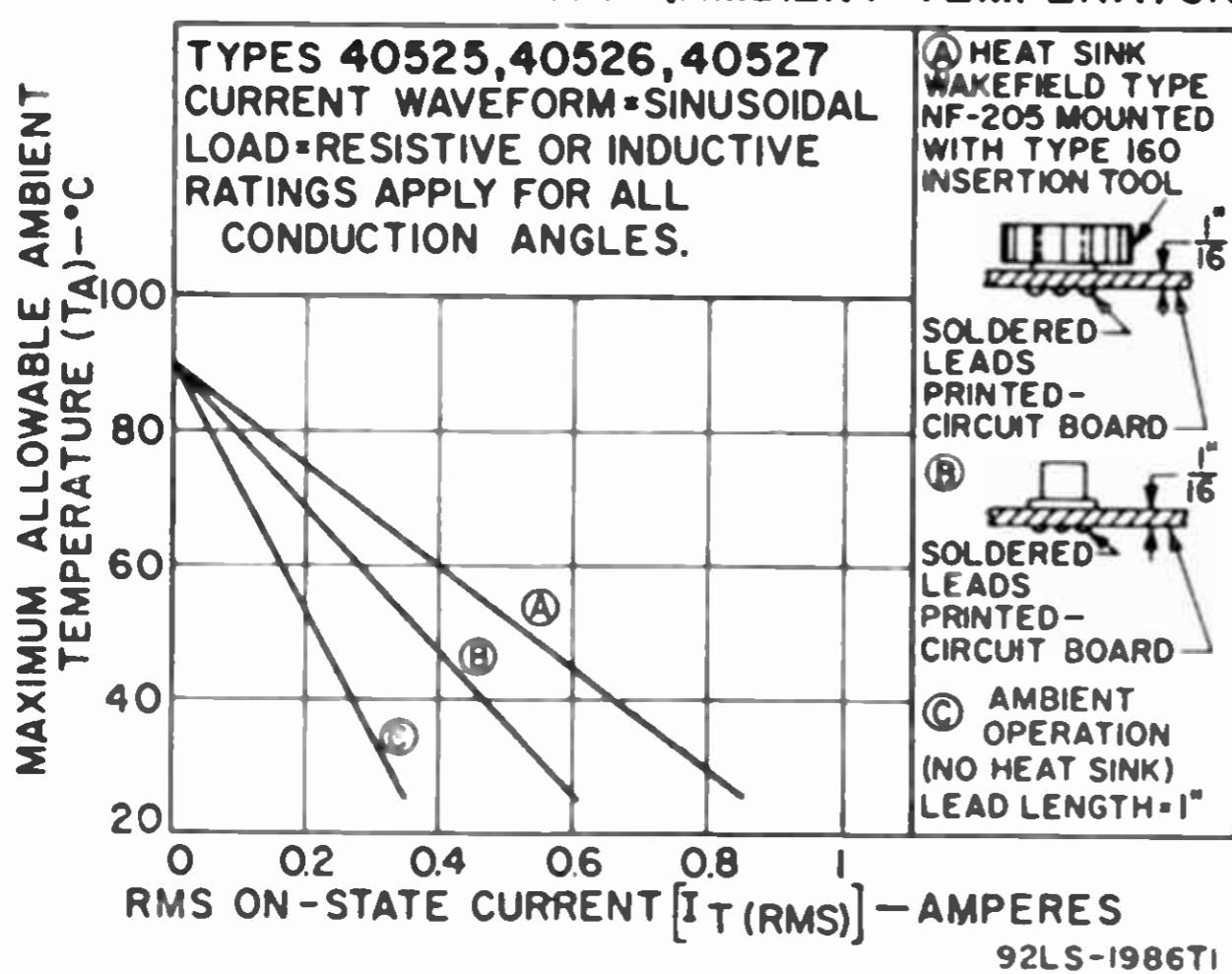
Critical dv/dt [●] (V _D = V _{DROM} , exponential voltage rise, gate open):	40525	40526	40527	40528	40529	40530	
T _C = 100°C	—	—	—	—	10	—	V/μs
T _C = 90°C	—	5	—	—	—	—	V/μs
I _{GT} [■] (V _D = 6 Vdc, R _L = 39 Ω):							
I ⁺ mode, V _{MT2} positive, V _G positive	—	1 typ; 3 max	—	—	3.5 typ; 10 max	—	mA (dc)
I ⁻ mode, V _{MT2} positive, V _G negative	—	2 typ; 3 max	—	—	7 typ; 10 max	—	mA (dc)
III ⁺ mode, V _{MT2} negative, V _G positive	—	2 typ; 3 max	—	—	7 typ; 10 max	—	mA (dc)
III ⁻ mode, V _{MT2} negative, V _G negative	—	1 typ; 3 max	—	—	3.5 typ; 10 max	—	mA (dc)
V _{GT} [■] :							
V _D = 6 Vdc, R _L = 39 Ω	—	—	1 typ; 2.2 max	—	—	—	V
V _D = V _{DROM} , R _L = 125 Ω, T _C = 100°C	—	—	—	—	0.15 min	—	V
V _D = V _{DROM} , R _L = 125 Ω, T _C = 90°C	—	—	0.15 min	—	—	—	V

- For either polarity of main-terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
- For either polarity of gate voltage (V_G) with reference to main terminal 1.

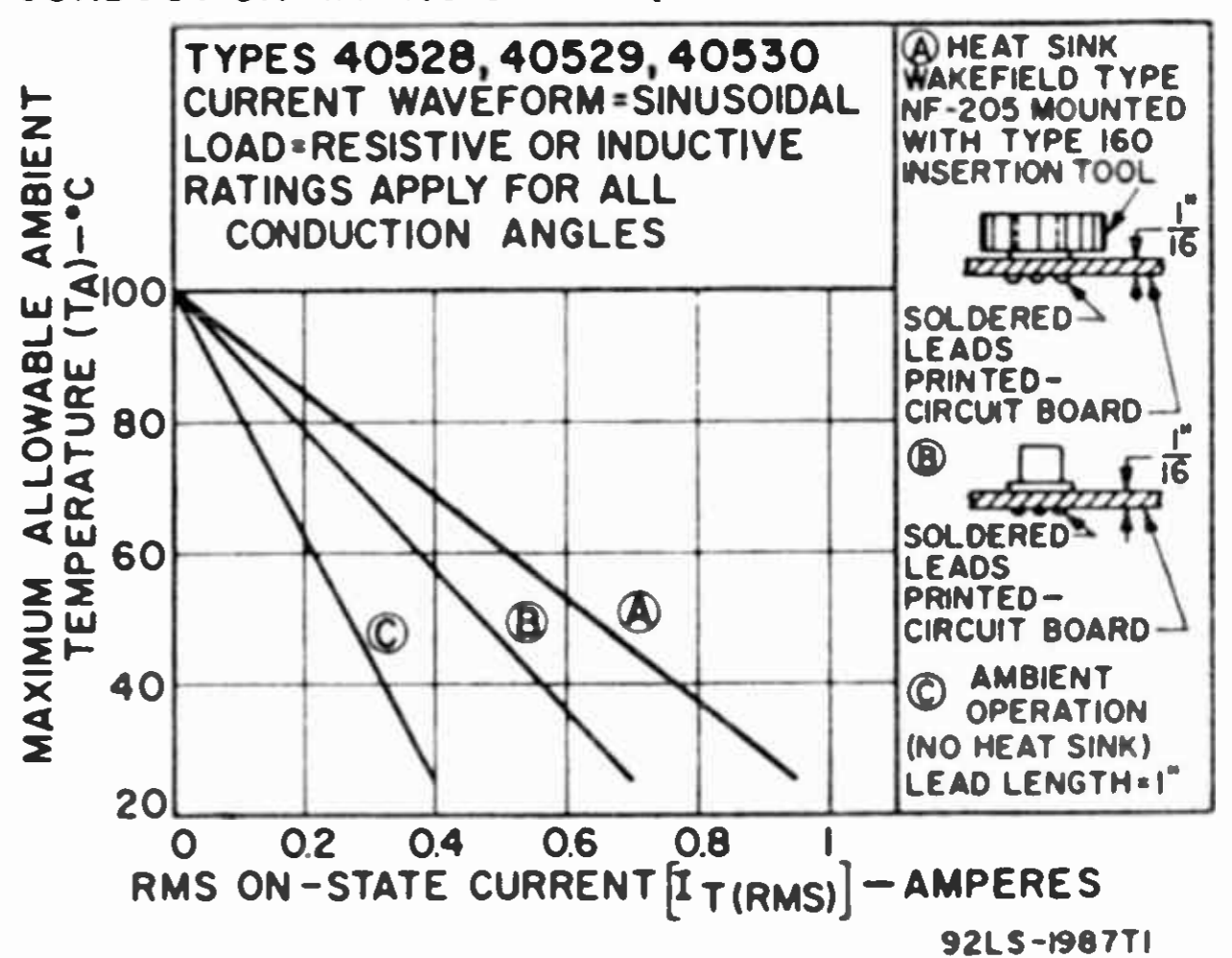
CONDUCTION RATING CHART (CASE TEMPERATURE)



CONDUCTION RATING CHART (AMBIENT TEMPERATURE)

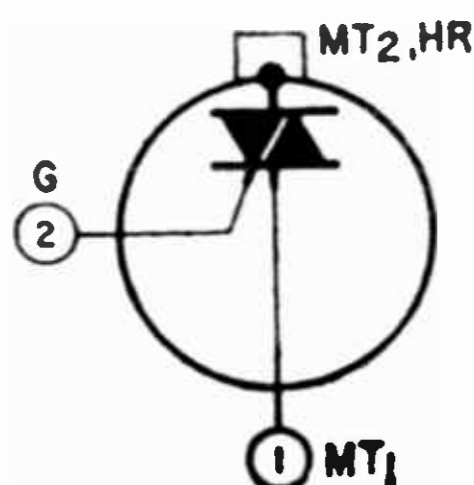


CONDUCTION RATING CHART (AMBIENT TEMPERATURE)



TRIACS

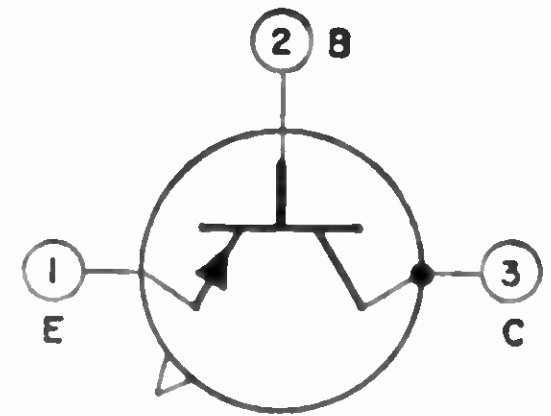
40531-40536



Si gated bidirectional types used for power-control and power-switching applications. JEDEC TO-5 (with heat radiator), Outline No.8. Types 40531, 40532, 40533, 40534, 40535, and 40536 are electrically identical with types 40525, 40526, 40527, 40528, 40529, and 40530, respectively.

40537 POWER TRANSISTOR

Si p-n-p double-diffused epitaxial planar type used as a driver in audio-amplifier circuits. JEDEC TO-5, Outline No.5.



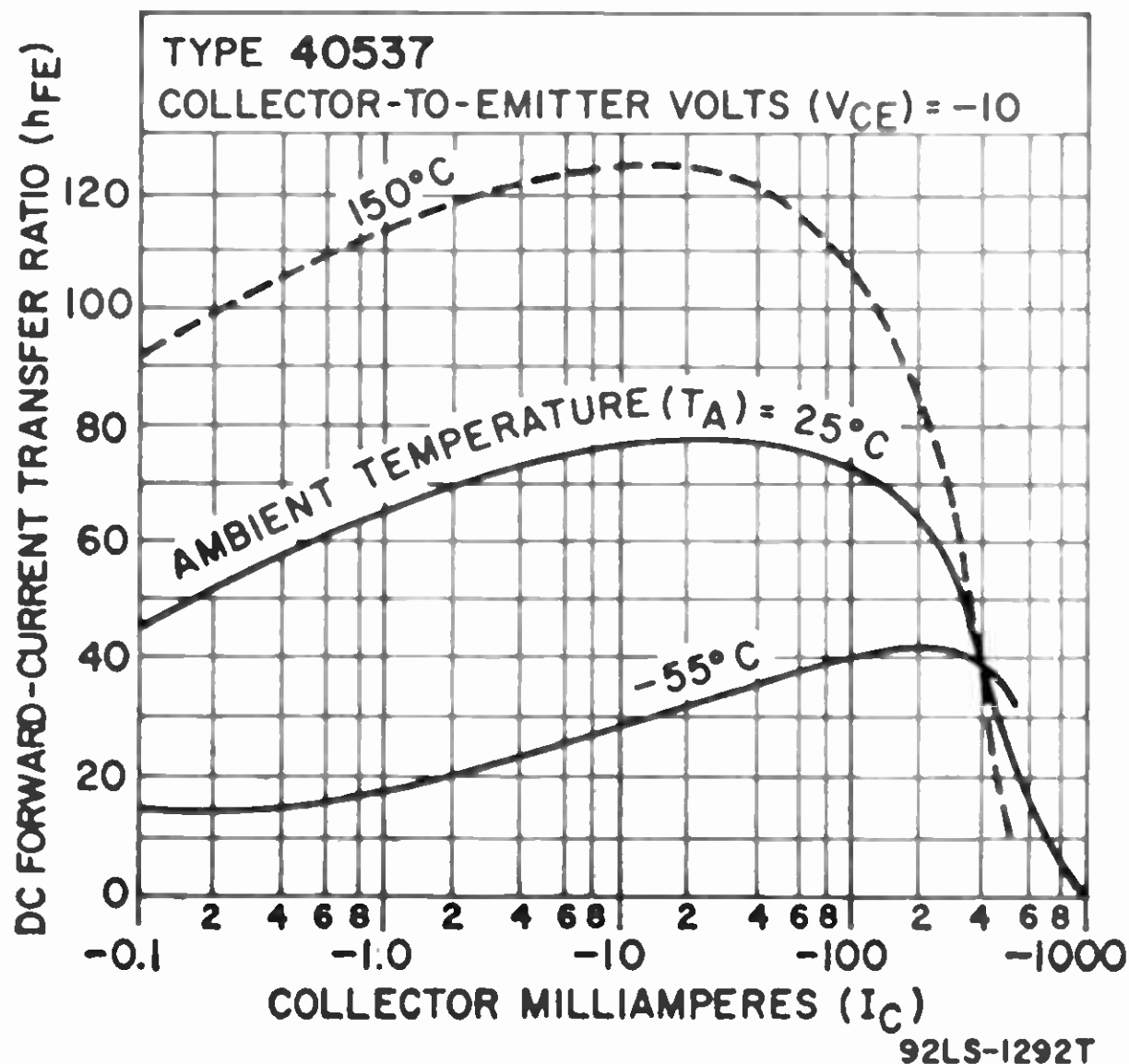
MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage ($R_{BE} = 500 \Omega$)	$V_{CE(SUS)}$	-55	V
Emitter-to-Base Voltage	V_{EBO}	-5	V
Collector Current	I_C	-0.7	A
Base Current	I_B	-0.2	A
Transistor Dissipation:			
T_C up to 25°C	P_T	5	W
T_C above 25°C	P_T	Derate linearly to 0 W at 200 °C	
T_A up to 25°C	P_T	1	W
T_A above 25°C	P_T	Derate linearly to 0 W at 200 °C	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	230	°C

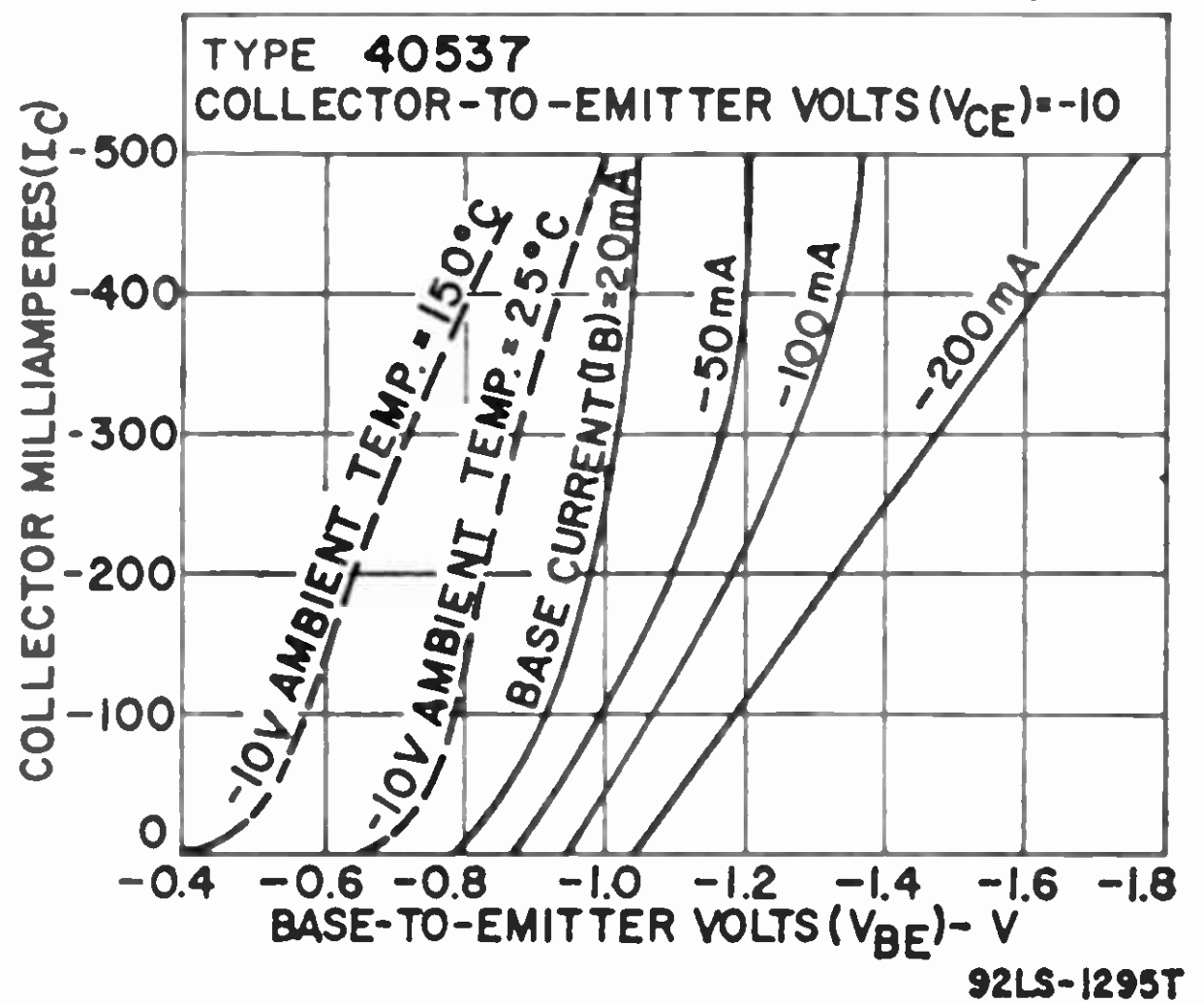
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_C = -100 \text{ mA}, R_{BE} = 500 \Omega$)	$V_{CE(SUS)}$	-55 min	V
Collector-to-Emitter Saturation Voltage ($I_C = -50 \text{ mA}, I_B = -5 \text{ mA}$)	$V_{CE(sat)}$	-1.1 max	V
Base-to-Emitter Voltage ($V_{CE} = -4 \text{ V}, I_C = -50 \text{ mA}$)	V_{BE}	-1.8	V
Collector-Cutoff Current ($V_{CE} = -45 \text{ V}, R_{BE} = 500 \Omega$)	I_{CER}	-10 max	μA
Emitter-Cutoff Current ($V_{EB} = -5 \text{ V}, I_C = 0$)	I_{EBO}	-1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = -4 \text{ V}, I_C = -50 \text{ mA}$)	h_{FE}	50 to 300	
Gain-Bandwidth Product ($V_{CE} = -4 \text{ V}, I_C = -50 \text{ mA}$)	f_T	100	MHz
Thermal Resistance, Junction-to-Ambient	θ_{J-A}	175	°C/W

TYPICAL DC FORWARD-CURRENT TRANSFER-RATIO CHARACTERISTICS

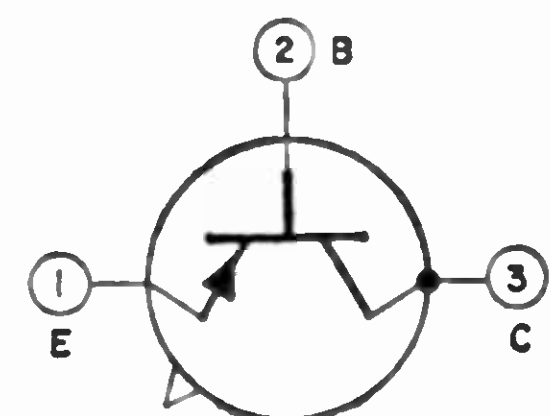


TYPICAL TRANSFER CHARACTERISTICS



40538 POWER TRANSISTOR

Si p-n-p double-diffused epitaxial planar type used in complementary-symmetry output stages. P-N-P structure permits complementary operation with a matching n-p-n type such as the 40539. JEDEC TO-5, Outline No.5. This type is identical to type 40537 except for the following items:

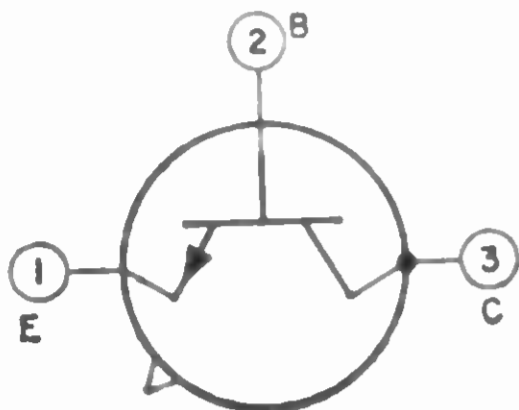


CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Saturation Voltage ($I_C = -500$ mA, $I_B = -50$ mA)	$V_{CE(sat)}$	-2 max	V
Base-to-Emitter Voltage ($V_{CE} = -4$ V, $I_C = -500$ mA)	V_{BE}	-2.7 max	V
Pulsed Forward-Current Transfer Ratio ($V_{CE} = -4$ V, $I_C = -500$ mA, $t_P = 300$ μ s, $df < 2\%$)	h_{FE} (pulsed)	15 to 90	

POWER TRANSISTOR

40539



Si n-p-n triple-diffused planar type used in complementary-symmetry output stages. N-P-N structure permits complementary operation with a matching p-n-p type such as the 40538. JEDEC TO-5, Outline No.5.

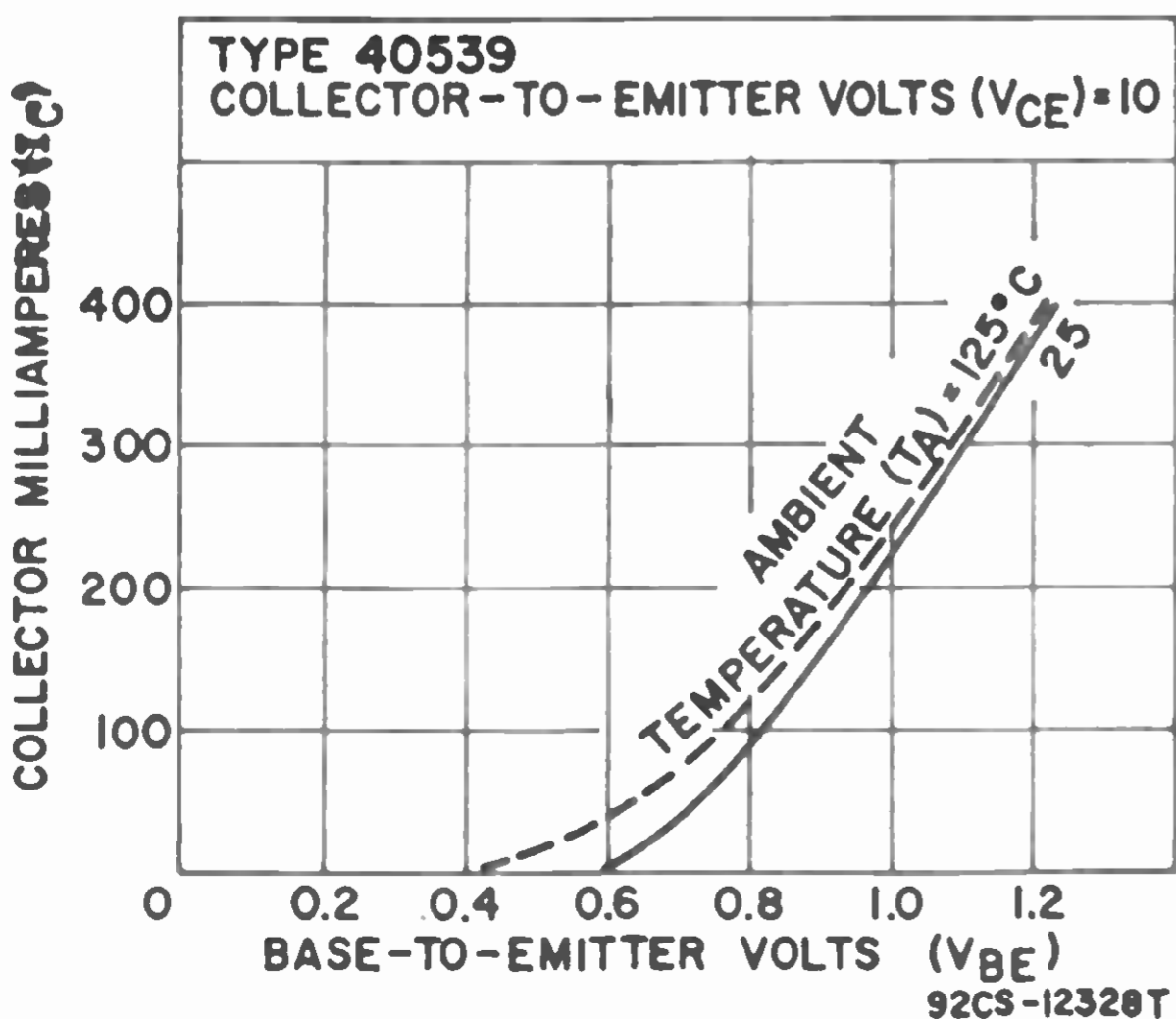
MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage $R_{BE} = 500 \Omega$	$V_{CER(sus)}$	55	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	0.7	A
Transistor Dissipation:			
T_C up to 25°C	P_T	5	W
T_C above 25°C	P_T	Derate linearly to 0 W at 200 °C	
T_A up to 25°C	P_T	1	W
T_C above 25°C	P_T	Derate linearly to 0 W at 200 °C	
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	255	°C

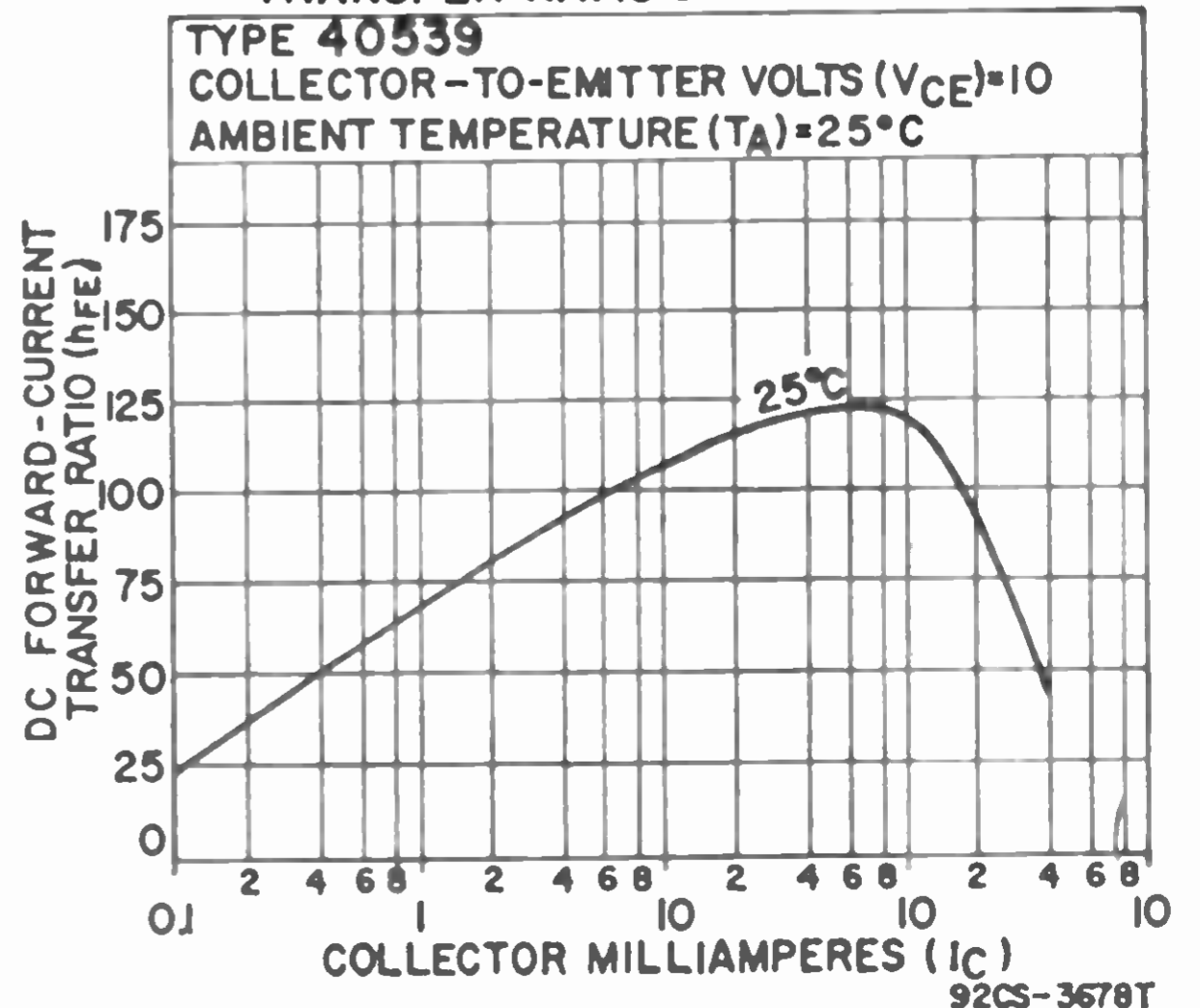
CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_C = 100$ mA, $R_{BE} = 500 \Omega$)	$V_{CER(sus)}$	55 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 500$ mA, $I_B = 50$ mA)	$V_{CE(sat)}$	2 max	V
Base-to-Emitter Voltage ($V_{CE} = 4$ V, $I_C = 500$ mA)	V_{BE}	2.7 max	V
Collector-Cutoff Current ($V_{CE} = 45$ V, $R_{BE} = 500 \Omega$)	I_{CER}	10 max	μ A
Emitter-Cutoff Current ($V_{EB} = 5$ V, $I_C = 0$)	I_{EBO}	1 max	mA
Static Forward-Current Transfer Ratio ($V_{EB} = 4$ V, $I_C = 500$ mA)	h_{FE}	15 to 90	
Gain-Bandwidth Product ($V_{CE} = 4$ V, $I_C = 50$ mA)	f_T	100	MHz
Thermal Resistance, Junction-to-Case	θ_{J-C}	35	°C/W

TYPICAL TRANSFER CHARACTERISTICS

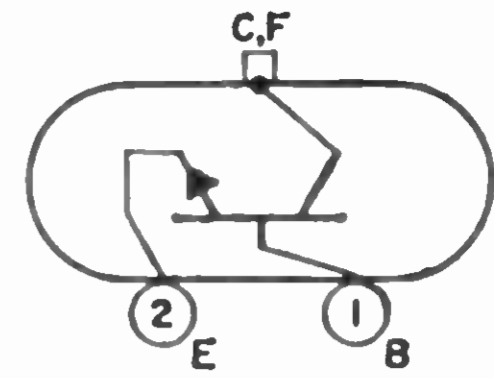


TYPICAL DC FORWARD-CURRENT TRANSFER RATIO CHARACTERISTIC



40542 POWER TRANSISTOR

Si n-p-n type featuring a base comprised of a homogeneous-resistivity silicon material and molded silicon plastic package with vertical leads. This type fits a standard TO-3 socket. It is used in complementary-symmetry output stages of audio-amplifier circuits. It permits complementary operation with a matching p-n-p type such as 40051. Outline No.50. See Mounting Hardware for desired mounting arrangement.



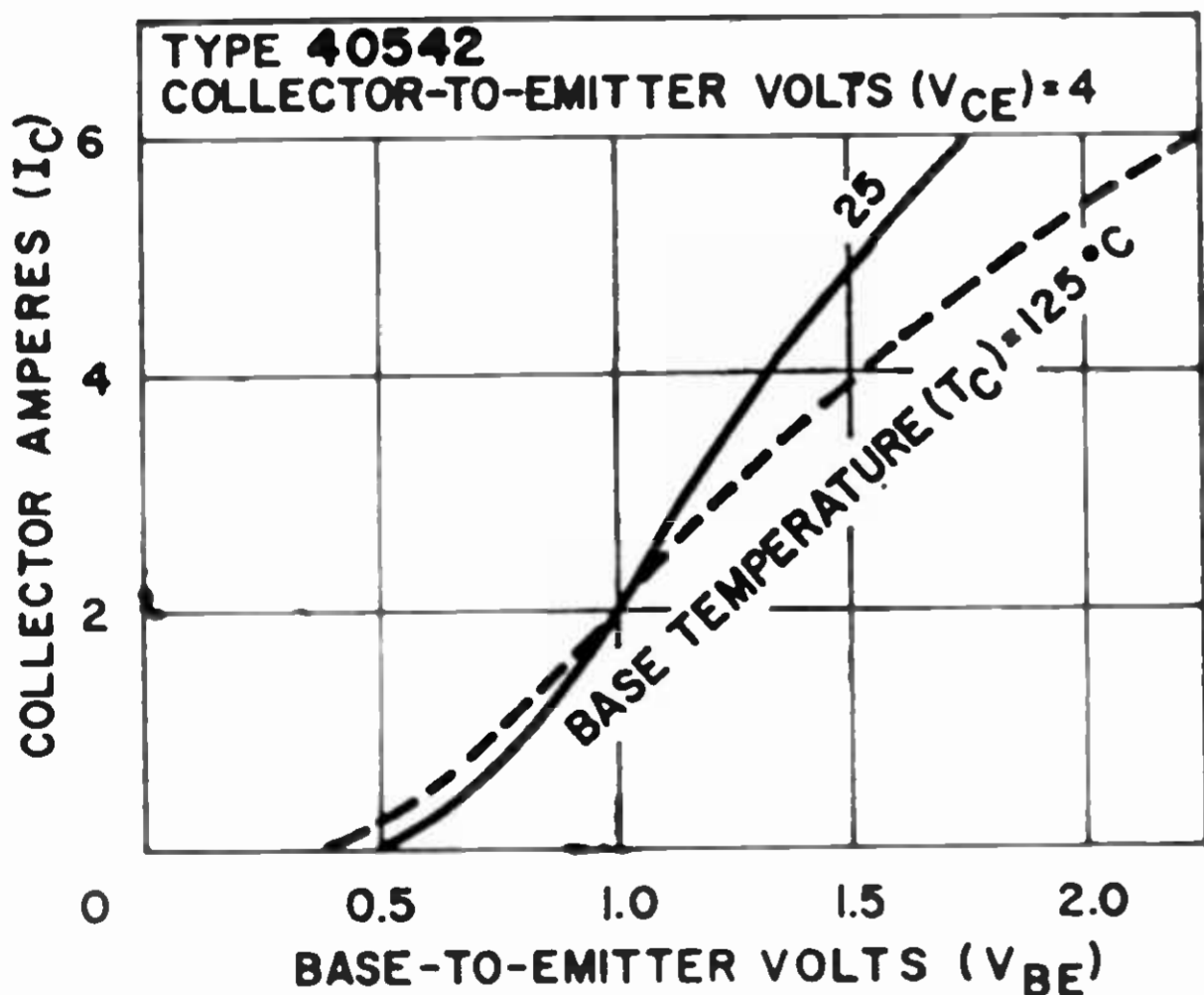
MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage ($R_{BE} = 100 \Omega$)	$V_{CER(sus)}$	50	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	6	A
Transistor Dissipation:			
T_c up to 25°C	P_T	83	W
T_c above 25°C	P_T	Derate linearly 0 W at 150 °C	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 150	°C
Storage	T_{STG}	-65 to 150	°C
Lead-Soldering Temperature (10 s max)	T_L	235	°C

CHARACTERISTICS (At case temperature = 25°C)

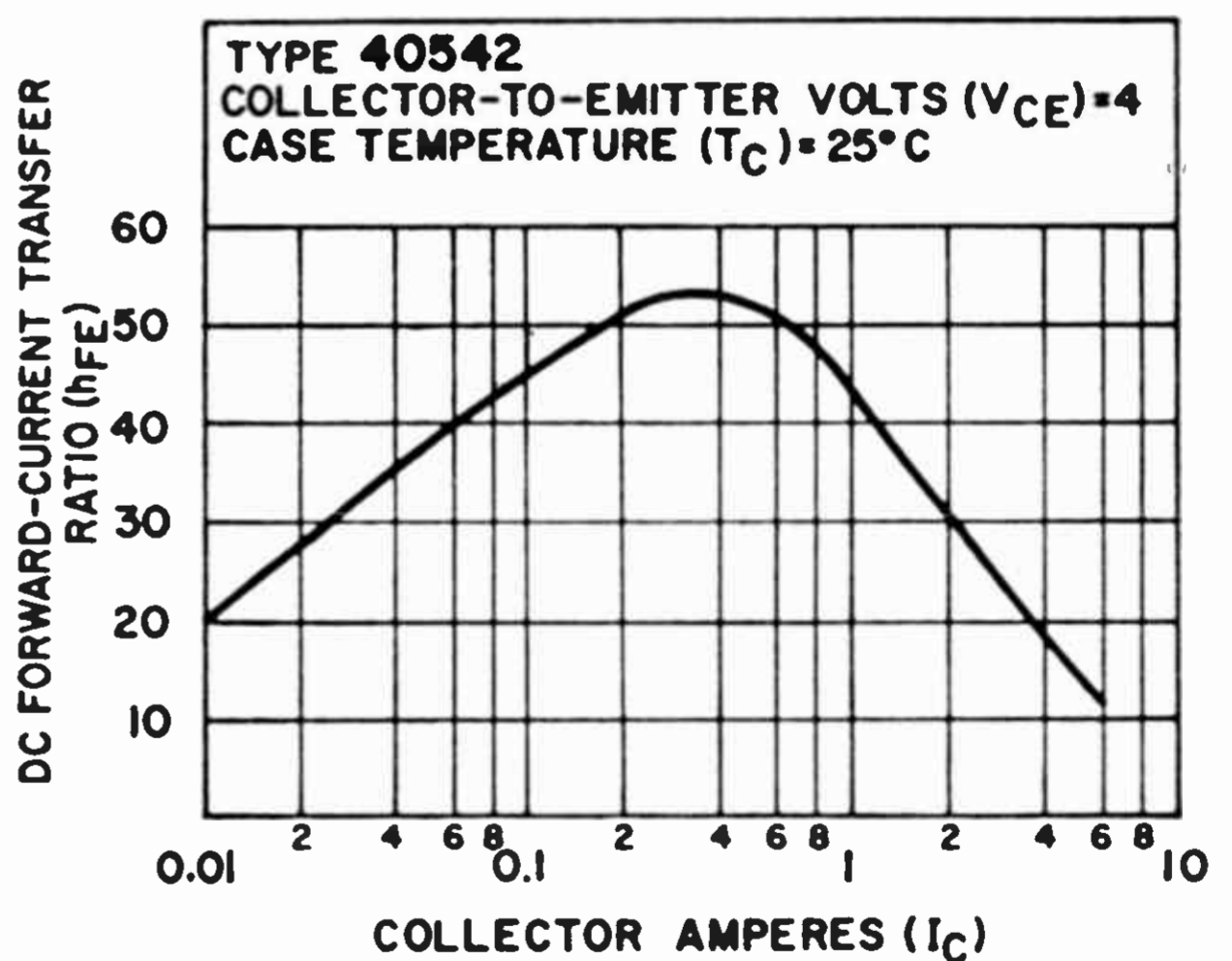
Collector-to-Emitter Sustaining Voltage ($I_C = 0.2$ A, $R_{BE} = 100 \Omega$, $t_P = 300 \mu s$, $df = 1.8\%$)	$V_{CER(sus)}$	50 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 2.5$ A, $I_B = 0.25$ A, $t_P = 300 \mu s$, $df = 1.8\%$)	$V_{CE(sat)}$	1 max	V
Base-to-Emitter Voltage ($V_{CE} = 4$ V, $I_C = 2.5$ A, $t_P = 300 \mu s$, $df = 1.8\%$)	V_{BE}	1.7 max	V
Collector-Cutoff Current ($V_{CE} = 40$ V, $R_{BE} = 100 \Omega$)	I_{CER}	1 max	mA
Emitter-Cutoff Current ($V_{EB} = 5$ V, $I_C = 0$)	I_{EBO}	5 max	mA
Pulsed Static Forward-Current Transfer Ratio ($V_{CE} = 4$ V, $I_C = 2.5$ A, $t_P = 300 \mu s$, $df = 1.8\%$)	$h_{FE}(pulsed)$	20 to 70	
Gain-Bandwidth Product ($V_{CE} = 4$ V, $I_C = 0.5$ A)	f_T	0.8 to 2.8	MHz
Thermal Resistance, Junction-to-Case	θ_{J-c}	1.5 max	°C/W

TYPICAL TRANSFER CHARACTERISTICS



92SS-3603T

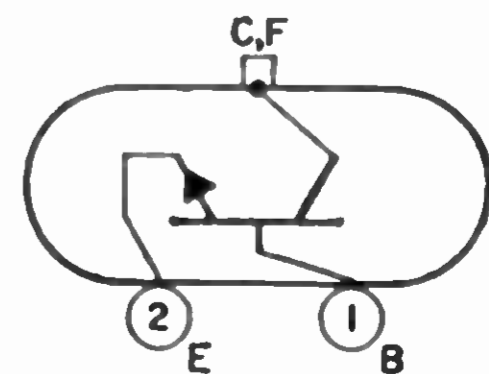
TYPICAL DC FORWARD-CURRENT TRANSFER-RATIO CHARACTERISTIC



92SS-3606T

40543 POWER TRANSISTOR

Si n-p-n type featuring a base comprised of a homogeneous-resistivity silicon material and molded silicone plastic package with vertical leads. This type fits a standard TO-3 socket. It is designed specifically for amplifier applications. Outline No.50. See Mounting Hardware for desired mounting arrangement. This type is identical with type 40542 except for the following items:

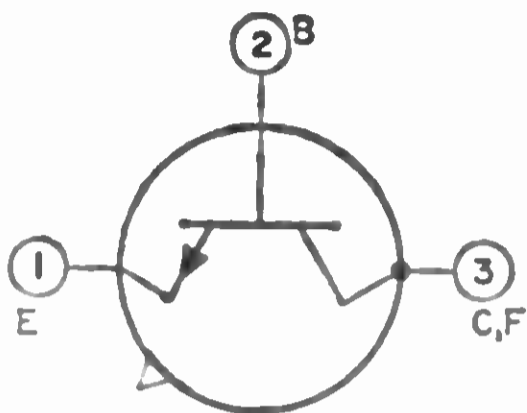


MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage ($R_{BE} = 100 \Omega$)	$V_{CER(SUS)}$	60	V
Collector Current	I_C	8	A

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_C = 0.2 \text{ A}$, $R_{BE} = 100 \Omega$, $t_P = 300 \mu\text{s}$, $df = 1.8\%$)	$V_{CER(SUS)}$	60	V
Collector-to-Emitter Saturation Voltage ($I_C = 3 \text{ A}$, $I_B = 0.3 \text{ A}$, $t_P = 300 \mu\text{s}$, $df = 1.8\%$)	$V_{CE(sat)}$	1	V
Base-to-Emitter Voltage ($V_{CE} = 4 \text{ V}$, $I_C = 3 \text{ A}$, $t_P = 300 \mu\text{s}$, $df = 1.8\%$)	V_{BE}	1.7	V
Collector-Cutoff Current ($V_{CE} = 50 \text{ V}$, $R_{BE} = 100 \Omega$)	I_{CER}	1	mA
Pulsed Static Forward-Current Transfer Ratio ($V_{CE} = 4 \text{ V}$, $I_C = 3 \text{ A}$, $t_P = 300 \mu\text{s}$, $df = 1.8\%$)	$h_{FE}(\text{pulsed})$	20 to 70	



POWER TRANSISTOR

40544

Si n-p-n triple-diffused planar type used specifically as a driver in audio-amplifier circuits. JEDEC TO-5, Outline No.6.

MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage $R_{BE} = 100 \Omega$	$V_{CER(SUS)}$	50	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	0.7	A
Transistor Dissipation: T_C up to 25°C	P_T	7	W
T_A above 25°C	P_T	Derate linearly to 0 W at 200 °C	
Temperature Range: Operating (Junction)	$T_J(\text{opr})$	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	255	°C

CHARACTERISTICS (At case temperature = 25°C)

Collector-to-Emitter Sustaining Voltage ($I_C = 100 \text{ mA}$, $R_{BE} = 100 \Omega$)	$V_{CER(SUS)}$	50 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 150 \text{ mA}$, $I_B = 15 \text{ mA}$)	$V_{CE(sat)}$	1 max	V
Base-to-Emitter Voltage ($V_{CE} = 4 \text{ V}$, $I_C = 50 \text{ mA}$)	V_{BE}	1.7 max	V
Collector-Cutoff Current ($V_{CE} = 40 \text{ V}$, $R_{BE} = 100 \Omega$)	I_{CER}	10 max	μA
Emitter-Cutoff Current ($V_{EB} = 5 \text{ V}$, $I_C = 0$)	I_{EBO}	1 max	mA
Static Forward-Current Transfer Ratio ($V_{EB} = 4 \text{ V}$, $I_C = 50 \text{ mA}$)	h_{FE}	35 to 200	
Gain-Bandwidth Product ($V_{CE} = 4 \text{ V}$, $I_C = 50 \text{ mA}$)	f_T	100	MHz
Thermal Resistance, Junction-to-Case	θ_{J-C}	25 max	°C/W

Refer to Chart of Discontinued Transistors

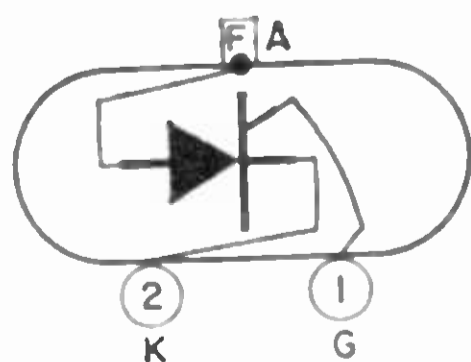
40546

Refer to Chart of Discontinued Transistors

40547

SILICON CONTROLLED RECTIFIERS

**40553-
40555**



Si all-diffused three-junction types for use in inverter applications such as ultrasonics and fluorescent lighting. See Mounting Hardware for desired mounting arrangement. JEDEC TO-66, Outline No.25.

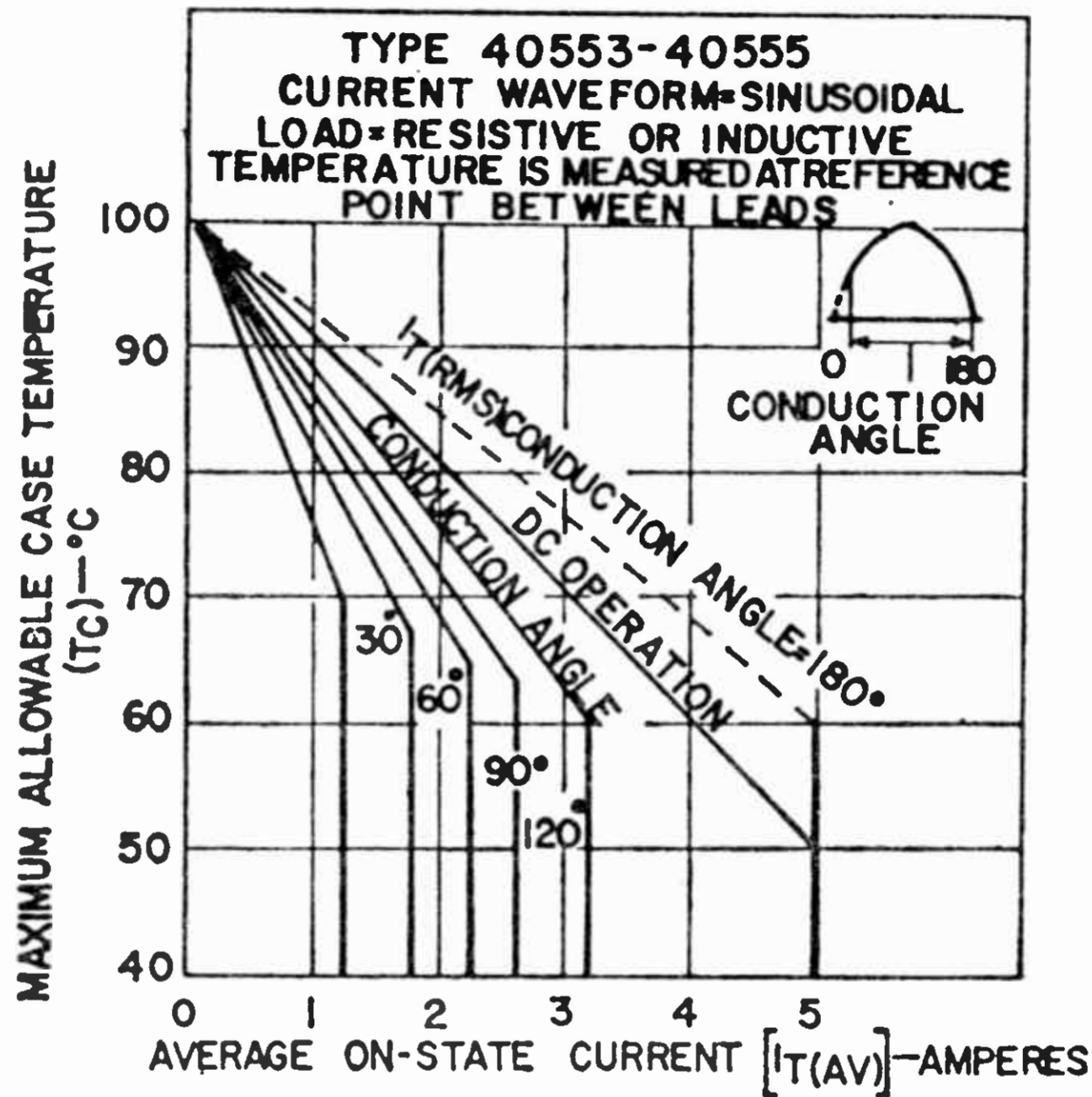
MAXIMUM RATINGS (For sinusoidal ac supply voltage at low to ultrasonic frequencies with resistive or inductive load)

	40553	40554	40555	
V_{RSOM}	330	660	700	V
V_{RROM}	200	400	600	V
V_{DROM}		700		V

MAXIMUM RATINGS (cont'd)

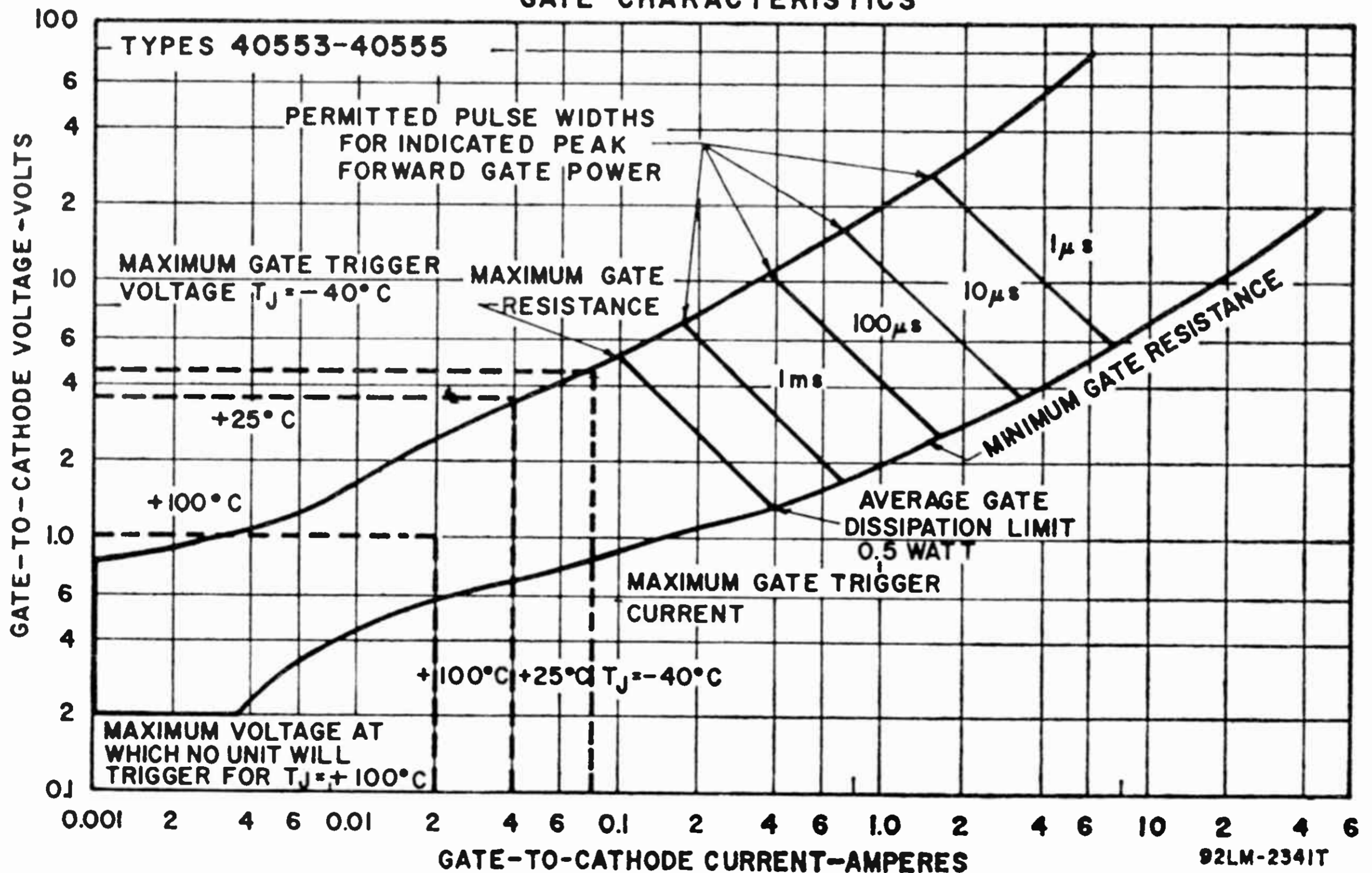
$I_{T(AV)}$ ($T_c = 60^\circ\text{C}$, 60 Hz at conduction angle = 180°)	_____	3.2	_____	A
$I_{T(RMS)}$	_____	5	_____	A
I_{TSM} (1 cycle of voltage)	_____	80	_____	A
$[I_{TS(RMS)}]^2 t$ (at 8.3 ms)	_____	25	_____	A ² s
Critical di/dt ($V_D = V_{F(BO)}$, $I_{GT} = 50$ mA, $t_r = 0.1 \mu\text{s}$)	_____	200	_____	A/ μs
P_{GM} (10 μs)	_____	13	_____	W
$P_{G(AV)}$	_____	0.5	_____	W
T_{STG}	_____	40 to 150	_____	$^\circ\text{C}$
$T_c(\text{opr})$	_____	40 to 100	_____	$^\circ\text{C}$

**CONDUCTION RATING CHART
CASE TEMPERATURE**



92LS-2342T

GATE CHARACTERISTICS

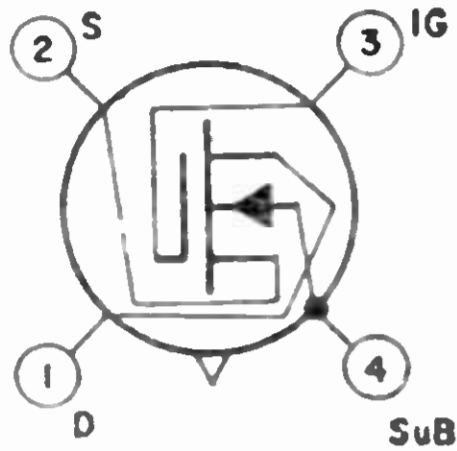


92LM-2341T

CHARACTERISTICS (At maximum electrical ratings at $T_c = 25^\circ\text{C}$)

	200 min	400 min	600 min	V
$V_{F(BO)O}$ ($T_c = 100^\circ\text{C}$)	—	—	—	V
I_{DOM} ($V_{DO} = V_{F(BO)O}$)	—	0.5 typ; 3 max	—	mA
I_{RRM} ($V_{RO} = V_{RRM}$)	—	0.3 typ; 1.5 max	—	mA
V_{TM} ($i_T = 30\text{ A}$)	—	2.2 typ; 3 max	—	V
I_{GT}	—	15 typ; 40 max	—	mA (dc)
V_{GT}	—	1.8 typ; 3.5 max	—	V (dc)
I_{HO}	—	20 typ; 50 max	—	mA
Critical dv/dt ($V_{DO} = V_{F(BO)O}$, $T_c = 80^\circ\text{C}$)	—	100 min; 250 typ	—	V/ μs
t_{gt} ($V_D = V_{F(BO)O}$, $I_{TM} = 2\text{ A}$, $I_{GT} = 300\text{ mA}$, $t_r = 0.1$)	—	0.7	—	μs
t_{cl} ($V_D = V_{F(BO)O}$, $i_T = 2\text{ A}$, $t_p = 50\ \mu\text{s}$, $V_R = 80\text{ V min}$, $t_r = 0.1\ \mu\text{s}$, $dv/dt =$ $100\text{ V}/\mu\text{s}$, $di_R/dt = 10\text{ A}/\mu\text{s}$, $I_{GT} = 100\text{ mA}$ at t_{on} , $V_{GT} = 0\text{V}$ at t_{off} , $T_c = 80^\circ\text{C}$)	—	4 typ; 6 max	—	μs

FIELD-EFFECT TRANSISTOR 40559



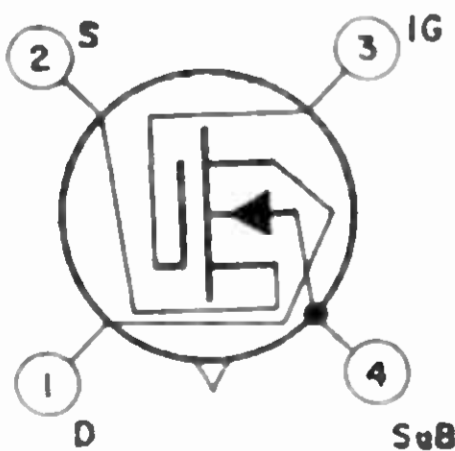
Si insulated-gate field-effect (MOS) n-channel depletion type used as a mixer in receivers covering the 88-to-108-MHz band and for general amplifier applications at frequencies up to 125 MHz. JEDEC TO-104, Outline No.31. For maximum ratings refer to type 40468. For typical forward transconductance characteristics curves,

refer to type 3N140.

CHARACTERISTICS

Gate-to-Source Cutoff Voltage ($V_{DS} = 20\text{ V}$, $I_D = 0.05\text{ mA}$)	$V_{GS}(\text{off})$	-4 typ; -6 max	V
Gate Reverse Current ($V_{GS} = -8\text{ V}$, $V_{DS} = 0$)	I_{GSS}	1 max	nA
Zero-Gate-Voltage Drain Current ($V_{DS} = 15\text{ V}$, $V_{GS} = 0$)	I_{DSS}	5 to 50	mA
Small-Signal Reverse Transfer Capacitance, Drain-to-Gate ($V_{DS} = 15\text{ V}$, $I_D = 5\text{ mA}$, $f = 1\text{ MHz}$)	C_{rss}	0.1 to 0.2	pF
Input Resistance: $V_{DS} = 15\text{ V}$, $I_D = 5\text{ mA}$, $f = 100\text{ MHz}$	r_{iss}	4.5	k Ω
$V_{DS} = 15\text{ V}$, $I_D = 2\text{ mA}$, $f = 100\text{ MHz}$	r_{iss}	5	k Ω
Output Resistance: $V_{DS} = 15\text{ V}$, $I_D = 5\text{ mA}$, $f = 100\text{ MHz}$	r_{oss}	4.2	k Ω
$V_{DS} = 15\text{ V}$, $I_D = 5\text{ mA}$, $f = 10.7\text{ MHz}$	r_{oss}	18 max	k Ω
Input Capacitance ($V_{DS} = 15\text{ V}$, $I_D = 5\text{ mA}$, $f = 100\text{ MHz}$)	C_{iss}	5.5	pF
Output Capacitance ($V_{DS} = 15\text{ V}$, $I_D = 2\text{ mA}$, $f = 10.7\text{ MHz}$)	C_{oss}	1.4	pF
Forward Conversion Conductance ($V_{DS} = 15\text{ V}$, $I_D = 2\text{ mA}$, $f = 100\text{ MHz}$)	g_c	1.3	mmhos
Maximum Available Conversion Gain ($V_{DS} = 15\text{ V}$, $I_D = 2\text{ mA}$, $f_{in} = 100\text{ MHz}$, $f_{out} = 10.7\text{ MHz}$)	MAG _c	25.8	dB

FIELD-EFFECT TRANSISTOR 40559A



Si insulated-gate field-effect (MOS) n-channel depletion type used in mixer applications in FM receivers covering the 88-to-108-MHz band, and in general amplifier applications at frequencies up to 125 MHz. JEDEC TO-72, Outline No.28. For maximum ratings, refer to type 40468A. For typical forward transconductance characteristics curves, refer to type 3N140.

refer to type 3N140.

CHARACTERISTICS

Drain-to-Source Cutoff Current ($V_{DS} = 12\text{ V}$, $V_{GS} = -8\text{ V}$)	$I_D(\text{off})$	500 max	μA
Gate Leakage Current: $V_{GS} = -8\text{ V}$, $V_{DS} = 0$	I_{GSS}	1 max	nA
$V_{GS} = 1\text{ V}$, $V_{DS} = 0$	I_{GSS}	1 max	nA
Zero-Bias Drain Current ($V_{DS} = 15\text{ V}$, $V_{GS} = 0$, $t_p \leq 20\text{ ms}$, $df \leq 0.15$)	I_{DSS}	5 to 25	mA
Small-Signal Reverse-Transfer Capacitance, Drain-to-Gate ($V_{DS} = 15\text{ V}$, $I_D = 5\text{ mA}$, $f = 1\text{ MHz}$)	C_{rss}	0.15 typ; 0.3 max	pF
Input Capacitance ($V_{DS} = 15\text{ V}$, $I_D = 5\text{ mA}$, $f = 1\text{ MHz}$)	C_{iss}	5.5	pF

CHARACTERISTICS (cont'd)

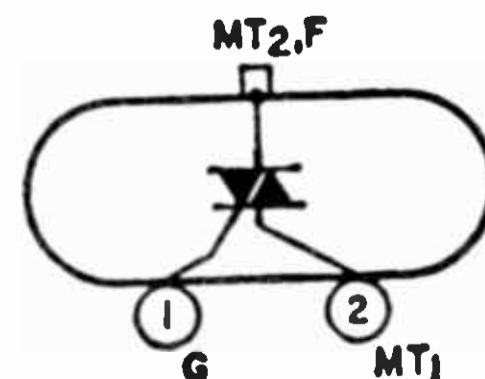
Output Capacitance ($V_{DS} = 15\text{ V}$, $I_D = 5\text{ mA}$, $f = 1\text{ MHz}$)	C_{oss}	1.4	pF
Input Resistance ($V_{DS} = 15\text{ V}$, $I_D = 3\text{ mA}$, $V_{BS} = -3\text{ V}$, $f = 100\text{ MHz}$)	r_{iss}	6	k Ω
Output Resistance ($V_{DS} = 15\text{ V}$, $I_D = 3\text{ mA}$, $V_{BS} = -3\text{ V}$, $f = 10.7\text{ MHz}$)	r_{oss}	12	k Ω
Forward Conversion Transconductance ($V_{DS} = 15\text{ V}$, $I_D = 3\text{ mA}$, $V_{BS} = -3\text{ V}$, $f = 1\text{ kHz}$)	$g_{fs}(c)$	2800	μmhos
Maximum Available Conversion Gain ($V_{DS} = 15\text{ V}$, $I_D = 3\text{ mA}$, $f_{in} = 100\text{ MHz}$, $f_{out} = 10.7\text{ MHz}$)	MAG _c	21	dB

- 40561** Refer to Chart of Tunnel Diode Data
- 40562** Refer to Chart of Tunnel Diode Data
- 40563** Refer to Chart of Tunnel Diode Data
- 40564** Refer to Chart of Tunnel Diode Data
- 40565** Refer to Chart of Tunnel Diode Data
- 40566** Refer to Chart of Tunnel Diode Data
- 40567** Refer to Chart of Tunnel Diode Data
- 40568** Refer to Chart of Tunnel Diode Data
- 40569** Refer to Chart of Tunnel Diode Data
- 40570** Refer to Chart of Tunnel Diode Data
- 40571** Refer to Chart of Tunnel Diode Data
- 40572** Refer to Chart of Tunnel Diode Data
- 40573** Refer to Chart of Tunnel Diode Data
- 40574** Refer to Chart of Tunnel Diode Data

40575
40576

TRIACS

Si gate-controlled full-wave types used for the control of ac loads in applications such as space heater, oven, and furnace controls. See **Mounting Hardware** for desired mounting arrangement. JEDEC TO-66, Outline No.25.



MAXIMUM RATINGS (For sinusoidal supply voltage at 50/60 Hz with resistive or inductive load)

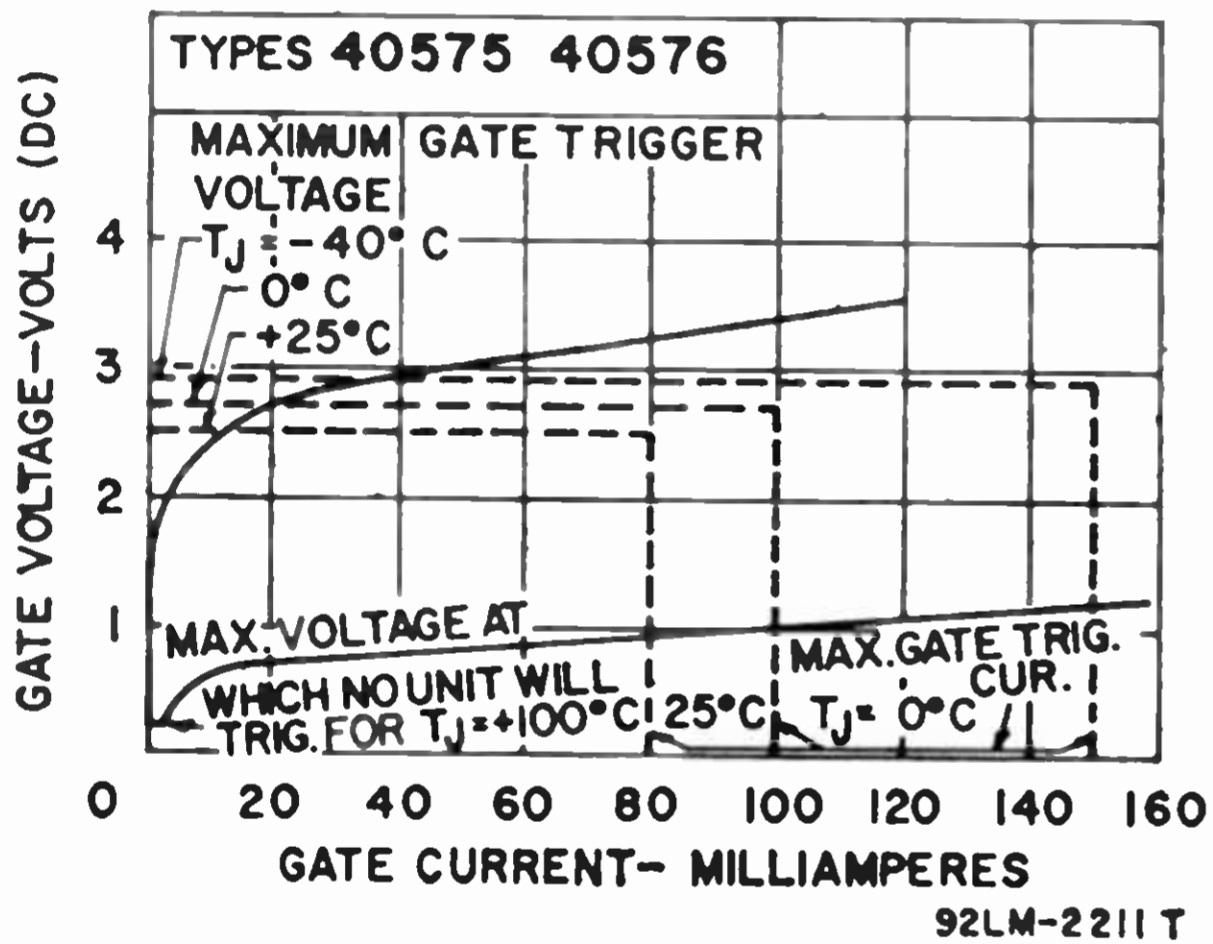
	40575		40576	
V_{DROM}^* ($T_J = -40^\circ\text{C}$ to 100°C)	200		400	V
$I_{T(RMS)}$ ($T_C = 70^\circ\text{C}$, conduction angle of 360°)	_____	15	_____	A
I_{TSM} (1 cycle sinusoidal principal voltage)	_____	100	_____	A
$I_{GTM}\ddagger$ ($2\ \mu\text{s}$ max.)	_____	1	_____	A
P_{GM} ($2\ \mu\text{s}$ max, $I_{GTM} \leq 1\text{ A}$ peak)	_____	20	_____	W
$P_{G(AV)}$	_____	0.45	_____	W
T_{STG}	_____	-40 to 150	_____	$^\circ\text{C}$
$T_C(\text{opr})$	_____	-40 to 100	_____	$^\circ\text{C}$

CHARACTERISTICS (At maximum electrical ratings at $T_c = 25^\circ\text{C}$)

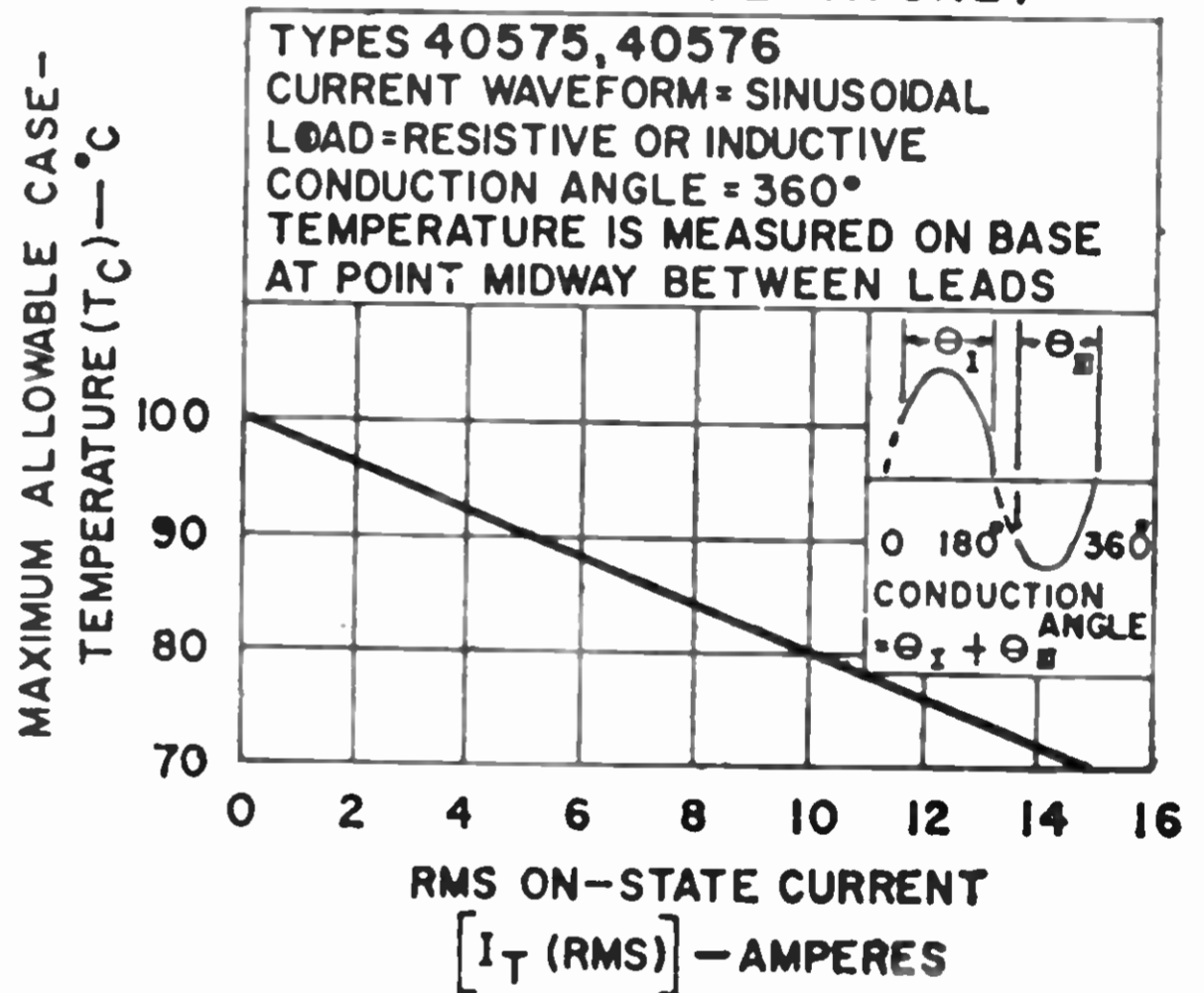
I_{DROM}^* ($T_J = 100^\circ\text{C}$, $V_{DROM} = \text{max rated value}$)	_____ 0.2 typ; 4 max _____	mA
V_{TM}^* ($i_T = 30 \text{ A peak}$)	_____ 1.6 typ; 2 max _____	V (peak)
I_{HO}^* (initial principal current = 150 mA dc)	_____ 15 typ; 60 max _____	mA (dc)
Commutating dv/dt^* ($v_D = V_{DROM}$, $I_{T(RMS)} = 15 \text{ A}$, commutating $di/dt = 8 \text{ A/ms}$, gate unenergized at $T_c = 70^\circ\text{C}$)	_____ 10 _____	V/ μs
Critical dv/dt^* ($v_D = V_{DROM}$, exponential voltage rise, $T_c = 100^\circ\text{C}$)	_____ 40 _____	V/ μs
I_{GT}^{\ddagger} ($v_D = 6 \text{ Vdc}$, $R_L = 12 \Omega$):		
I ⁺ mode, V_{MT2} positive, V_G positive	_____ 15 typ; 30 max _____	mA (dc)
I ⁻ mode, V_{MT2} positive, V_G negative	_____ 35 typ; 80 max _____	mA (dc)
III ⁺ mode, V_{MT2} negative, V_G positive	_____ 35 typ; 80 max _____	mA (dc)
III ⁻ mode, V_{MT2} negative, V_G negative	_____ 15 typ; 30 max _____	mA (dc)
V_{GT}^{\ddagger} ($v_D = 6 \text{ Vdc}$, $R_L = 12 \Omega$)	_____ 1 typ; 2.5 max _____	V (dc)
V_{GT}^{\ddagger} ($v_D = V_{DROM}$, $R_L = 125 \Omega$, $T_c = 100^\circ\text{C}$)	_____ 0.2 min _____	V (dc)
t_{gt} ($v_D = V_{DROM}$, $I_{GT} = 160 \text{ mA}$, $t_r = 0.1 \mu\text{s}$, $i_T = 25 \text{ A peak}$)	_____ 3 _____	μs
θ_{J-C}	_____ 1.3 max _____	$^\circ\text{C/W}$

* For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
 \ddagger For either polarity of gate voltage (V_G) with reference to main terminal 1.

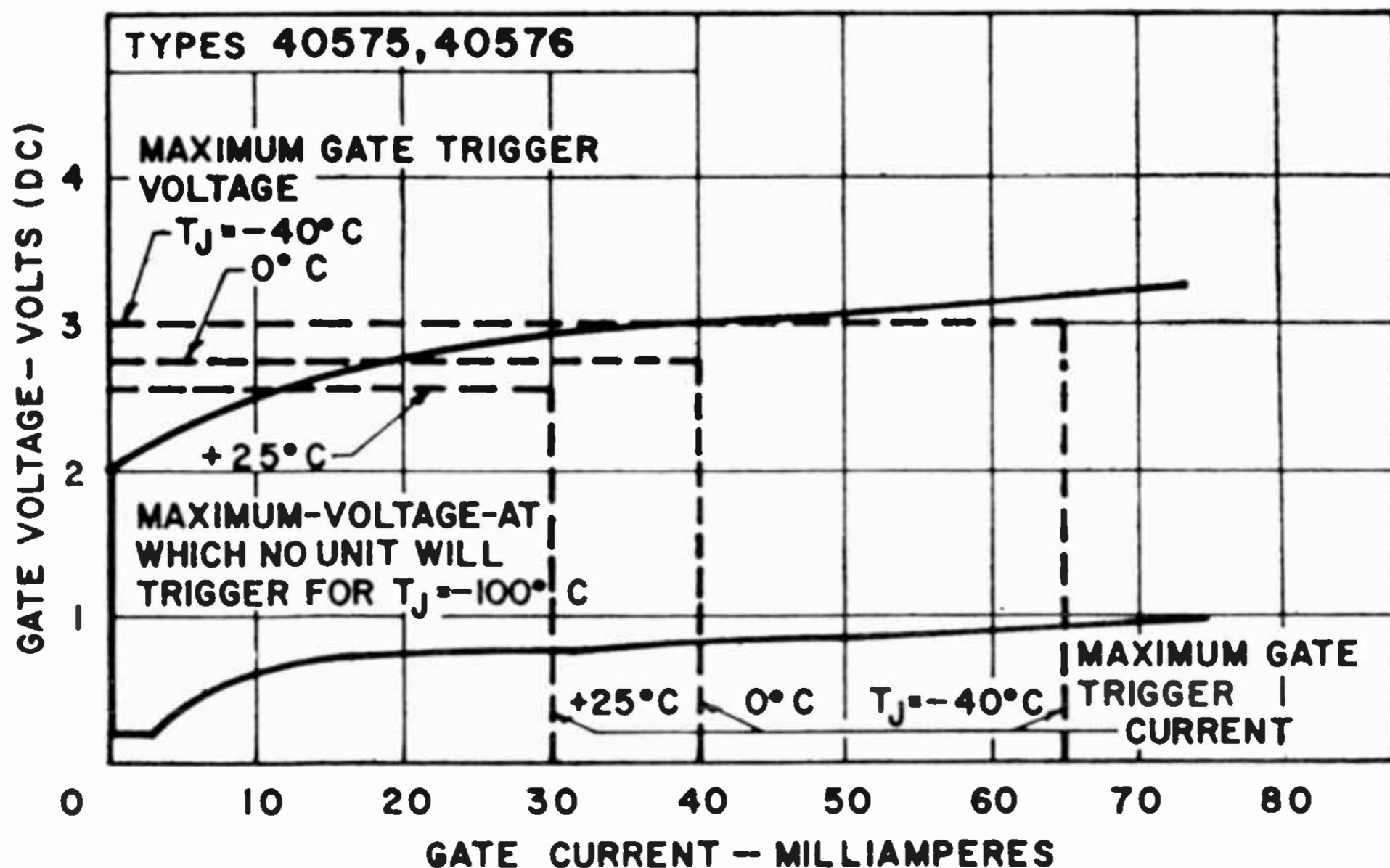
**GATE CHARACTERISTICS
(I⁻ AND III⁺)**



**CONDUCTION RATING CHART
(CASE TEMPERATURE)**



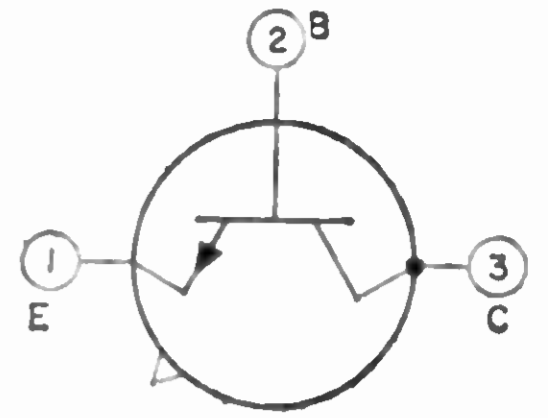
**GATE CHARACTERISTICS
(I⁺ AND III⁻)**



40577

POWER TRANSISTOR

Si n-p-n "overlay" triple-diffused type is subjected to special preconditioning tests for high-reliability operation in high-power vhf applications in military and industrial equipment. JEDEC TO-5, Outline No.5. This type is a high-reliability version of type 2N3118.



MAXIMUM RATINGS

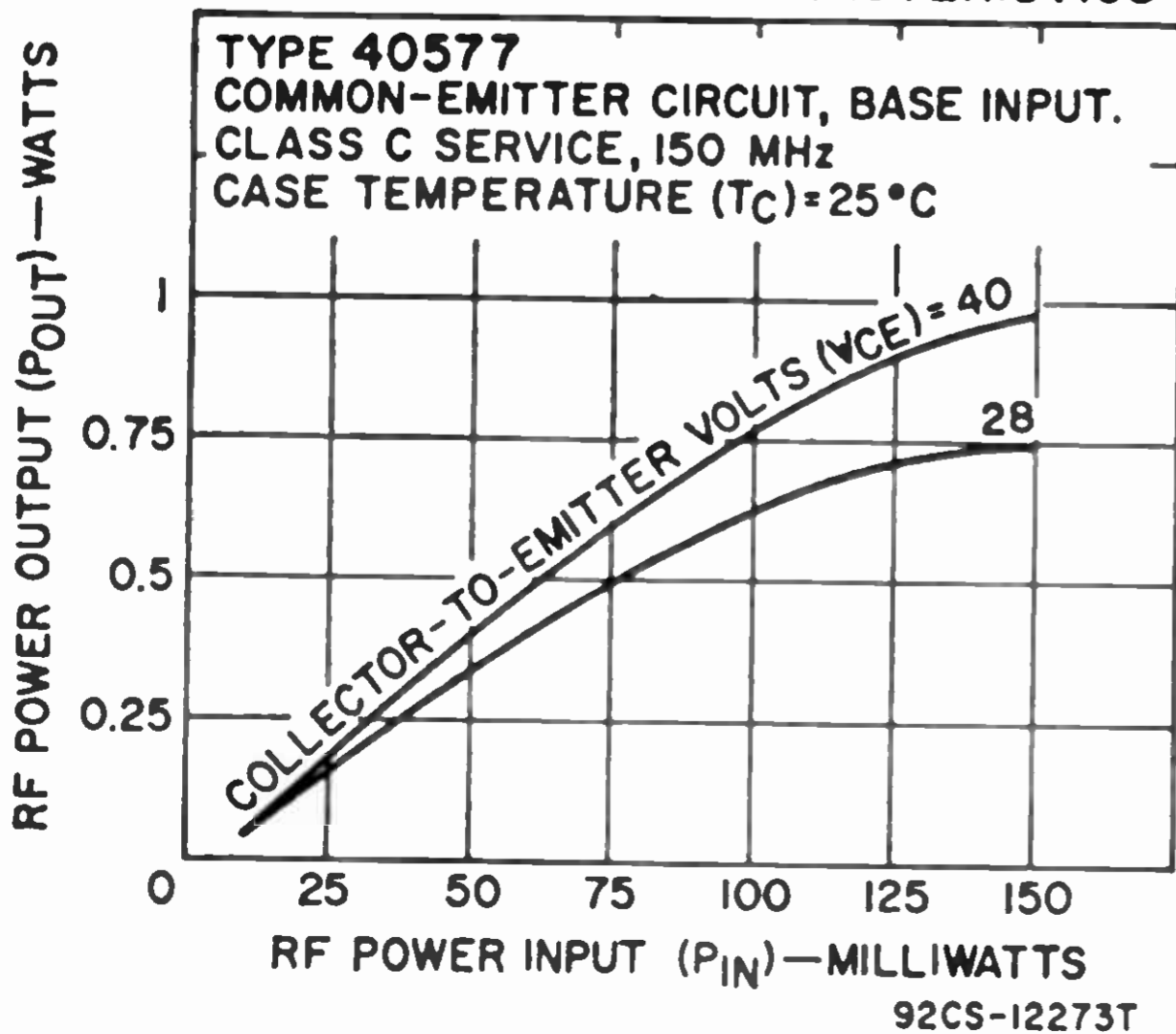
Collector-to-Emitter Voltage:

$V_{BE} = -1.5$ V	V_{CEV}	85	V
Base open	V_{CEO}	60	V
Emitter-to-Base Voltage	V_{EBO}	4	V
Collector Current	I_C	0.5	A
Transistor Dissipation:			
T_c up to 25°C	P_T	3	W
T_A up to 25°C	P_T	5	W
T_c above 25°C			See curve page 300
Temperature Range:			
Operating (Junction)	T_J (opr)	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	230	°C

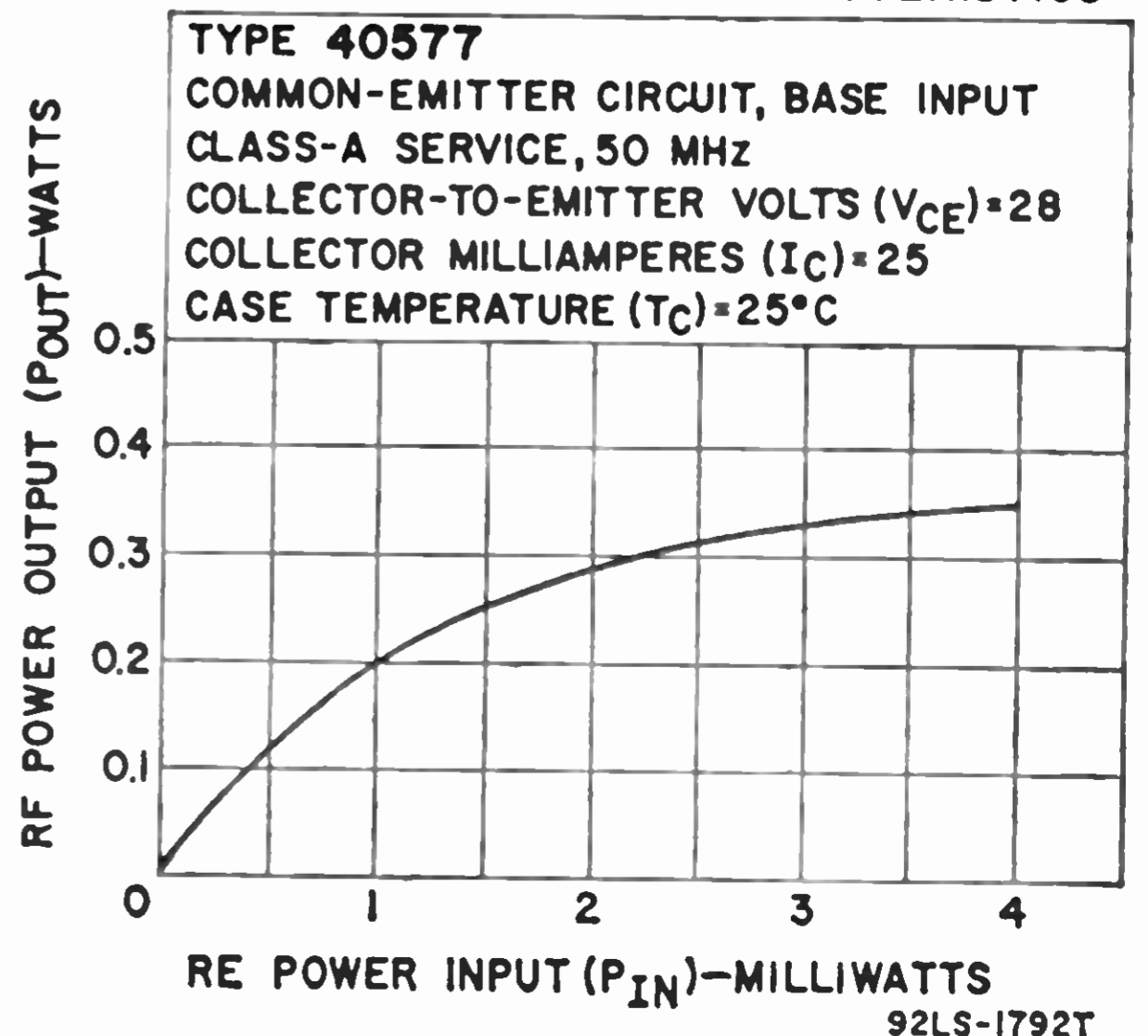
CHARACTERISTICS (At case temperature = 25°C)

Emitter-to-Base Breakdown Voltage ($I_E = 0.1$ mA, $I_C = 0$)	$V_{(BR)EBO}$	4 min	V
Collector-to-Emitter Breakdown Sustaining Voltage ($I_C = 10$ mA, $I_B = 0$, $t_P = 300$ μ s, $df < 1.8\%$)	$V_{(BR)CEO}$ (sus)	60 min	V
Reverse Collector-to-Emitter Breakdown Voltage ($V_{BE} = 1.5$ V, $I_C = 0.1$ mA)	$V_{(BR)CEX}$	85 min	V
Collector-Cutoff Current:			
$V_{CB} = 30$ V, $I_E = 0$, $T_A = 25^\circ$ C	I_{CBO}	10 max	nA
$V_{CB} = 30$ V, $I_E = 0$, $T_A = 150^\circ$ C	I_{CBO}	5 max	μ A
Output Capacitance ($V_{CB} = 28$ V, $I_C = 0$, $f = 1$ MHz)	C_{obo}	6 max	pF
$r_{bb'}$ $C_{b'c}$ Product ($V_{CE} = 28$ V, $I_C = 25$ mA, $f = 50$ MHz)	$r_{bb'}$ $C_{b'c}$	60 max	ps
Pulsed Static Forward-Current Transfer Ratio: ($V_{CE} = 5$ V, $I_C = 100$ mA, $t_P = 300$ μ s, $df < 1.8\%$)	h_{FE} (pulsed)	50 to 275	
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 28$ V, $I_C = 25$ mA, $f = 50$ MHz)	h_{fe}	5 min	
Small-Signal Short-Circuit Input Impedance Real Part ($V_{CE} = 28$ V, $I_C = 25$ mA, $f = 50$ MHz)	R_e (h_{ie})	25 to 75	Ω
Small-Signal Short-Circuit Output Impedance Real Part ($V_{CE} = 28$ V, $I_C = 25$ mA, $f = 50$ MHz)	$\frac{1}{Y_{22}}$ (real)	500 to 1000	
Power Output, Class C Service (with heat sink):			
$V_{CE} = 28$ V, $P_{in} = 0.1$ W, $f = 50$ MHz	P_{oe}	1 min	W
$V_{CE} = 28$ V, $P_{in} = 0.1$ W, $f = 150$ MHz	P_{oe}	0.4 min	W
Power Gain, Class A Service (with heat sink) ($V_{CE} = 28$ V, $I_C = 25$ mA, $P_{out} = 0.2$ W, $f = 50$ MHz)	G_{pe}	18 min	dB

TYPICAL LARGE-SIGNAL CLASS C RF POWER-OUTPUT CHARACTERISTICS

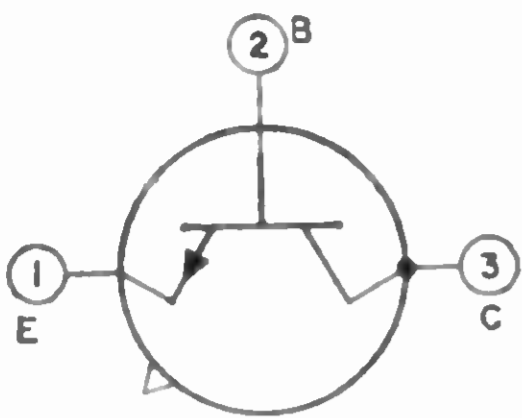


TYPICAL OPERATION CHARACTERISTICS



UHF TRANSISTOR

40578



Si n-p-n "overlay" epitaxial planar type subjected to special preconditioning tests for high-reliability, class A, B, and C amplifier, frequency multiplier, or oscillator operation, driver or pre-driver stages, vhf-uhf applications in space, military, and industrial communications equipment. JEDEC TO-39, Outline No.15. This

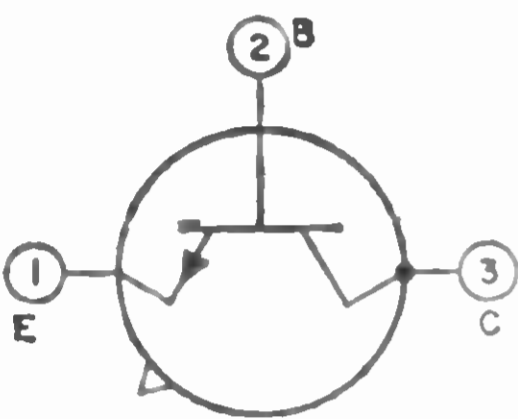
type is identical to type 2N3866 except for the following item:

CHARACTERISTICS (At case temperature = 25°C)

Collector-Cutoff Current ($V_{CE} = 28 \text{ V}, I_B = 0$)	I_{CEO}	100 max	nA
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POWER TRANSISTOR

40581



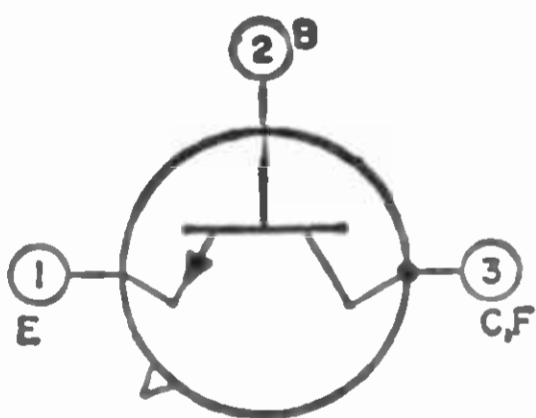
Si n-p-n triple-diffused planar type used for power-amplifier applications in conjunction with transistor types 40080 (oscillator), and 40081 (driver), in a 5-watt, 27-MHz citizens-band transmitter. JEDEC TO-39, Outline No.15. This type is identical to type 40082 except for the following item:

CHARACTERISTICS (At case temperature = 25°C)

RF Power Output ($V_{CC} = 12 \text{ V}, I_C = 415 \text{ mA}, P_{IE} = 350 \text{ mW}, f = 27 \text{ MHz}$)	P_{OE}	3.5 min	W
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POWER TRANSISTOR

40582



Si n-p-n triple-diffused planar type used for power-amplifier applications in conjunction with transistor types 40080 (oscillator), and 40081 (driver), in a 5-watt, 27-MHz citizens-band transmitter. JEDEC TO-39, Outline No.6. See Mounting Hardware for desired arrangement. This type is identical with type 40082 except for the following items:

MAXIMUM RATINGS

Transistor Dissipation T_c up to 25°C	P_T	10	W
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CHARACTERISTICS (At case temperature = 25°C)

RF Power Output ($V_{CC} = 12 \text{ V}, I_C = 415 \text{ mA}, f = 27 \text{ MHz}, P_{IE} = 350 \text{ mW}$)	P_{OE}	3.5 min	W
Thermal Resistance, Junction-to-Case	θ_{J-C}	17.5	°C/W

DIAC

40583



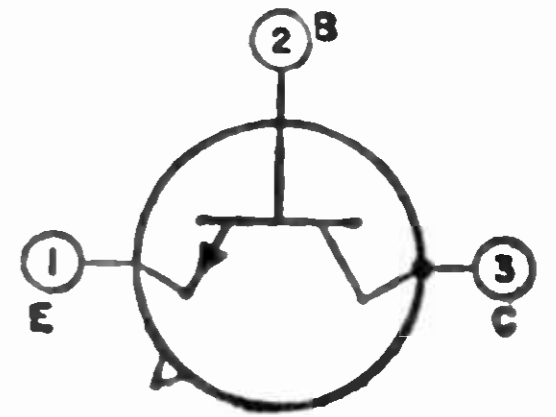
Si all-diffused three-layer trigger diode type used for triac phase-control circuits for lamp dimming, universal-motor speed, and heat controls. JEDEC DO-26, Outline No.66. This type is identical with type 1N5411 except for the following item:

CHARACTERISTICS (At case temperature = 25°C)

Breakover Voltage, Forward or Reverse	$V_{(BO)}$	27 to 37	V
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40594 POWER TRANSISTOR

Si n-p-n type used for driver applications in high-fidelity amplifier circuits. This type and type 40495 form a complementary pair of driver transistors suitable for quasi-complementary-symmetry circuits. JEDEC TO-5, Outline No.5.



MAXIMUM RATINGS

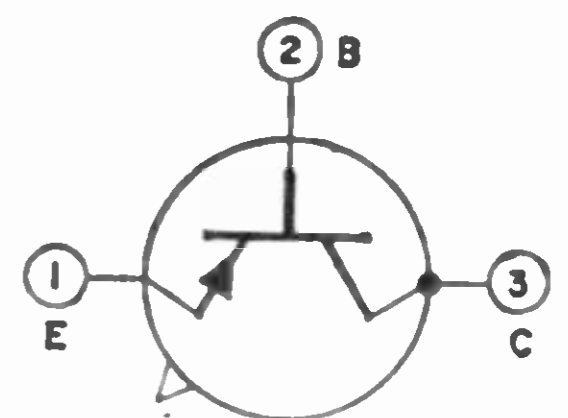
Collector-to-Emitter Sustaining Voltage $R_{BE} = 100 \Omega$	$V_{CER(SUS)}$	95	V
Emitter-to-Base Voltage	V_{EBO}	4	V
Collector Current	I_C	2	A
Base Current	I_B	1	A
Transistor Dissipation:			
$T_C = 25^\circ C$	P_T	10	W
$T_A = 25^\circ C$	P_T	1.2	W
Temperature Range:			
Operating	$T(opr)$	-65 to 200	$^\circ C$
Storage	T_{STG}	-65 to 200	$^\circ C$

CHARACTERISTICS

Collector-to-Emitter Sustaining Voltage ($I_C = 100 \text{ mA}$, $R_{BE} = 100 \Omega$)	$V_{CER(SUS)}$	95 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 300 \text{ mA}$, $I_B = 30 \text{ mA}$)	$V_{CE(sat)}$	0.8 max	V
Base-to-Emitter Voltage ($V_{CE} = 4 \text{ V}$, $I_C = 300 \text{ mA}$)	V_{BE}	1.4 max	V
Collector-Cutoff Current ($V_{CE} = 85 \text{ V}$, $R_{BE} = 100 \Omega$)	I_{CER}	10 max	μA
Emitter-Cutoff Current ($V_{EB} = 4 \text{ V}$)	I_{EBO}	0.1 max	μA
Static Forward Current Transfer Ratio ($V_{CE} = 4 \text{ V}$, $I_C = 300 \text{ mA}$)	h_{FE}	70 to 350	

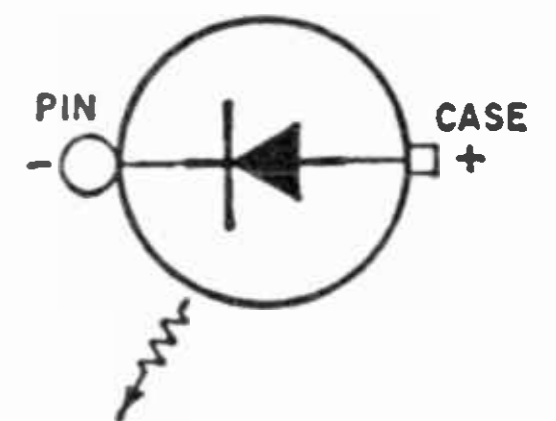
40595 POWER TRANSISTOR

Si p-n-p type used for driver applications in high-fidelity amplifier circuits. This type and type 40495 form a complementary pair of driver transistors suitable for quasi-complementary-symmetry circuits. JEDEC TO-5, Outline No.5. This type is electrically identical with type 40594 except for the reversal of all polarity signs.



40598A EMITTING DIODE

GaAs high-frequency type used for continuous or pulse applications in military, industrial, and commercial equipment. Outline No.67.



MAXIMUM RATINGS

Peak Forward Current	I_{FM}	1	A
Average Forward Current:			
T_C from -73 to $50^\circ C$	$I_{F(AV)}$	50	mA
T_C from 50 to $75^\circ C$	$I_{F(AV)}$	See Rating Chart	
Peak Reverse Voltage	V_{RM}	2	V
T_C from -73 to $50^\circ C$	$P_{IN(AV)}$	90	
T_C from 50 to $75^\circ C$	$P_{IN(AV)}$	See Rating Chart	
Temperature:			
Operating	T_C	-73 to 75	$^\circ C$
Storage	T_{STG}	-72 to 100	$^\circ C$
During Soldering (5 s)		130	$^\circ C$

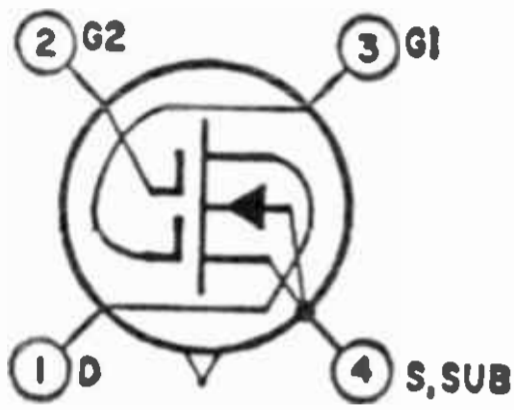
CHARACTERISTICS (At case temperature = $27^\circ C$)

DC Forward Voltage Drop ($I_F = 10 \text{ mA}$)	V_F	1.2 typ; 1.5 max	V
DC Forward Voltage Drop ($I_F = 50 \text{ mA}$)	V_F	1.4 typ; 1.8 max	V

CHARACTERISTICS (cont'd)

Peak Reverse Current ($V_R = 2\text{ V}$)	I_{RM}	10 max	μA
Continuous Service ($I_F = 50\text{ mA}$):			
DC Forward Voltage	V_F	1.4	V
Radiant Power Output*	P_O	1 min; 1.6 typ	mW
Radiant Power Output per Ampere	P_O/A	20 min; 32 typ	mW/A
Power Efficiency ($P_O/V_F I_F$)	η	1.1 min; 2.3 typ	%
Pulse Service:			
Peak Radiant Power Output ($I_F = 1\text{ A}$, $t_p = 2\ \mu\text{s}$, $df = 1\%$, pulse rep. rate = 500 p/s)	P_{OM}	24	mW
Radiation Characteristics, Continuous or Pulse Service:			
Wavelength at Peak of Emitted Spectrum	λ	9100 to 9500	$^\circ\text{A}$
Line Width at Half-Power Points		500	$^\circ\text{A}$
Half-Angle Beam Spread: At Half-Power Point	α	15 degrees	
At 20% Power Point	α	30 degrees	

* Radiant Power Output is derived by measuring the short-circuit current in a calibrated silicon photovoltaic cell positioned close to the emitter to collect the total infrared emission.



FIELD-EFFECT TRANSISTOR 40600

Si dual insulated-gate field-effect (MOS) n-channel depletion type used in rf-amplifier applications in vhf television receivers and other types of commercial equipment operating at frequencies up to approximately 250 MHz. JEDEC TO-72, Outline No.28. For typical drain characteristics and typical forward transconductance curves, refer to type 3N140.

MAXIMUM RATINGS

Drain-to-Source Voltage	V_{DS}	0 to 20	V
Gate No.1-to-Source Voltage:			
Continuous (dc)	V_{G1S}	-8 to 1	V
Peak (ac)	V_{G1S}	-8 to 20	V
Gate No.2-to-Source Voltage:			
Continuous (dc)	V_{G2S}	-8 to (0.4 V_{DS})	V
Peak (ac)	V_{G2S}	-8 to 20	V
Drain-to-Gate 1.o. 1 Voltage	V_{DG1}	20	V
Drain-to-Gate No. 2 Voltage	V_{DG2}	20	V
Drain Current ($t_p \leq 20\text{ ms}$, $df \leq 0.15$)	I_D (pulsed)	50	mA
Transistor Dissipation:			
T_A up to 25 $^\circ\text{C}$	P_T	400	mW
T_A above 25 $^\circ\text{C}$	P_T Derate linearly at 2.67		mW/ $^\circ\text{C}$
Temperature Range:			
Operating	T (opr)	-65 to 175	$^\circ\text{C}$
Storage	T_{STG}	-65 to 175	$^\circ\text{C}$
Lead-Soldering Temperature (10 s max)	T_L	265	$^\circ\text{C}$

CHARACTERISTICS

Gate-No.1-to-Source Voltage ($V_{DS} = 15\text{ V}$, $V_{G2S} = 4\text{ V}$, $I_D = 200\ \mu\text{A}$)	V_{G1S} (off)	-2	V
Gate-No.2-to-Source Cutoff Voltage ($V_{DS} = 15\text{ V}$, $V_{G1S} = 0$, $I_D = 200\ \mu\text{A}$)	V_{G2S} (off)	-2	V
Gate-No.1 Leakage Current ($V_{G1S} = -20\text{ V}$, $V_{G2S} = 0$, $V_{DS} = 0$)	I_{G1SS}	1 max	nA
Gate-No.2 Leakage Current ($V_{G2S} = -20\text{ V}$, $V_{G1S} = 0$, $V_{DS} = 0$)	I_{G2SS}	1 max	nA
Drain Current ($V_{DS} = 13\text{ V}$, $V_{G2S} = 4\text{ V}$, $V_{G1S} = 0$)	I_{DSS}	18	mA
Forward Transconductance ($V_{DS} = 13\text{ V}$, $V_{G2S} = 4\text{ V}$, $I_D = 10\text{ mA}$, $f = 1\text{ kHz}$)	g_{fs}	10000	μmhos
Small-Signal Reverse Transfer Capacitance, Drain to Gate No.1 ($V_{DS} = 13\text{ V}$, $V_{G2S} = 4\text{ V}$, $I_D = 10\text{ mA}$, $f = 1\text{ MHz}$)	C_{rss}	0.02 typ; 0.03 max	pF
Output Capacitance ($V_{DS} = 13\text{ V}$, $V_{G2S} = 4\text{ V}$, $I_D = 10\text{ mA}$, $f = 200\text{ MHz}$)	C_{oss}	2.2	pF
Input Capacitance ($V_{DS} = 13\text{ V}$, $V_{G2S} = 4\text{ V}$, $I_D = 10\text{ mA}$, $f = 200\text{ MHz}$)	C_{iss}	5.5	pF
Input Resistance ($V_{DS} = 13\text{ V}$, $V_{G2S} = 4\text{ V}$, $I_D = 10\text{ mA}$, $f = 200\text{ MHz}$)	r_{iss}	1.2	k Ω
Output Resistance ($V_{DS} = 13\text{ V}$, $V_{G2S} = 4\text{ V}$, $I_D = 10\text{ mA}$, $f = 200\text{ MHz}$)	r_{oss}	2.8	k Ω

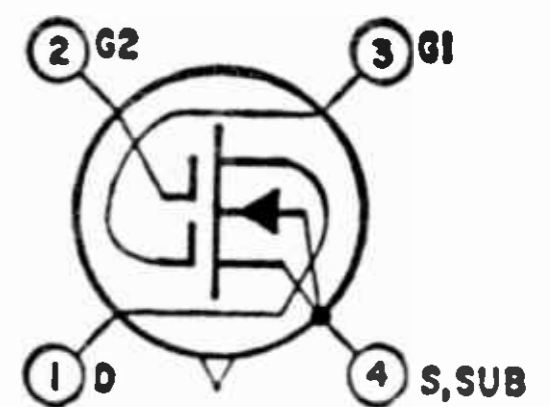
CHARACTERISTICS (cont'd)

Magnitude of Forward Transadmittance ($V_{DS} = 13$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, $f = 200$ MHz)	$ Y_{fs} $	11000	μ mhos
Phase Angle of Forward Transadmittance ($V_{DS} = 13$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, $f = 200$ MHz)	$\angle \theta$	-46	degrees
Maximum Available Power Gain ($V_{DS} = 13$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, $f = 200$ MHz)	MAG	20	dB
Maximum Usable Power Gain, Unneutralized ($V_{DS} = 13$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, $f = 200$ MHz)	MUG	20 [^]	dB
Power Gain ($V_{DS} = 13$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, $f = 200$ MHz)	G_{PS}	17.5 [†]	dB
Noise Figure ($V_{DS} = 13$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, $f = 200$ MHz)	NF	5 [†] max	dB

[^]Limited by practical design considerations.
[†]This characteristic does not apply to ty 40602.

40601 FIELD-EFFECT TRANSISTOR

Si dual insulated-gate field-effect (MOS) n-channel depletion type used in mixer applications in vhf television receivers and other types of commercial equipment operating at frequencies up to approximately 250 MHz. JEDEC TO-72, Outline No.28. The maximum ratings for this type are identical with type 40600.

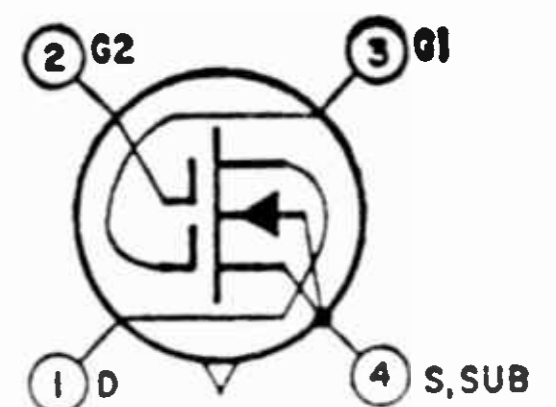


CHARACTERISTICS

Gate-No.1-to-Source Cutoff Voltage ($V_{DS} = 15$ V, $V_{G2S} = 4$ V, $I_D = 200$ μ A)	$V_{G1S}(\text{off})$	-2	V
Gate-No.2-to-Source Cutoff Voltage ($V_{DS} = 15$ V, $V_{G2S} = 4$ V, $I_D = 200$ μ A)	$V_{G2S}(\text{off})$	-2	V
Gate-No.1 Leakage Current ($V_{G1S} = -20$ V, $V_{G2S} = 0$, $V_{DS} = 0$)	I_{G1SS}	1 max	nA
Gate-No.2 Leakage Current ($V_{G2S} = -20$ V, $V_{G1S} = 0$, $V_{DS} = 0$)	I_{G2SS}	1 max	nA
Drain Current ($V_{DS} = 13$ V, $V_{G2S} = 4$ V, $V_{G1S} = 0$)	I_{DSS}	18	mA
Forward Transconductance ($V_{DS} = 13$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, $f = 1$ kHz)	g_{fs}	10000	μ mhos
The following test conditions apply to all remaining characteristics, unless otherwise specified: Local-oscillator injection voltage on gate No.2 = 750 mV, $V_{DS} = 15$ V, $V_{G2S} = 0.6$ V, $V_{G1S} = 0.75$ V, $f = 200$ MHz.			
Small-Signal Reverse Transfer Capacitance, Drain-to-Gate No.1 ($f = 1$ MHz)	C_{rss}	0.02 typ; 0.03 max	pF
Output Capacitance ($f = 44$ MHz)	C_{oss}	2.2	pF
Input Capacitance	C_{iss}	5.5	pF
Input Resistance	r_{iss}	1.2	k Ω
Output Resistance ($f = 44$ MHz)	r_{oss}	12	k Ω
Magnitude of Forward Conversion Transadmittance	$ Y_{fs(c)} $	2700	μ mhos
Maximum Available Conversion Gain	MAG _c	14	dB

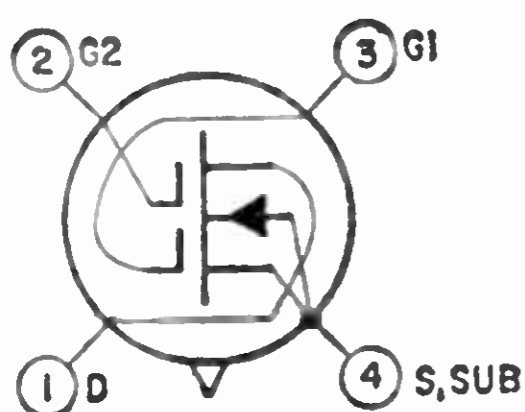
40602 FIELD-EFFECT TRANSISTOR

Si dual insulated-gate field-effect (MOS) n-channel depletion type used in first-if amplifier applications in vhf television receivers and other types of commercial equipment operating at frequencies up to approximately 250 MHz. JEDEC TO-72, Outline No.28. This type is identical with type 40600 except for the following items:



CHARACTERISTICS

Input Resistance	r_{iss}	10	k Ω
Output Resistance	r_{oss}	12	k Ω
Phase Angle of Forward Transadmittance	$\angle \theta$	-11	degrees
Maximum Available Power Gain	MAG	35	dB
Maximum Usable Power Gain, Unneutralized:			
For 1 stage	MUG	28	dB
For 2 stages	MUG	26	dB
For 3 stages	MUG	24	dB



FIELD-EFFECT TRANSISTOR 40603

Si dual insulated-gate field-effect (MOS) n-channel depletion type used in rf amplifier applications in FM tuners and other commercial equipment operating at frequencies up to approximately 150 MHz. JEDEC TO-72, Outline No.28. For typical forward transconductance

curves, refer to type 3N140.

MAXIMUM RATINGS

Drain-to-Source Voltage	V_{DS}	0 to 20	V
Gate-No.1-to-Source Voltage:			
Continuous (dc)	V_{G1S}	-8 to 1	V
Peak (ac)	V_{G1S}	-8 to 20	V
Gate-No.2-to-Source Voltage:			
Continuous (dc)	V_{G2S}	-8 to (0.4 V_{DS})	V
Peak (ac)	V_{G2S}	-8 to 20	V
Drain-to-Gate-No.1 Voltage	V_{G1S}	20	V
Drain-to-Gate-No.2 Voltage	V_{G2S}	20	V
Drain Current ($t_P \leq 20$ ms, $df \leq 0.15$)	I_D (pulsed)	50	mA
Transistor Dissipation:			
T_A up to 25°C	P_T	400	mW
T_A above 25°C	P_T	Derate linearly at 2.67	mW/°C
Temperature Range:			
Operating	T (opr)	-65 to 175	°C
Storage	T_{STG}	-65 to 175	°C
Lead-Soldering Temperature (10 s max)	T_L	265	°C

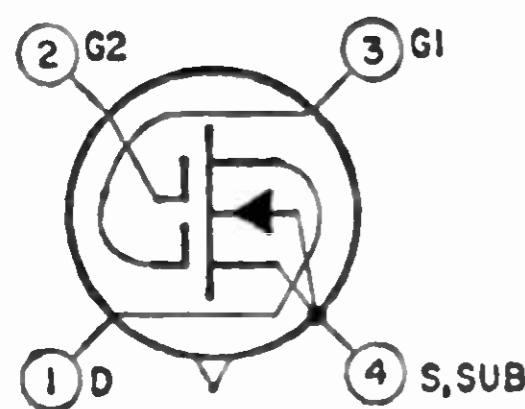
CHARACTERISTICS

Gate-No.1-to-Source Cutoff Voltage ($V_{DS} = 15$ V, $V_{G2S} = 4$ V, $I_D = 200$ μ A)	V_{G1S} (off)	-2	V
Gate-No.2-to-Source Cutoff Voltage ($V_{DS} = 15$ V, $V_{G1S} = 0$, $I_D = 200$ μ A)	V_{G2S} (off)	-2	V
Gate-No.1 Leakage Current ($V_{G1S} = -20$ V, $V_{G2S} = 0$, $V_{DS} = 0$)	I_{G1SS}	1 max	nA
Gate-No.2 Leakage Current ($V_{G2S} = -20$ V, $V_{G1S} = 0$, $V_{DS} = 0$)	I_{G2SS}	1 max	nA
Zero-Bias-Voltage Drain Current ($V_{G2S} = 4$ V, $V_{G1S} = 0$, $V_{DS} = 13$ V)	I_{DSS}	18	mA
Small-Signal Reverse Transfer Capacitance, Drain-to-Gate-No.1 ($V_{DS} = 13$ V, $I_D = 10$ mA, $V_{G2S} = 4$ V, $f = 1$ MHz)	C_{rss}	0.02 typ; 0.03 max	pF
Input Capacitance ($V_{DS} = 13$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, $f = 1$ MHz)	C_{iss}	5.5	pF
Output Capacitance ($V_{DS} = 13$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, $f = 100$ MHz)	C_{oss}	21	pF
Input Resistance ($V_{DS} = 13$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, $f = 100$ MHz)	r_{iss}	3.5	k Ω
Output Resistance ($V_{DS} = 13$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, $f = 100$ MHz)	r_{oss}	4	k Ω
Forward Transconductance ($V_{DS} = 13$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, $f = 1$ kHz)	g_{fs}	10000 [•]	μ mhos
Maximum Available Power Gain ($V_{DS} = 13$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, $f = 100$ MHz)	MAG	26	dB
Maximum Usable Power Gain, Unneutralized ($V_{DS} = 13$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, $f = 100$ MHz)	MUG	25 [▲]	dB
Noise Figure ($V_{DS} = 13$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, $f = 100$ MHz)	NF	2.5 [•]	dB

[▲]Limited by practical design considerations.

[•]This characteristic does not apply to type 40604.

FIELD-EFFECT TRANSISTOR 40604



Si dual insulated-gate field-effect (MOS) n-channel depletion type used in mixer applications in FM tuners and other commercial equipment operating at frequencies up to approximately 150 MHz. JEDEC TO-72, Outline No.28. This type is identical with type 40603 except for the following items:

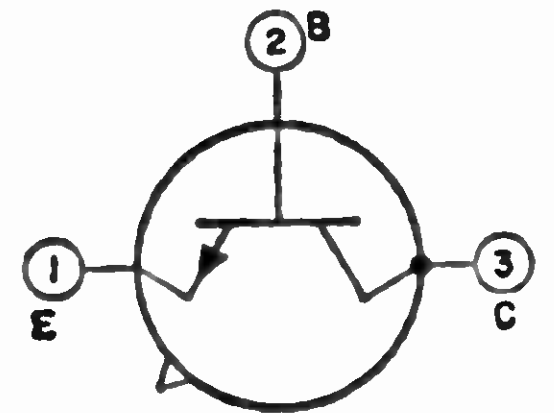
CHARACTERISTICS

Output Capacitance ($V_{DS} = 13$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, $f = 100$ MHz)	C_{oss}	2.3	pF
Output Resistance ($V_{DS} = 13$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, $f = 10.7$ MHz)	r_{oss}	20	k Ω
Conversion Transconductance ($V_{DS} = 13$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, $f = 1$ kHz)	$g_{fs}(c)$	2800	μ mhos
Maximum Available Power Gain ($V_{DS} = 13$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, $f = 100$ MHz, $f_{out} = 10.7$ MHz)	MAG	21	dB

40608

POWER TRANSISTOR

Si n-p-n "overlay" epitaxial type used for operation as a class A wide-band power amplifier in vhf circuits. JEDEC TO-39, Outline No.15.



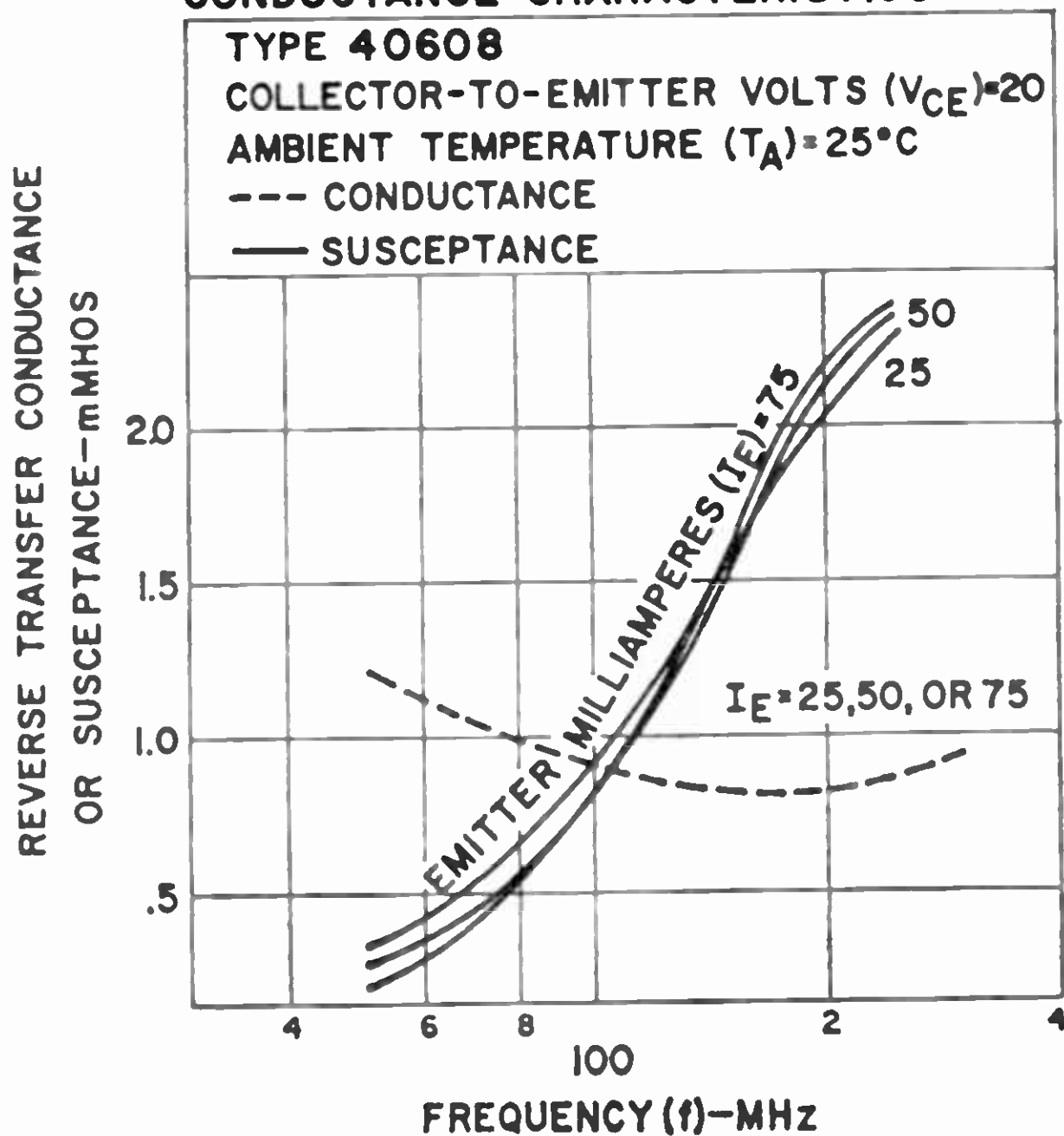
MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	40	V
Collector-to-Emitter Voltage ($V_{BE} = 100$ Ω)	V_{CER}	40	V
Emitter-to-Base Voltage	V_{EBO}	2	V
Collector Current	I_C	0.4	A
Transistor Dissipation:			
T_c up to 25°C	P_T	3.5	W
T_c above 25°C	P_T	See curve page 300	
Temperature Range:			
Operating (Junction)	$T_J(opr)$	-65 to 200	°C
Storage	T_{STG}	-65 to 200	°C
Lead-Soldering Temperature (10 s max)	T_L	230	°C

CHARACTERISTICS (At case temperature = 25°C)

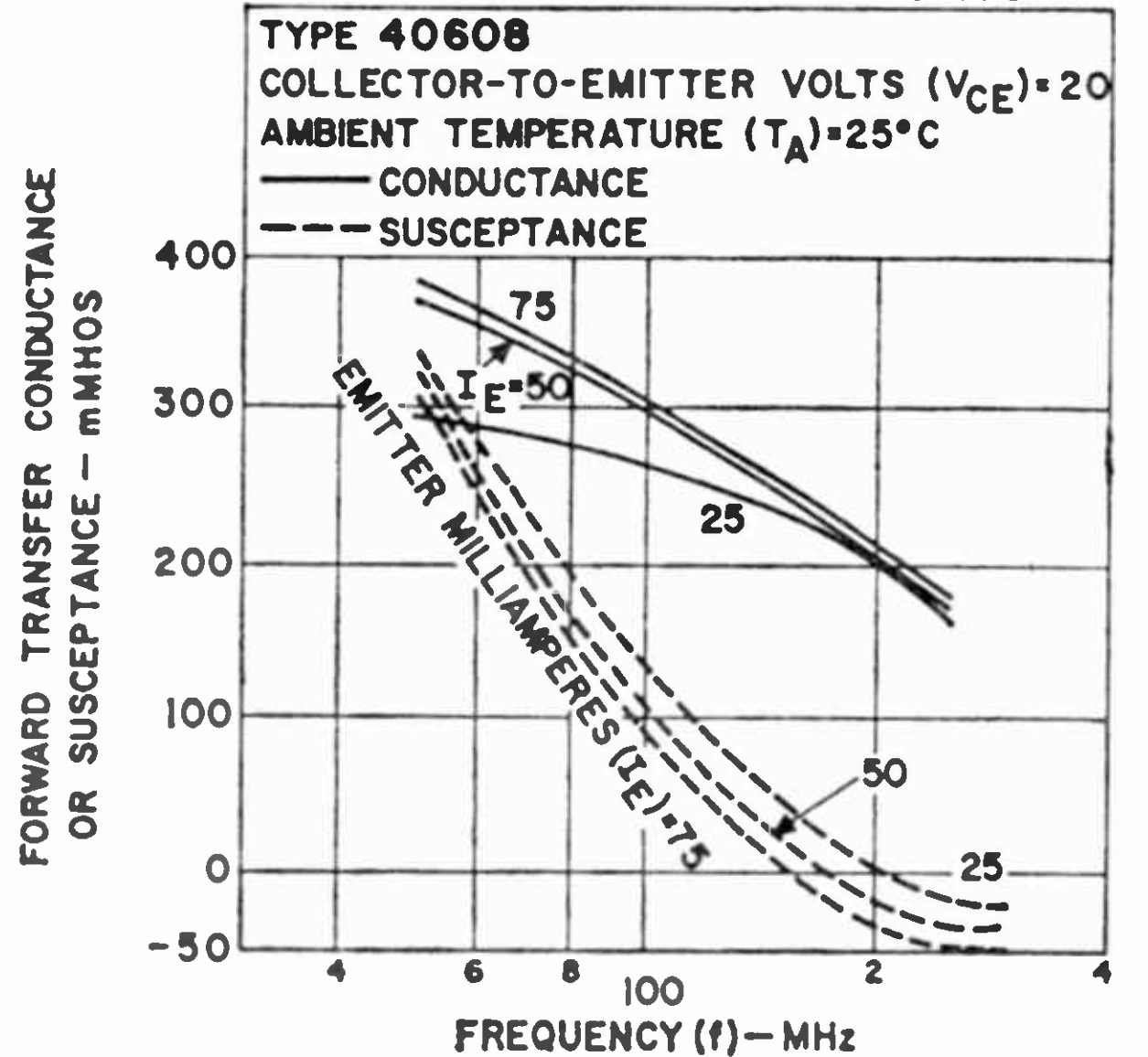
Collector-to-Base Breakdown Voltage ($I_C = 0.1$ mA, $I_E = 0$)	$V_{(BR)CBO}$	40 min	V
Emitter-to-Base Breakdown Voltage ($I_E = 0.1$ mA, $I_C = 0$)	$V_{(BR)EBO}$	2 min	V
Collector-to-Emitter Sustaining Voltage ($I_C = 50$ mA, $R_{BE} = 100$ Ω pulsed through inductor $L = 20$ mH, $df = 50\%$)	$V_{CER}(sus)$	40 min	V
Collector-to-Emitter Saturation Voltage ($I_B = 10$ mA, $I_C = 50$ mA)	$V_{CE}(sat)$	1 max	V

TYPICAL REVERSE-TRANSFER CONDUCTANCE CHARACTERISTICS



92LS-1238T2

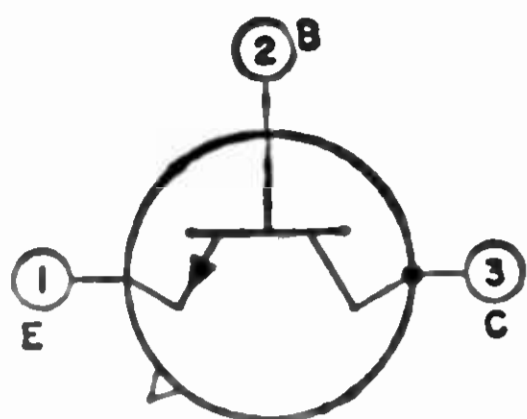
TYPICAL FORWARD-TRANSFER CONDUCTANCE CHARACTERISTICS



92LS-1234T2

CHARACTERISTICS (cont'd)

Collector-Cutoff Current ($V_{CE} = 20\text{ V}$, $I_B = 0$)	I_{CEO}	100 max	μA
Collector-to-Base Capacitance ($V_{CB} = 30\text{ V}$, $I_E = 0$, $f = 1\text{ MHz}$)	C_{obo}	3 max	pF
Gain-Bandwidth Product ($V_{CE} = 15\text{ V}$, $I_C = 50\text{ mA}$)	f_T	700 min	MHz
Static Forward-Current Transfer Ratio ($V_{CE} = 15\text{ V}$, $I_C = 50\text{ mA}$)	h_{FE}	35 to 120	
Voltage Gain ($V_{CE} = 15\text{ V}$, $I_C = 50\text{ mA}$)	VG	11 min	dB
Cross Modulation at 46 dB mV ($V_{CE} = 15\text{ V}$, $I_C = 50\text{ mA}$, R_G and $R_L = 75\ \Omega$)	CM	-57	dB



POWER TRANSISTOR

40611

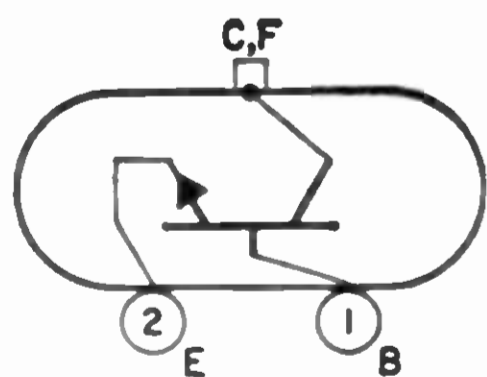
Si n-p-n type used for driver applications in high-fidelity amplifier circuits suitable for complementary-symmetry circuits. JEDEC TO-5, Outline No.5.

MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage	$V_{CEO}(\text{sus})$	25	V
Emitter-to-Base Voltage	V_{EBO}	2.5	V
Collector Current	I_C	0.7	A
Base Current	I_B	0.2	A
Transistor Dissipation:			
$T_C = 25^\circ\text{C}$	P_T	5	W
$T_A = 25^\circ\text{C}$	P_T	1	W
Temperature Range:			
Operating	T(opr)	-65 to 200	$^\circ\text{C}$
Storage	T_{STG}	-65 to 200	$^\circ\text{C}$

CHARACTERISTICS

Collector-to-Emitter Sustaining Voltage ($I_C = 100\text{ mA}$)	$V_{CEO}(\text{sus})$	25 min	V
Collector-Cutoff Current ($V_{CB} = 15\text{ V}$)	I_{CBO}	0.5 max	μA
Collector-Cutoff Current ($V_{EB} = 2.5\text{ V}$)	I_{EBO}	1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 4\text{ V}$, $I_C = 59\text{ mA}$)	h_{FE}	70 to 500	



POWER TRANSISTOR

40612

Ge p-n-p type used for output stages in high-fidelity amplifier circuits suitable for complementary-symmetry circuits. JEDEC TO-3, Outline No.2.

MAXIMUM RATINGS

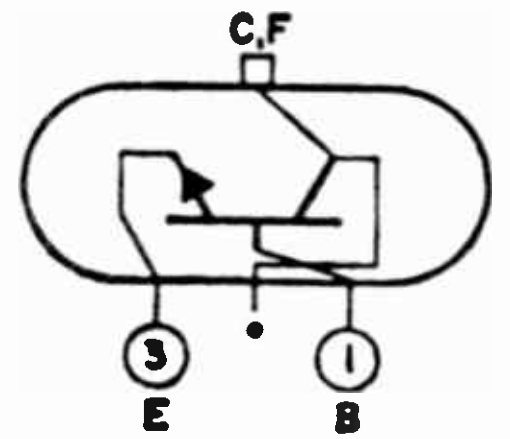
Collector-to-Emitter Sustaining Voltage $R_{BE} = 68\ \Omega$	$V_{CER}(\text{sus})$	-25	V
Emitter-to-Base Voltage	V_{EBO}	-5	V
Collector Current	I_C	-5	A
Base Current	I_B	-1	A
Transistor Dissipation $T_C = 25^\circ\text{C}$	P_T	12.5	W
Temperature Range:			
Operating	T(opr)	-65 to 100	$^\circ\text{C}$
Storage	T_{STG}	-65 to 100	$^\circ\text{C}$

CHARACTERISTICS

Collector-to-Emitter Sustaining Voltage ($I_C = -200\text{ mA}$, $R_{BE} = 68\ \Omega$)	$V_{CER}(\text{sus})$	-25 min	V
Collector-Cutoff Current ($V_{CB} = -30\text{ V}$)	I_{CBO}	-3 max	μA
Emitter-Cutoff Current ($V_{EB} = -5\text{ V}$)	I_{EBO}	-2 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = -2\text{ V}$, $I_C = -1000\text{ mA}$)	h_{FE}	30 to 150	

40613 POWER TRANSISTOR

Si n-p-n type used for output stages in high-fidelity amplifier circuits suitable for complementary-symmetry circuits. This type features a base comprised of a homogeneous-resistivity and molded silicone plastic package with vertical leads. This type fits a standard TO-66 socket. Outline No.52.



MAXIMUM RATINGS

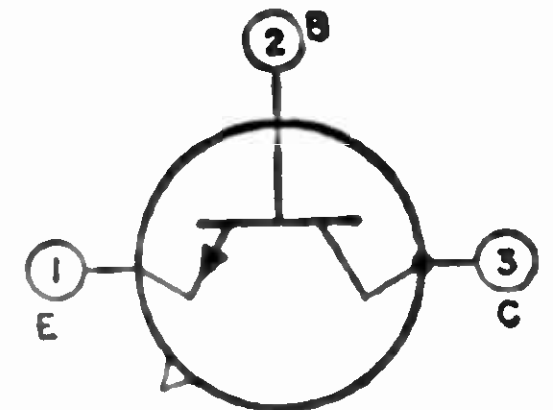
Collector-to-Emitter Sustaining Voltage	$V_{CEO(sus)}$	25	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	4	A
Base Current	I_B	2	A
Transistor Dissipation:			
$T_C = 25^\circ C$	P_T	36	W
$T_A = 25^\circ C$	P_T	1.8	W
Temperature Range:			
Operating	$T(opr)$	-65 to 150	$^\circ C$
Storage	T_{STG}	-65 to 150	$^\circ C$

CHARACTERISTICS

Collector-to-Emitter Sustaining Voltage ($I_C = 100\text{ mA}$)	$V_{CEO(sus)}$	25 min	V
Base-to-Emitter Voltage ($V_{CE} = 4\text{ V}$, $I_C = 1000\text{ mA}$)	V_{BE}	1.3 max	V
Collector-Cutoff Current ($V_{CB} = 25\text{ V}$)	I_{CBO}	2 max	μA
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}	1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 4\text{ V}$, $I_C = 1000\text{ mA}$)	h_{FE}	30 to 120	

40616 POWER TRANSISTOR

Si n-p-n type used for driver applications in high-fidelity amplifier circuits suitable for complementary-symmetry circuits. JEDEC TO-5, Outline No.5.



MAXIMUM RATINGS

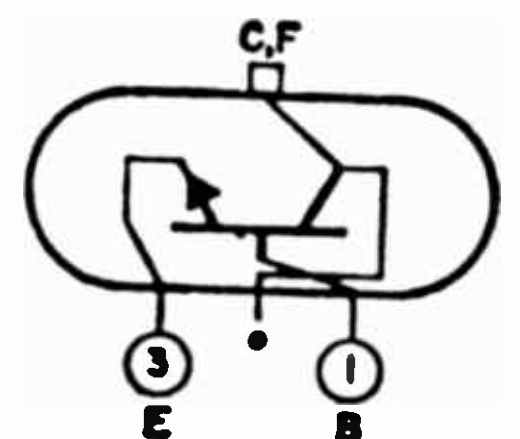
Collector-to-Emitter Sustaining Voltage	$V_{CEO(sus)}$	32	V
Emitter-to-Base Voltage	V_{EBO}	2.5	V
Collector Current	I_C	0.7	A
Base Current	I_B	0.2	A
Transistor Dissipation:			
$T_C = 25^\circ C$	P_T	5	W
$T_A = 25^\circ C$	P_T	1	W
Temperature Range:			
Operating	$T(opr)$	-65 to 200	$^\circ C$
Storage	T_{STG}	-65 to 200	$^\circ C$

CHARACTERISTICS

Collector-to-Emitter Sustaining Voltage ($I_C = 100\text{ mA}$)	$V_{CEO(sus)}$	32 min	V
Collector-Cutoff Current ($V_{CB} = 15\text{ V}$)	I_{CBO}	0.5 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 4\text{ V}$, $I_C = 50\text{ mA}$)	h_{FE}	70 to 500	

40618 POWER TRANSISTOR

Si n-p-n type used for output stages in high-fidelity amplifier circuits suitable for complementary-symmetry circuits. This type features a base comprised of a homogeneous-resistivity and molded silicone plastic package with vertical leads. This type fits a standard TO-66 socket. Outline No.52.



MAXIMUM RATINGS

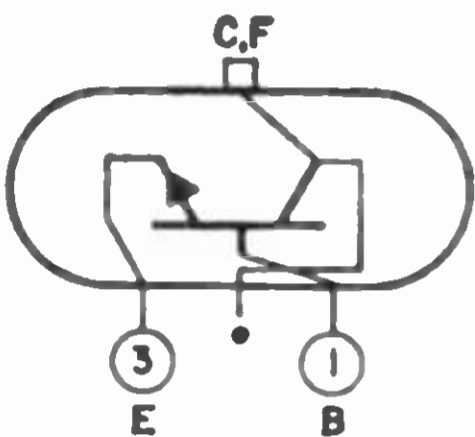
Collector-to-Emitter Sustaining Voltage	$V_{CEO(sus)}$	30	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	4	A
Base Current	I_B	2	A
Transistor Dissipation:			
$T_C = 25^\circ C$	P_T	36	W
$T_A = 25^\circ C$	P_T	1.8	W
Temperature Range:			
Operating	$T(opr)$	-65 to 150	$^\circ C$
Storage	T_{STG}	-65 to 150	$^\circ C$

CHARACTERISTICS

Collector-to-Emitter Sustaining Voltage ($I_C = 100\text{ mA}$)	$V_{CEO(sus)}$	30 min	V
Collector-Cutoff Current ($V_{CB} = 30\text{ V}$)	I_{CBO}	2 max	μA
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}	1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 4\text{ V}, I_C = 1000\text{ mA}$)	h_{FE}	30 to 120	

POWER TRANSISTOR

40621



Si n-p-n type used for output stages in high-fidelity circuits suitable for complementary-symmetry circuits. This type features a base comprised of a homogeneous-resistivity and molded silicone plastic package with vertical leads. This type fits a standard TO-66 socket. Outline No.52.

MAXIMUM RATINGS

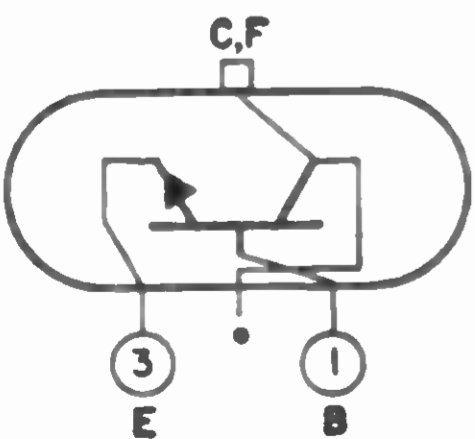
Collector-to-Emitter Sustaining Voltage	$V_{CEO(sus)}$	32	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	4	A
Base Current	I_B	2	A
Transistor Dissipation:			
$T_C = 25^\circ C$	P_T	36	W
$T_A = 25^\circ C$	P_T	1.8	W
Temperature Range:			
Operating	$T(opr)$	-65 to 150	$^\circ C$
Storage	T_{STG}	-65 to 150	$^\circ C$

CHARACTERISTICS

Collector-to-Emitter Sustaining Voltage ($I_C = 100\text{ mA}$)	$V_{CEO(sus)}$	32 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 1500\text{ mA}, I_B = 150\text{ mA}$)	$V_{CE(sat)}$	1 max	V
Base-to-Emitter Voltage ($V_{CE} = 4\text{ V}, I_C = 1500\text{ mA}$)	V_{BE}	1.5 max	V
Collector-Cutoff Current ($V_{CB} = 30\text{ V}$)	I_{CBO}	0.5 max	μA
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}	1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 4\text{ V}, I_C = 1500\text{ mA}$)	h_{FE}	25 to 100	

POWER TRANSISTOR

40622



Si n-p-n type used for output stages in high-fidelity amplifier circuits suitable for complementary-symmetry circuits. This type features a base comprised of a homogeneous-resistivity and molded silicone plastic package with vertical leads. This type fits a standard TO-66 socket. Outline No.52.

MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage	$V_{CEO(sus)}$	40	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	4	A
Base Current	I_B	2	A
Transistor Dissipation:			
$T_C = 25^\circ C$	P_T	36	W
$T_A = 25^\circ C$	P_T	1.8	W

MAXIMUM RATINGS (cont'd)

Temperature Range:			
Operating	T (opr)	-65 to 150	°C
Storage	T _{STG}	-65 to 150	°C

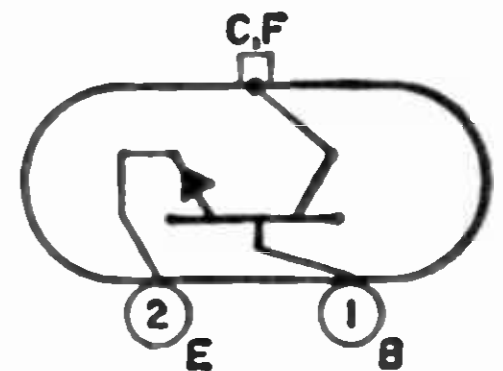
CHARACTERISTICS

Collector-to-Emitter Sustaining Voltage (I _C = 100 mA)	V _{CEO(sus)}	40 min	V
Collector-to-Emitter Saturation Voltage (I _C = 1500 mA, I _B = 150 mA)	V _{CE(sat)}	1 max	V
Base-to-Emitter Voltage (V _{CE} = 4 V, I _C = 1500 mA)	V _{BE}	1.5 max	V
Collector-Cutoff Current (V _{CE} = 40 V, R _{BE} = 100 Ω)	I _{CER}	500 max	μA
Emitter-Cutoff Current (V _{EB} = 5 V)	I _{EBO}	1 max	mA
Static Forward-Current Transfer Ratio (V _{CE} = 4 V, I _C = 1500 mA)	h _{FE}	25 to 100	

40623

POWER TRANSISTOR

Ge p-n-p type used for output stages in high-fidelity amplifier circuits suitable for complementary-symmetry circuits. JEDEC TO-3, Outline No.3.



MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage R _{BE} = 68 Ω	V _{CER(sus)}	-45	V
Emitter-to-Base Voltage	V _{EBO}	-5	V
Collector Current	I _C	-5	A
Base Current	I _B	-1	A
Transistor Dissipation (T _c = 25°C)	P _T	12.5	W
Temperature Range:			
Operating	T (opr)	-65 to 100	°C
Storage	T _{STG}	-65 to 100	°C

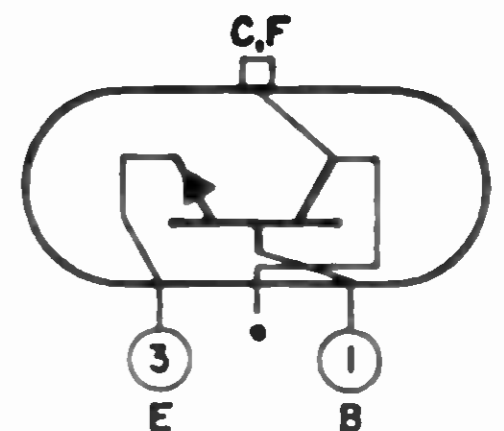
CHARACTERISTICS

Collector-to-Emitter Sustaining Voltage (I _C = -200 mA, R _{BE} = 68 Ω)	V _{CER(sus)}	-45 min	V
Collector-Cutoff Current (V _{CB} = -30 V)	I _{CBO}	-500 max	μA
Emitter-Cutoff Current (V _{EB} = -5 V)	I _{EBO}	-2 max	mA
Static Forward-Current Transfer Ratio (V _{CE} = -2 V, I _C = -1000 mA)	h _{FE}	50 to 170	

40624

POWER TRANSISTOR

Si n-p-n type used for output stages in high-fidelity amplifier circuits suitable for complementary-symmetry circuits. This type features a base comprised of a homogeneous-resistivity and molded silicone plastic package with vertical leads. This type fits a standard TO-66 socket. Outline No.52.



MAXIMUM RATINGS

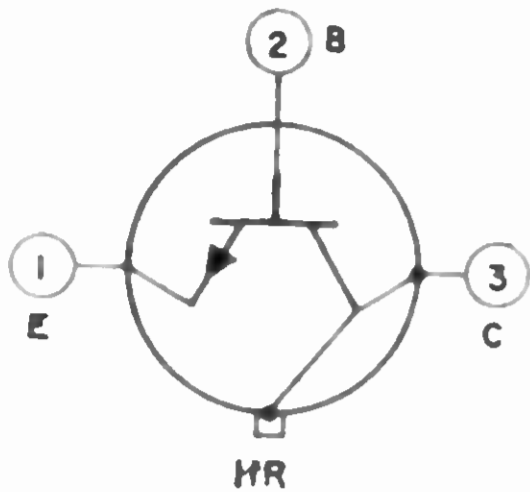
Collector-to-Emitter Sustaining Voltage	V _{CEO(sus)}	45	V
Emitter-to-Base Voltage	V _{EBO}	5	V
Collector Current	I _C	6	A
Base Current	I _B	3	A
Transistor Dissipation:			
T _c = 25°C	P _T	50	W
T _A = 25°C	P _T	1.8	W
Temperature Range:			
Operating	T (opr)	-65 to 150	°C
Storage	T _{STG}	-65 to 150	°C

CHARACTERISTICS

Collector-to-Emitter Sustaining Voltage (I _C = 100 mA)	V _{CEO(sus)}	45 min	V
Collector-to-Emitter Saturation Voltage (I _C = 2500 mA, I _B = 250 mA)	V _{CE(sat)}	1 max	V

CHARACTERISTICS (cont'd)

Base-to-Emitter Voltage ($V_{CE} = 4\text{ V}$, $I_C = 2500\text{ mA}$)	V_{BE}	1.7 max	V
Collector-Cutoff Current ($V_{CE} = 45\text{ V}$, $R_{BE} = 100\ \Omega$)	I_{CER}	500 max	μA
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}	1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 4\text{ V}$, $I_C = 2500\text{ mA}$)	h_{FE}	20 to 100	



POWER TRANSISTOR

40625

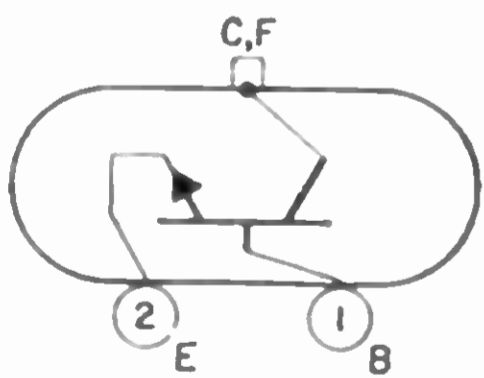
Si n-p-n type used for driver applications in high-fidelity amplifier circuits suitable for complementary-symmetry circuits. JEDEC TO-5 (with heat-radiator), Outline No.8.

MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage	$V_{CE0}(\text{sus})$	45	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Collector Current	I_C	1	A
Transistor Dissipation ($T_A = 25^\circ\text{C}$)	P_T	3.5	W
Temperature Range:			
Operating	$T(\text{opr})$	-65 to 200	$^\circ\text{C}$
Storage	T_{STG}	-65 to 200	$^\circ\text{C}$

CHARACTERISTICS

Collector-to-Emitter Sustaining Voltage ($I_C = 100\text{ mA}$)	$V_{CE0}(\text{sus})$	45 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 150\text{ mA}$, $I_B = 15\text{ mA}$)	$V_{CE}(\text{sat})$	0.5 max	V
Base-to-Emitter Voltage ($I_C = 150\text{ mA}$, $V_{CE} = 4\text{ V}$) ...	V_{BE}	1 max	V
Collector-Cutoff Current ($V_{CB} = 60\text{ V}$)	I_{CBO}	0.25 max	μA
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}	1 max	μA
Static Forward-Current Transfer Ratio ($V_{CE} = 10\text{ V}$, $I_C = 150\text{ mA}$)	h_{FE}	100 to 300	



POWER TRANSISTOR

40626

Ge p-n-p type used for output stages in high-fidelity amplifier circuits suitable for complementary-symmetry circuits. JEDEC TO-3, Outline No.2.

MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage ($R_{BE} = 68\ \Omega$)	$V_{CE0}(\text{sus})$	-55	V
Emitter-to-Base Voltage	V_{EBO}	-5	V
Collector Current	I_C	-5	A
Base Current	I_B	-1	A
Transistor Dissipation ($T_C = 25^\circ\text{C}$)	P_T	12.5	W
Temperature Range:			
Operating	$T(\text{opr})$	-65 to 100	$^\circ\text{C}$
Storage	T_{STG}	-65 to 100	$^\circ\text{C}$

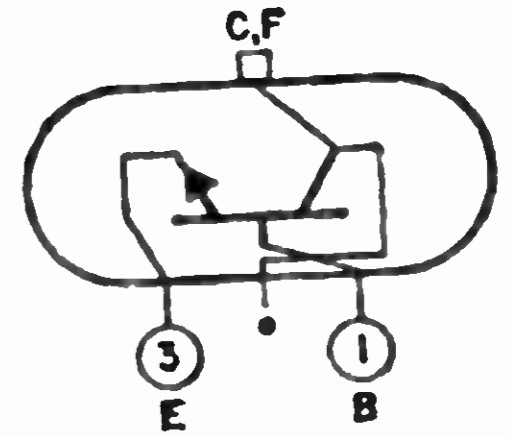
CHARACTERISTICS

Collector-to-Emitter Sustaining Voltage ($I_C = -200\text{ mA}$, $R_{BE} = 68\ \Omega$)	$V_{CE0}(\text{sus})$	-55 min	V
Collector-Cutoff Current ($V_{CB} = -30\text{ V}$)	I_{CBO}	-500 max	μA
Emitter-Cutoff Current ($V_{EB} = -5\text{ V}$)	I_{EBO}	-2 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = -2\text{ V}$, $I_C = -1000\text{ mA}$)	h_{FE}	50 to 170	

40627

POWER TRANSISTOR

Si n-p-n type used for output stages in high-fidelity amplifier circuits suitable for complementary-symmetry circuits. This type features a base comprised of a homogeneous-resistivity and molded silicone plastic package with vertical leads. This type fits a standard TO-66 socket. Outline No.52.



MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage	$V_{CEO(sus)}$	55	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	6	A
Base Current	I_B	3	A
Transistor Dissipation:			
$T_c = 25^\circ C$	P_T	50	W
$T_A = 25^\circ C$	P_T	1.8	W
Temperature Range:			
Operating	$T(opr)$	-65 to 150	$^\circ C$
Storage	T_{STG}	-65 to 150	$^\circ C$

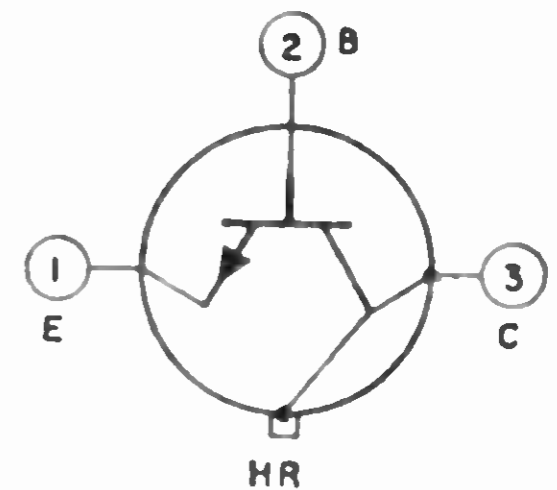
CHARACTERISTICS

Collector-to-Emitter Sustaining Voltage ($I_C = 100\text{ mA}$)	$V_{CEO(sus)}$	55 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 2500\text{ mA}, I_B = 250\text{ mA}$)	$V_{CE(sat)}$	1 max	V
Base-to-Emitter Voltage ($V_{CE} = 4\text{ V}, I_C = 2500\text{ mA}$)	V_{BE}	1.7 max	V
Collector-Cutoff Current ($V_{CE} = 55\text{ V}, R_{BE} = 100\ \Omega$)	I_{CER}	500 max	μA
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}	1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 4\text{ V}, I_C = 2500\text{ mA}$)	h_{FE}	20 to 100	

40628

POWER TRANSISTOR

Si n-p-n type used for driver applications in high-fidelity amplifier circuits suitable in complementary-symmetry circuits. JEDEC TO-5 (with heat-radiator), Outline No.8.



MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage	$V_{CEO(sus)}$	55	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Collector Current	I_C	1	A
Transistor Dissipation ($T_A = 25^\circ C$)	P_T	3.5	W
Temperature Range:			
Operating	$T(opr)$	-65 to 200	$^\circ C$
Storage	T_{STG}	-65 to 200	$^\circ C$

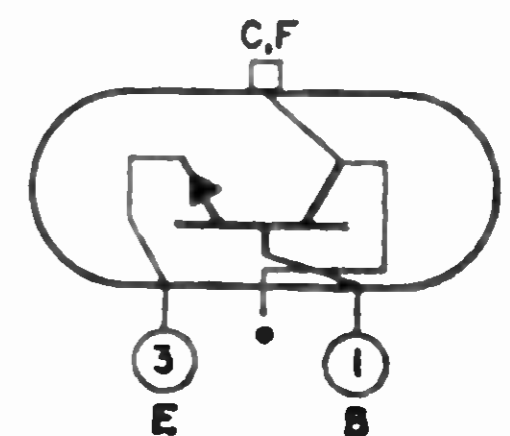
CHARACTERISTICS

Collector-to-Emitter Sustaining Voltage ($I_C = 100\text{ mA}$)	$V_{CEO(sus)}$	55 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 150\text{ mA}, I_B = 15\text{ mA}$)	$V_{CE(sat)}$	0.5 max	V
Base-to-Emitter Voltage ($V_{CE} = 4\text{ V}, I_C = 150\text{ mA}$)	V_{BE}	1 max	V
Collector-Cutoff Current ($V_{CB} = 60\text{ V}$)	I_{CBO}	0.25 max	μA
Emitter-Cutoff Current ($V_{EB} = 5\text{ V}$)	I_{EBO}	1 max	μA
Static Forward-Current Transfer Ratio ($I_C = 150\text{ mA}, V_{CE} = 10\text{ V}$)	h_{FE}	100 to 300	

40629

POWER TRANSISTOR

Si n-p-n type used for output stages in high-fidelity amplifier circuits. This type features a base comprised of a homogeneous-resistivity and molded silicone plastic package with vertical leads. This type fits a standard TO-66 socket. Outline No.52.

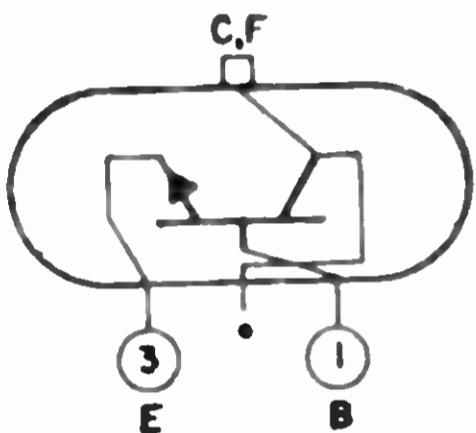


MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage $R_{BE} = 100 \Omega$	$V_{CER(sus)}$	35	V
Emitter-to-Base Voltage	V_{EB0}	5	V
Collector Current	I_C	4	A
Base Current	I_B	2	A
Transistor Dissipation:			
$T_C = 25^\circ C$	P_T	36	W
$T_A = 25^\circ C$	P_T	1.8	W
Temperature Range:			
Operating	$T(opr)$	-65 to 150	$^\circ C$
Storage	T_{STG}	-65 to 150	$^\circ C$

CHARACTERISTICS

Collector-to-Emitter Sustaining Voltage ($I_C = 100 \text{ mA}$, $R_{BE} = 100 \Omega$)	$V_{CER(sus)}$	35 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 1000 \text{ mA}$, $I_B = 100 \text{ mA}$)	$V_{CE(sat)}$	1 max	V
Base-to-Emitter Voltage ($V_{CE} = 4 \text{ V}$, $I_C = 1000 \text{ mA}$)	V_{BE}	1.3 max	V
Collector-Cutoff Current ($V_{CE} = 30 \text{ V}$, $R_{BE} = 100 \Omega$)	I_{CER}	0.5 max	mA
Emitter-Cutoff Current ($V_{EB} = 5 \text{ V}$)	I_{EB0}	1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 4 \text{ V}$, $I_C = 1000 \text{ mA}$)	h_{FE}	20 to 70	



POWER TRANSISTOR

40630

Si n-p-n type used for output stages in high-fidelity amplifier circuits. This type features a base comprised of a homogeneous-resistivity and molded silicone package with vertical leads. This type fits a standard TO-66 socket. Outline No.52.

MAXIMUM RATINGS

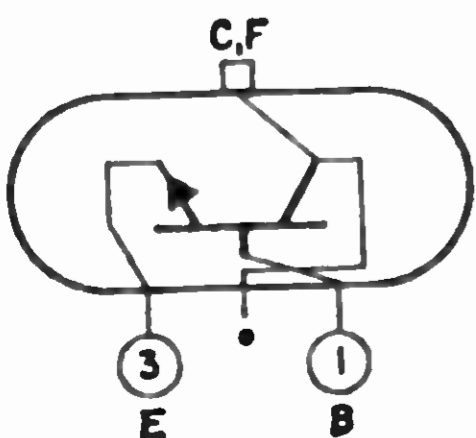
Collector-to-Emitter Sustaining Voltage $R_{BE} = 100 \Omega$	$V_{CER(sus)}$	40	V
Emitter-to-Base Voltage	V_{EB0}	5	V
Collector Current	I_C	4	A
Base Current	I_B	2	A
Transistor Dissipation:			
$T_C = 25^\circ C$	P_T	36	W
$T_A = 25^\circ C$	P_T	1.8	W
Temperature Range:			
Operating	$T(opr)$	-65 to 150	$^\circ C$
Storage	T_{STG}	-65 to 150	$^\circ C$

CHARACTERISTICS

Collector-to-Emitter Sustaining Voltage ($I_C = 100 \text{ mA}$, $R_{BE} = 100 \Omega$)	$V_{CER(sus)}$	40 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 1500 \text{ mA}$, $I_B = 150 \text{ mA}$)	$V_{CE(sat)}$	1 max	V
Base-to-Emitter Voltage ($V_{CE} = 4 \text{ V}$, $I_C = 1500 \text{ mA}$)	V_{BE}	1.4 max	V
Collector-Cutoff Current ($V_{CE} = 35 \text{ V}$, $R_{BE} = 100 \Omega$)	I_{CER}	0.5 max	mA
Emitter-Cutoff Current ($V_{EB} = 5 \text{ V}$)	I_{EB0}	1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 4 \text{ V}$, $I_C = 1500 \text{ mA}$)	h_{FE}	20 to 70	

POWER TRANSISTOR

40631



Si n-p-n type used for output stages in high-fidelity amplifier circuits suitable for quasi-complementary-symmetry circuits. This type features a base comprised of a homogeneous-resistivity and molded silicone plastic package with vertical leads. This type fits a standard TO-66 socket. Outline No.52.

MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage	$V_{CER(sus)}$	45	V
$R_{BE} = 100 \Omega$	V_{EBO}	5	V
Emitter-to-Base Voltage	I_C	4	A
Collector Current	I_B	2	A
Base Current	Transistor Dissipation:		
$T_C = 25^\circ C$	P_T	36	W
$T_A = 25^\circ C$	P_T	1.8	W
Temperature Range:	Operating		
Operating	$T(opr)$	-65 to 150	$^\circ C$
Storage	T_{STG}	-65 to 150	$^\circ C$

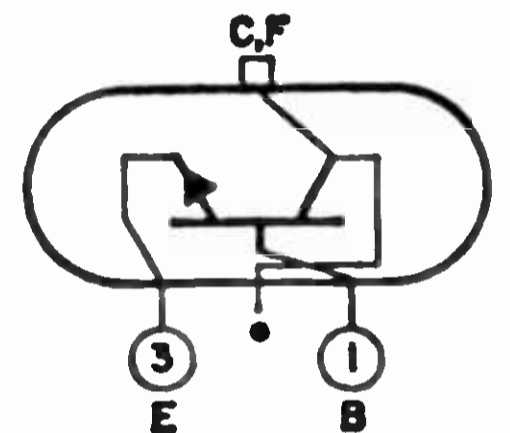
CHARACTERISTICS

Collector-to-Emitter Sustaining Voltage ($I_C = 100 \text{ mA}$, $R_{BE} = 100 \Omega$)	$V_{CER(sus)}$	45 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 2000 \text{ mA}$, $I_B = 200 \text{ mA}$)	$V_{CE(sat)}$	1 max	V
Base-to-Emitter Voltage ($V_{CE} = 4 \text{ V}$, $I_C = 2000 \text{ mA}$)	V_{BE}	1.5 max	V
Collector-Cutoff Current ($V_{CE} = 40 \text{ V}$, $R_{BE} = 100 \Omega$)	I_{CER}	0.5 max	mA
Emitter-Cutoff Current ($V_{EB} = 5 \text{ V}$)	I_{EBO}	1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 4 \text{ V}$, $I_C = 2000 \text{ mA}$)	h_{FE}	20 to 70	

40632

POWER TRANSISTOR

Si n-p-n type used for output stages in high-fidelity amplifier circuits suitable for quasi-complementary-symmetry circuits. This type features a base comprised of a homogeneous-resistivity and molded silicone plastic package with vertical leads. This type fits a standard TO-66 socket. Outline No.52.



MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage $R_{BE} = 100 \Omega$	$V_{CER(sus)}$	60	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	6	A
Base Current	I_B	3	A
Transistor Dissipation:	Operating		
$T_C = 25^\circ C$	P_T	50	W
$T_A = 25^\circ C$	P_T	1.8	W
Temperature Range:	Operating		
Operating	$T(opr)$	-65 to 150	$^\circ C$
Storage	T_{STG}	-65 to 150	$^\circ C$

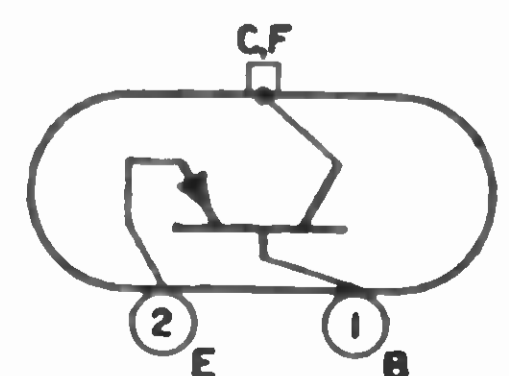
CHARACTERISTICS

Collector-to-Emitter Sustaining Voltage ($I_C = 100 \text{ mA}$, $R_{BE} = 100 \Omega$)	$V_{CER(sus)}$	60 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 3000 \text{ mA}$, $I_B = 300 \text{ mA}$)	$V_{CE(sat)}$	1 max	V
Base-to-Emitter Voltage ($V_{CE} = 4 \text{ V}$, $I_C = 3000 \text{ mA}$)	V_{BE}	1.4 max	V
Collector-Cutoff Current ($V_{CE} = 50 \text{ V}$, $R_{BE} = 100 \Omega$)	I_{CER}	0.5 max	mA
Emitter-Cutoff Current ($V_{EB} = 5 \text{ V}$)	I_{EBO}	1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 4 \text{ V}$, $I_C = 3000 \text{ mA}$)	h_{FE}	20 to 70	

40633

POWER TRANSISTOR

Si n-p-n type used for output stages in high-fidelity amplifier circuits suitable for quasi-complementary-symmetry circuits. This type features a base comprised of a homogeneous-resistivity and molded silicone plastic package with vertical leads. This type fits a standard TO-3 socket. Outline No.50.



MAXIMUM RATINGS

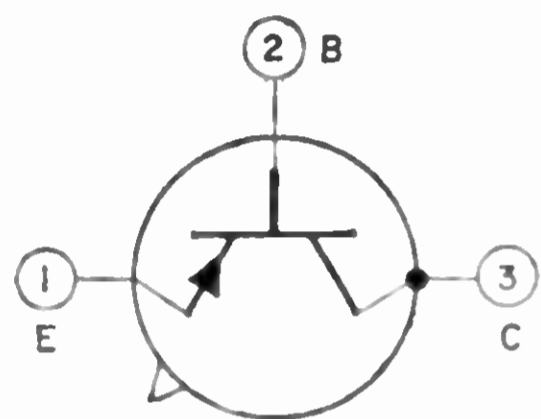
Collector-to-Emitter Sustaining Voltage $R_{BE} = 100 \Omega$	$V_{CER(sus)}$	75	V
Emitter-to-Base Voltage	V_{EB0}	5	V
Collector Current	I_C	8	A
Base Current	I_B	6	A
Transistor Dissipation:			
$T_C = 25^\circ C$	P_T	83	W
$T_A = 25^\circ C$	P_T	2	W
Temperature Range:			
Operating	$T(opr)$	-65 to 150	$^\circ C$
Storage	T_{STG}	-65 to 150	$^\circ C$

CHARACTERISTICS

Collector-to-Emitter Sustaining Voltage ($I_C = 200 \text{ mA}$, $R_{BE} = 100 \Omega$)	$V_{CER(sus)}$	75 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 4000 \text{ mA}$, $I_B = 400 \text{ mA}$)	$V_{CE(sat)}$	1 max	V
Base-to-Emitter Voltage ($V_{CE} = 4 \text{ V}$, $I_C = 4000 \text{ mA}$)	V_{BE}	1.4 max	V
Collector-Cutoff Current ($V_{CE} = 65 \text{ V}$, $R_{BE} = 100 \Omega$)	I_{CER}	0.5 max	mA
Emitter-Cutoff Current ($V_{EB} = 5 \text{ V}$)	I_{EB0}	1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 4 \text{ V}$, $I_C = 4000 \text{ mA}$)	h_{FE}	20 to 70	

POWER TRANSISTOR

40634



Si p-n-p type used for driver applications in high-fidelity amplifier circuits. This type and type 40635 form a complementary pair of driver transistors suitable for quasi-complementary-symmetry circuits. JEDEC TO-5, Outline No.5.

MAXIMUM RATINGS

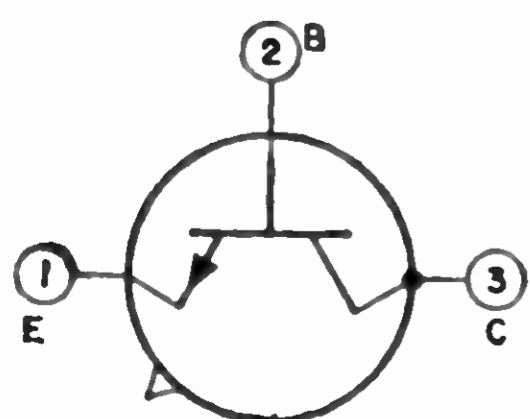
Collector-to-Emitter Sustaining Voltage $R_{BE} = 100 \Omega$	$V_{CER(sus)}$	-75	V
Emitter-to-Base Voltage	V_{EB0}	-7	V
Collector Current	I_C	-0.7	A
Base Current	I_B	-0.2	A
Transistor Dissipation:			
$T_C = 25^\circ C$	P_T	5	W
$T_C = 25^\circ C$	P_T	1	W
Temperature Range:			
Operating	$T(opr)$	-65 to 200	$^\circ C$
Storage	T_{STG}	-65 to 200	$^\circ C$

CHARACTERISTICS

Collector-to-Emitter Sustaining Voltage ($I_C = -100 \text{ mA}$, $R_{BE} = 100 \Omega$)	$V_{CER(sus)}$	-75 min	V
Collector-to-Emitter Saturation Voltage ($I_C = -150 \text{ mA}$, $I_B = -15 \text{ mA}$)	$V_{CE(sat)}$	-0.8 min	V
Base-to-Emitter Voltage ($V_{CE} = -4 \text{ V}$, $I_C = -150 \text{ mA}$)	V_{BE}	-1.4 max	V
Collector-Cutoff Current ($V_{CE} = -65 \text{ V}$, $R_{BE} = 100 \Omega$)	I_{CER}	-10 max	μA
Emitter-Cutoff Current ($V_{EB} = -4 \text{ V}$)	I_{EB0}	-0.1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = -4 \text{ V}$, $I_C = -150 \text{ mA}$)	h_{FE}	50 to 250	

POWER TRANSISTOR

40635



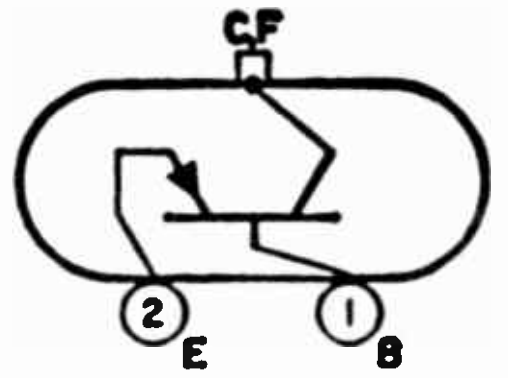
Si n-p-n type used for driver applications in high-fidelity amplifier circuits. This type and type 40634 form a complementary pair of driver transistors suitable for quasi-complementary-symmetry circuits. JEDEC TO-5, Outline No.5. This type is electrically identical with type 40634 except for the reversal of

all polarity signs.

40636

POWER TRANSISTOR

Si n-p-n type used for output stages in high-fidelity amplifier circuits suitable for quasi-complementary-symmetry circuits. JEDEC TO-3, Outline No.2.



MAXIMUM RATINGS

Collector-to-Emitter Sustaining Voltage $R_{BE} = 100 \Omega$	$V_{CER(sus)}$	95	V
Emitter-to-Base Voltage	V_{EBO}	7	V
Collector Current	I_C	15	A
Base Current	I_B	7	A
Transistor Dissipation $T_C = 25^\circ C$	P_T	115	W
Temperature Range: Operating	$T(opr)$	-65 to 200	$^\circ C$
Storage	T_{STG}	-65 to 200	$^\circ C$

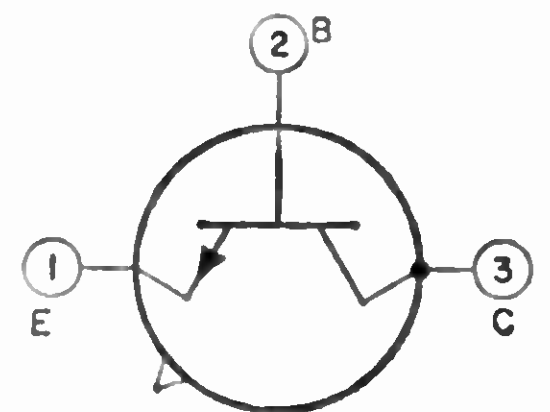
CHARACTERISTICS

Collector-to-Emitter Sustaining Voltage ($I_C = 200 \text{ mA}$, $R_{BE} = 100 \Omega$)	$V_{CER(sus)}$	95 min	V
Collector-to-Emitter Saturation Voltage ($I_C = 4000 \text{ mA}$, $I_B = 400 \text{ mA}$)	$V_{CE(sat)}$	1 max	V
Base-to-Emitter Voltage ($V_{CE} = 4 \text{ V}$, $I_C = 4000 \text{ mA}$)	V_{BE}	1.4 max	V
Collector-Cutoff Current ($V_{CE} = 85 \text{ V}$, $R_{BE} = 100 \Omega$)	I_{CER}	0.5 max	mA
Emitter-Cutoff Current ($V_{EB} = 4 \text{ V}$)	I_{EBO}	1 max	mA
Static Forward-Current Transfer Ratio ($V_{CE} = 4 \text{ V}$, $I_C = 4000 \text{ mA}$)	h_{FE}	20 to 70	

40637

RF TRANSISTOR

Si n-p-n epitaxial planar type used for frequency multiplier service to 175 MHz for low-level stages in mobile, marine and sonobouy vhf transmitters. JEDEC TO-52, Outline No.21.



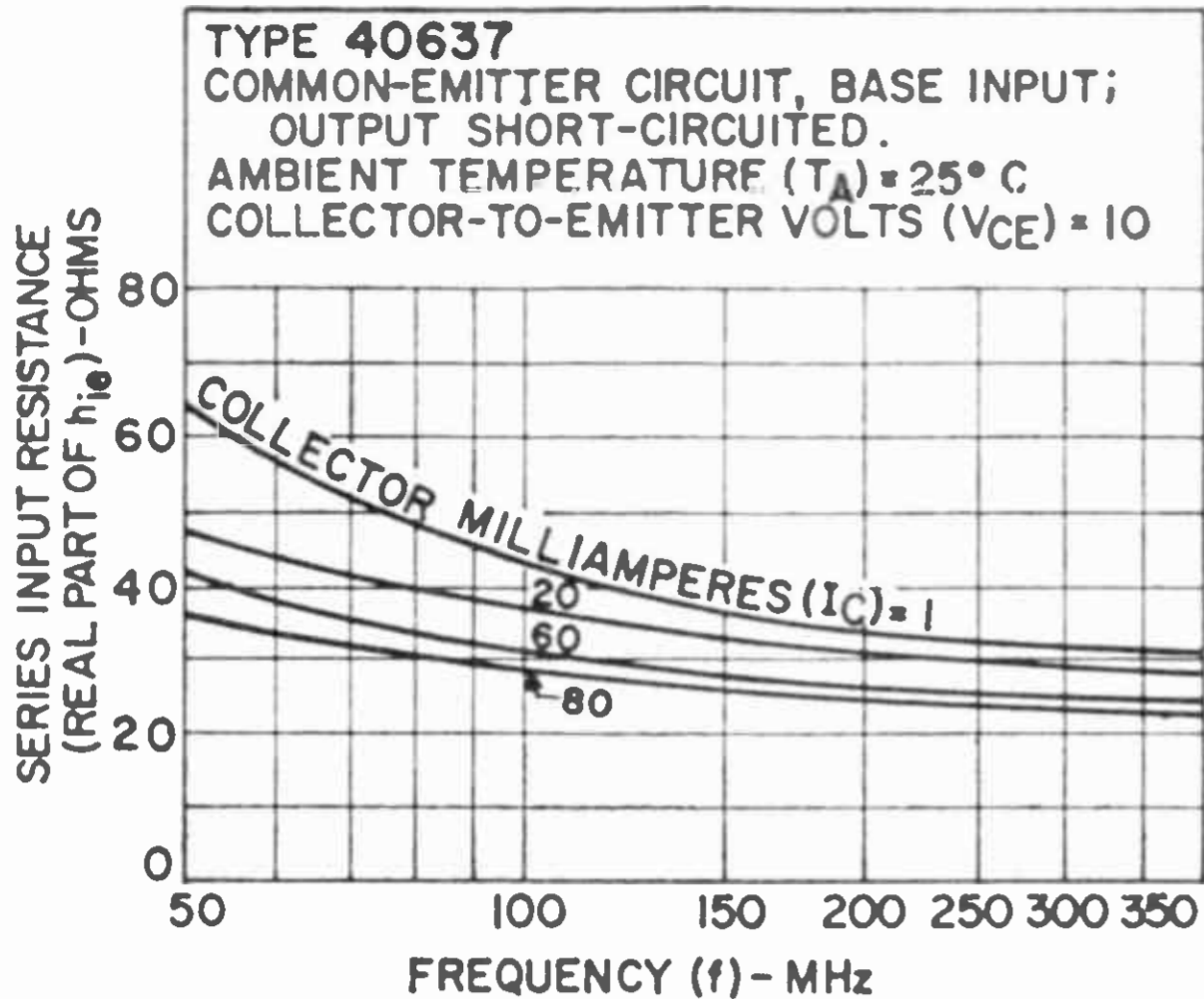
MAXIMUM RATINGS

Collector-to-Emitter Voltage	V_{CES}	30	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	100	mA
Transistor Dissipation: T_C up to $25^\circ C$	P_T	1	W
T_C above $25^\circ C$	P_T	See curve page 300	
T_A up to $25^\circ C$	P_T	0.3	W
T_A above $25^\circ C$	P_T	See curve page 300	
Temperature Range: Operating	$T(opr)$	-65 to 200	$^\circ C$
Storage	T_{STG}	-65 to 175	$^\circ C$
Lead-Soldering Temperature (10 s max)	T_L	265	$^\circ C$

CHARACTERISTICS

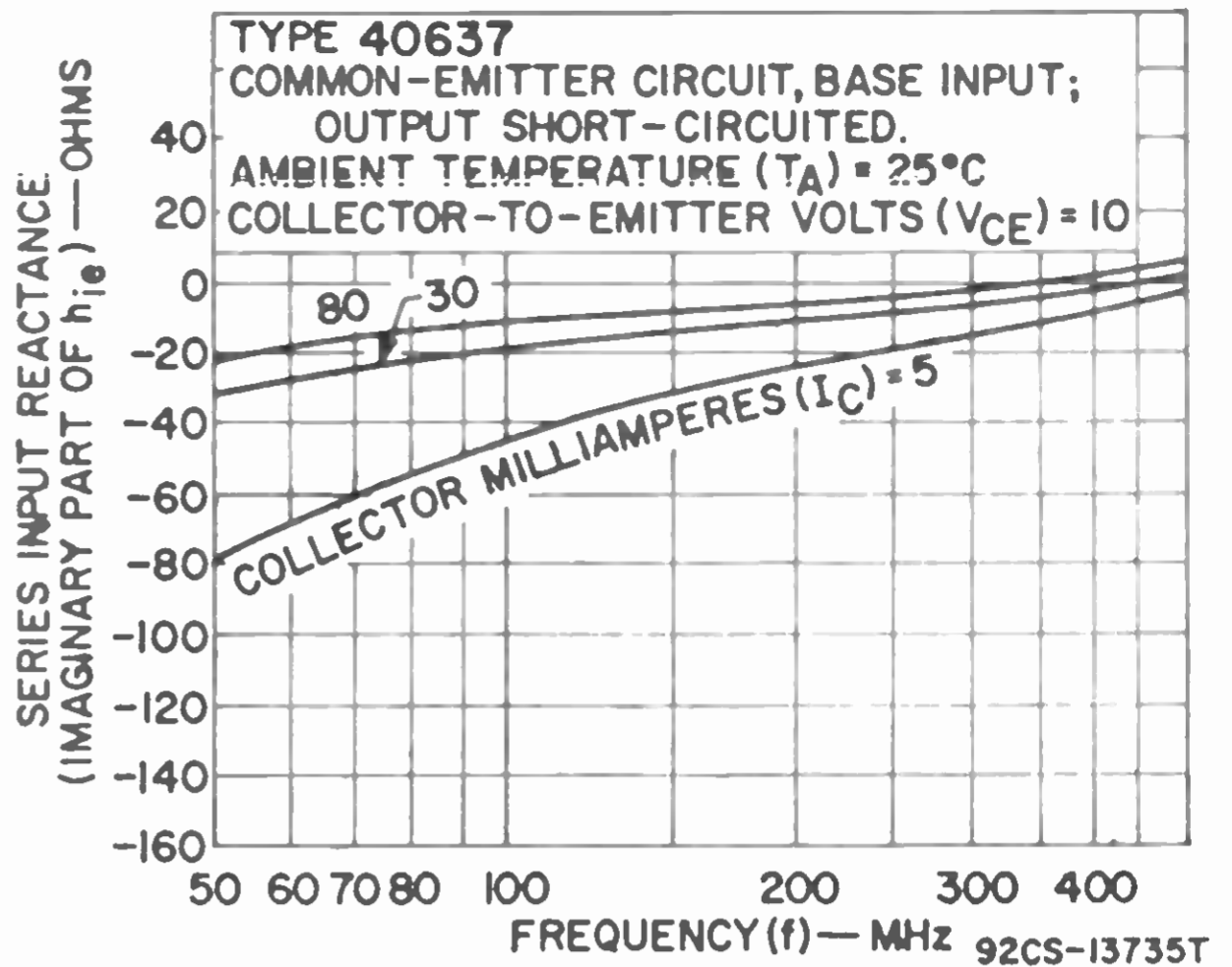
Collector-to-Emitter Breakdown Voltage ($I_C = 0.01 \text{ mA}$, $V_{BE} = 0$)	$V_{(BR)CES}$	30 min	V
Emitter-to-Base Breakdown Voltage ($I_E = -0.01 \text{ mA}$, $I_C = 0$)	$V_{(BR)EBO}$	5 min	V
Collector-to-Emitter Saturation Voltage ($I_B = 1 \text{ mA}$, $I_C = 10 \text{ mA}$)	$V_{CE(sat)}$	0.6 max	V
Magnitude of Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 1 \text{ V}$, $I_C = 50 \text{ mA}$, $f = 100 \text{ MHz}$)	$ h_{fe} $	3	
Collector-to-Base Capacitance ($V_{CB} = 12 \text{ V}$, $I_E = 0$, $f = 0.1$ to 1 MHz)	C_{obo}	3	pF
Power Output, Frequency Doubler ($P_{ie} = 37 \text{ mW}$, $f_{in} = 78 \text{ MHz}$, $f_{out} = 156 \text{ MHz}$)	P_{oe}	100 min	mW
Efficiency, Frequency Doubler ($f_{in} = 78 \text{ MHz}$, $f_{out} = 156 \text{ MHz}$)	η	18 min	%
Thermal Resistance, Junction-to-Case	θ_{J-C}	0.15 max	$^\circ C/mW$

TYPICAL RESISTANCE CHARACTERISTICS



92CS-13736T

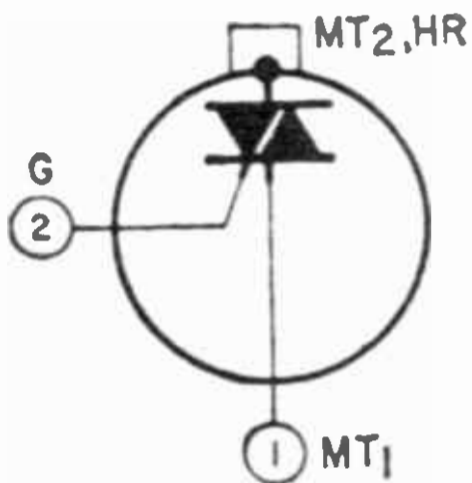
TYPICAL INPUT REACTANCE CHARACTERISTICS



92CS-13735T

TRIACS

40638
40639



Si gate-controlled full-wave types used for the control of ac loads in applications such as heating controls, motor controls, light dimmers, and power switching systems. These types have integral heat spreaders. Outline No.59. Types 40638 and 40639 are identical with types 40485 and 40486, respectively, except for

the following items:

MAXIMUM RATINGS (For sinusoidal ac supply voltage at 50/60 Hz with resistive or inductive load)

$I_{T(RMS)}$ ($T_c = 75^\circ C$, conduction angle = 360°)	40638	4	40639	A
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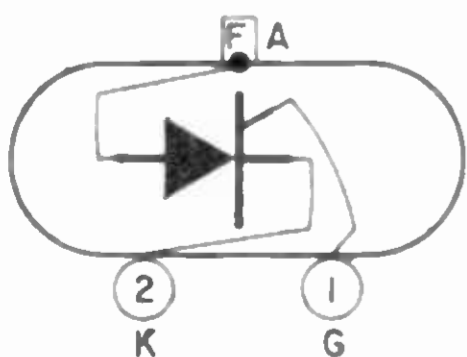
CHARACTERISTICS (At maximum electrical ratings at $T_c = 25^\circ C$)

I_{DROM}^* ($T_j = 100^\circ C$, $V_{DROM} = \text{max rated value}$)	0.2 typ; 4 max	mA
Commutating dv/dt^* ($V_D = V_{DROM}$, commutating $dv/dt = 3.2 \text{ A/ms}$, $I_{T(RMS)}$ and T_{HS} specified in Rating Chart (Heat Sink Temperature))	3 min; 10 typ	$V/\mu s$
θ_{J-HS}	7 max	$^\circ C/W$

*.For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.

SILICON CONTROLLED RECTIFIER

40640



Si type used for horizontal deflection circuits of large-screen color-TV receivers. This type and type 40642 (silicon rectifier), are the trace circuit components. They provide bipolar switching action for controlling the horizontal yoke current during the picture tube beam-trace interval, JEDEC TO-66, Outline No.25.

MAXIMUM RATINGS

V_{DROM}	600	V
V_{RRM}	5	V
$I_{T(AV)}$ (60 Hz dc at conduction angle = 180° , $T_c = 60^\circ C$)	3.2	A
$I_{T(RMS)}$	5	A
I_{TSM}	80	A
Critical di/dt ($V_D = V_{F(BO)}$ rated value, $I_{GT} = 50 \text{ mA}$, $t_r = 0.1 \mu s$)	200	$A/\mu s$
P_{GM} (peak (forward or reverse) 10 s max)	25	W

MAXIMUM RATINGS (cont'd)

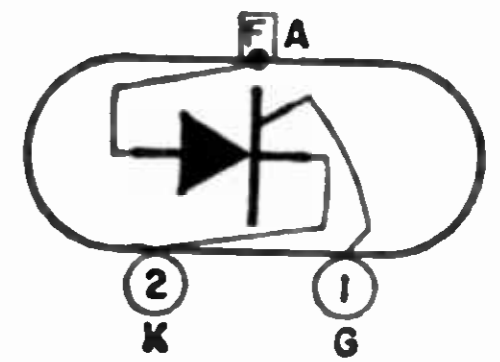
T_{STG}	-40 to 150	°C
T_C	-40 to 100	°C

CHARACTERISTICS (At maximum electrical ratings at $T_C = 25^\circ\text{C}$)

$V_{F(BO)O}$ ($T_C = 80^\circ\text{C}$)	550 min	V
I_{DOM} ($T_C = 80^\circ\text{C}$)	0.5 typ; 1.5 max	mA
V_T (on-state = 30 A)	2.2 typ; 3 max	V
I_{GT}	15 typ; 30 max	mA (dc)
V_{GT}	1.8 typ; 4 max	V (dc)
θ_{J-C}	4 max	°C/W
t_q ($I_{TM} = 6$ A ($t_r = 25$ μs , $di/dt = 2.5$ A/ μs), $V_D = 0$ V (prior to turn on), $V_D = 400$ V (reapplied at 175 V/ μs), $V_R = 0.8$ V (min), $I_{GT} = 100$ mA, V_{GK} (bias) = -30 V (68 Ω source), $f = 15.75$ kHz, $T_C = 70^\circ\text{C}$)	2.5	μs

40641 SILICON CONTROLLED RECTIFIER

Si type used for horizontal deflection circuits of large-screen color-TV receivers. This type and type 40643 (silicon rectifier), are the commutating (retrace) circuit components. They control the yoke current during the retrace interval. JEDEC TO-66, Outline No.25. This type is identical with type 40640 except for the following items:



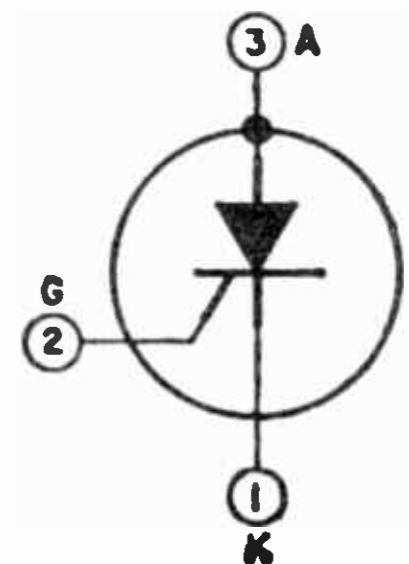
CHARACTERISTICS (At maximum electrical ratings at $T_C = 25^\circ\text{C}$)

$V_{F(BO)O}$ ($T_C = 100^\circ\text{C}$)	400 min	V
I_{DOM} ($T_C = 100^\circ\text{C}$)	0.5 typ; 1.5 max	mA
t_q ($I_{TM} = 13$ A, ($1/2$ sine wave, 7 μs base, initial $di/dt = 20$ A/ μs to 3 A), $V_D = 350$ V (prior to turn on), $dV/dt = 400$ V/ μs (to 100 V), $V_R = 0.8$ V (min), $I_{GT} = 100$ mA ($t_p = 3$ μs , $t_r = 0.2$ μs), V_{GK} (bias) = -2.5 V (47 Ω source during turn off), $f = 15.75$ kHz, $T_C = 70^\circ\text{C}$)	4.5 max	μs

- 40642** Refer to Charts of Rectifier Data
- 40643** Refer to Charts of Rectifier Data
- 40644** Refer to Charts of Rectifier Data

40654 40655 SILICON CONTROLLED RECTIFIERS

Si all-diffused three-junction types for use in capacitor-discharge ignition systems, high-voltage generators, and power-switching and control applications. Outline No.60.



MAXIMUM RATINGS (For sinusoidal ac supply voltage at $f = 50$ to 400 Hz with resistive or inductive load)

$V_{RSOM}\dagger$	40654	40655	V
$V_{DSOM}\dagger$	200	400	
$V_{RRM}\dagger$	250	500	
$V_{DRM}\dagger$	200	400	
I_{TSM} (1 cycle of principal voltage at 60 Hz)	200	400	A
		80	

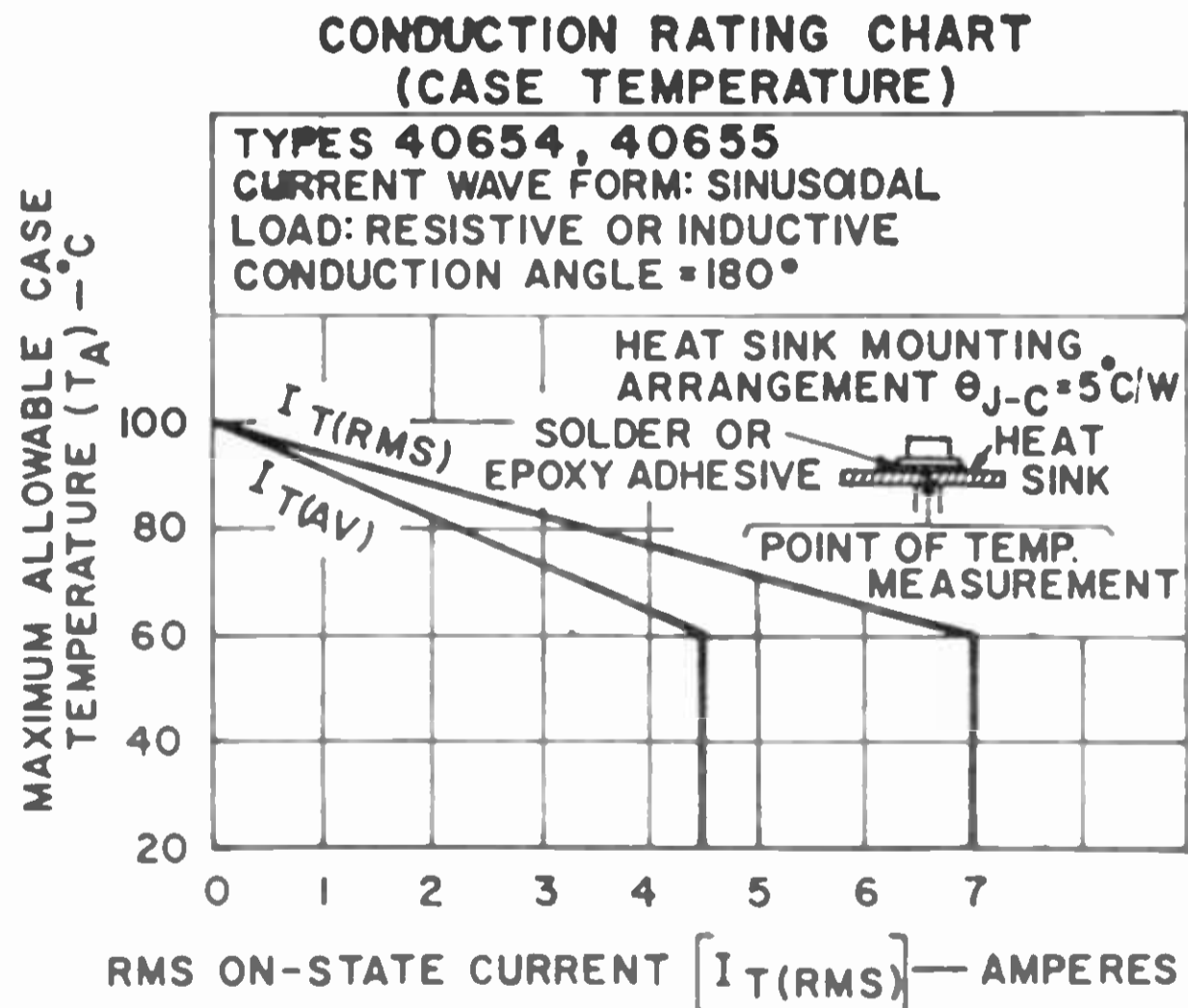
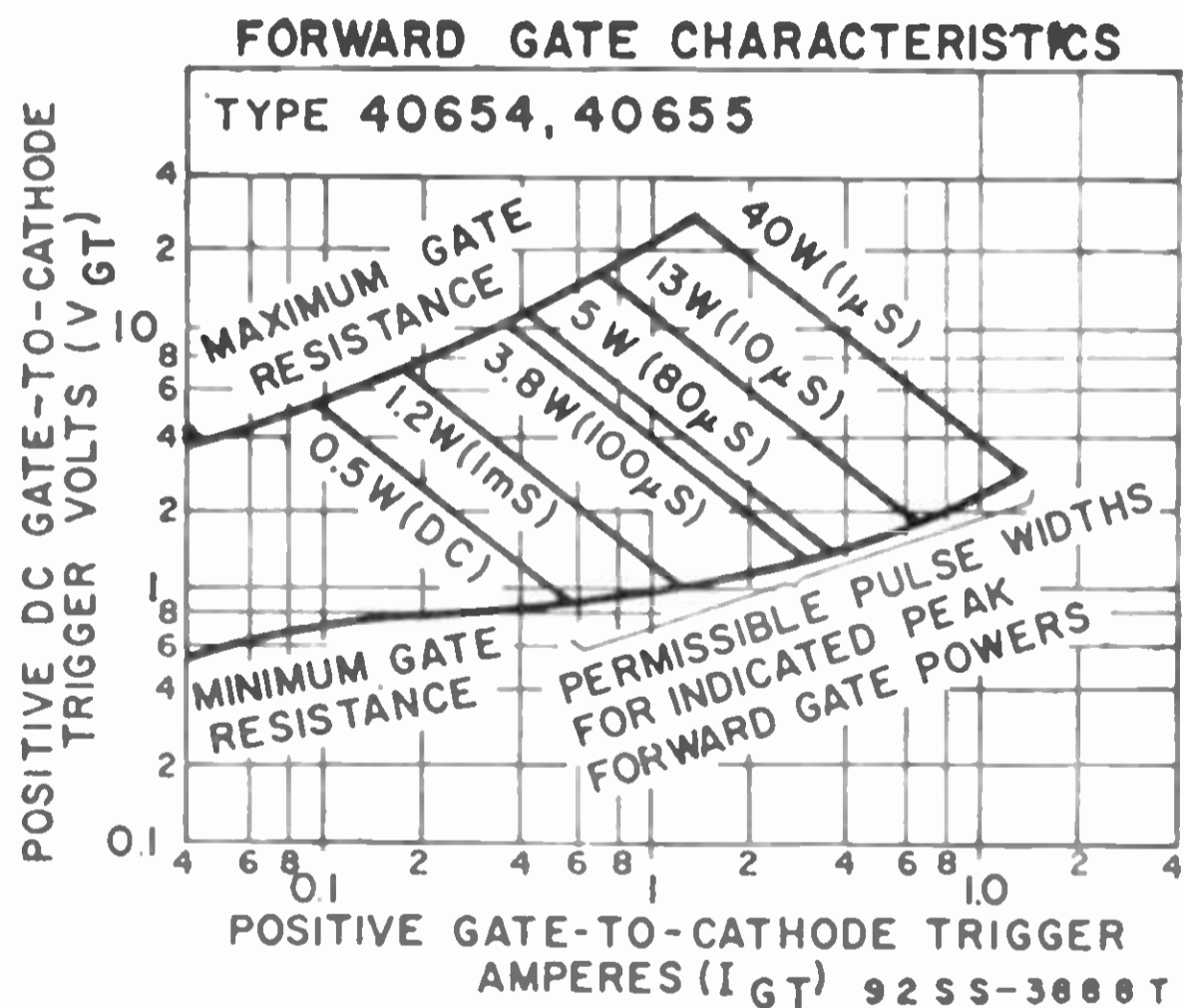
MAXIMUM RATINGS (cont'd)

I_{TRM} :			
df = 0.1%, $T_c = 75^\circ\text{C}$, $t_p = 2.5 \mu\text{s}$ min ...	100		A
$t_p = 5 \mu\text{s}$ min		100	A
$I_{T(RMS)}$:			
$T_c = 60^\circ\text{C}$, conduction angle = 180° ▲ ...		7	A
T_A up to 100°C , conduction angle = 180° *	See Conduction Rating Chart (Ambient Temperature)		
P_{GM} ●		40	W
$P_{G(AV)}$ ●		0.5	W
T_{STG} ■		-65 to 150	$^\circ\text{C}$
T_c (opr) ■		-65 to 100	$^\circ\text{C}$
T_s ■ (10 s max)		225	$^\circ\text{C}$

CHARACTERISTICS (At maximum electrical ratings at $T_c = 25^\circ\text{C}$)

$V_{F(BO)}$ ($T_c = 100^\circ\text{C}$)	250 min	500 min	V
I_{DOM} ($V_{DO} = V_{DROM}$, $T_c = 100^\circ\text{C}$)	0.1 typ; 0.5 max	0.2 typ; 0.5 max	mA
I_{RROM} ($V_{RO} = V_{RROM}$, $T_c = 100^\circ\text{C}$)	0.05 typ; 0.5 max	0.1 typ; 0.5 max	mA
V_T ($i_T = 30 \text{ A}$)	1.9 typ; 2.6 max		V
I_{GT} ($V_D = 12 \text{ Vdc}$, $R_L = 30 \Omega$)	6 typ; 15 max		mA
V_{GT} ($V_D = 12 \text{ Vdc}$, $R_L = 30 \Omega$)	0.65 typ; 1.5 max		V
i_{HO}	9 typ; 20 max		mA
Critical dv/dt ($V_{DO} = V_{F(BO)}$)	20 min; 200 typ		V/ μs
t_{gt} ($V_D = V_{F(BO)}$, $i_T = 4.5 \text{ A}$, $I_{GT} = 200 \text{ mA}$, $t_r = 0.1 \mu\text{s}$)	1.5		μs
t_q ($V_D = V_{F(BO)}$, $i_T = 2 \text{ A}$, $t_p = 50 \mu\text{s}$, $dv/dt = -20 \text{ V}/\mu\text{s}$, $di_T/dt = -30 \text{ A}/\mu\text{s}$, $I_{GT} = 200 \text{ mA}$ at t_{on} , $T_c = 75^\circ\text{C}$)	15 typ; 50 max		μs
θ_{J-C}	5 max		$^\circ\text{C}/\text{W}$
θ_{J-A} *	75 max		$^\circ\text{C}/\text{W}$

- ‡ This value does not apply if there is a positive gate signal. Gate must be open, terminated, or have negative bias.
- Any values of peak gate current or peak gate voltage to give the maximum gate power are permissible.
- When this device is soldered directly to the heat sink, a 60/40 solder should be used. Case heating time should be minimum . . . sufficient to allow the solder to flow freely.
- ▲ This characteristic does not apply to types 40658 and 40659.
- * This characteristic does not apply to types 40656 and 40657.



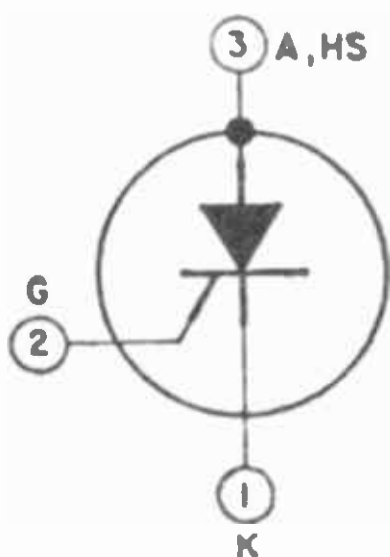
92SS-3882T1

SILICON CONTROLLED RECTIFIERS

40656
40657

Si all-diffused three-junction types for use in capacitor-discharge ignition systems, high-voltage generators, and power-switching and control applications. See Mounting Hardware for desired mounting arrangement. Outline No.59. Types 40656 and 40657 are identical with types 40654 and 40655, respectively, except for the

following items:

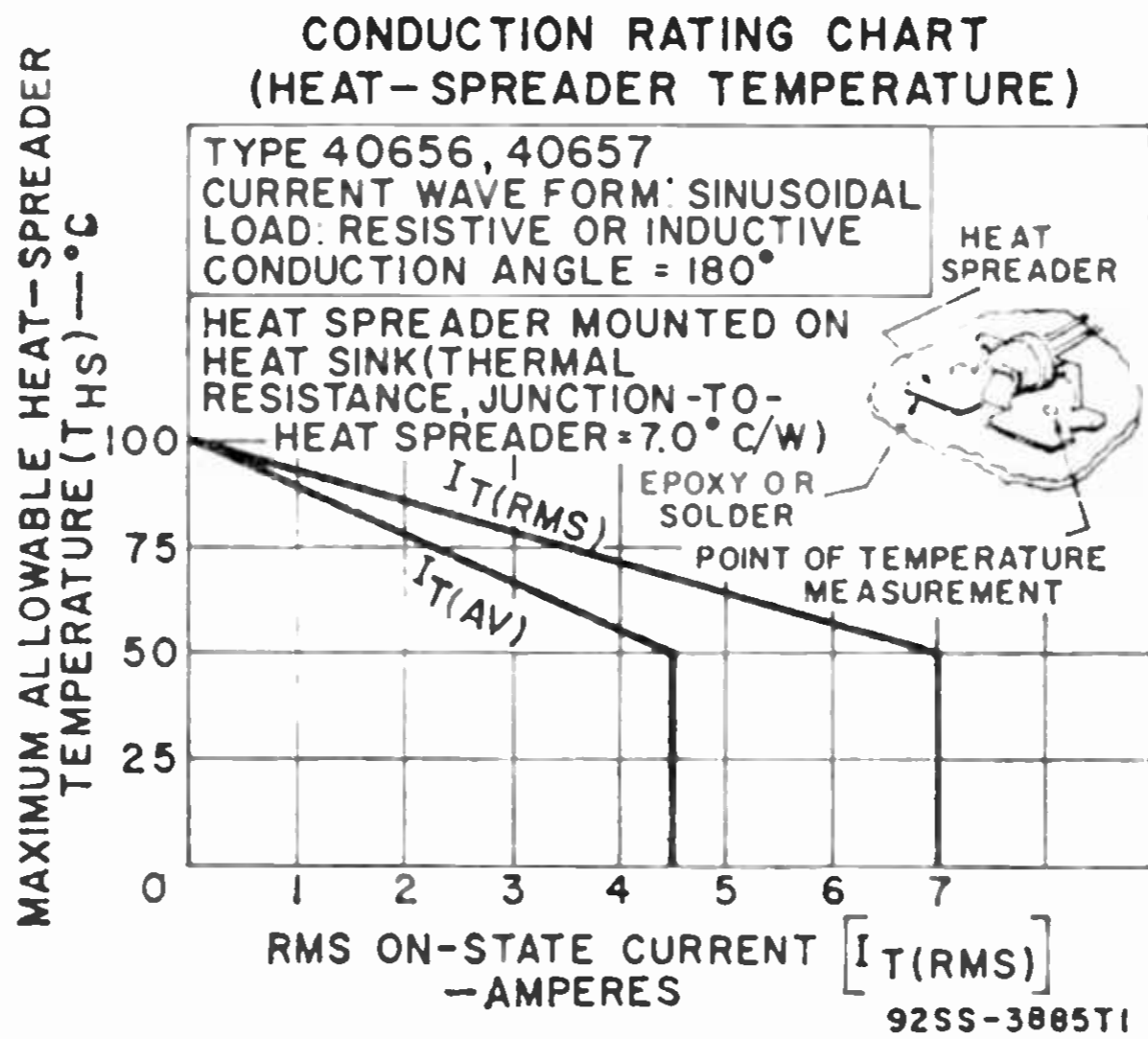


MAXIMUM RATINGS (For sinusoidal ac supply voltage at $f = 50$ to 400 Hz with resistive or inductive load)

	40656	40657	
		See Conduction Rating	
$I_{T(RMS)}$ ($T_c = 60^\circ\text{C}$, conduction angle = 180°)		Chart (Heat-Spreader Temperature)	

CHARACTERISTICS (At maximum electrical ratings at $T_c = 25^\circ\text{C}$)

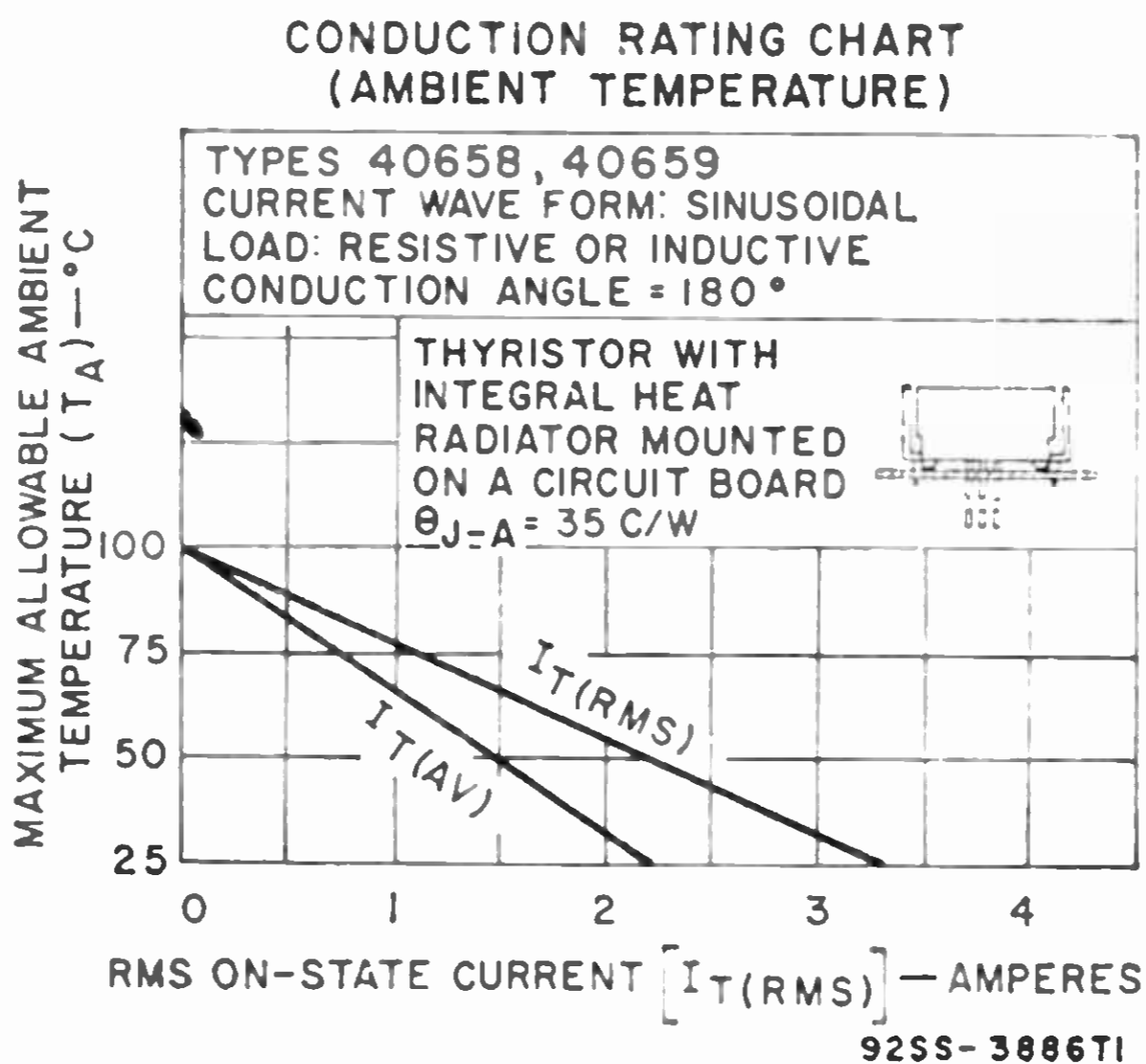
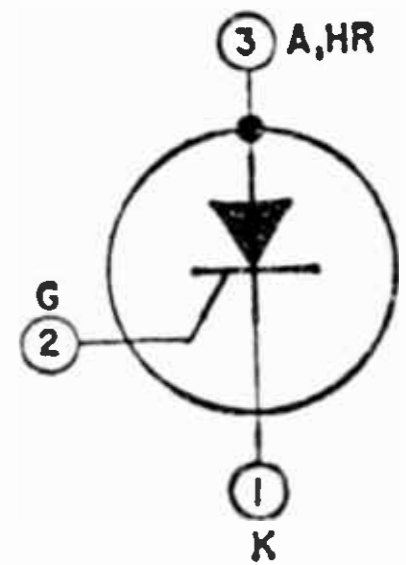
I_{DOM} ($V_{DO} = V_{DROM}$)	0.1 typ; 1.5 max	0.2 typ; 1.5 max	mA
I_{RROM} ($V_{RO} = V_{RROM}$)	0.05 typ; 1.5 max	0.1 typ; 1.5 max	mA
θ_{J-HS}	7 max		$^\circ\text{C/W}$



**40658
40659**

**SILICON
CONTROLLED RECTIFIERS**

Si all-diffused three-junction types for use in capacitor-discharge igniton systems, high-voltage generators, and power-switching and control applications. Outline No.8. Types 40658 and 40659 are identical with types 40654 and 40655, respectively, except for the following items:



MAXIMUM RATINGS (For sinusoidal ac supply voltage at $f = 50$ to 400 Hz with resistive or inductive load)

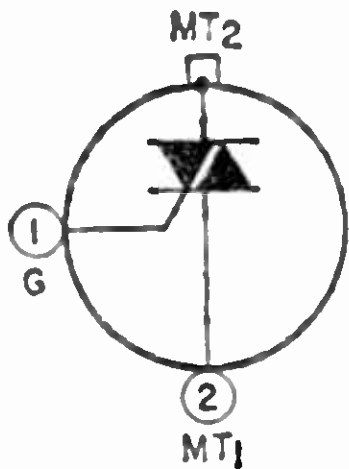
$I_{T(RMS)}$ (T_A up to 100°C , conduction angle = 180°)	40658	40659	
	See Conduction Rating Chart (Ambient Temperature)		

CHARACTERISTICS (At maximum electrical ratings at $T_c = 25^\circ\text{C}$)

I_{DOM} ($V_{DO} = V_{DROM}$)	0.1 typ; 1.5 max	0.2 typ; 1.5 max	mA
I_{RROM} ($V_{RO} = V_{RROM}$)	0.05 typ; 1.5 max	0.1 typ; 1.5 max	mA
θ_{JA}	35 max		$^\circ\text{C/W}$

**40660
40661**

TRIACS



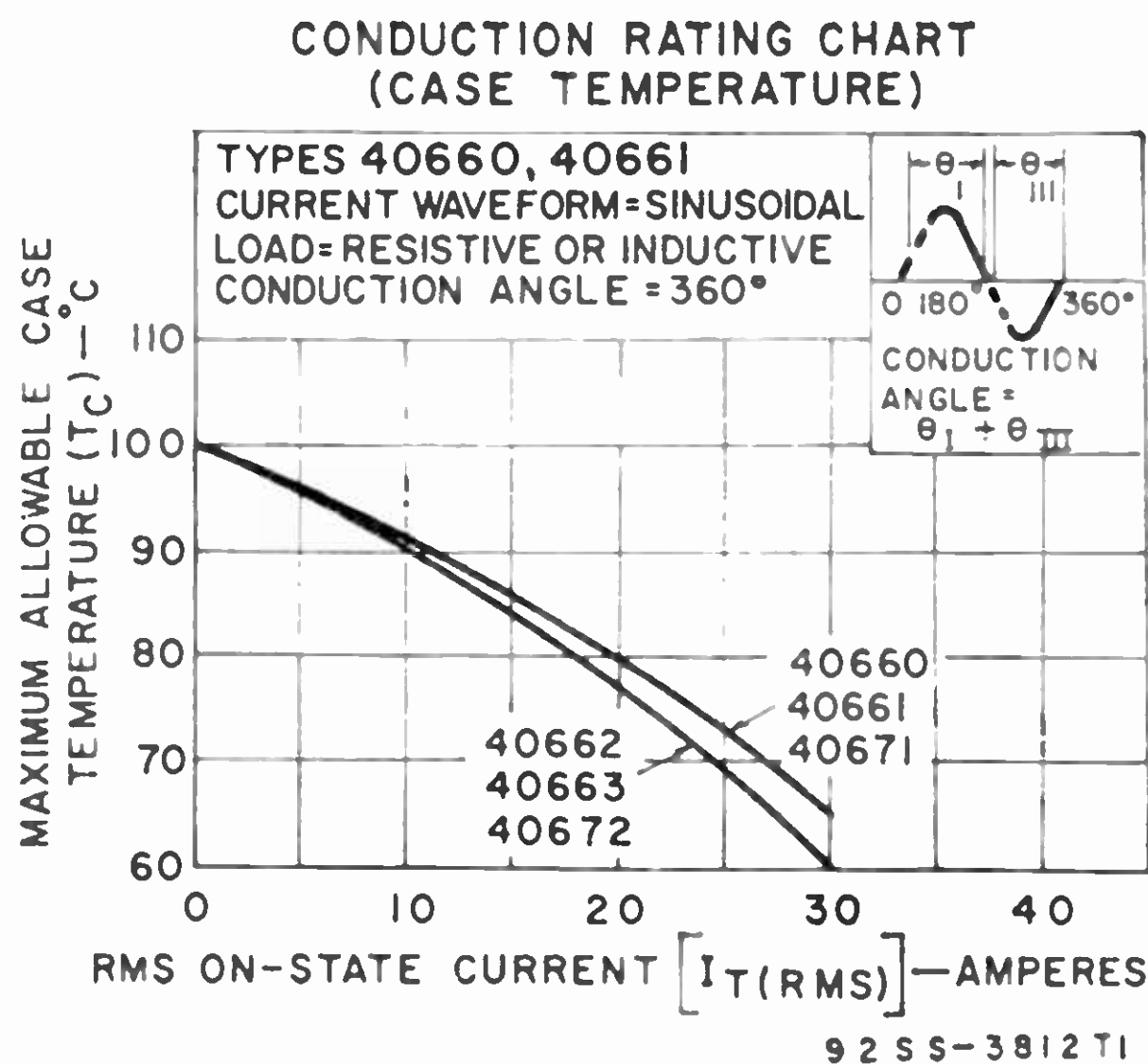
Si gate-controlled full-wave types used for the control of ac loads in applications such as heating controls, motor controls, arc welding equipment, light dimmers, and power switching systems. See **Mounting Hardware** for desired mounting arrangement. Outline No.36.

MAXIMUM RATINGS (For sinusoidal supply voltage at 50/60 Hz with resistive or inductive load)

V_{DROM}^* ($T_J = -65^\circ\text{C}$ to 100°C)	40660	40661	V
$I_{T(RMS)}$ ($T_c = 65^\circ\text{C}$, conduction angle = 360°)	200	400	A
I_{TSM} :			
1 cycle of principal voltage at 60 Hz		300	A
1 cycle of principal voltage at 50 Hz		265	A
I_{GTM}^\ddagger ($1 \mu\text{s}$ max)		12	A
P_{GM}^\ddagger ($10 \mu\text{s}$ max, $I_{GTM} \leq 4$ A peak)		40	W
$P_{G(AV)}$		0.75	W
T_{STG}		-65 to 150	$^\circ\text{C}$
T_c (ODF)		-65 to 100	$^\circ\text{C}$

CHARACTERISTICS (At maximum electrical ratings at $T_c = 25^\circ\text{C}$)

I_{DROM}^* ($T_J = 100^\circ\text{C}$, $V_{DROM} =$ max rated value)	0.2 typ; 4 max	mA
V_{TM}^* ($i_T = 100$ A peak)	2.1 typ; 2.5 max	V
I_{HO}^* (initial principal current = 150 mA dc)	25 typ; 60 max	mA
Commutating dv/dt^* ($v_D = V_{DROM}$, $I_{T(RMS)} = 30$ A, commutating $di/dt = 16$ A/ms, gate unenergized at $T_c = 60^\circ\text{C}$)	3 min; 20 typ	$\text{V}/\mu\text{s}$
Critical dv/dt^* ($v_D = V_{DROM}$, exponential voltage rise, $T_c = 100^\circ\text{C}$)	40 min; 200 typ 25 min; 150 typ	$\text{V}/\mu\text{s}$



CHARACTERISTICS (cont'd)

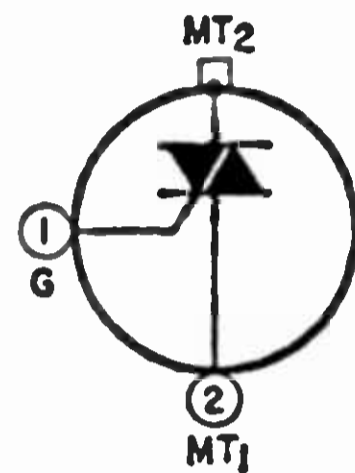
	40660	40661	
$I_{GT}^* \ddagger$ ($V_D = 12$ Vdc, $R_L = 12 \Omega$):			
I+ mode, V_{MT2} positive, V_G positive	15 typ; 50 max		mA
I- mode, V_{MT2} positive, V_G negative	30 typ; 80 max		mA
III+ mode, V_{MT2} negative, V_G positive	40 typ; 80 max		mA
III- mode, V_{MT2} negative, V_G positive	20 typ; 50 max		mA
$V_{GT}^* \ddagger$ ($V_D = 12$ Vdc, $R_L = 12 \Omega$)			
$V_{GT}^* \ddagger$ ($V_D = V_{DROM}$, $R_L = 125 \Omega$, $T_c = 100^\circ\text{C}$)	0.2 min		V
t_{gt} ($V_D = V_{DROM}$, $I_{GT} = 120$ mA, $t_r =$ 0.1 μs , $i_T = 43$ A peak)	3		μs
θ_{J-C} (steady-state)	0.8 max		$^\circ\text{C}/\text{W}$

* For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
 \ddagger For either polarity of gate voltage (V_G) with reference to main terminal 1.

40662
40663

TRIACS

Si gate-controlled full wave types used for the control of ac loads in applications such as heating controls, motor controls, arc-welding equipment, light dimmers, and power switching system. See Mounting Hardware for desired mounting arrangement. Outline No.37. Types 40662 and 40663 are identical with types 40660 and 40661 respectively, except for the following items:



MAXIMUM RATINGS (For sinusoidal supply voltage at 50/60 Hz with resistive or inductive load)

	40662	40663	
$I_{T(RMS)}$ ($T_c = 60^\circ\text{C}$, conduction angle = 360°)	30		A

CHARACTERISTICS (At maximum electrical ratings at $T_c = 25^\circ\text{C}$)

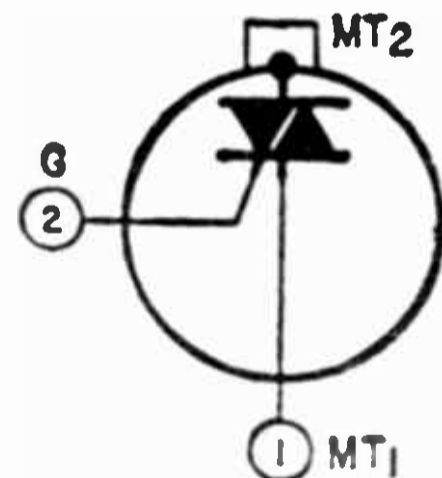
Commutating dv/dt^* ($V_D = V_{DROM}$, $I_{T(RMS)}$ = 30 A, commutating $di/dt = 16$ A/ms, gate unenergized at $T_c = 65^\circ\text{C}$)	3 min; 20 typ		$\text{V}/\mu\text{s}$
θ_{J-C} (steady-state)	0.9 max		$^\circ\text{C}/\text{W}$

* For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.

40664

TRIAC

Si gate-controlled full wave type used for 240-volt line light-dimmer and resistive load-control applications. Outline No.7.



MAXIMUM RATINGS (For sinusoidal supply voltage at 50/60 Hz with resistive or inductive load)

V_{DROM}^* ($T_J = -65^\circ\text{C}$ to 100°C)	450		V
$I_{T(RMS)}$ ($T_c = 75^\circ\text{C}$, conduction angle = 360°)	6		A
I_{TSM} :			
1 cycle of principal voltage at 60 Hz	100		A
1 cycle of principal voltage at 50 Hz	84		A
$I_{GTM} \ddagger$ (1 μs max)	4		A
$P_{GM} \ddagger$ (1 μs max, $I_{GTM} \leq 4$ A peak)	16		W
$P_{G(AV)}$	0.2		W
$T_{STG} \Delta$	-65 to 150		$^\circ\text{C}$
$T_c \Delta$ (opr)	-65 to 100		$^\circ\text{C}$
$T_c \Delta$ (soldering)	225		$^\circ\text{C}$

CHARACTERISTICS (At maximum electrical ratings at $T_c = 25^\circ\text{C}$)

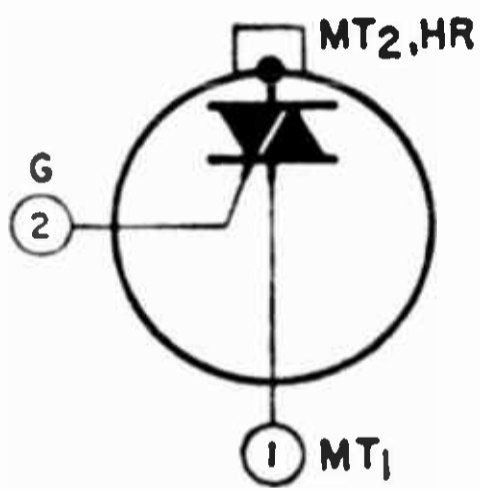
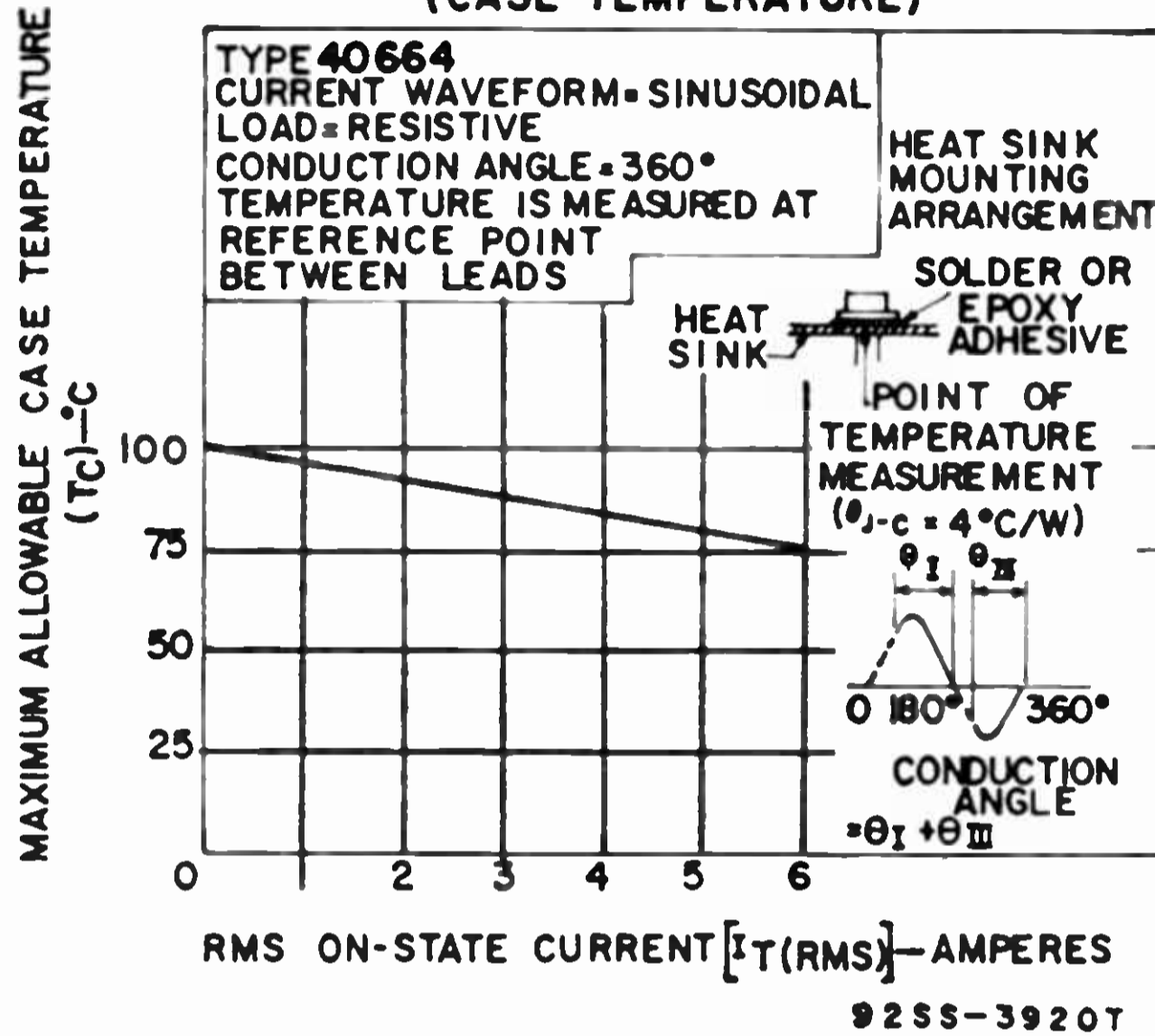
I_{DROM}^* ($T_J = 100^\circ\text{C}$, $V_{DROM} = \text{max. rated value}$)	0.2 typ; 4 max		mA
V_{TM}^* ($i_T = 10$ A peak)	1.1 typ; 2.25		V
Critical dv/dt^* ($V_D = V_{DROM}$, exponential voltage rise, gate open, $T_c = 100^\circ\text{C}$)	10 min; 100 typ		$\text{V}/\mu\text{s}$

CHARACTERISTICS (cont'd)

I_{GT}^* ($V_D = 12\text{ Vdc}$, $R_L = 30\ \Omega$):			
I+ mode, V_{MT2} positive, V_G positive	15 typ; 50 max	mA	
III- mode, V_{MT2} negative, V_G negative	15 typ; 50 max	mA	
V_{GT}^* ($V_D = 12\text{ Vdc}$, $R_L = 30\ \Omega$)	1 typ; 4 max	V	
θ_{J-C}^\bullet (steady-state)	4 max	$^\circ\text{C/W}$	

- * For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
- ‡ For either polarity of gate voltage (V_G) with reference to main terminal 1.
- This characteristic does not apply to type 40667.
- ▲ When soldered directly to the heat sink, a 60/40 solder should be used. Case heating time should be a minimum . . . sufficient to allow the solder to flow freely.

**CONDUCTION RATING CHART
(CASE TEMPERATURE)**



TRIAC

40667

Si gate-controlled full wave type used for 240-volt line light-dimmer and resistive load-control applications. It employs an integral heat spreader to provide efficient heat transfer to an external heat sink. See Mounting Hardware for desired mounting arrangement. Outline No.59. This type is identical with type 40664 except

for the following item:

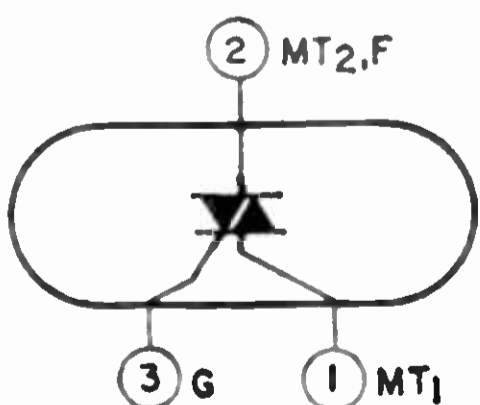
CHARACTERISTICS

θ_{J-HS} , Steady-State	5.5 max	$^\circ\text{C/W}$
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TRIACS

40668

40669



Si gate-controlled full-wave types used for the control of ac loads in such applications as motor controls, light dimmers, heating controls, and power-switching systems. See Mounting Hardware for desired mounting arrangement. Outline No.53.

MAXIMUM RATINGS (For sinusoidal ac supply voltage at $f = 50/60\text{ Hz}$ with resistive or inductive load)

V_{DROM}^* ($T_J = -65^\circ\text{C}$ to 100°C)	40668 200		40669 400	V
$I_{T(RMS)}$ ($T_C = 80^\circ\text{C}$, conduction angle = 360°)	_____	8	_____	A
I_{TSM} :				
1 cycle of principal voltage at 60 Hz	_____	100	_____	A
1 cycle of principal voltage at 50 Hz	_____	85	_____	A
I_{GTM}^\ddagger (10 μs max)	_____	4	_____	A

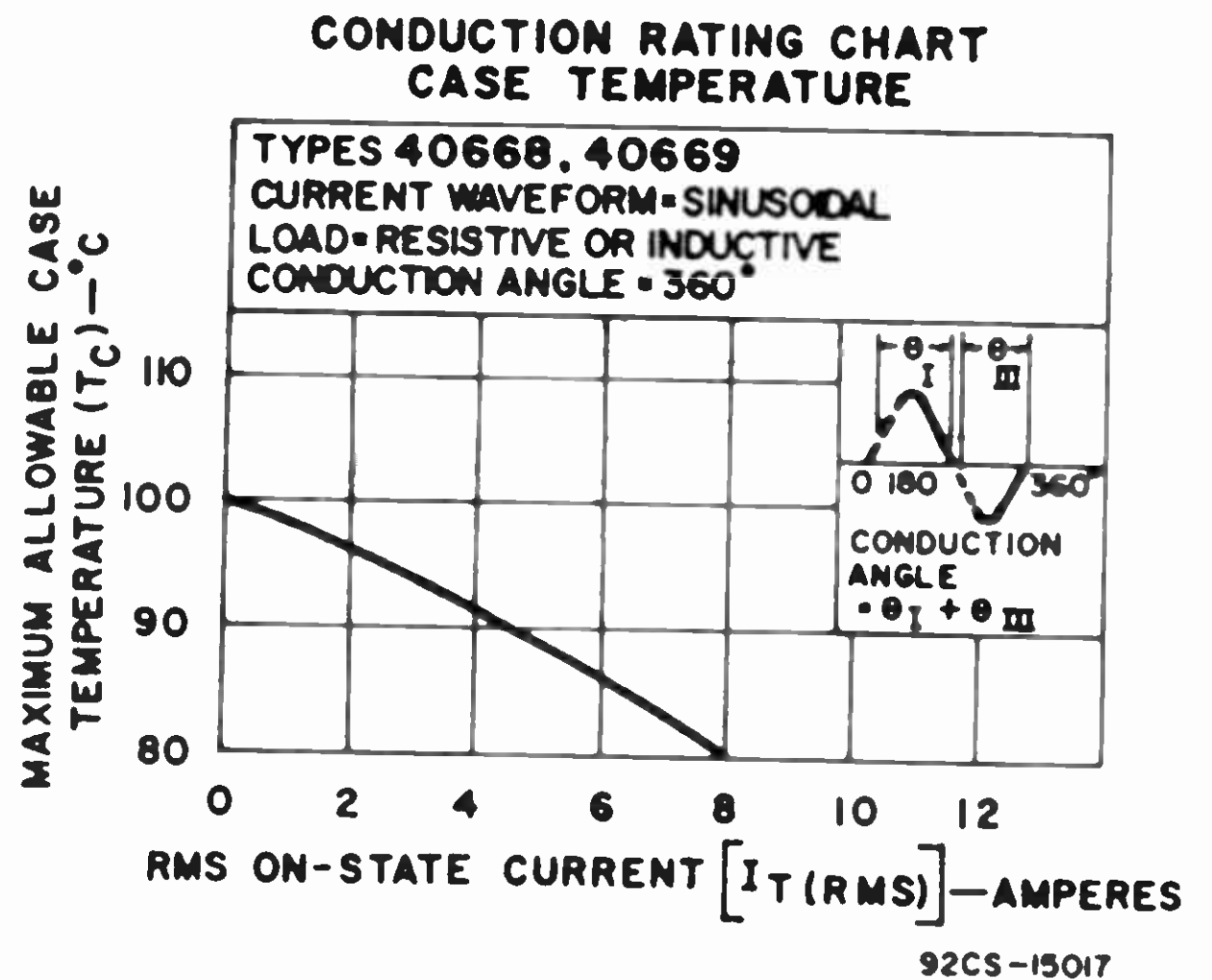
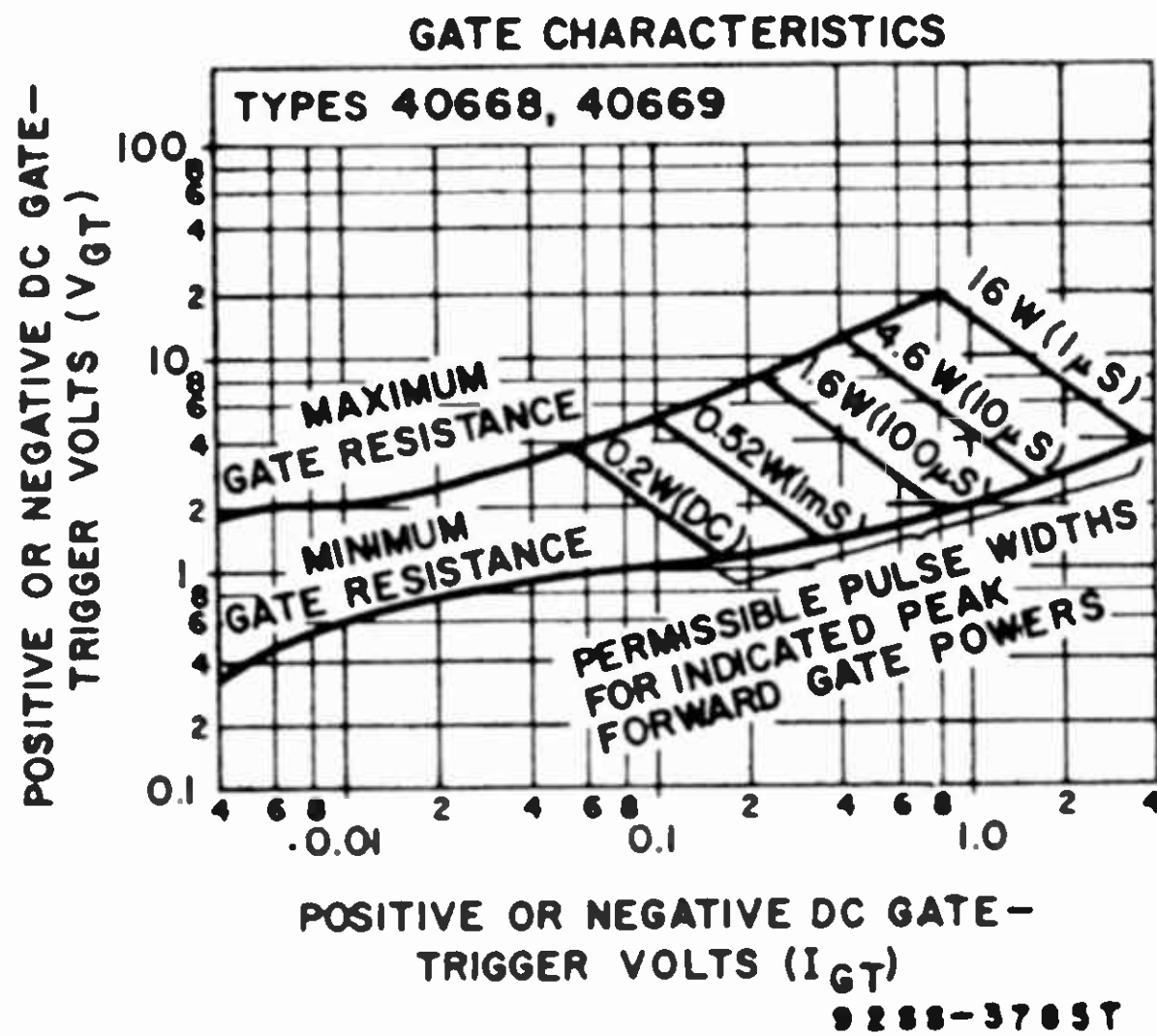
MAXIMUM RATINGS (cont'd)

$P_{GM} \ddagger$ (10 μ s max, $I_{GT} \leq 4$ A peak)	16	W
$P_{G(AV)}$	0.2	W
T_{STG}	-65 to 150	$^{\circ}$ C
T_c (opr)	-65 to 100	$^{\circ}$ C

CHARACTERISTICS (At maximum electrical ratings at $T_c = 25^{\circ}$ C)

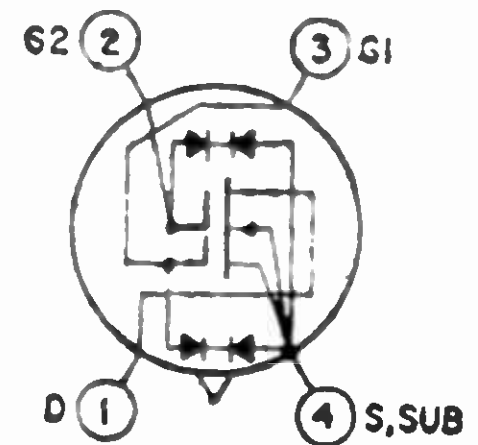
I_{DROM}^* ($T_J = 100^{\circ}$ C, $V_{DROM} =$ max rated value)	0.1 typ; 2 max	mA
V_{TM}^* ($i_T = 30$ A)	1.7 typ; 2 max	V
I_{HO}^* (initial principal current = 150 mA dc)	15 typ; 30 max	mA
Commutating dv/dt^* ($v_D = V_{DROM}$, $I_{T(RMS)} = 8$ A, commutating $di/dt = 4.3$ A/ms, gate unenergized at $T_c = 80^{\circ}$ C)	4 min; 10 typ	V/ μ s
Critical dv/dt^* ($v_D = V_{DROM}$, exponential voltage rise, gate open, $T_c = 100^{\circ}$ C)	100 min; 300 typ 75 min; 250 typ	V/ μ s
I_{GT}^{\ddagger} ($v_D = 12$ V, $R_L = 12 \Omega$):		
I ⁺ mode, V_{MT2} positive, V_G positive	10 typ; 25 max	mA
I ⁻ mode, V_{MT2} positive, V_G negative	20 typ; 60 max	mA
III ⁺ mode, V_{MT2} negative, V_G positive	30 typ; 60 max	mA
III ⁻ mode, V_{MT2} negative, V_G negative	15 typ; 25 max	mA
V_{GT}^{\ddagger} ($v_D = 12$ V, $R_L = 12 \Omega$)	1.25 typ; 2.5 max	V
V_{GT}^{\ddagger} ($v_D = V_{DROM}$, $R_L = 125 \Omega$, $T_c = 100^{\circ}$ C)	0.2 min	V
t_{gt} ($v_D = V_{DROM}$, $I_{GT} = 80$ mA, $t_r = 0.1 \mu$ s, $i_T = 10$ A peak)	2.2	μ s
θ_{J-C}	2.2 max	$^{\circ}$ C/W
θ_{J-A}	60 max	$^{\circ}$ C/W

* For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
 \ddagger For either polarity of gate voltage (V_G) with reference to main terminal 1.



40673 FIELD-EFFECT TRANSISTOR

Si dual-insulated gate field-effect (MOS) n-channel depletion type with integrated gate-protection circuits for rf-amplifier applications up to 400 MHz. JEDEC TO-72, Outline No.28.



MAXIMUM RATINGS

Drain-to-Source Voltage	V_{DS}	-0.2 to 20	V
Gate-No. 1-to-Source Voltage:			
Continuous (dc)	V_{G1S}	-6 to 1	V
Peak (ac)	V_{G1S}	-6 to 6	V
Gate-No. 2-to-Source Voltage:			
Continuous	V_{G2S}	-6 to (0.3 V_{DS})	V
Peak (ac)	V_{G2S}	-6 to 6	V
Drain-to-Gate-No. 1 Voltage	V_{DG1}	20	V
Drain-to-Gate-No. 2 Voltage	V_{DG2}	20	V
Drain Current	I_D	50	mA

MAXIMUM RATINGS (cont'd)

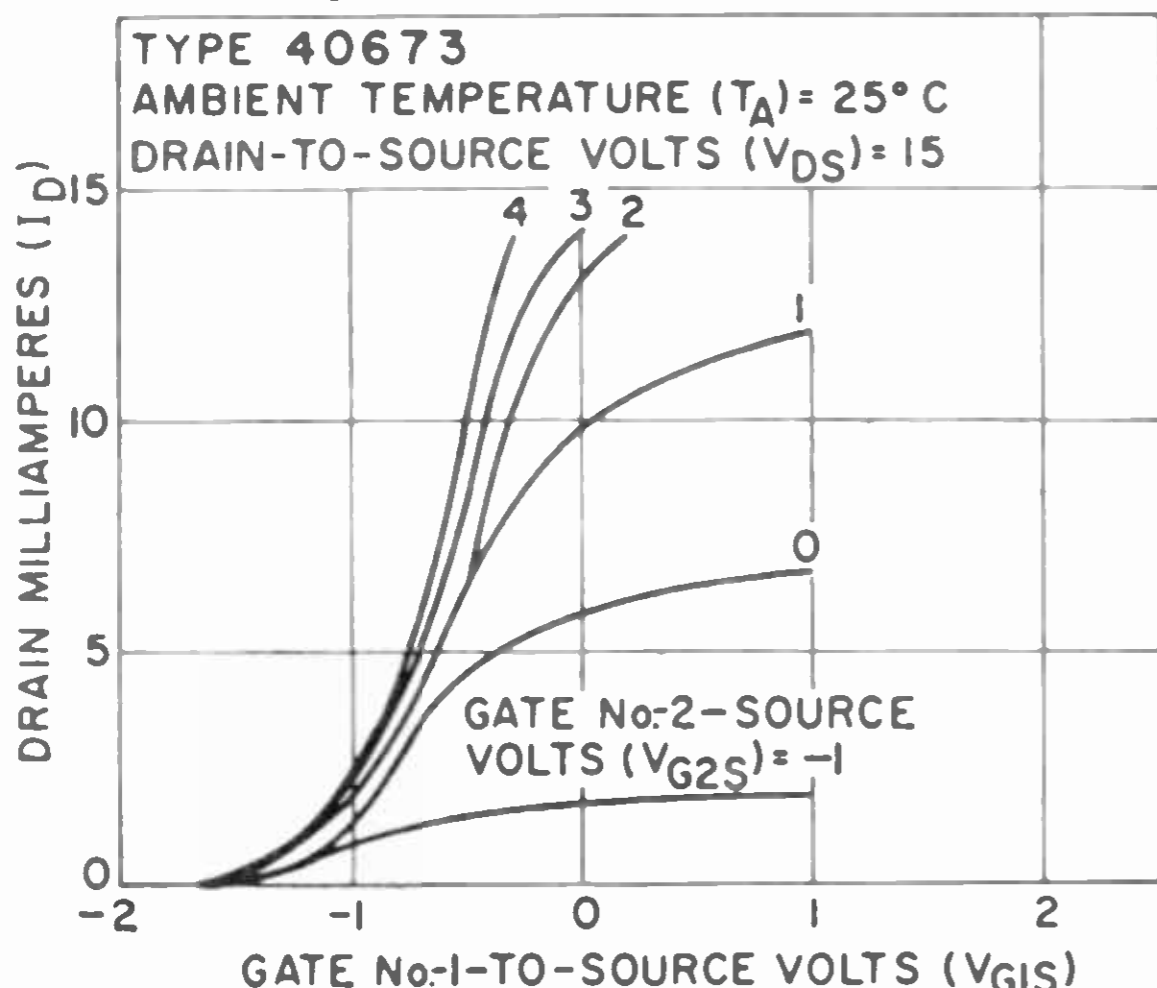
Transistor Dissipation:		P_T	330	mW
T_A up to 25°C		P_T	Derate linearly at 2.2 mW/°C	
T_A above 25°C				
Temperature Range:		$T(opr)$	-65 to 175	°C
Operating		T_{STG}	-65 to 175	°C
Storage		T_L	265	°C
Lead-Soldering Temperature (10 s max)				

CHARACTERISTICS

Gate-No. 1-to-Source Cutoff Voltage ($V_{DS} = 15\text{ V}$, $V_{G2S} = 4\text{ V}$, $I_D = 200\ \mu\text{A}$)	$V_{G1S}(off)$	-2 typ; -4 max	V
Gate-No. 2-to-Source Cutoff Voltage ($V_{DS} = 15\text{ V}$, $V_{G1S} = 0$, $I_D = 200\ \mu\text{A}$)	$V_{G2S}(off)$	-2 typ; -4 max	V
Gate-No. 1 Leakage Current ($V_{G1S} = 1\text{ or }-6\text{ V}$, $V_{G2S} = 0$, $V_{DS} = 0$)	I_{G1SS}	20 max	nA
Gate-No. 2 Leakage Current ($V_{G2S} = \pm 6\text{ V}$, $V_{G1S} = 0$, $V_{DS} = 0$)	I_{G2SS}	20 max	nA
Zero-Bias Drain Current ($V_{DS} = 15\text{ V}$, $V_{G1S} = 0$, $V_{G2S} = 4\text{ V}$)	I_{DSS}	5 to 35	mA
Forward Transconductance, Gate No. 1-to-Drain ($V_{DS} = 15\text{ V}$, $V_{G2S} = 4\text{ V}$, $I_D = 10\text{ mA}$, $f = 1\text{ kHz}$)	g_{fs}	12000	μmhos
Small-Signal Input Capacitance* ($V_{DS} = 15\text{ V}$, $V_{G2S} = 4\text{ V}$, $I_D = 10\text{ mA}$, $f = 1\text{ MHz}$)	C_{iss}	6	pF
Small-Signal Reverse Transfer Capacitance, Drain-to-Gate No. 1 ‡ ($V_{DS} = 15\text{ V}$, $V_{G2S} = 4\text{ V}$, $I_D = 10\text{ mA}$, $f = 1\text{ MHz}$)	C_{rss}	0.01 to 0.03	pF
Small-Signal Output Capacitance ($V_{DS} = 15\text{ V}$, $V_{G2S} = 4\text{ V}$, $I_D = 10\text{ mA}$, $f = 1\text{ MHz}$)	C_{oss}	2	pF
Power Gain ($V_{DS} = 15\text{ V}$, $V_{G2S} = 4\text{ V}$, $I_D = 10\text{ mA}$, $f = 200\text{ MHz}$)	G_{PS}	14 min; 18 typ	dB
Maximum Available Power Gain ($V_{DS} = 15\text{ V}$, $V_{G2S} = 4\text{ V}$, $I_D = 10\text{ mA}$, $f = 200\text{ MHz}$)	MAG	20	dB
Maximum Usable Power Gain(Unneutralized ($V_{DS} = 15\text{ V}$, $V_{G2S} = 4\text{ V}$, $I_D = 10\text{ mA}$, $f = 200\text{ MHz}$)	MUG	20■	dB
Noise Figure ($V_{DS} = 15\text{ V}$, $V_{G2S} = 4\text{ V}$, $I_D = 10\text{ mA}$, $f = 200\text{ MHz}$)	NF	3.5 typ; 6 max	dB
Magnitude of Forward Transadmittance ($V_{DS} = 15\text{ V}$, $V_{G2S} = 4\text{ V}$, $I_D = 10\text{ mA}$, $f = 200\text{ MHz}$)	$ Y_{fs} $	12000	μmho
Phase Angle of Forward Transadmittance ($V_{DS} = 15\text{ V}$, $V_{G2S} = 4\text{ V}$, $I_D = 10\text{ mA}$, $f = 200\text{ MHz}$)	θ	-35	degrees
Input Resistance ($V_{DS} = 15\text{ V}$, $V_{G2S} = 4\text{ V}$, $I_D = 10\text{ mA}$, $f = 200\text{ MHz}$)	r_{iss}	1	k Ω
Output Resistance ($V_{DS} = 15\text{ V}$, $V_{G2S} = 4\text{ V}$, $I_D = 10\text{ mA}$, $f = 200\text{ MHz}$)	r_{oss}	2.8	k Ω
Protective Diode Knee Voltage ($I_{DIODE(REVERSE)} = \pm 100\ \mu\text{A}$)	V_{knee}	± 10	V

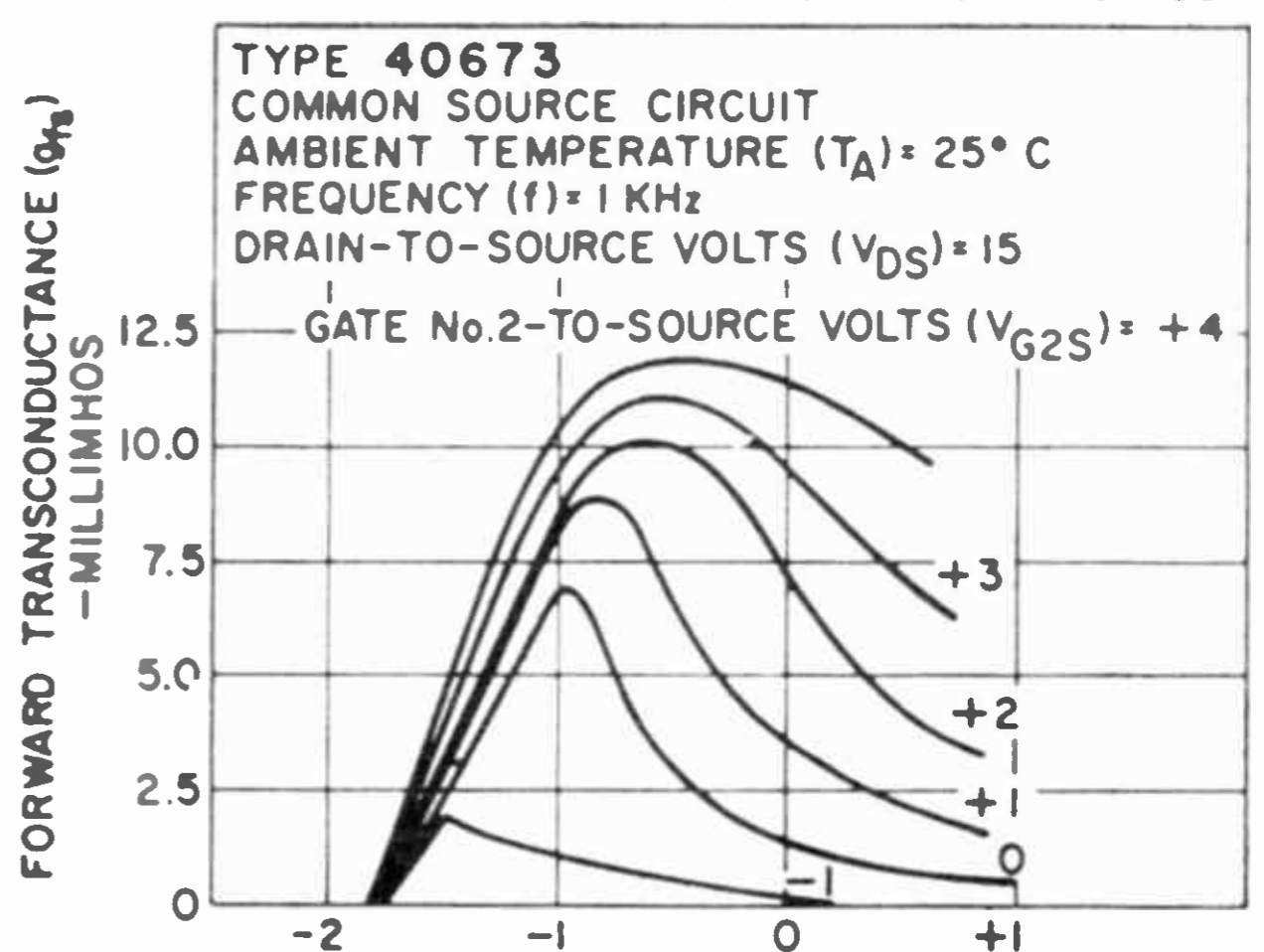
* Capacitance between gate No. 1 and all other terminals.
 ‡ Three-terminal measurement with gate No. 2 and all other terminals.
 ■ Limited only by practical design considerations.

TYPICAL DRAIN CHARACTERISTICS



92CS-14790T2

TYPICAL FORWARD TRANSCONDUCTANCE CHARACTERISTICS



92SS-4096T

CR101	Refer to Charts of Rectifier Data
CR102	Refer to Charts of Rectifier Data
CR103	Refer to Charts of Rectifier Data
CR104	Refer to Charts of Rectifier Data
CR105	Refer to Charts of Rectifier Data
CR106	Refer to Charts of Rectifier Data
CR107	Refer to Charts of Rectifier Data
CR108	Refer to Charts of Rectifier Data
CR109	Refer to Charts of Rectifier Data
CR110	Refer to Charts of Rectifier Data
CR201	Refer to Charts of Rectifier Data
CR203	Refer to Charts of Rectifier Data
CR204	Refer to Charts of Rectifier Data
CR206	Refer to Charts of Rectifier Data
CR208	Refer to Charts of Rectifier Data
CR210	Refer to Charts of Rectifier Data
CR212	Refer to Charts of Rectifier Data
CR273/8008	Refer to Charts of Rectifier Data
CR274/872A	Refer to Charts of Rectifier Data
CR275/866A/3B28	Refer to Charts of Rectifier Data
CR301	Refer to Charts of Rectifier Data
CR302	Refer to Charts of Rectifier Data
CR303	Refer to Charts of Rectifier Data
CR304	Refer to Charts of Rectifier Data
CR305	Refer to Charts of Rectifier Data
CR306	Refer to Charts of Rectifier Data
CR307	Refer to Charts of Rectifier Data
CR311	Refer to Charts of Rectifier Data
CR312	Refer to Charts of Rectifier Data
CR313	Refer to Charts of Rectifier Data
CR314	Refer to Charts of Rectifier Data
CR315	Refer to Charts of Rectifier Data

Refer to Charts of Rectifier Data	CR316
Refer to Charts of Rectifier Data	CR317
Refer to Charts of Rectifier Data	CR321
Refer to Charts of Rectifier Data	CR322
Refer to Charts of Rectifier Data	CR323
Refer to Charts of Rectifier Data	CR324
Refer to Charts of Rectifier Data	CR325
Refer to Charts of Rectifier Data	CR331
Refer to Charts of Rectifier Data	CR332
Refer to Charts of Rectifier Data	CR333
Refer to Charts of Rectifier Data	CR334
Refer to Charts of Rectifier Data	CR335
Refer to Charts of Rectifier Data	CR341
Refer to Charts of Rectifier Data	CR342
Refer to Charts of Rectifier Data	CR343
Refer to Charts of Rectifier Data	CR344
Refer to Charts of Rectifier Data	CR351
Refer to Charts of Rectifier Data	CR352
Refer to Charts of Rectifier Data	CR353
Refer to Charts of Rectifier Data	CR354
Refer to Charts of Rectifier Data	CR401
Refer to Charts of Rectifier Data	CR402
Refer to Charts of Rectifier Data	CR403
Refer to Charts of Rectifier Data	CR404
Refer to Charts of Rectifier Data	CR405
Refer to Charts of Rectifier Data	CR406
Refer to Charts of Rectifier Data	CR407
Refer to Charts of Rectifier Data	CR408
Refer to Charts of Rectifier Data	CR409
Refer to Charts of Rectifier Data	CR501
Refer to Charts of Rectifier Data	CR502
Refer to Charts of Rectifier Data	CR503

CR504	Refer to Charts of Rectifier Data
CR505	Refer to Charts of Rectifier Data
CR506	Refer to Charts of Rectifier Data
SQ2502	Refer to Charts of Photocell Data
SQ2503	Refer to Charts of Photocell Data
SQ2508	Refer to Charts of Photocell Data
SQ2519	Refer to Charts of Photocell Data
SQ2520	Refer to Charts of Photocell Data
SQ2521	Refer to Charts of Photocell Data
SQ2526	Refer to Charts of Photocell Data
SQ2527	Refer to Charts of Photocell Data
SQ2529	Refer to Charts of Photocell Data
SQ2534	Refer to Charts of Photocell Data
SQ2535	Refer to Charts of Photocell Data
SQ2536	Refer to Charts of Photocell Data
SQ2543	Refer to Charts of Photocell Data
SQ2544	Refer to Charts of Photocell Data
SQ2544V1	Refer to Charts of Photocell Data
SQ2545	Refer to Charts of Photocell Data
SQ2545V1	Refer to Charts of Photocell Data
SQ2546	Refer to Charts of Photocell Data
SQ2554	Refer to Charts of Photocell Data
SQ2555	Refer to Charts of Photocell Data
SQ2556	Refer to Charts of Photocell Data
SQ2557	Refer to Charts of Photocell Data
SQ2558	Refer to Charts of Photocell Data

CHART OF DISCONTINUED TRANSISTORS

(Shown for reference only; see page 211 for symbol identification.)

BIPOLAR TYPES

RCA Type	Bas- ing ‡	Mate- rial	Out- line	MAXIMUM RATINGS				CHARACTER- ISTICS		Maximum Operating Tempera- ture (°C)	Can be replaced by RCA type
				V _{CB} (volts)	V _{EB} (volts)	I _C (amperes)	P _T (watts)	Min. h _{FE}	I _{CB} (μA)		
2N105	1	Ge	*	-25	—	-0.015	0.035	55	-5	55	2N408
2N139	12	Ge	16	-16	—	-0.015	0.035	48	-6	70	—
2N173	2	Ge	14	-60	-40	-15	150	35	-100	100	—
2N174	2	Ge	14	-80	-60	-15	150	25	-100	100	—
2N206	1	Ge	1	-30	—	-0.050	0.075	33	-10	85	2N408
2N218	1	Ge	1	-16	—	-0.015	0.035	48	-6	70	—
2N219	1	Ge	1	-16	—	-0.015	0.08	75	-6	71	—
2N247	3	Ge	9	-35	—	-0.010	0.080	60	-10	71	2N1180
2N269	1	Ge	1	-25	-12	-0.100	0.120	24	-5	85	2N404
2N277	2	Ge	14	-40	-20	-15	150	35	-4000	100	—
2N278	2	Ge	14	-50	-30	-15	150	35	-15000	100	—
2N301	4	Ge	2	-40	-10	-3	11	70	-100	91	2N2869/2N301
2N301A	4	Ge	2	-60	-10	-3	11	70	-100	91	2N2870/2N301A
2N387	4	Ge	2	-35	—	-1	10	20	-1500	75	2N2869
2N331	1	Ge	11	-30	-12	-0.200	0.200	50	-16	71	2N1638
2N356	5	Ge	*	20	20	0.5	0.100	30	5	85	2N647
2N357	5	Ge	*	20	20	0.5	0.100	30	5	85	2N647
2N358	5	Ge	*	20	20	0.5	0.100	30	5	85	2N647
2N371	3	Ge	9	-24	-0.5	-0.010	0.08	80	-20	71	—
2N373	3	Ge	9	-25	-0.5	-0.010	0.080	60	-8	71	2N1638
2N374	3	Ge	9	-25	-0.5	-0.010	0.080	60	-8	71	2N1631
2N395	17	Ge	5	-30	-20	-0.2	0.15	10	-6	85	—
2N396A	17	Ge	5	-30	-20	-0.2	0.20	15	-6	85	—
2N397	17	Ge	5	-30	-20	-0.2	0.20	20	-6	85	—
2N441	2	Ge	14	-40	-20	-15	150	20	-4000	100	—
2N442	2	Ge	14	-50	-30	-15	150	20	-4000	100	—
2N443	2	Ge	14	-60	-40	-15	150	20	-4000	100	—
2N456	4	Ge	25	-40	-20	-5	50	52	—	95	2N2869
2N457	4	Ge	25	-60	-20	-5	50	52	—	95	2N2869
2N497	6	Si	5	60	8	—	4	12	10	200	—
2N544	3	Ge	9	-18	-1	-0.010	0.080	60	-4	71	2N217
2N561	4	Ge	25	-80	-60	-10	50	75	—	100	2N2869
2N578	1	Ge	11	-20	-12	-0.400	0.120	10	-5	71	2N412
2N579	1	Ge	11	-20	-12	-0.400	0.120	20	-5	71	2N412
2N580	1	Ge	11	-20	-12	-0.400	0.120	30	-5	71	2N412
2N583	1	Ge	1	-18	-10	-0.100	0.120	20	-10	85	2N412
2N584	1	Ge	1	-25	-12	-0.100	0.120	40	-5	85	2N408
2N640	3	Ge	9	-34	-1	-0.010	0.080	50	-5	71	2N1637
2N641	3	Ge	9	-34	-1	-0.010	0.080	50	-7	71	2N1638
2N642	3	Ge	9	-34	-1	-0.010	0.080	50	-7	71	2N1639
2N643	1	Ge	11	-30	-2	-0.100	0.120	20	-10	71	—

* 1 - emitter, 2 - base, 3 - collector.
 ‡ For terminal connections diagrams, see page 557.

CHART OF DISCONTINUED TRANSISTORS (cont'd)

BIPOLAR TYPES (cont'd)

RCA Type	Bas- \ddagger ing	Material	Outline	MAXIMUM RATINGS				CHARACTERISTICS		Maximum Operating Temperature (°C)	Can be replaced by RCA type
				V _{CB} (volts)	V _{EB} (volts)	I _C (amperes)	P _T (watts)	Min. h _{FE}	I _{CB} (μA)		
2N644	1	Ge	11	-30	-2	-0.100	0.100	20	-10	71	—
2N645	1	Ge	11	-30	-2	-0.100	0.120	20	-10	71	—
2N656	6	Si	5	60	8	—	4	30	10	200	—
2N696	6	Si	5	60	5	-0.500	2	20	1	175	—
2N705	7	Ge	12	-15	-3.5	-0.05	0.15	25	-3	100	—
2N708	6	Si	12	40	—	—	0.36	15	0.025	200	—
2N710	7	Ge	12	-15	-2	-0.05	0.15	25	-3	100	—
2N711	7	Ge	12	-12	-1	-0.1	0.15	20	-3	100	—
2N794	7	Ge	12	-13	-1	-0.100	0.150	30	-3	85	2N1300
2N795	7	Ge	12	-13	-4	-0.100	0.150	30	-3	85	2N1301
2N796	7	Ge	12	-13	-4	-0.100	0.150	50	-3	85	2N1683
2N828	7	Ge	12	-15	-2.5	-0.2	0.3	25	-3	100	—
2N914	6	Si	12	40	—	—	0.36	10	0.025	200	—
2N955	6	Ge	12	12	2	0.1	0.15	30	5	100	—
2N955A	6	Ge	12	12	2	0.15	0.15	30	5	100	—
2N960	7	Ge	12	-15	-2.5	-0.1	0.3	20	-3	100	—
2N961	7	Ge	12	-12	-2	-0.1	0.3	20	-3	100	—
2N962	7	Ge	12	-12	-1.25	-0.1	0.3	20	-3	100	—
2N963	7	Ge	12	-12	-1.25	-0.1	0.3	20	-5	100	—
2N964	7	Ge	12	-15	-2.5	-0.1	0.3	40	-3	100	—
2N965	7	Ge	12	-12	-2	-0.1	0.3	40	-3	100	—
2N966	7	Ge	12	-12	-1.25	-0.1	0.3	40	-3	100	—
2N967	7	Ge	12	-12	-1.25	-0.1	0.3	40	-5	100	—
2N1014	4	Ge	25	-100	-60	-10	50	75	—	100	2N2869
2N1067	8	Si	10	60	12	0.5	5	35	15	175	2N3053
2N1068	8	Si	10	60	12	1.5	10	38	15	175	2N3262
2N1069	9	Si	2	60	1.7	4	50	20	25	175	2N1489
2N1070	9	Si	2	60	9	4	50	20	25	175	2N1702
2N1092	6	Si	5	60	12	0.5	2	35	15	175	—
2N1099	2	Ge	14	-80	-40	-15	150	35	-4000	100	—
2N1100	2	Ge	14	-100	-80	-15	150	25	-4000	100	—
2N1169	2	Ge	5	25	25	0.4	0.12	20	10	71	—
2N1170	10	Ge	5	40	40	0.4	0.12	20	8	71	—
2N1213	7	Ge	5	-25	-1	-0.100	0.075	—	-3	85	—
2N1214	10	Ge	5	-25	-1	-0.100	0.075	—	-3	85	—
2N1215	10	Ge	5	-25	-1	-0.100	0.075	—	-3	85	—
2N1216	10	Ge	5	-25	-1	-0.100	0.075	—	-3	85	—
2N1319	10	Ge	5	-20	-20	-0.4	0.12	15	-6	71	—
2N1358	2	Ge	14	-80	-60	-15	150	25	-200	100	—
2N1384	10	14	Ge	-30	-1	-0.5	0.24	20	-8	85	—

‡ For terminal connections diagrams, see page 557.

CHART OF DISCONTINUED TRANSISTORS (cont'd)

BIPOLAR TYPES (cont'd)

RCA Type	Bas- ing ‡	Mate- rial	Out- line	MAXIMUM RATINGS				CHARACTER- ISTICS		Maximum Operating Tempera- ture (°C)	Can be replaced by RCA type
				V _{CB} (volts)	V _{EB} (volts)	I _C (amperes)	P _T (watts)	Min. h _{FE}	I _{CB} (μA)		
2N1412	2	Ge	14	-100	-80	-15	150	25	-4000	100	—
2N1425	3	Ge	9	-24	-0.5	-0.010	0.080	50	-12	71	2N1638
2N1426	3	Ge	9	-24	-0.5	-0.010	0.080	130	-12	71	2N1638
2N1450	1	Ge	11	-30	-1	-0.100	0.120	20	-10	85	2N217
2N1511	11	Si	14	60	60	6	75	15	25	200	2N1487
2N1512	11	Si	14	100	100	6	75	15	25	200	2N1488
2N1513	11	Si	14	60	60	6	75	15	25	200	2N1489
2N1514	11	Si	14	100	100	6	75	15	25	200	2N1490
2N1633	12	Ge	16	-34	-0.5	-0.010	0.080	75	-16	85	2N1638
2N1634	1	Ge	1	-34	-0.5	-0.010	0.080	75	-16	85	2N1638
2N1635	12	Ge	16	-34	-0.5	-0.010	0.080	75	-16	85	2N1638
2N1636	1	Ge	1	-34	-0.5	-0.010	0.080	75	-16	85	2N1638
2N1708	6	Si	12	25	3	0.2	0.3	20	0.025	175	—
2N1768	23	Si	22	60	12	3	40	35	15	200	2N1485
2N1769	23	Si	22	100	12	3	40	35	15	200	2N1486
2N2205	6	Si	12	25	—	0.2	0.3	20	0.025	175	—
2N2206	6	Si	19	25	3	0.2	1	40	0.025	175	—
2N2273	7	Ge	12	-25	-1	-0.1	0.1	20	-10	100	2N1179
2N2339	23	Si	22	60	40	2.5	40	20	3000	200	2N1701
2N2482	6	Ge	12	20	3	0.1	0.15	25	5	100	—
2N2873	13	Ge	1	-35	-0.1	-0.010	0.115	40	12	100	—
2N2898	6	Si	19	120	7	1	1.8	40	0.002	200	—
2N2899	6	Si	19	140	7	1	1.8	60	0.01	200	—
2N2900	6	Si	19	60	7	1	1.8	50	0.05	200	—
2N2938	6	Si	21	25	—	0.5	0.3	25	0.025	175	—
2N3230	25	Si	30	80	10	7	25	1000	—	200	—
2N3231	25	Si	30	100	10	7	25	1000	—	200	—
2N3241	8	Si	32	30	5	0.1	2	50	0.1	175	2N3241A
2N3242	8	Si	32	30	5	0.2	2	75	0.01	175	2N3242A
2N3435	6	Si	5	80	4	0.25	1	50	0.05	200	—
2N4081	18	Si	31	40	3	—	0.2	40	0.02	200	—
2N4395	9	Si	2	60	4	5	62.5	20	100	150	—
2N4396	9	Si	2	80	4	5	62.5	20	100	150	—
2N4397	18	Si	31	40	3	—	0.2	40	0.02	200	—
2N5017	—	Si	49	—	4	4.5	30	—	—	200	—
3746	—	Ge	17	-34	-0.5	-0.20	0.080	—	-16	85	—
3907/ 2N404	10	Ge	5	-25	-12	-0.2	0.15	30	-5	85	—
40217	6	Si	21	25	3	—	0.3	20	0.5	175	—
40218	6	Si	21	25	5	50	0.3	20	0.5	175	—
40219	6	Si	21	40	—	—	0.36	15	0.025	200	—
40220	6	Si	21	40	5	0.2	0.3	25	0.5	175	—
40221	6	Si	21	40	—	—	0.36	10	0.025	200	—
40222	6	Si	21	25	—	0.2	0.3	20	0.025	175	—

‡ For terminal connections diagrams, see page 557.

CHART OF DISCONTINUED TRANSISTORS (cont'd)

BIPOLAR TYPES (cont'd)

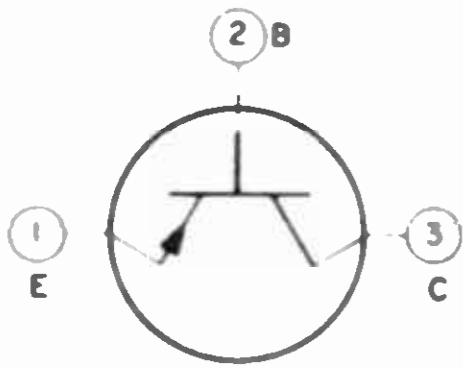
RCA Type	Bas- \ddagger ing	Material	Out-line	MAXIMUM RATINGS				CHARACTERISTICS		Maximum Operating Temperature (°C)	Can be replaced by RCA type
				V _{CB} (volts)	V _{EB} (volts)	I _C (amperes)	P _T (watts)	Min. h _{FE}	I _{CB} (μA)		
40255	14	Si	5	450	7	1	10	30	—	200	—
40256	14	Si	5	300	7	1	10	30	—	200	—
40264	24	Si	34	300	3	0.1	4	30	100	150	—
40269	10	Ge	5	-25	-12	0.1	0.15	50	-5	85	—
40283	6	Si	19	60	5	—	0.4	10	—	200	—
40350	15	Si	31	35	—	0.025	0.18	40	1	175	—
40351	15	Si	31	35	—	0.025	0.18	40	1	175	—
40352	15	Si	31	35	—	0.025	0.18	27	1	175	—
40403	19	Ge	5	-30	-20	-0.2	0.2	15	-6	85	—
40404	6	Si	21	40	5	0.5	1	25	0.025	175	—
40422	9	Si	25	300	2	0.15	8	50	100	150	—
40423	9	Si	27	300	2	0.15	3.8	50	100	150	—
40424	9	Si	25	300	2	0.15	8	30	100	150	—
40425	9	Si	27	300	2	0.15	3.8	30	100	150	—
40426	9	Si	25	300	2	0.15	8	20	100	150	—
40427	9	Si	27	300	2	0.15	3.8	20	100	150	—
40444	9	Si	2	120	7	20	140	20	—	200	—
40457	6	Si	32	—	7	1	0.5	30	0.5	175	—
40464	9	Si	2	35	4	5	40	30	250	150	—
40465	9	Si	2	40	4	5	40	70	0.1	150	—
40466	9	Si	2	50	4	5	40	50	100	150	—
40469	18	Si	31	45	3	0.05	0.18	40	0.02	175	—
40470	18	Si	31	45	3	0.05	0.18	40	0.02	175	—
40471	18	Si	31	45	3	0.05	0.18	27	0.02	175	—
40500	6	Si	31	7.5	7.5	0.2	2	50	0.1	175	—
40501	20	Si	33	7.5	7.5	0.2	1	50	0.1	175	—
40546	9	Si	25	—	—	0.15	8	50	100	150	—
40547	9	Si	25	—	—	0.15	8	20	100	150	—

MOS FIELD-EFFECT TYPES

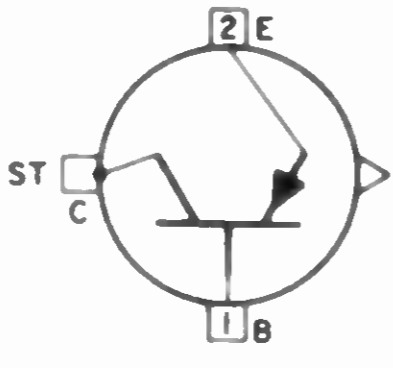
RCA Type	Bas- \ddagger ing	Material	Out-line	MAXIMUM RATINGS			CHARACTERISTICS			Maximum Operating Temperature (°C)	Can be replaced by RCA type
				I _D (mA)	V _{DS} (volts)	P _T (watts)	Y _{fs} (μmhos)	I _{DS(off)} (pA)	r _{DS(on)} (ohms)		
3N98	16	Si	28	15	32	0.15	1500	50	900	85	—
3N99	16	Si	28	15	32	0.15	2000	50	800	85	—
40460	21	Si	28	—	±25	0.15	3500	—	90	125	—
40461	21	Si	28	—	25	0.15	3500	—	—	125	—
40467	21	Si	31	—	0-20	0.1	7400	—	—	125	—

\ddagger For terminal connections diagrams, see page 557.

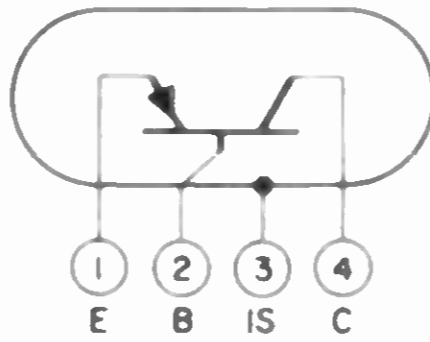
TERMINAL DIAGRAMS FOR DISCONTINUED TYPES



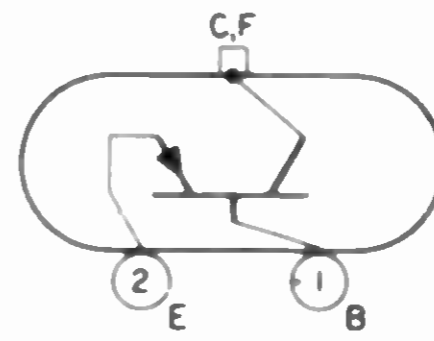
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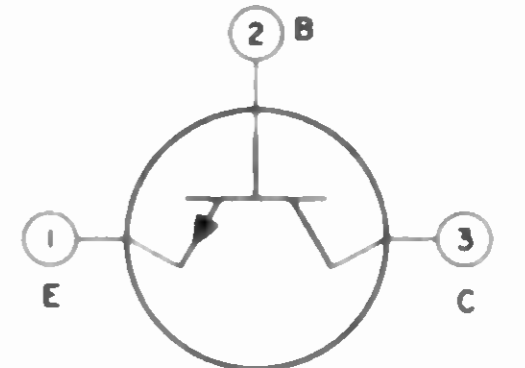
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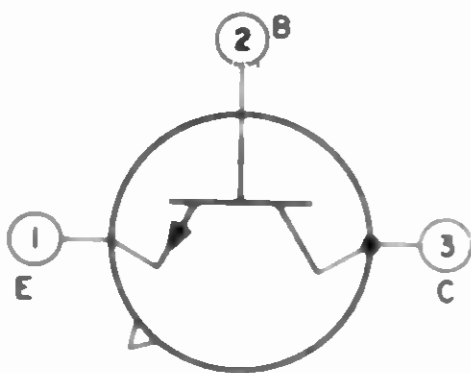
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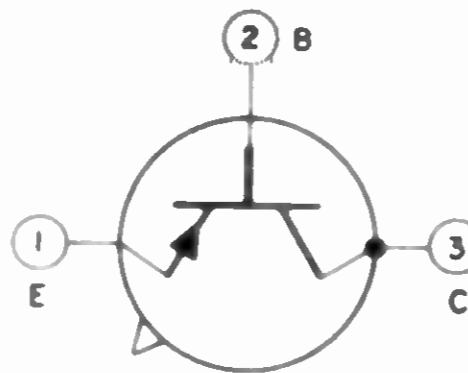
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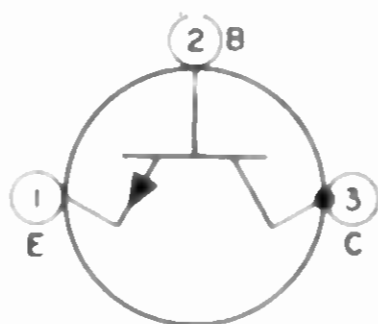
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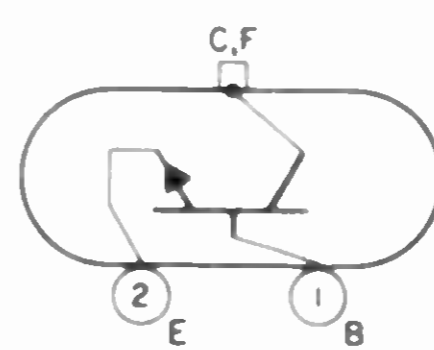
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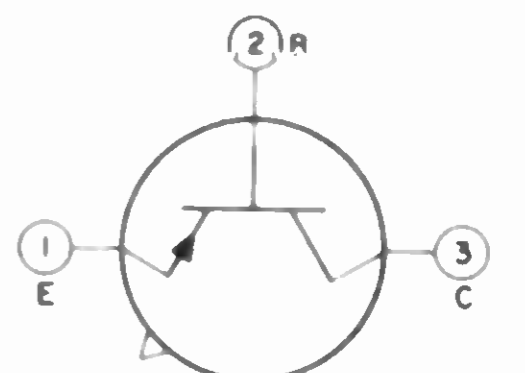
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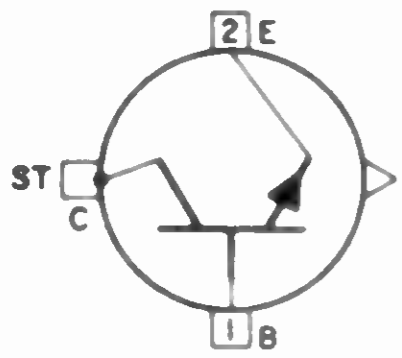
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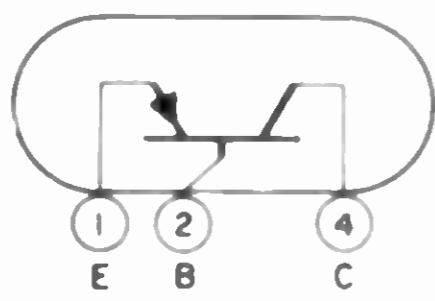
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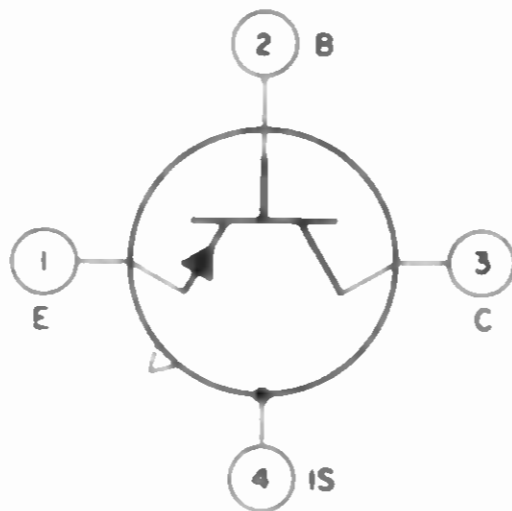
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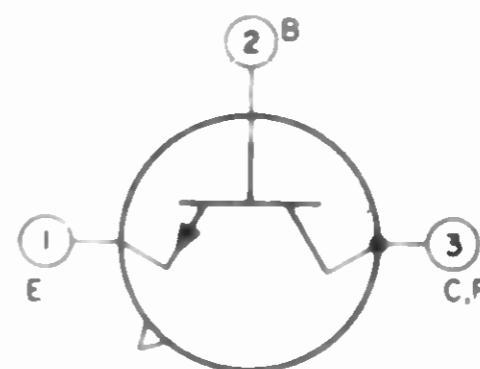
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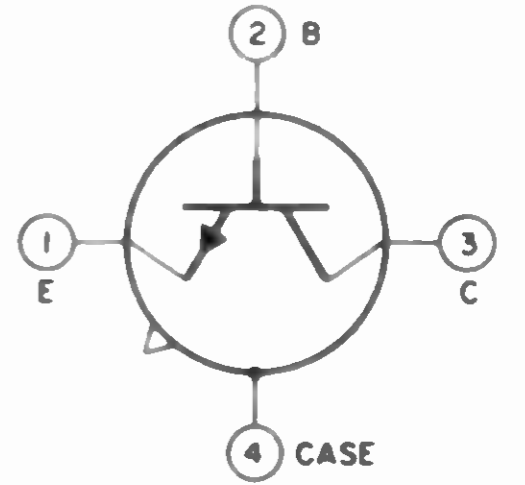
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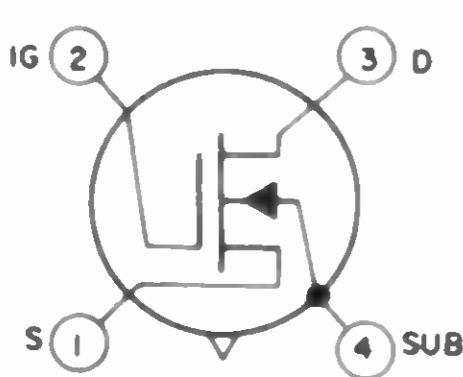
13



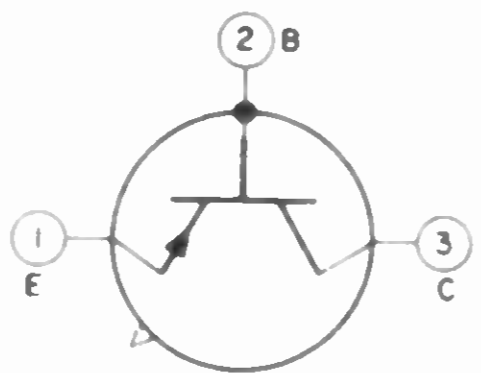
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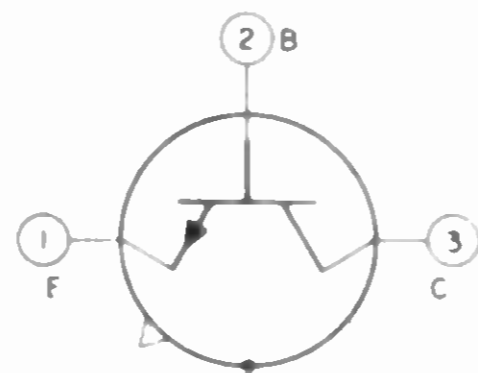
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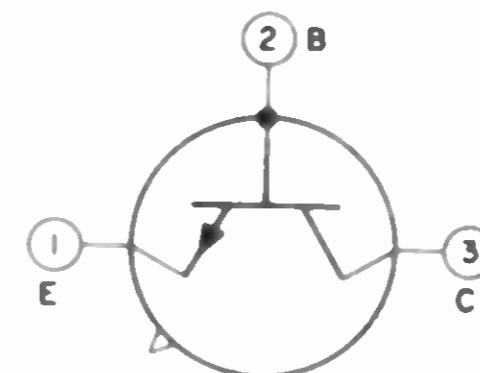
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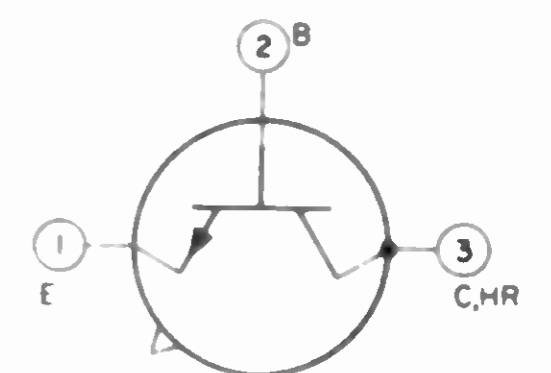
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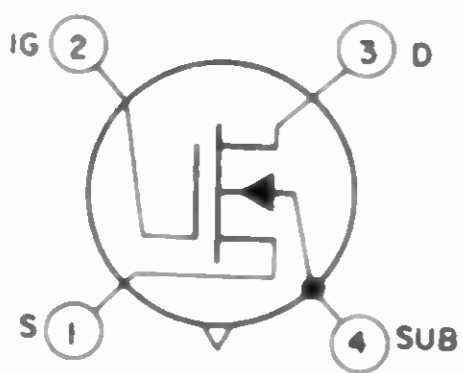
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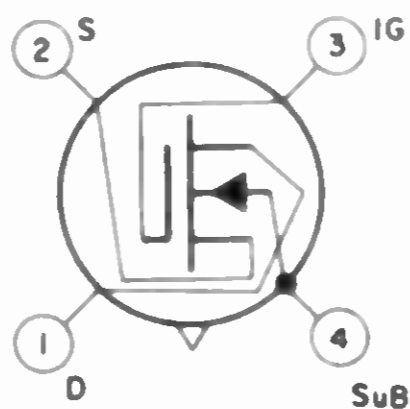
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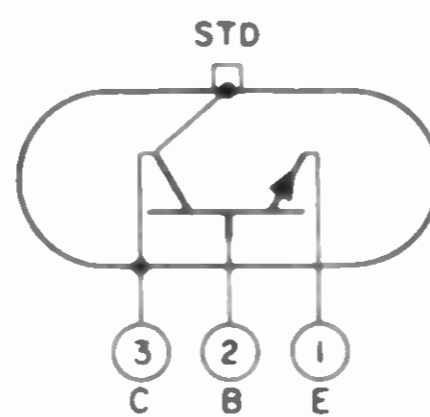
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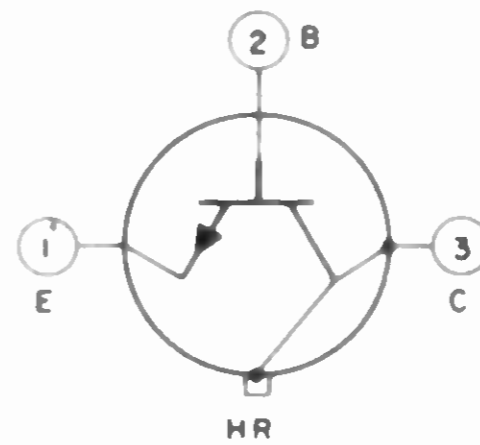
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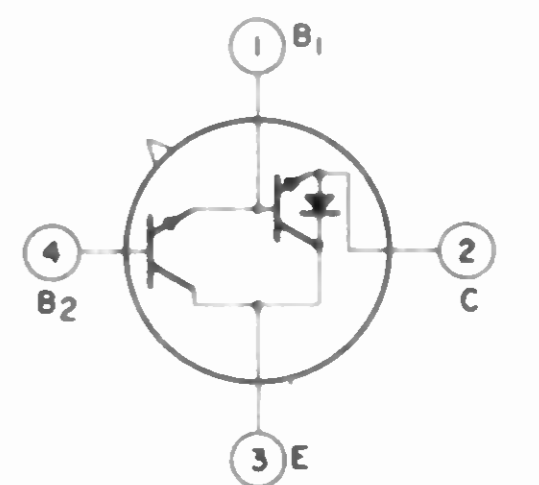
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Silicon Diffused-Junction Rectifiers

RCA TYPE	OUTLINE		MAXIMUM RATINGS					CHARAC- TERISTICS		
	JEDEC	NO.	I_{FAV} at T_C A	$^{\circ}C$	i_{FM} (rep) A	i_{FM} (surge) A	V_{RMS} V	V_{RM} and V_M (block) V	V_{FM} V	I_{RM} (dynamic) mA
1N248C [■]	D0-5	43	20	150	90	350	39	55 [▲]	0.6	3.8
1N249C [■]	D0-5	43	20	150	90	350	77	110 [▲]	0.6	3.6
1N250C [■]	D0-5	43	20	150	90	350	154	220 [▲]	0.6	3.4
1N440B	D0-1	38	0.75	50	3.5	15	70	100	1.5	0.3 [●]
1N441B	D0-1	38	0.75	50	3.5	15	140	200	1.5	0.75 [●]
1N442B	D0-1	38	0.75	50	3.5	15	210	300	1.5	1 [●]
1N443B	D0-1	38	0.75	50	3.5	15	280	400	1.5	1.5 [●]
1N444B	D0-1	38	0.65	50	3.5	15	350	500	1.5	1.75 [●]
1N445B	D0-1	38	0.65	50	3.5	15	420	600	1.5	2 [●]
1N536	D0-1	38	0.75	50	—	15	35	50	1.1	5 [●]
1N537	D0-1	38	0.75	50	—	15	70	100	1.1	5 [●]
1N538	D0-1	38	0.75	50	—	15	140	200	1.1	5 [●]
1N539	D0-1	38	0.75	50	—	15	210	300	1.1	5 [●]
1N540	D0-1	38	0.75	50	—	15	280	400	1.1	5 [●]
1N547	D0-1	38	0.75	50	—	15	420	600	1.2	5 [●]
1N1095	D0-1	38	0.75	50	—	15	350	500	1.2	5 [●]
1N1183A [■]	D0-5	43	40	150	195	800	35	50	0.65	2.5
1N1184A [■]	D0-5	43	40	150	195	800	70	100	0.65	2.5
1N1186A [■]	D0-5	43	40	150	195	800	140	200	0.65	2.5
1N1187A [■]	D0-5	43	40	150	195	800	212	300	0.65	2.5
1N1188A [■]	D0-5	43	40	150	195	800	284	400	0.65	2.2
1N1189A [■]	D0-5	43	40	150	195	800	355	500	0.65	2
1N1190A [■]	D0-5	43	40	150	195	800	424	600	0.65	1.8
1N1195A [■]	D0-5	43	20	150	90	350	212	300	0.6	3.2
1N1196A [■]	D0-5	43	20	150	90	350	284	400	0.6	2.5
1N1197A [■]	D0-5	43	20	150	90	350	355	500	0.6	2.2
1N1198A [■]	D0-5	43	20	150	90	350	424	600	0.6	1.5
1N1199A [■]	D0-4	42	12	150	50	240	35	50	0.55	3
1N1200A [■]	D0-4	42	12	150	50	240	70	100	0.55	2.5
1N1202A [■]	D0-4	42	12	150	50	240	140	200	0.55	2
1N1203A [■]	D0-4	42	12	150	50	240	212	300	0.55	1.75
1N1204A [■]	D0-4	42	12	150	50	240	284	400	0.55	1.5
1N1205A [■]	D0-4	42	12	150	50	240	355	500	0.55	1.25
1N1206A [■]	D0-4	42	12	150	50	240	424	600	0.55	1
1N1341B [■]	D0-4	42	6	150	25	160	35	50	0.65	0.45
1N1342B [■]	D0-4	42	6	150	25	160	70	100	0.65	0.45
1N1344B [■]	D0-4	42	6	150	25	160	140	200	0.65	0.45
1N1345B [■]	D0-4	42	6	150	25	160	212	300	0.65	0.45
1N1346B [■]	D0-4	42	6	150	25	160	284	400	0.65	0.45
1N1347B [■]	D0-4	42	6	150	25	160	355	500	0.65	0.45
1N1348B [■]	D0-4	42	6	150	25	160	424	600	0.65	0.45
1N1612 [■]	D0-4	42	5	135	15	—	35	50	1.5	1
1N1613 [■]	D0-4	42	5	135	15	—	70	100	1.5	1
1N1614 [■]	D0-4	42	5	135	15	—	140	200	1.5	1
1N1615 [■]	D0-4	42	5	135	15	—	280	400	1.5	1

■ Reverse-polarity version available.

▲ V_M (block) is 10% less.

● Static value in μA .

Silicon Diffused-Junction Rectifiers (cont'd)

RCA TYPE	OUTLINE		MAXIMUM RATINGS				CHARACTERISTICS			
	JEDEC	NO.	I_{FAV} at T_c A	$^{\circ}C$	i_{FM} (rep) A	i_{FM} (surge) A	V_{RMS} V	V_{RM} and V_M (block) V	V_{FM} V	I_{RM} (dynamic) mA
1N1616 [■]	D0-4	42	5	135	15	—	420	600	1.5	1
1N1763A	D0-1	38	1	75	5	35	280	400	1.2	0.1
1N1764A	D0-1	38	1	75	5	35	350	500	1.2	0.1
1N2858A	D0-1	38	1	75	5	35	35	50	1.2	0.1
1N2859A	D0-1	38	1	75	5	35	70	100	1.2	0.1
1N2860A	D0-1	38	1	75	5	35	140	200	1.2	0.1
1N2861A	D0-1	38	1	75	5	35	210	300	1.2	0.1
1N2862A	D0-1	38	1	75	5	35	280	400	1.2	0.1
1N2863A	D0-1	38	1	75	5	35	350	500	1.2	0.1
1N2864A	D0-1	38	1	75	5	35	420	600	1.2	0.1
1N3193	TO-1 [‡]	39	0.5*	75	6*	35*	140	200	1.2	0.2
1N3194	TO-1 [‡]	39	0.5*	75	6*	35*	280	400	1.2	0.2
1N3195	TO-1 [‡]	39	0.5*	75	6*	35*	420	600	1.2	0.2
1N3196	TO-1 [‡]	39	0.4*	75	5*	35*	560	800	1.2	0.2
1N3253	TO-1 [°]	40	Insulated version of 1N3193							
1N3254	TO-1 [°]	40	Insulated version of 1N3194							
1N3255	TO-1 [°]	40	Insulated version of 1N3195							
1N3256	TO-1 [°]	41	Insulated version of 1N3196							
1N3563	TO-1 [°]	40	0.3*	75	4*	35*	700	1000	1.2	0.2
1N3754	TO-1 ^{**}	41	0.125	65	1.3	30	35	100	1	0.3
1N3755	TO-1 ^{**}	41	0.125	65	1.3	30	70	200	1	0.3
1N3756	TO-1 ^{**}	41	0.125	65	1.3	30	140	400	1	0.3
40108 [■]	D0-4	42	10	150	40	140	—	50	0.6	2
40109 [■]	D0-4	42	10	150	40	140	—	100	0.6	2
40110 [■]	D0-4	42	10	150	40	140	—	200	0.6	1.5
40111 [■]	D0-4	42	10	150	40	140	—	300	0.6	1.5
40112 [■]	D0-4	42	10	150	40	140	—	400	0.6	1
40113 [■]	D0-4	42	10	150	40	140	—	500	0.6	0.85
40114 [■]	D0-4	42	10	150	40	140	—	600	0.6	0.75
40115 [■]	D0-4	42	10	150	40	140	—	800	0.6	0.65
40208 [■]	D0-5	43	18	150	72	250	—	50	0.65	3
40209 [■]	D0-5	43	18	150	72	250	—	100	0.65	3
40210 [■]	D0-5	43	18	150	72	250	—	200	0.65	2.5
40211 [■]	D0-5	43	18	150	72	250	—	300	0.65	2.5
40212 [■]	D0-5	43	18	150	72	250	—	400	0.65	2
40213 [■]	D0-5	43	18	150	72	250	—	500	0.65	1.75
40214 [■]	D0-5	43	18	150	72	250	—	600	0.65	1.5
40259	D0-4	42	12	150	50	250	424	600	0.55	0.6
40265	TO-1 ^{**}	41	0.125	65	1.3	30	140	400	1	0.4
40266	D0-1	38	2*	105	10	35	35	100	3	10 [†]
40267	D0-1	38	2*	105	10	35	70	200	3	10 [†]
40642	D0-26	40	1	—	6.5	70	—	700 [▲]	2	10 [Ⓞ]
40643	D0-26	40	1	—	6	10	—	800 [●]	1.3	10 [Ⓞ]
40644	D0-26	40	1	—	0.3	20	—	700 [▲]	1.3	10 [Ⓞ]

[■] Reverse-polarity version available. † Value in μA . ▲ $V_{RM}(\text{block}) = 550V$.
[‡] Similar to TO-1 package with axial leads. ● $V_{RM}(\text{block}) = 450V$. Ⓞ Static condition.
[°] Similar to TO-1 package with axial leads and insulated plastic sleeve over metal case.
^{**} Similar to TO-1 package with lead 3 omitted. * With capacitive load.

Silicon Diffused-Junction Stack Rectifiers

RCA TYPE	OUTLINE NO.	MAXIMUM RATINGS						CHARACTERISTICS		
		I_{FAV} at 100°C A	i_{FM} (rep) A	i_{FM} (surge) A	V V_{RMS}	V_{RM} (rep) and V_M (block) V	$V_{RM}\ddagger$ (non- rep) V	$V_{FM}\blacksquare$	$I_{RM}\blacksquare$ (dynamic) A	C_s (max) pF
CR101	44a	0.385	5	20	895	1265	1520	1.2	0.3	600
CR102	44b	0.355	5	20	1790	2530	3035	2.4	0.3	320
CR103	44c	0.315	5	20	2240	3165	3800	3	0.3	250
CR104	44d	0.270	5	20	3130	4430	5315	4.2	0.3	175
CR105	44e	0.270	5	20	3580	5065	6080	4.8	0.3	160
CR106	44f	0.250	5	20	4475	6330	7600	6	0.3	125
CR107	44g	0.230	5	20	5370	7595	9115	7.2	0.3	105
CR108	44h	0.230	5	20	5820	8230	9875	7.8	0.3	100
CR109	44i	0.230	5	20	6710	9495	11395	9	0.3	90
CR110	44j	0.230	5	20	7160	10130	12155	9.6	0.3	80
CR201	45a	0.155	3	10	1345	1900	2280	1.8	0.1	—
CR203	45b	0.155	3	10	2240	3165	3800	3	0.1	—
CR204	45c	0.155	3	10	3395	4800	5760	3.6	0.1	—
CR206	45d	0.155	3	10	4475	6330	7600	6	0.1	—
CR208	45e	0.155	3	10	5655	8000	9600	6	0.1	—
CR210	45f	0.155	3	10	7070	10000	12000	7.2	0.1	—
CR212	45g	0.155	3	10	8485	12000	14400	9	0.1	—
CR301	46a	2.5	—	250	1695	2400	2880	—	1.5	**
CR302	46b	2.5	—	250	2545	3600	4320	—	1.5	**
CR303	46c	2.5	—	250	3395	4800	5760	—	1.5	**
CR304	46d	2.5	—	250	4240	6000	7200	—	1.5	**
CR305	46e	2.5	—	250	5090	7200	8640	—	1.5	**
CR306	46f	2.5	—	250	5935	8400	10080	—	1.5	**
CR307	46g	2.5	—	250	6785	9600	11520	—	1.5	**
CR311	46h	4.5	—	250	1695	2400	2880	—	1.5	**
CR312	46i	4.5	—	250	2545	3600	4320	—	1.5	**
CR313	46j	4.5	—	250	3395	4800	5760	—	1.5	**
CR314	46k	4.5	—	250	4240	6000	7200	—	1.5	**
CR315	46l	4.5	—	250	5090	7200	8640	—	1.5	**
CR316	46m	4.5	—	250	5935	8400	10080	—	1.5	**
CR317	46n	4.5	—	250	6785	9600	11520	—	1.5	**
CR321	46o	6	—	400	1695	2400	2880	—	1.5	**
CR322	46p	6	—	400	2545	3600	4320	—	1.5	**
CR323	46q	6	—	400	3395	4800	5760	—	1.5	**
CR324	46r	6	—	400	4240	6000	7200	—	1.5	**
CR325	46s	6	—	400	5090	7200	8640	—	1.5	**
CR331	46t	8.5	—	400	1695	2400	2880	—	1.5	**
CR332	46u	8.5	—	400	2545	3600	4320	—	1.5	**
CR333	46v	8.5	—	400	3395	4800	5760	—	1.5	**
CR334	46w	8.5	—	400	4240	6000	7200	—	1.5	**
CR335	46x	8.5	—	400	5090	7200	8640	—	1.5	**
CR341	46y	11.5	—	850	1695	2400	2880	—	1.5	**
CR342	46z	11.5	—	850	2545	3600	4320	—	1.5	**
CR343	46aa	11.5	—	850	3395	4800	5760	—	1.5	**
CR344	46bb	11.5	—	850	4240	6000	7200	—	1.5	**
CR351	46cc	17.5	—	850	1695	2400	2880	—	1.5	**
CR352	46dd	17.5	—	850	2545	3600	4320	—	1.5	**
CR353	46ee	17.5	—	850	3395	4800	5760	—	1.5	**
CR354	46ff	17.5	—	850	4240	6000	7200	—	1.5	**

‡ For duration of 5 ms max; $T_c = 60$ to 125°C .

■ At maximum rated operating conditions.

** C_s typically $0.01 \mu\text{F}$ per cell.

Silicon Plug-in Rectifiers

Silicon Bridge Rectifiers

RCA TYPE	OUTLINE NO.	AVERAGE DC OUTPUT		RMS SUPPLY V
		A	V	
CR401†	46a	18	200	222
CR402†	46a	18	400	444
CR403†	46c	18	800	888
CR404†	46o	34	200	222
CR405†	46o	34	400	444
CR406†	46v	34	800	888
CR407†	46y	70	200	222
CR408†	46y	70	400	444
CR409†	46aa	70	800	888
CR501‡	46b	24	300	222
CR502‡	46b	24	600	444
CR503‡	46p	46	300	222
CR504‡	46p	46	600	444
CR505‡	46z	92	300	222
CR506‡	46z	92	600	441

These high-voltage diffused-junction types are direct replacements for the mercury-vapor and gas rectifier tubes indicated. Data for the tube-type rectifiers are given in the **RCA Transmitting Tube Manual TT-5**.

RCA TYPE	REPLACES TYPE(S)
CR273/8008	8008
CR274/872A	872, 872A
CR275/866A/3B28	866, 866A, 3B28

† Single-phase, full-wave types.
‡ Three phase, full-wave types

Photocells

RCA Type ^a	Out-line	Wave-length of Peak Response (angstroms)	MAXIMUM RATINGS				CHARACTERISTICS AT 25°C				
			Voltage Between Terminals DC or Peak AC (volts)	Power Dissipation ^b (watts)		Photo-current (mA)	Voltage Between Terminals (ac volts)	Illumination ^d (foot-candles)	Photocurrent ^c (mA)		Max. Decay Current ^e (μA)
				Continu-ous Service	Demand Service ^b				Min.	Max.	
SQ2503	61	5100	600	0.75	1	75	50	1	0.8	1.7	40
7163	61	5100	600	0.75	1	75	50	1	1	3	40
4448	61	5100	600	0.75	1	75	50	1	1.5	4	40
4404	61	5100	600	0.75	1	75	50	1	2.5	5	40
SQ2502 ^c	61	5100	600	0.75	1	75	50	1	2.5	5	40
4453	61	5100	600	0.75	1	75	50	1	3	7	40
4403	61	5100	350	0.75	1	100	50	1	8	16	78
SQ2546	61	6150	200	0.75	1	100	12 (dc)	1 ^h	5	15	5

RCA Type ^a	Out-line	Wave-length of Peak Response (angstroms)	MAXIMUM RATINGS				CHARACTERISTICS AT 25°C				
			Voltage Between Terminals DC or Peak AC (volts)	Power Dissipation ^b (watts)	Photo-current (mA)	Voltage Between Terminals (dc volts)	Illumination ^d (foot-candles)	Photocurrent ^c (mA)		Max. Decay Current ^e (μA)	
								Min.	Max.		
SQ2508	63	5100	300	0.075	10	12	1	0.065 ^e	0.275 ^e	1	
SQ2519	63	5100	300	0.075	20	12	10	1.6 ^{j, e}	— ^e	12	
SQ2520	62	5100	200	0.35	75	12	1	3.6	14.5	80	
SQ2521	62	5100	250	0.35	50	50 (ac)	1 ^h	1.5	4	40	

Photocells (cont'd)

RCA Type ^a	Out-line	Wave-length of Peak Response (angstroms)	MAXIMUM RATINGS			CHARACTERISTICS AT 25°C				
			Voltage Between Terminals DC or Peak AC (volts)	Power Dissipation ^b (watts)	Photo-current (mA)	Voltage Between Terminals (dc volts)	Illumination ^h (foot-candles)	Photocurrent (mA)		Max. Decay Current ^c (μA)
								Min.	Max.	
SQ2526	62	5100	200	0.35	75	12	1	1	3	80
SQ2527	62	5100	200	0.35	75	12	1	2	6	80
SQ2529	63	5100	300	0.075	3	12	1	0.004 ^e	0.012 ^e	0.1
SQ2534	63	5100	300	0.075	1	90	30	0.057 ^e	0.65 ^e	0.1
SQ2535	64	5100	200	0.03	10	12	10	0.8	2.5	12
SQ2536	63	5100	150	0.075	25	12	1	1 ^e	3 ^e	15
SQ2543	64	6150	100	0.03	15	12	1	0.45	1.35	0.5
SQ2544	63	6150	100	0.075	25	12	1	1.5 ^e	4.5 ^e	2
SQ2544V1	63	6150	150	0.075	25	12	1	0.6 ^e	1.8 ^e	2
SQ2545	62	6150	125	0.35	75	12	1	4	12	15
SQ2545V1	62	6150	200	0.35	75	12	1	2.5	7.5	7.5
SQ2554	63	5100	150	0.075	25	12	1	1.6 ^e	4.8 ^e	15
SQ2555	63	5100	200	0.075	15	12	10	1.4 ^e	2.75 ^e	12
SQ2556	62	5100	200	0.35	75	12	1	2	—	80
SQ2557	65	5100	100	0.075	5 ^m	12	1	0.033 ^m	0.13 ^m	5 ^m
SQ2558	65	5100	100	0.075	10 ^m	12	1	0.3 ^m	1.2 ^m	20 ^m

Tunnel Diodes

Electrical Characteristics (At T_A = 25°C)

RCA Type	Peak Forward Current (mA)	Max Valley Current (mA)	Min Peak-to-Valley Current Ratio	Peak Voltage (mV)	Min Valley Voltage (mV)	Forward Voltage (mV)	Max Capacitance* (pF)	Max Series Resistance (ohms)	Rise Time (ps) typ.
40561	4.5-5.5	0.75	6:1	—	—	430-590	25	3	1800
40562	9-11	1.5	6:1	—	—	440-600	25	2.5	900
40563	18-22	3	6:1	—	—	460-620	30	2	600
40564	45-55	7.5	6:1	—	—	530-640	40	1.5	350
40565	90-110	15	6:1	—	—	540-650	40	1	150
40566	4.75-5.25	0.6	8:1	50-90	305	490-560	15	3	1200
40567	9.5-10.5	1.2	8:1	55-95	325	510-580	15	2.5	600
40568	19-21	2.4	8:1	65-105	340	530-600	20	2	400
40569	47.5-52.5	6	8:1	80-130	355	550-620	25	1.5	200
40570	95-105	12	8:1	90-140	365	550-630	25	1	100
40571	4.75-5.25	0.6	8:1	50-90	305	490-560	8	3	600
40572	9.5-10.5	1.2	8:1	55-95	325	510-580	8	2.5	300
40573	19-21	2.4	8:1	65-105	340	530-600	10	2	200
40574	47.5-52.5	6	8:1	80-130	355	550-620	12	1.5	100

* Includes typical case capacitance of 0.8 pF.

- ^a The maximum ambient operating temperature range of the sensitive surface of these cells is -40°C to $+75^{\circ}\text{C}$.
- ^b With sensitive surface of cell fully illuminated. These dissipation ratings apply up to a case temperature of $+40^{\circ}\text{C}$ from which point the cells are derated linearly to 0 watts at $+75^{\circ}\text{C}$.
- ^c The demand rating is a dissipation rating to which the cell may be exposed in outdoor applications. The rating may be utilized twice every 24 hours for a period of 20 minutes each time provided the interval between demand period is not less than 4 hours.
- ^d For conditions where light flux from a tungsten-filament lamp operated at a color temperature of 2854°K is transmitted through a filter (Corning C.S. No. 1-62 which an effective transmission of luminous flux of 13.3%) onto the sensitive surface. The value of illumination incident on the sensitive surface is 7.5 footcandles measured before positioning the filter between the lamp and the

- cell. The sensitive surface of the cell is fully illuminated.
- ^e This characteristic is determined after the cell has been exposed for a period of 16 to 24 hours to 500 footcandle illumination (daylight fluorescent light).
- ^f Measured 10 seconds after removal of incident-illumination level.
- ^g Type SQ2502 is not recommended for new equipment design. It is identical with type 4404 except it is supplied with attached Intermediate-Shell Octal 5-pin base (JEDEC No.B5-10).
- ^h For conditions where the light source is a tungsten-filament lamp operated at a color temperature of 2854°K .
- ⁱ This characteristic is determined after the cell has been exposed for a period of 16 to 24 hours to 50 to 100 footcandle illumination (daylight fluorescent light).
- ^k The value shown is the total dissipation for both elements of the photocell.
- ^m The value shown applies for each element of the photocell.

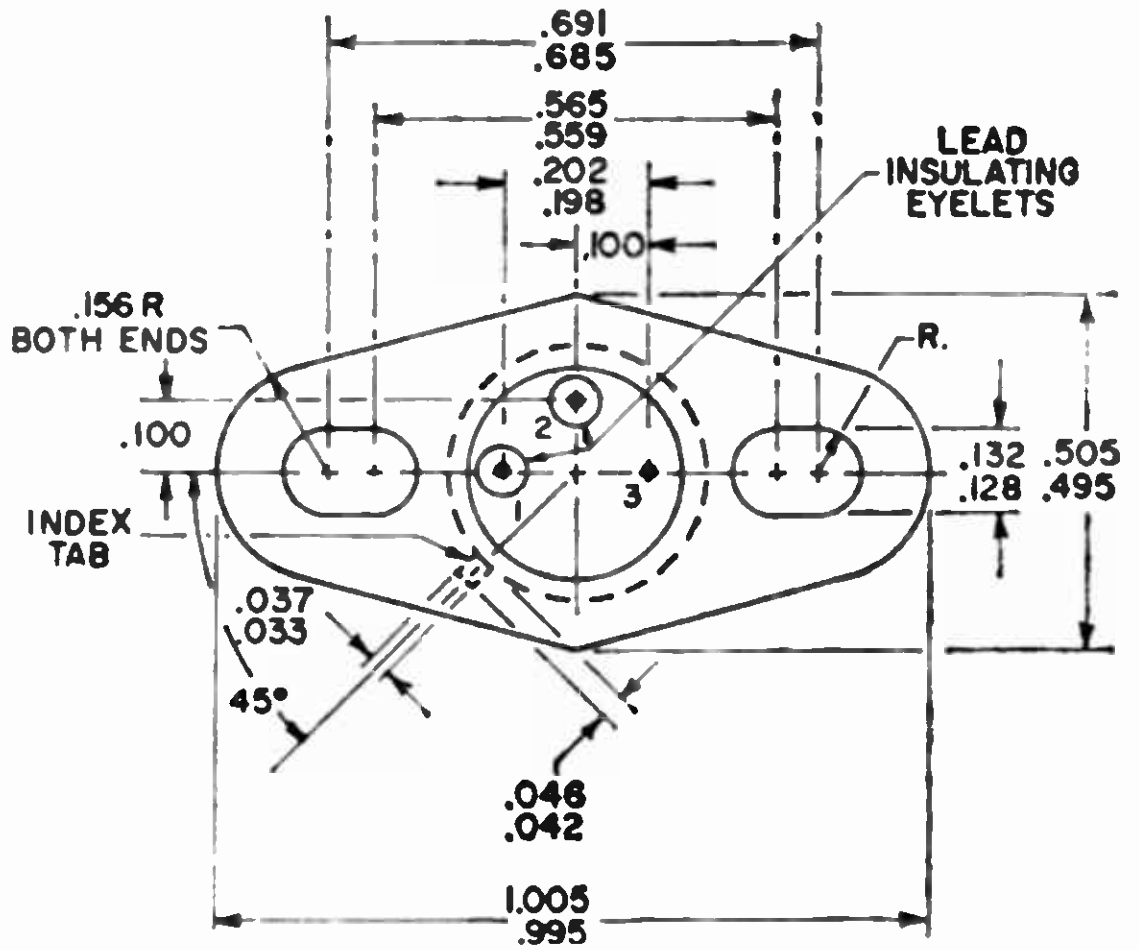
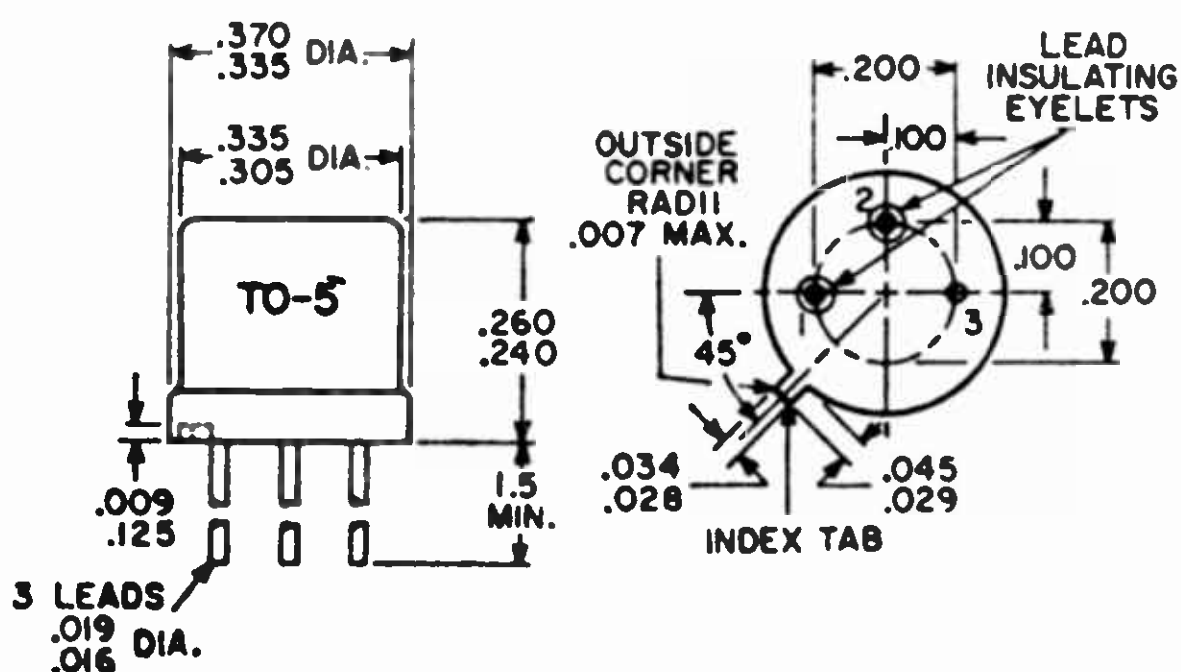
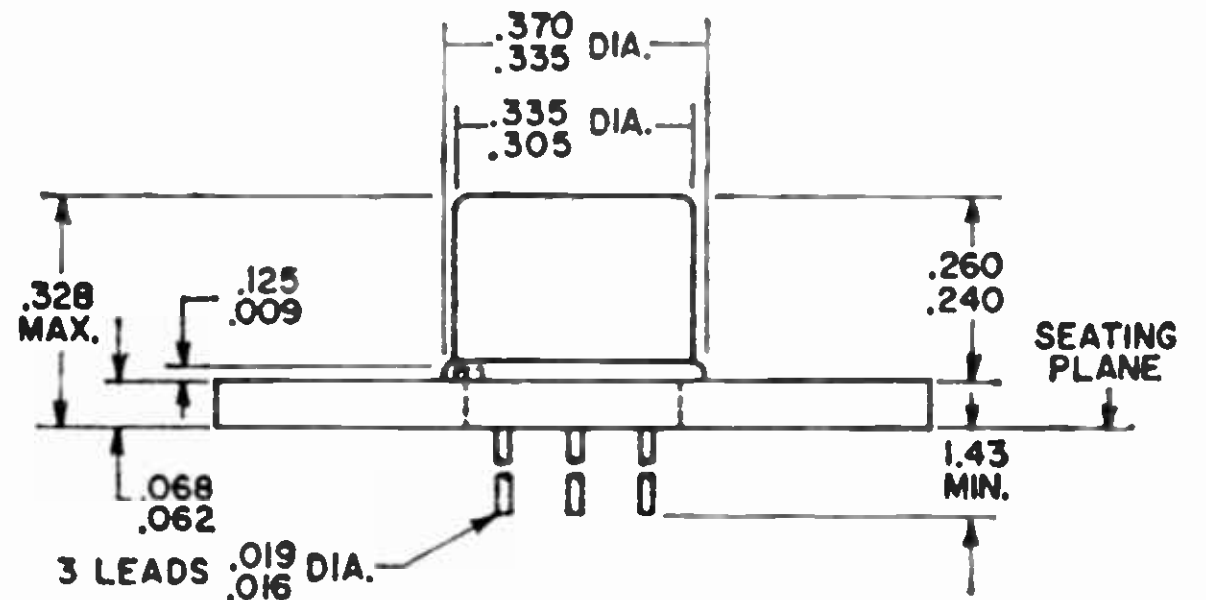
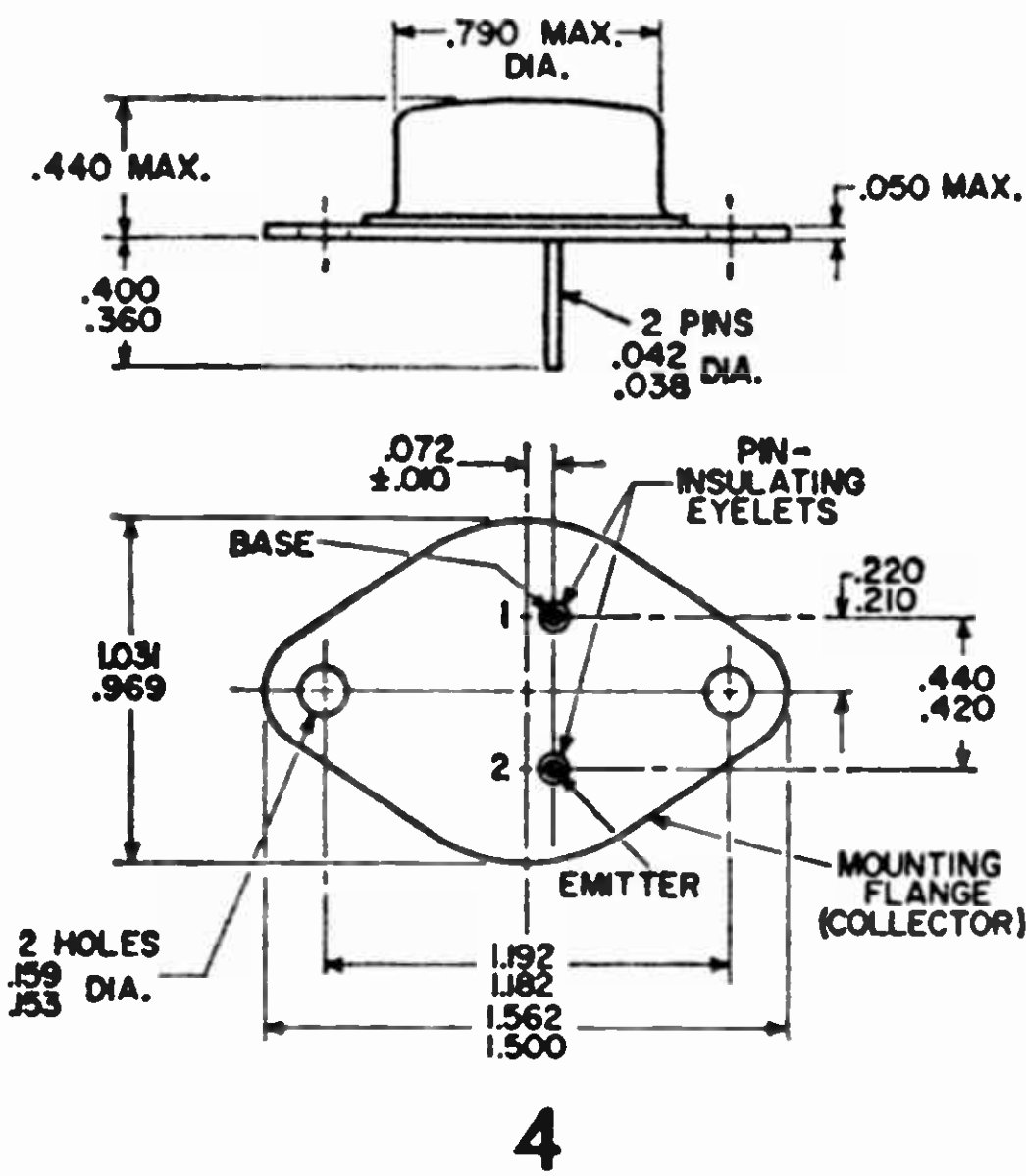
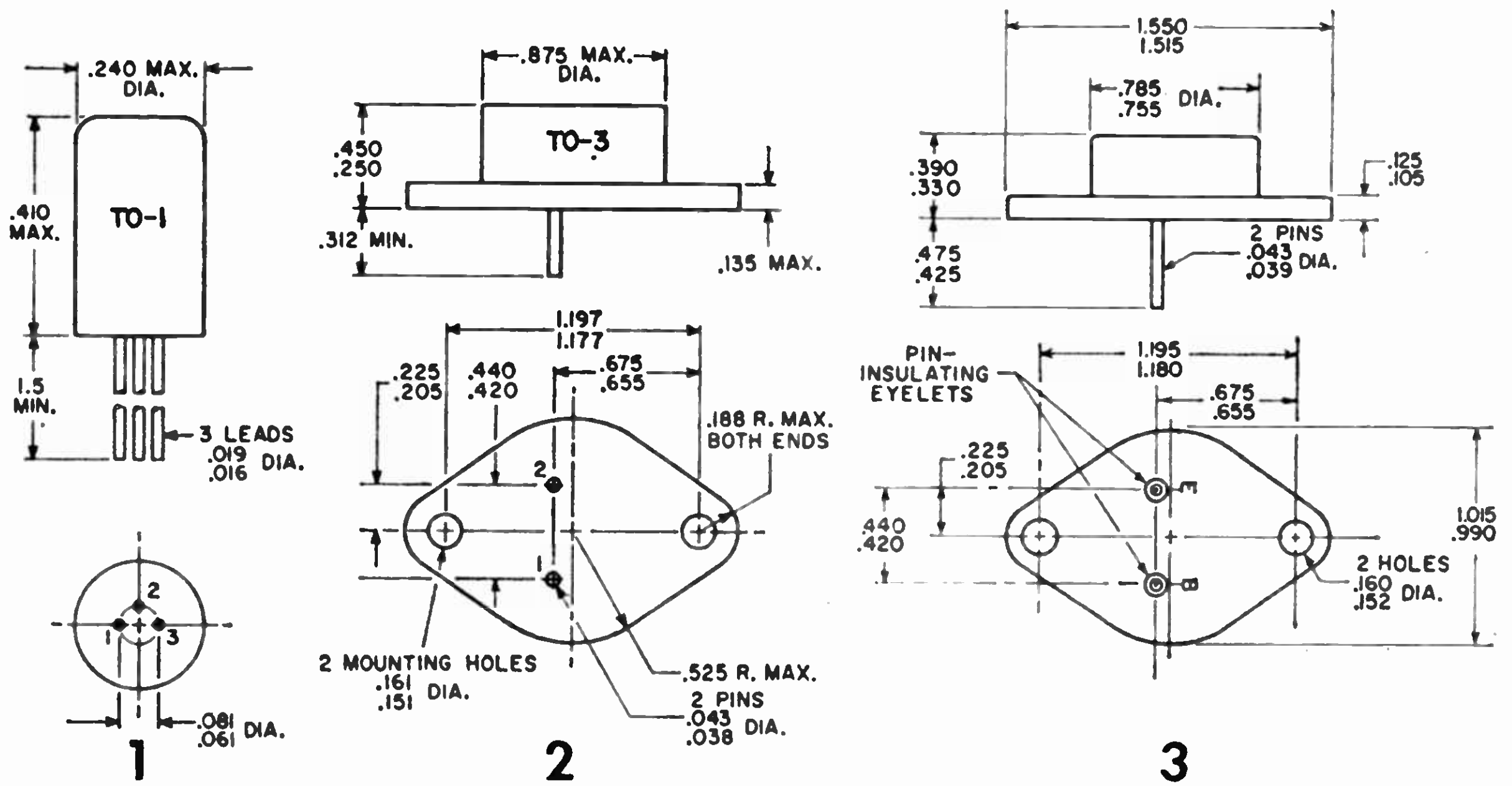
Tunnel Diodes

Maximum Ratings (At $T_A = 25^{\circ}\text{C}$)

DC Current (mA)		Dissipation ‡ (mW)	Ambient-Temperature ($^{\circ}\text{C}$) Range		Lead Temperature ($^{\circ}\text{C}$) (3 seconds maximum)	Material	Out-line	RCA Type
Forward	Reverse		Operating	Storage				
10	15	5	-35 to 100		175	Ge	48	40561
18	25	15	-35 to 100		175	Ge	48	40562
35	50	20	-35 to 100		175	Ge	48	40563
85	125	50	-35 to 100		175	Ge	48	40564
170	250	100	-35 to 100		175	Ge	48	40565
10	15	5	-35 to 100		175	Ge	48	40566
18	25	10	-35 to 100		175	Ge	48	40567
35	50	20	-35 to 100		175	Ge	48	40568
85	125	50	-35 to 100		175	Ge	48	40569
170	250	100	-35 to 100		175	Ge	48	40570
10	15	5	-35 to 100		175	Ge	48	40571
18	25	10	-35 to 100		175	Ge	48	40572
35	50	20	-35 to 100		175	Ge	48	40573
85	125	50	-35 to 100		175	Ge	48	40574

‡ Above 25°C , derate linearly to 0 mW at $T_A = 100^{\circ}\text{C}$.

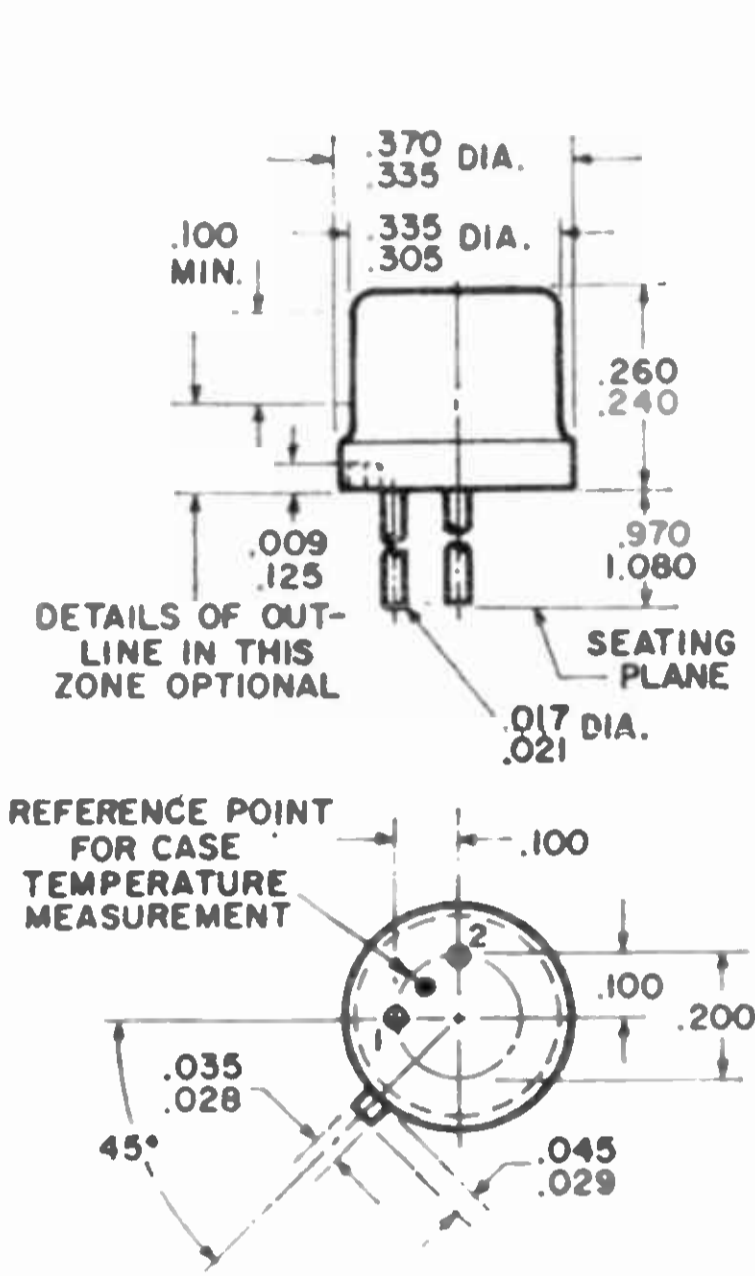
Outlines



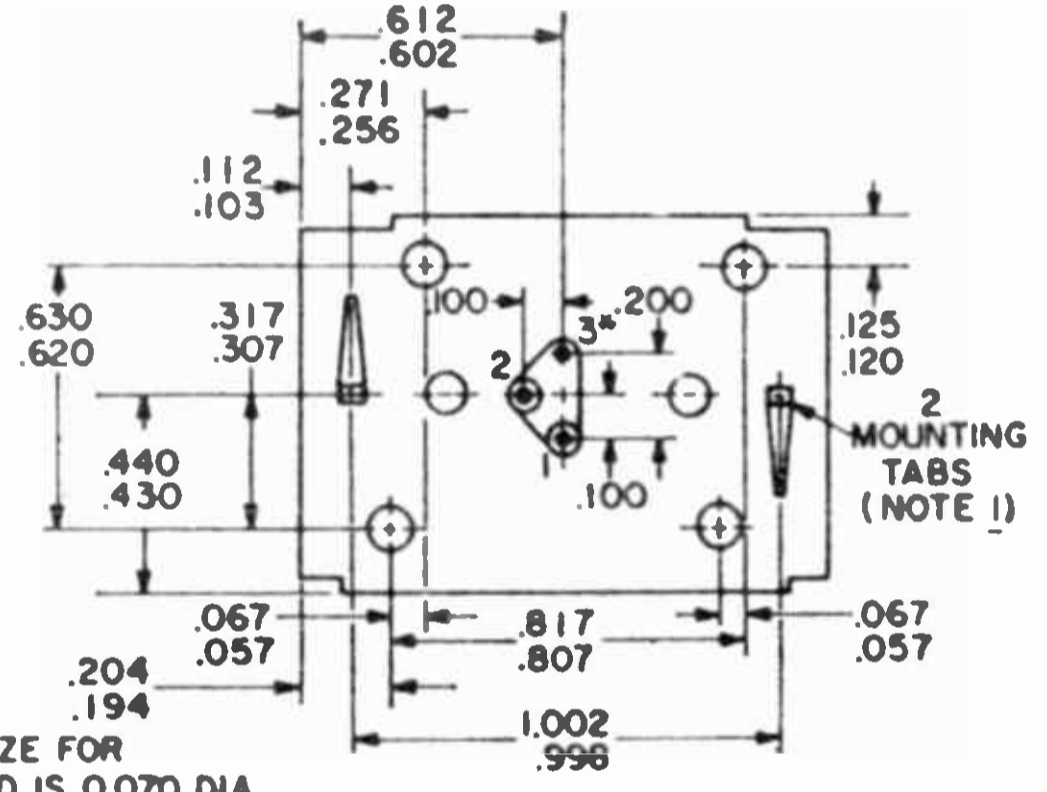
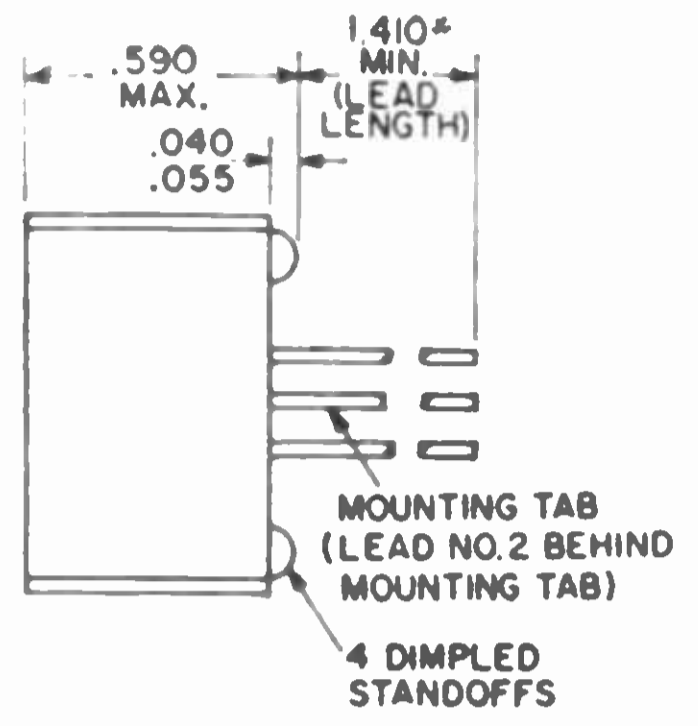
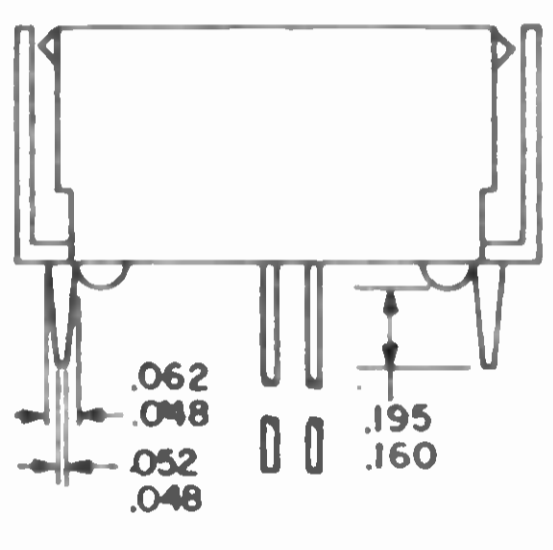
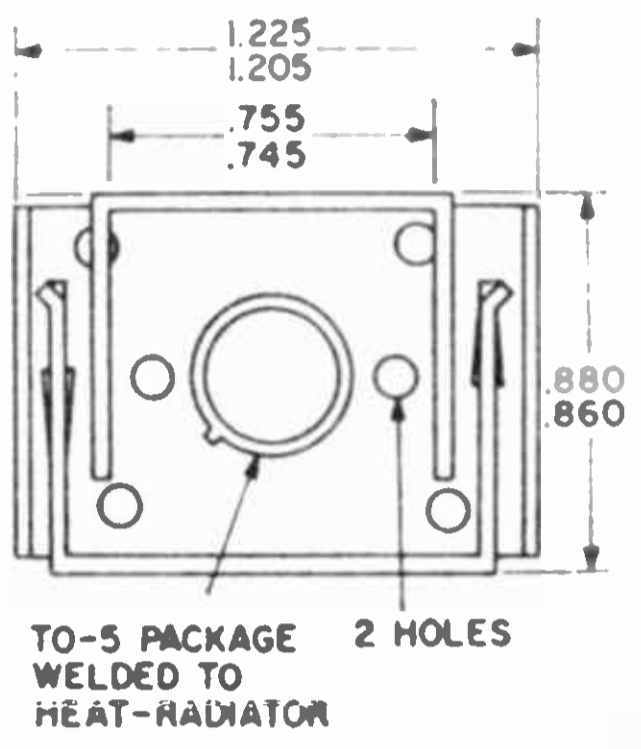
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Outlines (cont'd)

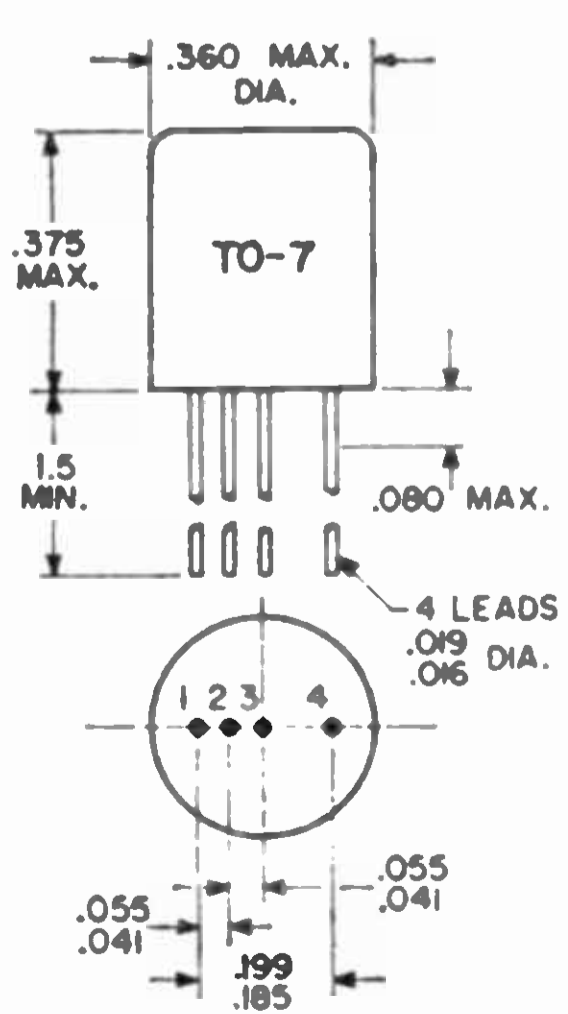


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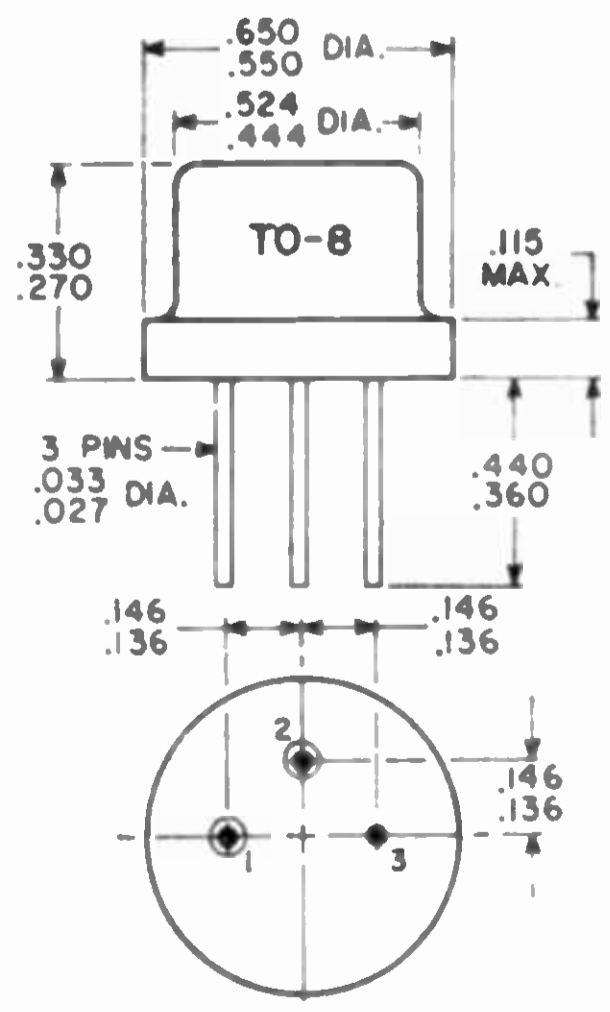


NOTE 1: RECOMMENDED HOLE SIZE FOR PRINTED-CIRCUIT BOARD IS 0.070 DIA.
* MODIFIED TO-5 TYPE IS A 2 LEAD PACKAGE HAVING LEAD LENGTHS OF 0.9 mm. LENGTH.

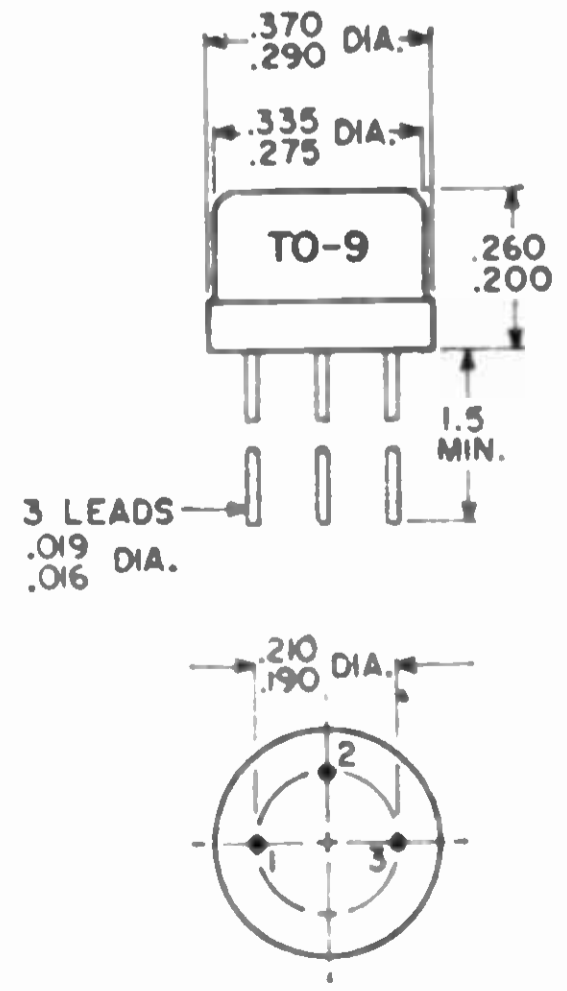
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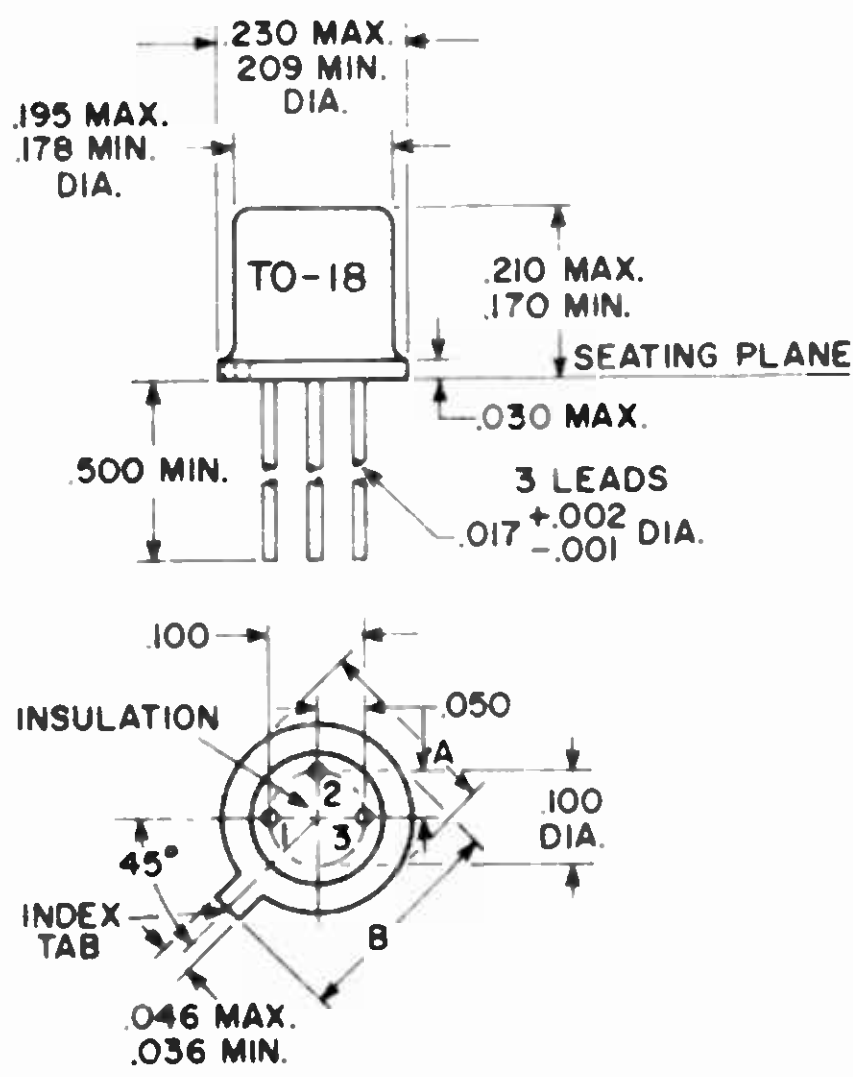


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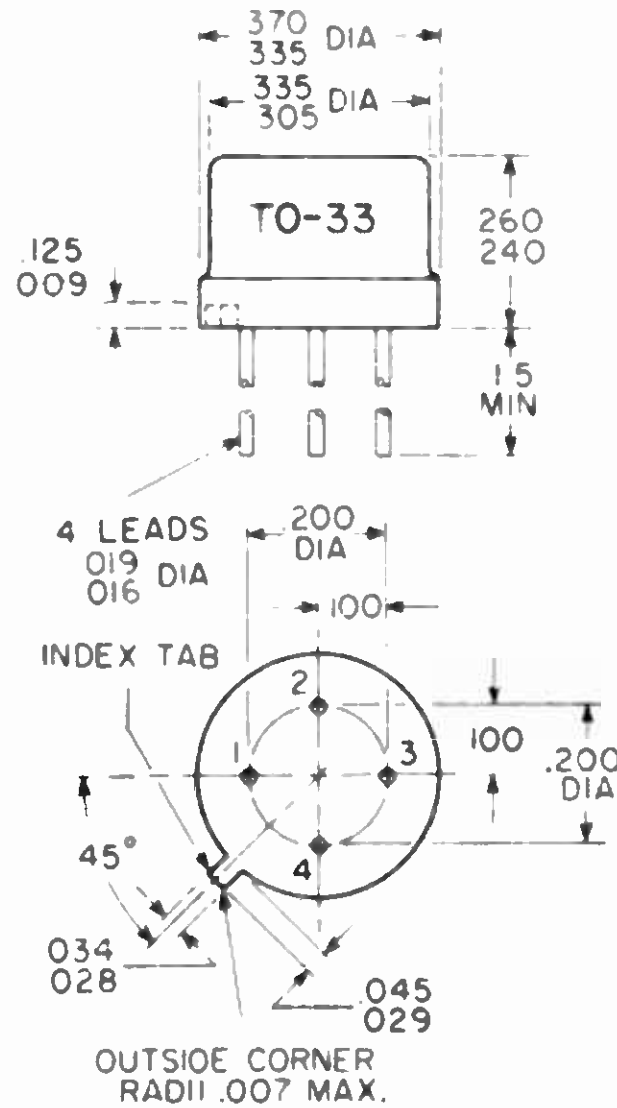


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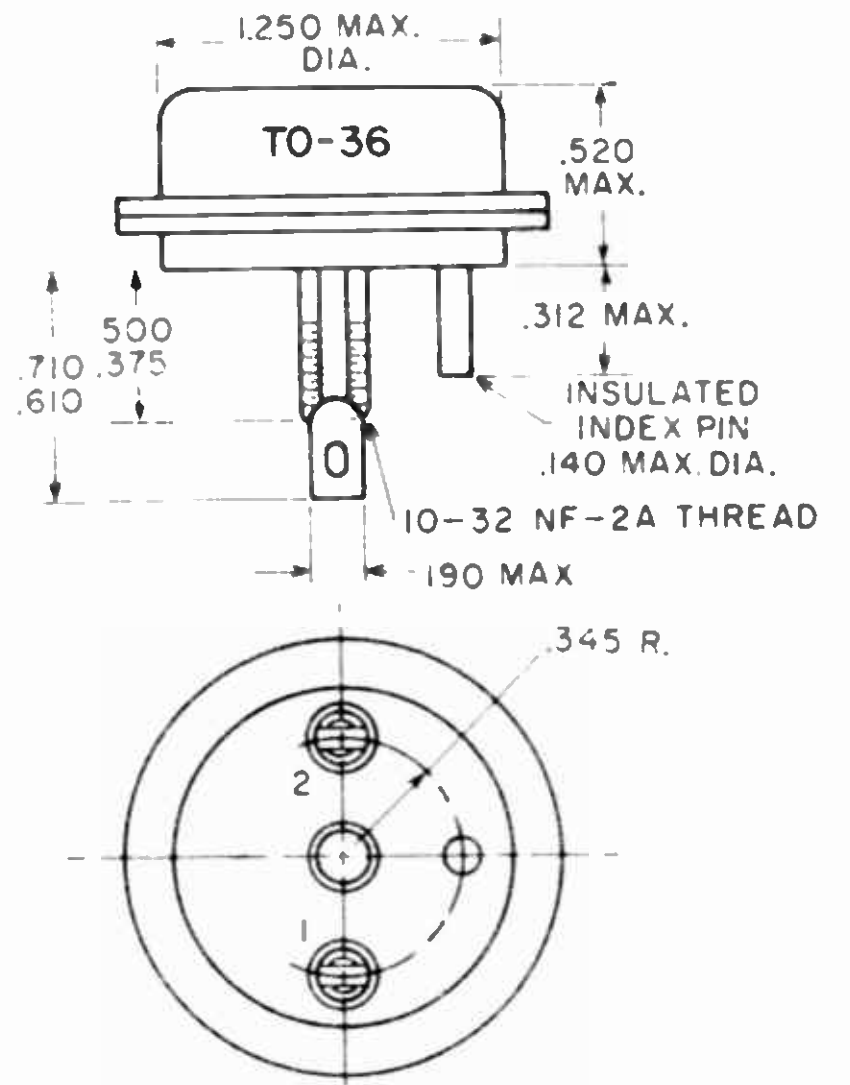
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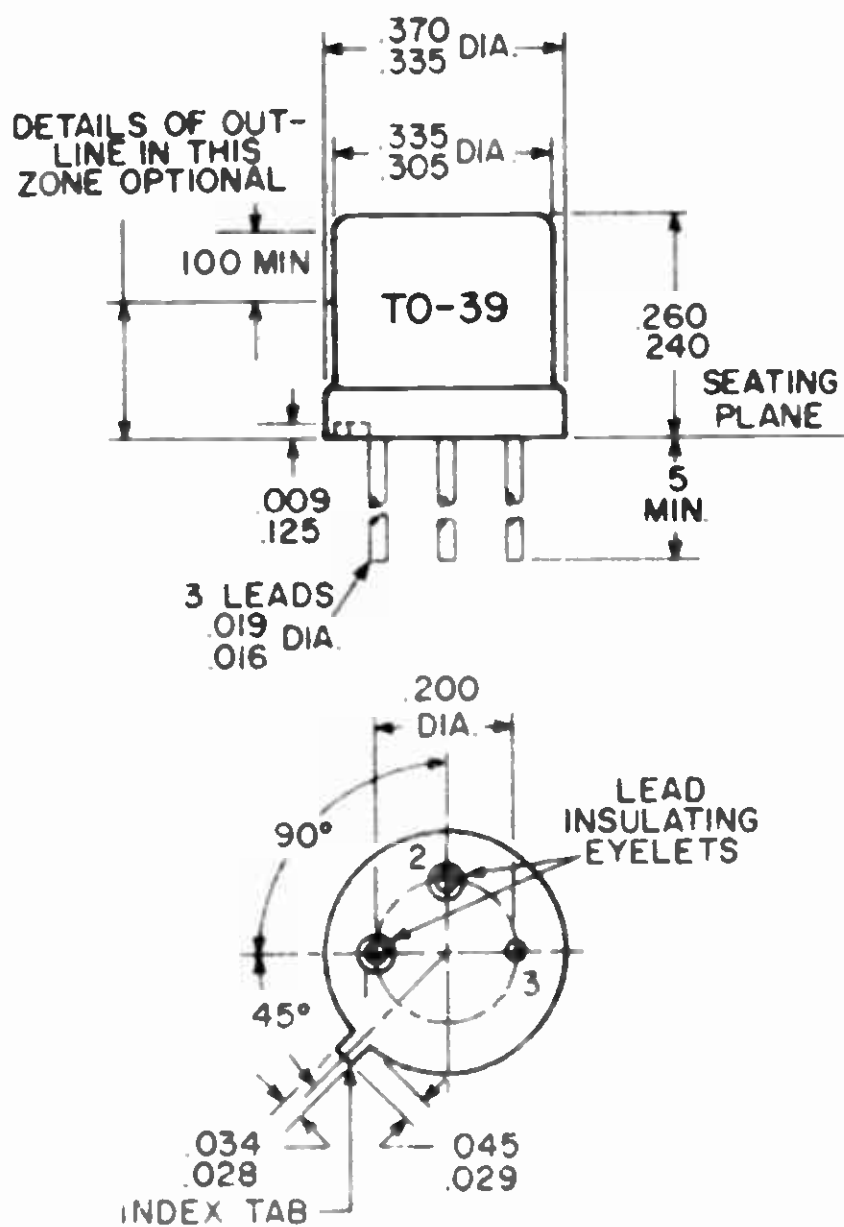
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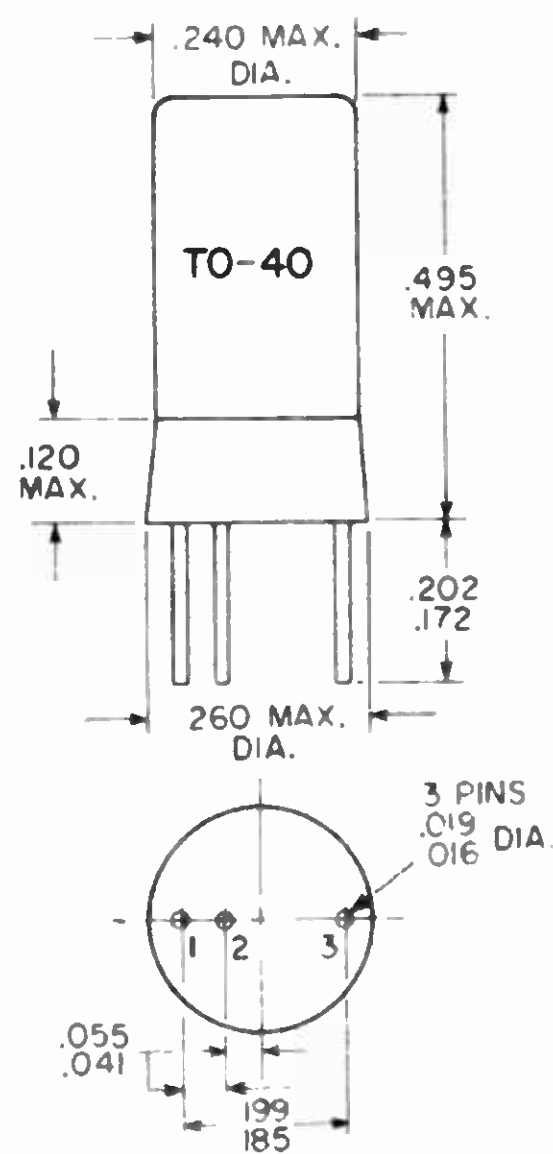
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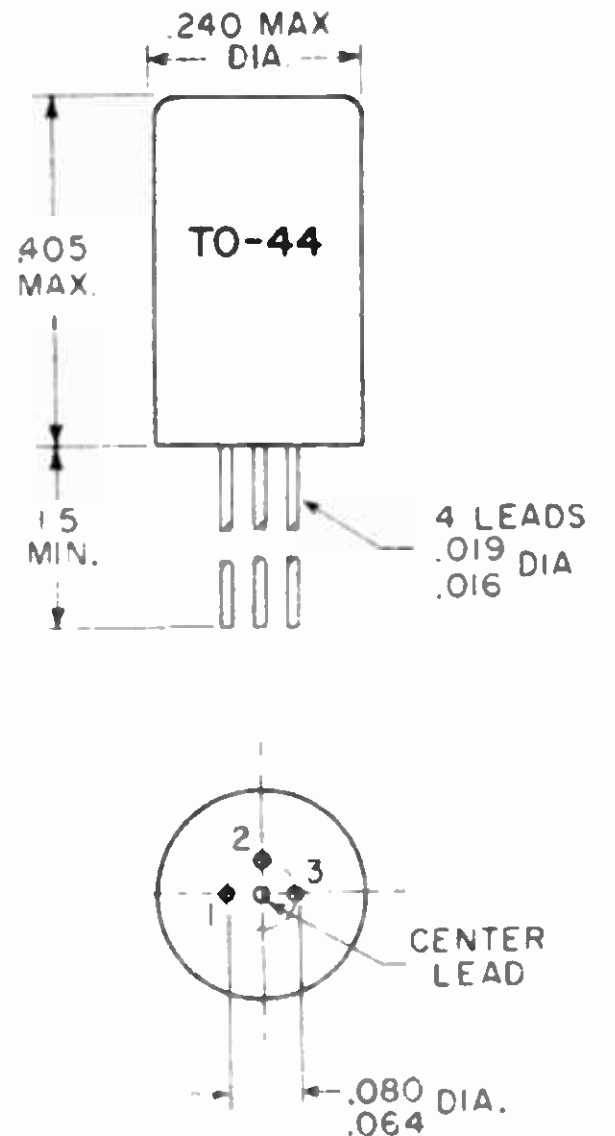
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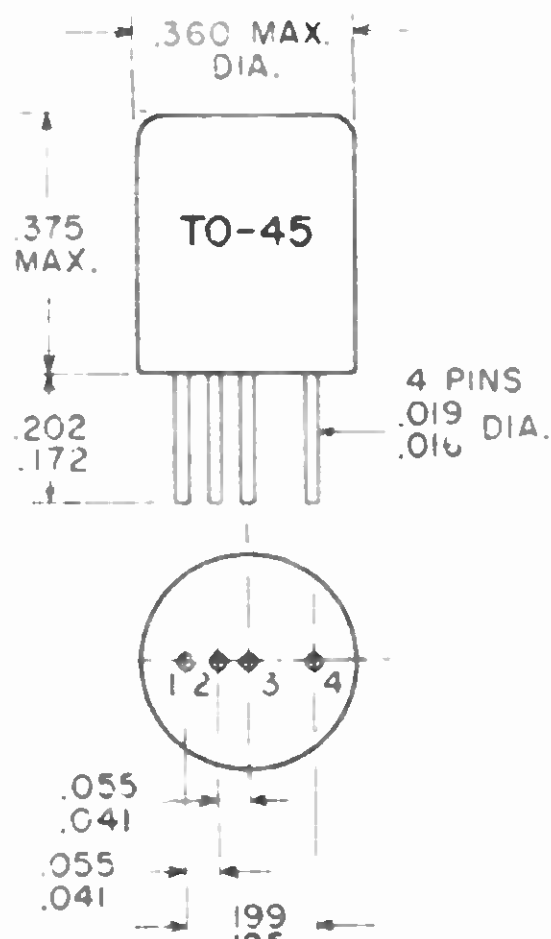
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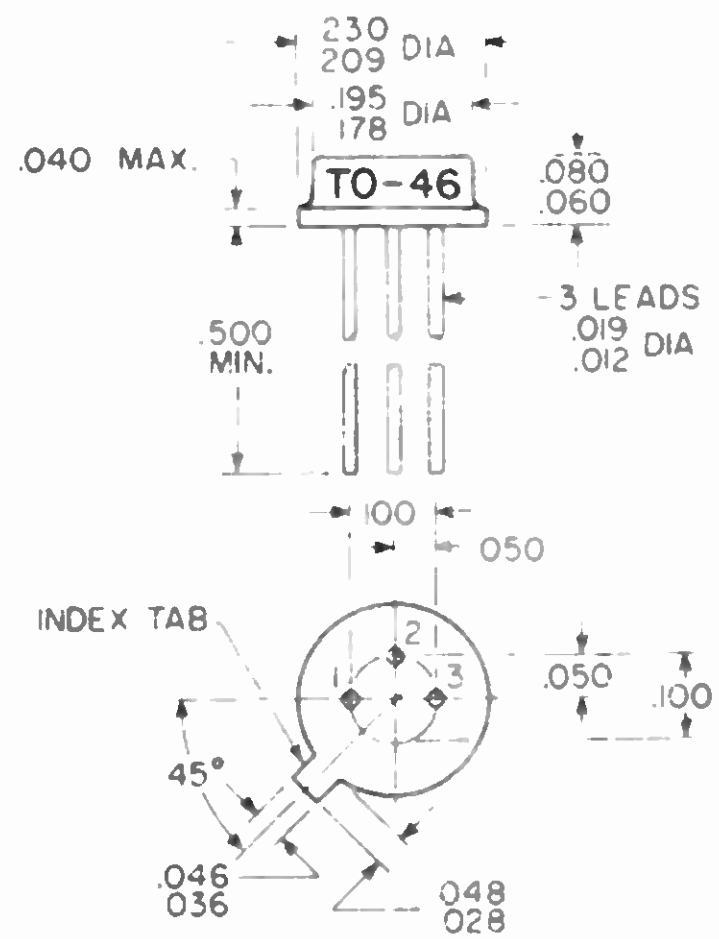
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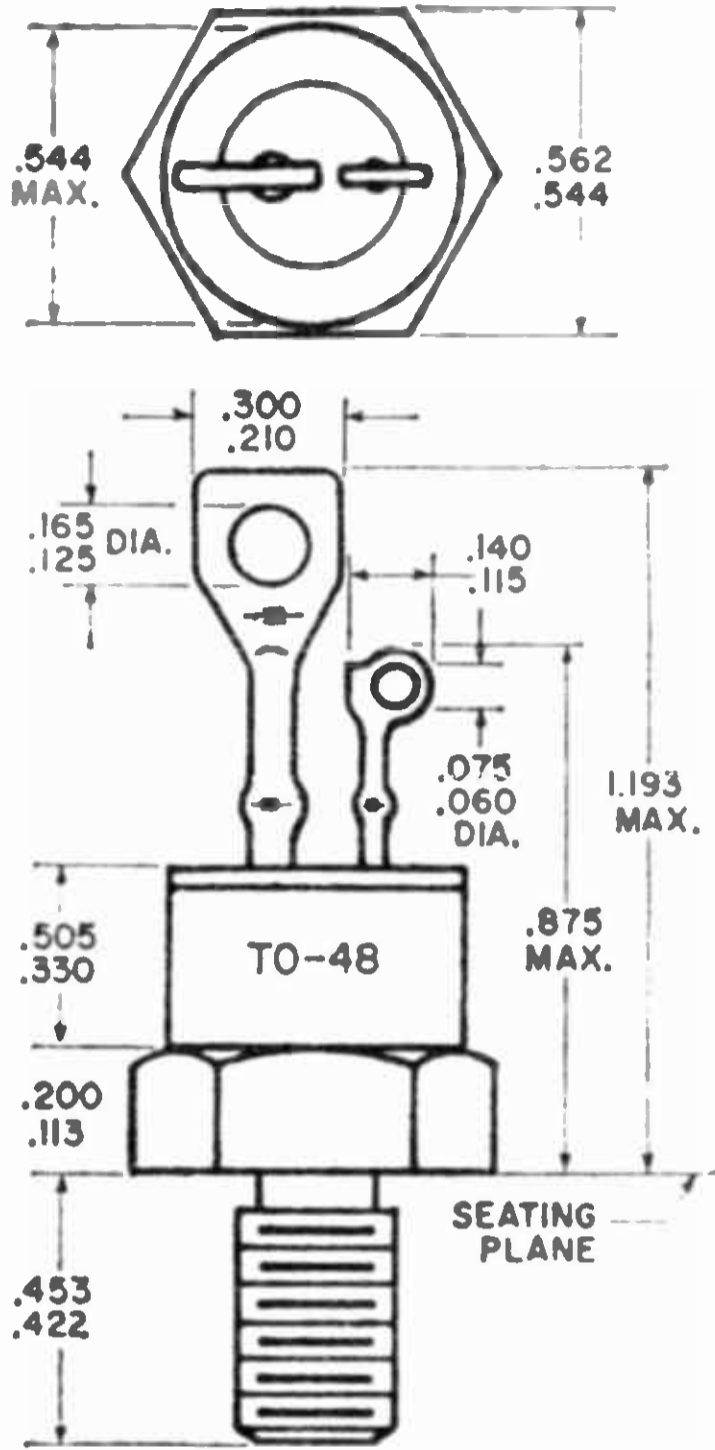


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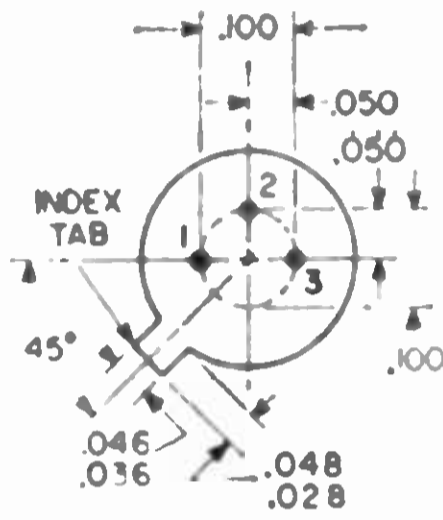
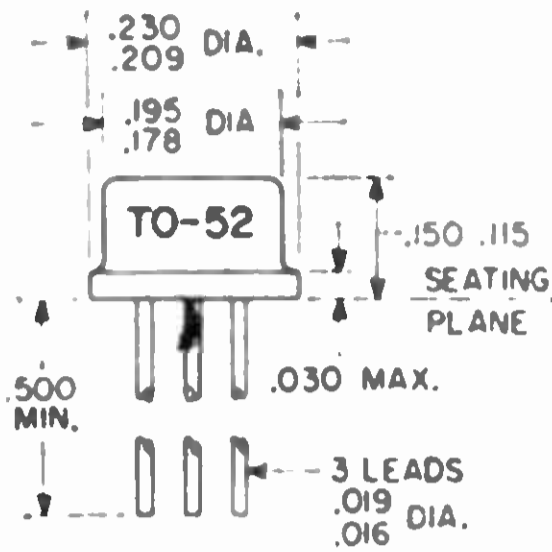


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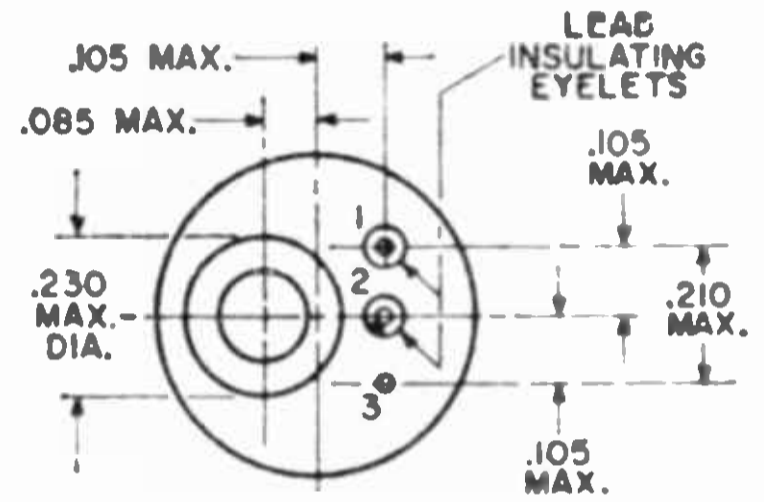
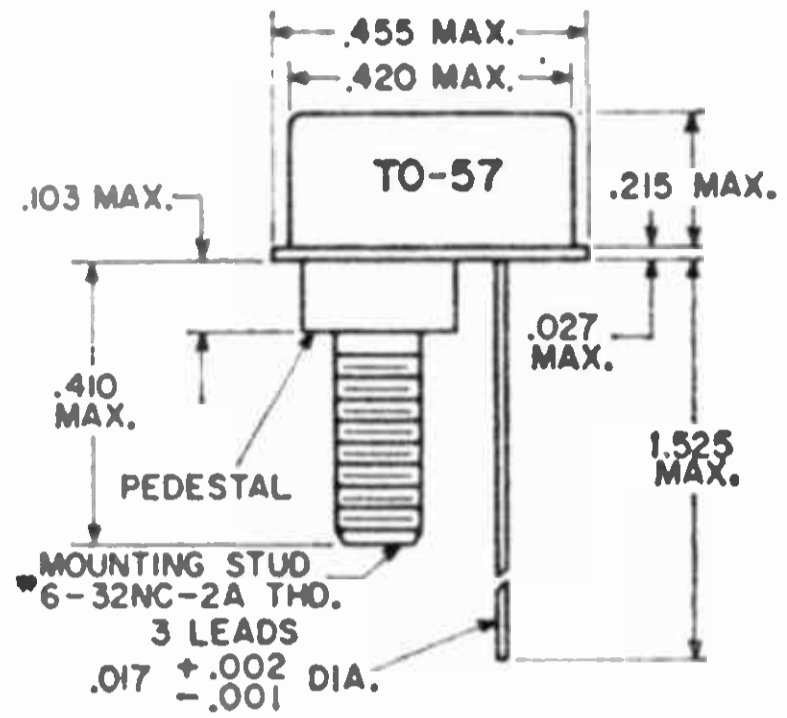
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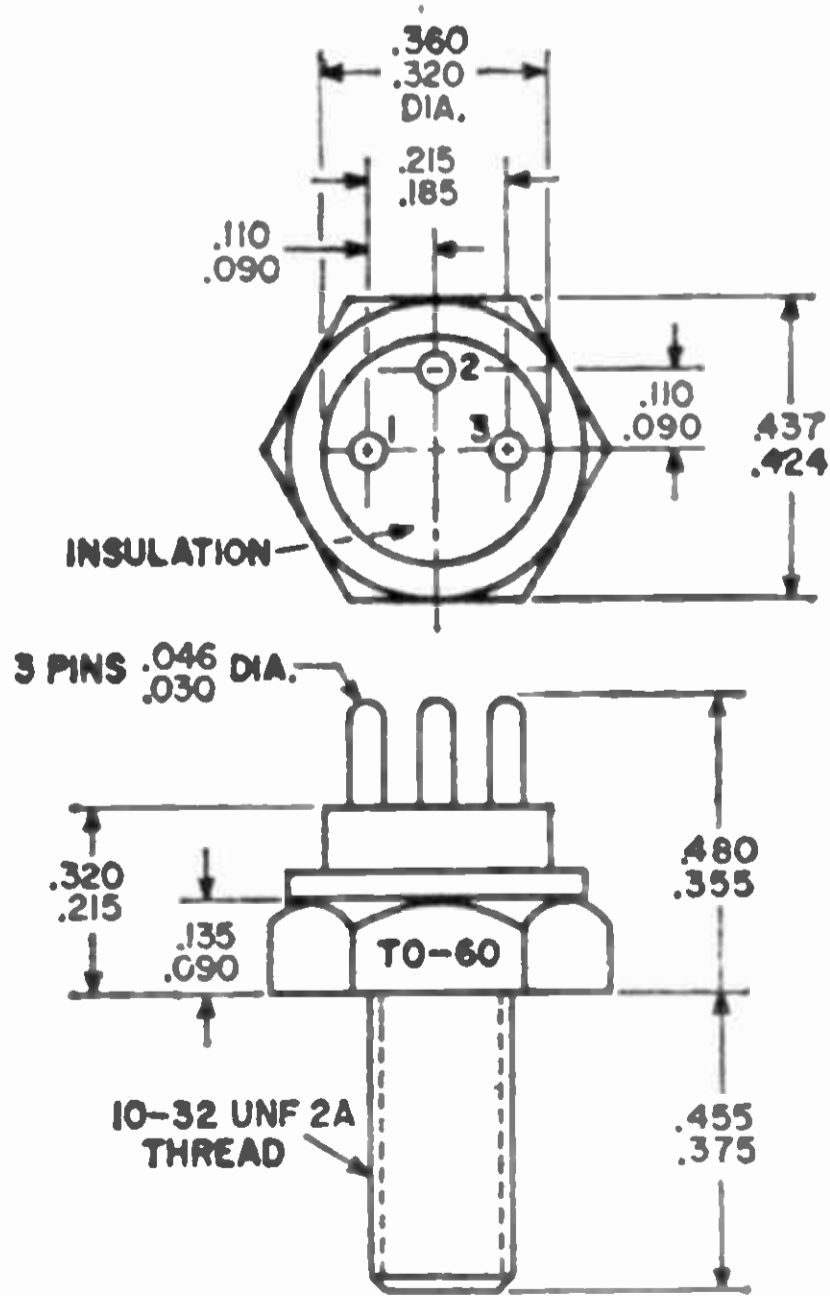
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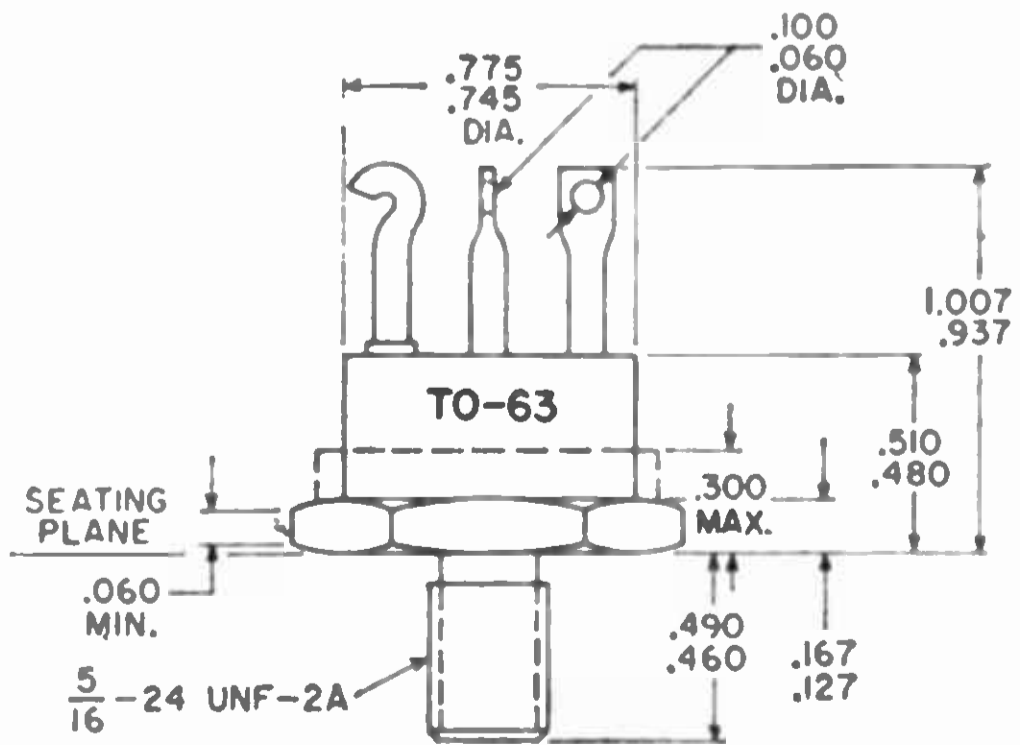
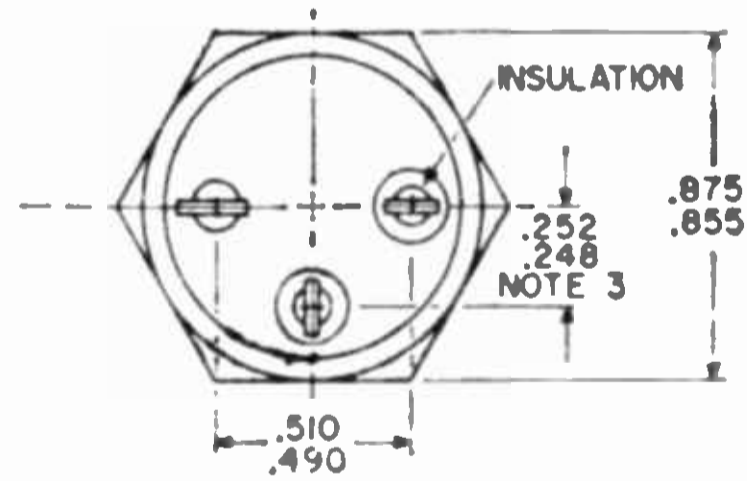
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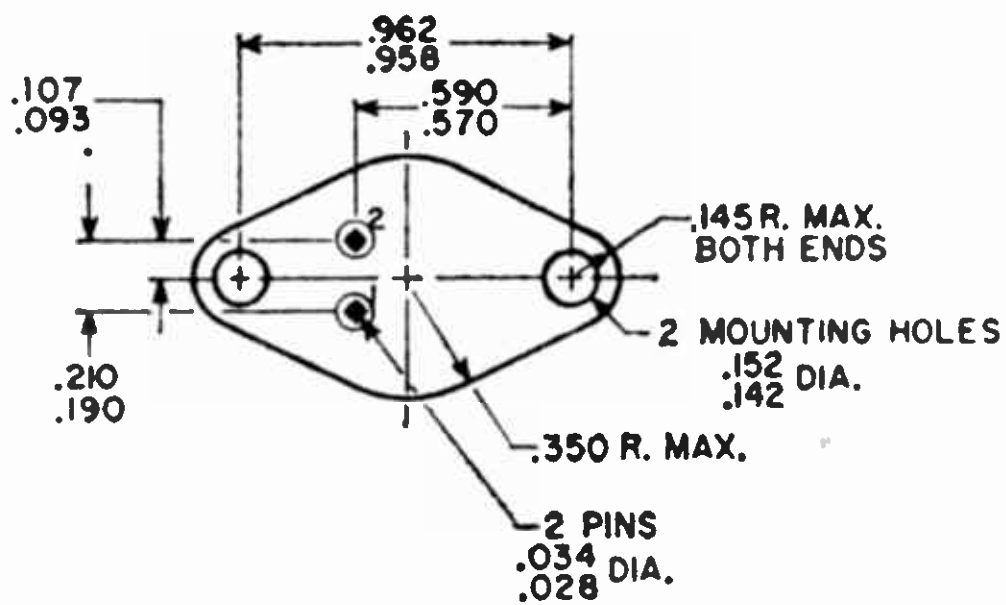
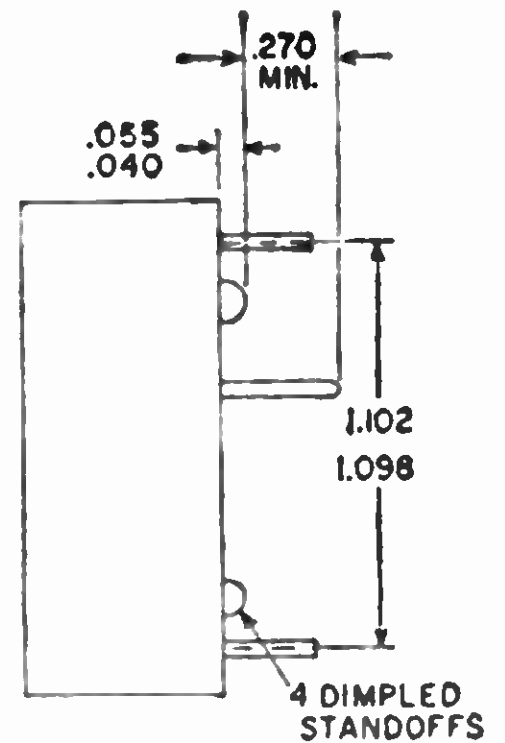
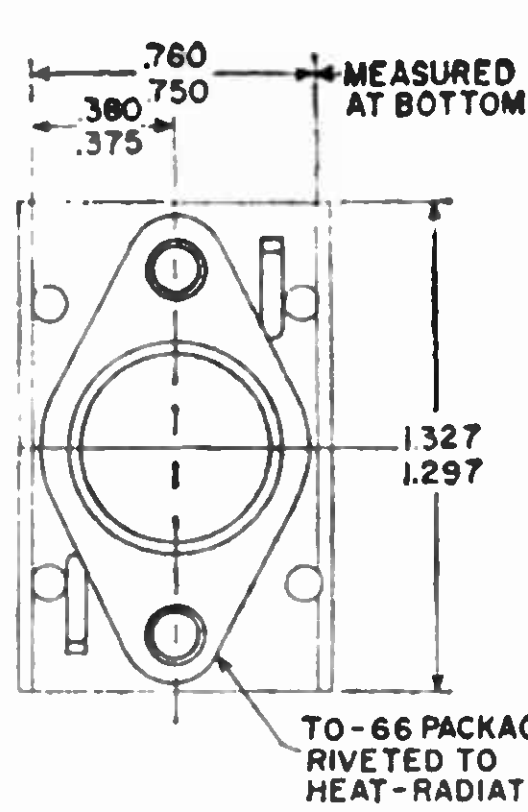
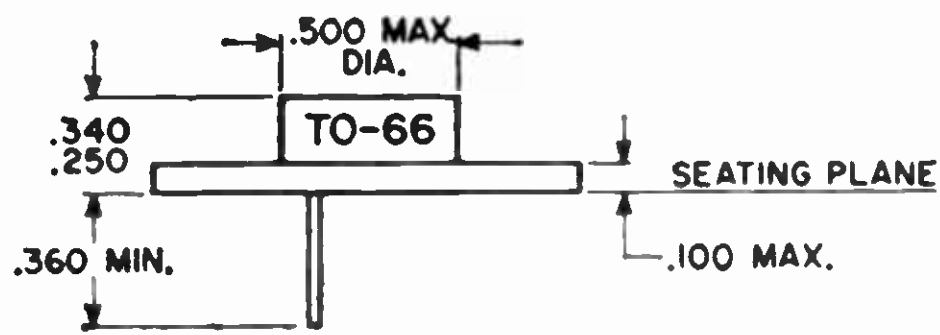


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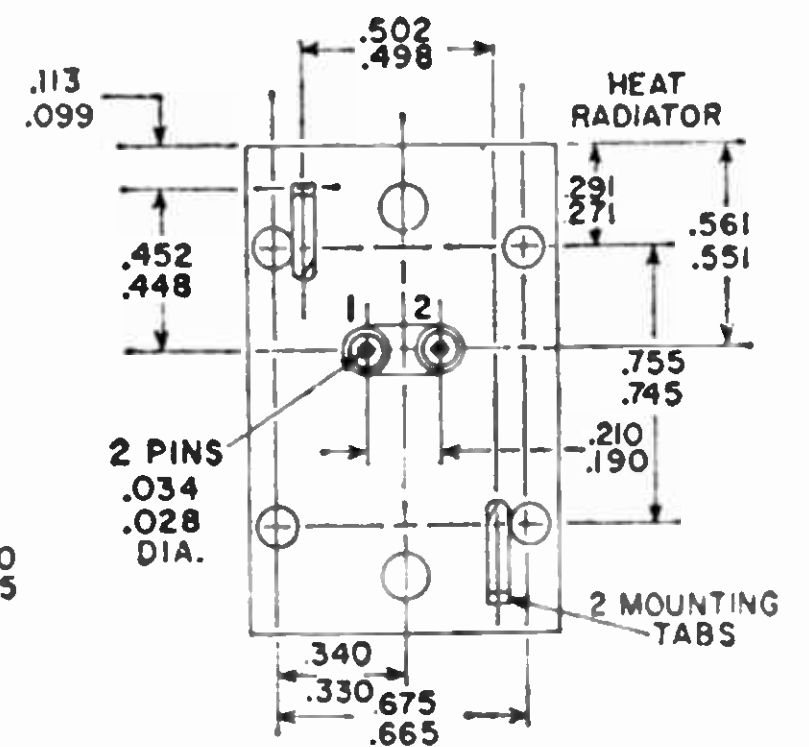
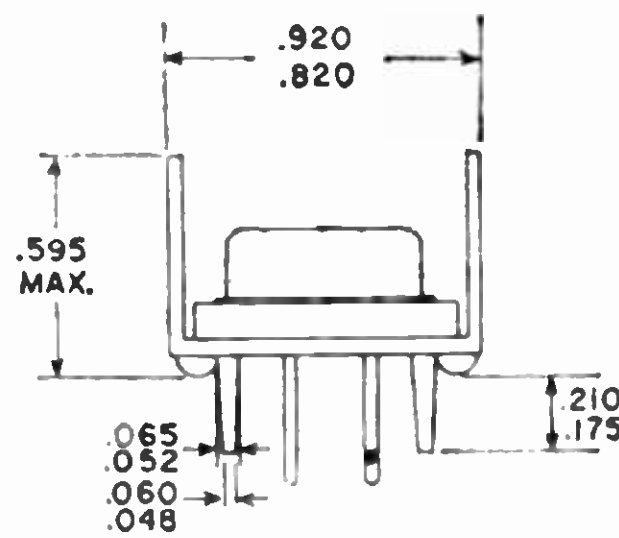


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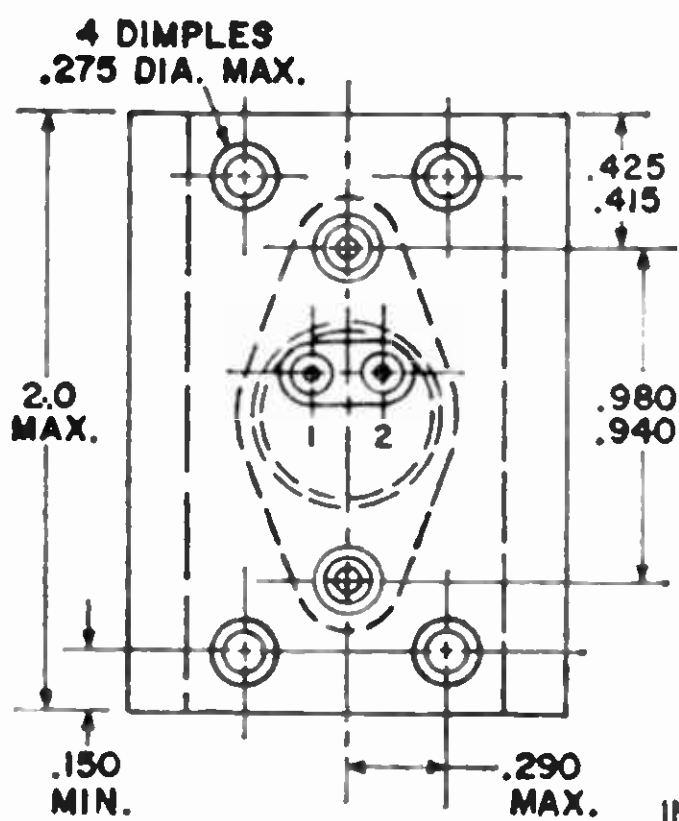
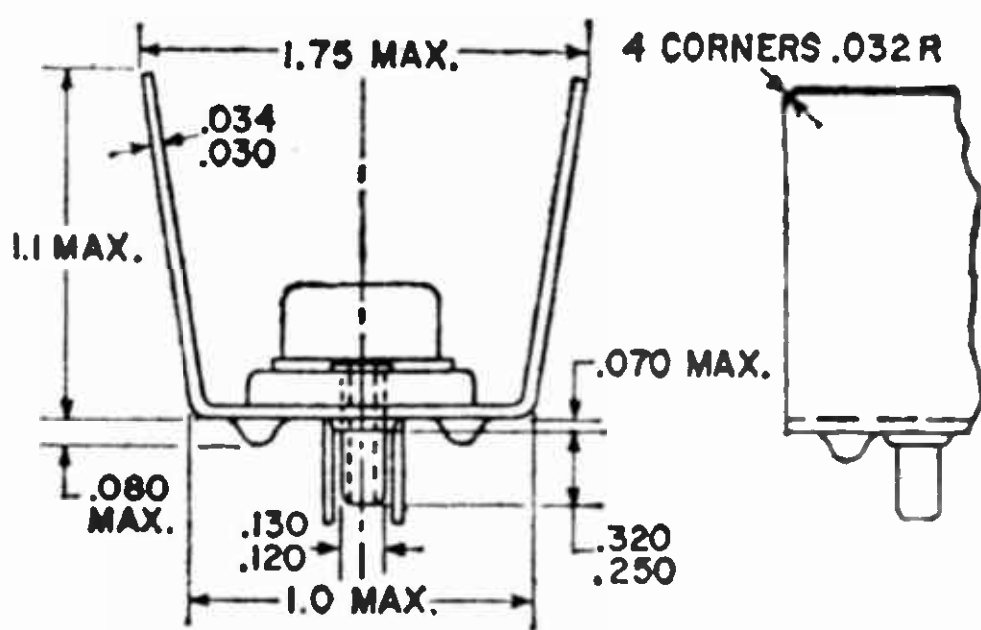
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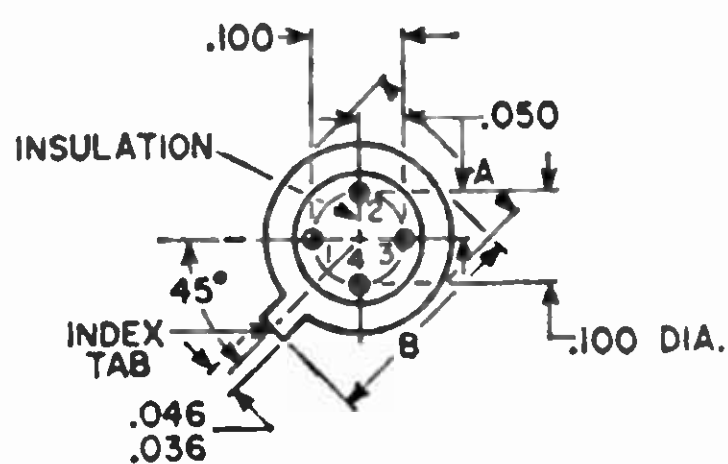
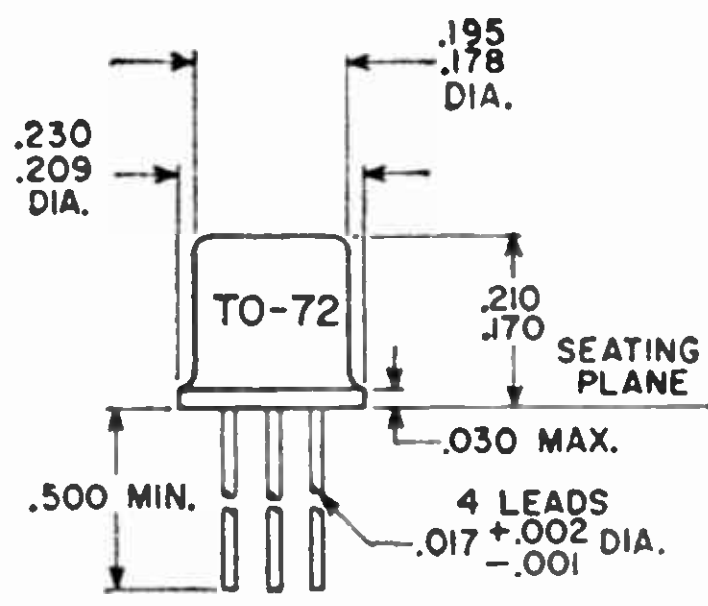
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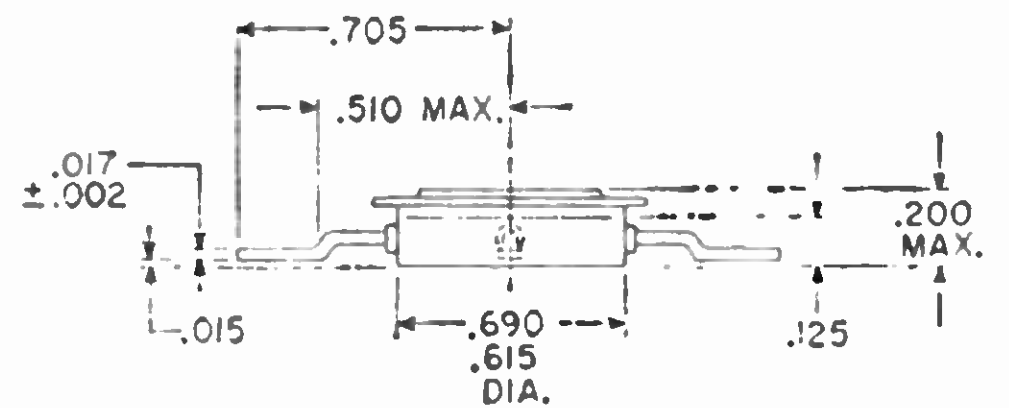
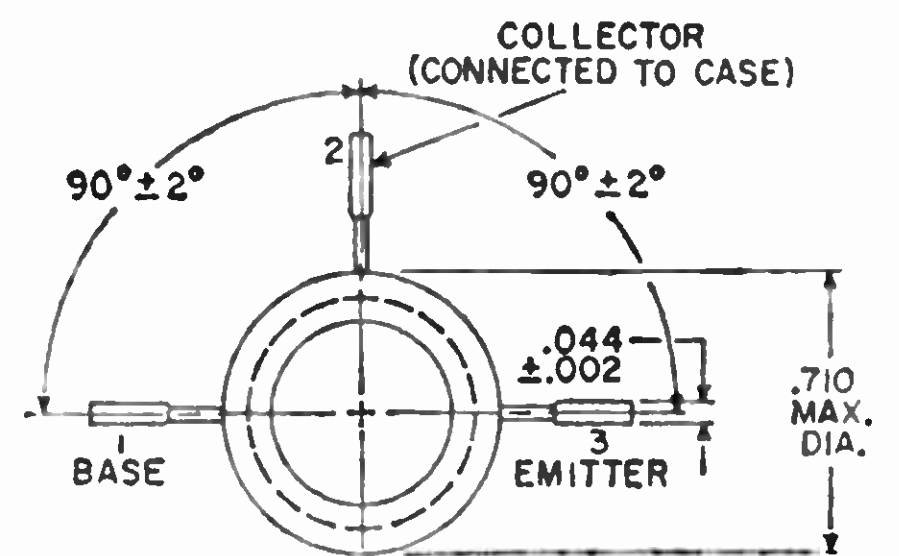
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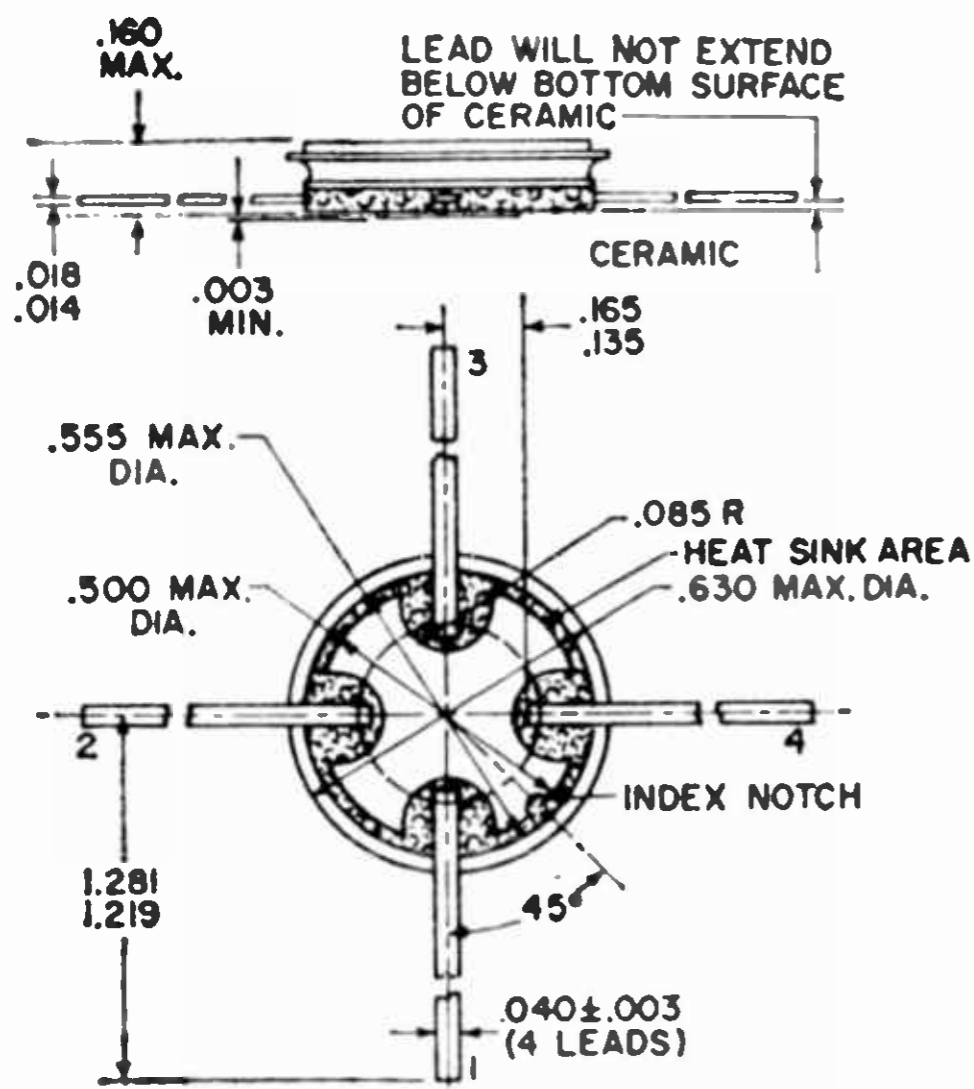


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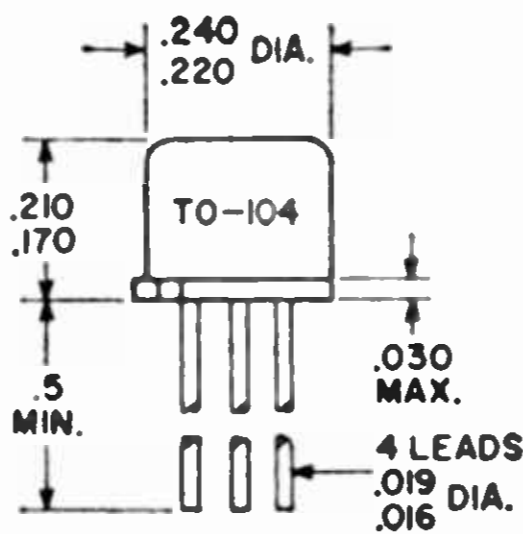


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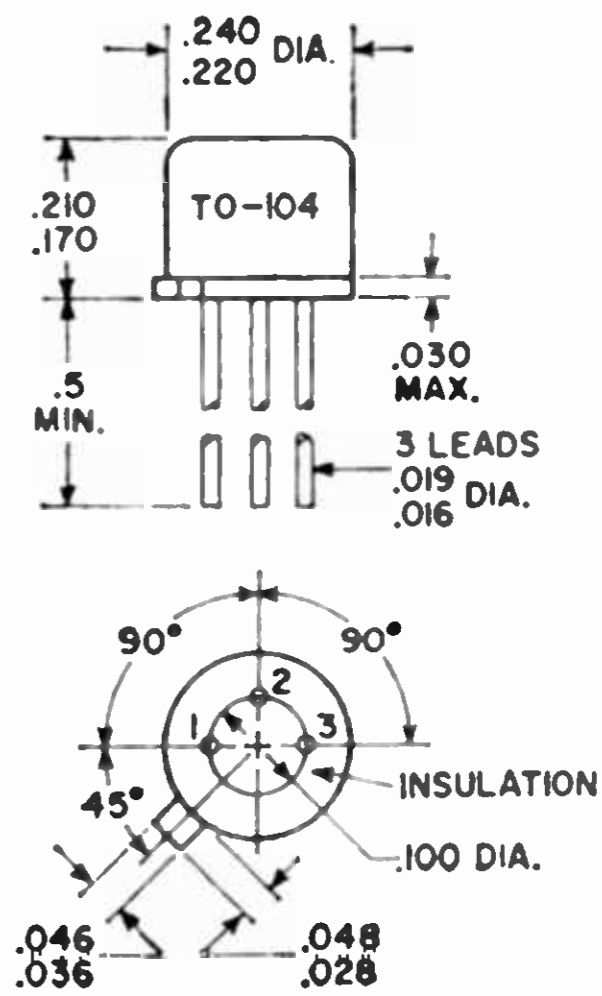
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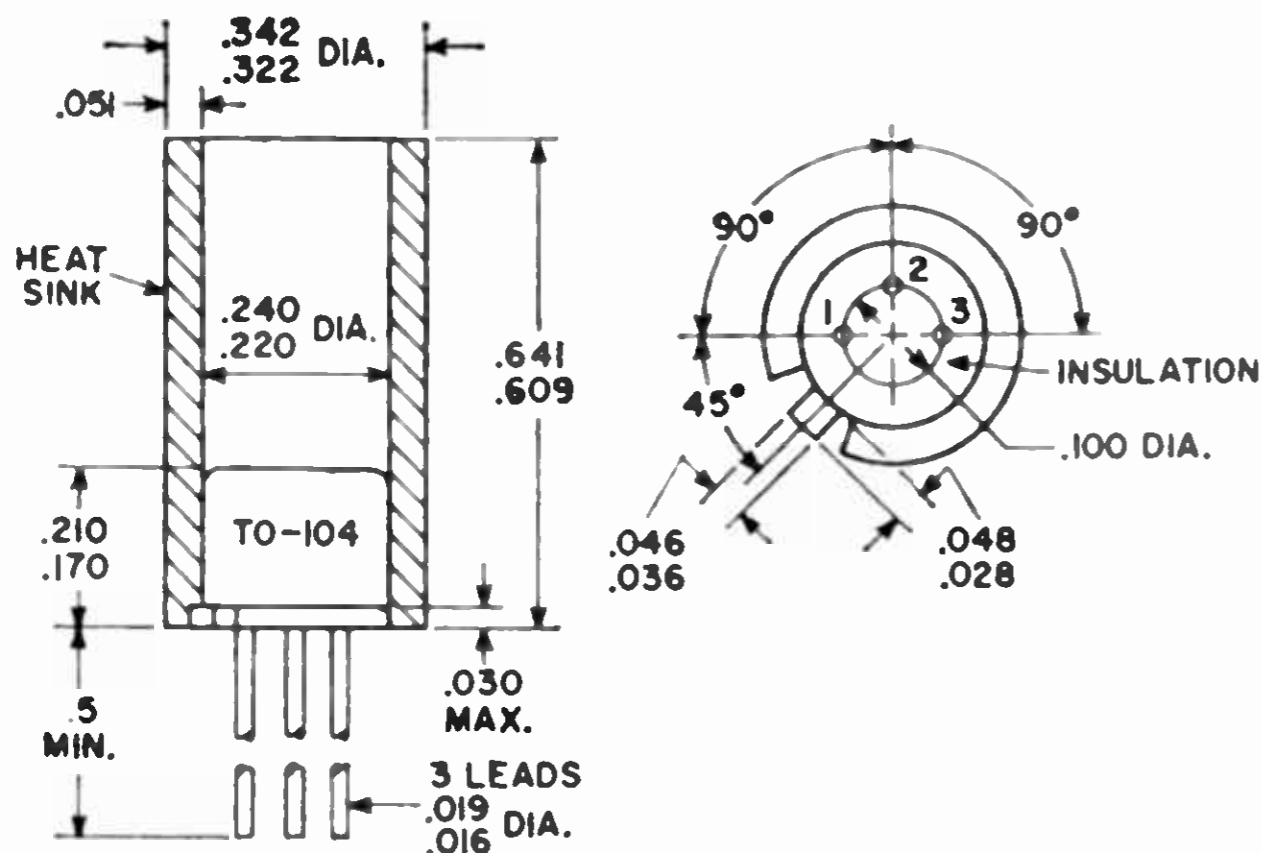
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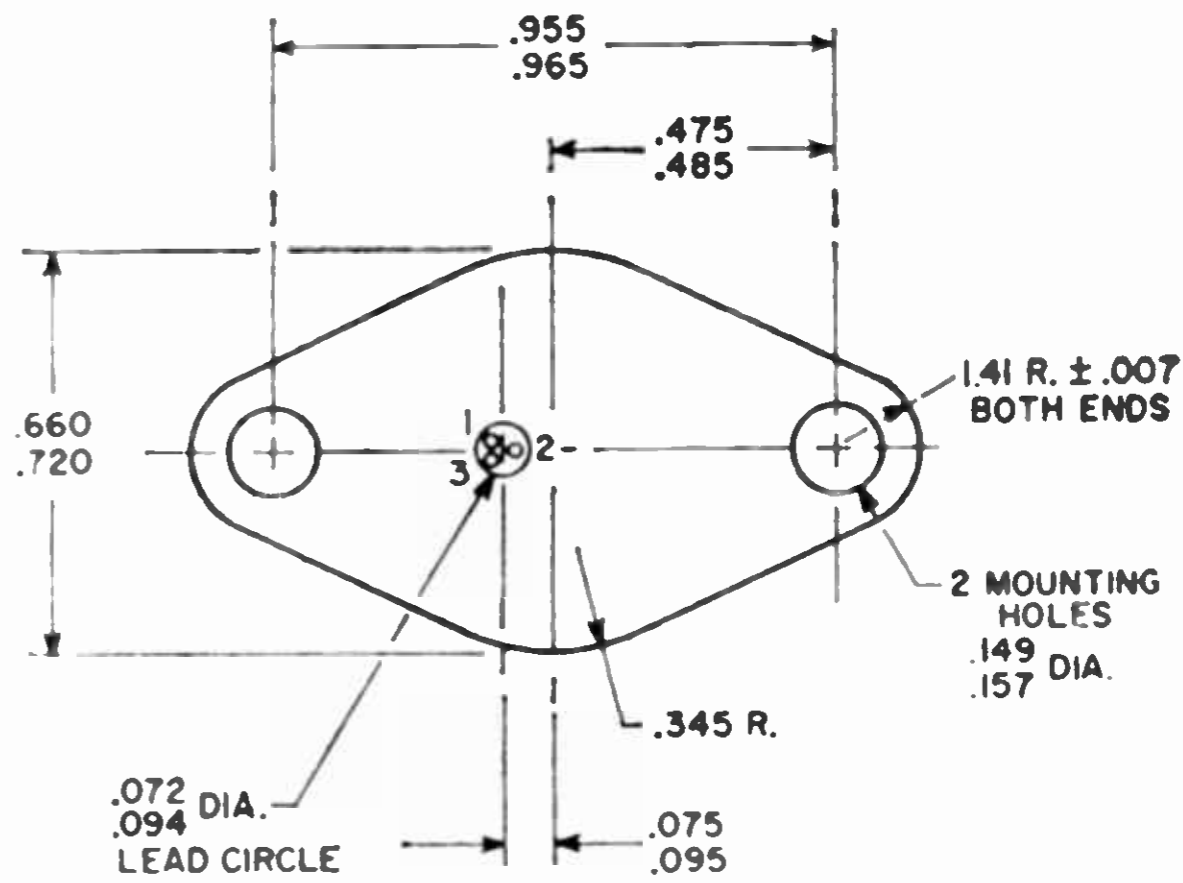
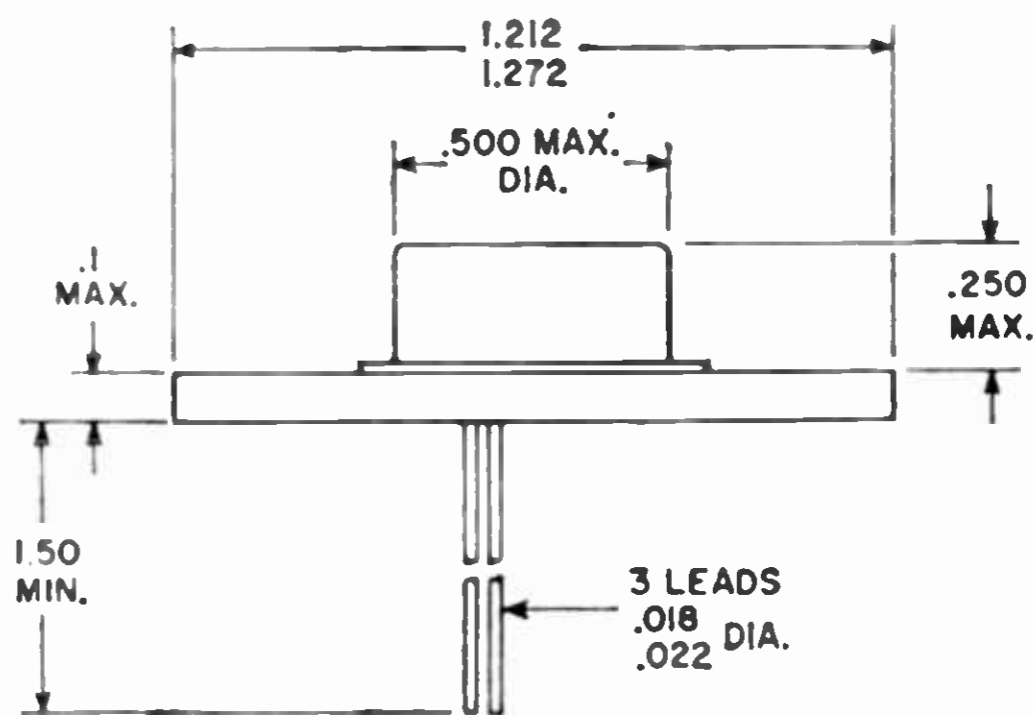
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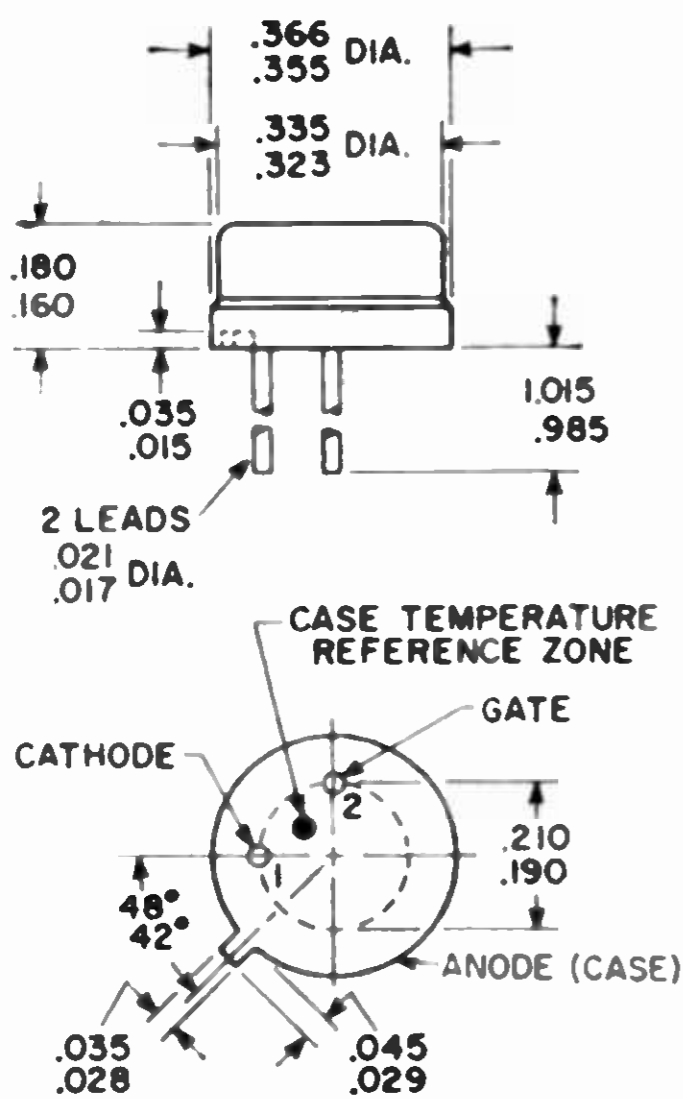
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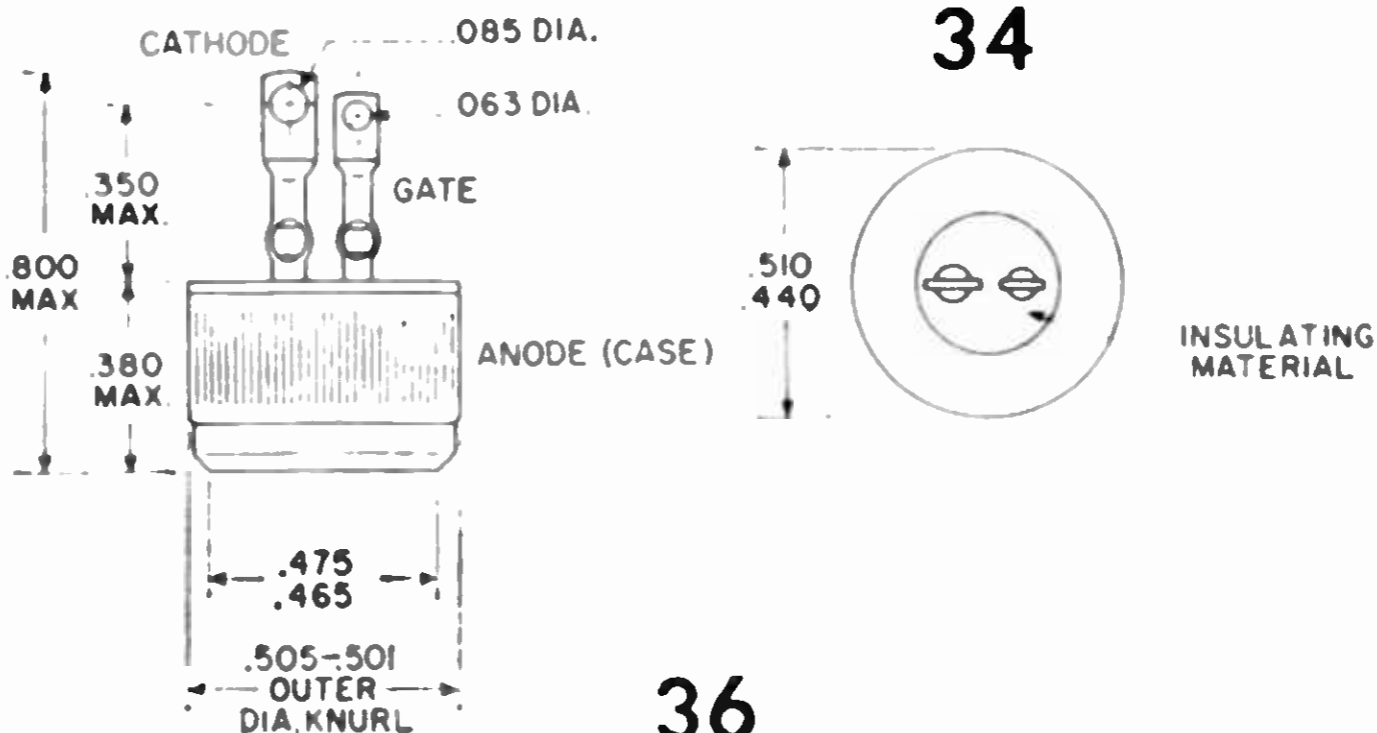
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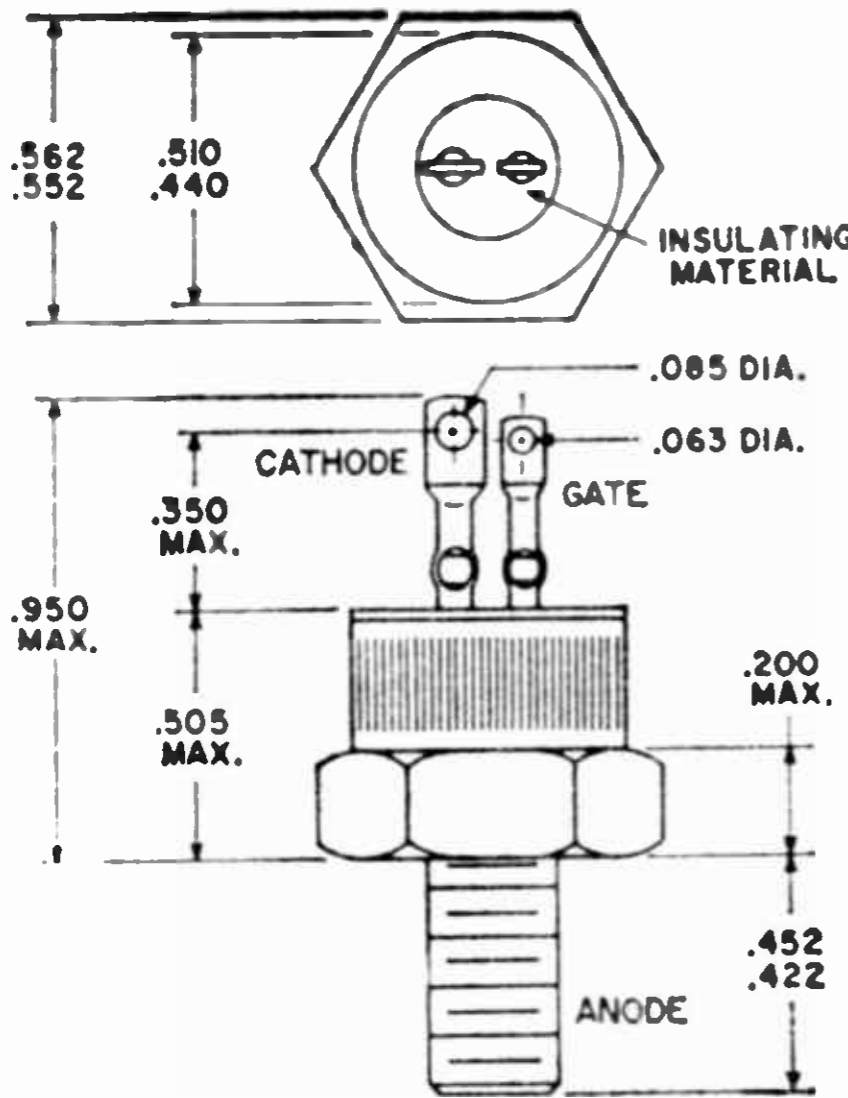


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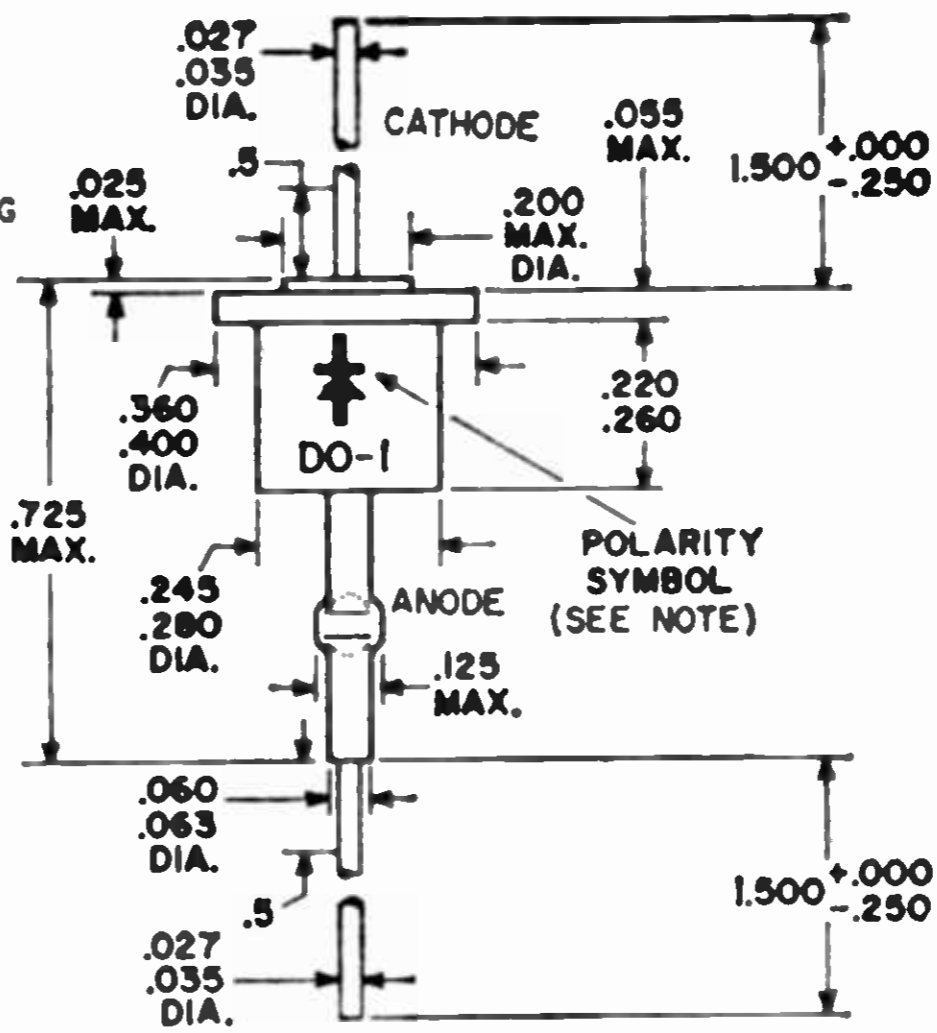


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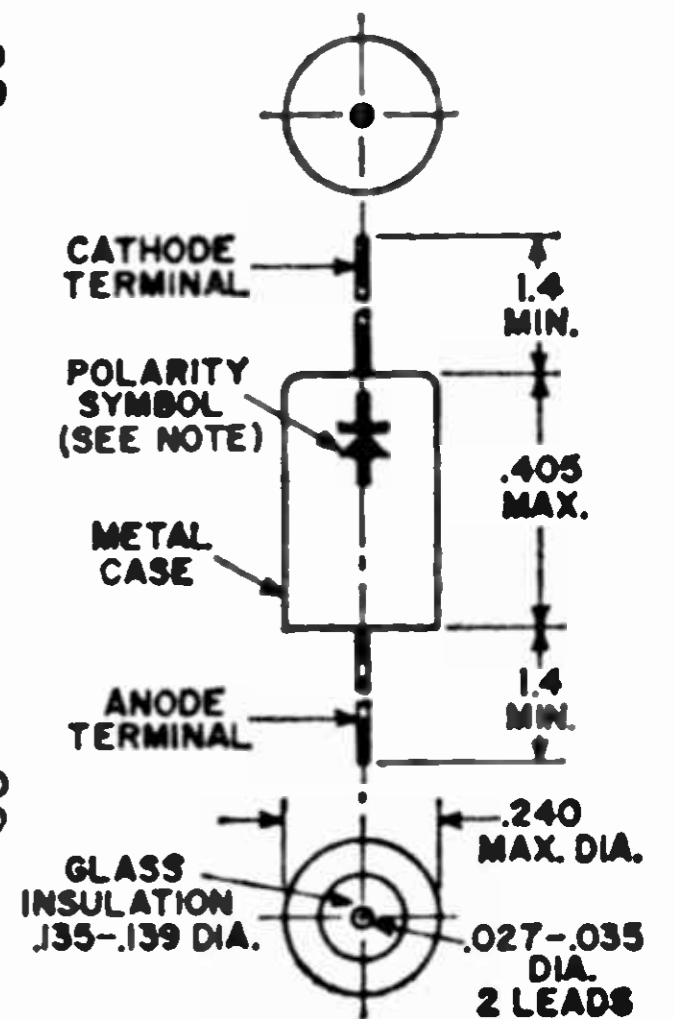
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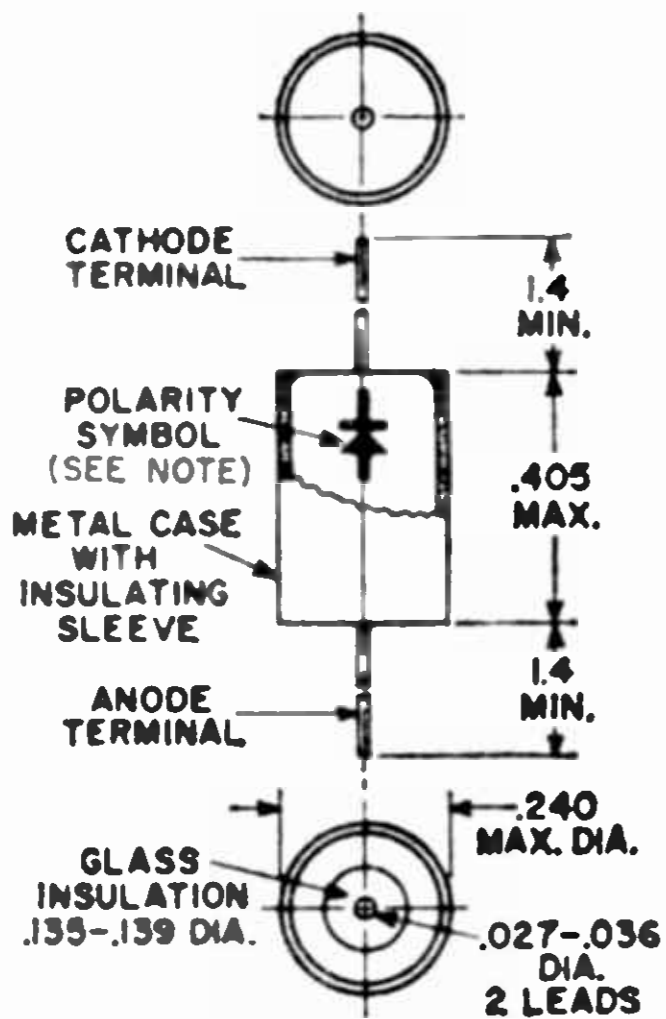
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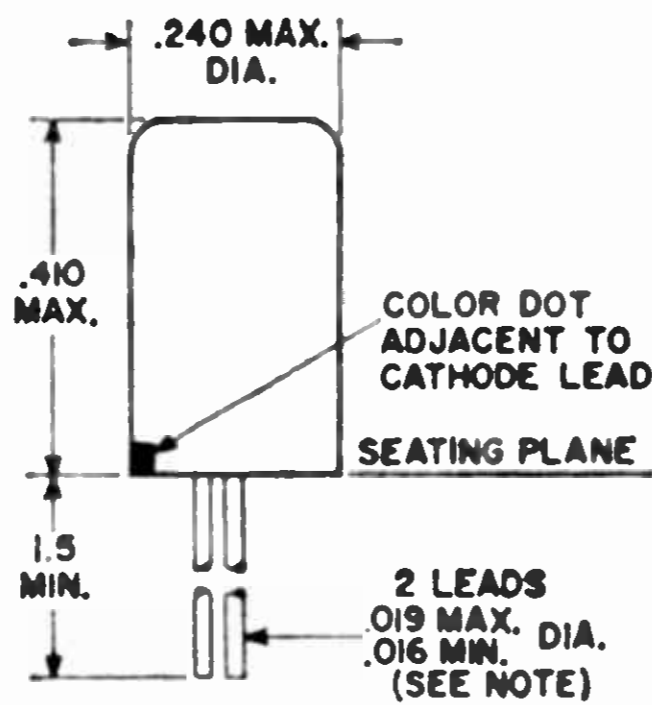
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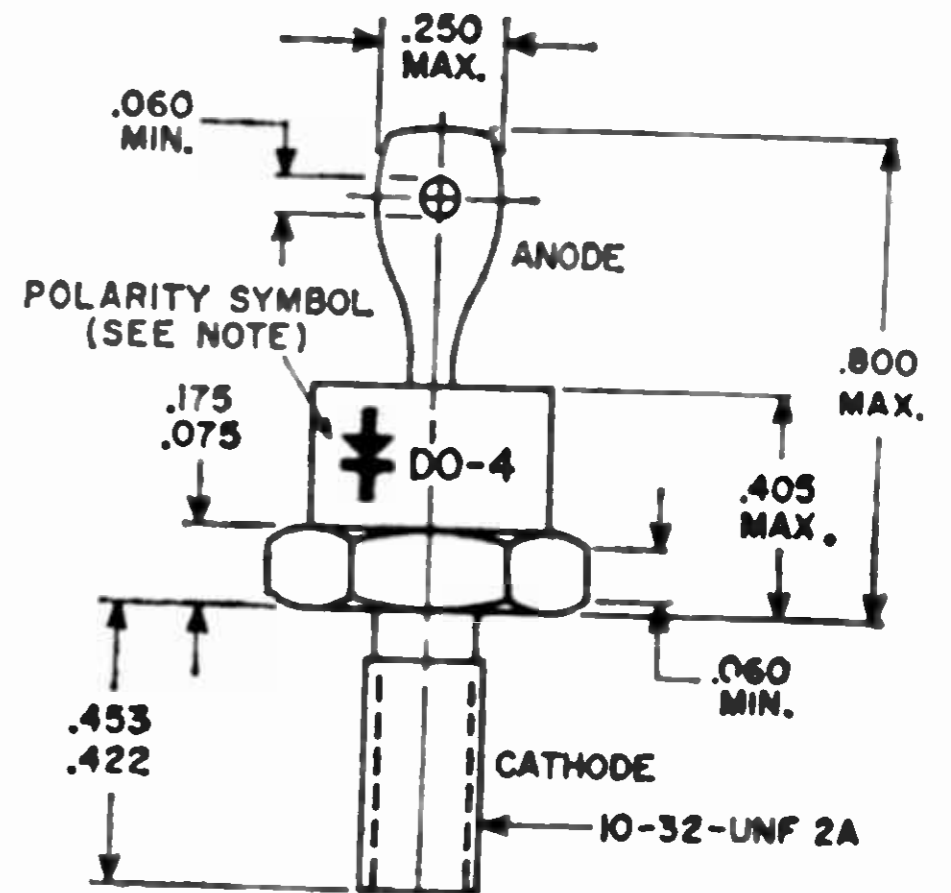
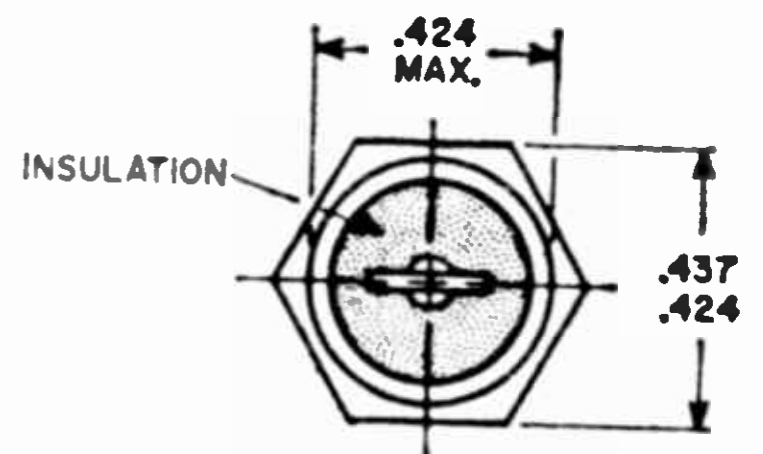
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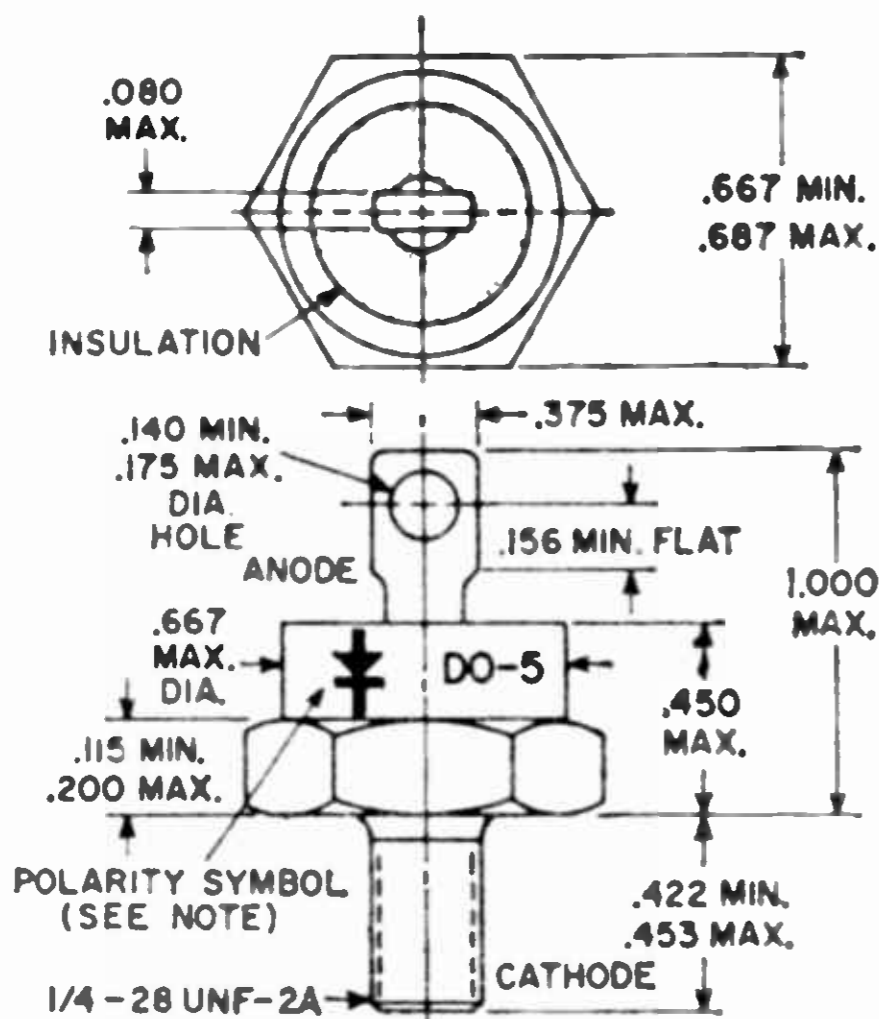
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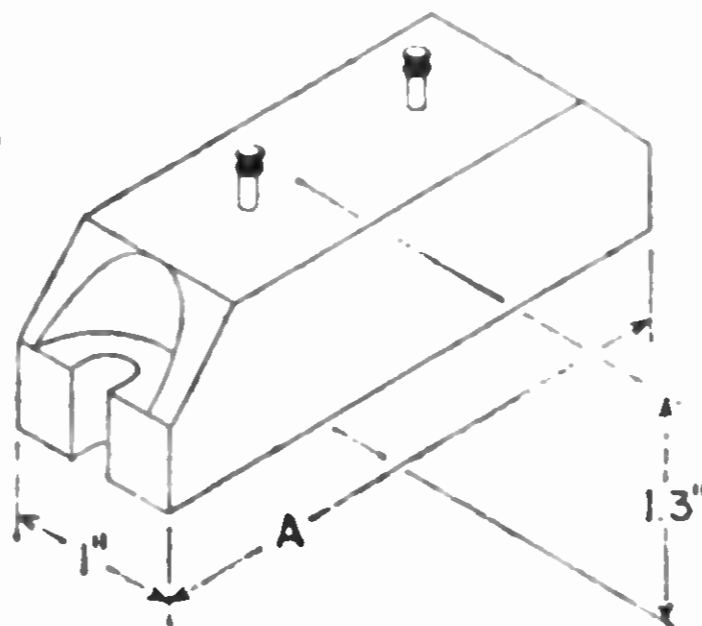
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43

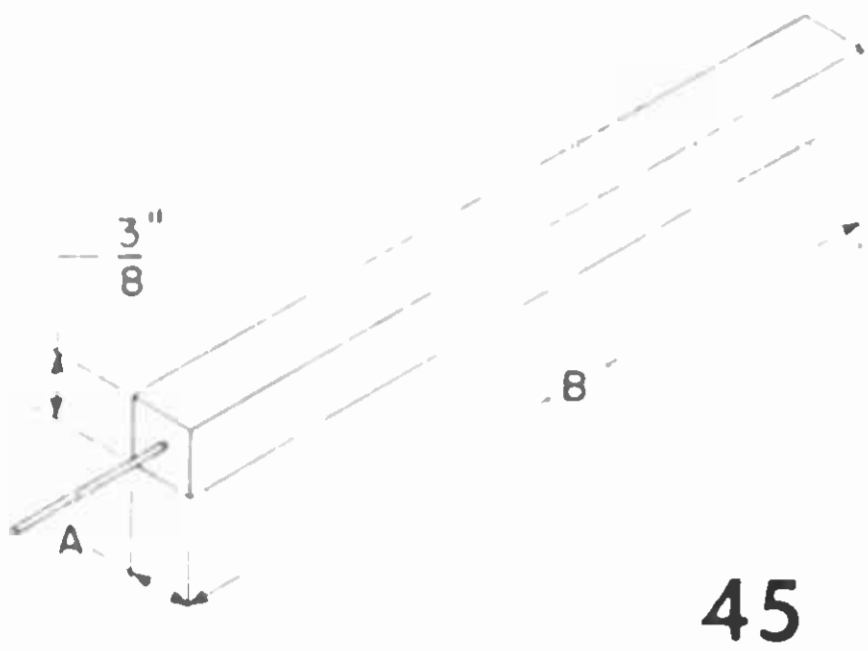


44

Outline No.	"A" (Inches)
44a	2 3/8
44b	2 3/8
44c	2 3/8
44d	3 1/4
44e	3 1/4
44f	4 1/2
44g	4 1/2
44h	4 1/2
44i	5 1/2
44j	5 1/2

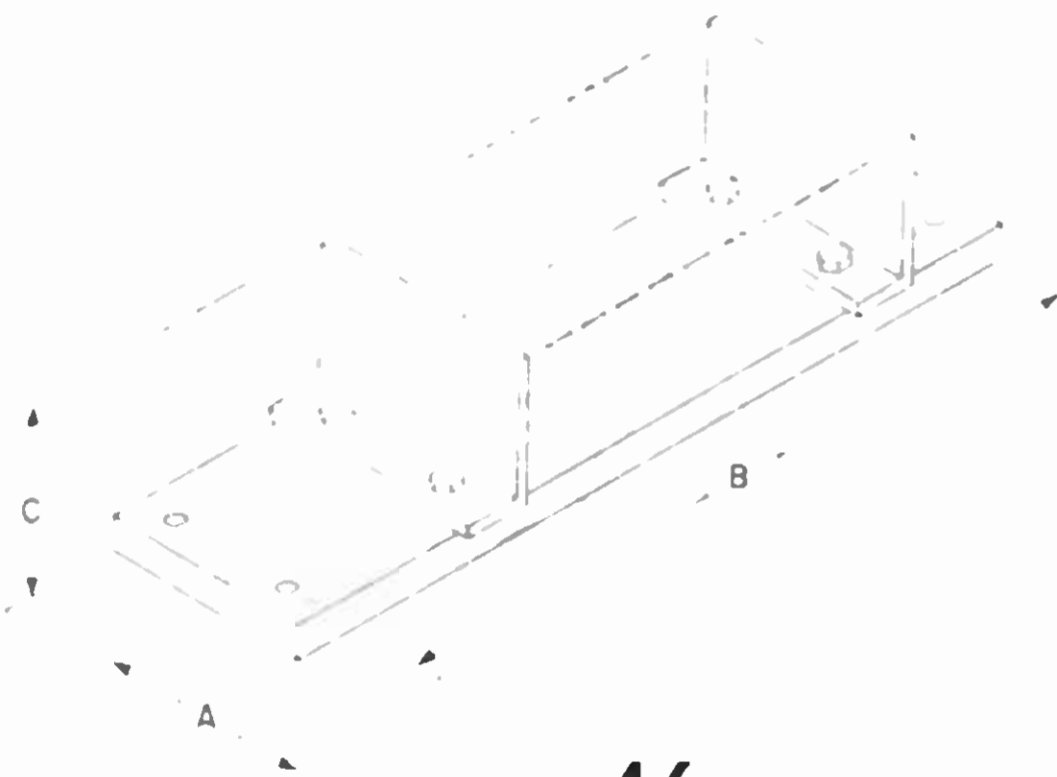
NOTE: ARROW INDICATES DIRECTION OF FORWARD CURRENT AS INDICATED BY DC AMMETER

Outlines (cont'd)



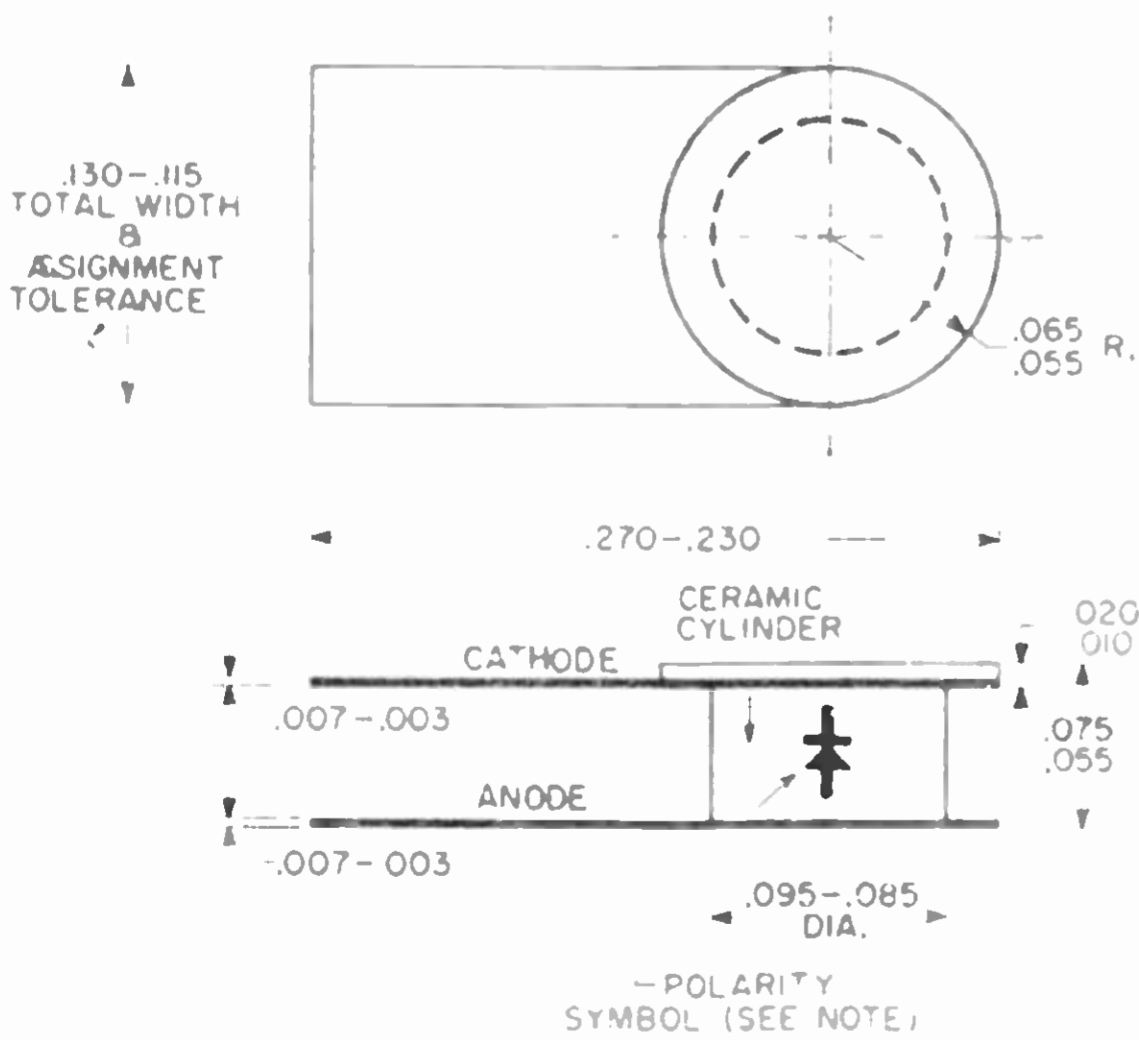
45

Outline No.	"A" (Inches)	"B"
45a	3/8	2
45b	3/8	3 1/2
45c	3/8	4 1/2
45d	3/4	3 1/2
45e	3/4	3 1/2
45f	3/4	4 1/2
45g	3/4	4 1/2

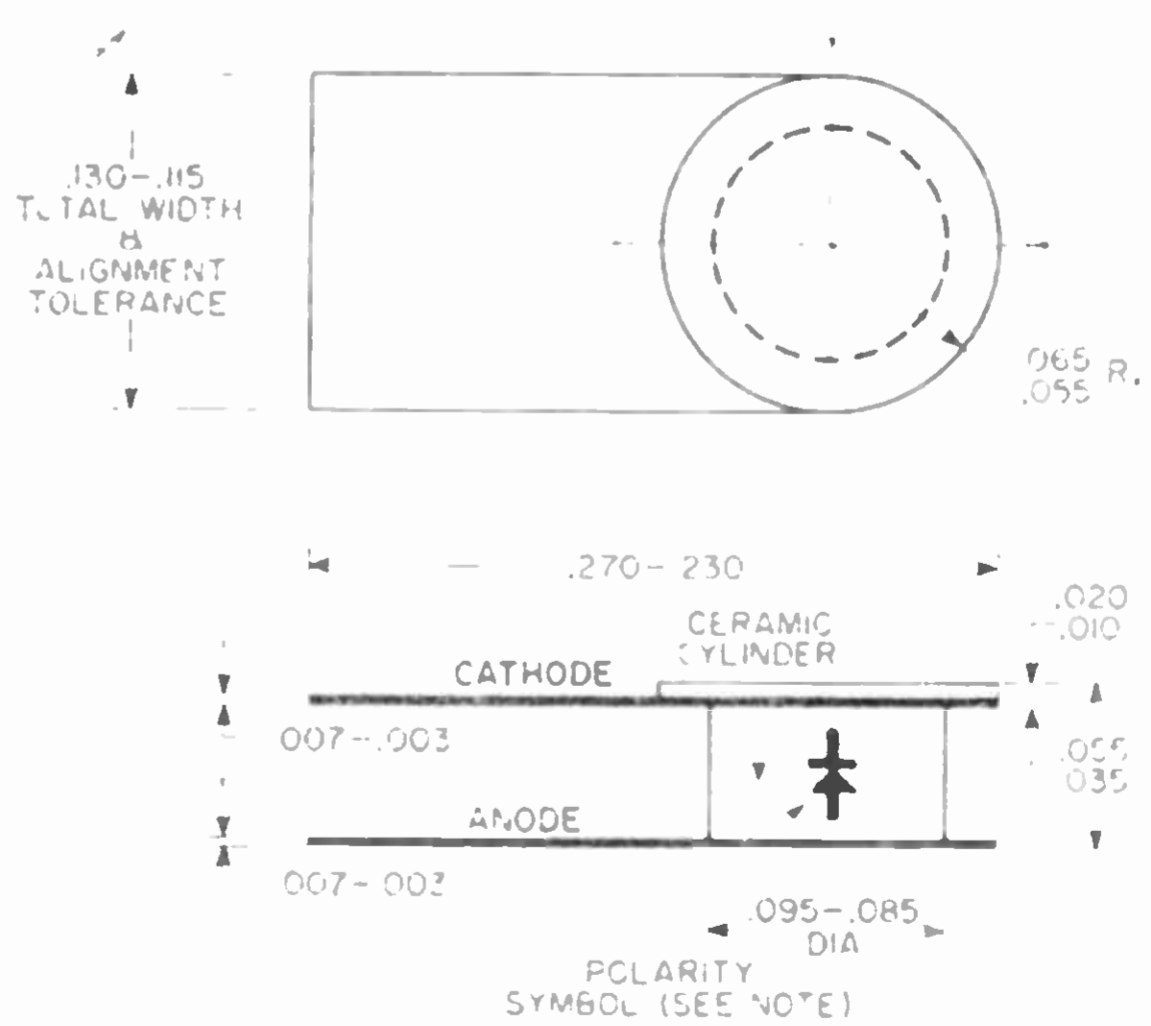


46

Outline No.	"A" (Inches)	"B"	"C"	Outline No.	"A" (Inches)	"B"	"C"
46a	2 1/4	5 1/4	2	41q	3	11 7/8	3 3/4
46b	2 1/4	7	2	41r	3	14 1/4	3 3/4
46c	2 1/4	8 3/4	2	41s	3	16 5/8	3 3/4
46d	2 1/4	10 1/2	2	41t	3	7 1/2	3 3/4
46e	2 1/4	12 1/4	2	41u	3	9 1/2	3 3/4
46f	2 1/4	14	2	41v	3	11 7/8	3 3/4
46g	2 1/4	15 3/4	2	41w	3	14 1/4	3 3/4
46h	2 1/4	5 1/4	2	41x	3	16 5/8	3 3/4
46i	2 1/4	7	2	41y	5 1/2	7 11/16	5 3/4
46j	2 1/4	8 3/4	2	41z	5 1/2	10 1/4	5 3/4
46k	2 1/4	10 1/2	2	41aa	5 1/2	12 13/16	5 3/4
46l	2 1/4	12 1/4	2	41bb	5 1/2	15 3/8	5 3/4
46m	2 1/4	14	2	41cc	5 1/2	7 11/16	5 3/4
46n	2 1/4	15 3/4	2	41dd	5 1/2	10 1/4	5 3/4
46o	3	7 1/8	3 3/8	41ee	5 1/2	12 13/16	5 3/4
46p	3	9 1/2	3 3/8	41ff	5 1/2	15 3/8	5 3/4



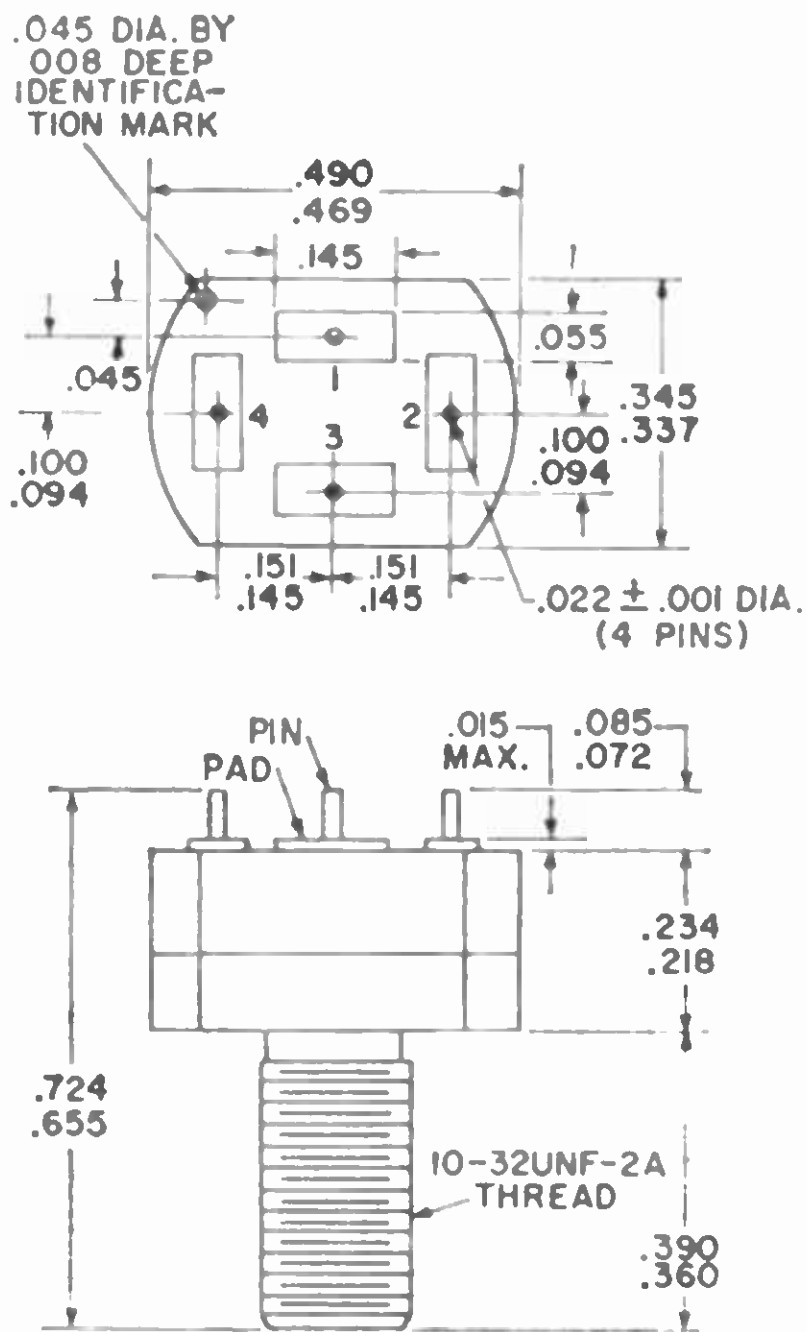
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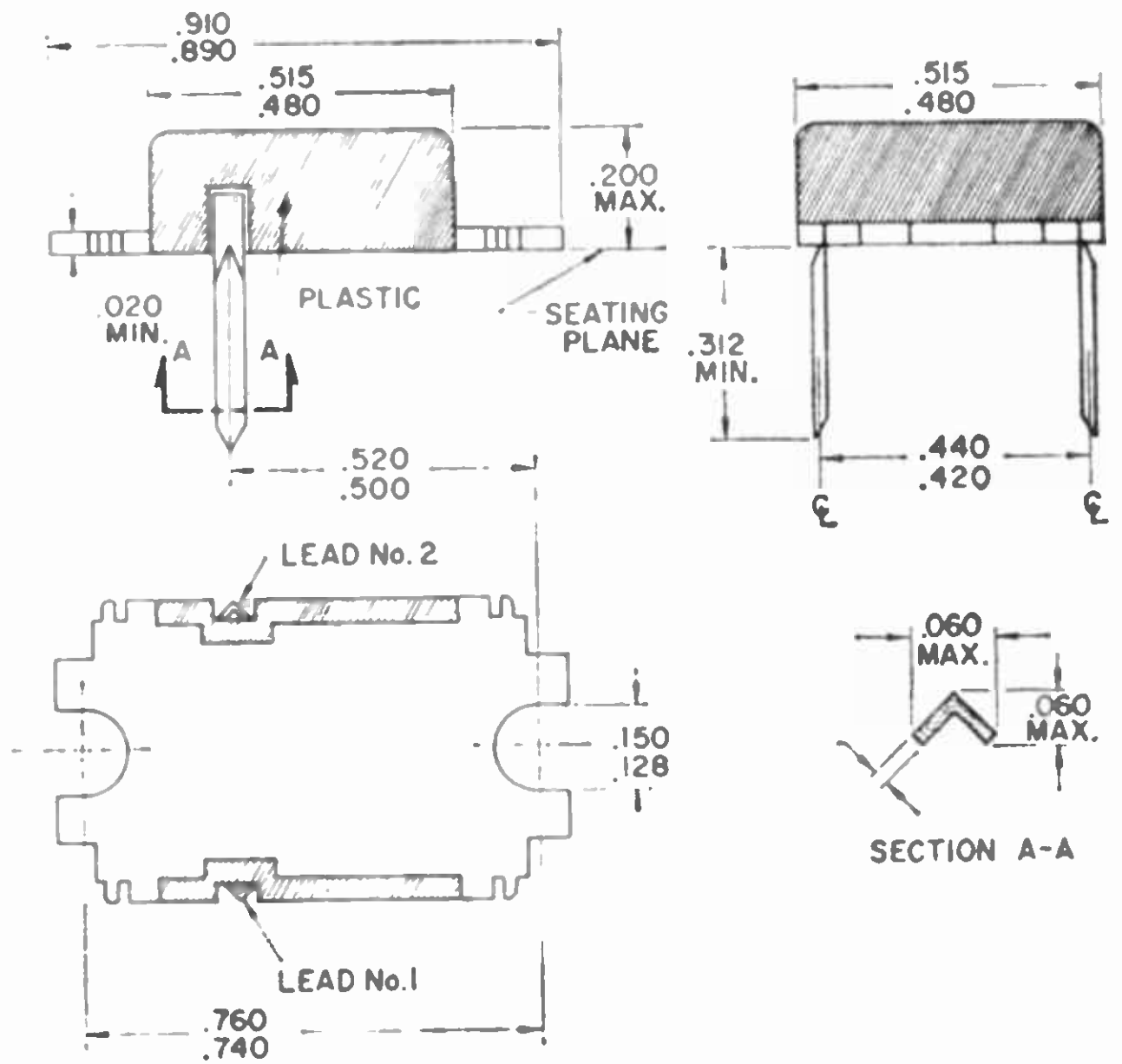
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NOTE: ARROW INDICATES DIRECTION OF FORWARD CURRENT AS INDICATED BY DC AMMETER

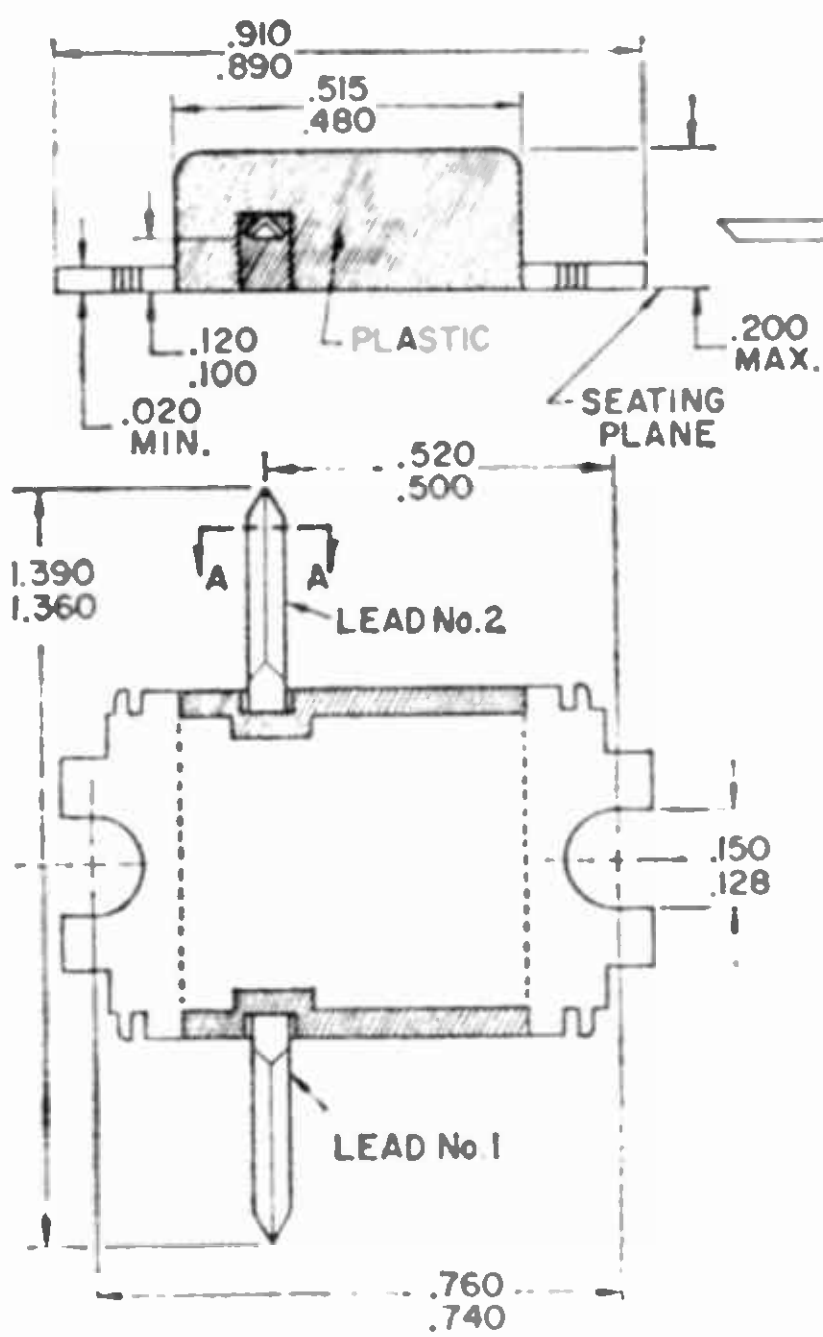
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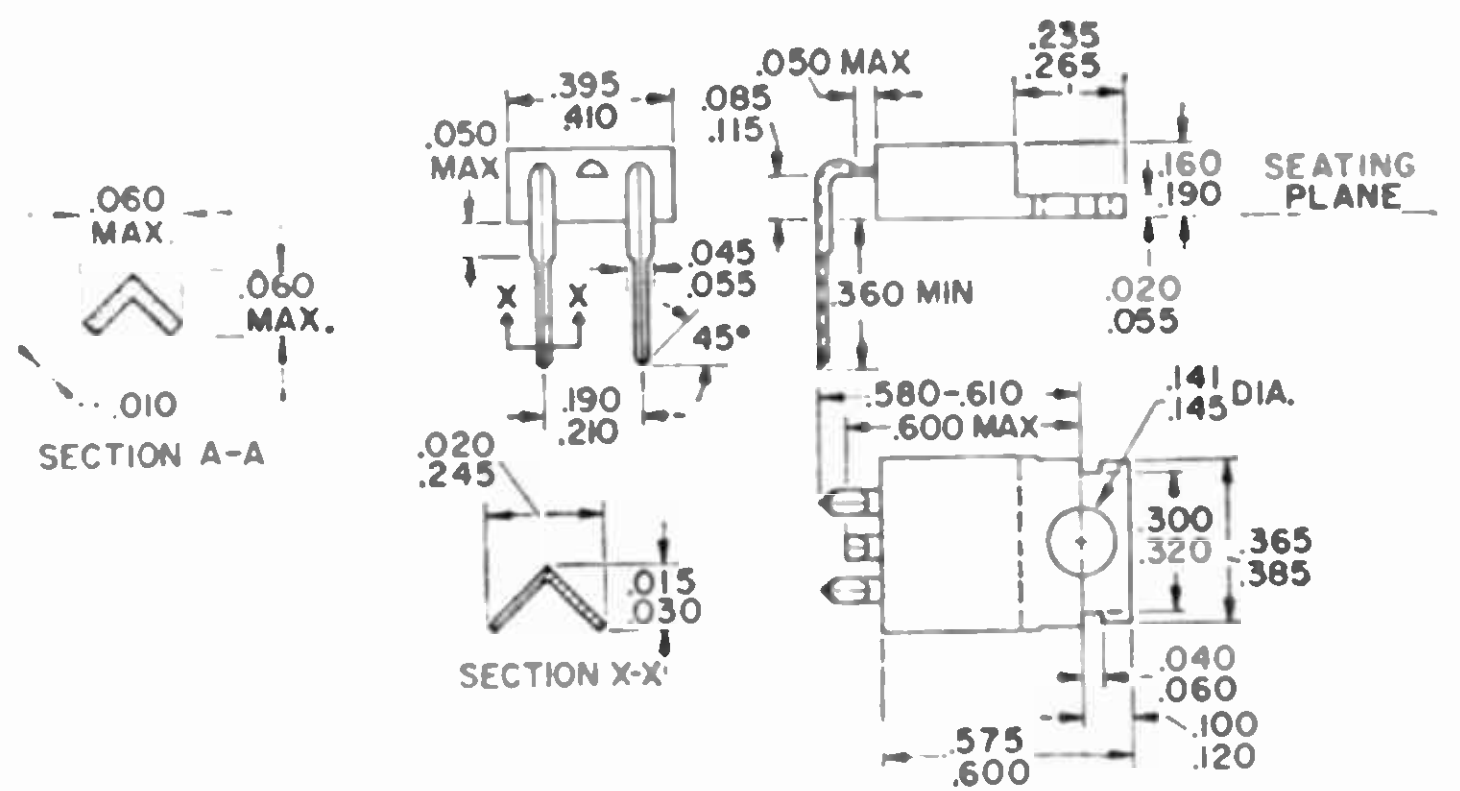
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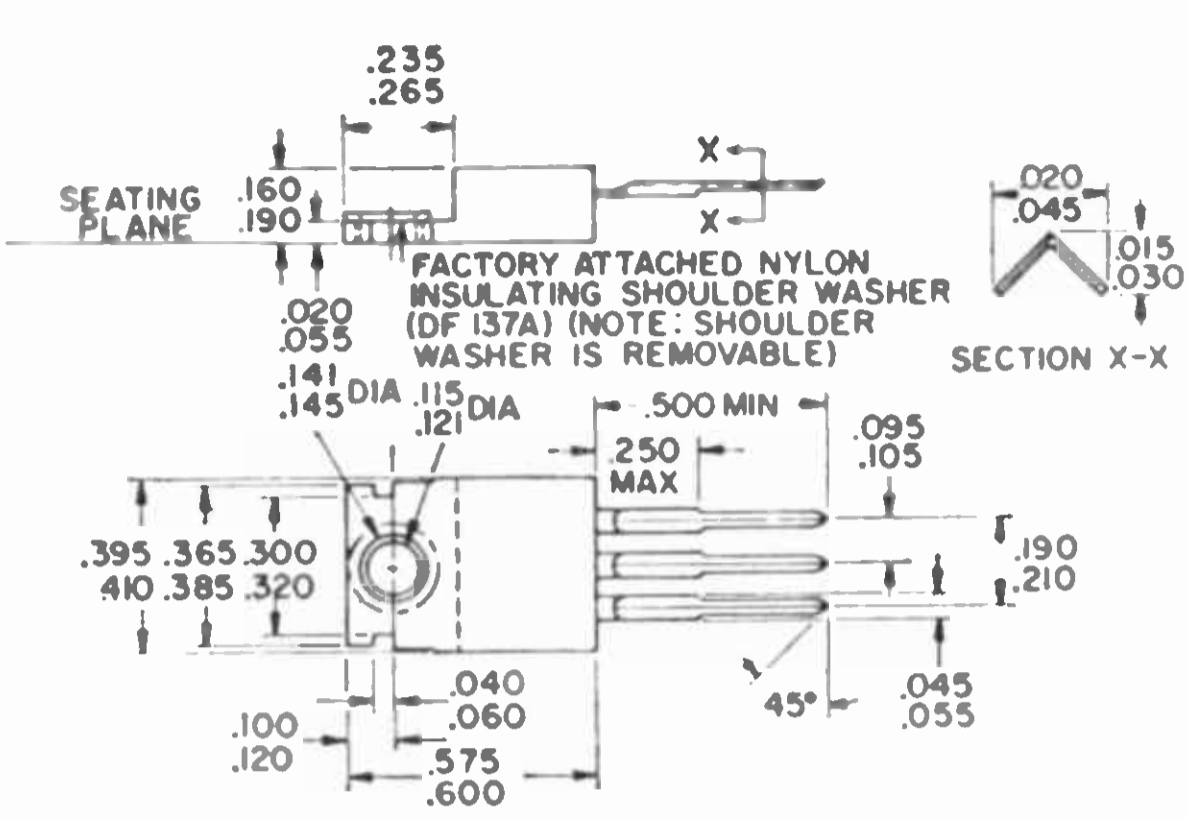


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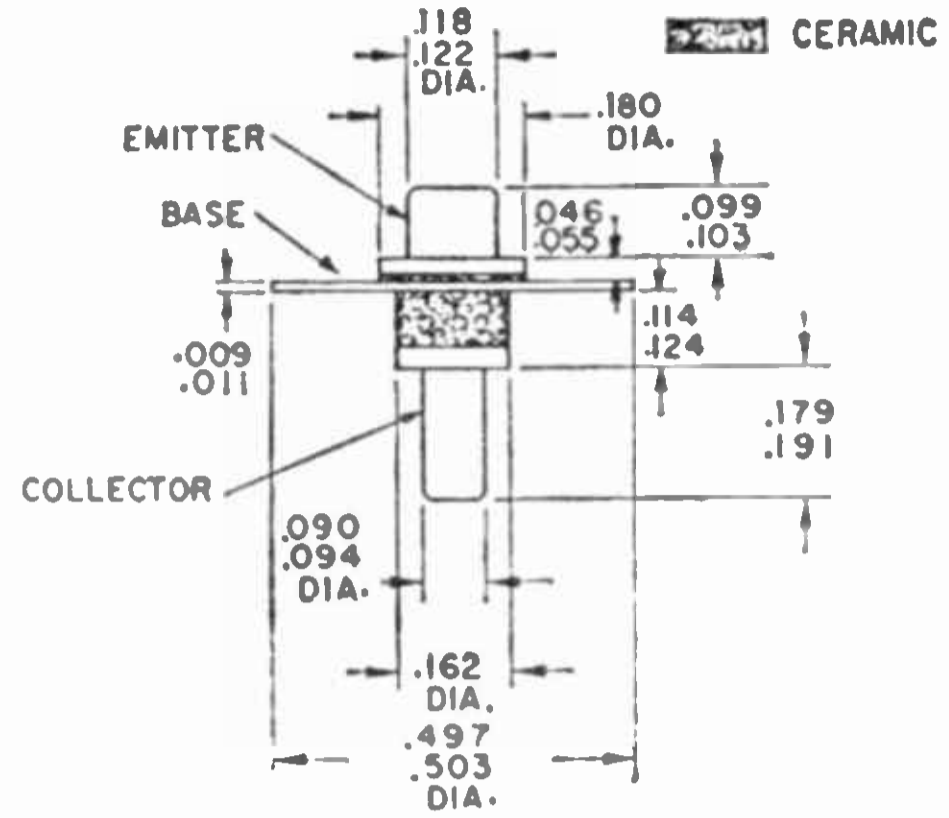


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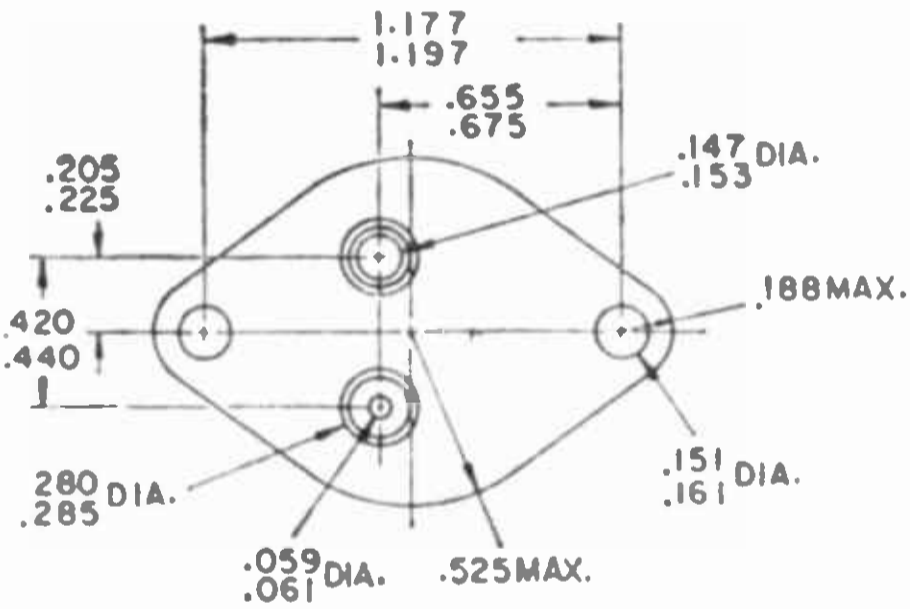
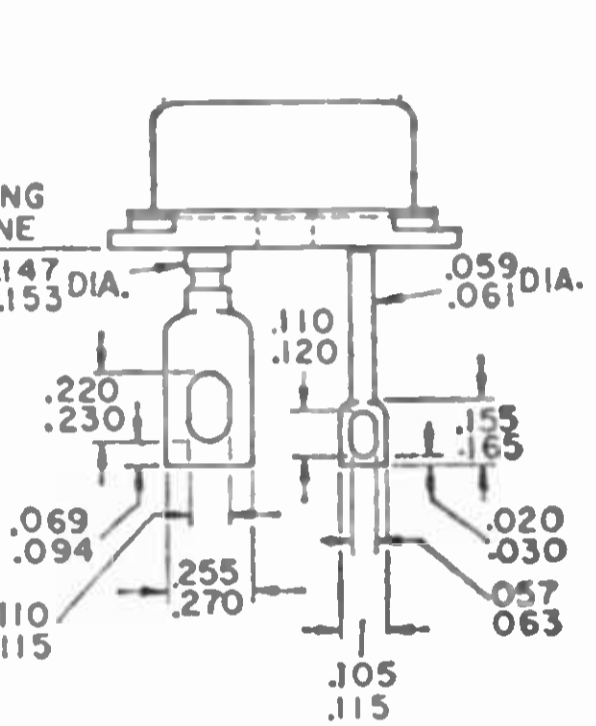
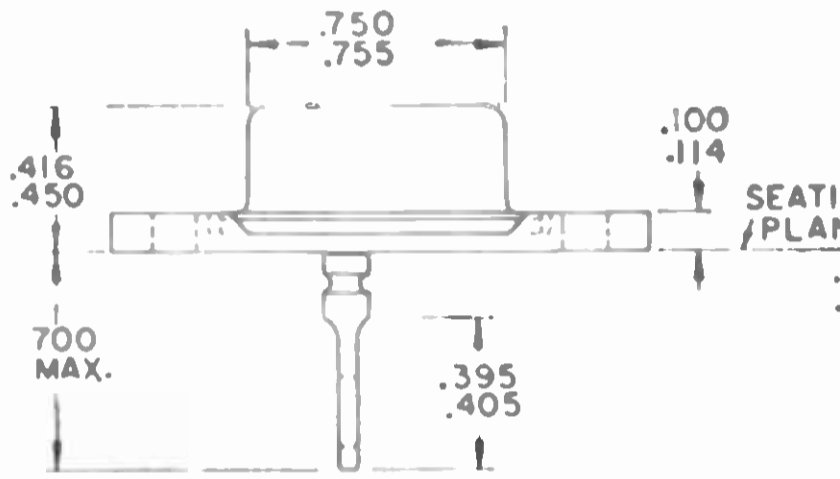
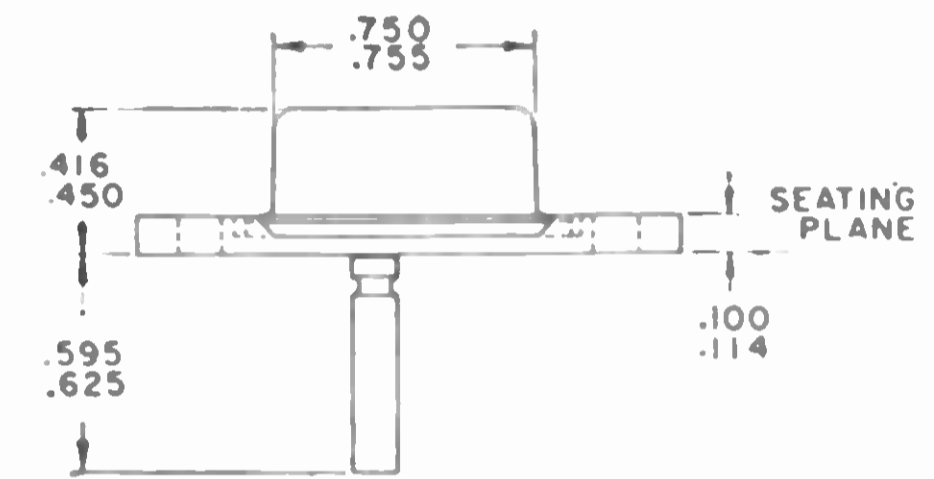
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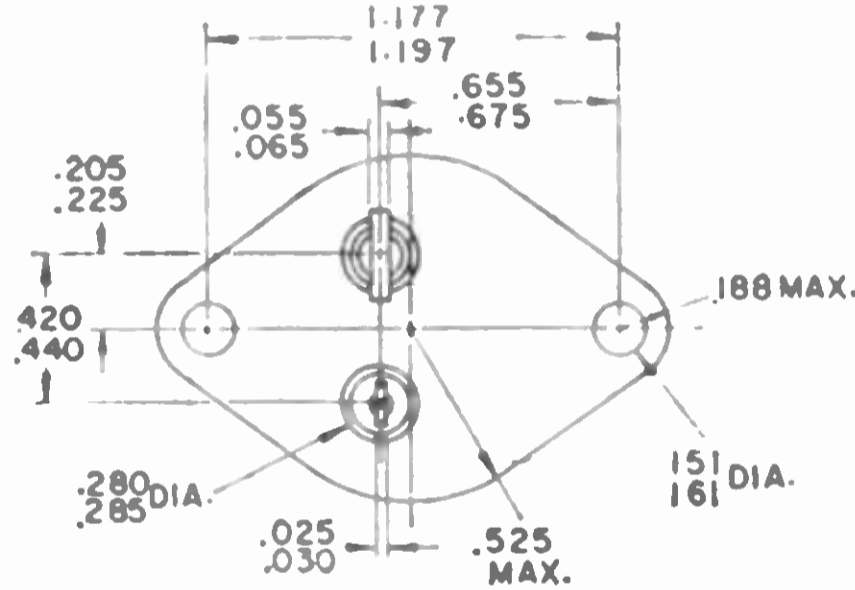
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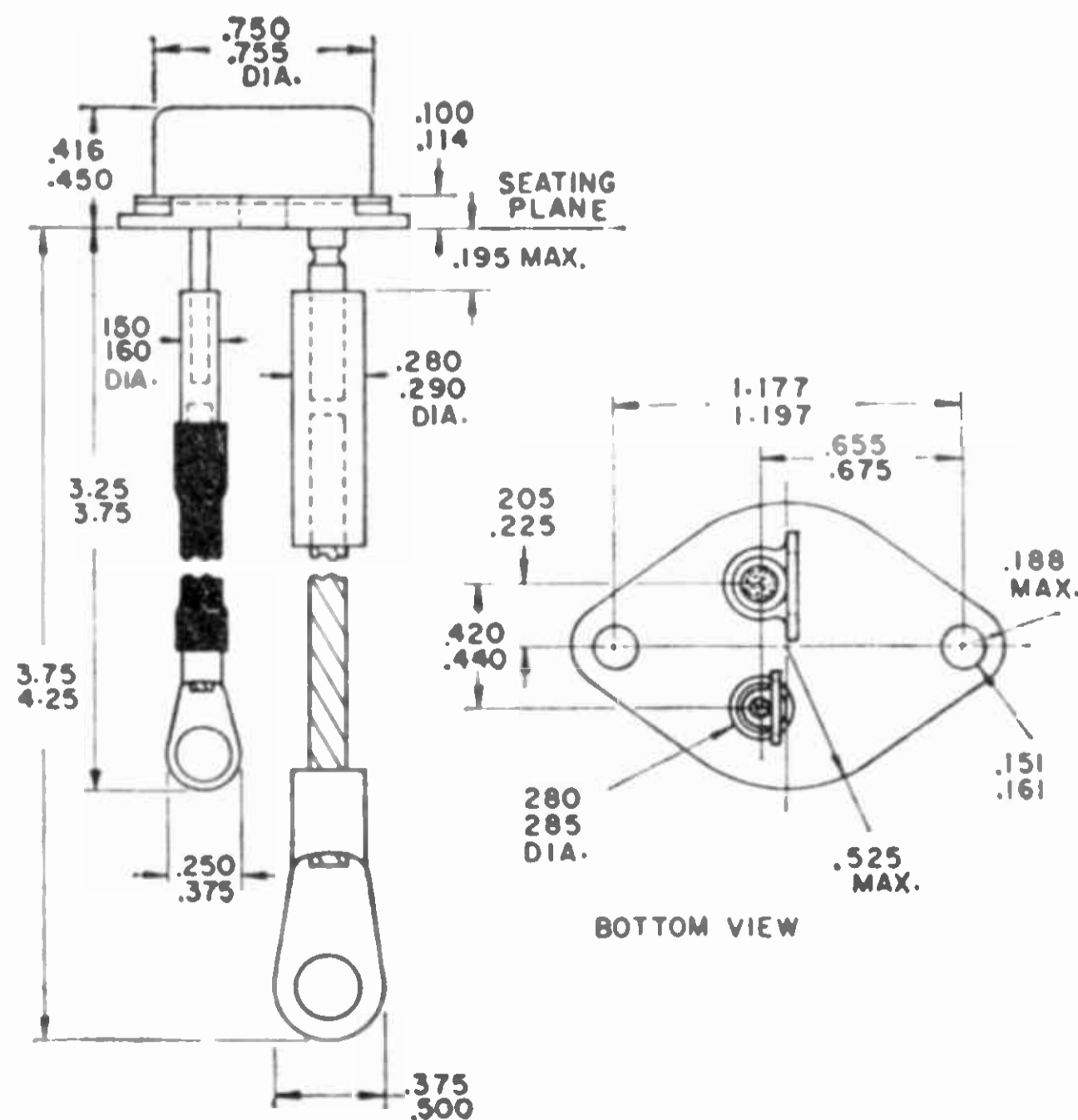
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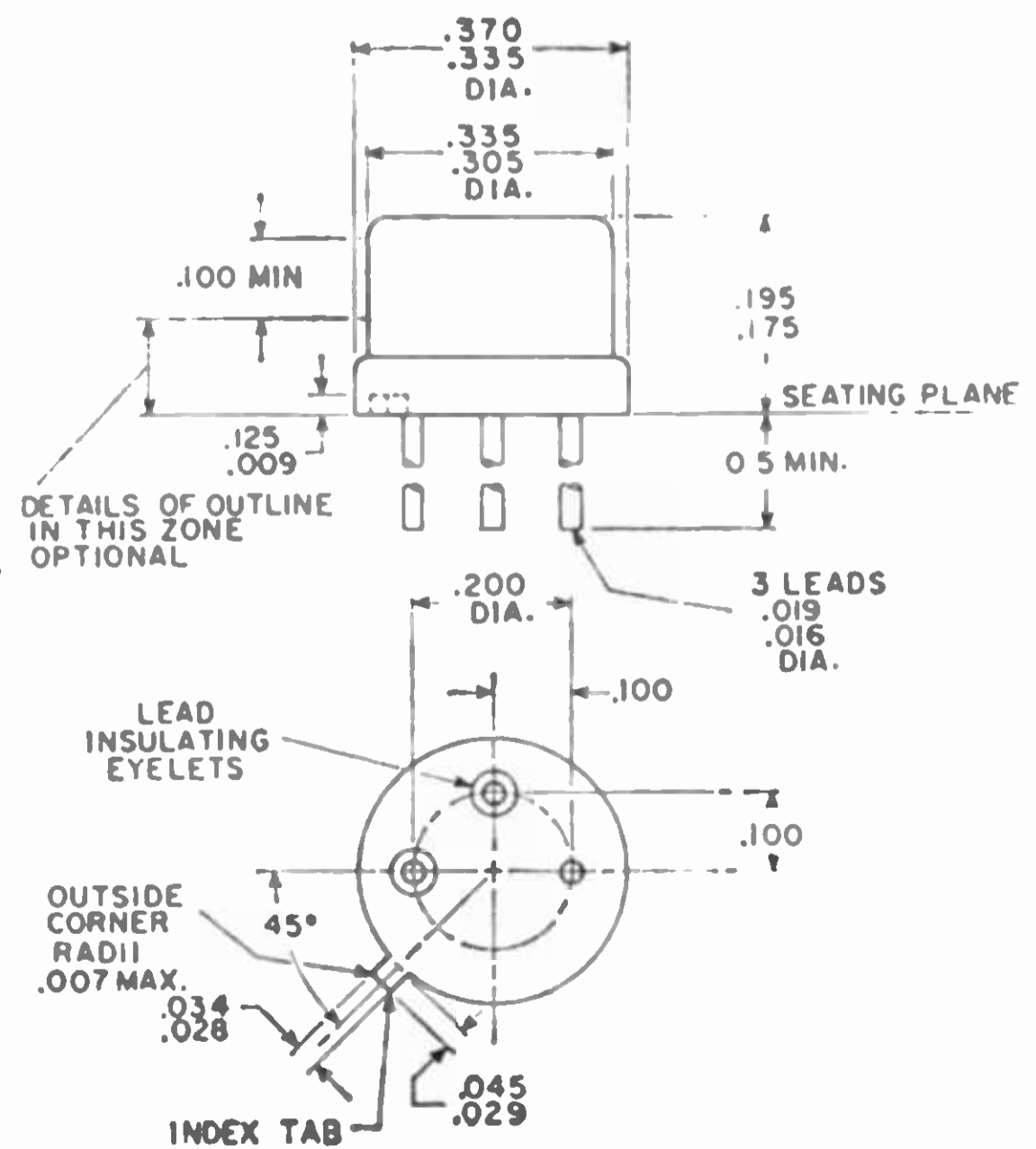
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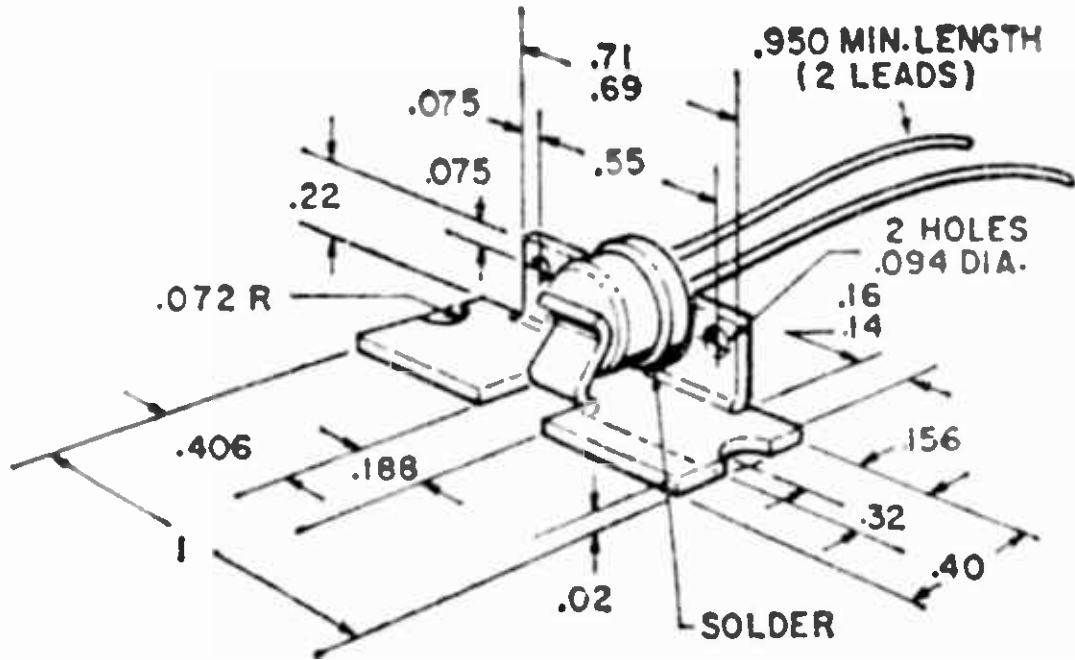


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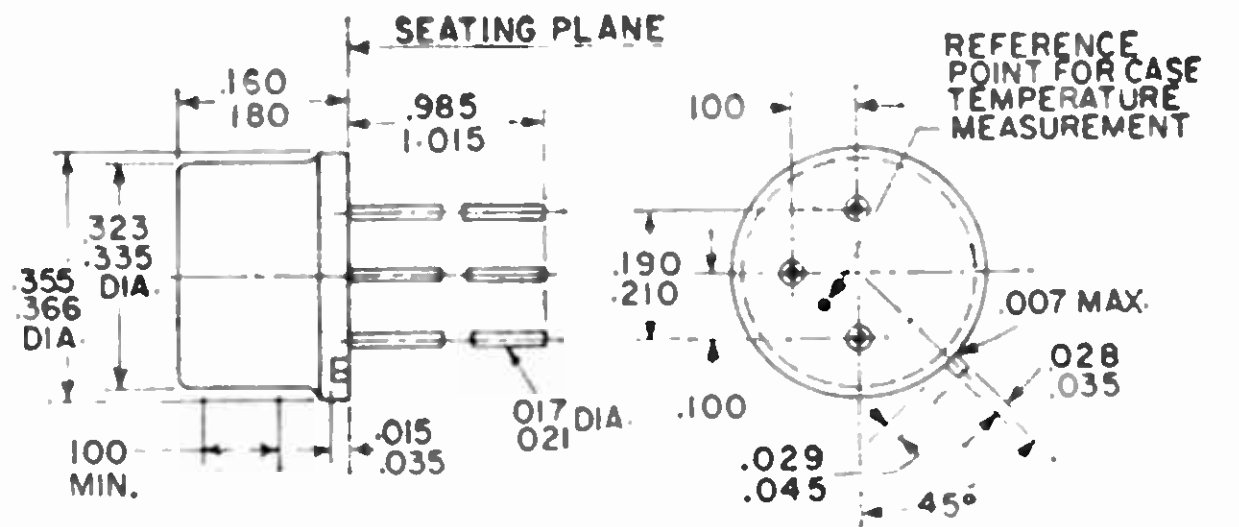


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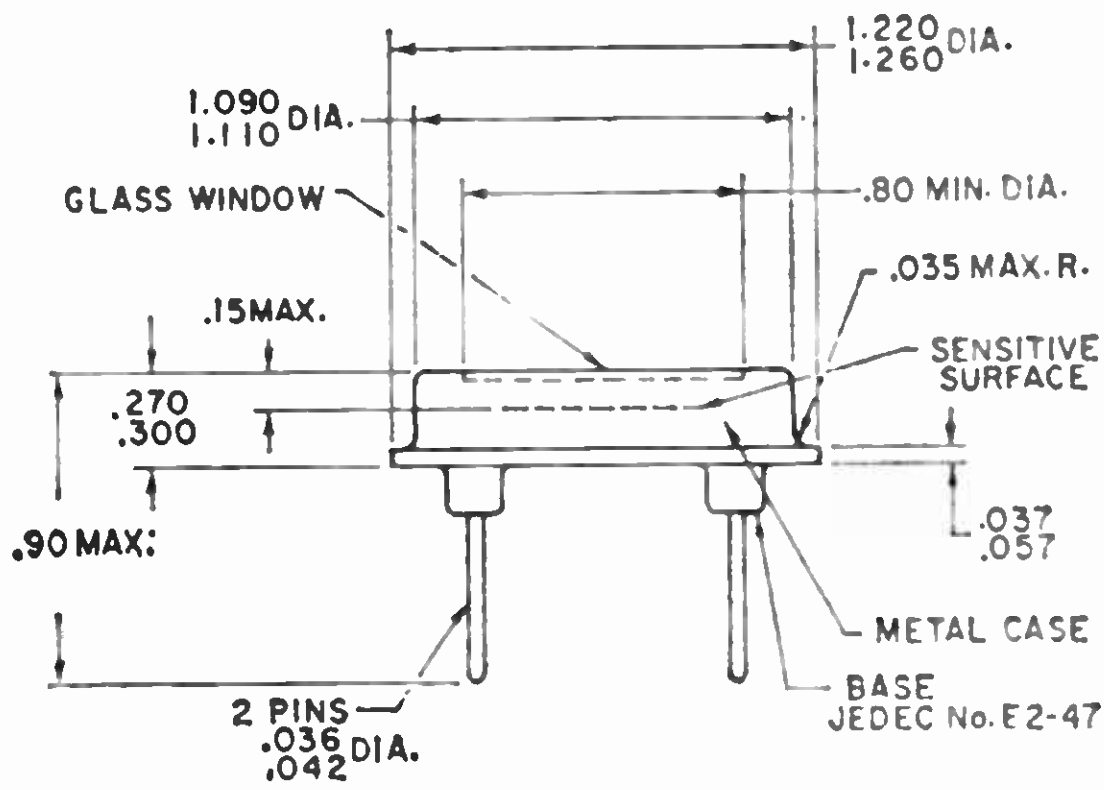
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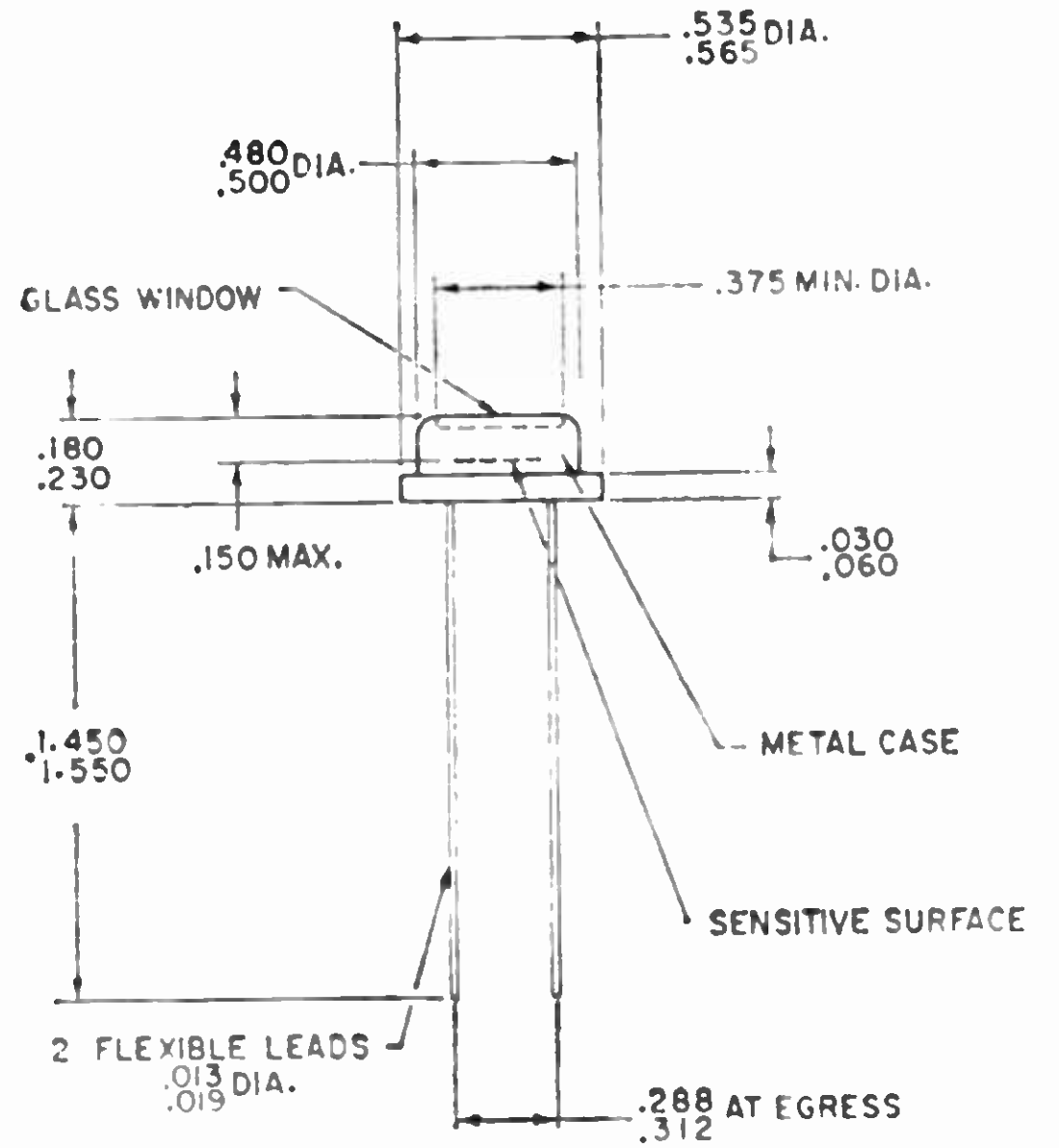
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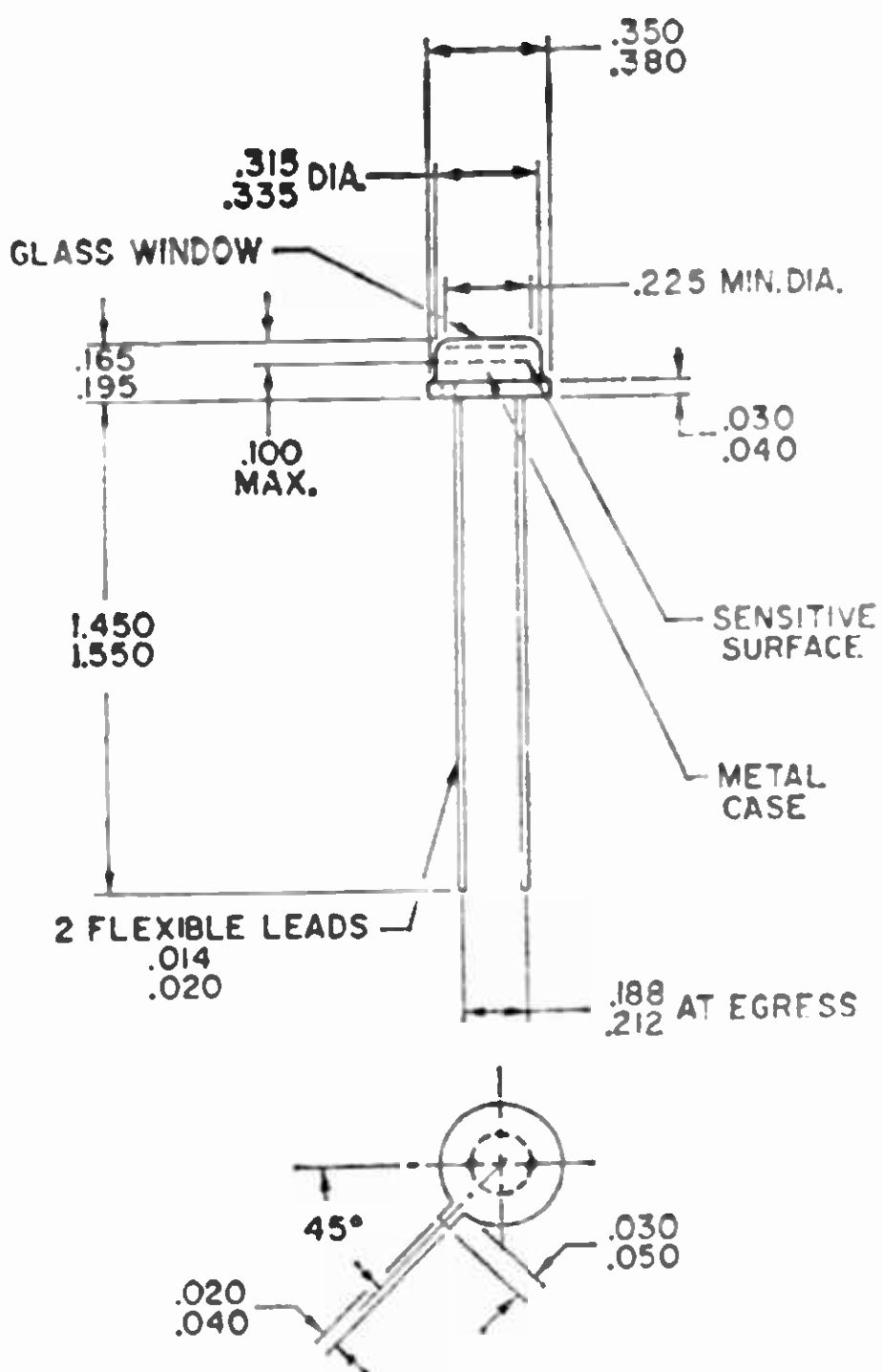
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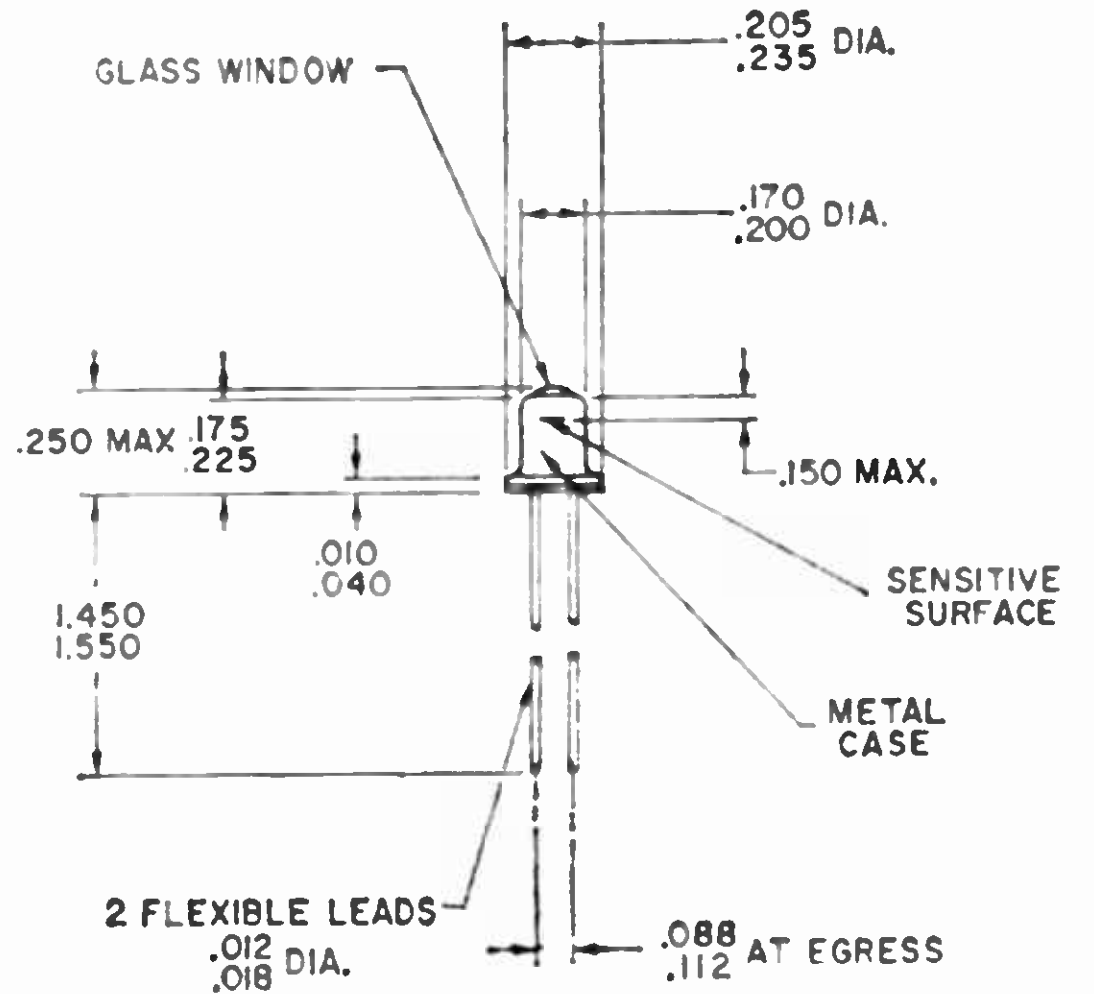
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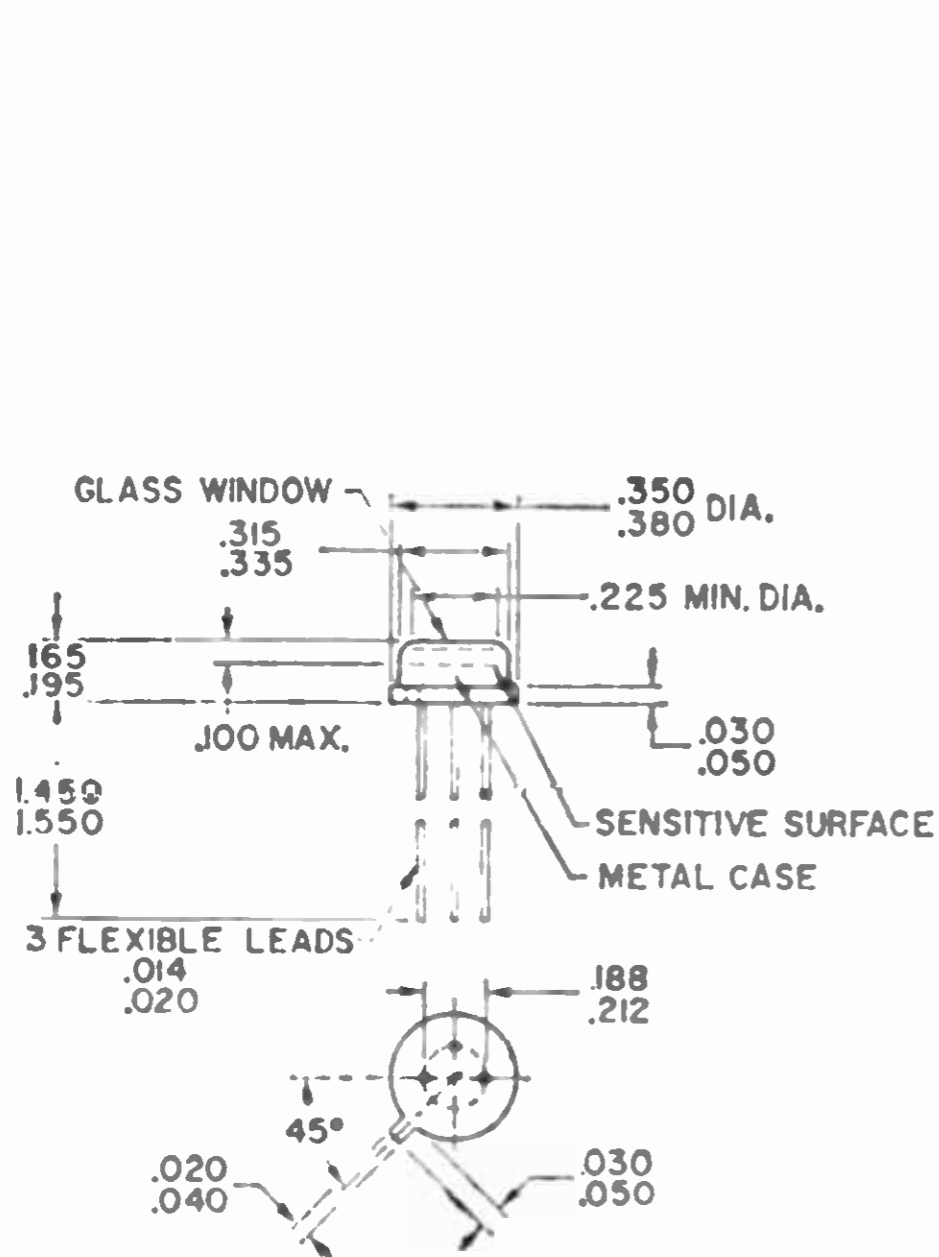


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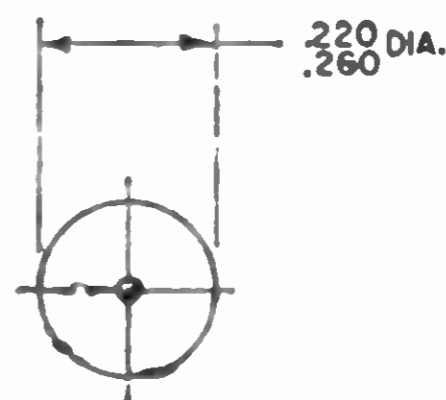
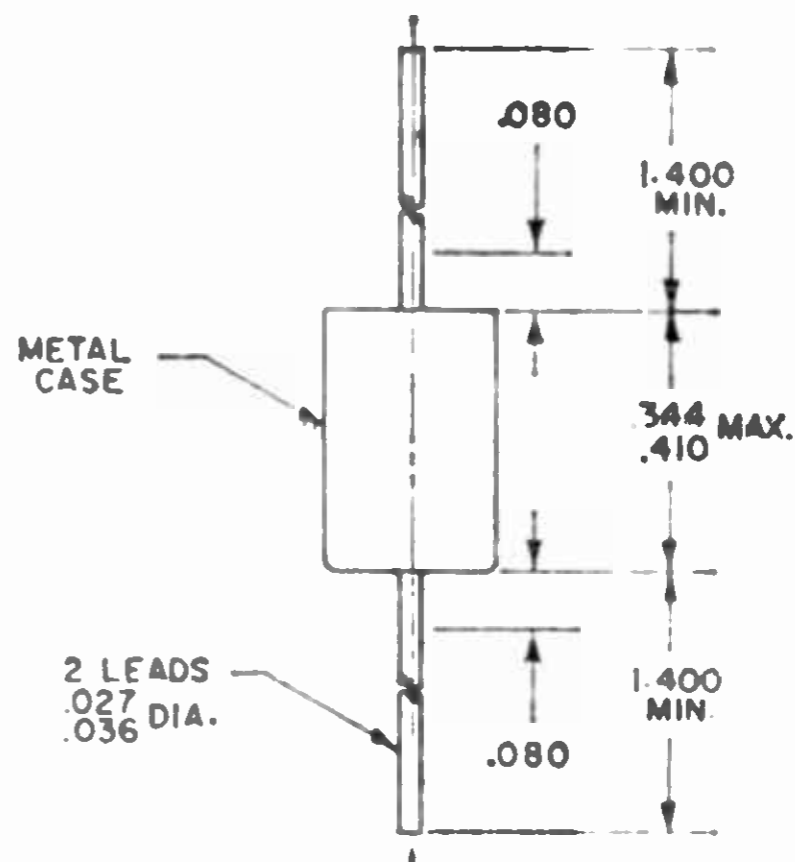
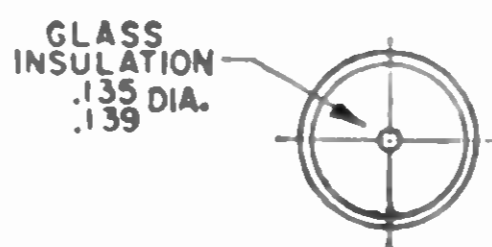


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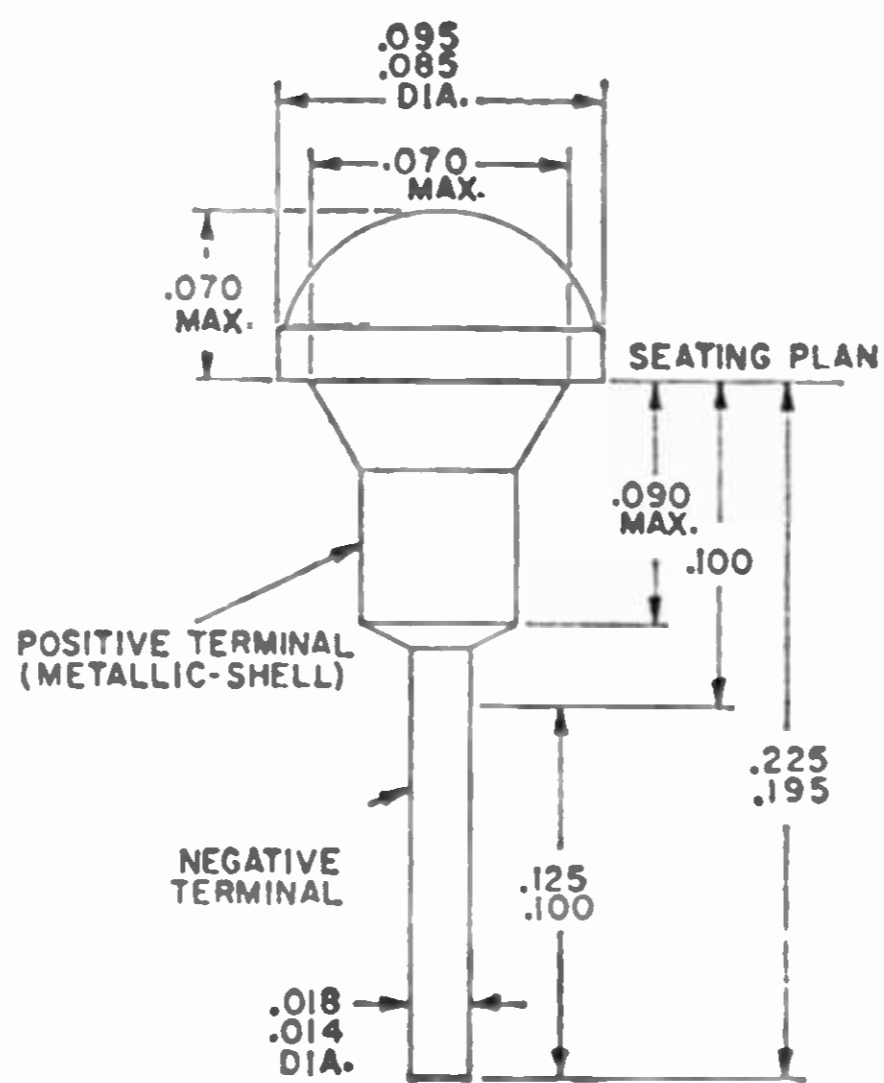
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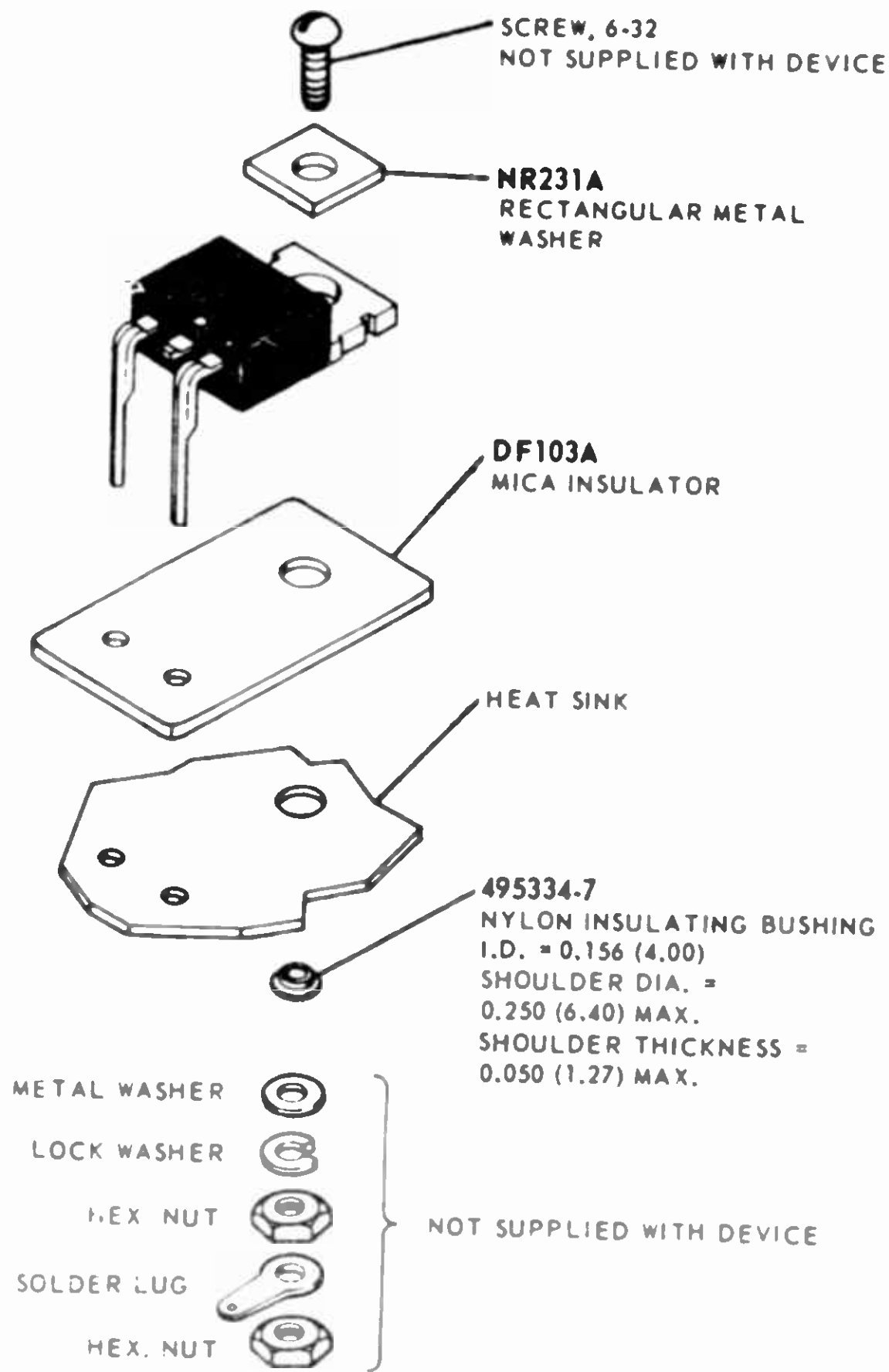
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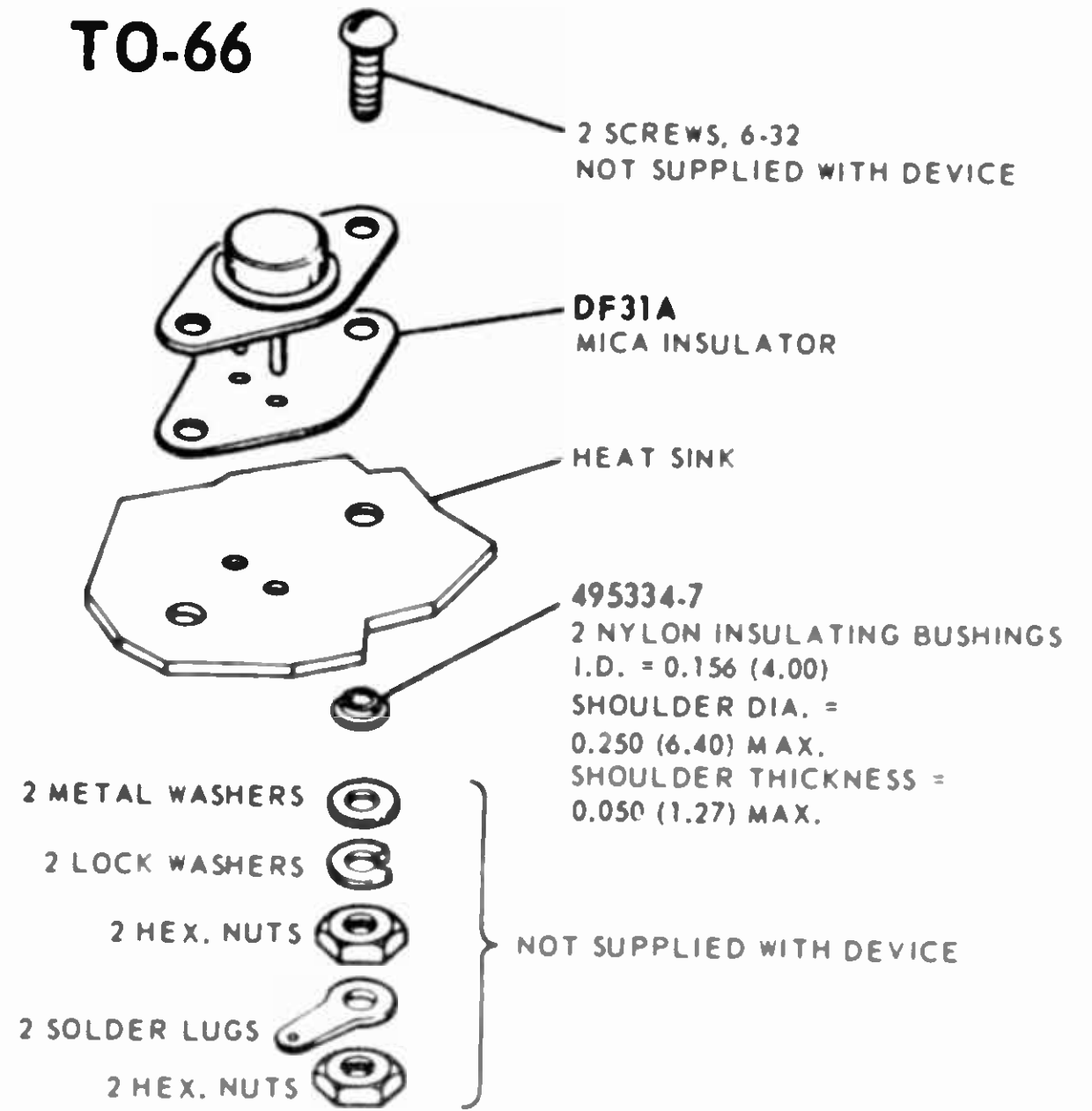
67

Mounting Hardware

CHASSIS MOUNTING (TO-60 SOCKET)



TO-66



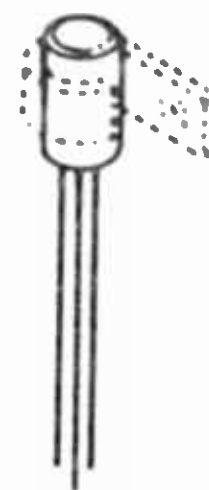
TO-1



TO-104



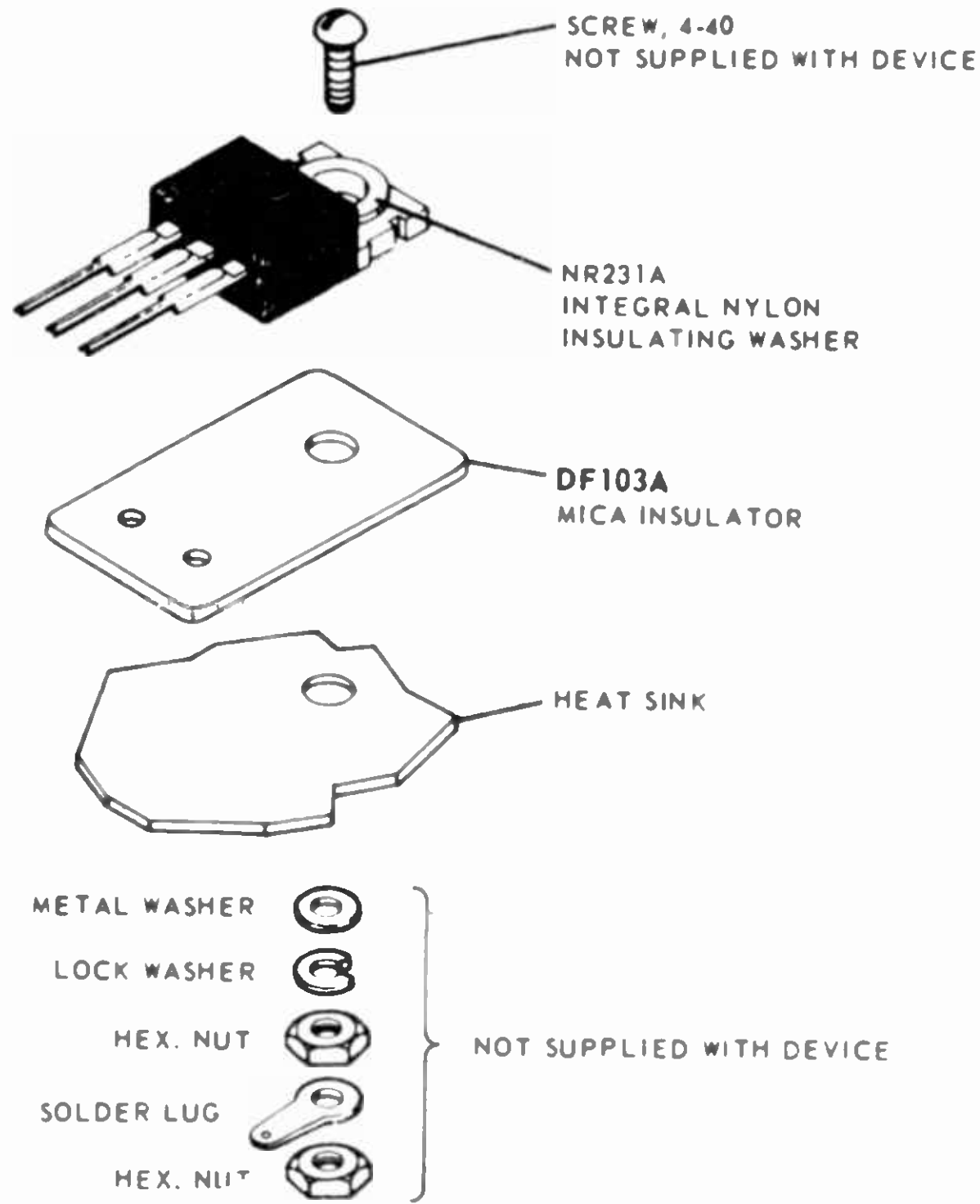
FOR MOUNTING HARDWARE INSTRUCTIONS SEE TO-1



^oPort is not supplied with device but is available from RCA or an authorized RCA distributor.

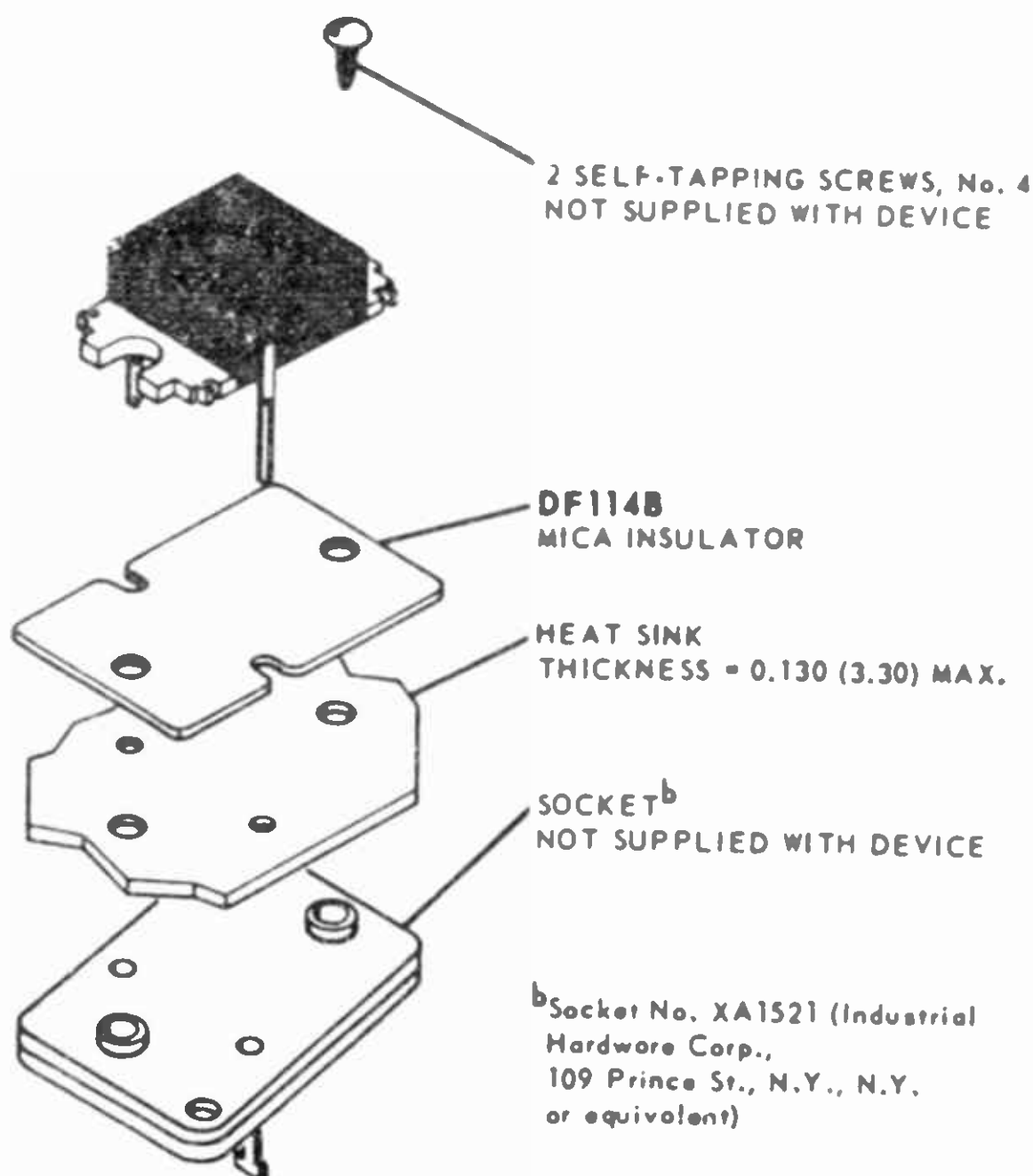
Mounting Hardware (cont'd)

PRINTED-CIRCUIT BOARD MOUNTING
(ALTERNATE ARRANGEMENT)

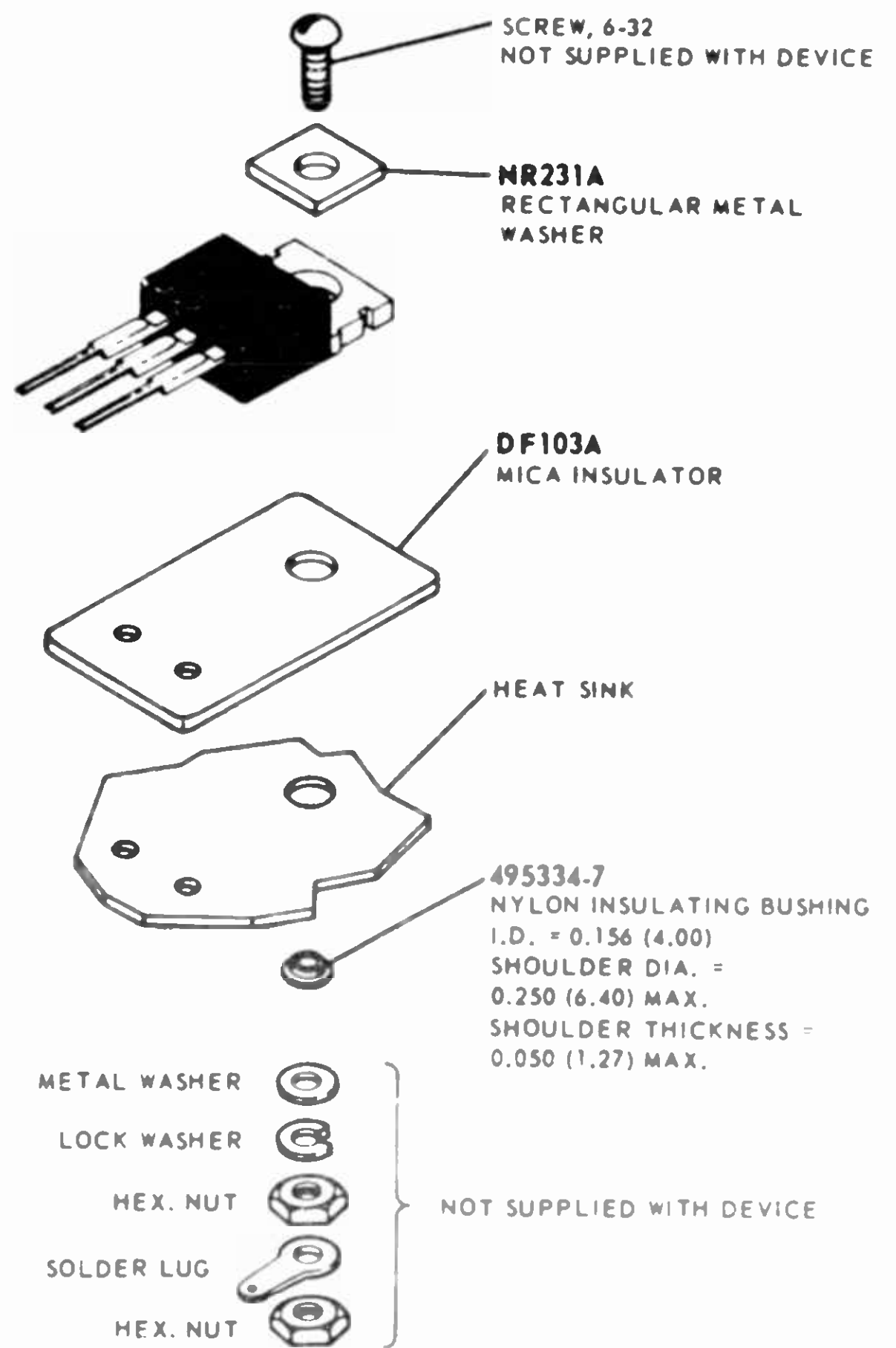


SOCKET MOUNTING

Although supplied, the insulating bushing is not required when the transistor is socket mounted.

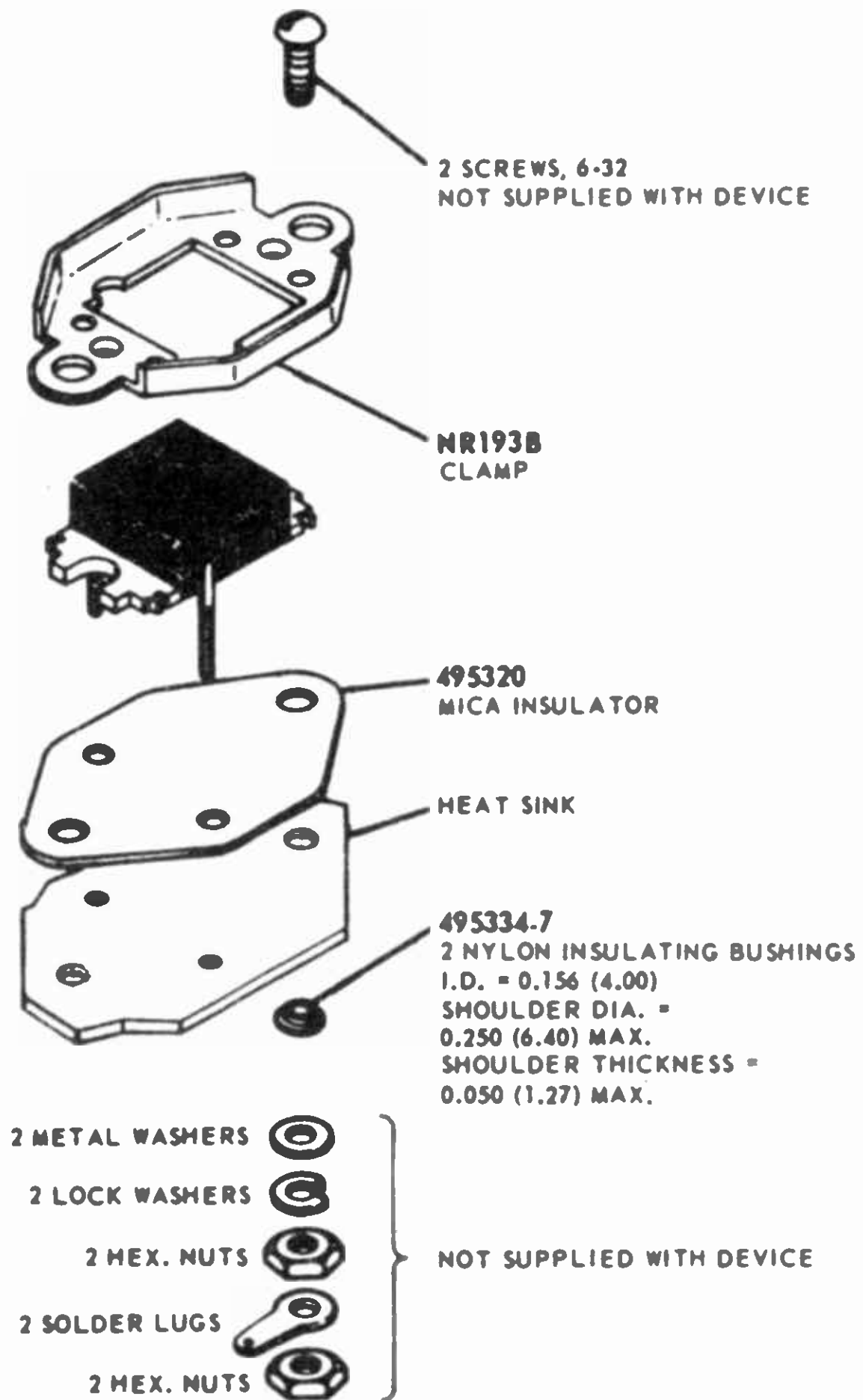


PRINTED-CIRCUIT BOARD MOUNTING

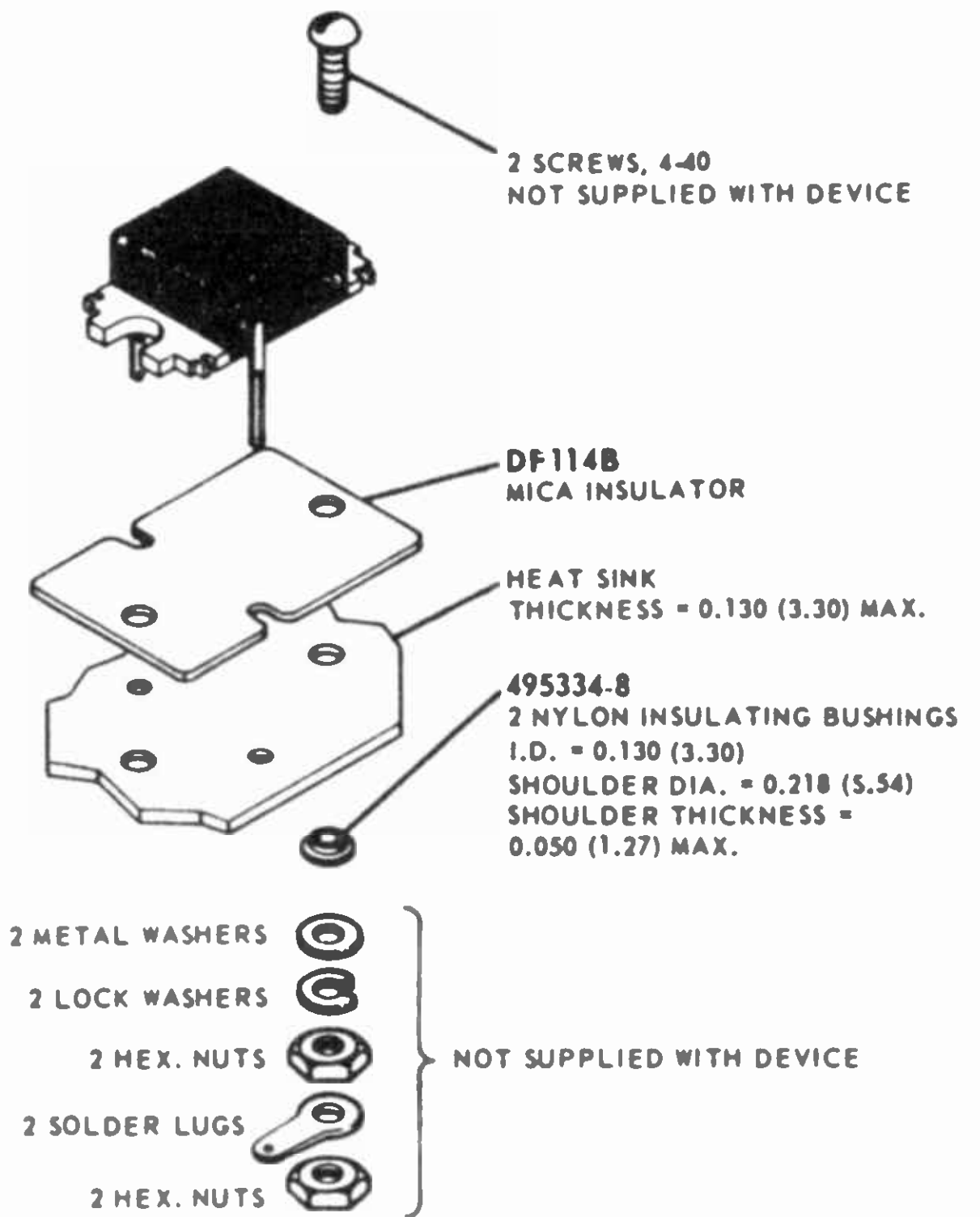


Mounting Hardware (cont'd)

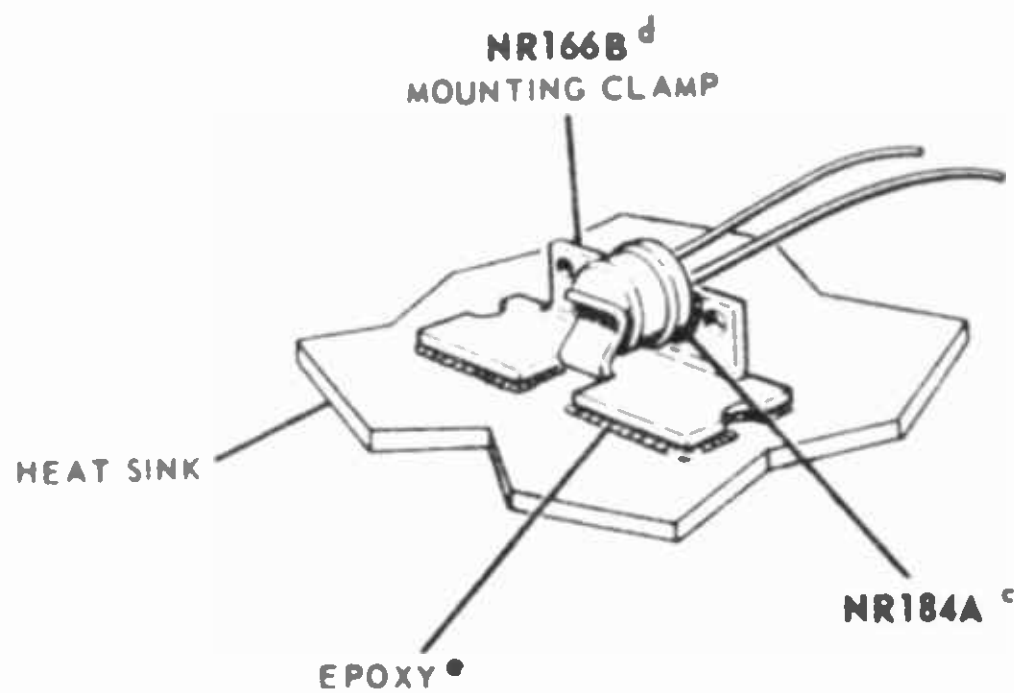
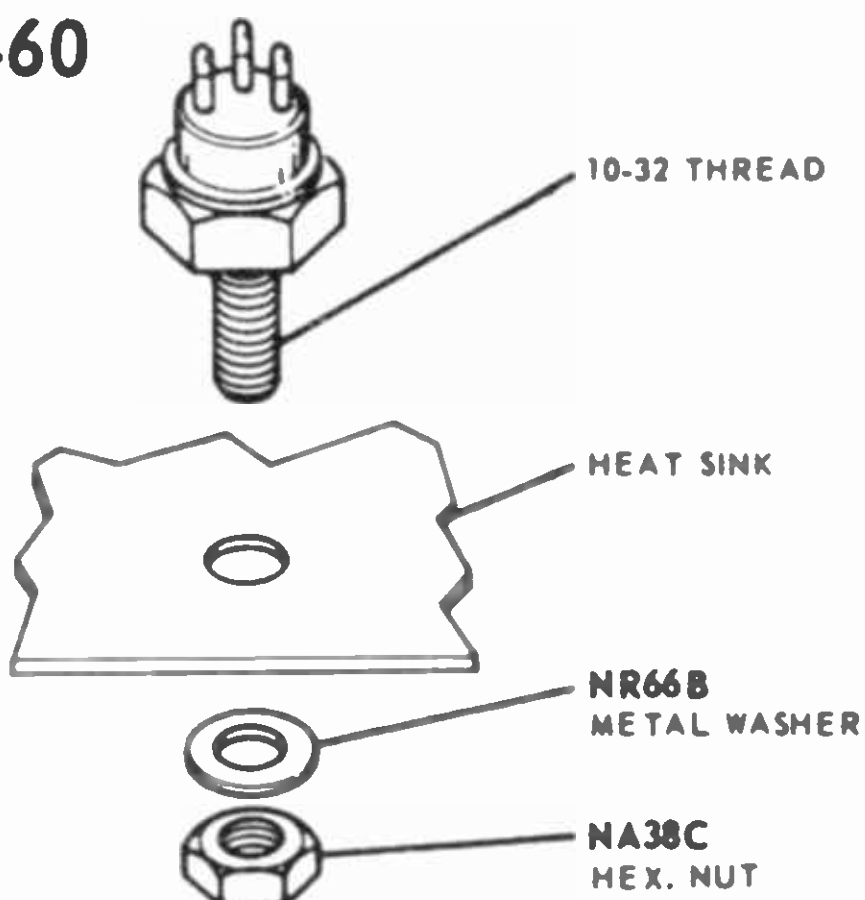
CHASSIS MOUNTING WITH TOP CLAMP
(ALTERNATE ARRANGEMENT)



CHASSIS MOUNTING



TO-60



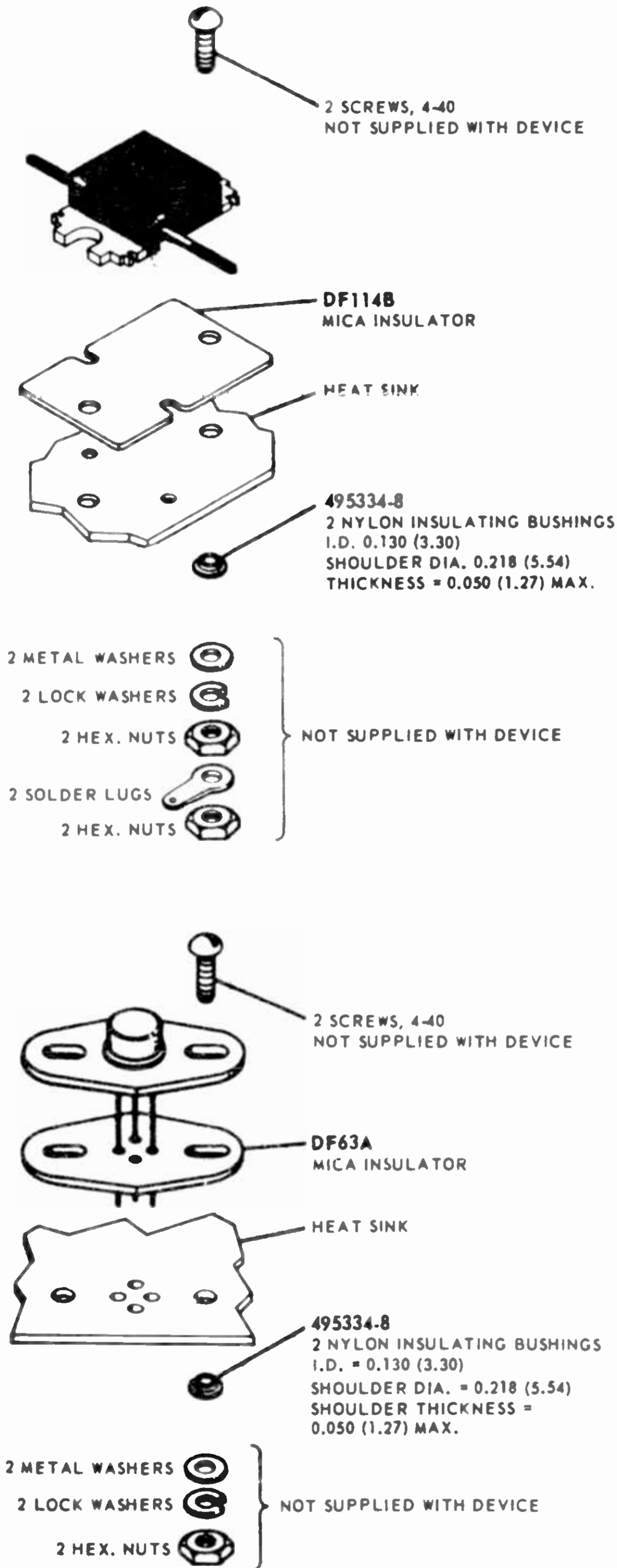
^c Part is not supplied with device but is available from RCA (Part No. NR184A) and from Kester Solder Co., Newark, N.J. 07105, (Part No. KSFD-375005) or equivalent.

^d Part is not supplied with device but is available from RCA (Part No. NR166B) and from General Stamping Co., Inc., Denville, N.J. 07834 (Part No. 14-110), or equivalent.

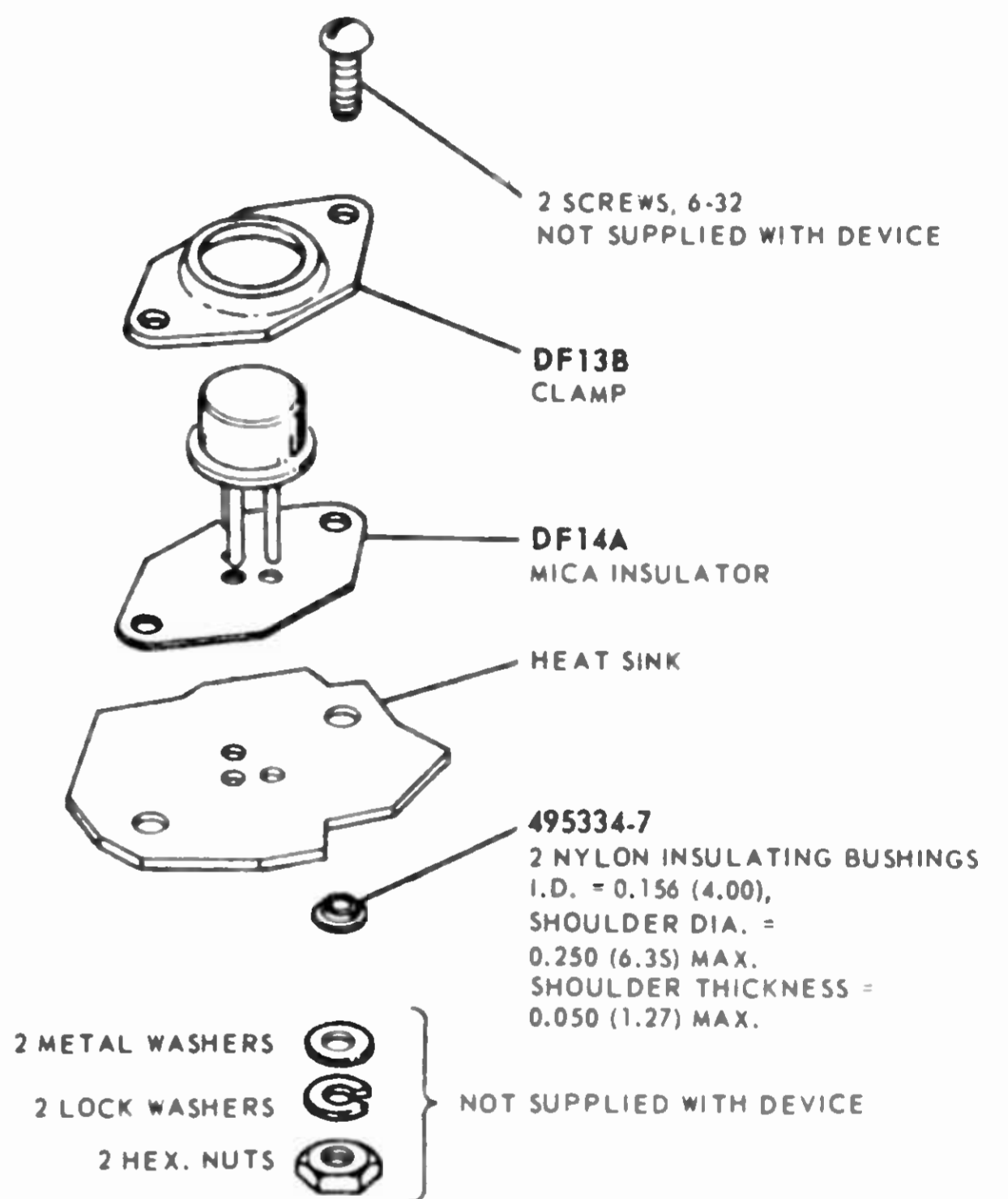
^e An epoxy such as Hysol-Epoxy Patch Kit 6C, Hysol Corp., Olean, N.Y. 14761 or equivalent.

Mounting Hardware (cont'd)

PRINTED-CIRCUIT BOARD MOUNTING

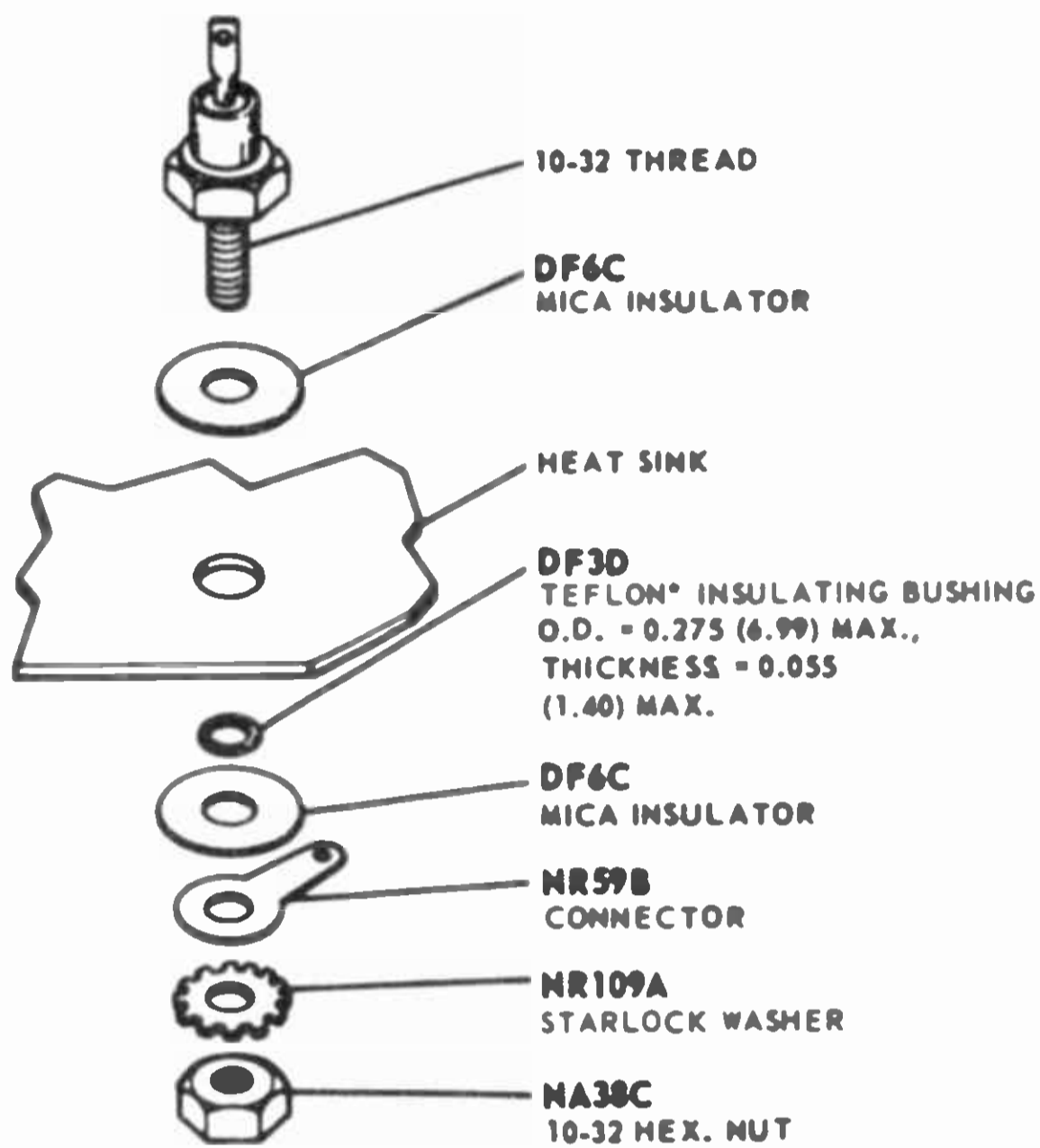


TO-8



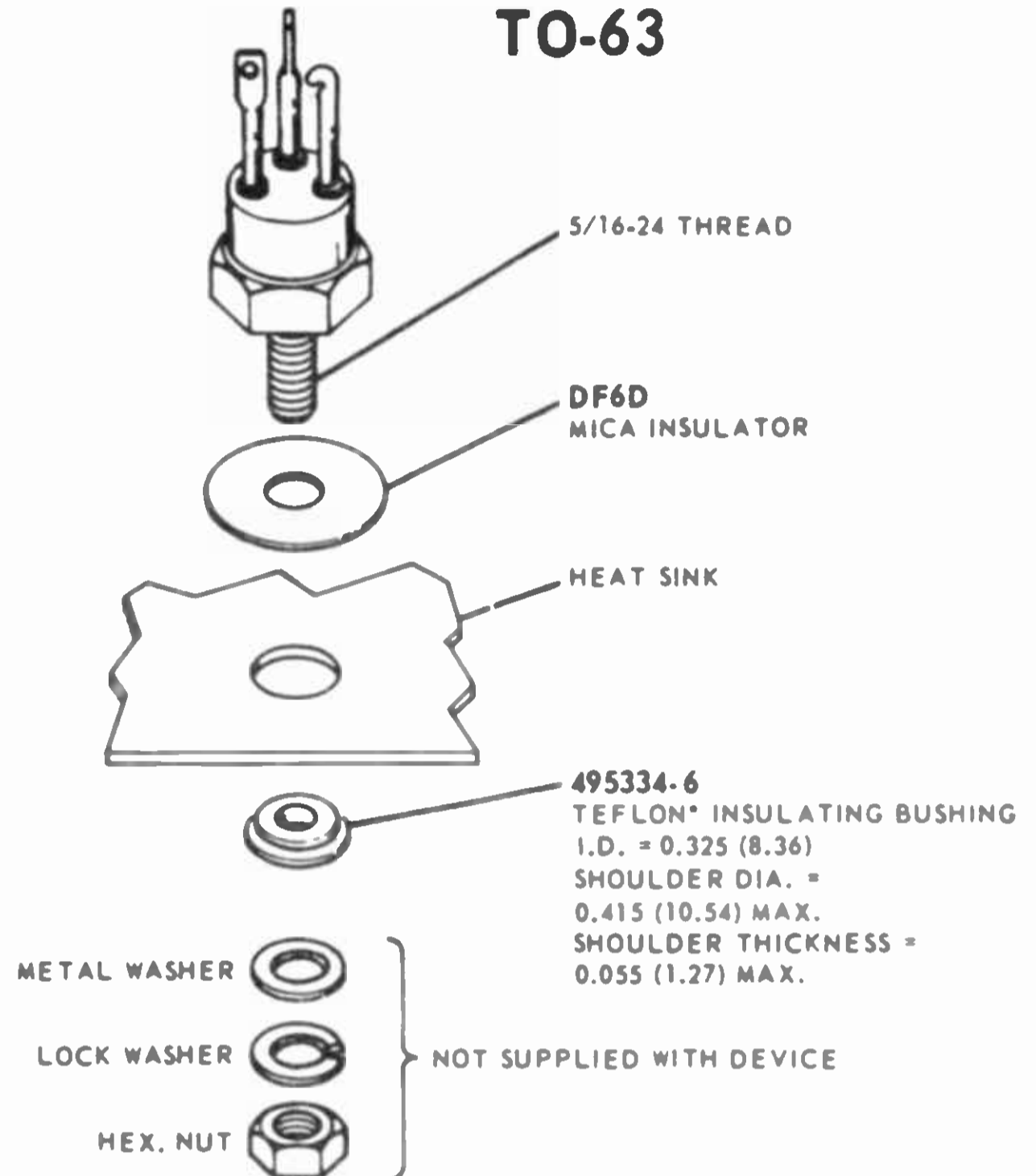
Mounting Hardware (cont'd)

DO-4



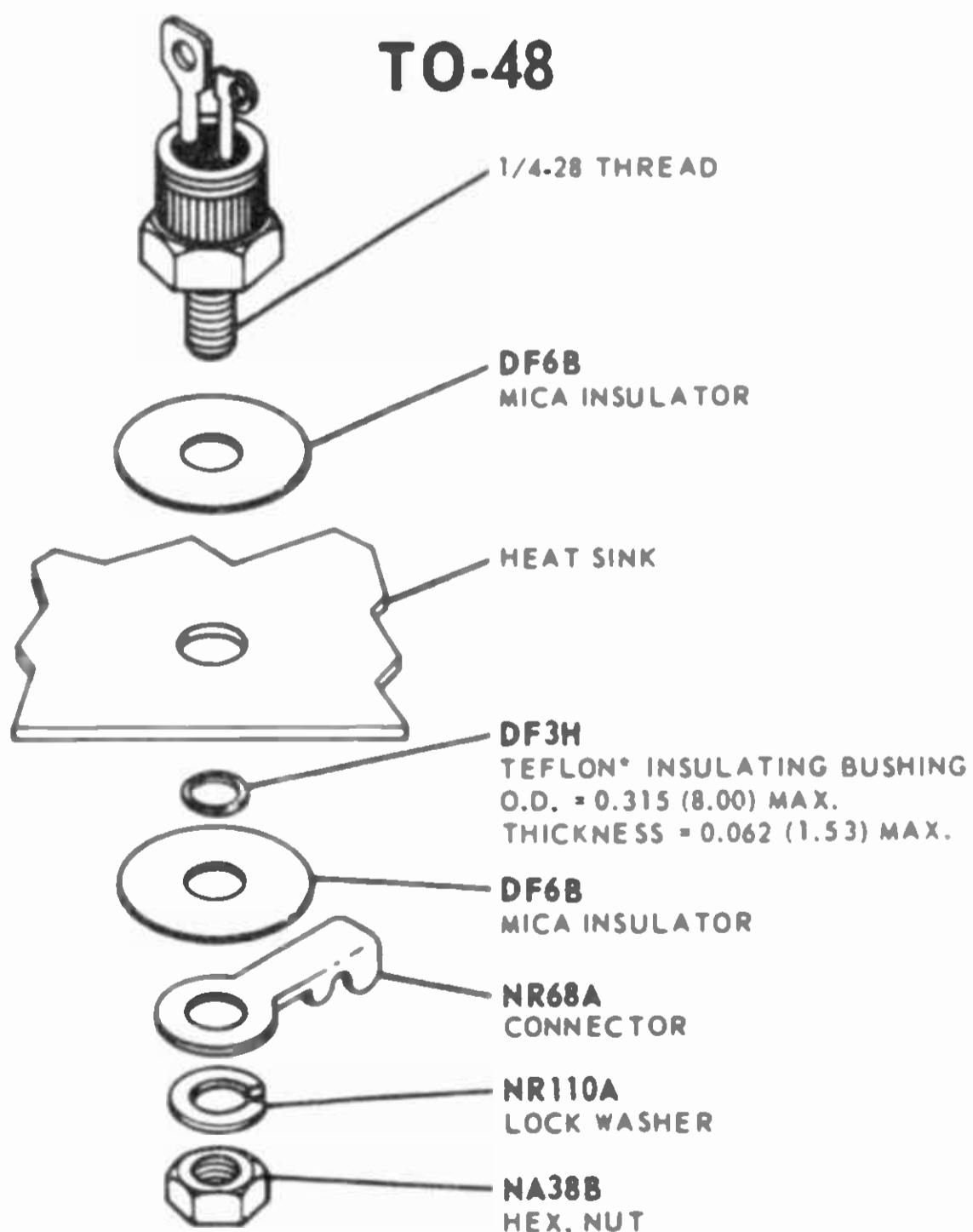
*REGISTERED TRADEMARK OF E.I. DUPONT DE NEMOURS & CO.

TO-63



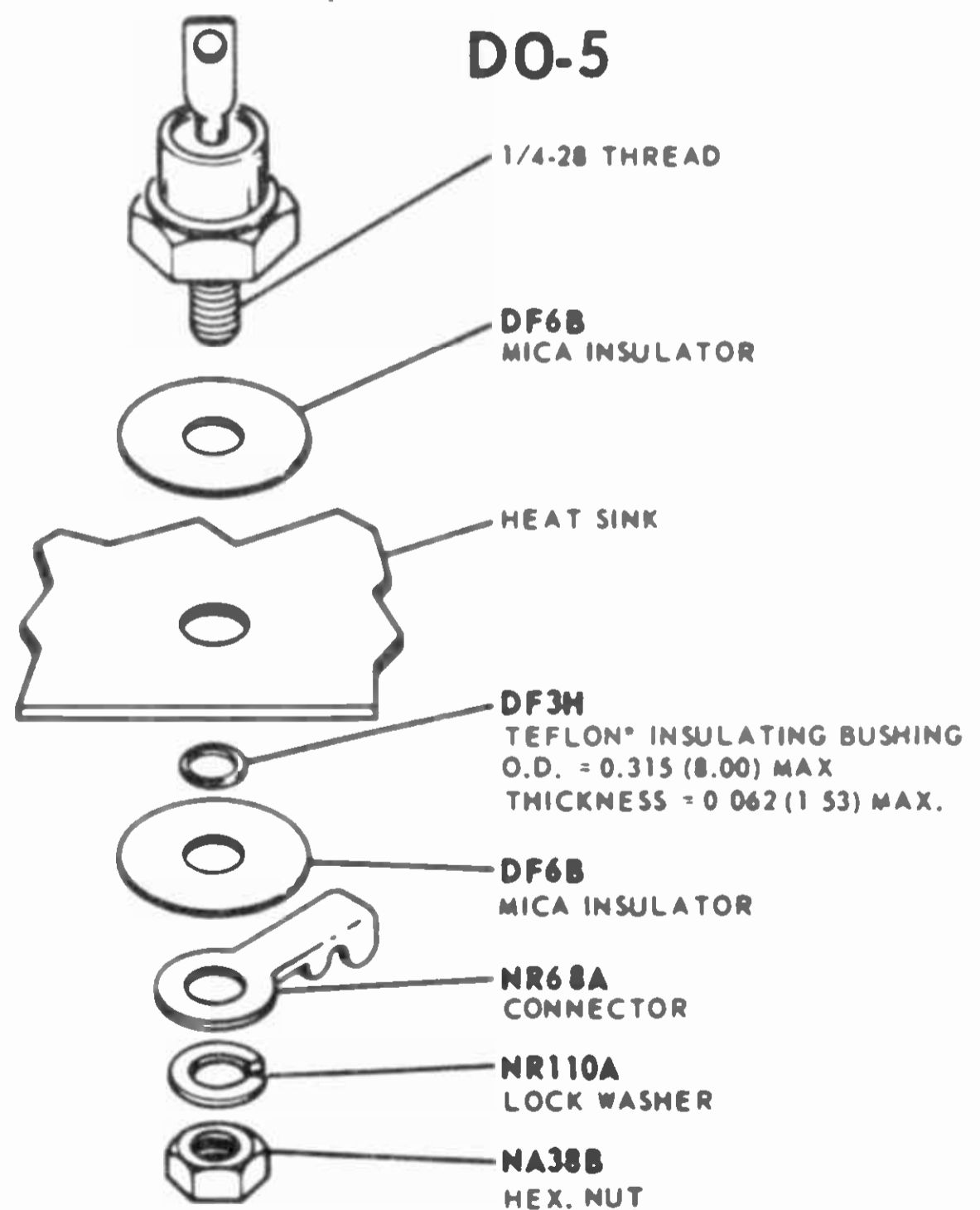
*REGISTERED TRADEMARK OF E.I. DUPONT DE NEMOURS & CO.

TO-48



*REGISTERED TRADEMARK OF E.I. DUPONT DE NEMOURS & CO.

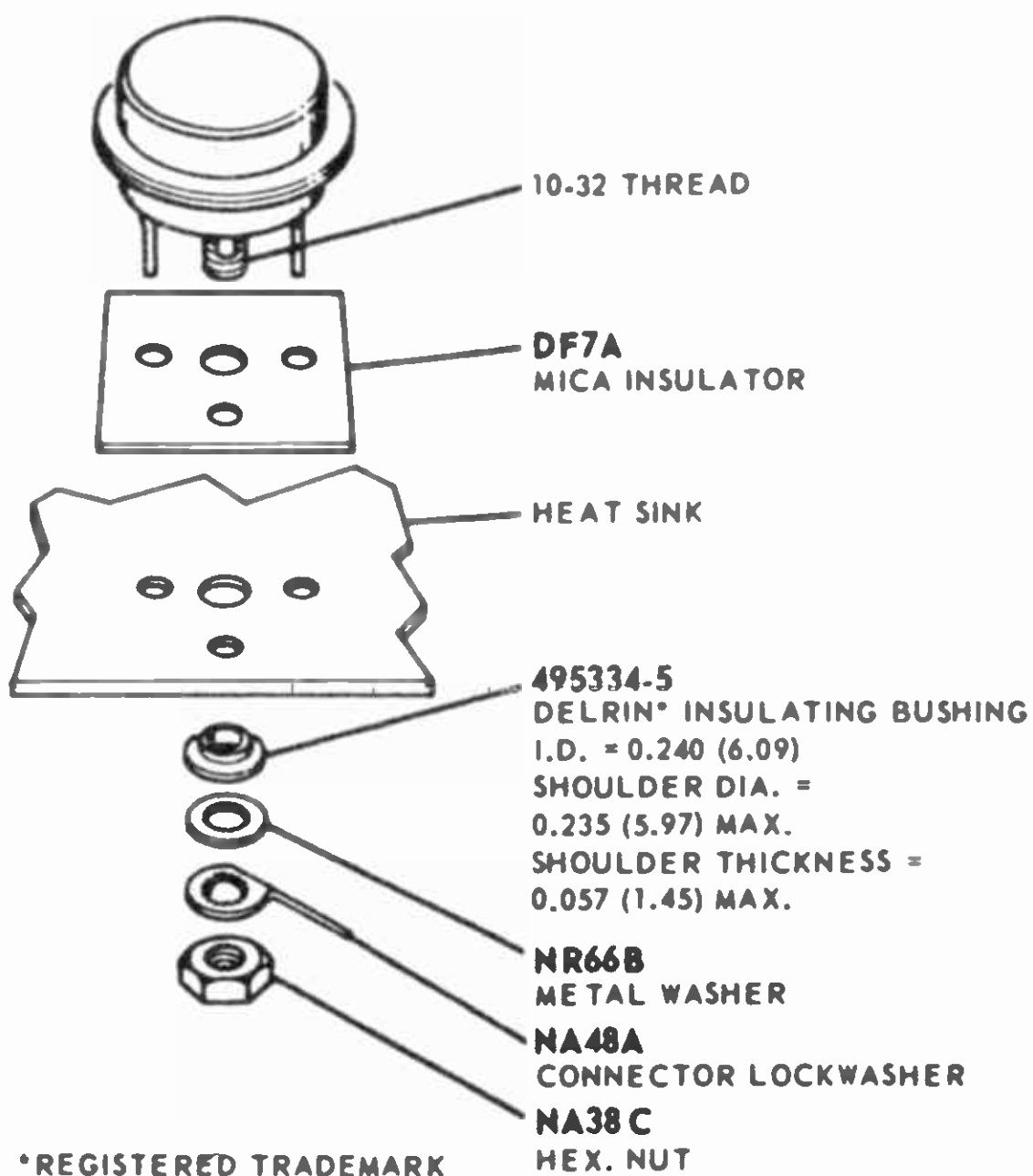
DO-5



*REGISTERED TRADEMARK OF E.I. DUPONT DE NEMOURS & CO.

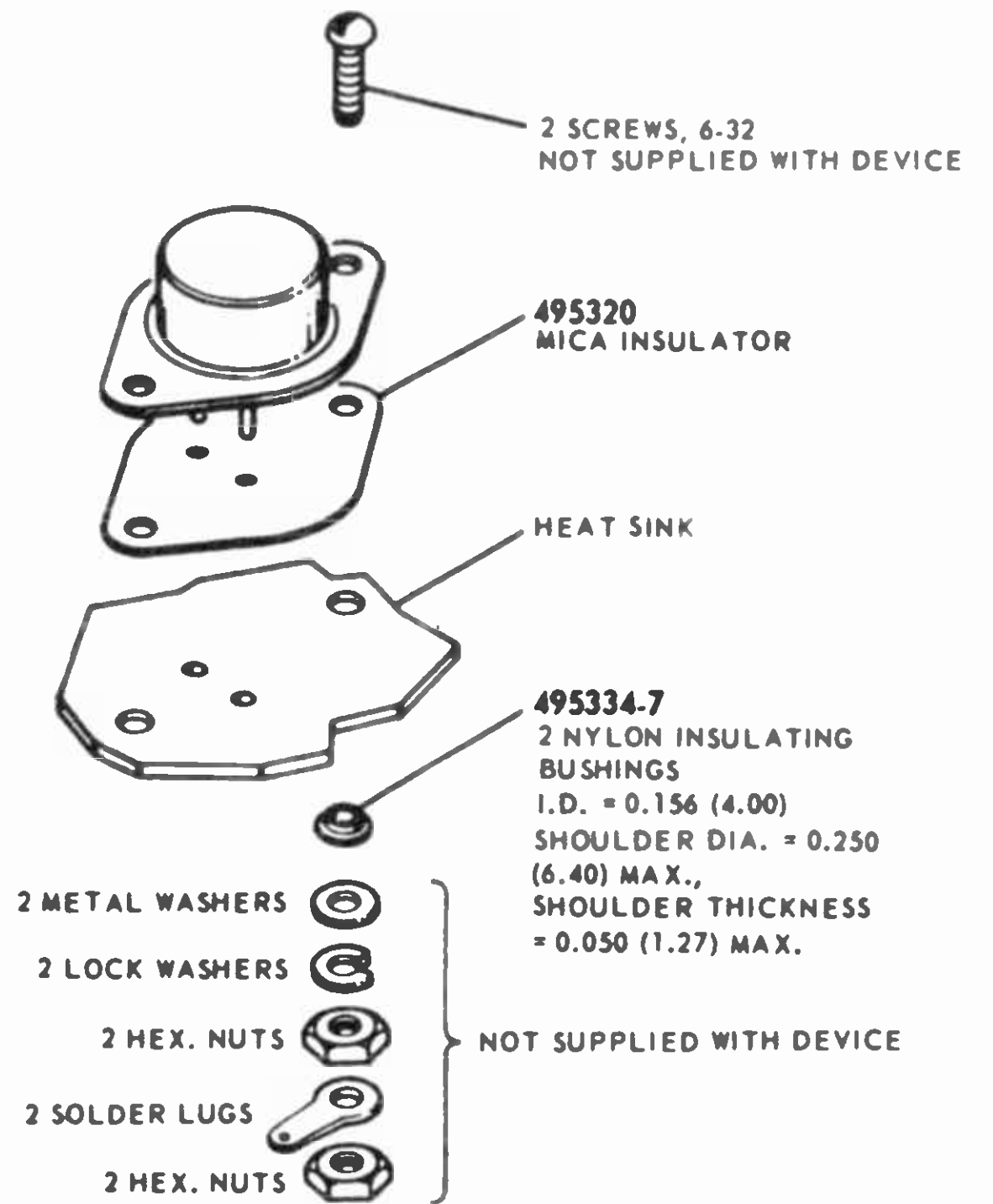
Mounting Hardware (cont'd)

TO-36

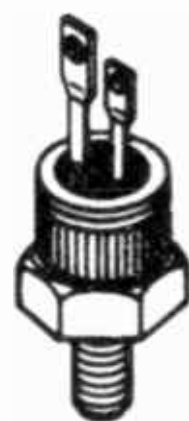


*REGISTERED TRADEMARK
OF E.I. DUPONT
DE NEMOURS & CO.

TO-3



FOR MOUNTING HARDWARE INSTRUCTIONS SEE DO-5



Circuits

THE CIRCUITS in this section illustrate some of the more important applications of RCA semiconductor devices; they are not necessarily examples of commercial practice. These circuits have been conservatively designed and are capable of excellent performance. The brief description provided with each circuit explains the functional relationships of the various stages and points out the intended applications, the major performance characteristics, and significant design features of the over-all circuit. Detailed descriptive information on individual circuit stages (such as detectors, amplifiers, or oscillators) is given earlier in this Manual, as well as in many textbooks on semiconductor circuits.

Electrical specifications are given for circuit components to assist those interested in home construction. Layouts and mechanical details are omitted because they vary widely with the requirements of individual set builders and with the sizes and shapes of the components employed.

Performance of these circuits depends as much on the quality of the components selected and the care employed in layout and construction as on the circuits themselves. Good signal reproduction from receivers and amplifiers requires the use of good-quality speakers, transformers, chokes and input sources (microphones, phonograph pickups, etc.).

Coils for the receiver circuits may be purchased at local parts dealers by specifying the characteristics required: for rf coils, the circuit posi-

tion (antenna or interstage), tuning range desired, and tuning capacitances employed; for if coils or transformers, the intermediate frequency, circuit position (1st if, 2nd if, etc.), and, in some cases, the associated transistor types; for oscillator coils, the receiver tuning range, intermediate frequency, type of converter transistor, and type of winding (tapped or transformer-coupled).

The voltage ratings specified for capacitors are the minimum dc working voltages required. Paper, mica, or ceramic capacitors having higher voltage ratings than those specified may be used except insofar as the physical sizes of such capacitors may affect equipment layout. However, if electrolytic capacitors having substantially higher voltage ratings than those specified are used, they may not "form" completely at the operating voltage, with the result that the effective capacitances of such units may be below their rated value. The wattage ratings specified for resistors assume methods of construction that provide adequate ventilation; compact installations having poor ventilation may require resistors of higher wattage ratings.

Circuits which work at very high frequencies or which are required to handle very wide bandwidths demand more than ordinary skill and experience in construction. Placement of component parts is quite critical and may require considerable experimentation. All rf leads to components including bypass capacitors must be kept short and must be properly dressed to mini-

mize undesirable coupling and capacitance effects. Correct circuit alignment and oscillator tracking may require the use of a cathode-ray oscilloscope, a high-impedance vacuum-tube voltmeter, and a signal generator capable of supplying a

properly modulated signal at the appropriate frequencies. Unless the builder has had considerable experience with broad-band, high-frequency circuits, he should not undertake the construction of such circuits.

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14-38	Light Dimmers	649

MANUFACTURERS OF SPECIAL COMPONENTS AND MATERIALS REFERRED TO IN PARTS LISTS

AirDux, trade name of
Icore Electro-Plastics, Inc.
Subsidiary of Icore Industries
1050 Kifer Road
Sunnyvale, Calif.

Alpha Wire Corporation
180 Varick Street
New York, N. Y.

Amphenol Connector Division
Amphenol-Borg Electronics Corp.
1830 South 54th Street
Chicago, Ill.

Arco Electronics, Inc.
Community Drive
Great Neck, N. Y.

Automatic Winding Division
General Instrument Co.
65 Gouverneur Street
Newark, N. J.

B and W, Inc.
Canal and Beaver Dam Road
Bristol, Pa.

Bud Radio, Inc.
4605 E. 355th Street
Willoughby, Ohio

Cambridge Thermionic Corp. (CTC)
445 Concord Avenue
Cambridge, Mass.

Centralab
Division of Globe Union, Inc.
P.O. Box 591
Milwaukee, Wisc.

Cutler-Hammer, Inc.
4201 North 27th Street
Milwaukee, Wisc.

Erie Technological Products, Inc.
644 West 12th Street
Erie, Pa.

Ferroxcube Corp. of America
Old Kings Highway
Saugerties, N. Y.

Freed Transformer Co.
1718 Weirfield Street
Brooklyn, N. Y.

General Ceramics Corp.
Crows Mill Road
Keasby, N. J.

Hammarlund Manufacturing Co.
Hammarlund Drive
Mars Hill, N. C.

Litz, trade name of
Alpha Wire Corp.
180 Varick Street
New York, N. Y.

Magnetic Metals Corp.
Hayes Avenue at 21st Street
Camden, N. J.

P. R. Mallory and Co., Inc.
3029 E. Washington Street
Indianapolis, Ind.

Mallory Controls Co.
Div. P. R. Mallory and Co., Inc.
Box 231
Frankfort, Ind

Micro Switch
Division of Honeywell, Inc.
Freeport, Ill.

Microtran Co., Inc.
145 East Mineola Avenue
Valley Stream, N. Y.

Mid-West Coil and Transformer Co.
1642 North Halstead
Chicago, Ill.

James Millen Manufacturing Co.
150 Exchange Street
Malden, Mass.

J. W. Miller Co.
5917 South Main Street
Los Angeles, Calif.

Potter and Brumfield
Division of American Machine
and Foundry Co.
1200 East Broadway
Princeton, Ind.

Radio Condenser Corp.
Division of TRW, Inc.
Davin and Copewood Street
Camden, N. J.

Simpson Electric Co.
5200 West Kinzie Street
Chicago, Ill.

MANUFACTURERS (cont'd)

F. W. Sickles Division
General Instrument Corp.
165 Front Street
Chicopee, Mass.

Sprague Electric Co.
481 Marshall St.
North Adams, Mass.

Stancor (Chicago-Stancor)
3501 West Addison Street
Chicago, Ill.

Thordarson-Meissner
7th and Belmont
Mt. Carmel, Ill.

NOTES: Components and materials identified by RCA stock numbers may be obtained through authorized RCA distributors. In general, all components specified in the circuit parts lists can be purchased from local radio and electronic supply stores or mail-order houses. If the parts are not available from these sources, they may be obtained from the pertinent manufacturers listed above.

Triad
305 North Briant Street
Huntington, Ind.

Triwec Transformer Co.
3261 Milwaukee Avenue
Chicago, Ill.

Vibroplex Co., Inc.
833 Broadway
New York, N. Y.

Vitramon, Inc.
Box 544
Bridgeport, Conn.

Wakefield Engineering, Inc.
139 Foundry Street
Wakefield, Mass.

14-1 12-VOLT AUTOMOBILE RADIO RECEIVER**Circuit Description**

This 5-transistor superheterodyne radio receiver operates from the storage battery in automobiles that employ a 12-volt ignition system. The rf amplifier uses a high-gain 2N1637 transistor to provide the increased sensitivity and higher signal-to-noise ratio required in automobile radio receivers. The tuned rf amplifier selects and amplifies the amplitude-modulated rf signals from the desired broadcast station picked up by the automobile whip antenna. In the 2N1639 converter stage, the amplitude-modulated rf signal from the rf amplifier is mixed with a local-oscillator signal developed by the tuned circuit consisting of oscillator coil L_1 and capacitors C_{11} and C_{12} to provide a signal at the receiver intermediate frequency of 262.5 kHz (this value, rather than 455 kHz, is used in auto radios because the if amplifier provides greater gain and selectivity at the lower frequency).

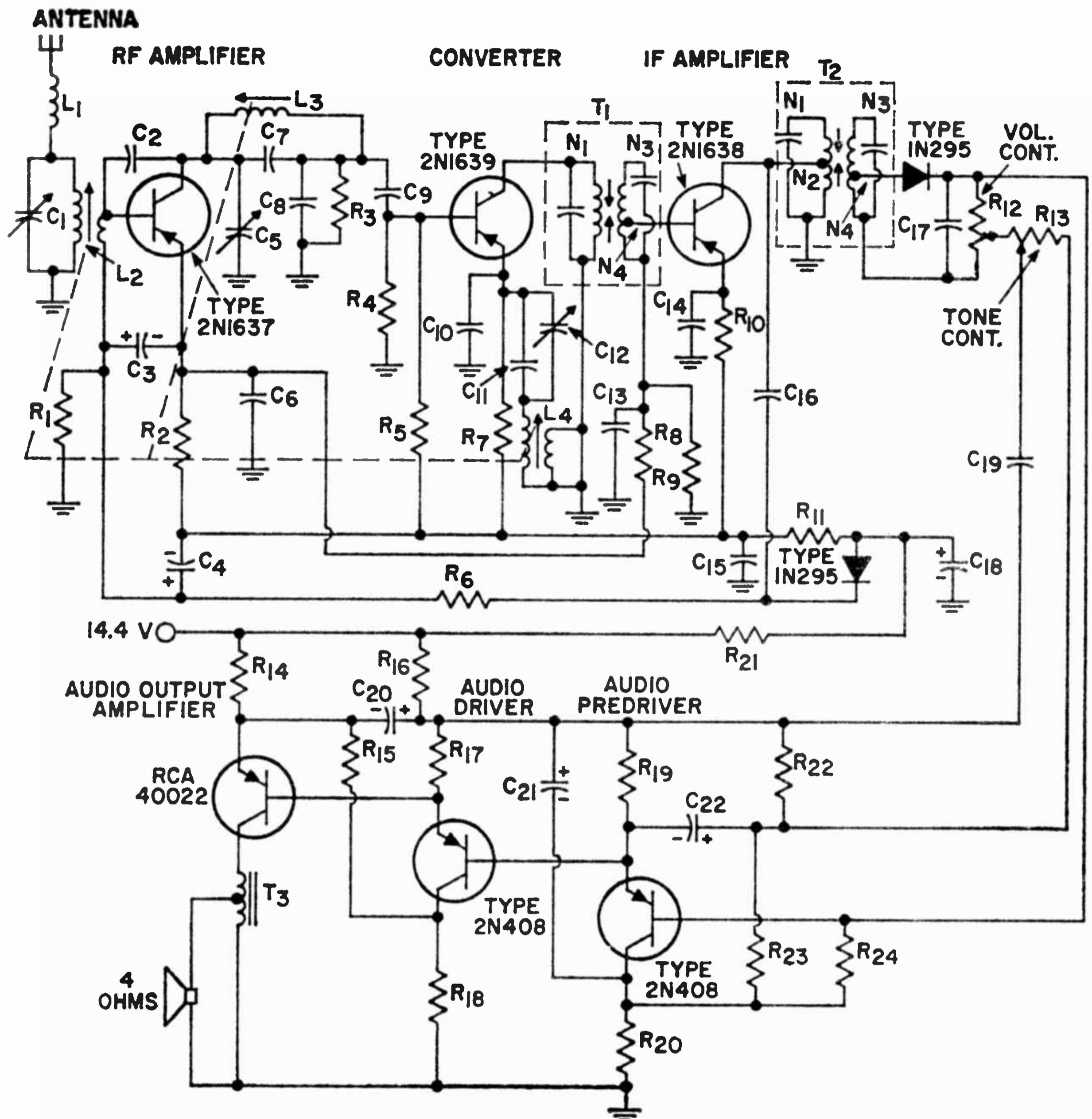
The antenna circuit, rf amplifier, and converter are tuned together by means of mechanically ganged variable inductors L_2 , L_3 , and L_4 so that the local-oscillator frequency is always 262.5 kHz above the frequency

to which the other circuits are tuned. Trimmer capacitors C_1 , C_5 , and C_{12} are adjusted to provide the proper tracking relationship.

The 262.5-kHz signal from the converter stage is amplified by a single 2N1638 if amplifier and is then demodulated in the 1N295 second-detector circuit. The audio signal from the detector, which is developed across the volume-control potentiometer R_{12} , is coupled through the tone-control potentiometer R_{13} to the audio-amplifier section of the receiver. In this section, the audio signal is amplified by two 2N408 voltage amplifiers (audio predriver and driver stages) and applied to the base circuit of the 40022 power amplifier stage which drives the speaker.

A portion of the audio-frequency signal from the detector is coupled from the wiper arm of the tone control through a frequency-selective network to the audio amplifiers. The tone-control network by de-emphasis of low frequencies tends to equalize the amplitudes of low- and high-frequency audio signals.

14-1 12-VOLT AUTOMOBILE RADIO RECEIVER (cont'd)



NOTE: This circuit uses coils and transformers that are not available as stock items from any manufacturer. Home construction of this circuit should not be attempted unless the builder has had considerable experience in the winding of inductive components and has access to the special equipment required. The builder should also refer to the general considerations for construction of high-frequency and broadband circuits given on page 582.

Parts List

C₁ = trimmer capacitor, 5 to 80 pF, Arco No. 462 or equiv.
 C₂ = 2 pF, silver mica
 C₃ = 2.2 μ F, electrolytic, 3 V
 C₄ = 25 μ F, electrolytic, 6 V
 C₅, C₁₂ = trimmer capacitor, 110 to 580 pF, Arco No. 467 or equiv.
 C₆, C₉, C₁₃, C₁₄, C₁₅, C₁₉ = 0.05 μ F ceramic disc
 C₇ = 200 pF, silver mica
 C₈ = 0.005 μ F, ceramic disc

C₁₀ = 0.0075 μ F, ceramic disc
 C₁₁ = 330 pF, silver mica
 C₁₆ = 180 pF, silver mica
 C₁₇ = 0.02 μ F, ceramic disc
 C₁₈ = 100 μ F, electrolytic, 15 V
 C₂₀ = 500 μ F, electrolytic, 3 V
 C₂₁ = 50 μ F, electrolytic, 6 V
 C₂₂ = 100 μ F, electrolytic, 3 V
 L₁ = rf choke, 5 μ H
 L₂, L₃, L₄ = ganged tuning-

coil assembly; manufactured by F. W. Sickles Co. and Radio Condenser Corp.

L₂ = antenna coil; primary = variable inductor, tunes with 110-pF capacitance from 535 to 1610 kHz, Q = 65 at 1610 kHz; secondary = 3½ turns
 L₃ = rf coil, variable inductor, tunes with 600-pF capacitance from 535 to 1610 kHz, Q = 65 at 1610 kHz

14-1 12-VOLT AUTOMOBILE RADIO RECEIVER (cont'd)

Parts List (cont'd)

L_1 = oscillator coil; primary = variable inductor, tunes with 470-pF capacitance from 797.5 to 1872.5 kHz, $Q = 65$ at 1872.5 kHz; secondary = 30 turns	tiometer, 1000 ohms, 0.5 watt, audio taper	ance = 68200 ohms; turns ratio of tapped secondary, $N_3/N_1 = 18.25$
R_1 = 82000 ohms, 0.5 watt	R_{14} = 3.3 ohms, 1 watt	T_2 = second if (262.5-kHz) transformer (includes 110-pF capacitor across each winding); primary unloaded $Q = 47$, primary loaded $Q = 33.8$; secondary unloaded $Q = 47$, secondary loaded $Q = 23.5$; turns ratio of tapped primary, $N_1/N_2 = 4.28$; turns ratio of tapped secondary $N_3/N_1 = 10.2$; input impedance = 0.85
R_2 = 560 ohms, 0.5 watt	R_{15} = 82 ohms, 0.5 watt	T_3 = output transformer; transforms 22 ohms at 425 mA dc to 3.5 ohms; Thordarson-Meissner No. TR-168, or equiv.
R_3 = 180 ohms, 0.5 watt	R_{16} = 68 ohms, 0.5 watt	
R_4 = 56000 ohms, 0.5 watt	R_{17} = 120 ohms, 0.5 watt	
R_5 = 5700 ohms, 0.5 watt	R_{18} = 220 ohms, 0.5 watt	
R_6 = 8200 ohms, 0.5 watt	R_{19} = 1200 ohms, 0.5 watt	
R_7 = 1500 ohms, 0.5 watt	R_{20} = 4700 ohms, 0.5 watt	
R_8 = 5600 ohms, 0.5 watt	R_{21} = 680 ohms, 0.5 watt	
R_9 = 0.1 megohm, 0.5 watt	R_{22}, R_{24} = 3300 ohms, 0.5 watt	
R_{10} = 470 ohms, 0.5 watt	R_{23} = 33000 ohms, 0.5 watt	
R_{11} = 100 ohms, 0.5 watt	T_1 = first if (262.5-kHz) transformer (includes 220-pF capacitor across each winding); primary unloaded $Q = 47$, primary loaded $Q = 40.56$; secondary unloaded $Q = 47$; secondary loaded $Q = 39.4$; input imped-	
R_{12} = volume control, potentiometer, 2500 ohms, 0.5 watt, audio taper		
R_{13} = tone control, poten-		

14-2 ALL-AMERICAN-FIVE AC/DC RADIO RECEIVER

Circuit Description

This five-transistor radio receiver operates directly from either an ac power line or a dc supply of 117 volts. AC power inputs are converted to dc power by the 40495 half-wave rectifier circuit. This receiver is comparable in both performance and cost with a typical five-tube broadcast receiver of the type commonly referred to as the "All America Five." Previous five-transistor receivers have matched the performance of five-tube receivers except with respect to overload capability. Limitations on the allowable voltage swing at the base of transistors impose a restriction not normally encountered with vacuum tubes and have usually required the use of an overload diode.

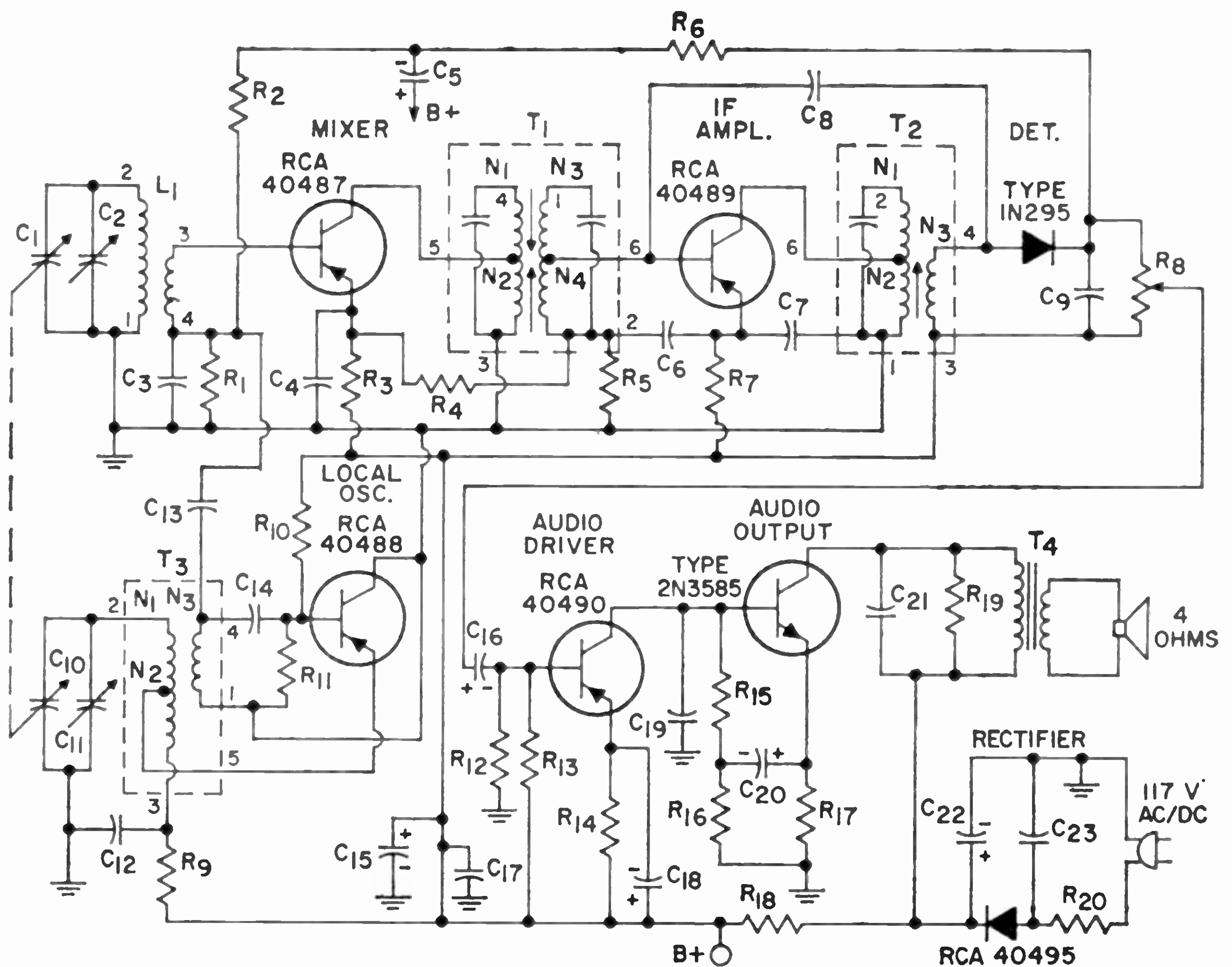
The receiver uses separate mixer and oscillator stages with one if-amplifier stage, rather than the more conventional complement of a converter stage with two if-amplifier stages, to permit application of agc voltage at a point where signal voltages are low, i.e., at the base of the mixer stage. This technique results in good overload performance without need for an overload diode. The use of a separate grounded-collector

oscillator stage also provides excellent frequency stability throughout the agc range.

The mixer stage uses a 40487 germanium transistor that has a collector idling current of 1.4 milliamperes. The oscillator signal is injected to the base of the mixer transistor by the local oscillator stage which uses a 40488 transistor. The secondary winding of the antenna coil L_1 is designed to keep signal voltages as low as possible on the base of the mixer. Under maximum agc conditions, the operating current of the mixer transistor is reduced to approximately 20 microamperes. Optimum mixer gain is obtained when the oscillator signal is injected at a level of 120 millivolts. The mixer-oscillator approach also provides low noise and excellent oscillator stability (0.018 kHz per volt per meter of input signal and 0.085 kHz per volt of supply-voltage variation).

The if-amplifier stage employs a neutralized 40489 transistor that provides power gain of 41 dB within the limits of unconditional stability. The operating point of this stage is set at 18 volts and 2.5 milliamperes

14-2 ALL-AMERICAN-FIVE AC/DC RADIO RECEIVER (cont'd)



NOTE: This circuit uses coils and transformers that are not available as stock items from any manufacturer. Home construction of this circuit should not be attempted unless the builder has had considerable experience in the winding of inductive components and has access to the special equipment required. The builder should also refer to the general considerations for construction of high-frequency and broadband circuits given on page 582.

Parts List

C_1, C_2, C_{10}, C_{11} = ganged tuning capacitor; antenna section ($C_1 + C_2$), 10 to 228 pF; oscillator section ($C_{10} + C_{11}$), 9 to 118 pF
 C_3 = 0.005 μ F, ceramic disc
 $C_4, C_6, C_7, C_{12}, C_{17}$ = 0.05 μ F, ceramic disc
 C_5 = 10 μ F, electrolytic, 3 V
 C_8 = 6.8 pF, NPO ceramic
 C_9 = 0.02 μ F, ceramic disc
 C_{13} = 0.001 μ F, ceramic disc
 C_{14} = 200 pF, ceramic disc
 C_{15} = 100 μ F, electrolytic, 25 V
 C_{16} = 10 μ F, electrolytic, 12 V
 C_{18} = 100 μ F, electrolytic, 10 V
 C_{19} = 0.047 μ F, ceramic disc
 C_{20} = 10 μ F, electrolytic, 10 V
 C_{21}, C_{23} = 0.01 μ F, ceramic disc, 300 V
 C_{22} = 100 μ F, electrolytic, 150 V

L_1 = antenna coil; core material, Ferramic Q or equiv.; primary, 120 turns of No. 32 wire wound 43 turns per inch; secondary, 5 turns of No. 34 wire; output impedance, 260 ohms at 1500 kHz; primary inductance, 0.413 μ H at 790 kHz; unloaded Q, 125 at 600 kHz and 130 at 1400 kHz
 R_1 = 0.27 megohm, 0.5 watt
 R_2 = 1000 ohms, 0.5 watt
 R_3 = 0.82 megohm, 0.5 watt
 R_4 = 2200 ohms, 0.5 watt
 R_5 = 82000 ohms, 0.5 watt
 R_6 = 18000 ohms, 0.5 watt
 R_7 = 680 ohms, 0.5 watt
 R_8 = Volume control, potentiometer, 2500 ohms, 0.5 watt, audio taper
 R_9, R_{11} = 6800 ohms, 0.5 watt
 R_{10}, R_{12} = 22000 ohms, 0.5 watt
 R_{13} = 4700 ohms, 0.5 watt

R_{14} = 560 ohms, 0.5 watt
 R_{15} = 1500 ohms, 0.5 watt
 R_{16} = 180 ohms, 0.5 watt
 R_{17} = 270 ohms, 0.5 watt
 R_{18} = 5600 ohms, 0.5 watt
 R_{19} = 10000 ohms, 0.5 watt
 R_{20} = 250 ohms, 0.5 watt
 T_1 = first if (455-kHz) transformer (includes 110-pF capacitors across primary and secondary windings); turns ratio of tapped primary, $N_1/N_2 = 3.16$; turns ratio of tapped secondary, $N_3/N_1 = 33.4$; primary unloaded Q = 80, primary loaded Q = 75.68; secondary unloaded Q = 80; secondary loaded Q = 64; input impedance = 14550 ohms; coefficient of coupling = 0.85
 T_2 = second if (455-kHz) transformer (includes 110-pF capacitor across primary winding);

14-2 ALL-AMERICAN-FIVE AC/DC RADIO RECEIVER (cont'd)

Parts List (cont'd)

turns ratio of tapped primary, $N_1/N_2 = 2.57$;	ohms	pF capacitance at 990 kHz
turns ratio of lower section of primary to secondary, $N_2/N_3 = 3.36$;	$T_3 =$ oscillator coil; turns ratio of full primary to section of primary below tap, $N_1/N_2 = 26$;	$T_4 =$ audio output transformer; primary impedance, 2500 ohms; secondary impedance, 3.2 ohms;
unloaded $Q = 80$;	ratio of full primary to secondary, $N_1/N_3 = 9.6$;	Triad No. S-12X, or equiv.
loaded $Q = 35.2$; input impedance = 18000	full primary tunes with 100-	

Circuit Description (cont'd)

for optimum dynamic range and improved large-signal-handling capability. The oscillator transistor also receives partial gain control under very strong signal conditions. Selectivity is determined by the double-tuned input transformer T_1 and the single-tuned output transformer T_2 . The if transformers have equal unloaded Q and equal tuning capacitance for economy and ease of production. The receiver is designed for transistor interchangeability, and over-all gain variations are minimal.

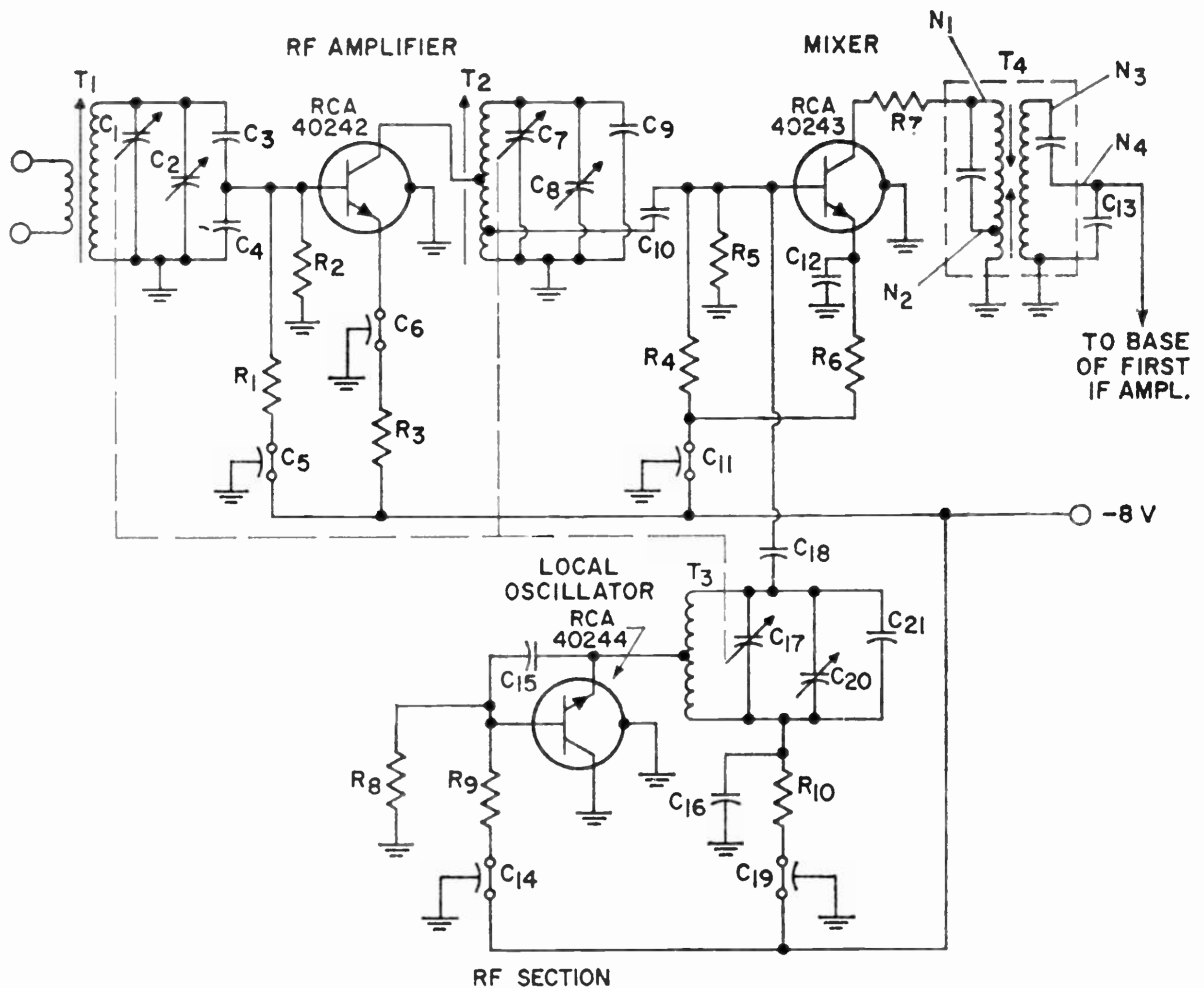
The 40490 driver transistor and 2N3585 output transistor used in the two-stage audio amplifier section develop a power gain of 75 dB and deliver an output of one watt to a 3-ohm load with distortion of less than 10 per cent. The 2N3585 output

transistor is designed to operate from the ac power line with no protective devices. High-voltage transients may be developed when the output transistor is overdriven to high values of collector current and is then abruptly cut off. Protection from such transients is provided by use of an unbypassed 270-ohm resistor in the emitter circuit of the output stage to limit the base current of the output unit to a safe maximum value. The voltage developed across the resistor (R_{17}) at the maximum safe value of collector current is designed to equal the maximum voltage on the base. As a result, the output current is clamped to a value equal to this voltage divided by the emitter resistance.

Performance Characteristics

Frequency	600	1000	1400	kHz
50-mW Sensitivity	175	130	100	$\mu\text{V}/\text{m}$
(S + N)/N at Sensitivity	21	21	20	dB
AGC Figure of Merit	27.4	29.4	30	dB
(50,000 $\mu\text{V}/\text{m}$ reference)				
Image Rejection	—	—	48	dB
IF Rejection	40	—	—	dB
Adjacent-Channel Attenuation	32	24	23	dB
(1000 $\mu\text{V}/\text{m}$ level)				
6-dB Bandwidth	5.1	8.3	8.5	kHz
20-dB Bandwidth	13.8	16.5	20.2	kHz
60-dB Bandwidth	52	62	70	kHz
RF Overload:				
at 30% Modulation	—	2	—	V/m
at 80% Modulation	—	0.9	—	V/m

14-3 HIGH-QUALITY FM TUNER FOR MULTIPLEX RECEIVER



NOTE: This circuit uses coils and transformers that are not available as stock items from any manufacturer. Home construction of this circuit should not be attempted unless the builder has had considerable experience in the winding of inductive components and has access to the special equipment required. The builder should also refer to the general considerations for construction of high-frequency and broadband circuits given on page 582.

Parts List for RF Section

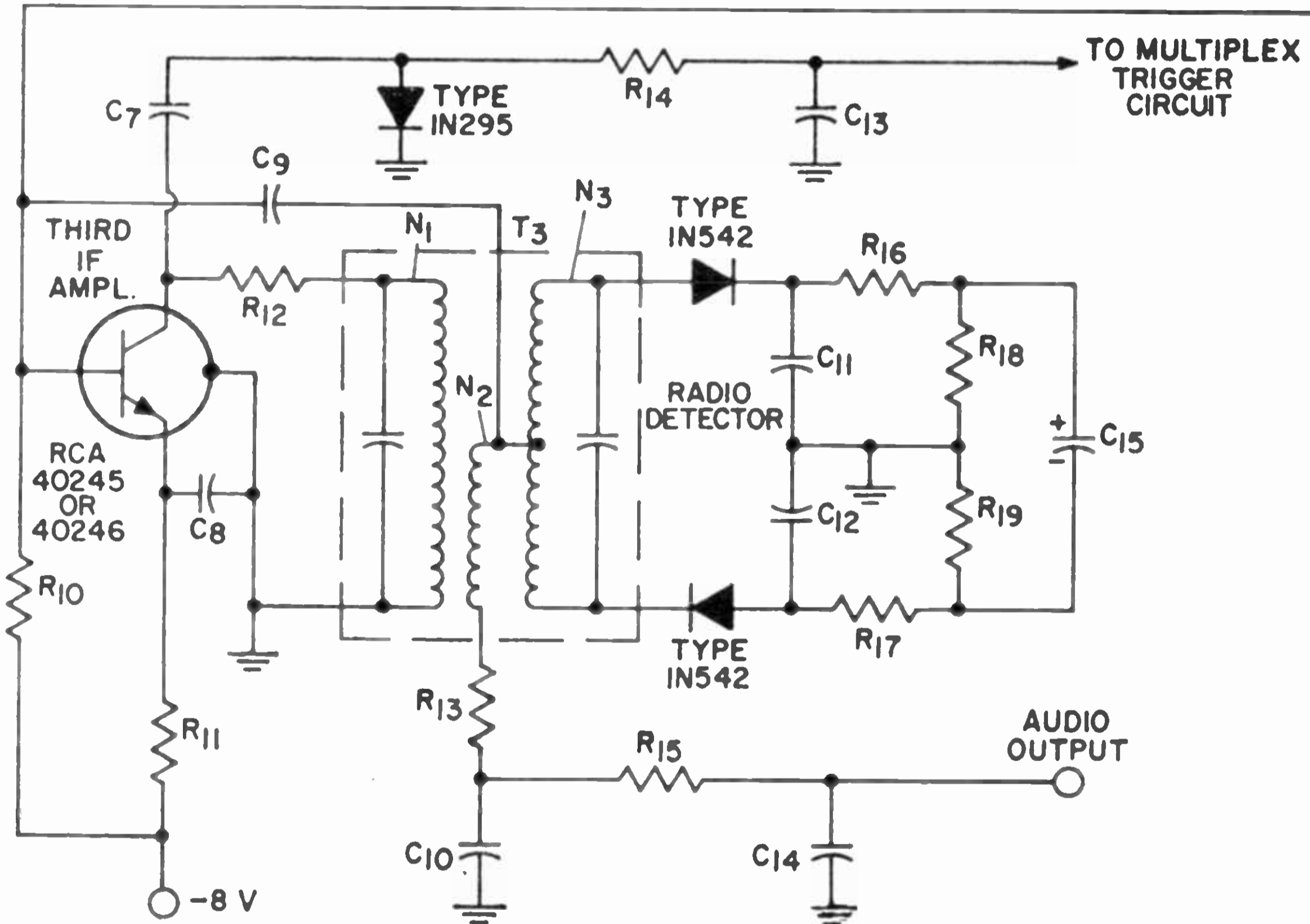
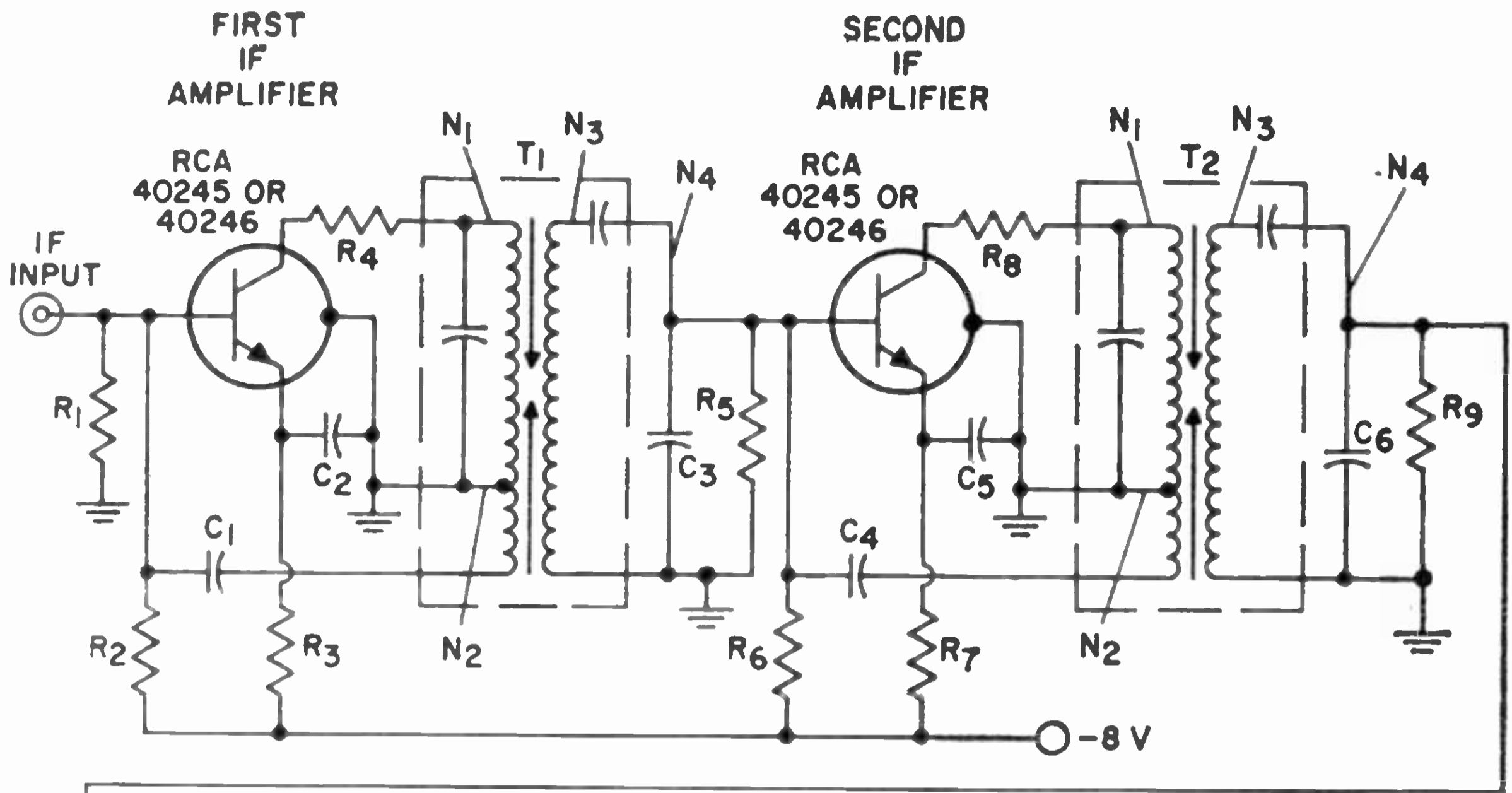
C_1, C_7, C_{17} = ganged tuning capacitors, C_1, C_7 = 7.25 to 19 pF; C_{17} = 6 to 21 pF
 C_2, C_8 = trimmer capacitor (part of ganged tuning capacitor assembly), approximately 17 pF maximum.
 C_3, C_9 = 5.6 pF, miniature ceramic
 C_4 = 27 pF, ceramic disc
 $C_5, C_6, C_{11}, C_{11}, C_{19}$ = feed-through capacitor, 1000 pF
 C_{10} = 2000 pF, ceramic disc, 1000 V
 C_{12} = 0.01 μ F, ceramic disc
 C_{13}, C_{16} = 1000 pF, ceramic disc, 1000 V
 C_{15} = 3.3 pF, NPO ceramic
 C_{18} = 0.22 pF to 3.3 pF (value determines oscillator injection voltage and is dependent upon factors such as circuit layout and placement of components)

C_{20} = tubular trimmer capacitor, 1.5 to 10 pF
 C_{21} = 12 pF, ceramic disc
 R_1, R_1 = 3300 ohms, 0.5 watt
 R_2, R_5 = 18000 ohms, 0.5 watt
 R_3, R_6 = 330 ohms, 0.5 watt
 R_7 = 100 ohms, 0.5 watt
 R_8 = 8200 ohms, 0.5 watt
 R_9 = 4700 ohms, 0.5 watt
 R_{10} = 1500 ohms, 0.5 watt
 T_1 = FM antenna transformer; slug-tuned; slug, 0.250 inch long, 0.181 inch in diameter, Arnold Type 1RN9 or equiv.; secondary, 4 turns of No. 22 bare-tinned copper wire wound with 1 wire-diameter spacing between adjacent turns or 7/32-inch outer-diameter coil form, resonates with 27-pF capacitance at 100 MHz, impedance = 6100 ohms; primary, 2 turns of No.

30 Gripeze wire close wound below cold end of secondary and in same direction, impedance (includes shunting effect of rf amplifier biasing network) = 460 ohms.
 T_2 = rf interstage coil; 4 turns of No. 18 bare-tinned copper wire wound with approximately $\frac{1}{8}$ -inch spacing between turns on 5/16-inch diameter coil form (coil form is removed after coil is wound); resonates with 27-pF capacitance at 100 MHz; impedance of full winding, 6100 ohms; input tap located so that impedance at tap = 590 ohms; output tap located so that impedance at input tap is 540 ohms with the transformer properly loaded.

14-3

HIGH-QUALITY FM TUNER (cont'd)



IF SECTION

NOTE: Type 1N542 diodes are a matched pair.

Parts List for RF Section (cont'd)

T_3 = oscillator coil; $3\frac{1}{2}$ turns of No. 18 bare-tinned copper wire wound with $\frac{3}{32}$ -inch spacing between turns on $\frac{7}{32}$ -inch-diameter coil form (coil form is removed after coil is wound), center tapped.
 T_1 = first if (10.7-MHz) transformer, primary unloaded $Q = 60$, primary loaded $Q = 60$, ratio of

full secondary to section below tap (N_1/N_2) = 7.27, secondary unloaded $Q = 62.3$, secondary loaded $Q = 60$, ratio of full secondary to section that corresponds to lower tuning capacitor (N_3/N_1 , as determined by tapped capacitors) = 26.65, output impedance = 6070 ohms, per cent of critical coupling = 90

Parts List for IF Section

C_1, C_1 = 4.7 pF, ceramic disc
 C_2, C_3, C_8 = 0.01 μ F, ceramic disc
 C_3, C_6 = 1000 pF, ceramic disc, 1000 V
 C_7 = 5 pF, ceramic disc
 C_9 = 1.0 pF, ceramic disc
 C_{10}, C_{11}, C_{12} = 330 pF, ceramic
 C_{13} = 0.05 μ F, ceramic disc
 C_{14} = 0.02 μ F, ceramic disc

14-3

HIGH-QUALITY FM TUNER (cont'd)

Parts List for IF Section (cont'd)

$C_{15} = 5 \mu\text{F}$, electrolytic, 10 V.	7.27, secondary unloaded $Q = 62.3$, secondary loaded $Q = 60$, ratio of full secondary to section that corresponds to lower tuning capacitor (N_3/N_4 , as determined by tapped capacitors) = 26.65, output impedance = 6070 ohms, per cent of critical coupling = 90	lower tuning capacitor (N_3/N_4 , as determined by tapped capacitors) = 27.5 output impedance = 6070 ohms, per cent of critical coupling = 90
$R_1, R_5, R_9 = 12000$ ohms, 0.5 watt		$T_3 =$ ratio-detector transformer, primary unloaded Q (with tertiary winding N_2 returned to ground through a 68-ohm resistance) = 65, primary loaded $Q = 28.5$, primary-to-tertiary turns ratio (N_1/N_2) = 2.5, secondary unloaded $Q = 65$, secondary loaded $Q = 24.75$, output impedance = 6070 ohms, per cent of critical coupling = 90
$R_2, R_6, R_{10} = 2700$ ohms, 0.5 watt		
$R_3, R_4, R_7, R_8, R_{11} = 220$ ohms, 0.5 watt		
$R_{12} = 470$ ohms, 0.5 watt		
$R_{13} = 68$ ohms, 0.5 watt		
$R_{14} = 22000$ ohms, 0.5 watt		
$R_{15} = 3900$ ohms, 0.5 watt		
$R_{16} = 1000$ ohms, 0.5 watt		
$R_{17} = 1500$ ohms, 0.5 watt		
$R_{18}, R_{19} = 6800$ ohms, 0.5 watt		
$T_1 =$ second if (10.7-MHz) transformer, primary unloaded $Q = 72.4$, primary loaded $Q = 60$, ratio of full primary to section below tap (N_1/N_2) =	$T_2 =$ third if (10.7-MHz) transformer, primary unloaded $Q = 49.7$, primary loaded $Q = 41.2$, ratio of full primary to section below tap (N_1/N_2) = 7.27, secondary unloaded $Q = 64.2$, secondary loaded $Q = 61.85$, ratio of full secondary to section that corresponds to	

Circuit Description

This high-quality FM tuner uses silicon n-p-n transistors that provide good receiver quieting and limiting performance because of their high usable gains and low noise levels (typical device noise is 3 dB at 100 MHz for a 300-ohm source impedance). These transistors provide excellent amplification in the FM band and are capable of sustained oscillation at frequencies up to 1100 MHz.

RF section—The rf-amplifier stage uses a 40242 transistor in a common-emitter circuit configuration to obtain the highest stable gain over the entire FM broadcast frequency range. This stage can provide an unneutralized gain of 15.4 dB. The operating point of the stage is chosen so that agc can be applied effectively.

The 40243 mixer transistor is also operated in a common-emitter configuration. An oscillator-signal injection voltage of approximately 90 millivolts is coupled across capacitor C_{18} to the base of the mixer transistor from the oscillator resonant circuit C_{17}, C_{20}, C_{21} and T_1 . The 40244 oscillator stage is adjusted to provide a uniform injection voltage to the base of the mixer transistor over the entire FM oscillator-frequency range.

IF section—The three stage if-amplifier strip uses three 40245 or 40246 transistors in a common-emitter circuit configuration to provide 23.4 dB of stable gain per stage. The three double-tuned if transformers T_1, T_2 , and T_3 provide a 6-dB bandwidth of 300 kHz, which is adequate for reproduction of stereo signals.

The 1N295 diode and associated components in the collector circuit of the third if amplifier develops a negative voltage proportional to the rf input signal. This voltage is used to drive a schmitt trigger stage associated with the noise immunity circuit of the FM stereo demodulator (refer to discussion of the demodulator, circuit 13-5). If desired, the negative voltage may also be applied to the base of the 40242 transistor in the rf amplifier as agc bias. As a result, the final 40246 if-amplifier transistor can go into full limiting before appreciable agc is developed. This arrangement provides a relatively wide agc bandwidth which is helpful in tuning to strong signals.

FM detection is accomplished by the ratio-detector circuit, which includes a matched pair of IN542 diodes and associated components. The detector transformer T_3 is designed

14-3 HIGH-QUALITY FM TUNER (cont'd)

Circuit Description (cont'd)

to provide the wide peak-to-peak separation (450 kHz) required for good stereo multiplex operation. R_{15} and C_{14} in the output circuit of the

ratio detector form a standard FM de-emphasis network for high audio frequencies.

14-4 FM TUNER USING AN MOS-TRANSISTOR RF AMPLIFIER

Circuit Description

This FM tuner uses a 40468 MOS transistor in the rf-amplifier stage and 40479 and 40244 bipolar transistors in the mixer and local-oscillator stages, respectively, to achieve an over-all front-end-section gain of 34.5 dB. The if section and the ratio detector are identical to those used in the **High Quality FM Tuner** shown as circuit 14-3. The tuner operates from a dc supply of -15 volts.

The rf amplifier in the tuner is designed to minimize the spurious responses normally found in FM receivers as a result of mixing of the harmonics of unwanted incoming signals with harmonics of the local-oscillator signal to produce difference frequencies within the if pass band. This objective necessitated some compromise between optimum receiver sensitivity and spurious-response rejection in the selection of the source and load impedance for the rf amplifier.

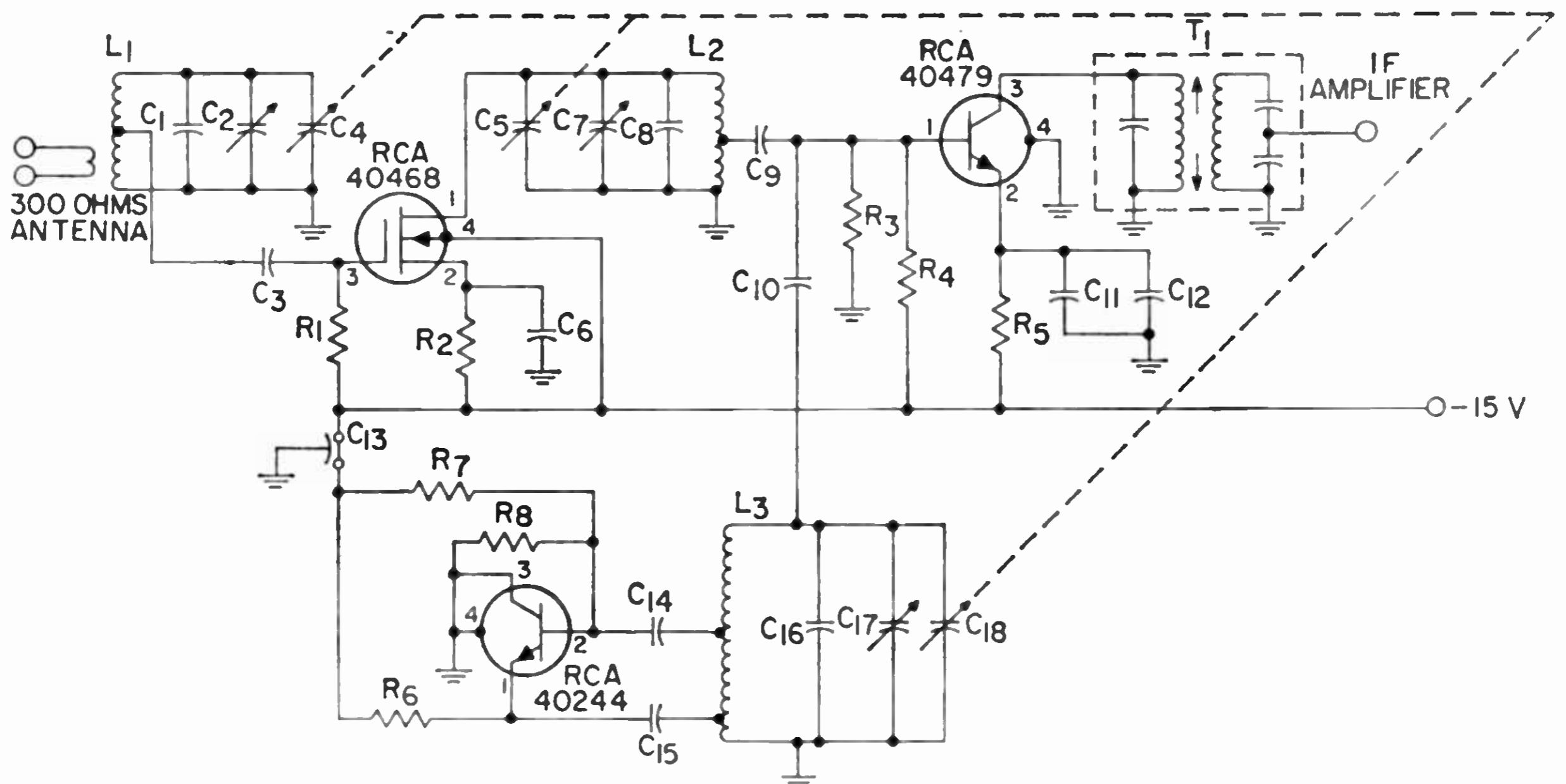
Achievement of minimum spurious responses requires that the gate input to the 40468 rf-amplifier be obtained from a tap as far down on the antenna coil (L_1) as gain and noise considerations permit. This arrangement assures the smallest practical input voltage swing to the gate and, therefore, makes possible optimum use of the available dynamic range of the MOS transistor. In addition, the low spurious-response objective requires that the entire rf interstage coil (L_2) be used as the load for the 40468 MOS transistor.

This coil, selected on the basis of the optimum compromise between gain and bandwidth requirements, provides a load impedance to the rf amplifier of 3800 ohms, which presents a slight mismatch to the 4200-ohm output impedance of the 40468 MOS transistor. Although the compromises in the input and output circuits of the rf amplifier result in a slight loading of the interstage coil L_2 and cause some degradation in the selectivity of the front end, these undesirable effects can be tolerated because the antenna coil is not loaded by the gate of the MOS transistor. The effectiveness of these compromises is demonstrated by the excellent spurious-response rejection (more than 100 dB) provided by the FM tuner.

The 40648 MOS transistor used in the rf amplifier has a maximum available gain of 24 dB. The compromises in circuit design between optimum receiver sensitivity and spurious-response rejection, however, result in a total mismatch and insertion loss of 11.3 dB. The actual net gain of the rf amplifier, therefore, is 12.7 dB. This stage amplifies the frequency-modulated rf signal coupled from a 300-ohm FM antenna by the antenna coil L_1 and applies this amplified signal to the base of the mixer transistor.

The 40479 bipolar transistor used in the mixer stage is operated in a common-emitter circuit configuration that provides a conversion power gain of 21.8 dB. Both the frequency-

14-4

FM TUNER USING AN MOS-TRANSISTOR
RF AMPLIFIER (cont'd)

NOTE: This circuit uses coils and transformers that are not available as stock items from any manufacturer. Home construction of this circuit should not be attempted unless the builder has had considerable experience in the winding of inductive components and has access to the special equipment required. The builder should also refer to the general considerations for construction of high-frequency and broadband circuits given on page 582.

Parts List

$C_1, C_8, C_{16} = 16$ pF, ceramic
 $C_2, C_7 =$ trimmer capacitor, 2 to 12 pF, Arco No. 420 or equiv.
 $C_3, C_6 = 0.002$ μ F, tubular film
 $C_4, C_5, C_{18} =$ ganged tuning capacitors; each section = 5.5 to 22.5 pF
 $C_9 = 5000$ pF, ceramic
 $C_{10} = 2.7$ pF, ceramic
 $C_{11} = 0.01$ μ F, ceramic disc
 $C_{12}, C_{14}, C_{15} = 1000$ pF, ceramic disc
 $C_{13} =$ feedthrough capacitor, 1000 pF
 $C_{17} =$ trimmer capacitor, 2 to 17 pF, Arco No. 402 or equiv.
 $L_1 =$ tapped antenna coil (with antenna link); 4 turns of No. 18 bare copper wire, $\frac{1}{4}$ -inch diameter, $\frac{7}{16}$ -inch winding length, unloaded Q at 100 MHz = 130, tunes with 34-pF capacitance at

100 MHz; antenna link located approximately 1 turn from ground end of coil; gate tap (N_3) located approximately $1\frac{1}{2}$ turns from ground end.
 $L_2 =$ rf interstage coil, 4 turns of No. 18 bare copper wire, $\frac{1}{4}$ -inch inner diameter, $\frac{7}{16}$ -inch winding length; unloaded Q at 100 MHz = 120; base tap (N_2) located approximately $\frac{3}{4}$ turn from ground end.
 $L_3 =$ oscillator coil, 4 turns of No. 18 bare copper wire, $\frac{7}{32}$ -inch inner diameter, $\frac{7}{16}$ -inch winding length, unloaded Q at 100 MHz = 120, tunes with 34-pF capacitance at 100 MHz, emitter tap (N_3) located approximately $1\frac{1}{2}$ turns from ground end, base tap (N_2) located approxi-

mately 2 turns from ground end.
 $R_1 = 0.1$ megohm, 0.5 watt
 $R_2 = 0.22$ megohm, 0.5 watt
 $R_3, R_4 = 47000$ ohms, 0.5 watt
 $R_5 = 4700$ ohms, 0.5 watt
 $R_6 = 8200$ ohms, 0.5 watt
 $R_7 = 0.12$ megohm, 0.5 watt
 $R_8 = 22000$ ohms, 0.5 watt
 $T_1 =$ first if (10.7-MHz) transformer; double-tuned with 90 per cent of critical coupling; primary unloaded uncoupled $Q = 76$ with 47-pF tuning capacitance; primary: 15 turns of No. 32 enamel wire, space wound at 60 turns per inch on 0.25-by-0.5-inch slug; secondary: 18 turns of No. 36 enamel wire, close wound on 0.25 - by - 0.25-inch slug; both coils wound on $\frac{7}{32}$ -inch coil form.

Circuit Description (cont'd)

modulated rf input signal and the continuous-wave local-oscillator signal are applied to the base terminal of this transistor. The two signals are heterodyned in the mixer stage to produce the 10.7-MHz difference

frequency used as the intermediate frequency in FM receivers.

The 40244 bipolar oscillator transistor is operated in a common-collector circuit that generates an extremely clean oscillator waveform.

14-4 FM TUNER USING AN MOS-TRANSISTOR RF AMPLIFIER (cont'd)

Circuit Description (cont'd)

In addition, the low injection level at the base of the mixer transistor, 25 to 30 millivolts, together with the conservative design of the rf amplifier, limits the maximum possible signal at the input to the mixer. These factors further minimize the generation of spurious responses in the FM tuner.

The performance of this tuner with respect to sensitivity limiting, if rejection, image rejection, and other factors compares favorably with that of tuners using all high-performance bipolar transistor, as indicated by the chart of tuner performance characteristics. Tuner performance, however, particularly in relation to spurious-response rejection is highly dependent on factors such as physical layout, care

in construction, and power-supply decoupling. The use of a negative supply voltage facilitates the grounding of tuned circuits and decoupling of the supply.

Performance Characteristics

Carrier Frequency	100	MHz
Modulation	400 Hz, 22.5 kHz deviation	
Sensitivity:*		
For 20-db signal-to-noise ratio	1.4	μ V
For 30-db signal-to-noise ratio	2.2	μ V
For -3-db limiting point (with 94-db if strip)	1.6	μ V
Image Rejection♦	72	dB
IF Rejection♦	91	dB
Half-IF Rejection♦	96	dB
Rejection of Other Spurious Responses♦ (with 0.2 volt at antenna terminals)	>100	dB

* Measured at antenna terminals (300-ohm nominal impedance).
♦ Relative to 2 μ V.

14-5 FM TUNER USING AN MOS TRANSISTOR RF AMPLIFIER AND MIXER

Circuit Description

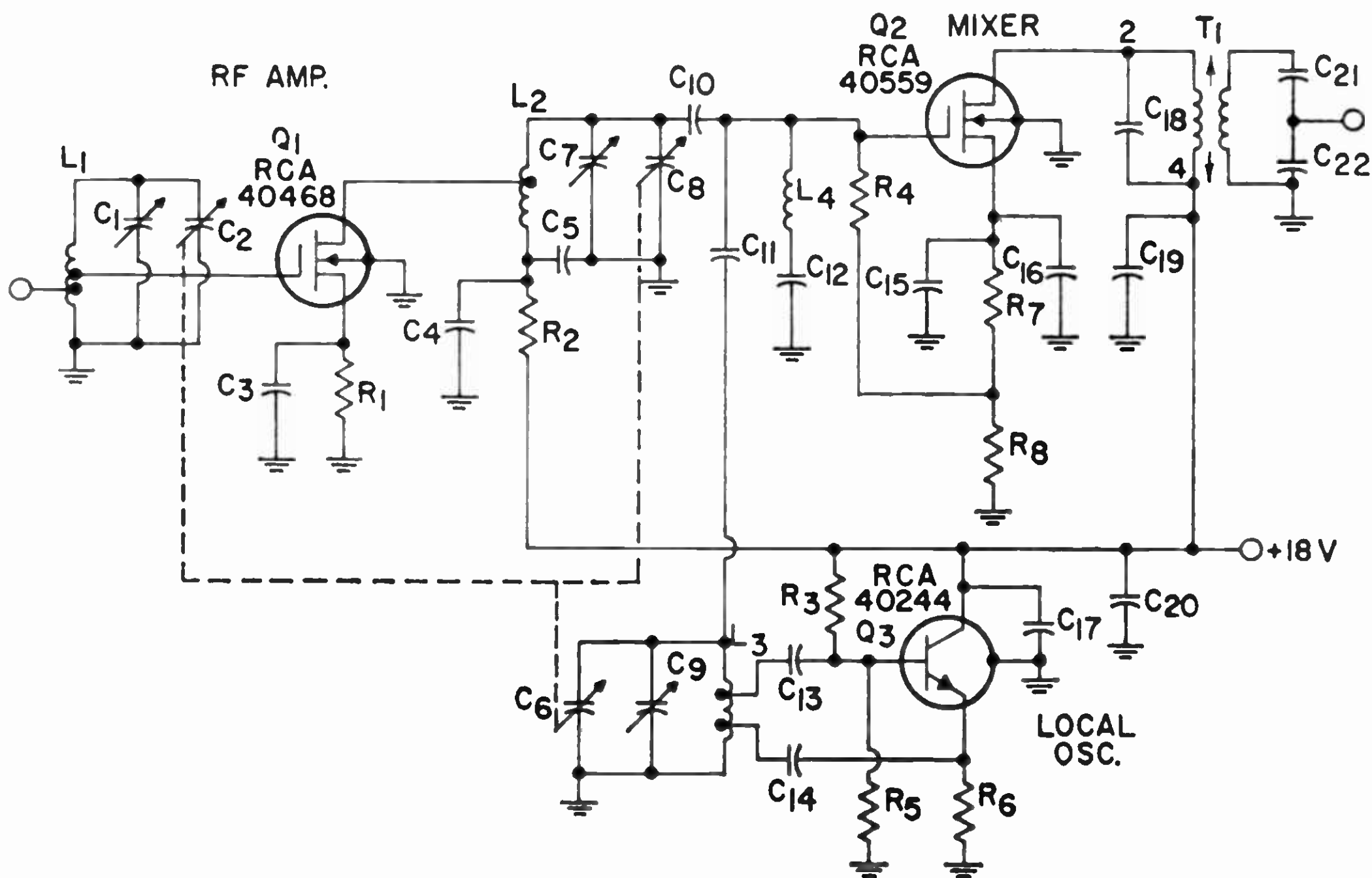
This FM tuner uses single-gate MOS field-effect transistors in the rf-amplifier and mixer stages and a bipolar transistor in the local oscillator to provide an over-all front-end-section gain of 30.2 dB. The 40468 rf-amplifier transistor operates in the common-source configuration with a stage gain of 12.7 dB. This stage is essentially identical to the rf amplifier of the FM tuner illustrated by circuit 14-4. The 40559 mixer transistor also operates in the common-source configuration, with both the rf and local-oscillator signals applied to the gate terminal. The 40244 bipolar oscillator transistor operates in the common-collector mode. The conversion power gain from the mixer stage is 17.5 dB.

The mixer circuit is designed for operation into an 8000-ohm-load. A load up to 12,000 ohms is permissible and provides a gain increase of about 1 dB from the mixer. The input circuit is tapped down by a 2.7-picofarad capacitor in series with the device input capacitance to improve dynamic range. These mismatch losses result in a stage gain of 17.5 dB, as compared to the maximum available gain of 21.5 dB shown in the published data for the 40559 transistor. The trap consisting of a 1-microhenry inductor (L_4) and 270-picofarad capacitor (C_{12}) is designed to bypass any 10.7-MHz component that may appear at the input to the mixer.

The biasing arrangement for the

14-5

FM TUNER USING AN MOS-TRANSISTOR RF AMPLIFIER AND MIXER (cont'd)



Parts List

C_1, C_7, C_9 = trimmer capacitor, 10 pF maximum, Arco No. 402 or equiv.
 C_2, C_6, C_8 = 3-gang tuning capacitor, TRW 5-plate model V2133 (with trimmers stripped off) or equiv.
 C_3, C_{17} = 0.002 μ F, tubular film
 $C_4, C_{16}, C_{19}, C_{25}, C_{29}, C_{34}$ = 0.01 μ F, ceramic disc
 $C_5, C_{13}, C_{15}, C_{27}, C_{32}, C_{36}$ = 0.001 μ F, ceramic disc
 C_{10} = 2.7 pF, ceramic
 C_{11} = 1.5 pF, ceramic disc
 C_{12} = 270 pF, ceramic
 C_{14} = 0.005 μ F, ceramic disc
 C_{18} = 68 pF, ceramic
 $C_{20}, C_{23}, C_{26}, C_{30}, C_{31}, C_{35}$ = 0.02 μ F, ceramic disc
 C_{21} = 50 pF, ceramic
 C_{22} = 1200 pF, ceramic
 C_{24}, C_{28} = 4.7 pF, silver mica
 C_{33} = 1 pF, silver mica
 C_{37}, C_{38} = 330 pF, miniature ceramic
 C_{39} = 10 μ F, electrolytic, 6 V
 L_1 = antenna coil; 5 turns of No. 18 bare copper wire wound on $1\frac{5}{64}$ -inch coil form; $\frac{1}{2}$ inch in length; slug-tuned with Arnold type IRN 0.25-by-0.25-inch slug (or equiv.); unloaded $Q = 164$; antenna tap at 0.8 turn and output tap at 1.4 turns from ground end.
 L_2 = rf interstage coil; 5

turns of No. 18 bare copper wire wound on $1\frac{5}{64}$ -inch coil form; $\frac{1}{2}$ inch in length; slug-tuned with Arnold 0.181-by-0.375-inch coil form; $\frac{1}{2}$ inch in length; loaded $Q = 104$

L_3 = oscillator coil; 5 turns of No. 18 bare copper wire, air core type with outer diameter of $\frac{3}{8}$ inch; $\frac{1}{2}$ inch in length; emitter tap at $1\frac{1}{2}$ turns and feedback tap at 2 turns from ground end; $Q = 164$.

R_1 = 200 ohms, 0.5 watt
 R_2, R_{10} = 430 ohms, 0.5 watt
 R_3 = 8200 ohms, 0.5 watt
 R_4 = 0.1 megohm, 0.5 watt
 R_5 = 15000 ohms, 0.5 watt
 R_6 = 4700 ohms, 0.5 watt
 R_7, R_{20} = 330 ohms, 0.5 watt
 R_8 = 680 ohms, 0.5 watt
 R_9, R_{14}, R_{18} = 12000 ohms, 0.5 watt
 R_{11}, R_{15}, R_{19} = 2700 ohms, 0.5 watt
 $R_{12}, R_{13}, R_{16}, R_{17}, R_{21}$ = 220 ohms, 0.5 watt
 R_{22} = 68 ohms, 0.5 watt
 R_{23} = 1000 ohms, 0.5 watt
 R_{24} = 1500 ohms, 0.5 watt
 R_{25}, R_{26} = 6800 ohms, 0.5 watt

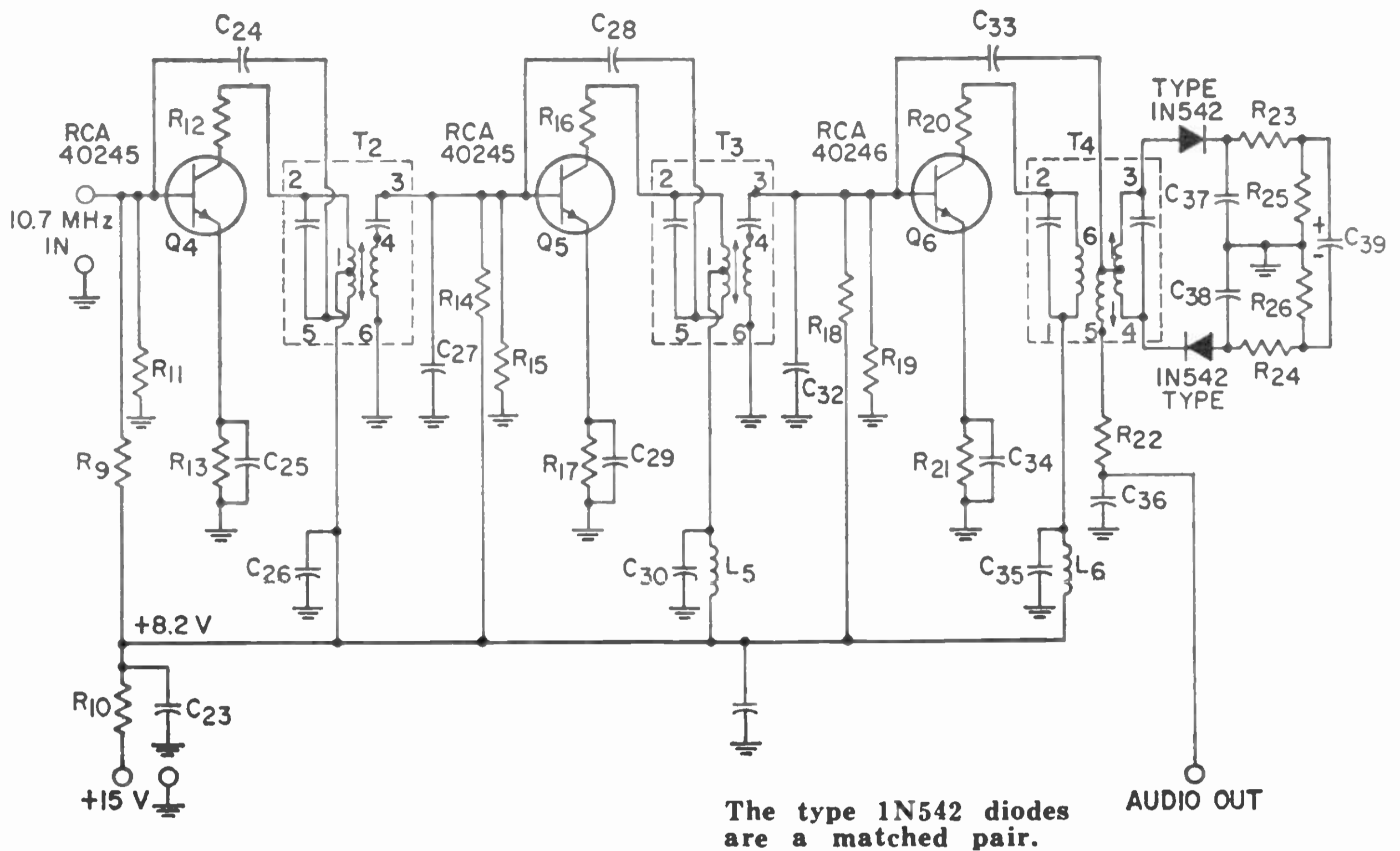
T_1 = first if (10.7-MHz) transformer; double-tuned with 90 per cent of critical coupling; primary unloaded uncoupled $Q = 76$ with 47-pF tuning capacitance; primary: 15

turns of No. 32 enamel wire, space wound at 60 turns per inch on 0.25-by-0.5-inch slug; secondary: 18 turns of No. 36 enamel wire, close wound on 0.25-by-0.25-inch slug; both coils wound on $\frac{3}{32}$ -inch coil form.

T_2, T_3 = if (10.7-MHz) transformer, double-tuned with 90 per cent of critical coupling, primary unloaded $Q = 72.4$, primary loaded $Q = 60$, ratio of full primary to section below tap (N_1/N_2) = 7.27, secondary unloaded $Q = 62.3$, secondary loaded $Q = 60$, ratio of full secondary to section that corresponds to lower tuning capacitor (N_3/N_4 , as determined by tapped capacitors) = 26.65, output impedance = 6070 ohms

T_4 = ratio-detector transformer, double-tuned with 90 per cent of critical coupling, primary unloaded Q (with tertiary winding N_2 returned to ground through a 68-ohm resistance) = 65, primary loaded $Q = 28.5$, primary-to-tertiary turns ratio (N_1/N_2) 2.5, secondary unloaded $Q = 65$, secondary loaded $Q = 24.75$, output impedance = 6070 ohms

14-5

FM TUNER USING AN MOS-TRANSISTOR
RF AMPLIFIER AND MIXER (cont'd)

NOTE: This circuit uses coils and transformers that are not available as stock items from any manufacturer. Home construction of this circuit should not be attempted unless the builder has had considerable experience in the winding of inductive components and has access to the special equipment required. The builder should also refer to the general considerations for construction of high-frequency and broadband circuits given on page 582.

Circuit Description (cont'd)

mixer stage is particularly important; substrate bias is used to provide the optimum combination of mixing and spurious-response rejection. On the basis of this requirement, the optimum operating conditions for the mixer circuit were empirically established at an effective gate bias of -1 volt and an effective substrate bias of -3 volts to provide a typical drain current of 3 milliamperes.

The 40244 common-collector local-oscillator circuit generates an extremely clean output waveform. The absence of harmonics in the oscillator signal is an important factor in good tuner design. The oscillator signal is coupled to the mixer gate by means of 1.5-picofarad capacitor C_{11} , which isolates the tuned circuit of the oscillator from the input circuit of the mixer and thus minimizes the possibility of oscillator

instabilities as a result of "pulling." The injection level at the gate of the mixer transistor is 700 millivolts.

The 10.7-MHz if output from the mixer is coupled to the first if-amplifier stage by means of a double-tuned transformer T_1 . The if amplifier employs two 40245 and one 40246 bipolar transistors, each operating in a neutralized common-emitter configuration at a collector current of 3.5 milliamperes. The over-all gain if the if amplifier is 88 dB. The frequency-modulated output of the if strip is demodulated by a ratio-detector circuit that uses a matched pair of 1N542 diodes. The operation of this if strip and ratio-detector circuit is very similar to the corresponding section of the High-Quality FM Tuner shown in circuit 14-3.

The performance of the single-

14-5 FM TUNER USING AN MOS-TRANSISTOR RF AMPLIFIER AND MIXER (cont'd)

Circuit Description (cont'd)

gate MOS tuner with respect to sensitivity, limiting, and particularly spurious response exceeds that obtained with the best bipolar transistors. The chart on tuner performance characteristics summarizes typical tuner capabilities. In general, spurious-response performance can be degraded by inadequate circuit layout and wiring practices. For this reason, care should be exercised in arranging the physical layout of the tuner, and power-supply decoupling should be used. The circuit

operates from a dc supply of 15 volts.

Performance Characteristics

Carrier Frequency	100	MHz
Modulation Frequency	400	Hz
Deviation (except IHFM) ...	22.5	kHz
Sensitivity:		
IHF _M	1.75	μV
20-dB Quieting	1.5	μV
30-dB Quieting	1.75	μV
3-dB Limiting	2.5	μV
Image Rejection	62	dB
IF Rejection	96	dB
Half-IF Rejection	92	dB
Spurious Response across		
VHF band with $e_{gen} =$		
0.35 volt		None

14-6 FM STEREO MULTIPLEX DEMODULATOR

Circuit Description

This FM stereo multiplex demodulator separates complex signals supplied by an FM tuner into right- and left-channel inputs for stereo audio output stages. The demodulator features a high input impedance, a noise immunity circuit, and automatic switching for stereophonic or monaural reception.

Operation of an FM tuner in the stereo mode may be unsatisfactory under weak-signal conditions because the signal-to-noise ratio is poorer for stereo reception than for monaural reception. In addition, if switching is permitted on weak signals the 19-kHz component of noise which is present between stations may cause undesired operation.

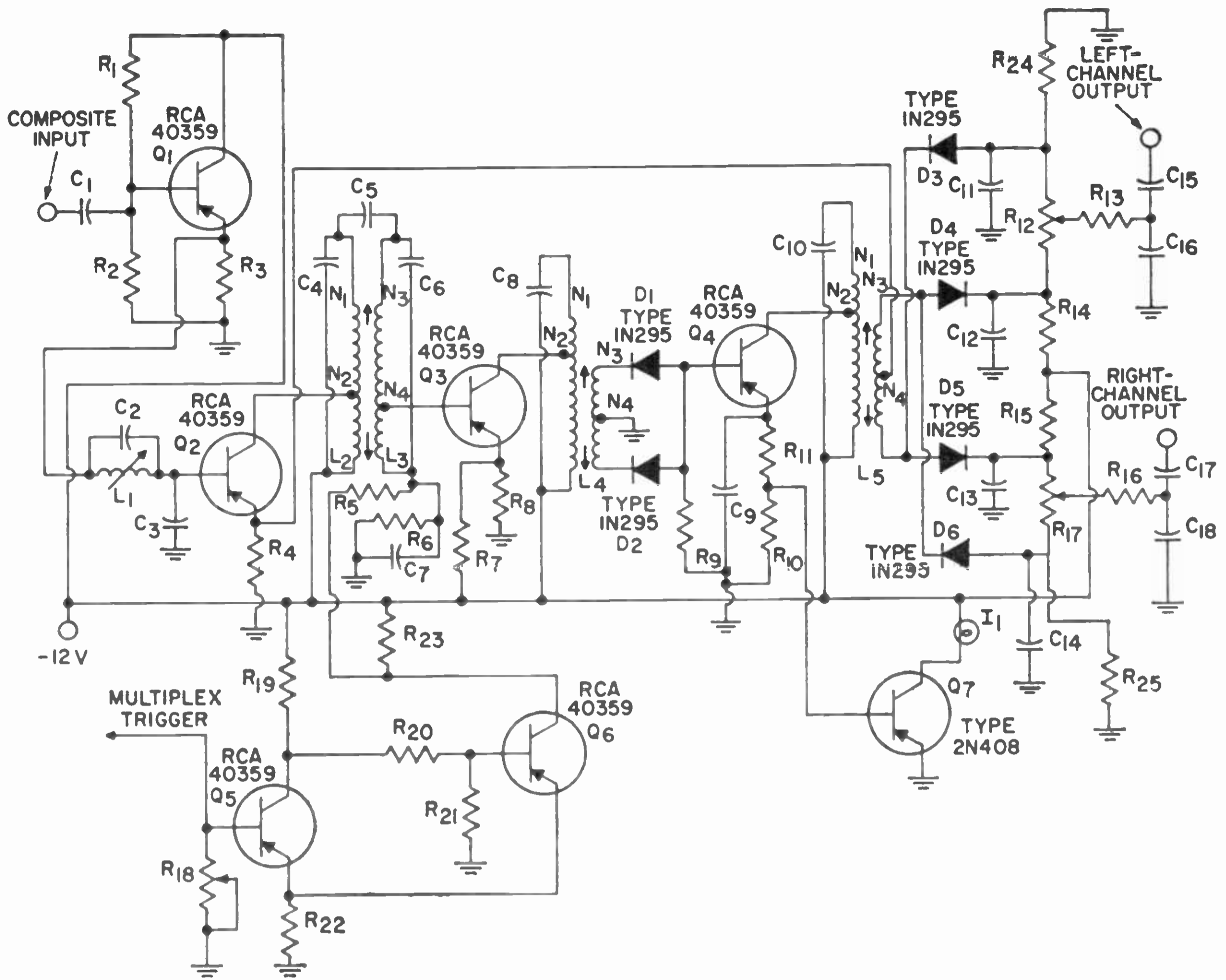
The demodulator incorporates circuits that sense the presence of adequately strong FM signals and provide automatic switching in the presence of 19-kHz pilot signal. It has a separation at 1 kHz of 36.5 dB, S.C.A. rejection of 59.4 dB, residual 38-kHz subcarrier rejection of 60 dB, insertion loss at 1 kHz of 2.5 dB, and total harmonic distortion at 1 kHz of 0.4 per cent. Six RCA-40359 transistors and one 2N408

transistor are used to provide the automatic switching and noise immunity. The demodulator is designed tuners, such as circuits 14-3, 14-4, and 14-5, which provide an audio output of approximately 400 millivolts with 75-kHz deviation under strong signal conditions. If a tuner that provides less audio output is used, the gain in the sub-carrier amplifier can be increased by bypassing R_8 . If a tuner of higher output is used, it may be necessary to use a voltage divider at the input.

The composite multiplex signal from the ratio detector of the FM tuner is applied to the base of transistor Q_1 . Transistor Q_1 is an isolation stage which provides a high-impedance load for the ratio detector and a low-impedance source for the S.C.A. filter. The parallel resonant circuit L_1C_2 is tuned to 72 kHz to provide maximum S.C.A. rejection at low beat frequencies.

Transistor Q_2 is a 19-kHz amplifier which also serves to separate the pilot from the composite signal. L_2 , L_3 , and C_5 constitute a top-coupled double-tuned circuit which resonates at 19 kHz and thus passes only the

74-6 FM STEREO MULTIPLEX DEMODULATOR (cont'd)



NOTE: This circuit uses coils and transformers that are not available as stock items from any manufacturer. Home construction of this circuit should not be attempted unless the builder has had considerable experience in the winding of inductive components and has access to the special equipment required. The builder should also refer to the general considerations for construction of high-frequency and broadband circuits given on page 582.

Parts List

- | | | |
|---|--|--|
| $C_1 = 0.33 \mu\text{F}$ | $L_2 = 69 \text{ mH}, Q = 93 \text{ at } 19 \text{ kHz}; N_1/N_2 = 5.66;$
(includes C_1) | $R_3 = 6800 \text{ ohms}, 0.5 \text{ watt}$ |
| $C_2 = 560 \text{ pF}$ | $L_3 = 69 \text{ mH}, Q = 93 \text{ at } 19 \text{ kHz}, N_1/N_2 = 40.2;$
(includes C_6) | $R_4 = 1000 \text{ ohms}, 0.5 \text{ watt}$ |
| $C_3 = 300 \text{ pF}$ (adjust for optimum separation) | $L_4 = 69 \text{ mH}, Q = 88 \text{ at } 19 \text{ kHz}, N_1/N_2 = 5.24, N_1/N_3 = 5.21, N_3/N_4 = 2;$
(includes C_5) | $R_5 = 18,000 \text{ ohms}, 0.5 \text{ watt}$ |
| $C_4 = 1000 \text{ pF}, \text{ part of } L_2$ | $L_5 = 41 \text{ mH}, Q = 108 \text{ at } 38 \text{ kHz}, N_1/N_2 = 11.62, N_1/N_3 = 19.8, N_3/N_4 = 2;$
(includes C_{10}) | $R_6, R_{13}, R_{16}, R_{21} = 3300 \text{ ohms}, 0.5 \text{ watt}$ |
| $C_5 = 10 \text{ pF}$ | | $R_7, R_9, R_{11}, R_{15}, R_{23}, R_{24}, R_{25} = 10,000 \text{ ohms}, 0.5 \text{ watt}$ |
| $C_6 = 1000 \text{ pF}, \text{ part of } L_3$ | | $R_8 = 510 \text{ ohms}, 0.5 \text{ watt}$ |
| $C_7, C_9 = 0.47 \mu\text{F}$ | | $R_{10} = 220 \text{ ohms}, 0.5 \text{ watt}$ |
| $C_8 = 1000 \text{ pF}, \text{ part of } L_1$ | | $R_{11} = 1500 \text{ ohms}, 0.5 \text{ watt}$ |
| $C_9 = 1000 \text{ pF}, \text{ part of } L_4$ | | $R_{12}, R_{17} = \text{potentiometer}, 5000 \text{ ohms}, 0.5 \text{ watt}$ |
| $C_{10} = 390 \text{ pF}, \text{ part of } L_5$ | | $R_{18} = \text{potentiometer}, 10,000 \text{ ohms}, 0.5 \text{ watt}$ |
| $C_{11}, C_{12}, C_{13}, C_{14} = 7500 \text{ pF}, \pm 5\%$ | | $R_{19} = 8200 \text{ ohms}, 0.5 \text{ watt}$ |
| $C_{15}, C_{17} = 1.0 \mu\text{F}$ | | $R_{20} = 15,000 \text{ ohms}, 0.5 \text{ watt}$ |
| $C_{16}, C_{18} = 0.02 \mu\text{F}$ | | $R_{22} = 820 \text{ ohms}, 0.5 \text{ watt}$ |
| $I_1 = \text{stereo lamp}, 14 \text{ mA at } 10 \text{ V}$ | | |
| $L_1 = 10 \text{ mH}, Q = 46 \text{ at } 67 \text{ kHz}$ | | |

Circuit Description (cont'd)

19-kHz portion of the composite signal to transistor Q3. The remainder of the signal is taken from the emit-

ter resistor R1 and fed into the balanced demodulator at the secondary winding of L5. Capacitor C3 compen-

14-6 FM STEREO MULTIPLEX DEMODULATOR (cont'd)

Circuit Description (cont'd)

sates for the degradation of the composite signal as it passes through the S.C.A. filter.

Transistors Q_5 and Q_6 comprise a Schmitt trigger used as a noise-immunity circuit. A negative agc voltage obtained from the if amplifier of the tuner is applied to the base of Q_5 . When no agc voltage is present, Q_5 is turned off, and Q_6 is turned on. In this state, which occurs under weak signal conditions, resistor R_5 is returned to a low-voltage point, and, therefore, transistor Q_3 is turned off. When a preset agc voltage is reached, Q_6 is turned off, R_5 is returned to the supply voltage through R_{23} , and Q_3 is turned on.

The multiplex output from the FM tuner drives the Schmitt trigger. The "on" trigger level can be adjusted by variation of R_{14} . The "off" trigger level is then determined by the hysteresis of the Schmitt-trigger circuit. Hysteresis is desirable because it prevents intermittent switching caused by slight signal variations in the vicinity of the trigger point. The hysteresis can be changed by adjustment of R_{10} .

Transistor Q_3 serves as a 19-kHz pilot amplifier and limiter when it is turned on by Q_6 . When Q_3 is turned off, it acts as an open switch which stops the pilot signal. The emitter of Q_3 is reverse-biased by the current through R_7 . Because this reverse bias exceeds the 19-kHz level at the base of Q_3 , it prevents the 19-kHz pilot signal of a weak station from turning on Q_3 and thereby over-riding the noise-immunity circuit.

The output of the pilot amplifier

Q_3 is fed to a balanced full-wave rectifier which consists of D_1 , D_2 , and the secondary winding of L_4 . The output of the rectifier is unfiltered and develops both a dc component and a 38-kHz component. The dc component is used to bias transistor Q_1 on. The 38-kHz component is amplified by Q_1 (which also acts as a limiter), and appears at the secondary winding of L_5 . In the absence of a pilot signal, Q_1 is turned off because there is no 19-kHz output from Q_3 to be rectified.

The composite signal taken from the emitter resistor R_4 is added to the 38-kHz subcarrier in the secondary winding of L_5 . When the subcarrier has the proper phase with respect to the composite signal, a 38-kHz amplitude-modulated signal is formed in which one side of the envelope contains right-channel information and the other side contains left-channel information.

Diodes D_3 and D_4 form a balanced detector which permits one side of the envelope to pass. Resistor R_{12} is adjusted for minimum 38-kHz residual signal at the output. When Q_1 is off and no subcarrier is present in the secondary winding of L_5 , the left-plus-right portion of the composite signal is passed by the detector circuit, and the left-minus-right portion is filtered out. Diodes D_5 and D_6 form the balanced detector for the other channel. R_{13} , C_{16} , R_{16} , and C_{18} form de-emphasis networks. Q_7 acts as a switch which lights a stereo indicator lamp when Q_1 is turned on.

14-7 PREAMPLIFIER FOR 6-, 10-, OR 15-METER AMATEUR-BAND RECEIVER

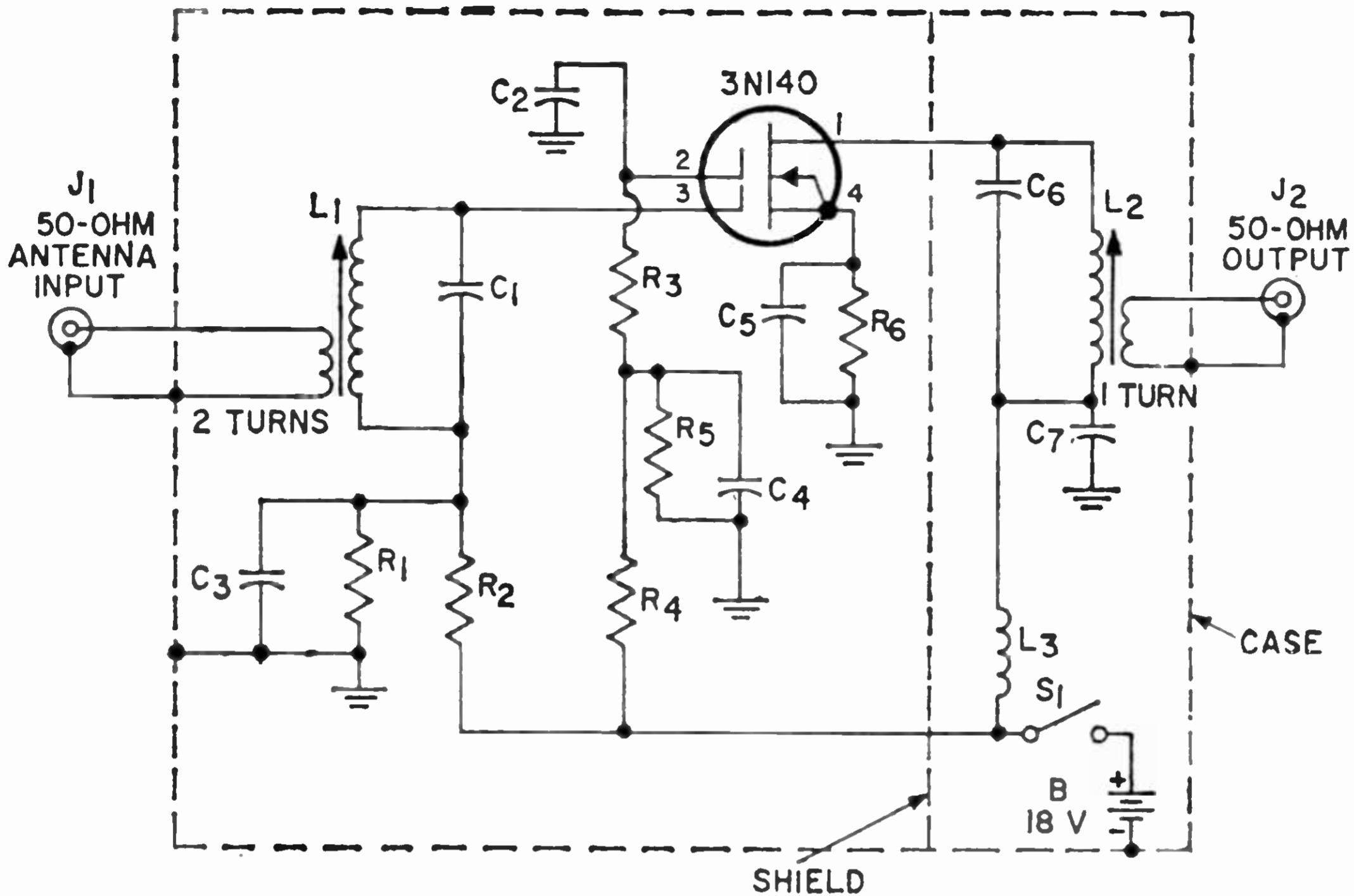
Circuit Description

This inexpensive, easily constructed preamplifier circuit uses an 3N140 dual-gate MOS transistor to provide more than 26 dB of gain

ahead of a receiver operated in the 6-, 10-, or 15-meter amateur band. This additional gain, together with the low noise figure of the pre-

14-7

PREAMPLIFIER FOR 6-, 10-, OR 15-METER AMATEUR-BAND RECEIVER (cont'd)



NOTE: See general considerations for construction of high-frequency and broadband circuits on page 582.

Parts List

B = Two RCA type VS323 batteries for transistor service; and one case, Bud-CU2103A or equivalent.
 C₁ = 8 pF, mica or ceramic tubular
 C₂, C₃, C₄, C₅, C₇ = 0.01 μF, ceramic
 C₆ = 10 pF, mica or ceramic tubular

J₁, J₂ = Coaxial receptacle, Amphenol BNC type UG-1094 or equiv.
 L₁, L₂ = 1.6 to 3.1 μH, adjustable, Miller 4404 or equiv.
 L₃ = 22 μH, Miller 74F-225A1 or equiv.
 R₁ = 27,000 ohms, 0.25 watt, 10%
 R₂ = 150,000 ohms, 0.25

watt, 10% carbon
 R₃ = 1,800 ohms, 0.25 watt, 10% carbon
 R₄ = 100,000 ohms, 0.25 watt, 10% carbon
 R₅ = 33,000 ohms, 0.25 watt, 10% carbon
 R₆ = 270 ohms, 0.25 watt, 10% carbon
 S₁ = toggle switch, single-pole, single-throw

Tuned-Circuit Components for 21 and 50 MHz

Component	Value	
	21 MHz	50 MHz
C ₁	22 pF	8 pF
C ₂ , C ₃ , C ₄ , C ₅ , C ₇	No Change	1,000 pF, ceramic
C ₆	22 pF	10 pF
L ₁	No Change	8 turns, No. 30 E wire on 1/4-inch diameter core (Miller 4500 or equiv.) Link: 2 turns, No. 30 E wire on ground end.
L ₂	No Change	Same as L ₁
L ₃	No Change	6.8 μH (Miller 74F686AP or equiv.)

14-7 PREAMPLIFIER FOR 6-, 10-, OR 15-METER AMATEUR-BAND RECEIVER (cont'd)

Circuit Description (cont'd)

amplifier (less than 2.5 dB), substantially increases both the sensitivity and signal-to-noise ratio of the receiver. The circuit as shown is intended for use in the 10-meter (28-MHz) frequency band; the 3N140 MOS transistor, however, has excellent performance characteristics at frequencies well below the 10-meter band and up to 200 MHz. The preamplifier, therefore, can be readily adapted for use in other frequency bands with only a few changes in tuned-circuit components. A chart is provided to show the changes in tuned-circuit components required for operation in the 15-meter (21-MHz) and 6-meter (50-MHz) bands. The dc operating voltage for the preamplifier may be obtained from a battery supply, as shown in the circuit diagram, or from any other reasonably well-filtered dc supply voltage of 15 to 18 volts.

The dual-gate MOS transistor in the preamplifier is operated so that essentially it is electrically equivalent to two single-gate MOS transistors connected in cascode and enclosed in the same package. The advantage of the dual gate transistor is that it provides an inexpensive cascode circuit that offers maximum resistance to cross-modulation from nearby transmitters.

The rf input is link coupled from

the antenna to the input tuned circuit formed by L_1 and C_1 and applied to gate No. 1 (pin 3) of the 3N140 transistor. This gate, which is equivalent to the gate (or base) of the grounded-source (or -emitter) section of a two-transistor cascode circuit, is forward-biased by the dc voltage at the junction of the voltage-divider resistors R_1 and R_2 . The source resistor R_2 is large enough to assure that gate No. 1 is always negative with respect to the source. Gate No. 2 (pin 2), in accordance with cascode-circuit requirements, is returned to ac ground through capacitor C_2 . The dc bias level for this gate, established by the voltage divider R_3 and R_5 , represents a compromise between optimum gain and optimum cross-modulation resistance. The amplified rf signals developed in the drain circuit of the 3N140 transistor are link coupled from the tuned-circuit drain load impedance formed by L_2 and C_3 , through coaxial connector J_2 to the input of the receiver.

Tuning of the preamplifier is simplified because no special neutralization is required, even at frequencies as high as 155 MHz. Rough adjustments of coils L_1 and L_2 can be made by use of a grid-dip oscillator. The finishing adjustments are then made while listening to a weak station.

14-8

TWO-METER CONVERTER

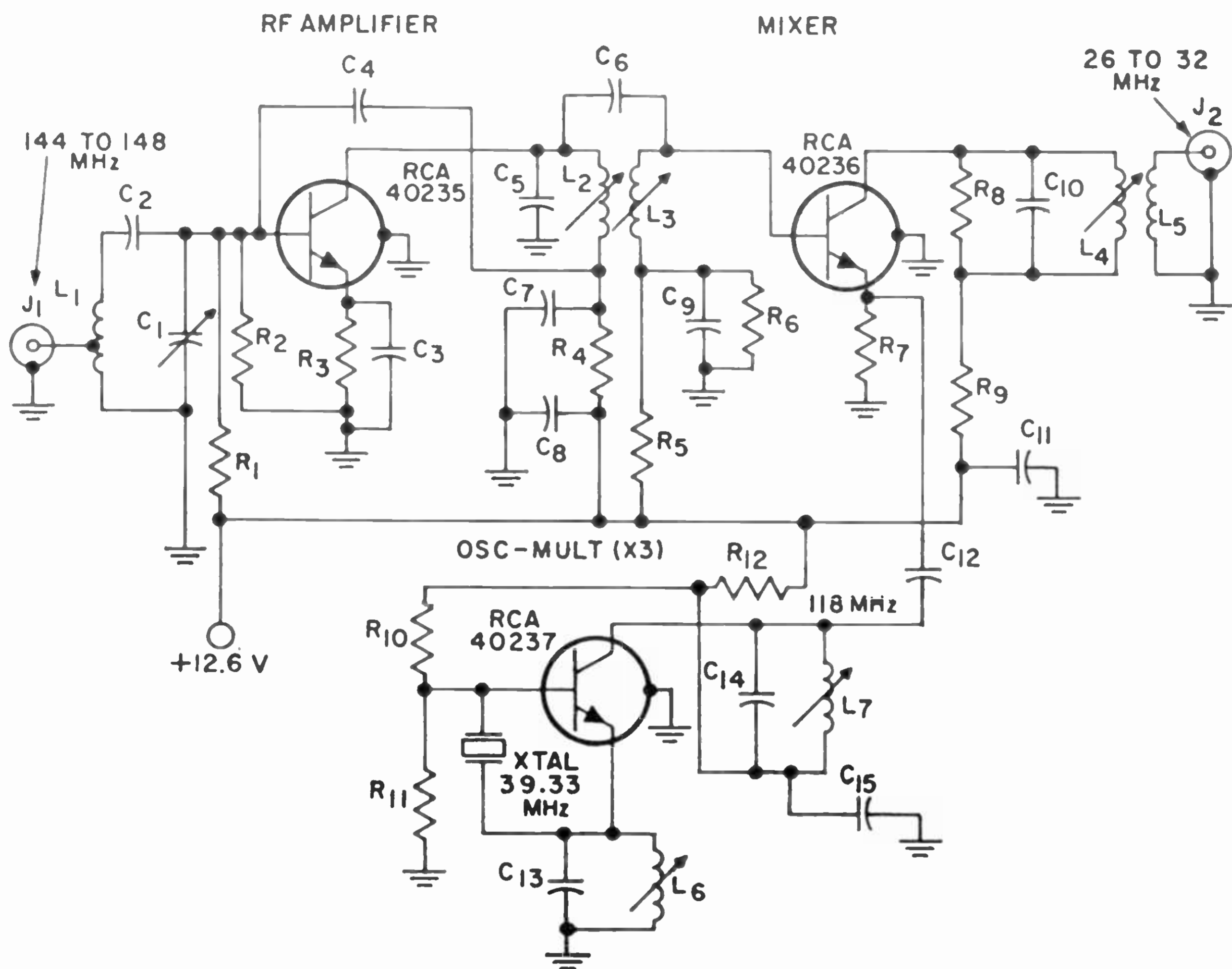
Circuit Description

This converter circuit can be used ahead of a 10-meter amateur-band radio receiver to provide amplification and the frequency conversion required to enable reception of signals in the 2-meter (144-to-148-MHz) amateur band. With minor

circuit modification, the converter can also be used to adapt a 20-meter amateur-band receiver to receive 2-meter signals. The converter uses RCA 40235, 40236, and 40237 vhf transistors in common-emitter circuit configurations to provide to

14-8

TWO-METER CONVERTER (cont'd)



NOTES: (1) See general considerations for the construction of high-frequency and broadband circuits on page 582. (2) This circuit uses coils that are not standard commercial items; such coils must be wound by the circuit builder.

Parts List

$C_1 = 0.5$ to 5 pF, tubular trimmer, Erie 532-3R or equiv.
 $C_2 = 10$ pF, ceramic tubular, Centralab TCZ-10 or equiv.
 $C_3, C_9, C_{11} = 500$ pF, silver button, Erie 662-003-501K or equiv.
 $C_4 = 4.7$ pF, ceramic tubular, Centralab TCZ-4R7 or equiv.
 $C_5, C_{12}, C_{14} = 3.3$ pF, ceramic tubular Centralab TCZ-3R3 or equiv.
 $C_6 = 2.2$ pF, ceramic tubular, Centralab TCZ-2R2 or equiv.
 $C_7 = 25$ pF silver button, Erie 662-003-250 or equiv.
 $C_8, C_{13}, C_{15} = 500$ pF, ceramic disc, Centralab DD-501 or equiv.

$C_{10}, C_{13} = 30$ pF, ceramic tubular, Centralab TCZ-30 or equiv.
 $J_1, J_2 =$ BNC-type coaxial jack
 $L_1 = 5$ turns of No. 16 bare wire, $\frac{1}{4}$ -inch diameter (spaced wire diameter), tap one turn up from bottom
 $L_2, L_3 = 4$ turns of No. 26 enamelled wire, close wound on $\frac{1}{4}$ -inch diameter ceramic slug-tuned form, Miller 4500 or equiv.
 $L_4 = 11$ turns of No. 26 enamelled wire, close wound on $\frac{3}{8}$ -inch diameter phenolic slug-tuned form, Miller 21A000RBI or equiv.
 $L_5 = 3$ turns of insulated wire, close-wound link

$L_6 = 5$ turns of No. 26 enamelled wire, close wound on $\frac{3}{8}$ -inch diameter phenolic slug-tuned form, Miller 21A000RBI or equiv.
 $L_7 = 7$ turns of No. 26 enamelled wire, close wound on $\frac{1}{4}$ -inch diameter ceramic slug-tuned form, Miller 4500 or equiv.
 $R_1 = 27,000$ ohms, 0.5 watt
 $R_2 = 3,900$ ohms, 0.5 watt
 $R_3, R_7 = 470$ ohms, 0.5 watt
 $R_4, R_9 = 820$ ohms, 0.5 watt
 $R_5 = 18,000$ ohms, 0.5 watt
 $R_6 = 2,700$ ohms, 0.5 watt
 $R_8 = 5,100$ ohms, 0.5 watt
 $R_{10} = 0.1$ megohm, 0.5 watt
 $R_{11} = 8,200$ ohms, 0.5 watt
 $R_{12} = 1,000$ ohms, 0.5 watt
 XTAL = 39.33 MHz, overtone crystal

Circuit Description (cont'd)

required amplification and frequency-conversion functions with a noise figure (at 144 MHz) of less than

3 dB. The circuit operates from a 12.6-volt, 10-milliampere dc supply and, therefore, is ideally suited for

14-8

TWO-METER CONVERTER (cont'd)

Circuit Description (cont'd)

mobile, as well as fixed-station, operations.

The 40235 transistor is used in a neutralized low-noise rf-amplifier stage. Capacitor C_4 couples the neutralizing feedback from collector circuit to base circuit required to ensure stable operation of this stage. Signals in the two-meter band are coupled from the antenna through the coaxial connector J_1 and the tuned input circuit formed by L_1 , C_1 and C_2 to the base of the 40235 transistor. The variable capacitor C_1 is adjusted to tune the input circuit to select any desired signal in the 144-to-148-MHz frequency band. The selected signals are amplified by the 40235 transistor and coupled from the collector circuit of this transistor by tuning coils L_2 and L_3 and capacitor C_6 to the base of the 40236 transistor used in the mixer stage.

The 40237 transistor is operated in an overtone-crystal oscillator-multiplier stage to develop the local-oscillator signal for the converter. The crystal used in the base-to-emitter circuit of the oscillator-multiplier has a fundamental frequency of 39.33 MHz; the collector load circuit, formed by oscillator tuning coil L_7 and capacitor C_{14} , however, is tuned to select the third harmonic of the crystal fundamental. The oscillator-multiplier stage, therefore, develops a fixed-frequency 118-MHz local-oscillator signal that is coupled by capacitor C_{12} to the

emitter circuit of the 40236 mixer transistor.

In the mixer stage, the rf input signal from the antenna and the local-oscillator signal are heterodyned to derive the difference frequency used as the input to the 10-meter-band receiver. Output tuning coil L_4 , capacitor C_{10} , and resistor R_4 forms a collector load circuit that is broadly tuned to select the difference-frequency signal developed in the mixer stage. This signal is transferred by the coupling link L_5 and the coaxial connector J_2 to the input of the 10-meter-band receiver.

The 118-MHz local-oscillator frequency was selected so that the heterodyning action in the mixer provides a converter output of 26 to 32 MHz, depending upon the frequency of the selected rf input signal from the antenna. For example, a 144-MHz rf input signal results in a difference-frequency output of 144 MHz—118 MHz (or 26 MHz; a 148-MHz input frequency results in an output frequency of 148 MHz—118 MHz, or 32 MHz. The converter circuit, however, can be readily modified to provide a lower-frequency output. If it is desired to adapt a 20-meter-band receiver to receive 2-meter-band signals, it is necessary merely to use a crystal that has a fundamental frequency of 43.33 MHz and to double the number of turns in the output tuning coil L_4 . No other changes are required.

14-9

STABLE VARIABLE-FREQUENCY OSCILLATOR

Circuit Description

This VFO circuit uses a 40468 or 3N128 MOS transistor in a highly stable variable-frequency oscillator stage and 40245 and 2N3241A bipolar transistors in a two-stage

isolation (output) amplifier to achieve exceptional frequency stability at low dc operating potentials. The MOS-transistor oscillator circuit is useful at any frequency up

14-9 STABLE VARIABLE-FREQUENCY OSCILLATOR (cont'd)

Circuit Description (cont'd)

to and including the 144-MHz band. Tuned-circuit data are provided for the standard 3.5-to-4-MHz band, for the 5-to-5.5-MHz band for single-sideband transmitters, and for the 8-to-9-MHz band for 50- and 144-MHz transmitters. (See chart on page 607.)

The oscillator stage is a Colpitts type. The variable capacitor C_1 is the tuning control for the circuit. With a Millen 10037 (or equivalent) "no sting" dial coupled to the shaft of this capacitor, the oscillator tuning range encompasses essentially the full dial area. Capacitor C_2 is the trimmer adjustment for the circuit. The effect of changes in transistor-element capacitances is reduced to a minimum by use of a three-capacitor (C_4 , C_5 , and C_6) voltage divider. The relatively large values of the capacitors C_5 and C_6 , which are connected across the gate-to-source circuit of the MOS transistor, almost completely obviate the effect of the transistor capacitances. The rf choke L_1 provides the required low voltage (IR) drop for the source current of the MOS transistor.

The 1N914 silicon rectifier in the gate circuit of the oscillator stage is used to provide the rectified gate current for the MOS transistor. This rectifier makes possible a degree of automatic bias comparable to that obtainable with an electron tube and, in this way, contributes substantially to the frequency stability of the VFO circuit. The use of silver-mica types for all fixed-value capacitors in the oscillator stage assures a stable frequency-temperature characteristic.

The output of the oscillator stage is coupled from the source of the MOS transistor, through capacitor C_7 and resistor R_1 , to the base of the 40245 bipolar transistor used in the input stage of the isolation amplifier. The output of the 40245 transistor, in turn, drives the 2N3241A emitter-follower output stage. The isolation amplifier is es-

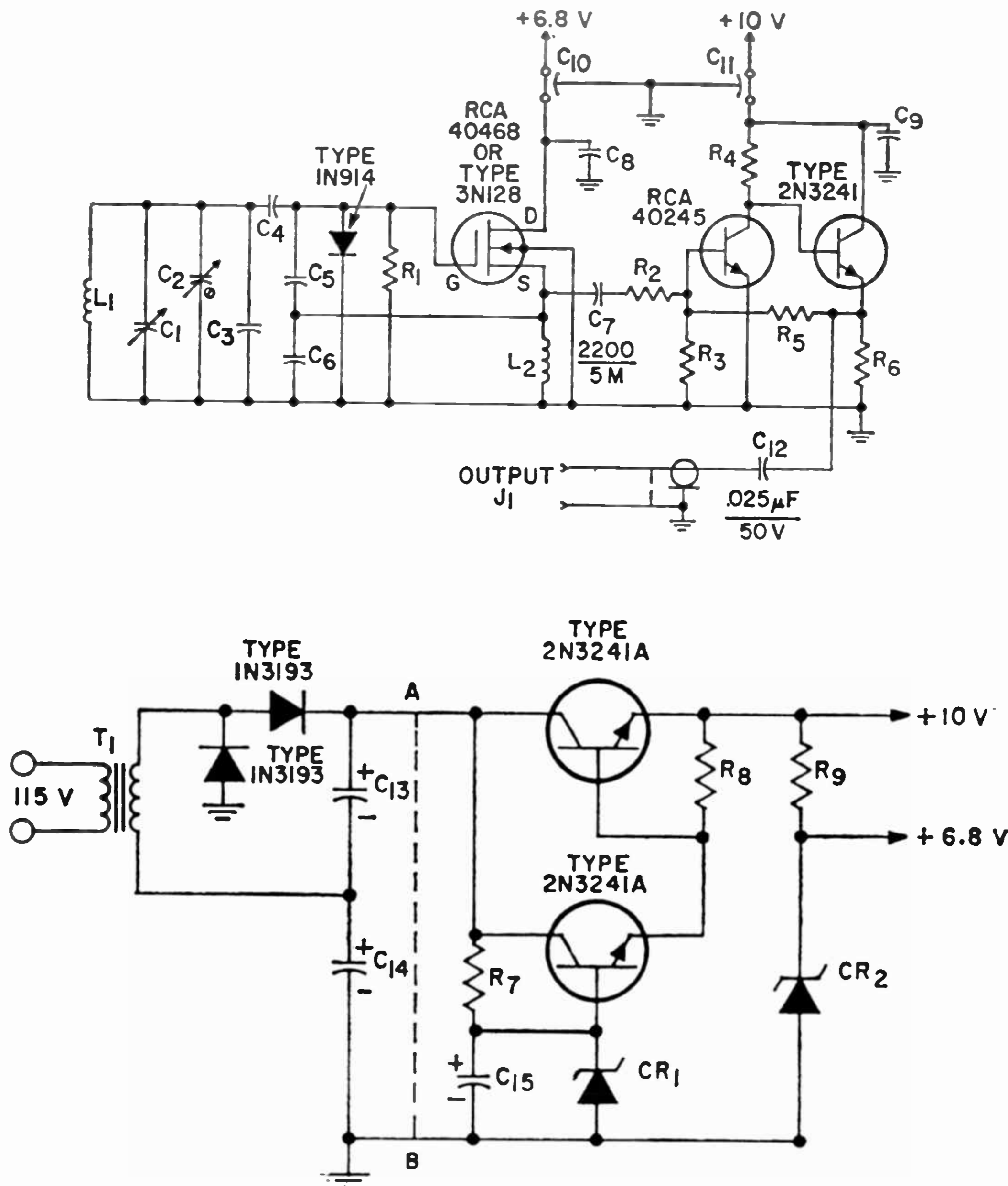
entially a two-stage, direct-coupled, negative-feedback output circuit that greatly reduces the effect of a change in output conditions on oscillator performances and provides a convenient means (by a change in the value of resistor R_1) to vary the output voltage of the VFO circuit.

The dc operating potentials for the VFO circuit can be obtained directly from a 12-volt source. For operation from a 117-volt, 60-Hz ac source, a low-voltage dc supply, such as that shown in the circuit diagram, may be used to supply the required voltage. The 117-volt ac source voltage is stepped down to 6.3 volts ac by the power transformer T_1 and then converted to a dc voltage of 12 volts by the voltage-doubler circuit formed by the 1N3193 rectifier diodes and filter capacitors C_{13} and C_{14} . The two 2N3241A bipolar transistors and the Zener diodes CR_1 and CR_2 connected between points A and B of the voltage-doubler circuit form an electronic voltage regulator that maintains constant dc output voltages with changes in the input ac voltage.

The voltage-regulator circuit is also used when the VFO is operated in a mobile system. For this type of operation, the power transformer T_1 and the voltage doubler are disconnected from the remainder of the circuit, and points A and B are connected to the positive and negative terminals, respectively, of a 12-volt battery.

The VFO circuit is characterized by its exceptional frequency stability. A unit designed to operate in the 3.5-to-4-MHz frequency range exhibits a frequency drift of less than 30 Hz in 2 hours after a 30-second warm-up. A 5-to-5.5-MHz unit has a frequency drift of less than 50 Hz for the same period, and a 8-to-9-MHz unit has a frequency drift of only slightly more than 200 Hz.

14-9 STABLE VARIABLE-FREQUENCY OSCILLATOR (cont'd)



NOTE: See general considerations for the construction of high-frequency and broadband circuits on page 582.

Parts List

C_1 = Double-bearing variable capacitor, Millen 23100 or 23050 (or equiv.) depending upon frequency range (see Tuned-Circuit Data)
 C_2 = Air-type trimmer capacitor, 25 pF maximum, Hammarlund APC-25 or equiv.
 C_3, C_4, C_5, C_6 = silver-mica capacitors (see Tuned-Circuit Data for values)
 C_7 = 2200 pF, silver mica
 C_8 = 0.05 pF, ceramic disc, 50 V.
 C_9 = 0.1 pF, ceramic disc, 50 V.

C_{10}, C_{11} = 1500 pF, feed-through
 C_{12} = 0.025 μ F, ceramic disc, 50 V.
 C_{13} = 500 μ F, electrolytic, 12 V.
 C_{14} = 500 μ F, electrolytic, 12 V.
 C_{15} = 50 μ F, electrolytic, 12 V.
 CR_1 = Zener diode, 12-volt, 1-watt
 CR_2 = Zener diode, 6.8 volt, 1-watt
 J_1 = Coaxial connector
 L_1 = Variable inductor (see Tuned-Circuit Data for details)

L_2 = Miniature rf choke, 2.5 mH, iron core
 R_1 = 22000 ohms, 0.5 watt
 R_2 = 12000 to 47000 ohms, 0.5 watt; select value for 2-volt peak output level at input to transmitter
 R_3 = 12000 ohms, 0.5 watt
 R_4 = 820 ohms, 0.5 watt
 R_5 = 47000 ohms, 0.5 watt
 R_6 = 240 ohms, 0.5 watt
 R_7 = 2200 ohms, 0.5 watt
 R_8 = 220 ohms, 0.5 watt
 R_9 = 180 ohms, 0.5 watt
 T_1 = 6.3-volt, 1.2-ampere filament transformer

14-9 STABLE VARIABLE-FREQUENCY OSCILLATOR (cont'd)

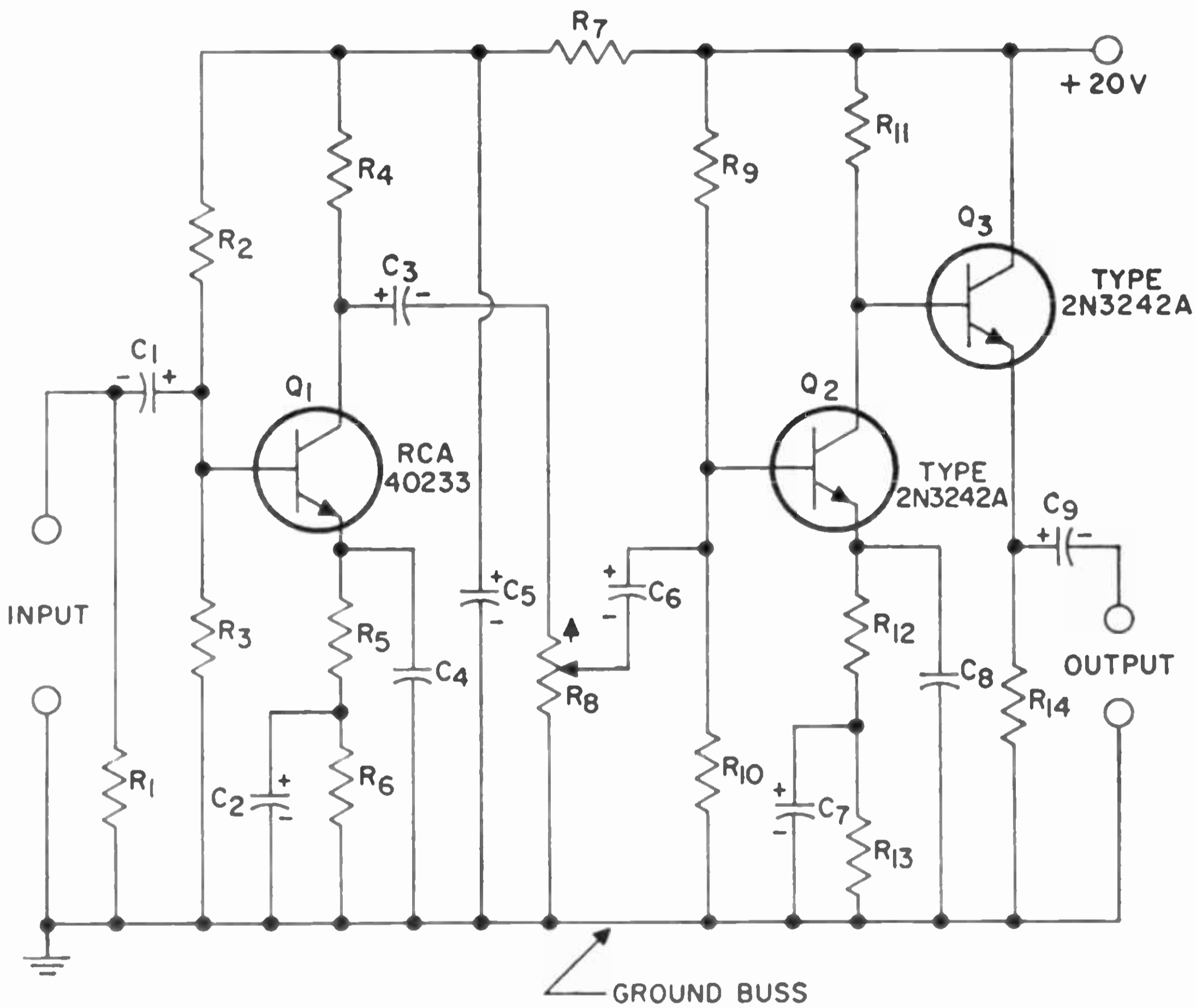
Tuned-Circuit Data

	3.5-4.0 MHz	5.0-5.5 MHz	8.0-9.0 MHz
L₁			
No. of turns	17*	14 ³ / ₄ *	11 ¹ / ₂ **
Wire size	20	20	18
Turns/inch	16	16	8
Diam., inches	1	1	1
C ₁ , p.	100	50	50
C ₂ , pf.	25	25	25
C ₃ , pf.	100	None	None
C ₄ , pf.	390	390	270
C ₅ , pf.	680	680	560
C ₆ , pf.	680	680	560

* B & W 3015, AirDux 816T, or equiv.
 ** B & W 3014, AirDux 808T, or equiv.

14-10

MICROPHONE PREAMPLIFIER With High Dynamic Range



Parts List

C₁, C₆ = 15 μF, electrolytic, 6 V
 C₂, C₇ = 300 μF, electrolytic, 6 V
 C₃ = 10 μF, electrolytic, 15 V
 C₄, C₅ = 0.05 μF, paper
 C₈ = 250 μF, electrolytic, 25 V
 C₉ = 50 μF, electrolytic, 15 V

R₁ = value required to match microphone line impedance (up to 10000 ohms), 10%, 0.5 watt
 R₂, R₉ = 0.1 megohm, 10%, 0.5 watt
 R₃, R₁₀ = 6200 ohms, 10%, 0.5 watt
 R₄, R₁₁ = 10000 ohms, 10%, 0.5 watt

R₅, R₁₂ = 68 ohms, 10%, 0.5 watt
 R₆, R₁₃ = 470 ohms, 10%, 0.5 watt
 R₇ = 820 ohms, 10%, 0.5 watt
 R₈ = potentiometer, 10000 ohms, 0.5 watt, audio taper
 R₁₄ = 1000 ohms, 0.5 watt

14-10 MICROPHONE PREAMPLIFIER (cont'd)

Circuit Description

This three-stage preamplifier is designed for use with high-level microphones. It has an over-all voltage gain of 1500 to 2000 and can provide a maximum undistorted output voltage of 5 volts rms to a load impedance of 500 ohms or greater for a maximum undistorted input of 0.4 volt rms. The frequency response of the preamplifier is flat from 20 Hz to 30 kHz. The dc power requirements of the circuit are 20 volts at 30 milliamperes.

The preamplifier uses a low-noise 40233 in a class A input stage and two 2N3242A transistors in direct-coupled class A driver and emitter-follower output stages. The circuit operates equally well with either low-impedance or high-impedance microphones provided that the value of the input resistor R_1 is selected to match the microphone line impedance up to a maximum of 10,000 ohms.

14-11 HIGH-FIDELITY PREAMPLIFIER FOR PHONO, FM, OR TAPE PICKUP

Circuit Description

This phonograph preamplifier can be used with an audio power amplifier, such as circuits 14-15 through 14-19, to provide an excellent high-fidelity system. The circuit is designed for use with a magnetic pickup that can supply an input signal of at least 5 millivolts. Provisions are also included in the preamplifier for tape and tuner inputs. For a 5-millivolt input signal, the preamplifier delivers an output of at least 1 volt. An input of 300 millivolts from a tuner or tape recorder is required to produce an output of 1 volt. The preamplifier requires a dc supply of 20 volts at 7.5 milliamperes.

The preamplifier uses a low-noise 40233 transistor Q_1 and a 2N3242A transistor Q_2 in a two-stage direct-coupled input circuit. A frequency-shaping network in the feedback circuit of transistor Q_2 provides frequency compensation when the preamplifier is used with a magnetic phonograph pickup. The output circuit of transistor Q_2 contains a level control R_{10} that feeds the loudness control R_{12} through the selector

switch S_1 . The loudness control, in turn, drives the tone-control circuits of the preamplifier. Tape, tuner, or phono inputs can be selected by means of the selector switch; an output connector in the arm of the selector switch permits tape recordings to be made without affecting volume or loudness and vice versa.

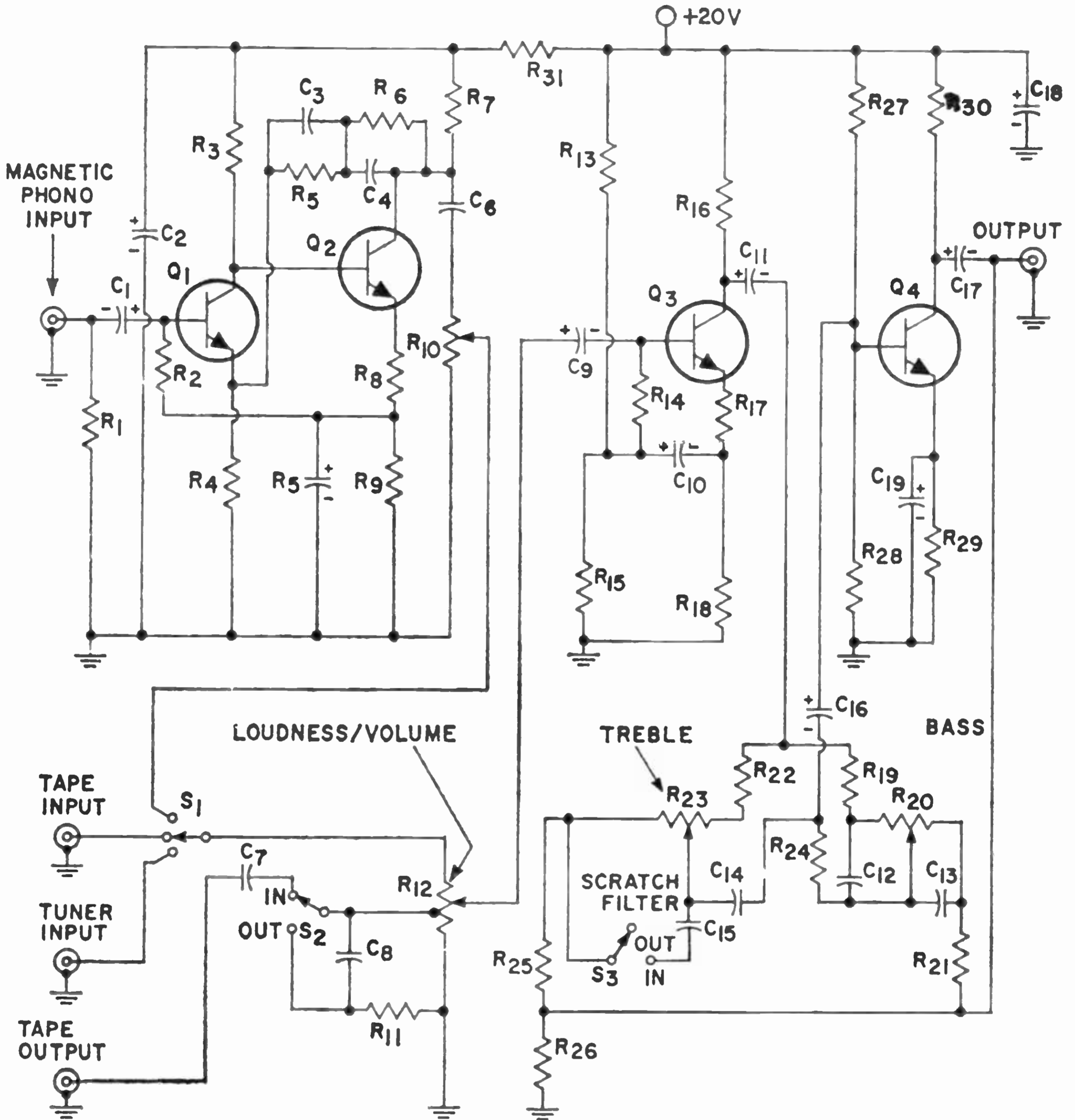
The treble and bass tone controls provide boost of 10 dB and cut of 15 dB for deep bass and high treble frequencies. Each control operates independently so that precise tone shaping is possible. When both controls are in the center position, the response is flat; the bass and treble frequencies are equally mixed.

Output distortion is low at all frequencies for any setting of either the bass or the treble tone control. The collector-to-base feedback in the 2N3242A transistors Q_3 and Q_4 works with the tone controls to provide the over-all tonal response of the preamplifier.

Included in the preamplifier is a loudness/volume control switch S_2 . With the loudness control in, lower

14-11

HIGH-FIDELITY PREAMPLIFIER (cont'd)



Parts List

C₁ = 2 μF, electrolytic, 6 V
 C₂, C₁₇, C₁₈ = 25 μF, electrolytic, 25 V
 C₃ = 0.0027 μF, paper, 200 V
 C₄ = 0.01 μF, paper, 200 V
 C₅ = 100 μF, electrolytic, 3 V
 C₆ = 1 μF, electrolytic, 25 V
 C₇ = 180 pF, mica, 500 V
 C₈ = 0.033 μF, paper, 200 V
 C₉ = 1 μF, electrolytic, 12 V
 C₁₀, C₁₆ = 10 μF, electrolytic, 10 V
 C₁₁ = 10 μF, electrolytic, 25 V

C₁₂, C₁₃ = 0.022 μF, paper, 200 V
 C₁₄ = 0.0039 μF, paper, 200 V
 C₁₅ = 0.0047 μF, paper, 200 V
 C₁₉ = 100 μF, electrolytic, 6 V
 R₁, R₃ = 6800 ohms, 10%, 0.5 watt
 R₂ = 0.18 megohm, 10%, 0.5 watt
 R₄ = 470 ohms, 10%, 0.5 watt
 R₅ = 27000 ohms, 10%, 0.5 watt
 R₆ = 0.47 megohm, 10%, 0.5 watt

R₇, R₁₀, R₂₁, R₂₄ = 10000 ohms, 10%, 0.5 watt
 R₈ = 82 ohms, 10%, 0.5 watt
 R₉ = 1800 ohms, 10%, 0.5 watt
 R₁₀ = potentiometer, 0.1 megohm, 0.5 watt, audio taper
 R₁₁ = 8200 ohms, 10%, 0.5 watt
 R₁₂ = potentiometer, 0.25 megohm, 0.5 watt, audio taper with tap, Centralab F11-250K or equiv.
 R₁₃ = 33000 ohms, 10%, 0.5 watt

14-11 HIGH-FIDELITY PREAMPLIFIER (cont'd)

Parts List (cont'd)

R ₁₄ , R ₂₈ = 18000 ohms, 10%, 0.5 watt	ohms, 10%, 0.5 watt	R ₃₀ = 2700 ohms, 10%, 0.5 watt
R ₁₅ , R ₃₁ = 4700 ohms, 10%, 0.5 watt	R ₂₀ , R ₂₃ = potentiometer, 0.1 megohm, 0.5 watt, linear taper	S ₁ = switch, single-pole, 3-position, wafer
R ₁₆ = 6800 ohms, 10%, 0.5 watt	R ₂₆ = 47000 ohms, 10%, 0.5 watt	S ₂ = switch, single-pole, double-throw, toggle
R ₁₇ = 68 ohms, 10%, 0.5 watt	R ₂₇ = 56000 ohms, 10%, 0.5 watt	S ₃ = switch, single-pole, single-throw, toggle
R ₁₈ , R ₂₂ , R ₂₅ , R ₂₉ = 1000		

Circuit Description (cont'd)

tones are enhanced at low output levels and a more pleasing sound is produced; when the loudness control is switched out, the volume control attenuates all tones equally.

The scratch filter attenuates somewhat the frequencies at which scratch noise from scratched records is most prevalent.

14-12 HIGH-QUALITY PREAMPLIFIER FOR PHONO, FM, OR TAPE PICKUP

Circuit Description

This preamplifier has equalized input circuits for FM stereo (flat), ceramic and magnetic phonograph pickups, and tape-recorder heads. Level controls are provided for FM and ceramic and magnetic phonograph inputs. High input impedance and input equalization are provided in each operating mode by a directly coupled two-stage input section that uses frequency-sensitive negative feedback to provide the desired input characteristics. The 2N2613 transistor used in the first stage has low noise, low saturation current, wide frequency response, and high gain. The 2N591 transistor used in the second stage has excellent linearity and better-than-average noise characteristics. The operating points selected for these stages provide both low noise performance and an adequate dynamic range.

Both tone controls in the pre-

amplifier provide full-range boost and cut functions; interaction is negligible. Distortion is low for any tone-control setting. The collector-to-base feedback in the third and fourth stages works with the tone controls to provide the over-all tonal response of the preamplifier. The 2N408 stages amplify the signal to the input level required by most transistor audio power amplifiers. For a given input level, the output response of the preamplifier (with controls flat) is constant within ± 1 dB from 10 to 20,000 Hz.

The dc power for the preamplifier may be obtained from the power supply for the audio amplifier. If necessary, a voltage-dropping resistor should be used to reduce the supply voltage to the -18 to -22 volts required for the preamplifier stages.

Performance Characteristics

Sensitivity (at full volume):

Tape input = 1-mV rms input for 42-mV output at 1000 Hz

FM (flat) input = 100-mV rms input for 42-mV output at 1000 Hz

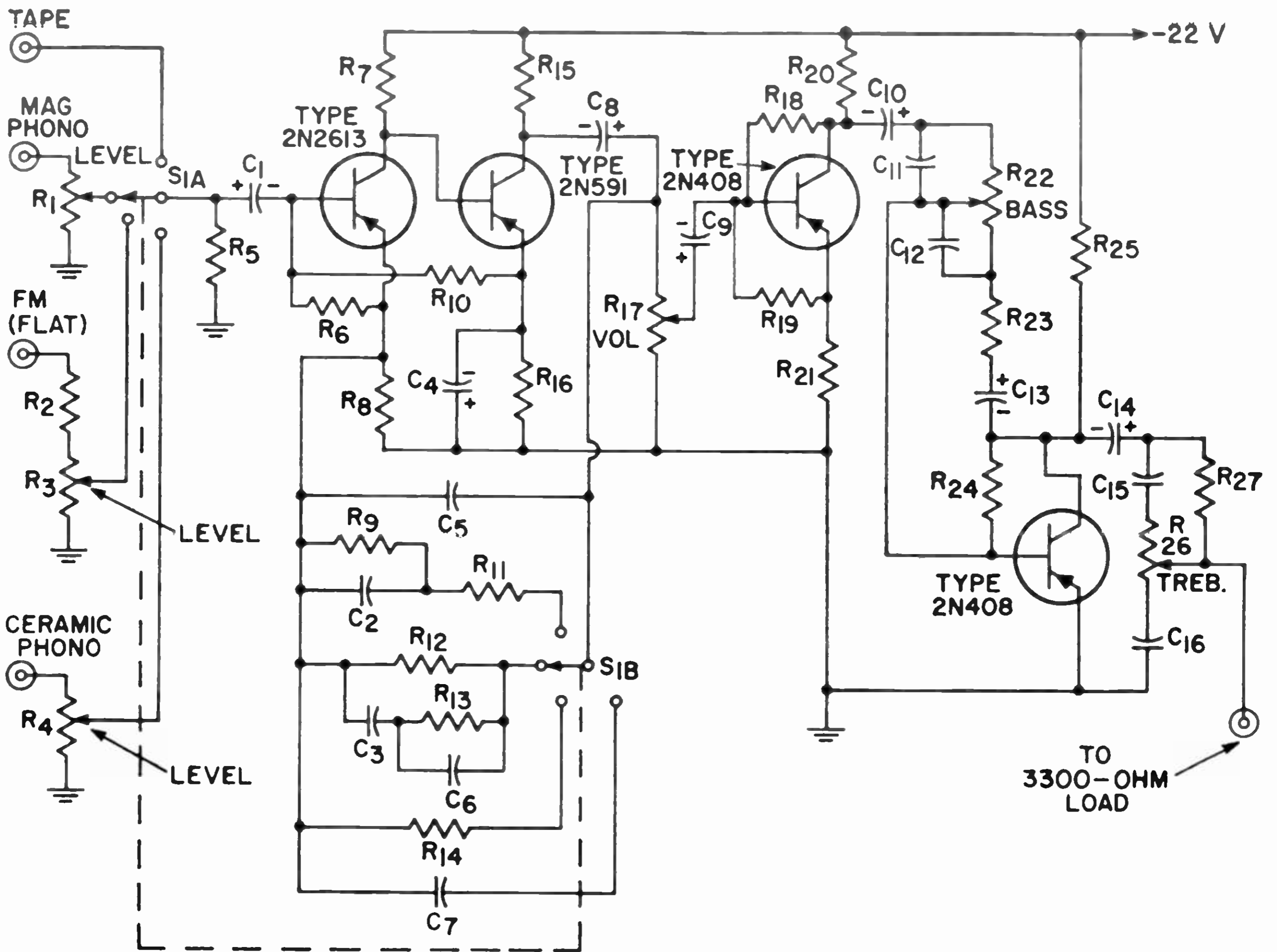
Magnetic-phono input = 2-mV rms input for 42-mV output at 1000 Hz

Ceramic-phono input = 100-mV rms input fed in through 1000 pF

(equivalent capacitance of crystal cartridge) for 42-mV output at 1000 Hz

14-12

HIGH-QUALITY PREAMPLIFIER (cont'd)



Parts List

- | | | |
|--|--|--|
| $C_1 = 25 \mu\text{F}$, electrolytic, 3 V | $R_1 =$ level control, potentiometer, 50000 ohms, 0.5 watt | $R_{11} = 1000$ ohms, 0.5 watt |
| $C_2 = 0.06 \mu\text{F} \pm 5\%$, ceramic, 50 V | $R_2 = 51000$ ohms, 0.5 watt | $R_{15} = 1800$ ohms, 0.5 watt |
| $C_3 = 0.2 \mu\text{F} \pm 5\%$, ceramic, 25 V | $R_3 =$ level control, potentiometer, 1000 ohms, 0.5 watt | $R_{16} = 330$ ohms, 0.5 watt |
| $C_4 = 50 \mu\text{F}$, electrolytic, 3 V | $R_4 =$ level control, potentiometer, 5000 ohms, 0.5 watt | $R_{17} =$ volume control, potentiometer, 10000 ohms, 0.5 watt |
| $C_5 = 270$ pF, ceramic, 600 V | $R_5 = 1$ megohm, 0.5 watt | $R_{18} = 56000$ ohms, 0.5 watt |
| $C_6, C_{16} = 0.05 \mu\text{F} \pm 5\%$, ceramic, 50 V | $R_6 = 15000$ ohms, 0.5 watt | $R_{19} = 6800$ ohms, 0.5 watt |
| $C_7 = 0.25 \mu\text{F}$, ceramic, 50 V | $R_7 = 47000$ ohms, 0.5 watt | $R_{20}, R_{23} = 2700$ ohms, 0.5 watt |
| $C_8 = 25 \mu\text{F}$, electrolytic, 15 V | $R_8 = 100$ ohms, 0.5 watt | $R_{21} = 180$ ohms, 0.5 watt |
| $C_9 = 2 \mu\text{F}$, electrolytic, 3 V | $R_9 = 0.1$ megohm $\pm 5\%$, 0.5 watt | $R_{22} =$ bass control, potentiometer, 50000 ohms, 0.5 watt |
| $C_{10}, C_{11} = 2 \mu\text{F}$, electrolytic, 10 V | $R_{10} = 0.18$ megohm, 0.5 watt | $R_{25} = 0.1$ megohm, 0.5 watt |
| $C_{12} = 0.15 \mu\text{F} \pm 5\%$, ceramic, 50 V | $R_{11} = 820$ ohms $\pm 5\%$, 0.5 watt | $R_{26} = 3300$ ohms, 0.5 watt |
| $C_{13} = 0.12 \mu\text{F} \pm 5\%$, ceramic, 50 V | $R_{12} = 27000$ ohms $\pm 5\%$, 0.5 watt | $R_{27} =$ treble control, potentiometer, 0.1 megohm, 0.5 watt |
| $C_{14} = 10 \mu\text{F}$, electrolytic, 10 V | $R_{13} = 27000$ ohms $\pm 5\%$, 0.5 watt | $R_{27} = 27000$ ohms, 0.5 watt |
| $C_{15} = 0.003 \mu\text{F} \pm 5\%$, ceramic, 500 V | $R_{14} = 1500$ ohms $\pm 5\%$, 0.5 watt | $S_1 =$ selector switch; rotary type; 2-pole, 3-position |

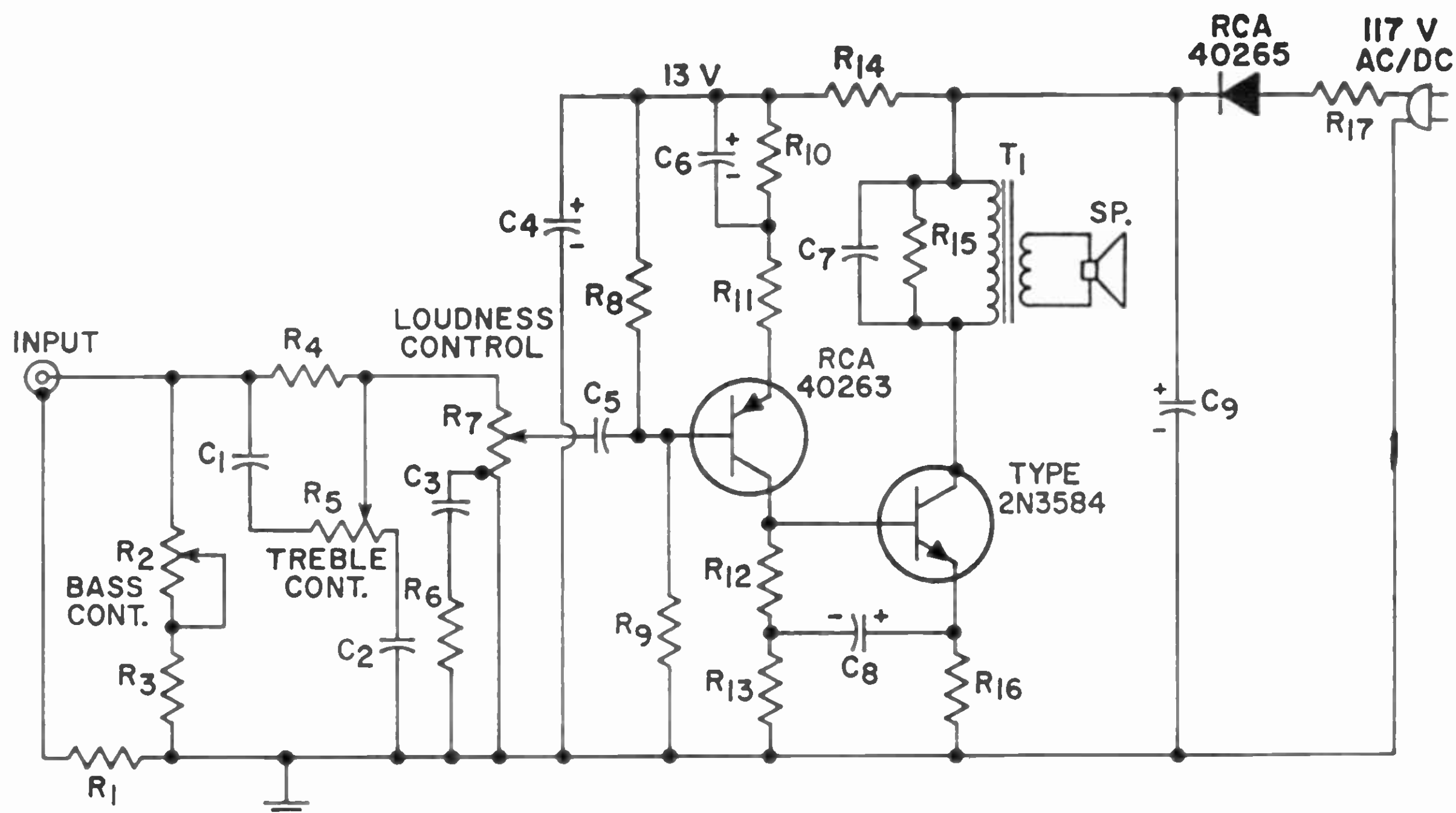
Performance Characteristics (cont'd)

- Overload = more than 30 dB above full-volume input
- Output response (tone controls flat) = ± 1 dB from 10 Hz to 22 kHz
- Tone-control range:
 - Treble (at 20 kHz) = -21 dB cut to +17 dB boost
 - Bass (at 20 Hz) = -25 dB cut to +18 dB boost

14-13

1-WATT AC/DC PHONOGRAPH AMPLIFIER

IHFM Music Power Rating, 2.5 W



NOTE: The 2N3584 transistor must be mounted on an adequate heat sink (see circuit description for details).

Parts List

$C_1, C_2 = 1200$ pF, ceramic disc
 $C_3 = 0.005$ μ F, ceramic disc
 $C_4 = 80$ μ F, electrolytic, 25 V
 $C_5 = 0.1$ μ F, ceramic disc
 $C_6, C_8 = 25$ μ F, electrolytic, 6 V
 $C_7 = 0.01$ μ F, ceramic disc
 $C_9 = 80$ μ F, electrolytic, 150 V
 $R_1 = 56000$ ohms, 0.5 watt
 $R_2 =$ base control, potentiometer, 3 megohms, 0.5 watt, audio taper

$R_3 = 68000$ ohms, 0.5 watt
 $R_4 = 0.33$ megohm, 0.5 watt
 $R_5 =$ treble control, potentiometer, 1 megohm, 0.5 watt, audio taper
 $R_6 = 10000$ ohms, 0.5 watt
 $R_7 =$ loudness control, potentiometer, 2 megohms, tapped at 1 megohm, 0.5 watt, linear taper
 $R_8, R_{11} = 18000$ ohms, 0.5 watt
 $R_9 = 33000$ ohms, 0.5 watt
 $R_{10}, R_{15} = 1000$ ohms, 0.5 watt

$R_{11} = 68$ ohms, 0.5 watt
 $R_{12} = 470$ ohms, 0.5 watt
 $R_{13} = 820$ ohms, 0.5 watt
 $R_{16} = 120$ ohms, 0.5 watt
 $R_{17} = 250$ ohms, 4 watts
 $T_1 =$ audio output transformer; matches collector load impedance of 2500 ohms to speaker voice-coil impedance of 3.2 ohms; Freed No. RCA-8, Triad No. S-12X, or equiv.

Circuit Description

This two-transistor amplifier delivers an rms power output of more than 1 watt to a 4-ohm speaker; its IHFM music power rating is 2.5 watts. The input to the amplifier is obtained from a conventional 0.5-volt, 1000-picofarad ceramic phonograph cartridge; full power output is attained at average record levels for the maximum volume setting. The amplifier incorporates bass and treble tone controls, as well as a tapped loudness control for bass boosting at low volume settings. It has high gain, operates at low noise levels, and provides stable operation at temperatures up to 55°C. The circuit operates directly from either an

ac power line or a dc power supply of 117 volts. AC inputs are converted to dc power by the 40265 half-wave rectifier circuit.

The input stage of the phonograph amplifier consists of a 40263 n-p-n transistor operated in essentially a collector-follower circuit configuration. The signal developed at the collector of the 40263 directly drives the 2N3584 p-n-p transistor used in the output stage. The output stage is basically a common-emitter class A power amplifier that is transformer coupled to the speaker. Output transformer T_1 matches the collector impedance of the output transistor to the speaker.

14-13 1-WATT AC/DC PHONOGRAPH AMPLIFIER (cont'd)

Circuit Description (cont'd)

The phonograph amplifier provides an over-all power gain of 72 dB. The input impedance of the circuit is typically 3000 ohms. An rms input of 3 millivolts, therefore, results in an rms output of 50 milliwatts. An rms input of 16 millivolts is required to obtain the rated output of 1 watt. The stability of the amplifier is excellent, and the sensitivity remains essentially constant at temperatures up to 55°C. The total harmonic distortion is less than 1 per cent for outputs below 50 milliwatts and is approximately 10 per cent for outputs at the 1-watt level. The hum

and noise level is 70 dB below the rated output of 1 watt at the zero volume setting and 58 dB below the rated output at the maximum volume setting. The frequency response of the amplifier is flat within 3 dB from 120 Hz to 7.6 kHz.

The 2N3584 transistor used in the output stage of the phonograph amplifier should be mounted on a suitable heat sink. A vertical heat sink made of 1/16-inch-thick aluminum that provides a total effective cooling-surface area of 28 square inches will provide adequate heat-sink protection.

14-14 9.5-WATT COMPLEMENTARY-SYMMETRY AUDIO POWER AMPLIFIER IHFM Music Power Rating, 19 W

Circuit Description

This 4-stage audio power amplifier delivers 9.5 watts of rms power output to a 8-ohm load impedance with less than 100 millivolts of input signal. Two of these amplifiers can be used in a dual-channel (stereo) system to provide 19 watts of IHFM music power per channel or 38 watts total. The amplifier uses a direct-coupled complementary-symmetry output stage with conventional "bootstrap" drive to provide excellent frequency response. The large amounts of negative feedback employed assure low distortion. The amplifier operates from a dc power supply of 28 volts.

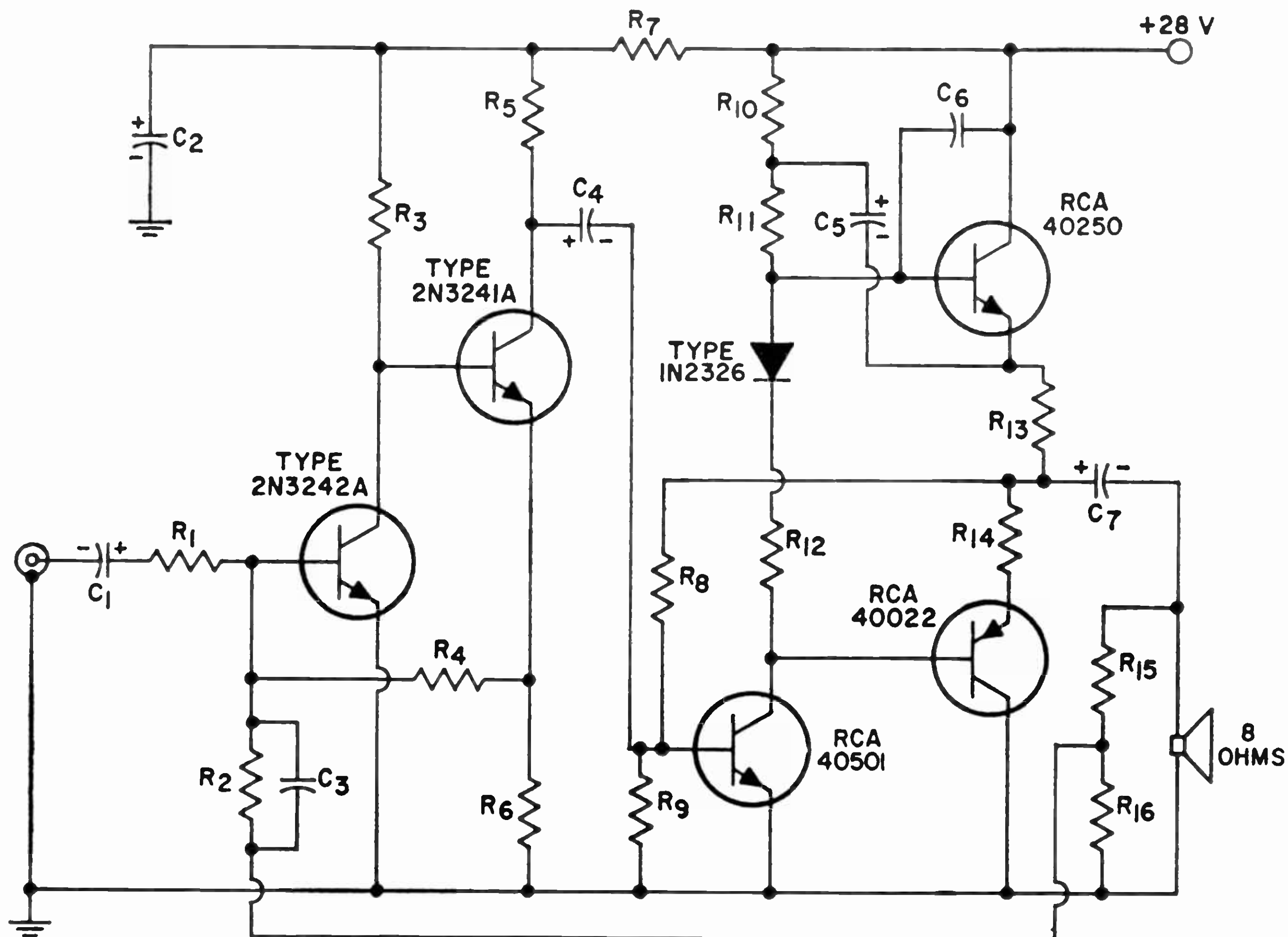
The amplifier employs a 2N3242A transistor in the input stage, a 2N3241A transistor in the predriver stage, a 40501 transistor in the driver stage and a 40022 p-n-p tran-

sistor and a 40250 n-p-n transistor in the complementary-symmetry output stage. The direct-coupled input and predriver stages provide good dc stability and local feedback. The 40501 driver transistor has an integral heat radiator to provide the high dissipation capability that is required. The 1N2326 compensating diode is used to provide thermal stability. This diode, which is thermally connected to the heat sink of the output transistors, must be used if the output stage is to operate reliably at an ambient temperature of 55°C.

The 0.0056-microfarad capacitor C_6 from collector to base of the 40250 transistor reduces the high-frequency response of this n-p-n silicon transistor to approximately that of

14-14

9.5-WATT COMPLEMENTARY-SYMMETRY AUDIO POWER AMPLIFIER (cont'd)



NOTE: The 40022 and 40250 output transistors and the 1N2326 compensating diode should be mounted on a common heat sink that has a thermal resistance of 1.8°C per watt or less. Diode may be attached to heat sink by use of small metal cable clamps.

Parts List

$C_1 = 50 \mu\text{F}$, electrolytic, 15 V
 $C_2, C_4 = 1000 \mu\text{F}$, electrolytic, 25 V
 $C_3 = 18 \text{ pF}$, ceramic
 $C_5 = 100 \mu\text{F}$, electrolytic, 12 V
 $C_6 = 0.0056 \mu\text{F}$, NPO ceramic disc

$C_7 = 500 \mu\text{F}$, electrolytic, 30 V
 $R_1 = 3300 \text{ ohms}$, 0.5 watt
 $R_2, R_7 = 0.1 \text{ megohm}$, 0.5 watt
 $R_3 = 33000 \text{ ohms}$, 0.5 watt
 $R_5 = 680 \text{ ohms}$, 0.5 watt
 $R_6, R_{10}, R_{11} = 120 \text{ ohms}$, 0.5

watt
 $R_7 = 560 \text{ ohms}$, 0.5 watt
 $R_8 = 1800 \text{ ohms}$, 0.5 watt
 $R_9 = 82 \text{ ohms}$, 0.5 watt
 $R_{12} = 5.6 \text{ ohms}$, 0.5 watt
 $R_{13}, R_{14} = 0.68 \text{ ohm}$, 1 watt
 $R_{15} = 820 \text{ ohms}$, 0.5 watt
 $R_{16} = 180 \text{ ohms}$, 0.5 watt

Circuit Description (cont'd)

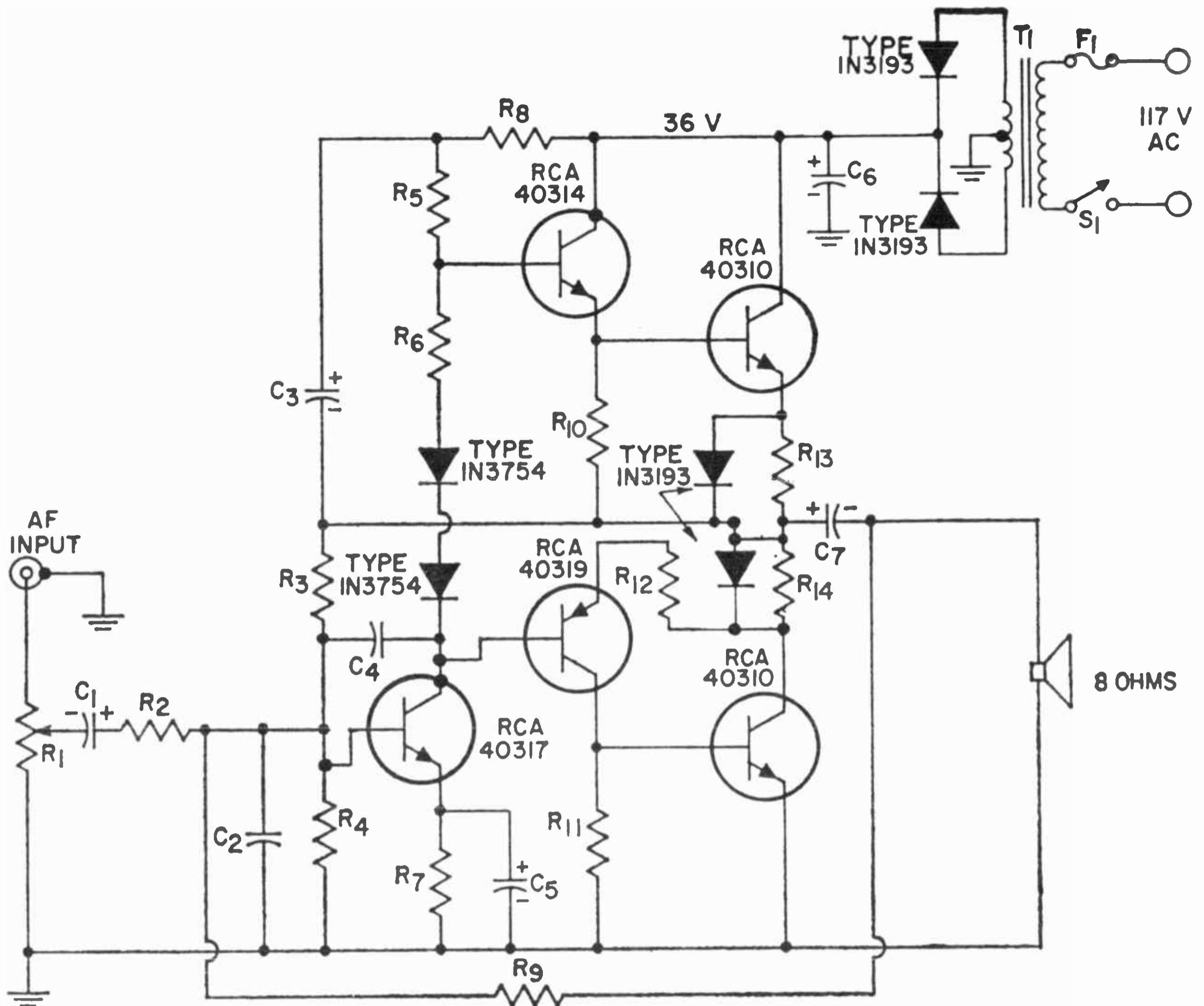
the 40022 p-n-p germanium transistor. Both halves of the output stage thus have substantially the same frequency response characteristics—a feature which simplifies the addition of negative feedback.

The resistor voltage divider across

the speaker terminals provides the proper amount of voltage for the loop feedback network (0.1 megohm and 18 picofarads) and acts as a load impedance, both when the speaker is removed and at high frequencies.

14-15 HIGH-QUALITY 10-WATT QUASI-COMPLEMENTARY-SYMMETRY AUDIO POWER AMPLIFIER

IHFM Music Power Rating, 20 W



NOTE: The 1N3754 diodes in the driver stage are thermally connected (by use of small metal cable clamps) to the heat sink of the 40310 output transistors. For heat sink, use Wakefield No. 400 series or equivalent.

Parts List

$C_1 = 50 \mu\text{F}$, electrolytic, 6 V
 $C_2 = 180 \text{ pF}$, ceramic
 $C_3 = 50 \mu\text{F}$, electrolytic, 25 V
 $C_4 = 68 \text{ pF}$, ceramic
 $C_5 = 100 \mu\text{F}$, electrolytic, 6 V
 $C_6 = 1000 \mu\text{F}$, electrolytic, 50 V
 $C_7 = 1000 \mu\text{F}$, electrolytic, 25 V
 $F_1 = \text{fuse, 1 ampere}$

$R_1 = \text{volume control, potentiometer, 10000 ohms, 0.5 watt (part of assembly with ON-OFF switch } S_1)$
 $R_2 = 3300 \text{ ohms, 0.5 watt}$
 $R_3 = 47000 \text{ ohms, 0.5 watt}$
 $R_4 = 5600 \text{ ohms, 0.5 watt}$
 $R_5 = 4700 \text{ ohms, 0.5 watt}$
 $R_{12} = 4.7 \text{ ohms, 0.5 watt}$
 $R_6, R_{10}, R_{11} = 220 \text{ ohms, 0.5 watt}$
 $R_7 = 270 \text{ ohms, 0.5 watt}$

$R_8 = 1000 \text{ ohms, 0.5 watt}$
 $R_9 = 0.1 \text{ megohm, 0.5 watt}$
 $R_{13}, R_{14} = 1 \text{ ohm, 1 watt}$
 $S_1 = \text{ON-OFF switch (part of assembly with volume-control potentiometer } R_1)$
 $T_1 = \text{power transformer; primary, 117 volts rms; secondary, center-tapped, 28 volts rms from center tap to each end at 500 mA dc; Triwec Transformer Co. No. RCA-111, or equiv.}$

Circuit Description

This high-quality audio power amplifier can supply 10 watts of rms power or 20 watts of IHFM music power to an 8-ohm speaker for an input of 1 volt rms. The amplifier

employs a 40314 n-p-n silicon transistor and a 40319 p-n-p silicon transistor as complementary drivers for the pair of series-connected 40310 n-p-n silicon transistors used in the

14-15 HIGH-QUALITY 10-WATT QUASI-COMPLEMENTARY-SYMMETRY AUDIO POWER AMPLIFIER (cont'd)

Circuit Description (cont'd)

output stage. The absence of both driver and output transformers helps to provide exceptional frequency response at low cost without the hum pick up and feedback problems often encountered in the design of audio power amplifiers.

The use of direct coupling between stages and local dc feedback for each stage makes possible very stable quiescent operation at all temperatures up to 71°C. The use of an over-all negative feedback of 6 dB helps to provide a frequency response that is flat within 3 dB from 15 Hz to 100 kHz. For operation at the rated output, the amplifier provides a total harmonic distortion of less than 0.7 per cent at 1000 Hz. The amplifier provides more than 48 dB of power gain and has a quiescent dissipation of less than 1 watt.

The input stage of the amplifier employs a 40317 n-p-n transistor connected in a class A common-emitter circuit configuration. Negative feedback from collector to base of the transistor stabilizes operation of the input stage.

The amplified signal developed at the collector of the 40317 is directly coupled to the base of the 40319 driver transistor, and the signal at the junction of the collector load resistors R_5 and R_6 is directly coupled to the base of the 40314. Because these driver transistors are connected in complementary symmetry, the outputs developed across resistor

R_{10} and R_{11} are 180 degrees out of phase. The IN3754 diodes connected between the bases of the driver transistors are used to compensate for the effect of temperature variations on the performance of the output transistors.

The 40310 series-connected output transistors are operated in class AB rather than class B to prevent crossover distortion. The drive input from the 40314 driver transistor is applied between the emitter and base terminals of its output transistor so that this output transistor is effectively operated in a common-emitter configuration. As a result, both output transistors provide equal voltage gain. The small amount of degenerative feedback developed across resistors R_{13} and R_{14} helps to stabilize the output stage. The limiting action of the 1N3193 diodes connected in shunt with these resistors prevents excessive power losses across them when the amplifier is operated to provide the full rated output of 10 watts.

This audio power amplifier operates from a 117-volt, 60-c/s ac power input. The input is coupled by power transformer T_1 to a conventional full-wave rectifier using two 1N3193 diodes. The rectifier provides a 36-volt dc output for use as the collector supply voltage for the amplifier. This rectifier circuit can provide the dc power requirements for both channels of a stereo system that uses the 10-watt amplifier.

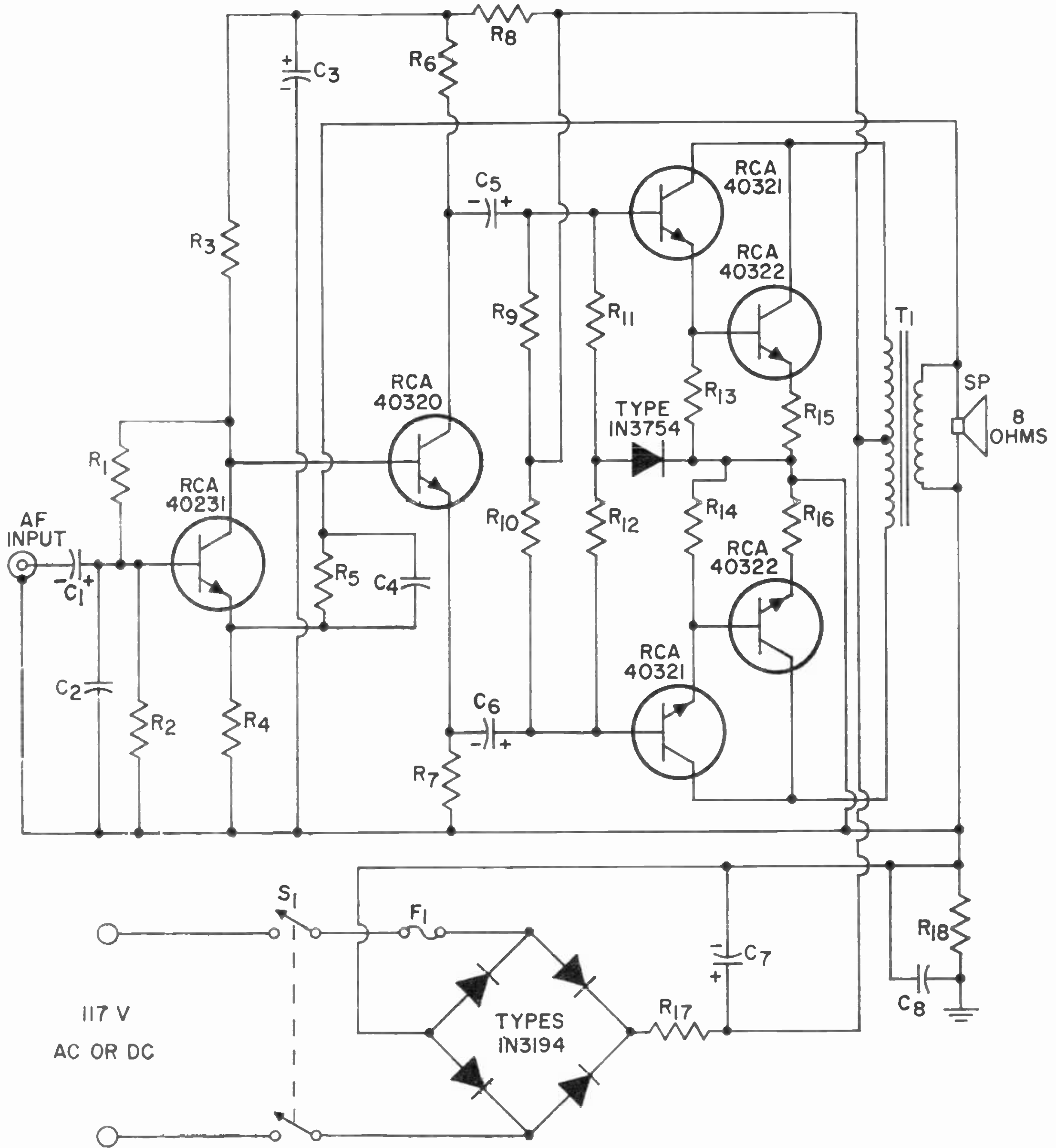
14-16 25-WATT AC/DC AUDIO POWER AMPLIFIER

Circuit Description

This amplifier is intended primarily for use in public-address systems and other audio applications in which flexibility with respect to

load impedance is important. The amplifier provides more than 60 dB of power gain and has a flat frequency response from 35 to 15,000

14-16 25-WATT AC/DC AUDIO POWER AMPLIFIER (cont'd)



Parts List

- | | | |
|--|---|--|
| C ₁ = 1 μF, electrolytic, 3 V | R ₁ = 15000 ohms, 0.5 watt | 0.5 watt |
| C ₂ = 0.02 μF, ceramic disc | R ₂ = 3000 ohms, 0.5 watt | R ₁₅ , R ₁₆ = 5 ohms, 5 watts |
| C ₃ = 250 μF, electrolytic, 25 V | R ₃ = 2200 ohms, 0.5 watt | R ₁₇ = 10 ohms, 20 watts |
| C ₄ = 0.002 μF, ceramic disc | R ₄ = 51 ohms, 0.5 watt | R ₁₈ = 0.22 megohm, 0.5 watt |
| C ₅ , C ₆ = 2 μF, electrolytic, 25 V | R ₅ = 5100 ohms, 0.5 watt | S ₁ = ON-OFF switch, double-pole, single-throw |
| C ₇ = 250 μF, electrolytic, 150 V | R ₆ , R ₇ = 300 ohms, 0.5 watt | T ₁ = audio output transformer; primary, 600 ohms, center tapped; secondary, 8 ohms |
| C ₈ = 0.1 μF, ceramic disc | R ₈ = 4000 ohms, 5 watts | |
| F ₁ = fuse, 1.5-ampere | R ₉ , R ₁₀ = 0.18 megohm, 0.5 watt | |
| | R ₁₁ , R ₁₂ , R ₁₃ , R ₁₄ = 510 ohms, | |

Circuit Description (cont'd)

Hz. Total harmonic distortion at the rated output is less than 1 per cent, and the hum and noise level is 63 dB below the output for operation at the

rated power level. The high breakdown voltage of the silicon transistors used in the output and driver stages permits the amplifier to be

14-16 25-WATT AC/DC AUDIO POWER AMPLIFIER (cont'd)**Circuit Description (cont'd)**

operated directly from either an ac power line or a dc supply of 117 volts. AC inputs are converted to a smooth dc supply voltage by four 1N3194 diodes in a full-wave bridge rectifier, together with a simple RC filter network R_{17} and C_7 . This power supply circuit is common to both channels of a stereo system that uses the 25-watt amplifier.

The input stage of the amplifier uses a 40231 transistor in a class A common-emitter configuration. This configuration, together with negative feedback of approximately 10 dB from the output (speaker terminal) to the emitter of the 40231, results in an amplifier input impedance of 2500 ohms. The amplified signal at the collector of the input transistor is directly coupled to the base of a 40320 transistor used in a simple phase-splitter circuit to develop the out-of-phase signals required to drive the push-pull output stage. Because the collector and emitter load resistors in the phase-splitter stage are of equal value, the signals developed at the emitter and collector of the 40320 are equal

in amplitude but 180 degrees out of phase. These signals are capacitively coupled to the bases of the 40321 driver transistors.

The driver transistors are connected to the 40322 high-voltage output transistors in a Darlington configuration which provides the high power gain required to develop the desired power output from the signals supplied from the phase-splitter. Resistors R_9 , R_{10} , R_{11} , and R_{12} and the 1N3754 diode bias the driver and output stages for class AB operation. These stages are operated in class AB rather than class B to minimize cross-over distortion. The 1N3754 diode also provides the temperature compensation required to maintain a relatively constant quiescent current with small changes in temperature or line voltage. At the rated output, the dissipation in each output transistor is less than 15 watts at room temperature; therefore, the amplifier can be operated at temperatures up to 70°C without transistor derating.

14-17 HIGH-FIDELITY 25-WATT QUASI-COMPLEMENTARY-SYMMETRY AUDIO POWER AMPLIFIER
IHF M Music Power Rating, 38 W

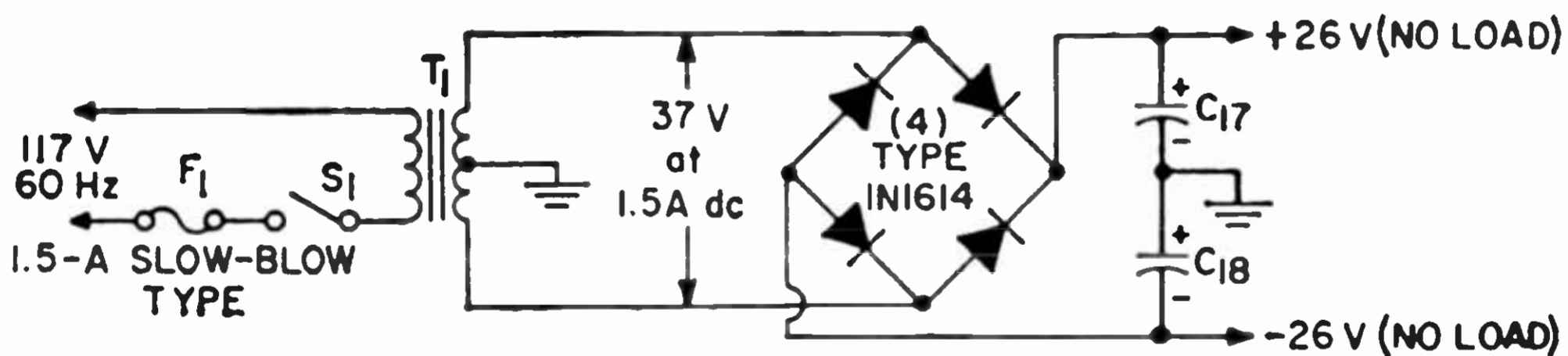
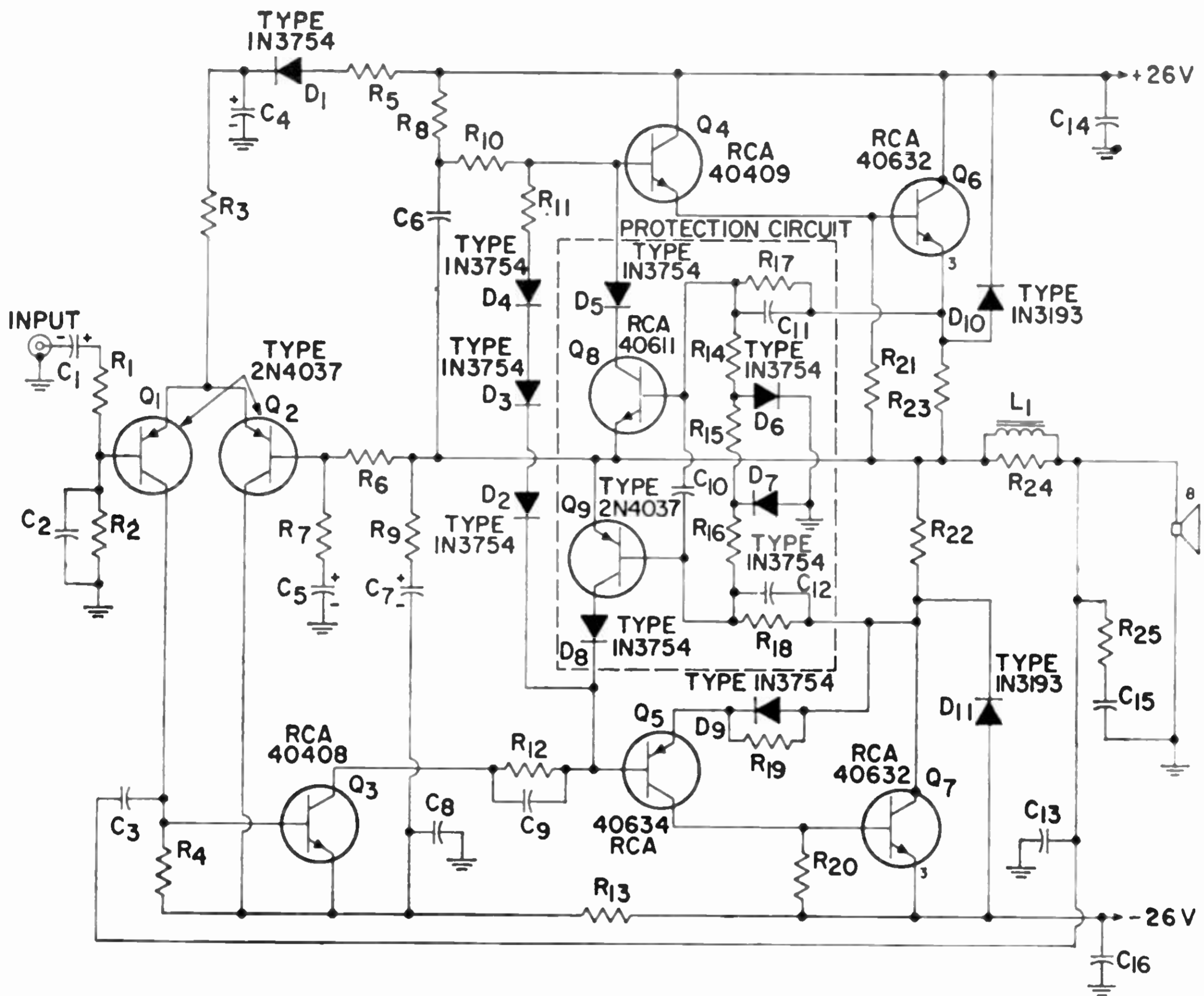
Circuit Description

This high-fidelity amplifier provides 25 watts of rms power output (38 watts of IHF M music power output) for an input of 0.6 volt rms. The amplifier has a frequency response that is flat within 1 dB from 10 to 50,000 Hz. Total harmonic distortion at the full rated output of 25 watts is less than 1 per cent at 1000 Hz. The amplifier requires no driver or output transformer and has built-in safe-area limiting protection that prevents damage to the driver and output stages from high currents and excessive power dissipation.

The input stage uses two 2N4037 p-n-p transistors (Q_1 and Q_2) in a differential amplifier circuit. These transistors are matched for V_{BE} characteristics to give a minimum offset voltage between their bases and, therefore, between input and output. The action of the feedback loop is to amplify negatively (i.e., in opposite phase) any voltage difference that develops between input and output, and, in this way, to cause the output voltage to follow the input voltage.

The predriver stage employs a 40408 n-p-n transistor (Q_3) in a

14-17 HIGH-FIDELITY 25-WATT QUASI-COMPLEMENTARY-SYMMETRY AUDIO POWER AMPLIFIER (cont'd)



NOTES: (1) Output transistors Q₆ and Q₇ and diodes D₂ through D₄ should be mounted on a common heat sink (Wakefield Type NC-403K or equiv.). Diodes should be attached to under side of heat sink by use of small metal cable clamps. (2) Transistors Q₁ and Q₂ should be matched for base-to-emitter voltage within 0.04 volt and should be selected for a beta between 100 and 300 at 1 milliamper and 5 volts.

Parts List

- | | | |
|---|--|--|
| C ₁ = 5 μF, electrolytic, 12 V | F ₁ = fuse, 1.5-ampere, slow-blow | R ₁₁ , R ₁₆ = 1000 ohms, 0.5 watt |
| C ₂ = 180 pF, ceramic, 50 V | L ₁ = 10 μH, Miller 4622 or equiv. | R ₁₅ = 4700 ohms, 0.5 watt |
| C ₃ = 39 pF, ceramic, 50 V | R ₁ , R ₈ = 1800 ohms, 0.5 watt | R ₁₇ , R ₁₈ = 68 ohms, 0.5 watt |
| C ₄ , C ₇ = 50 μF, electrolytic, 50 V | R ₂ , R ₆ = 18000 ohms, 0.5 watt | R ₂₂ , R ₂₃ = 0.43 ohms, 5 watts |
| C ₅ = 50 μF, electrolytic, 12 V | R ₃ = 12000 ohms, 0.5 watt | R ₂₄ , R ₂₅ = 22 ohms, 0.5 watt |
| C ₆ = 50 μF, ceramic, 50 V | R ₄ , R ₇ = 680 ohms, 0.5 watt | S ₁ = ON-OFF switch, single-pole, single-throw |
| C ₈ , C ₉ , C ₁₅ = 0.02 μF, ceramic, 50 V | R ₅ = 180 ohms, 0.5 watt | T ₁ = power transformer; primary 117 volts; secondary, center-tapped, 37 volts at 1.5 amperes; Triwec Transformer Co. No. RCA-120 or equiv. |
| C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄ , C ₁₆ = 0.5 μF, ceramic, 50 V | R ₉ , R ₁₂ = 270 ohms, 0.5 watt | |
| C ₁₇ , C ₁₈ = 2100 μF, electrolytic, 35 V | R ₁₀ = 2200 ohms, 0.5 watt | |
| | R ₁₁ = 47 ohms, 0.5 watt | |
| | R ₁₃ , R ₁₉ , R ₂₀ , R ₂₁ = 100 ohms, 0.5 watt | |

14-17 HIGH-FIDELITY 25-WATT QUASI-COMPLEMENTARY-SYMMETRY AUDIO POWER AMPLIFIER (cont'd)

Circuit Description (cont'd)

common-emitter circuit. This circuit has a minimum loading effect on the input stage and provides the necessary voltage amplification for the entire amplifier. The subsequent stages provide the required current gain.

The driver stage uses a 40409 n-p-n transistor (Q_1) and a 40634 p-n-p transistor (Q_5) connected in complementary symmetry to develop push-pull drive for the output stage. Two 40632 silicon power transistors (Q_6 and Q_7) used in the output stage are connected in series with separate positive and negative supply voltages. The output is directly coupled to an 8-ohm speaker from the common point between the two transistors. Negative feedback of 35 dB is provided by R_6 , R_7 and C_5 . Feedback stabilization and proper frequency response are provided by the reactive elements C_5 , C_{15} and L_1 .

Bias voltage for the complementary driver stages is provided by the forward voltage drop across the three 1N3754 diodes (D_2 , D_3 , and D_4) and resistor R_{11} . This voltage is necessary to maintain the output stages in class AB operation to avoid cross-over distortion. The 1N3754 diodes are connected thermally to the heat sink of the output transistors to provide the necessary thermal feedback to stabilize the quiescent current at its preset value at all case temperatures up to 100°C. Because of the high-temperature compensation provided by this thermal feedback network, the required stability in the output stages can be provided by small emitter resistors (R_{22} and R_{23}) and losses are held to a minimum. (The Q_5 - Q_7 pair operates like a large p-n-p transistor whose "emitter" is the collector of Q_7 . Resistor R_{22} , therefore, is in the "effective emitter" of the pair.)

Safe-area limiting is provided by a current-limiting circuit whose prin-

cipal components are the emitter resistors R_{22} and R_{23} and the 2N4037 p-n-p transistor Q_9 and 40611 n-p-n transistor Q_8 connected to them, respectively. If any condition exists which causes an excessive current to flow through either resistor, the resultant voltage developed across the resistor will turn on its corresponding protection transistor, removing the excessive base drive current from the appropriate driver transistor (Q_1 or Q_5). The value of current that is "excessive" depends on the output voltage. At an output voltage near ground (such as would be encountered with a short circuit) essentially the full voltage across the emitter resistor is applied across the base-emitter terminals of the protection transistor, which then turns on at a particular value of output current. When the output voltage is well above from ground, however, (as in the peaks in a normal operating situation) the emitter-to-ground voltage is applied to the network in the protection circuit and a voltage drop is developed across resistor R_{17} or R_{18} . As a result, the full voltage across the emitter resistor is not applied to the protection transistor, and a larger output current that produces a larger voltage drop must occur before limiting takes place. Because the power dissipation of a transistor is the product of the voltage across it and the current through it, high currents may be tolerated at low values of voltage across the transistor (i.e., high values of output voltage, because the sum of output voltage and transistor voltage is equal to the supply voltage). Both the driver and output transistors, therefore, are protected from any excessive power dissipation, whether by a short circuit or with a normal load.

Further safe-area limiting is provided by the 1N3193 diodes D_{10} and D_{13} placed across the output transis-

14-17 HIGH-FIDELITY 25-WATT QUASI-COMPLEMENTARY-SYMMETRY AUDIO POWER AMPLIFIER (cont'd)

Circuit Description (cont'd)

tors. These diodes guard against damage due to a highly inductive load by providing a path to return the energy from the inductor to the power supply when the load voltage and load current differ in sign. This energy must find a return path in any case. If the diodes are not present, the energy will flow through the output transistor in the reverse direction from normal current flow, and possibly cause breakdown.

The amplifier operates from a full-wave bridge power supply which provides symmetrical positive and negative dc outputs of 26 volts. This power supply may be used for both channels of a stereo system.

Performance Characteristics

(Measured at a line voltage of 120V, an ambient temperature of 25°C, and a frequency of 1 kHz, unless otherwise specified.)

Power Output (8-ohm load)	
Music (at 5% THD, regulated supply)	38W
Dynamic (at 1% THD, regulated supply)	33W
Continuous (at 1% THD, unregulated supply)	25W
Sensitivity (For continuous power output rating):	600 mV
Hum and Noise (below continuous power output):	
Input shorted	80 dB
Input open	75 dB
Input Resistance	20,000 ohms
Intermodulation Distortion [10 dB below continuous power output at 60 Hz and 7 kHz (4:1)]	0.1%

14-18 HIGH-FIDELITY 40-WATT QUASI-COMPLEMENTARY-SYMMETRY AUDIO POWER AMPLIFIER IHF M Music Power Rating, 55 W

Circuit Description

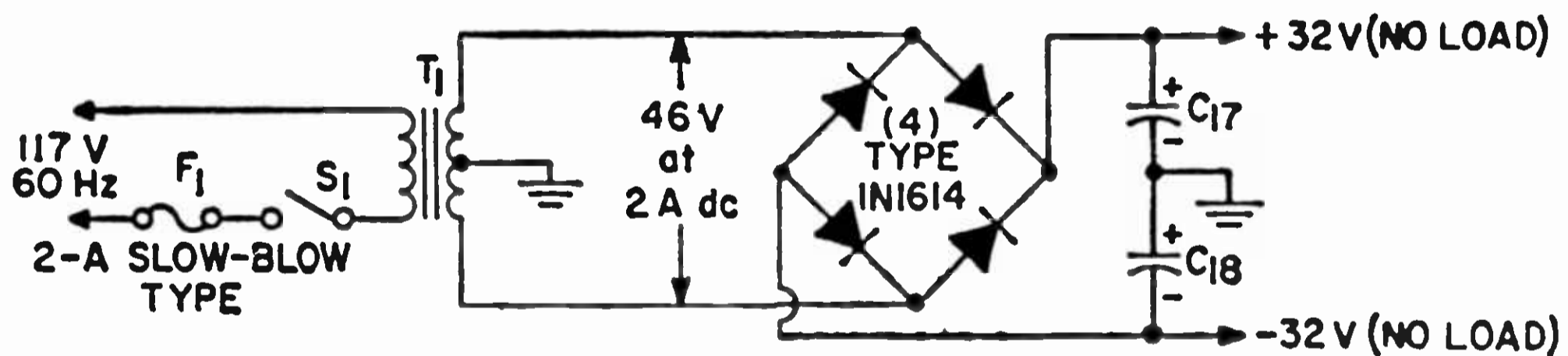
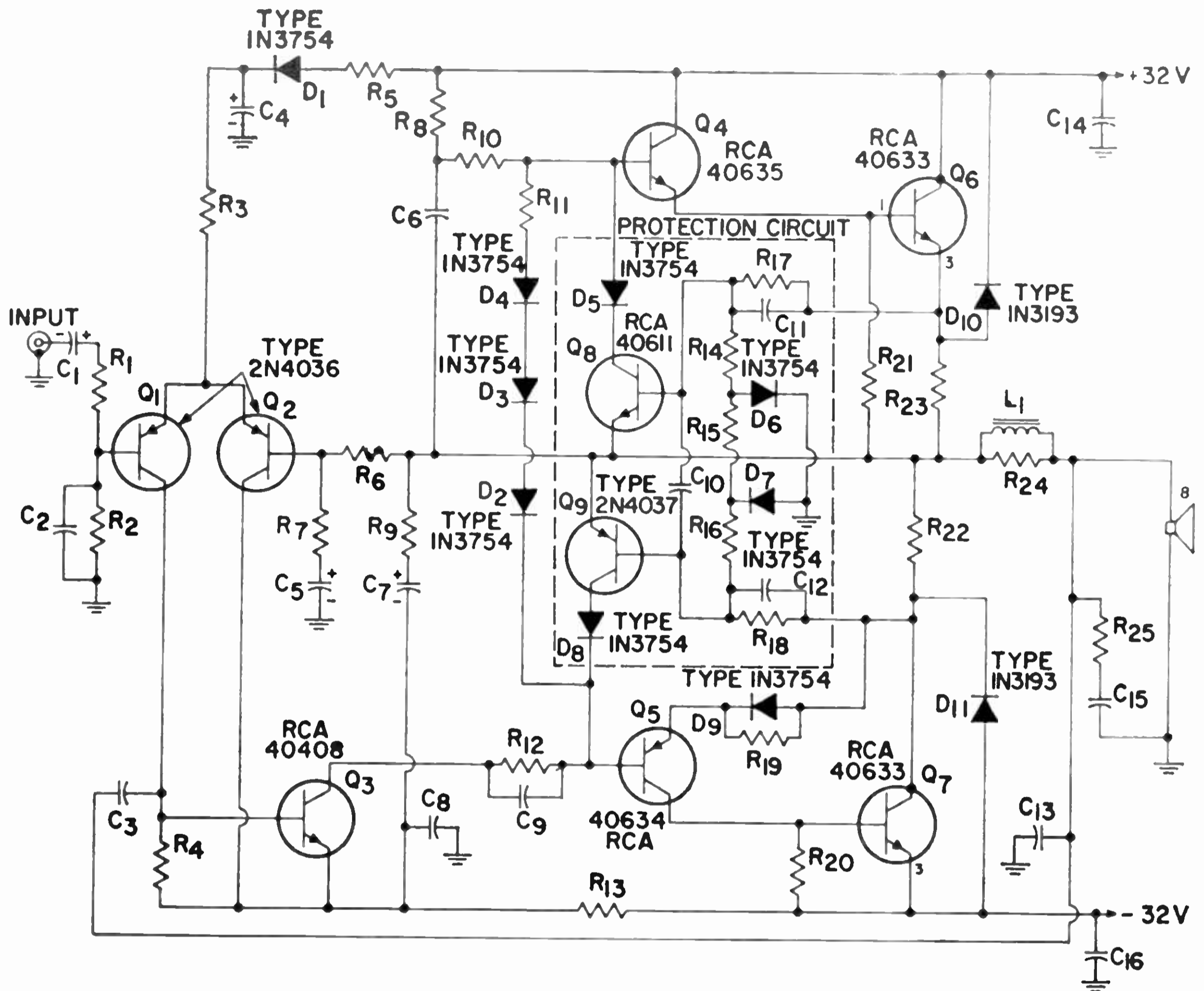
This high-fidelity audio power amplifier can deliver 40 watts of rms power output (55 watts of IHF M music power output) for an input of 0.6 volt rms. The frequency response of the amplifier is flat within 1 dB from 10 to 50,000 Hz. Total harmonic distortion at the full rated output of 40 watts is less than 1 per cent at 1000 Hz. Although component values, the transistor complement, and supply voltages differ, the circuit configuration of this amplifier is the same as that of the 25-watt amplifier in circuit 14-17, and the operation of the two amplifiers is identical.

Performance Characteristics

(Measured at a line voltage of 120V, an ambient temperature of 25°C, and a frequency of 1 kHz, unless otherwise specified.)

Power Output (8-ohm load)	
Music (at 5% THD, regulated supply)	55W
Dynamic (at 1% THD, regulated supply)	50W
Continuous (at 1% THD, unregulated supply)	40W
Sensitivity for continuous power output rating	600 mV
Hum and Noise:	
Below continuous power output:	
Input shorted	80 dB
Input open	75 dB
Input Resistance	20,000 ohms
Intermodulation Distortion [10 dB below continuous power output at 60 Hz and 7 kHz (4:1)]	0.1%

14-18 HIGH-FIDELITY 40-WATT QUASI-COMPLEMENTARY-SYMMETRY AUDIO POWER AMPLIFIER (cont'd)



NOTE: (1) Output transistors Q_6 and Q_7 and diodes D_2 through D_4 should be mounted on a common heat sink (Wakefield Type NC403K or equiv.). Diodes should be attached to under side of heat sink by use of small metal cable clamps. (2) Transistors Q_1 and Q_2 should be matched for base-to-emitter voltage within 0.04 volt and should be selected for a beta between 100 and 300 at 1 millampere and 5 volts.

Parts List

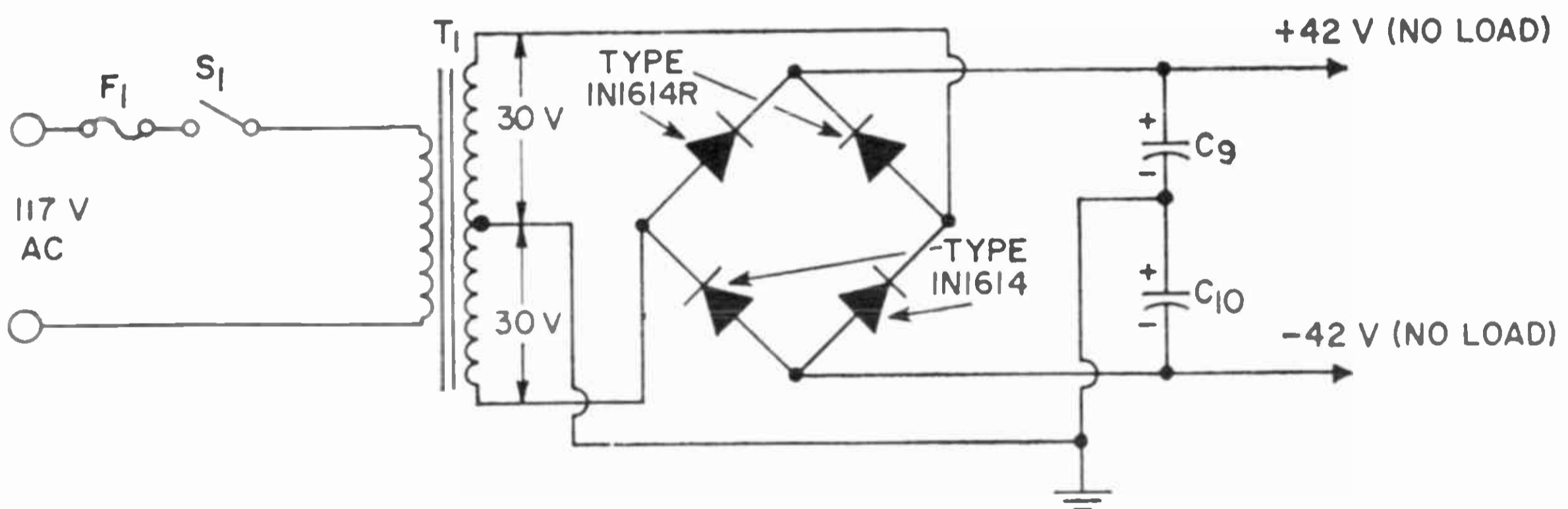
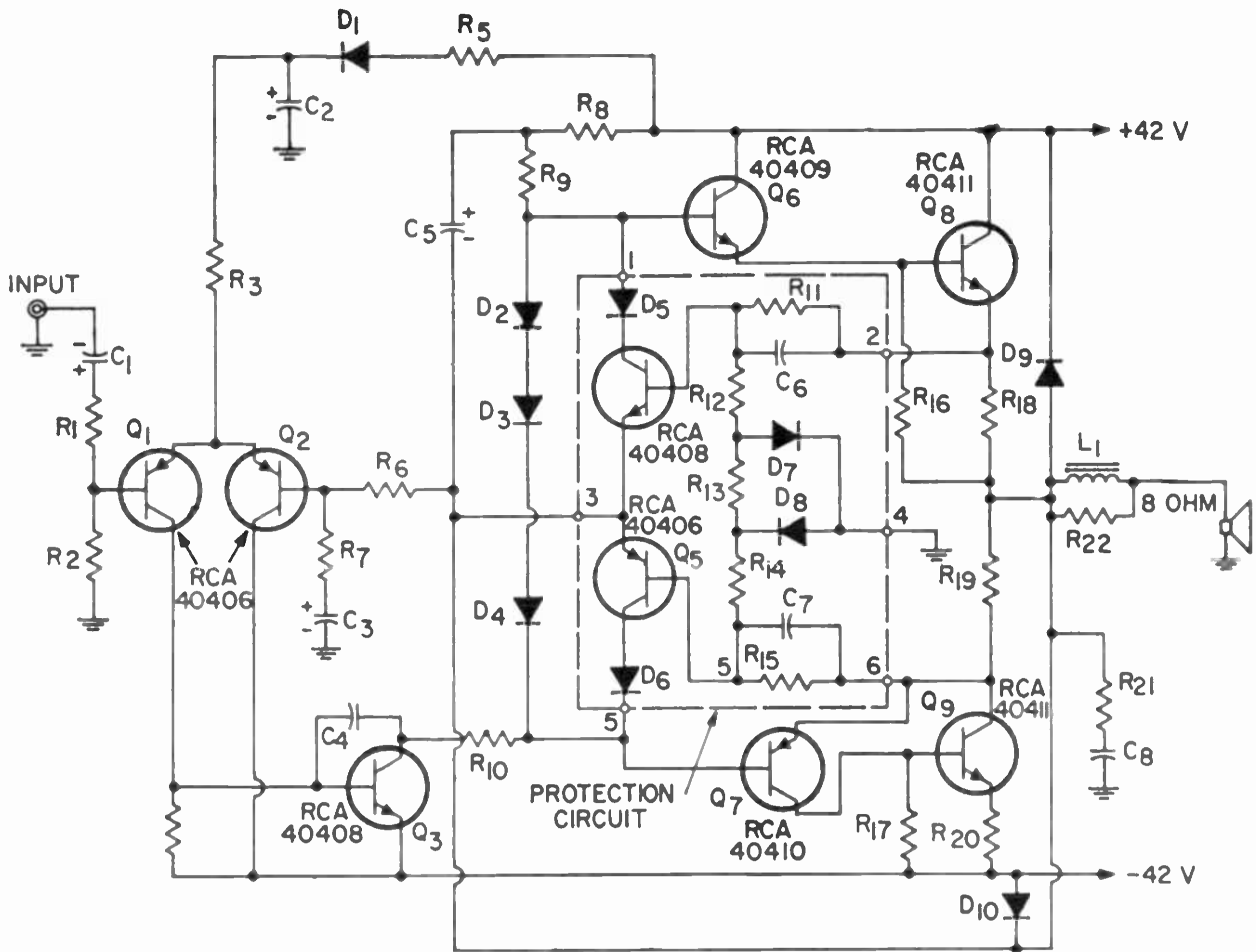
$C_1 = 5 \mu\text{F}$, electrolytic, 12 V
 $C_2 = 180 \text{ pF}$, ceramic, 50 V
 $C_3 = 39 \text{ pF}$, ceramic, 50 V
 $C_4, C_7 = 50 \mu\text{F}$, electrolytic, 50 V
 $C_5 = 50 \mu\text{F}$, electrolytic, 12 V
 $C_6 = 50 \mu\text{F}$, ceramic, 50 V
 $C_8, C_9, C_{15} = 0.02 \mu\text{F}$, ceramic, 50 V
 $C_{10}, C_{11}, C_{12}, C_{13}, C_{14}, C_{16} = 0.05 \mu\text{F}$, ceramic, 50 V
 $C_{17}, C_{18} = 3500 \mu\text{F}$, electrolytic, 50 V
 $F_1 = \text{fuse, 2-ampere, slow-blow}$

$L_1 = 10 \mu\text{H}$, Miller 4622 or equiv.
 $R_1 = 1800 \text{ ohms}$, 0.5 watt
 $R_2, R_3 = 18000 \text{ ohms}$, 0.5 watt
 $R_4 = 15000 \text{ ohms}$, 0.5 watt
 $R_5 = 680 \text{ ohms}$, 0.5 watt
 $R_6 = 180 \text{ ohms}$, 0.5 watt
 $R_7 = 560 \text{ ohms}$, 0.5 watt
 $R_8 = 2200 \text{ ohms}$, 0.5 watt
 $R_9 = 270 \text{ ohms}$, 0.5 watt
 $R_{10} = 2700 \text{ ohms}$, 0.5 watt
 $R_{11} = 47 \text{ ohms}$, 0.5 watt
 $R_{12} = 390 \text{ ohms}$, 0.5 watt
 $R_{13}, R_{19}, R_{20}, R_{21} = 100 \text{ ohms}$, 0.5 watt

$R_{11}, R_{16} = 1000 \text{ ohms}$, 0.5 watt
 $R_{15} = 4700 \text{ ohms}$, 0.5 watt
 $R_{17}, R_{18} = 68 \text{ ohms}$, 0.5 watt
 $R_{22}, R_{23} = 0.39 \text{ ohm}$, 5 watts
 $R_{24}, R_{25} = 22 \text{ ohms}$, 0.5 watt
 $S_1 = \text{ON-OFF switch, single-pole, single-throw}$
 $T_1 = \text{power transformer; primary 117 volts; secondary, center-tapped, 46 volts at 2 amperes; Triwec Transformer Co. No. RCA-119 or equiv.}$

14-19 HIGH-FIDELITY 70-WATT QUASI-COMPLEMENTARY-SYMMETRY AUDIO POWER AMPLIFIER (cont'd)

IHFM Music Power Rating, 100 W



NOTES: (1) Output transistors Q_4 and Q_6 and diodes D_2 through D_4 should be mounted on a common heat sink (Wakefield Type NC-403K or equiv.). Diodes should be attached to under side of heat sink by use of small metal cable clamps. (2) Transistors Q_1 and Q_2 should be matched for base-to-emitter voltage within 0.4 volt and should be selected for a beta between 100 and 300 at 1 milliamperes and 5 volts.

Parts List

$C_1 = 10 \mu\text{F}$, electrolytic, 6 V
 $C_2, C_5 = 100 \mu\text{F}$, electrolytic, 50 V
 $C_3 = 100 \mu\text{F}$, electrolytic, 12 V
 $C_4 = 47 \text{ pF}$, ceramic
 $C_6, C_7 = 0.05 \mu\text{F}$, ceramic
 $C_8 = 0.1 \mu\text{F}$, ceramic
 $C_9, C_{10} = 3000 \mu\text{F}$, electrolytic, 75 V
 $L_1 = 10 \mu\text{H}$, J. W. Miller No. 4622 or equiv.
 $R_1, R_{12}, R_{13}, R_{14} = 1000$

ohms, 0.5 watt
 $R_2, R_6 = 10000$ ohms, 0.5 watt
 $R_3 = 18000$ ohms, 0.5 watt
 $R_4 = 680$ ohms, 0.5 watt
 $R_5, R_{10}, R_{16}, R_{17} = 1000$ ohms, 0.5 watt
 $R_7 = 330$ ohms, 0.5 watt
 $R_8 = 3900$ ohms, 0.5 watt
 $R_9 = 5600$ ohms, 0.5 watt
 $R_{11}, R_{15} = 68$ ohms, 0.5 watt
 $R_{18}, R_{19}, R_{20} = 0.33$ ohm, 5 watts

$R_{21} = 22$ ohms, 2 watts
 $R_{22} = 22$ ohms, 0.5 watt
 $S_1 = \text{ON-OFF}$ switch, single-pole, single throw
 $T_1 = \text{power transformer}$; primary, 117 volts rms; secondary, center-tapped, 30 volts rms from center tap to each end (with no external load on power supply); Triwec Transformer Co. No. RCA-113 or equiv.

14-19 HIGH-FIDELITY 70-WATT QUASI-COMPLEMENTARY-SYMMETRY AUDIO POWER AMPLIFIER (cont'd)
IHFM Music Power Rating, 100 W

Circuit Description

This high-fidelity audio power amplifier provides 70 watts of rms power output (100 watts of IHFM music power output) for an input of 1 volt rms. The frequency response of the amplifier is flat within 1 dB from 5 to 25000 Hz. Total harmonic distortion at the full rated power output of 70 watts is less than 0.25 per cent at 1000 Hz. Although component values, the transistor complement, and supply voltages differ, the basic configuration and the operation of this amplifier are essentially identical to the 25-watt amplifier in circuit 14-17.

Performance Characteristics

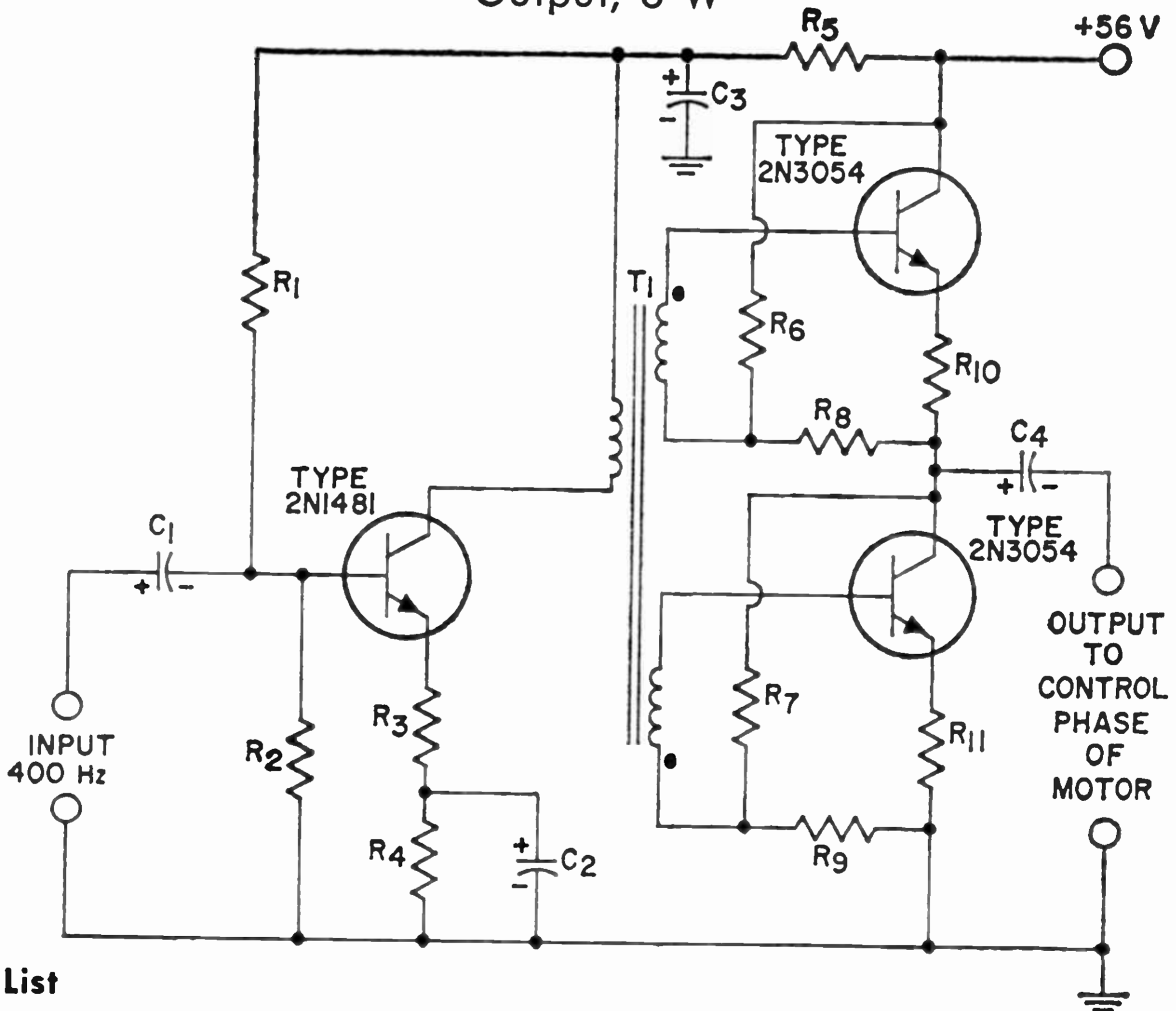
(Measured at a line voltage of 120V, ambient temperature of 25°C, and a frequency of 1 kHz, unless otherwise specified)

Power Output:	
Music (at 5% THD, regulated supply, 8-ohm load)	100W
Dynamic (at 1% THD, regulated supply, 8-ohm load)	88W
Continuous (at 1% THD, unregulated supply, 8-ohm load)	70W
Sensitivity for continuous power output rating	700 mV
Hum and Noise (below continuous power output):	
Input shorted	85 dB
Input open	80 dB
Input Resistance	20,000 ohms
Intermodulation Distortion [10 dB below continuous power output at 60 Hz and 7 kHz (4:1)]	0.1%

14-20

SERVO AMPLIFIER

Output, 6 W



Parts List

- C₁ = 10 μF, electrolytic, 15 V
- C₂ = 47 μF, electrolytic, 15 V
- C₃ = 20 μF, electrolytic, 50 V
- C₄ = 500 μF, electrolytic, 50 V

- R₁ = 68000 ohms, 0.5 watt
- R₂ = 5600 ohms, 0.5 watt
- R₃ = 56 ohms, 0.5 watt
- R₄ = 560 ohms, 0.5 watt
- R₅ = 3300 ohms, 0.5 watt
- R₆, R₇ = 18000 ohms, 0.5 watt
- R₈, R₉ = 400 ohms, 0.5 watt
- R₁₀, R₁₁ = 4 ohms, 1 watt

T₁ = driver transformer; core material 0.014-inch Magnetic Metals Corp. "Crystalligned" or equiv.; primary 1500 turns; secondary 450 turns, bifilar wound (each section 225 turns)

14-20

SERVO AMPLIFIER (cont'd)

Circuit Description

This servo amplifier can supply up to 6 watts of power to the drive motor of a servo system. The amplifier is driven by a 400-Hz ac signal and is operated from a dc supply voltage of 56 volts. A pair of 2N3054 silicon power transistors are used in a class AB, push-pull, single-ended output stage to develop the required output power.

A 2N1481 common-emitter input stage amplifies the 400-Hz input to the level required to drive the 2N3054 output transistors. The amplified 400-Hz signal at the collector of the 2N1481 transistor is coupled to the base of each 2N3054 output transistor by the transformer T_1 . The secondary of T_1 is split to form two identical windings which are oriented so that the inputs to the output transistors are equal in amplitude and 180 degrees out of phase, as required for push-pull drive.

If the input to the upper output transistor were applied between the base and ground, this transistor would be operated as an emitter follower and could not provide voltage gain. The input, however, is applied between the base and the emitter so that, in effect, the upper transistor is operated as a common-emitter amplifier except that there is no phase reversal between input and output. Its gain, therefore, is equal to that of the lower output transistor, which is operated in a conventional common-emitter amplifier configuration. The positive half-cycle of the output signal developed by the upper transistor and the negative half-cycle developed by the lower transistor then have equal voltage swings. This output is coupled to the control-phase winding of the drive motor by the series output capacitor C_1 .

14-21

27-MHz, 5-WATT CITIZENS-BAND TRANSMITTER

Circuit Description

This transmitter operates directly from a 12-volt supply without the need for dc-to-dc converters, and is thus adaptable to mobile operations employing 12-volt systems. Its low power drain also makes it adaptable to portable use with small storage batteries.

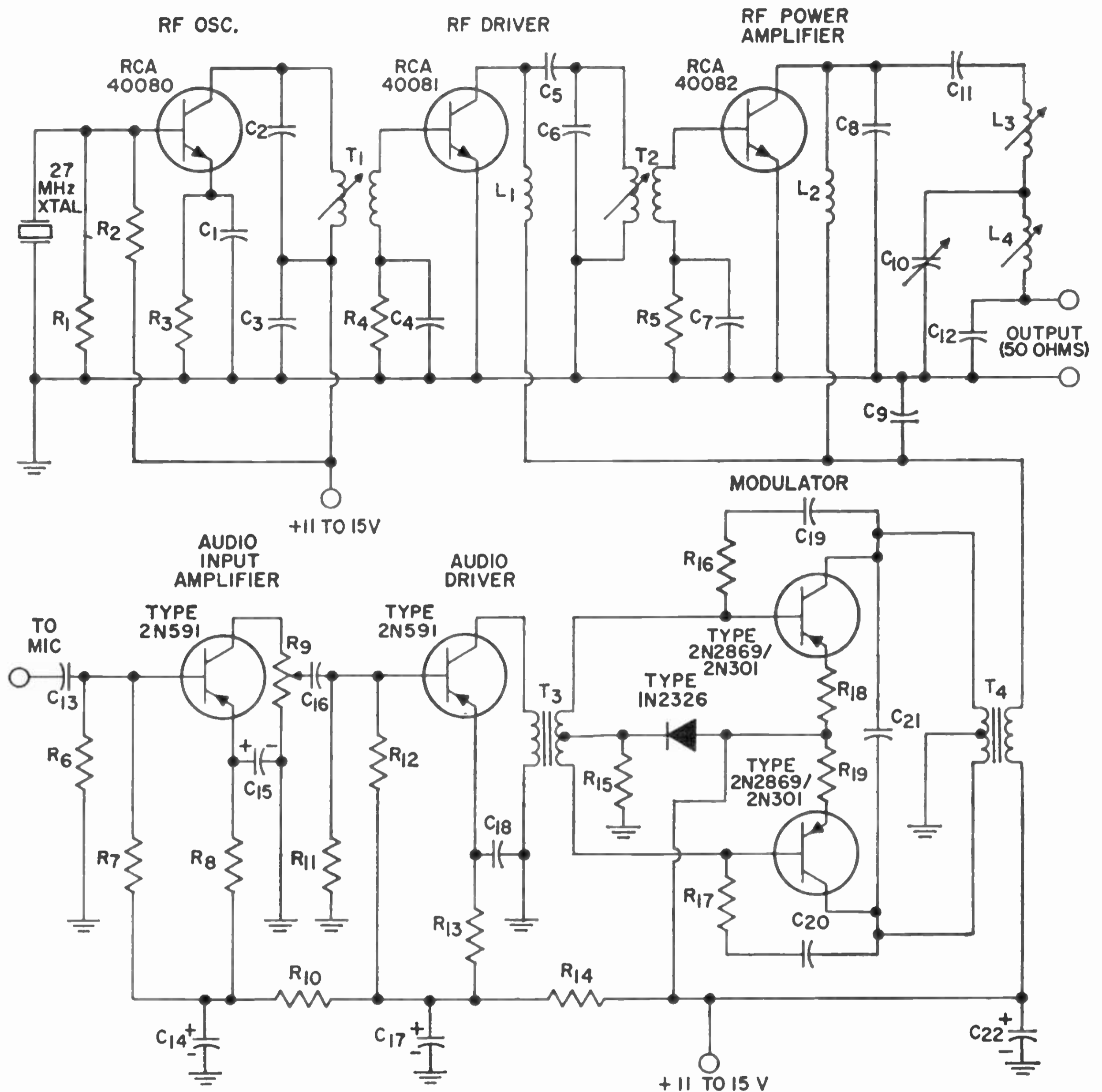
The rf section of the transmitter, which consists of a 40080 crystal-controlled oscillator, a 40081 driver, and a 40082 power amplifier, develops 3.5 watts of rf power output at 27 MHz. Both the driver and the power amplifier are modulated to achieve 100-per-cent amplitude modulation.

The 40080 crystal-controlled oscillator stage is a Colpitts type of circuit that provides excellent frequency stability with respect to collector supply voltage and temperature (well within the 0.005-per-

cent tolerance permitted by F.C.C. regulations) and delivers a minimum rf power of 100 milliwatts to the input of the driver stage.

The 40081 driver stage uses a class C common-emitter configuration. The modulation input is applied to the collector circuit. This stage delivers a minimum of 400 milliwatts of modulated rf power to the power amplifier. A heat dissipator should be mounted on the case of the 40081. The 40082 power-amplifier stage also uses a class C common-emitter configuration and is modulated through the collector circuit. The double- π network used as the output resonant circuit provides harmonic rejection of 50 dB, as required by F.C.C. regulations. The minimum rf power output supplied to the antenna from the power amplifier is 3 watts.

14-21 27-MHz, 5-WATT CITIZENS-BAND TRANSMITTER (cont'd)



NOTES: (1) See general considerations for construction of high-frequency and broadband circuits on page 582. (2) The 40082 transistor used in the rf power amplifier should be mounted on a good heat sink. (3) This circuit uses coils that are not standard commercial items; such coils must be wound by the circuit builder.

Parts List

C₁ = 75 pF, ceramic
 C₂ = 30 pF, ceramic
 C₃, C₇ = 0.01 μ F, ceramic
 C₄ = 0.001 μ F, ceramic
 C₅ = 47 pF, ceramic
 C₆ = 51 pF, mica
 C₈ = 24 pF, mica
 C₉ = 0.01 μ F, ceramic
 C₁₀ = variable capacitor, 90 to 400 pF (ARCO 429, or equiv.)
 C₁₁ = 100 pF, ceramic
 C₁₂ = 220 pF, ceramic
 C₁₃ = 5 μ F, ceramic
 C₁₄, C₁₇ = 50 μ F, electrolytic, 25 V
 C₁₅ = 10 μ F, electrolytic, 15 V
 C₁₆, C₁₈ = 10 μ F, ceramic
 C₁₉, C₂₀ = 0.2 μ F, ceramic
 C₂₁ = 0.1 μ F, ceramic

C₂₂ = 500 μ F, electrolytic, 15 V
 L₁, L₂ = rf choke, 15 μ H, Miller 4624, or equiv.
 L₃ = variable inductor (0.75 to 1.2 μ H); 11 turns No. 22 wire wound on $\frac{1}{4}$ -inch CTC coil form having a "green dot" core; Q = 120
 L₄ = variable inductor (0.5 to 0.9 μ H); 7 turns No. 22 wire wound on $\frac{1}{4}$ -inch CTC coil form having a "green dot" core; Q = 140
 R₁ = 510 ohms, 0.5 watt
 R₂, R₁₂ = 5100 ohms, 0.5 watt
 R₃ = 51 ohms, 0.5 watt
 R₄ = 120 ohms, 0.5 watt
 R₅ = 47 ohms, 0.5 watt
 R₆ = 0.1 megohm, 0.5 watt

R₇ = 10000 ohms, 0.5 watt
 R₈ = 2000 ohms, 0.5 watt
 R₉ = potentiometer, 10000 ohms
 R₁₀ = 3600 ohms, 0.5 watt
 R₁₁ = 15000 ohms, 0.5 watt
 R₁₃ = 1000 ohms, 0.5 watt
 R₁₄ = 1200 ohms, 0.5 watt
 R₁₅ = 240 ohms, 0.5 watt
 R₁₆, R₁₇ = 2700 ohms, 0.5 watt
 R₁₈, R₁₉ = 1.5 ohms, 0.5 watt
 T₁ = rf transformer; primary 14 turns, secondary 3 turns of No. 22 wire wound on $\frac{1}{4}$ -inch CTC coil form having a "green dot" core; slug-tuned (0.75 to 1.2 μ H); Q = 100
 T₂ = rf transformer; primary 14 turns, secondary

14-21 27-MHz, 5-WATT CITIZENS-BAND TRANSMITTER (cont'd)**Parts List (cont'd)**

2-3/4 turns of No. 22 wire wound on 1/4-inch CTC coil form having a "green dot" core; slug-tuned (0.75 to 1.2 μ H); Q = 100

T₃ = transformer; primary: 2500 ohms; secondary 200 ohms center-tapped; Microtran SMT 17-SB or equiv.

T₄ = transformer; primary: 100 ohms center-tapped; secondary: 30 ohms
XTAL = 27-MHz transmitting crystal

Circuit Description (cont'd)

In the audio (modulator) section of the transmitter, two 2N591 class A amplifier stages are used to drive a class AB push-pull output stage using two 2N2869/2N301 transistors. This design provides maximum efficiency with low distortion. A 1N2326 compensating diode is used

in the biasing network to provide thermal stability. The modulation transformer T₄ is designed to match the collector-to-collector load impedance of the modulator to the impedance of the rf driver and power-amplifier stages.

14-22 50-MHz, 40-WATT CW TRANSMITTER

With Load-Mismatch Protection

Circuit Description

This cw transmitter uses a VSWR bridge circuit to maintain a steady-state dissipation in the output stage under all conditions of antenna mismatch. This technique makes it possible to realize the full power potential of the 40341 overlay transistor used in the output stage.

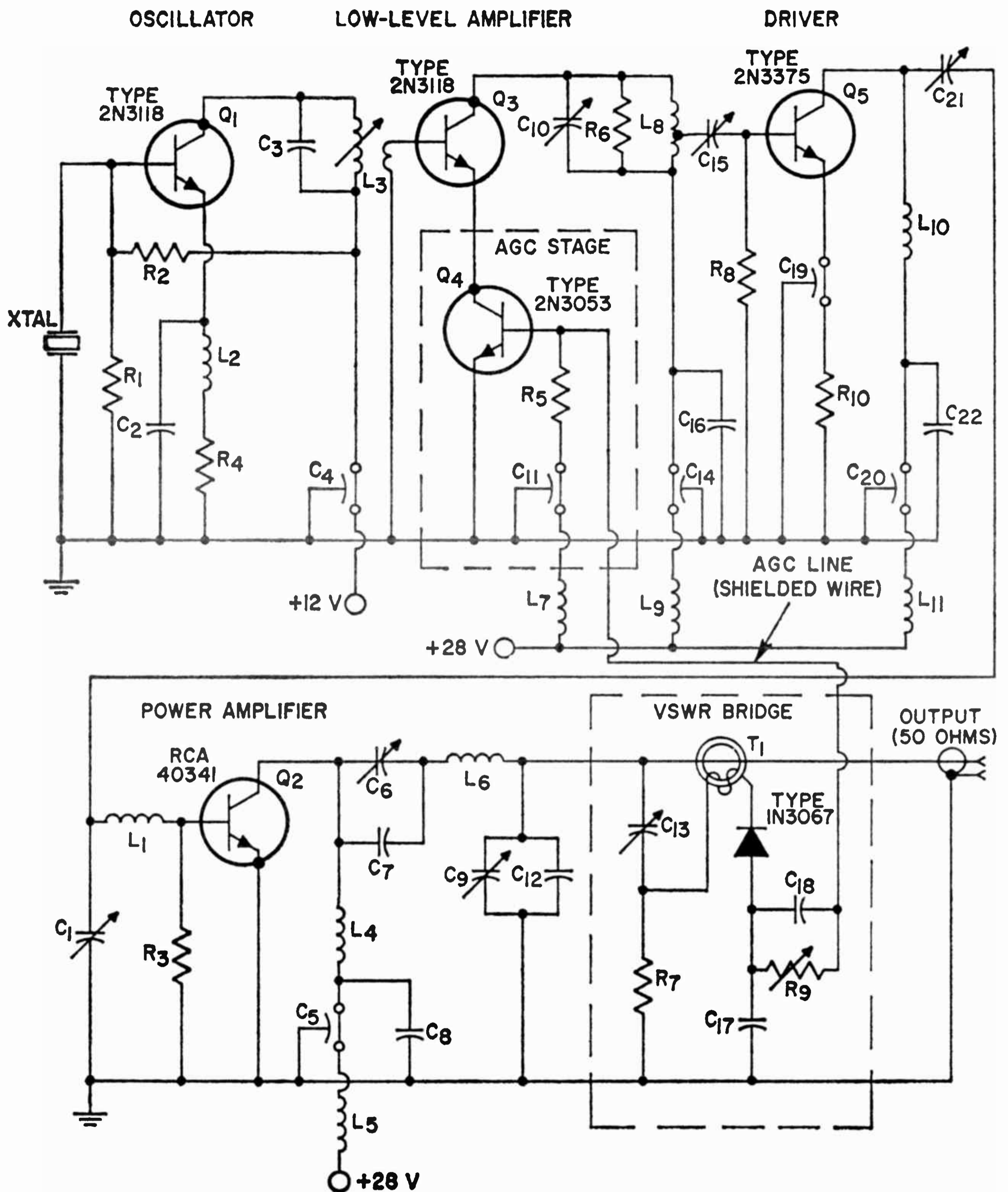
The 50-MHz crystal-controlled 2N3118 oscillator stage develops the low-level excitation signal for the transmitter. The 50-MHz output signal from the collector of the oscillator transistor is coupled by L₃ to the base of a second 2N3118 used in a predriver stage (low-level amplifier). This step-down transformer matches the collector impedance of the oscillator transistor to the low-impedance base circuit of the predriver transistor. The collector circuit of the predriver is tuned to provide maximum signal output at 50 MHz. This signal is coupled from a tap on inductor L₅ to the input (base) circuit of the driver stage, which uses a 2N3375 silicon power transistor to develop the power required to drive the output stage.

The 40341 overlay transistor used in the output stage develops 40 watts of power output at the transmitting frequency of 50 MHz. The driving power for the output stage is

coupled from the collector of the driver transistor through a bandpass filter to the base of the output transistor. The filter networks in the collector circuit of the 40341 provide the required harmonic and spurious-frequency rejection. The 50-MHz output from these filter sections is coupled through a length of 50-ohm coaxial line to the antenna. Capacitors C₁₁, C₁₂, and C₁₃ are adjusted to provide optimum impedance match between the transmitter and the antenna.

The output of the transmitter is sampled by a current transformer (toroid) T₁ loosely coupled about the output transmission line. This transformer is the sensor for a VSWR bridge detector used to prevent excessive dissipation in the output stage under conditions of antenna mismatch. If the antenna is disconnected or poorly matched to the transmitter, large standing waves of voltage and current occur on the output transmission line. A portion of this standing-wave energy is applied by T₁ to the 1N3067 diode in the bridge circuit. The rectified current from this diode charges capacitor C₁₄ to a dc voltage proportional to the amplitude of the standing waves. This voltage, which is essentially an agc bias, is applied to the

14-22 50-MHz, 40-WATT CW TRANSMITTER (cont'd)



NOTE: See general considerations for construction of high-frequency and broadband circuits on page 582.

Parts List

C₁ = variable capacitor, 90 to 400 pF, Arco No. 429 or equiv.
 C₂ = 51 pF, mica
 C₃ = 30 pF, ceramic
 C₄, C₅, C₁₁, C₁₄, C₁₉, C₂₀ = feedthrough capacitor, 1000 pF
 C₆ = variable capacitor, 1.5 to 20 pF, Arco No. 402 or equiv.
 C₇ = 36 pF, mica

C₈, C₁₆, C₂₂ = 0.02 μ F, ceramic
 C₉, C₁₀ = variable capacitor, 8 to 60 pF, Arco No. 404 or equiv.
 C₁₂ = 91 pF, mica
 C₁₃ = variable capacitor, 0.9 to 7 pF, Vitramon No. 400 or equiv.
 C₁₅ = variable capacitor, 14 to 150 pF, Arco No. 426 or equiv.

C₁₇ = 1000 pF, ceramic
 C₁₈ = 0.01 μ F, ceramic
 C₂₁ = variable capacitor, 32 to 250 pF, Vitramon No. 464 or equiv.
 L₁ = 1 turn of No. 16 wire; inner diameter, $\frac{5}{16}$ inch; length, $\frac{1}{8}$ inch
 L₂ = rf choke, 1 μ H
 L₃ = oscillator coil; primary, 7 turns; secondary, 1- $\frac{3}{4}$ turns; wound from

14-22 50-MHz, 40-WATT CW TRANSMITTER (cont'd)**Parts List (cont'd)**

No. 22 wire on CTC coil form having "white dot" core	$L_8 = 6$ turns of No. 16 wire; inner diameter, $\frac{3}{8}$ inch; length, $\frac{3}{4}$ inch	$R_7 = 240$ ohms, 0.5 watt
$L_4 = 5$ turns of No. 16 wire; inner diameter, $\frac{5}{16}$ inch; length, $\frac{1}{2}$ inch	$R_1, R_6 = 510$ ohms, 0.5 watt	$R_9 =$ agc control, potentiometer, 50000 ohms
$L_5, L_7, L_9, L_{10}, L_{11} =$ rf choke, 7 μ H	$R_2 = 3900$ ohms, 0.5 watt	$R_{10} = 5.6$ ohms, 1 watt
$L_6 = 4$ turns of B & W No. 3006 coil stock	$R_3, R_8 = 2.2$ ohms, wire-wound, 0.5 watt	$T_1 =$ current transformer (toroid), Arnold No. A4-437-125-SF, or equiv.
	$R_4 = 51$ ohms, 0.5 watt	XTAL = 50-MHz transmitting crystal
	$R_5 = 24000$ ohms, 0.5 watt	

Circuit Description (cont'd)

base of the 2N3053 agc amplifier stage. The output of the agc stage biases the 2N3118 predriver stage so that its gain changes in inverse proportion to the amplitude of the standing wave on the output transmission line. Therefore, as the amplitude of the standing waves increases (tending to cause higher

heat dissipation in the output transistor), the input drive to the output stage is reduced. This compensating effect maintains a steady-state dissipation in the output transistor regardless of mismatch conditions between the transmitter output circuit and the antenna.

14-23**175-MHz, 35-WATT AMPLIFIER****Circuit Description**

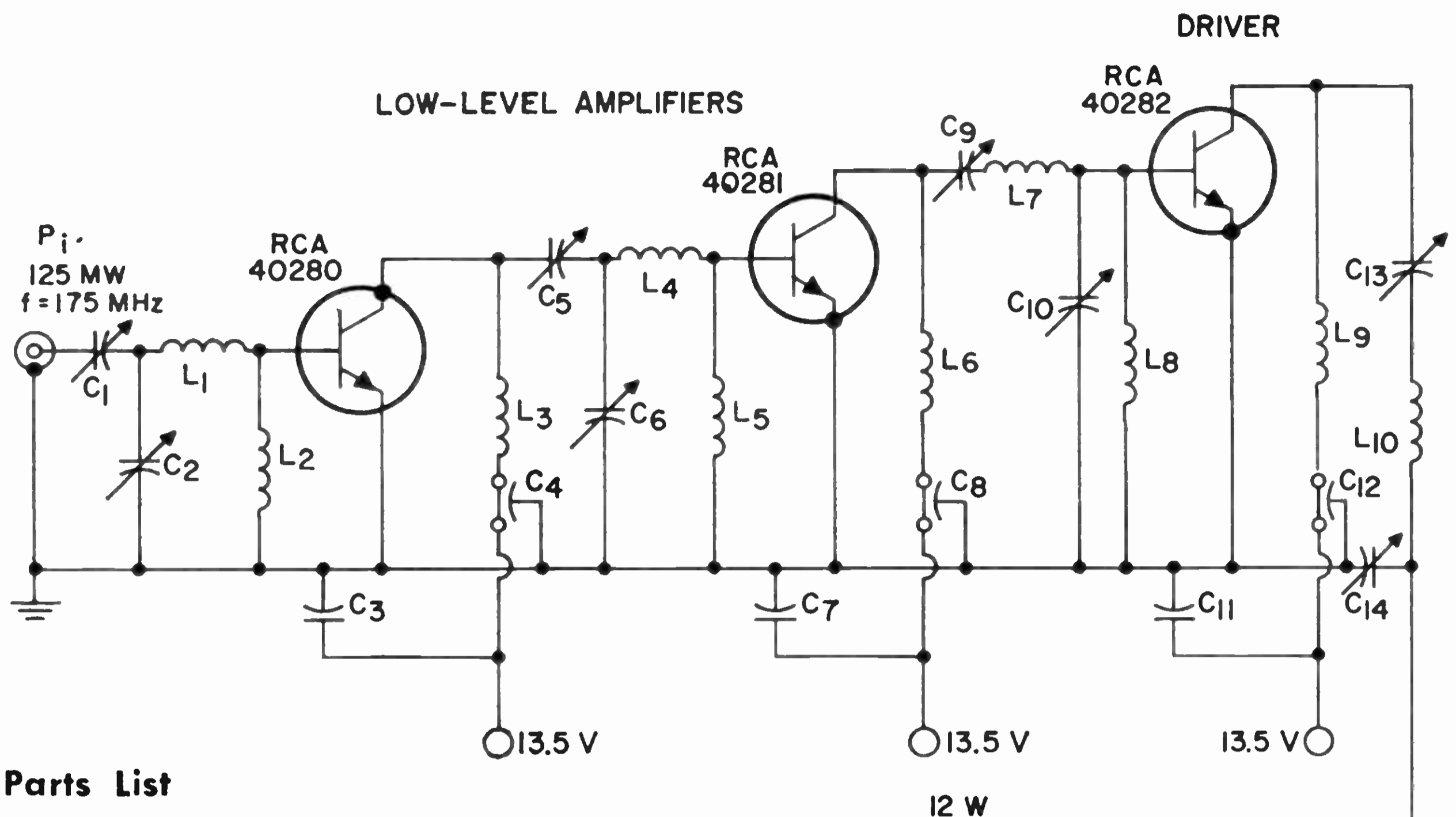
This four-stage rf power amplifier operates from a dc supply of 13.5 volts and delivers 35 watts of power output at 175 MHz for an input of 125 milliwatts. The silicon overlay transistors used in the amplifier supply maximum output power at this level of dc voltage for use in mobile systems.

The low-level portion of the amplifier consists of three unneutralized, class C, common-emitter rf amplifier stages interconnected by band-pass filters tuned to provide maximum transfer of energy at 175 MHz. The 40280 input stage develops 1 watt of power output when a 125-milliwatt 175-MHz signal is applied to the amplifier input terminal. This output is increased to 4 watts by the 40281 transistor used in the second stage. The 40282 driver transistor then develops 12 watts of driving power for the output stage.

When the low-level stages and the output stage are mounted on separate chassis, the output from the driver stage is coupled to the output stage through a low-loss coaxial line. The line is terminated by variable capacitors C_{15} and C_{16} and inductor L_{11} . The capacitors are adjusted to assure a good impedance match between the output of the driver and the input of the output stage at 175 MHz. The driving signal developed across inductor L_{11} is applied to the tuned input networks of three parallel-connected 40282 transistors in the single-ended output stage. For an input of 12 watts, the three 40282 transistors deliver 35 watts of 175-MHz power to the output terminal of the amplifier. Capacitors C_{26} and C_{27} are adjusted to match the amplifier output to the load impedance at the operating frequency.

14-23

175-MHz, 35-WATT AMPLIFIER (cont'd)

**Parts List**

C_1 = variable capacitor, 3 to 35 pF, Arco No. 403, or equiv.

$C_2, C_8, C_{16}, C_{17}, C_{18}, C_{19}, C_{27}$ = variable capacitor, 8 to 60 pF, Arco No. 404, or equiv.

C_3, C_7, C_{11} = 0.1 μF , ceramic disc

$C_4, C_8, C_{12}, C_{21}, C_{23}, C_{25}$ = feedthrough capacitor, 1500 pF

$C_5, C_{10}, C_{13}, C_{14}, C_{28}$ = variable capacitor, 7 to 100 pF, Arco No. 423, or equiv.

C_9 = variable capacitor, 14 to 150 pF, Arco No. 424 or equiv.

C_{15} = variable capacitor, 1.5 to 20 pF, Arco No. 402 or equiv.

C_{20}, C_{22}, C_{24} = 0.2 μF , ceramic disc

L_1 = 2 turns of No. 16 wire; inner diameter, $\frac{3}{16}$ inch; length, $\frac{1}{4}$ inch

L_2, L_5, L_8 = 450-ohm ferrite rf choke

L_3, L_6, L_{11} = rf choke, 1.0 μH

L_4, L_7 = 3 turns of No. 16 wire; inner diameter, $\frac{3}{16}$ inch; length, $\frac{1}{4}$ inch

L_9 = 1- $\frac{1}{2}$ turns of No. 16 wire; inner diameter, $\frac{1}{4}$ inch; length, $\frac{3}{8}$ inch

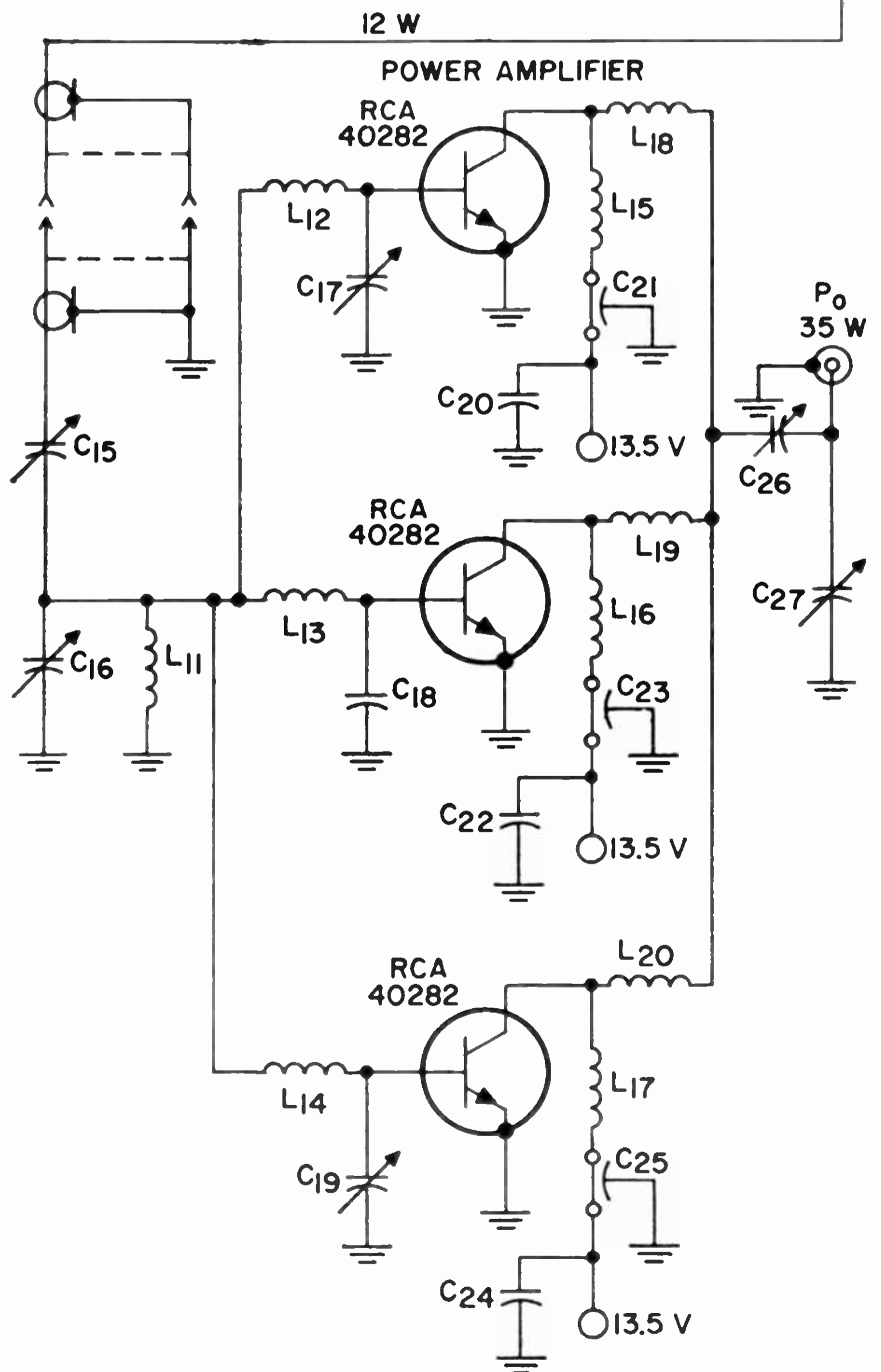
L_{10} = 2 turns of No. 16 wire; inner diameter, $\frac{1}{4}$ inch; length, $\frac{5}{16}$ inch

L_{12}, L_{13}, L_{14} = 5 turns of No. 16 wire; inner diameter, $\frac{1}{4}$ inch; length, $\frac{1}{2}$ inch

L_{15}, L_{16}, L_{17} = 2 turns of No. 18 wire; inner diameter, $\frac{1}{8}$ inch; length, $\frac{1}{8}$ inch

L_{18}, L_{19}, L_{20} = 2 turns of No. 16 wire; inner diameter, $\frac{1}{4}$ inch; length, $\frac{1}{4}$ inch

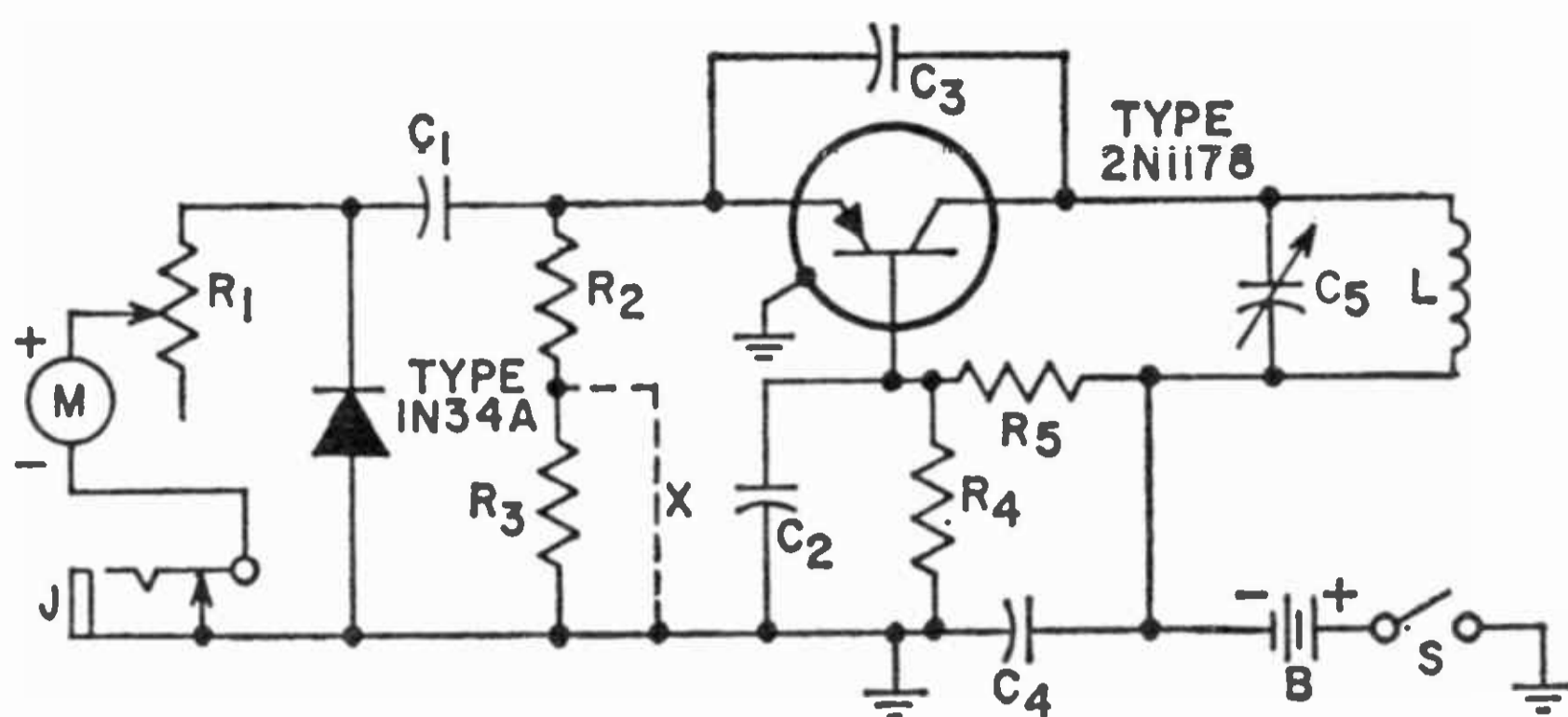
NOTE: See general considerations for construction of high-frequency and broadband circuits on page 582.



14-24

"GRID-DIP" METER

For Measuring Resonant Frequencies from 3.5 to 1000 MHz



Parts List

B = 13.5 volts, RCA VS304
 C₁ = 33 pF, mica, 50 V
 C₂ = 0.01 μF, paper, 50 V
 C₃ = 5 pF, mica, 50 V
 C₄ = 0.01 μF, paper, 50 V
 C₅ = variable capacitor, 50 pF, Hammarlund type HF-50 or equivalent

J = phone jack, normally closed
 L = plug-in coil
 M = microammeter, 0 to 50 μA, Simpson model 1227 or equivalent
 R₁ = variable resistor, 0-0.25

megohm, 0.5 watt
 R₂ = 220 ohms, 0.5 watt
 R₃ = 3,000 ohms, 0.5 watt
 R₄ = 3,900 ohms, 0.5 watt
 R₅ = 39,000 ohms, 0.5 watt
 X = jumper, omit for measurements below 45 MHz

Coil-Winding Data

Coil Freq. Range	Wire Size	No. of Turns
1 3.4-6.9 MHz	#28, enamel	48 ¹ / ₄ , close wound
2 6.7-13.5 MHz	#24, enamel	22, close wound
3 13-27 MHz	#24, enamel	9 ¹ / ₈ , close wound
4 25-47 MHz	#24, enamel	4 ¹ / ₈ , close wound
5 46-78 MHz	#24, enamel	1 ¹ / ₂ , close wound
6 74-97 MHz	#16, tinned	hairpin formed, 1 ⁷ / ₈ inches long including pins, and ¹ / ₄ inch wide

Coil forms are Amphenol type 24-5H or equivalent.

Circuit Description

This circuit, which is essentially a transistor version of the electron-tube grid-dip meter, determines the frequency of resonant circuits quickly and accurately. Basically, it consists of a 2N1178 common-base rf oscillator stage that can be tuned over a wide frequency range. A 1N34A diode and a dc microammeter are used to show when rf power is being absorbed from the oscillator tuned circuit. The dc power for the oscillator is obtained from a 13.5-volt miniature battery such as the RCA VS304.

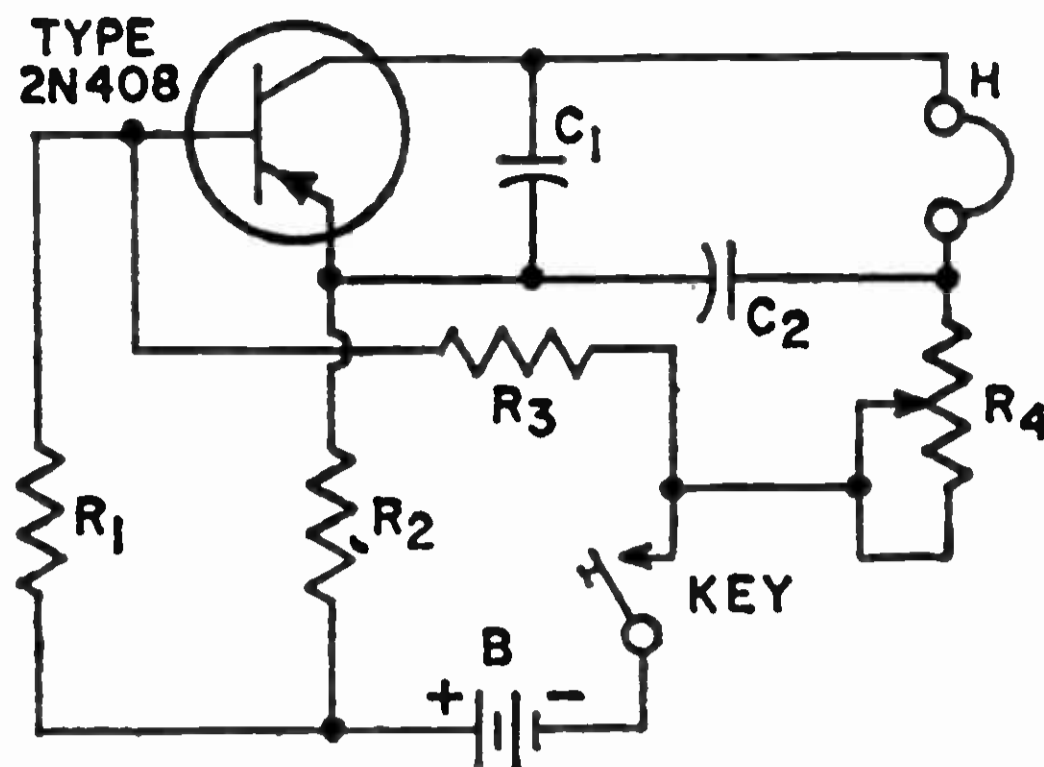
Inductor L and capacitor C₅ form the oscillator resonant circuit. Feedback to sustain oscillations in the resonant circuit is coupled by capacitor C₃ from the collector to the emitter of the 2N1178. RF voltage in the emitter-to-base circuit is coupled by C₁ to the 1N34A diode, and the rectified output appears on the dc microammeter. When power

is absorbed from the oscillator resonant circuit, rf feedback is reduced and the reading on the microammeter decreases.

The coil used for inductor L is selected for the operating frequency desired. A frequency-tuning dial mounted on the same shaft with the variable capacitor C₅ indicates the operating frequency of the meter. For measurement of the frequency of a resonant circuit, a coil having a suitable frequency range is inserted in the grid-dip meter, and the meter control knob is adjusted for a reading of about half-scale. The grid-dip meter is then tightly coupled to the unknown tuned circuit, and the tuning dial is rotated until a dip in the meter reading occurs. When transmitter tank circuits are measured, the transmitter plate supply must be turned off to eliminate danger of shock.

14-25

CODE-PRACTICE OSCILLATOR



Parts List

B = 1.5-4.5 V (One to three series-connected RCA VS036 dry cells may be used, depending upon the volume level desired.)

$C_1, C_2 = 0.1 \mu\text{F}$, paper, 150 V
H = Headphone, 2000-ohm, magnetic
 $R_1 = 2200$ ohms, 0.5 watt

$R_2 = 27000$ ohms, 0.5 watt
 $R_3 = 3000$ ohms, 0.5 watt
 $R_4 =$ volume control potentiometer, 50000 ohms, 0.5 watt

Circuit Description

This simple audio oscillator operates from a dc supply of 1.5 to 4.5 volts, depending on the amount of output desired. Magnetic headphones provide an audible indication of keying. When the key is closed, the 2N408 transistor supplies energy to the resonant circuit formed by capacitors C_1 and C_2 and the inductance

of the headphones, and this circuit resonates to produce an audio tone in the headphones. Positive feedback to sustain oscillation is coupled from the resonant circuit through C_1 and C_2 to the emitter of the 2N408. R_4 is adjusted to obtain the desired level of sound from the headphones.

14-26

AUDIO OSCILLATOR

Circuit Description

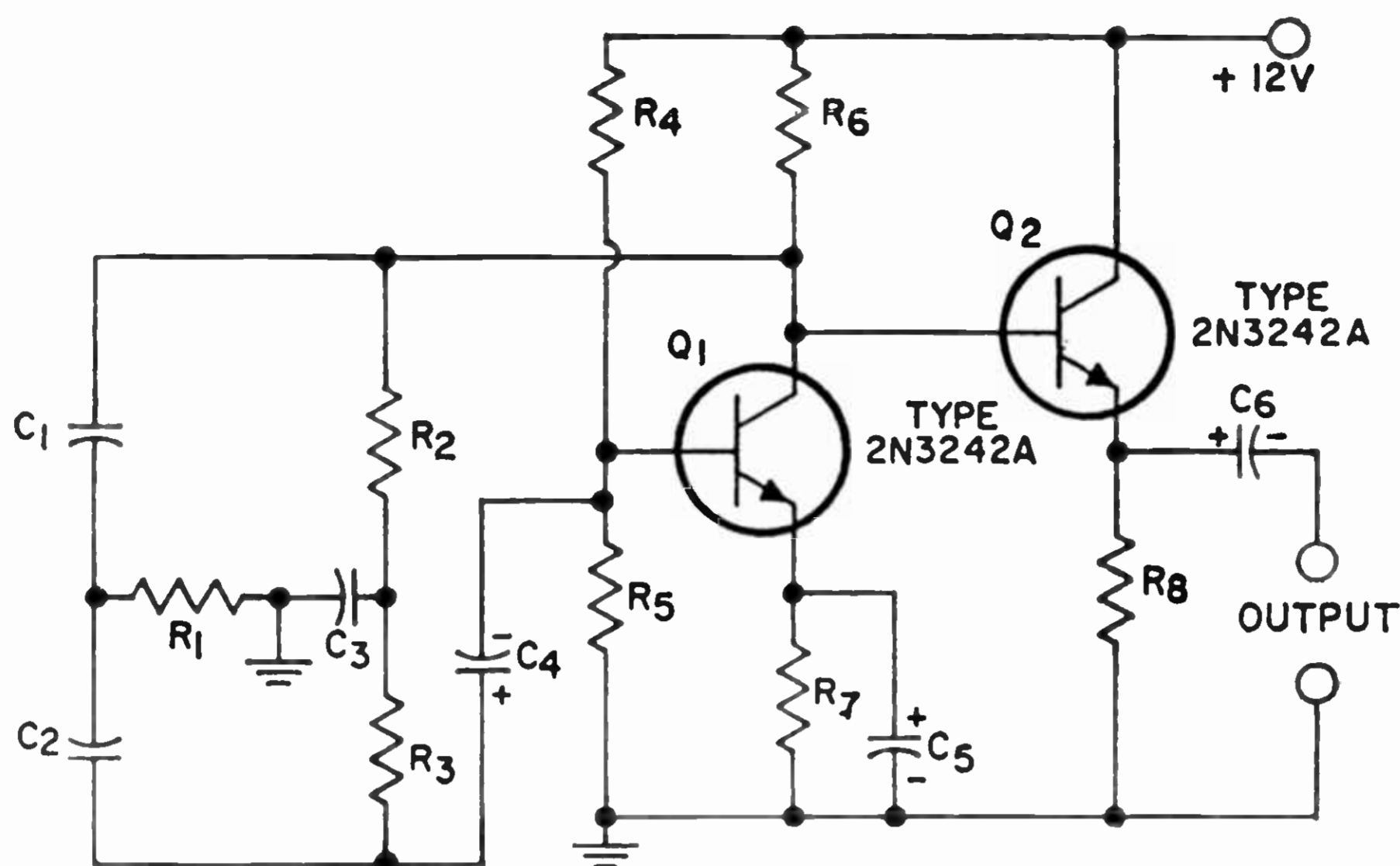
This basic audio-oscillator circuit may be used to provide a single-tone sine-wave output at any frequency from 2 Hz to 175 kHz. (A chart of capacitance values is shown for different frequencies of operation.) The circuit is excellently suited for use in the testing of high-fidelity audio equipment and amateur radio transmitters; it can also be adapted for use as a code-practice oscillator. The oscillator operates from a dc supply of 12 volts and supplies a relatively distortion-free output waveform to any circuit that has an input impedance of 3000 ohms or more.

The 2N3241A amplifier transistor Q_1 , capacitors C_1, C_2, C_3 , and C_4 , and

resistors R_1, R_2 , and R_3 form a basic twin-T oscillator circuit. A portion of the signal developed at the collector of transistor Q_1 is applied to the twin-T network formed by C_1, C_2, C_3, R_1, R_2 , and R_3 . The output of this network is then coupled to the base of transistor Q_1 through capacitor C_4 to supply the positive feedback required to sustain oscillation. The oscillator-stage output from the collector of transistor Q_1 is applied to the base of the 2N3241A output transistor Q_2 , which is operated in an emitter-follower circuit configuration. This stage amplifies the oscillator output to provide the sine-wave output signal.

14-26

AUDIO OSCILLATOR (cont'd)



Parts List

- | | | | | | | | | | | | |
|--|--|---|--|---|--------------------------------------|--|---------------------------------------|---------------------------------------|--------------------------------------|--------------------------------------|-------------------------------------|
| C ₁ , C ₂ = see chart for value, mica or paper | C ₃ = twice the value of C ₁ , mica or paper | C ₄ = 1 μF, electrolytic, 12 V | C ₅ = 300 μF for frequencies below 2000 Hz or 5 μF for frequencies above 2000 Hz, electrolytic, 6 V | C ₆ = 20 μF, electrolytic, 6 V | R ₁ = 2700 ohms, 0.5 watt | R ₂ , R ₃ = 27000 ohms, 0.5 watt | R ₄ = 0.1 megohm, 0.5 watt | R ₅ = 22000 ohms, 0.5 watt | R ₆ = 6800 ohms, 0.5 watt | R ₇ = 2200 ohms, 0.5 watt | R ₈ = 820 ohms, 0.5 watt |
|--|--|---|--|---|--------------------------------------|--|---------------------------------------|---------------------------------------|--------------------------------------|--------------------------------------|-------------------------------------|

Capacitor Selection Chart for Different Operating Frequencies

Approx. Freq. (Hz)	Value of C ₁ and C ₂
175000	50 pF
95000	100 pF
10000	500 pF
2000	1000 pF
200	0.01 μF
100	0.05 μF
20	0.1 μF
10	0.5 μF
2	5 μF*

* 6-volt electrolytic capacitors may be used for this value.

14-27

ELECTRONIC KEYS

Circuit Description

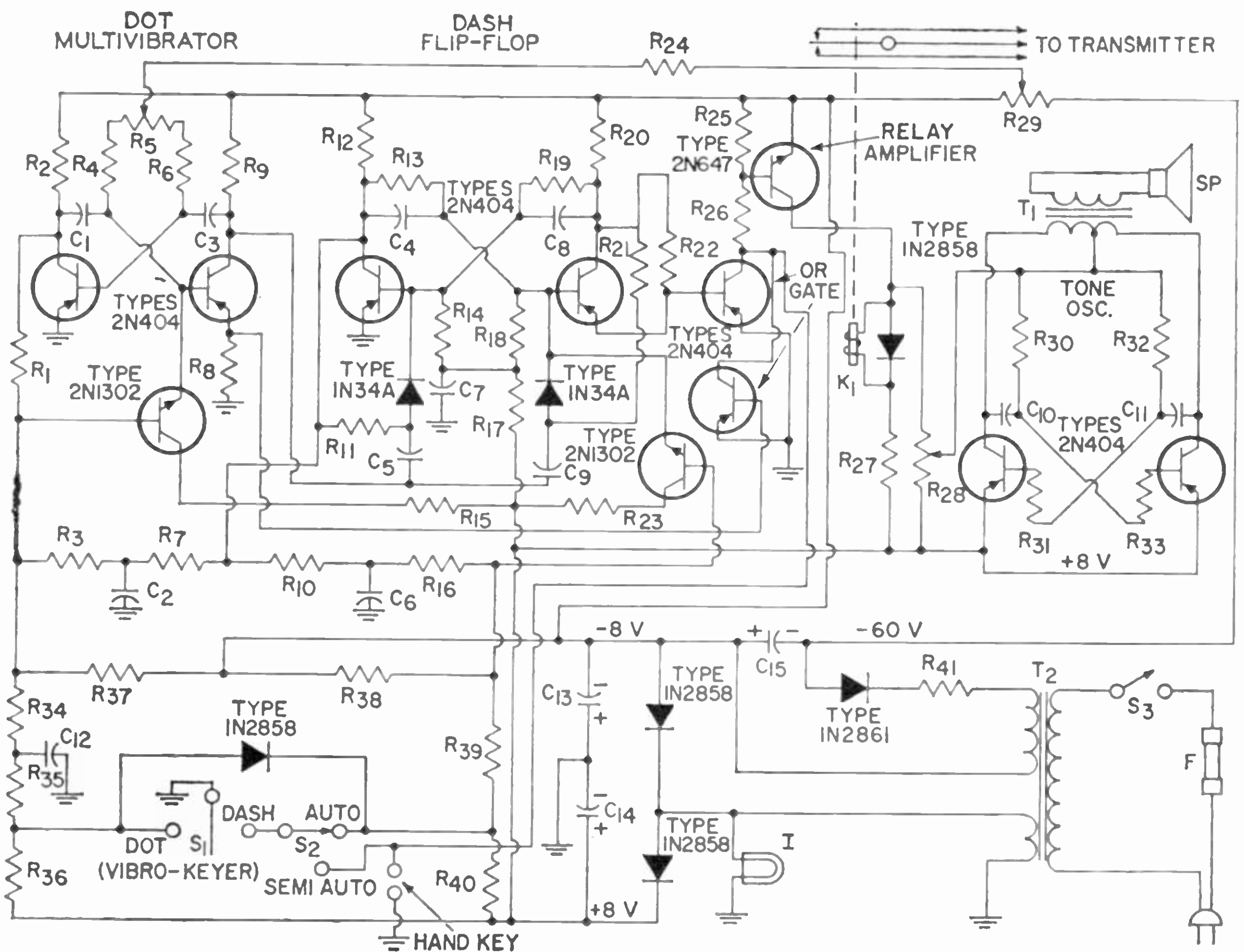
This compact electronic keyer can be used for automatic keying of a cw transmitter at speeds up to 60 words per minute. Two multivibrator trigger circuits using 2N404 transistors automatically control the dot and dash transmissions. A "Vibro-Keyer", which is spring-loaded to the OFF position, selects the type of transmission desired. Unless the "Vibro-Keyer" is moved to either the DOT or the DASH position, both multivibrators are held

inoperative by the biasing action of 2N1302 clamping circuits.

When the "Vibro-Keyer" S₁ is deflected to the DOT position, the first 2N1302 clamp transistor becomes inoperative, and the dot multivibrator is allowed to operate as a free-running circuit. Feedback circuits in the multivibrator assure continued operation, regardless of whether S₁ remains in the DOT position, long enough to develop the square-wave output that controls both the dura-

14-27

ELECTRONIC KEYS (cont'd)



Parts List

$C_1, C_3 = 1 \mu\text{F}$, paper (or Mylar), 200 V
 $C_2 = 0.47 \mu\text{F}$, ceramic, 25 V
 $C_4, C_8 = 560 \text{ pF}$, ceramic, 600 V
 $C_5, C_9 = 330 \text{ pF}$, ceramic, 600 V
 $C_6, C_7 = 0.01 \mu\text{F}$, ceramic, 50 V
 $C_{10}, C_{11} = 0.02 \mu\text{F}$, ceramic, 50 V
 $C_{12} = 0.1 \mu\text{F}$, ceramic, 50 V
 $C_{13}, C_{14} = 2000 \mu\text{F}$, electrolytic, 15 V
 $C_{15} = 16 \mu\text{F}$, electrolytic, 150 V
 F = fuse, 1 ampere
 I = indicator lamp No. 47
 K = dc relay; coil resistance = 1350 ohms; Potter & Brumfield RS5D-V or equiv.
 $R_1 = 39000 \text{ ohms}$, 0.5 watt
 $R_2, R_9, R_{12}, R_{20} = 3900 \text{ ohms}$,

0.5 watt
 $R_3, R_{16} = 18000 \text{ ohms}$, 0.5 watt
 $R_4, R_8 = 51000 \text{ ohms}$, 0.5 watt
 $R_5, R_{29} = \text{potentiometer}$, 10000 ohms
 $R_7, R_{10} = 22000 \text{ ohms}$, 0.5 watt
 $R_8, R_{22} = 180 \text{ ohms}$, 0.5 watt
 $R_{11}, R_{21} = 15000 \text{ ohms}$, 0.5 watt
 $R_{13}, R_{19} = 33000 \text{ ohms}$, 0.5 watt
 $R_{14}, R_{18}, R_{30}, R_{32} = 27000 \text{ ohms}$, 0.5 watt
 $R_{15}, R_{23} = 270 \text{ ohms}$, 0.5 watt
 $R_{17} = 68000 \text{ ohms}$, 0.5 watt
 $R_{24} = 100000 \text{ ohms}$, 0.5 watt
 $R_{25} = 68 \text{ ohms}$, 0.5 watt
 $R_{26} = 560 \text{ ohms}$, 0.5 watt
 $R_{27} = 620 \text{ ohms}$, 0.5 watt
 $R_{28} = \text{volume-control}$

potentiometer, 50000 ohms
 $R_{31}, R_{33} = 10000 \text{ ohms}$, 0.5 watt
 $R_{34} = 6800 \text{ ohms}$, 0.5 watt
 $R_{35} = 8200 \text{ ohms}$, 0.5 watt
 $R_{36}, R_{39}, R_{10} = 15000 \text{ ohms}$, 0.5 watt
 $R_{37}, R_{38} = 47000 \text{ ohms}$, 0.5 watt
 $R_{41} = 10000 \text{ ohms}$, 1 watt
 $S_1 = \text{Vibroplex keyer}$, or equiv.
 $S_2 = \text{toggle switch}$, double-pole, double-throw
 $S_3 = \text{toggle switch}$; single-pole, single-throw
 $T_1 = \text{push-pull output transformer}$ (14000 ohm to V.C.), Stancor No. A3496, or equiv.
 $T_2 = \text{power transformer}$, Stancor PS8415, PS8421, or equiv.

Circuit Description (cont'd)

tion of the dot and the space that follows it. When S_1 is set to the DASH position, both clamp transistors become inoperative. The dot multivibrator and the dash flip-flop then operate simultaneously. The

dash flip-flop is triggered by the positive pulses from the dot multivibrator. The 1N34A steering diodes prevent triggering of the flip-flop by negative pulses. Because two positive pulses are required to produce

14-27

ELECTRONIC KEYER (cont'd)**Circuit Description (cont'd)**

one complete cycle of output from the flip-flop, the frequency of this circuit is one-half that of the dot multivibrator.

The square-wave outputs from the dot multivibrator and the dash flip-flop are coupled to two more 2N404 transistors used in an OR gate circuit. During the positive half-cycle of the square-wave inputs, the OR gate conducts to remove the cutoff bias from the 2N647 relay amplifier, which controls the operation of keying relay K_1 . The relay is then energized, and its contacts close for the period required to key the transmitter for the selected type of transmission. One section of K_1 may be used to mute the receiver during key-down periods. Because the OR gate circuit is keyed successively by signals from the dot multivibrator and the dash flip-flop in the formation of a dash, the duration of a dash is three times that of a dot.

The keying speed of this electronic keyer is determined by the frequency of the dot multivibrator. This frequency is adjustable by means of potentiometer R_{29} , which varies the amplitude of the negative dc voltage. As the negative voltage at the armature of potentiometer R_5 is increased to a maximum value of 60 volts, the keying speed is increased to a maximum of 60 words per minute. Potentiometer R_5 controls the ratio of "on time" to "off time" of the dot multivibrator transistors, and thus determines the

duration of both dot and dash transmissions and the minimum spacing between successive transmissions. The over-all keying speed is not affected by this adjustment.

The electronic keyer may also be operated as a semiautomatic key ("bug") when selector switch S_2 is placed in the SEMIAUTO position. Dots are still produced automatically, but the automatic keying circuits are bypassed when S_1 is moved to the DASH position. The formation of dashes is then controlled manually. When S_2 is in the MAN position, a hand key (connected across the terminals marked HAND KEY) may be used for manual control of the keyer; the automatic keying circuits are then bypassed during the formation of both dots and dashes.

The keyer operates from a 117-volt, 60-Hz ac power input applied through a step-down power transformer T_2 . The ac input voltage is converted to the negative dc voltage used to control keying speed by a 1N2861 half-wave rectifier circuit. Two other 2N2861 diodes are used in a voltage-doubler circuit that operates from the 6.3-volt secondary winding of transformer T_2 to produce the dc supply voltage for the various circuits in the keyer. A 2N404 tone oscillator, which is gated on by the relay-amplifier circuit, provides an audible indication of keying.

14-28

POWER SUPPLY FOR AMATEUR TRANSMITTER

600 Volts; 300 Volts; Total Current 330 Milliamperes

(Intermittent Duty)

Circuit Description

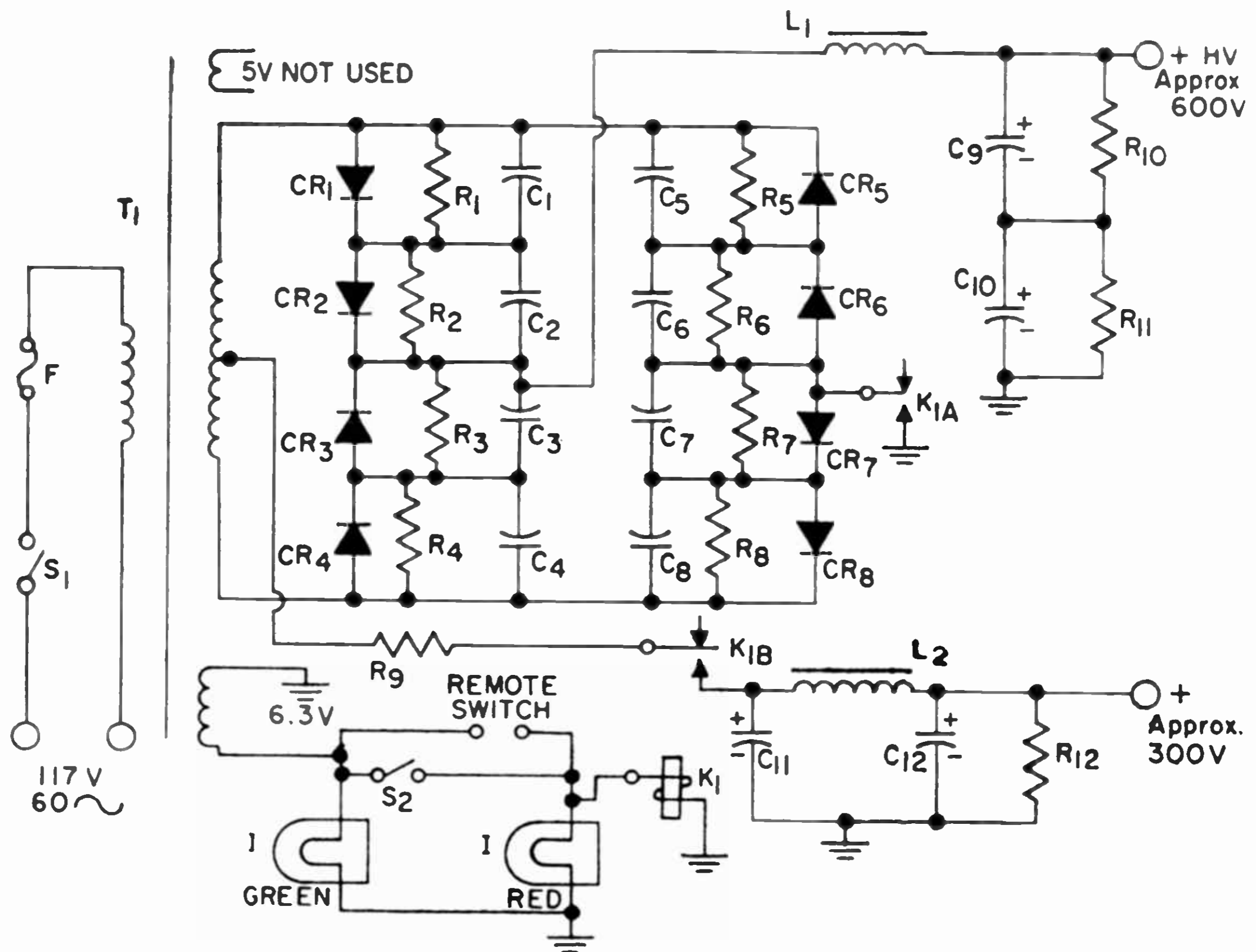
This power supply uses eight 1N2864 silicon diodes in series-connected pairs in a bridge-rectifier circuit to supply a 600-volt dc output from a 117-volt ac input. The second set of diode pairs (CR_5 through CR_8) is also used in a conventional full-wave rectifier circuit

to supply a 300-volt dc output. Series-connected pairs of diodes are used to provide the rectification in this circuit because the peak-inverse-voltage rating of such combinations is twice that of a single diode.

The operation of the power supply is controlled by two switches.

14-28

POWER SUPPLY FOR AMATEUR TRANSMITTER (cont'd)



Parts List

C_1 C_2 C_3 C_4 C_5 C_6 C_7 C_8 =
0.001 μ F, ceramic disc,
1000 V
 C_9 , C_{10} , C_{11} , C_{12} = 40 μ F,
electrolytic, 450 V
 CR_1 CR_2 CR_3 CR_4 CR_5 CR_6
 CR_7 CR_8 = RCA-1N2864
F = fuse, 5 amperes
I = indicator lamp

K_1 = relay; Potter and
Brumfield KA11AY or
equiv.
 L_1 = 2.8 henries, 300 mA;
Stancor C-2334 or equiv.
 L_2 = 4 henries, 175 mA;
Stancor C-1410 or equiv.
 R_1 R_2 R_3 R_4 R_5 R_6 R_7 R_8 =
0.47 megohm, 0.5 watt

R_9 = 47 ohms, 1 watt
 R_{10} R_{11} = 15000 ohms, 10
watts
 R_{12} = 47000 ohms, 2 watts
 S_1 S_2 = toggle switch, single-
pole single-throw
T = power transformer;
Stancor P-8166 or equiv.

Circuit Description (cont'd)

When the ON-OFF switch S_1 is closed, the 117-volt 60-c/s ac input power is applied across the primary of the step-up power transformer T_1 . The power supply does not become operative, however, until switch S_2 is also closed. Relay K_1 is then energized, and the closed contacts of the relay complete the ground return paths for the power-supply circuits. Switch S_2 can be used as a STANDBY switch for the transmitter, or another switch may be connected in parallel with S_2 so that the standby-to-on function can be controlled from a remote location.

During the half-cycle of ac input for which the voltage across the

secondary winding of T_1 is positive at the top end and negative at the bottom end, current flows from the bottom of the secondary through diodes CR_7 and CR_8 (which are oriented in the proper direction), out the K_{1A} section of the relay contacts to ground, and then up through bleeder resistors R_{10} and R_{11} and the external load connected in shunt with the resistors to develop the 600-volt output. The return flow is completed through filter choke L_1 , diodes CR_1 and CR_2 , and the entire secondary winding. During the next half-cycle of the ac input, the polarity of the voltage across the secondary reverses, and the current flows

14-28 POWER SUPPLY FOR AMATEUR TRANSMITTER (cont'd)

through diodes CR₅ and CR₆, through the bleeder resistors and the external load circuit in the same direction as before, and then through diodes CR₃ and CR₄. Capacitors C₉ and C₁₀ and choke L₁ provide the filtering to smooth out the pulsations in the 600-volt dc output.

For the 300-volt dc output, only one-half the voltage across the secondary winding of T₁ is required. The CR₅-CR₆ and CR₇-CR₈ diode pairs are operated in a full-wave rectifier configuration to provide this

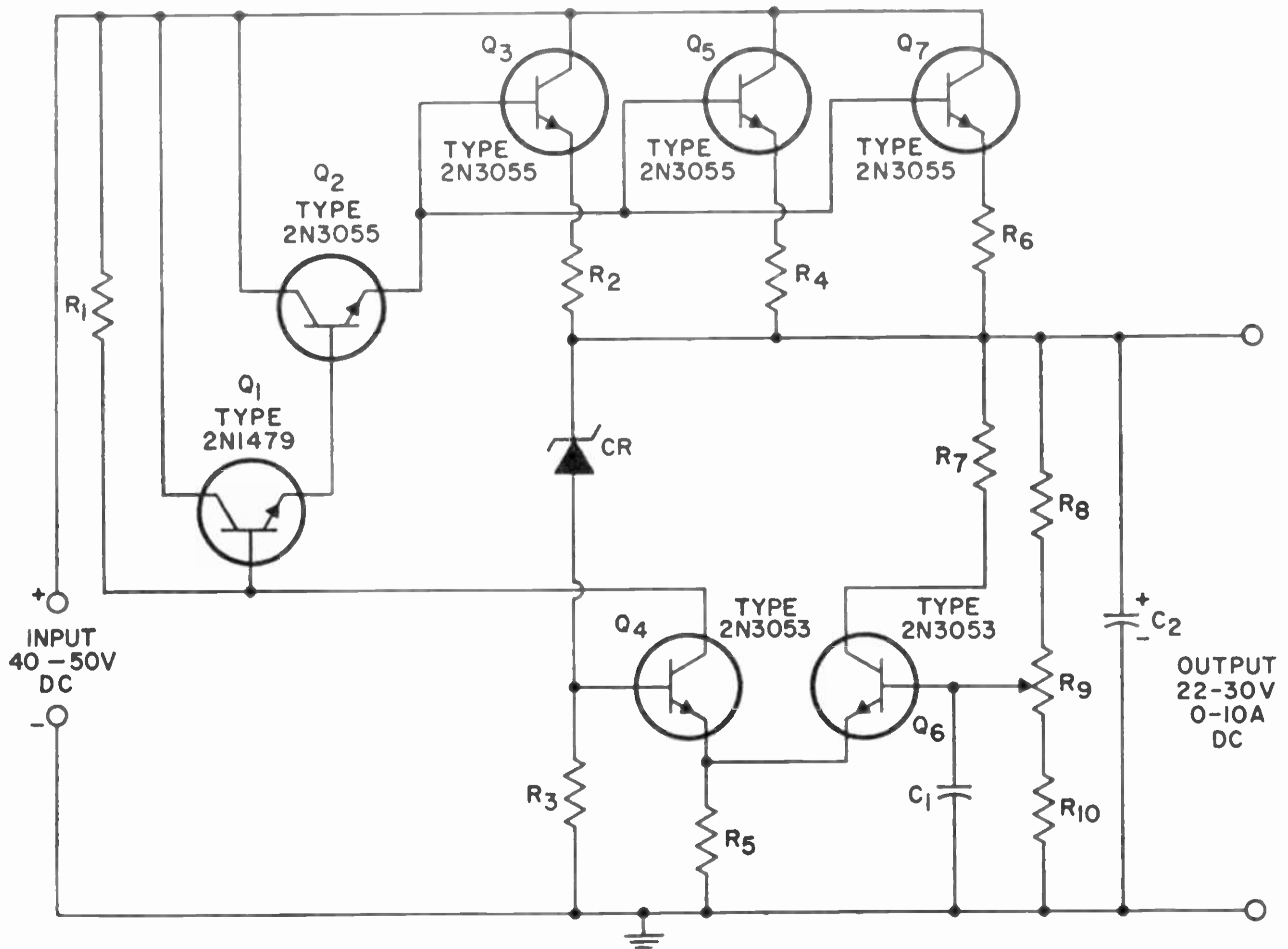
output (diodes CR₁ through CR₄ are not included in the 300-volt circuit.) The current flow through the diode pairs is the same as described before, but the current is directed from the relay contacts up through bleeder resistor R₁₂ and the external load circuit to develop the 300-volt output. The return flow is through choke L₂ and the transformer center tap. Capacitors C₁₁ and C₁₂ and choke L₂ provide the filtering for the 300-volt dc output.

14-29 VOLTAGE REGULATOR, SERIES TYPE

With Adjustable Output

Line Regulation within 1.0%

Load Regulation within 0.5%



Parts List

- | | | |
|---|--|--|
| C ₁ = 1 μF, paper, 25 V | R ₁ = 1200 ohms, 0.5 watt | R ₇ = 270 ohms, 0.5 watt |
| C ₂ = 100 μF, electrolytic, 50 V | R ₂ R ₄ R ₆ = 0.1 ohm, 0.5 watt | R ₈ R ₁₀ = 1000 ohms, 0.5 watt |
| CR = reference diode, 12 V, 1 watt | R ₃ = 2000 ohms, 0.5 watt | R ₉ = potentiometer, 1000 ohms, 0.5 watt |
| | R ₅ = 570 ohms, 0.5 watt | |

14-29 VOLTAGE REGULATOR, SERIES TYPE (cont'd)

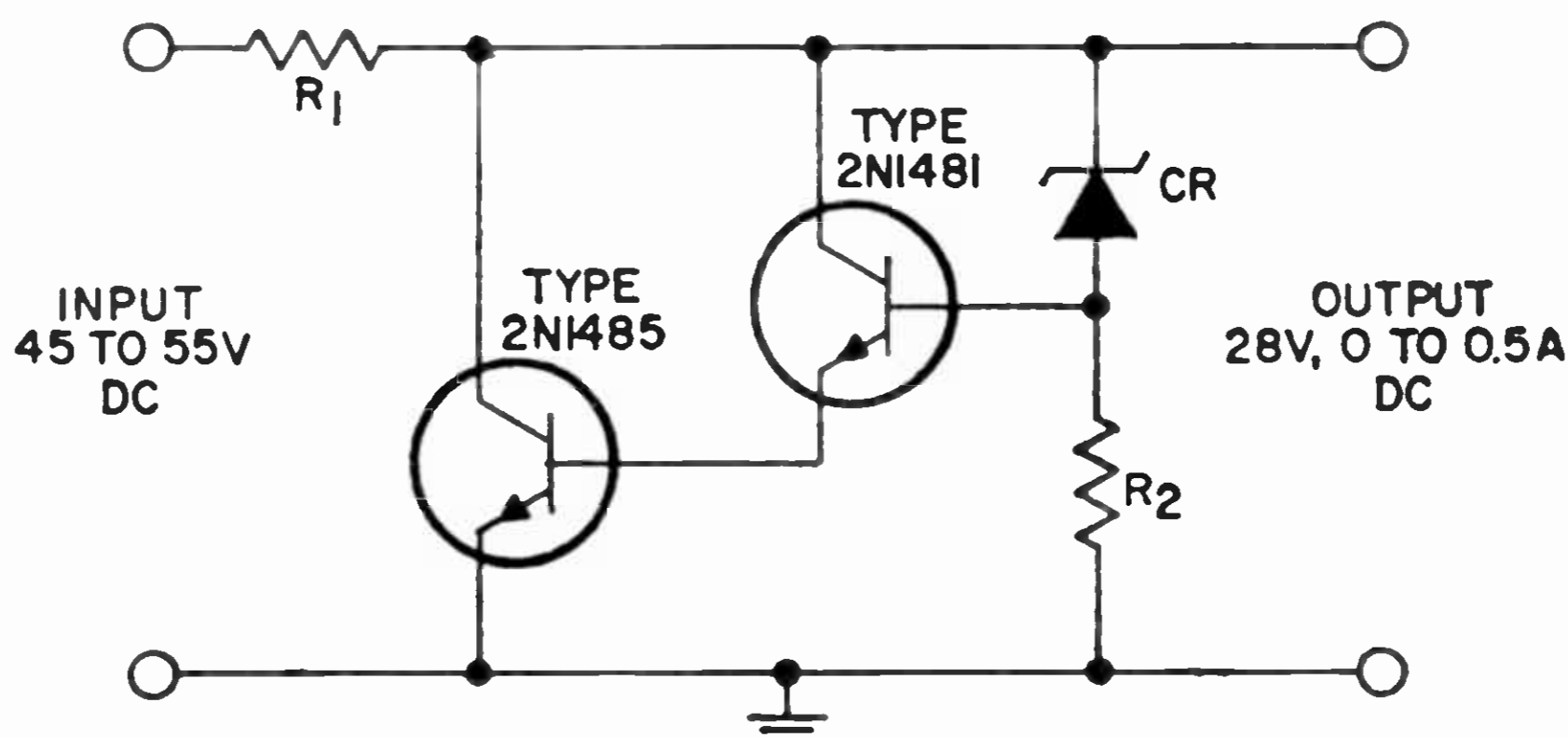
Circuit Description

In this series-type voltage regulator, regulation is accomplished by varying the current through three paralleled 2N3055 transistors connected in series with the load circuit. A reverse-bias-connected Zener diode provides the reference voltage for the circuit. The voltage drop across this diode remains constant at the reference potential of 12 volts over a wide range of current through the diode.

If the output voltage tends to rise for any reason, the total increase in voltage is distributed across bleeder resistors R_8 , R_9 , and R_{10} . If potentiometer R_9 , the output-voltage adjustment, is set to the mid-point of its range, one-half the increase in output voltage is applied to the base of the 2N3053 transistor Q_6 . This increased voltage is coupled (through the emitter-to-base junction of transistor Q_6) to the base of the 2N3053 transistor Q_1 by R_5 , the common emitter resistor for the two transistors. The reference diode CR and its series resistor R_3 are connected in parallel with the bleeder resistors, and the increase in output voltage is also reflected across the diode-resistor network. However, because the voltage drop across CR remains constant, the full increase in voltage is developed across R_3

and thus is applied directly to the base of Q_1 . Because the increase in voltage at the base is higher than that at the emitter, the collector current of the transistor Q_1 increases.

As the 2N3053 collector current of Q_1 increases, the base voltage of the 2N1479 transistor Q_2 decreases by the amount of the increased drop across R_1 . The resultant decrease in current through the 2N1479 transistor Q_2 causes a decrease in the emitter voltage of this transistor. The resultant decrease in current through transistor Q_2 causes a decrease in the emitter voltage and thus in the base voltage of the 2N3055 transistor Q_3 . Similar action by Q_3 results in a negative-going voltage at the base of each of the three 2N3055 transistors Q_4 , Q_5 , and Q_7 . As a result, the current through these transistors, and through the load impedance in series with them, decreases. The decrease in load current tends to reduce the voltage developed across the load circuit to cancel the original tendency for an increase in the output voltage. Similarly, if the output voltage tends to decrease, the current through the three paralleled 2N3055 transistors and through the load circuit increases, so that the output voltage remains constant.

14-30 VOLTAGE REGULATOR, SHUNT TYPE
Regulation 0.5%

Parts List

CR = reference diode, 27 V, 0.5 watt
 R_1 = 28 ohms, 50 watts (in-

cludes source resistance of transformers, rectifiers,

etc.)
 R_2 = 1000 ohms, 0.5 watt

14-30 VOLTAGE REGULATOR, SHUNT TYPE (cont'd)

Circuit Description

This simple two-transistor shunt-type voltage regulator can provide a constant (within 0.5 per cent) dc output of 28 volts for load currents up to 0.5 ampere and dc inputs from 45 to 55 volts. The two transistors operate as variable resistors to provide the output regulation. A 27-volt Zener reference diode is used as the control, or sensing, element for the circuit.

With a 28-volt output, the reverse-bias-connected reference diode, CR, operates in the breakdown-voltage region. In this region, the voltage drop across the diode remains constant (at the reference potential of 27 volts) over a wide range of reverse currents through the diode.

The output voltage tends to rise with an increase in either the applied voltage or the load-circuit impedance. The current through resistor R_2 and reference diode CR then increases. However, the voltage drop across CR remains constant at 27 volts, and the full increase in the output voltage is developed across R_2 . This increased voltage across R_2 is directly coupled to the base of the 2N1481 transistor and increases the forward bias so that the 2N1481 conducts more heavily.

The rise in the emitter current of the 2N1481 increases the forward bias on the 2N1485, and the current through this transistor also increases.

As the increased currents of the transistors flow through resistor R_1 , which is in series with the load impedance, the voltage drop across R_1 becomes a larger proportion of the total applied voltage. In this way, any tendency for an increase in the output voltage is immediately reflected as an increased voltage drop across R_1 so that the output voltage delivered to the load circuit remains constant.

If the output voltage tends to decrease slightly, the voltage drop across reference diode CR still remains constant, and the full decrease occurs across R_2 . As a result, the forward bias of both transistors decreases so that less current flows through R_1 . The resultant decrease in the proportional amount of the applied voltage dropped across this resistor immediately cancels any tendency for a decrease in the output voltage, and the voltage applied to the load circuit again remains constant.

14-31 LIGHT MINDER FOR AUTOMOBILES

Circuit Description

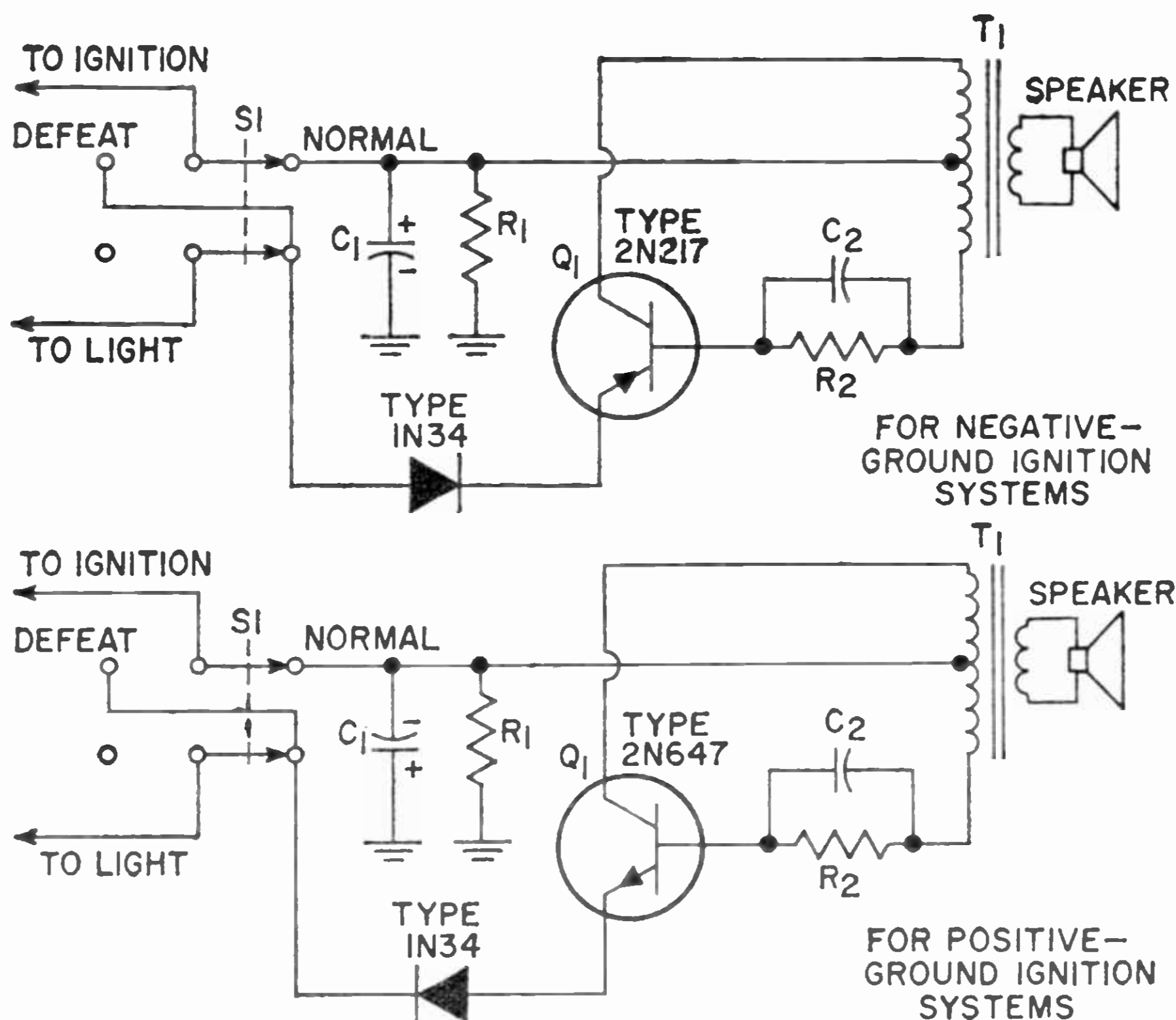
This light-minder circuit sounds an alarm if the lights of a car are left on when the ignition is turned off. The alarm stops when the lights are turned off. When the lights are intentionally left on for a period of time, the alarm can be defeated so that no warning sounds. The alarm then sounds when the ignition switch is turned on as a reminder that the system has been defeated and the switch should be returned to its "normal" position.

The circuit is essentially an oscillator that obtains its supply volt-

age from two possible sources, the ignition system or the light system of the car. In the "normal" mode of operation, the ignition system is connected to the collector circuit of the 2N217 (or 2N647) transistor, and the light system is connected through the 1N34 diode to the 2N217 (or 2N647) emitter. When the ignition switch is on, the collector of the transistor is at the supply voltage. If, at the same time, the lights are on, the emitter of the transistor is also at the supply voltage. Because both the emitter and the collector

14-31

LIGHT MINDER FOR AUTOMOBILES (cont'd)



Parts List

$C_1 = 30 \mu\text{F}$, electrolytic,
25 volts
 $C_2 = 0.22 \mu\text{F}$, 15 volts
 $R_1 = 15000$ ohms, 0.5 watt
 $R_2 = 680$ ohms, 0.5 watt

$S_1 =$ switch, double-pole,
double-throw
Speaker = $1\frac{1}{2}$ -inch permanent-
magnet type; voice-
coil impedance, 3.2 ohms

$T_1 =$ audio-output trans-
former; 400-ohm pri-
mary, 3.2-ohm secondary;
Stancor No. TA-42 or
equiv.

Circuit Description (cont'd)

are at the same voltage, the circuit does not oscillate and no alarm sounds. When the ignition is turned off, the collector is returned to ground through R_1 and C_1 , but the emitter remains at the supply voltage and provides the necessary bias for the circuit to oscillate. Turning the lights out removes the supply voltage and stops the oscillation.

In the "defeat" mode of operation, the ignition system is connected through the 1N34 diode to the emitter of the transistor, and the light system is completely disconnected. The lights can then be turned on without the alarm sounding. When the ignition is turned on, it supplies the necessary voltage to the emitter of the transistor to cause the alarm to sound.

14-32

BATTERY CHARGERS

For 6- and 12-Volt Automobile Batteries

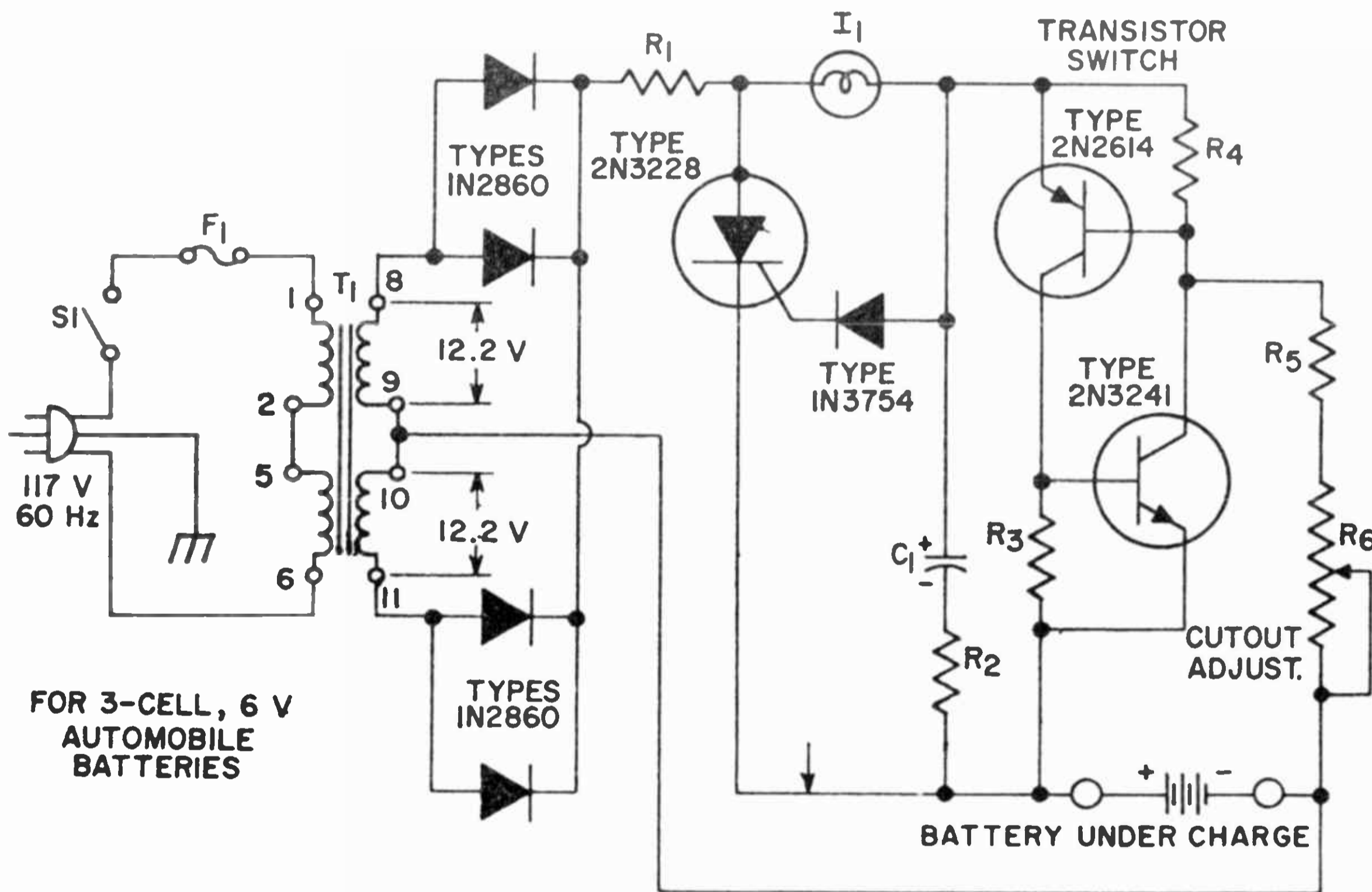
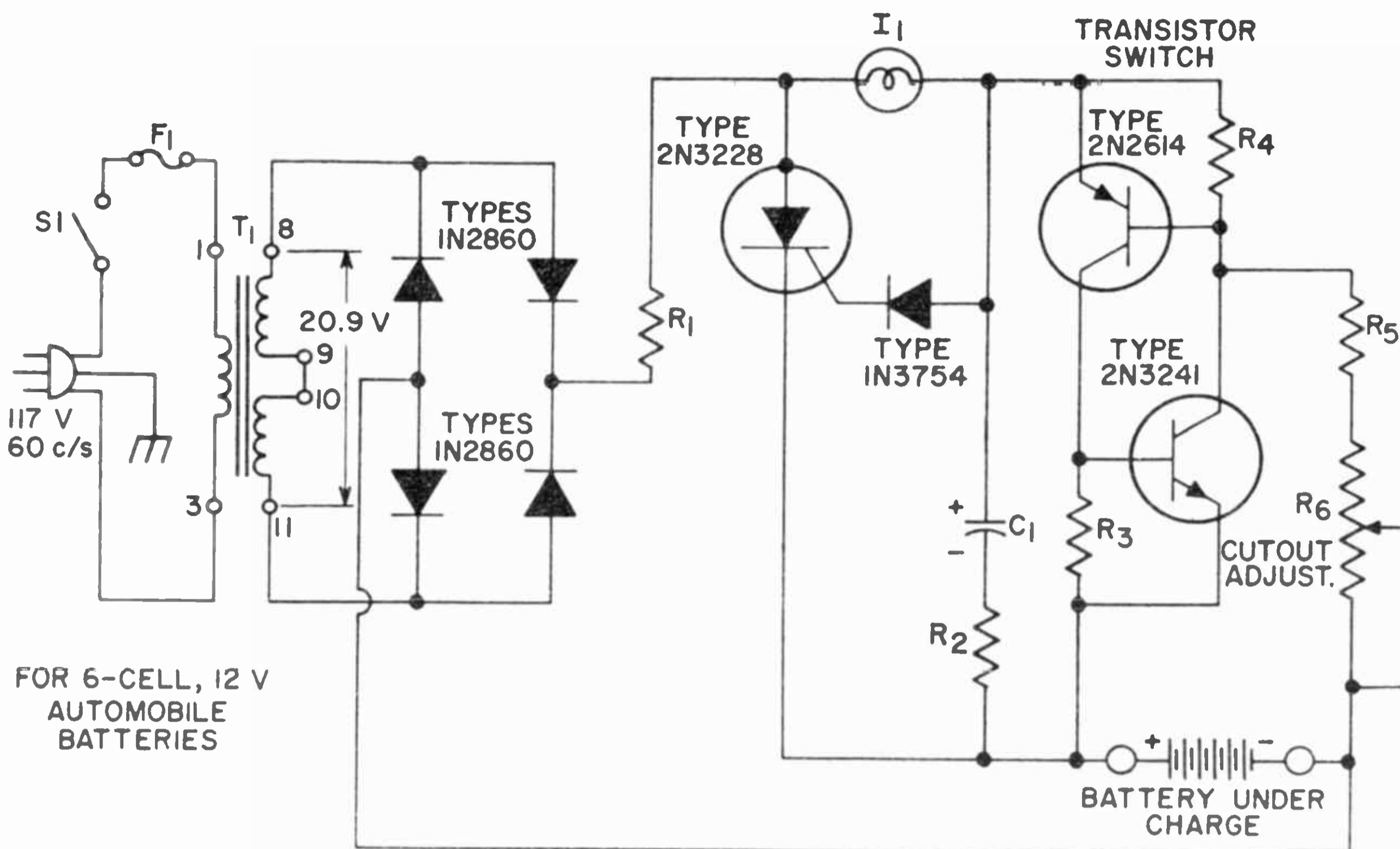
Circuit Description

These battery chargers can be used to recharge run-down batteries in automobiles and other vehicles without removing them from their original mounting and without the need for constant attention. When

the battery is fully charged, the charger circuits automatically switch from charging current to "trickle" charge, and an indicator lamp lights to provide a visual indication of this condition.

14-32

BATTERY CHARGERS (cont'd)



NOTE: Heat sinks are required for the 1N2860 rectifiers. A simple, effective method is to mount the rectifiers in fuse clips.

Parts List

- $C_1 = 50 \mu\text{F}$, electrolytic, 15 V
- $F_1 =$ fuse, 1-ampere, 3 AG
- $I_1 =$ pilot lamp, No. 1488 (14 V, 150 mA) for 12-volt system or No. 47 (6.3 V, 150 mA) for 6-volt system
- $R_1 = 5$ ohms, 20 watts for 12-volt system or 2 ohms, 25 watts for 6-volt system
- $R_2 = 33$ ohms, 0.5 watt
- $R_3 = 470$ ohms, 0.5 watt
- $R_4 = 150$ ohms, 0.5 watt
- $R_5 = 1800$ ohms, 0.5 watt
- $R_6 =$ potentiometer, cutoff adjustment, 10000 ohms, 2 watts
- $S_1 =$ toggle switch, single-pole, single-throw, 3-ampere, 125-volt
- $T_1 =$ power transformer, Stancor No. RT-202, or equiv.

14-32

BATTERY CHARGERS (cont'd)**Circuit Description (cont'd)**

12-Volt Battery Charger—This circuit can be used to charge 6-cell, 12-volt lead storage batteries at a maximum charging rate of 2 amperes. When switch S_1 is closed, the rectified current produced by the four 1N2860 silicon diodes in the full-wave bridge rectifier charges capacitor C_1 through resistors R_1 and R_2 and the No. 1488 indicator lamp, I_1 . As C_1 charges, the anode of the 1N3754 diode is rapidly raised to a positive voltage high enough so that the diode is allowed to conduct. Gate current is then supplied to the 2N3228 SCR to trigger it into conduction. The SCR and the battery under charge then form essentially the full load on the bridge rectifier, and a charging current flows through the battery that is proportional to the difference in potential between the battery voltage and the rectifier output. Resistor R_1 limits the current to a safe value to protect the 1N2860 rectifier diodes in the event that the load is a "dead" battery. The energy stored in C_1 assures that the SCR conducts and, thereby, that the charging current flows for practically the full 180 degrees of each successive half-cycle of input until the battery is fully charged. (The SCR is actually cut off near the end of each half-cycle but is re-triggered shortly after the beginning of each succeeding half-cycle by the gate current applied through the 1N3754 diode as a result of the steady potential on C_1 .)

When the battery is fully charged, the two-transistor regenerative switch is triggered into conduction

(the triggering point is preset by means of potentiometer R_6). As a result of the regenerative action, the 2N2614 and 2N3241 transistors in the switch are rapidly driven to saturation and thus provide a low-impedance discharge path for C_1 . The capacitor then discharges through these transistors and resistor R_2 to about 1 volt (the voltage drop across the transistors). This value is too low to sustain conduction of the 1N3754 diode, and the 2N3228 SCR is not triggered on the succeeding half-cycle of the input. The saturated transistor switch also provides a low-resistance path for the current to the No. 1488 indicator lamp, which glows to signal the fully charged condition of the battery. The current in the lamp circuit (R_1 , lamp, and transistor switch) provides a "trickle" charge of approximately 150 milliamperes to the battery.

6-Volt Battery Charger—This circuit can be used to charge 3-cell, 6-volt lead storage batteries at a maximum charging rate of 3.2 amperes. It is very similar to the 12-volt battery charger except for the rectifier configuration. In the 6-volt circuit, the four 1N2860 diodes are connected in a full-wave center-tapped rectifier circuit that provides the higher charging current of 3.2 amperes to the 6-volt battery. With the exception of the rectifier circuit, the indicator lamp, and the value used for R_1 , the 6-volt charger is identical to the 12-volt charger and operates in the same way.

14-33

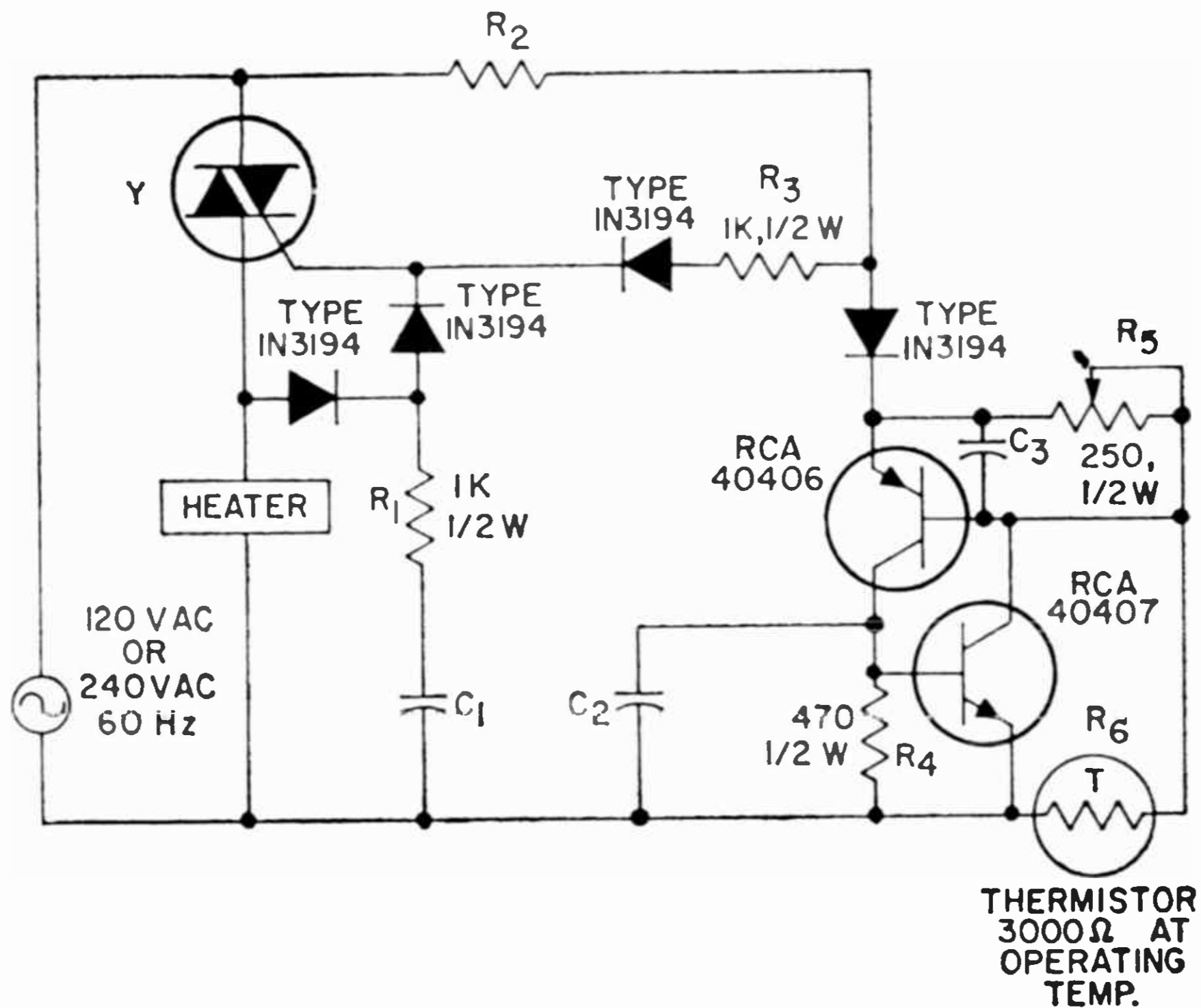
ON-OFF HEAT CONTROL WITH SYNCHRONOUS SWITCHING**Circuit Description**

This triac heat control is useful for the control of resistance-heating elements. It provides synchronous

switching near the beginning of the zero-voltage crossing of the input voltage to minimize rfi interference.

14-33

ON-OFF HEAT CONTROL WITH SYNCHRONOUS SWITCHING (cont'd)



Parts List

$C_1 = 0.5 \mu\text{F}$, 200 V for 120-volt operation; or $0.5 \mu\text{F}$, 400 volts for 240 volt operation
 $R_1, R_3 = 1000$ ohms, 0.5 watt

$R_2 = 2200$ ohms, 5 watts for 120-volt operation; or 3900 ohms, 5 watts for 240-volt operation
 $R_4 = 470$ ohm, 0.5 watt

$R_5 = 250$ ohms, 0.5 watt
 $R_6 =$ Thermistor, negative-temperature coefficient, 3000 ohms at the operating temperature

Circuit Description (cont'd)

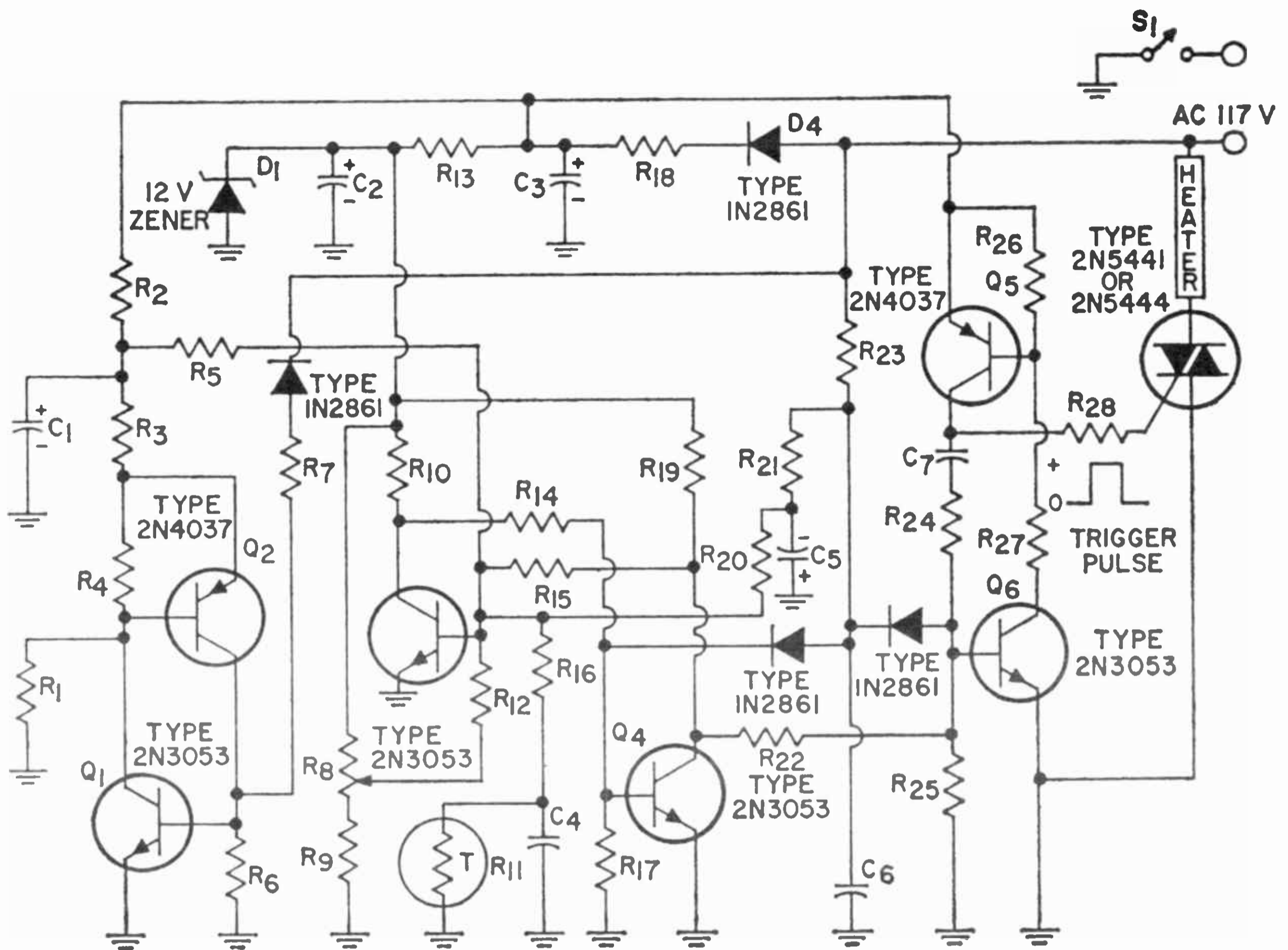
With just a few change in circuit components this heat control can be adapted for operation from either a 120-volt or 240-volt 60-Hz ac source. For 120-volt operation, a 40575 triac is used; for 240-operation, a 40576 triac is used.

A thermistor R_6 controls the operation of a two-transistor regenerative switch that employs a 40406 p-n-p transistor and a 40607 n-p-n transistor. The two-transistor switch, in turn, controls the operation of the triac. When the temperature being controlled is low, the resistance of the thermistor is high, and the regenerative switch is OFF. The triac is then triggered directly from the ac line on positive half cycles of the input voltage. When the triac is triggered, essentially the full ac input voltage is applied across the heater load, and capacitor C_1 charges to approximately the peak value of the input ac voltage. During the negative half cycle of the

input ac voltage this capacitor discharges through resistor R_1 , the 1N3194 diode D_1 , and the triac gate to trigger the triac into conduction. The slaving network formed by capacitor C_1 , resistor R_1 , and diode D_1 assures that the triac is triggered on negative half cycles of the input ac voltage after it has been triggered on the positive half cycles to provide integral cycles of ac power to the heater load.

When the temperature being controlled rises to the desired value, as sensed by the thermistor R_6 , the two-transistor regenerative switch conducts at the beginning of the positive alternation of the input-voltage cycle to shunt the trigger current away from the gate of the triac. The triac does not conduct as long as the resistance of the thermistor is small enough so that the regenerative switch is turned on before the triac can be triggered.

14-34 PROPORTIONAL INTEGRAL-CYCLE HEAT CONTROL



Parts List

$C_1 = 100 \mu\text{F}$, electrolytic, 10 V
 $C_2 = 10 \mu\text{F}$, electrolytic, 15 V
 $C_3 = 50 \mu\text{F}$, electrolytic, 25 V
 $C_4 = 0.1 \mu\text{F}$, 50 V
 $C_5 = 1 \mu\text{F}$, electrolytic, 3 V
 $C_6 = 0.01 \mu\text{F}$
 $C_7 = 0.03 \mu\text{F}$
 $R_1 = 0.15 \text{ megohm}$, 0.5 watt, 10%
 $R_2, R_6, R_{19}, R_{21}, R_{23} = 33000 \text{ ohms}$, 0.5 watt, 10%
 $R_3 = 47 \text{ ohms}$, 0.5 watt, 10%
 $R_4 = 6800 \text{ ohms}$, 0.5 watt, 10%

$R_5 = 0.1 \text{ megohm}$, 0.5 watt, 10%
 $R_7 = 0.12 \text{ megohm}$, 0.5 watt, 10%
 $R_8 = \text{temperature control potentiometer}$, 10000 ohms, 0.5 watt
 $R_9 = 1800 \text{ ohms}$, 0.5 watt, 10%
 $R_{10}, R_{27} = 3300 \text{ ohms}$, 0.5 watt, 10%
 $R_{11} = \text{thermistor}$, negative temperature coefficient, 3000 ohms at operating temperature
 $R_{12}, R_{20} = 15000 \text{ ohms}$, 0.5 watt, 10%
 $R_{13} = 1200 \text{ ohms}$, 0.5 watt, 10%
 $R_{14}, R_{15} = 22000 \text{ ohms}$, 0.5

watt, 10%
 $R_{16} = 120 \text{ ohms}$, 0.5 watt, 10%
 $R_{17} = 2700 \text{ ohms}$, 0.5 watt, 10%
 $R_{18} = 2700 \text{ ohms}$, 2 watts, 10%
 $R_{22} = 8200 \text{ ohms}$, 0.5 watt, 10%
 $R_{24} = 4700 \text{ ohms}$, 0.5 watt, 10%
 $R_{25} = 1500 \text{ ohms}$, 0.5 watt, 10%
 $R_{26} = 2200 \text{ ohms}$, 0.5 watt, 10%
 $R_{28} = 1000 \text{ ohms}$, 0.5 watt, 10%
 $S_1 = \text{ON-OFF switch}$, single-pole, single-throw, toggle

Circuit Description

In this circuit, a fixed-frequency sawtooth (ramp) voltage is summed with a dc control voltage to control the switching of a 2N5441 or 2N5444 triac connected in series with the heater load and 117-volt ac source voltage. The ramp generator establishes the period, or time base, for the system. The dc control voltage is supplied by a temperature-sensing network. As the ramp volt-

age rises, a level is reached which causes the triac to be triggered, and ac power is applied to the heating elements. As the temperature at the sensor changes, the level of the dc control voltage shifts accordingly, and changes the length of time that power is applied to the heating elements within the established period.

When the demand for heat is high, the dc control signal is high and a

14-34 PROPORTIONAL INTEGRAL-CYCLE HEAT CONTROL (cont'd)

Circuit Description (cont'd)

relatively large amount of power is applied to the heating elements. When the demand is completely satisfied, the dc control signal is low, and only a small amount of power is supplied to the heating elements. Usually, this proportional integral-cycle heat control operates continuously somewhere between full ON and full OFF to satisfy the demand for heat.

The ramp voltage is generated by charging of capacitor C_1 through resistor R_2 for approximately 2 seconds for the values given for this circuit. The length of the ramp is determined by the voltage magnitude required to trigger the regenerative switch consisting of the 2N3053 n-p-n and 2N4037 p-n-p transistors Q_1 and Q_2 . The temperature sensor consisting of the 2N3053 transistors Q_3 and Q_4 , together with the controlling thermistor R_{11} , establishes a voltage level at the base of transistor Q_3 which depends upon the resistance value of the thermistor.

Transistors Q_3 and Q_4 form a bistable multivibrator. The state of the multivibrator depends upon the base bias of Q_3 . When Q_3 is conducting, Q_4 is cut off. The pulse generator is energized and generates pulses to trigger the triac. The pulse generator is essentially another two-transistor regenerative switch which also uses a 2N4037 transistor Q_5 and a 2N3053 transistor Q_6 . The output of the pulse generator is synchronized to the line voltage on the negative half-cycle by the 1N2861 diode D_5 and resistor R_{14} and on the positive half-cycle by the 1N2861 diode D_4 and resistor R_{14} . The pulses are, therefore, generated at the zero-voltage crossings and trigger the triacs into conduction at only these points. This synchronous switching minimizes the generation of high-frequency transients that could interfere with the rf circuits of nearby equipment. As a result, no rfi suppression artworks are required.

14-35 SHIFT REGISTER OR RING COUNTER

Circuit Description

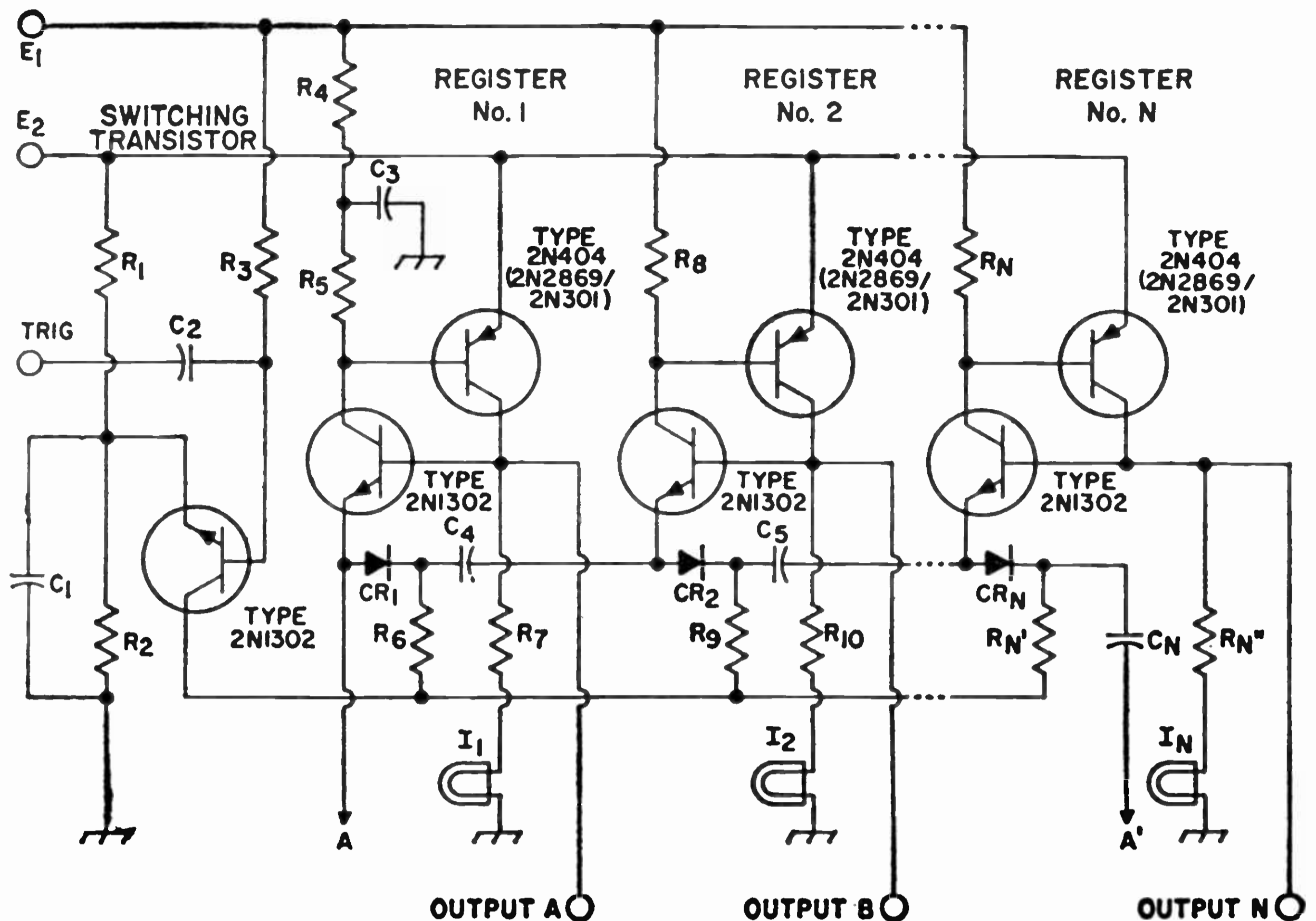
In this basic shift register, the successive outputs from the various stages are delayed (or shifted) from those of the preceding stages by a controlled time interval (i.e., the duration between input trigger pulses). These outputs are coupled through OR gates (not shown on circuit schematic) and may be used to program the timing sequence for various digital switching operations. If point A' on the circuit is connected to point A, the register becomes regenerative and may be used as a ring counter.

The dc supply voltages E_1 and E_2 are obtained from separate taps on a resistive voltage divider. With these voltages applied, the 2N1302 switching transistor is immediately triggered into conduction by the

positive voltage applied to its base through R_3 . One of the register stages must be triggered simultaneously to provide a complete path for the current through the switching transistor.

Each register stage is basically a two-transistor regenerative switch that employs an n-p-n triggering transistor and a p-n-p output transistor. For the E_1 and E_2 voltages used (see notes below circuit schematic), the n-p-n transistor is a 2N1302, and the p-n-p transistor is a 2N404 or a 2N2869/2N301 depending upon the level of output current desired. If either of the transistors in a register stage starts to conduct, both of them are quickly driven into saturation by the regenerative action of the stage. The relatively high

14-35 SHIFT REGISTER OR RING COUNTER (cont'd)

**NOTES:**

The shift register may use as many stages as desired and may be made regenerative by connecting points A and A'. In addition, the basic circuit can be adapted for operation at many different output-current levels. The circuit as shown is designed for an output-current level of 40 mA ($E_1 = 12$

V; $E_2 = 9$ V). Transistor types and component values shown in parentheses indicate the changes necessary for operation at an output-current level of 3 amperes ($E_1 = 27$ V; $E_2 = 24$ V). The voltages E_1 and E_2 should be obtained from a well-regulated dc power supply.

Parts List

$C_1 = 100 \mu\text{F}$, electrolytic, 6 V
 $C_2, C_4, C_5, C_N = 0.05 \mu\text{F}$ (or $0.1 \mu\text{F}$), ceramic, 50 V
 $C_3 = 1 \mu\text{F}$, (or $25 \mu\text{F}$), electrolytic, 25 V
 $CR_1, CR_2, CR_N =$ crystal diode 1N270 or equiv.
 $I_1, I_2, I_N =$ indicator lamp

No. 49; 2-volt, 60-mA (or No. 1488; 14-volt, 150-mA)
 $R_1 = 1000$ ohms, 0.5 watt (or 680 ohms, 1 watt)
 $R_2 = 27$ ohms, 0.5 watt (or 12 ohms, 1 watt)
 $R_3 = 1000$ ohms, 0.5 watt
 $R_4 = 1000$ ohms, 0.5 watt (or

330 ohms, 0.5 watt)
 $R_5, R_8, R_N = 2200$ ohms, 0.5 watt (or 680 ohms, 0.5 watt)
 $R_6, R_9, R_N' = 560$ ohms, 0.5 watt (or 180 ohms, 1 watt)
 $R_7, R_{10}, R_N'' = 150$ ohms, 1 watt (or 82 ohms, 2 watts)

Circuit Description (cont'd)

current from the p-n-p transistor in the stage flows through the resistance that exists between the E_1 and E_2 taps on the power-supply voltage divider. The increased voltage drop across this resistance reduces the E_2 voltage to a value less than that required to trigger the other register stages, and these stages are held inoperative.

When power is initially applied to the circuit, C_3 and R_4 assure that the first register stage is triggered into

conduction before current flows through any of the other register stages. When the power is first applied, the initial surge of current through C_3 and R_4 immediately triggers the 2N1302 transistor in the first stage into conduction. This transistor and the p-n-p output transistor are then quickly driven into saturation by the regenerative action of the stage. No other register stage is then allowed to conduct, and the lamp I_1 in the collector of the

14-35 SHIFT REGISTER OR RING COUNTER (cont'd)

Circuit Description (cont'd)

p-n-p transistor in the first stage lights to indicate that the output is being supplied by this stage. This condition is maintained until an input trigger pulse is applied. During this period, C_4 charges through diode CR_1 , the 2N1302 transistor, and resistors R_4 and R_5 to the E_1 voltage less the sum of the voltages dropped across the other components in the charging path.

A negative trigger pulse is applied to the base of the 2N1302 switching transistor to initiate a register shift. A sufficiently large negative pulse will drive the switching transistor to cut off. All the register stages are then held inoperative for the duration of the trigger pulse. When the trigger pulse is removed, the switching transistor again conducts through one of the register stages. This time, however, no quick surge of current can flow through C_3 and R_4 to trigger the first register stage, because C_3 has fully charged to the E_1 voltage.

Moreover, the charge on C_4 tends to reverse-bias diode CR_1 , and thus impedes the flow of current through the first register stage. The charge on C_4 , however, is series-aiding with the dc supply voltage in the second register stage. This series-aiding effect causes the second stage to be triggered into conduction before current can flow through any of the other stages. The biasing action of this stage then holds the other stages inoperative. The lamp I_2 then lights to indicate that the output is being supplied by the second stage.

When the next register shift is initiated by a negative trigger pulse, the charge on C_5 assures that the third register stage will be triggered to supply the output. In this way, the operation of the register is shifted from one stage to the next each time a negative trigger pulse is applied. The register can be reset so that the operation starts with the first stage at any time by discharging capacitor C_3 .

14-36

ASTABLE MULTIVIBRATOR

(Frequency = 7000 Hz)

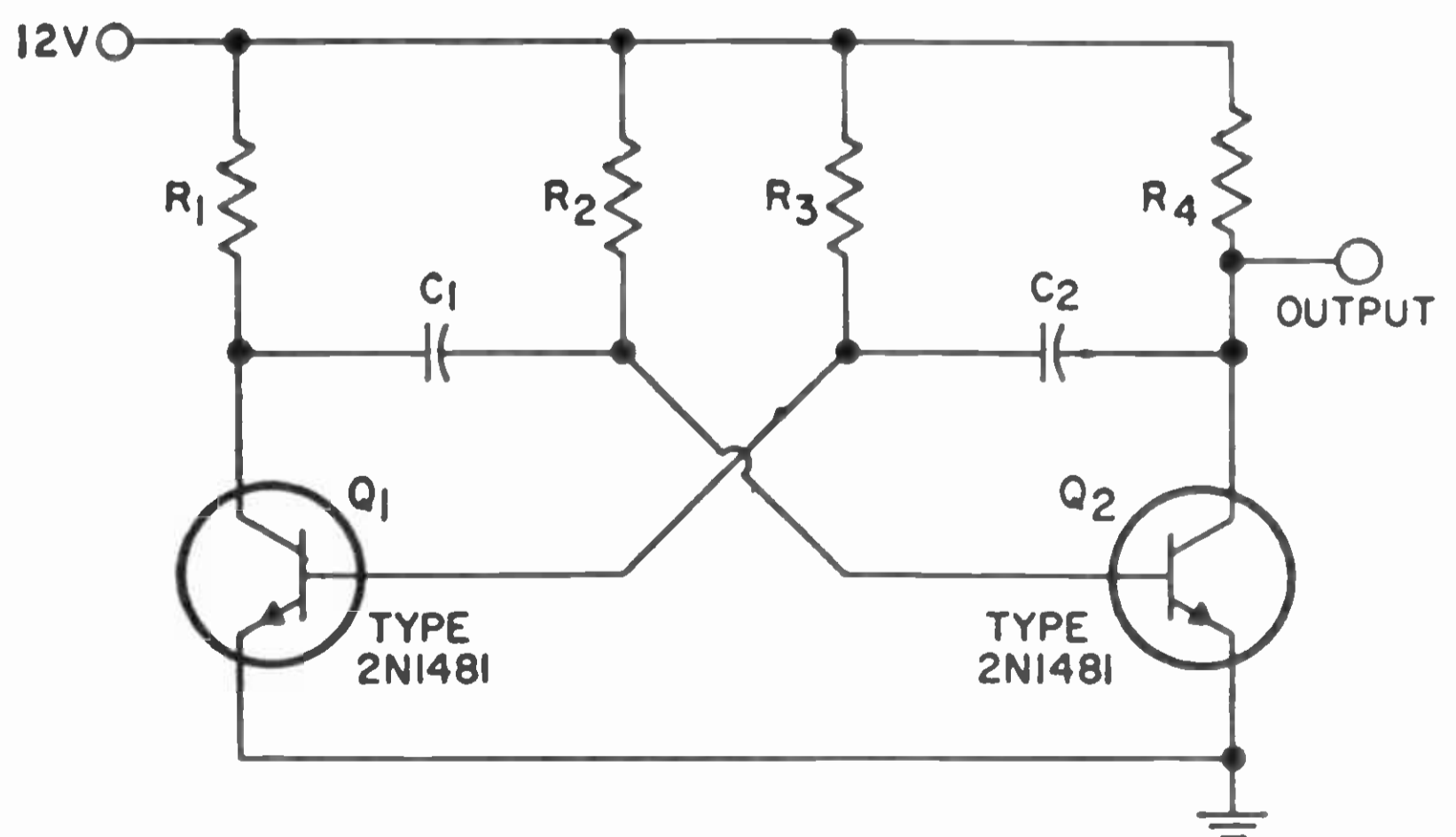
$$f = \frac{1}{(0.7C_1R_2) + (0.7C_2R_3)}$$

Parts List

$C_1, C_2 = 0.1 \mu\text{F}$, paper, 25 V
 $R_1, R_4 = 60$ ohms, 5 watts
 $R_2, R_3 = 1000$ ohms, 0.5 watt

Circuit Description

This astable (free-running) multivibrator develops a square-wave output that has a peak value equal to the dc supply voltage ($V_{CC} = 12$ volts) and a minimum value equal to the collector saturation voltage of the transistors. The circuit is basic-



ally a two-stage nonsinusoidal oscillator in which one stage conducts at saturation while the other is cut off until a point is reached at which the stages reverse their conditions. The circuit employs two 2N1481 transistors operated in identical

14-36

ASTABLE MULTIVIBRATOR (cont'd)

Circuit Description (cont'd)

common-emitter amplifier stages with regenerative feedback resistance-capacitance coupled from the collector of each transistor to the base of the other transistor.

When power is initially applied to the circuit, the same amount of current tends to flow through each transistor. It is unlikely, however, that a perfect balance will be maintained, and if the current through transistor Q_1 , for example, should increase slightly without an attendant increase in that through transistor Q_2 , the multivibrator will oscillate to generate a square-wave output.

As the current through transistor Q_1 increases, the resultant decrease in collector voltage is immediately coupled to the base of transistor Q_2 by the discharge of capacitor C_1 through resistor R_2 . This negative voltage at the base reduces the current through transistor Q_2 , and its collector voltage rises. The charge of capacitor C_2 through resistor R_3 couples the increase in voltage at the collector of transistor Q_2 to the base of transistor Q_1 , and further increases the flow of current through Q_1 . The collector voltage of Q_1 decreases even more, and the base of Q_2 is driven more negative. As a result of this regenerative action, transistor Q_1 is driven to saturation almost instantaneously, and, just as quickly, transistor Q_2 is cut off. This condition is maintained as long as the discharge current of C_1 develops sufficient voltage across R_2 to hold Q_2 cut off. The time constant of C_1

and R_2 , therefore, determines the time that Q_2 remains cut off (i.e., the duration of the positive half-cycle of the square-wave output). During this period, the voltage at the output terminal is the dc supply voltage (12 volts).

The discharge current from C_1 decreases exponentially, as determined by the time constant of the discharge path, and eventually becomes so small that the voltage developed across R_2 is insufficient to hold Q_2 cut off. The decrease in collector voltage that results when Q_2 conducts is coupled by C_2 and R_3 to the base of Q_1 . The current through Q_1 then decreases, and the collector voltage of this transistor rises. The positive swing of the voltage at the collector of Q_1 is coupled by C_1 and R_2 to the base of Q_2 to increase further the conduction of Q_2 . The regenerative action of the multivibrator then quickly drives Q_2 to saturation and Q_1 to cutoff. The length of time that this condition is maintained is determined by the time constant of C_2 and R_3 . During this period, which represents the negative half-cycle of the square-wave output, the voltage at the output terminal is the collector saturation potential of Q_2 .

If desired, a square-wave output may also be obtained from the collector of transistor Q_1 . This output will be equal in magnitude to that at the collector of transistor Q_2 , but will be opposite in phase.

14-37

LIGHT FLASHER

100 Flashes Per Minute

Circuit Description

In this circuit, a free-running, asymmetrical multivibrator is used to gate the operation of a two-stage amplifier. An incandescent lamp or other load may be connected in series with the collector of the output transistor, and each time the transistor

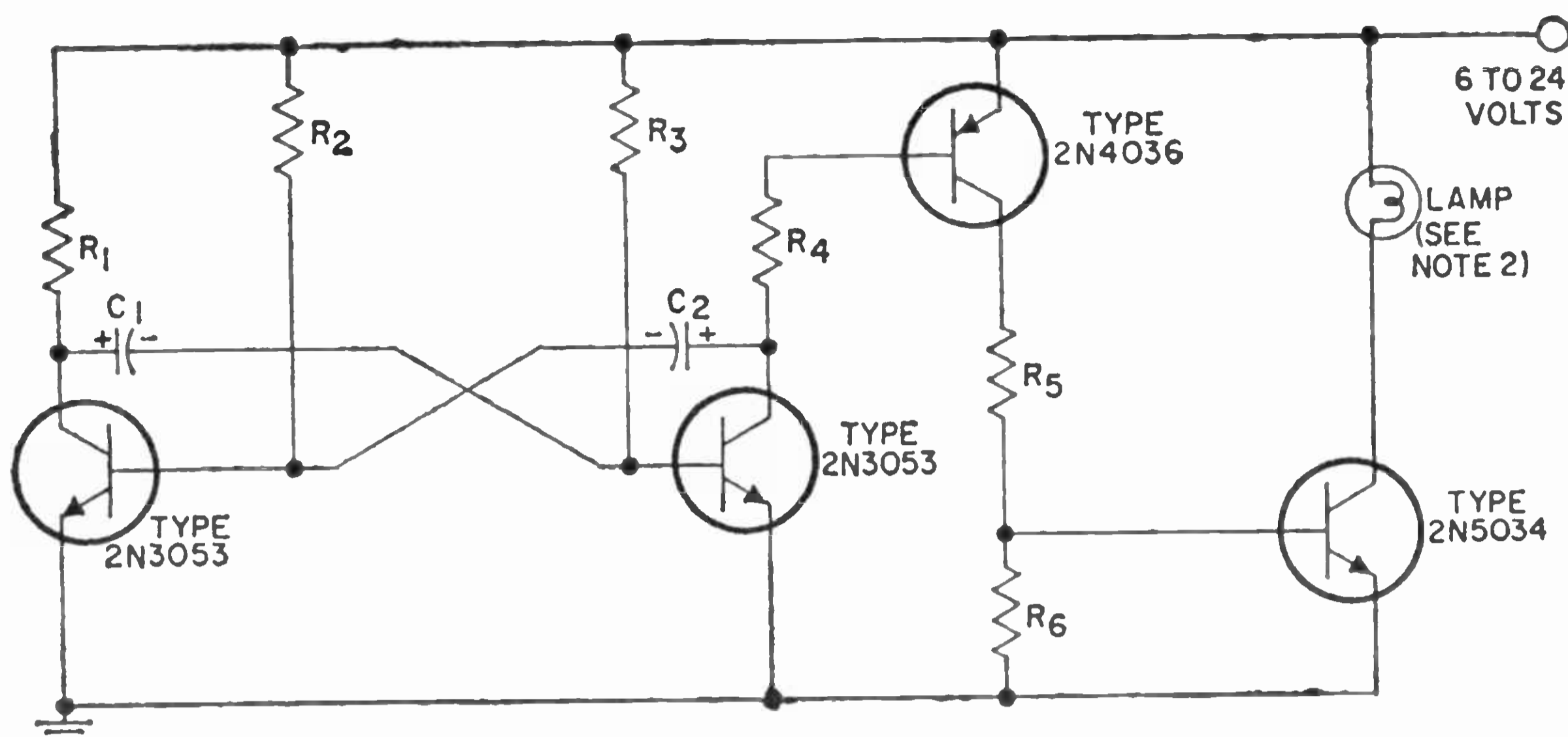
conducts, voltage is applied across the bulb or alternate load. The input power may be any dc voltage from 6 to 24 volts.

The multivibrator uses a pair of 2N3053 transistors. The rectangular wave output developed at the col-

14-37

LIGHT FLASHER (cont'd)

100 Flashes Per Minute



NOTES: 1. Values of capacitors C_1 and C_2 may be changed to alter the flashing rate.
 2. Bulbs and resistive loads up to 2.0 amperes may be used; however, if the flasher circuit is used to switch loads that have inductive components, diode protection must be provided for the 2N5034 output transistor.

Parts List

$C_1 = 25 \mu\text{F}$, electrolytic, 25 V	$R_1 = 2000$ ohms, 0.5 watt	$R_4 = 510$ ohms, 2 watts
$C_2 = 1 \mu\text{F}$, electrolytic, 25 V	$R_2 = 0.1$ megohm, 0.5 watt	$R_5 = 50$ ohms, 10 watts
	$R_3 = 24000$ ohms, 0.5 watt	$R_6 = 100$ ohms, 0.5 watt

Circuit Description (cont'd)

lector of the second transistor is resistively coupled to the base of the 2N4036 p-n-p transistor operated in a common-emitter amplifier stage.

The 2N4036 transistor is gated on and off by the rectangular-wave signal from the multivibrator. This stage in turn gates the operation of the 2N5034 n-p-n transistor used in the output stage. A lamp bulb or alternate load is connected from the positive side of the power supply to the collector of the output-stage transistor. The lamp, therefore, flashes at the frequency of the multivibrator. The frequency of operation, calculated by use of the equation given for circuit 14-36, is approximately 100 flashes per minute.

The repetition rate may be changed by altering the values of capacitors C_1 and C_2 . The ON time changes proportionally with the value of C_2 , and the OFF time changes proportionally with the value of C_1 .

For operation at dc supply voltages less than 24 volts, capacitor working voltages and resistor dissipation ratings may be reduced. Capacitor ratings may be reduced to the maximum supply voltage. The dissipation requirements of the resistors are proportional to the square of the supply voltage, e.g., for 12-volt operation, the dissipation rating for R_5 is required to be only 2.5 watts.

14-38

LIGHT DIMMERS

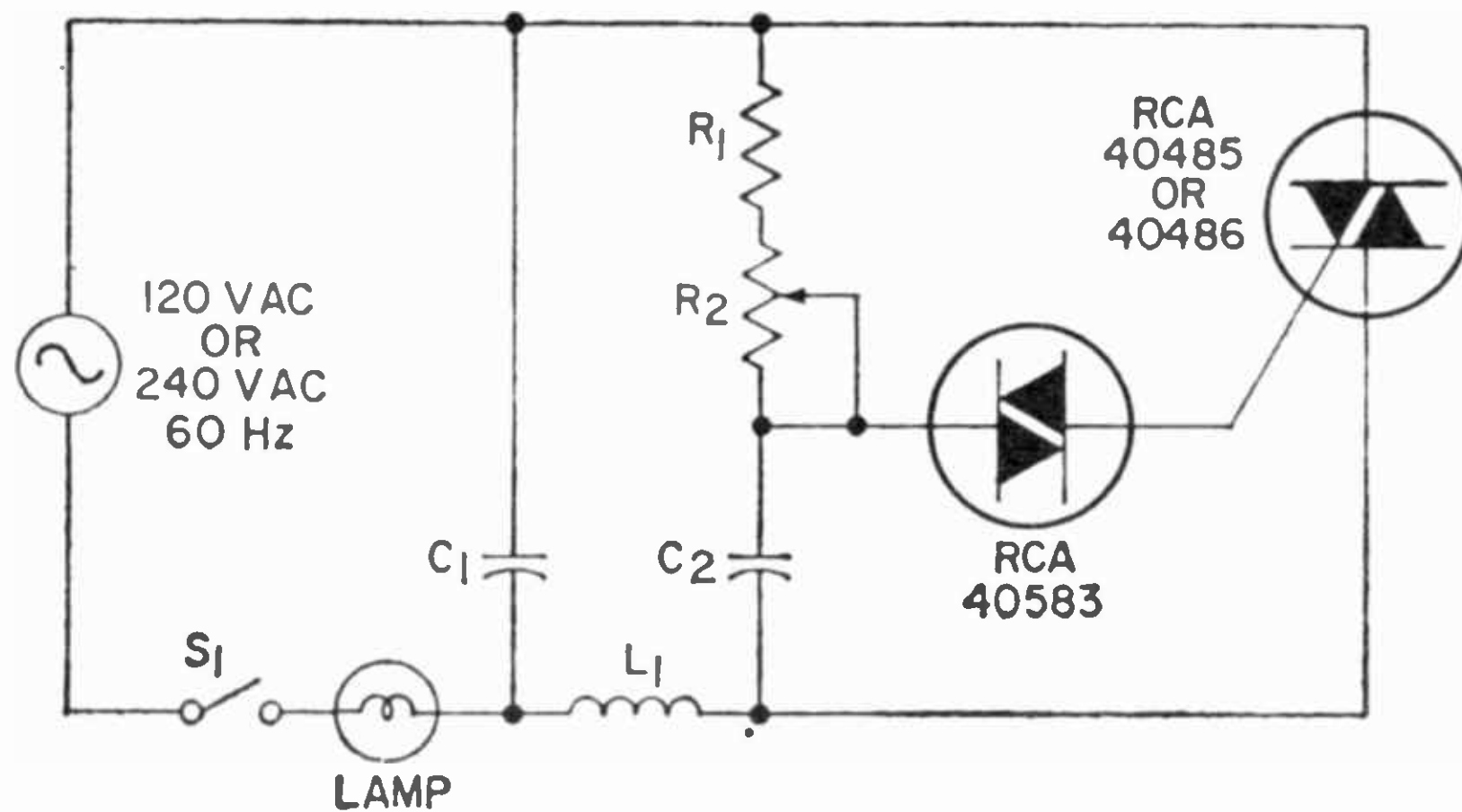
Circuit Description

These triac light-dimmer circuits are designed to provide full-wave control of the light intensity of incandescent lamps. Component values

and triac types are shown for operation of the circuits from a 60-Hz ac source of 120 or 240 volts. For 120-volt operation, the 40485 triac is

14-38

LIGHT DIMMERS (cont'd)



(a) Single-time-constant light-dimmer circuit.

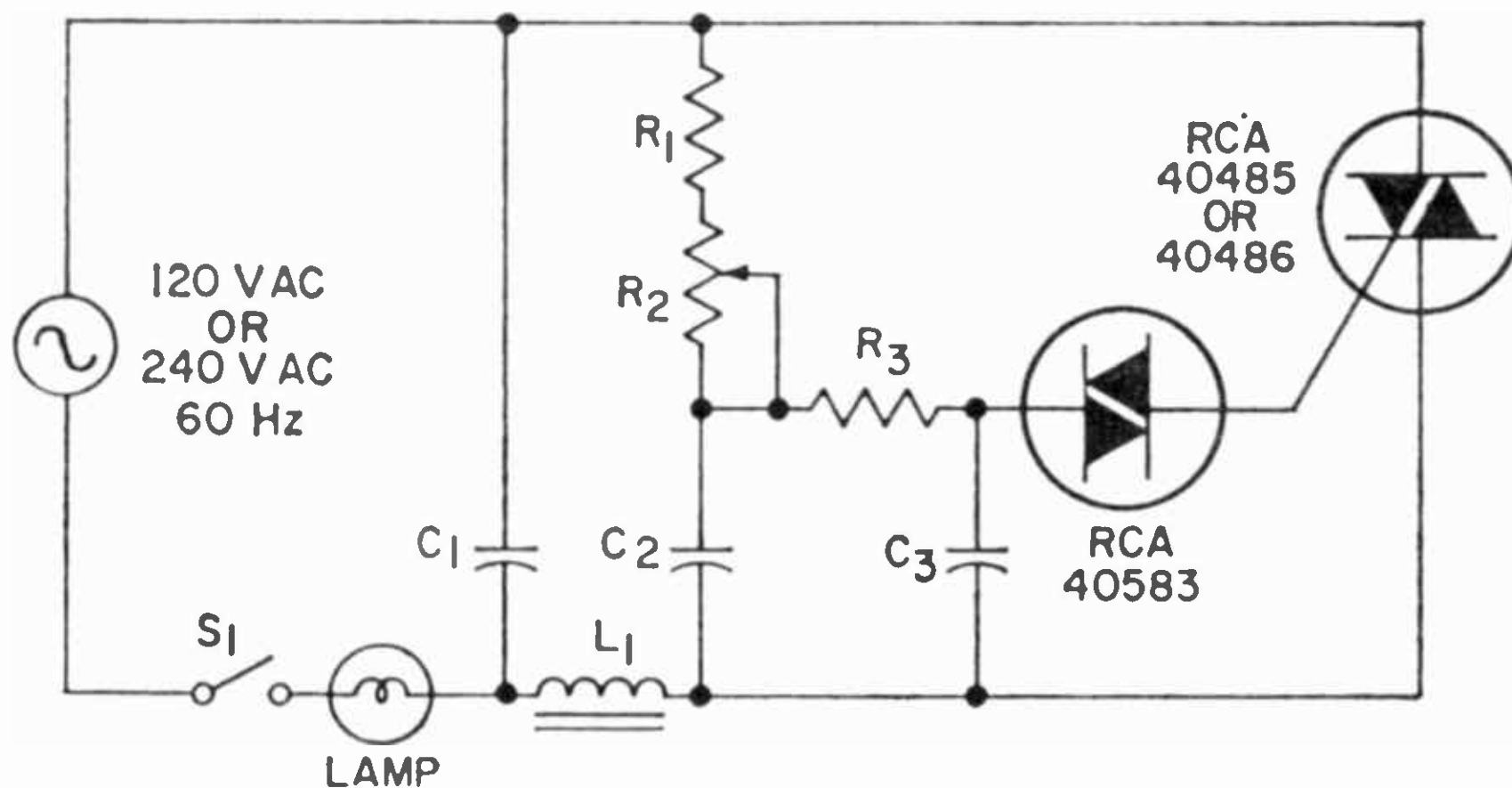
Parts List

120-Volt, 60-Hz Operation
 $C_1, C_2 = 0.05 \mu\text{F}, 100 \text{ V}$
 $L_1 = 100 \mu\text{H}$
 $R_1 = 3300 \text{ ohms}, 0.5 \text{ watt}$
 $R_2 = \text{light control, poten-}$

tiometer, 0.25 megohm,
 0.5 watt

$L_1 = 200 \mu\text{H}$
 $R_1 = 4700 \text{ ohms}, 0.5 \text{ watt}$
 $R_2 = \text{light control, poten-}$
 tiometer, 0.25 megohm,
 1 watt

240-Volt, 60-Hz Operation
 $C_1, C_2 = 0.1 \mu\text{F}, 100 \text{ V}$



(b) Double-time-constant light-dimmer circuit.

Parts List

120-Volt, 60-Hz Operation
 $C_1, C_2, C_3 = 0.1, 200 \text{ V}$
 $L_1 = 100 \mu\text{H}$
 $R_1 = 2200 \text{ ohms}, 0.5 \text{ watt}$
 $R_2 = \text{light control, poten-}$
 tiometer, 0.1 megohm,

0.5 watt

240-Volt, 60-Hz Operation
 $R_3 = 15000 \text{ ohms}, 0.5 \text{ watt}$
 $C_1, C_2, C_3 = 0.1 \mu\text{F}, 400 \text{ V}$

$L_1 = 200 \mu\text{H}$
 $R_1 = 3300 \text{ ohms}, 0.5 \text{ watt}$
 $R_2 = \text{light control, poten-}$
 tiometer, 0.2 megohm,
 1 watt
 $R_3 = 15000 \text{ ohms}, 0.5 \text{ watt}$

Circuit Description (cont'd)

recommended; for 240-volt operation, the higher-power 40486 triac should be used. A 40583 trigger diode (diac), together with associated resistance-capacitance time-constant networks, is used to develop the gate current pulses that trigger the selected triac into conduction. In applications where space is premium,

the triac and associated trigger diode may be replaced by the 40431 for 120-volt operation or the 40432 for 240-volt operation, because these devices combine the functions of both the triac and the diac in the same package.

In each light-dimmer circuit, the triac is connected in series with the

14-38

LIGHT DIMMERS (cont'd)

Circuit Description (cont'd)

lamp load. During the beginning of each half cycle of the input ac voltage, the triac is in the OFF state. As a result, the entire line voltage appears across the triac, and the lamp is not lighted. The entire line voltage, however, is also impressed across the resistance capacitance network connected in parallel with the triac, and this voltage charges the capacitor(s) in this network. When the voltage across the trigger capacitor, C_2 in circuit (a) or C_3 in circuit (b), rises to the breakover voltage V_{BO} of the diac, and the diac conducts. The capacitor then discharges through the diac and the triac gate to trigger the triac. At this point, the line voltage is transferred from the triac to the lamp load for the remainder of that half cycle of the input ac power. This sequence of events is repeated for each half cycle of either polarity.

The potentiometer R_2 is adjusted to control the brightness of the incandescent lamp. If the resistance of the potentiometer is decreased, the trigger capacitor charges more rapidly, and the breakover voltage of the diac is reached earlier in the cycle so that the power applied to the lamp and thus the intensity of the light is increased. Conversely, if the resistance of the potentiometer is increased, triggering occurs later in the cycle, and the light intensity is decreased. The resistor R_1 in series with the potentiometer protects the potentiometer by limiting the current when the potentiometer is at the low-resistance end of its range.

Capacitor C_1 and inductor L_1 form an rfi suppression network. This network suppresses the high-frequency transients generated by the rapid ON-and-OFF switching of the triac so that these transients do not produce noise interference in nearby electrical equipment.

The two lamp-dimmer circuits differ in that circuit (a) employs a

single-time-constant trigger network and circuit (b) uses a double-time-constant trigger circuit. As pointed out earlier in the section on Power Switching and Control, the use of the second time constant network reduces hysteresis effects and thereby extends the effective range of the light-control potentiometer. As applied to light dimmers, the term hysteresis refers to a difference in the control-potentiometer setting at which the lamp turns on and the setting at which the light is extinguished. The additional capacitor C_2 in circuit (b) reduces hysteresis by charging to a higher voltage than capacitor C_3 . During gate triggering, C_3 discharges to form the gate current pulse. Capacitor C_2 , however, has a longer discharge time constant and this capacitor restores some of the charge removed from C_3 by the gate current pulse.

It is important to realize that a triac in these circuits dissipates power at the rate of about one watt per ampere. Therefore, some means of heat removal must be provided to keep the device within its safe operating-temperature range. On a small light-control circuit such as one built into a lamp socket, the lead-in wire serves as an effective heat sink. Attachment of the triac case directly to one of the lead-in wires provides sufficient heat dissipation for operating currents up to 2 amperes (rms). On wall mounted controls operating up to 6 amperes, the combination of face plate and wall box serves as an effective heat sink. For higher-power controls, however, the ordinary face plate and wallbox do not provide sufficient heat-sink area. In this case, additional area may be obtained by use of a finned face plate that has a cover plate which stands out from the wall so air can circulate freely over the fins.

On wall-mounted controls, it is

14-38

LIGHT DIMMERS (cont'd)

Circuit Description (cont'd)

also important that the triac be electrically isolated from the face plate, but at the same time be in good thermal contact with it. Although the thermal conductivity of most electrical insulators is relatively low when compared with metals, a low-thermal-resistance, electrically iso-

lated bond of triac to face plate can be obtained if the thickness of the insulator is minimized, and the area for heat transfer through the insulator is maximized. Suitable insulating materials are fiber-glass tape, ceramic sheet, mica, and polyimide film.

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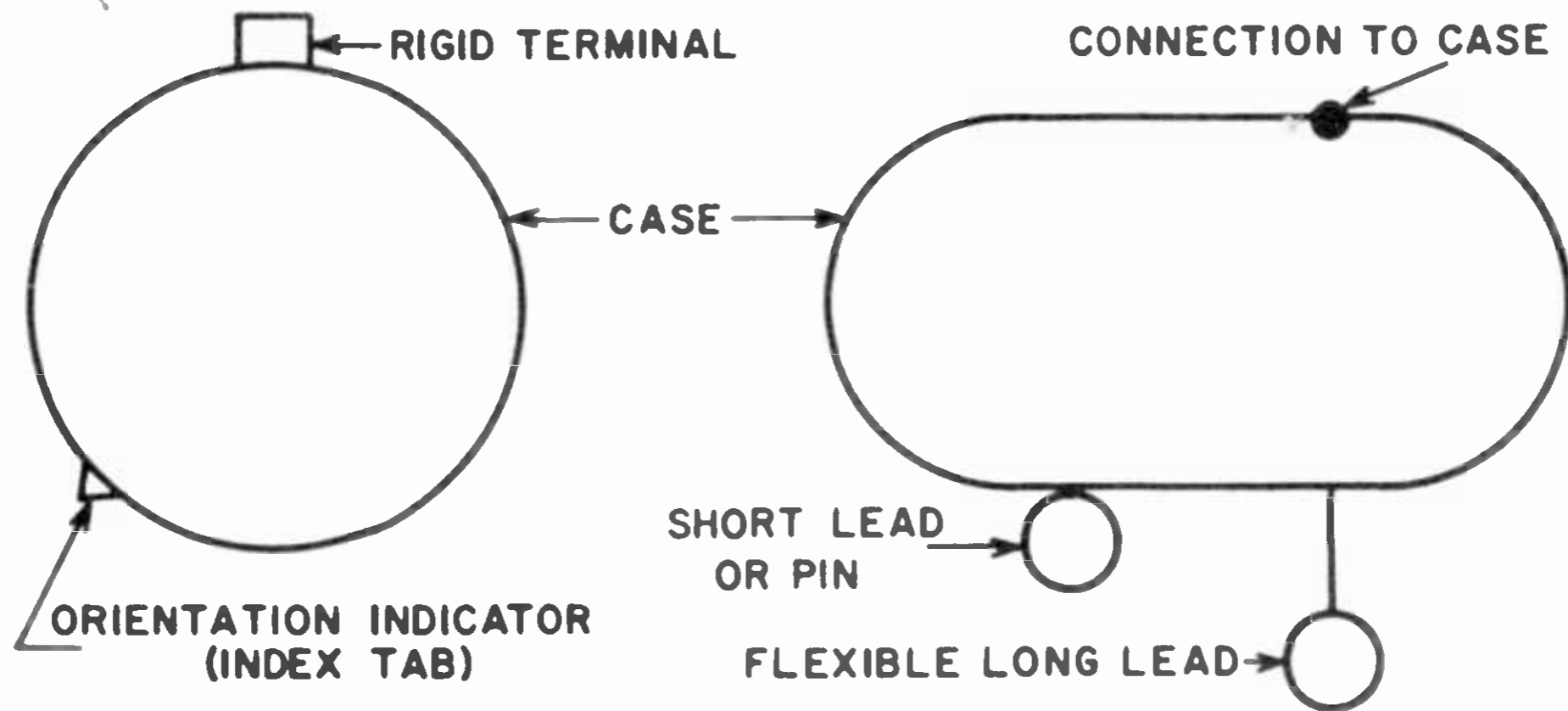
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KEY: TERMINAL-CONNECTION DIAGRAMS (Bottom Views)



A	Anode	G	Gate	K	Cathode
B	Base	HR	Heat Radiator	L	Lug
C	Collector	HS	Heat Sink	S	Source
D	Drain	IG	Insulated Gate	ST	Stud
E	Emitter	IS	Interlead Shield	SUB	Substrate
F	Mounting Flange			MT	Main Terminal

OTHER RCA TECHNICAL MANUALS

RCA Power Circuits (SP-51)	\$2.00
RCA Linear Integrated Circuits (IC-41)	\$2.00
RCA Solid-State Hobby Circuits Manual (HM-90)	\$1.75
RCA Silicon Controlled Rectifier Experimenter's Manual (KM-71) .	\$0.95
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RCA Receiving-Tube Manual (RC-26)	\$1.75
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RCA Transmitting Tube Manual (TT-5)	\$1.00
RCA Transistor Servicing Guide (1A1673)	\$3.50

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