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PROCEEDINGS

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PROCEEDINGS OF THE 1954 WESCON COMPUTER SESSIONS

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A DEPENDENT VARIABLE ANALOG FUNCTION GENERATOR

C. J. Savant, Jr.
University of Southern California Engineering Center
and
R. C. Howard
Bell Telephone Laboratories

Summary

The solution of nonlinear engineering design problems demonstrates the need for a special function generator. The generator described in this paper satisfies this need. The basic components of the unit are discussed and the forms of functions which can be generated are shown. It is concluded from tests on the system that the function generator is a valuable aid in the handling of nonlinear design problems.

Introduction

The engineer need not look far in his work to find a nonlinear problem. The mechanical engineer knows that springs and dashpots are linear in only small regions. Familiar stress-strain diagrams, gas-expansion laws, and even the simple pendulum cannot be described in all regions by linear equations. The electrical engineer is familiar with the saturation of iron-core inductors, nonlinear vacuum tube characteristics and curved torque-speed curves of servo motors. These are just a few of the common relationships which engineers usually linearize in order to obtain a solution based on classical linear theory. Practically all of the characteristics of nature are nonlinear, and the linearizations commonly practiced are approximations, valid only in restricted regions.

Mathematicians have attacked the second-order nonlinear differential equation, and some results have been obtained with iteration and perturbation techniques (Cf. Ref. 1). The problem becomes unwieldy even for small nonlinearities, and hence these methods are not satisfactory for use by engineers. Since the convergence of these methods often depends upon the nonlinearity's being small, the methods are not even applicable when the nonlinearity is large. Numerical integration can always be performed, but the labor involved in finding just one solution is often prohibitive. Topological methods (Cf. Ref. 2) have aided in the solution of second-order systems, but little has been done with higher-order equations by graphical techniques.

Both analog and digital computers have been employed by engineers in the solution of nonlinear equations. In many of these solutions, considerable time is expended in setting the nonlinearity into the computer. Existing techniques do not lend themselves to easy change of the nonlinear function.

The need for a versatile arbitrary function generator of a dependent variable is strongly felt in feedback control system design. For example, consider a control system, the response of which requires improvement. It may be possible to better the performance if appropriate nonlinear functions be added, either in the forward loop or in the feedback path. In determining the nature of this nonlinear function, one is not so concerned with a high degree of accuracy as in the ease of modifying one function into another in an attempt to discover an optimum. The nature of the design problem demands a highly versatile function generator with only a reasonable accuracy (perhaps 5%) required.

The arbitrary function generator discussed in this paper satisfies the needs of the designer

in that the form of the permissible nonlinearities can be changed by the setting of two knobs.

The present function generator boasts another advantage. In many problems it may be necessary to generate products of arbitrary functions of two or more variables. The unit described in this paper permits products of the general form

$$\left[f(t)\right]^{\alpha}\left[g(t)\right]^{\beta}\left[h(t)\right]^{\gamma}$$

where f(t), g(t), and h(t) may be the response variables of a given problem or may be any independent variables. The exponents α, β, and γ may be either positive or negative.

Principles of Operation

The principle of operation of the multiplier is based on the logarithmic function, which has the following property:

$$\alpha \log_a f(x) + \beta \log_a g(y) + \gamma \log_a h(z)$$
$$= \log_a \left\{\left[f(x)\right]^{\alpha}\left[g(y)\right]^{\beta}\left[h(z)\right]^{\gamma}\right\} \qquad (1)$$

where "a" is any number greater than unity.

Since summation is an easy operation with electronic circuits, the logarithms of three voltages can be added simply, and the taking of the inverse logarithm of the sum results in the product. Hence the difficult operation of analog multiplication (or division) is performed easily by adding voltages. Thus the first work centered about the development of two electronic circuits which have the required logarithmic and inverse logarithmic characteristics. This development resulted in two basic units: the log-taking element (LTE), the output of which is the negative logarithm of the input voltage, and the inverse-log-taking element (ILTE), the output voltage of which is the inverse logarithm of the input. These two units plus necessary polarity inverting equipment comprise the arbitrary function generator of a dependent variable.

Linear - to - logarithmic Converter

The log taking element (LTE) is an electronic converter whose output is the negative logarithm of the input voltage. The circuit diagram of this unit is given in Figure 1. The details of the LTE have been reported in a previous paper (Cf. Ref. 3). The important fact to know in connection with the LTE is that for positive input voltages from 0.3 to 300 volts the output has the form:

$$-\log_a e_{in}$$

The output voltage varies over a range of -0.3 to -30 volts with a logarithm base, a, of approximately 1.20.

The LTE units are interchangeable and a drift stability of 75 mv hr. at the output is attained. The accuracy of the logarithmic function can be verified by reference to Figure 2 where the static characteristic is plotted on semi-logarithmic paper.

Inverse - log - taking Element

The underlying concept governing the operation of the inverse-log-taking element, hereafter known as the ILTE, is simple, namely, use of a high-gain amplifier with an LTE in the feedback loop. The operation can best be understood from a consideration of Figure 3. With the symbols defined on the figure, one can readily write the following basic equations of the circuit.

$$\frac{e_f + e_{in}}{2} = \qquad (2)$$

$$\epsilon A = e_o \qquad (3)$$

$$-\log_a e_o = e_f \qquad \text{(valid if } e_{in} > 0) \qquad (4)$$

Combination of equations (2), (3), and (4) results in the expression:

$$\epsilon = \frac{-\log_a e_o + e_{in}}{2} = \frac{e_o}{A} \qquad (5)$$

It A is very large, and positive, equation 5 reduces to

$$e_o = \exp_a e_i \qquad (6)$$

Equation (6) demonstrates tnat the output voltage of the ILTE is proportional to the inverse logarithm of the input voltage.

A more complete analysis shows that

$$e_o = \exp_a \left\{\left[e_{in}\right]\left[1 + (\Delta + 2\delta)\ln a\right]\left[1 + \frac{2}{A} e_o \ln a\right]\right\} \qquad (7)$$

where

δ = drift voltage of amplifier referred to the input.

Δ = drift voltage of LTE referred to the output and A is large but not infinite.

From equation (7) approximate percent-error

expressions resulting from drift and insufficient gain can be obtained as follows:

$$\text{percent error from drift} = E_d \doteq 100(\Delta + 25)\ln a \quad (8)$$

$$\text{percent error from lack of gain} = E_g \doteq \frac{200}{A} e_o \ln a \quad (9)$$

With nominal values $\Delta = 50$ mv, $\delta = 25$ mv, $\alpha = 1.20$, $e_o = 300$ v, $A = 8000$ substituted in equations (8) and (9), the maximum possible errors are

$$E_d = 2.3\% \qquad E_g = 2.1\% \quad (10)$$

With appropriate adjustment of the final unit, E_d can be reduced considerably, and E_g can be eliminated completely. The drift of the ILTE has been observed in operation to be about 1 volt per hour with 3.0 volts out and 3 volts per hour with 300 volts out.

Polarity Inverting Problem: Input

From a purely mathematical point of view, the logarithm of a negative number is complex. When presented with negative input signals, the electronic LTE, however, produces incorrect output voltages since the LTE functions much the same as an amplifier when the grid signal is negative. The response of the LTE is proportional to the logarithm of the input voltage for positive applied voltages from +0.3 volt to +300 volts. For values less than 0.3 volt, the response is no longer logarithmic. To avoid the negative-signal difficulty, the system shown in the block diagram of Figure 4 was developed. The signs of all input signals are converted to a positive sense and in this form are sent through the LTE and the remainder of the computer. At the output of the computer, the all-positive signals and the all-negative signals which are obtained at the output of a negative gain amplifier are sent into the output polarity inverter. A polarity senser is used to measure the sign of the input and to switch electronically the positive or negative signal to the output, depending on the input polarity. The appropriate sign of the resulting output has thus been restored.

The input inverter unit operates much the same as a full-wave rectifier. For varying input voltages in the range -150 to +150 volts, the output voltage is positive, ranging from 0 to +105 volts. The gain is approximately 0.7, with a gain stability $\Delta A \leq 1/2$ percent. The drift voltage of the output is less than 0.3 volt.

Polarity Inverting Problem: Output

The output polarity inverter, because of its logical system, is more complicated than the input inverter. The heart of the inverter is a pair of amplifiers; one inverts the input signal, and the other does not. The sensing part of the inverter allows only one amplifier to operate at a time, thus controlling the polarity of the output. Input signals applied to the sensing input terminals control the sensing circuit in such a manner that the correct algebraic sign is restored to the output. Consider, for example, the multiplication of two voltages. If both input voltages have the same polarity (i.e., both negative or both positive), then the output voltage should be positive. If, however, the two input signals have opposite signs, then the output voltage should be negative. The sensing input terminals of the inverter are connected at points in the circuit where the signals to be multiplied have proper signs (i.e., before the input polarity inverter), and the correct signs of the signals passing through the output inverter are again restored.

Two switches, labeled input bias, are mounted on the front and permit the use of the inverter with only one applied signal. When only one voltage is to be inverted, a positive or negative constant voltage is applied to the other sensing channel with the input bias switch.

Arbitrary Function of an Independent Variable

Although the computer finds its primary use as an arbitrary function generator of a dependent variable, the multiplier also can act as an arbitrary function generator of an independent variable. In this latter application, the computer competes both in accuracy and in versatility with the existing arbitrary function generators. To demonstrate a few of the driving functions obtainable with the AFINV, the system shown in the block diagram of Figure 5 was set up. With this arrangement the output of three log-taking elements are summed and fed to the LTE. A linear sweep added to a constant voltage E and E drives two LTE's yielding functions of the form

$$y_1 = A(t + a) \text{ and } y_2 = B(t + b) \quad (11)$$

The third LTE is driven with an audio oscillator which provides a function

$$y = c \sin kt \quad (12)$$

To prevent the LTE signal from becoming negative, the input polarity inverters are appropriately inserted. Only two inverters are necessary

since one signal is always positive. An output polarity inverter is used to restore the correct sign to the output signal which is displayed on an oscilloscope.

As connected, the nonlinear computer provides multipilcations of the form

$$y = A(t + a)^{\alpha}(t + b)^{\beta}(\sin kt)^{\gamma} \qquad (13)$$

If other functions g(t), h(t), and f(t), are supplied to the LTE units, the more general function

$$y = A\left[g(t)\right]^{\alpha}\left[h(t)\right]^{\beta}\left[f(t)\right]^{\gamma} \qquad (14)$$

is possible. Various functions of the form of Equation (13) are demonstrated in the oscillograms of Figures 6 through 10, with the explanation included on the figures.

Duffing's Equation

In this section the differential equation of the form

$$\ddot{x} + c\dot{x} + (\alpha x + \beta x^3) = F\cos\omega t \qquad (15)$$

is studied. This equation occurs in several different types of physical problems, for example, the pendulum with an external periodic force applied. The problem of a mass subjected to a spring restoring force leads in general to an expression of the form of equation (15). Saturation effects in iron-core inductances and in rotating machinery are other examples of physical problems which lead to this same expression. Equation (15) is often called Duffing's equation since it was Duffing who first made significant contributions to the harmonic solutions of this equation.

Explicit solutions of an elementary character are not known for the Duffing equation. In fact, this simple-looking equation has a great variety of periodic solutions alone for which the mathematical theory has been investigated only slightly. Almost nothing is known about the nonperiodic solutions to this equation.

The computer solution of Duffing's equation is demonstrated in Figure 11, where the loop analysis yields the analogous electric equation

$$L\ddot{q} + R\dot{q} + \frac{1}{C}q + kq^n = E\cos\omega t \qquad (16)$$

Appropriate variation of the exponent adjustment permits the choice of any desirable n. The classical equation dictates an n of 3, but any $n > 1$ demonstrates similar phenomena.

Oscillograms of Duffing's equation are demonstrated on Figures 12 and 13.

Van der Pol's Equation

Consider as the next example an equation which arises in numerous oscillator and multivibrator applications, the equation due to Van der Pol. When normalized, this equation has the form

$$\ddot{x} - \mu(1 - x^2)\dot{x} + x = 0 \qquad (17)$$

For comparison purposes, this expression is solved by both topological and computer methods.

In order to have a direct compaison with computer results, the phase trajectories are constructed by the method of isoclines. By taking $\dot{x} = y$ and substituting in the differential equation, one obtains

$$\dot{y} = \mu(1 - x^2)\, y - x \qquad (18)$$

The isoclines, found by setting $\lambda = dy/dx = $ constant, are given by the equation

$$y = \frac{x}{\mu(1 - x^2) - \lambda} \qquad (19)$$

If is taken as unity, equation (19) simplifies to

$$y = \frac{x}{(1 - \lambda) - x^2} \qquad (20)$$

The equation of the family of isoclines (equation 20) is plotted for various values of λ on Figure 14, where also is shown the phase trajectories. As one should expect from this equation, there exists a limit cycle (Cf. Figure 14). This cycle is due physically to the fact that the sign of the damping force changes as x is greater or less than 1. Hence for x 1 the system builds up, whereas for x 1 the system damps down, culminating in a stable-limit cycle or oscillation.

The solution of this problem on the computer is greatly simplified if one multiplies equation (17) by dt and integrates from 0 to t:

$$\int_0^t \frac{d}{dt}\left(\frac{dx}{dt}\right) dt - \mu\int_0^t (1 - x^2)\frac{dx}{dt}\, dt + \int_0^t x\, dt = C$$

$$\frac{dx}{dt} - \mu\left(x - \frac{x^3}{3}\right) + \int_0^t x\, dt = C \qquad (21)$$

The computer analog of equation (21) is shown in the block diagram of Figure 15, where the loop equation yields

$$\frac{di}{dt} - \mu\left(i - \frac{i^3}{3}\right) + \int_0^t i\,dt = 0 \qquad (22)$$

As in the case of Duffing's equation, the computer is able to establish any exponent in the nonlinear term, but for the sake of comparison with the classical expression, the cubic exponent was used. The similarity of the calculated phase trajectory of Figure 14 and the computer trajectory of Figure 16 demonstrates the good comparison between topological and computer solutions.

References

1. J. J. Stoker, "Nonlinear Vibrations in Mechanical and Electrical Systems" (1950) Interscience Publishers.

2. N. Minorsky, "Introduction to Nonlinear Mechanics" (1947) J. W. Edwards.

3. C. J. Savant, R. C. Howard, and R. S. Neiswander, "A Linear-to-Logarithmic Converter" Electronic, July 1953, Vol. 26 No. 7 pp. 156.

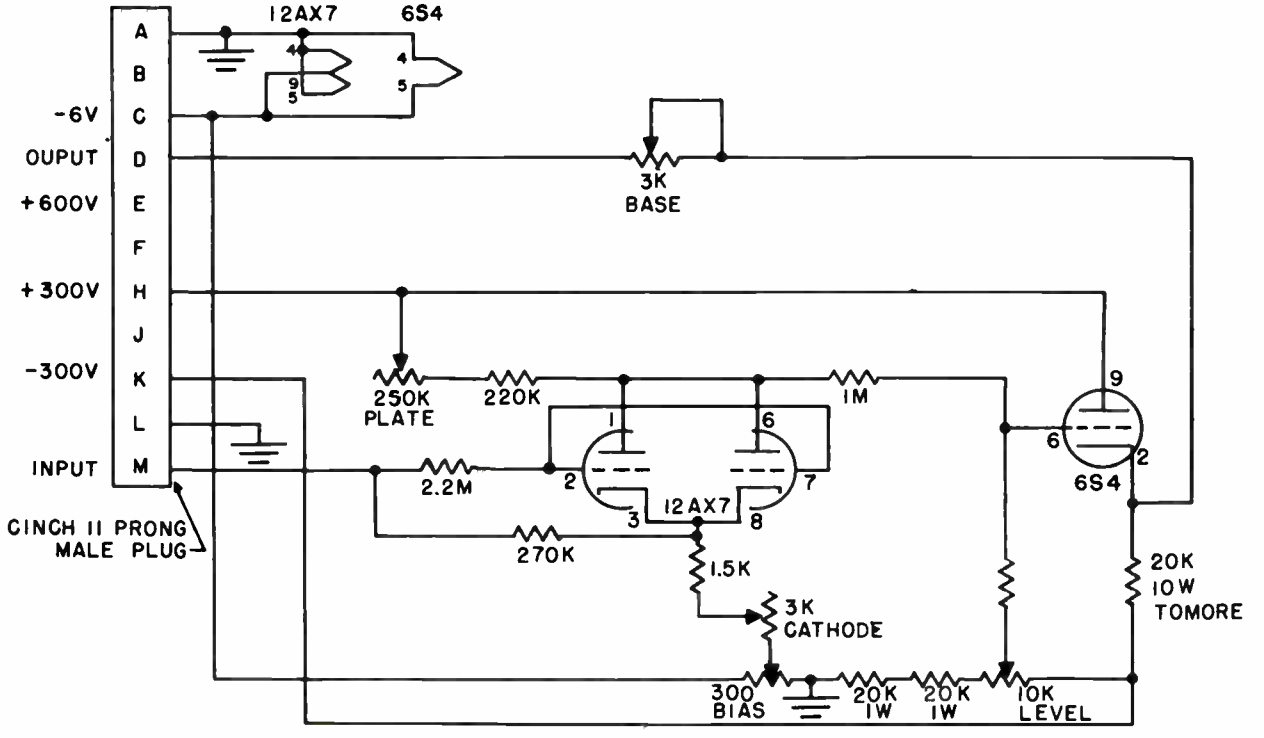


FIG. 1 - LTE CIRCUIT DIAGRAM

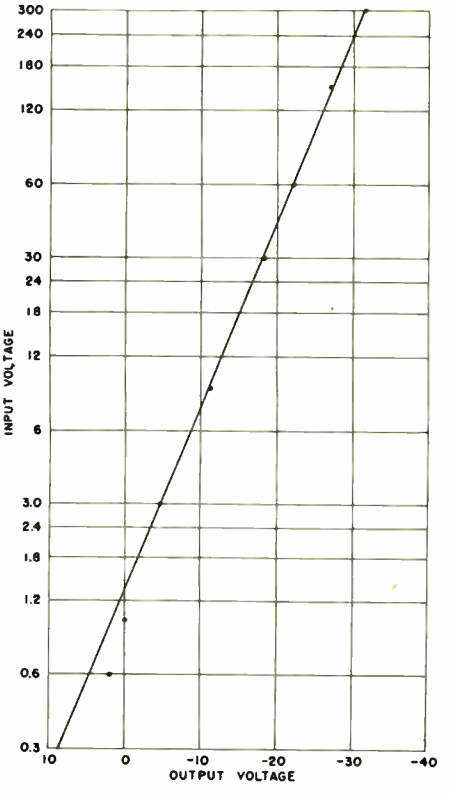


FIG. 2 - LTE RESPONSE CURVE

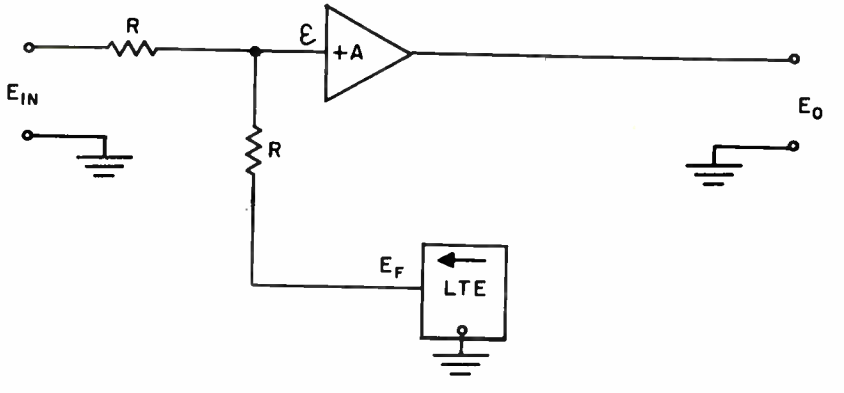


FIG. 3 - BLOCK DIAGRAM OF ILTE

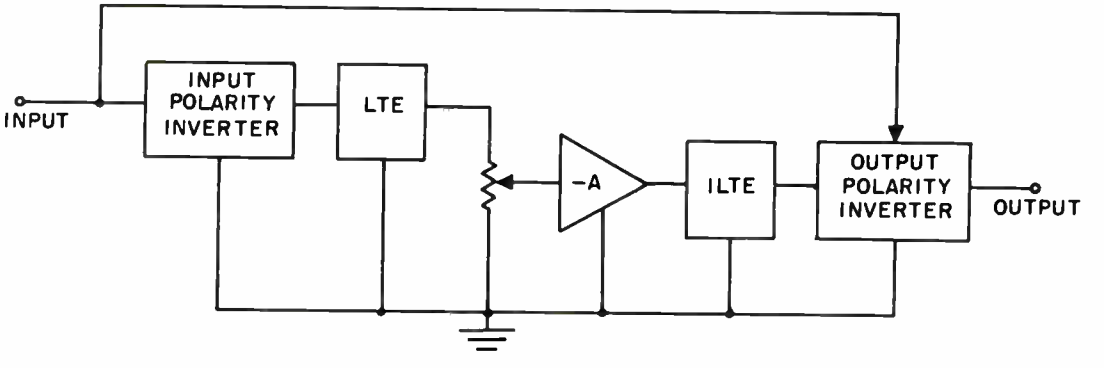


FIG. 4 - BLOCK DIAGRAM OF COMPLETE SYSTEM

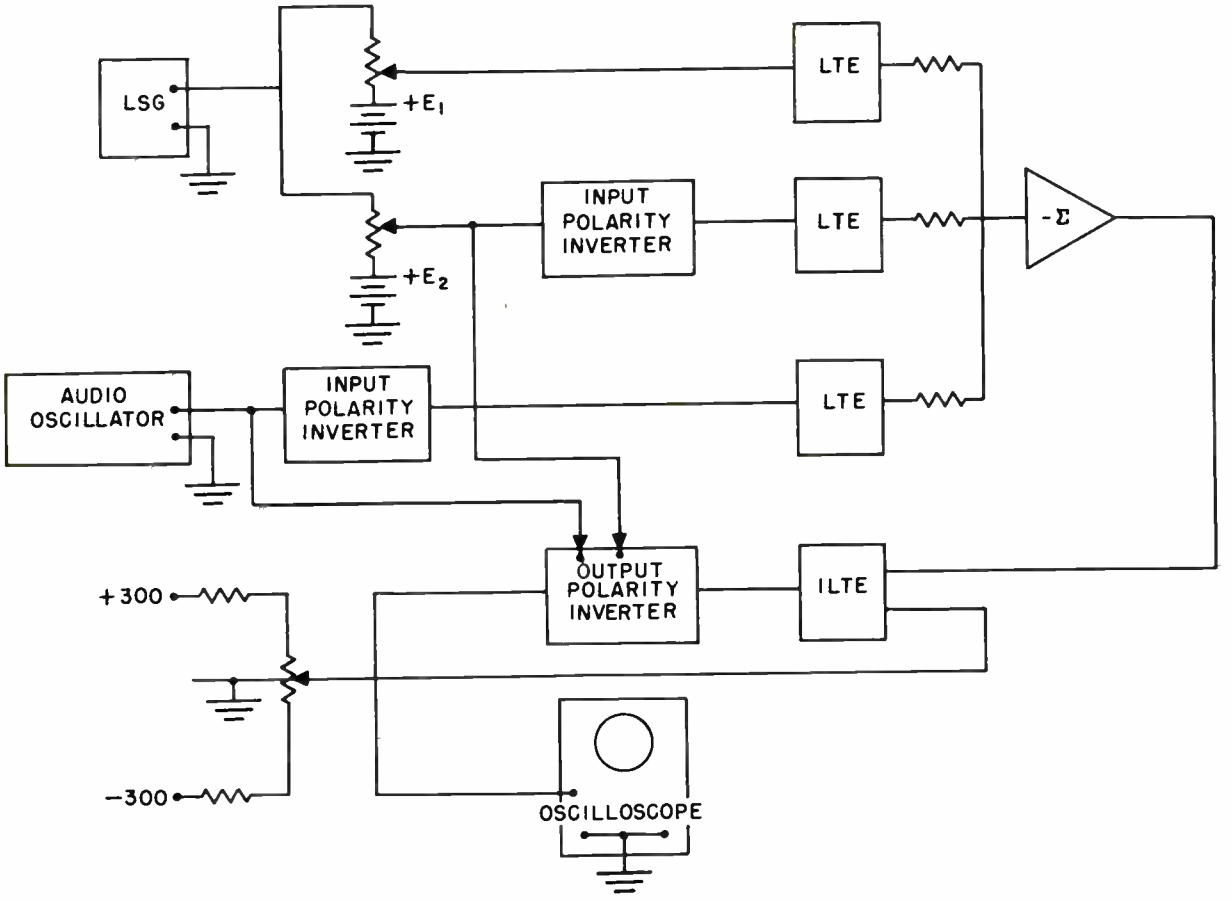


FIG. 5-USE OF COMPUTER AS ARBITRARY FUNCTION GENERATOR

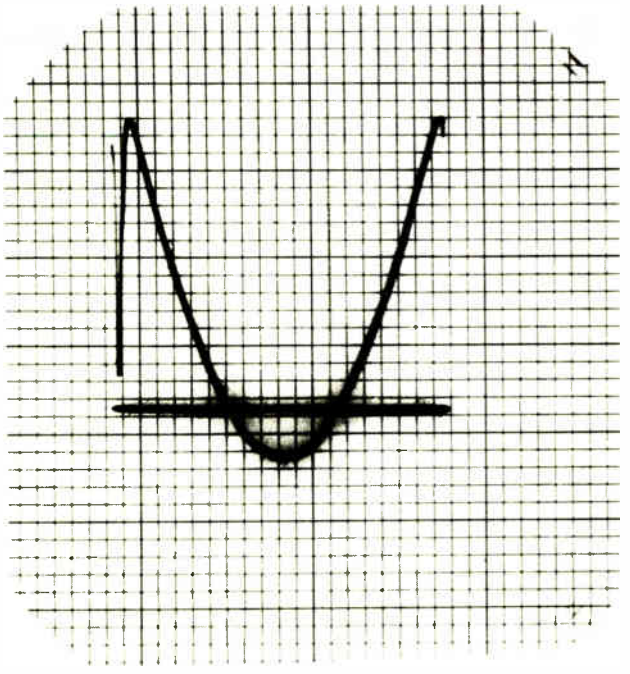


FIG. 6-OSCILLOGRAM OF $A(t+a)(t+b)$

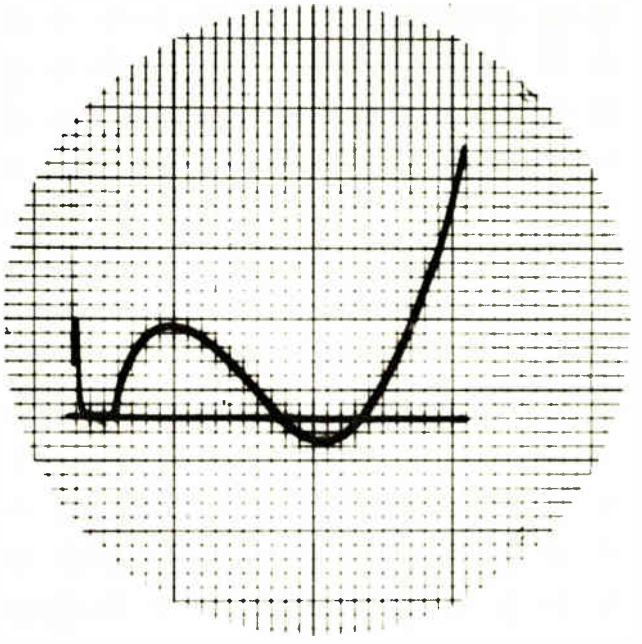


FIG. 7-OSCILLOGRAM OF $A(t+a)(t+b)t$

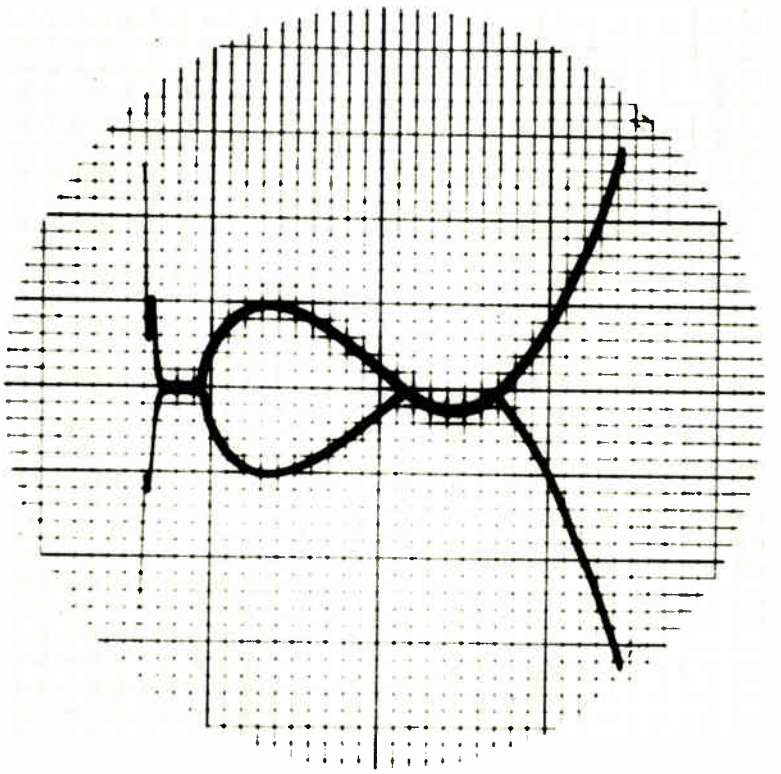


FIG. 8 - OSCILLOGRAM OF $A(t+a)(t+b)t$ BUT WITH OUTPUT POLARITY INVERTER INOPERATIVE

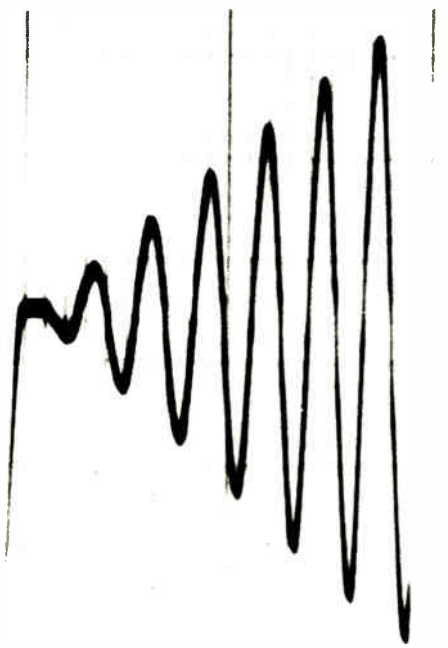


FIG. 9 - OSCILLOGRAM OF $At\sin\omega t$

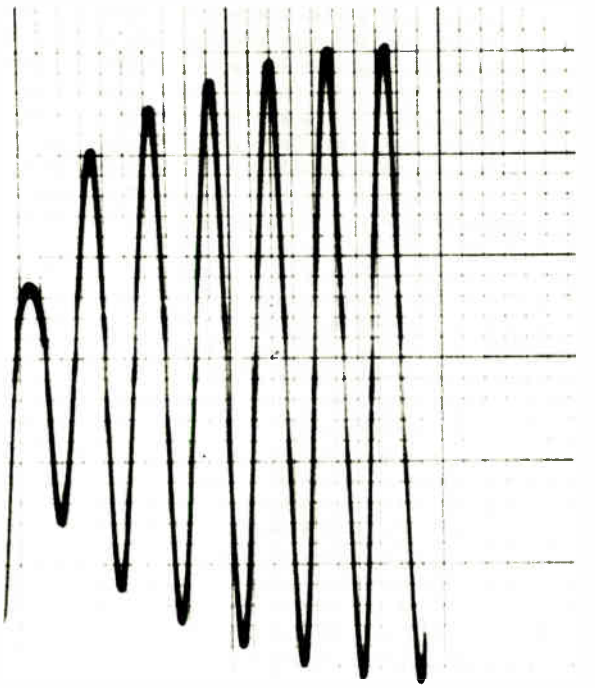


FIG. 10 - OSCILLOGRAM OF $At^{w}\sin\omega t$, $n<1$

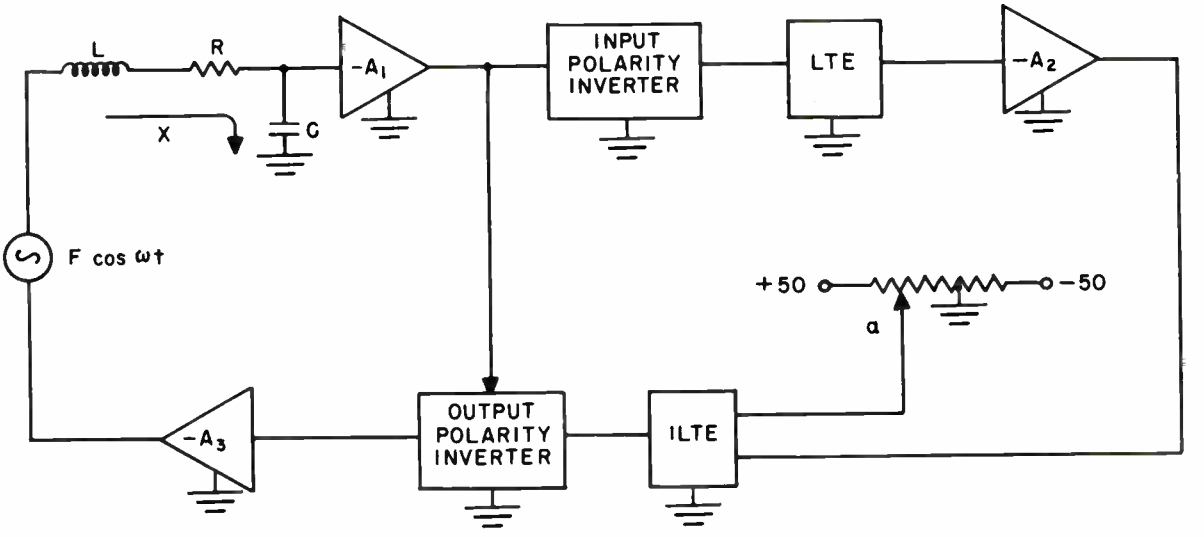


FIG. 11 – COMPUTER SOLUTION OF DUFFING'S EQUATION

$\ddot{x} + c\dot{x} + (\alpha x + \beta x^3) = F \cos \omega t$

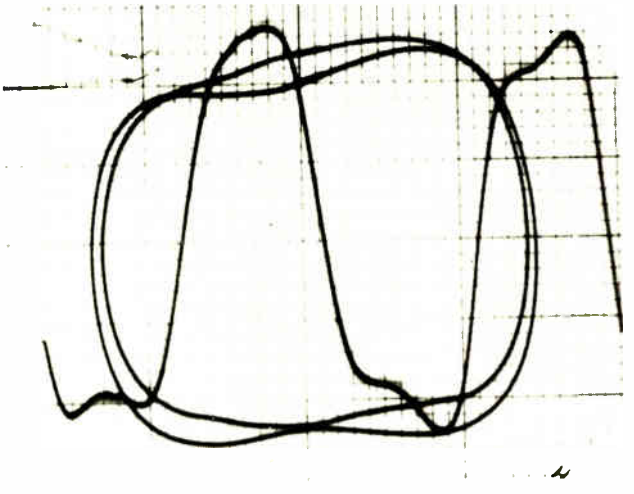


FIG. 12 – PHASE TRAJECTORY OF DUFFING'S EQUATION, f = 24 CPS

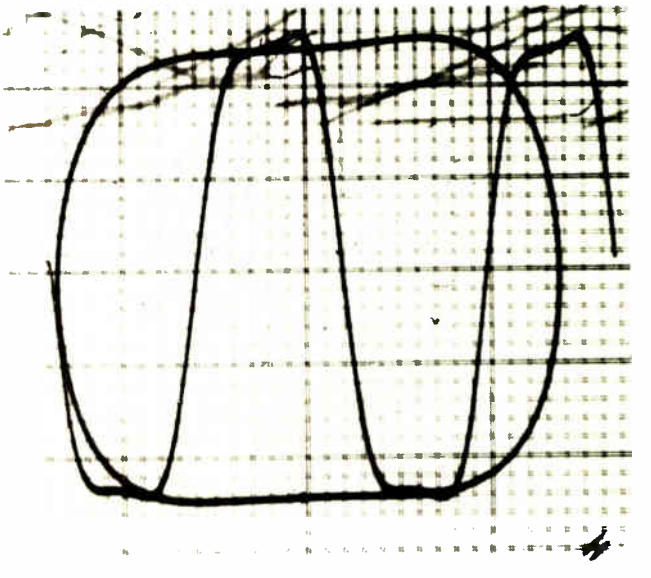


FIG. 13 – PHASE TRAJECORY OF DUFFING'S EQUATION, f = 34 CPS

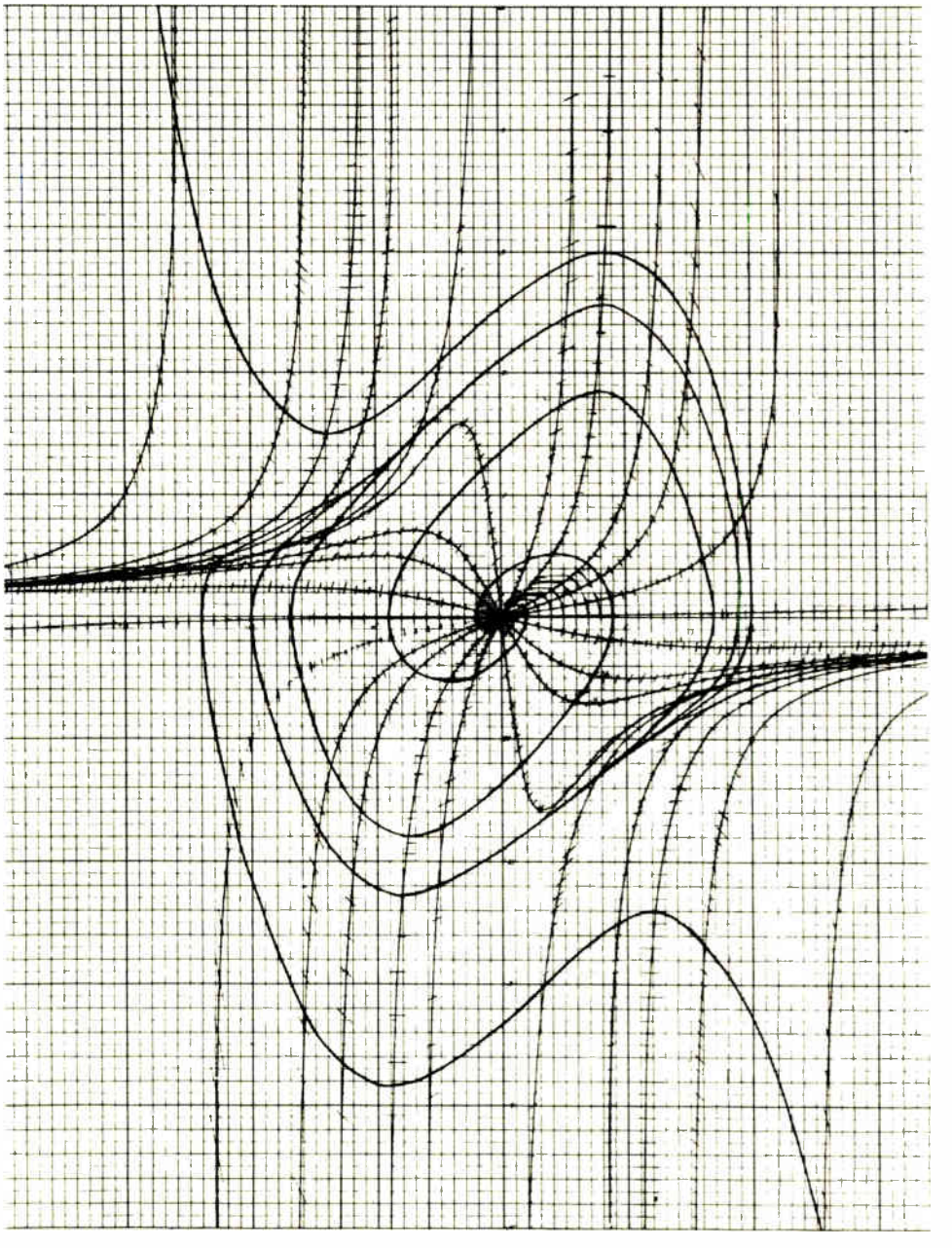


FIG. 14-ANALYTIC SOLUTION OF VAN DER POL'S EQUATION

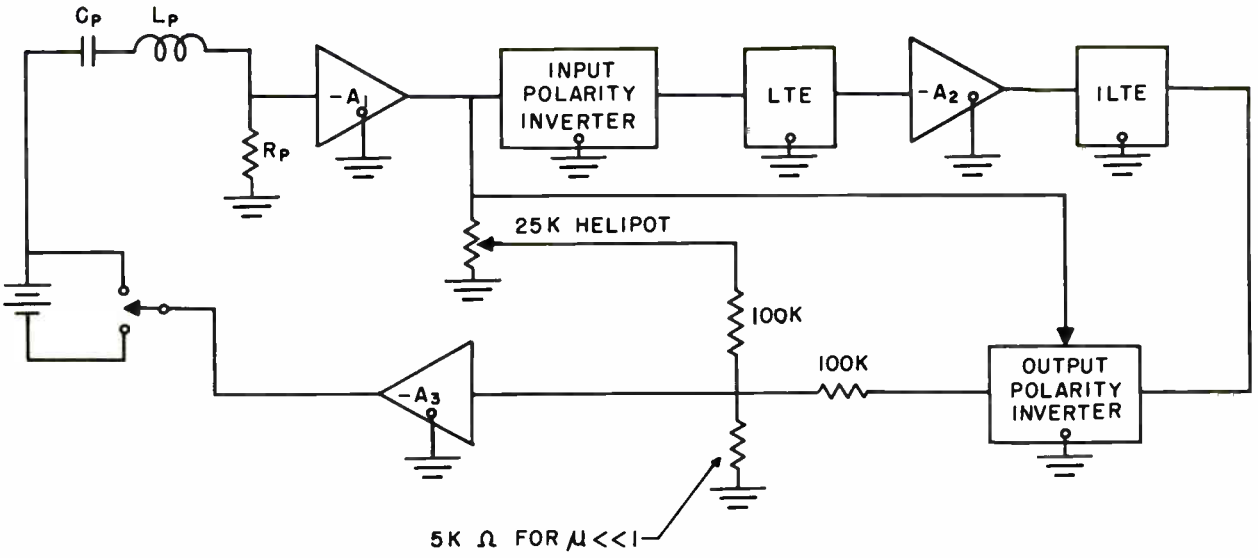


FIG. 15-COMPUTER SOLUTION OF VAN DER POL'S EQUATION

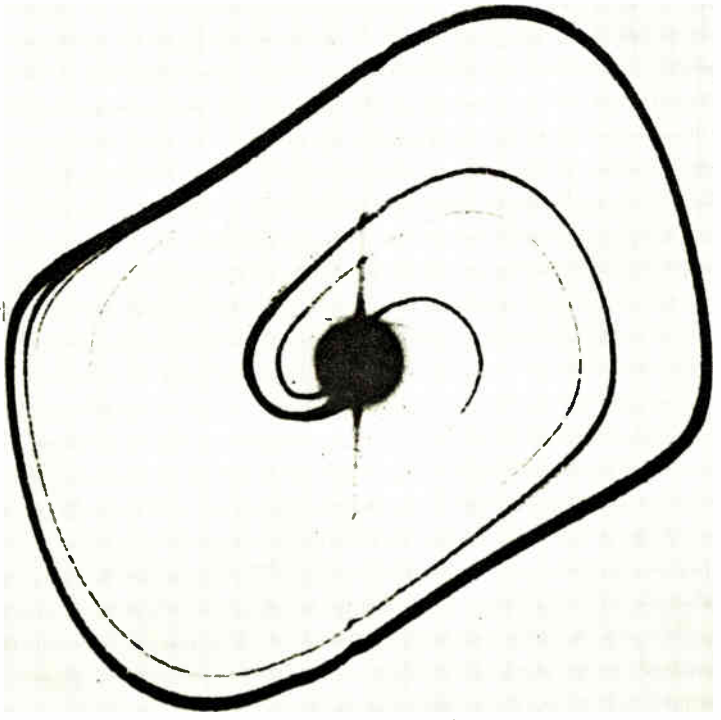


FIG. 16-COMPUTER SOLUTION OF VAN DER POL'S EQUATION

AUTOMATIC ITERATION ON AN ELECTRONIC ANALOG COMPUTER

Louis B. Wadel
Chance Vought Aircraft, Incorporated
Dallas, Texas

Abstract

An electronic analog computer is employed for automatic solution of ordinary differential equations whose computer solution depends upon the application of an iterative process. Three types of equations falling into this category are noted, and a simple example of each is given. A computer solution procedure applicable to each example is outlined, with some circuit diagrams included. Also described is the use of a multi-pole stepping-relay to effect the iteration procedures required. Illustrative results are presented.

Introduction

Definition

Automatic iteration is defined as the repeated solution of a basic differential equation, a procedure in making variations in parameters or initial conditions being followed automatically by the computer such that these settings depend upon the results of the previous solution(s), and such that a pre-specified result is obtained as the limit solution.

Examples

Noted below are three cases, together with an example of each, which require iterative solution when an electronic analog computer is employed. The examples have been chosen simple enough to permit straightforward manual solution for checking purposes. Also, they demonstrate the automatic handling of a search for an initial condition, for an additive constant, and for a multiplicative constant.

(A) A split boundary condition problem:

$$\ddot{x} + 0.2\,\dot{x} + 0.01\,x = 0 \qquad (1)$$

Find $\dot{x}(0)$ and $x(t)$, given $x(0) = 50$ and $x(10) = 0$.

(B) An implicit problem:

$$\ddot{x} + x = 12.5 + 0.104\int_0^{\infty} x(t)\exp(-0.2\,t)\,dt \qquad (2)$$

Find $x(t)$, given $x(0) = \dot{x}(0) = 0$.

(C) A minimization problem:

$$\ddot{x} + 2k\,\dot{x} + x = 0 \qquad (3)$$

Find k such that $J = \int_0^{\infty} x^2\,dt$ is minimized, given $x(0) = 40$ and $\dot{x}(0) = 0$.

Find also the corresponding J and $x(t)$.

Philosophy

The iteration process is as follows: (1) Assume and set into the computer an arbitrary "starting value" for the unknown parameter or initial condition; (2) solve the resulting differential equation; (3) observe the "error" --- i.e., the difference between the desired result and the actual result; (4) based on this error, obtain a "corrected" value for the unknown parameter or initial condition; (5) solve the modified differential equation; (6) observe the new error ... Continue the sequence of operations until the corrections become negligible.

Depending upon the particular problem, the starting value for the unknown parameter or initial condition, and the relation set up between the observed error and the correction made, the required solution may be approached as a limit or the computer solutions may diverge from the true solution. Thus, while it is desired that the computer automatically carry out all the steps of the iteration process, a judicious choice of starting value and of correction procedure may at times be essential and will in all cases result in more efficient problem solution.

Computer Controls

The three basic states of an electronic analog computer are (1) RESET, (2) OPERATE, and (3) HOLD. In RESET, variables and their derivatives are fixed at their "initial conditions". When OPERATE is executed, the problem solution begins. If HOLD is executed, the solution is frozen at whatever conditions exist at the moment of execution. A return to OPERATE from HOLD causes the solution to proceed again from the stopping point. The computer may be RESET at any time. Change from one basic state to another is effected by relays which control internal connections of the integrating units.[1] In conventional problems, all computer units are in the same basic state at the same time. To solve differential equations by iteration, however, it is necessary to provide for the separate control of certain units.

Split Boundary Conditions

Circuit Operation

The basic computer circuit for the solution of equation (1) is shown inside the dashed boundary of Figure 1, and will be referred to as "Unit M". The other elements of Figure 1 constitute the iteration control elements, and consist of an

Integrator G and a convergence control Potentiometer P. The iteration cycle is as follows:

State	Unit M	Integrator G
1	RESET	HOLD
2	OPERATE	HOLD
3	HOLD	OPERATE
4	HOLD	HOLD

From the starting state, State 1, the system is switched to State 2, and Unit M OPERATES for ten seconds, since x(10) has been specified. The system then passes to State 3, during which the output of Integrator 2 is automatically HELD at the value x(10); this is the solution "error", since it was specified that x(10) be zero. Integrator G OPERATES for the duration of State 3 and therefore this error, multiplied by the setting of Potentiometer P, drives Integrator G during State 3. The result is that the output of Integrator G is increased by the product of the solution error and the convergence factor "m", where "m" is the negative of the product of the setting of Potentiometer P and the time duration of State 3. Integrator G is returned to HOLD for State 4, a buffer state. (A buffer state is a state included solely to ensure proper sequencing of relay contacts.) Unit M is then restored to RESET --- State 1. Integrator 1, whose output is $-\dot{x}(t)$, now has a corrected initial condition as supplied by Integrator G, and the program is repeated.

In the foregoing description, it was assumed that the starting value chosen for $\dot{x}(0)$ was zero. However, any other starting value can be utilized by setting the proper initial condition on Integrator G before the system is first placed in State 1.

This method of obtaining corrected values of $\dot{x}(0)$ has the following properties:

Convergence Factor "m"	Iterative Approach to True Solution
$m > 0$	monotonic divergence
$0 > m > -0.1\ e$	monotonic convergence
$-0.1\ e > m > -0.2\ e$	oscillatory convergence
$-0.2\ e > m$	oscillatory divergence

Control Mechanization

From an equipment point of view, the mechanization of the 4-State program outlined above reduces to the problem of energizing relays according to a prescribed time pattern. In our equipment, each integrator has two relays which, in combination, control the state of that integrator:

State/Relay	X	Y
RESET	Energized	Energized
OPERATE	Unenergized	Unenergized
HOLD	Unenergized	Energized

In terms of relays, then, the iteration routine may be expressed as

State	Unit M		Integrator G	
	X-Relays	Y-Relays	X-Relay	Y-Relay
1	Engzd	Engzd	Unengzd	Engzd
2	Unengzd	Unengzd	Unengzd	Engzd
3	Unengzd	Engzd	Unengzd	Unengzd
4	Unengzd	Engzd	Unengzd	Engzd

Note that the X-Relay of Integrator G is always unenergized in the above program; therefore only three independent controls are required.

The relay control system employs a synchronous motor and cam arrangement, which causes an electric pulse to be generated once per second (by other gearing, or by the use of multiple cams, other intervals can be obtained). These pulses step a 6-pole 26-throw stepping-relay. Thus, up to six quantities can be controlled independently over an iteration cycle of 26 intervals (26 seconds if one-second pulses are used to drive the stepping-relay). A state will consist of one or more intervals. In the present problem the duration of only State 2 must be adjusted accurately. The duration of the other states can be set arbitrarily at an integral number of seconds, and hence integral stepping-relay intervals. The duration of State 2 happens to be integral number of seconds (ten), so that exactly ten intervals of the stepping-relay are covered. If a non-integral duration were required, the problem time-scale could be altered slightly to result in an integer for machine duration of State 2, or else external timing devices might be employed. (Somewhat different control schemes have been discussed elsewhere.[2,3])

All contact points are brought out to the front panel of the programming unit, so that any sequencing pattern can be established by connecting the proper terminals together and patching voltage to points as required. Provision for external stepping signals has also been made, as it may be desirable in some problems to have the stepping done by non-time-based signals. The connections made for the problem under discussion are indicated in Figure 2.

Results

A plotting-board is convenient to use for plotting automatically the successive results of an iterative process, because a superimposed presentation of the individual solutions can be obtained. It was advantageous to use a fourth pole of the stepping-relay to control the pen-lift relay so that the pen was lifted from the plotting surface while the pen slewed between States 4 and 1.

Figure 3 depicts the results of solving equation (1) according to the procedure outlined, with the convergence factor "m" set at various values. Figure 3a demonstrates monotonic divergence; 3b, monotonic convergence; 3c, oscillatory convergence;

and 3d, oscillatory divergence. The correct solution is shown as a dashed curve.

Implicit Term

The computer diagram for equation (2) is shown in Figure 4. The elements necessary to solve the basic equation are included within the dashed boundary and are collectively denoted "Unit M". The only element required for iteration control is Integrator G, shown outside the dashed boundary. The iteration sequence is identical with that of the previous problem, although the durations of the individual states are not the same as before.

The desired starting value F_o for the definite integral is set into Integrator G as its initial condition before the system is first placed in State 1. When State 2 is begun, Unit M solves equation (2) for the first time, yielding $x_o(t)$. Simultaneously, calculation of the definite integral, "F", is performed by Integrator 4 of Unit M. (Since the upper limit of integration is infinity, the integration is in actual practice carried out over an interval large compared with the five-second time constant of the exponential term.) During State 3, the output of Integrator 4 of Unit M, now on HOLD, is proportional to the corrected value F_1 of F. In this problem a correction or "error" voltage does not explicitly exist in the circuit, it being more convenient to compute the corrected value itself rather than an increment to be added to the previous value of F. Integrator G is on OPERATE for State 3; its output therefore assumes the value $0.10^4 F_1$, the negative of the output of Integrator 4. Both Unit M and Integrator G HOLD for State 4, a buffer state. The system is next returned to State 1 for another iteration cycle; this time, $x_1(t)$ and F_2 are computed. The process will converge.

None of the states is of critical time duration, and thus an integral number of stepping-relay intervals is satisfactory for each state. A period of twenty-two seconds was used for State 2, which theoretically requires infinite time. Figure 5 shows the first few solutions x(t) as obtained from the computer.

Minimization Problem

The computer procedure used for solving equation (3) is rather crude in concept. A starting value k_o for k is chosen, the equation is solved using this value for k, and the corresponding value J_o of J is computed. Equation (3) is next solved again, using now for k the corrected value $k_1 = k_o + h$, where h is a preset constant, and J_1 is computed. J_1 is compared with J_o; if $J_1 < J_o$, it is assumed that the minimum value of J will be approached if corrections of the same sign continue to be made to k. Equation (3) is therefore re-solved, using for k the value $k_2 = k_1 + h$, and simultaneously J_2 is computed. The process is repeated so long as $J_n < J_{n-1}$. Finally a $J_n > J_{n-1}$ will be obtained, indicating that k_n has overshot the value of k which will yield the minimum value of J. Thereupon, a correction is made to k of amount -h/2, rather than the +h which was used before. These -h/2 corrections are used in each iteration cycle until again an overshooting of the desired value of k is indicated; again the sign of the corrections is reversed and the magnitude halved. This general scheme is carried out so long as it continues to be profitable. A five-state program is required for each iteration cycle.

Figure 6 shows a plot of successive J and k values computed. The discrete points were obtained on the plotting-board by automatically lowering the pen to the plotting surface during only one state of each iteration cycle.

Conclusion

An electronic analog computer can be profitably employed to solve automatically an ordinary differential equation whose computer solution depends upon the application of an iterative process. However, care must be taken to choose a valid and efficient iteration routine for each problem type. The methods of iteration mechanization discussed in this paper are intended to be merely suggestive in nature, and it is to be expected that a variety of additional techniques will be developed in the future.

Acknowledgment

It is a pleasure to acknowledge the general assistance of Messrs. J. D. Stenquist and O. J. Sullivan, as well as the assistance of Mr. Billy Cox as technician, Mmes. Martha Cohen and Eartha Vaughan in typing the manuscript, and Mmes. Geraldine Barnes and Betty Scarborough in executing the figures.

References

1. Electronic Analog Computers by Granino A. Korn and Theresa M. Korn, McGraw-Hill Book Company, Inc., 1952.

2. "Application of REAC Equipment to the Solution of Problems Involving Integral Operators, I" by P. Brock and S. Sherman, Project Cyclone Symposium I, 15-16 March 1951.

3. "The Time-Sequence Controller for Automatic Operation of the Electronic Differential Analyzer" by George R. Hansen, Jr., Memorandum No. 20-81, Jet Propulsion Laboratory, California Institute of Technology, 2 March 1953.

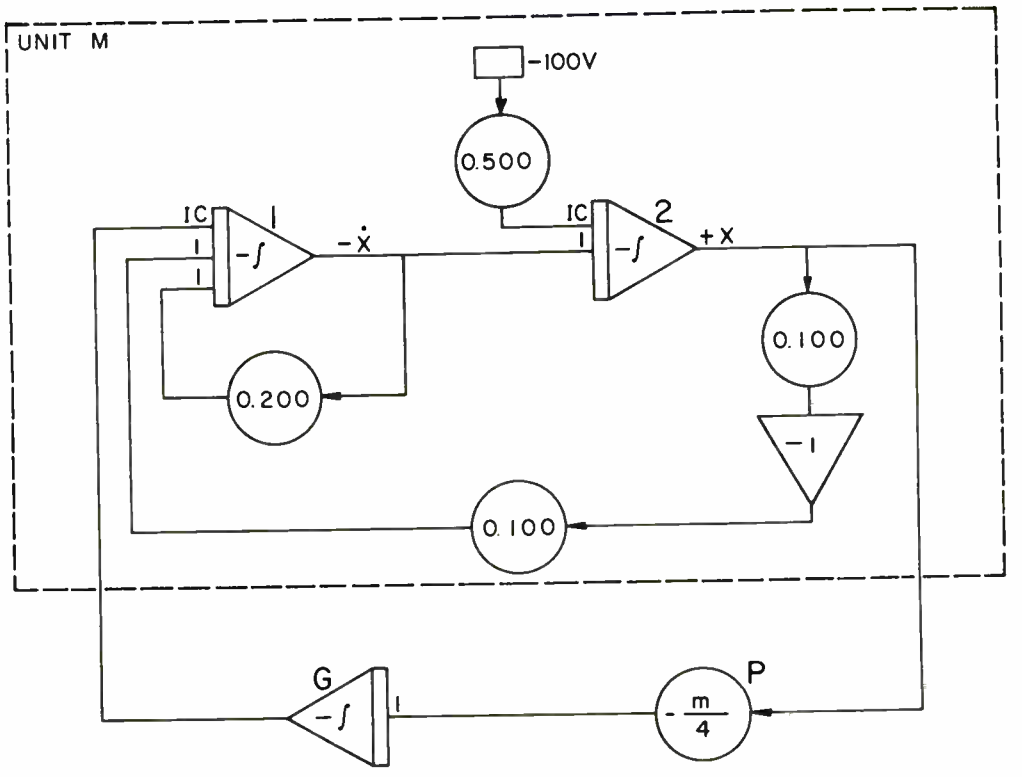
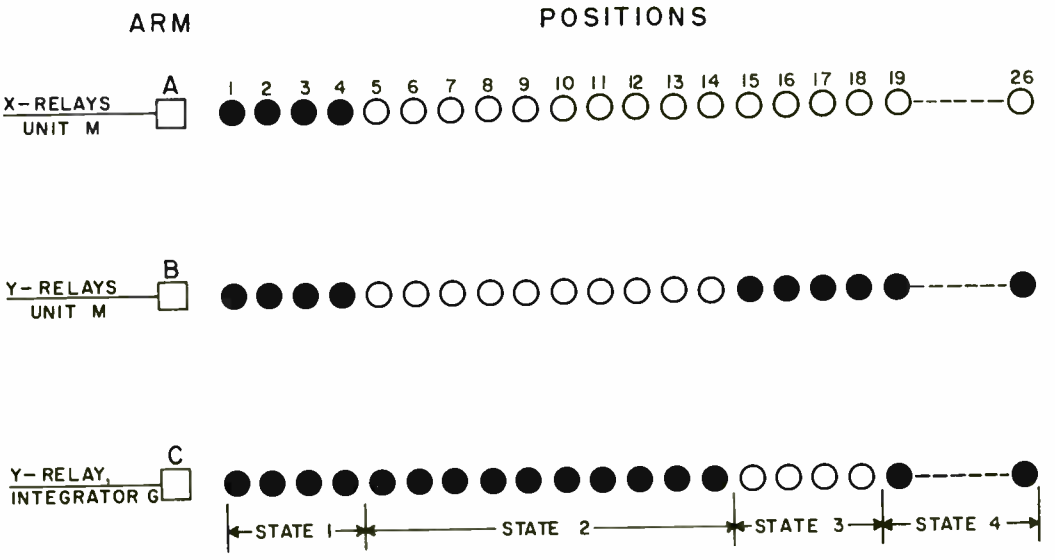


Fig. 1 - Split boundary conditions circuit.



KEY :

○ OPEN CONNECTION

● + 26 VOLTS CONNECTED HERE

Fig. 2 - Stepping-relay connections.

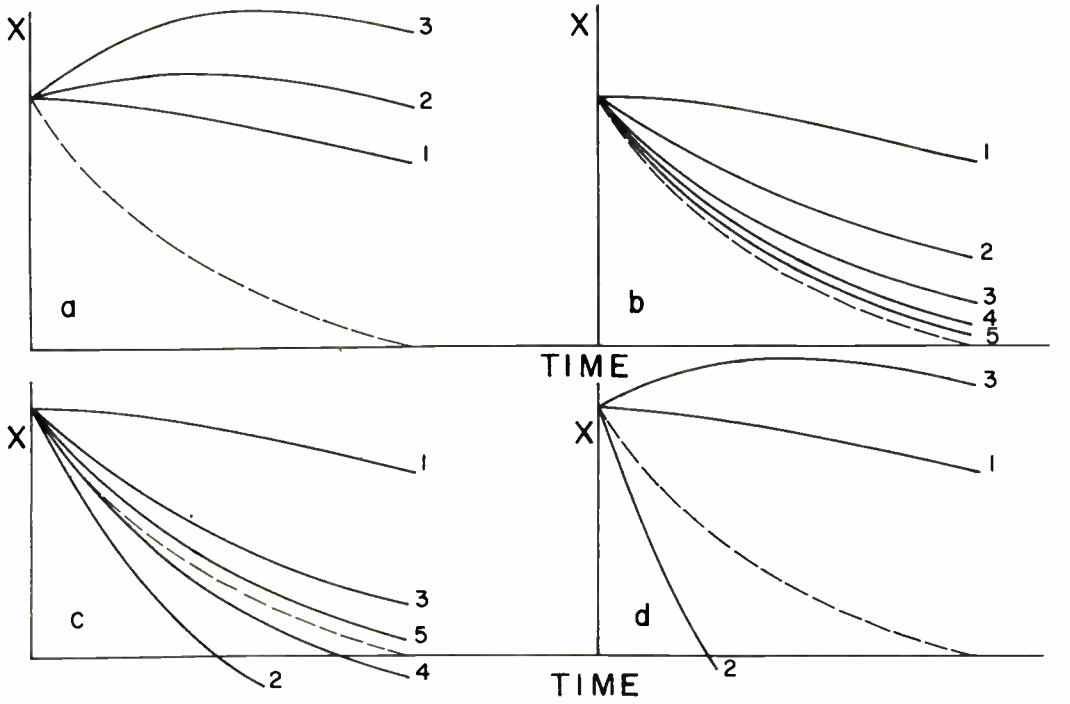


Fig. 3 - Split boundary conditions results.

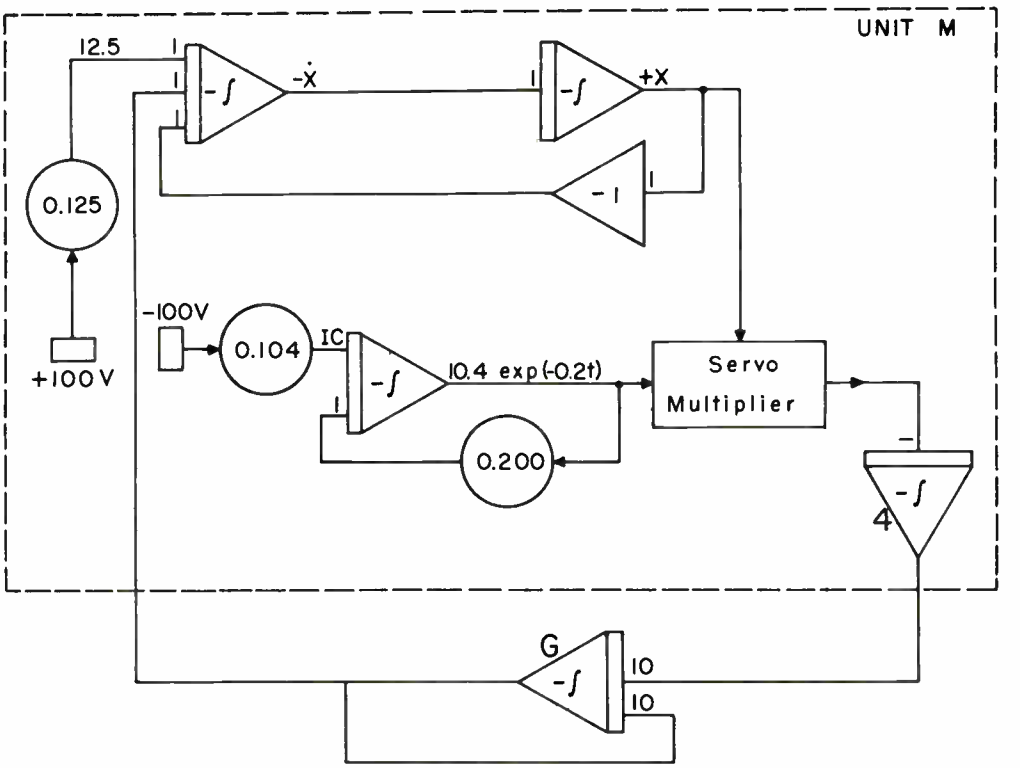


Fig. 4 - Implicit equation circuit.

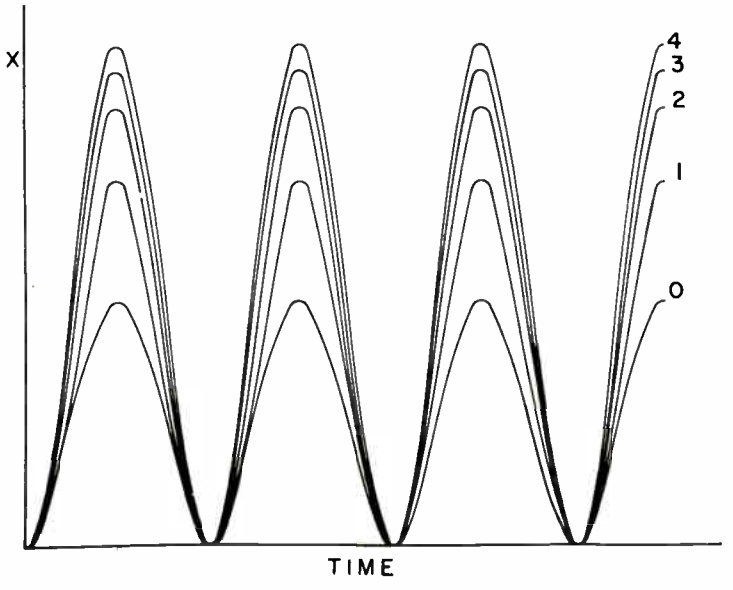


Fig. 5 - Successive computer solutions.

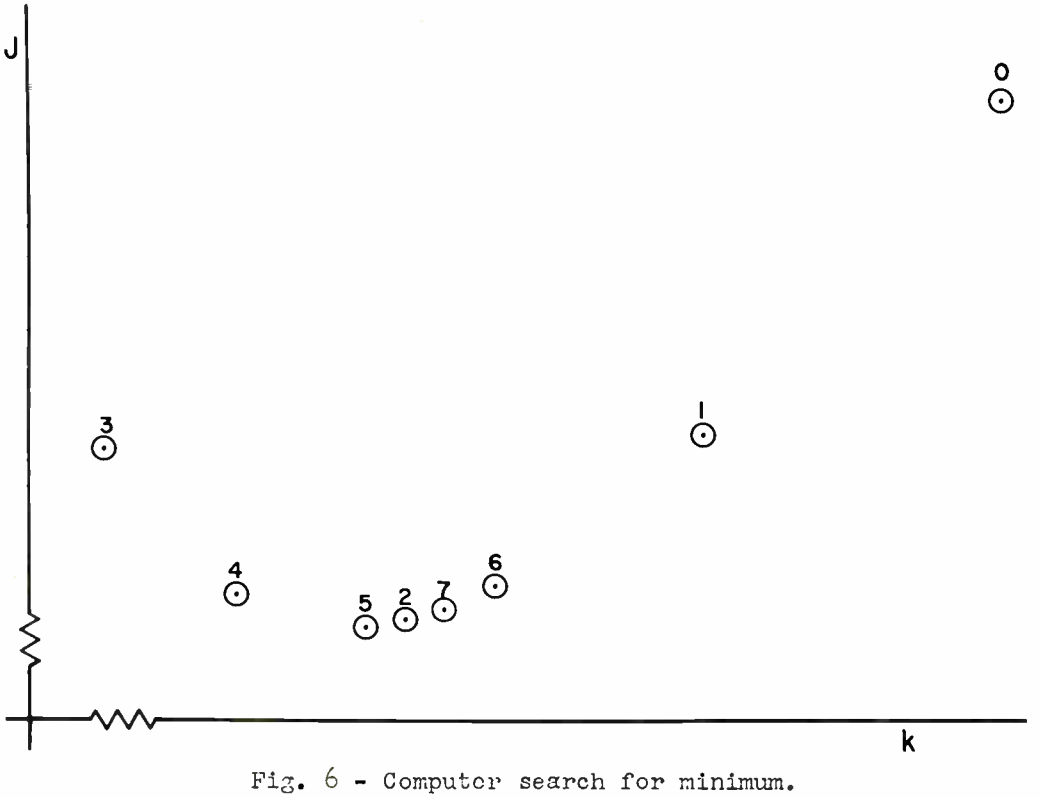


Fig. 6 - Computer search for minimum.

A LOGARITHMIC VOLTAGE QUANTIZER

E. M. Glaser and H. Blasbalg
Radiation Laboratory, The Johns Hopkins University
Baltimore, Maryland

INTRODUCTION

This paper describes an analog to digital converter which converts voltage into a number which is proportional to the logarithm of the voltage. The device is completely automatic. It can handle input data at the rate of 10,000 voltage samples per second. The accuracy of conversion or quantization is adjustable to either 5% or 10%. Samples of length greater than .5 microsecond can be quantized.

GENERAL

The quantizer accepts a voltage sample and converts it to an equivalent pulse whose duration is proportional to the logarithm of the voltage of the sample. The pulse duration is quantized linearly by counting the number of pulses produced by a fixed frequency pulse generator during the interval. This number is then proportional to the logarithm of the input sample.

The conversion from voltage to time is performed in a simple RC circuit. The mathematical analysis of the conversion and quantization is given below. From the analysis useful design equations are obtained.

ANALYSIS

An RC network shown in Fig. 1 is charged to voltage E by closing of switch S. After the switch is opened at t = 0, the voltage e(t) decays exponentially:

$$e(t) = E\,\varepsilon^{-t/RC} \tag{1}$$

Let T = time for e(t) to decay to a fixed voltage, E_T.
Then,

$$E_T = E\,\varepsilon^{-T/RC} \tag{2}$$

or

$$E = E_T\,\varepsilon^{T/RC} \tag{3}$$

and

$$\log E = \log E_T + \frac{T}{RC}. \tag{4}$$

T is now subdivided into equal increments ΔT and the number of complete increments required for E to decay to E_T is counted.

Let E_n = value of E which decays to E_T in exactly $n\Delta T$ seconds and E_{n+1} = value of E which decays to E_T in exactly $(n+1)\,\Delta T$ seconds;
then, $E_o = E_T$.

From Eq. (4),

$$\log E_n = \log E_T + \frac{n\Delta T}{RC} \tag{5}$$

and

$$\log E_{n+1} = \log E_T + \frac{(n+1)\,\Delta T}{RC}. \tag{6}$$

Subtracting Eq. (5) from Eq. (6),

$$\log E_{n+1} - \log E_n = \frac{\Delta T}{RC} = \frac{\Delta T}{\tau} \tag{7}$$

where $\tau = RC$.

Let $\bar{E}_n = \frac{1}{2}(E_{n+1} + E_n)$

and $\Delta E_n = E_{n+1} - E_n$,

then,

$$\frac{\Delta E_n}{\bar{E}_n} = 2\left(\frac{E_{n+1} - E_n}{E_{n+1} + E_n}\right). \tag{8}$$

Also, by expanding,

$$\log E_{n+1} - \log E_n = 2\left[\left(\frac{E_{n+1} - E_n}{E_{n+1} + E_n}\right) + \frac{1}{3}\left(\frac{E_{n+1} - E_n}{E_{n+1} + E_n}\right)^3 + \cdots\right] = \frac{\Delta T}{\tau} \tag{9}$$

Therefore, by neglecting all but the first term

$$\frac{\Delta T}{\tau} \approx \frac{\Delta E_n}{\bar{E}_n} \tag{10}$$

with error

$$\delta \leq \frac{2}{3}\,\frac{S^3}{\sqrt{1-S^2}}$$

where

$$S = \frac{1}{2}\,\frac{\Delta E_n}{\bar{E}_n} = \frac{1}{2}\,\frac{\Delta T}{\tau} \tag{11}$$

Equation (11) gives the order of the error in the approximation in solving Eq. (9) for E_{n+1}. Substituting Eq. (11) in Eq. (8) and solving gives

$$E_{n+1} = E_n \frac{1 + \frac{1}{2}\frac{\Delta T}{\tau}}{1 - \frac{1}{2}\frac{\Delta T}{\tau}} = r\,E_n \qquad (12)$$

where $$r = \frac{1 + \frac{1}{2}\frac{\Delta T}{\tau}}{1 - \frac{1}{2}\frac{\Delta T}{\tau}}.$$

From this

$$E_n = r^n E_o. \qquad (13)$$

The voltage levels E_n and $\bar{E}_n$, it should be form geometric series.

The maximum quantization error will occur when either E_n or E_{n+1} is quantized as $\bar{E}_n$. This error will be, in either case,

$$\text{max. error} = \frac{1}{2}\frac{\Delta E_n}{\bar{E}_n} \qquad (14)$$

$$\text{max. error} = S = \frac{1}{2}\frac{\Delta T}{\tau}$$

If N = maximum quantized time intervals, and E_N = maximum quantizable voltage, then the dynamic range, R, of the quantizer is

$$R = \frac{E_N}{E_T} = \frac{E_N}{E_o} = r^N \qquad (15)$$

$$\log R = N \log r = N \log \left(\frac{1+s}{1-s}\right)$$

$$= 2N\left(s + \frac{1}{3}s^3 + \frac{1}{5}s^5 + \ldots.\right) \qquad (16)$$

and again, by neglecting all but the first term,

$$\log R \approx 2NS \qquad (17)$$

with error

$$\delta \leq \frac{2}{3}\frac{NS^3}{\sqrt{1-S^2}}$$

Then

$$N = \frac{1}{2s}\log R \qquad (18)$$

The rate at which the exponential e(t) decays when $e(t) = E_T$ is

$$\left.\frac{de(t)}{dt}\right|_{t=T} = \frac{-E}{RC}\varepsilon^{-T/RC}$$

and from Eq. (2)

$$\left.\frac{de(t)}{dt}\right|_{t=T} = \frac{-E_T}{RC} = \frac{-E_T}{\tau}.$$

The rate of voltage decay at the threshold is therefore independent of the initial sample voltage E. The accuracy of the threshold amplitude comparator is therefore constant throughout the quantization range.

The equations useful for quantizer design are given below.

$$\text{max. error} = s = \frac{1}{2}\frac{\Delta T}{\tau} \qquad (14)$$

The number of quantization intervals is given by,

$$N = \frac{1}{2s}\log R \qquad (18)$$

The quantizer is designed to operate over a dynamic range of 30:1 with E_T = 3.3 volts and E_N = 100 volts.

The maximum error is 5% or 10%.

$$\text{For } s = .05,\ N = \frac{1}{2 \times .05}\log 30 \qquad (19)$$

$$= 34$$

$$\text{For } s = .1,\ N = \frac{1}{2 \times .1}\log 30 \qquad (20)$$

$$= 17$$

The quantizer generates a pulse at the start of the exponential, if $E \geq E_T$. At the end of each interval, ΔT, another pulse is generated repeating the process until the exponential falls below E_T. (See Fig. 2.)

Voltage	Number of Pulses
$E < E_T$	0
$E_T \leq E \leq rE_T$	1
$rE_T \leq E \leq r^2E_T$	2
$r^2E_T \leq E \leq r^3E_T$	3
$r^{N-1}E_T \leq E \leq r^NE_T$	N
$r^NE_T \leq E$	N+1

For R = 30, s = .05 the maximum number of pulses generated is N + 1 = 18.
For R = 30, s = .1, the maximum number of pulses is N + 1 = 35.

The time increment of quantization is one microsecond. This minimizes analysis time without unduly complicating the device. The time constant is determined from Eq. (14).

For s = 0.05

$$\tau = \frac{\Delta T}{2s} = \frac{1 \times 10^{-6}}{2 \times .05}$$

$$\tau = 10 \times 10^{-6} \text{ sec.}$$

For s = 0.1

$$\tau = 5 \times 10^{-6} \text{ sec.}$$

A table relating input voltage to $\bar{E}_n$ and the quantization level (number of output pulses) is shown in Fig. 3 for s = .05 and s = 0.1.

The maximum sampling rate of a waveform by the quantizer can be obtained by means of Eq. (18). The maximum time per quantization, T_q, is

$$T_q = N\Delta T = \frac{\Delta T}{2S} \log R \qquad (21)$$

Then the maximum sampling rate, F, is

$$F = \frac{1}{T_q} = \frac{2S}{\Delta T} \frac{1}{\log R}$$

$$F = 2Sf \frac{1}{\log R} \qquad (22)$$

where f = frequency of the pulse generator.

This equation allows for no recovery time of the quantizer between samples. Allowing, conservatively, a recovery time equal to the maximum quantization time gives for the sampling rate, F',

$$F' = Sf \frac{1}{\log R}. \qquad (23)$$

For S = .05, $f = 1 \times 10^6$, R = 30

$$F' = \frac{.05 \times 10^6}{\log 30} = 14.7 \times 10^3 \text{ samples/sec.}$$

For S = .10, $f = 1 \times 10^6$, R = 30

$$F' = 29.4 \times 10^3 \text{ samples/sec.}$$

CIRCUIT DESIGN

The quantizer is designed to work with voltage samples ranging from 3.3 volts to 100 volts and a minimum duration of .5 microsecond. A block diagram is shown in Fig. 4, and the circuit schematic in Fig. 5.

Input Cathode Follower, V_1.

The cathode follower consists of both sections of a 2C51 operating in the high g_m region, thus permitting rapid charging of the capacitors in the diode holding circuit without drawing grid current.

Diode Holding Circuit.

Two 6AL5 diodes in series charge the holding capacitor to the peak sample voltage. The low forward resistance permits complete charging of the capacitor in .3 microsecond.

Holding Circuit Cathode Follower, V_{3a}.

The diode holding capacitor voltage is fed to the grid of a cathode follower consisting of one section of a 2C51. The low impedance output charges the RC exponential decay combination through another diode holding network. The output reference level of the cathode follower is adjusted by a potentiometer R1 in the grid circuit of the input cathode follower.

Exponential Decay.

The time constant of the RC decay circuits can be adjusted by trimmer condensers to either 5 microseconds or 10 microseconds giving either 10% or 5% accuracy of quantization.

Cathode Follower Driven by Decay Circuit, V3b.

A cathode follower isolates the exponential decay from the amplifier grid circuit. This prevents loading of the decay network by shunt resistance and Miller capacitance.

Two Stage Amplifier, V5.

The output of V3b is direct coupled to a two-stage amplifier consisting of direct coupled 2C51 triodes. Potentiometer R2 sets the grid bias of the first stage for maximum amplification at the threshold level. A germanium diode prevents grid current flow in the first amplifier stage and overloading of the cathode follower output when the output of the decay circuit is large. Potentiometer R3 adjusts the grid bias of the second amplifier and thereby controls the comparison level the following amplitude comparator.

Amplitude Comparator, V_6.

The amplitude comparator is a conventional Schmidt circuit. It is turned on when the input to the RC network exceeds the comparator threshold and is turned off when the exponential voltage decays below the threshold. Because of the high gain amplifier which drives it, the comparator hysteresis has negligible effect on the overall performance of the quantizer.

The comparator output pulse is differentiated and the leading edge pulse used to trigger a delay multivibrator. The trailing edge pulse is used to trigger off the reset flip-flop.

Delay Multivibrator, V_7, and Blocking Oscillator, V_8.

The delay MV is a one-shot 12AT7 multivibrator with a quasi-stable state of approximately 10 microseconds. The trailing edge of the pulse is differentiated in a pulse transformer and used to trigger a 2-microsecond 12AT7 blocking oscillator. The blocking oscillator output pulse is fed to the control grid of the 6AS6 double coincidence gate. The delay period is arbitrary in length. It permits the input sample to reach its maximum before quantization begins.

One Megacycle Oscillator, V_{11}.

Accurately spaced .1 microsecond pulses are obtained from a one megacycle free-running electron coupled oscillator. A 6CL6 pentode is operated as a Class C Hartley oscillator. Negative output pulses are derived from the plate. These are inverted in a pulse transformer. The pulses are then fed into the 6AS6 double coincidence gates.

Double Coincidence Gate, V_{10}.

This is a gate which passes the one megacycle pulse when there is coincidence between one of these pulses and the blocking oscillator pulse. The output pulse triggers the reset flip-flop on.

Reset Flip-Flop, V_9, and Clear Switch, V_{13}.

The reset flip-flop is a long-duration one-shot 12AT7 multivibrator. The output pulse drives the normally cutoff 2C51 clear switch into conduction, discharging the diode holding capacitor and starting the exponential decay. The output gate pulse is also supplied to the output 6AS6 double coincidence gate.

Double Coincidence Output Gate, V_{12}.

This is another 6AS6 gate which passes the one megacycle pulses which occur at the same time as the reset flip-flop pulse. These two are in coincidence during the time that the exponential is above the preset threshold. The output pulses are 30 volts in amplitude and of .1 microsecond duration.

Timing Logic Diagram.

Idealized waveforms of the quantizer are shown in Fig. 6, illustrating the timing logic of the quantizer.

In all pulse circuits, timing will be affected by unavoidable delays in pulse transmission. In the quantizer there is a delay between the "on" triggering of the reset flip-flop and the start of the exponential decay. There is also a delay between the time the exponential decay falls through the threshold level and the "off" triggering of the reset flip-flop. These delays are constant regardless of the magnitude of the voltage sample. Because of the nature of the exponential decay, the delays are equivalent only to a change in the threshold level. Their effect can be completely eliminated by a simple adjustment of the threshold level. Delay lines are not necessary.

A more recent, somewhat simpler, version of the quantizer is shown in block diagram form in Fig. 7. Its feature is a gated one megacycle blocking-oscillator which eliminates the need for the coincidence circuits. The timing logic is the same.

EXPERIMENTAL RESULTS

The quantizer shown in Fig. 8 was tested with one microsecond inout pulses at a two kilocycle PRF. Adjustments are made in three steps. First, the input pulse is set at 3.3 volts amplitude and R2 is adjusted until one pulse is observed at the output. The input pulse is then set at 100 volts. With switch S1 in the 10% position, trimmer condenser C1 is adjusted until 18 output pulses are observed. Then with S1 in the 5% position, trimmer C2 is adjusted until 35 output pulses are observed. For proper logarithmic quantization, it was found that R1 should be set so that the voltage at the output of the holding circuit cathode follower is -.75 volts.

The voltage increment corresponding to each quantization interval is determined by measuring the change in input voltage at which the number of output pulses changes by one. Figure 9 shows the theoretical transition voltages for 5% and 10% quantization. Results of typical runs at 5% and 10% quantization settings are shown in Fig. 9. The straight line passes through the theoretical quantization voltages. The odd-numbered 5% quantization levels correspond to the 10% quantization levels. The experimental points for these levels only are shown.

The overall accuracy of the quantizer at present is 12% for the nominal 10% range and 7% for the nominal 5% range. This has been caused principally by the difficulty of obtaining linearity in the cathode follower stages over the wide range of input sample voltages. Drift in the transition voltages is negligible.

APPLICATIONS

Any quantity which can be converted into an analog voltage can be quantized logarithmically.

In its present application, the quantizer is used to measure to 5% accuracy the time interval between two successive pulses whose separation may vary between 1 and 27,000 microseconds. Three linear sweeps 1 - 30 microseconds, 30 -900 microseconds, 900 - 2700 are generated in sequence. Each range is quantized into 32 levels. The first pulse starts the sequence operation; the second pulse terminates the sweep and starts the quantization. When the sweep switches to the next higher range, 32 counts are read into the counter which measures pulse separation.

Multiplication of any two quantities expressible as analog voltages is performed by logarithmic quantization of the inputs and their addition in a counter. The sum is the logarithm of the product of the two quantities. Division is performed by subtraction of the logarithms. In this connection it should be noted that the quantizer takes the logarithm of the ratio $\frac{E}{E_T}$. Therefore, in multiplication of E_a and E_b,

$$\log \frac{E_a}{E_T} + \log \frac{E_b}{E_T} = \log \frac{E_a E_b}{E_T^2}, \quad (24)$$

and in division

$$\log \frac{E_a}{E_T} - \log \frac{E_b}{E_T} = \log \frac{E_a}{E_b}. \quad (25)$$

If E_T is made equal to ϵ in the design of the quantizer, multiplication of E_a and E_b yields

$$\log \frac{E_a}{\epsilon} + \log \frac{E_b}{\epsilon} = \log E_a E_b - 2. \quad (26)$$

If E_T is made 1,

$$\log \frac{E_a}{1} + \log \frac{E_b}{1} = \log E_a E_b. \quad (27)$$

The quantizer can be used to sample and code a complex wave. Sampling is performed by synchronizing the quantizer at evenly spaced intervals equal to one over twice the signal bandwidth. The quantization accuracy, range, and timing interval determine the upper limit on the bandwidth of the signal which the quantizer can handle, as shown in Eq. (23) where F' is twice the bandwidth of the sampled signal.

The quantizer will permit measurement of amplitudes of pulses whose durations are as short as one-half microsecond. Repetitive pulse trains are not necessary since only a single pulse is used for the measurement.

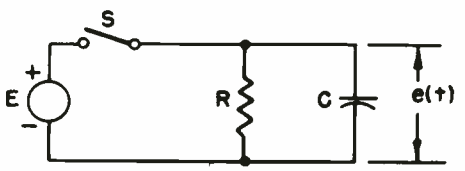


Fig. 1

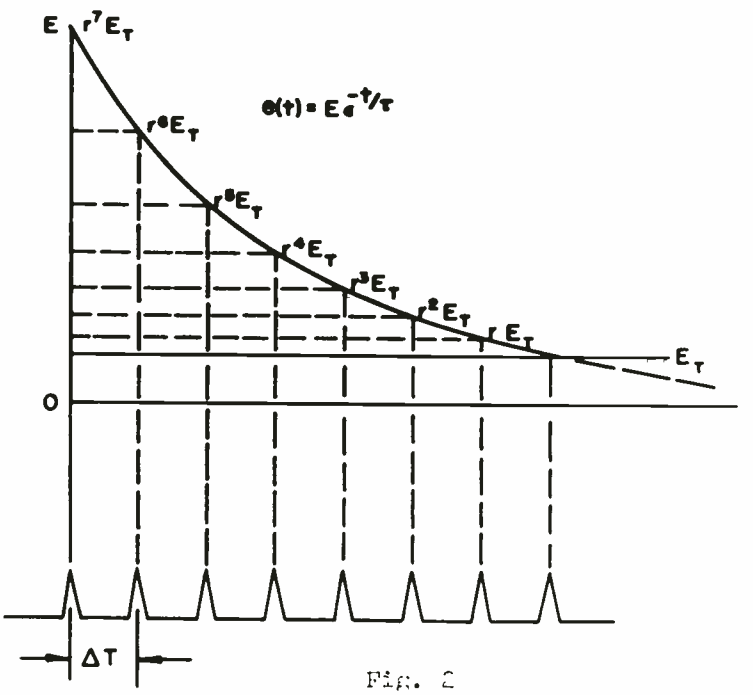


Fig. 2

QUANTIZATION LEVEL AND QUANTIZED VOLTAGE
VS. INPUT VOLTAGE

S=.05 (5% QUANT.)			S=.10 (10% QUANT.)		
INPUT VOLTAGE	QUANT. LEVEL	$\bar{E}_n$	INPUT VOLTAGE	QUANT. LEVEL	$\bar{E}_n$
3.33-3.68	1	3.51	3.33-4.07	1	3.70
3.68-4.07	2	3.88			
4.07-4.50	3	4.29	4.07-4.97	2	4.52
4.50-4.97	4	4.74			
4.97-5.49	5	5.23	4.97-6.07	3	5.52
5.49-6.07	6	5.78			
6.07-6.71	7	6.39	6.07-7.41	4	6.74
6.71-7.41	8	7.06			
7.41-8.19	9	7.80	7.41-9.05	5	8.23
8.19-9.05	10	8.62			
9.05-10.0	11	9.53	9.05-11.1	6	10.1
10.0-11.1	12	10.6			
11.1-12.2	13	11.7	11.1-13.5	7	12.3
12.2-13.5	14	12.9			
13.5-14.9	15	14.2	13.5-16.5	8	15.0
14.9-16.5	16	15.7			
16.5-18.2	17	17.4	16.5-20.1	9	18.3
18.2-20.1	18	19.2			
20.1-22.2	19	21.2	20.1-24.6	10	22.4
22.2-24.6	20	23.4			
24.6-27.2	21	25.9	24.6-30.1	11	27.4
27.2-30.1	22	28.7			
30.1-33.3	23	31.7	30.1-36.8	12	33.5
33.3-36.8	24	35.1			
36.8-40.6	25	38.7	36.8-44.9	13	40.9
40.6-44.9	26	42.8			
44.9-49.6	27	47.3	44.9-54.8	14	49.9
49.6-54.8	28	54.2			
54.8-60.6	29	57.7	54.8-67.0	15	60.9
60.6-67.0	30	63.8			
67.0-74.1	31	70.6	67.0-81.9	16	74.5
74.1-81.9	32	78.0			
81.9-90.5	33	86.2	81.9-100.0	17	91.0
90.5-100.0	34	95.3			

Fig. 3

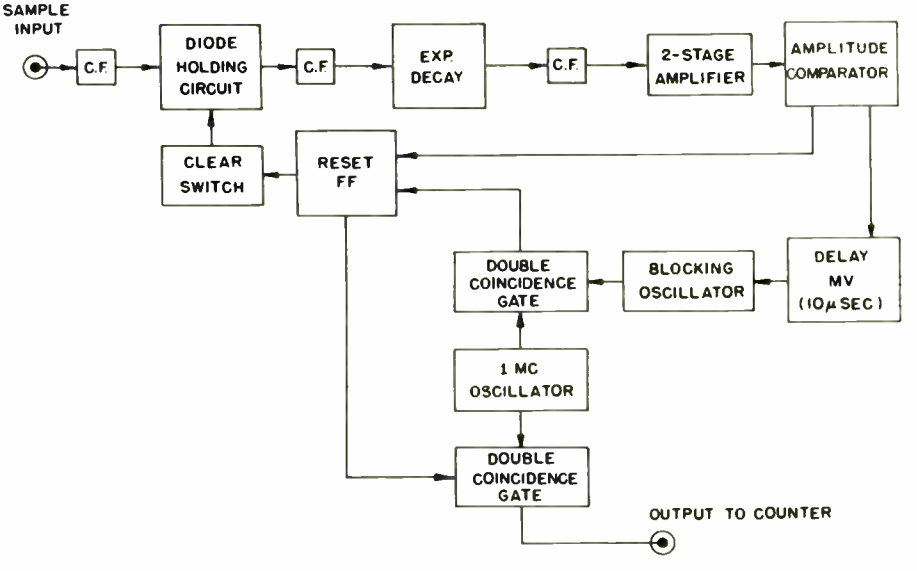


Fig. 4

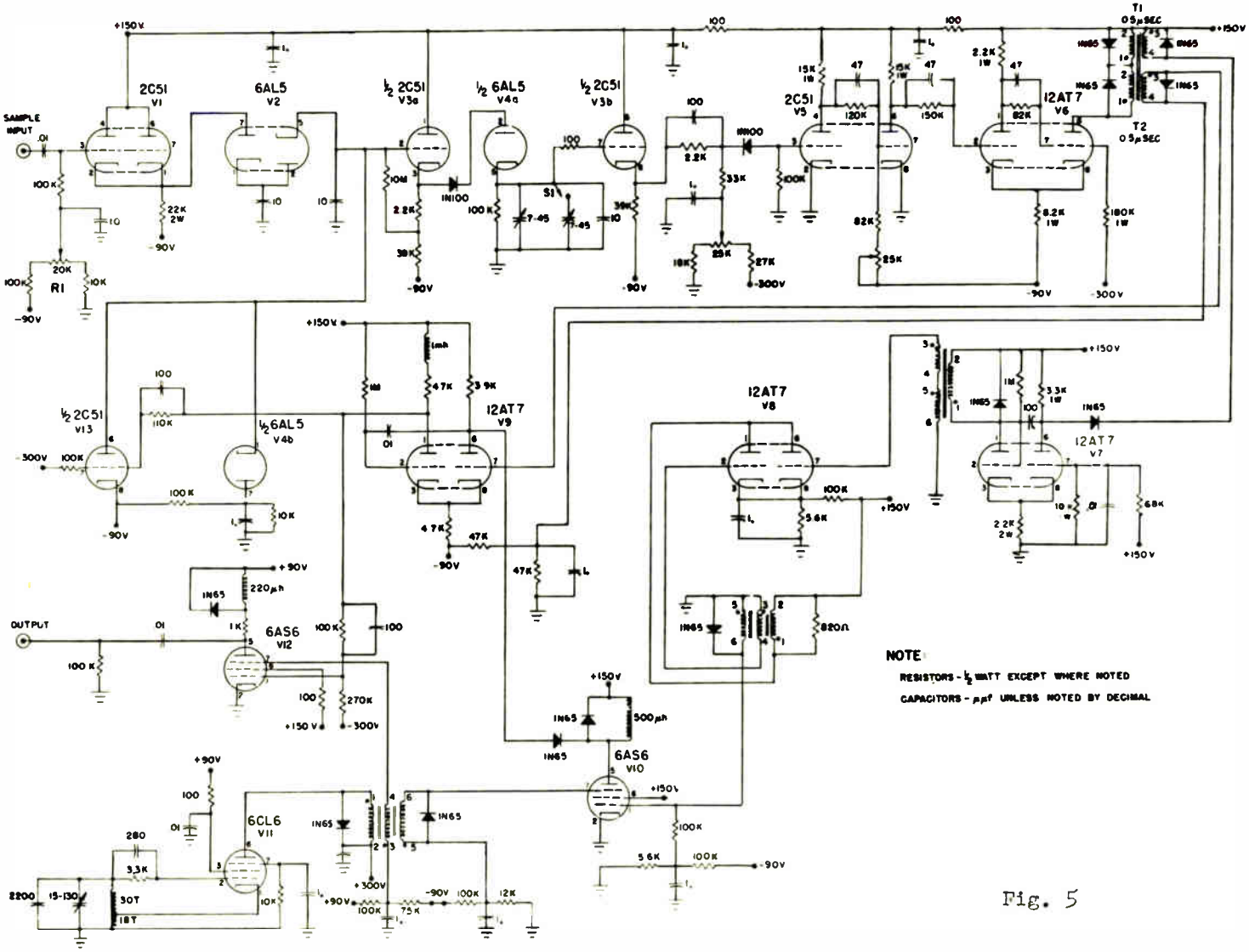


Fig. 5

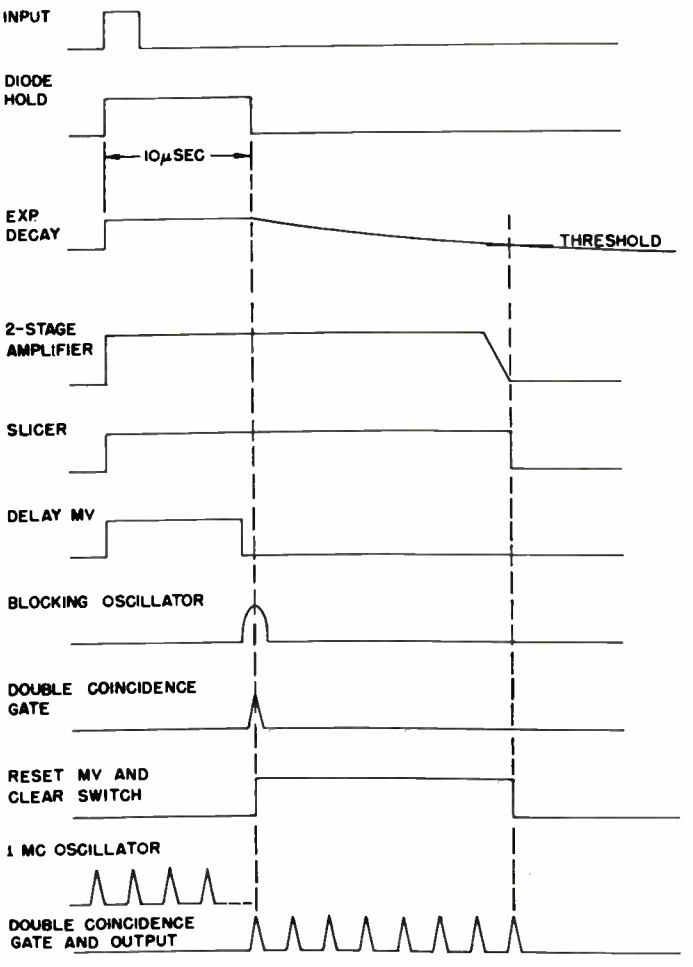


Fig. 6

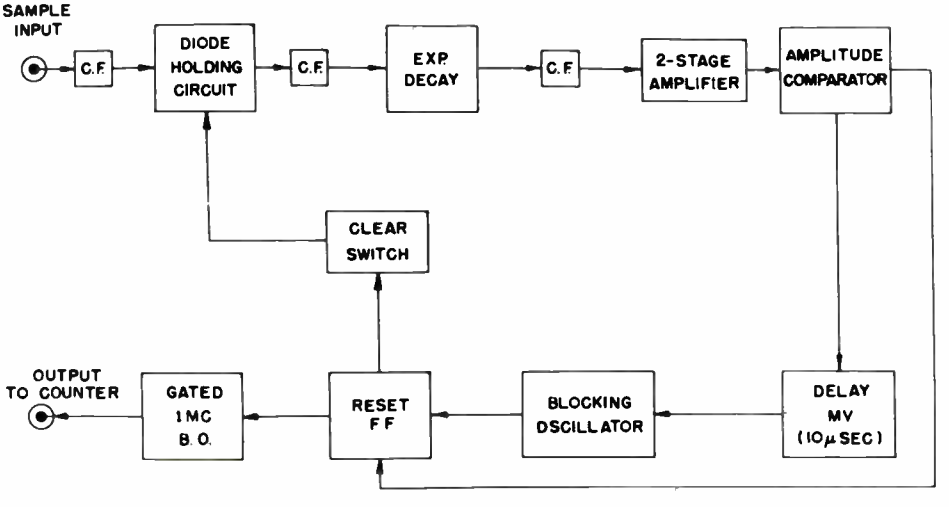


Fig. 7

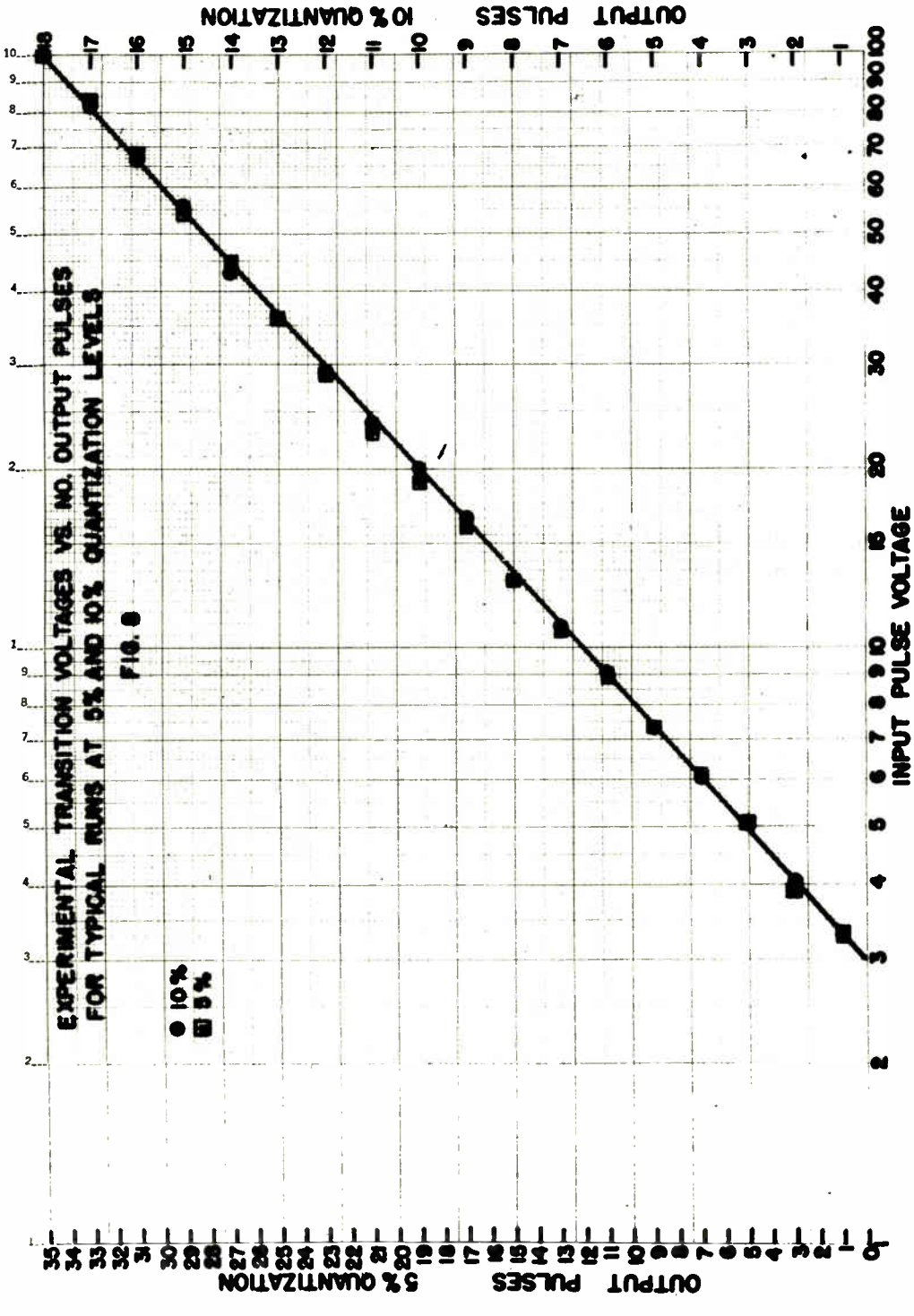


Fig. 8

NUMBER OF PULSES VS. TRANSITION VOLTAGE

TRANSITION VOLTAGE	NUMBER OF PULSES	
	5% QUANT.	10% QUANT
3.33	1	1
3.68	2	
4.07	3	2
4.50	4	
4.97	5	3
5.49	6	
6.07	7	4
6.71	8	
7.41	9	5
8.19	10	
9.05	11	6
10.0	12	
11.1	13	7
12.2	14	
13.5	15	8
14.9	16	
16.5	17	9
18.2	18	
20.1	19	10
22.2	20	
24.6	21	11
27.2	22	
30.1	23	12
33.3	24	
36.8	25	13
40.6	26	
44.9	27	14
49.6	28	
54.8	29	15
60.6	30	
67.0	31	16
74.1	32	
81.9	33	17
90.5	34	
100.0	35	18

Fig. 9

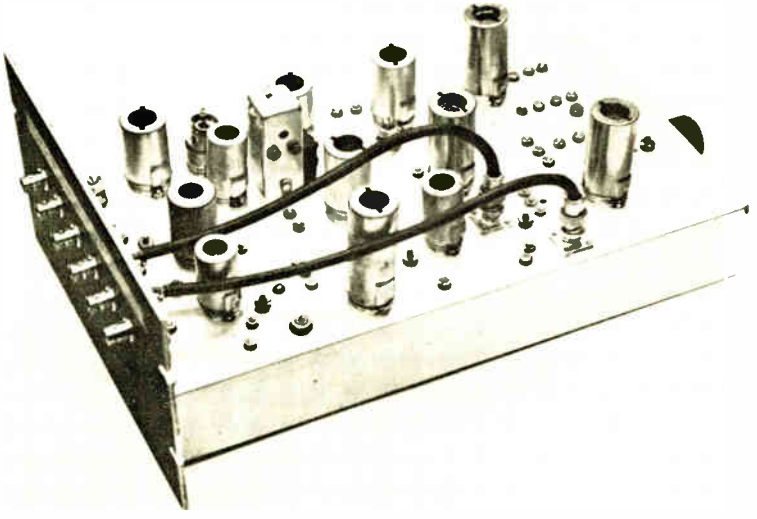


Fig. 10

A DIGITAL CONVERTER

Jack B. Speller

The Norden Laboratories Corporation
White Plains, New York

Introduction

One of the important requirements of a digital computing system may be to convert shaft motion into digital notation. A digital converter, with a shaft rotation as the input and electrical signals in the natural binary code as the output, was designed to satisfy this requirement.

Characteristics

General

Figure 1 is a block diagram of a system using the converter as an input device to a digital computer.

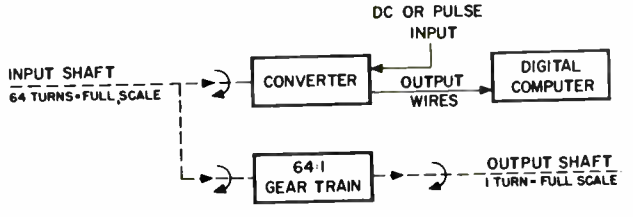


Fig. 1 - System block diagram.

When the input shaft is rotated 64 turns, the unit travels its full scale of thirteen binary digits or 0 through 8191. Sixteen wires carry the thirteen digit number in parallel to the digital computer.

The input to the converter may be D.C., A.C. or pulse voltages.

By connecting a precise 64:1 gear train to the input shaft, the output shaft of the gear train will rotate one turn for the full scale of the converter and its position will be known to about one part in 16,000.

Physical

Figure 2 is a picture of the instrument. The aluminum case is 1 3/4 inches in diameter and 2 3/4 inches long, exclusive of input shaft and plug. It weighs less than 7 ounces. The converter is provided with a standard synchro mounting.

Layout

Figure 3 is an inside view of the converter.

Fig. 2

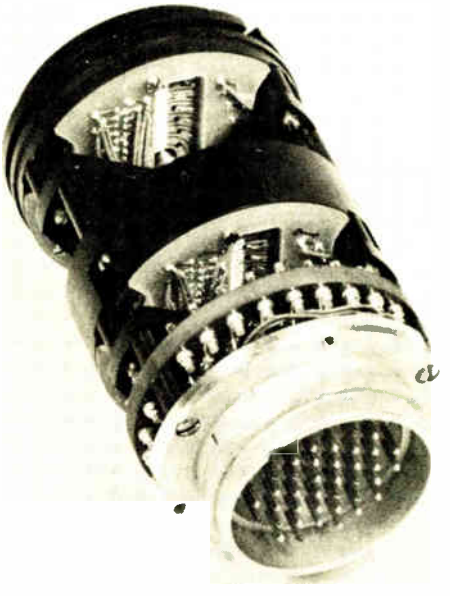


Fig. 3

Two disks, which have a unique pattern on them, provide the switching for the unambiguous binary output. The high speed disk may be seen at the forward end of the unit, while the low speed disk is seen at the rear. Small metal brushes conduct the currents to and from the disks. In the space between the two disks is a 64:1 gear train connecting the high speed disk to the low speed disk. Twenty-four isolation crystals are mounted at the rear of the unit. Sufficient pins are in the plug to simultaneously provide the binary number and its complement.

Electrical Output

When a "1" is on an output wire, the voltage is high. When a "0" is represented, then the voltage is low. The values of the voltages are arbitrary although it is desireable to keep the voltages below 35 volts.

How It Works

Logic

Four brushes per digit are used to achieve an unambiguous binary output without transformations. One of two commutator brushes are selected by the output of the previous digit. The brush selected always contacts the central portion of the segment. As a result, the brush is not required to make or break current at the edge of segment. Both tolerances and wear qualities of disks and brushes are thus helped. The third and fourth brushes remove the voltage from the disk through slip-rings. The output of these brushes are then fed through crystals into the commutator brushes of the next digit and the process repeated.

The input digit has only two brushes, commutator and slip-ring brushes. The push-pull action of the input circuit provides the voltages to the commutator brushes of the second least significant digit. Other input circuits may be used with advantages under certain conditions.

Operation

A schematic presentation of the disk pattern and converter circuit are shown in Figure 4.

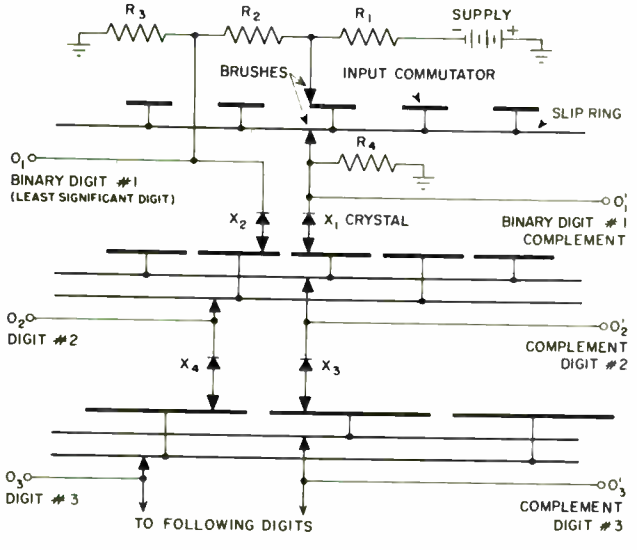


Fig. 4 - Converter schematic.

Resistors R_1, R_2, R_3 and R_4 make up the input circuit. The bars are the commutator segments on the disk while the horizontal lines represent slip-rings. The arrow heads are small metal brushes. The top row is the least significant digit. The next significant digit is the second row from the top, and so forth. By moving all the brushes along the commutator segments, the switching action may be checked.

Since the position shown in Figure 4 represents the zero position of the shaft, all the outputs O_1, O_2, O_3, etc., have zeros. The complement outputs, O^1_1, O^1_2, O^1_3, etc., have ones. The zeros in this case are not zero voltages but rather an arbitrary value given by the ratio of R_2 and R_3 and that current flowing through R4. Now the voltage at O^1_1, passes through crystal X_1, the commutator and slip-ring assembly to output O^1_2. O^1_3 and the ten remaining complementary digits are derived in a similar manner. They all have "1"s.

Now move all the brushes to the right so that the input brush is not making contact with the input commutator. Since R4 is no longer connected to the junction of R_1 and R_2, the voltage at the O^1_1 changes to zero and the voltage at the junction of R_2 and R_3 increases negatively to produce a "1" at the output O_1. Crystal X_2 now passes voltage to the commutator and slip-ring previously energized by X_1. Output O^1_2 is, therefore, still energized as before when the brush assembly was in its original position. Since no energized crystals are touching the commutator-slip-ring-assembly connected to output O_2, O_2 is at zero voltage, representing a "0". Similarly, O_3 is at zero voltage and represents a "0".

Thus the output changed from 000 to 001 by moving the brush assembly one segment width to the right. Moving the assembly another segment width to the right will produce the natural binary number 010. The procedure may be continued until the 13 digit binary number has all "1"s at the outputs O_1 through O_{13}. At this time all "0"s will be found at outputs O^1_1 through O^1_{13}.

The crystals are inserted to prevent voltage being fed back into the previous digit when both brushes are on a single segment. Twenty-four of these crystals are used in a thirteen digit converter.

Disk Pattern

As may be seen from Figure 5, the commutator segments increase in size

by approximately a factor of two moving from outside to the inside of the pattern.

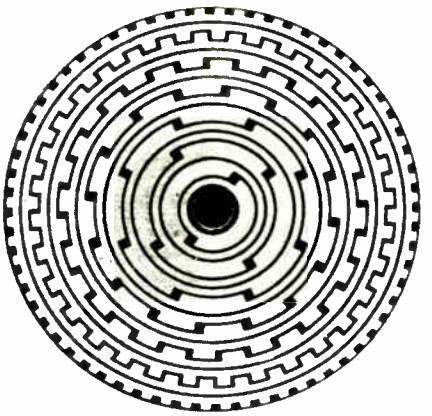


Fig. 5

The brush that is on the center half of the commutator segment is always the one that is energized. Therefore, the tolerance of brush alignment, segment position and insulation may be plus or minus one-quarter of a segment width. As the segments increase in size as the digit becomes more significant, so increases the permissible tolerances and insulation.

Circuit

The schematic is the same for all thirteen digits. The first seven digits are on the high speed disk while the last six digits are on the slow speed disk. The output of the seventh digit merely couples into the first (or the eighth digit) digit of the slow speed disk.

Capabilities

Unambiguous Thirteen Digit Binary Number

The converter produces an unambiguous thirteen digit number in the natural binary code without any transformations. This is done using a pattern which selects the brush which is in the center half of the commutator segment.

High Reading Rate

The digits are available nearly simultaneously thus allowing a high reading rate - about 10^6/second. The complement of the binary number is also simultaneously available.

Clockwise or Counterwise Motion

Clockwise and counterwise motion can produce increasing numbers merely by selecting the appropriate output wires.

Low Torque

The torque required to turn the input shaft is uniform and low, about 0.2 in-oz. The input shaft can be turned at 200 rpm and higher. The life depends upon the operation required of the instrument.

Various Types of Input Voltages

D.C., A.C. or pulse voltages may be fed into the unit depending upon the application.

Greater Number of Digits

By adding an additional disk and a 64:1 gear train, a nineteen digit instrument is produced with a count of over a half a million. The number of digits is practically unlimited.

Use As An Input Or Output Unit

The converter may be used as an input device for a digital computer. Also it may be used as an output device in conjunction with a servo loop.

Other Codes

Binary-decimal and other codes may be used in the converter rather than the natural binary code. However, since both the binary number and its complement are simultaneously available in the converter, a simple crystal matrix may be used to convert to the binary-decimal code, some arbitrary function, or program.

In a sense the digital converter is to a digital system as a synchro or a potentiometer is to an analogue system.

EFFICIENT LINKAGE OF GRAPHICAL DATA WITH DIGITAL COMPUTERS

E. D. Lucas, Jr.
President, Best Electronics Corporation
Beverly Hills, California

My first look at an early digital computer was in 1942 when the author was a lowly lieutenant (j.g.) in the United States Naval Reserve. It was housed in a room at M.I.T. where Professor Edgerton and his group had, several years before, done the pioneer work on the stroboscope and its applications to highspeed photography.

My guide was Professor Louis Woodruff, a co-author of one of the standard preliminary texts for those studying radar, namely "Ultra-High Frequency Techniques". Woodruff was also an excellent squash racquets player and the inventor of an automatic bridge table which dealt four hands rapidly and systematically while the human players struggled imperfectly with the machine's previous "square deal". This particular invention was less successful commercially than the professor's many other inventions, but should have been a boon to duplicate clubs, it would appear.

So much for invention and introduction, the former hazardous for both inventor and associates only too often, the latter obnoxious for both writer and reader.

Advances in Computers

As everyone familiar with the art knows, the progress in computer design in the past 12 years has been formidable. To illustrate this point, since the author has no photograph of the room strung with cables, cluttered with racks of plug-ins and diodes, its benches loaded with overworked oscilloscopes, vintage 1942, it is suggested that one admire the many articles and photographs describing such modern computers as the large IBM 701, Univac, SWAC, and other so-called "giant brains" or the more modest general-purpose digital computers including the CRC 102-A, Elicom, Alwac, Circle, and the new models being built by J. B. Rea Company in Santa Monica.

The CRC 102-A, for example, built by The National Cash Register Company, Electronics Division, formerly Computer Research Corporation of California, is the 1954 model of an earlier general-purpose computer, the CADAC, built under Government contract for M.I.T.

This is a digital computer utilizing a magnetic drum with a storage of 1024 words of 42-bit length, plus a high-speed access buffer register having a capacity of eight words. One of the most attractive features of this computer is the variety and speed of input and output devices which may be connected to it, as illustrated in Figure 1.

Input-Output Devices

In connection with reading scientific and engineering data, one problem is transfer of data on graphical records into such digital form as to be immediately useful to a computer. The complementary problem is converting computed digital data into graphical form.

A recently developed machine, the Benson-Lehner OSCAR, makes possible the graphical solution of a wide variety of problems in analyzing and reading oscillographic records. By the use of two simple manual controls, which operate two 5000-ohm precision linear potentiometers and are connected to the resistance bridge in any of a number of analog-to-digital converters, the operator of this OSCAR machine can perform both arithmetic and algebraic operations automatically while reading multi-channel traces.

For example, the simple arithmetic processes of addition, subtraction, multiplication and division can be applied to oscillograph traces merely by shifting a linear overlay. See Figure 2.

This is a plastic overlay or "tongue depressor" of varying lengths -- usually lucite 4", 6", 9" or 12" long, depending on the application, and with a scribed center line. The overlay is held in a steel clamp attached to a vertical steel overlay bar, and the clamp may be moved up or down on the bar. By moving the clamp up or down, the reference line relative to the center of the lucite overlay is also moved, and thus numerical values adding to or subtracting from an original reference line on the oscillograph record may be obtained quickly by a simple manual adjustment.

For multiplication, the plastic overlay is tilted at an angle, and a numerical value is set on the analog-to-digital converter, whether it be the Benson-Lehner Decimal Converter or Electronolog, a modified Giannini disc converter, or some other type of ADC*. Suppose that the value of 1000 units is established in the analog-to-decimal converter for a certain angle of the overlay, which corresponds to full travel from left to right of the left potentiometer control (used for measuring Y amplitudes). Then, as shown in Figure 3, the process of multiplication may be achieved graphically merely by increasing the angle of tilt of the linear overlay.

If division is required, the tilt angle of the overlay is reduced.

* ADC is an abbreviation for analog-to-digital converter.

For measuring such ΔX or incremental X values on oscillograph records as, for instance, time history, phase shift, amplitude of period of a sinusoidal oscillation, peak-to-peak amplitude and others, the linear overlay is placed vertically in the clamp holder. Then the movement of the overlay from a vertical reference line permanently scribed on a plastic underlay or "reference overlay" is measured electrically by the manual movement of the OSCAR left control, which operates a 5K potentiometer, as mentioned before. In this way, it is easy to determine numerical values for phase shift, for instance, using an ADC connected to the oscillograph trace reader.

Since most oscillograph records are non-linear, however, and non linear calibrations must be applied in a majority of cases, it is convenient to apply these directly while reading the records. This may be done with the OSCAR by using a rectangular plastic overlay on which is scribed a suitable calibration curve.

The recommended procedure for accuracy is to utilize a Pantograph (Keuffel & Esser), an instrument which makes it possible to take an existing calibration curve of practically any useful dimensions and transcribe it on the rectangular plastic overlay.

In this way corrections for electrical or mechanical hysteresis, or logarithmic, trigonometric and exponential functions, and many others may be made, using the calibration curve scribed on the rectangular overlay rather than the straight line of the linear overlay previously described.

Because of the limitations in length of this paper, it is recommended that the reader who is not familiar with the operations of such oscillograph trace readers as the OSCAR obtain a copy of the operations manual supplied by the manufacturer, as well as the instructions for operating the Pantograph. The Benson-Lehner operations manual contains detailed drawings and instructions as to how to solve such problems as vector analysis by using the oscillograph trace reader and associated ADC equipment.

It might be noted that a relatively simple instrument such as the OSCAR, and similar trace readers made by such companies as Telecomputing Corporation and others, are dependent for their success on the ingenuity of the operator or "programmer". Thus a training course for operators, who are usually girls with some mathematical background, is essential. The author recently gave such a course, which was attended by six male students and only one female. However, the men were destined to instruct female operators and by the end of the week were prepared to instruct the instructor, which made it a highly successful short course.

During this course, a number of special problems with applications in the aircraft and guided missile fields were discussed, and graphical methods for rapid reduction of data from oscillograph records were obtained. For instance, by tilting a linear overlay and then using it to measure incremental X values, it is possible to measure varying amounts of phase shift of one oscillograph trace as compared with a full cycle (360°) of another sinusoidal trace on the same record. This was a problem bothering an engineer at Convair, San Diego, to obtain phase shift in degrees as a fraction of the amplitude of a second trace, when both the original amplitude and the phase shift are varying non-linearly.

Reading Film Records

Just as in the case of oscillograph records, film records such as Askania, Contraves and other theodolite records, high-speed motion picture films, and dial films and manometer tube films are classified as a necessary nuisance by those required to reduce the data obtained on such records.

The simplest instrument is the Recordak (Eastman Kodak), widely used for reading dial film taken in aircraft flights and other similar applications. To speed the process of reading such films, which are merely enlarged and moved forward, frame by frame, by the Recordak, one technique utilized by many companies, including the General Electric jet engine test laboratory at Edwards Air Force Base, is to provide for the operator a remote keyboard connected to an electric typewriter. One version of this is the Benson-Lehner Electrotyper Model F, which makes it possible for the operator to read dial numbers and type them immediately on a prepared form, with the correct number of tab stops set for the desired number of columns.

Another type of reader is the BOSCAR, which permits reading either 16 mm or 35 mm (single or double frame) film records, frame by frame. This film reader utilizes a spot or cross of light which is placed over the point the coordinates of which are desired. The light spot is controlled by a small "joystick" which, through mechanical linkage, establishes the electrical position of two 10K potentiometers.

The reading is done at the rate of from 10 to 30 points per minute by pointing the light spot at each point to be read, and pressing read-out controls for X and Y either separately or simultaneously. As the desired points -- for example, position of guided missile and target -- on each frame are read, the next frame moves into position with positive pin registration. Alignment is accurate to 0.0005" at the film plane.

Present applications of this machine include reading X-Y coordinates of ballistics and theodolite films where it is often desirable to utilize several numerical scales on the associated ADC and print-out devices. This is necessary where corrections must be made for variations in azimuth and elevation, for instance. Manometer

tube and dial films may also be read with this machine.

Digitizing Graphical Data for Computer Input

It might also be mentioned that there are numerous other semi-automatic machines for reading film records, including the Coleman, Iconolog (developed by Douglas Aircraft) and others. The Research Institute of the University of Denver and other research laboratories are at present working to develop high-speed automatic methods for reading various forms of film records, including 16 mm, 35 mm single and double frame, 70 mm and even wider records. The author believes that it is entirely possible to develop such machines and to utilize new techniques for high-speed analog-to-digital conversion and magnetic tape recording so as to make the entire process of reading film records at least 10 times as fast as by the present semi-automatic techniques.

Other techniques for reading film records include those developed by Telecomputing, and a variation of the Benson-Lehner OSCAR, the newly developed Model F, which includes a film drive mechanism and interchangeable projectors for handling continuous 16 mm and 35 mm film records, and which may also be utilized for reading wider films, considered as though they were paper oscillograph records.

Digitizing Graphical Data for Computer Input

Among the many types of ADC equipment available for use with such oscillograph and film readers as the OSCAR and BOSCAR are:

a. A resistance-bridge decimal converter
b. An analog-to-digital voltmeter
c. A shaft digitizer.

Considering first the decimal converter, its action is to convert resistance values from 5K potentiometer outputs from an oscillograph trace reader (or any other analog source) into digital values by means of a self-balancing bridge containing an amplifier and a null detector. This converter also provides zero settings and scaling controls for up to eight output channels from the film or oscillograph readers, including one X and seven Y readings.

This converter has a numerical range from -999 to +999, and thus an effective span of approximately 2000 counts. Accuracy is $\pm$ 0.1% if the ADC is correctly aligned and operated by a trained operator. Since the zero potentiometer for each output channel may be set at any desired numerical value in this range, addition and subtration may be applied automatically before the output data is tabulated or punched on business-machine cards or paper tape. Similarly, by changing the scaling potentiometers, it is possible to perform multiplication or division prior to output of digitized data.

From one to three digits of fixed data may be inserted before the three-digit coordinate data obtained from the reader and converter; and there is provision by means of a switch for inserting a decimal point where desired in the six-digit number. Thus, for example, a typical Y_1 reading would be 924.053, where the first three fixed digits "924" may refer to the record number (or any other desired pre-set three-digit number) and "053" is the numerical value of Y_1 as read from the oscillograph trace or film record.

Additional fixed data input and decimal point insertion, up to a total of 10 digits, is also provided with adjustable switch controls. This is useful for identifying recorded data by date, operator's number, etc., prior to computation.

A second form of digitizer includes a relatively new digital voltmeter, manufactured by Non-Linear Systems, Inc., Del Mar, California, with many desirable features. The design utilizes etched circuit techniques and the data presentation provides for up to five digits as well as sign ($\pm$). Sensitivity is from 1 mil (0.001 volt) to 100 volts, if desired, although a more typical input range is from 1 mil to 10 volts. To utilize this digital voltmeter with resistance inputs from machines such as the OSCAR and BOSCAR, it is necessary to provide an input matrix. Also output circuitry is required so as to operate such machines as a modified IBM electric typewriter, a Flexowriter, or an IBM key punch.

Advantages of the digital-voltmeter ADC include relatively small size and low cost. Its principal disadvantages are that output data may be obtained from only two channels, one X and one Y; and both channels must have the same zero setting and scaling. Decimal point insertion is provided, but no fixed data input. This digitizer, therefore, lacks some of the flexibility of the decimal converter.

A third type is a shaft digitizer, such as those manufactured by Genisco and L. P. Giannini, which will provide a single channel of output data over a typical range of 1000 counts (000 to 999). This may also be included in an ADC which will accept potentiometer inputs and provide suitable output signals to operate output devices such as automatic electric typewriters and other business machines. The applications of this machine are necessarily because it can handle only one channel, either X or Y, at a time. Its virtues include economy and negligible maintenance, since it contains no vacuum tubes, and the most modern versions utilize etched or printed circuit techniques.

A variety of outputs is available from each of these three types of digitizers or ADC's, to meet the input requirements of various digital computers. Among these outputs are punched paper tapes, including Flexowriter and teletype tapes with several different codes as required; punched

business cards, that is, output to IBM and Remington Rand machines; and magnetic tapes. This latter type of output has, in the opinion of the author, the major promise for future usefulness because of both speed and accuracy, elimination of mechanical parts, and applications in fully automatic data processing systems.

It should also be mentioned that several high-speed ADC units have now been designed and constructed, chiefly for Government applications. Among the leaders in such work are Electronic Engineering of California, Los Angeles, and the J. B. Rea Company, Santa Monica. Speeds of up to 10,000 digits per second are now being achieved, taking the output from an analog computer or magnetic tape units and converting this information into digital form for input to a digital computer.

Automatic Plotting of Computed Data

Many types of automatic or semi-automatic plotting machines are now available, to accept the digital output from various computers.

There are two accepted methods of connecting digital computers to such automatic plotters:

1. To connect the plotter directly to the computer. For example, this has been done with California Computer Products plotters connected to the CRC 102-A general-purpose digital computer and Logrinc and Benson-Lehner plotters connected to the CRC 105 digital differential analyzer and to Alwac computers. In this case, the input to the computer is by means of plug-in flip-flops rather than by means of relays, and hence the plotter is timed by the computer. Also the computer can be performing computations, say, of the coordinates of desired points between intervals of plotting, since these point plotters, step plotters and curve followers operate at relatively slow speeds (30 points per minute).

2. To operate the plotter as a separate unit. For example, the Benson-Lehner Electroplotter is a large flat-bed plotter with plotting head driven by two servos, with the table size ranging in useful area from 11" x 17" to 24" x 30". Its inputs include IBM cards from any of several models of summary punch; paper tape, on special request; and keyboard (manual), as digital inputs. Analog inputs directly from the OSCAR or BOSCAR or any 5K potentiometer source are also provided.

Even more advantageous in many cases are such plotters as those manufactured by Librascope Inc., Burbank, and the Francis L. Moseley Company, Pasadena, which permit direct input from either analog or paper-tape producing devices such as the Flexowriter. One of the typical Moseley plotters (Figure 4) is a flat-bed unit which may be used either as a curve follower or a digital point plotter, at the option of the user. Its input plugs include connections either to a digital source or to an analog source. The cost is low, excellent production techniques have been achieved, and the reproducability of points compares favorably with much larger and more elaborate automatic plotting machines. Accuracy of this machine is 0.1%, and its speed is approximately 60 points per minute, which is in excess of most production plotters.

Among manufacturers of larger plotters of considerable accuracy and flexibility of input both Electronic Associates, New Jersey, and Telecomputing Corporation, Burbank, should be mentioned. The advantages of such equipment in accuracy are, in some cases, considerable. The major disadvantage is the large number of vacuum tubes used, so that both initial cost and maintenance tend to be high.

A development in high-speed automatic plotting that is of major significance is that initiated by the Computing Service Department of Northrop Aircraft, Inc., Hawthorne, California, under the direction of Rex Rice, assistant chief. A plotter with a single stylus that operates at a speed of 600 points per minute has already been developed, and was manufactured in Seattle. See the typical plot, Figure 5. With four styli, it is understood that the machine will plot up to 40 points per second, or 2400 points per minute. This is evidently a major advance in obtaining graphical output at speeds comparable with present digital printed or tabulated outputs available from numerous high-speed printers, either under development or in production.

A Glance at the Future

While presenting this paper during the recent meeting of the Western Section of the Institute of Radio Engineers, held at the Ambassador Hotel in Los Angeles, the author attempted to indicate in block-diagram form the type of completely automatic data processing system which can be visualized for future use. As presented, the diagram included inputs of FM/FM multi-channel magnetic tape, or PWM or AM tape, fed into a high-speed ADC. The latter would also accept inputs from devices such as those previously described for reading oscillograph or film records. From the high-speed ADC, the input could go into a parallel storage and delay device containing ferrite cores, with serial output to a digital computer or computers such as the CRC 102-A or the Electrodata 203. In either case, the computer could then be programmed to store the data temporarily on auxiliary magnetic tape units such as the CRC 126, which will store approximately 1,000,000 decimal digits including sign ($\pm$) and has effectively zero access time if the machine is correctly programmed. It is also possible to link more than one computer together so as to utilize several magnetic tape storage machines. From such a computing system, in which the typical operations of a digital computer (arithmetic, algebraic and logical) may be performed at high speed, the outputs may go to numerous Flexowriters or similar machines; or to high-speed

printers; or to high-speed digital plotters or curve followers.

It may also be noted that a more desirable approach to the problem is, as was pointed out in a statement by Gerhard L. Hollander of Clevite-Brush Development Co. in the question-and-answer period following this paper, to record data on magnetic tape directly in digital form, preferably in binary (bit) code as desired for input to any specific computer. It is also highly advantageous to utilize a computer with a ferrite core memory of a type similar to that being developed by Project Lincoln, M.I.T., and described by James Robert Freeman during this IRE session. With the advances in ferromagnetic memories under way by RCA, International Telemeter Corporation, National Cash Register Company, and in the laboratories of the leading business machine and computer manufacturers, it is apparent that access times in the order of microseconds rather than milliseconds will soon be commonplace.

The author invites inquiries as to any phases of this latter brief discussion, since he and his associates are now engaged in research work as to some aspects of such a completely automatic system, which permits one or two operators to process either engineering or accounting data automatically at high speed, with a presentation of both graphical (plotted) and digital (printed) data.

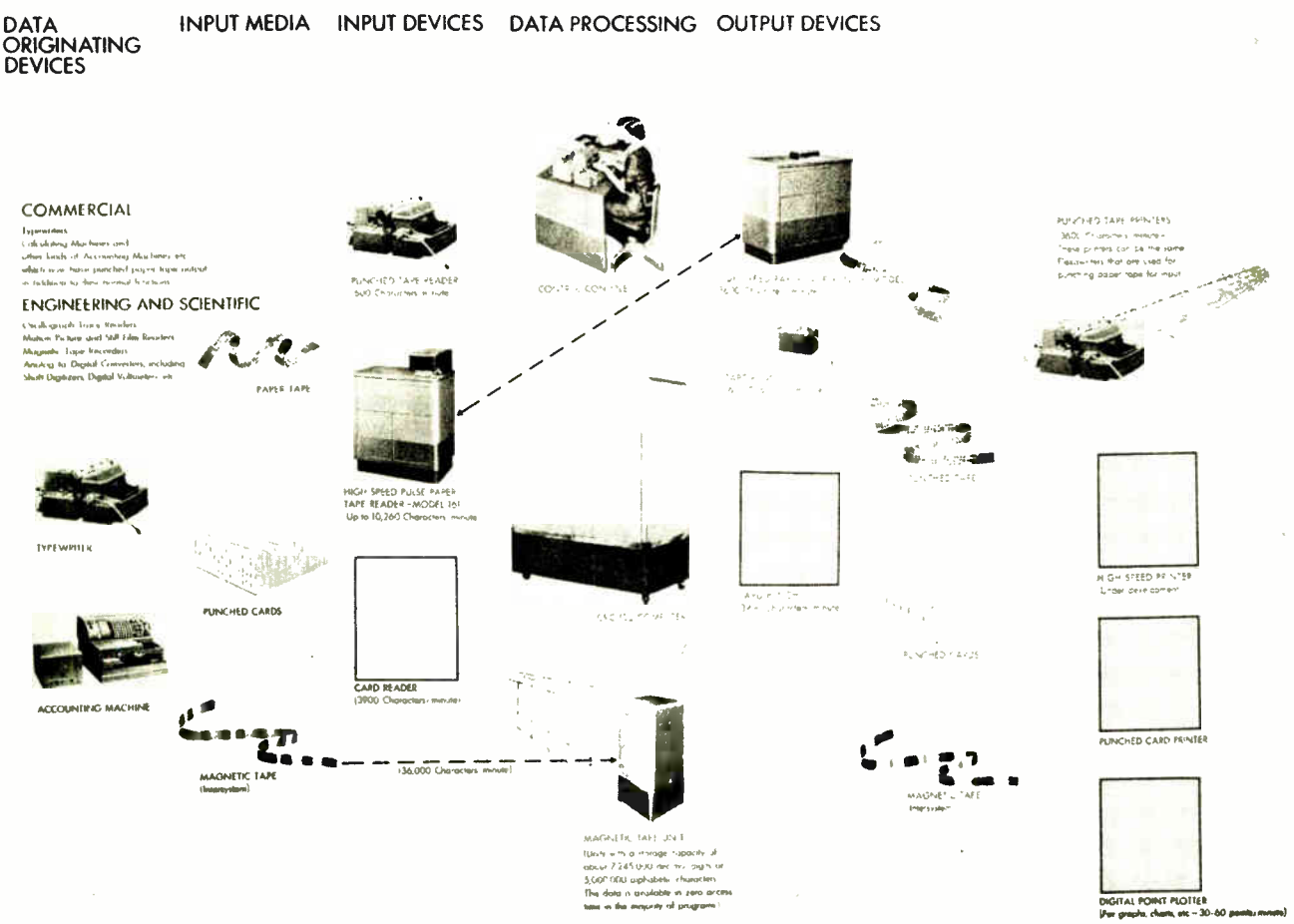


Fig. 1

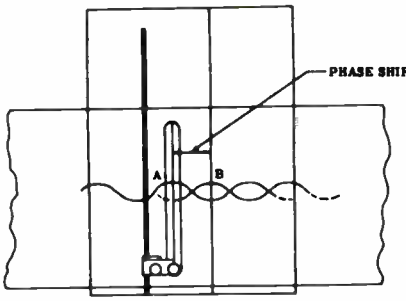


Fig. 2

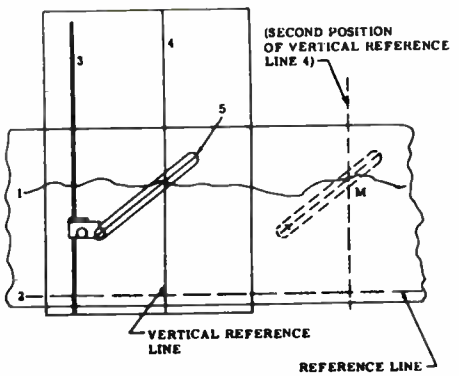


Fig. 3 - Reading Y with linear overlays.

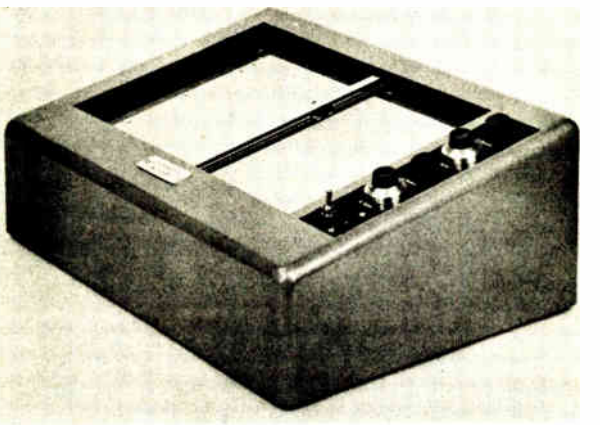


Fig. 4

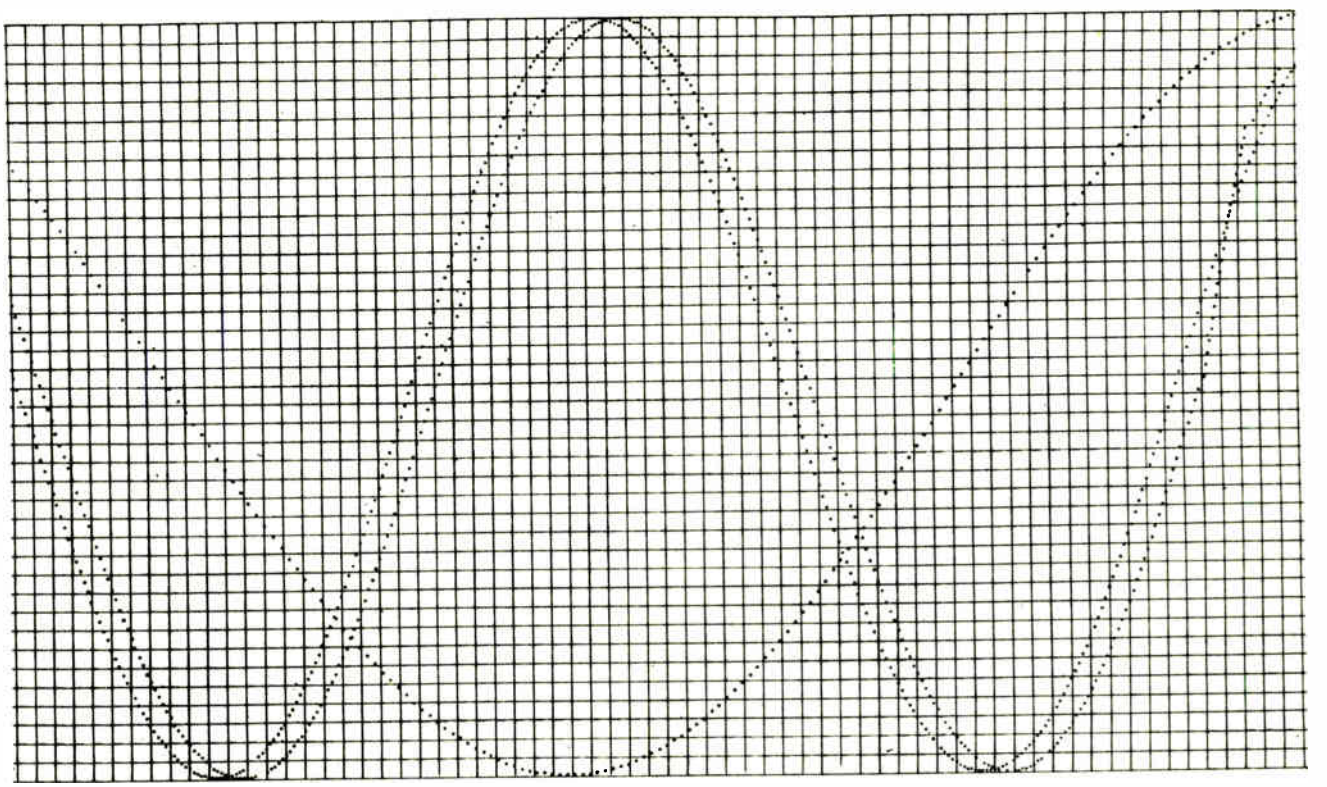


Fig. 5
Plot with Northrop High-Speed Plotter (10 points/second or 600 points/minute) utilizing one stylus.

COMPUTER CIRCUITS AND COMPONENTS

TRANSISTOR FLIP-FLOPS FOR HIGH-SPEED DIGITAL COMPUTER APPLICATIONS*

Edmund U. Cohler**
Massachusetts Institute of Technology
Lincoln Laboratory
Lexington 73, Massachusetts

INTRODUCTION

This paper is an attempt to summarize some of the designs and capabilities of conventional flip-flops employing transistors. It cannot claim to cover all possible types; it does try to give a general picture of transistor capabilities. Types with which I have had no experience, such as the slave flip-flop or dynamic flip-flop, have been neglected; those I know have been overemphasized. However, experience with these circuits is important because the conventional flip-flop forms the basis of most switching circuits, and is itself the major building block of many computers.

Computer Description:

Before I consider the flip-flops themselves it will be wise to give a short description of the computer techniques used at Lincoln Laboratory. The Whirlwind I computer and similar machines use parallel logic which achieves the ultimate in speed and flexibility by sacrificing something to large equipment counts. Most of the logic wired into the machine is implemented with flip-flops and pulse-level "and" gates. Some explanation is necessary to clarify the terminology we use at Lincoln Laboratory to describe the various types of flip-flop inputs. There are three inputs to the flip-flop: set, clear, and complement. A pulse to either the "set" or "clear" terminal will put the flip-flop into the corresponding state, while a pulse to the "complement" input will always change the state of the flip-flop. The "and" gates employed pass a pulse upon coincidence of a pulse and a high level. Most of the logical nets are realized in plug-in form using these two elements.

Another important facet of these machines should be emphasized. Parallel logic involves relatively large quantities of equipment, and thus each circuit and component must be rigidly reliable. In basic circuit design, this requires a compromise between circuit stabilization and number of components. In order to achieve this goal circuits must be made as simple as possible, without sacrifice of good stability.

Terminology:

Just as some of the circuit terminology used above is peculiar to Lincoln Laboratory, so is some of the transistor terminology. To clarify this, I will briefly describe the three states (of import to us) of the transistor. First, the state of the transistor in which it is an active element with a power amplification, is called the "active" state. Second, when the current flowing is such that the transistor appears as a low-resistance three-terminal device, like two diodes both conducting to a common cathode, it is said to be in the "on" or saturated state. Third, when it appears as a high-resistance three-terminal device, like two common-cathode diodes back biased, it is said to be "off." These terms correspond closely to the vacuum-tube states of active, saturated, and cut off.

THE TWO-TRANSISTOR POINT-CONTACT FLIP-FLOP DESIGN

The most common type of flip-flop is the two-transistor point-contact saturating circuit shown in its basic form in Figure 1. In the lower right-hand corner of Figure 1 is shown the voltage-current characteristic which one observes when looking in at points AA' with R_e removed. This characteristic is called the composite N-curve. It is easily found from the characteristics of the separate transistors and forms the basis for the design of the d-c circuit. A little

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** Formerly with the staff of Lincoln Laboratory, Massachusetts Institute of Technology, Cambridge, Massachusetts; now on active duty with the Air Force at Air Force Cambridge Research Center, Lexington, Massachusetts.

explanation of this curve will make its use clearer. It is obtained from the single N-curves of the two transistors by adding the emitter currents of each for successive emitter voltages. Each of the branches is then labeled with the states of the two transistors. For instance, the "on-off" branch of the composite curve represents the emitter voltage-current characteristic when one transistor is "on" and the other is "off." Because of the symmetry involved this really represents two different states, i.e., "on-off" or "off-on."

By choosing a suitable load to be inserted in the position of R_e, an operating point may be set anywhere on this characteristic. For instance, to design a saturating flip-flop, one makes the load a simple resistance, R_e, whose characteristic intersects the N-curve within the "on-off" region. Moreover, it is desirable that the intersection be just to the right of the valley point. This choice will ensure that one transistor is "on" and the other is "off"; that there is little saturation (thus reducing hole storage to a minimum); and that there is no chance for a third stable state (such as both transistors "on"). Notice that if the load were a resistance of too small a magnitude then there would be two intersections on dark portions of the curve (possible stable points), which would imply three possible stable states: "off-on," "on-off," and "on-on." It is also possible to obtain a stable equilibrium point on the composite N-curve in the active-off region. The vertical load line (current generator) shown in Figure 1 is typical of such a load line. Thus a nonsaturating flip-flop might be designed by this method. This, then, indicates how the composite N-curve is used to design the flip-flop for proper steady-state conditions. In addition, several of the possible types of flip-flops to be derived from such a design have been mentioned.

Relative Merits:

Saturating Capacitor-Coupled Type. Now it will be well to consider the relative advantages and disadvantages of the various flip-flops of the two-transistor type. The simple, saturating, capacitor-coupled flip-flop shown in Figure 2 has certain advantages over single-transistor and nonsaturating circuits. First, its stability with regard to noise triggering is enhanced by the hole storage in the "on" transistor. Any noise pulse which is too narrow to last beyond the turnoff time of the saturated transistor will fail to trigger the flip-flop, whereas a nonsaturating flip-flop, or a single-transistor flip-flop in the "off" state, may be triggered by a much narrower noise pulse. Second, the two-transistor flip-flop is symmetric, which means that it may have gates attached to both sides to provide a logical "and" for both states. The single-transistor flip-flop would require gates of different circuitry to achieve this purpose.

The transient characteristics of a capacitor-coupled flip-flop are determined by the responses of the transistors and the size of the capacitors. In general, the bigger the capacitors are made, the more sensitive the flip-flop becomes and the wider the range of pulses that can be used for triggering. However, as the capacitors are enlarged the maximum frequency of operation goes down, so that a compromise must be made between sensitivity and speed. The simplest and most sensitive method for complementing such a flip-flop is to apply negative pulses in the emitter circuit. This is accomplished by including a triggering transformer in series with the emitter load (see Figure 2). A satisfactory set of parameter values is: $R_b = R_e = 1500$ ohms, $R_c = 3900$ ohms, $C = 56$ μμf, and the supply voltage is -30 volts.

Transformer Coupled Type. An improvement may be achieved in triggering sensitivity by coupling the transient with a transformer instead of two capacitors as is customary. This has the added advantage of causing each of the transistors to act like a blocking oscillator during the switching time which speeds the switching transient. This circuit is shown in Figure 3. The advantage of the transformer arises partly from this "autoswitching" effect but also from the fact that the transformer couples the current directly from collector to base and the transistor collector acts very much like a current generator in the switching.

Nonsaturating Type. Finally, the nonsaturating circuit of Figure 4 offers the advantages of speed and sensitivity to narrower triggering pulses. Since there is no saturation of either transistor during operation, there is no delay due to hole storage. This increases the maximum speed with comparable transistors and circuitry by as much as four times and generally about two times. This speed may be a sufficiently important asset to compensate for the concomitant disadvantages. For example, the output levels of nonsaturating circuits are not as consistent as in saturating types unless clamping diodes are added. For example, the output swing may vary by as much as 5 volts in 20 with ordinary variations in the transistors. Moreover, the nonsaturating flip-flop will be more sensitive to narrow noise pulses, just as it is more sensitive to narrow trigger pulses. Such a flip-flop cannot be complemented in the emitter because the impedance of the current generator in the emitter is very large which makes the time constant of the transformer too small to pass a pulse of reasonable width. In this case, triggering may be done with a diode steering circuit (Figure 4). This causes a decrease in voltage sensitivity of the flip-flop, i.e., a higher-amplitude pulse is required for triggering. Finally, the output swing from a nonsaturating circuit is approximately half that from a comparable saturating circuit. Nonetheless, for consistent operation at high speeds this is the best type of circuit that transistors can offer.

Summary. To sum up, the basis of design for the steady-state conditions of the two-transistor flip-flop is the composite N-curve. Various types of coupling circuits may be used

to increase the gain of the loop during the switching transients, capacitor coupling being the commonest and cheapest, transformer coupling offering somewhat more sensitivity to the complement trigger. Finally, the choice between saturating and nonsaturating circuitry is based on the relative importance of speed and circuit simplicity (the nonsaturating flip-flop gives about a two to one advantage in speed).

SINGLE-TRANSISTOR CIRCUITS

The point-contact transistor offers the unique possibility of designing a two-state circuit with but one transistor. The single-transistor circuits with which we have had the most success are the so-called "current" types described by Williams and Chaplin.[1] The basic circuit for such a flip-flop is shown in Figure 5, along with the simple design equations. This circuit takes advantage of the fact that the transistor in its active state acts very much like a current amplifier and consequently can be designed to switch a current between an external diode and itself. This type of circuitry is very tolerant of transistor parameter variation, and indeed, if the parameters are such as to satisfy the equations, the transistor will work invariably. The equations given apply to design of a saturating-type flip-flop, but a nonsaturating circuit may be designed with the aid of additional clamping diodes.

The obvious economy of this circuit in components, power, and cost gives it great possibilities for computer applications. However, its advantages are not without offsetting difficulties. With but one transistor in the circuit, gates can be tied on at only one point. Thus two different gate circuits are needed if they are to be operative for either state of the flip-flop. Moreover, use of a single transistor imposes all the disadvantages of the nonsaturating flip-flop with none of its advantages (unless a nonsaturating single-transistor flip-flop were used). Specifically the flip-flop is very sensitive to narrow noise pulses when in the "off" state, because there is no saturation to overcome. However, its speed is no better than that of the other saturating types, because hole storage in the "on" state slows up the transient enough to require large coupling condensers (or transformers) which in turn limit the maximum trigger rate. Figure 5, the basic circuit, does not show any provision for complement triggering. In general, the margins on pulse width and amplitude required for successful complementing are not as good in a single-transistor flip-flop as in a two-transistor flip-flop. Nonetheless, with a simple capacitor-coupled steering circuit given by Williams[1] such a flip-flop has been triggered over a range of five to one in both pulse amplitude and pulse width.

1. Williams, F. C. and Chaplin, G. B. B., "A Method of Designing Transistor Trigger Circuits," Proc. I.E.E., vol. 100, No. 66, Part III, pp. 228-248, July 1953.

JUNCTION FLIP-FLOPS

When I originally undertook to present this paper on high-speed flip-flops, the junction transistors then available did not warrant consideration for such circuitry. However, since then the development in both germanium and silicon junctions has been such that junction flip-flops may be considered for medium-speed applications. I intend, therefore, to describe some of their salient features and capabilities.

The junction flip-flop requires at least two transistors. The proper gain and phase inversion, required for two stable states, is obtained by cross-coupling two grounded-emitter amplifiers. Thus, the basic circuit is similar to the corresponding vacuum-tube circuit. Adding capacitors across the coupling resistors or adding a coupling transformer will serve to increase the loop gain of the circuit during the switching transient. The characteristics of these two types of coupling are similar to those found in point-contact circuits using the same techniques.

Junction flip-flops are invariably operated nonsaturating because of the tremendous hole-storage sensitivity of this type of transistor. Clamping may or may not be provided to standardize output levels, but the same problems of level variation are present as were found with the point-contact nonsaturating circuits. In general, the fastest of the junctions (among lower priced units) are the silicon n-p-n's which have recently appeared on the market. Following the silicons in order of speed are the grown n-p-n's and the diffused p-n-p's. Because some feeling has existed that there was little promise in point-contact work, there has been great incentive to make high-speed flip-flops with junction transistors. Efforts in this direction have led to circuits similar to vacuum-tube flip-flops which employ cathode followers for cross-coupling. These four-transistor circuits gain about two to one in speed over the two-transistor counterpart. The junction flip-flops may run anywhere from a third to a tenth as fast as the point-contact types. The output swings available from junctions are as great as those from the point-contacts, and the power available is as great or greater. The triggering requirements are similar to those found in point-contact types.

CAPABILITIES OF VARIOUS TYPES OF FLIP-FLOPS

In order to present a better idea of the general field of flip-flop performance, I have refrained from giving any quantitative evaluations of the various types up to this point. Now let us consider the actual scope of speeds, output swings, and triggering ranges available.

Speed Limits:

All the saturating types of flip-flops are limited to maximum speeds around 1 megacycle. This applies to well designed circuits employing transistor types which have low hole-storage coefficients. Experience has shown that reach-

ing 1-mc operation requires some selection from production samples of transistors: about 80% of the transistors are acceptable. For computer work or other large systems, circuitry of this type may be relied on to operate at basic maximum rates of 200 to 500 kilocycles. The waveforms in Figures 2 and 3 show operation at 500 kilocycles. Nonsaturating circuits using the same transistors will approximately double these limits; they may go even faster, but the waveform begins to deteriorate radically when the pulse-repetition period becomes of the order of the rise and fall times. The waveform shown in Figure 4 was taken at a pulse-repetition frequency of 3.5 megacycles. However, this was with very high-frequency transistors not now commercially available. Junction flip-flops using p-n-p transistors will operate up to 200 kilocycles with the lower-priced models available from some manufacturers. Use of n-p-n transistors extends this limit to about 300 kilocycles, while silicon n-p-n's will push this speed to 450 kilocycles. With a four-transistor flip-flop using silicon-junction transistors, operation can be obtained at rates as high as 1 megacycle.

Trigger Limits:

All of these circuits trigger with pulses in the range of 2 to 30 volts. Generally speaking, circuits which employ steering-circuit triggering are less sensitive but less critical. For instance, with steering diodes a pulse of 15 to 30 volts will trigger the flip-flop at all pulse widths from 0.1 to 2 microseconds while triggering in the emitter with a transformer may be accomplished with pulses from 5 to 20 volts in a range from 0.5 to 1.5 microseconds.

As for the pulse width required, pulses which are too broad or too narrow will fail to trigger any given flip-flop. The lower limit is usually of more concern, because slightly higher speeds may be achieved with narrower pulses. Nonsaturating circuits are best with respect to this criterion; they will trigger easily on a 0.1-μsec, 0.5-sine-wave pulse. Most other circuits will not trigger at all on such narrow pulses or else require excessive amplitude. The one exception to this rule is the transformer-coupled saturating type which will trigger on 0.1-μsec pulses and is somewhat more sensitive than the capacitor-coupled nonsaturating circuit. The remainder of the saturating circuits require pulse widths in excess of 0.2 microsecond. The upper limit of pulse widths which will trigger a flip-flop depends largely on the storage elements involved in the feedback circuits. Since these elements also affect the speed of the flip-flop there must be some compromise between speed and pulse standardization. Finally, junction transistor flip-flops require pulse widths from 0.2 to 1.0 microsecond. Generally they are subject to the same conditions as have been described for the point contacts but require slightly wider pulses for the same sensitivity.

Output Available:

The transistor is essentially a low-power device and as such is more subject to noise interference than vacuum-tube circuitry. In order to rise as far above the noise level as possible, circuits are designed for maximum swings. The swing is limited by the "off" power dissipation in point-contact units and by the reverse breakdown voltage for junction types. These factors limit swings to less than 30 volts in all cases encountered; a more practical value for final design has been found to be about 20 volts. The rise time of the flip-flops is invariably shorter than the fall time, and the fall time may vary from 0.1 microsecond to several microseconds for the slower circuits and transistors. It might be noted that very often, even though high repetition rates will not be encountered in a particular application, it is required that the flip-flop waveform achieve its final value in a short time. This means use of one of the high-speed circuits.

GATES

Before proceeding to the description of a typical application of these flip-flops, it will be well to describe briefly the characteristics of the gates to be used in the system. I have previously explained that the computer involved employs pulse-level gates. In high-speed application, such gates require the following characteristics: they must operate fast; they must isolate the input and output from each other; they must not cause heavy loading on either the pulse source or level source; and they must amplify or regenerate the input pulse. Gates of this description must employ an asymmetric active device, and we have found the transistor ideal in that application. Our present circuit is simple, and as many as ten gates can be driven from one flip-flop. Moreover, the gate will operate as fast as the flip-flop "sets up." (Further details are beyond the scope of this paper.)

APPLICATION FOR STUDY

In order to gain insight into the problems involved in the use of transistor circuitry, a small system modeled after an existing section of a vacuum-tube computer was designed and built. The "angular-position counter" and checking circuit (Figure 6) employ 48 transistors and are designed to provide a tally of positions on the surface of a magnetic-drum memory. They also serve to synchronize the drum with the rest of the computer operation and thus provide a means of reading into, and out of, proper positions on the drum. The basic rate of the counter is 100 kilocycles, at which speed the transistors have little difficulty in performing their jobs. The only use that has been made of junction transistors in this setup is in a pulse amplifier.

This amplifier supplies a 20-v pulse to a 200-ohm impedance. There are 11 two-transistor flip-flops in the counter itself, 2 two-transistor flip-flops in the checking circuit, and 1 single-transistor flip-flop in the checking circuit.

This system has been operative for some time, and is revealing to us some of the problems and joys of transistor circuits. The comparative power of the transistor circuit is minuscule: 4 watts as compared with 240 watts for the vacuum-tube system. The size reduction is also impressive. Although the reduction has not yet been carried to its practical limit, the transistor system is about one-tenth of the area of the vacuum-tube system. The cost of constructing computer systems is very little dependent on the actual price of transistors versus tubes, so that the transistor circuits are in the same price class as tube circuits even now.

Now, for some of the gloomy parts of the picture. Since transistors are small-power devices, power-line noise has become a problem; supplies will require better filtering at high frequencies. Supplying low voltages at relatively high currents and good efficiencies is a problem which is yet to be solved. Finally, the old question of reliability comes up. Generally, the tendency is to blame the device for the failings of the engineer, the major weakness being in the circuitry and associated equipment rather than the transistor. At the time we built this counter the point-contact transistors received were considered relatively good and quite reliable devices. Indeed, one small accumulator incorporating early-model transistors has operated at Lincoln Laboratory for 13,000 hours with only one outright failure. Nonetheless, adverse reports on the economics, and reliability of point-contact units, have encouraged many manufacturers to leave the field. Our experience with junction transistors shows that they too have had their difficulties, but these are being eliminated with great rapidity. At present some manufacturers are quoting reliability figures for transistors, both point-contact and junction, which are comparable to those usually given for "reliable" tubes.

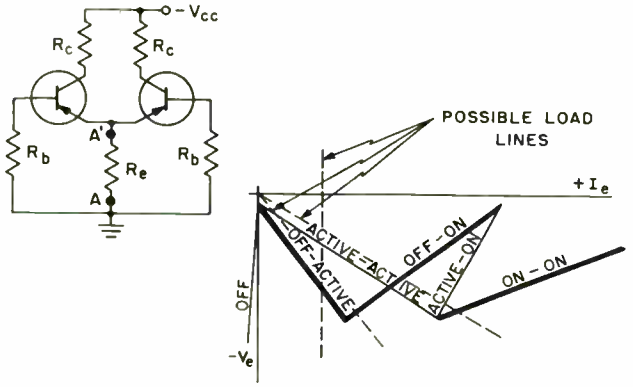


Fig. 1
Basic flip-flop and common emitter characteristic.

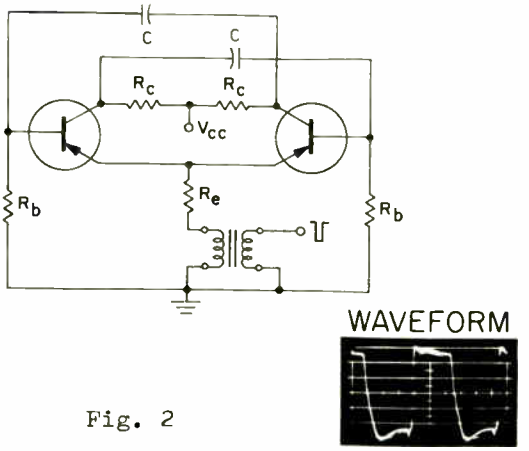


Fig. 2
Capacitor-coupled flip-flop.

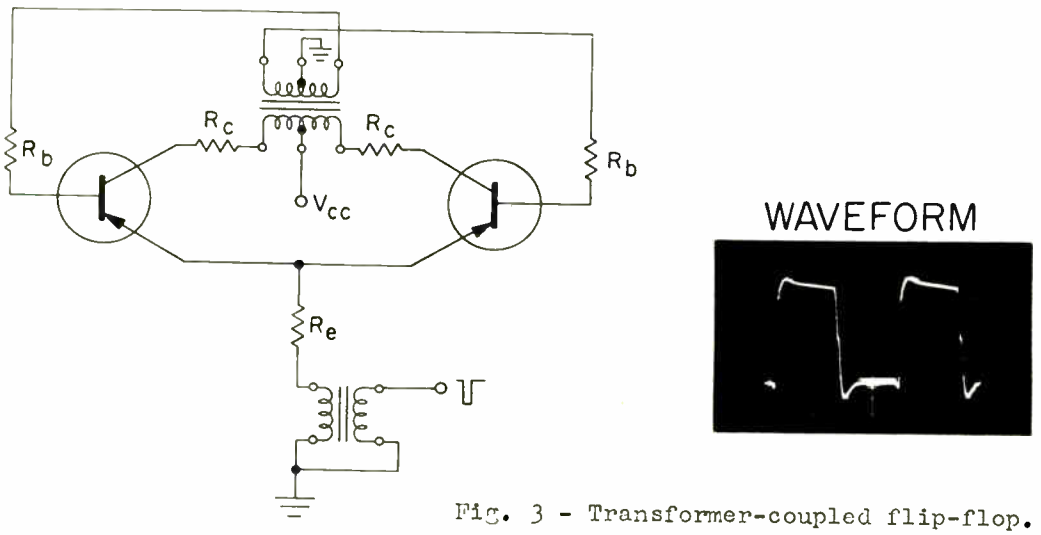
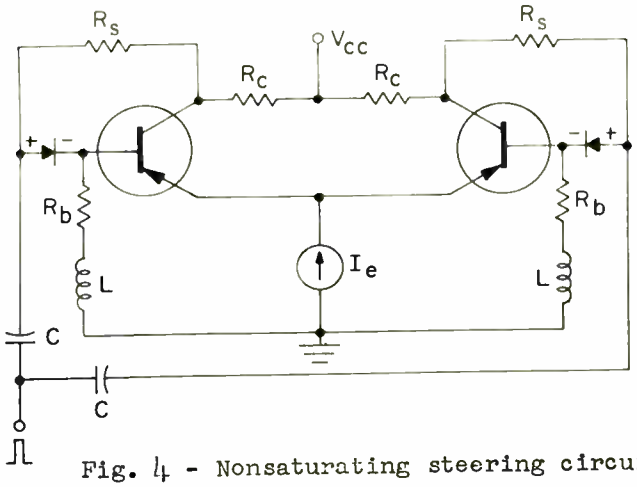


Fig. 3 - Transformer-coupled flip-flop.



WAVEFORM

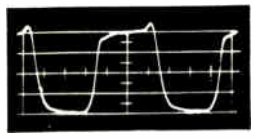
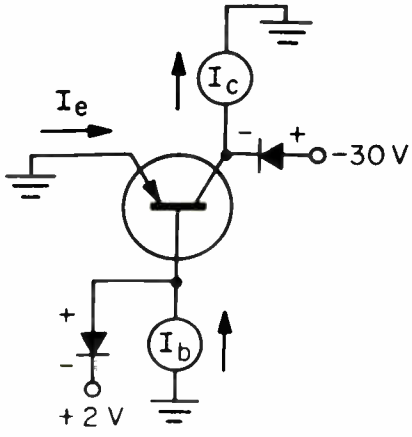


Fig. 4 - Nonsaturating steering circuit-coupled flip-flop.



$$I_e = I_c - I_b$$

TO INSURE A SATURATED STATE:

$$\alpha I_e \geq I_c$$

Fig. 5 - Basic single-transistor flip-flop.

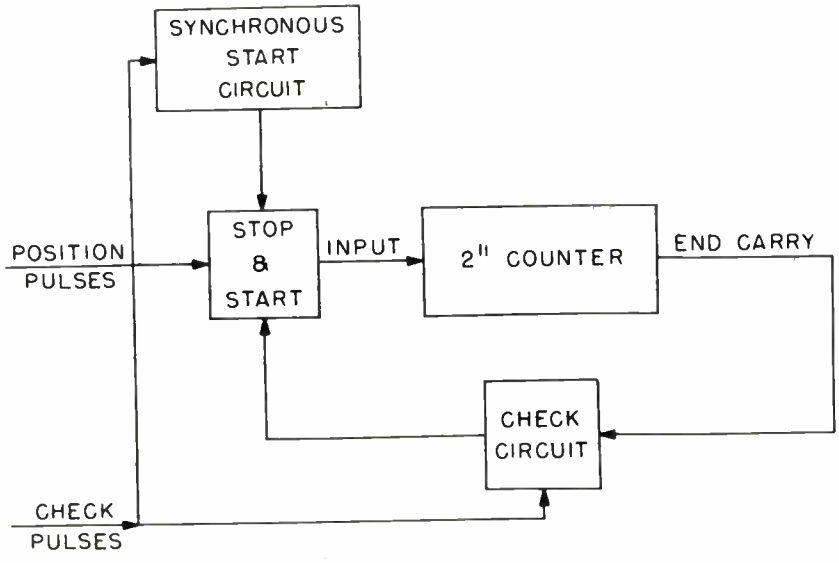


Fig. 6 - Drum-position detector.

DESIGN FUNDAMENTALS OF PHOTOGRAPHIC DATA STORAGE

Gerhard L. Hollander
Clevite-Brush Development Company
Cleveland 8, Ohio

Since densities up to 10^6 cells per square inch are practical with photographic data-storage media, they should be used more widely for certain computer and recording purposes. This paper is designed to give in one place sufficient background in the fundamentals of photography to permit engineers to evaluate film as a storage medium. The exposure can be determined by simple graphical design instead of experimentation by use of curves given in the paper. The main shortcoming of photographic storage is the lack of certain data which the film manufacturers should supply.

Introduction

Photographic materials have not taken their rightful place among the available storage media. Many applications, such as function tables for computers and recorders for test data, could take advantage of the dense storage potential and non-volatility of photographic media when their non-erasability is acceptable. Practical design goals are densities of 10^5 storage locations per square inch for film and 10^6 storage locations per square inch for plates.

Even more information can be stored if we take advantage of several density levels and several colors in the same cell (storage location). At least three colors and as many as ten density levels could be employed. By allowing ten different combinations of colors and density levels, each cell can represent a decimal digit instead of the usual binary digit. This increases the practical storage density of photographic materials by another factor of over three and makes it ideal for equipment operating in decimal notation.

From a designer's point of view one of the chief shortcomings of the photographic storage media is the lack of enough quantitative data and curves to enable him to do most of his design on paper. In contrast to magnetic media only the barest information is available for photographic storage.

When evaluating various photographic materials, the designer's first questions are:

1. How many storage cells can be reliably placed in a unit area?
2. How bright must the available light source be?
3. How long must the film be exposed?
4. How much density contrast is available after developing?

Many of these questions cannot be answered readily with the characteristics that are published by the manufacturers of photographic materials. This is especially disconcerting to an electrical engineer, because procedures similar to vacuum-tube-circuit designs should be possible.

A typical application for which photographic data storage had been investigated was a digital data-recorder.[1] A large mass of information had to be stored in minimum space. Here the volume of the entire recording equipment had to be minimized, not only the space occupied but the storage medium itself. Information had to be recorded at a high rate although the readout speed and readout complexity were secondary considerations.

For the digital data-recorder, the first question of the permissible storage density would determine how much storage medium was required to store the large mass of information. The second question on the brightness of the light source would determine how large the light source must be. Required exposure time would determine if the light sources could be time-shared between various tracks or if several light sources were needed to expose each storage location long enough.

In other applications, such as permanent function tables for computers, the second and third questions are not as important, because the time for exposing the film and the space for the light source are only secondary considerations. However, even here the designer would like to know how long he must expose the film without going through a lengthy cut-and-try procedure.

With so many potential applications for photographic media, it is surprising that significant papers from only two groups have come to the author's attention. Publications by A. Tyler and R. D. O'Neal of the Eastman Kodak Company indicate that they consider as practical, storage densities of 10^5 cells per square inch for film and 10^6 cells per square inch for plates.[2,3] King, Brown, and Ridenour have investigated methods for increasing the ability to select a particular cell, thereby increasing the effective resolution of the photographic materials as storage medium.[4]

The purpose of this paper is to outline a design procedure that can be used with film and to propose the characteristic curves that are needed for such procedure. This requires a brief

review of the properties of photographic materials and unique and universally adopted definitions for such terms as "sensitivity".

Deviations of the characteristics from the published curves will be examined so that the design problems can be anticipated.

Resolution

Two common usages of the term "resolution" should be carefully distinguished. The photographer defines resolution of a photographic medium as the closest number of lines per mm that can be distinguished as separated in a photographic image. A denser array of lines would appear as an indistinct gray mass.[5] This resolution is primarily a function of the grain structure of the photographic emulsion, but cannot be used as the permissible resolution in a computer application. For example, the eye auto-correlates even when some of the lines are broken. Today some emulsions have such high resolution that no available lens has enough resolving power to test them.[6]

For computers and recording, a definite meaning is assigned to each storage cell. This requires that:

1. The particular cell can be identified as either predominantly exposed or predominantly unexposed, without reference to any adjacent cell.
2. The cell can be found and uniquely identified during playback.

Furthermore, specks of dust or film irregularities should not cover too many storage cells. For digital applications the resolution is normally limited more by the ability to select the storage location than by the emulsion of the film. The work by King et al[4] treats this problem.

Characteristic Curves

Figure 1 contains a set of characteristic curves that are supplied by the manufacturer of photographic materials.[7] The abscissa is plotted as the logarithm of exposure where:

$$\text{exposure} = \frac{\text{candle power} \times \text{exposure time}}{(\text{source distance in m})^2} \qquad (1)$$

The ordinate is density, which is defined for processed film as:

$$\text{density} = \frac{\text{incident light}}{\text{transmitted light}} \qquad (2)$$

If the desired density is known the designer now expects to be able to answer Questions 1 and 2 of the Introduction, how bright the light source must be and how long the film must be exposed, because these two terms determine the exposure per Equation 1. However, things are not that simple. These curves have been plotted for an exposure for a 3000°K tungsten light. They hold only if the actual exposure time and the light source are identical to those used in the preparation of the curves.

The five major reasons for deviations from these characteristic curves are:

1. Variation of characteristics with the spectrum of the light source.
2. Failure of the reciprocity law.
3. Environmental conditions.
4. Non-uniformity of photographic material.
5. Intermittency effect.

Spectrum of Light Source

The manufacturer supplies curves like those in Figure 2 to show the variation of the film sensitivity with the wavelengths of the light source. These curves are at best a qualitative relation. First of all, the ordinates are plotted as sensitivity, which does not give sufficient information about the entire film characteristics for various exposures and densities. Secondly, most practical light sources are not monochromatic but contain several frequencies as shown in Figure 3 for example.

In order to determine the exposure time for a light source for which the radiance spectrum is given, the manufacturer should supply families of spectral sensitivity curves as shown in Figure 4. By an extension of Van Kreveld's summation law, derived in Appendix A, exposure time "t" is related to the exposure "E" and the intensity "I" by:

$$\frac{1}{t} = \int \frac{I}{E}\, d\lambda \qquad (3)$$

The exposure time can be determined easily from Figures 3 and 4 by graphical evaluation of the product integral in Equation 3. This process is not difficult since straight line approximations can be made. While the integral implies integration from zero to infinity, only the portion near the visible spectrum needs to be investigated. Also, the spectra for the light-source intensity and the film sensitivity cut off very sharply so that we need to investigate only the range where both have a significant value.

Failure of the Reciprocity Law

The definition of the term "exposure" in Equation 1 is based on the Bunsen-Roscoe reciprocity law of photographic material, that the density is only a function of the product of light intensity and exposure time, regardless of their individual values. This law holds only as a first approximation. For more precise applications or for extremely short or long exposure times, the deviations from the reciprocity law must be taken into account.

Figure 5 shows a typical curve of the reciprocity law failure.[8] To obtain a constant density, the exposure must be increased when the intensity becomes very small or very large. If the reciprocity law were valid, the constant density curve should be a straight horizontal line as shown dotted in Figure 5. Normally, the

characteristic curves supplied by the manufacturer are plotted for the optimal intensity I_o at which the required exposure for a given density is minimum.

Since Figure 4 is plotted against a function of exposure, the reciprocity-law failure is not taken into account. While some authors have proposed empirical relations that approximate the failure of the reciprocity law, these approximations do not apply to the extremely short exposure times used in many digital data storage applications. Therefore, several sets of spectral sensitivity curves, like those in Figure 4, for different exposure times are preferable. This does not imply an infinite number of curves, because exposure-time steps of two or three decades are usually sufficient. Thus, we would probably have two or three sets of these curves for practical engineering design work.

Other Effects

The environmental conditions, the nonuniformity of the photographic material, and the intermittency effect are normally of lesser importance to the designer of photographic data-storage devices. The effect of the first two deviations are described by their name. The intermittency effect takes into account that film is not a perfect integrator when a spot is exposed repeatedly to brief flashes of light. The resultant density may be more or less than that produced by a steady application of the light source for an equal time. This intermittency effect does not affect data storage applications, because a single light flash is normally used.

Lastly, we must remember that any characteristics supplied by manufacturers apply only to the average of their production runs, just as in vacuum tubes a band of tolerances must be considered around each characteristic curve. Every effort should be made to have the supplier of photographic material state the tolerances on his characteristics, just as the tube manufacturer does for his product.

Film Imperfections

Manufacturers of photographic film should publish more information concerning film imperfections as is done by high-quality-tape manufacturers. According to Eastman Kodak scientists, at a storage density of 100 lines per millimeter bad spots could lose as many as 10 to 20 cells, but no value for the frequency of these blemishes is available. Of course, it is much harder to test film for imperfections than to do the same thing for magnetic tape, because film is not erasable and imperfections could be introduced during the processing. In general, films from production runs show fewer blemishes than identical films from special laboratory runs. Dr. Tyler of Eastman Kodak reports that film blemishes large enough to obliterate a spot of 0.01 inch by 0.02 inch occur less than once for 10^8 cells.[9]

It would be nice if a method could be found whereby film imperfections could be detected before exposure, so that bad sections would not be depended upon for critical recording. If this is impossible, then the manufacturing processes should at least be improved to the point that the probability of blemishes is low, even when a dense array of stored information is used. With present techniques, error-checking and error-correcting codes appear to be the best solution. It is also advisable to interlace several track groups so that an occasional large blemish does not destroy the error-checking feature by obliterating several digits in the same word.

Light Sources

For the recording of digital data, the light sources must be bright, modulated at relatively high frequencies, and have a small spot size. When the overall dimensions of a recording device are also critical, the light source must be small. Arcs from a carbon lamp and cathode-ray beams have been used in digital storage applications.

Particularly interesting are small neon tubes capable of being intensity modulated at a high rate. Experimental bulbs of 0.05-inch diameter have been developed with a built-in lens at the tip and a top frequency between 20 and 35 kc.[10,11] However, the final production model of this bulb, designed by the Westinghouse Electric Company, has been changed so that the light emerges along the 1-inch length of the bulb. The recording characteristics of these tubes could probably be improved if xenon instead of neon were used as a gas.

Even with these bulbs we must still solve the problem of arraying them so that the maximum practical storage density on the film can be achieved. It has been suggested to use arrays of these bulbs from which the light could be reduced by optical means to the allowable spot diameter on the film. Selection of one bulb in such an array will be no more difficult than core selection in a static magnetic memory.

Summary

Some writers feel that densities of 10^6 cells per square inch can be achieved practically with photographic data-storage devices. This makes photographic materials desirable storage media where:

1. Dense storage is needed.
2. No erasures are required.
3. The delay of developing can be tolerated.

So that an engineer can systematically evaluate photographic materials for a specific application and can design the equipment, he should have:

1. A spectral distribution curve of his light source similar to Figure 3.

2. Spectral sensitivity curves for the photographic material at the approximate contemplated exposure time similar to those shown in Figure 4.

3. Tolerance bands on the film characteristics.

The last two items should be supplied by the manufacturer of photographic materials. The first is generally available for light sources that are commonly used.

The exposure time "t", the exposure "E", and the light intensity "I" are related by:

$$\frac{1}{t} = \int \frac{I}{E} d\lambda \qquad (3)$$

The product integral can be graphically evaluated from Figures 3 and 4 with straight line approximations.

Acknowledgment

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Appendix A

Extension of Van Kreveld's Law for a Continuous Spectrum

In order to determine from Figure 3 and Figure 4 the exposure time required to obtain a certain density on the photographic medium for a given light source, we must know how the densities due to different wavelengths add in the film. Van Kreveld[12] showed heuristically and proved experimentally that if an exposure "E_1" of a given wavelength is needed to produce a certain density "S" in the film, simultaneous application of two or three wavelengths reduces the required exposure E_T for the same density by:

$$\frac{a_1}{E_1} + \frac{a_2}{E_2} + \cdots = \Sigma \frac{a_i}{E_i} = \frac{1}{E_T} \qquad (4)$$

where "a_i" is the fraction of each frequency. Since we often deal with a continuous light spectrum, not in individual wavelengths, van Kreveld's summation law must be extended.

The total exposure E_T is a product of the exposure time "t" and the total intensity "I".

$$E_T = t \int I \, d\lambda \qquad (5)$$

where the intensity is the resultant intensity of all wavelengths together. By substituting Equation 5 into Equation 4 and expressing the left-hand side for a continuous spectrum we get:

$$\frac{1}{\int I d\lambda} \int \frac{I}{E} d\lambda = \frac{1}{t \int I d\lambda} \qquad (6)$$

This may be simplified to get the expression for the required exposure time:

$$\frac{1}{t} = \int \frac{I}{E} d\lambda \qquad (3)$$

References

1. G. L. Hollander, "A Digital Data-Recorder for Dense Storage of Continuous Voltages," A.I.E.E. Transactions, vol. 73, part 1, pp. 253-259; July 1954.

2. R. D. O'Neal, Photographic Methods for Handling Input and Output Data, Symposium on Large-Scale Digital Calculating Machinery, Harvard University Press, Cambridge, Mass., pp. 260-266; 1948.

3. A. W. Tyler, "Recording Techniques for Digital Coded Data," "Review of Input and Output Equipment," American Institute of Electrical Engineers, New York, pp. 3-7; March 1953.

4. G. W. King, G. W. Brown, and L. N. Ridenour, "Photographic Techniques for Information Storage," Proc. I.R.E., vol. 41, pp. 1421-1428; October 1953.

5. Eastman Kodak Co., Kodak Films, 5th ed., Eastman Kodak Co., Rochester, N.Y., p. 13; 1951.

6. Reference 3, p. 5

7. Eastman Kodak Co., Kodak Linograph Papers and Films for Instrument Recording, Eastman Kodak Co., Rochester, N.Y., p. 3; 1952.

8. W. E. Forsythe, Measurement of Radiant Energy, McGraw-Hill Book Co., New York, N.Y., p. 258; 1937.

9. Reference 3, p. 6.

10. G. P. Wilson and N. R. Gunderson, "Progress Report in Miniaturization of Neon Tubes for Digital Recorders," Techn. Memo. 562, U. S. Naval Ordnance Test Station, Inyokern, Calif.; 1951.

11. N. R. Gunderson, "Miniaturization of Neon Tubes for Digital Recorders," Techn. Memo. 1262, U. S. Naval Ordnance Test Station, Inyokern, Calif.; 1953.

12. A. van Kreveld, "Ein Gesetz für die Schwärzungskurven bei Mischfarben," Zeitschrift für wissenschaftliche Photographie, vol. 32, pp. 222-230; January 1934.

13. G. L. Hollander, "Digital Data Recorder - An Investigation of Dense Storage of Information," Techn. Memo. 6897-TM-12, M.I.T.

Servomechanisms Laboratory, Cambridge, Mass., pp. 110-133; 1953.

14. A. C. Hardy and F. H. Perrin, The Principles of Optics, 1st ed., McGraw-Hill Book Co., New York, N.Y.; 1932.

15. G. L. Hollander, "Bibliography on Data Storage and Recording," A.I.E.E. Transactions, vol. 73, part 1, pp. 49-58; March 1954.

16. C. E. K. Mees, The Theory of the Photographic Process, The Macmillian Company, New York, N.Y.; 1942.

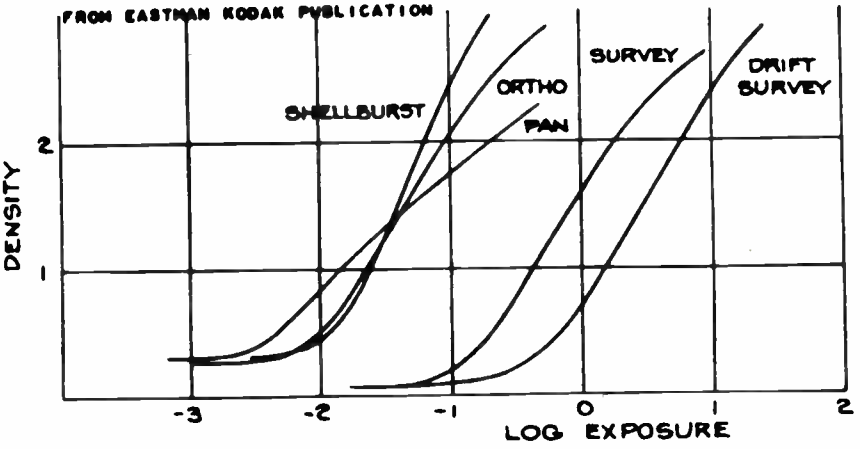

Fig. 1 - Characteristics of some Eastman Kodak films.

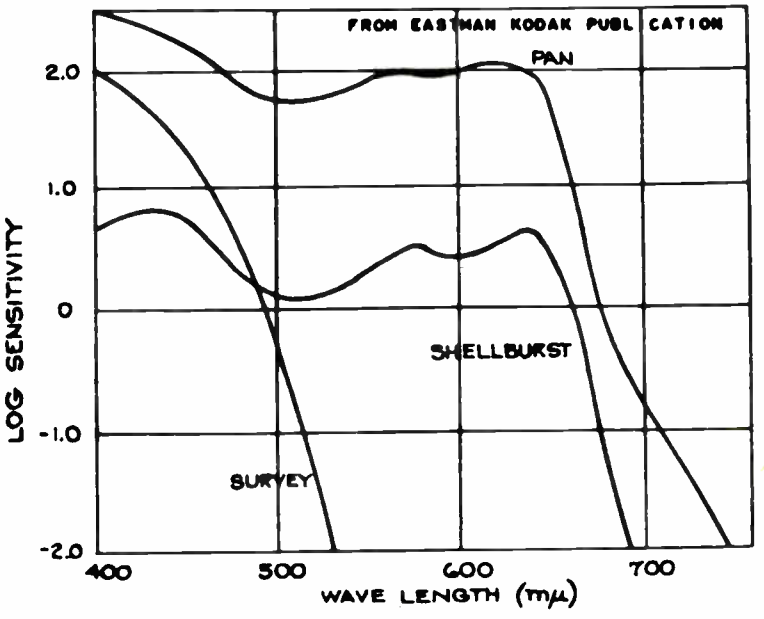

Fig. 2 - Response spectra of Kodak films.

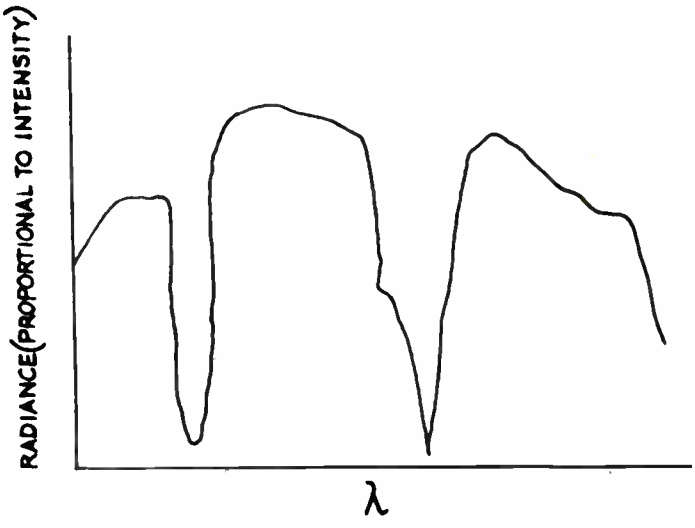

Fig. 3 - Possible light source spectrum.

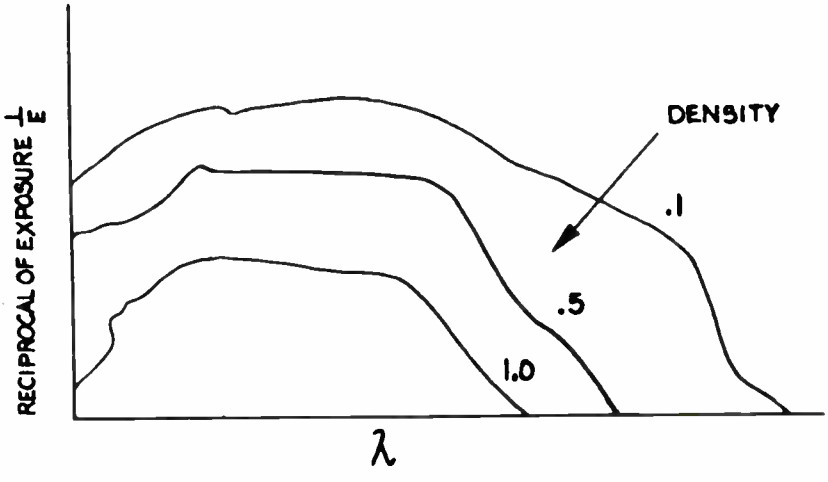

Fig. 4 - Possible spectral sensitivity curves for different density values.

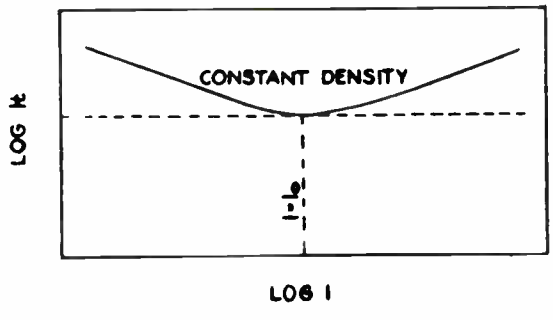

Fig. 5 - Typical curves of reciprocity-law failure.

PULSE RESPONSES OF FERRITE MEMORY CORES*

James Robert Freeman**
Massachusetts Institute of Technology
Lexington, Massachusetts

Summary. The responses of magnetic-ferrite cores to current pulses such as used in a two-to-one selection coincident-current magnetic memory are classified as fourteen basic voltage outputs. These outputs are defined and described with relation to the hysteresis loops and pulse sequences involved. Photographs of the pulse responses are presented and certain distinctive differences compared. The concept of reversible and irreversible outputs is explained. Curves of the various core voltage outputs, and the switching and peaking times versus the driving current are presented for the General Ceramics' body Ferramic S-1, size F-394. Analytical expressions for the peak full-selected ONE and the switching time are given. The convergence ratio is defined and an example of its use in the evaluation of memory cores is given. The effect of disturb sensitivity caused by overdriving is illustrated.

Introduction

The development of magnetic-ferrite cores with rectangular hysteresis loops and short switching times has made the high-speed arbitrary-access magnetic-memory possible. The M.I.T. coincident-current memories utilize the permanent magnetic properties of ferrite cores to store binary information, and the nonlinear properties to descriminate between full-amplitude selecting pulses and half-amplitude pulses. Cores are assembled in square matrices called memory planes with selection wires passing through each row and column. Figure 1. A core is addressed by passing half-amplitude pulses of current down both the particular row and the column of the core selected. In this way the selected core receives a net full-amplitude pulse; all other cores on the same row or column as the selected core receive half-amplitude current pulses. These cores are said to be half-selected. The cores which are neither half-selected, nor are the selected core, are called unselected cores.

Memory Plane Pulse Sequences

The binary information, ONE or ZERO, stored in a toroidal memory core is determined by the polarity of its remnant magnetization. See Figure 2. The information is extracted when the core is selected by a full-amplitude READ current-pulse. The READ pulse polarity is such that the magnetization is reversed when the core holds a ONE. The cores are relatively insensitive to half-amplitude pulses. A sense winding passes through all cores in a plane. Figure 1. A ONE is "read" by detecting the voltage that is induced in the sense winding by the reversal of the selected core's magnetization when a READ pulse is applied. The absence of such a voltage indicates no reversal and consequently a ZERO in the selected core.

When selecting a core, a READ pulse followed by a WRITE pulse of opposite polarity is used. Figure 2. The WRITE pulse will leave a ONE in the selected core. If it is desired to leave a ZERO in the selected core, an inhibiting half-READ pulse is supplied simultaneously with the WRITE pulse resulting in a net half-WRITE pulse. Therefore a ZERO is written into a core by pulsing it with a full-READ followed by a half-WRITE pulse. The inhibiting half-READ pulse is supplied by the inhibit winding which links all cores in the memory plane. See Figure 1.

On the basis of the mode of operation described above, Table I presents the various possible pulse sequences to which a core in a memory may be subjected. Theoretically, a core may be selected, half-selected, and unselected in any order. A study of Table I from this point of view will indicate the possible sequences of pulses a core may experience.

Core Voltage Outputs

As previously explained, the outputs of cores are sensed at the time of application of the READ pulses. Because this is so, the voltage responses to READ polarity pulses are the ones of interest.

Many distinct voltage outputs are possible, but basically only fourteen kinds exist.† Table II lists these outputs by name and symbol, and indicates the simplest series of pulses which will produce them. The last pulse of each sequence is the selecting pulse.

The output of a core depends on its magnetic state and whether it receives a full- or half-amplitude selecting pulse. The magnetic state is determined by the information (i.e. ONE or

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** Staff Member, Lincoln Laboratory, Massachusetts Institute of Technology.

† The use of very short duration driving pulses, overdriving cores, disturb sensitivity, and other such conditions give rise to output variations which are less basic in nature. All such observed outputs may be classified as special cases of the basic fourteen outputs.

ZERO) and by the sequence of half-amplitude pulses that have preceded the selecting pulse in question. Half-amplitude pulses either leave the magnetic state of a core undisturbed or slightly modified. A core in one of the modified magnetic states is said to be a disturbed core; and a half-amplitude pulse that modifies the magnetic state is said to be a disturbing pulse. The disturbed states are referred to as write-disturbed or read-disturbed depending on whether the last disturbing pulse preceding the selecting pulse was a half-amplitude WRITE or a half-amplitude READ, respectively.

Figure 3 shows the remnant magnetic states from which the fourteen basic pulsed voltage outputs are obtained, together with the magnetic hysteresis loops that memory cores operate on in a two-to-one selection system. In Figure 3, the remant magnetic states are identified by the subscripts of the symbols used to designate the corresponding full-selected voltage outputs obtained from those states.

Voltage Outputs From Reversible Magnetization Changes

Figure 3 shows ten states of remnant magnetization which occur in two-to-one selection of magnetic cores. By tracing the various hysteresis loops involved, it is seen that the remnant magnetizations of cores in the rl, rz, or uz states are not changed by the application of half-amplitude READ pulses and even full-amplitude READ pulses do not affect the uz state. The output voltages that occur under these conditions are the result of reversible magnetization changes. Such reversible outputs are spikes of voltage which for any practical consideration are linear functions of the time derivative of the driving current pulse. That is to say, that in the case of reversible outputs, a core responds essentially as a linear inductance. Therefore, a reversible output from a core may be expressed mathematically as

$$V_r = M \frac{dI_m}{dt} \qquad (1)$$

where V_r is the reversible voltage of the core output,
I_m the current of the driving pulse,
t the time,
and M the mutual inductance between the drive wires and the sense winding.

The mutual inductance, M, depends on the core dimensions, the winding geometry, and the differential permeability of the particular assymmetrical minor hysteresis loop traversed. The voltage outputs reported in this paper are the responses from General Ceramics' Ferramic S-1 memory cores, size F394, with single turn sense windings wound tightly about the core cross sections and leads twisted to eliminate air pick-up. The drive wire is oriented axially through the cores.

Outputs from the Undisturbed ZERO State (uVz, uVhz)

A study of the possible pulse sequences as indicated by Table I shows that full-amplitude READ pulses are always followed by WRITE polarity pulses. For this reason, neither the undisturbed ZERO nor the half-selected undisturbed ZERO outputs can ever occur in the memory. However, because of the basic nature of uVz and uVhz they are included for the sake of completeness.

The undisturbed ZERO, uVz, and the half-selected undisturbed ZERO, uVhz, are the most rudimentary pulse responses that can be obtained from a magnetic core. Since they are reversible they have the shape of the time derivative of the driving current pulse. Figure 4 shows a composite photograph of a full-amplitude READ current pulse and the resulting uVz output. The shape of the output is seen to be that of the time derivative of the driving pulse.

Figures 5 and 12 include photographs of the uVhz and uVz outputs, respectively. The only difference between the two outputs is in their amplitudes. The relative amplitudes depend on the rate of rise of the respective driving currents, therefore, with the same rise time, the uVz amplitude should be essentially twice that of the uVhz. However, due to slight differences in the differential permeabilities of their respective hysteresis loops, the uVhz is found to be somewhat greater than half the uVz.

Half-Selected Read-Disturbed Outputs (rVhl, rVhz)

As previously explained, the undisturbed ZERO outputs are never obtained in the coincident-current magnetic-memory. The half-selected read-disturbed outputs, rVhl and rVhz, however, are of prime importance in the memory. rVhl and rVhz are reversible and therefore have the same shapes as the uVz and uVhz outputs. Figures 5 and 6 are photographic comparisons of the various half-selected ZERO and half-selected ONE outputs, respectively. With a particular drive current the relative amplitudes of reversible outputs depend only on the differential permeabilities of their respective assymmetrical minor loops. The differential permeabilities of these loops are greater for smaller magnetization, being maximum for the loop at zero remnant magnetization, and least for the loop at saturation. Understanding this fact and referring to the relative values of magnetization represented by the rl, rz, and uz states, it is clear that

$$r^V_{hl} > r^V_{hz} > u^V_{hz} \qquad (2)$$

Equation 2 is substantiated by the curves in Figure 7.

Figure 7 shows the reversible half-selected outputs to be relatively insensitive to the amplitude of the driving current. This fact is due to the compensating effects of two factors governing the amplitudes of reversible outputs. For a

given rise time, the reversible output of a core is directly proportional to the amplitude of the driving pulse. However, the magnitude of the magnetization of the remnant state also depends on the amplitude of the driving pulses. At low driving currents the remnant magnetization is low and therefore the differential permeability is larger. These compensating effects make the various reversible outputs nearly insensitive to driving current variations.

Voltage Outputs from Irreversible Magnetization Changes

Figure 3 indicates that the voltage outputs obtained with half-amplitude READ polarity pulses from cores in the ul, wl, dz, and wz states are irreversible because the remnant magnetization is changed by the driving pulse; also, all full-selected outputs except the uVz are irreversible. Irreversible outputs retain the reversible "spike" of voltage caused by the rise of the drive current pulse, but in addition produce a voltage caused by the change of magnetic flux which results from irreversible domain wall growth. The superposition of these two voltages is the total output. The irreversible wall motion essentially begins instantaneously when the necessary driving force is applied. The duration of the motion depends on the relaxation time and the total flux change involved. The relaxation time is longer when a core is being demagnetized than when the magnetization is being increased by the driving pulse. With a step function drive the irreversible voltage response begins from an initial value and ultimately decays assymptotically to zero. For full-amplitude pulses, and for half-amplitude pulses at high driving currents, the irreversible voltage may increase from its initial value to a "peak" before decaying to zero. See Figures 5, 6, 8 and 12.

Half-Selected Write-Disturbed Outputs (wVhl, wVhz, dVhz)

The half-selected write-disturbed outputs are irreversible. Figure 7 shows their characteristics to be very much alike. It is seen that these outputs are larger than the reversible half-selected outputs already discussed. This is due to the contribution of the irreversible voltage. Figure 7 shows that with currents where the half-amplitude pulses are large enough to cause an appreciable switching of the core, an abrupt increase in the amplitudes of the half-selected write-disturbed outputs occurs. Under these conditions a core is said to be overdriven.

The amplitude of the irreversible component of voltage depends on the amount of magnetic flux change resulting and the relaxation time. Two symmetrical minor hysteresis loops are shown in Figure 3 which represent the half-amplitude responses from the dz and wz states. The dVhz output involves a flux change represented by the larger loop. The subsequent wVhz outputs traverse the smaller loop inside. Because of the greater flux change attending the dVhz at normal driving currents than the wVhz outputs, the dVhz output is proportionately larger. This difference is clearly shown in Figure 5 and also indicated by the curves in Figure 7. A similar analysis of the wVhl outputs shows, that to a lesser extent, a difference between the first wVhl and the subsequent wVhl outputs also might be expected. A split in the wVhl outputs may be observed but the difference is very much smaller than that between the dVhz and wVhz.

For normal driving currents the wVhl and dVhz are slightly larger than the wVhz. However, when overdriven Figure 7 shows the wVhz to be the largest half-selected output. READ polarity pulses tend to demagnetize the ONE states but act oppositely on the ZERO states, therefore, the relaxation time of the irreversible component of the wVhl is longer than those of the dVhz and wVhz outputs. For this reason when overdriving, the wVhz and dVhz outputs are larger in amplitude but proportionately shorter in duration than the wVhl outputs. See Figures 5 and 6. For the same reason Figure 5 shows the dVhz to be of smaller amplitude and longer duration than the wVhz outputs when overdriven.

First Half-Selected ONE Output (uVhl)

The first half-selected ONE is important because of its large irreversible component. In the normal driving range the uVhl is decidedly the largest half-selected output. See Figures 6 and 7. Unlike the other irreversible half-selected outputs however, its amplitude is relatively insensitive to overdriving; rather, the uVhl responds to overdriving by developing an extremely prolonged irreversible voltage output which has a duration several times longer than the total full-selected switching time of the core. See Figure 6. This fact has a significant effect on the operation of a magnetic memory since, if sufficient time is not allowed for the irreversible change associated with the uVhl to take place, the phenomenon of disturb sensitivity is introduced. Disturb sensitivity is a condition where a single disturbing pulse is not sufficient to stabilize the remnant magnetic state of a core. It is this same effect, when acting from the uz state with the half-WRITE pulse that causes the wVhz to become greater than the dVhz when overdriving.

Disturb sensitivity occurs with all irreversible outputs when overdriving. For example, Figure 14 shows the effect of disturb sensitivity on strobe time value of the wVhl output. Figures 5 and 6 photographically show the differences between the first and second wVhz and wVhl, respectively.

Undisturbed ONE Output (uVl)

The undisturbed ONE output is the fundamental pulse response of a magnetic core. Figure 8 is a set of composite photographs of the full-selected ONE outputs at three different drive currents. The reversible "spike" at the time of maximum

current rise may be seen and subsequently the "peak" of the irreversible voltage output occurs. It is the peak voltage that is of prime interest and usefulness.

Figure 9 shows the value of the peak undisturbed ONE to be a linear function of the drive current amplitude, Im. The slope Sv, of the uV1 versus Im curve is called the transfer coefficient. The value of the peak undisturbed ONE for a given drive current may be expressed analytically as

$$ {}_{u}V_{1}(I_{m}) = {}_{u}V_{1}(I_{t}) + S_{v}(I_{m} - I_{t}) \quad I_{m} > I_{t} \qquad (3) $$

I_t is the threshold current, below which no voltage "peak" appears. This point is called the threshold of switching. See Figure 8. A core is said to be underdriven when $I_m < I_t$.

Switching Time (T_s)

The switching time of a core is defined as the elapsed time between the time at which the drive current attains the value of the half-amplitude driving current and the time at which the switching voltage has dropped to ten percent of its peak. The time of peak output is measured from the same initial time. Figure 10 is a plot of the switching and peaking times of the full-selected ONE outputs; and the reciprocal of the switching time versus the driving current for the uV1 output is plotted in Figure 11. Figure 11 reveals that at higher driving currents the switching time of a core varies inversely with the drive and therefore may be expressed analytically as

$$ (I_{m} - I_{o})T_{s} = S_{w} \quad I_{m} > 2I_{o} \qquad (4) $$

where I_o is called the intercept current and S_w, the switching coefficient. The switching coefficient is a good figure of merit for a core. Since both low driving currents and fast switching times are desirable, low S_w is favorable. The departure from linearity of the inverse switching time curve at lower currents is a function of core geometry.

Read-Disturbed ONE Output (rV1)

The read-disturbed ONE output responds substantially like the undisturbed ONE except at high driving currents where the core is overdriven. When a core is overdriven the half-amplitude disturbing pulses are of sufficient magnitude to cause excessive degradation of the rV1 output. See Figures 8 and 9. Observation of the photographs in Figure 8 shows, that in addition to having a slightly smaller peak value, the rV1 response is also slightly delayed. The response of the rV1 output to a step function is faster than the uV1; however, contrary to the situation for the uV1, the rV1 irreversible magnetization change cannot begin until the driving pulse has risen to the half-amplitude value. Therefore, a delay in the rV1 switching equal to the time required to achieve half-amplitude drive occurs. Up to this time the rV1 output is completely reversible. Consequently, with rise times of the order of 0.1 μs or greater, the peak of the rV1 output occurs after the peak of the uV1 output; also, for the same reason, the spike of the rV1 is more pronounced and smaller in amplitude.

Write-Disturbed ONE Output (wV1)

The write-disturbed ONE has much in common with the other fully-selected ONE outputs. As might be expected the wV1 has a spike of intermediate amplitude between those of the uV1 and rV1; and the switching and peaking times at normal driving currents and ordinary rise times are slightly shorter than the rV1 but longer than the uV1. See Figures 8, 9, and 10. The wV1 output departs strikingly from both the uV1 and rV1 when a core is overdriven. The wV1 becomes assymetrical in appearance and the response time becomes increasingly shorter in comparison to the uV1. At very high driving currents the peak wV1 becomes greater in amplitude than the peak uV1 although the total intergrated value (i.e. the flux change) does not. This is because the wV1 switching time shortens proportionately.

Irreversible Full-Selected ZERO Outputs (dVz, wVz, rVz)

Figure 12 is a composite photograph of the full-selected ZERO outputs. The reversible uVz output is the smallest and is included for comparison purposes. Slightly larger than the uVz is the rVz output which is characterized by a distinctive double peak. The double peak of the rVz is the result of the accentuation of the spike caused by the delay in the commencement of the irreversible portion of the voltage output analogous to the situation explained for the rV1 output. This delay is further manifested in the slower response of the rVz than the other irreversible ZERO outputs.

The largest output in Figure 12 is that of the first-disturbed ZERO, dVz. It is the full-selected counterpart of the dVhz and is the ZERO output obtained from a core in a memory which has not been otherwise disturbed since writing. The remaining output shown in Figure 12, slightly smaller than the first-disturbed ZERO, is the trace of the wVz output.

Analysis of Memory Plane Outputs

Consider a memory plane consisting of a square array of n^2 cores. When a particular core is selected, the output voltage on the sense winding is the sum of the selected core output plus the half-selected outputs of the 2(n-1) half-selected cores. In order to distinguish between a ONE and a ZERO, it is necessary that the largest possible ZERO read out of the plane not be sufficiently large to be confused with a ONE. To minimize the contribution of the half-selected outputs on the read-out voltage, the sense winding is passed through the cores of the plane in a manner which results in core voltage

outputs of alternate polarities on the sense winding. A study of Figure 1 shows that the net output voltage of a plane is composed of the selected core output minus two half-selected outputs plus the net output of the remaining half-selected cores which tend to cancel one another. This latter output is referred to as the delta voltage of the plane. An equation expressing the output of such a memory plane may be written as follows:

$$V_{out} = V_s - 2V_{hs} \pm (n-2)V_\delta \qquad (5)$$

where V_{out} is the read-out voltage of the plane;
V_s the voltage output of the selected core;
V_{hs} the voltage output of any half-selected core whose output polarity on the sense winding is opposite to that of the selected core.
and V_δ the difference between the average voltage output of the half-selected cores whose polarities on the sense winding are the same as that of the selected core and the average voltage output of the half-selected cores whose polarities on the sense winding are opposite to that of the selected core, exclusive of the two Vhs outputs.

A comparison of the lowest possible ONE read-out with the largest possible ZERO read-out yields a figure of merit for a memory plane. The absolute value of the ratio of the largest possible ZERO read-out to the smallest possible ONE read-out is called the convergence ratio, C_v. The delta voltage may be either positive or negative with respect to the output of the selected core, therefore the maximum absolute value of the delta voltage is always the one which yields the most adverse output and therefore is the one of interest in evaluating cores for a memory.

Strobe Time Values

Since it is desirable to minimize the convergence ratio, the output voltage of a plane is sensed for 0.1 μs at approximately the peaking time of the rV1 output. This time of sensing is called the strobe time. Therefore the strobe time value of a core output is its value at the time of peak rV1 for the normal operating current. Figure 13 shows curves of the strobe time values versus driving current for the various half-selected outputs and the wVz and rVz outputs. No curves are shown for the reversible outputs since for a flat topped driving pulse no reversible output exists after the current rise is over. Also, it is seen that because of their short relaxation times the half-selected write-disturbed ZERO outputs do not have strobe time values in the normal driving range. However, due to the more prolonged duration of the irreversible half-selected ONE outputs, significant strobe time values do exist for them.

Memory Core Evaluation

The curves of Figure 13 enable a computation of the convergence ratio, C_v. The largest half-selected strobe time value in the normal driving range is seen to be the uVhl output. However, due to the inherent principle of operation of a memory plane, only one undisturbed core can exist on any row or column. Therefore no more than two uVhl outputs can occur with any read-out. At the lower and normal driving currents it is found that

$$C_v = \frac{wV_z - 2_uV_{hl} - (n-2)(_wV_{hl} - _wV_{hz})}{wV_1 - 2_uV_{hl} - (n-2)(_wV_{hl} - _wV_{hz})} \qquad (6)$$

When overdriving,

$$C_v = \frac{rV_z - 2_wV_{hz} - (n-2)(_wV_{hz} - _rV_{hz})}{rV_1 - 2_wV_{hz} - (n-2)(_wV_{hz} - _rV_{hz})} \qquad (7)$$

Experience with M.I.T. magnetic memories indicates that the maximum limit of convergence that is acceptable is approximately 25-30 percent. In computing C_v, the driving current operating range should be taken into account by computing the numerator for the upper current limit and the denominator for the lower limit. For example, the normal driving range for the 64 x 64 M.I.T. magnetic memories is between 750 and 900 ma. For this range and the cores represented by the curves of Figure 13, the convergence ratio from equation 6 is

$$C_v = \frac{0.16 - 2 \times 1.24 - 62 \times 0.21}{74 - 2 \times 1.20 - 62 \times 0.16} = \frac{15.3}{62} \qquad (8)$$

Therefore, for the operating range between 720 and 900 ma the convergence is 25 percent, a satisfactory figure. A smaller convergence ratio may be assured by using a narrower driving range.

When overdriving, disturb sensitivity becomes a consideration in the determination of C_v. Figure 14 shows the strobe time values of wVhl at 1125 ma as a function of the number of times the core has been half-selected for a ONE. The same phenomenon holds for all irreversible outputs. Therefore, when using equation 7 to determine the convergence ratio, the values of the voltage outputs used should be those for a core many times disturbed.

Conclusions

The pulsed voltage outputs obtained from magnetic cores with two-to-one selection may be classified as either reversible or irreversible. Basically, only fourteen different outputs exist, four reversible and ten irreversible. Reversible outputs are linear functions of the time derivative of the driving current pulse whereas irreversible outputs have an additional component caused by an irreversible change in the magnetization. Reversible outputs are insensitive to overdriving whereas irreversible outputs are extremely sensitive.

The linear characteristic of the full-selected ONE output may be expressed analytically by equation 3 and the switching time by equation 4.

The output voltage of a magnetic core memory plane of the M.I.T. type is given by equation 5. Based on equation 5 and the knowledge presented concerning core voltage outputs, the quality of memory cores may be evaluated by the computation of the convergence ratio as demonstrated.

Bibliography

1. J. W. Forrester, "Digital information storage in three dimensions using magnetic cores," Jour. Appl. Phys., vol. 22, pp. 44-48; January, 1951.

2. W. N. Papian, "A coincident-current magnetic memory cell for the storage of digital information," Proc. I.R.E., vol. 40, pp. 475-478; April, 1952.

3. Jan A. Rajchman, "Static magnetic matrix memory and switching circuits," RCA Rev., vol. XIII, pp. 183-201; June, 1952.

4. D. R. Brown and E. Albers-Schoenberg, "Ferrites speed digital computers," Electronics, pp. 146-149; April, 1952.

5. Jan A. Rajchman, "A myriabit magnetic-core matrix memory," Proc. I.R.E., vol. 41, pp. 1407-1421; October, 1953.

6. W. N. Papian, "The MIT magnetic-core memory," Proc. Eastern Joint Computer Conference, pp. 37-42; December, 1953.

7. D. R. Brown, D. A. Buck, and N. Menyuk, "A comparison of metals and ferrites for high-speed pulse operation," To be published in A.I.E.E. Transactions.

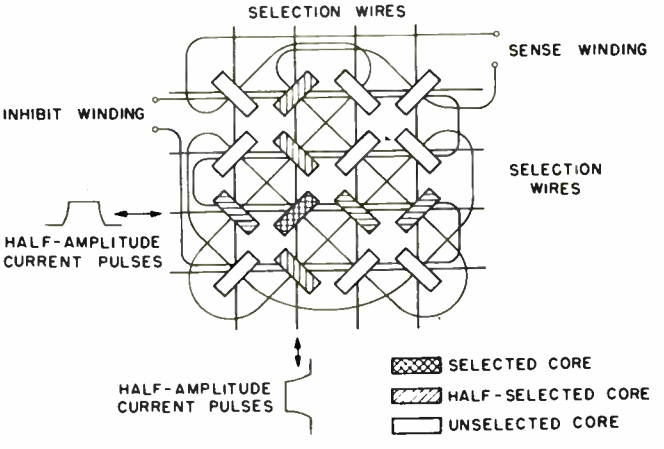


Fig. 1
Diagram of M.I.T. magnetic core memory plane showing the scheme of core selection and the wiring patterns used.

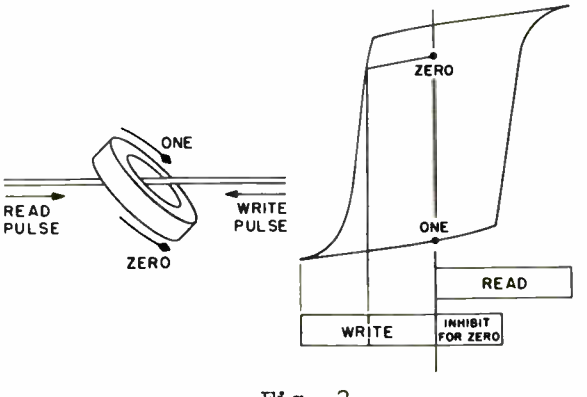


Fig. 2
Schematic indication of the storage of binary information in a magnetic core. READ pulses magnetize the cores in the ZERO direction, WRITE pulses in the ONE.

IF THE CORE IN QUESTION IS:	IF THE INFORMATION WRITTEN INTO THE SELECTED CORE IS:	
	ONE	ZERO
SELECTED	READ, WRITE	READ, $\frac{1}{2}$ WRITE
HALF-SELECTED	$\frac{1}{2}$ READ, $\frac{1}{2}$ WRITE	$\frac{1}{2}$ READ, NONE
UNSELECTED	NONE, NONE	NONE, $\frac{1}{2}$ READ

Table I
Sequences of pulses received by cores in a magnetic memory plane.

NAME	SYMBOL	PULSE SEQUENCE (READ PULSES UP, WRITE PULSES DOWN)
UNDISTURBED ONE	uV_1	
READ-DISTURBED ONE	rV_1	
WRITE-DISTURBED ONE	wV_1	
UNDISTURBED ZERO	uV_z	
FIRST-DISTURBED ZERO	dV_z	
READ-DISTURBED ZERO	rV_z	
WRITE-DISTURBED ZERO	wV_z	
FIRST HALF-SELECTED ONE	uV_{h1}	
HALF-SELECTED READ-DISTURBED ONE	rV_{h1}	
HALF-SELECTED WRITE-DISTURBED ONE	wV_{h1}	
HALF-SELECTED UNDISTURBED ZERO	uV_{hz}	
FIRST HALF-SELECTED ZERO	dV_{hz}	
HALF-SELECTED READ-DISTURBED ZERO	rV_{hz}	
HALF-SELECTED WRITE-DISTURBED ZERO	wV_{hz}	

Table II
The fourteen basic pulsed voltage outputs of magnetic memory cores for a two-to-one selection system.

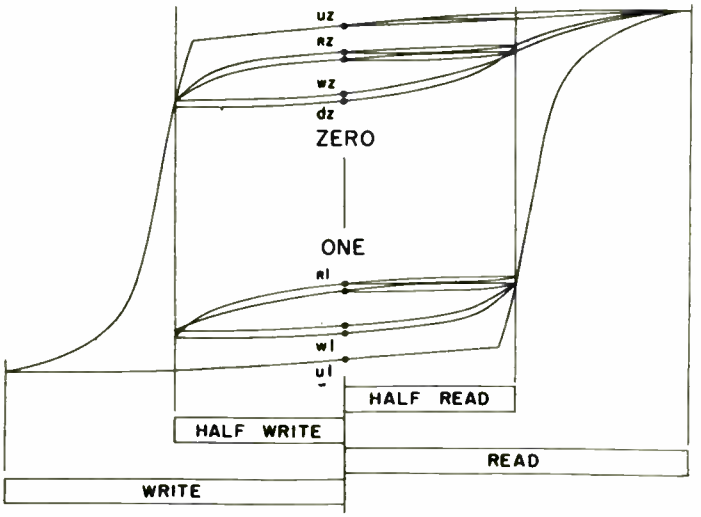


Fig. 3
The basic hysteresis loops associated with magnetic memory core operation in a two-to-one selection system.

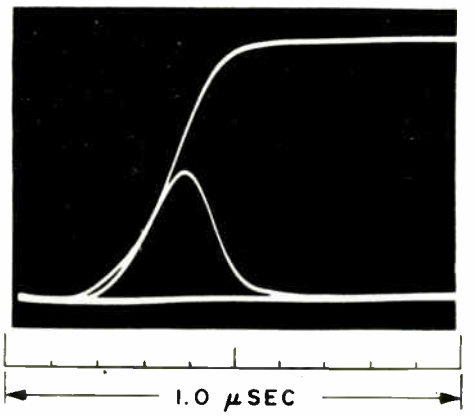


Fig. 4
A photographic comparison of the uVz output with the driving current pulse producing it illustrates how reversible outputs are constant multiples of the time derivative of the driving current pulses.

FERRAMIC S-1 MEMORY CORE

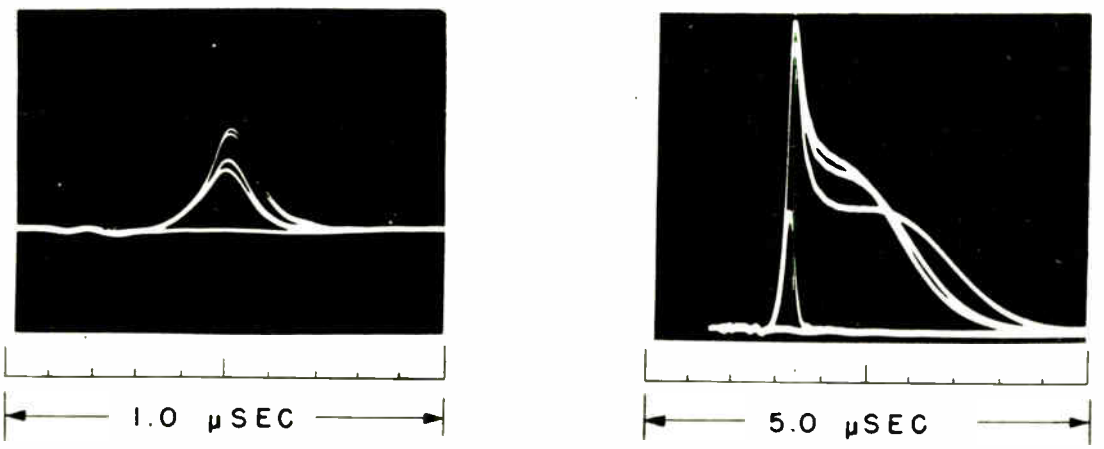


Fig. 5
Photographs of the half-selected ZERO outputs. For normal drive, from smallest to largest, uVhz, rVhz, wVhz, dVhz. For overdriven, uVhz not shown, rVhz purely reversible, wVhz and dVhz outputs show great sensitivity to overdriving. When overdriven, the dVhz is smaller in amplitude but longer in duration than the wVhz outputs. The first and second wVhz outputs are shown in order to illustrate the effect of disturb sensitivity.

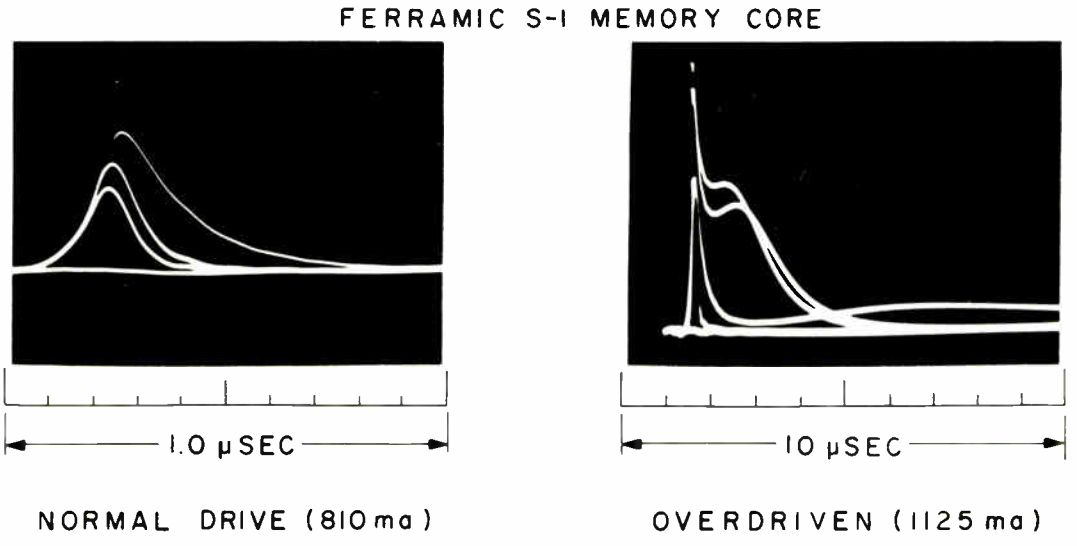


Fig. 6
Photographs of the half-selected ONE outputs. For normal drive, from smallest to largest, rVhl, wVhl, uVhl. For overdriven, rVhl purely reversible, wVhl shows great sensitivity to overdriving, uVhl responds to overdriving by developing extremely prolonged irreversible output. The first and second wVhl outputs are shown to illustrate the effect of disturb sensitivity.

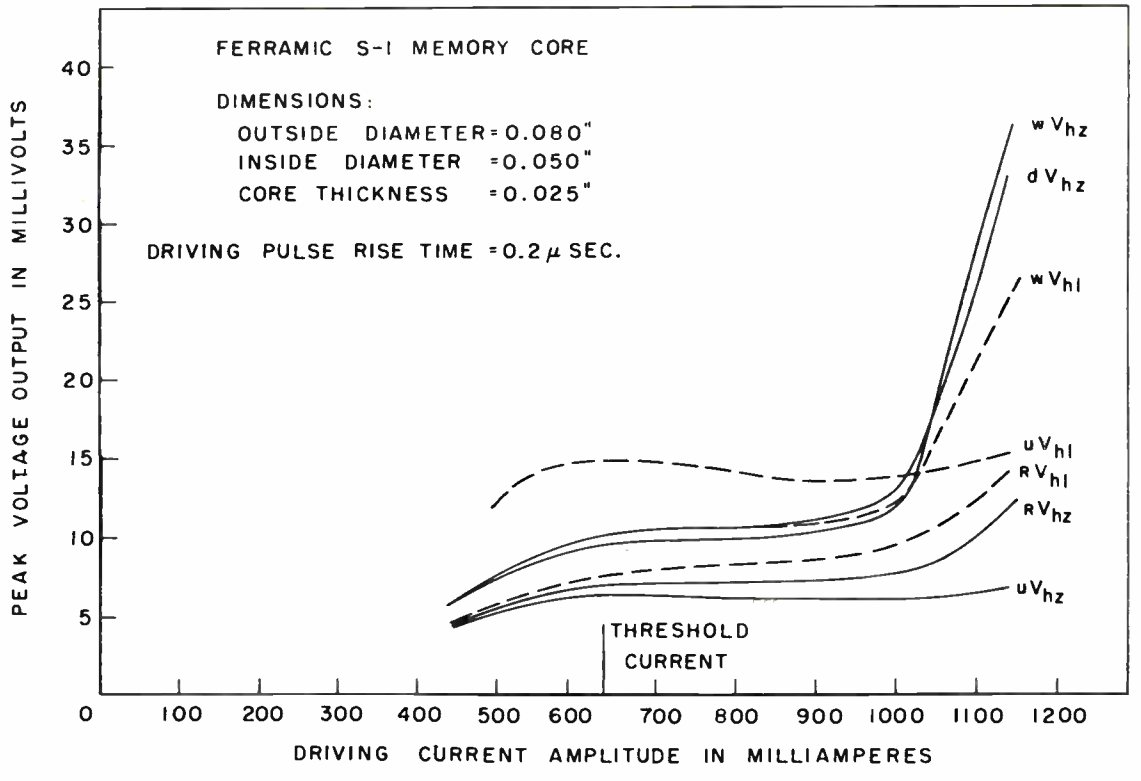


Fig. 7
Curves of the peak half-selected memory core outputs versus driving current.

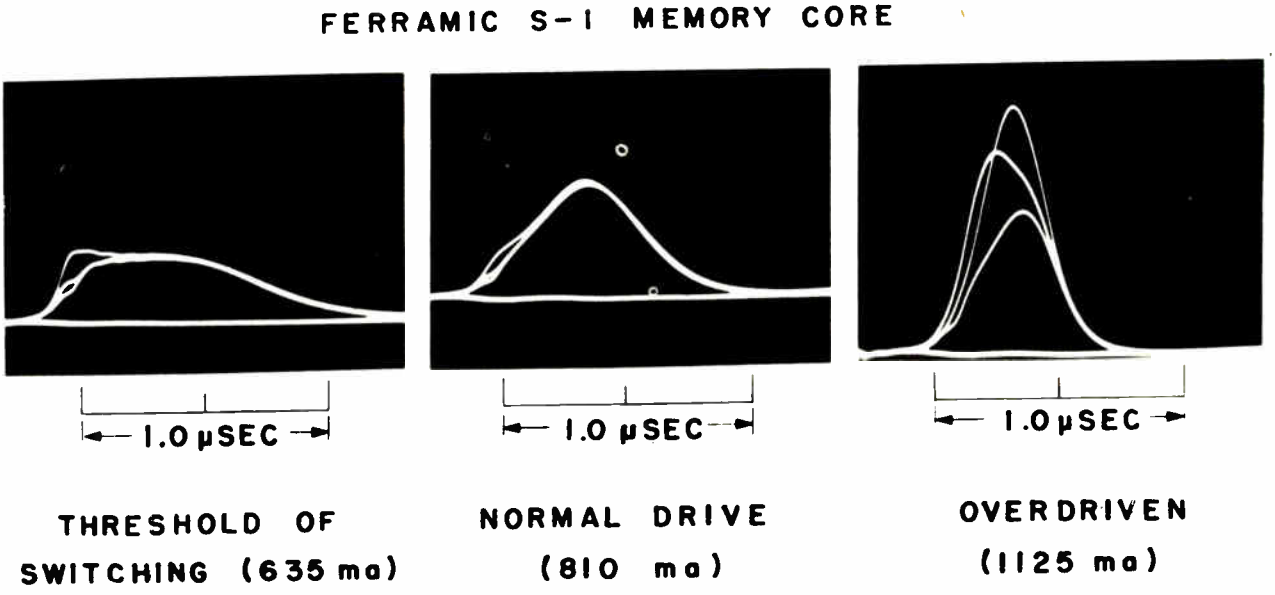


Fig. 8
Photographs of the full-selected ONE outputs showing the outputs at the threshold of switching, at normal drive, and when overdriven. From smallest to largest the outputs are rV1, wV1, and uV1.

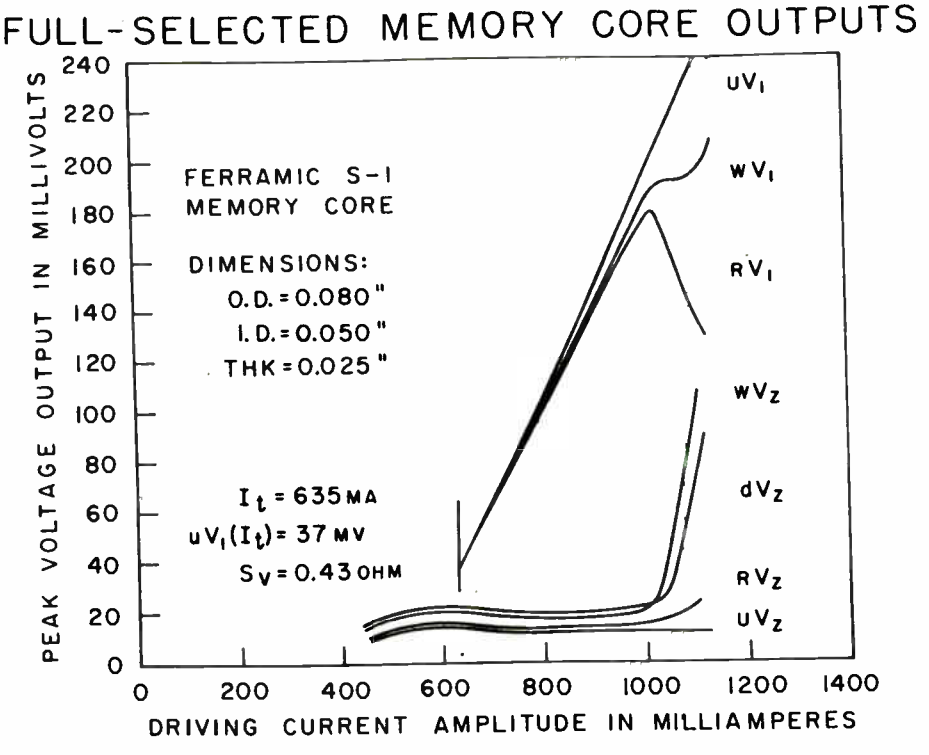


Fig. 9
Curves of the peak full-selected memory core outputs versus driving current. Note the linear response of the full-selected ONE outputs with respect to drive.

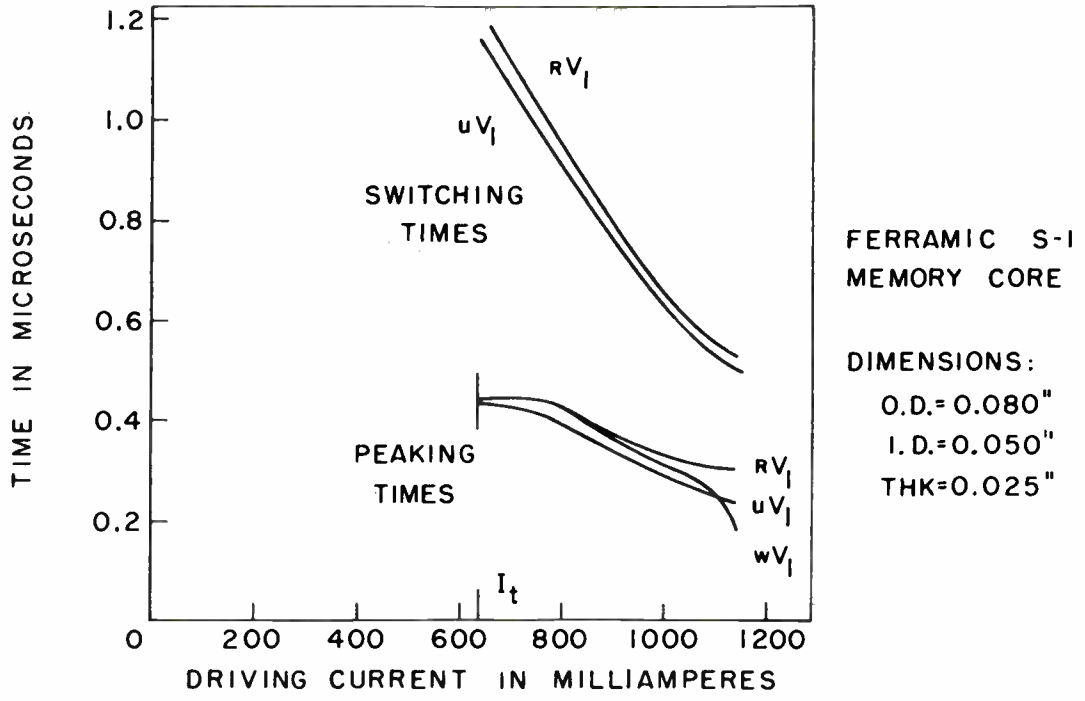


Fig. 10
Curves of the peaking and switching times of the full-selected ONE outputs versus driving current.

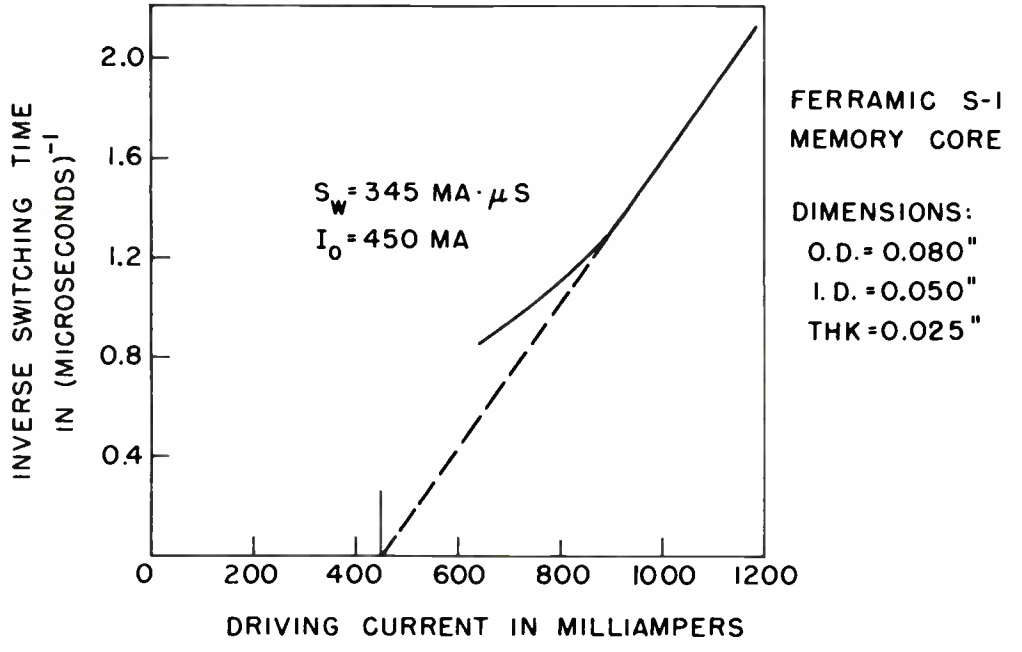


Fig. 11
Curve of the reciprocal of the switching time versus driving current showing the linear relationship of the inverse switching time with drive.

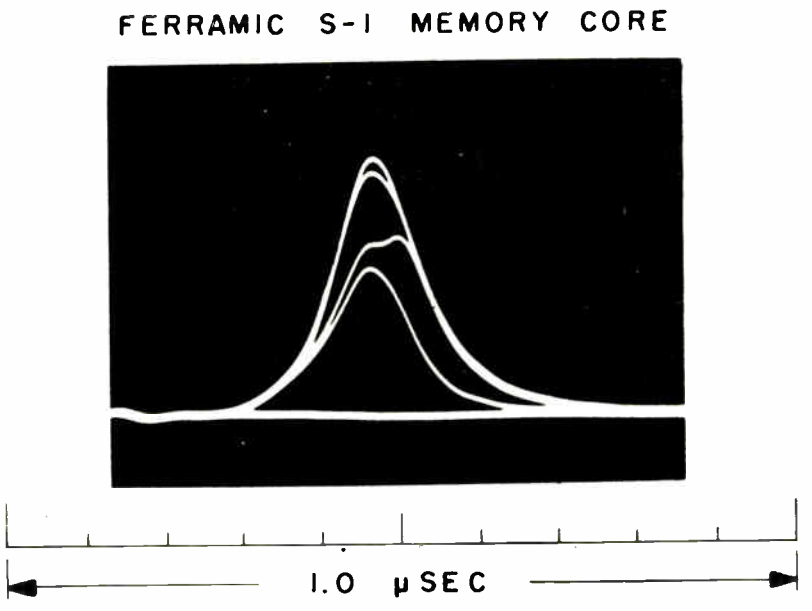


Fig. 12
Photographs of the full-selected ZERO outputs, showing from smallest to largest, uVz, rVz, wVz, dVz.

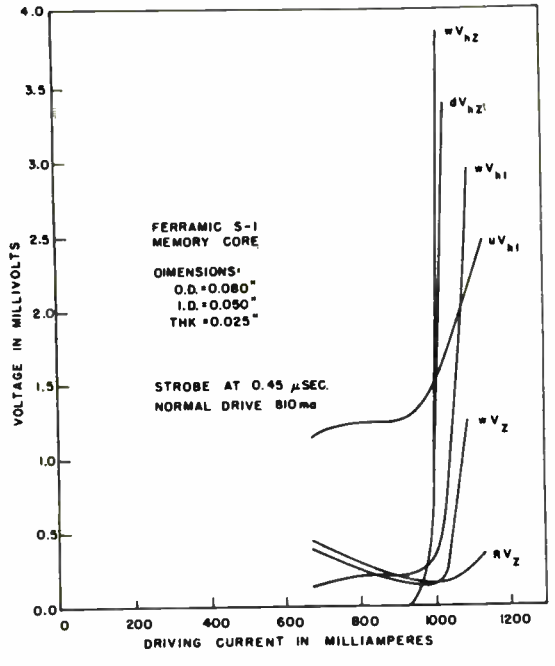


Fig. 13
Curves of the strobe time values of the various core voltage outputs versus driving current.

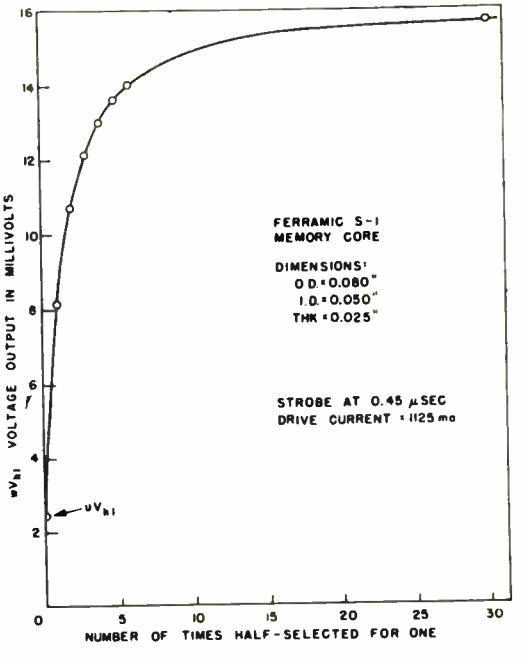


Fig. 14
Curve of strobe time values of the half-selected write-disturbed ONE outputs when overdriven versus the number of times the core has been disturbed by a half-READ followed by a half-WRITE pulse. This curve illustrates the effect of disturb sensitivity on core voltage outputs.

DIGITAL COMPUTER SYSTEMS

COMPUTER-PROGRAMMED PREVENTIVE MAINTENANCE FOR INTERNAL MEMORY SECTIONS OF THE ERA 1103 COMPUTER SYSTEM

Seymour R. Cray
Remington Rand Inc., Engineering Research Associates Division
St. Paul, Minnesota

Introduction

The ERA 1103 is a recent addition to Remington Rand's line of general purpose digital computer systems. It was designed and is being produced in quantity by the Engineering Research Associates Division. The system incorporates large internal storage capacity with very high computation rates and is intended for real time control problems as well as general scientific computation. A perspective view of this equipment is shown in Figure 1. The system operates in the parallel mode, and arithmetic is performed in the one's complement binary system. Basic internal word size is 36 binary digits. A word may represent an instruction, a pure number, or an arbitrarily-coded quantity.

Two-address instructions are employed with a program address counter normally providing the storage address of the next instruction. The form of the instruction is shown in Figure 2.

Of the 64 possible combinations in the six-bit operation code portion of the instruction, 45 are actually employed in the system repertoire. The two 15-bit address portions of the instruction generally refer to the location of operands in storage, but in some cases they specify the number of shifts or other information related to the performance of the instruction.

OPERATION	u ADDRESS	v ADDRESS
6 BITS	15 BITS	15 BITS

Figure 2. Two-Address Instruction

All arithmetic operations are performed in a double-length accumulator. This 72-bit register permits the summing of full-length products and performance of double-precision operations with a minimum of program instructions. In addition to the normal arithmetic operations, a large variety of logical operations and jump instructions are included in the system repertoire.

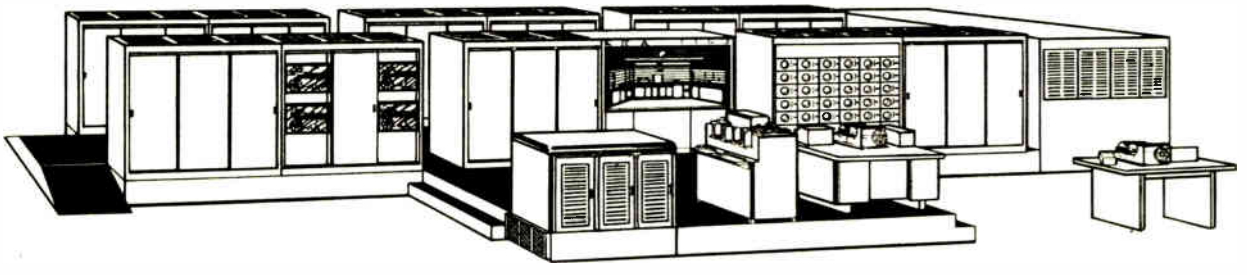


Figure 1. ERA 1103 Computer

Storage Systems

The internal memory of the ERA 1103 employs three storage media. The rapid-access portion of the memory consists of 1024 words of electrostatic (CRT) storage with an access time of 10 microseconds. The medium-speed portion consists of 16,384 words of magnetic drum storage with an average random access time of 17 milliseconds. The slow-speed memory consists of 200,000 words of magnetic tape storage on four magnetic tape mechanisms. In addition to these internal storage units, a number of external magnetic tape units and punched card equipment or other input-output devices may be used under direct system control through the input-output registers of the ERA 1103. An EXTERNAL FUNCTION instruction permits the equipment to "reach out" in effect and control external units with a wide variety of characteristics.

The electrostatic and magnetic drum storage systems are individually addressed, providing a total of 17,408 registers of directly-addressed storage. Each of these storage units communicates directly with the arithmetic system, and the magnetic drum does not depend on the electrostatic storage as a buffer. These features permit the magnetic drum system to test the electrostatic system as an isolated unit, and they permit the electrostatic system to test the magnetic drum as an isolated unit.

Preventive Maintenance

Rather elaborate provisions have been made in the ERA 1103 to detect aging elements in the computer system before the elements have become sufficiently marginal to cause failure during normal system operation. Preventive maintenance periods are scheduled at the beginning of every eight-hour period of operation. During these periods a rigorous procedure is followed which reveals any component in the system that has deteriorated to a point where it may cause failure during the following operation. A predetermined margin is thus insured about the normal operating conditions of the system. For this an extensive set of maintenance programs have been prepared which systematically examine every portion of the system as a unit while abnormally severe conditions are imposed on that unit. In the event of failure, sub-routines are provided which analyze the failure and present to maintenance personnel, via a monitoring typewriter, that portion of the system which failed. Spare plug-in chassis are provided for every position in the system so that the faulty unit may be re-

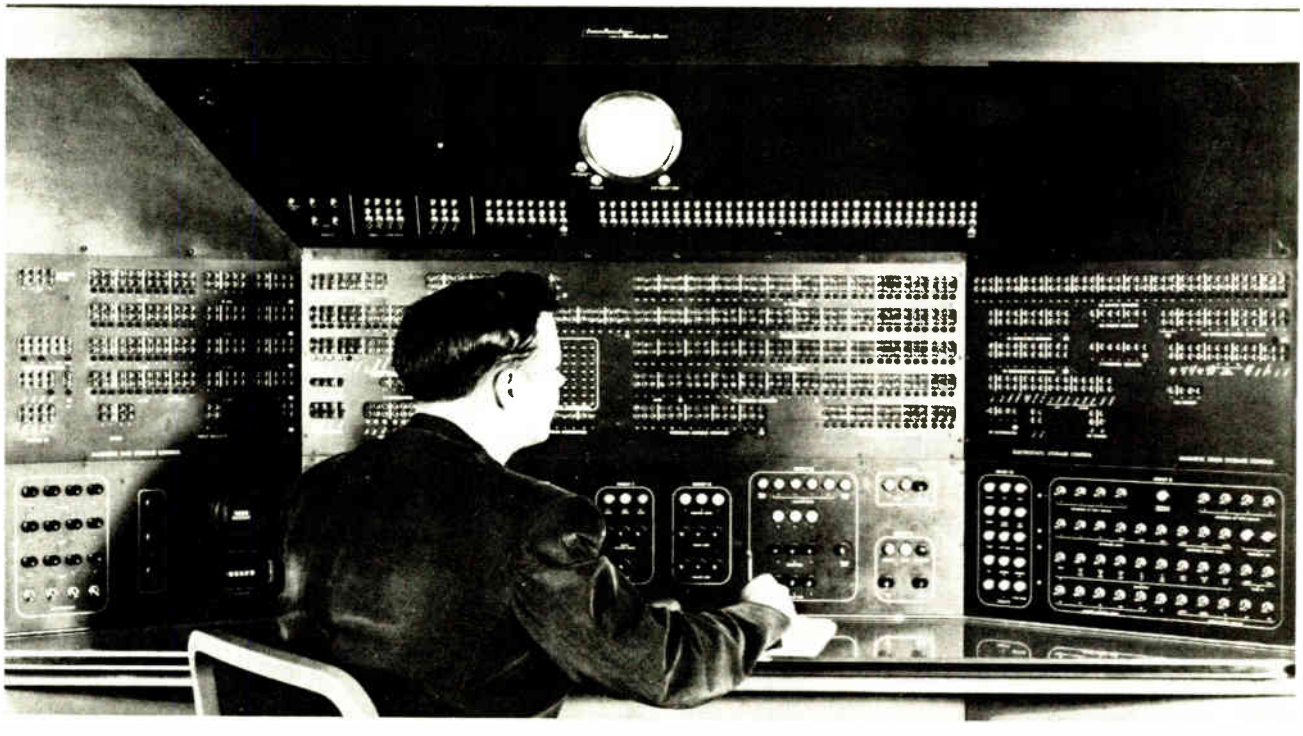


Figure 3. ERA 1103 Control Panel

placed for later repair.

Certain vital portions of the arithmetic section of the computer cannot be effectively analyzed by the maintenance program alone. For failures in this portion of the system, a control panel is provided on which both the "one" and "zero" side of every flip-flop in the system is indicated with a neon lamp. This panel is shown in Figure 3. A faulty flip-flop is identified by both lamps on, or both lamps off. Faulty transmission paths are checked by running a specially-prepared program at reduced speed. This program provides easily-identified visual indication of that transmission path which failed.

The various preventive maintenance programs are stored on a section of magnetic tape. During the scheduled maintenance periods, this magnetic tape is placed on one of the four internal magnetic tape units which are under computer control. The maintenance procedure is then a matter of selecting the desired test by manual insertion of a code number on the control panel and starting the computer in a mode designated as "Magnetic Tape Start". The desired test is then transferred from the magnetic tape to the computer directly addressed memory by an automatic "boot strap" routine on the magnetic tape.

Marginal Checks

The predetermined operating margin previously mentioned is established during maintenance periods by three types of marginal checking devices. Experience has shown that no one of these devices is really sufficient for the system as a whole, but taken together they provide a really effective overall operating margin. These abnormal conditions which are temporarily imposed on a unit during the test period fall into three categories.

(1) Reduced Filament Voltage.

During a portion of the maintenance test period, the vacumm tube heater voltage in the section of the computer under test is reduced from 6.3 volts to 5.5 volts. This provides a very effective check on the pulse amplifier and gate circuits in the system, a partial check on the flip-flop circuits, and a relatively ineffective check on the reading amplifiers in storage sections of the computer.

(2) Power Supply Variations.

Power supply voltage variations of plus and minus ten percent of normal are used to establish margins, particularly on the static elements in the system. Eight supply voltages are used in the 1103 system, and these are sequentially varied over a 20 percent range about normal while the test routine is running. This check is quite effective in establishing flip-flop margins and crystal diode network tolerances.

(3) Threshold Levels.

In the storage sections of the computer, the most effective marginal check is a variation in the reading amplifier signal threshold levels. Special equipment is provided to raise or lower the threshold clipping level during the maintenance routine in each reading amplifier in the selected storage section. Satisfactory operation with the lower threshold level establishes that no noise is within the predetermined margin of the normal discrimination level. Satisfactory operation with the upper threshold level establishes that every signal pulse is greater than the normal discrimination level by at least the predetermined margin.

Electrostatic Storage

The electrostatic portion of the 1103 memory provides 1024 words of storage with an access time between 8 and 12 microseconds depending on the phase of regeneration at the time of reference request from the control section of the system. Storage is provided by 36 special five inch cathode ray tubes using a dot-diagonal-dash type of beam deflection. Each storage tube supplies one binary digit for each of the 1024 words in a 32 by 32 array of dots and dashes. The storage tube, with associated reading amplifier and control circuitry for a digit of memory, is packaged in a plug-in unit for ease of maintenance.

ES Cycle Test

The ES Cycle Test is designed to check the access control circuitry, the addressing and deflection circuits, and the normal storage properties of the electrostatic system, but it does not check the read-around ratio of the storage tubes. The test takes 59 seconds of system time and makes over two million operand references to the ES storage with no program references. The program is operated entirely out of the magnetic drum storage section so that abnormal conditions imposed on the ES storage section will not jeopardize the proper operation of the program.

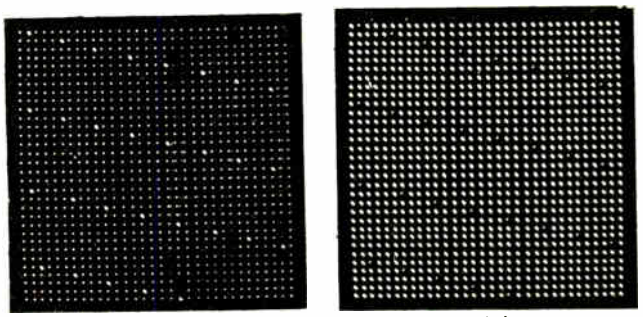
The storage pattern used in the cycle test is defined by the expression:

$$(k) = 2^k \pmod{2^{36}-1}$$

That is, the word stored at address k is the binary number 2^k corrected to machine modulus. Each word contains a single "one", in a digit position determined by k. A typical pattern which appears on the storage tubes during this test is shown in figure 4a. This pattern, when cycled through all of the ES address positions, presents many of the data singularities which can occur in a random distribution.

Considerable use is made in this and other maintenance programs of an 1103 instruction

called the "Repeat Instruction." This instruction provides for the automatic repetition of the next instruction in the program up to 1024 times with selective advancing of the execution addresses and without further references to storage. The use of this instruction permits a great reduction in program time whereever repetitive processes are involved.



(a) (b)

Figure 4. E.S. Cycle Test Patterns

Operation of the ES Cycle Test may be outlined as follows.

(1) The 1024 word pattern defined by the above expression is generated in the magnetic drum storage section and then copied into the ES storage section. The pattern is formed on the magnetic drum in one drum revolution using a repeated "Add and Transmit" instruction. Then, using a repeated "Transmit Positive" instruction, the pattern is transferred in a block to the ES system.

(2) The pattern is cycled through the ES address positions by repeated "Transmit Positive" instructions from address k to address k-1, with the execution addresses advanced after each operation. (The repeat instruction treats the ES storage system as a closed address set, with the last address followed by the first.) The effect of these repeated transmissions is a regression of the test pattern by one address location for each 1023 transmissions.

(3) After approximately 300,000 such transmissions, the pattern has regressed one third of a complete cycle. At this point in the program the "Transmit Positive" instruction is changed to a "Transmit Negative" with the result that for the next 300,000 transmissions the pattern alternates between predominately ones and predominately zeros.

(4) After an odd number of negations of the entire pattern, the repeated instruction is returned to a "Transmit Positive", and the remainder of the cycle is completed with a predominance of ones stored, as shown in Figure 4b.

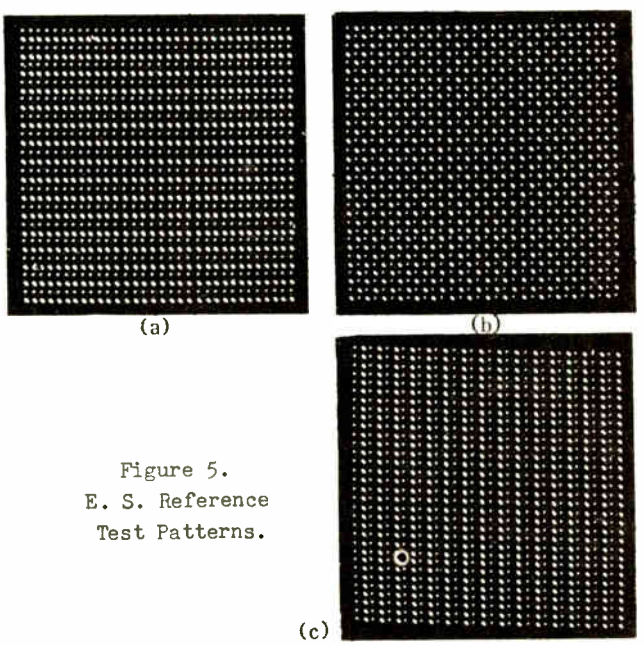
(5) After the completion of $(1023)^2$ such operations, the ES test pattern has regressed to its original position and is the complement of the original pattern as stored on the magnetic drum.

(6) A word-by-word comparison is then made with the original pattern on the magnetic drum. In the event of a discrepancy, a subroutine presents the digit position of failure to maintenance personnel through the monitoring typewriter. Since the circuitry for each digit position is contained in a unit chassis, the digit position of failure identifies which chassis must be removed for maintenance.

ES Reference Test

The "ES Reference Test" is designed to check interaction between storage positions as a result of repeated references to the same address. During this test each address in the ES storage system is sequentially referenced N times in rapid succession, where N is a parameter stored in the program with a normal value of 256. Following these repeated transmissions, a word-by-word comparison is made between the entire ES storage contents and a reference pattern on the magnetic drum. In the event of a discrepancy, indicating interaction in the ES system, the digit position of failure together with the reference number N and the type of pattern used, is presented to the maintenance personnel through the monitoring typewriter.

Any one of the three test patterns shown in Figure 5 may be selected for the ES Reference



(a) (b) (c)

Figure 5.
E. S. Reference
Test Patterns.

Test. Each test provides two scans of the entire pattern, once as shown in Figure 5 and once with the complement of that pattern. In this way each address location is tested both with a one and with a zero stored.

In the event of several simultaneous failures during a maintenance period, the repetition of the test with the three different patterns provides information as to adjustments that may be necessary on the dash deflection circuits which are common to all storage units. For example, if pattern 5a causes storage errors and patterns 5b and 5c do not, a change in the dash angle toward the horizontal is indicated. If only pattern 5c causes failures, the dash angle should be shifted toward the vertical.

Magnetic Drum Storage

The magnetic drum portion of the 1103 memory provides 16,384 words of directly-addressed storage. The information is divided into four groups of tracks with 4096 angular positions about the periphery of the drum. Surface speed is 1600 inches per second with a pulse density of 80 per inch. The period of the drum is 34 milliseconds. The reading and writing circuits are designed so that either a reading or a writing reference may be accepted every 32 microseconds. This feature is particularly valuable with the repeat instruction since many types of repeated operations can take advantage of the sequential character of the storage locations.

MD Storage Test

The preventive maintenance program for the magnetic drum storage system is operated entirely from the electrostatic system. This test takes 100 seconds of system time and includes 16 reading references and 16 writing references to each of the 16,348 addresses on the magnetic drum. Various combinations of adjacent data and transient conditions are tested for both a one and a zero stored in each bit position on the drum. These operations, performed with the repeat instruction and an eight-cell drum interlace, make 1024 references of alternate read and write per drum revolution. Each of the transient conditions of read after write with minimum spacing is checked for the four combinations of binary data. In the event of a check discrepancy in any one of the transfer verifications, the maintenance program provides for an automatic search of the entire drum contents and a presentation on the monitoring typewriter of the addresses involved in the failure and the conditions associated with the failure.

Results

Figure 6 presents a summary of operational experience on the ERA 1103 for the first six months of 1954. Scheduled maintenance periods are provided once per eight-hour shift. The unscheduled maintenance classification includes down time due to failures in auxiliary equipment and power failures as well as internal system failures.

	Jan.	Feb.	March	April	May	June
Total hours	338	325	400	366	409	549
Production time	61%	70%	68%	74%	75%	82%
Scheduled maintenance	30%	26%	25%	23%	21%	14%
Unscheduled maintenance	9%	4%	7%	3%	4%	4%
Average hours production time between unscheduled maintenance periods	18	21	24	25	28	41

Figure 6. Summary of ERA 1103 Operation.

AN INPUT-OUTPUT SYSTEM FOR A DIGITAL CONTROL COMPUTER

L. P. Retzinger, Jr.
Senior Engineer
Librascope, Incorporated
Glendale, California

Summary--A control system involving twelve input functions and fourteen output functions using a digital computer as the computation element is discussed. A method of converting shaft rotation to serial binary information, time-sharing the basic circuitry, is described. In going from serial digital control signals to output shaft positions, a novel system is used to generate and store semi-proportional positioning signals which serve as inputs to magnetic amplifiers. Throughout the system, time-sharing is utilized to a high degree, and independence of supply voltage, temperature, and other factors normally affecting analog systems is stressed.

Introduction

Until recent years, automatic control systems have been greatly limited in accuracy and resolution because they have usually involved the use of analog data transmission and computation techniques. The development of digital computation techniques and the incorporation of these techniques in the control loop of an automatic system now make it possible to combine digital control signals to an almost unlimited degree of accuracy and resolution, thus producing a digital controlling signal of equal accuracy and resolution. Since automatic systems generally involve the control of physical elements which are analog in nature, i. e., shaft rotations, linear displacements, etc., the high degree of accuracy obtainable using digital computation techniques is of little value unless these analog quantities can be translated to their digital equivalents with equally high accuracy. Likewise, the digital controlling signal produced must be translated to its equivalent analog form without losing any of its significance. During the past five years, many digital control development programs have been in progress. In the early stages of development of a control computer, the stress is often placed on the arithmetic problem involved in a solution of the control problem, with insufficient attention given to the input-output or communication problem.

An input-output system for a digital control computer may have the following characteristics in keeping with digital techniques:

1. Conversion from analog-to-digital without involving intermediate analog steps is desirable.

2. Accuracy and repeatability of system should be as independent of supply voltage, frequency, temperature, and other variations as basic digital components and systems.

3. For multi-channel input and output systems, maximum time-sharing is important, with switching effected on digital rather than analog signals.

4. Conversion time should be compatible with sampling rate.

Due to the nature of the control signals in many physical systems, it is often impossible to provide an ideal input-output system efficiently. A large number of automatic control systems, however, do receive a set of shaft positions as analog inputs. The control problem involves the conversion of these shaft positions to equivalent digital data, and combination of the data by a digital arithmetic unit in accordance with the control equations of the system, thus producing digital controlling signals for positioning a set of output shafts. This paper deals with a multi-channel input-output system of this type.

Shaft Position-to-Binary Transducer

The input-output system to be described is used with a serial binary digital differential analyzer. In order to understand the nature of the input-output problem, it is desirable to describe briefly the nature of the computer. Using a magnetic drum memory, the computer operates at a clock pulse rate of approximately 200 kilocycles. Each number storage channel of the drum is divided into 127 blocks or words, containing 18 binary digits per block. One channel in the memory, called the U line, is available for recording all input and output signals. The rotating drum provides an access time of about 12 milliseconds.

To be compatible with the computer program, the input signals must be made available for recording in the memory in serial binary code,

least significant digit first. The computer is provided with a block counter and a pulse counter for locating any word or digit in the memory and for supplying program signals to the input-output system.

The analog inputs to the control system consist of 12 shaft positions provided by synchro follow-ups, multi-turn potentiometers, hand-cranks, etc. The range of conversion on the inputs varies from 7 binary digits to 17 binary digits. In transferring from a shaft position to a digital representation, each input must be made available for recording during its programmed block interval in serial manner, with the least significant digit appearing first in time during pulse position one of the block.

The basic element used in the conversion from shaft rotation to binary numbers is the binary coded commutator disk using a double set of pick-off brushes in order to eliminate ambiguity. The logic for using a dual sensing scheme on a digit track has been described in several technical reports and has been incorporated in the design of shaft-digital converters, both binary and decimal, throughout the country. [1] To reduce mechanical complexity and accuracy requirements, an all electronic switching scheme is used for providing the necessary systematic pick-off brush selection for non-ambiguous binary number reading. Figure 1 shows the code pattern and brush locations for the converter. The least significant or $(2)^0$ track is the outer track on disk No. 1, and has only one brush pick-off, the index brush, labeled B_0. All other digit tracks have the necessary two pick-off brushes labeled B_1, B^*_1; B_2, B^*_2; etc. The optimum angular location of pick-off brush B_n with respect to the index radius is $+\frac{360}{(2)^{k_1+2-n}}$ degrees for $1 \leq n \leq (k_1 - 1)$ where k_1 is the number of digits carried on code disk No. 1.

Pick-off B^*_n is located at $-\frac{360}{(2)^{k_1+2-n}}$ degrees with respect to the index radius. The standard converter used in the input-output system carries 7 binary digits on the input or high-speed disk, thus producing 128 binary counts per revolution of its input shaft. The range of the converter is extended to either 13 or 19 digits by gearing down by a ratio of 64 to 1 to additional code disks each containing 6 binary digits. As indicated in figure 1, the optimum angular locations on subsequent disks are the same as on the first disk with the exception that two brushes are required on the outer track.

Since the angular locations stated for either brush on the nth track are only the optimum locations, allowable limits, over which the system of brush reading is workable, may be given. In the practical converter the allowable tolerance on brush placement, with safety factor, is in the order of $\pm 1/2 \frac{360}{(2)^{k_1+2-n}}$ degrees. It is therefore evident that the angular location of brushes on the more significant tracks of a code disk is not critical. Examination of the logic involved in reading the code disks will bear out these facts.

Unambiguous Input Scanning

If a positive voltage is placed on the common brush track of the converter making all brushes in contact with metal, high or one, and all those not in contact, low or zero, a set of simple rules must be followed in reading the binary value corresponding to the input shaft position. Reading the tracks sequentially from the least significant, ambiguity is eliminated by selecting and reading the proper brush on each track as follows: If B_0 is low or zero, B^*_1 is read. If B_0 is high, B_1 is read. B^*_2 or B_2 is chosen if the reading on the $(2)^1$ track is zero or one, respectively; or generalizing:

If digit 2^{n-1} is zero, read B^*_n

If digit 2^{n-1} is one, read B_n

It becomes evident, therefore, that when reading the code disk sequentially or serially a one-digit delay memory must be provided for the digit (n-1) so that proper brush selection can be made for the nth digit. This delay memory is provided by a flip-flop called M. In order to scan the binary code tracks, a set of scan signals, P_0 P_1 P_2 P_3 . . . . . P_{16}, is required. These signals are provided by the computer pulse counter. P_0 is a 5-microsecond pulse occurring during the first digit interval of each of the 127 eighteen-digit blocks; P_1 is a 5-microsecond pulse occurring during the second digit interval, etc. Using conventional diode gating, the flip-flop M is controlled to generate the unambiguous serial binary number in the form of voltage states of its outputs M and $\overline{M}$, with the least significant digit occurring during pulse position one (i.e., at P_1 time) of a block. At the same time, the necessary brush selection signals are provided by the output of M to its input gating network. With input m receiving a trigger when its voltage level is high or one, and $_L\overline{m}$ having a low pass gate on its input, (i.e., it will receive a trigger when the gating voltage is low or zero) the logical control

networks for the M flip-flop are described by the following Boolean expressions:

$$m = (P_0 B_0 + P_1 B^*_1 + P_2 B^*_2 + P_3 B^*_3 + \ldots\ldots + P_{16} B^*_{16})\,\overline{MC}$$

$$L^{\overline{m}} = (P_0 B_0 + P_1 B_1 + P_2 B_2 + P_3 B_3 \ldots\ldots + P_{16} B_{16} + \overline{M})\,C_c$$

Here C is the computer negative clock pulse biased at the high or one signal level, and C_c is the same clock capacity coupled into the low pass gate.

Using the scan logic above and operating at a pulse rate of 200 kilocycles, an unambiguous serial binary number will be produced if commutator disk No. 1 does not turn through more than an angle of $\pm\frac{360}{2^{7+2-1}}$ or $\frac{360^\circ}{256}$ degrees during the interval between reading of $(2)^0$ and $(2)^1$; or $(2)^1$ and $(2)^2$. This disk rotation corresponds to a shaft rotation of 1/2 binary count in one pulse period and assumes that the pick-off brushes B_0, B_1, B^*_1, B_2, and B^*_2, have zero circumferential width and are located in the optimum position previously described. Due to practical mechanical considerations and the finite brush width, the motion of the disk must be limited to about 1/4 binary count during one pulse period. The maximum permissible slew rate of the disk scanning at 200 kilocycles is, therefore, given by:

$$\frac{\text{Number of counts allowable in one pulse time}}{\text{Pulse period}}$$

$$= \frac{1/4 \text{ binary count}}{5 \times 10^{-6} \text{ sec}} = 50{,}000 \text{ binary counts/sec}$$

This count rate is, of course, far above the mechanical limitation of a device of this type. The maximum slew rate necessary to meet system requirements is of the order of 200 binary counts per second.

Figure 2 is a photograph of the production model 13-digit converter designed to meet airborne specifications. The converter package includes the binary coded commutator disks, brush block assembly, and gear train between disks. Also included in the converter is a set of germanium diodes, one in series with each pick-off brush for isolation purposes when used in a multi-channel system.

The basic circuitry required to produce the binary conversion consists of 105 diodes and flip-flop M. This scan and switching circuitry is time-shared for all 12 inputs and 14 outputs. Figure 3 shows the method by which multiple inputs are handled. In order to select and read individual inputs, a, b, c, etc., block gating signals called β_a, β_b, β_c, etc., are required. These signals, 18 pulse times in length, are applied to the common brush of the converters according to the computer program. This, in effect, produces the brush summing signals B_0, B_1, B^*_1, B_2, B^*_2, etc., so that one scan matrix and flip-flop may be time-shared for all inputs and outputs; that is:

$$B_0 = \beta_a B_{0a} + \beta_b B_{0b} + \ldots\ldots\ldots + \beta_n B_{0n}$$

$$B_1 = \beta_a B_{1a} + \beta_b B_{1b} + \ldots\ldots\ldots + \beta_n B_{1n}$$

$$B^*_1 = \beta_a B^*_{1a} + \beta_b B^*_{1b} + \ldots\ldots + \beta_n B^*_{1n}$$

$$\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots$$

$$B^*_{16} = \beta_a B^*_{16a} + \beta_b B^*_{16b} + \ldots\ldots + \beta_n B^*_{16n}$$

In order to assign a specified number of binary digits for the full range of any input, k, the required number of digit tracks are connected as inputs to the scan matrix so that M will be zero for all digits in block β_k beyond the digit chosen as the most significant. The least significant digit of any input may be located in any pulse position of the block by wiring it properly into the scan matrix.

To produce necessary incremental information for the differential analyzer used for arithmetic operations of the control system, input information available at the output of the scan flip-flop is not recorded directly on the drum. By using a digital servo, the binary values contained on the input blocks of the U line are driven to the input value at the rate of one binary increment per revolution of the drum. By performing the digital operation (U-M), a digital difference signal, E, is produced. An increment is added to or subtracted from U in each input block depending on whether the sign of E produced by the previous operation (U-M) is negative or positive. U is thus servoed to the value of M for each input block.

Digital-Analog Output Servo

The output control signals produced by the arithmetic operations within the computer are required to position fourteen shafts which serve as inputs to decimal counter displays,

potentiometers, and synchro transmitters. In order to time-share the basic output elements for all outputs, the computer program is restricted so that no two outputs occur in two successive blocks on the U line. Since the outputs have different numbers of digits for their full range, flip-flop S, controlled by the computer program, is used to set the length of the output word in each output block. This flip-flop is high or one during digit time one through the most significant digit time, during each output block. By scanning a converter tied to the output shaft in accordance with the output program, error signal E, developed by operation (U-M), represents the digital difference between output shaft position M and desired output shaft position U.

Using the digital error signal, a semi-proportional error voltage is developed called $(\mathcal{E} - \mathcal{E}')$. $(\mathcal{E} - \mathcal{E}')$ is proportional to the digital error over a region called the proportional region. When digital error E is outside the proportional region, the error voltage is a constant maximum. The proportional region is chosen so that the digital error vs error voltage plot appears as in figure 4. An example of the digital results of operation (U-M) for a 10-digit output is given in table 1. The sign of the error is on the left and is always zero, for zero or positive error, and one for negative error. In order to store the 16 discrete values of digital error as shown in table 1, four flip-flops, E_4, E_3, E_2, and E_1, are required. The digital error signals stored in the error register are coded as shown in table 1. If the error is 7 binary units or greater, it will be coded in the register as +7 (binary 0111). If the error is greater than /-8/ it will be defined as a -8 (binary 1000). For $E \geq O$, flip-flop E_4 is set to the zero state. For $E < O$, E_4 is set to the one state. The Boolean expressions describing the E_4 trigger are therefore:

$$e_4 = ESC$$

$$\bar{e}_4 = \bar{E}SC$$

Here the term S prevents E_4 from changing state except during the output block when the comparison (U-M) is being made. By allowing information contained on E_4 to shift into the remainder of the error register during pulse times P_1 through P_4, the error register will be left in the proper state for $-8 \leq E \leq +7$ (i.e., E is in the proportional region). When the error is outside of the proportional region (i.e., $-8 > E > +7$), indication must be given so that E_3, E_2, and E_1 are set to either 111 for $E > +7$ or 000 for $E < -8$, as indicated in table 1. Outside the proportional region the four least significant digits of E become meaningless, since all combinations of these digits occur for both positive and negative error. Referring to table 1, it is seen that the fourth through the most significant digit of E are the same (either all ones or all zeros) only for values of digital error inside the proportional region. Applying this fact, it is evident that the control for the remainder of the error register may be described by:

$$\begin{aligned}
e_3 &= (E_4 P_{1/4} + \bar{E} E_4 P_{5/17}) SC \\
\bar{e}_3 &= (\bar{E}_4 P_{1/4} + E \bar{E}_4 P_{5/17}) SC \\
e_2 &= (E_3 P_{1/4} + \bar{E} E_4 P_{5/17}) SC \\
\bar{e}_2 &= (\bar{E}_3 P_{1/4} + E \bar{E}_4 P_{5/17}) SC \\
e_1 &= (E_2 P_{1/4} + \bar{E} E_4 P_{5/17}) SC \\
\bar{e}_1 &= (\bar{E}_2 P_{1/4} + E \bar{E}_4 P_{5/17}) SC
\end{aligned}$$

For a given output block, βk, it is therefore seen that the error register will be set to the semi-proportional digital difference between the position of output shaft k, represented by the serial binary value M_k, and the desired position of the output shaft given by U_k.

Balanced Digital-to-Voltage Converter

Since flip-flop S is always programmed low during a block following an output block, the error register will hold its outputs for conversion to error voltage and storage for approximately 90 microseconds during block β_{k+1}.

The conversion from the semi-proportional digital error, contained in the error register, to error voltage is effected by using the resistive binary weighting network shown in figure 5. A double-ended or push-pull weighting system is used in order to make the null condition on $(\mathcal{E} - \mathcal{E}')$ insensitive to supply voltage variations over a wide range. The error register flip-flops are designed having their outputs (E_4, $\bar{E}_4$, E_3, etc.) clamped between limits V_0 and V_1, to within approximately one percent of the flip-flop signal, $(V_1 - V_0)$ over supply voltage variations of the magnitude allowable for computer operations (approximately ±30 percent). The outputs of the weighting network, using the weighting resistance values shown are given by:

$$\mathcal{E} = \frac{1}{2}\left(E_4 + \frac{E_3}{2} + \frac{E_2}{4} + \frac{E_1}{8} + \frac{V_0}{8}\right)$$

$$\mathcal{E}' = \frac{1}{2}\left(E_4 + \frac{\bar{E}_3}{2} + \frac{\bar{E}_2}{4} + \frac{\bar{E}_1}{8} + \frac{V_1}{8}\right)$$

From table 1 zero error is given by $E_4 = E_3 = E_2 = E_1 = V_0$ and $\bar{E}_4 = \bar{E}_3 = \bar{E}_2 = \bar{E}_1 = V_1$.

Substituting:

$$\mathcal{E} = \frac{V_1 + V_0}{2} \qquad \mathcal{E} - \mathcal{E}' = 0$$

$$\mathcal{E}' = \frac{V_1 + V_0}{2}$$

Likewise for an error of + 1 binary units:
$E_4 = E_3 = E_2 = \overline{E}_1 = V_0$ and $\overline{E}_4 = \overline{E}_3 = \overline{E}_2 = E_1 = V_1$

$$\mathcal{E} = \frac{7\,V_0 + 9\,V_1}{16}$$

$$\mathcal{E}' = \frac{9\,V_0 + 7\,V_1}{16}$$

$$\mathcal{E} - \mathcal{E}' = \frac{V_1 - V_0}{8}$$

In general, the equation describing the output of the digital error to error voltage converter is:

$$\mathcal{E} - \mathcal{E}' = E\left(\frac{V_1 - V_0}{8}\right)$$

where E is any integer in the range

$$-8 \leq E \leq +7$$

Outside the proportional region:

$$\mathcal{E} - \mathcal{E}' = 7\left(\frac{V_1 - V_0}{8}\right) \quad \text{for } E > +7$$

$$\text{and } \mathcal{E} - \mathcal{E}' = -8\left(\frac{V_1 - V_0}{8}\right) \quad \text{for } E < -8$$

The weighting network shown in figure 5 terminates in a pair of push-pull cathode followers so that current may be made available for driving the capacitor error storage devices used. A maximum conversion error of about two percent of full scale error can be expected in the digital error to voltage error converter. This error can be tolerated since an increment of error represents about six percent of full scale error. No balance adjustments are provided in the weighting network or capacitor memories; however, a balance potentiometer is provided with each magnetic amplifier to correct for null unbalance in each individual output loop.

Error Signal Storage

Having developed a particular error voltage ($\mathcal{E}_k - \mathcal{E}_k'$) during output block β_k, provision must be made for a holding or desampling device to retain the sampled error during the 12-millisecond interval between samples. Figure 6 is a schematic diagram of a capacitor type memory used for this purpose. During block time β_{k+1} voltages $\mathcal{E}_k$ and $\mathcal{E}_k'$ are gated to condensers C_k and C_k'. Gating signals β_{k+1} and $\overline{\beta_{k+1}}$ are supplied by the computer block counter. Block signal β_{k+1} is at a voltage V_L where $V_L \leq V_0$ except during the block following the kth block, when it is at a voltage V_H, where $V_H \geq V_1$. $\overline{\beta_{k+1}}$ is a complementary signal. Diodes X_1 and X_2 (vacuum tube diodes) are normally back-biased so that the memory condensers hold their charge. During block interval β_{k+1} when the gate is opened, the memory condensers will charge or discharge to the voltage levels of $\mathcal{E}_k$ and $\mathcal{E}_k'$. The time constants R_1C and R_2C are such that the memory condensers can take on several increments of error during desampling impulse β_{k+1}.

Each capacitor memory in the output system receives a new value of error voltage every revolution of the magnetic drum memory (i.e., every 12 milliseconds).

The outputs of the capacitor memories terminate in push-pull cathode followers which drive the control windings of magnetic amplifiers. The magnetic amplifiers used operate on 400-cycle power and have sufficient gain to hold the error within plus or minus two binary units at maximum slew speeds of the output functions. A lag network is used as feedback within the magnetic amplifier to increase stability in the system. The magnetic amplifiers supply power to 400-cycle servomotors which are properly phased to drive the output shaft toward zero error. The input torque for the converter is in the order of 0.1 to 0.2 ounce-inches so that in most cases where the output is positioning a potentiometer or decimal counter, the loading due to the converter is a small percentage of the total load on the servomotor.

Figure 7 is a block diagram of several output loops which time-share the basic digital components. A mathematical analysis of this system is difficult due to its extremely nonlinear nature. An analytical study is now in progress to determine the effect of variation of system parameters.

1. References:

A Photoelectric Decimal Coded Shaft Digitizer, W. H. Libaw and L. J. Craig, Transactions of the I.R.E., PGEC, vol. EC-2 no. 3, pp. 1-4 September 1953.

An Analog-to-Digital Converter, A. D. Scarbrough,

Transactions of the I.R.E., PGEC, vol. EC-2 no. 3, pp. 5-7 September 1953

A Shaft-to-Digital Encoder, B.M. Gordon, M.A. Meyer and R.N. Nicola, Proceedings of the Western Computer Conference, Los Angeles, California, pp. 128-133 April 1954

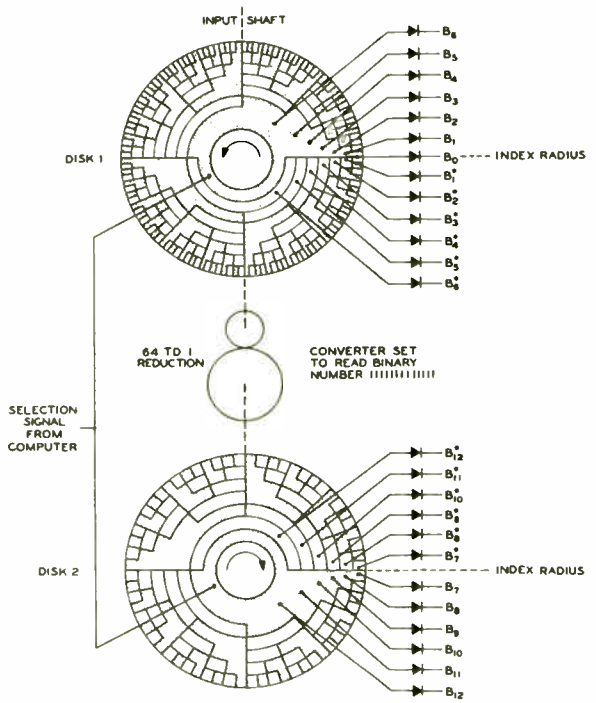


Fig. 1
Binary coded commutator showing pick-off brush locations.

Fig. 2
Analog-digital converter.

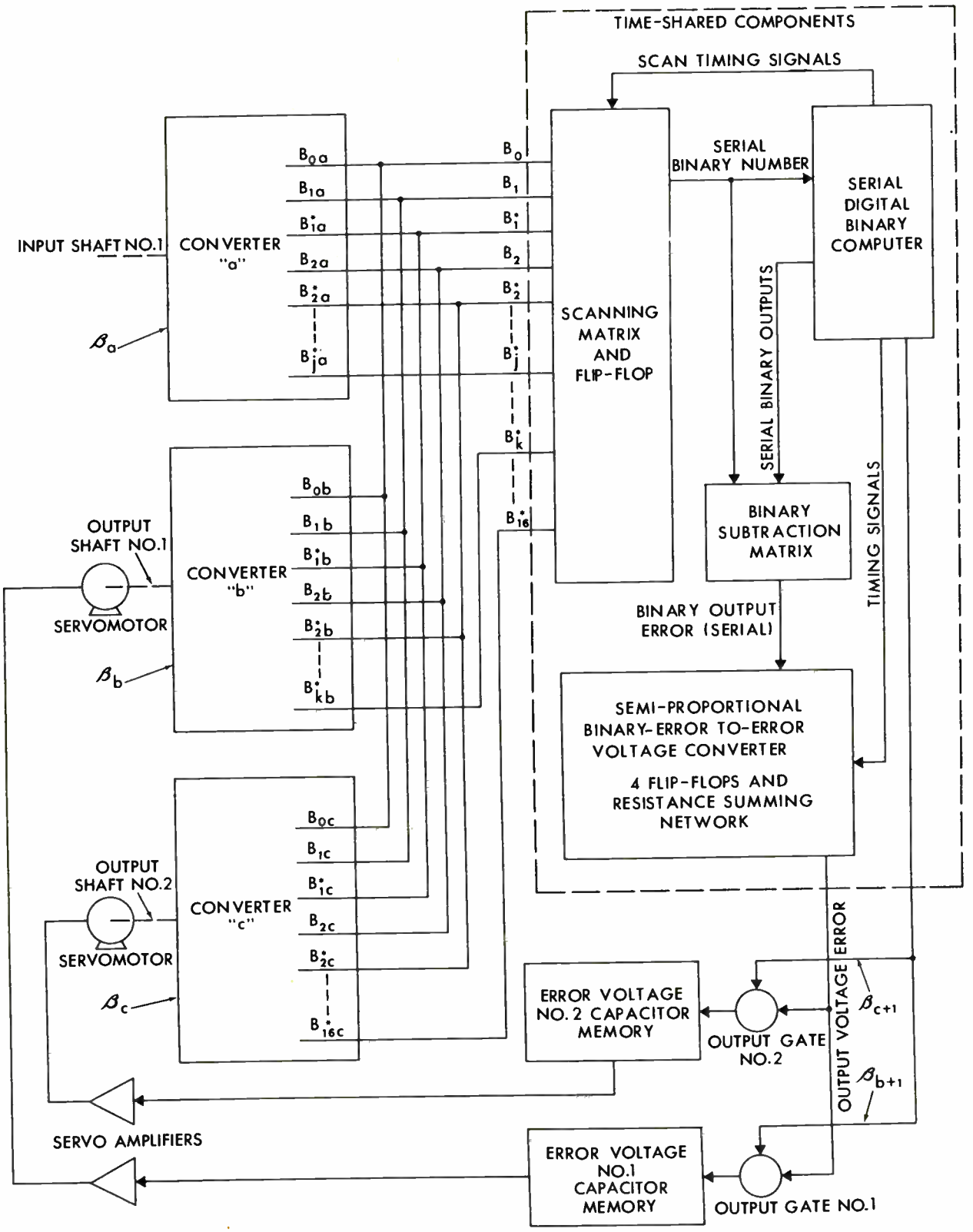


Fig. 3
Block and functional schematic, multi-channel analog-digital converter.

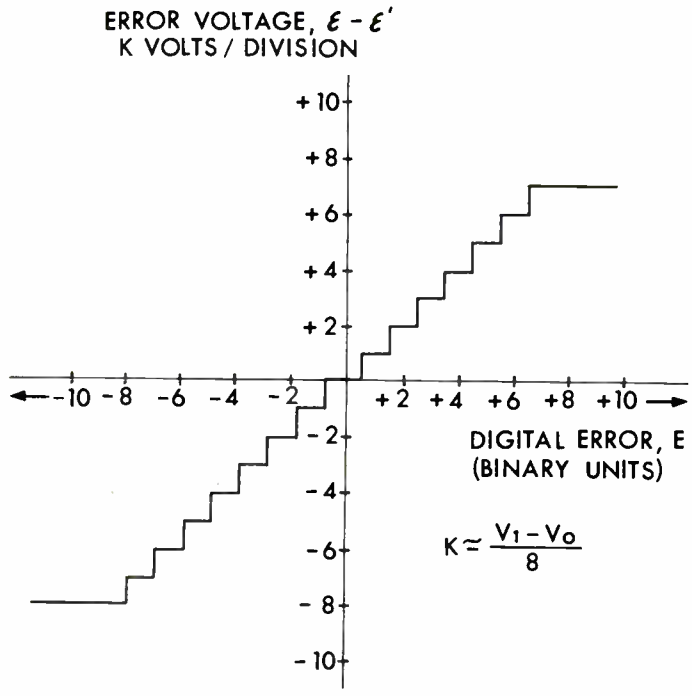


Fig. 4
Digital error vs. error voltage plot.

	Binary Digital Error, E	Decimal Value	Error Register Coding $E_4 E_3 E_2 E_1$
	1 0 0 0 0 0 0 0 0 0 0	-512	1 0 0 0
	0 1 1 1 1 1 1 1 1 1 1	+511	0 1 1 1
	0 1 1 1 1 1 1 1 1 1 0	+510	0 1 1 1
	.	.	.
	.	.	.
	.	.	.
	.	.	.
	.	.	.
	0 0 1 1 0 1 0 0 0 0	+208	0 1 1 1
	.	.	.
	.	.	.
	.	.	.
	0 0 0 0 0 0 1 0 1 1	.	.
	0 0 0 0 0 0 1 0 1 0	+10	0 1 1 1
	0 0 0 0 0 0 1 0 0 1	+9	0 1 1 1
	0 0 0 0 0 0 1 0 0 0	+8	0 1 1 1
	0 0 0 0 0 0 0 1 1 1	+7	0 1 1 1
	0 0 0 0 0 0 0 1 1 0	+6	0 1 1 0
	0 0 0 0 0 0 0 1 0 1	+5	0 1 0 1
	0 0 0 0 0 0 0 1 0 0	+4	0 1 0 0
	0 0 0 0 0 0 0 0 1 1	+3	0 0 1 1
	0 0 0 0 0 0 0 0 1 0	+2	0 0 1 0
Proportional Region	0 0 0 0 0 0 0 0 0 1	+1	0 0 0 1
	0 0 0 0 0 0 0 0 0 0	0	0 0 0 0
	1 1 1 1 1 1 1 1 1 1	-1	1 1 1 1
	1 1 1 1 1 1 1 1 1 0	-2	1 1 1 0
	1 1 1 1 1 1 1 1 0 1	-3	1 1 0 1
	1 1 1 1 1 1 1 1 0 0	-4	1 1 0 0
	1 1 1 1 1 1 1 0 1 1	-5	1 0 1 1
	1 1 1 1 1 1 1 0 1 0	-6	1 0 1 0
	1 1 1 1 1 1 1 0 0 1	-7	1 0 0 1
	1 1 1 1 1 1 1 0 0 0	-8	1 0 0 0
	1 1 1 1 1 1 0 1 1 1	-9	1 0 0 0
	1 1 1 1 1 1 0 1 1 0	-10	1 0 0 0
	1 1 1 1 1 1 0 1 0 1	-11	1 0 0 0
	.	.	.
	.	.	.
	1 0 1 0 1 0 0 0 0 0	-352	1 0 0 0
	.	.	.
	.	.	.
	.	.	.
	1 0 0 0 0 0 0 0 1 0	-510	1 0 0 0
	1 0 0 0 0 0 0 0 0 1	-511	1 0 0 0
	1 0 0 0 0 0 0 0 0 0	-512	1 0 0 0
	0 0 0 1 1 1 1 1 1 1 1 1 1 0 0 0 S		
	17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	Pulse Time	

Table I

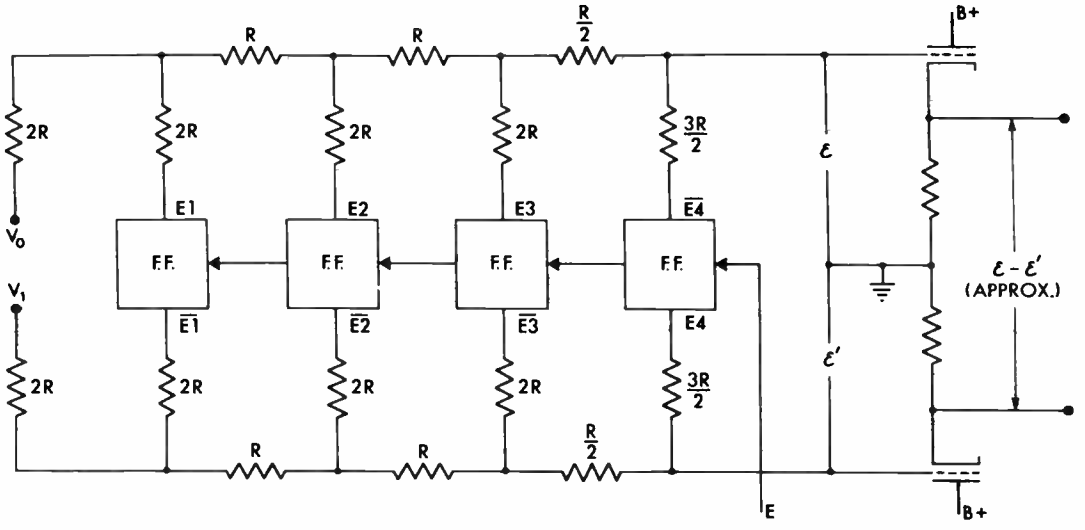


Fig. 5 - Error register and binary weighting network.

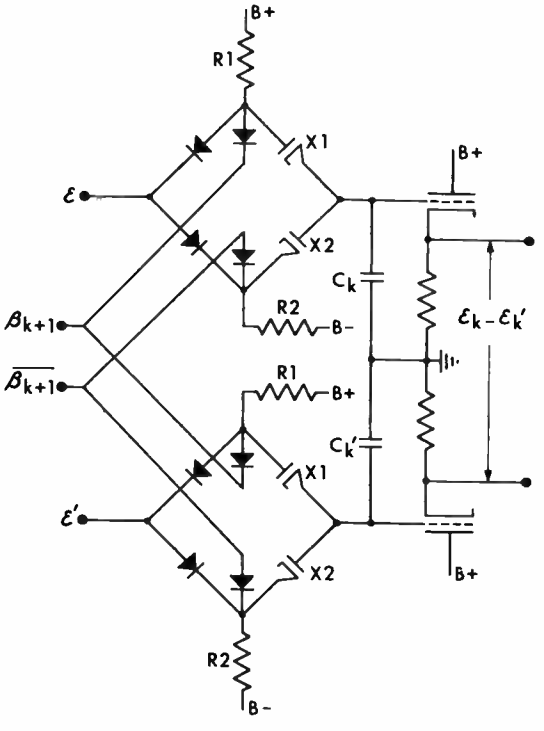


Fig. 6 - Capacitor memory and bridge gate.

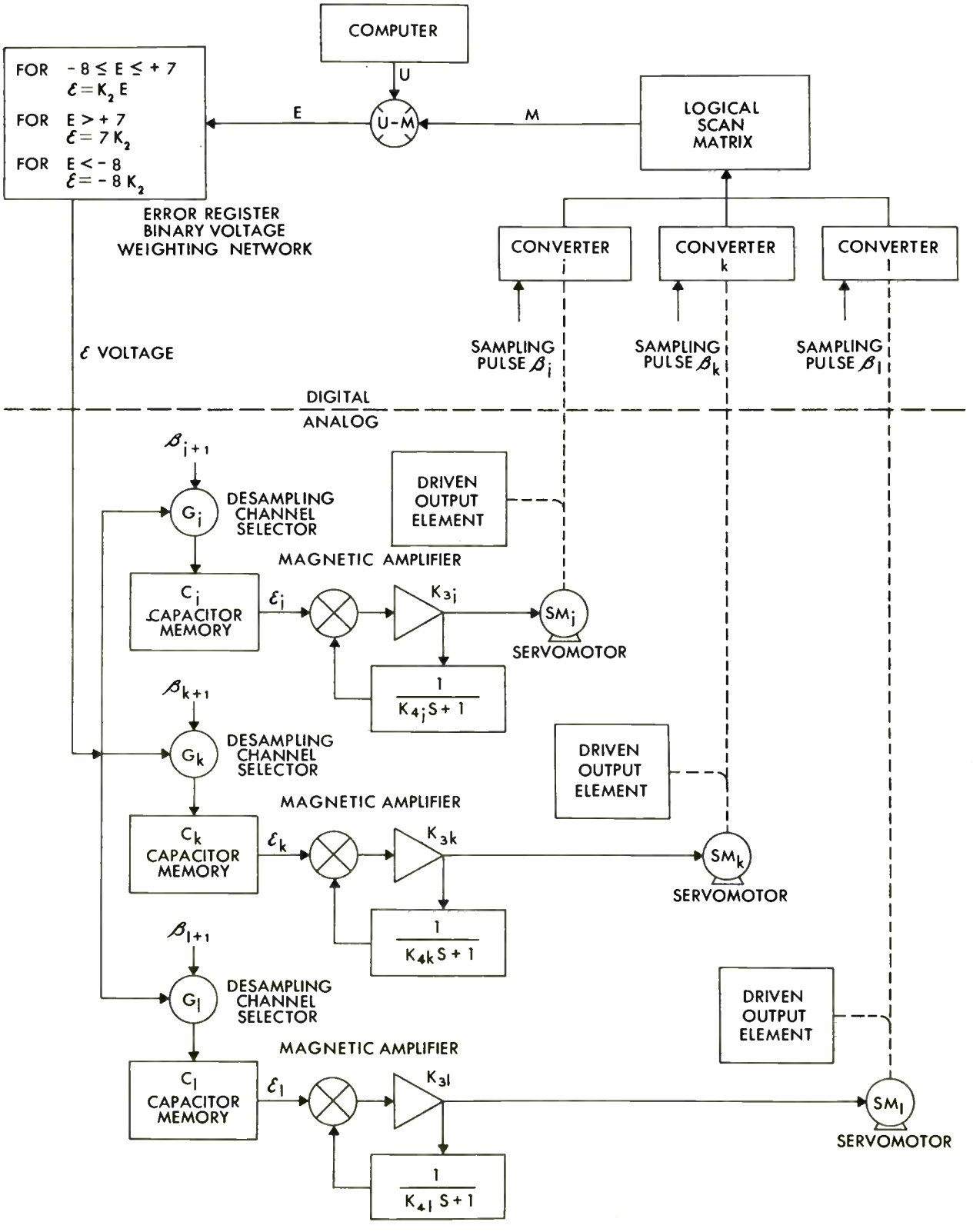


Fig. 7 - Output-servo diagram.

CHARACTERISTICS OF A LOGISTICS COMPUTER

Eugene Leonard
Electronic Computer Division
Underwood Corporation
Long Island City 6, New York

Nature of the Problem

The branches of the armed services and the subdivisions of these branches have the task of calculating their future requirements in order to determine purchasing schedules, allocation of equipment, requests to Congress for appropriations, etc. As the development of Armed Forces in the various theatres throughout the world changes, in response to changing world conditions, new calculations of future requirements must be made. To expedite these calculations, the Ordnance Department of the Army ordered the design and construction of the ORDFIAC.

When the specifications were set forth, it was decided to include enough instructions in the machine to allow its use as a general purpose computer. The fact that all the data for the requirements problem was on IBM cards plus the fact that the sources of new, raw data used IBM installations, dictated the use of IBM equipment for input and output. At the present time there is some thought of adding magnetic tape equipment because of the growth of the problem which has trebled or quadrupled in size since the machine was ordered. Because of the huge mass of data the machine would have to use, it was required that a considerable amount of error checking circuitry be built in.

Specifications

The ORDFIAC is a completely serial machine with a basic clock rate of 107 kilocycles. It uses a three-address, excess-three decimal representation with a 36-bit word length representing eight decimal digits and the sign. The decimal point is fixed at the extreme left. The memory consists of a magnetic drum with a capacity of 10,000 words which are distributed among 100 relay selected channels. The drum has two 10-word recirculating, rapid access channels and two timing channels, one serving as a spare.

The overall speed of the machine observed in actual use is about 5% faster than the speed specified; however, this is probably due in a large measure to the conservative speed specification for the vector instruction to be described below. The logical or control instructions include the following.

Input

Read, from either of two IBM input stations, the number of cards specified and store the results sequentially on the drum starting with the address specified.

Output

Punch the number of cards specified via an IBM output station, based on the data stored on the drum starting with the address specified. (Input and output speeds are controlled by the standard IBM rate of 100 cards per minute or 150 characters per second, counting the sign as a character.)

Transfer (Branch)

Direct the machine to seek its next instruction from any one of three addresses depending upon whether the contents of a specified address are equal to, larger than, or less than zero. (Specified time - 85 milliseconds.)

Shift and Extract

Shift the contents of the first specified address the direction and number of digits required. Then, under the control of the digits of the contents of the second specified address, extract digits of the above shifted result into the contents of the third specified address. (Specified time - 100 milliseconds.)

Overflow

Direct the machine to seek its next instruction from either of two addresses depending upon whether or not the previous instruction resulted in an answer which exceeded the machine's capacity. (Specified time - 85 milliseconds.)

The following arithmetic instructions all have specified times of 85 milliseconds (except for the vector instruction). In addition, modification of the sign of the contents of the first address is possible in all the instructions. The sign may be reversed, forced positive, forced negative or left unchanged.

Add

The contents of the first address are algebraically added to the contents of the second address and the result stored in the third address.

Multiply

The contents of the second address are multiplied (high order multiplication with round-off) by the contents of the first address and the result stored in the third address.

Divide

The contents of the first address are divided by the contents of the second address and the rounded off quotient stored in the third address. If the quotient is equal to or greater than one, 0.99999999 is stored and overflow occurs.

Square Root

The square root of the contents of the first address is extracted (without round-off) and stored in the third address.

Vector

The contents of any number (up to 100) contained in addresses starting with the second address are multiplied (low order multiplication) individually by the contents of the first address. The individual products are algebraically added to the contents of each of an equal number (up to 100) of addresses starting with the third address and the results stored in the third and subsequent addresses. (Specified time - 1 second for 30 multiplications and additions.)

It will be seen that the operation of the vector instruction which takes the form

$$a \times b_{j+1} + c_{j+1} \qquad \text{where} \quad 0 \leq j \leq 99$$

can be easily adapted to a number of uses to be discussed below.

Physical Description of the ORDFIAC

Figure 1 shows the machine from the operator's side. Two rows of seven racks each are placed back to back with a catwalk between, affording ready accessibility to plug-in components on the outside of the racks and to the chassis wiring on the inside. This view also shows the test equipment rack, control panel and test oscilloscopes. The main computer cabinet is approximately 16 feet long, $7\frac{1}{2}$ feet high and 6 feet wide. Blowers mounted behind the bottom louvres provide cooling for those racks which require it. The racks are bolted together and the interconnecting harness arranged so that it may be removed in one unit. In this way, disassembly for transporting the machine is quite straightforward. In fact, besides the time for crating and uncrating the individual racks, disassembly and installation each take about one week.

Figure 2 shows a typical view of the outside of a rack with the crystal clusters, d.c. amplifiers and tubes plugged in. Figure 3 shows the wiring side of a chassis. It will be noted that the delay lines are mounted so that the taps are exposed and accessible. All harness leads are labelled and, of course, all components are located, on the schematics, by means of a coordinate system. Because the machine operates at 100 kilocycles, lead capacities are not critical and the cabled form of wiring shown in Figure 3 is quite satisfactory electrically as well as appearance-wise.

The machine contains about 600 vacuum tubes and about 6,500 germanium diodes arranged in four types of cluster configurations with each configuration containing either four or six diodes. An additional 1,200 diodes are used in the 200 d.c. amplifier plug-ins. The total power consumption is about 6 Kva and is brought into the machine via a 220 volt, three phase, four wire 60 cycle line. Power supply regulation is afforded only by three 2 Kva Sola regulating transformers, one of which is used exclusively for supplying heater voltage. A motor driven 2 Kva Variac transformer is used to apply heater voltage slowly when the machine is first turned on.

The 10,000-word (360,000-bit) drum is shock mounted at the bottom of one rack. The drive motor which is mounted at the top of the vertical shaft is a 3/4 h.p., three phase, 1760 r.p.m. induction motor. It was necessary to arrange the motor circuitry so that when input a.c. is switched off, the motor windings and the Sola transformer input windings are disconnected. Otherwise, the drum motor tends to act as a generator and imposes a sudden mechanical strain on the coupling between the drum and the motor.

Two separate head mounts are used to carry the writing and reading heads for the rapid access channels as well as the heads for the two timer channels. The drum was built up of a series of aluminum disks which were individually balanced, pressed on the shaft and then the whole assembly balanced. After the assembly was complete, a finishing cut was taken with the drum in its own bearings and the magnetic oxide coating was sprayed on.

Figure 4 shows a close-up of the back side of the drum assembly where a hinged panel carries the channel switching relays and associated crystal diodes. The heads may be seen in this view. Two heads are included in each dual head mount. Nine such head mounts are bolted to each head adjusting block (of which there are six) and lapped flat before installation. A shielded twisted pair is plugged into each head and connects to the appropriate channel switching relay on the hinged panel.

Logical Design Considerations

General

Since the ORDFIAC is a three-address, decimal machine with 10^4 memory locations and an eight digit word length, two instruction words are required, and two one-word (or one minor cycle) control registers provided, to store the instructions. In addition an 18-bit control register is provided to store the address of the next instruction to be done. Provision is made so that any of the control registers can have their recirculation path completed through one of the two decimal adder units in the machine.

A twelve-stage counter is used to program the machine through the steps of any given instruction. Stepping of this counter is controlled by either the completion of a memory transfer to or from the drum, or by overflows in the main decimal adder, or by completion of the formation of a partial product, etc.

The output of an instruction decoder unit and the program counter just described enter a function table to set appropriate d.c. amplifier type flip flops which enable appropriate machine functions for each step of each instruction. The section shown in Figure 2 is a portion of this function table.

Additional control equipment includes the address selector unit and the controls for the auxiliary IBM input-output equipment. The address selector divides into a channel selector and a time selector. The former compares the next channel to be selected with the presently selected channel and forces a relay check to occur if the two channels differ. The time selector unit compares the output of an address marker generator (which cycles from 00 through 99 with each drum revolution) and, upon coincidence, generates a memory transfer enabling signal. However, before this signal can occur, several checks are made as described below. In the event that memory transfer is called for and none occurs during the next two revolutions of the drum, the machine halts, lighting an appropriate indicator lamp.

The arithmetic sections of the machine include, beside the two decimal adders mentioned above, three 36-bit registers. The A and X registers may allow one digit right shift, one or two digits left shift, and one bit left shift. The L register provides for a one digit left shift. The two rapid access channels are used as ten-word registers in the input-output and vector instructions. One of these channels may have the A register inserted in its loop to provide an end-around left shift of one word. The other recirculating channel includes a one digit left shift path and also a doubler circuit. This latter register is also used in input-output operations and includes a comparison circuit used in the output or punch instruction. The arithmetic section is completed by a comparison unit.

The instructions for addition, multiplication, division, transfer, shift and overflow are quite straightforward and can be covered quite briefly. Addition is algebraic with a sign difference in the two inputs setting a "subtract" flip flop. Also, the sign of the operand whose absolute magnitude is larger, is carried through to the answer. Multiplication involves the usual formation of partial products and shifting. For convenience, the multiplier is nines complemented and stored in the X register. A least significant 1 is added to the X register contents every minor cycle, and when the least significant digit in X reaches 9, the necessary shifts occur. The round-off digit goes in as the first partial product.

Division makes use of the non-restoring system. That is, successive subtractions of the divisor from the dividend take place until overflow occurs, then the necessary shifts followed by successive additions of the divisor to the preceding remainder take place until overflow again occurs. At this point, shifts again occur and are followed by a series of subtractions. During these operations the X register, which was originally filled with minus ones (binary twos) has one added to its least significant digit during each minor cycle of addition or subtraction. The resultant least significant digit in the X register, after a series of additions has overflowed, is nines complemented to form the proper quotient digit. Upon the completion of the determination of nine quotient digits, the round-off digit is added, the sum shifted right once and the result stored in the 'c' address on the drum.

Input-Output

Input-output is possible via three IBM523 Summary Punches. Two are connected for input or reading and one for output or punching. All three machines operate at their normal 100 cards per minute rate. Since each card contains ten 8-digit words and their signs, the basic input-output rate is 150 characters per second. Punching of zero is suppressed to prevent weakening the IBM cards. However, the machine will read cards properly whether the input cards have zero suppressed or punched. A negative sign is represented by an X row punch in the most significant digit column of each word.

During the input instruction the cards are, of course, scanned row. The contents of the ten words are gradually built up in the input-output recirculating channel. When the whole card has been scanned, and a check for absence of an IBM jam completed, the contents of the recirculating channel are transferred to the proper address in the main memory. A restriction is placed on the programmer to the effect that the first word of each group of ten must occupy an address on the drum ending in zero.

In the event a jam occurs (or a computer error occurs) the machine halts. The first word address and the card count number which represent the card which jammed are preserved in the machine. Thus, after the jam is cleared, the last card is done over again and the process continued from there. The same is true in the case of a card jam (or computer error) during print out.

In the print out operation, a block of ten words, starting with a word whose address ends in zero, is taken from the main memory and stored in the recirculating channel. Then, as the IBM card progresses through the punch, a comparison circuit causes the appropriate ones of eighty thyratrons to be set. These thyratrons activate

the IBM punch magnets. After the punch stroke is started a group of four Western Electric type 275 mercury relays break the supply voltage to the punch magnets and reset the thyratrons.

Square Root

The square root instruction is similar to the divide instruction in that a non-restoring system is used. Instead of a fixed quantity (the divisor) being added or subtracted, the sum of a series is added or subtracted from first the two most significant digits of the number whose square is to be taken and, in subsequent steps, the various remainders which have been built up. The basic series used which forms the artificial subtrahend is:

$$N_i = \sum_{n=1}^{n_i} 2n_i - 1 = (n_i)^2$$

When these subtractions result in an overdraft, shifts occur. The remainder, which appears in the A register, is shifted left two places and the next two most significant digits of the original number brought into the least significant digit positions just vacated in the A register. The resulting artificial subtrahend, which is stored in the L register, is corrected after a one place left shift and the process goes into its second step.

In the second step, the process reverses. That is, a constantly decreasing quantity is added repetitively to the shifted remainder of step one, which is a negative quantity, until the result is positive as indicated by an overdraft in the adder. Again shifts and corrections occur and the third step, which is similar in action to the first, is reached. The process continues in this fashion for a total of eight steps. Following this the resultant artificial subtrahend is multiplied by five and shifted right once to give the desired square root. This latter scheme is used rather than the equivalent of the one used in division where the number of subtractions or additions required to complete each step is stored in a register to form the quotient. In square root all three arithmetic registers are used and none are free for this function. The answer, in this case, is not rounded off and frequently shows a one digit round-off error on the low side in the eighth place.

Vector Instruction

This instruction has proven itself very useful. Besides its use in matrix multiplication from which it derives its name, it is quite fast and convenient for clearing sections of the drum and transferring blocks of data on the drum. The instruction involves an iterative use of a 12-step process which handles ten words at a time until the required number of iterations has been accomplished. The common multiplier is stored in one register until the entire instruction is complete. The other data and computations are handled in the two recirculating channels on the drum.

The input-output recirculating channel stores the multiplicands in groups of ten words at a time. The partial products (as well as the final product) are built up and stored in the second recirculating channel known as the product register. As usual, the partial product addition continues until the present least significant multiplier digit has been satisfied. Then shifts occur in the normal way.

When the multiplication is complete, the input-output channel is loaded with the contents of the ten 'c' addresses next to be operated upon. After some manipulation to align the data and to check signs and magnitudes (which utilizes the one bit left shift feature of the A and X registers), the contents of the two recirculating channels are fed into the adder and the result stored in the product register until the occurrence of a memory strike allows the data to be transferred to the 'c' addresses on the drum.

In using the vector instruction for clearing to zero, all that is necessary is to make the 'b' and 'c' addresses the same, let the contents of 'a' be 10^{-8} and force a negative sign in the contents of 'a' as it is used for the vector instruction. Once a section has been cleared, other data may be transferred in by letting the cleared section represent the 'c' addresses.

Error Checking

Since the machine uses four binary digits to represent one decimal digit, it is obvious that the disallowed combination form of error checking may be used. While this type of error checking is quite powerful in the main circuitry of the machine, transfers to and from the drum offer a strong possibility of errors occurring which will not be subject to this form of checking. For this reason, three types of error checking are used.

Disallowed Number Check - In the excess-three code the six disallowed combinations are binary zero, one, two, thirteen, fourteen and fifteen. Four sets of error detectors capable of causing a halt upon the appearance of any of the above combinations are built into the machine. Two of these error detectors are used to monitor the two inputs to the main decimal adder. One is used to monitor the data input to the secondary decimal adder. The fourth error detector is used to monitor the data passing through the memory switch to and from the drum.

Relay Check - Since one hundred relays are used to select channels it is desirable to check on the functioning of these mechanical, and hence less reliable, devices. Two types of errors are possible, failure to make properly and failure to break properly.

Since the required "made" characteristics

are different for reading and for writing, somewhat different checks can be made. As was mentioned earlier, before a memory transfer can be accomplished these checks must occur. When reading, it is necessary that signal be coming from the drum before a memory transfer can occur. For writing the situation is somewhat more complex.

The most significant bit of any word is always a zero on the main memory. As will be indicated below, the recording system gives a definite output for a zero as well as for a one. Thus, when the machine goes into a writing step, before any data can be written, a zero is written in the most significant bit of every word (that is, every minor cycle). The current pulses (called 'J' pulses) in the main bus are monitored and must be of proper amplitude before the actual memory transfer to the drum is enabled. In this fashion it is possible to guarantee that at least one drum head is connected for reading or writing.

In order to check against the possibility that more than one head was connected, a relay interlock system was first used which proved entirely inadequate. Double-pole double-throw relays were used with the common bus connected to the forward contacts, the head to the center arms and a check circuit to the back contacts. The relay back contacts were connected to a logical net which required that ninety-nine back contacts be made and further, that the only relay in the forward position be the relay which was called for by the two relay matrix driving flip flops which were set. (A ten by ten matrix with twenty driving flip flops is used for channel selection).

Unfortunately, after 5,000 to 10,000 operations the relay adjustment seemed to change and, while failure to make forward rarely occurred, failure to make back contacts and shorting of all three contacts became quite frequent. As a result numerous halts occurred because of relay errors. Interestingly enough, the data being handled was unaffected in most cases. When it was affected the cause was found to be the simultaneous shorting of the three contacts (front, back and swinging). The relay error detector now functioned as an error generator.

Testing of the machine was halted and after consultation with the supplier a new batch of relays was procured. After a somewhat longer time the same phenomena occurred.

At this point it was decided to change the method of relay checking. All connections to the relay back contacts were removed and the output of the drum reading amplifier was used as is shown in Figure 5. When comparison between the present and next channel requirements indicate that a channel switch is required, all relays are reset and the output of the drum reading amplifier is examined. This output must disappear before the next relay is selected, thus causing a halt if a relay fails to break its forward contacts when it is no longer needed.

Figure 5 shows the output of the drum reading amplifier and starts during a writing step prior to the actual memory transfer. A sequence of one pulse per minor cycle occurs which represents the writing signal check discussed earlier. These are shown as 'J' signals, in Figure 5. Finally the memory transfer occurs and the group of pulses labelled "data", lasting for one minor cycle, appear. During all this time the drum reading amplifier has been electronically degated (or made far less sensitive). The drum reading amplifier is never disconnected from the common head bus. (The reason for this is explained below.)

Following the memory transfer, a short blank period appears as the degating signal is removed from the drum reading amplifier. The output of the amplifier then shows the appearance of output from the drum head until the channel relay finally breaks at point "b". This disappearance of signal then constitutes the check that the relay has not stuck forward. If the reading amplifier were connected to the common bus only during reading, it is apparent the time interval from the end of a writing memory transfer until the read-write relay made its "read" position, would serve to give a false indication of no signal output. For this reason the reading amplifier is permanently connected to the common bus and desensitized during writing.

Shortly after the relay break point "b" the new channel relay is set and, after an appropriate time, normal drum head output appears following point "m" in Figure 5. The effect of the one minor cycle blanking signal is apparent in this part of the trace.

Drum Output Check - The method of recording on the drum utilizes a phase-shift technique which gives definite indications for both binary one and binary zero. This means that the drum amplifier output waveform, before it is reshaped into the standard computer pulse waveform may be checked. The requirement is simply that both zero and one may not occur simultaneously and that either zero or one must occur in a given bit position.

Such checks have been incorporated at the main drum reading amplifier and at the two recirculating channel reading amplifiers. They have proven very powerful in detecting trouble in the drum circuitry. In nearly every case the check circuit has given its trouble indication before the actual transfer of data was affected.

Controls

The controls for the machine have been kept as simple as possible. Figure 1 shows the control arrangement involving two oscilloscopes and auxiliary equipment. Figure 6 shows a close-up of the main control panel which is sufficient for all normal manipulation of the machine. It

affords provision for one instruction operation, one memory transfer operation, breakpoint, overflow and proceed keys, for lock-up of either the control count register or all the control registers, and finally for manual control of the transfer and overflow instructions.

Figure 7 shows the auxiliary controls which may be used in maintenance or in trouble-shooting. By means of 36 toggle switches any word may be set up manually and, by means of four rotary switches, inserted at any memory location on the drum.

Two oscilloscopes are used. One serves as a display unit since it may be used to observe the contents of any register in the machine under the control of a rotary switch. It has been found that a scope display of this type has many advantages and the time required for an operator to become experienced at reading the scope is quite short. The second oscilloscope is used for maintenance and trouble-shooting.

Maintenance

The maintenance procedure which has been worked out proved relatively simple. A most effective check has been to examine pulse amplifier grid waveforms. Too much positive drive at this point indicates a weak tube. The presence of spikes, incomplete pulses, or base line noise at the grid indicates defective gating and/or delay lines. The output of a d.c. amplifier is examined for sufficient voltage drive. For purposes of maintenance a test program was developed which rapidly used all the machine instructions (except input-output) in sequence, and which was self-checking.

Each morning during the second part of the two and one half month acceptance test period, about one hour was devoted to checking the machine, section by section in the above manner. A second hour was devoted to instruction of the personnel who were to operate the machine upon delivery. The remainder of the time was devoted to running a typical requirements problem and debugging the program for that problem.

Operating Experience

Thus far, all operating experience has been under acceptance test conditions. The original contract called for an acceptance test period of up to three months. Testing started in early April, 1954, with a leap frog test. This test required forty hours free of major errors and five additional hours for each major error thereafter. During the first forty hours, five minor errors were allowed. Down time was not to exceed running time and at least one eight-hour run without any error was required.

During the test a poor solder joint in a delay line caused one major error and three minor errors. However, the machine was run until the end of the work day on a Friday, by which time it had 50 good hours, about 9 hours of down time and had completed three runs of 8 hours without error.

When the sample requirements program was started it was realized that the program called for a rapid succession of one card read-ins. The IBM drive motors could not take this treatment and a circuit change was made so that the IBM drive motors could run continuously.

By May 10, 1954, the actual run of the first part of the requirements problem was started. Operation was based on an eight-hour day with the schedule previously described under maintenance. The table of Figure 8 shows the week-by-week results as well as the totals. During this period preventative maintenance picked up 68 weak tubes. One line was found to be intermittent and replaced (this accounted for 6½ hours of down time on May 24) and one gating resistor opened requiring replacement. The only crystal replacements occurred when three crystals and a pulse transformer in a reclocking stage were blown due to the faulty placement of the oscilloscope probe during maintenance.

After June 4, since additional input data did not arrive, the test was considered completed. The raw data contained in some thirty thousand input cards had been reduced and the results compared with those previously obtained from the same input cards by other means. The comparison showed no discrepancies and the machine was accepted.

The error checking was sufficiently powerful to assure that even in a problem whose nature did not allow for checking in the program or checking by repetition, the chance of undetected errors is very small. In order to utilize this feature properly, one precaution was observed. After every two hours of operation the contents of the drum were punched out. This meant that whenever an error occurred, no more than two hours' work were in question. (This step is somewhat awkward and could be eliminated if magnetic tape was available in the machine.) In the course of the test one such two-hour series was questioned because of a circuit failure. It was redone and proved to be correct, indicating that the error was caught immediately.

Based on experience with the machine to date, some questions remain regarding maintenance procedures. Unfortunately, during the period from June 9 until July 26, the machine was not operated because it was cleaned up and crated for shipment. On July 27 installation was begun. Mechanical installation took six working days and after a wait for power to be supplied, the operational check out was begun on August 9. The machine operated satisfactorily by August 16; however, this was too late to permit inclusion of any significant operating data in this paper. Therefore, it has not yet been possible to resolve certain questions as to the proper amount of time to devote to

the maintenance procedure, how often crystals should be checked, indeed whether diode checking is necessary at all, etc.

Conclusion

There has been some discussion as to the best way to check for errors in a machine designed to handle large amounts of data. The presently available experience with the ORDFIAC indicates that the error checking circuitry described is highly dependable. Of the three general systems for error checking (duplication of equipment for checking, re-doing the problem for checking or, as in this case, specialized built-in checking equipment) the system used in this machine is most economical of time and equipment. It is gratifying, therefore, to find this type of system behaving so reliably. Obviously, the best type of special error checking circuitry to be built into a machine depends on the logic and the circuitry of the given machine and requires a good deal of design consideration. Error checking systems of the other two types save this time and expense. Nevertheless, it is felt that in future machines, where error checking is required, special internal circuitry, and not any form of duplication, should be employed.

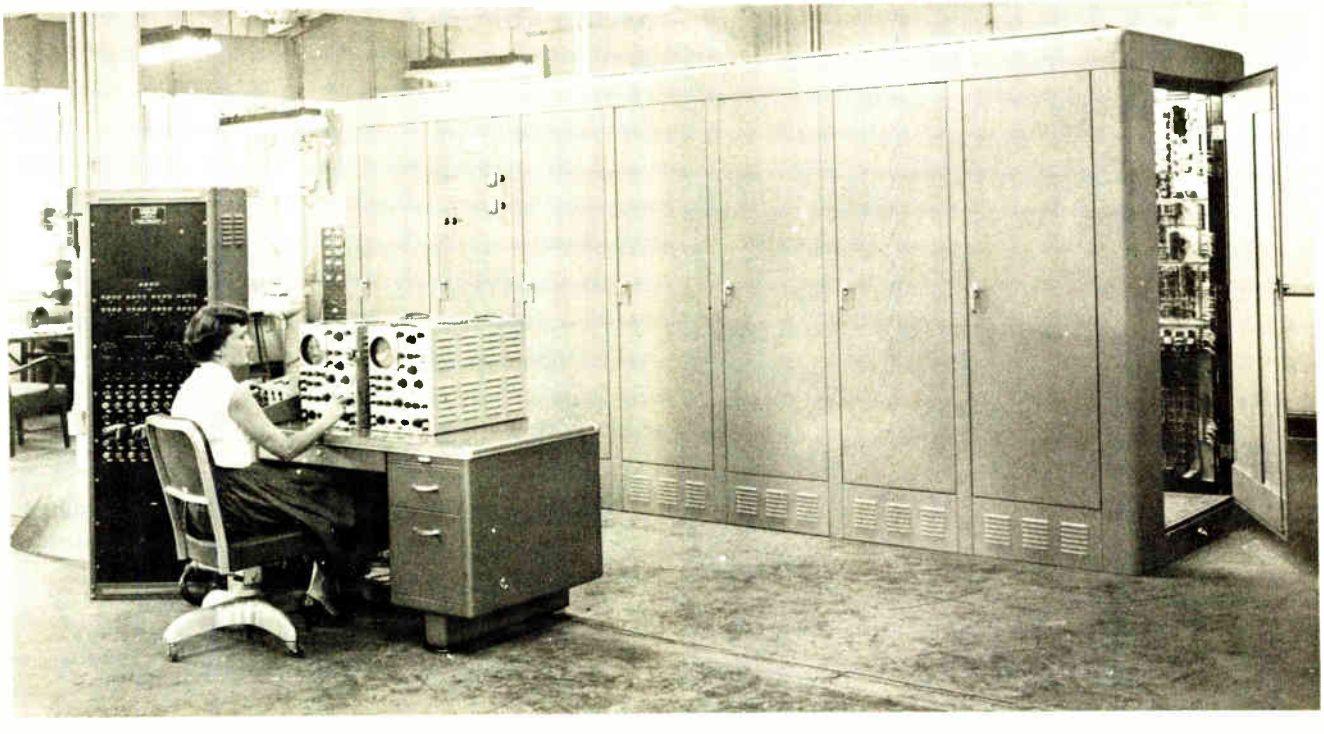


Fig. 1 - Over-all view of ORDFIAC.

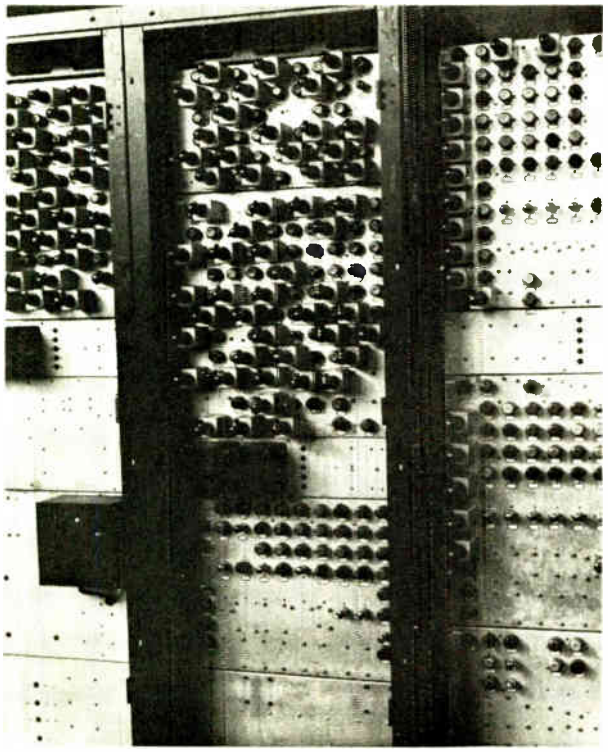


Fig. 2
Outside view of rack showing plug-in components.

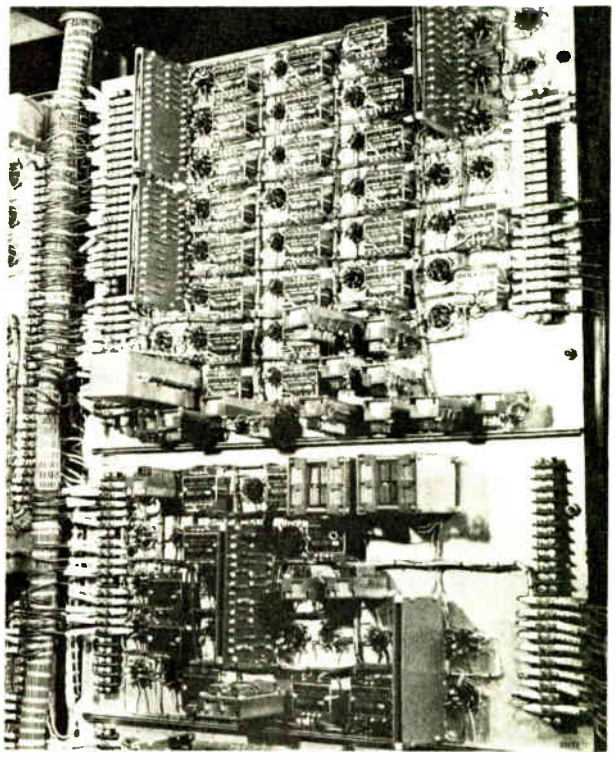


Fig. 3
Wire side view of rack.

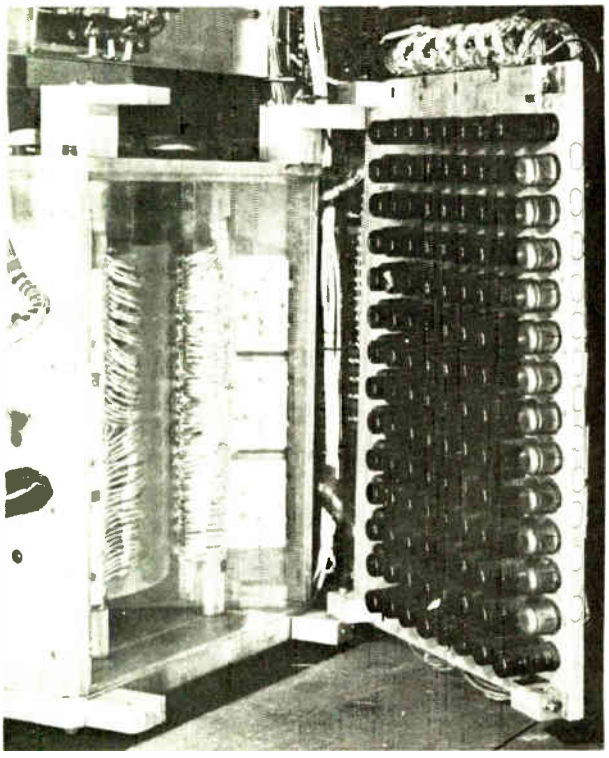


Fig. 4
Drum and channel selecting relays.

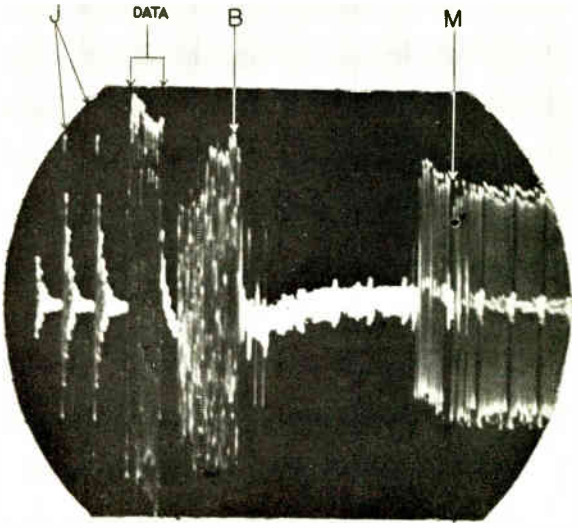


Fig. 5
Drum output waveform during relay check operation.

Fig. 6
Main control box.

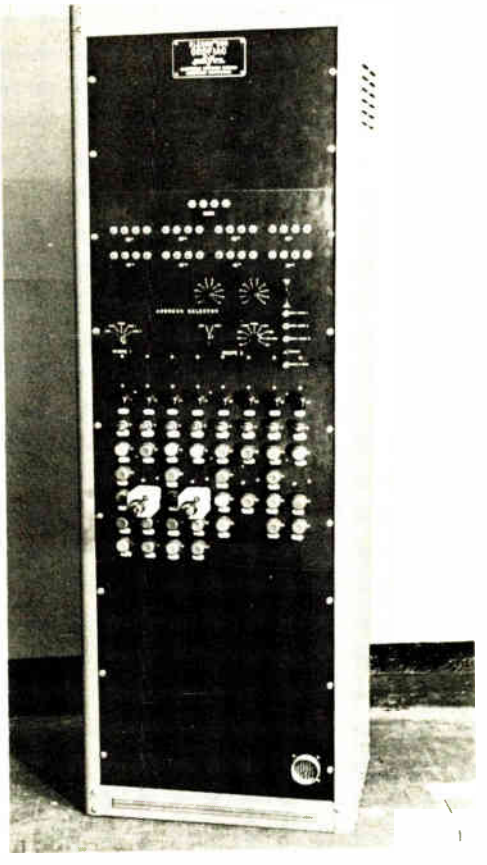


Fig. 7
Word generator, synchronizer and allied test equipment.

Period	---Maintenance--- Hours	Percentage	-----Training---- Hours	Percentage	------Down------- Hours	Percentage	-----Problem----- Hours	Percentage
5/10-5/14	7.00	16	9.16	21	3.58	8	23.75	55
5/17-5/21	7.16	18	6.33	16	7.67	20	17.92	46
5/24-5/28	8.00	18	7.08	16	7.50	17	21.42	49
6/1-6/4	6.50	21	4.50	14	-0-	0	20.00	65
Total	28.66	18	27.07	17	18.75	12	83.09	53

Fig. 8
Breakdown of ORDFIAC operating time.

THE DICO 20 DIGITAL DIFFERENTIAL ANALYZER

Floyd Steele
Digital Control Systems, Inc.

ABSTRACT

Dico 20 is a twenty integrator magnetic drum differential analyzer. The four information channels are interplexed to form two recirculating channels. Trapezoidal integration is used. Integrator numbers are 20 significant digits long. Complete integrator communication exists and either the dx or dy integrator inputs may be multiple. Decoding is accomplished for multiple inputs by nonnumerical addition. Variables are represented and processed as difference numbers. Decision is achieved by an ordinary integrator.

Dico 20 has 6 logical flip-flops and 4 memory flip-flops. There are 180 logical diodes. Conventional computer techniques are used in electronic design. The drum speed is 30 rps and the clock rate is 50 kc.

THE BENDIX G-15 GENERAL PURPOSE COMPUTER

Dr. Harry D. Huskey
University of California at Los Angeles
Los Angeles, California

and

Dr. David C. Evans
Bendix Computer Division
Bendix Aviation Corporation
Los Angeles, California

Introduction

The Bendix Model G-15 general purpose computer is a stored program machine with over 2000 words of high speed memory. All memory switching is electronic and there are sixteen words of quick access memory with average access of 600 microseconds per word. With this quick access memory and using minimum access coding it is possible to approximate a rate of 2000 additions or subtractions per second. The components of a vector may be summed using a single command per vector at the rate of 3000 terms per second. Sixty single precision multiplications or divisions may be done each second.

Standard input and output equipment includes an electric typewriter, a five hole paper tape punch, a high speed photo-electric tape reader. The computer is designed to accommodate several magnetic tape units as auxiliary memory or as input and output. With some extra equipment punched card input and output may be added. Input and output take place while computation is in process.

As available auxiliary equipment, but mounted in the same cabinet, a digital differential analyzer may be had. This digital differential analyzer has a capacity of 54 integrators and 54 constant multipliers. It may be easily programmed and accepts input and produces output in the decimal system. It produces the signals required to actuate an incremental type graph plotter.

The standard machine, except for this typewriter, is all mounted in a cabinet 27" by 30" by 60" high.

The Bendix G-15 general purpose computer is noted for the following characteristics:

First, it is small in physical size, it occupies the space of about two four-drawer letter-size filing cabinets plus a typewriter.

Second, it makes use of modern printed circuit construction.

Third, a very flexible command structure is used in the computer.

Fourth, the speed of the computation is high due to the ease of minimum access coding.

Fifth, another factor producing increased speed is the ability for the computer to carry on computation while input and output are in process.

Sixth, double precision operations generally take no more commands and less than twice the time of single precision operations.

Seventh, one cycle operations, the use of break point and of marked place operations, as well as print and type into accumulator facilitates efficient program checking.

Memory

The memory of the G-15 is a magnetic drum that rotates at 1800 revolutions per minute. On this drum there are 20 blocks of 108 words each. Each block is cyclic in character since it represents a single recirculating track on the drum. Thus, the information in each track passes through a reading amplifier, the drum is erased, and the signal is re-recorded continuously. This provides a system wherein the switching for transferring information to and from the memory is all done at high signal level. All such switching is done electronically and at high speed, there being no gaps between words. Besides this 2160 word block of memory, there is a 16 word block of quick access memory. This is in the form of 4 four-word lines. The recirculation time for a four-word line is 1.2 milliseconds. So the average access time for a number in this part of the memory is only 600 microseconds. By making use of minimum access coding, two numbers not in the same or consecutive word positions in the fast memory may be added and the answer placed in an arbitrary word position there in an average of 1.7 milliseconds.

The Command Structure

Each command in the G-15, generally, specifies a transfer type operation. That is, information is picked up from one place in the computer and sent to another place. Not only do all memory

positions serve as sources and destinations for information, but all arithmetic registers may be used as well. For example, when no multiplications or divisions are being done, the multiply register may be used as a temporary storage. Any time that information is transferred it may be modified by the sign circuits. The actual modification is specified by a part of the command and the possibilities are 1) to transfer the information unchanged; 2) to transfer the absolute value of the numbers involved; 3) to add, in which case all negative numbers are converted to complementary form; and 4) to subtract wherein negative numbers are made positive and positive are made negative and complemented with respect to 2^{28} or 2^{57}. Each command specifies whether the information being handled is to be considered a single length (29 binary digits) or double length (58 binary digits).

A single command in the computer may transfer a consecutive set of n numbers in one memory block where n is any number between 1 and 108. In this transfer the individual numbers may be considered as either single length or double length numbers. Information transferred from one memory block to another will, in general, show up in corresponding positions in the later block.

One binary position of each command is used to specify breakpoint. Breakpoint is a means of halting computation at certain points in the problem in order that the operator may check the values of numbers or see how the computation is proceeding. If things are operating satisfactorily, the flip of the switch will allow the computation to proceed and all breakpoints may be ignored. Since a particular digit in each command specifies whether that command involved breakpoint or not, it is possible to insert and remove breakpoints at will any place in the entire program. This means that the operator doesn't have to anticipate in advance the optimum place for the placing of breakpoints. Since the computer may do a maximum of almost 2000 commands in a second, it is necessary to have this breakpoint facility in order to go through the computation to a given point. It would be impractical to reach such points by one cycle operation. At such speeds it is also impractical for the operator to halt the machine at any moment and expect to be within more than a few hundred commands of where he would like to be.

It has been indicated that each command specifies a transfer from one place in the computer to another. In general, this is a matter of specifying certain long lines or blocks in the memory or one of the arithmetic registers, and of specifying a time when the transfer is to take place so that the particular word in the block is transferred.

Normally, the successive commands that the computer obeys will come from line zero or block zero or block number 1. Whether it is block 1 or 0 is determined by a flip-flop which may be set or reset by the commands. In the general mode of operation, it is expected that the main routine will be stored in block 0, and that subroutines may be stored in block number 1. The fact that commands must come from one of these two lines is no real limitation in the computer, since it requires only one command to completely replace the contents of one of these lines with the contents of any other line in the computer.

The Arithmetic Circuits

In the computer there are two accumulators, one to handle single word operation, and one to handle double word operation. The single word accumulator is used for addition and subtraction operations of single length numbers, the double word accumulator is used for addition and subtraction operations of double length numbers. The double word accumulator is also used for shift operations and in multiplication and division of both single and double length numbers.

During an execution of the addition command, the number comes from the memory and passes through the sign circuits into the accumulator. The sign circuits inspect the sign of the number and complements the number as required. The number can be added directly into the accumulator with no delay, and in fact, this makes it possible in one pass to add a sequence of consecutive numbers coming from a particular memory block. Thus, there are commands in the computer which will give the sum of all the numbers stored in one block or any smaller set of consecutive numbers stored in such a block. In the same fashion consecutive double length numbers may be added in the double length accumulator. In a similar way, minus the sum may be computed or the sum of the absolute values of consecutive numbers in a block of the memory may be computed by the use of a single command.

Besides the accumulator, there are two other two word registers used in multiplication and division. In multiplication these two registers store the multiplicand and the multiplier, and in division they store the denominator and the quotient. The numerator and the partial products are stored in the double word accumulator.

In multiplication the multiplier and the multiplicand shift and the partial products remain fixed in position. This makes it possible to terminate the product earlier than normal, multiplying by fewer than the number of significant digits in the multiplier and still producing an answer in the proper positions for use in subsequent computation. After the multiplier and multiplicand are in position, a single precision multiplication producing a double length answer may be accomplished in just 56 word times, which is approximately one-half a drum revolution in the computer. If desired, by means of two commands the multiplication may be continued another 56 word times in which case, effectively, a double precision multiplier and a double precision multiplicand have been used. However, there has been truncation of the partial products, since only

double length results can be retained. This can be corrected in a statistical manner by adding in a value for the average carry that is lost in the truncation process. This produces a reasonable approximation to a double precision answer. Of course, if exact double precision results are desired, it is possible to carry out the multiplication piece-wise, doing three single precision products and accumulating the answers as is done in many other computers. Division is carried out by repeated subtraction and addition process without restoration of the sign of the numerator. This makes it possible to develop a digit in the quotient each two word times so that a single precision quotient may be obtained in 56 word times. As in other computer, it is required that the denominator be greater than half the numerator before the division process is started. A double precision quotient may be obtained by repeating the division command with no further manipulation in between.

Operation Times

The time for addition and subtraction operations depends upon access to the memory. If minimum access coding could be fully utilized, it has been mentioned above that an addition may be performed in as little as 540 microseconds, counting the time for picking up the next command. After the operands have been obtained, a single length multiplication or division may be performed in half a drum revolution, which is approximately 15 milliseconds. If the operands are picked up from the fast access memory, and the commands are placed appropriately the complete time for a multiplication or division will not be more than 16 milliseconds.

Conditional Transfer of Control

A very flexible conditional transfer of control has been designed into the computer. The conditional transfer can be made to depend upon a number of different situations. In parts of the quick access memory there are logical facilities that give logical products and logical addition. These may be used in conjunction with the conditional transfer control to make it depend upon the presence of a digit in one number or another number. For example, conditional transfer of control may be made to depend upon the sign of the number in the accumulator, upon the sign of the number in the two word accumulator, or upon the presence of information in any particular word position in the memory, or even the presence of certain digits in the parts of the memory. The effect of a conditional transfer is to cause the next command to be one position later than usual in line 0.

Shift

There are shift commands to multiply effectively numbers by powers of 2. It is possible to multiply a number by any power of 2 between +54 and -54. When numbers are shifted, a counting process takes place in the accumulator, which makes it possible to keep track of scale factors easily, and later on to reshift automatically numbers into the appropriate position. There is also a normalize command which will shift numbers until they lie between 1/2 and 1 in size when the binary point is considered to be at the beginning of the single or double length number. During this process of normalization, counting takes place in the accumulator so that there is a record of how far the number had to be shifted. This particular command makes it easy to carry out floating point operations in this computer.

The Input and Output Circuitry

The standard version of the computer has a typewriter, a photo-electric tape reader, and a mechanical tape punch as input and output equipment. As an accessory, a magnetic tape unit will be available, which may be used for auxiliary storage or input and output purposes. Also available as an auxiliary equipment is circuitry which will permit punch cards to be used as input and output medium.

A very important feature of the input and output circuitry is the ability for the computer to carry on computation while input and output is in process. Generally, output takes place by placing the information to be sent out into memory line 19 and starting the output device. Input fills line 19 with new information. The appropriate input or output process may be started by execution of a command in the computer. Thereafter, the computer may proceed with its program carrying out its own computation doing any operations that do not refer to line 19. At any point in the computation the input and output circuits may be queried by execution of a command to find out if that step in the input or output process is complete. If not complete, at the programmers option, computation may be continued or the computer may wait until the input and output circuits are ready. This method of inter-lock prevents any trouble from early transfers to or from line 19 before the input or output process is complete. The speed of the typewriter is approximately 10 characters per second, and of the mechanical tape punch is approximately 15 characters per second. The speed of the photo-reader is approximately 200 characters per second. The magnetic tape will operate at 350 characters per second. These are relatively modest speeds as far as input and output equipment is concerned, but the expectation is that with such modest speeds correspondingly more reliable operation over much longer periods of time may be had.

Manual Control

Manual control of the computer is available from keys and switches on the typewriter. In general, the computer may be operated at full speed, it may halt due to break points, in which case the operator may cause the computer to start

again, or the computer may be operated in a 1 cycle mode, wherein for each operation of the key on the typewriter the computer carries out the next following command. Such a facility will be used in checking out new programs. When operating in the 1 cycle mode other keys in the typewriter may cause the information in the accumulator to be printed or may cause the next command to be transferred to the accumulator and be printed. It is also possible to type new information into the accumulator, and in particular to type new commands into the computer and obey them. To facilitate this last operation, a marked place operation is available. Upon operation of a key on the typewriter, the information which determines location of the next command is stored in the memory and the operator may go on and obey a sequence of commands from the accumulator or from another location in the memory of the computer, and at some later time return to the proper place in the main program as determined by the mark place operation. This is another facility that is expected to be particularly useful in code checking.

Physical Design

All the discussions so far have been in terms of the logical design of the computer. Consider now the electronic design. It has been mentioned that it occupies the space of two filing cabinets. The lower portion of the cabinet contains the power supplies, the magnetic drum, and ventilating equipment. The upper part has two gates which swing open. These gates carry all the electronic circuitry in the form of printed circuit plug-in packages. The photo-electric tape reader is on the front of this cabinet. Probably the computer will usually be set at the end of a desk with a typewriter being located on the desk and connected to the computer with a cable. Neon lights on the computer cabinet itself indicate the state of various flip-flops in the computer. The unit uses approximately 3 kw of power and has forced air ventilation. For installation in offices where the range in temperature is such that this extra amount of heat cannot be tolerated, a special top will be supplied on the computer which makes it possible to connect a ventilating duct to exhaust the hot air outside the room. There are nine kinds of plug-in units used in the computer. These units are denumerated and their functions briefly explained below.

The flip-flop is schematically represented in Figure 1. Note that the circuit is cathode biased to assure satisfactory operation over a wide range of tube characteristics. The flip-flop proper is isolated from load current fluctuations by means of the series resistors R_1 and the germanium diode clamps. The input circuit composed of the resistors R, the capacitors C, and associated germanium diodes provide for a given side of the flip-flop to be triggered to the non-conducting state by the negative-going clock pulse CP if the corresponding input terminal A or B is at the upper gate potential. The networks RC serve to give a brief signal delay so that a single-phase clock system is used. This method of diode triggering has the advantage that the flip-flop operating point is independent of the back resistance of the triggering diode.

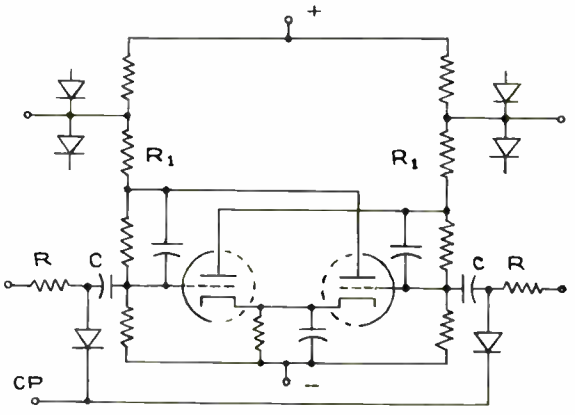


Fig. 1

The buffer-inverter is a Schmidt-trigger type of circuit employing the same circuit constants and output circuit as does the flip-flop. However, the input to one grid is from the plate of a single triode amplifier. Thus, for example, if the input signal to the grid of this amplifier is high, one clamped output will be at the upper clamp level and the other output will be at the lower clamp level. The purpose of this circuit is then two-fold. It restores signal levels to standard, and it gives the logical complement or inverse of the input signal.

The cathode follower circuit is conventional and serves two functions. The first is simply to increase the available current. The second is as a common cathode mixer or "or" gate.

The main computing network is composed of the above three tube packages and the diode packages of which there are four types. The first of these is a clamp package which actually contains all clamping diodes such as those shown in the flip-flop schematic Figure 1.

There are in addition three different configurations of diodes and resistors which are used to realize the logical gate network of the computer. These gates are conventional DC circuits by which the logical "and" and "or" are realized.

The two remaining plug-in units are the magnetic drum reading and writing amplifiers. The drum memory system used employs separate reading and writing heads on each channel along with an associated permanent magnet erasing head. A return-to-zero recording system is used in which the write-pulse to represent each "one" has a duration of about 1.5 microseconds. A write amplifier is composed of a cathode follower which operates an "and" gate to pass a standard positive write pulse to a pentode which is normally biased beyond plate current cut off.

The read amplifier has its first stage located on the pre-amplifier chassis which is near to the drum itself. The pre-amplifier for each channel consists of a triode class A amplifier followed by a cathode follower to drive the cable to the read amplifier. The input to the read amplifier proper is transformer coupled. In the read amplifier a pulse is formed from the signal to set a flip-flop which again has the same component values as above. The read flip-flop is set in this manner by each "one" signal and reset each clock period by the clock pulse. In this manner an economical memory system is obtained in which there exists adequate margin for reliability. The amplifier itself is stabilized against tube aging by degenerative feed-back.

In order to minimize faulty operation due to defective components; vacuum tubes, germanium diodes, resistors, and capacitors are used conservatively with most components having their voltage, current, or dissipation limited to half of the manufacturers rating. Vacuum tubes may deteriorate to one half their initial specifications, and germanium diodes may deteriorate by a factor of three without impairing computing accuracy. This conservative use of components coupled with the built-in marginal checking will help to minimize down time.

The mechanical design of the memory drum is novel. The individual heads which have both radial and tangential adjustment are small and entirely located on one side of the drum housing. The other side of the housing has a removable dust cover. With this cover removed, it is possible to inspect, clean, or even replace the drum coating without disturbing the head adjustment. In fact, it is never necessary to disassemble the memory, even if it becomes necessary to grind the drum surface.

A standard installation of a G-15 computer will include a number of spare packages of each sort so that normal breakdown of the computer may be repaired by simply replacing the appropriate plug-in unit. It might be well to mention here that due to the multiciplicy of lines which may serve as a source of commands, a relatively small fraction of the computer needs to be operating in order to run test routines, so that normal expectation is that most faults in the computer can be identified by a diagnostic sub-routine, and the appropriate packages causing the trouble may be replaced and the calculator will be operable again. Faulty plug-in packages may be repaired by the customer or may be returned to Bendix for repair. The general philosophy of design in the computer has been to use modest speeds and modest pulse packing to give maximum tolerances in the various aspects of the design. It is expected that this will pay off in substantial increase in reliability of operation.