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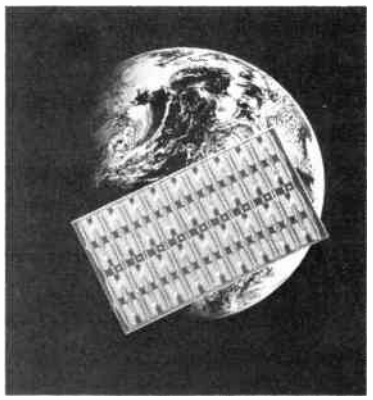

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MRF420	75 W	10 dB	12.5 V	211-02
MRF422	150 W	10 dB	28.0 V	211-04
MRF421	100 W	10 dB	12.5 V	211-04

heavyweight

from Motorola, the RF producer.

Circle No. 2 on Reader Service Card

the cover

Honeywell's multistation automatic test system typifies the trend to computer-controlled testing described in the article beginning on page 44. Shown is one station of several at the company's new product evaluation laboratory in Arlington Heights, Ill. Designed and built by Honeywell's Government and Aeronautical Products Div., the system checks functional modules of building-automation systems prior to production, and monitors production operations, too.

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IEEE spectrum SEPTEMBER VOLUME 11 ☐ NUMBER 9

spectral lines

Who gets published? Part III: Proceedings

The *Proceedings of the IEEE*, it should be remembered, is the offspring (some would say continuation) of the *Proceedings of the Institute of Radio Engineers*, a journal which, during the history of IRE, served as its core publication. Today, *Proceedings* retains many of the traditional characteristics of *Proceedings of the IRE*, yet differs in important ways. In particular, it is available to members by subscription (some 30 000 at present subscribe, and its readers represent all the Groups and Societies of IEEE, including those, like the Power Engineering Society, that were not constituents of IRE). During 1973, *Proceedings* published more than 1800 editorial pages, encompassing 144 papers and 225 technical letters.

As in the case of its predecessor, the aim of the *Proceedings* is to publish general-interest papers having technical depth. It differs from *Spectrum* in that articles are usually much longer, more detailed, contain all relevant mathematics, and are accompanied by extensive bibliographies. It attempts to avoid papers that would appeal narrowly to one Group or Society, and which would therefore be more appropriate for one of the *Transactions*.

A *Proceedings* issue presently appears in one of two formats: "regular" or "special." The Editor of the *Proceedings*, Robert Lucky of Bell Laboratories, distinguishes between the two as follows: "In the case of special issues, I appoint guest editors who have complete editorial control over the issues they handle. Topics and possible guest editors for these issues are suggested to me by the Editorial Board of the *Proceedings*. Once appointed an editor can obtain material for his special issue either through a special call for papers or through inviting particular papers from preselected authors. Both approaches have been used in the past. We have had completely invited special issues, and we have had those which were obtained entirely from contributed manuscripts. In either event, review procedures are entirely at the discretion of the guest editor. Regular issues consist both of invited papers and of contributed [not specifically solicited] papers. In the past, nearly all papers were contributed. Starting about six years ago, the supply of contributed papers was supplemented with invitations to selected authors to write tutorial-review papers on important subjects. In the last few years, these invited papers have constituted about half the contents of the journal."

In 1973, five special issues were published; thus far in 1974, six special issues have been published and one more is planned. In the case of regular issues, both the invited and contributed manuscripts are reviewed by a minimum of three reviewers expert in the field. For the purposes of our present discussion, we shall concentrate on regular issues, and, in particular, on contributed manuscripts.

Editor Lucky observes that the number of contributed papers in recent years has continually declined, due largely to the development of the individual *Transactions*. If that trend continues, the *Proceedings* could evolve into an all-invited journal. There is, of course, the question of whether this would be good or bad.

A serious problem cited by Dr. Lucky is the general misunderstanding of the role of *Proceedings* by prospective authors, so that most of the unsolicited manuscripts are much too specialized; many of them are promptly recommended for resubmission to an appropriate *Transactions*. On the other hand, the kind of paper that *Proceedings* is seeking (the authoritative tutorial/review) is not the kind that an author is apt to write "on speculation." It is, rather, the kind that warrants prior negotiation.

As a result, the *Proceedings* has set a new policy of soliciting proposals for tutorial-review articles. The policy enables a prospective author to send an outline of the contents of the proposed article, prior to actually generating the complete manuscript. He is encouraged to include a brief description of why the subject is of current interest, along with a few words about his own relationship to the field and his qualifications to write the paper. Such a proposal would be examined by the Editorial Board of the *Proceedings*, and, if approved, the author would be invited to prepare the paper. While the manuscript would, of course, still be required to undergo review, Dr. Lucky emphasizes that the author would be guaranteed that the *Proceedings* had a genuine interest in the topic, had no competing papers scheduled, and was prepared to publish the manuscript providing it survived the review process.

Donald Christiansen, Editor

Automatic test systems

Seven basic elements make up the ideal ATS; neglect of any one is an invitation to disaster

There is probably an automatic test system (ATS) in the future of almost every product designer and instrumentation engineer. For those engineers directly responsible for solving test and repair problems, such systems—particularly those built around computer data bases—are fast becoming an everyday necessity.

With modern electronic testing techniques now less than ten years old, it is not surprising that many engineers haven't yet had the opportunity to discover how automatic testing systems work and what they can do. While recognizing that the art of automatic circuit testing continues to develop rapidly—with new concepts and methods constantly being discovered—this article aims to provide a general survey of the field. Starting with the basic elements of automatic testing systems, the discussion covers the essentials of ATE hardware and software techniques, highlights some of the major problems and pitfalls involved in successful use of the systems, and points to the types of people and organizations that now play a key role in automatic testing.

Automatic testing—the basic elements

An automatic testing system consists of seven main elements (see Fig. 1):

1. Data base of circuit descriptions
2. Means of circuit simulation
3. Method of test generation
4. A language with which to command a piece of automatic test equipment to carry out tests and a library of programs in this language
5. Automatic test equipment (ATE)
6. A diagnostic (fault-locating) method
7. Some scheme for managing the mass of data

Not to consider all seven of these components in establishing an automatic testing system is to invite both frustration and financial loss. In fact, it is still not widely understood in the industry that the need is far greater for test systems than just test equipment.

For maximum efficiency, an enlightened manufacturer will apply a test system to products in one or all of the following: design verification, testing during manufacture, and diagnosis by a repair organization.

The data base

Although very recent products may be associated with a computer data base of circuit descriptions (e.g., bills of materials, wiring lists, pin loading requirements, printed board art masters, schematic diagrams, IC types, etc.), slightly older products may be documented either by manually retrievable means or in a form not readily available.

Undoubtedly, the processing of this data for purposes of computer simulation and test generation can become one of the most time consuming and tortuous tasks involved in the application of an ATS to a given product. It is still rare for this process to be automated to a significant degree—although a computer-readable data base makes this possible in principle. Therefore, one corollary for the manager or engineer convinced of the need to systematize is:

Know your data base and its relationship to your available means of simulation and test generation, and devise as efficient a means as possible of obtaining a simulatable model from the data base.

Currently, only a few large manufacturers—those with extensive design automation commitments—have completely grasped this lesson and applied it to new product lines.

Circuit simulation

To simulate a circuit you must have a model of the circuit—a problem that can be extremely nontrivial if the model is to be faithful both to the design intent and to the modes of circuit failure.

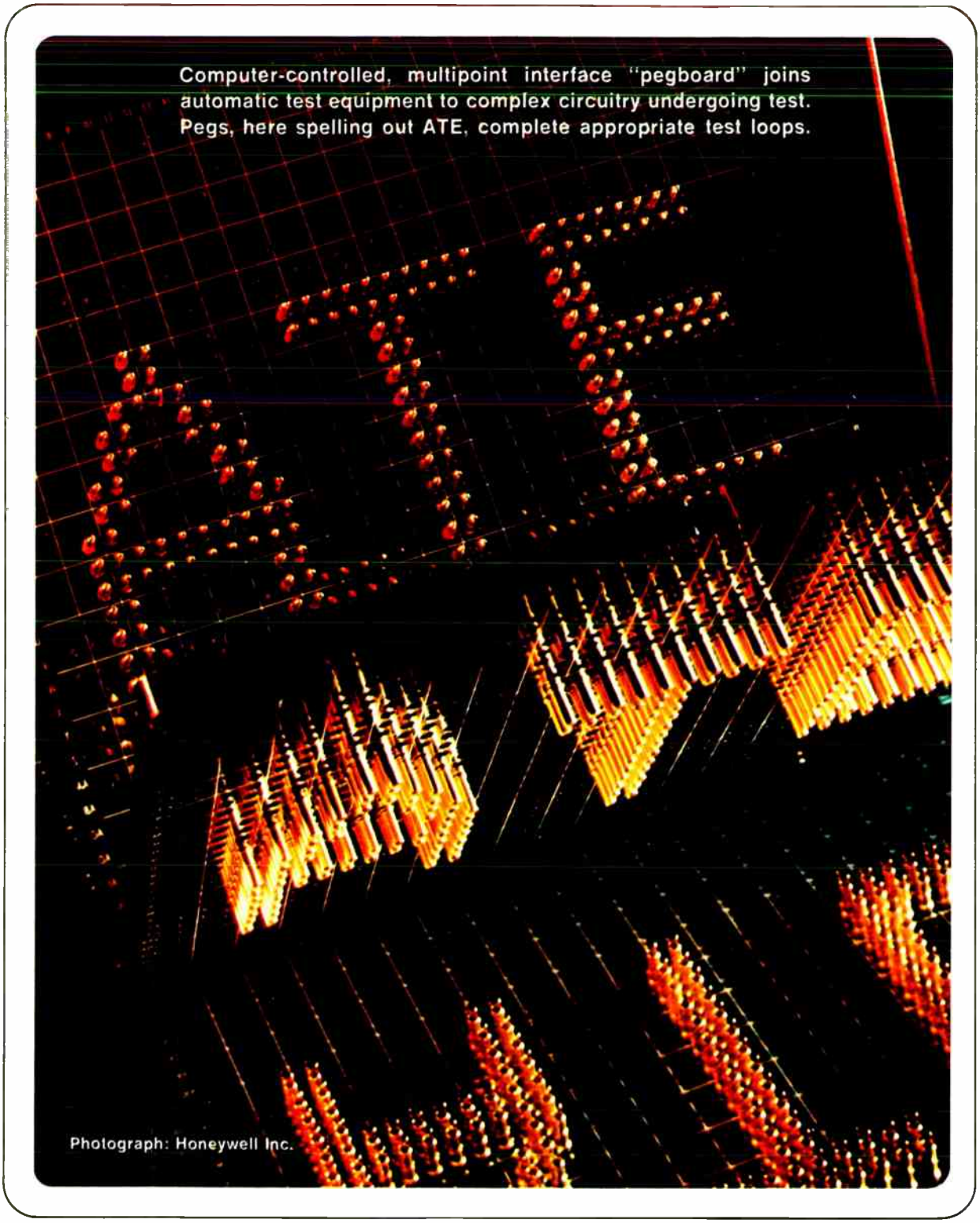
The best automated test systems are based on a tremendous one-time expenditure on software and modeling of small components from which products are constructed. In the average case, however, human input to the modeling of products is still needed.

In the worst case—and all test engineers have seen this happen—an engineer prepares a logic diagram that he assumes correct. He then traces input signals through the diagram by hand. If the circuit has any complexity, there is no hope of verifying the correctness of the model or generating a set of inputs that will test the circuit for a significant proportion of all possible faults. More and more frequently, computer simulation is becoming an absolute necessity.* Although a computer simulator may be designed for a specific product, the ideal simulator in an ATS should be applicable to a broad range of products.

If a simulator is to be widely utilizable, there must be a means of providing it with circuit models. In a fully automated test system, the model is automatically derived from wiring lists and a library of component models. More commonly, a circuit model is described to a simulator by means of a special circuit description language. These languages have syntaxes ranging from fixed position numerical codes to English-like formats.

Kilin To, R. E. Tulloss Western Electric

* Some will disagree with this contention on the grounds that there are some practical disadvantages to computer simulation. There are cases in which a test sequence can be built up by hand and a fault dictionary built empirically through experience with an ATE.



Computer-controlled, multipoint interface "pegboard" joins automatic test equipment to complex circuitry undergoing test. Pegs, here spelling out ATE, complete appropriate test loops.

Photograph: Honeywell Inc.

Creating the model to be described is, of course, the sticky point. For circuits composed of standard digital ICs, modeling can be greatly simplified. Engineers or technicians who can model mixed-technology circuits accurately and rapidly, however, are an asset to the company that employs them, for they are rare birds, indeed.

Simulators may fall into any of the following types:

1. Waveform network analysis
2. Gate-level simulation
3. Functional simulation
4. Layered simulation (a combination of types 1–3)

For design purposes, the *waveform analysis* approach may be almost a necessity. For TTL logic that has been in production for some time, *gate-level* simulation is common and useful. As the building block

components gain greater and greater functional complexity, however, the need for simulating their internal workings decreases and *functional* or *layered* simulation becomes more desirable.

Simulation of a fault-free model enables the engineer to check that model against the behavior of the actual product—model validation. The problem becomes one of obtaining a set of inputs that will distinguish good products from failing ones (fault detection) and, if economically feasible, will provide a sufficiently large set of stimuli to allow for better fault-location resolution in the failing products.

Test generation

Although "test generation" generally implies the preparation of tests for digital logic, some analog test generation methods have recently emerged. Of course, complete testing of a circuit board may require the measurement of some analog parameters, but automatic generation of tests for these parameters is extremely unusual today. The general procedure is to separate analog and digital testing, even though they may both be accomplished by a single test program.

A number of algorithms and heuristic methods exist for the generation of test sequences that are regarded as "complete"—i.e., the test sequence can be shown to detect the presence of any single, stuck-at-0/1-type (also called stuck-at-type) fault in a given circuit by the use of a fault simulator. But in highly sequential circuits, if complete coverage of all detectable faults is desired, an engineer will more likely than not find it necessary to finish off the test generation by hand even when a computerized test generation algorithm is available.

Command language and program library

A test command language is a programming language that directs an ATE through the testing of any member of a given class of products. Most manufacturers of ATE provide a test command language and compiler with their hardware; but the level of the language varies from rudimentary mnemonics to English-like languages. Certainly test command languages like general-purpose programming languages are most useful if they can be easily understood.

From the test system's point of view, it is always desirable to have the maximum information about a product available with minimum effort. Hence, a

Problems, pitfalls, and pluses of an automatic test system

The problems encountered in managing a test system depend, of course, on the system's sophistication (see Box, pp. 50–51). At one extreme, the "strictly manual" test system (if adequate for the product) requires the least effort in the preparation of test specifications; however, it takes highly skilled technicians to troubleshoot, locate, replace, and repair the faulty components. Because human judgment is involved both in the preparation of test specifications and in troubleshooting, the process is slow and prone to error. Eventually, the quality of the tested products suffers or falls into question. On the other hand, a highly skilled technician's knowledge of the product under test may compensate, at times, for inadequately written test specifications.

At the other extreme, a highly automated test system has problems of its own that managers have come to recognize only recently. Since automatic test systems are more and more common today and definitely the trend of the future, it is worthwhile to point out to those who will manage them possible problem areas and pitfalls.

Lack of system concepts: Since ATE is the tangible part of an automatic test system, potential users are often preoccupied with it to the extent that insufficient effort is spent on the rest of the system, with total performance affected for the worse.

An ATS is far more than the hardware involved. Off-line modeling, simulation, and fault analysis are all indispensable to the system and should not be taken lightly. Before any other work has started, the ATS manager must plan where and by what personnel each of the steps in a test system is supposed to be handled. An example of mismatch in design would be a system where the ATE is fitted with probes that are never used because no probing instructions are provided by the off-line test command program generator.

Using a software simulator: The circuit to be simulated may have basic building blocks that are not readily available among the simulator's circuit description primitives (basic simulator elements). Difficulties often arise in trying to describe to the simulator the circuit with a limited set of modeling primitives; the description must perform functionally like the physical circuit in both fault-free and faulty conditions.

To lessen the consequences of not having the right primitives, some simulators provide macro facilities or utilize truth-table descriptions of a circuit's basic building blocks. When a data base of basic circuit building blocks is lacking, the time it takes to describe some circuits in the simulator's circuit description language is long, with one man-month per circuit not uncommon.

Modeling limitations of fault simulation: Most digital simulators inject only single faults of the stuck-at-0/1 type. The test sequence previously verified to be complete by the fault simulator may not detect some actual faults in the circuits that do not fall within the set of faults known to the fault simulator. The frequency of occurrence of these nonsimulated faults obviously affects the usefulness of the test sequence, which should be validated by testing actual circuits on an ATE before production testing.

Test program validation: The processes of circuit modeling, test generation, and simulation are prone to errors caused by human oversight and too much idealization of real-life circuit parameters. ATE hardware limitations, as well, necessitate that the test program, once written, be carefully validated before release to production testing; this is accomplished by actually running it with sample circuits in the ATE.

If the system also provides automatic diagnosis, this process becomes even more important. In such a case, the validation would have to include the insertion of real faults into the sample circuits in order to check that they are diagnosed correctly—a tedious and time-consuming job. Some ATE vendors are attacking this problem, and there are now commercially available ATEs that can automatically insert physical faults on the pins of IC DIPs (dual in-line packets) through built-in relays.

Wasting computer time: Because a fault simulator is available to verify the completeness of test sequences, the test engineer is not motivated to obtain short, complete test sequences. This increases expenses incurred in computer simulation time, and extends ATE test time for a single unit.

System cost: Most first-time users of an ATS have the misconception that the cost of the ATE is the cost of the entire system. (This is equivalent to saying that the cost of running a computer system is equal to the cost of the com-

high-level test command language (preferably with sophisticated macro capability and one that allows in-line comments) has the distinct advantage that, for a given product, a carefully written and documented test program in such a language can serve as a company-wide test specification—even to locations that may test the same product manually, semiautomatically, or automatically on different hardware. The confusion that can be saved by such care in writing the test program cannot be overemphasized.

ATE

Automatic test equipment appears in a variety of species, ranging from comparators driven by paper tape, to systems composed of sensing devices directed by a dedicated minicomputer.

The direction now being taken by industrial test engineers is toward more sophisticated ATEs with a wide range of capabilities that can be applied to a number of product lines with minimal reconfiguration. This type of equipment is becoming more and more suitable for testing systems that have minimum human intervention between circuit design and test command program generation.

The ideal ATE has sufficient capability so that its influence on modeling and simulation efforts can be either minimized or clearly and concisely catalogued for reference. It should allow the use of a high-level programming language, for which a compiler must be readily accessible. If economically necessary, its software package should contain an adequate fault-locating routine to speed up repair and if it does not, then the software should be designed so that addition of such a routine is a simple matter.

The diagnostic method

Once a faulty circuit is detected, the next step is to locate the fault within the circuit. The words "fault location," "fault isolation," and "fault diagnosis" are synonyms. We shall briefly discuss three different ATE approaches to fault location:

1. Fault-location capabilities can be implicitly written into the program that directs the ATE sending and receiving signals. Such a test consists of comparisons of the actual and desired responses. If the network is fault free, then the test program will follow the "go" path to a terminal printout (or display) that indicates "no trouble found."

puter hardware.) It often comes as a shock to the novice that the test command programs and related software of the ATS cost as much, if not more, than the ATE itself.

ATS overenthusiasm: Some people are so attracted by the sophisticated capabilities of ATS that they immediately want to replace their existing test procedure. Old test procedures need not always be replaced if they are doing the job properly and economically.

Maintenance problems: The maintenance of an ATE requires specialized personnel that most existing shops do not have, and implies a knowledge about computers and interaction with the maintenance crews of a number of vendors. Building and training such a staff is often costly and time consuming, but it is inevitable.

The all-purpose ATE: Subconsciously, people believe that an ATE can be easily programmed to test product lines other than the one the machine was purchased to test. Unless other product lines were taken into consideration during the planning stage of the ATS, preparing the ATE for broader testing may not be easy at all. Often it is an impossibility.

Words like "universality" and "modularity"—loosely used to describe ATE—can be more meaningful if they are interpreted as: "This ATE is universal enough to test a small class of products (not any product)," or "This language is universal enough that a written test command program will run any configuration of this ATE as long as it has the same or more capabilities than the standard configuration." A modular ATE is one that has a repertoire of software drivers and hardware instruments that can be reconfigured for application to a particular product or set of products.

Engineering changes: Engineering changes on the product under test often affect the test command program, diagnosis, etc. Hence, a procedure must be worked out to update the ATS quickly in order to cope with these modifications. This often means some changes in the test program—another reason to have a test command language that is easy for the test engineer to understand.

Designing testable circuits: Some circuits are hard to test because they are designed by well-intentioned design engineers using tricks of the trade. Such circuits are poorly laid out with few access points or with some components difficult to remove and replace. The problem is that people who are in charge of testing and repair normally have a hard time getting a more testable circuit from the design group. Unfortunately, this situation will remain until we have established a theory of testable circuit design. One remedy is to demand the design engineer also to derive and validate the test sequence for his circuits.

Buying the ATE first: Sometimes the choice of the ATE inadvertently compromises or limits the choice of other levels of the test system; comparators and pattern generators are good examples of this, and we have sought to describe their merits elsewhere in this article.

Misunderstanding simulation: At this very moment, a number of testing engineers are engaged in futile attempts to write comprehensive test programs for highly sequential digital circuits. In the majority of these cases, the engineers are not fully aware that any hope of obtaining a test sequence based on hand calculations would require the commitment of many unborn generations. There are many circuits with such large numbers of inputs and outputs and significant sequential depth that they require more than 2^{100} calculations simply to verify that a test sequence is complete for stuck-at-0/1-type faults!

Save now—pay dearly later: Some ideas intended to reduce manufacturing cost unintentionally increase the cost of testing and repair. Substituting stock components or material may alter the life of the components and increase the incidence of testing and repairing the circuit.

Pay now—save later: Although putting extra test points in a circuit increases the cost of manufacturing, the savings realized in testing and repairing may be large enough to be well worth it.

Quality control: In many cases, most of the data that is available during testing are not collected because to do so would slow down the testing process. In the manual mode of testing, to gather sample data, special studies have to be conducted. These studies are not only disruptive to the testing process, but they are costly as well. Fortunately, in a computer-controlled ATS, data collection can be done by the computer and the extra cost is mostly a one-time expenditure for some additional software.

K. T. and R. E. T.

Such an approach to fault location often requires tedious manual coding and debugging of the test command program and a "weaving in" of the fault-locating capability. Moreover, any future changes in the network under test, due to engineering updates or new issues of the same product, necessitate laborious recoding of the test command program. This entails efforts similar to implementing additional features into an intricately woven, previously coded computer program, the woes of which are well documented in software journals.

2. By using a fault simulator, a tabulation of failure symptoms vs. faults (often called a fault dictionary) can be derived. It is used in the following manner.

First, a sequence of tests is simulated on a circuit under test (CUT) and the actual responses of the CUT are recorded. If one or more of the responses is not equal to the corresponding response in the simulated fault-free circuit, then the circuit is faulty. A fault signature is calculated, which is composed of both the numbers of failing test steps and a faulty output list for each of the failing steps, although this information may be compacted by some hashing technique. A search for a matching signature in the fault dictionary will frequently yield the identifiers of the faulty modules.

3. To employ a dynamic on-line fault locator involves some complex on-line circuit tracing algorithms plus sophisticated off-line software aids. To do this, one takes the "good old test engineer's" own troubleshooting approach, in which the following pieces of information are normally available: (1) a complete sequence of tests and a set of corresponding responses for a fault-free circuit, and (2) the schematic diagram, and perhaps the logic diagram of the circuit, and a description of the boundaries of the replaceable modules the circuit contains.

The test engineer executes the given sequence of tests on the circuit, records the corresponding responses, and compares them with the given responses of the fault-free circuit. If a difference is noted, he applies his knowledge of electronics and traces through the schematic and/or logic diagram following one of two schemes:

Pessimist's method—Start with one of the faulty

Data management: computer-age need

The need for data management can be amply justified by the following case history, which—though hypothetical—parallels the experiences of many actual electronics firms with which the authors and the reader are familiar:

The XYZ Company tests 100 different circuit types with a multistation ATE. As in many manufacturing and repair center environments, available space is restricted and there is a logistics problem. For every circuit tested there is a 3–6-inch stack of computer printouts, schematics, a plug-in patch board, and a variety of fault-free sample boards, interface boards, and probe mats. In addition, there is a library of 15–20 magnetic disks containing test and diagnostic programs, with duplicates for each of the disks.

As if this were not enough, the test programs undergo frequent alterations (about 2–5 per month)—improvements required by design changes.

It is obvious that someone has to keep tabs on what is happening. Has the back-up pack for circuit *X* been updated? Where is circuit *Y*'s "gold-plated" good board? Disk *Z* has been clobbered, where is the back-up? Where is the circuit drawing for circuit *A*, for which an error in the patch-board wiring is suspected?

The job of data management is a big one requiring extensive familiarity not just with the ATE but with the entire automatic test system. We call the person handling this job the *data manager*, a position that is seldom assigned explicitly, but that falls by default on one or more test engineers who systematize logistics up to the point where most crises are averted. A written logistics plan is fairly rare under these circumstances, so temporary chaos can result when any of these *de facto* data managers leaves the company. It is not uncommon to find an updated test program put onto disk with the diagnostic programs of an earlier version or even a different circuit.

The job of effectively minimizing such errors is not an easy one, but would certainly be optimized by the increased use of data managers.

K. T. and R. E. T.

Wanted: more research

Without belaboring the research work of the past, we can broadly outline current trends in the field of electronic circuit testing. This does not mean that some of these problems have only recently appeared. It is just that they have always been known to be conceptually difficult to handle.

Most of the work done in *fault analysis* is in the digital circuit area. Much less effort has been expended on fault analysis of analog circuits, and even less on hybrid networks (circuits consisting of analog and digital subcircuits and relays). Since all these circuits abundantly coexist in the real world, why not develop test and repair techniques for all three areas?

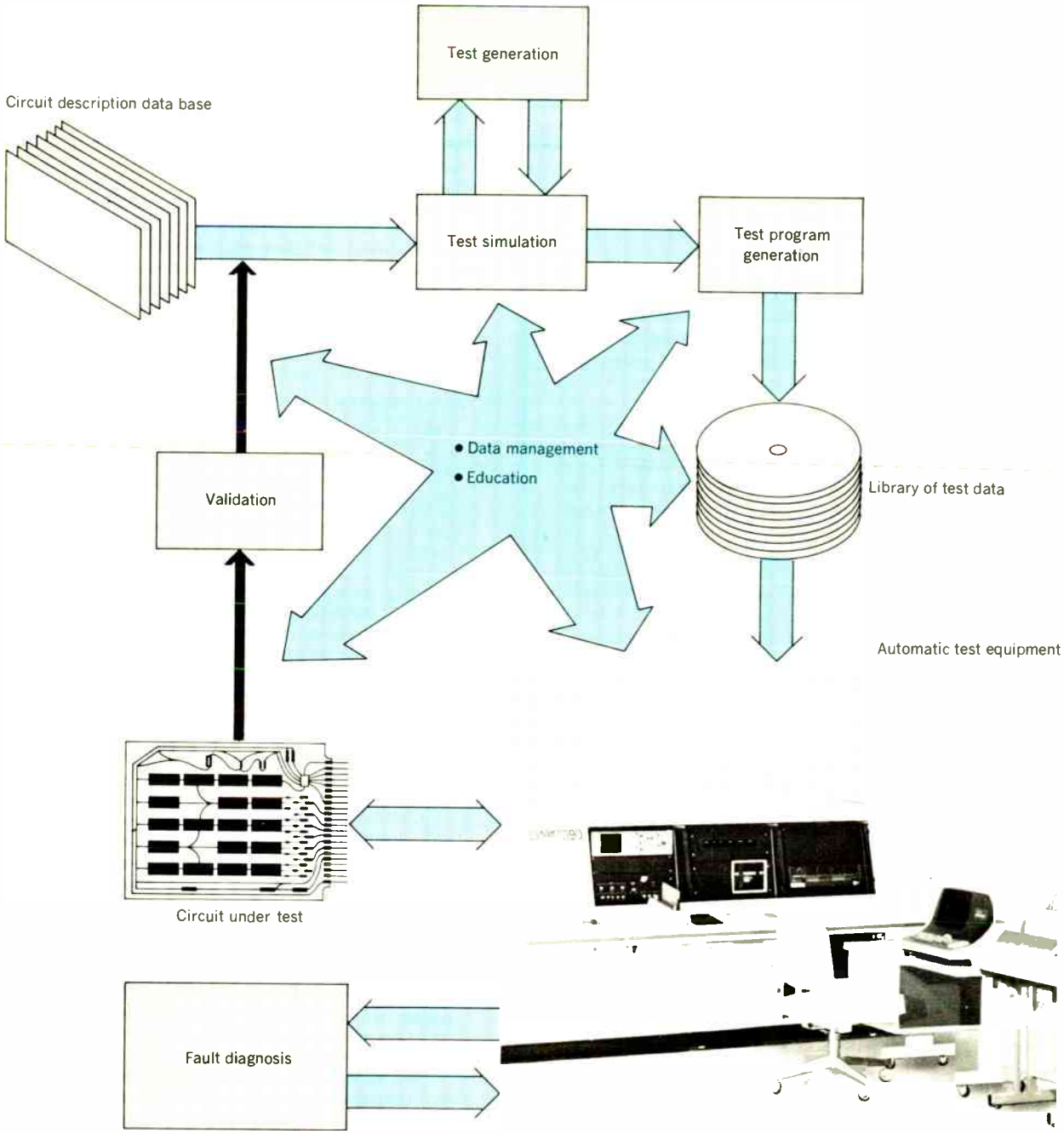
A lot of research work has been confined to classical stuck-at-0- and stuck-at-1-type faults. However, other types such as intermittent faults, pin shorts, and "wrong component" faults frequently occur. Recent articles have reported explorations in this direction.

Many studies in fault analysis have been entirely dependent on the "single-fault" assumption. Multiple faulting in combinational circuits has been researched in some detail, but multiple faulting in sequential circuits is an area that has not produced many applicable results.

Efficient algorithms for *generating tests*, while developed for combinational circuits, still take too much computation time for highly sequential circuits. In the case of analog circuits, automatic test generation has barely been mentioned in the literature. As discussed in the text, there is an important and necessary distinction between fault simulation and test generation.

Substantial time has been devoted to the analysis of the effects of faults on a circuit. Recently, work has appeared on synthesis—the principles of design—with the idea of simplifying testing problems by the allocation of test points, partitioning, packaging, etc. With such an improved design methodology, many testing economies can be effected.

K. T. and R. E. T.



[1] An automatic test system is much more than just the ATE hardware, which may cost as little as a quarter of the entire system. With large investments going into such "intangibles" as data processing and software, it is no wonder that the need is increasing for better data management and more informative testing education.

primary outputs, using perhaps the single-fault assumption, and see what subcircuit is electrically connected to this particular output. Then, using the operating principles of gates, deduce what gate could possibly cause such an output.

Optimist's method—Instead of starting with the faulty primary outputs, start with the correct outputs and say, "If this output is correct under this test input and with a given state of the circuit, then this gate and those gates must be fault free." Do this by checking off faults that cannot be present given the correct responses at the output pins for each test input. In the end, what is left will be a list of gates that cannot be logically deduced to be fault free.

Data management

A position of *data manager* (a person who coordinates necessary information for testing a particular

product) has become necessary to keep an orderly library of test programs and to cross-reference them with simulation models and the original circuit data base entries; in some cases, product samples may also be kept as standards.

The importance of this data manager cannot be overemphasized (see Box, page 48). Poor control here means that engineering changes will lead to chaos on the testing floor. Product changes—which result in modeling changes, new simulation and analysis data, new test generation, and new test command programs—all must be carried out in an efficient, orderly manner. In the majority of automatic testing applications, this data management position is never created; consequently, the system deteriorates over time because data becomes older and more irrelevant.

Who makes up the testing population?

The four major groups involved in testing are the academicians, the instrument manufacturers, the software houses, and the hard-pressed testing engineers. Unfortunately, these diverse groups often do not understand each other's jargon—especially at testing conferences—which can be an extremely frustrating experience.

The four groups can be defined by their interests, as described in the following sections.

The academicians

It appears that most articles published in professional journals on automatic testing are written either by university professors, graduate students, or persons from research and development centers. Their work consists mainly of test generation techniques, design of testable circuits, simulation, fault diagnosis, and failure tolerant systems. Well-known test generation methods include path sensitization, D algorithms, and Boolean difference techniques. To make problems more tractable, faults are assumed to be of the stuck-at-0 and stuck-at-1 type, although recently papers have started to explore the effects of other types of faults, such as intermittent faults.

Most research reported to date has concentrated on test generation for single faults; however, recent publications have begun to consider multiple faults. Unfortunately, most present test generation methods, while good for combinational circuits, are not easily adaptable to sequential networks—an area that is not too well understood.

Because they are more and more widely used and conceptually simpler to work with, digital circuits seem to attract the main efforts of automatic testing research. Digital circuits are composed of building blocks such as NANDs, NORs, flip-flops, etc., but many analog circuits are single (perhaps even unique) entities. A good example of the imbalance that exists in the automatic testing field is seen in the fact that work on test generation for analog circuitry is almost nonexistent (see Box, page 48).

The development of criteria for designing testable circuitry (again mainly digital) that the practicing engineer can readily use is still in its infancy. Although there is work being done on LSI (large-scale integration) cellular arrays and fail-safe machines, theories in these areas are still in their infancy and seldom used by practicing design engineers. Tech-

ATE—a hardware to go!

At the very heart of every automatic test system can be found a piece of test equipment. With interest in automatic testing stimulated by the necessities of maintaining today's highly complex electronics systems, the market is virtually exploding with all sorts of ATE hardware. Basically, however, the field can be narrowed down to either fixed program or variable stored program hardware. The advantages, problems, and solutions of the various approaches within these two ATE classes give some indication of the broad range of performances that can be expected from ATE systems.

Fixed program

The comparator approach ($1000–$30 000). Circuits under test (CUT) are inserted one at a time into the test equipment, and random signals are fed into the input pins. Signal values of the output pins of the CUT and, possibly, of some internal nodes are then compared with the values measured from the corresponding pins and nodes of a known-good circuit that is used as a reference. A board that is fault-free serves as the standard to which all CUT measured values are compared.

The advantages of the comparator approach are that there is basically no programming required (therefore no software overhead) and that the system is inexpensive to build. There are problems, however, which are:

1. It is not suitable for testing sequential circuits with no reset line, since the CUT normally powers up in a different internal state than that of the known-good circuit.
2. Because of the random inputs used as tests, fault coverage of the test is usually not complete and, in fact, fairly poor for deeply sequential circuits.
3. Since a known-good board (a board verified fault-free by some manual or functional method) is used as a standard for each of a number of different types of CUTs, and since at least one board of each type must be kept at each of the locations testing them, a high inventory of known-good boards must always be kept. Known-good boards or so-called "golden boards" also deteriorate with time.
4. Comparators have limited capabilities for connecting instruments to different pins of a CUT.

The following solutions can be used to overcome the problems encountered with comparator testing:

1. In a sequential circuit, a CUT plugged in and powered up could be in any state and probably is in a different state than the known-good circuit. If a test sequence is fed in, outputs will differ, and good circuits will not pass the test and be unnecessarily rejected. If a reset line is available, however, both circuit boards can be reset to the same state. Otherwise, a homing sequence (an input sequence to initialize the circuit to some known state) must be derived to serve as an initialization both of the CUT and of the standard good circuit before the actual test begins. Some comparators do not allow for this solution.
2. Random inputs normally can detect 30–60 percent of the faults of the CUT during the first few inputs. However, many more random inputs will be required in order to increase the fault coverage, and will involve an almost exhaustive trial and error process. For sequential circuits, this problem is further compounded by the fact that the order of the tests is also important. If a fault simulator is available, tests can be generated manually or by any known algo-

rithm (such as path sensitization, *D*-algorithm, or Boolean difference methods) and verified for completeness. Again, some comparators do not allow for this solution.

3. Known-good circuits do not necessarily have to be kept and used as standards. The values of good circuits can be predicted either by a fault simulator or from the actual measurement of a known-good circuit when the complete tests are fed in. These values can in turn be retained in hard copy form: paper tape, cards, etc. In this way, there is no fear of known-good circuit deterioration.

4. A limited amount of switching can be incorporated to move some instruments from pin to pin.

The pattern generator approach ($500–$15 000). The pattern-generator concept of automatic testing involves applying a test vector to the input pins of a known-good board and recording its output vectors or making a count on the number of transitions from 1 to 0 and from 0 to 1 for each output pin. Any circuit under test that does not have the same output vectors or transition counts on corresponding output pins is then concluded to be faulty. For fault location purposes, transition counts for internal nodes are also recorded. In order to avoid race conditions, one input pin is changed at a time, with Gray code, 1-out-of-n code, etc., normally used.

The advantages of the pattern generator approach include:

1. Because of the fixed test procedure, it is considerably less expensive than computerized testers and the associated software cost is nil.

2. Presumably the code generator can carry out tests very fast.

3. The test sequence is exhaustive if the circuit under test is combinational or if all of its flip-flops can be set/reset and sensed externally.

This testing technique has the following inherent deficiencies:

1. *Initialization problem:* Because combinational circuits do not have initialization problems, this method is more applicable to combinational circuits. However, sequential circuits may power-up in unknown states. Starting the CUT in a state different from the state in which the reference unit started at the time of the reference count will cause rejection of fault-free CUTs.

2. *Faulty circuits with correct transition counts:* If the heuristic method of keeping the output pin transition counts is used instead of recording all of the actually received output vectors, then there exist circuits such that if a fault is present, the transition count of the output pin is the same as the good circuit, except that the transitions occurred under different input combinations. In other words, the transition count is not unique to the good circuit, presenting the possibility of passing bad circuits.

3. *Incompleteness of test sequence:* Since a fixed pattern is used as a test sequence, it may not detect all possible faults for sequential circuits. Again, this may lead to passing bad circuits.

Solutions to the problems just described include:

1. A homing sequence to reset the CUT must be used for sequential circuits that have no reset line. This may be impossible in some pattern generators.

2. A fault simulator can be used to verify whether the transition count is unique to the good circuit. Although fault simulation is not usually thought of as useful in this fashion, it can be done easily.

3. The completeness of the fixed test pattern for a particular circuit can be verified—again by a fault simulator. Instead of using a fixed pattern generator, we can have a PROM (programmable read-only memory) as a pattern generator. A complete test sequence (produced and verified by a fault simulator) can be programmed into the PROM, which means building your own pattern generator or doing some careful shopping around.

With a complete test sequence, fault location can be obtained by executing the sequence again and again while tracing back from the bad output pin probing each stage and comparing with precalculated values until the good output is measured. The fault must then reside just after the good output.

Variable stored program

Computer-controlled test system approach ($50 000 and up and still rising). The computer-controlled test system is the most flexible and expensive of all ATEs. Test sequences are usually verified to be complete by simulator, and the faults are located by addressing a fault dictionary or an on-line fault locator.

The different organizations mentioned here affect the inherent speed of test execution. In the following descriptions, *SV* means send (input) vector, and *RV* means received (output) vector:

Single buffered SV, RV: In the following methods, the time required between one test and the next is bounded by the memory cycle time. The time required to shift the test sequence into the send vector buffer is proportional to $W(SV)/W(BUS)$, where $W(SV)$ is the width of the send vector in number of bits and $W(BUS)$ is the width of the bus from the computer to the send vector buffer: parallel shifting of the test sequence can be achieved by addressing the bits in a particular bus width. Usually, the test sequence does not change in too many bits from one test to the next. Therefore, the changed bit can be selectively addressed. The speed will be the number of changes multiplied by memory cycle time plus the time required to send back the *RV*. Some cycle stealing can be achieved; however, time is essentially bounded by memory cycle time.

Fully buffered SV, RV: Instead of loading the *SV* and taking up the *RV* one at a time, a multiple buffer on both the *SV* and the *RV* can be used. The computer will send out complete test sequences into the buffer, then start execution of the test at the highest speed determined by a local clock to the full buffer. Received vectors are stored in the RV multiple buffer.

Flexibility is the strong point of computer-controlled test equipment. This is inherent because (1) stored program control is used, (2) the switching system routes the instrument connections, (3) any data processing needed can be performed by using the existing computer, (4) there is a wide selection of vendors from whom to select the test equipment building blocks (although most commercial ATE manufacturers prefer that core instruments be their own), and (5) there is an expandable capability through addition or deletion of software or hardware building blocks.

The management problem of operating and maintaining such a complicated test system is enormous and not unlike managing a computer center. It is here that the job of data manager will be especially needed (see Box, page 48).

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niques have been explored to improve the speed of fault analysis by dealing with classes of faults as units. For fault location purposes, fault tables and related methods are also being researched and used in many locations.

The instrument manufacturer

Instrument manufacturers—who make and sell automatic test equipment—are becoming increasingly involved in the implementation of high-level test command languages and on-line fault simulation and location methods. Hardware organization schemes seem to be as varied as the companies making ATEs themselves. ATE hardware can be conceptually divided into two basic classes: those with fixed programs, and those with variable stored programs. Of course, one can always find a combination or variation of these two configurations. (It should be remembered that ATE of either type may or may not be controlled by a general-purpose computer.)

As an aid to the reader's understanding of automatic testing, each of the two basic automatic test equipment types is examined in the box on pp. 50–51, along with potential solutions to some of their inherent problems.

The software houses

The software service houses that are in the testing business are often set up by people who have developed fault simulation software either at a university or in the design automation department of a large corporation. They provide such services as test generation, fault simulation, translation of test inputs into the test command language of the customer's ATE, and fault dictionary preparation; mainly for digital circuits. The fee normally charged for these services usually depends upon the percentage of complete fault coverage required and the complexity of the circuit to be tested.

As a rule, software vendors provide single-fault simulation of the stuck-at-0/1 type in digital circuits, with an occasional timing fault analysis capability. The most commonly used commercial ICs (integrated circuits) are sometimes already modeled in a data base; hence a circuit board can often be described easily to the simulator just by describing the wiring between the previously modeled IC building blocks. The fault diagnosis information that is provided is normally in a fault dictionary format. These dictionaries may be organized to disclose at which test steps and at what output terminals a given fault is detected, and they may even give the expected logic values of each IC terminal, allowing for the possibility of using IC clips to locate bad ICs.

This segment of the electronic testing industry is just beginning to flourish and the quality of software service varies greatly from vendor to vendor. However, corporations that have large R&D budgets and manufacturers of the more expensive automatic test systems (ATS) are attempting to fill this gap by providing their own fault simulation packages.

The test engineer

Because testing has become a rather specialized field with its own "in" jargon, most engineers who are confronted with a testing assignment may not be able to assess the entire testing problem. The problem is compounded further by the nonexistence of a unified body of knowledge in the form of tutorial texts on automatic testing; hence the engineer must wade through voluminous and not so easily digested technical journals before finding something that can be readily applied. The engineer's most frequent compromise, therefore, is to take what is available commercially (after an inexhaustive study of the field) and tailor whatever he buys to fit the product that is to be tested. As a result, there is a tendency to buy ATE haphazardly or build the whole ATS from scratch with great expenditure of time and money.

The eighth component

To obtain a truly successful ATS, an eighth component is required. We think the proper name for it is *education:* (1) self-education, planning, preparation of detailed specifications unifying off-line software, on-line software, hardware, and human processing; (2) education of potential ATS users as to the significance of real needs and the meaning of a system approach; and (3) education of managers regarding the necessity for both better testing and the complex system required to perform it, and the savings that can be expected in spite of the initial cost.

The engineer or manager committed to introducing an ATS will be faced again and again with the need to explain that his system is something much more elaborate than just hardware. Hardware is central to an ATS; but though it is more tangible than software and human elements, it is only a single component in a system requiring much more in order to be coherent and operational. Hence, the successful ATS man is an educator who must constantly and lucidly justify spending one, two, or three times his hardware costs on the intangible information processing that will make the hardware more than merely a dust collector.

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Get to know op amps; use a curve tracer

For the out of the ordinary application, it is not surprising to find op amp spec sheets wanting

Working with operational amplifiers often requires no more information about their characteristics than is provided in manufacturers' spec sheets. But under nontypical conditions, such as use of a +5-volt and a −5-volt power supply instead of the standard ±15 volts, most spec sheets are inadequate. In such cases, a curve tracer is a valuable tool for determining what to expect from the op amp. The instrument is also useful for verifying op-amp manufacturers' claims under standard conditions.

The reason that op amp spec sheets don't always give sufficient information (except, perhaps, for the more costly op amps), is that it is impractical to characterize the devices in ways that only a few customers might find useful. To verify such characteristics means added production costs.

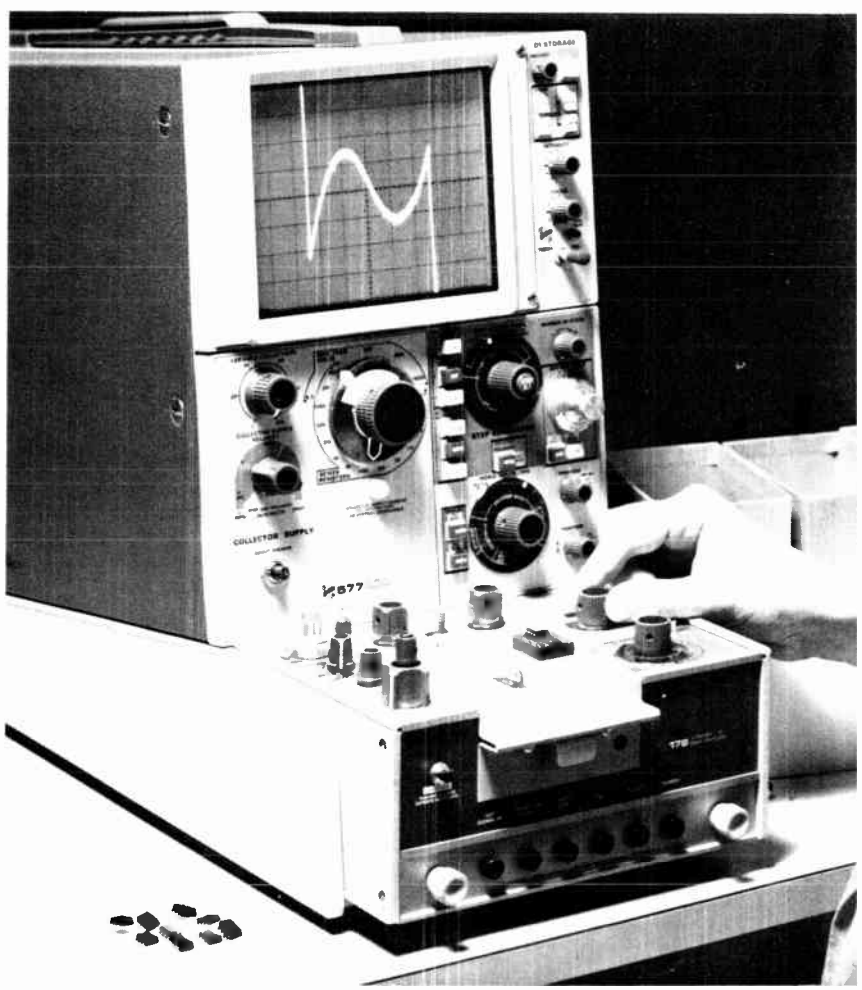
Point-to-point op amp testers

Production testing of op amps—as is the case with other high-volume components—is usually done with automatic testers that separate most bad op amps from the good ones. These testers make point-to-point measurements of key parameters in a fairly rapid sequence. For example, open-loop gain may be measured by applying an input voltage that causes the output to be +10 volts, measuring that input voltage, changing the input voltage so that the output is −10 volts, measuring the new input voltage, subtracting the lower input voltage from the higher one, and dividing that number into 20 (the output voltage swing). By this procedure, the ratio of output voltage swing to input voltage swing is obtained. It is a point-to-point measurement since it is from the +10-volt to the −10-volt point. These two points can be identified easily in the gain curve produced by a curve tracer. Such a curve would have output voltage change plotted against input voltage change. The curve would show all the points between the +10-volt and −10-volt output levels. If desired, the curve can be made to extend past these levels into the saturation region, near ±15 volts.

Op amp curve tracing can be done on paper or on the screen of a cathode-ray tube—a storage CRT is needed because the open-loop 3-dB bandwidth of many op amps is so low that the curves must be plotted slowly.

Typical op amp curves that can be plotted with a curve tracer are listed in Table I and a functional block diagram for an op amp curve tracer is shown in Fig. 1. The functional block diagram changes somewhat depending upon what kind of curve is being traced. In Fig. 1, the configuration is that used for plotting offset, the voltage between inputs versus the output voltage. A similar configuration is used for plotting gain. The main difference, in this case, is that a dc voltage is produced internally and applied

The op amp curves in this article were taken using the Tektronix 577 curve tracer. It is converted from a transistor curve tracer to an op amp curve tracer by adding two interchangeable plug-on test fixtures. A single switch selects the type of curve to be displayed.



John Mulvey, Jack Millay Tektronix, Inc.

to point A in Fig. 1 to center the display automatically.

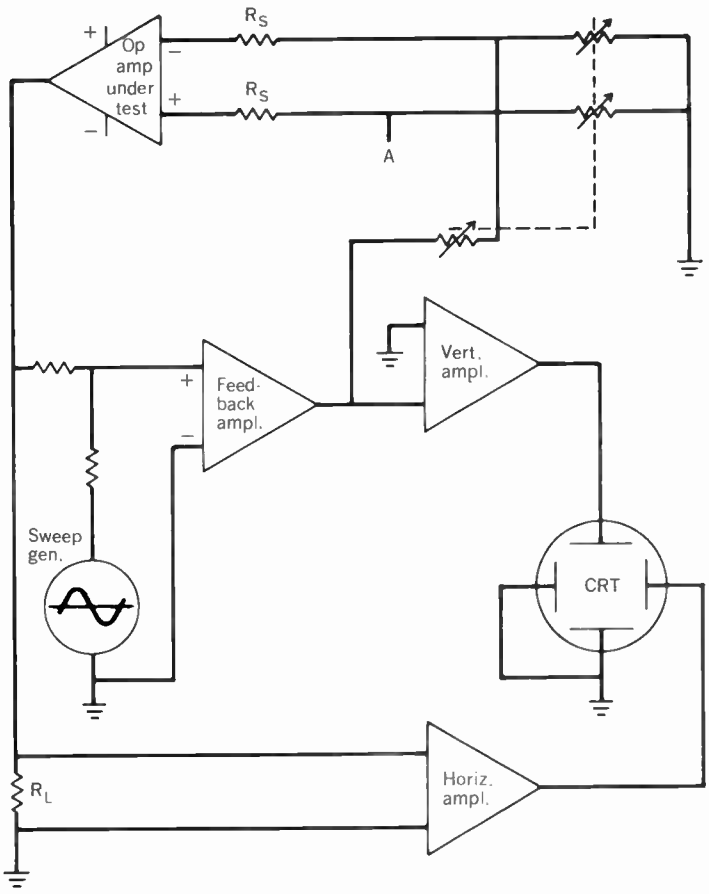
The op amp to be tested is made part of a feedback loop that tends to keep the positive input of the feedback amplifier constant (near ground potential) as the sine-wave sweep generator causes the positive input to change. The amplitude of the vertical deflection signal depends on the amplitude setting of the sweep signal, the ratio of the resistors between feedback and ground at the negative input of the op amp under test, and the open-loop gain of the op amp. Horizontal deflection is proportional to the output voltage of the op amp.

I. Op amp characteristic curves plotted on a curve tracer

Curve	Vertical (Y-Axis) Input	Horizontal (X-Axis) Input
Offset	Voltage between inputs	Voltage between output and ground
Gain	Voltage change between inputs	Voltage change between output and ground
CMRR*	Voltage change between inputs	Voltage between inputs and ground
+Input 1*	+Input bias current	Voltage between +input and ground
−Input 1*	−Input bias current	Voltage between −input and ground
+Supply 1	+Supply current	+Supply voltage
−Supply 1	−Supply current	−Supply voltage
+PSRR*	Voltage change between inputs	+Supply voltage
−PSRR*	Voltage change between inputs	−Supply voltage
±PSRR*	Voltage change between inputs	±Supply voltage (tracking)

* The output voltage is held constant at close to 0 volts for these common-mode rejection ratio (CMRR), input, and power supply rejection ratio (PSRR) curves.

[1] In the configuration shown, the op amp curve tracer is used for plotting offset, the voltage between inputs versus the output voltage.



Open-loop gain measurement

Figure 2 shows a nearly ideal gain curve. Input voltage is plotted vertically against output voltage plotted horizontally. Supply voltages are +15 and −15 volts and load resistance is 20 kilohms. The input signal (sweep) has enough amplitude to drive the output into saturation in both the plus and minus directions. Gain is equal to any output voltage change divided by the input voltage change that causes it. The slope of the curve at any point depicts the small-signal gain near that point. The more horizontal the slope, the greater the gain. In Fig. 2, the slope of the curve between −12 and +12 volts is fairly constant, signifying that large-signal gain is nearly equal to small-signal gain. The output can swing between −12 and +12 volts before saturation gets significant. Saturation occurs near the positive extreme at a slightly lower voltage than at the negative extreme. Scaling the horizontal and vertical distances between points 1 and 2 indicates that a 20-volt, peak-to-peak output signal (−10 to +10 volts) was caused by a change of slightly less than 0.10 mV between the two inputs. Gain, therefore, would be slightly higher than 20 divided by 0.1×10^{-3}, or slightly more than 200 000.

Figure 3 shows the effect on the gain curve for the same op amp when the load is 2000, instead of 20 000, ohms. Not only is the gain different from what it was in Fig. 2, it is radically different for different output signals. If the op amp were to be used in an open-loop configuration (an unlikely event), there would be severe distortion at the output.

In the curve of Fig. 3, thermal feedback accounts for the radical shape. With a 2000-ohm load, more power is delivered to the load than was the case with the 20 000-ohm load and, as a result, the op amp heats up more. Since the output transistors in the op amp generate most of the heat, there is a higher temperature rise at the power-transistor locations than elsewhere on the integrated circuit. For slowly changing output voltages, the position of the hottest spot shifts, depending upon whether the output is positive or negative. Temperature gradients in an op amp affect its response in a manner that is dependent on the physical location of the different elements of the op amp. The curve, therefore, is characteristic of the layout of the op amp, and will vary considerably from manufacturer to manufacturer.

If the op amp output voltage swings between 0 and −5 volts (points 3 and 4 in Fig. 3), the voltage between inputs will have changed by 140 μV (the vertical distance between points 3 and 4). Gain is 5 volts divided by 140 μV, or 36 000. The minimum large-signal gain spec for this particular op amp with a 2000-ohm load is 70 000.

When the output of the op amp swings from 0 to +5 volts, the voltage between inputs will have changed by 120 μV for a gain of 42 000. The change in

direction of the slope of the transfer function for output signals between 0 and −5 volts, compared to output signals between 0 and +5 volts, is important. If the op amp is placed in a closed-loop configuration where a gain of 1000 would result in an ideal op amp, the gain will be high by about three percent (1000 divided by 36 000) for 0- to −5-volt swings. And the gain would be low by about 2.5 percent (1000 divided by 42 000) for 0- to +5-volt swings.

This type of gain error cannot be compensated for by the usual technique of slightly altering the ratio of the feedback resistor to the input resistor. To do so would improve the gain error for some small signals but only at the expense of increasing the error for other small signals. A sine wave amplified by such an op amp would be compressed on one half-cycle and expanded on the other half-cycle.

The slope of an imaginary line between points 6 and 7 of Fig. 3 is nearly horizontal, signifying that gain is very high for a 20-volt, peak-to-peak output signal that varies between −10 and +10 volts. Since there is less than 20 μV difference between points 6 and 7 on the vertical scale, gain is greater than 1 000 000 (20 volts divided by 20 μV). It is interesting to speculate about a gain measurement made by a point-to-point tester that measures the input voltage swing necessary to obtain an output voltage swing from −10 to +10 volts across a 2000-ohm load. Such a specification is very common on data sheets. And it is misleading since it implies high gain when, in actuality, gain is very poor for small signals.

Figure 4 shows the gain curve for an op amp driving a 20 000-ohm load. The gain curve is linear but the slope is reversed from that in Fig. 2. This suggests that, in an open-loop configuration, a positive-going signal on the positive input to the op amp causes the output to be negative-going. It is interesting to note that a small amount of feedback to the negative input terminal will actually raise the op amp gain. Figure 5 shows the gain curve for the same op amp as was used for the curve in Fig. 4 with a 6.2-megohm resistor placed between the output and the negative input. Gain is raised to over one million. If the ratio of feedback resistance to input resistance is 100 000 to 1 on an op amp with an open-loop gain of 100 000, the gain would theoretically go to infinity if the slope of the gain curve was as shown in Fig. 4.

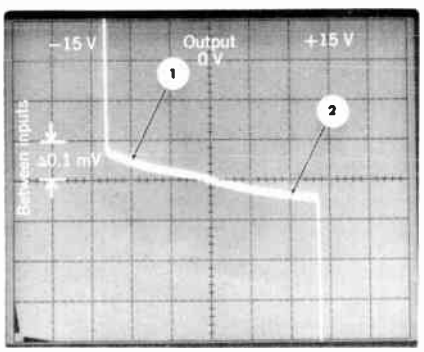
Figure 6 shows the gain characteristics of the same op amp as used for Figs. 4 and 5 except that the load was changed from 20 000 to 2000 ohms. The effects of thermal feedback can be contrasted with those shown in Fig. 3.

Note that with a 2000-ohm load there is still a reversal of slope. The open-loop gain measured between +10 and −10 volts (points 8 and 9) is over 500 000. Again that would be a deceptively high indication of gain for most output signals from this particular op amp.

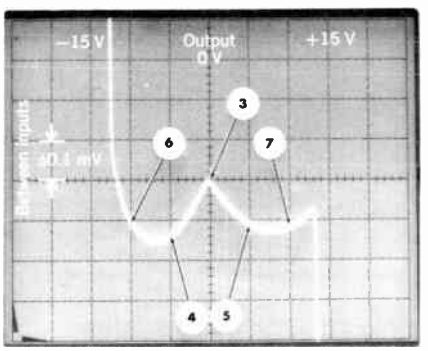
The nonlinearities of open-loop gain curves indicate the extent to which op amp gain will change for different size signals when used in a closed-loop configuration. In applications where extremely good gain linearity is important, one should look at curves, not just at two points. It is sometimes possible to buffer the output of op amps that won't drive low-impedance loads as linearly as necessary, once the curve tracer has been used to measure the actual characteristics of the op amp.

Input offset voltage

Offset voltage is an important parameter when an op amp is used to amplify small direct voltages. Figure 7 shows the curve for a type 741 op amp with 2.5 mV of positive offset voltage. The zero-volt reference level is placed at center screen. Point

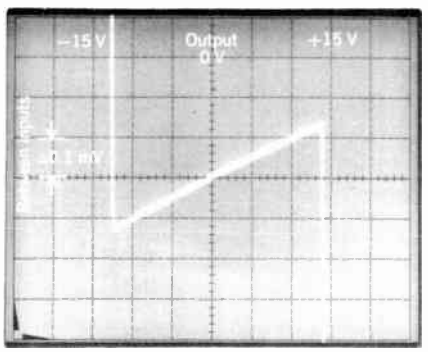


[2] Gain for a type 1456 op amp, ±15-volt supply, 20 000-ohm load.

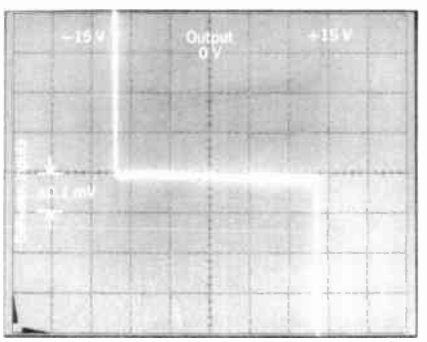


[3] Gain, type 1456 op amp, ±15-volt supply, 2000-ohm load.

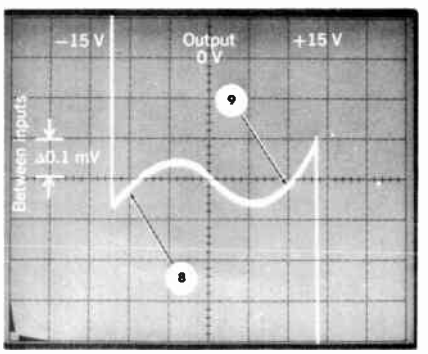
[4] Gain, type 741 op amp, ±15-volt supply, 20 000-ohm load.



[5] Gain with feedback, type 741 op amp, ±15-volt supply, 20 000-ohm load.



[6] Gain, type 741 op amp, ±15-volt supply, 2000-ohm load.



10 corresponds to zero output voltage.

Figure 8 shows the result of using the same op amp as was used for the curve in Fig. 7 but with negative offset voltage at room temperature (middle curve). The input offset voltage is about −0.35 mV compared to +2.5 mV for the op amp in Fig. 7.

To illustrate the effect of temperature gradients with an op amp, one was tested under three conditions. The top curve in Fig. 8 shows a great reduction in offset voltage as the tip of a small 15-watt soldering iron was held on one end of the dual-in-line package. The bottom curve was traced after putting the tip of the hot iron on the opposite end of the package. Regardless of how small the drift-versus-temperature spec may be, it is important to consider how well isolated the op amp will be from local sources of heat that can produce a difference in temperature across the integrated circuit.

Figure 9 shows curves for the same op amp as was used for the curves of Fig. 8 but tested for offset with three different pairs of supply voltages: ±15 volts, ±10 volts, and ±5 volts. Offset with the ±5-volt supply is shown to be less than half of that for the ±15-volt supply. An interesting effect that was not part of the test is apparent on the curves. The slope of the curves becomes more horizontal as the supply voltage is decreased. With ±5 volts, for example, the gain is much higher than for ±15 volts.

Offset null

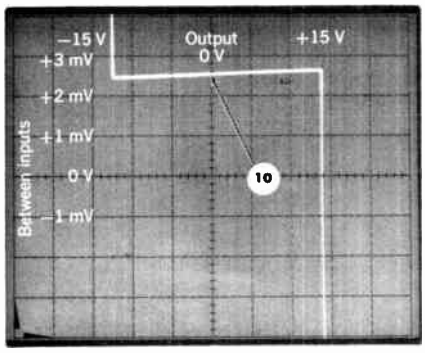
There is a pair of terminals on some op amps that is labeled "offset null." If a potentiometer is wired between these two points, with the slider of the pot connected to the positive voltage supply, adjustment of the pot permits the input offset voltage to be adjusted to zero. When this is done, however, other characteristics, such as common-mode rejection ratio or power supply rejection ratio, may suffer or be improved, or the offset null adjustments may be used to optimize a characteristic that needs to be better than what was specified.

Figure 10 shows three gain curves for one 741 op amp with the offset null adjustment set for highest gain (middle curve) and set at opposite extremes of the potentiometer for the other curves. Input offset bias was +15 mV at one extreme and −15 mV at the other.

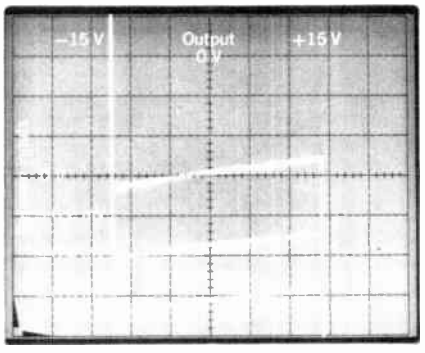
Common mode rejection ratio

The common mode rejection ratio (CMRR) of an op amp can be evaluated and measured with a curve tracer. Use of the null adjustment can improve the CMRR, but when some other parameter is optimized with the null adjustment, CMRR may suffer.

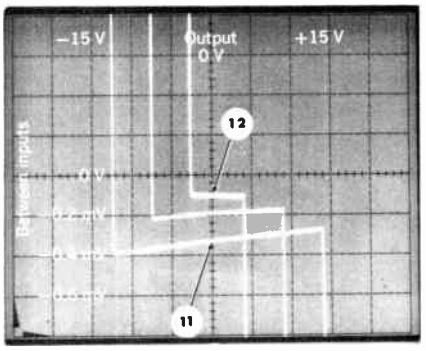
Figure 11 shows the CMRR of a type 741 op amp. The change in voltage between the two inputs is plotted vertically against common mode input voltage, plotted horizontally. The output of the op amp under test was held nearly constant at 0 volts while the test signal exercised the op amp. The CMRR is fairly linear for input swings from −10 to +10 volts (points 13 and 14). The voltage between the inputs had to be changed by about 0.4 mV to hold the output at 0 volts while the common mode input changed from −10 to +10 volts. The CMRR is about 20 volts divided by 0.4 mV or 50 000.



[7] **Offset voltage, type 741 op amp, ±15-volt supply, 20 000-ohm load.**

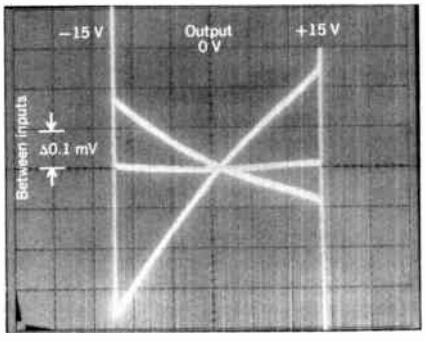


[8] **Offset voltage with temperature gradients, type 741 op amp, ±15-volt supply, 20 000-ohm load.**

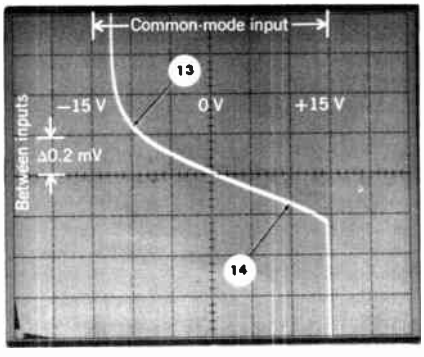


[9] **Input offset; type 741 op amp; ±5-, ±10-, and ±15-volt supplies; 20 000-ohm load.**

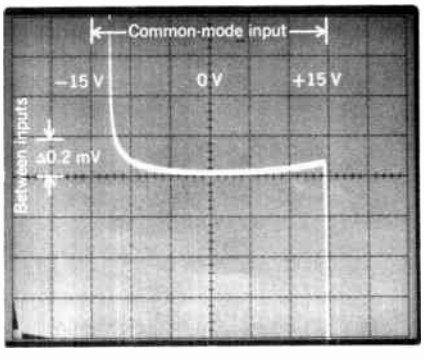
[10] **Gain change with three offset null adjustments, type 741 op amp, ±15-volt supply, 20 000-ohm load.**



[11] **Common-mode rejection ratio, type 741 op amp, ±15-volt supply.**



[12] **Common-mode rejection ratio, optimized with offset null adjustment, type 741 op amp, ±15-volt supply.**



Using the offset null adjustment with the same op amp, the slope of the CMRR curve was flattened, as shown in Fig. 12. Between the −10- and +10-volt points on the curve, the voltage between the inputs has to be changed no more than 0.08 mV to keep the output at 0 volts. This is comparable to a CMRR of 250 000. The offset voltage was changed from −0.35 mV to +1.3 mV to accomplish this improvement in CMRR. It should be noted that this procedure will also increase the offset voltage drift by about 3 μV/°C/mV of offset.

Power supply rejection ratio

Power supply rejection ratio (PSRR) may also be plotted and measured with a curve tracer. PSRR shows the effects that a change in power supply voltage may have on the output of an op amp. Either the positive or negative supply may be changed to show the effect, or both the positive and negative supplies may be increased and decreased simultaneously by the same amount to show the effect of that kind of change. The output of the op amp is held close to zero volts during these changes by applying the right amount of voltage between its inputs. Input voltage is plotted against power supply voltage.

In Fig. 13, the curve was traced with both the positive supply and the negative supply changing between 0 and 15 volts. The curve, however, shows only the positive half of the total power supply swing. The negative half is almost identical. Below about ±2 volts there is not enough voltage for the op amp to function normally. Points 15 and 16 correspond to the 5- and 10-volt supply levels and show that a change of 5 volts in the positive supply is comparable to about 0.8 mV of signal between its inputs. The ratio of 10 volts (±5 volts) to 0.8 mV equals 12 500. That ratio could be increased greatly by adjusting the null control to produce the curve shown in Fig. 14. For the op amp used, the offset had to be changed from +0.4 mV to −1.5 mV to optimize the plus and minus power supply rejection ratio.

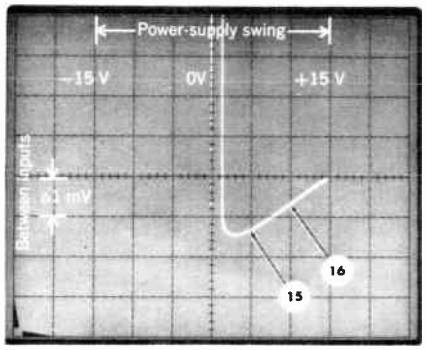
Supply current vs. supply voltage

Figure 15 shows the symmetry and linearity of supply current versus supply voltage for a type 1456 op amp. Only one supply voltage was swept at one time. The top half of the display is produced as the positive supply is swept from 0 to 15 volts. The bottom half is produced as the negative supply is swept from 0 to 15 volts. Below about 1 volt in either direction, current diminishes greatly and the op amp can no longer function normally.

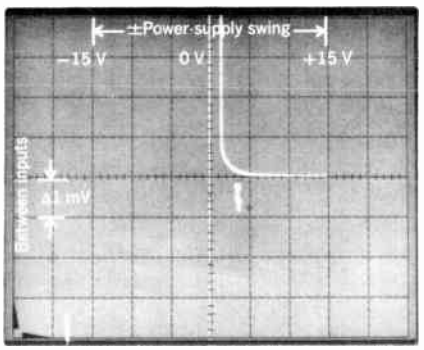
Figure 16 shows the curves for a type 308 op amp. In this case, supply current is practically independent of supply voltage from about 1 to 15 volts for either polarity. The curves are produced by changing the voltage between inputs enough to keep the op amp output close to 0 volts as one supply is swept from 0 to 15 volts.

Input current

Input current may be plotted in relation to common mode input voltage. Either the current passing through the positive input terminal or that passing through the negative input terminal may be displayed. Figure 17 shows both. Current at the negative input (bottom curve) is shown to be a rather linear function of common mode input voltage. Sometimes the curves even cross each other. Input current for the positive input is 100 nA (point 17) and the current for the negative input is 94 nA (point 18), 6 nA less. Input bias, defined as the difference between the two input currents at 0 volts output, is then 6 nA for this op amp. A notable aspect of the display

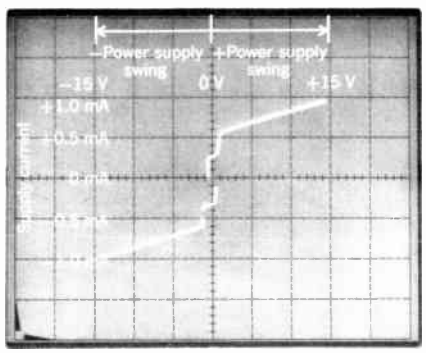


[13] ±Power supply rejection ratio, type 1456 op amp.

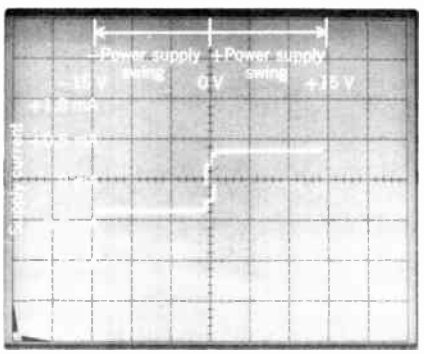


[14] ±Power supply rejection ratio, optimized with offset null adjustment, type 1456 op amp.

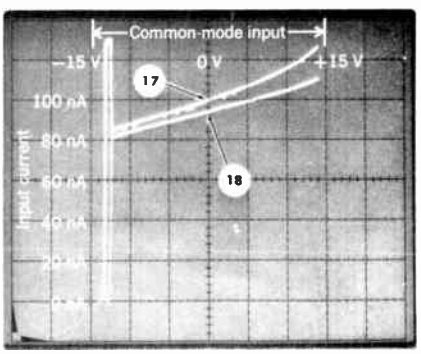
[15] Supply current versus supply voltage, type 1456 op amp.

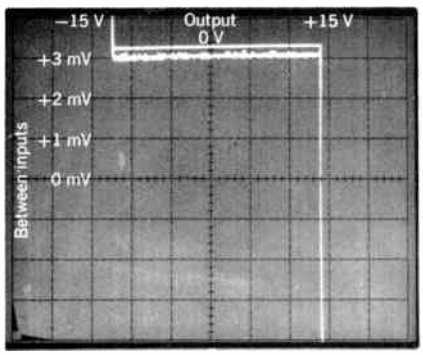


[16] Supply current versus supply voltage, type 308 op amp.

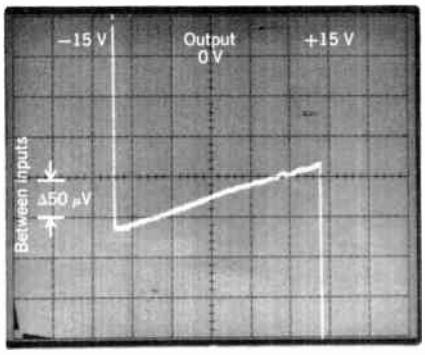


[17] Input current versus common-mode input voltage, ±15-volt supply.

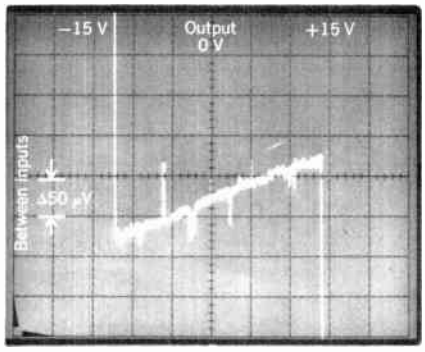




[18] Low-frequency noise versus source resistance, type 741 op amp, ±15-volt supply.

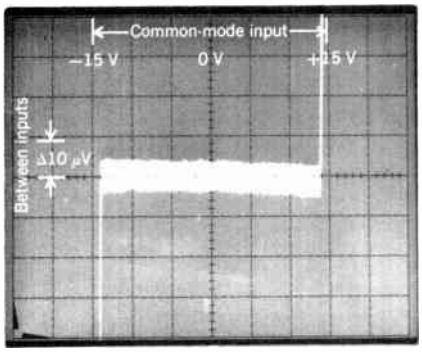


[19] Noise from 50-ohm source, type 741 op amp, ±15-volt supply.

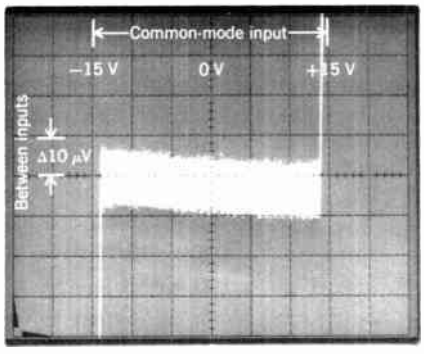


[20] Noise from 50 000-ohm source, type 741 op amp, ±15-volt supply.

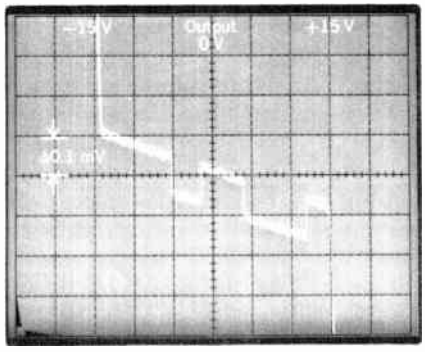
[21] Noise from 50-ohm source, type 308 op amp, ±15-volt supply.



[22] Noise from 50 000-ohm source, type 308 op amp, ±15-volt supply.



[23] Popcorn noise, type 741 op amp, ±15-volt supply.



is the extra noise current that is present at the positive input.

Chasing noise

It is interesting to see whether noise also shows up when measuring offset voltage. Figure 18 shows offset voltage measured two ways. The top curve indicates offset bias is 3.3 mV, but noise is not evident because the input resistances are only 550 ohms. When the input resistances are 50 000 ohms, however, the indicated offset bias goes down to 3 mV and noise again becomes evident.

In Figs. 19 and 20, the vertical scale was changed by a factor of 20 compared with Fig. 18. At this higher sensitivity, a dramatic difference between 50-ohm inputs (Fig. 19) and 50 000-ohm inputs (Fig. 20) can be seen clearly.

Not all kinds of noise show such a radical dependence on input resistance. And it should be remembered that, in the examples given, most of the noise was associated with just the positive input to the op amp.

A comparison of the effects of 50-ohms versus 50 000-ohms input resistance was made using another type of op amp, the 308. The results are shown in Figs. 21 and 22. There is about a 1.5 to 2 times increase in noise for 50 000-ohm sources. The high-frequency components of this kind of noise are evident in the two displays. The approximate amount of peak-to-peak noise can be seen to be slightly less than one vertical division in Fig. 21, which is equal to only 10 μV.

One of the most interesting types of noise found in op amps is so-called popcorn noise. The term is usually used to mean a type of noise that is characterized by a fairly low average frequency and random shifts between two discrete levels. Figure 23 shows an example. Popcorn noise may take several seconds to become evident and fast, point-to-point testers may miss it completely.

Although the value of op amp curve tracers has not been widely recognized, the examples cited in this article will hopefully give the reader a feeling for the usefulness and versatility of the instrument for this particular application.

John Mulvey has been with Tektronix for more than 20 years working in the production, marketing, and engineering departments. He spent nearly six years as a field engineer in Philadelphia and Los Angeles and, in recent years, had been providing technical training and support to field engineers. He is the author of two Tektronix Concepts books—one on sampling oscilloscope circuits and the other on semiconductor device measurements.

Jack Millay joined Tektronix in 1958 and has been involved with component evaluation since that time. He has managed the Curve Tracer Development Group for the past five years and is responsible for the design of many curve tracer products. Prior to doing instrument design work, he managed the Component Evaluation Group. He has written many technical articles for a number of electronics journals and for *Tekscope*, a Tektronix publication.

Linking microprocessors to the real world

A proper interface serves as communications traffic cop, setting priorities and directing the flow of messages

Microcomputers promise the engineer new design freedom. But, to harness the potential power of tiny computer chips, he has to enter an often unfamiliar world where software and circuitry must be skillfully combined. In forging the connections between various pieces of microcomputer system equipment, the engineer faces a task that demands the full use of these skills.

The box on this page reviews some of the basic terms used to describe this interconnection, or interfacing process.

Starting on the next page, Paul Russo and Michael Lippman describe how they designed the interfaces for a microcomputer-based store-and-forward communications system. Their experience illustrates how interfacing techniques can be combined to meet the requirements of a particular system design.

Howard Falk Senior Associate Editor

Taking a more general view, it seems important to consider the overall role of a microcomputer interface. The basic job of such an interface is to allow the transfer of information, back and forth between the processor section of the microcomputer system and various devices such as communication lines, keyboards, CRT displays, large memories, data collection devices, and control actuators.

Since the processor usually talks to all its peripherals over only one or two main interconnecting busses, the interface must insure that processor outputs reach only the intended peripheral. In the reverse direction, the interface must provide a means for information from each peripheral to reach the processor without interfering with other units hanging on the system busses. In addition, the interface must reconcile any differences between microprocessor and peripheral timing. The microprocessor runs on its own internal clock. Peripherals may, or may not, have internal clocks of their own.

What is a peripheral interface?

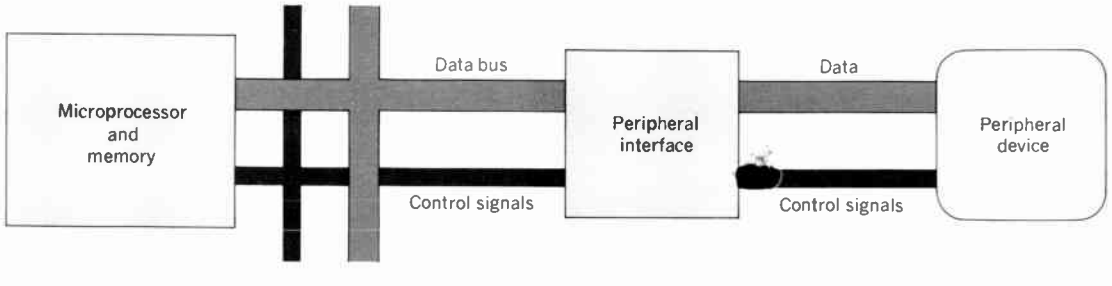
A *Microcomputer system* centers around a *Microprocessor* unit, capable of performing logical functions under the control of sequences of software instructions. Closely tied to the microprocessor is a *Memory* unit, capable of storing data and programmed (software) instructions.

The rest of the system is made up of peripheral units. Devices such as keyboards, teletypes, tape readers, CRT displays, disk memories, and even communications links, are all considered to be peripherals, when they are connected to the processor.

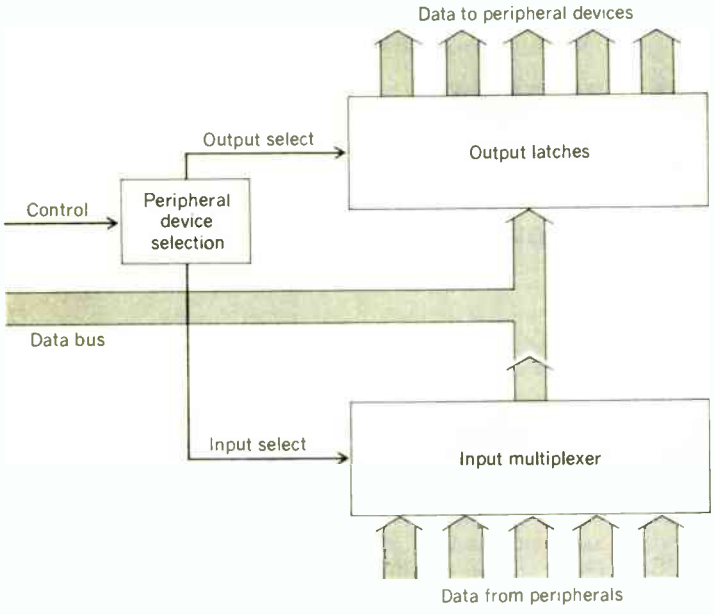
Data flows between the processor and the peripherals over a *Data bus*. Individual, binary data bits, travel on this bus in groups called *bytes*. For most microprocessors, a byte consists of 8 bits (however, there are also 4-, 12-, and 16-bit processors). One of these can be a *parity* bit, which may be added to make the sum of the 8 bits in the byte either an odd or an even number. This process can then be used to check for possible errors in the data, caused by noise or system malfunction.

The *Peripheral interface* is necessary to convert the data from the processor format to one that is acceptable to the peripheral device, and also to perform the required conversion from peripheral to processor data formats. The interface also reconciles timing differences and relays processor instructions in the form of control signals to the peripheral.

Flags—usually flip-flops—in the interface, are set to inform the processor of significant current, peripheral conditions. *Interrupts* are signals generated by the interface to force the processor to take immediate action when the peripheral must have quick service.—*H. F.*



[1] **Simple microcomputer input-output interface. Output latches, an input multiplexer, and their controls provide the elements needed to connect peripheral devices.**



The interface usually handles timing problems by temporarily storing data in shift registers or flip-flops. Then, when the processor is ready to take the data from a peripheral, the bits can be "clocked" out of this temporary storage by the processor clock.

Beyond the problem of reconciling data-transfer timing, the interface provides means for the processor to control peripheral actions and to get status information from the peripherals. Most microprocessors also provide one or more interrupt lines that the peripheral devices can yank, when they have an urgent need for attention from the processor.

Latches and multiplexers are basic

A simple input-output interface arrangement is shown in Fig. 1. Here, the bus from the processor transfers data to the peripherals through groups of flip-flops, called latches. A control signal from the processor selects the flip-flop group in which each segment of output data is to be stored, and each of these groups is connected to a different peripheral device.

Data coming into the processor from the peripherals is fed into a multiplexer. Using input select sig-

Case history: store and forward

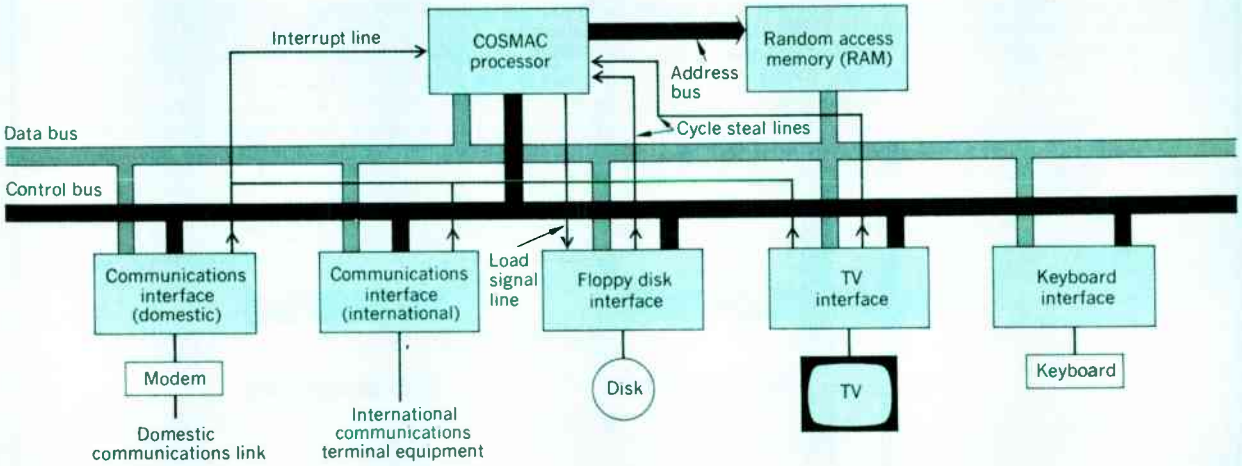
Here, in one system, are interfaces for communications, a floppy disk, and a TV display

Interfaces were a central concern in our design of a microprocessor-based store-and-forward system at RCA, for international leased line communications.

We found it desirable to make a number of interface parameters program-selectable, or programmable. For example, in our communication link interfaces, transmission characteristics such as data rate, stop-bit length, character length, and parity are programmable and can all be set by simple software instructions.

Paul M. Russo, Michael D. Lippman
RCA Laboratories

[A] **System-interface interconnections. Linking the processor and the peripheral interfaces are a data bus, a control bus, and special lines for: interrupts, cycle stealing, and initial program loading.**



nals the processor can choose which input it wishes to connect to its data bus.

Multiplexing is generally done by hanging a set of logic gates on the data bus connected to the output of each peripheral device. When enabled, a given group of gates connect the desired peripheral output to the data bus.

Tri-state gates are increasingly used for this function. In addition to the usual input and output signal lines, tri-state gates have a special control line input. When the control line is ON, the gate looks like any other logic gate—that is, its outputs can be either in the "1 or 0 state." The added feature comes in when the control line is OFF. Then the output of the gate has a very high impedence, and looks almost like an open circuit.

For the engineer who wants to connect many different devices directly to a single, common bus, the tri-state gate is indeed a boon. It virtually eliminates the need to deal with complicated impedance loading calculations, and substitutes simple control line selection of devices, for what might otherwise be a more cumbersome multiplexing procedure.

However, many logic designers don't yet feel comfortable connecting outputs directly together, in the way made possible by tri-state gates.

Interfaces on a chip are appearing

Most I/O interfaces for microcomputer systems are built up on integrated logic circuit packages, but complete interface packages on a single chip are beginning to appear.

Designing and producing a large-scale integrated (LSI) chip is expensive, but many powerful features can be packed into a small space. The idea is to provide one part that can be set to serve many different interface functions. Then each peripheral device can interact with the microprocessor through its own interface chip. With one chip for each peripheral, the volume use of the chips make the use of LSI economical.

The *Peripheral Interface Adapter* (PIA), shown in Fig. 2, was designed by Motorola Semiconductor Products Inc. to serve peripheral devices. Data from the microprocessor reaches the peripheral through either of two *Peripheral Interface Registers* that contain the necessary latches. Data from the peripheral to the processor is gated directly onto the processor

Just how our design finally took shape will become evident as we present a description of the system's interface hardware and software.

Moving messages through the system

Incoming messages enter the system through one of two communications interfaces. Here the messages are converted from a stream of bits into characters, each contained in an 8-bit data byte. These bytes are transferred, one at a time, into the system's semiconductor random access memory (RAM). When 232 bytes accumulate, they form a *block* of data.

The data block is then moved into the larger disk memory, where it is held until needed for retransmission. Outgoing data blocks move from disk, to RAM, to the appropriate communications line.

The RCA COSMAC microprocessor controls this sequence of events with programs written to fill the requirements of the overall store-and-forward communication process.

The entire microcomputer system (Fig. A) consists of a large-scale integrated microprocessor, a 4096-byte RAM, and five peripheral interfaces, each of which use a group of integrated circuit packages, and serve to connect different "devices" to the system.

The microprocessor makes both a data bus and a control bus available to the peripherals. These busses carry almost all the information that flows between the processor and the peripherals.

Since several different interfaces are connected to these busses, there must be a clear way to indicate which interface is permitted to be active at any given moment. The *Select* instruction performs this assignment function.

Each interface has its own, unique selection number. For example, a *Select* instruction together with the number 08 on the data bus, will activate the floppy disk interface. Once an interface is selected, it is free to act on further processor instructions.

To control certain peripheral functions—such as disk startup and head location, or communications transmission speed—the processor issues a *Set* instruction. Other processor instructions are used to test the state of external flag lines. These lines are connected to flip-flops, set by the peripheral interfaces to indicate such conditions as readiness to read or write, as well as faults and error conditions.

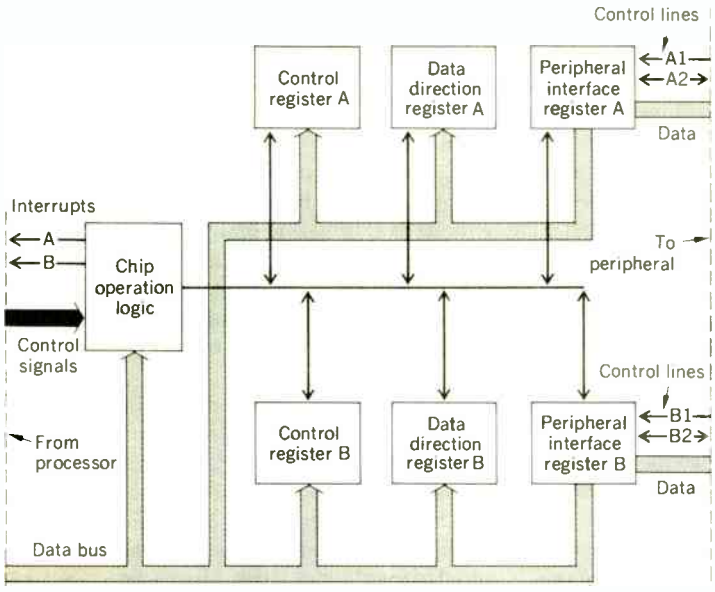
Three special lines allow the peripheral interfaces to initiate system actions, without first getting permission from the processor. By using the *Interrupt line*, the communication interfaces demand immediate handling of incoming data as it arrives on the communications links, and an immediate supply of outgoing data from the RAM, as it is needed for transmission over the links. With the *Cycle steal lines*, the floppy disk memory and TV display gain direct access to the RAM so they can write into the memory, or read from it, without software instructions. Finally, via the *Load line*, the system can be reset and restarted—using a disk-stored program—after a catastrophic failure or loss of power.

Inside the communications interface

When a communications interface has received an incoming character from its communications link, it raises the microprocessor interrupt line. At the same time, this unit raises an external flag, EF1, to indicate that a received character is available.

At the microprocessor, the interrupt causes the ongoing program to branch to a special software routine designed to service interrupts. Since there is only one interrupt line, the routine must first find out

[2] Interface on a chip. This flexible and sophisticated interface was designed to connect a wide variety of peripherals to the Motorola M6800 microprocessor system. Two sets of lines are used to send and receive peripheral data.



data bus.

The processor selects the peripheral device it wishes to talk to, by sending *chip select* control signals to the PIA *Control and Select Logic*. Every peripheral interface chip in the system is selectively wired so that these signals will activate only the interface that is selected.

Other control signals from the processor allow the processor data bus to reach any one of the six PIA registers shown in Fig. 2. There are also signals that properly time the peripheral interface outputs to the processor and that reset the interface circuits when system power comes on. Two interrupt lines allow the PIA to initiate needed processor activities.

The PIA is capable of a wide variety of different operations, including several powerful, automatic modes. For example, a single command from the processor can send a data byte through the PIA to its peripheral on a handshaking basis, and the PIA will do all the necessary details of housekeeping completely automatically.

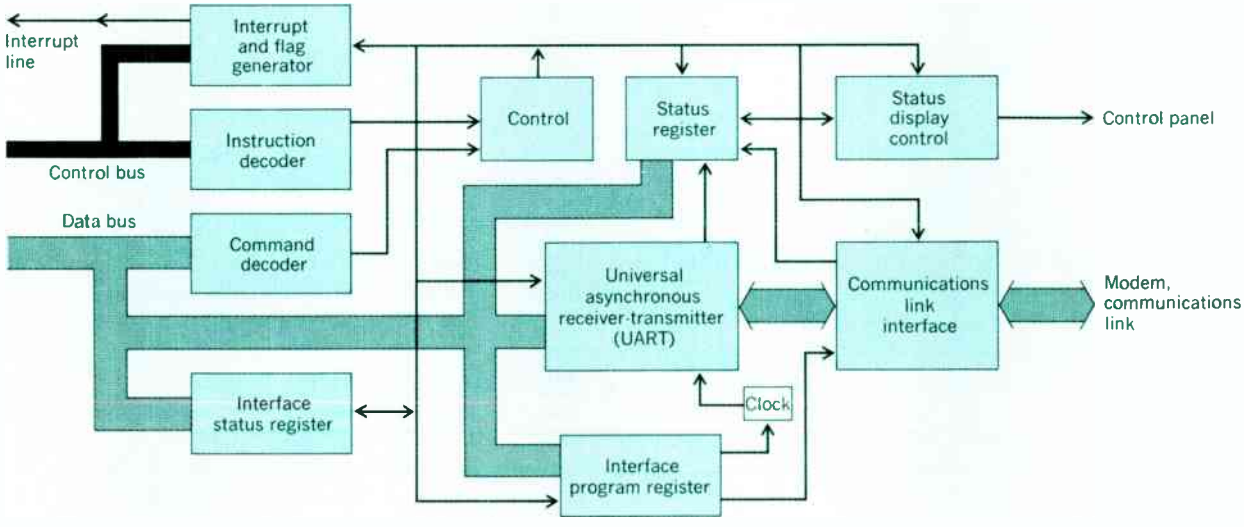
To get this kind of operation, the PIA must first be set up, by loading appropriate control bits in its *Control* and *Data direction* registers. These registers are

which of the two communications interfaces sent the interrupt, and then determine what kind of service is needed. This information is obtained by testing to see which external flags are raised.

The actual programmed sequence in the interrupt routine includes a *Select* instruction for each communications interface. After an interface is selected, its external flags are tested to determine the presence and cause of the pending interrupt. Knowing the device and its flagged condition, the processor issues an appropriate instruction to service that condition. For example, in response to flag EF1, indicating a received byte of data is available, a *Read* instruction would be issued to call for the transfer of a byte of data from the communications interface to the processor (for transfers in the opposite direction, a *Write* instruction is used). On receipt of the *Read* instruction, the interface places the received byte on the ingoing data bus, and the processor clocks the byte into RAM memory.

The system allows up to four external flags (EFs) for each peripheral interface, and the meaning of each of these flags—or combinations of flags—can be different for each interface. For the communications interfaces, EF4 is set in conjunction with EF1 if the received character is erroneous (bad parity). When an interface is transmitting data, EF2 is set to indicate that the next character can be transferred. Finally,

[B] Internal functions of the communications interface. Two of these interfaces are used in the system. One handles the domestic traffic link; the other, the overseas traffic link.



each set up by a single control byte (8 bits of data) sent from the processor on the system data bus. Separate control signals to the *Chip operation logic* specify the register that will receive the first control byte. When such a byte is received, its bits set the registers for the kind of peripheral operation that is desired.

For example, the *Data direction register* control bits define whether data can flow into, or out of, the system data bus lines connected to *Peripheral interface registers A* and *B*. The data bus includes eight parallel bit-lines and the direction of each of these can be independently set.

Usually the "A" data lines are set to send data in from the peripheral to the processor, while the "B" lines are used to send data out to the peripheral. Indeed the A and B sides of the PIA are specifically designed to handle these data transfers efficiently. The *Control registers* are set up to select the use of the interrupt lines to the processor and the control lines to and from the peripheral. One combination of control bits in *Control register B* might set up control line B2 (see Fig. 2) to go low, right after a data word from the processor is loaded into *Peripheral interface register B*. The same control setup could also specify that B2 would remain low until a signal from the peripheral—on line B1—indicates that the data has been received. Finally, the same control setup could relay the B1 signal back to the processor, on Interrupt line B, to call for another data word to the peripheral. With this kind of automatic operation, the programmer can set up the PIAs to handle peripherals with very simple and fast software routines.

The PIA has two "interrupt" lines going to the microprocessor. These can be set up as flag lines—presenting information about the status of the peripheral to the processor—or they can be set to be used as interrupts, which demand the immediate attention of the processor.

For situations where input-output needs don't have to be served immediately, polling techniques are often used. In that case, the microprocessor is programmed to test the *Control registers* every so often, for given logic levels on the flag lines, and when these are found, it can leave its ongoing program temporarily, to serve the peripheral device that needs attention. When peripherals require more immediate attention, interrupts from the peripheral are used to force the processor to branch from its ongoing pro-

EF3 is used to indicate special conditions, such as abnormal communication line operation.

While a given interrupt is being serviced, all other interrupts must wait their turn. Priorities for servicing interrupts are established in the processor's software interrupt routine. For example, the domestic communications interface is always selected first by the routine. Domestic data rates are usually higher than international rates, and therefore the penalty for keeping the domestic line waiting is greater. Likewise, *Read* interrupts are always given priority over *Write* interrupts, because failure to read may result in loss of data, but the worst penalty for failure to write is time lost on an idle transmission line.

The interrupt-driven form of data transfer is well suited to the communications function. Competing functions and devices are easily queued; each input character can be examined and processed as it is received; new devices are easily added; and existing device priorities are easily changed.

The hardware that communicates

Communications interface hardware centers on a large-scale integrated circuit—contained in a single 40-lead chip—that handles several key functions. This circuit, called a *Universal asynchronous receiver-transmitter* (UART), converts data bytes from the microprocessor into a stream of serial bits for the communications link. The UART also performs the opposite conversion, taking serial bits from the communications link and shaping them into characters for the microcomputer system. Actually, each character consists of up to 8 data bits, and an odd-even parity bit may be added. When called for, these parity bits are generated by the UART as it transmits characters, and the UART also checks the parity of incoming characters from the communications link.

Surrounding the UART are a number of functional blocks implemented in transistor-transistor logic (see Fig. B). The *Interface program register* provides the means for microcomputer program instructions to control the *Clock* and the communications mode (half- or full-duplex). Flip-flops in this register select speed-control lines into the clock to allow program selection of bit-per-second transmission and reception rates. The type of parity (even or odd), length of characters, and number of stop bits used in serial transmission are also under program control.

To connect the transistor-transistor logic (TTL) circuits in the interface to communications link circuits, some matching is necessary. This is done in the *Communications link interface* circuitry. For links using RS-232 industry-standard data interfaces, voltage-level shifting of TTL signals is needed. For teletype links, output currents must be controlled to specified levels. Some communications links require that there be no direct ground connections. For these, optical isolation devices must also be included.

Instructions to the communications interface from the processor are received over the system's control bus and routed through the *Instruction decoder* which interprets microprocessor codes and generates logic signals that can be used to control the interface hardware. Since some of these microprocessor codes come over the system data bus, there is a *Command decoder* to interpret this added information. The *Interface status register* indicates whether the interface is, or is not, currently selected and thus allowed to communicate with the processor.

The *Control* logic distributes all the appropriate information to the *Interface program register*, the *UART*, and other parts of the interface. The external

gram to one that will serve the peripheral as soon as possible.

Interrupts and more interrupts

Most present-day microprocessors make some form of interrupt capability available. But there are interrupts and interrupts. Some processors just give the user a single general interrupt signal to work with, and that is often far from adequate. To handle the interrupt properly, the system usually needs to know where it originated and why it occurred.

Other processors, like the Intel 8008, use a single interrupt line, but offer a somewhat more elaborate capability. The user can code three bits, which allow him to reach specified main memory locations. The idea is to store the first instruction of an appropriate interrupt-handling routine at each of these locations. With three binary bits, up to eight different interrupt routines can be addressed. The capability is called a *vector* interrupt.

Some of the newer processors offer more than one interrupt line. The National Semiconductor IMP-16C microprocessors offer two lines—one is a vector interrupt; the other, a general interrupt. Motorola's M6800 processor provides two interrupt lines, and the Toshiba TLCS-12 processor has eight independent lines, with a hardware-implemented priority scheme.

Of course, the system designer can usually make his application work with a single, general interrupt line, but there may be extra costs attached to his design. He may use external circuitry to handle priority when several different interrupts occur together. That will mean added equipment costs. He may be able to solve the priority problem with software. But an interrupt-handling subroutine takes time to handle the job, and time can be a critical design parameter.

The capabilities of the interrupt lines give only part of the design picture. Important also is the sequence of events that occur when an interrupt takes place.

At that time, the processor is probably churning away at ongoing program tasks. When an interrupt occurs, the processor is supposed to complete the current ongoing program step, and then drop everything to take care of the interrupt.

The problem is, that after the interrupt has been served, the processor is supposed to continue the ongoing program just where it left off. To return to this task smoothly, it is always necessary to store

flags that inform the processor of the interface current status are placed on the system's control bus by the *Interrupt and flag generator*. This information comes from the UART and *Status register*, which is used by the UART and other circuits to record the occurrence of such fault conditions as parity errors and open communications lines.

The third major element of the system, in addition to the communications interface and the microprocessor-RAM combination, is the floppy disk interface.

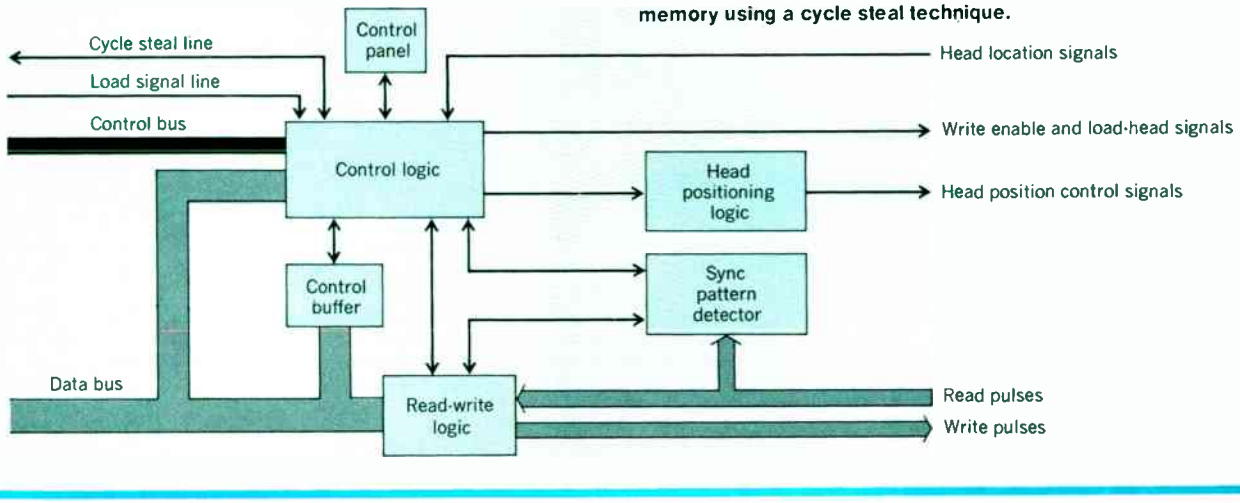
Stealing cycles for more efficient operation

The key feature of the floppy disk interface is its direct access to RAM memory, without need for detailed microcomputer program control. Using this direct memory access feature—built into the COSMAC processor—the disk can put data bytes into the RAM, or take them out, without receiving even a *Select* command. In fact, it can transfer this data while the processor is occupied with other tasks, such as talking to a communications interface.

The direct memory access mechanism used here is called cycle stealing. There are normally two microprocessor cycles for each program instruction: a fetch cycle, followed by an execute cycle. When the cycle steal line comes up, say during a fetch, the processor will complete that fetch, and the corresponding execute cycle, and then hold its breath for a one-cycle interval before moving on with the next instruction, fetch cycle. It is during these stolen one-cycle intervals that data bytes are moved between the RAM and the disk.

Before the cycle stealing can begin, a direct memory access address register must be loaded with the

[C] Floppy disk interface. Once set in motion by processor commands, the disk speaks directly to the system's RAM memory using a cycle steal technique.



something. Ideally it would be best to store the entire state of the machine including the contents of the arithmetic accumulator, and all registers, as well as all of the flags that indicate the statuses of various system operations. In practical terms, storing the contents of a few key registers may be adequate.

Having stored the ongoing program status, the processor is free to handle the interrupt. When finished, it can retrieve the status information and smoothly resume its ongoing tasks. This store-and-go operation should, ideally, be as fast and simple as possible.

Some of the newer processors, like the Intel 8080, Motorola 6800, and the RCA COSMAC, take care of this store-and-go operation automatically, but with other machines, the process may be more difficult.

For example, a simple store-and-go procedure is not possible in the Intel 8008. After an interrupt, the 8008 registers that are used to reach the microcomputer memory continue to hold address values needed by the interrupted program. The user can get around this shortcoming by reserving two of the processor's general-purpose registers to hold the contents of these main storage address registers during the interrupt. But this is awkward, because in addition to the time lost for the necessary program steps, two of the system's seven registers are then not available for processing the interrupt.

A more acceptable alternative is to add enough external circuitry to supply a register that can hold three bytes of information. By passing the contents of the two storage address registers through the 8008's accumulator register, the contents of all three of these registers—all the information needed to resume the interrupted program—can be stored in the new external register.

Following the interrupt servicing process, the end registers can be reloaded by using an input instruction to the external register. This process can be quite efficient, in terms of the number of program steps required, if the external register is in the form of a push down stack that can be both "pushed" and "popped" by a single instruction. However, it does mean that added hardware—the external register—must be used.

One-chip communications interfaces

In minicomputer and microcomputer systems, interfaces with communications lines have usually been

first RAM memory address of the data block to be read from, or written on, the disk. Then the register is automatically incremented at each succeeding stolen cycle, until an entire block of 232 data bytes has been transferred. And all the processor sees is a slight slowdown, usually less than a 1-percent reduction in the time available for its ongoing program activities.

Controlling the floppy disk

The floppy disks used in this system are 7.5 inches in diameter. Data is recorded on one side of the disk —coated with oxide material—which is made of flexible plastic. The disk is packeted in a paper envelope, and a recording band, about one inch wide is accessible through the envelope.

During reading and writing the disk is "loaded," so that physical contact is made between the read–write head and the disk surface. Since this causes wear, it is desirable to unload the disk as soon as possible. The disk rotates at 90 r/min, can store 1.4 Mb, and costs about $5. Data can be transferred from the disk at a rate of 33 kb/s, and it takes an average of 560 ms to reach a desired specific data block on the disk.

Each of the disk's 64 concentric data tracks can hold 8 complete blocks of data. And each of these blocks begins with 16 bytes of synchronization information, followed by 232 bytes of data, and capped off by 8 bytes of trailing zeros.

This structure provides an 11-ms gap between adjacent blocks on the same track, and this gives the system enough time to process the blocks one right after another.

Data from the disk is always transferred to the system's RAM memory, before going elsewhere, and all data stored on the disk comes to it from the RAM.

As with the communications interfaces, a *Select* instruction—including the disk's identifying number—is used to initiate contact between the processor and the disk. Four additional instructions are used to control disk functions. *Locate A* and *Locate B* specify the disk storage location for each block of data; *Start* loads the disk head and allows data flow to or from the disk when the desired location is reached; *Stop* unloads the disk when the desired data transfer is completed.

To follow these disk control operations in more detail, refer to the interface function diagram in Fig. C. The *Locate A* instruction sends the desired track-location number to the interface *Control Logic*, and *Locate B* sends the corresponding sector-location number.

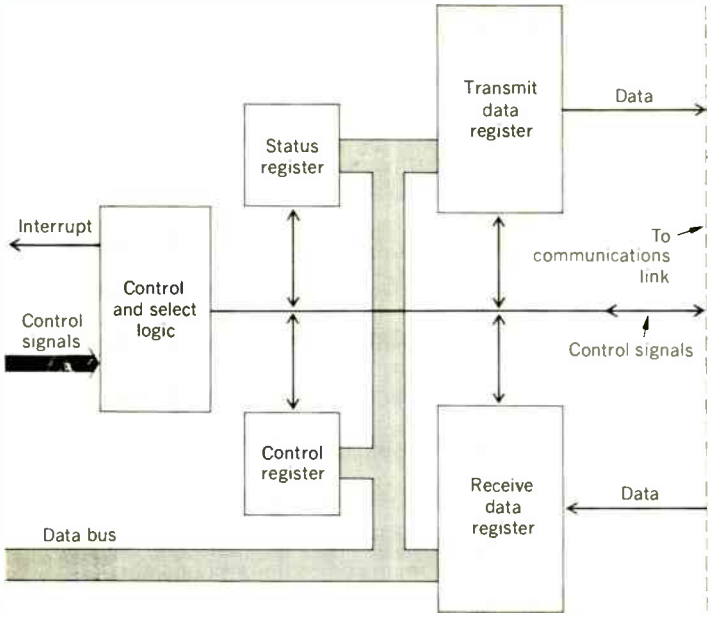
Actually, the *Locate B* instruction serves a double purpose since it also tells the control logic whether data is to be written onto the disk or read from it. This information, along with the current track and sector location data, is stored in the *Control Buffer*, where it is available until updated by new *Locate A* or *Locate B* instructions.

When a *Start* instruction is received, the *Control Logic* activates the *Head Positioning Logic* to move the head into the position stored in the *Control Buffer*, and simultaneously loads the head into contact with the disk.

After the disk mechanisms have had time to settle to steady-state operation (delays to guarantee this are generated by the *Control Logic*), the actual data transfer is initiated by the interface itself. No processor instructions are needed during this transfer, which is not complete until an entire block of data has been moved.

When the disk is to be read, the disk head is first loaded, the desired location is reached, and the read

[3] Asynchronous Communications Interface Adapter (ACIA). On a single chip, this device provides a variety of program-selectable functions.



constructed of dozens of integrated circuit logic packages mounted on large boards. Development of standard Universal asynchronous receiver-transmitter (UART) chips, each replacing 20 to 25 logic packages, has considerably simplified this type of equipment. The communications interfaces described by Russo and Lippman in this article, illustrate a UART-based design.

Recently, single-chip communications interfaces have been announced and are expected to be on the market soon. These large-scale integrated circuits combine, in a single package, all of the functions needed to connect a microprocessor system to a communications link.

Motorola Semiconductor seems to have the most sophisticated of these new single-chip devices. Called the Asynchronous Communications Interface Adapter (ACIA), this device operates with the Motorola M6800 microcomputer system to provide software control of a variety of interface functions. Serial data flows from the communications link into a shift register in the ACIA's *Receive data register* section (see Fig. 3).

Here, incoming bits are assembled into bytes, to be

circuits are activated somewhere within the 16-byte synchronizing pattern that prefaces the desired block of 232 data bytes. The *Sync Pattern Detector* then searches for the synchronizing pattern to determine the exact moment when the first data bit in the block is about to move into position under the read-write head. This mode of operation allows large design tolerances on both the location of the head and on the timing for reading and writing.

The *Read-Write Logic* frames the data bytes while the disk is read. That is, it defines the beginning and end of each byte as it appears in the serial stream of one-bit read pulses from the disk. When it is time to transfer a byte of data to the microcomputer RAM, the *Control Logic* raises one of the cycle steal lines, and the byte is then placed on the system data bus. When data is being recorded on the disk, the *Read-Write Logic* takes in each data byte and converts it into a stream of one-bit write pulses to the disk head.

At the present time, the *Read-Write Logic* adds a parity bit after every 8 bits it sends to the disk. When the disk is read, these parity bits are checked to get indications of errors that may have occurred during the disk read operation. Since disk errors tend to occur in bunches, or bursts, future system design plans call for the use of burst error-detecting coding techniques rather than parity bits. The savings in available storage space should be substantial.

In addition to coordinating all the other disk interface operations, the *Control Logic* sets the external flags that notify the processor about disk conditions. For example, a flag is raised when the interface finishes transferring a complete block of data to the RAM, or when a complete block of data has been written on the disk. By testing this flag, the microprocessor program can decide when to change *Locate* instructions, and initiate new *Start* instructions to read or write additional data blocks.

As a convenience feature, the disk stores a bootstrap program that can restart the entire microcomputer system from scratch after power is lost, or after some other unanticipated condition puts the system out of commission. Any other program residing on the disk can then be loaded using this bootstrap program, eliminating the need for auxiliary program load devices such as cassettes or paper tape, and greatly simplifying system regeneration after a crash.

Less vital to the system than the floppy disk, but still interesting from an interfacing viewpoint, is the TV display.

Talking to a TV display

The TV can display text indicating communication-link fault conditions, and other system status conditions. But experience has shown that its most useful function is to display memory patterns; bit patterns on the data bus; and other information for diagnosis, test, and maintenance of the system.

A standard, unmodified TV set is used for the display which is refreshed from 128 bytes of RAM memory. This storage space is dedicated to the display, and these data provide 1024 dots for the display. Like the floppy disk, the TV display uses the direct memory access (cycle-stealing) capability of the system.

Every 60th of a second, the TV interface interrupts the processor and asks for new information. The interrupt routine then points to the beginning of the 128 bytes of RAM memory that contain the TV display data. These data are then sent to the TV interface on a cycle-stealing basis.

Since only one peripheral device can be served at a time by the direct memory access capability, the disk

sent to the microprocessor on the system data bus. Outgoing data moves from the system data bus to the *Transmit data register*, where it is shifted out as a stream of serial bits—with necessary added trimmings, such as start bits and parity bits—onto the communications link.

Operation of the interface is set up by software, in the form of a single byte of control information stored in the *Control register*. Among the communications parameters controlled by the contents of this register are: the word length, parity (even or odd), and number of stop bits for each transmitted or received character.

It is interesting to note that Paul Russo and Michael Lippman (see companion article below) also made programmable parameters a feature of their communication system interfaces. In fact, after completing their equipment, they felt that their floppy disk interface would also have benefitted from the use of programmable parameters.

They found that this approach is preferable, in most applications, to one that requires manual hardware modification, whether this consists of logic modification or simple strap selection. For their disk, they felt parameters such as parity, block length, character length, sector size, and head stepping-time could all have been made program-selectable. The interface would then have been capable of controlling a multitude of different disk drives with only minor modifications to its hardware.

The ACIA contains its own clock, to time incoming and outgoing data, and the rate of this clock is set by control register bits. Here, control is limited to the basic clock rate and rates of $\frac{1}{16}$ and $\frac{1}{64}$ of the basic rate. The control register contents also determine whether or not an interrupt will be generated when the receive data register is ready to communicate with the microprocessor. Finally, the control register provides for optional transmission of a break level (space) on the communications link, sets the level of request-to-send signals for controlling a communications modem, and enables or disables a ready-to-transmit interrupt to the microprocessor.

The *Status register* stores the flags that notify the microprocessor of important conditions at the interface. These include indications that data has been received from the communications link, and that the transmitter is ready for data from the microprocessor, as well as such error indications as overrun (data coming in faster than it is being read) and parity error.

The ACIA can be operated on a polling basis, in which case the microcomputer program checks status flags and initiates all transfers of data to and from the interface. It can also be operated on an interrupt basis. Interrupts to the microprocessor are generated when the *Receive data register* contains a full byte of data for the processor, and also when the presence of a carrier is first detected on the communications link.

A second one-chip communications interface is the Telecommunications Data Interface (TDI) designed for use with Rockwell International's PPS microprocessor systems. Like the ACIA, the TDI accepts serial bits from a communications link, converts them into bytes for the microprocessor, and vice-versa, while taking care of formatting, parity, and other communications housekeeping chores.

A unique feature of the TDI is the inclusion of a full modem on the same chip as the interface circuitry. The 1200-b/s modem is designed to drive a telephone line through an operational amplifier.

The TDI generates interrupts when the transmitter register is empty and when the receiver register is full. These must be followed by microprocessor instructions to test the source of the interrupt. From one to eight characters may be transmitted or received within a single pair of start and stop bits, allowing very flexible formats.

Parameters like bit-rates, parity, and word length are set by wired-in circuit straps and cannot be changed—as they are in the ACIC—by program instructions.

and the TV cannot operate simultaneously. The disk, vital to the main communications function of the system, is given absolute priority over the TV. The result is that when disk and TV needs conflict, the TV display may flicker or show a reset pattern for up to about ½ second.

The lowest-priority peripheral in the system is the *manual keyboard* used to enter data bytes (in the hexadecimal code internally used by the system) into the RAM memory. This provides a means to debug and modify programs—for example, to change track and sector numbers manually for floppy disk operations.

Paul M. Russo (M) joined RCA Laboratories, Princeton, N.J., in September 1970. There, he has done research in the areas of computer architecture, program behavior, computer system performance evaluation, microprocessors, and data communications. During the 1969–70 academic year, he taught circuit theory and circuit optimization at the University of California, Berkeley. Dr. Russo was born in Plevlje, Yugoslavia, in 1943. He received the B.Eng. degree in Engineering Physics from McGill University in 1965, and the M.S. and Ph.D. degress in electrical engineering from the University of California, Berkeley, in 1966 and 1970. He is a member of ACM, Eta Kappa Nu, and Sigma Xi.

Michael D. Lippman (M) has been a member of the Technical Staff of the RCA Laboratories, Princeton, N.J., since 1966. He has done research on magnetic recording, vapor transport processes, and graphics data compression. He is currently engaged in the development and design of microprocessor-based data communications systems. Mr. Lippman is a member of Tau Beta Pi and Eta Kappa Nu.

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Electronics and Swiss railways

Switzerland's rail system designers' bag of tricks ranges from wayside signals to sophisticated telecommunication and automation

The Swiss rail network has become as sophisticated in its services to its passengers as any in Europe (see the first of this two-part series in the August *Spectrum*, pp. 44–54). Though less extensive, Swiss suburban commuter and urban transit systems are equally advanced. Why? Speed and traffic density have necessitated a radical upgrading in design sophistication of signaling, safety, and telecommunications systems.

Rail vehicle automation

The obvious answer for meeting increasingly rigorous performance criteria—the needs for more rapid acceleration and deceleration and for decreased train headways, for example—was to transfer the train control operations from the driver to a compatible automatic train supervision (ATS) system.[1] Accomplishing this objective permits the driver to focus his attention more completely on the visual monitoring and surveillance of the track ahead and the wayside signal system.

However, at speeds over 125 km/h, the driver's task of accurately observing wayside signal aspects can become very difficult, especially under adverse weather conditions.

Brown, Boveri Company engineers at Oerlikon indicate that the current policy of the Swiss Federal Railways (the Schweizerische Bundesbahnen, or SBB) is to keep the driver in manual control of his train while the ATS continuously checks his operations. The primary task of the ATS is to indicate to the driver the permissible zone speed and/or speed restrictions in heavily trafficked sections and interlockings. These engineers feel that full automatic train operation (ATO) is not yet feasible for Swiss mainline trains, but they foresee its near-term application to S-Bahn systems (which will be discussed later in this article).

Nevertheless, the establishment of command and control speed and braking programs, routing, and station-stop scheduling, which will be transmitted from fixed stations, is proceeding apace with the ultimate goal of mainline ATO in mind. In such a configuration, both on-board and fixed-station computers will be the central components. The telecommunications link for this projected system must function universally for various classes and vintages of locomotives and train sets under all climatic conditions (and Alpine winters can be very rough!). Further, the signals must be capable of being transmitted through long tunnels (see Box, p. 75)—and, especially, the spirals. Therefore, the SBB selected a special continuous-cable track conductor for its circuits. As of the end of last year, 30 km of such conductors were installed along a section south of the St. Gotthard tunnel.

Gordon D. Friedlander Senior Staff Writer

A basic ATC system layout

Figure 1 is a block circuit diagram illustrating the basic principles of an automatic train control system and showing the basic layout of speed-control and braking subsystems.[2] In operation, the driving switch, or master controller, provides to the speed regulator (1) the difference V_t between the desired speed V_c and the actual speed V. Beyond the speed regulator, the configuration divides into the motor-current-control circuit (top) and the braking circuit (bottom). The speed regulator furnishes the required value current I_c, which is a dependent variable of the difference (V_t) between desired and actual speeds, and this current is fed into the motor-current-control circuit. The speed regulator also supplies the pneumatic-brake pressure reduction P_{oc} in the brake-control circuit subsystem.

The motor-control circuit comprises the

- Motor-current controller (2), which acts on the tap-changer position S
- Tap changer, with transformer taps (3) supplying the motor voltage U_m
- Traction motors (4)

The current controller regulates the motor current to the desired value I_c.* By limiting the value of I_c, the motor current can be easily restricted to the maximum permissible value both for running as well as for regenerative (dynamic) braking, because the controller can only reach the maximum desired value of the motor current.

The brake controller (5), which gives the required pressure P_c for the main line of the air brakes, is located in the brake-controlled branch, together with the electropneumatic pressure transducer (6). This last-mentioned component converts the desired P_c to the corresponding pressure P in the compressed-air line. The subsystem also includes the compressed-air brake (7), which is applied throughout the train.

The brake controller ensures equalized and uniform application and release of the air brake to attain the desired pressure reduction P_{oc}. Further, it is inter-

* For traction, or running, operation, the value of I_t is positive (+), and negative (−) for regenerative brake operation of the traction motors. The motor-current controller must also act on the reversing/brake-changeover switch (not explicitly indicated in Fig. 1).

esting to note that the characteristics of the speed regulator for the two desired current and pressure reduction values (I_c and P_{oc}) are so coordinated with each other that the air brake does not engage until the electric regenerative braking force is insufficient to maintain the speed difference, or deviation (V_c), within allowable limits.

The traction motors thus supply the regenerative braking force Z, while the mechanical force Z_b is furnished by the air brake. The resultant force (Z_r) acts on both the traction vehicle (locomotive) and the train loading, or trailer cars (8), and these two variables determine the traveling speed V.

A practical example: if a train proceeds from a level section through a transition into an ascending grade, the climbing resistance W'_s will increase,† thereby initially causing the speed V to decrease. This speed change is immediately measured by the speed regulator, and the required value for the motor current I_c is increased. This is the reason why the motor-current controller regulates the motor current I by notching up the tap changer to a higher position; thus, the tractive effort Z is increased and the speed V is maintained constant.

However, if the train enters a downgrade section, the traveling speed V will initially increase a bit. But the speed regulator reacts instantly to this speed change by a reduction of I_c. This, in turn, causes the tap changer to be switched back, the reversing and brake changeover switch are set to braking mode, and a brake stage is selected that will maintain the speed at an almost constant value. If the electric regenerative effort is not enough, the air brake is also automatically cut in.

The desired speed value V_c is increased or lowered for acceleration and deceleration, respectively. The speed regulator then monitors I_c or P_{oc} so that the speed V follows the value of V_c as closely as possible.

This procedure has been tested with prototype equipment. With certain modifications, it can be used for multiple-unit operation (two or more traction vehicles used in tandem). The lead traction vehicle handles the entire regulation and control operations in this mode, with the exception of the motor-current controller; the other components are locked out in the remainder of the traction vehicles.

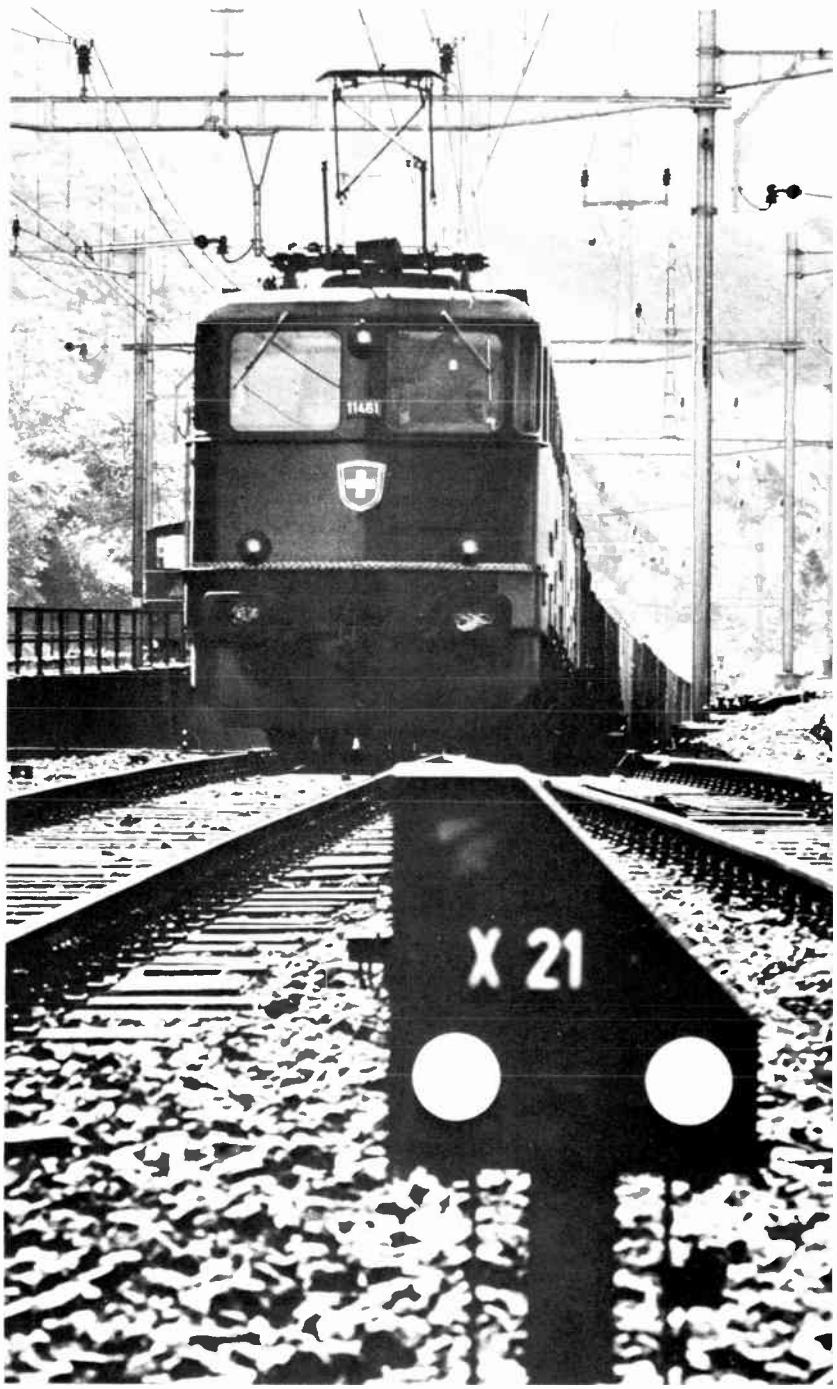
The SBB has also installed on the Gotthardbahn an ITT-built (Standard Elektrik Lorenz AG) CATC system, called CORECT, similar to that which is in operation in Germany between Hamburg and Bremen. The first portion (24 route kilometers) of the CORECT system will go into service before the end of this year.

Signaling and communications

Similar to the system employed on the German Federal Railways (see "Germany automates its rails," *Spectrum*, July, pp. 73–77), track circuits are used for wayside-to-train and train-to-station communications. Coded information is transmitted from wayside stations to trains at a frequency of 30 kHz. The optimum transmission rate is 1200 bauds per second.

In the supervisory sections, which are usually 12 km long, the fixed station must have the following

† The effect of the catenary voltage U_f on the motor voltage U_m, together with the climbing resistance W'_s of the line section acting on the traveling speed V are both "disturbance values."



Workhorse of the Swiss railways, the SBB Ae 6/6 engine develops 4480 kW with speeds of about 120 km/h. In the foreground is a dwarf signal, located at each station switch to indicate route settings and shunting movements for incoming and outgoing trains.

characteristics and data from each train in its control area in order to calculate permissible speed, headway, and safe-braking distance:

1. Type of train (freight, local passenger, or express passenger)
2. Weight and length of train
3. Total number of axles
4. Total braking capacity (electric regenerative and pneumatic)
5. Instantaneous speed and location of train.

In the SBB philosophy, the primary task of telecommunications and automatic control is to keep the traction vehicle driver continuously aware of the permissible speed in all supervised zones, and to rely on a combination of wayside signal aspects in both supervised and unsupervised zones.

Marshaling yard at Chiasso

The Chiasso marshaling yard at the southern end of the main railway route from northern and western Europe to Italy is one of the most important facilities of this type on the Continent. The yard was completely rebuilt and extended in 1964–68. It receives 70–80 merchandise trains daily; thus, a total of 3000–4000 freight cars are remarshaled in every 24-hour period. The yard comprises 23 siding tracks (Fig. 2).

One of the problems inhibiting yard expansion at Chiasso is the terrain: it lies in a narrow valley hemmed in by mountains to the east and west. Therefore it was not possible to build independent north- and southbound yards; hence, a single unidirectional yard was designed to cope with traffic in both directions. One of the principal features of the layout is a large semicircular loop that brings northbound trains from Italy along the west side of the valley and into the receiving sidings at the yard's northern end.

The original shunting capacity of about two freight cars per minute was not fast enough for the large number of trains that had to be processed by international customs examination, documentation, and rerouting. The only answer to breaking this "log jam" of traffic lay in the semiautomation of many procedures, with a long-range objective of full cybernetic control. As a first step, the yard was divided into siding groups, identified by letters, as shown in Table I.

Because of the difference between the 15-kV, 16⅔-Hz, and 3000-volt dc electric traction systems of the SBB and Italian State Railways (FS), respectively, special switching arrangements are required at the arrival sidings. In section L (Table I), for example, tracks 1 to 4 are only energized at the SBB's 15 kV, but tracks 5 to 11 can be energized at either 15 or 3 kV—the voltage being switched from the signal-control panel in the Chiasso cabin.*

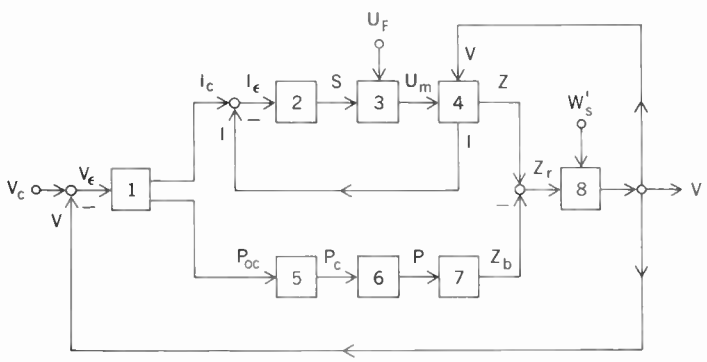
Control, supervision, and automation

A new signaling installation is now functioning in the Chiasso cabin that controls the marshaling yard and the 3-km-long approach track from Balerna (northwest of Chiasso). Siemens-built entrance/exit panels are provided for route-setting in the yard area. A main control and supervision panel is under the surveillance of the inspector in charge of operations. This panel controls the receiving sidings in group L, the block section to Balerna and to "Chiasso No. 4 signal box" (the Italian wayside station controlling the south end of the Chiasso passenger station), with override control of connections to group U, the hump in section K, and the connections in sidings in groups N, O, P, R, S, and Z (refer again to Table I).

Subsystem, or auxiliary, panels, can be operated by signalmen independent of the main control board (under supervision of the inspector), and are used for route-setting and shunting movements in various parts of the yard. One such panel controls sorting sid-

* The Swiss end of section L is energized only at 15 kV; arriving Italian locomotives (whose operation is compatible only with 3000-volt dc on the catenary) lower their pantographs, after coming to a full stop. They are then uncoupled from their trains and hauled away by a Swiss diesel-electric yard shunter; then, the FS electrics are returned by the shunter to track 11, where the catenary is energized at the required 3000-volt dc level.

[1] Regulating circuits of an automatic train control system, including speed-control elements.



Legend:

1 Speed regulator
2 Motor-current controller
3 Tap changer and transformer tappings
4 Traction motors
5 Brake controller
6 Electropneumatic pressure transducer
7 Compressed-air brake
8 Traction vehicle and train loading

I. Identification and use of Chiasso sidings

ID Letter Code (group)	Use
C	Departure sidings to the north and south
K	Hump area
L	Receiving sidings for trains from the north and south, and departure of block trains to the north
M	Sundries traffic, north–south
N	Sorting sidings for south–north traffic
O	Sorting sidings for north–south traffic
P	Customs group, with accommodation for cars destined for goods sheds 10–13 in group Z (see below)
R	Customs group, with handling facilities for fresh meat
S	Customs group, with cattle dock
T	Subsidiary sorting sidings
U	Holding sidings for cars or trains that have arrived ahead of customs-clearance documents
V	Car repair shops
Z	Sundries group, south–north

ings N and O; also the transfer sidings in group T, and the goods shed sidings in section M. Another auxiliary panel handles sorting sidings in group P, the customs group sidings in R and S, and the goods shed in group Z. A third subsidiary panel covers shunting movements in sections L and U. An independent single-panel board controls the hump and the connections to sidings N, O, and P (for humping action of cars). A second independent panel is used to control the track brakes (horizontal squeeze-action speed retarders set in the track that press against the wheel flanges). The retarders are applied automatically when a car passes over them, but they are released manually by pushbutton on the control panel.

A degree of automation is applied for hump route setting. For example, after a goods train arrives in the receiving sidings (L), the shunter examines the train, uncouples cars as necessary, and makes out a "cut card" (a sheet noting how the train is to be broken up and how the cars are to be reassembled and incorporated as part of other trains). The cut card is transmitted, via pneumatic tube, to the teleprinter office where a copy of the cut list is typed out simultaneously with the production of a punched-tape record. A copy of the typed cut list is then sent to the operating floor of the Chiasso cabin where the hump operator sets up the pushbutton program to execute the orders on the cut list. The hump-route order is set up for an entire train, and the routes are stored and executed automatically as each cut passes over the hump.

In addition to normal loudspeakers and telephone equipment in the yard area, considerable use is made of two-way radio communication between shunters on the line and the shunting locomotives in the yard. Radio communication is also provided on mainline locomotives and in freight train cabooses, although the broadest range is limited to immediate wayside station or signal-cabin areas. There is also two-way radio contact between intermediate stations along the Gotthardbahn and on-board train crews.

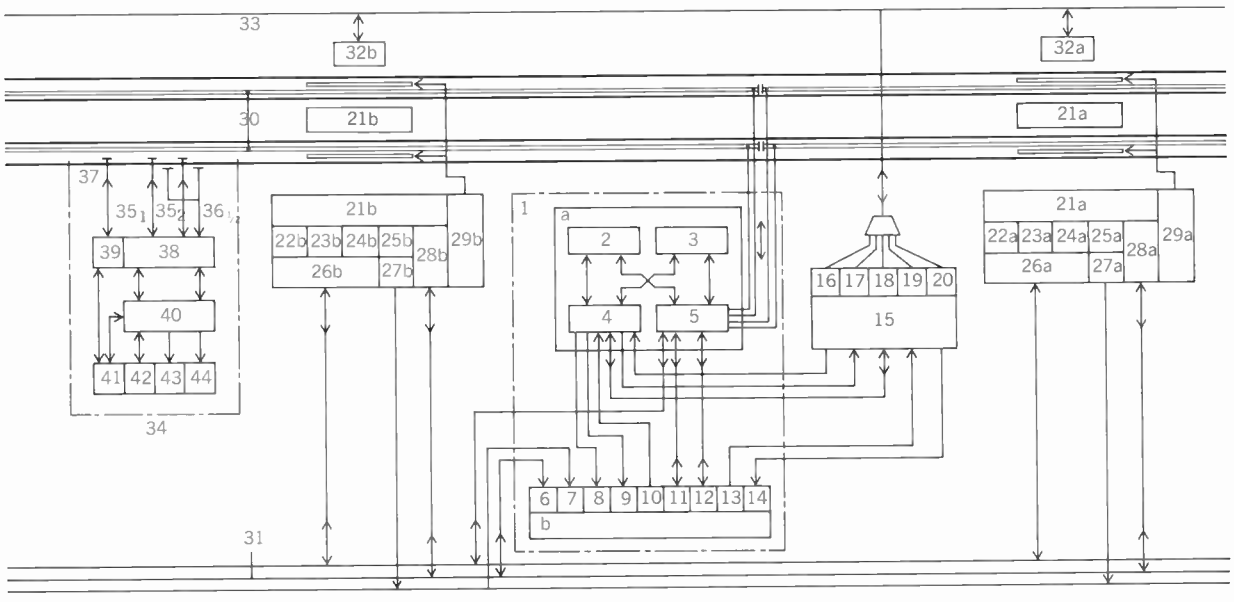
The semiautomation of the new Chiasso marshaling yard has reduced the locomotive shunting time from 10 to 15 percent, and has permitted a cut of 40 staff personnel in the yard area. The net annual savings on the new operation are estimated at about 3 million Swiss francs (about $1 million). Operation of the new yard has expedited the passage and clearance of freight trains across the Swiss–Italian frontier; this, in turn, has increased the capacity of the entire Gotthardbahn. Freight trains no longer need to be held at sidings and intermediate stations for the conventional, time-consuming clearance formalities at Chiasso.

ATO for Swiss U- and S-Bahn systems

At the present time, automatic train operation (ATO) for urban underground and mass-transit systems is in the planning and developmental stages.[3] Criteria for a comprehensive configuration for *full automatic operation* of such transit schemes could include

- Maintenance of the proper interval (headway) between trains for passenger safety
- Automatic train dispatching from terminals and

[2] View of the Chiasso marshaling yards on the Swiss–Italian border. Here, an ever-increasing degree of semiautomation in customs clearance and reassembling and routing of trains expedites the arrivals and departures of international trains.



Legend:

1. Central control with
   a: computer room containing 2–5
   b: control room containing 6–14
2. Train running—protection computer
3. Operations computer
4. Interface
5. Transmission system
6. Telephone
7. Closed-circuit television transmitted from stations
8. Computer display
9. Computer output
10. Computer input
11. Commands to and information from stations
12. Telephone link with trains through line conductor
13. Manual input to central signal box
14. Information from central signal box
15. Central signal box containing 16–20
16. Points control
17. Dwarf signals
18. Substitute signals
19. Points heating
20. Track—current circuits

21a, b. Stations containing 22–29
22a, b. Destination display and announcement
23a, b. Lighting, ventilation, escalators, etc.
24a, b. Fixed-point stop check
25a, b. Television cameras
26a, b. Transmitter
27a, b. Television transmission
28a, b. Telephone
29a, b. Emergency—stop equipment
30. Line conductor
31. Coaxial cable link for:
   telephone
   television transmission
   station supervision

32a, b. Signalling equipment outside the stations
33. Cables to signal boxes
34. Traction—vehicle equipment, including 35–44
35_1, 35_2. Aerials for data transmission
36_1, 36_2. Aerials for emergency stop at station
37. Telephone aerial
38. Data transmitter
39. Telephone transmitter
40. Processor
41. Cab
42. Automatic door—closing device
43. Visual display
44. Announcements

[3] General arrangement of a fully automatic control system (ATO) prototype design for urban rapid transit (S-Bahn) and underground (U-Bahn) railways.

intermediate stations in accordance to schedules—and the determination of optimum train running time

The Swiss philosophy in going to ATO in U- and S-Bahn operations is primarily aimed at maintaining uniform train speed with maximum reliability and safety. In densely trafficked urban and suburban commuter operations, where trains may run on headways from 1.5 to 5 minutes during peak-hour periods, and 5 to 15 minutes on off-peak hours, the main concern is not with rigid adherence to timetable scheduling, but rather with handling efficiently the *volume* of traffic by improving the throughput capacity of a line during the peak periods.

The individual wayside and on-board components shown in Fig. 3 include

1. Fixed installations in a central control room that provides necessary data for each train

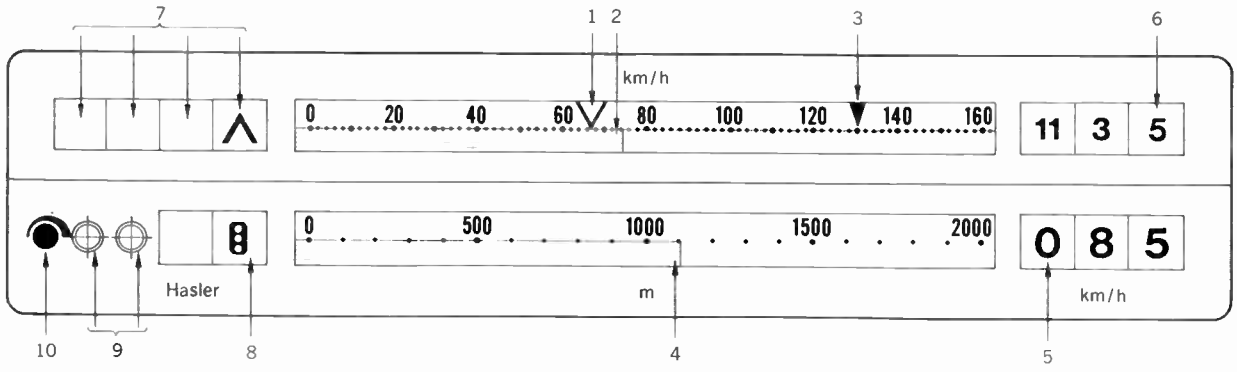
2. Transmission equipment for the transferral of information between central control and all trains operating on the system

3. On-board data-processing equipment that contains automatic monitoring/braking control capability

4. The appropriate electronic gear for centralized traffic control at stations, and also embracing compiled operational data for each station at central control, transmission equipment between central control and all stations, and EDPs at all stations

Finally, the display unit (Fig. 4), similar to the version used on the German Federal Railway (see also Fig. 3, p. 75, *Spectrum*, July 1974), has three strip indicators: one for the actual speed of the train, one for the set speed as transmitted from central control, and the third for the target distance (in meters) at which the set speed must be reduced. Note that the target speed in Fig. 4 (callout 5) is given in digital readout form. A series of symbols (7) and (8) are employed to indicate the reason(s) for the speed reduction.

However, Brown, Boveri engineers and the SBB feel that ATO is a new concept and that no urban or suburban transit system anywhere (even BART!) has had a backlog of practical experience in the routine



Legend:
1. Actual speed
2. Set speed
3. Maximum speed of traction vehicle
4. Target distance
5. Target speed
6. Time
7. Additional information, such as unoccupied stations
starting command—neutral section route display—left or right speed display—faster, slower, steady
8. Target
9. Check lamps
10. Lighting setting

[4] Display unit for traction vehicles with continuous automatic train control (CATC). This unit is similar to the type used by the German Federal Railway (DB) that was illustrated in the July *Spectrum* article (pp. 73–77).

operation of such a system. Thus, with the eventual introduction of ATO into Swiss railways, initial operation would require a motorman or operator in the train's cab, together with a visual display unit such as that in Fig. 4.

Electronic reservations

By the summer of 1970, the SBB had installed a comprehensive electronic seat and sleeping car reservation system that is essentially comparable to that installed in Sweden (see *Spectrum*, March, p. 63), Germany, and other European countries. Forty SBB railway stations and 27 private travel agencies in towns and cities throughout Switzerland are equipped to handle electronic place reservations (EPR) for train passengers bound for both domestic and foreign destinations.

The principal component in the EPR system is the 256K-byte IBM 360/40 computer in the reservation computer center. A four-disk memory storage can hold about 1 million available place reservations. If a reservation is made at any of the Swiss railway stations equipped with terminals, a seat reservation can be made quickly and efficiently.

In describing the SBB's electronic reservation system, let's take a hypothetical example:

You are a traveler who wishes to take a train from Zürich's *Hauptbahnhof* (main station, or "HB") to Como, Italy. Although it is late in September, Como is still a popular tourist area. The express train you

Transition to automation

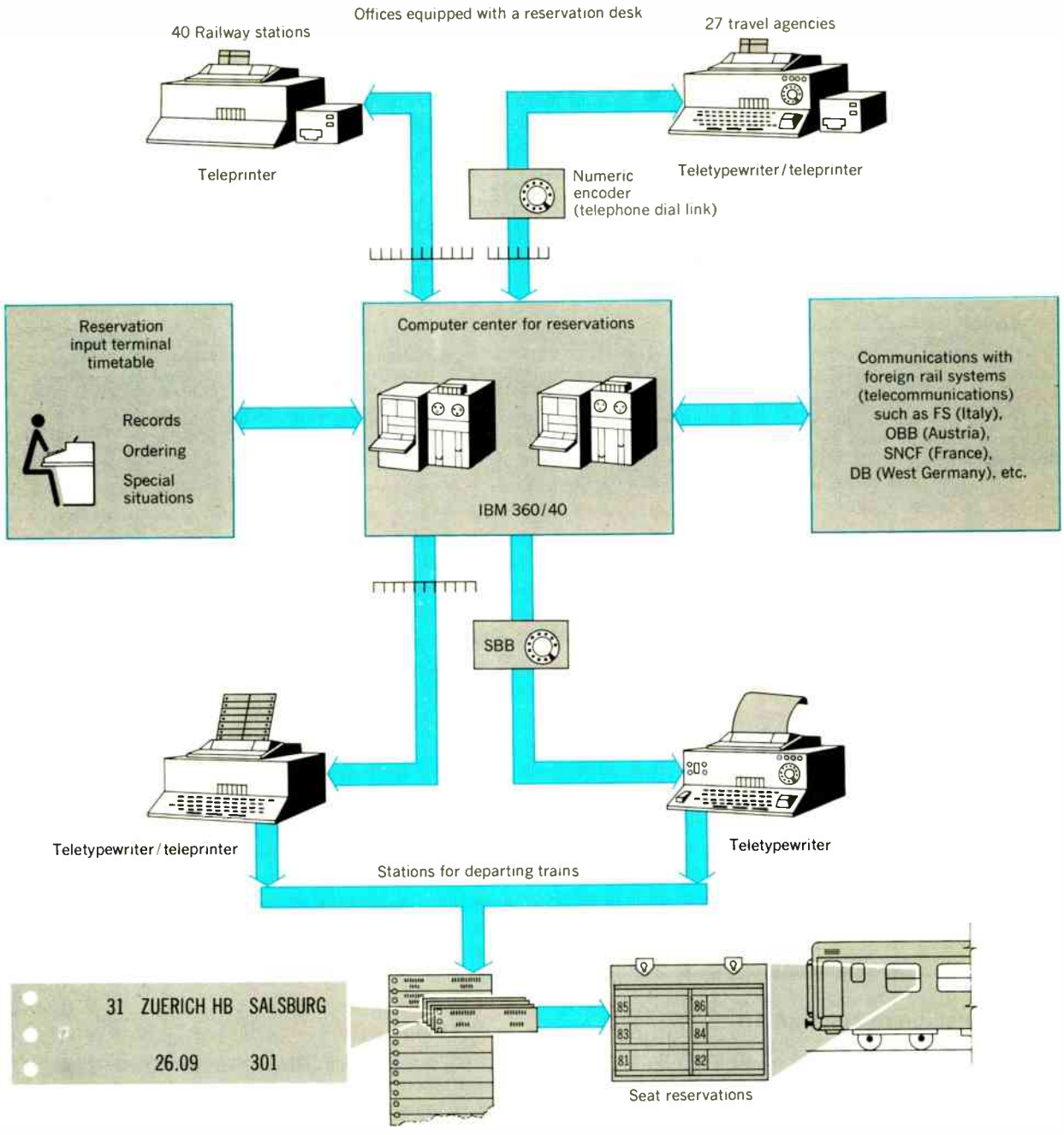
A top-priority objective of the SBB is to conduct normal railway operations with a reduced number of personnel. However, this is not a plan that would tend to increase unemployment among workers. Paradoxically, Switzerland is one of the few countries in the world that suffers from "negative unemployment"—more jobs available than there are applicants!

As its operations continue to expand, the SBB is confronted by the difficulty of recruiting new railway employees. Thus, automation is a logical solution to the problem. Telecommunications and radio control are the first steps in this direction. Fixed-station control points are being established along mainline rights-of-way. Also, contrary to the practice in the U.S., there is only one man in the cab of a Swiss locomotive—the driver; and his degree of versatility must be unusually broad. For example, a qualified locomotive driver is expected to handle any machine—from the now-antiquated Be 6/8 "Crocodile" (that was built in the 1920s) to the latest Re 6/6. In fact, my host Beat Steiner of BBC told me that the young man driving the four-current deluxe TEE train "Gottardo" (see last month's issue of *Spectrum*) might very well be next assigned to an Ac 4/7 (built in the 1930s), at the head end of a freight train.

Thus, the incentive to automate lies in the fact that the machine will not displace nonexistent personnel in unfilled jobs! Furthermore, labor unions in Switzerland do not have the powerful influence that they enjoy in the U.S. So, the resistance to automation is practically nil. Nevertheless—and perhaps again paradoxically—the Swiss, because of their difficult terrain for railway operations, place much more faith in human control than machine control for decision making in emergency situations. Therefore, complete automation will probably proceed more slowly than in neighboring countries.

The foreseeable areas in which automation will eventually play a large role are

- The projected high-speed line between Olten and Bern. This will be an additional right-of-way, with trains operating at speeds between 140 and 160 km/h. It will serve to relieve the heavily trafficked existing freight train route in this area that has interfered with passenger express trains.
- Extension of S-Bahn projects, especially in a 50-km radius of Zurich.
- The building of center-city to airport mass-transit systems, such as the new Zurich-Airport line, which will be incorporated into the SBB system.
- The introduction of automatic coupling at marshaling yards and freight depots.



[5] Automated system for seat and sleeping-car reservations presently in use at 40 railway stations and 27 travel agencies in Switzerland. Note the telecommunications links to the railway systems of bordering countries. At the lower left is a typical reservation marker that is simultaneously printed out for placement in an appropriate slot aboard the train; it corresponds with the most pertinent information on the reservation slip issued to the passenger.

want to take runs from Zürich to Milan. This, plus the fact that it is a deluxe TEE train that departs at 8:49 a.m., means that it will also be favored by business men on a one-day roundtrip between these terminal cities. Therefore, to ensure a seat, you go to the reservation window at the Hauptbahnhof and stipulate the number of your train, its scheduled departure time and day, and the number of seat reservations required. You may also specify the class* (first or second on regular trains) of the coach, whether you wish a smoking or nonsmoking car (or section in a car), and whether you prefer a window seat.

This information is keyboarded by the attendant on his terminal console, and the teletyped request is transmitted via telephone or private leased lines to the computer center. In a matter of seconds, the computer will advise whether or not your reservation can be honored. In the event there is space, you will be advised to step over to a nearby window, where a teletypewriter is printing out your *reservierungsausweis* (seat reservation card). At the same time, another teletypewriter is printing out the reservation marker (Fig 5), corresponding to your card, that will

* TEE trains carry only first-class accommodations.

The long tunnels

One of the problems in telecommunications, automatic train control, and wayside signal automation is to be found in the story of three of the world's longest tunnels—and how to ensure fail-safe operation of electronic equipments in bores of such great length. In chronological order of their construction, they are

St. Gotthard

The valleys of the rivers Reuss and Ticino form a natural north–south cleft, or pass, crossing the main Swiss Alps in one "jump." This topographic feature indicated to railway engineers—as far back as the mid-19th century—an ideal rail route for heavy goods and passenger traffic flow from the English Channel ports, and technologically oriented Germany, to the industrial areas of northern Italy, notably Milan and Turin.

The 15-km-long tunnel pierces the massifs between Goschenen, on the north, and Airolo, on the south. Its construction began in 1872 and was completed in 1881. It was, perhaps, the most daring and dramatic engineering feat accomplished in the latter half of that century.

In those predynamite days, black powder was used for blasting, and steam drills were employed for the rock boring. As might be expected in such an unprecedented project, many lives were lost among the Swiss and Italian workmen as unexpected geologic anomalies and rock spalls caused cave-ins and flooding during the nine-year-long endeavor. To ventilate the tunnel adequately for the steam traction of the day, large blower stations were installed at both portals. The first steam-locomotive-hauled train passed through the bore on January 1, 1882.

Simplon

The initial construction of the world's longest tunnel (20 km) between Switzerland and Italy began in 1898. By the turn of the century, engineers realized that the elaborate ventilation system devised for steam-locomotive traction would be impracticable for a tunnel of such great length. The Brown, Boveri Company at Baden then made plans for the implementation of three-phase ac traction. The first electrically hauled train passed through the bore on June 1, 1906.

The further extension of the electrified SBB line to Lausanne was delayed until 1923, when single-phase 15 kV, 16 2/3 Hz began to replace the original three-phase system.

Lotschberg

The third great tunnel, the Lotschberg, was authorized in June 1906. This tunnel, unlike the other two, has a pronounced "S-bend" that starts shortly south of the northern portal. The reason for this departure from the original plan was the disaster of July 24, 1908, when 25 laborers were buried under an avalanche of mud and water that cascaded upon them after the detonation of a string of dynamite charges. This accident stopped further construction for six months, pending an investigation. It was finally decided to abandon the flooded section and to divert the bore clear of the scene of the mishap by running the line eastward (hence the bend). This made the tunnel 800 meters longer than had been originally intended.

On July 15, 1913, the BLS was opened for full service from Bern to Brig, completing, via the Simplon tunnel, the link with Italy.

be placed either in a frame in your compartment's corridor or, in this case, since you are traveling in a TEE "électromotrice" six-car train set, the card will be placed in a slot directly at your seat.

Since your journey is aboard an international TEE train, you can sit back and relax, because your reservation is not subject to change or cancellation at the Italian frontier. However, if you plan to travel on a regular train whose cars will cross the border onto another country's railway and traction system; say, for example on a trip from Zürich to Salzburg, it may be necessary for the computer center to transmit a request for a continuation of your Swiss reservation into Austria; or, if necessary, a second reservation may have to be made for a seat somewhere else in the same car—or another car—when the train enters the control of the Austrian Federal Railways. In this case, the computer center transmits an inquiry to the Öesterreichische Bundesbahnen (ÖBB) processing center for verification. If the Austrian reservation is confirmed, you will be issued, in addition, a computer punch card, marked "ÖBB" giving the information concerning the status of your seat reservation when your train crosses the Austrian border.

At present, the Swiss computer center has direct telecommunications connections—in addition to the ÖBB—with the Italian State Railways (FS), the French National Railways (SNCF), and the German Federal Railway (DB).

Now, let's say that, instead of being at Zürich's HB, you are closer to a private travel agency that has a computer terminal for handling reservations. No sweat. The same information is keyboarded into a teletypewriter/teleprinter unit and is transmitted to the computer center just as if you were at the railway station. Your confirmation will be relayed to the travel agency in a minute, or less.

And now, a look ahead

Thus far, in our international railway epic we have covered the rail systems of three countries: Sweden, West Germany, and Switzerland. Our next episode will cover the French SNCF, the only country to utilize commercial frequency (50 Hz) over a portion of its electrified system. So, we have a vicarious date, with Paris as the rendezvous, in a forthcoming issue of *Spectrum*.

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'Fax' in the home: looking back and ahead

Great hopes are held for facsimile for consumer use. Will it "go broadcast" again, as it did 35 years ago?

When Scotsman Alexander Bain invented, in 1842, his system of synchronized electric clocks to send crude graphic messages over telegraph wires, no one could foresee where this discovery would lead. It took roughly half a century for the basic concept to evolve into a means for sending pictures by wires and an additional half century for it to inspire a unique broadcasting venture aimed at printing the daily newspaper right in the customer's home. "Facsimile"—or "fax," as it came to be known—came remarkably close to preceding both hi-fi music and television into the nation's living rooms, and, although the "electronic newspaper" concept failed to gain public approval, its eventual debut remains within the realm of probability.

It all began in the mid-1930s, with a handful of experimenters who were convinced that fax was the natural successor to the daily newspaper. Although radio had become established as *the* home entertainment medium, and despite its potential for rendering the printed newspaper obsolete, the latter was still being delivered daily— by car, bike, and on foot—to millions of homes across the nation. The reason, apparently, was that people still craved pictures and visible records of events, not to mention such extras as crossword puzzles, comic strips, printed recipes, and illustrated ads. What's more, you could not wrap fish in radio waves.

But fax could readily fill the gaps in radio's capabilities. So said its proponents, some of whom had already proved their point in limited experiments.

The concept of fax broadcasting of printed news was probably originated by C. F. Jenkins in 1924. He proposed to use fax to distribute news headlines in advance of the detailed news, which would continue to reach the home via newspaper. Another proposal, made at that early stage, was to use fax broadcasting merely to deliver daily printed program schedules to radio listeners.

The earliest fax broadcast venture was that of Austin Cooley in 1926. He managed to persuade more than two dozen broadcasters to experiment with a system he had devised, called "ray photo." The system employed a unique recording technique using a corona discharge. It worked, but was soon to be abandoned because of its very low speed and its production of noisy signals that offended the ears of radio listeners. A few years after Cooley's experiment, both RCA and General Electric ran field tests of broadcast fax receivers.

Meanwhile, significant advances had been made in the use of fax as the transmission medium for news photos and weather charts, and, by the mid-1930s, the worldwide transmission of photos by facsimile—via wire and radio—had been developed to a high degree of refinement. The Associated Press had, in fact, made such a phenomenal success of its national "wirephoto" network, that four new development and manufacturing firms were formed almost simultaneously to meet the sudden demand for apparatus. Finch Telecommunications and Radio Inventions were founded by W. G. H. Finch and J. V. L. Hogan, respectively, the latter a well-known TV pioneer. About the same time, Austin Cooley founded Times Telephoto Equipment (later renamed Times Facsimile), and Acme Newspictures established its own manufacturing facility. Bell Telephone's Western Electric was already supplying apparatus for the AP picture net.

Very soon after the news-picture networks had begun to flourish, fax's "grand" experiment officially got underway. The new watchword was *broadcast*, implying the delivery of daily newspapers by radio-facsimile, right into the "subscriber's" own living room. In the eyes of the general public, it was a rather fanciful "blue sky" concept for its day. But not to technologists like Finch, Hogan, and RCA's illustrious fax development team, all of whom felt that it was both technically and economically feasible and therefore ripe for launching.

Daniel M. Costigan Bell Laboratories

The names of the game

As it evolved, facsimile took various names, stressing usually its specific use at the time the name was given. There were "copying telegraph" and "picture telegraph," for example; and, later, "phototelegraphy" and its complement "telephotography." At some point, the word 'facsimile' was introduced, derived from the Latin *fac simile* meaning 'make similar,' which is basically what this technology of sending graphic messages over the wire is all about. Thus, "facsimile telegraphy" was picked up. When broadcasting got underway, there came "photo radio" and "radio facsimile" too. But "facsimile" was to stick, followed by "fax," its abbreviated phonetic successor, which holds to this day.

The first actual "deliveries" of newspapers via commercial radio broadcast stations were made in 1937, by KSTP in St. Paul, Minnesota; WGH in Norfolk, Virginia; WHO in Des Moines, Iowa; and WOR in New York. The very first experimental fax broadcasting license had been granted in September of that year, to a New York noncommercial station, W2XBF, owned and operated by W. G. H. Finch, who had designed the transmitters and receivers that were to be used in most of the other trials.

The idea caught on rapidly, and by the end of that year there were a total of nine commercial stations licensed for experimental fax transmission.

In 1938, the St. Louis *Post-Dispatch* joined the list of pioneering experimenters, and Chicago's WGN, Cincinnati's WLW, and Cleveland's WHK joined WOR to form the first facsimile broadcast network. By the spring of that year, the number of experimental fax broadcasters had more than doubled, and interest within the broadcasting community continued to mount.

Broadcasters engaging in experimental fax transmissions were required by the Federal Communications Commission (FCC) to install a minimum of 50 receivers (or receiver accessories) in selected residences within the area served by the station. Thus, by early 1939, there were *at least* 1000 private homes throughout the country equipped with fax receivers. Most of these early receivers were provided by Finch Telecommunications and RCA, with the broadcasters footing the bill.

By the close of the thirties, there were nearly 40 commercial stations regularly broadcasting fax newspapers, and by 1941, more than 10 000 fax receivers had been sold for home use—a phenomenal number for a single application, even by today's standards. The receivers retailed in the range of $50 to a little over $100, which was also surprisingly moderately priced, even allowing for the higher value of the dollar at the time. One of the more popular receivers, a radio attachment designed by Finch Telecommunications and produced and marketed by Crosley Radio, was purchasable in some of the country's large department stores—Macy's in New York City, for example.

But in spite of the apparent success of the venture, there were definite signs, by late 1940, of a declining public interest. One reason was that the price of the home receivers, fair as it seemed, was still more than the average family could really afford in the depressed economy of the 1930s, particularly for something that still had to be regarded as a novelty, despite its practical potential. On top of that, the apparatus was slow, somewhat noisy, and perhaps not as reliable as one might have liked it to be.

Another problem was that no agreement had been reached on what constituted the best printing process. In some machines, the mechanism was complex and wasteful of materials, and in others, it was simpler, but produced a copy of marginal quality or required a very special type of paper, or both.

Meanwhile the United States had gone to war and the emphasis in fax development had shifted to military applications. In its new role, fax overcame some of its prewar shortcomings and matured sufficiently

(Continued on page 81)

Fax: specs and projections

The fax broadcasting venture of the '30s and the '40s (described in detail by Daniel M. Costigan in the accompanying article) was but one of the many faces facsimile communication has shown in its long and somewhat capricious history. It assumed its present role as a standard business communications tool in 1962, with the official opening of the telephone dial network (via appropriate interfaces) to customer-provided fax terminals. It has matured steadily in this latest role, finally achieving status as an industry in its own right.

Specifications of fax apparatus

Fax transmitters and receivers are offered today by many vendors. Applications vary from weather-map transmission to relay of police records and fingerprints. Specifications, too, vary accordingly. While an average office document can require a vertical resolution no greater than 60 to 90 lines per inch (lpi), upwards of 200 lpi is needed for police transmission of fingerprints. Scanning and transmission speeds are of great concern as well. In this respect, there is a marked difference between an analog fax apparatus, where about three to six minutes are required for a transmission of an 8.5- × 11-inch standard office document, and its digital counterpart, doing the same job in a fraction of a minute.

In an analog fax system, there is normally a trade-off between the scanning speed and the resolution. Some customers would prefer the faster machines—i.e., equipment with a three-minute or less scanning time for a standard page, while others may assign top priority to resolution. Some vendors, however, provide a selection of a few resolution and speed values in one transceiver (a combined transmitting and receiving apparatus).

About the highest transmission speed demonstrated to date in a digital fax system via voice-grade circuits is 15 seconds per "average" standard office document, and this has been achieved through use of a variable-velocity scanning technique developed by Comfax Communications Industries in equipment now commercially available from EAI. Similarly, digital data-compression techniques, like those used in both the Dacom and Rapifax systems, permit increased scan rate with no sacrifice of resolution.

To convert the information of the scanned page into a signal that can be transmitted over regular telephone lines (the so-called voice-grade circuits), and vice versa, a modulator and demodulator (modem) is required. Most modem equipment is designed for use on voice-grade circuits, but modulation

Gadi Kaplan Associate Editor

I. Typical facsimile transceivers and their specifications

Manufacturer	Model No.	Max. Page Size		Min. Scan Time Per Page, s	Transmission Mode			Max. Resolution		Scan. Tech.
					Digital	Analog				
		Input, in × in	Output, in × in		kbits/s	Bandwidth, kHz	Modulation	Horiz. pel/in	Vert. lines/in	
Alden	11	24 × cont.	11 × cont.	408	—	1.2	VSBAM	—	166	
	18	18 × 24	18 × cont.	132	—			—	166	
	600	6 × cont.	6 × cont.		—			—	96	
Dacom	300	25 × 24	25 × 24	360	150	—	—	2000	1200	PE
	410	8.5 × 14	8.5 × 14	40	4.8	—	—	200	200	PE
	412	8.5 × 14	8.5 × 14	40	32	—	—	200	200	PE
	430	8.5 × 14	8.5 × 14	40	4.8	—	—	200	200	PE
	441	8.5 × 14	8.5 × 14	40	4.8	—	—	200	400	PE
Datalog	Message fax	8.5 × 14	8.5 × 14	250	—	—	VSBAM	—	91	PE
	Digifax I	8.5 × 11	8.5 × 11	210	9.6	—	—	—	96	PE
	MX-T, R	8.5 × 14	8.5 × cont.	210	—	—	AM	—	91	
	501	22 × 15.4	22 × 15.4	180	—	—	AM	—	600	
	DDR	24 × 17	24 × 17	1200	10.8	—	—	—	—	
EAI	FAX-1 15	9.5 × 14		*15	9.6	—	—	—	192	FS
	FAX-1 30	9.5 × 14		*30	4.8	—	—	—	192	FS
	FAX-1 60	9.5 × 14		*60	2.4	—	—	—	192	FS
Faxon	811	8.3 × 10.8	8.5 × 11	32	—	—	FM		100	FS
Graphic Sciences	dex broadcaster	9 × 14	9 × 14	180	—	1.4	VSBAM	—	88	PE
	dex I	9 × 14	9 × 14	360	—	1.4	VSBAM	—	88	PE
	dex VI	9 × 14	9 × 14	360	—	1.4	VSBAM	—	88	PE
	dex VII	9 × 14	9 × 14	360	—	1.4	VSBAM	—	88	PE
	dex IX	9 × 14	9 × 14	240	—	1.4	VSBAM	—	62	PE
	dex 120	9 × 14	9 × 14	120	—	1.4	VSBAM	—	62	PE
	dex 180	9 × 14	9 × 14	180	—	1.4	VSBAM	—	88	PE
	dex 181	9 × 14	9 × 14	180	—	1.4	VSBAM	—	88	PE
	dex 182	9 × 14	9 × 14	180	—	1.4	VSBAM	—	88	PE
	dex 185	9 × 14	9 × 14	360	—	1.4	VSBAM	—	88	PE
	dex 580	9 × 14	9 × 14	180	—	1.4	VSBAM; FM	—	88	PE
	dex 3000	8.5 × 11	8.5 × cont.	180	—	1.4	VSBAM	—	88	PE
	dex 3400	8.5 × 14	8.5 × cont.	180	—	1.4	VSBAM; FM	—	88	PE
	dex 4100	8.5 × cont.	8.5 × cont.	120	—		VSBAM; FM	—	64	PE
3M	VRC II	8.5 × 14	8.5 × cont.	240	—		FM	96	96	
	VRC 600	8.8 × 14	8.5 × cont.	240	—		FM	96	96	
	VRC 603	8.5 × 11.8	8.5 × 11	180	—		FM	96	96	
Muirhead	180		9.8 × cont.	360	—	0.8	FM		90	
	240		9.8 × cont.	246	—	0.8	FM		90	
	300		9.8 × cont.	196	—		VSBAM		90	
	500		9.8 × cont.	120	—				90	
	K-351-D/F (Tr)	8 × 10	8 × 10	820	—	1.3	VSBAM		200	
	K-300-D/F (Rec)	8 × 8	8 × 8	820	—	1.3	VSBAM		200	
	Mercury IV			60	—	0.3	FM		90	
Rapifax	100	8.5 × 14	8.5 × 14	35	2.4/4.8	—	—	200	200	PE
Stewart Warner	Datafax 150	8.5 × 11	8.5 × 11	540	—	1.0	FM		137	
	Datafax 180	8.5 × 11	8.5 × 11	360	—	1.0	FM		96	
	Datafax 240	8.5 × 11	8.5 × 11	270	—	1.0	FM		96	
	Datafax 360	8.5 × 11	8.5 × 11	180	—	1.0	FM		90	
	FT(R) 3628A(B)	8.5 × 11	8.5 × 11	180	—		AM		96	
	FT(R) 9095A(B)	8.5 × 11	8.5 × 11	60	—		AM		96	
Telautograph	300D	8.5 × cont.	9 × cont.	180	—	2.0	VSBAM		83.3	PE
	300AD	8.5 × cont.	8.5 × cont.	180	—	2.0	AM		83.3	PE
	300	8.5 × cont.		180	—				83.3	PE
	900	8.5 × cont.	8.5 × cont.	72	—	9.1	AM		100	PE
Victor Graphic Systems	3618	8.5 × 11	8.5 × cont.	100	—		FM		100	
	4828	8.5 × 11	8.5 × cont.	138	—		FM		100	
	6030	8.5 × 11	8.5 × cont.	108	—		FM		100	
	9045	8.5 × 11	8.5 × cont.	72	—		FM		100	
Xerox	Telecopier 400	8.5 × 11	8.5 × 11	240	—	2.5	FM	96	96	PE
	Telecopier 400-I	8.5 × 11	8.5 × 11	240	—	2.5	FM	96	96	PE
	Telecopier III	8.5 × 11	8.5 × cont.	240	—	2.5	FM	96	96	PE
	Telecopier 410	8.5 × 11	8.5 × 11	240	—	2.5	FM	96	96	PE

techniques vary. While FM or vestigial sideband AM is preferred by manufacturers of conventional analog equipment, digital data-compression techniques are fast catching on. But equipment using the latter techniques is naturally more expensive.

Coupling to the phone lines in facsimile transceivers is normally accomplished either through a specific data-access arrangement (DAA), usually leased from the phone company, or, as is the case in more conventional analog equipment, through acoustic coupling to the telephone receiver.

Purchase price and monthly rental rates vary widely. Generally, the more expensive the unit becomes, the more likely some special features are offered with

Record. Tech.	Sync.	Data Comp.	Error Correct.	Automatic Trans.	Automatic Rec.	Line Coupl.	Power W	Biggest Dimension, in	Weight, lbs	Purchase Price/ Monthly Rental, dollars	Options
El		—	—	—	√	A/DAA/HW	700	50 (h)	613		Auto. feeder
El		—	—	—	√	A/DAA/HW	700	55 (h)	809		Auto. feeder
El		—	—	√	√	A/DAA/HW	150	21 (d)	125		
Ph	—	√	√			Modem		64.5 (h)			
Es	—	√	√	√	√	DAA	1150	39 (h)	375	13 000/510	Auto. feeder
Es	—	√	√	√	√	DAA	1150	39 (h)	375	14 130/520	Auto. feeder
Es	—	√	√	√	√	DAA	1035	39 (h)	375	14 920/545	Auto. feeder
Es	—	√	√	√	√	DAA	1150	39 (h)	375	12 700/470	Auto. feeder
El	PG	—	—	—	—	HW	250	21.3 (w)	78		
El	PG	—	—	√	√						
		—	—	—	—						
Ph		—	—	—	—		2300	47.5 (h)			
		√	—	—	—		1200	47.5 (h)			
Es	—	√	—			DAA	920	43 (h)	300	9800/300	Auto. feeder
Es	—	√	—			DAA	920	43 (h)	300	9800/300	Auto. feeder
Es	—	√	—			DAA	920	43 (h)	300	11 300/300	Auto. feeder, Auto. answer
Es	—	√	√	√	√	DAA	1150	40 (w)	200		
Sp	CL	—	—	—	—	HW/DAA	180	22 (w)	47	9900/190	
Sp	CL	—	—	—	—	A	180	22 (w)	47	1200/57.5	
Sp	CL	—	—	—	—	A	180	22 (w)	47	1200/57.5	
Sp	CL	—	—	—	—	DAA	180	22 (w)	47	1200/57.5	
Sp	CL	—	—	—	—	A	180	22 (w)	47	1200/57.5	
Sp	CL	—	—	—	—	A	180	22 (w)	47	4000/85	
Sp	CL	—	—	—	—	A	180	22 (w)	47	4000/85	
Sp	CL	—	—	—	—	DAA	180	22 (w)	47	4000/85	
Sp	CL	—	—	—	—	DAA	180	22 (w)	47	4000/85	
Sp	CL	—	—	—	—	DAA	180	22 (w)	47	4700/95	
Sp	CL	—	—	√	—	A	180	22 (w)	47	4600/95	
Sp	CL	—	—	√	√	DAA	180	24.5 (w)	58	5400/91.5	
Sp	CL	—	—	√	√	DAA	180	24.5 (w)	60	6000/100	
Sp	CL	—	—	√	√	DAA	300	34 (w)	75		
Es	CL	—	—	√	√	DAA	275	24 (w)	59	3195/90	Auto. feeder
Es	CL	—	—	—	√	DAA	275	24 (w)	59	2995/85	
Es	CL	—	—	—	—	A		18.4 (w)	18	1645/57.5	
El	PG	—	—	—	√			16 (w)	87		
El	PG	—	—	—	√			16 (w)	87		
El	PG	—	—	—	√		100	16 (w)	87		
El	PG	—	—	—	√	HW		16 (w)	87		
Ph	CL	—	—	—	—		100	23 (w)	75		
Ph	CL	—	—	—	—		370	50 (h)	376		
El	CL	—	—	—	—			16.8 (d)	80.5		
Es	—	√	—	√	√	DAA	1035	42 (h)	375		
El	CL	—	—	√	√	HW	375	21 (d)	45		Auto. feeder
El	CL	—	—	√	√	HW	375	21 (d)	45		Auto. feeder
El	CL	—	—	√	√	HW	375	21 (d)	45		Auto. feeder
El	CL	—	—	√	√	HW	375	21 (d)	45		Auto. feeder
El	PG/CL	—	—	√	√	HW		19.5 (d)	160		Auto. feeder
El	PG/CL	—	—	√	√	HW		19.5 (d)	163		Auto. feeder
El	CL	—	—	—	—	HW	700	19 (d)	136	6000/	
El	CL	—	—	—	√	HW	700	19 (d)	136	6000/	
El	CL	—	—	—	√	HW	700	19 (d)	136	6000/	
El	CL	—	—	—	—	HW	700	19 (d)	136	6000/	
El	CL	√	—	√	√	HW/DAA		18.5 (d)	123	5500/270	Auto. feeder
El	CL	√	—	√	√	HW/DAA		18.5 (d)	123	5600/280	Auto. feeder
El	CL	√	—	√	√	HW		18.5 (d)	123	5700/290	Auto. feeder
El	CL	√	—	√	√	HW		18.5 (d)	123	5900/320	Auto. feeder
Sp	CL	—	—	—	—	A		18.4 (w)	18	1540/60	
Sp	CL	—	—	—	—	A		30 (d)	65	1540/60	
Me	CL	—	—	—	√	A/DAA		19.8 (w)	46	1825/62.5	UA
Sp	CL	—	—	√	√	A	500	30 (d)	65	4580/100	

it—error correction, automatic transmission and/or reception, line-fault indication, automatic document loading, automatic cutting of the received page to the required length, to mention but a few. Some vendors even offer a scrambling circuit as an option.

The table above represents a typical segment of facsimile transmitters and receivers available today. It is by no means a comprehensive one. Very specialized equipment has been omitted.

What's in the table?

Following the *manufacturer's name* and the *model identification number*, the apparatus' characteristics gradually reveal themselves. (*Continued on next page*)

In the *Max. page size* column, "*Cont.*" stands for a continuous reel of paper, automatically cut to length. The *Min. scan time per page* column refers to the fastest scanning for a maximum page size. Asterisks indicate a statistical average of the scanning time computed for ten or more office documents of the "standard" 8.5- × 11-inch dimension, the scan speed being variable according to the printed message.

In the *modulation* column, *VSBAM* is the abbreviation for vestigial-sideband amplitude modulation. *Horiz.* is, of course, horizontal, but *pel/in* is a resolution unit of picture elements per inch. Vertical is abbreviated as *Vert.* and *Scan. tech.* is simply the scanning technique that is used in the apparatus. This technique can be either purely photoelectric (*PE*) or a cathode-ray tube flying-spot technique (*FS*). But the recording technique—*Record. tech.*—refers to any of the following: electrostatic (*Es*), electrolytic (*El*), photographic (*Ph*), the technique of electrical sparking (*Sp*), and that of a mechanical impact (*Me*).

Sync. stands for synchronization between transmitter and receiver, which is essential in analog facsimile. *PG* is the conventional synchronization by the power-grid waveform, while *CL* stands for an internal clock or frequency standard. Among the extra features available in some fax apparatus are *data comp.* or data compression; *error correct.*, error correction; and *Automatic trans./rec.*, automatic transmission or reception. Availability of any such feature is indicated by a ✓ sign.

Line coupl. is line coupling, where *A* stands for an acoustic coupler to the telephone apparatus, and *DAA* is a data-access arrangement. *HW* is simply hard wiring to a telephone line dedicated to facsimile communication. In the *options* column, *UA* means unattended answering.

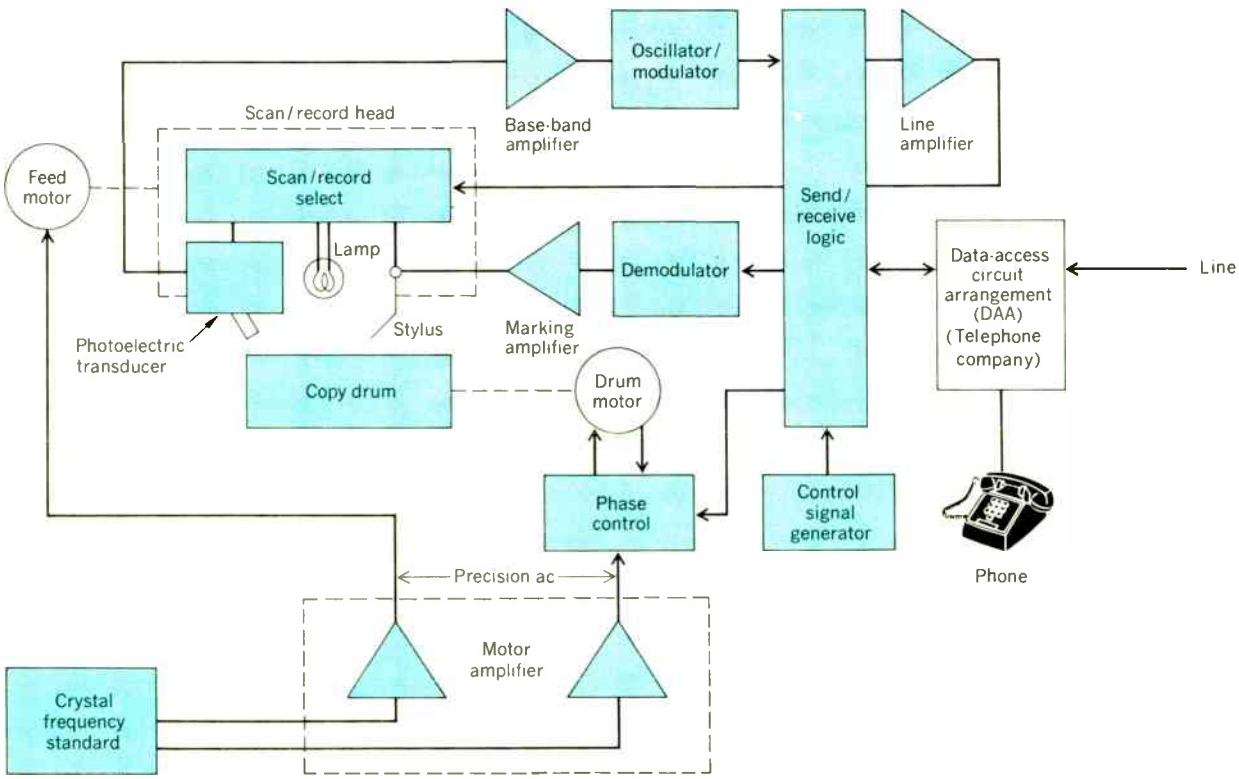
Once aware of the general facsimile picture, one can get a better insight of the technology involved, by analyzing the functioning of a typical analog fax transceiver.

Analog fax transceivers—how they work

The common phone-coupled analog fax transceiver, designed as a business communication tool, is made of the following basic building blocks: (1) A scanning

[1] A phone-coupled fax transceiver like this one from Graphic Sciences (left), an increasingly common sight in business offices, may be tomorrow's newest rage in home appliances.

[2] Functional diagram of a typical phone-coupled analog fax transceiver. Coupling to phone lines can be made via a data access arrangement (DAA), provided by the phone company, or via an acoustic coupler, normally supplied by the terminal vendor.



and recording mechanism. (2) A modulated oscillator and demodulator circuits. (3) Control logic. (4) Frequency standard for synchronization of transmission and reception. (5) A circuit coupling the transceiver to phone lines.

The scanner signal is used to modulate the oscillator (AM or FM) within the conventional telephone circuit bandwidth (roughly, 0.3 to 3.0 kHz). The typical system transmits at a speed of 180 scan lines per minute. At that speed, the system is able to resolve about 100 picture elements (pels) along the scan axis (i.e., horizontally across the scanned document). At a vertical resolution of 100 scan lines per inch, an 8.5- × 11-inch document will be transmitted in about six minutes.

Initial "phasing" of the "send" and "receive" drums is achieved by the latter being held at a lower or higher speed until a received and a locally generated end-of-line pulse occur simultaneously. Both receiver and transmitter will now remain aligned through the transmission. To ensure alignment, the motors are energized from precision power supplies. Recording may be by one of several processes—e.g., electrolytic, electroresistive, electrostatic, electropercussive—all of which result in direct, permanent recordings, requiring no subsequent processing.

Future comeback of home fax?

With ever expanding markets for fax apparatus and increased sophistication of the equipment manufactured, there is still a question to be asked whether the fax broadcast venture should be regarded as having died or as merely having become dormant.

An intriguing question in this respect, as raised by Daniel Costigan, is whether the failure of the fax news broadcast venture some 25 years ago was just an error in timing on the part of its promotors. According to Mr. Costigan, it is entirely possible that had that venture endured until TV's initial novelty had worn off, it might have survived. Now that facsimile has become an industry in its own right, with several large companies lending their developmental and promotional skills, the potential for fax as a home entertainment and information medium is, according to Mr. Costigan, as strong as ever.

Mr. Costigan also maintains that immediate possibilities exist for home fax broadcast. One such possibility is that of dialing up a special phone number, or a CATV channel, to receive up to the minute news and pictures in any one of a dozen different categories.

In addition to that scheme, Mr. Costigan also claims it is even possible that commercial FM radio may yet serve as a fax broadcast medium, as originally planned. As has recently been verified, the Federal Communications Commission's standards for that service of an FM broadcast are still on the books, and at least one enterpreneur is currently taking advantage of that fact. John Porterfield, a veteran communications engineer, has been broadcasting fax experimentally from New York's WNYC-FM for the past three years.

In light of this, the chances are good, according to Mr. Costigan, that the survivors of the ill-fated grand experiment of the '30s and '40s may yet see some of their high hopes and promises fulfilled.

(Continued from page 77)

in the first three years of the war for the broadcasting industry to begin preparing for phase II of the grand experiment.

Under the guidance of Hogan and Finch, the fax industry and the broadcasters agreed upon a set of standards under which the fax-in-the-home venture would be resumed. The FCC consented to issue official operating standards, and General Electric was licensed under Hogan patents to produce the initial run of required standard transmitters and receivers. The choice of FM broadcasting (advocated by Finch) and Hogan's improved electrolytic recording technique were definite improvements over the chaotic situation of the '30s.

Phase II got underway about 1947 with test transmissions by Finch's commercial FM station WGHF in New York and by the *Miami Herald* via its WQAM-FM outlet. Meanwhile, interest had been stimulated among a number of other FM radio stations as well as several major newspapers. Two additional manufacturers had also joined the fold—Stewart Warner and Alden Products. The former had drawn up plans for a line of broadcast receivers that included special units for installation in public places, while Alden was to manufacture a variety of fax devices of its own design. Finch Telecommunications, already in the market, was preparing for high-volume production of home receivers designed to the new broadcast standards.

The FCC's fax broadcast standards went into effect in June, 1948, by which time four of the country's leading newspapers—*The Chicago Tribune*, *The New York Times*, *The Philadelphia Inquirer*, and *The Miami Herald*—were already on the air with experimental fax editions. *The Inquirer* had established a regular 8-page weekly edition, and *The Herald* was transmitting five editions daily! The latter leased receivers to hotels for $85 a month. By July of that year, a total of 11 stations were authorized to broadcast fax "programs" experimentally.

Until late in 1949, there still seemed ample reason, in some quarters, to believe that the fax radio newspaper was here to stay. Receiver manufacturers were confidently predicting that, with increased production, recorder attachments for existing FM radios would soon be retailing for under $100, comparable to prewar pricing. But within a matter of months, whatever optimism still existed began rapidly to fade, and by early 1950, it was pretty much all over. Two decades of dreams and innovations had evaporated with the failure of a venture that, for a while, seemed to have everything going for it.

It was not as if the participants in the experiment had been oblivious to the advent of commercial television. Indeed, they had already foreseen it in the '30s and were well aware of its implications regarding the fax venture. But they had clung stubbornly to the idea that the public would not be content with television's fleeting images, that the need would remain for a printed communications medium, and that facsimile and television could therefore coexist. Unfortunately, they had misjudged the public's elusive tastes.

It is a measure of fax's durability that, of all the major participants in the venture, only one name was subsequently to disappear from the roster, and—iron-

Early fax broadcast apparatus

In the fax broadcast experiment of the thirties, the transmitted original news page was a paste-up of hand-typed text and original photographs and line drawings (including ad copy). This material was intermixed as on a conventional newspaper page, but with the content judiciously abridged to fill a page measuring about 8½ × 11 inches. For transmission, this paste-up master was wrapped around a drum of an optical scanner, and scanned "lathe style," with a laterally moving scan head, as the drum revolved at about 360 r/min. The scanner's baseband output modulated a subcarrier, which, in turn, amplitude-modulated the transmitted carrier of the broadcast station.

The combination of a comparatively low scanning speed and a resolution of about 100 picture elements per inch of scan stroke, permitted the use of a subcarrier that was within the audio range, and which could therefore merely be substituted for the normal audio input to the transmitter. Line-by-line pulses were provided to sync the receiver to the transmitter.

The fax receiver generally consisted of an existing standard broadcast receiver with a graphic recording accessory. It was a kind of nocturnal robot that would stand idle by day and go into action after the household retired for the night. In the recorder, a metal stylus connected to the receiver output and arranged to effect a sweeping motion, visibly reconstructed the transmitted baseband analog, line-by-line, on electrosensitive paper fed from a roll within the machine. For compactness, some receivers were designed to record on 4-inch-wide paper. Obviously, the stylus stroke length and the paper feed rate in these mini-receivers had to be proportionately adjusted so that the received page, while smaller than the transmitted master, was nonetheless complete and geometrically undistorted.

Regardless of the design of the fax receiver, the received copy was immediately visible upon recording (no subsequent processing was required). This copy was essentially permanent, and, if reception was good, had generally good contrast and crispness. But facsimile reception was vulnerable to all of the same transmission impairments and circuit malfunctions that occasionally plagued normal audio reception via AM radio—fading, "static," drift, beat frequency howls, etc.—and, under adverse conditions, the copy quality suffered accordingly.

This ad appeared in a 1939 issue of *Radio News*. $49.50 and a little assembly work were all that was needed to convert any FM receiver to a radio-operated home "printing press."

ically—it was that of Finch Telecommunications, which had been bought out and renamed, and which, for reasons best known to its new managers at that time, went out of business shortly thereafter. Finch himself had left his firm in the 1940s to serve as a U.S. Naval officer, and had returned to it briefly after the war—just long enough to help to guide its reconversion into a civilian product line.

Radio Inventions changed its name to Hogan Faximile, which continues to exist as a subsidiary of the Teleautograph Corporation; and the Alden name continues to be carried on a broad line of commercial fax equipment now produced by a spin-off of the original firm.

Of the larger participants, GE terminated its subcontracting role upon fulfillment of its initial contract, and has not since been active in the fax field. RCA, on the other hand, while not actively promoting fax, has by no means written off its potential as a communications tool. Stewart Warner, which had been only briefly involved in the broadcast venture, has since returned to the production of commercial fax apparatus. As for the participating broadcasters and newspapers, they merely returned full time to vending their services in more conventional ways.

Daniel M. Costigan (M) has been an information-systems analyst at Bell Labs since 1962, at which time he helped to develop the Bell System's pioneering microfilm program for engineering drawings. Mr. Costigan's interest in facsimile communication goes back many years, but his first real involvement with it was in 1964, when Bell Labs began to assess its potential to speed the internal flow of graphic engineering documentation. The author is chairman of the joint National Microfilm/Electronic Industries Association Microfilm-Facsimile Standards Committee (EIA TR 29.1), and a member of the National Microfilm Association Publications Committee. He is author of a book on fax, and has published several articles and papers on various technical topics during the last 20 years. Mr. Costigan received a B.S. degree from New York University in 1964.

Refuse turns resource

Diverted from land fills to hammer mills, municipal waste becomes an economic energy resource

Gasoline, heating oil, and electric bills in recent months all testify to the inflationary effect of unchecked demand on limited supply. Short-term, workable solutions to the problem seem tangled in a web of expert opinion. Scientists argue the merits of nuclear fusion, solar power derived from synchronous satellites, or the hydrogen economy. Environmentalists champion austerity, conservation, and a curtailment of open-ended public consumption. But at least part of the answer could lie outside Buck Rogers and bureaucratic thinking in the earthy, engineering realm of bootstrapping. The municipal waste of industrial nations—long relegated to rat-infested land fills—can be diverted to fueling electric power and steam plants. Practical, workable systems already exist, while others are under advanced development. And it's a safe bet that no one need worry about running out of trash!

Today the U.S. produces approximately 0.9 tonne of solid waste per person per year[1,2] (or over 180 000 000 tonnes total) and this quantity has been growing, until recently, at an annual rate of 5 percent. It was estimated, and later verified by research (carried out at the University of Louisville), that some 50 to 60 percent of this waste is combustible.[2] Thus, the potential exists for burning at least 90 000 000 tonnes of refuse each year. The heat content of this fuel, when properly classified, will vary with the characteristics of the local waste itself, but as a general rule the heat content of two tonnes of refuse fuel is equivalent to that of one tonne of average-grade coal.[3] By simple arithmetic, recovery of energy from this waste would be equivalent to burning 45 000 000 tonnes of coal, but if the fuel needed to mine and haul this quantity of coal to urban areas is considered, the refuse substitute becomes an even more impressive energy source (1.05×10^{18} joules potentially available from refuse versus 78.4×10^{18} joules total U.S. energy consumption in 1973). The Environmental Protection Agency claims there may be almost $1 billion worth of energy waiting to be released from solid waste every year.

John E. Heer, Jr., D. Joseph Hagerty
University of Illinois

From disposal to recovery

The field of solid waste management has experienced two complete reversals of philosophy in the past seven or eight years. In 1965, the U.S. Congress passed the Solid Waste Disposal Act, which simply

These curbside companions harbor just a few days fallout from the "good life." But society's continued affluence may well depend on efficient use of the humble contents.

told those involved to find the most economical waste disposal methods. In 1970, the act was renewed as the "Resources Recovery Act." The emphasis at that time was put upon the recovery of recyclable materials and economic disposal of everything else.[4]

Some 18 to 24 months ago the U.S. began to see the first research efforts primarily devoted to both recyclable resources *and* energy recovery. Serious consideration of power generation from solid waste predates the present "energy crisis" by nearly two years.

Efforts to reclaim energy from solid waste can be broadly classified into four distinct schemes: direct heat recovery from special incinerators, supplementary fueling of power plants, destructive distillation (pyrolysis), and a systems approach adapting off-the-shelf hardware to waste-heat recovery.

The first and oldest of these methods dates back twenty years in its present resurgence, in both Europe and the U.S. Actually, many small incinerators attempted heat recovery around World War I, but these early projects were abandoned because of the waste's low caloric content (at that time) and the wide seasonal variation in waste characteristics.

Incinerator update: a steamy situation

Recently, however, several large incinerators have been installed in the U.S. with either add-on boilers or waterwalls. The most notable of these are in Chicago (both the Northwest and Southwest installations), and the Hempstead, Long Island, plant. The Hempstead plant generates 68 000 kg of steam per hour both for in-plant use and for the desalinating of seawater. The Chicago Southwest plant currently has contracts for supplying 454 000 kg of steam per day to adjacent industries in the stockyards area. The newer Northwest Chicago plant has no firm contracts as yet; but since the plant is in an industrial park, the Chicago authorities anticipate several substantial steam contracts very soon.

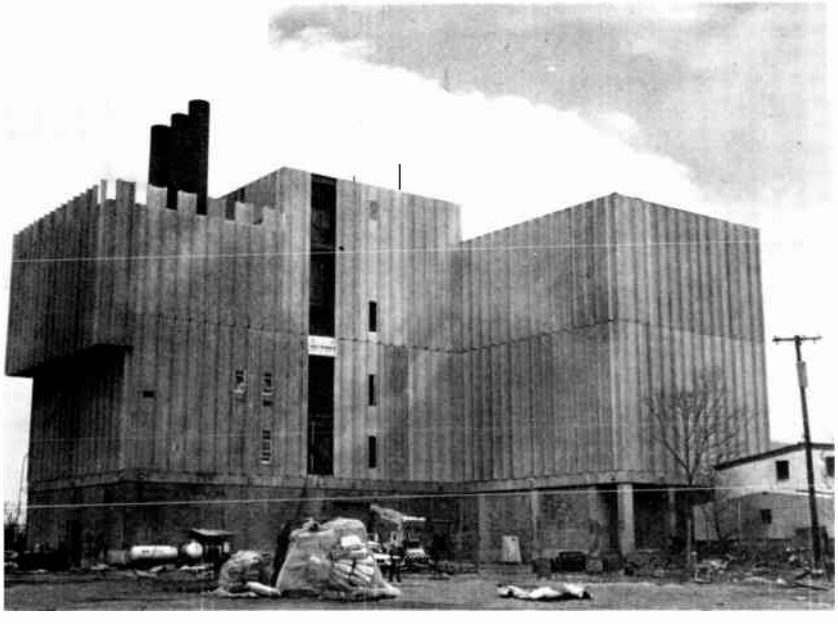
A plant currently under construction in Nashville, Tennessee, is quite similar to those just mentioned, but somewhat more fortunate since it is being built by the city in the center of the state government buildings complex (Fig. 1). Such logistics guarantee the installation of a year-round market for the steam, which can be used for either heat or air conditioning. And plant construction has received rather wide publicity, probably more for the unusual location and financing than for any unique technology.

Refuse will be delivered to the plant by Nashville, at no cost, under the terms of a 30-year contract and the steam generated will be used in 32 adjacent buildings. Revenue bonds, raised for construction funds, are guaranteed by the clients buying the steam. Ownership of the facility will revert to Nashville upon retirement of the bonds.

With respect to direct waste-heat recovery, European solid waste management is quite advanced relative to that in the U.S. Almost every large incinerator built in Europe during the last decade has incorporated a waste-heat recovery system. And at least three distinct system types are currently being used.

The new Edmonton incinerator, built on the northern outskirts of London, in the United Kingdom, incorporates a waterwall furnace design, with the exhaust gases from the combustion chamber passing through an economizer to aid in the generation of

[1] This incinerator facility under construction in Nashville, Tenn., generates steam which will provide year-round heat or air conditioning to nearby government office buildings.



What have they done to the rain?

The trouble, of course, with just about every power generation scheme involving combustion is pollution. In recent years, the particulate portion of the problem has yielded to the adoption of electrostatic precipitators. Where many industrial smokestacks once belched forth an ominous pall over neighboring communities, now an innocent-looking, almost colorless plume drifts skyward.

Unfortunately, the net result of this cleanup may already have helped create acid rains far more serious than the local dirt and smell associated with untreated smoke. A recent study in the June 14, 1974 issue of *Science* magazine by Gene E. Linkens, Section of Ecology and Systematics, Cornell University, and F. Herbert Bormann, School of Forestry and Environment Studies, Yale University, gives the details.

Drs. Linkens and Bormann suggest that a documented increase in acidic rain falling on the northeastern U.S. and Scandinavia is attributable to large amounts of sulphur dioxide (SO_2) and oxides of nitrogen being injected into the atmosphere in the absence of equivalent alkaline substances. By removing solid particles which, when present, combine with SO_2 to form salts, tall smokestacks fitted with the latest scrubbers have liberated considerable SO_2 which is retained in airborne moisture and converted to sulphuric acid (H_2SO_4). Fish kills, stunted tree growth, and corrosive damage to buildings highlight the prospects of precipitation gone permanently sour.

Recovery of energy from solid waste could appear even more attractive when this acid rain research is fully considered. Unlike most fossil fuels (other than natural gas), municipal refuse has a low sulphur content and therefore little potential for producing SO_2. As yet, there is no reliable, accepted method to remove SO_2 from industrial stack gases.—*Editor.*

steam. Under normal conditions this steam is used to drive three 12.5-MW turbogenerators, which create approximately 30 MW for export sale to the Greater London Electric Utility, and to provide additional power for in-house needs.

In Paris, a somewhat different approach has been taken. Here a principal use of the steam has been space heating, although some 200 million kWh of electricity is also generated and sold to Electricité de France. The center of the City of Paris is underlaid with an elaborate steam piping network, much like U.S. water and sewerage systems. Three strategically located incinerators (all built within the last twenty years, with the last one, at Ivry, finished in 1969) supply steam to this system. Some 1.8 million tonnes of steam are produced yearly for heating over 100 000 dwelling units.

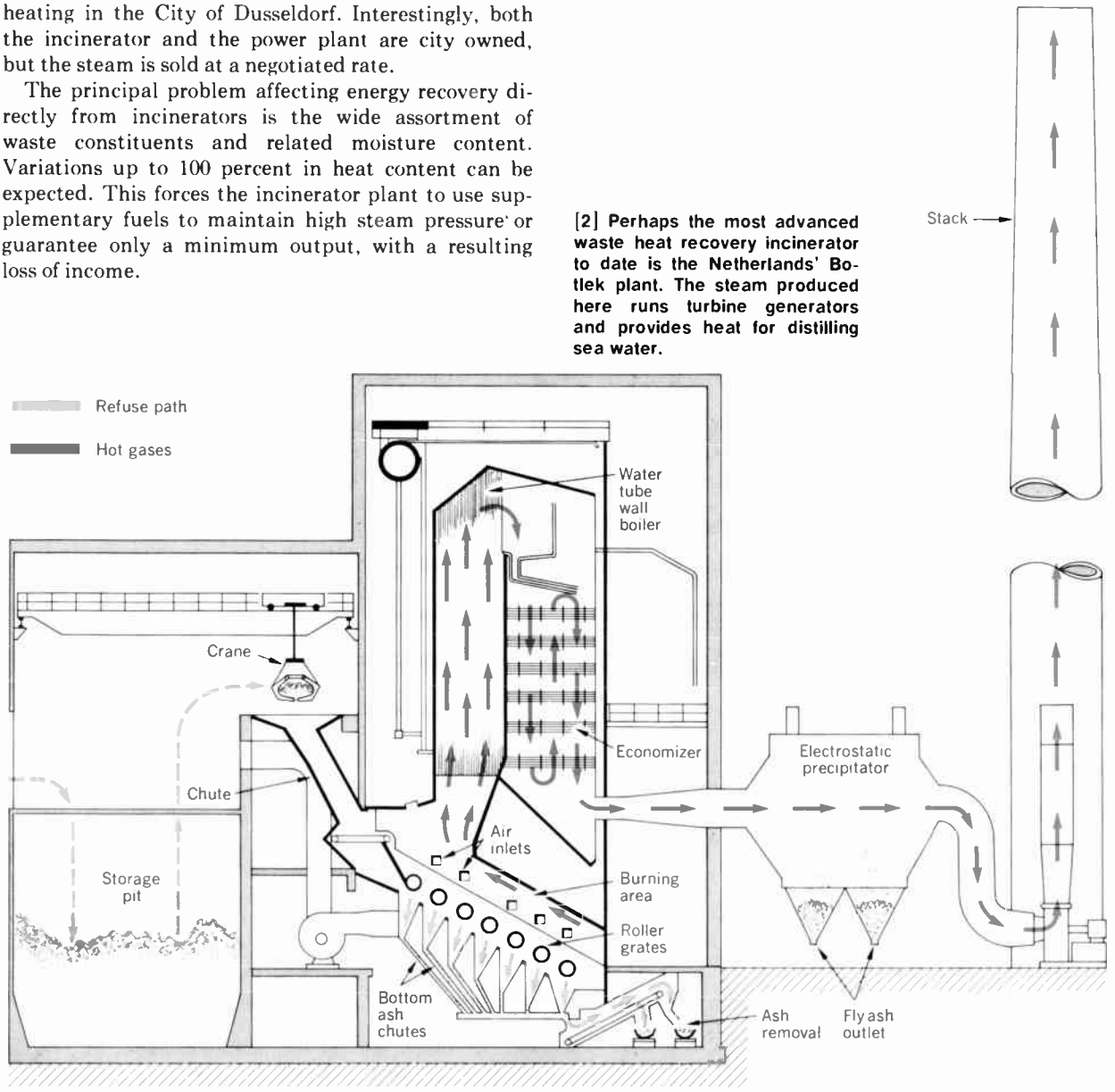
In Dusseldorf, West Germany, an example of a third type of waste-heat recovery system can be found. Here the facility is quite similar to both the Edmonton plant and the Ivry incinerator; however, the steam, after generation, is first delivered to a nearby municipal power plant and used to generate electricity. The spent steam is then used for central heating in the City of Dusseldorf. Interestingly, both the incinerator and the power plant are city owned, but the steam is sold at a negotiated rate.

The principal problem affecting energy recovery directly from incinerators is the wide assortment of waste constituents and related moisture content. Variations up to 100 percent in heat content can be expected. This forces the incinerator plant to use supplementary fuels to maintain high steam pressure or guarantee only a minimum output, with a resulting loss of income.

Perhaps the most modern and sophisticated waste heat recovery incinerator now in use was completed recently near Rotterdam, in the Netherlands. This incinerator, owned by Rotterdam and 23 small neighboring communities, is located in the highly industrialized Botlek area on the Netherlands seacoast (Fig. 2). Approximately 90 000 tonnes of domestic and household wastes are to be processed each year in addition to about 400 000 tonnes of industrial waste and about 63 500 tonnes of chemical wastes.

The domestic wastes and nontoxic solid industrial wastes are processed in six furnaces, with five of the furnaces being used at any one time and the sixth furnace kept in reserve. Each furnace is capable of incinerating roughly 14.5 tonnes of refuse per hour, and producing 45 tonnes of steam per hour at about 30 atmospheres pressure at 350°C. Computerized controls regulate circulation and mixing to ensure uniform temperatures and pressures in the outlet steam. One third of the produced steam passes through a turbo-

[2] Perhaps the most advanced waste heat recovery incinerator to date is the Netherlands' Botlek plant. The steam produced here runs turbine generators and provides heat for distilling sea water.



generator, is condensed, and then returned to the boiler units. The remaining steam also passes through turbines, but exits to distilling plants. Here, contaminated and mineralized water (including seawater) is distilled. At present, three distilling plants are in operation, each producing 408 tonnes of demineralized water per hour.

The purified water is sold to industrial plants in the Botlek area for use in boilers, chemical processes, etc. The power generated by the turbines is sold through an electrical utility system. While a minimum of 11 MW is guaranteed (by contract) to this utility, the incinerator turbines can produce up to 55 MW (maximum capacity).

A solid supplement

A second system of energy recovery uses solid waste as a supplementary fuel. In the U.S., this method is becoming widely known as the "St. Louis System."[4] Attempting to minimize the impact of seasonal variations in solid waste's heat content, the consulting engineering firm of Horner and Shifrin (in conjunction with the Union Electric Company of St. Louis) has investigated using solid waste as an auxiliary fuel.

Under a grant from the Environmental Protection Agency, a comprehensive study of the situation concluded that the operating problems of coal-fired boilers would not be significantly increased, if at all, by burning properly prepared refuse as a supplementary fuel. The Union Electric Company displayed its interest in the project by making one, and later two, of its major boiler units available for full-scale testing of the process. The company further offered to bear the capital expenditures required to modify its portion of the prototype facilities.

Initial refuse preparation (Fig. 3) occurs at city-operated facilities where material to be processed is discharged from packer trucks to the floor of the raw-refuse receiving building. Waste is then shredded in a hammer mill and conveyed to a storage bin. The head end of the conveyor is equipped with a magnetic separator to remove ferrous metals for recycling. Until recently, this was the extent of waste preparation; however, in the last several months an air-classification system has been added to remove most of the remaining noncombustibles.

The preparation process was designed to be as simple as possible to minimize operational problems associated with the refuse processing. Those problems that have occurred during the system's first months of operation have been mechanical in nature, and mainly due to the preculiarities of the milled refuse. Storage and handling has required special consideration since milled solid waste tends to compact under its own weight into a laminar, springy mass. Consequently, power requirements have been constantly underestimated for the handling equipment.

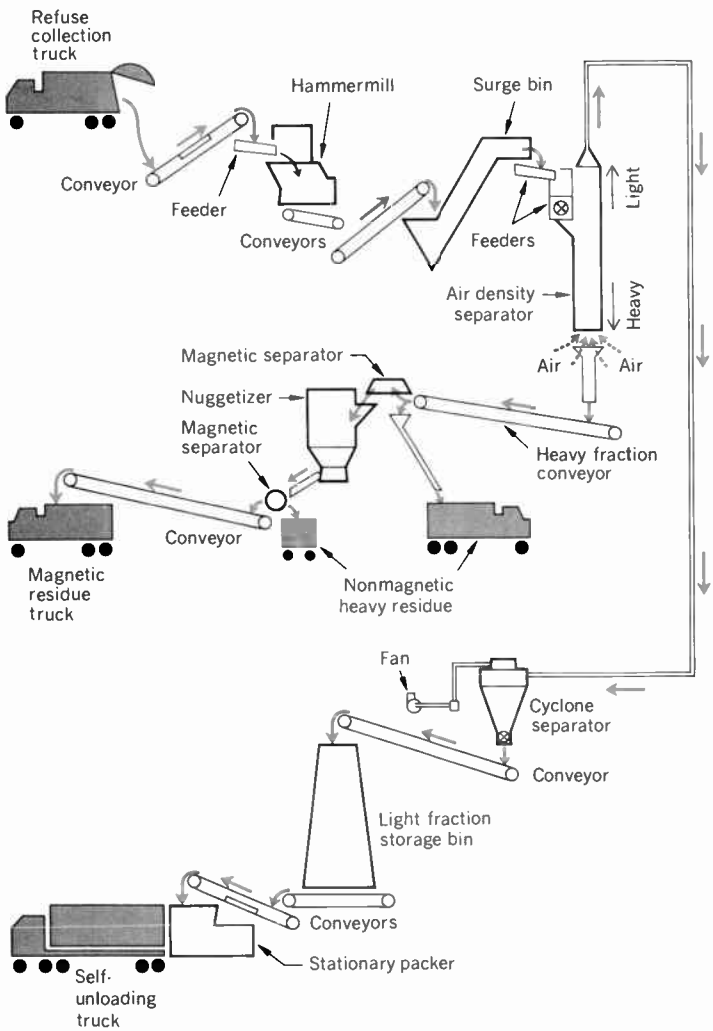
In the St. Louis prototype system, the processed solid waste is transported 29 km to the Union Electric Company's power plant. (However, pneumatic conveyance directly to the boilers from the storage bin would be feasible if the power plant were nearby.)

The transported, prepared refuse is dumped into a receiving bin, which supplies a belt conveyor, and is then discharged through a 30.5-cm pneumatic feeder line to a 244-cubic-meter surge bin. Crude metering of the refuse feed is accomplished with variable-speed conveyor drag chains.

Prepared refuse is burned in two twenty-year-old, tangentially fired Combustion Engineering boilers, located 213 meters from the storage bin. These boilers have a nominal rating of 135 MW each, with a maximum gross output of about 142 MW. Although the boilers are not "modern," the same basic furnace and burner design is still used in new units just now being put into service.

The Union Electric Company did not mix the prepared refuse with coal in the feed system because spontaneous combustion could occur in the coal pulverizers, and proper operation of the combustion control system was potentially threatened. Therefore, one gas nozzle in each corner of the furnace was removed, providing space for special refuse burners. Thus, solid waste is fired (independently of the coal) through these burners at 10 to 15 percent, by heat value, of the boiler's full-load fuel requirement. A 10-percent firing rate at this plant amounts to about 11.3 tonnes of refuse per hour.

[3] Solid waste can be burned in a coal-fired power plant as a supplement fuel if it is properly processed. The "St. Louis System," illustrated here, removes magnetic residue, noncombustible solids, and moisture from raw refuse before it is shipped to generation sites.



Since prepared refuse is fired to the boilers at a constant rate, coal firing must be adjusted to accommodate variations in waste-heat content or boiler-heat requirements. There has been no carry-over of unburned (waste) particles into the back passes of the boiler, nor any slagging due to firing refuse. Performance of the boilers, when fired with refuse and coal, has been identical to the performance of the unit when fired only with coal. Unfortunately, data regarding the long-term corrosion effects of refuse on boiler components are not yet available. Refuse's low sulfur content should decrease corrosion potential, while its higher chlorine content will have an opposite effect.

The heat value of prepared refuse used in the St. Louis project depends somewhat upon the moisture present. Since most prepared waste has an average heat value of 11.6×10^6 joules/kg (as fired), it is logical to assume this represents a lower limit for air-classified (and presumably dry) refuse.

Refuse preparation costs at St. Louis have been estimated between $4.95 and $6.61 per processed tonne. However, Chicago recently signed a long-term contract to supply such fuel to a local utility at $3.97 per tonne (the equivalent of coal at $7.94 per tonne), making the economics of waste heat recovery appear more favorable as the cost of coal advances.

Recovery under wraps

A third method of energy recovery from refuse is pyrolysis, which is destructive distillation of solid waste in an oxygen-free environment. Here the organic portion of the refuse can be converted into gas, liquid, and an inert char. The gas and liquid portions can then be converted into energy (even the char has some fuel potential). But this system for disposing of solid waste is as yet unproven. There are several major industrial companies that have such projects in the pilot-plant or design stages; however, because the processes are proprietary, results released to date are sketchy and inconclusive.

A laboratory study on mixed municipal refuse conducted by the U.S. Bureau of Mines in 1970 demonstrated that 0.9 tonne of refuse could yield 68 to 181 kg of solid residue, 1.89 to 22.7 liters of tar, 3.79 to 15.1 liters of light oil, and 227 to 510 cubic meters of gas. This gas was found more than sufficient to provide heat for sustaining the pyrolysis process.

A process similar to the Bureau of Mines experiment has been tested by the Garrett Research and Development Company, a subsidiary of the Occidental Petroleum Corporation. The Garrett system, now in the pilot-plant stage, employs a "flash" pyrolysis process designed to recover one barrel of synthetic fuel oil for every 0.9 tonne of as-received refuse. This synthetic fuel is low in sulfur, with a heat value approaching 75 percent of standard No. 6 oil. The Garrett pilot plant has been successfully operated on a 3.63-tonne-per-day basis and a full-scale installation using this system has been proposed for the City of San Diego. Refuse must be preshredded to particles smaller than 5.08 cm, then air-classified to remove inorganics, and finally dried to 3-percent moisture content. Glass and metals are separated through air classification and subsequent screening. But so far proprietary considerations have prevented details of the pyrolysis reactor from being released.

Several other schemes, inappropriately called "pyrolysis" systems, are in fact more closely related to high-temperature incineration. Such developments include the Torrax System, now operating in Erie County, New York, and the Monsanto Landgard system to be used in a 907-tonne-per-day plant now under construction in Baltimore, Maryland.

Contemplated, compact combustion

A fourth and final energy-recovery method attempts to take existing off-the-shelf hardware and adapt it to solid waste disposal. This system is under development by the Combustion Power Company at Menlo Park, California, and is known as the CPU-400 unit.

After required shredding and air classification, waste will be burned in a fluidized-bed combustor, and the hot gases produced will flow through a turbine, powering an electric generator. The system also provides for materials recovery through subsystem processing.

Currently envisioned installations will occupy less than 8100 square meters of land, allowing several plants to operate as refuse processing "satellites" around large urban areas. Such a satellite system could minimize expensive refuse collection and haulage costs.

Combustion should take place at a relatively constant 820°C. Hot gases from the combustor will pass through a series of inertial separators that collect particulate matter. Cleansed gases will pass through the turbine generator and out the exhaust stack.

This system is essentially at the drawing board and pilot-plant stage, with no major installations as yet planned. The economics and performance characteristics of the process are available only from manufacturers' estimates, and are not easily compared with the other proposed energy-recovery systems.

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John E. Heer, Jr. and **D. Joseph Hagerty** have been involved in solid waste management research since the passage of the Solid Waste Act of 1965, and have jointly authored two books on the subject. They are both currently on the faculty of the University of Louisville, Department of Civil Engineering. They recently completed a fifteen-month study concerning solid waste management which included an extensive tour of European installations. They have served as waste management consultants to local, state, and regional governments, and to the Appalachian Regional Development Commission. Drs. Hagerty and Heer both received the B.C.E. and M.Eng. degrees from the University of Louisville and the M.S. and Ph.D. degrees from the University of Illinois.

majority of business does so (again, quite possibly because of business' key role in establishing said ethic). But for the corporation to change, corporate leaders must foster changes in ethical standards. We must now arrest and reverse the downward trend of ethical standards, and the cynical outlook extant in the U.S. What is the general public to think when business leaders insist on remaining silent concerning Watergate and its related crimes and offenses against decent government?

In the second place, business leaders need to foster changes in *social* standards. Richard Gerstenberg, chairman of the General Motors Corporation, states the objectives, if not the vitally needed methodology to accomplish such social goals: "As a nation we have launched ourselves on a most ambitious social agenda. We want to achieve even higher standards of education, health, and well-being for all our people. We want to abolish poverty. We want to preserve and restore the beauty of our great resources; our land, our waters, and our skies. We want to give every American—of whatever color, religion, or background—an equal opportunity to become all he is capable of becoming. We aim for full employment, and even more —the full opportunity for everyone to participate in all that America has to offer."

Third, and perhaps most important, corporate leaders must foster internal management adaptation. A list of recent past and future management practices, developed by George A. Steiner of the U.C.L.A. Graduate Business School and representing a change in the world view of management, is given in Table I.

According to this new view of social responsibility, the aim of business is not to ameliorate social problems; it is to make definite and positive contributions to help the larger society achieve the goals it sets for itself. (Perhaps the classic definition of management remains appropriate for small corporations. It is the actions of large corporations that are crucial!)

The far-reaching intellectual revolution essentially involves realizing that new wealth is more and more going to flow from infusions of knowledge into both social and economic processes and from substituting energy for materials in production processes. The United States enjoys real opportunities for social and economic innovation. But in recent years, the probability has risen that major responses to such opportunities by established institutions will be reactionary and nostalgic, rather than imaginative and confident. Credibility has declined because of leadership timidity, traditionalism, and defensiveness.

Challenges

Let me list some elements in the challenges facing our society and the corporation of the future. The actions that business must consider are:

1. Realize and promote actively new Government policy that applies real science to *social* affairs, just as business took the lead in the 19th Century in applying real science to *industrial* affairs. A burst of innovation is needed to develop systems that would measure gains in social welfare. The approach should be in terms of major systems, their observation, structural interaction, and desired evolution.

2. Seek actively the creation of social markets for private production of the public goods people want in order to enhance the quality of their lives.

3. Initiate broad efforts to improve governance of, along with public participation in, our present national system of urban regions, by, for example, establishing, in order to analyze and finance urban innovation, a nationwide network of urban-observatory development banks combined with a central development bank.

4. Take the lead in constructively restructuring economic policy by realizing business's own need for vastly improved and expanded public policy analysis, in order to refashion policy consistent with environmental imperatives that are scientifically valid rather than emotion-generated.

5. Instigate a marketing revolution to shift from design, manufacture, and sale of products to functionally oriented marketing of systems for satisfying human wants. Business would sell health maintenance, transportation services, shelter services, and nutrition, instead of selling health products, cars and trucks, houses and durable goods, and food and drink.

6. Create entirely new advertising and communications philosophies, consistent with new marketing systems and values.

7. Initiate changes in investment theory and policy to avoid overvaluing short-run profit results at the expense of long-range human results. Restructure the role of investment analysts and broaden corporate ownership.

In my opinion, the new age offers the promise of a good life for all citizens of the U.S. and peace and cooperation with other countries. The challenge to the Space Age corporation and its leaders is to invent a future that people want. Finally, but by no means least, the electronics industry, with its fantastic promise derived from prospects of a million-fold increase in the speed of communication, should itself take the leadership in infusing our society with knowledge that can ease the transition to the new corporation.

Carl H. Madden is the Chief Economist for the Chamber of Commerce of the United States, a post he has held since December 1963. Prior to that he was Economist for the U.S. Senate Banking and Currency Committee, and was dean of the College of Business Administration at Lehigh University. Dr. Madden is manager of the Chamber's Economic Analysis and Study Group which examines long-range problems of national policy over a wide spectrum of economic and social questions. He has been chairman of the Conference of Business Economists and of the Business Advisory Council of the Labor Dept. Dr. Madden is a member of the board of trustees of the Joint Council on Economic Education and of the board of directors of the World Future Society. He was graduated from the University of Virginia with a B.A. degree, with honors in philosophy, and holds the M.A. and Ph.D. degrees in economics from the same university. He is also a graduate of the Stonier Graduate School of Banking at Rutgers University, where he has been a member of the faculty. The present article is based upon Dr. Madden's remarks before the Electronic Industries Association's 1974 Spring Meeting.

Spectrum's special report on

WESCON '74

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The Los Angeles Convention Center

1. Capsule guide

Twenty-seven technical sessions complement over 280 exhibits and cover many disciplines

A closer look at the 1974 WESCON technical program shows the technical papers about evenly divided between advanced-component technologies and marketing and management topics. The former includes papers on the latest display technologies, CCDs (charge-coupled devices), microprocessor ICs, and microwave components. The latter includes the entire gamut of business-related topics from how to raise capital for a new business venture to the ability of corporate, manufacturing, and marketing personnel to develop strategies for meeting such business crises as parts and power shortages.

WESCON will be held in the Los Angeles Convention Center, Tuesday, September 10, through Friday, September 13. Exhibits will be on the Center's main floor and the technical program on the mezzanine level. Show hours are from 9:30 a.m. to 5:00 p.m., Tuesday and Thursday; 9:30 a.m. to 9:00 p.m., Wednesday; and 9:30 a.m. to 4.00 p.m., Friday. Technical-paper sessions are in the morning (10:00 a.m. to 12:30 p.m.) and afternoon (2:00 to 4:30 p.m.). Doors to the Center will open for registration at 8:30 a.m. daily.

Special features include science-and-engineering and management film theaters, an industrial-distribution marketing session (Monday, September 9), and a special "Psychotronics" session (Wednesday, September 11, 7:00 to 10:00 p.m.) in which researchers from U.C.L.A.'s Neuropsychiatric Institute will discuss their findings on human parapsychological phenomena. A special evening session on engineering pensions has also been scheduled, to be held Tuesday, September 10, 8:00 to 10:00 p.m.

Roger Allan Associate Editor

2. Scanning the sessions

WESCON's technical program follows the product exhibits closely. The four exhibit categories of components and microelectronics, instruments and instrumentation, production and packaging, and computers and communication constitute four of five areas of technical-program coverage—the fifth being management, marketing, and finance.

This year's show has fewer sessions than last year's (27 vs. 33) and approximately the same average of four to five papers per session. To keep the technical-program attendance from sagging by the week's end, two of the most interesting sessions, 26 and 27, are scheduled for Friday morning. To allow show attendees enough travel time to and from WESCON, no technical sessions have been scheduled all day Monday and Friday afternoon. A brief description of the five broad areas of coverage follows.

Components and microelectronics

Six of the 27 sessions are devoted to charge-coupled devices (CCDs) and microprocessors. Session 2 provides a basic understanding of what CCDs are, how they work, and where they can be applied. Session 6 points out the distinct advantages of CCDs as low-cost, mass-storage memories to replace disk and drum memories. Most major semiconductor manufacturers are quietly engaged in CCD-memory research and some have produced a few experimental devices.

The microprocessor's impact on the way engineers design circuits is already being felt, as more and more microprocessor ICs become available commercially. There are four microprocessor sessions that are designed to provide all there is to know about microprocessors—not only how they work and what they can do, but also what is available on the market, and their impact on future as well as current product designs.

Session 11 provides an overview of the microprocessor market—ways of getting started, software availability and performance, and how to select the right microprocessor for a given application. Its follow-up session (15) will describe several new microprocessor systems such as the Fairchild Semiconductor F8; Motorola's M6800; National's FACE (Field-Alterable Control Element); and new families from Signetics, Intel, Rockwell Microelectronics, and RCA Semiconductor.

Session 19 is a semitutorial one—explaining and exploring the concept of microprocessors. Speakers include academicians as well as industry experts. The follow-up session (23) shows the microprocessor's impact on electronic equipment design. Several design examples of microprocessor applications will be presented.

The continuous process in the various types of display technologies will be reviewed in session 26, "Emerging Display Technologies." Optical characteristics of ac plasma panels, multilayer aspects of gas-discharge panels, thin-film-transistor liquid-crystal matrix arrays, and a photooptical video-disk system will be reviewed.

Session 3 will review the progress of "Microwave and Millimeter Solid-State Components." Papers are slated on low-noise, high-gain microwave amplifiers that operate in the 4.0- to 8.0-GHz frequency range, tuned oscillators, mixers and millimeter IMPATT, and Gunn-effect devices.

Instruments and instrumentation

With modern ECL and Schottky TTL digital circuitry, nanosecond-rise-time signals with clock/pulse repetition rates to 200 MHz are becoming all too common. However, measuring these types of high-speed signals accurately presents many problems. Session 27 addresses itself to these problems within three broad categories which are: systems, time, and amplitude.

Organized by a group of engineers that did Department of Defense contract work at the Massachusetts Institute of Technology's Lincoln Laboratory, this session concentrates on accurate measurement techniques developed using digital logic ICs, some of which are currently available on the market, for high-speed amplitude and timing measurements.

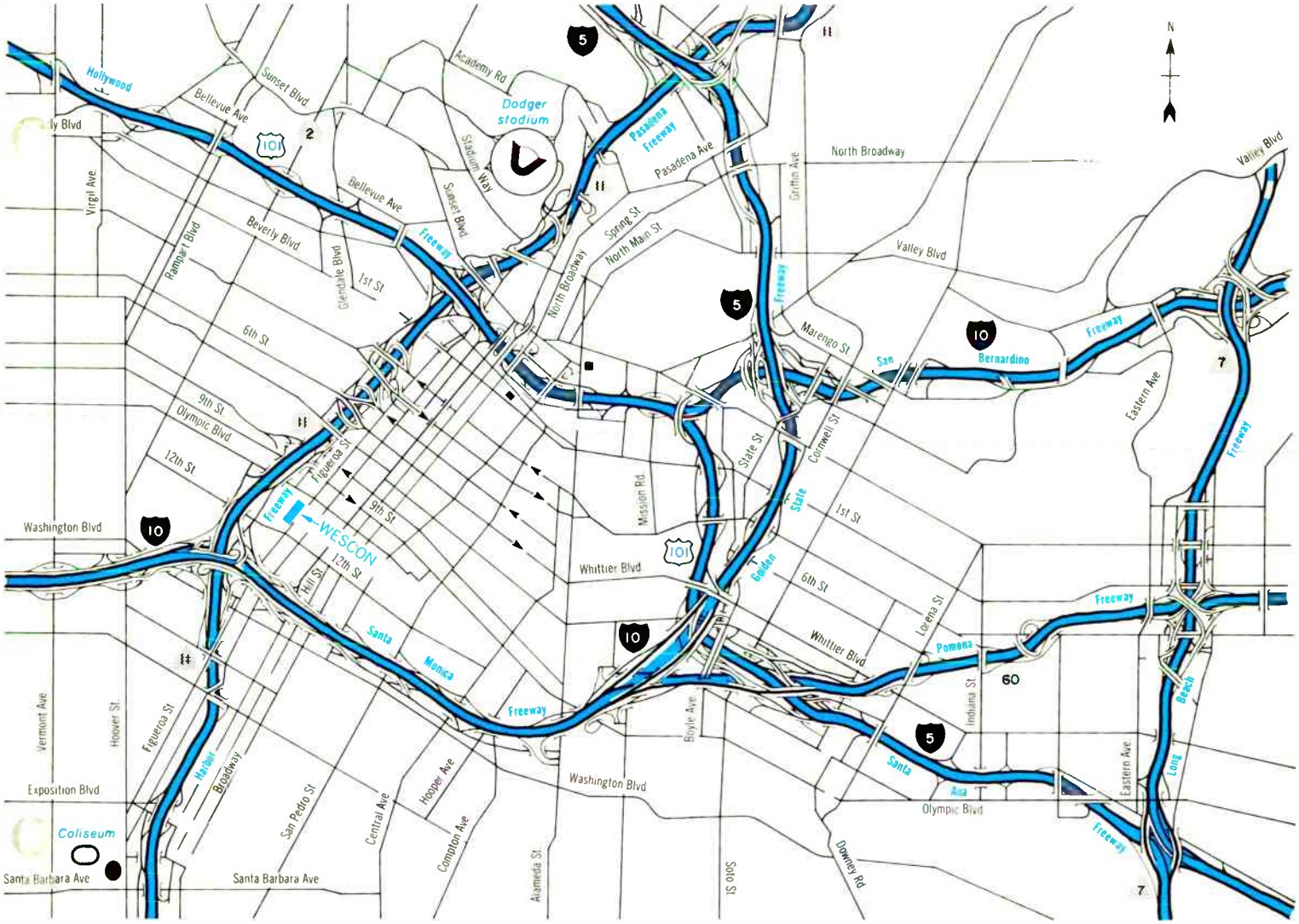
On the systems level, examples will be given of systems problems that are unique to high-speed circuits. These include finite-velocity signal-propagation allowances, excessive signal losses during transmission and reception, and the elimination of "ringing" and signal reflections. Amplitude-measurement problems discussed include examples in threshold, sample-and-hold, and nanosecond pulse generator circuits. And lastly, in terms of the time domain, methods for solving problems associated with the measurement of the interval between two unknown signals or the generation of a predetermined time interval will be considered.

On the subject of high-speed signals, workshop panel session 20 will demonstrate some solutions to problems encountered when working with very fast pulses used in TDR (Time Domain Reflectometry) and FDR (Frequency Domain Reflectometry) measurement techniques for detecting faults (open or short circuits) in transmission lines.

Automatic testing of electronic components and systems is today more of an economic necessity for many industries than ever before. This new ATE (Automatic Test Equipment) technology has spawned many problems, not uncommon to emerging technologies that will be debugged with time. Session 22 addresses itself to LSI (Large-Scale Integration) testing problems at the component level. Testing on the wafer level, the merits and cost-effectiveness of different LSI test methods, CMOS (Complementary Metal-Oxide Silicon) testing, and testing of LSI memories are all on the agenda.

Session 25 is all about testing ICs on the printed-circuit-board level. Because digital logic ICs have become more complex, their testing has become even more expensive. This session will explore new systems to beat the high-cost testing problem.

Session 12 covers the range of needs and trends in medical electronics instrumentation. Included will be papers on progress in blood-flow measurements, measurements of blood-flow by magnetic resonance, ap-



plications of pulsed ultrasonic doppler and flowmeters, and pacemaker evaluation methods.

Production and packaging

The continued miniaturization of electronic components, such as ICs, has placed great demands on packaging and production methods. It is one thing to design a novel device with fantastic potential on paper and altogether another thing to manufacture and package that device at a reliable yet economical level, consistent in small size with other miniature components with which it is to be mated. Three sessions (9, 17, and 21) address themselves to some of these problems.

For several years, we've heard the pros and cons of various bonding techniques for semiconductor devices in hybrid circuits—the step that connects the inside world of the semiconductor IC to the outside world of the much larger discrete component. In fact, no body of expert opinion can agree on "the best" bonding method. Session 17, a clinic on hybrid microelectronics semiconductor bonding, will host a "round robin" user panel familiar with everyday problems and solutions involving "chip-and-wire," "flip-chip," and "beam-lead" bonding technologies.

Session 21 is intended to clarify and develop proper perspectives on a number of misconceptions, widely held, about additive-circuit manufacturing methods for making printed circuits. Their advantages and limitations will be looked at. Papers will deal with the status of the additive process, how a user sees this process, combining additive and subtractive processes, using a dry-film resist for the additive process, and a look at a fully additive process that uses no liquid.

The economics, availability, and reliability of plastic encapsulated microelectronic circuits (monolithic and hybrid) as well as discrete components will be heard from the user's viewpoint in session 9. Speakers representing the automotive, computer, and calculator fields will present papers.

Computers and communications

Ever since the historic Carterfone decision in 1968, which allowed other companies to compete with the Bell System in the manufacture of data-communications equipment, there has been an explosive growth in this field. The proliferation of common-carrier companies has given the user a wide choice of service, which has not been without its problems. Session 14

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"THE BIG M"

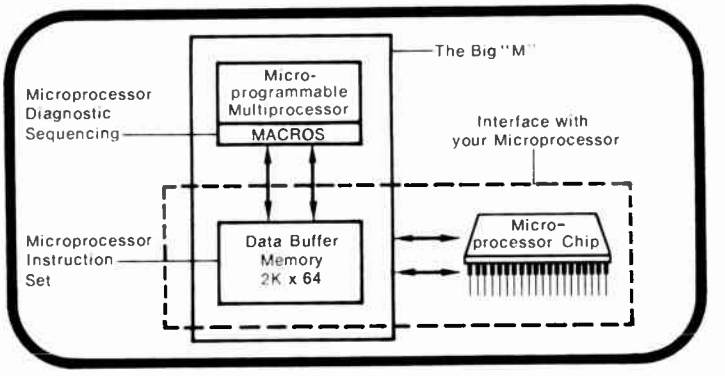
the first low-cost microprocessor tester.

Once semiconductor memories were "impossible" to test. Then Macrodata came up with the answer. Now, testing microprocessors is a whole new game. Even if you test all the logic on your chip with tens of thousands of test patterns, it does not guarantee that your microprocessor is a good device.

Classically, computers are tested through the simulation of instructions, so each and every individual instruction must be simulated. But experience has proven that even when each individual instruction works, it is no final guarantee of processor logic. Therefore, sequences of instructions must also be tested—which implies the use of new test techniques.

That's where Macrodata's new Big "M" Microprocessor Tester comes in. With its processor-controlled buffer memory, the Big "M" provides the only low-cost solution to this testing problem. The Big "M" can do simulation on your microprocessor not only on an instructional basis but also on sequences of instructions.

Whether you're a manufacturer or a user of microprocessors, Macrodata's new Big "M" is your answer! For immediate action, call the marketing department, or send for more information.



Macrodata

Macrodata Corporation, 6203 Variel Avenue, Woodland Hills, California 91364, Phone: (213) 887-5550, Telex: 65-1345

Sales Offices: *Northern California Area* Tel. (408) 735-9560 • *Scottsdale* Tel. (602) 966-2179 • *Minneapolis Area* Tel. (612) 454-2034 • *Chicago Area* Tel. (312) 297-8746 • *Cleveland Area* Tel. (216) 461-8333 • *Dayton Area* Tel. (513) 293-3145 • *East Coast* Tel. (516) 543-8600 **International:** *West Germany — Munich* Tel. (0811) 34 56 00 Telex: (841) 521-5969 • *Milan, Italy* Tel. 871-988/899-248 Telex: (843) 34314 • *Sweden and Norway — Stockholm* Tel. (08)-380-370 • *Tel Aviv, Israel* Tel. 25 55 69 • *Tokyo, Japan* Tel. (03) 985-5266 Telex: (781) 272-2171 • *Buckinghamshire, England* Tel. High Wycombe (0494) 36 3 81 Telex: (851) 837236

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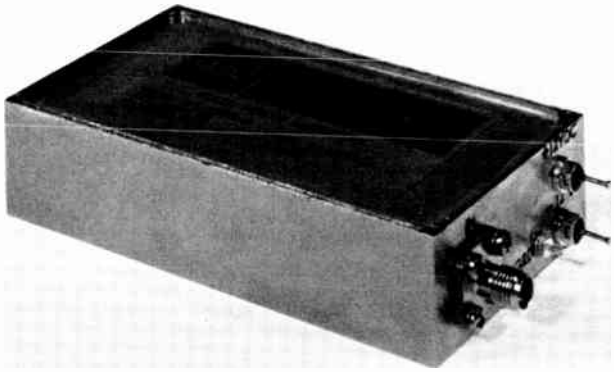
sheds some light on this area by presenting new and significant advances in communications networking. Four speakers, three of them common-carrier spokesmen (AT&T, Western Union, and Bell Canada) and the fourth, a consultant, describe the real world of digital communications—what is currently available to fill the user's needs.

Session 7 presents a broad survey of the current status of and near-future projections for radar technology. Four papers will survey four main radar fields: the rapidly growing area of RF solid-state technology; modern long-range surveillance radar; high-resolution, synthetic-aperture, mapping radar with applications to earth-resources studies; and recent developments in airborne MTI (Moving-Target Indicator) doppler radar, using advanced digital signal-processing techniques to improve radar resolution.

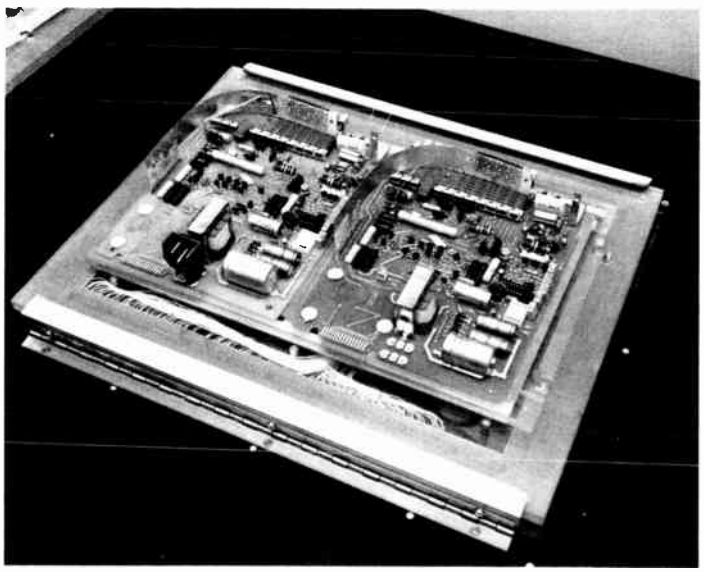
The special session on "Psychotronics" Wednesday evening is all about communications of a different kind—telepathic. Five speakers from U.C.L.A.'s Neuropsychiatric Institute headed by Dr. Thelma Moss will talk about their work in applying electronic equipment to study the "human energy" field. Slides, photographs, live demonstrations and motion-picture film will be used to exhibit experiments in Kirlian photography (the science of photographing human-energy emanations with high-voltage discharges around the body), bio-energy and human interactions, and some unorthodox therapeutic techniques.

Session 10 deals with computer power. The problems of line-voltage and frequency variation and of brownouts and blackouts as seen by a large computer-systems manufacturer, a semiconductor-memory manufacturer, a power-supply manufacturer, and a major public utility will be presented.



GaAs FETs allow this advanced full C-Band amplifier to operate over 4.0 to 8.0 GHz at 20-dB gain and 6.5-dB maximum noise (session 3).

A test fixture, part of a cost-effective testing system used in the manufacture of electronic subassemblies. The two boards on the fixture are Fluke 8000A digital-voltmeter subassemblies under test (session 25).



Management, marketing, and finance

The number of sessions dealing with the business aspects of electronics is constantly increasing. This is in recognition of the fact that commercial activity of the electronics community is as important as engineering development—if not more so.

If you're trying to run an electronics company today, a constant environment of crisis and uncertainty can be expected—ranging from local power-cut problems that may force you out of business to parts shortages involving waits of up to 60 weeks for capacitor deliveries. How to develop strategies to deal with such crises as these will be the subject of discussion during session 4.

In the same vein, six distinguished panelists will discuss how to sell a "better" product in session 18. Marketing, sales, advertising, publicity, and inquiry follow-through strategies will be explored.

Session 5 deals with the crucial problem of raising capital for either starting a new business or expanding a growing operation in a tight-money world. A panel of financial and management experts will discuss how to prepare an effective business plan containing the key elements that an experienced venture capitalist, financial analyst, and banker looks for.

Electronics is always looking at new markets to be penetrated. One such market is agriculture. Session 8 is intended to stimulate members of the electronics community to view their technology in the light of the problems facing agriculture in the U.S. This includes such problems as livestock-identification means, using computers in the dairy industry, and using electronic technology for animal health care.

Panel session 13 has three senior electronics executives who will give short case histories of how each of them translated new technologies into marketable products.

What will the future role of electronics be in society? How will it affect the quality of life? What technological changes can we foresee as a result? Session 16 attempts to answer these questions.

Session 24 takes a look at how designers can cope with a set of design specifications within a fixed design cost. It will compare some military design programs to ones in the industrial sector.

And, finally, how to teach nontechnical personnel to operate and maintain technical equipment is the subject of session 1.

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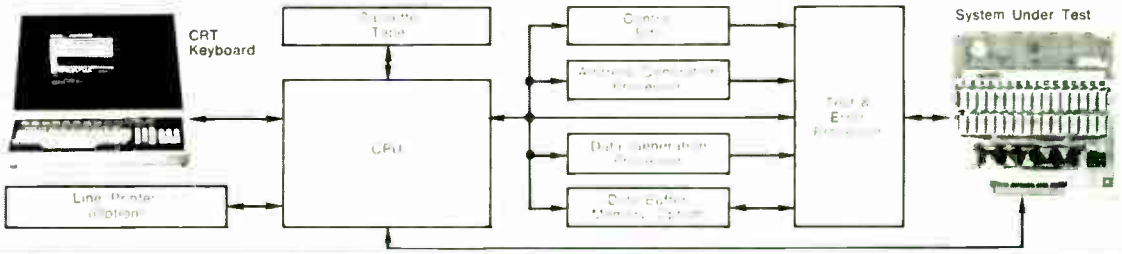
For the full story, send for the MD-107 brochure, or call us directly.

SYSTEM BLOCK DIAGRAM



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1974 WESCON TECHNICAL PROGRAM (Los Angeles Convention Center Mezzanine)

Date and Time	Room 212A	Room 212B	Room 217A	Room 217B
Tuesday September 10 10 a.m.– 12:30 p.m.	**Session 1** Teaching Nontechnical Personnel to Understand and Use Electronic Equipment	**Session 2** Introduction to Charge-Coupled Devices	**Session 3** Microwave and Millimeter Solid-State Components	**Session 4** Strategy for Crisis
Tuesday September 10 2 p.m.– 4:30 p.m.	**Session 5** How to Prepare an Effective Business Plan to Raise Capital	**Session 6** Advances in CCD Memories	**Session 7** Modern Radar Technology	**Session 8** New Markets in Agriculture for Electronic Technology
Wednesday September 11 10 a.m.– 12:30 p.m.	**Session 9** Status of Plastic Encapsulated Semiconductors—Fact, Not Fiction	**Session 10** What To Do If the Lights Go Out—The Uninterruptible Power Story	**Session 11** Microprocessors—Market, Design, Applications	**Session 12** Needs and Trends in Medical Electronics—1974
Wednesday September 11 2 p.m.– 4:30 p.m.	**Session 13** Taking Your Technology to New Markets	**Session 14** The Real World of Digital Communications	**Session 15** Microprocessors—The Second Generation	**Session 16** Quo-Vadis Electronics?
Thursday September 12 10 a.m.– 12:30 p.m.	**Session 17** Hybrid Microelectronics Clinic on Semiconductor Bonding	**Session 18** Selling Your "Better Mousetrap"	**Session 19** The Microprocessor Revolution—Part I	**Session 20** Fault Detection in Transmission Lines Using TDR and FDR Techniques (Panel)
Thursday September 12 2 p.m.– 4:30 p.m.	**Session 21** The Status of Additive Printed Circuits Today	**Session 22** LSI Testing	**Session 23** The Microprocessor Revolution—Part II	**Session 24** Design-To-Price
Friday September 13 10 a.m.– 12:30 p.m.	**Session 25** Automatic Testing of PCBs—Ways and Methods	**Session 26** Emerging Display Technologies	**Session 27** Applications of Digital Logic to High-Speed Amplitude and Timing Measurements	

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3. WESCON technical program

Tuesday, September 10 Morning Sessions 10:00 a.m.–12:30 p.m.

Session 1: Teaching Nontechnical Personnel to Understand and Use Electronic Equipment

Room 212A

Session Organizer and Chairman: Erich A. Pfeiffer, Biomedical Engineering Section, Veterans Administration Hospital, Sepulveda, Calif.

1/1 **Lectures, Slides, and Other Visual Aids,** *Fred J. Weibell, Biomedical Engineering and Computing Center, V. A. Hospital, Sepulveda, Calif.*

1/2 **Manuals, Models, and Simulators,** *Erich A. Pfeiffer, V. A. Hospital, Sepulveda, Calif.*

1/3 **Filmstrips,** *Ralph Tuchman, Harris-Tuchman Productions, Hollywood, Calif.*

1/4 **Video Tapes,** *Walt Robson, Hewlett-Packard, Palo Alto, Calif.*

Session 2: Introduction to Charge-Coupled Devices

Room 212B

Session Organizer and Chairman: Jules H. Gilder, Electronic Design Magazine, Rochelle Park, N.J.

2/1 **Charge-Coupled Devices –An Overview,** *Walter F. Kosonocky, RCA Laboratories, Princeton, N.J.*

2/2 **Signal-Processing Applications for CCDs,** *Robert Broderson and D. D. Buss, Texas Instruments, Dallas, Tex.*

2/3 **CCD Image Sensors,** *Allen L. Solomon, Fairchild Semiconductor, Palo Alto, Calif.*

Session 3: Microwave and Millimeter Solid-State Components

Room 217A

Session Organizer and Chairman: W. K. Kennedy, Watkins-Johnson, Palo Alto, Calif.

3/1 **Microwave Amplifiers,** *Martin Walker, Watkins-Johnson*

3/2 **Millimeter IMPATT Devices,** *Bruce Kramer, Hughes Aircraft, Electron Dynamics Div., Torrance, Calif.*

3/3 **Millimeter Gunn-Effect Devices,** *Robert Goldwasser, Varian Associates, Solid State West Div., Palo Alto, Calif.*

3/4 **Microwave Varactor-Tuned Oscillators,** *Ronald Buswell, Watkins-Johnson, Palo Alto, Calif.*

3/5 **Microwave Mixers,** *Ferenc Marki, Watkins-Johnson, Palo Alto, Calif.*

Session 4: Strategy for Crisis

Room 217B

Session Organizer and Chairman: Frank Burge, Integrated Communications Systems, Sunnyvale, Calif.

4/1 **Introduction,** *Frank Burge, Integrated Communications Systems*

4/2 **Minimizing Risks, Delays in Custom MOS Circuits,** *Joe Mingione, American Microsystems, Santa Clara, Calif.*

4/3 **The Demand Crisis and Its Effect on Manufacturing,** *George Winn, John Fluke Manufacturing, Seattle, Wash.*

4/4 **The Backlog Crisis and Its Effect on Marketing and Distribution,** *Larry Pond, Liberty Electronics, El Segundo, Calif.*

4/5 **The Financing Organization's Viewpoint,** *Tom Swegle, Wells Fargo, Special Industries Group, Costa Mesa, Calif.*

Tuesday, September 10 Afternoon Sessions 2:00 p.m.–4:30 p.m.

Session 5: How to Prepare an Effective Business Plan to Raise Capital

Room 212A

Session Organizer and Chairman: C. C. E. Hoebich, Hoebich Venture Management, Palo Alto, Calif.

Panelists:
Eugene Kleiner, Kleiner & Perkins, Menlo Park, Calif.
Burton R. Cohn, Private Investor, Sherman Oaks, Calif.
Brent T. Rider, Union Venture, Los Angeles, Calif.
Christain Hoebich, Hoebich Venture Management, Palo Alto, Calif.

Session 6: Advances in CCD Memories

Room 212B

Session Organizer and Chairman: Jules H. Gilder, Electronic Design Magazine, Rochelle Park, N.J.

6/1 **CCDs as Drum and Disk Equivalents,** *James M. Chambers, Donald J. Sauer, and Walter F. Kosonocky, RCA, Van Nuys, Calif.*

6/2 **CCD Memory Concepts,** *Marc Guidry, Fairchild Semiconductor, Palo Alto, Calif.*

6/3 **Serial-Memory Charged-Coupled Devices,** *Douglas R. Colton, Bell-Northern Research, Ottawa, Canada*

6/4 **A 16 384-Bit Low-Cost Serial CCD Memory Element,** *Marvin White, Westinghouse Electric, Baltimore, Md.*

Session 7: Modern Radar Technology

Room 217A

Session Organizer and Chairman: Gene W. Zeoli, Hughes Aircraft, Aerospace Group, Culver City, Calif.

7/1 **Advanced RF Solid-State Radar Technology,** *John Smith and Robert T. Kemerly, AFAL/TEM, Wright Patterson AFB, Dayton, Ohio*

7/2 **Recent Developments of Airborne MTI Doppler Radar,** *David A. Kramer and Ethan Aronoff, Hughes Aircraft, Culver City, Calif.*

7/3 **Modern Long-Range Surveillance Radars,** *William S. Jones and Louis F. Meren, Westinghouse Electric, Baltimore, Md.*

7/4 **Synthetic-Aperture Radar,** *L. C. Graham, Goodyear Aerospace, Litchfield Park, Ariz.*

Session 8: New Markets in Agriculture for Electronic Technology

Room 217B

Session Organizer and Chairman: John Hanton, Montana State University, Bozeman, Mont.

8/1 **Animal Health and Ultra-Technology—Today Versus Tomorrow,** *Coleman Hensley, Los Alamos Scientific Laboratories, Los Alamos, N.M.*

8/2 **Application of Computers to the Dairy Industry,** *Bliss Crandall, DHI Computer Center, Provo, Utah*

8/3 **Problems of Western Agriculture,** *Ronald D. Plowman, Utah State University, Logan, Utah*

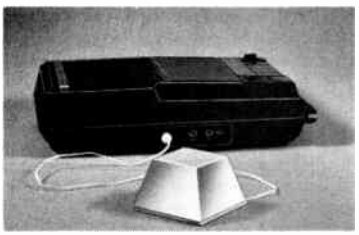
8/4 **Electronic Means of Livestock Identification,** *John Hanton, Montana State University, Bozeman, Mont.*

VISIT UTAH! wescon 74

BOOTHS No. 4009 and No. 4010

see the miniature Vidicon Television Camera, one of a dozen special use television cameras manufactured in Utah by Edo Western Corp.

see the new Metric Conversion personal computer. Manufactured in Utah by Summit Corp.



see Soundcaster, – "Product of the year, 1973" – the transmitter that turns ANY sound source into a miniature broadcasting station. Manufactured in Utah by Soundcaster Audio Corporation.

see the Quarza watch, the finest liquid crystal digital timepiece available, with an accuracy of 12-seconds a year. Manufactured in Utah by Cox Electronics Systems, Inc.

see the Television Character Generator which provides alphanumeric displays for CATV, Broadcast and Closed Circuit Systems. Manufactured in Utah by TeleMation, Inc.

see the new lightweight Stability Augmentation System (SAS) and Autopilot, along with various electronic boards and modules. Manufactured in Utah by E-Systems Inc., Montek Division.

discover why Electronics manufacturers can expect a 10% higher net income in Utah. (New research shows electronics manufacturers can expect higher profits in Utah than other parts of the country. Ask for a copy of the report.)

win one of the products shown above by taking our two-minute quiz about Utah. We'll be giving away other gifts and mementoes, too. The easy-to-find answers to the quiz can be found at our exhibit. You'll learn some interesting facts you didn't know about Utah and you may win a valuable prize.

Win the West from UTAH!

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Wednesday, September 11 Morning Sessions 10:00 a.m.–12:30 p.m.

Session 9: Status of Plastic Encapsulated Semiconductors—Fact, Not Fiction

Room 212A

Session Organizer and Chairman: Edward B. Hakim, U.S. Army Electronics Command, Fort Monmouth, N.J.

9/1 **Plastic-Encapsulated Semiconductors in Auto Radios,** *K. Kobersberger, Delco Electronics, GMC, Kokomo, Ind.*

9/2 **Proving Plastic for Profits,** *J. Pignatiello, National Cash Register, Dayton, Ohio*

9/3 **A Reliability Evaluation of Plastic-Encapsulated Semiconductor Components,** *H. C. Gorton, Vector Comptometer, Des Plaines, Ill.*

9/4 **Reliability of Ceramic and Plastic Encapsulated ICs in a Computer Environment,** *M. Halleck and K. A. Johnson, Honeywell Information Systems, Phoenix, Ariz.*

Session 10: What To Do If the Lights Go Out—The Uninterruptable Power Story

Room 212B

Session Organizer and Chairman: David N. Kaye, Electronic Design Magazine, Inglewood, Calif.

10/1 **Designing Protection Against Brownouts and Blackouts into a Large Computer System,** *John M. Roberts, IBM Systems Products Div., Kingston, N.Y.*

10/2 **Protecting Semiconductor Memory Against Power Variation of Interruption,** *Milton Watson, Texas Instruments, Digital Systems, Austin, Tex.*

10/3 **Uninterruptable Power—Through the Eyes of a Power-Supply Manufacturer,** *Kenneth E. Olson, Topaz Electronics, San Diego, Calif.*

10/4 **Uninterruptable Power—Through the Eyes of a Major Power Company,** *Carl F. Osborn, Los Angeles Department of Water and Power, Los Angeles, Calif.*

Session 11: Microprocessors—Market, Design, Applications

Room 217A

Session Organizer and Chairman: David Froelich, IC Update/Master, Sunnyvale, Calif.

11/1 **The Microprocessor Market—Now and Future,** *Bob Wickham, Creative Strategies, Palo Alto, Calif.*

11/2 **Building Low-Cost Systems with Microprocessor Hardware,** *Matt Bieuer, Pro-Log, Monterey, Calif.*

11/3 **Microprocessor Design—Use the Software Too,** *Jim Lally, Intel, Santa Clara, Calif.*

11/4 **How to Select a Microprocessor for Your Application,** *Jerry Larkin, National Semiconductor, Santa Clara, Calif.*

Session 12: Needs and Trends in Medical Electronics—1974

Room 217B

Session Organizer and Chairman: Morton D. Schwartz, California State University, Long Beach, Calif.

12/1 **Electronics in Medicine: An Overview,** *Morton D. Schwartz, California State University, Long Beach, Calif.*

12/2 **Electronic Applications in Therapeutic Devices,** *Albert M. Cook, California State University, Sacramento, Calif.*

12/3 **Pacemaker Evaluation Methods,** *Brewer Ward, St. Mary's Hospital, Long Beach, Calif.*

12/4 **The Plasatron as a High-Voltage Switch in Defibrillators,** *Dick Fleenor, Gould Medical Systems, Sunnyvale, Calif.*

12/5 **Progress in Blood-Flow Measurements,** *Jay R. Singer, University of California, Berkeley, Calif.*

12/6 **Measurements of Blood Characteristics by Magnetic Resonance,** *Larry Crooks, University of California, Berkeley, Calif.*

12/7 **Pulsed Ultrasonic Doppler Flowmeter Applications in Medicine,** *Wayne S. Foletta, Stanford Electronics Laboratory, Stanford, Calif.*

Wednesday, September 11 Afternoon Sessions 2:00 p.m.–4:30 p.m.

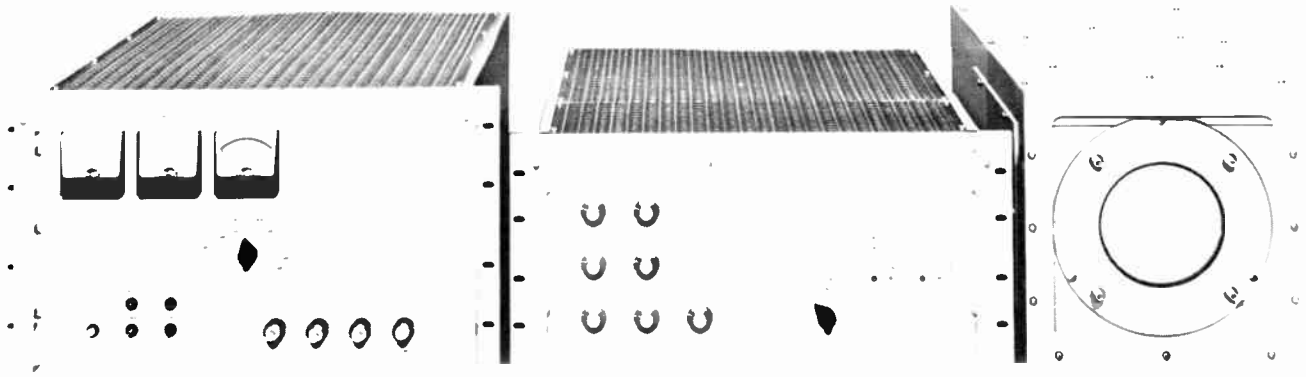
Session 13: Taking Your Technology to New Markets (Panel)

Room 212A

Session Organizer: William J. Schroeder, McKinsey & Co., Los Angeles, Calif.
Session Chairman: Robert D. Paulson, McKinsey & Co., Los Angeles, Calif.

Panelists:
Donald C. Forster, Associate Director, Hughes Research Laboratories, Malibu, Calif.

The "Above-Average" Sub-System by Celco



CELCO makes Precision CRT Displays for your "above-average" CRT requirements.

Need a CRT spot-size as small as 0.00065"? This standard CELCO 5" CRT display is being used for Satellite Photography. They needed the best they could get. You can get performance like that too with CELCO's DS5-065 Precision CRT Display.

A CELCO DS5-08 with 0.1% linearity, and spot size of 0.0008" is being used by another CELCO customer for Nuclear Photography Film Recording. Special features include programmable Raster Generators, and triple-layer and articulated shielding for ambient fields from earth's field and from dc to RF fields.

Fingerprint Scanning is the job of CELCO's DS5-10 Optical Character Recognition System for one of our customers. They needed that wide 2.5 MHz deflection bandwidth for high-speed scanning of vast amounts of data. And the DS5-10 has a settling time of 10 microseconds to 0.1% large signal, and 350 nanoseconds to 0.02% small signal settling time. Spot-size is 0.001".

One CELCO customer is using our 5" Color Display System for color separation and color photo scanning. One display does all that!

If your *needs* are "above-average" but your budget is *below*-average, CELCO also makes a 5" Precision CRT Display System especially for you that's ideal for your Low-Cost Film-Scan applications. Or if your display needs are larger, CELCO makes standard precision 7" and 9" CRT displays.

Our DS5-075 provides NASA with a 0.00075" spot-size for their Viking Orbiter and Viking Lander satellite photography. They needed 0.01% repeatability too. And they got it. From CELCO.

Two different customers with "above-average" display needs are using CELCO CRT Display Systems for Astronomy Research. One is an observatory; they're keeping their eye on the Sun. The other is recording their Stellar Observations with a CELCO CRT Display System.

High-speed map making is the task of another CELCO customer using a CELCO precision display for topographical projects.

CELCO displays are helping a leading Oil Company in their oil explorations. While another CELCO display is being used in Eye Research.

Maps and satellites, eyeballs and oilwells. All "above-average" display requirements. If your needs are ABOVE-AVERAGE, you need a CELCO "above-average" Precision CRT Display System.

(Don't you think so too?)

Call CELCO for your "above-average" CRT Display System.

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Donald A. Mitchell, Executive Vice President, Rockwell International Electronics Group, Anaheim, Calif.
William L. Quigley, Director, Marketing and Planning, Hoffman Electronics, NavCom Systems Div., El Monte, Calif.

Session 14: The Real World of Digital Communications

Room 212B

Session Organizer and Chairman: R. W. Sanders, Computer Transmission, El Segundo, Calif.

14/1 **The User's Current Needs,** *Dixon Doll, Consultant, Ann Arbor, Mich.*

14/2 **Dataphone Digital System (DDS),** *Richard Aiken, AT&T, New York, N.Y.*

14/3 **Canadian Nationwide Dataroute System,** *David Horton, Bell Canada, Ottawa, Canada*

14/4 **International Digital Data Service (IDTS),** *Ken Jockers, Western Union International, New York, N.Y.*

Session 15: Microprocessors—The Second Generation

Room 217A

Session Organizer and Chairman: Jerry Metzger, IC Update/Master, Sunnyvale, Calif.

15/1 **The F8 Microprocessor,** *David Chung, Fairchild Semiconductor, Mountain View, Calif.*

15/2 **A New Microcomputer Family,** *Hal Feeney, Intel, Santa Clara, Calif.*

15/3 **The M6800 N-Channel Processor Family,** *Van Lewing, Motorola Semiconductor, Phoenix, Ariz.*

15/4 **FACE, A Field-Alterable Control Element,** *Philip Roybal, National Semiconductor, Santa Clara, Calif.*

15/5 **The COS/MOS Microprocessor,** *Robert Winder, RCA Solid State, Somerville, N.J.*

15/6 **The 8-Bit Parallel Processing System,** *Michel Ebertin, Rockwell Microelectronics, Anaheim, Calif.*

15/7 **The 2650 8-Bit Processor,** *Joe Kroeger, Signetics, Sunnyvale, Calif.*

Session 16: Quo Vadis Electronics?

Room 217B

Session Organizer and Chairman: Rudolf Panholzer, Naval Postgraduate School, Monterey, Calif.

16/1 **The Future of Electronics,** *Harold Chestnut, General Electric, Schenectady, N.Y.*

16/2 **The Corporation's Measurement of Success,** *William D. Walker, Tektronix, Beaverton, Oreg.*

16/3 **The Role of Telecommunications and Computers in Facilitating Technological Changes,** *William K. Linvill, Stanford University, Stanford, Calif.*

16/4 **Electronics and the Quality of Life,** *W. D. Rowe, Environmental Protection Agency, Washington, D.C.*

Thursday, September 12 Morning Sessions 10:00 a.m.–12:30 p.m.

Session 17: Hybrid Microelectronics Clinic on Semiconductor Bonding

Room 212A

Session Organizer: Stanley Stuhlberg, Raytheon, Bedford, Mass.
Session Chairman: W. B. Burford, Westinghouse Aerospace Div., Baltimore, Md.

Panelists:
W. A. Farrand, Rockwell Autonetics, Anaheim, Calif.
J. Swafford, Bendix, Kansas City, Mo.
Mauro Walker, Motorola Communications, Fort Lauderdale, Fla.
R. Ponce de Leon, Motorola Government Electronics, Scottsdale, Ariz.
Ralph Redemske, Teledyne Microelectronics, Los Angeles, Calif.
Lew F. Miller, IBM Systems Product Div., Hopewell Junction, N.Y.
Randolph Early, General Electric, Lynchburg, Va.

Session 18: Selling Your "Better Mousetrap"

Room 212B

Session Organizer and Chairman: Larry Courtney, Larry Courtney Associates, Thousand Oaks, Calif.

18/1 **Factory Salesmen or Reps—and How To Motivate Them,** *Jerry Frank, IMA, Sherman Oaks, Calif.*

18/2 **Successfully Marketing a New Product,** *Jerome Froland, John Fluke Mfg., Seattle, Wash.*

18/3 **Using the Trade Press Effectively,** *Dan McMillan, Electronics Magazine, New York, N.Y.*

18/4 **How to Work with an Advertising Agency,** *Larry Courtney, Larry Courtney Associates, Calabasas, Calif.*

18/5 **Using Publicity To Launch a New Product,** *David Simon, Simon Public Relations, Los Angeles, Calif.*

18/6 **After You've Got All the Bingo Cards—What Do You Do with Them?** *Mike Simon, Inquiry Handling Service, North Hollywood, Calif.*

Electronics Manufacturers: Why do your competitors earn up to 8 times more profits in Puerto Rico?

Find out at Wescon'74, Booth 1319

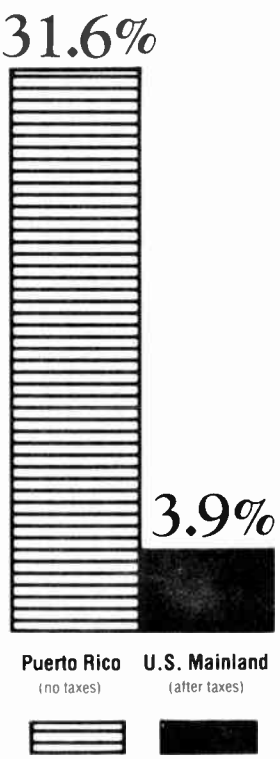
ONE look at the chart tells the story. Electronics manufacturers on the U.S. Mainland show an average profit-to-sales ratio of only 3.9%. Your competitors in Puerto Rico average 31.6%. That's eight times more profits.

RCA, Digital Equipment, Technicon, Bell & Howell, General Electric, and Westinghouse are some among the leading electronics manufacturers who have opened plants in Puerto Rico.

Here are a few of the reasons why U.S. manufacturers have come to regard Puerto Rico as the "Profit Island."

No Taxes. Because of Puerto Rico's unique Commonwealth relationship with the U.S., federal taxes do not apply. And Puerto Rico offers qualified manufacturers 100% exemption from all local taxes. That means no corporate income tax. No real or personal property taxes. No excise or municipal taxes.

Net Profit as Percent of Sales*



Intelligent Willing Workers. A labor force of 921,000 people with 100,000 immediately available for employment. And Puerto Rican workers rival the Japanese for industriousness. Most plants reach 90% to 95% efficiency within the first year of operation.

Reasonable Wages. The average hourly wage in Puerto Rico's electronics industry is $2.43, as opposed to an electronics industry average of $4.07 on the U.S. Mainland.

Factory Space Ready and Waiting. You can choose from a large inventory of both single-story and multi-level plants. Units ranging from 4,000 sq. ft. to 23,000 sq. ft. are available. And at rates as low as 75¢ per sq. ft.

Modern Transportation and Services. San Juan, a major international port, is serviced by over 30 shipping lines and 15 scheduled airlines. Point-to-point trucking service over a 6,000-mile network of roads. Electric power, water and sewage systems as advanced as any in the U.S.

No other industrial site in the world can offer the manufacturer such a unique combination of advantages. And, of course, a Puerto Rican plant gives you duty-free access to the U.S. Mainland and the protection of the U.S. Constitution.

Your competitors have already discovered Puerto Rico. Isn't it time you did, too?

*Source: (1) Latest available profitability figures (1972), Commonwealth of Puerto Rico, Economic Development Administration, Office of Industrial Economics and Promotional Services, January, 1974. (2) Federal Trade Commission Quarterly & Financial Report for Manufacturing Corporations, First Quarter, 1973.

Puerto Rico delivers on the bottom line

Circle No. 130 on Reader Service Card

Session 19: The Microprocessor Revolution—Part I

Room 217A

Session Organizer and Chairman: Rudolf Panholzer, Naval Postgraduate School, Monterey, Calif.

19/1 **A Teacher Looks at the Microprocessors,** *B. W. Jordan, Northwestern University, Evanston, Ill.*

19/2 **Systems Languages: Management's Key to Controlled Software Evolution,** *Gary A. Kindall, Naval Postgraduate School, Monterey, Calif.*

19/3 **The Monolithic Microprocessor as a Universal Standard Part,** *D. H. Chung, Fairchild Camera and Instrument, Mountain View, Calif.*

19/4 **Digital System Implementation—Microcontrollers, Microcomputers, and Minicomputers,** *C. Gordon Bell and S. Teicher, Digital Equipment, Maynard, Mass.*

Session 20: Fault Detection in Transmission Lines Using TDR and FDR Techniques (Panel)

Room 217B

Session Organizer: Martin Marshall, E-H Research Laboratories, Oakland, Calif.
Session Chairman: Al Hart, Singer Instrumentation, Palo Alto, Calif.

Panelists:
Earl Olsen, E-H Research Laboratories, Oakland, Calif.
Kenneth Lindsay, Tektronix, Beaverton, Oreg.
Gene Ball, U.S. Naval Station, Pt. Mugu, Calif.

Thursday, September 12 Afternoon Sessions 2:00 p.m.–4:30 p.m.

Session 21: The Status of Additive Printed Circuits Today

Room 212A

Session Organizer and Chairman: George Messner, Photocircuits Div., Kollmorgen, Glen Cove, N.Y.

21/1 **The Status of Additive Circuits Today,** *Sam Smookler and Joseph Cannizzaro, Photocircuits Div., Kollmorgen, Glen Cove, N.Y.*

21/2 **Additive Circuits—Users' View,** *Ignatious C. Serra, Applied Digital Data Systems, Hauppauge, N.Y.*

21/3 **Combining Additive and Subtractive Processing in the Manufacturing Facility,** *John C. Eckhardt, Methode Electronics, Chicago, Ill.*

21/4 **Dry-Film Resist of Additive Plating,** *Harold Powell, Photo Products Dept., E. I. duPont de Nemours, Wilmington, Del.*

21/5 **A Zero Liquid Effluent System for a Fully Additive Printed-Circuit Plant,** *George A. Butter, Photocircuits Div., Kollmorgen, Glen Cove, N.Y., and E. V. Klein, Abcor, Cambridge, Mass.*

Session 22: LSI Testing

Room 212B

Session Organizer: Martin Marshall, E-H Research Laboratories, Oakland, Calif.
Session Chairman: Roy Nesson, Hughes Aircraft, Culver City, Calif.

22/1 **Full-Wafer LSI Testing,** *Roy H. Nesson, Hughes Aircraft, Culver City, Calif.*

22/2 **New-Generation Test Systems To Solve New-Generation Test Problems,** *Bill Boggs and John Worcester, E-H Research Laboratories, Oakland, Calif.*

22/3 *Jack G. Salvador, Teradyne Digital Systems, Chatsworth, Calif.*

22/4 **CMOS/LSI Testing,** *George P. Nelson, Naval Research Laboratory, Washington, D.C.*

22/5 **Microprocessor Testing,** *James Fisher, Tektronix, Beaverton, Oreg.*

22/6 **Microprocessor Test Techniques,** *William J. Mandl, Macrodata, Woodland Hills, Calif.*

Session 23: The Microprocessor Revolution—Part II

Room 217A

Session Organizer and Chairman: Rudolf Panholzer, Naval Postgraduate School, Monterey, Calif.

23/1 **How To Use Your Microcomputer for All Its Worth—During Data Handling,** *Vinay Khanna, Motorola, Tempe, Ariz.*

23/2 **A Dedicated Calculator for Solution of Maneuvering Problems on U.S. Navy Ships,** *R. W. Cherry, Naval Electronics Lab. Center, San Diego, Calif.*

23/3 **Microprocessors: A Component for All Seasons,** *Mona Saba and Jack D. Grimes, Tektronix, Beaverton, Oreg.*

23/4 **Distributed Data Acquisition with Microprocessors,** *Bernie Kute and Alan Weissberger, National Semiconductor, Santa Clara, Calif.*

Session 24: Design-to-Price

Room 217B

Session Organizer: Robert A. Hullander, USN, Naval Electronics Systems Command, Washington, D.C.
Session Chairman: Julian S. Lake, Naval

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Electronics Systems Command, Washington, D.C.

24/1 **Introduction,** *Julian S. Lake, Navelex, Washington, D.C.*

24/2 **The DOD Design-to-Cost Program,** *George Sutherland, Assistant Director, Engineering Development, DDR&E, Washington, D.C.*

24/3 **Design-to-Cost in Action,** *Robert A. Hullander, Navelex, Washington, D.C.*

24/4 **Implementation of Design-to-Cost in Industry,** *Robert J. Veale, Hughes Aircraft, Fullerton, Calif.; Dick Curtis Raytheon, Goleta, Calif., J. Chabrow, TRW Systems Group, Redondo Beach, Calif.*

Friday, September 13 Morning Sessions 10:00 a.m.–12:30 p.m.

Session 25: Automatic Testing of PCBs—Ways and Methods

Room 212A

Session Organizer and Chairman: Gerald Kutcher, Inforex, Burlington, Mass.

25/1 **Practical Approach to the Problem of Test-Pattern Generation,** *Temon Taschioglou, Teradyne, Boston, Mass.*

25/2 **Automatic Diagnosis of Printed-Circuit Board Failures,** *William Martin, Zehntel, Concord, Calif.*

25/3 **Circuit-Assembly Process Verification and Fault Isolation,** *John Fluke, Jr., John Fluke Mfg., Seattle, Wash.*

25/4 **A Reasonable Approach to Distributing ATE Systems,** *David Borton, Hewlett-Packard, Sunnyvale, Calif., and William Whitehouse, U.S. Navy, Keypoint, Wash.*

25/5 **A New Approach to Logic-Circuit Testing,** *Robert Anderson, Mirco Systems, Phoenix, Ariz.*

Session 26: Emerging Display Technologies

Room 212B

Session Organizer and Chairman: Roy A. Cedarstrom, Hughes Aircraft, Fullerton, Calif.

26/1 **Optical Characteristics of AC Plasma Panels,** *Michael E. Fein, Owens Illinois, Perrysburg, Ohio*

26/2 **Operational Characteristics of a Six-Inch-by-Six-Inch, TFT-Matrix Array, Liquid-Crystal Display,** *F. C. Luo, Westinghouse Research Laboratories, Pittsburgh, Pa.*

26/3 **The Multilayer Gas-Discharge Display Panel,** *Geoffey P. Watts, Beckman Instruments, Scottsdale, Ariz.*

26/4 **A Photo-Optical Video Disk System,** *Edward M. Kaczorowski, I/O Metric, Sunnyvale, Calif.*

Session 27: Applications of Digital Logic to High-Speed Amplitude and Timing Measurements

Room 217A

Session Organizer and Chairman: Jack V. Rogers, J.V.R., Walnut Creek, Calif.

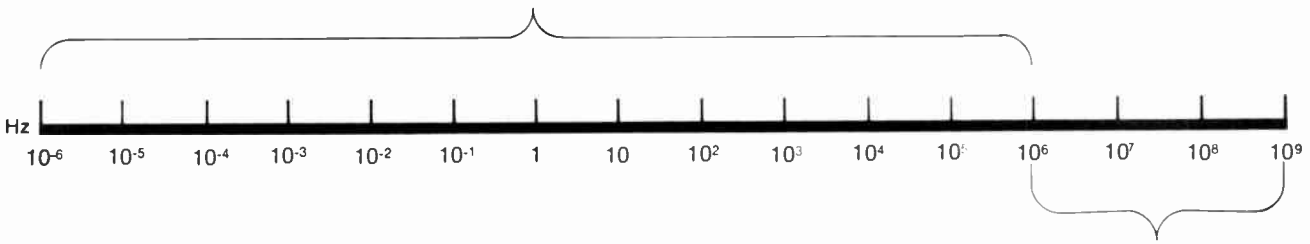
27/1 **Solving Systems Problems at "State of the Art,"** *Jack V. Rogers, J.V.R., Walnut Creek, Calif.*

27/2 **The Amplitude Axis—Digital Approaches to Generation and Measurement Problems,** *Chuck Mullett, Mullett Associates, Playa del Rey, Calif.*

27/3 **Applications of High-Speed Digital Circuits to the Time Domain,** *Zoltan Tarczy-Hornoch, Systron-Donner, Concord, Calif., and Wayne Merryman, Merryman Engineering*

Panelists:
Paul D'Anneo, J.V.R.
Seymour N. Rubin, Berkeley Nucleonics
Chuck Mullett, Mullett Associates
Zoltan Tarczy-Hornoch, Systron-Donner
Wayne Merryman, Merryman Engineering

the Nicolet 1090 digital oscilloscope is crown prince of measurement in the frequency realm from 10^{-6} to 10^{6} Hz.



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It has many times the accuracy and resolution.

It's a lot simpler and easier to operate.

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It can be used as a digital voltmeter.

It can record signals under remote control.

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