

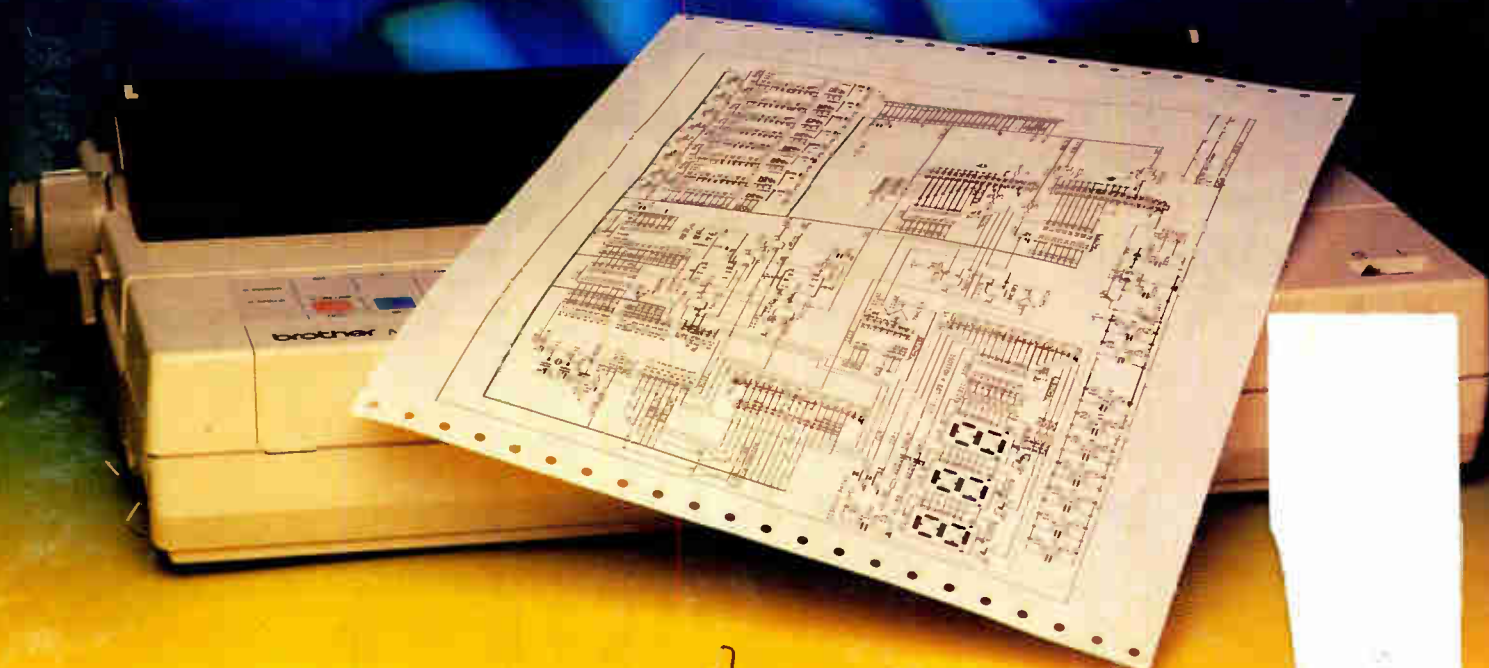
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- Audio DAC
- Fuzzy logic
- Mark 2 QTC 80/40 loop
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- Opto-card for multi-purpose bus*

* *It is regretted that, owing to circumstances beyond our control, this article had to be postponed to the July issue.*

Front cover

Print files, whether they contain text, graphics, or both, seem to become larger and larger as the programs that output them, and the printers that produce the 'hard copy', become smarter by the day. That is all very well, but nobody wants to see his fast PC held up by a simple thing like printing. A solution to this 'bottleneck' is offered by the fast intermediate storage device shown. It has a large memory—1 Mbyte or 4 Mbyte—to capture the printer data supplied by the computer and is Centronics compatible.

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EDITORIAL

- 9 Dropping Kits from Heathkit

AUDIO & HI-FI

- 24 **PROJECT:** Audio-Video Processor—Part 2
An ELV Design

COMPONENTS

- 56 Elements of Passive Electronic Components—Part 2
Design by Steve Knight, B.Sc.

COMPUTERS & MICROPROCESSORS

- 34 **PROJECT:** 4 Megabyte Printer Buffer
Design by R. Degen
- 41 **PROJECT:** Multi-Purpose Z80 Card—Part 2
Design by A. Rietjens
- 50 **COURSE:** 8051/8032 Assembler—Part 4
by Dr. M. Ohsmann

DESIGN IDEAS

- 21 Plant Warmer
by Samuel Dick

ELECTROPHONICS

- 18 **PROJECT:** Guitar Tuner
Design by W. Herrmann

GENERAL INTEREST

- 48 Analyser III: A Review
by Mike Wooding, G6IQM

POWER SUPPLIES & BATTERY CHARGER

- 32 **PROJECT:** MAX660 Inverter/Doubler
Design by J. Ruiters

RADIO, TELEVISION & COMMUNICATIONS

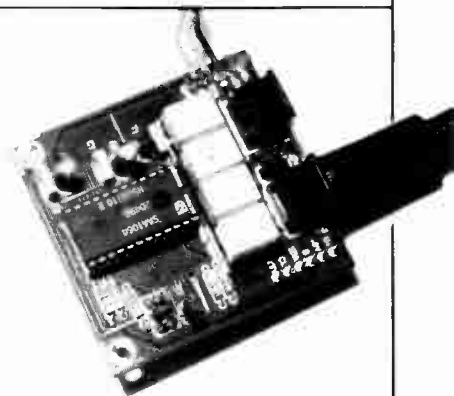
- 24 **PROJECT:** Audio-Video Processor—Part 2
An ELV Design
- 27 **PROJECT:** FM Tuner—Part 4
Design by H. Reelsen

TEST & MEASUREMENTS

- 14 **PROJECT:** I²C LED Display
Design by J. Ruffell

MISCELLANEOUS INFORMATION

Electronics Scene 10–12; New Books 13; Letters 58;
Readers Services 61; Terms of Business 62;
Advertisers' Index 60; Classifieds 60


 I²C LED display – p. 14


Guitar tuner - p. 18



Audio-video processor – p. 24



FM tuner – p. 27

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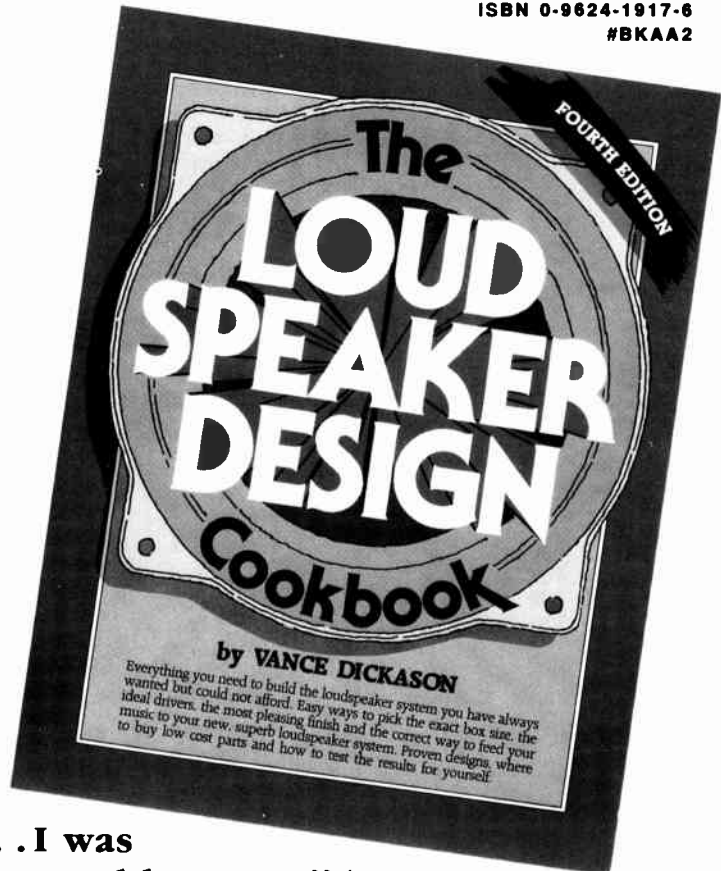
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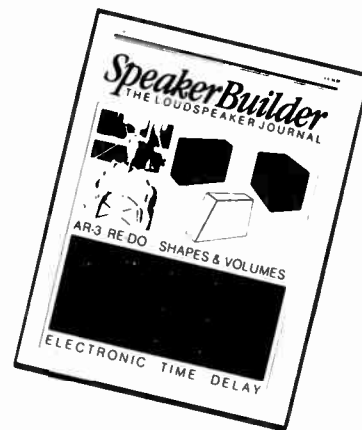
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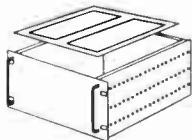
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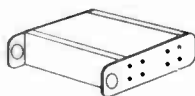
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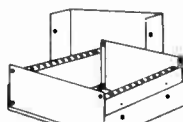
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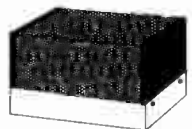


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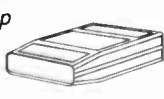
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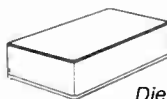
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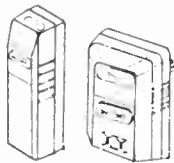
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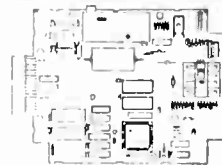
12' beige coil cord with modular plugs on each end. Small modular plugs for handset to phone connection. Retracted length is 2'.

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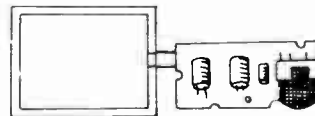
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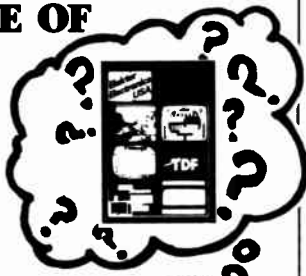
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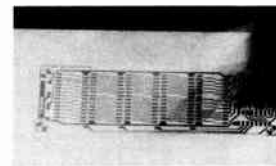
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DROPPING KITS FROM HEATHKIT

The Heath Company announced in March an end to what many have been observing as a trend for at least a decade: they are ceasing to offer electronic construction projects in kit form. When Heath delivers its last kit, a golden age will have closed. Heath set a world standard for how a do-it-yourself electronic kit should be packaged and documented.

It would be difficult to overestimate the influence of Heath's test equipment and other kit offerings on the development of an informed, enthusiastic population of technicians. Many of us moved with justified confidence from a simple amplifier kit that worked the first time it was plugged in, onward to the test and measurement instruments the company produced. A fully equipped technician's test bench was not only available in kit form, it was remarkably inexpensive. And with rare exceptions, the equipment performed better than advertised.

During that period Heath was still in the hands of its earliest staff and the enthusiasm for hand-built equipment was still understood in Benton Harbor. Inevitably, the company became a cash-cow for a series of larger conglomerates who, like most large corporations, put business types in charge of management and finally, policy. These people are almost always total ignoramuses about anything except money. Witness the fact that sometime during the 60s, Heath began to rely exclusively on advertising their catalog as their only appeal. This contrasts strongly with their earliest advertising which was multi-page and featured mouth-watering photos of the latest in electronic marvels. The company responded to such ads with information about their kits that ranged from a single sheet to eight pages. These contained photos of the device, often with interior views, and full schematics with parts values and performance specifications. But over the years, Heath's catalog became less and less technical.

What the ad people at Heath stopped understanding was that the purchaser's prime motive in buying their kits was not economy, or saving money. The appeal was the basic human instinct for making things. This instinct lives on in American society, but only in the antique, nonthreatening technologies which have not been the victim of overselling the complexities of high tech. Other cultures in Europe and the Asian rim are not covered by the technological paranoia Americans seem to enjoy. Such an attitude has been wonderfully

fruitful for those who foster the throw-away style of appliance manufacturing. While this has been great from the balance sheet viewpoint, it has been nearly totally successful in destroying the average American's technological self respect.

Thus if Heath management assumed that price was the real reason customers were buying kits, then when automated manufacturing methods for consumer gear began to develop, the cost differential between a kit and an assembled unit began to widen at an alarming rate. Kits became far more expensive to manufacture than a production line product put together entirely by machines. Also, the basic philosophy about what an appliance is, began to change. Hand-assembled units are repairable. Machine assembled units are so difficult to assemble or so costly to try to disassemble and repair, that kits began to look more and more like dinosaurs.

This disaster is of course defined by assumptions. And the assumption here is wrong. How Heath's people could have missed this basic bit of consumer information I do not understand. If you ask how I know this was their attitude the answer is simple; I asked them.

Their advertising has not, for over 25 years, paid any attention to why people build their kits. They spent no money that I know of extolling the fun of building equipment. While they listened to the designated builders among their employees, they seemed not to pay much attention to what their customers were thinking or saying.

Given the rapid rate of technological change over the last three decades, kit building's future needed some kind of re-evaluation and a conscious effort to keep it a green and flourishing enterprise in North America. Kits are alive and well in Europe and Asia. The periodicals there flourish, support, and are supported by a diverse kit industry. The US periodicals that could have continued to support kit building, or audio as handcraft, abandoned the idea in favor of higher advertising revenues from companies which made finished, higher ticket items.

I suppose we must all accept the seemingly inevitable phenomenon which we might call "the Camelot effect," which is only another way of saying that nothing which is really excellent lasts forever. But the survival time for the good ones seems to get shorter and shorter in our accelerating world.—E.T.D.

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Editor/Publisher: Edward T. Dell, Jr.

Editorial Offices:

305 Union St., P.O. Box 876
Peterborough, NH 03458-0876 USA

Telephone: 603-924-9464 (National)

or +1 (603) 924-9464 (International)

FAX: (603) 924-9467 (National)

or +1 (603) 924-9467 (International)

Advertising: Maureen E. McHugh

Telephone: (603) 358-3756

FAX: (603) 358-0157

Subscriptions: Katharine Gadwah

Elektor Electronics USA

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Uitgeversmaatschappij Elektor b.v.

P.O. Box 75

6190 AB BEEK

The Netherlands

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FAX: +31 46 37 01 61

European Offices:

Elektor BV

Postbus 75

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Telephone: 011 31 4638 9444

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Elektor EPE

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Editor: E. Xanthoulis

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Elektor Elektronikai folyoirat

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Editor: Lakatos Andras

INDIA

Elektor Electronics PVT Ltd

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Editor: Surendra Iyer

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Elektorcal

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1000 LISBOA

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SPAIN

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FREE HAM CATALOG

MFJ Enterprises, Inc., releases its free 1992 Ham Catalog containing new product announcements of accessories for Ham radio operators. The catalog includes their 20-page amateur radio new products listings, Ameritron amplifier and other new product offerings, with complete descriptions and prices of all items.

For a free copy, contact MFJ Enterprises, Inc., PO Box 494, Mississippi State, MS 39762, (800) 647-1800.

TECHNICAL NOTES

ARX Systems' second newsletter in a series of three application notes (*EEUSA* 5/92, p. 12) concerns the Afterburner, a compressor limiter. Suggestions from audio engineers and the ARX design team form the basis for these practical uses for the Afterburner. The notes, while primarily intended for users of ARX Systems' products, contain technical information applicable to similar products. Available to anyone who sends a self-addressed stamped envelope, the company plans to release one set of notes per month.

Contact ARX Systems, PO Box 842, Silverado, CA 92676-0842, (714) 649-2346.

CATOPRENE CABLES

Cat Wire and Cable Corporation introduces a line of flexible multiconductor Catoprene cables for use in electronic control, audio, instrumentation, and general interconnect applications. The Catoprene jacket, available in 12 colors, offers high and low temperature performance, is abrasion-, flame-, and oil-resistant, and are an alternative to rubber-jacketed cables. They are available in both shielded and unshielded versions from 2-30 conductor in AWG sizes 10-26.

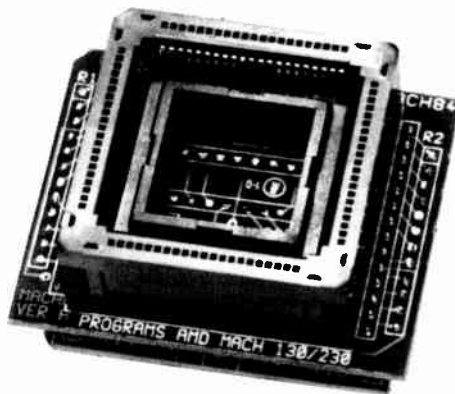
Catoprene cables are also available in zero halogen constructions. For details, contact Cat Wire and Cable Corp., 1139 NW 72nd St., Miami FL 33150, (305) 836-3600.

ELECTRONICS SCENE

DIP ADAPTERS

Logical Systems Corporation offers three adapters for use on BP Microsystems, Digelec, and Logical Devices programmers. The PA-MACH210 for \$115 supports MACH 110 and MACH 210; the PA-MACH68 supports MACH 120 and 220 for \$165; and the PA-MACH84 supports MACH 130 and 230 for \$199. They plug into the 28-pin ZIF socket of the logic programmer and accept MACH devices for programming. They are all high density, CMOS, 84-pin PLCC packages. A socket extender and pin protector are included with each adapter.

For information, contact Logical Systems Corp., PO Box 6184, Syracuse, NY 133217, (315) 478-0722, FAX (315) 475-8460.



WARNING DEVICES

Scantek, Inc., distributes two dynamic warning devices for areas with potentially high sound levels. The Electronic Orange (GA904), for control of amplified entertainment noise, uses the cut-off principle if the sound exceeds a preset, adjustable level. If the warning lights remain on for a given time, the amplification power is cut off automatically.

A Noise Activated Warning Sign (GA902) alerts industrial workers when noise exceeds a preset, adjustable level as well, an LDC advising them to don approved hearing protection.

Contact Scantek, Inc., 916 Gist Ave., Silver Spring, MD 20910, (301) 495-7738, FAX (301) 495-7739.

In "Electronics Scene" (*EEUSA* April 1992, p. 13), the incorrect area code accompanied the item, "Fiber Optics Primer." Industrial Fiber Optics' corrected phone number is (612) 731-8459.



COAXIAL ASSEMBLIES

Nemal Electronics International, Inc., announces a line of EMI/RFI suppressed coaxial and multiconductor cable assemblies, available in 50 and 75Ω versions with either type N, BNC, or UHF connectors. The multiconductor assemblies are available in 2- to 40-conductor configurations with D-subminiature or circular connectors. They offer optimum performance over the desired frequency range; exact position and mechanical integrity are provided by a section of heat-shrink tubing. They are available in assorted colors and tested for continuity and dielectric withstand voltage.

Specify length, frequency range, cable and connector types for pricing. Contact Nemal Electronics International, Inc., 12240 NE 14th Ave., North Miami, FL 33161, (800) 522-2253, FAX (305) 895-8178.

INSTRUMENT CATALOG

Specialized Products Company produces a comprehensive and informative free catalog, with 256 pages listing 5,000 electronic tools, test equipment, and service accessories for applications in computer/electronic, data communications, and telephone service requirements. Products are guaranteed and next-day delivery is available. This 64-page supplement updates the full catalog.

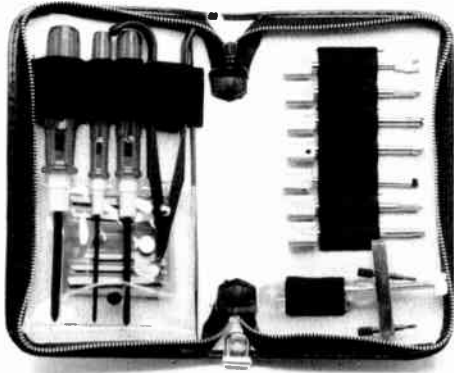
Request your full catalog and/or the 1992 Update on Test Equipment from Specialized Products Company, 3131 Premier Dr., Irving, TX 75063, (800) 527-5018.

WINDOWS 100 AWARD

Acoustic Research (AR) announced that the Powered Partner 570 is the winner of the Windows 100 Award, chosen as this year's best hardware product for use with PCs. It is the only loudspeaker selected to earn this honor. The Powered Partner is a two-way, amplified, acoustic suspension system which provides reference quality performance from a small enclosure. It uses a 5" polypropylene woofer fitted with a butyl surround and delivers 35W RMS. The 570 costs \$475 per pair. To obtain review samples, call Glen Ilacqua at (800) 225-9847.

VCR-TOOLS PACK

Techni-Tool offers a set of 21 tools for technicians to service, repair, align, and adjust most VCRs. Tec-Tuff® VCR Service/Repair Kit contains the tools in a convenient zipper pouch for easy transporting. Request information on cleaning products or a free 240-page catalog from Techni-Tool, 5 Apollo Rd., PO Box 368, Plymouth Meeting, PA 19462, (215) 941-2400, FAX (215) 828-5623.



CARVER'S DCC PLAYER

Carver Corporation announces the Carver DTD-1880, a digital compact cassette (DCC) for home use which lets you record and play CD-quality digital audio in a tape format, while also allowing you to play back conventional analog audio-cassette tapes.

The DTD-1880 offers flat-frequency response, low distortion, and wide dynamic range. It has Dolby B and C noise reduction for playback of analog tapes. Music can be accessed from both sides of the tape, a ninth track is free for tape management, and a pair of stereo analog playback heads improve conventional tape performance.

Efficient data usage is due to precision adaptive sub-coding (PASC), a process which reduces data needed for sound recreation. The DTD-1880's fluorescent display shows album and song titles, vocalist's name, elapsed time, and other information. It offers connections to three types of inputs and outputs: analog, digital, and digital fiber optic. Price ranges between \$800-\$900.

For further information, contact Carver Corporation, PO Box 1237, Lynnwood, WA 98046, (206) 775-1202, FAX (206) 776-9453.



ELECTRONICS SCENE

GLOBAL STANDARDIZATION

The American National Standards Institute (ANSI) second effort to effect international standardizations comes in video form titled "Global Connections," which is available to senior management at major US corporations. In it, three leading US executives offer their views on the significance of standardization in the global marketplace. Copies of the video are available on a loan-basis, with a handling fee, for a period of three weeks; FAX those requests to the attention of Russell Bodoff at (212) 398-0023. Those interested in purchasing the video, contact ANSI's Customer Service Department at (212) 642-4900. It costs \$25 for ANSI members; \$50 for nonmembers.

The first part of this educational-awareness campaign was *FORTUNE* magazine's publication of a supplement titled "Global Connections: The Quest for Worldwide Standardization." Copies of the insert are available by FAXing ANSI's External Relations Department at (212) 398-0023.

Other queries, write ANSI, 11 West 42nd St., NY, NY 10036.

TRAVEL INK JET

Eastman Kodak Company offers its Diconix 701 printer that provides laser-quality from its first mobile ink-jet type. Featuring 300 x 300 dots-per-inch resolution in an 86.6 sq. in. footprint, the 701's feeder holds up to 30 pages of paper, its print speeds are competitively fast, and internal font rotation allows storage. It includes an MS Windows driver, two built-in printer emulations, and compatibility with a variety of software. DOS-compatible, the Diconix 701 (\$549 in the US; \$675 in Canada) weighs under six pounds without batteries and has an optional Ni-Cad rechargeable battery.

For more information about printer products, call (800) 344-0006.



HAND-HELD TERMINAL

Two Technologies, Inc., releases the PDS, a programmable, full-function ASCII, handheld terminal designed for a variety of applications. The software developed on one computer can be downloaded to the PDS or the PDS can be reprogrammed in the field by downloading via modem.

Other features include an 8051 microprocessor, serial UART to 19,200 baud, 32k-bytes, battery-backed RAM, 128 bytes non-volatile EEPROM, 4-line by 20-character liquid-crystal display (LCD), programmable LCD contrast control, and a full-function speaker. Housing is ergonomically designed to be both rugged and comfortable to use.

Contact Two Technologies, Inc., 419 Sargon Way, Horsham, PA 19044, (215) 441-5305, FAX (215) 441-0423.

THERMOCOUPLE CARD

Global Specialties offers an eight-channel Thermocouple card, the Model TIP-8, which plugs directly into an I/O slot of an IBM PC-compatible, allowing eight thermocouple inputs for measuring temperature. The card combines the functions of a standard analog input card with the functions of thermocouple amplifiers, avoiding the cost and inconvenience of external equipment. The TIP-8 (\$375) uses a 12-bit converter to produce an 8-bit temperature measurement. Measurement ranges are programmable, the on-board linearizer accepts one thermocouple type, and a 16-point connector is provided.

Contact Global Specialties, 70 Fulton Terrace, New Haven, CT 06512, (800) 572-1028, FAX (203) 468-0060.



RUGGED MAINFRAME

IBI Systems, Inc., announces the Model ST-4100E personal rack-mount computer box meeting NEMA-12 standards. Its switched 300W power supply operates at 100kHz. The unit is 20G operating shock tolerant. Designed for rugged industrial uses, its 12-slot passive backplane accepts any processor board, PC enhancement boards for video imaging, process control, data acquisition, or telephone networking. Priced from \$2,700 to \$5,900, the ST-4100E weighs 25 lbs., sports a keylock switch, and offers a year's warranty.

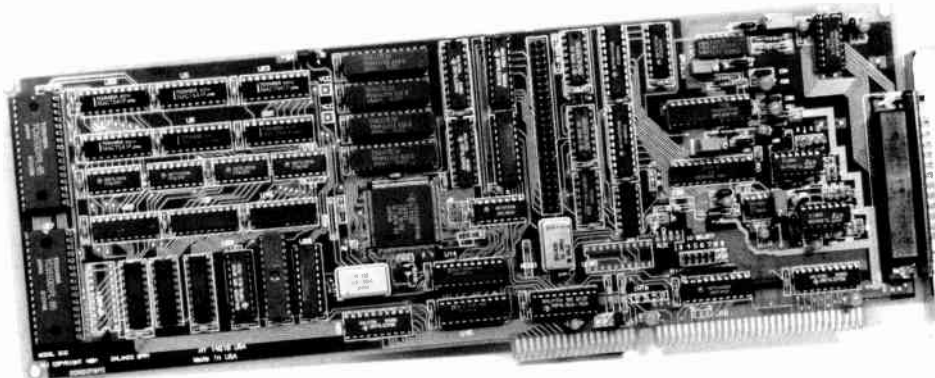
Contact IBI Systems, Inc., 6842 NW 20th Ave., Fort Lauderdale, FL 33306, (305) 978-9225, FAX (305) 978-9226.

DSP BOARD

Dalanco Spry announces the Model 500, a digital signal processing (DSP) board with analog and digital I/O. Designed for PC AT and ISA-bus compatible microcomputers, applications include instrumentation, telecommunications, biomedical, audio, and DSP software development. It provides data acquisition for eight channels at 12-bit resolution and a maximum of 225kHz sampling rate.

The Model 500 includes two 12-bit analog output channels, a buffered digital I/O connector for user expansion, and two serial interfaces of the TI DSP. A variety of software accompanies the Model 500: TMS320C51 Assembler and Debugger, FFT, real-time signal and spectrum display, concurrent record and playback to or from disk, digital filter examples, FIR filter code generator, and a waveform editor.

The Model 500 with TMS320C51 costs \$1,600. For further details, contact Dalanco Spry, 89 Westland Ave., Rochester, NY 14618, voice and FAX (716) 473-3610.



ELECTRONICS SCENE

INSTANT PC BOARDS

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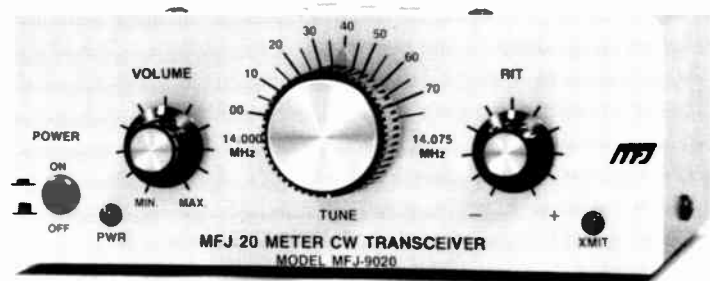
Five sheets of 8½" × 11" transfer paper and a special iron-protector sheet are included for \$9.95 plus \$2.50 shipping (California residents add 8.25% sales tax). Contact Dyna Art Designs, 3535 Stillmeadow Lane, Lancaster, CA 93536-6624, (805) 943-4746.



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PORTABLE TRANSCEIVER

MFJ Enterprises, Inc., announces the Model MFJ-9020, a 5W 20M CW transceiver that covers 14.000-14.075MHz, has a superhetrodyne receiver, RIT, audio-derived AGC, and a built-in earphone jack. This transceiver, which fits easily in a briefcase, has an 8-pole crystal filter with 500Hz bandwidth, Vernier tuning, and operates from 12-15V DC.

The Model MFJ-9020 costs \$39.95. For details, contact MFJ Enterprises, Inc., PO Box 494, Mississippi State, MS 39762, (800) 647-1800.

DOS LOGIC SIMULATOR

Capilano Computing Systems Ltd. has now released an MS-DOS version of LogicWorks, an educational electronic schematic and simulation software package, formerly available only to Mac users. Its fully interactive digital simulation lets probes, displays, and switches be placed directly on the circuit diagram so that it operates like a real circuit breadboard. Clicks of the mouse can change device delays, clock rates, and signal connections letting you test circuit ideas on the spot. The simulator uses 13 different logic states to correctly predict resistive drives, pullups, open-collector devices, and unknown states, handles an area up to 5ft² and simulates thousands of elements from gates to TTL parts to microprocessors, and allows you to create your own symbols and more.

LogicWorks costs \$300; discounts are available to students and educational institutions.

For information, contact Capilano Computing Systems Ltd., 960 Quayside Dr., Suite 406, New Westminster, BC, Canada, V3M 6G2, (800) 444-9064, (604) 522-6200, FAX (604) 522-3972.

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Edited by Ian Hickman

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This book could be subtitled "The Best of EDN." Since its first appearance in 1956, EDN magazine has established for itself the unassailable position as the most useful and widely read of the controlled-circulation electronics magazines with a combined, fortnightly circulation in the USA, UK, and Europe of over 160,000.

The selection of articles from EDN reflects the editor's interests as a longstanding analog-circuit design engineer, but digital subjects are far from ignored.

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This book is the second English edition of an international best seller on electronic circuit design and application. It has been thoroughly updated and expanded. Aimed at the student, practicing engineer, and scientist, it covers all important aspects and applications of modern analog and digital circuit design. Part I, Basics, contains the material of a one-year's undergraduate course on elementary electronics and describes the circuit components by their electrical behavior rather than by their semiconductor physics.

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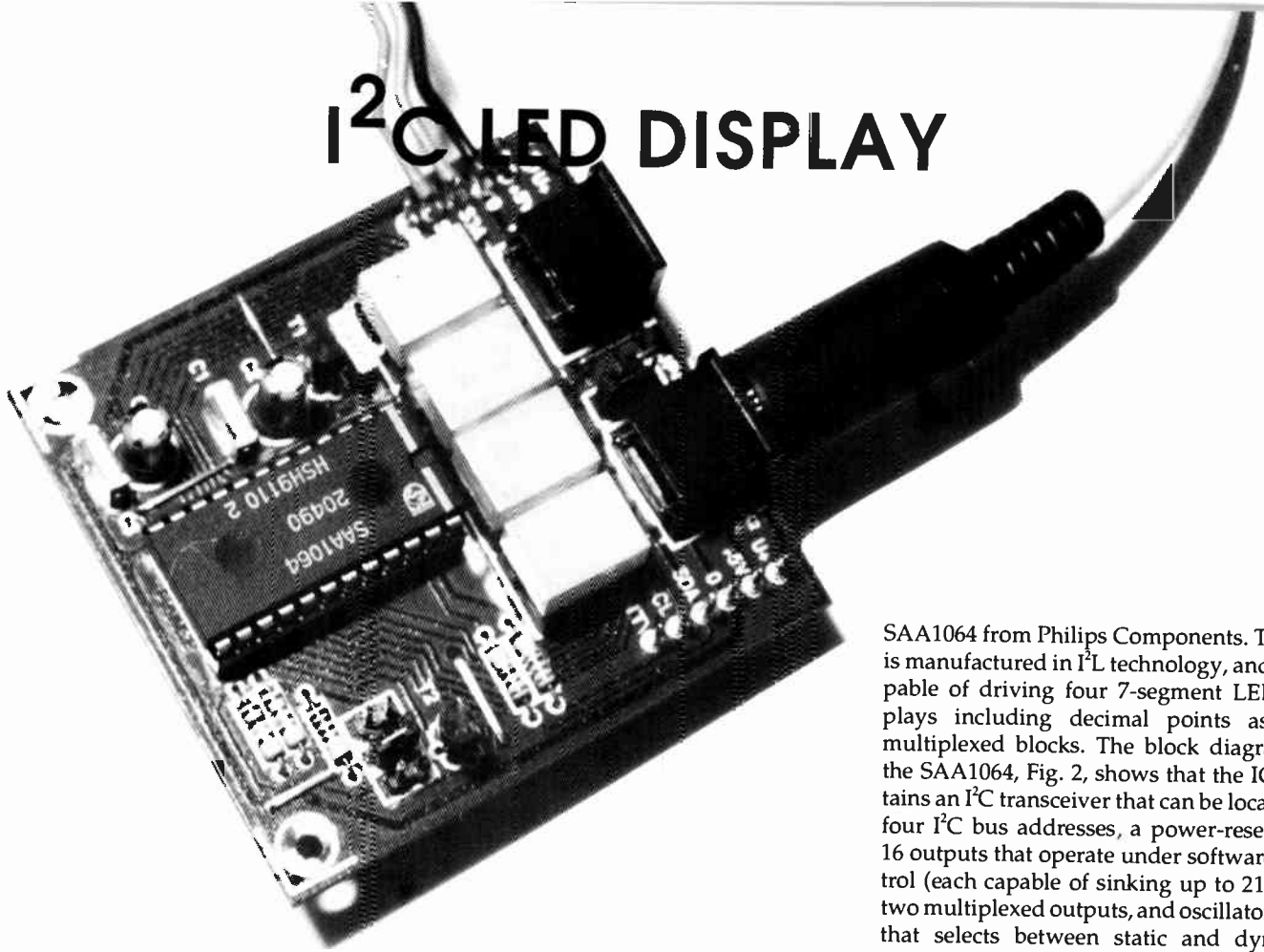
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I²C LED DISPLAY



Our earlier publications on I²C-compatible circuits having met with a great deal of interest, we now move on to a four-digit seven-segment LED display unit that can be used in many applications as a bright and easy to drive readout.

Design by J. Ruffell

SO far it has appeared a matter of course that the readout function in a computerized measurement system is invariably provided by the screen of the PC. The present 4-digit LED display unit may, however, prove an attractive alternative in many cases. It allows a PC fitted with an I²C controller card (Ref. 1), or any other I²C controller, to indicate, for instance, measured data in bright green, red or yellow numbers on an LED display. In other words, it is no longer necessary to reserve a part of the PC's screen for displaying measured values. This means that the PC can continue to run its main program, while a background program takes care of outputting measurement data to the LED display at regular intervals.

Another possibility is to use the display as a time and/or date indication. In a PC, the parameters needed for this application are easily copied from the system software or the PC's internal real-time clock. Another possible application that comes to mind is to use the display to bring to your attention the status of a certain measurement program that runs in the background.

The present display is, of course, software-compatible with the I²C device driver published earlier (Ref. 2), and its control is, therefore, 'food for programmers'. Those of you who work with microcontrollers will also find that the I²C display unit is readily used and fairly simple to control. Today, an increasing number of microcontrollers is available with an on-chip I²C interface, which makes connecting the present display unit a piece of cake.

The circuit

The circuit shown in Fig. 1 is best described with three words: compact, simple and inexpensive. Apart from one IC, two transistors and, of course, four 7-segment LED displays, only a handful of passive parts is required to complete the circuit. As with the other circuits in our I²C series, the communication with the outside world is via two miniature 6-way DIN sockets. A length of 6-way cable is all that is required to convey the two serial signals, ground, the supply voltage and an interrupt signal (the +5 V supply voltage is carried via two wires).

The heart of the circuit is formed by a four-digit I²C-compatible LED driver Type

SAA1064 from Philips Components. This IC is manufactured in I²L technology, and is capable of driving four 7-segment LED displays including decimal points as two multiplexed blocks. The block diagram of the SAA1064, Fig. 2, shows that the IC contains an I²C transceiver that can be located at four I²C bus addresses, a power-reset flag, 16 outputs that operate under software control (each capable of sinking up to 21 mA), two multiplexed outputs, and oscillator, a bit that selects between static and dynamic mode, and, finally, a bit for test purposes.

As could be expected of an I²C application circuit, the control of the display driver is a matter of sending the right command to a previously determined address, which is the 'location' of the IC in the I²C network. Here, the address of the SAA1064 can be set with the aid of jumpers. Remarkably, only one IC pin is used to select one of four possible addresses in the system. Resistors R₃, R₄ and R₅ form a voltage divider which supplies the address selection voltage to the ADR pin of the SAA1064. The voltage level, i.e., the IC address, is determined by three jumpers. The four voltage levels that can be set are 0 V, 3/8V_{cc}, 5/8V_{cc} and V_{cc}. Each of these levels corresponds to one of the four combinations of the two address bits, A₀ and A₁.

The base address of the SAA1064 is

0 1 1 1 0 A₁ A₀ x

To select an address, fit the jumpers as shown in Table 1. All other bits in the I²C ad-

Table 1.

A0	A1	JP1	JP2	JP3
0	0	0	1	0
1	0	0	0	0
0	1	0	0	1
1	1	1	0	0

0 = open

1 = jumper fitted

addresses are 'burnt' in the IC hardware, and can not be changed. As usual with I²C compatible ICs, the 'x' at the end of the address is a bit that selects between a read (x=1) or a write (x=0) operation. The 'read' addresses are 70H, 72H, 74H and 76H. The 'write' addresses are 71H, 73H, 75H and 77H.

Transistors T1 and T2 are required to multiplex the four common-anode displays pair-wise. They function as switches, with the hardware in the SAA1064 determining the current flow through the display segments. Software control allows the segment current to be set between 3 mA and 21 mA in steps of 3 mA. In dynamic mode, the segments light about half the time (48.2% typ. min.). The circuit configuration used here results in a multiplex frequency of about 150 Hz, which can be increased to about 800 Hz or 1,500 Hz by reducing C5 to 820 pF or 390 pF respectively.

The multiplex duty factor results in an average segment current that is about half the programmed current. Since the brightness of the Type HD11050 LED displays (manufacturer: Siemens) is sufficient at a segment current of 4.5 mA, a segment current of 9 mA is programmed.

Jumper JP4 allows the display to be powered by a separate supply, which may be required when more than one display is used. The external voltage is applied via PCB terminal 'U+', and may be up to 15 V, pro-

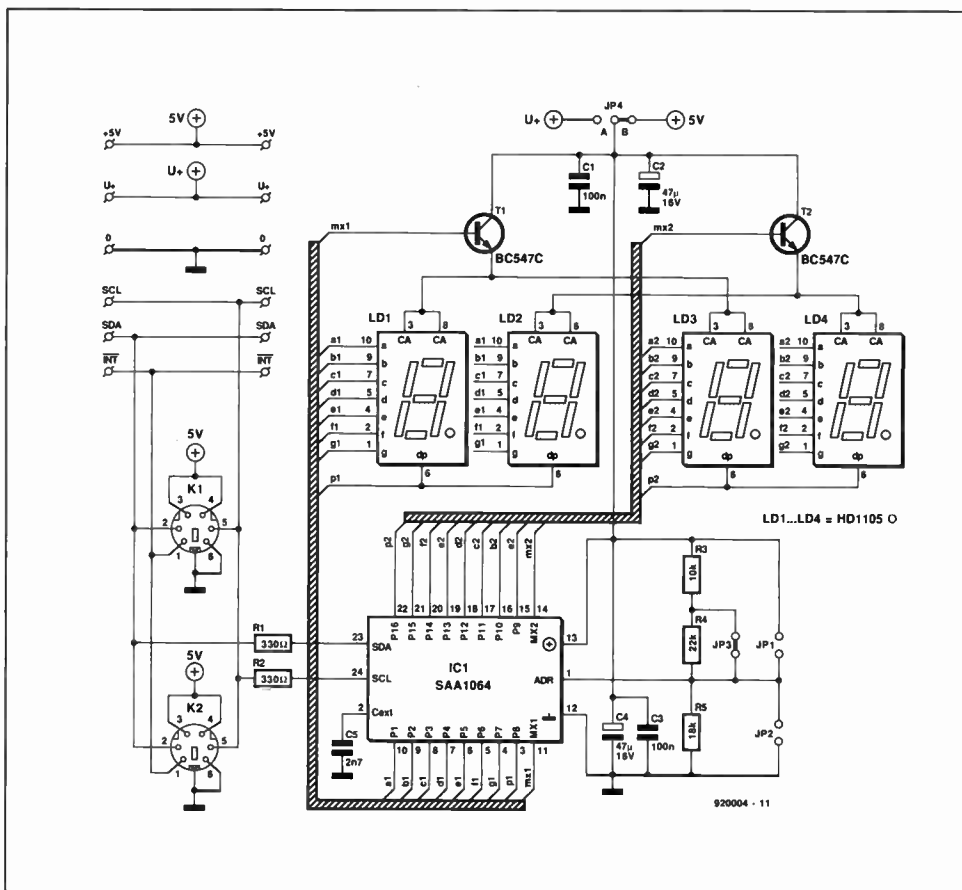


Fig. 1. The circuit for driving four 7-segment displays is very compact thanks to the power of the I²C protocol.

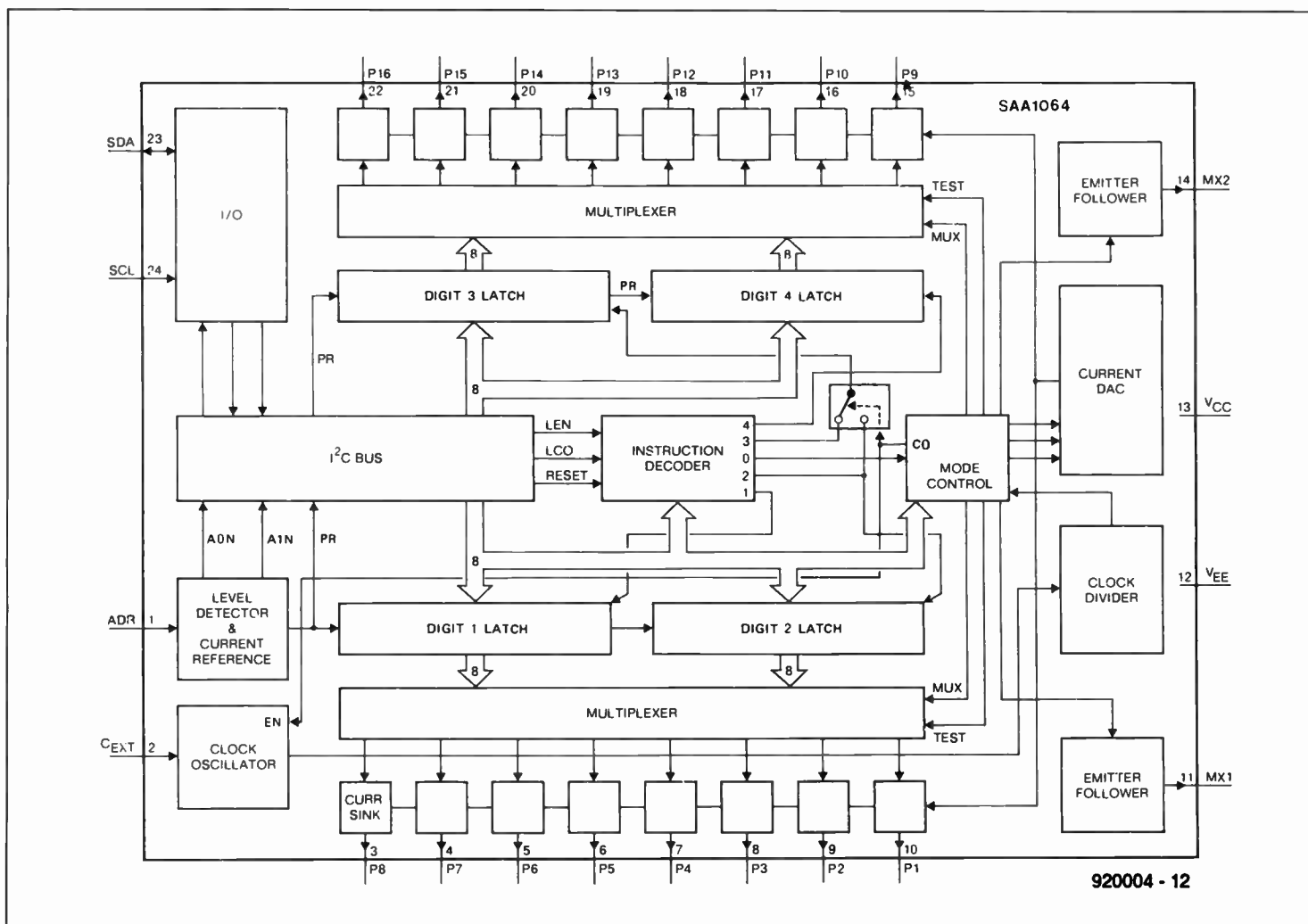


Fig. 2. Internal diagram of the SAA1064 LED display controller (courtesy Philips Components).

Figure 4 shows how the controller communicates with the SAA1064. Reading results in a status byte, which, among others, shows the state of the power-reset flag. This flag is set by the SAA1064 when power is applied, after which all registers contain zeroes, and the display is blank.

There are a number of ways in which we can write to the SAA1064. Writing to the device requires the relevant control register to be set to the right mode, and data to be sent to the display digits. After addressing the SAA1064, an instruction byte is sent that selects one of the eight internal registers. Which register is selected first is determined by the level of bits SA, SB and SC. The auto-increment function of the IC ensures that the next register is automatically selected for writing to. The pointer of the auto-increment function is cyclic, and changes to '0' again after '7'. The three least-significant bits of the instruction byte select the registers as follows:

b2 b1 b0

0	0	0	control register
0	0	1	LD1 register
0	1	0	LD2 register
0	1	1	LD3 register
1	0	0	LD4 register
1	0	1	free
1	1	0	free
1	1	1	free

where b7 to b3 = 0

The structure of the control byte is as follows:

- b0 = 1: dynamic mode (multiplex digits)
- b1 = 1: enable digits 1 and 3
- b2 = 1: enable digits 2 and 4
- b3 = 1: segment test, all outputs active
- b4 = 1: increase segment current by 3 mA
- b5 = 1: increase segment current by 6 mA
- b6 = 1: increase segment current by 12 mA
- b7: reserved

A segment is actuated (switched on) by making the associated bit '1'; a '0' switches it off again. This means that we are not limited to just displaying numbers 0 through 9: characters A through F are also possible, which is useful for making a hexadecimal readout.

Diskette ESS 1671 contains a demonstration file, LDIS.PAS, which contains the I²C driver as well as the routines for controlling the A-D/D-A converter and the I/O port. LDIS.PAS is written in Turbo Pascal. Figure 5 shows the main procedure, which starts with moving the decimal point of the most significant digit to the least significant digit. Next, the program counts up from 0 to 9999, and starts again. The counter values appear on the display as well as on the PC screen. ■

References:

1. "I²C Interface for PCs," *Elektor Electronics USA*, February 1992.
2. "ADC/DAC and I/O for I²C Bus," *Elektor Electronics USA*, March 1992.

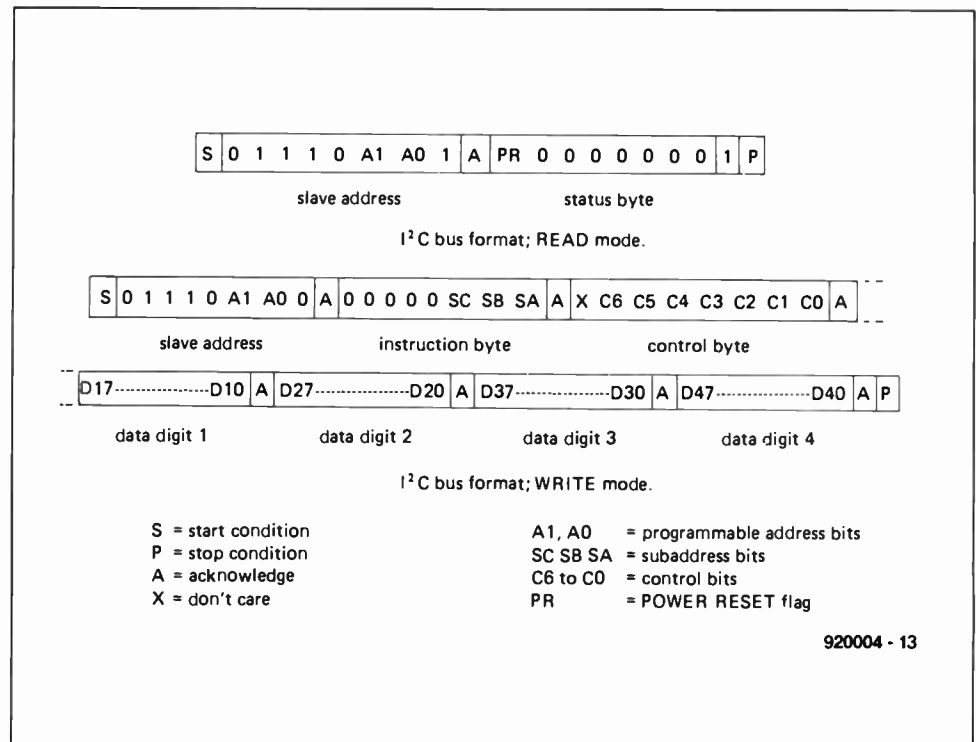


Fig. 4. Sending commands to the controller is pretty simple if you make use of the I²C driver contained on the floppy disk supplied for this project.

```

begin (* LedDisplayTest *)
  Start (Bus);                                {-Start communication on I2C-bus.}

  InitLedDisplayTest;

  Address (DisplayAddr);                       {-After being addressed, the LED-driver
                                                expects an instruction byte.}

  Inst:=GetInstructionByte(1);                 {-The byte following the instruction
                                                byte will be stored in the control
                                                register....}

  write (Bus, Inst);

  Ctrl:=GetControlByte(1);                     {-Prepare loop.}
  Counter:=0;

  Repeat
    write (Bus, Ctrl);                         {- go!}

    with Digit do
      begin
        Split (Counter, D1, D2, D3, D4);
        write (Bus, DCode [D1], DCode [D2], DCode [D3], DCode [D4]);
      end;
    Screen(1);

    write (Bus, Du, Du, Du);                   {-After these three dummy bytes have
                                                been sent, the LED-driver expects
                                                a control byte again....}

    delay (t);

    if Counter=0                               {-Shift decimal points.}
      then
        for Counter:=5 downto 0 do
          begin
            write (Bus, Ctrl, DP, B1, B1, B1, Du, Du, Du); Screen(2); delay (t);
            write (Bus, Ctrl, B1, DP, B1, B1, Du, Du, Du); Screen(3); delay (t);
            write (Bus, Ctrl, B1, B1, DP, B1, Du, Du, Du); Screen(4); delay (t);
            write (Bus, Ctrl, B1, B1, B1, DP, Du, Du, Du); Screen(5); delay (t);
          end;

          inc (Counter);
          if Counter>MaxCount
            then
              Counter:=0;
        Until keypressed;

  UnInitLedDisplayTest;

  Close (Bus)                                  {-Stop communication on I2C-bus.}
end. (* LedDisplayTest *)

```

920004 - 14

Fig. 5. Main procedure in the display test program LDIS.PAS.

GUITAR TUNER

Design by W. Herrmann

This tuner was designed because many commercial (analogue) models were found not robust enough for the practical, hard use required of them. After all, a guitar is an instrument that needs to be tuned daily.

IN THE design of the tuner, hands-off operation was a prime requirement. Consequently, all functions are either automatic or foot-operated. The input is connected to the output as long as the tuner is not in use. That means that it can remain in the signal path between the guitar and the amplifier system.

When the 'on' button is pressed (by foot), the unit is switched on, provided a plug is inserted into the input socket. At the same time, the output of the unit is removed from the amplifier, so that no tuning signals are output over the speakers.

When the unit is on, the LED associated with the high E ($f_E = 329.63 \text{ Hz}$ – equal temperament tuning) lights. When the high-E string is plucked, several LEDs light. If the band of light appears to move to the left, the played tone is too low; if it moves to the right, the played tone is too high. There is a period of 20 seconds to tune the string; correct tuning is indicated by the band of light standing still.

Each subsequent pressing of the 'on' button switches the tone to the next lower note, B_1, G_1, \dots, E_2 , indicated by the lighting of the associated LED. In each case, there is a period of 20 seconds to tune the relevant string. At the seventh pressing of the button, the LED associated with the high E lights again.

Tuning may be ended with the second footswitch, which switches the tuner to standby, whereupon the guitar signal is reconnected automatically to the amplifier.

If the 20-second period is not long enough to tune a string, the unit must be returned to operation at the relevant frequency by repeatedly (six times) pressing the 'on' button. Neither on-switching nor off-switching causes any audible noise or contact bounce.

Crystal control

The circuit in Fig. 1 depends for its correct operation on a crystal-controlled oscillator, $IC_{5a}-IC_{5b}-IC_{5d}$, and a divider, $IC_6-IC_8-IC_{9a}$, that is programmed by a diode matrix. To keep the current drain down to a minimum, all ICs used are CMOS types.

The oscillator output is used to clock IC_6 . The Q_0-Q_{11} outputs of this circuit are fed to a diode matrix with which a number of scale factors can be preset. Only six of the eight columns of the matrix are used here: one for each string of the guitar.

The scaled-down oscillator frequency is used as a reference and as clock for binary counter IC_2 , which controls multiplexer IC_1

via its outputs 0–3.

An LED is connected to each of the 16 outputs of the multiplexer. The LEDs form a 'running light' that, depending on the frequency of the plucked string, moves from D_1 to D_{16} or vice versa. The 'running light' effect arises because the E input of IC_1 is controlled by the signal from the guitar. Only when the reference frequency is an exact quadruple or octuple of the measured guitar signal, will the running light stand still. If the frequency of the guitar signal is not correct, the running light moves in a direction that depends on whether the frequency is too high or too low. The larger the difference between the reference and guitar signal frequencies, the faster the running light moves.

Opamps IC_{3a} (threshold switch) and IC_{3b} (amplifier) convert the sinusoidal output voltage from the guitar pickup into a rectangular signal to drive the multiplexer.

Immediately after switch-on, all outputs of IC_6 are logic low, the oscillator begins to operate, and IC_6 starts to count. The reverse-biased diodes of the first matrix column and pull-up resistor R_{20} at the input of D bistable IC_8 provide an AND function: the level at pin 3 of IC_8 can go high only when those outputs of IC_6 that are connected to diodes in the first matrix column are high. That condition is met only at certain states of IC_6 . The consequent logic 1 becomes available at the output of IC_9 (pin 1), whereupon IC_6 is reset. Without IC_9 , the reset pulse would be too short to clock IC_2 .

Counter IC_{11} drives the three address lines of IC_8 in binary form; it proceeds one step every time a clock pulse, debounced by $R_{13}-C_8-IC_{10a}$, arrives from 'on' switch S_1 at its input. At the same time, demultiplexer IC_7 , which operates in step with IC_8 , causes one of LEDs $D_{17}-D_{22}$ to light to indicate which of the guitar strings can be tuned.

After S_1 has been pressed six times, output 6 of IC_7 goes high, which causes a reset



of IC_{11} .

After switch-on, the tuner is always preset to the high E string frequency because of the reset provided by $R_{19}-C_{13}$.

In the standby mode, battery power is available but the tuning mode is disabled. In this state, only three ICs are powered: quadruple analogue switch IC_4 ; bistable IC_9 ; and inverter $IC_{10a\dots f}$. In this mode, the current drain is a mere $1.5 \mu\text{A}$.

When, in the standby mode, S_1 is pressed, bistable IC_{9a} is reset, whereupon T_1 is switched on to provide power to the remaining ICs. At the same time, analogue switch IC_{4b} connects the guitar output to the amplifier, IC_{4c} becomes high-impedance, and IC_{4d} short-circuits the output of the tuner.

Capacitor C_{12} is charged slowly via R_{16} . After about 20 seconds, the voltage across it has reached the threshold level of IC_{10b} , and this inverter then switches off the tuner via gate IC_{10c} . If, before the 20-second period has elapsed, the 'on' button is pressed, for instance, to allow the next string to be tuned, C_{12} discharges via IC_{10a} , D_{26} and R_{25} , whereupon there is a further delay of 20 seconds before the tuner is switched off.

Stop button S_2 can, of course, reset bistable IC_{9a} at any moment if required.

In practice, a period of 20 seconds has been found just right for tuning a string. The period may, however, be made longer by increasing the value of C_{12} .

The battery voltage is monitored by IC_{10e} ,

- Tuning indication by LED running light
- Suitable for bass and guitar
- Foot operated
- Six reference frequencies with a tolerance of $<0.05 \text{ Hz}$
- Loop-through connection
- Amplifier muted during tuning
- Low current drain: 20 mA during operation; $1.5 \mu\text{A}$ during standby
- Battery life about 2 years
- Low battery indication
- Automatic or foot-operated switch-off

where f_s is the fundamental frequency of the relevant string—see Table 1. Once the scale factor has been determined, it has to be incorporated into the diode matrix.

For instance, the scale factor for the E string (equal temperament tuning) is calculated as follows.

$$f_c = 2.4576 \text{ MHz};$$

$$f_s = 329.63 \text{ Hz};$$

$$f_r = 8 \times 329.63 = 2637.04 \text{ Hz}.$$

$$\text{Scale factor} = 2.4576 \times 10^6 / 2637.04 - 1 = 931$$

The outputs of IC₆ have been given binary values as shown in Fig. 1. The diodes in the matrix must be connected in such a manner that the sum of six of the outputs is equal to the scale factor. How this is done for the E string is shown in Table 2. The string, its fundamental frequency (equal temperament tuning), the reference frequency and the resulting scale factor are tabulated in Table 3. The maximum tolerance on the tuned frequency is <0.05 Hz.

Construction

Building the tuner on the ready-made printed-

string frequency	harmonic tuning	equal temp. tuning
f_{E2}	82.50 Hz	82.41 Hz
f_{A2}	110.00 Hz	110.00 Hz
f_{D1}	146.83 Hz	146.83 Hz
f_{G1}	195.56 Hz	196.00 Hz
f_{B1}	247.50 Hz	246.94 Hz
f_E	330.00 Hz	329.63 Hz

Q0 = 1	→ 1
Q1 = 2	→ 2
Q3 = 4	
Q4 = 8	
Q5 = 32	→ 32
Q6 = 64	
Q7 = 128	→ 128
Q8 = 256	→ 256
Q9 = 512	→ 512
Total	931

string	f_s	f_r	scale factor
E ₂	82.407 Hz	659.25 Hz	3727
A ₂	110.000 Hz	880.00 Hz	2792
D ₁	146.832 Hz	1174.65 Hz	2091
G ₁	195.998 Hz	1567.98 Hz	1566
B ₁	246.942 Hz	1975.83 Hz	1243
E	329.628 Hz	2637.02 Hz	931

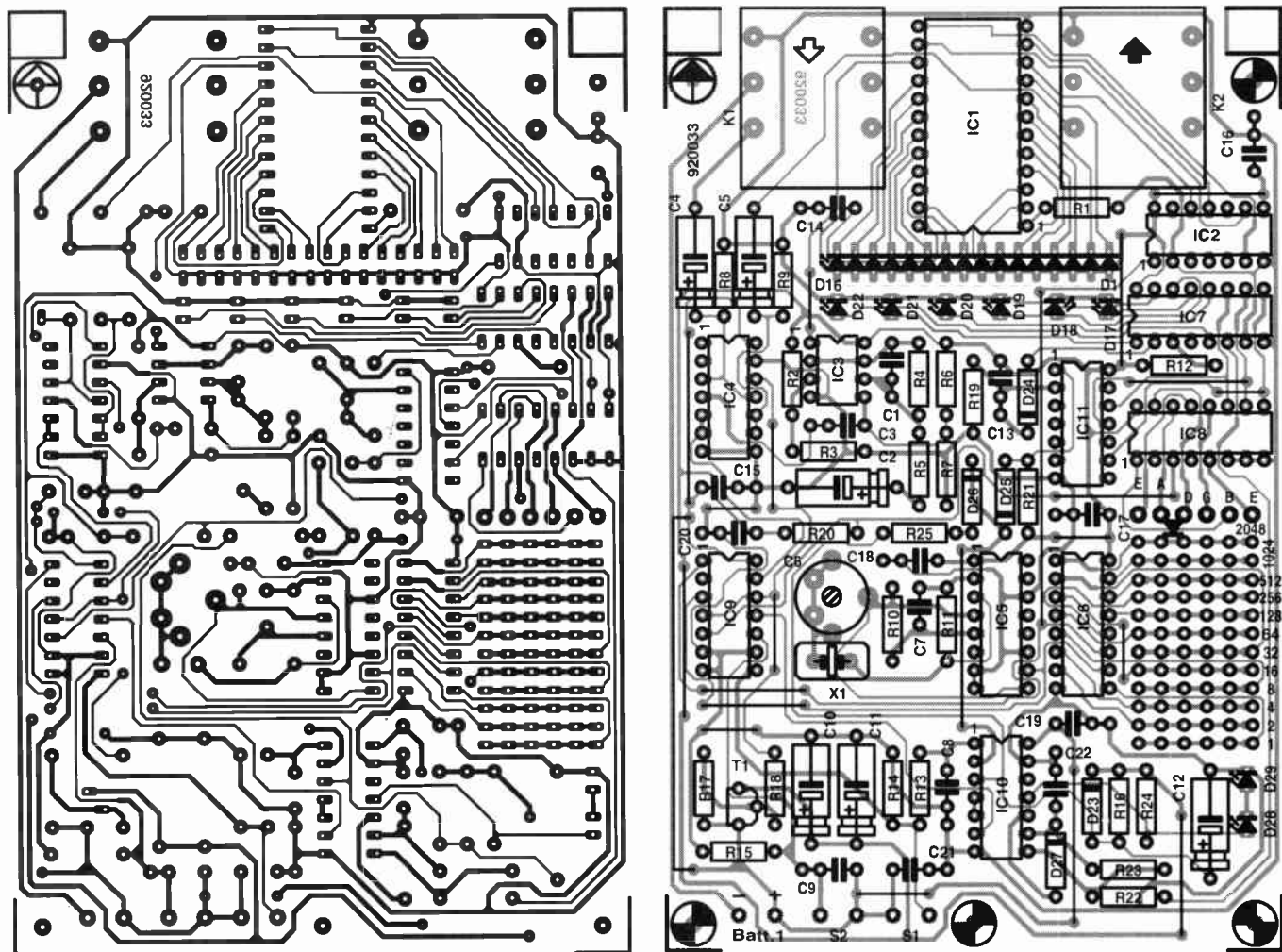


Fig. 2. Printed-circuit board for the guitar tuner.

circuitboard—see Fig. 2—should not present any problems. Mount the LEDs on the board without soldering, insert the board into the prepared enclosure and turn the enclosure over. The LEDs can then be correctly accommodated into previously drilled and squared (filed) holes in the front panel, after which they can be soldered on to the board.

A ready-made front panel foil is available—see Fig. 3.

Switches S_1 and S_2 can be linked to the board with normal circuit wire: because of the short length of these connections, screened cable was not found necessary.

The negative terminal of the battery must be connected to the contact on the stereo input socket to ensure that the tuner is switched on only when the cable from the guitar is inserted into the tuner. ■

It should be noted that this article assumes equal temperament tuning throughout. In this, each semitone is made an equal interval, which has the advantage that the instrument may be played in virtually any key. The disadvantage, however, is that the tones do not sound 'natural', which is why many guitarists prefer to tune their instruments to harmonics. (Ed).

PARTS LIST

Resistors:

R1 = 47 k Ω
 R2, R3, R17, R18, R21, R22, R24 = 10 k Ω
 R4, R8, R9, R19 = 1 M Ω
 R5 = 4.7 k Ω
 R6 = 820 k Ω
 R7 = 680 k Ω
 R10, R11 = 2.7 k Ω
 R12, R25 = 1.2 k Ω
 R13–R15 = 100 k Ω
 R16 = 3.3 M Ω
 R20 = 2.2 k Ω
 R23 = 5.6 M Ω

Capacitors:

C1 = 1 nF
 C2 = 1 μ F, 16 V
 C3, C8, C9, C13–C22 = 100 nF
 C4, C5, C12 = 10 μ F, 16 V
 C6 = 40 pF trimmer
 C7 = 33 pF
 C10, C11 = 4.7 μ F, 16 V

Miscellaneous:

D1–D16 = rectangular LED, green
 D17–D22, D28, D29 = rectangular LED, red

D23–D27 = 1N4148
 D30–Dxx = 1N4148 (for matrix—see text)
 T1 = BC327
 IC1 = 4067
 IC2, IC11 = 4024
 IC3 = TLC272
 IC4 = 4066
 IC5 = 4049
 IC6 = 4040
 IC7, IC8 = 4051
 IC9 = 4013
 IC10 = 40106

Miscellaneous:

S1, S2 = single-pole on-off switch, press to close
 K1 = 6.35 mm stereo audio socket with switch for PCB mounting
 K2 = 6.35 mm mono audio socket for PCB mounting
 Bt1 = PP3/6F22 (9 V)
 X1 = quartz crystal 2.4576 MHz
 Enclosure (for instance, Pactec Hp-9Vb) with battery compartment
 PCB 920033
 Front panel foil 920033F

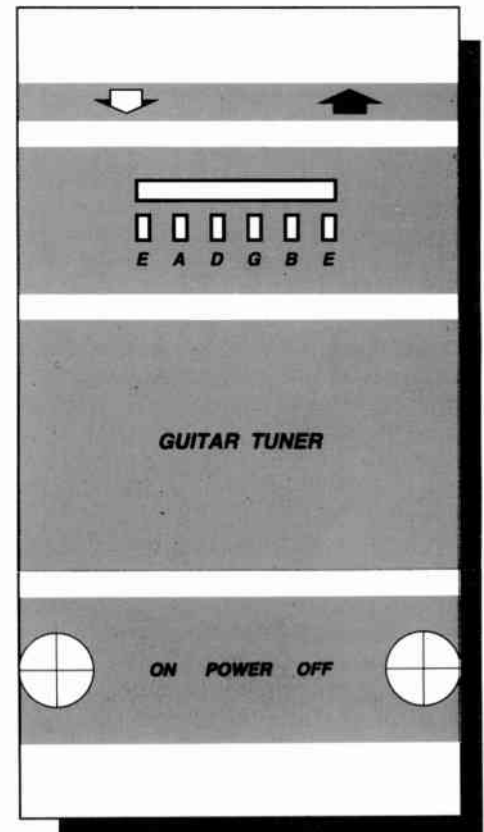


Fig. 3. Front panel foil.

DESIGN IDEAS

The contents of this column are based solely on information supplied by the author and do not imply practical experience by *Elektor Electronics*

PLANT WARMER

by Samuel Dick

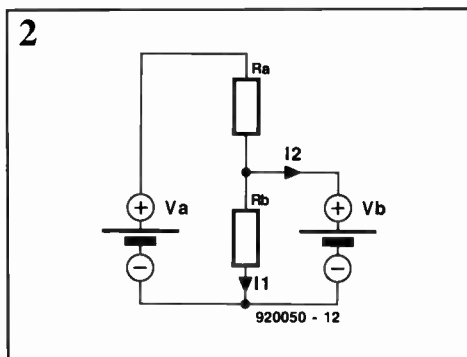
Frost is a gardener's nightmare. It is especially damaging in the late autumn when plants may not (yet) have been moved to their winter site or during the spring when growing conditions are normally favourable but a sudden, unexpected frost can kill many young plants.

THE classic solution to the problem of frost for small gardens is a coldframe. It occupies less space than a greenhouse, while still providing storage for many plants or seed trays. But during cold weather, the tempera-

ture in a coldframe may still drop below freezing and, during the spring, the temperature may not rise high enough to significantly boost the growth of seeds and young plants.

The 'plant warmer' offers a solution to these

problems. By placing a sensor and two heating elements in the coldframe, a simple heating system may be constructed. In this design, the two heating elements are controlled independently; one heater is set for a higher tem-



be calculated as follows—see Fig. 3. The voltage with R_{12} in circuit is $V_{o1} = V_s R_c / (R_a + R_b + R_c)$, where V_s is the supply voltage (12 V). With R_{12} (R_a in these equations) is shorted, the new output voltage, $V_{o2} = V_s R_c / (R_b + R_c)$. Note that $R_b + R_c = P_1$ in the circuit. Consequently,

$$R_{12} = P_1^2 \Delta V / (V_s R_c - \Delta V P_1),$$

where ΔV is the voltage increase required (say, 0.15 V corresponding to 15 °C higher than the frost protection set point). When the propagator mode is required, R_c is given by $V_{set} P_1 / V_s$.

Construction

The plant warmer was constructed on the printed-circuit board shown in Fig. 4 and fitted into a suitable box.

The two heating elements, R_5 and R_7 , may be made as follows. The lower-powered heater, R_7 , is made from thirty 1.0 Ω resistors, soldered together in series and then inserted into heatshrink sleeving for protection. The higher-powered heater, R_5 , is made from two resistor chains, identical to R_7 , connected in parallel. The values of the resistors and the number used have been calculated so that each resistor runs within its rated power dissipation. There is no need to shrink the sleeving after construction—indeed, this is undesir-

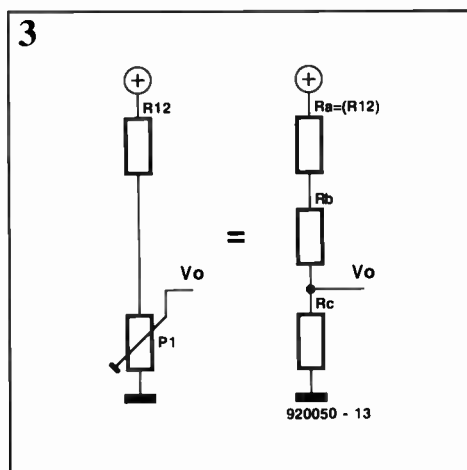
able since it makes the element less easy to bend, which could make fitting it to the cold-frame difficult.

As the heating elements and sensor have to operate in damp conditions, care should be taken to cover the connections with an epoxy potting compound to prevent ingress of dampness.

In use

The heating elements should be placed around the bottom of the coldframe and the sensor mounted near the bottom, too, but clear of either element. Some attention should be paid to the thermal insulation of the cold-frame. If at all possible, an insulating layer should be placed between the ground and the elements and plant pots. This prevents the heat from being absorbed by the ground. Similarly, insulation over the top of the cold-frame will help contain heat—the most suitable form of insulation is transparent plastic sheets of air-filled bubbles, like those used for packing delicate items.

The values of P_1 and P_2 should be set, with the heating off, with the aid of a digital multimeter to give voltages of 2.80 V and 2.76 V respectively. ■



PARTS LIST

Resistors:

(all resistors 250 mW)

- R1 = 8.2 k Ω
- R2, R3 = 33 k Ω
- R4 = 390 k Ω
- R5 = see text
- R6, R8 = 2.2 k Ω
- R7 = see text
- R9 = 2.7 k Ω
- R10, R11 = 6.8 k Ω
- R12 = 150 Ω
- P1, P2 = 5 k Ω preset, multiturn

Capacitors:

- C1 = 6.8 μ F, 63 V
- C2, C4, C5 = 100 μ F, 16 V
- C3 = 47 μ F, 25 V

Semiconductors:

- D1 = LM335Z (temperature sensor)
- D2 = BZY88C, 12 V, 500 mW zener
- D3 = 1N4002
- D4, D5, D6 = LED, green
- IC1 = LM319 (voltage comparator)
- N1 = mains voltage neon, green, with integral resistor

Miscellaneous:

- BR1 = 100 V, 6 A bridge rectifier
- T1 = 0–15 V, 2 A secondary mains transformer
- S1 = DPDT, 250 VAC, 2A
- S2 = SPST, low voltage
- Case, with feet
- Grommets (2)
- 4-core cable for heater wires
- Audio-quality coax cable for temperature sensor
- Heatshrink sleeving to cover R_5

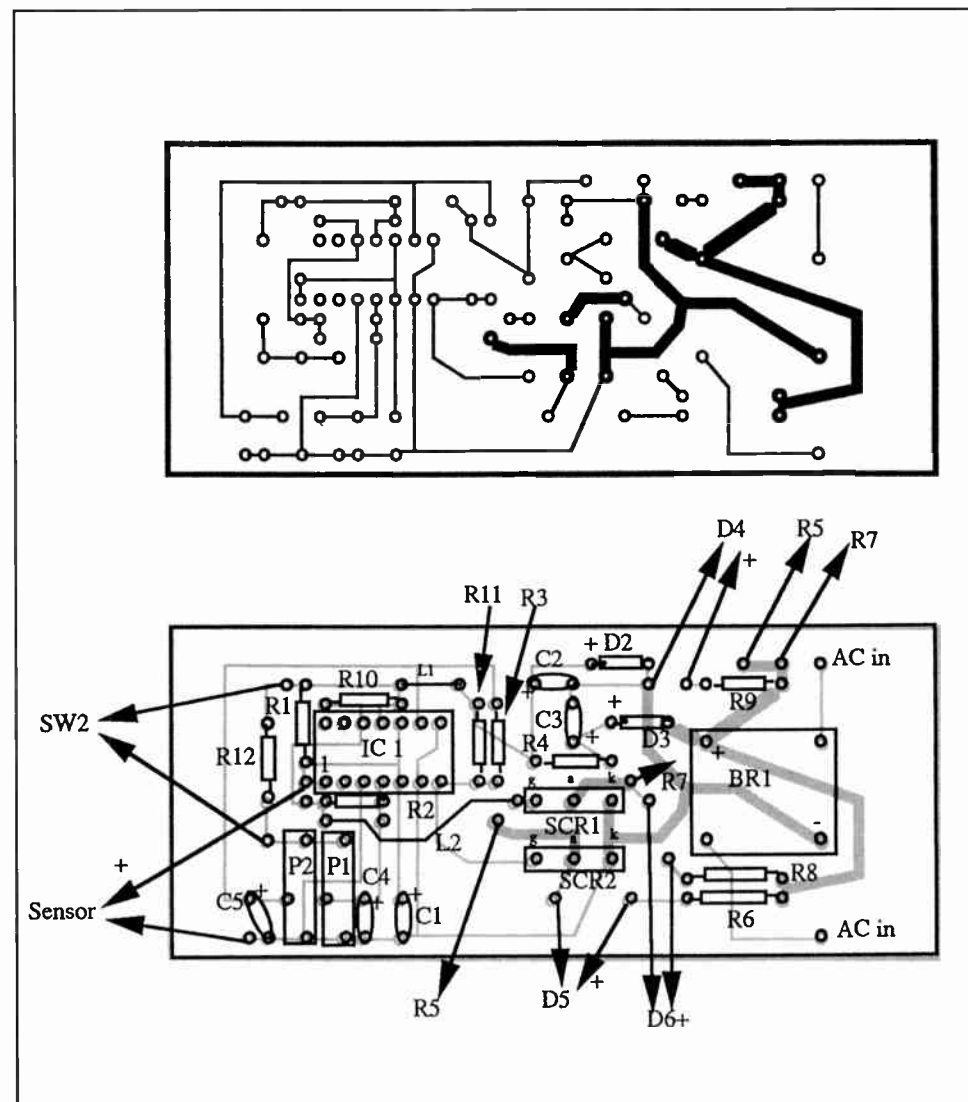


Fig. 4. Printed-circuit board for the plant warmer.

AUDIO-VIDEO PROCESSOR TYPE AVP300 – PART 2

An ELV design

Input circuits and chroma-VBS separation filter

THE circuit in Fig. 3 serves to select one of the inputs and to separate the chroma and VBS signals. Note that, in spite of the English-language front panel, some rear panels have the annotation 'FBAS' instead of CVBS. FBAS is the acronym of the German Farbbild Austast Synchronsignal = chroma, video, blanking,

synchronization signal.

The input signals may be divided into two groups: CVBS and S-VHS signals. In case of the former, the chroma and the VBS signals must be separated; with S-VHS signals that has already been done.

The CVBS signals are applied from the input selector circuit to two filters via S₂₀₁. Both these filters, L₂₀₃-C₂₂₇ and L₂₀₂-C₂₁₂, are tuned to the colour subcarrier. Filter L₂₀₃-C₂₂₇ is a band-stop filter that passes only the VBS sig-

nal to the output. The other filter passes only the subcarrier, and thus the colour signal, to the chroma output.

Filter L₂₀₃-C₂₂₇ operates in conjunction with four transistors, T₂₀₉-T₂₁₂, that share a common emitter resistance, R₂₆₀. The d.c. operating points of the transistors ensure that at any one time only one of them is switched on: the others are off. Which one is switched on depends on the selected input and the colour standard identified by the

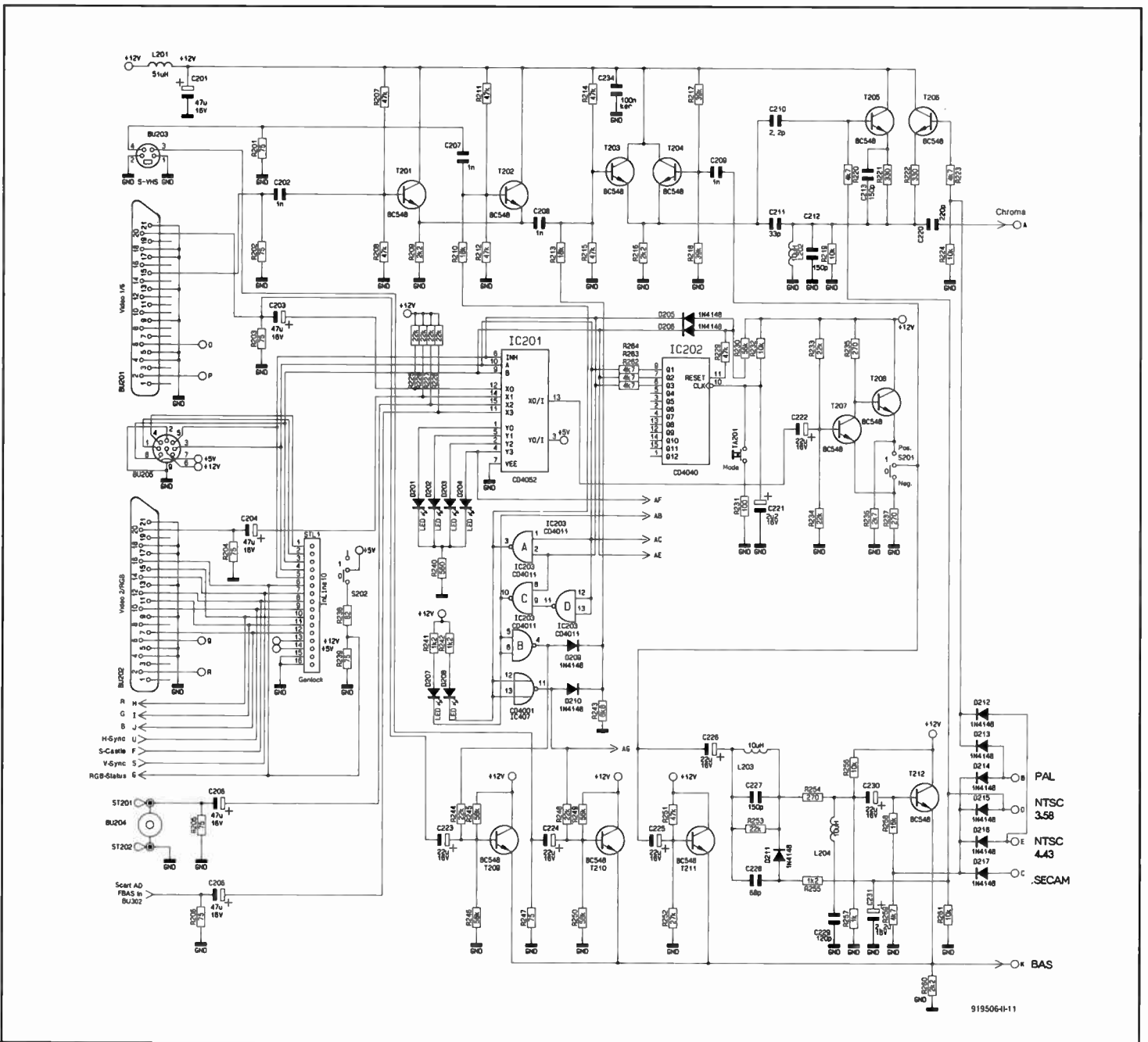


Fig. 3. Circuit diagram of the input stages and the chroma-VBS separation filter.

multi-standard decoder elsewhere in the processor.

Assuming that an input with a CVBS signal has been selected, a potential of about 2.5 V will be put on to the switching lines of the multi-standard decoder. Only T₂₁₁ is then switched on, resulting in the complete CVBS signal being applied to terminal K. This has the additional advantage that in case of a black-and-white signal (when the decoder cannot identify a colour standard) no filters are switched into circuit, which is beneficial to the picture quality.

If a colour standard has been identified, the potential on one of the switching lines, B-E, becomes 5.5-6 V. That voltage is used, via D₂₁₄-D₂₁₇, to set the d.c. operating point of T₂₁₂. The drop across R₂₆₀ then rises to a value that causes T₂₁₁ to switch off. The CVBS signal is then forced to pass through band-stop filter L₂₀₃-C₂₂₇ before it becomes available, via K, at T₂₁₂.

If the multi-standard decoder has also recognized that the signal is an NTSC signal with a 3.58 MHz subcarrier, diode D₂₁₁ is switched on. This causes C₂₂₈ to be connected in parallel with the band-stop filter so that the resonance frequency is shifted appropriately. Although the band-stop frequency for all other signals is 4.434 MHz, it should be noted that the SECAM subcarrier of 4.286 MHz is also suppressed adequately.

If no CVBS signal has been selected, the control logic ensures that T₂₀₉ and T₂₁₀ are switched on. The VBS signal of one of the S-VHS inputs is then passed directly to terminal K. At the same time, the drop across R₂₆₀ ensures that both T₂₁₁ and T₂₁₂ are switched off.

The circuit associated with the chroma filter operates in a manner similar to that of the VBS band-stop filter. Here, the common emitter resistance of transistors T₂₀₃-T₂₀₆ is R₂₁₆. The resonant frequency and Q of the



filter are chosen for the SECAM signal (4.286 MHz). To enable the filter to handle the greater bandwidth of PAL and NTSC 4.434 MHz signals, it is shunted by R₂₂₂ via T₂₀₆ and decoupling capacitor C₂₃₄. The Q of the network will then drop, while the bandwidth increases. The small difference with the required bandwidth is negligible, so that the filter does not need retuning. To enable the filter to handle NTSC 3.58 MHz signals, it is shunted by capacitor C₂₁₃ via T₂₀₅, while at

the same time the bandwidth is increased because the Q factor is lowered by R₂₂₁.

The chroma filter selects between CVBS and S-VHS signals with the aid of T₂₀₃. In contrast to the VBS band-stop filter, the chroma filter is always in circuit. This does not affect the quality of the output signal.

When T₂₀₃ is switched on (by its base voltage), one of the two S-VHS signals is passed to the chroma output, depending on the base potential of T₂₀₂. When that transistor is on, T₂₀₁ is off and the VBS signal at input Video 5 is passed. When T₂₀₁ is on and T₂₀₂ is off, the signal at Video 1/6 is selected.

The switching of input signals is effected by IC₂₀₁-IC₂₀₃. Video signals (audio signals will be reverted to later) are present at one of the four input connectors. The standard value of their signal strength is 1 V_{pp}. All inputs are terminated into a 75 Ω resistor, R₂₀₃-R₂₀₆. The signals are passed to analogue multiplexer IC₂₀₁ (2x4 positions) via coupling capacitors C₂₀₃-C₂₀₆. The multiplexer selects one of the signals, which is indicated by the associated LEDs.

The control signals for the multiplexer are provided by counter IC₂₀₂, which is operated by switch TA₃₀₁.

The selected signal is applied to buffer/inverter T₂₀₇-T₂₀₈. The processor may be set for positively or negatively modulated signals by switch S₂₀₁. From that switch, the signal is split into two: one part to the chroma filter and the other to the VBS band-stop filter.

Since SCART connector BU₂₀₁ also serves as an S-VHS input, the signal at pin 20 is passed not only to the multiplexer, but also directly to the VBS band-stop filter.

S-VHS signals are not switched by the multiplexer, but by transistor stages in the filter sections: T₂₀₁-T₂₀₂ and T₂₀₉-T₂₁₀. The necessary switching signals are derived from the state of counter IC₂₀₂ by IC₂₀₃.

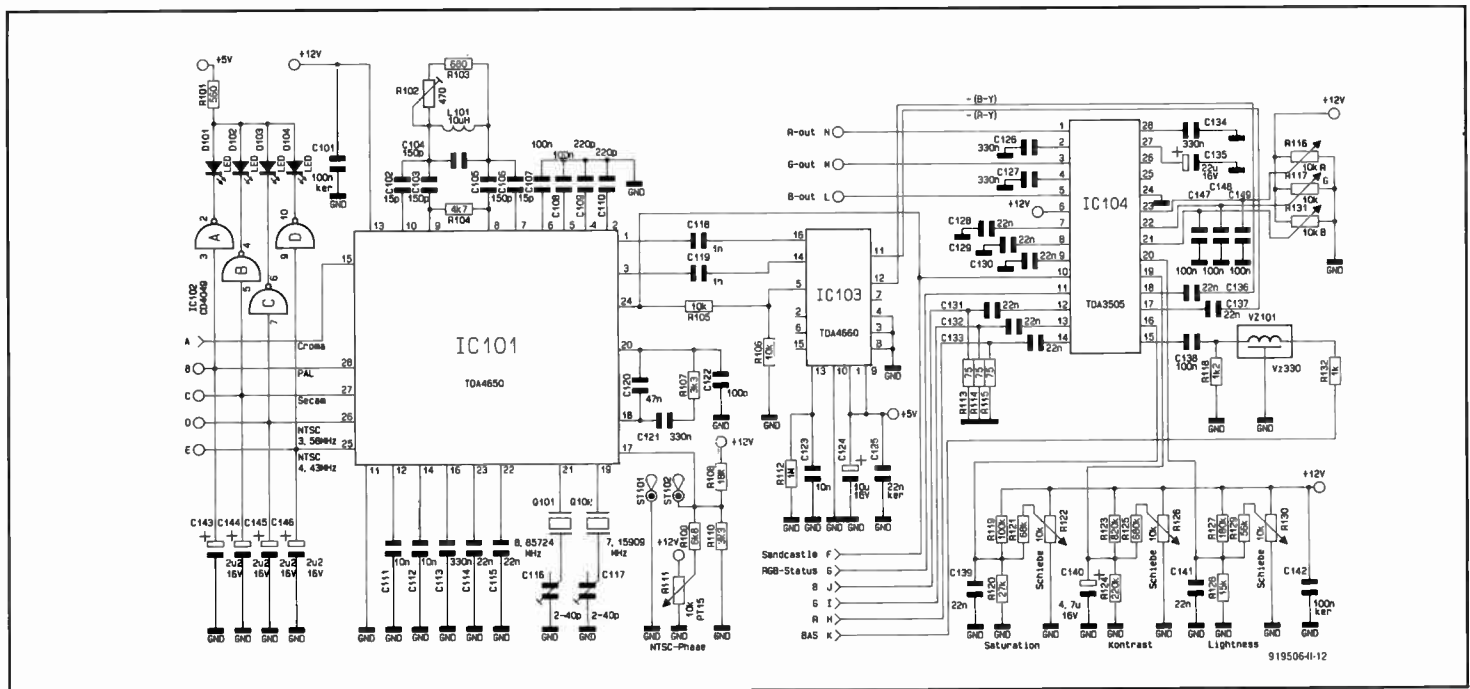


Fig. 4. Circuit diagram of the multi-standard decoder and the video colour controller.

Multi-standard decoder and video colour controller

The circuit of the multi-standard decoder and video colour controller, shown in Fig. 4, carries out the decoding and processing of all video signals.

The actual decoding is effected by IC₁₀₁. The standard of the incoming signal is determined by IC₁₀₁ on the basis of the chroma signal at pin 15. The chroma filter is set up (wide band) to enable any chroma signal to be passed correctly. The standard is translated into appropriate voltage levels at input/output pins 25–28. Four levels are recognized: 0.5 V—standard out; 2.5 V—search mode; 6 V—standard on; 9 V—forced acceptance of a standard.

Although the multi-standard decoder is a fairly complex circuit, it has only three calibration points, which, by the way, have nothing to do with the internal of the IC, but are merely intended for adjusting some external components. These are (1) the SECAM reference circuit, L₁₀₁–C₁₀₄, (2) Q₁₀₁ and (3) Q₁₀₂.

Because NTSC signals lack a colour burst,

there is no reference for the chroma signals. R₁₁₁ is provided to make sure that the reference of the decoder is, nevertheless, the same as that of the transmitter. Maladjustment of this potentiometer results in unnatural colouring of the picture.

The output of IC₁₀₁ consists of two colour difference-signals that are applied to delay line IC₁₀₃. The output of this line is also two colour-difference signals but with corrected transit times. These signals are then ready for the final stage in the decoding and for being processed into a picture signal. Those tasks are performed by IC₁₀₄, the video colour controller.

In addition to the colour-difference signals, the inputs to IC₁₀₄ consist of the VBS signal that is provided via delay line VZ₁₀₁, or the RGB signals that are input via Video 2 and terminals H–J.

Circuit IC₁₀₄ synthesizes the colour-difference and VBS signals to an RGB signal. This synthesis may be affected by the setting of R₁₁₁ (colour saturation control). Apart from its white-point adjustment, the RGB signal can be modified in respect of brightness and contrast. The final RGB signal is applied to the

PAL/NTSC encoder via pins 1, 3 and 5.

PAL/NTSC encoder

The diagram of the circuit that reconverts the RGB signal into a CVBS signal, PAL or NTSC standard, is shown in Fig. 5. Apart from the RGB signal, the Type TPE1378A encoder, IC₃₀₁, requires a number of other signals. The first of these is the synchronization signal at pin 15, which is provided by the synchronization circuit to be discussed in Part 3 of this article.

Generation of the colour subcarrier requires a generator: since NTSC 4.43 MHz as well as NTSC 3.56 MHz signals can be handled, two generators are needed. When either of these is energized, the relevant band-pass filter, BPF₃₀₁ or BPF₃₀₂, is also actuated. To compensate for the delay of the chroma signal in the filter, the VBS signal is also delayed: in VZ₃₀₁.

The RGB input signal is also available as a buffered output of IC₃₀₁. The RGB lines are connected to the relevant pins of connector BU₃₀₂ (Video 4 output) via coupling capacitors and terminating resistors. A voltage can be applied to this connector by S₃₀₁ to force the equipment connected to the processor to use the RGB signals instead of the CVBS signal on pin 19 as input.

The CVBS signal is available at pin 5 of IC₃₀₁. It is applied to S₃₀₄ via a coupling capacitor and a terminating resistor, and to electronic switch IC₃₀₂. That switch ensures that, if Video 4 is used as input and as output, for instance, during format conversion, the CVBS signal is replaced by a composite sync (BS or Blanking/Synchronization) signal. This arrangement prevents the arising of noise and interference between the colour subcarriers of the input and output signals in the connecting cable. This means, of course, that in the final analysis only the RGB signal can be used as an output signal.

The remaining signals provided by IC₃₀₁ are the VBS and chroma signals for the S-VHS outputs. These signals are applied to the relevant connectors, BU₃₀₁ and BU₃₀₃, via a buffer stage. To ensure that the terminating impedance of the VBS or chroma signal is correct, connectors BU₃₀₁ and BU₃₀₃ must not be used simultaneously, unless S₃₀₄ is in position CVBS and no S-VHS equipment is connected to BU₃₀₁.

The instalment in the July issue will describe the audio, power supply and synchronization circuits, while that in the September issue will deal with the construction and setting up.

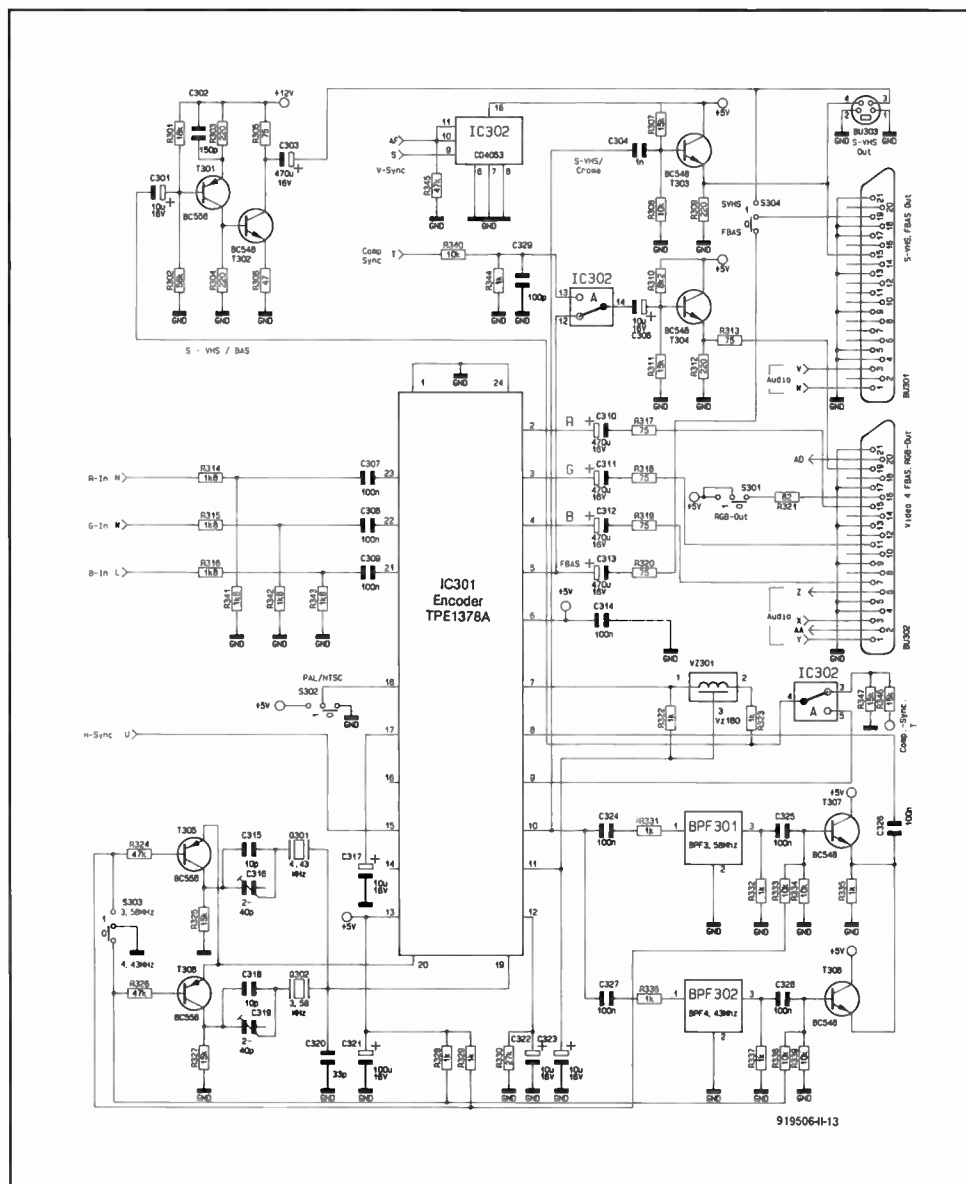
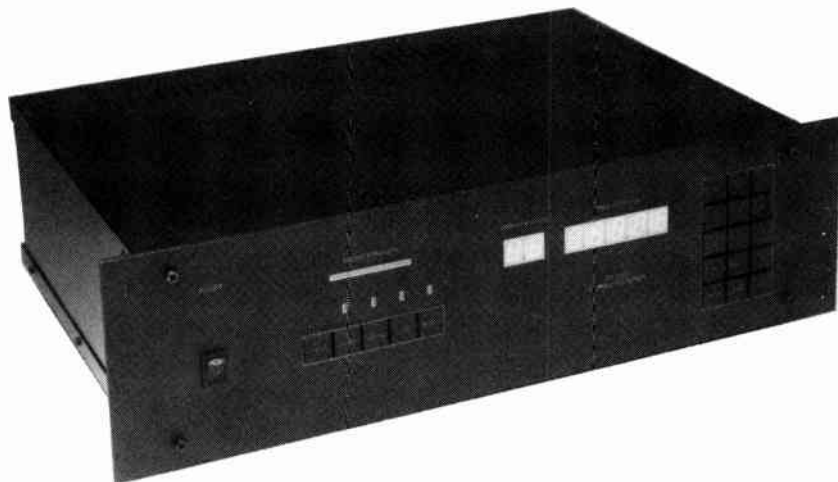


Fig. 5. Circuit diagram of the PAL/NTSC encoder

FM TUNER

PART 4: KEYBOARD, DISPLAY AND MODE CONTROL



In this instalment we deal with the construction of the synthesizer board, and the operation of the combined keyboard/display/controls unit.

Design by H. Reelsen

The introductory photograph shows the completed FM tuner in a 19-inch rack style enclosure, which follows the line of other high-end audio equipment published over the past year or so in this magazine. Inside the enclosure are six printed circuit boards:

1. Main tuner board (PCB no. 920005) which combines all RF and audio electronics; described in *Elektor Electronics USA*, March 1992, Part 1.
2. Power supply (PCB no. 920005-2) described in *Elektor Electronics USA*, April and May 1992, Parts 2 and 3.
3. Mode control board (PCB no. 920005-3) described in this installment, Part 4.
4. Keyboard and display board (PCB no. 920005-4) also described in this installment, Part 4.
5. Synthesizer (920005-5; circuit diagram described in *Elektor Electronics USA*, May 1992, Part 3.
6. Field strength indicator (PCB no. 920005-6), to be described in July/August 1992, Part 5, together with the construction of the keyboard/display unit, and, possibly, details on wiring.

Audio mode and mono/stereo control unit

While the large keyboard and display keyboard control and indicate all synthesizer functions, a smaller board, described here, arranges the audio mode switching of the main tuner board. The circuit shown in Fig. 12 operates independently of the microprocessor on the synthesizer board, so that it

is also useful if the synthesizer is omitted, and 'replaced' by manual tuning (by a precision multiturn potentiometer). The printed circuit board for the mode control unit (Fig. 13) is designed such that it can be fitted at the inside of the receiver's front panel. The PCB accommodates five push-buttons, of which four have a built-in LED. Starting at the left, the first three keys are used to select different modes of the TDA3810 audio IC, while the remaining two serve to control the mono/stereo switching of the TDA1578 stereo decoder IC. Both the TDA3810 and the TDA1578 are located on the main tuner board.

The function of the push-buttons is as follows (left to right):

- S203: NORMAL audio mode (audio processor TDA3810).
- S204: WIDE audio mode (audio processor TDA3810). The stereo image is widened, and LED D203 lights.

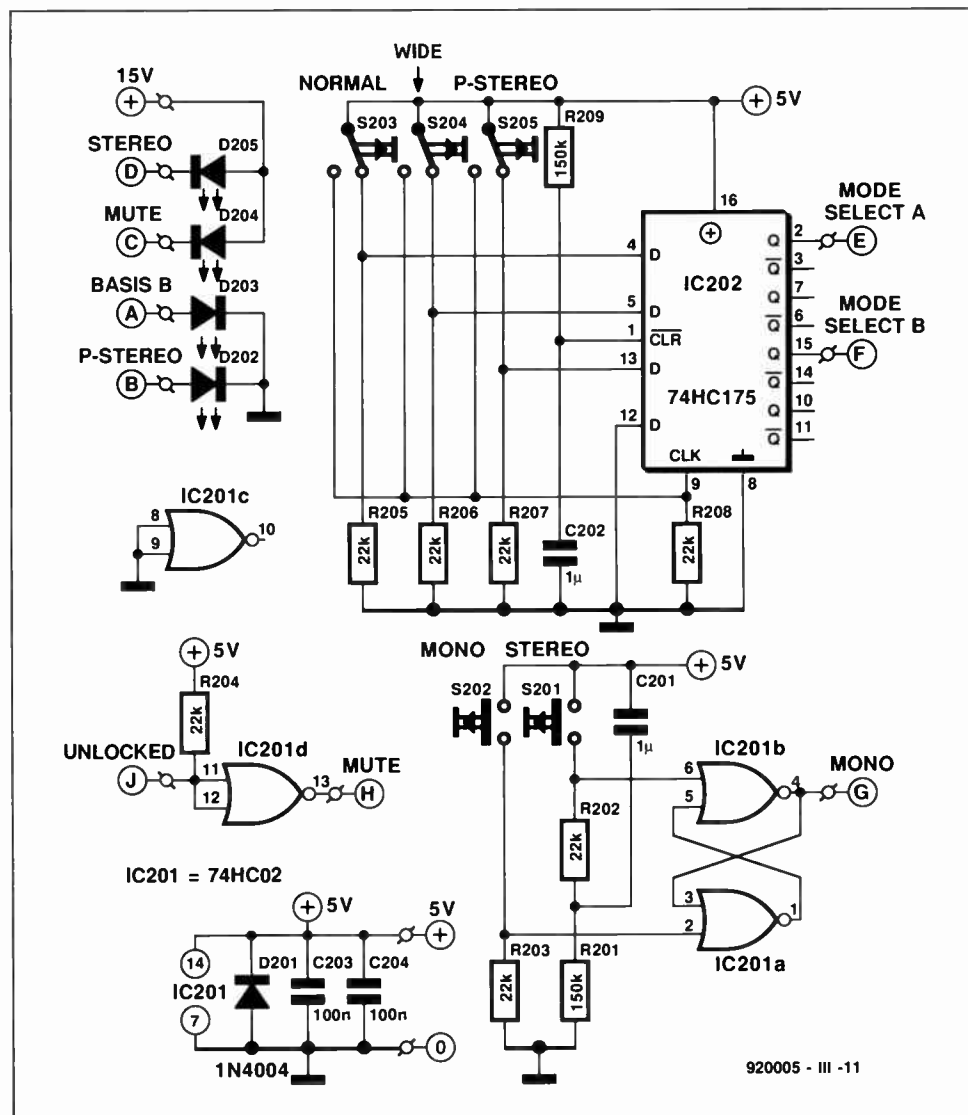


Fig. 12. Circuit diagram of the audio mode and mono/stereo control unit.

COMPONENTS LIST

AUDIO MODE CONTROL BOARD

Resistors:

2	150k Ω	R201;R209
7	22k Ω	R202-R208

Capacitors:

2	1 μ F solid MKT	C201;C202
2	100nF	C203;C204

Semiconductors:

1	1N4004	D201
4	green LED, rectangular	D202-D205
1	74HC02	IC201
1	74HC175	IC202

Miscellaneous:

5	Digitast push-button with 12.3-mm wide cap	S201-S205
1	Printed circuit board	920005-3

- S205: PSEUDO STEREO mode (audio processor TDA3810). This effect can be switched on with the stereo decoder in mono as well as stereo mode. When selected, LED D202 lights.
- S201: STEREO mode (stereo decoder TDA1578).
- S202: MONO mode (stereo decoder TDA1578). Mono/stereo mode is indicated by LED D205.

Since push-buttons are used to select the different modes, bistables are required to set the logic levels of the control lines to the main tuner board. The mono/stereo selection requires only one bistable, which consists of NOR gates IC201a and IC201b. When the 'stereo' key, S201, is pressed, the bistable output (terminal 'G' of the board) goes to 0 V. Terminal 'G' is connected to terminal 'MONO' on the main tuner board. When a stereo broadcast is received, the 'stereo' indicator, LED D205, lights. Terminal 'D' is connected to the terminal marked 'STEREO LED' on the main tuner board. When the 'mono' key is pressed, the bistable is reset, and terminal 'G' goes to +5 V. This causes the stereo decoder to switch to mono, and the 'stereo' LED to go out. Components C201-R201 form a power-up network that sets the bistable at power-on. This means that 'stereo' reception is selected automatically when the receiver is switched on.

The switching between the three audio modes offered by the TDA3810 works in a manner similar to that of the TDA1578 described above. Three of the four D-type bistables contained in the 74HC175 package are used. The three bistable inputs are connected to ground via 22-k Ω resistors. Push buttons S203, S204 and S205 at these inputs have toggle (change-over) contacts. They are normally closed (as indicated by the circuit symbol), so that the bistable inputs are held at +5 V. When one of these push-buttons is pressed, its contact switches to the other position, so that the corresponding bistable

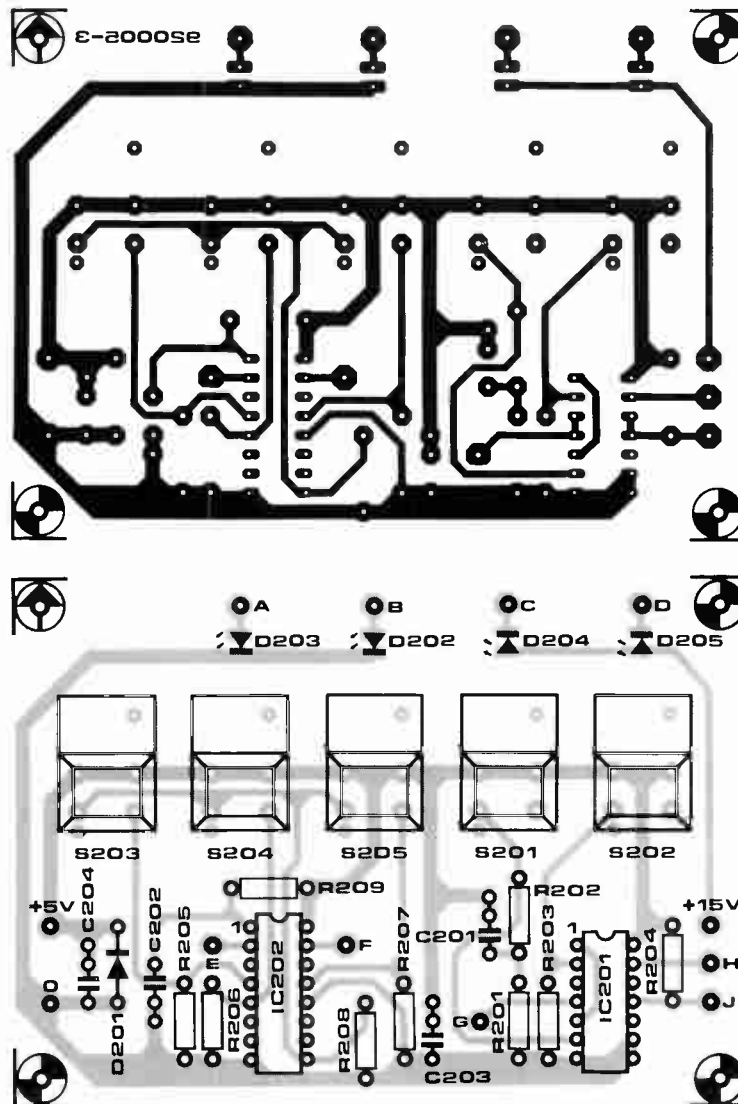
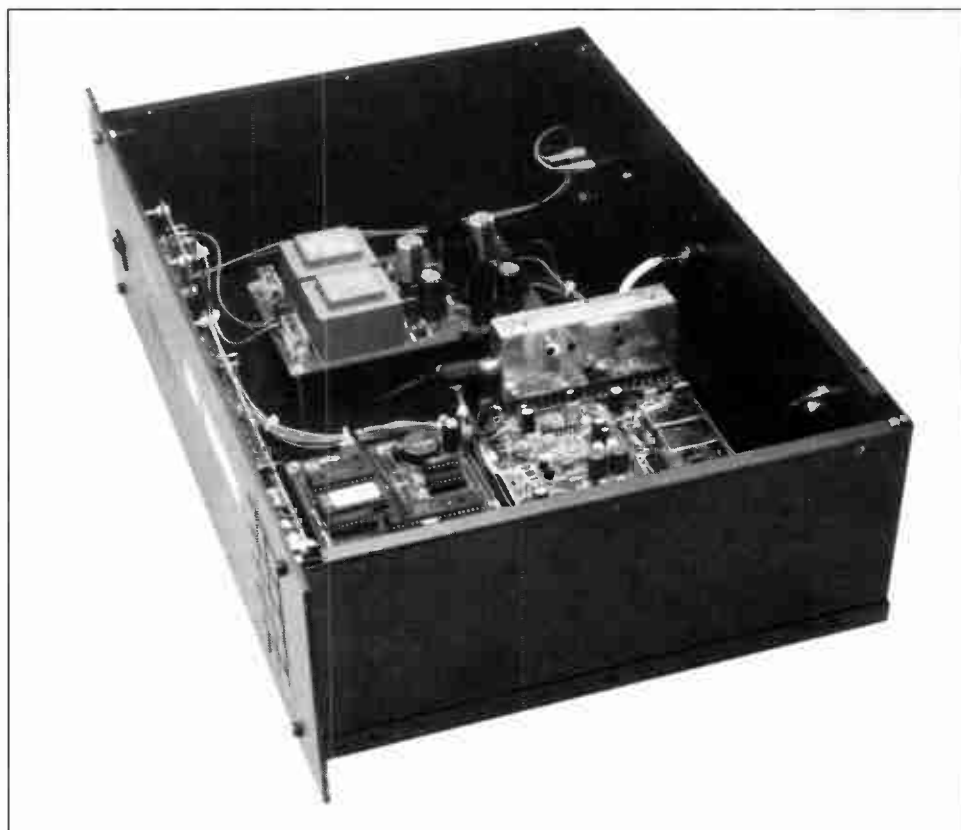


Fig. 13. Artwork for the audio mode and mono/stereo control board.



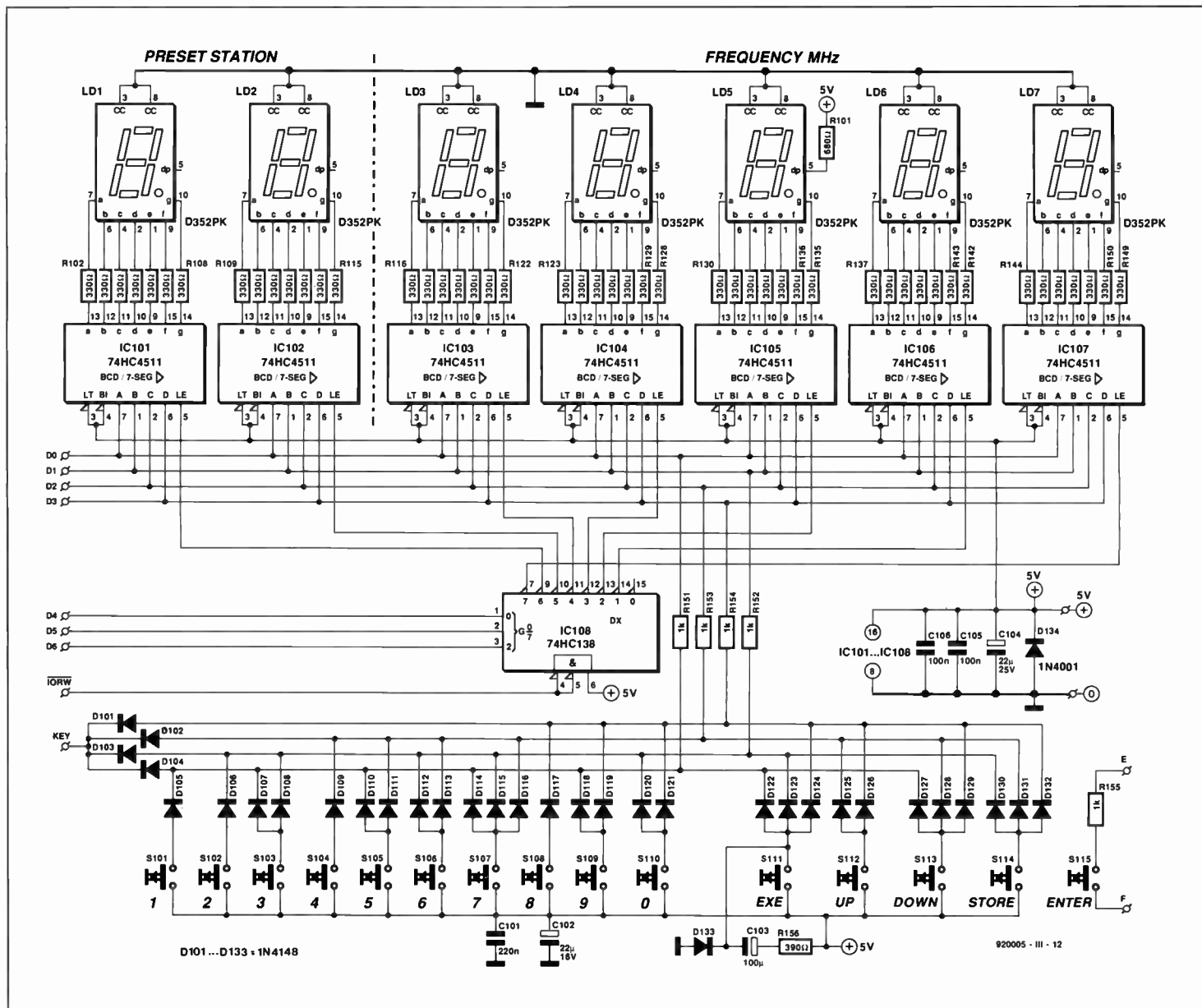


Fig. 14. Circuit diagram of the keyboard/display unit.

input goes low. At the same time, the level at the clock input (pin 9) changes from low to high. When this positive transition occurs, the logic level at the D (data) input of the bistable is transferred to the Q output, where it remains stable until the next positive edge at the clock input. This basic operation results in the following switching behaviour:

- When the 'NORMAL' key (S203) is pressed, the output of the first bistable (terminal 'E') goes low, and that of the third bistable (terminal 'F'), high.
- When the 'WIDE' key (S204) is pressed, both 'E' and 'F' go logic high.
- When the 'PSEUDO' key (S205) is pressed, 'E' goes high, and 'F' low.

The two outputs 'E' and 'F' are connected to the MODE SELECT A and MODE SELECT B terminals on the main board, where the logic levels result in the following modes:

Mode	A	B
Stereo	L	x
Wide image	H	H
Pseudo stereo	H	L

The associated indicators, LEDs D202 and D203, are driven by the main board. The connections are as follows: terminal 'A' goes to 'BASIS B LED' on the tuner board, and terminal 'B' to 'P-STEREO' on the tuner board.

The UNLOCKED (out of lock) signal supplied by the synthesizer requires to be inverted before it can be used. This is achieved with gate IC201D, whose output is fed to the 'MUTE' input of the tuner board via terminal 'H'. The mute indication is also driven by circuitry on the main board: the 'MUTE LED' output (at R46) is connected to terminal 'C' (at D204) on the small controls board.

Keyboard and display

The circuit diagram of the keyboard/display unit is given in Fig. 14. This unit is constructed on a separate printed circuit board which is also fitted at the inside of the receiver's front panel. Cut clearances in the front panel to enable the keys and the LED displays to protrude. The keyboard consists of 15 push-buttons of the 'Digitast' (ITT-Schadow) type with 12.3-mm wide caps, like the ones used on the smaller controls board.

The readout consists of seven 7-segment LED displays.

Only a single 8-bit bidirectional port is required to drive the displays and read the keys. However, this port must be capable of sinking as well as sourcing a current of 5 mA per line. This requirement is met by IC405 on the synthesizer board. The outputs of IC405 are connected to inputs D0 to D6 on the display board.

Datalines D0 to D3 are connected to all inputs of display drivers IC1 to IC7, which are Type 4511 7-segment LED display latches/decoders/drivers. A 'low' level at the LE (latch enable) input of a 4511 clocks the data into the display decoder. Address decoder IC8 determines which display driver accepts the data. The selection is made with the aid of the logic levels on the D4, D5 and D6 lines that exist when IORW is actuated. This forms the strobe signal that indicates that the data on D0-D6 are stable and valid.

The keyboard is encoded with the aid of diodes, which also serve as straight connections. This method is traditional as well as economic, since it enables the use of a single-

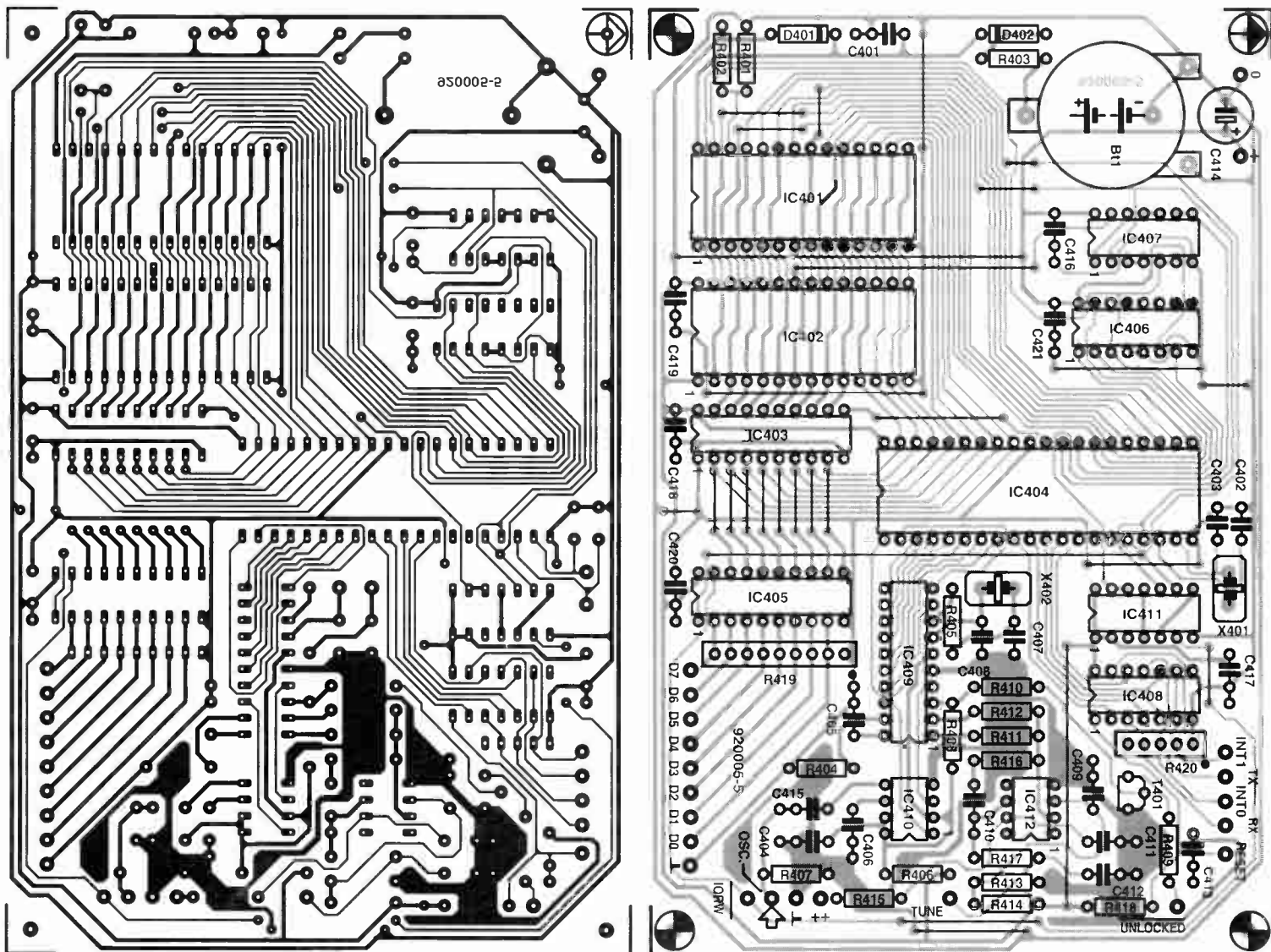


Fig. 15. Track layout (mirror image) and component mounting plan of the synthesizer board.

COMPONENTS LIST

SYNTHESIZER BOARD

Resistors:

- 3 1kΩ R401;R403;R405
- 3 2kΩ R402;R413;R414
- 1 33kΩ R404
- 2 56Ω R406;R415
- 1 68Ω R407
- 2 10kΩ R408;R416
- 1 270Ω R409
- 1 2kΩ R410
- 1 237kΩ 1% R411
- 1 18kΩ R412
- 1 4kΩ R417
- 1 1MΩ R418
- 1 8-way 10kΩ SIL array R419
- 1 4-way 2kΩ SIL array R420

Capacitors:

- 1 220nF C401

- 2 33pF
- 3 1μF solid MKT
- 1 1nF
- 3 4nF7
- 2 56pF
- 1 33nF
- 1 100μF 25V radial
- 6 100nF

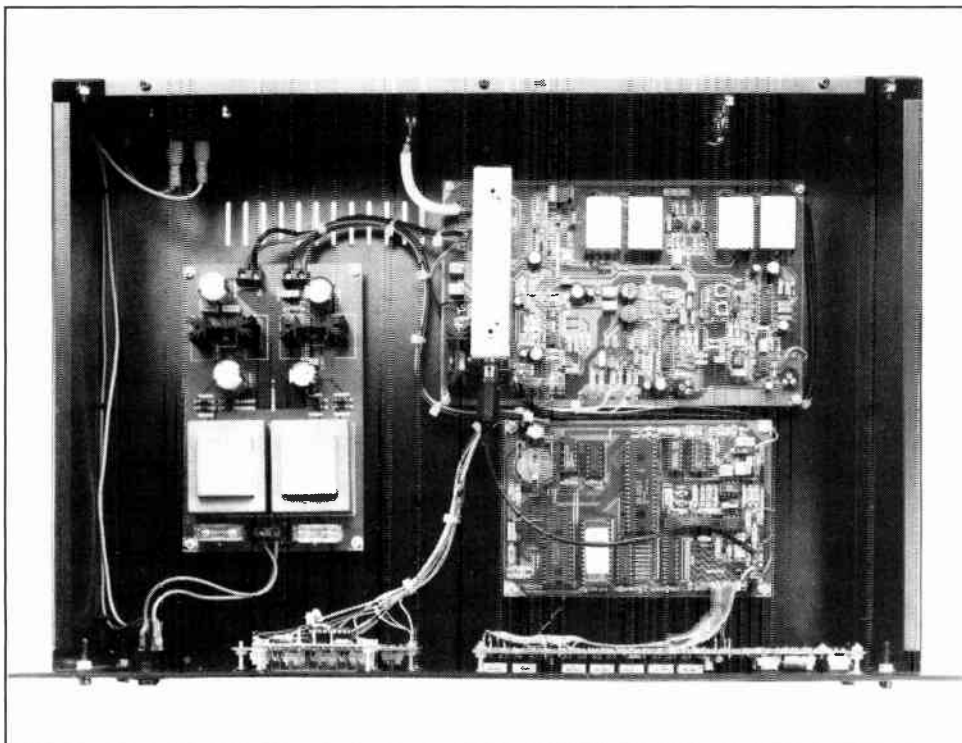
Semiconductors:

- 2 1N4148
- 1 BC547B
- 1 6264LP-15 RAM
- 1 27C256 (ESS6101) EPROM
- 1 74HC573
- 1 80C32
- 1 74HC245
- 1 74HC138

- C402;C403 1 74HC02 IC407
- C404;C409;C411 1 74HC04 IC408
- C405 1 NJ8821 (GEC-Plessey) IC409
- C406;C412;C415 1 SP8795 (GEC-Plessey) IC410
- C407;C408 1 74HC00 IC411
- C410 1 TL081 IC412
- C413
- C414
- C416-C421
- D401;D402 1 Lithium battery CR2032 with PCB-mount holder Bt1
- T401 1 Quartz crystal 2MHz X402
- IC401 1 Quartz crystal 16MHz X401
- IC402 1 Printed circuit board 920005-5
- IC403
- IC404
- IC405
- IC406

Miscellaneous:

- 1 Lithium battery CR2032 with PCB-mount holder Bt1
- 1 Quartz crystal 2MHz X402
- 1 Quartz crystal 16MHz X401
- 1 Printed circuit board 920005-5



sided PCB.

Pressing a key on the tuning keyboard causes a high level on one or more datalines, but only when the driver on the synthesizer board is switched to 'receive'. When this is so, the key code is applied to IC405 via R51-R54 and datalines D0-D3. When it happens that a key is pressed while the driver 'transmits', no bus conflict occurs because the driver 'overcomes' the keyboard lines with their 1-k Ω resistors. Resistors R51-R54 then function as pull-ups only.

Push-button S115, which is connected to the 'F' and 'E' terminals via 1-k Ω resistors, has a special function. We are talking about the reset key. When S115 is pressed, the reset input line of the synthesizer tuning system is pulled to ground. As described last month, the synthesizer is switched off during normal operation of the receiver. The push-button that causes the reset action is labelled 'ENTER' because it restarts the microcontroller, and needs to be pressed before every new entry.

A further novelty of the circuit is the 'EXECUTE' key, S111, which is used to terminate entries. The parallel R-C network R156-C103 ensures that an 'execute' key action is simulated at power on.

The tuning functions

The upper part of the keyboard has the number keys 0 to 9 to enter frequencies and station presets. The receive frequency is shown on the five LED displays to the right of the readout, while the first two digits show the preset number. This means that a total of 99 presets is available.

In addition to the 9 numerical keys there are 5 function keys:

- ENTER to start every entry;
- STORE to store a frequency entered or displayed;

- EXECUTE to close off any entry (except when STORE is used);
- UP to increase the tuning frequency;
- DOWN to decrease the tuning frequency in steps of 50 kHz.

The operation of the keyboard is simplicity itself. When power is applied, the receiver is automatically tuned to the station it was last tuned to, and the display shows the station frequency. The following keys have to be pressed to select another station from the memory:

ENTER — Station number (1-99) — EXECUTE

Alternatively, you may want to enter the station frequency, e.g. 98.50 MHz:

ENTER — 9850 — EXECUTE

When it is desired to store the displayed frequency as preset (station number) 15, press

ENTER — 15 — STORE

To tune the receiver up or down press
ENTER — UP

or

ENTER — DOWN

The frequency changes as long as you hold the UP or DOWN key pressed. When the key is released, the frequency remains static for about 3 seconds, after which the microcontroller switches itself off. In the other entry modes, the microcontroller is switched off when the 'EXECUTE' or 'STORE' key is pressed, and 'woken up' again when the 'ENTER' key is pressed.

The lithium battery on the synthesizer board ensures that stored frequencies and station preset numbers remain intact for at least ten years. All entry errors, for instance, an out-of-band frequency (lower than 87.50 or higher than 108.00), are signalled by the display clearing to all zeroes, and flashing five times. After this error indication, you can attempt a new entry.

The frequency raster is 50 kHz in direct frequency entry mode. This means that the last digit can only be '0' or '5'. When another value is entered, the tuning program automatically rounds it to the nearest raster value.

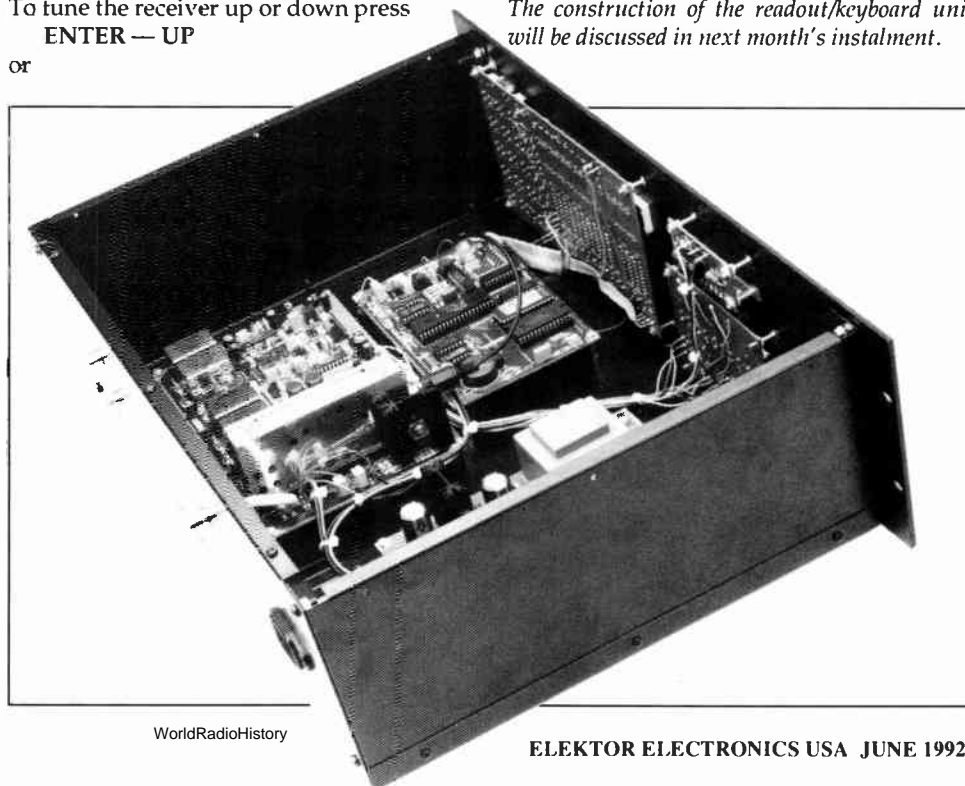
Synthesizer board

Although the synthesizer is a fairly complex circuit, its construction is entirely straightforward. Start your work by fitting the 27 wire links on the board (see the component overlay in Fig. 15). The rest of the work is mostly positioning components, and bending, soldering and cutting component wires. It is recommended to use sockets for all ICs.

Finally, note a small error in the circuit diagram of the synthesizer (Fig. 11): the 4.7-nF capacitor at the OSC input should be labelled C415, not C407.

A further error has been made with electrolytic capacitor C70 on the main tuner board: C70 is shown with the wrong polarity both in the circuit diagram, Fig. 4, and on the component overlay of the tuner board (also Fig. 5b).

The construction of the readout/keyboard unit will be discussed in next month's instalment.



MAX660 INVERTER/DOUBLER

Design by J. Ruiters

A small circuit is described that inverts a positive voltage into a negative one or doubles its level. It does not use inductors and is based on a single Type MAX660 chip.

THE power supply for a battery-operated design can often cause a few headaches as regards the level of the voltage or whether a symmetrical supply should be used. The latter, for instance, normally means a doubling of the number of batteries, which take twice the space originally allowed for and increase the weight: two undesirable factors. The obvious solution is a switch-mode supply, but the construction and/or dimensions of the in-

ductor required for that is another unwelcome element.

There is, however, another solution, provided the output current is not required to be larger than 100 mA: the Type MAX660 integrated circuit. This IC needs only a few capacitors and a diode to provide, from a positive supply, a negative voltage at the same level or double the voltage. It is, of course, possible to use a number of these ICs to increase

the output current or voltage, but the proposed design is based on just one.

The circuit

The internal of the MAX660 circuit is shown in Fig. 1; Fig. 1a is a design for a voltage inverter and Fig. 1b, for a voltage doubler. Within the IC, one of two pairs of CMOS switches is opened or closed by the internal

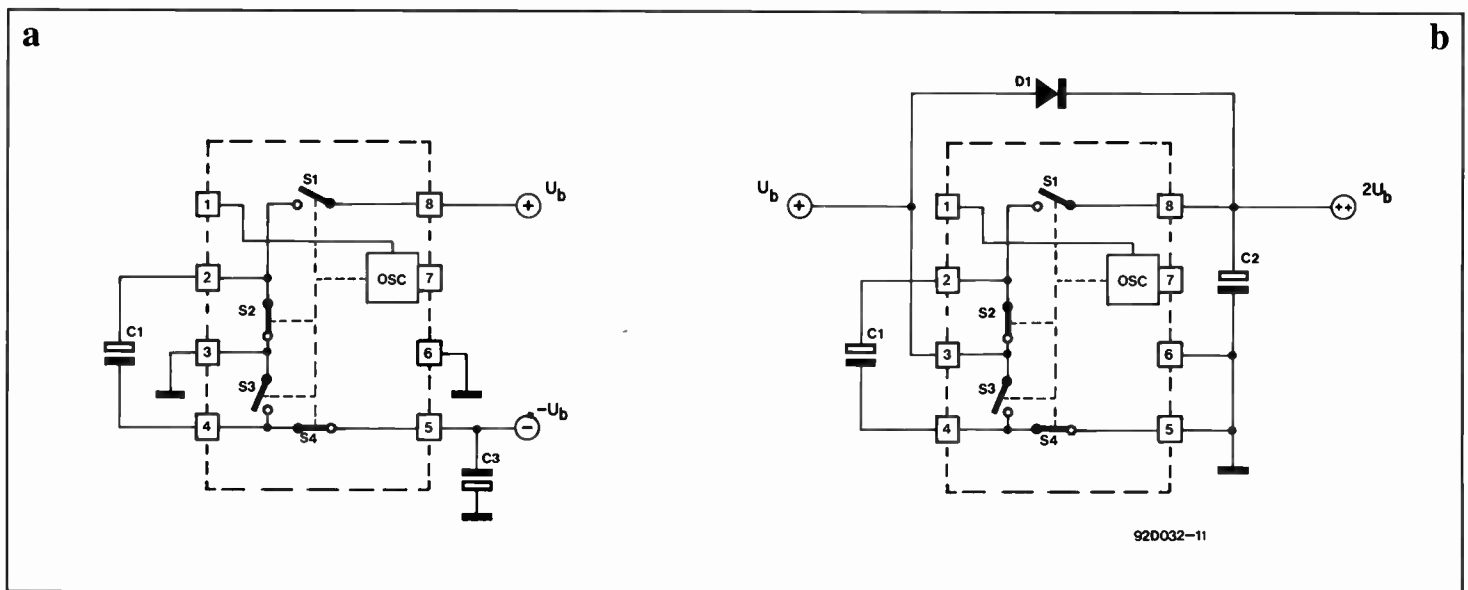


Fig. 1. Basic circuit of a voltage inverter (a) and a voltage doubler (b) based on a Type MAX660 integrated circuit.

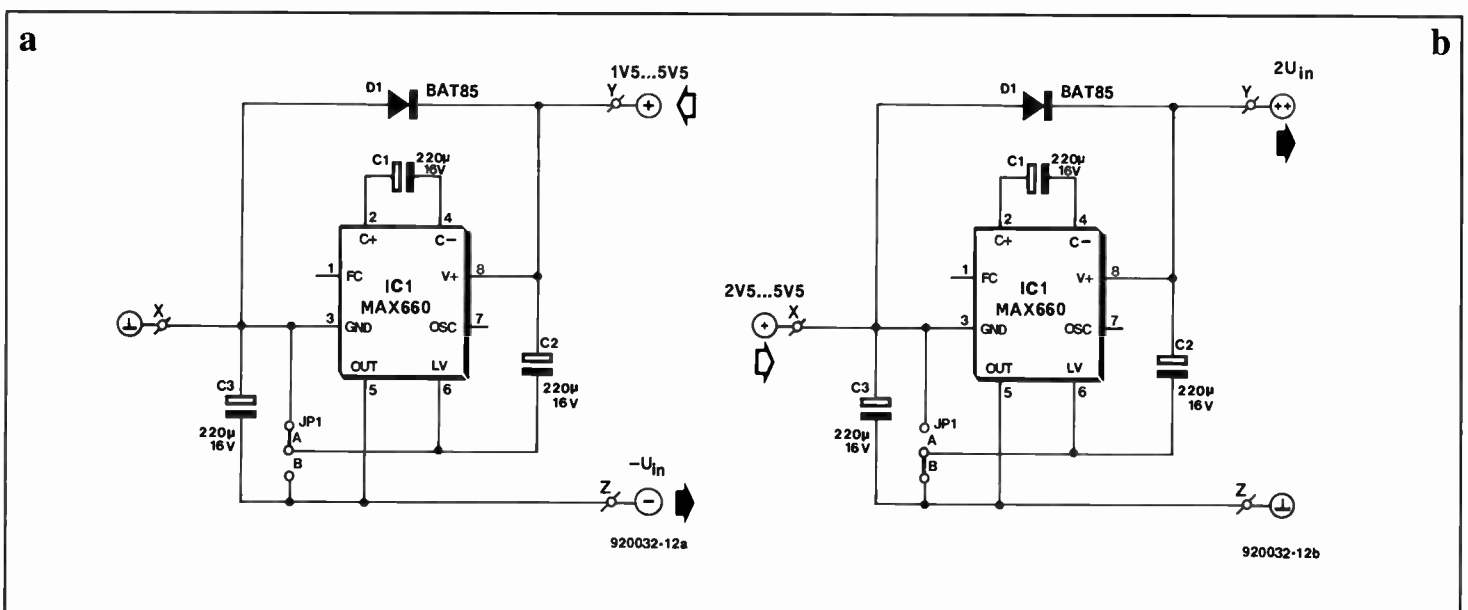


Fig. 2. The two circuits of Fig. 1 can be combined into one that can serve either as an inverter or as a doubler.

TABLE 1
Connections

	inverter	doubler
JP1	A	B
X	ground	in (2.5–5.5 V)
Y	in (1.5–5.5 V)	out
Z	out	ground

oscillator that operates at 10 kHz.

If, in Fig. 1a, S_1 and S_3 are closed (S_2 and S_4 are then open), C_1 will be charged. When these switches change over, C_1 and C_3 are in parallel, whereupon charge is transferred from C_1 to C_3 . Also, the polarity of C_1 with respect to earth is reversed (pin 2 was connected to $\oplus U_b$ and is now connected to earth, while pin 4 was connected to earth and is now connected to pin 5). The voltage across C_3 will thus be negative with respect to earth. In the absence of a load, a negative voltage

will arise across C_3 , whose level is equal to that of $\oplus U_b$. When the circuit is loaded, that negative voltage will not only decrease, but will also have a ripple. This is, of course, because C_1 can transfer only a limited charge, smaller than the one required, per unit time. On average, there will remain a smaller charge in C_3 , so that the voltage across this capacitor will drop.

When the switches are connected as in Fig. 1b, and a diode, D_1 , is added, the IC will double the input voltage. When the supply is switched on, C_2 is charged immediately to the supply voltage (less the forward voltage of the diode) via D_1 . This is necessary to ensure a supply to the oscillator. Furthermore, the charge need not be transferred via the IC. Here again, C_1 is the reservoir. It is charged when the switches are in the position shown. When the position of the switches is reversed, C_1 is in series with the supply voltage, U_b , so that the potential across it is $2U_b$. At the same time, C_2 is connected, so that charge is transferred from C_1 to C_2 . In that way, and provided the circuit is not loaded, a voltage arises across C_2 that is twice U_b . As in Fig. 1a, when a load is connected to the circuit, the output voltage, $2U_b$, will decrease in proportion to the load (see Table 3). Bear in mind that the input current will be twice as large as the output: the energy has to come from somewhere.

The circuits in Fig. 1a and Fig. 1b can be combined as shown in Fig. 2. The position of jumper JP1 and the connections to X, Y and Z are given in Table 1. Table 2 shows the function of each of the external components. When the circuit serves as voltage inverter, D_1 is not really required, but, together with a 160 mA fuse, it serves as protection against polarity reversal. Should the supply voltage be connected with incorrect polarity, it will be short-circuited by D_1 , whereupon the fuse blows.

The minimum input voltage to the doubler circuit cannot be as low as to the inverter circuit, because, in that configuration, the oscillator has difficulty in starting at too low a voltage. This happens particularly at input voltages below 3.5 V; above that level, the oscillator starts readily at all times.

Although the circuit is perfect for building into an existing design, there may be applications where it is used by itself and for those a printed circuit board—see Fig. 3—is provided.

TABLE 2
Function of various components

component	inverter	doubler
C1	pump	pump
C2	input buffer	output reservoir
C3	output reservoir	input buffer
D1	polarity protection	start up

TABLE 3
Measurement results

U_{in} (V)	R_L (Ω)	I_{in} (mA)	U_{out} (V)	U_{ripple} (mV _{pp})	Efficiency (%)
Inverter					
2.5	∞	0.1	-2.5	5	74
2.5	22	80	-1.8	100	
5.0	∞	0.2	-5.0	5	
5.0	47	97	-4.5	100	
Doubler					
2.5	∞	0.1	5.0	5	80
2.5	47	178	4.1	100	
5.0	∞	0.3	10.0	5	
5.0	100	190	9.5	100	

Maximum output current = 100 mA.

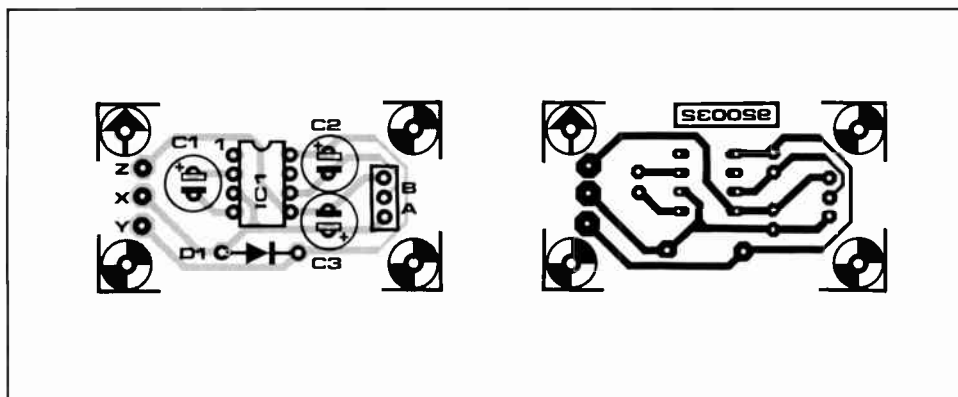


Fig. 3. Printed-circuit board for the inverter/doubler

PARTS LIST**Capacitors:**

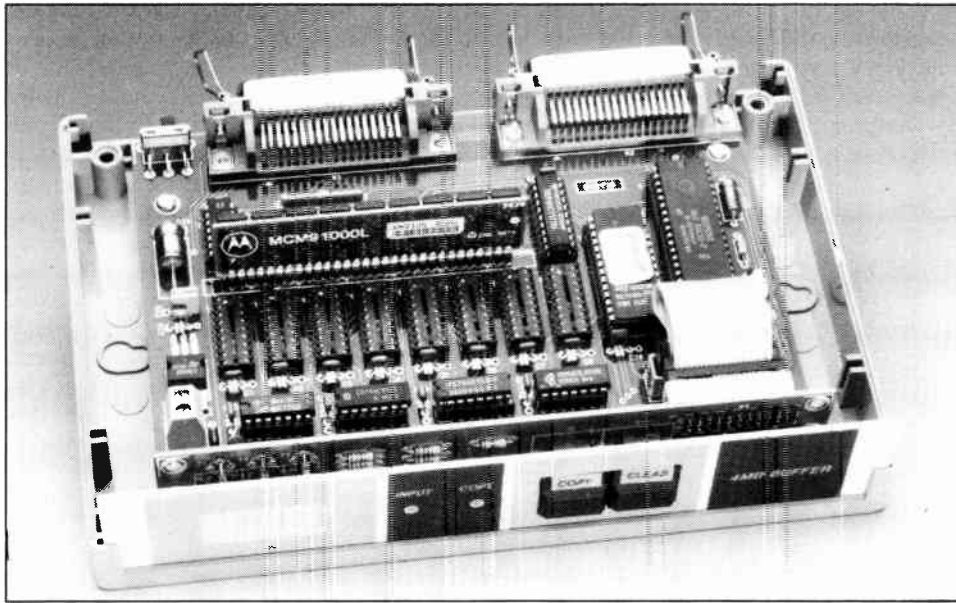
C_1 – C_3 = 220 μ F, 16 V, radial

Semiconductors:

D_1 = BAT85

IC1 = MAX660

4-MEGABYTE PRINTER BUFFER



Print files, whether they contain text, graphics or both, seem to become larger and larger as the programs that output them, and the printers that produce the 'hard copy', become smarter every day. That is all very well, but we do not want to see our ever so fast PC being held up by a simple task such as printing. The solution to this well-known bottleneck is to use a fast intermediate storage device with a large memory to capture the printer data supplied by the computer. Such a buffer is described here: it is Centronics-compatible, and offers a memory size of 1 MByte or 4 Mbyte.

Design by R. Degen

THE function of the printer buffer is easily described. It is a device connected between the computer's parallel printer (Centronics) port, and the input of the printer. The printer buffer accepts data very fast, and feeds it out again, patiently, to the printer. In other words, it is the printer buffer, not the computer, that has to wait for the printer. Precisely this feature saves you time, since the PC returns very quickly from its 'print' job, leaving the printer data in the buffer. The buffer, in turn, communicates with the printer at maximum speed. Since today's computers are nearly always faster than any type of printer, the buffer must be large enough to temporarily hold the largest possible 'chunk' of the data that forms the print file.

The above already defines the required interfaces: one at the computer side of the printer buffer, and one at the printer side. Here, the familiar Centronics interface is used at both sides. Apart from these (paral-

lel) interfaces, we require a couple of controls and a readout to keep an eye on what the printer buffer is doing. To keep the circuit as user-friendly as possible, it has been given some intelligence in the form of a microcontroller.

A brief overview

Figure 1 shows a simplified block diagram of the printer buffer, and Fig. 2 a flow chart of the control program executed by the internal microcontroller. Figures 1 and 2 lead up to the actual circuit diagram of the printer buffer, which is given in Fig. 3. Those of you familiar with microcontrollers will recognize the so-called embedded controller application, which is basically a small computer system tailored to a specific application.

The heart of the circuit is formed by three blocks: the microcontroller, IC9; the DRAM (dynamic random-access memory) section (IC1-IC8); and an EPROM, IC11. Further, the circuit contains three registers, IC13, IC14 and IC20, which provide a buffer function for the data that travels between the computer, the

MAIN SPECIFICATIONS

- Simple to use
- Compact design
- Uses industry-standard DRAMs or single SIP/SIM DRAM module
- One or four megabyte DRAM
- Power supply: internal or via printer
- Microprocessor-controlled (80C31)

printer and the display. Address decoding and register selection is arranged by IC12, a 74HCT138.

The circuit in detail

The control of the DRAM is fairly complex, and will therefore be looked at in some detail. Since an 8-bit microcontroller can address a RAM of 64 Kbyte only, some additional logic is needed if we want it to deal with a RAM of 4 MByte. Here, this additional logic consists of 2 bistables, four NAND gates and a little software.

DRAM refresh circuitry has to be added also, because it is not provided by the 8031 microcontroller. Although this would appear to call for a refresh counter implemented in software, a counting routine for 512 or 1,024 refresh cycles would, unfortunately, take too much valuable processor time. A different approach is, therefore, used.

To keep the refresh time as short as possible, the microcontroller's 'external memory access' signal is used. Since the PSEN output of the 8031 is actuated twice during every processor cycle ($16 \text{ MHz}/12 = 750 \text{ ns}$), it can be used to derive the RAS (row address strobe) signal needed for the DRAMs. Address information being available during the PSEN pulse, all that is needed further is ensuring that the correct addresses are applied to the RAMs. To arrange this, the processor jumps to a subroutine that starts at address 1000H, where a sequence of 512 2-byte instructions is started. The only function of this part of the program is to enable the controller to increase the value on address lines A0-A9 sequentially. This type of refresh control is usually referred to as RAS-only-refresh.

The control of the read and write functions of the DRAMs is arranged via the $\overline{\text{WR}}$ line of the microcontroller. To address a DRAM IC, the column address must be supplied before the row address. This is achieved by actuating the output of the controller's RAS-enable function (pin 15). Next,

the row address is put on to the databus with the aid of a MOVX instruction. At the same time, the controller's WR line is pulled low, which causes the output of the bistable (pin 6 of IC18a) to go low also. The signal arrives at the RAS connections of the DRAMs via NAND gates IC15b and IC15c. In this way, the row addresses are conveyed to the DRAMs.

Next, the column addresses have to be supplied. To begin with, the controller's CAS (column address strobe) enable function (pin 14) is actuated. Next, the column address is placed on to the databus with the aid of a MOVX instruction, while the microcontroller's WR line is pulled low. This signal arrives at the CAS inputs of the RAMs via NAND gate IC15d, and at the clock input of bistable IC18b. In this way, the column addresses are conveyed to the DRAMs.

When the output of IC18b is actuated on the positive edge of the WR signal, this bistable resets the RAS line to its normal level. An R-C network ensures that IC18b is reset immediately after the RAS line. From then on, the microcontroller can write data into the DRAMs.

A further interesting section of the circuit is the Centronics input. To enable this to respond sufficiently fast to the computer's strobe signal, a bistable circuit was designed that pulls the BUSY line high the instant the strobe pulse appears. At the same time, data

is stored in a register. The microcontroller resets the bistable after reading the register. The fast operation of this circuit prevents data loss.

The printer buffer may be powered in two ways: by its own, internal, supply, or by the printer it is connected to. The selection between these two possibilities is made with switch S3 on the board. If CMOS components are used, the current consumption of the buffer lies between 150 mA and 200 mA.

Control software

After powering up, the internal memory of the buffer is tested. When the test is finished, the memory size is briefly shown on the 3-digit LED readout. The indication '1.02' stands for 1 MByte, and '4.09' for 4 MByte. By the way, these figures do not indicate that all bits in the memory function correctly; the basic memory test is too simple for that, and, based on a few random tests, serves only to determine the memory size.

As soon as the memory size has been determined, the size indication is replaced by '000'. At the same time, the INT line on the Centronics bus is pulled low to reset the printer to its default mode. Next, the controller waits for the strobe line of the computer to go high. When this happens, the buffer is switched to receive mode. The advantage of

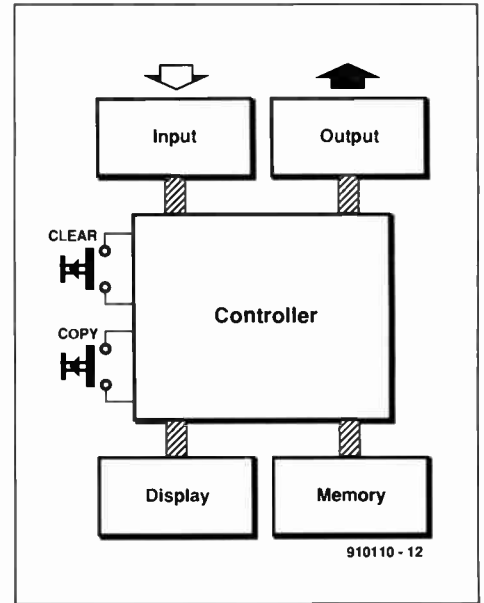


Fig. 1. Simplified block diagram of the printer buffer.

this sequence is that the buffer can not be loaded with incorrect data when the computer is not yet switched on, while the buffer is on.

RAM test

It is possible to test every bit in the buffer

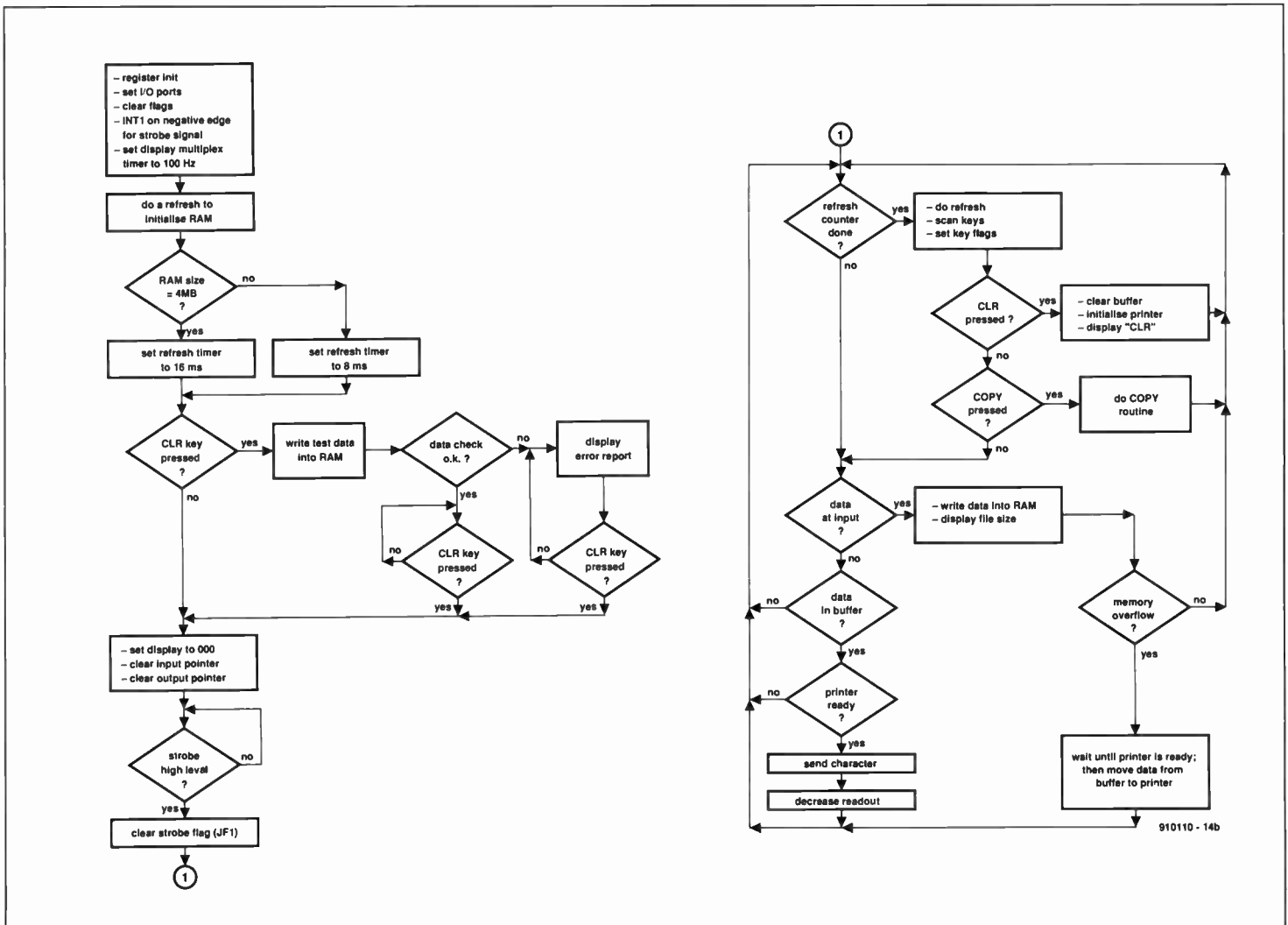


Fig. 2. Flow diagram of the control program developed for the printer buffer.

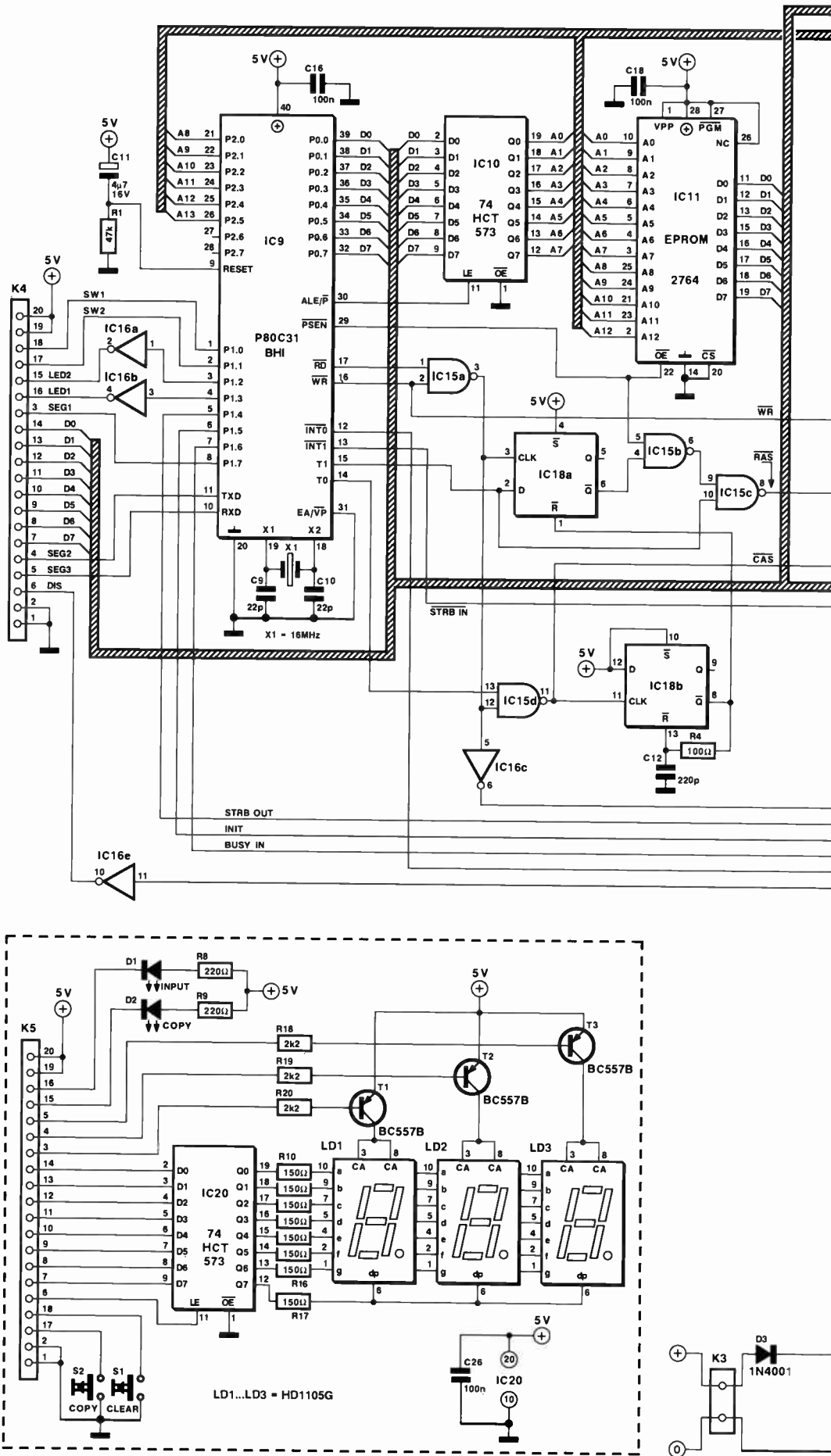
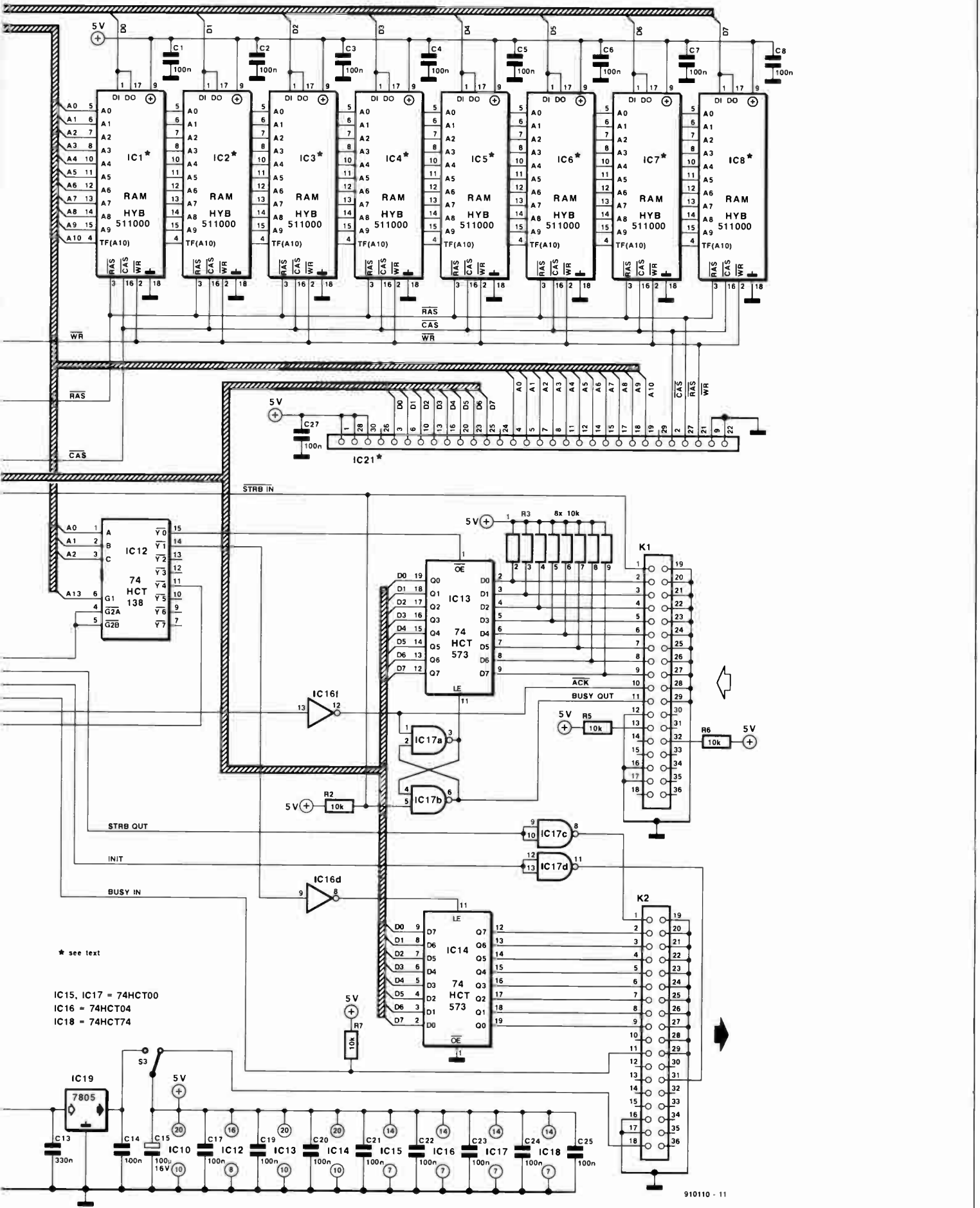


Fig. 3. Circuit diagram of the printer buffer. Remarkably, the microcontroller needs very little external hardware to perform a not so simple

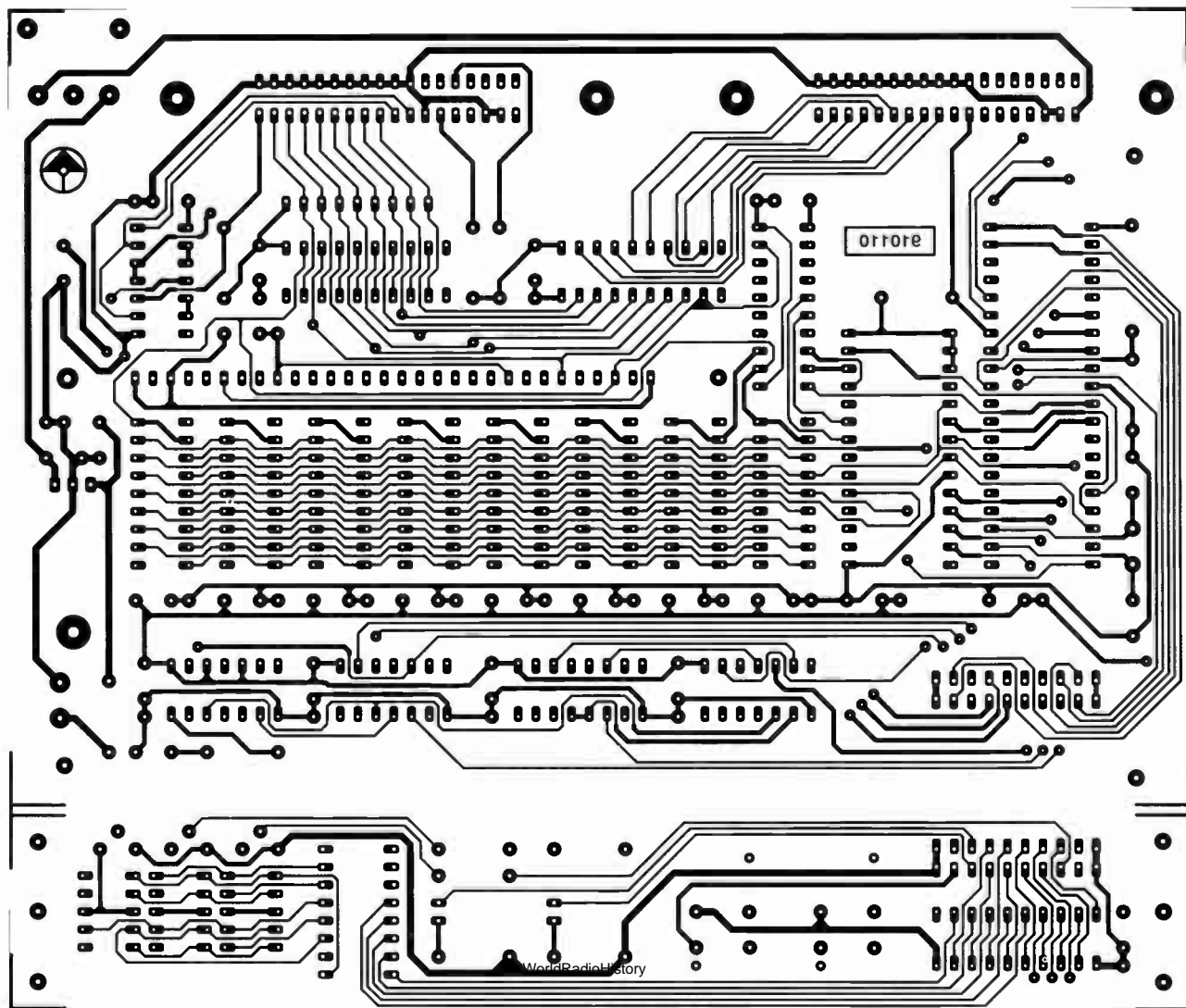
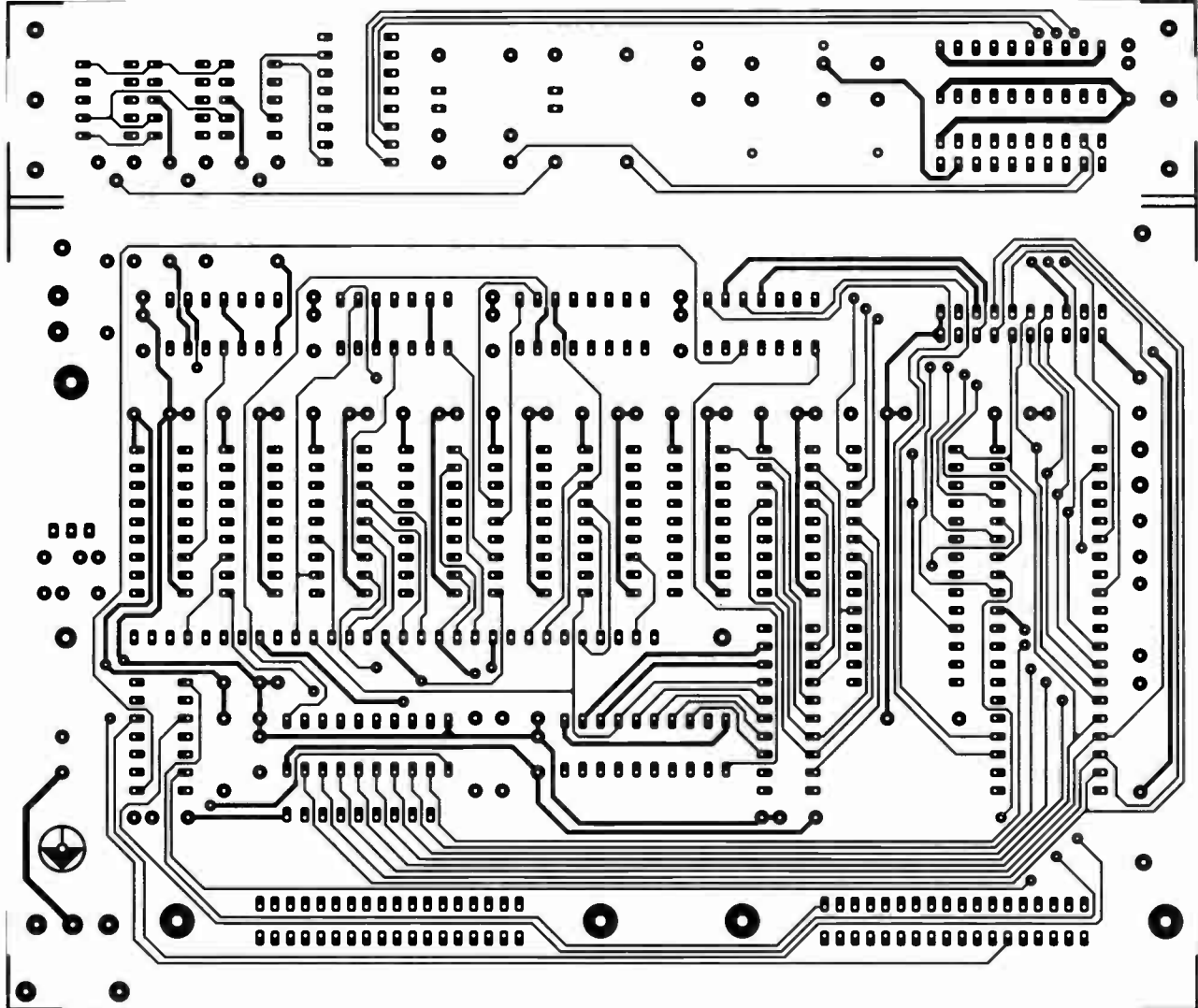


* see text

IC15, IC17 = 74HCT00
 IC16 = 74HCT04
 IC18 = 74HCT74

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function.



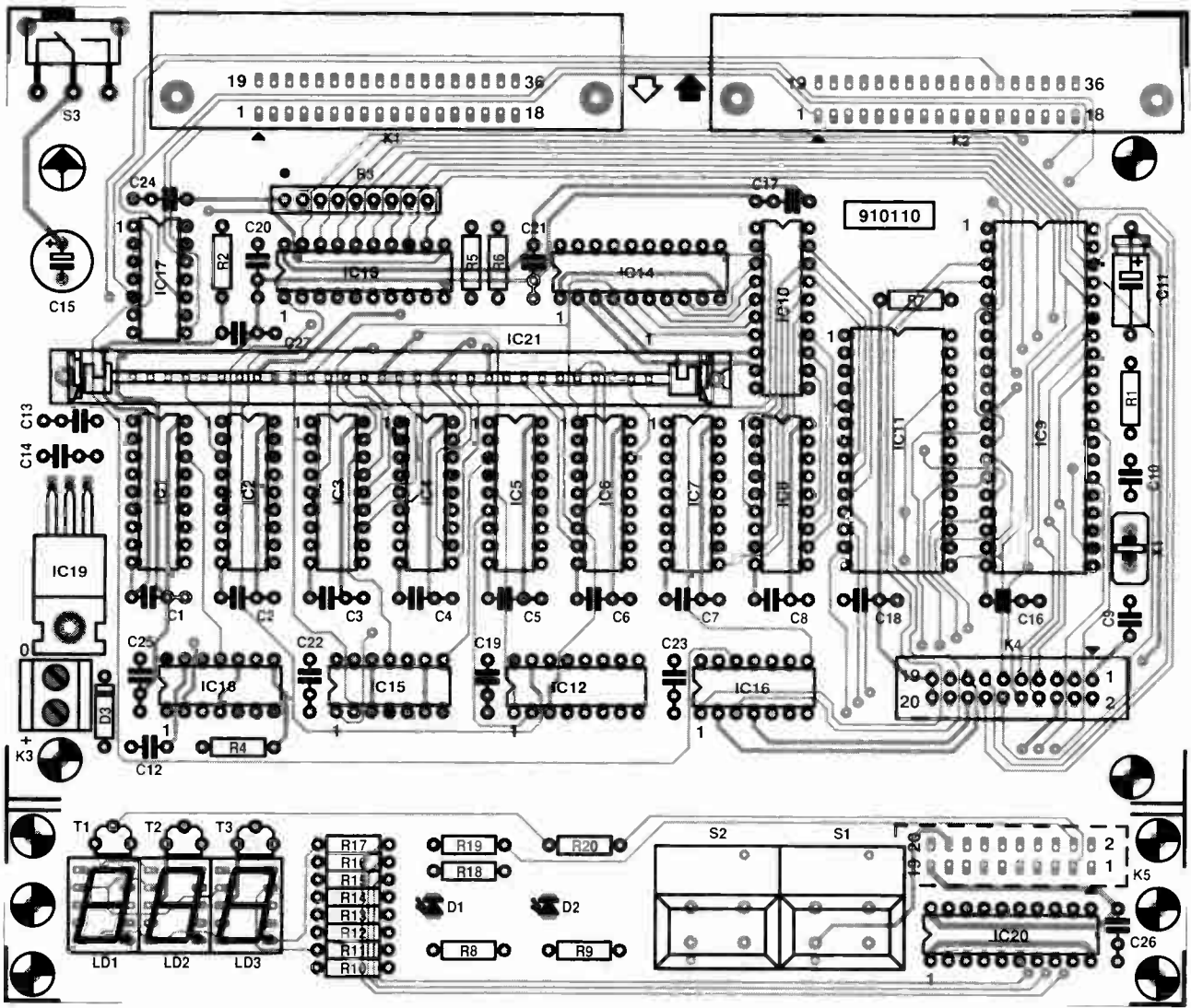


Fig. 4. On previous page: track layouts (mirror images) of the component side and the solder side of the double-sided through-plated PCB. Above: component overlay.

COMPONENTS LIST

Resistors:		or MT4C1004 (4MByte)	IC1-IC8	2 Digitast push-button	S1;S2
1 47kΩ	R1	OR		1 Change-over slide switch	
4 10kΩ	R2;R5;R6;R7	1 SIPP or SIMM 1MByte×8,		for PCB mounting, with	
1 8-way 10kΩ SIL array	R3	1MByte×9, 4Mbyte×8		angled pins	S3
1 100Ω	R4	or 4Mbyte×9	IC21	1 Quartz crystal 16MHz	X1
2 220Ω	R8;R9	1 80C31BH-1	IC9	1 Printed circuit board	910110
8 150Ω	R10-R17	4 74HCT573	IC10;IC13;IC14;	1 Front panel foil	910110-F
3 2kΩ	R18;R19;R20		IC20	1 Enclosure 75-1410J (Vero)	
		1 2764 (150ns)		1 SIMM adapter (if required)	
		(ESS6041)	IC11		
Capacitors:		1 74HCT138	IC12		
21 100nF	C1-C8;C14;	2 74HCT00	IC15;IC17		
	C16-C27	1 74HCT04	IC16		
2 22pF	C9;C10	1 74HCT74	IC18		
1 47μF 16V	C11	1 7805	IC19		
1 220pF	C12				
1 330nF	C13	3 HD1105G			
1 100μF 16V radial	C15	or TDS3150	LD1;LD2;LD3		
Semiconductors:		Miscellaneous:			
2 LED, red, 3mm	D1;D2	2 36-way female Centronics			
1 1N4001	D3	connector for PCB mounting	K1;K2		
3 BC557B	T1;T2;T3	1 2-way PCB terminal block			
8 HYB511000 (1MByte)		(pitch: 5mm)	K3		
		2 20-way box header	K4;K5		

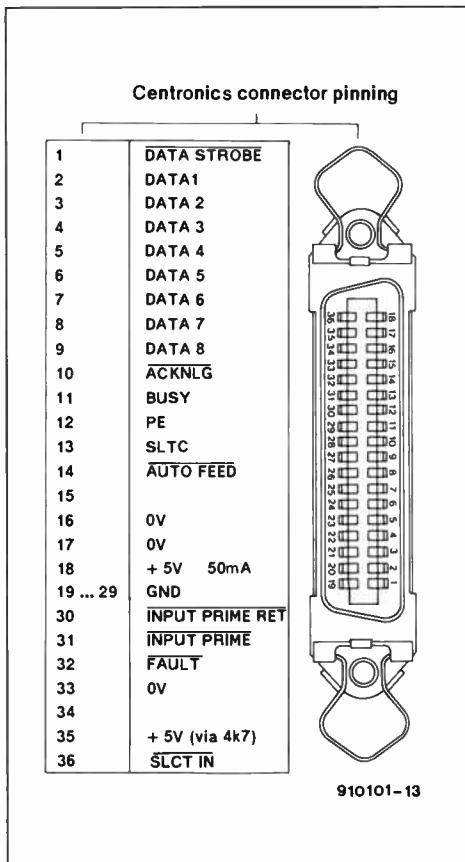
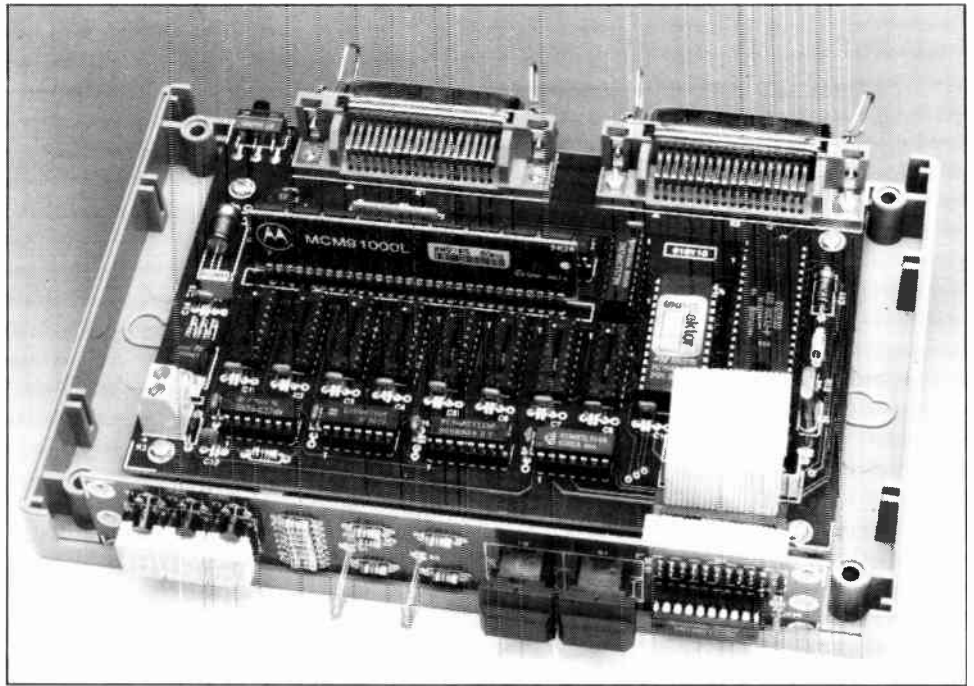


Fig. 5. Centronics connector pinning. Check this against the data given in the manual that came with your printer.

memory. This may be done by keeping the CLR key pressed while the buffer is switched on. As long as no error is found, a counter counts from 000 to 1.04 (for 1,048,576 bytes) or 4.19 (for 4,194,304 bytes). When a faulty RAM location is found, the counter stops, and the display indicates 'err'. The RAM test, which takes a few minutes to complete, may be terminated any time by pressing the CLR key.

Construction

The PCB section that forms the keyboard/display (controls) unit is cut off from the board supplied through the Readers Services. The artwork for the double-sided,



through-plated board is given in Fig. 4. The completed controls board is fitted behind the front panel of the Vero enclosure. When the LED displays are fitted in IC sockets, they are at about the same height as the key caps of the push-buttons.

There are several options in regard of the buffer RAM. One is to use so-called SIM modules (SIMMs), which are commonly used in PCs. These are available as 1-MByte or 4-MByte modules with a 'width' of 8 or 9 bits. SIMMs have PCB edge connectors like PC extension cards, and require a special adaptor with snap-in side latches (Fig. 6) to enable them to be mounted on to the main printer buffer board.

SIP modules are equally suitable, and also come in 1-MByte or 4-MByte, and 8- or 9-bit, versions. Having pin connections, they do not require adaptors to be fitted on to the board.

The last memory option is to use eight 1-Mbit or 4-Mbit RAM ICs in DIL packages. Unfortunately 4-Mbit ICs like the MT4C1004 are still pretty expensive and difficult to obtain. If you can get them, make sure that they

are 18-pin DIL types — it appears that the enclosure is not the same with all manufacturers. Finally, it is not possible to fit both a module and discrete RAMs at the same time, for instance, to create a RAM of 2 Mbyte.

Practical use

Connect the input of the printer buffer (K1) to the Centronics output of the computer, and the output of the printer buffer (K2) to the input of the printer. These connections are made with standard Centronics printer cables.

The amount of data sent to the printer buffer is shown on the display, rounded to whole kilobytes. The printer buffer starts to feed out data immediately if it finds that the printer is 'on line'. This may be stopped by pressing the CLR key, whereupon the display reads 'Clr'. Next, the data in the buffer is cleared, and the display indicates '000' again.

The copy function of the printer buffer may be used to produce copies of the print file. This function is available only when the computer is not sending data any more, and the printer has read all data from the buffer. The copy function is automatically disabled when a memory overflow occurs, so that only files that fit in the buffer memory can be printed more than once (i.e., copied). The copy function is started by pressing the 'COPY' key, whereupon the associated LED will start to flash. Copying can be terminated at any time by pressing the 'CLR' key, and started again by pressing 'COPY'. If, however, the 'CLR' key is pressed a second time, the buffer memory is cleared, and the printer is initialised. Since it is required for the copy function that the last received file is duplicated (rather than the complete contents of the buffer memory), the control software contains a strobe-timeout routine that marks the start and end addresses of a file, about 40 s after the last strobe signal received from the computer. ■

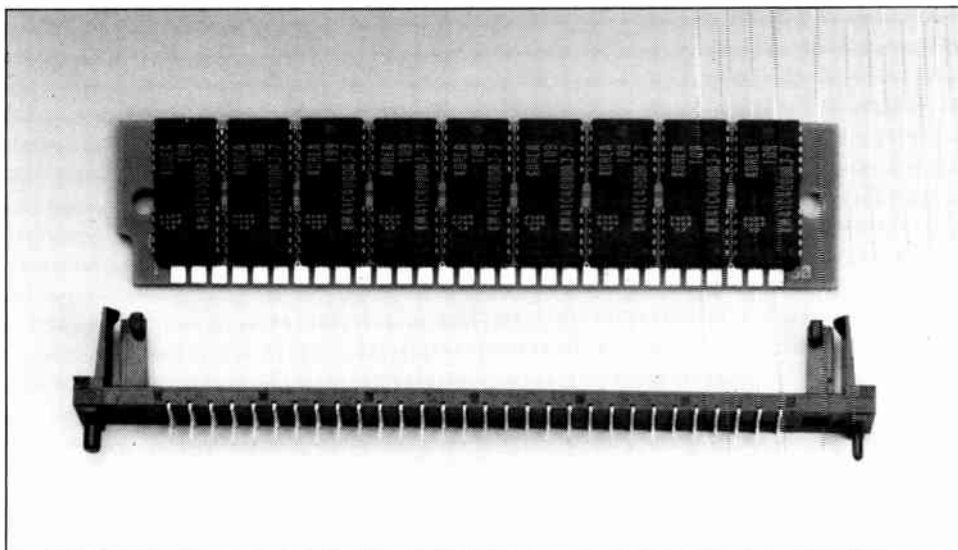
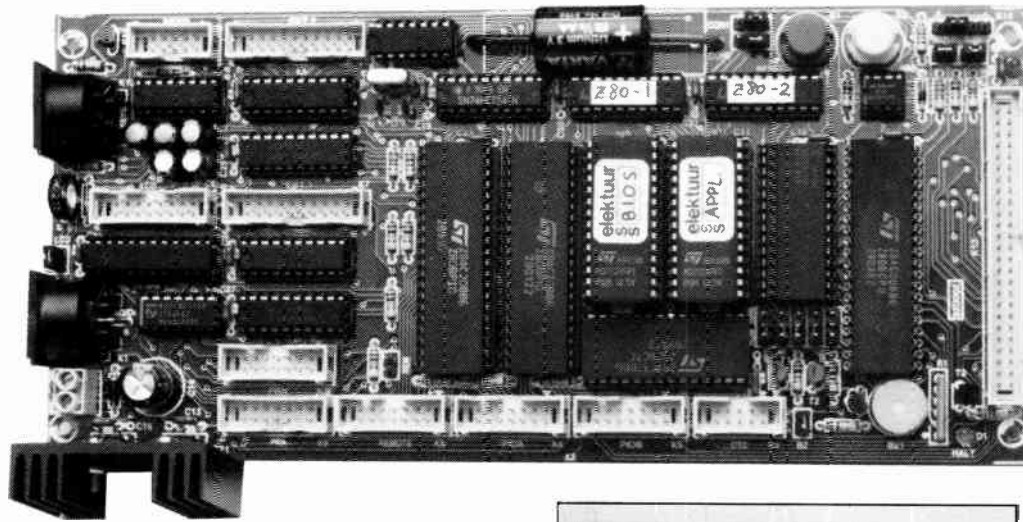


Fig. 6. A bracket-style adaptor as shown here is required if you want to use a SIM module.

MULTI-PURPOSE Z80 CARD

PART 2: CONSTRUCTION AND TEST



Following last month's description of the system structure and the circuit diagram, this second and last instalment looks at building and testing the card.

Design by A. Rietjens

Test routines in BIOS

The card can be tested with the aid of a number of routines contained in the BIOS. These test routines are called automatically when only the BIOS is present. However, they may also be run when an application program is executed that starts up the card. All that is required to call the tests is to keep a key pressed while the system starts. The way in which the application is called offers the possibility to change the I/O routines (to a certain extent) for your own use. This is so because two routines contained in the application EPROM are called when the system starts: the first before, and the second, after, the test routines. For example, the first routine may set up a key code translation table for the IR receiver, which may be verified via the keyboard test routine. The second routine then contains the application proper.

Software support

The diskette available for this project (MSDOS 360 KByte 5¼-inch; order code

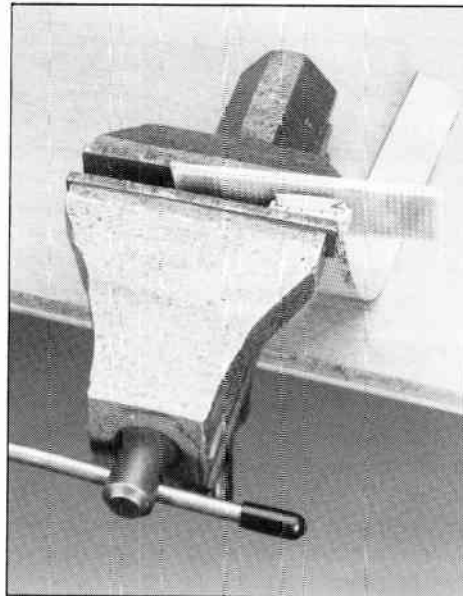


Fig. 7. There is nothing mysterious about fitting an IDC connector on to a flatcable. As shown here, a small vise does the trick. For IDC plugs, make sure that the pins are temporarily inserted into a few pieces of strip-board.

1711) contains examples that demonstrate the practical use of some of the software features discussed earlier. Among the examples are the things you have to put in an EPROM to enable it to be identified by the BIOS, and a software 'hook' that adds a routine to the 10-ms interrupt of Timer 3.

Also contained on the disk are the Turbo Pascal procedures used to produce the basic functions of the RS232 interface. After switching on the card, the baud rate and transmission format are automatically set to 2400 bit/s, 8 data bits, no parity, 1 stop bit.

The disk contains a file that enables owners of an EPROM programmer to burn their own BIOS EPROM. Those of you who do not have an EPROM programmer may

SOFTWARE SUPPORT

The multi-purpose Z80 is supported by the following software:

- **ESS 6111:** a set of two GALs for address decoding and memory decoding;
- **ESS 6121:** one programmed 27128 EPROM containing the BIOS;
- **ESS 1711:** one 5¼-inch 360-KByte MSDOS diskette containing the following files:
 - description of BIOS calls with examples (if necessary depending on the routine's level of complexity);
 - example of how the BIOS file can be incorporated in your own source code file;
 - description of the system variables;
 - EPROM listing of the BIOS in hexadecimal and binary format
 - assembly programming examples of (1) a 'hook' and (2) an EPROM definition for your own application;
 - description of how to put the contents of two EPROMs into a single 27256, so that 64 Kbyte RAM may be used;
 - Pascal source code listing of serial port control routines;
 - description of the serial command set.

Prices and ordering details relevant to these software items may be found on the Readers Services page elsewhere in this issue.

obtain the BIOS EPROM through our Readers Services as item 6121. The BIOS file is also required when you wish to use 64 KBytes of RAM, since in that case the BIOS and the application are both contained in a single 27256 EPROM. How the two are combined is explained on the diskette.

The source code (assembler file) of the BIOS is not contained on the diskette; only a list with call addresses is provided, and instructions for use.

Connections to the outside world

Your own hardware experiments may be connected to the Z80 card via flatcables. Care should be taken to observe the polarity of the IDC headers on the cables, and the box

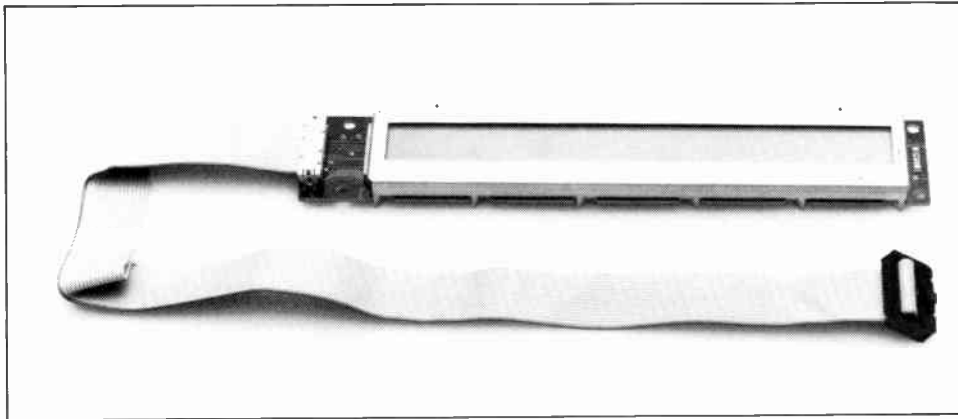


Fig. 8. The Hitachi LM092LN LCD is simple to connect via a 16-way flatcable with an IDC plug at one side, and an IDC socket at the other.

headers on the board. On both devices, pin 1 is usually marked by a small arrow. When making the flatcables, make sure that pins 1 of the IDC sockets you press on either end go to the same wire in the cable. To reduce cost, one side of the flatcable can be fitted with a connector for PCB mounting. In this way, you save on the cost of a boxheader. The PCB-mount IDC connector should, however, be fitted at one side of the cable only (preferably not at the side of the Z80 card). In this way, the Z80 card is always available as a kind of motherboard to which application circuits can be connected as required. Use a small vise to clamp the IDC sockets on to the flatcable. To protect the pins of the PCB connectors, these are best inserted into two or three stacked pieces of veroboard (see Fig. 7).

The components list contains all connec-

LCD CONNECTIONS		
	K10	Display
1	GND	VSS
2	+5V	VDD
3	CONTRAST	Vo
4	A1	RS
5	A0	R/W
6	DISP	E
7	D0	DB0
8	D1	DB1
9	D2	DB2
10	D3	DB3
11	D4	DB4
12	D5	DB5
13	D6	DB6
14	D7	DB7
15	BL	A(node)
16	GND	C(athode)

Fig. 9. Pinning of K10 (Z80 card) and the LCD. If necessary, the LCD back light may be powered separately via flatcable wires 15 and 16 (see text).

tors and flatcables necessary for the applications implemented on the Z80 card. The cables required are described below.

Liquid crystal display

The PCB connector for the LCD also provides the supply voltage for back-lighted displays. The LCD type given in the parts list is the easiest to use since it may be connected via a 'straight-through' 16-way cable. One end of a piece of 16-way flatcable is fitted with a normal IDC socket, and the other end with an IDC plug for PCB mounting (see Fig. 8). As already mentioned in last month's instalment, almost any LCD with one or two lines of up to 40 characters, with or without back-lighting, may be used. Although the pin functions of the LCDs seem to be standardised, the actual positions of the pins may differ. The back light must be an LED (there are also LCDs around that use a higher voltage for the back light). Depending on whether current drive or voltage drive is required, resistor R21 is calculated to pass the required current, or it is short-circuited. If the back light is powered via two separate connections instead of two wires in the flatcable, it is best to split wires 15 and 16 from the flatcable, and solder these directly (wire 15 = BL = anode; wire 16 = ground = cathode). The LCD connections are given in

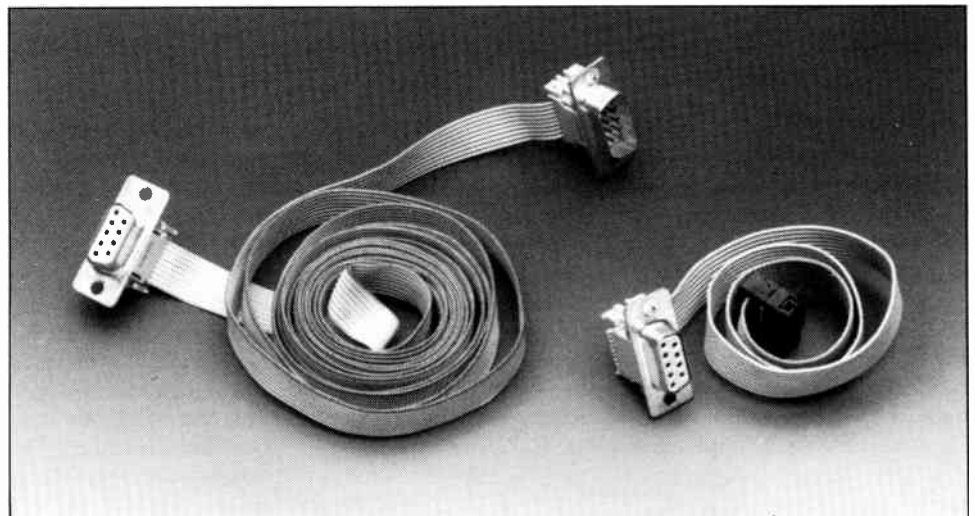


Fig. 11. A standard 9-to-9 male-to-female RS232 cable is not difficult to make from a length of flatcable and two IDC connectors.

RS232 CONNECTIONS	
K11	D9-Connector (female)
1	1
2	6
3	2
4	7
5	3
6	8
7	4
8	9
9	5
10	

Fig. 10. Refer to this pinning overview in case you are forced to use a solder type 9-way sub-D connector for the RS232 link.

Fig. 9 for your reference. Whatever LCD type you use, make sure you have at least the connection diagram!

RS232 cable

Pay attention when making the RS232 flatcable. The pinning of the PCB connector does not correspond to that of a standard solder-type 9-way female sub-D connector. Here, we suggest the use of an IDC-style sub-D connector, i.e., one for flatcable mounting. The other end of the 9-way flatcable is fitted with a 10-way IDC socket of which pin 10 is not used. Those of you who wish to use a solder-type sub-D connector may find the connections listed in Fig. 10.

When the Z80 card is fitted in an enclosure, the 9-way sub-D connector will normally be fitted on the rear panel, so that a very short cable is required. A standard 9-to-9 male-to-female RS232 cable is then used to connect the Z80 system to a PC. If you can not obtain such a cable, you may have to make one yourself from a length of flatcable and two IDC connectors (see Fig. 11). Make sure that pin 1 of the female connector goes

to pin 1 of the male connector.

Infra-red remote control

The RC-5 infra-red remote control receiver is connected to the Z80 card via a length of 14-way flatcable. One end of the cable is fitted with an IDC socket, the other with an IDC PCB connector (see Figs. 12 and 13). The IR receiver module may be fitted on a front panel, together with the LCD. It is then best mounted on a small aluminium plate, which is secured to the rear side of the LCD. This requires the connections to the LED and the photodiode to be extended with wires to enable these components to be fitted on the front panel (see Fig. 13).

Printer connection

There are two printer connections: a standard one, PRN, and another, PRN', for specific applications. Figures 14 and 15 illustrate how the PRN connector is wired to a 25-way female D connector, to which a standard Centronics printer cable may be connected.

Battery backup

The memory backup battery may be either a dry cell, a rechargeable battery, or a lithium battery. Depending on the battery type used, one or two jumpers have to be fitted (Fig. 16).

Make sure that the jumpers are correctly fitted, because dry cells and lithium batteries must never be charged. When a lithium cell is used, this must be shunted by a 3.3-M Ω resistor to compensate the leakage currents that would otherwise cause the battery to be charged. Although we could not measure the charge current even at a resolution of 0.1 μ A, it could be shown that the lithium battery on our prototype board was being charged, hence the use of the shunt resistor to prevent problems. The 3.3-M Ω resistor is best fitted at the solder side of the PCB.

The minimum and maximum battery voltages are 2 V and 4 V respectively. When the system is switched off, the current consumption of the RAM ICs is between 2 μ A and 4 μ A.

Construction and test

The PCB designed for this project is remarkably compact, and fits in a Retex Type RE.4 enclosure. Although the track layouts of both sides of the PCB are given in Fig. 17, along with the component mounting plan, it is not recommended to make this PCB yourself, mainly because of the high track density and the large number of through contacts.

Before you start populating the board, file away a small piece of PCB material near connector K2. This allows the supply wires to be bent away more easily later.

The ICs are best fitted last. It is recommended to use boxheaders in the connector positions on the board. A boxheader is a pin header with a plastic enclosure around it. It has a polarizing hole that prevents an IDC socket being inserted the wrong way around. If you have never seen a box header before, look at the photographs in this and last month's instalment. If the LCD men-

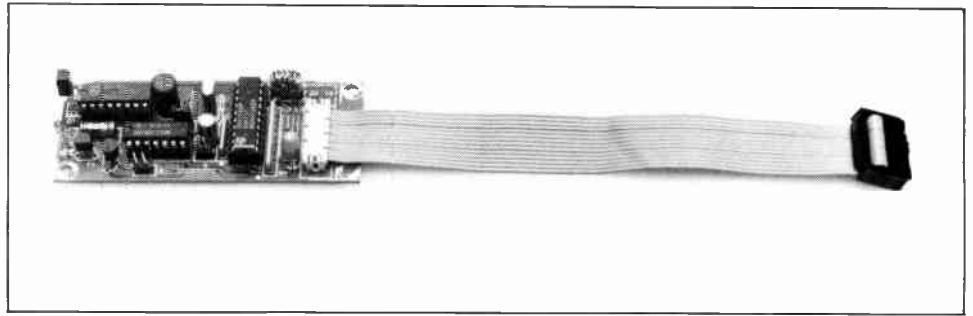


Fig. 12. The IR receiver is hooked to the Z80 card via a length of 14-way flatcable fitted with an IDC socket at one end, and an IDC plug (for PCB mounting) at the other.

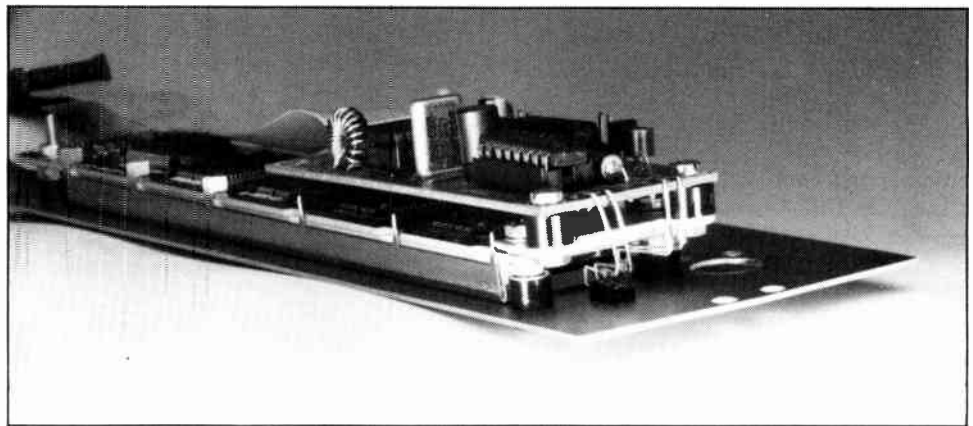


Fig. 13. Suggested mounting of the infra-red receiver on a small piece of aluminium secured to the rear of the LCD unit. The LED and photodiode connections need to be extended in this case to enable the opto components to be fitted on the front panel.

tioned in the parts list is used, fit a wire jumper in position R21.

First, connect the Z80 card to a suitable power supply, and check that the current consumption is normal, i.e., a few milli-amps (the ICs are not fitted as yet). Next, perform the step-by-step test procedure given below. Each time you switch on the card, keep an eye on the current consumption, which is a good indicator when something is amiss. The typical current consumption of the Z80 card with all IC fitted will be around 100 mA; about 150 mA with the PC-XT keyboard connected, and about 300 mA with the keyboard and the back-lighted LCD connected.

Do not forget to switch off the power supply in between the steps. If the circuit does not behave as described, check for errors around the component(s) last fitted.

1. Fit IC18, and use an oscilloscope to check that the oscillator works (pin 6).

2. Fit the following ICs and jumpers: IC4 (Z80B-CPU); IC8 and IC9 (Z80 decoder 1 and Z80 decoder 2; GALs; order code 6111), IC19 (bankswitching); JP1 to JP5 at the ROM-select side. Set the memory configuration to '0' by fitting the 'con-0' jumper in position '0', and the 'con-1' jumper in position '0' also.

3. Fit IC1 (EPROM ESS 6121, a type 27128), and the LCD. Before re-applying power, temporarily connect the cathode of D5 to ground, and set P1 to mid-travel.

PRINTER CONNECTIONS

K9	D25-Connector (female)
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	10
11	11
12	12
13	13
14	18 - 25

Fig. 14. Printer cable connections.

When power is applied, the Z80 runs a RAM test. Since there is no RAM as yet, he result is negative, and the processor is switched to the 'halt' status, which is retained because no interrupts have been initialized as yet. Thus, if the card works correctly so far, the 'halt' LED must light.

The LCD is not yet initialized, but will indicate an empty line and a black line when

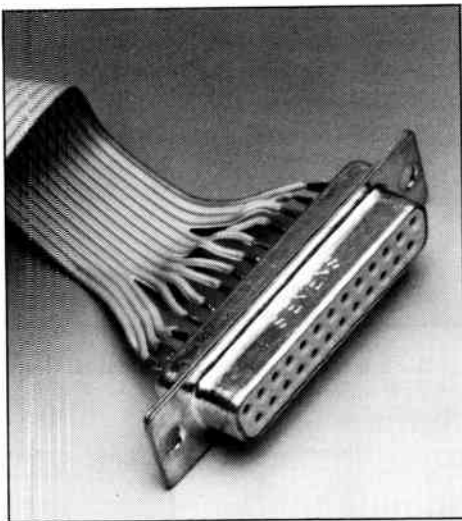


Fig. 15. Centronics printer cable details.

correctly connected. If nothing shows on the LCD, try to adjust the contrast by turning preset P1. If this does not work, review the LCD connections. If you are using a back-lighted LCD, concentrate on the LED current. Measure the current consumption via the jumper marked 'LCD' — typical values are of the order of 120 mA to 150 mA. When current drive is used, the value of R21 must be determined by experiment. Fit jumper 'LCD' if you wish to have the back light on permanently.

4. Fit IC3 (a 43256 32-KByte RAM), IC7 (Z80B-PIO), IC5 (Z80B-CTC), jumper BZ, IC:0 (MAX690), a jumper on pins 4 and 5 of K14; IR receiver and/or keyboard. After applying power, the 'halt' LED will not light permanently any more, which indicates that the upper addresses (08000H to 0FFFFH) in the RAM are 'good' (by the way, the RAM test is non-destructive, i.e., any data that was present before running the test remains intact and at the original location).

When this part of the RAM test is successfully completed, a copyright message is output to LCD, informing you that 32 KBytes of memory have been found. Also, a beep sounds to indicate that the I/O has been initialised. Next, a second RAM test is run to check for the presence of RAM in parallel with the EPROM (10000H to 17FFFH). After this test, a memory overview is shown. If no additional memory is found, the 'halt' LED lights briefly. If additional memory is found, a second beep sounds. The parallel RAM

BATTERY JUMPER CONNECTIONS					
Pin number (K14)	1	2	3	4	5
no battery				<u>4</u>	<u>5</u>
normal battery			<u>3</u>	<u>4</u>	
Lithium battery		<u>2</u>	<u>3</u>		
NiCd battery	<u>1</u>	<u>2</u>		<u>3</u>	<u>4</u>

Fig. 16. Battery options and jumper settings.

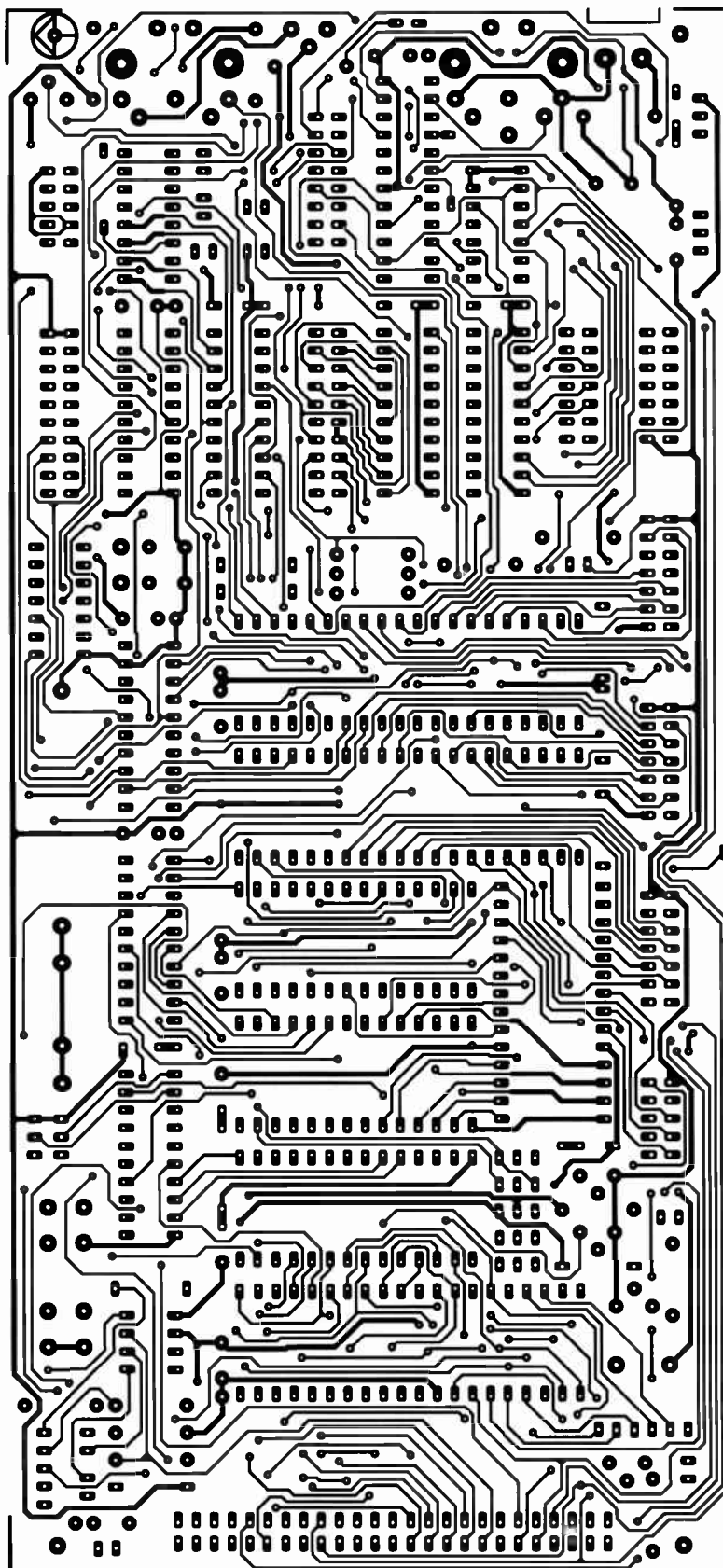


Fig. 17a. Component side track layout (mirror image).

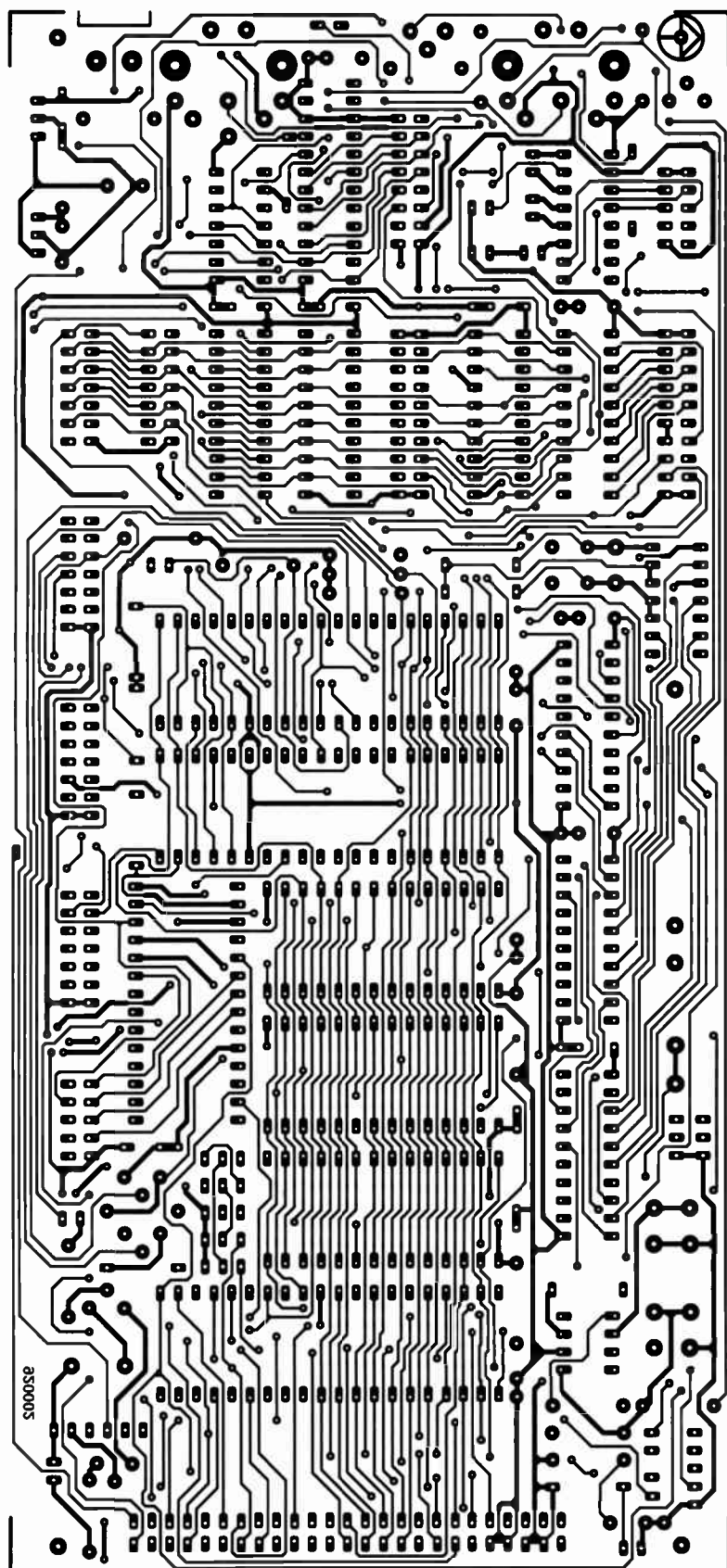


Fig. 17b. Solder side track layout (mirror image).

configuration is allowed in memory configurations 1, 2 and 3 only. Since we have set configuration '0' for the moment, no parallel RAM will be found, so that the RAM test will indicate 32 KByte, and only one beep sounds.

At this point, the Z80 card is in a wait cycle, which is left when a key is pressed on the keyboard. Next, the screen is cleared, and the system is in the display and keyboard test procedure.

The system tests the LC display as follows. Characters typed on the keyboard are displayed in the top line of the LCD. Next, the character is read back from the LCD, and copied to the same position in line 2. When a line is full, it is cleared for a short period, which results in the display flashing on and off while all positions show the last typed character. In this way, the system tests the read and write functions of the display.

When the ESC key is pressed, or the channel '1' key on the IR transmitter, the system switches to the next test routine. The system now responds to keyboard entries by beeping when a key is pressed, and displaying the character on the LCD. This test allows you to check that the keys work and produce the right codes.

5. Fit IC12 (COM81C17), and IC13 (MAX232). Before applying power, remove the wire between the cathode of D5 and ground, and set P1 to mid-travel. The RS232 interface is tested by connecting it to itself: connect RxD to TxD, and CTS to RTS. This is readily done by fitting two jumpers on the 10-way box header: link pin 3 to 5, and pin 4 to pin 6.

After powering up, readjust P1. Skip the first two tests by pressing the ESC key three times. In this way, you enter the RS232 test routine, which is basically the same as the LCD test. Typed characters are sent and received ('echoed') via the RS232 interface. If the jumpers are not fitted, you will only hear beeps, and no characters will appear on the LCD.

6. Fit IC11 (AD7569), and connect a 100-k Ω potentiometer and a multimeter to K1, as shown in Fig. 18.

After powering up, step through the test routines by pressing the ESC key until the A-D/D-A test routine is reached. The voltage reading on the multimeter must change proportionally as you turn the potentiometer. The voltage range is 0 V to 2.5 V when no jumper is fitted on pins 1 and 3. If the jumper is fitted, the range is 0 V to 1.25 V (in which case half of the travel of the potentiometer 'does nothing').

7. Fit IC16 (74HCT574) and IC17 (74HCT541). Press the ESC key as many times as necessary to arrive at the printer test routine. The message 'Test printer Y/N' appears. If you type 'Y', the Z80 card transmits three lines of text to the printer. An error message is produced when the printer is not connected. If everything is all right so far, the system prints the text shown in Fig. 19. When the system has finished printing the text, you are

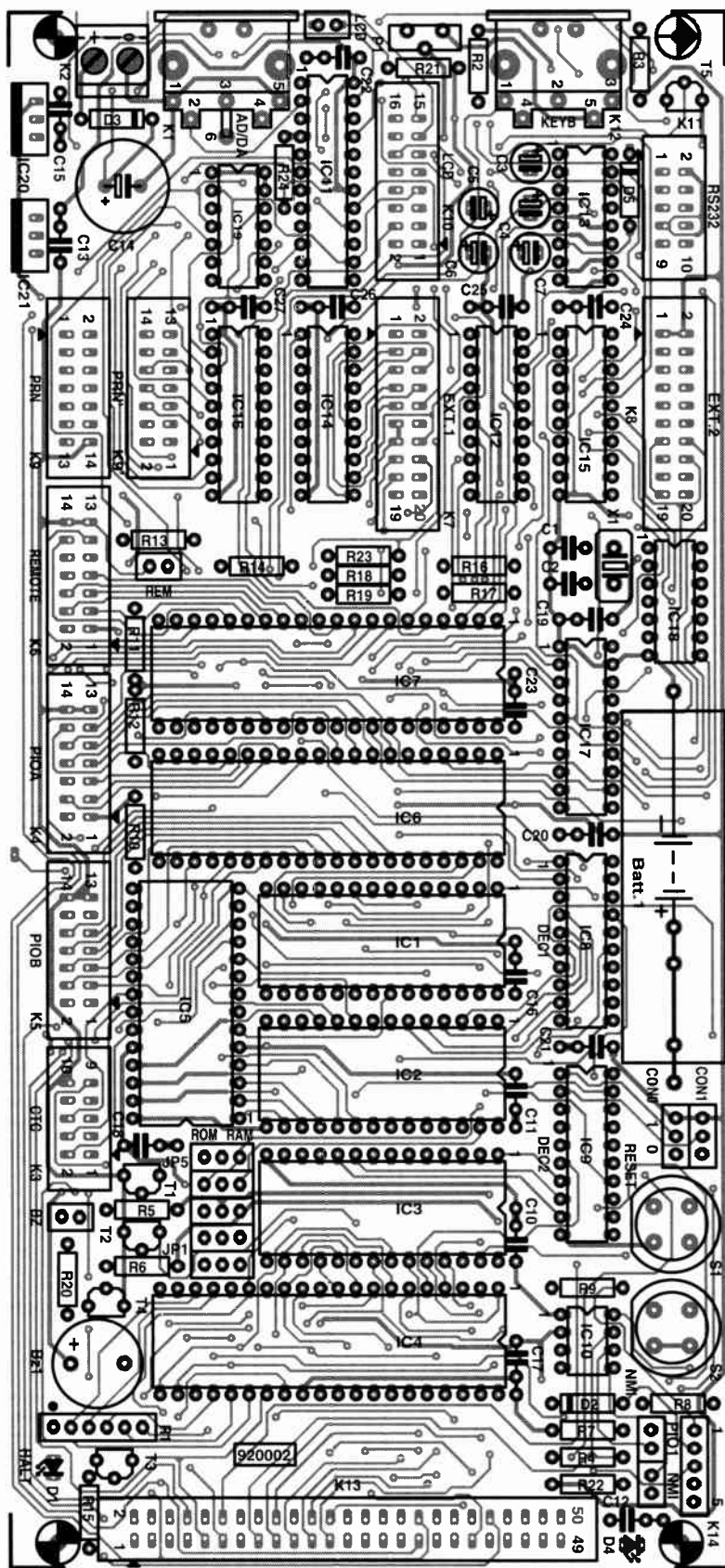


Fig. 17c. Component mounting plan.

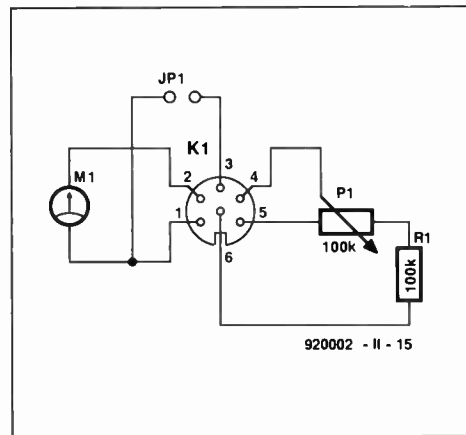


Fig. 18. ADC/DAC test circuit.

returned to the start of the test routine. This allows you to run the test repeatedly, which is useful when errors are to be eliminated.

8. Fit IC14 and IC15. Since the use of the external buses EXT1 and EXT is application-dependent, no provision is made to test them.

That concludes the test procedure. Depending on the application of the Z80 card, you may wish to fit it in an enclosure (as we did — see photographs), or build it into the enclosure of an existing application. In either case, flatcables are a good way to ensure a well-finished product (Fig. 20), that is, a neat looking unit without a wire mess inside. The flatcables may be left relatively long to enable them to be folded and tucked under the PCB. Note, however, that IC socket pins can cause problems by piercing the insulation of the flatcable wires when the PCB is pressed too hard on the flatcable. These problems may be avoided by cutting the protruding parts of the IC socket pins with pliers. Even better, do this before soldering the pins: fit the IC socket, and secure it by soldering two diagonally located corner pins only. Next, cut the other pins to the minimum length. Soldering will then not present problems in any case because the PCB is through-plated.

Practical use

Having constructed the Z80 card, you are ready to concentrate on applications. Unless you have a fully working application program in EPROM, you will need an EPROM simulator and a Z80 assembler to be able to develop software. Suitable assemblers are, for instance, the X80 and X280 from 2500 A.D. Software Inc., 109 Brookdale Ave, Box 480, Buena Vista, CO 81211, U.S.A.

If you expect to exchange EPROMs frequently, it is worthwhile to invest in a ZIF socket. Do not solder this straight on to the board, but use two or three stacked, normal, sockets in between. This has the advantage of being able to unplug the ZIF socket later, and use it in another circuit (removing an IC socket from a double-sided board is fairly difficult).

The description of the BIOS on the disk supplied for this project is sufficiently detailed to use the file, or parts of it, in your own source code. In many cases, the infor-

ANALYSER III — A REVIEW

by Mike Wooding G6IQM

ANALOGUE circuit design is traditionally difficult because all designs have to be tested to confirm that they work as desired. Even more difficult is the ability to conduct the sheer infinite number of tests over the full frequency spectrum that the design is intended to work over. Furthermore, the time spent on building bread-boarded prototypes to conduct the tests on is pretty expensive in most cases. One way to cut on development costs is to use a computer simulation of the design, and analyse its performance in theory before anything is built. Fortunately, computer programs to do this have descended from 'higher spheres' to a level where one encounters the intrepid hobbyist.

Analyser III is a fast, advanced and easy to use Linear Analogue Circuit Analysis program. The package allows electronic designs to be tested without soldering a single component and, often more important, without the need for expensive test equipment. The circuit design can be tested on a PC and modifications made until the circuit functions as required all without using a soldering iron in anger, or blowing up any expensive devices.

The system is ideal for the analysis of filters, amplifiers, cross-over networks, wideband amplifiers, aerial matching networks, radio and TV IF amplifiers, chrominance filters, linear integrated circuits, etc. Analysr III also has advantages over physical test equipment in that it allows analysis over a frequency range from 0.001 Hz to 999 GHz, showing gain, phase, group delay, and input and output impedances.

ANALYSER III

Analysr III is a linear analogue circuit analyser program that runs on PC/XT/AT/286/386/ or 486 computers running under MS-DOS 3.0 or later (also DR-DOS 5 and 6) and with either EGA or VGA graphics, preferably colour. The minimum RAM requirement is 512 Kbytes, and the software is supplied on both 5.25" and 3.5" format floppy disks.

Like almost any circuit analysis program, Analysr II keeps a high proportion of its temporary data on disk during operation. Consequently, when using a floppy



only based machine, Analysr III will be very sluggish.

The program also supports the use of a mouse, although the software is easy to use via the keyboard, and a choice of either 9 or 24-pin dot-matrix printers or HP Laserjet II printers.

The user manual

The comprehensive user manual is packaged in an A5 ring binder, which allows the easy insertion of upgrade instructions, personal notes, etc., and follows the well established pattern of Number One Systems' program documentation (see photograph). The first few pages of the manual deal with an overview of Analysr III, the installation and running of the program.

The next section in the manual is called 'First Impressions' and gives an outline of the screen presentations and some of the basic commands used to manipulate these screens and move around in them. Once the user is familiar with these basic commands, it's on to the next section, 'The Grand Tour'.

'The Grand Tour' comprises the greater part of the user manual and takes the user through a step-by-step simulation; from entering the initial design netlist to the final proven circuit. To assist with the instruction, a pre-designed simple passive twin 'T' notch filter circuit is used as a practical example, from which a netlist is

composed.

A netlist is a file of connections between the various components within the circuit, their values and any other associated parameters, such as small-signal gain (h_{fe}) or transition frequency (f_t), for example, for a bipolar transistor. The libraries supplied within Analysr III contain ready-made netlist outlines for many basic circuit structures and various popular bipolar and FET transistors, opamps, etc.

After the comprehensive chapter dealing with netlist editing and production, the next section in the manual tackles the actual operation of the analyser. To begin with, you need to select the input and output connections. Next, Analysr III calculates and displays the frequency and phase response curves of the circuit. Initially, the display defaults to a frequency range of 1 kHz to 1 MHz, but this range, and any other of the display parameters,

can be changed simply by a few clicks of the mouse button or keyboard presses, which are explained in detail in the next section of the manual.

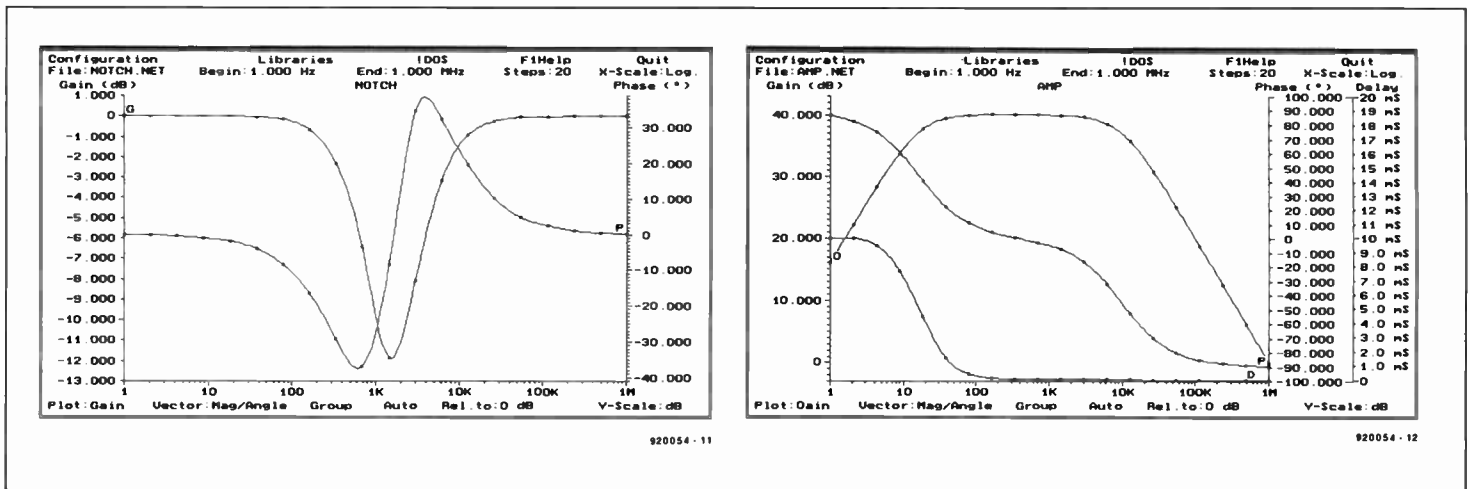
The 'Grand Tour' then continues with the various different displayed parameters available, such as group delay, vector selection, scaling the various plots, including offsets in the analysis, using the display grids and tabulating the results.

The remaining sections of the user manual deal with printing out the plots, converting circuits to single components for inclusion in more complex circuits (e.g., using the notch filter in the feedback loop of an amplifier) and adding them as library entries, using the libraries, customising Analysr III to your exact requirements, using the DOS browser and, finally, a list of the built-in library component entries is given.

The analyser

Once a circuit netlist has been created and the input, output and ground connections established, Analysr III simulates the circuit operation and displays on the screen a plot of the frequency and phase versus gain such as one would see displayed on a circuit analyser or spectrum analyser, but only after the circuit had been built.

The 'tilde' key (~) will trigger a printout of the current screen (including any menus, etc.) in 'extra' dot-matrix, Laserjet



or GEM format, as defined in the Configuration menu.

The display screen is divided into three main areas. The top of the screen contains the main menu, showing Analyser III's top-level commands, with the currently active mode highlighted. The program defaults to the analyser mode on start-up. The other modes are:

Configuration	Customises Analyser III
Libraries	Maintains Component libraries
!DOS	Manipulates Files and Directories
F1	Help (on-line help information)
Quit	Leave Analyser III

Also shown in the menu area are the file name of the circuit currently being analysed, the frequency limits of the analysis, the number of steps in the analysis and whether the scales are logarithmic or linear.

Configuration:

This command selects a set of menus which allow the default parameters for Analyser III to be set according to the user's choice. The default search paths for files, the time and date format, etc., can all be preset by the user, and the configuration saved.

Libraries:

The library command allows the various libraries to be scanned and manipulated.

!DOS:

Selecting this command displays a menu of basic DOS commands which are available for use without leaving Analyser III. Also selectable is a DOS Shell, which allows you to exit Analyser III to the DOS prompt, but without losing any data currently held in Analyser III. Quitting the DOS Shell returns you to Analyser III, exactly where you left it.

F1 (HELP) and **QUIT** are self-explanatory.

The main area of the screen is devoted to the analyser display with the moveable cursor.

At the bottom of the screen is a sub-menu of control commands for the different plots, a display of the relative level of the plot and the scaling factor for the Y axis.

With Analyser III the only limitation to the frequency range of the analysis is that it lies within the limits 0.001 Hz to 999 GHz! In other words, just about any circuit that you care to analyse can be accommodated within Analyser III's capabilities. Having spent most of my working life in electronic test laboratories, I think I can safely say that I do not know of any circuit or spectrum analysis equipment that will directly look at frequencies much above 100 GHz, let alone 999 GHz! The usual way to perform such tests is to down-convert the final signal before conventional display analysis, and that system has all sorts of inherent inaccuracies present. Also, it would have to be 'normalised' to eliminate the effects that the down-conversion has on the display. Finally, the circuit has to be prototyped and built before such analysis can take place.

The libraries

As I mentioned earlier, there are inbuilt libraries in Analyser III, which make the creating of netlists much quicker. The libraries are:

1. PRIM.ALB: a library of all the basic device models.

2. DEVICE.ALB: this library contains a selection of 'real' device models. All the components in this library are made up from the primitive elements in the PRIM.ALB library with the appropriate parameters set. As there are many thousands of different devices, and every engineer has his/her particular favourites, this library is really intended as a set of examples to help the user create his/her own personal set of libraries.

After building up netlists for a circuit, and subsequently naming the component

type being used, Analyser III responds by reading the pin and parameter information from the library for the device. All you have to do is enter the various connection details.

Circuit blocks previously designed and tested can be added to the libraries, which is very useful if you require a particular circuit, or part of a circuit, more than once.

Conclusions

After having familiarised myself a little with the concept of a netlist, I successfully created the one for the example circuit. Following the instructions I then connected my inputs and outputs, and Analyser III analysed the circuit and presented the plots on the screen.

It soon became evident to me that the facilities available are quite extensive. Using conventional circuit and spectrum analysers often as I do, I can imagine that in a development environment Analyser III would be far more ideal. The fact that a design circuit does not actually have to be built would be one great advantage. That, coupled with the ability of Analyser III to analyse the circuit over as wide a frequency spectrum as you like, plus the ability to change devices in the circuit for re-analysis, could prove a great boon to circuit designers.

I can heartily recommend Analyser II to anyone engaged in linear circuit design and testing work. This software enables a designer to test a circuit ideally up to the production stage, without even raising a soldering iron in anger and committing any devices to the breadboard, or dustbin! ■

I wish to thank Mr. Espin and the staff of Number One Systems Limited for their help and advice, and for the review software.

ANALYSER III costs US\$375 (delivered), with manual, 5¼ and 3½" disks. Send checks to Number One Systems, 1795 Granger Ave., Los Altos CA 94024 (CA add tax). Send credit card orders by mail or FAX to Number One Systems, Harding Way, Somersham Rd., St. Ives Cambs England PE17 4WR, UK. Tel: 011-44-480-61778; FAX: 011-44-480-494042. Orders ship within 24hrs of receipt.

8051/8032 ASSEMBLER COURSE

PART 4: FLAGS, BIT ADDRESSING, PSW, CONDITIONAL JUMPS, LOGIC OPERATORS

By Dr. M. Ohsmann

In this instalment of the course we will deepen our knowledge of the 8051 instruction set, and also get to grips with the concept of bit addressing. The new instructions allow programs to be written with 'real world' applications such as the control of a small servo motor in a model boat, and outputting an analogue voltage. Both applications make use of the hardware extensions described in last month's instalment.

Flags and bit addressing

It is often required for a program to wait for a certain signal to change state, which is called a condition. Such a conditional signal may be supplied by an external source, for instance, the output of a comparator, which is connected to an input port line. It may, however, also be internal, i.e., a bit or a flag, for instance, bit 3 in the accumulator (written as ACC.3). The 8051 family of microcontrollers offer a number of instructions for bit addressing and logic bit manipulation (for instance, an OR function) that allow bit states (0 or 1) to be evaluated in a simple way.

The microcontrollers in the 8051 series can address 256 bits in the range 000H to 0FFH. As with direct addressing, the function of the addresses smaller than or equal to 127 is different from those greater than 127. The addresses from 0 up to and including 127 are used to address bits in the internal RAM. Bit address 0 corresponds to bit 0 of the byte at address 20H in the internal RAM. Likewise, bit address 127 corresponds to bit 7 of the byte at address 2FH in the internal RAM. Hence, the 16 bytes 20H to 2FH of the internal RAM store bits 0 to 127 (see Fig. 5 in part 1 of the course).

Bit addresses 128 to 255 enable bits in the special function registers (SFRs) to be addressed. The effective bit address is the sum of the SFR address and the bit number to be addressed. Thus, bit address 0E3H is used to address bit 3 in the accumulator (SFR 0E0H). The assembler used during this course does all the adding automatically if you use the so-called point nota-

Bits (flags) in program status word (PSW)

CY	PSW.7	Carry Flag	:	carry (overflow) flag, bit accumulator C
AC	PSW.6	Auxiliary Carry	:	aux. flag for BCD applications
FO	PSW.5	FLAG0	:	available for general applications
RS1	PSW.4	Reg. bank select 1	:	selects register bank; bit RS1
RS0	PSW.3	Reg. bank select 0	:	selects register bank; bit RS0
OV	PSW.2	Overflow	:	overflow flag
	PSW.1		:	available for general applications
P	PSW.0	Parity	:	parity in accumulator

Register bank selection

RS1	RS0	Register bank	Addresses in internal RAM
0	0	0	00H - 07H
0	1	1	08H - 0FH
1	0	2	10H - 17H
1	1	3	18H - 1FH

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Fig. 13. Function of the flags contained in the PSW (program status word).

tion, which means that a point is inserted between the SFR and the bit number. For example:

```
JB ACC.3, THERE ;jump to THERE
                  when Accu bit 3
                  is set
```

Note, however, that this requires an EQU statement for the accumulator SFR address to be assigned to constant 'ACC'.

Only those SFRs whose address ends with three '0' bits are bit addressable; these are the SFRs marked with an asterisk (*) in Fig. 8 (see part 2).

Instructions that change flags

MNEMONIC	C	OV	AC
ADD	x	x	x
ADDC	x	x	x
SUBB	x	x	x
MUL	0	x	
DIV	0	x	
DA	x		
RRC	x		
RLC	x		
SETB C	1		
CLR C	0		
CPL C	x		
ANL C,bit	x		
ANL C,/bit	x		
ORL C,bit	x		
ORL C,/bit	x		
MOV C,bit	x		
CNJE	x		

x = flag changed
 1 = flag set
 0 = flag reset
 /bit = inverted bit combined

Note: flags also changed by writing to SFR address 0D0H.

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Fig. 14. Overview of MCS51 instructions that change the flags in the PSW.

Program status word (PSW)

The program status word, PSW, is stored at SFR address 0D0H in the 8051. The PSW contains bits (flags) that indicate, for instance, whether or not a carry has occurred as a result of a subtraction. This information is stored in bit 7, and can be accessed via bit address PSW.7. This bit, which is also called the C-Flag, can be addressed via many bit manipulation instructions. Since it contains the result of logic bit combination operations (OR, AND and NOT), the C-flag thus forms a kind of one-bit accumulator for bit manipulation.

The parity bit, PSW.0, is set when the accumulator contains an odd number of ones. The flags OV (PSW.2) and AC (PSW.6) have checking functions when signed numbers (e.g., BCD numbers) are used. Bits 3 and 4 in the PSW allow the programmer to determine which register bank is addressed. Since only bank 0 is used during this course, these bits should not be changed. Bits 1 and 5 are free for general use and may be set and interrogated as required.

Figure 13 shows an overview of the bit functions and identifications, and Fig. 14 a list of instructions that change the flags in the PSW.

Conditional jumps

Conditional jump instructions are used to perform certain functions in a program, depending on the state of certain external signals or occurrences. The conditional jump is made when the relevant condition set up by the instruction is fulfilled. If the condition is not fulfilled, the program simply continues with the next instruction. Practical examples of the use of conditional jumps may be found in XAMPLE06.A51 and XAMPLE07.A51 on your course disk. The respective list files are given in Figs. 20 and 21. The microcontrollers in the MCS-51 series offer the following conditional jump instructions:

JZ	addr	;jump to addr if accu=0
JC	addr	;jump to addr if carry flag (PSW.7) is set
JB	bit,addr	;jump to addr if bit at bit address is 1
JBC	bit,addr	as JB, but clear bit

The first three of these instructions are also available in the form of a negative condition, marked by a preceding 'N'.

Conditional jumps are 'short' jumps, i.e., they can be used for an address difference within the range +127 to -128

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What you need to follow this course:

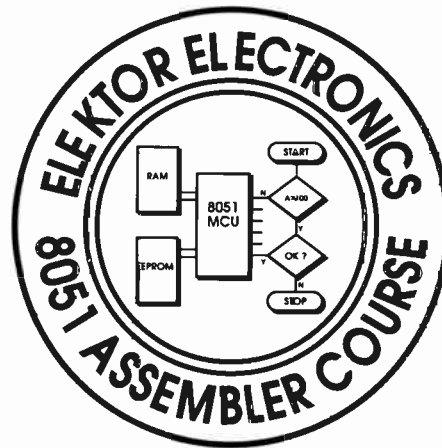
- a **8032/8052AH-BASIC single board computer as described in Elektor Electronics May 1991. The preferred CPU is a 8051 or 80C32. Alternatively, any other MCS52-based microcontroller system (but read part 1 of the course);**
- a **course diskette (IBM: order part number 1661; Atari: order part number 1681) containing programming examples, hex file conversion utilities, and an assembler;**
- a **monitor EPROM (order part number 6091);**
- an **IBM PC or compatible operating under MS-DOS, or an Atari ST with a monochrome display.**

Appeared so far;

Part 1: Introduction (February 1992)

Part 2: First 8051 instructions (March 1992)

Part 3: Hardware extensions for 80C32 SBC (April 1992)



(refer back to 'SJMP' in part 2). Because of this, it may be necessary to conditionally jump to a 'long jump' instruction.

Compare instruction

The 'compare' instruction of the 8051 takes the form of a conditional jump:

CNJEop1,op2,address ;jump to address if
op1 is not equal
to op2

The operands that may be used are given in the instruction set overview. This instruction is particularly useful to direct the program flow depending on whether a certain

register contains a predetermined value.

Count instruction DJNZ

Wherever program loops are used, and the number of iterations is between 1 and 255, the command

DJNZRn,rel

may be used. The DJNZ instruction first decreases the contents of the indicated register by one. Next, a check is made to see if the register content is nought. If not, the program continues with the instruction at the indicated jump address, 'rel'; else, the next instruction is fetched. As shown in the instruction set overview, it is possible to use a directly addressable byte instead of a register.

For a practical example of the use of the DJNZ instruction, refer to XAMPLE06 on your course disk. This illustrates how a time delay is created. First, a register is loaded with a value that indicates the length of the delay. Next, a few 'idle' commands are executed before the loop is started again with the DJNZ instruction. The value loaded into register R1 determines how many times the loop from line 29 to line 33 is repeated. Since each of the instructions inside the loop takes 10 μ s to complete (see the 'T' column in the .LST file), the loop 'WAIT' creates a delay of about 10 times R1 microseconds. Not exactly 10R1 μ s, because time taken by the ACALL, RET, CLR and SETB instructions should be added. These increase the actual pulse length by about 5 μ s.

Logic combinations

The MCS-51 microcontrollers offer the following instructions to perform logic combinations: OR, AND and XR (exclusive OR). The logic combination comprises all bits of both operands. They are:

ANL target,source	;target replaced by (target AND source)
ORL target,source	;target replaced by (target OR source)
XRL target,source	;target replaced by (target XOR source)

Again, the possible operands (source and target) are taken from the instruction set overview. Assuming, for instance, that the accumulator contains the value

10010111B = 97H = 151,

and register R0 the value

11110010B = F2H = 242,

the logic operators give the following results:

Instruction	ANL A,R0	ORL A,R0	XRL A,R0
A before:	10010111	10010111	10010111
R0 before:	11110010	11110010	11110010
A afterwards:	10010010	11110111	01100101

The ANL instruction may be used, for instance, to reset (clear) certain bits in a byte, without changing the others. Likewise, the ORL instruction is used to set certain bits. The setting or resetting of certain bits in a byte is called masking. This technique is used, for example, to check if one of the bits 0, 1 2, or 7 in the accumulator is set, as shown in the programming example

```
ANL A,#10000111 ;mask bits 7, 2, 1 and 0
JNZ set ;A not 0 when one of these bits is set
```

The operation of the related instructions

```
CLR A ;clear accumulator
CPL A ;invert bits in accumulator
```

speaks for itself.

Bit manipulation instructions

The bit manipulation instructions

```
CLR bit-operand ;clear bit
SETB bit-operand ;set bit
CPL bit-operand ;invert bit
ANL C,bit-operand ;C replaced by (C AND bit)
ORL C,bit-operand ;C replaced by (C OR bit)
MOV bit,operand,C ;bit replaced by C
MOV C,bit-operand ;C replaced by bit
```

allow single-bit manipulations to be carried out on bytes. Their usage is similar to that of the logic manipulations. The C-bit (bit 7 in the PSW) is used as a result register. The bit manipulations are often used to set or reset single bits, for instance, of an output port, without affecting the state of the others.

Testing a servo motor

The function of the program given in the assembly file XAMPL06.A51 is to gener-

ate pulses to control a servo motor that operates the rudder in a remotely controlled model boat. Fig. 15 shows the timing of the pulses involved. As you can see, it is required that the program generates 'short'

pulses of 800 μs when push-button 'A' is pressed, and 'long' pulses of 1600 μs when push-button 'B' is pressed. These pulse lengths result in the rudder being turned to the left and the right respectively. To keep the rudder fixed in the centre position (i.e., to make the boat sail straight on), the program generates pulses with a length of 1200 μs. The pulses are separated by 10-ms long pauses.

For this example application we make use of the hardware extensions described in last month's instalment. Push-buttons 'A' and 'B' are realized with the aid of

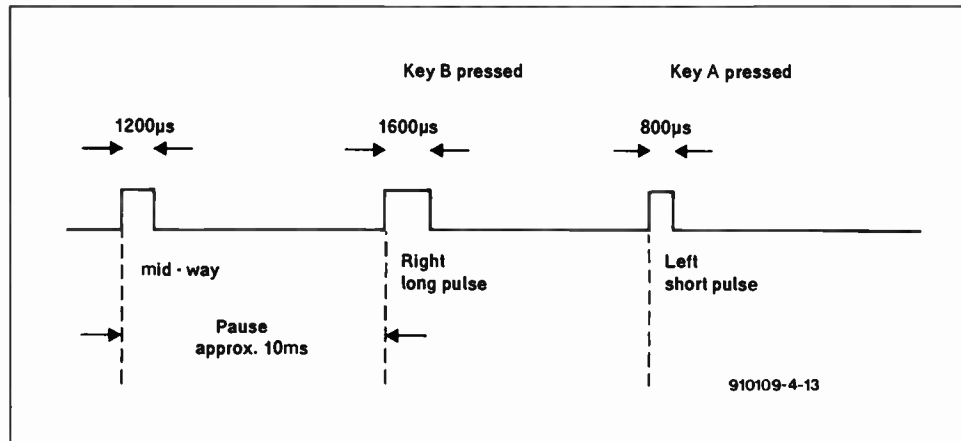


Fig. 15. Pulses used to control a small servo motor.

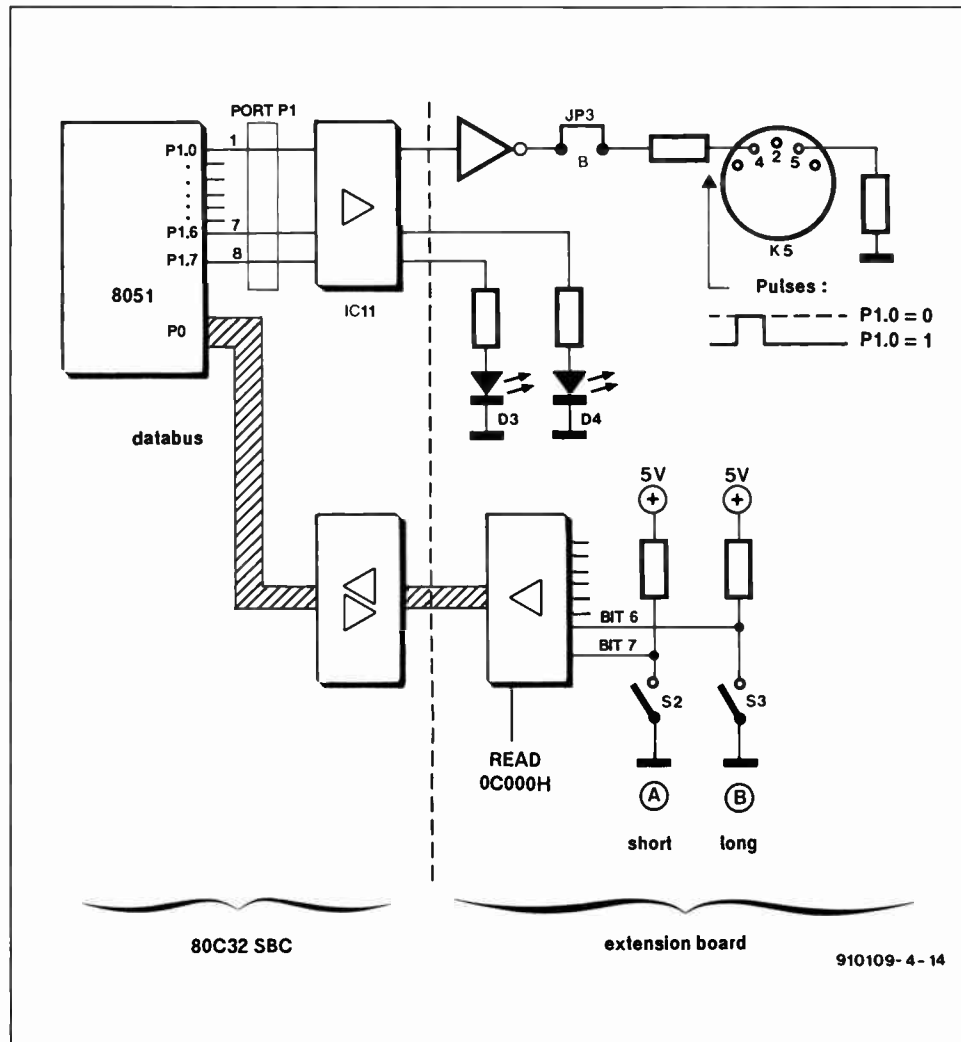


Fig. 16. Signal flow in the pulse generator.

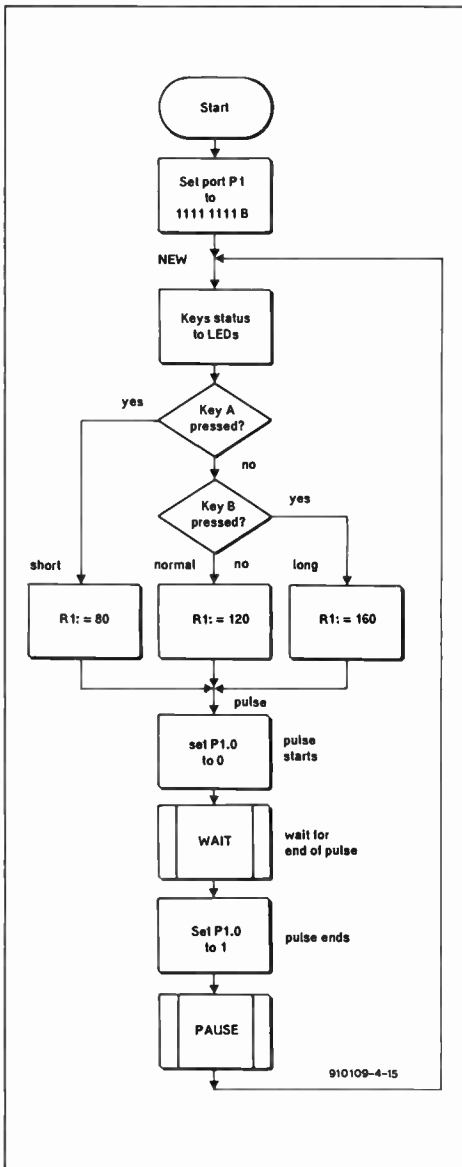


Fig. 17. Flow diagram of the pulse generator program.

switches S2 and S3 respectively. The status of these keys can be interrogated via address 0C000H (access to memory mapped I/O in external RAM). The pulses are to be output via pin 4 of the MIDI socket, K5. This requires jumper JP3 to be set to position 'B'. Because of inverter IC4c on the extension board, a '0' sent to port P1.0 results in a 'high' level at socket K5. The simplified system diagram is shown in Fig. 16, and the flow diagram of the control program in Fig. 17. The listing of the actual assembly-language control program is given in Fig. 20.

After the initialisation of port P1, the program enters an endless loop at label 'NEW'. First, the status of the keys is read and indicated on the LEDs connected to port P1. The ORL instruction in line 14 ensures that the pulse output bit, P1.0, remains 'one'. Lines 16 and 17 illustrate the use of the conditional jump instructions discussed above. Here, the JNB instruction is used in combination with bit-addressing of the accumulator to determine the status

of the push-buttons. If push-button 'A' is pressed, bit 7 in the accumulator has a '0', which sets up a condition evaluated by line 16.

Depending on which push-button is pressed, the value written into register R1 indicates the length of the individual pulse. In line 23, the output bit, P1.0, is set to '0'. This causes the MIDI output to go high (positive), and the pulse starts.

The subroutine 'WAIT' called in line 24 provides the delay that determines the pulse length. When the required time has elapsed, the pulse is ended with the aid of the instruction in line 25. The previously discussed bit manipulation instructions are used to set and reset the output bits.

Next, a pause of about 10 ms is created by calling subroutine 'PAUSE'. When the pause has elapsed, the program jumps to 'NEW', and starts again.

The two timing loops in the program (one for the 'mark' time and one for the 'space' time) are implemented with the aid of the DJNZ instruction.

If you do not have a servo, it is, of course, possible to test the program by connecting pin 4 of K5 to an oscilloscope. A small modification will enable the program to be used as a simple sound generator. All that is required is to change line 36 into

```
MOV R2,#1
```

and change bit P1.0 into bit P1.1 in lines 23 and 25. This causes the loudspeaker (connected to P1.1) to produce a sound of which the frequency depends on the push-button pressed.

It goes without saying that the above changes to the program can be taken further by those of you who want to generate

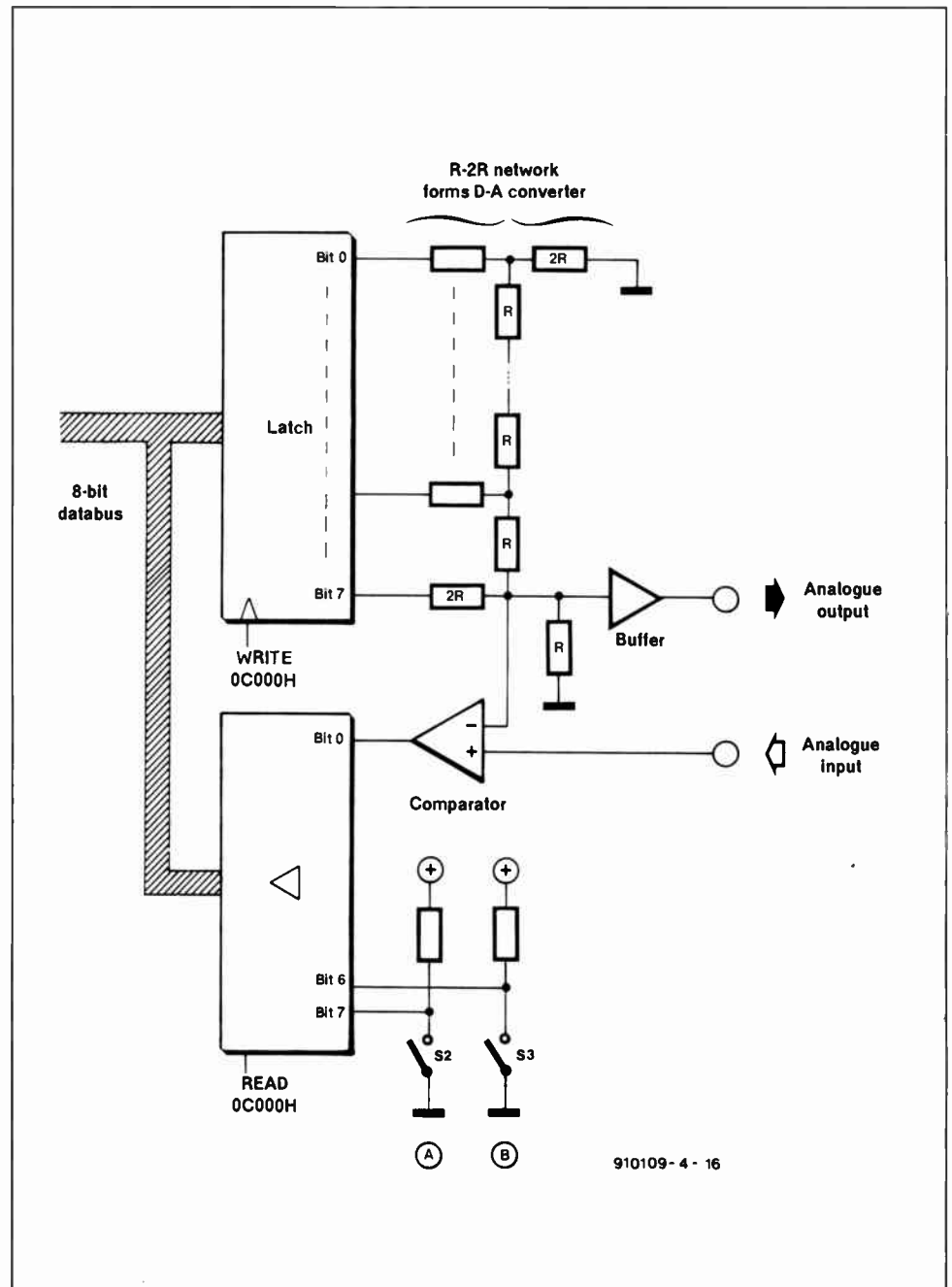


Fig. 18. Basic connection of the D-A converter to the 80C32 single-board computer.

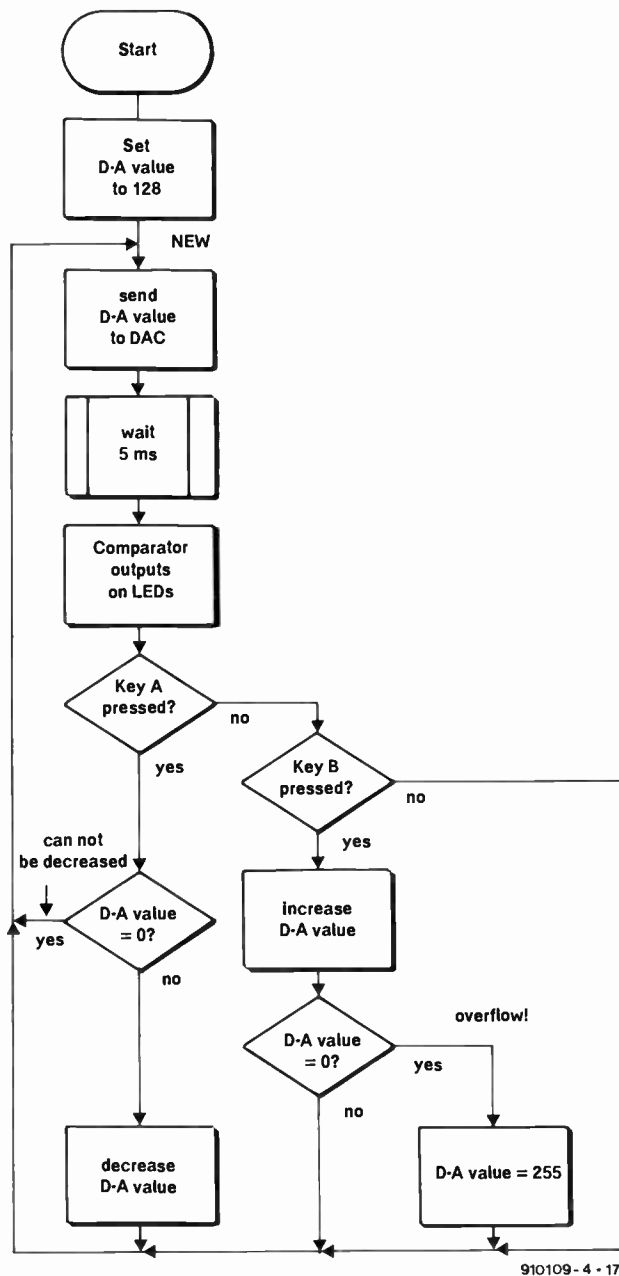


Fig. 19. Flow diagram of the D-A converter output routine.

signals with a specific pulse length or pulse order. The first step towards a programmable pulse generator has been taken.

Counting

The following instructions are available to count within the range of one byte, i.e., from 0 to 255:

INC	Byte-operand	;increment byte by 1
DEC	Byte-operand	;decrease byte by 1
INC	DPTR	;increase 16-bit DPTR by 1

As usual, the byte-operands that may be used are given in the instruction set overview in part 2. The INC and DEC instructions do not change any of the flags, including the carry flag. Increasing the value 255 results in 0, and decreasing 0 results in 255. A simple application of the DEC and INC instructions may be found in XAMPL07.

The INC DPTR instruction is often used to implement successive addressing of tables in the program or data memory.

Testing the D-A converter

Fig. 18 shows the functional diagram of the digital-to-analogue (D-A) converter on the extension board. The output voltage of the *R-2R* ladder network is buffered at the analogue output, and also fed to the $-$ input of three comparators (the diagram shows only one of these). This set-up allows the

Below: One of our readers, Mr. W. Otten of Germany, sent us this photograph of his remote-controlled model truck 'loaded' with an 80C32 SBC, batteries and a number of home-made extension cards.



```

***** LISTING of EASM51 (XAMPLE06) *****
LINE LOC OBJ T SOURCE
1 0000 ; ***** FILE XAMPLE06.A51 *****
2 0000 ;
3 0000 ACC EQU 0E0H ; SFR address of accumulator
4 0000 P1 EQU 090H ; SFR PORT1 address = 090H
5 0000 KEYS EQU 0C000H ; keys address in external data MEM
6 0000 short EQU 80 ; short pulse 800 microsec.
7 0000 normal EQU 120 ; normal pulse 1000 microsec.
8 0000 long EQU 160 ; long pulse 1600 microsec.
9 0000 ;
10 0000 ; ORG 4100H ; program to run from 4100H
11 4100 75 90 FF [2] START MOV P1,#11111111B ; all port bits = 1
12 4103 90 C0 00 [2] NEW MOV DPTR,#KEYS ; keys address
13 4106 E0 [2] MOVX A,@DPTR ; read keys (bits 4,5,6,7)
14 4107 44 0F [1] ORL A,#00001111B ; set bits 0,1,2,3 to 1
15 4109 F5 90 [2] MOV P1,A ; LEDs correspond to keys, P1.0=1
16 410B 30 E7 07 [2] JNB ACC.7,KEYa ; key A = short pulse
17 410E 30 E6 08 [2] JNB ACC.6,KEYb ; key B = long pulse
18 4111 79 78 [1] MOV R1,#normal ; no key, normal pulse
19 4113 80 06 [2] SJMP PULSE ; do pulse
20 4115 79 50 [1] KEYa MOV R1,#short ; different length
21 4117 80 02 [2] SJMP PULSE
22 4119 79 A0 [1] KEYb MOV R1,#long ; different length
23 411B C2 90 [1] PULSE CLR P1.0 ; P1.0 goes low, MIDI goes high
24 411D 31 25 [2] ACALL WAIT ; wait for pulse length (R1)
25 411F D2 90 [1] SETB P1.0 ; end pulse
26 4121 31 30 [2] ACALL PAUSE ; 10 milliseconds pause
27 4123 80 DE [2] SJMP NEW ; and another round
28 4125 ;
29 4125 AF E0 [2] WAIT MOV R7,ACC ; subroutine R1*10 microsec
30 4127 AF E0 [2] MOV R7,ACC ; 2 microsec. each
31 4129 AF E0 [2] MOV R7,ACC ; get timing right
32 412B AF E0 [2] MOV R7,ACC
33 412D D9 F6 [2] DJNZ R1,WAIT ; R1 times 10 cycles of 1 microsec.
34 412F 22 [2] RET ; end of subroutine
35 4130 ;
36 4130 7A 0A [1] PAUSE MOV R2,#10 ; 10 milliseconds
37 4132 79 64 [1] PAUSE1 MOV R1,#100 ; equals 10*100*10 microseconds
38 4134 31 25 [2] ACALL WAIT ; wait 1000 microsec. here
39 4136 DA FA [2] DJNZ R2,PAUSE1 ; continue outer loop
40 4138 22 [2] RET ; End of subroutine
41 4139 ;
42 4139 END
***** SYMBOLTABLE (14 symbols) *****
ACC :00E0 P1 :0090 KEYS :C000 short :0050
normal :0078 long :00A0 START :4100 NEW :4103
KEYa :4115 KEYb :4119 PULSE :411B WAIT :4125
PAUSE :4130 PAUSE1 :4132

```

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Fig. 20. This program, contained on your diskette as XAMPLE06.A51, generates pulses for the control of a small servo motor.

```

***** LISTING of EASM51 (XAMPLE07) *****
LINE LOC OBJ T SOURCE
1 0000 ; ***** FILE XAMPLE07.A51 *****
2 0000 ;
3 0000 ACC EQU 0E0H ; SFR address of accumulator
4 0000 P1 EQU 090H ; SFR PORT1 Address = 090H
5 0000 KEYS EQU 0C000H ; keys address in external data MEM.
6 0000 DA_ADDR EQU 0C000H ; DA-converter address
7 0000 ;
8 0000 ; RAM
9 0000 DA_VALU EQU 050H ; reserve 1 byte at address 50H
10 0000 ; ; i.e. above loc. occupied by EMON51
11 0000 ; ORG 4100H ; program to run from 4100H
12 4100 75 50 80 [2] START MOV DA_VALU,#128
13 4103 NEW EQU S_
14 4103 90 C0 00 [2] MOV DPTR,#DA_ADDR ; address of DA-converter
15 4106 E5 50 [1] MOV A,DA_VALU ; get current value into accu
16 4108 F0 [2] MOVX @DPTR,A ; send to DA-converter
17 4109 90 00 05 [2] MOV DPTR,#5 ; wait 5 millisecs
18 410C 31 32 [2] ACALL TIME
19 410E 90 C0 00 [2] MOV DPTR,#KEYS
20 4111 E0 [1] MOVX A,@DPTR ; get comparators into bits 0,1,2
21 4112 C4 [2] SWAP A ; swap bits 0-3 with bits 4-7
22 4113 F5 90 [1] MOV P1,A ; send to LEDs
23 4115 E0 [2] MOVX A,@DPTR ; get key status
24 4116 30 E7 05 [2] JNB ACC.7,KEYa ; key A pressed?
25 4119 30 E6 0B [2] JNB ACC.6,KEYb ; key B ?
26 411C 80 E5 [2] SJMP NEW ; no key pressed, run again
27 411E E5 50 [1] KEYa MOV A,DA_VALU ; value must be lowered
28 4120 60 E1 [2] JZ NEW ; may be nought, then do nothing
29 4122 14 [1] DEC A ; lower
30 4123 F5 50 [1] MOV DA_VALU,A ; and store new value into internal RAM
31 4125 80 DC [2] SJMP NEW ; start again
32 4127 E5 50 [1] KEYb MOV A,DA_VALU ; fetch value from internal RAM
33 4129 04 [1] INC A ; increase
34 412A 70 02 [2] JNZ IS_OK ; okay when not 0
35 412C 74 FF [1] MOV A,#255 ; otherwise it was and is 255
36 412E F5 50 [1] IS_OK MOV DA_VALU,A ; store new value
37 4130 80 D1 [2] SJMP NEW ; and again
38 4132 ; MONITOR INTERFACE ; the usual...
39 4132 cclTIME EQU 021H ; MONITOR command, DPTR millisecs delay
40 4132 COMMAND EQU 030H ; MONITOR command memory location
41 4132 MON EQU 0200H ; MONITOR jump address
42 4132 ;
43 4132 75 30 21 [2] TIME MOV COMMAND,#cclTIME
44 4135 02 02 00 [2] LJMP MON
45 4138 END
***** SYMBOLTABLE (14 symbols) *****
ACC :00E0 P1 :0090 KEYS :C000 DA_ADDR :C000
DA_VALU :0050 START :4100 NEW :4103 KEYa :411E
KEYb :4127 IS_OK :412E cclTIME :0021 COMMAND :0030
MON :0200 TIME :4132

```

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Fig. 21. List file of XAMPLE07, a program that turns the 80C32 SBC into a programmable voltage source.

output voltage of the DAC to be compared to the voltage applied to inputs 1, 2 or 3. The function of program XAMPLE07 is as follows: generate an output voltage that can be increased or decreased by pressing push-button 'A' or 'B' respectively. In addition, show the status of the comparator outputs on the three LEDs.

Summarizing, the proposed system allows us to program an output voltage, and find out if this is greater or smaller than the voltages at the three comparator inputs.

The flow diagram of the program we have in mind is given in Fig. 19. The assembly language program (Fig. 21) has a couple of instructions that may be new to you. Also, internal RAM addressing is used for the first time. Let us have a look at the listing in Fig. 21. The current value of the voltage is stored at address 050H in the internal RAM. This address is assigned the label 'DA_VALU' in line 9. When the program starts, the voltage is set to 128 in line 12. In the loop that starts with the label 'NEW', DA_VALU, i.e. the value at 050H, is sent to the DAC (lines 14, 15 and 16). Next, the program waits 5 ms before sending the comparator output signals to the LEDs (lines 19 to 22). Lines 23, 24 and 25 serve to check if a key is pressed. If so, the program jumps to the corresponding subroutine, which causes DA_VALU to be increased (lines 32 to 36) or decreased (lines 27 to 31). In each subroutine provision is made to prevent the minimum value being decreased, and the maximum value being increased.

Assignment

On the basis of what you have learned so far, combine XAMPLE06 and XAMPLE07 in such a way that the position of the rudder (i.e., the length of the pulses generated by XAMPLE06) can be controlled with the push-buttons, just like the output voltage in XAMPLE07.

You may also have a go at outputting a sawtooth via the DAC, or any other waveform you find interesting. This will quickly take you to a level where you will start writing your own assembly language routines, however simple to start with.

Next time: the fifth instalment of the course will address the remaining arithmetical instructions. Based on that information, we will tackle methods of implementing simple calculations with the aid of the 8051 (calculations are often required to process measured values). Part 5 will also introduce some programming techniques, including those required for receiving and transmitting (MIDI) data via the serial interface.

ELEMENTS OF PASSIVE ELECTRONIC COMPONENTS

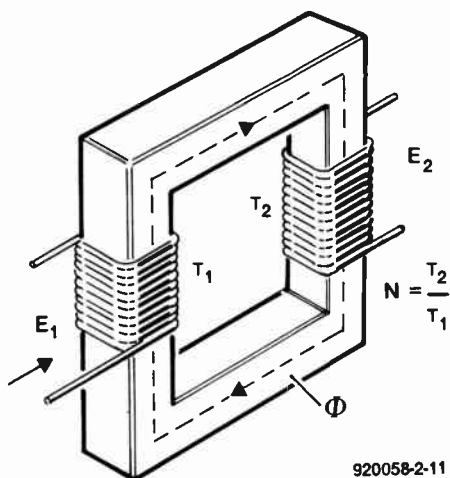
PART 2: THE IRON-CORED TRANSFORMER

by Steve Knight, B.Sc.

THE iron-cored power transformer is usually looked on as simply a device for raising or lowering the voltage of an alternating supply, with a corresponding decrease or increase in the current, but there is more to its functions in life than this simplistic view suggests. The transformer is an electromagnetic energy converter, whose operation is explainable in terms of the behaviour of a magnetic circuit excited by an alternating or changing current. As such, a brief review of its operational behaviour as a passive electronic component, is justified.

Faraday, in his experiments into mutual induction, which were described in the first part of this short series, used an iron-cored transformer that differed in construction from the toroidal forms we have today in nothing but possibly the technology of the core material. Essentially, in the construction of any transformer, there are two insulated windings wound upon a closed magnetic circuit of low reluctance: one winding is referred to as the primary (or input) coil, and the other as the secondary (or output) coil. In practice, there may be a number of output coils, but this does not affect the basic operational principles of the transformer. For clarity, Fig. 1 illustrates the input and output windings as being on separate limbs of the magnetic circuit, but however they are disposed, both windings are assumed to be linked by the same magnetic flux.

There is no direct connection between input and output; the transformer isolates one circuit from the other while allowing an exchange of energy between them. In addition, the transformer may be used to transform not only voltage and current, but also impedance, which enables the transfer of maximum power through impedance matching. Further, since



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Fig. 1. Schematic representation of transformer operation.

only alternating or changing current are transformed, the output circuit can be isolated from direct-current components in the input signal. All of these functions can be performed with high efficiency and precision.

For power applications, the frequency range of operation is in general 50–800 Hz, but special design refinements make the iron-core transformer of value over the audio range of 20 Hz to 25 kHz.

Voltage transformation

Because of the relatively large number of primary turns and the presence of the closed magnetic circuit, the self-inductance of the primary coil of a commonplace power transformer is large; and because of the tightness of the coupling between primary and secondary, the coils have a high mutual inductance. When the primary coil is connected to an alternating supply, the transformer will simply exhibit the characteristics of an iron-cored inductor. A current will flow and an alternating flux will be established in the core, a high proportion of which will link with the turns of the secondary. An e.m.f. of mutual induction will be set up in the secondary and, if the secondary circuit is completed through an external load, a current will flow in the load. Energy is, therefore, transferred from the input to the output circuit entirely by way of the magnetic coupling.

Assuming for the moment that we have a near-ideal component, the levels of the primary and secondary induced voltages, e_1 and e_2 respectively, will be proportional to the number of turns in the respective windings, since all the flux set up by the primary can be assumed to link with the secondary and is changing at the same rate, $d\phi/dt$, for both windings.

For a sinusoidal variation in the core flux of the form $\phi = |\phi| \sin \omega t$, the induced e.m.f.s are, from Faraday's law:

$$e_1 = T_1(d\phi/dt) = T_1 \omega |\phi| \cos \omega t = E_1 \cos \omega t$$

and

$$e_2 = T_2(d\phi/dt) = T_2 \omega |\phi| \cos \omega t = E_2 \cos \omega t,$$

where T_1 and T_2 are the turns in the primary and secondary winding respectively, and E_1 and E_2 are the r.m.s. values of the sinusoidal e.m.f.s. Hence,

$$e_2:e_1 = E_2:E_1 = T_2:T_1 = n$$

demonstrates that the ratio of the induced e.m.f.s is equal to the turns ratio, n . For $n > 1$, the transformer is a step-up, for $n < 1$, it is a

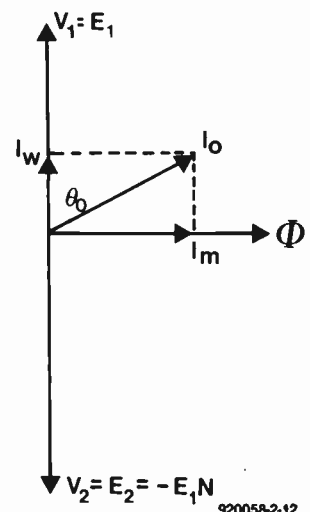
step-down. These terms are applied to the voltage transformation ratio.

In practical transformers, the terminal voltages, designated V , differ slightly from the induced e.m.f.s owing to the presence of effectual internal resistance in both the primary and the secondary coil; the terminal voltage ratio is, therefore, not the same as the turns ratio, but the difference can be considered as negligible for most applications.

The unloaded transformer

We have noted that when the secondary terminals of a transformer are open-circuit, the primary winding behaves as a large inductive impedance, through which a small no-load current, I_0 , will flow that lags the applied voltage, V_1 , by an angle θ_0 , which will be close to 90° . A component of this current will set up an alternating in-phase flux ϕ in the core that in turn produces primary and secondary e.m.f.s, E_1 and E_2 . There will be a hysteresis loss in the core when the flux is established and this loss will appear as heat, unaffected by the lamination of the core which is designed to reduce the other loss component, eddy currents. The no-load current, I_0 , must, therefore, contain an iron-loss component in addition to the true magnetizing component, I_m .

The phasor diagram for the unloaded transformer is shown in Fig. 2, where ϕ is taken as the reference phasor since it is common to the primary and secondary circuits. Ignoring the small difference between the applied voltage, V_1 , and the primary induced e.m.f., E_1 , the latter will be in anti-phase with the for-



920058-2-12

Fig. 2. Phasor diagram of the unloaded transformer.

mer. Further, the alternating flux that links with the primary turns and induces a back-e.m.f. of $-E_1$ volts also links with the secondary; consequently, there is induced in the secondary an e.m.f. E_2 that is in phase with the primary back-e.m.f. For a transformation ratio of n , therefore, $E_2 = -E_1 n$.

The two components of I_0 are $I_0 \sin \theta_0$ in phase with the flux, which is the magnetizing current I_m , a purely reactive component that is just sufficient to establish the flux; and the loss component, $I_w = I_0 \cos \theta_0$ in phase with the applied voltage. This component supplies the iron losses.

Under no-load conditions, the $I_0 R$ copper loss is very small and the overall losses are found in the iron circuit, so that I_0 is almost equal to I_m . Strictly, the magnetizing current is not sinusoidal for a sinusoidal input, since the $B-H$ magnetizing curve for the core material is non-linear, but for small I_m the phasor representation is perfectly valid.

What is important to appreciate at this stage is that, since the induced primary e.m.f. must depend on the magnitude of the alternating flux, it follows that this magnitude is determined *solely* by the magnitude of the applied primary voltage. Therefore, if V_1 is constant, ϕ is constant. This has two important consequences: ϕ must remain constant *irrespective* of any other currents that may be caused to flow in either the primary or the secondary winding when the transformer is loaded; and, on full load, the core flux is the same as on no load, so that the full-load iron losses are identical to the no-load iron losses. What does increase with loading are the $I^2 R$ copper losses in both windings. It can be demonstrated that the efficiency of the transformer is a maximum when the copper losses are equal to the iron losses.

The loaded conditions

In Fig. 3, the secondary terminals of the transformer are connected to a load that, as an example, is assumed to be a positive impedance (the most common circumstance). Ignoring the copper losses, the secondary terminal voltage, V_2 , will be identical to the secondary induced e.m.f., E_2 , and the primary applied voltage, V_1 , will be equal to, and in anti-phase with, the induced (back-)e.m.f. in the primary winding.

The induced secondary e.m.f., E_2 , will cause a current, I_2 , to flow through impedance Z_2 . This current will lag E_2 by an angle θ_2

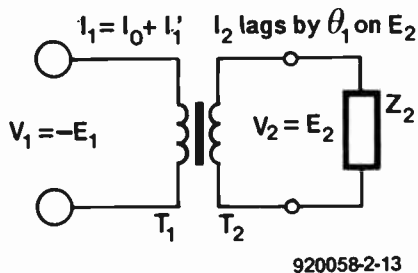


Fig. 3. Transformer operation with a complex secondary load.

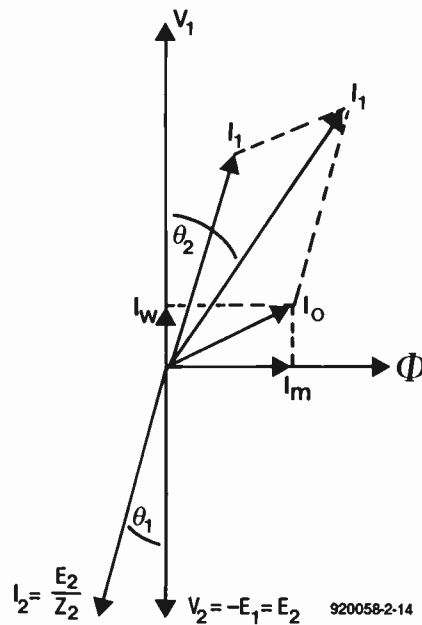


Fig. 4. Phasor diagram of the loaded transformer.

and will attempt to create a flux of its own in the transformer core. It is here that the constancy of the flux, ϕ , must be taken into account, since there has been no voltage change in V_1 . Some action must, therefore, take place to neutralize the effect of the secondary load current on the core flux; what happens is that a primary current flows of such a magnitude and phase the effect of the secondary current is nullified. The demagnetizing magnetomotive force, m.m.f., $I_2 T_2$ ampere-turns, is neutralized, in effect, by an additional primary current that increases the primary m.m.f. to $I_1' T_1 = I_2 T_2$ ampere-turns. Current I_1' is known as the balancing current and must, therefore, be 180° out of phase with I_2 and of such a magnitude that the total effective resultant flux introduced by the two currents is zero. This implies that the new effective m.m.f. must equal the m.m.f. caused by I_m alone, or,

$$I_m T_1 - I_2 T_2 + I_1' T_1 = I_m T_1,$$

so that,

$$I_1' T_1 = I_2 T_2,$$

or,

$$I_1' / I_2 = T_2 / T_1.$$

Notice that the current ratio $I_2 / I_1' = 1/n$. This accords with the well-known fact that a transformer converts a high-voltage, small-current power into a low-voltage, high-current one, and vice versa.

The phasor diagram for the loaded transformer under discussion is given in Fig. 4. For convenience and clarity, n is taken as 1. The total primary current, I_1 , is the phasor sum of the no-load current, I_0 , and the balancing current, I_1' , lagging the primary voltage by an angle θ_2 . In practice, I_1' is much larger than I_0 , and I_1' and I_1 can be looked on as being equal in magnitude. Angle θ_1

by which the secondary current lags the secondary e.m.f. is then practically equal to θ_2 . This means that the power factor is roughly the same for both the primary and the secondary winding and that the transformer does not to any great extent alter the phase relationship between current and voltage. Because, in practice, θ_2 is always slightly greater than θ_1 , the use of a transformer tends to decrease the overall power factor of a system.

Impedance transformation

When the primary current increases owing to the application of a secondary load, the primary impedance effectually falls. There is clearly a relationship between the load impedance and that seen at the primary terminals when such a load is connected.

In Fig. 5, suppose the secondary load impedance to be Z_2 ; the secondary e.m.f. will then be $E_1 n$ volts and the secondary current will be $E_1 n / Z_2$. The primary balancing current will consequently be $n(E_1 n / Z_2) = E_1 n^2 / Z_2$ and this will equal the primary current if the magnetizing current is small. Therefore, $I_1 = E_1 n^2 / Z_2$ and $E_1 / I_1 = Z_2 / n^2$. Thus, since $E_1 / I_1 = Z_1$, the impedance seen at the primary terminals is $Z_1 = Z_2 / n^2$.

For a step-up turns ratio, Z_1 will be smaller than Z_2 ; for a step-down ratio, Z_1 will be larger than Z_2 . Impedance is, therefore, transferred across the transformer from secondary to primary and is increased or decreased (from the primary viewpoint) according as the turns ratio, n , is (looking from the secondary side) up or down respectively.

The impedance matching abilities of a transformer have little relevance in power transformers, but are of importance in audio-frequency transformers.

Audio-frequency transformers

When a transformer is designed for a range of frequencies, unlike power transformers that are made for a single frequency, the equivalent circuit that the transformer presents to the input system is often quite different at one end of the range from what it is at the other. If a reasonably uniform response over, say, the audio-frequency range is desired, the transformer, including interstage types, output types, input matching devices, and so on, requires careful design considerations. In a practical transformer, there are a number of losses that may be represented as

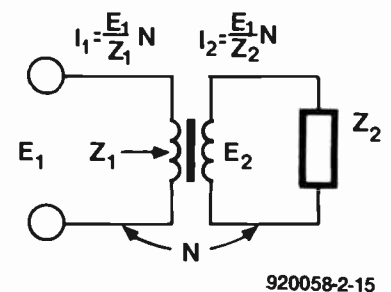
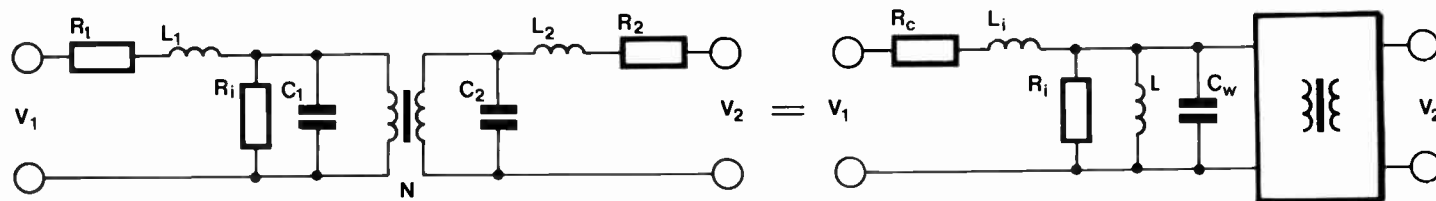


Fig. 5. The transformer used as an impedance transfer device.



920058-2-16

Fig. 6. Deriving the equivalent of a transformer model with losses isolated from an ideal device.

extra components added to the external circuits of an otherwise 'ideal' transformer, as illustrated in Fig. 6. The copper losses are shown as external resistances, R_1 and R_2 , in the primary and secondary circuits respectively; hysteresis and eddy current losses are represented by a parallel primary resistance, R_i ; flux leakages by series inductors L_1 and L_2 ; and the self-capacitances of the windings as parallel capacitors C_1 and C_2 . At power frequencies, the self-capacitances and the leakage inductances are not particularly important.

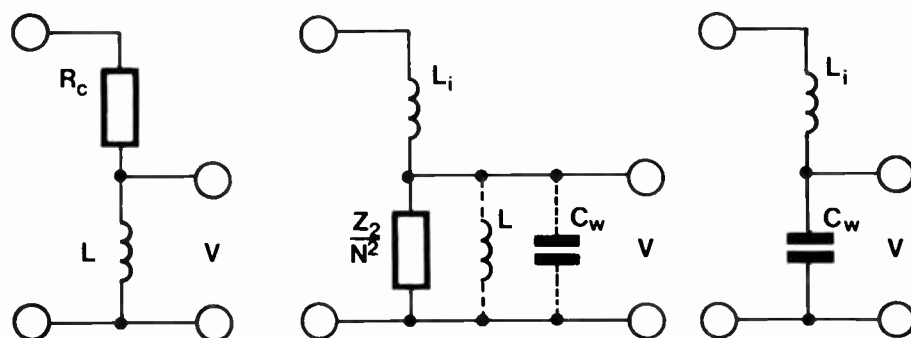
By transferring the secondary loss components to the primary circuit, the equivalent

model becomes as shown in Fig. 6(b), where R_c , the total copper loss, $= R_1 + R_2/n^2$; the total leakage inductance, $L_i = L_1 + L_2/n^2$; and the total effective winding capacitance $C_w = C_1 + C_2/n^2$. There is also L , the effective primary inductance with the secondary on open-circuit, such that $V_1/\omega L$ gives the magnetizing current. The remaining ideal transformer is then a component without the imperfections of the real device.

What happens to this model when it is used over the audio-frequency range? At very low frequencies, the input impedance will approximate that shown in Fig. 7, where the series inductance L_i is neglected along with

the shunt resistance and the winding capacitance, C_w . Hence, the ratio of the terminal voltage, V_1 , and the effective primary voltage V will be small, so the output voltage, V_2 , will be small. At some mid-frequency in the range, the transferred load resistance, Z_2/n^2 , will be very much larger than the resistance of L_i and there will be a tendency for C_w and L to resonate, so making the ratio V_2/V_1 approach n . At high frequencies, the shunt capacitance, C_w , has a low reactance relative to that of L_i and becomes dominant. This means that the response falls relatively rapidly.

The high-frequency response can be extended by sectionalized windings to reduce the self-capacitances and by getting the resonant condition to fall in the upper third of the range. In the same way, the low-frequency fall-off can be curbed by maintaining a high primary inductance (often achieved by barring direct currents from the winding) and by keeping the winding resistances small, though there is a conflict of requirements here. The choice of core material and thin laminations or ferrite is also important. ■



920058-2-17

Fig. 7. The simplified audio-frequency model.

Next month's final instalment of this short series will deal with the capacitor.

LOW FREQUENCY COUNTER

I obtained the PCBs for the low-frequency counter (January 1992, p. 42), but have difficulty in finding a supplier of the crystal-controlled programmable frequency pulse generator made by Seiko. I have tried RS Components, Cricklewood, STC, ElectroValue, and Seiko (UK) without success. In fact, Seiko (UK) says they do not stock it in the UK, but their German company might.

H.L. Gee
Sorking, UK

Editor replies:

We are surprised to learn that Seiko (UK) does not stock the SPG8650B, since at the time of accepting the article we were assured they would. We can only suggest that

LETTERS

you write to (or order from) Seiko Epson Europe BV, Prof. J. H. Bavincklaan 5, NL-1183, Amstelveen, The Netherlands; Tel +3120 547 5222, FAX +3120 452 295, or Seiko Instruments GmbH, Lyoner Strasse 36, W-6000 Frankfurt am Main 71, Germany; Tel +49 69 663 0000, FAX +49 69 666 7003.

UGQ5140K HALL POWER SENSOR

In the April 1992 issue you published an article on the "Lamp/Solenoid Driver UGQ5140K" Power Hall Sensor (pp. 56-57). Although the article was accurate, the source information was not.

On December 20, 1990, Sprague sold its complete semiconductor operation to Sanken of Japan. The new owners set up

the operation as a self-contained company with the name Allegro Microsystems, Inc. The address you gave was closed down in June 1992 and a new building was moved into, also in Concord, NH. For European users, our own address is suitable for contacting since the offices house sales and applications departments that can provide any assistance required.

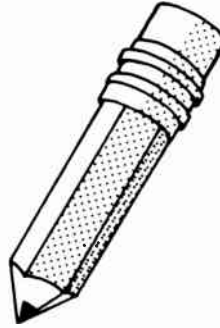
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Walton-on-Thames KT12 2TD
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Editor replies:

We apologize for this oversight and trust that this has not inconvenienced anyone. ■

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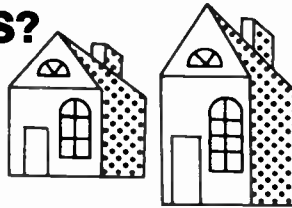
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This further volume in *Elektor Electronics' Microprocessor Data Book* series deals with general peripheral chips that, at least as far as their type-coding is concerned, do not belong to a specific family of microprocessors. There are so many of these, however, that only a portion of them can be dealt with in one book. Those contained in this collection have been chosen carefully on the basis of their practical application and frequency of use. Complete data are given for coprocessors from the 80 series (AMD, Cyrix, ITT, Intel, Weitek); real-time clocks from MEM, OKI, Statek, National Semiconductor, and Dallas Semiconductor; transmitters and receivers of serial interfaces RS232, 422, 423, 485 from Motorola, Newport Components, Maxim, Texas Instruments, National Semiconductor, Dallas Semiconductor, and Linear Technology; UARTS, DUARTS, and QUARTS (i.e., programmable ICs intended for data transfer); and the CS8221 set of ICs from Chips & Technology that are used in a great number of PC mother boards (also included is the data sheet of associated software LIM 4.0 for the management of the Extended Memory System).

Apart from the actual data, the book contains much other useful information, such as comparisons between and second sources for all important IC families; addresses of manufacturers and their representatives; and overviews of all peripheral chips (including many that could not be included in this book) that are available from various manufacturers.

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DATABOOK 5: APPLICATION NOTES

This book presents a series of application notes and design briefs that cover a wide variety of subjects. Apart from a number of applications related to specific components, the book also includes articles on basic design theory and the practical use of certain components. For example, there is an article reprint from Advanced Micro Devices that provides information on programming the motion of a stepper motor with the aid of a PAL (programmable array logic). Similarly, an article reprint from Motorola presents an overview of protocols and conventions used for serial communication between computers.

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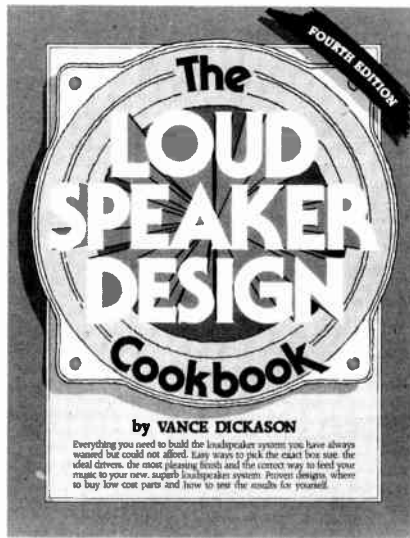
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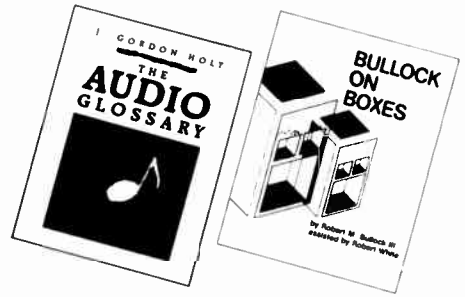
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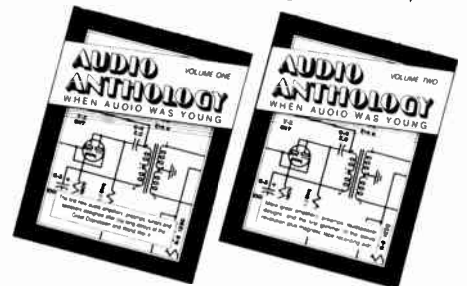
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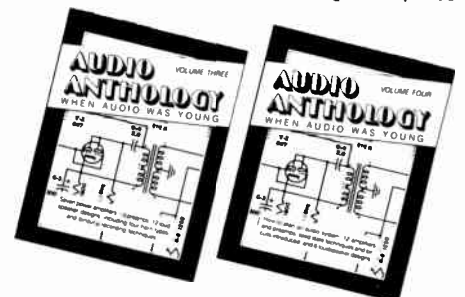
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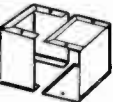
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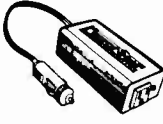
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