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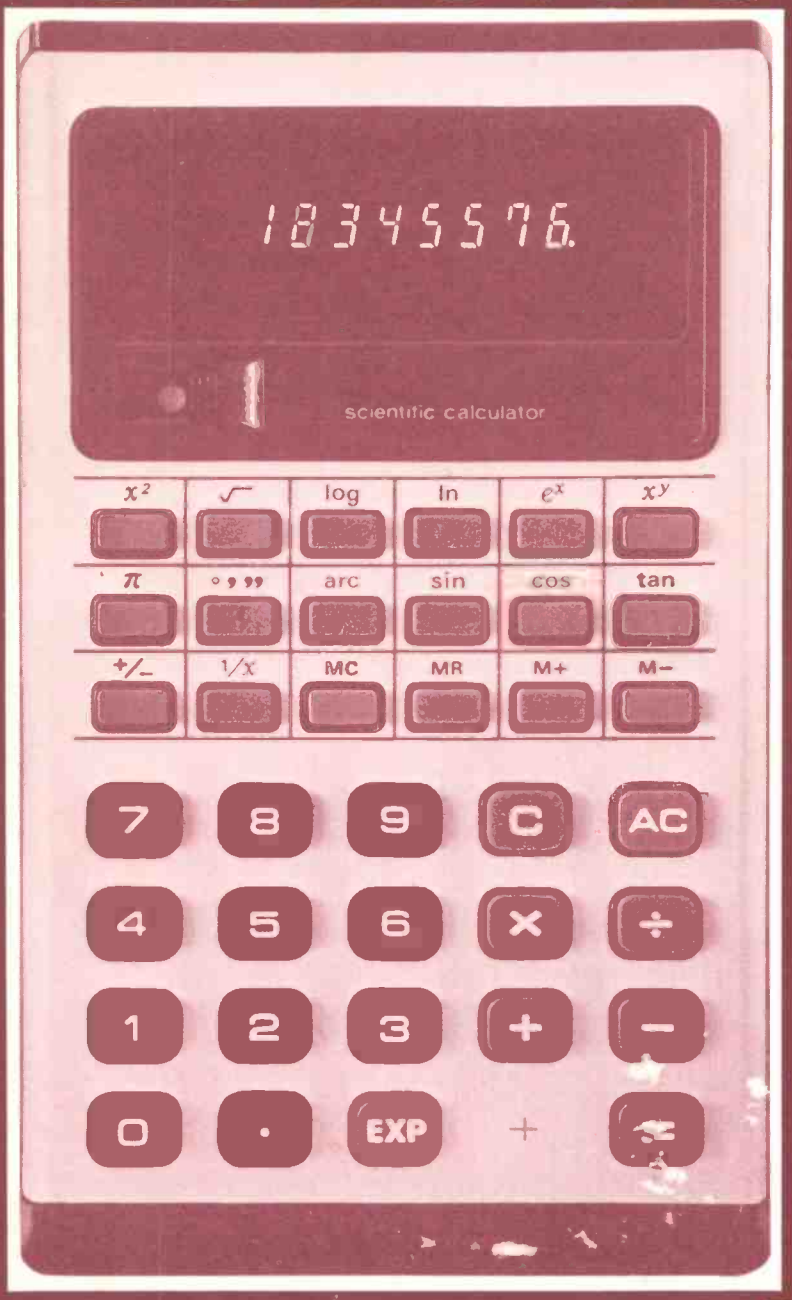
Electronics



DESIGNER'S CASEBOOK

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Electronics

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Automatic gain control quells amplifier thump

by Paul Brokaw
Analog Devices Inc., Semiconductor Division, Wilmington, Mass.

If an audio amplifier with automatic gain control makes a thumping noise when the input signal level changes quickly, the cause may be unwanted feedthrough of the gain control signal to the amplifier output. A simple solution is the addition of a resistor to prevent variations in the control voltage from being fed through to the output.

In the "thumpless" agc circuit of (a), transistors Q_1 and Q_2 form a differential amplifier that has a gain determined by the emitter current of the pair, I_E. This emitter current varies the transconductance and therefore the gain of transistors Q_1 and Q_2. But if gain changes too quickly, a thump may be heard. Inserting resistor R_1 in the emitter-current control circuit eliminates the thump.

Emitter current I_E is made nearly equal to the current (I_2) flowing through resistor R_2 by using identical same-substrate transistors for Q_3 and Q_4. When the base-emitter voltages of these two devices are equal, their collector currents (I_E and I_2) are also equal.

Since the base and collector of transistor Q_4 are shorted together, this device's base-emitter voltage will rise until its collector current becomes equal to $(1 - 2/\beta)I_2$, where β is the common-emitter current transfer ratio. Since transistor Q_3 is identical to transistor Q_4, Q_3's collector current will also rise to the same value. If current transfer ratio β is large and the reverse voltage feedback ratio of the transistor is small, Q_3's collector current (I_E) will nearly equal resistor current I_2. The value of current I_2 is:

$$I_2 = (E_{control} - V_{B4})/R_2$$

where V_{B4} is the voltage at the base of transistor Q_4.

Because the collector currents of transistors Q_3 and Q_4 are approximately equal, the transconductance of the differential pair (transistors Q_1 and Q_2) will vary in direct proportion to the control voltage. If Q_1 and Q_2 are identical, emitter current I_E will divide equally between them. Each transistor will have a collector current of $\alpha I_E/2$, where α is the common-base current gain.

If α is approximately equal to 1 and I_E is approximately equal to I_2, the collector currents of transistors Q_1 and Q_2 become:

$$I_{C1} = I_{C2} \approx I_2/2$$
$$I_{C1} = I_{C2} \approx (E_{control} - V_{B4})/2R_2$$

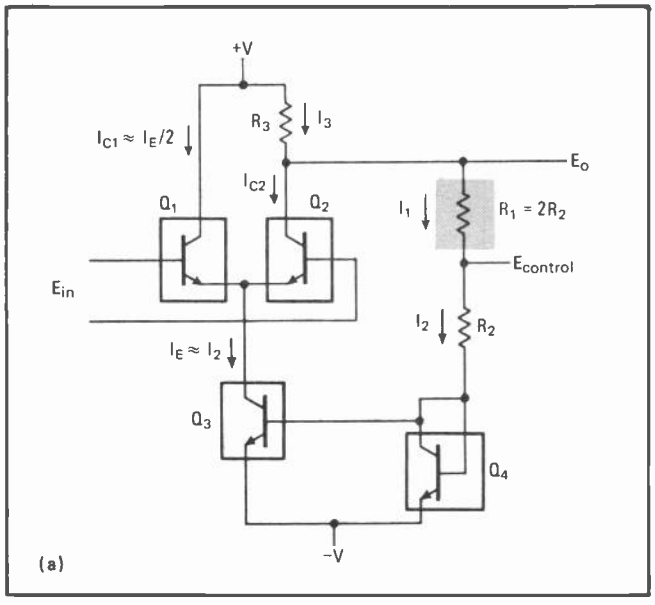
where I_{C1} is the collector current of transistor Q_1 and I_{C2} the collector current of transistor Q_2. The current (I_3) through resistor R_3 is due to both resistor current I_1 and collector current I_{C2}. Current I_1, which flows through resistor R_1, is given by:

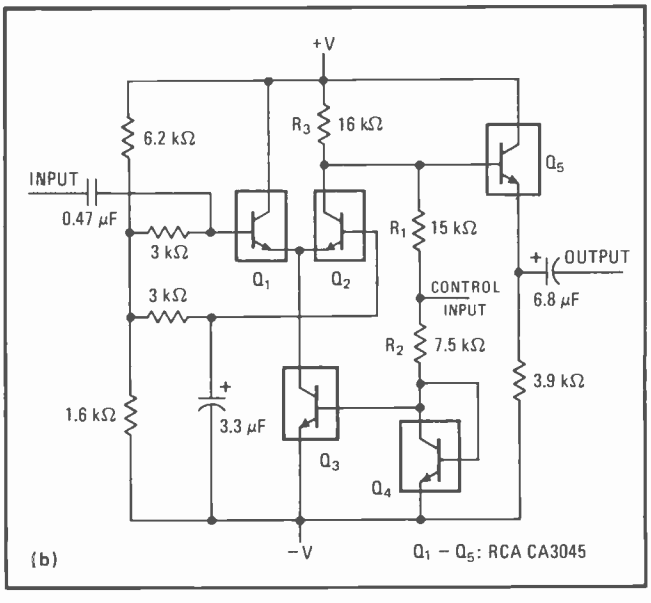
$$I_1 = (E_o - E_{control})/R_1$$

Resistor current I_3 is the sum of collector current I_{C2} and resistor current I_1:

$$I_3 = I_{C2} + I_1$$
$$I_3 = \frac{E_o}{R_1} - \frac{V_{B4}}{2R_2} + \left(\frac{1}{2R_2} - \frac{1}{R_1}\right)E_{control}$$

If $R_1 = 2R_2$, the last term in this equation drops out, making current I_3 independent of the control voltage,





Improved agc. Automatic-gain-control circuit (a) for audio amplifier applications eliminates unwanted thumping that may be heard when the input-signal level changes abruptly. Resistor R_1 prevents sudden variations in the control voltage from reaching the output as an audible thumping. An audio amplifier using this agc scheme is shown in (b); amplifier gain is 30 for a control voltage of 15 volts.

except for a small contribution caused by the dependence of V_{B4} on $E_{control}$. Since the output voltage is proportional to resistor current I_3, and not to the control voltage, variations in the control voltage will not be fed through to the output.

To implement a complete audio amplifier (b) with agc requires only a single monolithic array of five matched transistors. Two transistor pairs are used as indicated in (a), while the fifth remaining transistor is used as an output signal buffer.

The base current error introduced by transistor Q_4 can be reduced by making resistor R_2 slightly less than what the half-value approximation calls for. If resistors R_1 and R_2 are made variable, the performance of the circuit can be optimized by adjusting them for minimum feedthrough. For the component values indicated, the amplifier's voltage gain is about 30 when the control voltage is 15 volts. Circuit gain is directly proportional to the control voltage minus V_{B4}. (Voltage V_{B4} can be approximated as 0.55 V.)

Naturally, amplifier performance is limited by component tolerances. With components having 5% tolerances, the feedthrough signal can typically be suppressed by 20 to 30 decibels. Tighter tolerances will, of course, improve feedthrough suppression, but at some point, the various approximations made (like neglecting the transistor base current error) will limit performance. For a large control voltage, amplifier gain becomes inversely proportional to absolute temperature. At room temperature, this variation in amplifier gain amounts to about 0.03 dB/°C, which is not objectionable for most automatic-gain-control applications. □

Transistor array cuts cost of algebraic inversion

by Pavel Ghelfan
M.G. Electronics Ltd., Rehovot, Israel

Monolithic operators for algebraic inversion are convenient, but a reliable algebraic inverter can be built quite simply and at less cost from an integrated five-transistor array and two operational amplifiers. The circuit first converts the input signal to a logarithmic equivalent and then takes the antilog of this.

The output voltage (V_L) of amplifier A_1 is a logarithmic function of the input current (I_{in}) and the current (I_R) that the transistor array sinks at pin 13:

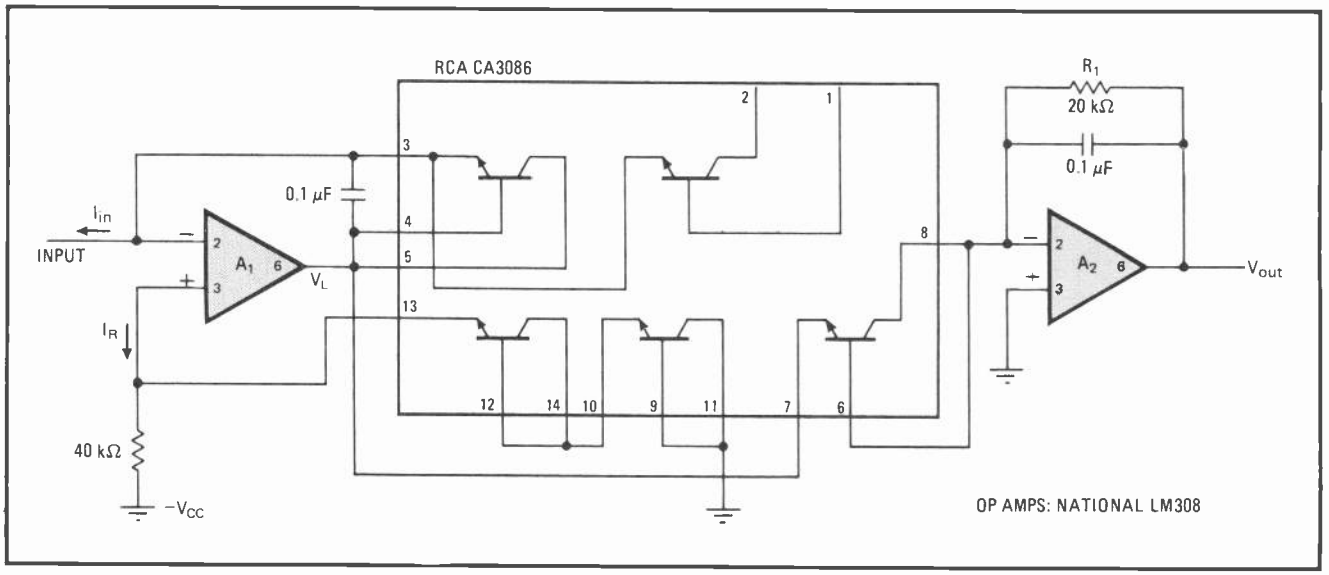
$$V_L = \frac{2kT}{q} ln\left(\frac{I_R}{I_{ES}}\right) - \frac{kT}{q} ln\left(\frac{I_{in}}{I_{ES}}\right) = \frac{kT}{q} ln\left(\frac{I_R^2}{I_{in} I_{ES}}\right)$$

where I_{ES} is the emitter saturation current (with collector shorted to base) of the array's transistors, k is Boltzman's constant, q is the charge of an electron, and T is absolute temperature. The antilogarithmic operation is performed by amplifier A_2. The circuit's output signal can be expressed as:

$$V_{out} = I_{ES} R_1 exp(qV_L/kT) = I_R^2 R_1 / I_{in}$$

Trimming the value of constant current I_{IR} will adjust the numerator of this equation so that the output voltage of the circuit is brought to the desired value and kept there.

This inversion operator maintains good stability over a 50°C temperature range, as well as over three decades of signal amplitude variation. Its amplitude range can be significantly broadened by using low-bias-current operational amplifiers. □



Taking the reciprocal. Algebraic inverter employs IC transistor array to keep costs low and to provide good temperature stability. The circuit converts the input signal to a logarithmic voltage and then takes the antilogarithm of this voltage to develop the output signal. The output, of course, is indirectly proportional to the input and can be brought to the desired value by adjusting resistor R_1.

Economical series regulator supplies up to 10 amperes

by J.E. Buchanan and C.W. Nelson
Westinghouse Electric Corp., Systems Development Division, Baltimore, Md.

A highly efficient series regulator made of standard IC components is an ideal high-current digital-logic supply. It provides an output voltage of 5 to 6 volts at a current of up to 10 amperes, without needing separate bias sources or special transformers.

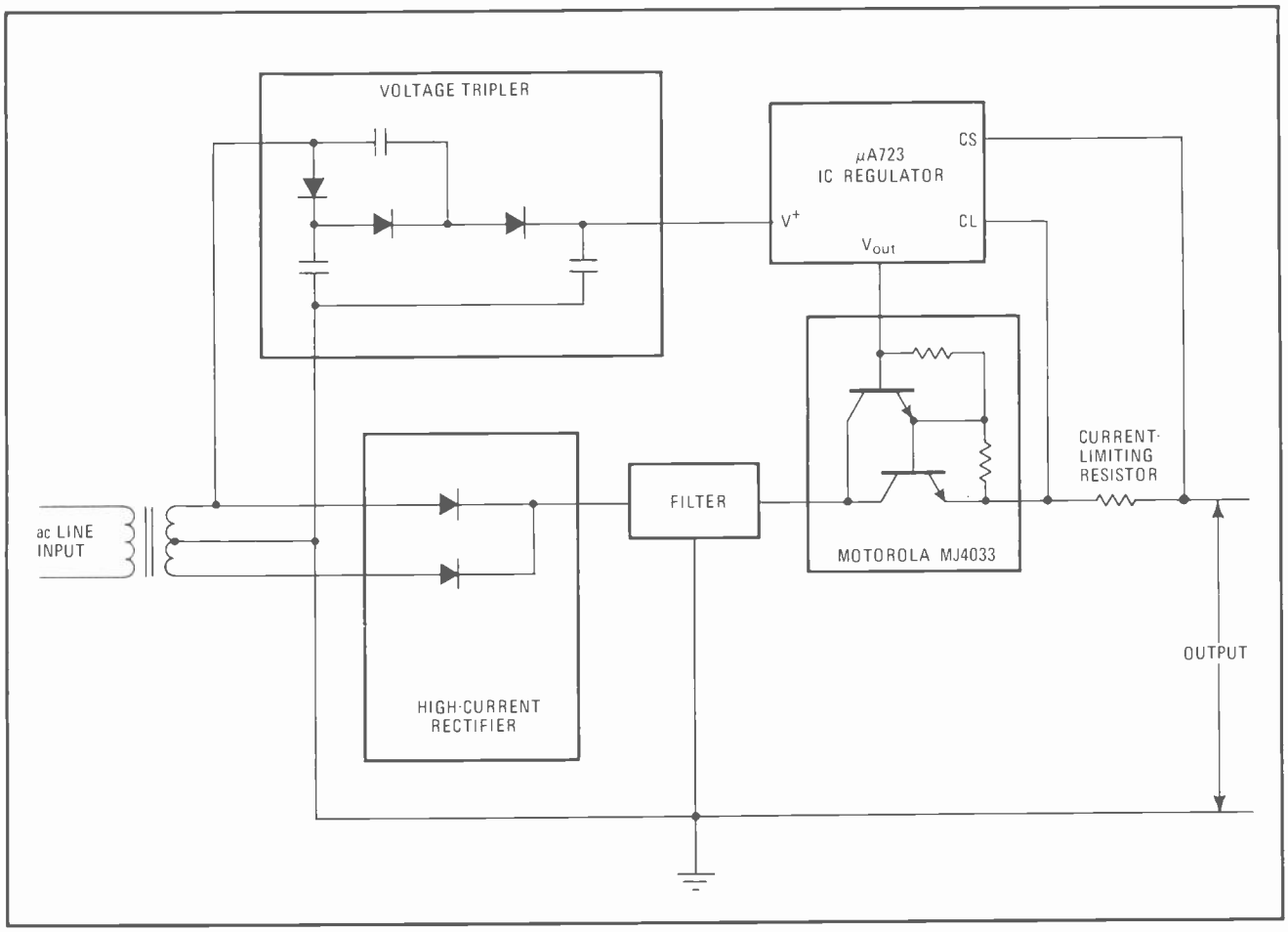
As shown in the figure, a standard transformer is used at the input of the circuit. The transformer's output voltage is rectified and filtered in a conventional manner for the high-current-supply path to the output of the circuit.

This transformer voltage also goes to a voltage tripler, which raises it so that it becomes large enough to drive the IC regulator without help from any outside bias supply. Most three-terminal IC regulators require 10 V or more to bias their internal references properly, preserving their stability with changing input, load, or temperature conditions.

The IC regulator, in turn, drives a high-current power Darlington transistor pair, which is biased by the high-current rectifier. The Darlington pair acts as the circuit's series-pass element and increases the low-milliampere current output from the IC regulator to several amperes.

The circuit's efficiency is very good because the voltage of the high-current supply path can be kept low, permitting the Darlington pair to be driven near saturation with a minimum high-current source voltage. A single transistor can be used instead of the Darlington pair if a lower output current is desired. □

High-current logic supply. This series regulator develops 5 volts at 10 amperes for powering digital-logic circuits. High efficiency is achieved by using a voltage tripler, which operates directly from the input-line transformer, to bias the IC regulator's internal reference. This eliminates the need for a special bias supply or a special transformer. The Darlington transistor pair serves as the series-pass element.



Multiphase clock produces nonoverlapping pulses

by Glen Coers
Texas Instruments, Components Group, Dallas, Texas

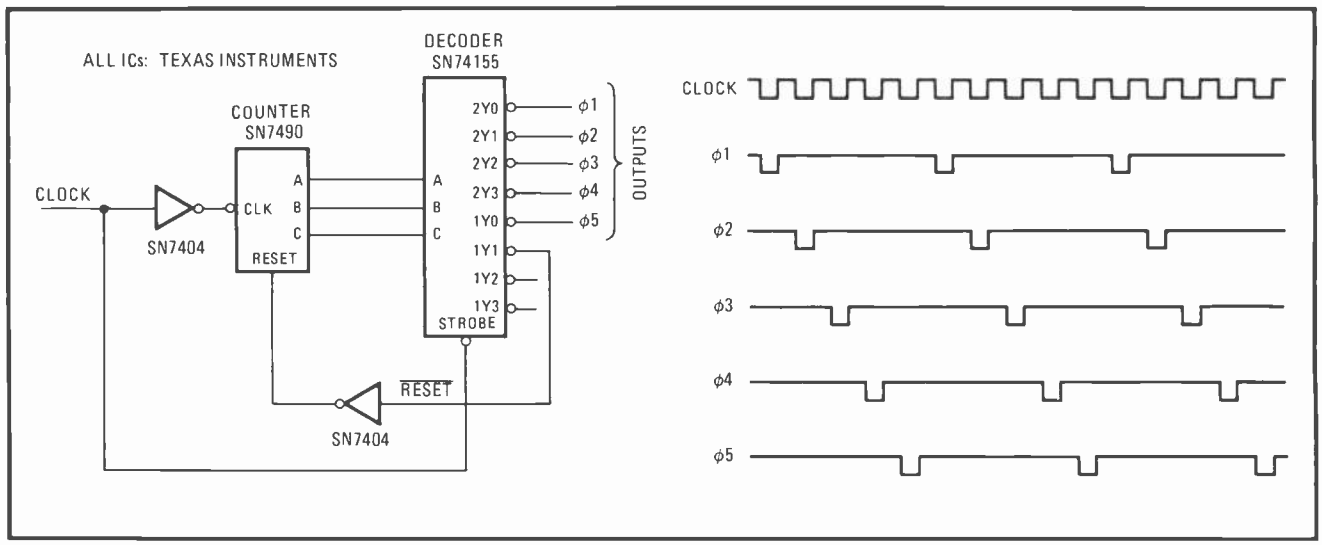
A multiphase clock pulse generator can be put together from a few IC packages by taking advantage of the versatility of an MSI TTL decoder/demultiplexer. The clock generator can be programed to produce from two to seven differently phased clock-pulse trains, and none of the pulse edges will overlap. Furthermore, the time between the pulses of the various clock phases is the same as the width of a single pulse. This means that each individual clock phase is well-defined, and there is no pulse-edge ambiguity, as with other clock-generating techniques.

An MSI decade counter is used with the MSI decoder/demultiplexer, which is connected as a three-line-to-eight-line decoder. Only three of the outputs of the decade counter are needed.

The number of clock phases is determined by the decoder output that is selected to reset the counter to zero. The counter's reset line is simply connected to the decoder's output line that is next in the sequence. As shown in the figure, a five-phase clock is produced by wiring the counter-reset line to the sixth decoder's output line.

The inverter at the input of the counter assures that the decoder is disabled when the count is changing and enabled after the data has stabilized. This eliminates the transients that can appear on the decoder's output lines when the counter is changing states. □

Programable clock. Two MSI devices—a decade counter and a three-line-to-eight-line decoder—can be wired as a simple multiphase clock generator. The circuit can produce from two to seven clock phases without any overlapping pulse edges. The number of clock phases is determined by connecting the counter's reset line to the decoder output line that is next in sequence. A five-phase clock is shown here.



Phase-locked loop adjusts to varying signal conditions

by Charles A. Watson
E-Systems Inc., Greenville, Texas

In many phase-locked receivers, the gain of the amplifier in the phase-locked loop must be changed to adapt the loop gain to varying signal conditions. If the amplifier's gain and offset voltage are changed simultaneously, the signal-acquisition time can be shortened, and signal-to-noise ratios can be optimized.

When the entire loop, including the phase detector, operates from a single supply, the output of the phase detector must be other than zero to have the VCO rest at its midrange frequency. If not of the proper magnitude, this nonzero output offsets or even saturates the loop amplifier, driving the VCO to some non-midrange frequency.

Therefore, an offset voltge, which permits the loop to be adjusted for a midrange VCO rest frequency, is usually introduced at the loop amplifier. If the loop amplifier's gain must be changed to accommodate varying input-signal conditions, this offset voltage must also be changed to maintain the same VCO midrange frequency.

The figure contains a block diagram of a phase-locked loop (a) that includes a switched-gain amplifier, which provides offset compensation for the loop amplifier in response to remotely commanded gain adjust-

ments. The schematic (b) for this variable-gain amplifier, which only requires a quad comparator and a single transistor, is also given in the figure.

When the input logic command to the circuit is high, comparators $COMP_1$ and $COMP_2$ clamp resistors R_1 and R_2 to ground. The circuit's voltage gain can be written as:

$$A_{v(1)} = \left(\frac{R_1}{R_1+R_3}\right)\left(\frac{R_4}{R_2+R_4}\right)$$

Since $R_1 = R_2 = R_3 = R_4$, then:

$$R_4/R_2 = R_3/R_1$$

and:

$$A_{v(1)} = 1$$

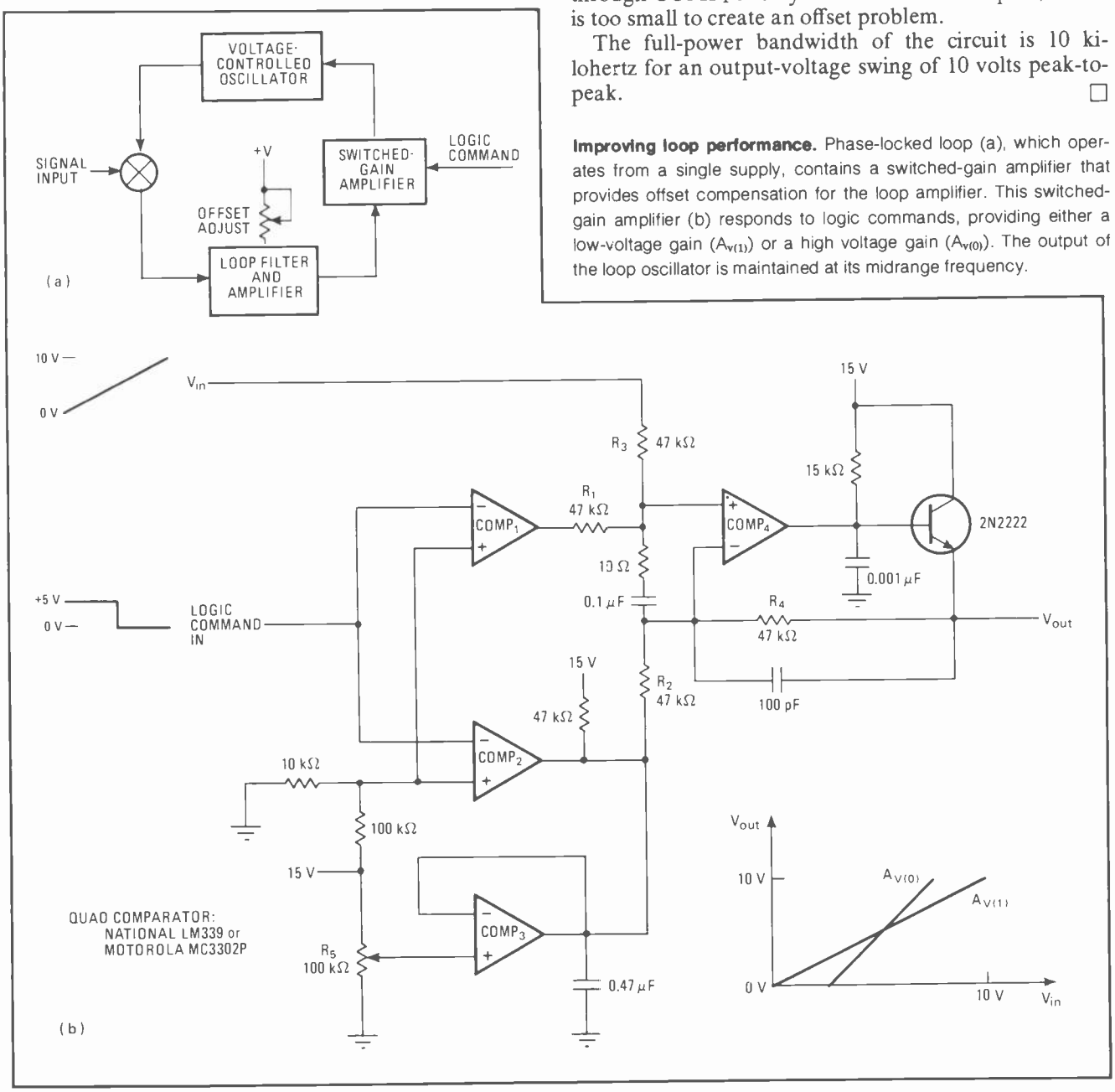
When the input-logic command to the circuit is low, comparators $COMP_1$ and $COMP_2$ unlatch so that resistor R_1 is no longer grounded and comparator $COMP_3$ performs as a voltage-follower, clamping the voltage across resistor R_2 to the desired midrange offset value. The circuit's voltage gain can now be written as:

$$A_{v(0)} = (R_2+R_4)/R_2 = 2$$

Therefore, if the relationship of $R_4/R_2 = R_3/R_1$ is maintained, the circuit's gain can be switched between $A_{v(1)} = 1$ and $A_{v(0)} = (R_2+R_4)/R_2$. Potentiometer R_5 is used to adjust the offset voltage for the circuit's high-gain mode.

Offset and drift problems are minimal with this circuit because the comparators have unusually low output-saturation characteristics (10 millivolts at 0.1 milliampere). Also, when the circuit is in its low-gain mode, the outputs of comparators $COMP_1$ and $COMP_2$ appear as common-mode (temperature-tracking) signals to output comparator $COMP_4$. Moreover, when the circuit is in its high-gain mode, the leakage current through $COMP_1$ is only around 0.1 nanoampere, which is too small to create an offset problem.

The full-power bandwidth of the circuit is 10 kilohertz for an output-voltage swing of 10 volts peak-to-peak. □



Improving loop performance. Phase-locked loop (a), which operates from a single supply, contains a switched-gain amplifier that provides offset compensation for the loop amplifier. This switched-gain amplifier (b) responds to logic commands, providing either a low-voltage gain ($A_{v(1)}$) or a high voltage gain ($A_{v(0)}$). The output of the loop oscillator is maintained at its midrange frequency.

External gate doubles counter speed

by Jeffrey Mattox
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The counting rate of a standard synchronous up/down binary or decade counter can be doubled without altering the clock frequency. A single external gate does the trick for the count-up or the count-down mode.

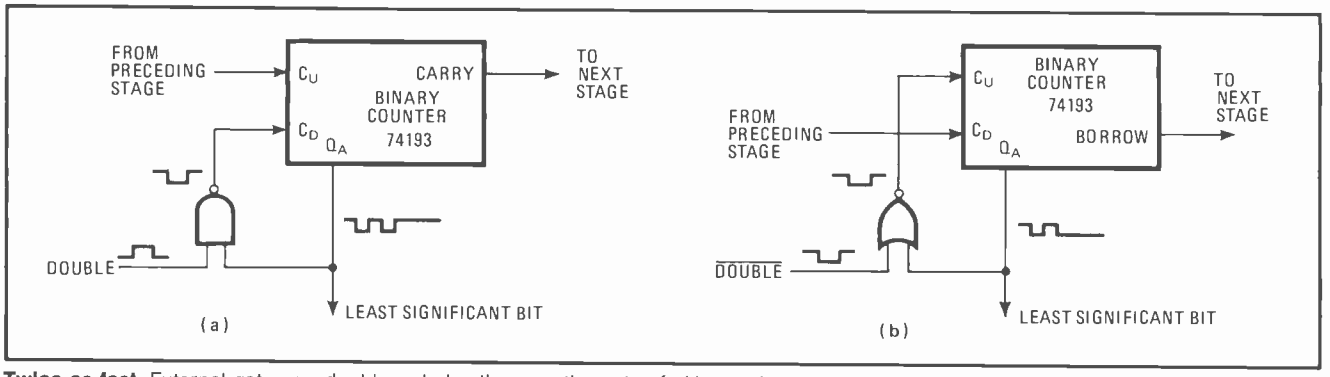
The ability to double the counting rate is useful for applications where a counter must be advanced at twice the normal rate, as in racing the digits to set a digital-clock stage. The extra gate can also be used to halve the counting rate, depending on the logic level of the controlling signal.

Both the decade counter (for example, a type 74192) and the binary counter (for example, a type 74193) have two clock lines—one for the count-up mode, and the other for the count-down mode. The clock input that is not being used is usually tied to the supply line. For either type of counter, there is a counting flip-flop for each output bit.

By sensing the counter's least significant output bit and lowering the alternate-clock input at the proper time, the least significant bit is kept static, and the second counter flip-flop receives all the primary clock pulses. In addition, the state of the least significant bit locks out the alternate-clock input from the other counting flip-flops. For an up-counter, the least significant bit must be high; for a down-counter, it must be low.

The circuit of (a) shows a type 74193 binary counter connected for the count-up mode. The alternate-clock input, in this case the count-down input (C_D), is controlled by a NAND gate. When the DOUBLE input goes high, the C_D input is brought low as soon as the least significant bit is high. The least significant bit remains high until the DOUBLE input returns to the low level. Meanwhile, the count frequency appears to double.

The circuit of (b) is for the count-down mode. It is similar to the one for the count-up mode, but an OR gate is used instead and the DOUBLE control signal must be inverted. The CARRY and BORROW outputs of the counter operate normally so that the doubled counting rate may be carried to the next stage. □



Twice as fast. External gate can double or halve the counting rate of either a decade or binary up/down counter, depending on the logic level of the control signal. The actual clock frequency remains the same. Here, the operating speed of a binary counter is doubled for both the count-up mode (a) and the count-down mode (b). The counter's unused alternate-clock input goes to the controlling logic signal.

Eliminating current spiking from dc-to-dc converters

by Carlo Venditti
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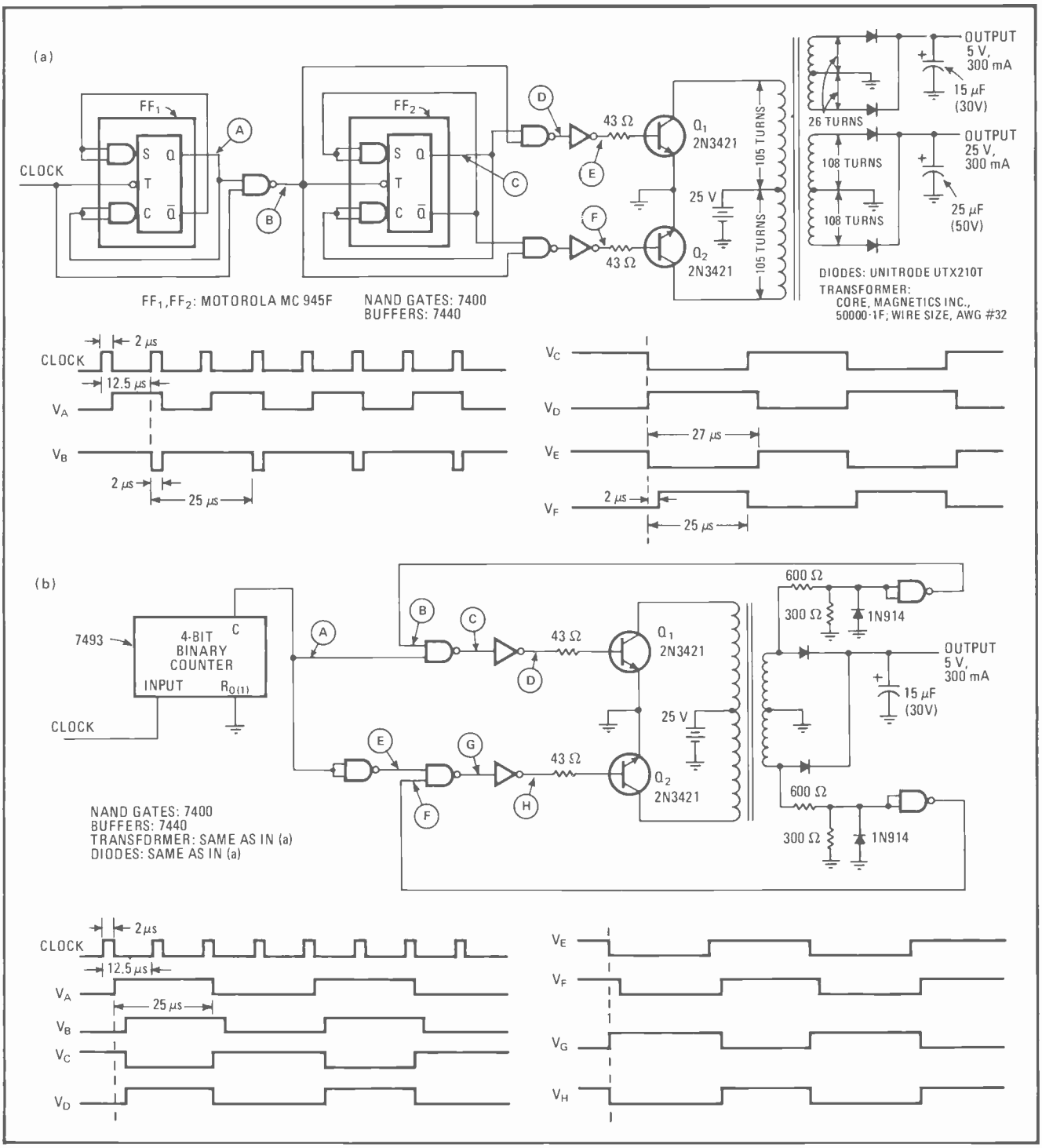
When the two inverter transistors in a push-pull dc-to-dc converter conduct at the same time, current spiking will occur and at worst destroy the circuit, at least degrade its efficiency. These undesirable effects can be prevented by delaying a clock pulse train with standard logic circuits.

Ideally one transistor turns on as soon as the other turns off. But because of their storage time constants, one is often still on when the other is beginning to conduct. All risk of simultaneous conduction will, however, be eliminated if the square-wave base drive signals to the transistors are made asymmetrical. The delay provided by logic gates ensures that, for a short length of time, there is no current drive signal at all. This delay can be fixed (constant) or controlled by feedback.

The figure shows two ways of designing a nonspiking static push-pull dc-to-dc converter. In (a), the current-drive delay time is fixed, and in (b), the delay depends on a feedback signal. In both cases, the transistor on-time is made smaller than the transistor off-time.

There are two output voltage levels for the converter in (a)—5 and 25 volts at a current of 300 milliamperes. The converter in (b) has just the one 5-V 300-mA output. Although a clock pulse generator operating at 80 kilohertz is used to synchronize each converter, the



Improving dc-dc converter efficiency. These dc-dc converters employ push-pull inverter transistors that switch at 20 kilohertz. Conventional digital ICs are used to delay the drive signals to the switching transistors so that these devices cannot conduct simultaneously, causing unwanted current spikes. The converter in (a) has a fixed delay, while the delay of the converter in (b) depends on a feedback signal voltage.

switching frequency is only 20 kHz in each case, and the nominal transistor on/off time is 25 microseconds (total period of 50 μs).

In the fixed-delay circuit of (a), flip-flops FF_1 and FF_2 generate the basic square-wave drive for transistors Q_1 and Q_2. The flip-flops divide the clock frequency down from 80 to 20 kilohertz, and the NAND gates provide the delays for the transistor drive signals.

The resulting asymmetrical driving waveforms have an on-time of 23 μs and an off-time of 27 μs. This means that each transistor experiences a 2-μs delay in its drive signal. For the transistors used here, this delay prevents current from flowing into the transformer primary for 0.5 μs. The width of the delay pulse (2 μs here) is too wide if the converter's output ripple voltage increases and too narrow if there is no deadband for the transformer primary current.

In the feedback-adjusted-delay circuit of (b), a binary counter, rather than flip-flops, divides the clock frequency down to 20 kHz. NAND gates again provide the

appropriate delays for producing asymmetrical transistor drive signals.

The feedback voltage, which is taken from the transformer secondary, determines when the transistors turn on, while the reference voltage from the counter output determines when they turn off. To delay the turn-on feedback signal properly, the storage time of the rectifier diodes, as well as the flux flyback time of the transformer, must be taken into account. For circuit (b), the deadband time is 0.3 μs. □

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SCR crowbar circuit fires quickly and surely

by Steve Summer
Hauppauge, N.Y.

A monolithic voltage regulator's presence in an SCR crowbar circuit makes the circuit fast-acting, dependable, and capable of producing fast-risetime drive currents as large as several amperes. The circuit shown in the diagram is simple yet effective, providing a drive current of 200 milliamperes with a risetime of 1 microsecond. The 723-type IC regulator is used as a comparator that contains its own stable reference voltage source. The setpoint of the comparator establishes the protection voltage level for the power-supply bus.

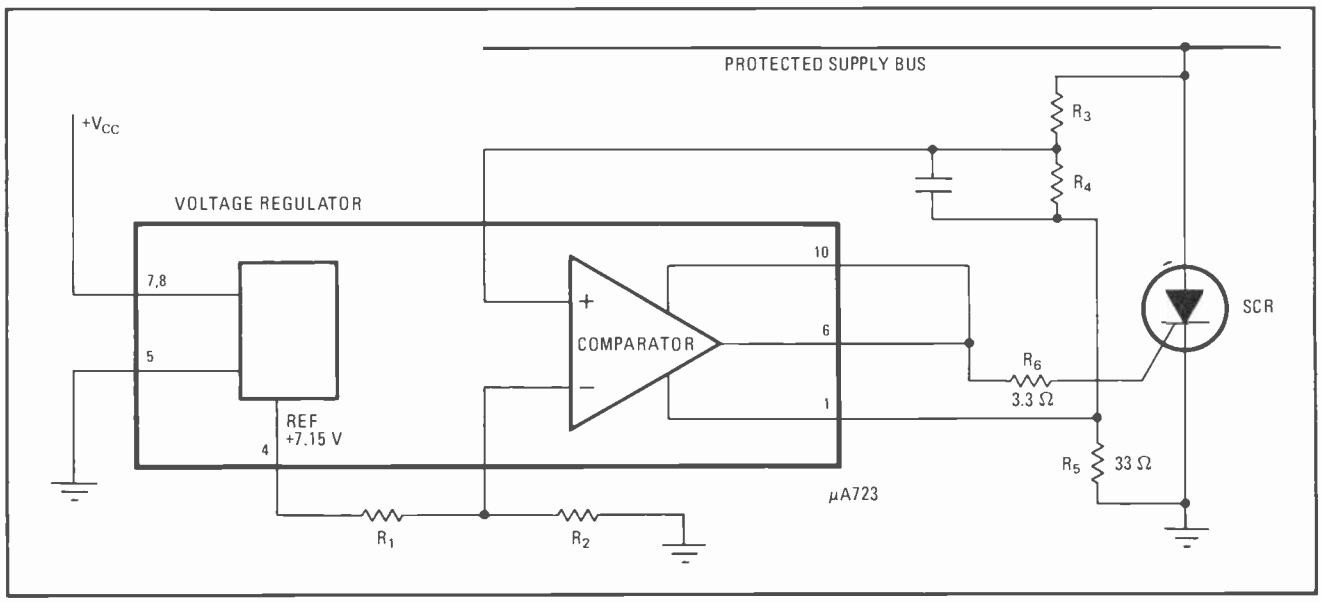
A satisfactory crowbar circuit for good power-supply protection generally asks a lot of the crowbar SCR. Typically, power supplies have large output capacitances that impose high surge currents and di/dt levels on the crowbar SCR when it is fired. These large current surges can cause SCR failure or degradation if the SCR drive current is inadequate or soft (has a slow risetime).

The gate drive required to attain the SCR's specified surge and di/dt capability may be many times greater than the worst-case gate drive needed for turn-on. In addition, for best di/dt resistance, the risetime of the gate drive should be quite short, preferably less than a microsecond.

Many simple crowbar circuits use such devices as zener diodes to fire the crowbar SCR. Although this results in a soft turn-on that will fire the SCR at least once, the dependability of such a scheme is questionable.

The circuit shown, however, is hard-firing. Resistors R_1 and R_2 make up a voltage divider that nominally sets the voltage at the inverting input of the comparator to 2 volts. Another voltage divider, consisting of resistors R_3 and R_4, samples the power-supply bus and drives the comparator's noninverting input. When the voltage on the power-supply bus exceeds the setpoint of the comparator, the output of the regulator rises. This voltage rise, which appears across resistor R_5, adds (in phase) to the voltage at the comparator's noninverting input, providing rapid regeneration, as well as a fast-rising pulse to drive the SCR.

Resistor R_6 limits the SCR drive current to about 200 milliamperes, a value that is adequate for sensitive-gate or amplifying-gate devices. To obtain larger drive currents of up to several amperes, an emitter-follower stage can be added at the output of the regulator. The capacitor acts as a filter to prevent the crowbar from firing in response to transient voltages. □



Hard-firing SCR. Crowbar protection circuit employs an IC voltage regulator to produce a fast-risetime large-value gate drive current for the SCR. The regulator, which is used as a comparator, has its own voltage reference source. When the voltage on the power-supply bus exceeds the set point of the comparator, the regulator's output voltage increases, producing a large fast-rising pulse that fires the SCR.

Adjustable discriminator cleans up signal noise

by Dennis D. Barber
University of Houston, Houston, Texas

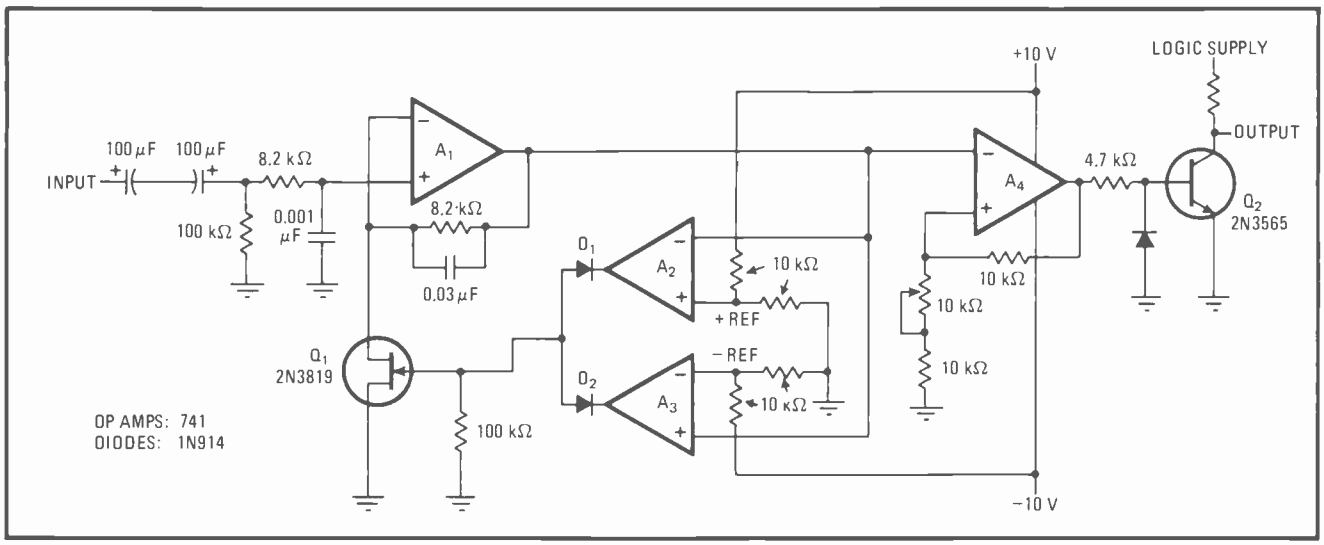
Telemetry signals or other logic signals often pick up a lot of extra noise during transmission. But they can easily be cleaned up at the receiving end by a discriminator circuit having adjustable hysteresis.

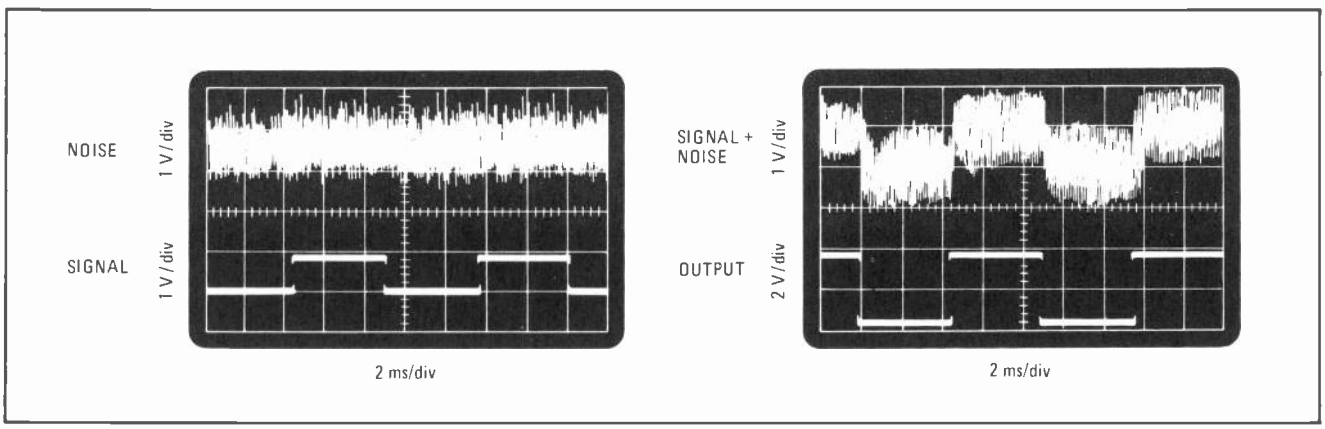
The voltage discriminator shown in the figure can clean up signals containing as much as 70% noise without the need to alter the signal amplitude or dc level. The input to the amplifier that serves as the voltage-discriminator (amplifier A_4) is kept constant at 5 volts peak-to-peak. But the signal to be conditioned, the one at the input to the circuit, does not have to be critically maintained or its level known precisely.

Amplifier A_1 is gain-controlled, with field-effect transistor Q_1 acting as the gain-control element. This FET, which functions as a voltage-variable resistor, is controlled by amplifiers A_2 and A_3. Amplifier A_4 is the voltage-discriminator stage that provides the adjustable hysteresis through its variable regenerative feedback.

Before the capacitively coupled input signal goes positive or negative, the output of amplifier A_1 may be treated as if it were at ground. The gain of amplifier A_1 is then at its maximum since the inputs to amplifiers A_2 and A_3 are below (in absolute magnitude) their respective reference voltages. The output of each amplifier is now positive, and diodes D_1 and D_2 are back-biased, which allows transistor Q_1 to turn fully on.

If the input signal goes positive, the output of A_1 will move towards the positive power-supply level. When it reaches the reference voltage of A_2, the output of A_2 quickly swings negative, turning transistor Q_1 partially off and thus lowering the gain of A_1. The output of A_1 is held at the positive reference voltage until this reference level is greater than the input voltage multiplied by the maximum gain of A_1. At this point, the input voltage is only a few millivolts above ground.





Pulling the data out of the noise. Adjustable-hysteresis voltage discriminator makes significant improvement in signal-to-noise ratios, as can be seen from the scope traces. The level of regenerative feedback of amplifier A_4, the voltage-discriminator stage, is adjusted to provide optimum noise immunity. The gain of amplifier A_1 is controlled by transistor Q_1, which is operated as a voltage-variable resistor.

As the input signal swings from positive to negative, the output of amplifier A_2 goes positive, but the output of amplifier A_3 becomes negative. The gain of amplifier A_1, therefore, is limited until the input signal again returns to very near ground.

In this way, the input voltage to amplifier A_4, the voltage discriminator, is maintained at a constant level. The threshold voltages for A_4 can be set slightly less than the reference voltages of A_2 and A_3, enabling the circuit to provide excellent noise immunity.

The capacitors at the input of the circuit are used to limit the amplitude of high-frequency spikes. The 100-microfarad capacitor values indicated in the diagram function well over a frequency range of 1 cycle per minute to 1,000 cycles per second and over an input amplitude range of 1 to 10 v pk-pk.

Transistor Q_1 can be almost any junction FET. Transistor Q_2 is included to make the output of the circuit compatible with the type of logic being used. Many types of general-purpose op amps should work in the circuit, and even Norton amplifiers like the type-3900 units can probably be used if the appropriate circuit modifications are made.

The oscilloscope photographs show how dramatically this discriminator can clean up signals. One photo shows separate signal and noise voltages, while the other photo shows the total input signal and the resulting output. □

Controlling ac loads with C-MOS bilateral switches

by Arthur Johnson
Darlington, Md.

Power to an ac load can be efficiently controlled by an integrated complementary-MOS quad bilateral switch and a capacitively triggered sensitive-gate triac. The necessary gate-triggering current comes, not from the low-voltage C-MOS power supply, but from the ac line.

Capacitor-triggering is best for firing the triac because it produces the maximum current (at 90° phase shift) when the ac voltage crosses the zero-voltage level. Therefore, the fullest possible use is made of gate-triggering current. Also, the triac is switched into conduction at a low voltage to reduce switching transients, and maximum power is delivered to the load.

The driver circuit for ac loads is drawn in the diagram. Because the on-resistance of each C-MOS bilateral switch is several hundred ohms, circuit voltages could falsely trigger the triac. The triac gate therefore needs to be isolated by the series switch, which, in turn, needs to be protected in its nonconducting state by the shunt switch from possibly damaging high voltages.

Two power-supply voltages, +7.5 volts and −7.5 v, are needed to control both positive and negative ac voltage excursions. This may prove to be a minor inconvenience. But since the necessary gate-triggering current does not have to come from these supplies, they may be simple half-wave-rectified high-resistance sources.

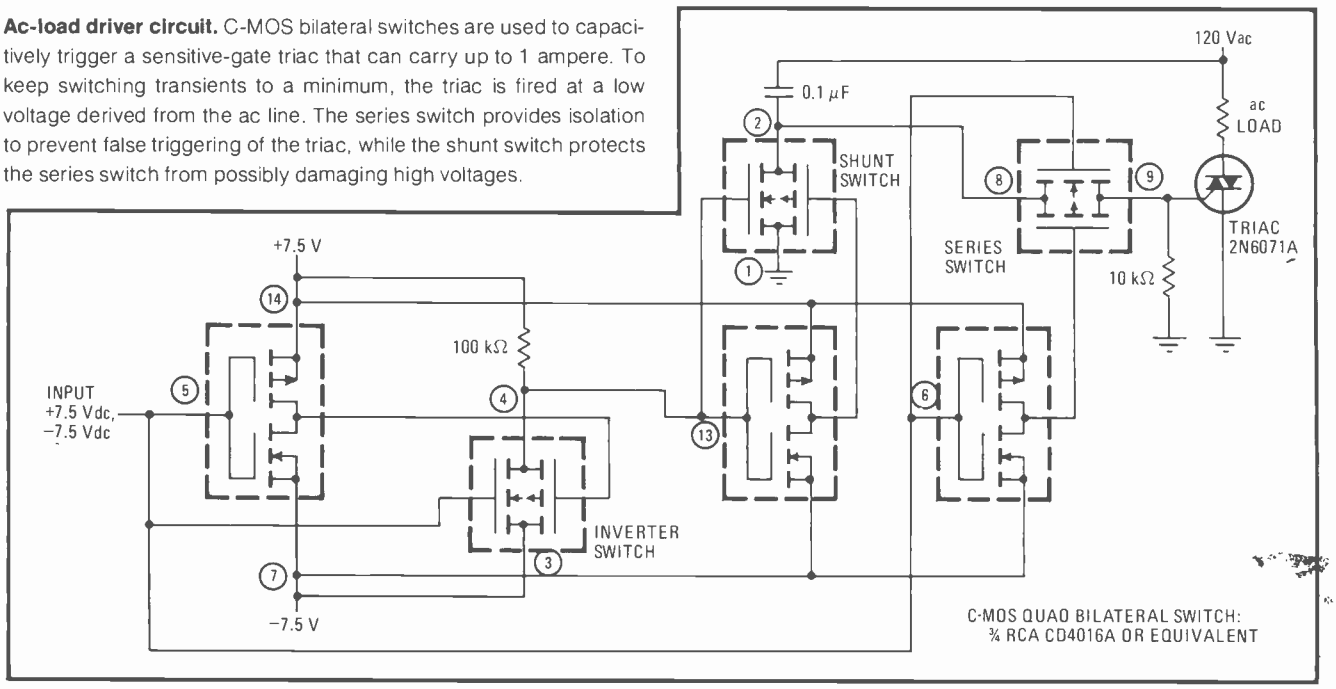
The sensitive-gate triac used here has a maximum current-carrying capacity of 1 ampere. If a larger load must be handled, a triac with higher ratings can be controlled by the smaller triac. In this way, a large load can be controlled without wasting a large amount of energy.

The capacitor value is chosen to provide the required triac-triggering current of 5 milliamperes maximum:

$$C = (5\ mA)/2\pi f E_{max}$$

where f is the ac frequency and e_{max} is the zero-to-peak ac voltage level. □

Ac-load driver circuit. C-MOS bilateral switches are used to capacitively trigger a sensitive-gate triac that can carry up to 1 ampere. To keep switching transients to a minimum, the triac is fired at a low voltage derived from the ac line. The series switch provides isolation to prevent false triggering of the triac, while the shunt switch protects the series switch from possibly damaging high voltages.



IC timer makes economical automobile voltage regulator

by T.J. Fusar
Powell-Mac Electronics, Madison, Wis.

A 555-type IC timer, in combination with a power Darlington transistor pair, can provide low-cost automotive voltage regulation. Such a regulator can even make it easier to start a car in cold weather.

As the diagram shows, the circuit requires very few parts. The value of resistor R_1 is chosen to prevent the timer's quiescent current, when the timer is off (output, pin 3, low), from turning on the Darlington pair.

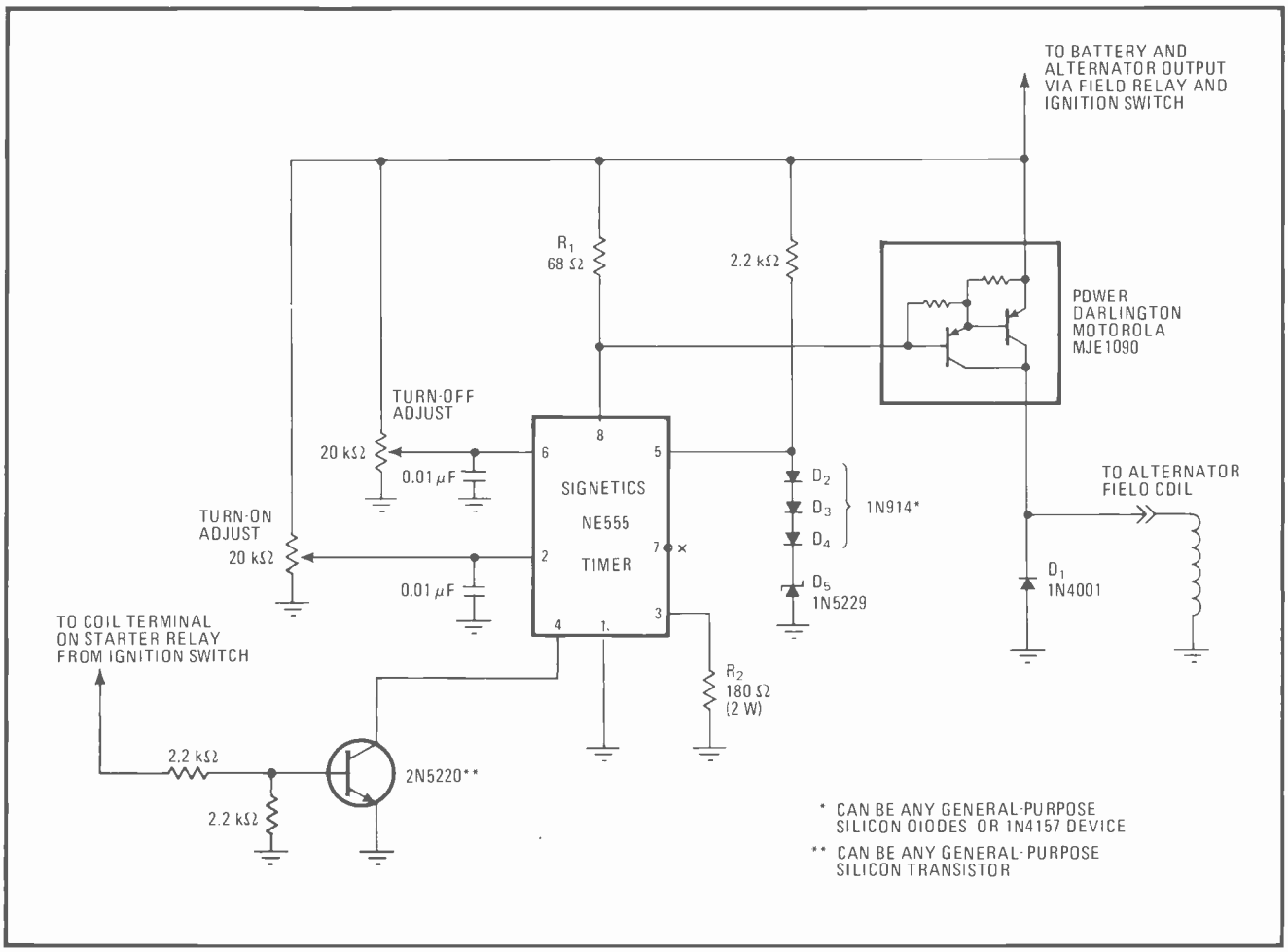
If battery voltage becomes too low, the timer turns on, driving its output high and drawing a current of about 60 milliamperes through resistor R_2. This causes a sufficient biasing voltage to be developed across resistor R_1 and the Darlington turns on, supplying the energizing current to the field coil of the car's alternator. Diode D_1 suppresses the reverse voltage of the field coil when the Darlington pair is turned off.

The regulator's low-voltage turn-on point is fixed by setting the voltage at the timer's trigger input (pin 2) to approximately half the reference voltage existing at its control-voltage input (pin 5). The high-voltage turn-off point is set by making the voltage at the timer's threshold input (pin 6) equal to the reference voltage at pin 5. At 77°F, the turn-on voltage is typically 14.4 volts, and the turn-off voltage is typically 14.9 v. These voltage levels, of course, should be set to match the charging requirement of a given car's specific battery-alternator combination.

The value of the reference voltage is established by the diode string, D_2 through D_5; here, it is approximately 5.9 v. The output voltage has a negative temperature coefficient of -11 millivolts/°F.

A transistor and a couple of resistors can be added to the circuit for better cold-weather starting. These parts are drawn in color in the figure. During starting, the transistor holds the timer in its off state, lightening the load on the car's cranking motor. (And to prevent radio interference, a 10-microfarad capacitor can be connected from the Darlington emitter to ground.) □

Regulating car voltage cheaply. Monolithic 555-type timer is the heart of this simple automobile voltage regulator. When the timer is off so that its output (pin 3) is low, the power Darlington transistor pair is also off. If battery voltage becomes too low (less than 14.4 volts in this case), the timer turns on and the Darlington pair conducts. The parts drawn in color permit easier starting in cold weather.



Transistor array converts to fast-switching thyristors

by H.S. Kothari
Central Electronics Engineering Research Institute, Pilani, India

An ordinary monolithic transistor array can be wired to perform as multiple four-layer silicon-controlled switches by making use of the terminal to the array's substrate. For example, a seven-transistor array having common emitters can be used to implement a seven-stage ring counter.

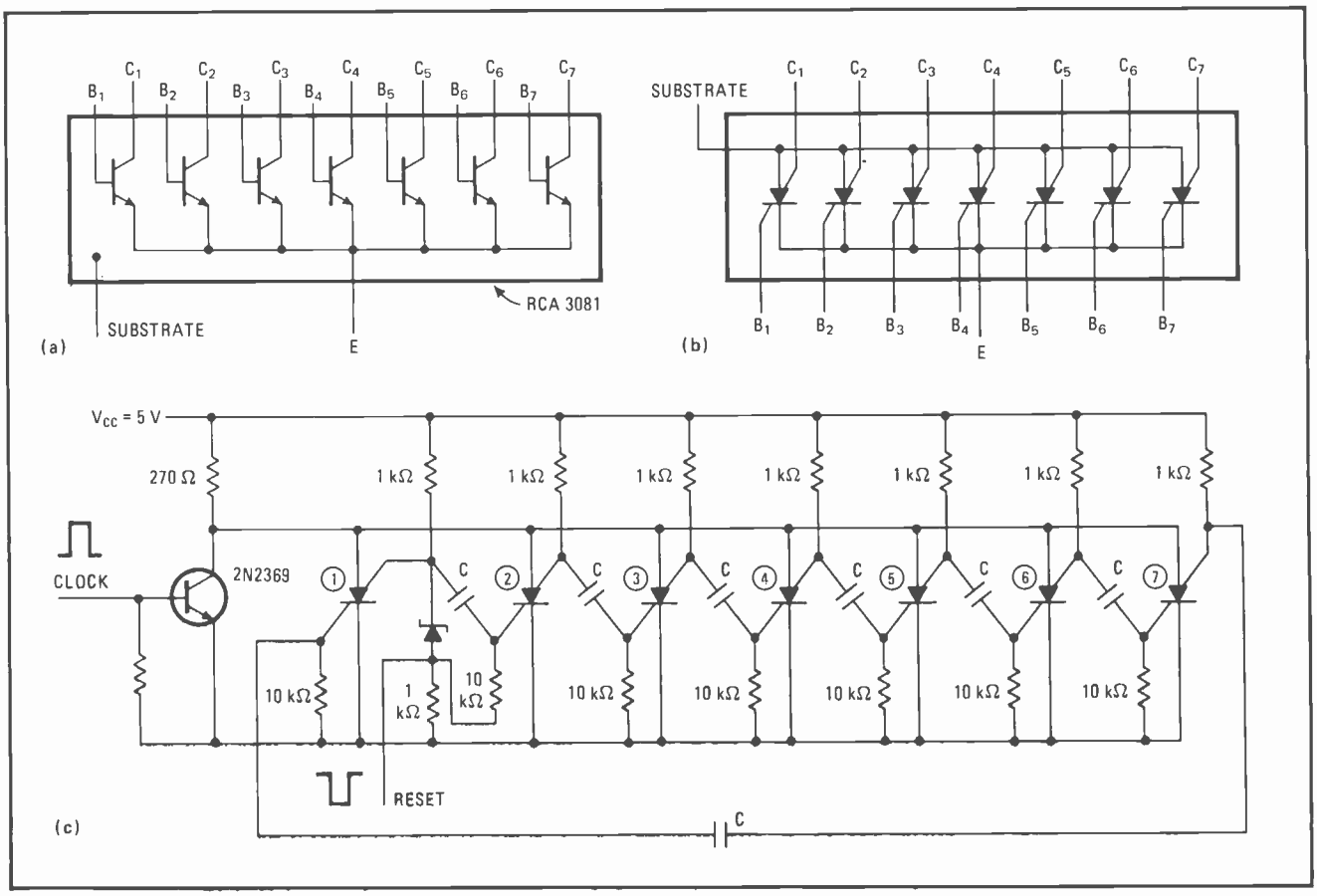
As shown in (a), the npn transistor array has a separate connection to its p-type substrate. The array is easily wired as shown in (b), with the substrate being employed as a common anode to form pnpn structures that can be regarded as silicon-controlled switches. And since the geometry of each transistor is very small, switching times can be on the order of a few nanoseconds.

The schematic of the ring counter is drawn in (c). The first stage is turned on by the trailing edge of the reset pulse. Now, when a clock pulse is applied to the input transistor, the voltage at this transistor's collector drops, and the other counter stages are turned off. In this way, a trigger pulse is transferred from the first stage to the second stage. The next clock pulse causes a trigger pulse to go from the second to the third stage. This process continues and repeats when the seventh counter stage triggers on the first counter stage.

The hold-on current for any stage can be between 50 microamperes and 1 milliampere. The negative voltage amplitude of the reset pulse should be large enough to lower the voltage of the anode gate of the first stage so that this stage is sure to fire. The anode-gate voltage, therefore, is made negative with respect to the anode voltage.

The length of the triggering delay is determined by the capacitance value selected. Voltage amplitudes can be made as large as the collector-emitter breakdown limit of each transistor by increasing the supply voltage, as well as the zener voltage, to some suitable maximum level. □

Wiring transistors as thyristors. Integrated seven-transistor array (a) can be wired as silicon-controlled switches by making use of their common substrate connection. The transistors can then be operated as four-layer devices (b) that have switching times on the order of a few nanoseconds. One application for the pnpn switch array is illustrated in (c)—a seven-stage ring counter.



C-MOS touch-switch array controls analog signals

by Max W. Hauser
Berkeley, Calif.

A few inexpensive complementary-MOS ICs can be used to create a bounceless buttonless touch-switch array. The resulting switching circuit takes advantage of the extremely high input impedance of C-MOS devices to detect the ambient signals (electrostatic charge and power-line hum) present on a person's finger. The circuit's outputs are solid-state switches that are capable of controlling audio or analog signals with negligible distortion and that, in many cases, are compatible with existing circuitry. Light-emitting diodes provide a visual display of the current state of these switches.

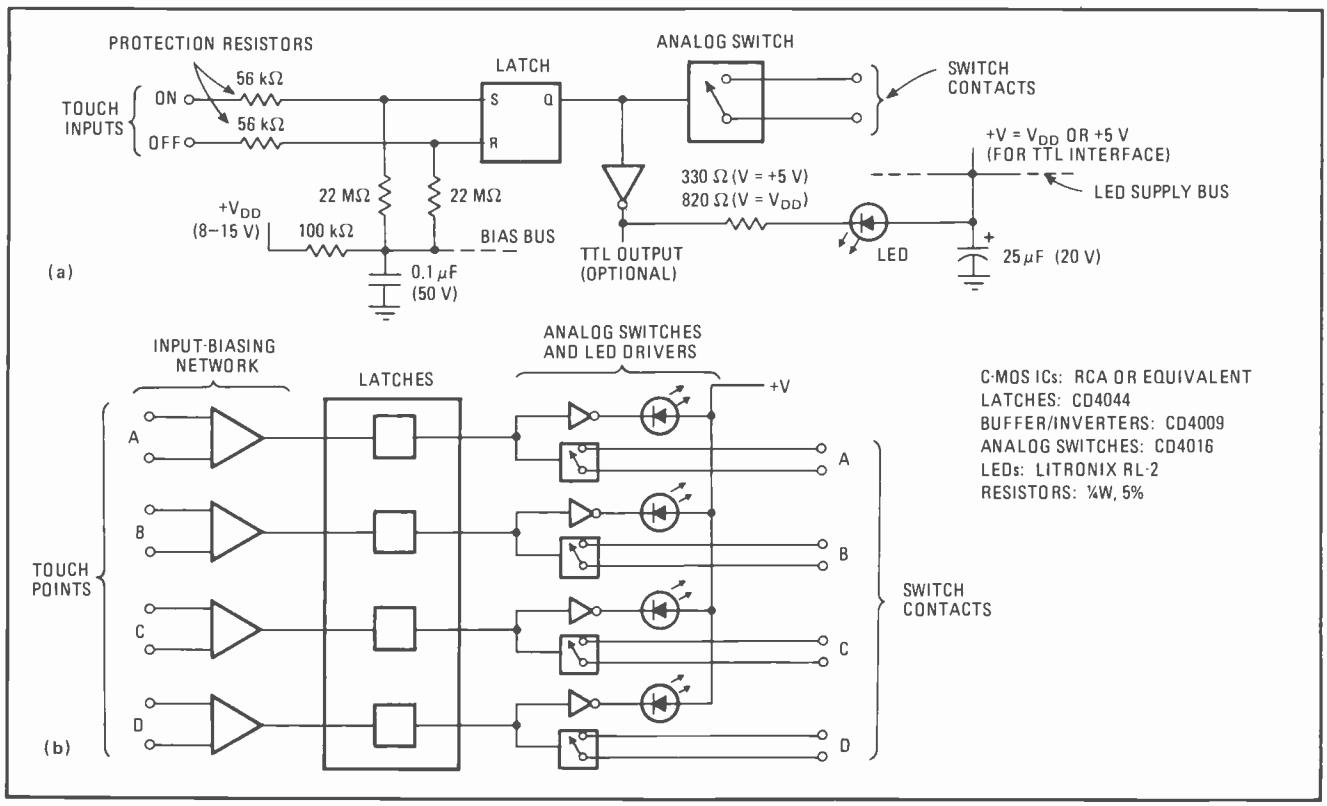
The heart of each touch-switch (a) is a set-reset flip-flop (one-quarter of a quad latch) whose inputs are biased to the V_{DD} supply through 22-megohm resistors. Under normal (resting) conditions, this renders the inputs inactive, and the flip-flop retains its last state. When a finger or large conductive object touches either the on or off input, a noise voltage appears across the bias resistor at that input and is amplified through the regenerative action of the flip-flop. This sets the flip-flop to the desired output state, where it remains until reset by touching the other input.

The flip-flop's output simultaneously controls an analog switch and a buffer/inverter that drives a panel-mounted LED. The output from the buffer can also be used to activate a TTL input, provided that the internal pull-up supply (V_{CC}) is made equal to the TTL power-supply voltage. The 100-kilohm resistor and the 0.1-microfarad capacitor serve to decouple the V_{DD} bias supply so that there is no interaction between the input and display portions of the circuit.

The block diagram (b) shows how a quadruple touch-switch array looks. The touch-sensors should be small metal plates—squares or disks having a side or diameter of 1 to 2 centimeters are best. A substantial increase in plate area results in a proportionate increase in the quiescent hum pickup, and can reduce circuit reliability unless the sensor is mounted very carefully. At the expense of added construction complexity, the LEDs or their mountings can be given a conductive coating, permitting them to serve as the solid-state equivalent of illuminated push-button switches.

Type-CD4016 analog switches work well for noncritical applications, for example, if the circuit is to be used as a source selector for an audio-mixing console. In more critical systems, however, it may be desirable to substitute lower-impedance devices, such as type-CD4066 units. Of course, each flip-flop output can drive many analog switches, and a complex switching arrangement can be created that might be difficult or uneconomical to implement with mechanical devices. Normally closed switching is possible by driving the analog switches with the buffer/inverter outputs, but the cir-

Touch-actuated switching. A simple touch-switch (a) can be built with complementary-MOS ICs. The high input impedance of the C-MOS latch permits the ambient signals of a fingertip to be sensed. The latch's output then controls a C-MOS analog switch, which implements the desired switching function. The LED indicates whether this analog switch is on or off. A quadruple touch-switch array is shown in (b).



cuit's TTL interface must be sacrificed.

In remote locations, where power lines or other major electromagnetic-field sources are not available, it is advisable to install a second contact (at ground potential) on each sensor, so that a slight conduction between the two contacts will assure triggering. Also, to eliminate any chance of damage to the flip-flop inputs from an external power source, the inputs should be protected against excessive current flow with 56-kilohm resistors, as shown. □

Switching regulator produces constant-current output

by Steven E. Summer
Hauppauge, N.Y.

The high efficiency that can be achieved with switching regulators need not be restricted solely to voltage regulators. By taking advantage of the convenience of a monolithic voltage regulator, a free-running constant-current switching regulator having a 1-ampere output can be built for applications like battery charging.

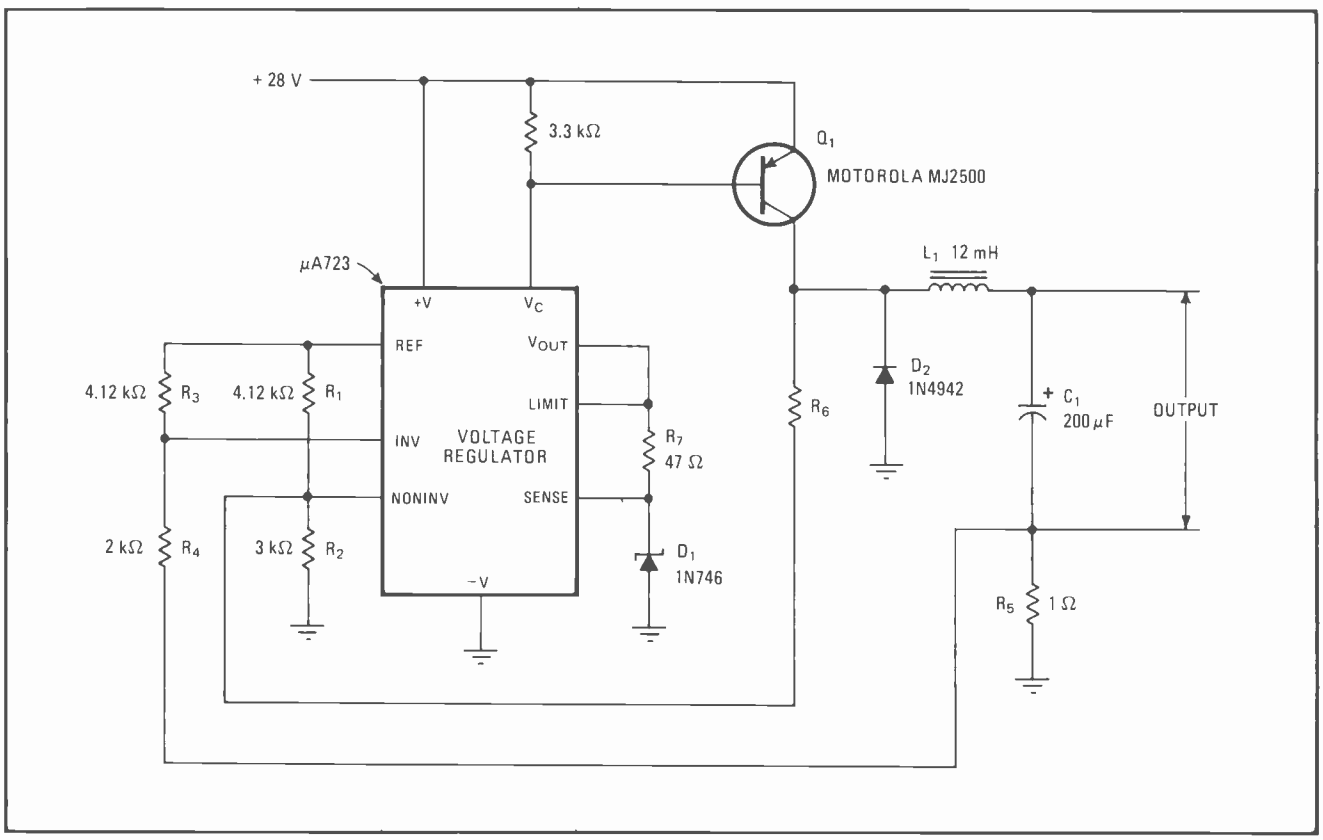
A 723-type IC regulator acts as the circuit's reference and comparator. The IC's 7.15-volt internal reference is scaled to approximately 3 V by the voltage divider formed by resistors R_1 and R_2. These resistors also feed the IC's noninverting input, while resistors R_3 and R_4 drive the IC's inverting input. The lower end of resistor R_4 is connected to shunt resistor R_5, and approximately 1 V appears across this shunt when the IC's comparator terminals are nearly balanced.

A hysteresis voltage of around 28 millivolts is applied to the IC's noninverting input through resistor R_6. This sets the minimum output ripple of the circuit at 28 milliamperes peak to peak. But if the storage time of output transistor Q_1 is significant, the ripple current will be higher.

When the circuit's feedback loop calls for a current increase, the output stage of the IC regulator conducts and a current pulse of 12 mA flows into the V_C terminal. (The size of the current pulse is determined by resistor R_7.) This current pulse drives transistor Q_1.

The zener diode (D_1) is used to bias the output stage of the IC regulator, while the junction diode (D_2) operates as a freewheeling diode. Inductor L_1 and capacitor C_1 filter the switched waveform. The circuit's maximum operating frequency depends on the size of the load and is typically 20 kilohertz. □

Constant-current source. Switching regulator circuit provides a 1-ampere constant-current output that has a peak-to-peak ripple of 28 milliamperes. The integrated 723-type voltage regulator functions as a reference source and a comparator. Transistor Q_1 is a current booster, while inductor L_1 and capacitor C_1 filter the switched waveform. The circuit's operating frequency can be as high as 20 kilohertz.



Ordinary cassette recorder can be full-time phone monitor

by G. Breindel
University of Washington, Seattle, Washington

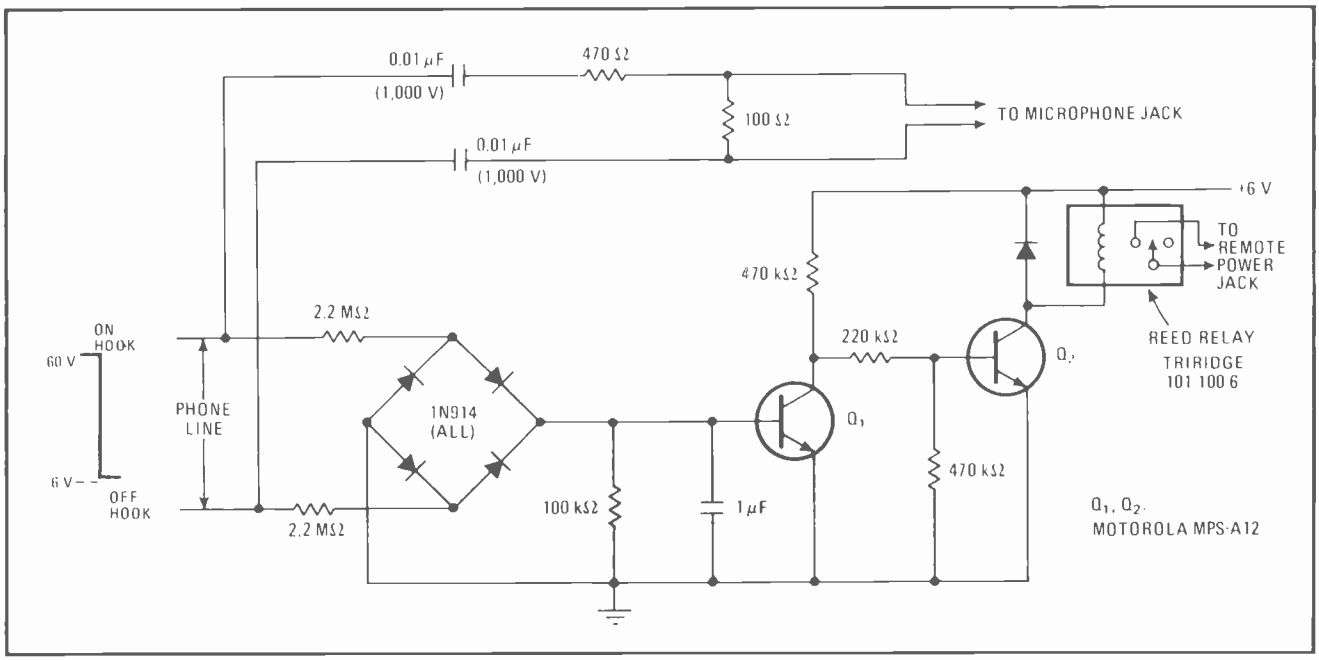
A simple circuit can convert an inexpensive conventional cassette-type recorder into a telephone recorder that automatically tapes all incoming and outgoing calls. Parts cost is less than $5, and there's no need to modify the recorder's internal circuitry. The circuit will work, provided that the recorder has a microphone (audio in) jack and a remote power jack (a jack for the remote control of power to the recorder's internal circuitry).

Besides automatically taping all calls, the circuit makes a recording (in pulse or tone format) of all the numbers dialed from the line to which it is connected. It acts as only a negligible load on the phone line, and it draws very little current when the phone is not in use. Even so, such a phone-line attachment should be approved by your local telephone company.

When the phone receiver is on the hook, transistor Q_1 is on while transistor Q_2 is off. When the receiver is off the hook, the phone-line voltage drops to less than 10 volts. Transistor Q_1 now turns off and transistor Q_2 turns on, energizing the reed relay, which shorts the recorder's remote jack and starts the recording process.

The diode bridge permits the circuit to be connected to the phone line without regard to polarity. The two capacitors provide the necessary audio coupling while isolating the recorder from the phone line. Power for the circuit can be obtained from the recorder's own battery supply (four type-D cells) or from a separate 6-v battery.

To comply with phone company regulations, a tone should be heard on the line every 15 seconds. This can be easily accomplished by adding a couple of unijunction transistors to the circuit. □



On the line. Economical circuit automatically activates a standard cassette recorder so that the recorder tapes all calls, as well as the numbers dialed. A pair of Darlington transistors is used to switch the reed relay that controls the recorder's remote power jack. The diode bridge allows the circuit to be hooked up to the phone line without concern for polarity. A tone beep signal can be added easily.

State-variable filter uses only two op amps

by Charles Croskey
Pennsylvania State University, University Park, Pa.

One of the more useful circuits for an active filter design—the state-variable active filter—can be somewhat expensive to build because it normally requires three operational amplifiers. Two of these op amps function as integrators, while the third is used as an inverter, since a difference integrator has been rather difficult to make with a normal op amp.

The state-variable filter in the diagram, however, re-

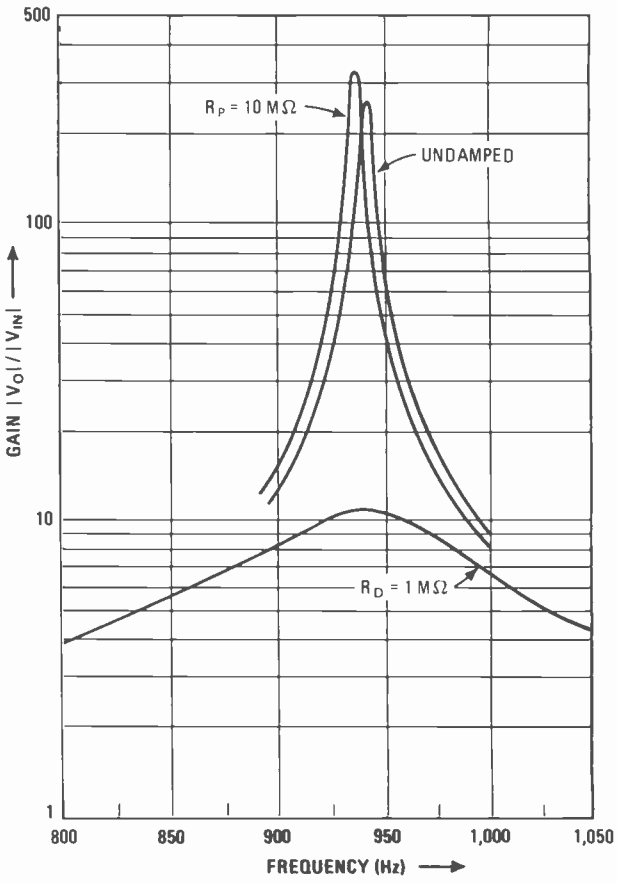
quires only two op amps. The circuit takes advantage of the recently introduced integrated quad amplifiers, such as Motorola's MC3401 and National's LM3900, which respond to a current difference instead of a voltage difference. Such amplifiers permit a difference integrator to be built simply.

The center frequency of the filter's bandpass function is still determined by the usual relationship of:

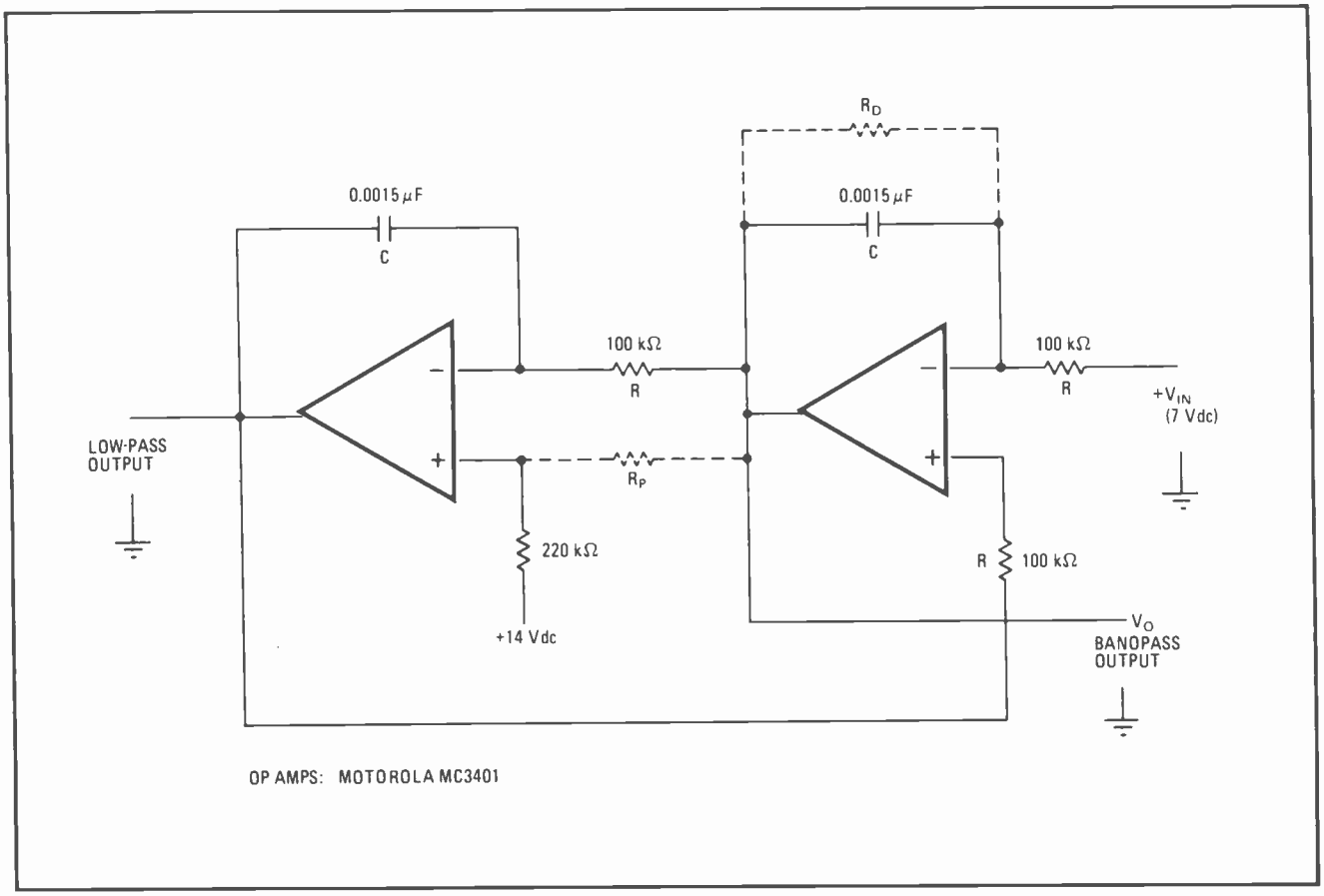
$$\omega_o = 1/RC$$

For the circuit values shown here, the center frequency is approximatley 940 hertz. The filter's damping factor, and therefore its Q value, can be adjusted by resistors R_D and R_P. To increase the Q value, some positive feedback can be added through resistor R_P; to decrease the Q value, resistive damping can be added by means of resistor R_D. As can be seen from the gain curves drawn in the figure, the Q value rises to 260 from a nominal (undamped) value of 248 when a 10-megohm resistor is used for R_P. Or if a 1-megohm resistor is used for R_D, the filter's Q value drops to 9.3.

Since the circuit requires only half of a quad amplifier package, the remaining two op amps can be employed as another filter or for additional gain. The filter also provides a low-pass output. □



Eliminating an op amp. This state-variable active filter employs only two op amps, instead of the three normally required. The usual inverter amplifier can be eliminated because the two op amps are connected as difference integrators. To adjust the filter's Q, resistor R_D or resistor R_P can be added to the circuit. The gain curves show both damped and undamped responses for the filter.



Winking LED notes null for IC-timer resistance bridge

by James A. Blackburn
Wilfrid Laurier University, Waterloo, Ont., Canada

A resistance bridge that makes use of the popular 555-type IC timer operates without requiring the usual combination of a meter and an amplifier. Moreover, the circuit's sensitivity does not depend on the unknown resistance. And since a light-emitting diode is used for visual indication, there's no need to worry about shock-isolation for a meter movement. Two possible applications for the bridge are as a thermometer (where the unknown could be a thermistor) or as a photometer (where the unknown could be a photoresistor).

The color block in the diagram shows where unknown resistor R_X is inserted in the bridge. When the resistance of the dual potentiometer is increased, the brightness of the LED also steadily increases. Then, at a particular setting of the potentiometer (R_{POT}), the LED's brightness is suddenly halved. The ratio of R_{POT}:R_X at which this winking occurs is determined solely by the properties of the two IC timers.

The first timer ($TIMER_1$) operates in its astable mode and, therefore, is free-running. Its output (signal A) is low for a period of $T_1 = 0.693R_XC$ seconds and high for a period of $T_2 = 0.693(R_X + R_{POT})C$ seconds. The output from $TIMER_1$ is differentiated and then used to trigger the second timer ($TIMER_2$), which is operating in its monostable mode.

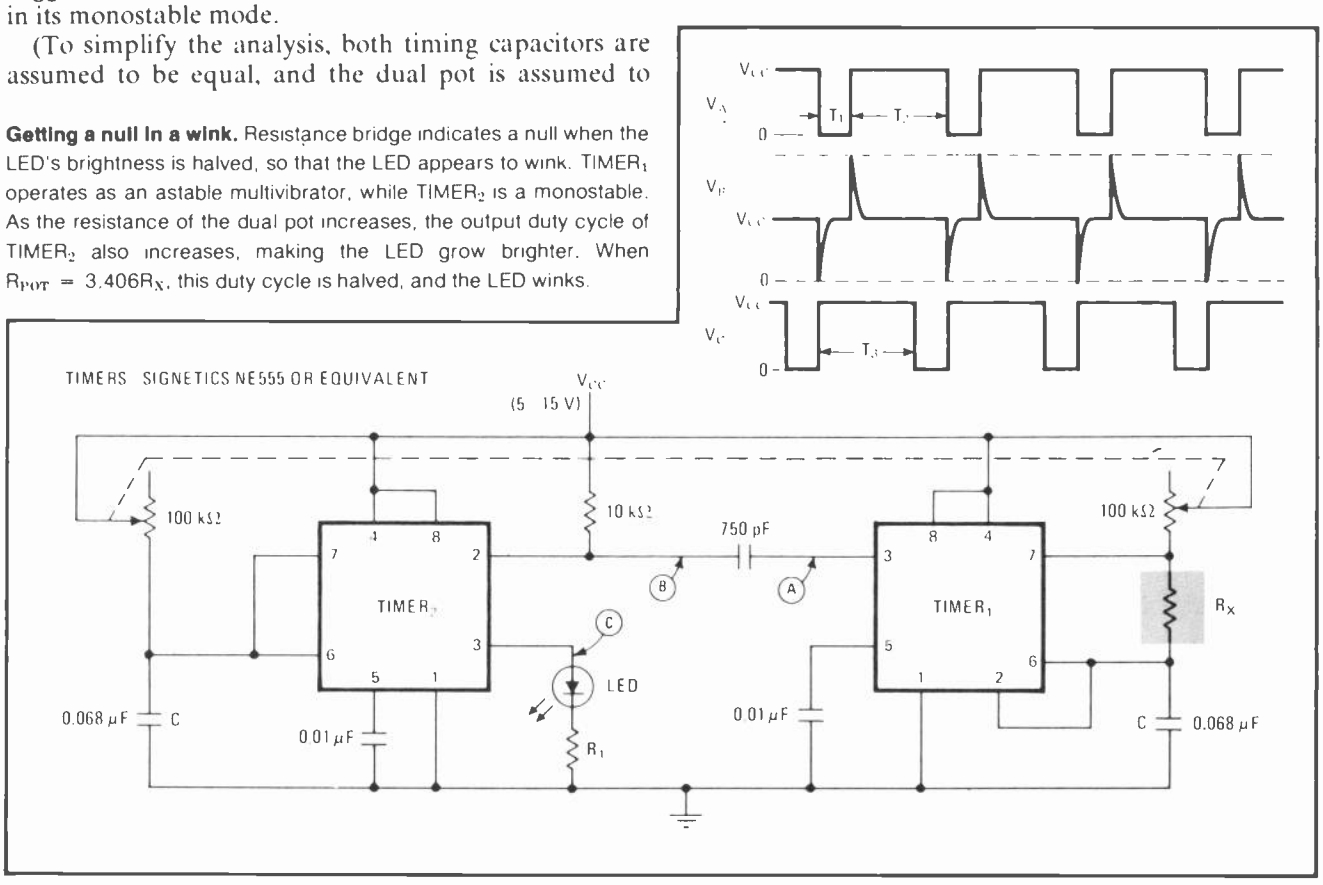
(To simplify the analysis, both timing capacitors are assumed to be equal, and the dual pot is assumed to track without error. In addition, the triggering spikes are considered to be of negligible width compared to period T_1.)

As R_{POT} is increased, the periods of signals A and B become longer, and the on-time of $TIMER_2$ ($T_3 = 1.1R_{POT}C$) starts to increase at a slightly faster rate. This means that the duty cycle of signal C is getting larger, and the LED will appear to grow brighter.

A closer look at the waveforms reveals that when period T_3 is just slightly less that $T_1 + T_2$, the duty cycle of signal C is nearly 100%. But when T_3 is slightly greater than $T_1 + T_2$, the duty cycle of the signal C drops to 50% and, at the same time, the frequency of this signal decreases to half the frequency of signal A. This happens because $TIMER_2$ locks out trigger pulses while its output is still high and, therefore, ignores all alternate negative-going spikes.

Further increases in R_{POT} cause the duty cycle of signal C to rise again slowly from 50% to a limiting value of 79.4%. The abrupt transition from 100% to 50% occurs when $R_{POT} = 3.406R_X$, making the calibration of this resistance bridge intrinsically linear. Circuit performance is limited by the desired upper and lower operating frequencies and the width of the triggering pulses.

For the component values shown, the circuit can operate over a fairly wide range of unknown resistance values—from 1 kilohm to 100 kilohms. The value selected for the LED's current-limiting resistor, R_1, depends on the supply voltage used. □



Getting a null in a wink. Resistance bridge indicates a null when the LED's brightness is halved, so that the LED appears to wink. $TIMER_1$ operates as an astable multivibrator, while $TIMER_2$ is a monostable. As the resistance of the dual pot increases, the output duty cycle of $TIMER_2$ also increases, making the LED grow brighter. When $R_{POT} = 3.406R_X$, this duty cycle is halved, and the LED winks.

Two-amplifier integrator extends timing performance

by Nabil R. Bechai
Leigh Controls Ltd., Ottawa, Ont., Canada

A simple integrator normally consists of a single operational amplifier and an RC network for setting up the desired time constant. Although uncomplicated, this approach can be troublesome if either a very small or a very large time constant is needed.

The integrator in the figure, however, makes it easy to obtain either short or long timing periods because the values of the timing components are scaled by a straight resistance ratio. The integrator's output voltage is given by:

$$V_{out} = -\frac{R_1}{RCR_2}\int V_{in}\,dt$$

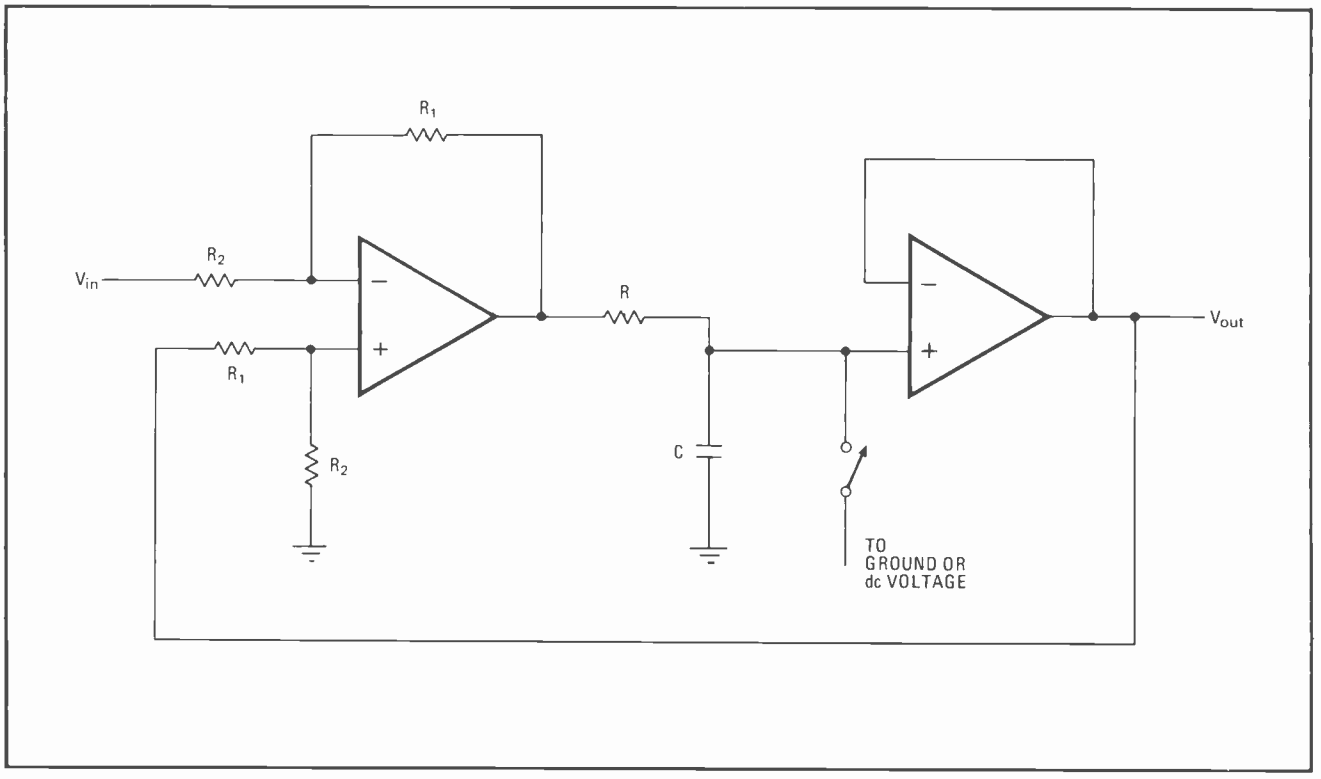
and its time constant becomes $(R_2/R_1)RC$. The circuit provides very good linearity when precision resistors having a tolerance of ±0.1% are used for resistors R_1 and R_2.

Although a second op amp is needed to build the integrator, the circuit offers some additional advantages. For example, it permits initial conditions to be established easily. One of the capacitor's leads goes to ground, and if one end of the switch is connected either to ground or to some dc voltage, the capacitor's initial condition can be set up as either zero or otherwise by simply closing the switch.

Furthermore, when the switch is activated, the integrator's output is not shorted, and the circuit's output op amp operates as a voltage-follower. In a conventional integrator, the initial-condition switch is generally placed across the capacitor, which is in the op amp's feedback loop. With the switch closed, then, the output of a conventional integrator is shorted to the op amp's inverting input.

The integration period of the two-amplifier circuit described here can be as short as 1 nanosecond or as long as 1,000 seconds. The bandwidth of the integrator depends on which op amps are used. For high-frequency operation, National's type LM318 op amp and RCA's type CA3100 op amp are recommended. □

Broad timing range. An extra op amp permits this integrator's time constant to be scaled by resistors R_1 and R_2 so that an exceptionally short or long timing period can be obtained easily. The time constant is $(R_2/R_1)RC$, rather than the usual RC alone. The desired initial condition for the capacitor is established by simply closing the switch, which can go to ground (for zero initial charge) or to some dc voltage.



Sure-fire ignition system safely limits engine rpm

by L.G. Smeins
Ball Brothers Research Corp., Boulder, Colo.

For a capacitive-discharge automobile ignition system to work properly, the SCR in the circuit must receive an accurate and stable triggering signal. The circuit shown not only produces a reliable SCR trigger, but also filters point-bounce, limits rpm, and buffers the point opening.

The trigger pulses for the SCR are generated by a conventional unijunction-transistor trigger circuit that contains a UJT having a high intrinsic standoff ratio (η). The values of resistors R_1 and R_2 are chosen to make $R_2/(R_1+R_2)$ less than η.

When the points close, the bipolar transistor turns off and the base-2 voltage (V_{B2}) of the UJT becomes approximately $12R_{BB}/(R_{BB}+1\ k\Omega)$, provided that resistor R_1 is much greater than 1 kilohm. (R_{BB} is the interbase resistance of the UJT.) Capacitor C_1 charges to a voltage that is slightly less than ηV_{B2}.

When the points open, the bipolar transistor saturates, pulling V_{B2} to about 6 V and raising the capacitor's voltage to more than ηV_{B2}. The UJT now goes into avalanche, producing a voltage pulse across resistor R_3 that fires the SCR. The charging rate of capacitor C_1 limits the SCR's firing repetition rate, thereby providing point-bounce filtering and rpm-limiting.

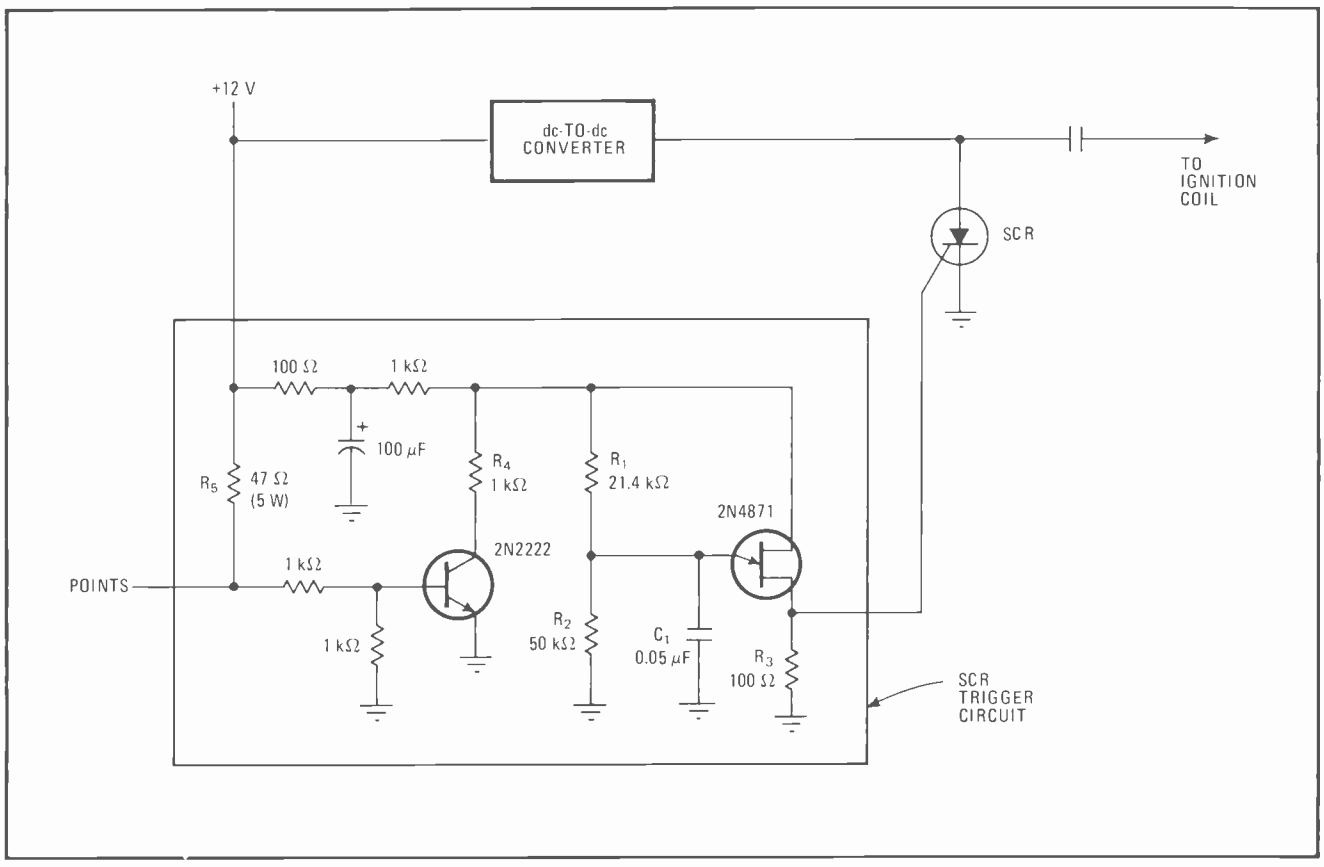
Suppose that an rpm limit of 6,000 is to be imposed on an eight-cylinder engine. For a type-2N4871 UJT, $\eta = 0.75$ and $R_{BB} = 6$ kilohms. Resistor R_1 can be set equal to 21.4 kilohms, and resistor R_2 to 50 kilohms, so that $R_2/(R_1+R_2) = 0.7$, which is less than η. The firing voltage for the UJT is 4.55 V, and capacitor C_1 must charge to this voltage 6,000 times per minute.

Two different charging rates occur because the target capacitor's voltage changes when the points close. If the point gap is adjusted properly, the ratio of the closed period to the open period is ⅔ to ⅓. Since the total period is 2.5 milliseconds, the points remain open for 0.833 ms and closed for 1.67 ms. The value required for capacitor C_1 can be found by computing capacitor voltage at the end of each of these periods. In this case, a value of 0.05 microfarad has been chosen for C_1.

The exact rpm setting needed for limiting can be obtained by adjusting the value of resistor R_4 slightly. When the limiting speed is reached, the ignition fires every other plug, in this way avoiding the severe transient loads associated with circuits that shut down completely to limit rpm.

Although the circuit shown here is for a point-driven system, it can be adapted easily for a magnetic or optical pickup by removing resistor R_5 and driving the bipolar transistor with a logic-level signal. □

Improving gas mileage. Efficient automobile combustion is provided by this capacitive-discharge electronic ignition, which features reliable SCR-triggering. The charging rate of capacitor C_1, because it determines how often the SCR is fired, provides rpm-limiting and point-bounce filtering. When the limiting speed is reached, only every other plug is fired to avoid the transient loading caused by a complete shutdown.



FET-controlled op amp permits wide dynamic range

by Henry E. Santana
Hewlett-Packard, Loveland Instrument Division, Loveland, Colo.

When a field-effect transistor is operated as a voltage-controlled resistor, it is usually limited to a relatively small dynamic signal-voltage range. This is due to the nonlinearity of its drain-source resistance over a wide range of drain-source voltage.

But a wide-range voltage-controlled amplifier can be realized if a pair of FETs is connected in the bridge configuration shown in the diagram. The inverting terminal of the operational amplifier is kept at virtual ground, permitting the range of each FET's drain-source voltage to remain small, regardless of how broad the actual signal-voltage range is. This also assures that the excursions of V_{DS} will remain well within the FET's pinch-off region.

The circuit's voltage-transfer function can be written as:

$$A_V = -(R_2/R_1) + N(R_1+R_2)/R_1 + NR_2r_{on}[1 - (V_{GS}/V_P)]$$

where r_{on} is the on-resistance of the right-hand FET, V_{GS} is the gate-source voltage, and V_P is the pinch-off voltage. Variable N represents a resistance ratio:

$$N = r_{on}/(r_{on}+R_1)$$

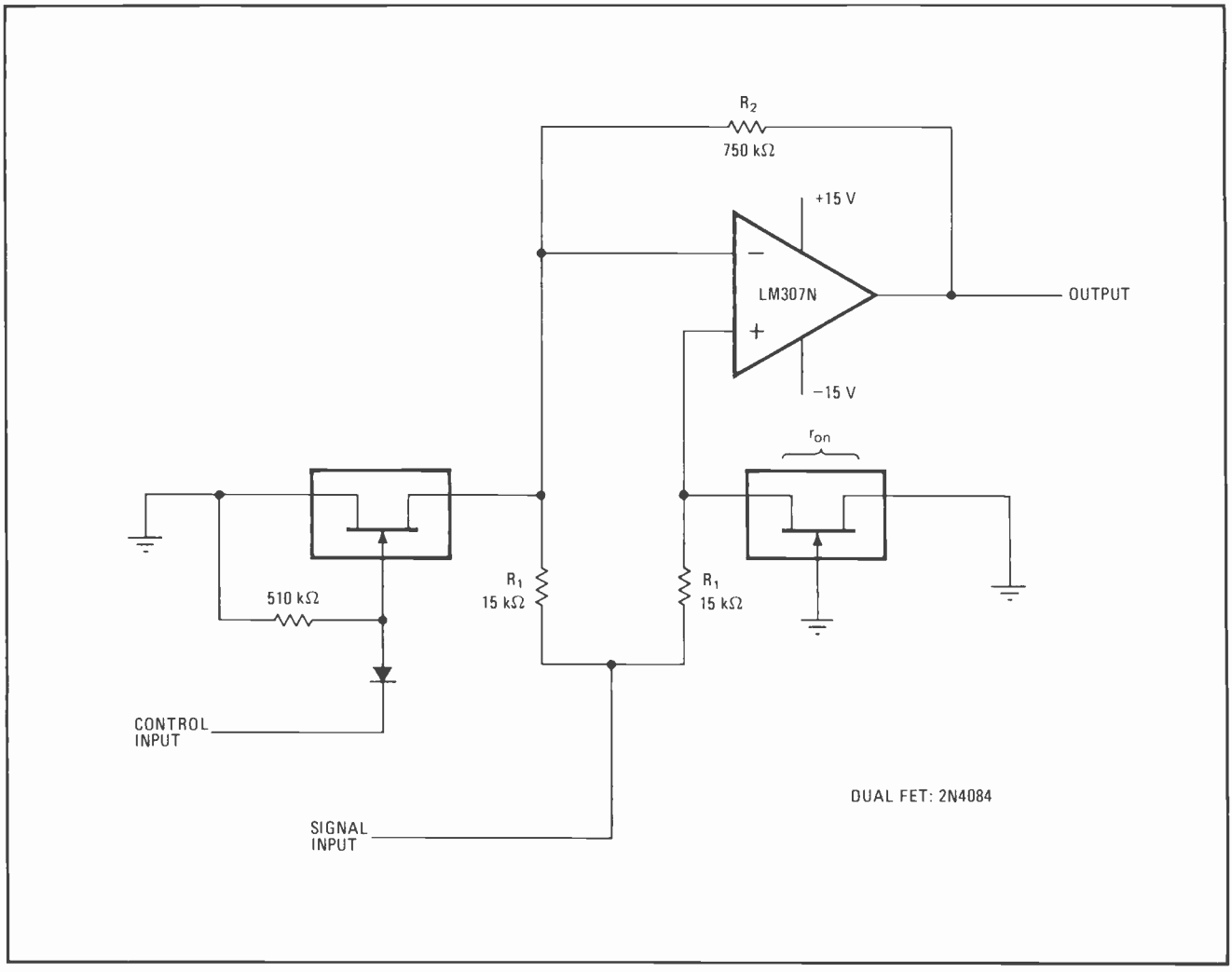
If N is very small, and r_{on} is much less than R_1, then:

$$AV = -(R_2/R_1)(V_{GS}/V_P)$$

Although N must be small, it must, nevertheless, be greater than zero for the circuit to work. The control voltage for the circuit can range from 0 to V_P, and the peak ac input-signal voltage is determined by $I_{DS}R_1$.

Applications for this voltage-controlled amplifier include automatic gain control, true rms conversion, amplitude compression, and signal modulation. □

Wide-ranging. Voltage-variable amplifier can operate over a broad range of input-signal voltages. The FETs, which function as voltage-controlled resistors, are wired in a bridge configuration. Their inherent resistance nonlinearity is avoided by limiting each FET's drain-source voltage range, no matter how large the signal voltage becomes. The op amp's inverting input is held at virtual ground.



IC logic units simplify binary number conversion

by Harvey F. Hoffman
Norden Division, United Aircraft Corp., Norwalk, Conn.

A variety of digital arithmetic processing applications require one arithmetic notation to be converted to another. Six of the most widely used conversions can be accomplished easily with a pair of medium-scale integrated circuits called arithmetic logic units. The table lists these six conversions and their associated rules.

The function chart for an arithmetic logic unit is given in Fig. 1. As an example of how to wire the ICs, consider circuit (a) in Fig. 2 for converting an 8-bit number in two's-complement notation to a number in signed-binary notation. The number to be converted is N, and the converted number is P. The eighth bit (N_7, P_7) is the sign bit, and the least significant bit is the first number bit (N_0, P_0).

The function-select inputs are $S_0 = 0$, $S_1 = S_2 = S_3 = 1$, and the mode (M) input controls the sign bit. The arithmetic function (when M = 0) that may be performed is A plus (A OR $\overline{B}$) with no carry (C_n) input to the first unit. (A and B are the input numbers.) The logic operation (when M = 1) for these same function-select inputs is A OR B, no matter the state of the first unit's carry input.

If number A is set to zero and the carry-in term is set to one, then to arithmetic operation (M = 0) is $\overline{B}$ plus 1, which is the binary representation of a negative number in two's-complement notation. With number A again set to zero, the logic operation (M = 1) gives an output of B.

Therefore, if the inverse of the sign bit is applied to the mode (M) input, the A inputs are held at zero and the number in two's-complement form is applied to the B inputs. The resulting output is then in signed binary notation. If only the magnitude of the number is required, the sign bit, P_7, should not be used.

This notation conversion is completely reversible. That is, the identical circuit may be used to convert

ARITHMETIC-NOTATION CONVERSION RULES

From signed binary to two's complement:
- If sign bit is negative, complement each number bit and add 1 to result.
- If sign bit is positive, output number equals input number.

From two's complement to signed binary:
- If sign bit is negative, complement each number bit and add 1 to result.
- If sign bit is positive, output number equals input number.

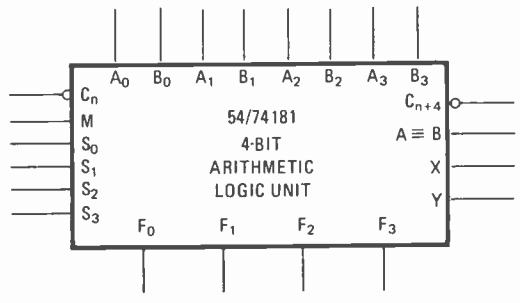
From signed binary to one's complement:
- If sign bit is negative, complement each number bit.
- If sign bit is positive, output number equals input number.

From one's complement to signed binary:
- If sign bit is negative, complement each number bit.
- If sign bit is positive, output number equals input number.

From two's complement to one's complement:
- If sign bit is negative, subtract 1 from number.
- If sign bit is positive, output number equals input number.

From one's complement to two's complement:
- If sign bit is negative, add 1 to number.
- If sign bit is positive, output number equals input number.

Notes:
- The sign bit is the most significant bit.
- A logic 1 in the sign bit location represents a negative number.
- A logic 0 in the sign bit location represents a positive number.

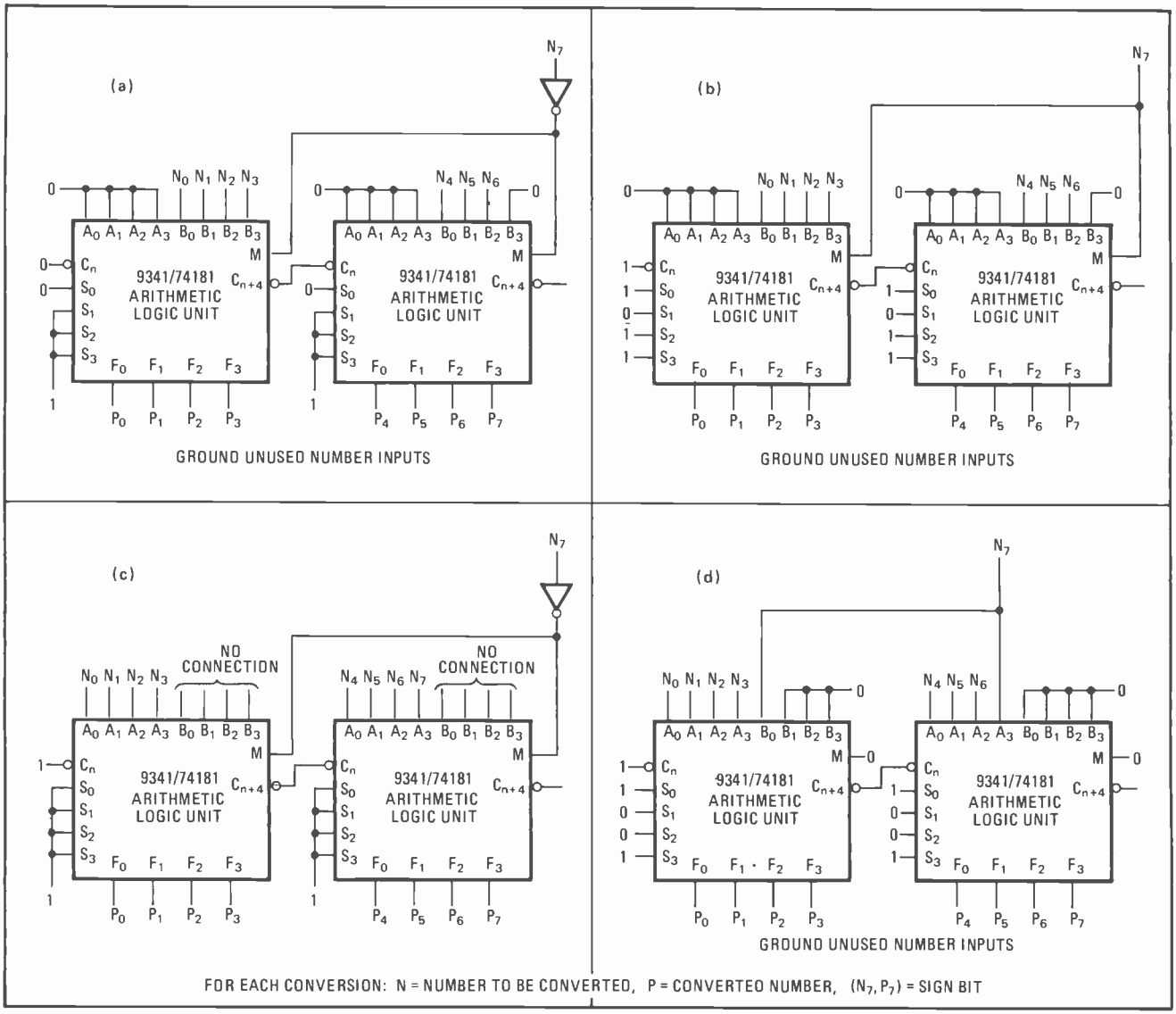


S_0 S_1 S_2 S_3	Arithmetic (M = 0, $\overline{C}_n$ = 1)	Logic (M = 1)
0 0 0 0	F = A	$F = \overline{A}$
1 0 0 0	F = A + B	$F = \overline{A + B}$
0 1 0 0	F = A + $\overline{B}$	$F = \overline{A}B$
1 1 0 0	F = minus 1 (2's comp.)	F = Logic 0
0 0 1 0	F = A plus A$\overline{B}$	$F = \overline{A\overline{B}}$
1 0 1 0	F = A$\overline{B}$ plus [A + $\overline{B}$]	$F = \overline{B}$
0 1 1 0	F = A minus B minus 1	$F = A \oplus B$
1 1 1 0	F = A$\overline{B}$ minus 1	$F = A\overline{B}$
0 0 0 1	F = A plus A$\overline{B}$	$F = \overline{A} + B$
1 0 0 1	F = A plus B	$F = \overline{A \oplus B}$
0 1 0 1	F = AB plus [A + $\overline{B}$]	F = B
1 1 0 1	F = AB minus 1	F = AB
0 0 1 1	F = A plus A (2 × A)	F = Logic 1
1 0 1 1	F = A plus [A + B]	$F = A + \overline{B}$
0 1 1 1	F = A plus [A + $\overline{B}$]	F = A + B
1 1 1 1	F = A minus 1	F = A

1. Functional capability. The operation of an arithmetic logic unit is outlined in the table for all possible selection (S_0, S_1, S_2, and S_3) inputs. The input numbers are A and B, and the output number is F. When the unit's mode (M) input is low, it produces the arithmetic function given in the middle column. When the mode input is high, a logic operation takes place, as indicated in the right-hand column.

from signed-binary notation to two's-complement notation.

The wiring connections for the four other conversions listed in the table are also shown in the figure. Circuit (b) is for converting from one's-complement notation to signed-binary notation, or vice versa. Circuit (c) is for converting from two's-complement notation to one's-complement notation. And circuit (d) is for converting from one's-complement notation to two's-complement notation. □



2. Number conversion. Two arithmetic logic units can be interconnected to change a number's arithmetic notation. The circuit of (a) converts two's-complement notation to signed-binary notation, or vice versa; circuit (b) converts one's complement to signed binary, or vice versa; circuit (c) converts two's complement to one's complement; and circuit (d) converts one's complement to two's complement.

Storing computer data with a cassette recorder

by Richard Eckhardt
Massachusetts Institute of Technology, Cambridge, Mass.

Two simple interface circuits permit data from a teletypewriter to be recorded and played back on a portable cassette tape recorder. This means that a conventional tape recorder can be employed as a compact reusable storage device for minicomputers, with a teletypewriter operating as the only input/output equipment. And remember that a single 120-minute cassette will hold as much information as 600 feet of paper tape.

Teletypewriter data is transmitted at the rate of 10 characters per second (110 bits per second), a frequency that is far too low for most audio recorders. Therefore, the data is converted to tone bursts at a frequency the recorder can use. On playback, the tone bursts are detected, and the original data format is reconstructed.

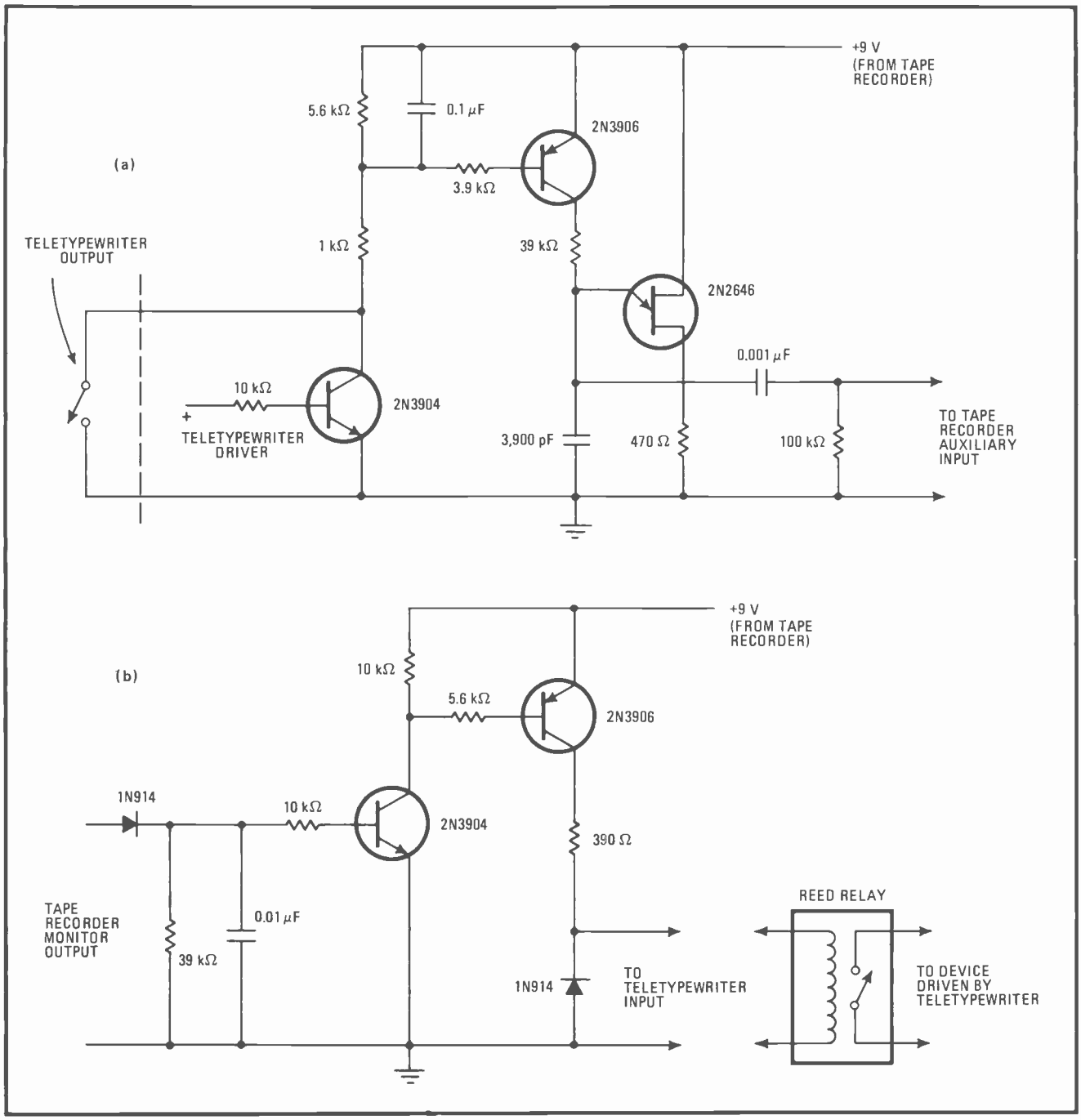
The teletypewriter-to-recorder interface circuit (a) can be driven either directly by the teletypewriter output or by the circuitry that drives the teletypewriter.

The output of a teletypewriter resembles the opening and closing of a switch. In the interface circuit, this switching waveform is first filtered slightly to remove bounce, and then it is used to gate a unijunction oscillator. If a teletypewriter driver is used instead as the input device, its drive current is fed to the base of a transistor that simulates the teletypewriter's switching action.

The circuit's output is a sawtooth waveform having a frequency of 6 kilohertz. It is applied to the recorder's auxiliary input (high-impedance low-sensitivity input). If the recorder does not have this input, it can be simulated by placing a 470-kilohm resistor in series with the microphone input.

The recorder-to-teletypewriter interface circuit (b) detects the recorder's output, and then rectifies and filters it so that a positive voltage is developed whenever a tone is present. A bleeder resistor is placed across the recorder output lines to produce the proper decay when the tone is removed. This decay voltage is then used to turn on a two-transistor driver that operates the teletypewriter. The output of this detector circuit can also be used to drive a reed relay to produce switch closures like those of a standard teletypewriter output.

It should also be noted that both interface circuits run off of a 9-volt supply, which can often be taken from the recorder's battery pack. □



Economical minicomputer data storage. Interface circuits for an everyday cassette tape recorder enable the unit to record and playback teletypewriter information. The recording circuit (a) can be driven by either the teletypewriter itself or by a teletypewriter driver. The playback circuit (b) can drive the teletypewriter directly or interface with a relay driver. The recorder's battery can run both circuits.

Making music with IC timers

by Kenneth R. Dugan
General Telephone and Electronics, Clearwater, Fla.

The versatile 555-type IC timer has yet another application—as a poor-man's music synthesizer for playing the musical signature of simple songs. Two timers are needed: one generates the rhythm, while the other produces the tones.

The circuit shown is intended for use as an audible alarm for a telephone exchange; it plays the first 10 notes of "A Pretty Girl Is Like a Melody." With the CONTROL INPUT lead of $Timer_1$ returned to the V_{CC} supply line, the tune will recycle continuously. But if a relay or flip-flop is connected to this lead, the number of times that the tune recycles can be controlled.

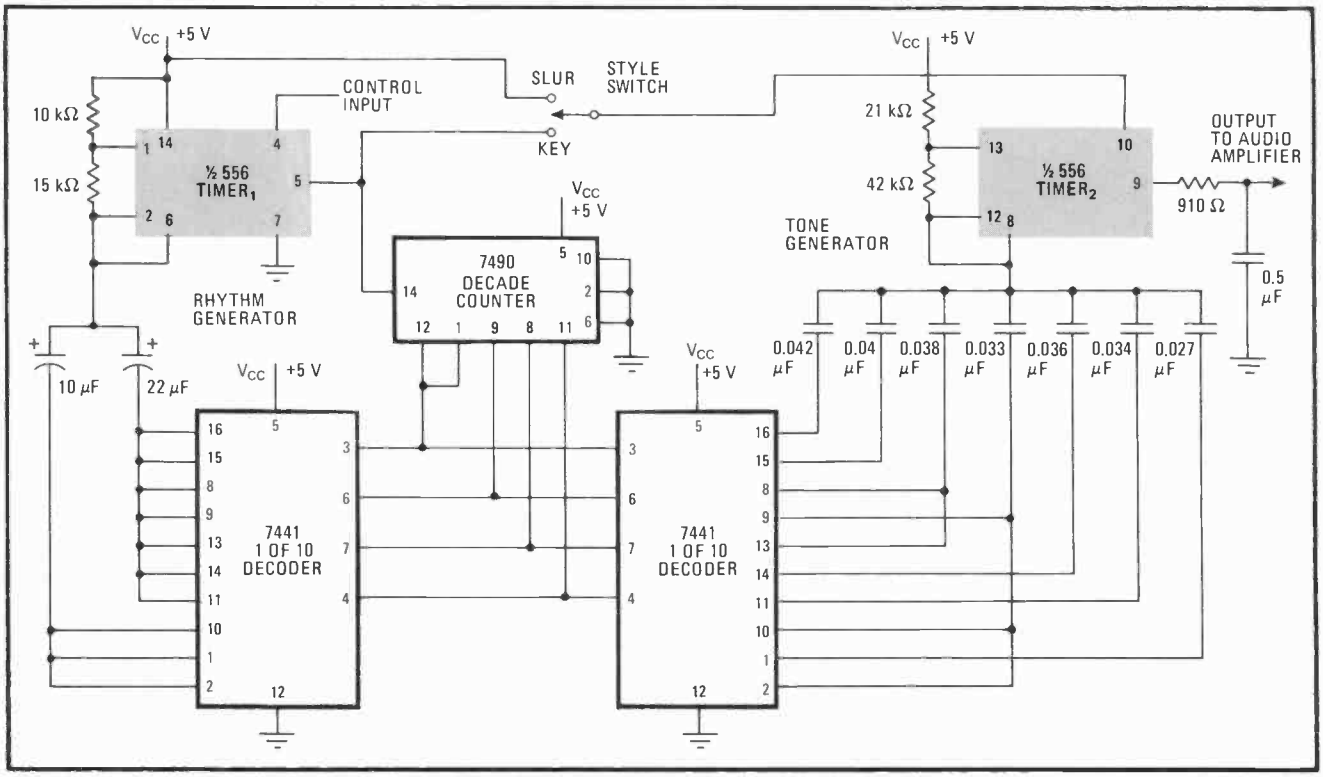
Since the output for $Timer_2$ is a pulse train having a duty cycle between 40% and 60%, a low-pass filter is used to soften the somewhat harsh audio quality of this waveshape. The setting of the STYLE switch causes the notes to either step or glide through the tune.

When used in conjunction with a diode bridge that detects the presence or absence of a ringing generator on the telephone line, the circuit can be programed to play a distinctive musical signature as a personalized telephone bell signal. Of course, many different combinations of resistors and capacitors can be used to obtain the desired music frequencies.

TONE-GENERATOR FREQUENCIES FOR "A PRETTY GIRL IS LIKE A MELODY"

COUNT	TONE CAPACITOR (μF)	FREQUENCY (Hz)
0	0.042	329
1	0.040	349
2	0.038	370
3	0.033	440
4	0.038	370
5	0.036	392
6	0.034	415
7	0.033	440
8	0.027	523
9	0.033	440

One less IC package is needed if a dual 556-type timer is employed, as done here, instead of two individual 555-type timers. □



Tuneful timers. This music synthesizer, which relies on two IC timers, can play a simple 10-note song. $Timer_1$ generates the rhythm for the tune, while $Timer_2$ generates the tones. If the CONTROL INPUT is tied to the supply line, the tune recycles continuously. The position of the STYLE switch determines whether the tones are played individually or blended. This circuit plays "A Pretty Girl Is Like a Melody."

Schottky diode pair makes an rf detector stable

by Roland J. Turner
AEL Communications Corp., Lansdale, Pa.

If broadband rf detection is to be efficient at low signal levels, detection thresholds must be stable—a design goal achievable with a pair of matched Schottky diodes. The diode-stabilized circuit shown here, for instance, maintains a detection stability of ±0.06 decibel over a temperature range of -20°C to +90°C for an rf drive level that is a 10th of that of a conventional detector.

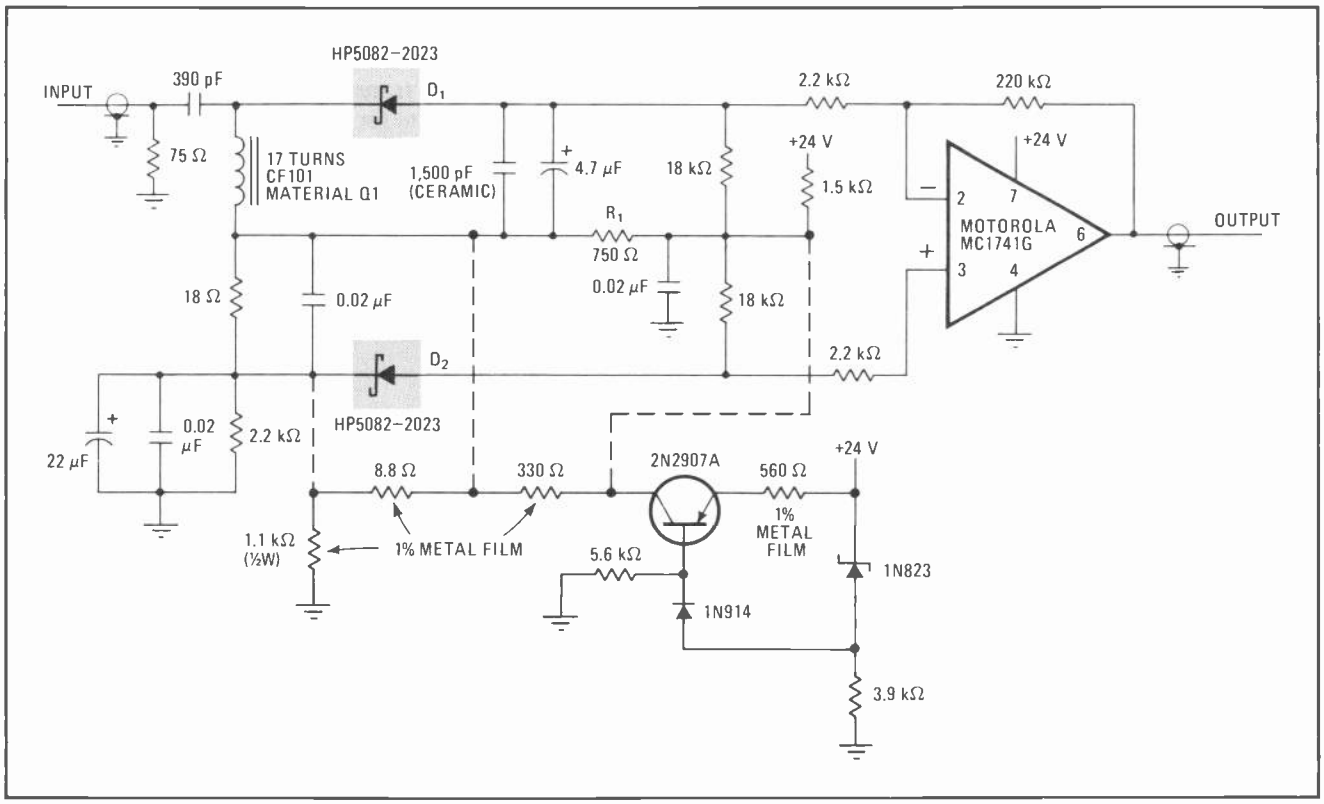
With such a circuit, the amount of rf circuitry required can be much reduced because accurate stabilized detection thresholds can be set for low rf drive levels. Also, the circuit's temperature stability and detection efficiency permit the realization of a sensitive receiver—one that can have a high video gain as well as a low rf gain.

Normally, it is hard to achieve high detection efficiency at a low rf drive level while keeping detection efficiency constant over a wide temperature range. This is because of the nature of the forward blocking voltage of a diode. For example, at room temperature, a silicon diode has a forward voltage of about 500 millivolts and a temperature coefficient of 2 mV/°C, so that the forward voltage will vary considerably—from 370 mV at 90°C to 590 mV at -20°C.

The rf drive level needed to start the detection action must exceed the diode's forward blocking voltage so that load current may flow. However, since the forward voltage changes by 220 mV from -20°C to +90°C, the rf drive level required must vary accordingly to maintain detection action. The inherent detection efficiency, therefore, is low and strongly dependent on temperature, limiting the maximum video gain that may follow the detector.

The rf detector depicted here, though, solves these problems. The two Schottky diodes, D_1 and D_2, are matched to within 5 mV from 0.1 to 0.5 milliampere and are connected in a half-wave rf detector configuration. The dc bias developed across diode D_2 and resistor R_1 serves as an arming bias for the detector diode, D_1, establishing temperature tracking between the two diodes.

The voltage drop across resistor R_1 establishes a reverse offset bias on diode D_1, in this way setting a known rf threshold that the rf drive level must exceed before detection action takes place. And the voltage drop across diode D_2 acts as a temperature-dependent forward arming bias on diode D_1. The level of this arm-



Temperature stabilized. High-efficiency rf detector operates at low input drive levels over a wide temperature range. Matched Schottky diodes (D_1 and D_2) and a fixed rf threshold bias (via resistor R_1) permit the circuit to hold voltage detection stability to ±0.06 dB from -20°C to +90°C for a 55-mV input. Sensitivity to supply-voltage changes can be minimized by adding colored network (and omitting R_1).

ing bias tracks the forward blocking voltage of diode D_1 as the temperature changes.

Because of this temperature-compensating arming bias, it is possible to realize constant detection efficiency over a wide temperature range, in addition to a constant rf threshold detection level. For a constant rf input of 55 mV, the detection voltage developed by the circuit varies only 1.8 mV between −20°C and +90°C. Rf peak voltages as large as 80 mV can be detected quite efficiently.

The operational amplifier at the output of the circuit senses the detection voltage and translates it to a 12-volt level. This output voltage varies only 2.1% from −20°C to +90°C for a constant rf input drive. Here, the op amp's gain is 40 dB, a figure that can be safely increased to 50 dB without adversely affecting the output stability of the circuit.

The circuit's performance will be further enhanced if the detector is made insensitive to variations in supply voltage. This can be done by adding a current source (shown in color in the diagram). The current source keeps the rf threshold voltage constant, despite supply variations of ±0.5 V. In connecting this source, resistor R_1 must be omitted. □

Crowbar protection circuit senses load voltage directly

by Thomas E. Skopal
Acopian Corp., Easton, Pa.

The triggering point of the overvoltage-protection crowbar circuit for a power supply can be decreased without increasing the circuit's sensitivity to transients. The trick is to have the crowbar circuit sense the voltage across the load, rather than the output voltage of the power supply, as is usually done.

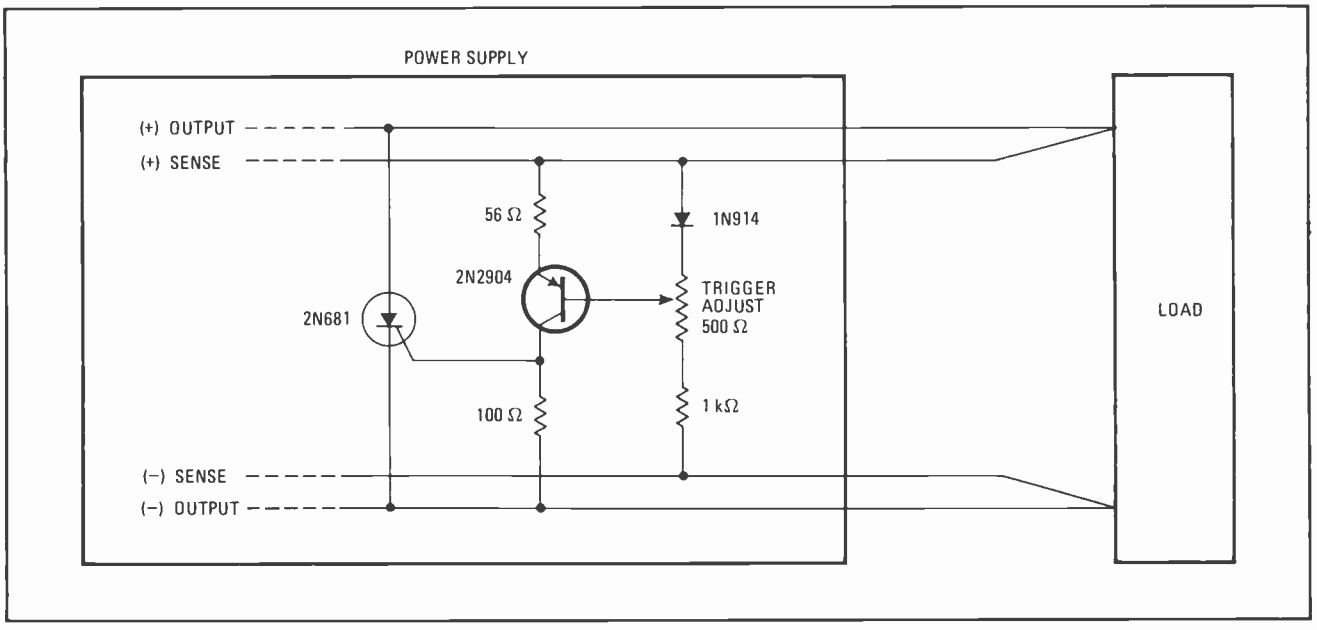
To provide maximum protection, a crowbar circuit is generally set reasonably close to the operating voltage required by the load. Typically, a compromise setting of about 15% above the load's operating voltage is chosen, because commonly encountered transients may cause spurious crowbar triggering and interfere with normal system operation if a tighter differential is used.

However, when voltage drops in the supply's output wiring exceed 2% or 3% of the output voltage—a common occurrence with low-voltage, high-current logic supplies—the system designer is faced with a dilemma. If he compensates for these drops with an increase in power-supply output voltage, the differential will be reduced and the crowbar's sensitivity to transients increased. And if crowbar setting is increased to maintain the same differential, load protection is degraded.

This conflict can be resolved by using the four-terminal crowbar circuit shown in the figure. It senses the voltage across the load, much as a supply's remote-sensing connections may be used to automatically compensate for voltage drops caused by long wires.

The crowbar's triggering point is a function of the voltage seen by the load, as opposed to the output voltage of the supply, and it is unaffected by the amplitude of the wiring voltage drops. Since the sensing connections of the crowbar share the sense lines of the supply's regulator, no additional system wiring is required.

The diode in the circuit provides temperature compensation for the transistor. The component values given are appropriate for power supplies having outputs of 4 to 10 volts and of up to 20 amperes. □



Better protection. Crowbar circuit protects a power supply from overvoltages by sensing the voltage across the load, instead of the supply's output voltage, which is the usual approach. This means that overvoltage sensing will not be affected by wiring voltage drops, nor will there be an increased sensitivity to voltage transients. The components shown here are for a power supply of 4 to 10 volts at up to 20 amperes.

Simple gating circuit marks both pulse edges

by Ralph Tenny
Texas Instruments, Central Research Laboratories, Dallas, Texas

A bidirectional edge detector can be built from only two integrated-circuit packages—or with only one package if exclusive-OR gates are used. Applications for the circuit include triggering for event counters and frequency doubling for digital data communications.

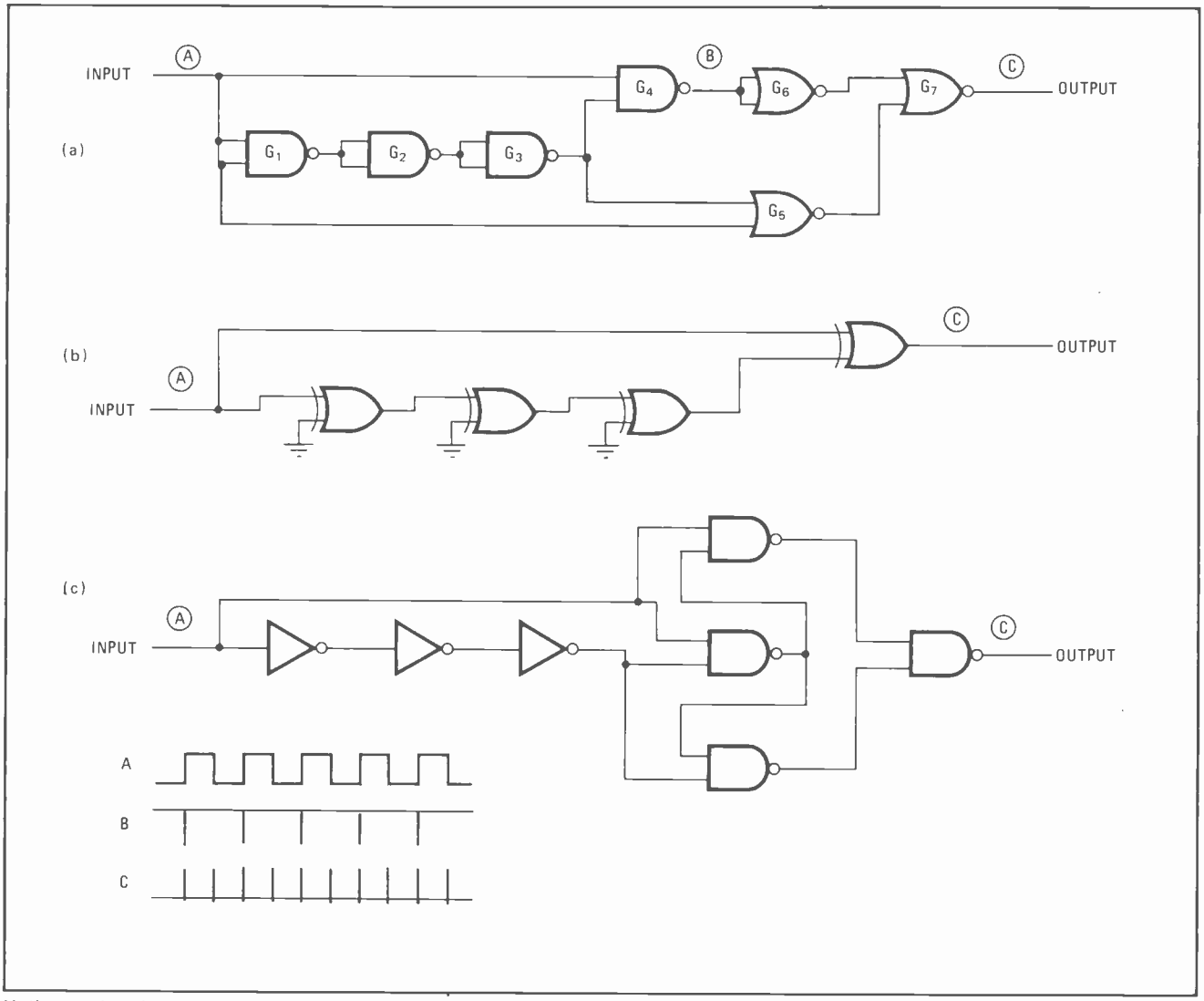
The configuration for the standard edge detector is drawn in black in (a). If NAND gates are used, as indicated here, the circuit responds to positive-going edges. If NOR gates are used, it detects negative-going edges.

When the input signal is low, the output of gate G_4 will be high. And when the input becomes high, G_4's output goes low one gate propagation delay later. Meanwhile, the input signal ripples through gates G_1, G_2, and G_3, causing G_3's output to go low after three gate delays. The output of G_4 then become high again one gate delay later. This means that G_4's output is a negative pulse that is three gate delays wide. The four gates, therefore, mark the positive-going edges of the input.

Adding three NOR gates to this standard circuit, as shown in color in (a), enables the circuit to mark both positive and negative edges. Gate G_5, together with gates G_1, G_2, and G_3, form a negative-edge detector. Gate G_6 simply inverts the output from gate G_4, while gate G_7 simply sums and inverts the detected edges.

The same dual edge detection can be obtained from a single quad exclusive-OR gate package when the gates are connected as indicated in (b). Or, an equivalent circuit can be constructed by hooking up three inverters and four NAND gates, as in (c).

The timing diagram shows the key waveforms for all the circuits. □



Noting each pulse-edge direction. Both positive and negative pulse edges can be detected with the same circuit by adding the three gates drawn in color in (a) to a standard unidirectional edge detector (drawn in black). If exclusive-OR gates are used, as in (b), the bidirectional edge detector requires only one IC package. Inverters and NAND gates, as in (c), can also provide the same circuit function.

Controlled current source is versatile and precise

by Jerald Graeme
Burr-Brown Research Corp., Tucson, Ariz.

A precision voltage-controlled current source can be made by placing a pair of complementary field-effect transistors in the feedback loop of an operational amplifier. The resulting circuit will have a differential input, as well as a bipolar output current that can be used to drive either grounded or floating loads. From signals of up to ±10 volts, the circuit develops a ±10-milliampere output, accurate to within ±0.01%.

Signal voltages are usually derived from control voltages, but sometimes it is better to derive signal currents from the control voltages for either testing or driving certain loads. For example, a voltage-controlled current source can provide a simple programmable bias current for transistor testing.[1] Or it can be used for resistance measurement, since contact resistance will not affect the test signal supplied by a current source. A current output is also needed for process-control instrumentation or for driving a meter or a dc torque motor.

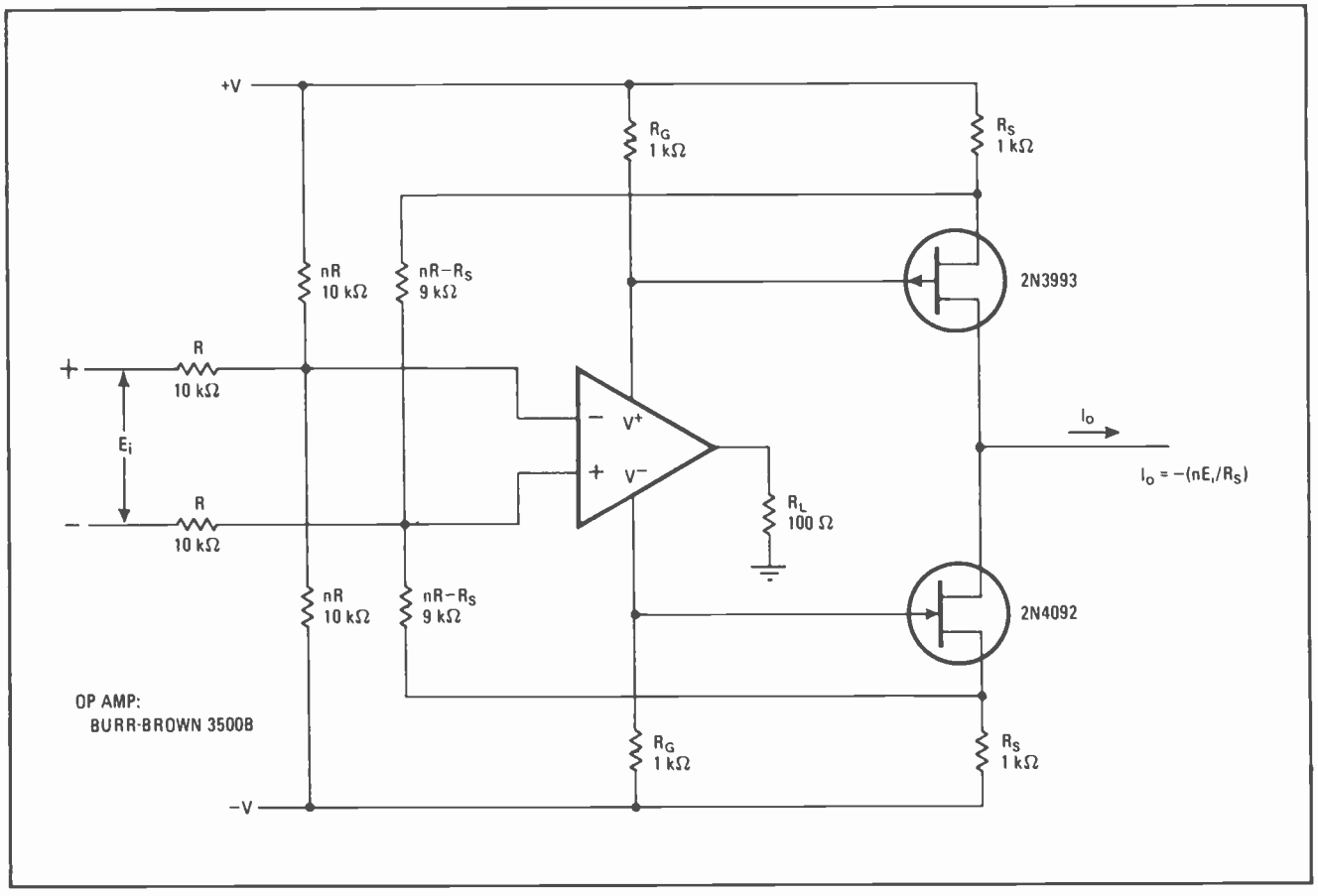
These varying applications may involve unipolar or bipolar output currents, single-ended or differential inputs, grounded or floating loads or sources, and varying degrees of accuracy. The circuit shown in the diagram can satisfy all of these requirements, and it is simpler than many previous not-as-versatile current sources.[1,2]

The circuit here consists of opposing FET current sources that are controlled by high-gain feedback around an op amp. The difference in FET currents produces the output current, and this difference current is controlled by summing the feedback, at the amplifier input, from the current-sensing source resistors (R_S). At feedback equilibrium, the sum of the two feedback signals is directly related to the differential input signal. The circuit's output current is given by:

$$I_o = -nE_i/R_S$$

where n represents the desired resistance-ratio factor.

Differential inputs and high power-supply rejection are provided by an attenuator network at the inverting amplifier input; it matches the feedback network con-



Current drive. Voltage-controlled current source can accept a single-ended or differential input, supply a unipolar or bipolar output, and handle a grounded or floating load or source. The difference current developed by the complementary FETs is sensed by resistors R_S and fed back to the amplifier input, where it is summed with the input signal voltage. Both FET gates are driven from the op-amp supply terminals.

nected to the other amplifier input. This is analogous to the matched input and feedback networks connected to an op amp to form the common difference amplifier.[2]

To simplify biasing and improve large-signal bandwidth, the gates of both FETs are driven from the op-amp supply terminals, rather than from the op-amp output terminal. Quiescent biasing for the FETs is obtained from the quiescent current drains of the op amp, and no level-shifting bias must be set up from the amplifer to the FETs.

Large-signal bandwidth is also improved by the reduced output swing required from the amplifier. Only a 1-volt swing is needed across amplifier load resistor R_L to obtain the rated output current, which is drawn through the supply terminals for maximum drive to the FETs.

Additionally, the lower amplifier output swing is not as greatly bandwidth-limited by the amplifier slewing-rate limit, as it is in other designs. Optimum bandwidth is achieved by making resistor R_L small enough to limit output swing without excessively lowering amplifier gain. Large-signal bandwidth is then limited by the amplifier's maximum common-mode swing rate.

The circuit's output current is controlled by the input voltage to within the accuracies of the resistors selected and within the gain-bandwidth and power-supply-rejection limitations of the op amp used. Most accuracy limitations caused by the FETs are overcome by the feedback, except for the small contributions from gate-drain leakage currents.

Output current is limited to the I_{DSS} level of the FETs but can be boosted by using the transconductance multiplying technique sometimes employed for common FET controlled current sources.[1] Output impedance is multiplied, through the feedback, from that of the FETs to the practical limit imposed by stray and parasitic effects—it is around 10^{12} ohms shunted by 10 picofarads.

By virtue of the circuit's differential inputs, common-mode signals are eliminated by a common-mode rejection that is adjustable to over 90 decibels. The primary common-mode-rejection limitations are the accuracies of the resistor ratios and the resistor matches, except for the noncritical match between the FET gate resistors (R_G).

The common-mode rejection can be adjusted by trimming the input resistors. Prior to this adjustment, any desired nulling of dc offset voltage should be performed by trimming the resistors denoted as nR. □

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2. G. Tobey, J. Graeme, and L. Huelsman, "Operational Amplifiers—Design and Applications," McGraw-Hill, New York, 1971.

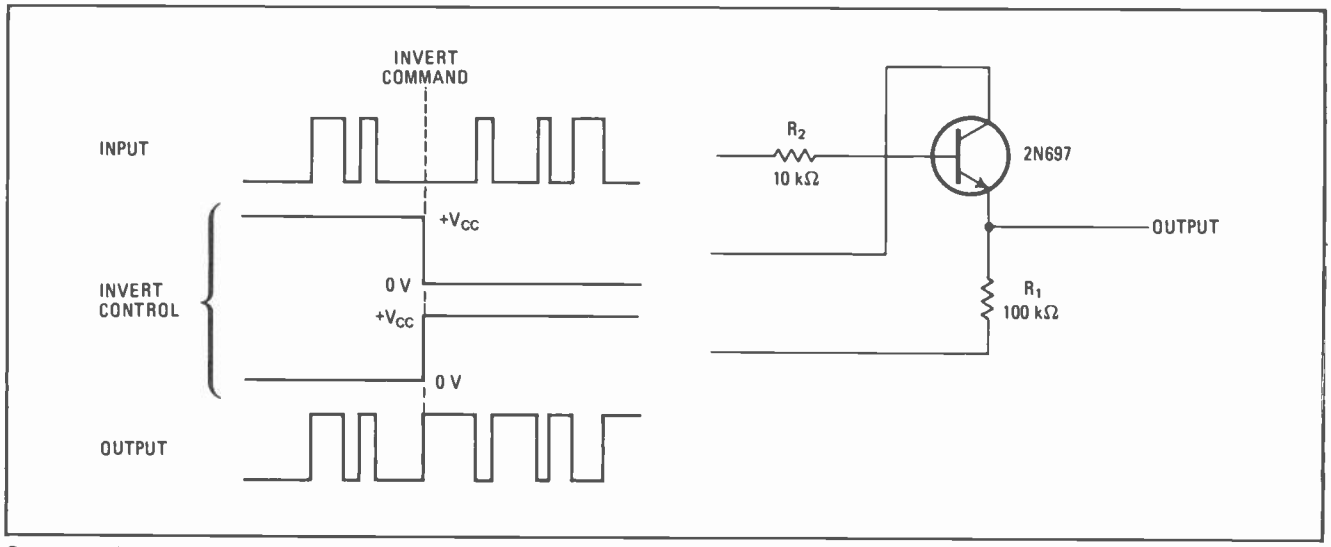
Single bipolar transistor inverts pulses on command

By Dale Hileman
Sphygmetrics Inc., Woodland Hills, Calif.

An ordinary bipolar transistor can be made to function as a command inverter—that is, it will pass a pulse signal without modifying the pulse, but it can invert the signal upon command. The command is a simple reversal of the polarity of the supply voltage.

To do this usually requires several gates, involving perhaps dozens of parts and interconnections. The command inverter shown here, however, requires only three parts: a single bipolar transistor and two ordinary resistors.

The key to this circuit's operation is that the role of a transistor's emitter and collector can be interchanged if the supply polarity is reversed. When the polarity of the invert control signal is normal, the transistor operates as an emitter-follower, so that the polarity of the output



Command Inverter. With normal supply polarity, this bipolar transistor operates as an emitter-follower, passing the input pulse train to the output without modifying it. But when the supply polarity is reversed, the transistor's emitter acts as its collector, and the transistor's collector acts as its emitter. Now the polarity of the input pulse train will be inverted at the transistor's output.

pulse train is the same as the polarity of the input pulse train.

The invert command reverses the polarity of the supply voltage, making the transistor's collector act as an emitter and its emitter act as a collector. Now the circuit becomes an inverting amplifier, with resistor R_1 serving as the collector load resistor. Under this condition, resistor R_2 simply limits the transistor base current to a safe value.

Any general-purpose npn or pnp bipolar transistor may be used in the circuit, and the precision of neither resistor R_1 nor resistor R_2 is critical. This command inverter will work with virtually any value of supply voltage and any input pulse level that the transistor will tolerate. □

Norton quad amplifier can be a low-cost function generator

by P. Vlcek
Orbit Controls Ltd.,
Cheltenham, Gloucester, England

A versatile function generator that minimizes hardware as well as cost can be built with one of the newly introduced Norton quad amplifiers [*Electronics,* Dec. 6, 1973, pp. 116-120]. The price of the complete generator is less than $3, and the entire unit can fit on a circuit board as small as a 1½-inch square.

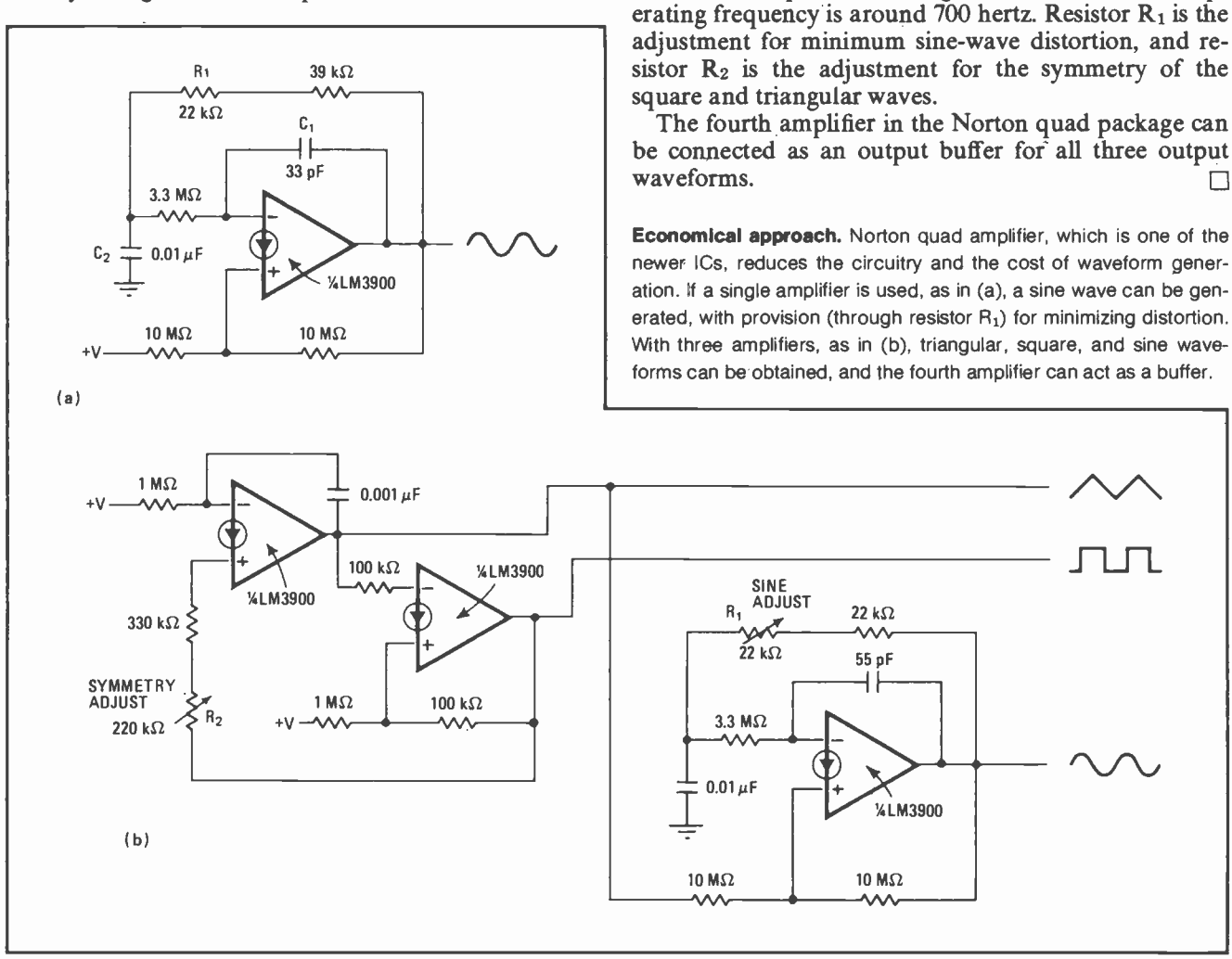
Only a single Norton amplifier is needed to obtain a sine-wave generator (a). When resistor R_1 and capacitor C_1 are omitted from this circuit, the resulting configuration is the standard one for a Norton-amplifier square-wave generator, with the timing current passing through capacitor C_2.

The addition of integrating capacitor C_1 to this square-wave generator produces a resonably accurate sine wave at the output. Resistor R_1, which helps to match the circuit's time constants, can be used to adjust the output sine wave for minimum distortion.

A similar circuit can be used to add a sine-wave output to the conventional hookup for a square-wave/triangular-wave generator built with two Norton amplifiers. As shown in (b), the triangular output acts as the input for the sine-shaper amplifier.

For the component values given here, the circuit's operating frequency is around 700 hertz. Resistor R_1 is the adjustment for minimum sine-wave distortion, and resistor R_2 is the adjustment for the symmetry of the square and triangular waves.

The fourth amplifier in the Norton quad package can be connected as an output buffer for all three output waveforms. □



Economical approach. Norton quad amplifier, which is one of the newer ICs, reduces the circuitry and the cost of waveform generation. If a single amplifier is used, as in (a), a sine wave can be generated, with provision (through resistor R_1) for minimizing distortion. With three amplifiers, as in (b), triangular, square, and sine waveforms can be obtained, and the fourth amplifier can act as a buffer.

Voltage regulator protects logic pull-up transistors

by Stephen F. Moore
Resdel Engineering Corp., Arcadia, Calif.

A monolithic three-terminal voltage regulator and a Norton-type operational amplifier can provide excellent short-circuit protection—particularly for the transistor that's providing active pull-up at the output of a logic circuit.

All too often, transistors operated in this way are destroyed when the logic output is inadvertently shorted to ground. Sometimes, too, protecting these transistors is further complicated because the logic must be run at 28 volts. An easy solution would appear to be a current regulator. But most current limiters have one of two drawbacks—either they introduce an unacceptably large voltage drop, or they create excessive heat in biasing resistors.

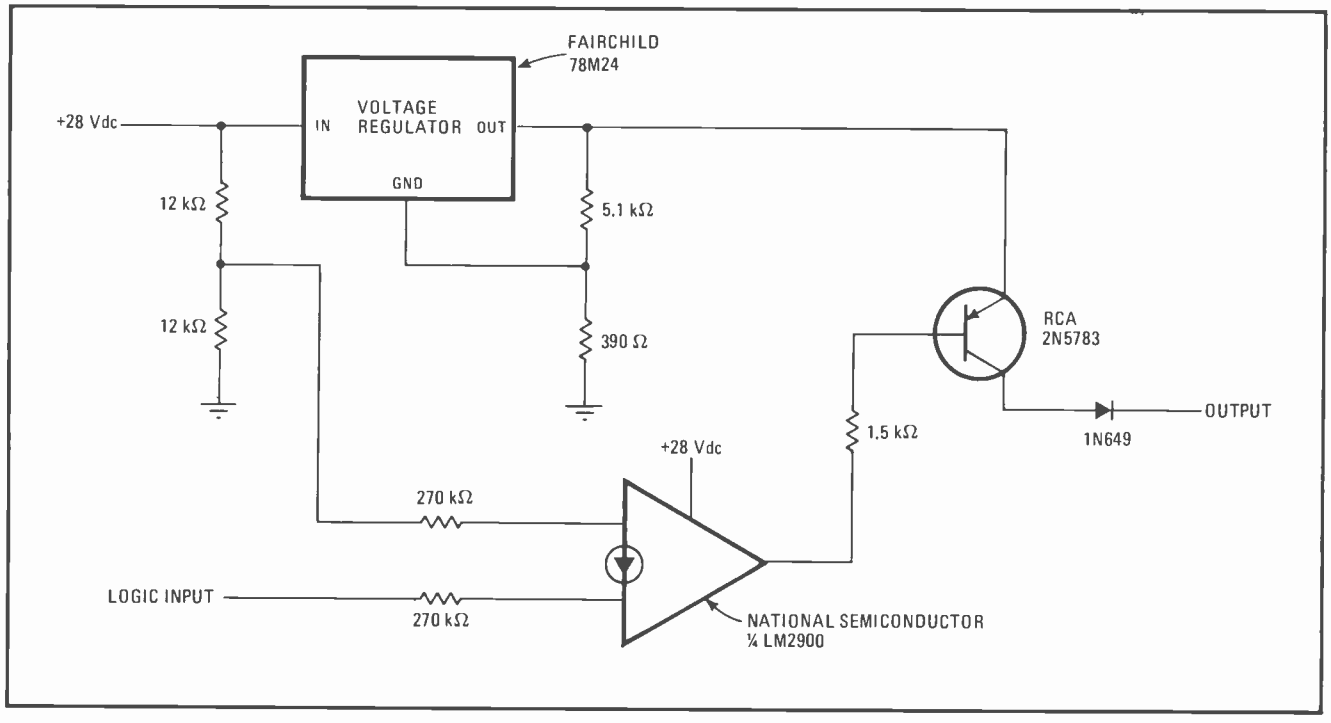
A monolithic three-terminal voltage regulator, however, has neither defect. When the regulator is not overloaded, the voltage drop across the device is only about 1.5 V. When it is overloaded, the heat it creates remains within an acceptable range. Usually, the highest output voltage that one of these regulators can supply is 24 V. But, if the device's ground terminal is biased at 2 V (depending on the manufacturer's recommendations), the output of a 24-V regulator can be increased to 26.5 V.

When connected as shown, the regulator provides current limiting in two ways. Through its internal circuitry, it acts as a surge-current limiter of about 2 amperes. It also operates as a thermal-current limiter that reduces that output voltage when the current demand becomes excessive. This keeps the power dissipated in the regulator from exceeding the maximum allowable limit. Here, the thermal-current limiting will start at around 400 milliamperes.

Limiting the current available for the active-pull-up transistor will prevent the transistor from being destroyed as long as it is kept in saturation or in cutoff. A Norton amplifier allows both these conditions to be met—its current-sinking capability is greater than 30 mA, and it has an active pull-up in its output circuit. Because of the voltage drop across the regulator, this active pull-up creates a reverse bias on the transistor being protected, eliminating the need for the transistor's pull-up resistor. Also, a Norton amplifier will work reliably with a single-ended power supply at, as well as above, a supply voltage of 28 V.

The diode at the output of the circuit protects the transistor from overvoltages. For example, this diode will guard against an overvoltage caused by an inductive kickback that could forward-bias the base-collector junction of the transistor. □

Guarding against short circuits. An IC voltage regulator and a Norton amplifier keep this active-pull-up transistor from being permanently damaged if the input logic signal is mistakenly shorted to ground. The regulator provides both surge-current limiting and thermal-current limiting. The Norton amplifier keeps the transistor either fully saturated or fully cut off, and the output diode protects against overvoltages.



Generating tone bursts with only two IC timers

by L. W. Herring
LWH Associates, Dallas, Texas

With very few external components, two IC timers can be made to function as a tone-burst generator that is useful for radio and telephone applications. In the circuit shown here, one timer controls the tone burst, and the other generates its frequency.

Normally, a tone-burst generator is built with three timers, two being required for the control function. Although a single timer in its delay mode could provide the initial time period, the second timer is required to generate the burst length and reset the first timer. Alternatively, in the astable mode, a single timer's output duty cycle could be adjusted for the quiet and burst periods, except for one thing—the time to the first burst would be almost twice as long as the time to subsequent bursts because the initial charging period of the timing capacitor is longer than later periods.

Nevertheless, a single timer can in a sense be fooled into providing the control function on its own if an RC network (resistor R_2 and capacitor C_2 in the figure) is added to the timer's ($TIMER_1$) threshold and trigger inputs. Of course, the larger primary timing network (resistor R_1 and capacitor C_1 in the figure) remains connected to the timer's discharge circuit.

$TIMER_1$ is set up as an astable oscillator. But its threshold inputs are kept high by the additional RC network (R_2 and C_2) for longer than it takes the timer's discharge circuit to completely discharge the main RC network (R_1 and C_1). This assures that the output period of $TIMER_1$ remains almost constant, no matter if the burst is the first one or the last one.

The period that $TIMER_1$'s output remains high can be approximated by the standard equation for delay-mode operation:

$$T_{on} = 1.1R_1(C_1+C_2)$$

The burst output time (when the output is low) can be adjusted to the desired value by the R_2C_2 network. This period is approximated by the equation for astable-mode operation:

$$T_{off} = 0.693R_2C_2$$

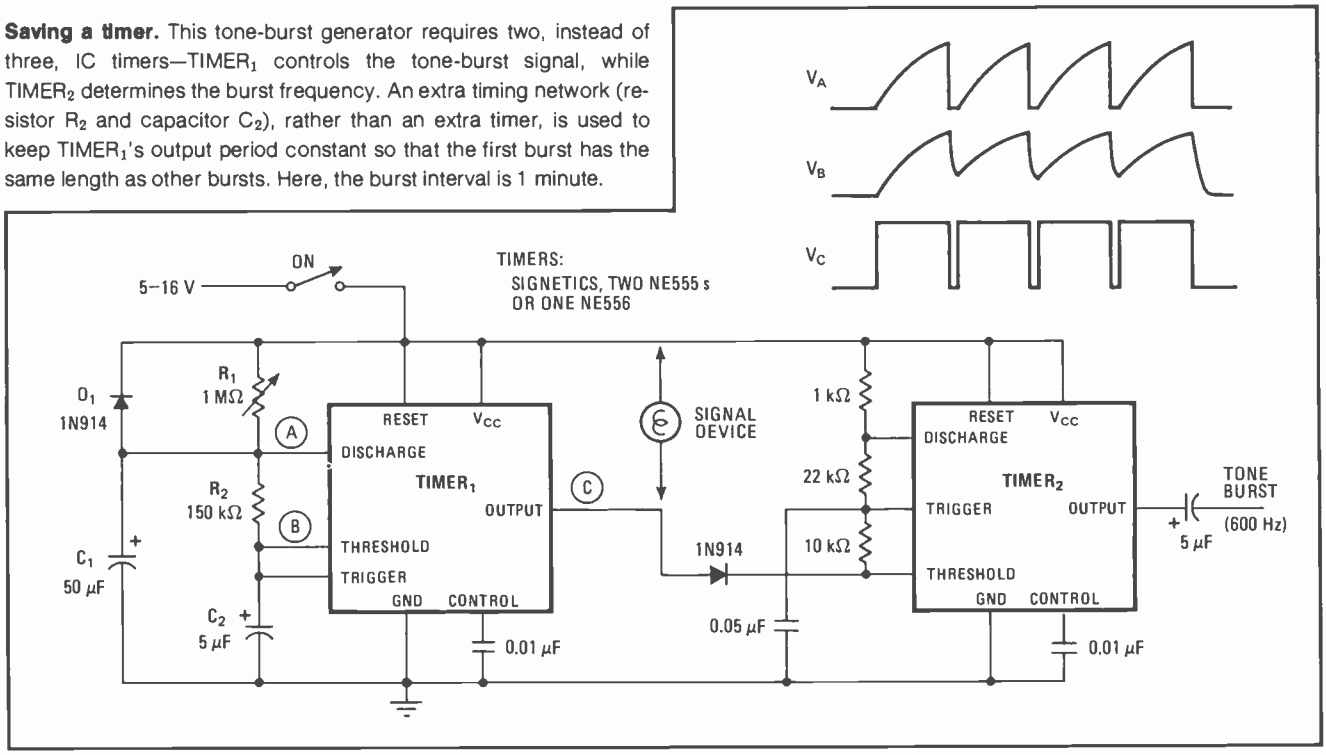
When the added time period (burst length) approaches or exceeds the main time period, the two timing networks interact.

For this circuit, the output of $TIMER_1$ remains high for 1 minute and goes low for a half second. The best way to activate the circuit is to switch the V_{CC} supply lead for the entire circuit. Diode D_1 assures that capacitor C_1 will be discharged after any partial periods.

The control timer ($TIMER_1$) can provide the output for a lamp, bell, buzzer, or other signaling device. (This timer's output must be used to sink the signaling device, which must also be wired to the supply line.) $TIMER_2$ operates as the tone oscillator, determining the frequency of the tone burst. The manner in which $TIMER_2$ is keyed eliminates the need for an intermediate device to invert the output of $TIMER_1$ to operate the reset lead of $TIMER_2$.

This simple tone-burst generator can be used as an audible timing reminder for long-distance telephone calls or for radio repeaters that have 3-minute shutdown timers. The same arrangement can be used to generate sampling pulses for a sample-and-hold circuit or for a serial-to-parallel data converter for Ascii-character detectors. □

Saving a timer. This tone-burst generator requires two, instead of three, IC timers—$TIMER_1$ controls the tone-burst signal, while $TIMER_2$ determines the burst frequency. An extra timing network (resistor R_2 and capacitor C_2), rather than an extra timer, is used to keep $TIMER_1$'s output period constant so that the first burst has the same length as other bursts. Here, the burst interval is 1 minute.



Simplifying sum-correction logic for adding two BCD numbers

by Robert D. Guyton
Mississippi State University, Mississippi State, Miss.

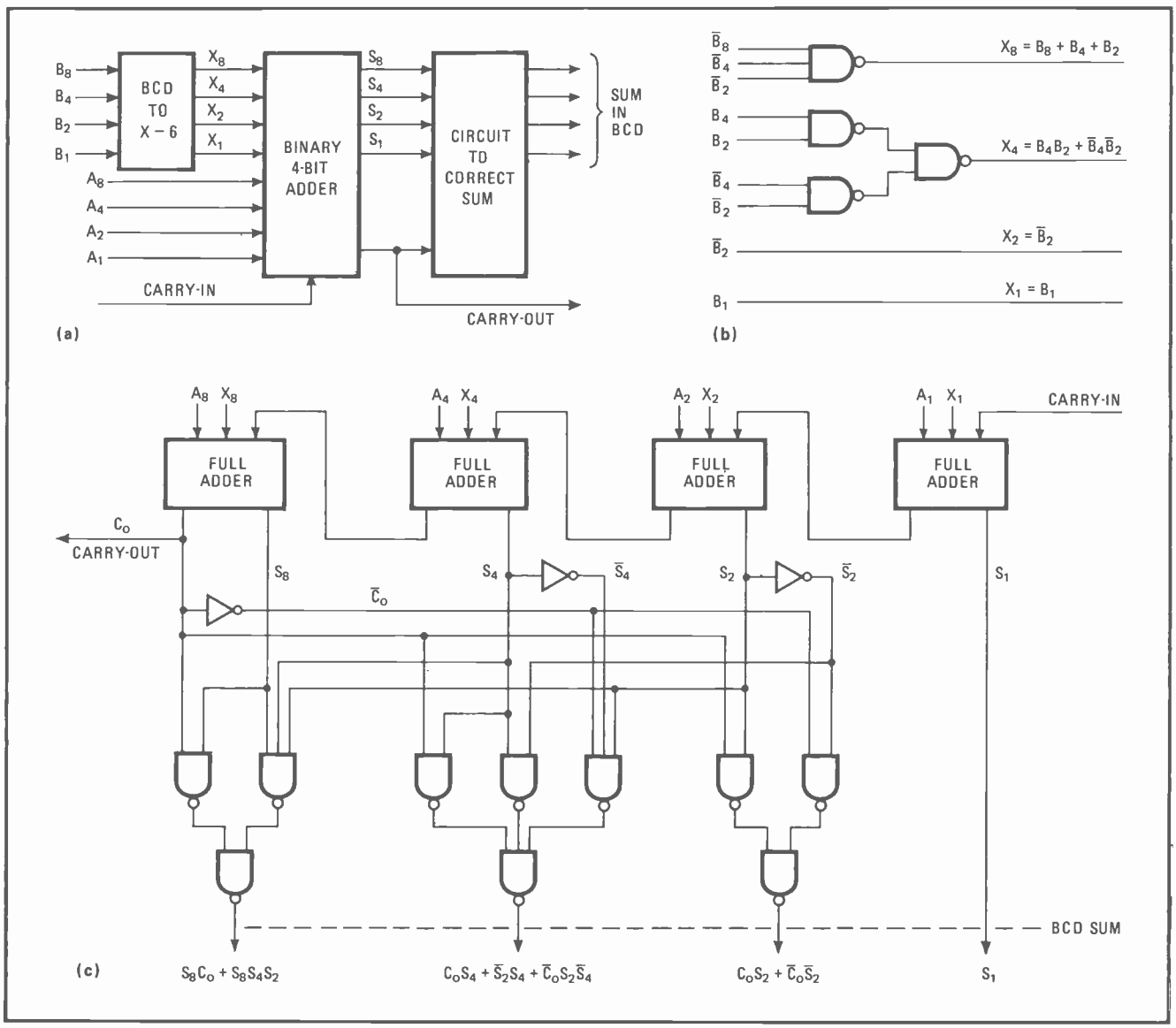
To add two numbers in binary-coded decimal form, much less logic hardware is needed if one of the numbers is converted to the excess-6 binary code before the addition is done. The other number remains unchanged.

The block diagram of (a) outlines the approach. One BCD input is converted to the excess-6 code by a second-level logic circuit, which is drawn in (b). This translated number and the unchanged BCD number are then added by a 4-bit binary adder. The resulting output carry is correct, but the sum must still be corrected—and can be corrected by a simple second-level logic circuit, rather than a multilevel type of logic circuit based on half and full adders.

The BCD-to-excess-6 translator circuit needs four NAND gates and three inverter gates. The rest of the over-all addition circuit is shown in (c): the four-bit binary adder requires four full adders, while the sum-correction circuitry requires 10 NAND gates and three inverter gates.

The complete excess-6 addition circuit, therefore, consists of 14 NAND gates, six inverter gates, and four full adders. As against an addition circuit based on excess-3 code conversion, that's a savings of six NAND gates, three inverter gates, one full adder, and two half adders. □

Conserving logic hardware. The circuit for adding two binary-coded-decimal numbers can be implemented with fewer devices by changing one of the BCD numbers to the excess-6 code format. When this conversion is done, simple logic gates can be used to perform the necessary sum correction. The figure shows the circuit's block diagram (a), the excess-6 code translator (b), and the complete circuit (c).



Synchronous noise blanker cleans up audio signals

by M.J. Salvati
Sony Corp. of America, Long Island City, N.Y.

Fluorescent lights, gas rectifiers, neon lamps, SCRs, and triacs all produce a substantial rf signal that often radiates through their power-line connections and interferes with nearby communications receivers. This type of radio interference desensitizes the receiver and makes the recovered audio signal very difficult to understand.

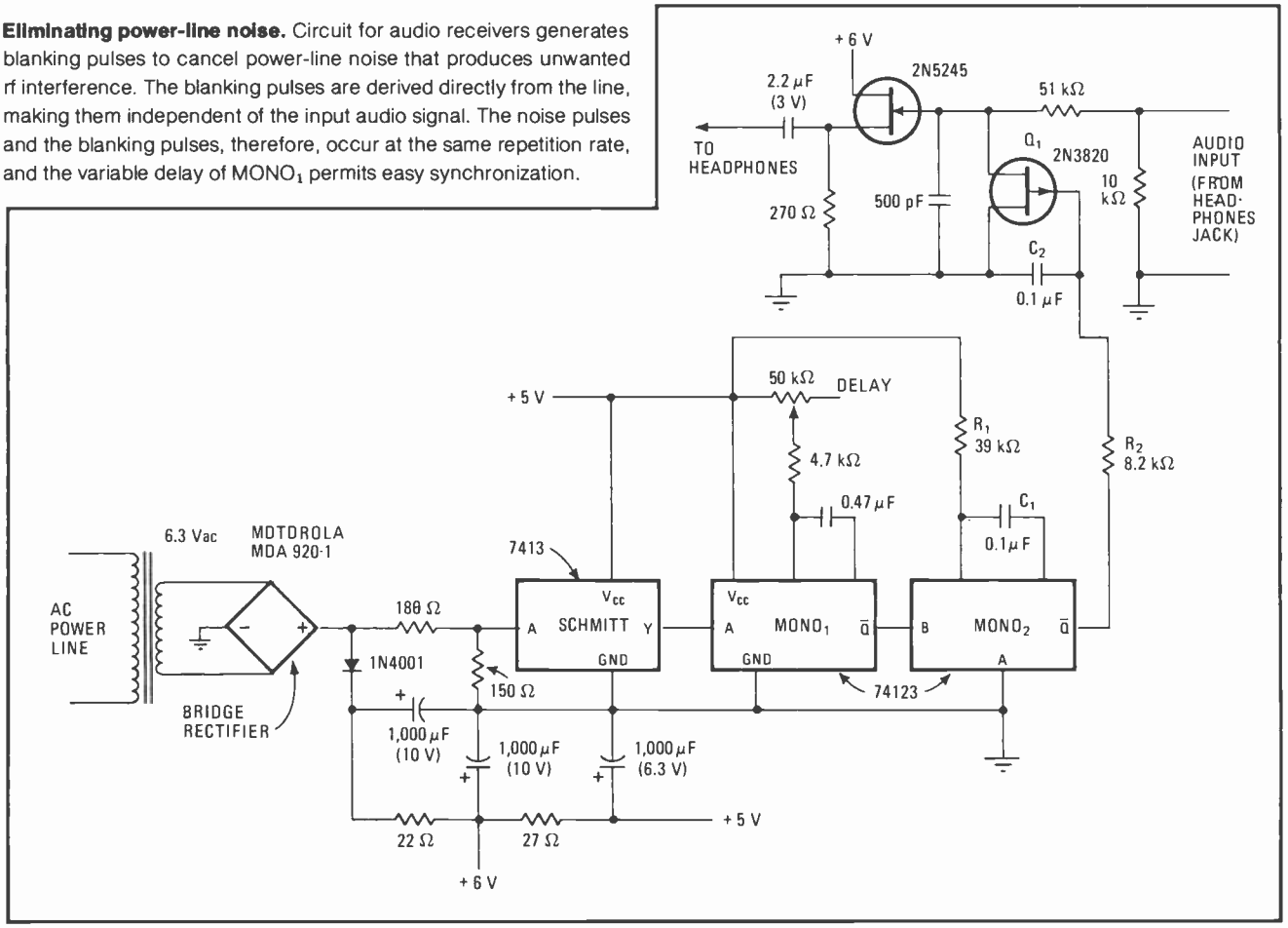
The circuit shown here significantly improves the audio intelligibility of a receiver by eliminating the noise pulses generated by a single dominant nearby noise source. The noise pulses are removed from the audio signal with only slight distortion. Moreover, since this noise-blanking circuit is not internally connected to the receiver, it can be moved from one receiver to another as needed.

The noise pulses produced by power-line radiation occur at a repetition rate of twice the local power-line frequency. Since the noise-blanking circuit is driven by the same power utility as the noise source, the output signal from the bridge-rectifier section of the noise blanker will have the same rate as the noise pulses.

The source of the blanking pulses, therefore, is independent of the input audio signal. The blanking pulses cause the FET gate (transistor Q_1) to conduct to silence the receiver. Since the blanking pulses are not derived from the input signal, their timing does not depend on the shape and rise time of the noise pulses, nor is it affected by the modulation characteristics of the desired signal.

The output from the bridge rectifier is shaped by a Schmitt trigger that drives a dual monostable multivibrator. The first monostable ($MONO_1$) delays the blanking pulse, which is produced by the second monostable ($MONO_2$), relative to the rectifier's output. The delay is variable so that the blanking pulse can be positioned to coincide with the noise pulse.

The width of the blanking pulse is determined by resistor R_1 and capacitor C_1. The fast rise time of the blanking pulse (from $MONO_2$) is slowed down by the low-pass filter formed by resistor R_2 and capacitor C_2, thereby minimizing the distortion of the recovered audio signal □



Eliminating power-line noise. Circuit for audio receivers generates blanking pulses to cancel power-line noise that produces unwanted rf interference. The blanking pulses are derived directly from the line, making them independent of the input audio signal. The noise pulses and the blanking pulses, therefore, occur at the same repetition rate, and the variable delay of $MONO_1$ permits easy synchronization.

Variable voltage source has independently adjustable TC

by Nathan O. Sokal
Design Automation Inc., Lexington, Mass.

A reference voltage source, which is built around a suitably stable general-purpose operational amplifier, offers an adjustable output-voltage magnitude, as well as an adjustable output-voltage temperature coefficient. Both the voltage magnitude and the temperature coefficient may be varied independently of each other.

The output voltage can be positive or negative, and it is continuously variable from 0.7 to 13 v. The temperature coefficient is also continuously variable, from −0.3%/°C to +0.3%/°C. For the circuit shown in the figure, the output voltage is positive. To obtain a negative voltage, the polarities of all the diodes and the supply (except to the op amp) are simply reversed.

The temperature coefficients of the zener-diode voltage, the resistance values, the op-amp input offset voltage, the op-amp input bias and offset currents, and the power-supply voltage need not all be zero. Rather, their values as functions of temperature must be stable with time and retrace well with temperature cycling. This is also true of the V-I characteristics of diodes D_1 and D_2. Moreover, these two diodes do not have to be matched.

If a narrower range of output voltage is adequate, part of resistance R_1 should be a stable fixed resistor. Likewise, if a narrower temperature-coefficient range is satisfactory, part of resistance R_2 should be a stable fixed resistor. Resistances R_1, R_2, and R_3 should be multi-turn potentiometers if both wide-range adjustment and high resolution are desired. Or they should be combinations of potentiometers and fixed resistors if a narrow adjustment range will do. Or they should be only fixed resistors when the desired output voltage and temperature coefficient need not be adjusted.

The fixed resistors used in this circuit should be film or wire-wound types for good long-term stability. A reference-type zener diode, such as the 1N4894, will improve voltage stability still further. All the resistors and semiconductor devices should be thermally coupled to each other for a good transient response to changes in ambient temperature.

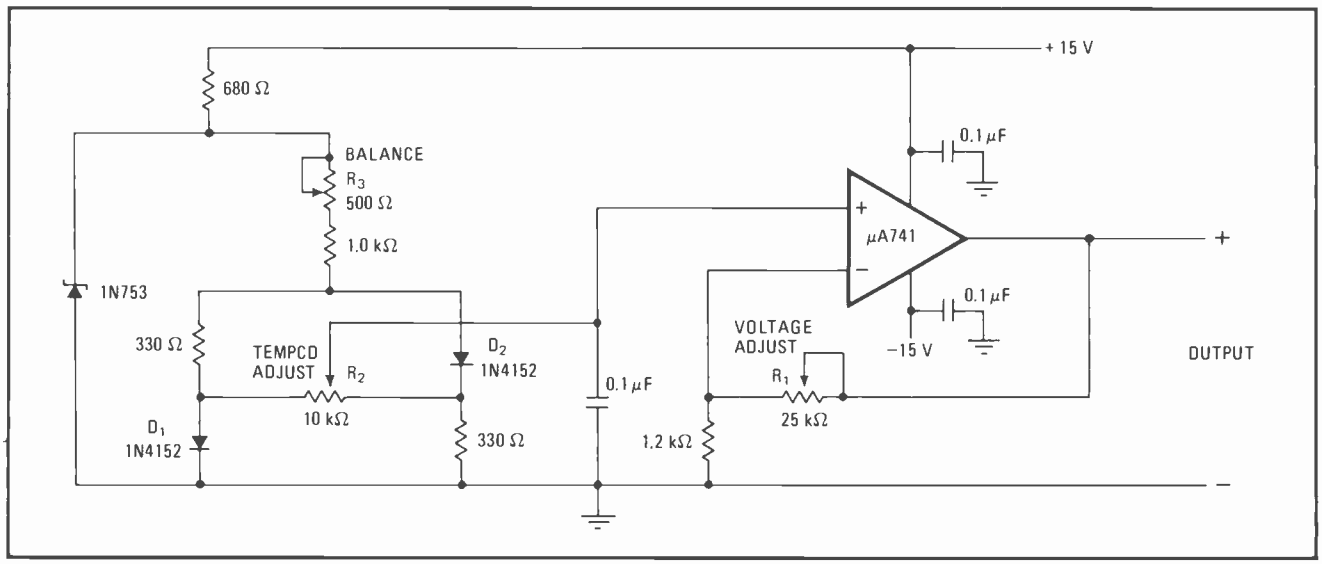
A simple procedure can be followed to adjust the circuit to desired operating conditions. First, set potentiometers R_1 and R_2 approximately at their mid-range positions. Then adjust potentiometer R_3 until the voltage across R_2 is zero at the reference temperature. This is the temperature at which it must be possible to adjust the temperature coefficient without changing the output voltage. Next, position potentiometer R_1 to give the desired output voltage at the reference temperature.

The last step is to adjust potentiometer R_2 for the desired temperature coefficient. This adjustment, which should not affect the output voltage at the reference temperature, can be made by heating or cooling the entire circuit to some temperature other than the reference temperature and then adjusting R_2 to obtain the desired output voltage at that temperature.

As a precaution, the circuit's output voltage should be checked for changing temperature. If it is not within the desired tolerance, repeat all the adjustment steps but the first one. Usually no such repetition will be needed.

More output current can be obtained from this reference voltage source by adding an npn power transistor, wired as an emitter-follower, at the circuit's output. The output from the op amp goes to this transistor's base, and resistor R_1 is then connected to the transistor's emitter, which becomes the circuit output. If the output voltage is negative, a pnp emitter-follower should be used. Without an emitter-follower, the output current can be as large as 10 milliamperes for most general-purpose op amps. □

Stable voltage source. The output voltage of this reference voltage source can be adjusted from 0.7 to 13 volts. And the circuit's output-voltage temperature coefficient is also adjustable, from −0.3%/°C to +0.3%/°C. These two adjustments are independent of each other. Potentiometer R_1 sets the output voltage, potentiometer R_2, the temperature coefficient, and potentiometer R_3, the reference temperature.



Switched frequency doubler provides multiple outputs

by Michael F. Black
Texas Instruments, Systems Analysis Section, Dallas, Texas

Frequency doublers that operate in the vhf/uhf range typically consist of complicated arrangements of saturated amplifiers, tuned circuits, and harmonic-suppression traps. With these circuits, a constant input impedance is usually difficult to sustain with changing temperature. Also, if the doubler must be switched, it is difficult to maintain circuit simplicity and high isolation ratios.

The switched frequency doubler shown here, however, provides high harmonic rejection, as well as constant input impedance, and it requires a minimum of adjustment. The circuit, which consists of a double-balanced mixer followed by a linear amplifier, accepts a 50-megahertz input of 5 dBm. In addition, it has provision for fast on/off switching and multiple 100-MHz outputs to 50-ohm loads.

The input power is split by the two-way power divider, HY1, and applied to the RF and LO ports of the mixer, M1. The mixer output, of course, is made up of several frequencies: twice the input frequency, the input frequency itself, the difference frequency (between the input and the local oscillator), and harmonics.

The difference frequency, which is dc, is shorted by the rf choke (L_1), and the input-frequency component is attenuated by the LO/i-f and rf/i-f isolation of the mixer. Transistor Q_1 is tuned to the doubled frequency, and the high-Q circuit in its collector loop further attenuates the unwanted frequencies to about 50-dB down. Through inductor L_2, the matching structure of this collector loop provides the only circuit adjustment.

Only three 50-ohm outputs are shown here, but more can be added. For each output, two capacitors (C_1 and C_2) transform the 50-ohm load up to a resistance value that output transistor Q_1 can drive satisfactorily. The reactance of inductor L_2 then tunes out the capacitance to present a high-value real load to Q_1's collector at the doubled frequency.

The value of L_2's reactance is:

$$X_{L2} = (⅓)(R_P/Q)$$

where R_P is the load resistance that transistor Q_1 sees, and Q is the circuit's figure of merit. The reactances of the transformation capacitors, C_1 and C_2, are also dependent on R_P and Q. They can be expressed as:

$$X_{C1} = [R_P/(1+Q_2)][Q - [(50/R_P)(1+Q^2) - 1]^{1/2}]$$
$$X_{C2} = 50/[(50/R_P)(1+Q^2) - 1]^{1/2}$$

Circuit Q is selected according to the harmonic rejection required. The higher the value of Q is, the higher the harmonic rejection will be, but the more difficult some component values may become to obtain. For the circuit given here:

$Q = 6$
$R_P = 1.5$ *kilohms*
$X_{L2} = 83$ *ohms at 100 MHz* $= 0.13$ *microhenry*
$X_{C1} = 222$ *ohms at 100 MHz* $= 6$ *picofarads*

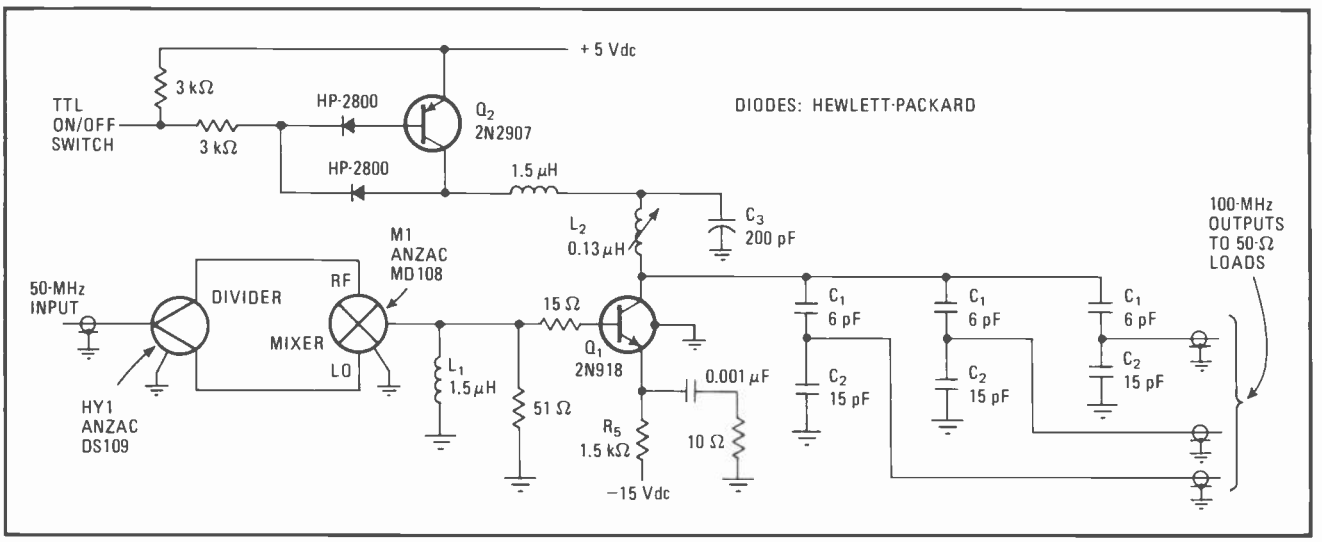
and:

$X_{C2} = 104$ *ohms at 100 MHz* $= 15$ *pF*

Each output of the circuit supplies a power level of +3 dBm at a frequency of 100 MHz.

Transistor Q_2 is a nonsaturating switch that is compatible with a TTL open-collector input. Together with its associated circuitry, transistor Q_2 switches transistor Q_1, providing the mutiple gated outputs. Switching times of well under 1 microsecond can be realized when an appropriate value is chosen for capacitor C_3. The circuit's on/off isolation is better than 50 dB. □

Rf frequency doubler. From a 5-dBm input at 50 megahertz, this switched frequency doubler develops multiple 3-dBm outputs at 100 MHz, seen by output transistor Q_1 so that the circuit can handle 50-ohm loads with relative ease. The doubler's only adjustment, inductor L_2, is used to tune out this added capacitance. Transistor Q_2 is used to switch transistor Q_1.



Electronic combination lock offers double protection

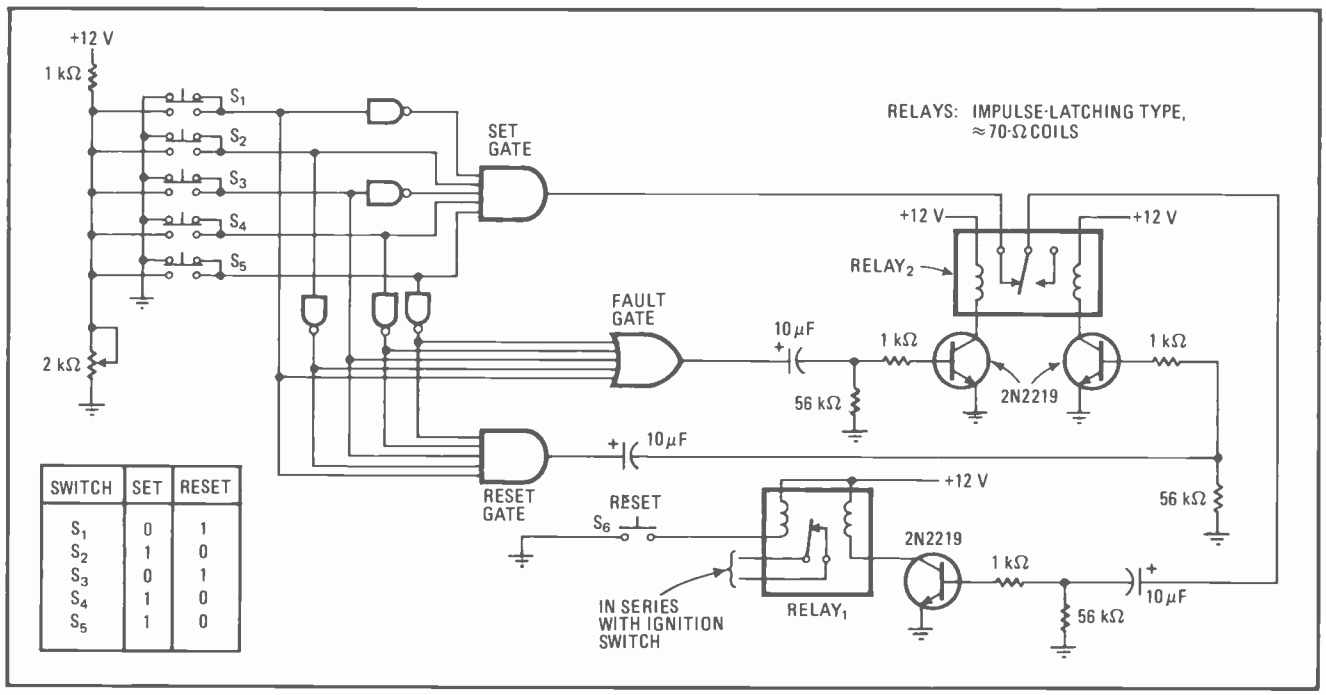
by Louis F. Caso
Bethpage, N.Y.

If you need a doubly safe lock, try the electronic combination lock shown here. It will not unlock unless the correct combination of switches is depressed, and if the wrong combination is chosen, the lock will not open until it is reset with another combination.

The circuit in the figure is intended for installation in an automobile, but it can be easily modified for other applications. When the correct combination of switches S_1 through S_5 is depressed, the output of the SET gate goes to logic 1, closing the contacts of $RELAY_1$. When the car's ignition is turned off, this relay should be reset (contacts opened) by using switch S_6.

To open (set) the lock, switches S_2, S_4, and S_5 are depressed simultaneously. If an error is made, the output of the FAULT gate goes to logic 1, and the contacts of $RELAY_2$ will open. When this happens, the lock must be reset before the opening combination can be used again. Switches S_1 and S_3 are depressed simultaneously to reset the lock.

Any secret combination of push buttons can be selected by arranging the switches as desired. For most applications, the multiple-input logic gates can be obtained by interconnecting standard dual-input gates. □



Safe and sound. To open this electronic combination lock, depress the correct combination of switches S_1 through S_5. But if an error is made, the lock must be reset with another switch combination before it can be opened again (The switches are depressed simultaneously.) The circuit shown here is for locking an automobile ignition, but it can be readily adapted for other uses.

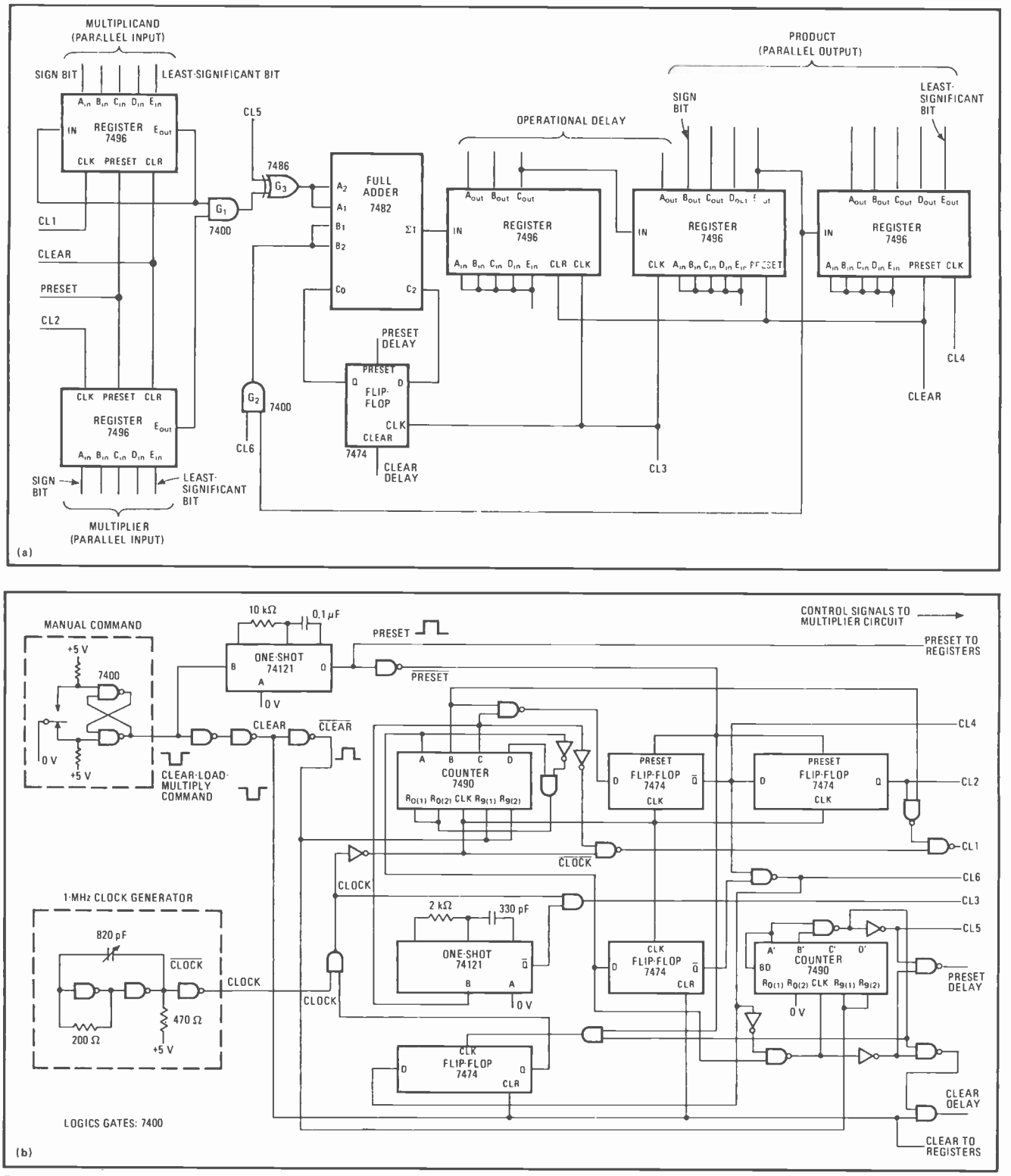
Serial digital multiplier handles two five-bit numbers

by T.K. Tawfig and H.L. Hvims
Allerod, Denmark

Because of the fast operating speeds of today's digital circuits, the serial type of digital multiplier can be regarded as a practical alternative to the parallel or serial/parallel type in many applications. The serial approach can mean a large savings in the number of ICs required to do the job.

The circuit shown is an expandable serial digital multiplier that can accept two 5-bit numbers in two's-complement form. It is useful in such applications as digital filters, signal correlators, and other digital systems that employ two's-complement notation. The multiplier circuitry is shown in (a), while the circuitry used to get the necessary control signals is shown in (b).

The multiplication process is started by a CLEAR-LOAD-MULTIPLY command, which is generated by a manual latch, and stops automatically upon completion. When this start command initiates the control sig-



Serial multiplication. The number of ICs needed to build this digital multiplier is minimized because the circuit performs the multiplication serially. The two 5-bit two's-complement input numbers, however, as well as the output number, are in parallel form. The multiplier circuitry is given in (a), and the control-signal circuitry in (b). The system is easily expanded to accommodate larger numbers.

nals, the two numbers to be multiplied—the multiplicand and the multiplier—are loaded into their respective registers.

Each bit of the multiplicand is gated by each bit of the multiplier through gate G_1. To obtain the final product, the partial sums are added to the partial products. Gate G_2 passes the partial sums, and gate G_3 provides an inversion when the flip-flop delay is preset. This inversion causes the multiplicand to be subtracted when it is gated by the sign bit of the multiplier. An additional shift register provides an OPERATIONAL DELAY for spreading the sign bit. The final product is available in parallel form from the two output registers.

The basic clock frequency for the multiplier circuit is

1 megahertz. Naturally, a faster clock is needed if bigger numbers are to be multiplied. The number of clock pulses required to multiply two n-bit numbers (where n includes the sign bit) is 2n(n–1). Additionally, larger numbers will mean more registers in the multiplier circuitry and more counters in the control-signal circuitry. (Some minor circuit changes must also be made.)

There is a useful rule of thumb to keep in mind to minimize modification when the multiplier is expanded. Choose the factor 2(n–1) to be the nearest larger integer power of 2 and then set the extra bits introduced in the multiplicand and the multiplier to zero. □

Regulating supply voltage all the way down to zero

by Brother Thomas McGahee
Don Bosco Technical School, Boston, Mass.

Precision monolithic voltage regulators make it fairly easy to design a high-performance power supply with a minimum of external components. These regulators have one general fault, however—they cannot regulate to any voltage lower than their reference, which is usually about 7 V. Sometimes, a voltage divider can be used to reduce the reference voltage, but if the reference voltage is reduced below approximately 2 V, good regulation can no longer be maintained.

The circuit shown in the figure, on the other hand, allows the reference voltage to be adjusted all the way down to the offset voltage of the regulator's internal op amp. REGULATOR$_1$ and its associated circuitry form a bias supply that provides a voltage of about –7 V for the V$^-$ terminal of the main regulator (REGULATOR$_2$). Since the noninverting input of this regulator is connected to the common ground of the circuit, its reference voltage appears to be +7 V with respect to this V$^-$terminal.

There will be a 7-V drop across resistors R_2 and R_3. When R_1 is set to its minimum value, the circuit's output voltage will be equal to the reference voltage. If the output is measured with respect to the V$^-$ terminal of REGULATOR$_2$, it will be 7 V. But if it is measured with respect to the common ground, it will be zero.

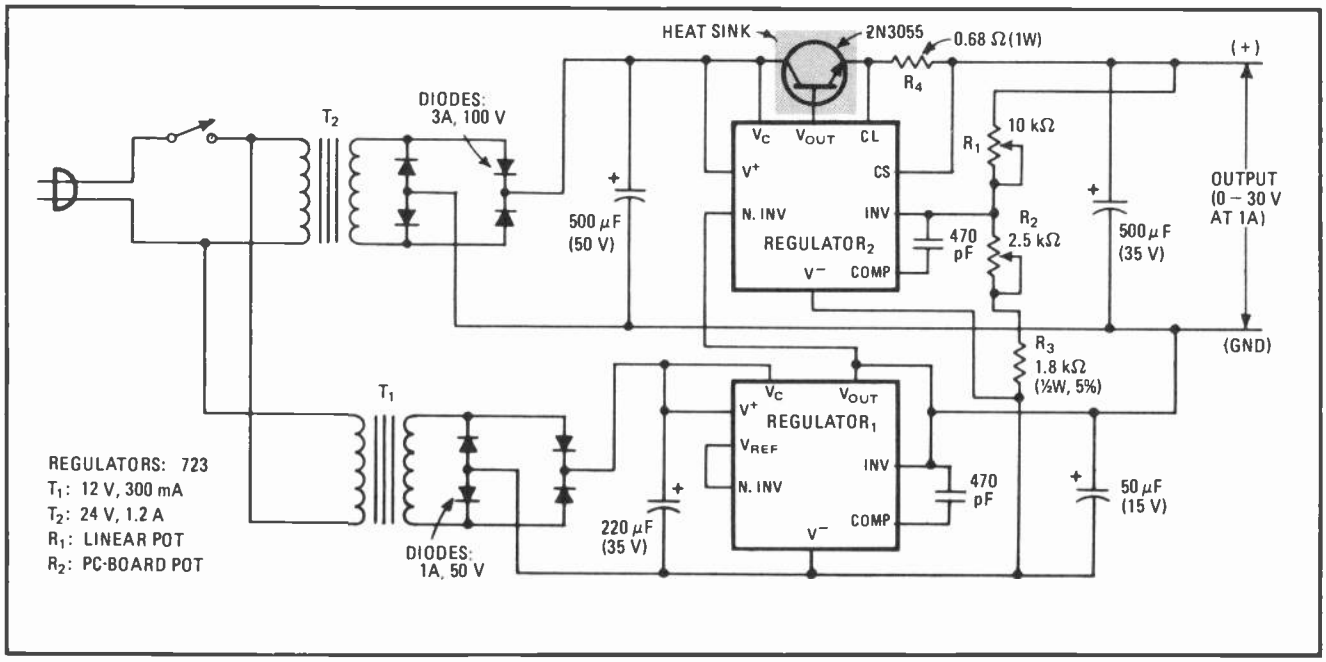
The maximum voltage available at the output is determined by the value of resistor R_2. For the component values shown here, the maximum voltage may be set anywhere from 16 to 39 V. But voltages above 30 V will not be regulated very well because the supply is using a 24-V transformer (T_2).

The equation for the output voltage is:

$$V_{OUT} = R_1 V_B/(R_2 + R_3)$$

where V_B is the absolute value of the bias voltage (7 V in this case). The bias supply normally will be producing about 12 milliamperes of current. Under worst-case conditions, however, it may be required to provide a maximum of 40 mA. Transformer T_1, therefore, should be a 12-V unit capable of supplying at least 50 mA (since REGULATOR$_1$ will require some current itself).

The transistor at the output of REGULATOR$_2$ boosts the circuit's output current. Resistor R_4 acts as the current-limiting resistor. □



Variable supply. This power supply, which employs two IC voltage regulators, produces a regulated output voltage of between 0 and 30 V. REGULATOR$_1$ provides the bias voltage for REGULATOR$_2$ so that the latter device can operate with respect to a common ground. The lowest regulated output voltage, then, is approximately zero, rather than the reference voltage of REGULATOR$_2$.

Capacitance-coupled logic fills unusual jobs

by Stephen R. Pareles
Cook College of Environmental Science, New Brunswick, N.J.

Capacitively coupling logic signals may prove to be a simple way to do several not-so-simple jobs. For instance, capacitive coupling can make short work of bidirectional pulse-edge detection, as well as comparison of an analog signal and a digital signal.

With the circuit of Fig. 1 and a single-trace oscilloscope, an analog signal and a digital signal can be displayed at the same time, allowing the two signals to be compared or synchronized. The circuit's output is the analog signal with superimposed digital cursors.

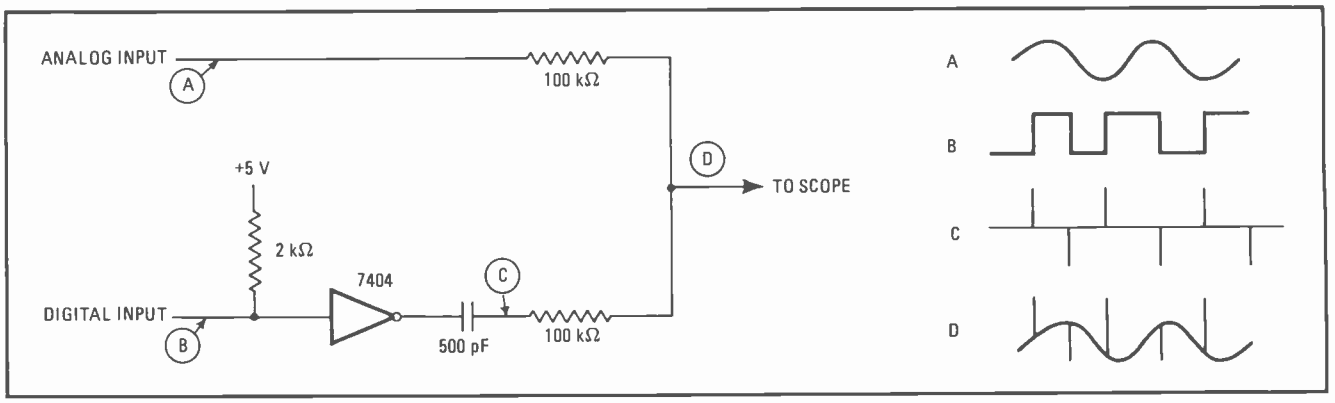
The capacitor serves as a bidirectional edge-detector for the buffered arbitrary logic train. Analog-level transients are produced by the capacitor from this input logic train. They are positive for leading pulse edges and negative for trailing pulse edges.

These transients are then cross-coupled with the analog signal through resistors that provide cross-current isolation (100-kilohm resistors are sufficient for most applications). A capacitance of 500 picofarads is ideal for slow horizontal sweep rates of up to about 100 hertz. Smaller capacitance values should be used for faster sweep rates to prevent the trailing edges of the transients from becoming observable.

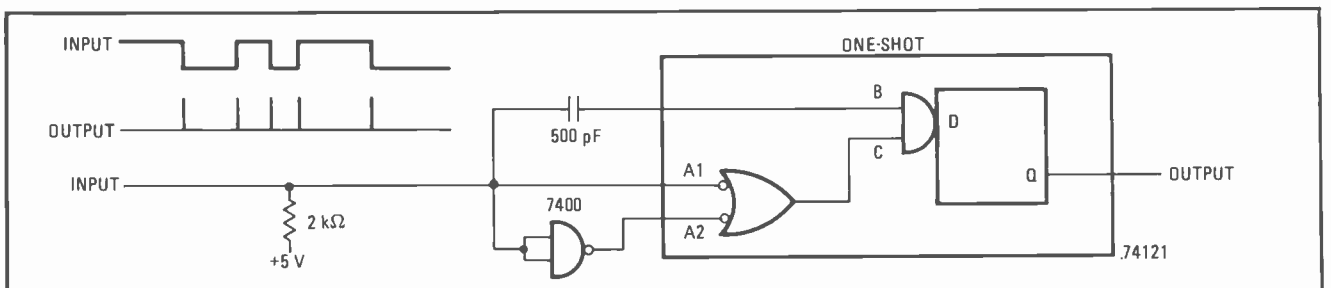
Capacitive coupling can also be used to perform bidirectional edge-detection when a logic-level output is desired. The detector circuit, which is drawn in Fig. 2, can even handle variable pulse widths.

Normally, a 74121-type one-shot is only triggered by a positive transition at point D, following a low condition at points D and Q. When the input first goes high, point A1 goes high. Since point A2 is still high, point C momentarily remains low. When A2 goes low and C high, the one-shot is triggered by the positive edge at D. Point B is kept high throughout.

When the input goes low, A1 goes low before A2 goes high, so that C remains high. Point B, however, is momentarily low. When B goes high again, the one-shot is triggered by the positive edge at C, as before. The tables in Fig. 2 detail the circuit's operation at key points. □



1. Two-signal display. A capacitor simplifies the task of observing two signals on a single-trace oscilloscope. The circuit's output becomes the analog input with superimposed digital timing cursors. The two 100-kilohm resistors provide the necessary cross-current isolation.



CIRCUIT OPERATION

TIME	POSITIVE INPUT TRANSITION							NEGATIVE INPUT TRANSITION						
	INPUT	A1	A2	C	B	D	Q	INPUT	A1	A2	C	B	D	Q
t_n	0	0	1	1	1	1	0	1	1	0	1	1	1	0
TRANSITION	1	1	1	0	1	0	0	0	0	0	1	0	0	0
t_{n+1}	1	1	0	1	1	1	ONE-SHOT	0	0	1	1	1	1	ONE-SHOT

2. Dual edge-detection. Both the leading and trailing edges of the input-pulse train are detected by this capacitively coupled circuit.

Continuing biasing improves clamping amplifier

by Jerry Graeme
Burr-Brown Research Corp Tucson Ariz

A clamping amplifier can be made faster and more accurate by biasing its zener clamping element so that it is always on. This biasing technique also results in reduced clamp capacitance, sharper turn-on, broader bandwidth, and lower thermal drift.

Clamping amplifiers or feedback limiters are frequently used to provide amplitude limiting for signal clipping, signal squaring, or overload protection. One of the simplest clamping elements for these applications is a zener diode.

A zener diode connected across the feedback resistor of an operational amplifier will conduct when the op-amp output level reaches the zener voltage. The zener overrides the feedback resistor and limits the op-amp output swing at the zener voltage. To obtain bipolar amplitude limiting, two zener diodes are generally connected, in series-opposing fashion, across the feedback resistor, as shown in (a).

Zener diodes used in this way, however, impose serious limitations on the clamp because of their large capacitance, insufficiently sharp turn-on characteristic, high leakage current, and undesirable thermal drift.

Zener parasitic capacitance, which is typically a comparatively high 700 picofarads, can result in a long turn-on time for the clamp, as well as restricted signal bandwidth. For the zener to turn on, its capacitance must be charged through resistor R_1, which is often a large value, to preserve the circuit's input resistance. Signal bandwidth is limited because resistor R_2 is capacitively shunted by the zener.

When the zener conducts, it goes from a high-resistance state to a low one. But since this transition is not abrupt, sharp limiting cannot be achieved, and the clamping is rounded. Even in its high-resistance state, the zener, through its leakage current, introduces error into the amplifier's summing junction. Furthermore, when the zener is on, the clamp level it sets is subject to thermal drift since the zener will probably not be held at its zero-temperature-coefficient current.

All of these limitations can be overcome to a significant extent with the biased zener clamp of (b). Here, the zener is continuously biased on so that it does not limit the op-amp output swing until the diode bridge places the zener in the feedback path.

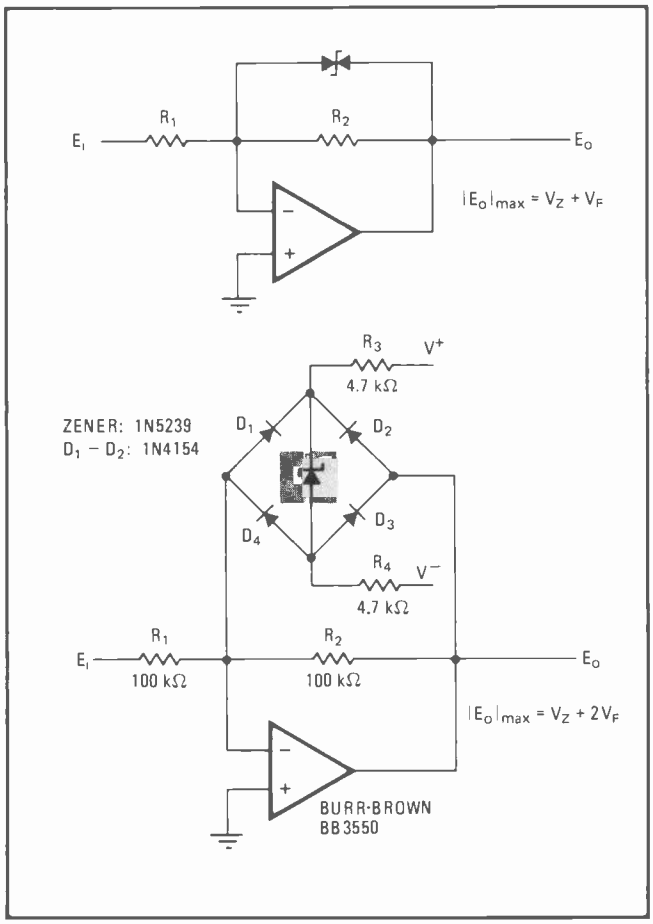
Clamping occurs when the voltage across resistor R_2 can support the zener voltage as well as forward-bias two of the bridge diodes. Positive-polarity signals are clamped when diodes D_1 and D_3 conduct, connecting the zener across the feedback path. When diodes D_2 and D_4 conduct, the zener limits signals of the opposite polarity. Since the same zener is used for both signal polarities, the output clamping will be symmetrical.

The continuous zener bias dramatically reduces the clamp's shunt capacitance, sharpens the clamping response, and often means lower thermal drift. To reduce thermal drift, resistor R_3 is chosen to produce a zener thermal variation that is canceled by that of two bridge diodes. When the clamp is on, the zener current is approximately:

$$I_Z = (V^+ + V_F)/R_3 \text{ or } (-V^- + V_F)/R_3$$

where V_F is the forward voltage of a junction diode, and V^+ and V^- are the supply voltages. (This equation neglects the signal current from resistor R_1, which is generally small compared to the zener current.)

Sharper clamping is achieved by avoiding the zener turn-on characteristic and leakage current. The clamping circuit is now turned on by the bridge diodes, and the sharper turn-on of these junction diodes improves



Whetting sharpness of zener clamp. Standard zener-type clamping amplifier (a) can be slow and sloppy because of large zener capacitance and zener leakage. But a dramatically faster and crisper response can be obtained by adding a bridge of junction diodes to keep the zener always biased on, no matter the input signal polarity The improved clamp (b) also provides more bandwidth and less drift

clamping sharpness by around 8:1. Zener leakage current no longer reduces signal current as the clamping level is approached. Leakage to the amplifier summing junction is now the much smaller leakage of junction diodes D_1 and D_4.

Additionally, the capacitance of the clamping circuit is reduced by avoiding the charging and discharging of the zener capacitance. Only small voltage changes, the ones produced by signal current flow in the continuously biased zener, occur across the zener capacitance. Large voltage changes are restricted to the junction diodes, which have a far lower capacitance than the zener. The equivalent clamp capacitance that must now be charged through resistor R_1 is merely the combined capacitances of diodes D_1 and D_4. Typically, this represents a 100:1 reduction from the basic zener clamp capacitance so that turn-on time is faster.

And lastly, the bandwidth-limiting capacitive shunt on resistor R_2 is reduced by more than 100:1. Amplifier signals that do not turn the clamp on are not even affected by the small bridge-diode capacitance. When the bridge diodes are off, fixed voltages are established at one end of diodes D_1 and D_4 by the zener and its bias resistors. The only signal swing on these two input shunting diodes, then, is the very small summing junction signal. The equivalent capacitive shunt of resistor R_2 is reduced to $2C_F/A$, where C_F is the forward capacitance of a junction diode, and A is the open-loop gain of the op amp. (This capacitance is negligible compared to other parasitic capacitances.)

For the components shown in the figure, large- and small-signal bandwidths are boosted from 3 kilohertz to 400 kHz; clamping sharpness error is reduced from 0.8 volt to 0.1 V; clamp leakage current is decreased from 400 nanoamperes to 7 nA; and clamp-level thermal drift is brought down from 7 mV/°C to 0.6 mV/°C. □

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G. Tobey, J. Graeme, and L. Huelsman, "Operational Amplifiers—Design and Applications," McGraw-Hill, 1971.

LED display shows beat frequency

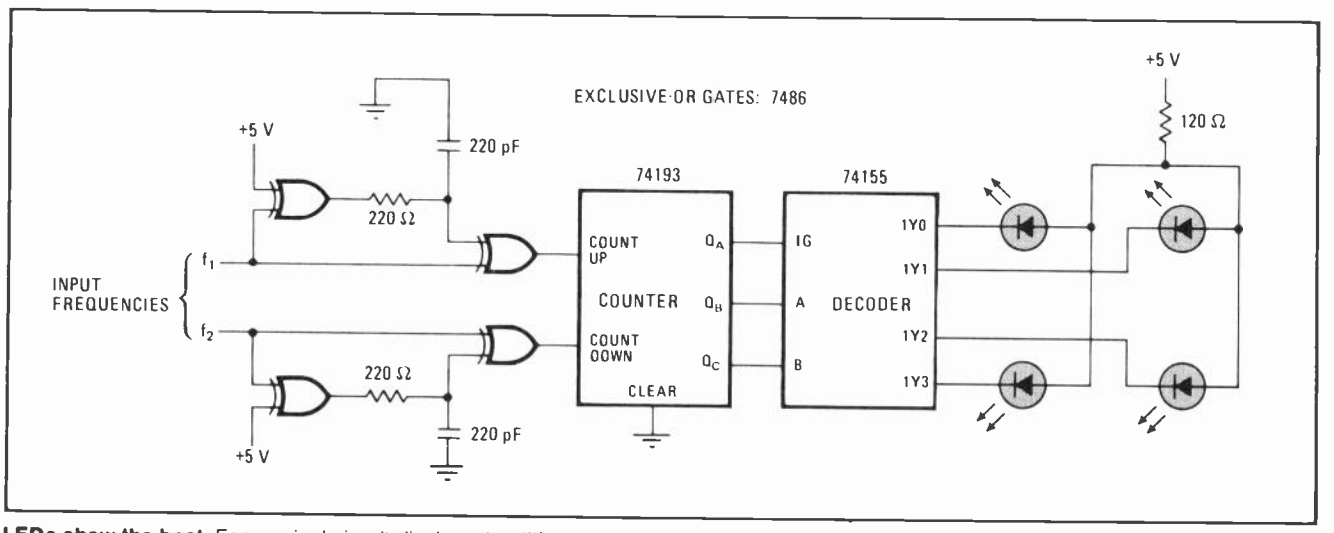
by Sergio Franco
Oberlin College, Oberlin, Ohio

A simple, easy-to-use beat-frequency indicator can be built at a cost of only about $5. The circuit, which employs four light-emitting diodes as its display, can be used in a variety of applications, but is particularly suited to the tuning of musical instruments.

The heart of the circuit is a 4-bit synchronous up/down binary counter. After undergoing proper shaping by exclusive-OR gates, input frequencies f_1 and f_2 are applied, respectively, to the count-up and count-down terminals of the counter. The net count, therefore, will be in either the up or the down direction, depending on whether f_1 is greater than or less than f_2. When f_1 equals f_2, the counter alternates between two consecutive states, producing a net count of zero.

These three input conditions can be easily displayed by means of four LEDs arranged in a circle. (A decoder is used to drive the LEDs from the counter output lines.) Only one LED is on at a time. Therefore, when f_1 is greater than f_2, a dot of light is produced that rotates clockwise; when f_1 is less than f_2, the dot rotates counterclockwise; and when f_1 equals f_2, there is no rotation.

Furthermore, since the exclusive-OR shaping network produces a sharp negative pulse for each transition of the two inputs, the dot of light moves one step for every beat. The rate of apparent rotation of the dot, then, is an exact indication of the beat frequency. □



LEDs show the beat. Economical circuit displays the difference frequency between its two inputs, as well as indicating their relative magnitude. Since only one LED conducts at a time, what is displayed is a dot of light. The dot rotates clockwise when f_1 is greater than f_2 and counterclockwise when f_1 is smaller. The rate of rotation is the beat frequency. When f_1 equals f_2, the dot remains stationary.

Interfacing a teletypewriter with an IC microprocessor

by Steven K. Roberts
Cybertronic Systems, Louisville, Ky.

The lengthy software service routine generally required to interface a teletypewriter and an IC microprocessor, such as the Intel 8008, can be eliminated by the circuit shown here. A shift register and some control logic are all that it takes, bringing total component cost to only about $6.50.

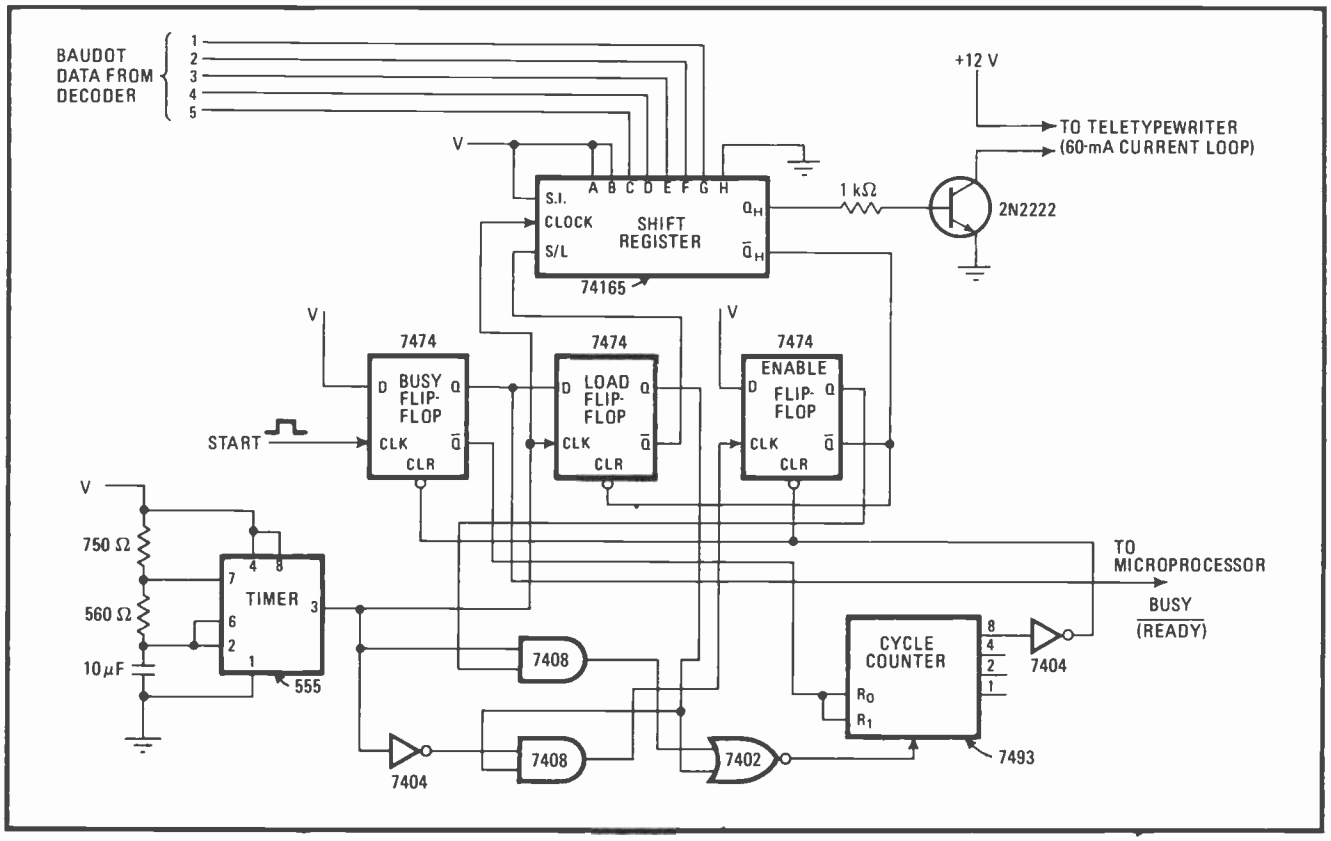
In the 8008 system, synchronization with the central-processing unit is accomplished through this microprocessor's READY line, making modification of the teletypewriter itself unnecessary. The hardware configuration given in the figure is designed for a 10-character-per-second Model 28 Teletype, which uses the five-level Baudot code. If the intended application will not easily accommodate data storage in the Baudot code, conversion may be accomplished with a read-only memory, such as National's MM5221TM. (A Model 33 Teletype presents no decoding problem.)

During the time that the input parallel data is valid, the circuit receives the START pulse, which sets the BUSY flip-flop and takes the READY line low. The BUSY flip-flop also removes the reset from the cycle counter and enables the LOAD flip-flop, which is set on the next clock pulse. This action loads the data at the input to the shift register and increments the cycle counter once.

On the succeeding clock pulse, the ENABLE flip-flop is set, and the data in the register begins to shift to the right. For each shift pulse, the cycle counter is incremented by one until it reaches a binary count of 8. Then, the BUSY and ENABLE flip-flops are both reset, and the READY signal is restored to the microprocessor so that the central-processing unit can resume operation.

In the data character presented to the shift register, bit H, which is constantly held low, corresponds to the teletypewriter START pulse. Similarly, the register's A and B bits are tied high, corresponding to the teletypewriter STOP pulse. Since the STOP signal must be applied to the teletypewriter for approximately 1.5 times longer than the other pulses, the BUSY flip-flop is reset on the falling edge of the clock, during the time that bit A is present at the register's Q_H output. The serial output of the register switches the 60-milliampere teletypewriter current loop through the transistor.

The clock signal for the circuit is derived from the IC timer that is free-running at approximately 75 hertz. For teletypewriters that operate at 6 characters per second, the clock frequency should be about 45.5 Hz. □



Software bypass. Digital interface circuit provides synchronization between a teletypewriter and a microprocessor chip through the latter device's READY line. Normally, a long software routine is needed to make the interface. The input data is in the parallel Baudot code, and the output is for a 10-character-per-second teletypewriter. A free-running IC timer is used to produce the clock signal.

Diode pair senses differential temperature

by Don DeKold
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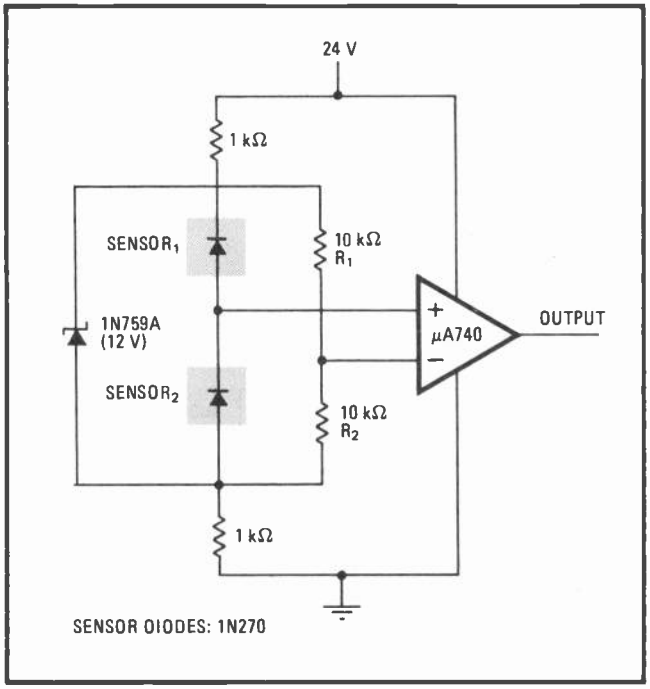
Normally, a germanium diode functioning as a temperature sensor relies on the linear variation of its forward voltage with temperature. But a pair of germanium diodes can be made to serve as a differential-temperature comparator if the circuit exploits a much less used temperature-dependent diode property—the logarithmic variation with temperature of the reverse saturation current. The resulting circuit is useful for industrial-control applications.

When one diode ($SENSOR_1$) is at temperature T_1 and the other diode ($SENSOR_2$) is at temperature T_2, the circuit output will change state as the temperature differential (T_1–T_2) approaches and crosses a differential threshold, $\Delta T_{1,2}$. For the circuit shown here, $\Delta T_{1,2}$ is 13°C—when (T_1–T_2) is less than 13°C, the circuit's output is low; and when (T_1–T_2) is greater than 13°C, the output goes high. The circuit has a fairly wide and useful temperature range of 20°C to 120°C.

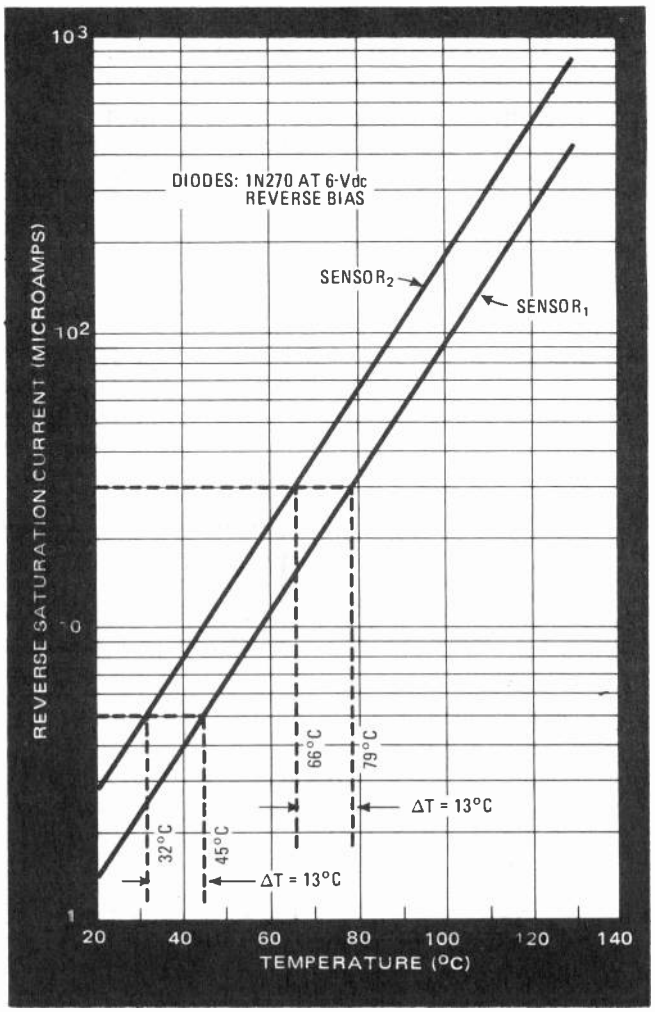
The two diodes, along with resistors R_1 and R_2, form a resistance bridge. The right-hand side of the bridge consists of equal resistances that divide the bridge voltage in half, establishing a reference voltage at the inverting terminal of the FET-input operational amplifier. The noninverting op-amp terminal receives the temperature-dependent voltage, which is derived from the division of the bridge voltage across the diode temperature sensors.



In general, the reverse saturation currents of two unmatched diodes are different at a single temperature. However, when plotted as a function of temperature on semilog paper, the two reverse-current characteristics will be parallel to each other. That is, a diode's reverse current may vary from one unit to the next at a single temperature, but it will increase in an identically proportional manner from one unit to the next as a function of temperature.

For instance, for the type 1N270 germanium diodes used here, the current doubles every 13°C. The doubling is highly regular, producing a nearly linear semilog plot over a fairly wide temperature range, as shown by the graph of reverse saturation current versus temperature for two type IN270 diodes.

Now, when a diode is reverse-biased, it in effect becomes a temperature-dependent current source with a reverse saturation current that is only negligibly influenced by the actual magnitude of the reverse voltage. But as the reverse voltage approaches zero, the reverse current decreases. When two diodes are connected in series, therefore, the voltage across them will divide equally only when their currents are the same, a condition that occurs at a fixed temperature difference between the two. This equal-current temperature differ-



Temperature comparator. Unmatched germanium diodes have different reverse saturation currents at the same temperature. But this difference remains proportionate with changing temperature so that the temperature differential between the two currents stays the same, as shown by the graph. A differential-temperature comparator can be built by connecting two unmatched diodes in a bridge configuration.

ential is the $\Delta T_{1,2}$ threshold for the circuit.

The diode having the lower reverse saturation current acts here as $SENSOR_1$, so that practically all of the bridge voltage will be dropped across it. This keeps the voltage at the noninverting op-amp input below that of the inverting op-amp input, and the circuit's output is low. As the temperature of $SENSOR_1$ increases, its reverse leakage current will also rise.

When $SENSOR_1$ is $\Delta T_{1,2}$ degrees celsius above $SENSOR_2$, the voltages at the op-amp inputs will be equal. With an additional temperature increase of $SENSOR_1$, most of the bridge voltage will then be dropped across $SENSOR_2$. This raises the voltage of the noninverting op-amp input above that of the inverting op-amp input, causing the circuit's output to go high.

Various operating conditions can be set up for the differential-temperature comparator by interchanging the locations of the low-current and high-current diodes or by switching the input connections to the op amp. Different diode pairs will provide different values of threshold temperature. Basically, $\Delta T_{1,2}$ is determined by the ratio of diode leakage currents at a fixed temperature, and this current ratio increases as the comparator differential increases. Diodes with identical reverse currents at the same temperature produce a $\Delta T_{1,2}$ of 0°C.

A FET-input op amp must be used here to assure that there is practically no loading of the bridge diode divider. Minimal loading is particularly important if the absolute temperatures to be compared differentially are low. □

Generating nanosecond pulses with TTL monostables

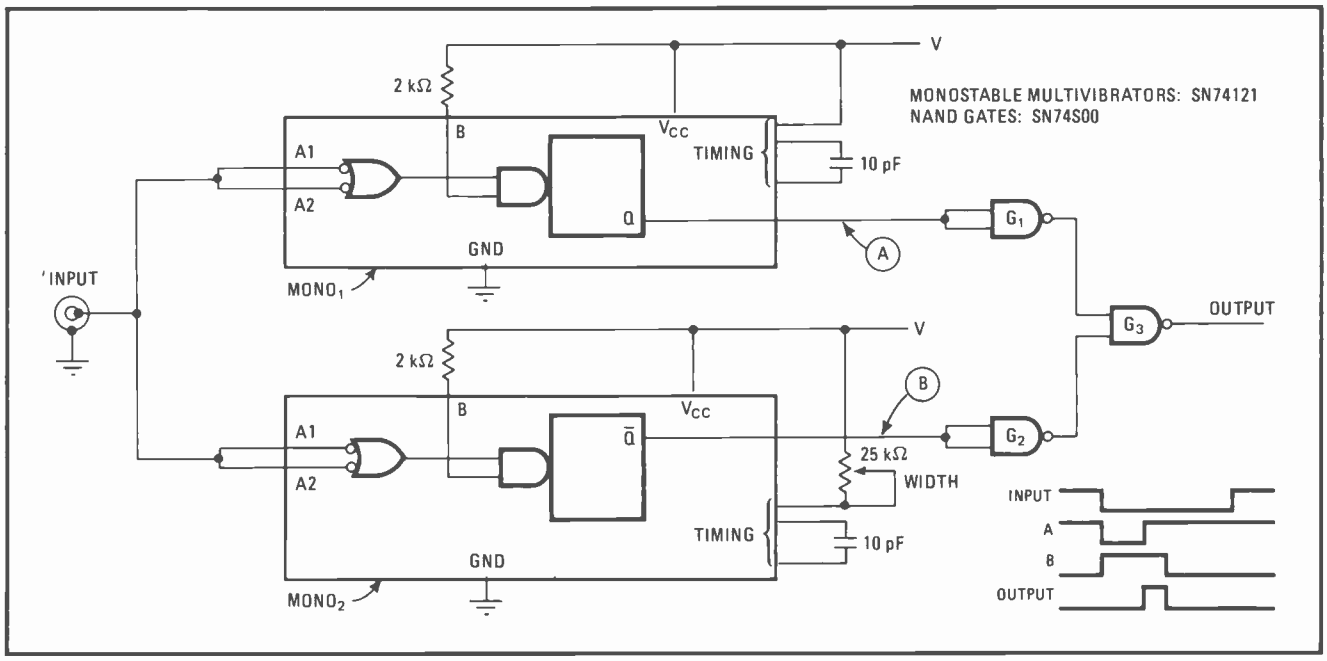
by Robert J. Broughton
Yale University, New Haven, Conn.

Narrow fast pulses—with widths down to a few nanoseconds and rise and fall times of 2 ns—can be produced by a circuit based on transistor-transistor logic. The circuit's output pulse width is variable, and pulses as wide as 220 ns can be obtained.

The trick is to take the difference between two pulses generated by a pair of standard TTL monostable multivibrators. The input signal is applied to the edge-triggered inputs of $MONO_1$ and $MONO_2$. Those two monostable inputs are wired in parallel, while the Schmitt-trigger monostable inputs are kept high by the 2-kilohm resistors tied to the supply voltage.

$MONO_1$ is wired to produce a 30-ns pulse, which is conditioned by a Schottky-TTL NAND gate, G_1, to speed up its rise and fall times. Similarly, $MONO_2$ generates an output pulse that is complementary to the one generated by $MONO_1$ and that is conditioned by a second Schottky-TTL NAND gate, G_2. The width of this pulse is adjustable from 30 ns to more than 250 ns.

The third and last Schottky-TTL NAND gate, G_3, accepts the conditioned pulses from gates G_1 and G_2. The output of this gate is a fast narrow pulse whose width is the difference between the pulses produced by $MONO_1$ and $MONO_2$. An output pulse having a width of 8 ns and rise and fall times of 2ns can be easily obtained with the generator circuit. □



Pulse generator. A pair of standard TTL monostables can be made to produce sharp nanosecond pulses by using a Schottky-TTL NAND gate to accept their complementary outputs. The pulse width of $MONO_1$ is fixed at 30 ns, while the pulse width of $MONO_2$ is variable from around 30 ns to better than 250 ns. Gate G_3 takes the difference between these two pulse widths. Output rise and fall times are 2 ns.

Full-wave rectifier needs only three matched resistors

by Jerald Graeme
Burr-Brown Research Corp., Tucson, Ariz.

Precision rectifiers or absolute-value circuits will accurately rectify even a millivolt-level signal for applications requiring precise magnitude detection. But because of their low input resistance, most of these circuits require many resistors to be matched. With the precision rectifier drawn in the figure, however, a high input impedance can be achieved without the addition of a buffer amplifier—and only three resistors have to be matched.

In an absolute-value conversion, the input signal is converted from a bipolar form to a unipolar form, a standard requirement for magnitude detection in many average-reading measuring instruments. There are several absolute-value circuits that can be built with an operational amplifier to obtain the desired high accuracy for full-wave rectification.

In these circuits, rectification is carried out without sacrificing a significant portion of the input signal to forward-bias the rectifying diodes. These diodes are placed in the op-amp's feedback loop so that the high gain of the op amp reduces signal loss. This means that only very small signal changes are needed to drive the diodes into and out of conduction, and millivolt-level signals can be rectified.

Most precision rectifier circuits have a low input impedance, which is set by input summing resistors, so that a buffer amplifier must often be added. However, the need for an additional op amp is avoided by the circuit shown because its input impedance is the common-mode input impedance of an op amp, and the usual input summing resistors are eliminated. This results in a typical input resistance either of 25 megohms for an op amp having a bipolar-transistor input or of 10^{12} ohms for an op amp having a FET input.

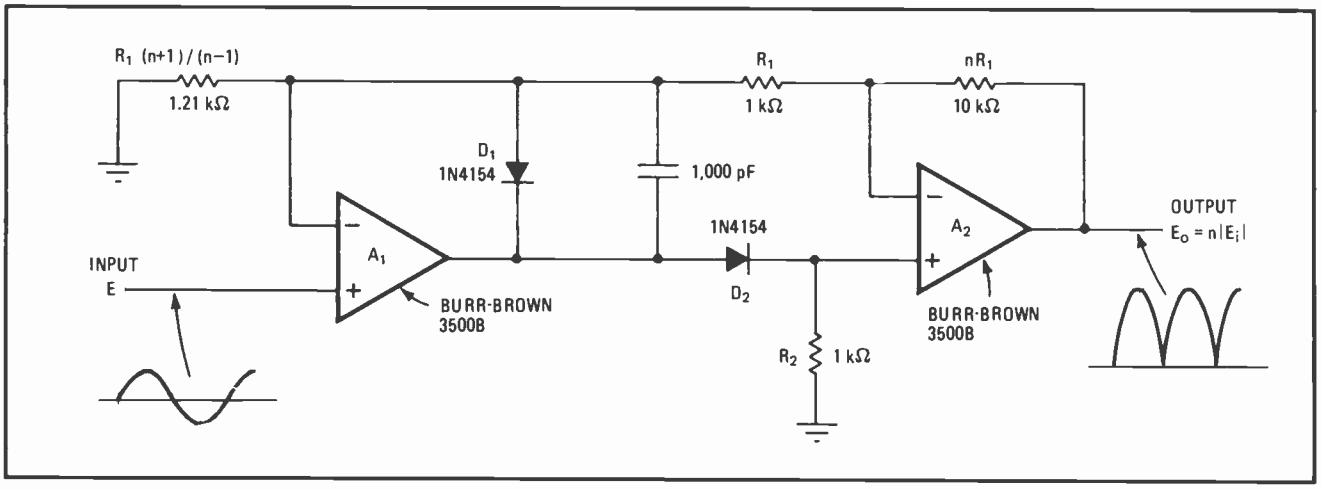
Full-wave rectification is produced by diode switching that reverses the polarity of the net circuit gain when the polarity of the input signal reverses. The polarity of the output signal is therefore prevented from changing. This feature, coupled with the circuit's equal-gain magnitude for input signals of either polarity, results in an absolute-value conversion.

Gain polarity is switched by the diodes as they alternate the connection of the output of amplifier A_1 between the two inputs of amplifier A_2. Positive input signals cause the output of A_1 to become positive, reverse-biasing diode D_1 and forward-biasing diode D_2. Since the output of A_1 is now connected to the noninverting input of A_2, amplifier A_2 provides a gain having a positive polarity.

Gain magnitude is controlled by three feedback resistors that are designated as multiples of R_1 in the diagram. Feedback forces the output of amplifier A_2 to the level that develops a voltage equal to E_i across the $R_1(n+1)/(n-1)$ resistor. For the positive-signal case, the associated gain (E_o/E_i) is n. Since both amplifiers are connected in a common feedback loop for the positive-signal mode, additional phase compensation may be required with the capacitor shown.

Negative input signals are amplified by a gain of opposite polarity. They cause the output of amplifier A_1 to swing negative, forward-biasing diode D_1 and reverse-biasing diode D_2. Now amplifier A_1 drives the inverting, rather than the noninverting, input of amplifier A_2. Because the noninverting input of A_2 is connected to ground through resistor R_2, A_2 acts as an inverting amplifier, providing a negative gain for the signal supplied by A_1.

With its feedback shorted by diode D_1, amplifier A_1 performs as a voltage-follower, supplying inverting am-



Improved rectifier circuit. High-accuracy full-wave rectifier requires matching only three resistors. The circuit has a high input impedance, without an extra buffer amplifier, because the common-mode input impedance of amplifier A_1 faces the circuit's input. For positive signals, amplifier A_2 is noninverting so that circuit gain is + n. For negative signals, A_2 becomes inverting, and circuit gain is −n.

plifier A_2 with a signal that equals input voltage E_i. The over-all circuit gain is now -n. Circuit gain, therefore, is switched from +n for positive signals to -n for negative signals.

The performance of the circuit is limited by a number of factors, including resistor matching, as well as the amplifiers' input offset voltages, input bias currents, fastest slewing rates, and maximum gains.

The input offset voltages and input bias currents introduce a deadband around zero, in addition to an output offset. These two errors are removed by first nulling the offset voltage of amplifier A_1 to eliminate the deadband, and then nulling the offset voltage of amplifier A_2 to get rid of the output offset. Because of the interaction of these two nulls, this procedure must generally be repeated. The slewing rate and gain of amplifier A_1 and the diode capacitances also create a deadband around zero that limits the upper rectification frequency.

Any deviation from the resistor-matching ratios indicated here will produce a gain error that, in some cases, will make the gain magnitudes different for the two input signal polarities. This gain error can be removed by first adjusting the circuit's gain for negative signals through trimming resistor R_1 or resistor nR_1. Circuit gain for positive signals can then be matched to the negative-signal gain by adjusting resistor $R_1(n+1)/(n-1)$. Prior to these gain trims, it may be necessary to null out any existing deadband error since this error can also produce unequal outputs for equal positive and negative input signals.

With the component values shown, the circuit can accept a maximum input voltage of 2 V peak-to-peak and produce a maximum output voltage of 10 V. Circuit gain is 10. □

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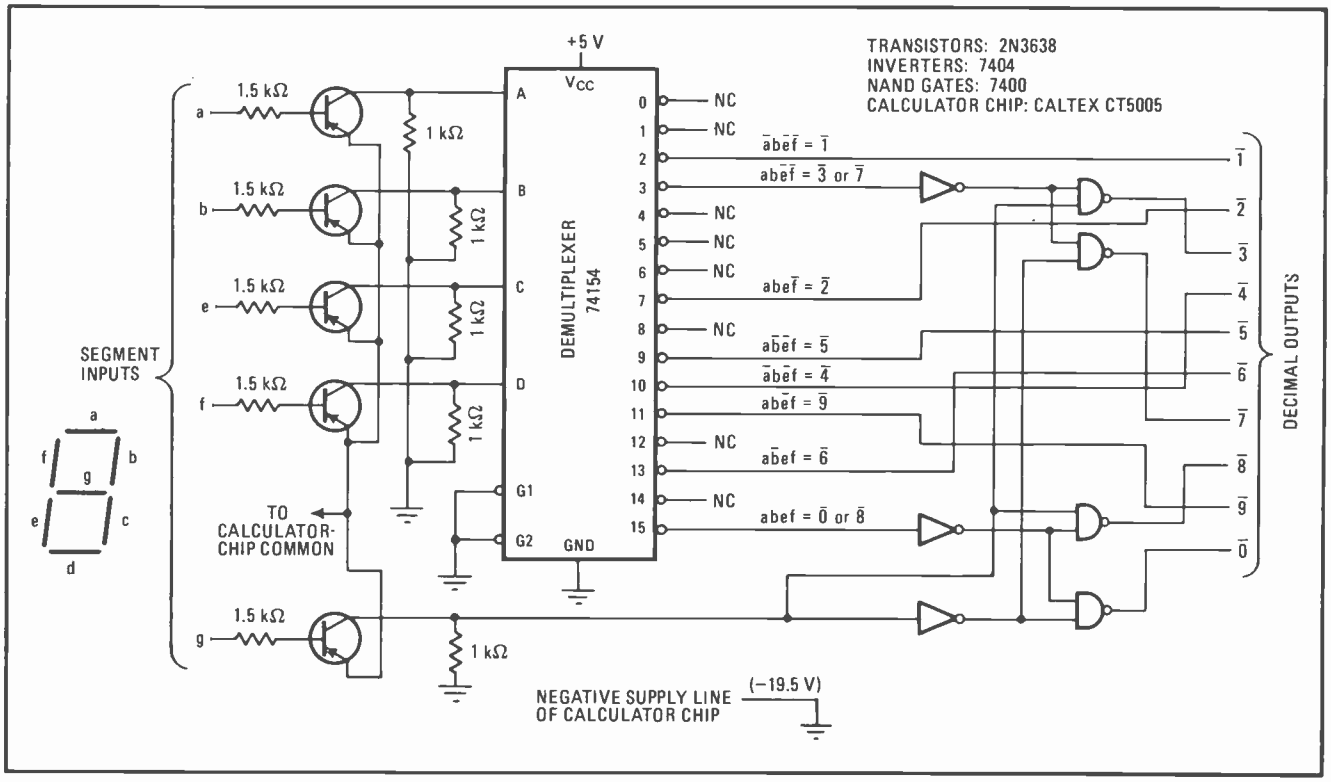
Providing a decimal output for a calculator chip

by Jack Lambert

Lambert Associates, Lexington, Mass.

Calculator chips, which are becoming readily available, can be used to advantage in applications other than pocket calculators. However, these chips usually have an output that drives a multiplexed seven-segment display. This is not really convenient for performing subsequent operations or even for interfacing with Nixie-type readouts.

With the circuit shown here, the output of a calculator chip can be converted to the more convenient decimal form. If desired, this decimal output can also be converted, for example, to a binary-coded-decimal form. A calculator chip having a decimal output can be used as an input to another calculator, to operate a



More applications. Decoder circuit converts the seven-segment-display outputs of a calculator chip to decimal form, greatly increasing the application versatility of the chip. All 10 of the decimal outputs can be derived from only five of the segment inputs. The same power supply is used for both the chip and the decoder's TTL circuitry. The chip's negative supply line acts as ground for the TTL supply.

large dot-matrix display, to feed a printer, or to drive a digital controller or computer.

Although the conversion circuit is not necessarily the simplest logic scheme, it is easy to set up and to wire. Only three TTL IC packages are required—they are a four-line-to-16-line demultiplexer, a hex inverter, and a quad two-input NAND gate.

The lower-case letters in the diagram correspond to the display segments used to set up the logic for the conversion circuit. Only five of the seven possible segment inputs are needed to develop all of the decimal outputs; the other two segments are redundant. The seven-segment logic inputs are high, while the decimal outputs are low. The gate inputs (G1 and G2) to the demultiplexer may be used if desired, otherwise they should be tied low, as shown.

This particular conversion circuit is intended for the Caltex type CT5005 calculator chip. A separate 5-volt supply is used for the TTL ICs, but the negative line (−19.5 V) of the chip supply is made the ground line of the TTL supply. This allows a single supply, one having the proper dropping resistors and regulation, to be used for both the chip and the conversion circuit.

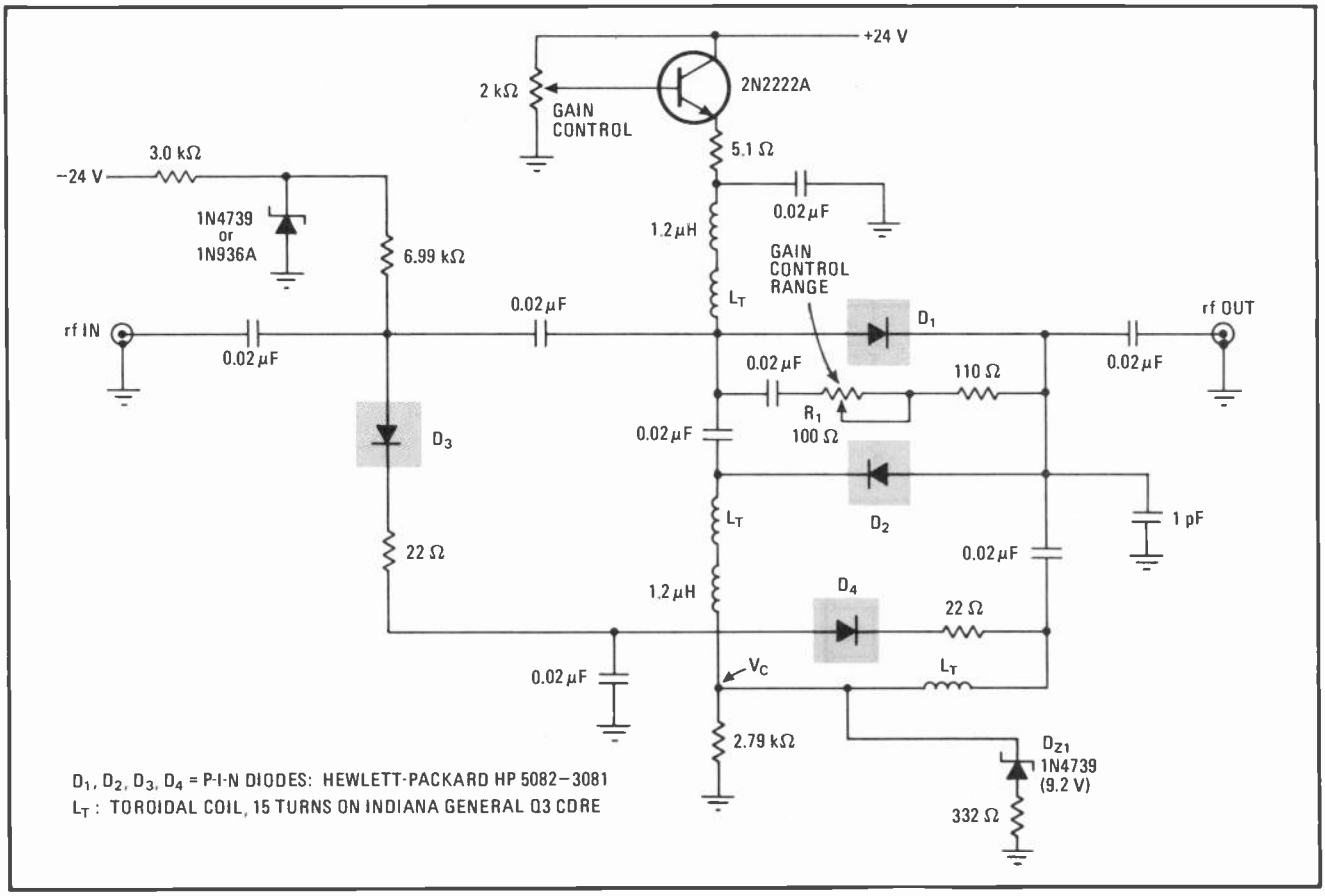
The discrete transistors serve as a simple interface between the chip and TTL devices. This means that the display outputs of the chip can directly drive the conversion circuit. Of course, a chip other than the type CT5005 device may require other interfacing.

The use of the type 74154 demultiplexer results in a certain amount of redundancy in the circuit's decoding process. However, the demultiplexer does keep the wiring simple, and it also conserves board space without increasing parts cost significantly. The entire circuit costs about $3.50 to build. □

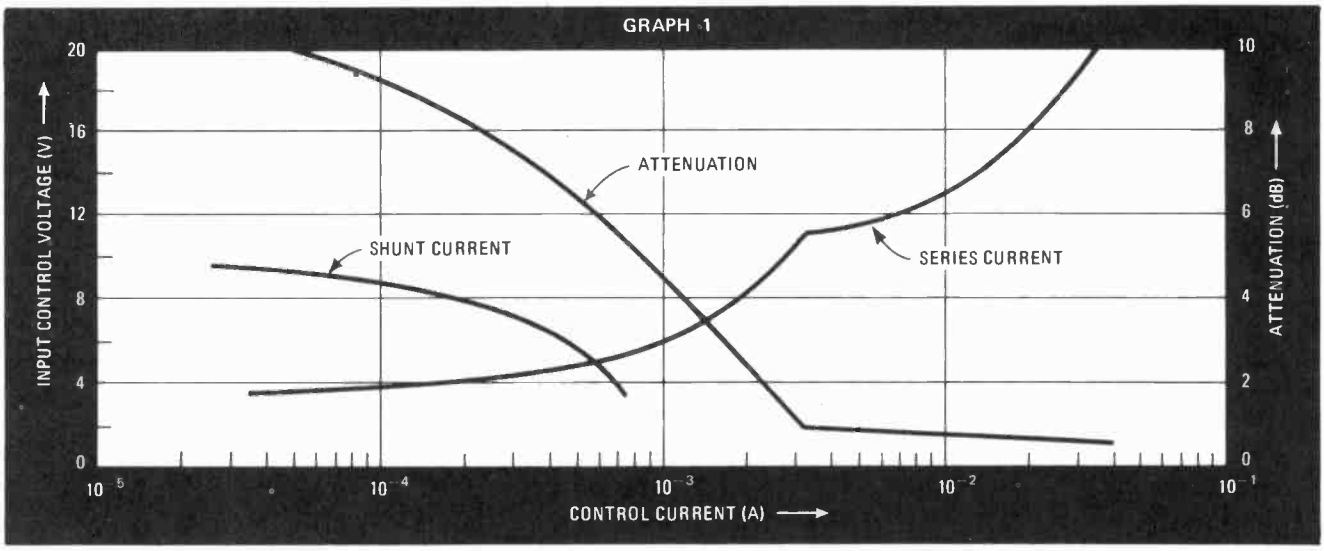
Broadband p-i-n attenuator has wide input dynamic range

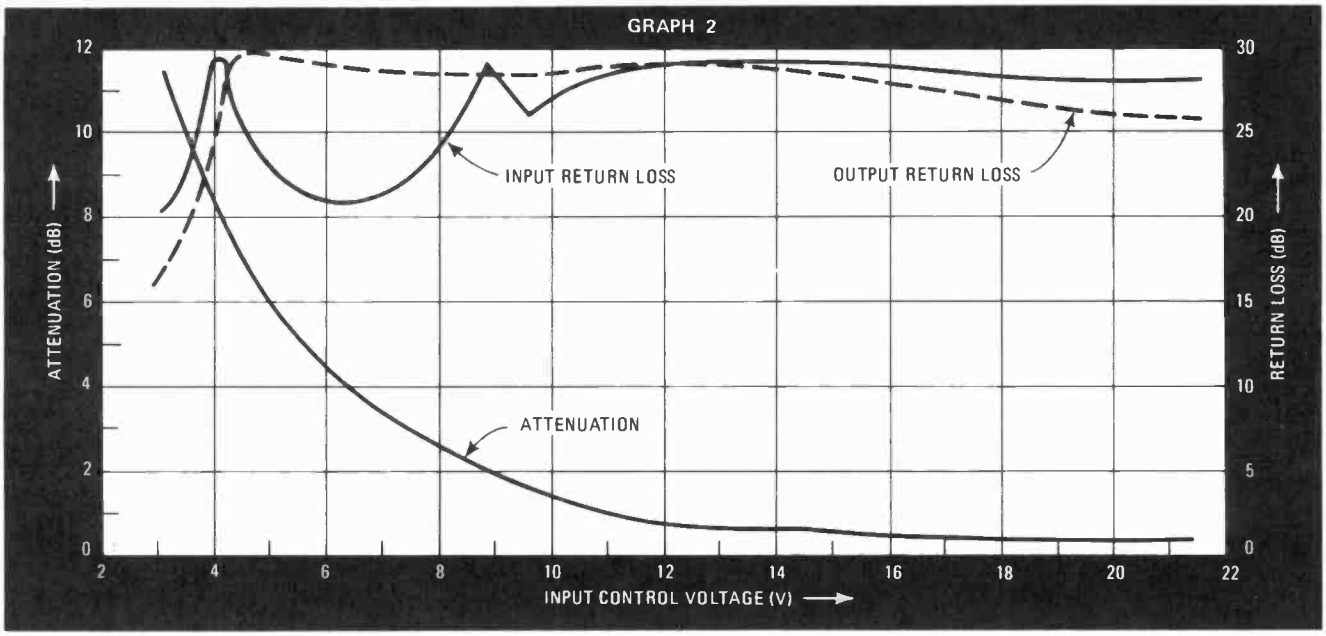
by Roland J. Turner
American Electronic Labs, Colmar, Pa.

A low-loss broadband attenuator that is built with p-i-n diodes offers an exceptionally flat response over a wide input dynamic range. The circuit, which employs the p-i-n diodes in a π configuration, is useful for automatic-gain-control applications over the frequency range of 50 to 300 megahertz. Its response remains flat to within ±0.10 decibel over the full 11-dB input control range. Insertion loss is less than 0.50 dB, and the input/output return loss exceeds 20 dB over the entire op-



High performer. This rf attenuator provides exceptional response flatness over a wide input dynamic range from 50 to 300 megahertz. High-quality p-i-n diodes connected in a π configuration minimize the circuit's intermodulation distortion. Diodes D_1 and D_2 form the series arm of the π network, while diodes D_3 and D_4 form the shunt arm. Graphs 1 and 2 show the attenuator's primary characteristics.





erating frequency range and gain-control range.

A π configuration, as opposed to a bridged-T network, is used here because of its superior performance. The π attenuator requires less current-drive shaping, and it reduces the effect of parasitic inductances on input/output return losses, since stabilizing resistors can be used in its shunt arm. The bridged-T attenuator, on the other hand, requires low resistance values in its shunt arm so that stabilizing resistors cannot be used. Therefore, the input return loss and response flatness of the bridged-T attenuator are seriously affected by reactive current at high attenuation levels.

The high-performance π attenuator shown in the figure uses p-i-n diodes that exhibit very low intermodulation distortion across the circuit's full operating band. P-i-n diodes D_1 and D_2 form the series arm of the π-configuration attenuator—they are connected in parallel for signal transfer and in series for the control bias.

When low attenuator loss is desired (for control voltages of more than 10 V), zener diode D_{Z1} conducts and forces the series control bias current to exceed 35 milliamperes. For an attenuation level of greater than 1.5 dB, D_{Z1} is nonconducting, and the series control current in diodes D_1 and D_2 is less than 5 mA. Series resistor R_1 is used to set the gain control range between 8 and 13 dB.

The attenuator's control circuit is quite simple. The control bias voltage, V_C, which governs the turn-on of shunt diodes D_3 and D_4, is determined by the amount of series control current that flows. Consequently, when the series control current decreases, the shunt control current automatically increases.

Graph 1 shows the series and shunt control currents, as well as the attenuation level, produced at various input control voltages. The gain-control characteristic and the input/output return loss generated by this current profile are plotted in Graph 2.

The operating frequency range of the attenuator is limited by the p-i-n diodes used. With the ones called for here, the attenuator should provide similar performance characteristics down to 5 MHz. □

IC timer and voltage doubler form a dc-dc converter

by Todd Gartner
Motorola Inc., Automotive Research & Development, Franklin Park, Ill.

A dc-dc converter in which an IC timer serves as a free-running relaxation oscillator is ideal for powering op amps in battery-operated equipment or whenever a single positive supply is all that's available. Furthermore, the converter develops an output voltage of −15 V that is regulated to within ±1% for load currents of up to 30 milliamperes. The circuit's no-load current is 11 mA.

The free-running frequency of the timer is determined by resistors R_A and R_B and capacitor C_T. The output from the timer is used to drive the voltage-doubler network consisting of diodes D_1 through D_4 and capacitors C_1 through C_4.

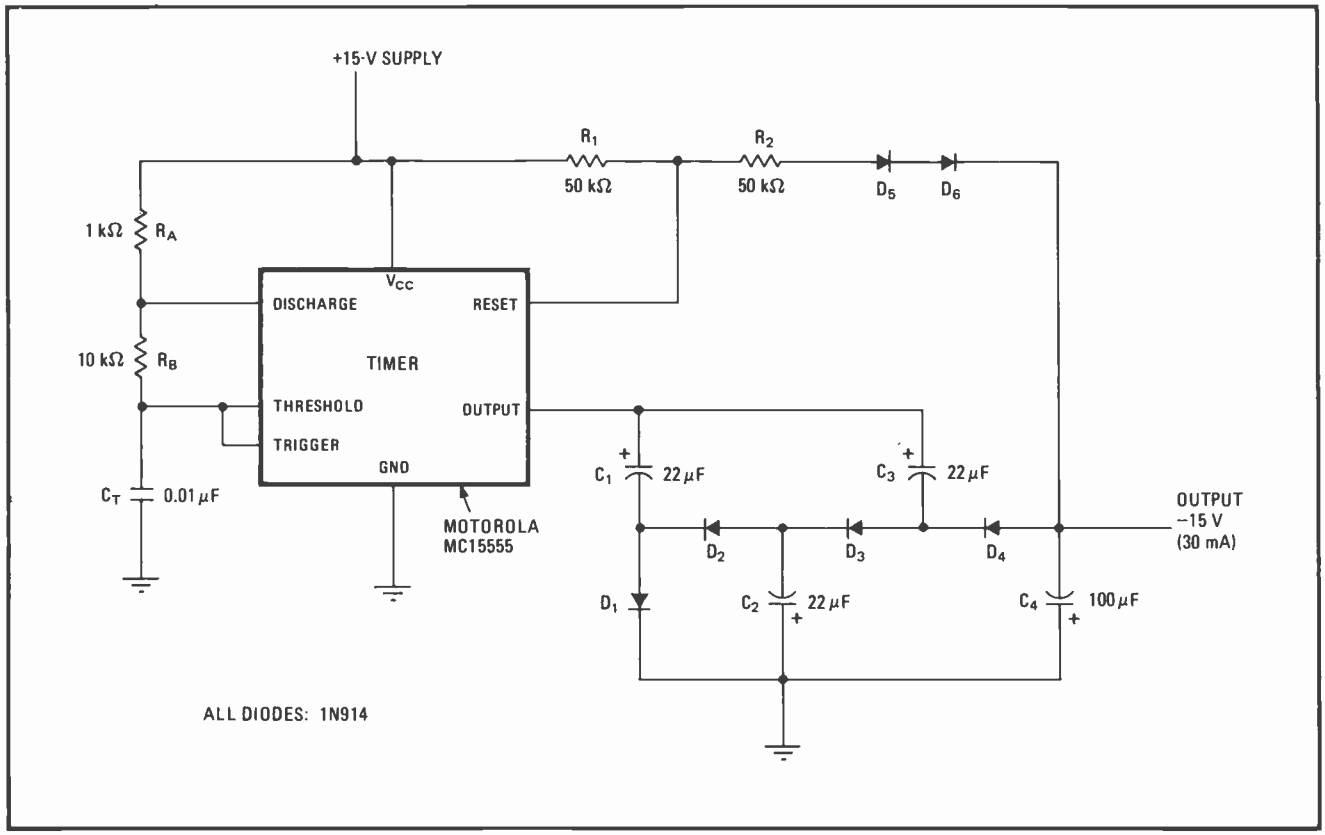
Without the feedback connection between the output of the voltage doubler and the reset input of the timer, the circuit's output under a no-load condition will float to about 30 V minus four diode voltage drops. With the feedback connection, the voltage divider formed by diodes D_5 and D_6 and resistors R_1 and R_2 places a 0.7-V voltage at the timer's reset input when the negative output voltage equals the positive input supply voltage in magnitude.

If the output voltage becomes more negative than −15 V, the timer's oscillation is inhibited, and therefore, the drive signal to the voltage doubler is removed. This type of circuit action provides switching-mode regulation of the output voltage.

The voltage doubler deserves a closer look because it may not be immediately apparent how it works. When the timer's output goes positive, capacitor C_1 is charged through diode D_1, and diode D_2 is reverse-biased. When the timer's output becomes negative, some of the charge on capacitor C_1 is transferred to capacitor C_2 through diode D_2, and diode D_1 is now reverse-biased.

As the output from the timer swings positive again, capacitor C_3 charges through capacitor C_2 and diode D_3 to approximately twice the supply voltage. For the timer's negative output swing, this charge is transferred to capacitor C_4 via diode D_4, doubling the output voltage from the timer. Such a voltage-doubler arrangement requires the driving source to supply, as well as sink, current.

The output voltage of the dc-dc converter will track the input supply voltage with reasonable accuracy. If resistors R_1 and R_2 are replaced by a single 100-kilohm potentiometer, the output voltage can be made contin-



For op amps. This dc-dc converter produces a −15-volt output from a +15-V supply input. The IC timer, which is wired as a free-running relaxation oscillator, drives a voltage doubler. The timer is reset so that its output is inhibited if the converter's output tries to go more negative than −15 V. The converter's output is regulated to within ±1% for load currents of up to 30 milliamperes.

uously variable down to zero. To regulate the output more fully against input voltage changes, resistor R_2 may be replaced by an appropriate zener diode. Diodes D_5 and D_6 are optional—they are used to offset the positive 0.7-V reset threshold of the timer to improve the circuit's output-to-input voltage tracking. □

SCR zero-cross trigger limits maximum load power

by Richard Eckhardt
Electronics Consulting & Development, Cambridge, Mass.

A zero-cross trigger for a silicon controlled rectifier will limit the maximum power delivered to a load if it is made to fire the SCR only on alternate cycles of the ac line input. Such an SCR triggering circuit is useful for driving loads rated at less than 110 volts. There are two advantages to limiting SCR conduction in this way—large amounts of power do not have to be wasted through dissipation, and the load can be powered continuously without the need for a power transformer.

With a zero-cross trigger, the SCR is fired only when the voltage across it is at or near the zero point in the driving ac waveform or pulsating dc waveform. Zero-voltage firing minimizes the generation of noise spikes that may occur when the voltage and current to the load are changed too rapidly.

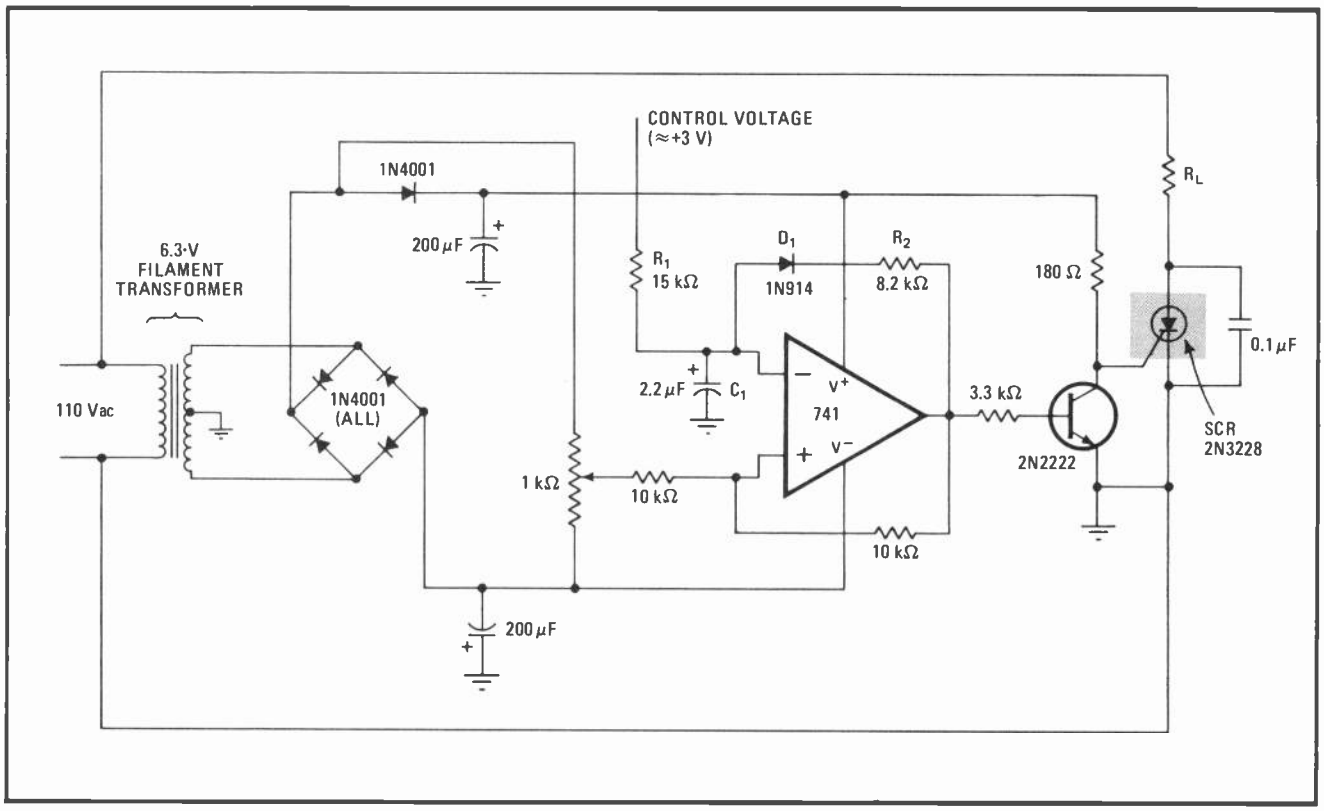
The zero-cross trigger shown here employs a general-purpose operational amplifier as a comparator. The control-voltage input varies the power applied to the load by governing the ratio of SCR on cycles to SCR off cycles. To increase the power supplied to the load, the control voltage is made larger.

Some of the pulsating dc voltage produced by the rectifier bridge is applied to the noninverting input of the op amp. The control voltage, which goes to the op amp's inverting input, charges capacitor C_1 through resistor R_1 until the capacitor's voltage exceeds the minimum point of the pulsating dc voltage.

When this happens, the output of the op amp goes negative, switching off the transistor and permitting the SCR to fire. Since the SCR is triggered at the minimum point of the pulsating dc voltage, the SCR turns on only when the ac voltage across it is at or near zero. The output of the op amp remains low until capacitor C_1 discharges through diode D_1 and resistor R_2.

This capacitor must be charged again by the control voltage before the SCR can be fired again. The charging time of capacitor C_1 determines how many successive cycles of the input voltage are included in the interval between SCR firings.

The circuit's dynamic range is established by the resistance ratio of charging resistor R_1 to discharging resistor R_2. □



Power limiting without power waste. Because this zero-cross trigger fires its SCR only on every other cycle of the ac line, the maximum power delivered to the load can be limited without the need for a power transformer or wasteful power dissipation. The control-voltage input determines the ratio of SCR on cycles to SCR off cycles. The larger the control voltage is, the greater the power to the load.

Phase-locked loop includes lock indicator

by J.A. Connelly and G.E. Prescott
Georgia Institute of Technology, Atlanta, Ga.

One problem with phase-locked loops is that it's often hard to tell exactly when the loop is locked to the input signal. In many applications, it would be very useful to include a lock indicator in a phase-locked loop to display the state of the loop.

For example, in automatic test equipment, the lock indicator would afford a simple, yet efficient, way to measure the tracking and capture ranges of a phase-locked loop. Also, various low-pass filter configurations could be evaluated easily by sweeping the loop's input frequency range. A straightforward implementation for a phase-locked loop with lock indication is shown in the figure.

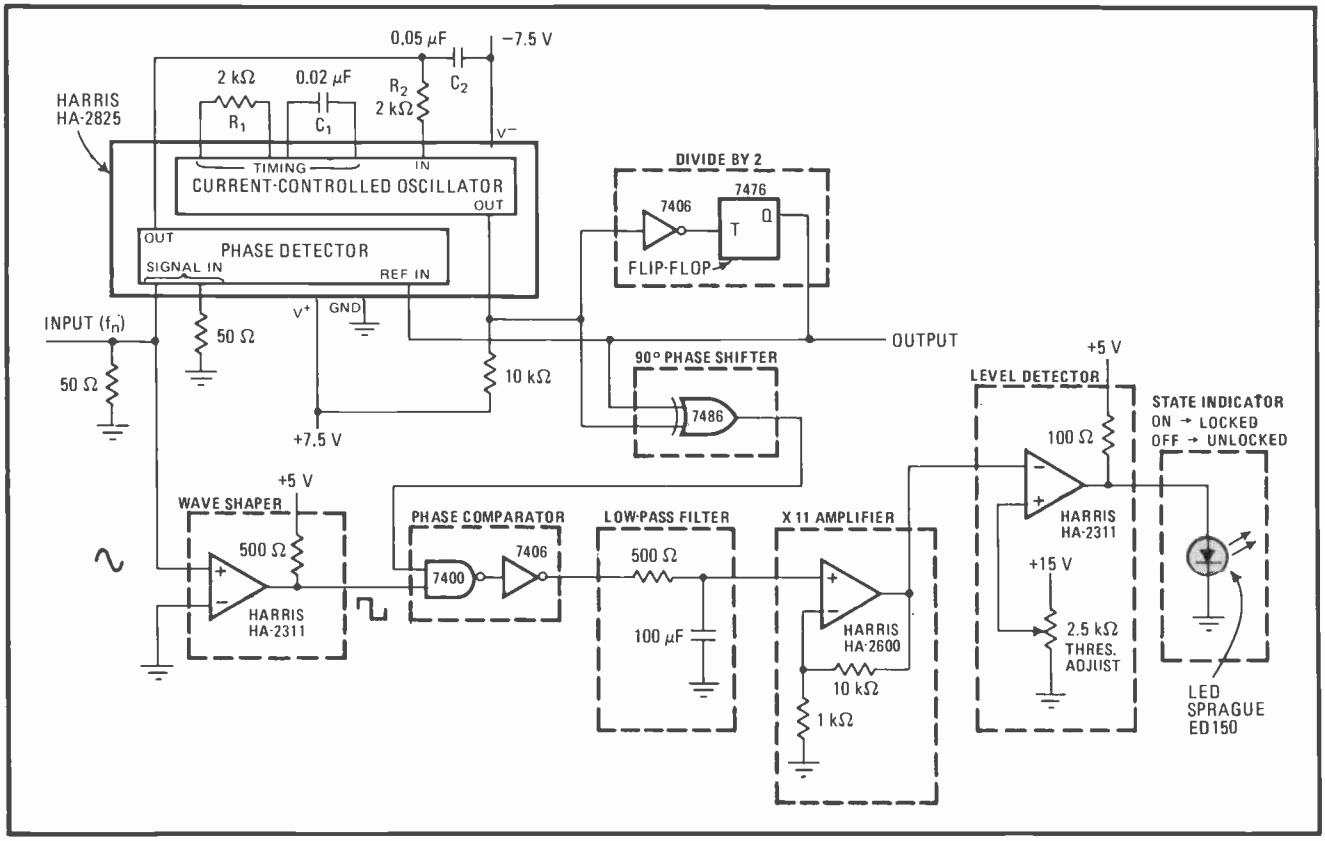
A phase-locked loop can be in its locked state over a range of input frequencies. The center frequency of this range occurs when the frequency of the input signal (f_n) is identical to the free-running frequency of the loop's controlled oscillator (CO). At the center frequency, the output of the CO will be shifted by 90° with respect to f_n. The CO frequency will track variations in f_n until the phase error of the feedback signal with respect to f_n reaches a limit set by the loop gain. For input-frequency variations beyond this limit, the loop reverts to its unlocked mode of operation, and the CO output returns to its free-running frequency.

In the circuit drawn here, the loop's feedback path is altered by breaking the normal feedback loop and inserting a divide-by-2 network. Since this network halves the CO output frequency, the CO free-running frequency must be doubled to achieve normal loop operation.

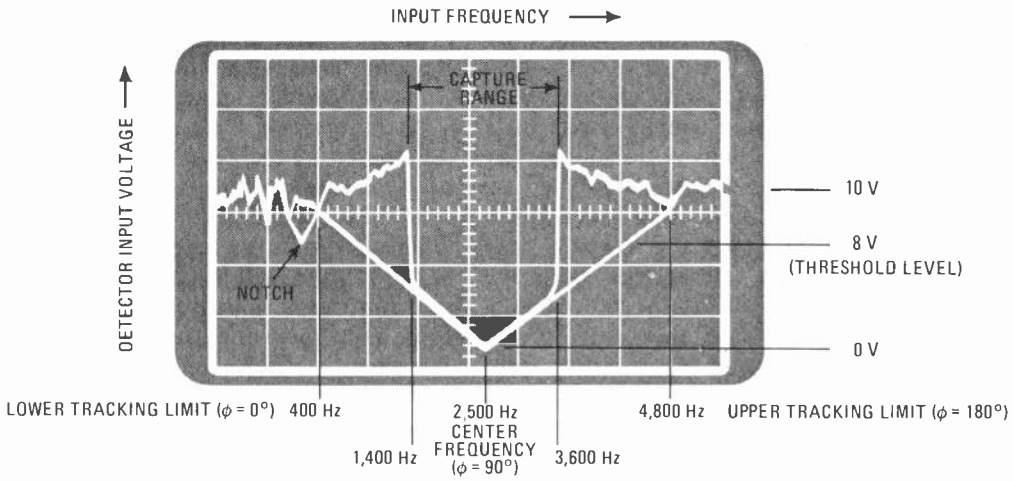
Both the output of the CO ($2f_n$) and the output of the divide-by-2 network feed a phase shifter, which produces a signal that lags the output from the divide-by-2 network by exactly 90°. The signal from the phase shifter is then compared with the input frequency, after this latter signal has been squared up by a wave shaper.

Whenever the input frequency is half the free-running frequency of the CO, the output of the CO will be shifted by 90° with respect to the input. The phase shifter introduces an additional 90° shift, causing the inputs to the phase comparator to be 180° out of phase with each other. Comparing two signals that have the same frequency but that are 180° out of phase produces a constant zero-level output.

However, if the input frequency changes, the inputs



Monitoring loop state. This phase-locked loop has an LED indicator that lights when the loop is locked and goes off when the loop is unlocked. The loop's normal feedback path is opened to accommodate the lock-indicator circuitry. And the free-running frequency of the loop's controlled oscillator must be doubled because of the divide-by-2 network. The circuit's output frequency characteristic is also shown.



to the phase comparator will no longer be exactly 180° out of phase. Instead, they will be skewed somewhat, depending on the phase error between the feedback signal and f_n. Variations in the input frequency cause a series of narrow pulses to be fed into the low-pass filter, which attenuates high frequencies and applies a dc voltage to the level detector.

As the input-frequency deviations from the free-running CO frequency become larger, the phase comparator and low-pass filter produce correspondingly larger dc voltages for the level detector. For a locked loop, the output of the level detector is high, and the LED lock indicator is turned on. When the loop is unlocked, the detector's output goes low, turning off the LED.

For the components shown here, resistor R_1 and capacitor C_1 set the CO free-running frequency at 5,000 hertz, making the input center frequency equal to 2,500 Hz. Resistor R_2 and capacitor C_2 serve as the conventional low-pass filter for the loop. The loop's capture range can be expressed as:

$$\textit{capture range} = \pm(8\pi^2)/[2\pi C_2(R_2+R_{in})]^{1/2}\ Hz$$

where R_{in} is the CO input impedance, which is approximately 500 ohms for the part used here.

The actual output frequency characteristic of the entire loop is also shown in the figure. This waveform is obtained by slowly sweeping the loop's input-frequency range, while monitoring the input voltage to the loop's level detector. The minimum voltage is developed when the loop is locked—the input frequency and the CO output are 90° out of phase. Any input-frequency deviation from this null point will result in a positive dc voltage. The steep edges within the V portion of the characteristic define the capture range of the loop. These abrupt transitions are created as the loop suddenly enters the locked mode from the unlocked condition.

When the input and CO output signals are either 0° or 180° out of phase, the inputs to the phase comparator will be in phase, and the voltage to the detector will be at its maximum level. At this point, the loop becomes unlocked, and the CO and input frequencies are no longer related. The notch appearing at the left end of the V trough is caused by beat frequencies that occur as the loop attempts to capture the input signal. For proper circuit operation over a wide frequency range, the threshold voltage of the level detector should be set lower than the minimum amplitude of this notch.

Through the threshold adjustment, the reference voltage for the level detector can be set as close as is practical to the maximum input detector voltage, without tripping the detector for the unlocked condition. When the input detector voltage drops below this reference level, the output from the detector goes high, lighting the LED to indicate that the loop is locked. In this circuit, the reference voltage is set at approximately 8 V.

If a bank of switchable active filters is used as the loop's normal filter, the lock indicator can serve as a control circuit for changing the tracking and capture ranges of the loop automatically. It does this by switching the loop filter upon loss of track. □

Window comparator needs only one op amp

by Jerald Graeme
Burr-Brown Research Corp., Tucson, Ariz.

Diode gating can considerably simplify the circuitry for a window comparator, reducing it to just one operational amplifier, a single voltage reference element, and a diode bridge. A window comparator indicates whether or not a signal is within a given voltage range for applications such as go/no-go testing. Normally, it requires two op amps and two voltage references, as well as an AND gate.

A signal within the comparator's defined range produces a low output state, while a signal above or below that range produces a high output state. In the conventional window comparator, one op amp detects signals above the acceptable range, and the other op amp de-

tects signals below the range,[1] by comparing the signal against separate voltage references. To provide a single comparator output, the signals from the op amps are combined by an AND gate.

For applications where moderate accuracy, say 1%, is acceptable, the circuit shown here can be used. Since only one op amp is required, there is no longer any need for a gate to combine the outputs from two op amps. Also, the same reference element, a zener diode, now serves to define both the upper and lower voltage limits. Because of this common reference element, the upper and lower limits will be well-matched about zero. For limits not centered about zero, the center of the range can be shifted by connecting bias resistors from the power-supply voltages to the appropriate amplifier input.

Through diode gating, the input signal is directed to the proper amplifier input. Input signals above the positive limit forward-bias diode D_1, pulling the zener voltage upward so that diode D_2 is also forward-biased. A positive voltage is now applied to the noninverting input of the amplifier, causing this device's output to swing to its positive state. The upper range limit, therefore, is the zener voltage plus two forward diode drops ($V_Z + 2V_F$).

A positive output swing is also produced by negative input signals that exceed $-V_Z - 2V_F$. These negative signals will forward-bias diodes D_3 and D_4 so that a negative signal appears at the amplifier's inverting input. Signals within the range defined by the positive and negative voltage limits are not passed by the diode bridge to the amplifier, and the amplifier's output is negative because of the bias voltage from resistor R_1.

The accuracy of this comparator is controlled by the diode voltages at low input frequencies and by the amplifier's gain-bandwidth limit at high input frequencies. Since both the zener and diode voltages are subject to tolerance and temperature variations, the range limits can be in error by several percent. To reduce the temperature sensitivity of the range limits, resistors R_2 and R_3 bias the zener so that its thermal voltage variation approximately cancels those of two junction diodes. (The dc voltage shift introduced by resistor R_1 adds to the amplifier's offset voltage error, making this offset error comparatively small.)

At high input frequencies, the comparator error is dominated by the gain-bandwidth-limited output swing of the amplifier from its positive state to its negative state. This transition occurs when the input signal is disconnected from the amplifier by the diode bridge, leaving only the small voltage developed by resistor R_1 at the amplifier's noninverting input. The limited input drive voltage to the amplifier results in a slow output fall time.

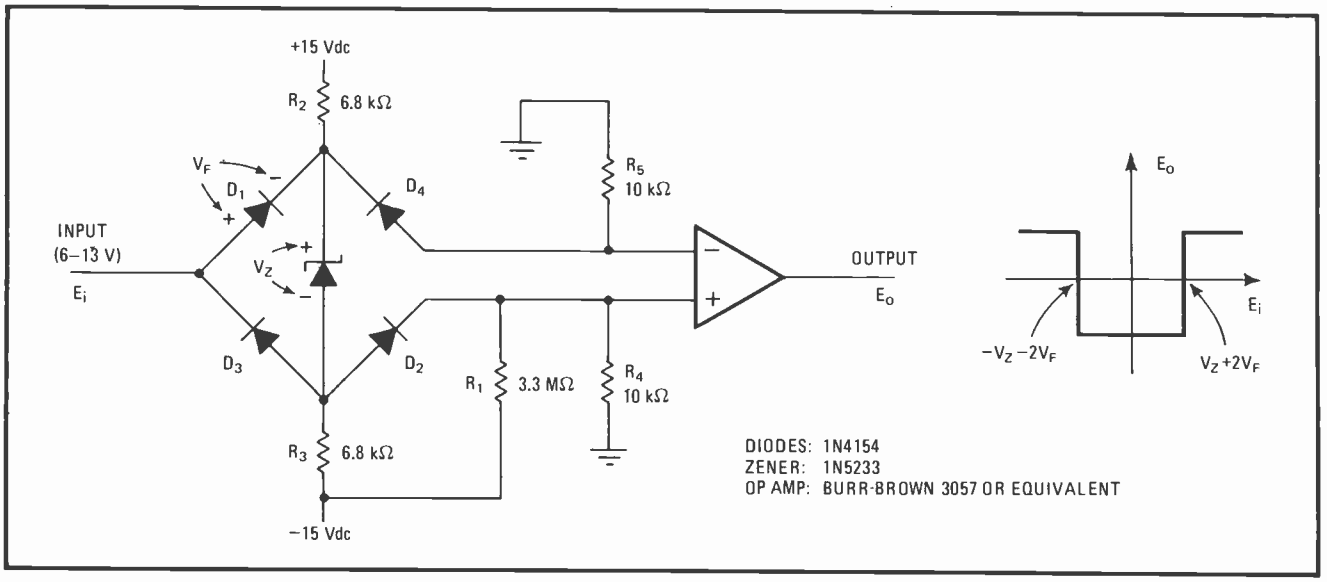
If a compensated op amp is being used in the circuit, its gain-bandwidth product can be improved by removing the device's phase compensation. Or, an uncompensated op amp can be used instead, as is done here. With the uncompensated op amp shown, the window comparator will have a bandwidth of 2 kilohertz and an ac error of only 1%.

There are a couple of other response limitations that should be considered. They are the amplifier's overload recovery delay and the discharging time of the diode capacitances. In order to switch, the amplifier must first recover from its saturated condition—this introduces a time delay. Fortunately, removing the phase compensation from most op amps shortens their overload recovery time.

Another switching delay can be produced by the capacitance discharging time of diodes D_2 and D_4 through resistors R_4 and R_5, respectively. This factor, along with the input resistance, is determined by one of these resistors shunted by either resistor R_2 or R_3. □

REFERENCE

1. "Applications of Operational Amplifiers—Third-Generation Techniques," J. Graeme, McGraw-Hill Inc., 1973.



Saving an op amp. Window comparator for moderate-accuracy applications can be built with only one op amp. The zener diode and the diode bridge determine the circuit's voltage limits, directing positive and negative signals to the appropriate amplifier input. The circuit's output is low for signals within the defined range. D_1 and D_2 conduct for positive signals, while D_3 and D_4 conduct for negative signals.

Two-component light sensor has high voltage output

by Thomas T. Yen
Statham Instruments Inc., Oxnard, Calif.

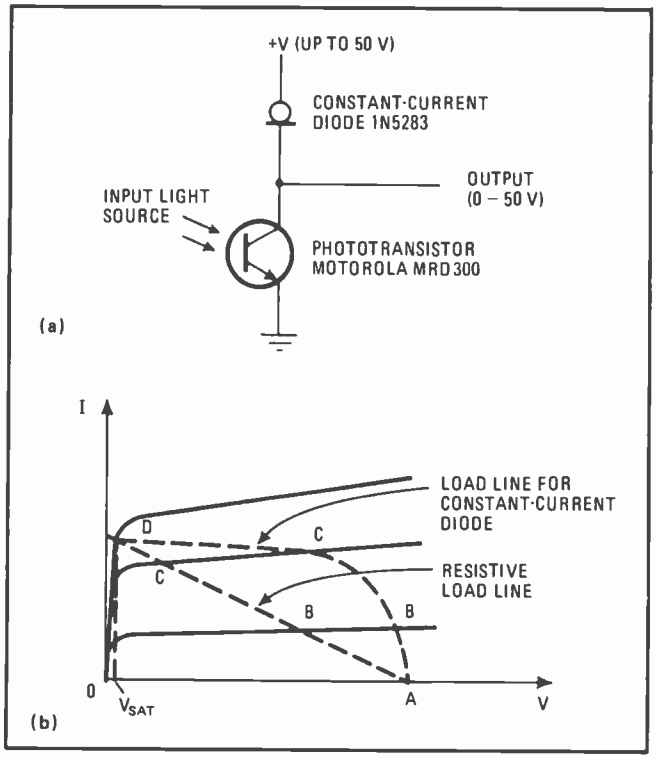
An output voltage of up to 50 volts can be developed by a light-sensing circuit that uses a constant-current diode as the load for a phototransistor. The circuit, which is drawn in (a), provides high noise immunity because its output remains relatively constant until the input light-level threshold is reached. Since the circuit can operate over a wide range of voltages, it is compatible with C-MOS devices. And, at high light levels, it is also compatible with TTL and DTL devices because of the high-current-sinking capability of its phototransistor.

The current-voltage characteristics of a typical phototransistor are shown in (b). The nonlinear load line of the constant-current diode and the linear load line of a resistor, the standard phototransistor load element, are superimposed on the I-V curves for comparison at four light levels.

At level A, the phototransistor is cut off, while at level D, it is saturated. When the input light intensity goes from intermediate level C to saturation level D, or vice versa, the change in the phototransistor's output voltage is far larger for the nonlinear load than for the linear load. In circuit (a), therefore, the output voltage remains high until the input light intensity is large enough for the phototransistor's light current to match the diode's pinchoff current. At this point the circuit's output voltage decreases abruptly and becomes the saturation voltage of the phototransistor.

When the input light changes from bright to dark, the circuit's output voltage rises slowly, as the constant current from the diode charges the phototransistor's collector capacitance. In this circuit, the charging time will be on the order of 100 microseconds. The output rise time can be shortened either by clamping the output to a lower final voltage or by using a diode with a higher current rating.

With the components shown, the circuit is limited to medium-speed (1 kilohertz) applications—for example, an event-counting sensor for industrial purposes. Faster operating speeds can be realized by substituting a photodiode for the phototransistor. But, a photodiode requires a low-current diode, one with a rating on the order of 20 microamperes, and such a constant-current diode is not currently available. Furthermore, integrating the constant-current diode and the phototransistor on the same chip would permit the circuit's risetime to be optimized, because device capacitance could then be minimized through the chip layout. □



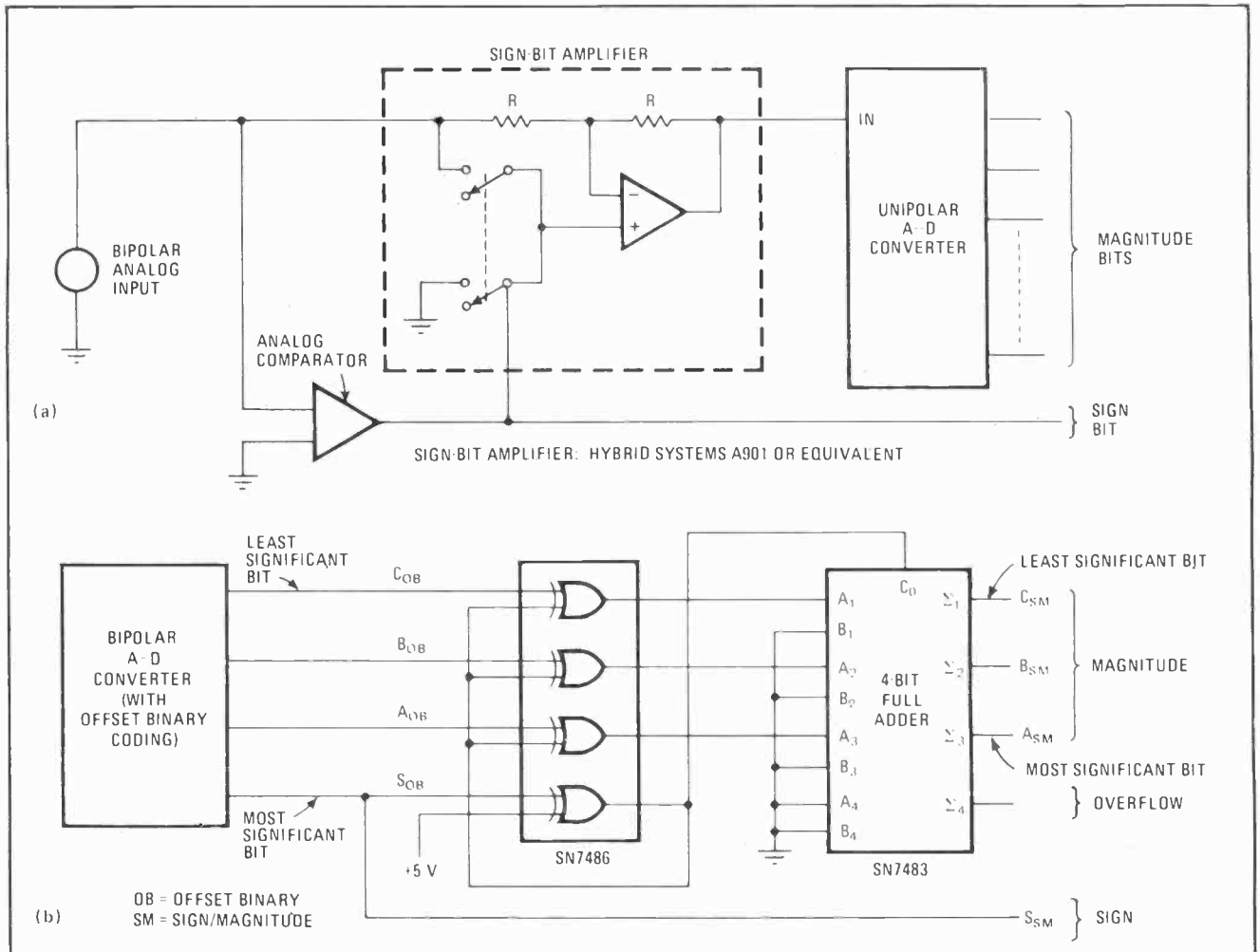
Light detector. Constant-current diode acts as a nonlinear load for a phototransistor so that the output voltage of this light sensor (a) remains high until the phototransistor's current equals the diode's pinchoff current. When the input light threshold is reached, the circuit's output switches to the saturation voltage of the phototransistor, as shown by the I-V curves (b) of a typical phototransistor.

Coding a-d converters for sign and magnitude

by William D. Miller
Hybrid Systems Corp., Burlington, Mass.

Successive-approximation analog-to-digital converters that provide a sign/magnitude type of output coding are not only hard to come by, they also tend to be costly. In a sign/magnitude-coded output, the output bit values are identical for either positive or negative inputs of the same magnitude, and an extra bit (a sign bit) is used to distinguish between the two input polarities. A fairly simple circuit can be used to develop sign/magnitude output coding for either a unipolar converter or a bipolar converter having an offset-binary-coded output.

For the unipolar converter, an analog circuit (a) consisting of a sign-bit amplifier (or an equivalent absolute-value network) and an analog comparator is placed at the input end of the converter. The circuit maintains the



unipolar input to the converter to preserve the magnitude information, while the sign information is generated on a separate line.

Besides accommodating any unipolar code, this approach provides the zero-plus and zero-minus codes that occur within ±½ least significant bit of the true zero input. Parts cost for the circuit, however, is rather high—in the range of $30.

A more economical digital approach (b) can be used if the a-d converter is one of the readily available bipolar types having an offset-binary-coded output. Exclusive-OR gates and full adders are the logic elements needed to convert from the offset binary code to the sign/magnitude code. With this technique, parts cost is only $5 or so for a 12-bit converter.

The figure shows a representative four-bit system. The table compares the offset binary and sign/magnitude codes for the 16 corresponding digital output words. For words 1 through 8, each bit in each code is identical. For words 9 through 16, one code is the two's complement of the other code. For clarity, the most significant bit of each code is assumed to be the same for the same word.

For words 9 through 16, the exclusive-OR gates translate the offset-binary-coded output bits from the converter to a one's complement code. These gates also develop the carry-in bit for the four-bit adder. Three of

CODE CONVERSION

	FROM OFFSET BINARY				TO SIGN/MAGNITUDE			
WORD	S_{OB}	A_{OB}	B_{OB}	C_{OB}	S_{SM}	A_{SM}	B_{SM}	C_{SM}
1	1	1	1	1	1	1	1	1
2	1	1	1	0	1	1	1	0
3	1	1	0	1	1	1	0	1
4	1	1	0	0	1	1	0	0
5	1	0	1	1	1	0	1	1
6	1	0	1	0	1	0	1	0
7	1	0	0	1	1	0	0	1
8	1	0	0	0	1	0	0	0
9	0	1	1	1	0	0	0	1
10	0	1	1	0	0	0	1	0
11	0	1	0	1	0	0	1	1
12	0	1	0	0	0	1	0	0
13	0	0	1	1	0	1	0	1
14	0	0	1	0	0	1	1	0
15	0	0	0	1	0	1	1	1
16	0	0	0	0	← OVERFLOW AT Σ_4 →			
	SIGN	MAGNITUDE			SIGN	MAGNITUDE		

Simple conversion. Analog circuit of (a) enables a unipolar a-d converter to accept bipolar inputs and produce a sign/magnitude-coded output. A sign-bit amplifier or an equivalent absolute-value network performs the polarity selection. The digital circuit of (b) translates the offset-binary-coded output of a bipolar a-d converter to a sign/magnitude-coded output. A four-bit system is shown here.

the adder's output sums provide the sign/magnitude data in the desired two's complement code. The adder's fourth output sum acts as an overflow bit to indicate when the input count exceeds the adder's capacity.

Circuit (b) produces a single nonpolarized output word of 1000 when the analog input is within ±½ least significant bit. Therefore, this circuit is suitable for applications requiring mirror symmetry between corresponding nonzero positive and negative words but not ultrafine resolution about zero. □

Getting extra control over output periods of IC timer

by Arthur R. Klinger
United States Air Force, Sheppard Air Force Base, Wichita Falls, Texas

The 555-type IC timer, which is a versatile circuit building block, becomes even more useful when its low and high output periods are controlled fully. The two circuits shown here, for example, enable the designer to have full-range, completely independent control over the timer's output periods, or, conversely, to make the periods fully dependent so that the output duty cycle can be varied easily over a wide range while keeping output pulse rate constant.

Circuit (a) is for independent control over the periods. Diodes D_1 and D_2 provide separate paths for the timing capacitor's (C) charging and discharging currents. Potentiometers R_1 and R_2 control the high and low periods independently over the timer's complete normal range. Resistor R_3 is included to provide the same minimum fixed resistance in the discharge loop as resistor R_4 provides in the charging loop.

When $R_1 = R_3$ and $R_2 = R_4$, a single calibrated dial can be shared by potentiometers R_1 and R_2 (through a concentric control). If $R_1 = R_2 = 10$ megohms and $R_3 = R_4 = 1{,}000$ ohms, the ratio of high-to-low or low-to-high periods can approach 10,000:1.

Circuit (b), which is only a slightly modified version of circuit (a), makes the periods dependent. As potentiometer R_1 is varied, one period is decreased while the other is increased proportionately. If $R_1 = 10$ megohms and $R_2 = R_3 = 1{,}000$ ohms, the timer's duty cycle will range from about 0.01% to 99.99%, with little change in the output pulse frequency.

In both circuits, the voltage drop across the diodes decreases the effective voltage across the RC timing network, so that the output periods will be smaller than they usually are. Normally, the timer's high output period can be described by:

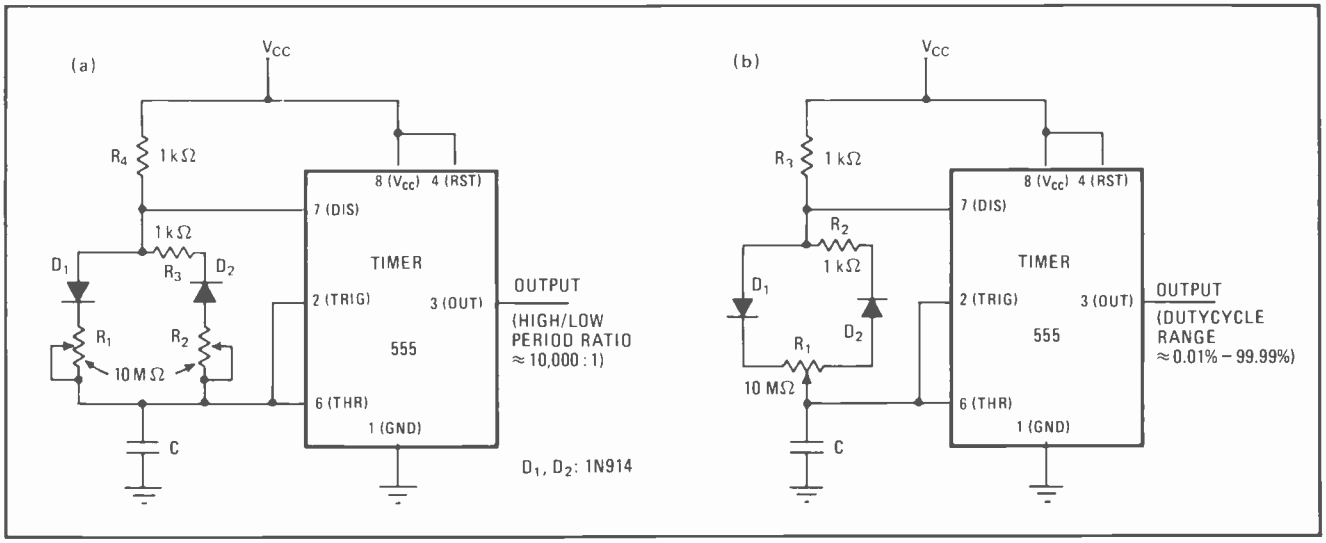
$$T_{HI} = RC\,ln[(V_{CC} - V_1)/(V_{CC} - V_2)]$$

where R is the total resistance in series with timing capacitor C, V_{CC} is the supply voltage, V_1 is the low trigger threshold, and V_2 is the high trigger threshold.

For these circuits, however, the constant voltage drop across the diodes must be accounted for. If each diode drop is approximately 0.6 volt, then:

$$T_{HI} = RC\,ln[((V_{CC} - 0.6) - V_1)/((V_{CC} - 0.6) - V_2)]$$

The lower the supply voltage, then, the greater is the effect of the diode drop. When the timer is operated in its astable mode, the period is roughly 0.76RC for a 15-V supply, and for astable operation with 5-V supply, the period is about 1.4RC. This means that the timer's output periods will be more sensitive to variations in the power-supply voltage, which may be a disadvantage in some applications. □



Simple but effective. When a pair of diodes is used to separate the charging and discharging paths of an IC timer, the high and low output periods of this device can be controlled easily. The periods can be made independent of each other, as in (a), or fully dependent without changing the output pulse frequency, as in (b). The diode drops, however, make the timer more sensitive to supply variations.

Regulator for op amps practically powers itself

by Richard Eckhardt
Electronics Consulting & Development, Cambridge, Mass.

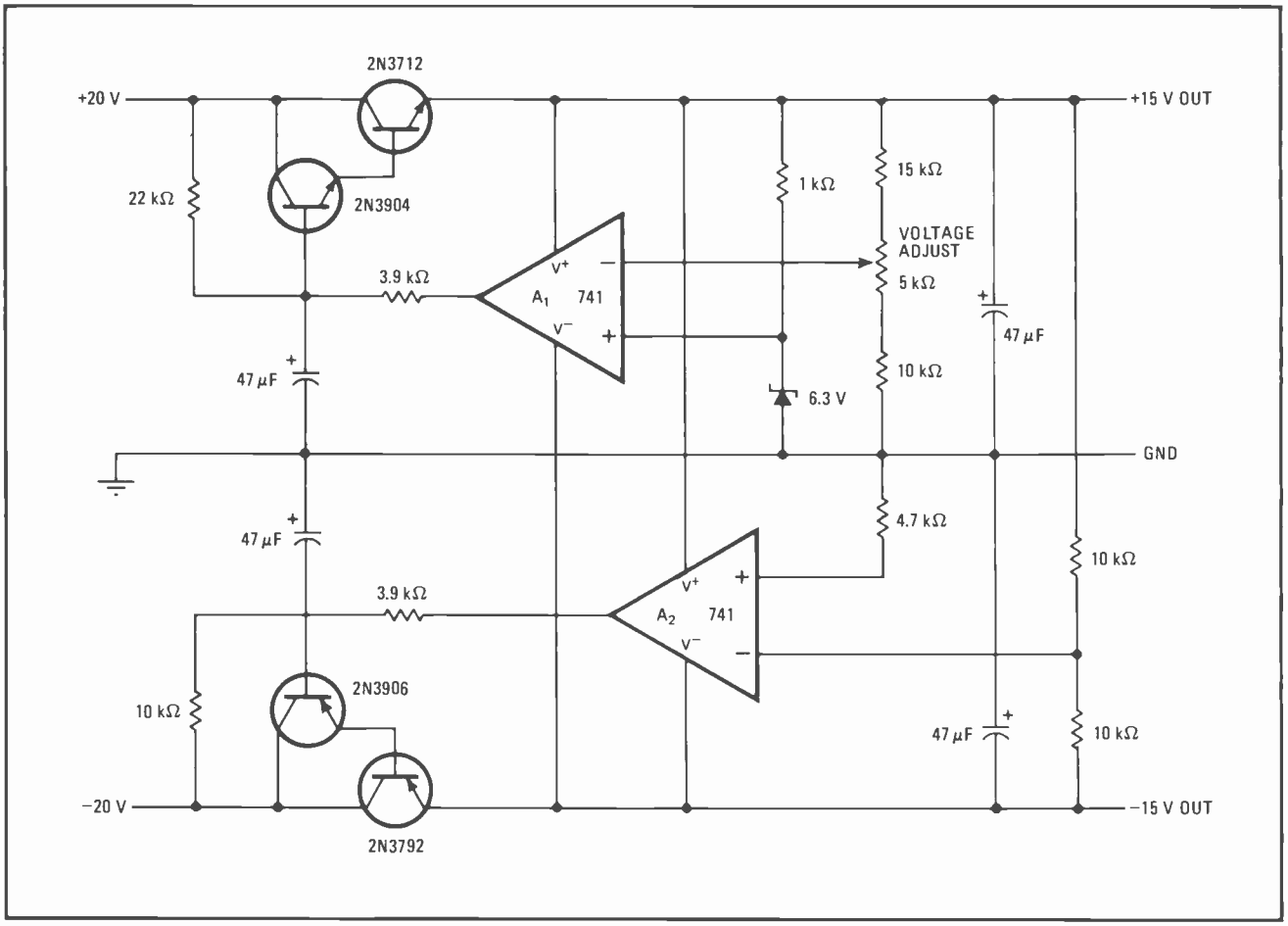
Here's a rather novel way to build a dual-voltage regulator for powering operational amplifiers that offers good tracking, as well as low ripple. Tracking between the two output voltages is good because only one reference source is used for both the positive and negative sides of the regulator. Although the circuit employs two op amps itself, they are powered by their own outputs. Furthermore, the circuit's output-current capability is on the order of several amperes, and output ripple is held to less than 1 millivolt peak-to-peak.

The circuit, shown in the figure, operates as a conventional series-pass regulator on its positive side to develop its +15-volt output. Amplifier A_1 is used for error-detection. The pass transistor for the positive side is biased on from the unregulated +20-V input supply voltage. The output voltage from amplifier A_1 then adjusts this transistor's output.

On the negative side (−15-V output) of the regulator, amplifier A_2 operates as a unity-gain follower. The pass transistor on the negative side is biased in a manner similar to its positive counterpart. The value of the biasing resistor for the negative pass transistor is different from the value of the biasing resistor for the positive pass transistor in order to bring A_2's output closer to the negative supply voltage.

Since amplifier A_2 is wired in a follower configuration, the reference voltage developed by the zener diode can be used for both the positive and negative sides of the regulator. The two output voltages, therefore, track each other within approximately 50 mV.

With suitable modification, the same circuit approach can be used to build a regulator for devices other than op amps that require a split supply. □



Split supply. Regulator circuit for op amps develops ±15-V outputs from a ±20-V unregulated source with less than 1 millivolt of ripple. Although the regulator uses op amps itself, they receive their power inputs from their own outputs. Ampflier A_1 acts as an error detector, while amplifier A_2 is a voltage follower. The single zener voltage reference means that tracking is good between the positive and negative sides.

Analog filter can be programed digitally

by Leonard M. Smithline
Lansing Research Corp., Ithaca, N.Y.

The frequency response of an analog active filter can be selected digitally, yet with the resolution and accuracy of resistive tuning and the dc stability of capacitive tuning. The filter accepts TTL inputs, permitting it to be controlled directly by a computer and making it ideal for electronically switched systems. Furthermore, this digitally programable filter is cost-competitive with mechanically switched types of filters, especially for high-order filter functions.

A simple first-order low-pass filter is drawn in (a). The corner frequency of this circuit is determined by the proportion (α) of the amplifier output voltage (V) that is applied to the feedback capacitor (C). Since applying a voltage of magnitude αV to capacitor C produces the same feedback current as applying a voltage of magnitude V to capacitor αC, the value of capacitor C is effectively multiplied by α. Therefore, the filter's corner frequency can be written as:

$$\omega_b = 1/\alpha R_f C$$

where R_f is the feedback resistor. The over-all dc gain of the circuit is unaffected by loop gain α.

The effective multiplication of capacitance C by gain α can be used to control the filter's corner frequency, as shown in (b). In this circuit, the filter's corner frequency is determined by logic inputs through a voltage-divider setup. Resistor R_a is the upper leg of the divider, while the resistance of the lower leg is selected by enabling the appropriate TTL inverter buffer. When a logic input turns on one of the buffers, the resistor associated with that buffer is shorted to ground.

Resistor R_b provides the appropriate bias voltage for the buffers. The transistor, which is wired as an emitter-follower, reduces the resistance of the voltage divider that is reflected forward in series with capacitor C. This Thevinin equivalent resistance (R_T) is divided by the current gain (β) of the emitter-follower. For the circuit to operate properly:

$$R_T/\beta \text{ must be much less than } R_i \parallel R_f$$

where R_i is the input resistor. Since the dc levels of both the buffers and the transistor are blocked by the capacitor, there is no need for any bias stabilization circuitry.

If the effects of biasing resistor R_c are neglected, programable gain α can be expressed as:

$$\alpha = 1/[1 + (R_a/R_b) + \Sigma R_a G_i]$$

where G_i represents the conductance of those resistors, R_1 through R_n, whose buffers are enabled. The filter's corner frequency now becomes:

$$\omega_b = \omega_o(K + \Sigma R_a G_i)$$

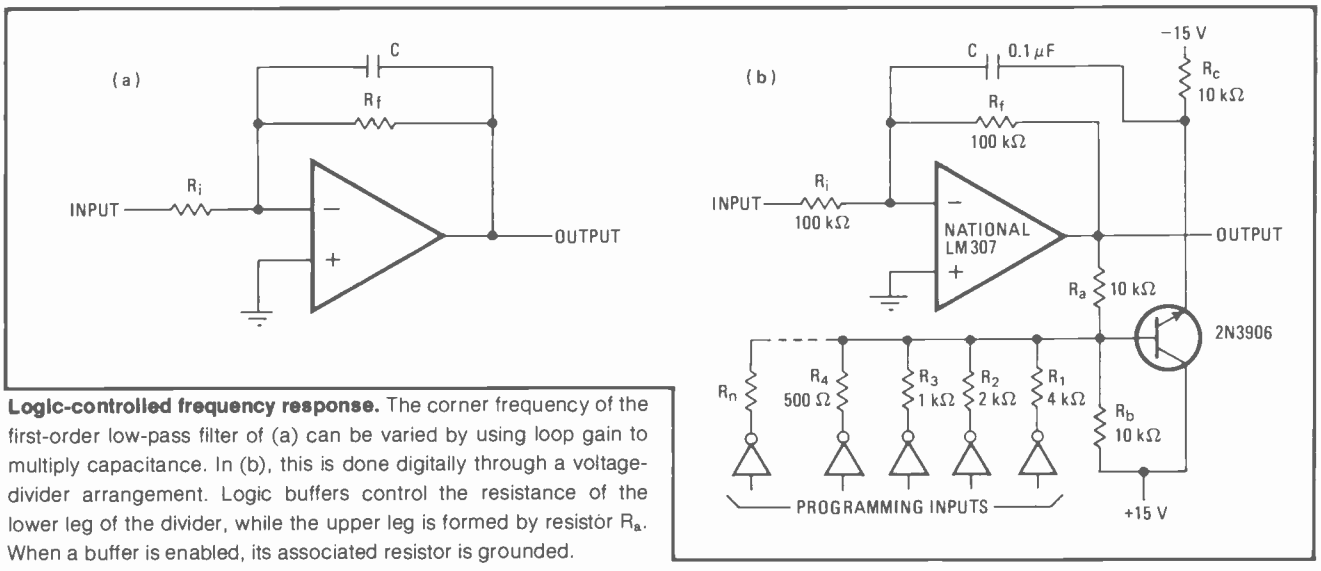
where:

$$\omega_o = 1/R_f C$$
$$K = 1 + (R_a/R_b)$$

The filter's starting frequency—that is, the corner frequency of the filter with none of the logic buffers enabled—is equal to $K\omega_o$. And each increment above this frequency, as each logic buffer is enabled, is equal to $\omega_o R_a G_i$. Since the effects of the enabled buffers are additive, the filter can be programed to accept either standard binary codes or a binary-coded-decimal input. For the component values cited in the figure, ω_o is 100 radians/second, K is 2, the starting frequency is 200 rad/s, and the frequency increment is 250 rad/s.

Moreover, the programing approach that is shown here can be extended to higher-order filters through the use of either the standard biquad or state-variable filter configurations.[1,2] □

REFERENCES
1. A.E. Schultz, "Active Filters Are Moving toward Standardization," Electronic Products, June 18, 1973
2. G.E. Tobey, J.G. Graeme, L.P. Huelsman, "Operational Amplifiers—Design and Applications," McGraw-Hill Inc., 1971



Logic-controlled frequency response. The corner frequency of the first-order low-pass filter of (a) can be varied by using loop gain to multiply capacitance. In (b), this is done digitally through a voltage-divider arrangement. Logic buffers control the resistance of the lower leg of the divider, while the upper leg is formed by resistor R_a. When a buffer is enabled, its associated resistor is grounded.

Attenuating transients in analog FET switches

by Leland Shaeffer
Siliconix Inc., Santa Clara, Calif.

Analog field-effect-transistor switches may be high-speed devices, but the faster they are toggled, the greater is the risk of unwanted output switching transients. The amplitude of these glitches or spikes can be greatly attentuated by synchronizing the toggling of one FET switch with a second FET switch through logic pulses that have variable rise times and fixed fall times.

Undesirable spiking can occur at the output of an analog switch during toggling because, inside the device, charge can be coupled through either its gate-source or gate-drain capacitance. Previous attempts to cancel these glitches by applying out-of-phase spikes from a second switch failed because turn-on and turn-off times generally vary too much between devices.

In the circuit shown here, TTL inverters having open-collector outputs are used to develop the synchronizing logic pulses. Since these inverters have a pull-down current that is an order of magnitude greater than their pull-up current, the rise time of their output pulses can be increased without appreciably affecting the fall time of their output pulses. Fixed resistors (R_L) establish the pull-up currents for the inverters.

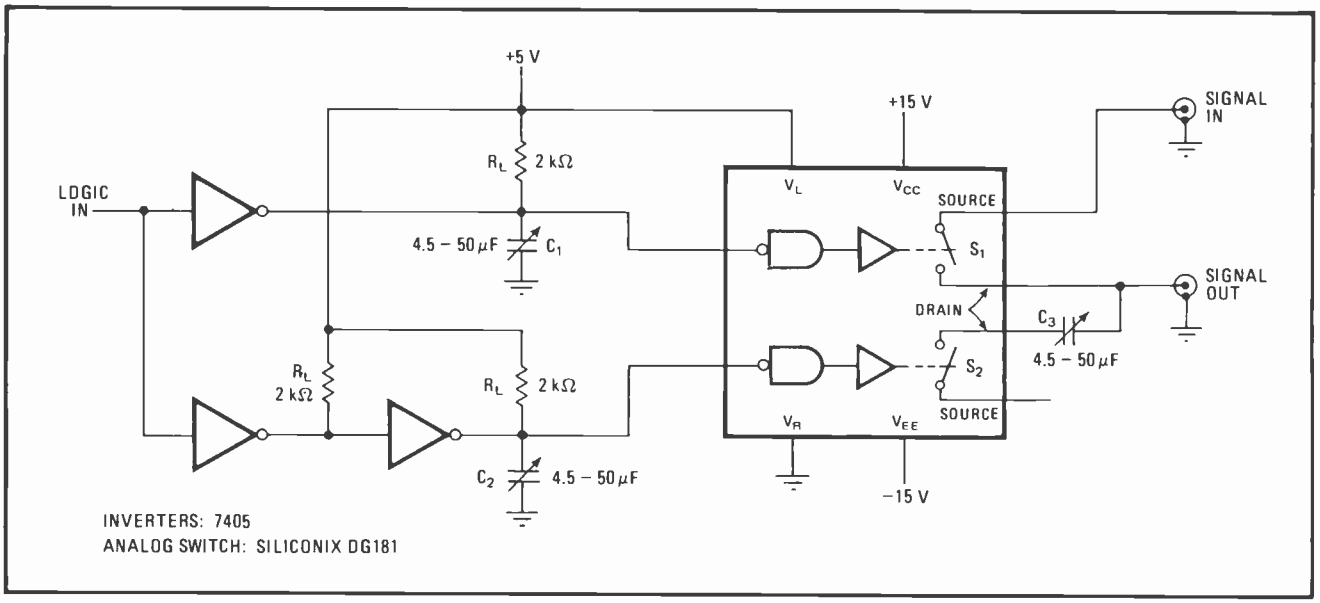
The output rise times of the inverters determine the times required to reach the toggling thresholds of analog switches S_1 and S_2. For the FET devices used here, this threshold is approximately 1.4 volts. Variable capacitors (C_1 and C_2) at the outputs of the inverters permit the rise times of these units to be set at the values needed to synchronize switches S_1 and S_2.

Now the turn-on of switch S_1 can be made to coincide with the turn-off of switch S_2, and the turn-off of S_1 can be synchronized with the turn-on of S_2. When the switches are properly matched in this way, the transients appearing at the output of S_1 can be reduced by a factor of 5 or more if R_L is greater than or equal to 10 kilohms and C_1 and C_2 are about 12 picofarads. For R_L = 75 ohms, the magnitude of the unwanted transients will at least be halved.

Transient attenuation can be improved still further by connecting a zener diode (a 6.8-v device, in this example) shunted with a bypass capacitor in series with the negative power supply. The glitches will then be reduced by an additional factor of 2 for both R_L = 75 ohms and R_L = 10 kilohms. However, the analog output voltage swing, which is normally +15 v to -7.5 v, will now be limited to +15 v and -½ v.

To adjust the circuit properly, first set capacitor C_3 at its minimum value and adjust capacitor C_1 for a minimum turn-off transient. The value of capacitor C_3 is then increased until maximum transient cancellation is obtained. Next, capacitor C_2 is adjusted for a minimum turn-on transient. Capacitors C_1 and C_2 will interact slightly with each other, and some compromise may be necessary in the adjustment of C_3 for minimum turn-on and turn-off transients.

In the circuit drawn in the figure, only one signal source is used, and switches S_1 and S_2 provide single-pole, single-throw switching action. To accommodate a second signal source and obtain single-pole, double-throw action, the drain of S_1 is connected directly (without capacitor C_3) to the drain of S_2. The second signal source is then applied to the source terminal of switch S_2. When the switches are wired in this manner, the make-before-break interval is about 30 nanoseconds. □



Squelching spikes. Switching transients at the output of an analog FET switch can be greatly attenuated by synchronizing the turn-on and turn-off of one switch with those of a second switch. Open-collector TTL inverters produce logic pulses whose output rise times can be varied while their output fall times remain fixed. The turn-on of switch S_1 is made to coincide with the turn-off of switch S_2, and vice versa.

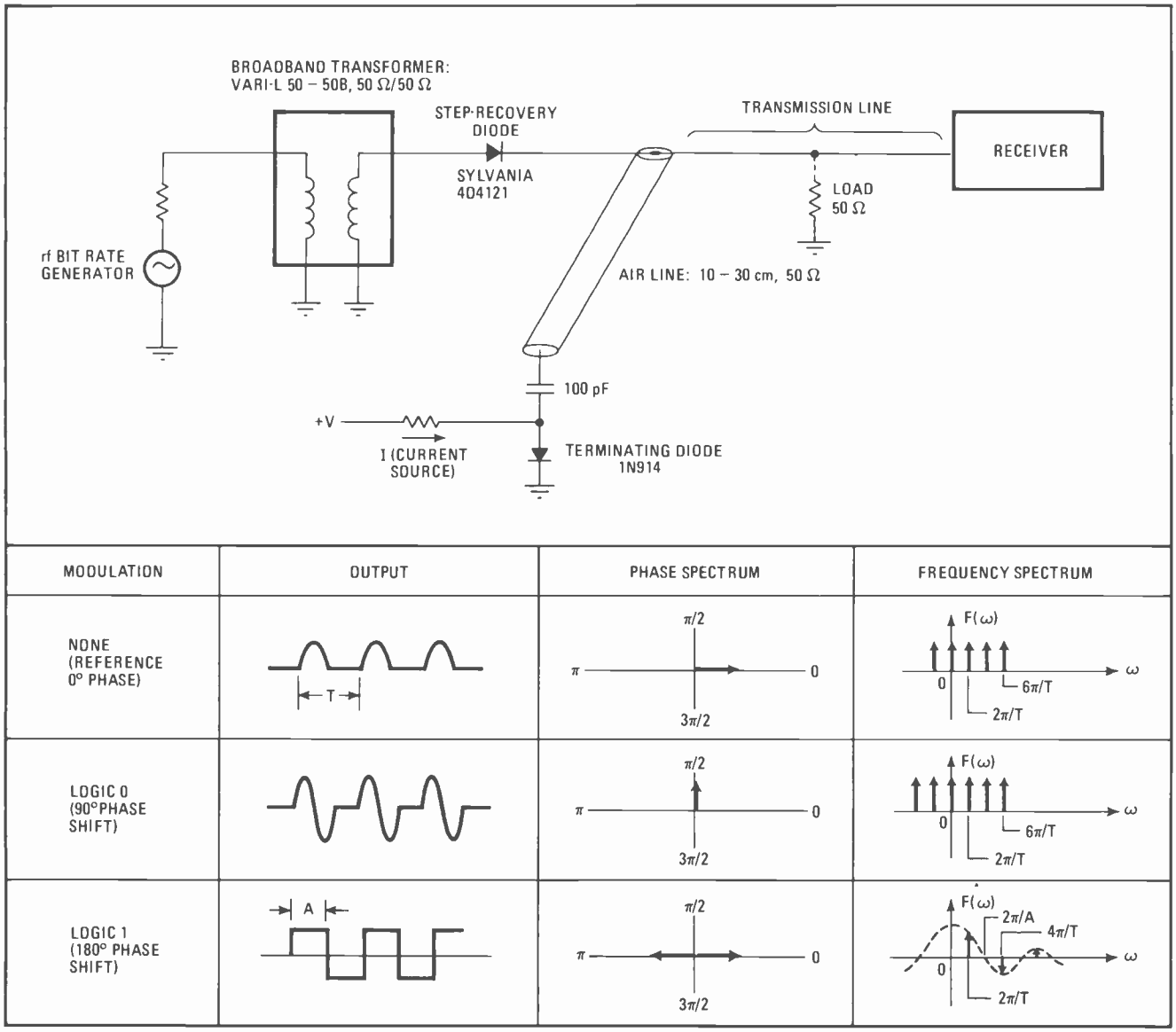
Coherent phase modulation attains data rates of 100 MHz

by Roland J. Turner
General Electric Co., Space Division, King of Prussia, Pa.

Though phase-modulation schemes have till now been limited to modulation rates at video frequencies of 5 megahertz or less, a new technique permits 100- to 200-MHz data rates. The key is an ordinary step-recovery diode that produces a three-level phase code by the simple means of varying the reflection coefficient of the transmission line.

In the modulation setup shown in the figure, the short air line is terminated with an rf diode, whose state determines the reflection coefficient of the transmission line. The state of this terminating diode is established by its drive current. A type 1N914 device is used here, but a hot-carrier or p-i-n diode could be used instead.

The step-recovery diode generates an impulse function each time the input rf sine wave passes through zero in the negative-going direction. This impulse function, which occurs at the input rf bit rate, establishes the



High-speed transmission. Data can be transmitted at rf rates of 100 to 200 megahertz with this coherent-phase-modulation scheme. A three-level phase code is set up by changing the reflection coefficient of the transmission line by means of the terminating diode at the end of the air line. The step-recovery diode acts as a waveform generator, producing impulse, doublet, and square-wave functions.

setup's reference phase (no modulation). For this case, the transmission line is terminated in its characteristic impedance, and there is no reflection. Therefore, the reference phase is represented by a 0° phase shift.

As the sine-wave drive signal reverse-biases the step-recovery diode, this device's capacitance drops radically. However, because of the minority-charge storage in the diode, the current charge is not neutralized quickly, and it forces the voltage across the diode to rise very rapidly. The result is an impulse function that lasts only 1 to 2 nanoseconds.

When there is a logic 0 at the end of the air line, this line is terminated in an impedance that's low in relation to the characteristic impedance of the transmission line. The reflection coefficient now is −1, and a doublet waveform is produced at the step-recovery diode. The phase difference between the impulse and doublet waveforms is 90°.

When there is a logic 1 at the end of the air line, this line is terminated in a high impedance with respect to the characteristic impedance of the transmission line. The reflection coefficient becomes +1, and the step-recovery diode generates a double-width square wave, which is 180° out of phase with the reference impulse function.

The three waveforms form a flat comb spectrum with coherent phase modulation on all spectral lines. This means that the phase from one spectral line to the next remains the same. The coherent phase modulation can be used to represent a three-level code in the phase domain.

The 0° phase, which is represented by the impulse function, can be used in a passive receiver to demodulate the other two discrete phases—the 90° and 180° shifts produced by the doublet and square-wave functions. These latter two phases can then represent a binary code in the phase domain that provides coherent phase modulation on all spectral lines of the comb spectrum. For an rf bit rate of 100 MHz, a spectral line will occur at multiples of 100 MHz, up to about 1 gigahertz.

With this type of phase coding, data can be transmitted at half the rf bit rate. For example, if the basic rf bit rate is 100 MHz, information can be transmitted at 50 million bits per second. Additionally, the redundant coherent reception on the many spectral lines makes the receiver immune to Johnson or man-generated noise.

The modulation scheme can also be used for a broadband rf impulse noise jammer by modulating the current of the terminating diode with white video noise. Or, it can be the basis for an rf test function generator for evaluating the transient response of communication subsystems to complex excitation.

The output amplitude of the modulation circuit is 1 volt peak into 50 ohms for the impulse and square-wave functions and 2 V, peak to peak, into 50 ohms for the doublet function. □

Single switch regulates number of pulses

by Mahesh Bhuta
IBM Corp., General Products division, San Jose, Calif.

A simple SCR ring counter or a serial-in/parallel-out shift register will make a pulse generator produce a predetermined number of pulses at the activation of a single switch. The number of pulses generated depends on which switch is closed. A pulse frequency of 100 kilohertz is easily attainable.

Circuit (a), which contains the SCR ring counter, employs a conventional astable multivibrator as its basic pulse source. Transistors Q_1 and Q_2 make up this multivibrator. When any one of the switches is closed, transistor Q_1 turns on, triggering the astable.

The astable includes an SCR so that transistor Q_2 will always saturate before transistor Q_1. When Q_2 generates the first output pulse, the rising edge of this initial pulse fires SCR_A, enabling the astable to operate in its free-running mode. Bleeder resistor R_B provides the holding current for SCR_A.

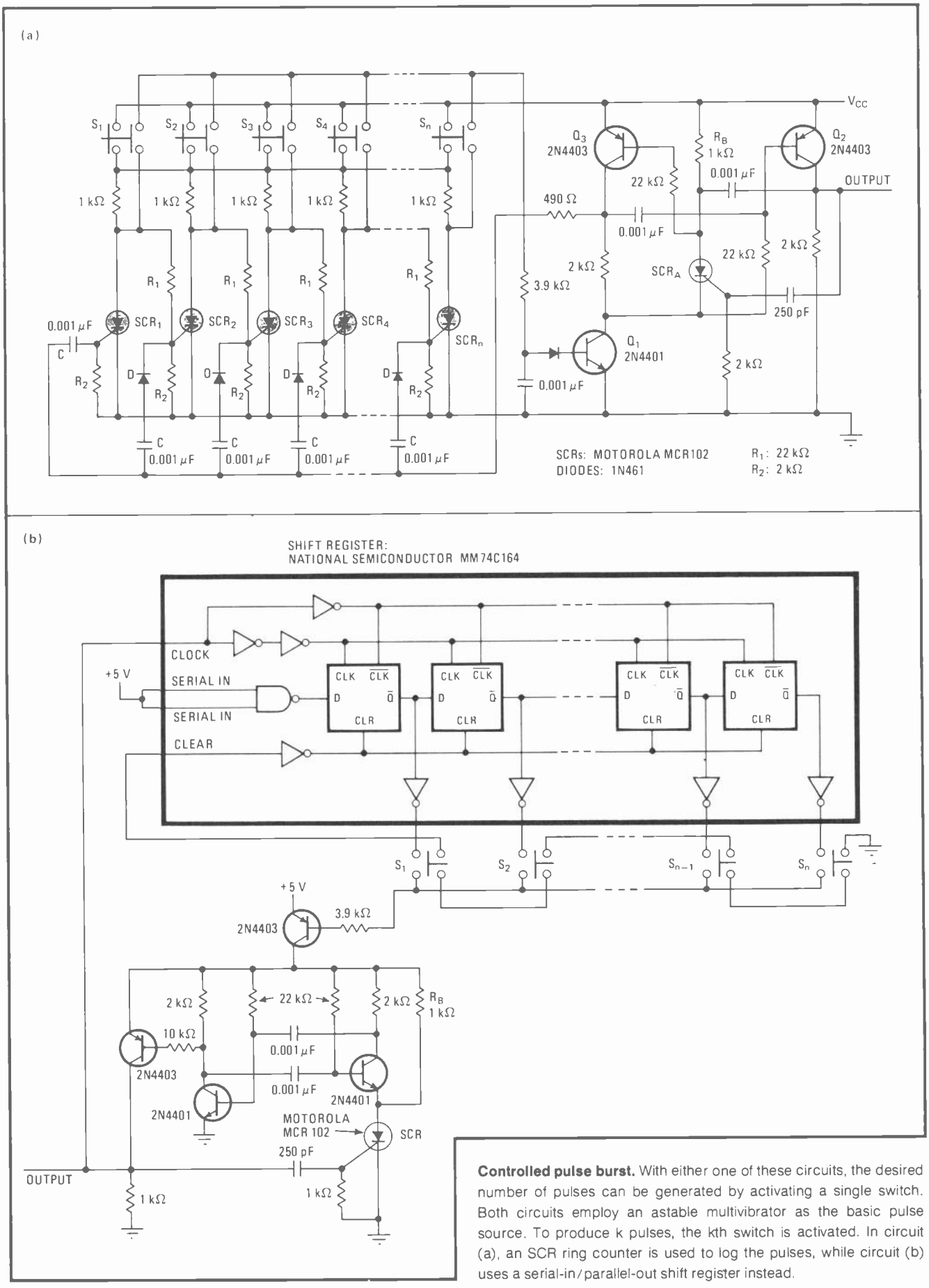
The output from transistor Q_3 is fed to the SCR ring counter. Capacitors C, diodes D, and resistors R form the steering circuit that enables the appropriate pulse from Q_3 to fire the appropriate number of SCRs. If k pulses are desired, the kth switch is activated, the astable will generate k pulses, and the kth pulse will fire the kth SCR, making its anode go to 0.3 volt. This immediately deprives transistor Q_1 of its base drive, and the astable is turned off.

When the kth switch is released, the power to the SCR counter is removed, and the SCRs are switched off. The counter is automatically reset so that it is ready to generate the next desired set of pulses.

The SCR counter can be replaced with a serial-in/parallel-out shift register, as shown in (b). The register's SERIAL inputs are tied high. When the switches are in their normally closed positions, the register's CLEAR input and all its outputs are low.

Transistors Q_1 and Q_2 are connected as an astable multivibrator. When any one of the switches is activated, transistor Q_1 turns on. The rising edge of the first pulse from transistor Q_2 will trigger the SCR, which will stay on because of bleeder resistor R_B.

The output pulses from the astable provide the clock signal for the shift register. Each pulse advances the register until the kth output—the one that is connected to the base of transistor Q_1 through the kth switch—goes high. Once this happens, the astable switches off. When the kth switch is released, the register's CLEAR input goes low, and the shift register is automatically reset. The next set of pulses can now be generated. □



Controlled pulse burst. With either one of these circuits, the desired number of pulses can be generated by activating a single switch. Both circuits employ an astable multivibrator as the basic pulse source. To produce k pulses, the kth switch is activated. In circuit (a), an SCR ring counter is used to log the pulses, while circuit (b) uses a serial-in/parallel-out shift register instead.

Analog gate and zener diode give 70-dB isolation at 80 MHz

by Roland J. Turner
General Electric Co., King of Prussia, Pa.

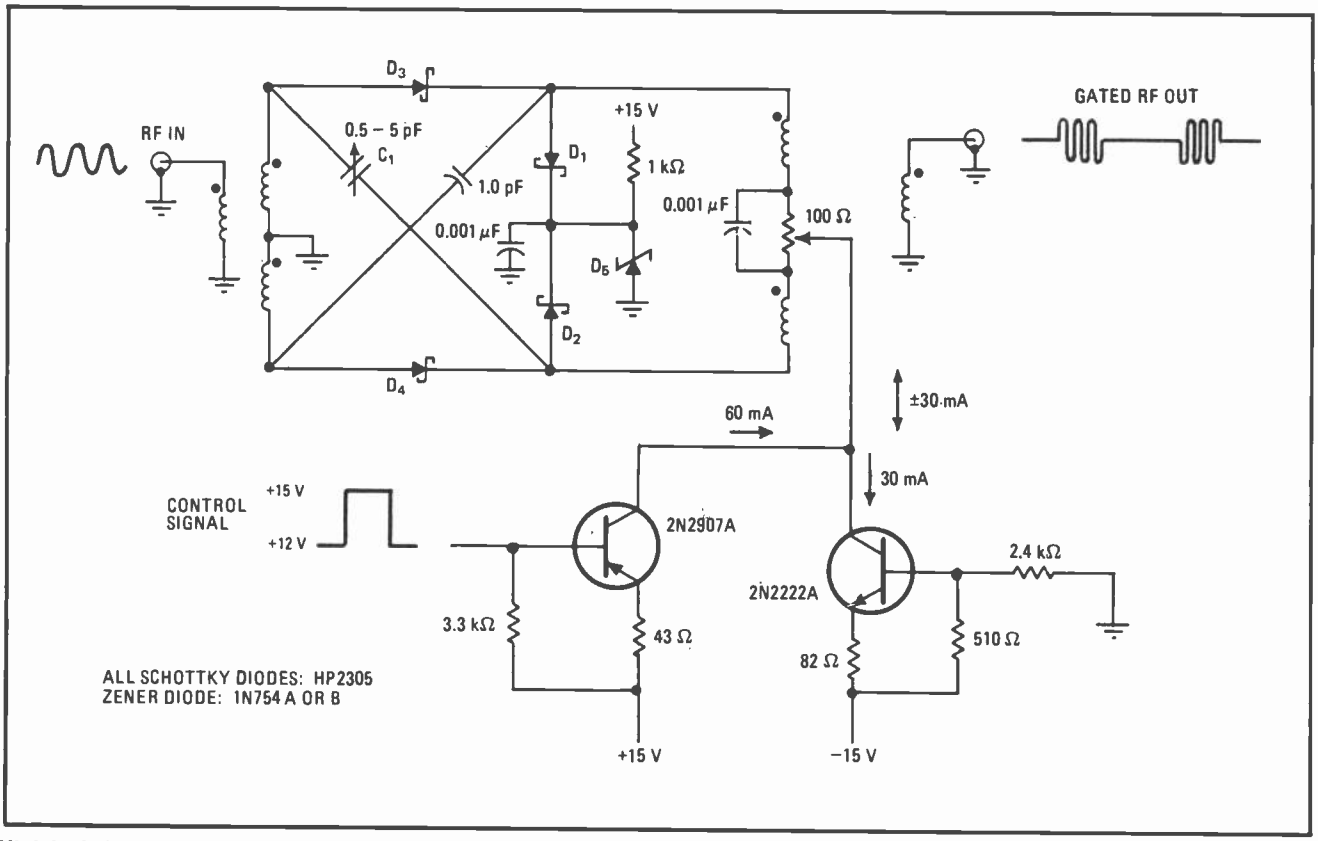
When conventional double-balanced Schottky diode mixers are used as analog signal gates, they have two serious limitations: the "off" impedance of a series diode offers a switch isolation of less than 40 decibels, and the peak radio-frequency input signal cannot exceed the series diode's forward blocking voltage—500 millivolts at room temperature, but falling to 300 mV at higher temperatures. An rf analog gate with both larger signal-handling capability and higher "off" isolation would be very useful, for example, in a pair of switches controlling a transmitter and receiver that share a common antenna.

The analog gate shown in the diagram achieves an "off" isolation of as much as 70 dB at 80 megahertz without using matched diodes. When +30 milliamperes is supplied to the gate, it turns on shunt diodes D_1 and D_2, while the series diodes D_3 and D_4 are reverse-biased by a voltage equal to the zener voltage at D_5 minus the positive swing of the input signal. With the gate biased off in this way, variable capacitor C_1 is trimmed, so that out-of-phase signals cancel signal leakage through the gate.

With a 6-V zener diode, this circuit isolates input signals of as much as 10 V peak to peak—whereas the mixer gate cannot handle even 1 V without letting the signal break through.

On the other hand, when the current is −30 mA, diodes D_3 and D_4 are forward-biased and the shunt diodes D_1 and D_2 become reverse-biased. The Schottky diodes have a dynamic impedance of 10 ohms, which is much less than the typical antenna impedance as seen from this gate (about 200 ohms). Thus the input signal passes through the gate with an insertion loss of less than 0.50 dB.

The gate's on-off status is controlled by the current source shown at the bottom of the diagram. When the control signal is at 12 V, the pnp transistor on the left is turned on, supplying +60 mA—half to the gate to turn it off, and half to the npn current sink on the right. But when the control signal rises to 15 V, the pnp transistor is cut off and the npn device, which stays on, reverses



High isolation. Control signal (lower left) turns on pnp transistor, providing +30 mA to gate circuit at top, to turn it off and block passage of rf signal to antenna. When control is up, npn device takes over, drawing −30 mA from gate and turning it on. Zener voltage minus positive swing of input signal establishes reverse bias on series diodes, achieving isolation of as much as 70 dB at 80 MHz.

the current passing through the gate connection.

Both input and output transformers are conventional components, with bifilar 1:1:1 windings on Indiana General Q-3 core material. The center tap of the input transformer is grounded, while that of the output is split. At this point an RC network collects the -30-mA current when the gate is on. Because the two shunt diodes may have different voltage drops, the resistance is a potentiometer that can be adjusted to eliminate any dc bias at the output. □

Single op amp compares bipolar voltage magnitudes

by F.N. Trofimenkoff and R.E. Smallwood
University of Calgary, Alta., Canada

The operational-amplifier bridge circuit shown in Fig. 1 is a window comparator for bipolar signals. It indicates when the magnitude of the input signal exceeds a preset value. Selection of resistor values sets positive and negative trigger levels independently, so that the trip levels for the two polarities need not be the same.

To analyze the circuit, first ignore the output clamping diode. The input diodes isolate one of the two signal paths, depending on the polarity of e_i. For e_i positive:

$$e_o = -(e_i - e_d)(R_2/R_1) - e_r(R_2/R_3)$$

where e_d is the voltage drop across the diode when it conducts. For e_i negative:

$$e_o = (e_i + e_d)\frac{[1+(R_2/R_3)+(R_2/R_6)]}{[1+(R_4/R_5)]} - e_r(R_2/R_3)$$

The switch-over points are defined by setting $e_o = 0$ in each of these expressions. For e_i positive:

$$(e_i - e_d) = e_r(R_1/R_3) \quad (1)$$

and for e_i negative:

$$(e_i + e_d) = \frac{-e_r[1+(R_4/R_5)]}{[1+(R_3/R_2)+(R_3/R_6)]} \quad (2)$$

If the positive and negative trip levels must have the same magnitude, then the coefficients of e_r in equations (1) and (2) are equal. The equality reduces to:

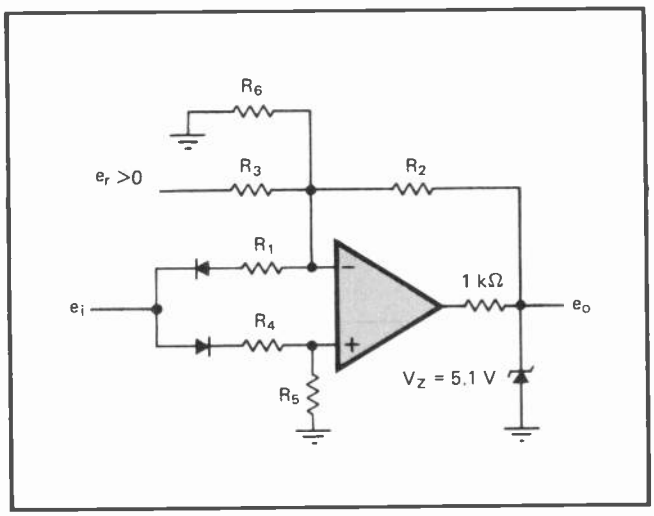
$$[1+(R_3/R_2)+(R_3/R_6)] = [1+(R_4/R_5)](R_3/R_1) \quad (3)$$

If the switching levels are different, equations (1) and (2) must be used to determine the resistor ratios. But regardless of the levels, R_2 is very large and may even be infinite—that is, the circuit may have an open-loop configuration—to provide the maximum gain and thereby produce a sharp transition between the output states at the switch-over points.

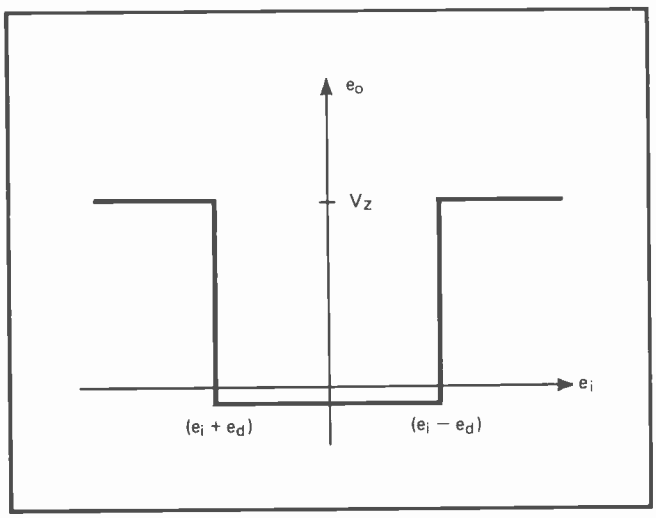
The circuit may be simplified if, for example, the reference voltage is greater than the desired switch-over point. In that case, $R_4 = 0$. If it is less, then R_6 is omitted from the circuit. For symmetrical switching, making $R_4 + R_5$ approximately the same as R_1 equalizes the diode currents, thus more nearly matching the diode forward voltage drops.

If now the output clamp is taken into account, it keeps the lower level of the output from going more than very slightly negative, as shown in Fig. 2. The complement of this transfer function is obtained by changing the polarities of the input diodes and the reference voltage.

As a design example, suppose ±10.0-volt switch-over points are required, and $e_r = 15$ V. Assume $e_d = 0.5$ V, and use 11 kilohms for R_1 and an open circuit for R_2. Equations (1) and (3) show that $R_3 = 17.4$ kilohms, $R_4 = 0$, $R_5 = 11$ kilohms, and $R_6 = 29.9$ kilohms. Building the circuit with these component values results in measured switch-over points of -10.12 and +10.15 V. The actual switching is completed during a change in



1. Comparator. Amplifier output is low when the input is between two levels set by choice of resistances, and high when outside these levels. The two trigger levels are independent.



2. Transfer function. Output clamp keeps low level only a fraction of a volt below ground. The complementary function is obtainable by inverting the two input diodes and the reference voltage.

the input of less than a millivolt, because the amplifier gain is high and the open-loop configuration is used.

This simple circuit has some disadvantages. Among these are the forward voltage drops of the input diodes, which are significant. Consequently, the circuit cannot be operated near $e_i = 0$. These voltage drops can be minimized with germanium or hot-carrier diodes.

Another disadvantage is that the switch-over points are temperature-sensitive, because the diode forward drops have a temperature coefficient. Finally, the speed of the circuit depends on the type of operational amplifier and on the clamping scheme. Using a comparator in place of the operational amplifier permits somewhat faster switching. □

Regulating voltage with just one quad IC and one supply

by R. A. Koehler
York University, Toronto, Canada

Full-range, high-performance power supplies are often bulky and expensive because they require two independent voltage sources—one main and one reference—with associated rectifiers, filter capacitors, and reference regulator circuitry.

But only one unregulated source of about 26 volts dc and one ground-sensing quad operational amplifier are necessary in a regulated power supply that provides 1 ampere at 0 to 20 V with foldback current-limiting and overload indication. It achieves line and load regulation within ±0.02% over the full range of load conditions, even when the input voltage varies between 24 and 28 V dc. When the regulator is quiescent, its current requirement amounts to less than 10 milliamperes.

Amplifier A_1 is a self-biased, constant-current amplifier that provides a stable reference voltage [*Electronics*, March 13, 1972, p. 74]. Its output, V_1, depends on the breakdown voltage V_z of the zener diode, D_1:

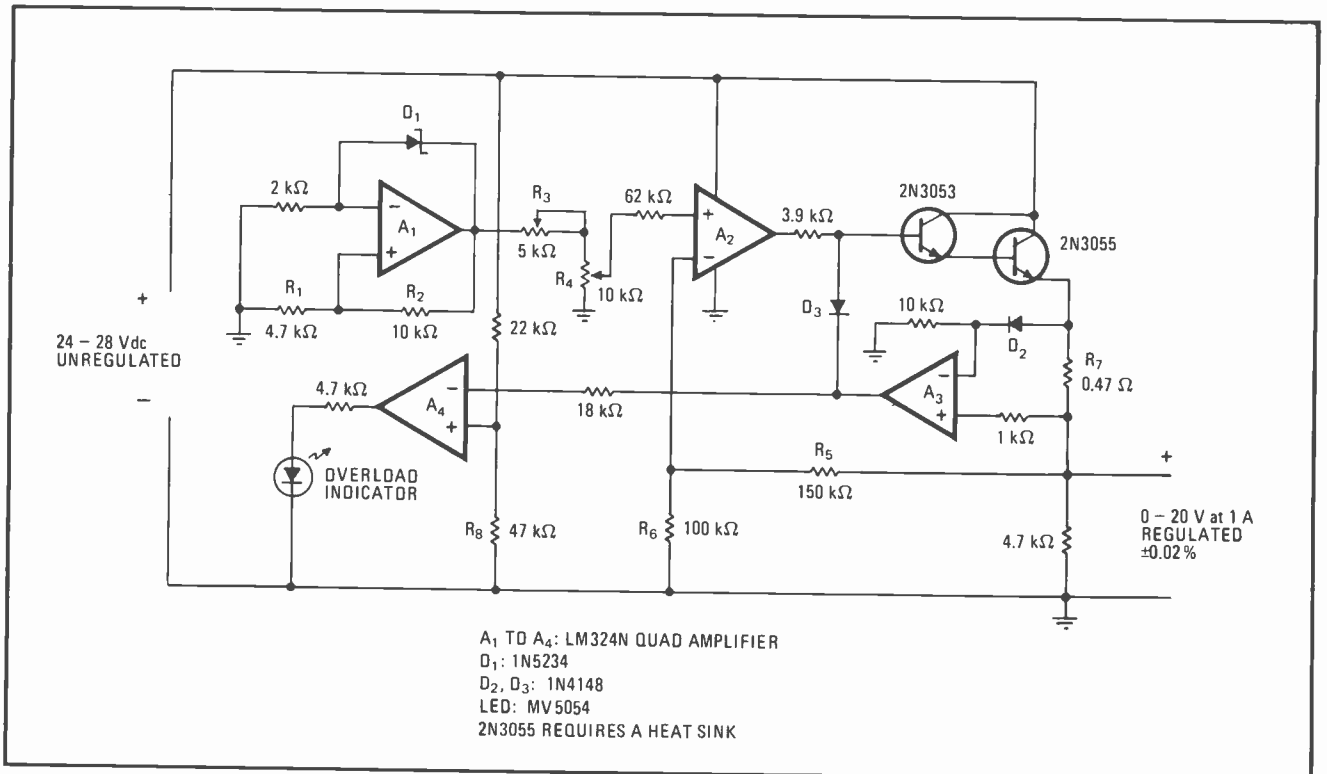
$$V_1 = V_z[1 + (R_1/R_2)]$$

It is approximately 9.1 V for the values shown in the diagram. The potentiometers R_3 and R_4 bring V_1 down to a desired value V_2, which is amplified by A_2 and the Darlington output stage to the output level:

$$V_{out} = V_2(R_5 + R_6)/R_6$$

With R_4 at its maximum-voltage position, variable resistor R_3 sets the voltage at exactly 20 V; thereafter, R_4 varies the output voltage over its full range. The output stage gain is 2.5 for the values shown.

Amplifier A_3 monitors the regulator's output current under varying loads. It compares the voltage across R_7 (a very small resistance) with the drop across diode D_2. Whenever the former is greater than the latter, the output of A_3 drops, biasing diode D_3 for-



Op amp regulator. An unregulated 26-volt source becomes a 1-ampere 0-to-20-V supply regulated to within ±0.02% by a simple quad operational amplifier. Input can vary between 24 V and 28 V, and quiescent current is less than 10 mA. A light-emitting diode gives an overload indication, the level of which depends on the value of resistor R_8. Single power Darlington can replace the two transistors.

ward; thus it reduces the output voltage by removing the drive to the Darlington stage. If the load continues to increase, the output of A_3 becomes low enough to indicate, through amplifier A_4, and a light-emitting diode, an overload condition. The circuit's overload threshold may be changed, if desired, by changing the value of resistor R_8.

The output transistors may be replaced by a single power Darlington, such as 2N6050, to reduce the package count from three to two. □

As clipper, IC comparator is improved by feedback

by Arthur D. Delagrange,
Naval Surface Weapons Center, Silver Spring, Md.

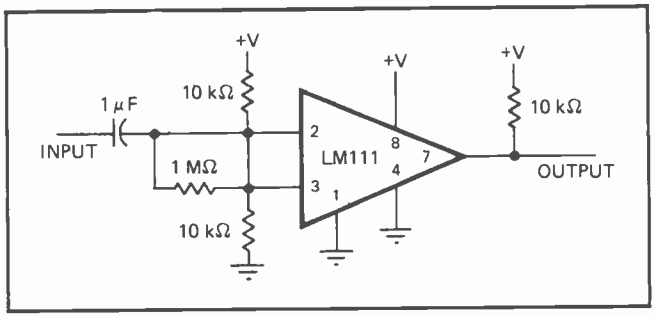
When used as clippers, modern integrated-circuit comparators are generally limited by input offset, not gain. To assure that the output will switch in a conventional circuit (Fig. 1), the peak input voltage must be greater than the differential current offset multiplied by the bias resistor value and added to the differential voltage offset.

A smaller peak input voltage can be used, however, if dc negative feedback is added to the negative input at pin 3, as shown in Fig. 2. The input offset is effectively reduced by the gain of the comparator as the circuit seeks its own bias point, just as operational-amplifier circuits do. The output is symmetrical, even for input levels near or below the comparator input offset.

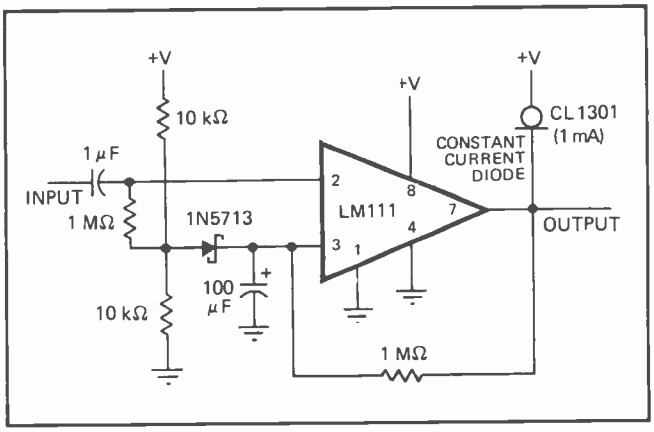
Substituting a current-limiting diode for the pullup resistor further improves output symmetry. The Schottky diode provides a charging path for the low-pass capacitor to minimize startup time. If startup time is not a problem, the Schottky diode may be replaced by an ordinary diode or eliminated altogether. To prevent the ac signal from feeding back and reducing sensitivity, the feedback RC time constant must be an order of magnitude longer than the signal period times the gain. A multiple-stage RC network cannot be used because it would introduce additional phase shift that might cause the circuit to oscillate.

As shown, the circuit does not work well with an unsymmetrical rectangular pulse-train input. For this special case, the voltage divider ratio must be the same as the input symmetry ratio. This technique can also be used to give an unsymmetrical output for a symmetrical input (except square wave) if desired.

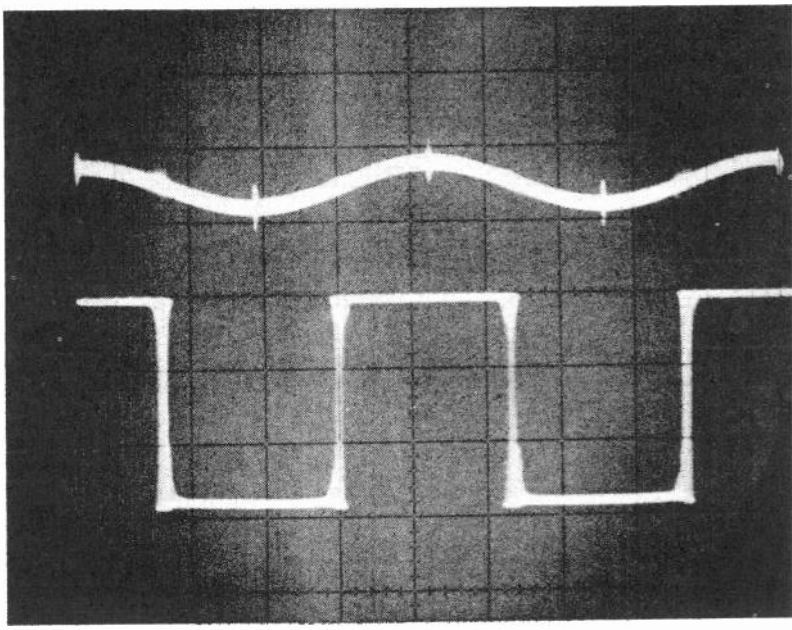
Input and output waveforms are shown in Fig. 3 for a sine wave input at a frequency of 1 kilohertz and an amplitude of 100 microvolts root-mean-square. Since the difference between input and output levels is about 90 dB, circuit arrangements that create parasitics must be carefully avoided. To obtain the waveforms of Fig. 3, a 50-ohm source was used, the output was loaded only by an oscilloscope, and power came from a well-regulated supply with a 1-microfarad ceramic bypass capacitor at the comparator. □



1. Conventional. Input offset limits the utility of the comparator when used as a clipper; it won't work with very small signals.



2. Improvement. Adding dc negative feedback reduces input offset, produces symmetrical output if input divider has 50:50 ratio.



3. Result. In this trace, the horizontal scale is 200 microseconds per division. Vertical scales are 500 microvolts per division for input (top), and 5 volts per division for output.

One-transistor regulator minimizes amplifier distortion

by Dale Hileman
Sphygmetrics Inc., Woodland Hills, Calif.

In a complementary-transistor power-amplifier stage, crossover distortion is usually difficult to control because the extremely critical bias point of the stage is hard to maintain. But when a single bipolar transistor is connected as a voltage regulator, the bias point can be controlled easily through a potentiometer that allows the biasing conditions to be set exactly.

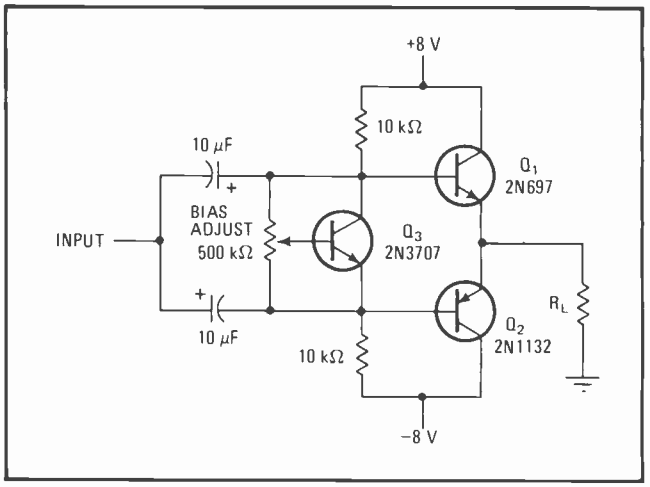
If the base bias current is too small, the stage exhibits severe crossover distortion. On the other hand, too much bias causes a needlessly high collector current; the transistors can be damaged, or their lifetimes considerably shortened. If the stage is powered by batteries (for example, in portable equipment), battery life will be shortened, too.

A resistive voltage divider is sometimes used to bias the complementary transistors, but this scheme can be entirely unsatisfactory unless the bias source is regulated. Additionally, such a divider does not provide compensation for the effects of temperature on the base-emitter junctions of the transistors.

To obtain better regulation and temperature compensation from the divider approach, a diode (or two) is often connected between the bases of the two transistors. This diode must be selected carefully, since it must produce the exact voltage drop needed. What's more, if this voltage drop changes as the equipment ages, the biasing will suffer accordingly.

The circuit shown in the diagram overcomes these problems. It employs a bipolar transistor as a simple voltage regulator and has a potentiometer that sets the stage's bias point precisely. Transistors Q_1 and Q_2 serve as the complementary power amplifier, with transistor Q_3 acting as the bias regulator.

The input to the stage is applied through the two coupling capacitors, and the collector-emitter voltage of transistor Q_3 is set by the potentiometer. The setup provides the optimum base bias for transistors Q_1 and Q_2. If the circuit's operating temperature varies, transistor Q_3 automatically adjusts the bias voltage to compensate transistors Q_1 and Q_2. □



Crossover-distortion regulator. Complementary transistors Q_1 and Q_2 form a power amplifier stage in which the bias point is controlled closely through transistor Q_3 acting as a voltage regulator. The bias-adjusting potentiometer permits exact setting of the stage's bias point so that crossover distortion is held to a minimum. The transistor regulator also automatically compensates for varying temperature.

Timer circuit generates precision power-on reset

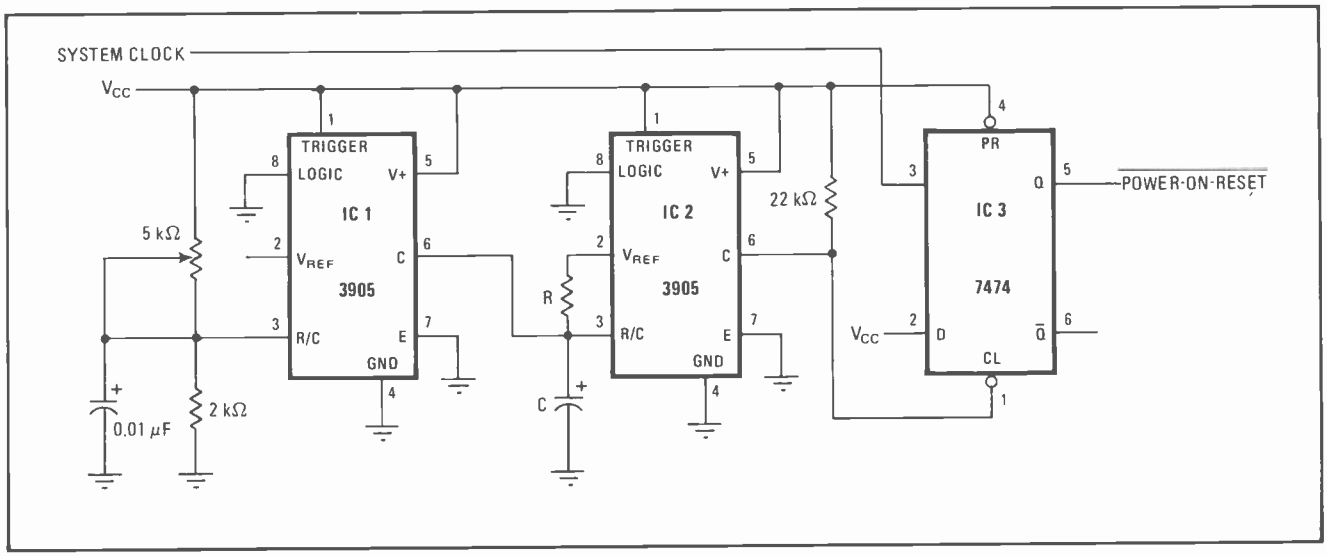
by Jim Felps
Texas Instruments Inc., Austin, Texas

Digital systems are commonly initialized with a power-on reset, generated automatically when the power switch is turned on, but at no other time. A typical circuit simply holds a reset line long enough for all the power transients to die out, then drops it. Its duration isn't well defined, and it doesn't respond to dips or glitches in the primary power line.

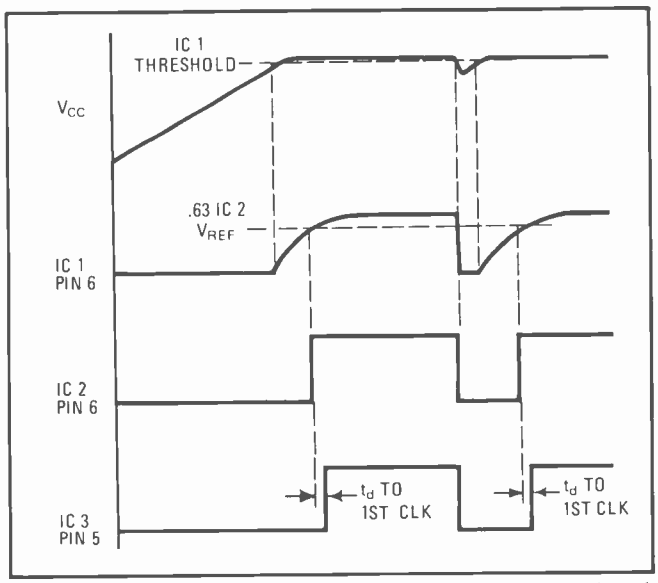
Until recently, a more precise power-on reset circuit would have been too complex and too costly to be justified. Now, however, new integrated circuits are available that contain voltage comparators and references that work at supply voltages as low as 4.5 volts. One such IC is the National Semiconductor LM 3905 N—a comparator, reference, and precision timer all in one eight-lead package.

In a power-on reset circuit based on the 3905 (Fig. 1), the timing begins only when the incoming V_{cc} has reached a suitable level, which can be very precisely established, and it is repeated if V_{cc} later drops even momentarily below that level. As a result, all logic circuits in the system are properly reset, even if the power reaches its nominal level only after an exceptionally long rise time, and no random logic failures can be caused by a power-line glitch.

IC 1 is a 3905 used as a comparator, which monitors the level of V_{cc} (nominally 5 volts for transistor-transistor logic). It keeps the reset on whenever V_{cc} is less than



1. Reset generator. One comparator, one timer and a flip-flop join forces to produce a precisely timed power-on reset.



2. Sequence. When V_{cc} reaches a threshold defined by the setting of the 5-kilohm potentiometer, IC 1 turns on. Its rise is delayed by the RC network on IC 2. After one time constant, the clear input to IC 3 is released, and the flip-flop is set by the next clock pulse.

4.75 V; its triggering level is established by setting V_{cc} at 4.75 and adjusting the 5-kilohm potentiometer at the point where the circuit's output (pin 5 of IC 3) just switches. Thereafter, when power is turned on and V_{cc} rises above this 4.75-V threshold (Fig. 2), IC 2, a 3905 used as a timer, is released. One time constant later, as determined by the RC network connected to pins 2 and 3 of IC 2, an ordinary 7474 D-type flip-flop, IC 3, is released. By this time the system clock should be running smoothly; at the next positive-going clock pulse the flip-flop is set, thus removing the power-on reset.

If the level of V_{cc} drops below 4.75 V at any time, both timers and the flip-flop immediately go down, generating another reset to the rest of the system. Restoration of V_{cc} initiates the power-on sequence again.

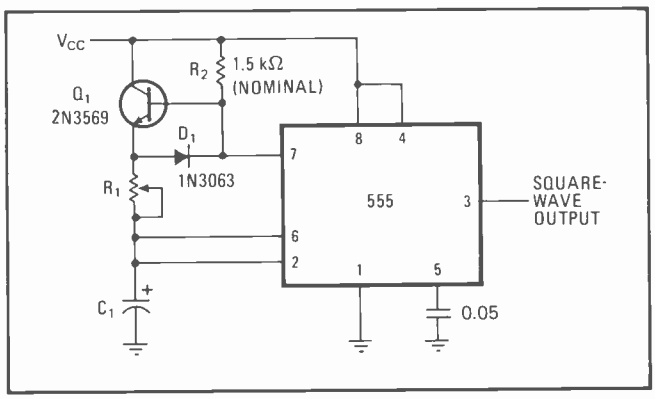
If less precise reset timing is necessary, IC 2 may be omitted. The output of IC 1 then rises as soon as the threshold has been passed, and the flip-flop is set by the next clock pulse. If several power supplies have to reach their nominal levels before the reset terminates, a separate 3095 as comparator can be connected to each supply and all the outputs (pin 6) connected to each other as a wired OR. □

Generator's duty cycle stays constant under load

by Arthur R. Klinger
School of Health Care Sciences, Sheppard AFB, Wichita Falls, Texas

In the 555 timer, configured as a square-wave generator, adding one transistor and a diode to the RC timing network permits the frequency to be varied over a wide range while maintaining a constant 50% duty cycle [see also *Electronics*, Sept. 19, p. 112].

In one simple configuration, a capacitor's charge and discharge currents flow through only one resistor. The



Workhorse. This configuration of the 555 timer can drive a heavy load without distorting its square-wave output, even over a very wide frequency range, unlike simpler hookups.

high and low periods should be equal at any frequency, but, with heavy loads, the output may be offset by 1 volt or more from V_{cc} or ground. This varies the potentials across the RC network, creating quite large changes in duty cycle or frequency. Noise on the output lines can also cause erratic changes in the periods.

The circuit shown in the diagram removes the timing network from the output. While the timer's output is high, Q_1 is biased into saturation by R_2, so that charging current passes through Q_1 and R_1 to C. When the output goes low, the discharge switch (pin 7) cuts off Q_1 and discharges the capacitor through R_1 and D_1. With the same impedance in both paths, the high and low periods of the square wave are equal.

Q_1 should have a high β value so that R_2 can be large and still drive the transistor into saturation. With R_2 large, the IC's discharge transistor, which can sink 20 to 30 milliamperes, gets most of that current from the discharging capacitor and very little through R_2. The voltage drops in Q_1, D_1, and the internal discharge switch decrease the effective voltage across R_1, causing the actual periods to be slightly longer than those given by the astable and bistable formulas in the data sheets—0.69RC and 1.1RC, respectively. A high-conductance germanium or Schottky diode for D_1 would minimize these diode-voltage drops in D_1 and Q_1.

For precise square waves, the on characteristic of Q_1 should be the same as that of D_1 and the IC's internal pull-down switch. To optimize this balance, set the timing network to its highest frequency range, and adjust R^2 while monitoring the square wave output. Once adjusted at this frequency, an excellent square wave is maintained for all combinations of R_1 and C_1.

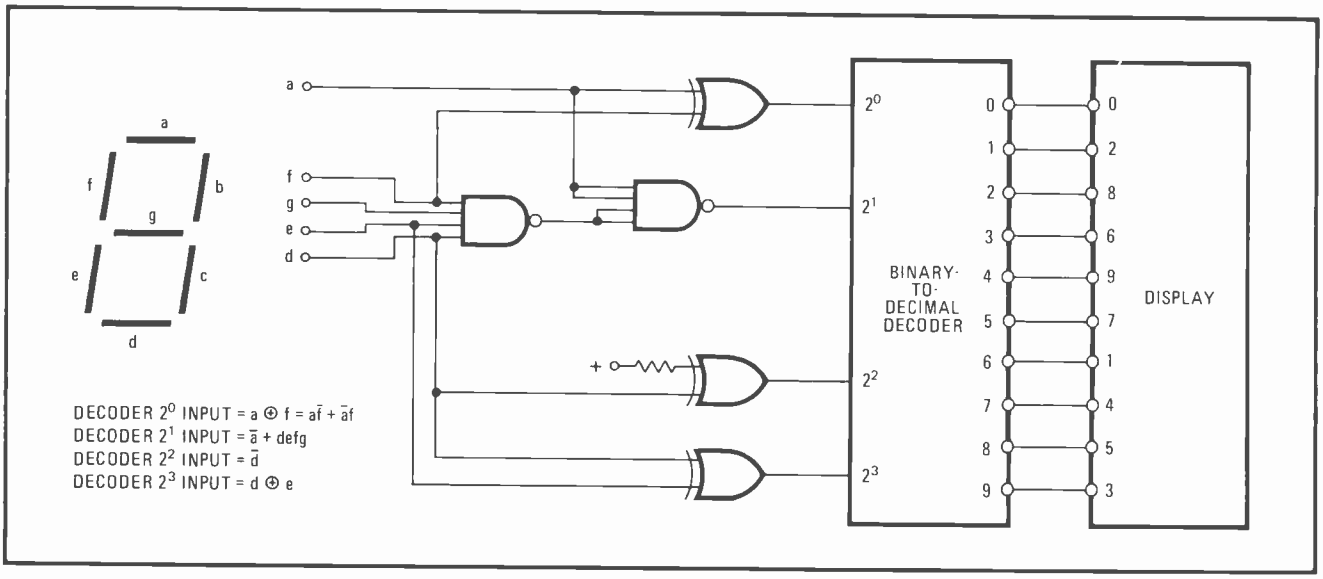
Since the usual current-limiting resistor is not needed, the minimum value of R_1 can be as little as a few hundred ohms. Such a small resistance carries large charge and discharge currents, leading to a frequency range twice as wide as the usual configuration provides. For example, if R_1 = 10 megohms, the frequency range can exceed 20,000 to 1 for a single choice of C. □

IC trio converts 7-segment code to decimal

by James Southway
McDonnell Douglas Astronautics Co., St. Louis, Mo.

A device that converts a seven-segment display code into decimal code and is less expensive than the demultiplexer described in a previous article [*Electronics*, Aug. 8, p. 105], uses only three integrated circuits. The only other requirement is front-end buffering, and only if its TTL circuitry is to be used with a MOS system. Like the demultiplexer, this device enables a seven-segment display code to directly drive any kind of cold-cathode gas discharge indicator tubes.

The small number of ICs is made possible, in part, by combining the logic of the binary-to-decimal decoder with a few external logic gates, and by cross-wiring the decoder outputs to the display inputs. In other words, output 1 of the decoder drives the display input for 2; output 4 drives the input 9, and so on. (The only uncrossed output is 0, as shown in the diagram.) The decoder is a 74141 or equivalent; the external logic is one dual four-input NAND, 7420, and one quad exclusive-OR, 7486. Another saving is made by using one of the four exclusive-OR gates in the 7486 as an inverter, and one of the two four-input NANDs in the 7420 as a two-input NAND. □



Converter. Seven-segment display code is converted into a 1-out-of-10 code for driving such things as indicator tubes, and uses only three integrated circuits. Decoder, external logic, and cross-wired outputs keep the IC count low.

Rectifying wide-range signals with precision, variable gain

by Jerald Graeme
Burr-Brown Research Corp., Tucson, Ariz

Millivolt-level signals cannot be rectified directly because they are smaller than the typical 0.7-volt drop across a forward-biased diode. An operational amplifier can reduce this loss to around 10 microvolts. But such circuits have a fixed gain when designed straightforwardly, whereas variable gain is needed for range control in many applications—amplitude detection in ac voltmeters, for example.

Varying the gain has usually required either the adjustment of more than one resistor or, in very complex circuits, the use of a separate input amplifier. With the precision rectifier shown in the diagram, however, variable gain is achieved without a gain-control amplifier.

Gain is controlled by a single variable resistor, which can be a potentiometer or a multiple-tap resistor. In addition, this circuit has a high input impedance without an input buffer and requires only one resistance match. It has a gain range from unity to several thousand, for signals from 1 millivolt to 10 V.

Rectification results when the feedback diodes are switched by a reversal of the signal polarity, which in turn reverses the circuit gain polarity. With the diodes in one orientation, the signal path to the output is a noninverting amplifier; when they switch, it becomes a voltage follower and an inverting amplifier.

An input of positive signals produces a positive current i_1 that turns diodes D_2 and D_3 on and D_1 and D_4 off. This connects the noninverting amplifier A_1 to the output with a gain of $1/x$, where x is a fraction representing the potentiometer setting. In this mode A_2 is merely a ground return for the resistance xR_1; its output is disconnected from the circuit output by the reverse-biased diode D_4. Thus the circuit output, controlled by A_1 alone, is $e_o = e_i/x$.

When the input signal swings negative, so does the current i_1. It switches off D_2 and D_3 and turns on D_1 and D_4. Now the output of A_2 is connected to the circuit output, and A_1 merely maintains a signal equal to e_i at its own inverting input. In doing so it also develops this signal across the resistance xR_1. That resistance acts as the input resistor to A_2, connected as an inverting amplifier. With a gain of $-1/x$, this inverting amplifier develops $e_o = -e_i/x$, the negative of that produced by positive signals. Since the polarity of the gain switches with that of the input signals, the output signal is always positive, and $e_o = |e_i/x|$.

Gain can be varied from unity to several thousand to accommodate a wide range of signal levels. To insure continually equal gain for positive and negative signals, it is only necessary to match the resistor R_2 to the total potentiometer resistance R_1. Op amp gain error directly affects circuit gain, but identically for both positive and negative signals.

Otherwise, circuit accuracy depends upon the noises, dc errors, and ac responses of the op amps. Noise isn't generally a major source of error in the practical signal range of 1 mV to 10 V, as long as the resistance levels are low enough to limit the effects of noise currents at the amplifier inputs.

Ideally, the diodes would switch just as the input signal crosses zero, but the op amps' dc offset voltages—the input levels below which the amplifiers produce no outputs, as a result of mismatched transistors in the amplifiers—cause the circuit to depart from this ideal. The error currents are:

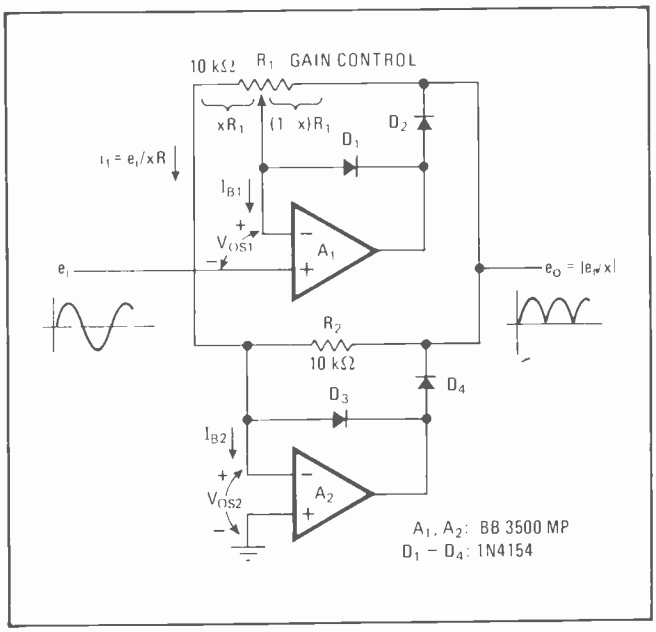
$$(V_{OS1} - V_{OS2})/xR_1 + I_{B1}$$

and

$$(V_{OS1} - V_{OS2})/xR_2 - I_{B2}$$

This switching-point offset limits the circuit's operation with very small signals. To extend it, the amplifiers are chosen for low bias currents, and the op-amp offset voltages are nulled. Matched op amps insure low initial dc errors and thermal drifts.

Another output offset is produced by input currents flowing through the feedback resistances. This offset cannot be removed by the op-amp null controls without again offsetting the diode switching, but it is minimized



Precision rectifier. Variable gain is achieved without a separate gain-control amplifier, since the control potentiometer varies the gains of both amplifiers identically. Circuit gain ranges from unity to several thousand. Forward or reverse biasing of diodes make the circuit either an inverting or noninverting amplifier.

by the choice of suitable op amps and resistances.

High-frequency performance is limited by the speed with which the op-amp outputs can turn off one rectifying diode and turn on the other. While the first diode is being turned off, the signal with the wrong polarity passes, and while the second diode is turning on, no signal passes. Ideally, this transition should be instantaneous, but in practice it always takes a finite time, limited by the operational amplifiers' slewing rates and their bandwidths, which are expressed by the speed with which the amplifiers can swing their outputs through two diode voltage drops, $2V_f$.

If the input signal is small, the rate of change of the amplifier output voltages equals the rate of change of the input signal multiplied by the open-loop gain of the amplifier at the signal frequency, $A(f_i)$, and therefore the transition time is the time required for the input signal to change by $2V_f/A(f_i)$. For larger signals the rate of change of the amplifier output voltage can be no more than its slewing rate limit S_r, so that the transition time is $2V_f/S_r$. These considerations limit the usable bandwidth of the precision rectifier to about 1 kilohertz. □

Power-failure detector is good for short lapses

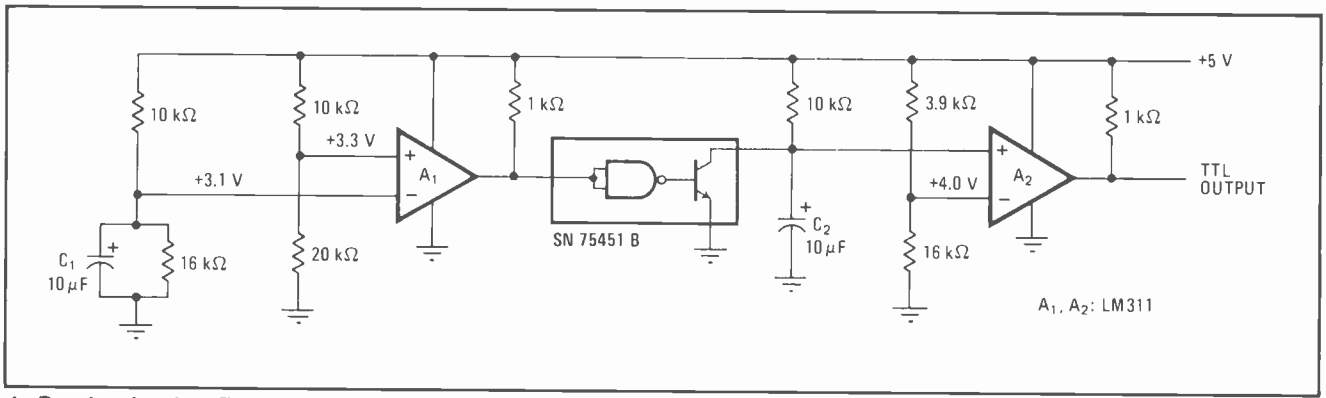
by K.C. Seino,
Fermi National Accelerator Laboratory, Batavia, Ill.

A power-failure-detection circuit for a digital system should be reliable for any interruption, whether it lasts for milliseconds or hours. It should also produce reset and restart timing pulses. The conventional power-clear circuit, which consists of a gate with an RC delaying network at its input, works well for power failures of long duration, but not after a momentary failure. Nevertheless, the system must still be reset and checked before it is restarted.

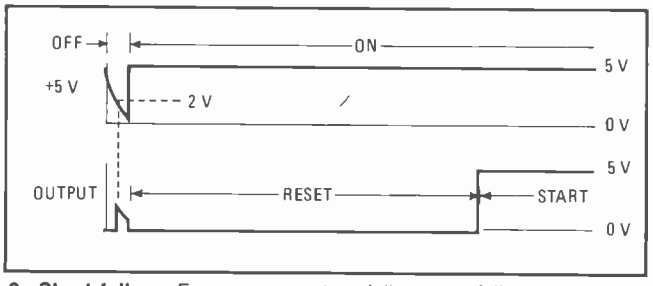
Two voltage comparators and an open-collector gate can be the basis of such a circuit as shown in Fig. 1. The diagram shows the LM 311, which can be operated with only a +5-volt power supply, and the peripheral driver SN 75451 B, useful because of its small physical size. But any comparator or open-collector gate with the proper specifications can be used.

When power is present, the (+) input of comparator A_1 stays higher than the (-) side, and the output is high. The NAND gate inverts the level, cutting off the transistor. As soon as power starts to go down, the (+) input, nominally at 3.3 V, quickly drops below the 3.1-V level on the (-) input, which is maintained briefly by capacitor C_1. This reversal of the input levels causes the output of A_1 to become low; capacitor C_2, which is normally fully charged, discharges through the transistor, which turns on when the output of A_1 drops.

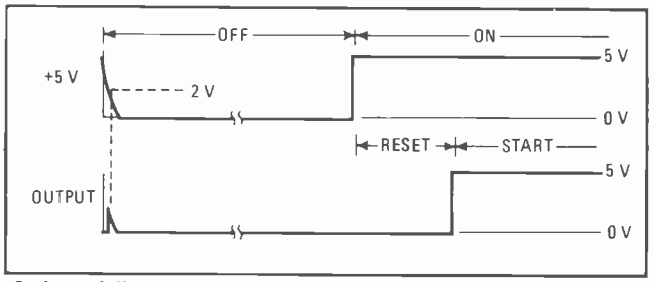
While the power-supply voltage is less than about 2 V, the output of both amplifiers simply follows whatever may be available on the supply line. But when full



1. Reset and restart. Two voltage comparators and a gate can reset a digital system and restart it after any power interruption, be it a glitch or a complete blackout. Wide variety of ICs can be used. Key components are the RC network at the input of A_2.



2. Short failure. Even a momentary failure that falls below 2 volts can cause problems. Reset begins the moment power is restored; start pulse is generated after restored power recharges capacitor.



3. Long failure. In the event of a total power failure, the output stays down after power is restored, again until capacitor has been recharged. Duration of reset depends on RC time constant.

power is restored, the capacitor C_2 begins to recharge. This takes time—the recharge path is through the 10-kilohm resistor, and the time constant is 100 milliseconds. The output of A_2 stays low until the capacitor voltage reaches 4.0 v, as shown in Figs. 2 and 3. This condition can be used as a reset pulse, and the transition to the high level when the capacitor voltage passes 4 v can generate a start pulse.

For a longer or shorter reset time, the 10-kilohm and 10-microfarad values can be changed. □

Complementary lighting control uses few parts

by Mark E. Anglin
Novar Electronics Corp., Barberton, Ohio

A very useful tool for stage lighting, light shows, or even home movies is a complementary lighting-control unit that will fade out one lamp while simultaneously increasing the light output of another. The usual design for such a control unit is rather complicated, relying on dual potentiometers, two fader circuits, and two of everything else. But the circuit in the diagram can perform this function with a minimum of parts, and the two loads track each other accurately without adjustments.

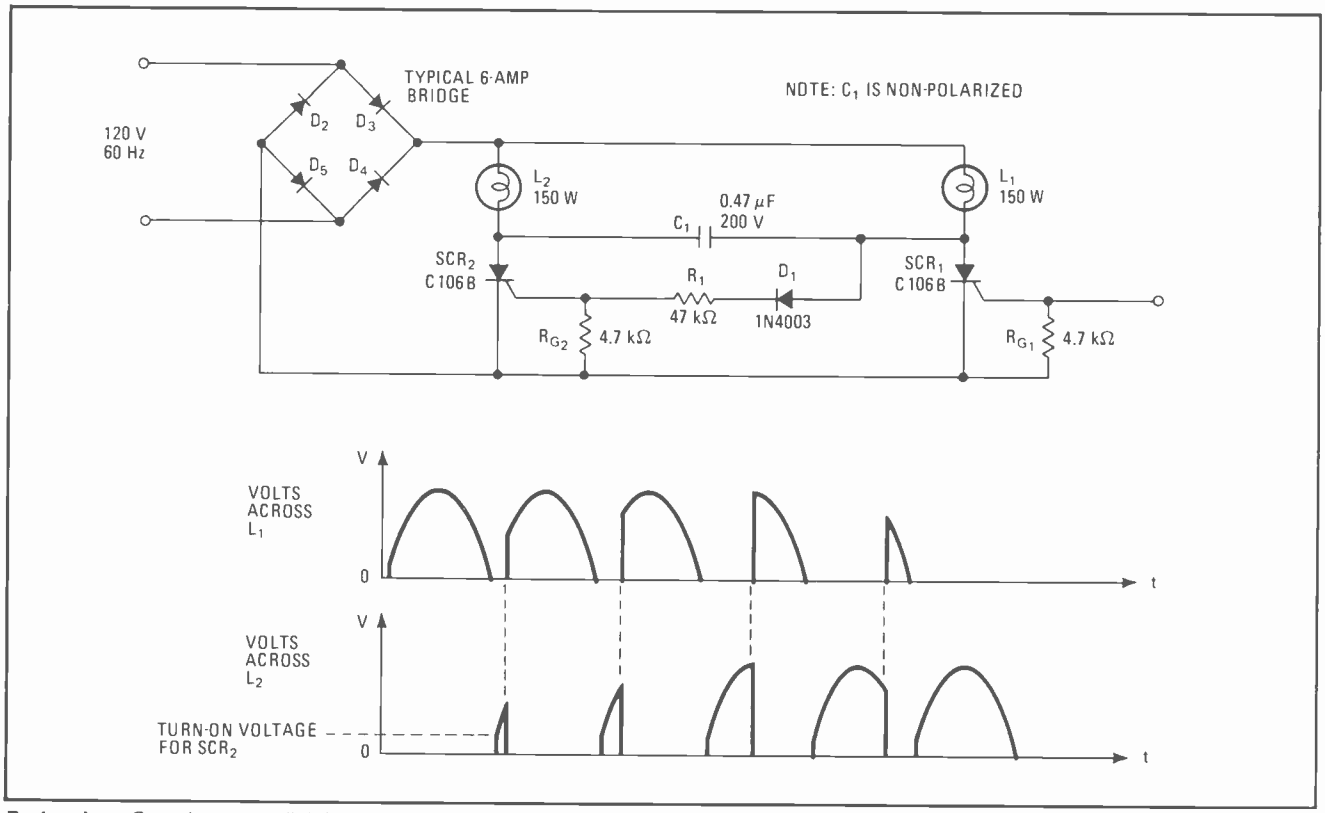
The gate of SCR_1, a silicon-controlled rectifier, is driven from a standard phase-control circuit, based, for example, on a unijunction transistor or a diac. It controls the brightness of lamp L_1 directly. Whenever SCR_1 is not on, a small current flows hrough L_1, D_1 and R_1, permitting SCR_2 to fire. When SCR_1 turns on, current flow ceases through D_1 and R_1; the energy stored in C_1 produces a negative spike that turns SCR_2 off.

In this circuit, the peak current through the diode bridge never exceeds the peak current through either SCR, because the two SCRs can never be conducting at the same time. This is an advantage over the conventional circuit, in which each SCR would be fired at a 45° phase angle to produce half brilliance from the lamps. This represents the worst case of simultaneous conduction and draws a peak current from the bridge that is twice the magnitude of the current of a single 150-watt lamp.

If this control circuit is to be used with lamps rated at more than 150 watts, the value of C_1 should be increased. The value of C_1, in microfarads, equals or exceeds:

$$(1.5\ t_{off}I)/E$$

where t_{off} is the turn-off time of the SCR in microseconds, I is the maximum load current, and E is the voltage at this maximum load current. □



Parts miser. Complementary lighting control fades one lamp out while bringing up the other one, with fewer parts than conventional controls use. Waveforms are segments of successive half-cycles of a full-rectified sine wave as control signal varies.

Low-speed counter uses low-priced calculator chip

by Dennis J. Flora
Stevens Institute of Technology, Hoboken, N. J.

A totalizing counter that runs at less than 40 hertz makes novel use of an inexpensive calculator IC, one of several now available. The IC in the illustrated counter is the MM 5736, a six-digit calculator chip that can directly drive the segments of small common-cathode light-emitting-diode displays. Because of this capability, the single IC replaces many discrete counter and decoder ICs; only a few extra logic chips are required.

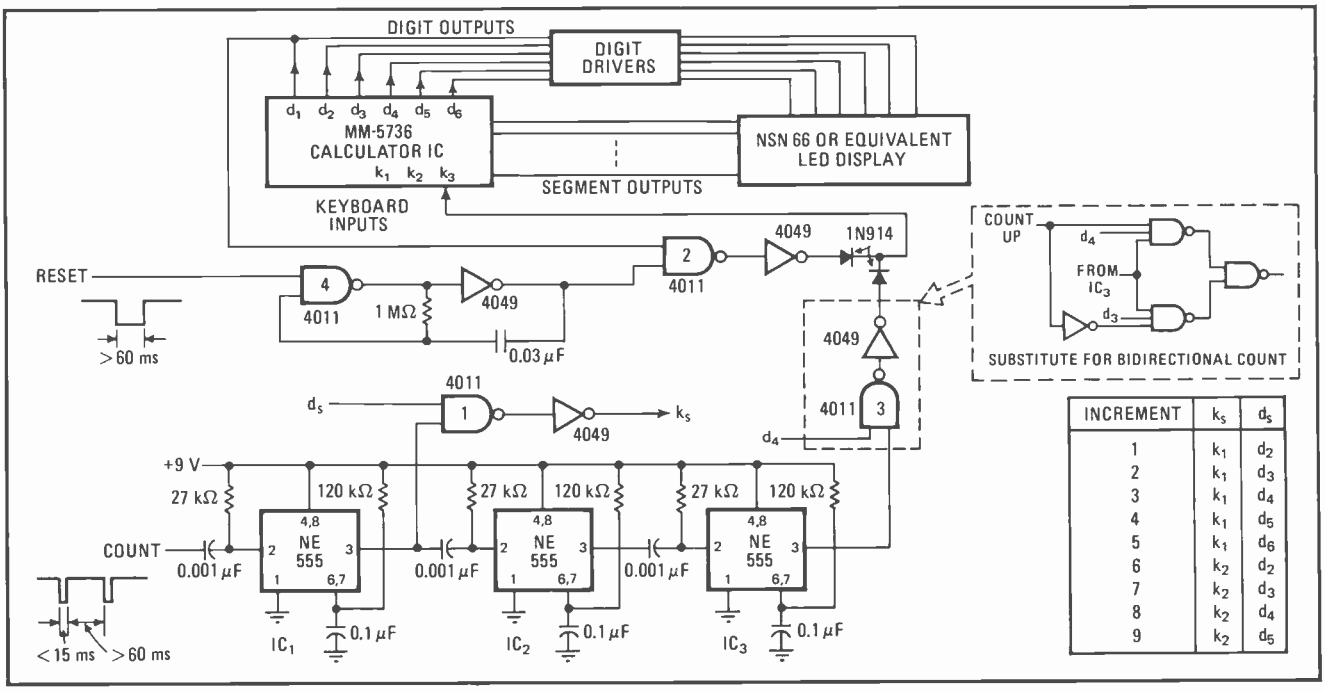
The MM 5736 has seven segment outputs, six digit outputs, and three keyboard inputs. In normal usage, the segment outputs drive the individual segments of all digits in a conventional display. The digit outputs drive the digits of the display, scanning rapidly from one to the next in synchronism with the segment outputs so that individual numerals are illuminated. These digit outputs also scan the keyboard. If any key is depressed, a connection is made from one digit output to one of the three keyboard inputs, uniquely identifying that key. The logic circuits in the chip respond to that input to display a digit or to begin an arithmetic operation.

The logic that is added in lieu of a keyboard includes three 555 timers, four two-input NAND gates, four inverters, and a few discrete components. The calculator chip and this logic together count events as signaled by an external count pulse, incrementing the display by 1, 2, or any integer up to 9.

The negative-going leading edge of each count pulse triggers a 555 timer connected as a monostable multivibrator, generating a pulse about 15 milliseconds long. This is long enough for the six digit outputs of the chip to complete many full scans, connecting what looks to the calculator like a key depression to one of the keyboard inputs. (In normal operation, a key depression is usually much longer than 15 ms because of human reaction time, and the corresponding digit entry is made in the calculator chip many times.) The "key" in this case is a hard-wired connection from one of the digit outputs to a NAND gate-inverter combination, and another is a hard-wired connection from the inverter to one of the keyboard inputs, in accordance with the table. By this means, the counting increment is entered into the calculator.

The end of the 15-ms pulse triggers a second timer that forces a delay during which the calculator can become stable after receiving the "key depression." (In normal operation, this delay is created as the user moves a finger from one key to another.) At the end of this delay, the third timer is triggered to produce a pulse that gates the digit output d_4 into the keyboard input k_3 to enter what the calculator sees as an instruction to add. Thus, for every incoming count pulse, the calculator chip adds the wired-in increment to the previous total and displays the result.

Normally, to clear this calculator, the clear button on the keyboard is pressed twice. To provide time to clear



Calculator counter. Logic blocks take the place of a keyboard to provide appropriate signals for the single-chip calculator, MM 5736, to serve as a simple counter. It costs less than the collection of discrete devices that otherwise would be required.

the counter, the reset pulse must be held low for at least 60 ms. During that time, an astable multivibrator assembled from another NAND gate, an inverter, a resistor, and a capacitor, provides at least two connections of digit output d_1 to keyboard input k_3. Since this is the same input used by the "add" pseudo-instruction, two diodes create the equivalent of an OR gate in front of k_3.

The counter can be expanded to count either up or down by removing the inverter following NAND gate 3 and inserting, before the gate, two three-input NANDs, as shown in the inset of the diagram. This connects either d_4 to k_3 to count up, as in the main diagram, or d_3 to k_3 to count down, controlled by a single additional logic input that specifies the direction of counting. This input has to be inverted to provide the proper level at both the three-input gates; the removed inverter can be used for this function.

The whole counter can be built for $15 to $20, an economical substitute for the six discrete counters and six decoder/drivers that would otherwise be required. □

Modified window comparator compensates for temperature

By C. E. Musser
General Electric Co., Binghamton, N.Y.

A window comparator circuit, which detects signal voltages at two different levels by comparing them to fixed references, can be modified to compensate for temperature variations that otherwise can affect the trip points that define the window.

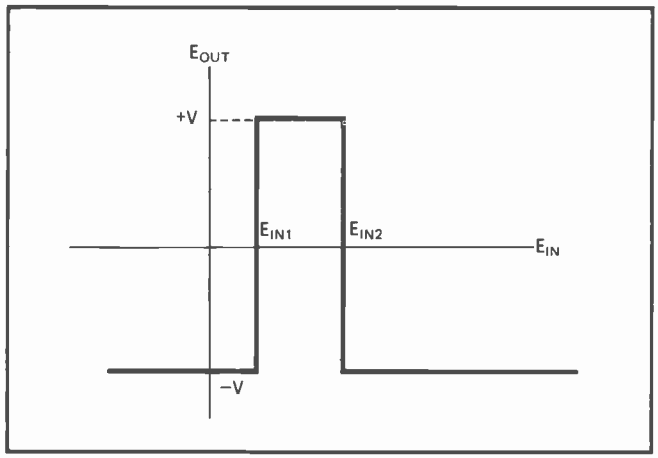
In the circuit's simplest configuration (Fig. 1), two voltage-reference dividers are connected to the inputs of an operational amplifier. Both dividers have the same excitation polarity, but the non-inverting input reference must be more positive than the inverting. Choosing the fractional resistance values establishes this inequality and defines the window's width.

An input signal is applied between diodes D_1 and D_2 from a low-impedance source, such as another op amp. For all signals that are at least one diode voltage drop more negative than the inverting input reference, diode D_2 is back-biased and not conducting, and the op amp is in negative saturation.

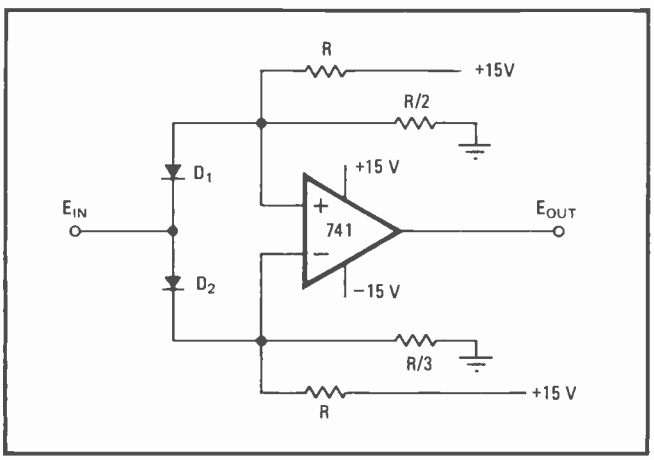
When the input signal is more than one diode drop more positive than the junction of the voltage divider at the inverting input, diode D_1 turns off and D_2 turns on. When the non-inverting op amp input becomes slightly more positive than the inverting input, the amplifier switches to positive saturation. In Fig. 2 this level is called E_{in1}.

A still larger positive excursion of the signal, to E_{in2} in Fig. 2, pulls the inverting input above the non-inverting one, making the op amp switch back again to negative saturation.

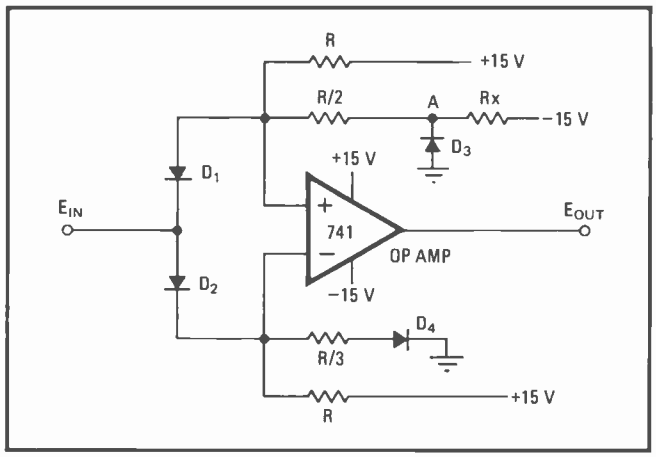
The two voltage references can be made negative by reversing the polarity of the excitation voltages and the input diodes. Doing this also reverses output polarity—it effectively turns Fig. 2 upside down. The reference volt-



2. Switching points. Op amp output is positive whenever input lies between E_{in1} and E_{in2}, negative for other levels.



1. Plain window. Operational amplifier, otherwise in positive saturation, is in negative saturation whenever input signal is more than 0.6 volt below negative reference or above positive reference.



3. Modified window. Because temperature changes can vary diode characteristics and change trip points, extra diodes in dividers vary in the same way and minimize the extent of the change.

ages for this circuit are

$$E_{in1} = V[(R/3)/(R+R/3)] - V_d = (V/4) - V_d$$
$$E_{in2} = V[(R/2)/(R+R/2)] + V_d = (V/3) + V_d$$

where V_d is the diode voltage drop.

Temperature changes cause diode variation that affect the trip points. Additional diodes in the dividers (Fig. 3) vary in the same way as the input diodes, and thus partially compensate for such changes. The resistor R_x should be chosen so that point A is slightly negative, just enough to bias the diode into continuous conduction. For the modified circuit the reference voltages are

$$E_{in1} = \eta[(V - V_d)(R/3)/(R + R/3)] + V_d\theta - V_d$$
$$= (V - V_d)/4$$
$$E_{in2} = \eta[(V + V_d)(R/2)/(R + R/2)] - V_d\theta + V_d$$
$$= (V + V_d)/3$$

Both of these circuit versions have been tested at room temperature using ±1% metal-film resistors, 1N4148 diodes, and 741 op amps. Assuming V_d to be 0.6 volts, the measured trip points agreed well with the calculated values. □

Timer pulse widths range from seconds to hours

by Ken Erickson
Interstate Electronics Corp., Anaheim, Calif.

A timer with output durations ranging from a few seconds to more than 100 hours can be built around a plating cell, thus avoiding the special low-leakage components or high resistances that such timers often require.

When the current direction in a plating cell is from reservoir electrode to working electrode, silver is plated onto the working electrode in an amount proportional to the charge passed through the cell. Conversely, when the current direction is from working electrode to reservoir electrode, silver is removed from the working electrode. As long as the electrode is plated, the impedance of the cell is only a few kilohms; but after all the plating is removed from the anode, the impedance across the cell increases to several megohms. When this happens, transistor Q_1 is turned on; otherwise, when the cell is plated, Q_1 is cut off.

The plating charge is the charge on capacitor C. When the input and output have both been low for a long time, C has charged fully to about 3.6 volts, and at 1,000 microfarads as shown, it holds 3.6×10^{-3} coulomb. Then, when the external input to gate G_1 goes high, its output drops to ground, and C discharges through the plating cell. The current, I_d, with the reference shown, is negative, causing the cell to be plated. The current's magnitude is limited by resistor R_1; the time constant for the values shown is about 1 second. Plating the cell drops the voltage at the base of Q_1 below its threshold, thus turning Q_1 off and Q_2 on. The collector of Q_2 drops almost to ground; this level is inverted by gate G_2, and the output goes high. This output feeds back to gate G_1 to make the circuit's operation independent of the input line once the timing cycle has begun.

The deplating current flows continuously through R_2; it is 1 microampere for the value of R_2 shown. When deplating is nearly completed, the cell's impedance begins increasing gradually, Q_1 turns back on, the timer output goes low, and if the timer input is low, capacitor C charges again.

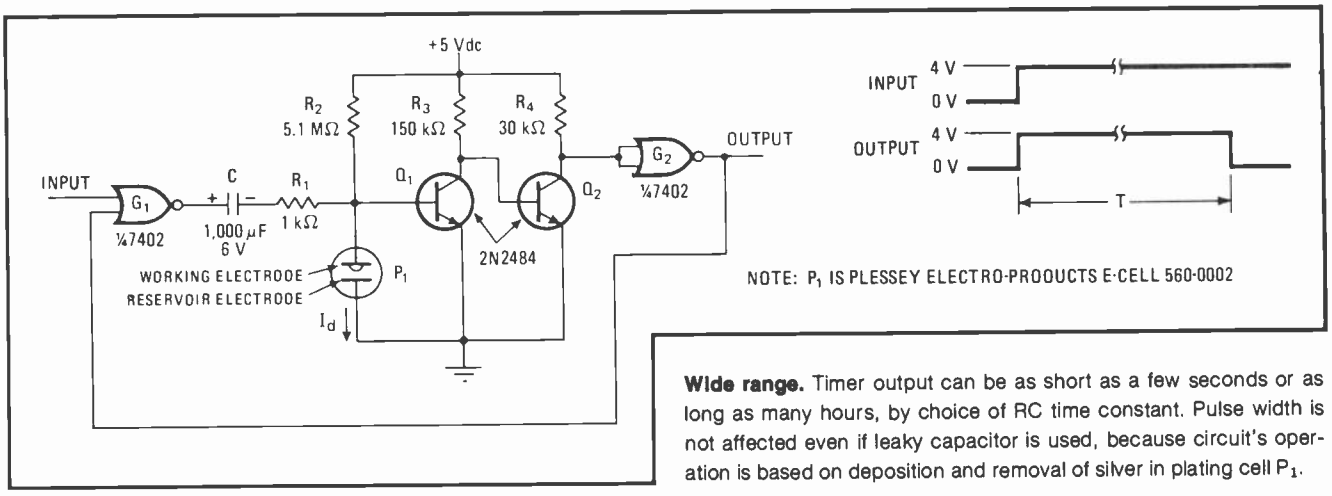
The charge transferred during either plating or deplating is represented by

$$Q = CV = I_d T$$

From this relationship, the time to transfer this charge is

$$T = CV/I_d$$

For a 1,000-microfarad capacitor, the time to deplate the cell is 3,600 seconds—a full hour. Other times can be obtained by using different values for the capacitor C or the resistor R_2. □



Wide range. Timer output can be as short as a few seconds or as long as many hours, by choice of RC time constant. Pulse width is not affected even if leaky capacitor is used, because circuit's operation is based on deposition and removal of silver in plating cell P_1.

Negative feedback keeps LED intensity constant

by Ken Erickson
Interstate Electronics Corp., Anaheim, Calif.

In applications where a passing object is detected as it partly obscures a light beam, a light source with a constant intensity may be desirable. A light-emitting diode, which has a longer life and switches faster than an incandescent lamp, would also be desirable, if it weren't for the fact that its light intensity may vary with temperature, especially as the device ages. But a LED's light intensity can be kept constant by the circuit shown here.

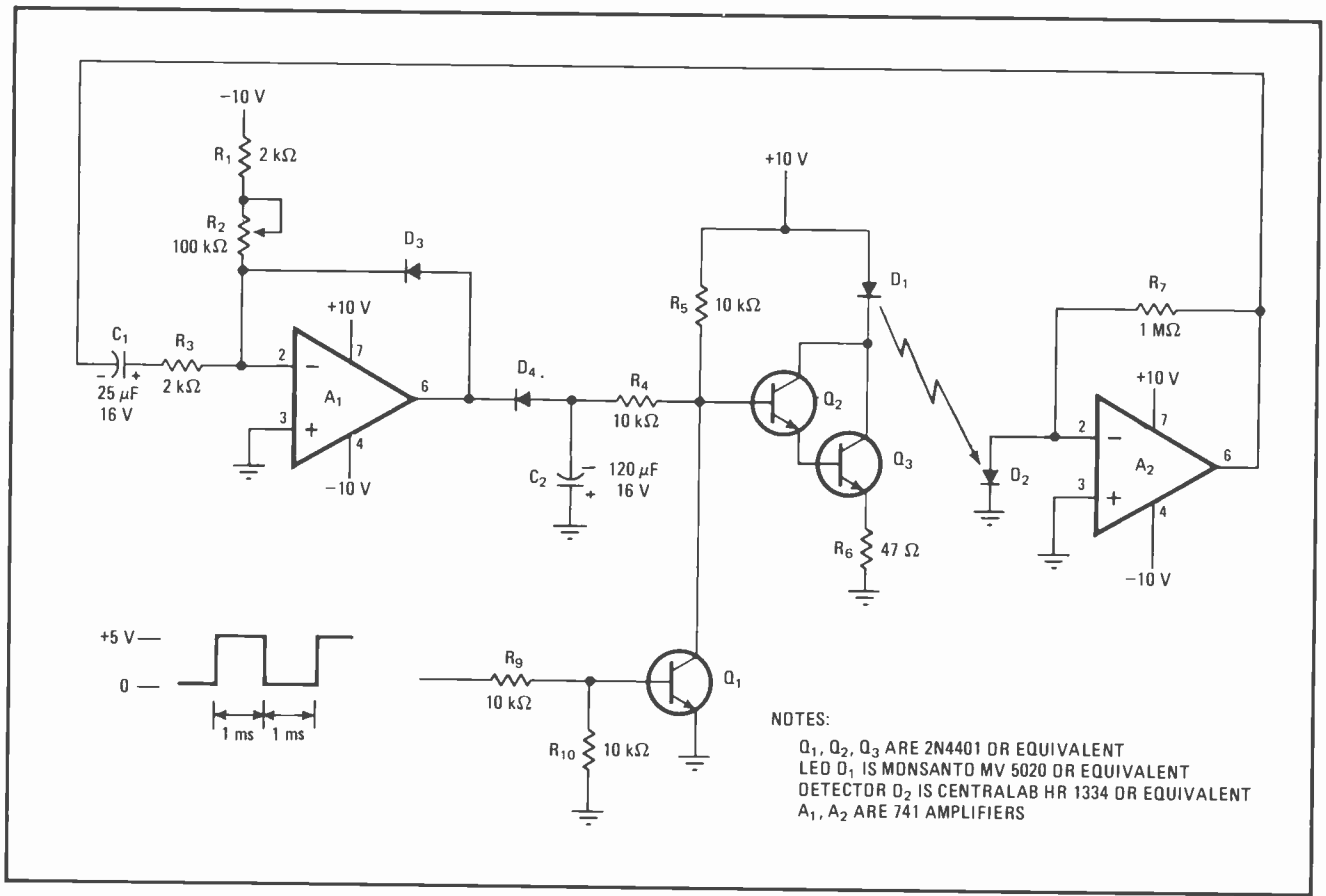
Light intensity is regulated by a silicon planar photovoltaic diode, D_2, the ac response of which is almost constant with temperature or time. Its current is converted to voltage by amplifier A_2 and resistor R_7. This diode is connected in a short-circuit mode to minimize its dark current.

D_1, a light-emitting diode, is driven by Darlington-connected transistors Q_2 and Q_3; its current is proportional to the voltage at the base of Q_2. Transistor Q_1, which is driven by a positive-going square wave, chops the dc level at the base of Q_2 so that it operates in an ac mode.

When the capacitively coupled output of amplifier A_2 is positive, amplifier A_1 charges capacitor C_2, when necessary, to maintain the current through R_3 equal to the current through R_1 and R_2. Because the current through R_1 and R_2 is constant, the amplitude of the square-wave signal at the junction of C_1 and R_3 is held constant.

When the output of A_2 is negative, the capacitively-coupled output of amplifier A_1 goes positive, but is clamped to 0.7 volt by diode D_3. This clamping maintains the output of the amplifier in the active region so that a virtual ground potential is maintained at its summing point. The light intensity level is adjusted by potentiometer R_2. The peak-to-peak voltage at the output of amplifier A_2 is held at $40/(R_1 + R_2)$ volts, where R_1 and R_2 are in kilohms.

Diode D_2 can be mounted near the LED, but to one side of the direct beam, so that it picks up enough light to generate the feedback signal but doesn't interfere with the primary detection function. □



Steady glow. Feedback loop senses variations in output of light-emitting diode, which may occur as temperature changes. Photodiode response is almost constant with temperature; it is amplified, and signal controls another amplifier whose output controls LED drive circuit.

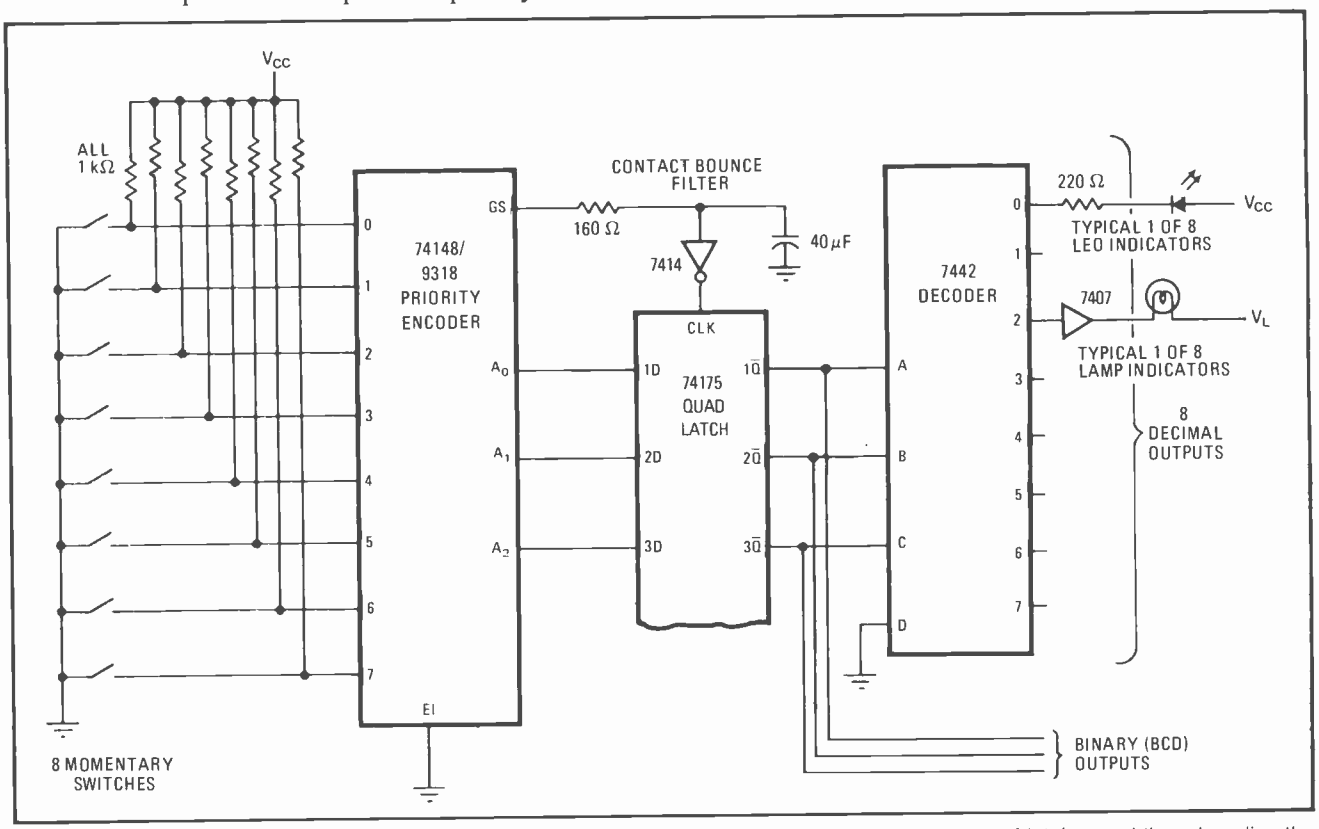
Latch circuits interlock remote switches electrically

by Jack Elias
Honeywell Inc., Fort Washington, Pa.

As many as eight momentary switches can be interlocked electrically even when they are physically separated from one another—an impossible task for mechanical interlocks. The keyboard-type momentary switches provide both binary-coded and individual outputs and are much more reliable than mechanically interlocked switches. The electrical interlock consists of an encoder, decoder and quad switch latch plus a Schmitt trigger and a few passive components.

The switches provide the inputs to a priority encoder, such as a TI 74148 or Fairchild 9318, which translates the identity of any actuated switch into a binary-coded output. The encoder also has an output, termed GS, for group-select, indicating when any one or more inputs are actuated; it provides a clock pulse for a 74175 quad latch, which stores the binary-coded output of the encoder. An RC filter and a Schmitt trigger remove uncertainty caused by switch bounce. The outputs of the flip-flops go to a 7442 decoder, which can drive either light-emitting diodes directly or incandescent lamps through buffers. Of course, the outputs can drive other circuits or systems that require the interlock.

If a second switch is actuated before the first is released, it has no effect because the Schmitt trigger has already generated its clock. Likewise, if the first switch is released while holding the second one down, the first switch's indication will be held until all the switches are released. The circuit can be expanded by cascading the encoders and using a larger decoder. □



Interlock. Momentary switches are interlocked from simultaneous operation by encoding them into a set of latches and then decoding the latch states to drive indicators or other apparatus. Circuit is more reliable than mechanical interlock, and switches can even be remote.

Common silicon diodes stabilize oscillator

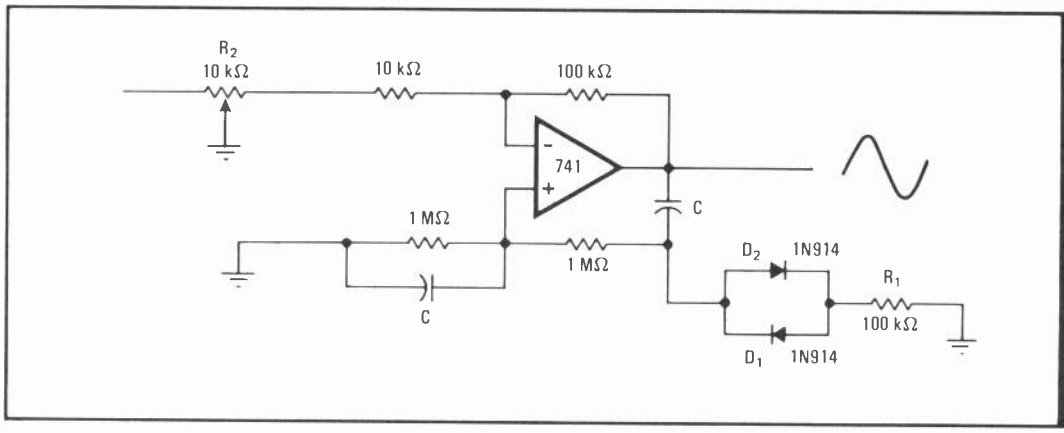
by Dale Hileman
Sphygmetrics Inc , Woodland Hills, Calif.

Two ordinary silicon diodes connected front-to-back in the feedback path of a Wien-bridge oscillator stabilize the feedback without introducing hunting or distortion. Stabilization makes them superior to the more commonly used thermistors or incandescent lamps, which have thermal inertia that introduces hunting when power is turned on or the frequency is changed, and to zener diodes, which distort the waveform.

The front-to-back connection of the silicon diodes simulates a back-to-back series connection of zener diodes, which might otherwise be used at this point in the circuit. Resistor R_1 is added to soften the effect of the knee of the forward-conduction characteristic, which would otherwise introduce distortion.

The best way to change the frequency of this circuit is to change the two capacitors, which must be closely matched. By this means, the output amplitude is always the same, regardless of the frequency. With the circuit values shown, amplitude is constant within ±0.3 dB over range of 100,000 to 1.

The setting of potentiometer R_2 establishes the amplitude, but it also affects the frequency somewhat. □



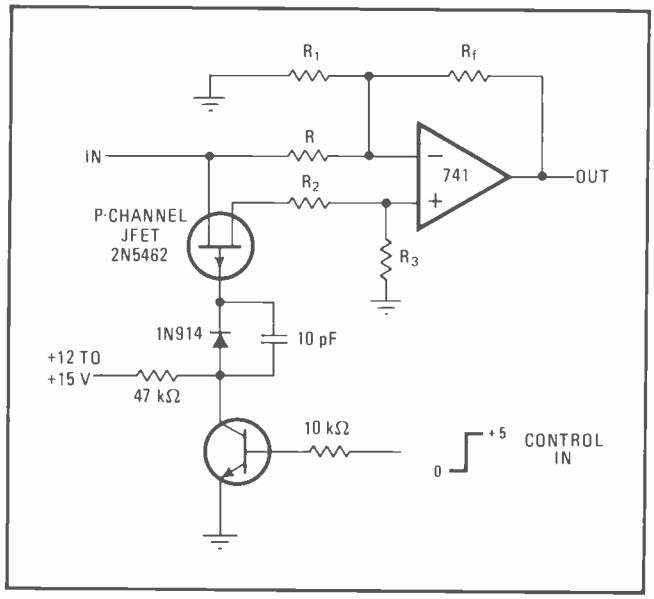
C	f
100 pF	5 kHz
1000 pF	500 Hz
0.01 μF	50 Hz
0.1 μF	5 Hz
1 μF	0.5 Hz
10 μF	0.05 Hz

Stabilizer. Front-to-back diodes in oscillator's feedback path acts as stabilizer, yet do not cause hunting or distortion, as lamps or zeners sometimes do. Capacitors, which control frequency, are matched; amplitude control is by potentiometer, which also affects frequency.

FET programs op amp for invertible gain

by Ken A. Dill and Mark Troll
Revelle College, University of California, La Jolla, Calif.

With only a few inexpensive components, an amplifier can be built with a gain of either +N or -N, depending on whether a field-effect transistor is turned off or on. Such a circuit is useful for programable inversion of analog signals or for programable phase-shifting of 180°



FET inverts op amp. Amplifier gain can be programmed either positive or negative, depending on whether the field-effect transistor is conducting or not conducting. Gain is the ratio of R_f to R; for gains of ±1, R_f, R_2, and R_3 are all equal value, and R_1 is half the value.

for signals that are symmetrical with respect to ground. When a comparator is added to program the inverter, the circuit becomes a precision rectifier, the output of which is:

$$V_{out} = |V_{in} - V_{ref}|$$

When the FET is off, the input signal goes only to the inverting input terminal of the operational amplifier; the gain is:

$$V_{out}/V_{in} = -R_f/R$$

But when the FET is on, the gain is:

$$V_{out}/V_{in} = \eta A/[1+(ARR_1)/(R_1R_f+RR_f+RR_1)]\theta \times [f-)R_1R_f)/(R_1R_f+RR_f+RR_1)]$$

where A is the open-loop gain of the op amp, and

$$f = R_3/(R_2+R_3)$$

Since A is large, this reduces to:

$$V_{out}/V_{in} = (f-1)(R_f/R) + f[(R_f/R_1)+1]$$

To make +N and -N numerically equal, choose the resistance values so that $R_f/R = N$. From that, it follows algebraically that:

$$N = (f-1)(N) + f[(NR/R_1)+1]$$
$$2N = fN + (fNR/R_1) + f$$
$$2NR_1 = fNR_1 + fNR + fR_1$$
$$2NR_1 - fNR_1 - fR_1 = fNR$$
$$R_1 = NRf/[2N-(N+1)f]$$

For the simplest case—a gain of ±1—all amplifier input and feedback resistors have the same value, except R_1, which is half that value.

The gate of the FET is controlled by a standard analog switch configuration, which allows the inputs to be 0 or +5 volts, compatible with TTL. □

Digital-to-analog converter controls active filter

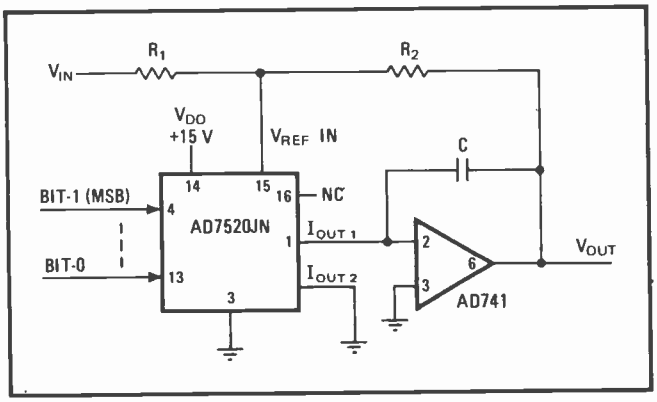
by Jerry Whitmore
Analog Devices, Santa Clara, Calif.

A monolithic digital-to-analog converter can be the control element of an active filter. Shown in Fig. 1 is a circuit that generates a low-pass, single pole that can be moved over a dynamic frequency range of 2^n:1, where n is the resolution in bits of the d-a converter. If, for example, a converter with 10-bit resolution is used in this circuit, dynamic range is 1,024:1.

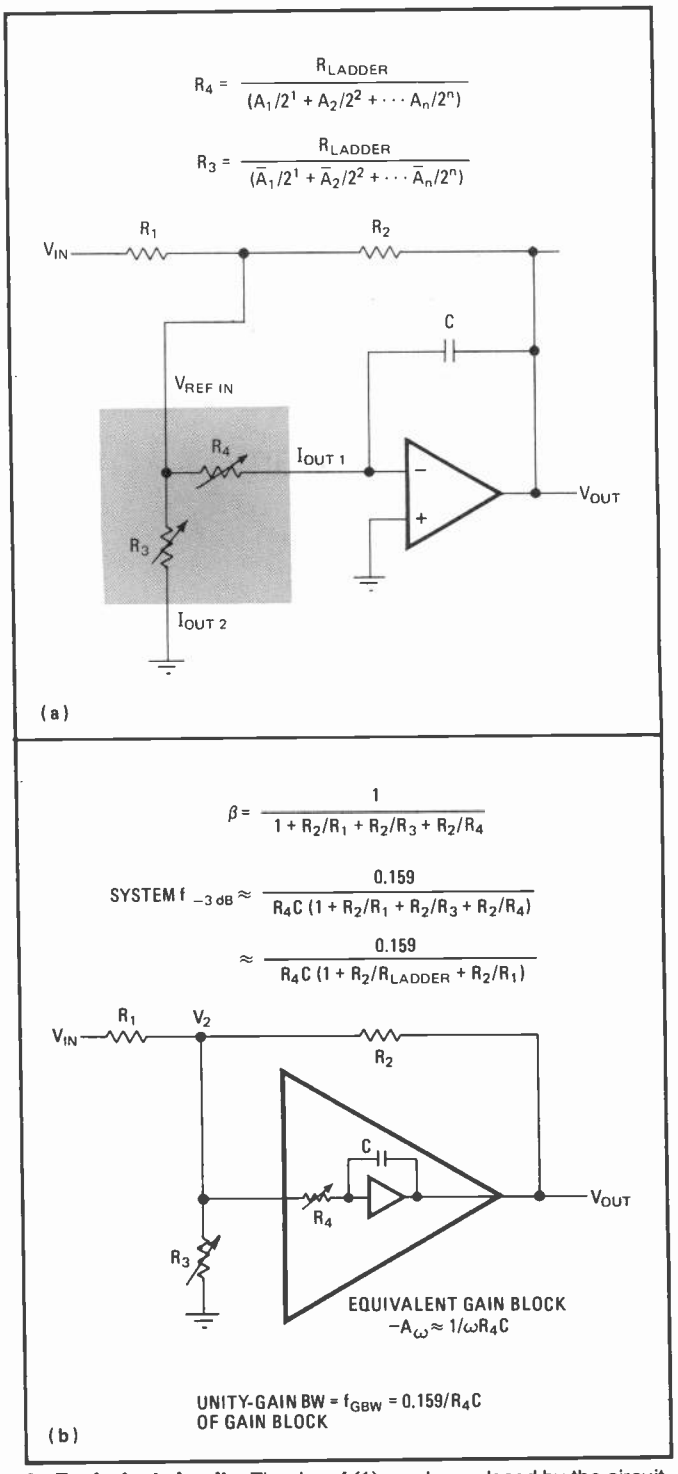
An equivalent simplified version of Fig. 1 is shown in Fig. 2(a), where R_4 and R_3 take on the values shown. R_{ladder} is the characteristic resistance of the R-2R ladder of the d-a converter and the coefficients A assume a value of 1 for an on bit, and zero for an off bit. Note that R_4 in parallel with R_3 equals R_{ladder}.

The circuit, consisting of R_4, C, and the amplifier, can be treated as a gain block as shown in Fig. 2(b). At frequencies above the open-loop corner, the response of the gain block is $A(\omega) = V_{out}/V_2$ or about $1/\omega R_4 C$. Its unity gain bandwidth is $F_{GBW} = 0.159/R_4C$.

Frequency response of a closed-loop amplifier is $F_{3dB} = BF_{GBW}$ where B is the amplifier feedback attenuation ratio. Using the unity gain bandwidth of the gain block and the system B results in the filter closed loop frequency response equations shown in Fig. 2(b). □



1. 1,024:1. An active low-pass filter such as this, built around an operational amplifier, passive components, and a 10-bit digital-to-analog converter, has a dynamic-frequency range of 1,024:1.



2. Equivalent circuits. The d-a of (1) can be replaced by the circuit within the dashed lines (a). A further simplification (b) lumps R4, C and the op amp into a gain block.

Twin oscillators form intruder detector

by Joshua Premack
Honeywell Inc., North Hopkins, Minn.

A system that can detect an intruder approaching an ungrounded metal object, such as a steel desk or a parked vehicle, is one job for a highly sensitive capacitive sensor. When scaled to operating frequencies high enough to give adequate bandwidth, the circuit is also suitable for many other applications, such as a capacitive microphone, capacitive seismic sensor, or an indicator of the eccentricity of the path of a rotating object.

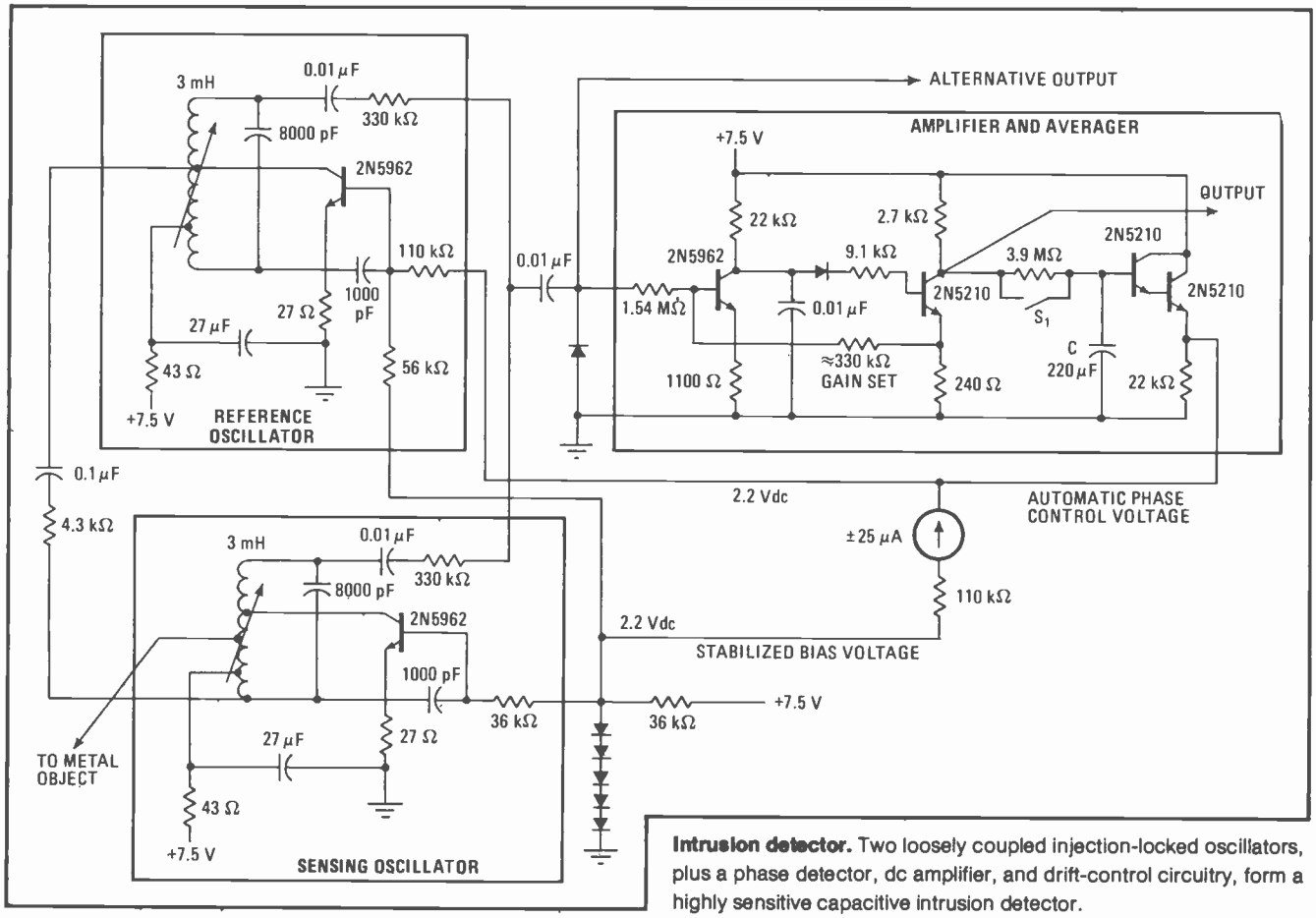
The circuit is based on the behavior of a pair of mutually synchronized oscillators. One oscillator is used as a reference, and the other is connected by a tap on its tank-circuit inductor to the object being protected. By this auto-transformer action, the loading effect on the oscillator, caused by the resistive component of the object, is reduced to an acceptable value. The protected object's capacitance is connected to an effective circuit capacitance of 2×10^6pF. A sensitivity of a few picofarads is available with a good signal-to-noise ratio. Bandwidth for a 33-kilohertz carrier is ± 25 hertz at 3 decibels down. If one of the oscillators, both of which have a small fixed coupling between their tuned circuits, is tuned to approach the frequency of the other, their combined output produces beats that indicate their frequency separation.

As tuning is continued in the same direction, the beat frequency decreases until the coupling pulls the oscillators into synchronism, whereupon the beats stop abruptly instead of decreasing smoothly to zero. At this adjustment, the oscillators are at the same frequency but are 90° apart in phase. As tuning is continued, the phase angle varies through 0° to 90° in the opposite direction. Then, with further tuning, the beats reappear.

If the coupling between the oscillators is reduced, the beat-free tuning interval narrows, but the ±90° phase shift always occurs between the onset and cessation of beats. This interval may be made very narrow by using very little coupling—provided that the oscillators are kept from drifting in frequency. Drift compensation is achieved with feedback by converting phase difference to an error voltage in a slow-feedback system, so that an interval of 5 to 6 pF on a base value of 8,000 is quite satisfactory.

In the intrusion-detection system, the two essentially identical oscillators have resistive coupling between the collector and base, which theoretically should keep the oscillators 180° out of phase when synchronized. The oscillators are actually designed to operate only 150° to 160° out of phase. Their outputs are summed at the junction of the two 330-kilohm resistors.

If the oscillators were exactly 180° out of phase, the voltage at the junction would be zero. The non-zero



Intrusion detector. Two loosely coupled injection-locked oscillators, plus a phase detector, dc amplifier, and drift-control circuitry, form a highly sensitive capacitive intrusion detector.

voltage at this point is the quiescent value, which increases as the capacitance in the sensing oscillator changes. This voltage is usable as an output of the circuit, especially when a wide dynamic range is wanted.

A two-stage dc amplifier provides an output and also charges a large capacitor—220 microfarads—through a 3.9-megohm resistor. This voltage changes very slowly in response to sudden changes in the capacitance of the sensing oscillator. This output also supplies part of the base bias for the reference oscillator, which compensates for any tendency of the oscillator to drift.

Before tuning the oscillators to synchronism and to the desired phase position, the time constant of the averaging circuit is shortened from 858 seconds to 0.594 second by closing the switch across the 3.9-megohm resistor. The tuning of the sensing oscillator is varied until the tuning meter dips suddenly, indicating that the oscillators are synchronized. When the meter reads zero, and after allowing several seconds to charge averaging capacitor C fully, the switch S is opened and the sensor is operational. This operation is easily automated.

When used as an intrusion detector, the circuit may be attached to ungrounded metal objects that have lossy (30% to 125% dissipation factors) capacitance, ranging from 500 to 15,000 picofarads. Overload-recovery time of the system from transients is in milliseconds, and that of desired signals is in the seconds range. The use of two injection-locked oscillators as a sensor is covered by patents 3,222,664 and 3,293,631.

No exotic measures were taken in the manufacture of these sensors, but care should be exercised to ensure good oscillator stability and tracking. Rapid temperature fluctuations should not be imposed on oscillator components, nor should large temperature differentials exist between the two oscillator assemblies. Careful attention should be given to confining the coupling between the oscillators to the desired path. Stray inductive coupling, common power-supply impedance, and possible paths where oscillator outputs are fed to the detector should be controlled. □

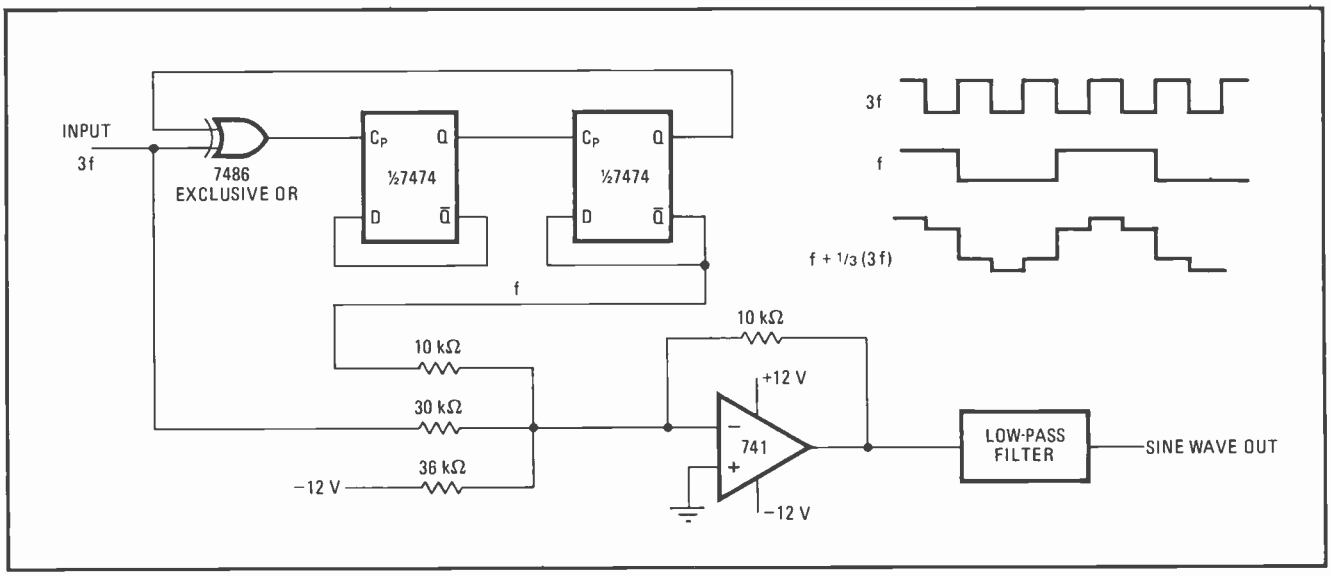
Frequency divider plus op amp approximates sine wave

by John Taylor
NOAA, Boulder, Colo.

A group of digital and analog integrated circuits can be combined to create an audio tone from a digital pulse train. Ordinarily a single flip-flop can convert pulses into a symmetrical square wave. But for many applications, it is desirable to produce a closer approximation to a sine wave.

This can be done with the circuit shown here. The frequency divider accepts a square wave at a frequency of 3f, and produces a square wave at the required output frequency f. Use of an exclusive-OR gate at the clock input of the first flip-flop results in two advantages over a more conventional divide-by-3 circuit: (1) the output is symmetric, and (2) the input (3f) is 180° out of phase with the third harmonic of the output (f).

This phase relation is such that if f and 3f are summed together in the 741 op amp (with weighting factors of ⅓ and 1 respectively), the third harmonic of square wave f is canceled. This produces a stepped waveform which is a much better approximation to a sine wave at frequency f than a square wave. If a zero average sine value is desired, a dc offset can also be included in the summation. If an approximate sine wave is not good enough, the output of the op amp can be filtered by a simple low-pass filter, since the lowest harmonic to be rejected is five times the fundamental. □



Pulse to audio. An exclusive OR, two-stage frequency divider and op amp are used to sum the third harmonic and fundamental of a square wave, producing a stepped approximation to a sine wave that is easily filtered.

Inductor simplifies memory-driver circuit

by Robert Johnson, Paul Feldman, and Edwin Fisher
Honeywell Information Systems, Billerica, Mass.

Designing memory systems with 4,096-bit n-channel random-access memories poses a number of problems with the associated interface circuitry. But a small inductance can at least eliminate the headache of having an extra power supply in the memory driver.

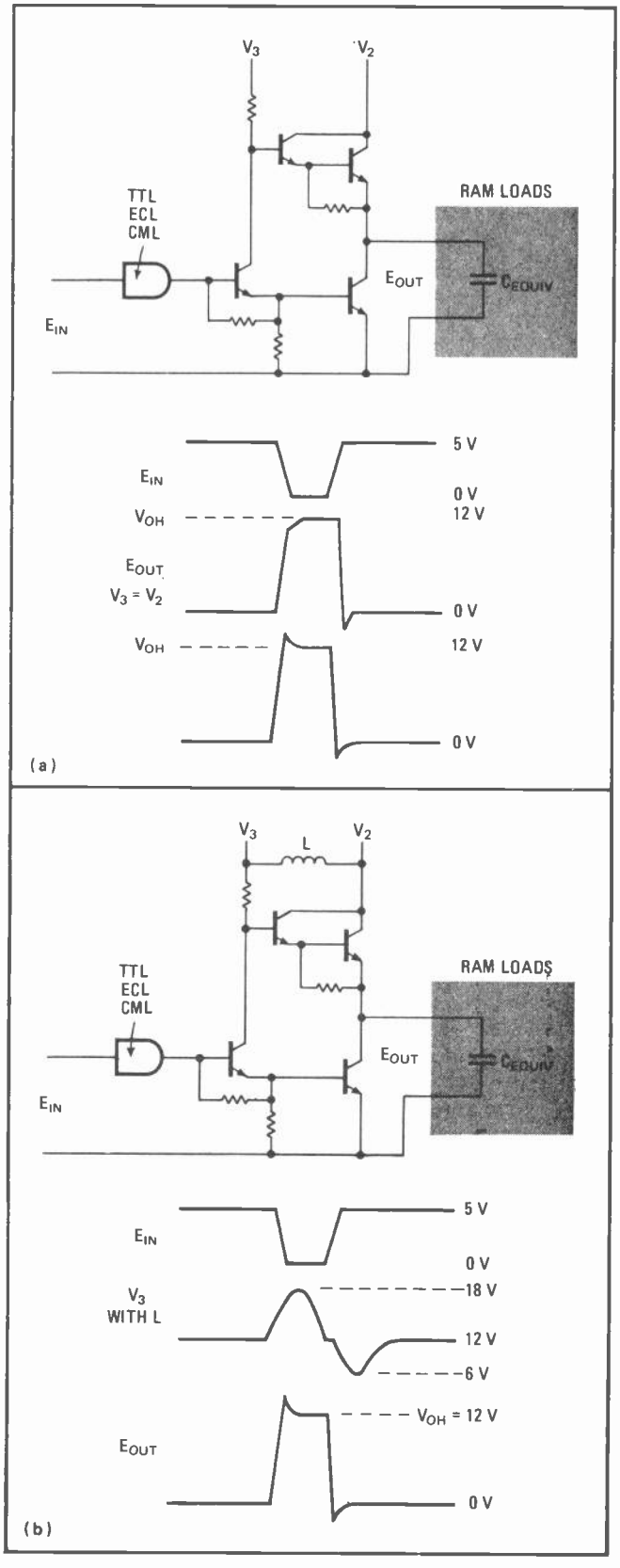
While most of such RAMs on the market today have inputs—all addresses, data-in, chip-select, and read/write—that are compatible with transistor-transistor logic, the clock or chip-enable clock input requires 0 to 12 volts for proper memory operation. Of particular concern is the memory's clock input, where a minimum high level of 11.4 V is required.

A common totem-pole output driver circuit—similar to the SN75365 or MC3960 initially used with p-channel RAMs—tied to a number of n-channel-RAM clock inputs, is shown in (a). Capacitive loading is typically 390 picofarads per clock driver. When $V_2 = V_3 = V_{DD}$, the outputs appear degraded, and $V_{OH} = V_{DD} - 1$ V at $I_{OH} = 50\ \mu A$. Increasing V_3 to $V_{DD} + 3$ V changes the output to a more acceptable level, normally $V_{DD} - 0.3$ V at $I_{OH} = 100\ \mu A$.

However, in n-channel systems, the values of V_{DD} and V_{CC} are usually 12 V and 5 V, respectively. If the method of increasing V_3 is used, V_{DD} must be raised to 15 V for V_3 and then dropped back down to 12 V for V_2 and other parts in the system to generate a separate supply voltage on each array card. The alternative is for a separate supply voltage to be bused in for V_3. These methods, while feasible, are not very practical because of increased power consumption and cost.

A way to provide the correct output levels for both chip and driver with only a +12 V supply is to place an inductor from V_3 to V_2. The inductor overcomes the drawbacks of operating with $V_3 = V_2$ without adding a supply greater than V_{DD} to the system, as shown in (b). The inductor provides an energy source in the form of a voltage "kick" whenever the output totem pole is in a transition state. The increased voltage on V_3 supplies the additional current needed as E_{out} changes from low to high, resulting in a smooth and uninterrupted transition to V_{OH}.

A small value of L will not provide an adequate voltage increase at V_3, while too large a value will not recover fast enough at high repetition rates. Values between 36 and 100 microhenries work well at a pulse width of 500 nanoseconds and repetition rates of 1 microsecond or less. □



Compensating the 555 timer for capacitance variations

by Kenneth Lickel
Philips Medical Systems Inc., Shelton, Conn.

With the 555 timer, any error in the value of the external timing capacitor causes a corresponding error in the duration of the output pulse. If several fixed timing resistors are used to permit selection of various output pulse widths, it may be desirable to compensate for the capacitor variation instead of changing each timing resistor. The circuit below allows correction for capacitor tolerance variations up to ±12.5% by adjustment of a single variable resistor.

The output pulse width, t, is given by the time required for the timing capacitor to rise to the value of the control voltage, V_{CON}. That relationship can be shown by the equation:

$$V_{CON} = V_{CC}(1 - e^{-t/RC})$$

or

$$t = -RC\ ln(1 - V_{CON}/V_{CC})$$

This equation shows that the pulse duration depends on the ratio of V_{CON} to supply voltage V_{CC} for given values of timing resistor R and timing capacitor C.

In the technique used to compensate for error in the timing-capacitor value, the ratio V_{CON}/V_{CC} is varied with an external resistance that shunts the 10-kilohm resistance inside the timer. As the circuit diagram shows, this external resistance consists of a 200-kilohm variable resistor R_A in series with a 17.8-kilohm fixed resistor R_B. The ratio V_{CON}/V_{CC} determined by the voltage-dividing network is:

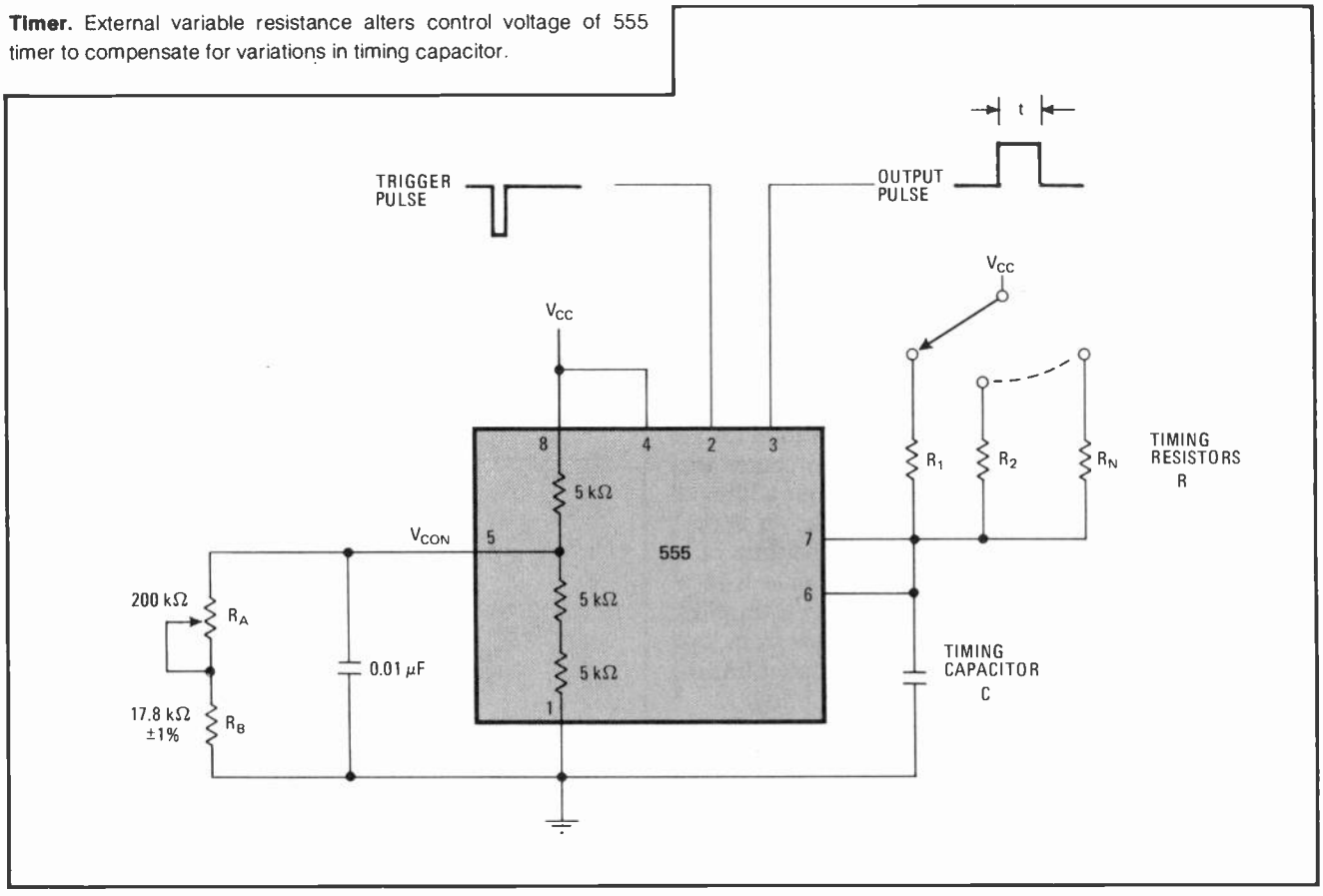
$$V_{CON}/V_{CC} = R_p/(R_p + 5\ k\Omega)$$

where

$$R_p = (10\ k\Omega)(R_A + R_B)/(10\ k\Omega + R_A + R_B)$$

If R_A is set at its minimum value (zero):

Timer. External variable resistance alters control voltage of 555 timer to compensate for variations in timing capacitor.



$R_p = 6.4\ k\Omega$

and

$V_{CON}/V_{CC} = 0.56$

Therefore, the pulse duration is

$t_{min} = 0.83\ RC$

Similarly, if R_A is set at its maximum value (200 kilohms), the pulse duration is:

$t_{max} = 1.07\ RC$

Thus the variation of R_A can vary the output-pulse width by ± 12.5% about a nominal value of (0.83 + 1.07)RC/2. For the circuit shown, therefore, the nominal width of the output pulse is:

$t_{nom} = 0.95\ RC$

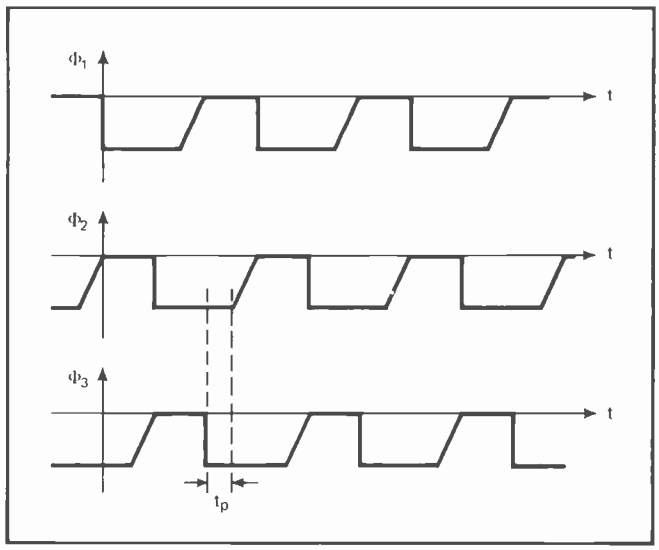
If values for the timing resistors and capacitor are calculated from this formula, then capacitor variations of ±12.5% can be compensated by adjustment of R_A. If wider tolerances are desired, R_B must be reduced; new values must then be calculated for R_p, V_{CON}/V_{CC}, t_{min}, t_{max}, and t_{nom}. □

Generating overlapped clock phases for CCD array

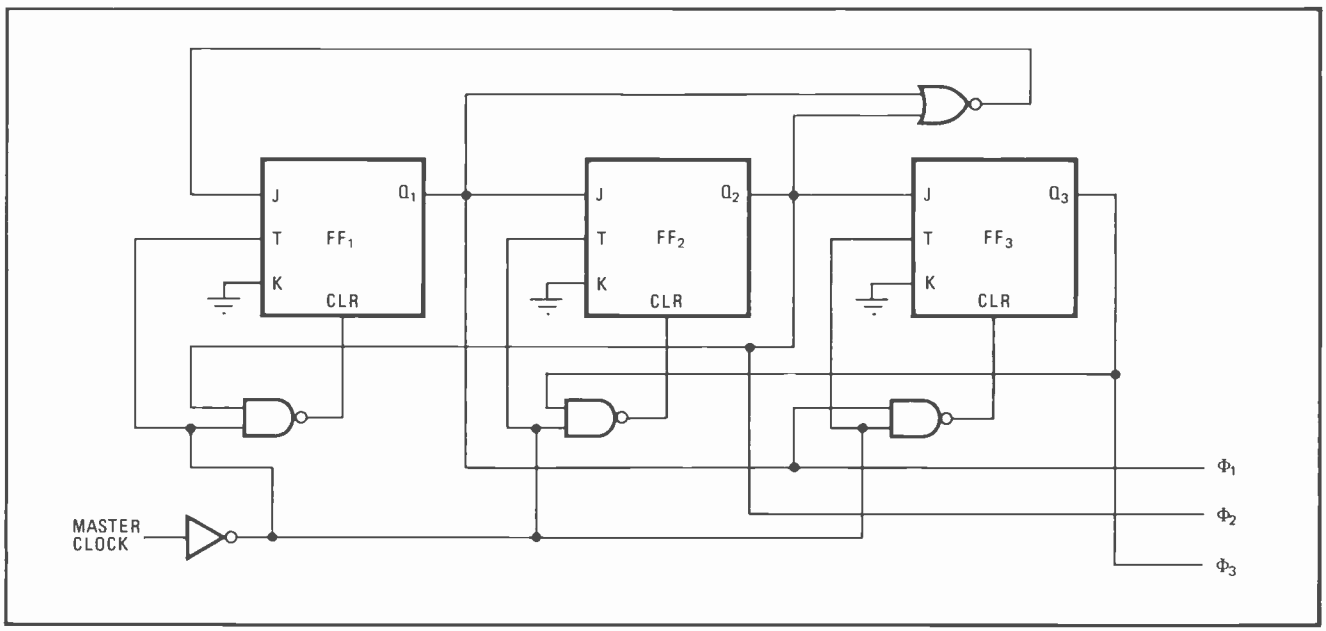
by Hans-Jörg Pfleiderer and K. Knauer
Siemens AG, Munich, Germany

Arrays of three-phase charge-coupled devices require overlapped clock pulses (Fig. 1) for satisfactory operation. To generate these overlapped pulses, Fairchild Semiconductor, which produces the arrays commercially, suggests a rather complicated logic circuit in a report that it circulates.

But a less complicated circuit (Fig. 2) can also generate the train of overlapped pulses, as shown in the timing chart (Fig. 3). When the master clock pulse goes high, J-K flip-flop FF_1 turns on only if the outputs Q_1 and Q_2 are both low. With FF_1 on, Q_1 rises, opening the gate so that the rise of the next master clock pulse turns on FF_2, without affecting FF_1. However, with Q_2 up,



1. Overlap. Arrays of three-phase charge-coupled devices require overlapping pulse trains for proper operation. The logic to produce these trains does not have to be complicated—it need not involve more than three flip-flops and a few gates.

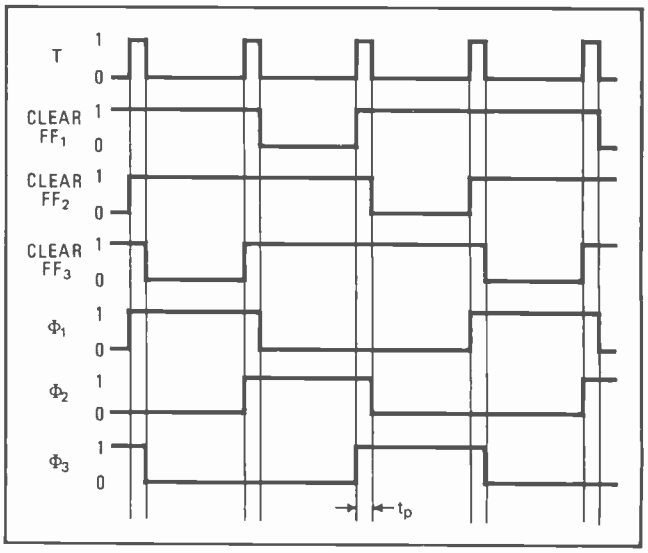


2. Pulse-train generator. When the master clock's pulse rises, one flip-flop turns on, gated by the state of the flip-flop before it. When the pulse falls, the preceding flip-flop turns off, this time gated by the state of the following flip-flop.

the fall of the master clock's pulse clears FF_1 via the CLR input of FF_1.

This approach—setting the output of each flip-flop high with the J input, provided the preceding flip-flop is already on, and setting it low with the clear input when the following flip-flop is on—is used for each of the three flip-flops. The width of the overlap is approximately equal to the width of the master clock's pulse, and the frequency of each waveform is one third that of the master clock's pulse. The circuit is self-correcting and also self-starting.

The same idea can also be used in driving the phase voltages for a two-phase CCD. □



3. Pulse timing. As the three flip-flops turn on and off (second, third, and fourth traces from top), their outputs overlap by the width of the clock pulse, minus circuit delays. The frequency of each waveform is one third that of the master clock's pulse.

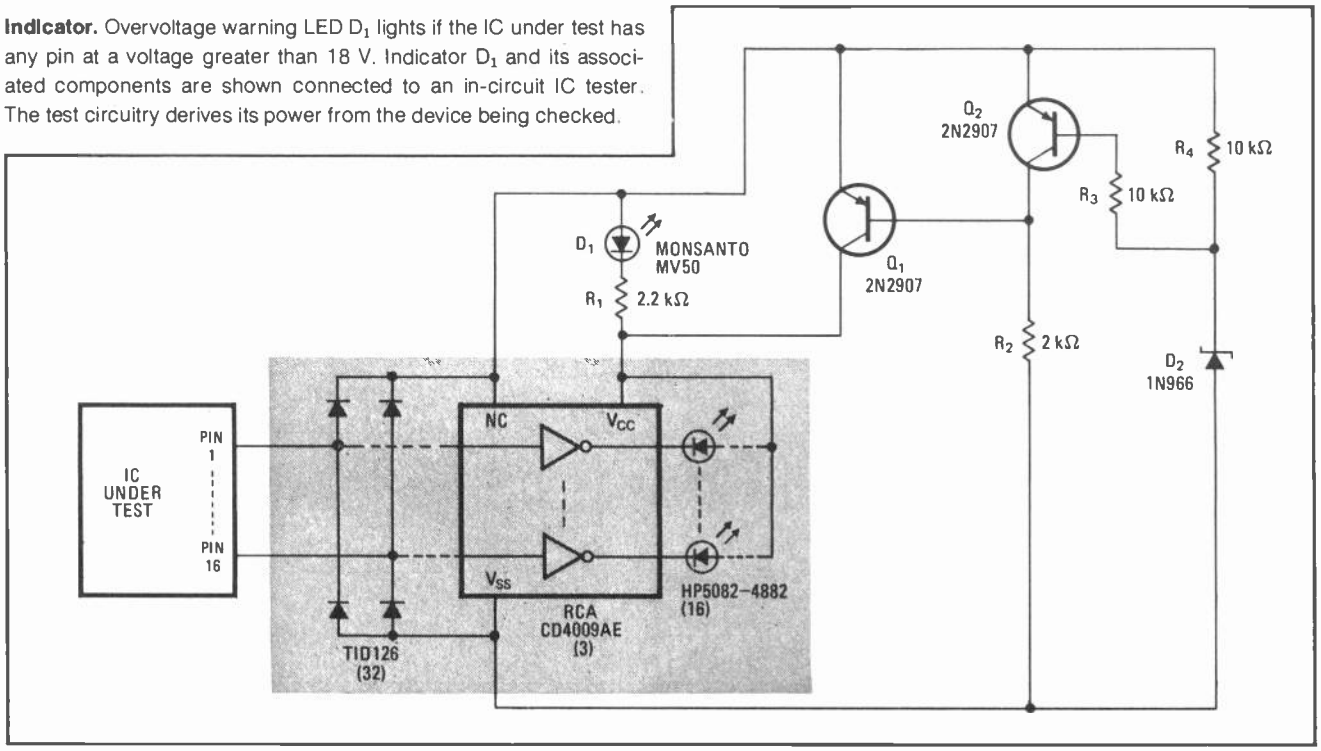
Overvoltage indicator can be added to C-MOS IC tester

by Rajni B. Shah
Rohde & Schwarz, Fairfield, N.J.

A warning light that signals the presence of an overvoltage can be added to the features described in "In-circuit IC tester checks TTL and C-MOS" [*Electronics*, May 30, 1974, p. 120]. A light-emitting diode glows if the IC under test has any pin voltage greater than 18 V. The warning circuit, like the rest of the test circuit, draws its power from the IC being checked. As described here, it can operate at overvoltages as high as 30 V.

The indicator circuitry, shown below, is connected to the tester described previously. Warning LED D_1 is shunted by Q_1, which is normally held in conduction by the potential applied to its base through R_2. Q_2 is normally inhibited by the base connection through R_3. If the voltage at any IC pin exceeds 18 V, however, zener diode D_2 breaks down, and Q_2 starts to conduct. Conduction in Q_2 pulls the base of Q_1 up to turn off Q_1. The voltage drop across Q_1 then is sufficient to light up LED D_1, indicating the overvoltage. □

Indicator. Overvoltage warning LED D_1 lights if the IC under test has any pin at a voltage greater than 18 V. Indicator D_1 and its associated components are shown connected to an in-circuit IC tester. The test circuitry derives its power from the device being checked.



Optically coupled ringer doesn't load phone line

by William D. Kraengel Jr.
Valley Stream, N.Y.

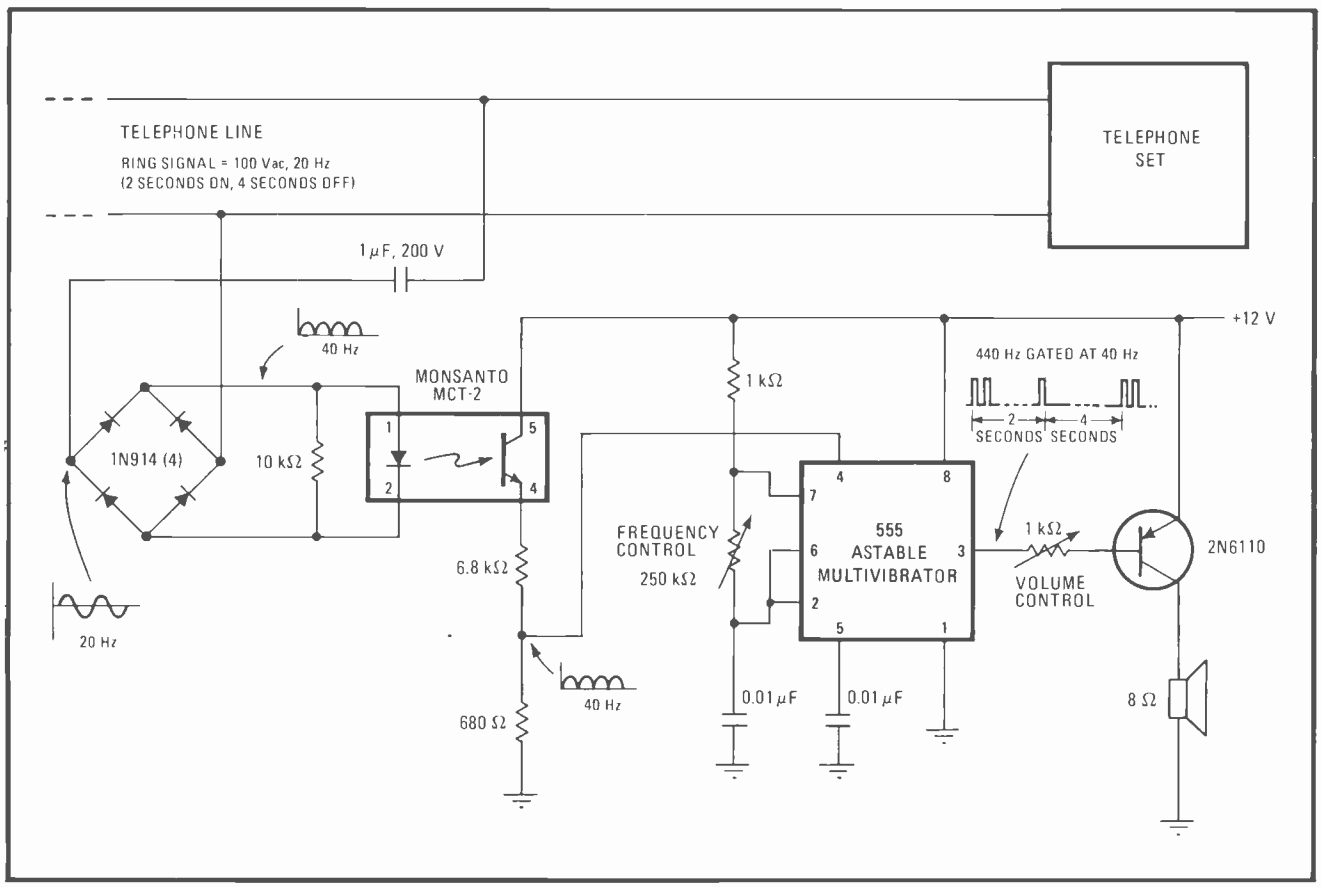
If passed through an opto-coupler, the ringing signal on a telephone line can be made to operate a remote ringer without overloading telephone-company lines, without interfering with company service, and without degrading operation of the line receiving the signal. The opto-coupler can also be used to operate other equipment, such as a telephone message recorder. The arrangement imposes only a 10-milliampere load on the ac ringing signal and no load at all on the dc voice signals.

In this arrangement, the opto-coupler transfers the ringing signal to the rest of the remote-ringer circuitry and also isolates that circuitry from the telephone line. The output current from the opto-coupler activates a 555 timer that is configured as an astable multivibrator; the audio frequency from the multivibrator, amplified and fed to the remote loudspeaker, then sounds whenever a ringing signal comes in on the telephone line.

As indicated on the circuit diagram, the telephone ringing signal of about 100 volts at 20 hertz has a cycle of 2 seconds on and 4 seconds off. This signal is applied to the light-emitting diode of the opto-coupler through a 1-microfarad capacitor; the capacitive reactance at 20 Hz is about 10 kilohms, which limits the current of the light-emitting diode to 10 mA. The frequency is doubled by the full-wave bridge simply because a 40-Hz gating rate in the sound from the loudspeaker is more pleasing to the ear than a 20-Hz rate.

The 40-Hz output from the coupler is applied to the reset input of the 555 multivibrator. The free-running frequency of the multivibrator is set at a nominal 440 Hz, which is the frequency of the ring-back tone in a telephone, or at whatever frequency is most pleasing to the listener. The frequency can be adjusted by the 250-kilohm resistor. The free-running duty cycle, which would be fixed at 50% by the 1-kilohm resistor, is approximately 35% here because of the 40-Hz modulation of the gating signal.

The output from a 555 timer is sufficient to drive a small speaker through a current-limiting series capacitor with no further amplification. In most applications, however, power-amplification is required. The amplification need only be of the switching type because of the rectangular output of the 555. At current levels below



Remote ringer. Opto-coupler flashes telephone-ringing signal to remote-ringer circuitry and isolates that circuitry from phone line. Circuit puts 10-mA load on ac ringing signal, and no load on dc voice signals. Frequency and volume at remote loudspeaker can be adjusted.

50 mA, the 555 is more effective as a current sink than as a current source; for maximum efficiency and power output, therefore, a pnp switching transistor is used.

The component values shown produce an output power of about 5.5 W, which is almost the theoretical maximum that can be obtained with a single 8-ohm speaker, a V_{CC} of 12 V, and a 35% duty cycle. Higher output-power levels can be achieved by greater amplification or lower speaker impedance. At higher levels, multiple speakers can be used in a series-parallel arrangement, with each speaker using a matching L-pad for individual level control.

This circuit draws a standby power of about 120 mW from the 12-V dc supply. To reduce standby power to almost zero, a dual opto-coupler can be used. The second isolated and synchronized output is used to gate a triac static switch that turns on the power supply.

Even though this optical-coupling technique avoids severe loading of the line, the telephone company should be consulted before the ringer is installed. □

Regulated power supply is adjustable from 0 to 38 V

by Frank P. Miles
Rochester, N.Y.

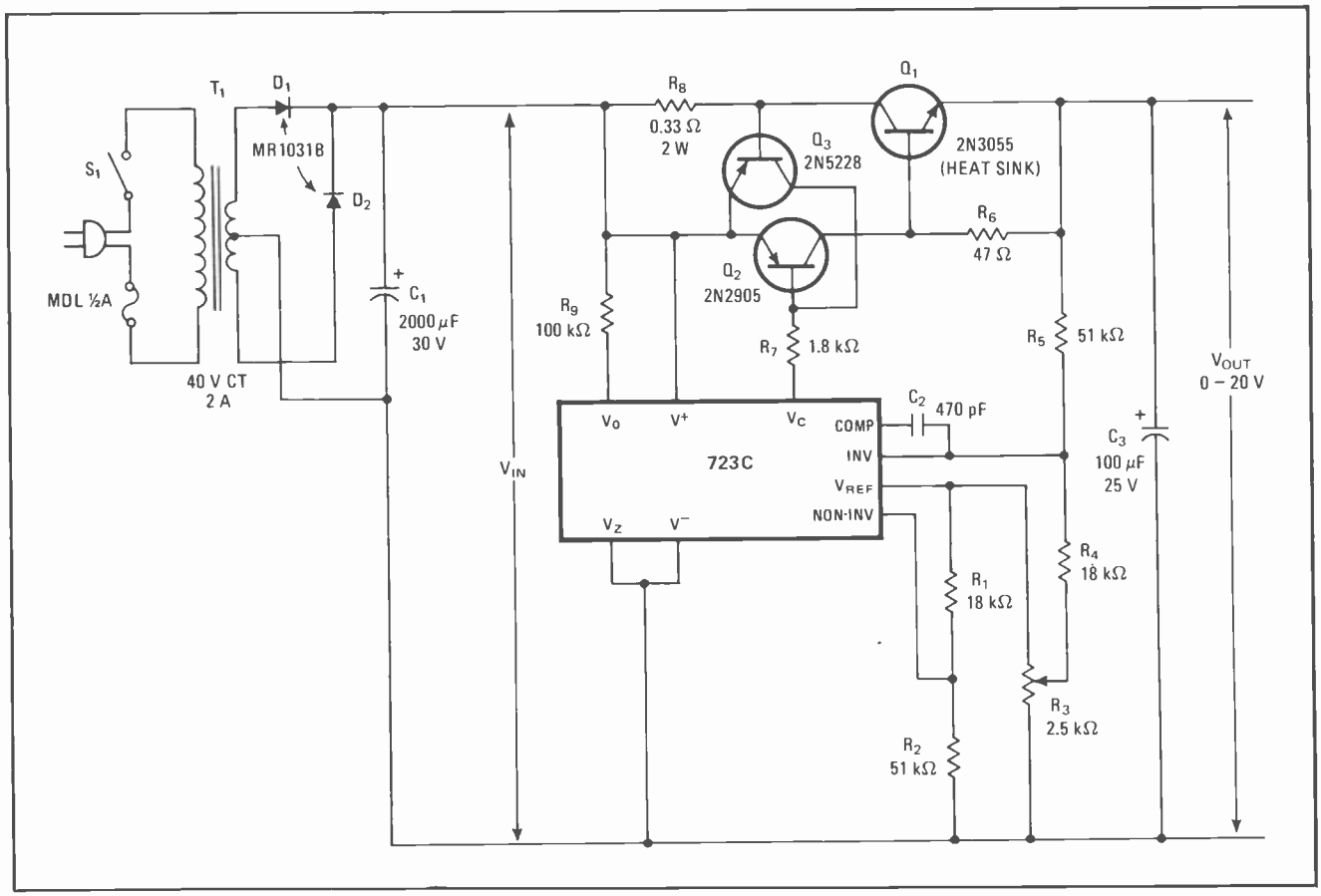
Through careful biasing of the error-sensing and the output driver for a 723C voltage regulator, a power supply that is variable from 0 to 38 volts can be designed. The stability of the circuit over both time and temperature is excellent, depending only on the internal reference of the chip and being essentially independent of output level. And finally, the circuit requires few components; most notably, it requires no zener diodes external to the 723C.

The schematic shows how simple it is to custom-design the supply. R_3 is a 2.5-kilohm potentiometer, chosen to keep the reference current below 5 milliamperes. $R_1 = R_4$ and $R_2 = R_5$ for best bias stability and output-range swing. The leakage-limiting resistor R_6 has a value of 47 ohms; it increases the safe operating area of Q_1.

The maximum output voltage is given by

$$V_{OUT(max)} = (R_2/R_1)V_{REF}$$

where the reference voltage V_{REF}, a characteristic of the 723C, is typically 7.15 V. Resistor R_1 is picked to be high enough to minimize loading of R_3, but small enough to avoid bias-current problems at the error-am-



Regulated power supply. Setting of R_3 gives output voltage as low as 0 V, or as high as V_{IN} minus small drop across Q_1. Value of V_{IN} must not exceed 40-V limit of the 723C. Components shown here are for 0–20-V, 2-A supply.

plifier inputs. Resistor R_2 is then calculated from

$$R_2 = (V_{OUT(max)}/V_{REF})R_4$$

The other resistors are calculated from straightforward circuit considerations. Resistor R_7 limits the output drive of the 723C to about 10 mA because the internal zener diode is used. Its value, in kilohms, is

$$R_7 \approx 0.1\ V_{IN} - 0.62$$

where V_{IN} is the unregulated voltage out of the rectifier. (The value of V_{IN} must not exceed the 40-V limit of the 723C.) R_8, calculated in ohms, provides the proper current-limit point:

$$R_8 \approx 0.65/I_{LIMIT}$$

where I_{LIMIT} is the maximum output current (in amperes). The pass transistor characteristics and heat sink are also determined by the value of I_{LIMIT}. Resistor R_9, calculated in kilohms, maintains zener regulation for low output currents:

$$R_9 \approx 5V_{IN} - 31$$

The output voltage from this supply can be as low as 0 V, or as high as V_{IN} minus a small drop across the pass transistor. The component values shown in the circuit diagram are chosen for a 0–20-V, 2-A supply. □

Comparator and D-MOS switch rectify small signals linearly

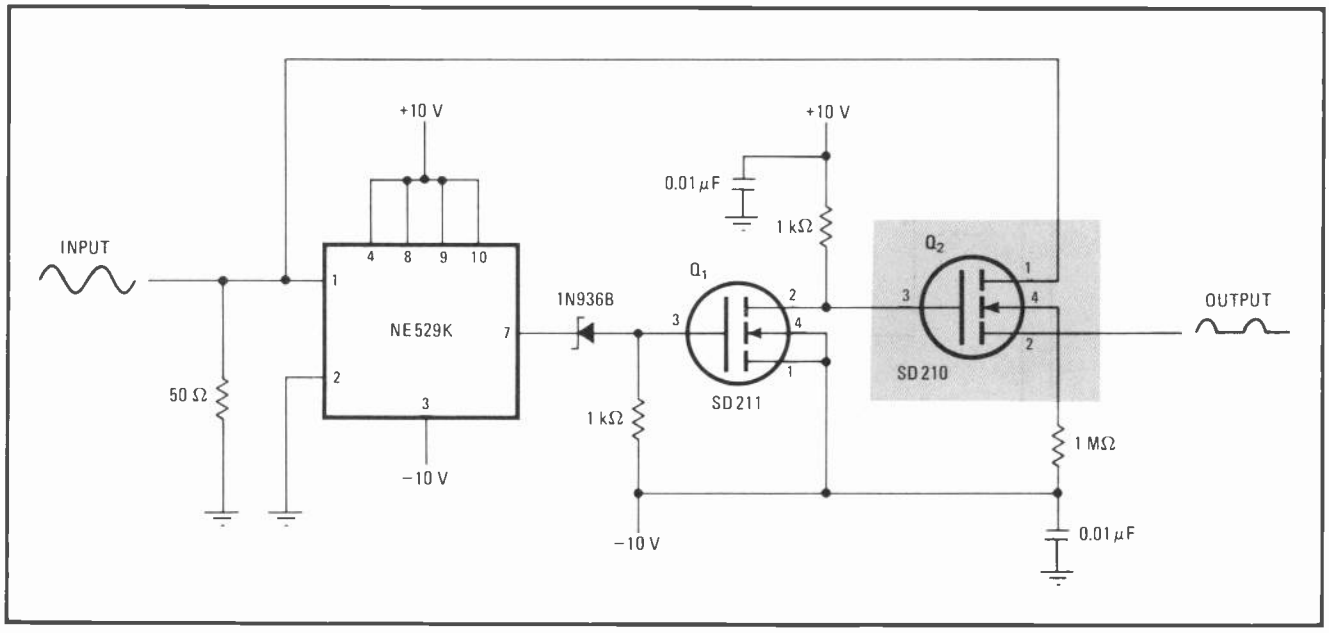
by Tom Cooper
TRW Systems, Redondo Beach, Calif.

Rectifying low-level signals with conventional silicon diodes has always been cumbersome. The reason: input signals lower than the diode's turn-on voltage of approximately 0.6 volt result in a nonlinear output that is generally made linear by the addition of one or two operational amplifiers. But if an analog comparator and a two-FET switch are used instead of the silicon-diode-and-amplifier combination, it's possible to rectify waveforms with amplitudes as low as 6 millivolts at frequencies as high as 3 megahertz, while providing an output that can be filtered to yield a dc value directly proportional to the amplitude of the input signal.

The circuit is shown below. In this precision half-wave rectifier, the input signal is applied to field-effect transistor Q_2 and also to the NE529 high-speed comparator (20-ns propagation delay), which senses the zero crossings of the input voltage. The output from the comparator passes through a level-setting zener diode and drives a high-speed analog switch (2-ns turn-on time) that consists of double-diffused metal-oxide-semiconductor (D-MOS) FETs Q_1 and Q_2. The comparator and Q_1 drive Q_2 into the on state at each positive zero crossing of the input waveform that is to be rectified, and into the off state at each negative zero crossing.

Because Q_2 is on when the input signal applied to its source terminal is positive and is off when the input is negative, the output from Q_2 is a half-wave-rectified version of the input waveform. □

Half-wave rectifier. Analog switch Q_2 is driven on and off at the zero crossings of the low-level input signal, producing a precise half-wave-rectified version of the input waveform. Amplitude can be as low as 6 mV and frequency as high as 3 MHz.



ICs interface keyboard to microprocessor

by Donald P. Martin and Kerry S. Berland
Martin Research Ltd., Chicago, Ill.

A compact, economical interface between a keyboard and a microprocessor can be designed with only three integrated-circuit chips. The ICs are a 5740 MOS scanning keyboard encode, a 2812 MOS first-in/first-out (FIFO) memory, and a 74125 quad three-state buffer. All three can be mounted with the standard array of keyswitches and diodes on a single circuit board.

The 5740 keyboard encoder has 10 scan inputs and nine scan outputs. A unique combination of one input and one output is assigned to each key, adding up to 90 keys in all. The keys are wired between the scan inputs and the outputs with a diode in series, as shown in the circuit diagram. The diodes block sneak signal paths and eliminate "phantom key" effects if several keys are pressed at the same instant.

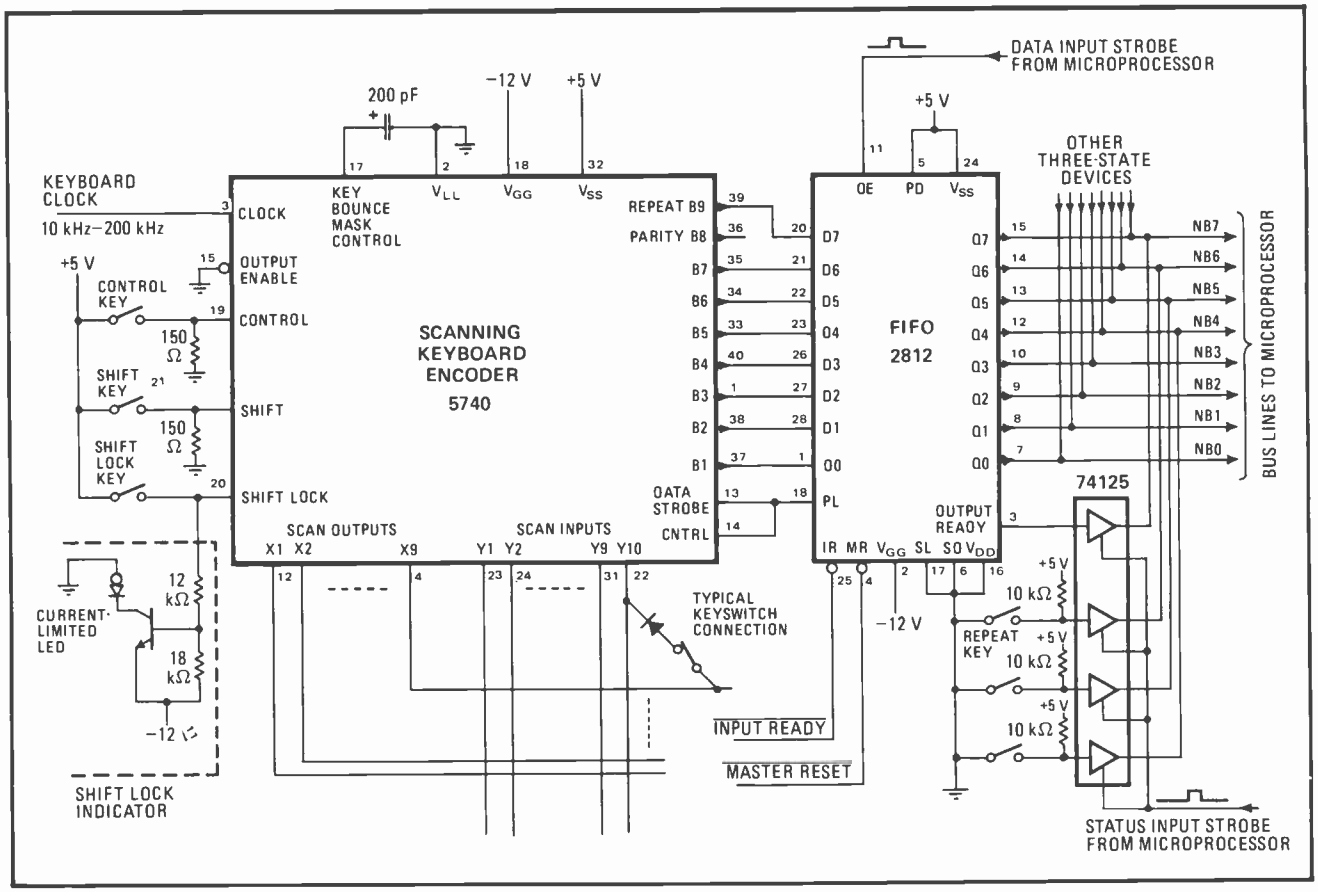
Internal ring counters simultaneously scan both the key matrix and an internal read-only memory. When a key is pressed, the ROM word corresponding to that key is transferred into a one-character nine-bit output latch. The word includes the seven-bit ASCII code for the character, parity bit B8 (which is not used in this design), and the selective repeat bit B9. The 5740 requires an external clock oscillator in the 10-to-200-kilohertz range to drive the scanning counters; this can be obtained from the main timing circuit of the microprocessor.

The internal circuitry of the encoder also performs other necessary functions; it suppresses keybounce effects, responds to key closures even if the previous key has not yet been released, and senses the shift, shift lock and control mode keys.

When the encoder recognizes a keystroke, it sets its data strobe output high. This terminal is wired directly to the encoder's data strobe control, an input terminal that resets the encoder output on the next falling edge of the keyboard clock. The data word is thus available at the encoder for only one clock period.

If no more data storage were provided than the one character stored by the encoder, the microprocessor would have to test for new keyboard data at a rapid rate. This requirement would be a severe constraint on the software, so the 2812 FIFO is included in the interface to provide storage of up to 32 characters.

The keystroke that sets the encoder data strobe high also strobes the parallel load (PL) input of the FIFO and loads the ASCII character into the FIFO. The loaded character moves down through the 32 positions until it either reaches the output or is stopped by a previously



Interface. Three ICs connect keyboard to microprocessor. Encoder provides up to 90 keys. FIFO stores 32 characters. Connections to microprocessor are made through three-state devices to the same 8 bus lines as used by other data sources. All three ICs can be mounted with keyswitches and diodes on a single circuit board, so when keyboard is not included in system, neither are interface components.

stored character. When there is at least one character stored in the FIFO, the output ready signal goes high. This signal is periodically tested by the microprocessor to see whether there is new data from the keyboard. With the FIFO providing buffer storage, the microprocessor needs to test for input data far less frequently.

The FIFO's parallel dump (PD) control is permanently enabled (wired to +5 volts). However, the parallel dump function is also internally gated with the output enable (OE) terminal; therefore the first-received character will not be dumped until the OE terminal is activated. Thus a single strobe to the 2812 first reads the keyboard word into the microcomputer, then dumps the word out of the FIFO, moving the next keyboard character into the output position. The delay between the leading edge of the data input strobe and the appearance of valid data on the microprocessor input bus is less than 400 nanoseconds for the 2812.

When power is first applied, the FIFO registers are cleared by a signal from the master reset circuit of the microprocessor. This signal goes low for a fraction of a second, preventing the FIFO from taking on initial random states that could be interpreted as keyboard data.

To load information into the microprocessor, status input and data input instructions are used. The microprocessor periodically pulses the status input strobe line. This pulse activates the 74125 three-state buffer, which puts the FIFO's output ready bit on the high-order input bus line of the microprocessor. (This is input bit 7, or NB7.) The microprocessor tests this bit to see whether keyboard data is available; if the bit is high, indicating that a character is stored in the FIFO, the microprocessor executes a data input instruction. This instruction activates the output enable terminal of the FIFO, and impresses the keyboard data word on to the input bus to the microprocessor.

The seven lower-order bits of the keyboard data word are the ASCII-encoded character. The high-order bit, NB7, is the selective repeat bit B9. The repeat switch is connected to the next-highest bit through an extra three-state buffer. The repeat function is implemented easily through a few instructions stored in the ROM. □

Digital command inverts signal

by Craig J. Hartley
Baylor College of Medicine, Houston, Texas

Many digital designs require voltage-controlled signal inversion. The circuit shown here accepts bipolar inputs with amplitudes up to ±7 volts and has a gain of either +1 or −1, depending on the logic level at the control terminal. A TTL-logic level of 1 produces a gain of +1 (no inversion of the input signal), and a logic level of 0 produces a gain of −1 (signal inversion). The circuit uses a 741 operational amplifier and two transistors.

When the control logic is high, both Q_1 and Q_2 are turned off, and the operational amplifier becomes a voltage follower. The input signal E_i is present at both input terminals and at the output terminal of the op amp, so no current flows through resistors R_1, R_2, or R_3. Therefore the gain in this logic-low mode is independent of the values of the resistors and is given by

$$E_o/E_i = +1$$

When the control logic is low, both Q_1 and Q_2 are saturated, so the noninverting terminal of the op amp is grounded and the input signal is applied only to the inverting terminal. Therefore the gain is

$$E_o/E_i = -R_2/R_1$$

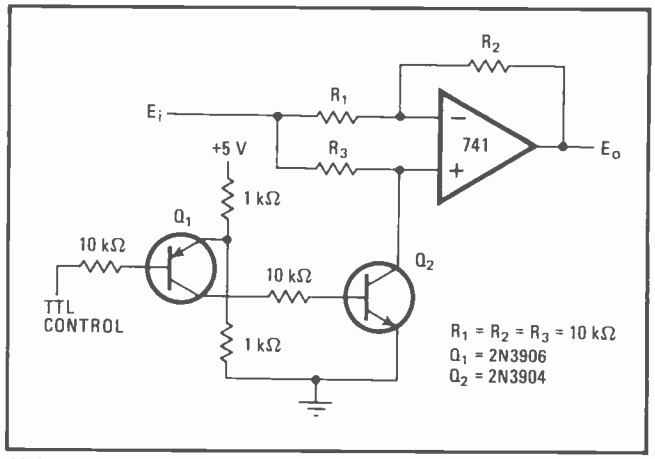
In this circuit R_1 and R_2 are equal, and therefore the gain in this logic-low mode is

$$E_o/E_i = -1$$

In this mode of operation, there is an offset proportional to the saturation voltage of Q_2:

$$V_{offset} = V_{sat}(1 + R_2/R_1) = 0.02\ V$$

Because this circuit is intended to handle bipolar input signals, Q_2 must be driven by a high-impedance source such as Q_1, so that Q_2 is turned off by having its base open-circuited, rather than by having its base grounded. If the base of Q_2 were grounded, negative input signals to the circuit would forward-bias the base-to-collector junction and distort the output signal. With the circuit shown here, the negative input swing is limited by the base-to-emitter breakdown voltage of Q_2 (i.e., 6 to 10 V), while the positive input swing is limited only by the op amp saturation voltage. □



Voltage-controlled inverter. Circuit transmits or inverts input signal, depending on logic level at control terminal. Logic 1 produces a gain of +1 (no inversion), and logic 0 produces gain of −1 (inversion). Maximum signal swing is ±7 volts. Offset is about 0.02 volt.

Silent timer warns of tape run-out

by Vernon R. Clark
Applied Automation Inc., Bartlesville, Okla.

At concerts and lectures especially, a cassette tape often runs out unnoticed. One solution is to install timing circuitry in the cassette-recorder case that will cause a light to flash when it's time to reverse or replace a cassette or to switch to another recorder. This silent warning system is also useful in duplicating cassette masters, where a preset recording time is important.

The alarm circuit operates from any voltage in the 5- to-15-volt range and can either be connected to the recorder bus or use its own battery. When the circuit is turned on, a light-emitting diode begins to blink once or twice per second, indicating that the circuit is functional and ready to start timing. When the start-timing button is pushed, the LED stops flashing and stays off for the duration of the timing period. At the end of the timing period, the LED begins to flash again, giving the signal to flip the tape.

The two main components of the circuit are a 14536 programable-timer integrated circuit and a 74C00 quad NAND gate IC. The timer contains an oscillator and a 24-stage counter. It counts pulses from the oscillator and, when some specified counter stage goes high, delivers a positive output pulse from the decode-out terminal (pin 13). Which of the counter stages triggers the output is specified by the voltages on pins 9, 10, 11, and 12. If these pins are high, high, low, and low, respectively (logic 1100), an output appears every time that stage 12 of the counter goes high. With all four pins high (logic 1111), output appears when stage 24 goes high.

Since this system was designed for a standard C90 cassette, which runs for 45 minutes a side, the timer is adjusted to provide a timing period of 44 minutes, or 2,640 seconds.Therefore the oscillator frequency is set at

$$f_{osc} = 2^{23}/2{,}640 = 3.2 \text{ kilohertz}$$

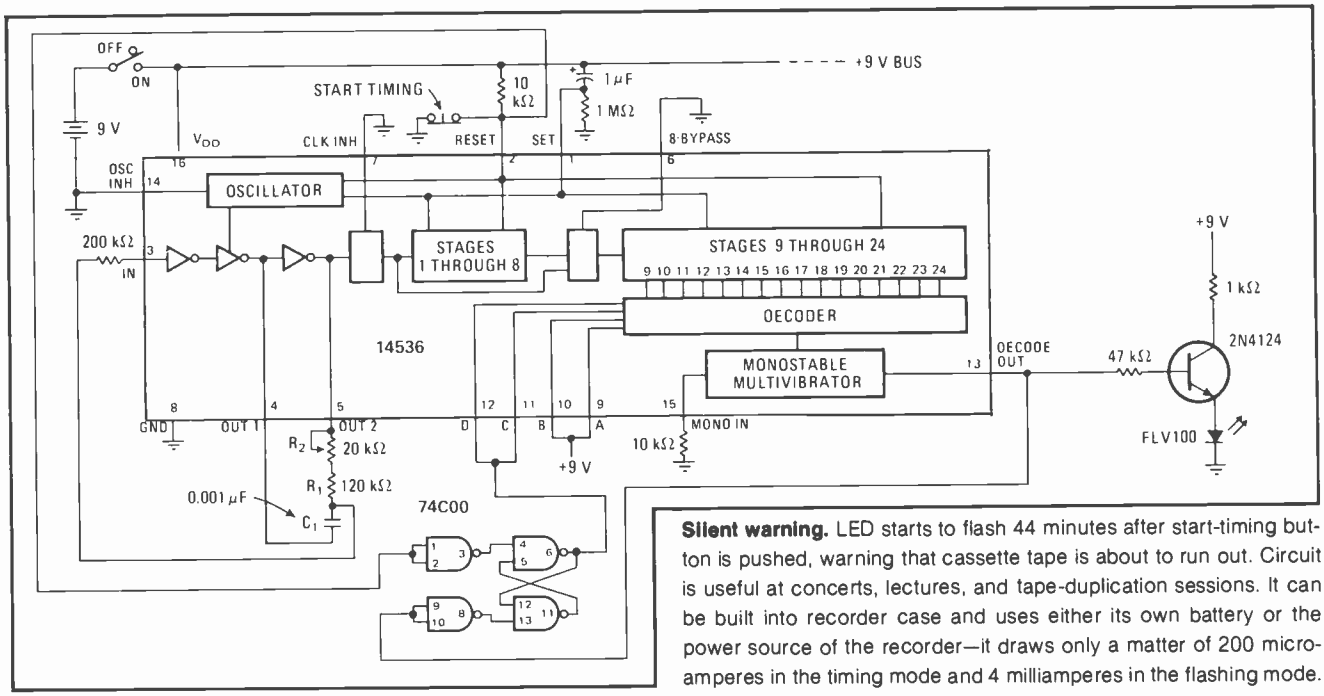
so that counting stage 24 will go high 44 minutes after the counter starts counting pulses from the oscillator (provided the decoder logic is 1111).

With this oscillator frequency, if the decoder terminals are set at logic 1100, stage 12 goes high after 2^{11} pulses, or

$$2^{11}/3.2 \text{ kHz} = 0.65 \text{ second}$$

The oscillation frequency is set by the time constant of C_1 and $(R_1 + R_2)$. A frequency meter is connected to pin 5, and R_2 is adjusted till the meter shows 3.2 kHz.

The circuit operates as follows: while the on-off switch is off, all pins are low. When the switch is turned on, pins 9 and 10 of the timer go high because they are wired to the positive-voltage bus. Therefore the decoder is programed with logic 1100, and the LED begins to flash every 0.65 second. When the start-timing button is pushed, the quad NAND circuit sets the decoder to logic 1111, so the LED stops flashing and the 44-minute count begins. After 44 minutes, the decode-out terminal (pin 13) goes high, resetting the decoder to 1100 so that the alarm signal flashes again. □



Silent warning. LED starts to flash 44 minutes after start-timing button is pushed, warning that cassette tape is about to run out. Circuit is useful at concerts, lectures, and tape-duplication sessions. It can be built into recorder case and uses either its own battery or the power source of the recorder—it draws only a matter of 200 microamperes in the timing mode and 4 milliamperes in the flashing mode.

Antilog function generator keeps VCO output linear

by J. A. Connelly and C. D. Thompson
Georgia Institute of Technology, Atlanta, Ga.

Accurate voltage control of oscillator frequency is crucial for such applications as electronic music synthesizers, filter test circuits, and phase-locked loops. In the voltage-controlled oscillator (VCO) described here, each 1-volt change in the control voltage changes the output frequency by one octave with a maximum deviation of ±0.4% over the entire audio range. This precision is achieved by temperature-compensation and buffering.

Circuit can be built with readily available parts, and the design equations allow adjustability and flexibility to meet a variety of specific needs. The total range of oscillation frequency can be shifted down one octave, for example, by doubling the capacitance of C_1 in the VCO.

This VCO is basically a relaxation oscillator: current source Q_5 charges low-leakage polystyrene capacitor C_1 until unijunction transistor Q_4 fires (at about 9 V); C_1 then discharges rapidly, and the cycle starts all over again. The sawtooth output voltage essentially results from the voltage across C_1 minus a couple of junction voltages, buffered by high-impedance MOSFET Q_2; by Q_3, which carries the current to fire Q_4; and by the unity-gain op amp. Most of the resistors limit transistor currents to safe levels.

The oscillation frequency is determined by the charging current into C_1. This current, which is the collector current from Q_{5B}, depends upon the control voltage because the base-to-emitter voltage V_{BE} in both halves of Q_5 is derived from the control voltage, thus,

$$I_C = \beta I_S \exp(qV_{BE}/kT)$$

where β is the short-circuit current gain, I_S is the reverse saturation current, kT/q is 0.026 per volt at 27°C, and V_{BE} is scaled from the control voltage V in a voltage-divider network:

$$V_{BE} = VR_{TC}/(R_{IN} + R_{TC})$$

Therefore, the collector current is given as a function of the control voltage by

$$I_C = \beta I_S \exp\left[\frac{qR_{TC}V}{kT(R_{IN} + R_{TC})}\right] = \beta I_S K^V$$

In this expression, the scale factor K is just a substitution that replaces several terms: that is,

$$K = \exp\left[\frac{qR_{TC}}{kT(R_{IN} + R_{TC})}\right]$$

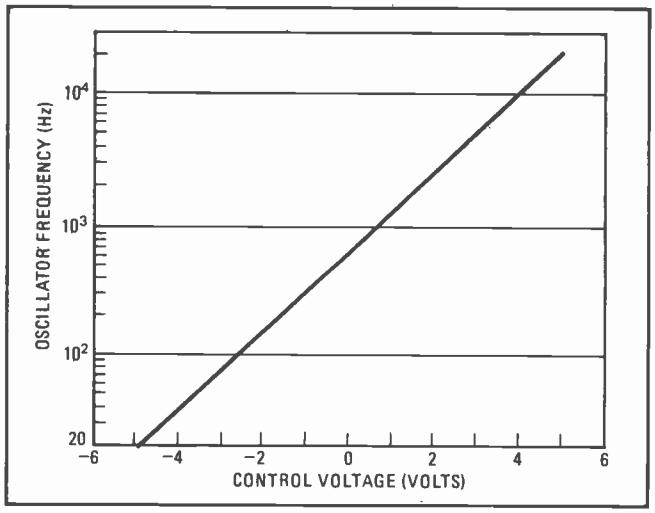
Current I_C is an antilog function (or exponential function) of voltage, and therefore the current source is called an antilog function generator.

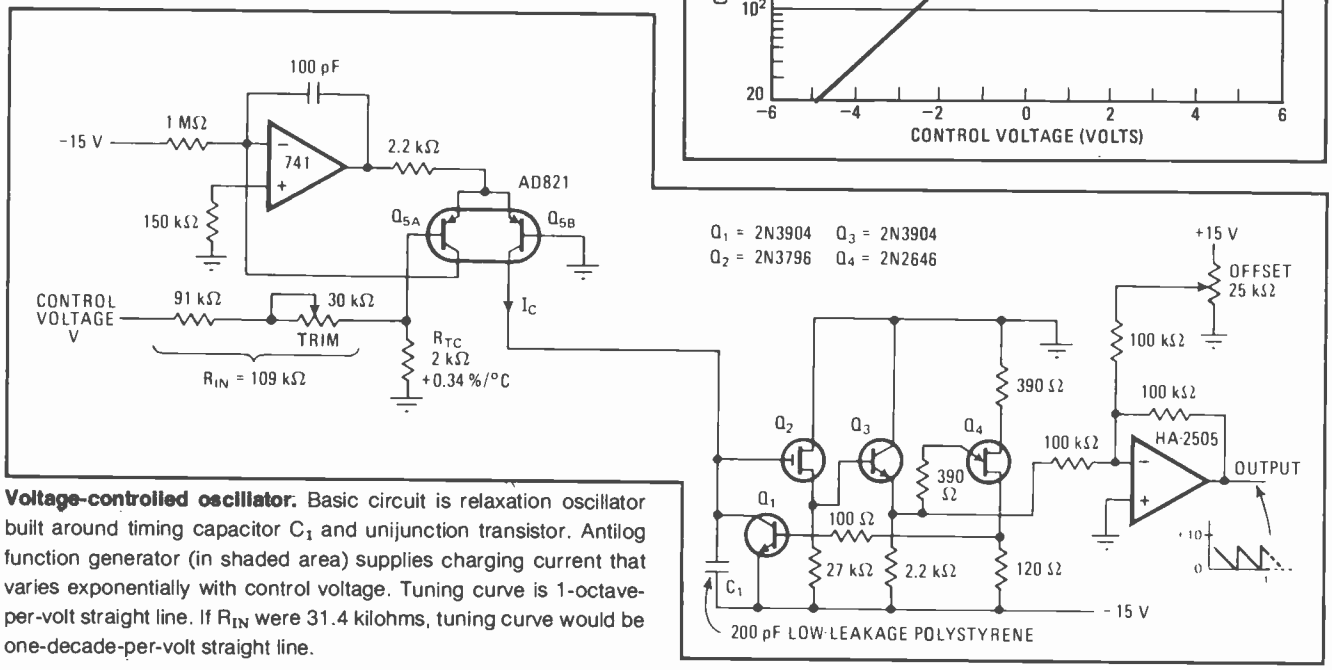
Because the frequency is directly proportional to I_C,

$$f \sim K^V = f_0 K^V$$

where f_0 is the free-running frequency (i.e., the oscillator frequency when control voltage V is zero). The frequency f_0 depends on the parameters of Q_5, the firing voltage of Q_4, and the capacitance of C_1.

The value of scale factor K is set by the resistors R_{IN}





Voltage-controlled oscillator. Basic circuit is relaxation oscillator built around timing capacitor C_1 and unijunction transistor. Antilog function generator (in shaded area) supplies charging current that varies exponentially with control voltage. Tuning curve is 1-octave-per-volt straight line. If R_{IN} were 31.4 kilohms, tuning curve would be one-decade-per-volt straight line.

and R_{TC} in the divider network. If K is 10, the oscillation frequency changes by one decade when V changes by 1 V. With the resistance values shown in the circuit diagram, however, K is 2, so the frequency changes by one octave when V changes by 1 V.

The temperature sensitivity of I_C is compensated by the temperature coefficient of thermistor R_{TC}, +0.34%/°C, which is equal in magnitude and opposite in sign to the effect of q/kT in the expression for K. Thus, scale factor K is independent of temperature if the thermistor and Q_5 have equal temperatures. To ensure this condition, the thermistor is mounted in thermal contact with the header of Q_5.

The tuning curve shows the experimental performance of the VCO. The maximum departure from the straight-line relationship is only ±0.4% over the audio-frequency range from 20 Hz to 20 kHz. Outside that range, the voltage control becomes less precise. □

Radiation monitor has linear output

by Paul Prazak, *Burr-Brown Research Corp., Tucson, Ariz.*, and Lt. William B. Scott, *Edwards AFB, Calif.*

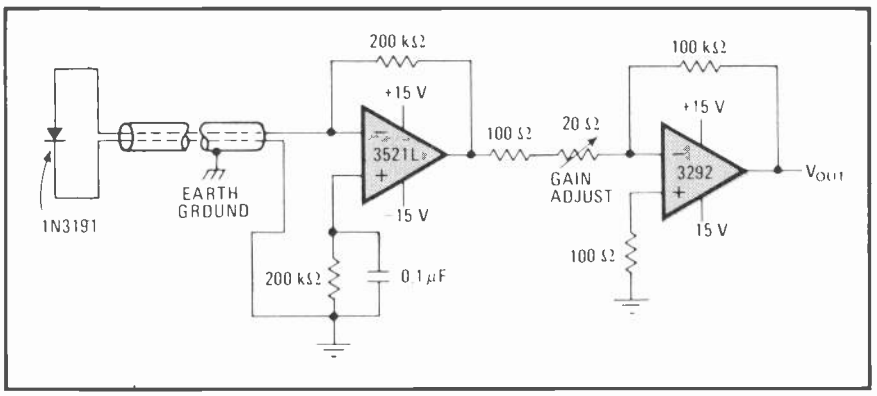
A commercial silicon diode can be used as a direct-reading detector of gamma rays and high-energy X rays in radiotherapy. Besides generating an output that is linearly proportional to the radiation intensity, the diode makes a small enough probe to map the radiation field accurately. The monitoring system of diode plus two operational amplifiers provides an output voltage that varies linearly from 0.1 volt to 10 V as the dose rate varies from 10 rads per minute to 1,000 rads/min.

The 1N3191 or other off-the-shelf diode is operated in a zero-bias short-circuit mode. Irradiation of the diode junction creates electrons and holes that are collected by the depletion gradient, producing a nanoampere current which is proportional to the intensity of the radiation.

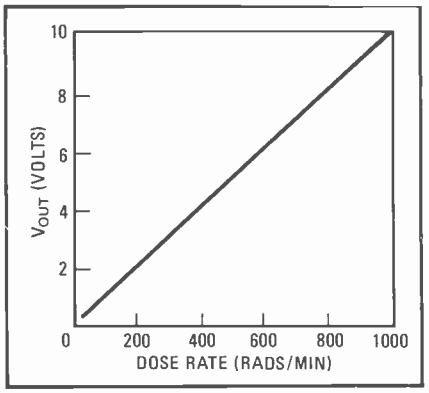
To amplify the small signal from the diode, a 3521L operational amplifier with low bias current (10 picoamperes maximum) and ultra-low offset voltage drift (±1 microvolt/°C maximum) is used. As shown in Fig. 1, the 3521L is connected in a current-to-voltage configuration where the inverting input appears as a virtual ground. This FET-input op amp delivers output voltages of 100 μV to 10 millivolts, which are well above the noise level. The 200-kilohm resistor between ground and the noninverting input serves to balance the amplifier, and the 0.1-microfarad capacitor stabilizes the amplifier by shunting out noise and preventing oscillations resulting from positive feedback.

An additional stage of gain amplifies the signal to the desired level. The offset-voltage drift of this stage must be extremely low because it is amplified along with the signal. Therefore the chopper-stabilized 3292 op amp, which has a maximum offset drift of only ±0.3 μV/°C is used here. The 100-ohm resistor again balances the inputs to the amplifier. The gain of this stage should be around 1,000; it is adjusted by means of the 20-ohm potentiometer so that an output voltage of 0.10 V to 10.00 V corresponds to a dose rate of 10 rads/min to 1,000 rads/min at the detector, as shown in Fig. 2.

The output voltage can be displayed on a 3½-digit panel meter, so that the numerals directly indicate radiation intensity. An alternative is to use an ultralinear voltage-to-frequency converter, an optical coupler, a counter, and a display to completely isolate the radiotherapy patient from the monitoring and recording system. An advantage of this approach is that the integrating input of the voltage/frequency converter would average out any high-frequency noise in the system. □



1. Dosage-rate meter. Commercial diode is detector in this highly accurate radiation monitor. Low-drift FET-input op amp amplifies detector current to usable level, and chopper-stabilized amplifier then provides additional gain while minimizing any error caused by ambient-temperature fluctuations. Gain is adjusted so that output voltage is 1% of incident radiation intensity in rads per minute; therefore voltage can be displayed on 3½-digit DVM for direct reading of dosage rate. Cost of parts for this monitor is about $90.



2. Linear response. Output voltage from monitor is linearly proportional to radiation intensity at diode. Over dosage rate range shown, total system error is less than 1%. Small size of diode probe permits accurate mapping of radiation field.

HP-45 calculator speeds rf amplifier design

by William J. Martin
Motorola Communications Division, Fort Lauderdale, Fla.

Important characteristics of an rf transistor amplifier can be evaluated quickly from the two-port scattering parameters of the transistor by using a Hewlett-Packard HP-45 scientific calculator. The calculations of stability, gain, and matching impedances use special programs for handling the complex terms in the amplifier analysis on the HP-45.

In using these programs, the designer should enter his data exactly as shown in the left-hand column and key it as shown in the center column. The result will appear as shown in the right-hand column after the last key in the center column is pressed.

The design of a 500-megahertz amplifier is carried through here to illustrate the procedure. This amplifier uses a Fairchild 2N2857 transistor with V_{CE} = 10 volts and I_C = 2 milliamperes; manufacturer's data give the S parameters in polar form (R,θ) as

$S_{11} = 0.394 \angle -158.7°$
$S_{12} = 0.048 \angle 63.5°$
$S_{21} = 2.084 \angle 79.2°$
$S_{22} = 0.816 \angle -20.4°$

The first step is to determine whether the transistor is stable under the given operating conditions. Calculation of the stability factor, K, requires complex quantity Δ, given by

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

The program for obtaining Δ on an HP-45 calculator is as follows

$S_{11\theta}$	↑	
$S_{22\theta}$	+	
S_{11R}	↑	
S_{22R}	X, →R, Σ+	
$S_{12\theta}$	↑	
$S_{21\theta}$	+	
S_{12R}	↑	
S_{21R}	X, →R, Σ −,	
	RCLΣ, →P	Δ_R
	↔	$\Delta\theta$

With the S parameters given above, this program yields

$\Delta = 0.251 \angle -164.8°$

Stability factor K is readily calculated from

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}S_{12}|} = 1.208$$

Because K has a positive value greater than unity, and S_{11} and S_{22} are less than unity, the 2N2857 is unconditionally stable; i.e., no source or load reflection coefficients exist that can cause instability. If the 2N2857 had not satisfied the stability criteria, the calculations would have been repeated for other transistors until a stable device was found.

To achieve the maximum possible power gain from this amplifier, the source and load impedances must be conjugately matched to the transistor. Therefore the next step in the amplifier design is to find these impedances. First a complex quantity, C_1, must be found. It is given by

$$C_1 = S_{11} - \Delta S_{22}^*$$

(The asterisk indicates a complex conjugate.) The HP-45 routine for C_1 is

$S_{11\theta}$	↑	
S_{11R}	→R, Σ+	
$\Delta\theta$	↑	
$S_{22\theta}$	CHS, +	
Δ_R	↑ ↓	
S_{22R}	X, →R, Σ−,	
	RCLΣ, →P	C_{1R}
	↔	$C_{1\theta}$

In this example, the value of C_1 is

$C_1 = 0.202 \angle -173.2°$

Another necessary quantity is B_1, given by

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 = 0.427$$

The input reflection coefficient ρ_{MS} that is required to conjugately match the transistor is

$$\rho_{MS} = C_1^* \left[\frac{B_1 \pm (B_1^2 - 4|C_1|^2)^{1/2}}{2|C_1|^2} \right]$$

The plus sign is used before the radical if B_1 is negative. The minus sign is used if B_1 is positive (as in this example). The value of ρ_{MS} here is

$\rho_{MS} = 0.719 \angle 173.2°$

To compute the output reflection coefficient that is re-

quired to conjugately match the output of the transistor, complex quantity C_2 must be found.

$$C_2 = S_{22} - \Delta S_{11}^*$$

The HP-45 routine for C_2 is completely analagous to that for C_1 and yields

$$C_2 = 0.721 \angle -22.3^\circ$$

Quantity B_2 is also required. It is given by

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2 = 1.448$$

The output reflection coefficient ρ_{ML} for conjugate match to the transistor is

$$\rho_{ML} = C_2^* \left[\frac{B_2 \pm (B_2^2 - 4|C_2|^2)^{1/2}}{2|C_2|^2} \right]$$

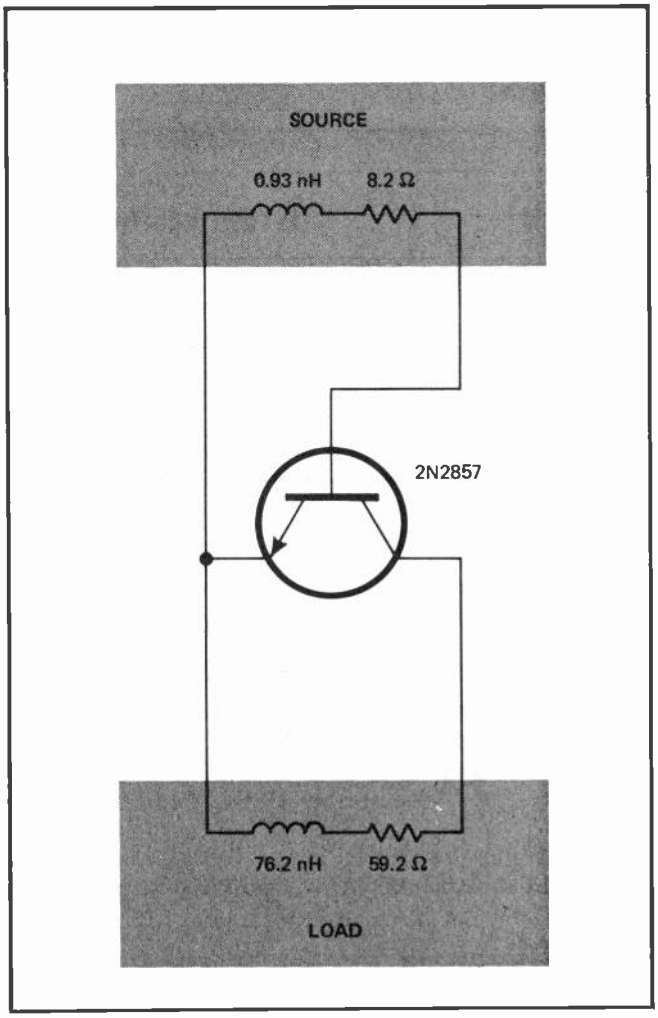
The plus sign is used for negative values of B_2, and the minus sign for positive values of B_2. Here

$$\rho_{ML} = 0.910 \angle 22.3^\circ$$

Reflection coefficients ρ_{MS} and ρ_{ML} can be converted to source and load impedances, respectively, by a graphical method (plotting on a Smith chart) or by the following HP-45 routine, which gives polar, series, and parallel forms for the impedance.

ρ_θ	↑		
ρ_R	→ R, 1, +, → P		
0	↑, 1, → R, Σ +, ↓, ↓		
ρ_θ	↑		
ρ_R	→ R, Σ −,		
	↓, ↓, RCL Σ +, → P,		
	↔, CHS, ↓, ÷,		
	↑, ↓, ↓, +, ↔, 50, X	MAG.	POLAR
	↔	θ	
	↔, → R,	R_S	SERIES
	↔,	X_S	
	↔, → P, ↓, ↑, ↓, COS,		
	÷, 50, X	R_P	PARALLEL
	↓, ↔, SIN, ÷, 50, X	X_P	

Matched circuit. Source and load impedances shown produce maximum possible power gain (13.6 dB) from 2N2857 operating at 500 MHz with V_{CE} = 10 volts and I_C = 2 milliamperes. Calculations of impedances and gain, as well as verification of amplifier stability, require only transistor S parameters and HP-45 scientific calculator.



The results, in series form, for this example are

$$Z_{source} = (8.19 + j\,2.91)\ ohms$$
$$Z_{load} = (59.23 + j\,239.15)\ ohms$$

Thus, the circuit shown in the accompanying diagram provides maximum possible power gain from this amplifier at the given values of frequency, voltage, and current.

The final step in the design analysis is to calculate the value of this maximum possible power gain. It is given in decibels as

$$G_{max} = \frac{|S_{21}|}{|S_{12}|} |K \pm (K^2 - 1)^{1/2}|$$

The plus sign is used in front of the radical if B_1 is negative. The minus sign is used if B_1 is positive, In this example the minus sign is used, and

$$G_{max} = 13.6\ dB$$

for a Fairchild 2N2857 transistor operated at 500 MHz with V_{CE} = 10 V and I_C = 2 mA.

This brief presentation has shown HP-45 routines for only the complex quantities Δ, C_1, and Z. Routines in the same format for the other quantities discussed (K, B_1, B_2, ρ_{MS}, and ρ_{ML}) are available from the author. Also available are routines for ρ_{MS}' and ρ_{ML}'. Quantity ρ_{MS}' gives the complex source impedance once the complex output impedance is known (from constant gain circles if a power gain other than G_{max} is desired). Quantity ρ_{ML}' gives the complex output impedance once the complex input impedance is known (e.g., for best noise match). □

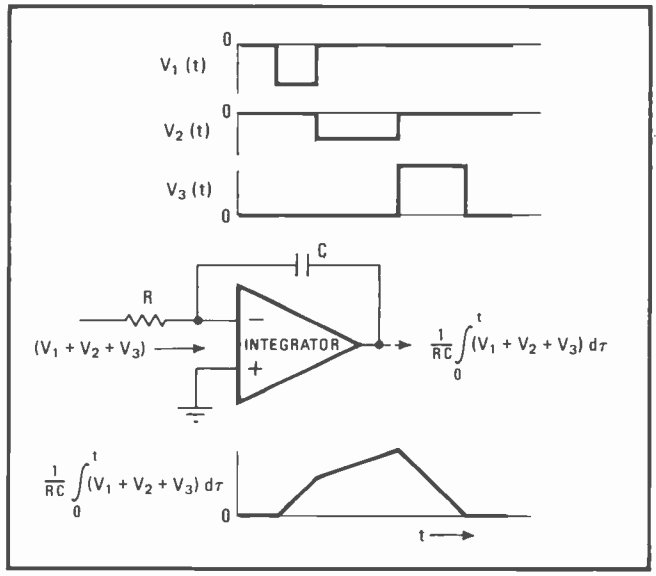
Waveform is synthesized from linear segments

by E. D. Urbanek
Bell Telephone Laboratories, Murray Hill, N.J.

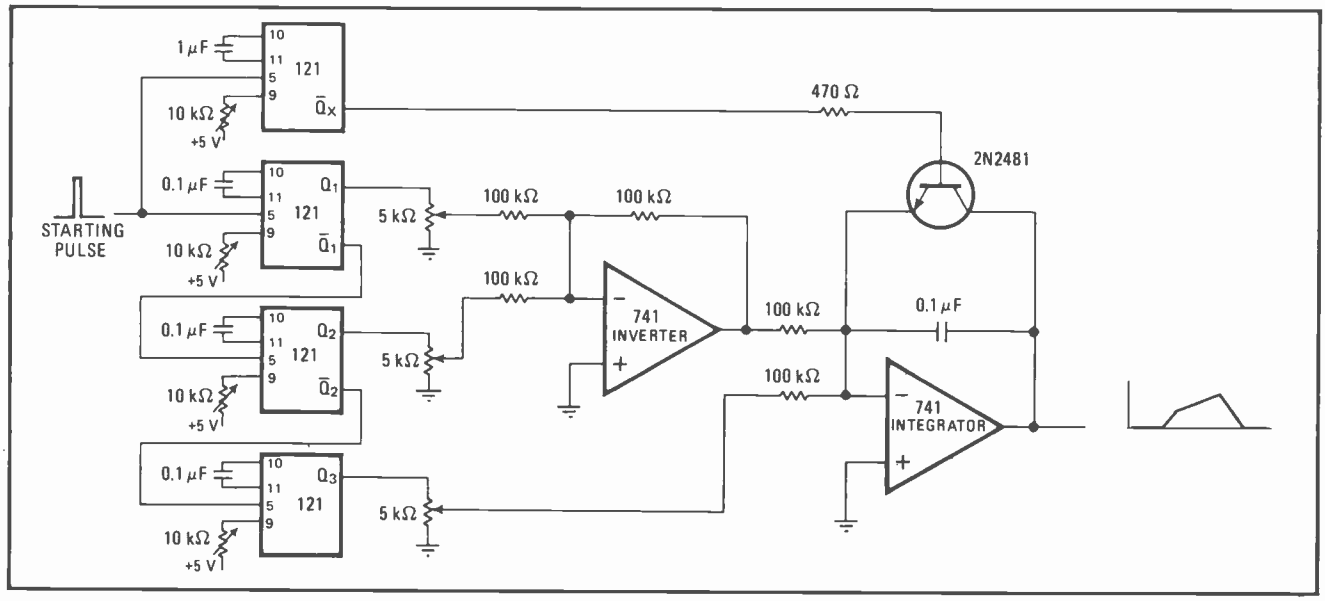
Just as a curve can be approximated by a series of straight lines, so can a waveform be approximated by a succession of voltage ramps. The voltage ramps may be the output of an integrator driven by a succession of rectangular pulses of various amplitudes and durations. Figure 1 shows how the integration of three such pulses produces three sequential ramps to yield a novel wave shape. The amplitude and polarity of each pulse determine the slope and direction of the corresponding ramp, and the width of the pulse determines the length of the ramp. The output voltage function can be made to resemble a curve if enough pulses and ramp segments are used.

A function generator that synthesizes waveforms in this manner is used as a control for automatic-gain-control circuits and for sweep generation. As shown in Fig. 2, it contains type 121 one-shot multivibrators to generate the pulses that are to be integrated, a 741 operational amplifier connected as an inverter to change the polarity of pulses when necessary, and another 741 op amp connected as an integrator. The 2N2481 transistor prevents drift.

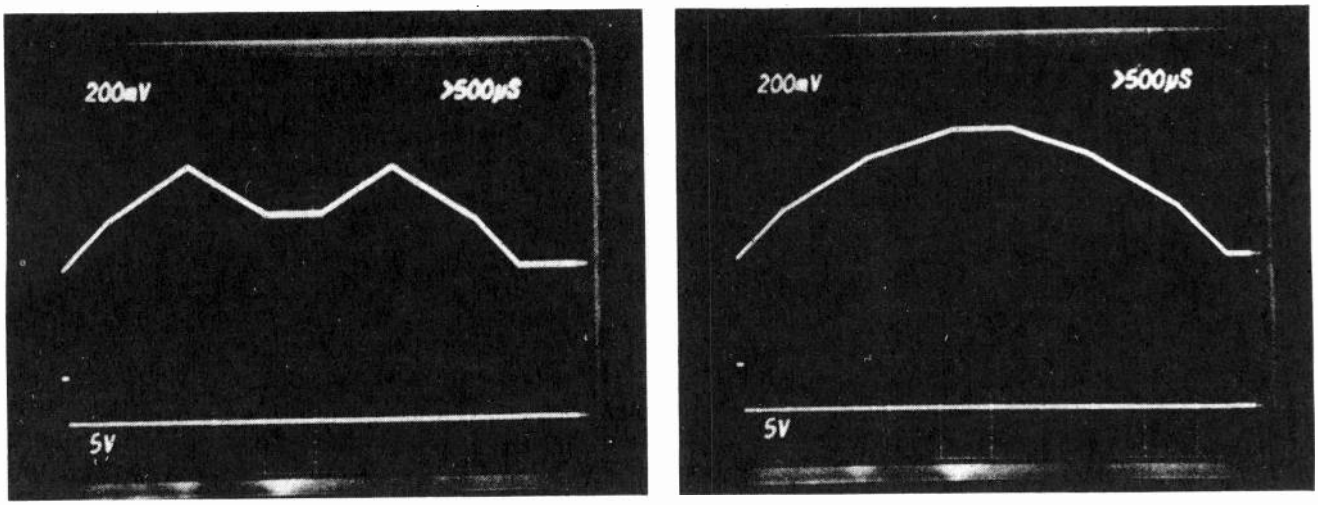
The one-shot units are arranged in a series so that the complementary output ($\bar{Q}$) of the first unit serves as the trigger for the second unit, and so forth. This arrangement produces a sequence of positive pulses. The duration of each pulse is determined by the timing resistor and capacitor of its one-shot, and the amplitude of each pulse is set by the potentiometer at the output of the one-shot. Each positive pulse can be connected directly to the integrator to produce a ramp with negative slope, or it can be connected through the inverter and thence to the integrator to produce a ramp with positive slope.



1. Waveform generation. Integration of sequential rectangular pulses produces sequential voltage ramps that make up output waveform. Amplitude, polarity, and duration of pulses determine the slope, direction, and length of the ramps.



2. Circuit. Function generator uses one-shot multivibrators to supply series of pulses to op amp connected as integrator. Pulse polarity can be reversed by op amp connected as inverter. Complementary output from each pulse generator triggers next pulse in sequence, producing continuity in wave shape. Pulse widths are set by RC time constant for each one-shot, and pulse amplitudes are set by potentiometers.



3. Waveforms. Scope traces generated by seven-segment function generator. Maximum voltage on these traces is about 0.5 volt, and duration of traces is about 4 milliseconds. Traces could be brought down to zero-voltage level smoothly, by sloping segments, or abruptly, by use of transistor to short-circuit integrating capacitor. Trace on right here shows that just a few segments suffice to approximate a curve.

An additional one-shot unit and the transistor are used to form an anti-drift control. The complementary output ($\overline{Q}_x$) of this one-shot is used to drive the transistor, which discharges the 0.1-microfarad integrating capacitor. With no input pulse applied, the transistor keeps the capacitor discharged. Holding the integrator output at zero in this way prevents integration of any offset voltages. When an input pulse is applied to start the function generator, ($\overline{Q}_x$) is driven off and the transistor releases the capacitor. The off time of ($\overline{Q}_x$) may be adjusted to coincide with the total on time of the function generator, or it may be adjusted to terminate the waveform at any point during the on time.

Scope traces of seven-segment waveforms are shown in Fig. 3. The voltage level remains constant (because there is no input pulse to the integrator) between the end of the seventh segment and the retriggering of the start pulse. The maximum voltage on each trace is about 0.5 volt, and the total duration of a trace is about 4 milliseconds.

In applications where a wide range of ramp slope is required, the potentiometer attenuators can be eliminated, and the input resistors on the inverter and integrator can be made variable. This increases inverter gain and allows control of both voltage and time constant of the integrator for adjusting the slopes. □

Direct-reading converter yields temperature

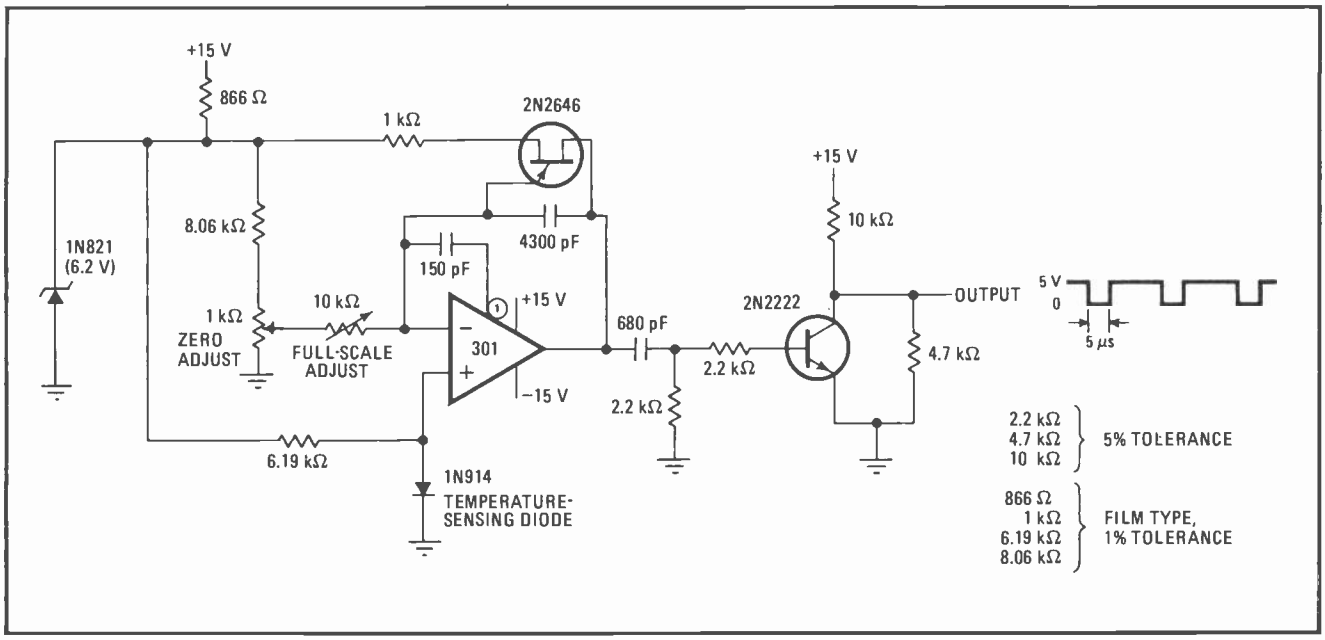
by James Williams and Thomas Durgavich
Massachusetts Institute of Technology, Cambridge, Mass.

It's possible to convert temperature accurately to a numerically equivalent frequency for direct display or for instrumentation. The circuit described here uses an 1N914 temperature-sensing diode to provide 0.1°C resolution from 0°C to 100°C, with accuracy of ±0.3°C over the entire range.

The 301A operational amplifier is set up as an integrator. The 150-picofarad capacitor from the inverting input to pin 1 provides feed-forward compensation for high slew rate. The 2N2646 unijunction transistor resets the integrator when the 4300-pF capacitor charges to about −10 volts. The 1N821 temperature-compensated diode provides a voltage reference that determines the firing point of the unijunction transistor, provides stable zero and full-scale references, and sends a 1-milliampere current through the 1N914 temperature-sensing diode. The 2N2222 transistor and its associated components provide an output pulse that is compatible with transistor-transistor logic.

In operation, the circuit functions as a voltage-to-frequency converter. The voltage at the wiper arm of the 1-kilohm potentiometer is integrated until the transistor's firing point is reached. When the transistor fires, it resets the capacitor. The frequency of oscillation is related to temperature because the diode voltage biases the integrator via the noninverting input. The only variable voltage available to the amplifier is the temperature-dependent (−2.2 millivolts per °C) potential from the 1N914 diode. To adjust the circuit, put the diode in a 100°C environment and turn the 10-kilohm potentiometer till the output frequency is 1,000 hertz. Then put the diode in a 0°C environment, and turn the 1-kilohm potentiometer for 0 Hz out. This procedure must be repeated two or three times, until the adjustments cease to interact. Once the circuit is adjusted, its output frequency is 10 times the sensed temperature within 0.3°C from 0° to 100°C. For example, if the temperature is 37.5°C, the meter will read 375 Hz.

The output frequency can be counted by TTL count-



Temperature-to-frequency converter. Frequency of relaxation oscillator varies with temperature-dependent voltage across 1N914 diode. Over 0°C-to-100°C temperature range, frequency changes linearly from 0 to 1,000 Hz. Therefore frequency meter at output can show temperature directly. Accuracy is ±0.3°C. Excellent performance and low cost (less than $5 for parts) make this circuit outstanding.

ers and a 1-Hz square wave. The 1-Hz square wave can be fed to the base of the 2N2222 through a 2.2-kilohm resistor, and the resultant gated pulses at the output can then be fed to TTL counters. □

One NOR gate starts shift-register loop

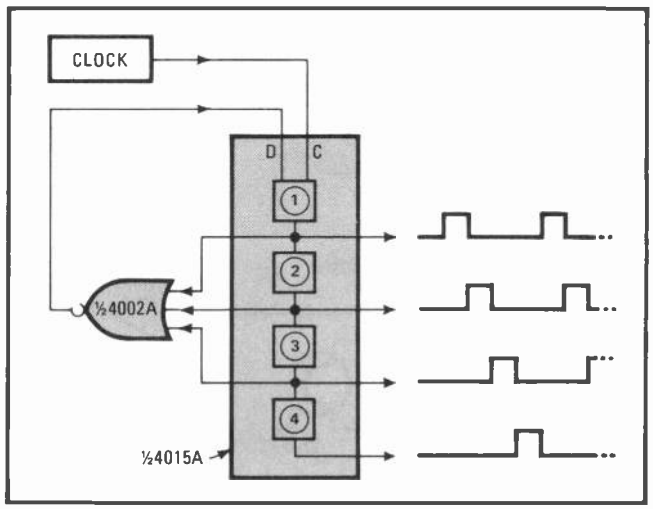
by Jean-Pierre Dujardin
Ohio State University, Columbus, Ohio

A circulating shift register with a single logic 1 in the loop is required in cyclic-triggering operations such as sampling transducers in time-sharing telemetry. Systems for starting this type of circuit are often complex, but the arrangement shown here simply uses a NOR gate with the four-stage shift register.

As the waveforms show, the output terminals of the 4015A shift register go high in a continuing sequence from stage one through stage four and then back to stage one again. The 4002A three-input NOR gate starts this operation and keeps it going.

The input terminals of the NOR gate are connected to the first three output terminals of the shift register. When these terminals are at logic 0, the output terminal of the gate is at logic 1, which is brought to the data input terminal (D) of the register. The next clock pulse transfers the logic 1 at D into the first stage of the register. When at least one of the inputs to the gate is a logic 1, the output from the gate is a 0, which is presented to the register input. Thus, after a maximum of three clock pulses, a single 1 is circulating.

This circuit requires no external timing to introduce the single 1 into the loop and no resetting. If external noise introduces errors, they are automatically corrected. Extension of the system to more than four shift-register stages is straightforward: outputs from all but the last stage are fed into a NOR gate that, in turn, feeds the D input of the first stage in the register. □



C-MOS ring circuit. Arrangement of NOR gate and four-stage shift register provides a pulse output that circulates to each of the output terminals in sequence, moving from one stage to the next as the clock cycles. The two C-MOS ICs determine performance level.

Comparator IC forms 10-bit a-d converter

by James M. Williams
Massachusetts Institute of Technology, Cambridge, Mass.

This analog-to-digital converter uses an integrated-circuit comparator to provide an accurate 10-bit representation of an analog signal in 1 millisecond or in 100 microseconds, depending on the clock rate. The circuit, which costs only $13 to build, is accurate over the temperature range from 15°C to 35°C.

In addition to low cost, advantages include low parts count, low power drain, immunity from power-supply fluctuations, and capability to transmit data over two wires. Disadvantages include the necessity for a stable clock (although one clock can serve many converters), and dependence upon a capacitor for stability. The circuit may be sensitive to noise, but a small RC filter can be used for noise suppression.

Operation over extended temperature ranges is not recommended. If such use is necessary, however, capacitor C (Fig. 1) should consist of a 0.03 silver-mica capacitor in parallel with a 0.01 polystyrene capacitor.

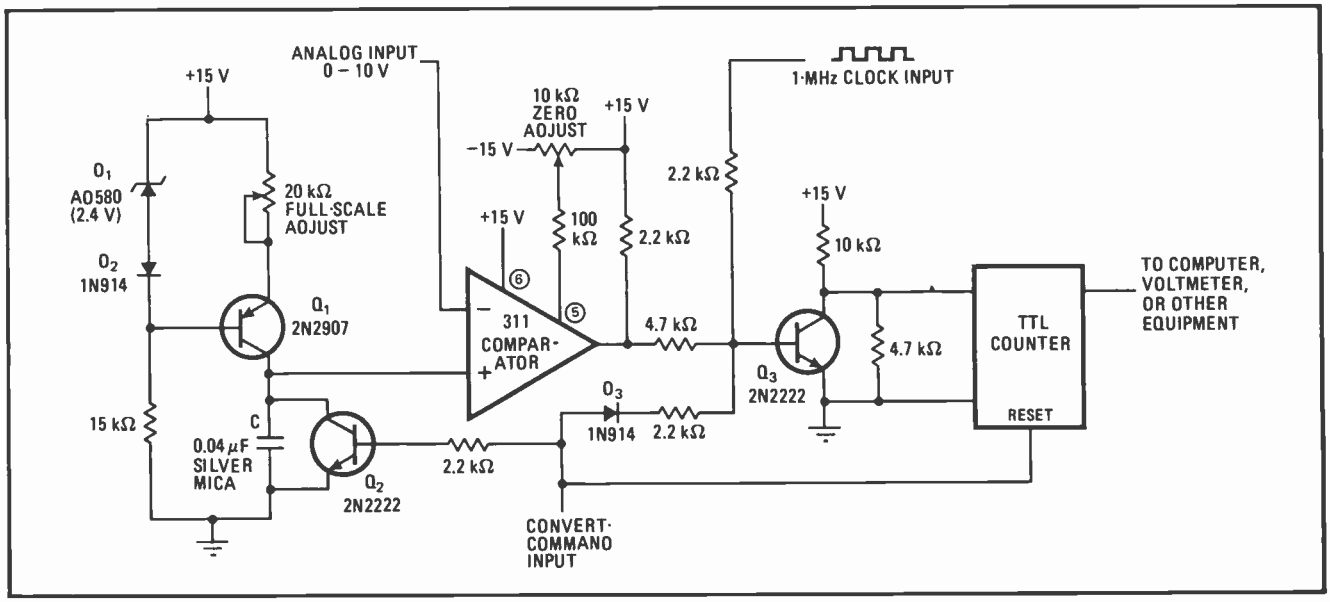
The digital output from this converter is the number of clock pulses counted during the time required for the capacitor to charge up to the level of the analog voltage. As the circuit diagram in Fig. 1 shows, the analog input can be any voltage from 0 to 10 V. This voltage and the voltage across the capacitor are compared in the IC. As long as the analog voltage is greater than capacitor voltage V_C, the comparator allows a counter to count clock pulses. But when V_C reaches the level of the analog voltage, the counting is stopped. The total number of pulses counted is a measure of the analog input. The charging rate of the capacitor is set so the pulse count is proportional to the voltage; e.g., 1,000 pulses corresponds to 10 V.

The detailed operation of the a-d converter in Fig. 1 is straightforward. Transistor Q_1, diodes D_1 and D_2, and the resistors constitute a constant-current source for charging capacitor C. The 2.4-V zener D_1 stabilizes the source against power-supply variations, and the voltage drop across D_2 matches the emitter-to-base voltage in Q_1, despite any temperature changes.

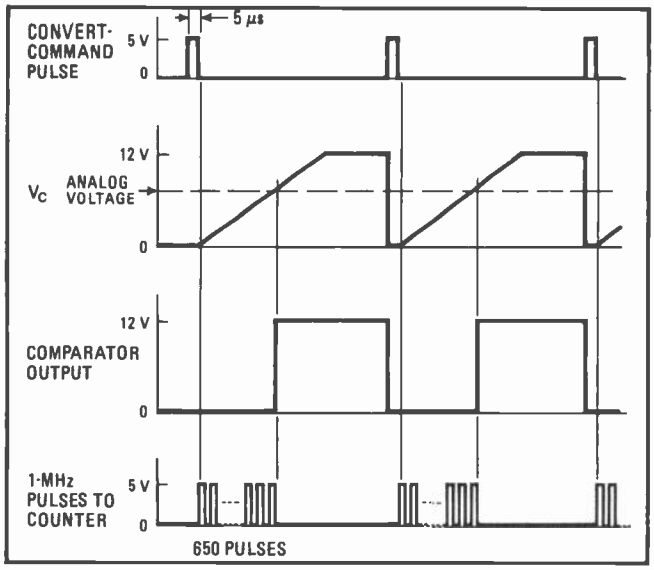
The type 311 IC compares the input voltage to the capacitor voltage V_C and controls transistor Q_3. The input voltage is applied to the inverting (–) input of the comparator, and V_C is applied to the noninverting (+) terminal. At quiescence, V_C is about 12 V, so the 311 output is high. This high signal keeps Q_3 on, so that the data line into the counter is grounded and no clock pulses are counted.

When a convert-command pulse is applied, transistor Q_2 turns on and discharges C, so that the 311 output goes to zero. Diode D_3 and the 2.2-kilohm resistor keep Q_3 on, however, so that no pulses can be counted during the convert command. On the falling edge of the command pulse, Q_1 begins to charge C linearly, and D_3 ceases to hold Q_3 on.

Now, because the output of the comparator is low, the clock pulses can turn Q_3 on and off, so that clock-frequency pulses are delivered to the counter. The combination of the 10-kilohm resistor and the 4.7-kilohm resistor makes the level of these pulses compatible with



1. A-d converter. Integrated-circuit comparator permits counting of clock pulses only while capacitor is charging up to level of analog voltage. With 1-MHz clock shown, conversion of 10-volt analog voltage to 10 bits (1,000 counts) takes 1 millisecond. If clock rate is 10 MHz, and C is 0.004 μF, conversion is accomplished in 100 microseconds.



2. Timing diagram. For an analog voltage of 6.5 V as in this example, 650 pulses are counted while capacitor charges up to turn off comparator output. Convert commands can be given at any rate up to 1 kHz for circuit as shown in Fig. 1.

transistor-transistor logic (TTL) in the counter circuit.

When V_C charges up to the level of the input voltage, the 311 output goes high again, which turns on Q_3 and grounds the data line so that no more pulses are counted. Fig. 2 shows the timing diagram for the converter operation.

To calibrate the counter, a 10-v signal is applied at the input, and the 20-kilohm potentiometer is adjusted so that 1,000 pulses appear at the counter for each conversion command. Then a 0.01-v signal is applied, and the 10-kilohm pot is adjusted so that 1 pulse is counted for each conversion. The unorthodox voltage-offset adjustment for the comparator corrects for incomplete discharge of C; the minimum voltage across C is V_{CE}(sat) of Q_2.

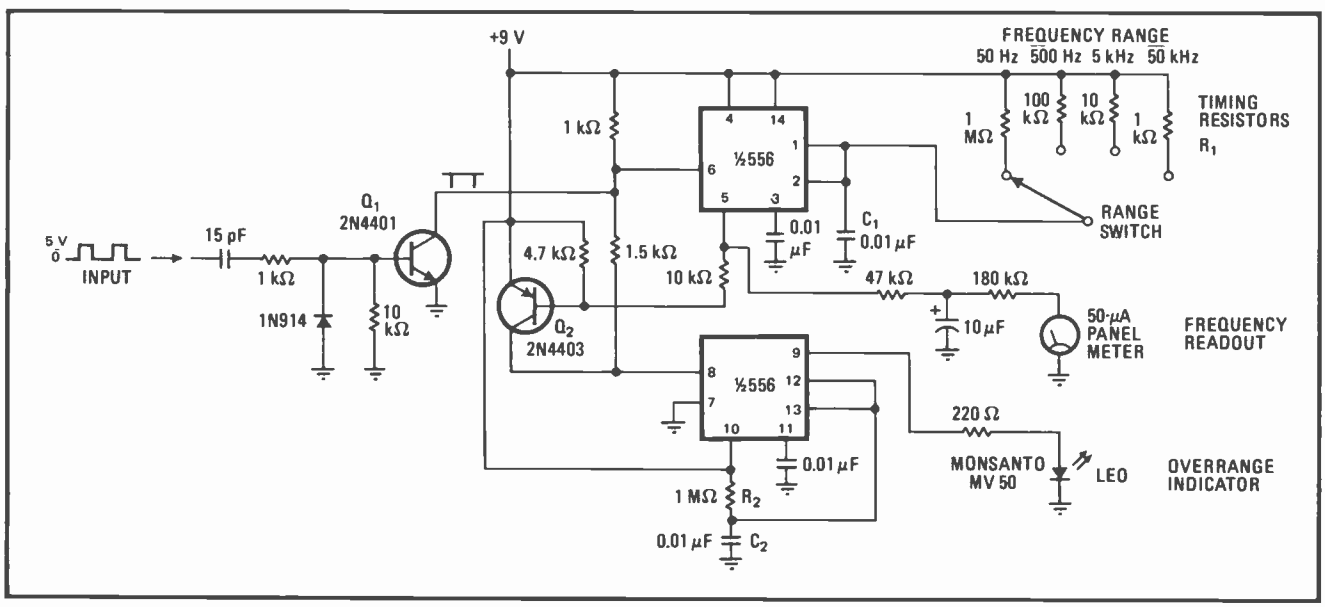
The circuit in Fig. 1 can convert 10 bits (i.e., count 1,000 pulses) in 1 ms. For conversion in 100 μs, the clock frequency must be 10 megahertz, and C must be 0.004 microfarad. Conversion commands can then be given at rates up to 10 kilohertz. □

Overrange indicator can enhance frequency meter

by F. E. Hinkle
The Applied Research Laboratories, University of Texas, Austin, Texas

By making use of a 556 integrated circuit, which is composed of two 555 timers in a single package, an overrange indicator can be economically added to an analog frequency meter. A 555 can be used alone as a monostable multivibrator that is triggered by the frequency to be measured. To provide unambiguous measurements, however, the meter described here uses a second timer to flash a warning light whenever the input exceeds the maximum frequency setting. Although the technique of using monostables in analog frequency meters is not new, the use of new circuit developments makes the design economical and easy to implement.

When the range switch on this meter is set to the 50-hertz range, any input frequency from near dc to 50 Hz causes a panel meter to read correctly; e.g., a frequency of 42 Hz produces a meter reading of 42 microamperes. However, the meter reading is incorrect when the input



Unambiguous. Addition of overrange indicator to analog frequency meter warns when switch is set to wrong frequency range. Transistor Q_2 allows input signal to trigger LED monostable whenever input frequency is greater than meter range. Inexpensive and reliable circuit shown is useful from near dc to well over 20 kHz.

frequency exceeds 50 Hz, and therefore a light-emitting-diode overrange indicator flashes. If the range switch is then moved to a setting higher than the frequency, the LED stops flashing and the meter again indicates correctly. For example, a 300-Hz signal would be measured on the 500-Hz range, and the meter would show 30 microamperes.

In the meter diagramed here, the upper portion of the circuit measures the frequency and has the 50-μA panel meter as its readout. The lower portion provides the overrange indication and has the LED as its warning light. These two portions of the circuit are driven by a common input.

The input signal is a rectangular pulse train; the pulses are differentiated to produce the negative spikes that are needed to trigger the timer. For a sine-wave or sawtooth input signal, a Schmitt trigger might be used to generate the negative impulses.

When pin 6 of the frequency-measurement monostable is triggered, pin 5 goes high. It stays high and delivers current for a time equal to $1.1R_1C_1$. This positive output pulse appears once for every cycle of the input frequency (unless the trigger impulse arrives while the output at pin 5 is already high). The current pulses, smoothed by the 10-microfarad capacitor, provide an average value that is shown on the microammeter.

At low frequencies, the output pulses are well separated, so the average current is low. At higher frequencies, however, they are closely spaced and approach a duty factor of about 95% at the upper frequency limit set by the range switch. Average current thus increases as the frequency increases. Resistors in the output circuit are chosen so that the average current is 50 μA at the maximum frequency in each range.

If the input frequency exceeds the meter range, a trigger spike arrives while the output is already high. As a result, that input cycle is not counted, so the frequency meter indication is erroneous.

To warn that trigger impulses are arriving while pin 5 is high, pin 5 is also connected to the base of pnp transistor Q_2. When pin 5 is low, Q_2 conducts and holds pin 8 high, thus preventing the warning-indicator monostable from being triggered. But when pin 5 is high, Q_2 is turned off; a negative input spike that reaches pin 8 therefore can trigger an output from pin 9 that flashes the LED. The duration of the flash is $1.1R_2C_2$. □

Pulse-frequency doubler requires no adjustment

by Thomas McGahee
Don Bosco Technical High School, Boston, Mass.

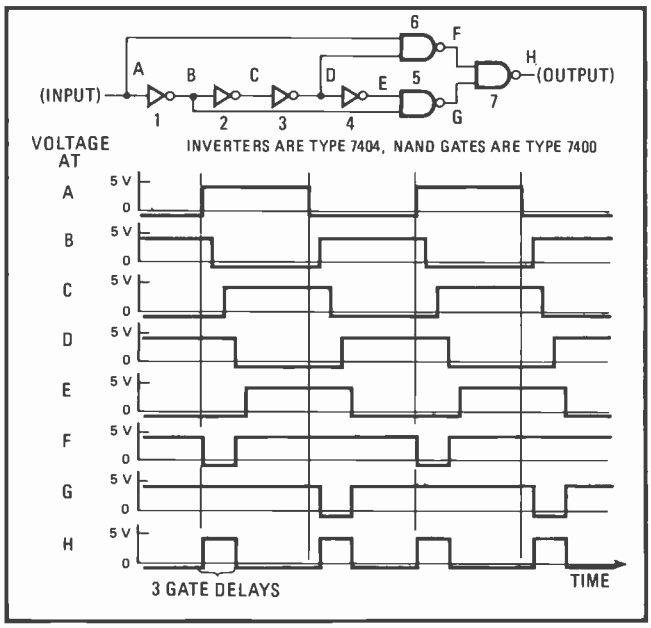
Sometimes a frequency doubler is needed in a digital system, and unfortunately most doubler circuits have to be adjusted for a particular operating frequency. However, this circuit, which has operated successfully in a specially designed divide-by-N counter, requires no adjustment over a range from near dc to 10 megahertz.

When a signal pulse passes through the circuit, each inverter introduces a small delay, typically of 20 nanoseconds, in addition to inverting the pulse. For example, the signal at point D inverts 60 ns after the input signal at point A has inverted; thus, gate 6 continues to have high signals at both of its input terminals for 60 ns after the input at point A changes from low to high. As a result, the output from gate 6 (i.e., point F) will go low for 60 ns after a positive-going transition at the input to the circuit.

Somewhat the same thing occurs at gate 5, except that it develops a 60-ns low output after a negative-going transition at the input. In the circuit diagram, inverters 1, 2, and 3 all serve double duty in producing these 60-ns low pulses at points F and G. This design reduces the number of gates needed.

The pulses from gates 5 and 6 are fed to the terminals of gate 7, which produces a positive pulse 60 ns wide every time either one of its input terminals goes low. Since one terminal goes low on the leading edge of each input pulse at point A, and the other terminal goes low on the trailing edge of each input pulse at A, the frequency of the output pulses at point H is twice the frequency of the input pulses at point A.

The output is in the form of positive pulses that are 60 ns wide. There is a 20-ns difference in the spacing between successive output pulses because the portion of the circuit that comprises the negative-going edge-detector has one more inverter stage than the positive-going edge-detector section does. This slight asymmetry is noticeable only at the highest frequencies. If particularly slow input signals are used, it is a good idea to place a Schmitt trigger just before the input. □



Frequency doubler. Propagation delays through inverters cause NAND gates 5 and 6 to go low for 60 nanoseconds following the rising and falling edges, respectively, of input pulse. Therefore output goes high twice as often as input.

Buffer keeps noise from triggering thyristor

by L. R. Rice
*Westinghouse Semiconductor Division, Youngwood, Pa.**

Certain shortcomings in passive noise-rejection networks have led to development of an active circuit designed to prevent false triggering of thyristors. Such undesired firing can occur when noise transients cross the thyristor gate conductors, and can produce fluctuations of load power, oscillations in control circuits, and equipment damage. The offending pulses usually arise from reactive-load energization or de-energization, such as the discharge of a capacitor or the switching of a relay.

In the field, passive networks that discriminate against both signal and noise, such as those shown in Fig. 1, are often used, but they are impractical at times and some application problems simply cannot be solved with these techniques. Therefore an active circuit, consisting of a buffer connected between the trigger source and the thyristor gate, is needed.

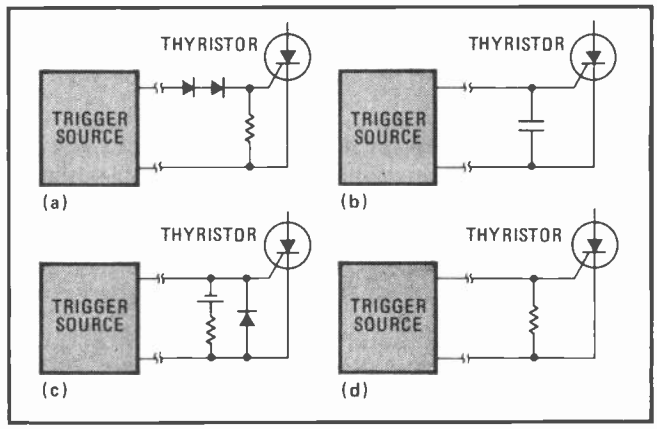
As shown in Fig. 2, this buffer consists of an RC integrating circuit, a comparator, and a pulse generator. An incoming voltage, either signal or noise, charges 0.02-microfarad capacitor C through resistor R. The 2N697 comparator amplifier turns on when the capacitor voltage reaches the threshold value equal to the sum of the voltage drops in diode D_2, the base-to-emitter junction, and zener diode D_3. This threshold voltage is given by

$$V_{TH} = V_{diode} + V_{BE} + V_{zener}$$
$$= (1.0 + 0.45 + 6.0)\ volts$$
$$= 7.45\ volts$$

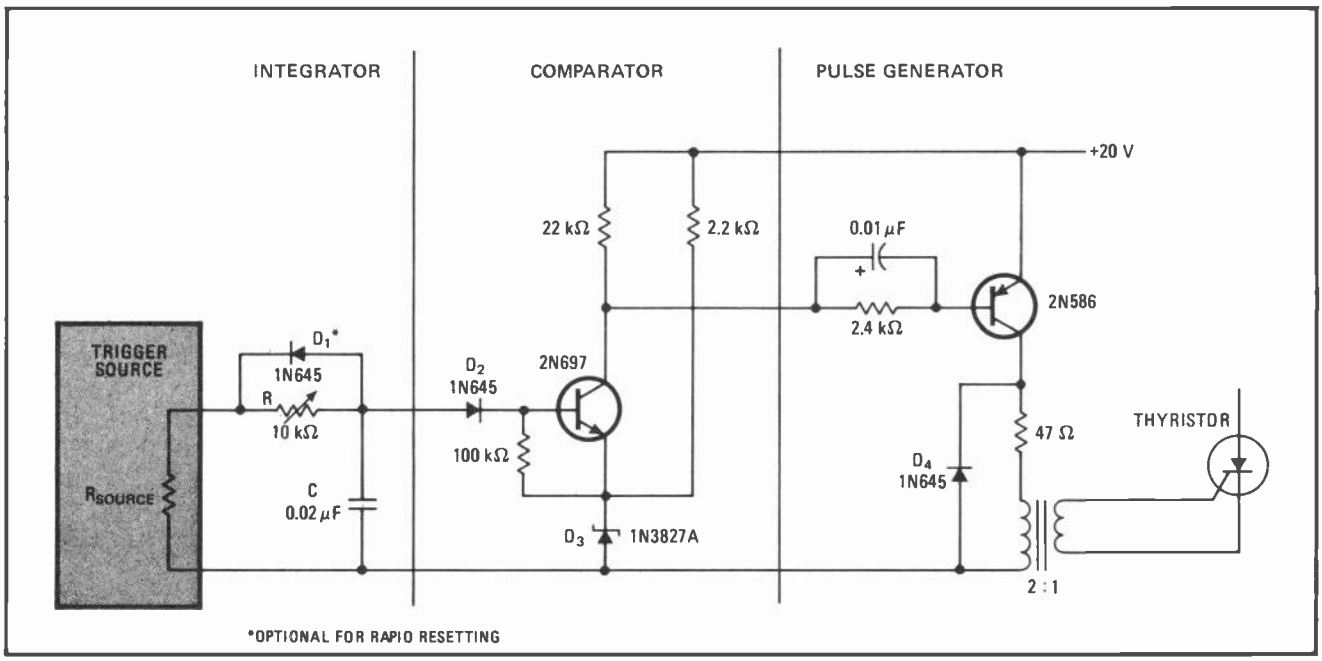
When the capacitor voltage reaches this value and turns on the comparator, the 2N586 pulse generator starts to conduct and fires the thyristor.

Variable resistor R is adjusted so that the time constant RC is large enough to prevent noise pulses from charging C to threshold. For example, if the noise ambience can be represented by a 50-volt pulse of 1-micro-

*Now with White-Westinghouse Corp., Mansfield, Ohio.



1. Quick fixes. Noise in thyristor gate lead is sometimes suppressed by one or another of these means: (a) diodes raise threshold voltage; (b) capacitor shunts high frequencies; (c) saturated diode reverse-biases gate; (d) resistor decreases gate sensitivity.



2. Buffer. Integrator prevents false triggering of thyristor by discriminating between genuine trigger signals and noise transients. Trigger signal must last long enough to charge capacitor C to the threshold voltage of the comparator, which then turns on the pulse generator. Variable resistor R permits adjustment of the charging-time constant so that noise pulses cannot charge C to the comparator's threshold.

second duration, the value of R that would allow C to just reach threshold in 1 μs is found from the charging equation

$$V_C = V_0 - V_0 exp(-t/RC)$$
$$7.45 = 50 - 50\, exp(-1/0.02R)$$
$$exp(-1/0.02R) = 0.85$$
$$R = 300\ ohms$$

Therefore, to prevent the 50-v/1-μs noise pulse from firing the thyristor, R is made a bit larger than 300 ohms.

After the noise pulse has ended, capacitor C discharges back through R, or through diode D_1 if quicker recovery is required.

A signal voltage from the trigger source charges up the capacitor just as a noise pulse does, but the signal duration is made long enough for the capacitor to reach threshold. If the trigger signal is 12 volts, for example, and R has been set for 300 ohms, then the signal must be applied for at least a time duration t (in microseconds) given by

$$7.45 = 12 - 12\, exp[-t/(300 \times 0.02)]$$

or t = 6 μs. Thus the 12-v trigger signal must last for 6 μs to fire the transistor.

Because this circuit delays the normal firing point to achieve noise rejection, timing in the trigger source may require adjustment if not controlled by feedback from the load. □

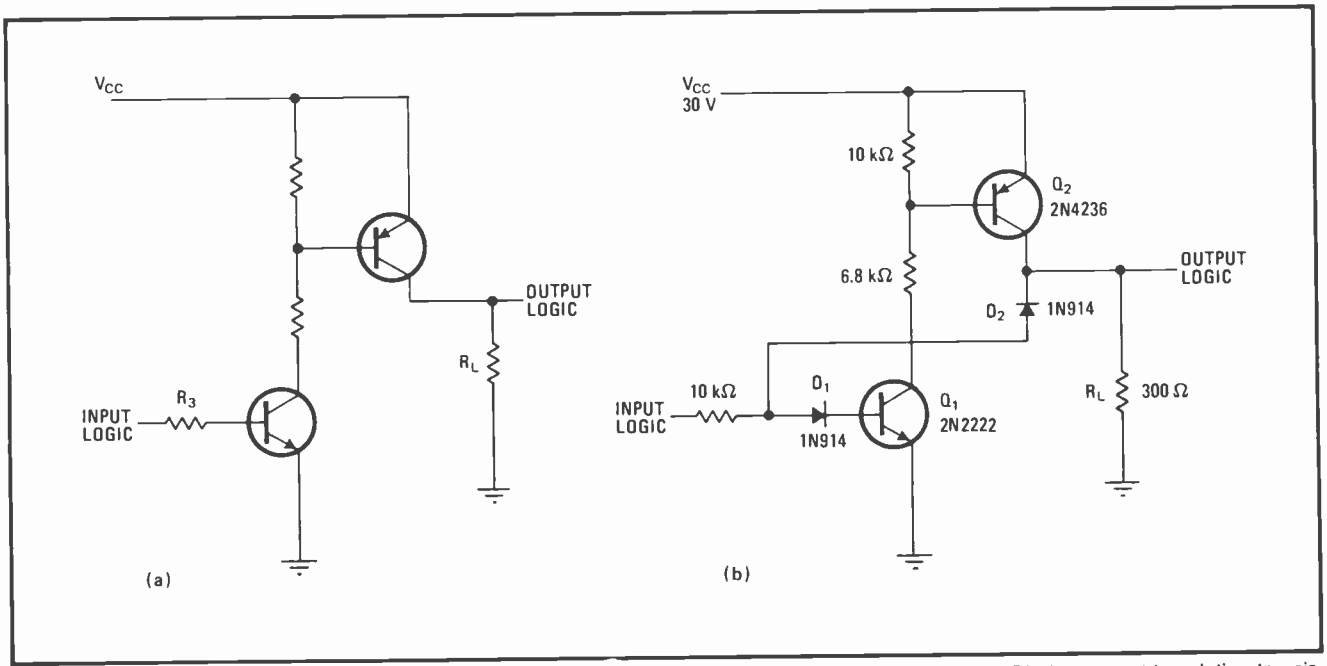
Two diodes protect logic-level translator

by P. R. K. Chetty
Indian Scientific Satellite Project, Bangalore, India

A level translator is used to interface between two circuits that operate at different logic levels. But the translating transistor (or level-up transistor) is often burned out when its load is accidentally short-circuited to ground. The addition of two diodes to the conventional level-up circuit can protect the transistor. Even a transistor that operates at 30 volts (as well as those meeting lower voltage requirements) can be safeguarded by the circuit modification described here.

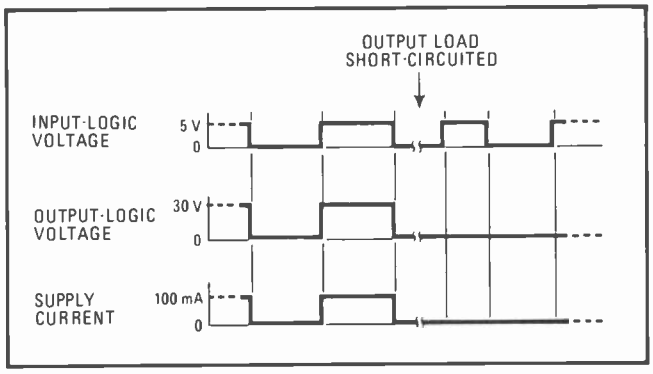
The conventional translation circuit (or logic level-up circuit) is shown in Fig. 1(a), and a modified version with two protection diodes added is shown in Fig. 1(b). The component values shown are chosen to provide a normal load current of about 100 milliamperes. In normal operation, when the input logic is high (logic 1), diode D_1 is forward-biased; Q_1 is turned on, and therefore Q_2 is turned on. Diode D_2 is reverse-biased, so the output-logic voltage across the load is nearly V_{CC}. When the input logic is low (logic 0), the transistors are turned off, and the output logic is zero.

If the output load is shorted to ground when the input is a logic 1, the anode of D_1 is above ground only by the amount of the forward-voltage drop through D_2. This voltage is not great enough to let Q_1 conduct because a voltage of at least two diode drops, V_{D1} and V_{BE}, would be required to turn on Q_1. Therefore Q_1 is turned off, and, as a result, transistor Q_2 is turned off too, which prevents it from conducting a destructive current straight to ground. The circuit remains shut down as



1. Protection. Conventional logic-level translator shown in (a) is modified by addition of two diodes in (b). Diodes protect translation transistor Q_2 from destructive current that would otherwise flow if load resistor were short-circuited. Diodes turn off both transistors, so no current is drawn from supply while load is shorted. In normal operation, load current of about 100 milliamperes is unaffected by diodes.

2. Waveforms. During normal operation of the logic-level translator, the output voltage and the current from the V_{CC} supply go on and off as the input logic goes high and low. If output load is short-circuited, diodes turn off transistors so that no currents flow.



long as the load is short-circuited, and it returns to normal operation when the short is removed.

Levels of input-logic voltage, output-logic voltage, and current from the high-voltage supply are shown in Fig. 2 for both normal operation of the circuit and the short-circuited-output condition. No current is drawn from the V_{CC} supply while the load is grounded. □

Power-supply add-on yields variable-ratio output

by Ying-Lau Lee
Cambridge, Mass.

A single-ended power supply can be converted into a double-ended supply with the addition of an operational amplifier, a transistor, and a few resistors. The two output voltages need not be equal and in fact can be made to have a ratio as big as 10:1 with the proper choice of resistor values.

The circuit is simple and works essentially as a parallel regulator. Potentiometer R_1 is set to the desired ratio of V_1/V_2; the 741 operational amplifier then compares the potentiometer voltage with the voltage at the collector of transistor Q and tries to minimize the difference by biasing Q to produce that ratio. If V_2 is too large, for example, the op amp drives Q farther into conduction. The drop across Q (i.e., V_2) then decreases.

The values of resistors R_2 and R_3 depend upon the maximum load allowed, input voltage, output voltage ratio, and transistor current gain h_{FE}. Approximate values for these resistors are calculated as follows:

$$R_2 = 0.8\,(V_1/V_2)R_{L2}$$
$$R_3 = h_{FE}\,V_{IN}R_{L1}R_2/V_1(R_{L1}+R_2)$$

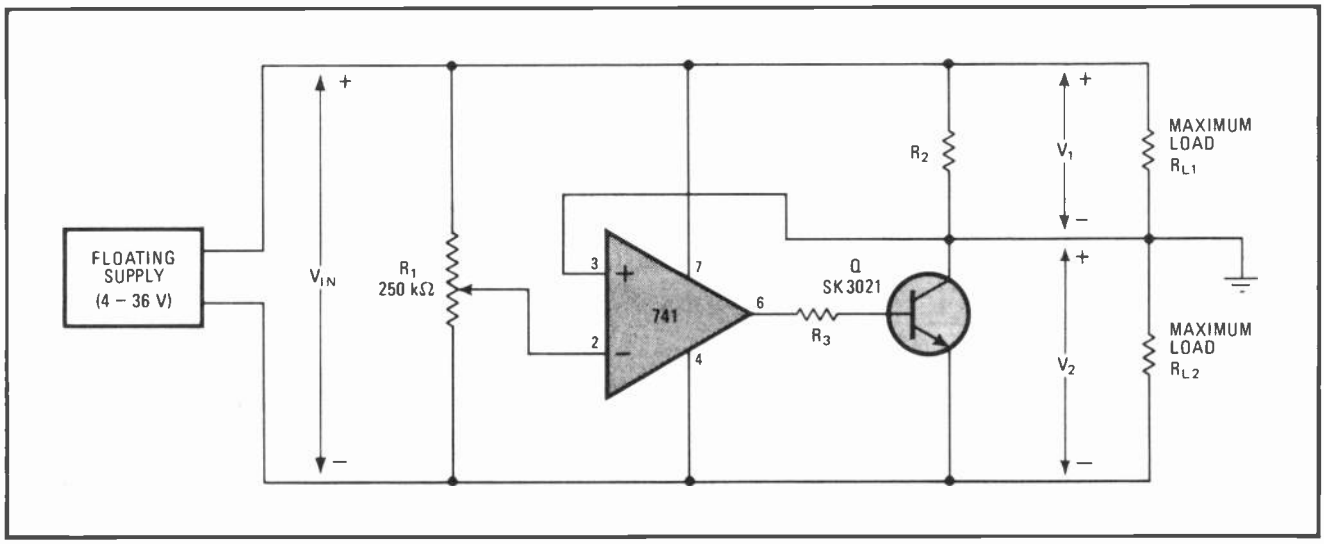
With R_2 and R_3 fixed, V_1/V_2 can be varied ±10% by adjustment of R_3.

If the outputs were balanced, no current would flow to ground. For unbalanced outputs, Q and R_2 carry the ground current. Transistor Q must be able to dissipate a power given by the following equation:

$$P_D = V_1V_2(R_{L1}+R_2)/R_{L1}R_2$$

The SK3021 transistor that is suggested in the schematic can dissipate 35 watts, but a lower-power device will be satisfactory in many cases. If Q drains too much current from the 741, a Darlington pair should be used to provide greater current gain.

Regulation of the output voltages is approximately that of the floating supply that is their source. The minimum value of output voltage V_2 is about 3 v (limited by the 741). The 741 is used for the operational amplifier because it is internally compensated and has overload protection. □



Two for one. Double-ended supply provides positive and negative voltages from a single source. Output voltages can be equal, or in ratio as great as 10:1. Potentiometer allows adjustment of V_1/V_2 around a "ballpark" value determined by resistors in circuit.

Matched optical couplers stabilize isolation circuit

by Arnold Nielsen
Ford Motor Co., Dearborn, Mich.

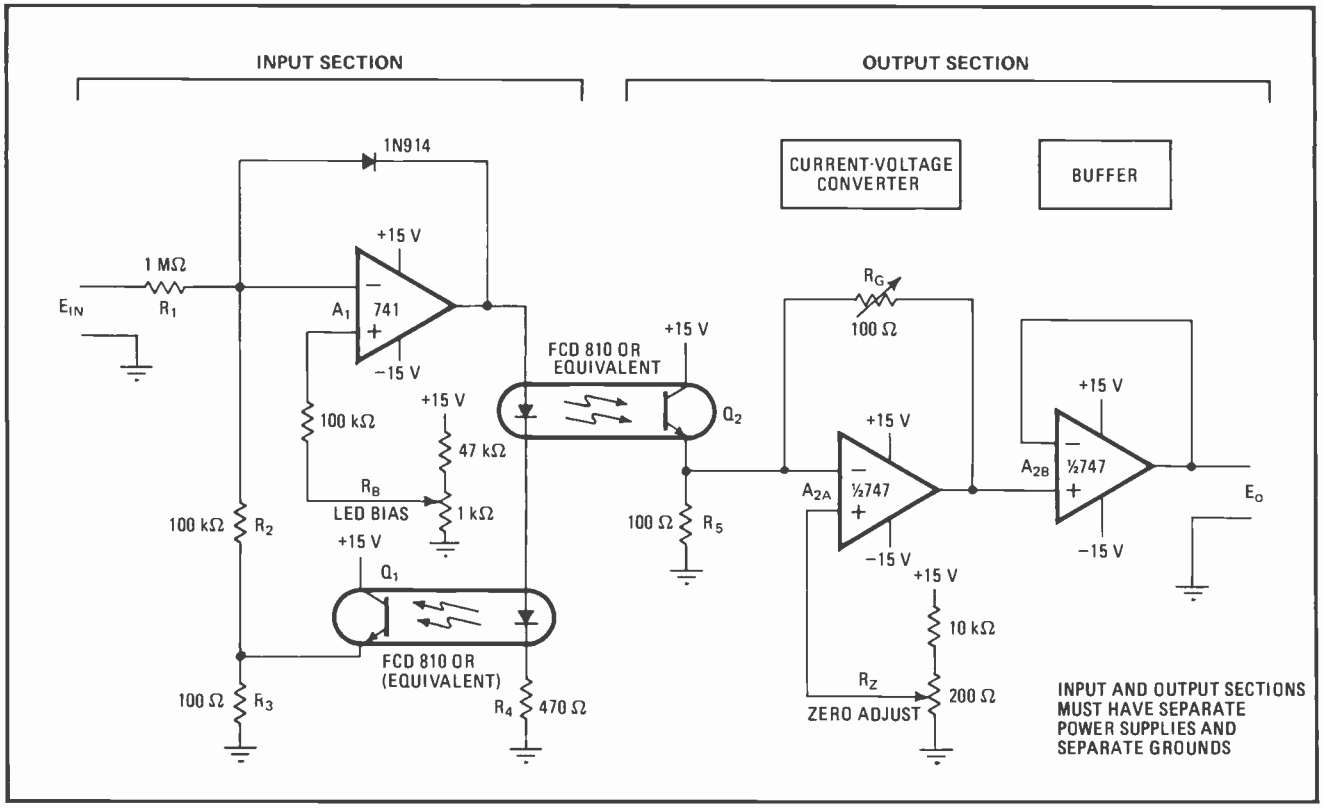
Temperature independence in an isolation circuit can be achieved by using a matched pair of optical couplers. In any optocoupler, the transfer characteristic is a function of T, and therefore the gain of an isolator with a single coupler depends on the temperature. But a second coupler in a feedback arrangement can cancel out temperature effects if the thermal characteristics of the two couplers are alike.

As the diagram shows, the light-emitting diodes of the two couplers are connected in series so that an input signal causes the same current to flow through both of them. One LED couples the input section of the circuit to the output section, and the other LED provides the feedback path that stabilizes the circuit. Thus, any temperature effect that changes coupling to the output section also changes the amount of feedback so that over-all circuit gain remains constant. The feedback also compensates for coupling nonlinearity.

A voltage from the LED bias potentiometer is fed to the noninverting-input terminal of operational amplifier A_1. This voltage, amplified through A_1, sets the LEDs in their most linear operating range. When an input signal is applied to the inverting terminal, operational amplifier A_1 drives the LEDs to a level at which collector current from Q_1 makes $I_{R2} = I_{R1}$, so that the inverting input is at virtual ground. (The 1N914 diode protects the LEDs against negative overvoltages; it is not part of the feedback circuit for A_1.) Because the LEDs are in series and are matched, $I_{R3} = I_{R5}$.

In the output section, the collector-to-base capacitance of Q_2 tends to decrease the frequency response of the circuit. This tendency is overcome by operating op amp A_{2A} in the current-to-voltage-converter mode, which maintains the signal voltage at the inverting input of A_{2A} and across Q_2 at virtual ground. Amplifier A_{2B} provides buffering at the output. The output voltage, E_O, is given by

$$E_O = I_{R5}R_G = I_{R3}R_G$$
$$\approx (R_2 + R_3)I_{R2}R_G/R_3$$
$$\approx (R_2 + R_3)E_{IN}R_G/R_1R_3$$



Stabilized by feedback. To avoid ground loop in instrumentation system, isolation between input and output is provided by optical coupling and by use of separate power supplies for each section. Temperature-sensitivity of optocoupler is compensated by second coupler in feedback loop of input op amp. The light-emitting-diodes are forward-biased for best linearity, and the feedback circuit further cancels nonlinear effects. Circuit operates with input signals of 0 to ±3 V at frequencies from dc to 50 kHz. Gain is 0.1 for circuit shown.

Therefore the gain (or attenuation) of the circuit can be stated as

$$E_O/E_{IN} \approx (R_2 + R_3)R_G/R_1R_3$$

For the component values shown in the diagram, the gain is approximately 0.1.

When the circuit is turned on, a sine wave is fed into the input. The output is displayed on a scope, and R_B is adjusted for symmetrical clipping as the signal amplitude is raised to 3 V. Then the input terminals are short-circuited, and potentiometer R_Z is adjusted so that the output voltage is zero. Finally, a 1-V signal is applied to the input, and R_G is adjusted to give the desired output level (0.1 V in this example). The gain then remains constant to within ±5% for any operating temperature between 0°C and 80°C.

The input signal can have any value from 0 to ±3 V, and the frequency response is determined mainly by the op amps used. The circuit shown here operates from dc to 50 kilohertz, where the signal is down 3 dB. The degree of isolation depends on the isolation resistance of the power supplies used for the input and output sections of the circuit. Therefore, power supplies that have high isolation resistance and electrostatic shielding are recommended, especially at low-millivolt signal levels. Isolation of at least 80 dB should be achieved without difficulty.

This circuit can be used as a single isolation amplifier or as part of a signal-distribution system. In the system application, one signal is common to all of the input sections, but the output sections are completely isolated from one another. □

How to prevent spurious tripping of protection circuits

by Thomas E. Skopal
Acopian Corp., Easton, Pa.

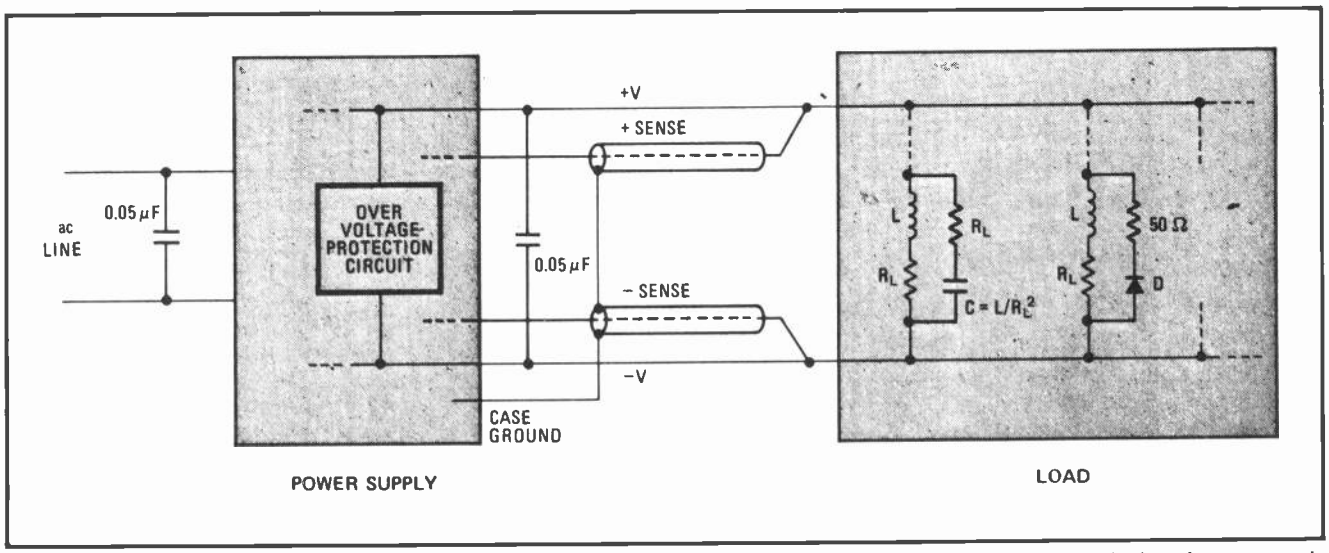
Users of power supplies sometimes find that crowbar circuits for overvoltage protection trip unnecessarily. The spurious tripping is caused by transients that are not dangerous to the load circuit, but that have enough amplitude to momentarily raise the voltage seen by the circuit to a level greater than its trip voltage.

The protection circuit is susceptible to this unwanted tripping because the trip level is set close to the rated output voltage of the supply and because the circuit is designed for quick response. The tripping should be prevented by suppressing the transients, not by reducing the sensitivity of the protection circuit.

Transients can reach the crowbar circuit in three ways: by coupling through the power supply from the ac line, by conduction through the output wiring from transient-generating elements in the load, and by picking up radiated transients in the system wiring.

Bypassing the input and output terminals of the power supply usually reduces transients from all causes to insignificant levels. To be most effective, nonpolarized capacitors should have good high-frequency characteristics, as provided by Mylar, disk ceramic, and mica types; a value of 0.05 to 1.0 microfarad is most effective. (The output capacitor of a typical power supply is usually an electrolytic type, which is intended for stabilizing the regulator circuit and for filtering, but is not an effective bypass for high frequencies.)

If additional leads are used for remote sensing or for output-voltage programing, shielded wire should be used, with the shields grounded only at the power-supply end. Bypassing these leads would help to suppress



Transient suppression. Suppressing all transients generated within or induced into a system prevents unnecessary tripping of power-supply overvoltage protectors. Four techniques described in the text are illustrated in this circuit. Capacitors at input and output terminals of the supply normally reduce transients to insignificant levels. Leads for remote sensing use shielded wire, grounded only at the supply end. Transients from electromechanical load element are suppressed by RC shunt. Reverse emf from inductive load is shunted through diode.

transients, but would also tend to slow the response of the supply, so shielded wire is used instead.

Crowbar operation is affected by electromechanical components in the load. Relays, counters, and solenoids tend to generate sizable transients that can damage a sensitive circuit; therefore, such transients must be suppressed at their source. They are most effectively suppressed by an RC network across the inductance. (Resistance in series with the bypass capacitor is necessary to prevent the high current surge that would otherwise flow into C when the load is energized. This current would burn switch contacts and cause noise.) The resistor value should equal the resistance of the load component, R_L, and the capacitor value should be equal to L/R_L^2, where L is the load inductance.

As an alternative, transients from an inductive component in a dc circuit may be suppressed simply by a diode connected across the component, back-biased relative to the supply voltage. The reverse voltage resulting from collapse of the magnetic field is shunted through the diode, and its amplitude is limited to the forward drop of the diode. However, this shunt diode tends to slow turnoff. The decay time-constant is given by $L/(R_L + R_{diode})$; if speed is critical, some suppression can be sacrificed for speed by adding a resistor (50 to 500 ohms) in series with the diode. □

555 as switching regulator supplies negative voltage

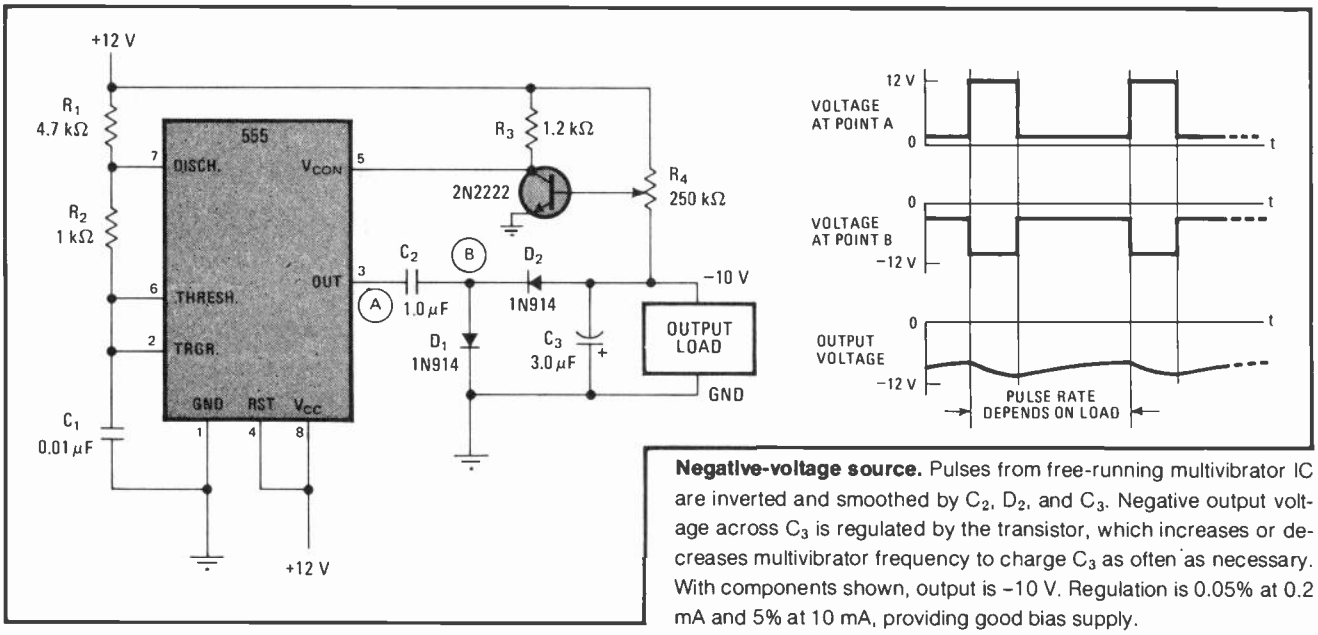
by S.L. Black
Western Electric Co., Columbus, Ohio

Latest addition to the 555 IC timer's seemingly endless bag of tricks is its use to generate a negative dc biasing voltage from a positive source. A current of well over 10 milliamperes can be delivered, and a form of switching regulation is employed to assure a constant output voltage. All of this is done with little more than an npn transistor and the 555 integrated circuit.

The 555 is operated in the astable mode, with the pulse width and frequency controlled by resistors R_1 and R_2 plus capacitor C_1. These parameters can be selected for maximum regulation at the output voltage level desired. Terminal 3 of the IC is connected to a network consisting of C_2, C_3, and diodes D_1 and D_2. Series capacitor C_2 causes the pulse train to lose its ground reference, so that D_1 and D_2 can rectify the signal and capacitor C_3 can filter it into a negative dc output voltage. The magnitude of this output voltage depends on the amplitude and repetition rate of the pulses coming from the IC.

To regulate the output voltage, the 2N2222 transistor varies the control voltage of the 555, increasing or decreasing the pulse repetition rate. Resistor R_3 acts as a collector load for the transistor; the base is driven from potentiometer R_4, which compares the output voltage to the supply voltage. If the output voltage becomes less negative, the control voltage goes closer to ground, causing the repetition rate of the 555 to increase so that C_3 recharges more frequently. If the output voltage becomes more negative, the control voltage goes closer to the positive supply voltage, so the repetition rate decreases, and C_3 is recharged less often.

The output voltage can be set to any level from 0 to −10 volts by means of potentiometer R_4. With the components shown in the figure, this circuit supplies −10 V from a 12-V source. Regulation is less than 5% at a current of 10 mA and less than 0.05% at 0.2 mA. □



Negative-voltage source. Pulses from free-running multivibrator IC are inverted and smoothed by C_2, D_2, and C_3. Negative output voltage across C_3 is regulated by the transistor, which increases or decreases multivibrator frequency to charge C_3 as often as necessary. With components shown, output is −10 V. Regulation is 0.05% at 0.2 mA and 5% at 10 mA, providing good bias supply.

Logic gates and LED indicate phase lock

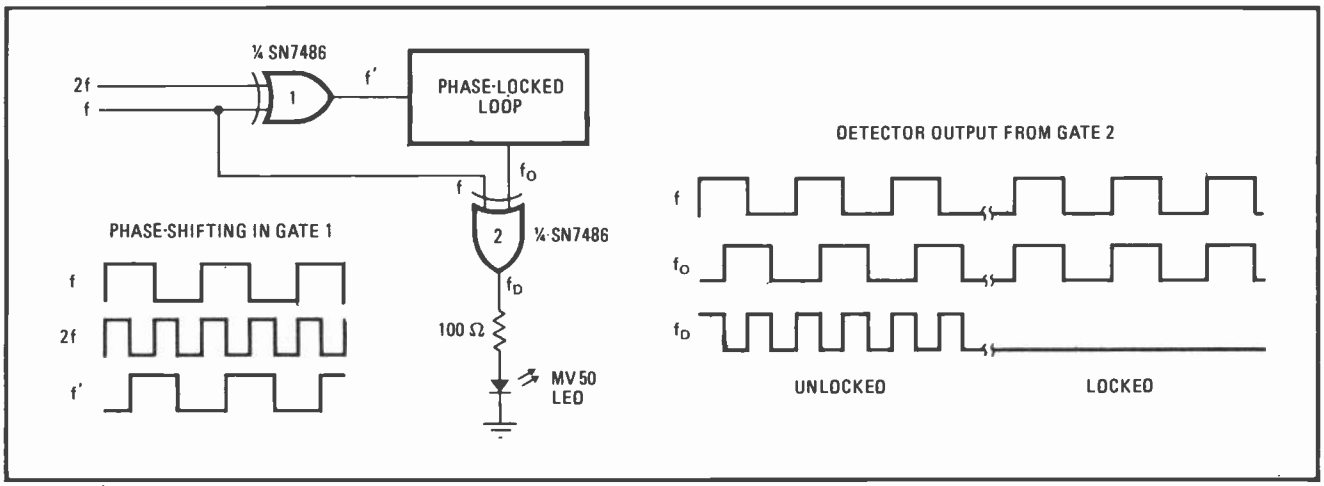
by R. P. Leck
Bell Laboratories, Crawford Hill, Holmdel, N.J.

Phase-locked loops are widely used for signal processing and digital applications such as fm demodulation, tone-decoding, and clock synchronization. If the error signal is accessible, signal acquisition and locking in the PLL can be observed from decrease of error voltage to zero. For integrated-circuit PLLs without an error-signal terminal, however, acquisition and lock can be indicated by two exclusive-OR gates and a light-emitting diode. The LED glows brightly when the input signal is first applied, then dims as the loop signal pulls into synchronism, and it goes out when the loop locks.

If the locked signal from the loop were in phase with the input to the loop, a single exclusive-OR gate would suffice for the indicator. In fact, however, the locked signal lags the input by 90°, so a second gate is needed to introduce an extra quadrature shift on either the input or output signal. As shown in the figure, the phase is shifted by applying frequencies f and 2f to an exclusive-OR gate. In the circuit shown here, the extra 90° is added to the locking signal before it goes into the loop; this procedure is convenient when f is generated by counting down from a master oscillator, because 2f is readily available.

From the square waves at f and 2f, gate 1 develops the 90°-shifted signal f′ that is the input to the loop-phase detector. Gate 2 functions as an auxiliary phase detector, comparing the phase between the loop output, f_O, and the non-phase-shifted input f. The output from gate 2, f_D, drives the light-emitting diode that indicates acquisition and lock.

When the loop is locked and its natural frequency is close to f, the inputs to the detector coincide. The resulting pulse width of the signal present at its output is either tiny or nonexistent, so the LED is turned off. When the loop is out of lock and its natural frequency is far from f, maximum output pulse width is obtained and the LED is turned on at its maximum brightness. As the loop acquires lock, the output-pulse width decreases, decreasing the brightness of the LED. □



Loop monitor. Phase-locked loop has LED monitor that glows brightly when loop is unlocked, dims as loop nears sync, and is dark at lock. Output from loop lags input by 90°; therefore, to permit comparison of output with locking signal, signal is shifted 90° before entering loop.

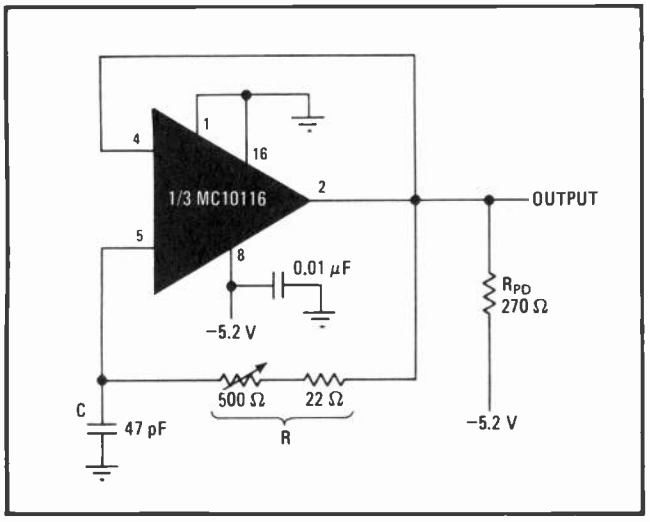
ECL IC oscillates from 10 to 50 MHz

by William A. Palm
Control Data Corp., Minneapolis, Minn.

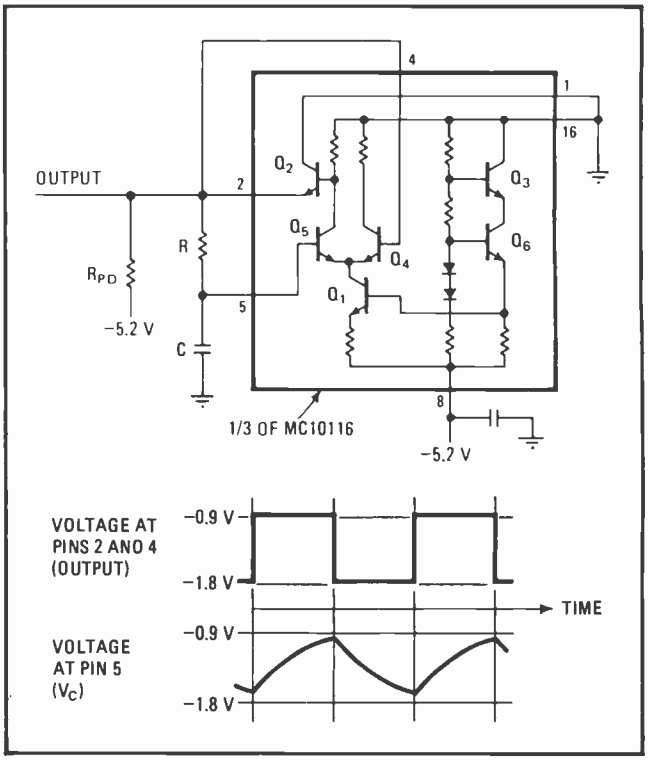
One of the simplest of oscillators, the emitter-coupled-logic type outlined in Fig. 1, uses one third of the circuitry of an MC10116 ECL integrated circuit. Besides the IC, the only elements required for the oscillator are resistor R and capacitor C. The frequency of oscillation equals 1/3.4 RC.

Details of the oscillator are shown in Fig. 2. Transistor Q_1 is a constant-current source for the differential amplifier made up of Q_4 and Q_5. The output signal, taken from emitter-follower Q_2 at pin 2, is fed back to Q_4 as the oscillator reference voltage at pin 4. Thus, pins 2 and 4 are always at the same voltage, and they switch between the ECL levels shown in the waveforms.

Operation of the circuit is indicated by the waveforms of voltage at pins 2 and 4, and at pin 5. The capacitor charges and discharges through resistor R when pins 2 and 4 go higher or lower than pin 5. When pins 2 and 4



1. Oscillator. Extremely simple connections to emitter-coupled-logic IC result in an oscillator that provides square-wave output. Adjustment of R tunes frequency across a range of 10 to 50 MHz. Different R and C permit band-switching over a 10:1 range of frequencies.



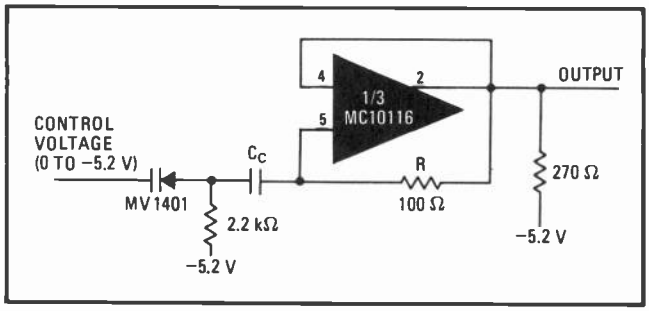
2. Operation. Circuit diagram shows how ECL oscillator operates. Output voltage is fed back to Q_4. Capacitor voltage at pin 5 tries to reach voltage at pin 4, causing output to switch between different ECL levels. Oscillator can never hang up.

are high, Q_4 conducts and Q_5 is off; the capacitor charges up until Q_5 starts to conduct, whereupon Q_4 cuts off and the voltage at pins 2 and 4 drops. The capacitor then discharges; when the capacitor voltage gets low enough, Q_4 starts to conduct, Q_5 cuts off, and the voltage at pins 2 and 4 jumps up. Thus, the capacitor voltage at pin 5 chases the voltage at pins 2 and 4, but never reaches their level because of the limited gain of the amplifier (approximately 8).

Values of R and C are not critical. The resistance of R can be as high as several kilohms or as low as 20 ohms. As R becomes smaller, pull-down resistor R_{PD} must also become smaller to keep emitter-follower Q_2 in conduction. For maximum oscillation frequency, R can be 20 ohms and C a few picofarads. The adjustable oscillator in Fig. 1 oscillates at frequencies in the range from 10 to 50 megahertz. Other choices for C and R can produce osillation at frequencies ranging from audio to vhf.

The frequency equation is inaccurate at the upper ranges because of propagation time, stray capacitance, and the difference between charge and discharge impedances presented at the output. It is desirable to buffer the oscillator through a second stage of the ECL IC.

Use of a varactor diode in place of capacitor C, as shown in Fig. 3, makes the circuit a voltage-controlled oscillator. A varactor with a capacitance range of 10:1, such as the MV1401, works well. Coupling capacitance C_C can be much larger than the diode capacitance, or can be chosen to limit the range of deviation. The oscillator in Fig. 3 operates at (15 ±10) MHz for a voltage swing of 0 to −5.2 volts at the VCO input. □



3. Voltage tuning. Varactor diode in place of C makes circuit a voltage-controlled oscillator. This VCO operates at (15 ±10) MHz.

Tri-level indicator monitors automobile's electrical system

by S. K. Wong
Torrance, California

The battery voltage of a car in operation indicates a great deal about the condition of the alternator, the voltage regulator, and the battery itself. Expensive sports cars are routinely equipped with gages to monitor voltage. Sedans may be optionally equipped with these voltmeters, but a good gage usually costs more than $30, and its size may make it difficult to install on the instrument panel.

Fortunately, exact voltage readings are not necessary to indicate the condition of the electrical system, even if a precise value could be read while the car is running. An instrument that shows three levels of voltage can give enough information to indicate that (1) a major component of the electrical system is faulty; (2) the battery voltage is fairly low, and the electrical system

should be checked; or (3) the battery voltage is adequate for efficient functioning of the system.

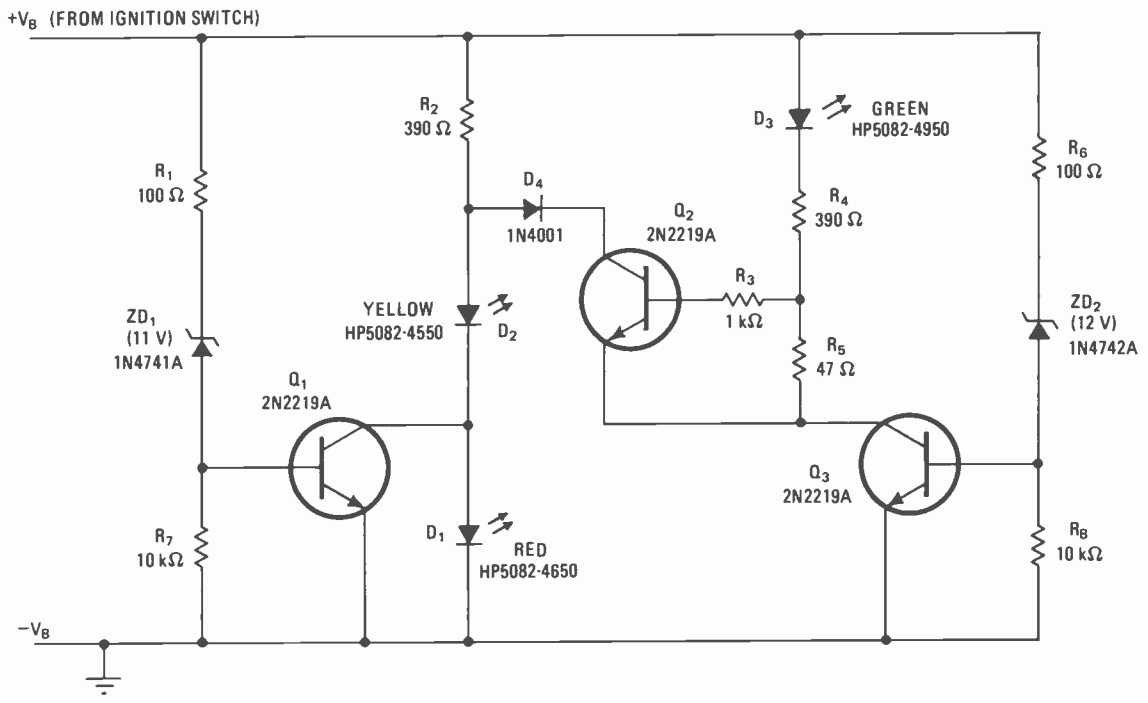
A solid-state tri-level voltage indicator that uses light-emitting diodes to show three voltage ranges can be built for $5 to $10, depending on the quality of the parts used, and it is a bargain for the purpose it serves. The circuit shown in the diagram uses, in addition to the three LEDs of different colors, three npn switching transistors, two zener diodes, one blocking diode, and a handful of 0.5-watt resistors. The red and yellow combination indicates a battery voltage of less than 11.7 V, yellow shows 11.7 to 12.7 V, and the green light shows that the battery voltage is 12.7 V or more.

If the battery voltage is below 11.7 V, all of the transistors are turned off. Diode D_4 blocks the current path through green LED D_3, the base and collector of Q_2, D_2, and D_1, so that current flows only through R_2, D_2, and D_1. The red and yellow LEDs light up to indicate that the battery, voltage regulator, alternator, or any combination of the three, is bad.

If the voltage is between 11.7 and 12.7 V, transistors Q_2 and Q_3 are still turned off, but zener ZD_1 conducts and lets Q_1 turn on to shunt out the red LED. Thus only the yellow LED lights up, warning the driver of a fairly low battery voltage. Unless this low-voltage situation improves after a few miles of driving, the electrical system of the car should be inspected for faults or high contact resistances.

If the battery voltage quickly reaches 12.7 V or more after the car is started, Q_3 also turns on. Current through Q_3 lights the green LED and also turns on Q_2 to shunt out the yellow LED. The resulting green light assures the driver of a functioning electrical power system in his car.

The user may choose zener diodes with somewhat different breakdown voltages if he wants to shift the three indication levels to fit his own requirements. □



BATTERY VOLTAGE	LEDs LIGHTED
$V_B \leq 11.7$ V	RED AND YELLOW
11.7 V $< V_B <$ 12.7 V	YELLOW
$V_B \geq 12.7$ V	GREEN

Battery-voltage indicator. Colored LEDs indicate three ranges of battery voltage in car. A weak battery turns on red and yellow, a stronger battery breaks down 11-V zener to light only yellow, and a strong battery turns on green as both zeners conduct. Resistors R_7 and R_8 provide high-temperature stability. This unit can warn of need for corrective maintenance of car's electrical system.

Monostable's pulse width is programable

by C.F. Reeves
Del Mar, Calif.

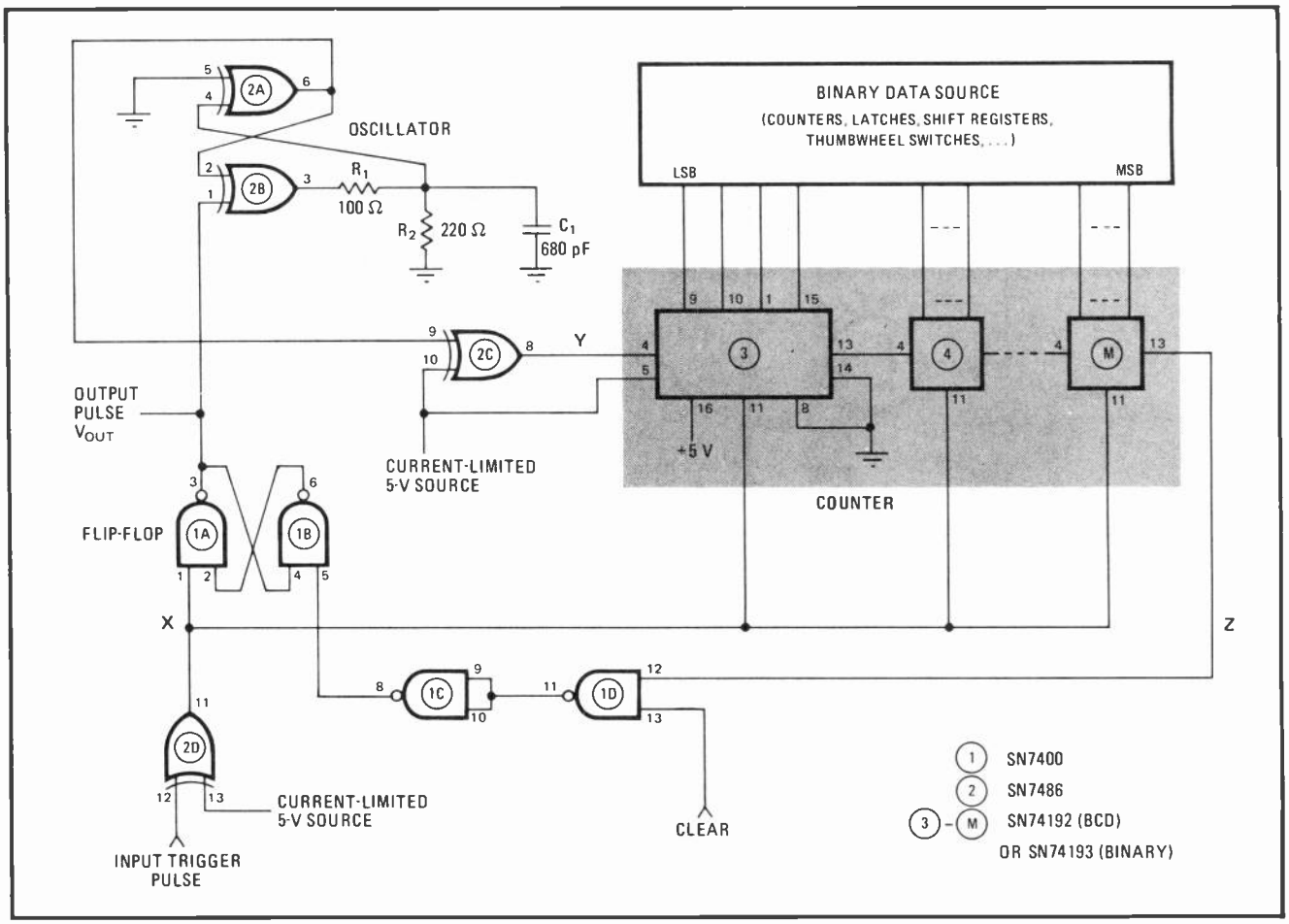
Variable-width pulses are required in many systems, and the widespread use of microprocessors as control elements makes numerical control of the pulse widths increasingly important. A numerically controlled one-shot multivibrator can be built that is particularly useful when the pulse-width range required is impractical or unattainable with conventional RC-time-constant one-shots.

For each input trigger pulse, the circuit produces an output pulse whose width is determined by an input binary number. The number may be taken from binary or binary-coded-decimal (BCD) sources such as shift registers, counters, bistable latches, thumbwheel switches, or the like.

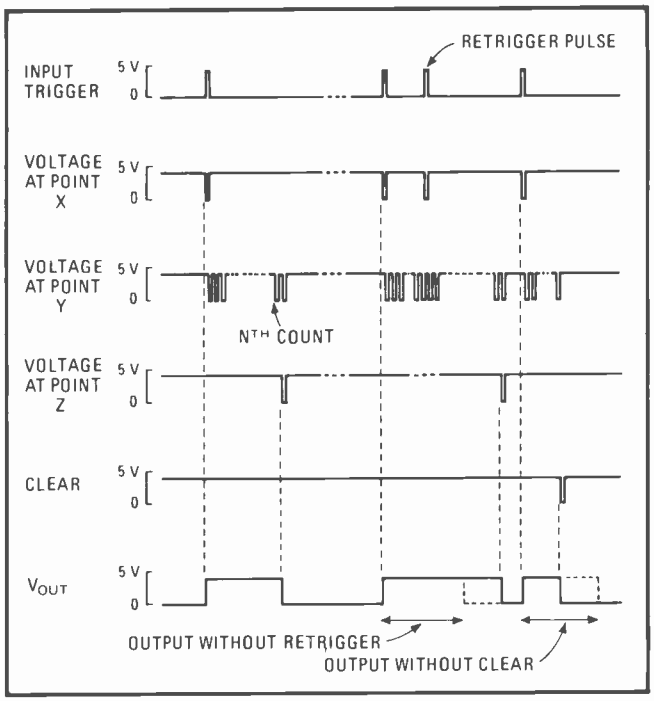
Functionally, the circuit is identical to the conventional one-shot in that it has one stable state and one temporary or quasistable state. The fundamental difference lies in the timing element that determines how long the circuit can remain in the quasistable state. In the conventional one-shot, this monostable period is set by the time constant of a resistor-capacitor network. The circuit shown here sets the monostable period by counting a preselected number of periods of a clock oscillator.

The range is thus limited only by the number of counter stages used. In Fig. 1 gates 2A and 2B form a clock oscillator that is gated on by a high logic level at pin 1. Resistors R_1 and R_2 and capacitor C_1 set the frequency at 10 megahertz. Gate 2C is an inverting buffer for the output pulses from the clock.

The input trigger pulse loads the counter chain (components 3 through M) with the number supplied by the binary data source. Simultaneously the trigger sets an



1. By the numbers. Binary number set into counter from data source determines duration of output pulse from this monostable circuit when input trigger pulse is applied. Output voltage V_{OUT} is high while counter counts the given number of cycles from the oscillator, as shown in Fig. 2. Typical applications for this circuit include variable-time-delay generation and pulse-code modulation.



2. Count. Waveforms for one-shot multivibrator in Fig. 1 illustrate operation. Input trigger makes V_{OUT} high and starts oscillator. Counter counts N cycles of oscillation (where N is decimal value of binary number set on counter by control source), then makes V_{OUT} low and stops oscillator. A trigger pulse applied during operation prolongs output pulse through countdown of newly loaded number. Output can be cut off at any time by grounding the clear terminal.

R/S flip-flop (1A and 1B), the output of which gates on the 10-MHz clock oscillator. The clock pulses cause the counter chain to count down to zero, whereupon the borrow pulse is generated at point Z. The borrow pulse resets the R/S flip-flop, disabling the clock oscillator and terminating the output pulse.

The width of the output pulse is determined by the binary input data and the clock frequency according to the following relationship:

$$PW = (N+1)/f_c$$

where N is the decimal value of the binary input number, and f_c is the clock frequency. The numerator is (N+1) instead of N because the counter generates the borrow pulse when leaving the zero state rather than when entering it. The output pulse-width range is determined by the number of 4-bit counter stages, K, and is expressed as $1:10^K$ for BCD input data and $1:16^K$ for binary input data. As the waveforms of Fig. 2 show, the one-shot is retriggerable. When an input trigger pulse occurs while the counter chain is counting down from a previous trigger, the chain simply reloads with the value of the binary data source and begins a new countdown. The result is a single elongated pulse. An additional circuit feature is that the output pulse may be terminated at any time by applying the logic zero to the "clear" input terminal. □

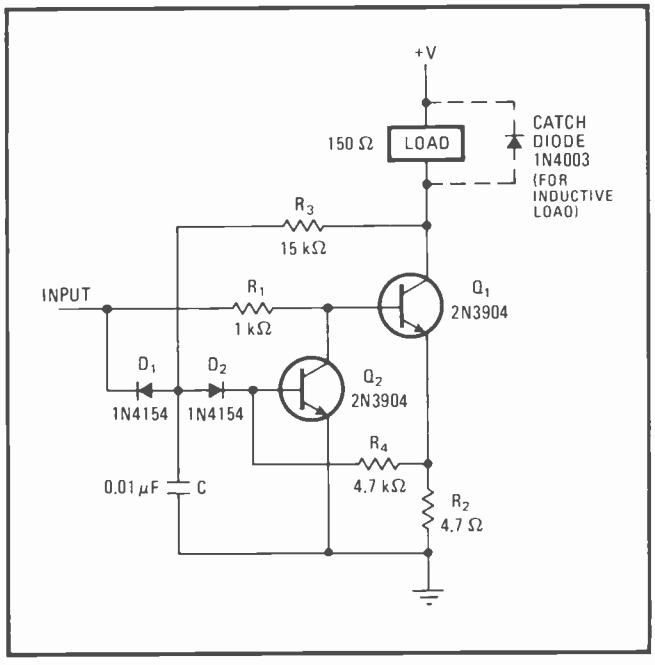
Current and power limiter protects switching transistor

by R.M. Stitt
Burr-Brown Research Corp., Tucson, Ariz.

Although a switching transistor dissipates little power in normal operation, it must be protected from destructive current and power overloads. Current-limiting alone is not sufficient protection; power-limiting is also necessary. But fortunately, a few components can be added to conventional current-limiting circuitry to provide power-limiting. A voltage rise across a transistor is sensed and used to cut down the drive current.

To understand why current-limiting alone fails to provide adequate protection, consider a switching transistor controlling a 100-ohm load connected to a 100-volt supply. The power dissipated in the load might be about 100 watts, but the maximum power dissipated in the transistor is merely the load current times the transistor's saturation voltage (if switching losses are neglected). The load current is about 1 ampere, so the transistor dissipates less than 1 W. A designer might use a 3-W device and provide a current-limiting level of 1.5 amperes.

Suppose, however, that the load is short-circuited so



Two-way protection. Switching transistor Q_1 is protected against excess current and/or excess power dissipation. If load current approaches limit, IR_2 drop turns on transistor Q_2 to shunt base drive from Q_1. A voltage rise across Q_1 acts through R_3 to turn on Q_2 and turn off Q_1. Capacitor C provides delay that allows Q_2 to saturate with each new cycle, and lets power-limiter ignore transient high currents. Diodes D_1 and D_2 reset power-limiter when input is low.

that the collector of the switching transistor is connected directly to the 100-V supply. Then the transistor dissipates 150 W, which destroys it.

To prevent this destruction, a power-limiter is required. Power-limiting can be added to a standard current-limiter by use of only four simple components. In Fig. 1, Q is the switching transistor, and the conventional current-limiter is formed by Q_2, R_2, and R_4. The power-limiter consists of capacitor C, diodes D_1 and D_2, and resistor R_3. To illustrate the operation of the circuit, assume that Q_1 is saturated and in normal operation. As the load current increases, the voltage drop across R_2 increases, turning on transistor Q_2 and thus shunting drive current away from the base of Q_1. Therefore, Q_1 begins to come out of saturation, so its collector voltage rises. This voltage across Q_1 further turns on Q_2 through R_3 and regeneratively turns off Q_1.

Diodes D_1 and D_2 form a switch so that the collector voltage of Q_1 is sampled only when its input is high. This switch also resets the power-limiting circuitry with each cycle of the input. The value of capacitor C is chosen to give the power-limiting portion of the circuit a turn-on delay, allowing time for Q_2 to become saturated. This delay also permits higher current transients to flow during switching, such as those that might occur in a switching regulator in which the catch diode must be discharged during each cycle.

The current-limiting portion of the circuitry is active at all times, protecting the switching transistor from current overloads. The circuit was set up to be driven by a TTL-level signal and to switch a 100-mA load at 400 Hz to +15 V. The protection circuit can easily be modified for nearly any input and output configuration. If a pnp-transistor switch is to be protected, transistor Q_2 should also be a pnp, and the polarities of D_1 and D_2 should be reversed. □

Compact dc-dc converter yields ±15 V from +5 V

by Thomas Durgavich
Massachusetts Institute of Technology, Cambridge, Mass.

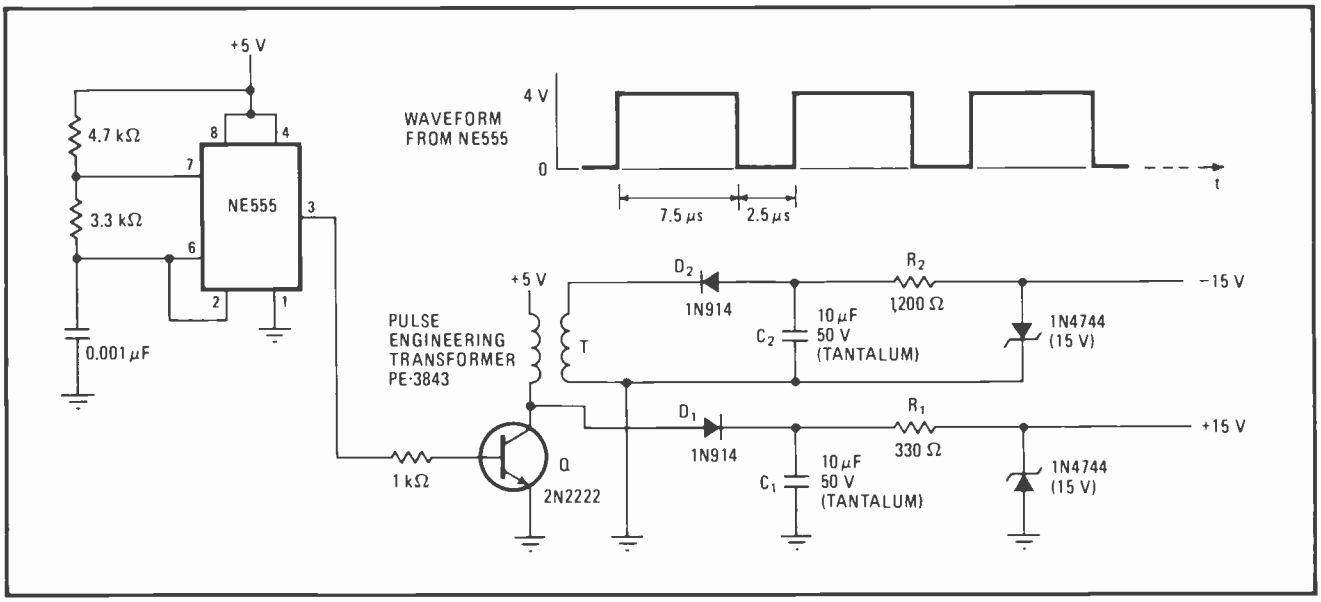
Many digital systems use a few operational amplifiers that require voltages of +15 V and -15 V, when all other elements require only 5 V. Both the +15 V and -15 V can be supplied at 10 milliamperes by a dc-to-dc converter that is compact enough to be built right on a printed-circuit board.

In this circuit, the NE555 operates as an astable multivibrator at 100 kilohertz with a 75% duty cycle. The value of frequency need not be exact, but this waveform has been found to optimize operation of the circuit.

The pulse train from the multivibrator drives the base of transistor Q to switch current on and off in the primary coil of transformer T. When the current is switched off, a spike of about 20 V occurs at the collector of Q. This voltage, rectified by D_1 and filtered by C_1 and R_1, is regulated by a simple zener-diode regulator to yield +15 V.

Simultaneously, a voltage spike appears across the secondary coil of transformer T. Because the transformer provides dc isolation, the higher-voltage end of the coil can be grounded to make the pulse negative. This voltage is also rectified, filtered, and regulated to yield -15 V.

This circuit is ideal when space is critical because small low-valued tantalum capacitors and a tiny pulse transformer replace the larger components that would be used in a conventional ±15-V supply. □



Space saver. Bipolar dc-to-dc converter operates from 5 volts and produces ±15 volts to supply op amps. Major advantage over conventional supply is small size, allowing assembly right on circuit board with other elements of system that it serves.

Microphone preamp gets power through signal cable

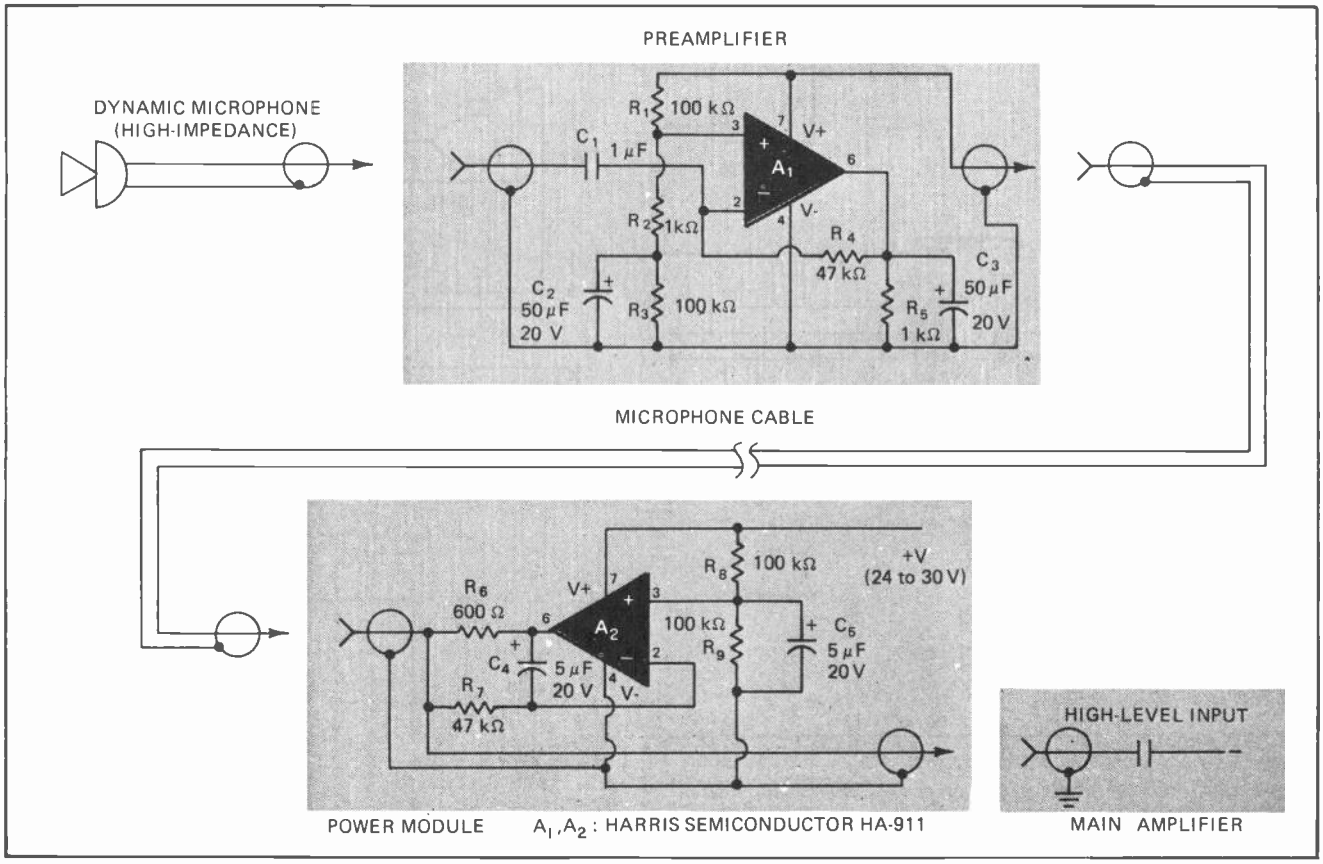
by Don Jones
Harris Semiconductor, Melbourne, Fla.

When a high-impedance microphone is at the end of more than 20 or 30 feet of cable, a preamplifier powered by batteries is often placed at the microphone to prevent high-frequency loss and to enhance the signal-to-noise ratio. But a preamp can be made much more compact if instead of using batteries it is powered remotely over the shielded or twisted-pair audio cable.

The hookup shown here is an unconventional application of an operational amplifier, but the performance will please any broadcaster or audio enthusiast. Performance is definitely high fidelity. Frequency response is better than ±1 decibel from 20 hertz to 20 kilohertz, and equivalent input noise is about 3 microvolts rms over this band.

The diagram shows the circuit arrangement. In the quiescent state, the output terminal (pin 6) of operational amplifier A_1 is biased by R_1, R_2, and R_3 to about half the power supply voltage, with negative feedback through R_4. However, the audio-output signal is not taken from pin 6; instead, the audio output comes from pin 7, the V+ terminal of the op amp. This output signal is inverted with respect to the normal amplifier output, so even though the audio-input signal from the microphone is fed into the inverting op-amp input terminal, the amplifier is actually noninverting. The gain (about 100) is determined by the ratio of R_1 and R_2, which form the feedback network from the V+ (audio-output) pin. The HA-911 op amp is used because its noise level (8 nV/Hz$^{1/2}$, 0.35 pA/Hz$^{1/2}$) and gain-bandwidth product (8 MHz) are many times better than those of general-purpose op amps.

In the power module, op amp A_2 supplies about 12 v dc at 7 milliamperes through a 600-ohm termination to the cable; the dc power for the module can probably be obtained from the main amplifier. Instead of using the power module, the power for the preamp could be supplied to the cable through a passive choke in series with a dc supply, but 150 henrys would be required to obtain the same noise isolation from the dc line. □



Two-way cable. Microphone cable carries power up to preamplifier and carries amplified signal down to main amplifier. Preamp, mounted at high-impedance microphone before long cable to preserve fidelity and suppress noise, is light and compact because its power is supplied through the cable, eliminating batteries. Although op amps are used in unconventional arrangements, performance is excellent.

Converter changes 7-segment output to decimal or BCD

by Prentice L. Orswell
National Oceanic and Atmospheric Administration, Boulder, Colo.

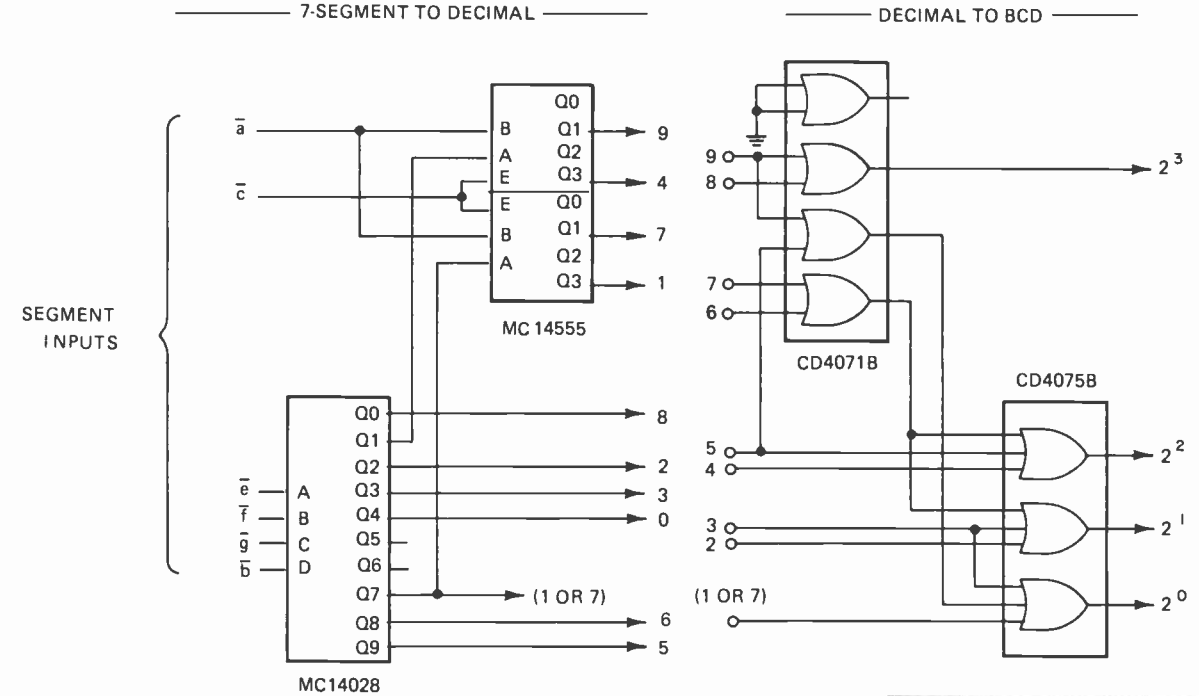
Calculator chips and other LSI circuits with outputs coded to drive seven-segment displays can have more varied applications if the seven-segment outputs are converted to decimal or binary-coded decimal. The converter described here accepts seven-segment MOS signals directly at voltages up to +15 volts and provides decimal and/or BCD outputs with blanking. It uses only four packages, at a component cost of less than $5. (For a seven-segment-to-decimal converter that used discrete transistors, gates, and an expensive demultiplexer, see *Electronics*, August 8, 1974, p. 105.)

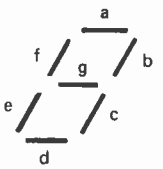
Only six of the segment outputs are required for this circuit. Four of them—b, e, f, and g—are applied to the input terminals of an MC14028 IC; a and c are applied to an MC14555, along with two signals from the MC14028. These two packages have a combined total of 10 output terminals, one of which goes high to represent a numeral (0 through 9) when the complements of the numeral's seven-segment voltages are applied at the input; most LSI circuits provide complementary outputs. The 10 terminals are the decimal outputs. (Another output, corresponding to either 1 or 7, is discussed below.)

If BCD outputs are desired, the decimal outputs are connected to the input terminals of a CD4071B and a CD4075B. These units provide a total of four output terminals, which go high to represent the four BCD bits.

In the seven-segment-to-decimal portion of the circuit, the MC14028 (which is a BCD-to-decimal decoder) uniquely determines six of the decimal outputs. The complements of b, e, f, and g segment voltages for both 1 and 7 decode to output Q7, and digits 4 and 9 both decode to Q1. To separate these in the MC14555 (which is a dual binary-to-1-of-4 decoder), the complement of a is used as an additional input. Full blanking is assured by applying the complement of c at the enable inputs.

Conversion to BCD from the decimal code could be accomplished in several ways. An ideal one-package so-





7-SEG. DIGIT	SEGMENT $\overline{a}\,\overline{c}\,d$	SEGMENT $b\,g\,f\,e$	MC14028 OUTPUT SELECTED
0	000	0100	Q4
1	101	0111	Q7
2	010	0010	Q2
3	000	0011	Q3
4	101	0001	Q1
5	000	1001	Q9
6	000	1000	Q8
7	001	0111	Q7
8	000	0000	Q0
9	000	0001	Q1
BLANK	111	1111	ALL LOW

Converter. Complements of seven-segment voltages, fed into inputs of this circuit, produce high level on one of the decimal-output lines and (if the conversion is carried over to the BCD) on one or more of the BCD output lines. Thus for segment voltages that could display a seven-segment 5, inputs for the b and e segments are high, producing a voltage on decimal output line marked 5; and if BCD-to-decimal stage is connected, lines marked 2^0 and 2^2 go high.

lution would be a 10-bit priority encoder, but this circuit is not available in C-MOS, so at least two packages are required to implement the encoder. An 8-bit priority encoder and some gating would work. A more economical approach, using OR gates, is shown in the diagram. Note that one gate is saved for other uses by utilizing the 1-or-7 output. All of the BCD outputs go low with blanking. □

Capacitive transducer senses tension in muscle fibers

by Robert M. Wise
Medical College of Virginia, Richmond, Va.

Tension in muscle fibers can be measured by the same capacitive transducers that measure displacement and pressure. The ubiquitous NE555 timer and an NE560B phase-locked loop combine with a specially made capacitor to produce an analog output whenever there's a change in capacitance. Tuned circuits are not required, and both size and stability of the timer permit design versatility.

The heart of the circuit is the timer. When pins 2 and 6 are connected, the timer triggers itself and runs free as a multivibrator. The transducer charges through R_1 and R_2 and discharges through R_2. The frequency is precise and independent of supply voltage. Charge time is:

$$t_1 = 0.693\,(R_1 + R_2)\,C_T$$

Discharge time is:

$$t_2 = 0.693\,(R_2)\,C_T$$

Frequency of oscillation is then:

$$f = 1/T = \frac{1.44}{(R_1 + 2R_2)\,C_T}$$

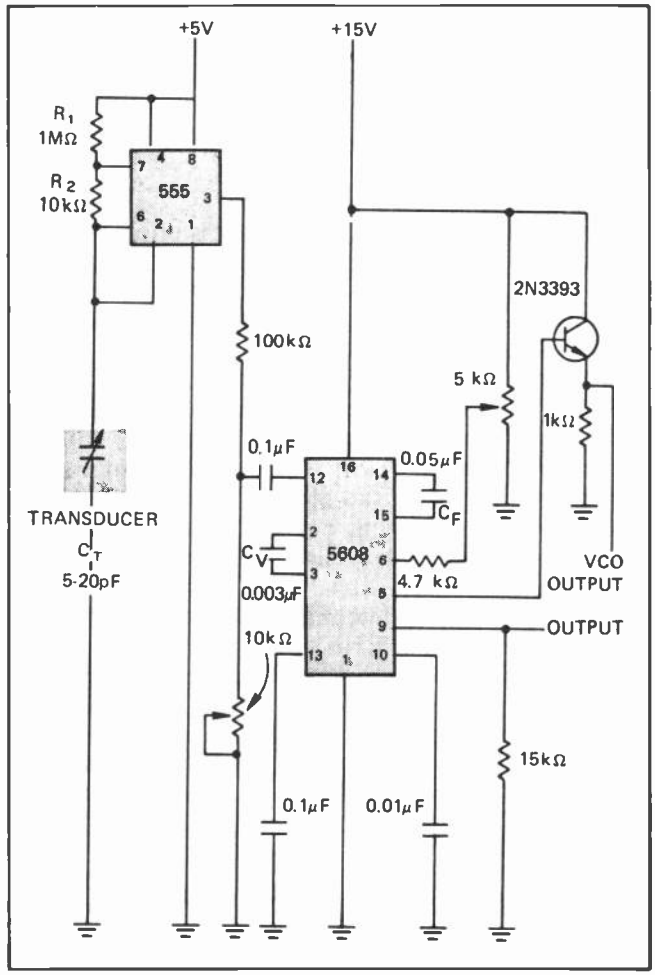
Any frequency between 0.1 hertz and 100 kilohertz can be selected; the component values shown in the figure are for a frequency of about 100 kHz.

The input signal to the 560B is phase-compared to an internal voltage-controlled oscillator. Error signal at the output of the comparator is filtered, amplified, and fed back to the VCO. Input frequency to the phase-locked loop through pin 12 must be attenuated to facilitate proper lock and capture of the transducer signal by the VCO. The voltage should be between 20 and 50 millivolts peak to peak.

The frequency of the VCO, which should be adjusted to coincide with the zero-position frequency of the transducer, is determined principally by the capacitor C_V connected between pins 2 and 3 of the NE560B:

$$f_{VCO} = 300/C_V$$

where C_V is expressed in microfarads. Fine adjustment of f_{VCO} can be made by a regulating current injected into pin 6 through a 4.7-kilohm resistor and controlled by the setting of the 5-kilohm potentiometer. The zero-position frequency of the transducer is measured at pin 12 of the phase-locked loop, and the VCO frequency is measured from pin 5 through the 2N3393 emitter-follower transistor to avoid pulling the VCO.



Frequency modulation. Capacitive transducer modulates frequency of 555 multivibrator. Frequency is detected in 560B phase-locked loop that produces dc output voltage. Arrangement is stable and compact, has fast response, and does not require any tuned circuits.

A filter capacitor C_F between pins 14 and 15 sets the desired bandwidth of demodulated information. The approximate value of C_F in microfarads can be found from the formula

$$C_F = 13/B$$

where B is the bandwidth in Hz. The 0.05-μF value shown gives a clean output swing of 100 millivolts.

The de-emphasis network uses an external capacitance of 0.01 μF in conjunction with an 8-kilohm internal resistance at pin 10 to produce a 75-microsecond time constant for the demodulated output at pin 9. The 100 mV output swing rides on a 12-V offset voltage. □

Digital word sets gain of amplifier

by Craig J. Hartley
Baylor College of Medicine, Houston, Texas

Digital control of gain or attenuation is often desirable in programable systems or when the gains of many circuits have to be varied simultaneously. In the circuit shown, the gain or attenuation of an analog signal is controlled by means of a binary input. The circuit, which is similar to a multiplying digital-to-analog converter, uses a single 741 operational amplifier for gain or attenuation, plus two transistors for each control bit.

The circuit has two parts. The first is a noninverting operational amplifier; the second is a set of resistors that can be connected in parallel to produce various values for an equivalent single resistor R_C between switch S and ground.

The value of R_C is determined by the digital inputs. When the input labeled 1 is low, transistors Q_1 and Q_2 are saturated, so that the 100-kilohm resistor R is connected from switch S to ground. When input 1 is high, Q_1 and Q_2 are off, so the bottom of R is open-circuited.

Similarly, if inputs 2, 4, and 8 are low, they connect R/2, R/4, and R/8 to ground. Therefore the control inputs can be considered as a binary number with negative logic (high voltage = 0, low voltage = 1) so that the total resistance connecting the switch to ground is

$$R_C = R/N$$

where N is the value of the binary input number. For example, if N equals 5, the binary number is 0101, which means that inputs 1 and 4 are low; therefore R and R/4 are connected in parallel to provide a resistance of R/5 from S to ground.

When switch S is in position A, the gain of the op amp is

$$G_A = E_o/E_i = 1 + R_F/R_C = 1 + NR_F/R$$

The values of R_F and R are equal, so

$$G_A = 1 + N = 1, 2, 3, 4, \ldots$$

For a 4-bit control word, the maximum G_A value is 16.

When the switch is in position B, the op amp is connected as a voltage follower fed by a voltage divider, so the gain is

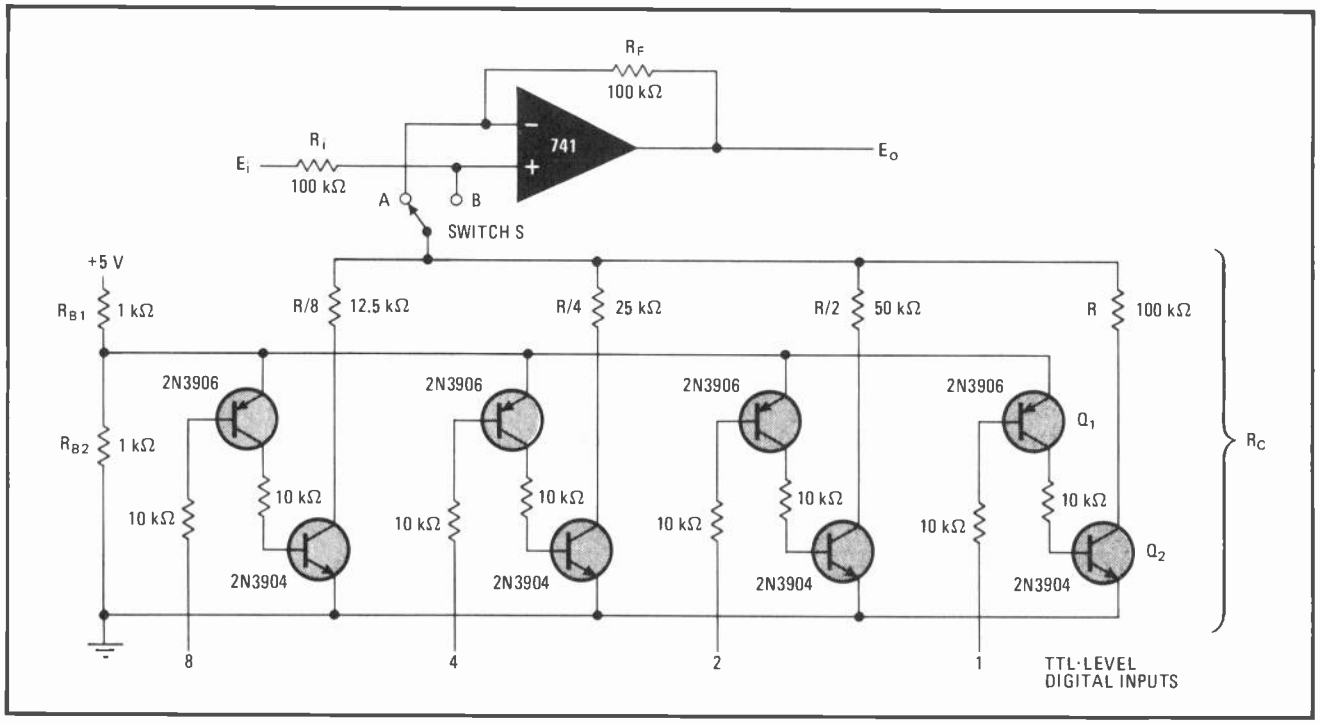
$$G_B = R_C/(R_i + R_C) = (R/N)/(R_i + R/N)$$

Because R_i is equal to R,

$$G_B = 1/(N+1) = 1, \tfrac{1}{2}, \tfrac{1}{3}, \tfrac{1}{4}, \ldots$$

Thus the circuit can amplify (switch position A) or attenuate (switch position B).

The circuit as shown will handle analog input levels



Programable gain or attenuation. The operational-amplifier circuit has a gain of $G_A = N + 1$ or $G_B = 1/(N+1)$, depending on whether switch S is set to position A or position B. The number N is the value of the negative-logic binary number applied to the digital inputs. If programable sign-reversal is required, a digitally controlled inverter [*Electronics*, March 6, p. 85] can be used in tandem with the amplifier.

of ±7 volts, and the digital inputs will accept TTL logic levels. The bias resistors and supply voltage can be varied as needed for use with other logic forms. The offset is about 0.02 v maximum in the B mode and 0.25 v maximum in the A mode and is a function of gain. Additional digits can be added for finer control. □

Bootstrap circuit generates high-voltage pulse train

by Lawrence H. Bannister
Center for Space Research, MIT, Cambridge, Mass.

A circuit can easily be built to generate a high-voltage pulse train from a low-voltage power supply. Such a circuit is used in a recently developed spacecraft instrument to generate a 400-hertz square wave with an amplitude of 4 kilovolts from 20 identical 200-volt stages connected in series. A high-voltage supply is not needed because each stage includes a capacitor that functions as a floating power supply for the next stage. These capacitors are charged in parallel and then connected in series so that the pulse generator does its own dc-to-dc conversion.

The schematic of Fig. 1 is drawn to emphasize the modularity of the circuit. To simplify the explanation, it is assumed that all transistors and diodes are perfect switches, having infinite impedance when turned off and zero voltage-drop when turned on.

Suppose, first, that transistors $Q_{1\text{-}1}$, $Q_{1\text{-}2}$, . . . $Q_{1\text{-}N}$ are all turned off. Then diodes $D_{1\text{-}1}$, $D_{1\text{-}2}$, . . . $D_{1\text{-}N}$ are forward-biased and transistors $Q_{2\text{-}1}$, $Q_{2\text{-}2}$, . . . $Q_{2\text{-}N}$ are driven to saturation. Capacitor $C_{1\text{-}1}$ charges through the path $D_{3\text{-}1}$, $C_{1\text{-}1}$, $D_{2\text{-}1}$, and $Q_{2\text{-}1}$. Concurrently, $C_{1\text{-}2}$ charges through the path $D_{3\text{-}2}$, $C_{1\text{-}2}$, $D_{2\text{-}2}$, and $Q_{2\text{-}2}$. So, in this circuit condition, all of the capacitors charge in parallel, and the potential difference across each capacitor is equal to the supply line voltage of 200 volts:

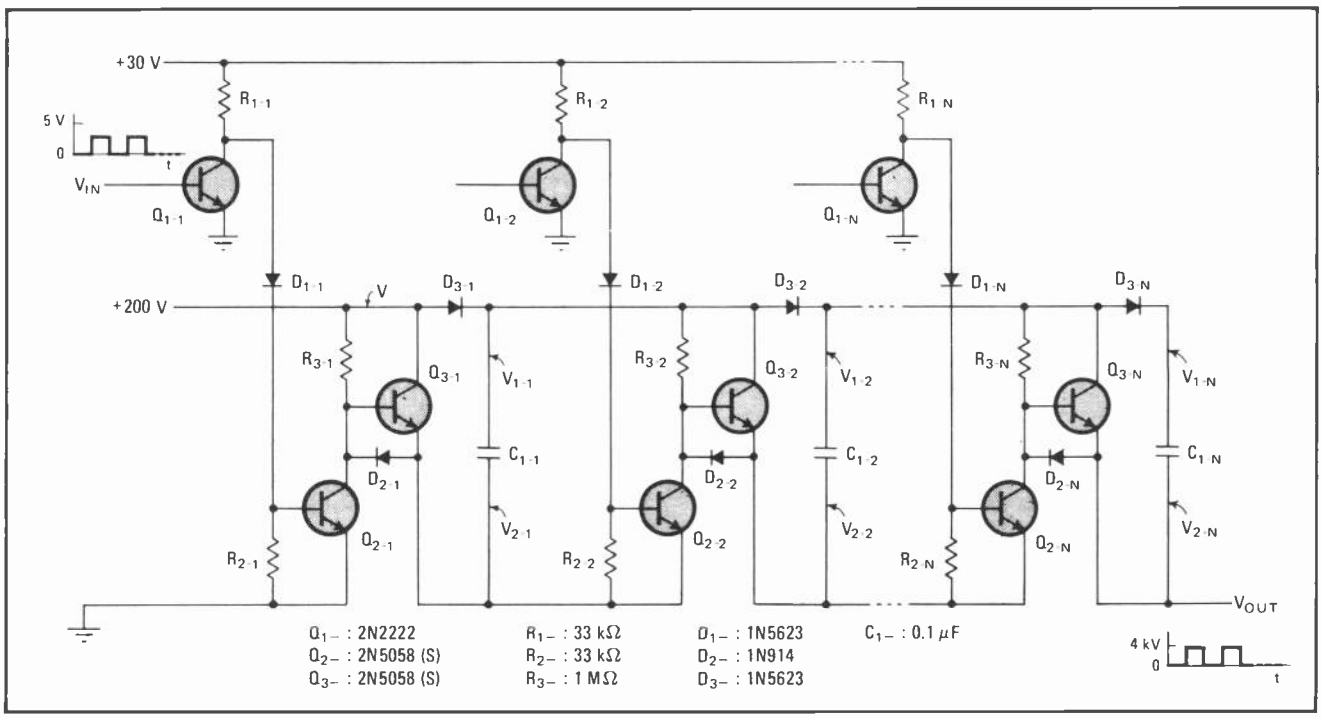
$$V_{1\text{-}N} = V_{1\text{-}2} = V_{1\text{-}1} = V = +200\ v$$
$$V_{out} = V_{2\text{-}N} = V_{2\text{-}2} = V_{2\text{-}1} = 0$$

If, now, $Q_{1\text{-}1}$ is turned on, diode $D_{1\text{-}1}$ no longer conducts, so $Q_{2\text{-}1}$ turns off. Current through resistor $R_{3\text{-}1}$ then causes $Q_{3\text{-}1}$ to turn on, and the emitter potential of $Q_{3\text{-}1}$ approaches its collector potential so that $V_{2\text{-}1} = V = +200$ v. And, because $C_{1\text{-}1}$ was previously charged to the supply voltage, $V_{1\text{-}1} = V_{2\text{-}1} + V = 2V = +400$ v.

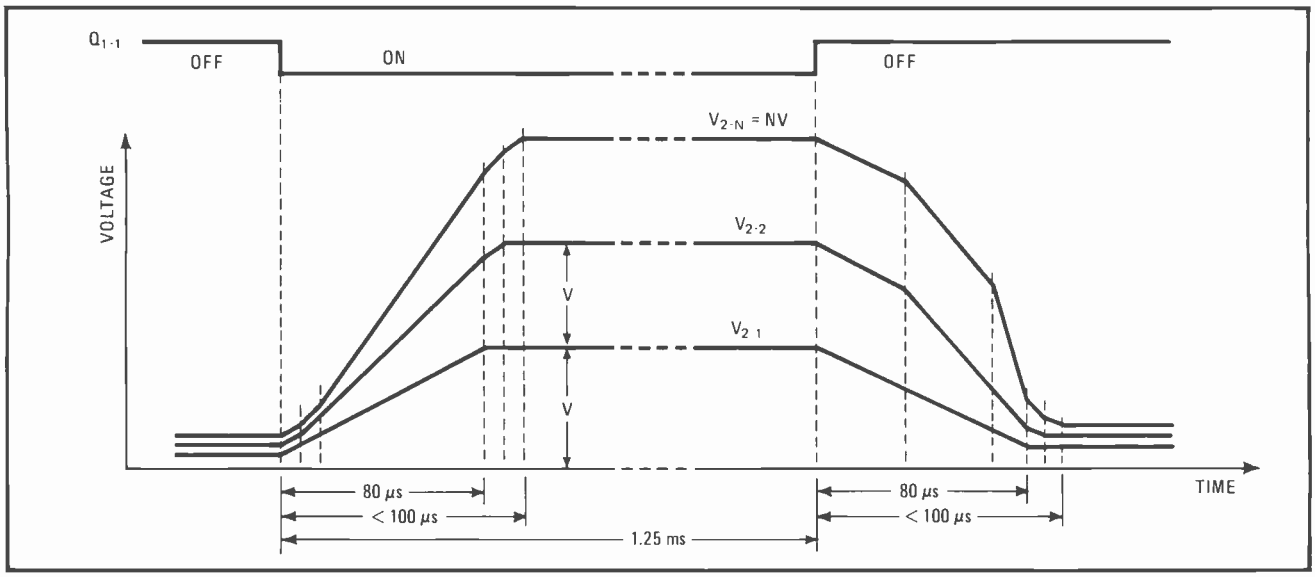
Now, regardless of the state of $Q_{1\text{-}2}$, when $V_{2\text{-}1}$ becomes positive, $D_{1\text{-}2}$ becomes reverse-biased, and therefore $Q_{2\text{-}2}$ turns off. Current through $R_{3\text{-}2}$ then causes $Q_{3\text{-}2}$ to turn on, and the emitter potential of this transistor approaches its collector potential so that:

$$V_{2\text{-}2} = V_{1\text{-}1} = 2V = +400\ v$$
$$V_{1\text{-}2} = V_{2\text{-}2} + V = 3V = +600\ v$$

As illustrated by Fig. 2, this sequence continues along the series of stages, each stage increasing the positive level of the pulse by V volts. The final output voltage is NV volts, where N is the number of stages and V is the



1. Kilovolt generator. Square wave of 4 kV at 400 Hz is produced by circuit with 20 low-voltage stages. Each stage includes a capacitor (C_1) that acts as a floating power supply for the next stage. The capacitors are charged in parallel and then connected in series. If lower output voltage is desired, input can be applied to $Q_{1\text{-}2}$ or $Q_{1\text{-}3}$ or . . . instead of $Q_{1\text{-}1}$. (Actual circuit also includes elements shown in Fig. 3.)



2. Timing. The stages start switching sequentially, as diodes $D_{1\text{-}1}$, $D_{1\text{-}2}$, . . . successively become back-biased, but after all stages are switched, they change voltage levels concurrently. Therefore the rise time is essentially that of a single stage. Similarly, the fall time is essentially independent of the number of stages. The output amplitude is the product of the power-supply voltage and the number of stages.

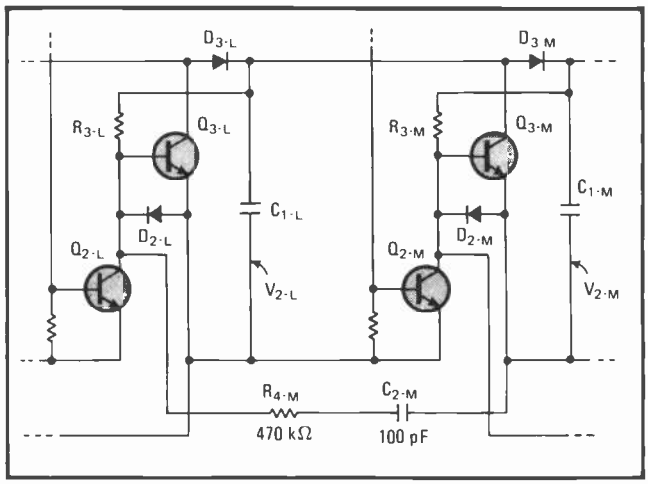
supply voltage. Because the stages switch concurrently, the total pulse rise time is only slightly longer than the rise time of one stage.

Smaller-amplitude pulses can be generated by switching only the last few stages to the "high" state. For example, if $Q_{1\text{-}1}$ remains off, but $Q_{1\text{-}2}$ is turned on, the first stage will remain in the "low" state with $V_{1\text{-}1}$ = V = +200 V but all subsequent stages will switch to the "high" state so that V_{out} = (N - 1)V. If only $Q_{1\text{-}N}$ is turned on, the preceding stages will remain in the "low" state and the output pulse amplitude will just be V volts. Generally, then, the output-pulse amplitude can be selected in increments of V up to a maximum of NV.

The positive-going edge of the pulse generated by the circuit of Fig. 1 is quite slow because, in each stage, when Q_2 is turned off, the potential at the base of Q_3 increases exponentially toward a limiting value. Further, the output impedance of the circuit is quite large because the current in R_3 approaches zero in the "high" state and Q_3 never really saturates.

The circuit modification shown in Fig. 3 prevents these problems by the use of positive feedback in and between the stages. R_3 is connected to provide positive feedback within the stage; when Q_2 is turned off and Q_3 starts to conduct, the potential at the top end of R_3 remains V volts above the potential at the emitter of Q_3. Thus, the potential difference across R_3 is sensibly constant, and Q_3 is driven by a constant current supply so that its base potential increases linearly until the base-collector junction is forward-biased. Q_3 then behaves like an inverted switch transistor with a very low offset voltage that is just the difference between the voltage drops of the base-emitter and base-collector diodes.

R_4 and C_2 provide positive feedback from one stage to the immediately preceding stage to speed the switching action. For example, when the stages switch to the "high" state, $V_{2\text{-}L}$ increases toward LV while $V_{2\text{-}M}$ increases toward MV. The difference between these voltages, MV - LV = (L+1)V - LV = V, causes a transient current through $R_{4\text{-}M}$ that drives the base of $Q_{3\text{-}L}$ positive more rapidly.



3. Feedback. To achieve 400-Hz operation, the circuit in Fig. 1 is modified as shown here. R_3s provide positive feedback within each stage, and R_4s and C_2s provide positive feedback from each stage to the preceding stages. Without the feedback, rise time is about 1 ms; with feedback, rise and fall times are both less than 0.1 ms.

With these feedback connections, the operating circuit produces a 400-Hz square wave with rise and fall times of about 100 microseconds that are essentially independent of the number of stages switched. The number of stages switched changes only the amplitude of the square wave; this amplitude can be selected in increments of 200 V, up to a maximum of 4,000 V for a 20-stage circuit. The only high-voltage components are the diodes labelled D_1 in Fig. 1. In the spacecraft instrument, series strings of diodes are used as D_1 to provide the necessary isolation for the higher-voltage stages of the pulse generator. □

D-a converter forms programable gain control

by Jim Edrington
The Applied Research Laboratories, University of Texas, Austin, Texas

A monolithic multiplying digital-to-analog converter can be used with an operational amplifier to produce a simple digitally controlled amplifier. Logic voltages applied at the 10 input terminals of a converter such as the Analog Devices AD7520 control the gain. These voltages can provide 2^{10} discrete levels of amplification for an analog signal applied to the operational amplifier. The integrated circuit can handle analog signals up to ±10 volts, and the digital input levels are compatible with transistor-transistor logic and complementary-MOS.

A BCD-to-decimal decoder drives the d-a converter in the circuit of Fig. 1, giving gains as high as 60 decibels in 10 6-dB steps. The circuit requires only a few components because the multiplying converter IC contains the C-MOS switches and precision-resistor ladder network that set the gain of the amplifier.

The 741 op amp is connected as a conventional inverting amplifier, with an input resistor and a feedback resistor. As shown in Fig. 2, these resistors are elements of the d-a converter, and its control inputs determine the amount of resistance in the feedback loop.

Current from the output of the op amp that enters terminal 15 (V_{REF}) of the converter sees a resistance of R. This current, I_{REF}, divides in half at every node of a ladder network made up of resistors R and 2R. Part of this current goes to ground, and the remainder goes to the inverting input terminal of the op amp (virtual ground). In Fig. 2, since only the second control bit is high, I_F, the current fed back, is $I_{REF}/4$.

The input signal to the amplifier circuit is applied to terminal 16 of the AD7520 (the terminal marked $R_{FEEDBACK}$) because the internal resistor at this terminal matches the others in the converter. The input signal also sees a resistance of R and delivers a current equal to I_F. The gain of the amplifier circuit is

$$e_o/e_i = -I_{REF}R/I_FR = -I_{REF}/I_F$$

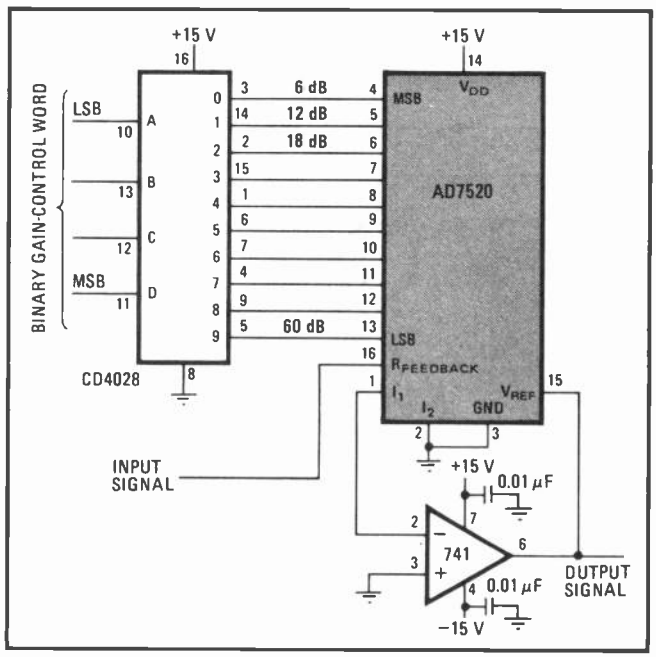
For the example in Fig. 2, where I_F is $I_{REF}/4$, the gain is -4, or 12 dB.

The input word in Fig. 1 causes only one of the AD7520's control inputs to go high. The voltage gain of the amplifier can be written as (-2^{n+1}). Expressed in decibels,

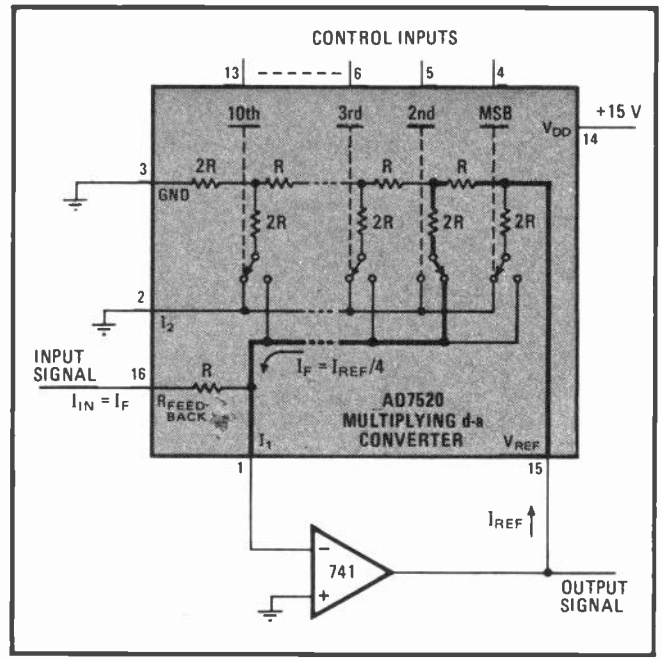
$$G = 6(n+1)\ dB$$

where n = 0, 1, . . . 9 is the value of the input word.

External resistors may be added in series or parallel at the amplifier's input to change the over-all gain or to allow input summing. Any standard op amp may be used, but fast op amps should be compensated carefully because many are unstable in low-gain configurations.□



1. Programable gain. Amplifier has gain of 6(n + 1) dB, where n is decimal value of binary-input word. Component count for circuit is low because the switches and resistors that control gain are all in AD7520 IC. Voltage levels for input logic are compatible with TTL and C-MOS, and analog input signal can be as large as ±10 V.



2. Resistors. Ladder network in AD7520 multiplying d-a converter provides feedback path for op amp. Current I_{REF} divides in half at every node of ladder, and switches set by control inputs determine current I_F that gets back to op amp's input terminal. Circuit gain is I_{REF}/I_F; for configuration shown, gain is −4, or 12 dB.

One-shot with feedback loop maintains constant duty cycle

by H.P.D. Lanyon
Worcester Polytechnic Institute, Worcester, Mass.

Electronic equipment often generates a sequence of fixed-length pulses with a variable repetition rate. A circuit can be built that adjusts the widths of the pulses to produce an output train with a constant duty cycle. The output-pulse rate is the same as the input rate, which can vary over a range of 1,000:1. This circuit can control device loading, for example, protecting a transistor from being driven beyond its safe dissipation rating.

The key element of the circuit is a 74121 one-shot multivibrator that is triggered by the input pulses. The normal programing resistor for the 74121 is replaced by a transistor that has its effective impedance changed by a feedback loop to maintain the desired duty cycle. The duty cycle is set by a single potentiometer.

As the circuit diagram indicates, the output from terminal 6 of the multivibrator is fed through resistor R_I to the inverting input of a 741 operational amplifier. This voltage, V'_O, is either high (V_H) or low (V_L). Potentiometer R_P sets the noninverting input to a reference potential, V_{REF}, so that the instantaneous current flowing through R_I is equal to $(V'_O - V_{REF})/R_I$. The value of R_I must be chosen so that this current does not exceed the 74121's limit of 400 microamperes. The current causes the feedback capacitor C_I alternately to charge and discharge, resulting in changes of the amplifier-output voltage V_f as a function of time.

If the instantaneous input period is τ and the output duty cycle is α, V'_O is in the high state for a time $\alpha\tau$ and in the low state for $(1 - \alpha)\tau$. The average current $\bar{i}$ through R_I is given by the formula

$$\bar{i}\tau = [(V_H - V_{REF})\alpha\tau + (V_L - V_{REF})(1 - \alpha)\tau]/R_I$$

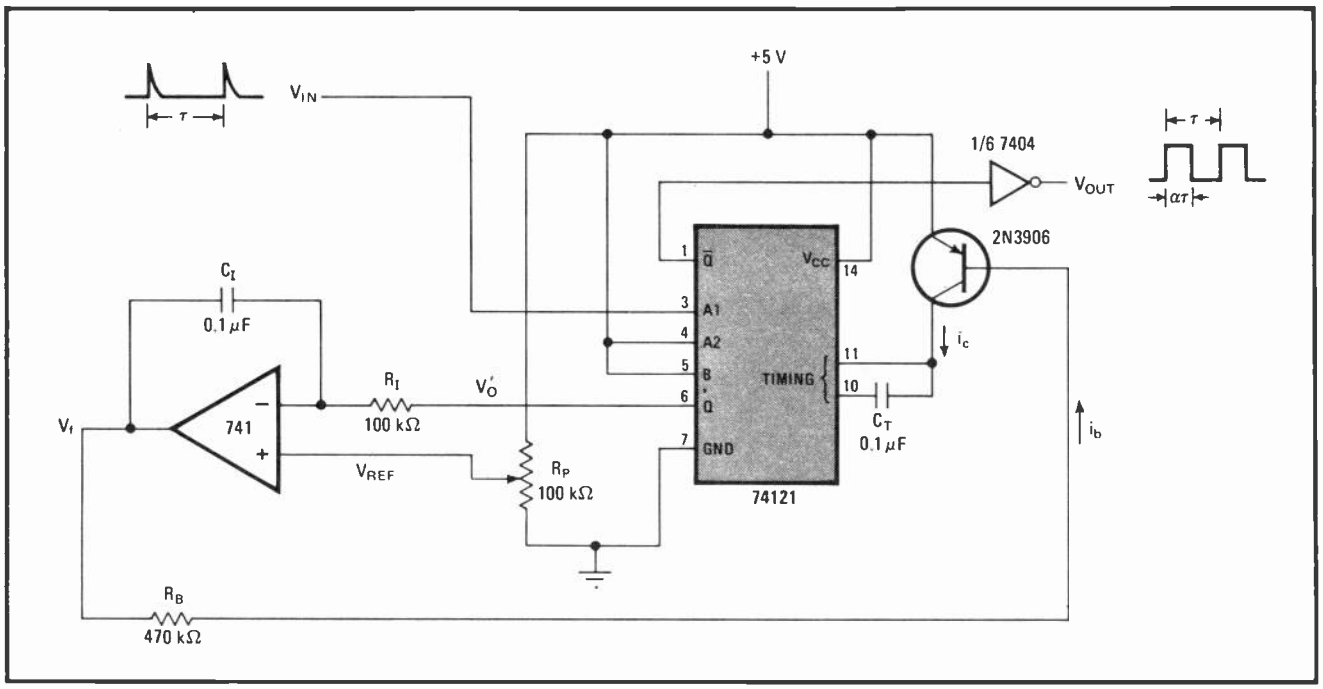
In steady-state operation, when the output waveform has the desired duty cycle α_{set}, the average current to the capacitor must be zero, maintaining a constant operating point from one cycle to the next. Therefore

$$\alpha_{set} = (V_{REF} - V_L)/(V_H - V_L)$$

i.e., the output duty cycle is independent of the input repetition rate $1/\tau$, and depends only on the values of V_{REF}, V_H, and V_L. In general, the values of V_H and V_L are dependent on the output loading. Therefore, to avoid loading problems at the output of the circuit, the output is taken from the $\bar{Q}$ output (pin 1) of the 74121 through an inverting gate (1/6 of a 7404) rather than from the Q output (pin 6).

If the instantaneous α of the circuit is greater than α_{set}, $\bar{i}$ is positive, and the amplifier's output voltage V_f becomes more negative during a complete cycle of operation. Conversely, if α is less than α_{set}, V_f becomes more positive. The time constant for response to such an imbalance is R_IC_I, which should be larger than the longest expected τ in normal operation to minimize the variations in V_f from its average value and ensure that the amplifier does not saturate at any point of the duty cycle. Normally V_f is between -14 v and +6 v.

Voltage V_f controls the base current of the 2N3906 pnp transistor, and thus controls the collector current that charges the 74121 one-shot multivibrator. The ef-



Constant duty cycle. Input to this circuit is a train of fixed-length pulses with variable repetition rate, but op-amp output voltage changes effective transistor impedance to maintain constant duty cycle over a 1,000:1 range of input-pulse frequency. Using the components shown, the on-time of the 74121 monostable can be changed from 30 μs to 30 ms, allowing a 33% duty cycle to be maintained from 10 to 10,000 baud. It is possible to vary the duty cycle all the way from 20% to 80% by the setting of potentiometer R_P.

fect of making V_f more positive is to decrease the base current, $(5 - V_{BE} - V_f)/R_B$, resulting in an increase in the effective resistance of the transistor. Since the duration of the on state is proportional to this resistance, the value of α increases to a value closer to α_{set}. The value of 470 kilohoms for R_B is chosen to limit the maximum collector current i_c to approximately 5 milliamperes, which is consistent with the currents through the programing resistors normally used with the 74121. Assuming a minimum transistor impedance of 500 ohms at the maximum repetition rate, the value of timing capacitor C_T is chosen to determine the length of the on pulse. The maximum value of transistor impedance appears to be about 500 kΩ, so a given choice of fixed components allows a 1,000:1 range of input frequencies.

The analysis of the circuit has stressed the average value of V_f, rather than the instantaneous departures from this value that occur in normal operation of the circuit. This approach is reasonable because the function of the feedback circuit is to supply charge to the capacitance C_T so that the 74121 switches on and off at the correct point of the cycle; the instantaneous variations in current during this charging period are not important in this function.

The operation of the circuit is not critically dependent on the values chosen for R_I, C_I, R_P, or R_B. Neither is it particularly dependent on the bandwidth of the operational amplifier or the linearity of the system in steady-state operation. The input-pulse train must be properly terminated, because reflections at the input can cause the circuit to maintain the required duty cycle with multiple triggering of the 74121. Therefore, a 50-ohm resistor should be hung across the multivibrator input if it is fed through a 50-ohm cable. □

Optocoupler converts ac tone to digital logic levels

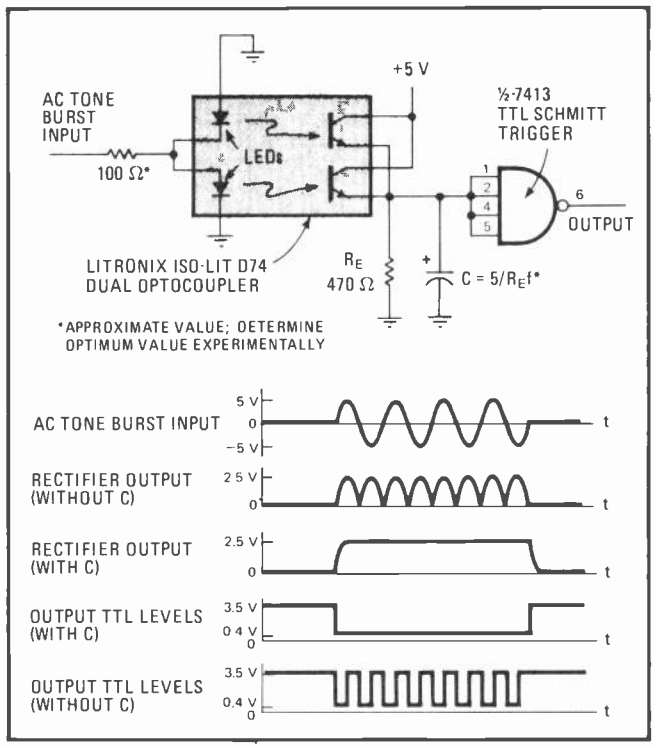
by Louis E. Frenzel
Heath Co., Benton Harbor, Mich.

In some tone signaling, telemetry, and data communications applications, it is necessary to convert an ac tone burst or a few consecutive sine-wave cycles into a logic pulse of the same duration. This can be done by rectifying and filtering the tone burst, then shaping it as required to develop the binary logic levels. In the circuit described here, the rectification of audio-frequency signals is performed by optical couplers—an approach that uses a minimum of components and therefore ensures low cost, high reliability, and small size.

A dual optocoupler using LEDs and phototransistors is connected so that it operates as a full-wave rectifier. The advantage of an optocoupler here is that the usual push-pull ac signal source (center tapped transformer, two op amps, etc.) is not required, considerably reducing the circuit's size, weight, and cost.

The ac tone burst can be applied directly to the LEDs in the optocoupler, as shown, if enough signal power is available. Otherwise, an amplifier can be used; a 741 op amp works well. The two LEDs in the coupler conduct on alternate half-cycles of the ac input, so that a pulsating dc signal is developed across emitter resistor R_E. The transistors in the optocoupler are connected as emitter followers with a common emitter resistor. Capacitor C filters the pulses across R_E into a dc level. The value of C is a function of the size of R_E, the frequency of the tone burst, f, and the size of the load. A capacitance of $5/R_Ef$ is a good starting value, but it should then be adjusted for optimum results.

The dc across R_E and C is shaped by a 7413 TTL Schmitt trigger IC. The output is a clean rectangular pulse with the proper TTL logic levels, as shown in the attached waveforms.



Rectify lightly. Dual optocoupler is full-wave rectifier for ac pulse signals, driving Schmitt trigger to produce rectangular pulses at TTL logic levels. Parts count, cost, size, and weight of circuit are all low; reliability is high. Waveforms show performance and also illustrate frequency-doubler operation of circuit when capacitor is removed.

An optocoupler can be used to advantage in any application requiring full-wave rectification for frequencies well beyond the audio range.

Removing the filter capacitor from the circuit described turns the output into a series of rectangular pulses occuring at twice the frequency of the input. With this minor modification, the circuit performs as a frequency doubler. □

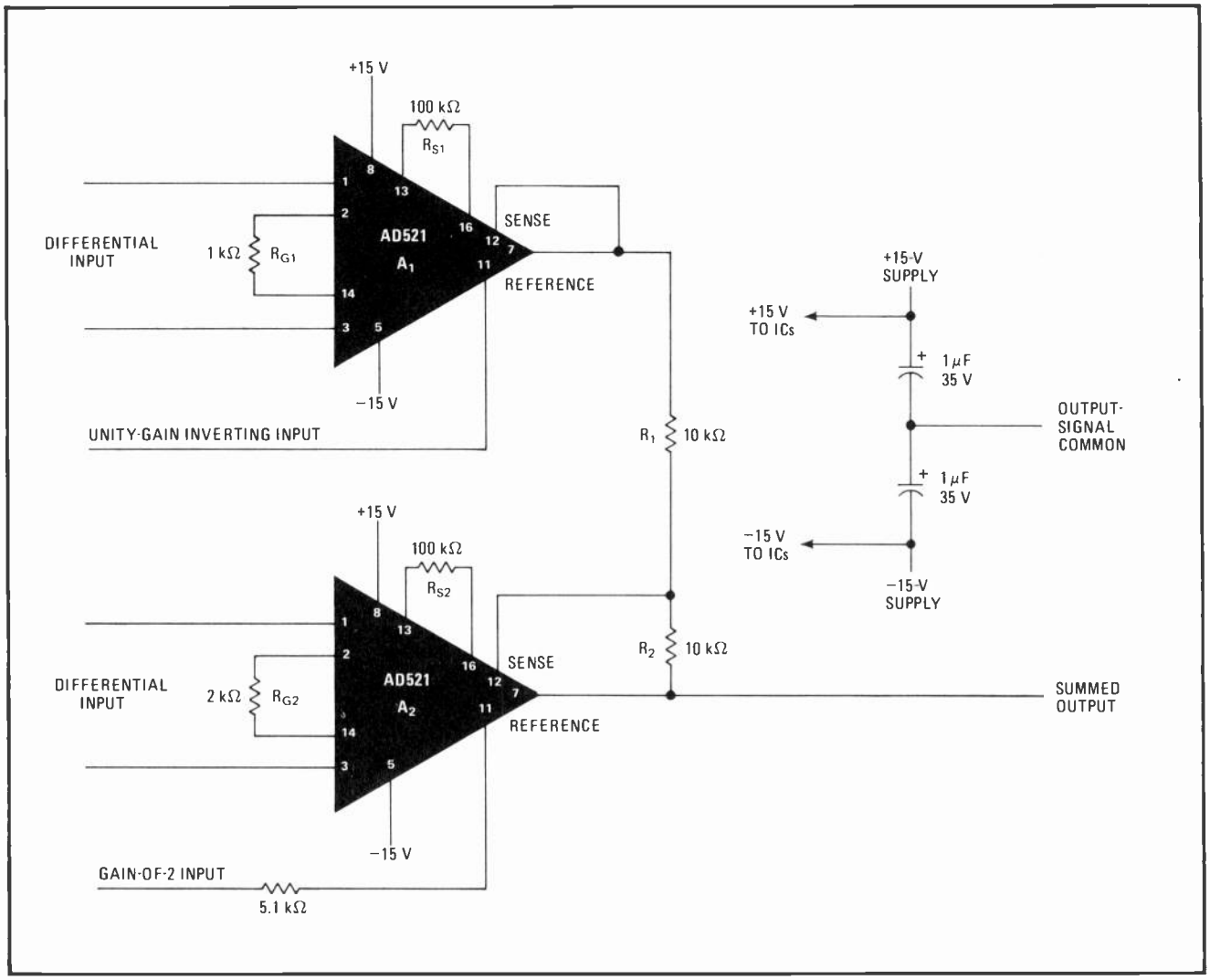
Two instrument ICs sum six inputs

by A. Paul Brokaw
Analog Devices Semiconductor, Wilmington, Mass.

Connecting two IC instrumentation amplifiers (in-amps) as shown produces an amplifier that will sum six input signals. The six inputs may be independent signals that can be added or subtracted to produce a single output. Alternatively, some of the inputs may be paired in the usual fashion, as shown, to yield two floating differential inputs, leaving the remaining two inputs available for independent use. This latter arrangement sums two input signals that lack a common reference or ground, and the two remaining inputs allow the addition of single-ended signals that are referred to the output signal ground.

One example of the use of this technique is to find the difference between the output signals from two independent bridge circuits, then multiply this difference by a gain of 100, subtract a fixed offset voltage, and provide an adjustable zero offset. The output of the summing amplifier can then be used to drive a strip-chart recorder.

This technique surpasses conventional op-amp summing amplifiers that use virtual-ground current-summing techniques. Op-amp summing amplifiers present a relatively low input impedance to input signals, and



Six-pack. Two instrumentation-amplifier (in-amp) ICs can sum six input signals. The six inputs may be either independent signals or pairs of inputs that lack a common reference or ground and form a differential input as shown. The remaining inputs allow the addition of single-ended signals that are referred to the output-signal common. This technique surpasses conventional operational-amplifier summing that uses virtual-ground current-summing; the op-amp adders work only with single-ended inputs and therefore cannot sum independent signals.

moreover, they work only with single-ended inputs and therefore will not sum independent signals.

The output reference terminals of these in-amps can be used as true signal inputs. The output of amplifier A_1 will thus follow signals applied to this high-impedance point. This output represents the sum of the amplified differential input signal and the reference input signal. Since the ratio of resistor R_{S1} to R_{G1} is 100 to 1, the differential input to A_1 is amplified by a gain of approximately 100.

The output sense terminal of amplifier A_2 is used as a separate high-impedance input in an inverting configuration. This terminal closes amplifier A_2's feedback loop. Resistors R_1 and R_2 convert amplifier A_2 into a unity-gain inverter for the output signal from A_1. These resistors also double the gain of A_2 for signals from its differential and reference input. The ratio of A_2's resistors R_{S2} and R_{G2} is 50 to 1, both to compensate for this gain and to balance the contribution from the two differential inputs to the output signal.

The resulting output consists of A_2's differential input amplified by a gain of 100, from which A_1's differential input amplified by 100 is subtracted, A_2's reference input is doubled and added, and A_1's reference input is subtracted.

The gains of the two differential input channels may be modified by changing the value of resistors R_{G1} and R_{G2} to vary the R_S/R_G ratios. The gains of the two reference terminals may also be modified by changing the ratio of the sense feedback resistors (R_1 and R_2). However, this change may reduce the input signal range. The two gains cannot be changed independently.

If a seventh input is desired, the sense feedback loop of amplifier A_1 should be opened and a pair of resistors added. These resistors will provide an extra input, like R_1 and R_2, with a noninverting (actually twice-inverted) gain to the output. Unlike the other six inputs, however, this seventh one will have a relatively low input impedance and will present a variable load that depends upon the upper reference input voltage. □

Touch Tone receiver front end provides agc and filtering

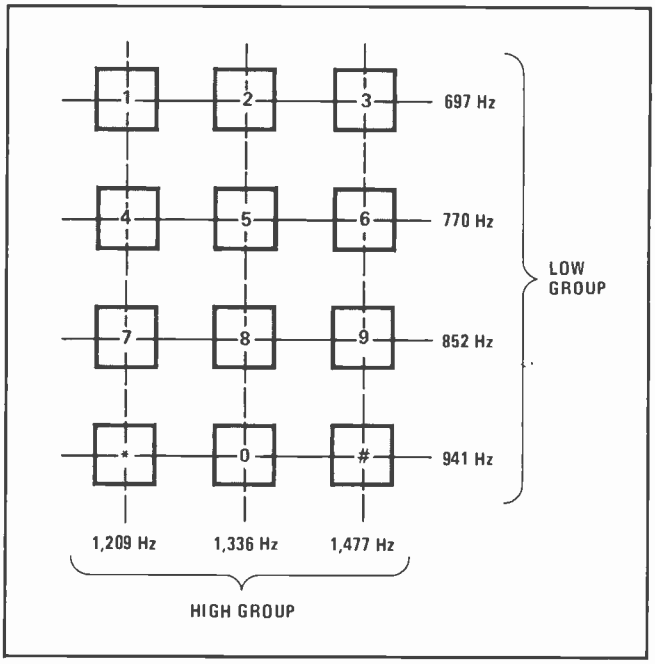
by Jack D. Dennon
Computerphone System, Renton, Wash.

Signals from Touch Tone phone buttons can initiate remotely controlled operations such as turning on a front-door light or entering a sales order in a computer. Such control functions utilize the two-frequency signal that is generated on the phone line when one of the Touch Tone buttons is pushed. As indicated in Fig. 1, one frequency is from the low group (LG), and the other is from the high group (HG). A receiver that measures the two frequencies can respond to a specific button.

Touch Tone receiver circuits can be built inexpensively with either phase-locked-loop tone decoders such as the Signetics 567, or decoders based on active filters using operational amplifiers. For optimum performance from either type of decoder, the receiver should have a front end that consists of an amplifier to provide automatic gain control and high-pass and low-pass filters to separate HG frequencies from LG frequencies.

The simple Touch Tone receiver front end shown in Fig. 2 performs these functions, using only a Norton-type LM3900 quad op-amp and a single complementary-MOS 74C04 hex inverter. The circuit, which uses inexpensive components that are widely available, operates from a single supply voltage of 4 to 15 volts.

The incoming two-tone signal can be taken directly from a line-isolation transformer. It divides across a potentiometer that is set to provide the indicated voltage levels and then is amplified in the automatic-gain-control amplifier and the C-MOS fixed-gain amplifier. Analog operation of the C-MOS digital IC is obtained by biasing the inverting amplifiers to the center of their linear range; the gain is fixed at 2 MΩ/100 kΩ, or 20.

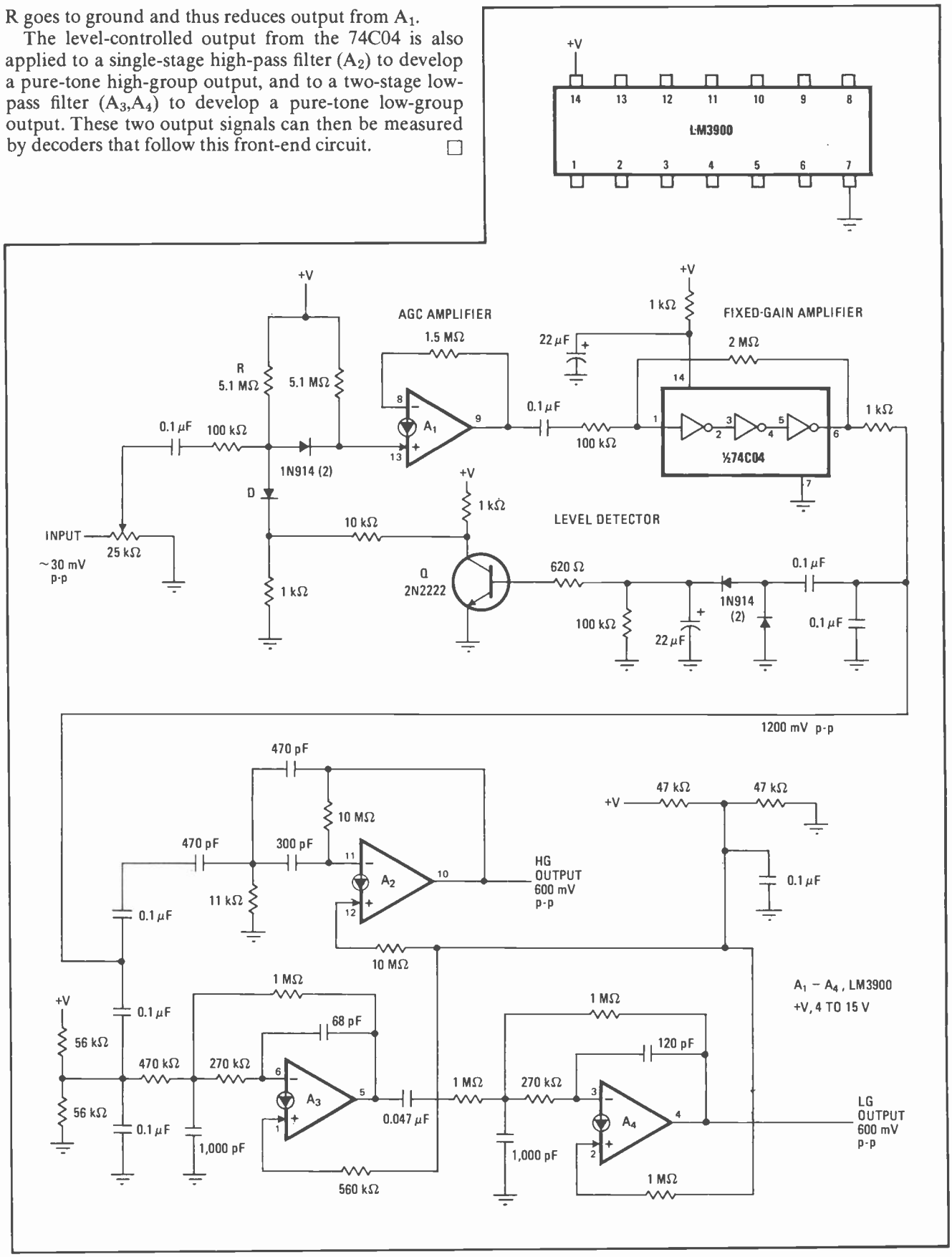


1. Coding. Each button on a Touch Tone phone is identified by the pair of frequencies that is generated when the button is pushed. Four low-group frequencies correspond to the four rows of buttons, and three high-group frequencies correspond to the three columns. To determine which button was touched, the two frequencies are separated in the receiver front end described here and measured in the decoders that follow the front end.

The agc signal that is taken from the output of the 74C04 fixed-gain amplifier is rectified and smoothed to drive transistor Q. The transistor controls the output from the agc amplifier by controlling the bias on diode D. A weak signal into Q back-biases D so that current flowing from the supply through the resistor R is forced into A_1 and produces a large output; a strong signal into Q leaves D forward-biased, so that the current through

R goes to ground and thus reduces output from A_1.

The level-controlled output from the 74C04 is also applied to a single-stage high-pass filter (A_2) to develop a pure-tone high-group output, and to a two-stage low-pass filter (A_3,A_4) to develop a pure-tone low-group output. These two output signals can then be measured by decoders that follow this front-end circuit. □



2. Front-end circuit. The two-frequency signal coming in from a Touch Tone phone is boosted or attenuated to a convenient level in agc amplifier, and then is separated into a low-group output and a high-group output by low-pass and high-pass filters. Only two inexpensive and widely available ICs are required to implement these functions. Many operations can be controlled remotely by the Touch Tone push buttons.

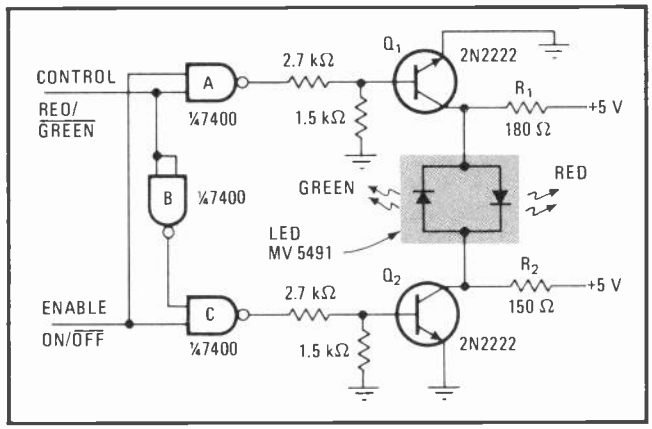
Two-color LED pair is digital status indicator

by Bill Schweber
GTE Sylvania, Needham, Mass.

A red-and-green LED pair in a single package, such as the Monsanto MV 5491, can serve as a status indicator for digital levels with a single supply-voltage circuit. The polarity across the LED is reversed by changing the relative potentials at the two LED terminals, rather than by having one of its terminals at ground and putting positive and negative voltages on the other.

An on/off line enables the entire indicator. Transistors Q_1 and Q_2 serve as LED drivers. When the red/green control line is high (and the enable line is high), the output of gate A is low, turning Q_1 off, while gate C's output is high, so Q_2 is on. Current goes through limiting resistor R_1, and the LED glows red.

When the control line is low, the situation reverses, as does the difference of potential across the LED, which glows green with R_2 limiting current. Note that R_1 and R_2 are of different values because of the different forward drop across the LED, depending on which way it is biased. Pulling the enable line low causes the outputs of gates A and C to go high, so Q_1 and Q_2 turn on, putting both ends of the LED at the same potential; therefore the LED stays off. □



Logic probe. A red-and-green LED packaged pair, such as the Monsanto MV 5491, can serve as a status indicator for digital levels.

C-MOS decade divider clocks bucket-brigade delay line

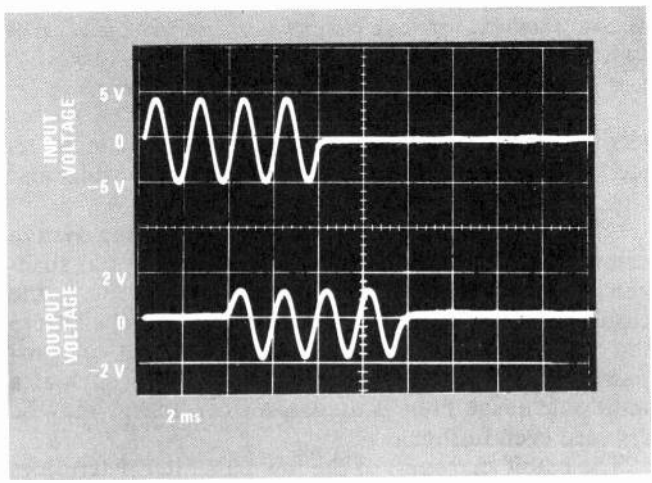
by F.E. Hinkle
The Applied Research Laboratories, University of Texas, Austin, Texas

The bucket-brigade analog shift register is a charge-transfer device that can delay an input signal by a fixed or variable time. A TCA350 MOS bucket-brigade shift register, which has 185 stages, delays the signal by a time $t = 185/2f_c$, where f_c is the clock frequency. The clock frequency must be considerably higher than the signal frequency f_s for sampling and filtering reasons (f_c must be filtered from f_s at the output), so the maximum signal delay is about $10/f_s$. A TCA350 was used to delay 1-kilohertz tone bursts, as illustrated in Fig. 1, for measurements of distortion and insertion loss.

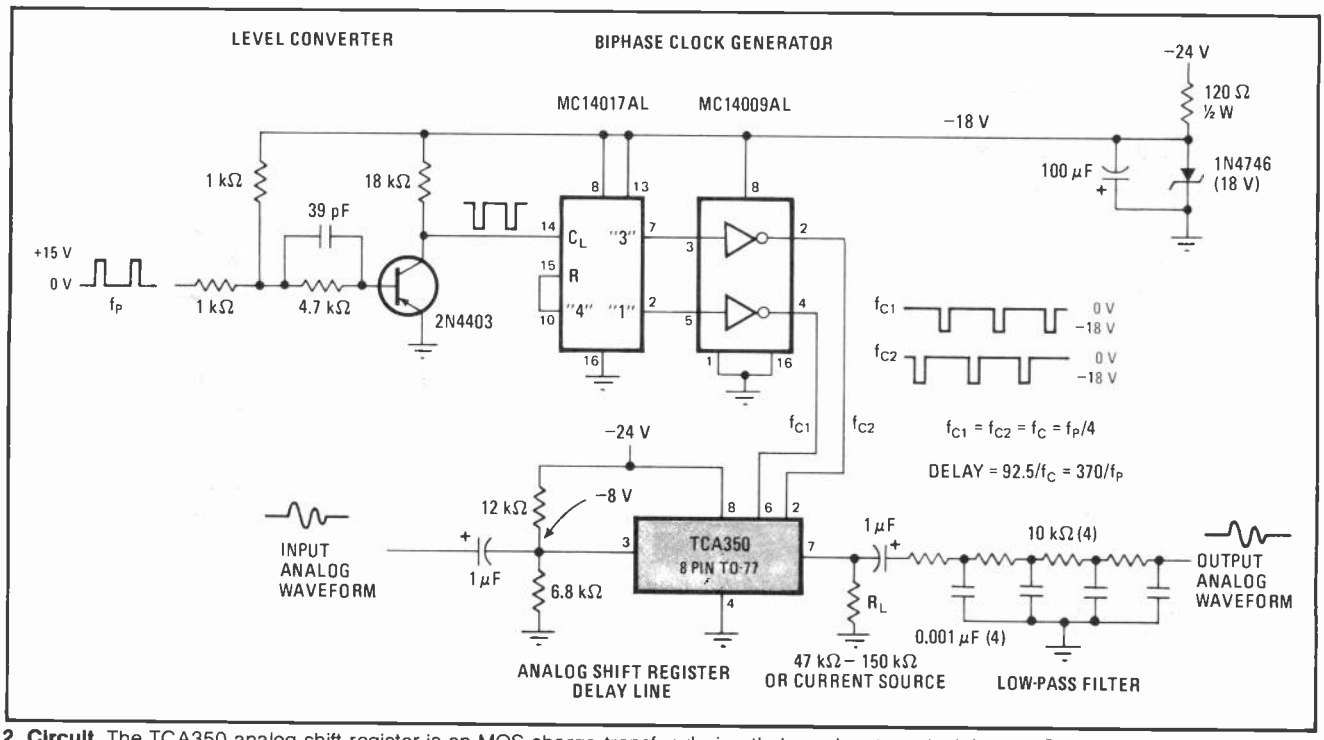
The TCA350 requires two clock-pulse trains of -18 volts; both are at frequency f_c, but they are separated in phase by 180°. [The function of the biphase clock in the charge transfer process is described in *Electronics*, June 21, 1971, p. 58.] A drain supply of -24 V and an input bias voltage of -8 V are also required. Figure 2 shows the circuit for the shift-register delay line, complete with clock generator and output filter.

In this circuit, an externally generated train of positive pulses at frequency f_p is applied to the 2N4403 transistor switch/level-converter, which produces negative pulses suitable for driving the biphase clock generator. The generator, a divide-by-four circuit that uses an MC14017AL C-MOS divider, is biased at -18 V and therefore can drive the TCA350 directly. It generates two non-overlapping pulses at $f_c = f_p/4$, separated by 180°. An MC14009AL C-MOS hex buffer inverts the clock pulses.

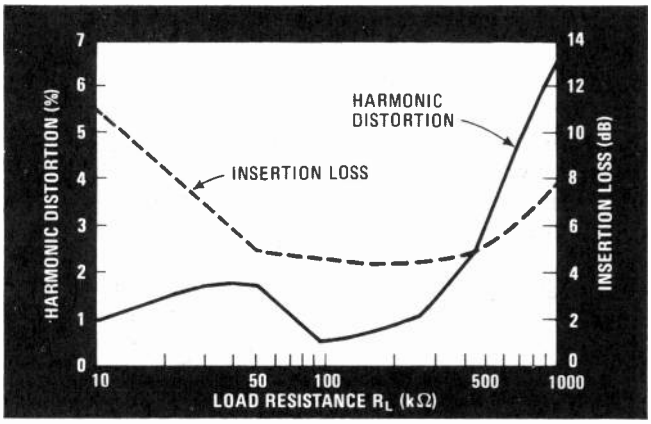
The output from the delay line consists of the delayed input signal superimposed on a clock-generated waveform. The output wave that is generated by the clocking pulses has an rms value of 3 V, and its frequency spectrum is integral multiples of f_c. A filter is needed to re-



1. Delay. Dual-trace scope photo shows 2-millisecond delay of 1-kHz tone burst in bucket-brigade delay line. Output has been filtered to remove clock-frequency components. Delay is inversely proportional to clock frequency; here f_c = 46.25 kHz.



2. Circuit. The TCA350 analog shift register is an MOS charge-transfer device that requires two clock inputs. Clocks of required amplitude and phase relationship are generated by C-MOS divider plus inverters from a conventional input pulse train. Low-pass filter removes clock frequencies from output waveform. Note dc bias at input of delay line. Cascaded shift registers can delay signals for tens of milliseconds.



3. Load carefully. Harmonic distortion and insertion loss in circuit depend upon value of load resistor R_L, as shown. Data assumes that f_s = 1 kHz, f_c = 46.25 kHz, and input signal = 0.77 V rms.

ject the clock frequency and its multiples; the more rejection the filter provides at f_c, the better the wideband signal-to-noise ratio is.

Of course, if f_c is so high that the following system cannot detect it, the filter requirements are not as stringent. For the four-section RC filter shown in Fig. 2, the clock-frequency energy is down about 50 decibels from the maximum allowable output signal within the low-pass filter passband. If a more elaborate filter such as a multipole active filter is used, the clock energy may be reduced even further.

The cutoff sharpness of the low-pass filter determines the maximum amount of delay realizable because a sharp cutoff allows a lower f_c. With the four-section RC filter shown, the maximum delay before signal degradation is about 2 milliseconds. The minimum delay is about 180 μs. The longest practical delay is about 18 ms. With such a long delay, however, the signal is less than 500 hertz. Since the delay changes with clock frequency, the worst-case f_c must be determined when calculating the s/n ratio of the delay line.

The usable dynamic range of the shift register also depends upon the filter response and acceptable s/n ratio. The dynamic range of the shift register is greater than 70 dB when a sharp-cutoff filter is used to remove the clock frequency. The analog shift register tracked within 1 dB as the input signal level changed from 3 V to less than 300 μV. The tracking error was measured in a filter bandwidth of 200 Hz, centered at 2 kilohertz. For input voltages above 3 V rms, the harmonic distortion exceeds 4%. For input amplitude levels of less than 0.5 V rms, the distortion is less than 0.5%. At higher input levels, clipping of signal peaks causes a distortion that is a nonlinear function of the input level.

The output stage of the TCA350 is a source follower that must be terminated in either a load resistor R_L or a constant-current load of about 0.5 milliampere. The relationship between harmonic distortion and load resistance is shown in Fig. 3; note that there is an optimum value for R_L. The distortion curve reflects a 0.2% distortion in the input signal plus the nonlinearity of the bucket brigade. If a current source is used in place of the load resistor, the current should be adjusted for minimum distortion.

Figure 3 also indicates that the attenuation of the input signal varies between 4 and 11 dB as the size of the load resistor is changed. □

Outputs of op-amp networks have fixed phase difference

by Richard K. Dickey
California Polytechnic State University, San Luis Obispo, Calif.

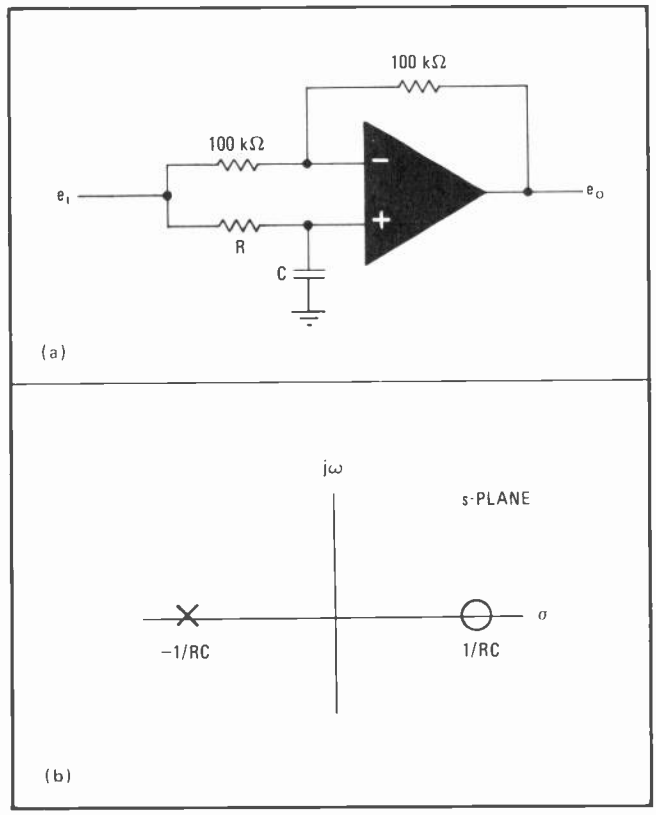
In the phasing method of single-sideband generation, two modulating signals are derived from the audio input. The two signals must have equal amplitudes, but must differ in phase by 90° at all frequencies in the audio band. A differential-phase-shift system that provides these two signals can be made from resistors, capacitors, and operational amplifiers.

The basic section of the constant-phase-shift system is the op-amp circuit shown in Fig. 1. The transfer function of this circuit is

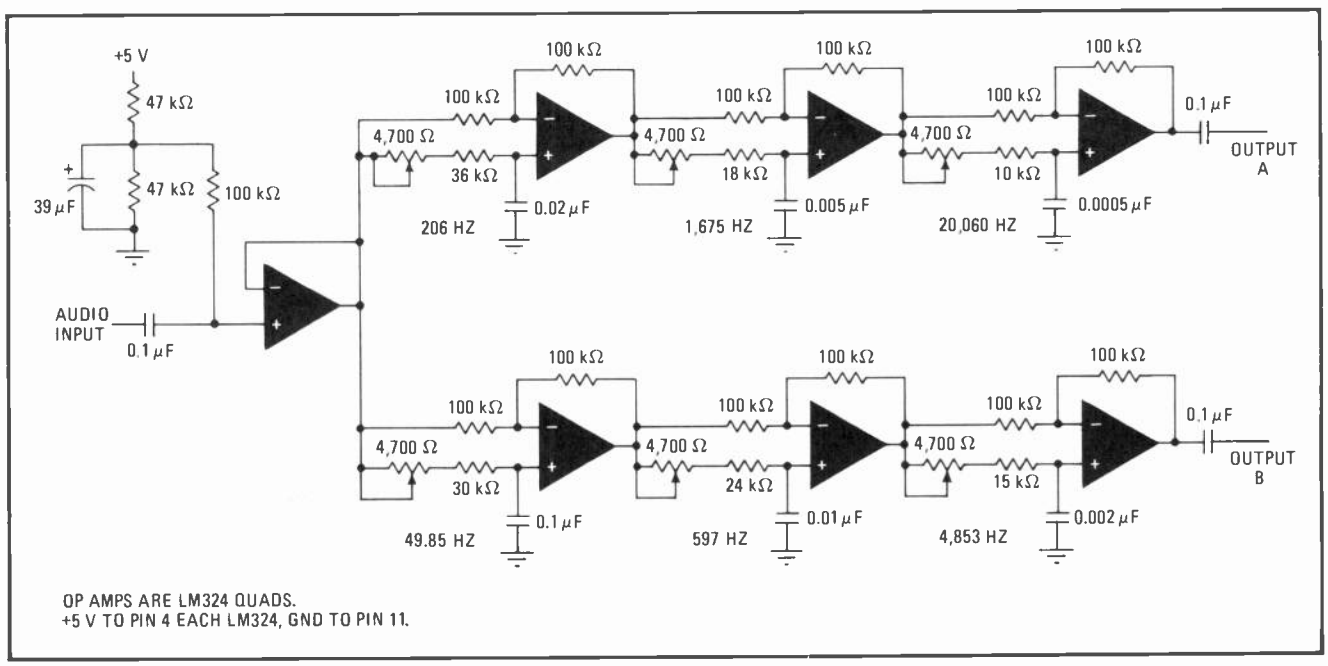
$$e_o/e_i = (1 - j\omega RC)/(1 + j\omega RC)$$
$$= 1 \angle -2 \arctan \omega RC$$

Thus the gain is always unity, and the phase shift decreases from 0 to −180° as frequency increases from zero to infinity. The shape of the phase-shift curve depends upon the time constant RC, i.e., upon the locations of the singularities in the s-plane plot that is included in Fig. 1.

If three of these basic sections are cascaded, the over-all gain remains constant at unity, and the over-all phase shift through the network falls from 0 to −540° at



1. Basic section. Op amp connected as shown (a) is a unity-gain phase shifter. Singularities of circuit are shown (b) in s-plane plot. Phase shift ranges from 0 at dc to −180° at infinite frequency; however, gain is unity at all frequencies.



2. Quadrature. Differential phase shifter converts audio-frequency input signal to two outputs, 90° out of phase, for SSB modulation. Simple transformerless circuit uses quad op amps driven by a single-ended 5-volt supply. The individual sections are adjusted for 90° phase shift at the frequencies indicated on the figure; the two outputs are then in quadrature to within 2° from 100 Hz to 10 kHz.

a rate that is determined by the three RC products.

Two such phase-shift networks, fed from a common input (as shown in Fig. 2), can be designed so that the phase shift through one lags behind the phase shift through the other by 90° over a substantial frequency range. The time constants are chosen so that the singularities of the two networks interlace.

The all-pass system in Fig. 2 provides two equal-amplitude outputs that differ in phase by (90 ± 2)° over the frequency interval from 100 hertz to 10 kilohertz. The various R and C values were calculated from the table published by S.D. Bedrosion, "Normalized Design of 90 Degree Phase Difference Networks," IRE Transactions on Circuit Theory, June 1960, pp. 128–136. In each section, RC = $\frac{1}{2\pi f}$, where f is the 90° frequency for that section as shown in Fig. 2. An exception is the 20,060-Hz stage, where R was decreased to compensate for the inherent phase shift in the op amp.

Each section of each network should be individually adjusted to an exactly 90° phase shift at the indicated frequency. This adjustment can be made by connecting the input and output of that section to the horizontal and vertical inputs of an oscilloscope, and then varying the 4,700-ohm potentiometer until the Lissajous figure is a circle. Alternatively, a phasemeter can be used.

Each op amp is one quarter of an LM324 quad amplifier. The input biasing network allows operation from a single 5-volt supply. □

Linear pot and op amp provide tapered audio volume control

by Robert C. Moore
Applied Physics Laboratory, Johns Hopkins University, Silver Spring, Md.

Tapered potentiometers are used in audio amplifiers to compensate for the nonlinear response of the human ear. However, at a lower cost, a linear potentiometer and an operational amplifier can approximate the response of the tapered pot.

The audio taper for potentiometers is described by the gain function

$$V_{out}/V_{in} = f(\alpha) = 10^{2(\alpha-1)}$$

where the potentiometer displacement α can range from $\alpha = 0$ (in the full counter-clockwise position) to $\alpha = 1$ (in the full clockwise position). Signal attenuation through the potentiometer can be expressed in decibels as

$$Attenuation = 20\log(V_{in}/V_{out}) = 40(1-\alpha)\ dB$$

This expression shows that the attenuation in decibels is proportional to the potentiometer displacement from the full clockwise position. To obtain this reverse-logarithmic-gain function, special nonlinear potentiometers are usually used.

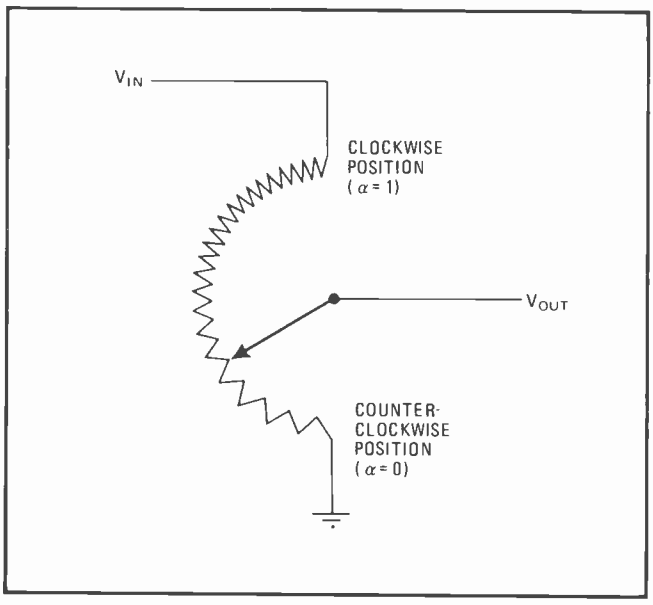
Because these potentiometers cannot be loaded heavily without distorting the gain function, in practical audio applications they are usually followed by a gain stage or a high-input-impedance voltage follower. However, the reverse-logarithmic-gain function can be closely approximated by using a linear potentiometer, a single operational amplifier, and one fixed resistor, as shown in Fig. 2. The operational amplifier adds the capability of voltage gain; in this circuit the maximum voltage gain is 8, or 18 dB. The voltage-transfer function for the circuit of Fig. 2 is

$$V_{out}/V_{in} = (-8\alpha)/(9-8\alpha)$$

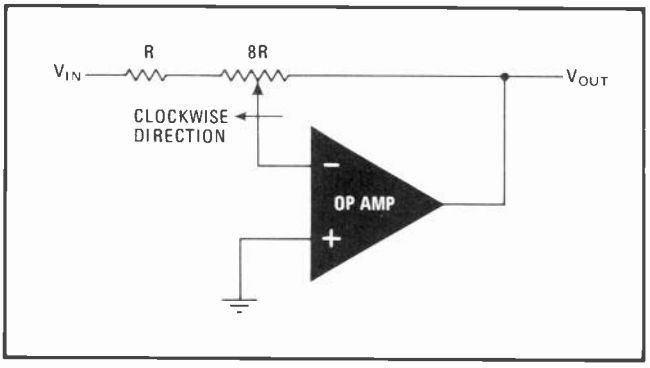
which closely approximates the attenuation function

$$Attenuation = 40(1-\alpha) - 18\ dB$$

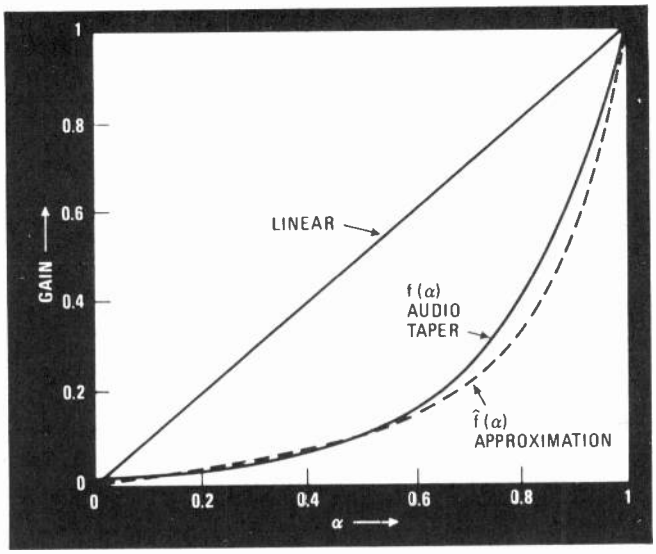
over most of the range of α. As a desirable advantage,



1. Audio taper. Volume-level potentiometer for sound systems has tapered resistivity to compensate for exponential response of human ear. Expensive tapered pot (which should be followed by a buffer stage to prevent loading effects) can be replaced by a linear pot, fixed resistor, and op amp.



2. Replacement. Linear potentiometer, fixed resistor, and operational amplifier, connected as an inverting amplifier, provide transfer function that approximates performance of audio-taper pot plus 18 dB of gain. The minimum input impedance is R.



3. Comparison. Approximation to audio taper is excellent for potentiometer-displacement values α below 0.5 and good everywhere else. The approximation is exact at $\alpha = 0.5$.

the attenuation goes to infinity at $\alpha = 0$.

The transfer function of the circuit in Fig. 2 is normalized to

$$\hat{f}(\alpha) = \alpha/(9 - 8\alpha)$$

and compared to the true audio taper in Fig. 3. The approximation, which is good everywhere, is especially close at the low values of α, where compensation for the reduced hearing sensitivity at low sound levels is most important. The two functions agree exactly at $\alpha = 0.5$.

Because it uses a linear potentiometer, this circuit is less expensive than the normal audio-taper level-control, and it is much more convenient to use in new designs.

The value of R can easily be chosen to suit the op-amp and the circuit impedance; for example, a 100-kΩ pot and a 12.4-kΩ fixed resistor can be combined with a 741 op amp. □

ECL tuned oscillators are voltage-stable

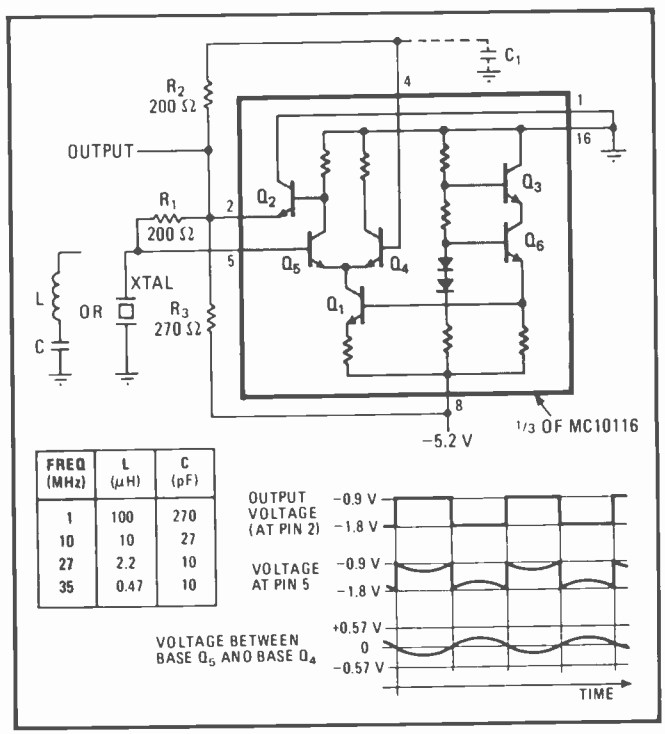
by Tom Hornak
Hewlett-Packard Co., Palo Alto, Calif.

A simple square-wave crystal oscillator or LC oscillator can be built by using one third of an MC10116 integrated circuit, which is a triple differential amplifier in the MECL 10,000 series. It has better frequency stability than a similar oscillator that uses a resistor and capacitor as the frequency-determining elements [*Electronics*, May 29, p. 106]. A 1-volt variation in supply voltage to the RC oscillator caused fractional frequency changes ranging from 0.09 at 10 megahertz to 0.02 at 50 MHz. The same voltage variation changes LC oscillator frequencies of 1, 10, 27, and 35 MHz by less than 0.003; and crystal oscillator frequencies of 10 and 20 MHz are changed less than 5×10^{-6}.

Details of the tuned oscillators are shown in the figure. Transistors Q_1, Q_4, and Q_5 form a differential amplifier. The output signal supplied by emitter follower Q_2 is fed back via resistors R_1 and R_2 to the bases of Q_4 (positive feedback) and Q_5 (negative feedback). If no crystal or LC combination is connected to the bases of Q_4 and Q_5, the feedback signals cancel each other because of the high common-mode rejection of the differential amplifier, and the circuit is thus quiescent.

When an LC circuit or a crystal is connected between the base of Q_5 and ground, the negative-feedback signal is attenuated by the divider consisting of R_1 and the low impedance of the LC circuit or crystal at the series-resonant frequency. Because positive feedback dominates, the circuit oscillates.

The top waveform represents the oscillator's output



FREQ (MHz)	L (μH)	C (pF)
1	100	270
10	10	27
27	2.2	10
35	0.47	10

Stable. ECL-oscillator frequency, determined by crystal or LC tank circuit, is insensitive to variations in supply voltage. Capacitor C_1 balances stray capacitances (e.g. from crystal holder) that might cause parasitic oscillations; its value is $(R_1/R_2)C_{stray}$.

voltage, i.e. a square wave alternating between ECL logic levels. The middle waveform displays the idealized signal on the base of Q_5, i.e. the output square wave with its fundamental frequency component attenuated by the divider. The bottom waveform represents the difference between the other two waveforms, which is the voltage acting between the bases of Q_5 and Q_4. This voltage, clipped and amplified by the differential amplifier, constitutes the oscillator output voltage. □

Phase-sequence detector trips circuit breaker

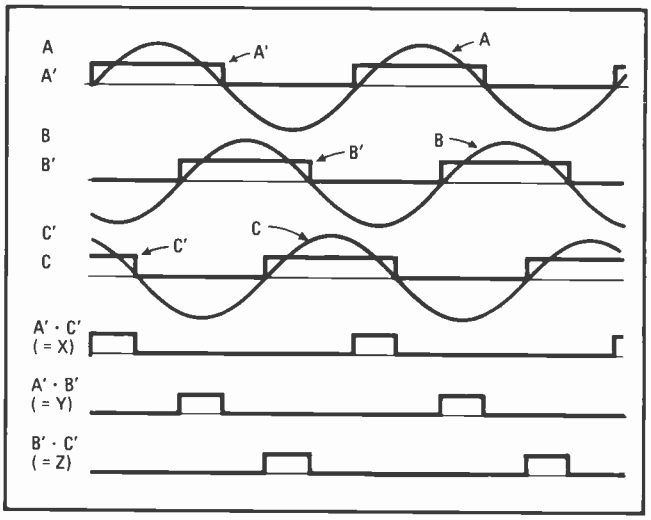
by Terry Malarkey
Motorola Semiconductor Products Inc., Phoenix, Ariz.

Some three-phase line-powered equipment is sensitive to the direction of rotation of the three phases. For example, if two of the connections to a three-phase motor are inadvertently reversed, the motor will reverse direction—a disaster if the motor is used to drive a pump or the compressor of an air conditioner. To guard against this failure, a low-power circuit can be built from standard complementary-MOS components that will detect the phase inversion and trigger a circuit breaker. Moreover, the circuit, which interfaces directly with C-MOS logic, can be appended easily to a line-undervoltage or line-unbalanced detector.

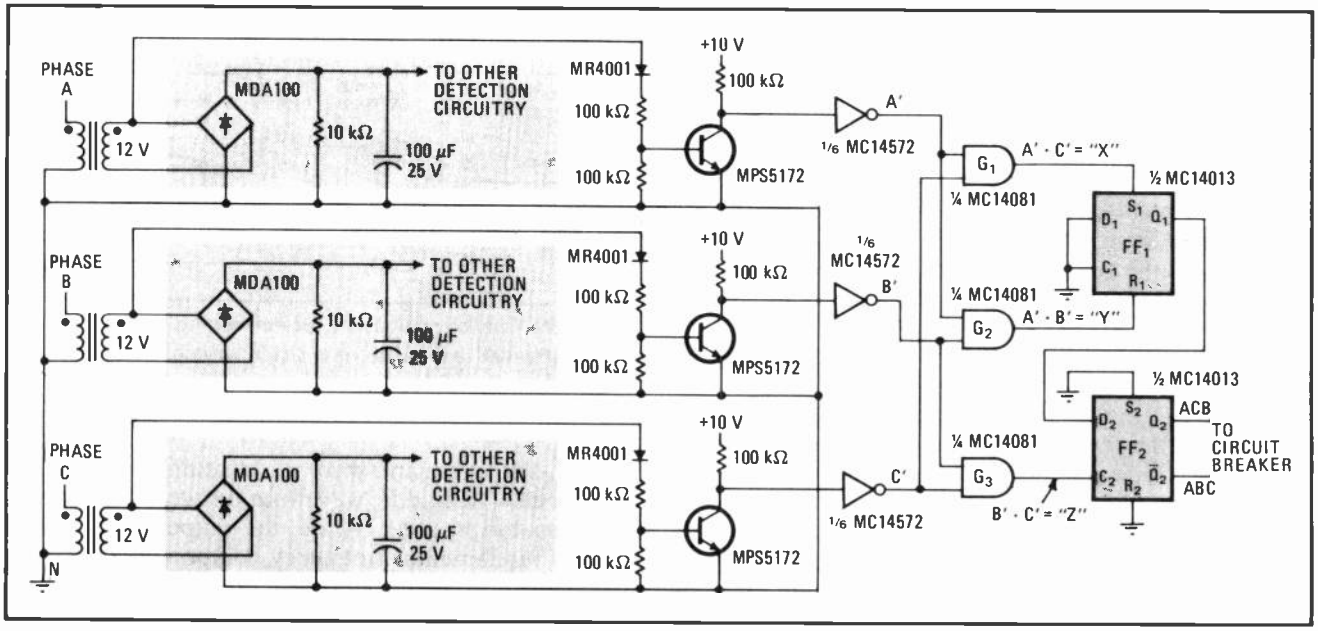
In the circuit (Fig. 1), the line voltages are stepped down and isolated by control transformers. The sine waves for phases A, B, and C are half-wave-rectified and shaped by the MR4001 diode and MPS5172 transistor, and shaped again by a C-MOS inverter. The resulting rectangular waveforms are shown as A′, B′, and C′ in Fig. 2.

The shaped outputs A′, B′, and C′ are now combined with one another in the AND gates G_1, G_2, and G_3, to produce the waveforms A′·C′, A′·B′, and B′·C′ (or X, Y, and Z in Fig. 2). The pulses X, Y, Z appear sequentially; this sequence will change to YXZ if, for instance, the B and C phases are interchanged.

The X, Y, and Z pulse trains are applied to D-type flip-flops FF_1 and FF_2 in such a way that the $\bar{Q}_2$ output of FF_2 is high if the sequence is XYZ (i.e., if the line phase sequence is ABC), and $\bar{Q}_2$ is low if the sequence is YXZ. For the XYZ sequence, an X pulse sets Q_1 and D_2 high, but then the Y pulse resets Q_1 and D_2 low. The Z pulse then clocks the low from D_2 to Q_2, making $\bar{Q}_2$ high.



2. Operation. Line phases A, B, and C are rectified and shaped to produce waveforms A′, B′, and C′. Overlaps of these rectangular waves produce AND-gate outputs A′·C′, A′·B′, and B′·C′; for convenience these outputs are referred to as X, Y, and Z. Line-phase sequence ABC generates XYZ; sequence ACB generates YXZ. These pulse trains cause flip-flop outputs to signal any phasing error.



1. Phase insurance. Incorrect sequence of line phases is detected by flip-flops, which trigger circuit breaker to prevent three-phase motor from running in reverse. Phase sequence ABC makes $\bar{Q}_2$ high, but sequence ACB makes Q_2 high; either output can be used to control protection devices. This phase-reversal detector can be a simple addition to other control circuitry, as shown here.

Either Q_2 or $\bar{Q}_2$ can be used to trip a circuit breaker via a solid-state or electromechanical relay, and thus pull a valuable piece of equipment off the line before it is damaged.

The MDA100 bridge rectifier, 10-kilohm resistor, and 100-microfarad capacitor, shown in the gray area of Fig. 1, are representative of typical applications requiring line-voltage detection. They are included in Fig. 1 to demonstrate how easily the phase-sequence detector can be added to other detection circuitry. They can, of course, be omitted; and the "bottom" of the transformer can be connected directly to circuit ground. □

Single preamplifier/isolator drives lf and vlf receivers

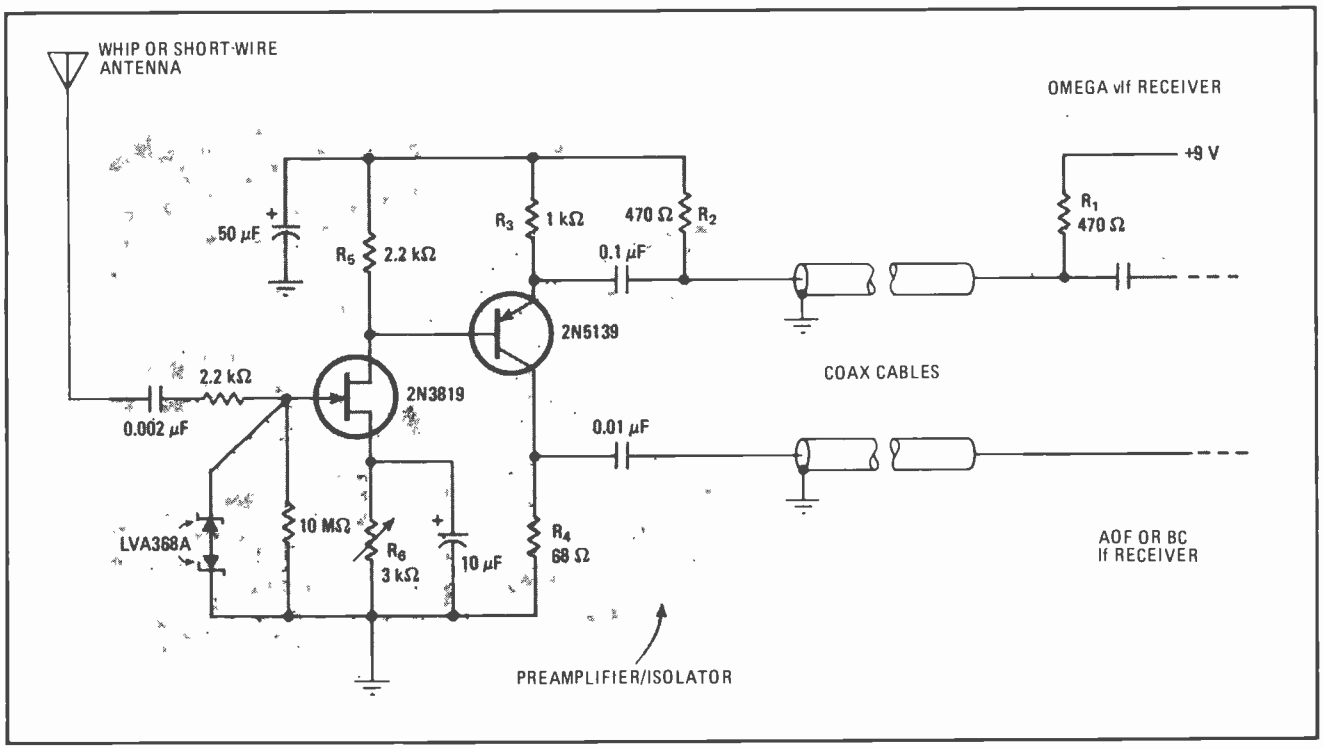
by R.W. Burhans
Ohio University, Athens, Ohio

Some rf front-end circuitry proposed for Omega receivers [*Electronics*, Sept. 5, 1974, p. 98] has now been used in several flight tests of simplified vlf navigation for general aviation. The results showed that the first-stage MOSFET occasionally burned out in the presence of very close lightning discharges, and that a common antenna, such as the automatic direction finder sense whip, should be used for both the Omega navigation receiver and the ADF receiver.

Corrections for both problems are made in the circuit of Fig. 1. The MOSFET has been replaced by a low-cost junction FET that provides a gain of 2 or 3 and adequate low-noise performance over the frequency range from 5 to 1,500 kHz. An expensive wideband line-isolating transformer used in the original preamplifier has been eliminated by using a simple resistor divider string (R_1, R_2) to carry power to the preamplifier and signal output to the Omega receiver over a single cable. A small resistor in the collector lead of the 2N5139 output emitter-follower provides a unity-gain buffer output for driving an ADF or broadcast-band receiver from the preamplifier at a low impedance level through a separate cable. Isolation between the vlf receiver (10–100 kHz and the ADF/broadcast-band receiver (200–1,500 kHz) is completely satisfactory.

The 2N3819 JFET is much less likely than a MOSFET to burn out with static charges, and the back-to-back zener diodes give gross protection from high-level short-duration burst interference. The atmospheric 5–1,500-kHz noise level is usually a limiting factor in high-output-impedance preamplifiers of this sort, so an ultra-low-noise MOSFET is not required.

Adjustment of source-bias resistor R_6 centers the operating point for equal positive and negative peak clipping on large signals. The circuit can handle input signal levels up to 0.1 volt rms before round-off distortion of the output waveform begins. For unity gain at the lf terminal, the ratio of R_4/R_3 is approximately B × A, where B is the current gain of the 2N5139 stage and A is



Dual-purpose front end. Preamplifier/isolator circuit, fed by a single antenna, drives a vlf navigation receiver and an lf broadcast-band or automatic-direction-finder receiver. The two receivers are connected to the preamp by separate coaxial cables that can be as long as 100 feet. Circuit is designed for small general-aviation aircraft, so size, weight, and cost are minimized and ruggedness is emphasized.

the gain of the 2N3819 stage. A gain of 2 or 3 at the vlf output is desirable to drive the additional filters and limiting amplifiers in the Omega receiver.

This isolating preamplifier can also be used in ground-station monitors with a single wire antenna driving two receivers, such as a WWVB 60-kHz time reference plus 100-kHz Loran C, or an Omega plus Loran C, and so forth. One of the receivers must supply power to the preamplifier, as shown in the figure. The upper frequency is limited to 1,500 kHz by the low-cost JFETs; somewhat higher-frequency performance might be achieved with JFETs such as the 2N4416. □

Unity-gain stage is 50-ohm driver

by William A. Palm
Control Data Corp., Minneapolis, Minn.

A recurring problem for the circuit designer is the connection of his op amp, his oscillator, or his test instrument to the low-impedance outside world. The simple buffer-driver shown here provides unity-gain class A operation, high input impedance, and 50-ohm output impedance over a wide frequency range. It also provides blast-out (short-circuit) protection and can be built with a single IC.

Because the base-to-emitter voltages of transistors Q_1 and Q_2 cancel each other, the dc voltage between input and output is near zero. With 2N2222 and 2N2907 transistors, actual offset voltage will run from 0 to 50 millivolts. This offset can be balanced out by adjustment of resistor R_5.

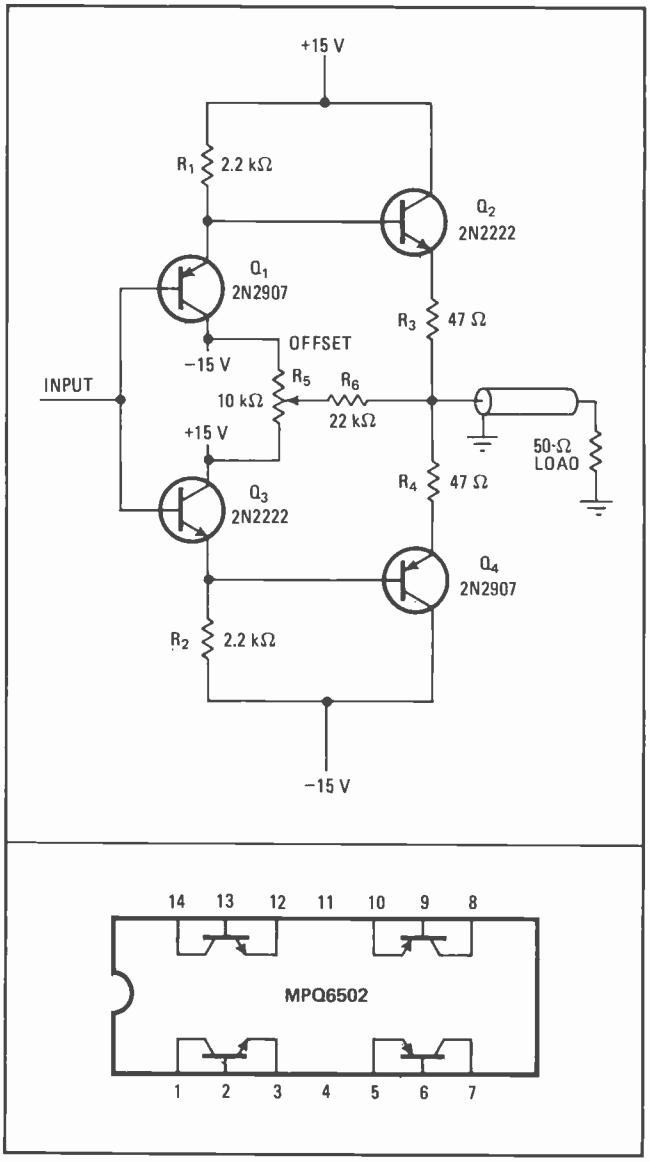
With ±15-V supplies and the resistor values shown, this driver will deliver 10 V peak to peak, undistorted, into a 50-ohm load. Without the external load, the output will double to 20 V p-p. For total circuit protection against a shorted output and dc inputs, resistors R_3 and R_4 should be rated at 4 watts. The circuit draws about 17 milliamperes in the quiescent state.

Actual supply voltages are not critical. Resistors R_1 and R_2 can be changed for the appropriate drive to accommodate any supply voltages from ±5 V to ±20 V. For ±5-V supplies, R_1 and R_2 should be 680 ohms.

The input impedance of the circuit is a function of the gains of the transistors used. For transistors with h_{FE} between 50 and 100, the input impedance is in the range from 50 to 100 kilohms at 1 kHz and decreases to 25 to 50 kilohms at 1 MHz. This impedance is normally high enough to offer imperceptible loading on op amps. Even a 2-kilohm potentiometer, used as an amplitude adjuster, sees only a 4% loading from low frequencies to 1 MHz.

For the circuit shown, the driver has a bandwidth of about 10 MHz when the source has an impedance of 1 kilohm. With a source impedance of 50 ohms, the frequency response is greater than 10 MHz.

A convenient means of packaging this circuit is the MPQ6502 complementary quad shown in the inset. The MPQ6502 has two 2N2222 (npn) and two 2N2907 (pnp) transistors in the handy 14-pin dual-in-line package. □



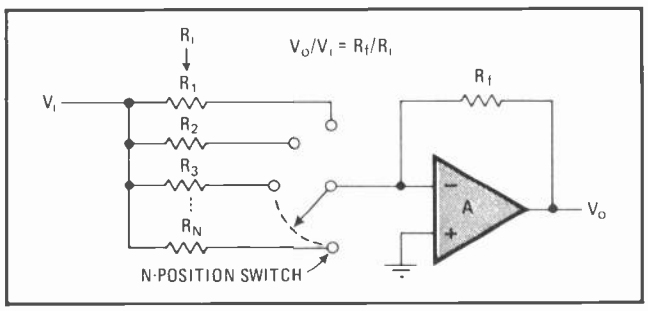
Driver delivers. Unity-gain driver has zero offset, delivers 20 V p-p into an open circuit, or 10 V p-p into a 50-ohm load. Useful as output for op amps and test instruments, it has high input impedance, good frequency response, and low current drain. Supply voltages are not critical. The four transistors are packaged in an MPQ6502 IC.

Combination logic cuts parts in digitally controlled amplifier

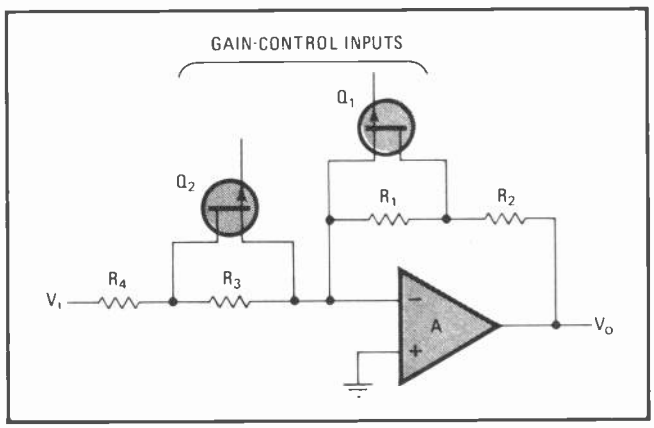
by Reinhard Metz
Bell Laboratories, Naperville, Ill.

Measurements on communications and transmission systems often require circuits that permit digital control of amplification or attenuation. These circuits may require many components when many different levels of amplification are required. However, N levels can be realized by using approximately $\log_2 N$ components in various combinations, instead of using N components without forming combinations.

A circuit arrangement that uses N different resistors to provide N different values of amplification (or attenuation) is shown in Fig. 1. The gain of the inverting operational-amplifier stage is equal to the ratio of feedback resistance, R_f, to input resistance, R_i. Here a different R_i is switched in for each desired level of gain.



1. Controllable gain. Ratio of feedback resistance to input resistance in op-amp circuit determines gain. Here N different values of R_i provide N different values of amplification (or attenuation).



2. Combinations control. Control voltages on two FETs switch R_1 and R_3 in or out of circuit in four possible combinations, providing four different values of gain. These values of gain, when expressed in dB, obey a simple rule: the sum of the highest and lowest is equal to the sum of the middle two. An amplifier can therefore be designed to provide equal increments of dB gain (or loss).

The technique of using various combinations of a set of resistors is shown in its basic form in Fig. 2. Using one op amp and four resistors, but only two field-effect transistors, this stage provides four digitally controllable gain values. The four on- and off-state combinations of the control inputs to the two FETs determine four possible values for the ratio of feedback resistance to input resistance in the inverting amplifier configuration, and thus determine the four values of gain and/or loss. The sources of the FET are at virtual ground, and therefore signal fluctuations cannot affect their on-off states. Also, no switch-drive decoding is required because there are already only two switches for four levels.

The four values of amplification or attenuation through the circuit in Fig. 2 obey a useful relationship: if a, b, c, and d are the gains or losses expressed in decibels, the sum of the highest and lowest is equal to the sum of the other two. To demonstrate the relationship, let

$$a = 20 \log \frac{R_1 + R_2}{R_4}, \text{ or } \frac{R_1 + R_2}{R_4} = 10^{a/20}$$

$$b = 20 \log \frac{R_1 + R_2}{R_3 + R_4}, \text{ or } \frac{R_1 + R_2}{R_3 + R_4} = 10^{b/20}$$

$$c = 20 \log \frac{R_2}{R_4}, \text{ or } \frac{R_2}{R_4} = 10^{c/20}$$

$$d = 20 \log \frac{R_2}{R_3 + R_4}, \text{ or } \frac{R_2}{R_3 + R_4} = 10^{d/20}$$

Multiplying the first equation by the last yields

$$\frac{R_1 + R_2}{R_4} \quad \frac{R_2}{R_3 + R_4} = 10^{(a+d)/20}$$

and multiplying the second equation by the third yields

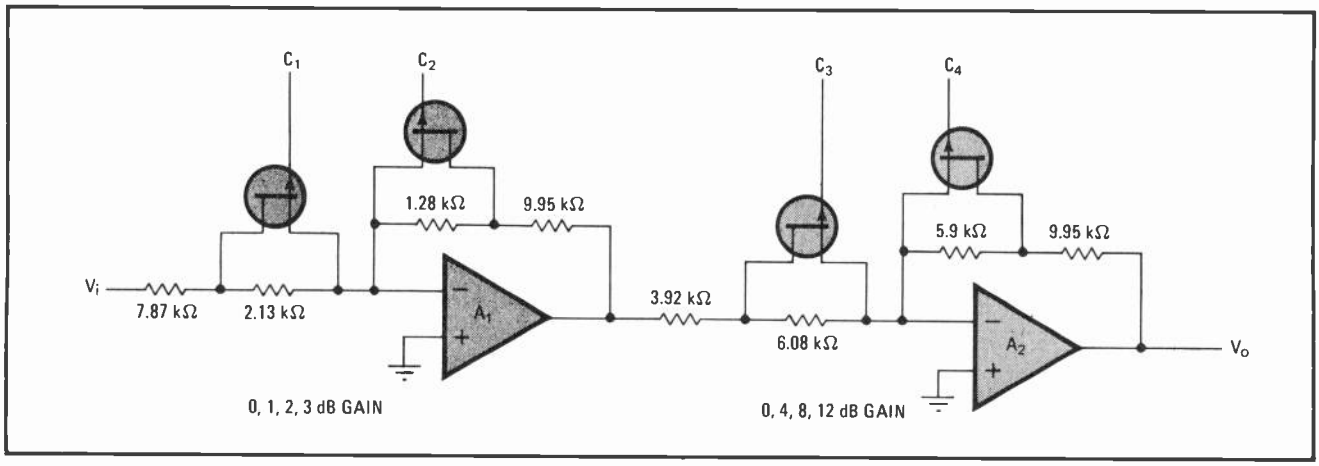
$$\frac{R_1 + R_2}{R_3 + R_4} \quad \frac{R_2}{R_4} = 10^{(b+c)/20}$$

The left sides of these two expressions are equal, and therefore

$$10^{(a+d)/20} = 10^{(b+c)/20} \text{ or } a + d = b + c$$

Thus, for any set of resistors R_1, R_2, R_3, and R_4, the sum of the highest and lowest gains or losses (expressed in dB) is equal to the sum of the middle two. In particular, this relationship is satisfied by any "symmetrical" set of gains, such as 0, 1, 2, 3 dB, or −10, −5, +5, +10 dB. Also, any equal-stepped set of gains or losses is symmetric.

A cascade of s stages, controlled by only 2s digital inputs, can extend controlled amplification/attenuation to any desired set of 4^s symmetrically spaced dB steps. Figure 3 shows a two-stage amplifier in which the gain is adjustable from 0 to 15 dB in 16 1-dB steps. The values of the resistors are calculated directly from the



3. More steps. Cascade of two symmetrically stepped stages provides 4^2 values of gain, with only 2 × 2 control terminals. Levels in each stage are chosen so that gain is adjustable from 0 to 15 dB in 16 1-dB steps. More generally, cascading s stages, controlled by only 2s digital inputs, can provide any desired set of 4^s symmetrically spaced steps of dB amplification or attenuation.

equations for a, b, c, and d, with the unity gain (0 dB) set at

$$\frac{R_3+R_4}{R_2} = \frac{10\,k\Omega}{10\,k\Omega} = 1$$

The approximately 50-ohm on resistance of a FET is taken into account by increasing the R_4s and R_2s, and decreasing the R_1s and R_3s from the calculated values.

Although Figs. 2 and 3 show 4^s different values of gain, where s is the number of stages, 2^s can be easily achieved by including one stage with only two values of gain if one value of gain in each stage is 0 dB. □

Bilateral current source is digitally programable

by Andrew Olesin
Soltek, Montrose, Colo.

Engineers use adjustable current sources for measuring device characteristics such as transistor beta or diode-breakdown voltage. To automate the procedure, a digitally controlled current source that can be programed for currents of ±1 nanoampere to ±1 milliampere can be made from two operational amplifiers and a multiplexer. The digital inputs can be directly driven by transistor-transistor logic or complementary-MOS, and the polarity of the input voltage determines whether the circuit is a current source or a current sink.

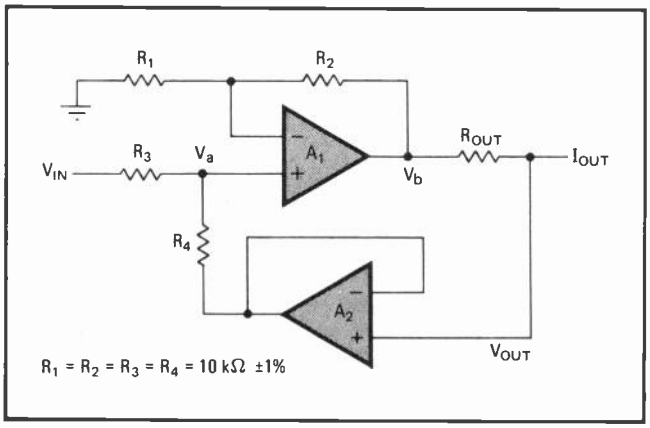
The basic bilateral current source is shown in Fig. 1. Operational amplifier A_2 is a high-input-impedance voltage follower that drives the node where voltages V_{IN} and V_{OUT} are summed. The node voltages are

$$V_a = (V_{OUT}+V_{IN})/2$$
$$V_b = V_a[1 + (R_2/R_1)] = 2\,V_a$$
$$= V_{OUT} + V_{IN}$$

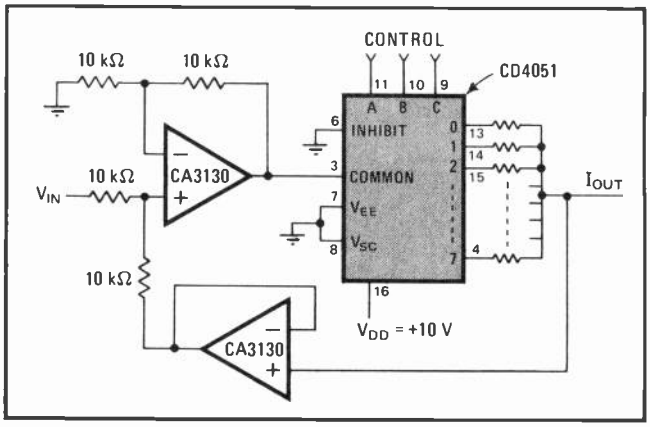
This last equation shows that the voltage across resistor R_{OUT} equals V_{IN}; therefore, because A_2 has a high input impedance,

$$I_{OUT} = V_{IN}/R_{OUT}$$

Maximum output current is limited by the current available from op amp A_1 at its maximum output volt-



1. Current source. Basic circuit provides output current of V_{IN}/R_{OUT}. Direction of current is given by sign of V_{IN}. Resistance R_{OUT} can be made digitally adjustable, as shown in Fig. 2.



2. Programable. C-MOS multiplexer connects various resistors into circuit to serve as R_{OUT}. Thus current is adjusted by digital control.

age. The minimum current is governed by the input current of A_2, which should be less than 1% of the minimum current from the source.

Although the circuit will function well with any general-purpose operational amplifier, the CA3130 C-MOS/bipolar op amp is especially suited for this application because of its field-effect-transistor input, full voltage output swing, and low cost.

Programable current ranges are obtained by inserting one or more CD4051 C-MOS analog multiplexers in series with resistors of selected values, as shown in Fig. 2. The CD4051 multiplexer has internal level-shift circuitry to accommodate different logic families.

For the higher current ranges (R_{OUT} less than 10 kilohms), it may be necessary to take the on resistance of the switches into account by adjusting the combined resistance of the switch and resistor to yield accurate currents. If V_{IN} is less than ±0.5 V, the op-amp input-offset voltages should be nulled. □

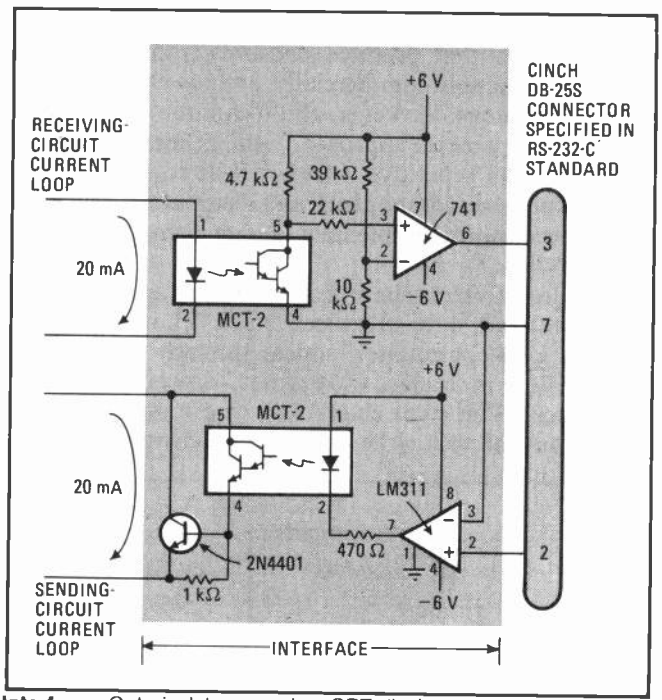
Opto-isolators couple CRT terminals to printer lines

by Andrew Longacre, Jr.
University of New Orleans, New Orleans, La..

When a terminal with a cathode-ray-tube display replaces a teleprinter terminal at the end of a full-duplex 20-milliampere current loop, the new interface is often complicated by the fact that the current loop must not be grounded at the terminal end. The University of New Orleans ran into this problem recently. It wanted to plug new CRT terminals into existing teleprinter hookups in its university-wide time-shared computer network in which the current loops are grounded at the computer. It succeeded with a simple and direct interface—receiving and sending circuits that are built round a pair of opto-isolators and take full advantage of the current driven in the loops.

Each circuit uses the 20-mA loop current to power one side of its opto-isolator. In the receiving circuit, which carries signals going to the screen of the terminal, the loop current directly drives the isolator's light-emitting diode, and the emitted light drives the integral photo-Darlington pair into saturation. ASCII-encoded signals occur as momentary interruptions in the 20-mA current, which in turn cause the photo-Darlington to cut off. The operational amplifier senses this condition and generates positive pulses corresponding to the interruptions.

The sending circuit, which carries signals coming from the keyboard, employs an analog comparator to sense the sign of the terminal's output and drive the opto-isolator LED on for the normally negative output. Once again, the light emitted from the LED saturates the photo-Darlington pair, which in turn drives the 2N4401 npn transistor into saturation so that it easily passes the 20-mA loop current. ASCII-encoded symbols occur here as positive pulses leaving the terminal, causing the LED to be turned off, the transistors to be cut off, and thus the loop current to be interrupted periodically.



Interface. Opto-isolator couples CRT-display terminal to current loops used for electromechanical teleprinters, in arrangement where loops are not grounded at the terminals. Output of the graphic terminal is compatible with RS-232-C standard, which specifies signal levels and connector types for a modem/teleprinter interface.

Two device characteristics primarily determine the maximum speed of the interface. In the receiving circuit, the output slew rate of the 741 proves the limiting factor, and the relatively low ±6-volt supplies were chosen to minimize its effect. In the sending circuit, the slowest part—indeed, the slowest link in the entire interface—is the phototransistor, which, however, would take even longer to turn off completely if it weren't for the 1-kilohm resistor.

In a closed-loop mode over more than 200 feet of cable, these interface circuits have run reliably and without errors at speeds up to 4,800 baud (480 characters per second). □

Digital pulses synthesize audio sine waves

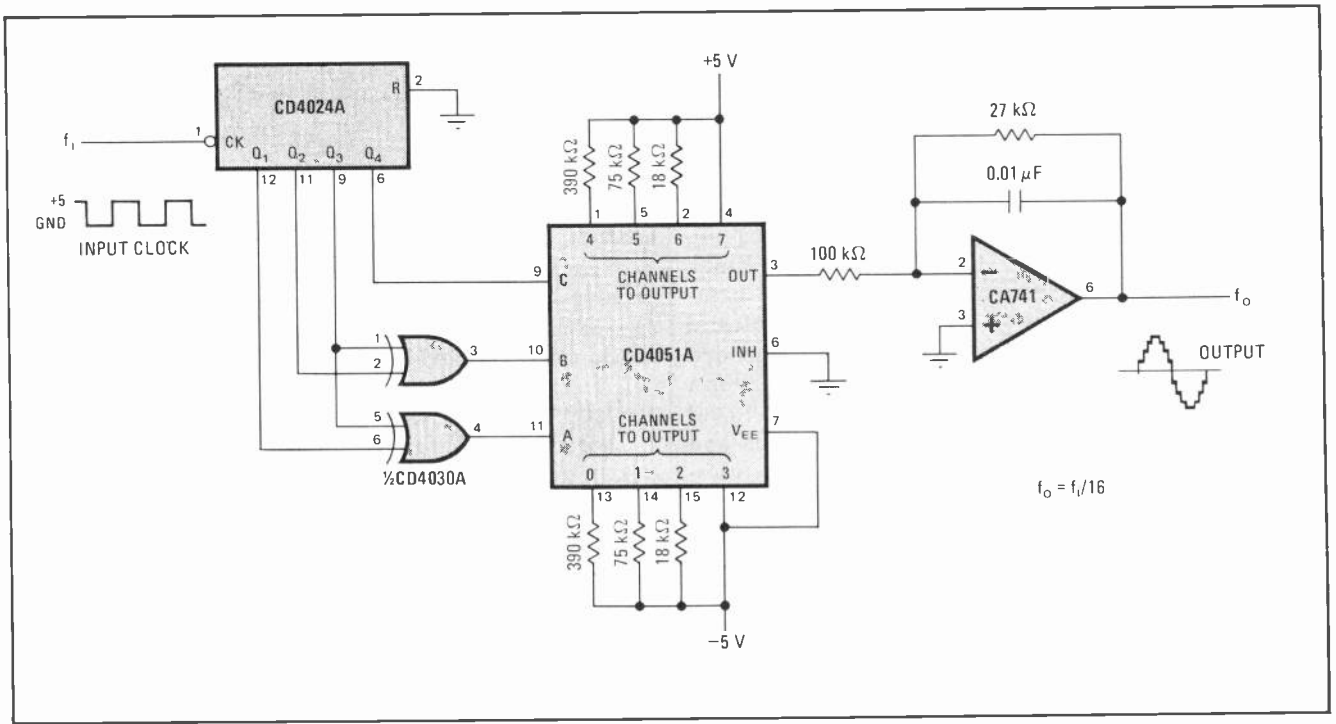
by Patrick L. McGuire
General Dynamics, Pomona, Calif.

Audio tones are often employed for signaling and control in digital systems. To minimize harmonic distortion and channel cross talk, the waveforms of these tones must resemble sine waves as nearly as possible. If the square-wave signal typical of a digital system were used directly, it would have to be thoroughly filtered. Integrated circuits that produce sinusoids from digital inputs, now available commercially, are powerful for their specific functions. However, the technique shown here offers a more general approach to the generation of sine waves or other repetitive waveforms. It requires only a few inexpensive components and dissipates very little power because it is implemented with complementary-MOS circuits.

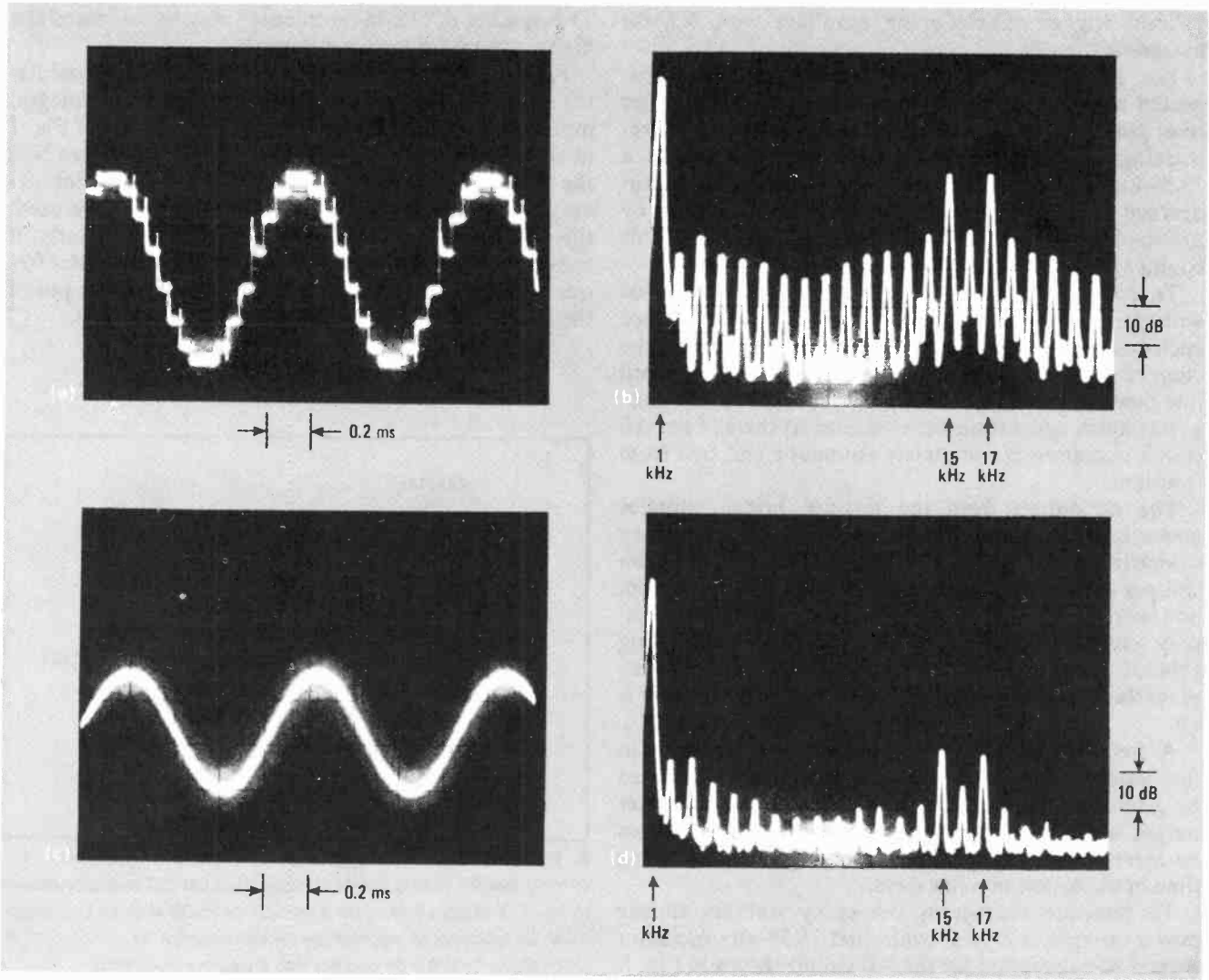
The circuit shown in Fig. 1 generates a 1-kilohertz sine wave from a 16-kHz clock input. The input clock drives a CD4024 counter, which, through some count modification in exclusive-OR gates, drives a CD4051 multiplexer. The eight channels of the multiplexer can deliver any of four different positive currents or four

GENERATING SINE WAVES

Pulse No.	Outputs from CD4024 Q_4	Q_3	Q_2	Q_1	Inputs to CD4051 C	B	A	ON channel of CD4051	Output voltage from 741
14	1	1	1	0	1	0	1	5	−0.77
15	1	1	1	1	1	0	0	4	−0.28
0	0	0	0	0	0	0	0	0	0.28
1	0	0	0	1	0	0	1	1	0.77
2	0	0	1	0	0	1	0	2	1.14
3	0	0	1	1	0	1	1	3	1.35
4	0	1	0	0	0	1	1	3	1.35
5	0	1	0	1	0	1	0	2	1.14
6	0	1	1	0	0	0	1	1	0.77
7	0	1	1	1	0	0	0	0	0.28
8	1	0	0	0	1	0	0	4	−0.28
9	1	0	0	1	1	0	1	5	−0.77
10	1	0	1	0	1	1	0	6	−1.14
11	1	0	1	1	1	1	1	7	−1.35
12	1	1	0	0	1	1	1	7	−1.35
13	1	1	0	1	1	1	0	6	−1.14
14	1	1	1	0	1	0	1	5	−0.77
15	1	1	1	1	1	0	0	4	−0.28
0	0	0	0	0	0	0	0	0	0.28
1	0	0	0	1	0	0	1	1	0.77



1. Sine-wave generator. The 16-kHz input clock drives a counter that, through X-OR gates, drives a multiplexer. The multiplexer simply routes currents in amplitudes proprotional to a sampled sine wave into the summing junction of the op amp. The feedback capacitor rolls off the frequency response of the amplifier at about 600 Hz. This technique of waveform generation can also be used for other repetitive waves.



2. Output. Wave shape and spectral composition of output from circuit in Fig. 1 are shown with and without filter capacitor in feedback circuit of output operational amplifier. Without filtering, waveform (a) clearly shows the discrete steps of synthesis, and spectrum (b) contains harmonics at 15 kHz and 17 kHz that are only 25 dB below the fundamental 1-kHz output. With frequency response rolled off at about 600 Hz by addition of filter capacitor to circuit, waveform (c) is smoothed, and all harmonics in spectrum (d) are down by more than 45 dB.

different negative currents to the summing junction of a 741 operational amplifier. The table indicates how the counter and X-OR gates ensure that these currents are delivered in the proper sequence to produce the output waveform shown in Fig. 2. The wave is smoothed by the feedback capacitor in the op-amp circuit.

The photographs in Fig. 2 demonstrate the step-by-step generation of the sine wave and the smoothing effect of the filter capacitor, as well as the harmonic content of the output. Without the filtering, the 15th and 17th harmonics are only 25 decibels weaker than the fundamental output signal, but the capacitor adds a corner at about 600 Hz so that these harmonics are reduced to 45 dB below the signal. □

Oscillator drives digital clock when ac power fails

by Robert C. Moore
Applied Physics Laboratory, Johns Hopkins University, Silver Spring, Md.

Including an oscillator in the design of a digital clock can keep the clock going during an interruption of the ac power. When ac power is present, the clock is driven by 60-hertz pulses that are generated from the 15.36-kilohertz oscillator and synchronized by the ac line. If the ac power is interrupted, a standby battery keeps the oscillator running to drive the clock. When ac power returns, the circuit automatically resynchronizes to the line frequency, giving excellent long-term stability.

The circuit that drives the clock chip uses two complementary-MOS integrated circuits—a 74C04 hex inverter and a 14520 dual hexadecimal counter (Fig. 1). Two of the inverters from the 74C04 are connected to form a

Schmitt trigger pulse-shaping amplifier with 4.5-volt hysteresis.

The Schmitt trigger drives another inverter, connected as a 40-μs one-shot to generate a 60-Hz master reset pulse that is synchronous with the ac line. The remaining three inverters in the 74C04 are used as a 15.36-kHz oscillator to drive the 14520 dual hexadecimal counter. The 14520 divides the 15.36 kHz by 256 to obtain 60 Hz for driving the 5314 clock chip. This counter should overflow 60 times a second.

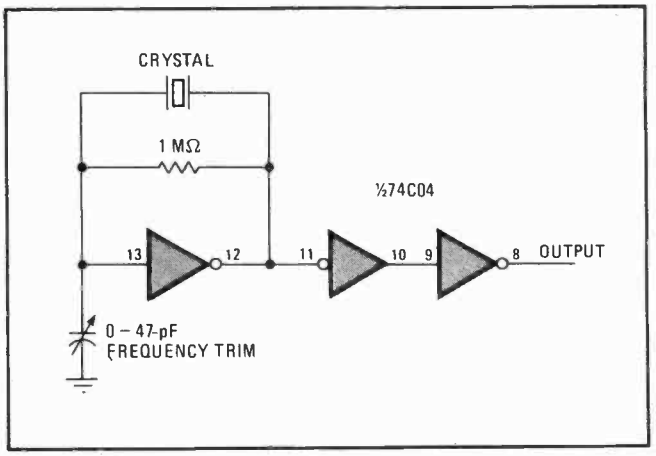
To ensure that the 14520 overflow is synchronous with the 60-Hz line, the counter is reset to zero once each cycle of the line. If ac-line power is interrupted, the counter simply runs free at its rate of nearly 60 Hz until line power is restored. When power is restored, the reset pulses again synchronize the counter to the ac line. All circuit operation is completely automatic and free from transients.

The dc output from the rectifier bridge supplies power to the C-MOS ICs, the clock chip, and the display device (not shown in Fig. 1). The dc current also trickle-charges the standby battery. During an ac interruption, however, the battery does not deliver power to the display circuit. To limit battery drain, the opposing 1N4001 diode prevents current from flowing to the display; therefore the display is dark while the ac power is off.

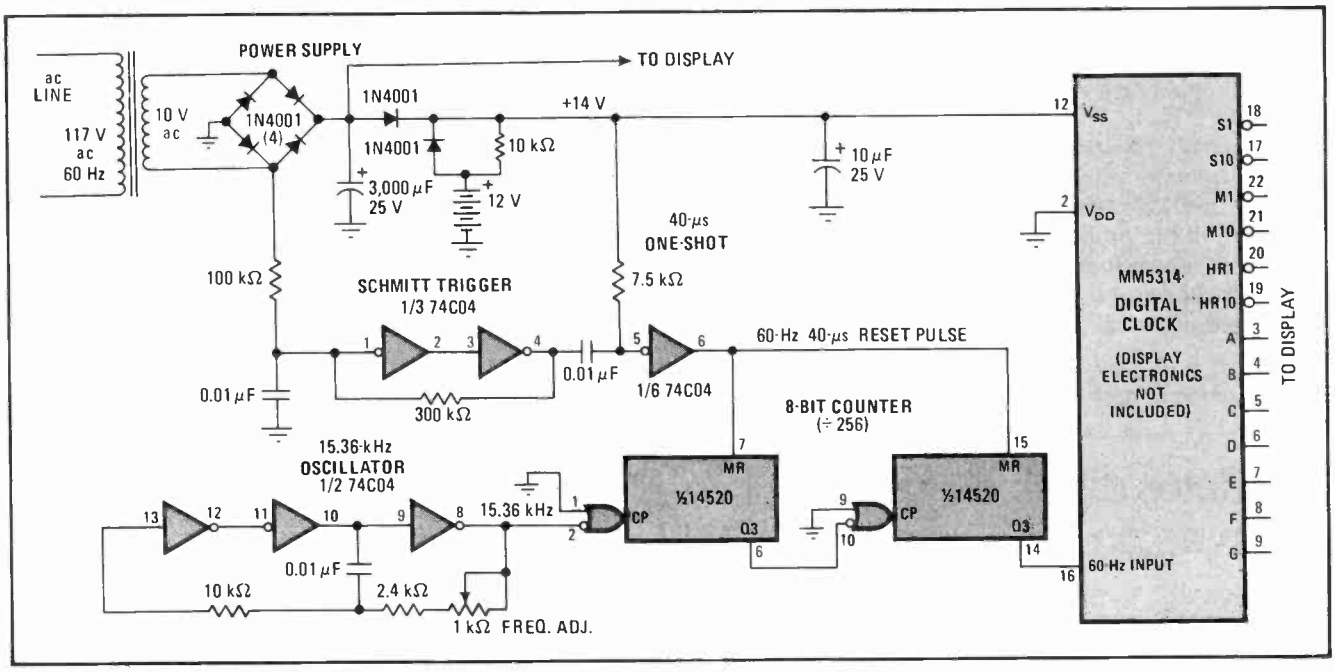
A frequency-trimming potentiometer is included in the oscillator circuit. This 10-turn pot can be adjusted by a screwdriver while the oscillator output or counter output is being checked on a frequency meter, or it can be merely touched up if the clock is gaining or losing time in the course of a few days.

To improve short-term frequency stability during power outages, a crystal-controlled 15.36-kHz oscillator should be substituted for the RC circuit shown in Fig. 1. The number of bits in the counter may be increased if a higher crystal frequency is desirable.

Figure 2 gives details of the crystal-controlled oscillator design. The crystal frequency must be an integral multiple of 15.36 kHz, and the oscillator circuit of Fig. 2 must be followed by a divide-by-N counter, where N is the crystal frequency divided by 15.36 kHz. For example, if a 4017 divide-by-10 counter were to be used, the crystal frequency would be 153.6 kHz. Similarly, if the counter were a 4024 (divide by 128), the crystal frequency would be 1.96608 MHz. The master reset pin of the counter should be connected to the reset pulse. □



2. Better time. Crystal-controlled oscillator provides better frequency stability during power outages than the RC oscillator shown in Fig. 1. Frequency must be a multiple of 15.36 kHz, and oscillator must be followed by appropriate divider/counter to provide 15.36 kHz into the 14520 8-bit counter that drives the clock chip.



1. Good time in blackout. Two C-MOS circuits enable digital clock to continue accurate time-keeping during interruptions of ac power. In normal operation, 60-Hz output of divide-by-256 counter is phase-locked to ac line. Counter output runs free at its rate of nearly 60 Hz during power interruption, drawing power from rechargeable standby battery. Display is not powered during battery operation.

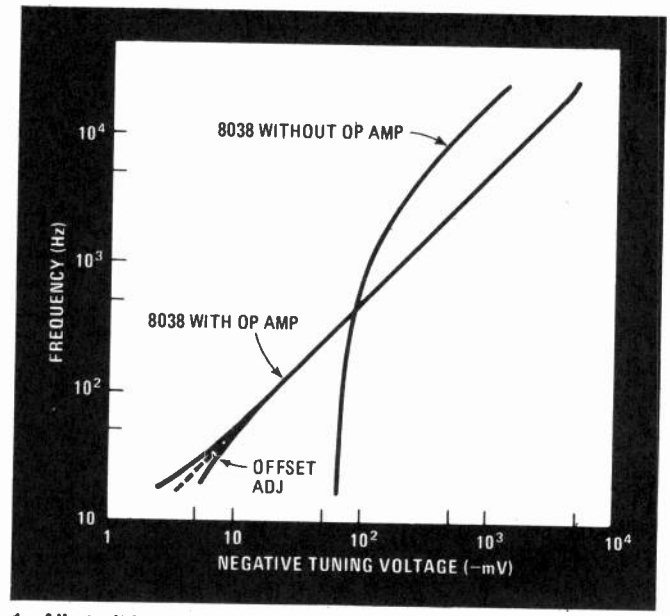
Modified function generator yields linear VCO

by Antonio Tagliavini
Bologna, Italy

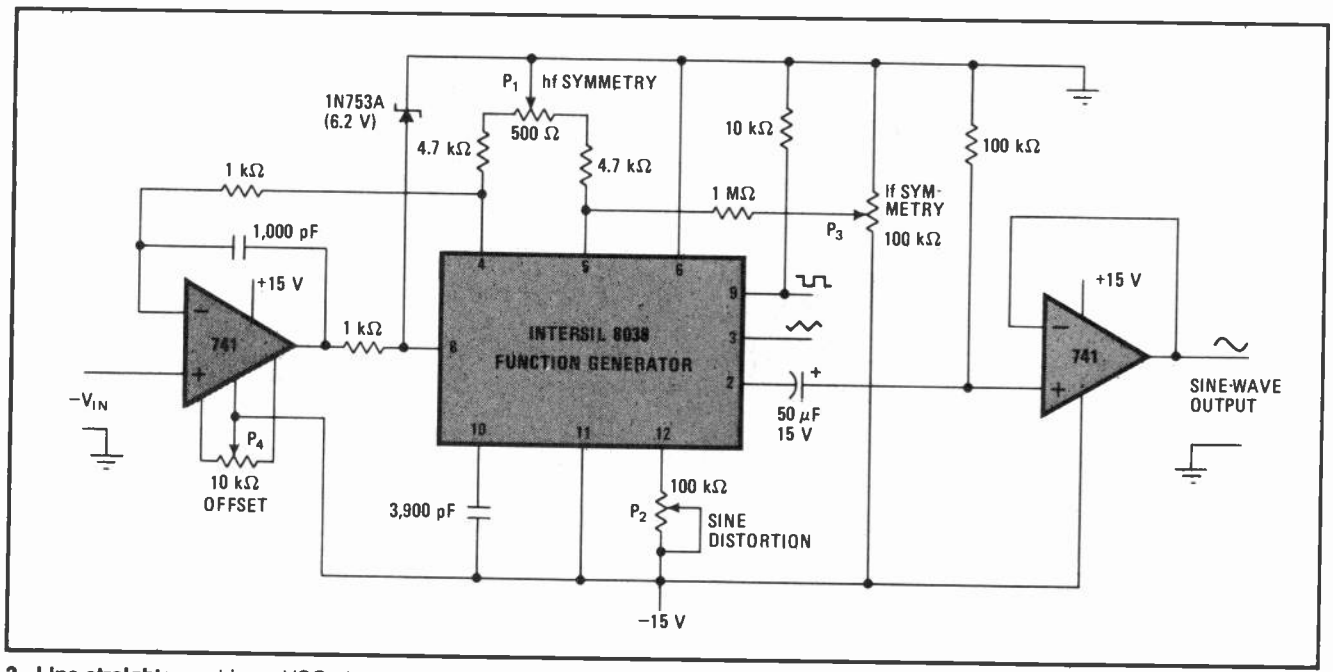
Because of its wide sweep capability, the Intersil 8038 integrated function generator is useful for realizing a voltage-controlled oscillator with a sine-wave output. But because of the limitations of the 8038's integrated current sources, its frequency-versus-voltage characteristic is nonlinear over a good part of its sweep range. As Fig. 1 shows, however, the tuning can be made linear over the entire audio range if an external operational amplifier is added before the function generator's control input.

The 8038 contains two current sources. One is always operating, supplying an external integrating capacitor with a constant current I. The other is switched on and off by a level comparator, supplying the capacitor with a current -2I when on. Therefore the capacitor is charged by I and discharged by -I, producing a symmetrical triangular wave (which is then converted into a sine wave) with a frequency that is proportional to current I. This current does not vary linearly with the input voltage, and therefore the relationship between input voltage and frequency is not linear.

To linearize the relationship, the timing voltage is applied to the control input terminal of the 8038 (pin 8) through an operational amplifier, as shown in Fig. 2. The op amp drives the integrated non-switched current source, and because the voltage fed back to the inverting input terminal of the op amp must equal V_{in}, the



1. All straightened out. Voltage/frequency characteristic of the Intersil 8038 voltage-controlled audio-frequency oscillator is not linear. But if the input voltage is applied to the 8038 through an operational amplifier, with feedback through one of the integrated current sources on the IC chip, the tuning curve becomes a straight line.



2. Line straightener. Linear VCO circuit uses 741 op-amp input to linearize one of the two current sources in the 8038 function generator. Because the two sources are inherently matched, the second source tracks the first and also gives linear current-to-voltage response. Output op-amp buffer provides low output impedance. Pots shape sinusoidal output wave form and maintain linearity at low frequencies.

current supplied by this source varies directly with V_{in}. The two integrated current generators in the 8038 are inherently matched, so the switched source tracks the non-switched one and therefore is also linearized. The switched source drives a current inverter/doubler that provides the current -2I.

The 1N753A zener diode protects the control input of the function generator IC against voltages more positive than +0.6 volt and more negative than -6.2 v. The output operational amplifier is merely a buffer, and may be omitted if low output impedance is not required.

Three potentiometers permit shaping of the output waveform. First, at a high frequency, P_1 is adjusted to obtain a symmetrical wave shape (square wave from pin 9). Then P_2 is set for best sinusoidal output. Finally P_3 is trimmed for good symmetry at the low-frequency end of the tuning curve. The offset adjustment, P_4, is then adjusted to provide tuning linearity.

With component values shown, the VCO covers the entire audio range (20 to 20,000 hertz). □

Converter lets processor drive teletypewriter

by Richard C. Pasco
Stanford University, Stanford, Calif.

An inexpensive circuit can replace a lengthy software routine at the interface between a teletypewriter and almost any microprocessor [*Electronics*, July 25, 1974, p. 96]. But only six integrated circuits are needed in an improved version that employs the standard 8-bit ASCII code, and only five ICs in the modification that processes the Baudot code.

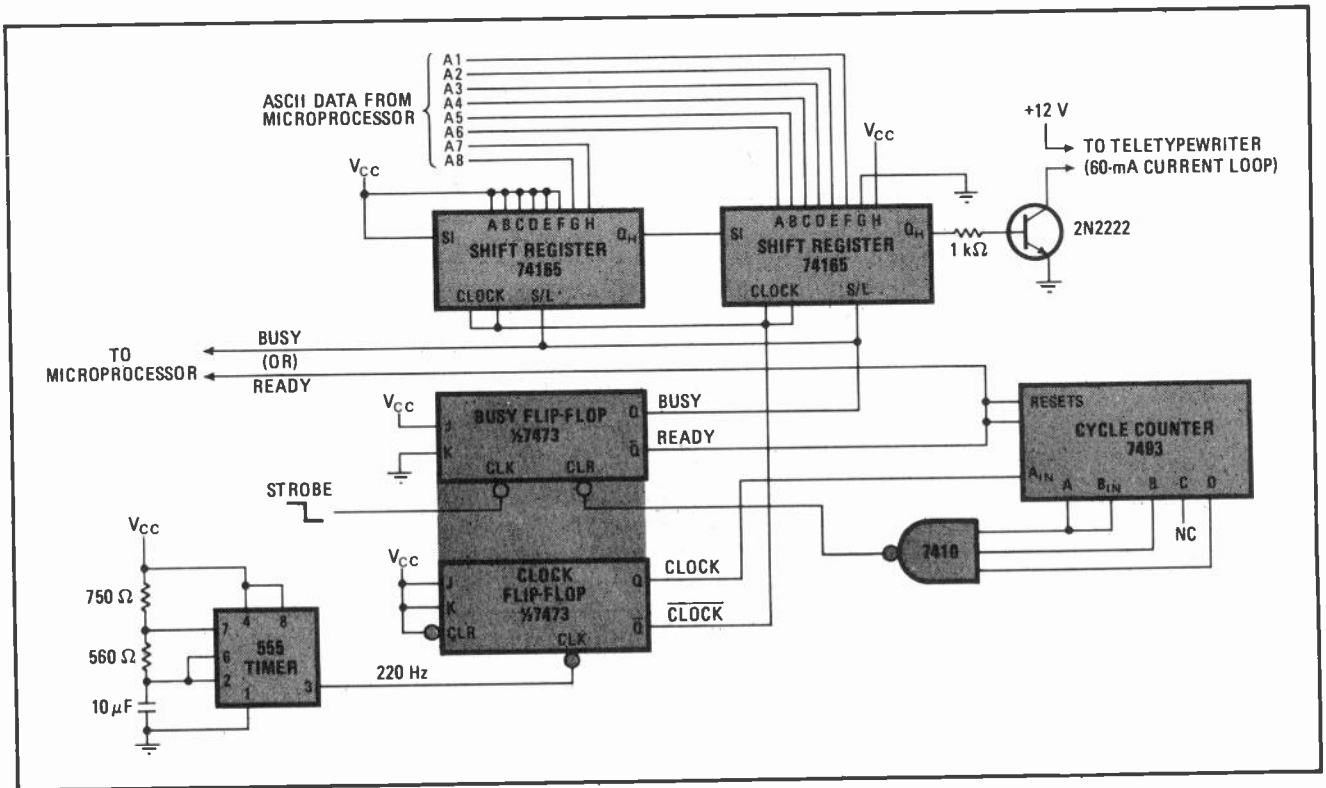
This parallel-to-serial converter has many applications. It will change the parallel output of a keyboard into a serial format for transmission by telephone via a modem, and it will interface the output of any parallel-output device with a teletypewriter for printing.

The converter's operation is easily followed with the aid of the accompanying circuit diagram. Initially the converter is in the READY mode—that is, the BUSY flip-flop is cleared. This keeps the 16-bit shift register in the LOAD mode and the cycle counter reset. The output of the shift register is held high because the parallel load input of its last stage is connected to V_{CC}.

Upon a negative-going transmission of the STROBE line, the BUSY flip-flop is set. This puts the shift register into the SHIFT mode, locking-in the data present at its inputs, and removes the reset from the cycle counter.

On the first negative-going transition of the clock after this strobe, the cycle counter enters state 1, and simultaneously the shift register shifts a logic zero to its output. This logic zero is the START signal.

On the next nine clocks, the shift register's output consists of 8 data bits and a high corresponding to the



Serial feed. Data from microprocessor, parallel-fed into shift register, is fed out serially to teletypewriter for printout. The STROBE and BUSY signals synchronize the circuit with the processor. Ten characters per second are transmitted in standard 8-bit ASCII code, but circuit is easily modified for Baudot code. This hardware eliminates a software routine for interfacing device to teletypewriter; parts cost less than $5.

STOP pulse. Meanwhile the cycle counter passes to states 2 through 10.

The next clock puts the cycle counter into state 11, but the gate detects this and clears the BUSY flip-flop. This in turn raises the READY line, resets the cycle counter, and puts the shift register back into the LOAD mode. Thus, the transition from state 10 to the READY mode proceeds asynchronously within a few nanoseconds. During this transition the shift-register output remains high because a logic 1 is loaded from the V_{CC} line.

Transmission at 10 characters per second results if a new character is provided within one clock period (9.09 ms) of this READY indication. Even if a new character is received immediately, however, the output will remain at 1 and transmission will not begin until the next clock. This insures a minimum stop pulse duration of two clock periods. If no character is received, the converter will wait in the READY mode indefinitely.

The following modifications adapt the circuit to the Baudot code. Delete the left-hand 74165, and connect the SI and A inputs of the right-hand 74165 to V_{CC}. Then replace the 7410 gate with a 7404 inverter driven off the 7493's D output (the A output now connects only to B_{in}; B and C outputs are left with no connection). □

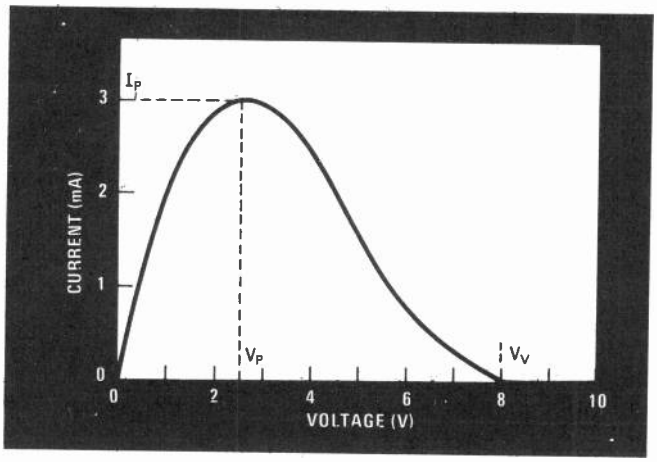
Complementary JFETS form bimode oscillator

by Gregory Hodowanec
Newark, N.J.

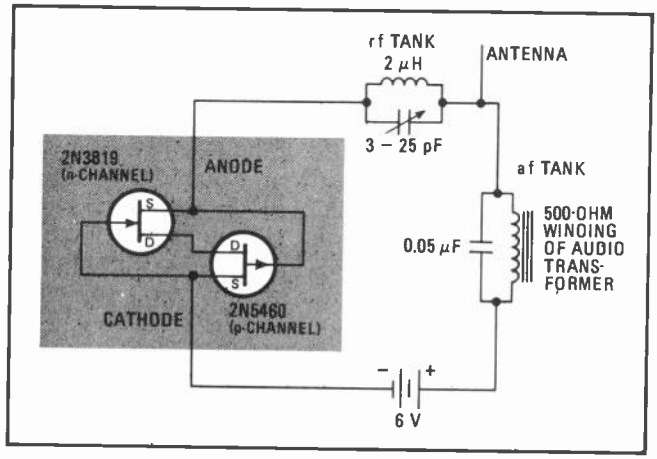
A complementary pair of junction field-effect transistors can be interconnected to form a negative-resistance two-terminal device, which makes a simple oscillator. In monolithic form this configuration is called a lambda diode [*Electronics*, June 26, p. 105] and is available with a wide range of characteristics. If two discrete JFETs are connected to make the diode, they do not have to be matched, but can be chosen to provide various values of peak current and negative-resistance-voltage range. Figure 1 shows current as a function of voltage for a combination consisting of an n-channel 2N3819 and a p-channel 2N5460.

The JFET "diode" can be made to oscillate at frequencies ranging from audio to vhf. All that is required is to connect the diode in series with an inductance-capacitance tank circuit and supply a bias voltage in the negative-resistance region. Figure 2 shows a simple bimode oscillator circuit capable of oscillating at both audio and radio frequencies simultaneously. Oscillation is at approximately the natural resonances of each tank circuit. The radio-frequency tank, consisting of a 2-microhenry choke shunted by a trimmer capacitor, can be tuned over a wide range centered near 20 megahertz. The audio section uses the 500-ohm winding of a miniature audio output transformer and a 0.05-microfarad ceramic capacitor for oscillation at approximately 440 hertz. The audio section cleanly amplitude-modulates the rf section, as demonstrated by reception of the radiated signal on a communications receiver. Power output is in the order of 25 milliwatts and the signal has a range of several hundred feet with no antenna on the oscillator. The range can be extended to several thousand feet with a short length of antenna, so a form of this oscillator can be adapted to radio-control appplications.

This circuit can be used as a simple signal source for many experimental purposes. The audio section can be eliminated or shorted out if an unmodulated signal is desired. The circuit can also be adapted to any design requiring a low-level signal source. Variable frequency control can be incorporated at either or both frequency levels. □



1. Negative resistance. Current-voltage characteristics are shown for a "diode" consisting of the arrangement of the two complementary JFETS shown in Fig. 2. For any terminal voltage between 2.5 V and 8 V, the combination has a negative resistance.



2. Bimode oscillator. JFET-combination "diode" and two tank circuits can oscillate at audio frequency and radio frequency simultaneously. Resultant signal is rf modulated by af; either component can be varied for communications or control applications.

IC timers control dc-dc converters

by P. R. K. Chetty
Indian Scientific Satellite Project, Bangalore, India

An integrated-circuit timer such as the MC1455 can be used as the control element in a simple dc-to-dc converter regulator. Shown below are a current step-up converter regulator and a polarity-reversing voltage step-up converter regulator. Both are regulated to within 0.5% for load currents of 300 milliamperes, and have a ripple of less than 5 mA.

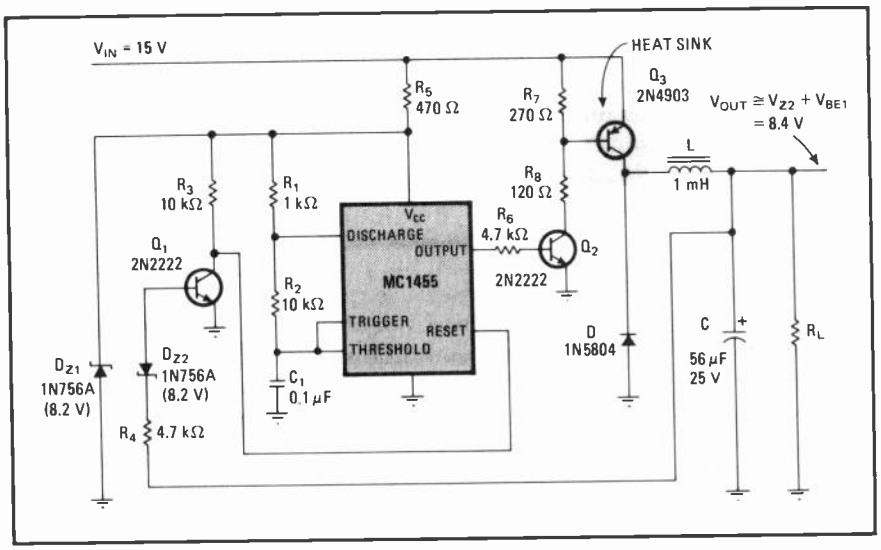
In these circuits the MC1455 operates as an astable multivibrator, turning the pass transistor on and off to keep the output-filter capacitor charged to the desired output voltage. Overvoltage is prevented by a feedback arrangement that turns off the multivibrator when the capacitor voltage reaches a predetermined level.

The astable-mode connection of the timer causes the voltage across capacitor C_1 to oscillate between $V_{CC}/3$ and $2\ V_{CC}/3$ at a frequency of approximately $1.44/(R_1+R_2)C_1$—about 1.3 kilohertz. The maximum operating voltage of the timer is 16 volts, but here its V_{CC} is clamped at 8.2 v by zener diode D_{Z1}. The input voltage therefore can have any value within the ratings of the pass transistor and the filter capacitor.

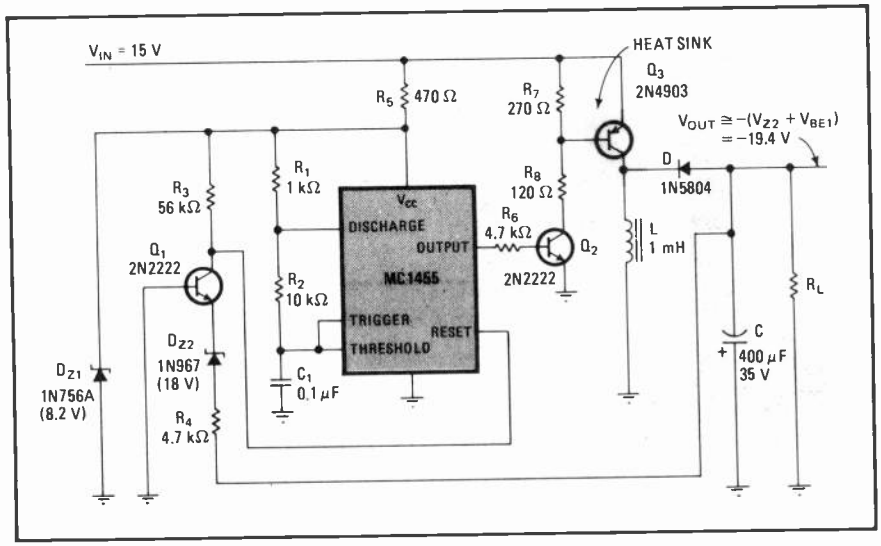
Figure 1 shows the current step-up converter regulator. When the output of the control timer is high, transistor Q_2 is turned on and therefore pass transistor Q_3 is turned on. Collector current from Q_3 flows through inductor L into the load and the filter capacitor. When the output of the timer goes low, the transistors turn off. Diode D commutates the current flow flowing through the inductor when Q_3 switches off. If there were no feedback circuit, the output voltage would depend upon the input voltage and the duty cycle.

The feedback circuit consists of R_4, zener diode D_{Z2}, transistor Q_1, and R_3, Whenever the output voltage exceeds $(V_{Z2}+V_{BE1})$, Q_1 turns on and drives the reset terminal of the 1455 low. The transistors Q_2 and Q_3 therefore stay off, allowing the output voltage to decrease. Thus the output voltage V_{out} is maintained approximately equal to $(V_{Z1}+V_{BE1})$.

The performance of the circuit in Fig. 1 is as follows:



1. Converted and regulated. Dc-to-dc converter includes IC timer for regulation. The MC1455, connected as free-running multivibrator, switches Q_3 on and off. If output gets too high, feedback circuit drives timer reset low to hold switch off. Regulation is less than 0.5% at 300 mA, and ripple is less than 5 mA. Output voltage is lower than input voltage, so current can be stepped up.



2. Polarity reversed. Positions of inductor, commutating diode, and feedback elements are changed here for negative output voltage. This circuit arrangement can step up magnitude of either voltage or current; components chosen here provide voltage step-up. Regulation is same as before.

Input voltage, V_{in} = 15 V
Output voltage, V_{out} = 8.4 V
Load current, I_{out} = 300 mA
Ripple, I_r (for I_{out} = 300 mA) = 5 mA
Load regulation (for V_{in} = 15 V and I_{out} = 0–300 mA) equals or is less than 0.5%
Line regulation (for V_{in} = 15–25 V and I_{out} = 300 mA) equals or is less than 2.5%

The polarity-reversing circuit of Fig. 2 differs from Fig. 1 in the arrangement of L, C, D, and the feedback elements. When Q_3 switches off, the commutating current in L charges C to produce an output voltage that is negative with respect to ground. This voltage is applied to the anode of D_{Z2} through limiting resistor R_4. Whenever the output is more negative than $-(V_{Z2} + V_{BE1})$, the timer reset goes low, allowing the voltage across the capacitor to become less negative. The output voltage of this circuit is therefore maintained at approximately $-(V_{Z2} + V_{BE1})$. This circuit can provide an output voltage equal to, less than, or greater than the input voltage.

The performance of the circuit in Fig. 2 is as follows:

Input voltage, V_{in} = +15 V
Output voltage, V_{out} = -19.4 V
Load current, I_{out} = 300 mA

Ripple and regulation are the same as in the earlier example. □

Discriminator displays first of four responses

by John S. French
Western Electric Co., Inc., Sunnyvale, Calif.

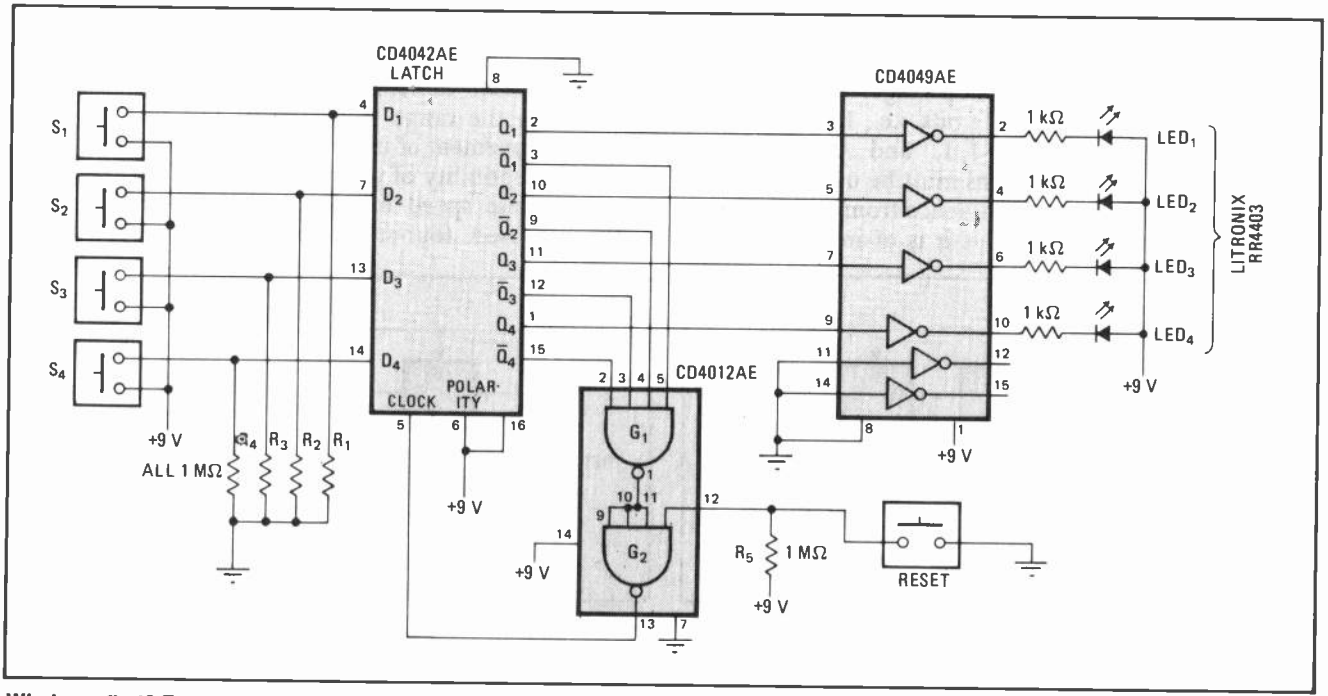
A first-response discriminator, which turns on a light indicating the first switch to close and simultaneously locks out the other switches, can be useful in sports, games, behaviorial learning studies, and experiments in physical science. The circuit shown here indicates which of four switches closes first. It uses three low-drain C-MOS integrated circuits and a 9-volt radio battery.

When the push-to-close switches S_1 through S_4 are open, inputs D_1 through D_4 to the 4042 quad latch are low. Therefore outputs Q_1 through Q_4 are low, and $\bar{Q}_1$ through $\bar{Q}_4$ are high. These four high inputs to NAND gate G_1 make G_1 low and G_2 high. The high output from G_2 is applied to the clock input of the latch; with the clock thus enabled, the outputs of the latch can follow the inputs.

If switch S_1 is closed, D_1 goes high and therefore Q_1 goes high, allowing light-emitting diode LED_1 to light. Simultaneously, $\bar{Q}_1$ goes low, sending G_1 high but G_2 and the clock input of the latch low. The clock low locks the latch so that D_2, D_3, and D_4 no longer control Q_2, Q_3, and Q_4. As a result, even if S_2, S_3, or S_4 is closed, the corresponding LED does not light.

The circuit is reset by momentary closing of the reset switch to set G_2 and clock high. If S_1 through S_4 are open, Q_1 through Q_4 go low for the next trial.

Expansion of this circuit to handle N inputs is straightforward. Only two NAND gates are required, but one of them must have N inputs. □



Who's on first? The first switch to close lights up its associated LED, and blocks all other LEDs from lighting if their switches are closed. Circuit can distinguish first-closed switch for time differences as small as 0.05 microsecond. Cost of parts for entire circuit is under $10.

Delay line in shift register speeds m-sequence generation

by J.T. Harvey
Amalgamated Wireless (Australasia) Ltd., North Ryde, Australia

The clock rate of a shift-register generator of maximal-length pulse sequences is significantly increased when a delay line replaces one or more of the register's stages. High-speed m-sequences, as maximal-length pulse sequences are called, are needed for testing data links, for generating repeatable pseudo-noise, and in spread-spectrum techniques [*Electronics*, May 29, p. 127].

Repetitive sequences of pulses can be generated by connecting the output of a shift register back to the input in some way, setting in some initial condition that is not all zeroes, and turning on the clock. In this situation, the length of the repeating pulse sequence that emerges from the register depends upon the feedback arrangement and perhaps upon the initial condition—if the register has N stages, the sequence may repeat after only two, N, or some other number of pulses.

However, the m-sequence is independent of the starting condition. This follows from two facts. First, its length is $2^N - 1$ pulses (the all-zero condition never appears in the register). Second, its generation involves every possible combination of 1s and 0s in the shift register except for the all-zero combination.

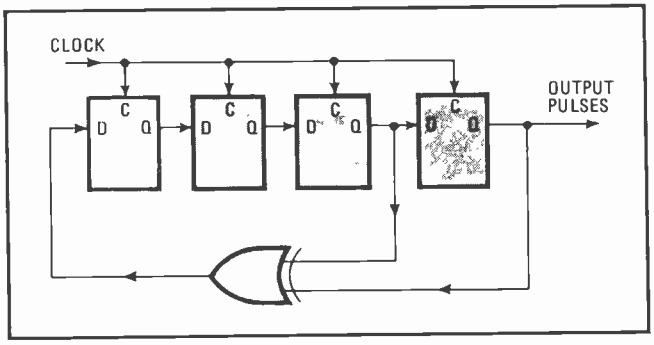
A typical m-sequence generator is shown in Fig. 1. The feedback signal in the four-stage device is obtained by taking the exclusive-OR (XOR) of the outputs from the last and next-to-last flip-flop stages. The resulting sequence repeats after $(2^4 - 1)$ bits, i.e., 15 bits. It goes 1, 1, 0, 0, 0, 1, 0, 0, 1, 1, 0, 1, 0, 1, 1, and then repeats. Various feedback combinations must be used to achieve the maximum-length pulse sequence from registers with various numbers of stages, but it is of interest to note that generators having 2, 3, 4, 6, 7, or 15 stages can operate by feeding back the XOR of the outputs from the last and next-to-last stages.

The limit to high-speed operation of this device occurs when the interval between clock pulses is less than the combined effective propagation delay in a shift-register stage and the XOR gate. For a given family of logic, the propagation time of the XOR is typically slightly less than that of a shift-register stage. Thus, the clock rate at which an m-sequence generator can operate is typically 0.5 to 0.7 of the rate at which the shift register can operate alone.

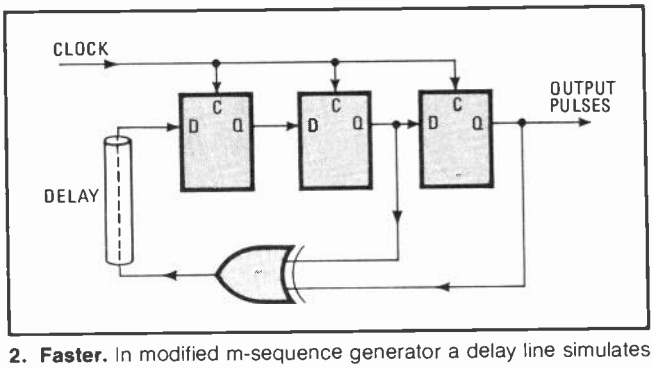
Provided that operation is required over a limited range of clock frequency (most are operated at a fixed clock rate), then the first stage of the shift register can be removed and a delay line substituted. This arrangement is shown in Fig. 2. The optimum delay is the interval between clock pulses less the exclusive-OR-gate propagation delay. The gate and delay line thus simulate a delay-free gate and one shift-register-stage delay. The maximum frequency of operation is then the maximum shifting rate of the flip-flops.

To demonstrate this idea, some experiments were conducted with MECL III logic, for which 270-megahertz flip-flop clock rate and 2.7-nanosecond gate propagation time worst-case figures are claimed. A pair of MC1670L D-type flip-flops were connected in a ring counter, which was observed to operate to 310 MHz. The same shift-register was used in a two-stage m-sequence generator with the addition of an MC1672L XOR gate, one section of which was used as an output buffer. At this point, the maximum clock rate was found to be only 215 MHz. Then this generator was converted to a three-stage device by the addition of a 20-cm length of 50-ohm coaxial cable, and satisfactory operation was observed in the range from 220 to 310 MHz, giving a speed improvement of up to 44%.

The susceptibility of the circuit to noise will be greatest near these speed limits. When a 90-cm length of cable was used, four-stage operation was observed in



1. Maximizes. Four-stage shift register with feedback arrangement cycles through all possible states except the all-zero condition, producing an output sequence of $2^4 - 1$ pulses. This is the maximum-length sequence (m-sequence) from a four-stage register. Speed of the m-sequence is limited by the propagation delay in the XOR gate.



2. Faster. In modified m-sequence generator a delay line simulates one stage of the shift register, so the output pulse sequence is the same as for the circuit of Fig. 1. The delay line is designed so it, plus the XOR gate, offers the same propagation delay as one register stage, permitting a 44% increase in clock rate for the m-sequence.

the range from 245 to 310 MHz, and a 220-cm length gave six-stage operation (63-bit sequence) at frequencies from 265 to 310 MHz. Similarly, 260 cm of coaxial cable yielded a seven-stage 127-bit sequence for clocks from 275 to 310 MHz.

For a given number of stages, an increase in the external delay decreases the upper and lower clocks in roughly the same ratio, while an increase in the number of simulated stages decreases the range in the clock rate. At least one shift-register stage must be used in front of the first feedback tap to eliminate the possibility of spurious oscillation. □

Memory, peripherals share microprocessor address range

by James A. Kuzdrall
Candia, N.H.

Designers find that the direct addressing mode of the M6800 microprocessor and similar devices cannot be beaten for convenience and efficiency. This mode allows the user to directly address the lowest 256 bytes in the machine—the bytes in locations 0 through 255.

Instructions that use the mode consist of one byte to designate the operation to be performed, plus a second byte to designate the address of the operand. By contrast, other addressing modes have to supply one bit for each of the 16 lines of the memory bus and therefore require a two-byte address for the operand. Thus the direct-addressing mode saves one byte, or 33% of program memory space, in each instruction.

Usually the designer sets aside a portion of the RAM for the easily accessed locations 0–255. However, it is also convenient to assign some of these locations to the peripheral-interface adapter chips that interface the microprocessor to peripheral equipment. The reason is that, in applications requiring a large amount of data input and output, the addresses of the PIA chips may be as active as the RAM addresses.

The circuit arrangement shown in the accompanying diagram allows the direct addressing range of memory locations to be used for both random-access memory and peripheral interface adaptors with a minimum of hardware. It provides control for RAM in locations 0–239, PIAs in locations 240–255, and ROM in locations 1,024–4,095. Although the decoding is not complete because address lines A_8, A_9, A_{12}–A_{15} are not fully decoded, the decoding does prevent two devices from being active on the data bus simultaneously.

In the circuit, decoding an address to reach RAM or a PIA requires only two integrated circuits—a 74LS10 triple NAND gate and a 74LS139 dual decoder.

Gate U_{1B} enables the decoder when valid memory-address data is present and the data is stable (ϕ_2 from clock U_{10} is high). Then address lines A_{10} and A_{11} of the central processing unit are decoded to make one of the 2Y outputs low. Decoder outputs 2Y1, 2Y2, and 2Y3 each select a 1-kilobyte section of ROM, i.e. ROM-1, ROM-2, or ROM-3. If both A_{10} and A_{11} are low, however, so that 2Y0 is low, the RAM and interface adapters are enabled. RAM-1, U_4, is selected if the address is below 128 (A_7 low). U_5 is enabled for addresses between 128 and 255 (A_7 high), but inhibited by gate U_{1A} for addresses 240–255.

To activate the interface adapters (U_6–U_9) for these unused addresses, the inhibit signal is inverted by U_{1C}. The decoder outputs 1Y0-1Y3 of U_2 provide the final selection among the interface adapters. The decoding meets all worst-case timing and loading requirements.

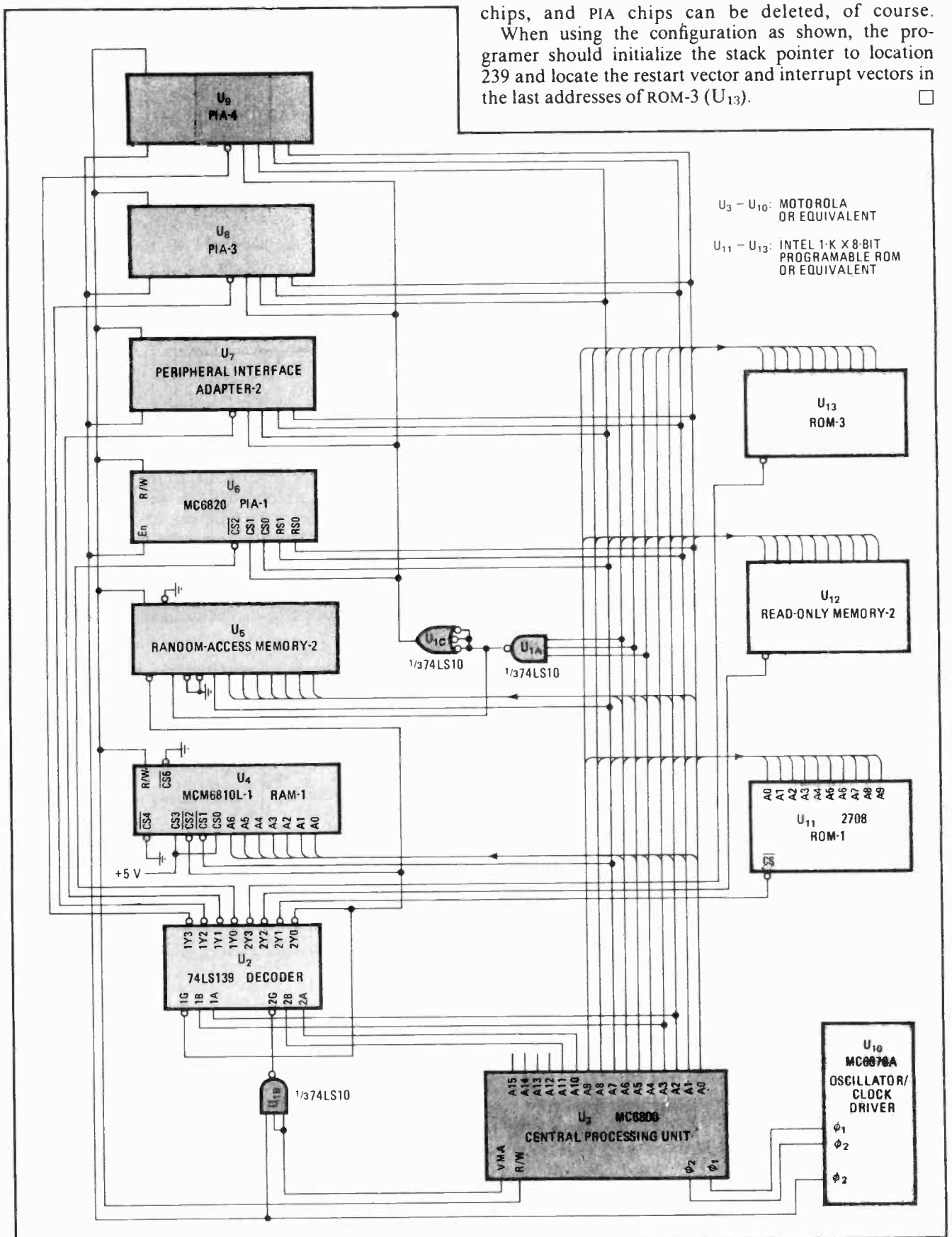
The table shows the contents of the microprocessor address locations for this circuit arrangement. The selection of devices addressed is shown only as an example. For instance, more RAM can easily be added in memory locations 256–511 using the enable inputs of the MCM6810L-1 devices. Unneeded ROM chips, RAM

CONTENTS OF MICROPROCESSOR ADDRESS LOCATIONS

Starting address	Finishing address	Chip	Contents
0	127	U_4	RAM-1 Random-access memory
128	239	U_5	RAM-2 Random-access memory
240	–	U_6	PIA-1 Data register A
241	–	U_6	PIA-1 Data register B
242	–	U_6	PIA-1 Control register A
243	–	U_6	PIA-1 Control register B
244	–	U_7	PIA-2 Data register A
245	–	U_7	PIA-2 Data register B
246	–	U_7	PIA-2 Control register A
247	–	U_7	PIA-2 Control register B
248	–	U_8	PIA-3 Data register A
249	–	U_8	PIA-3 Data register B
250	–	U_8	PIA-3 Control register A
251	–	U_8	PIA-3 Control register B
252	–	U_9	PIA-4 Data register A
253	–	U_9	PIA-4 Data register B
254	–	U_9	PIA-4 Control register A
255	–	U_9	PIA-4 Control register B
1024	2047	U_{11}	ROM-1 Read-only memory, program
2048	3071	U_{12}	ROM-2 Read-only memory, program
3072	4087	U_{13}	ROM-3 Read-only memory, program
4088	4095	U_{13}	ROM-3 Restart and interrupt vectors

chips, and PIA chips can be deleted, of course.

When using the configuration as shown, the programer should initialize the stack pointer to location 239 and locate the restart vector and interrupt vectors in the last addresses of ROM-3 (U_{13}). □



Versatile. This circuit arrangement allows both random-access memory and peripheral interface adapters to be addressed in direct-addressing-mode locations of M6800 microprocessor. This is convenient in operations with lots of data input and output. Logic gates enable the decoder for valid stable addresses and enable or disable the RAM and PIA sections. Lines A_2 and A_3 are decoded for final selection of PIA.

Optical isolator circuit shows phone-line status

by Matthew L. Fichtenbaum
General Radio Co., Concord, Mass.

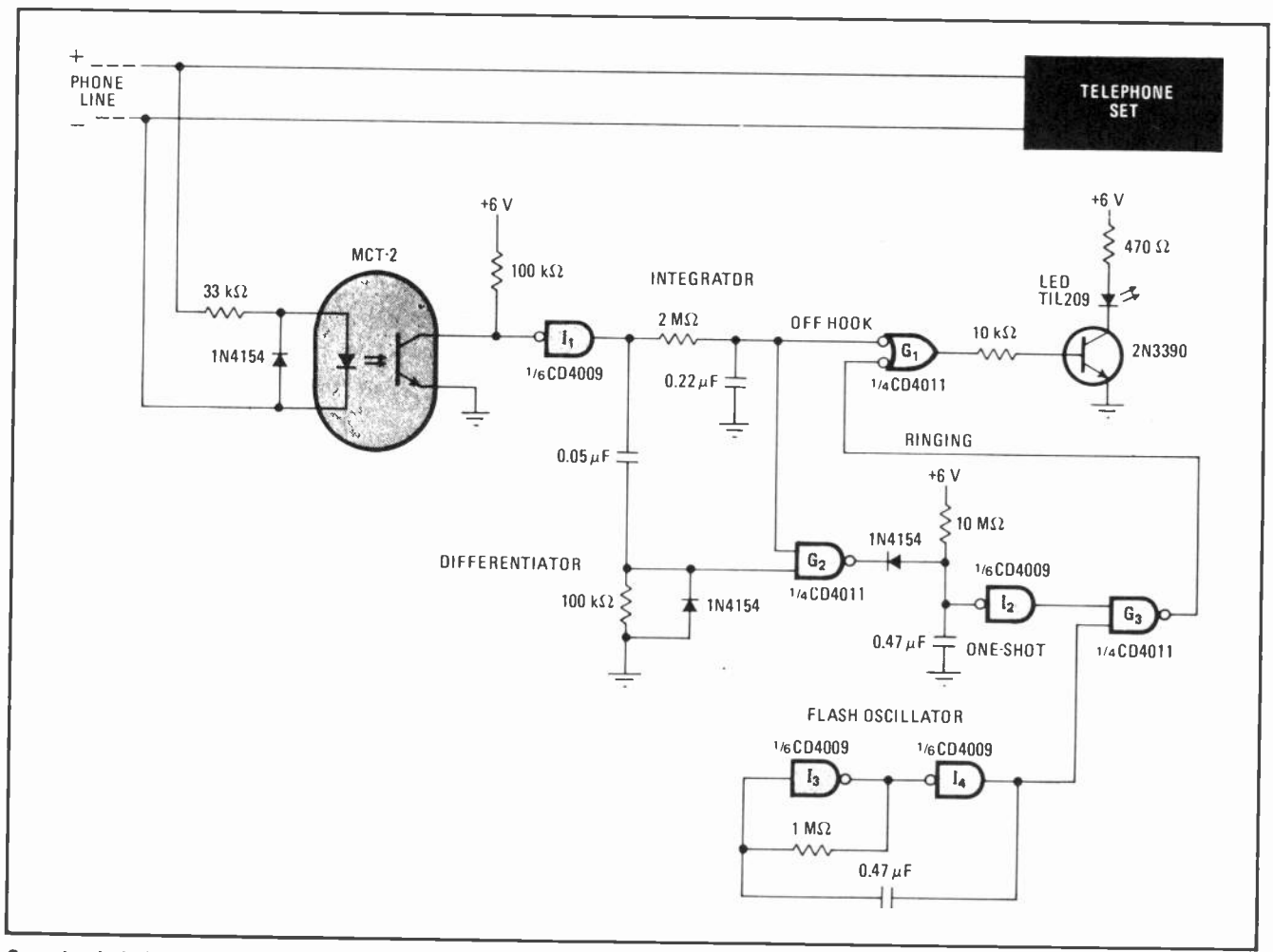
The status of a telephone line can be indicated at a remote location, such as the key unit on a secretary's desk, by a light-emitting diode connected in the circuit shown here. The LED is dark if the phone line is not in use, flashes on and off once every second if the phone is ringing, and stays on if the phone is off the hook.

The circuit includes an oscillator that operates continuously, some logic elements, and an optical coupler that senses the voltage on the phone line. If this voltage is ac, the logic circuit connects the oscillator to the LED, producing the flashing light. Low dc voltages, either steady or pulsed, hold the LED on, and high dc voltages leave it off. The table summarizes circuit performance.

OPERATION OF PHONE-STATUS-DISPLAY CIRCUIT

Phone condition	Line voltage (V)	Isolator output level	LED condition
On hook	50 dc	Low	Off
Ringing	100 ac	Pulses	Flashing
Off hook	6 – 8 dc	High	On
Dialing	6 – 50 dc	Pulses	On

As can be seen from the schematic diagram, the isolator output signal is applied to two RC networks—an integrator and a differentiator. The integrator filters out the ring and dial pulses, giving an output dependent on the steady state of the phone line. The differentiator extracts the pulses.



Secretary's helper. LED indicates status of a remote telephone. Light is off if phone is hung up, shines steadily if phone is off hook, and flashes on and off while phone rings and for 5 seconds after ringing stops. The flashing oscillator operates continuously, but can drive LED only when a ringing signal discharges the one-shot capacitor to enable NAND gate G_3. Thus, one oscillator handles several phone lines.

When the phone is on the hook, so that inverter I_1 has low input and high output, G_1 is deactivated and cannot turn the transistor or LED on.

When the phone rings, the high dc from I_1 and the high output from the differentiator combine to activate G_2, allowing the one-shot capacitor to discharge and enable G_3. Thus the output from the flash oscillator is applied to G_1, flashing the LED. Flashing continues during the slow charge-up of the 0.47-microfarad one-shot capacitor between rings and after ringing stops.

When the phone is off the hook, I_1 has high input and low output, so G_1 is able to turn on the transistor and let the LED light. The momentary high-voltage pulses that occur during dialing are suppressed by the integrator, so G_2 is not enabled.

The 100-V ac ringing signal might apply excessive reverse voltage to the light-emitting diode in the optical coupler. Therefore, the coupler input is shunted by a protecting 1N4154 diode.

Because the flash oscillator operates continuously, it can be connected to the NAND gates G_3 associated with a number of different phone lines and LEDs. In the author's office, one oscillator is used for 10 phones.

This circuit uses ordinary C-MOS ICs and operates from a noncritical supply voltage between 5 and 10 volts. The ac adapter from a pocket calculator is a convenient source. A single power supply can handle all of the phone lines.

The signals that are developed at the integrator and differentiator outputs can be used for other purposes than lighting a LED. Other areas of application include playing a recorded message when a phone rings, or running a timer while a phone is in use.

This circuit does not draw appreciable current from the phone line, feed back to the line, or reference any voltages to the line because the coupling is optical. Nonetheless, the telephone company should be consulted before the circuit is installed. □

Microprocessor converts pot position to digits

by John M. Schulein
Aeronutronic Ford Corp., Palo Alto, Calif.

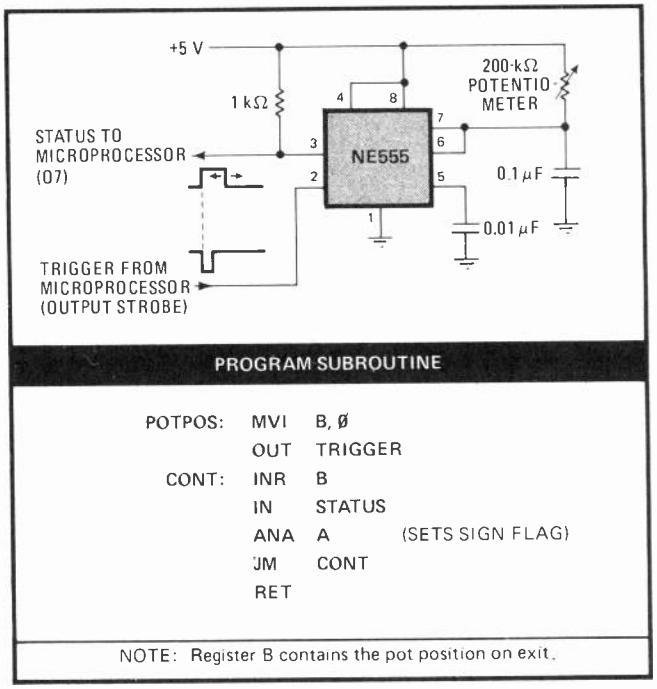
A few bytes of program in an 8008/8080 microprocessor, plus a 555 integrated-circuit timer, can convert the position of a potentiometer into a digital value. The arrangement is both economical and convenient when the position data is an input to a system already using the microprocessor, such as an industrial control system or a video game.

As the figure shows, a strobe pulse from the microprocessor triggers a 555 connected as a one-shot multivibrator. The output from the 555 stays high for a period of time that is proportional to the resistance of the pot. To measure this time period, the processor increments an internal register for as long as its input (D7) from the 555 remains high.

When data on the pot position is required, the microprocessor program calls up the POTPOS subroutine, which uses four flags, the accumulator, and the B register. In this subroutine, as the table shows, the processor:

1. Sets register B to 0.
2. Triggers the 555.
3. Increments register B.
4. Inputs the status of the 555 to bit D7 of the accumulator.
5. Sets a sign flag minus if status is high.
6. Jumps back to step 3 if flag is minus.
7. Returns to main program if flag is not minus.

Upon return to the main program, register B contains a number that measures the 555 output pulse duration and hence is a digital representation of the pot position.



Where is the pot? Potentiometer position is digitized by one-shot multivibrator and subroutine for the 8008/8080 microprocessors. When program calls subroutine, processor triggers one-shot and measures output pulse duration (which is proportional to resistance of pot). Register B stores this value for use in computation of next step in a TV game, process control, etc.

When the hardware and software are used on an 8008 system with a 2.5-microsecond clock, the B register digital output varies from 2 to 65 Hex, i.e., has 100 different values, as the potentiometer is varied across its range. The values of the pot and the timing capacitor can be modified to suit the speed of the processor and the desired range of the digitized output. □

Feedback in phase-locked loop linearizes phase demodulator

by Ron Rippy
Rf Technology Branch, Goddard Space Flight Center, Greenbelt, Md.

The phase of a carrier wave is easy to change, and therefore phase modulation (PM) is convenient in many applications. However, most phase detectors have at least two shortcomings: restriction of the linear operating region to about ±60° and an inability to lock to PM signals that have no carrier power. The circuit in Fig. 1 uses phase-compressive negative feedback to avoid these limitations. The linear operating region is set mainly by a phase modulator, rather than by the usual product detector, and extends to at least ±160°.

As shown in the circuit diagram, the data output from an ordinary phase-locked loop (PLL) is amplified, reversed in phase, and fed back to a linear phase modulator that is connected ahead of the product detector. Because the data fed back to the modulator is out of phase with the incoming data, it reduces the phase swing of the signal and restores some sideband power to the carrier. This carrier power allows the loop to lock to signals that had no carrier power before reaching the phase modulator.

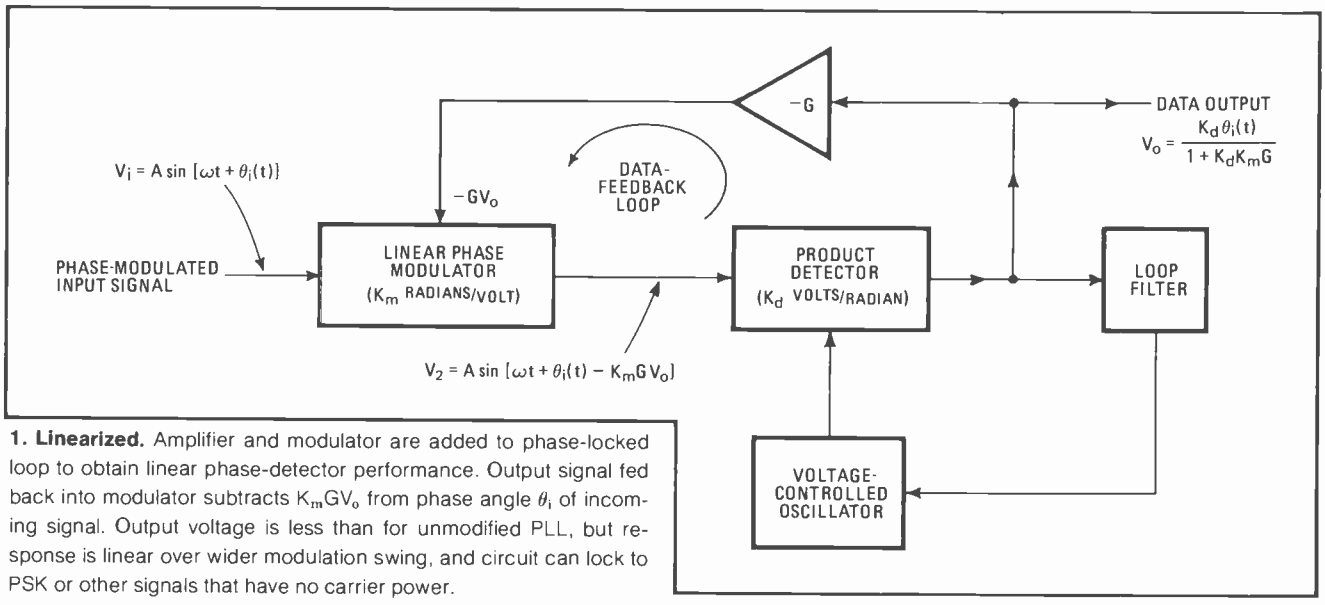
If an rf carrier is phase-modulated ±90° by a square wave, the carrier itself disappears, leaving only the modulation sidebands. This modulation technique is called phase-shift-keying. A conventional phase detector does not lock to such a signal because it has no carrier, but the circuit in Fig. 1 does lock. The amount of restored carrier power can be controlled by adjusting the gain of the feedback amplifier. This circuit can also be used to detect biphase modulation.

The compressive negative-feedback arrangement also tends to keep the product detector operating in its linear region at high modulation angles, where severe distortion would otherwise occur. The improvement in linearity is illustrated in Fig. 2, which shows the output of the phase detector when the input signal is a 2.2-gigahertz carrier modulated 160° by a triangular voltage. Without feedback, the detector distorts both the positive-going and negative-going ramps by turning them into segments of a sine wave.

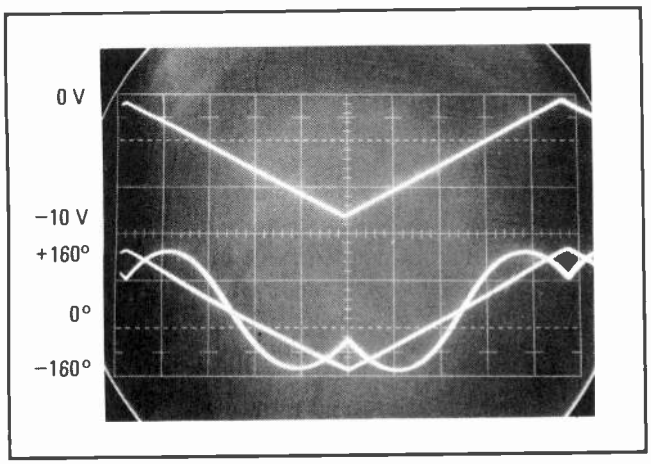
When the feedback loop is connected, however, the modulation swing is reduced, and operation in the linear region of the product detector is restored.

Another advantage of using feedback is that it increases the pull-in range of the phase-locked loop. When the loop is out of lock, the input signal is multiplied by the voltage-controlled-oscillator signal to produce a beat frequency that is fed back to the phase modulator. The beat note produces a modulation spectrum having one PM sideband that is always synchronous with the VCO frequency. This synchronous sideband results in a dc component at the output of the phase detector, which passes through the loop filter and pulls the VCO into lock. From experimental observation, the pull-in range appears to be of the same order of magnitude as the i-f bandwidth preceding the phase detector.

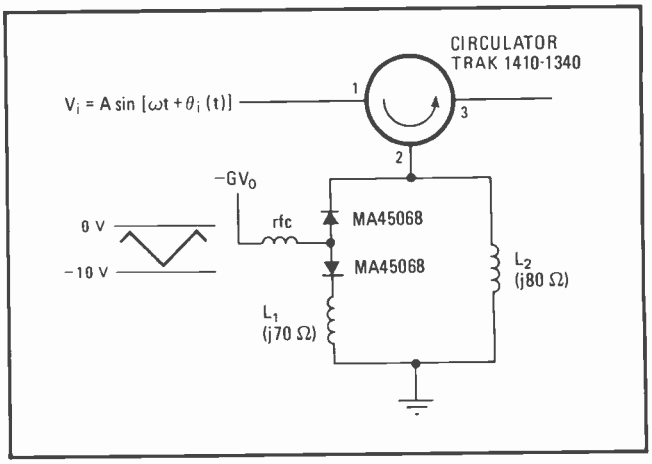
To prevent the data-feedback loop from oscillating, the open-loop gain must fall to 0 decibel before the open-loop phase shift climbs to 180°. This effect can be accomplished by using components in the loop that have wider bandwidth than needed and adding a single-pole or double-pole filter between the phase modulator and product detector to establish the over-all



1. Linearized. Amplifier and modulator are added to phase-locked loop to obtain linear phase-detector performance. Output signal fed back into modulator subtracts K_mGV_o from phase angle θ_i of incoming signal. Output voltage is less than for unmodified PLL, but response is linear over wider modulation swing, and circuit can lock to PSK or other signals that have no carrier power.



2. What you see is what you get. Effect of data-feedback loop on linearity is shown in scope photo. Top trace shows triangular voltage that modulates incoming 2.2-GHz carrier. Lower traces show detected angle without feedback (curved) and with feedback (linear).



3. Modulator. The linear phase modulator that is part of Fig. 1 can be realized at vhf and higher frequencies by use of a circulator and a variable reactance. Reflected signal in port 2 changes phase as voltage on back-to-back varactors changes.

data-loop bandwidth. If any sharp filtering is needed, it should be done ahead of the phase modulator. Then the data-loop bandwidth can be left rather wide to ensure a flat frequency response without degrading the phase-detection performance in the presence of noise.

Figure 3 shows the linear phase modulator that was used to implement the circuit for the test in Fig. 2. This modulator is useful at vhf and higher frequencies. (A similar modulator with a 3-dB hybrid in place of the circulator has been used at frequencies as low as 500 kilohertz.) The carrier enters port 1 of the circulator and travels to port 2, which is terminated in an LC combination that is voltage-tuned by two varactor diodes. Because this termination is purely reactive, all of the energy at port 2 is reflected to the rf-output port.

The angle of the reflected carrier varies with the modulating signal applied to the diodes. One modulator section of this type will produce about ±90° of linear modulation. Two sections were cascaded to produce the ±160° phase shift in Fig. 2. □

PROM converts binary code to drive 1½-digit display

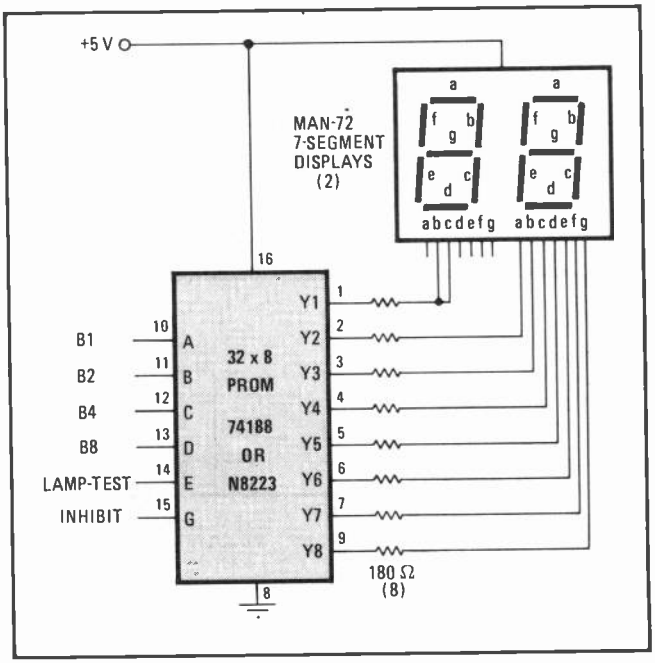
by V.R. Godbole
North Electric Co., Galion, Ohio

In providing visual readouts for test circuits, inspection equipment, error indicators, and the like, it is often necessary to go from a machine-generated 4-bit binary code to a 1½-digit display of the numbers 0 to 15. This process is usually performed in two steps, but a programable read-only memory can handle it in one.

In the usual approach, the first step is to convert the binary code into a BCD code by any one of the several available techniques. The second step is to use standard BCD seven-segment decoder/driver integrated circuits to drive the popular seven-segment visual readouts. The PROM, however, can be programed to accept the binary input signals and generate the proper outputs to drive the display directly.

This use of a PROM has several advantages. Conversion and driving are done in one step, thus providing direct interface to the visual display. Blanking and lamp-test can be included at no extra cost. Space is conserved, and cost is competitive with other approaches.

Binary coding of the numbers from 0 to 15 requires



Here's how. PROM drives seven-segment display to show decimal value of 4-bit input signal. This compact interface is convenient in microprocessor circuits, which often have spare PROM capacity. A 32-by-8-bit PROM can provide the drive signals for numbers 0 through 15 and also accommodate lamp-test and inhibit commands. Applications include test-number indication in small test instruments and display of settings on binary-output touch switches.

only four binary bits. The most-significant-digit position of the visual decimal display requires only a 1 or else no indication at all; therefore, this digit can be driven by generating only a single output signal that can turn on the segments to show a 1 when required. To drive the seven segments of the least significant digit, seven outputs are needed. Thus the converter/driver must accept four binary inputs and produce eight outputs to drive display segments.

A 32-by-8-bit PROM, type 74188 or N8223, can serve this purpose. The PROM has open-collector outputs with sink capability of 16 milliamperes per output at output voltage of 0.5 volt, enabling it to interface directly with the display segments through suitable resistors. Also, besides performing the necessary conversion, the PROM has additional word capacity that can be used for desirable features such as blanking and lamp-testing at no additional expense. The figure shows the complete circuit diagram for the converter; it requires only the display devices and eight resistors in addition to the memory IC. The truth table lists the instructions required to program the PROM.

Locations 0 through 15 contain the bit patterns that generate segment drives to produce numbers from 0 to 15. Locations 16 through 31 are left unprogramed; therefore when the lamp-test input is taken to a logic 1, one of locations 16 through 31 is addressed. This circuit state causes all outputs to be set at logic 0, turns all segments on, and produces the number 18. When the inhibit input is taken to a logic 1, the PROM outputs are turned off and cause the display to be blanked. □

TRUTH TABLE AND PROGRAM FOR DRIVING 1½-DIGIT DISPLAY

Inhibit	Lamp test	B8	B4	B2	B1	Display	Program in memory Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8
0	0	0	0	0	0	0	1	0	0	0	0	0	0	1
0	0	0	0	0	1	1	1	1	0	0	1	1	1	1
0	0	0	0	1	0	2	1	0	0	1	0	0	1	0
0	0	0	0	1	1	3	1	0	0	0	0	1	1	0
0	0	0	1	0	0	4	1	1	0	0	1	1	0	0
0	0	0	1	0	1	5	1	0	1	0	0	1	0	0
0	0	0	1	1	0	6	1	1	1	0	0	0	0	0
0	0	0	1	1	1	7	1	0	0	0	1	1	1	1
0	0	1	0	0	0	8	1	0	0	0	0	0	0	0
0	0	1	0	0	1	9	1	0	0	0	1	1	0	0
0	0	1	0	1	0	10	0	0	0	0	0	0	0	1
0	0	1	0	1	1	11	0	1	0	0	1	1	1	1
0	0	1	1	0	0	12	0	0	0	1	0	0	1	0
0	0	1	1	0	1	13	0	0	0	0	0	1	1	0
0	0	1	1	1	0	14	0	1	0	0	1	1	0	0
0	0	1	1	1	1	15	0	0	1	0	0	1	0	0
1	X	X	X	X	X	(OFF)	1	1	1	1	1	1	1	1
0	1	X	X	X	X	18	0	0	0	0	0	0	0	0

1 = HIGH 0 = LOW X = DON'T CARE

Sensing resistor limits power-supply current

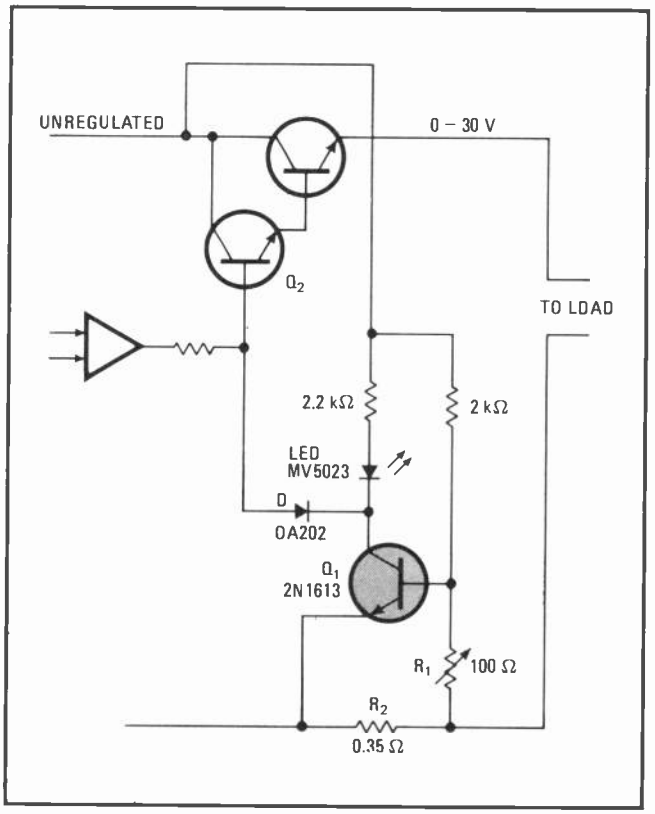
by Theo W. Smit
Euratom, Ispro, Italy

To protect a power supply against the excessive currents that would flow if the load were short-circuited, a simple drive-shunting transistor controlled by a sensing resistor is all that is necessary. As described here, the protection circuit is adjustable and includes an indicator light to warn of the current-limited condition.

The schematic diagram shows the current limiter connected in a 30-volt/2-ampere power supply. If adjustable resistor R_1 is set at zero, then the load current is limited to 2 A. If the current exceeds this level, the voltage drop across R_2 turns on transistor Q_1, which sinks the input current to driver transistor Q_2. Thus the load current is limited to the 2-A level.

If R_1 is set greater than zero, Q_1 turns on at a current less than 2 A, limiting the load to this reduced level.

The light-emitting diode lights up when Q_1 conducts, indicating that the current limiter is in operation. Diode D prevents the LED from lighting if Q_1 is off. □



Protective limiter. To limit current in power-supply circuit, voltage drop across resistor R_2 turns on transistor Q_1 when load current exceeds 2 amperes (current value will be lower if R_1 is greater than 0 ohm). Q_1 then shunts drive current away from Q_2, reducing current to the load. LED turns on to indicate conduction in Q_1.

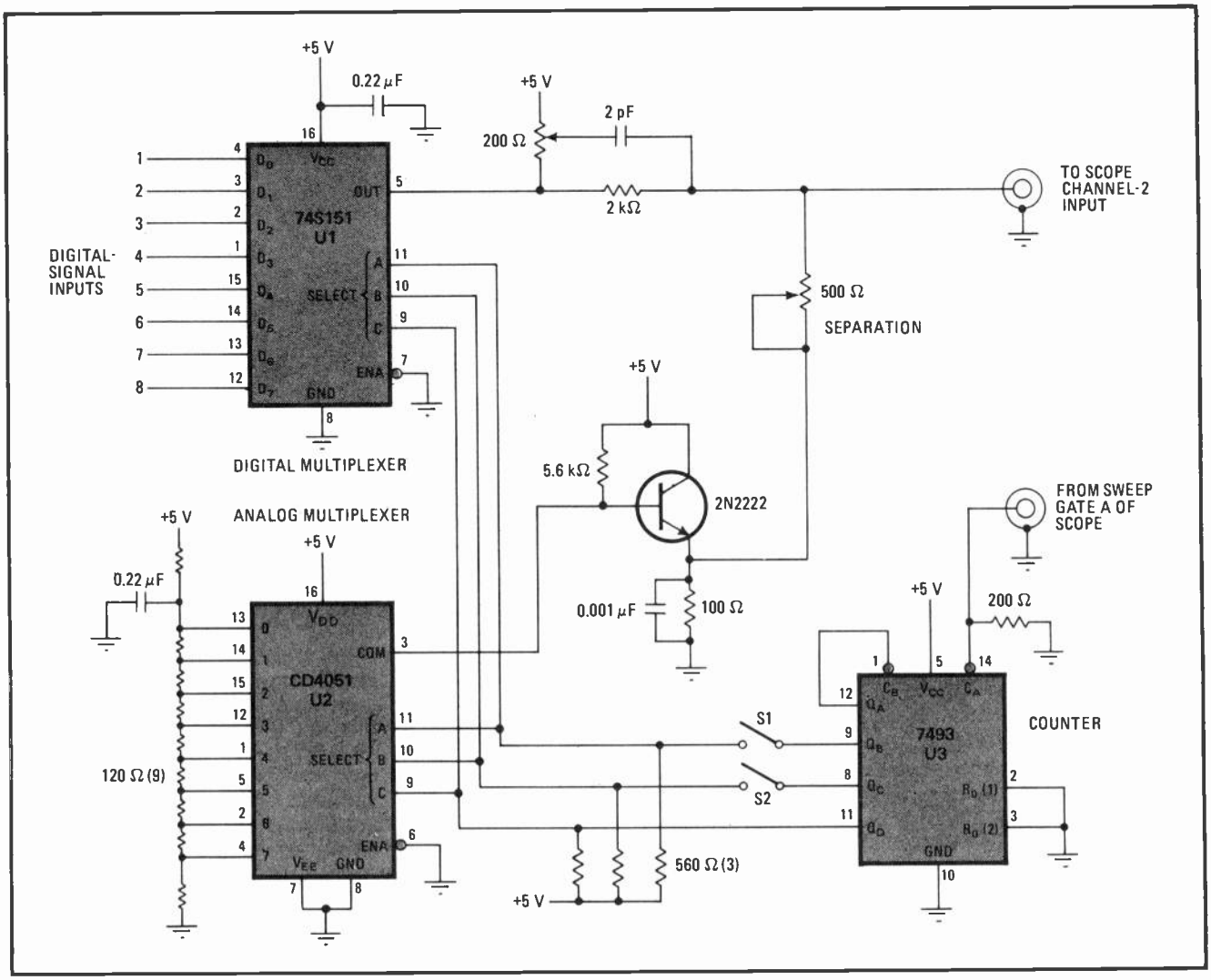
Scope display of eight signals helps debug sequential logic

by Matthew L. Fichtenbaum
General Radio Co., Concord, Mass.

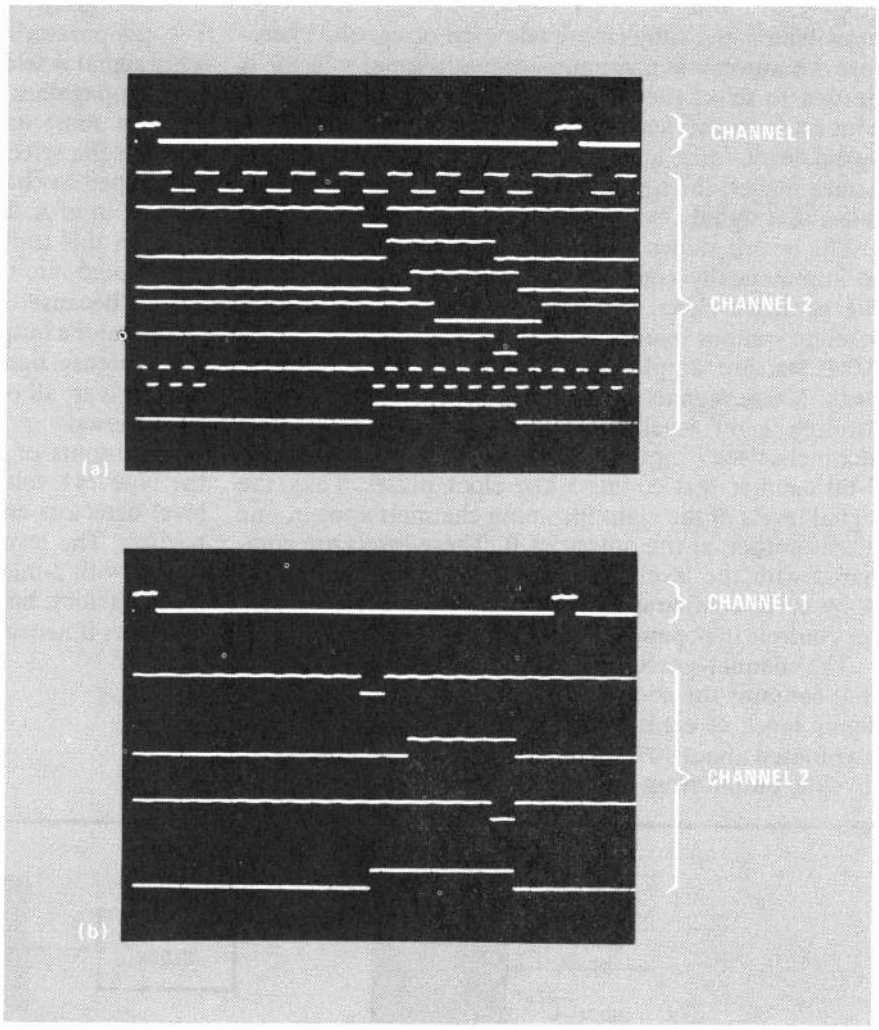
When debugging sequential logic, an engineer may have to observe several signals simultaneously. Logical states and the times that they change are of primary importance in the visual display; the exact values of voltage levels and the duration of rise times and fall times are of lesser importance.

Two, four, or eight digital signals can be displayed on one of the two channels of a Tektronix 454 or similar dual-trace oscilloscope, as demonstrated in the photographs on the next page. The other channel may then be used for triggering or for observation of a ninth signal. The eight signals are treated as logic levels and are gated by a digital multiplexer. Although this procedure does not preserve voltage levels and wave shapes, it does achieve maximum speed with simple circuitry.

The circuit for displaying the signals on the scope is illustrated in Fig. 1. The 7493 divide-by-16 counter (U3) is incremented after each scope sweep. The counter steps through the eight inputs sequentially, and the extra stage compensates for the use of every other sweep in the "alternate" display mode. The counter's highest three bits select an input signal via digital multiplexer U1, which is a 74S151 TTL Schottky type. At the same time, the CD4051 C-MOS analog multiplexer U2 picks a dc voltage off a resistor chain. This voltage is summed



1. Multi-trace adapter. Two, four, or eight digital input signals time-share the channel-2 trace of a dual-trace oscilloscope by means of this circuit. The digital multiplexer selects individual digital inputs in cyclic succession, and the analog multiplexer separates their wave forms vertically; sweep counter drives multiplexers. Switches S_1 and S_2 permit display of only two or four digital wave forms, instead of eight.



2. Signal tracing. Channel 2 of dual-trace scope is multiplexed to display eight different logic wave forms in (a) and four wave forms in (b). The channel-1 trace, used for triggering, appears at top in both photos; it is brighter than the channel-2 traces because of its higher duty ratio. This simultaneous display of several signals is convenient for logic-circuit debugging. High and low states, and the timing of their changes, are indicated accurately even though the multiplexing does not preserve voltage levels and wave shapes. The multi-trace adapter circuit is shown in Fig. 1 on the preceding page.

with the digital signal, providing a different reference level for each trace and thus separating the traces vertically from each other on the screen, as shown in Fig. 1.

The 500-ohm variable resistor adjusts the magnitude of the dc offset, varying the trace separation. The scope's variable vertical-sensitivity control may be used to adjust the over-all display amplitude. The 200-ohm potentiometer is adjusted for best transient response. Both the 500-ohm and 200-ohm pots should be cermet or other noninductive types. The three 560-ohm resistors pull up the levels of the inputs to the multiplexers.

The resistor chain could be replaced by eight potentiometers in parallel, with their wipers connected to the input terminals of the CD4051, for separate adjustments of the vertical positions of the individual traces.

If switch S_1 is open, the scope displays only four traces (digital inputs 1, 3, 5, 7). If both S_1 and S_2 are open, only two inputs (3 and 7) are displayed.

This time-division-multiplexing of channel 2 on the dual-trace scope of course makes the signal wave forms less bright than the channel-1 trace. In Fig. 2(a), the top trace is scanned eight times as often as each of the lower eight traces, and in Fig. 2(b), channel 1 is scanned four times as often as any one of the four offset wave forms that share channel 2.

The circuit may be built in a small box, with appropriate connectors to the scope and inputs. It should be used near the logic circuit under test to minimize signal-lead length and circuit-loading. Only 5 volts of dc power are required. □

Logic circuit selects most intense signal

by P. V. H. M. L. Narasimham
Indian Institute of Technology, Kanpur, India

In police wireless communications where each patrol car has its own frequency, messages from the cars are received at police headquarters via satellite receiver stations to avoid blind angles, obstacles, and dead zones. An operator at headquarters could select the best signal from these stations by manually sampling the various outputs from the HQ receiver and comparing their volumes. This method is unsatisfactory because of delays

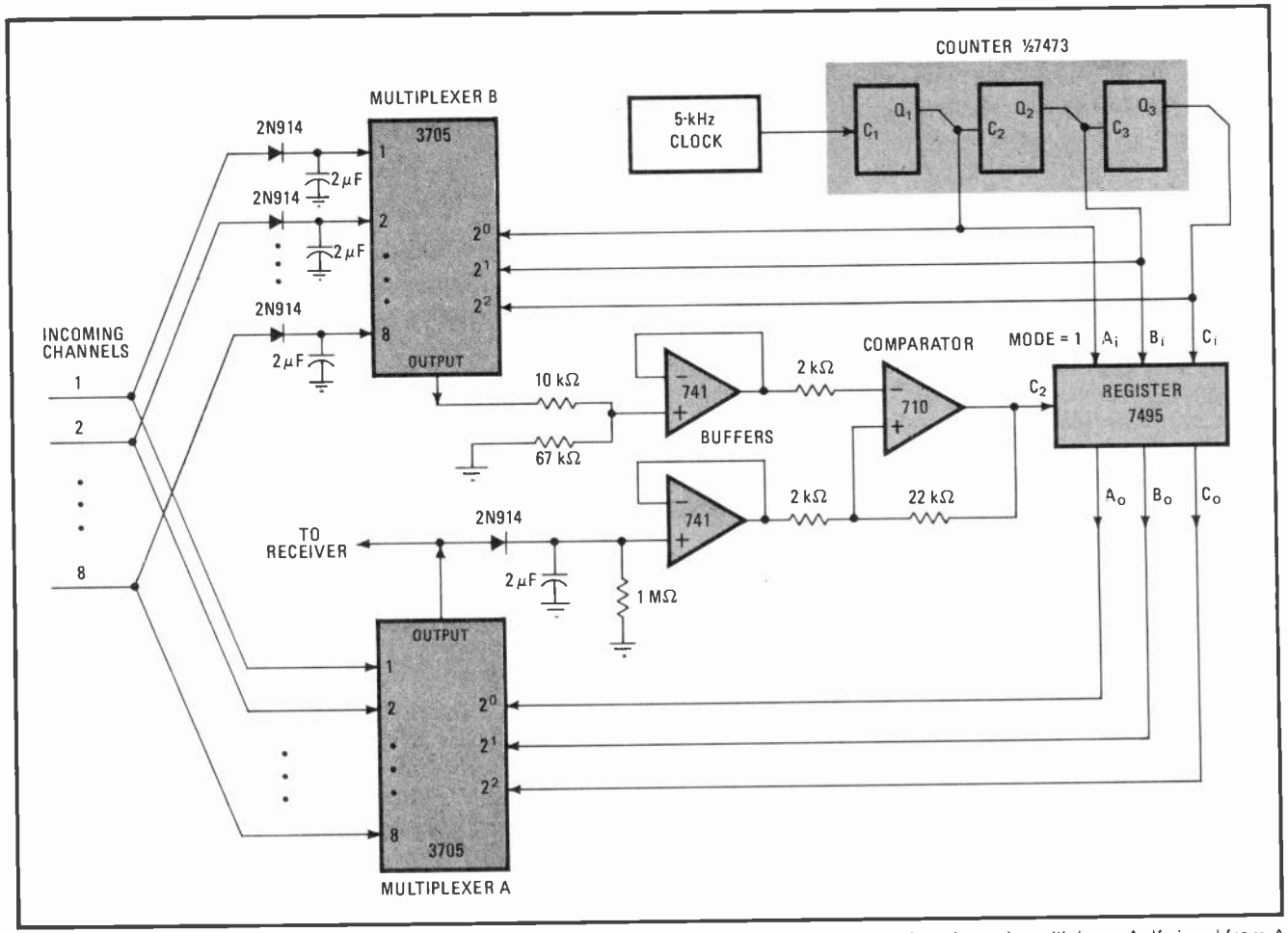
in switching and subjective evaluation of signals. Therefore, an automatic maximum-strength-signal selector is needed to select the strongest of incoming signals and connect it to the headquarters receiver. Whenever the signal level from any unselected relaying station becomes higher, the headquarters receiver must promptly select that signal.

The circuit shown uses a pair of analog multiplexers to automatically connect the headquarters receiver to the strongest signal. The incoming signals from eight satellite stations, band-limited to the range from 300 to 3,000 Hz, are amplitude-limited to ±5 volts peak to peak. These signals go to multiplexer A and also go through eight level-detectors to multiplexer B. The channel-selector inputs to multiplexer B are driven by a 3-bit counter that counts 5-kHz clock pulses. Thus, the signal levels of the eight incoming channels appear, one after another, at the output of B. These levels are compared with the level-detected output from multiplexer A by a 710 comparator. The output from the comparator controls the operation of a 7495 register.

The channel-selector inputs to A come from a register that contains the code for the channel with the highest signal level, as explained below. The output from B is attenuated about 10% by the resistive voltage divider, to give the output from A an advantage in the comparator. The comparator's output is high as long as the most intense signal is selected by A.

If propagation conditions change so that the signal level on some unselected channel, say U, exceeds the level on the selected channel, then when multiplexer B is switched to channel U the output of B is higher than the output of A. Therefore the comparator's output goes low. On this trailing edge, the contents of the counter are clocked into the register so that A also selects channel U. Because of the 10% advantage given to A, the comparator's output then becomes high again. Thus the most intense signal is selected by A and connected to the receiver; all of this takes place within a fraction of a clock period.

The inputs of the comparator are buffered through the type 741 voltage followers to avoid loading on the level detectors and thus preserve the accuracy of comparison. The level detectors are simple diode peak detectors with 2-microfarad capacitors. Their performance is satisfactory, but they may be replaced by better level-detectors if necessary. □



Goes with strength. Most intense signal coming from relaying stations is connected to central receiver through multiplexer A. If signal from A is not the strongest, comparator goes low when counter clocks multiplexer B to the stronger signal. Register then changes input code to A so that the stronger signal is connected to receiver. System allows police cars (each with own frequency) to contact HQ via satellite stations.

Logic circuit tests wiring assemblies

by Steven Graham
Parsippany, N. J.

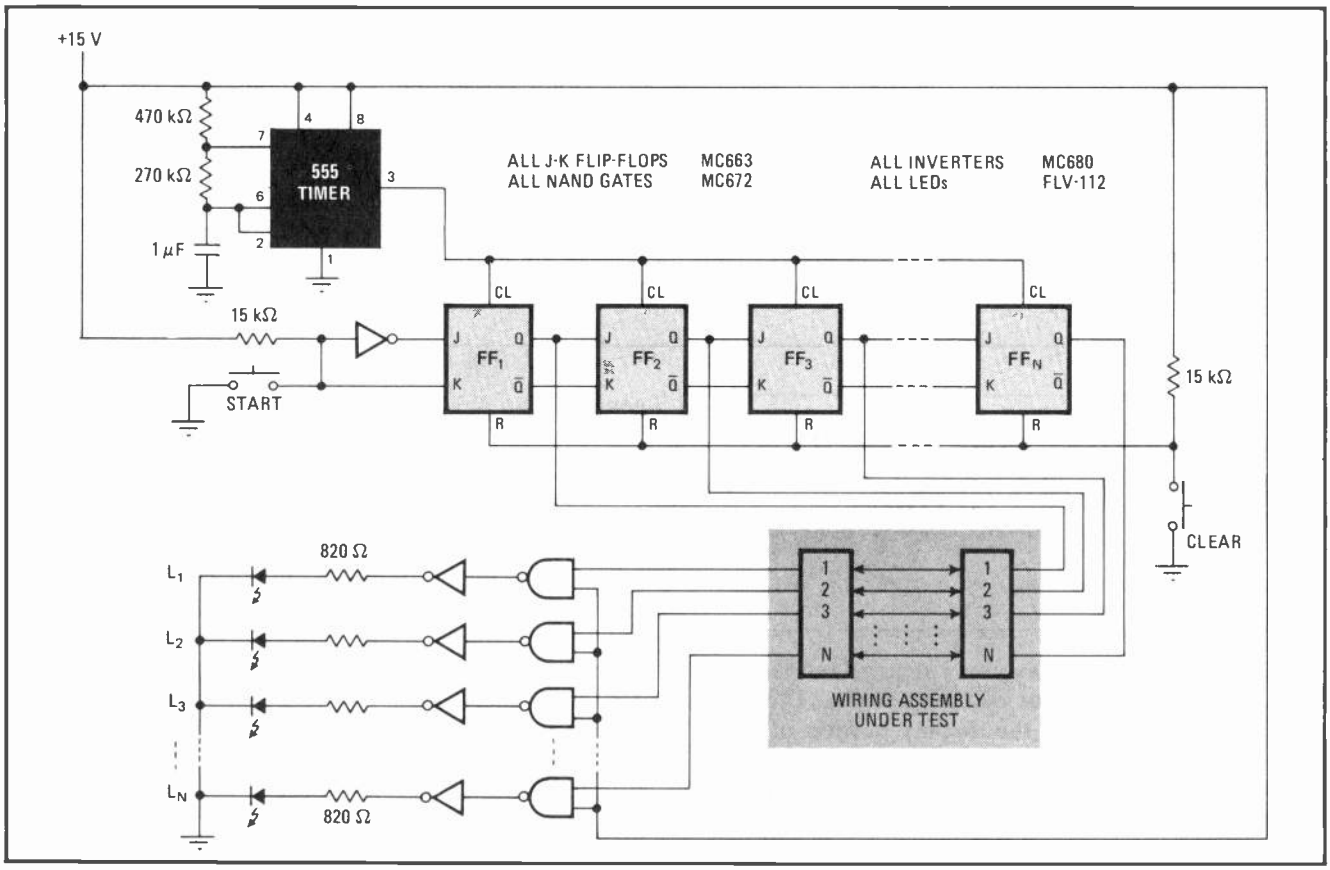
Before shipment or installation of wiring harnesses, the completed assemblies must be checked to verify that each pin of the connector at one end is wired to the corresponding pin of the connector at the other end. Open circuits, short circuits, and crossed wires can quickly be detected and identified by a testing circuit consisting of a pulse generator, a shift register, some gates, and light-emitting diodes. This circuit, shown in Fig. 1, provides an inexpensive and effective replacement for stepping switches, ohmmeters, and expensive analyzers.

To check a wiring assembly, the test-station operator plugs the two connectors into the test fixture, presses the CLEAR button if any of the LEDs is on initially, and then presses the START button. If the harness has been wired correctly, the LEDs turn on and off sequentially. Crossed wires are indicated when the LEDs come on out of sequence. A short circuit causes two LEDs to light simultaneously. An open circuit turns the LED on as soon as the harness is connected.

The circuit diagram shows that the 555 timer is connected as a free-running multivibrator with a frequency of a few hertz. The pulse train from the 555 clocks the flip-flops to shift the high starting pulse down the line, feeding a high input to each NAND gate sequentially.

If a wire in the harness is not connected, so that the input to a NAND gate is not connected to its flip-flop, that gate stays high all the time (even when the CLEAR button is pushed), and the LED stays on. If the wire bundle contains N wires, then N flip-flops and N LEDs are required. The 1-microfarad capacitor and the two resistors connected to the 555 may be changed to increase or decrease the test rate.

This circuit has been used for more than a year to check 12-wire jumper harnesses. It could be refined so that the LEDs turn on sequentially and stay on if the wiring is correct, and a latch could halt the sequential shift when a fault is located. The operator could do other things while the test proceeded; this improvement would be especially useful for many-wire harnesses. □

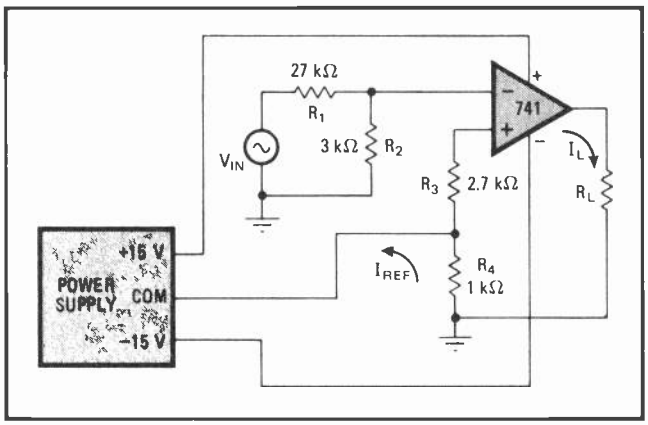


Flashing the word. Test arrangement checks feed-through wiring between two connectors on harness of N wires. Correct continuity is indicated by LEDs flashing on and off sequentially. Crossed wires cause LEDs to flash out of sequence, a short circuit makes two LEDs flash simultaneously, and an open causes a LED to glow continuously. Although high-threshold-logic elements are shown, TTL is satisfactory.

Controllable current source eliminates matched resistors

by James A. Stanko
State Univesity of New York, Stony Brook, N.Y.

A bipolar constant-current source that has a grounded voltage source and a grounded load is usually limited in accuracy and internal impedance by the degree of matching of two or more resistors. For the circuit below, however, no matched resistors are required; linearity and internal impedance are determined solely by the operational amplifier gain, offset, and power supply rejection ratio. This circuit takes advantage of the fact that the op amp's power supply can usually be floated.



Uncritical. Load current produced by this circuit depends on input voltage, not load resistance. Circuit does not require matched resistors for accurate control of current, but power supply must float.

To understand the operation of the circuit, remember that no current to speak of flows into the input terminals of the op amp under feedback conditions, and no voltage difference exists across the terminals. Thus, the op amp drives the common terminal of the power supply to the voltage level established at the inverting input. This voltage appears across the reference resistor R_4. It is set to a suitably low value by input attenuator R_1 and R_2 to avoid thermally induced errors caused by power dissipated in the reference resistor. The values of R_1 and R_2 are chosen to provide a convenient scale factor. The reference current thus established is exactly equal to the current flowing in the load, and therefore the load current is

$$I_L = -I_{ref} = -\frac{V_{in}}{R_4}\,\frac{R_2}{R_1 + R_2}$$

The value of load current does not depend upon the value of load resistance and can be controlled by the value of V_{in}.

The minus sign in the expression for load current indicates the degenerative feedback action of the circuit. If I_L increases, the extra voltage drop through R_4 drives the noninverting input of the op amp lower and thus decreases the output.

Resistor R_3 is made equal to the parallel combination of R_1 and R_2 to minimize any error caused by input bias current. For the values shown in the figure, input voltages up to ±10 volts produce current outputs up to ±10 milliamperes.

This circuit has been used for over a year to supply current to electromagnets. In this application it is boosted by an emitter follower for greater output current and more voltage compliance. □

Graduated-scale generator calibrates data display

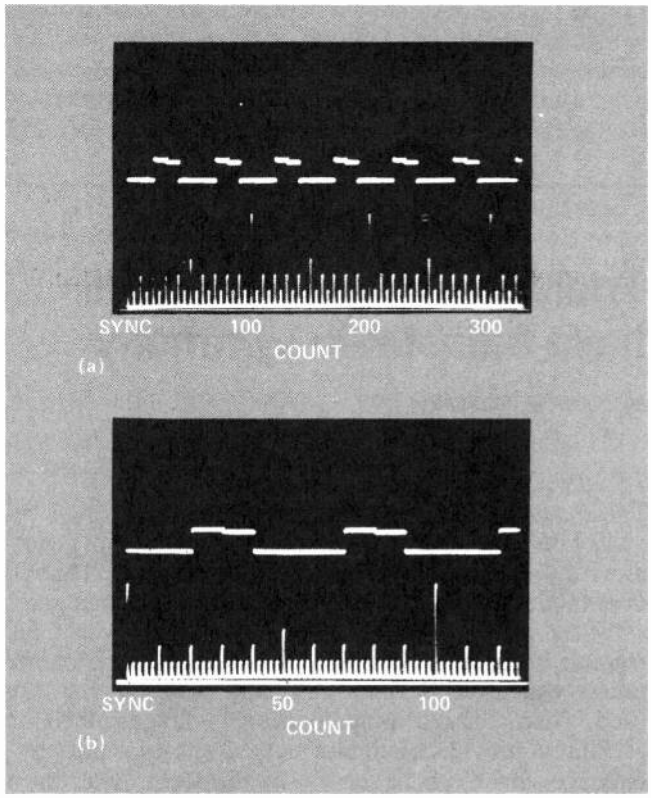
by Ken E. Anderson
IBME, University of Toronto, Canada

Scope and chart displays may require reference signals to indicate timing or counting scales. The circuit shown here is added to the display portion of a real-time digital data correlator at a cost of $3 or $4 to provide a graduated scale below the correlation display on a two-channel scope. Although it lacks the precision of a cursor, the continuous scale offers greater versatility and speed of operation. It also references the display data when stored on hard copy.

The photographs in Fig. 1 show two scales that can be generated to aid the observer in determining the pulse count or time at which a wave form rises or falls. In the lower trace of Fig. 1(a), every fifth clock pulse is indicated, and in Fig. 1(b), every second clock pulse is indicated. The upper trace in each photo shows a wave form that goes high at count 20, low at 40, high again at 70, low again at 90, and so forth. These counts can be read easily and accurately from the reference scales.

As shown in Fig. 2, the scale generator is remarkably simple. For two decades of unique graduations, two decade counters (7490) and one package of open-collector AND gates (7409) are required. These gates switch a crude voltage-divider digital-to-analog converter, generating the various pulse heights. Gate A in Fig. 2 ANDs the system clock with the basic scale unit—five in Fig. 2(a) or two in Fig. 2(b)—enabling the voltage-divider output to rise. Low gates B, C, or D (or combinations) clamp the output to appropriate levels as determined by R_1, R_2, R_3, and R_4. As higher-order counters progres-

1. Measurement aids. Graduated scales are generated on dual-trace scope or chart to facilitate probing of displayed data. In lower trace (a), every fifth clock pulse has a spike; in lower trace (b), every second clock has one. From these scales, observer sees that upper trace rises at count 20 and falls at count 40. Circuits for generating scales are shown in Fig. 2.

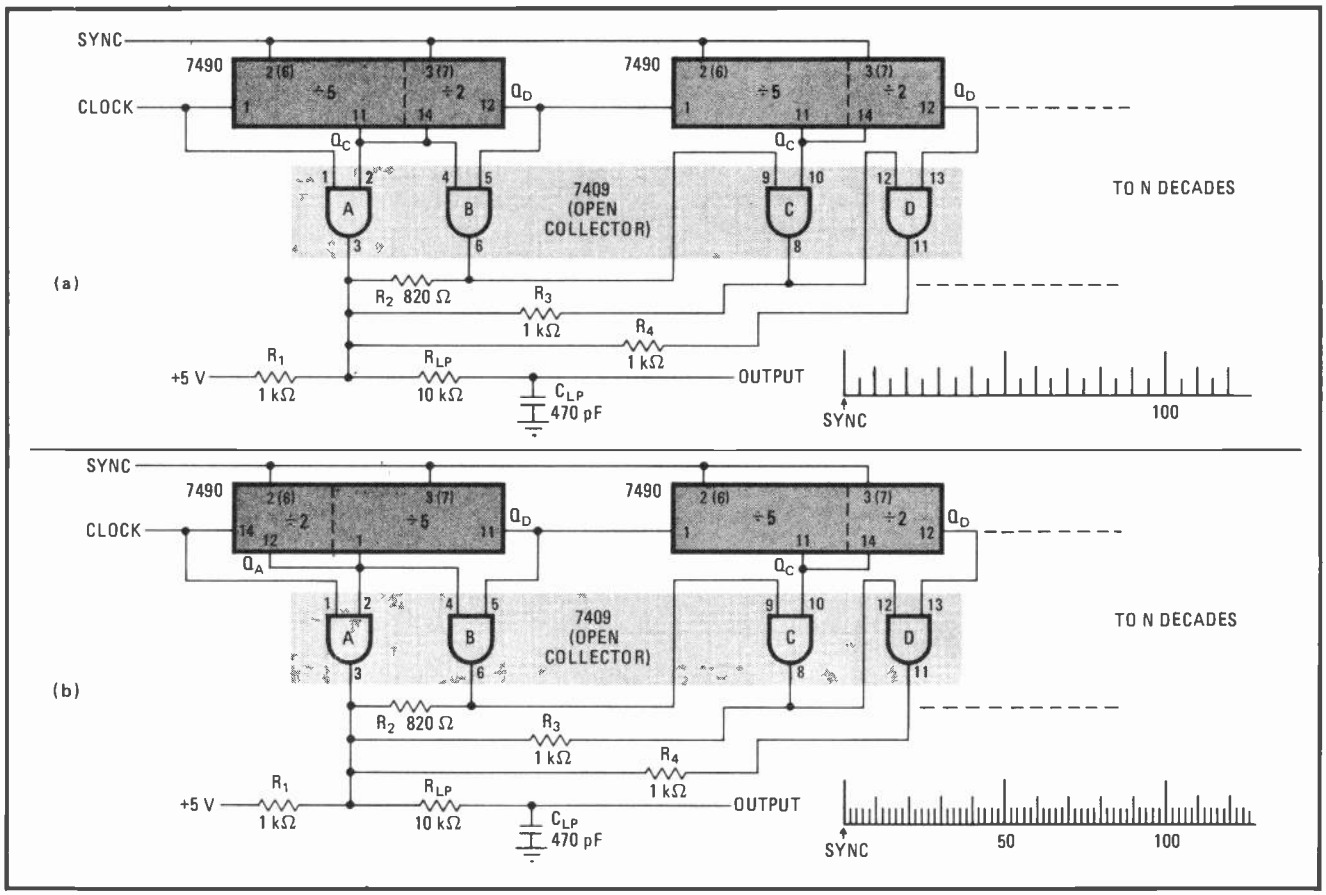


sively flip high, taller graduations are created.

Use of the 7490's quinary and binary counters obviates the need for extensive decoding. For example, the output of gate A in Fig. 2(a) goes high on the clock high of count 4, (9, 14, 19, etc); gate B ANDs this high signal with counts 5–9 (15–19, 25–29), thus decoding count 9 (19, 29). The cascaded decade circuit decodes counts 49 and 99. For display on a scope, a low-pass filter or integrator consisting of R_{LP} and C_{LP} is added to improve the appearance of the scale by increasing the rise and fall times of the pulses. Relative pulse heights may be altered via resistor ratios of R_1, R_2, R_3, and R_4. However, to ensure adequate noise margin at inputs of gates C and D, R_1 must not be greater than R_3 or R_4.

Synchronization of the scale generator to the scope and system output is accomplished by providing a pulse to reset the counters to zero (pins 2, 3) for graduations on counts 4, 9, 14, 19, etc. or to maximum (pins 6, 7) for graduations on counts 5, 10, 15, 20. . . .

The use of this graduated-scale generator can ensure



2. Here's how. Circuits for generating graduated scales of incoming clock pulses use decade counters. Two AND gates per decade switch voltage-divider d-a converter to produce various pulse heights; the AND gates have open collector outputs. Each counter in (a) divides by 5 and then by 2 to provide scale with a basic unit of 5 counts. In (b), first counter divides by 2 and then by 5 to provide a basic unit of 2. Second counter divides by 5 and then 2 to enhance pulses at 50 and 100. Values of R_{LP} and C_{LP} shown here are chosen for use with a 10-kHz clock.

precise tagging of displayed data even when the scope is being operated in the magnify, delayed-sweep, and uncalibrated-sweep modes. Other applications include generation of a time scale for sweep calibration of scopes (when clocked by a high-precision source) and generation of a clock-pulse scale for troubleshooting cyclic sequences. The latter application is illustrated by the upper traces in the two photographs; this waveform is actually the output of the second bit of the second quinary counter (pin 8 of the second 7490). □

Triangular waves from 555 have adjustable symmetry

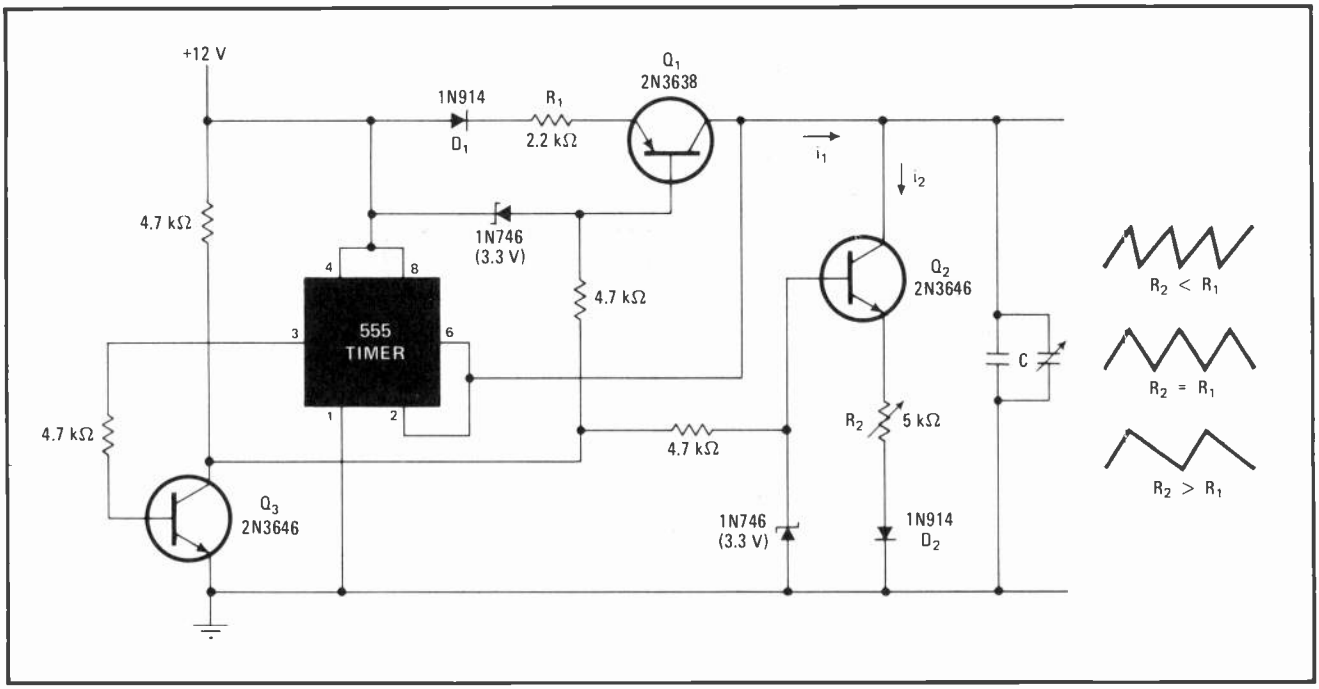
by Devlin M. Gualtieri
University of Pittsburgh, Pittsburgh, Pa.

The fixed-frequency triangular waveform so often required in pulse-duration modulators or sweep generators too often turns out costly to implement. Though operational-amplifier circuits can develop a triangular wave by integration of a square wave, the tips of the triangle become blunt at frequencies above 10 kilohertz unless expensive devices with high slewing rates are used. Also, though single-package voltage-controlled oscillators provide triangular output, they are not cost-effective for fixed-frequency applications, and most have high current drain. However, an inexpensive 555 timer and some transistors can generate triangular waves at frequencies up to about 100 kHz.

The circuit shown generates a triangular waveform by alternately charging and discharging a capacitor. The transistors Q_1 and Q_2 with their zeners act as a switched-current source and a switched-current sink that are activated by Q_3. When Q_3 is on so that its collector is low, the Q_1 current source is switched on, and a current i_1 charges capacitor C. The linear voltage ramp that appears across C corresponds to the charging law $dV/dt = i_1/C$.

Voltage V across the capacitor increases until it reaches a level that is two thirds of the supply voltage, which is the upper trip point of the 555 timer. The voltage at pin 3 of the timer then goes low, turning off Q_3. Since the collector of Q_3 is thus made high, the Q_1 current source is deactivated, and the Q_2 current sink is switched on. The capacitor is discharged by i_2 until the lower trip point of the 555 timer is reached, at one third of the supply voltage. At this point the 555 changes state and the cycle repeats. Thus the output voltage varies from 4 V to 8 V if the supply is 12 V.

Q_1 and Q_2 may be any high-gain pnp and npn transistors, such as 2N3638 and 2N3646. Q_3 may be any npn switching transistor, such as 2N3646. The forward voltage drops of D_1 and D_2 ensure turn-off of Q_1 and Q_2. Resistor R_2 is a symmetry adjustment, controlling the discharge rate of C by varying i_2. For the values shown, the frequency in hertz of the symmetrical triangular wave form is roughly 75/C, where C is in microfarads; thus, C determines the frequency. □



Ups and downs. Triangular waveform is generated across capacitor C by alternately charging and discharging through emitter-follower constant-current sources consisting of transistors Q_1 and Q_2 plus their zener diodes. Current sources are turned on and off by 555 timer.

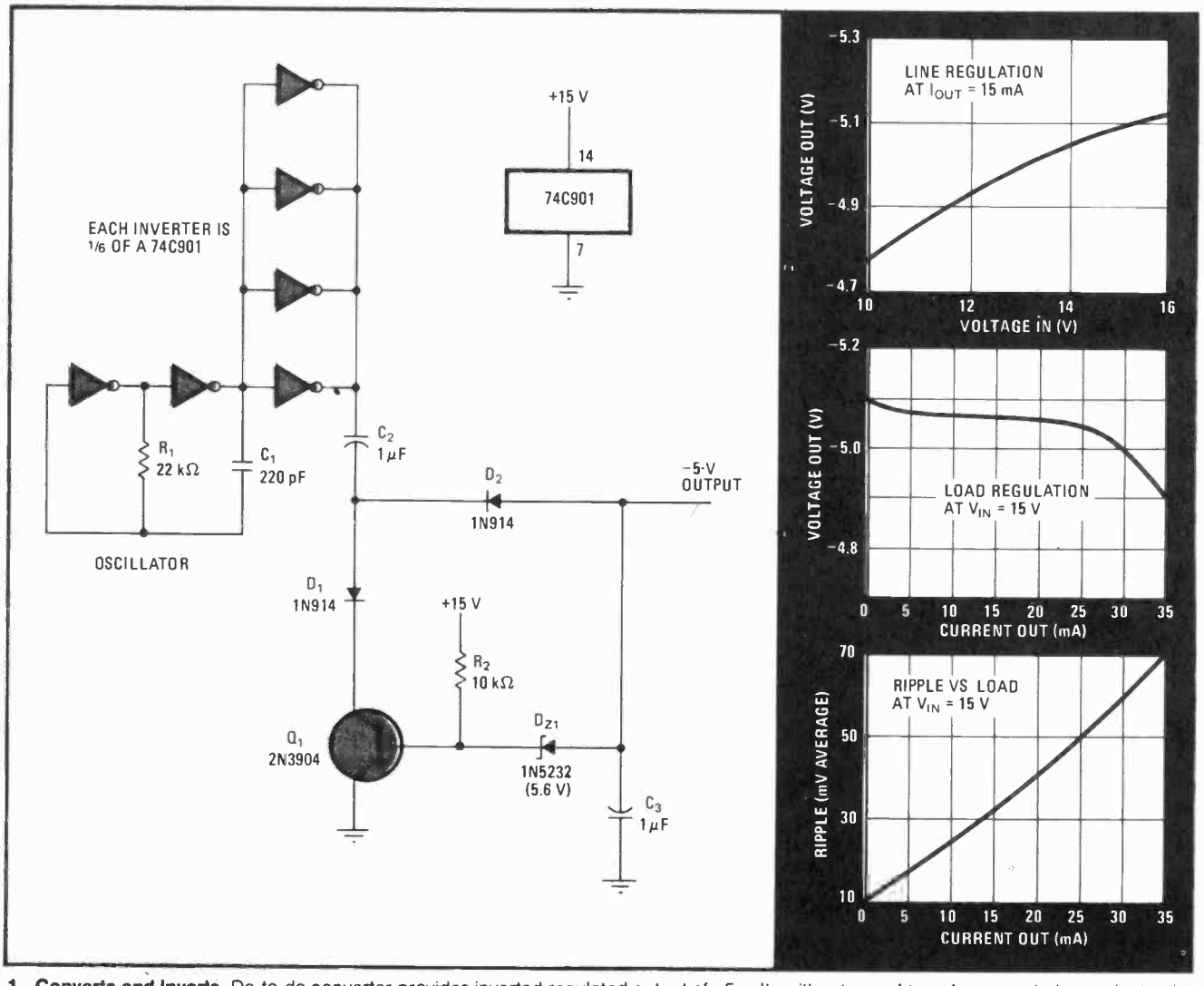
Inverting dc-to-dc converters require no inductors

by Craig Scott and R.M. Stitt
Burr-Brown Research Corp., Tucson, Ariz.

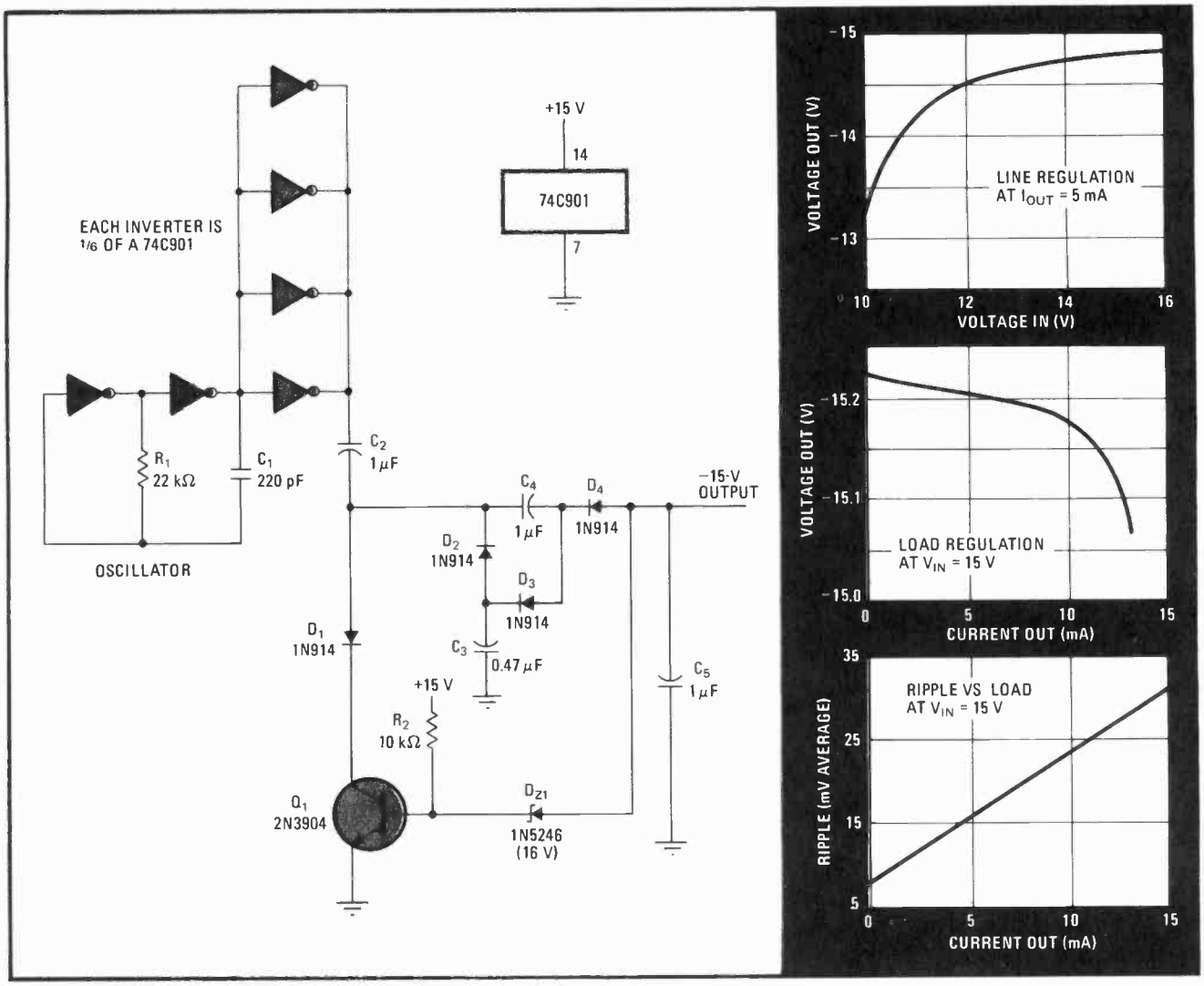
Many systems require a modest negative power source where only a positive power supply is available. Such a negative voltage can be produced by an inverting dc-to-dc converter installed right where it is needed. This arrangement is especially convenient in systems where the dc power is supplied remotely because only two wires need to be run to the point of use, instead of three. The inverting dc-to-dc converter described here requires no expensive transformers or inductors. Noise spikes associated with switching inductive loads are therefore eliminated.

To understand the operation of the circuit, consider first the -5-volt converter shown in Fig. 1. Resistor R_1, capacitor C_1, and two inverters form a free-running 100-kilohertz oscillator. The remaining four inverters in the hex-inverter package form a power driver. On the positive swing at the output of the power driver, C_2 is charged through diode D_1 and transistor Q_1 (assuming that Q_1 is on). When the output of the power driver drops back to zero, D_1 reverse-biases and D_2 forward-biases, so charge is transferred to C_3.

As the cycle repeats, C_3 is charged to a negative voltage that approaches the positive-output swing minus the diode drops, power-driver drop, and the drop across Q_1. Q_1 is held on by R_2 until the base-drive current is shunted away by the breakdown of D_{Z1}. This occurs when the negative output voltage exceeds the break-



1. Converts and inverts. Dc-to-dc converter provides inverted regulated output of -5 volts without use of transformer or inductor. Instead, it puts negative potential on C_3 by discharge of C_2 during off-cycle of oscillator. Performance curves show data for typical units.



2. More volts. Addition of voltage-multiplier stage to circuit in Fig. 1 allows it to deliver a regulated output of −15 V. These inverting-converter circuits are convenient for producing negative voltages at locations remote from the main positive power source.

down voltage rating of D_{Z1}, less the V_{BE} of Q_1. Thus, the output voltage is regulated at $V_{out} = -(V_{Z1} - V_{BE})$.

With the output loaded, the negative output voltage of this circuit evidently cannot exceed that of the positive power-supply input in size. It is possible, however, to modify the circuit so that it produces a negative voltage equal to or larger than the input voltage. By adding a voltage-multiplier stage to the circuit of Fig. 1, for instance, the maximum possible output voltage can be doubled.

Such a circuit is shown in Fig. 2, in which C_4 is charged through D_3 on the positive swing of the power-output stage. However, now C_4 is charged from the negative voltage that appears at the negative terminal of C_3. The voltage across C_4 then approaches twice the input voltage, minus the drops. This voltage is transferred to the output capacitor as before. The negative-output voltage can therefore approach twice the input voltage, less the drops. □

Photocoupler provides agc for audio communications

by Richard K. Dickey
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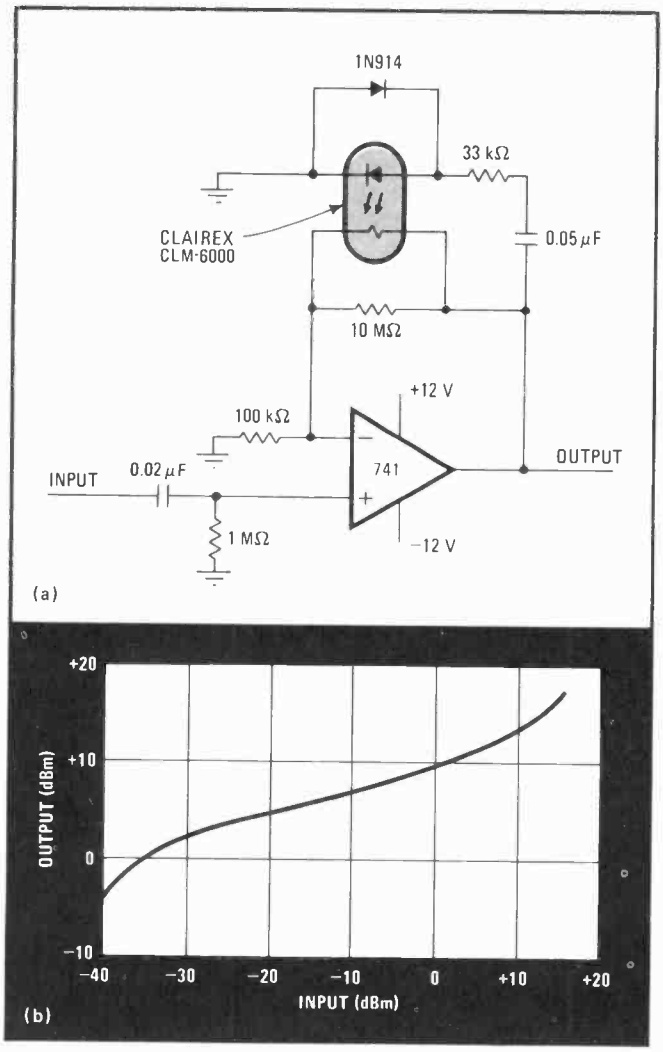
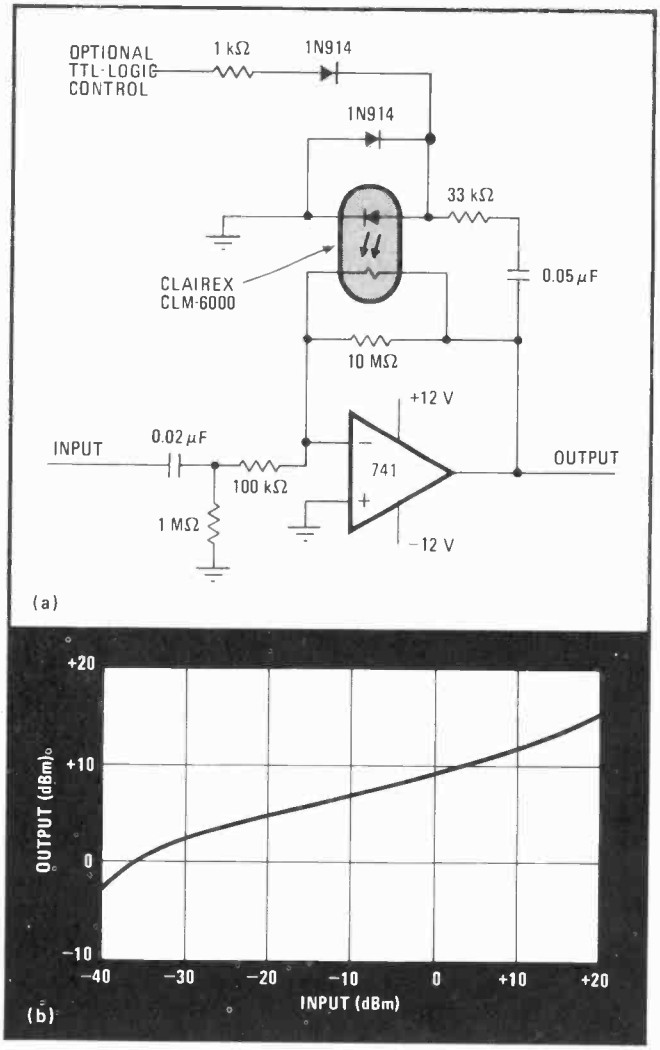
In all communications systems that have speech input, some form of automatic gain control is desirable to maintain the optimum signal level despite wide variations in the amplitude of the input level. To eliminate fluctuations caused by varying transmission efficiency, agc is also desirable at the receiving terminal.

A good agc system should introduce no amplitude or frequency distortion and should have a fast attack and a



1. Agc amplifier. Photoresistor in optical coupler provides feedback path for operational amplifier circuit in (a); output signal drives LED to reduce photoresistance and thus reduce gain. Transfer characteristics are shown in (b); 0 dBm is taken as 0.775 volt rms. The lower limitation on agc is shown by the curved portion of the characteristic at low input levels. Gain approaches unity at high input levels.



2. Wider range. Inverting connection of op amp (a) provides greater agc; transfer characteristics (b) show that 50-dB variation of input signal produces only 12.6-dB variation at output. The input impedance is less than for noninverting connection used in Fig. 1, and a constant low driving impedance is required. Optional portion of circuit shown in color allows a TTL signal to turn off output.

moderately slow decay. The circuit of Fig. 1(a), which has all these features, can reduce an input variation in excess of 50 decibels to an output variation of only 16 dB. This circuit uses a 741 operational amplifier connected in the noninverting mode. The gain of this configuration is $1 + R_F/10^5$, where R_F is the feedback resistance (in ohms). The feedback resistor is the photoresistor of a CLM-6000 optical coupler.

Unlike the more common phototransistor couplers, the CLM-6000 has a photoconductive cell; op-amp output voltage in excess of the forward drop of the coupler's light-emitting diode (about 1.4 V) decreases the photocell resistance. Therefore the 741 operates as a linear amplifier with a gain that is controlled by its own output. The characteristics of the photoresistor include a quick drop in resistance when illuminated and a slow recovery of resistance after darkness begins. The compression characteristics of the agc amplifier are shown in Fig. 1(b).

The 1N914 diode that shunts the LED completes the circuit for the negative phase of the ac signals, so that the 0.05-μF capacitor can discharge. The 10-megohm shunt across the photoresistor is necessary to prevent loss of dc feedback and consequent output saturation in the absence of signal. If output saturation were allowed to occur, the system would lock up, and no ac signal could appear at the output.

For a wider dynamic range, the inverting-mode operational amplifier circuit of Fig. 2(a) can be used; the input impedance is finite (100 kilohms), and a constant low driving impedance is required. For large input signals, the gain of this circuit goes below 1, so the circuit becomes an attenuator.

An additional feature of this configuration is that the output may be effectively switched off by a transistor-transistor-logic signal applied to the LED as shown. When the TTL signal is high, the LED emits so much light that the photoresistor conducts strongly and forces the gain to zero. When the TTL signal is low (less than 0.8 V), the circuit operates normally. □

Inductive proximity detector uses little power

by Matthew L. Fichtenbaum
General Radio Co., Concord, Mass.

A contactless limit switch and a tachometer pickup are two possible applications for the inductive proximity detector described here. This detector changes its output level from high (9 volts) to low (0 V) whenever a conducting object is close by. It uses less power than a photocell pickup and is immune to environmental dust and dirt.

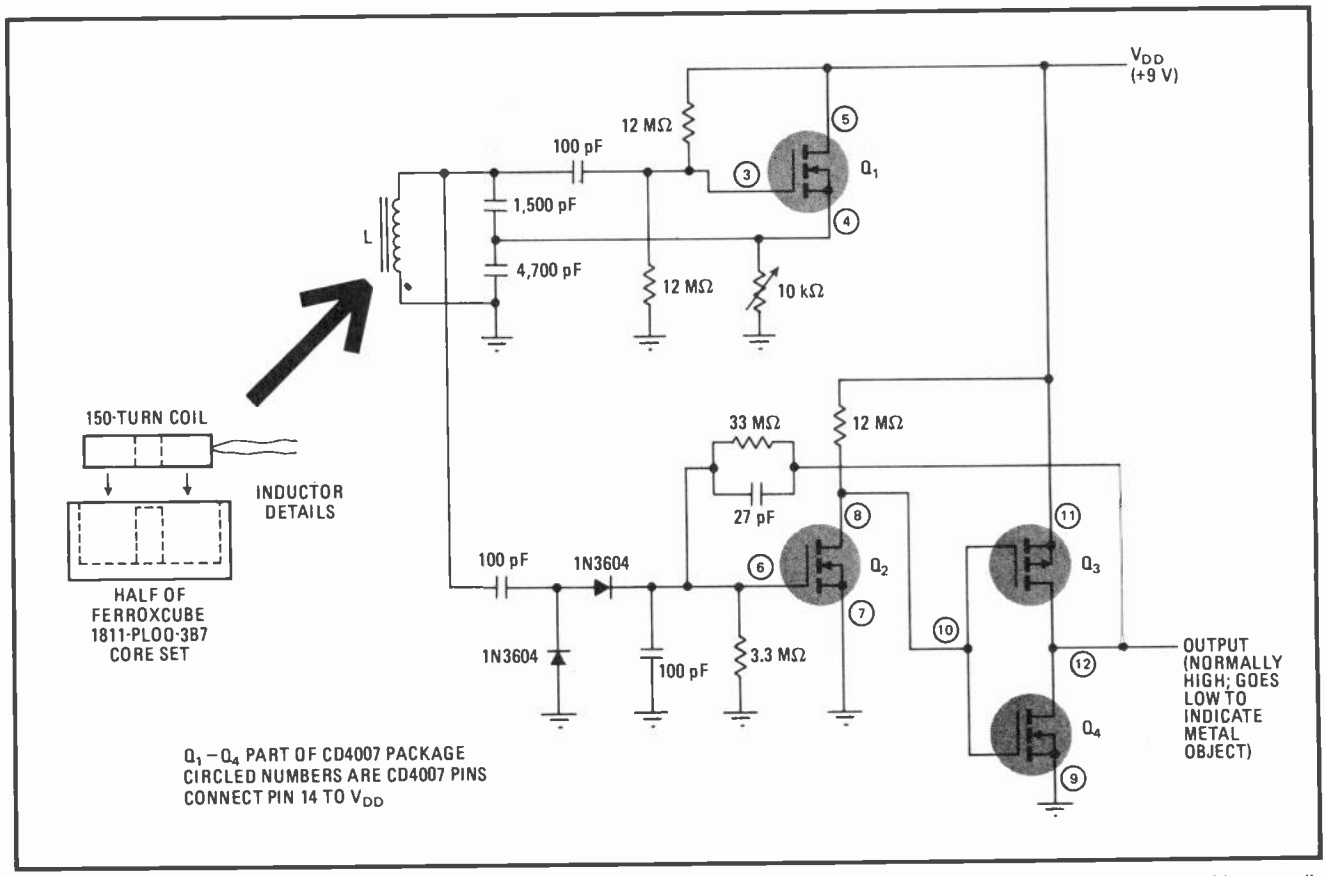
The sensing element is an unshielded high-Q inductor coil wound on a ferrite core. When a metallic object is brought close to the inductor, eddy currents that are induced in the metal absorb energy from the rf field of the coil and thus reduce its Q.

The active elements in the detector circuit are four of the C-MOS MOSFETs in a CD4007A package, and two 1N3604 diodes are included. FET Q_1 and its associated components, together with the inductor, constitute an oscillator that operates at about 100 kilohertz. The two diodes develop a dc voltage proportional to the peak-to-peak value of the oscillator signal. This voltage is applied to a Schmitt trigger composed of Q_2, Q_3, and Q_4 and holds this circuit in the "on" state.

A conductive object near the coil absorbs energy from the magnetic field of the coil, so that the oscillator amplitude drops. The rectified voltage therefore drops, and the Schmitt trigger turns off. The variable resistor adjusts the oscillator's operating level and hence its sensitivity to metal objects.

The inductor used in this circuit consists of 150 turns of #34 enameled wire inside half of a Ferroxcube 1811-PL00-3B7 pot core set, as shown in the figure. The inductance is approximately 2 millihenries. The circuit can detect the presence of metal objects at distances up to a centimeter from the open end of the coil.

This circuit draws about 250 microamperes at 9 V. It may be used to drive C-MOS logic directly or to drive a buffer that in turn drives TTL. □



Detects metal. Proximity detector consists of modified Colpitts oscillator, amplitude detector, and Schmitt trigger. Output signal is normally high; but when oscillator coil is loaded by presence of metal object, amplitude decreases and output from Schmitt trigger goes low. Detail drawing shows construction of the oscillator coil in a proximity detector that serves as the noncontacting pickup for a tachometer.

Low-distortion oscillator uses state-variable filter

by Walter G. Jung
Forest Hill, Md

The state-variable filter, which in any case excels as a flexible active-filter design block, can also be made to oscillate with only a little additional circuit complexity. With high-performance quad op amps now readily available, a single integrated circuit makes a ultra-low-distortion sine-wave oscillator with a output frequency of up to 5 kilohertz and three output phases for driving servo or instrumentation systems.

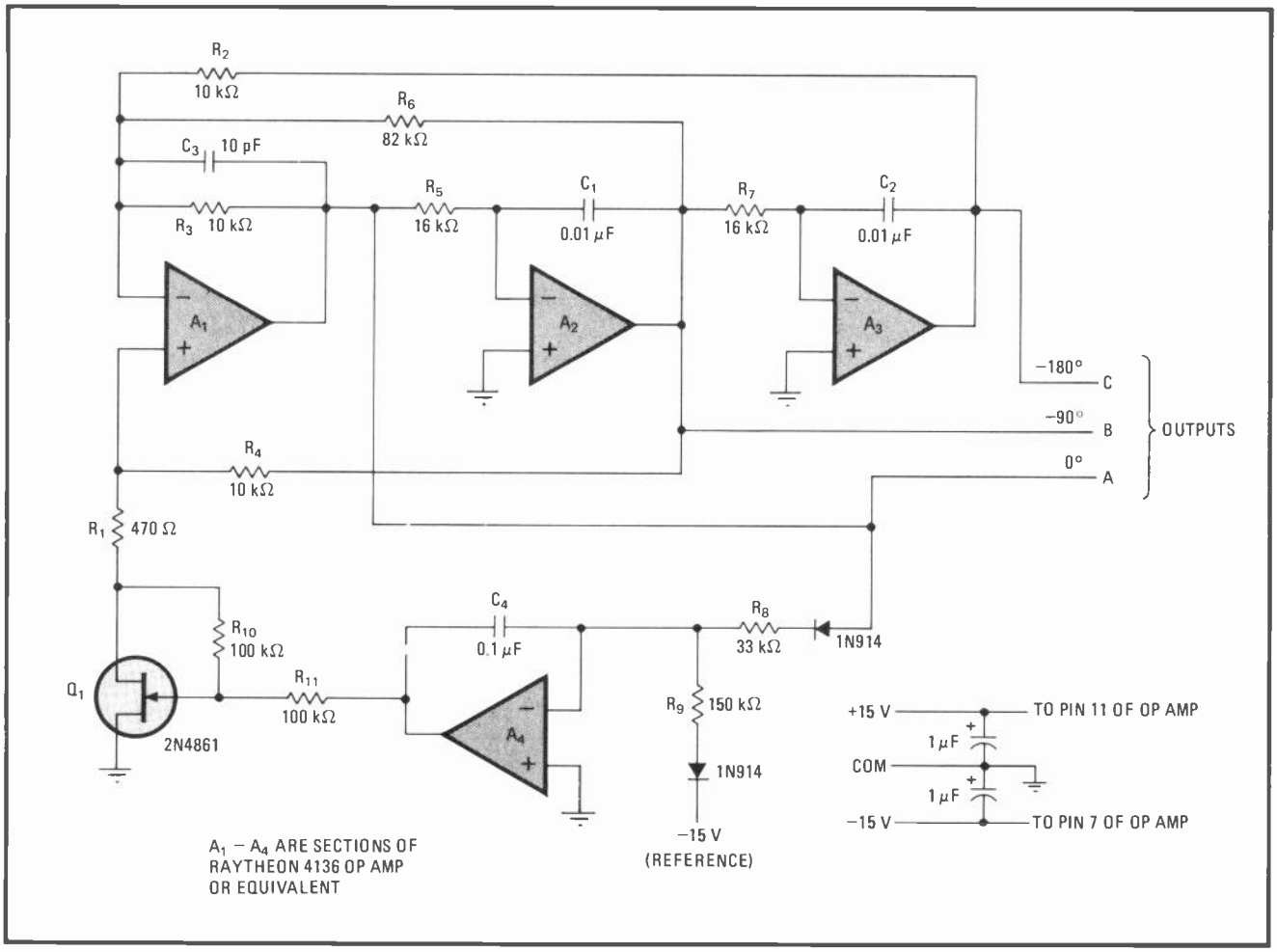
The schematic diagram shows the circuit of the oscillator. Operational amplifiers A_1, A_2, and A_3 comprise the state-variable filter, with its normal negative feedback path via R_4; positive feedback to sustain oscillation is provided by R_6. The oscillation frequency is given by:

$$f = \frac{1}{2\pi RC}$$

where R is the value of equal resistors R_5 and R_7 and C is the value of equal capacitors C_1 and C_2. For the circuit shown, f is 1 kilohertz.

As in other sine-wave oscillators, the positive and negative feedback paths must be carefully balanced to attain—and sustain—low-distortion operation. The balance is achieved by use of some type of automatic gain control; in this circuit the mechanism is the variable channel resistance of field-effect transistor Q_1.

The agc circuit in itself comprises an active loop that serves several important purposes. The integrator A_4 filters and smoothes the rectified output to provide a dc control voltage for the gate of Q_1. Low ripple on this control voltage is necessary to prevent modulation distortion on the output. The high dc gain of the integrator automatically adjusts the loop to the required dc bias for Q_1 in spite of parameter variations, thus eliminating



State-variable oscillator. Addition of regenerative feedback via R_6 changes state-variable filter into sine-wave oscillator with three phases of output. Filter uses three of the amplifiers in a quad op amp IC; the fourth amplifier is part of agc loop that ensures ultra-low distortion.

the necessity for device selection. The output voltage is regulated to a value that causes the average current in R_8 to be equal to that in R_9. Thus R_9 and the -15-V supply serve as a reference, and the agc loop tracks this reference to maintain the output peak voltage at about 10 V.

Resistors R_{10} and R_{11} provide a local feedback path around Q_1, to reduce distortion drastically below the straightforward connection. The high values of feedback resistance (100 kilohms) in relation to Q_1's "on" resistance (nominally 100 ohms) prevent undesirable interaction of the ac and dc signals.

In operation, the total harmonic distortion at the A output is on the order of 0.02%, and distortion in the B and C outputs is considerably less because of the low-pass filtering in the A_2 and A_3 integrator circuits. All outputs appear at the same level, with the phase relations shown.

The prototype of this circuit uses a Raytheon 4136 quad op amp, which has a 3-megahertz bandwidth. The Harris 4741, with similar ac characteristics, is another suitable unit. The Motorola 3403 and National 348, both 1-MHz devices, provide ultra-low-distortion performance at frequencies up to 2 kHz. The main asset of a quad device for this circuit is its cost-effectiveness—the entire circuit can be built for $10 or less. □

Two ICs make low-cost video-distribution amp

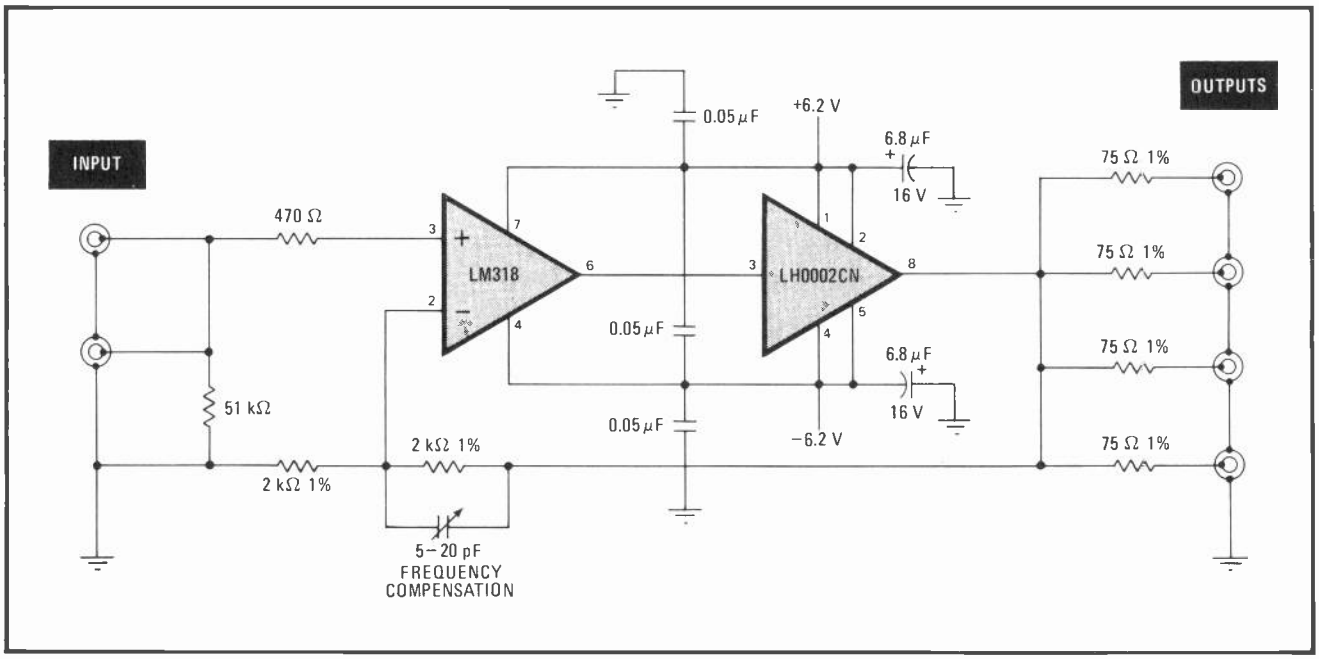
by M. J. Salvati
Sony Corp. of America, Long Island City, N Y.

For less than $25 in parts, a video distribution amplifier can be constructed with all the features of commercial models selling for over $300. The circuit shown in Fig. 1 takes the 1-volt peak-to-peak output of a standard video signal generator or TV camera and provides four or more independent outputs that each deliver 1-v pk-pk video into 75-ohm loads. Two input connectors are mounted in parallel because the 50-kilohm impedance is high enough to permit "loop-through" connection, in which a second distribution amplifier is paralleled with the first by means of the second connector. If not used for loop-through, the second connector should be terminated with 75 ohms. The frequency response of the unit is flat from dc to 4 megahertz.

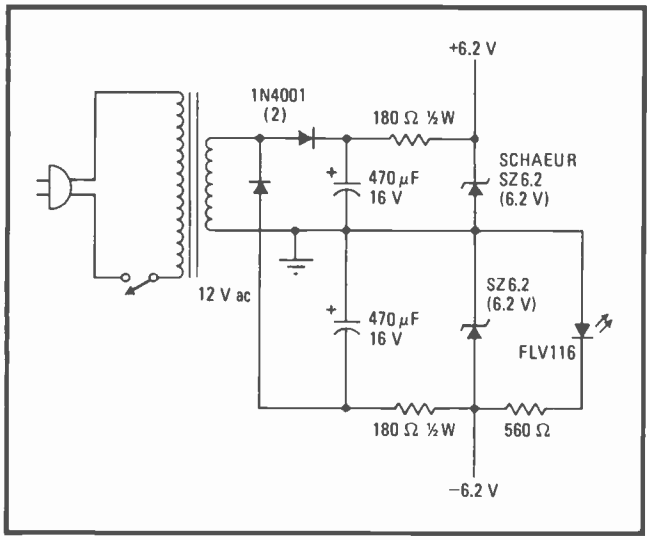
The video distribution amplifier circuit in Fig. 1 uses a National LM318 high-speed operational amplifier and a National LH0002CN current driver in a feedback loop. The resulting output impedance is so low that the output approximates a zero-impedance voltage source, so loads connected to the output resistors have no effect on each other. The 75-ohm output resistors provide the proper drive-source impedance for coaxial cable, short-circuit protection for the LH0002CN, and increased isolation between loads.

The only adjustment required is the frequency-response compensation capacitor. This trimmer is set to provide the same output amplitude with a 1-MHz sine-wave input as is obtained with a 10-kilohertz sine wave input.

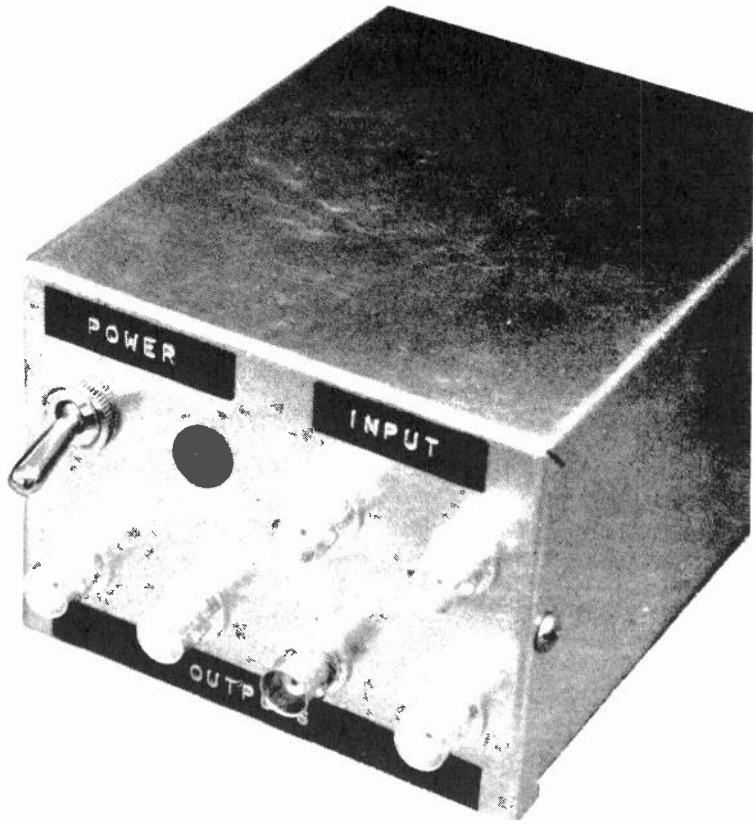
The 6.8-microfarad bypass capacitors should be tantalum electrolytics and should be installed close to the



1. Video distribution amplifier. Signal from TV camera or video signal generator is amplified to provide 1 v peak-to-peak at each of four outputs matched to 75-ohm loads. Second input connector can be used for "loop-through" connection of a second distribution amplifier or for a terminating resistor. Frequency-compensation adjustment balances stray capacitances, providing flat response from dc to 4 MHz.



2. Power supply. Compact supply uses zener-diode regulation to provide ±6.2 volts required for video distribution amplifier. This power supply and the amplifier shown in Fig. 1 are capable of driving more outputs than the four shown.



3. All packed up and ready to go. Amplifier-and-power-supply unit for 4-way distribution of video signals is packaged in metal box. Parts cost for complete assembly is less than $25.

LH0002CN pins. The 0.05-μF bypass capacitors should be disk ceramics installed as close to the LM318 pins as possible. The 75-ohm and 2-kilohm precision resistors must be noninductive types, such as metal film or carbon film.

The outstanding feature of this design is the low cost of the ICs implementing it. Although the slewing ability of the LM318 is insufficient to handle reliably a 2-V pk-pk output swing at 4 MHz, the amplitude of the highest-frequency component (color burst) in a standard composite video signal is only a small percentage of the overall amplitude, so the LM318 can easily handle a standard video signal.

The power supply recommended for use with this amplifier is shown in Fig. 2. Fig. 3 shows the complete video distribution amplifier and power supply unit packaged in a metal box. □

Four-bit a-d converter needs no clock

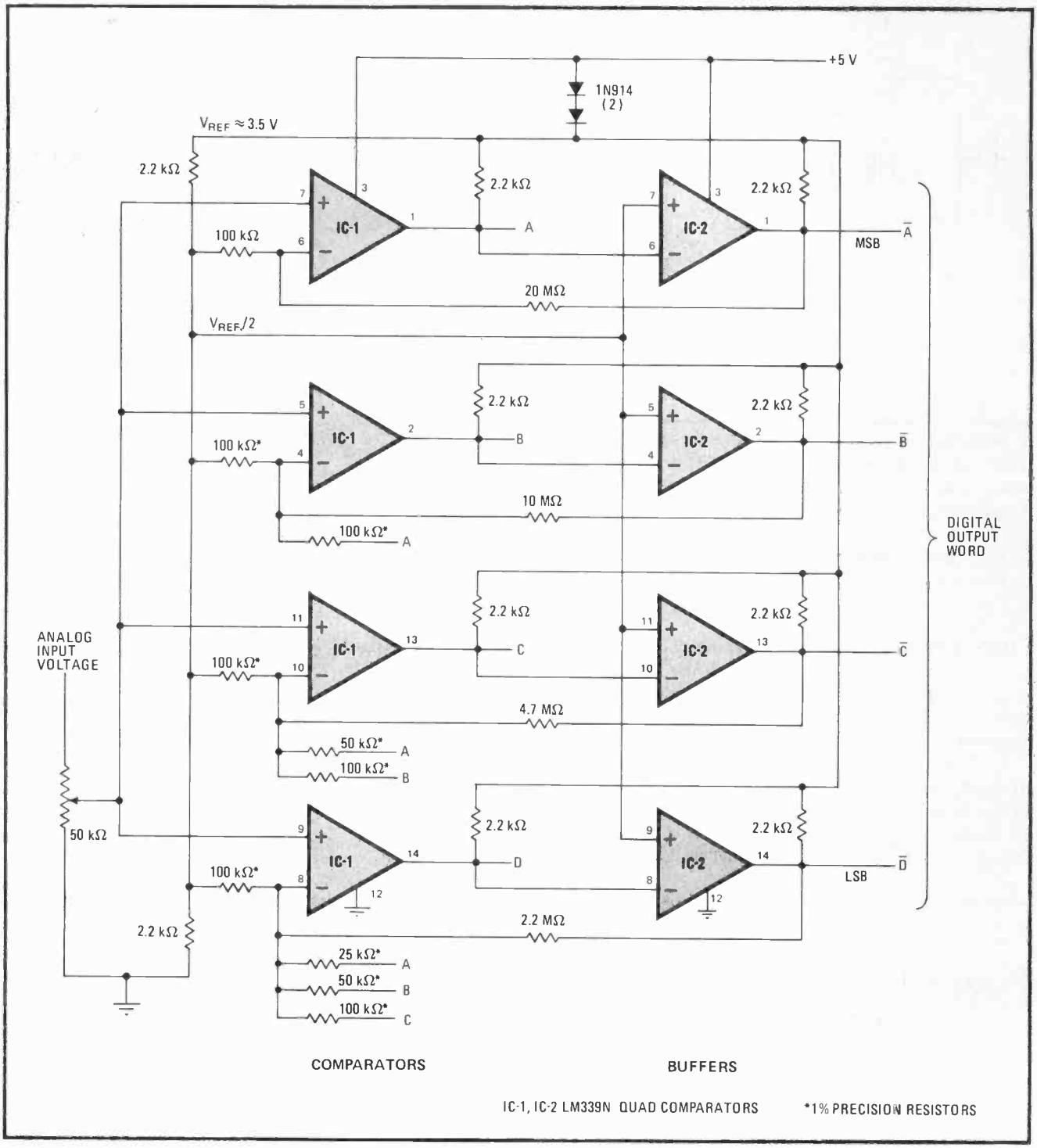
by Craig J. Hartley
Baylor College of Medicine, Houston, Texas

Many analog circuits utilize digitally controlled solid-state switches or multiplexers to adjust filter roll-off, amplifier gain, and the like; and in many such cases the adjustable parameter is itself a function of some analog voltage. As it happens, the 3-bit or 4-bit analog-to-digital converter required in such applications can be built from only three parts—a 5-volt supply and two quad comparators.

Other a-d converter designs generally include a counter, a clock, a d-a converter, a comparator, and other associated digital circuitry. In the design described here, however, the elements of one quad are used as comparators, while the elements in the other quad serve as buffers. The four outputs can drive TTL loads directly.

In operation the state of each output bit is determined in sequence, starting with the most significant bit. The reference voltage for each bit is determined by a resistor network at the inverting input of each comparator. The resistors are connected in a 1, ½, ¼ . . . sequence to ½ V_{ref} and the outputs of each of the more significant bits. The reference voltage for bit A (MSB) is always ½ V_{ref}. For bit B the reference voltage is ¼ V_{ref} if bit A (MSB) is low, or ¾ V_{ref} if bit A is high. The reference for bit C is ⅛, ⅜, ⅝, or ⅞ V_{ref}, depending on the states of bits A and B. The reference for bit D, the least significant bit, is 1/16, 3/16, . . . 15/16 V_{ref}. To eliminate unwanted output switching on input noise, hysteresis of about 0.02 volt is provided at each reference input by the 20-, 10-, 4.7-, and 2.2-megohm feedback resistors.

The full-scale input voltage is V_{ref}, which in this circuit is approximately 3.5 V. (The 50-kilohm potentiometer scales down higher input voltages.) The two diodes set V_{ref} at about 1.5 V below the 5-V supply to satisfy the maximum input conditions of the National LM339



Four-bit a-d converter. This conversion circuit uses negative feedback to match the digital output word to the analog input voltage one bit at a time. It distinguishes 16 voltage levels between 0 and 3.5 V. This converter does not require a clock, a d-a converter, or digital signals for operation, which makes it convenient for driving a digitally controlled switch in a system where all other elements are analog.

comparators and also to make the output voltage compatible with TTL. The output voltage is approximately 0.14 V (low) or 3.5 V (high). Because the comparator-buffer pairs are complementary (one is off while the other is on), the current through the diodes is nearly constant, making V_{ref} independent of the output states. Total supply current is about 8 milliamperes.

The digital outputs track the analog input with a worst-case acquisition time equal to the sum of the propagation delays of each comparator. This sum ranges from 1 microsecond up to 5 μs for the 339 comparator, depending on the rate of change of the input. A faster comparator would shorten the acquisition time significantly. Accuracy is controlled by the matching of the resistors indicated by an asterisk in the figure.

Compatibility with other logic forms can be achieved by adjusting the supply voltage, V_{ref}, and the load resistors on each comparator. □

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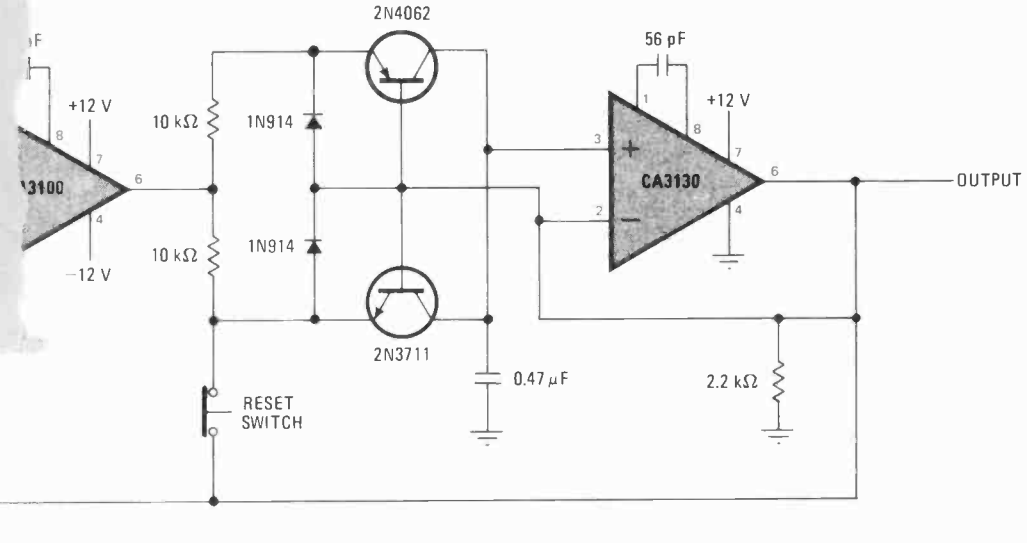
er uses a series diode for this
liode has a reverse leakage current that is unpredictable, temperature-dependent, and often on the order of several nanoamperes. To avoid this leakage, the circuit shown uses the base-collector junction of a pnp transistor to transfer charge. The current is injected into the emitter, with the base connected to the output of the buffer amplifier. As a result, the base-collector voltage is close to zero, and collector leakage current is small.

An npn transistor is added to allow the capacitor to be discharged. Normally, this transistor does not conduct because its base-emitter junction is shorted by the switch. Thus, when the switch is closed, the output voltage (which is equal to the voltage across the capacitor) is determined by the most positive level applied to the input terminal. When the switch is open, the output voltage tracks the input signal (Fig. 2).

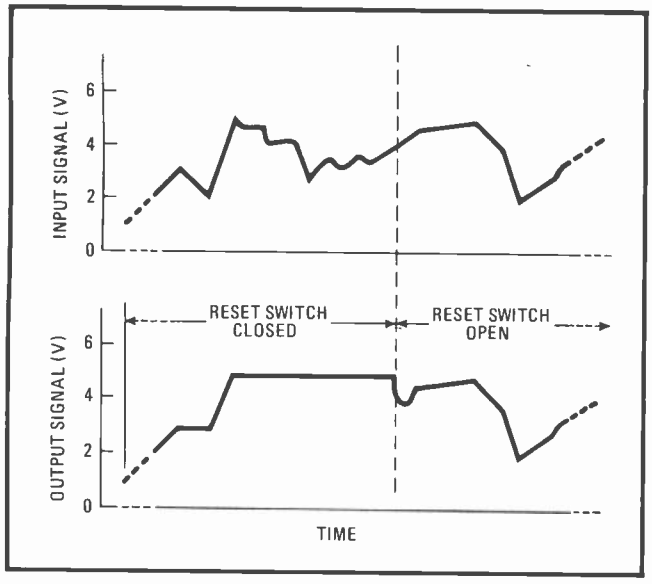
Holding performance of the circuit is quite good. If a 3-V signal is applied and removed, the output decays less than 10 millivolts in 10 minutes. This implies that the total leakage current into the capacitor is less than 10 picoamperes.

A drawback is the low slew rate. The minimum slew rate is set by the 10-kilohm resistors, the 0.47-μF capacitor, and the difference between the maximum output voltage of the CA3100 and the maximum signal voltage. With a 6-V input signal, the slew rate is about 850 V/s.

Several variations on the circuit are possible. The switch could be replaced by an electronically controlled device, such as a relay or a CD4016 complementary-metal-oxide-semiconductor transfer gate. This change



1. Stores maximum level. Peak detector circuit accepts analog input signals of 0 to 6 V in amplitude, provides output level that is maximum value of input. Use of pnp transistor for rectification minimizes charge leakage from capacitor, so peak level can be held for several minutes. Switch and npn transistor allow circuit to be reset. While reset switch is open, output signal follows input signal. If the reset switch is relocated to short the emitter to the base on the pnp transistor, the circuit is a minimum level detector, storing the lowest level of the input signal.



2. Holding the peak. Output from circuit of Fig. 1 is the highest level that has been applied to the input since switch was closed. If switch is opened, output slews down to input level, and then follows input. Circuit was developed for determining dynamic range of low-bandwidth scanning signal from an electron microscope, but is useful for any peak rectifier that requires low decay rate.

would allow electronic control of the reset function.

If the switch is moved to the emitter of the npn transistor, the circuit stores the lowest level of the input signal. If switches are placed in both locations, the circuit can function in four modes: tracking (both switches open), positive peak detector, minimum level detector, and holding (both switches closed).

By using both a positive peak detector and a minimum level detector in a circuit, maximum and minimum voltage levels can be stored for such purposes as setting the gains of variable-gain amplifiers, or storing the levels of transient peaks in a signal. □

Mark/space modulator drives acoustic coupler

by Jack D. Dennon
Computerphone Systems, Renton, Wash.

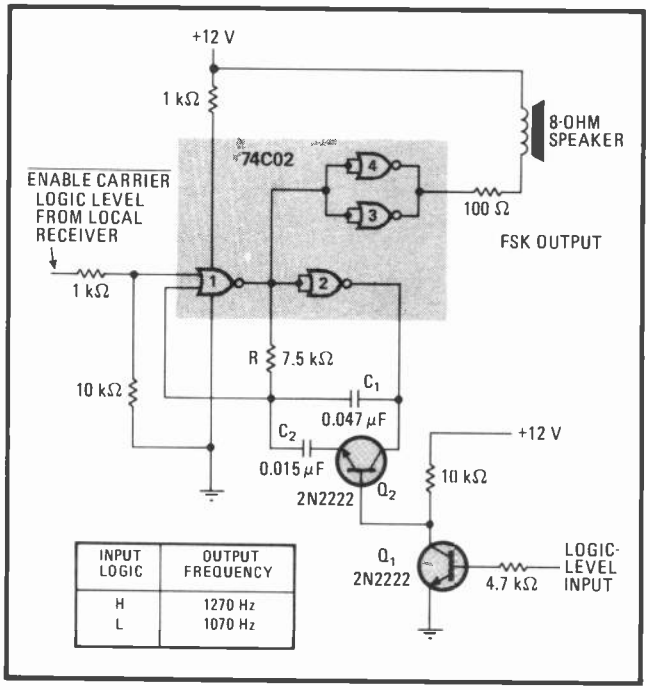
When data must be transmitted over a voice channel, the circuitry used to translate the logic lows and highs into audio-frequency signals usually includes frequency-trimming potentiometers. But precise enough mark and space audio signals can be obtained from a circuit that uses only standard resistor and capacitor values, provided the supply voltage is well-regulated.

The circuit shown translates serial logic-level data into audio-frequency analog frequency-shift-keyed signals for transmission by telephone, radio, or other voice channels. The modulation function, including provision for a logic-level data input and an active-low enable-carrier input, is implemented with a single complementary-MOS 74C02 quad NOR gate. The output buffer, which consists of gates 3 and 4 of the integrated circuit, has four n-channel transistors paralleled to ground for driving an 8-ohm speaker. The speaker provides acoustic coupling to a telephone handset.

Logic low at the data input turns off transistor Q_1 and turns on transistor Q_2. With Q_2 on, C_2 is switched into the circuit. The frequency of the audio oscillator, made from gates 1 and 2 of the integrated circuit, is proportional to $1/RC$ where $C = C_1 + C_2$. Switching C_2 into the circuit causes the output frequency to shift from K/RC_1 to $K/R(C_1+C_2)$ where K is a constant. With the component values shown, K/RC_1 = 1,269 hertz, and $K/R(C_1+C_2)$ = 1,052 Hz. These frequencies have been found to be sufficiently close to the specified 1,270-Hz mark frequency and 1,070-Hz space frequency for reliable transmission at a data rate of 110 bits per second to a Bell 103 dataset.

The circuit draws about 30 milliamperes from a regulated 12-volt supply. With appropriate changes in the values of components R, C_1, and C_2, supply voltages from 6 to 15 V can be used.

The enable-carrier input to the modulator is driven from a companion receiver circuit to complete the "handshake" sequence at the beginning of a data call; that is, the local receiver asserts the active-low enable



FSK modulator. C-MOS quad NOR gate is audio-signal generator and output driver/buffer for transmitting data over voice channel by frequency-shift-keyed audio signals. The logic-level enable-carrier input must be taken low for the modulator to operate; this input is driven by the local receiver and is used to properly sequence the initial exchange of signals called "handshaking." The enable carrier should be taken low about half a second after the dataset at the other end of the line answers the call with its 2,225-Hz marking tone.

carrier shortly after it first hears the 2,225-Hz marking tone coming from the dataset at the other end of the phone line.

Bell 103 line protocol calls for frequency-division-multiplexed simultaneous two-way transmission. The modem originating the call sends 1,270-Hz mark and 1,070-Hz space frequencies and receives 2,225-Hz mark and 2,025-Hz space frequencies from the answering dataset. At the beginning of the call, the answering dataset immediately places its 2,225-Hz mark signal on the line. On a long-distance call, this tone should be allowed to reside alone on the line for at least 400 milliseconds to disable any one-way-at-a-time devices (echo suppressors) on the telephone trunk lines. □

Common-gate, common-base circuits shift voltage levels

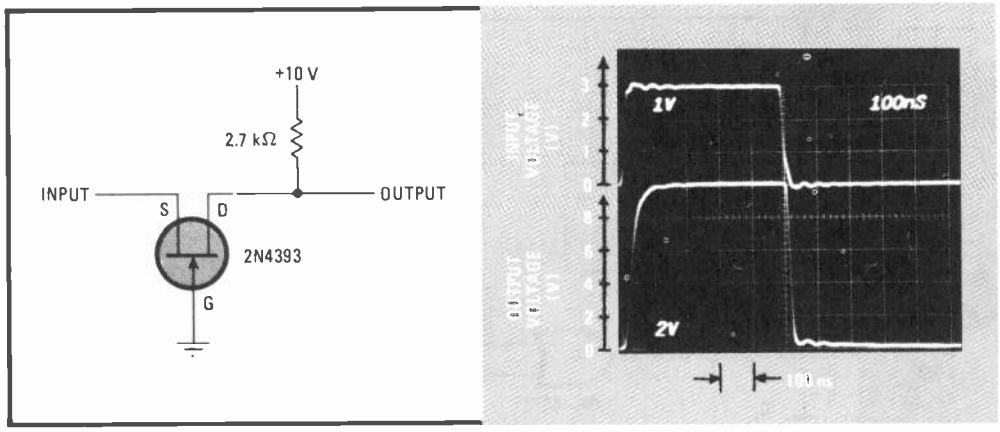
by Peter J. Bunge
Atomic Energy of Canada Ltd., Chalk River, Ontario

The voltage-shifting interface needed between incompatible logic systems can be quite straightforward—just a field-effect transistor in a common-gate circuit or a bipolar transistor in a common-base circuit. Both circuits are fast, uncomplicated, and economical in both parts cost and power drain.

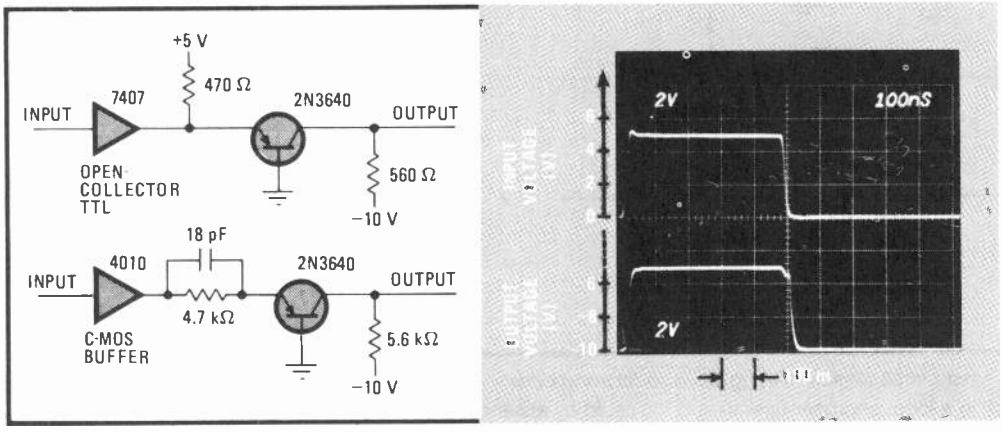
The common-gate FET circuit shown in Fig. 1 can couple the active outputs from any logic family to a voltage level higher than the V_{CC} of the logic—an impossibility with pullup resistor interfacing or complementary-metal-oxide-semiconductor buffer (4009, 4010) interfacing. It uses much less power than open-collector transistor-transistor-logic interfacing, especially when only one signal is involved, and it is much faster than some commercial level shifters (e.g. 100 nanoseconds versus 900 ns for the Solitron CM410AE). For the 2N4393 FET shown, the input range is 3 to 40 volts while the output range is 0 to 40 V (determined by the pinch-off and breakdown voltages of the device.)

The common-gate circuit provides only positive output voltages. A typical application is in interfacing an n-MOS random-access memory, which has 0-V and 3-V output levels, to C-MOS circuitry. Interfacing is necessary in this case because the 3-V level is just at the operating threshold of C-MOS when it is operating from a 5-V supply.

Common-base transistor circuits are used to interface positive voltage levels to negative-referenced logic. Figure 2 shows arrangements for translating 0-V or +5-V TTL or C-MOS levels to −10 V or −5 V. These methods are simple, require little power, and can be used with either active outputs or open-collector outputs, as shown. □



1. Level translator. A field-effect transistor in the common-gate configuration can provide output voltages that are higher than the supply voltage of the driving logic. Here the FET voltage-shifter accepts input levels of 0 or 3 V and delivers outputs of 0 or 10 V. The fast transitions and short delays that are demonstrated in the oscilloscope photo are achieved by minimizing the load capacitance.



2. Signal polarity inversion. Common-base level translator interfaces positive voltages to negative-referenced logic. Circuits here accept levels of 0 or 5 V and deliver outputs of −10 or −5 V. Waveforms shown are for circuit driven by open-collector TTL. Speed is sacrificed to conserve power in the circuit driven by a C-MOS buffer. The 18-pF speed-up capacitor charges input capacitance of transistor.

Dual-555-timer circuit restarts microprocessor

by James R. Bainter
Motorola Semiconductor Products, Phoenix, Ariz.

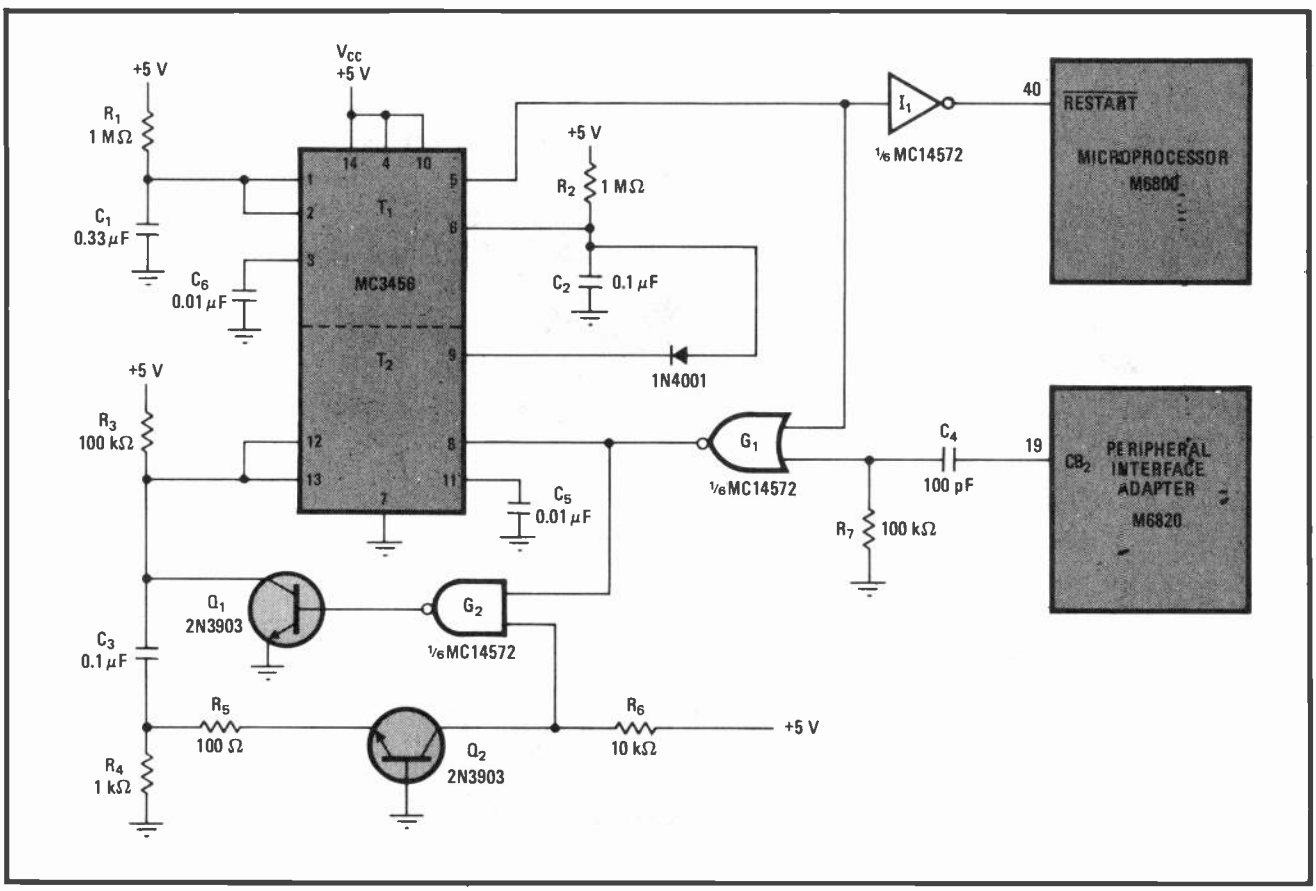
If noise on one of its bus lines garbles an instruction sequence, a microprocessor system will operate incorrectly—unless monitored by a timing circuit such as the one described here. When the circuit detects a garble, it generates a restart signal that causes the microprocessor to start its program all over again. The circuit also generates the power-on starting signal for the system.

Take the case of the M6800 microprocessor, which employs instructions composed of three 8-bit binary numbers, or bytes. The first byte is the operation code—describing the task to be accomplished—and the second and third bytes, if required, contain either data or address information. Now, suppose the hexadecimal number 20FE is to be loaded into the index register of the M6800. The instruction in machine code (hex representation) is CE,20,FE, and the three bytes reside in three consecutive memory locations. If noise from one of the data, address, or control buses were to make the processor skip the CE, the next byte, 20, would be interpreted as the operation code for "branch always," and then the byte FE would cause the processor to branch always on itself—in effect locking itself up in a loop with no exit.

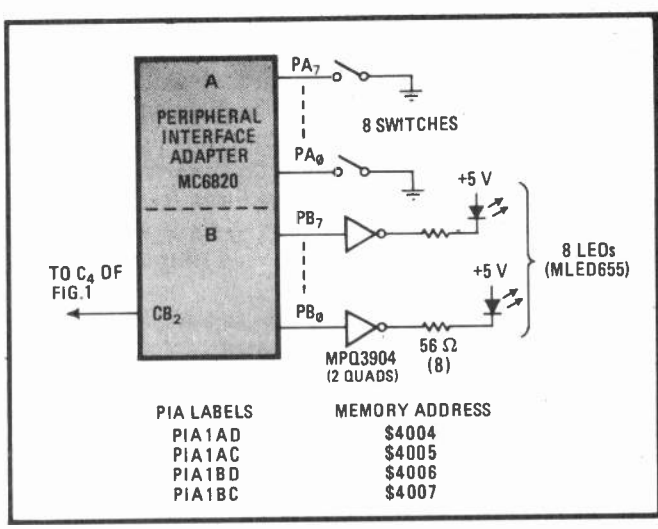
One way of restoring proper operation is to restart the system by pulling down the restart pin. In the case of the MC6800, this means driving pin 40 of its low-voltage condition—a job done by the circuit in Fig. 1.

The circuit is implemented with an MC3456 dual-555-type timer. Timing portion T_1 and timing networks R_1, C_1 and R_2, C_2 generate a 400-ms restart signal when power is applied. During normal program execution a signal lead applies a periodic pulse to T_2. In Fig. 1 this pulse comes from CB_2, the number 2 control lead from section B of a peripheral interface adapter. But if the processor goes off into never-never land or gets stuck in a loop with no exit, timer T_2 causes T_1 to generate a restart signal.

The circuit operates as follows Assume pin 5, the output of T_1, is in the logic 0 (low-level) state. The pulses



1. Generates a fresh start. Dual-timer circuit applies starting pulse to microprocessor and also restarts it if noise bursts or other troubles cause it to get off program or stuck in a loop. Improper operation is indicated by absence of timing pulse to T_2 from a adapter program.



TEST PROGRAM

Machine Code (HEX)			Assembly Listing		
CE	00	34		LDX #$0034	00→DDRA; $34→PIA1AC
FF	40	04		STX PIA1AD	
CE	FF	34		LDX #$FF34	$FF→DDRB; $34→PIA1BC
FF	40	06		STX PIA1BD	CB 2 LOW
FE	40	04	START	LDX PIA1AD	SWITCH DATA TO X(HIGH)
09			D1	DEX	
26	FD			BNE D1	X=0 ??
86	34			LDA A #$34	
C6	3C			LDA B #$3C	
F7	40	07		STA B PIA1BC	CB2 HIGH
B7	40	07		STA A PIA1BC	CB2 LOW
7C	40	06		INC PIA1BD	INC LEDS AT PIA1BD
20	EB			BRA START	GO TO START ALWAYS

2. Program listings. Automatic restart test program, stored in RAM, generates the pulse from the interface adapter. Switches connected to PA_7—PA_0 are read into the index register (X), which then decrements down to zero. Control lead CB_2 pulses, and then LEDs blink on in sequence if the microprocessor system is functioning properly. START follows four instructions programing interface adapter.

occurring on CB_2 will be coupled via capacitor C_4 to NOR gate G_1. Each pulse will appear inverted at the output of G_1, retriggering T_2 and discharging C_3 via transistor Q_1 and G_2. The transistor-gate combination of Q_2 and G_2 insures the discharge of C_3 is complete. The pulse is 5 microseconds long if the system clock frequency is 1 megahertz.

When the C_3 discharge current drops below 0.7 milliampere, Q_2 turns off, turning off Q_1 and allowing C_3 to recharge. If no input pulse arrives within 10 ms, C_3 will charge up to 0.67 V_{CC} level, and output pin 9 of T_2 will go low, discharging C_2. When C_2 discharges to 0.33 V_{CC}, T_1 output pin 5 will go high, generating a restart signal.

A high-level signal on pin 5 will also be presented to NOR gate G_1, causing T_2 pin 8 to go low. This resets T_2 pin 9 high, allowing C_2 to recharge. When C_2 recharges to 0.33 V_{CC}, C_1 will then recharge to 0.67 V_{CC}. T_1 output pin 5 will remain high until C_1 reaches the 0.67-V_{CC} level. Thus the restart (no pulse) signal will have a duration of R_1C_1 or 300 ms. This long restart signal is needed to turn on the power in a processor system that uses crystal-controlled clocks.

The test program in Fig. 2 is stored in the system's random-access memory. It generates the pulse on CB_2 and tests out the circuit shown in Fig. 1. It reads the switches at the A side of the interface adapter and places the switch data in the upper half of the index register, which it then decrements down to zero. Next, it stores a hex 30 in the B side control register, causing CB_2 to go high, followed by a hex 34, causing CB_2 to go low. The combination of these two instructions has thus caused a positive pulse on CB_2 that lasts for five machine cycles (5 μs for a 1-MHz clock).

The program then increments light-emitting diodes at the A side of the interface adapter, to give a visual indication of proper program execution. Then it branches back to where the switch data is loaded into the upper half of the index register.

As the higher-order switches are placed in the open (logic 1) position, the index register will be loaded with a larger number, and the program will take a longer time to decrement the index register down to zero. Thus the frequency of the pulses on CB_2 will be lower. With the values of R_3, C_3 in Fig. 1, timer T_2 will time out if a pulse does not occur on CB_2 at least once every 10 ms.

A real-life operating system would not use the test program of Fig. 2 to generate timing pulses to T_2. Instead the regular program residing in the system memory would include the two steps that drive CB_2 high and then low again. These would provide the pulse that indicates proper operation of the program; if the pulse failed to appear periodically, the T_1 timer would restart the program.

During system development, the output of T_2 pin 9 can be used to generate other signals, such as interrupts to print stack contents. This printout would be useful in pinpointing the cause of system problems. The signal could also be connected to a counter to record the number of system "hiccups" over a given time period. □

Timer IC stabilizes sawtooth generator

by Frank N. Cicchiello
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A temperature-independent audio-frequency sawtooth generator that uses a 555 integrated-circuit time is shown on page 109. Its sawtooth output maintains linearity within 1%, and its output is available from a low-impedance source that is fully buffered from the timing circuitry.

The circuit is superior to the more conventional approach that develops a linear sawtooth by adding a con-

stant-current pump to charge the sawtooth-forming capacitor. Since V_{BE} of the constant-current transistor changes with temperature in a conventional circuit, a corresponding change in its current would cause a variation in frequency of the output sawtooth. No such change occurs in this 555 circuit.

Connecting pin 2 to pin 6 (trigger and threshold inputs respectively) of the 555 causes it to trigger itself and free-run as an astable multivibrator. Consider the circuit action after the IC's internal discharge transistor (pin 7), having dumped the charge on the sawtooth-forming capacitor C_1 via R_3, has become an open circuit and allows C_1 to recharge.

C_1 begins to charge through R_1, R_2, and R_3 toward the supply voltage V_{CC}. For all practical purposes, the change in voltage at the junction of R_2 and R_3 is equal to that at the top side of C_1. This voltage change is applied to the base of a Darlington-type emitter follower, Q_1. Since Q_1 has virtually unity gain, it couples this same change in voltage back to the top side of R_2. As a result, the voltage across R_2 remains essentially constant during C_1's charging cycle and so produces the same effect (linear-ramping) as a constant-current source feeding C_1.

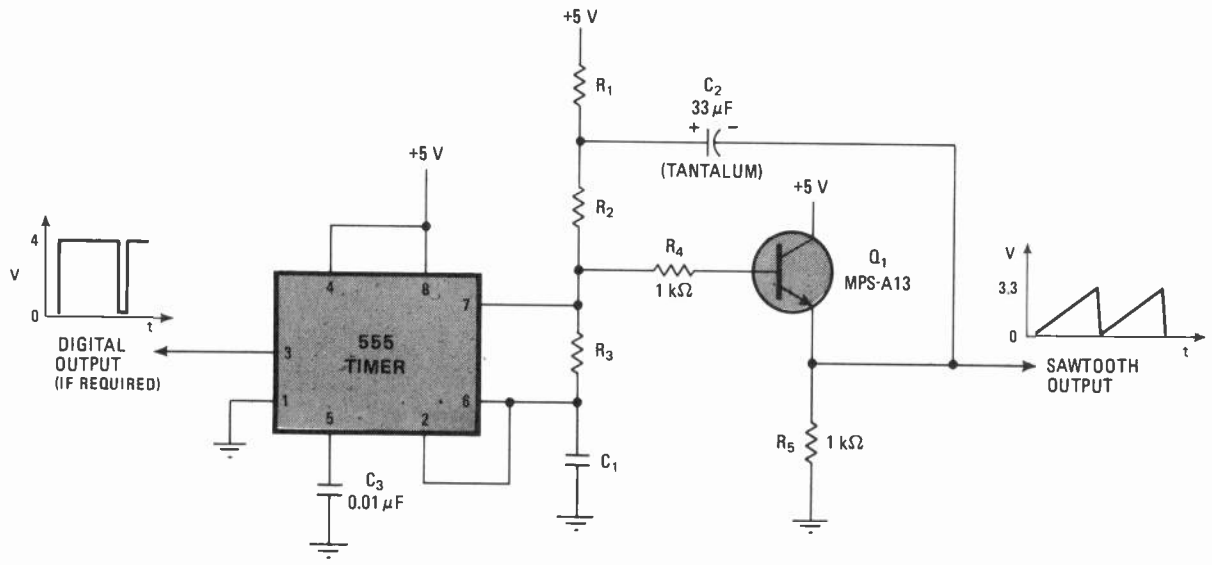
Once the linear sawtooth signal at pin 6 reaches a value of ⅔ V, the IC's internal comparator resets its flip-flops. The reset again activates the discharge transistor (pin 7), causing C_1 to dump through R_3; this action causes a new trigger wave to be applied to pin 2, thus repeating the circuit operational cycle.

Resistor R_3 is required to slow down the negative-discharge slope of the sawtooth wave form. Resistor R_4 is a parasite suppression resistor for Q_1. C_3 is a bypass capacitor on the voltage-control (pin 5) input of the IC, which is unused in this circuit.

The component and frequency relationships can be simply stated and easily implemented:

$R_1 = R_2$
R_2 *is equal to or greater than* $10\ R_5$
R_3C_1 *is equal to or greater than* 5×10^{-6} *s*
R_4 = *1 kilohm*
R_5 *is equal to or greater than 100 ohms*
R_1C_2 *is greater than* $10\ R_2C_1$
$f = 1/C_1[0.75(R_1 + R_2) + 0.693\ R_3]$

As in the conventional exponential sawtooth generator circuit, the output frequency is independent of variations in supply voltage. Typical performance data is shown in the table. □



FREQUENCY		R_3	R_1 & R_2	C_1
Computed	Measured			
54.2 kHz	50 kHz	5.1 kΩ	10 kΩ	1,000 pF
665 Hz	667 Hz	510 Ω	100 kΩ	0.01 μF
6.7 Hz	6.9 Hz	51 Ω	1 MΩ	0.1 μF

±5% TOLERANCE ON ALL COMPONENTS

Linear, buffered, and stable. Sawtooth voltage generator, developed for CRT sweep deflection, uses 555 astable multivibrator. Emitter-follower arrangement of the transistor maintains charging current to C_1 constant for linear ramps and provides buffered low-impedance output. Temperature-induced changes of V_{BE} do not affect frequency. Table shows typical frequency characteristics; supply voltage can be raised for greater output without changing frequency. In addition to the sawtooth wave form, a digital output is also available from 555 as shown; this signal may be useful for triggering a scope, for example, but it is not necessary for generating the sawtooth.

Active filter has stable notch, and response can be regulated

High Q of zeroes in transfer function is independent of component balance; notch depth depends on high gain, rather than precision of parts, and circuit-performance sensitivity to passive elements is low

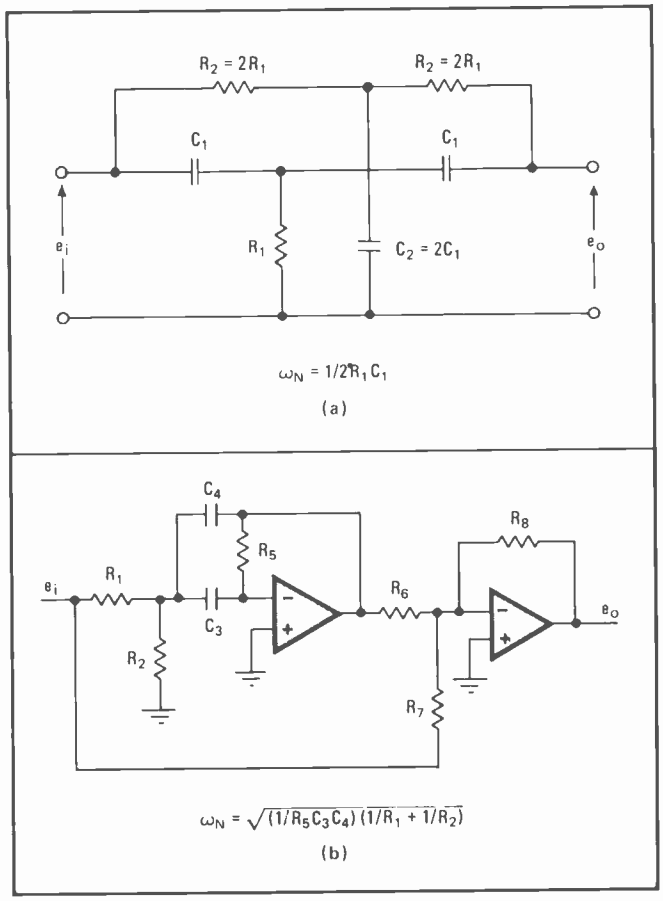
by James R. Bainter, *Motorola Semiconductor Products Inc , Phoenix, Ariz.*

☐ Many tone-signalling systems require elimination or rejection of a single frequency or a narrow range of frequencies. To produce this stop band, transfer functions with a notch response have been achieved by both active and passive networks. However, all the circuits that have been used in the past have required accurately matched component values to produce deep notches. Unfortunately, aging and temperature variations can affect the capacitances or resistances of carefully matched components differently, with the result that their match is degraded. Aging can thus reduce a rejection ratio of, say, 60 decibels to as little as 10 dB.

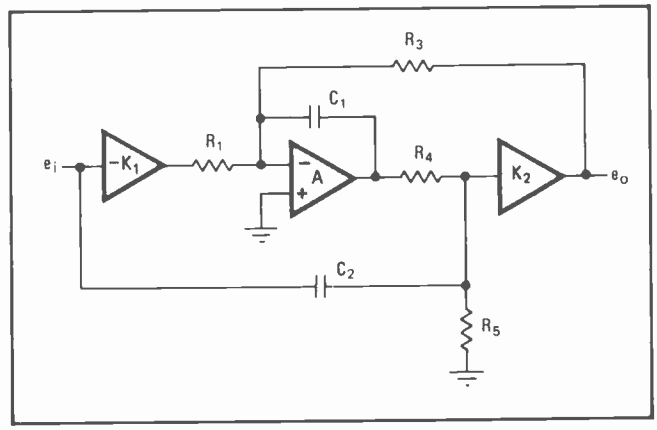
Now this need for perfect matching has been eliminated by an active filter in which the Q, or sharpness, of the null is a function of amplifier gain, rather than of precision balancing of passive components. The notch depth in the new network is constant so long as the gain remains high, even if resistors and capacitors drift. The active-filter network can also generate low-pass or high-pass filter blocks for frequencies above or below the rejection frequency. The passive component sensitivities of the network are 0.5 or less.

Considering null networks

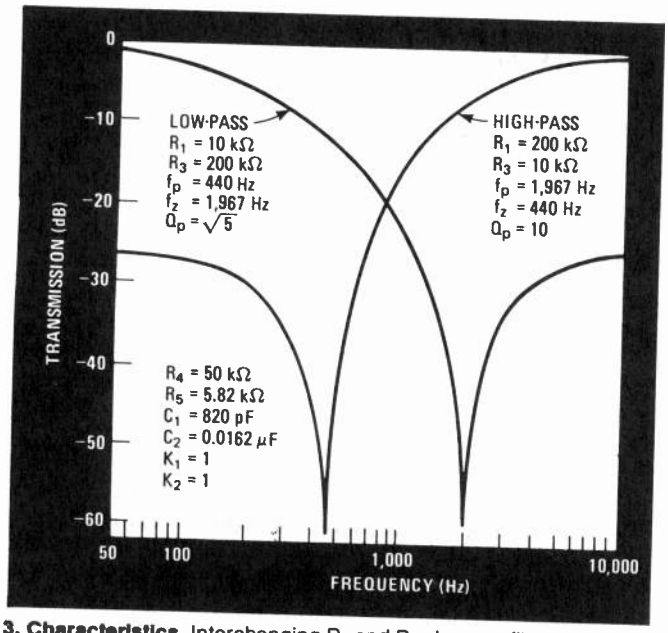
Among the passive bandstop networks that depend on the precision with which components are matched is the symmetrical parallel-T network shown in Fig. 1(a). One condition for balance is that the ratio of the series and shunt capacitors must be proportional to the ratio of the series and shunt resistors ($C_2/C_1 = 4R_1/R_2$). This balance, which is independent of frequency, implies that the depth of the notch at the rejection frequency depends solely on the accuracy of passive component matching. To get 60 dB of rejection at the notch frequency, the ratio of C_1 to C_2 must be held within 0.1% over the temperature range of interest.



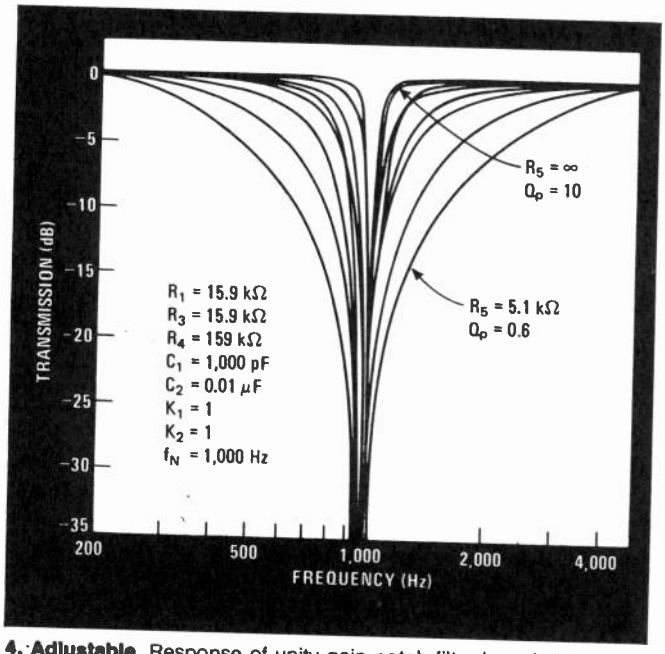
1. Null networks. Conventional notch filters may be passive circuits such as the bridged-T network in (a) or active circuits such as the subtractive arrangement in (b). In either type, the amount of signal rejection at the notch frequency depends upon ratios of passive components; therefore, component drift degrades performance.



2. Zero generation. New circuit can generate true zeroes at any frequency for which op amp has high gain. Notch depth is function of this gain alone, not of component ratios. Filter can combine low-pass or high-pass characteristics with notch. Pole and zero frequencies and pole Q-factor are independently adjustable.



3. Characteristics. Interchanging R_1 and R_3 changes filter response from low-pass to high-pass. If R_1 is equal to R_3, filter has symmetrical notch characteristic. Quality factor Q_p, which is measure of how fast the response returns from the notch to its passband characteristic, depends on values of resistances and capacitances.



4. Adjustable. Response of unity-gain notch filter is varied by varying R_5 to change Q_p value. Notch frequency is 1 kHz.

Other null networks have active circuits that subtract one signal from another to produce a notch at the desired rejection frequency. As an example, Fig. 1(b) shows a multiple-feedback bandpass active filter connected to a summing amplifier. At the node of R_6 and R_7, the input signal is subtracted from the output of the filter section. The final transfer function is

$$\frac{e_o}{e_i}(s) = -\frac{R_8}{R_7}\left[\frac{s^2 + s(1/C_3R_5 + 1/C_4R_5 - R_7/C_4R_1R_6) + \omega_N^2}{s^2 + s\omega_N/Q_p + \omega_N^2}\right]$$

where ω_N is 2π times the notch frequency, and Q_p determines notch width. To produce a deep notch with this circuit, the middle term in the numerator of the equation must be zero. That is,

$$R_5/R_1 = (R_6/R_7)(1 + C_4/C_3)$$

This expression shows that the amount of rejection at the notch frequency depends upon three ratios of passive components. Therefore, to maintain good notch depth, these ratios must be accurately set and maintained over the range of operating temperature.

Other bandpass filters, such as the state variable or biquad, may also be used; but they also require balancing of components, because the filter sections do not inherently generate transfer zeroes.

Generating transfer zeroes

The general form for the transfer function of an active filter is

$$\frac{e_o}{e_i}(s) = \frac{s^2 + (\omega_z/Q_z)s + \omega_z^2}{s^2 + (\omega_p/Q_p)s + \omega_p^2}$$

where ω_z and ω_p are the radian frequencies for the zeroes and poles, and Q_z and Q_p are the corresponding quality factors. For infinite Q_z, the coefficient of s in the numerator would be zero; this fact suggests that a circuit with a large gain factor in the denominator of this s-coefficient must have high Q_z. Such a circuit is shown in Fig. 2. The coefficient of s in the numerator of its transfer function is

$$\omega_z/Q_z = (1/R_1 + 1/R_3)/C_1(1 + A) \quad (1)$$

where ω_z^2 is the constant term in the numerator, $AK_1/R_1R_4C_1C_2(1+A)$. The value of Q_z is therefore given by the expression

$$Q_z = [K_1C_1A(A+1)/R_1R_4C_2]^{1/2}R_1R_3/(R_1 + R_3) \quad (2)$$

If the gain of the operational amplifier, A, is large (on the order of 10^4), Q_z is greater than 200. For such high values of A, the transfer function of the circuit in Fig. 2 is effectively

$$\frac{e_o}{e_i}(s) = K_2\frac{s^2 + [K_1/(R_1R_4C_1C_2)]}{s^2 + [s(R_4 + R_5)/(C_2R_4R_5)] + K_2/(R_3R_4C_1C_2)} \quad (3)$$

Since this equation has no s term in the numerator, the transmission function has a deep notch at the frequency given by

$$\omega_z^2 = \frac{K_1}{R_1R_4C_1C_2} \quad (4)$$

The notch frequency may shift if component values drift, but the depth of the notch will not be materially affected by such drift.

Calculating circuit performance

Equation (3) shows that the zero and pole frequencies, and Q_p, for the circuit in Fig. 2 are given by Eqs. (4) and

$$\omega_p^2 = \frac{K_2}{R_3R_4C_1C_2} \quad (5)$$

$$Q_p = \left[\frac{K_2C_2}{R_3R_4C_1}\right]^{1/2}\frac{R_4R_5}{R_4 + R_5} \quad (6)$$

$$\left[\frac{\omega_z}{\omega_p}\right]^2 = \frac{K_1}{K_2}\frac{R_3}{R_1} \tag{7}$$

The gain of the circuit in Fig. 2 at zero frequency is

$$\frac{e_o}{e_i} = \frac{K_1 R_3}{R_1} \tag{8}$$

and at infinite frequency is

$$\frac{e_o}{e_i} = K_2 \tag{9}$$

Thus, K_1, K_2 and R_3/R_1 can be used to set the transfer gain below and above the zero frequency ω_z.

Equations (7), (8), and (9) show how to select component values so that the circuit will function as a low-pass, high-pass, or notch filter: if $K_1 = K_2 = 1$,

- R_3 greater than R_1 gives a low-pass filter
- R_3 equal to R_1 gives a notch filter
- R_3 less than R_1 gives a high-pass filter

Figure 3 shows the result of interchanging R_1 and R_3 to convert the filter section from low-pass to high-pass.

Resistor R_5 can be used to adjust Q_p without affecting the zero or pole frequencies; in fact, the circuit can be designed without R_5. If R_5 is omitted, Q_p is

$$Q_p\Big|_{R_5=\infty} = \left[\frac{K_2 R_4 C_2}{R_3 C_1}\right]^{1/2} \tag{10}$$

Resistor R_5 can then be added to lower the total Q_p if the application requires that the Q_p be adjustable; to get a given value of Q_p, R_5 should be

$$R_5 = \frac{1}{(1/Q_p)(K_2C_2/R_3R_4C_1)^{1/2} - 1/R_4} \tag{11}$$

When R_5 is included in the circuit its value should be of similar to that of R_4; otherwise, the output of the op amp may saturate at the notch frequency. It is good practice to let $R_5 = R_4$ when using R_5 in the design. This value of R_5 results in low sensitivity of Q_p to R_4, as shown below.

The source that drives one of these filter sections should have a low resistance. The source resistance has no effect on the notch frequency, but it does affect the overall gain, ω_p, and Q_p.

The equations defining the component values may be further simplified for notch filters, in which $R_1 = R_3$ and therefore $\omega_z = \omega_p = \omega_N$, where $\omega_N^2 = 1/R_1R_4C_1C_2$ is the square of the notch frequency. Two sets of notch-filter equations that are useful to the designers are given in Table 1. One set of equations applies for the case where R_4 is equal to R_5, and the other set applies when R_5 is infinite; $K_1 = K_2 = 1$ is assumed throughout.

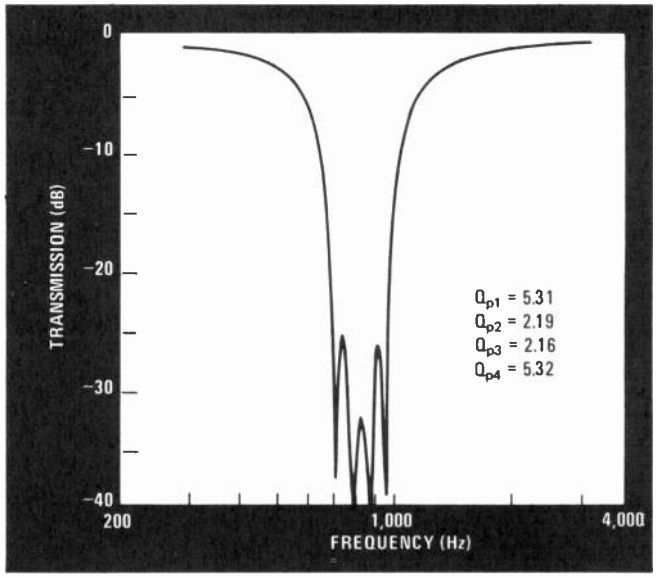
Comparison of Eqs. 14 and 17 shows that the component value spread is reduced by a factor of four if R_5 is set to infinity; but the flexibility in adjusting Q_p is lost.

To design a filter for a given ω_N, an appropriate Q_p is chosen, and C_1 is made equal to C_2 at some fraction-of-a-microfarad value that yields convenient resistor sizes.

Figure 4 shows the response of a unity-gain notch section where f_N is 1,000 Hz and Q_p is varied over the range from 0.6 to 10 by varying R_5.

In applications where it is required to notch out a significant bandwidth, as in the band-rejection filter for a Touch-Tone telephone receiver, individual notch sections can be cascaded. Figure 5 shows the response of four cascaded notch sections for such an application; the notch frequencies are 697, 770, 862, and 941 Hz. The frequencies from 700 to 1,000 Hz are rejected by 25 dB. And since resistor R_4 is common to both ω_z and ω_p, the notch frequency is adjusted by trimming R_4.

The sensitivities of the singularities and of Q_p to fractional changes of passive-component values are shown in Table 2. For $R_5 = R_4$ or for R_5 equal infinity, all sensitivities are ½ or less, resulting in active filter sections that are stable with respect to component drift. □



5. Stopband. Four cascaded notch sections with different rejection frequencies and different Q_p values produce a bandstop filter.

TABLE 1
NOTCH-FILTER EQUATIONS
(FOR $K_1 = K_2 = 1$)

FOR $R_4 = R_5$		FOR $R_5 = \infty$	
$R_1 = R_3 = \frac{1}{2\omega_N Q_p C_1}$	(12)	$R_1 = R_3 = \frac{1}{\omega_N Q_p C_1}$	(15)
$R_4 = R_5 = \frac{2Q_p}{\omega_N C_2}$	(13)	$R_4 = \frac{Q_p}{\omega_N C_2}$	(16)
$\frac{C_2}{C_1} = 4Q_p^2 \frac{R_1}{R_4}$	(14)	$\frac{C_2}{C_1} = Q_p^2 \frac{R_1}{R_4}$	(17)

TABLE 2
COMPONENT SENSITIVITIES (FOR CIRCUIT OF FIG. 2)

	R_1	R_3	R_4	R_5	C_1	C_2	K_1	K_2
ω_z	-1/2		-1/2		-1/2	-1/2	1/2	
ω_p		-1/2	-1/2		-1/2	-1/2		1/2
Q_p $R_5 < \infty$		-1/2	$\frac{1 - R_4/R_5}{2(1 + R_5/R_4)}$	$\frac{1}{1 + R_5/R_4}$	-1/2	1/2		1/2
Q_p $R_5 = \infty$		-1/2	1/2		-1/2	1/2		1/2