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Circuit Designer's Casebook

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By ROBERT G. HIBBERD, *Semiconductor-Components Division, Texas Instruments Incorporated*

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This unique work presents the principles of semiconductors in an unusual way. It starts with a description of semiconductors and their properties, the p-n junction and the junction transistors, and the characteristics of transistors and basic transistor amplifier circuits. It then describes the manufacture of transistors and other semiconductor materials and devices. The book also discusses the whole family of semiconductor devices and examines the applications of integrated circuits. Down to earth in presentation, it can be used by non-technical readers to obtain a working familiarity with the subject.

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This all-inclusive reference work offers you today's latest and most dependable source of guidance on thin film theory and practice. The volume serves both as an introduction to the field and a practical day-to-day guide for scientists engaged in thin film work. Profusely illustrated, it gives you easy access to all information you need, helping you to catch up with the fast-moving field. Each of the 23 detailed sections has been written by a recognized authority who covers the subject areas he knows best. Divided into four sections: Preparation of Thin Films, The Nature of Thin Films, Properties of Thin Films, and Applications of Thin Films (this latter section with particular emphasis on thin films in the electronics industry).

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Table of Contents

COMPUTER-AIDED DESIGN

Foreword

Ask any electronics engineer if he could use another filter to work with and, after mentally ticking off such types as constant-k, m-derived, Chebyshev, Butterworth, active, L-C, and a host of others, he'd probably say: "Thanks, but no thanks. I have enough problems building the ones I know about." But there is another kind of filter every engineer needs desperately — an information filter.

Probably no one works closer to ground zero in the information explosion than the electronics engineer. How can he recognize and save the published material that's of lasting value, but only note and then discard the current news information that has a built-in obsolescence factor? Making these evaluations under the real-time pressures of completing a design project isn't easy.

Books like this one, we feel, will help him assemble a readily accessible storehouse of design information with a long shelf life. In this case, we have done the filtering.

This book is a collection of recently published basic, how-to articles from the technical article section of Electronics, combined with brief circuit ideas from the Designer's Casebook section. It can be used both as an up-to-date practical design textbook and as an idea book.

The editors of Electronics

Nomograph determines aperture time error

by Stephen Muth
ILC Data Device Corp., Hicksville, N.Y.

A simple nomograph does away with the tedium of calculating the error due to aperture time for a sample-and-hold circuit. It can also be used to compute the conversion error of an analog-to-digital converter which has a varying dc signal or a low-frequency ac signal as its input.

Being a measure of the repeatability of the analog sampling switch characteristic, aperture time reflects the uncertainty of when exactly the switch opens. Errors due to it vary with the signal rate of change at the sample point. The voltage that is sampled and held can have an error of:

$E = (dv/dt)T$

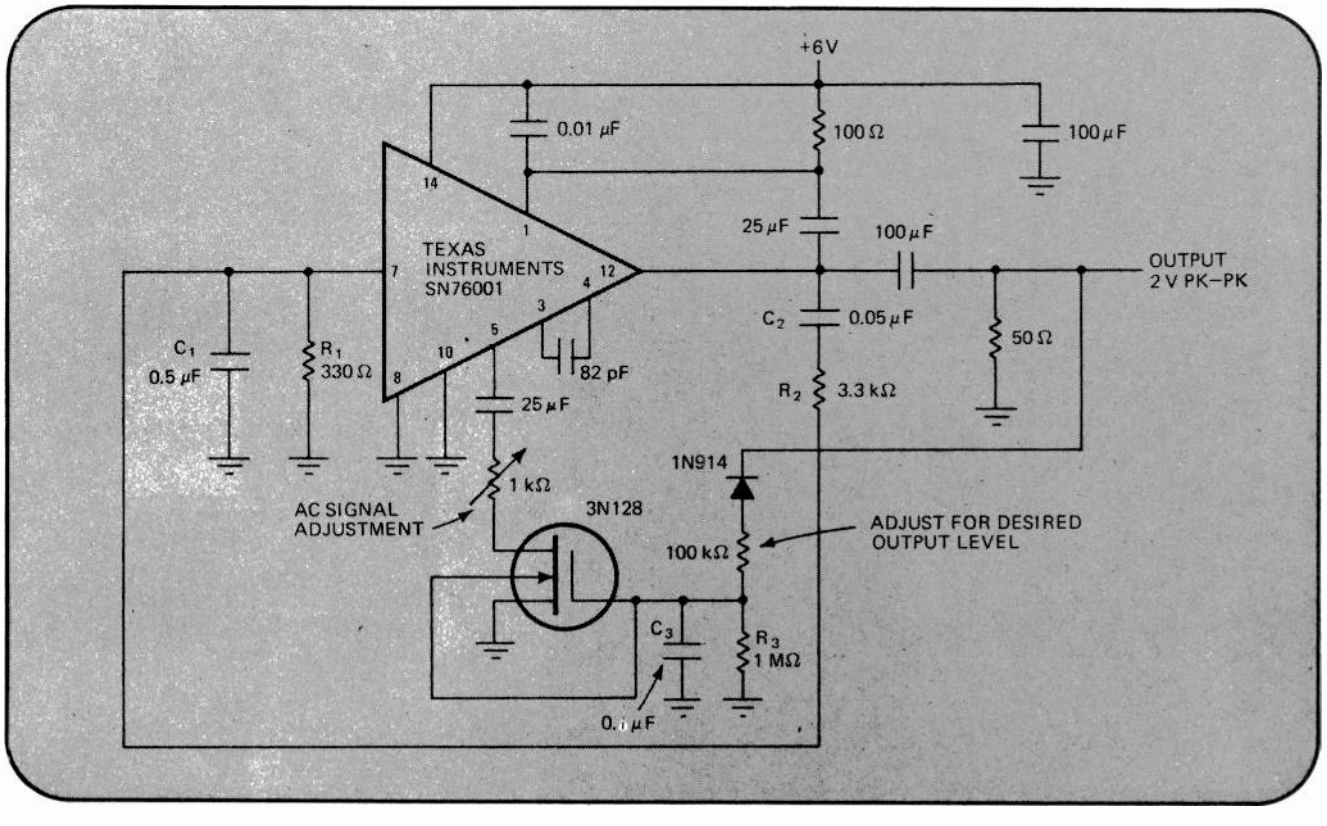
where E is the voltage change or error, dv/dt the maximum signal rate of change, and T the aperture time.

The nomograph shown is based on this relationship, and assumes a full-scale input voltage swing at the frequency of interest. If the signal is less than full scale, the error will be smaller. When the only limit on the input signal rate of change is slew rate limiting, dv/dt is easily computed and the nomograph is not necessary.

As an example, suppose the maximum allowable error for aperture time is 0.5% and the upper frequency limit is 2.6 megahertz. Use a straight-edge to intersect the frequency axis on the bottom and the error axis in the center. Maximum permissible aperture time is read from the top axis—300 picoseconds. (The present limit for aperture time in high-accuracy—0.1% linearity—sample-and-hold modules is about 100 ps.)

To find the error of an a/d converter with a conversion time of 22 microseconds and a dc input varying at 20 hertz maximum, treat conversion time as aperture time and signal rate variation as frequency. Use of straight-edge and nomograph shows the maximum error to be 0.3%. It should be noted that the error of the a/d converter can be reduced by two orders of magnitude by employing a sample-and-hold module to keep the converter's input constant for its full 22-μs conversion time.

Computation aid. Nomograph solves equation for percent-of-full-scale error due to aperture time of sample-and-hold circuit. Error, E, can be written in terms of signal rate, dv/dt, and aperture time, T: $E = (dv/dt)T$. Using straight-edge to intersect all three axes gives the answer. (Signal rate is represented by frequency axis.) Conversion error of a/d convertor can also be found by using the same technique.



SCR reset for integrator provides high speed

by Marshall W. Williams
University of Georgia, Athens, Ga.

A fast-switching three-gate reset circuit allows steady or varying dc voltage to be converted into TTL-compatible pulses for driving counters or other data storage or data processing devices. The circuit, actually a digitizing integrator, performs short-term integration on the input voltage. Each time an SCR conducts, the integrator section is reset, and a pulse output is obtained.

Because of its fast reset action, the circuit exhibits good linearity and accuracy. An output pulse rate of 10,000 counts per second injects an error of only 1%, which decreases to 0.001% at 10 counts per second (corresponding to a 25-millivolt input to the integrator.) Error, in this case, refers to the deviation from linearity of input voltage versus output frequency.

To avoid elaborate isolation circuitry, the SCR's cathode is connected to the integrator's summing point, permitting the integrator to accept only negative voltages. Positive voltages can be accommodated by preceding the integrator with an inverter stage.

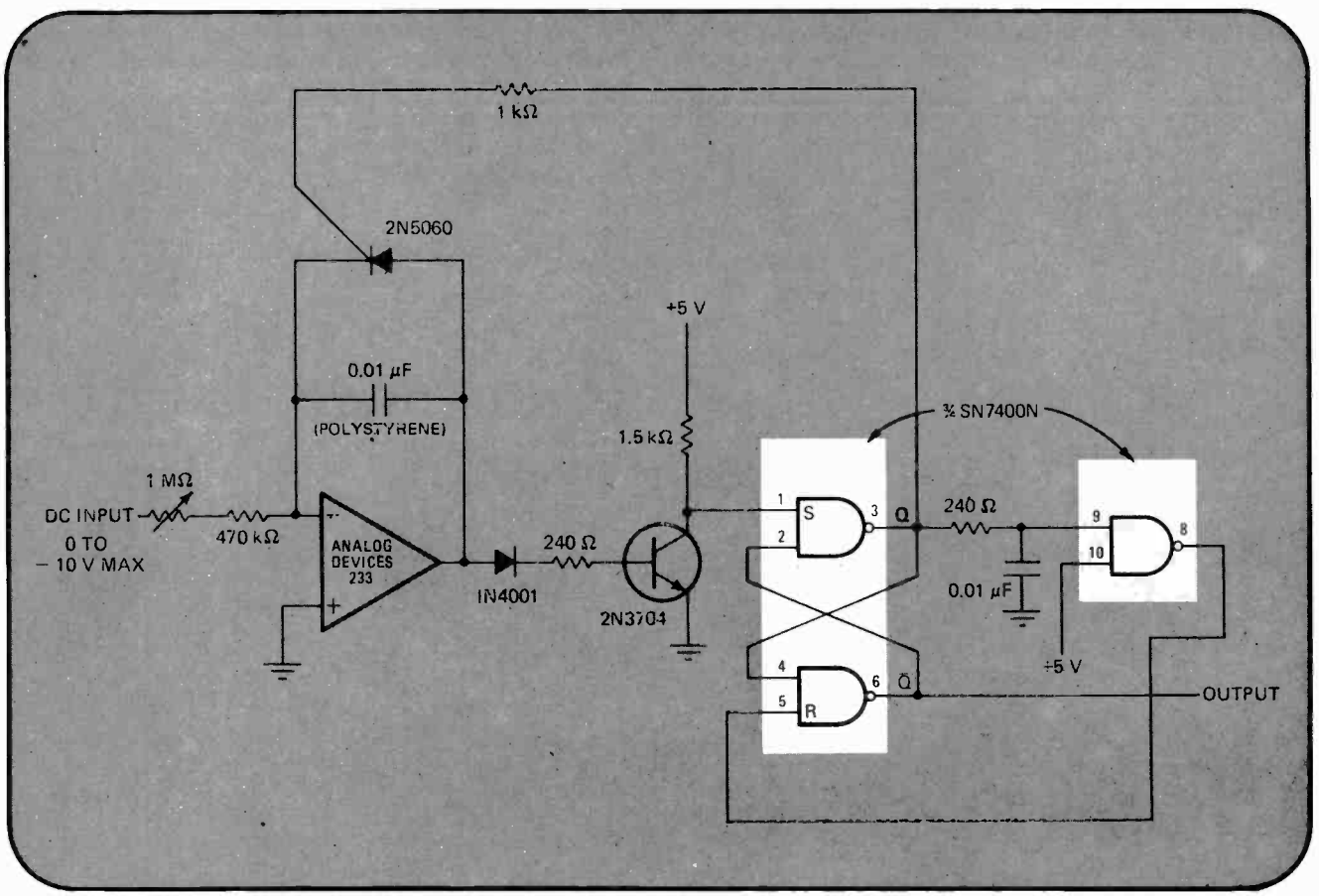
The reset circuit consists of cross-coupled NAND gates that form an R-S flip-flop and another NAND gate, connected in a 1-microsecond-delay inverter configuration, that keeps the flip-flop's Q output normally low. The integrator output is fed through a forward-biased diode to the base of a transistor, allowing the transistor to turn on only when the integrator output reaches approximately 1.4 volts.

When the transistor conducts, its collector goes low, applying a negative-going transition to the flip-flop's S input. The Q output of the flip-flop now goes high, turning on the SCR gate and producing a negative-going TTL-compatible pulse at the flip-flop's $\bar{Q}$ output.

As the Q output goes high, a delayed positive pulse is fed to the inverter gate, causing its output to go to logic 0 and resetting the flip-flop. The integrating capacitor is discharged to approximately 0.7 V (the turn-off voltage of the SCR) to initiate the next integration period.

With the input resistor values shown, integrator reset rate may be adjusted to around 0.25 millisecond when −10 V is applied to the input; lower input voltages give proportionately longer integration periods. A chopper-type operational amplifier is indicated in the diagram, but almost any op amp will work if larger drift errors can be tolerated.

Digitizing integrator. Dc input voltage is integrated and converted into TTL-compatible pulses by reset circuit that switches SCR to discharge integrating capacitor. When integrator output turns on transistor, Q output of flip-flop (cross-coupled gates) goes high, switching on SCR. Logic output pulse at flip-flop's $\bar{Q}$ output is terminated when inverter gate resets flip-flop and SCR turns off.



MOSFET network minimizes audio oscillator distortion

by Glen Coers
Texas Instruments Incorporated, Dallas, Texas

Because a MOSFET feedback control keeps the output level constant and prevents limiting, a low-distortion audio oscillator can deliver several volts into a 50-ohm load. The circuit uses a 1-watt audio amplifier as both an oscillating element and a power amplifier, and provides a total harmonic distortion of less than 1%. Moreover, it operates from a single supply, and holds output level change below 0.2 decibels if the supply voltage changes by 6 volts.

The oscillator circuit is a Wien-bridge type, in which resistors R_1 and R_2, and capacitors C_1 and C_2 function as frequency determining elements. First, R_1 is chosen between 100 ohms and 1 kilohm. Then $C_1 = \frac{1}{2\pi f_o R_1}$, where f_o is circuit resonant frequency. The values of R_2 and C_2 are directly proportional to R_1 and C_1, respectively: $R_2 = 10R_1$ and $C_2 = C_1/10$.

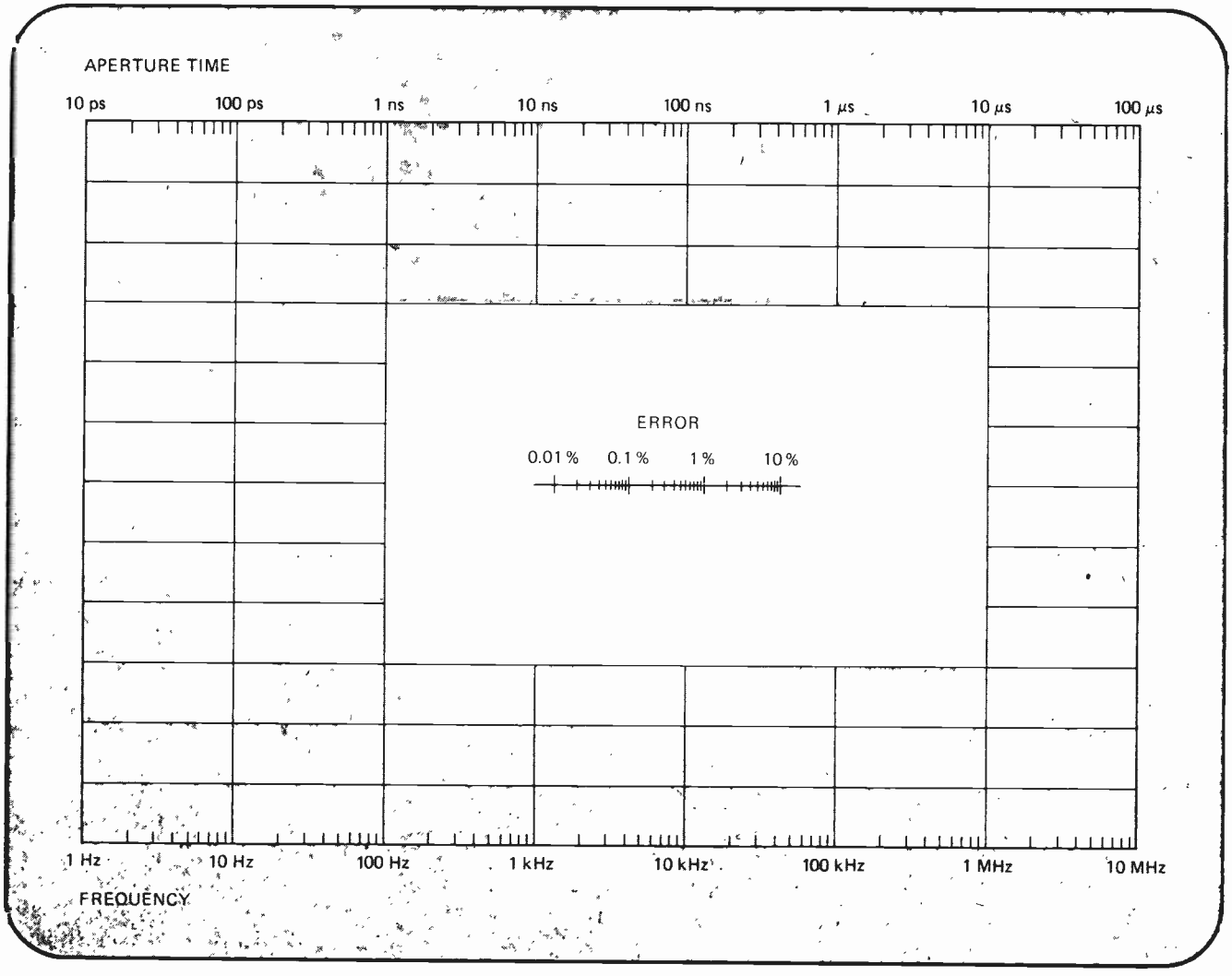
An automatic gain control network at the negative feedback terminal of the audio amplifier assures a low-distortion sine-wave output. The MOSFET acts as a variable resistor. Its resistance is set so that the gain of the amplifier and the loss of the frequency determining network are equal when the desired output is reached.

Negative half cycles of the output are rectified by a diode and filtered by capacitor C_3. Resistor R_3 provides a slight discharge path so that the peak level of the rectified voltage is maintained at the gate of the MOSFET, keeping output level constant.

If amplifier gain increases and output amplitude also rises, more negative bias is applied to the MOSFET's gate, increasing MOSFET resistance to reduce amplifier gain and output amplitude. If the amplitude decreases, the MOSFET becomes biased in the forward direction so that its resistance is lowered, and both gain and amplitude are increased.

The audio amplifier used has an open-loop gain of 70 dB. Attenuation of the frequency determining network is 26 dB.

Power audio oscillator. MOSFET acts as variable resistor to control gain of audio amplifier, which functions as both oscillating element and power amplifier. If output amplitude becomes larger than desired, MOSFET is back-biased, increasing its resistance and lowering amplifier gain. When amplitude falls below desired level, MOSFET is forward-biased to decrease its resistance and increase amplifier gain.



Bootstrapped capacitor stabilizes UJT oscillator

by Michael J. Debronsky
KDI Labtron Corp., Dayton, Ohio

A highly accurate low-frequency relaxation oscillator can be built by making the circuit independent of the unijunction transistor's interbase resistance. Simply bootstrapping the voltage of the charging capacitor through a temperature-compensated zener diode back to the UJT's $base_2$ does the job. Good frequency stability can be attained—0.05% over a 0°C–55°C temperature range and 0.5% for a 100% change in the supply.

There are certain circuit conditions that must be observed, however, for good stability. The value of timing capacitor C_1 must be much greater than that of bypass capacitor C_2. The latter bypasses any zener noise to avoid output jitter. Moreover, current through timing resistor R_1 must be more than Q_1's base current, and the UJT's voltage must be larger than the zener's.

C_1 is discharged by the UJT when its voltage is:

$V_e = \eta V_z(1-\eta)$

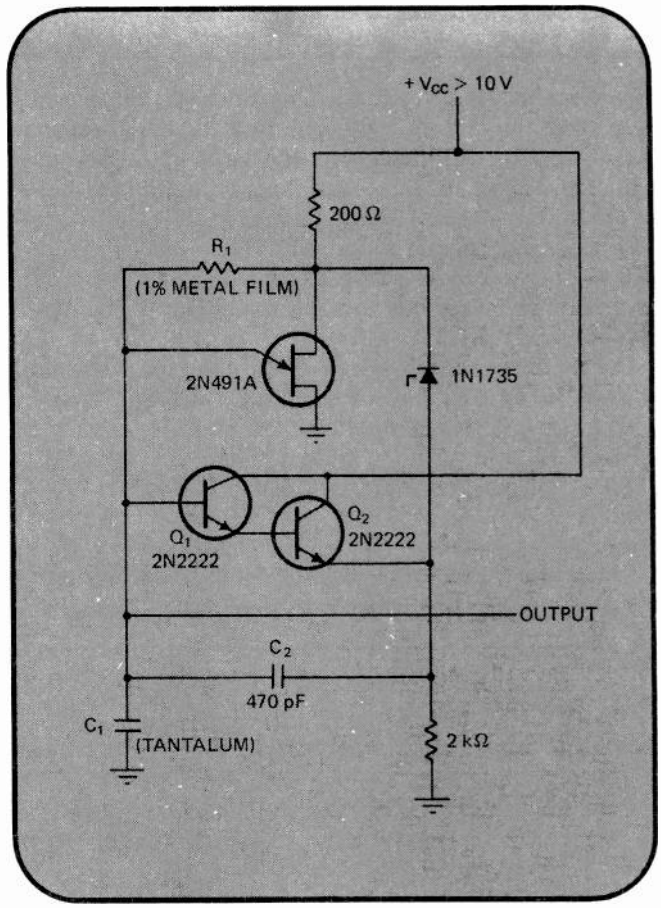
where η is the intrinsic standoff ratio of the UJT, and V_z is zener voltage. Usually, the base-emitter voltages of Q_1 and Q_2 are small compared to V_z. Then:

$$V_e = \frac{1}{C_1}\int i(t)\,dt = V_z t/R_1C_1$$

And output pulse duration becomes:

$t = 1/f = \eta R_1C_1/(1-\eta)$

For 60-Hz operation, R_1 ranges from 10 to 50 kilohms, and C_1 must be greater than 0.001 microfarad.



Tightening frequency stability. Low-frequency oscillator provides frequency stability of 0.05% over a temperature range of 0°C to 55°C. Bootstrapping voltage of timing capacitor C_1 back to $base_2$ of unijunction frees oscillator circuit from dependence on UJT's interbase resistance, the usual cause of instability. Temperature-compensated zener and bypass capacitor C_2 are also used.

Brief Fortran program for active low-pass filters

by Irvine P. Stapp, Jr.
University of Kentucky, Lexington, Ky.

A short computer program, written in 1130/1800 Fortran, makes it possible to design three-pole active low-pass Butterworth filters with gains between 1.00 and 2.00. What's more, the program can be easily translated into Basic computer language.

Unlike previous programs, the one shown in (a) uses a simple iterative procedure to converge on normalized element values, instead of solving for the roots of a cubic equation. This technique simplifies calculating gains other than unity. Finding capacitor values that are accurate to one part in 10^7 (0.1 ppm) requires about 30 traversals of the iteration loop.

A filter designed with the program shown in (b) provides a 15-hertz cutoff frequency and a gain of 1.20. The filter is intended to drive a multiplexer input network with a gain of 1/1.20.

If a small amount of gain is included in an active filter, many scaling amplifiers frequently can be eliminated from a multiplexed analog-to-digital system where over-all gain must be maintained at some established value. For example, certain process control com-

puters, like the IBM 1800, require multiplexer input points to be preloaded with low impedances, in the order of 1 kilohm shunted by 0.05 microfarad. Only a few operational amplifiers can tolerate this much capacitance with a tight feedback loop. But many will function properly if decoupled from the capacitive load by about 100 ohms.

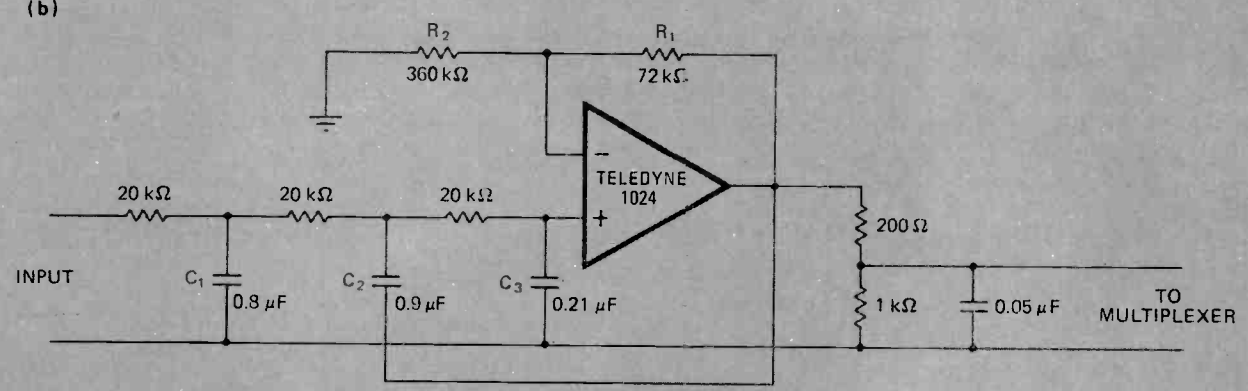
A sample of the program's output, also included in (b), shows the design solution: K is the number of iterations required to reach desired accuracy; L, M, and N are normalized capacitor values in farads for a 3-decibel point of 1 radian per second. Besides capacitor values, the program finds the values for R_1 and R_2 that yield optimum filter gain.

Other common low-pass filtering functions can be realized with the program by modifying the iterative equations. A data card is needed to indicate the number of runs, followed by cards specifying, for each run, the desired cutoff frequency in hertz, the resistance level in ohms, and amplifier gain. Program statement 23 points out where the data should be placed on the card. The program is easily adapted for remote terminals.

(a)

```
      WRITE (4,21)
21    FORMAT('1ELEMENT VALUES FOR 3-POLE LOW PASS BUTTERWORTH FILTER WIT
     1H PREASSIGNED GAIN BETWEEN 1.00 AND 2.00.'//' K IS LOOP INDEX WHEN
     2 SOLUTION CONVERGED TO 0.1 PPM.'//' L,M,N ARE CAPACITOR VALUES IN
     3FARADS, NORMALIZED TO 1 OHM, 1 RADIAN/SECOND.')
      READ (3,20) NRUN
20    FORMAT (I2)
      DO 88 J=1,NRUN
      READ (3,23) F,R,G
23    FORMAT (T1,E13.6,T15,E13.6,T30,E13.6)
      AM =1.
      AN = 1.
      AL = 1.
      E=G-1.
      DO 200 K=1,99
      BM=AM
      BN=AN
      BL=AL
      AL=2.-3.*AN+2.*AM*E
      AN=(2.+AM*AL*E)/(2*(AL+AM))
      AM=1./(AL*AN)
      IF (AL*AM*AN-1.E-04) 250,250,260
26C   IF (ABS(BL-AL)+ABS(BN-AN)+ABS(BM-AM)-1.E-07) 300,300,200
25C   E=E+1.E-05
 2CC  CONTINUE
30C   WRITE (4,22) K,AL,AM,AN ,G
 22   FORMAT('0',T3,'K=',I3    ,T21,'L=',E13.6,T38,'M=',E13.6,T56,'N=',E
     113.6,T74,'G=',E13.6 )
      Q= 159154.9/(F*R)
      C1=AL*Q
      C2=AM*Q
      C3=AN*Q
      RK=R*1.E-03
      R1=3.*G*RK
      R2=R1/E
      WRITE(4,24) G,RK,F,C1,C2,C3 ,R1,R2
24    FORMAT ('0','FOR GAIN OF',F6.2,' AND RESISTORS OF',F6.2,' KILOHMS
     1 A CUTOFF FREQUENCY OF',F9.2,' HERTZ REQUIRES'//' ','C1=',F9.6,3X
     2,'C2=',F9.6,3X,'C3=',F9.6,1X,'MICROFARADS. OPTIMUM GAIN-SETTING RE
     3SISTORS ARE '//' ','R1=',F9.4,3X,'R2=',F9.4,1X,'KILOHMS'///' ',119
     4('1H*'))
88    CONTINUE
      CALL EXIT
      END
```

(b)




```
ELEMENT VALUES FOR 3-POLE LOW PASS BUTTERWORTH FILTER WITH PREASSIGNED GAIN BETWEEN 1.00 AND 2.00.

K IS LOOP INDEX WHEN SOLUTION CONVERGED TO 0.1 PPM.

L,M,N ARE CAPACITOR VALUES IN FARADS, NORMALIZED TO 1 OHM, 1 RADIAN/SECOND.

 K= 29            L= 0.150211E 01  M= 0.169718E 01   N= 0.392253E 00   G= 0.120000E 01

FOR GAIN OF  1.20 AND RESISTORS OF 20.00 KILOHMS  A CUTOFF FREQUENCY OF    15.00 HERTZ REQUIRES

C1= 0.796896   C2= 0.900386   C3= 0.208096 MICROFARADS. OPTIMUM GAIN-SETTING RESISTORS ARE

R1=  71.9999   R2= 360.0000 KILOHMS
```

Filter design. Fortran listing (a) eases design of three-pole active low-pass Butterworth filters. Program finds capacitor values and optimum-gain resistors. Filter gain is preset between 1.00 and 2.00; the value of ladder resistors is also fixed. Program uses iteration for extremely accurate capacitor determination. Design example for 15-hertz filter and sample of program output are given in (b).

Feedback current switch divides rf inputs by 20

by Roland J. Turner
RCA Corp., Missile and Surface Radar division, Moorestown, N.J.

In a ripple-carry binary feedback counter, counting down to 20:1 requires five binary stages, and the time it takes for the signal to pass through all five stages limits counting speed. But an analog counter that employs positive feedback around a single current switch stage requires only one transition period to establish the count. This current switch, which has a transition time in the order of 1 nanosecond, counts a 1-gigahertz signal down to 50 megahertz in one stage. Two switches in cascade, then, provide a 400:1 countdown.

The usefulness of the counter lies in its ability to provide a low-frequency sync signal that is locked to an rf carrier, so that full advantage can be taken of an oscilloscope's vertical bandwidth. The detailed characteristics of each rf cycle of the signal may then be observed on a scope with a low-frequency sync capability.

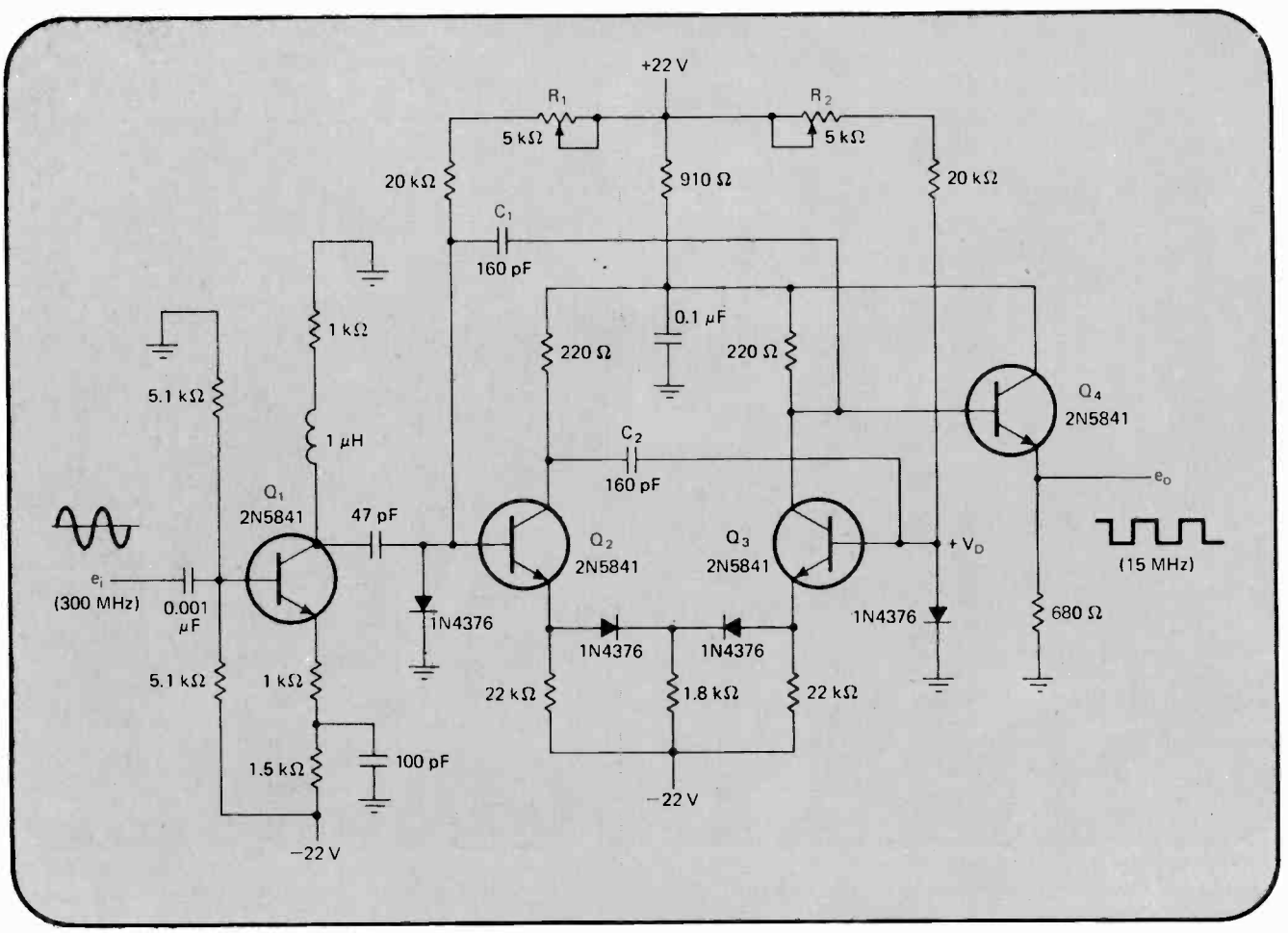
When an rf signal at the base of transistor Q_1 goes positive, the base of transistor Q_2 is driven negative, turning Q_2 off. As the emitter current of Q_2 changes, the emitter current of transistor Q_3 is forced to increase, and starts positive feedback action through capacitor C_1 to the base of Q_2. Additional positive feedback is fed from the collector of Q_2 to the base of Q_3 through C_2.

During the recovery period of Q_2, the current switch formed by Q_2 and Q_3 acts as a high-speed comparator, while the base voltage of Q_2 decreases toward ground. As soon as the most positive swing of the input signal exceeds the V_D bias at the base of Q_3, positive feedback begins again, and the switch automatically resets itself to the initial state. Transistor Q_4 serves as an output buffer to drive another analog stage. The output is a square wave with a 2.2-volt peak-to-peak amplitude.

Potentiometers R_1 and R_2 control the initial bias condition of Q_2 and Q_3, respectively. And the collector bias of both Q_2 and Q_3 is well above their saturation voltage. Moreover, when one of these transistors is in cutoff, it still has a 1-milliampere idling current to assure that it maintains a high f_T.

The countdown of the circuit can be altered by returning R_2 to a different supply voltage.

Divide-by-20 counter. Analog circuit counts down rf signal in one transition. For positive input, Q_2 turns off and Q_3 turns on, causing positive feedback to Q_2's base. While Q_2's base voltage approaches ground, Q_2 and Q_3 perform as high-speed comparator. When rf input exceeds Q_3's base bias, positive feedback resets Q_2 and Q_3 to their initial state. Q_4 is buffer stage for output square wave.



Tunable active filter has controllable high Q

by Max Artusy
Stanford Electronics Laboratories, Stanford, Calif.

A tunable variable-Q active narrowband filter can be built from a slightly modified Wien-bridge oscillator with a net loop gain of less than unity. Not only can Q be independently controlled, but stable single-frequency Qs as high as 2,000 can be realized. A gain of 600 is achieved with a Q of 2,000. Gain becomes approximately 140 when Q is 30, and Q remains constant within ±10% over a 10-to-1 tuning range. (Gain, in this case, refers to signal gain, from input to output, rather than amplifier or loop gain.)

Although it is generally known that the effective Q of an oscillating tuned circuit is infinite, it is often forgotten that stable finite Qs can be obtained by reducing the net loop gain below unity. In the conventional Wien-bridge oscillator, the gain of the amplifier looking into its non-inverting input is maintained at 3, and the circuit oscillates. For the modified oscillator, however, amplifier gain is less than 3, allowing the Q of the surrounding RC network to be increased. And, as can be seen from the diagram, the value of resistor R_1 is the same as that for resistor R_2, and the value of capacitor C_1 is identical to the value of capacitor C_2.

Signal current is introduced into the negative feedback loop by R_3, which also determines input impedance and circuit Q. For oscillation to occur:

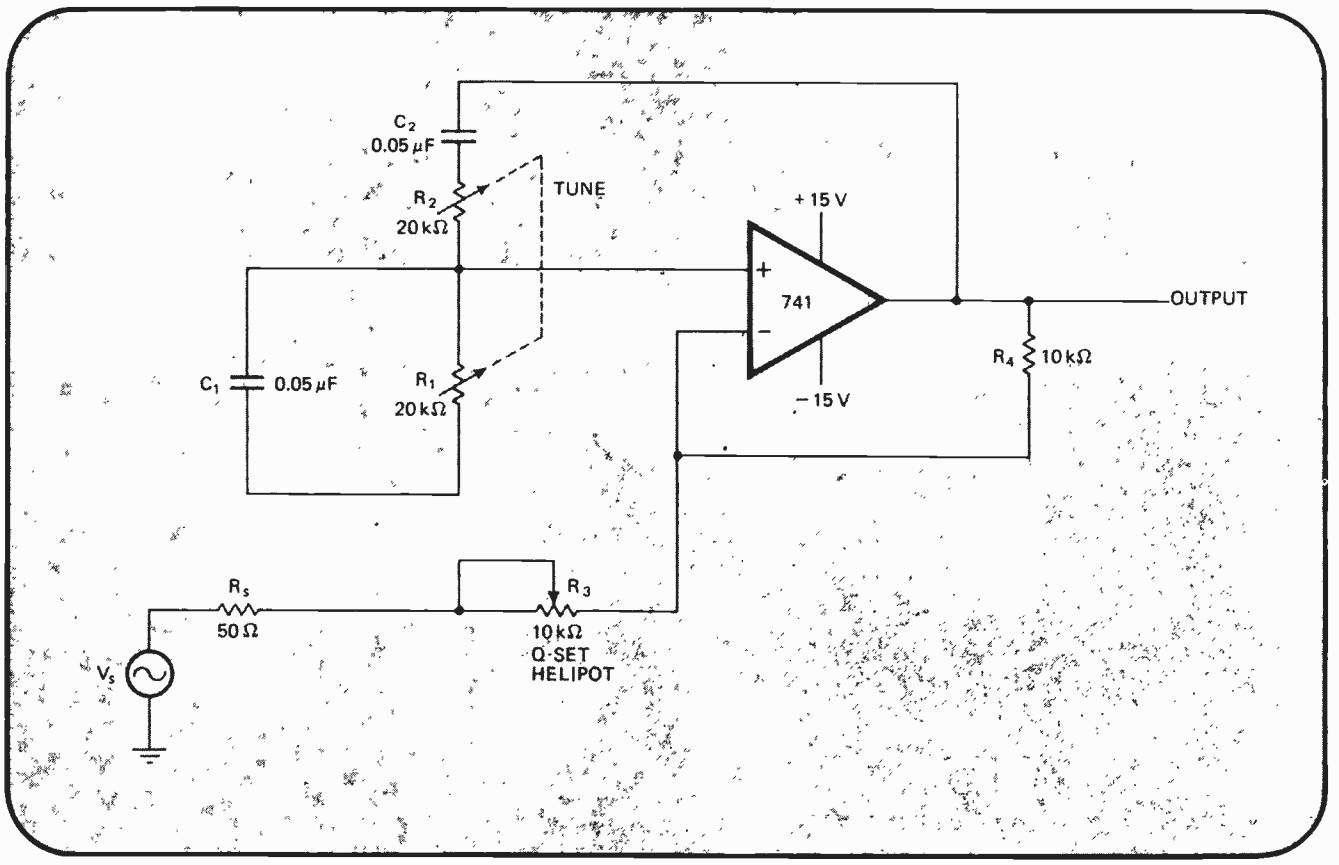
$1 + R_4/(R_3+R_s)$ must be less than 3.

where R_s is the source impedance. Resonant frequency becomes:

$f_o = \frac{1}{2\pi}(R_1R_2C_1C_2)^{1/2}$

Circuit components should be selected carefully for best tuning range and constant Q. In particular, well-matched wirewound potentiometers help maintain uniform Q with changing frequency. All capacitors should be Mylar. Nominal component values shown result in a tuning range of 160 hertz to 1.6 kilohertz for the circuit.

Adjustable Q. Active filter offers Q of up to 2,000 that is stable to within ±10% for moderate Qs over 10-to-1 tuned frequency range. Actually a modified Wien-bridge oscillator, the circuit operates with a net loop gain of less than 1 so that Q of RC network can be increased. Potentiometers R_1 and R_2 and capacitors C_1 and C_2 determine filter resonant frequency, while potentiometer R_3 is an independent Q adjustment.



Op amps generate precision staircase

by Jerald Graeme
Burr-Brown Research Corp., Tucson, Ariz.

A staircase generator with adequate precision for sequential control and multiple-level testing produces a staircase output by differentiating and then integrating only the negative transitions of a square wave. Although a staircase waveform can be generated precisely by a digital-to-analog converter driven by a clock-controlled counter, a simpler, but sufficient, circuit approach is to use operational amplifiers.

Amplifier A_1 differentiates and rectifies input square wave e_i, which is applied to capacitor C_1 through resistor R_1. For positive input transitions, transistors Q_1 and Q_2 are off, and diode D_1 conducts; for negative transitions, Q_1 and Q_2 conduct. From this rectification, only negative-going transitions are transferred to the second amplifier through Q_1 and Q_2. Transistor biasing is implemented by connecting one input of A_1 below ground through resistors R_2 and R_3.

The staircase output is produced by amplifier A_2, which integrates, through capacitor C_2, the current supplied by Q_1 and Q_2. The change in output voltage (Δe_o) becomes:

$$\Delta e_o = -\frac{I}{C_2}\int i(dt)$$

where:

$i = C_1 de_i/dt$

Or, whenever input voltage change (Δe_i) is less than 0:

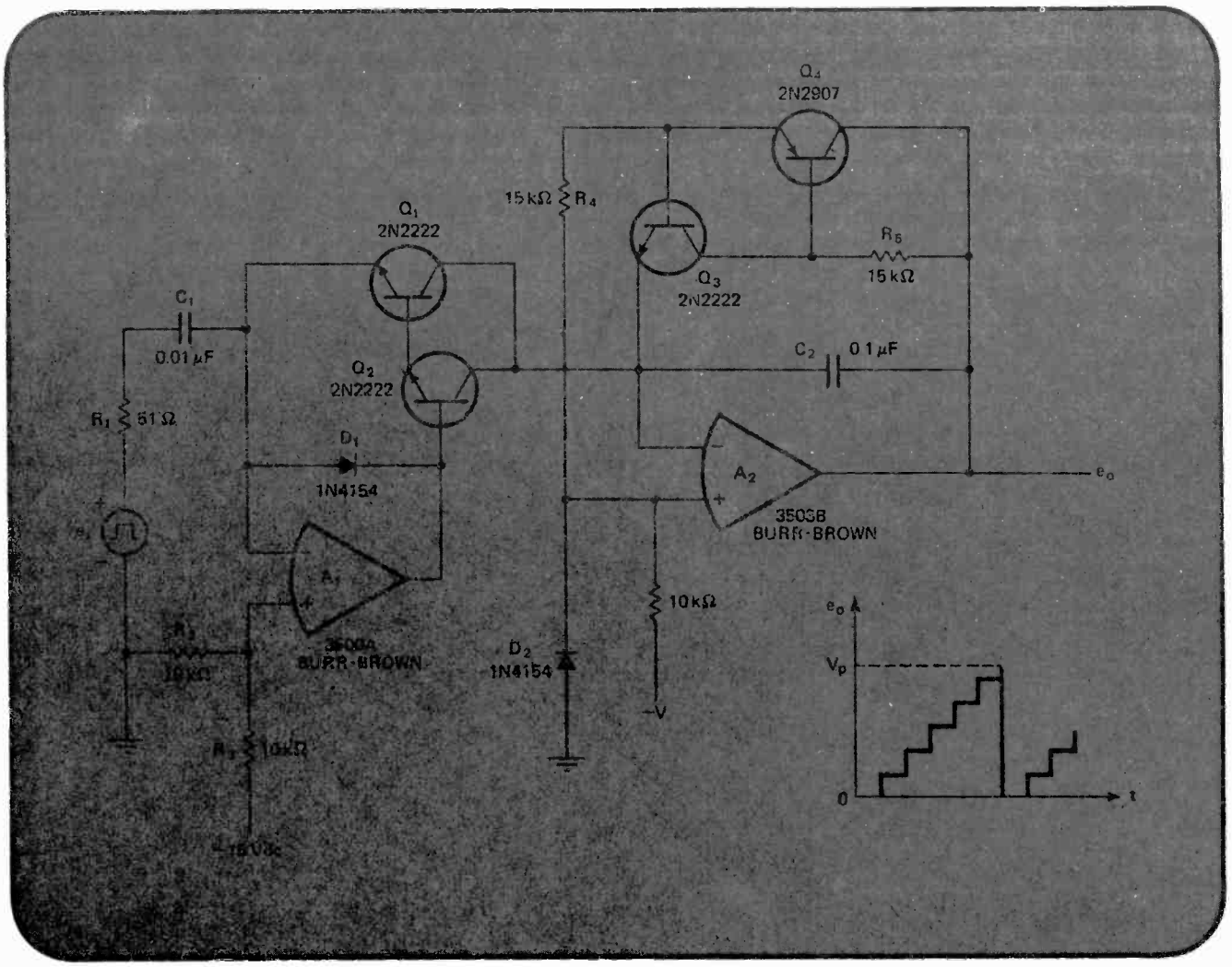
$\Delta e_o = -C_1 \Delta e_i / C_2$

Each negative transition of the input square wave creates a step in the output voltage, generating a staircase waveform. This stepping continues until the output voltage reaches the trigger level of the reset clamp formed by transistors Q_3 and Q_4.

The clamp triggers when the emitter-base junction of Q_4 breaks down, limiting the output to a peak voltage (V_p) of:

$V_p = V_{CB} - BV_{EB} + V_{BE} - V_f$

Stepping up. Staircase generator first differentiates and then integrates input square wave to supply precise stepped output. A_1 performs the differentiation, and Q_1 and Q_2 rectify all negative-going inputs, passing them on to integrator A_2. Positive input transitions are not used. Every negative input steps up the output until Q_3-Q_4 reset clamp triggers when Q_4's emitter-base junction breaks down.



where VCB is Q_4's collector-base voltage, BV_{EB} is Q_4's emitter-base breakdown voltage, V_{BE} is Q_3's base-emitter voltage, and V_f is the voltage across diode D_2. Because the collector-base junction of inverted transistor Q_4 is forward-biased, its voltage drop is around that of the diode, and:

$$V_{CB} - V_f = 0$$

—so that V_p is approximately equal to 7 volts:

$$V_p = V_{BE} - BV_{EB}$$

Since the thermal variations of V_{BE} and BV_{EB} approximately cancel, V_p is quite stable, with a temperature coefficient of around 0.01%/°C.

With Q_4's breakdown, base current through Q_3 activates the positive feedback loop formed by Q_3 and inverted transistor Q_4. Capacitor C_2 is then discharged until its voltage reaches V_{BE}, the cutoff for clamp conduction. Once output voltage returns to 0 V, the clamp turns off, and a new staircase begins.

Gain error and nonlinearity for this staircase generator vary with operating frequency and component characteristics. Operational amplifier input currents remove some of the derivative current pulses, and they also create output sag by discharging capacitor C_2. To prevent severe error from being introduced by these op amp input currents, amplifier input protection circuitry must be avoided since such circuitry will draw high current during an input overload.

Slewing rate and overload recovery limit the generator's operating frequency range. Another current transfer error results from the finite betas of transistors Q_1 and Q_2. However, for the Darlington pair used, the loss is only about 0.002%. Resistors R_4 and R_5 are included to reduce an output nonlinearity that is introduced by leakage of the reset clamp. Circuit gain error is typically about 0.05%, and nonlinearity is commonly around 0.1%.

Schottky diodes eliminate two-level NAND gating

by Charles J. Huber,
Westinghouse Electric Corp., Systems Development division, Baltimore, Md.

To eliminate the need for two-level gating with NAND gates, a pull-up resistor and Schottky diodes can perform the AND function at the input of a low-power TTL gate. NAND gating causes an unwanted increase in power consumption and delay time. The diode circuit can be used for decoding sequence-generator outputs, encoding digital signals, and implementing the AND function in counter designs.

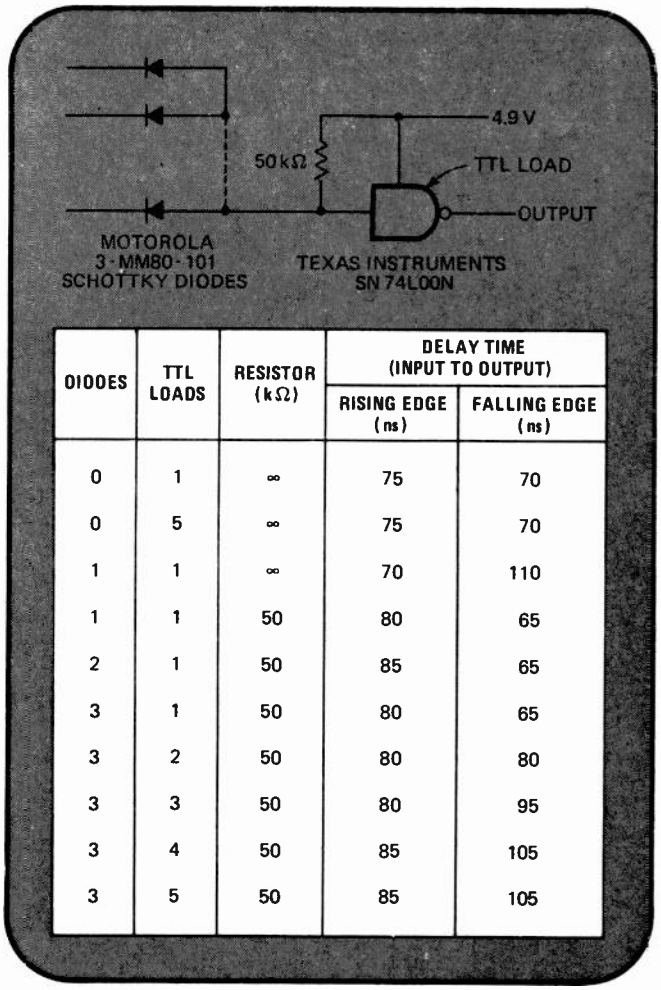
Conventional pn junction diodes are not suitable for use with low-power TTL gates since diode forward voltage drop is comparable to the maximum allowable logic 0 gate input voltage—around 0.7 volt. But Schottky-barrier diodes exhibit only half the voltage drop of pn junction diodes, permitting them to satisfy the TTL logic 0 condition.

Moreover, the dynamic change from logic 1 to logic 0 at the output of a TTL gate is limited, since the common-base input stage is not rapidly cut off. Gate response can be improved considerably by placing a resistor from the supply line to the gate's input pin.

The test results in the table show that the worst-case degradation of gate response time from no diodes to three diodes is 35 nanoseconds for five-TTL loads. Since this time factor is comparable to the propagation delay of only one TTL gate, an entire gate delay is saved and the power consumption is due principally to the pull-up resistor. When three diodes are used, the dc level at the diode-resistor junction is approximately 0.5 V.

Designer's casebook is a regular feature in Electronics. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $50 for each item published.

Diode gating. Pull-up resistor and Schottky diodes replace NAND gates at input of low-power TTL circuits, improving gate response time and decreasing power consumption. Since Schottky diode drop is only half that of pn junction diodes, Schottky diodes are compatible with logic 0 condition of TTL gates. Pull-up resistor decreases gate response time by connecting gate input directly to supply.



DIODES	TTL LOADS	RESISTOR (kΩ)	DELAY TIME (INPUT TO OUTPUT)	
			RISING EDGE (ns)	FALLING EDGE (ns)
0	1	∞	75	70
0	5	∞	75	70
1	1	∞	70	110
1	1	50	80	65
2	1	50	85	65
3	1	50	80	65
3	2	50	80	80
3	3	50	80	95
3	4	50	85	105
3	5	50	85	105

Stable square-wave generator provides broad bandwidth

by William Standke
Honeywell Inc., Corporate Research Center, Hopkins, Minn.

A high-speed analog comparator and a linear current source are the key elements in a stable square-wave generator that can oscillate from a few hertz up to several megahertz. The generator circumvents two common sources of stability error—a nonlinear capacitor-charging current and limited op amp bandwidth.

Current source Q_1 linearly charges capacitor C_1 until capacitor voltage exceeds the reference zener voltage on one of the comparator inputs. The normally high output of the NAND gate then goes low, starting the one-shot timing cycle. As the output of the one-shot goes high, Q_2 turns on and sinks the current from Q_1 so that C_1 is quickly discharged. When the one-shot finishes its timing cycle, its output goes low, Q_2 turns off, and C_1 begins to charge for the next cycle. Circuit oscillation period is approximately:

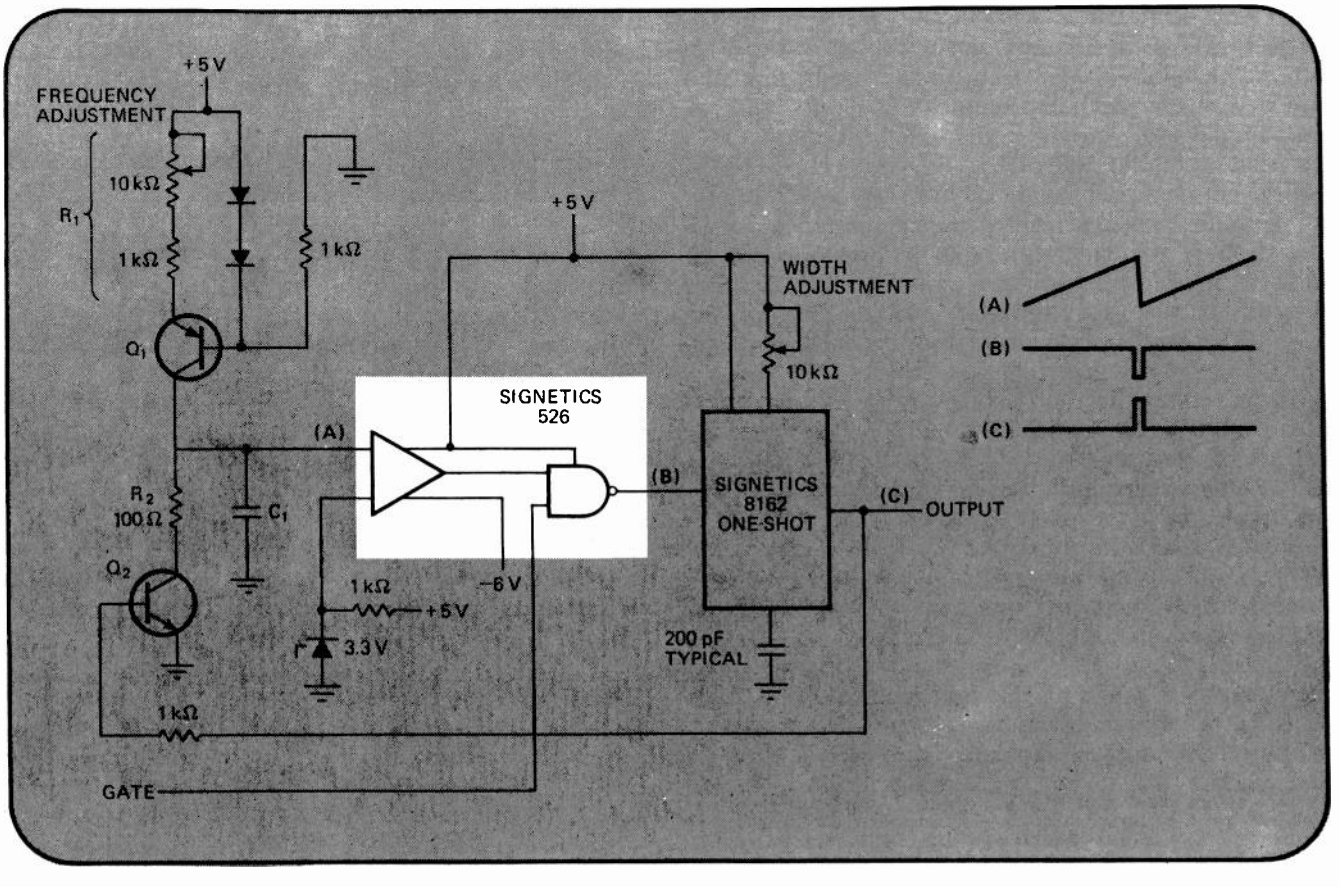
$T = 3.3C_1R_1/0.7$ + one-shot width

One-shot output pulse width should be as narrow as possible for width stability, but wide enough to discharge fully the timing capacitor. Resistor R_2 slows down this discharge. Although R_2 can be eliminated for small values of capacitance, it must be included for large capacitances to protect Q_2 from excessive currents.

The generator's gate input line allows it to be started and stopped with a digital signal. It should be noted that the generator always starts in the same phase, and its initial cycle has the same period as the subsequent ones. If the gating feature is not wanted, the gate line should be connected to a positive supply voltage (V_{CC}). In addition, the generator can be used as a voltage-controlled oscillator by replacing the zener with a control voltage or by controlling the base voltage of Q_1.

The silicon transistors and switching diodes selected, as well as capacitor C_1, depend on the operating frequency desired.

Controlled pulses. Square-wave generator offers stability and wide operating frequency range. C_1 accepts linear charge from Q_1 until its voltage reaches that of zener. Comparator then switches, starting one-shot and turning on Q_2, which discharges C_1. When one-shot timing cycle is complete, Q_2 goes off, and C_1 charges again. Gate input permits generator to be controlled digitally.



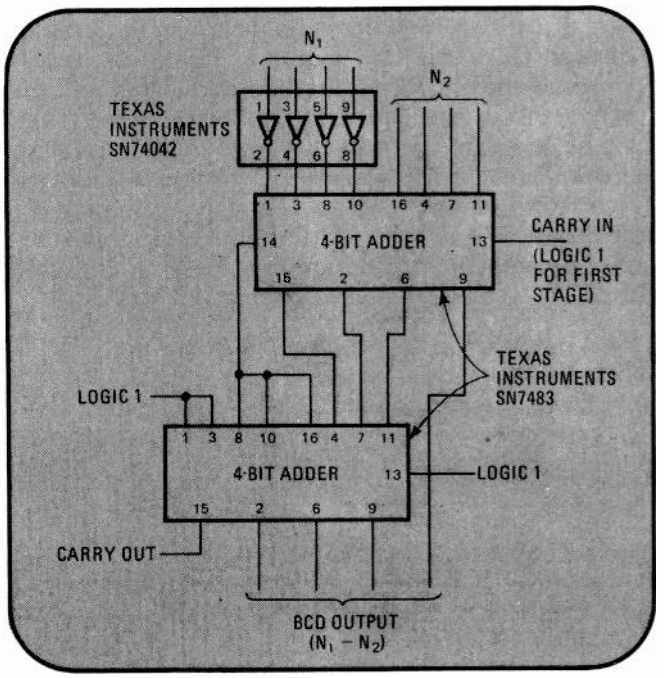
Two adders form BCD subtractor

by Peter K. Bice
Hewlett-Packard Co., Microwave Division, Palo Alto, Calif.

Engineers often avoid using binary-coded-decimal (BCD) designs because the arithmetic involved seems to be formidable. But BCD arithmetic can be almost as simple as binary arithmetic. The circuit shown, for instance, does BCD parallel subtraction. All that is needed for each digit is two four-bit adders and four inverters.

The first adder does the actual arithmetic, subtracting one digit from the other. The second adder converts this difference to BCD form and, if necessary, generates a "borrow" for a subsequent stage. The CARRY OUT is always logic 1 unless a "borrow" is being generated. The last subtractor stage will have a logic 1 CARRY OUT if the difference between the two numbers is positive or if the difference is zero.

The diagram shows one digit of a parallel subtractor. The stages can be cascaded, or one stage can service a serial shift register. BCD addition, it should be noted, cannot be implemented as easily as BCD subtraction since more hardware is required.



Digital arithmetic. A couple of four-bit adders and four inverters are all of the hardware required to build a BCD parallel subtraction circuit. Top adder takes actual difference between input numbers N_1 and N_2. Second adder then forms BCD number of this difference. Both "borrow" and CARRY OUT lines are included for use with other stages. Subtractors can be cascaded.

VSWR detector protects class C rf amplifiers

by Frederick A. Warren, Jr.
Harris-Intertype Corp., Radiation Systems division, Melbourne, Fla.

An inexpensive protection circuit against open-circuit damage to class C rf amplifiers senses and detects voltage standing wave ratio with a single-turn transformer. In addition, the circuit removes drive from high-power stages, has low insertion loss, and suppresses second harmonics with a notch filter.

Any class C rf power amplifier must be operated with a load, once supply voltage and an rf signal are applied. If the load is removed, a high VSWR is created, and rf power is reflected back to the output transistor's collector. The resulting rf voltage swing can exceed the transistor's collector-base breakdown voltage, causing collector current to increase in an avalanche manner so that the base-collector or base-emitter junction opens. Risking this destruction is normally unavoidable, unless the designer is willing to accept a significant insertion loss or pay a high price for protection.

Figure (a) shows a block diagram of a high-power class C vhf amplifier—consisting of transistors Q_1, Q_2 and Q_3—externally connected to the protection circuit. When the amplifier drives a properly matched load, a quiescent rf voltage develops across transformer T_1. This voltage is then rectified by hot-carrier diode D_1, producing a negative voltage at the junction of resistors R_1, R_2, and R_3. The values of R_2 and R_4 force transistors Q_4 and Q_5 into saturation, creating a short circuit between Q_4's collector and ground that allows Q_1 to operate normally, relatively insensitive to load phase.

If the amplifier load is removed or shorted, a high VSWR results, and the rf voltage across T_1 increases. The rectified voltage at the resistor junction then becomes more negative and pulls the base voltage of transistor Q_5 down, driving both Q_4 and Q_5 into cutoff. Now, Q_1's emitter opens, removing the drive to transistor Q_3 and therefore shutting off the amplifier.

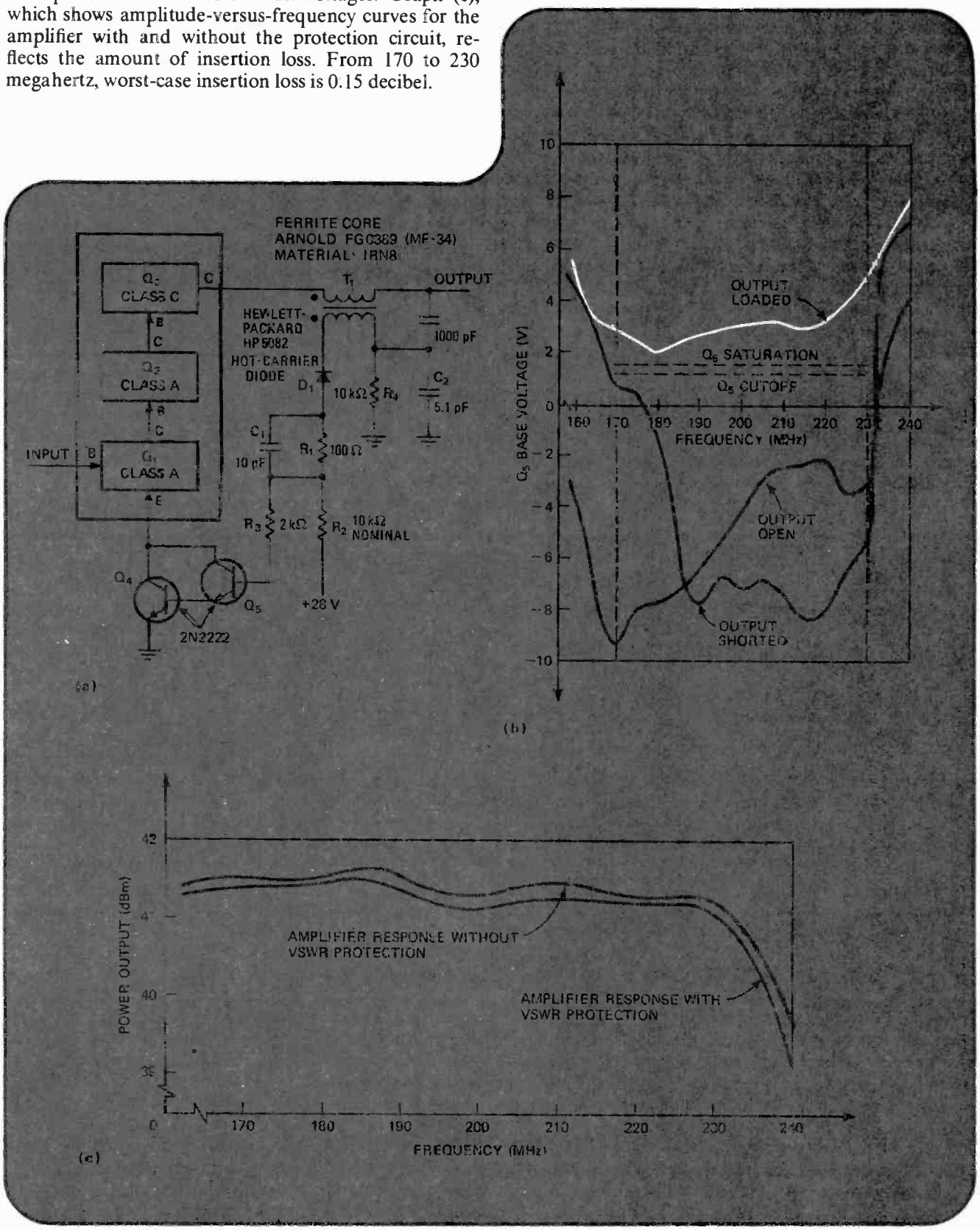
For adequate circuit reaction time, the R_1C_1 time constant should be less than one period of the amplifier's operating frequency. Resistor R_3 sets the quiescent base current of Q_5. And the Q_4-Q_5 Darlington pair operates with only a small drive voltage differential between transistor cutoff and saturation regions.

The protection circuit also offers the advantage of second harmonic suppression (the second harmonic of an amplifier must be below some maximum power level). Because a class C amplifier is usually operated in a saturated condition, it often generates high-level harmonics that require additional filtering after the output stage, thereby creating undesirable insertion loss or complexity. But the protection circuit provides an integral notch filter whenever its transformer's secondary winding and capacitor C_2 are tuned to the second harmonic of the amplifier's fundamental frequency. And VSWR detection by the protection circuit suffers only

negligible degradation because of the filter.

Graph (b) depicts the voltage levels at the base of transistor Q_5 when the amplifier output is loaded, opened, or shorted. The saturation and cutoff voltages shown are those needed for the Darlington circuit. They must be less than the loaded voltage but greater than the open-circuit and short-circuit voltages. Graph (c), which shows amplitude-versus-frequency curves for the amplifier with and without the protection circuit, reflects the amount of insertion loss. From 170 to 230 megahertz, worst-case insertion loss is 0.15 decibel.

Load watchdog. Output of class C rf amplifier (a) goes to protection circuit that shuts off amplifier when VSWR exceeds safe operating limit. Transformer T_1 performs as VSWR sensing and detection element. Removing or shorting load pulls down Q_5's base voltage, cutting off Q_4-Q_5 Darlington pair and opening Q_1's emitter to turn off amplifier. Plots (b) and (c) illustrate amplifier performance.



Transducer preamplifier conserves quiescent power

by Robert F. Downs
Ocean & Atmospheric Science Inc., Santa Ana, Calif.

A low-voltage micropower preamplifier holds power dissipation to approximately 13 microwatts because of the low bias current of its two-transistor impedance converter output stage. The preamplifier, which is intended for use with a capacitive transducer, operates at a quiescent current of 10 microamperes with a supply voltage of only 1.35 volts.

The gate of field-effect transistor Q_1 is essentially biased at 0 V through resistor R_1. Negative feedback, provided by resistor R_2, maintains Q_1's gate-to-source voltage at approximately -0.4 V, forcing its drain current to less than 4 μA. Resistor R_2, therefore, contributes significantly to Q_1's bias stability.

Preamplifier input impedance depends on both R_1 and the voltage gain of the field-effect transistor stage. Actual FET intrinsic input impedance can be ignored since it is orders of magnitude larger than R_1.

If e_i denotes input signal voltage, the voltage across R_1 can be expressed as $e_i(1+K_v)$, where K_v is the stage's voltage gain. Since current through R_1 is increased by a factor of $1 + K_v$, the apparent input impedance is $R_1/(1+K_v)$.

On a small-signal basis, then, the preamplifier's input stage is equivalent to a common-source configuration, while the bias arrangement is that of a source-follower. For the over-all circuit, the dc input impedance is around 1.5 megohms, while the ac input impedance is about 300 kilohms.

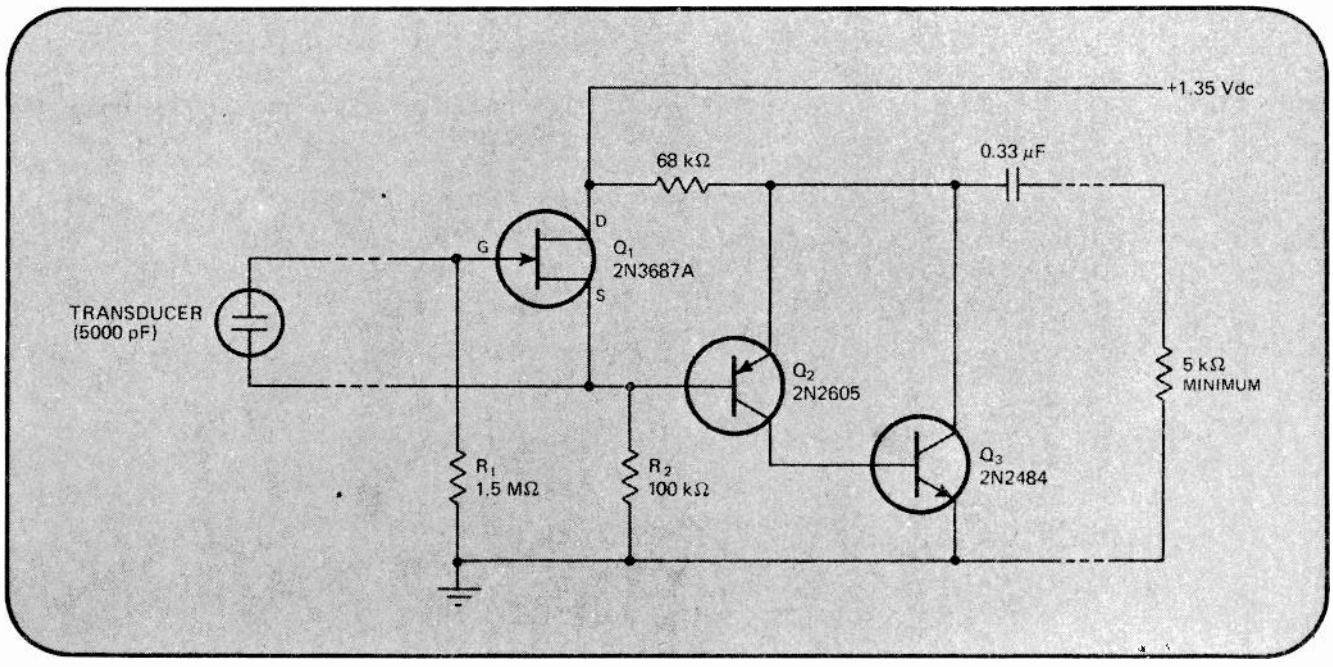
The FET selected for this circuit should have a low pinch-off voltage (V_P) and a low drain current (I_{DDS}) when the gate-source junction is shorted. For the device used, V_P is about 0.1 V and I_{DSS} approximately 100 μA. Because a FET's transconductance (g_m) depends on drain current, Q_1's g_m is only around 50 micromhos.

Since the FET's output conductance is negligible, its output impedance, like that of a common-source stage, essentially equals R_2. Because this is a high resistance value, two bipolar transistors, Q_2 and Q_3, are used as an impedance converter.

This converter stage operates like a pnp emitter-follower, providing very high values of current gain and input impedance. Moreover, it realizes greater bias voltage compatibility between the FET and bipolar stages than a conventional Darlington pair could. Converter bias current is about 6 μA, input impedance exceeds 2 megohms, and output impedance is about 4 kilohms.

For the preamplifier, equivalent input broadband noise is relatively low, about 33 μV from 140 hertz to 20 kilohertz. And voltage gain is nominally 5 (14 decibels).

Power pincher. Preamplifier for capacitive transducer input dissipates only 13 microwatts and operates from 1.35-volt supply. Bias current of impedance converter, composed of bipolar transistors Q_2 and Q_3, is only 6 microamperes, keeping total circuit current drain to only 10 μA. FET input stage has source-follower bias arrangement but provides voltage gain of common-source configuration.



Differentiate and count to find frequency error

by Robert C. Rogers
Texas A&M University, College Station, Texas

By counting differential pulse transitions for a known period, a simple error-detection circuit measures the frequency difference between a variable square wave and reference square wave. Usually, frequency error is found by counting both signals for some fixed period and then comparing the resultant values, or by mixing the signals and then counting the beat frequency. The first method often requires a considerable amount of digital logic if high-frequency signals are involved, while the second method is generally limited by the passband of the beat-frequency detector.

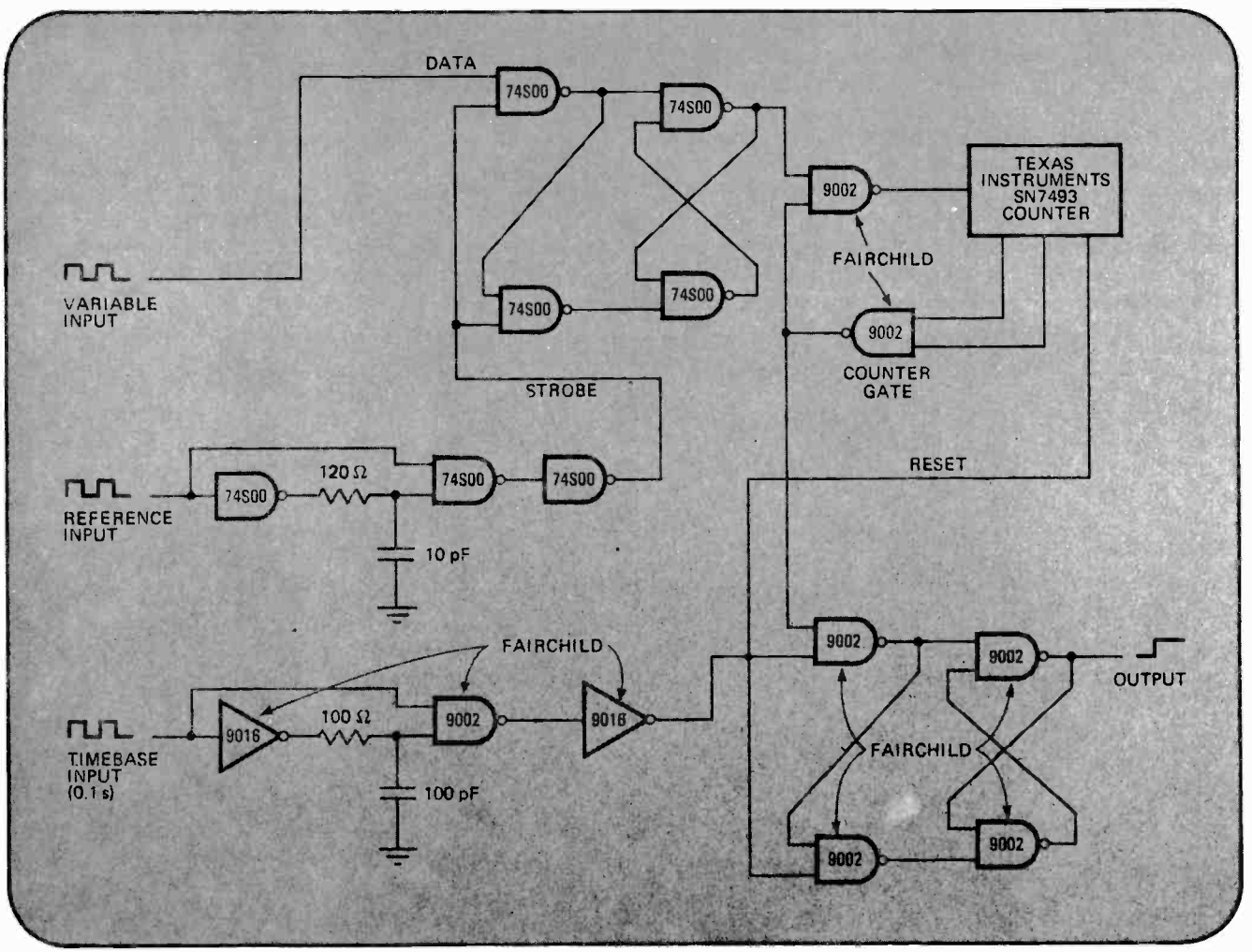
The frequency error detector shown requires input signals that are compatible with logic circuits. (A zero crossover detector could be used initially to prepare the inputs.) The reference square wave is differentiated and applied to the strobe input of a latch, and the variable square wave is applied to the data input of the latch.

How many positive or negative transitions the latch output makes in a given period represents the number of times the variable frequency has gained or lost a full cycle relative to the reference. Counting these transitions for a known period, then, yields the total frequency error during that period. A high-level output indicates that the variable is within the limit.

The time-base input signal sets the latch to a logic 1 if the four-bit counter does not reach a value of 10 in the preceding 0.1-second timing interval. This signal is also used to reset the counter for the next counting period, which begins when the reset pulse returns to zero.

There are two drawbacks that should be remembered. The detector fails if the variable frequency becomes identical to the reference in both frequency and phase, and it becomes ambiguous when the variable frequency is either a higher or lower harmonic of the reference. However, even with these limitations, the detector is useful and reliable over the reference range of 5 to 20 megahertz. Error limit for the circuit shown is ±100 hertz and can be changed by altering the number detected by the counter gate.

Frequency error detector. Differentiated reference square wave drives latch strobe input; variable square wave feeds latch data input. Counter logs either positive or negative transitions of latch output for specific period to total frequency error between inputs. High circuit output indicates error is within desired limit. Time-base signal sets latch and resets counter. Detector range is 5 to 20 MHz for ±100 Hz.



Feedback latch reduces memory recovery time

by Joseph McDowell and William Moss
Monolithic Memories Inc., Sunnyvale, Calif.

The cycle time of wire-ORed semiconductor memories can be improved with the addition of a feedback gate to a NAND gate latch. The resulting three-gate configuration, which also includes a diode and a resistor, provides latched data outputs from open-collector memory packages with significantly reduced turn-off delay.

For open-collector devices, like S_1 through S_N in the diagram, the common problem is choosing a pull-up resistor that is small enough for fast turnoff and large enough for the current sinking capability of the package's open-collector driver. Turn-on speed is not usually a problem, since capacitors C_1 through C_N are driven from a low-impedance saturated transistor.

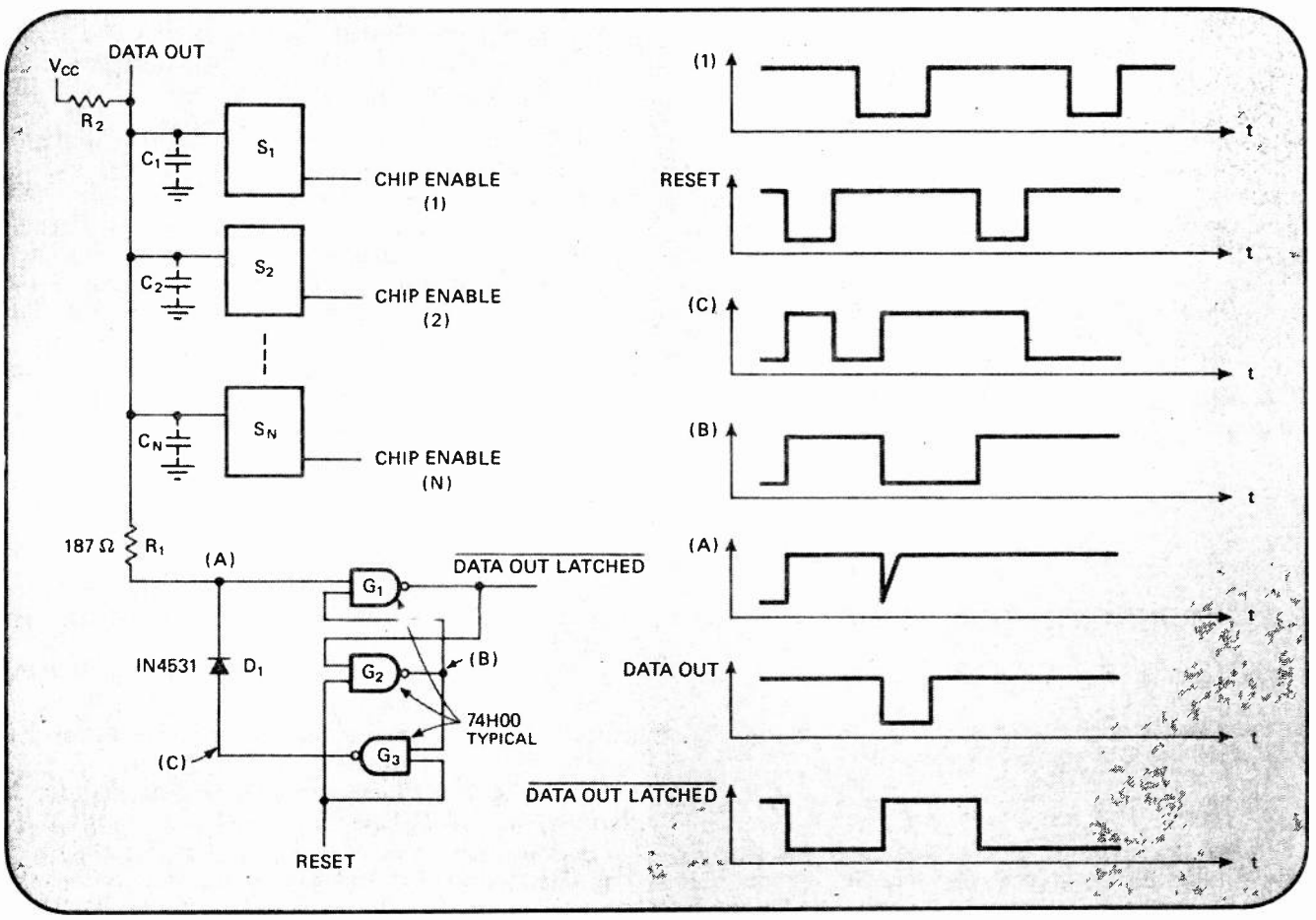
However, turn-off speed or recovery time is determined by the RC time constant at the wire-ORed node. If many memory outputs turn on at once (for example when all low-logic signals are stored in a 72-bit memory word), the change in the power supply load (about 1 ampere in 10 nanoseconds for 15-milliampere open-collector drivers) may require a large pull-up resistor to keep voltage noise within specifications at the expense of turn-off speed.

The illustrated latch employs the common cross-couple gate arrangement of G_1 and G_2. A feedback gate, G_3 actively pulls up the wire-ORed line (like a tri-state gate) after the cross-coupled gates latch. Diode D_1 isolates G_3 from node A, allowing low-level signals to be sensed at this point. To avoid transistor-transistor logic high-level signal problems at node A, D_1 should have a low forward-voltage drop.

Resistor R_1 is used to limit the current from gate G_3 to the open-collector outputs of memories S_1 through S_N. The value of R_1 must be small enough to provide an acceptably low signal level at the latch input. Only the output leakage of the wire-ORed memories and the input leakage of the feedback latch determine the maximum value of pull-up resistor R_2. Recommended values for resistor R_2 range from 1 to 10 kilohms, depending on power supply load considerations.

For 16 wire-ORed memory packages and a 4.7-kilohm pull-up resistor, the feedback latch can reduce turn-off time from 70 to 10 nanoseconds.

Speeding up wire-ORed memories. Cross-coupled gates G_1 and G_2, along with feedback gate G_3, trim turn-off delay for array of wire-ORed memories (S_1 through S_N). Three-gate feedback latch uses diode to isolate G_3 so that low-level signals can be detected at wire-ORed node A. Resistor R_1 prevents surge currents from G_3. Maximum value of pull-up resistor R_2 is determined by leakage currents.



Stable voltage reference uses single power supply

by Mahendra J. Shah
University of Wisconsin, Madison, Wis

When an integrated circuit differential operational amplifier is used in a voltage reference source, two supplies usually are needed—both positive and negative. Moreover, additional circuitry is generally required to establish output polarity. But if one supply line is grounded, only one supply becomes necessary—the one that gives the desired output polarity.

So long as the non-inverting input of the operational amplifier is maintained at some positive potential, even a tiny one, the output of the reference source will also be positive. Similarly, small negative potentials at the non-inverting input will result in negative outputs.

The voltage reference source shown employs a single 15-volt supply to give a positive output. To produce a negative output voltage, the positive supply line is grounded, the negative supply line is run to -15 v, and zener polarity must be reversed.

Zener diode D_Z establishes the reference voltage (V_Z) and the reference current (I_Z) for the circuit so that a constant-current source is provided by resistor R_1 and the buffering action of the op amp. Zener current is:

$I_Z = V_Z R_2 / R_1 R_3$

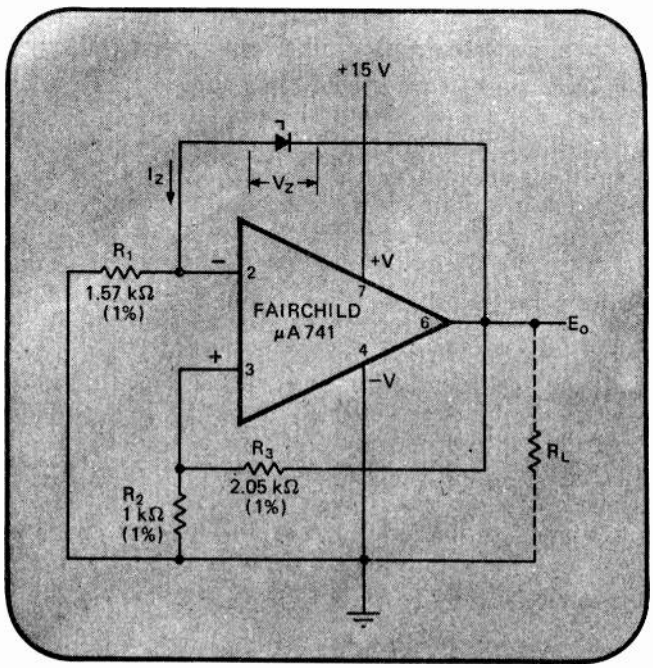
Due to the configuration of the op amp's output stage, circuit output voltage (E_o) will always be greater than 0.5 v when a positive 15-v supply is applied and the negative supply line is grounded. Therefore, a few tens of millivolts will always appear at the op amp's non-inverting input, making the output positive:

$E_o = V_Z(1 + R_2/R_3)$

With the positive supply line grounded and -15 v at the negative supply input, E_o will always be less than -0.5 v. The negative voltage at the op amp's noninverting input causes a negative output:

$E_o = -V_Z(1 + R_2/R_3)$

The reference zener voltage of 6.4 v yields a zener current of about 2 milliamperes. For a positive supply, output voltage is 9.547 v; temperature coefficient, 1.9 parts per million/°C; voltage stability, 9.5 ppm/v; and output impedance, 53 milliohms. For a negative supply, temperature coefficient remains the same; but output voltage becomes -9.560 v; voltage stability, 2.6 ppm/v; and output impedance, 21 milliohms.



Eliminating dual supplies. Voltage reference source has either positive or negative output, depending on polarity of supply used to bias op amp. Positive supply results in positive voltage at op amp's non-inverting input and, therefore, positive output. Negative supply produces negative output. In either case, final output voltage is about 10 volts. Zener diode acts as reference.

Fast-switching modulator reverses uhf signal phase

by R.N. Assaly
Massachusetts Institute of Technology, Lexington, Mass.

In just a few nanoseconds, a modulator for shaping transmitted ultrahigh-frequency radar signals can switch a signal through three states. The signal can be turned on or off, and while it is on, the phase can be reversed between 0° and 180°. An off signal is attenuated by at least 35 decibels.

The modulator (a) consists of a tri-state driver and a double-balanced mixer, which allows the rf signal to be controlled by video commands. Three values of control current— -30 milliamperes, 0 mA, and 30 mA— are generated by the driver for the three modulator states— 0° phase, off, and 180° phase, respectively.

The transition times of the two input logic signals, designated as code Q and gate P, are enhanced by a dual four-input AND gate. (The gate-P input turns the rf

signal on and off, performing a gating function; the code-Q input reverses the phase of an on signal, thereby coding signal phase.) A line driver then produces the outputs labeled A and B:

$A = \overline{PQ}$ and $B = \overline{PQ}$

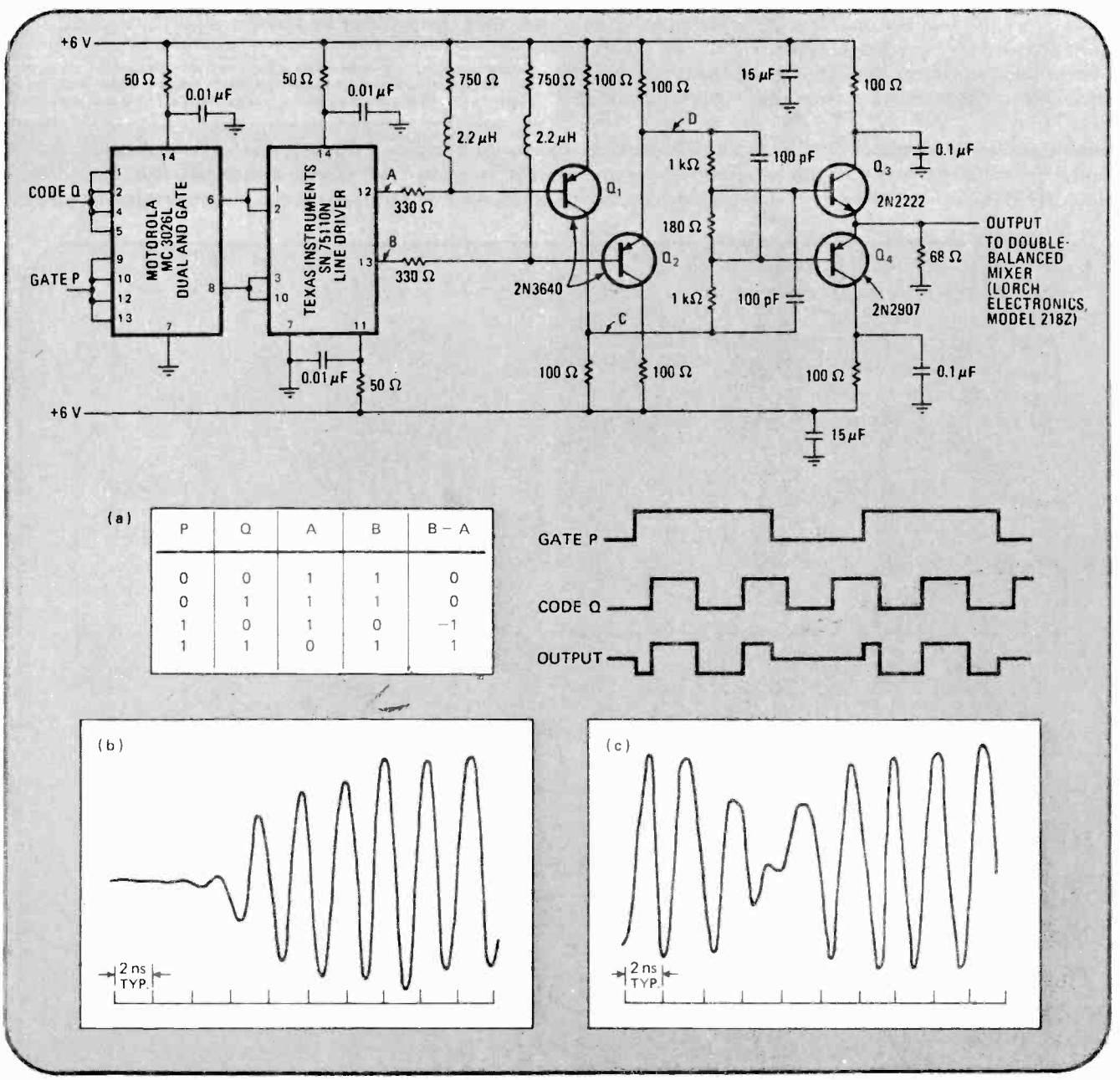
At the tri-state driver output, a difference signal, B–A, is used to provide the three desired states, as shown in the truth table.

To obtain this difference signal, transistor Q_1 inverts the A output of the line driver to produce signal C. And output B passes through transistor Q_2 without inversion, keeping the circuit balanced and resulting in signal D. A resistor network averages signals C and D, which are then applied to output transistors Q_3 and Q_4 that drive the double-balanced mixer.

Since Q_3 and Q_4 do not conduct if their base voltage is less than 0.6 volt, the resistor network holds bias voltage to about 0.5 V during the off state to reduce any delay during driver state transitions. Also, because a large base voltage must be applied either to Q_3 or Q_4 for conduction to occur, mixer current can be held to a very low value. If mixer current increases, to even just a few microamperes, the attenuation of an off signal becomes less than the desired 35 dB. For instance, attenuation degrades to about 30 dB when mixer current becomes approximately 10 microamperes.

Inductors and capacitors in the circuit are simply used to speed up state transitions. The turn-on of a 430-megahertz signal is illustrated in (b), while (c) shows a phase reversal. These transitions took less than 10 ns.

Uhf modulation. Three-state modulator (a) turns off uhf signals or reverses their phase between 0° and 180°. AND gate improves input signal transitions. To balance circuit, line driver output A is inverted by Q_1, while B passes through Q_2 without inversion. Transistors Q_3 and Q_4 drive mixer with difference signal of B–A. Turn-on (b) and phase reversal (c) traces are for 430-megahertz signal.



P	Q	A	B	B – A
0	0	1	1	0
0	1	1	1	0
1	0	1	0	−1
1	1	0	1	1

ECL gates stretch oscillator range

by William Blood
Motorola Semiconductor Products Inc., Phoenix, Ariz.

The frequency range of crystal-controlled oscillators can be extended easily with emitter-coupled logic gates. Selecting the proper crystal and the right number of frequency doublers results in accurate frequency signals over the range of 150 to 250 megahertz. Standard crystals are normally limited to less than 150 MHz because of the number of crystal overtones required to achieve higher frequencies.

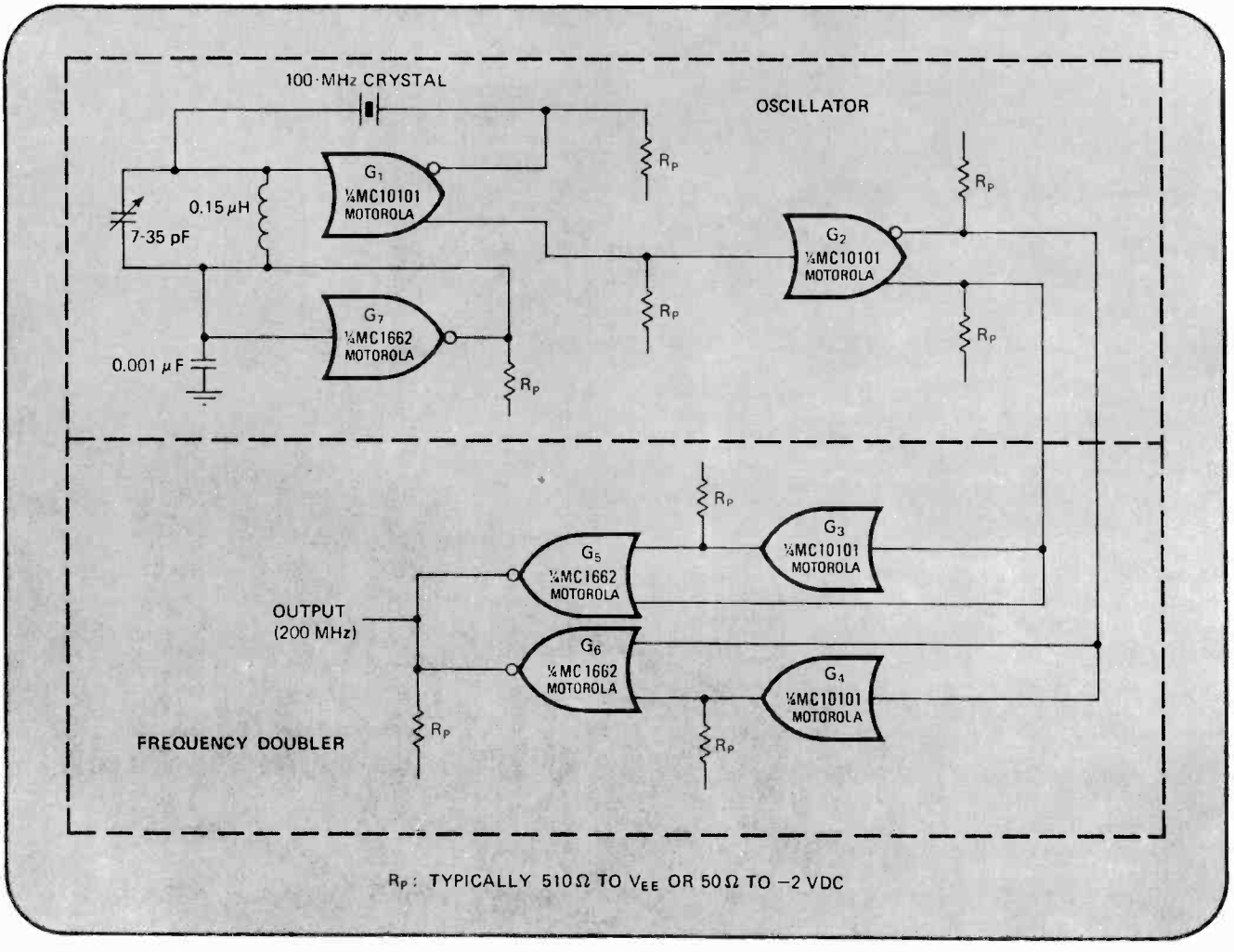
A 200-MHz crystal-controlled oscillator that is built with only two integrated circuit packages is shown in the diagram. Two types of ECL gates, one with a propagation delay of 1 nanosecond and the other with a 2-ns delay, are used for best performance.

In the oscillating section of the circuit, the crystal is in series with a feedback loop from the NOR output of a 2-ns gate, G_1. The LC tank circuit tunes the 100-MHz crystal overtone, and also acts as a fine-tuner. Another 2-ns gate, G_2, from the OR output of G_1, buffers the oscillating section and provides a complementary output.

The frequency doubler section of the circuit consists of two 2-ns gates (G_3 and G_4) performing as phase shifters, and two high-speed 1-ns NOR gates (G_5 and G_6) operating as summers. For a 50% output duty cycle, the complementary 100-MHz signals should be delayed one-fourth of a cycle, or 2.5 ns. This may be done precisely with delay lines, or approximated with gates G_5 and G_6, as shown. The gating method is easier to implement and causes only a slight offset in output duty cycle. Gates G_5 and G_6 combine the four-phase 100-MHz signals, yielding a 200-MHz output frequency, when their outputs are wired-OR.

A third 1-ns gate G_7 is used as a bias generator for the crystal oscillating section. Tying the output of this NOR gate back to its input assures that the oscillating section remains biased in the center of its linear region over wide temperature and power supply extremes.

Speeding up crystal oscillators. Emitter-coupled logic gates can increase the frequency output of crystal-controlled oscillators to 250 megahertz. For 200-MHz output, LC tank tunes 100-MHz overtone of crystal, while gate G_2 forms complementary 100-MHz signals. Phase shifters G_3 and G_4 and wired-OR summers G_5 and G_6 then delay and double these signals. Gate G_7 provides buffered bias supply for gate G_1.



Linear signal limiting with feedback multiplier

by R.J. Karwoski
Raytheon Co., Equipment division, Sudbury, Mass

A signal can be linearly compressed or limited over a wide dynamic range by using a four-quadrant analog multiplier as a feedback element. Particularly useful for audio applications, this linear limiting technique does away with the signal distortion that occurs with nonlinear methods. Also, the linear limiter does not require the careful calibration and many trial-and-error adjustments needed for a nonlinear limiter.

The control section of the linear limiter consists of three operational amplifiers and a multiplier. Op amp A_1 is the throughput amplifier with local feedback through resistors R_F, R_1, and R_2. When R_F is shorted, the control circuitry is bypassed, and the circuit becomes a linear voltage-follower:

$$e_o = e_i(1 + R_F/[R_1R_2/(R_1 + R_2)])$$

The fundamental feedback equation for the limiter is based on amplifier A_1:

$$e_o = A_o e_i/(1 + A_o\beta)$$

where gain A_o is determined by A_1's local feedback arrangement of R_F and R_1 in parallel with R_2. Feedback factor β depends on the control section, whose operating function resembles the basic feedback equation. The relationship between multiplier input e_Y and multiplier input e_X becomes:

$$e_Y = e_X/(1 + e_X)$$

For small values of e_X, this equation degenerates to:

$$e_Y = e_X$$

which is a linear function representing a 1:1 compression ratio between e_o and e_i. For large values of e_X, the function becomes asymptotically limiting:

$$e_Y = e_X/e_X = 1$$

Over-all limiter transfer function can be written as:

$$\frac{e_o}{e_i} = \frac{1 + R_F/[R_1R_2/(R_1 + R_2)]}{1 + 410R_F(e_i)_{pk}/R_2}$$

Multiplier output $e_Xe_Y/10$ and the product of gains of amplifiers A_2, A_3, and A_4 are represented by the factor $410(e_i)_{pk}$, where $(e_i)_{pk}$ is the peak input signal amplitude. Resistor R_F controls both circuit gain and compression. However, for any single value of e_i, the limiter can be set to provide a gain of unity, regardless of R_F's resistance and how much or how little limiting is needed. Additional over-all gain adjustments are then unnecessary, even if the compression ratio must be changed.

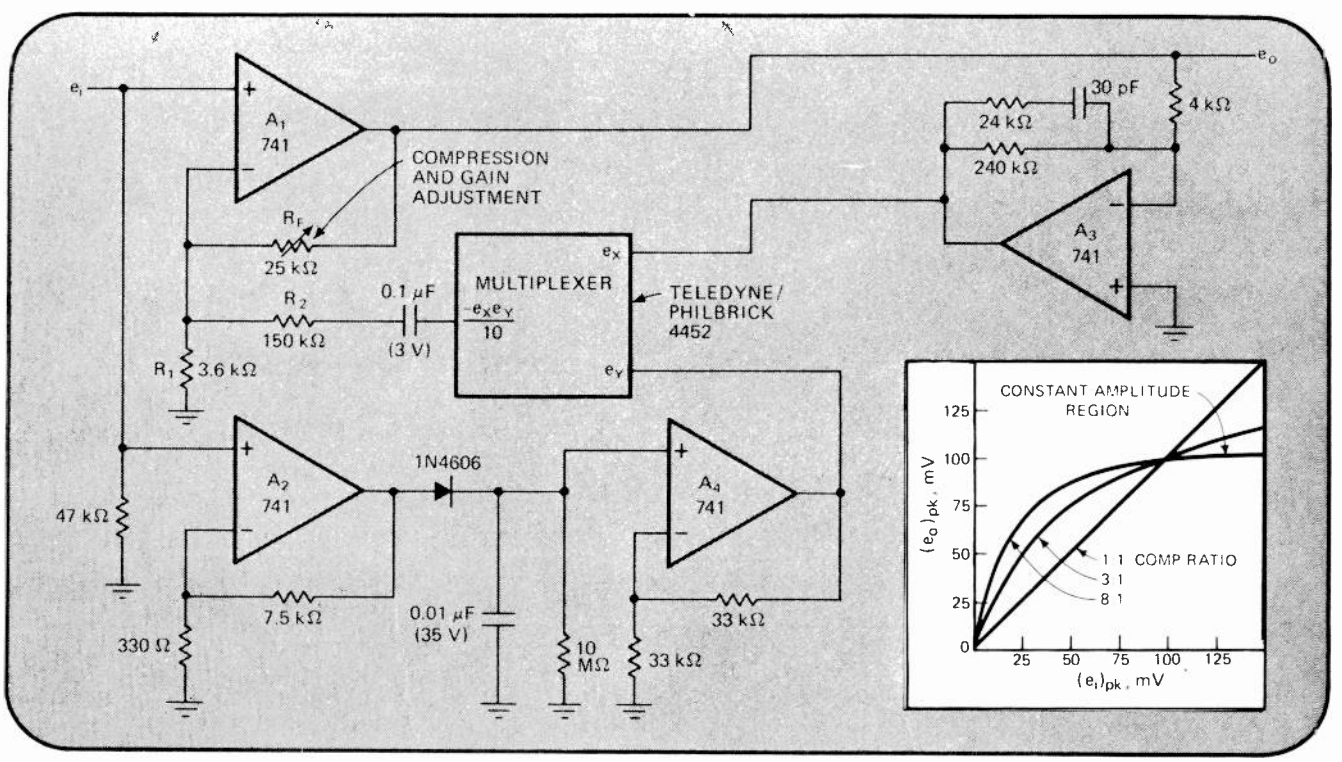
With a 100-millivolt input, the circuit illustrated supplies a 100-mV output, no matter what the setting of R_F. For any value of R_F, resistor R_1 is selected to keep:

$$1 + R_F/[R_1R_2/(R_1 + R_2)] = 1 + 410R_F(100\text{mV})/R_2$$

Circuit compression ratio can be varied by changing the value of R_F, but circuit gain remains unity for $e_i = e_o = 100$ mV.

The performance curves show the limiter's transfer function for three compression ratios with circuit unity-gain point at 100 mV—1:1 (no compression, $R_F = 0$), 8:1 (maximum compression, $R_F = 25$ kilohms), and 3:1 (midrange compression).

Variable linear limiter. Compression ratio can be varied by adjusting resistor R_F without changing circuit gain—limiter's unity-gain point remains $e_i = e_o = 100$ millivolts. Amplifier A_1 is controlled by local feedback through resistors R_F, R_1, and R_2 and by additional feedback from multiplier and amplifiers A_2, A_3, and A_4. When $R_F = 0$, compression ratio is 1:1, when $R_F = 25$ kilohms, compression is 8:1.



Simple logic circuits compare binary numbers

by Edward J. Murray
Inter-Computer Electronics Inc., Lansdale, Pa.

In real-time data acquisition applications, determining the relative magnitude of two binary numbers with hardware, rather than software, now requires only three logic modules if data is being transferred serially. Previously, rather complex circuitry was needed.

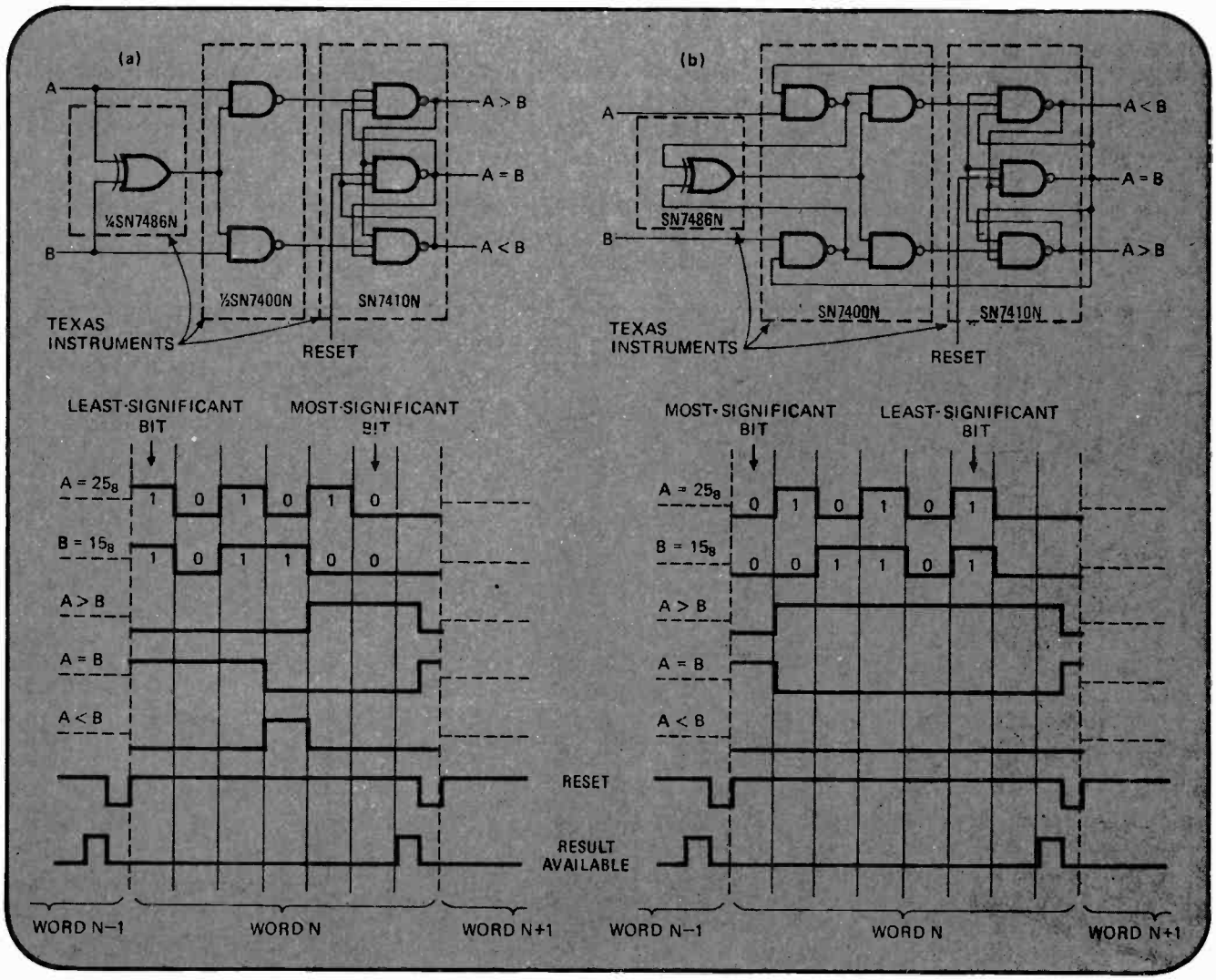
Only the most-significant difference between two coincident serial data streams defines their relative magnitude. If the least-significant bit is transmitted first, the last difference between coincident word bits determines which is the largest word. When the most-significant bit is the first transmitted, the first difference establishes relative magnitude, and all other differences can be ignored.

Six logic gates (a) can compare two words when the least-significant bit is the initial input. Eight logic gates (b) are needed when the most-significant bit arrives first. The heart of both schemes is a three-state latch that provides three comparisons for input words A and B: A is greater than B, A equals B, and A is less than B.

The timing diagrams in (a) and (b) illustrate circuit operation when input A is octal number 25 (binary 010101) and input B is octal number 15 (binary 001101). Signals A and B are not limited to a fixed number of bits per word. Any variable word size can be used if the results are interrogated after the word has been transmitted and a reset pulse precedes the word being interrogated.

This type of binary comparator is useful in preliminary data sorting and number ranging prior to software processing for multi-channel data acquisition. In the timing diagram, the "result available" waveform indicates the best interrogation periods.

Checking number size. To find relative magnitude of serial words A and B, only most-significant differences between coincident data bits must be considered. Transmitting least-significant bit first (a) requires six gates for comparison. Two additional gates are needed (b) if most-significant bit is transmitted first. In timing diagrams, octal 25 (binary 010101) is compared to octal 15 (binary 001101).



Series-connected op amps null offset voltage

by Lawrence Choice
Burr-Brown Research Corp., Tucson, Ariz.

The input offset voltage and offset voltage drift of a differential operational amplifier can be held essentially to zero by connecting a second amplifier at the inverting input of the first. This auxiliary op amp must have an offset voltage and drift that are matched to the primary op amp. The additional amplifier will then act as a floating voltage source, canceling any offset voltage.

As shown in (a), unity-feedback amplifier A_1 is connected to the inverting input of amplifier A_2, providing a floating offset voltage source between A_2's non-inverting input and its output. (If A_1's offset characteristics were matched with opposite polarity to those of A_2, then A_1 could be placed at A_2's non-inverting input.) Letting V_{os} represent the input offset voltage of A_2, V_{A1} the voltage across A_1, A_o the open-loop gain of A_2, and E_1 and E_2 the two input signals, then output voltage E_o can be written as:

$$E_o = -A_o(E_1-E_2) - A_o(V_{A1}-V_{os})$$

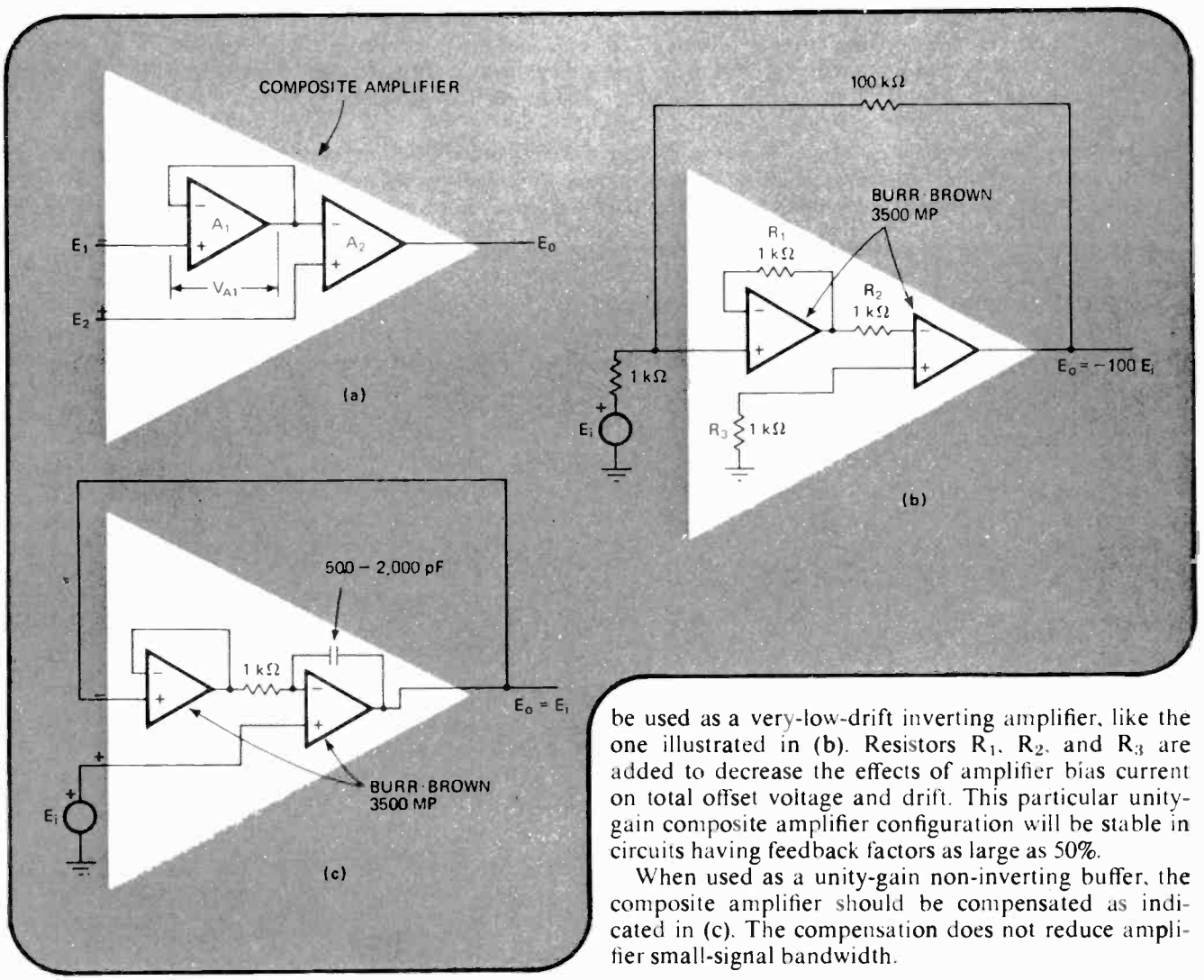
If $V_{A1} = V_{os}$, then:

$$E_o = -A_o(E_1-E_2)$$

The composite amplifier consisting of A_1 and A_2 can be used as a very-low-drift inverting amplifier, like the one illustrated in (b). Resistors R_1, R_2, and R_3 are added to decrease the effects of amplifier bias current on total offset voltage and drift. This particular unity-gain composite amplifier configuration will be stable in circuits having feedback factors as large as 50%.

When used as a unity-gain non-inverting buffer, the composite amplifier should be compensated as indicated in (c). The compensation does not reduce amplifier small-signal bandwidth.

Getting rid of offset voltage. Letting amplifier A_1 act as floating voltage source (a) effectively eliminates offset voltage and offset voltage drift of amplifier A_2. As long as A_1 and A_2 are matched, their offset voltages cancel, keeping offset of composite amplifier at zero. Composite amplifier of (a) can be used as conventional single operational amplifier for either inverting (b) or non-inverting (c) applications.



Unclocked logic element makes quick decisions

by Leslie K. Torok
University of Toronto, Toronto, Ont., Canada

A new kind of logic element can make logic decisions without requiring a clock for synchronization. Called Jade, this asynchronous decision element can operate at speeds as high as clocked logic blocks, offers easy debugging, and allows sequential logic systems to be mechanized directly from flow charts. Moreover, Jade will operate in clocked as well as unclocked systems.

A control signal, DO, functions much like the clock in synchronous logic, while input signal X represents the logic condition that must be decided and acted upon. The Jade element has two states—a quiescent state when signal DO is logic 0 and a decision state when DO is logic 1. There are four possible outputs: XTRUE (X is true), $\overline{\text{XTRUE}}$ (not XTRUE), XFALSE (X is false), and $\overline{\text{XFALSE}}$ (not XFALSE).

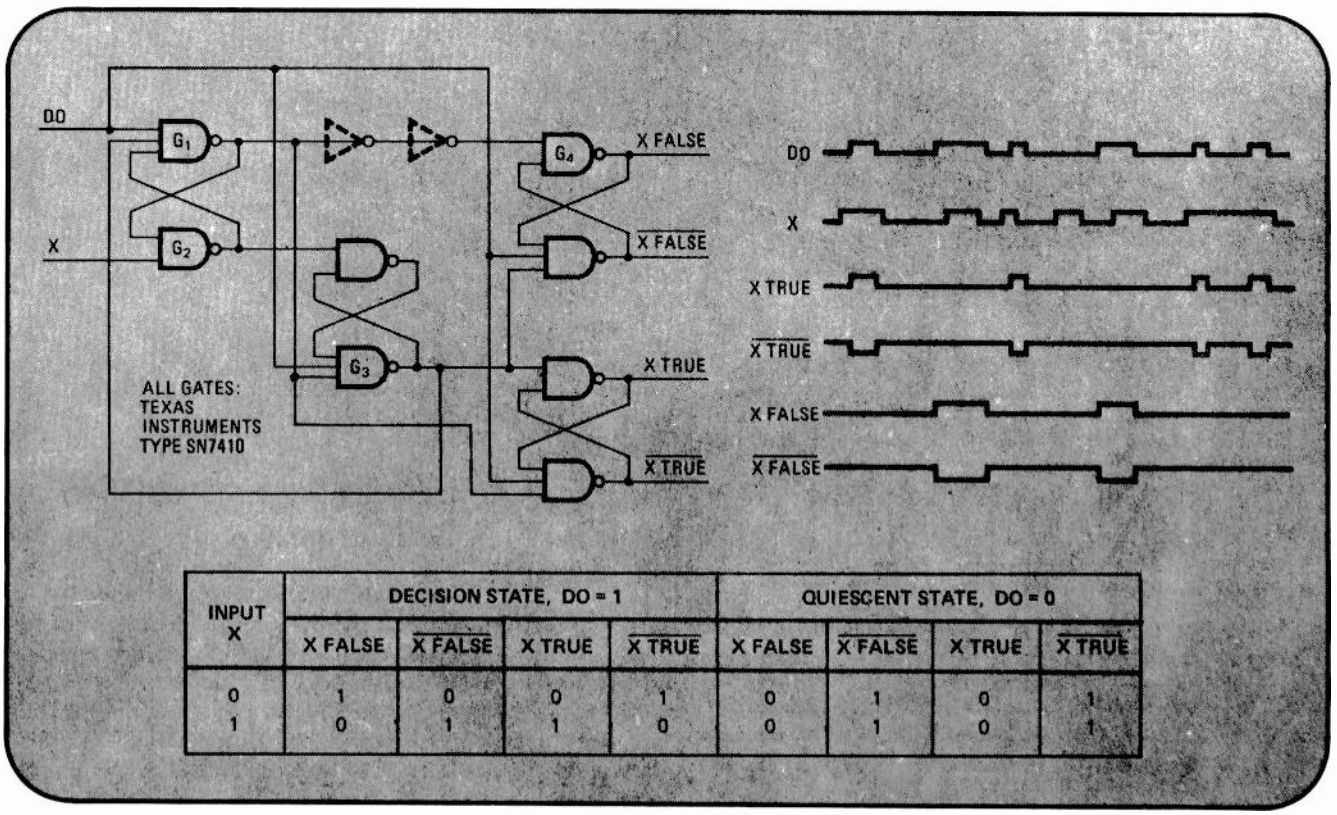
When the Jade is in its quiescent state (DO = 0), XTRUE = XFALSE = 0 and $\overline{\text{XTRUE}}$ = $\overline{\text{XFALSE}}$ = 1. For the decision state (DO = 1), Jade makes an exclusive and singular decision at the rising edge of signal DO — XTRUE = 1 and $\overline{\text{XTRUE}}$ = 0 if X = 1, or XFALSE = 1 and $\overline{\text{XFALSE}}$ = 0 if X = 0. The output decision then activates the appropriate task logic.

As long as DO = 1, further changes in X do not affect the output. Returning DO to logic 0 clears the decision, causing Jade to assume its quiescent state. It should be noted that XTRUE = XFALSE only in the quiescent state. For the decision state, XTRUE = $\overline{\text{XFALSE}}$ and $\overline{\text{XTRUE}}$ = XFALSE, since the outputs are exclusive. Those outputs that are not selected remain quiescent.

As X drops to logic 0 and DO rises, a spike may appear at the output of gate G_1 when the propagation delay of gate G_2 to a logic 1 is less than the propagation delay of gate G_3 to a logic 0. If the spike is wider than the minimum hold time of gate G_4, a double decision is made. To prevent this, two inverters can be placed between G_1 and G_4 to integrate the spike.

Jade can sort decisions at speeds of at least 10 megahertz, with signals X and DO having pulse widths of about 30 nanoseconds. □

Decisions, decisions. Asynchronous decision element named Jade uses control signal DO instead of clock to gate information signal X. When DO is logic 0, circuit is in quiescent state; when DO is logic 1, circuit is in decision state and provides single exclusive output out of four possibilities. Inverters can be added to avoid switching spike that causes erroneous double decision. Truth table shows logic characteristic.



INPUT X	DECISION STATE, DO = 1				QUIESCENT STATE, DO = 0			
	X FALSE	X FALSE	X TRUE	X TRUE	X FALSE	X FALSE	X TRUE	X TRUE
0	1	0	0	1	0	1	0	1
1	0	1	1	0	0	1	0	1

Height-to-width converter digitizes analog samples

by Roland J. Turner
RCA Corp., Missile and Surface Radar division, Moorestown, N.J.

By controlling the charge on a storage capacitor, a temperature-stabilized height-to-width converter can produce a gray code output from an analog input sample. The converter uses a differential diode-transistor arrangement to operate over a temperature range of −55°C to +65°C, and its conversion error is less than 0.15 microsecond for a full-scale output pulse width of 3.25 μs.

During the first half of the input sample, a clear pulse removes all charge from storage capacitor C_1. During the second half, a charge proportional to the sampled analog signal is placed on this same capacitor through transistors Q_1 and Q_2.

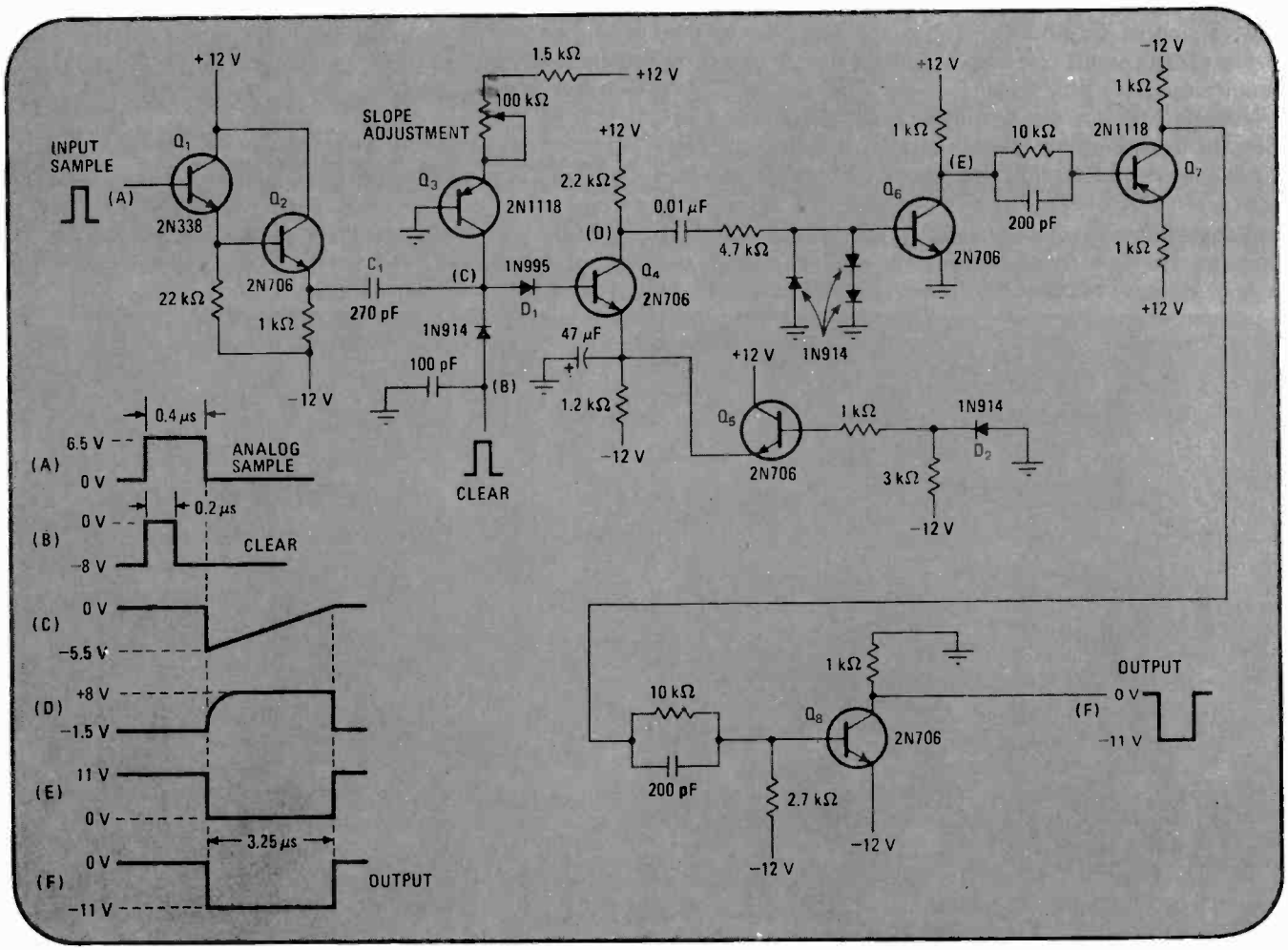
Current source Q_3 keeps diode D_1 forward-biased and transistor Q_4 fully on during the sample time. On the trailing edge of the analog sample, D_1 becomes reverse-biased by a voltage level equal to the amplitude of the analog sample before its termination. Transistor Q_4 is then cut off, and for a period of time that is proportional to the stored analog sample amplitude, a current source formed by Q_3 and the slope-control potentiomteter linearly discharges capacitor C_1.

During the time that Q_4 is off, the converter generates a pulse that has a width proportional to the amplitude of the analog sample. When the stored charge goes to zero, diode D_1 and transistor Q_4 are again turned on by the current source. After Q_4 conducts, a new sample may be processed. Transistors Q_6, Q_7, and Q_8 act as pulse shapers to yield the desired output.

Diodes D_1 and D_2 and transistors Q_4 and Q_5 are connected in a differential configuration to keep Q_4's conduction interval independent of temperature variations. The voltage drops of D_1 and D_2 and the base-emitter voltage drops of Q_4 and Q_5 track each other as temperature varies.

The converter in the diagram is designed to operate with a peak-to-peak video input level of 6.5 volts. Maximum output pulse width is determined by the slope adjustment, which is set to provide a pulse width of 3.25 μs for a an input video level of 6.5 V. The waveforms shown represent the maximum level of the gray code. □

Compensating for temperature. Differential hook-up of transistors Q_4 and Q_5 and diodes D_1 and D_2 maintains temperature stability of height-to-width converter. Amplitude of analog input sample is converted to gray code output. Second half of input sample charges capacitor C_1, then linear current ramp through transistor Q_3 discharges C_1. During discharge time, D_1 and Q_4 are off, and output pulse is produced.



Filament transformer output drops cost of 400-Hz supply

by Glen Coers
Texas Instruments, Components Group, Dallas, Texas

Power supplies with a 400-hertz output are often needed in testing servo systems and aircraft equipment, but they can be expensive to build when their output voltage must be on the order of 115 volts, root mean square. This being the equivalent of a peak-to-peak voltage of 325 V, the circuit transistors would have to have very high operating voltage ratings, and since there are no integrated amplifiers that can handle ±160 V, a discrete amplifier would be required.

Alternatively, the number of parts and component costs can both be considerably reduced by generating the 400-Hz sine wave at some low voltage level and then stepping it up with a transformer. This approach allows low-cost transistors and integrated circuit operational amplifiers to be used, yet it produces enough output power to operate small motors, servos, resolvers, and synchros. Larger output transistors and a larger transformer will, of course, increase output power.

The audio oscillator of (a) provides the sine-wave input for the amplifier of (b). The frequency-determining components for the oscillator are resistors R_1 and R_2 and capacitors C_1 and C_2. These are returned to the non-inverting input of an op amp that functions as the circuit's oscillating element.

Voltage gain for the amplifier is supplied by an op amp, while discrete transistors supply current gain. The input sine-wave frequency can vary from 60 to 400 Hz when a conventional filament transformer is used at the output. With the components shown, an output current of about 250 milliamperes is obtainable.

The amplitude of the input sine wave depends on the amount of feedback in the amplifier network. If the feedback factor is low, a small signal can drive the amplifier, but the output driving impedance becomes high, possibly causing current limiting in the output stage and therefore poor voltage regulation. If the feedback is high, a higher level of input voltage will be required, but the output driving impedance becomes lower and regulation is improved.

Here, op-amp closed-loop gain (A_{vc}) is 10, making the required drive voltage around 1 V rms. The value of feedback resistor R_f is determined by:

$R_f = R_s(A_{vc}-1) = 9$ kilohms

where R_s is source resistance. Feedback factor β is set by R_f and R_s:

$\beta = R_s/(R_s+R_f) = 0.1$

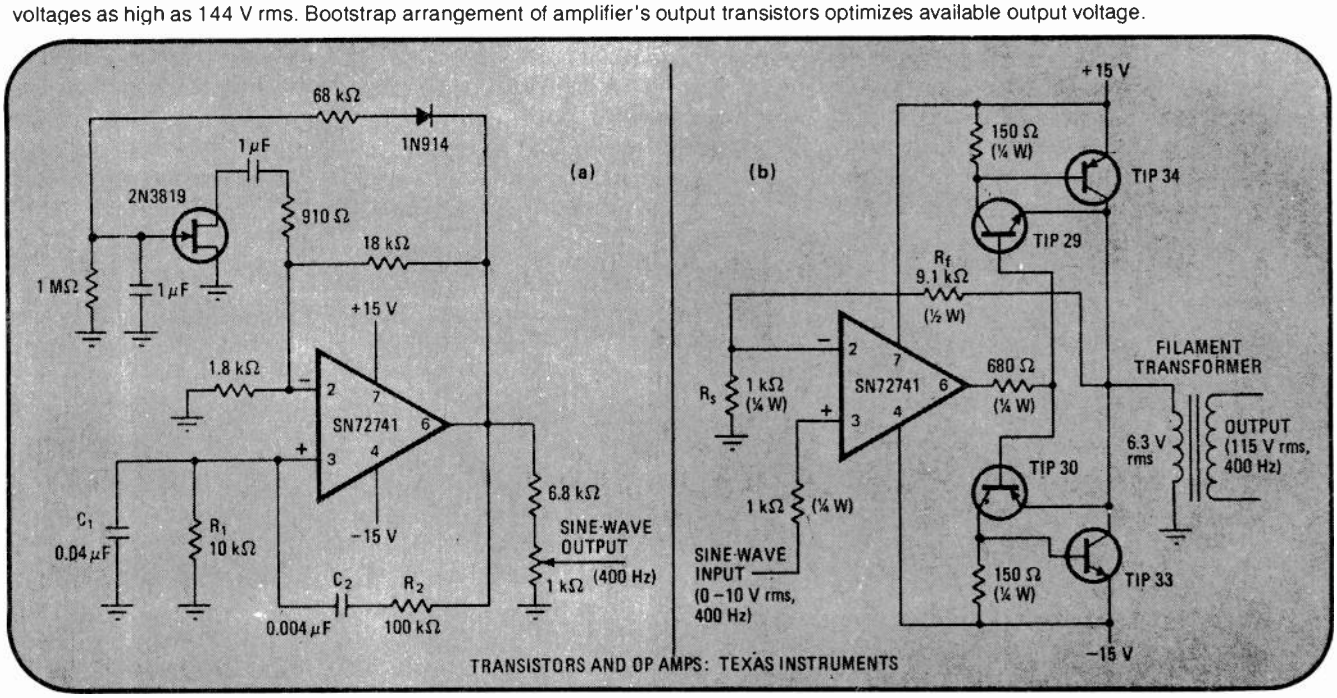
while closed-loop output resistance R_{out} becomes:

$R_{out} = R_o/A_{vo}\beta = 0.01$ ohms

when open-loop output resistance R_o equals 50 ohms, and open-loop gain A_{vo} is 50,000. This last equation indicates that circuit regulation should be adequate because the effective driving impedance is much lower than the load impedance.

The output transistors are connected in a bootstrap arrangement, eliminating two base-emitter voltage drops and allowing more ac voltage to be developed. A Darlington configuration could be substituted, but there would be a 5% drop in the available output voltage. Adjusting the 400-Hz drive voltage varies output voltage between 0 and 144 V rms. □

Servo supply. Amplifying low-level high-frequency sine-wave input cuts parts and price of 400-hertz 115-volt rms power supply. Audio oscillator (a) provides 1-V rms sine wave for amplifier (b). Standard filament transformer delivers output currents of up to 250 milliamperes and voltages as high as 144 V rms. Bootstrap arrangement of amplifier's output transistors optimizes available output voltage.



Regulating high voltage with low-voltage transistors

by Mahendra J. Shah
University of Wisconsin, Madison, Wis.

High-voltage regulation usually calls for high-voltage transistors. But, by absorbing the bulk of the output voltage with a zener diode, only relatively low-voltage devices are needed. The circuit illustrated regulates 250 volts with a 90-v transistor; however, the same concept can be applied to regulating voltages in the kilovolt range.

Transistor Q_1 operates as a shunt regulator, monitoring the output voltage, e_o, across the load. Without zener diode D_1, Q_1 would be subjected to nearly all the output voltage. But D_1 absorbs a good part of this voltage because it is in series with the collector of Q_1. This allows Q_1 to operate at the difference voltage between e_o and the voltage across the zener.

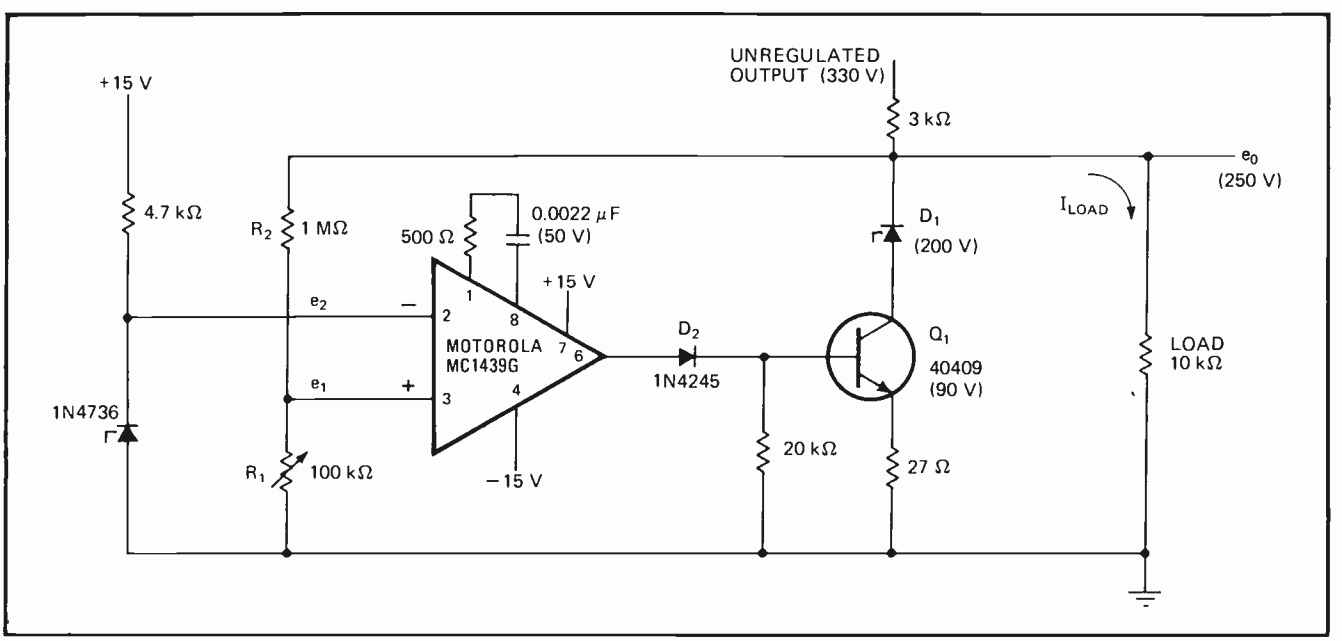
The output voltage is divided by resistors R_1 and R_2 and applied to the non-inverting input of an operational amplifier, which functions as a comparator. The op amp compares e_1 with e_2, and maintains output voltage e_o so that $e_1 = e_2$. Regulated output is a function of the comparator's inverting input voltage, e_2, and the resistors of the voltage divider:

$$e_o = e_2(1 + R_2/R_1)$$

Another diode, D_2, protects Q_1's base-emitter junction from reverse breakdown. During normal operation, D_1 is forward-biased, allowing Q_1 to receive base drive for proper regulation.

For the component values shown, voltage regulation from no load to full load (25 milliamperes) is less than 0.04%. Unregulated voltage is 330 v, and the voltage across Q_1's collector-emitter junction is approximately 40 v. □

Putting a zener to work. Zener diode D_1 handles most of 250-volt regulated output, permitting a mere 90-V transistor to be used. Transistor Q_1 acts as conventional shunt regulator for load resistance. Op-amp comparator maintains output voltage to keep its inputs e_1 and e_2 equal, thereby providing proper base drive for Q_1. Regulated output voltage is: $e_o = e_2(1 + R_2/R_1)$. Unregulated output of 330 V is also available.



Op amps multiply RC time constants

by Quentin Bristow
Geological Survey of Canada, Ottawa, Ont., Canada

Unusually long time constants can be generated with considerable accuracy by combining readily available low-value resistors and capacitors with a couple of general-purpose operational amplifiers. Besides being physically smaller than their higher-value counterparts, low-value components offer tighter value tolerances and do not have leakage or polarity problems. Furthermore, when high-value resistors are used, field-effect-transis-

tor-input op amps must be employed. They are more expensive than general-purpose op amps and do not provide as good input offset and temperature drift specifications.

A number of instrumentation applications require time constants in the order of seconds or minutes. Circuit (a), for instance, can be used to stretch one-shot output pulses, or as a low-pass insertion filter for monitoring slowly changing meteorological, oceanographic, or other geoscientific phenomena where low-frequency noise is undesirable. This network can multiply a basic RC time constant by a factor as large as 10,000. (For example, a 100-second time constant can be realized with R = 100 kilohms and C = 0.1 microfarad.)

When V_i is a step input, output voltages E_1 and E_2 rise exponentially to final values $-V_i$ and $+V_i$, respectively, with a time constant (taken at 63% of the final level) of $(N+2)RC$.

$$E_2 = -E_1 = V_i[1 - \exp(-t/(N+2)RC)]$$

The actual values of resistors R_1 and R_2 are not critical because the time constant is determined by ratio N and the values chosen for R and C. The components indicated provide a time constant of 50 seconds.

The drift and noise of either output referred to the original input V_i will be the same as that obtained when amplifier A_1 is operated at a closed-loop gain of $N+1$, modified of course, by the filtering effect of the time constant generated. After capacitor C is removed, the circuit can be seen to be an op amp (A_1) connected for a closed-loop gain of $N+1$, since amplifier A_2 is simply a unity-gain inverter.

The offset null trimmer permits the E_1 output to be set initially to zero for a zero input. Generally, the trimmer can be omitted for values of N less than 50. To avoid a tedious time lag in circuit output response when making this adjustment, one end of the capacitor should be disconnected temporarily.

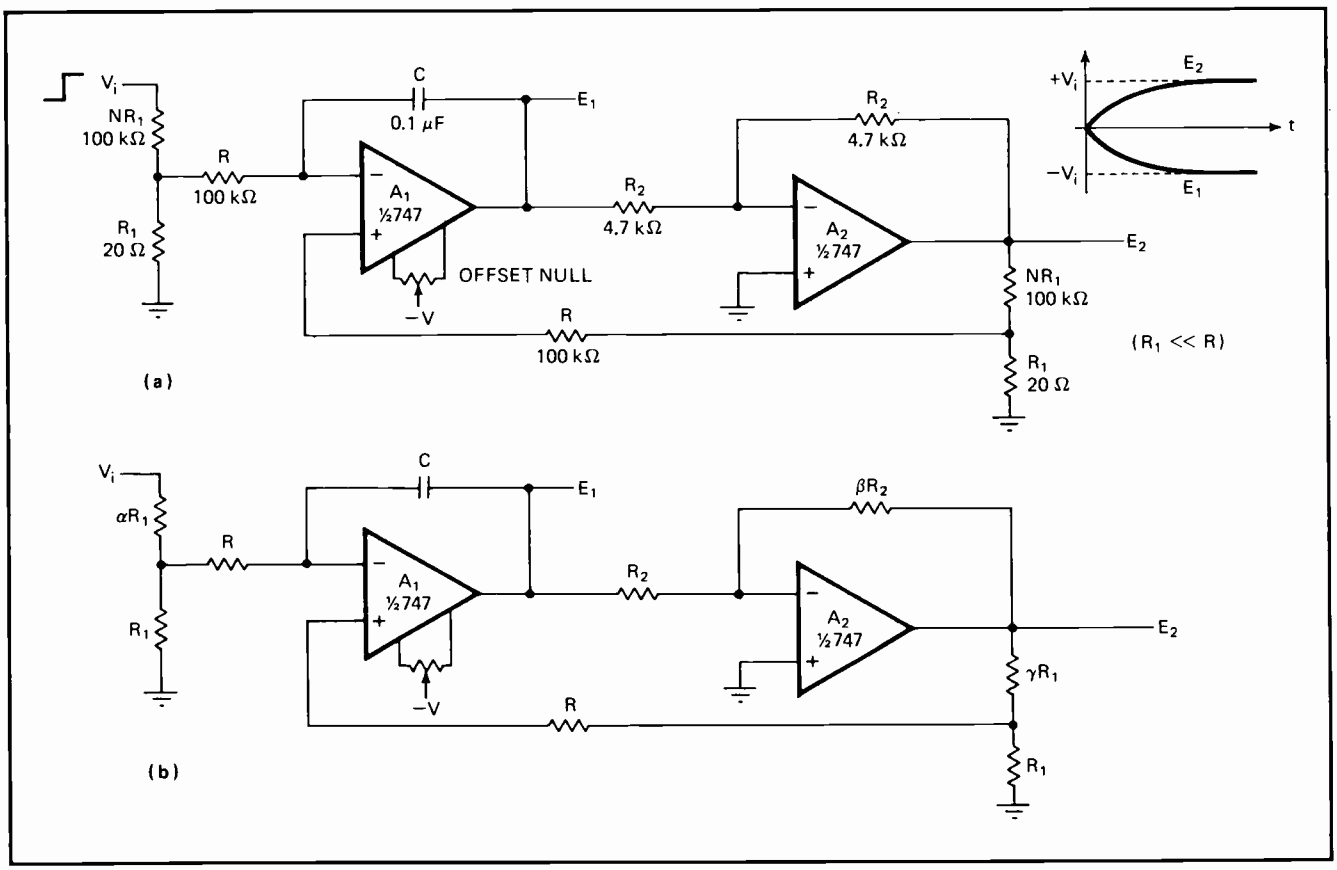
Gains other than plus or minus unity can be obtained at outputs E_1 and E_2 by making the input attenuation and feedback ratios unequal; they are both $1/(N+1)$ for circuit (a). Also, the inverting gain of amplifier A_2 can be other than unity. As shown in circuit (b), input attenuation can be controlled by ratio α, feedback by ratio γ, and inverting gain by ratio β. The two outputs become:

$$E_1 = -V_i(\gamma+1)[1 - \exp(-t\beta/(\beta+\gamma+1)RC)]/(\alpha+1)\beta$$

$$E_2 = V_i(\gamma+1)[1 - \exp(-t\beta/(\beta+\gamma+1)RC)]/(\alpha+1)$$

In applications where desired drift and noise specifications cannot be met by a 747-type op amp, amplifier A_1 can be stabilized with a temperature-controlled differential preamplifier, such as Fairchild's μA727B. This integrated circuit has an on-chip proportional temperature regulator, affording tight control of chip temperature at about 100°C. The 727-plus-747 combination provides excellent dc stability at high closed-loop gains and can be treated circuitwise as a single op amp. If a preamplifier is added, the null offset trimmer is no longer effective. □

Extending RC time constants. Low-value resistors and capacitors and two op amps can generate time constants that are several minutes long. Output voltages E_1 and E_2 exponentially approach level of step input V_i. Time constant, which is 50 seconds for circuit (a), primarily depends on R, C, and ratio N. For circuit (b), there are three controlling ratios: α for input attenuation, γ for feedback, and β for gain.



One-shot/flip-flop pairs detect frequency bands

by Edward E. Pearson
Opelousas, La.

A retriggerable monostable multivibrator and a type D flip-flop can form a simple reliable frequency comparator that senses if an input frequency is greater than or less than a predetermined reference. Connecting additional comparators in parallel, together with AND logic, permits the detection of input frequencies that fall within selected bands.

Both the one-shot and the flip-flop are wired for positive edge triggering. Each input pulse causes the monostable's output to go high for the period of its preset timing interval. The flip-flop is triggered simultaneously, but its output is determined by the state of its D input at the time of trigger threshold.

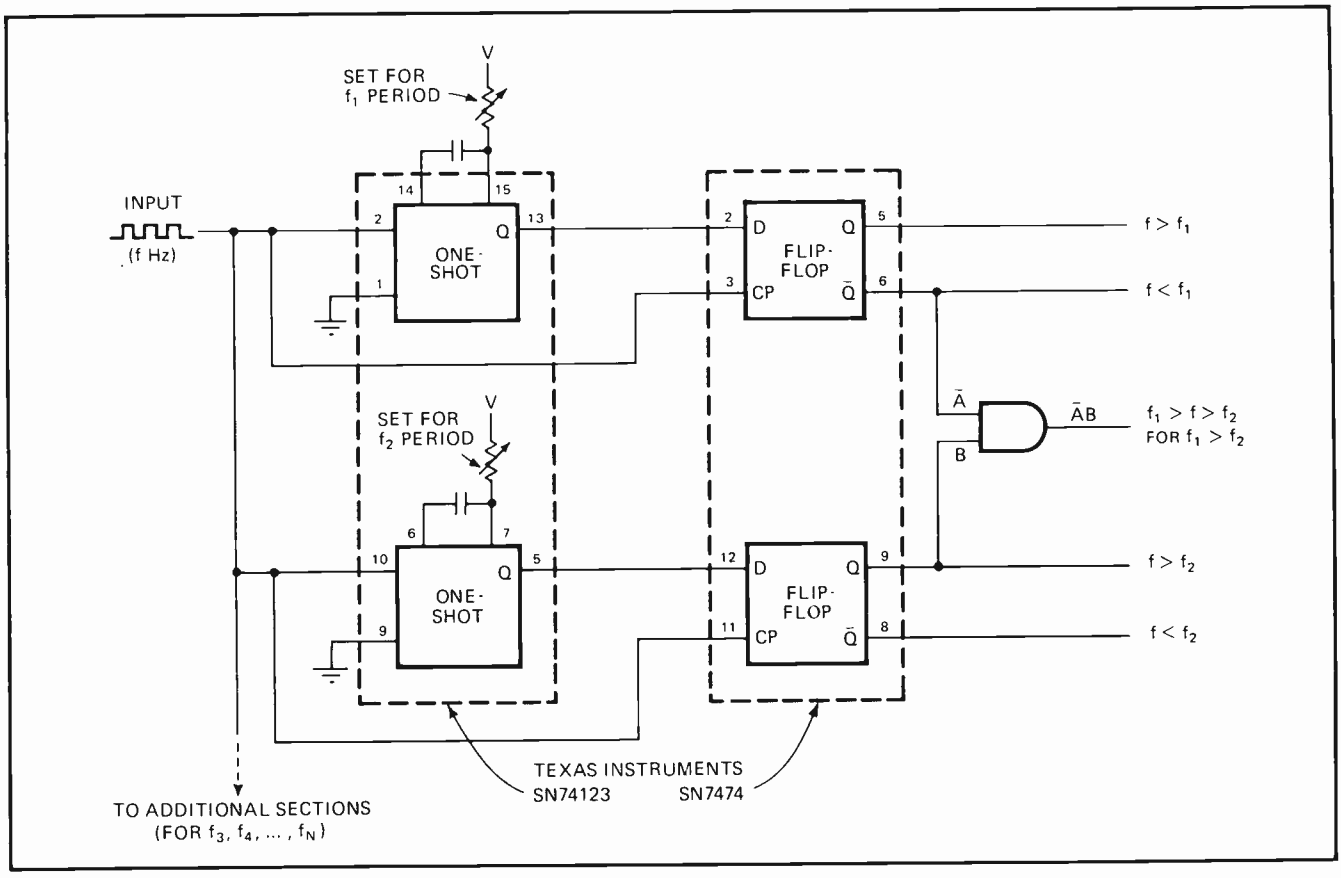
If the period of the input frequency is shorter than the preset timing of the monostable, a constant high level will be present at the D input, forcing the flip-flop's Q output to remain high. If the input frequency period becomes greater than that of the monostable, the D input will go low prior to the next incoming trigger. The flip-flop's Q output then goes low and remains low until the input period becomes shorter than that of the monostable.

To determine whether an input frequency (f) falls between two known frequencies, f_1 and f_2, two one-shot/flip-flop combinations are required, as shown. The top pair of devices detects an input greater or less than f_1, while the bottom pair detects an input greater or less than f_2. The AND gate provides a high output when the input frequency lies inside the preset band (less than f_1 or greater than f_2, if f_1 is greater than f_2). This detection scheme can be expanded to include any desired number of segments within the operating passband.

The frequency band detector also has an inherent memory function that could be particularly useful in control applications. When the input signal terminates, for example, with a tone burst, no trigger is available to the flip-flops, and all outputs remain static until the input signal returns.

Although the detector responds only to the period of the input signal and does not require the input to maintain a specific duty cycle, input pulses must have a rapid rise time. All trigger thresholds must be reached within an interval that is appreciably less than the monostable's propagation delay time. Circuit speed is limited only by the setup and hold performance of the components being used. □

Sensing frequency. Retriggerable one-shot and flip-flop compare frequency of input to preset reference frequency. To form frequency-band detector, two frequency comparators and AND gate are needed. Depending on period of input pulse train, each one-shot output is high or low. Each flip-flop triggers to level seen by its D input prior to trigger threshold. AND gate output goes high when f falls between f_1 and f_2.



Control one-shot divides frequency by up to 30

by Jerome Snaper
Leach Corp., Controls Div., Azusa, Calif.

A three-gate control allows precision frequency divisions of up to 30 merely by changing a resistance. A crystal oscillator acts as the frequency source so that all subharmonics of the reference frequency have crystal stability.

NAND gates G_1 and G_2 and the crystal comprise the oscillator that generates the reference frequency. The one-shot, consisting of NAND gates G_3 and G_4, controls gate G_5, which is synchronized by the oscillator.

After one pulse of the reference frequency passes to the output, the one-shot locks out gate G_5 for a period of time determined by the setting of potentiometer R_t. When the one-shot resets, another single pulse reaches the output, and the cycle repeats.

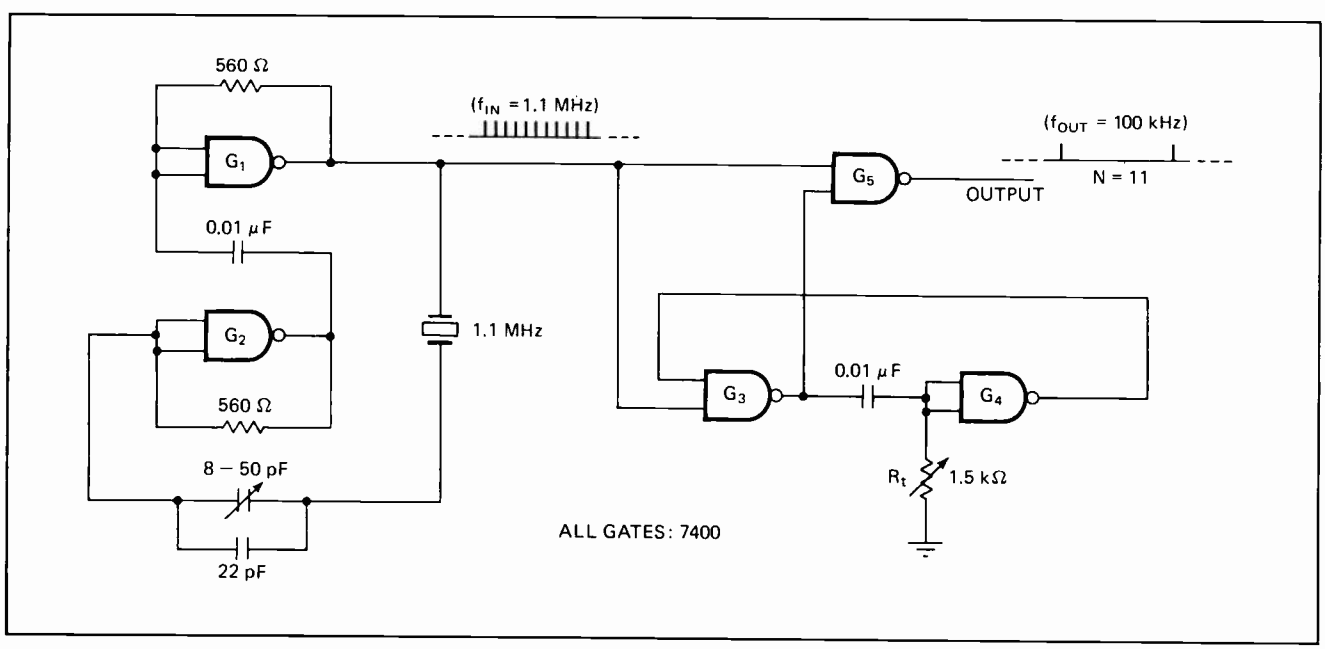
The input frequency, f_{in}, is simply a multiple of the output frequency, f_{out}:

$$f_{in} = Nf_{out}$$

where N is the division factor. N can have any integral value between 2 and 30. The circuit shown divides a 1.1-megahertz reference frequency by 11 to yield an output frequency of 100 kilohertz.

Additional versatility is possible by substituting a field-effect transistor or voltage-variable resistor for the potentiometer. Then, frequency divisions can be electronically swept over a wide range. □

Precision division. Crystal oscillator supplies reference frequency for three-gate divider scheme. NAND gates G_3 and G_4 form one-shot that controls gate G_5. After G_5 passes single reference pulse, one-shot inhibits this gate for period selected by adjustment of potentiometer R_t. When one-shot resets, another reference pulse passes to output. Crystal frequency can be divided by up to 30 without loss of stability.



Pulsed standby battery saves MOS memory data

by K. C. Herrick
Fisher Berkeley Corp., Emeryville, Calif.

A simple pulsed battery supply can reduce standby power necessary for MOS random-access memories to one-thousandth of the operational requirement. In many systems, this power-saving scheme allows inexpensive batteries to be used with essentially shelf-life longevity. In some cases, merely a capacitor can supply enough standby power to sustain memory until an auxiliary power source can come on-line.

A typical RAM cell consists of a cross-coupled multivibrator with active MOS transistor loads. When there is a power failure, the potential across the multivibrator declines toward zero. As long as its inputs are kept off, the cell is isolated from external influence, except for

leakages, when the MOS transistors cease conducting.

The charges remaining on the gates of the cross-coupled transistors then begin to leak off exponentially. If power is reapplied within a short period of time, however, sufficient differential charge levels remain on the gates to re-establish flip-flop conduction in the same state as when power failed.

It is this cell characteristic that can be exploited to save standby power. The potential across the multivibrator must be reapplied periodically, at a rate fast enough to replenish the MOS gate charges before they decline below threshold levels and for long enough to re-establish fully the charge levels. Usually, a sufficient rate is 1,000 hertz with a pulse width of 1 microsecond. For any given type of memory and upper temperature limit (leakages increase with temperature), the required duty cycle may vary.

Of course, the potential needed must be reapplied within the maximum period of time that is allowable (for example, 1 millisecond). The little-used series multivibrator and a 14-volt battery (a) will do the job. The nominal memory cell potential is 15 V, less one diode drop, or about 14.3 V.

When power fails, diode D_1 disconnects the RAM's V_{DD} line from the main supply. The memory potential of $V_{CC} - V_{DD}$ declines in magnitude until the voltage of $14 - (V_{CC} - V_{DD})$ is large enough to start the series multivibrator. Oscillations usually begin when the voltage across the multivibrator becomes about 0.75 V. The components shown yield a pulse width of about 1 μs and a pulse interval of about 500 μs.

If a rechargeable battery is used, the diode and resistor connected with dashed lines may be added to allow the battery to charge while the main power is applied. The memory's peripheral-circuit supply voltage V_D can become zero and remain zero during the loss of main power, without any effect on data retention.

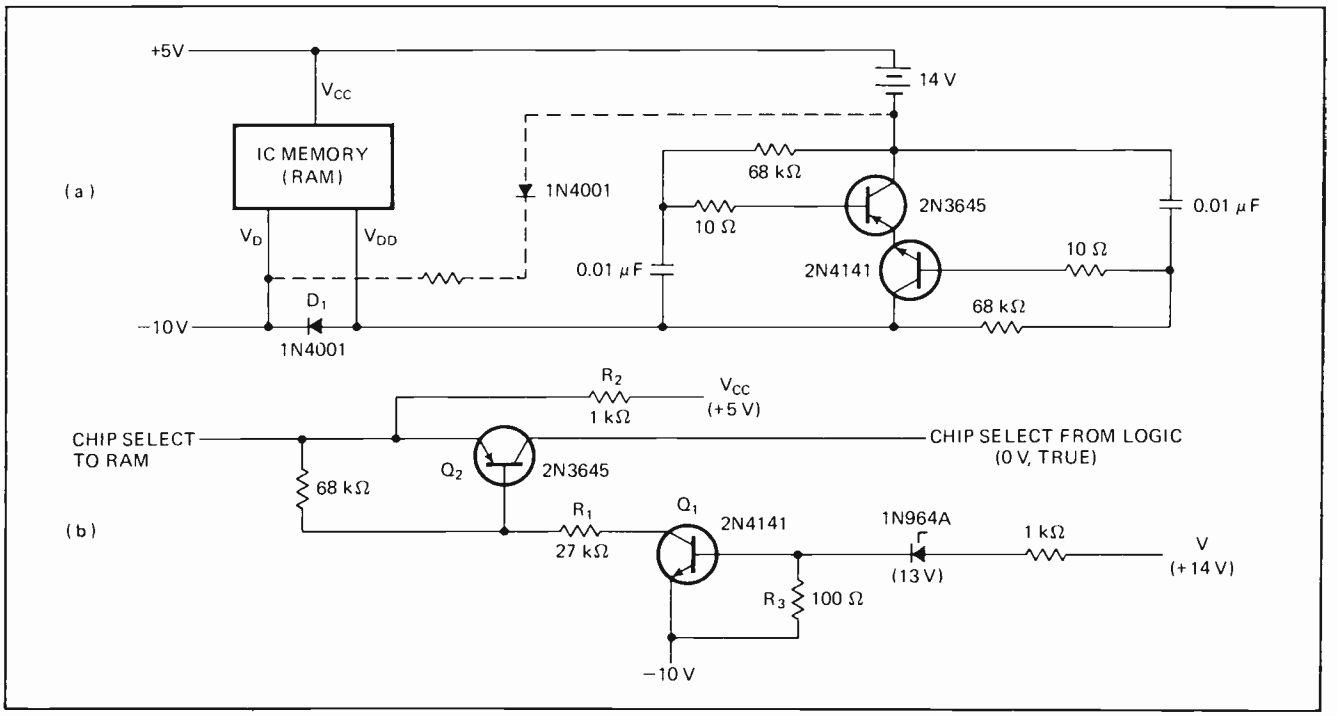
While the memory supply voltage is decreasing, the memory's chip-select input must be held FALSE at the V_{CC} (+5 V) potential. TTL devices or other elements driving this line may change state erratically when the 5-V logic supply loses voltage. The presence of these stray signals may cause a RAM cell to change state.

A circuit for maintaining the chip-select line at the instantaneous V_{CC} level is shown in (b). Since the 14-V (in this case) semi-regulated supply is the power source for the 5-V regulated logic supply, in the event of power failure the 14-V source will lose voltage before the logic supply.

Transistor Q_1 is normally kept on by base current from the 14-V supply via zener diode D_1. Collector current from Q_1 biases Q_2 on. Base current from Q_2 causes only a negligible drop below 5 V in the FALSE voltage level of the memory chip-select line, due to the high resistance ratio of R_1 to R_2. Whenever a zero chip-select voltage is applied to Q_2's collector from the control logic, Q_2 conducts, and its emitter voltage changes to the TRUE level (O V).

Upon power failure, the 14-V and 10-V supplies begin to lose voltage. Transistor Q_1's base current will become zero when resistor R_3's voltage drops below about 0.7 V. At this time, voltage V equals 10.7 V—20.7 V above −10 V or 5.7 V more positive than V_{CC}—a value that still maintains the 5-V V_{CC} level. When Q_1 stops conducting, Q_2 is cut off, and the memory's chip-select input line is connected only to V_{CC} via resistor R_2. Therefore, even if V_{CC} decreases in value, the chip-select line remains at the V_{CC} potential. □

Preserving memory contents. Series multivibrator and battery (a) allow MOS random-access memory to retain data when power fails. Circuit takes advantage of MOS charge retention property so that pulsed voltage is sufficient to refresh memory. Dashed components let battery recharge when main power is restored. Protection circuit (b) for chip-select line prevents erratic logic signals from changing memory state.



Triangular-wave generator spans eight decades

by William S. Shaw
University of Texas, Applied Research Laboratories, Austin, Texas.

Because of its nonsaturating design, a triangular-wave generator can cover eight decades of frequency—from 0.01 hertz to 2 megahertz. Lower and upper frequency limits are set by resistance adjustment. Circuit layout is not critical, and complementary circuitry assures output symmetry and amplitude stability, as well as the absence of dc offset. By decreasing output voltage swing and increasing current, the generator's frequency range can be made to span 1 to 20 MHz.

Transistors Q_1 and Q_2 are constant-current sources whose outputs are switched to produce the charging and discharging currents for the output capacitor. Transistor pairs Q_3-Q_4 and Q_5-Q_6 are differential amplifiers that function as comparators; Q_3 and Q_6 conduct whenever Q_4 and Q_5 switch off, and vice versa.

The series string of diodes D_1 and D_2 and resistors R_1, R_2, R_3, and R_4 set comparator voltages V_1 and V_2. Diodes D_1 through D_4 compensate the four-transistor integrated-circuit array so that the generator maintains its frequency stability with changing temperature. Comparator input and output currents are:

$$i_1 = 28.7R_1/(R_1+R_2+R_3+R_4)R_5$$

$$i_2 = R_7 i_1/R_6$$

When Q_4 and Q_5 are on, Q_3 and Q_6 are off, and output capacitor C_1 charges at a constant rate (since i_2 is a constant) until the upper trigger level (V_U) is reached:

$$V_U = V_{E1} + V_{BE1} + V_{D5}$$

where V_{E1} is the voltage at Q_1's emitter, V_{BE1} is Q_1's base-emitter voltage, and V_{D5} is the voltage across diode D_5. Once output voltage equals V_U, transistor Q_1 conducts and Q_2 switches off, turning Q_3 and Q_6 on. Since R_7 is larger than R_6, Q_4 and Q_5 will switch off.

Due to the symmetry of the circuit, capacitor C_1 is discharged by transistor Q_6 at the same constant rate as it was charged and by the same current, i_2. The capacitor discharges to the lower trigger level (V_L):

$$V_L = V_{E2} - V_{BE2} - V_{D6}$$

where V_{E2} is Q_2's emitter voltage, V_{BE2} is Q_2's base-emitter voltage, and V_{D6} is the voltage across diode D_6. When V_L is reached, Q_1 turns off, Q_2 turns on, and V_2 becomes larger than V_4. This switches on Q_4 and Q_5, causing Q_3 and Q_6 to switch off by feedback through capacitor C_2. The cycle can now repeat.

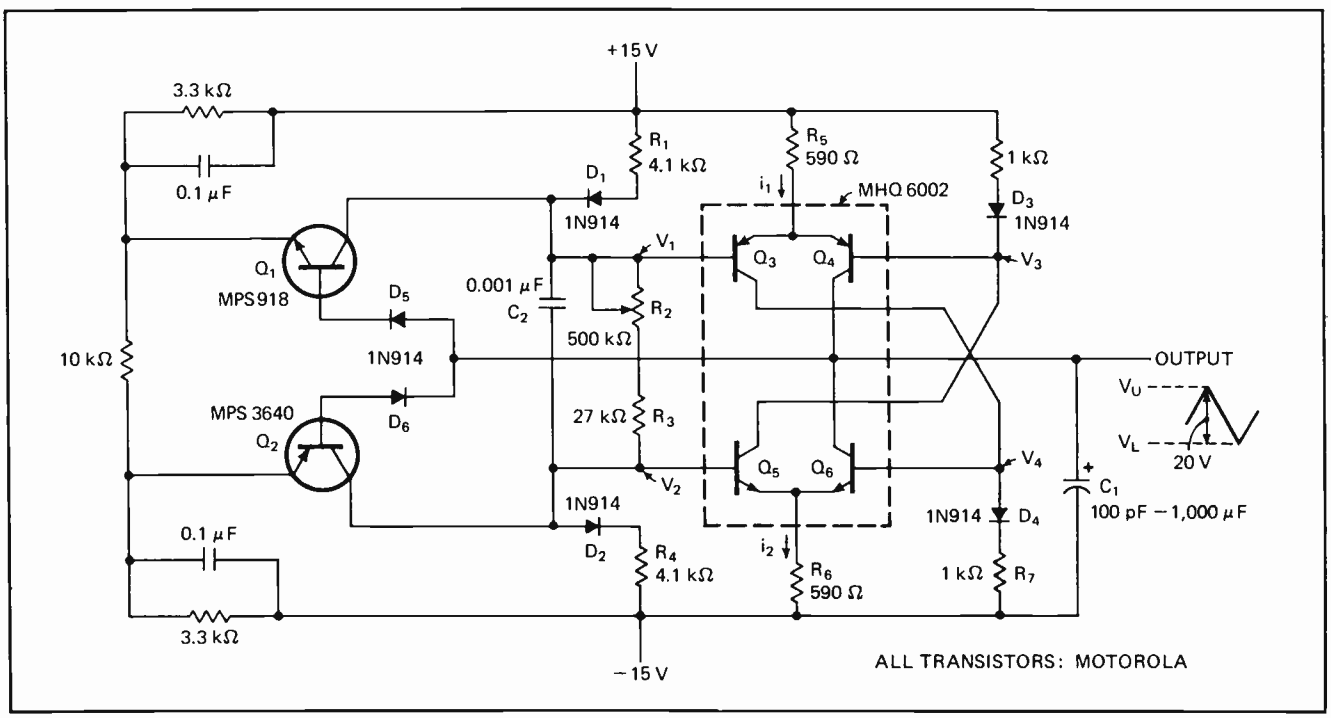
Diodes D_5 and D_6 allow the output to slew above and below the limits imposed by the emitter-base breakdown voltage (about 6 V) of Q_1 and Q_2. The generator will oscillate without latch-up as long as V_{E1} is less than V_1 and V_{E2} is greater than V_2.

For a 20-V peak-to-peak output, the frequency is:

$$f_{out} = 0.0425 i_1/C_1$$

Capacitor C_1 determines nominal output frequency, while resistor R_3 sets the lower frequency limit and potentiometer R_2 sets the upper limit in addition to providing a linear frequency span of 20:1. When R_2 = 500 kilohms and C_1 = 1,000 microfarads, f_{out} = 0.01 Hz; when R_2 = 0 and C_1 = 100 picofarads, f_{out} = 2 MHz. □

High-frequency triangles. Complementary nonsaturating circuitry permits triangular-wave generator to provide 20-volt output at frequencies as high as 2 megahertz. Output triangle is obtained by charging and discharging C_1. Current from Q_2 charges C_1 until output voltage reaches threshold V_U, then Q_3-Q_4 and Q_5-Q_6 comparators switch, and Q_1 supplies discharge current until threshold V_L is reached.



Output comparator enhances versatility of one-shot

by Harvey J. Scherr*
Westinghouse Corp., Systems Development Div., Baltimore, Md.

If an operational amplifier is used as an output comparator, a monostable multivibrator can provide wide and accurate output pulses over a broad temperature range. The one-shot is also retriggerable—that is, its output pulse duration can be extended by reapplying the input pulse. In addition, this multivibrator can be reset to accept a new trigger input within its timing period.

Each time an input pulse occurs, timing capacitor C_t is discharged by field-effect transistor Q_1, and comparator A_1 switches off. In the absence of a trigger input, C_t accepts charge from Q_1, and the comparator is turned on. Switching takes place when A_1's input voltages, e_1 and e_2, are equal. Because the comparator is off during the timing interval, there are no output errors introduced by op-amp input offset current.

Output pulse width, T, is determined by the supply voltage, V_{DD}, reference voltage, V_R, and the timing components, R_t and C_t. At the comparator's input:

$$e_1 = e_2 = V_{DD}\exp(-t/R_tC_t)$$

which can be rewritten as:

$$\exp(-t/R_tC_t) = V_{DD}/e_1 = V_{DD}/[V_RR_2/(R_1+R_2)]$$

Output pulse width becomes:

$$T = R_tC_t[\ln(V_{DD}) - \ln(V_RR_2/(R_1+R_2))]$$

If $V_{DD} = V_R$ and $R_1 = R_2$, this equation reduces to:

$$T = R_tC_t\ln(2) = 0.694R_tC_t$$

The timing equations illustrate that output pulse width is completely independent of any transistor junction voltage and therefore is independent of junction temperature dependence. Op-amp offset voltage drift principally determines the one-shot's temperature performance. And since offset drift is typically as low as 10 microvolts/°C, total variation in the multivibrator's timing interval is only about 0.002%/°C.

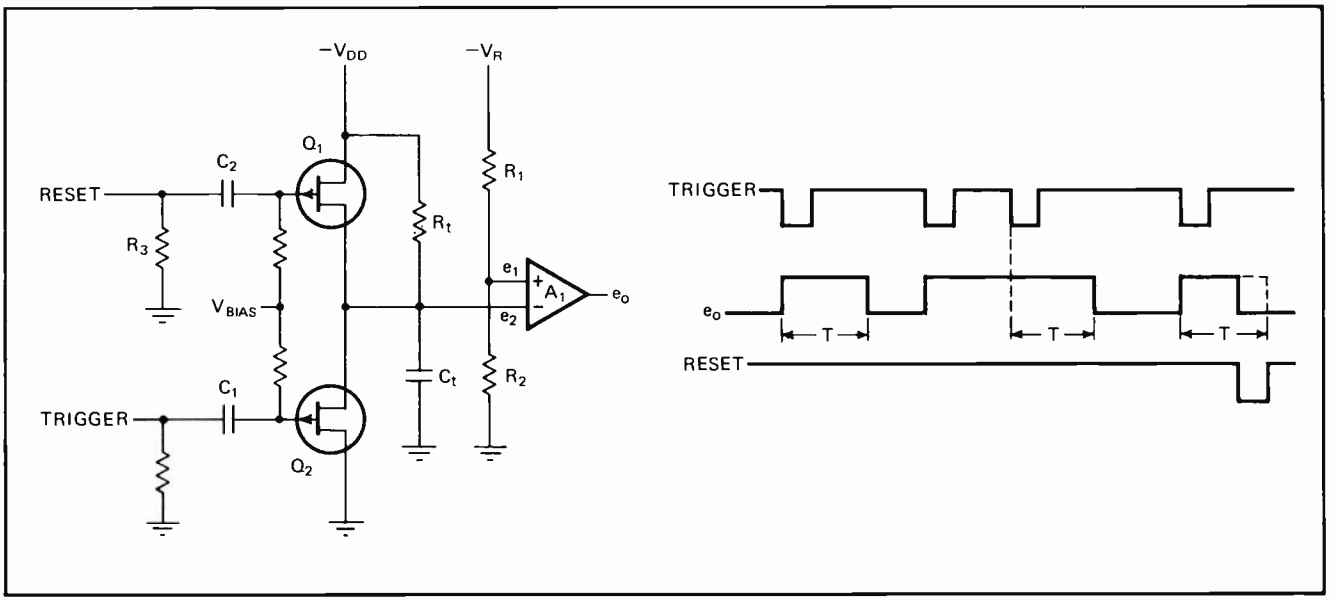
Unusually large time constants can be achieved because the primary restriction on the value of timing resistor R_t is op-amp bias current. R_t must be small enough to allow the voltage developed at A_1's inverting input to turn the comparator on. Since op-amp bias current generally ranges between 0.25 and 0.5 microamperes, resistor R_t can be as large as 10 megohms (when V_{DD} = 10 volts and e_1 = −5 V).

As illustrated in the timing diagram, the multivibrator can be re-initiated during its timing interval to stretch output pulse width. This is possible because transistor Q_1 discharges capacitor C_t every time an input pulse occurs. By adding transistor Q_2, capacitor C_1, and resistor R_3, the circuit can be reset by restoring it to its stable state. A fixed-width reset pulse cancels the remaining portion of the output pulse.

Substituting a resistor for capacitor C_2 alters the multivibrator's timing—a time out then occurs with the absence of a negative voltage from the input terminal. Circuit output polarity is easily reversed by interchanging the connections to the comparator's inverting and noninverting inputs. The active devices used determine component values. □

*Now with Stereo Equipment Sales Inc., Baltimore, Md.

Retriggerable monostable. Input trigger causes Q_1 to discharge capacitor C_t, turning off comparator A_1 and producing output. Before timing period is over, new trigger can be applied to extend output duration. Reset pulse through Q_2 can terminate output during any part of timing interval. Output comparator maintains one-shot temperature stability and permits unusually large time constant to be used.



Series resistance improves potentiometer linearity

by Harry H. Schwartz
Electrodesign Ltd., Ville Lasalle, Québec, Canada

Adding a series resistance to one end of a loaded linear potentiometer can reduce loading error by a factor of five or more. The price for this gain in linearity is a voltage loss across the pot. But losses in amplification or drive in the order of 3 to 4 decibels can usually be tolerated in view of the marked improvement in linearity.

As shown in (a), voltage E_i is applied to potentiometer R_p and series resistor R_s. The load resistor is R_m, the output voltage is E_o, and θ is the per-unit variation of the pot wiper. Letting:

$Y_\theta = E_o/E_i$, $P_m = R_m/R_p$, and $P_s = R_s/R_p$

the voltage transfer function can be expressed as:

$$Y_\theta = \theta P_m/(P_m P_s + P_m + \theta P_s + \theta - \theta^2)$$

If $Y_0 = Y_\theta$ when $\theta = 0$ and $Y_1 = Y_\theta$ when $\theta = 1$, then output impedance ratio Z_o is:

$$Z_o = Y_\theta/Y_1 = \theta/[1 - (1-\theta)(P_s - \theta)/(P_m + P_s + P_m P_s)]$$

For three points of this equation, the values of Z_o and θ are the same; or, since there is no linearity error, then $Z_o = \theta$. These points occur at $\theta = 0$, $\theta = 1$, and $\theta = P_s$.

The well-known curve (b) for a loaded potentiometer can be written in terms of θ and P_m:

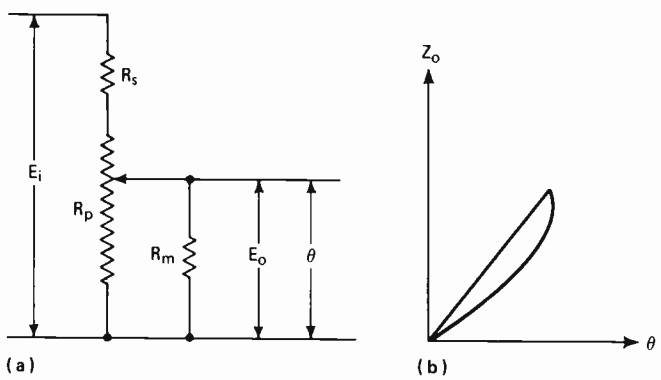
$$Z_o = \theta/[1 + \theta(1-\theta)/P_m]$$

When the load resistance is very high, P_m approaches infinity, and the pot output is the straight black line. For finite values of P_m, the nonlinear colored curve is obtained. As P_m becomes smaller, linearity error grows.

A short computer program (c) that solves the general equation for impedance ratio Z_o can be used to determine the effect of series resistance ratio P_s for various values of load resistance ratio P_m. Generally, the larger the magnitude of P_s, the greater is the error reduction. The program varies P_s from 0 to 2 in steps of 0.1 and θ from 0 to 1 in steps of 0.05 for P_m values of 1, 2, 5, 10, 20, and 50.

The plot of (d) shows that output linearity for $P_m = 1$ is improved by a factor of five when P_s is increased from 0 to 0.6. In (e), linearity error is plotted against θ for $P_m = 5$ and $P_m = 10$ for P_s values between 0 and 0.6. Again, linearity is greatly improved. Values of P_s should be held to 0.5 or less so that the series voltage loss is tolerable. □

Reducing loading effects. Output of loaded potentiometer (a) becomes nonlinear, as shown by graph (b), with smaller load resistance ratio ($P_m = R_m/R_p$). Increasing series resistance ratio ($P_s = R_s/R_p$) decreases loading error and improves linearity. Computer program (c) finds output impedance ratio Z_o for several values of P_m, P_s, and wiper position θ. Graphs (d) and (e) show effect of P_s on Z_o and linearity error.

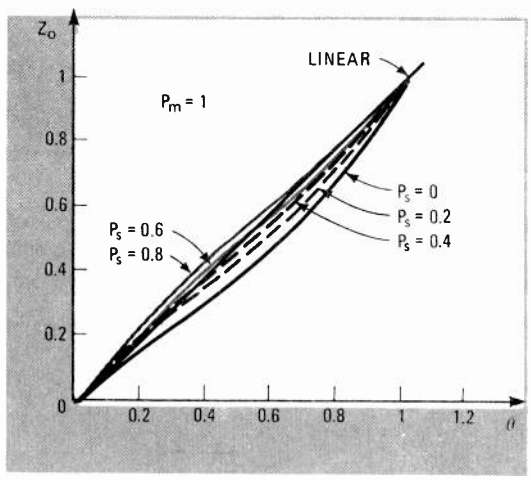


(a)

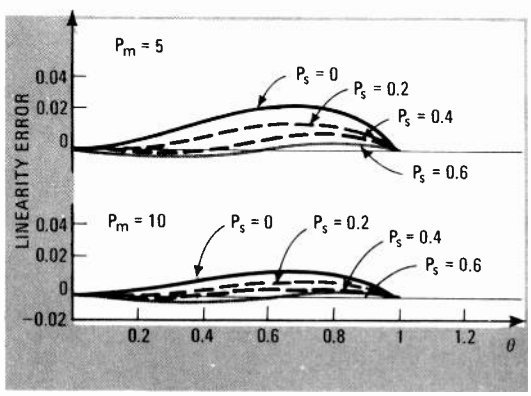
(b)

```
READY
PLIST
10    DATA 1, 2, 5, 10, 20, 50
30    READ P1
40    FOR P2=0 TO 2 STEP .1
45    PRINT " PM="P1," PS="P2
46    PRINT
47    PRINT " A","Z"
48    PRINT
50    FOR A=0 TO 1 STEP 5.00000E-02
60    LET Z=A/(1-((1-A)*(P2-A))/(P1 + P2 + P1 * P2))
70    PRINT A, Z
80    NEXT A
85    PRINT
86    PRINT
90    NEXT P2
95    PRINT
96    PRINT
100   GOTO 30
110   END
READY
RUN
```

(c)



(d)



(e)

Circumventing BCD addition in digital phase-locked loops

by Larry Martin
Hewlett-Packard Co., Palo Alto, Calif.

Many of the applications for a digital divide-by-N phase-locked loop require the locked oscillator to be offset by a fixed frequency. Usually, the first stage of the programable binary-coded-decimal divider circuit adds the input frequency to the desired offset frequency. This BCD addition, however, can be eliminated by detecting the proper number at the output of the counter divider chain.

If a receiver is tuned to 118.15 megahertz, and its intermediate-frequency stage is at 10.7 MHz, the local oscillator must then operate at 128.85 MHz. A standard divide-by-N circuit (a) adds the i-f frequency to the input frequency, takes the BCD nines complement of the sum, and then loads the result into a programable counter divider chain. Detection occurs when the counter outputs are all nines. The input number is then reloaded on the next clock pulse and the process repeats.

Let N be the input number; in this case, N = 11815 and the desired offset is 1070. The number at the outputs of the BCD adders is N + 1070, which becomes 19999 -(N + 1070) at the outputs of the complementing circuits. Therefore, the number of counts that occurs before the divider resets is the divider state that is sensed. Or, the input frequency is divided by:

19999 -[19999 -(N + 1070] = N + 1070

which can be rewritten as:

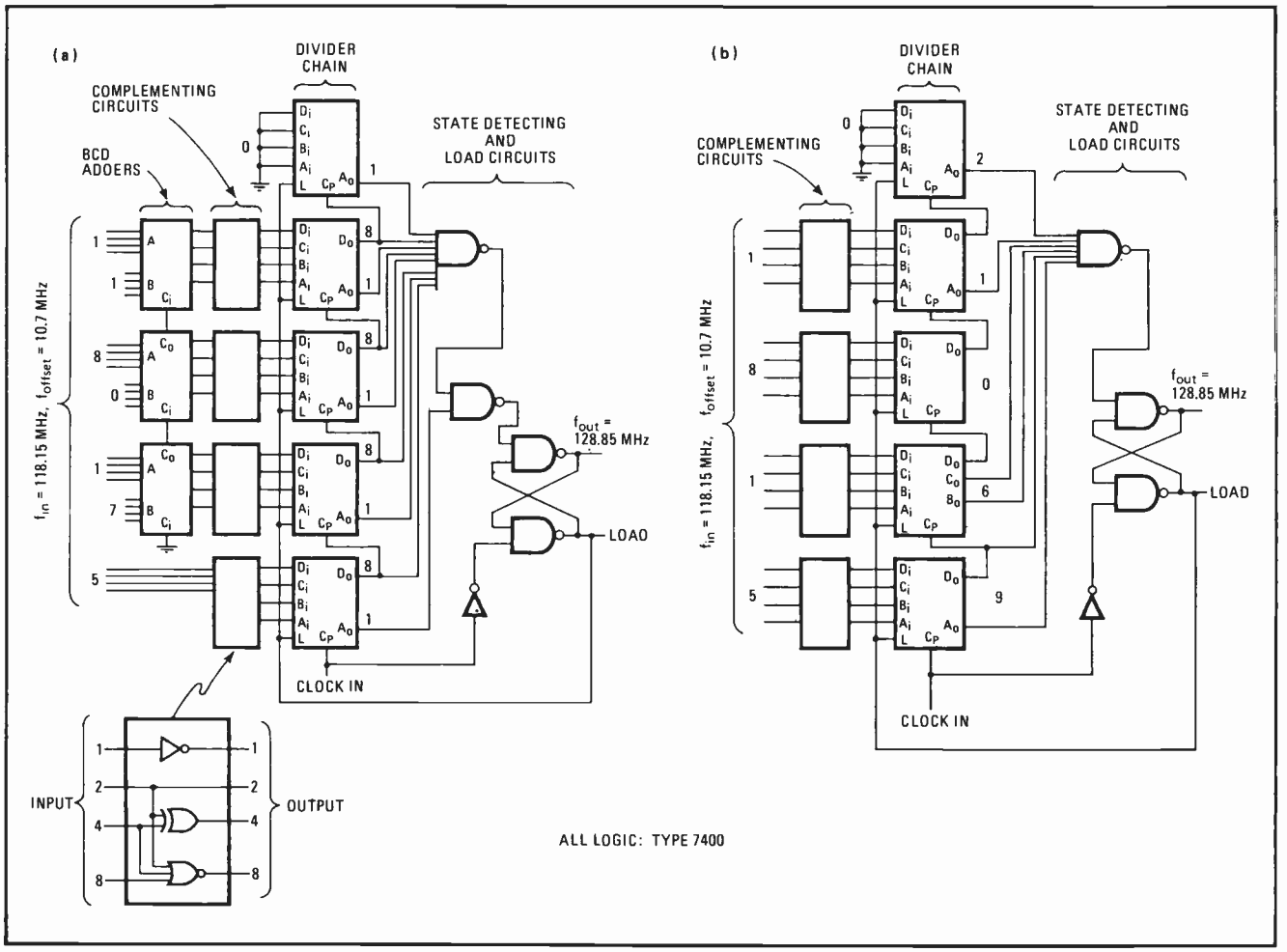
19999 + 1070 -(19999 - N) = N + 1070, or

21069 -(19999 - N) = N + 1070

By counting to 21069, instead of 19999, the proper number of counts still occurs before the divider resets. The BCD adders, then, can be removed simply by detecting a different output state of the counter, as shown in (b).

Since the divider is an up-counter, detection of the desired output state should be done when the proper outputs are ones. Because there are only six ones in 21069, as opposed to nine in 19999, one fewer output gate is needed. □

Frequency offsetting. Standard divide-by-N circuit (a) sums input frequency (118.15 MHz) with offset frequency (10.7 MHz), takes nines complement of sum, and then detects signal when counter outputs are all nines. BCD adders and one output gate can be omitted, as in (b), by detecting sum of nines complement and offset frequency (19999 + 1070 = 21069). Correct count is still reached before divider resets



Thumbwheel switches set synthesizer output frequency

by Jerrold L. Foote
University of Utah College of Medicine, Salt Lake City, Utah

Two binary-coded thumbwheel switches can set the output of a two-decade frequency synthesizer that includes the two switches, a single crystal oscillator, and two decade counters. Synthesizer output accuracy and long-term frequency stability are the same as that of the crystal used as the reference frequency source. Whatever pulse-to-pulse time variation occurs is minimized to an acceptable level by a chain of binary counters.

The synthesis technique involves generating a series of pulses and blank spaces, divided by as many binary counters (N) as needed to yield the desired output frequency (f_o). The frequency-selection circuit consists of thumbwheel switches, S_1 and S_2, two banks of diodes and their corresponding decade counters, and a flip-flop formed by gates G_1 and G_2. More decades of frequency control can be added easily.

The number of oscillator pulses passed by the flip-flop-controlled NOR gate, G_3, is determined by the thumbwheel switch setting (S). Blank spaces occur while the decade counters are counting beyond the switch setting. When these counters reach their maximum count (M), the flip-flop resets, and the oscillator pulses pass through gate G_3 to the binary countdown string. The output frequency is given by:

$$f_o = f_i S/MN$$

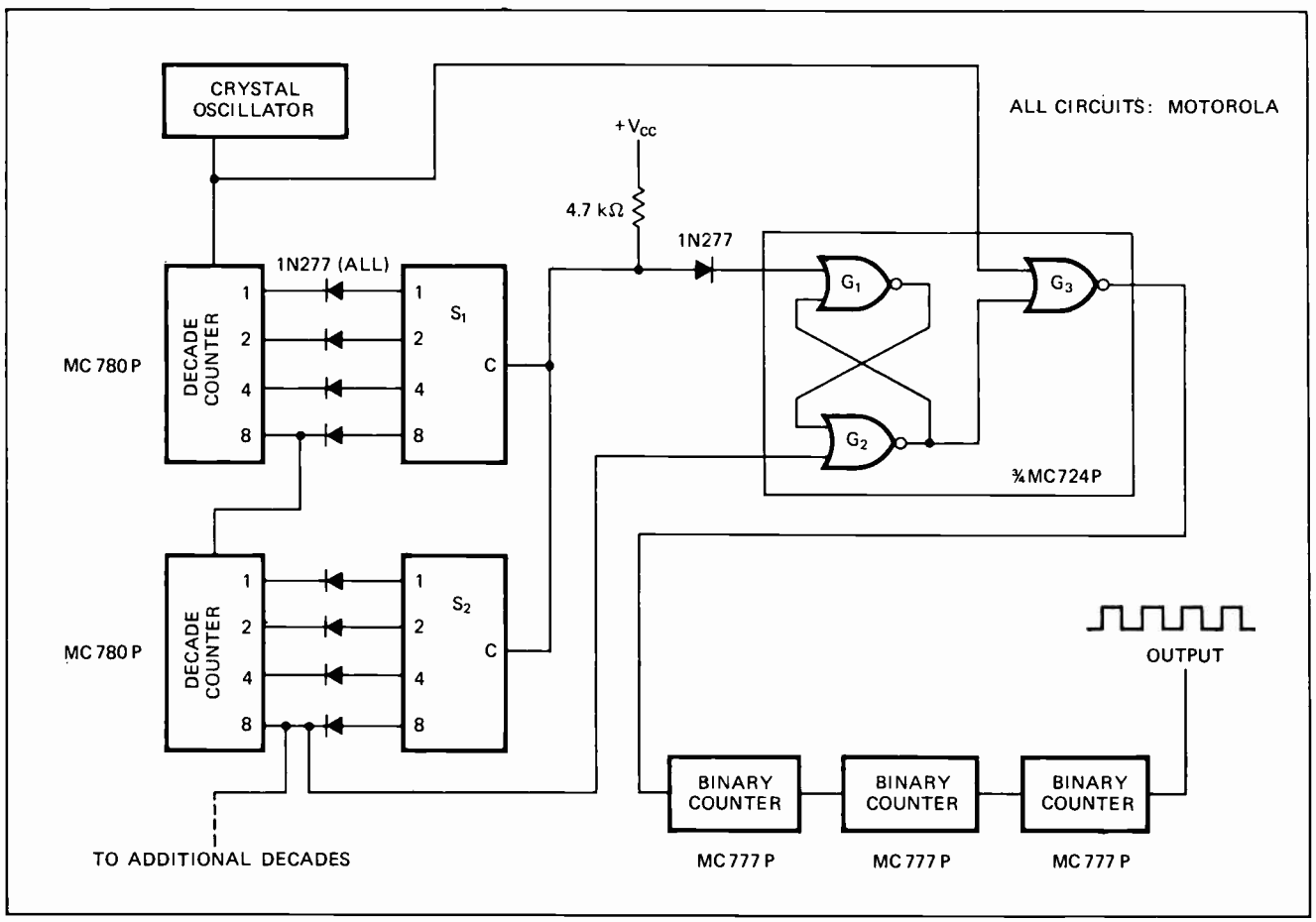
where f_i is the crystal frequency.

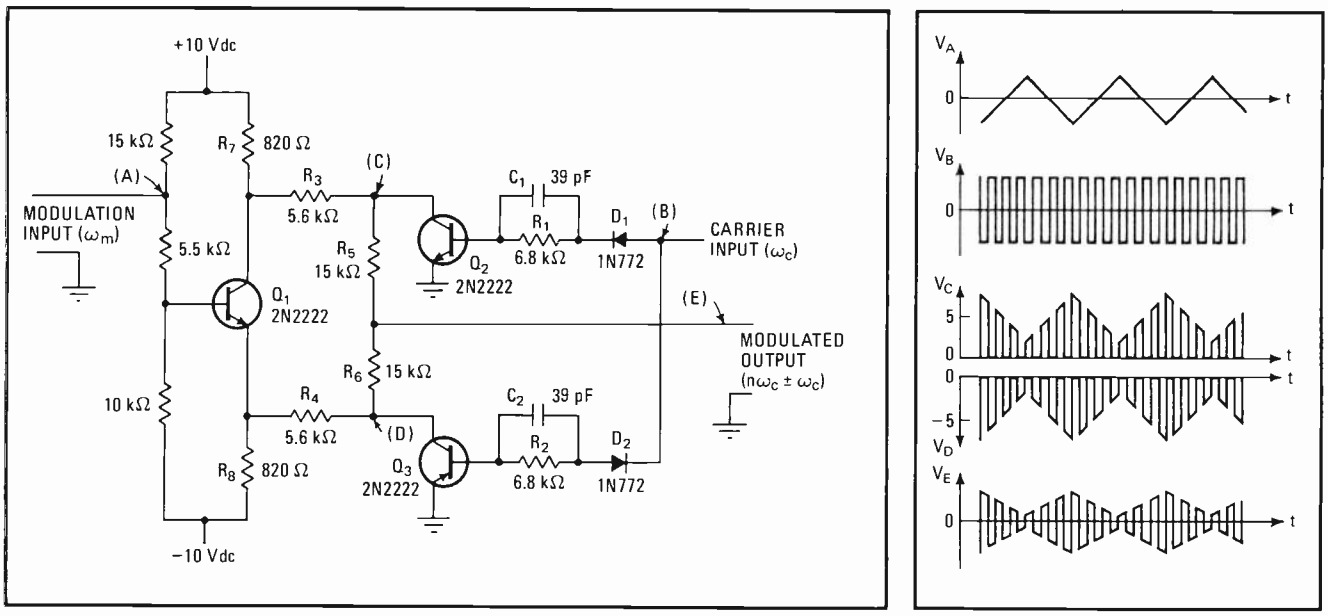
The output of gate G_3 is a train of pulses and blank spaces that must be time-averaged to reduce the pulse-to-pulse time variation (ΔT) in the output frequency. This time-averaging is performed by the binary countdown string. The closer the tolerance that must be held on ΔT, the larger is the number of binary counters required. Maximum pulse-to-pulse time variation is:

$$\Delta T = S/f_o N$$

Crystal frequency can be as high as 10 megahertz. □

Dialing frequency. Thumbwheel switches determine number of output decades for frequency synthesizer. Single crystal oscillator serves as frequency source. Decade counters generate pulse train that is divided by binary counter chain to obtain frequency set by switches. When switch-fixed decade count is reached, flip-flop formed by gates G_1 and G_2 resets, enabling gate G_3 so that pulses pass to binary counters.





Splitting and chopping. Highly linear amplitude modulator theoretically can operate at half the carrier frequency. Transistor Q_1 splits modulation input into two equal signals that are opposite in polarity and phase. Switch Q_2 passes positive half-cycles of square-wave carrier, while switch Q_3 passes negative half cycles. Chopped modulated signals (points C and D) are then summed by resistors R_5 and R_6.

Amplitude modulator is highly linear

by Donald DeKold
Santa Fe Junior College, Gainesville, Fla.

Besides offering good linearity, an amplitude-modulation circuit can operate at modulation signal frequencies ranging from dc to half of the carrier frequency. At modulation levels as high as 97.5%, the circuit retains its linearity. All signals are directly coupled without inductive or large capacitive elements.

Transistor Q_1 performs as a phase splitter for the modulation signal, which appears at Q_1's emitter with 0° phase shift and somewhat attenuated from its input level. The dc level of the modulation is approximately −5 V dc at Q_1's emitter and +5 V dc at the collector, where the signal is 180° out of phase with the input.

Transistors Q_2 and Q_3 are high-speed switches, driven alternately from saturation to cutoff by the carrier input. This signal, preferably a square wave, is applied to the bases of Q_2 and Q_3 through resistors R_1 and R_2 and diodes D_1 and D_2, respectively. The diodes protect the transistors from excessive reverse base-emitter voltage generated by possible overdrive from the carrier signal. Capacitors C_1 and C_2 speed up Q_2-Q_3 switching times.

The collectors of Q_2 and Q_3 are coupled to the two outputs of phase-splitter Q_1 through resistors R_3 and R_4. These isolate the modulation frequency portion of the circuit from the carrier frequency portion.

The modulation signal appearing at Q_1's collector is switched from its average 5-V dc level to ground by Q_2 on each positive half-cycle of the carrier. A chopped version of the modulation signal then appears at Q_2's collector. Similarly, the modulation signal at Q_1's emitter is chopped by Q_3; Q_3's cutoff-to-saturation transition occurs at each negative half-cycle of the carrier.

Positive and negative chopped modulation signals are then combined by a simple summing network composed of resistors R_5 and R_6. Signal components of the chopped outputs that occur at modulation frequencies are summed to zero. Therefore, under perfectly balanced conditions, the modulated output is spectrally devoid of modulation-frequency components but, of course, contains the modulation sidebands. Theoretically, this permits modulating to an upper frequency limit of one-half the carrier frequency without troublesome filtering problems. The modulation envelope, in this case, is 180° out of phase with the input modulation signal.

The circuit's output is an amplitude-modulated square wave containing harmonics principally at odd multiples of the carrier frequency. (Spectral content is $n\omega_c \pm \omega_m$, where ω_c = carrier frequency, ω_m = modulation frequency, and n = 1, 3, 5, ...) If a sinusoidal carrier is wanted, the output must be filtered. Since modulation frequency components are absent from the output spectrum, a low-pass filter can be employed to select the fundamental carrier frequency and its sidebands. However, a bandpass filter must be used if the output is to be some multiple of ω_c.

Modulator high-frequency performance depends largely on the speed of the switching transistors. For the transistors shown, useful modulated output extends to 1 megahertz. The modulator itself is essentially flat and linear to 250 kilohertz, with visually apparent distortion occurring in the modulation envelope above this frequency. At a carrier frequency of 100 kHz and modulation frequency of 1 kHz, good linear modulation can be obtained to a modulation depth of 95%.

For a modulation input signal of 14 V peak-to-peak, the maximum modulated output level will be 7.4 V peak-to-peak into an open circuit. The minimum carrier input level for a square-wave drive is 2.8 V peak-to-peak. And overdriving does not produce any unde-

sirable effects. The modulation can be any waveform.

A sine wave can be used as the carrier input, but chopping action will not be as good. Minimum sine-wave drive level is 4 V pk-pk. A linear modulation depth of 97.5% can be obtained at a carrier frequency of 10 kHz and a modulation input level of 14 V pk-pk.

Minimum carrier input drive levels remain essentially unchanged at a lower carrier frequency. Modulator performance, however, degrades somewhat at higher output frequencies—maximum linear modulation becomes only 94% at 500 kHz and 88% at 1 MHz. Output level also drops at higher frequencies, but can be improved by using faster switching transistors and lower impedance levels throughout the circuit.

Higher supply voltages offer an alternate method for improving circuit output level. The saturation voltage of the chopping transistors represents the theoretical limit of maximum modulation depth; this voltage becomes less significant when higher supply levels are used. Furthermore, using precision resistor pairs (R_3-R_4, R_5-R_6, and R_7-R_8) assures that positive and negative peak modulation signals are identical at the output. □

FETs remove transients from audio squelch circuit

by Glen Coers
Texas Instruments Components Group, Dallas, Texas

Using field-effect transistors instead of bipolar transistors for an audio squelch circuit eliminates switching transients without sacrificing switching time. Moreover, because there are no transients, the circuit's frequency response can be as low as desired.

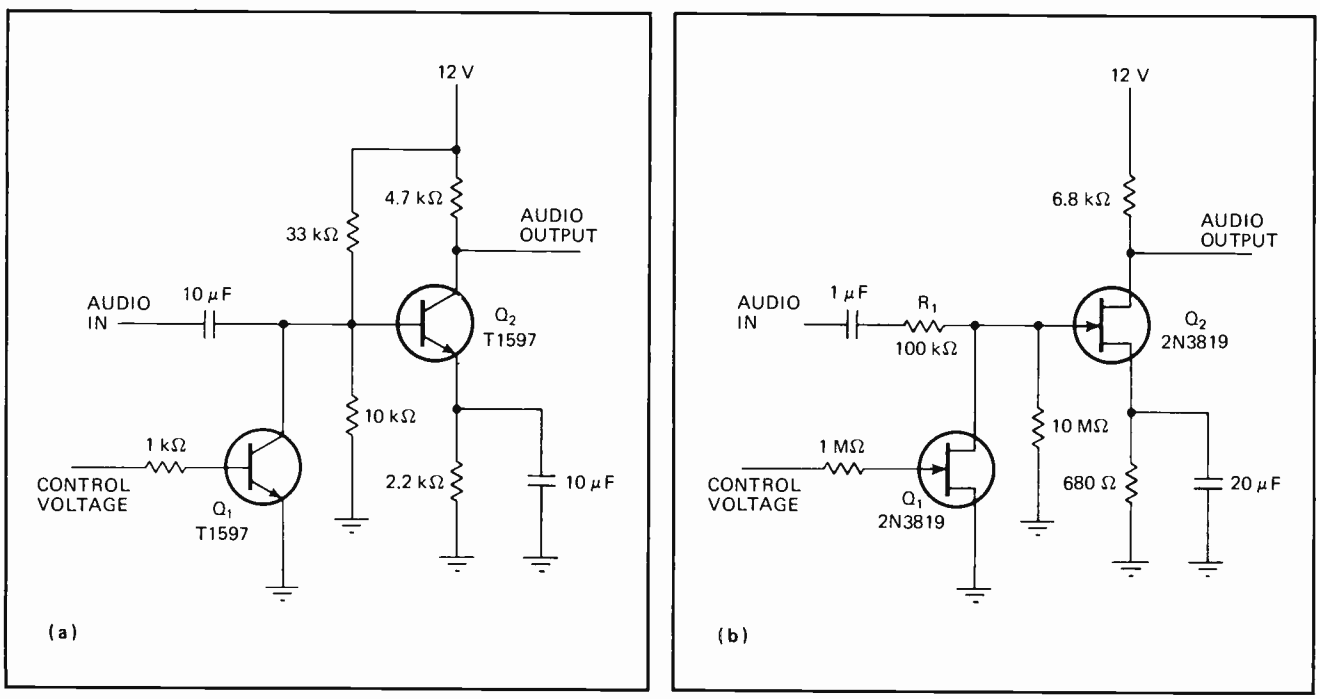
In a typical audio squelch circuit (a), bipolar transistor Q_1 acts as the control device for bipolar transistor Q_2, which serves as the amplifier. When Q_1 turns off Q_2, the base voltage of Q_2 switches from a dc level (in this case, 2.8 volts) to ground, causing a large transient output voltage spike to be generated.

The problem can be minimized by slowing the switching speed of Q_1 or raising the low end of the amplifier's frequency response. However, this method is not practical in applications requiring a broad frequency response, such as high-fidelity audio equipment.

Building the circuit with FETs (b) provides a better solution. Again, transistor Q_1 is the control, while transistor Q_2 is the amplifier. Only ac voltage is present at the gate of Q_2; its dc level is at ground potential so that there is no transient generated when Q_2 is switched off.

When Q_1's gate is at zero volts, the device itself conducts, bypassing the audio signal to ground. Transistor Q_1 and resistor R_1 form a voltage divider that attenuates the signal by about 60 decibels. The "on" resistance of the FET is approximately 100 ohms.

To pass the audio input, a negative voltage must be applied to Q_1's gate to turn the device off. The audio signal at the gate of Q_2 can then reach the output devoid of any switching transients. □



FETs replace bipolars. In bipolar-transistor audio squelch circuit (a), large output transient is generated when Q_2 turns off, because dc voltage at Q_2's base is grounded. Substituting FET circuit (b) eliminates transients without limiting switching speed. Control FET Q_1 turns off for negative gate voltage, allowing amplifier Q_2 to pass audio signal to output. Only ac voltage is present at Q_2's gate.

Diode plus low-cost op amp makes accurate thermostat

by Robert Koss
Adac Inc., Colchester, Vt.

Employing a silicon diode as the temperature-sensing element allows an inexpensive operational amplifier to control temperature to a variation of less than 0.05°C. A type 1N4148 diode, for instance, has a typical temperature coefficient of –2 millivolts/°C.

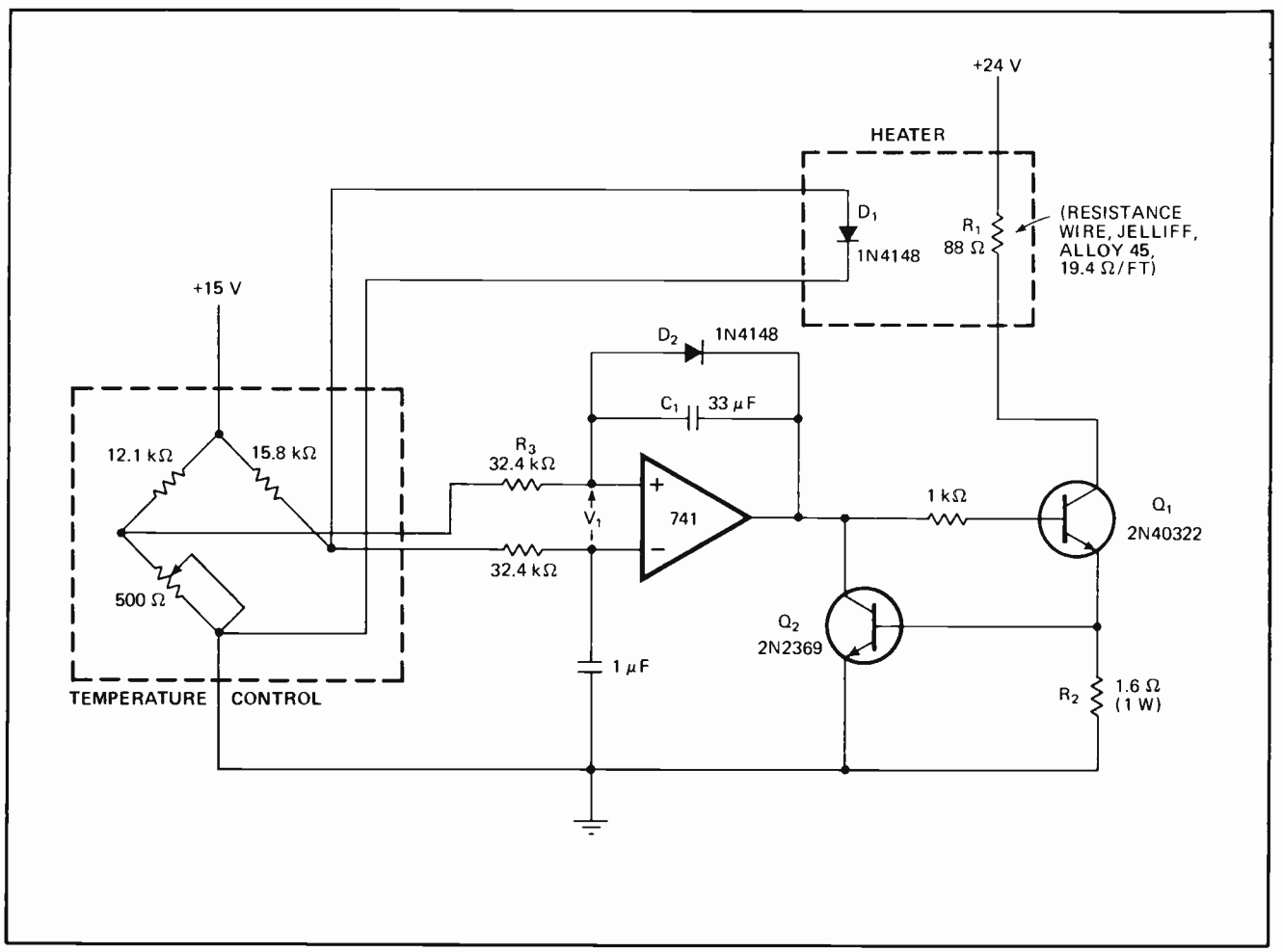
The resistance bridge in the diagram sets the temperature that is sensed by diode D_1 and that is maintained by the heater element, resistor R_1.

When temperature is too low, control voltage V_1 goes negative, limiting the op amp's output to 12–14 volts. Transistor Q_1 conducts and provides the necessary heater current. When temperature is too high, diode D_2 prevents amplifier output voltage from going negative, and transistor Q_1 turns off. Average current then is always positive and is controlled by the amplifier to compensate for changes in temperature.

Transistor Q_2 and resistor R_2 prevent the heater current from exceeding a specified limit. (For this circuit, maximum heater current is 375 mA.) If the voltage drop across resistor R_2 equals Q_2's 0.6-V base-emitter voltage, transistor Q_2 turns on, shorting the amplifier's current-limited output to ground, thus turning off transistor Q_1.

The stability of the control loop depends on several thermal time constants that are not easy to calculate. Computations can be reduced a little by using a relatively large time constant in the feed-forward direction for R_3C_1 and keeping the remaining thermal lags as small as possible. Sense diode D_1 should make good thermal contact with the object to be temperature-controlled. It should also be thermally insulated from changes in external conditions. □

Inexpensive thermostat. Tight temperature coefficient of silicon diode permits low-cost op amp to be used for controlling temperature to within 0.05°C. Resistance bridge sets temperature of heater containing sense diode D_1. For low temperatures, amplifier turns on transistor Q_1, which supplies heater current. For high temperatures, amplifier output remains positive because of diode D_2, but Q_1 stops conducting.



Logic system checks out analog-to-digital converter

by Charles J. Huber
Westinghouse Electric Corp., Systems Development Div., Baltimore, Md.

Testing the conversion accuracy of an analog-to-digital converter need not be a laborious and time-consuming task. The test configuration shown can reduce the job to a go/no-go operation without undue expense (approximately $36 for integrated circuits plus the cost of a digital-to-analog converter).

This test system produces a 12-bit digital ramp that is converted (by the d-a converter) to a 4,096-step analog ramp. The analog ramp is applied to the a-d converter under test, and the resulting output from the 10-bit a-d converter is compared to the 10 most significant bits of the 12-bit digital ramp.

An input clock is applied simultaneously to a one-shot delay network and to a ripple-through counter consisting of three four-bit binary counters. The delayed clock becomes the input for six four-bit buffer latches. These accept and delay all 12 of the bit outputs from the counter to remove glitches from the digital ramp. The delayed clock now acts as the basic time reference.

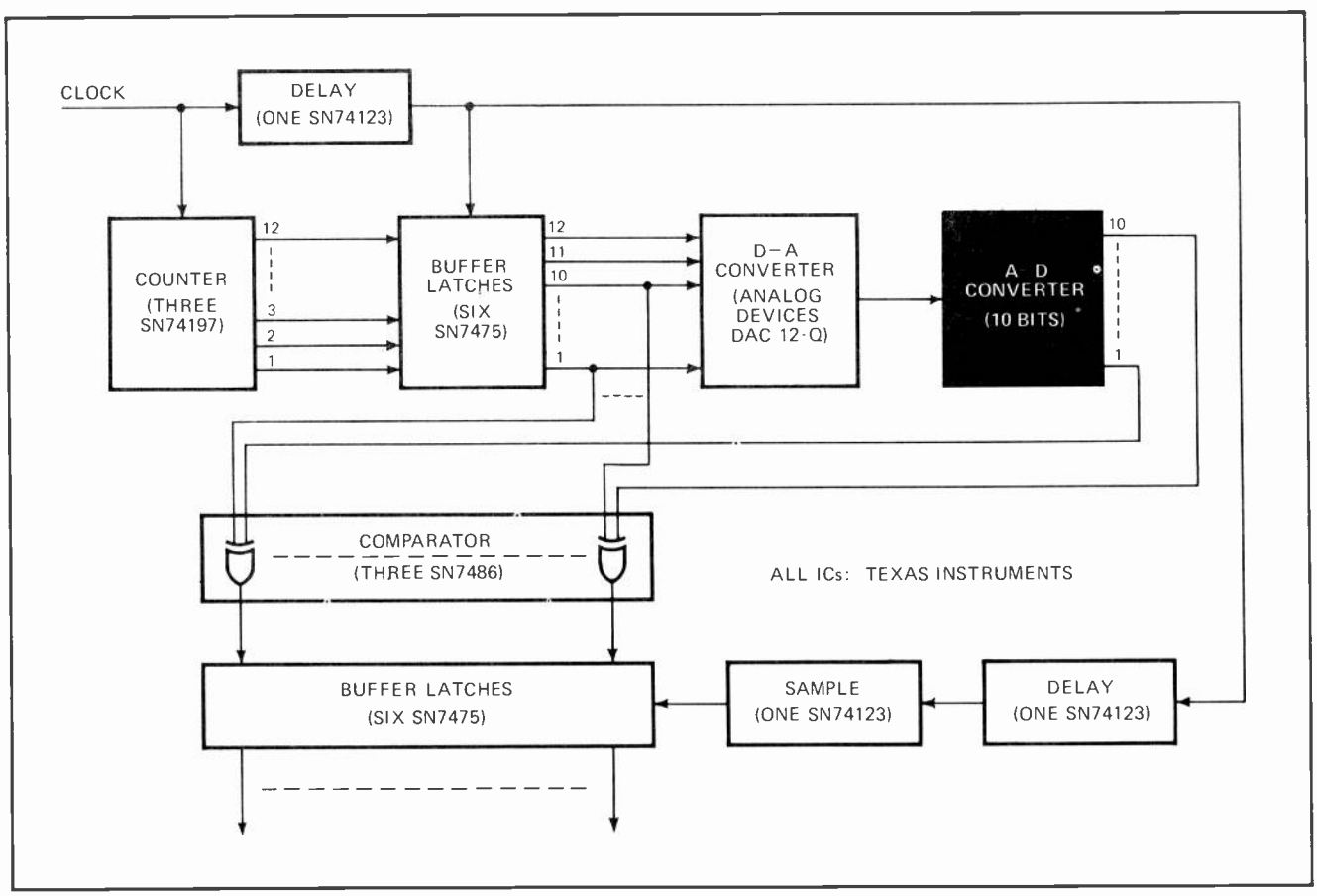
The 10 most significant bits from the latches drive both a d-a converter and a comparator formed by three quad exclusive-OR gates. These gates compare the bits of the digital ramp to the output bits of the a-d converter, on an individual basis. The analog output of the d-a converter corresponds to the input digital code within ±⅛ the least significant bit.

The delayed clock pulse also passes through another one-shot delay network before reaching a sample circuit, which strobes a second set of buffer latches. For zero error at the buffer outputs, the minimum strobe delay equals the a-d conversion time. An interpolating voltage applied to the d-a permits continuous voltage control of the a-d output over the ⅛-bit range.

The test system can accurately determine conversion times of 2 microseconds for successive-approximation and variable-reference a-d converters. Additionally, the nature and position of other conversion errors can be determined by relating displayed error pulses to the digital ramp. For example, small areas of the ramp can be investigated by making constants of the 10 most significant bits of the digital input and using the eleventh and twelfth bits as variable controls.

More system flexibility can be obtained by using an up/down counter to eliminate the d-a converter's slew time when the count changes from 111 . . . 1 to 000 . . . 0. Replacing the counter with a pseudo-random generator allows testing for all input changes. □

Verifying converter accuracy. A-d converter test system generates 12-bit digital ramp with ripple-through binary counter. Buffer latches smooth out any ramp glitches. D-a converter then develops analog input for a-d converter using only 10 most significant ramp bits. Exclusive-OR gates compare a-d output with ramp. Errors pass to another buffer for comparison with appropriately delayed clock.



Double-duty multivibrator gives complementary outputs

by Edward Beach
National Radio Institute, McGraw-Hill Inc., Washington, D.C.

Depending on its input signal period, a pulse generator operates as a one-shot or as a synchronous astable multivibrator. In either mode, the circuit provides complementary outputs. An ordinary grounding pushbutton switch can serve as the input device.

Gates G_1 and G_2 form a simple latch that prevents the circuit from operating in the absence of an input (high). When the input goes low, the latch changes state, allowing gate G_1 to act as an inverter. Gates G_1, G_3, and G_4 are the pulse-generating portion of the circuit.

If the input remains low for less than three generator time constants, single complementary pulses are produced by gates G_1 and G_4. The leading edge of each output pulse coincides (neglecting gate delays) with the leading edge of each input pulse. The trailing edge of the output pulse (again, neglecting gate delays) resets the latch and disables the generator.

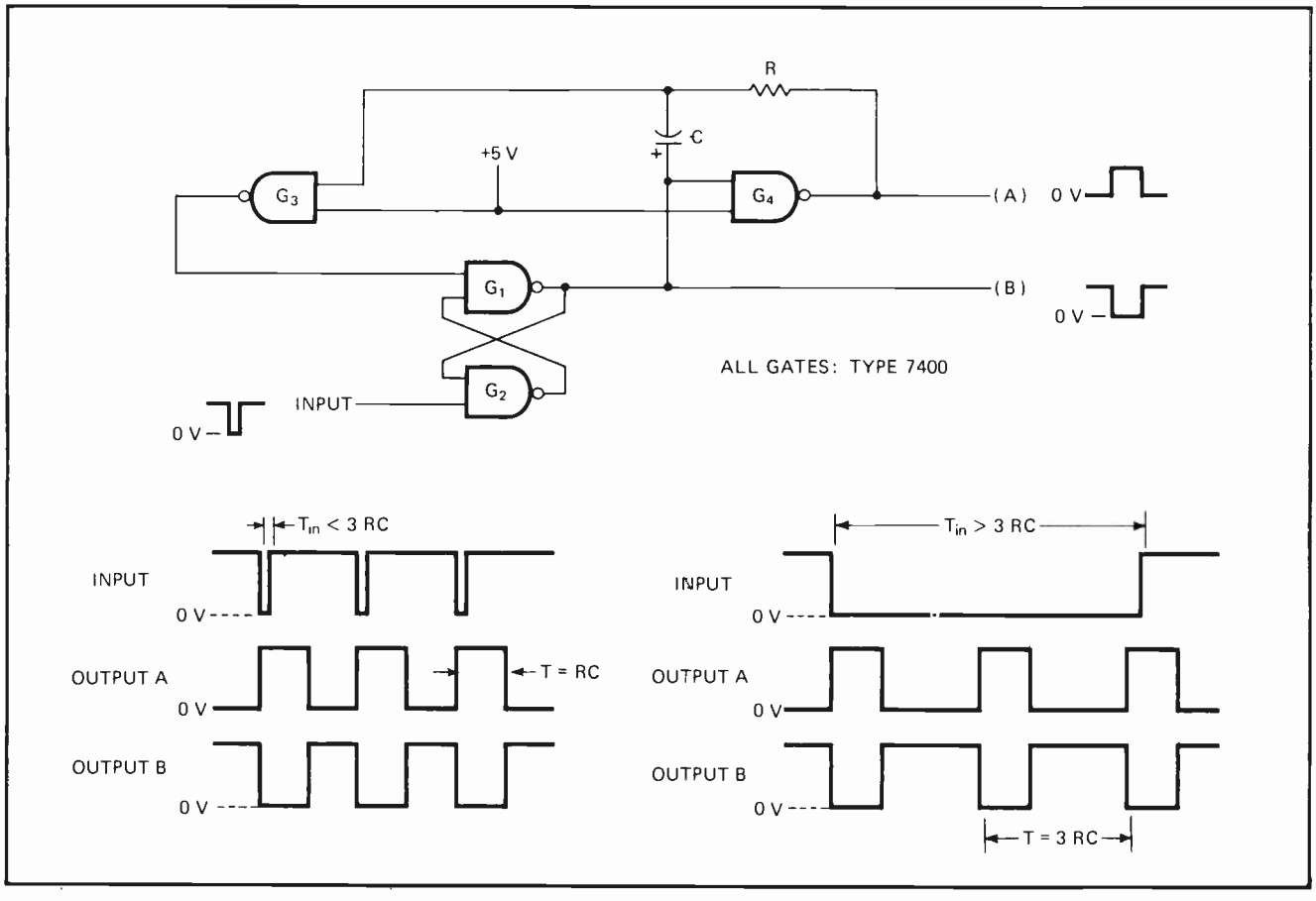
When the input signal remains low for longer than three time constants, at least two complete output pulses with a period equal to approximately three generator time constants are produced. In this case, the pulses begin and end synchronously. The first output pulse coincides with the leading edge of the input, and the last pulse is a full-width pulse, no matter when the input is removed.

Resistor R can range in value from 330 ohms to 1.5 kilohms, while capacitor C can be some value between 0.001 microfarad and 1,000 μF. For example, when R = 1,000 ohms and C = 100 μF, the circuit will produce either a 100-millisecond pulse or a 100-ms pulse train with a repetition rate of about 3 pulses per second.

For critical timing applications, a nonpolarized capacitor should be used when C is a high value; for less-critical applications, an ordinary electrolytic or tantalum capacitor will suffice. Since the reverse capacitor voltage is only about -0.7 volts, an inexpensive capacitor can be used.

The circuit can also function as an inexpensive transistor-transistor-logic clock simply by replacing gates G_1, G_3, and G_4 with half a type 7404 circuit. In addition, gate G_2 could be eliminated and an inverted version of the input signal applied directly to gate G_1, but this could shorten the last pulse in the pulse train. □

Manual pulser. Pushbutton-operated pulse generator functions either as a monostable or astable multivibrator. Low input signal enables G_1-G_2 latch so that G_1 becomes an inverter. Gates G_1, G_3, and G_4 then generate complementary output pulses. When input is low for less than three RC time constants, circuit is a one-shot; when input period exceeds 3RC, circuit is a synchronous astable multivibrator.



Schmitt trigger prevents clock train overlap

by R.R. Osborn
Roberts Enterprises, Flagstaff, Ariz.

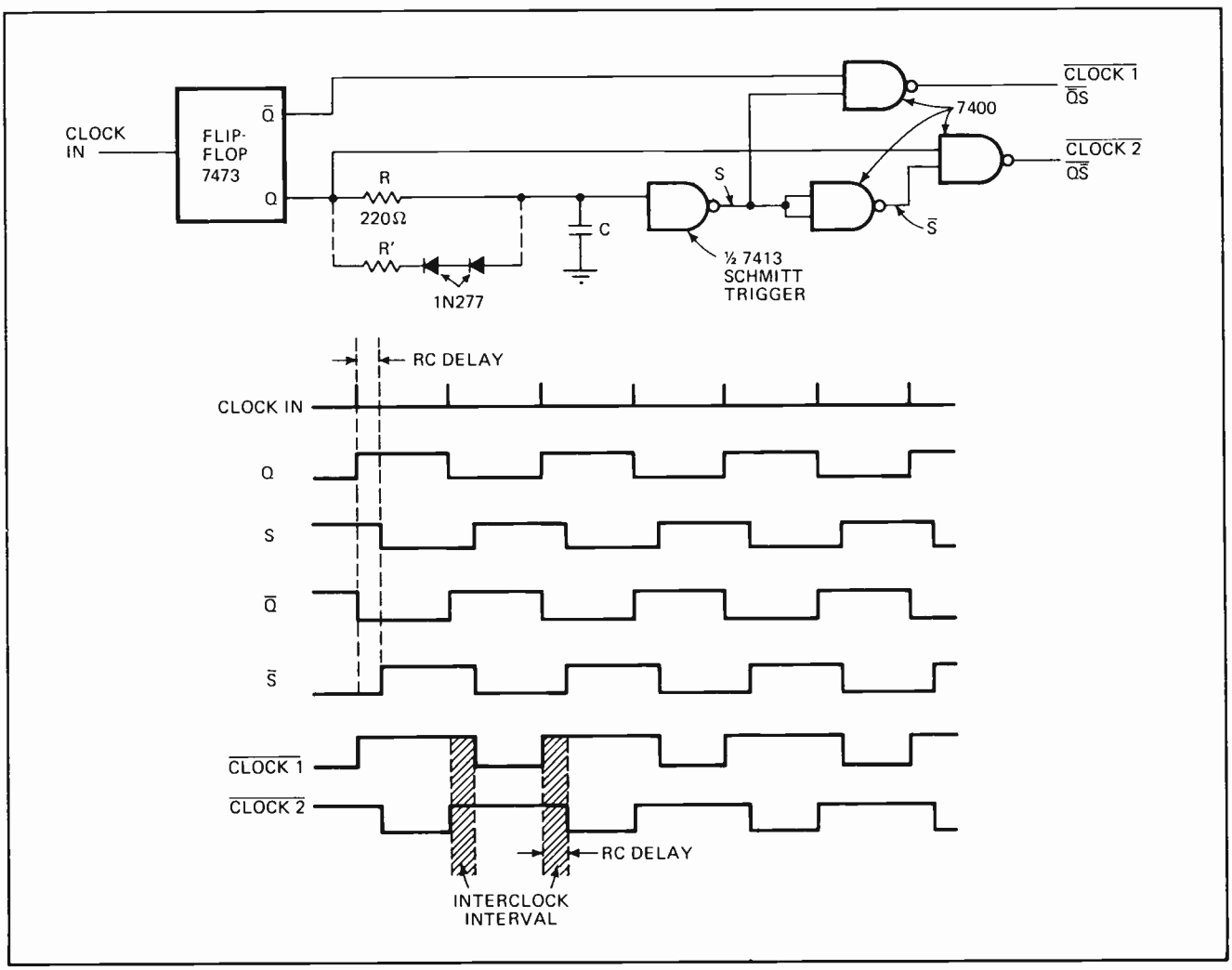
Non-overlapping clock trains are often required in digital systems, especially when transistor-transistor-logic circuits must be interfaced with metal-oxide-semiconductor logic circuits. A single integrated Schmitt trigger, using only one RC time constant, can provide the appropriate delay between clock trains. Moreover, the temperature stability of the IC Schmitt trigger assures that the separation between output clocks remains constant, despite changing temperature.

The Schmitt trigger delays the Q output of the flip-flop for the time fixed by resistor R and capacitor C; it does not delay the flip-flop's $\bar{Q}$ output. The delayed and undelayed pulse trains then pass through a combination of NAND gates, producing the two desired non-overlapping output clocks.

Interclock intervals, which occur when both clock outputs are high, are unequal if resistor R alone sets the delay, because of the flip-flop's output levels and the Schmitt trigger's input current. Adding resistor R′ and two diodes, as shown by the dashed lines, allows the interclock intervals to be made equal to each other. The value of R′ can range from 0 to 5 kilohms.

Capacitor C can vary from 0 to 1,000 microfarads, producing interclock intervals of 30 nanoseconds to 1 second. The time between input clock pulses must always be greater than the output clock interval; input clock frequency can be as high as 10 megahertz. □

Staggering clock phase. Circuit produces two non-overlapping output clock trains from single input clock to flip-flop. Q output of flip-flop is delayed by Schmitt trigger for one RC time constant. Delayed clock from Q and undelayed clock from $\bar{Q}$ are combined by NAND gates to yield separate output clock trains. Adding dashed components yields equal interclock intervals. Clock speed can be as fast as 10 MHz.



Broadband cutoff limiter is phase-transparent

by Roland J. Turner
RCA Missile & Surface Radar Division, Moorestown, N.J.

When information is transmitted in the phase domain, the video or intermediate-frequency processor in a radar or communications system frequently requires a limiter circuit that does not alter the zero crossings of the input signal.

By using current cutoff limiting, a broadband phase-transparent (zero phase-shift) limiter can be built that maintains input zero crossings within 14 picoseconds, while providing a gain of 20 decibels over its linear range. This limiter, which operates from dc to 30 megahertz, can improve receiver sensitivity, allowing smaller targets to be resolved in a radar system or, in a communications system, reducing level- and frequency-dependent phase noise so that phase-detection thresholds can be lowered.

The limiter circuit uses microwave transistors that have a unity-gain crossover frequency (f_T) of greater than 1 gigahertz. The bandwidths of the transistor stages making up the limiter can then exceed 500 MHz to yield the limiter's over-all wideband performance by using conventional microstrip techniques.

Exceptional signal control is realized by driving the transistors into their cutoff regions to achieve limiting action. Transistor cutoff parameters are more controllable and more clearly defined than transistor saturation parameters. And with cutoff signal limiting, the transistors look like high impedances to low load impedances, thereby achieving fast limiting action with controlled passive elements.

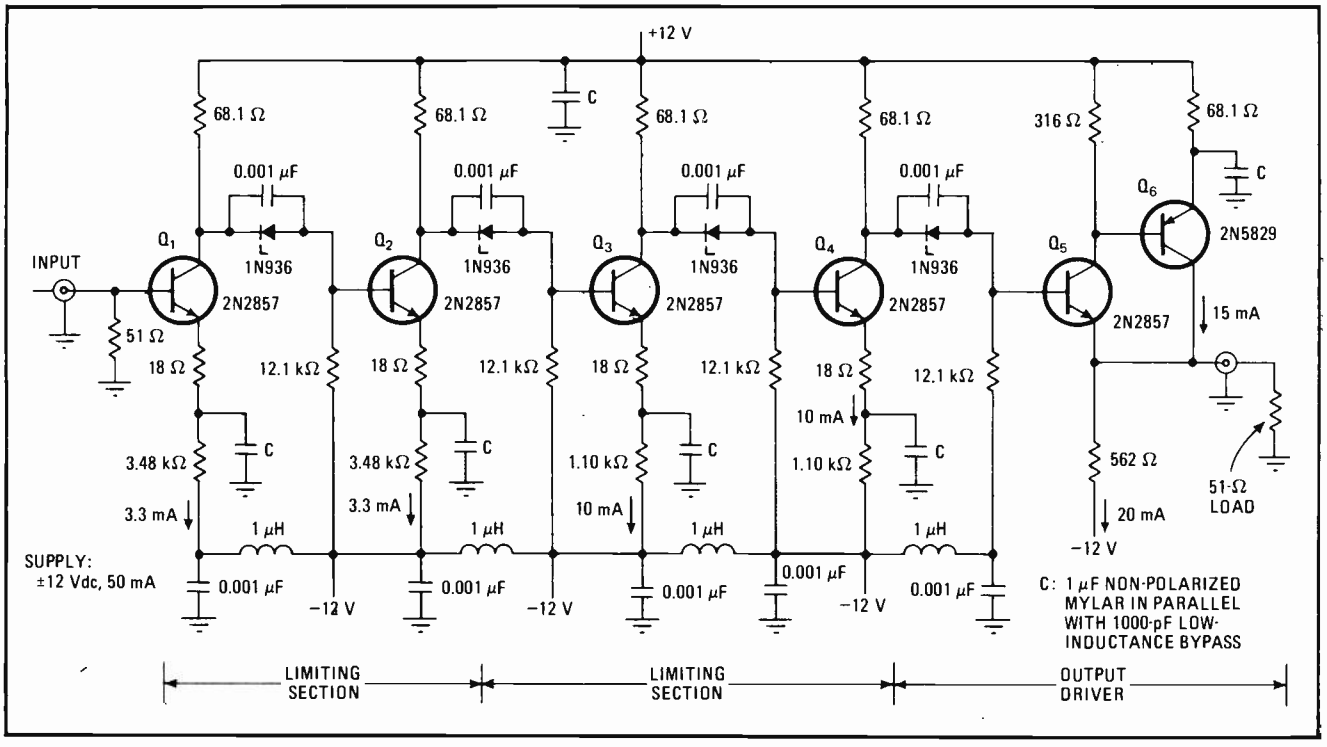
Transistors Q_1 through Q_4 perform the limiting function, while transistors Q_5 and Q_6 operate as a unity-gain output driver. There are two limiting sections, one consisting of Q_1 and Q_2, and the other of Q_3 and Q_4. Two transistor stages, then, form each limiting section.

For one polarity of the input signal, one transistor stage operates as a low-gain broadband amplifier, while the other limits the section's output by performing as a cutoff isolation amplifier. During the opposite polarity of the input signal, the transistor stages reverse roles. Each limiting section supplies a gain of 3.3. The output level of each section is determined by its quiescent operating point.

This limiting scheme provides extremely low carrier output phase shift for the full dynamic range of the input signal. Over a 40-dB input range, from 100 millivolts peak-to-peak to 10 volts pk-pk, the limiter circuit is phase-transparent within 0.25°. For example, the output is 1.2 V pk-pk for a 120-mV input. For frequencies up to 20 MHz, the output impedance of the driver section is less than 5 ohms.

From dc to 20 MHz, the time displacement of adjacent zero crossings of the output waveform are within 14 picoseconds of the period established by the input zero crossings. In the phase domain, this means that the phase of a 20-MHz input will be shifted less than 0.1° at the output, making the limiter phase-transparent for all practical purposes. □

Linear-phase signal limiting. Operating from dc to 30 megahertz, limiter circuit remains phase-transparent within 0.25° over 40-decibel input dynamic range. Each limiting section contains two transistor stages. Depending on input signal polarity, one stage is low-gain broadband amplifier, while the other acts as cutoff isolation amplifier. Optimum usage of transistor cutoff parameters achieves desired limiting action.



Preset generator produces desired number of pulses

by Glen Coers
Texas Instruments, Components Group, Dallas, Texas

Computer systems and medical instruments are likely applications for a digital pulse generator that will deliver, on command, any desired number of full-width pulses from 1 to 999. Three 10-position switches set the number wanted.

Rotary switches S_1, S_2, and S_3 fix the number of output pulses. S_1 controls the most significant digit, while S_3 controls the least significant digit. For example, if S_1 is set to 3, S_2 to 6, and S_3 to 8, the number of output pulses will be 368.

Gates G_1 through G_4 eliminate any count error caused by contact bounce from toggle switch S_4. When S_4 is placed in its count position, flip-flop FF_1 inhibits gate G_4 until the trailing edge of S_4's count pulse occurs, so that even the first output pulse is full width.

Placing S_4 in its count position results in a high at both inputs to G_2, enabling this gate (its output goes low) and resetting the decade counters to zero. The count command also causes one input of G_1 to go low, making its output high. This clears flip-flop FF_1 and keeps its Q output low. The high from G_1 also drives FF_1's preset function high, as well as one of the inputs to G_4. The output from G_5 is now low.

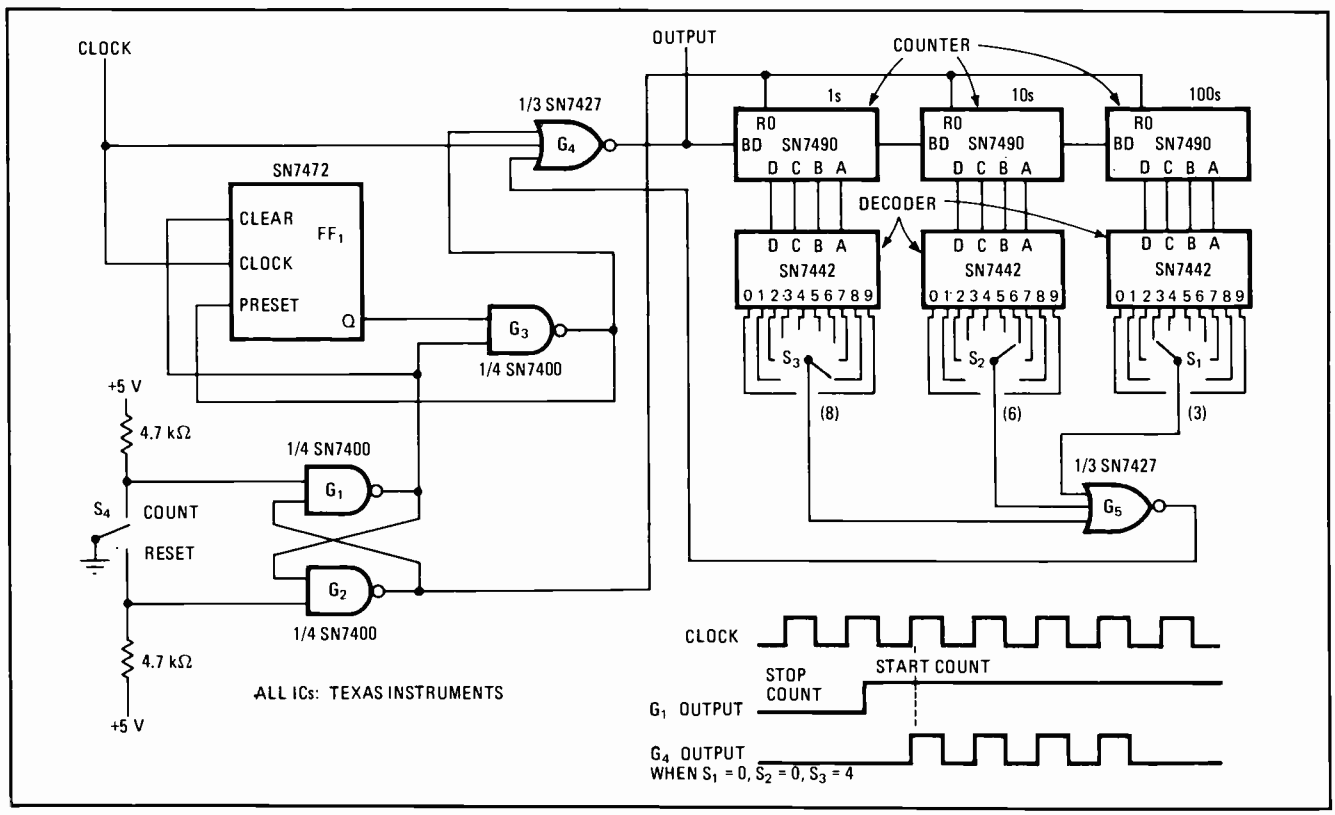
The first negative edge of a clock pulse triggers the flip-flop and makes Q go high. The output of G_3 then goes low, presetting the flip-flop to maintain Q in the high condition. When G_3's output goes low, one input to G_4 also goes low, enabling this gate so that clock pulses are passed to its output.

The binary-coded-decimal count that is accumulated in the divide-by-10 arrangement of decade counters is transferred to the BCD-to-decimal decoders. A decoder output goes low when that decoder reaches the setting of its associated rotary switch. When all three decoder outputs are low, gate G_5 is inhibited (its output goes high). This causes one input to G_4 to go high, stopping the transfer of pulses.

Placing switch S_4 in its reset position drives one input to gate G_2 low, making its output go high and operating the reset function of the decade counters. Both inputs of G_1 are now high, while its output, the clear function of the flip-flop and one input to G_3 are low. This clears Q to a low condition, causing G_1's output, FF_1's preset function, and one input to G_4 to go high. The circuit is now ready to start a new count.

Adding more counters, decoders, and switches will, of course, increase the number of pulses that can be counted. □

Pulse counter. Three rotary switches control number of output pulses that can be generated; settings may range from 1 to 999. Flip-flop and gates G_1 through G_4 assure that all output pulses are full width. Toggling switch S_4 to its count position allows gate G_4 to transfer clock pulses to divide-by-10 arrangement of decade counters. Each BCD-to-decimal decoder counts to setting of its rotary switch.



Frequency doubler accepts any waveshape

by Donald DeKold
Santa Fe Junior College, Gainesville, Fla.

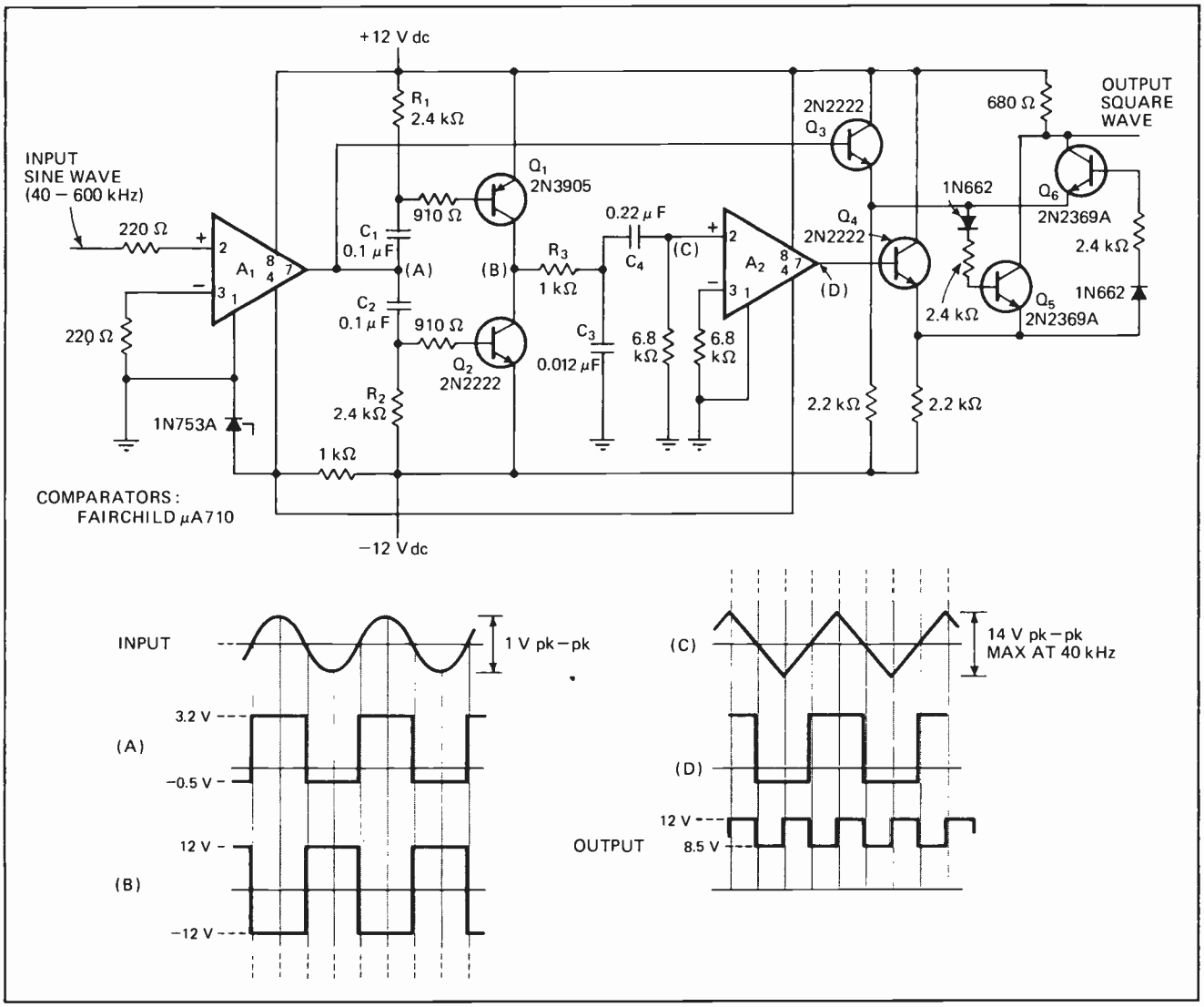
The frequency of nearly any waveform can be doubled by means of quadrature square waves that drive a biconditional logic circuit. Only two restrictions must be imposed on the input to this frequency doubler—the wave form must have a duty cycle of approximately 50% and a peak-to-peak amplitude of at least 0.5 volt.

For the circuit shown, the input is a sine wave that can vary in frequency from 40 to 600 kilohertz. The output is a square wave at twice the input frequency, having a duty cycle of about 38% for the lower-frequency inputs to around 65% for the higher-frequency inputs.

Comparator A_1 operates in its noninverting mode, accepting the input sine wave and producing a square wave at its output. Capacitors C_1 and C_2 couple this square wave to a pair of complementary switches, transistors Q_1 and Q_2. The switches boost the amplitude of the square wave to 24-v pk-pk. Resistors R_1 and R_2 prevent the bases of Q_1 and Q_2 from being clamped to dc voltages that would drive them into cutoff.

Capacitor C_3 is alternately charged and discharged through resistor R_3. When Q_1 is in saturation and Q_2 in cutoff, C_3 exponentially charges towards 12 v dc; with Q_1 cut off and Q_2 saturated, C_3 discharges towards

Frequency times two. Sine-wave input is converted into square wave by comparator A_1. Emitter-followers Q_1 and Q_2 charge and discharge capacitor C_3, producing triangular wave that drives comparator A_2. Resulting square-wave output of A_2 is in quadrature with square-wave output of A_1. Switches Q_5 and Q_6 conduct only when comparator states are different, providing square wave that is twice input frequency.



−12 V dc. When the charging or discharging interval is short compared to the R_3C_3 time constant, the voltage across capacitor C_3 approximates a triangular wave that has its peak value occurring 90° out of phase with the peak amplitude of the input sine wave.

The triangular wave is applied to the noninverting input of comparator A_2 through capacitor C_4. The comparator "squares" the triangular wave about its zero crossings, producing a square wave that is 90° out of phase with the output of the first comparator.

Transistors Q_3 and Q_4 are emitter-followers that act as buffer amplifiers for both comparators and drive a set of nonsaturating switches, transistors Q_5 and Q_6. When comparator states are the same, Q_5 and Q_6 are off; when comparator states differ, Q_5 or Q_6 conducts.

The switching action of transistors Q_5 and Q_6 is equivalent to the biconditional logic function:

$$XY + \overline{X}\overline{Y} = 1$$

which has the effect of doubling the frequency of quadrature square waves. A diode and resistor in each transistor's base-emitter loop prevent false switching when both comparators are in the same state, but may have different output levels.

A square wave with a 50% duty cycle can be realized for a nominal input frequency of 120 kHz. At lower frequencies, the duty cycle is smaller because the triangular wave becomes exponentially rounded. At higher frequencies, the duty cycle is larger, since the amplitude of the triangular wave decreases, thereby shortening the duty cycle of the square wave at the output of the second comparator. Also, circuit delays become significant compared to the period of high-frequency inputs.

The frequency doubler can operate below 40 kHz if higher capacitor values are used throughout the circuit. To operate at higher frequencies, faster switching devices must be used, and transistors Q_1 and Q_2 must not be allowed to saturate.

Since the maximum input voltage for the type μA710 comparator is ±7 V, the amplitude of the triangular wave must not exceed 14 V pk-pk. □

Op amp cancels video switching transients

by Steven E. Holzman
Electromagnetic Systems Laboratories, Sunnyvale, Calif.

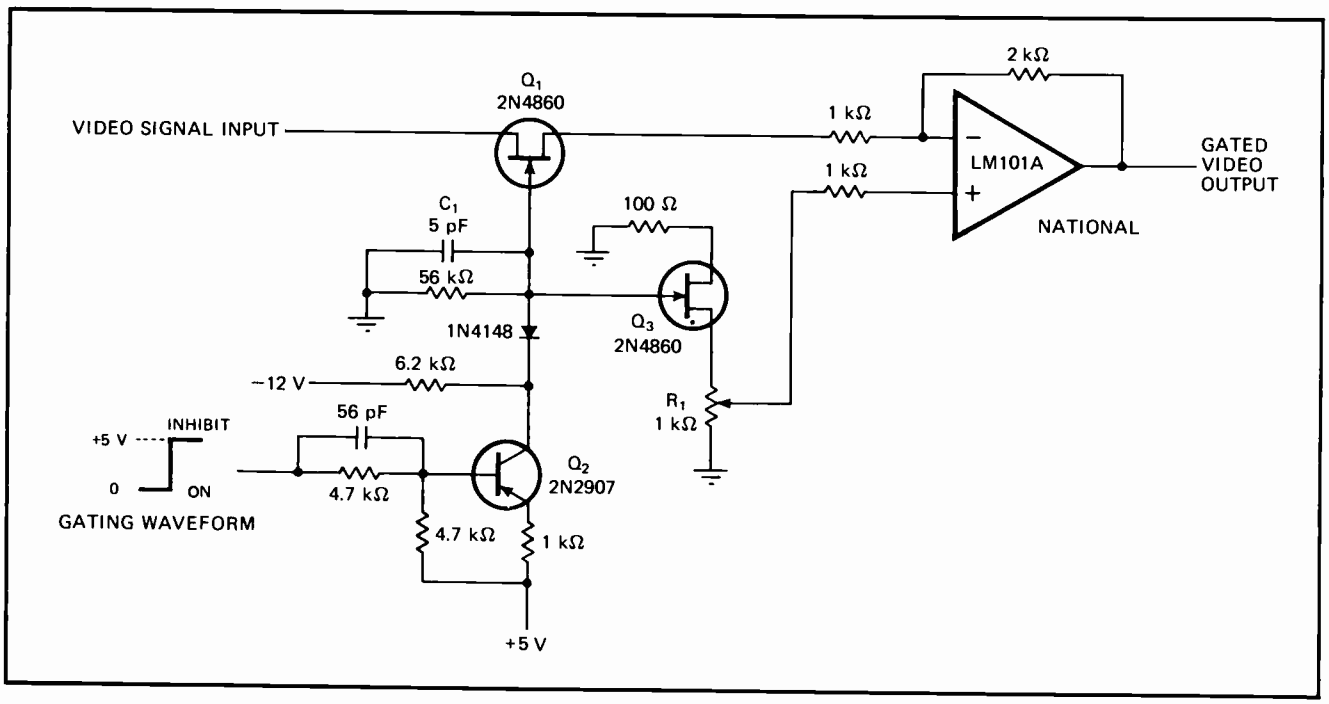
The common-mode rejection of an ordinary operational amplifier can help to minimize switching transients in low-level video gates. The transients are caused by the leading and trailing edges of the switching waveform.

The video gate basically consists of a switching field-effect transistor (Q_1), its associated TTL-compatible driver (bipolar transistor Q_2), and an output op amp. Transients are generated when the switching waveform edges pass through the FET's gate-drain junction.

By adding a second FET (Q_3) and its biasing resistors, the transients can be eliminated by forcing them to cancel through the op amp. Since the transients from transistor Q_1 will be identical to those from transistor Q_3, the op-amp's common-mode rejection stops these unwanted spikes from reaching the output.

Capacitor C_1 helps maintain equal feedthrough char-

Transient-free video gate. Leading and trailing edges of gating waveform create transients when passing through first FET, Q_1. Including a second FET, Q_3, duplicates signal path of Q_1 and permits op-amp common-mode rejection to cancel most transients. Capacitor C_1 equalizes feedthrough characteristics of the two FETs so that matched pair is not necessary. Bipolar transistor Q_2 makes circuit TTL-compatible.



acteristics for both Q_1 and Q_3. This eliminates the need for a matched pair of FETs. By simply adjusting resistor R_1, nearly all of the transients can be cancelled.

In the circuit shown, the amplitude of the switching transients can be reduced to less than 1 millivolt over an operating temperature range of −20 to +60°C. □

Pulse generator accuracy is immune to aging

by Frank Cicchiello
Digilog Systems Inc., Willow Grove, Pa.

This pulse generator for driving digital circuits won't change frequency, even after its components have aged or are replaced. And pulse repetition rate remains stable over a wide temperature range.

If any or all of its active devices are replaced or have aged, the generator exhibits only a 1.5% worst-case variation in rep rate. Replacing or aging any or all of the passive components causes a worst-case change of 1%. Typically, rep rate varies merely 0.5% over a 50°C temperature range, and all variations amount to less than 2% when taken collectively.

When the dc supply voltage (V_{CC}) is turned on, timing capacitor C_1 charges exponentially through resistor R_1 until capacitor voltage reaches the threshold voltage (V_T) of programable unijunction transistor (PUT) Q_1. This triggering level is established by the voltage divider formed by resistors R_2, R_3, and R_4. For optimum temperature stability when the supply is greater than 10 volts:

$$V_T = 0.5V_{CC}$$

Pulse rep rate is determined by:

$$\text{rep rate} = 1/[0.78R_1C_1 + (0.5 \times 10^{-12})R_1C_1]$$

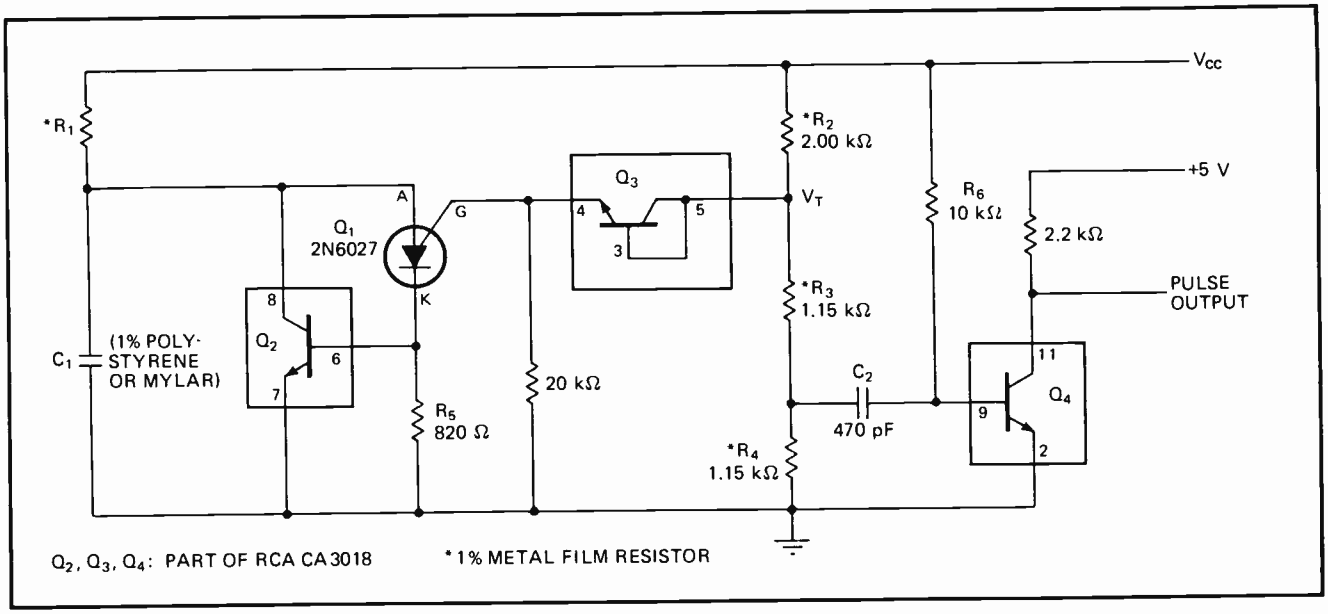
Once its triggering threshold is reached, the PUT switches, causing its gate voltage to swing in the negative direction. This produces a positive-going pulse across cathode resistor R_5, which turns on transistor Q_2 and discharges capacitor C_1.

The function of Q_2 is twofold. It rapidly discharges C_1 by passing the discharge current around the anode-cathode junction of the PUT. And it also effectively eliminates the PUT's valley-current offset. This allows timing resistor R_1 to have a value as low as 2 kilohms, rather than a value above 100 kilohms, as normally required. Output pulse rep rate can then vary over a 250:1 range for a given value of C_1 (500 picofarads to 1 microfarad). Output frequency can be up to 1 megahertz.

PUT temperature stability is assured by diode-connected transistor Q_3, which matches the temperature characteristic of the PUT's anode-gate junction, even if current flow is in the microampere region. Although most standard diodes cannot do this, almost any low-leakage diode-connected silicon transistor may be used for Q_3.

Negative-going pulses from the PUT are directly coupled to the base of transistor Q_4 through transistor Q_3; capacitor C_2 provides ac coupling. If pulses shorter than 4 to 5 microseconds (typical for this circuit) are required, the R_6C_2 time constant of Q_4's input coupling network can be reduced to differentiate the input signal and produce narrower positive-going output pulses. The output pulse train is compatible with both transistor-transistor and diode-transistor logic. □

Stable pulse generator. Power supply charges capacitor C_1 until threshold of programable unijunction transistor Q_1 is reached, Q_1 then switches, turning on transistor Q_2, which discharges C_1. Diode-connected transistor Q_3 dc couples resulting pulse to output transistor Q_4. Generator's repetition rate changes only 2% for worst-case variation of all its components, even if they age or are replaced.



Logic probe with LED display checks ECL circuits

by William Wilke
University of Wisconsin, Madison, Wis.

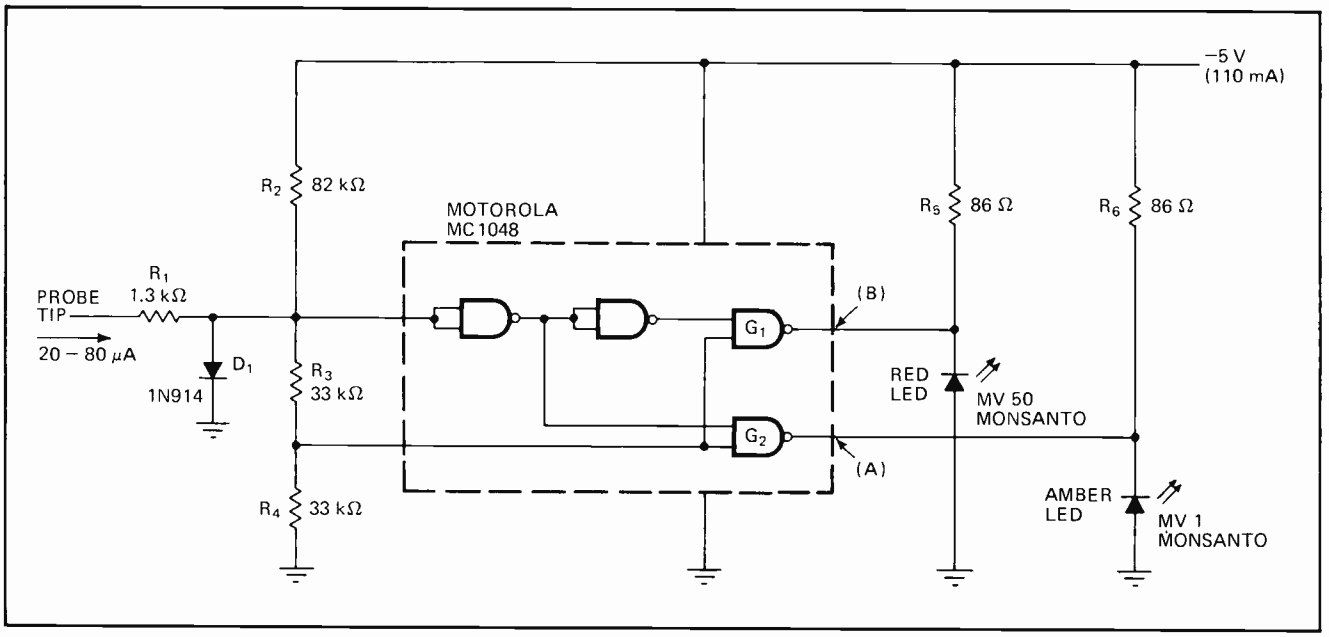
A simple logic probe for testing emitter-coupled-logic circuits identifies three input conditions—a logic high, a logic low, and an open circuit. The probe indicates a logic high (-0.75 volt) by lighting a red light-emitting diode, a logic low (-1.5 V) by lighting an amber LED, and an open-circuit condition by lighting neither. The circuit costs about $4–$5 to build.

Input resistor R_1 and diode D_1 protect the circuit against positive voltages. When an open circuit exists at the probe tip, resistors R_2, R_3, and R_4 hold point A at a logic low so that gates G_1 and G_2 are disabled. Since the LEDs only light for a logic low excitation voltage, both stay off regardless of the voltage level at point B.

When the probe tip is connected to a low or a high logic level, point B is forced to that level (-1.5 or -0.75 V) and point A is forced to a logic high level. Now gates G_1 and G_2 are enabled and, depending on the level at B, either the red or the amber LED lights up.

Resistors R_5 and R_6 allow the quad ECL NAND gate to switch up to 20 milliamperes through the LEDs for a brighter light output. The entire logic probe circuit can be assembled inside an ordinary felt tip pen or other small container. □

ECL logic probe. Red light-emitting diode lights up for logic high input, while amber LED indicates low input. Both LEDs are dark with open circuit at probe tip. When low or high is present at input, gates G_1 and G_2 are enabled, point A goes high, and point B goes to logic level at input, lighting proper LED. For open-circuit input, G_1 and G_2 are disabled and point A is low, keeping both LEDs off.



Converter for oscilloscope provides four-channel displays

by Grady M. Wood
Harris-Intertype Corp., Melbourne, Fla.

With the help of only two integrated circuits and a handful of passive components, conventional single- or dual-channel oscilloscopes can be economically converted to four-channel displays. The key element is a four-channel programable amplifier, the Harris type HA-2405. This is an operational amplifier with four identical input stages, any one of which may be electronically connected to the output stage by two binary address inputs.

For the scope converter circuit, each amplifier is wired in its unity-gain inverting mode. High-value (2 megohm) feedback resistors provide a high input impedance for each channel. All four non-inverting amplifier inputs go to a variable voltage source formed by a 500-kilohm potentiometer that is between the ±15-volt

power supplies. This arrangement provides an independent centering control for each channel. Any offset voltage resulting from the large feedback resistors is not a problem, since the centering control provides adequate amplifier adjustment range.

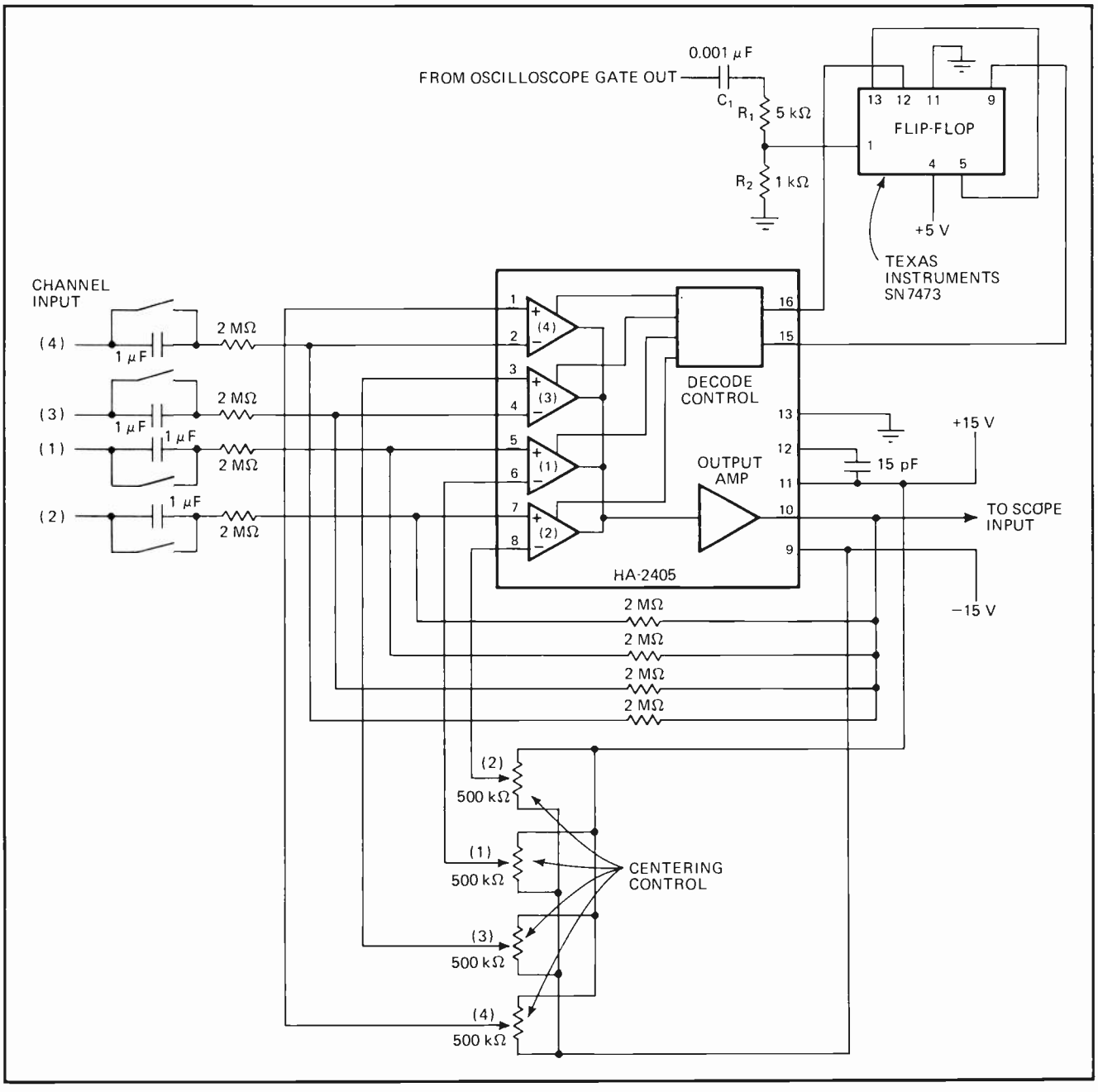
The scope's gate output is divided down by a dual J-K flip-flop to supply binary channel selection signals for the integrated amplifier circuit. This gate signal is synchronized to the scope's sweep, so that there are no timing difficulties. After each trace is completed, the negative-going gate signal selects the next channel. The retrace time allows adequate time for channel selection.

The passive network at the input to the flip-flop—capacitor C_1 and resistors R_1 and R_2—extracts a trigger pulse of approximately 5 V from the 30-V waveform obtained at the GATE OUT terminal of a Tektronix type 545 scope. Other scopes may require a different passive network.

Important circuit performance characteristics include: a gain of 1, a bandwidth of dc to 5 megahertz, a slew rate of 15 V/microsecond, a maximum input voltage of ±10 V, an input impedance of 2 megohms, and a crosstalk figure of 80 decibels.

Circuit voltage range, bandwidth, and input impedance can be increased by adding op amps to buffer each input. Making the gain of each of these buffers independently variable further improves circuit versatility. Approximate parts cost for the entire circuit is $25. □

Scope converter. Monolithic quad operational amplifier provides inexpensive way to increase display capability of standard oscilloscope. Binary inputs drive IC op amp; dual flip-flop divides scope's gate output to obtain channel selection signals. All channels have centering controls for nulling offset voltage. Negative-going scope gate signal selects next channel after each trace. Circuit operates out to 5 MHz.



Controlling op amp gain with one potentiometer

by T. Frank Ritter
San Antonio, Texas

A single potentiometer and a few resistors can control the gain of an operational amplifier from a selected negative value, through a null, to its positive open-loop gain. The variable-gain circuit, which is shown in (a), maintains a high input impedance, even at high amplification. It makes a convenient wide-range voltage reference for a voltage regulator because it eliminates the need to switch the op amp's circuit for above- or below-reference operation.

A graph of voltage gain versus potentiometer rotation is also shown in (a). The equation for output voltage can be written as:

$$E_o = [E_i R_F/(R_I + R_1)][(R_1/R_2) - (R_{I+}/R_{I-}) + (R_1/R_F)]$$

where R_I" is the resistor at the op amp's noninverting input, and R_{I-} the resistor at the inverting input. Varying feedback resistor R_F changes the magnitudes of both the positive and negative gains without changing the appearance of the graph; varying resistance ratio R_{I+}/R_{I-} shifts the null point.

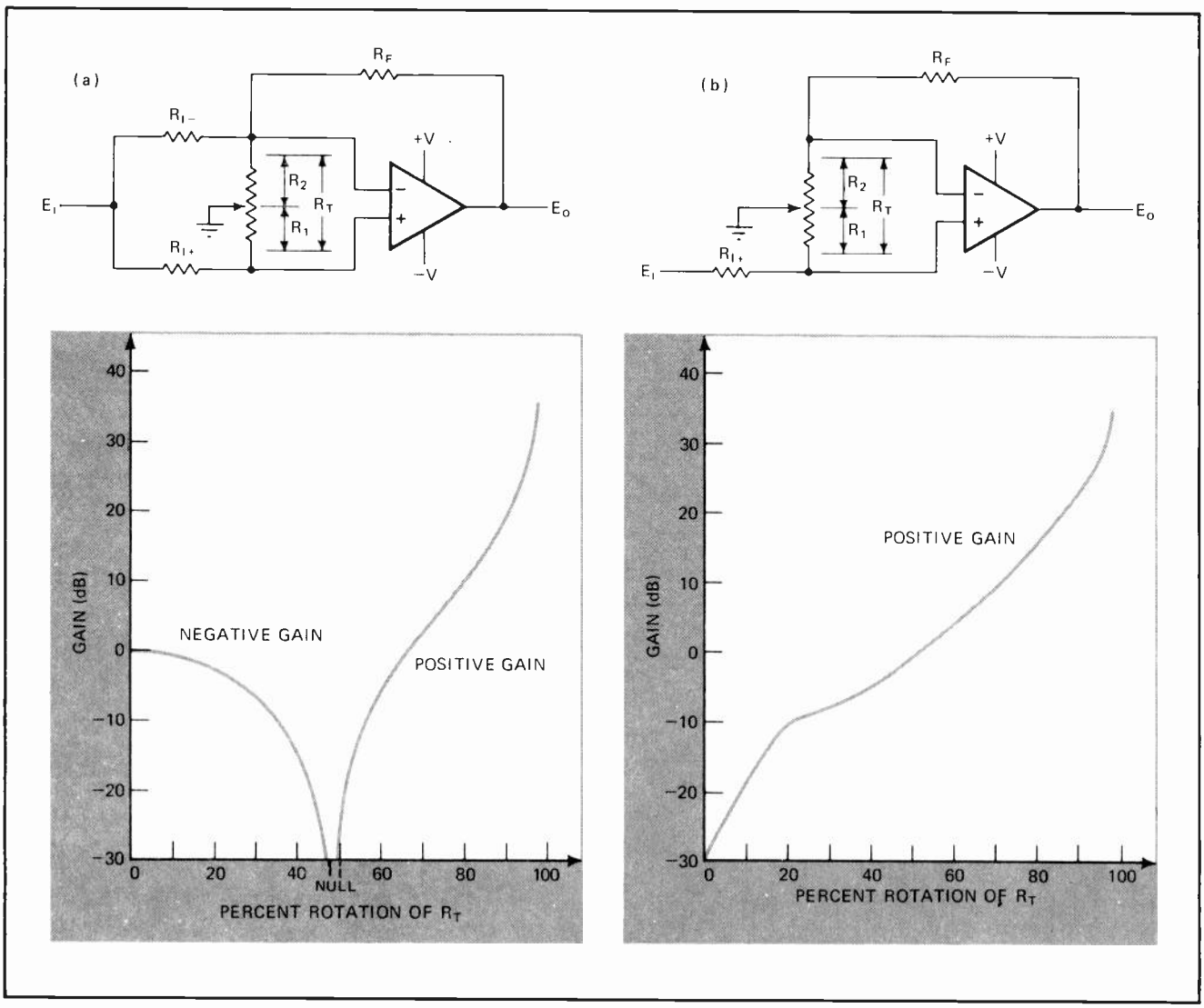
As resistor R_{I-} approaches infinity, op amp gain varies from null to positive infinity only, as illustrated in (b). The equation for output voltage becomes:

$$E_o = [E_i R_F/(R_{I+} + R_1)][(R_1/R_2) + (R_1/R_F)]$$

As can be seen from the figure, the gain curve for this circuit is nearly logarithmic.

For a potentiometer rotation of 10% to 90%, amplifier gain can be varied over four decades. The gain at 50% rotation is the ratio $(R_f + R_2)/(R_{I+} + R_1)$. Any general-purpose differential op amp can be used in the circuit. □

Wide-range gain adjustment. Potentiometer varies gain of operational amplifier (a) from chosen negative value to positive open-loop value. Null point can be shifted by changing resistance ratio of noninverting input resistor R_{I+} to inverting input resistor R_{I+}. Removing R_{I+} permits positive gains to be controlled over wide range, as shown in (b). Circuit's input impedance remains high over full gain range.



Logic driving gates double as d-a converter switches

by Amos Wilnai
Monolithic Memories Inc., Sunnyvale, Calif.

The design of a weighted-resistor digital-to-analog converter can be simplified by using the gate that supplies the digital input data as a switch. This approach permits a high-resolution converter to be built with standard open-collector logic. With 1% resistors, five-bit resolution is possible; tightening the tolerance to 0.1% can provide seven-bit resolution on selected units.

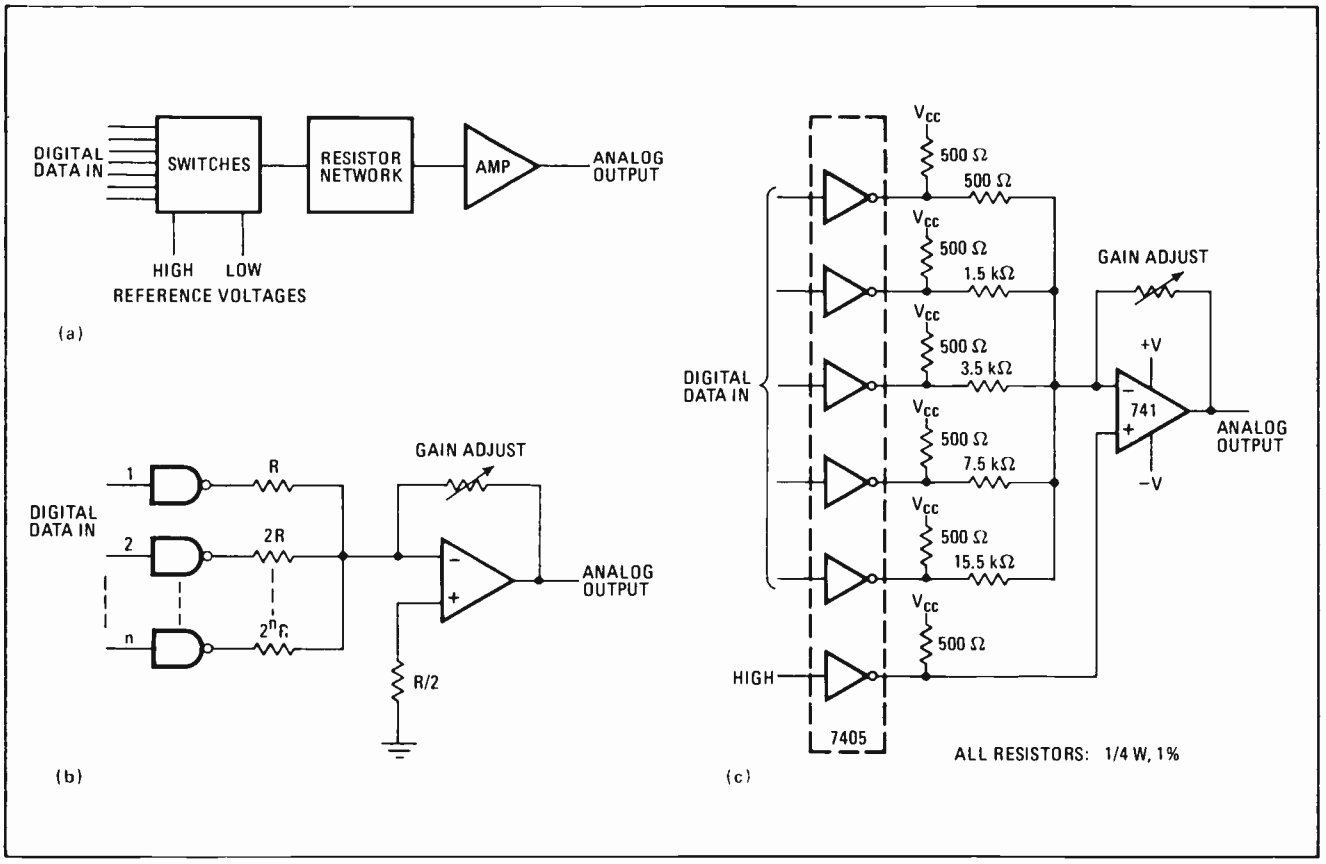
A d-a converter (a) usually contains input switches, a resistor network, and an operational amplifier that provides gain and a low-impedance analog voltage output. The digital input data is generally supplied at standard logic levels—for example, at transistor-transistor-logic levels or diode-transistor-logic levels. Logic gates driving the converter can therefore be used as its input switches (b).

Individually packaged gates, however, limit output word length to about two to three bits because of the marked gate-to-gate variation in logic low and logic high output levels. A TTL high, for instance, is guaranteed to be between 2.4 and 5 volts, while a low lies between 0 and 0.4 V. Output resistance also varies considerably from unit to unit. Excellent voltage-level tracking can, however, be obtained by using gates that share a common substrate if they are operated under the same load conditions. A five-bit converter (c) can be built with an open collector hex inverter performing the input switching function.

When the outputs of the open-collector gates are low, each gate has a load impedance of 500 ohms, and the collector-emitter saturation voltages of the gate output transistors are within millivolts of each other. When the outputs are high, each output transistor is off and the resistor network is referenced to supply voltage V_{CC}.

Longer output word lengths can be realized in the same way by utilizing two hex inverter packages. There may be some variation between packages in the low gate output voltage level, but this can be minimized by selecting the two packages from the same lot (by using the date code on the package). □

Let gates do the switching. Basic digital-to-analog converter (a) requires input switching network to interface digital input data. Using individual logic gates (b) to drive and switch converter limits resolution. However, up to five-bit word lengths can be obtained with open-collector hex inverter (c) as driving and switching network. Because inverters have common substrate, voltage-level tracking is good.



TTL gates speed up pulse-height analysis

by Joseph Laughter
University of Tennessee Medical Units, Memphis, Tenn.

Being used mainly for analyzing nuclear energy, determining white-noise amplitude, or counting blood cells, pulse-height analyzers require high-speed performance. They are complicated to design with discrete transistors. But with transistor-transistor logic and integrated comparators, fast operation can be realized at a fraction of the usual cost.

Positive dc voltage E_L is the lower limit for a pulse passing from input to output, and positive dc voltage E_U is its upper limit. At the instant the input pulse rises above E_L, lower-level comparator A_1 switches to zero, triggering monostable multivibrator OS_1. The output of OS_1 returns to zero after about 300 nanoseconds and triggers monostable OS_2, sending a 60-ns pulse to the anti-conic gate. The anti-conic gate inverts the pulse and triggers the output pulse shaper (monostable OS_3).

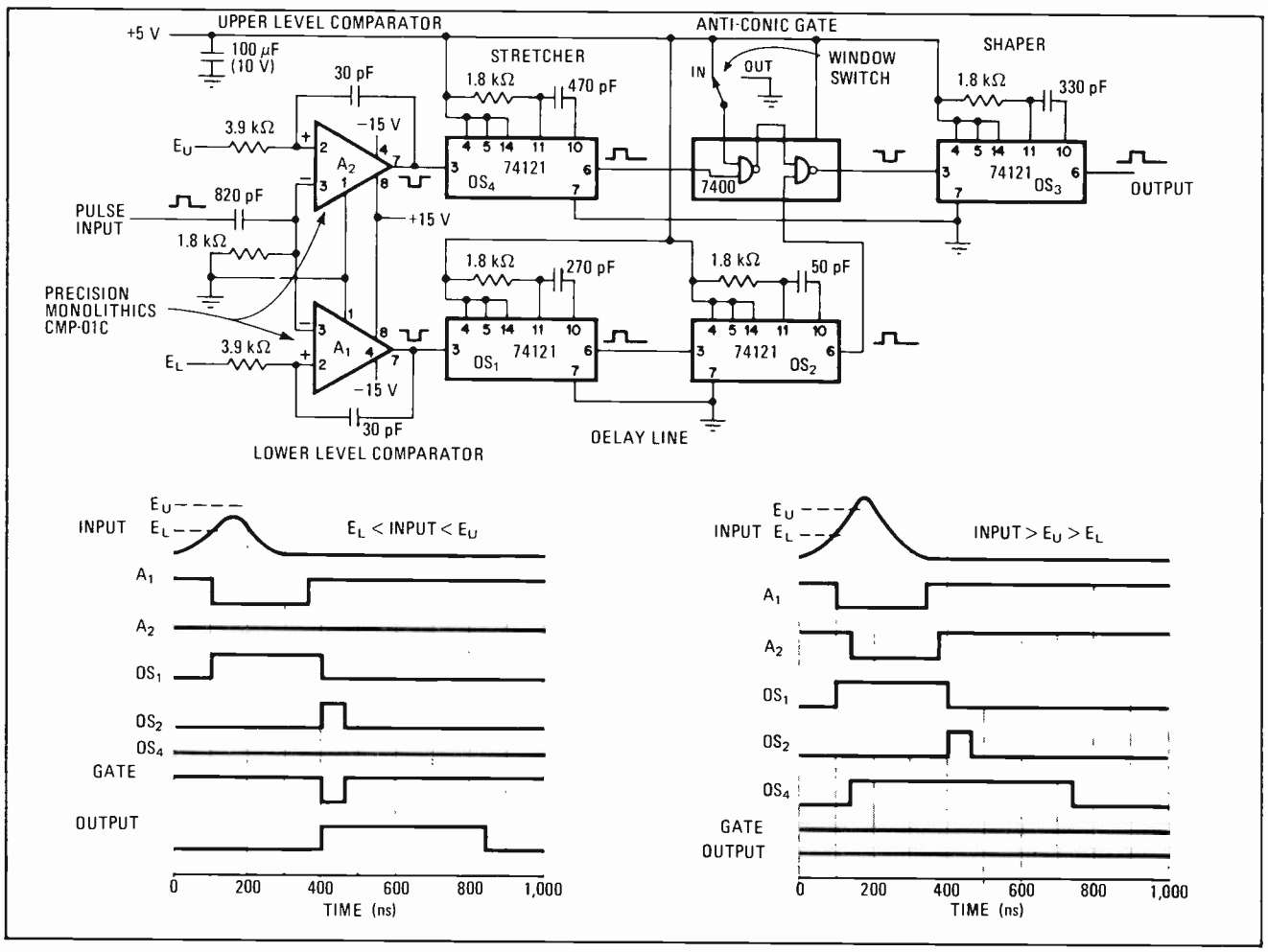
When input pulse height is greater than E_U, comparator A_1 is fired first, and then upper-level comparator A_2 is fired. Once A_2 switches on, the pulse stretcher (monostable OS_4) produces a positive pulse that turns off the anti-conic gate for 600 ns. Therefore, when the pulse from monostable OS_2 appears several nanoseconds later, it is blocked by the anti-conic gate and there is no output. Throwing the window switch to its "out" position disables the anti-conic gate, allowing a pulse to reach the output each time the input pulse exceeds the lower-level limit voltage.

This pulse-height analyzer can accept positive pulses having a maximum rise time of 250 ns and a maximum repetition rate of 500,000 pulses per second. The repetition rate can be increased by using lower-value timing capacitors for delay line OS_1, output pulse shaper OS_3, and pulse stretcher OS_4. However, input rise time requirements become more stringent.

The type CMP-01C comparators can be replaced by the more popular type 710 comparators if the supply voltage is changed from ±15 volts to +12 and -6 v. Although the type 710 is considerably cheaper, it does not perform as well in critical applications.

Timing curves show output wave forms for several important points in the circuit. □

Examining pulse height. Comparators A_1 and A_2 set lower (E_L) and upper (E_U) voltage limits. When pulse height exceeds E_L, one-shots OS_1 and OS_2 slow down pulse from A_1 and transmit it to anti-conic gate, which fires output pulse shaper OS_3. When input exceeds E_U, A_1 and A_2 switch, causing pulse stretcher OS_4 to turn off gate so that pulse from OS_2 cannot reach output. Window switch at "out" disables gate.



Analog voltage sensor controls LED threshold

by Thomas Mazur
Motorola Semiconductor Products, Phoenix, Ariz.

Most light-emitting diodes are found in alphanumeric displays and optically isolated circuits where they are usually controlled, either directly or indirectly, by digital logic systems. Analog LED control circuits can also be useful, provided that distinct light/dark LED transitions can be obtained. The scanning circuit in the diagram employs silicon unilateral switches, which function like four-layer diodes but have a gate control to produce sharp LED transitions for voltage-level sensing applications.

There are N circuit sections, depending on the number of voltage levels to be sensed. Each section consists of a LED, a silicon unilateral switch, a zener diode, a bipolar transistor, and two biasing resistors. The unilateral switch begins to conduct when its terminal voltage reaches a critical level, nominally 8 volts. Once the switch is turned on, its terminal voltage decreases to approximately 1 V.

While switch voltage is increasing, the LED and the transistor's base-emitter junction become forward-biased. LED current, which is limited by the emitter resistor, rises until the unilateral switch conducts. Since the transistor junction and the LED require around 2 V to be forward-biased, the LED shuts off when the switch voltage drops to 1 V.

Whether the switches are on or off, the voltage across the transistors continues to increase with rising input voltage. Because the transistors are separated by zener diodes, each succeeding section operates only after input voltage V_i increases by zener voltage V_Z. Therefore, accurate LED turn-on levels (V_D) can be set and, with the switches providing an abrupt turnoff, incremental control of each LED can be achieved.

Assuming that all the zeners have identical voltage ratings:

$(V_i)_{MIN} = V_{Z1} + V_{EB1} + V_{D1}$

$(V_i)_{MAX} = NV_Z + V_S$

where V_{EB} is transistor emitter-base junction voltage, and V_S is the critical voltage level of the preceding unilateral switch.

The LEDs may be operated sequentially or in an overlapping fashion by varying the type of zener used in each section. For a sequential mode:

V_S is less than or equal to $V_Z + V_{EB} + V_D$

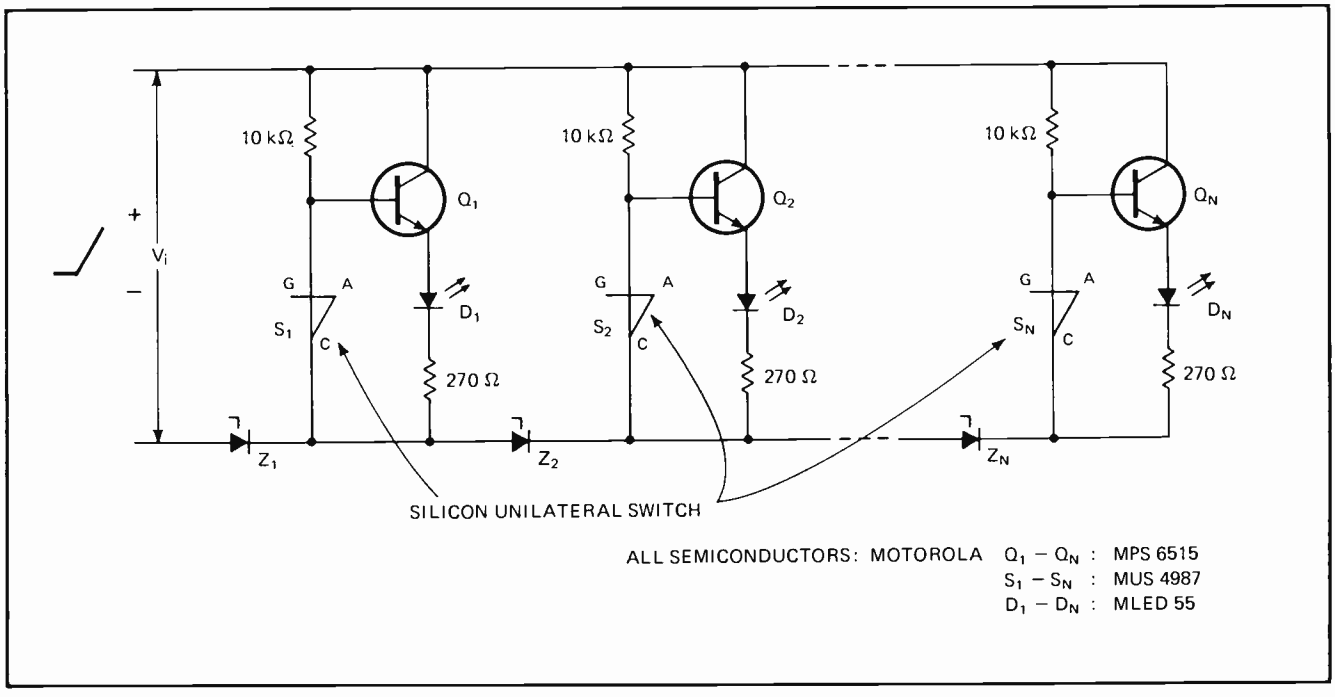
For an overlapping mode:

V_S is greater than or equal to $V_Z + V_{EB} + V_D$

In addition, the level of V_S may be reduced by connecting a zener diode between a switch's gate and cathode terminals.

The scanning circuit may be modified to provide highly discernible visual indication by replacing the emitter resistors by constant-current sources. This supplies the LEDs with uniform current pulses, allowing each one to produce a constant light output. Another modification permits the circuit to serve as a data transfer mechanism—phototransistors can be inserted between the LEDs and the emitter resistors so that the LEDs can be optically modulated. □

LED scanning circuit. Silicon unilateral switches S_1 through S_N require 8 volts to trigger, but only 1 V to stay on. Rising input voltage forward-biases transistor Q_1 and light-emitting diode D_1. LED emits light until switch S_1 conducts; it goes dark abruptly when switch voltage drops to 1 V. Zener diodes Z_1 through Z_N establish voltage levels that are sensed by each section of scanning circuit.



ALL SEMICONDUCTORS: MOTOROLA
$Q_1 - Q_N$: MPS 6515
$S_1 - S_N$: MUS 4987
$D_1 - D_N$: MLED 55

Wired-OR DTL gates increase multiplexer input capacity

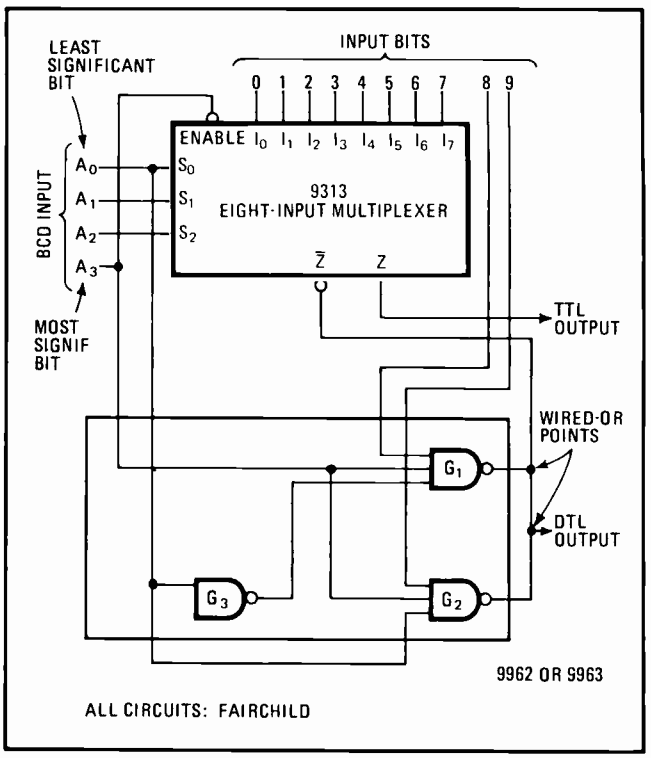
by Eric G. Breeze
Fairchild Semiconductor, Mountain View, Calif.

A 10-input multiplexer can be built by adding only one diode-transistor-logic gate package to an eight-input multiplexer that has an open-collector output. Decade multiplexers are not currently available as standard integrated circuits because of the lead constraints of conventional dual-in-line packages. Either an eight-input multiplexer in a 16-lead DIP or a 16-input multiplexer in a 24-lead DIP can be purchased. And modifying the 16-input unit is both an expensive and cumbersome way to build a decade multiplexer.

Only three DTL gates are needed to add two input bits to an eight-input multiplexer, provided the multiplexer has an open-collector output that can be wired-OR like all standard DTL gates. The decade multiplexer illustrated makes use of the OR tie facility of the $\bar{Z}$ output of Fairchild's type 9313 eight-input multiplexer.

The most significant bit of the binary-coded-decimal control input is connected to the ENABLE (active low) input of the multiplexer and to the inputs of gates G_1 and G_2. When the most significant control bit is low (code value of 0 to 7), the multiplexer operates normally, accepting input bits 0 through 7, and G_1 and G_2 are disabled (their outputs are high).

For BCD input selection codes of 8 or 9, the most significant control bit is high, the multiplexer is disabled, and input bits 8 and 9 can pass to the output, since both G_1 and G_2 are enabled. Gate G_3 performs as an inverter for the least significant control bit into the multiplexer to decode input selection code 8.



Two more bits. Binary-coded-decimal input controls selection of input bits to decade multiplexer. When most significant bit A_3 is low, gates G_1 and G_2 are disabled, and eight-input multiplexer operates normally for input bits 0 through 7. For high A_3 bit, eight-input multiplexer is disabled, but G_1 and G_2 transfer input bits 8 and 9 to output. DTL gates and $\bar{z}$ output are wired-OR.

The type 9313 multiplexer contains an inverter stage after its $\bar{Z}$ output, making both TRUE (Z, TTL-compatible) and ASSERTION ($\bar{Z}$, DTL/TTL-compatible) outputs available. □

Precision integrator resets as it samples

by Dennis J. Knowlton
University of Wyoming, Laramie, Wyo.

A circuit that continuously samples the integral of an input and resets itself achieves an accuracy of within 0.1%. Other integrators with this tight an accuracy can be expensive and complicated because they do not integrate continuously but rather require some time to sample and reset.

The integrator shown uses two sample-and-hold circuits—while one is sampling, the other is holding the previous integral value. Reset is also continuous—the previous value of the integral is fed back so that the circuit is continuously reset for the full integration time period. In this way, integration precision is determined primarily by hardware and not by technique. Adding an offset adjustment to each of the operational amplifiers permits accuracy to be improved by at least an order of magnitude.

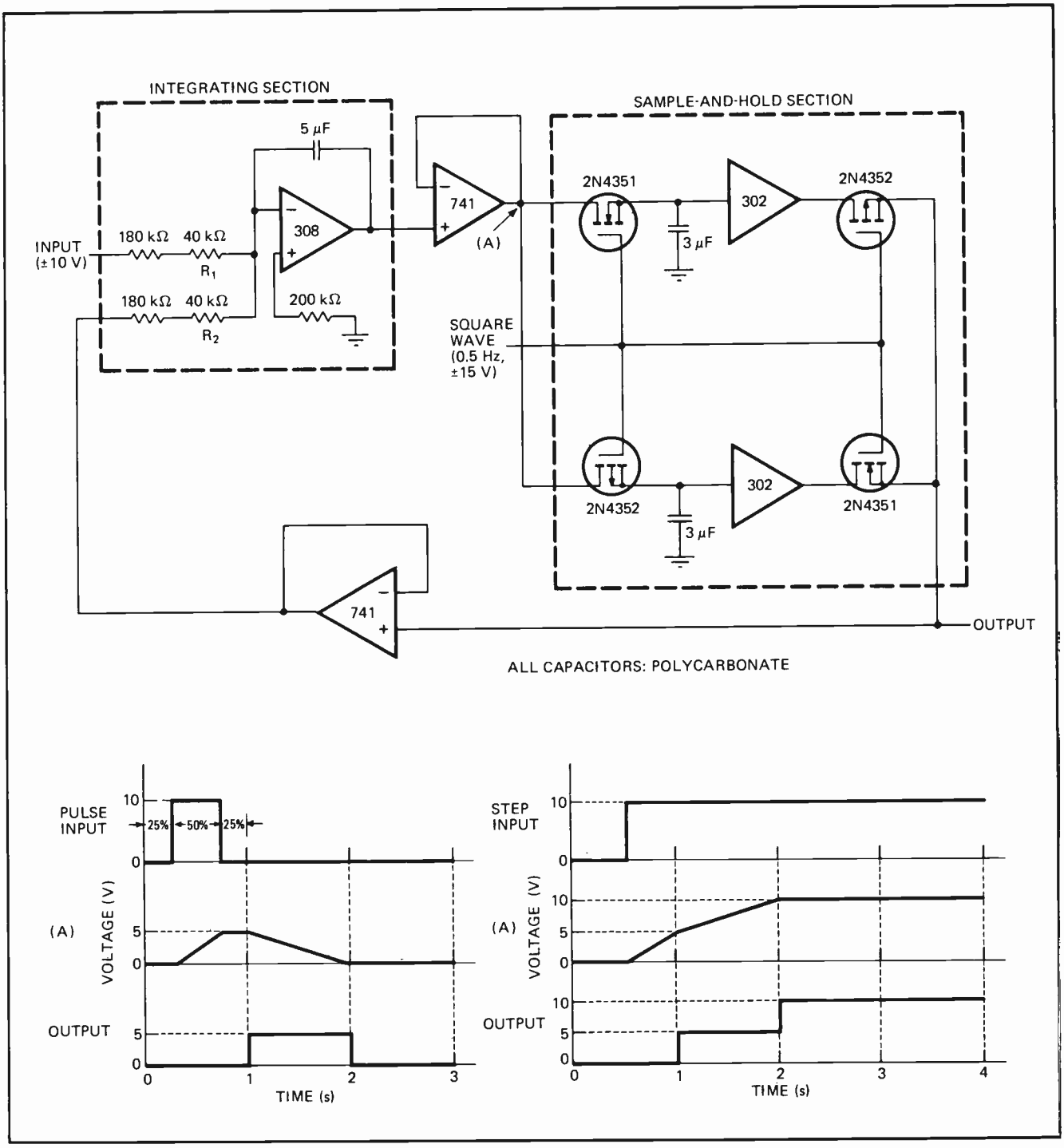
The integrating section is a simple integrator, composed of an op amp having a low input bias current and a feedback capacitor. The sample-and-hold section contains complementary MOSFETs. One portion of this section holds the integral, while the other follows (samples) the output from the integrating section. When the MOSFETs are switched, these roles are interchanged. The

741-type op amps are used in voltage-follower configurations to isolate the integrating section from the sample-and-hold section.

The integrator is a true feedback system. If the integration period is 1 second, the integral formed during a 1-second period is fed back to the input during the following 1-second period to reset the integrator. Meanwhile, new data is being integrated. The output, then, is the sum of the new integrated data, plus the old data that has been integrated back to zero, which simply yields the integral of the new data. Two timing diagrams show the circuit's response to a pulse input and to a step input.

Calibration procedure for the integrator is straightforward. After the feedback circuit is unhooked, resistor R_1 is adjusted to obtain the desired slope from the integrating section (for example, 1 volt out per second per volt in). The feedback circuit is then connected again, and resistor R_2 is adjusted so that there is no overshoot or undershoot to a step input. □

Precision Integration. Simple integrator can provide accuracy within 0.1% because it continuously integrates input. Output from integrating section is sampled by one sample-and-hold circuit, while the other holds previous integral and uses it to reset integrator. Complementary MOSFETs do the switching. Sample-hold roles reverse every integration period.



Wien bridge in notch filter gives 60 dB rejection

by Donald DeKold
University of Florida, Gainesville, Fla.

A modified phase splitter and Wien bridge network form a notch filter that is capable of providing 60 decibels of signal rejection. The bridge network, which consists of two capacitors and two resistors, makes this high rejection possible and allows the filter to be tuned with ganged capacitors or resistors. The three-capacitor, three-resistor bridge ordinarily used for the twin-T variety of notch filter is not as easy to null because more components must be trimmed, and maximum notch depth is usually about 45 dB.

Because of the wideband frequency response of its modified phase splitter, the filter (a) can operate from subaudio frequencies up to hundreds of kilohertz. For very-low-frequency performance, however, a direct coupling scheme must be worked out.

Unlike a unity-gain phase splitter, the filter's phase splitter has a gain of approximately -2 at its collector. If collector resistance is small with respect to resistor R of the bridge, the ac equivalent circuit of (b) can be drawn. The voltage transfer function of the equivalent circuit is:

$$H(s) = V_o(s)/V_i(s) = (s^2C^2R^2 + 1)/(s^2C^2R^2 + 3sCR + 1)$$

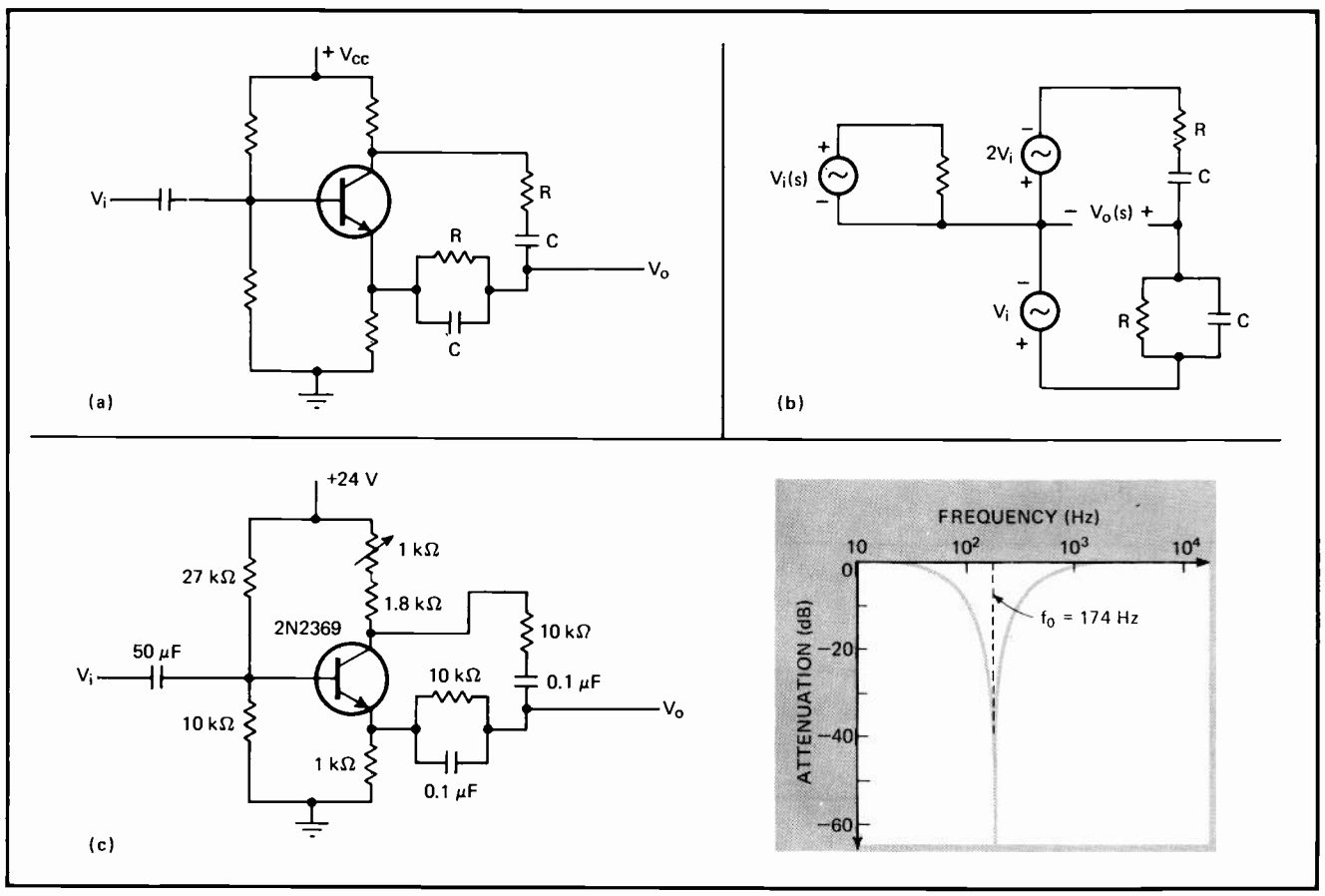
where $s = j\omega$, with ω representing frequency.

This transfer function has a transmission zero at $\omega = 1/RC$, the center frequency of the notch. At frequencies above and below the notch frequency, H(s) approaches unity. Since every R is paired with a C in the expression for H(s), the shape of the transfer characteristic cannot be changed by varying the ratio of R/C. The filter's Q, therefore, is constant for any value of R or C, or at any frequency for which the notch is designed.

A practical implementation of the filter is shown in (c), along with its frequency response. Instead of a single collector resistor, a potentiometer and a series resistor are used so that the filter can be adjusted for maximum signal rejection.

Employing a standard dual ganged variable capacitor for the bridge capacitors allows the notch to be tuned from 8 to 200 kHz. Notch depth may vary because of imperfect tracking of the capacitors, but will never drop below a minimum of 45 dB. Because the filter operates at a high impedance level, it should be shielded to avoid noise pickup at the output node. □

Effective notch. Non-unity-gain phase splitter and four-element Wein bridge make up notch filter (a) capable of suppressing unwanted signals by 60 decibels. Ganged variable components can be used for bridge R or C, allowing notch to be tuned over broad frequency range. Filter transfer function can be found from equivalent circuit (b). Practical filter (c) has adjustable collector resistance.



Multivibrator clock obeys digital commands

by Patrick L. McGuire
General Dynamics, Electrodynamic division, Pomona, Calif.

A simple variable-frequency multivibrator clock source can be made data-dependent by controlling the current into the multivibrator's timing network. When timing resistor values are selected in increments of two (doubling the preceding value), the relationship between binary input and frequency output is linear within 8%.

Inverters with open-collector outputs act as input buffers, providing the necessary pulldown of current from the timing resistors. Diodes are added to prevent signal interference at the inverter outputs.

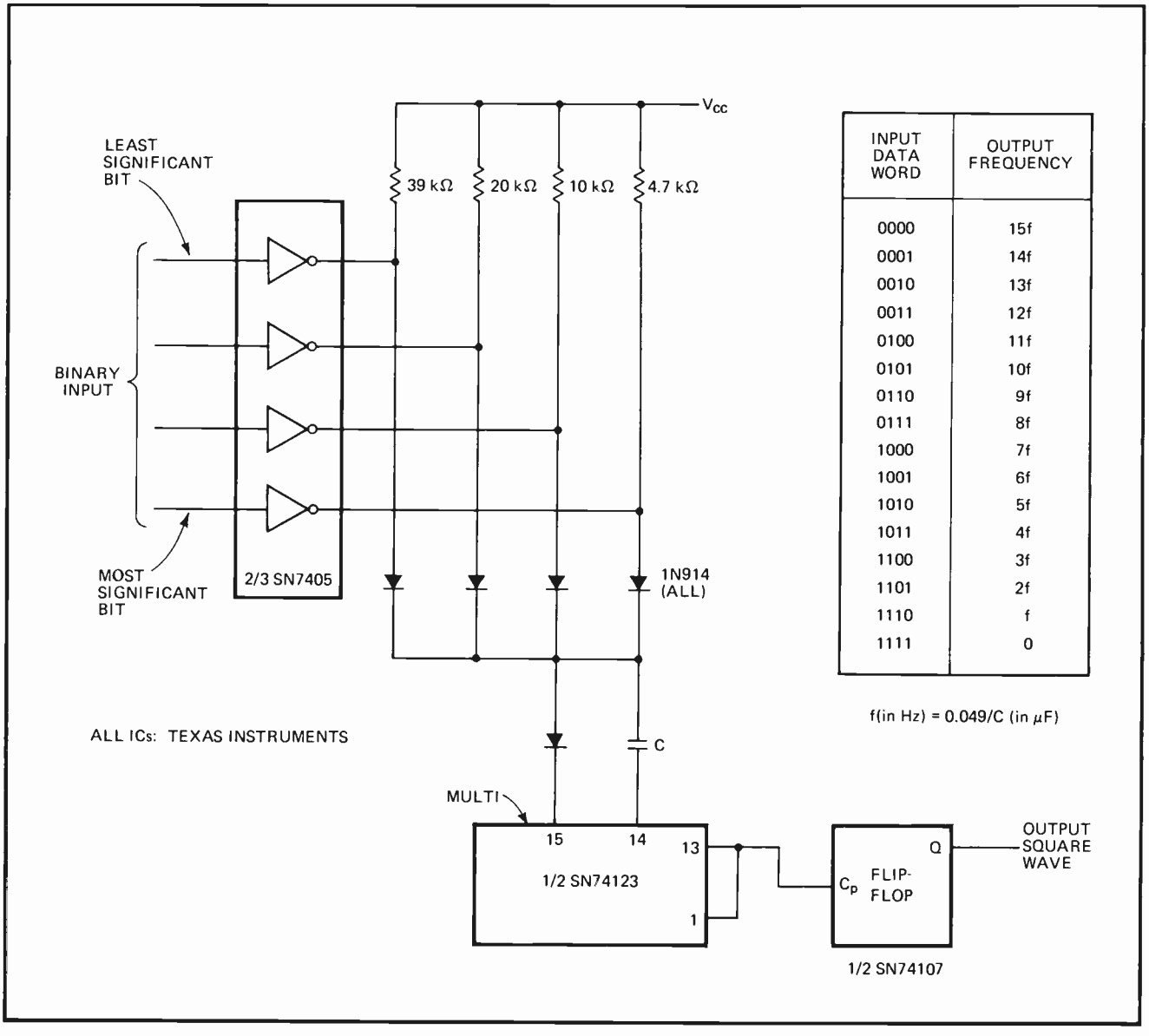
Circuit output is a square wave having a frequency of half the pulse rate from the multivibrator. Output frequency depends on the value of timing capacitor C:

$f = 0.049/C$

where f is in kilohertz and C in microfarads.

The graph shows the multiple of f determined by each input data word. □

Programable clock. Controlling current through multivibrator enables binary input to determine frequency of output square wave. Input/output relationship is practically linear because values of adjacent timing resistors differ by factor of two. Inverters buffer current from timing resistors, while diodes guard against signal interaction between bits. The flip-flop halves output pulse rate from the multivibrator.



INPUT DATA WORD	OUTPUT FREQUENCY
0000	15f
0001	14f
0010	13f
0011	12f
0100	11f
0101	10f
0110	9f
0111	8f
1000	7f
1001	6f
1010	5f
1011	4f
1100	3f
1101	2f
1110	f
1111	0

f(in Hz) = 0.049/C (in μF)

Op amp with feedback makes full-wave rectifier

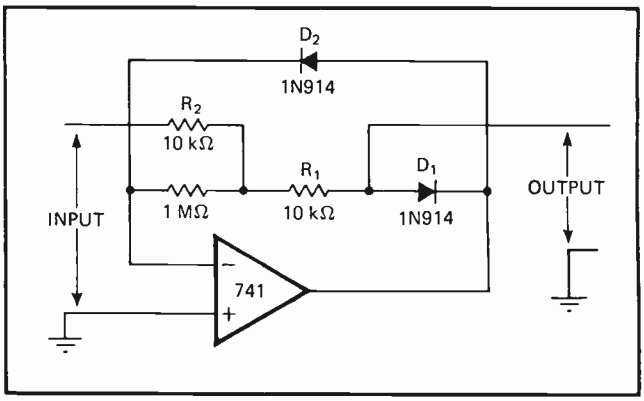
by Richard Knapp and Roger Melen
Stanford University, Palo Alto, Calif.

A feed-forward resistive element allows one operational amplifier to do the job of two op amps—perform full-wave rectification of low-level signals. The resulting circuit is useful for a wide variety of frequency-doubling and small-signal rectification applications, such as ac-to-dc converters, absolute-value detectors, and frequency multipliers.

For both positive and negative inputs, the op amp's inverting input is always at virtual ground. And for either input polarity, output voltage is developed by input current flow through feedback resistor R_1.

Diode D_1 is forward-biased during positive inputs, while diode D_2 remains off. Input current flows primarily through resistor R_1 to the output. During negative inputs, diode D_2 conducts and diode D_1 is off, maintaining the op amp's inverting input at virtual ground.

Circuit output impedance is approximately equal to the resistance of diode D_1 for positive voltages and to the sum of $R_1 + R_2$ for negative voltages. □



Full-wave rectifier. Inverting input of operational amplifier remains at virtual ground for both positive and negative input voltages so that output voltage is always developed by input current flow through feedback resistor R_1. Diode D_1 conducts only during positive inputs, and diode D_2 is on only for negative inputs. Normally, two amplifiers are required to perform full-wave rectification.

Gray-code generator avoids output glitches

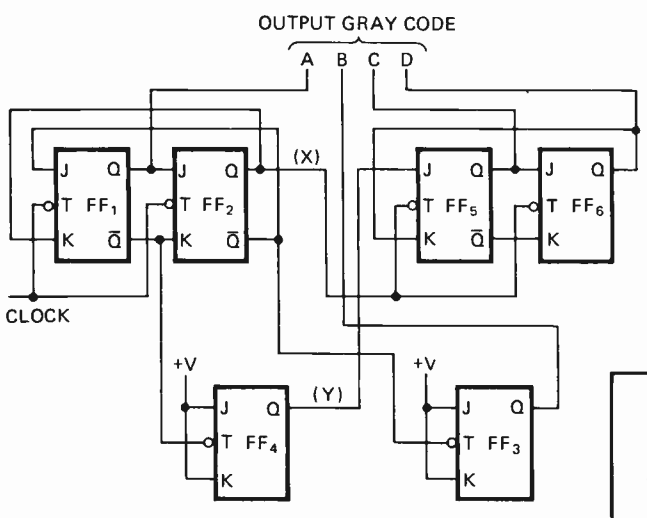
by Carl Moser
Western Electric Co., Winston-Salem, N.C.

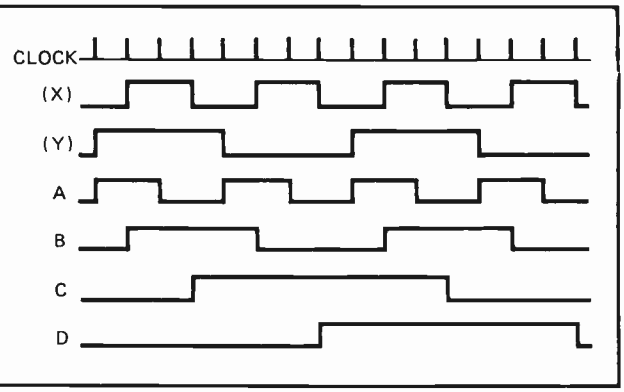
When binary signals are ANDed together, undesirable glitches can be generated at a circuit's output if one or more signal transitions are simultaneous. A Gray-code generator can be built with six J-K flip-flops that are arranged so that only one signal transition occurs at any particular time. Therefore, the four output signals forming the Gray code can be ANDed without glitches.

Flip-flops FF_1 and FF_2 are wired as a Johnson counter. The Q output or FF_1, which is 90° out of phase with the Q output of FF_2, provides the A Gray-code output line. Flip-flop FF_3 is toggled by the $\overline{Q}$ output of FF_2, causing it to produce the B Gray-code output line.

The other three flip-flops, FF_4 through FF_6, form a modified Johnson counter. FF_5 and FF_6 are toggled simultaneously by the Q outputs (labeled X and Y in the diagram) of FF_2 and FF_4. Output lines C and D are generated by FF_5 and FF_6, respectively.

Since the circuit is asynchronous, its maximum operating frequency is limited by the delay of the flip-flops. For correct output code generation, all the flip-flops must be cleared initially. □





Stopping glitches. Output lines of Gray-code generator have no simultaneous signal transitions, permitting them to be ANDed together without creating glitches. Six flip-flops comprise complete generator. FF_1 and FF_2 are connected as Johnson counter, while FF_5 and FF_6 form modified Johnson counter. FF_3 supplies one of the output lines; FF_4 is part of simultaneous toggling scheme for FF_5 and FF_6.

Active filter has separate band and frequency controls

by John Jenkins
Montgomery, Ala.

The bandwidth and center frequency of an active bandpass filter can be controlled independently by two separate resistors. Moreover, the filter's gain remains at unity over its full tuning range. Filter Q range is 2 to 200, while center frequency is 1 to 10 kilohertz.

The circuit shown in (a) has these properties, but it requires a variable inductor, which is usually difficult to tune, can be large, and cannot provide good temperature stability. The transfer function for this LC filter is:

$e_o/e_i = (s/R_1C_1)/(s^2 + s/R_1C_1 + 1/LC_1)$

Replacing the inductor with an active RC network, as illustrated in (b), yields a temperature-stable circuit. If all the components are ideal and $R_2C_2 = R_3C_3$, the equivalent inductance can be expressed as:

$L_{eq} = R_2C_2R_f$ henries

and the 3-decibel bandwidth as:

$BW = 1/(2\pi R_1C_1)$ hertz

and the center frequency as:

$f_o = 1/[2\pi(R_fC_1R_2C_2)^{1/2}]$ Hz

A wide range of component values can be used in the circuit, which is easy to design, once the desired filter specifications are established. As an example, a filter will be designed with a 5-Hz bandwidth, a center frequency of 1 kHz, and a maximum output voltage of 1 volt peak-to-peak. A few important operational amplifier specifications must also be known. Typically, input resistance (R_i) is greater than 40 kilohms, output resistance (R_o) is less than 200 ohms, voltage gain (G_v) is more than 10,000, and output voltage swing (V_{os}) exceeds 20 v pk-pk.

To solve the design equations, let:

$K_1 = (R_fC_1R_2C_2)^{1/2} = 1/(2\pi f_o) = 1.59 \times 10^{-4}$

$K_2 = R_1C_1 = 1/(2\pi BW) = 3.18 \times 10^{-2}$

$K_3 = (R_fC_1/R_2C_2)^{1/2}$

$= [(V_{os2}/e_{omax})^2 - 1]^{1/2} = 19.98$

then the filter's time constants can be computed:

$R_1C_1 = K_2 = 3.18 \times 10^{-2}$

$R_2C_2 = K_1/K_3 = 7.96 \times 10^{-6}$

$R_fC_1 = K_1K_3 = 3.18 \times 10^{-3}$

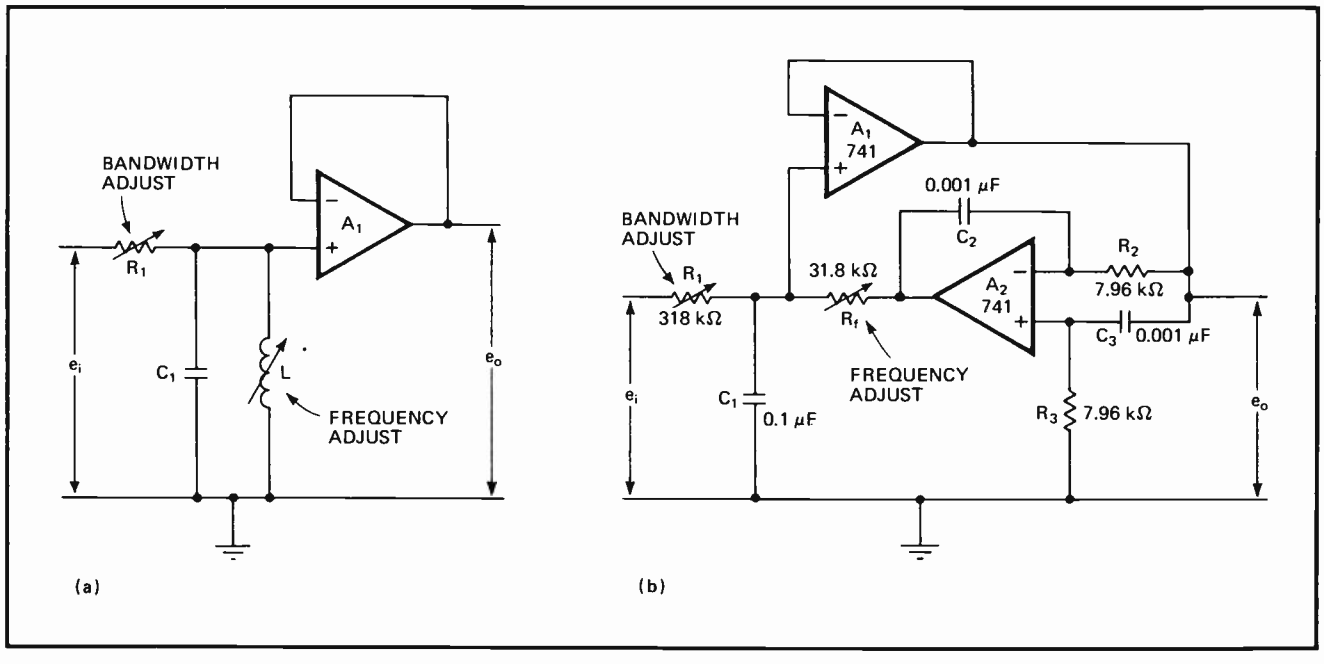
$R_f/R_1 = K_1K_3/K_2 = 0.1$

For most applications, a few simplified guidelines can be followed to choose component values: resistor R_1 should be less than 400 kilohms, resistor R_2 should lie between R_{i2} (about 40 kilohms) and 1 kilohm, the load resistance should be greater than 1 kilohm, and factor $(1 - R_3C_3/R_2C_2)$ should range between 0 and resistance ratio $(R_f/R_1) \times 10^{-2}$.

This last constraint requires that time constant R_2C_2 track R_3C_3 within +0% and -0.1%. Therefore, these resistors and capacitors must have closely matched temperature coefficients and operating temperatures. Metal-film resistors and NPO-type capacitors that are mounted close together can be used. (The R_2C_2 and R_3C_3 time constants can be aligned by first opening the filter's input to obtain maximum Q, then increasing R_3 until oscillation occurs, and then decreasing R_3 until oscillation just stops.)

A set of typical component values is noted in (b). As indicated, resistor R_1 tunes filter bandwidth, while resistor R_f adjusts center frequency. □

Active circuit ousts variable inductor. Bandpass filter (a) offers independent center frequency and bandwidth adjustments. Hard-to-tune variable inductor can be replaced by active circuit (b) that provides an equivalent inductance and better temperature stability. Fully active filter is easy to design and will operate over a broad range of component values. General-purpose amplifiers can be used.



Logic circuit converts synchronous motor to stepper

by Michael D. Doering
Food and Drug Administration, Bureau of Radiological Health, Rockville, Md.

A simple circuit that is compatible with transistor-transistor-logic circuits can convert a two-coil synchronous motor to a synchronous stepping motor. Since circuits that perform this conversion are not available commercially, the designer is usually forced to use relays or come up with his own stepper control circuit.

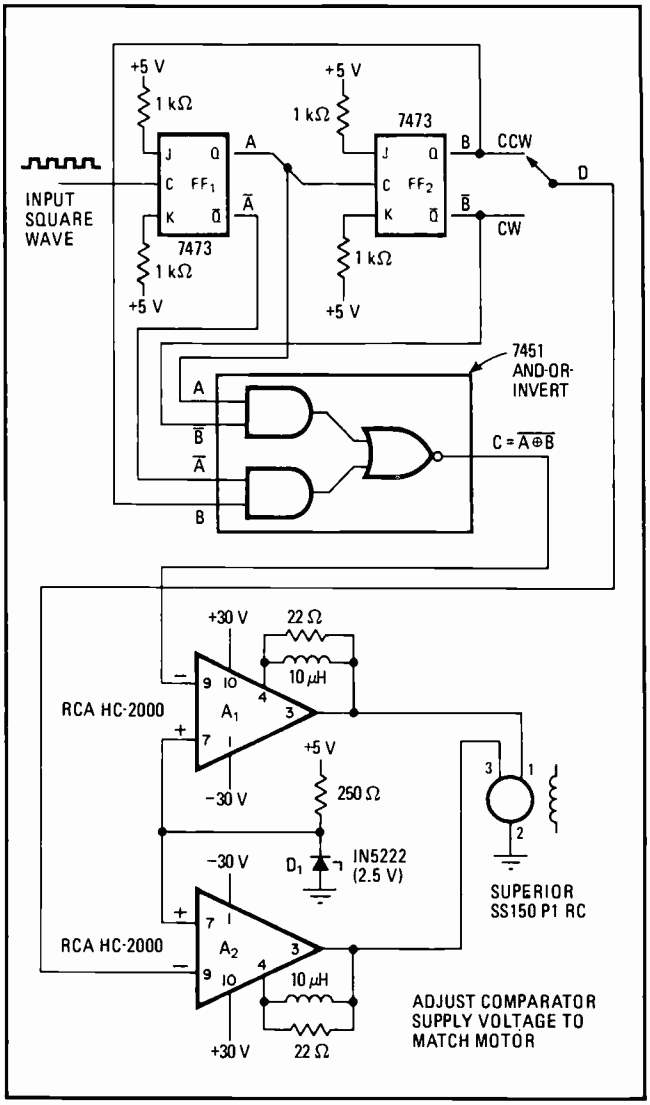
The problem of conversion generally arises when a variable-speed synchronous motor is needed that is capable of delivering up to 1,800 inch-ounces of torque, or when a variable-speed adaptor is required for a motor that is already installed. The converter, therefore, must be a high-current, high-voltage, variable-frequency circuit that can drive a two-phase 115-volt ac motor.

A variable-frequency square wave, which can be supplied by TTL integrated circuits, drives the converter and establishes motor stepping speed. Motor-speed accuracy depends on how accurate the input square-wave frequency is. The size of the step and the maximum stepping speed are determined by the motor used.

Flip-flops FF_1 and FF_2 are connected as a repeating two-bit counter, which has its output decoded by an AND-OR-INVERT circuit. This arrangement provides the four states, which are noted as A, B, C, and D in the diagram, needed to make the motor step properly.

The position of the switch at the output of FF_2 determines the direction of rotation. As can be seen from the figure, the D state simply represents the switch-selected B or $\bar{B}$ states.

Output states C and D are fed to the inverting inputs of high-power comparators A_1 and A_2, respectively. The voltage levels of these two states are then compared to the reference voltage established by the 5-v supply and zener diode D_1. Each comparator drives a separate motor coil and can develop a 75-v 100-watt output. □



Stepping a synchronous motor. Logic circuit plus high-power comparators step two-phase synchronous motor in clockwise or counterclockwise direction. Frequency of input square wave determines motor stepping speed. Two-bit counter formed by flip-flop pair and AND-OR-INVERT circuit produce four logic outputs (A, B, C, and D) that control motor. Each comparator output supplies one motor coil.

Ring counter eliminates false gating signals

by Glen Hamilton
Dickson, Tenn.

A ring counter that performs reliably at speeds up to 7 megahertz can be designed to prevent counting errors caused by false gating signals. Besides being able to clock in either direction (up or down), the counter can be reset from any ring output without losing a clock pulse. Only five dual in-line integrated-circuit packages are needed—a binary counter, a quad latch, a quad NAND gate, and two BCD-to-decimal decoders.

When the input clock pulse rises to logic 1, the binary counter is incremented up or down, depending on the position of switch S_1. The unused clock input to the binary counter must be held continuously at logic 1. For most applications, switch S_1 can be eliminated because only one clock direction is required. To switch between the two clock inputs, two gates must be added so that

the unused connection is always held at logic 1.

With the transition of the input clock pulse from logic 1 to logic 0, the binary counter outputs are loaded into the latches. The next clock pulse enables the NAND gates, allowing the $\bar{Q}$ signals from the latches to pass to the decoders, which then select the appropriate ring output to be enabled. Each succeeding clock pulse sequentially steps and enables the decoder outputs.

The number of stages in the ring is determined by the ring output at which switch S_2 is placed to implement the reset function. When the ring output tapped by switch S_2 is enabled, the binary counter is set to the number appearing at its preset input lines. These preset inputs can be either hardwired or made selectable.

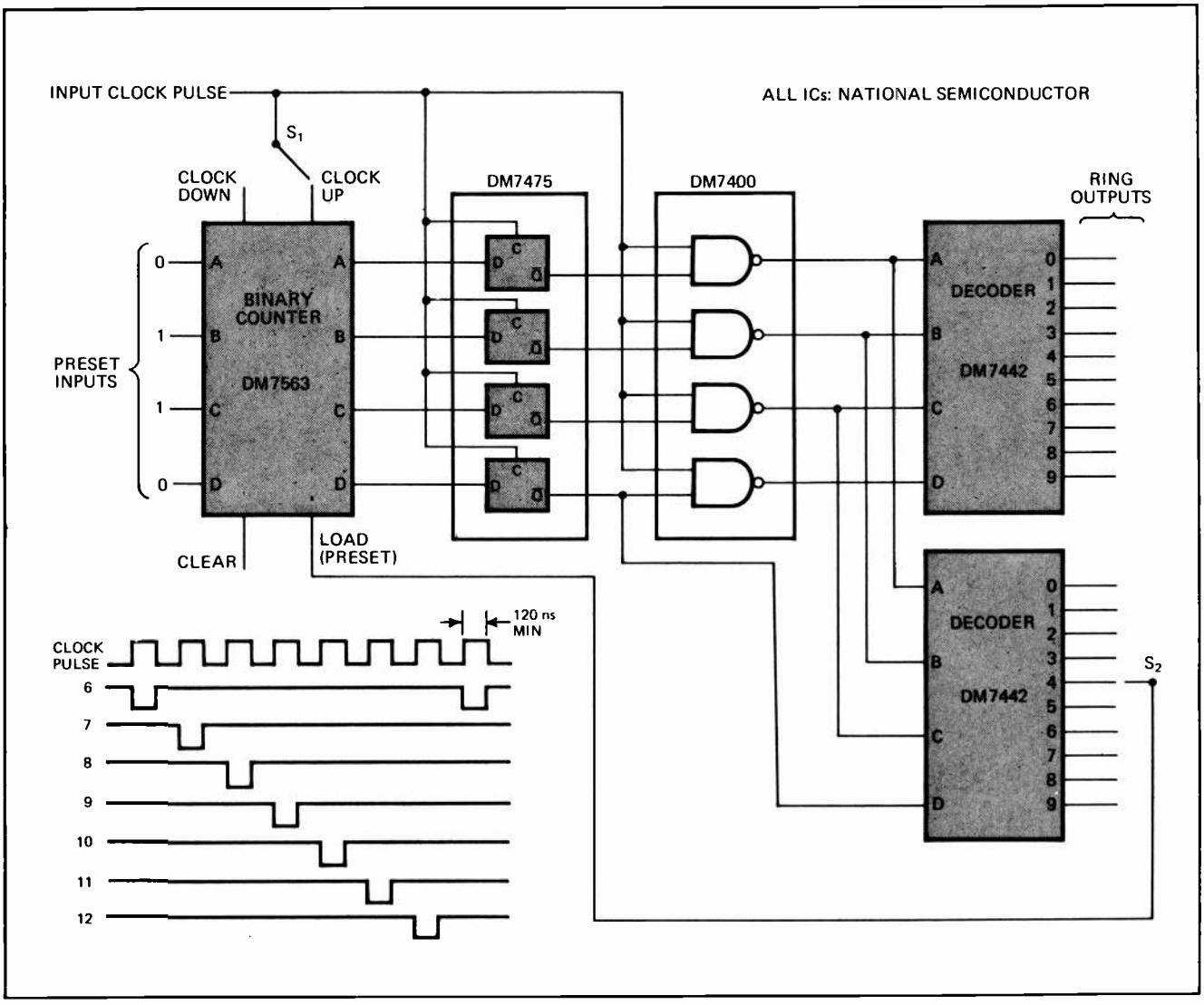
For the wiring connections shown, the binary counter has the binary number six continuously held at its preset inputs, and the ring counter's reset function is placed at the fourth output line of the second decoder. This hookup resets the binary counter to six each time the twelfth ring output is enabled, causing the ring counter to step sequentially from six to 12 and then repeat, as indicated by the waveforms in the timing diagram.

All ring outputs are disabled (in the logic 1 state) when the input clock pulse is logic 0. During this time, the ring outputs are inhibited by the NAND gates to prevent false gating due to transients. Also, all ring outputs are always 180° out of phase with the input clock pulse, and a transition from logic 1 to logic 0 is required to reset the ring counter. This means that the ring counter will be reset only when the ring output selected by switch S_2 is enabled (in the logic 0 state).

The circuit can also be used as a frequency divider that has its output pulse frequency determined by the width of the input clock pulse. Any integral divisor, from 2 to 15, can easily be selected by switch S_2. The divided frequency may be taken from any of the ring outputs.

The binary counter is provided with CARRY TO and BORROW FROM pins, permitting counters to be cascaded for generating more than 15 outputs. With two binary counters, up to 256 outputs can be produced, as long as an appropriate number of decoders is used. □

Sure-clocking ring counter. Input clock pulses sequentially step data through binary counter to latches (flip-flops) to NAND gates to BCD-to-decimal decoders. Switch S_1 permits clocking up or down, while switch S_2 selects number of stages in ring. S_2 also carries reset signal that sets binary counter to its preset input number. Counting proceeds only for clock transition from logic 0 to logic 1.



Complementary output stage improves op-amp response

by Robert Gagnon and Richard Karwoski
Raytheon Co., Equipment division, Sudbury, Mass.

The performance of a conventional 741-type operational amplifier can be considerably enhanced if it's given a complementary-transistor output stage. The op amp's gain-bandwidth product is extended from its normal 1 megahertz to 7.5 MHz for a 250-ohm load resistor, while slew rate is increased from 0.5 to 5 volts/microsecond. Similarly, the full-power bandwidth reaches 50 kilohertz, as opposed to 15 kHz, and the bandwidth at a voltage gain of -2 becomes 2.5 MHz, rather than 330 kHz.

The output stage (a), which contains transistors Q_1 and Q_2, acts as a current buffer, providing extra load drive capability. It is basically a bootstrap configuration using degenerative feedback. Transistor Q_2 is the principal source of load current, and the stage's dynamic input impedance is the product of the load resistance and the current amplification factors of both Q_1 and Q_2.

The two outboarded transistors form two complementary pairs with the output transistors inside the op amp—outboarded transistor Q_1 complements internal transistor Q_3, while Q_2 complements Q_4. This configuration (b) makes it possible to keep voltage gain independent of output load conditions and to be determined by a resistance ratio:

$$e_o/e_i = R_2/R_1$$

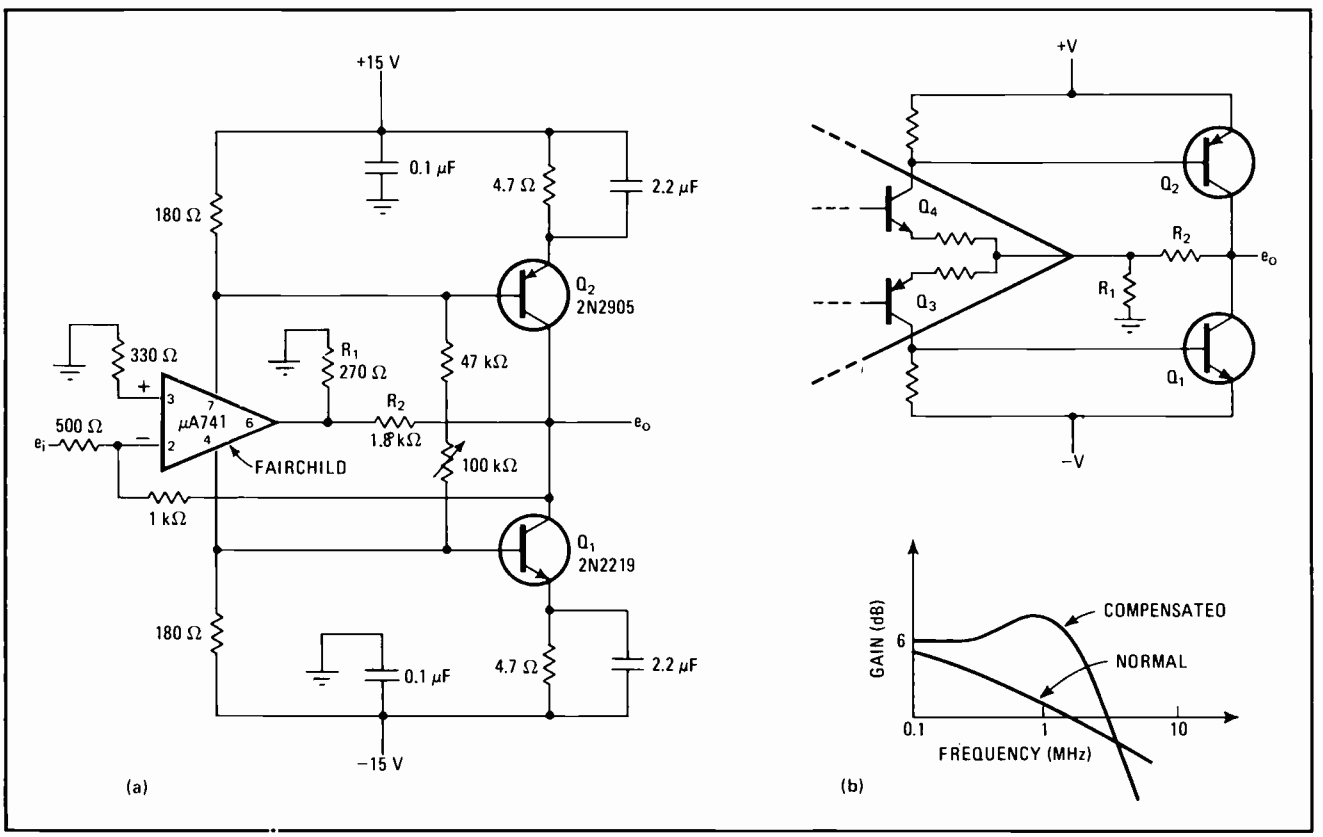
where R_1 is the load resistance for the op amp, and R_2 is the input resistor to the output stage.

If $R_2/R_1 = 10$, the op amp output voltage swing need only be ±1 V to realize a circuit output voltage swing of ±10 V. In practice, a resistance ratio of 6.7, with $R_1 = 270$ ohms, yields the best over-all results because of how the op amp responds to this load resistance value.

For a load resistance of around 300 ohms, the op amp's maximum output voltage swing is reduced by about 30%, but its slew rate remains approximately 0.5 V/μs for small voltage excursions. By fixing the gain of the output stage at about 10, the slew rate of the overall circuit is increased by a factor of 10, and the op amp's frequency response is extended.

Undesirable high-order effects of the 741-type op amp are far enough beyond its nominal 1-MHz crossover frequency that instability due to the gain added by the output stage is not a problem. A 100-kilohm cermet potentiometer is included in the circuit to permit cancellation of crossover effects. It should be adjusted at the full-power bandwidth limit—50 kHz and a maximum output voltage of 20 V peak-to-peak. □

Boosting op amp performance. Output stage (a) multiplies op amp slew rate by 10 and extends crossover frequency to 7.5 megahertz. As shown in (b), external transistors Q_1 and Q_2 complement internal transistors Q_3 and Q_4, respectively. Resistor R_1 acts as op amp load resistance so that resistance ratio R_2/R_1 fixes overall circuit gain. Additional gain lets op amp operate at low output voltage.



Generator independently varies pulse rate and width

by Mahendra Shah
Univ. of Wisconsin, Space Science and Engineering Center, Madison, Wis.

Capacitor charging current can be used to change the output frequency of a voltage-controlled pulse generator that also offers an independent control over output pulse width. The generator's output-pulse frequency can range from 1 to 75 kilohertz and output pulse width from 100 nanoseconds to 18 seconds. A dual retriggerable one-shot performs the actual pulse generation, while an operational amplifier and a couple of transistors convert the control voltage into a proportional charging current for the frequency timing capacitor.

The voltage divider created by resistors R_1 and R_2 determines the voltage level at the noninverting input of the op amp. Since the op amp and emitter-follower Q_1 form a unity-gain buffer having a high input impedance, the large open-loop gain of the op amp keeps the noninverting input voltage (V_1) equal to the inverting input voltage (V_2):

$$V_1 = V_2 = [R_2/(R_1+R_2)]V_i$$

and Q_1's emitter current becomes:

$$I_{E1} = V_2/R_3$$

Both V_1 and V_2 can range between 0 and 2 volts.

Transistor Q_1 has a minimum h_{FE} of 250, making its base current much smaller than its collector current so that constant current I_{C1} is maintained nearly equal to constant current I_{E1}. Because transistor Q_2 is also a large-h_{FE} device, it draws very little base current and almost all of I_{C1} passes through resistor R_4 and diode D_1.

Furthermore, the base-emitter voltage of Q_2 and the forward voltage drop of D_1 are about the same, permitting voltage V_3 to be written as:

$$V_3 = R_4 I_{C1}$$

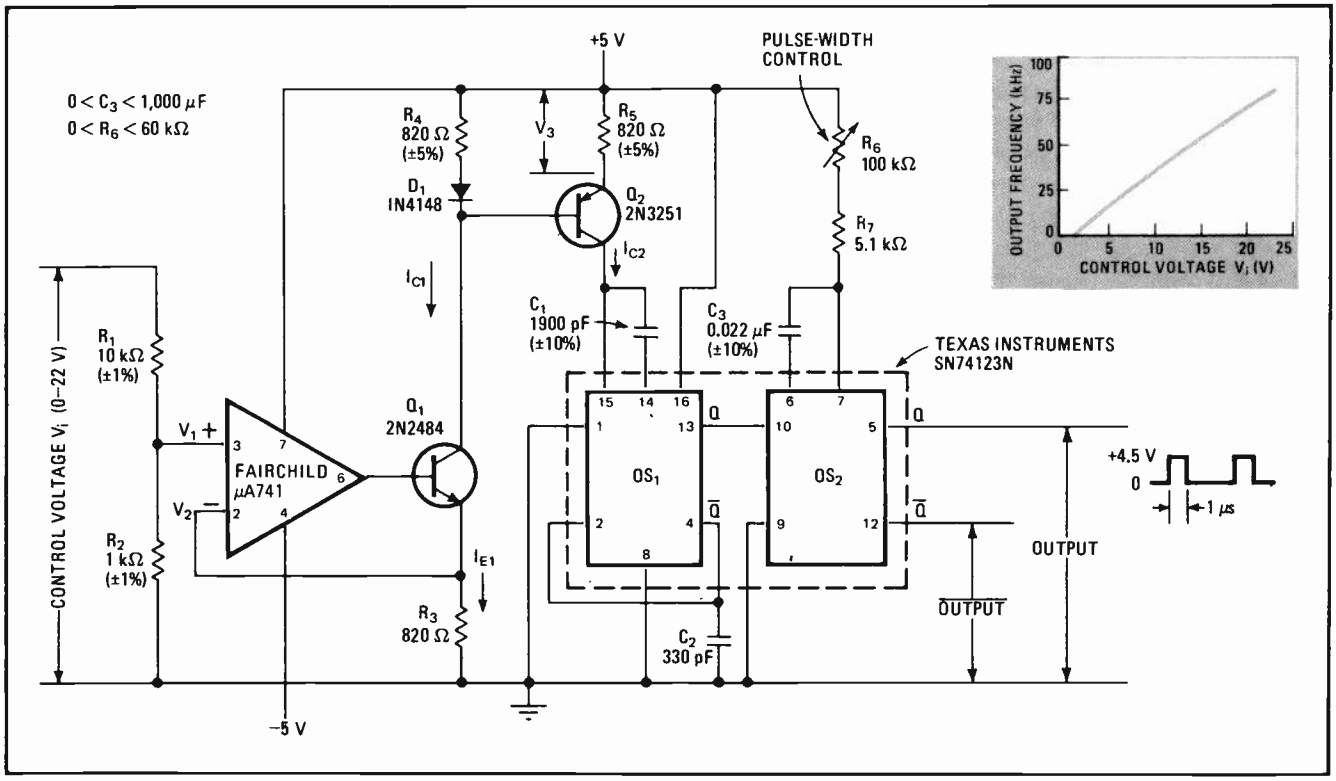
And the constant charging current, I_{C2}, for timing capacitor C_1 can be expressed in terms of voltage V_1:

$$I_{C2} = R_4 V_1/R_3 R_5$$

One-shot OS_1 can be retriggered during its on state within 100 nanoseconds of the end of the timing period, fixed by its timing components. The positive trigger input of OS_1 is connected to its $\bar{Q}$ terminal, and a small capacitive load (C_2) is added at the $\bar{Q}$ terminal to increase the retriggering delay by about 20 ns.

At the end of OS_1's timing cycle, its Q output makes a high-to-low transition, and its $\bar{Q}$ output makes a slightly delayed low-to-high transition, retriggering OS_1 back into its on state for another timing period. This cycle repeats at frequency f:

Voltage-variable rep rate. Input control voltage determines output frequency of pulse generator. Collector currents developed by transistors Q_1 and Q_2 are directly proportional to control voltage V_i. Constant current I_{C2} charges timing capacitor C_1, controlling pulse frequency of one-shot OS_1, which is retriggered by its own $\bar{Q}$ output. OS_1's Q output triggers one-shot OS_2, which controls output pulse width.



$f = 1/(T_1 + 60\ ns)$

where T_1 is OS_1's on-time. One-shot OS_2 is triggered by the low-to-high transitions of OS_1's Q output; these transitions generate positive-going pulses at OS_2's Q output. The width of OS_2's output pulses is controlled independently by resistors R_6 and R_7 and capacitor C_3.

Timing period T_1, which is usually much greater than 60 ns, is inversely proportional to voltage V_1. The circuit's output pulse frequency is almost linearly proportional to voltage V_1 and, therefore, to control voltage V_i. The graph shows that the pulse generator's frequency is practically linear over the control voltage range of 5 to 22 v (0.45 to 2 v for V_1).

Generator frequency range can be extended to higher or lower frequencies by scaling the value of capacitor C_1, but this capacitor's charging current, I_{C2}, should not be made greater than a few milliamperes. Voltage control of output pulse width can be obtained by replacing resistors R_6 and R_7 with a voltage-controlled constant-current source. □

Photodetector senses motion in noisy surroundings

by Richard T. Laubach
National Cash Register Co., Cambridge, Ohio

A digital phototransistor amplifier, consisting of a few readily available inexpensive components, can detect slowly moving objects in an electrically noisy environment. The circuit works reliably, even if long cables link its optical sensing section to its amplifying section.

The circuit detects objects that break the light beam between the light-emitting diode and the phototransistor. When the light beam is interrupted, transistor-output voltage V_1 increases, causing the potential at point A to rise until the threshold voltage (about 8 volts) of inverter I_1 is reached.

Both inverters I_1 and I_2 then switch, and voltage V_2 jumps from 0 to 12 v. This voltage jump supplies additional current at point A through feedback resistor R_f, reducing the pull-up resistance seen by the phototransistor so that voltage V_1 jumps from 8.5 to 11 v when voltage V_2 makes its low-to-high transition.

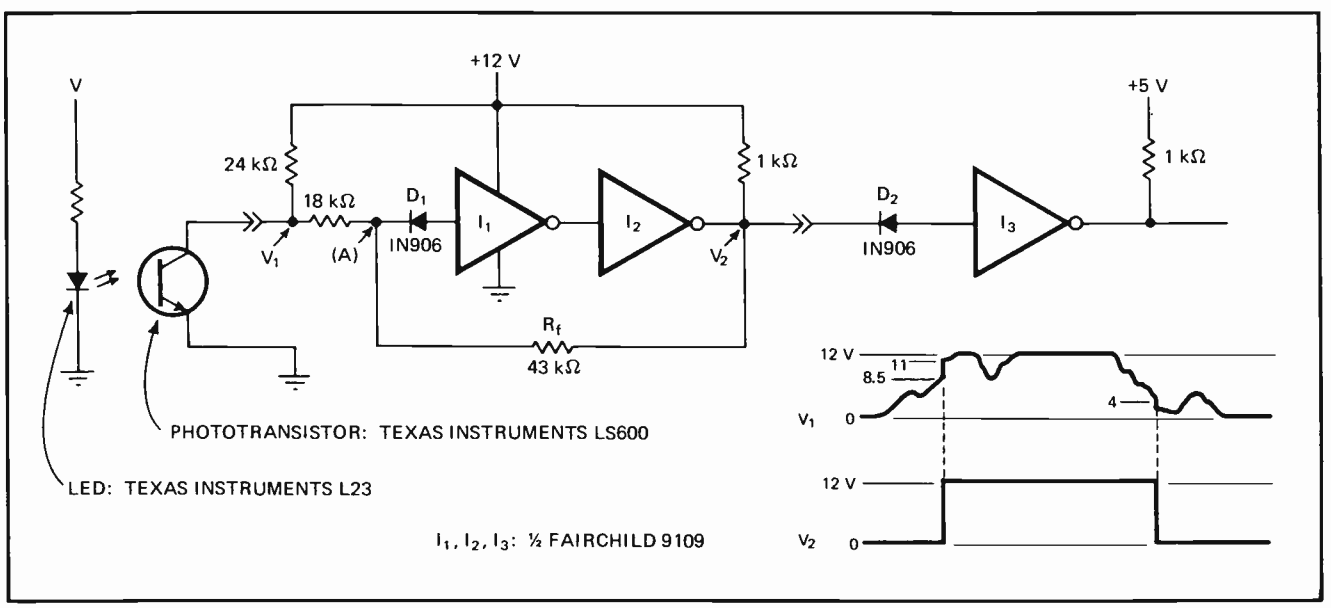
Besides protecting the input of inverter I_1, diode D_1 isolates point A, allowing the potential at this point to rise to 12 v. Without the diode, point A would be clamped at I_1's threshold voltage of 8 v and voltage V_1 would never reach 12 v.

Once the circuit is in its high state, transistor voltage V_1 must drop below 4 v to pull point A below I_1's threshold and to switch V_2 back to ground. When V_1 becomes less than 4 v, the phototransistor's pull-up resistance increases and speeds up the rate of decline of V_1. Feedback resistance R_f causes V_1's switching voltage levels to be different—first 11 v, then 4v—thereby providing 7 v of hysteresis and noise immunity.

Inverter I_3 and diode D_2 buffer voltage V_2, converting it to a 5-v transistor-transistor-logic signal. If desired, the 12-v output of V_2 can be used directly as the logic input voltage.

The circuit is operating successfully in an electromechanical printer where the cable from the phototransistor to the amplifier input is a twisted pair of wires 10 feet long that run near solenoid driver cables. Moving printed matter is detected by an existing circuit without any output-signal bounce, even though the edge of the matter momentarily stops as it breaks the light beam. □

Optical detector. When object breaks LED light beam, phototransistor output voltage V_1 increases, switching on inverters I_1 and I_2. Voltage V_1 then jumps up because additional current through resistor R_f to point A decreases phototransistor pullup resistance. Voltage V_2 stays high until V_1 drops to 4 V, increasing pullup resistance and causing V_2 to return to ground. Inverter I_3 converts V_2 to TTL-compatible output.



Quasi-matched MOSFETs form filterless squaring circuit

by W.V. Subbarao
North Dakota State University, Fargo, N.D.

By compensating inexpensive dual-gate MOSFETs so that they appear matched, a squaring and frequency-doubling circuit can be made to function reliably over a broad frequency range without the aid of a filter. Conventional filterless squaring circuits require costly high-quality matched components.

Biasing MOSFETs Q_1 and Q_2 to operate in their depletion region causes MOSFET behavior to resemble that of the junction field-effect transistor. The drain current (I_D) of either Q_1 or Q_2 is given by:

$$I_D = I_{DSS}(1 - V_{GS}/V_P)^2$$

where I_{DSS} is the drain current with both gates shorted to the source terminal, V_{GS} is the voltage between shorted gates and the source terminal, and V_P is the pinchoff voltage (the V_{GS} value when $I_D = 0$).

Since Q_1 and Q_2 are not matched, they may, however have about the same V_P value (approximately -1.5 volts) but exhibit different I_{DSS} values. If Q_2's I_{DSS} current is lower than that of Q_1, say 3 milliamperes as compared to 4 mA, the control gate (G_2) of Q_2 can be driven positive, making Q_2 more conductive so that its I_{DSS} current is compensated to equal that of Q_1. In this way, Q_1 and Q_2 can be made to look matched with the same I_{DSS} and V_P values. The transfer curves show how Q_2's characteristic tracks Q_1's characteristic.

Transistor Q_3 functions as a unity-gain stage, transferring input voltage V_i to produce voltages V_1 and V_2, which are equal in magnitude to V_i but 180° out of phase with each other:

$$V_1 = -V_2 = V_i$$

Effectively, the input to the main gate (G_1) of transistor Q_1 is V_i, and the input to the main gate of transistor Q_2 is $-V_i$. Input voltage V_i can then be considered as the V_{GS} voltage for both Q_1 and Q_2.

The MOSFET transfer characteristic can now be used to solve for the drain current that flows in resistor R_D:

$$I_{D1,2} = I_{D1} + I_{D2} = 2I_{DSS} + 2I_{DSS}(V_i/V_P)^2$$

The output signal voltage contribution can be separated from the output dc offset voltage of $2R_DI_{DSS}$:

$$V_o = 2R_DI_{DSS}(V_i/V_P)^2$$

Letting $K = 2R_DI_{DSS}/V_P^2$ allows the output voltage to be written as:

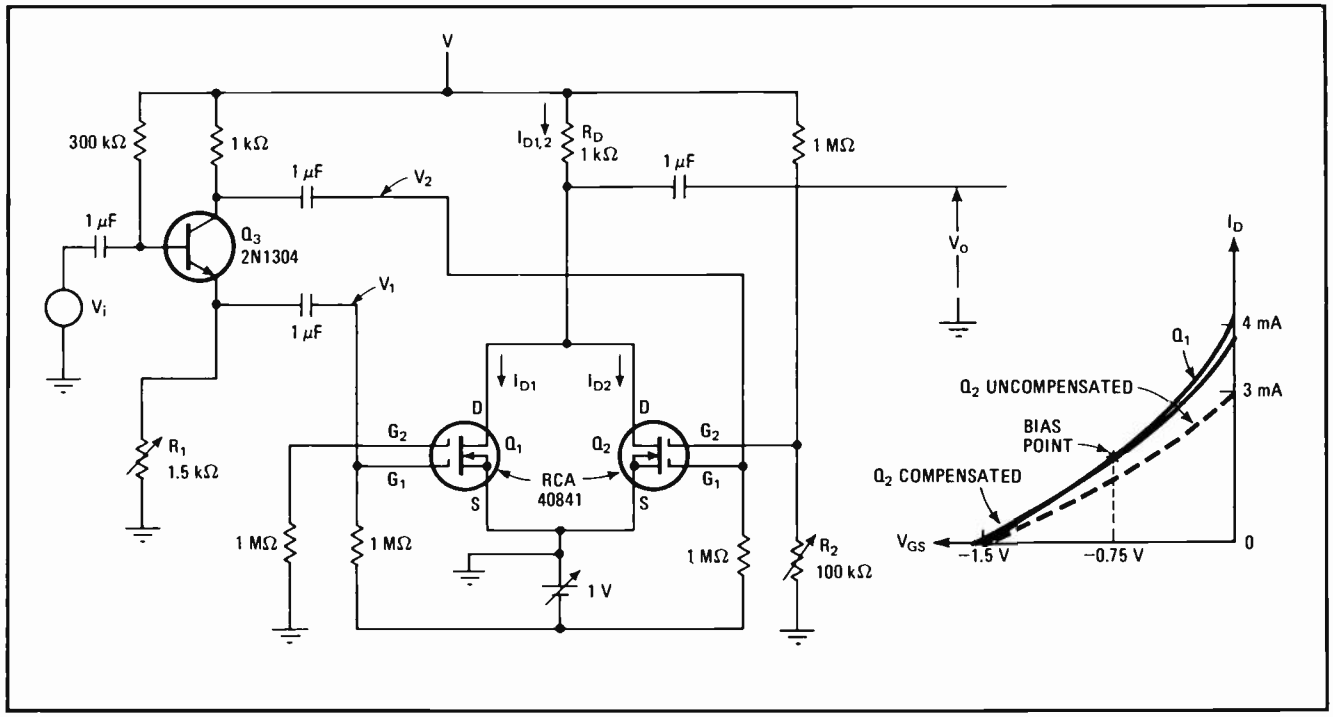
$$V_o = KV_i^2,$$

which is a squaring function.

The value of resistor R_D is held to 1 kilohm to prevent the dc offset current of $2I_{DSS}$ from saturating the MOSFETs when the circuit is operating. Also, peak output voltage swing is restricted to about 1 volt to keep from driving the MOSFETs away from their optimum midpoint bias condition.

For a sinusoidal input, V_o is also a sinusoid at double the input frequency and with a voltage gain of approximately 3.5. Resistors R_1 and R_2 are adjustable so that the Q_1-Q_2 match can be preserved for changing input signal conditions. This permits the circuit to operate from 200 hertz to 1 megahertz without any distortion. □

Compensated MOSFETs double frequency. Filterless squaring circuit works from 200 hertz to 1 megahertz. MOSFETs Q_1 and Q_2 are operated in their depletion mode, causing them to square voltages applied to their main gates (G_1). Adjusting control gate (G_2) voltage forces MOSFETs to simulate a matched pair. Unity-gain transistor Q_3 drives Q_1 and Q_2 with equal voltages of opposite polarity ($V_1 = -V_2 = V_i$).



Feedback linearizes resistance bridge

by Robert D. Guyton
Mississippi State University, State College, Miss.

With the addition of a feedback circuit, the output voltage of a standard resistance bridge can be made to vary linearly for a change in bridge resistance. The feedback circuit provides good sensitivity for a wide range of bridge resistance variations, while maintaining the full-scale linearity of the bridge output voltage to within 0.1%. Furthermore, either an ac or a dc voltage may be used to excite the bridge.

The output voltage of the standard bridge remains zero as long as its four resistance arms are equal to each other, with a resistance value of R ohms. One arm of the bridge is variable from this resistance null:

$$R_x = R + \Delta R$$

where ΔR represents the change in bridge resistance. For the standard bridge:

$$V_o' = V_1(\Delta R)/(2R+\Delta R)$$

This is not a linear relationship, since ΔR appears in the denominator. The standard bridge, therefore, is usually limited to those applications that involve only small values of ΔR.

The feedback circuit shown in the figure alters the bridge excitation voltage so that the relationship between the output voltage and ΔR becomes linear:

$$V_o = (1+2R_f/R)V(\Delta R)/2R$$

Feedback resistor R_f determines the circuit's sensitivity to the change in bridge resistance. Bridge excitation voltage can be written as:

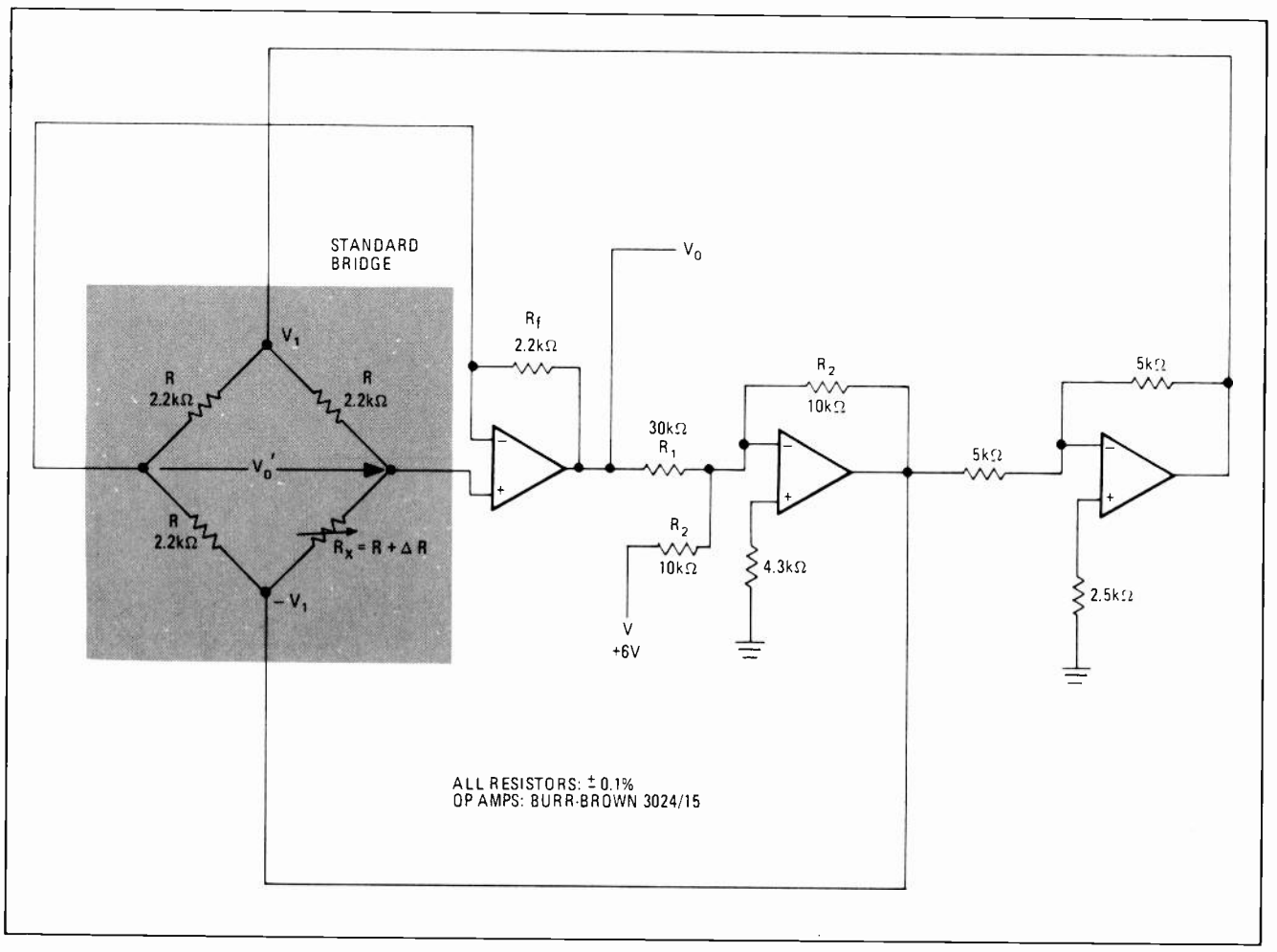
$$V_1 = V + RV_o/(R+2R_f)$$

when:

$$R_1 = R_2(R+2R_f)/R$$

Resistance R_x can vary from 0 to 2R. □

Linearized resistance bridge. Adding feedback circuit to standard resistance bridge allows output voltage V_o to be linearly related to variations in bridge resistor R_x. Changes in bridge resistance produce output voltage that is linear to within 0.1%. Circuit sensitivity is set by value of feedback resistor R_f. Amplifiers control bridge excitation voltage V_1, which can be due to either ac or dc source.



Soldering iron converts to constant-temperature probe

by Mahendra J. Shah
Univ. of Wisconsin, Space Science and Engineering Center, Madison, Wis.

Designing a circuit that has good temperature stability requires pinpointing those components that are the major drift contributors. These components can then be properly specified and compensated for temperature drift, if necessary. Unfortunately, the designer must frequently run temperature stability tests on the entire circuit because he cannot heat individual components selectively. And employing a soldering iron as a selective heat source does not produce precise temperature test results.

However, a conventional line-operated soldering iron can be easily converted into a constant-temperature probe. Since most low-power circuits operate very near ambient room temperature and most circuit components have a low thermal resistance for efficient heat transfer, the device being heated by the probe will be within a few degrees of the probe temperature. The drift contribution of the component can then be measured by noting the change in the circuit parameter of interest.

The temperature-control circuit in the diagram regulates the voltage applied to the tip of a 115-volt, 27-watt soldering iron, allowing tip temperature to be set from near room ambient to 125°C. A potentiometer permits the temperature setting to be varied continuously. The tip-temperature-sensing element is a thermistor, which is installed by drilling a small hole in the tip and then epoxy-mounting the thermistor in place.

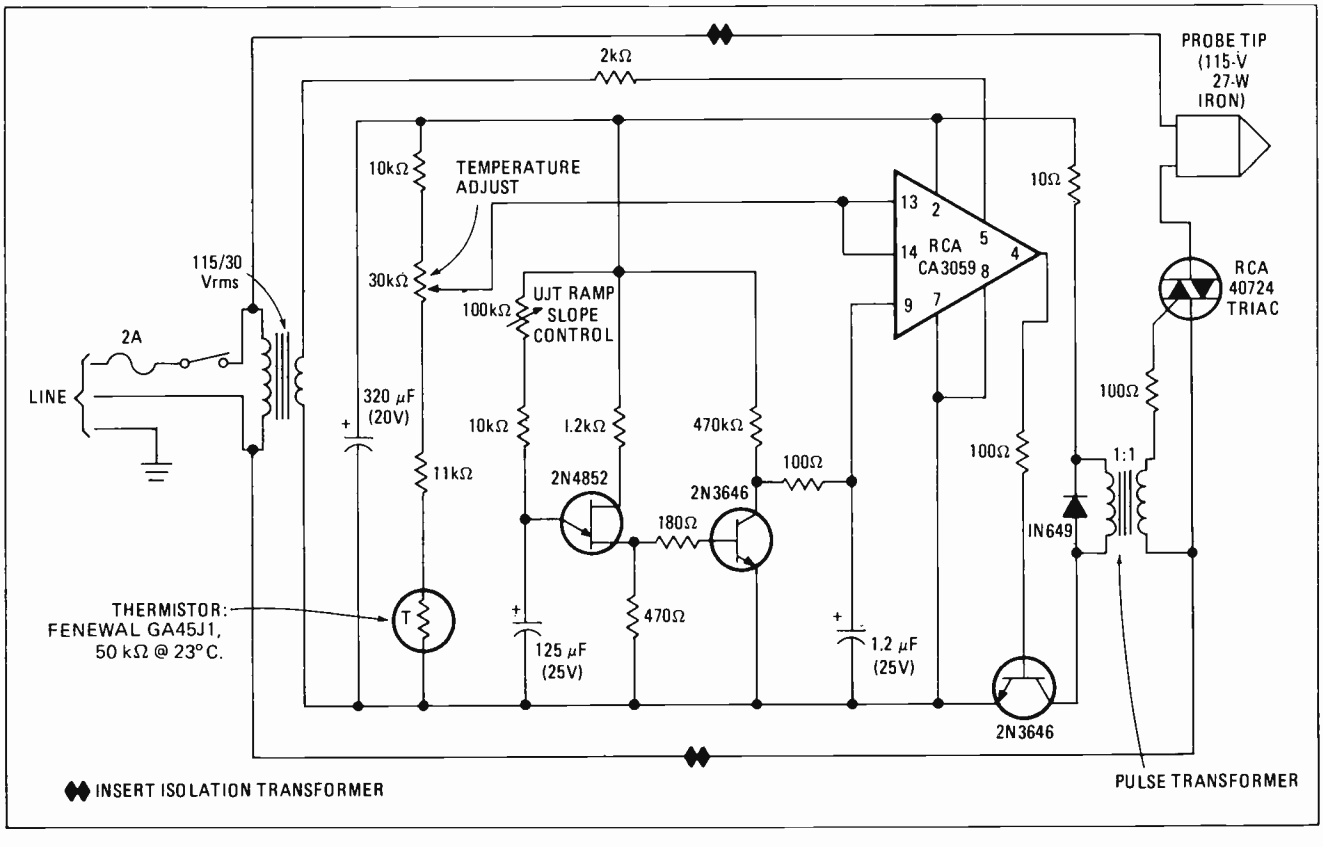
For best results, an isolation transformer should be placed between the source of line power to the tip and the triac at the output of the control circuit. The heat transfer of the probe can be improved by using silicone vacuum grease between the tip and the component under test.

Sometimes, testing component drift with a constant-temperature probe can reduce parts cost. For instance, suppose a regulated 600-v power supply that contains a high-stability zener reference costing about $24 is tested. When the temperature of the whole supply is increased by approximately 50°C, the supply output drops around 5 v.

A transistor junction is found, with the probe, to be the principal cause of the drift. Substituting a general-purpose zener selling for about $1 for the high-stability device will decrease over-all supply drift. The temperature-drift errors of the transistor junction and the low-cost zener almost cancel each other, since they have about the same magnitude but are of opposite polarity.

It is also possible to build a probe that lowers component temperature below room ambient by using a thermoelectric cooling element in a temperature-control loop. □

Pinpointing component drift. Constant-temperature probe can be built by controlling power to tip of soldering iron. Control circuit maintains tip temperature within a few degrees of desired setting, from room ambient to 125°C. Thermistor located inside probe tip acts as the temperature-sensing element. An isolation transformer (not shown) should be placed between the line input and circuit's output triac.



Exclusive-OR gate makes bidirectional one-shot

by Tim O'Toole
Tektronix Inc., Beaverton, Ore.

An exclusive-OR gate is an ideal device for building a bidirectional one-shot by running the same signal into both gate inputs, but putting a time delay on one of the inputs. The gate will then produce a pulse for every rising or falling edge of the input signal, and the width of the pulse is determined by the time delay.

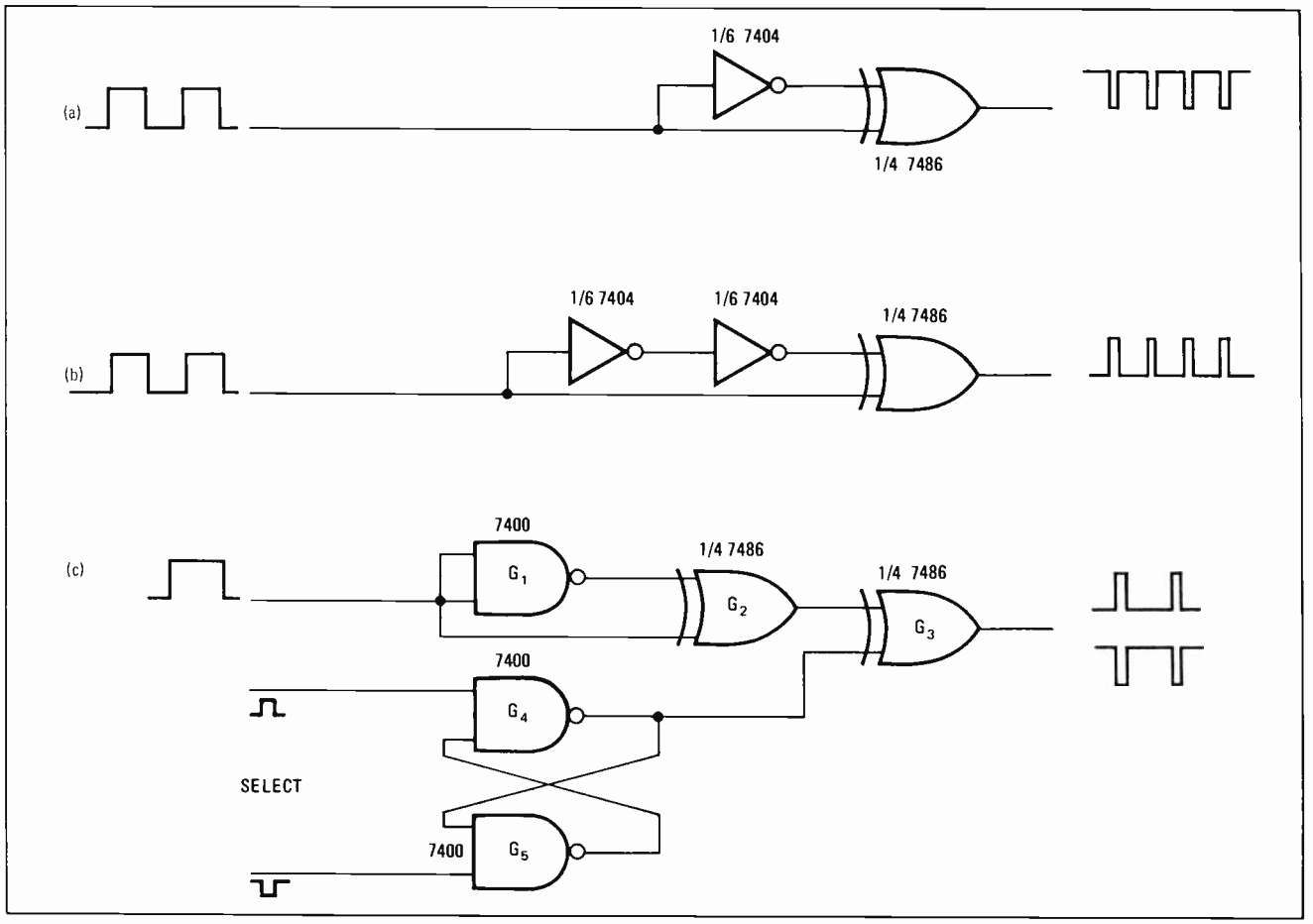
In (a), the gate inputs are inverted with respect to each other so that the gate output is in the high state for either a high or low input signal. When the input signal switches from high to low, both gate inputs are low until the inverter has a chance to change states. During this time, the gate output goes low until the inverter switches and causes the gate output to return to the high state. This process repeats when the input signal switches from low to high. Therefore, for every transition of the input signal, the gate puts out a negative-going pulse having a width equal to the delay time of the inverter.

Two inverters can also be used as the delay element, as shown in (b). Now the gate inputs have the same polarity, causing the gate output to be low for either a high or low input signal. The output will be a train of positive pulses with a width equal to a single inverter's delay time. These output pulses may be easily extended or stretched by inserting an RC timing network between the two inverters.

Applying the operating principles of circuits (a) and (b) permits the realization of a bidirectional one-shot (c) that has an addressable output pulse polarity. Gates G_1 and G_2 simply duplicate the one-shot of (a) and feed one of the inputs of the exclusive-OR output gate, G_3. A flip-flop, comprised of gates G_4 and G_5, drives G_3's other input. The polarity of the output pulses is now selectable, since the state of the flip-flop controls output pulse polarity.

If longer or more accurate output pulse widths are required, the delay element in any of the three one-shots can be changed to a delay line, such as the ones now available in 14- and 16-pin dual-in-line packages. The delay device could even be a standard off-the-shelf one-shot, for example, Texas Instruments' SN74121 or Fairchild's 9601. □

Selectable one-shot polarity. Either positive or negative output pulses can be generated by controlling high/low states of inputs to exclusive-OR gate. One-shot (a) uses time delay of single inverter to produce negative pulse train. One-shot (b) has additional inverter for positive output pulse train. Bidirectional one-shot (c) has addressable output polarity, which is determined by state of G_4-G_5 flip-flop.



Gated MOSFET acts as multiplexing switch

by Glen Coers
Texas Instruments, Dallas, Texas

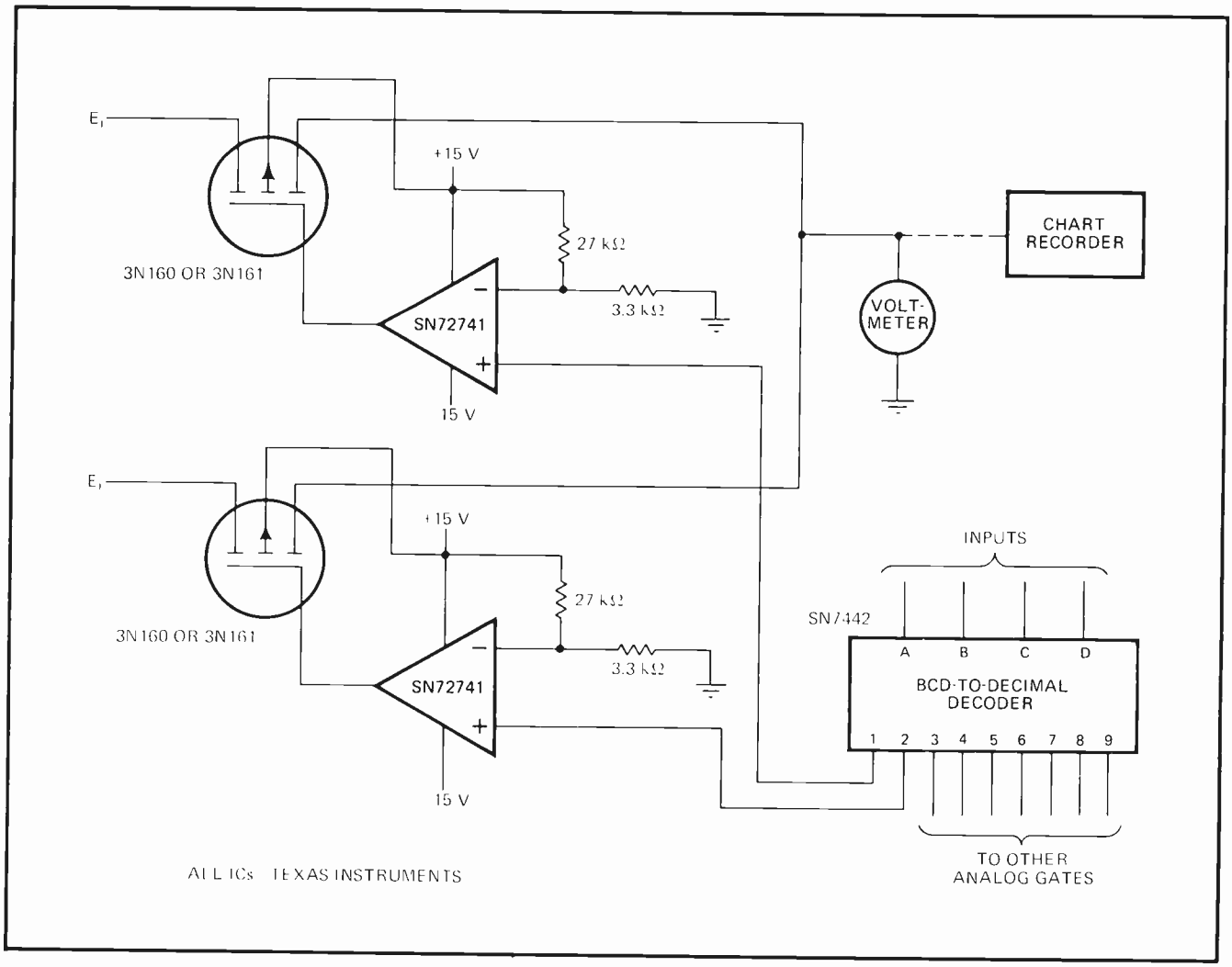
A four-terminal MOSFET makes a handy series analog gate for time-multiplexing either ac or dc signals. An array of these MOSFETs can, for instance, be used to gate a number of voltages that are being monitored periodically by a chart recorder or a voltmeter, as shown in the figure. Here, the BCD-to-decimal decoder switches one MOSFET analog gate at a time for a given interval before switching another.

The decoder outputs are high except for the output number being decoded. An operational amplifier, connected as a comparator, is used to switch each MOSFET on and off. Each comparator's inverting input is set to a dc reference voltage of approximately 1.6 volts.

When a logic 0 appears at the selected decoder output, the associated comparator's output goes to −14 V. The MOSFET that is tied to the comparator output then conducts, gating the analog input voltage to the voltmeter or chart recorder. When the decoder output returns to logic 1, the comparator output switches to 14 V, turning off the MOSFET.

Since MOSFETs are bilateral devices, they can handle both positive and negative voltages. For this circuit, the maximum input voltage swing is ±10 V, but can be extended by raising the level of the positive and negative supply voltages that bias the MOSFET's gate terminal. The multiplexer circuit has good isolation and leakage properties. □

MOSFET gate. Analog signals can be gated selectively by using a BCD-to-decimal decoder to switch array of MOSFETs. All decoder outputs are high, except for the one selected to be the output number. When selected decoder output goes low, output of associated comparator also goes low, turning on MOSFET and permitting analog input to pass to circuit's output. Both positive and negative inputs can be gated.



Stepper drive circuit boosts motor torque

by E. Wolf
Redactron Corp., Hauppauge, N.Y.

The output power of a stepping motor can be boosted when it's stepping, while the dissipated power during its dwell (holding) intervals is minimized, by effectively doubling the supply voltage of the motor-drive circuit with capacitor charge. The boosted drive circuit shown is intended for four-phase 28-volt motors.

During the dwell intervals, the drive circuit supplies the pair of motor coils that were energized during the previous clockwise step. Transistor Q_1 is on, but conducts only leakage current because transistors Q_2 and Q_3 are off. This permits capacitor C_1 to charge to the supply voltage of 24 v. (Transistors Q_1 and Q_2 form a complementary Darlington transistor pair.)

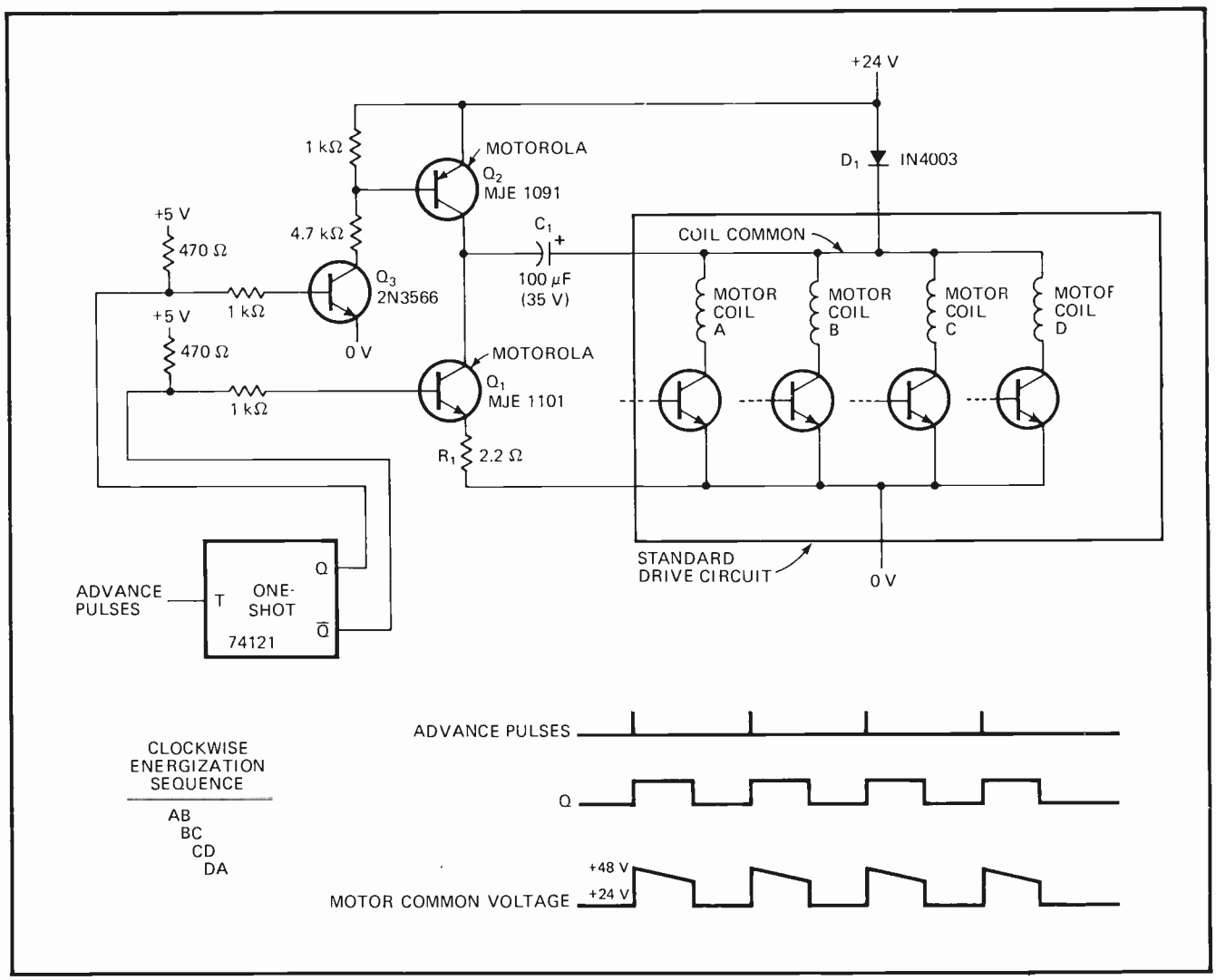
The motor's advance sequence is dictated by a pulse stream that increments the motor's winding-sequence counter and also triggers the monostable multivibrator at the input of the drive circuit. When the $\bar{Q}$ output of this one-shot goes low, its Q output goes high, turning off transistor Q_1 and turning on transistors Q_2 and Q_3.

Since diode D_1 is reverse-biased, the potential at Q_2's collector rises to about 24 v, and the capacitor is restricted to a discharge path through the motor windings. Therefore, the voltage available for the coil common lead is nearly two times the supply voltage—or approximately 48 v. With this boosted voltage, motor-winding current rises rapidly to enhance available torque.

Once the current buildup time is over, the one-shot completes its timing cycle, turning off transistors Q_2 and Q_3, while turning on transistor Q_1, which is current-limited by resistor R_1. Capacitor C_1 recharges to the supply-voltage level. This cycle repeats for every stepping pulse.

The timing of the one-shot is not critical. A reasonable timing period would be half of the shortest period between advance pulses. □

Stepping up torque. Drive circuit for stepping motor boosts available stepping power without increasing supply voltage. During motor dwell time, capacitor C_1 charges to 24-volt supply level. When advance pulse triggers one-shot, transistor Q_1 turns off while transistors Q_2 and Q_3 turn on. Coil common voltage then builds to twice the supply level because Q_2's collector voltage rises by 24 V.



Voltage-tuned filter varies center frequency linearly

by Vassilios J. Georgiou
University of Massachusetts, Amherst, Mass.

Although a voltage-tunable multiple-feedback active filter generally offers constant gain and constant bandwidth throughout its tuning range, its tuning curve for center frequency versus control voltage is usually highly nonlinear for extended frequencies. This is due to the nonlinearity of the field-effect transistor, which is used as a variable resistor, and because the center frequency varies inversely with the square root of the FET's drain-source resistance. Employing feedback, therefore, to linearize the FET's behavior is not a solution.

Instead, a modified version of the diode function generator can be used to drive the FET's gate terminal. For the voltage-tunable bandpass filter shown, center frequency remains nearly linear for changing control voltage over a center-frequency range of 4.5:1.

Resistor R_1 and supply voltage V_{GG} bias the FET at −3 volts, thereby setting the filter's first breakpoint for $V_C = 0$ at 1,460 hertz. For negative values of control voltage, only diode D_1 conducts, and the gain of the amplifier is determined by resistors R_2 and R_3.

For positive control voltages, diode D_2 conducts, and amplifier gain is about half the value it is for negative control voltages. As a result, the lower portion (right-hand side) of the filter's tuning curve tilts upward and aligns with the upper portion (left-hand side) to form a linear characteristic.

Diodes D_3 and D_4 define the second filter breakpoint—at $V_C = 2.4$ v—by further reducing amplifier gain and extending linear operation to 570 Hz. Preferably, the germanium diodes, D_1 and D_2, should be gold-doped so that they have a low forward-voltage drop. □

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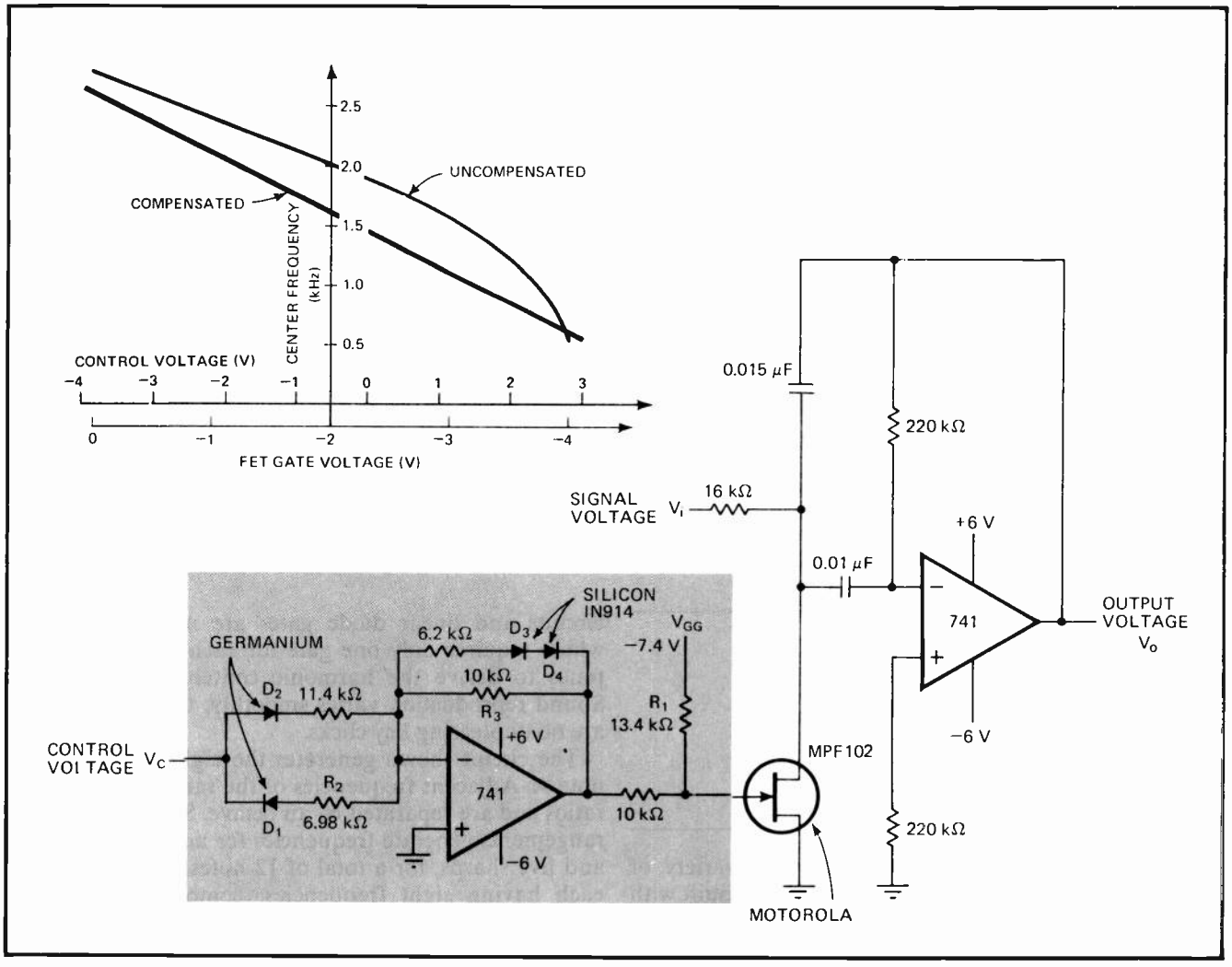
Straight-line tuning. Modified diode function generator (in color) drives FET variable resistor for voltage-tunable bandpass filter, causing center frequency to vary linearly with control voltage over 4.5:1 frequency range. Gain of function-generator amplifier is reduced for positive control voltages to raise lower section of (uncompensated) tuning curve. Compensated filter remains nearly linear.



Temperature-stable decoder for modulated pulse widths

by H.R. Beurrier
Bell Telephone Laboratories, Murray Hill, N.J.

Besides offering exceptional temperature stability, a pulse-width-modulation decoder for remote proportional radio control produces a presettable fail-safe analog output when the input control signal is interrupted. The circuit converts a time-modulated pulse input to an analog output.

Transistors Q_1 and Q_2 form a sawtooth generator with a ramp output that starts when the input control signal goes positive and that resets when the input goes negative. The control signal switches Q_2 alternately on and off.

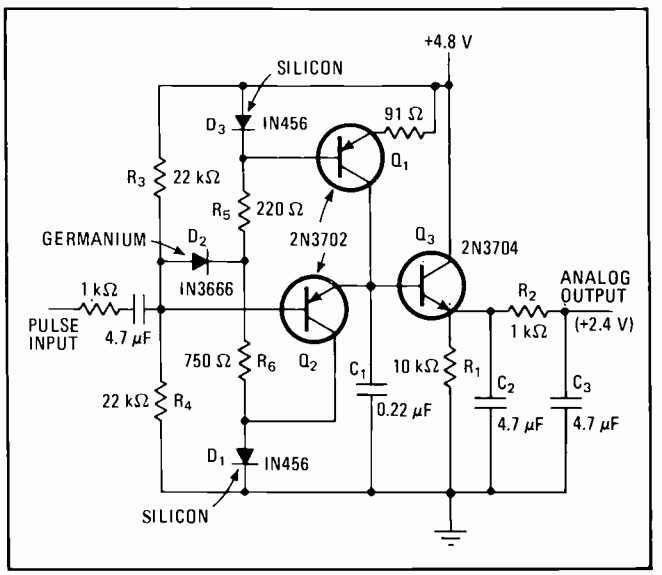
When the base of Q_2 is driven positive by the input, this transistor turns off and capacitor C_1 charges with the constant current supplied by transistor Q_1. (The longer the input pulse duration, the higher C_1's ramp voltage and the resulting output voltage.) When Q_2 is driven negative, it conducts, pulling its emitter voltage in the negative direction and partially discharging capacitor C_1.

Emitter-follower Q_3 acts as a peak-voltage detector that charges capacitor C_2 positively when its base is driven positive by the ramp voltage of capacitor C_1. If the voltage across C_1 is too negative to forward-bias the base-emitter junction of Q_3, capacitor C_2 discharges through resistor R_1. This portion of the circuit, therefore, acts as a diode peak detector with power gain. Resistor R_2 and capacitor C_3 are connected as a simple first-order output filter.

Once the input signal is terminated, the base voltage of transistor Q_2 settles to a level determined by the voltage divider of resistors R_3 and R_4. This voltage level is coupled to the output through transistors Q_2 and Q_3, which are connected as cascaded emitter-followers. The complementary arrangement of Q_2 and Q_3 causes any temperature-induced change in the base-emitter voltage of transistor Q_2 to be cancelled by an equal-in-magnitude, but opposite-in-polarity, change in the base-emitter voltage of transistor Q_3.

The circuit's output voltage is referenced to the lower point of capacitor C_1's charge/discharge cycle. When the input is negative, diode D_1 reverse-biases transistor Q_2's collector so that capacitor C_1 always discharges to the same level. Diode D_2 and resistors R_5 and R_6 clamp the capacitively coupled input control signal so that transistor Q_2's base is driven slightly negative. Diode D_3 simply fixes the base voltage of transistor Q_1.

With the component values shown, the circuit will convert a pulse width of 1.25 ±0.63 milliseconds to an analog output of 2.4 ±0.6 volts dc. The 1-kilohm input resistor simply reduces the loading on the driving source. □



PWM decoder. Circuit detects pulse-width-modulated signals, supplying dc analog output over wide operating temperature range. If input control signal is interrupted, decoder output goes to preset fail-safe level. Transistors Q_1 and Q_2 and capacitor C_1 make up sawtooth generator that drives transistor Q_3, which acts as peak-voltage detector. Q_2 and Q_3 are cascaded complementary emitter-followers.

C-MOS sums up tones for electronic organ

by Robert Woody
Hercules Inc., Radford, Va.

An electronic organ that produces a wide variety of voices, either singly or in combination, can be built with relatively simple circuitry if complementary-MOS logic circuits and linear diode gates are used. The organ, which requires only one gate for each frequency, adds tones to derive the harmonic content of each voice. Sound reproduction varies smoothly, too, so that there are no unpleasing key clicks.

The circuit shown generates the eight frequencies of note A. Adjacent frequencies of the same note have 2:1 ratios and are separated by an octave. Similar circuit arrangements generate frequencies for notes B through G and five sharps, for a total of 12 notes. These 12 notes, each having eight frequencies, comprise the 96 frequencies in the organ. Individual frequencies are spaced

at 6% intervals, from 32.7 to 7,902 hertz.

The eight square-wave outputs of the Hartley oscillator and the binary divider have precise frequencies, but are not musical because square waves contain only the fundamental frequency and odd (not even) harmonics. Furthermore, if these square-wave frequencies are turned on and off directly by key switches, the sounds begin and end too abruptly to be musically pleasing, and key clicks will be heard.

A diode gating circuit, like the one consisting of diode D_1, resistor R_1, and capacitor C_1, is used to convert each square wave to a sawtooth. This supplies the even harmonics and helps to turn the tones on and off gradually without clicks.

The square wave alternates between the supply voltage and ground. While the square wave is at ground, D_1 is forward-biased by current flowing through R_1, and the gate output is also at ground. When the square wave goes to the supply voltage level, D_1 is back-biased so that current through R_1 charges C_1, causing the gate output to have a rising slope. The capacitor discharges quickly through the diode when the square wave returns to ground, and the cycle repeats.

Resistor R_2 and capacitor C_2 slow the application of current to resistor R_1, permitting the gate to turn on and off gradually without clicks. Since C_1 charges for half the cycle of square-wave frequency f, time constant R_1C_1 is half the period of f, or:

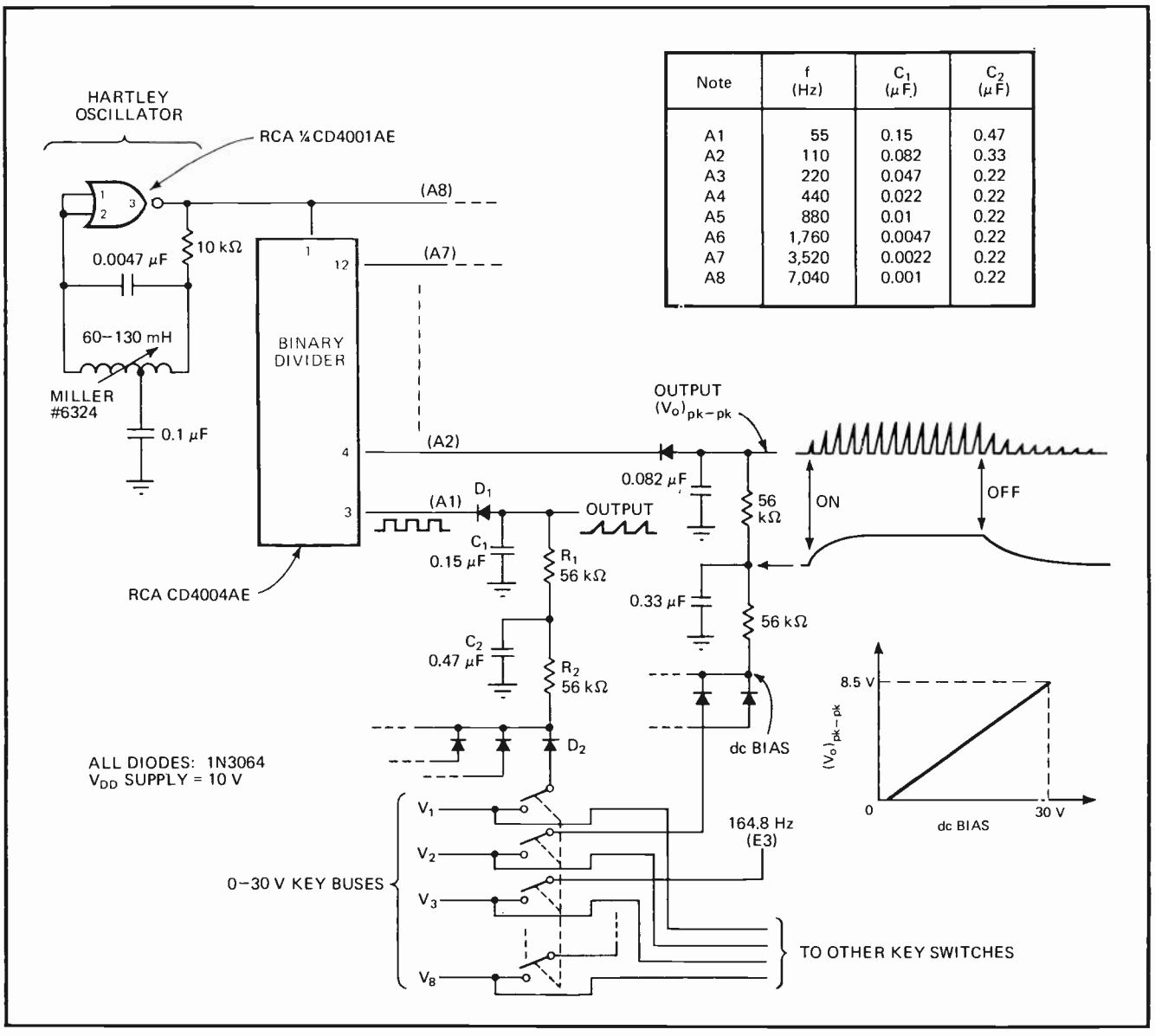
$C_1 = \frac{1}{2}fR_1$

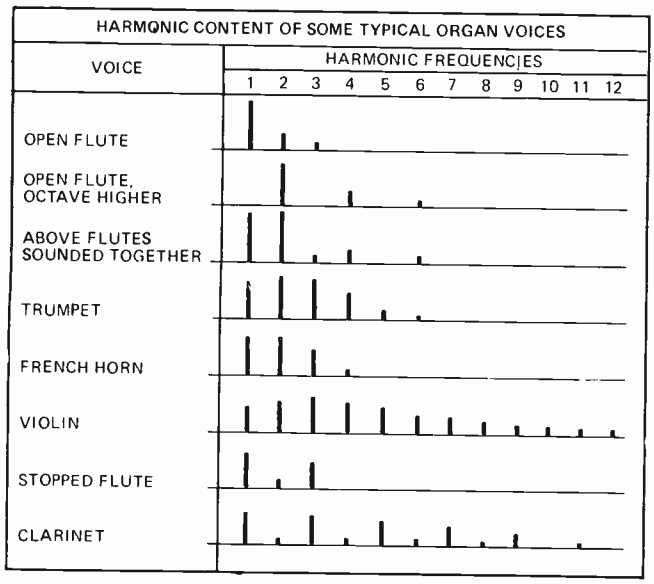
Values for capacitor C_2 are selected to approximate the switching times of organ pipes. Since the output of each gate is linearly proportional to its dc biasing voltage, the tone amplitude needed can be metered out precisely.

To sum tones to create the desired organ voices, which comprise several harmonically related tones, each gate output must be filtered to reduce its harmonics

C-MOS makes organ music. Complementary-MOS ICs add tones to produce eight frequencies that make up note A. Each of the remaining six notes, B through G, plus five sharps, requires its own Hartley oscillator and binary divider network to generate all 96 organ frequencies. Diode gate at each divider output converts that square wave to a sawtooth to get the necessary even harmonics.

Note	f (Hz)	C_1 (μF)	C_2 (μF)
A1	55	0.15	0.47
A2	110	0.082	0.33
A3	220	0.047	0.22
A4	440	0.022	0.22
A5	880	0.01	0.22
A6	1,760	0.0047	0.22
A7	3,520	0.0022	0.22
A8	7,040	0.001	0.22





down to the simplest voice produced in the organ, namely the flute. Since the eight frequencies of a note are multiples or submultiples of each other, they can be handled by one low-pass filter. This means that only 12 low-pass filters are needed for all 96 frequencies.

The diodes between the gates and the key switches—diode D_2, for instance—allow a given tone to be sounded by a number of different key switches. All of the key switches indicated are operated by the key for note A1. The voltages (V_1, V_2, V_3, . . .) on the key buses determine the amplitude at which the tones are sounded (V_1 controls the fundamental frequency tone, V_2 the second harmonic, V_3 the third, . . .). The key bus voltages set the harmonic content and, therefore, the voice of all the keys on the keyboard.

To conserve circuitry, the third harmonic, note A3, borrows a tone from the gate (not shown) used for note E3. The resulting 0.2-Hz frequency error cannot be heard. □

Transistor gating circuit cuts signal delay to 100 ps

by Arthur J. Metz
Tektronix Inc., Beaverton, Ore.

Frequently in emitter-coupled-logic design, a high-speed data signal must be gated by a dc control signal that is generated by a contact closure or a transistor-transistor-logic gate. When the propagation delay in the high-speed signal path must be held to a minimum, a simple transistor circuit can probably provide the fastest way to perform the gating function.

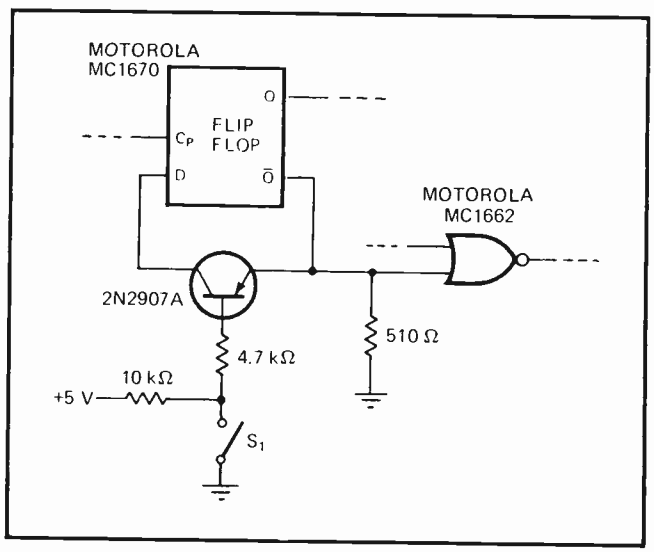
Propagation delay for the transistor gate is as low as 100 picoseconds, compared to the 1-nanosecond delays of the fastest integrated-circuit gates presently available. Moreover, the transistor gate consumes less power and costs less than the IC gate, especially if an additional IC gate package is needed to perform the gating function.

A typical application for the transistor gate is shown in the figure. Here, signal delay between the flip-flop's $\overline{Q}$ output and its D input must be minimized to realize the fastest possible toggle rate.

With switch S_1 open, the transistor's base-emitter junction is reverse-biased. An internal pull-down resistor of about 50 kilohms at the flip-flop's D input holds all data inputs near ground potential, reverse-biasing the flip-flop's input stage (by more than 3 volts) and assuring the rejection of any signal that passes through the internal capacitance of the transistor. When the switch is closed, the transistor saturates and provides a low-impedance signal path. For TTL applications, the function of switch S_1 is implemented by the appropriate TTL device.

The noise immunity of the gating circuit is maintained by keeping the transistor's collector-emitter voltage drop low. (With the type 2N2907A transistor, which has excellent saturation characteristics, the V_{CE} drop can be held to approximately 10 millivolts by using a forced beta of 0.1.) Driving several high-impedance inputs or perhaps one low-impedance input will cause some loss of noise immunity. Although driving a terminated line is not recommended, the gate may be driven from a terminated line.

As with any ECL design, care must be taken in laying out the circuit to realize maximum performance. Since the full logic-voltage swing appears at the transistor's base terminal, the base biasing resistor should be located close to that terminal to eliminate the transmission line effects of an interconnecting lead. □



Gating ECL signals. Bipolar transistor gate can transfer logic signals with propagation delay of as little as 100 picoseconds. With switch closed, transistor saturates and gates signals from flip-flop's $\overline{Q}$ output to its D input. When switch is open, transistor is cut off, and strong reverse bias at D input rejects all unwanted stray signals. The switch can be a pair of contacts or a TTL device.

Staircase generator resists output drift

by Maxwell Strange
NASA, Goddard Space Flight Center, Greenbelt, Md.

Tracking capacitors that mutually cancel temperature drift make a simple analog staircase generator, which is as accurate and stable as expensive circuits that employ precision digital-to-analog converters. Additionally, the strictly analog circuit is easier to adjust for any number of steps and to any step amplitude.

The generator essentially consists of two sections, a one-shot and an integrate-and-hold circuit. The one-shot, which drives the integrate-and-hold circuit, is triggered by an oscillator or system clock that determines the generator's stepping rate. During the high period (T) of the one-shot's output pulse, integrating capacitor C_1 is charged to produce an output voltage step:

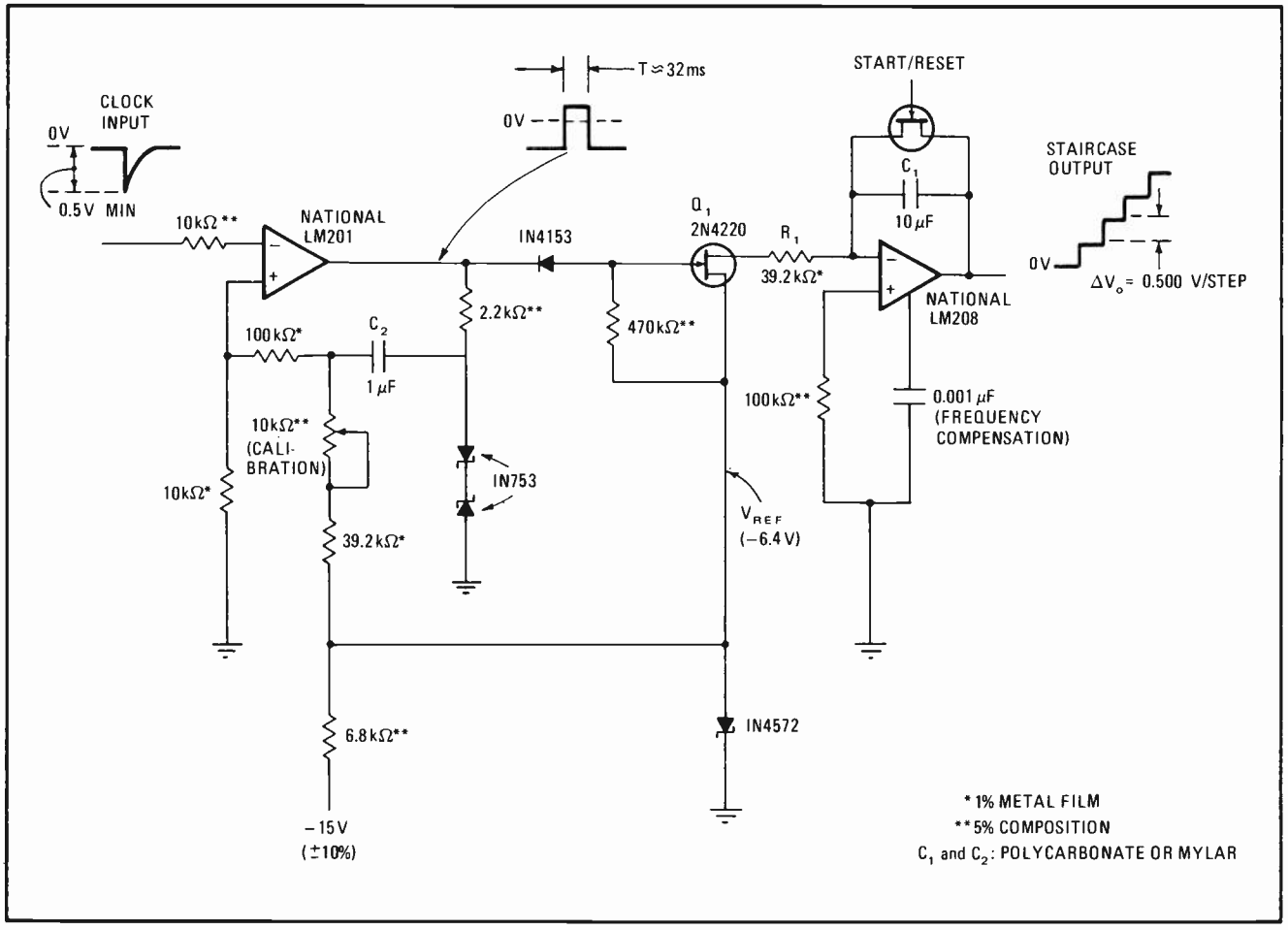
$$\Delta V_o = V_{REF}T/R_1C_1$$

Between one-shot output pulses, transistor Q_1 is off, and the integrator becomes a hold circuit and maintains the output constant.

Capacitors C_1 and C_2 are the two components with the greatest effect on step height stability. If the same type of capacitor is used in both the one-shot and the integrator sections of the circuit, the temperature coefficients of C_1 and C_2 will cancel. Staircase risetime is proportional to capacitor C_2, while integrator slope is proportional to capacitor C_1, so that step height is unaffected by a similar percentage change in both capacitors. The period of the one-shot's output pulse is directly proportional to the ratio of C_2/C_1.

As for the output voltage droop that occurs during the integrator's hold mode, the value of C_1 must be large enough to keep it negligible over the staircase cycle. For the components shown, output droop is only about 1 millivolt in 10 seconds, and step amplitude is stable within ±0.2% from 0°C to 50°C. □

Stepping up. Staircase generator employs one-shot to drive integrate-and-hold circuit. During one-shot period, capacitor C_1 charges and steps up output voltage. When one-shot is off, integrator section holds step height constant. Output voltage droop is kept to 1 millivolt in 10 seconds. Step amplitude drift is held to ±0.2% because temperature coefficients of same-type capacitors C_1 and C_2 cancel.



Four-ampere power supply costs just $13 to build

by Joseph Ennis
Automation Industries, Inc., Vitro Laboratories Division, Silver Spring, Md.

The cost of building a regulated power supply can be lowered to around $13 if a large capacitor is used to store energy at a higher voltage than is necessary. Under normal operating conditions, the supply, which is primarily intended for powering a stereo amplifier, can deliver an output of 4 amperes at 20 volts with load fluctuations down to 18 hertz and with regulation to better than 5%.

A high-value capacitor, one measuring tens of thousands of microfarads, stores charge so that only a small amount of transformer iron is needed to produce the 4-A operating current. The resulting higher-than-required capacitor voltage is then dropped to the desired 20-V level with a transistorized series regulator. Moreover, two inexpensive incandescent lamp bulbs are used for short-circuit protection, rather than a more costly current foldback technique.

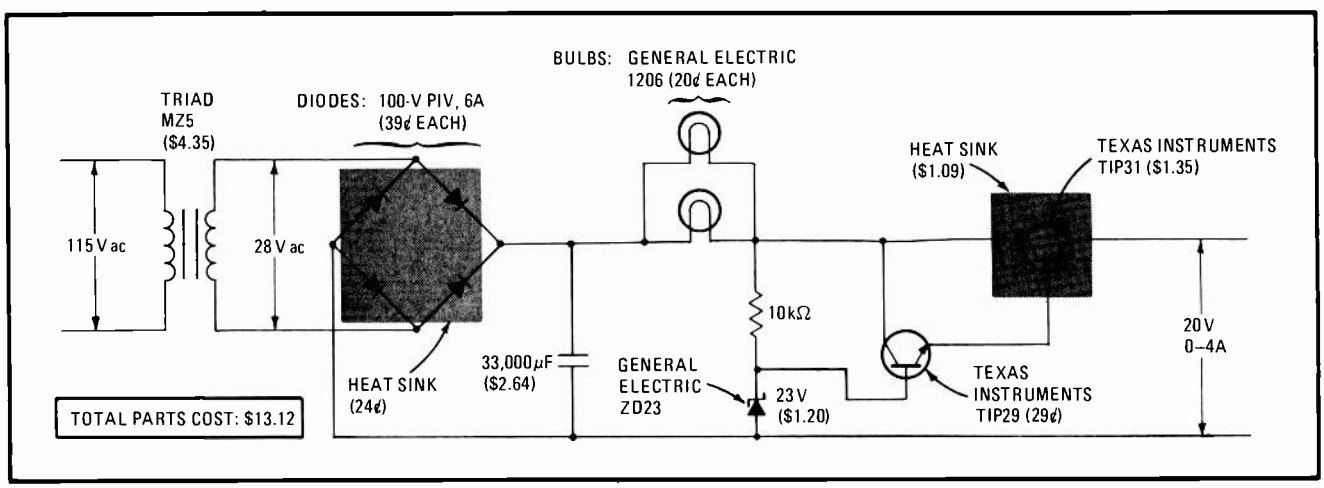
With no load at the output, the transformer charges the capacitor to about 39 V through the diode bridge. The transformer, which has a no-load secondary voltage rating of 28 V ac, can deliver the 4-A operating current but will not deliver this voltage under loading because of its core and copper losses. Although capacitor voltage may drop to around 24 V during peak loading, the series regulator will continue to provide a smooth 20-V output.

A current of more than 4 A could be controlled by the regulator transistor with the appropriate heat sinking, but the heat sink would cost more than the transistor. The heat-sink area is designed to handle only normal worst-case operating conditions and does not allow for any current foldback dissipation.

Instead, this dissipation is provided by two replacement-type automobile lamp bulbs. Besides acting as fuses when there is a short circuit at the output, they reduce the voltage drop across the regulator transistor, thereby decreasing the power it has to dissipate during normal supply operation.

To change the supply's output voltage to 15 V, the 23-V zener is replaced by a 17-V one. If a 5-V supply is needed, a transformer with a secondary voltage lower than 28 V should be selected to reduce the voltage drop that the regulator must handle. A negative-voltage supply can be constructed by substituting complementary transistor types TIP30 and TIP32 for the type TIP29 and TIP31 transistors. □

Economical regulated supply. Parts cost for power supply is pared to absolute minimum by storing energy in 33,000-microfarad capacitor at higher-than-required voltage level. This allows a fairly lossy, and therefore inexpensive, transformer to be used. Incandescent lamp bulbs serve as fuses in case of a short circuit and reduce voltage seen by series-regulator transistor. Output is 20 volts at 4 amperes.



Binary division produces harmonic frequencies

by Donald DeKold
Santa Fe Junior College, Gainesville, Fla.

Harmonically related frequencies—more specifically, a fundamental frequency and its first nine overtones—can be generated with binary division of a blanked pulse train. The harmonic frequency generator, which consists of a clock pulse generator, a decade counter, and a few NOR gates and flip-flops, produces square-wave outputs at frequencies f_o through $10f_o$.

The clock frequency must be 2^n times faster than the frequency of the highest harmonic of interest (n is the number of flip-flops used for the binary division). Therefore, to produce the highest harmonic, $10f_o$ in this case, the clock output is simply divided down by 2^n. For all harmonics but the fifth, however, the clock signal must be properly gated before it can be divided.

To understand why this is so, consider what happens

with the ninth harmonic. The uppermost NOR gate passes and inverts the first nine clock pulses to reach it. But the arrival of the tenth pulse coincides with the arrival of a high from the decade counter. Since the counter's output stays high for the full duration of the tenth clock pulse, the gate's output remains low, preventing the tenth pulse from propagating. This tenth-pulse rejection occurs every $2^n f_o$ times per second.

Clearly, the gate's output pulse frequency is nine-tenths that of the clock frequency, because one pulse is blanked for every ten delivered. The gate's output waveform may be regarded as the 2^nth overtone of $9f_o$, but one that is badly distorted with respect to phase. The nine pulses making up a full period of this waveform are cumulatively advanced in time from their proper locations as they progress through one complete period of the binaryfflovertone of thefffundamental.

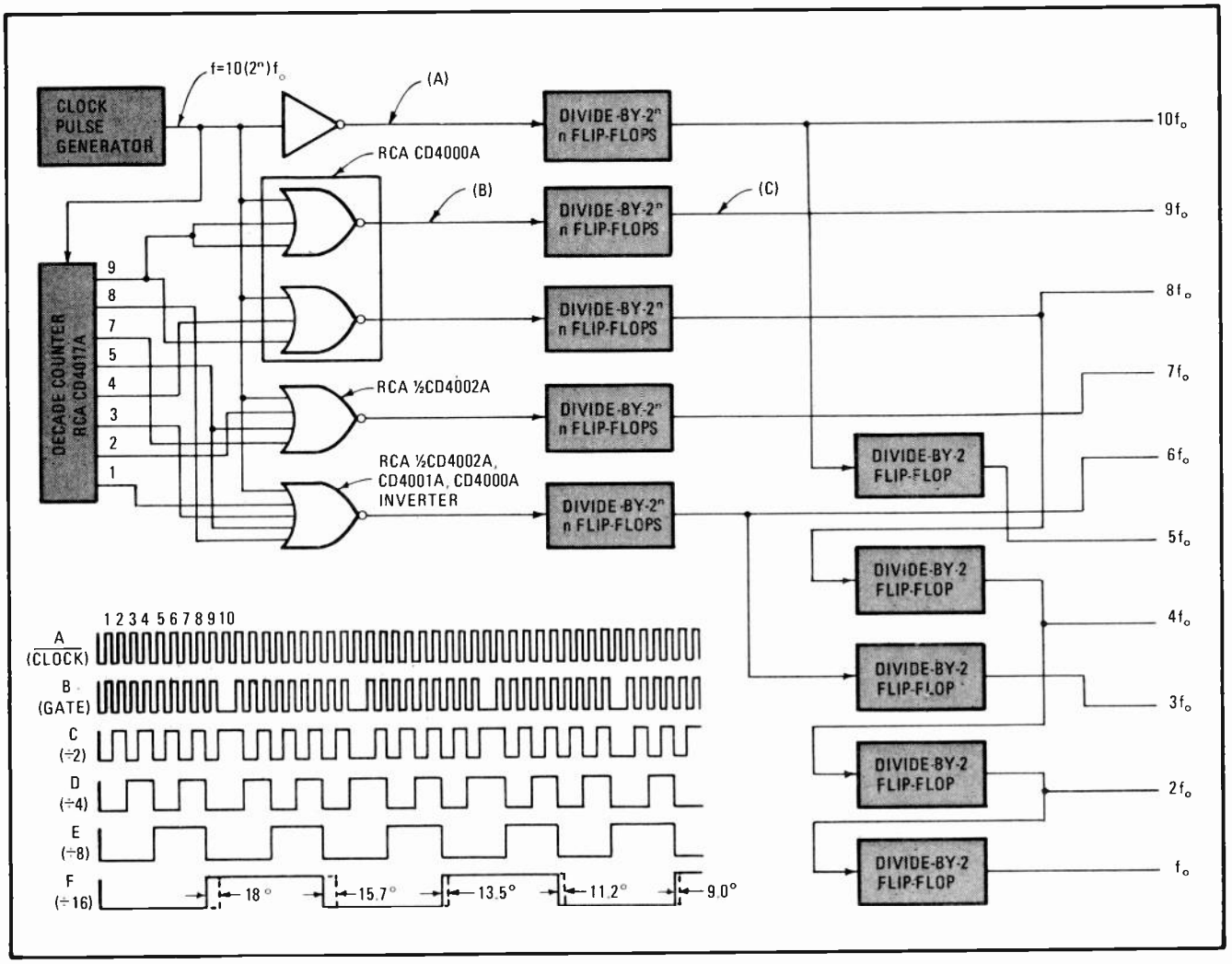
This phase distortion can be almost eliminated by successively dividing the gate output by two with flip-flops, as shown in the timing diagram. Waveforms A through F illustrate how the blanked space can be made smaller by flip-flop divisions of 2, 4, 8, and 16. Although only 2½ cycles of divided-by-16 waveform F are shown, the reduction of phase distortion is still evident.

The proper locations of this waveform's transitions—those that a true square wave of frequency $9(2^{n-4})f_o$ would produce if divided in the same way—are denoted by the colored dashed lines. The leftmost switching edge, which exhibits the largest error, is advanced by 18° from the true edge. At any stage of division, the maximum uncertainty in a transition will always be less than the period of the clock frequency.

Harmonic frequencies $6f_o$, $7f_o$, and $8f_o$ are developed in much the same way as $9f_o$. Two clock pulses must be blanked for $8f_o$, three for $7f_o$, and four for $6f_o$. To generate harmonics $5f_o$, $4f_o$, $3f_o$, $2f_o$, and f_o, binary divisions of harmonics $10f_o$, $8f_o$, and $6f_o$ are performed as indicated.

Complementary-MOS integrated circuits can be used to build this harmonic generator. If RCA's type CD4017A decade counter is chosen, the maximum clock frequency is limited to 5 megahertz. (An unused dual-input NOR gate in RCA's type CD4001A package can be employed as the clock inverter.) □

Harmonic generator. Single clock signal can be used to create fundamental frequency f_o and its first nine harmonics. Clock frequency can be divided directly for tenth and fifth harmonics, but other harmonics must be gated to produce appropriately blanked pulse train. (For instance, one clock pulse out of ten is blanked by top NOR gate for harmonic $9f_o$.) Flip-flops then divide gated outputs.



Precision auto tachometer squelches point bounce

by James B. Young
Canadian General Electric Ltd., Peterborough, Ont., Canada

A tachometer circuit for automobiles with capacitive-discharge ignition systems suppresses point bounce while measuring motor rpm accurately to within 1%. The circuit, which has an operating temperature range of -20°F to 150°F, can also be used as a temperature-compensated ratemeter or to eliminate relay-contact bounce.

Many automobile tachometers do not work properly with a capacitive-discharge ignition because this type of system employs the breaker points only for triggering an SCR. The voltage waveform across the breaker points, therefore, consists of a series of 14-volt pulses, rather than the 200-v spikes that exist in the usual kettering ignition system.

The tachometer circuit shown is composed of three sections: a relaxation oscillator at the input for point bounce suppression, a monostable multivibrator for pulse generation, and a buffer for driving a meter.

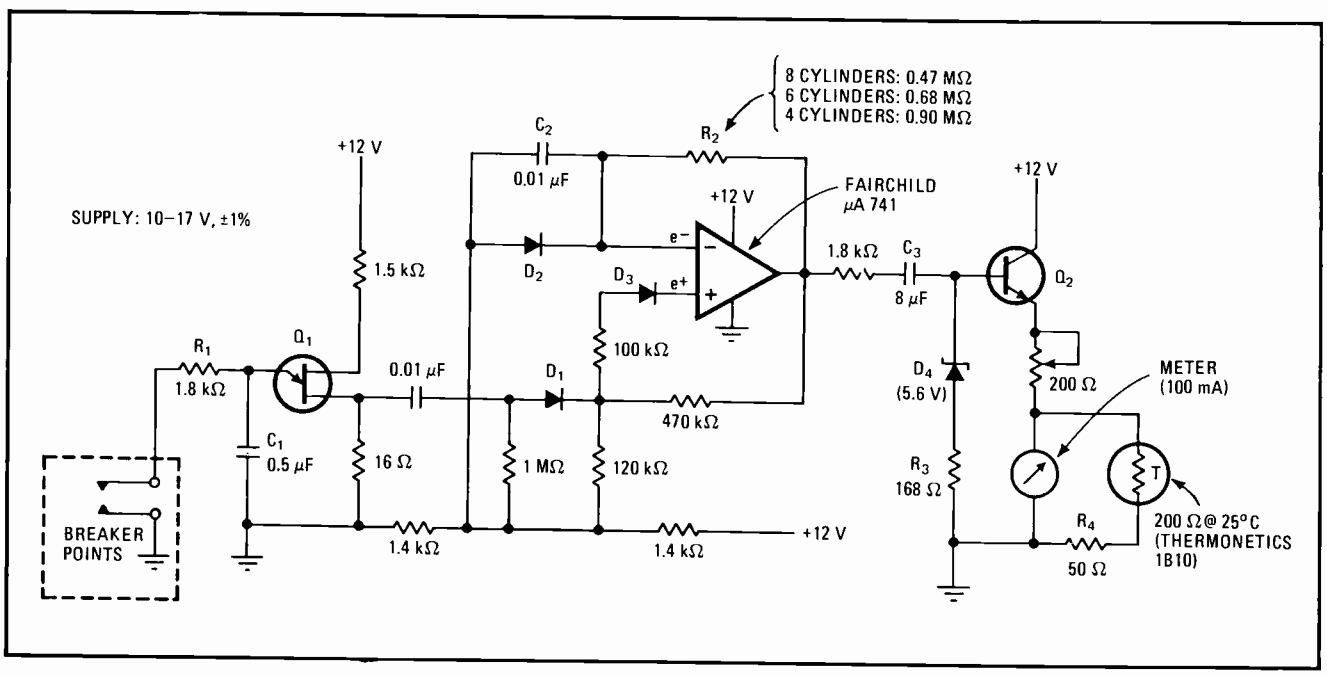
Unijunction transistor Q_1 is operated with an emitter current that is larger than its valley current so that it will not turn off after triggering. When the points open, capacitor C_1 charges through resistor R_1 until Q_1 fires (in 0.5 to 0.7 millisecond) and triggers the monostable. The current through R_1 keeps Q_1 on and prevents C_1 from charging until the points close. If the points bounce upon closure, they will not be open long enough to allow C_1 to charge and fire Q_1 again.

For every point opening, the monostable produces a pulse having a fixed width and amplitude. Normally, the output stage of the operational amplifier produces a negative saturation voltage. But when a positive trigger from the relaxation oscillator is applied through diode D_1, the op-amp's output switches to a positive saturation voltage, causing capacitor C_2 to charge positively through resistor R_2. Capacitor C_2 stores the charge until e^- is greater than e^+, and the op amp switches back to its stable state.

Diode D_2 clamps the voltage across C_2 to about -0.6 v, while diode D_3 provides temperature compensation for changes in D_2's junction-voltage drop. Both of these diodes should be kept in thermal contact with each other. Since the op amp is left floating so that it can be operated from a car's single supply voltage, it has a small positive output voltage when in its untriggered state, making capacitor C_3 necessary to decouple the meter.

Zener diode D_4 and resistor R_3 regulate the output against supply voltage variations, and the thermistor compensates for temperature variations in the base-emitter voltage of transitor Q_2. If a meter with a full-scale current rating of less than 5 milliamperes is used, the thermistor, as well as transistor Q_2 and resistor R_4, can be omitted. □

Measuring rpm. Intended primarily for automobiles with capacitive-discharge ignitions, tachometer circuit accurate within 1% is immune to breaker-point contact bounce. When points open, capacitor C_1 charges until unijunction transistor Q_1 fires and triggers one-shot formed by op amp. Point bounce is suppressed because C_1 takes 0.7 millisecond to charge before Q_1 can fire. Circuit can operate from -20°F to 150°F.



Agc rf threshold detector provides fast slewing

by Roland J. Turner
American Electronics Communications Corp., Lansdale, Pa.

In both radar and communication systems, an automatic-gain-control loop is commonly employed to keep signal level constant for enhanced signal detection. As systems become more adaptive, the agc loop must be more sophisticated, frequently forcing simple circuits to perform multiple functions.

Meeting this demand is an rf threshold detector for the agc loop in an rf receiver. The detector can process signals of 1 megahertz to 1 gigahertz with a slew rate of several volts a microsecond. It also permits delayed agc operation and can perform over a wide range of temperature and supply-voltage variations.

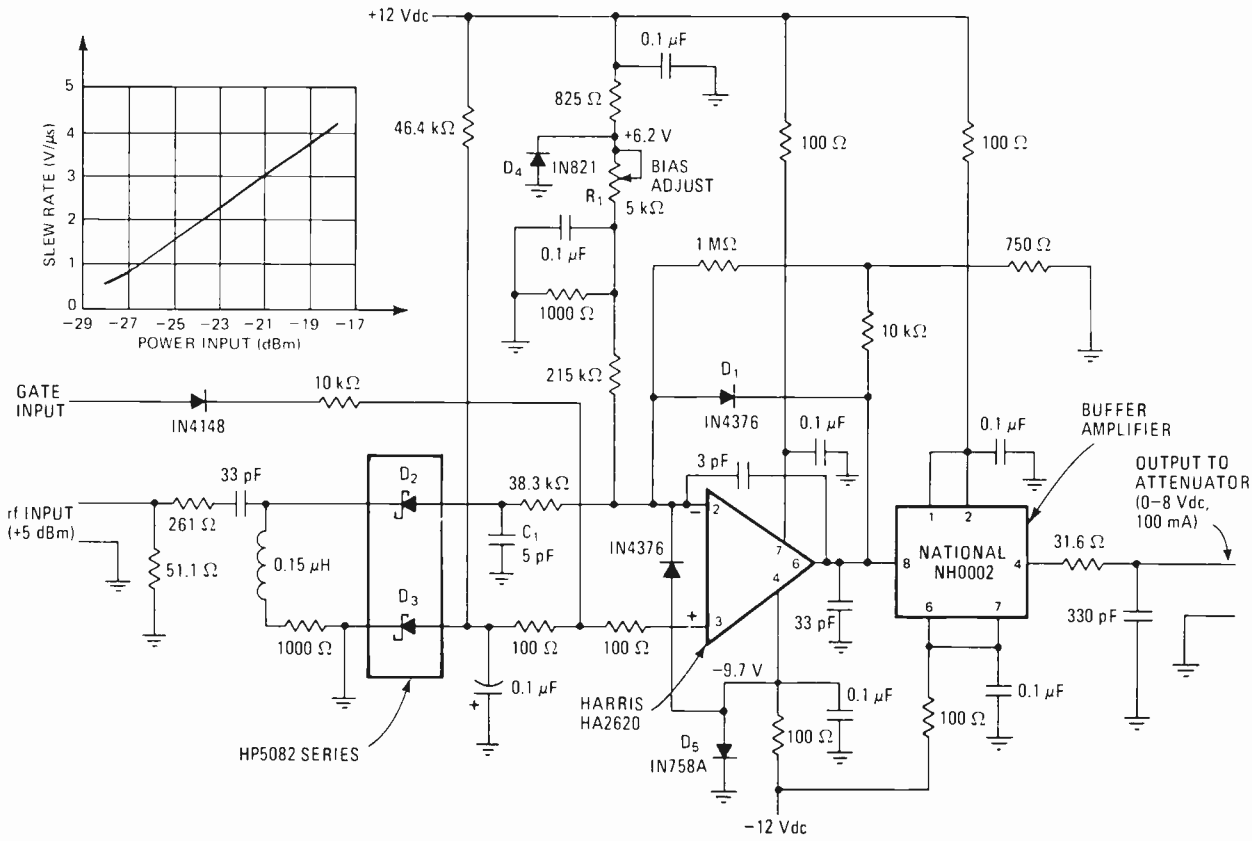
Furthermore, below the detection threshold, the signal can be processed linearly in the rf section of the receiver. Above the detection threshold, the output of the rf section is rapidly leveled so that such detrimental effects as limiting and hangup cannot occur in subsequent i-f stages. This fast action prevents the receiver from being desensitized at high signal levels and permits low-level targets to be detected even in the proximity of heavy clutter.

With the threshold power level (typically 0 to 5 dBm) applied at the detector's rf input, the input voltages of the operational amplifier are equalized so that there is no output voltage. For signal levels below the threshold, the op amp's inverting input swings positive, relative to the noninverting input, and the op-amp output is clamped by diode D_1 near the quiescent bias voltage set by potentiometer R_1. This clamp prevents the output of the op amp from swinging to the negative supply voltage and enhances the recovery time of the detector at its threshold level.

As soon as the rf input develops 3 millivolts of rectified bias voltage across capacitor C_1, the detector's output goes positive to 1 V, thereby activating the agc loop in which it is installed. Only the differential offset voltage between the dual Schottky diodes, D_2 and D_3, is impressed across the op amp's differential input. The op amp provides 50 decibels of gain, while Schottky diode D_3 provides automatic temperature stabilization for the detector. Diodes D_4 and D_5 are temperature-stabilized reference diodes that desensitize the detector to power supply variations.

The rf section of the receiver is gated by switching the voltage at the detector's gate input from its normal

Closing the loop. Threshold detector for agc loop in rf receiver can handle broadband signals with frequencies of 1 megahertz to 1 gigahertz at slew rates as fast as 1 volt/microsecond. Dual Schottky diodes and high-slew-rate op amp account for circuit's speed. Temperature compensation, from 0°C to 60°C, is provided by diodes D_2 and D_3, while diodes D_4 and D_5 compensate for supply variations of ±6%.



-10-v bias level to 10 v. This overrides any signal condition, forcing the detector's output to go to 8 vdc and forcing the associated attenuator in the agc loop to its maximum attentuation state.

For power levels above the detection threshold, the detector produces 4.2 v at its output per decibel of input power over the operating temperature range of 0°C to 60°C. Less than 0.5 dB of loop dynamic range is consumed by the static offset voltage of the transfer function over the same temperature range.

Moreover, the transfer function remains constant and unaffected by ±6% variations in the supply voltages. Less than 0.3 dB of loop dynamic range is consumed by static offsets in the transfer function for the same supply variations. For signals greater than 2 dB above threshold, the detector slew rate exceeds 1 v/μs. □

Phase comparator for servo loops

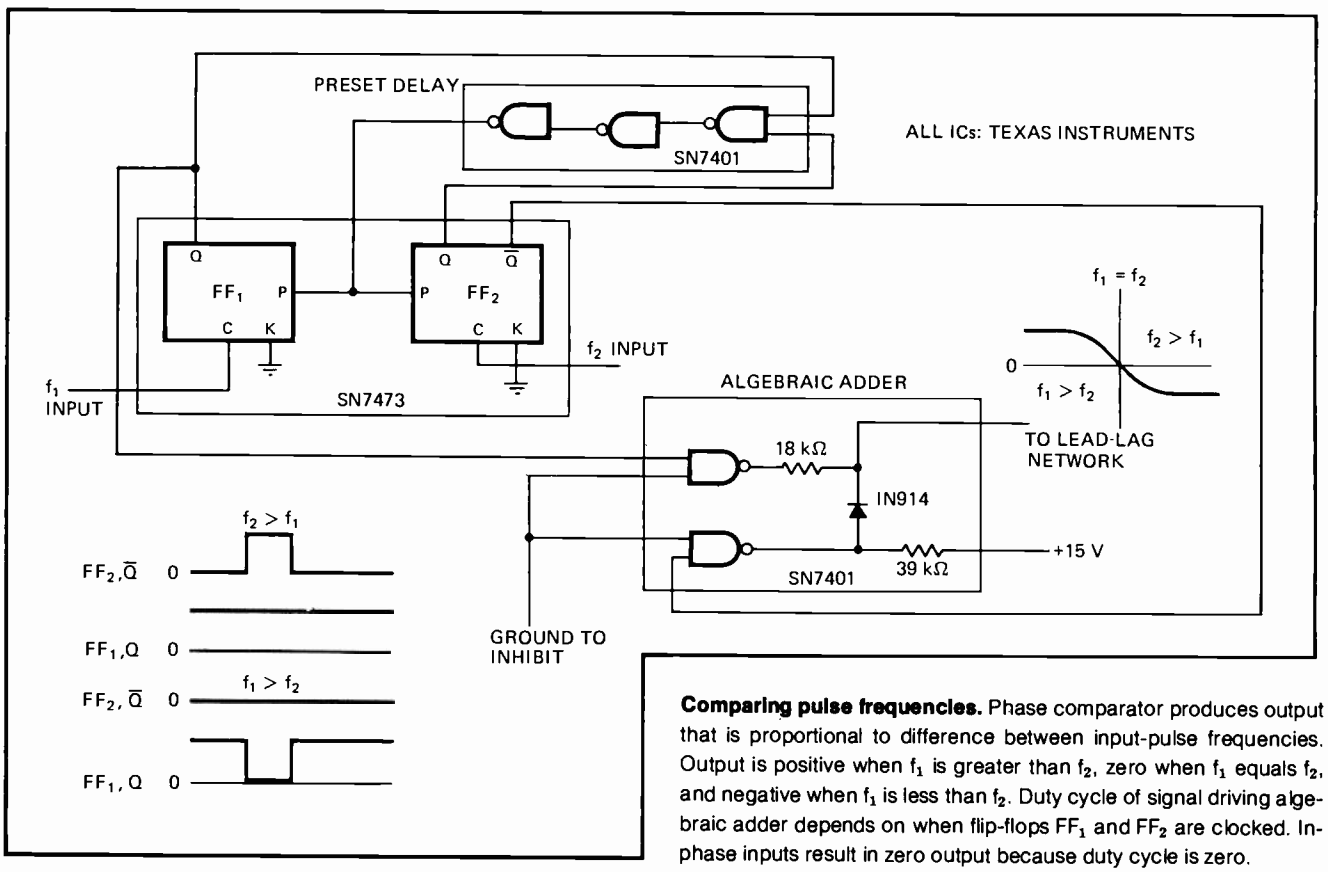
by Francis E. Adams
San Bernadino Microwave Society, Corona, Calif.

An easy-to-build phase comparator offers a number of advantages for use with dc servo motors and in voltage-controlled-oscillator loops. The output of the comparator is zero for inputs that are in phase, and, unlike the output of discriminators, it remains real, even for extreme differences in the two input-pulse frequencies. Moreover, the circuit, which is composed of low-cost, readily available ICs, can operate at a frequency that is limited only by the type of devices employed.

Both J-K flip-flops, FF_1 and FF_2, are preset so that their Q outputs are at logic 1. After an input pulse at frequency f_1 clocks FF_1 and causes its Q output to become logic 0, and an input pulse at frequency f_2 clocks FF_2 and produces a logic 0 at its Q output, the preset delay containing three NAND gates resets the flip-flops. The propagation delay time of these NAND gates assures that both flip-flops are preset.

The time lapse between FF_1 being clocked and FF_2 being clocked determines the duty cycle of the pulse train seen by the algebraic adder. As input pulse frequencies f_1 and f_2 approach each other, this duty cycle becomes smaller. When the two inputs are in phase ($f_1 = f_2$), the duty cycle is zero, except for a narrow contribution due to the preset time of the NAND gates, which is usually less than 1 microsecond.

If f_1 is greater than f_2, there is a positive output current that is proportional to the phase error. If f_2 is greater than f_1, then there is a negative output current, which is also proportional to the phase error. For $f_1 = f_2$, the output current is zero. □



Comparing pulse frequencies. Phase comparator produces output that is proportional to difference between input-pulse frequencies. Output is positive when f_1 is greater than f_2, zero when f_1 equals f_2, and negative when f_1 is less than f_2. Duty cycle of signal driving algebraic adder depends on when flip-flops FF_1 and FF_2 are clocked. In-phase inputs result in zero output because duty cycle is zero.

Diode switching matrices make a comeback

Poor noise immunity of standard logic gates has restricted diode use, but cost advantages of matrices now can be realized by constructing these networks with high-noise-immunity integrated circuits

by Dave Guzeman, *Teledyne Semiconductor, Palo Alto, Calif.*

☐ Since the advent of high-noise-immunity logic, diode switching matrices are being used more extensively in logic systems, particularly those for code conversion, because diode gates cost less than standard logic gates. Once a very popular logic building block, the diode switching matrix had lost ground because of the poor noise immunity of conventional logic gates.

The two most common 5-volt logic families, transistor-transistor logic (TTL) and diode-transistor logic (DTL), usually experience noise immunity degradation because of the voltage drop, about 0.7 V, across a forward-conducting diode. Improvement in circuit noise immunity becomes important for code conversion applications, such as decimal-to-excess-three encoders. And substituting a simple diode gate for a standard gate can reduce parts costs—often by a factor of four.

A noise immunity problem arises whenever simple diode gates are driven by conventional TTL or DTL. Since noise immunity voltage for any gate is the difference between the guaranteed input threshold voltage and the gate output voltage, the already narrow 400-millivolt noise immunity offered by most TTL is easily exceeded by the additional diode voltage drop.

Noise immunity: problem and solution

Suppose a simple diode AND gate is driven by a standard TTL active output gate whose maximum output voltage in the logic 0 state is 0.4 V. As shown in Fig. 1(a), the forward-biased diode at input A, which drops around 0.7 V, makes the logic 0 output voltage (V_{OL}) of the driving gate equal to 1.1 V. Since the guaranteed input logic 0 threshold of conventional TTL devices is 0.8 V, the noise immunity becomes 0.8 – 0.4 = 0.4 V, exceeding TTL's 400-mV noise immunity.

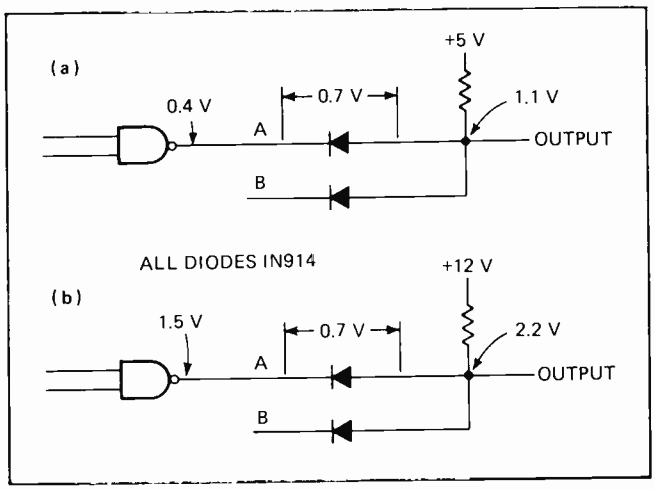
Consider the same circuit when high-noise-immunity logic is used, as indicated in Fig. 1(b). Now, the guaranteed driving gate V_{OL} increases to 1.5 V and the guaranteed input threshold increases to as high as 5 V. Adding the 0.7-V diode drop to the 1.5-V V_{OL} of the driving gate brings the output voltage of the diode AND gate to 2.2 V. The worst-case logic 0 noise immunity becomes 5 – 2.2 = 2.8 V. Many devices in high-noise-immunity families have open-collector or passive pull-up outputs whose guaranteed V_{OL} is 0.5 V. Then noise immunity of the diode AND gate is better yet: logic 0 output is 0.5 + 0.7 = 1.2 V, and noise immunity is 5 – 1.2 = 3.8 V.

This significant improvement in noise immunity over that of conventional TTL becomes important for code conversion applications; for example, decimal-to-excess-three encoders that use keyboard switch inputs. With high-noise-immunity logic, the keyboard switches can be located remotely from the logic cards, and worst-case noise immunity can be as high as 4.3 V.

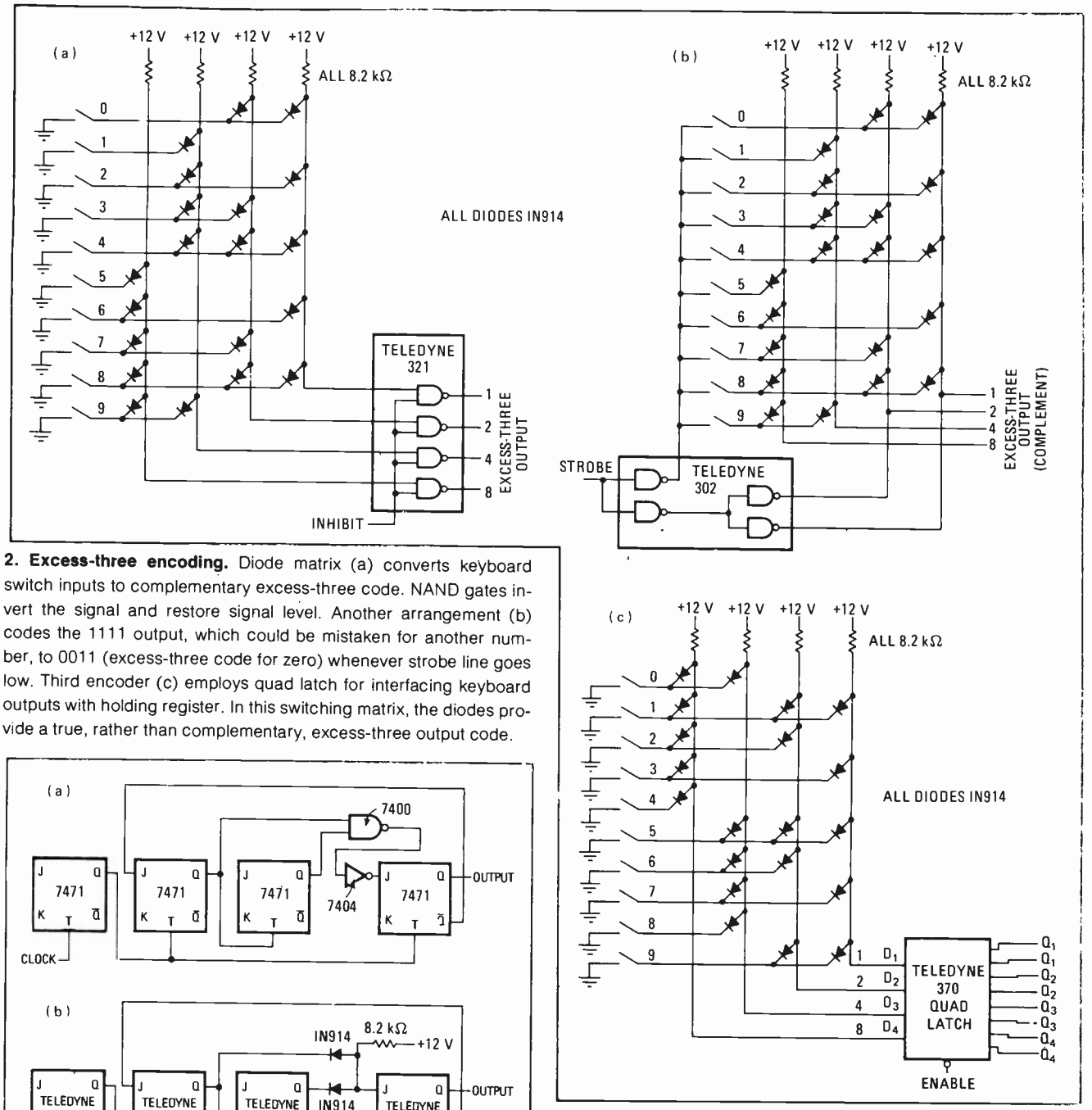
The excess-three encoder of Fig. 2(a) consists of 10 keyboard switches, four high-noise-immunity dual-input NAND gates and several diodes. Essentially, the encoder uses the same principle as the simple diode AND gate. As individual keyboard switches are closed, the diodes tied to the supply voltage through pull-up resistors become forward-biased. In this case, the diodes are wired to make the input to the NAND gates the complement of the desired excess-three code.

The NAND gates restore the input signal levels for full noise immunity in the system. An inhibit line is also provided to block or transfer data from the keyboard switches into the system logic.

This encoder, however, may present a problem since its output becomes 1111, which can be mistaken for some other number, causing an unwanted output when the inhibit line drops low. A more usable circuit is one whose output goes to 0011, the excess-three code for



1. Noise immunity. When conventional TTL gate with active output drives diode AND gate (a), noise immunity of TTL driving gate is exceeded because of the diode's forward voltage drop. Using high-noise-immunity logic driving gate (b) solves the problem since its guaranteed input threshold is 5 V, rather than the 0.8 V of standard TTL. Noise immunity, which is 0.4 V for (a), increases to 2.8 V for (b).



2. Excess-three encoding. Diode matrix (a) converts keyboard switch inputs to complementary excess-three code. NAND gates invert the signal and restore signal level. Another arrangement (b) codes the 1111 output, which could be mistaken for another number, to 0011 (excess-three code for zero) whenever strobe line goes low. Third encoder (c) employs quad latch for interfacing keyboard outputs with holding register. In this switching matrix, the diodes provide a true, rather than complementary, excess-three output code.

3. Saving dollars with diodes. Substituting a simple diode gate for standard logic gates can considerably reduce parts cost—often by a factor of four. For example, serial NAND gate and inverter (a) of BCD decoder/counter can be replaced by diode AND gate (b).

zero, rather than 1111. To implement such an encoder, shown in Fig. 2(b), several NAND gates are used to disconnect all keyboard switches from their common ground and to ground output lines 4 and 8. This corresponds to the complement of 0011. Since the NAND gates are open-collector devices, the matrix resistors serve as pull-ups for the NAND gates, while protecting their outputs from being grounded.

Another encoder variation should be implemented if the keyboard outputs must be fed into a holding register, as indicated in Fig. 2(c). Here, the diodes are connected within the matrix to provide true excess-three outputs, rather than the complementary form. These outputs then drive a quad latch, which consists of four Type D flip-flops. The latch is provided with an enable input that prevents data from being entered into the flip-flops, except when the enable line is low.

Besides encoder circuitry, diode gates can be used extensively in combinational logic. For example, many circuits in digital systems use NAND gates followed by inverters. In most instances, this common configuration can be replaced by a simple diode AND gate, at cost savings as high as four to one. The BCD decoder/counter of Fig. 3(a) provides a typical circuit for diode gate substitution. In Fig. 3(b), two diodes and a resistor replace the NAND gate and inverter. □

Approximating true log output at high frequencies

New way to build high-frequency log amplifiers eliminates interstage phase shift by using twin-gain amplifier blocks that consist of a unity-gain non-limiting amplifier and a high-gain limiting amplifier

by Douglas Clifford, *Hewlett-Packard Co., Loveland, Colo.*

☐ Many circuit analysis applications, such as those involving tuned receivers and spectrum analyzers, require displaying signals with a very broad dynamic range. Signal levels can typically vary from −120 to + 10 decibels referred to 1 milliwatt. But to display even a portion of such a signal requires some form of compression. Usually the signal is processed by forming a logarithmic function of signal level.

A recently developed technique eliminates the objections of poor frequency response above 5 megahertz that is characteristic of the previously least complicated method, successive limiting. The new design is similar to successive limiting, but it eliminates interstage phase shift by using twin-gain amplifier blocks to approximate the log curve as a series of straight lines.

Comparing approximation methods

Successive limiting, or linear approximation, is the most sophisticated of three traditional nonlinear methods, which use progressively more complex compensating circuitry to improve accuracy. The new twin-gain amplifier technique achieves accuracy with no compensating circuitry.

The method that requires heaviest compensation employs feedback with a nonlinear element. Generally, a transistor's base-emitter junction is used, since its characteristic is exponential.

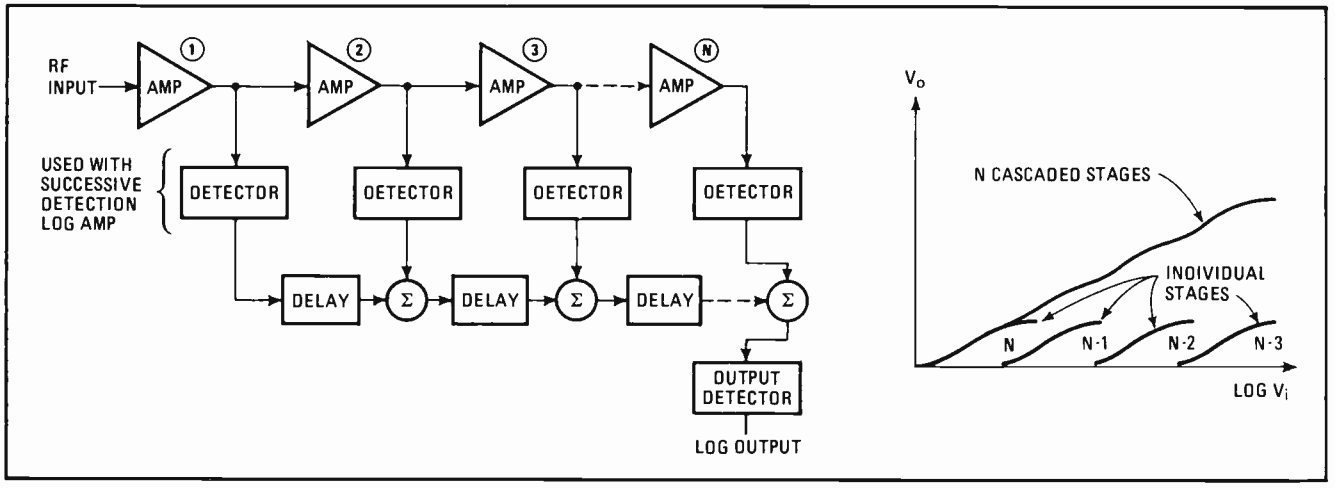
The second technique, which can achieve equal accuracy with less compensating circuitry, is also based on an exponential characteristic—that of transistor collector current. A single, simple transistor amplifier can usually provide exponential gain over a range of more than 20 dB. For larger dynamic ranges, transistors must be cascaded with intervening gain blocks to allow each stage to operate within its range.

The third method, successive limiting, has been the most popular at high frequencies because of its simplicity. Successive limiting approximates the logarithmic curve by summing either the rf signal outputs or the detected video signal outputs of a series of linear amplifiers that limit at a predetermined level. Figure 1 illustrates the circuit and its output characteristic.

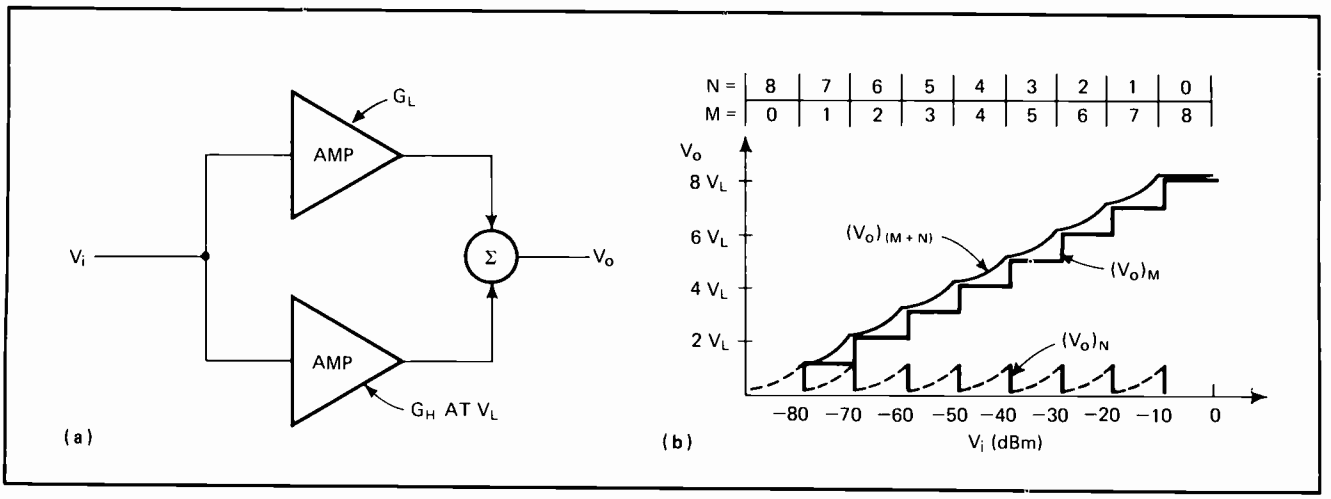
Poor frequency response is the main limitation of successive limiting. At frequencies above 5 MHz, phase shift between stages causes the rf signal components to be summed out of phase, and the logarithmic response deteriorates unless delay networks are inserted.

In applications where the log of the rf signal must be detected before further processing, detectors can be placed at the output of each amplifier. This solves the phase shift problem, but complicates circuitry and increases over-all thermal sensitivity because the detectors do not track each other as temperature changes.

A recently developed technique eliminates both the



1. Successive limiting. Summing the outputs of cascaded limiting amplifiers yields logarithm of input signal. Limited output of each stage is added to that of previous stage to approximate log curve. Delay networks become necessary when operating above 5 megahertz to compensate for phase shift between stages. Optional detectors allow rf signal to be detected before additional processing.



2. Double-amplifier log stage. Twin-gain amplifier block (a) can be cascaded to form log amplifier that does not need phase-shift correction. Low-gain (G_L) amplifier does not limit input signals, but high-gain (G_H) amplifier does, at limit level V_L. For logarithmic output to result, G_L must be unity. Plot (b) shows how eight cascaded stages of twin-gain amplifiers approximate log curve. Final output voltage, $(V_o)_{(M+N)}$, reflects addition of outputs from both limiting (M) and non-limiting (N) stages for total signal range of −80 to 0 dBm.

need for multiple detectors and rf phase shift problems. The method is similar to successive limiting, because a number of identical blocks are used with output characteristics that approximate the log curve with a series of straight lines.

As shown in Fig. 2(a), the signal is applied simultaneously to two amplifiers that form a twin-gain circuit. The low-gain (G_L) amplifier does not limit an input signal, but the high-gain (G_H) amplifier does, limiting it at a voltage level of V_L. The relationship between output voltage (V_o) and input voltage (V_i) can be written as:

$$V_o = V_i(G_H + G_L)$$

when V_i is less than V_L/G_H, and:

$$V_o = V_iG_L + V_L$$

when V_i is greater than V_L/G_H.

If V_i is less than $V_L/(G_H + G_L)^N$, the limit level for N cascaded amplifier blocks, the overall amplifier will be linear. However, when the magnitude of V_i causes the high-gain amplifiers in each block to limit, the system becomes nonlinear.

When all the stages are limiting, the output of one is still the input drive to the next. For M stages driven into limiting:

$$(V_o)_M = V_L(1 + G_L^2 + G_L^3 + \ldots + G_L^{M-1}) + V_iG_L^M$$

Combining N stages of non-limiting blocks and M stages of limiting blocks gives:

$$(V_o)_{(M+N)} = V_L(1 + G_L + G_L^2 + \ldots + G_L^{M-1}) + V_iG_L^M(G_H + G_L)^N$$

If G_L is set to unity, then:

$$(V_o)_{(M+N)} = V_LM + V_i(G_H + 1)^N$$

The maximum non-limiting gain for N stages is found by setting M = 0 and letting $V_o = V_L$:

$$(G_H + 1)^N = V_L/V_i$$

or:

$$N = \log(V_L/V_i)/\log(G_H + 1)$$

Substituting T = M + N, where T is the total number of gain blocks:

$$M = T + \log(V_i/V_L)/\log(G_H + 1)$$

If G_H and V_L are the same for each block, this equation reduces to:

$$M = K_2 + K_1\log(V_i)$$

where $K_1 = 1/\log(G_H + 1)$ and $K_2 = T - K_1\log(V_L)$

Since $V_i(G_H + 1)^N$ is greater than or equal to V_L:

$(V_o)_{(M+N)} = V_LM + V_X$, for V_X between 0 and V_L.

This last equation indicates that V_o is proportional to M, which is in turn related to $\log(V_i)$, making V_o proportional to the log of the input. It should also be noted that G_L must equal unity for the log approximation to hold.

A plot of the two parts of $(V_o)_{(M+N)}$ illustrates the logarithmic relationship between the output and the input. As an example, the graph of Fig. 2(b) results for cascaded twin-gain blocks when M + N = 8, $G_H + 1$ = 10 dB, and V_L = 0 dB into 50 ohms. Assuming G_L = 1 and N = 0 yields the output of M limiting blocks:

$$(V_o)_M = V_LM$$

And setting M = 0 and keeping G_L = 1 gives the output voltage for N non-limiting blocks:

$$(V_o)_N = V_i(G_H + 1)^N$$

The graph shows the contributions of both $(V_o)_M$ and $(V_o)_N$ for all combinations of M and N. The two outputs are simply added together for a total output voltage. Both output voltage level and input signal range become larger with increasing M and decreasing N.

From theory to hardware

A log amplifier with almost any given dynamic range and log fidelity can be constructed with twin-gain amplifier blocks. The fewer the stages used, the more gain each stage must provide for a given range, and the greater the deviation from the actual log curve.

The computer printout of Fig. 3 compares an eight-stage log amplifier to a five-stage one. For both computations, the maximum and minimum errors (differences) between the calculated values of $(V_o)_{(M+N)}$ and the actual log of V_i are printed. Also shown are the computed output voltages for inputs from −80 to −10 dBm. Output voltage figures are normalized to reflect a 1-V output change for a 10-dB input step.

The calculation for the eight-stage log amplifier, in Fig. 3(a), indicates a maximum error of 0.03 V and a minimum error of 0 V when G_H = 6.68 dB and V_L = −1 dBm into 50 ohms. (Here, maximum error represents

```
(a) GAIN DB,LIMIT  ?6.68,-1

   MAX ERROR= 3.12457E-02     MIN ERROR= 0
   DB=            -80         VOUT=          1.00247
   DB=            -70         VOUT=          2.00211
   DB=            -60         VOUT=          3.00176
   DB=            -50         VOUT=          4.0014
   DB=            -40         VOUT=          5.00105
   DB=            -30         VOUT=          6.0007
   DB=            -20         VOUT=          7.00035
   DB=            -10         VOUT=          8

(b) GAIN DB,LIMIT  ?14,-5
                               VMAX= .699427
   MAX ERROR= 8.13584E-02     MIN ERROR= 8.99811E-02
   DB=            -80         VOUT=          .979577
   DB=            -70         VOUT=          2.07618
   DB=            -60         VOUT=          3.00364
   DB=            -50         VOUT=          3.92999
   DB=            -40         VOUT=          5.01443
   DB=            -30         VOUT=          5.98255
   DB=            -20         VOUT=          6.91574
   DB=            -10         VOUT=          8
```

3. Computer comparison. Printouts for eight-stage (a) and five-stage (b) twin-gain log amplifiers list normalized (1 V = 10 dB) output voltage for inputs from -80 to -10 dBm. Maximum and minimum errors across this range are computed as difference between calculated $(V_o)_{(M+N)}$ and actual log of V_i. Eight-stage amplifier, whose G_H = 6.68 dB and V_L = -1 dBm, gives maximum error of 0.03 V and minimum error of 0 V. Five-stage amplifier, with G_H = 14 dB and V_L = -5 dBm, provides errors of 0.08 V max and 0.09 V min.

the largest positive deviation from the desired output, and minimum error the largest negative.) Error levels are higher for the five-stage amplifier, as indicated in Fig. 3(b), with G_H = 14 dB and V_L = -5 dBm into 50 ohms. Maximum error becomes 0.08 V, while minimum error is about 0.09 V, bringing the peak-to-peak error to 0.17 V or 1.7 dB.

As can be seen from the circuit equations, the critical design parameters are limit level V_L and high gain G_H. These quantities are influenced by the desired log range and number of stages. A computer program is generally used to determine them for the dynamic range and log fidelity desired.

One way to implement a twin-gain log amplifier is to use two differential transistor pairs driven in parallel and feeding a common load, as illustrated in Fig. 4(a). Transistors Q_1 and Q_2 form the unity-gain amplifier, while transistors Q_3 and Q_4 provide a high gain of G_H and limit at V_L. This design, it should be noted, is completely analogous to the theoretical model. Differential pairs are used because of the excellent limiting they provide when they are overdriven.

The gain of the low-gain amplifier is:

$$G_L = R_L/(2R_1+2r_{e'}) = R_L/(2R_2+2r_{e'}) = 1$$

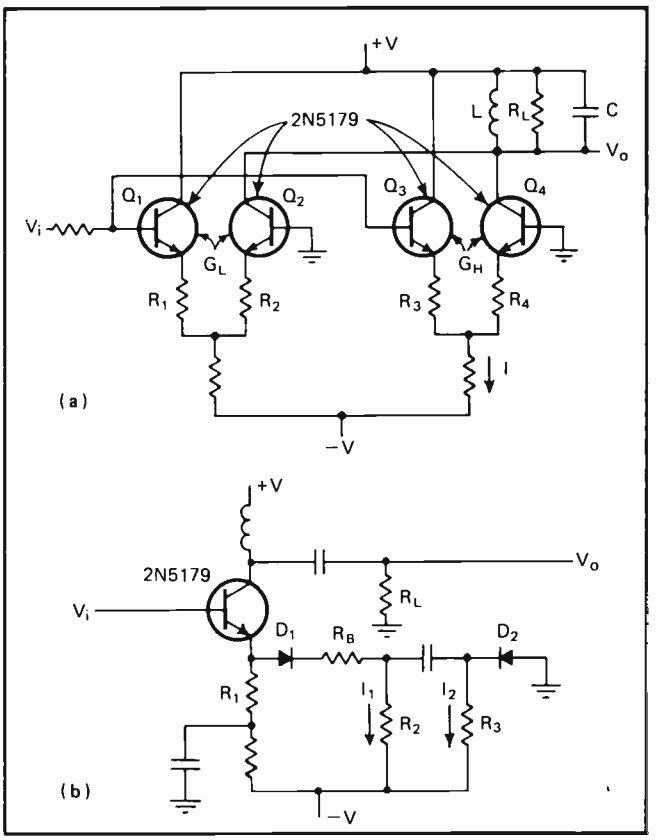
where $R_1 = R_2$, and $r_e{}'$ is transistor dynamic emitter resistance. High gain G_H is determined by:

$$G_H = R_L/(2R_3+2r_{e'}) = R_L/(2R_4+2r_{e'})$$

where $R_3 = R_4$. Limit level V_L is fixed by the peak-to-peak current swing allowed in R_L due to the high-gain amplifier:

$$V_L = IR_L$$

Usually, G_H and V_L are found first from a computer model of the circuit. Actual resistor values can then be determined from the equations. Amplifier bandwidth is established by components R_L, L and C. Transistors should be chosen so that amplifier input and output capacitances are small to obtain broadband frequency performance.



4. Building a log amp. Two differential pairs (a) drive common load to realize twin-gain log amplifier. Limit level V_L of high-gain (G_H) pair is determined by allowable peak-to-peak current through R_L. Single transistor (b) can also be used. When diodes are forward-biased, amplifier gain is G_H, and limit level is fixed by current flowing in diode limiter. For both circuits, low gain G_L is unity.

Another design method, shown in Fig. 4(b), uses the same amplifier to provide both G_L and G_H. Diodes D_1 and D_2 are forward-biased for small signal levels so that:

$$G_H = R_1/(R_B+2r_b) = R_L/(R_B+2r_b)$$

where $R_1 = R_L$, and r_b is diode resistance. Low gain G_L is obtained through the emitter resistance path:

$$G_L = R_L/R_1 = 1$$

The limit level for the high-gain portion of the amplifier is determined by how much current is flowing in the diode limiter:

$$V_L = I_1R_2 + I_2R_3$$

where V_L is the peak-to-peak voltage of the limit level. When the signal begins to reverse-bias the diodes, turning them off, the effective transistor emitter resistance increases, and gain drops. The final amplifier gain approaches unity.

Test results for this log amplifier configuration verify its predicted performance. An eight-stage amplifier, for example, with a nominal operating frequency of 20 MHz, provides an 80-dB input range for signal levels from -80 to 0 dBm. Moreover, its maximum output deviation from a true log curve is only 0.3 dB. For this tight peak-to-peak ripple performance, the emitter resistors must be adjusted to assure that G_L = 1 when a stage is limited. □

Doubling op amp summing power

Design equations make calculations for non-inverting amplifier input as simple as those for inverting input so that amplifier efficiency is maximized when several signals are summed at the same time

by Raymond G. Kostanty, *Bendix Corp., Navigation and Control division, Los Angeles, Calif.*

☐ Summation of multiple signals is a useful circuit technique whenever more than one signal must be amplified or attenuated with a single amplifier—for example, in instruments or avionics equipment. And the versatile operational amplifier makes it possible to sum simultaneously on both its inverting and non-inverting inputs.

Unfortunately, designers frequently utilize only the inverting input because calculations for the non-inverting input are usually tedious. A common practice is to use the inverting input of another amplifier, rather than going through the mathematics for the non-inverting input of a single stage.

A new set of equations simplifies summation circuit design by making the resistors for one input as easy to calculate as the resistors for the other. Thus, a single op amp may perform as well as two that use only the inverting input.

Relationships between signal gain, input and feedback resistors, and input and output voltages are uncomplicated for the inverting input, and each can be handled separately. But previously, the non-inverting input required the solution of simultaneous equations—one equation for each applied input. Although these equations were only first-order functions, their solution could become cumbersome for three or more inputs.

The new equations use up to two grounded resistors—one for each side of the amplifier—to control available amplifier gain. This technique permits all signal gains and all input resistors to be calculated without simultaneous equations and with only simple arithmetic.

Circuit functions are elementary

A few basic assumptions are necessary to minimize equation complexity. The amplifier, for example, is assumed to have infinite gain, infinite input resistance, and zero output resistance. Moreover, each of the amplifier's inputs is considered to be directly coupled from a low-impedance source resistance.

The equations set the dc resistance from the amplifier's inverting input to ground equal to the dc resistance from its non-inverting input to ground. This minimizes output null shift with changing temperature.

Output/input relationships for the fundamental amplifier configuration of Fig. 1 are easily defined. Let E_o be output voltage, E_I an input voltage at the inverting terminal, and E_N an input voltage at the non-inverting terminal. For the inverting amplifier input:

$E_o/E_{I1} = K_{I1}$, $E_o/E_{I2} = K_{I2}$, and $E_o/E_{IN} = K_{IN}$

where K_I represents the desired gain of the signal applied to the inverting input, and subscripts 1 through N designate signal number. For the non-inverting input:

$E_o/E_{N1} = K_{N1}$, $E_o/E_{N2} = K_{N2}$, and $E_o/E_{NN} = K_{NN}$

where K_N is the desired signal gain through the non-inverting input. Once a convenient value for feedback resistor R_F is selected, the input resistors can be found:

$$R_{I1} = R_F/K_{I1},\ R_{I2} = R_F/K_{I2}, \text{ and } R_{IN} = R_F/K_{IN} \quad (1)$$

$$R_{N1} = R_F/K_{N1},\ R_{N2} = R_F/K_{N2}, \text{ and } R_{NN} = R_F/K_{NN} \quad (2)$$

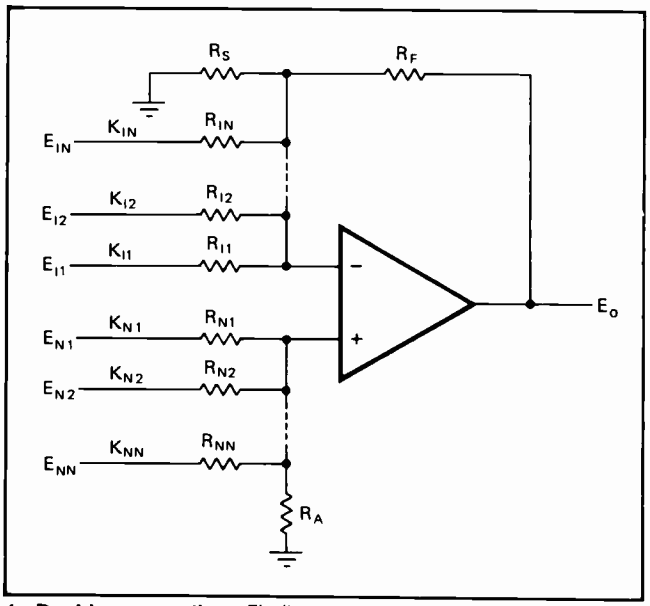
The values of resistors R_S and R_A depend on the relationship of the sum of the inverting gains to the sum of the non-inverting gains.

Let: $\Sigma K_{IN} = K_{I1} + K_{I2} + \ldots + K_{IN}$

and: $\Sigma K_{NN} = K_{N1} + K_{N2} + \ldots + K_{NN}$

If: $1 + \Sigma K_{IN}$ is greater than or equal to ΣK_{NN} (3)

then: $R_S = \infty$



1. Double summation. Finding resistor values when signals are summed at both inverting (I) and non-inverting (N) inputs of op amp can be reduced to elementary calculations. Up to N inputs to either terminal can be accommodated. Simple equations relate input and output voltages to signal gain. Input resistor values depend on R_F and signal gain: $R_{IN} = R_F/K_{IN}$, and $R_{NN} = R_F/K_{NN}$. Resistors R_S and R_A are determined after comparing gain summations.

and: $R_A = R_F/(1+\Sigma K_{IN} - \Sigma K_{NN})$ (4)
If: $1 + \Sigma K_{IN}$ is less than ΣK_{NN} (5)
then: $R_S = R_F/(K' - \Sigma K_{IN})$ (6)
and: $R_A = R_F/(1+K' - \Sigma K_{NN})$ (7)
where: $K' = R_F/R_S + \Sigma K_{IN}$ (8)

If Eq. 5 rather than Eq. 3 is satisfied, a minimum value is arbitrarily assigned to K', which represents the sum of the inverting gains:

K' must be greater than or equal to $\Sigma K_{NN} - 1$ (9)

Utilizing the results

Using these equations is not difficult and can be illustrated by a few examples. Suppose that an amplifier must be designed for $K_{I1} = 1$, $K_{I2} = 2$, $K_{N1} = 0.5$, and $K_{N2} = 2$; all other inputs are zero. First, a convenient value must be chosen for R_F. (It should be noted that the overall resistance level of the final circuit is proportional to R_F, and that amplifier offset current limits the maximum value of R_F.) Selecting an arbitrary R_F of 50 kilohms allows values of the input resistors to be found with Eqs. 1 and 2:

$R_{I1} = 50k/1 = 50$ kilohms
$R_{I2} = 50k/2 = 25$ kilohms
$R_{N1} = 50k/0.5 = 100$ kilohms
$R_{N2} = 50k/2 = 25$ kilohms

Since $\Sigma K_{IN} = 3$ and $\Sigma K_{NN} = 2.5$, Eq. 3 is satisfied:

$1 + 3$ is greater than or equal to 2.5

so that:

$R_S = \infty$

and from Eq. 4:

$R_A = 33.3$ kilohms

The final design is illustrated in Fig. 2(a). If signal conditions remain the same, but another input, $K_{I3} = 3$, is added, input resistor values do not change, and:

$R_{I3} = 50k/3 = 16.7$ kilohms

Because Eq. 3 is still satisfied, $R_S = \infty$, but:

$R_A = 11.1$ kilohms

Figure 2(b) shows this completed design.

If a non-inverting, rather than inverting, input is added to the first amplifier example, resistor values, when R_F is 50 kilohms, are unchanged for R_{I1}, R_{I2}, R_{N1}, and R_{N2}. For the new input, $K_{N3} = 3$:

$R_{N3} = 50k/3 = 16.7$ kilohms

Equation 3 is no longer satisfied, since $\Sigma K_{IN} = 3$ and $\Sigma K_{NN} = 5.5$, but Eq. 5 is:

$1 + 3$ is less than 5.5

Now, the minimum value of K' is found from Eq. 9:

K' is greater than or equal to $5.5 - 1 = 4.5$

Using this value for K', R_S and R_A can be computed with Eqs. 6 and 7, respectively:

$R_S = 33.3$ kilohms
$R_A = \infty$

The finished circuit is shown in Fig 2(c). If some of the non-inverting gains are expected to increase or some of the inverting gains to decrease, a larger value for K', such as 8, would be more appropriate. Resistors R_S and R_A then become $R_S = 10$ kilohms and $R_A = 14.3$ kilohms, as indicated in Fig. 2(d).

Modified designs

Given an existing circuit, it is possible to modify it with the design equations. Suppose non-inverting gain must be increased by 20% for the amplifier of Fig. 3(a), in which $R_F = 50$ kilohms, $R_{I1} = 25$ kilohms, $R_{I2} = 50$ kilohms, $R_{N1} = 10$ kilohms, $R_S = 16.7$ kilohms, and $R_A = 25$ kilohms. Existing signal gains must be determined first, using Eqs. 1 and 2:

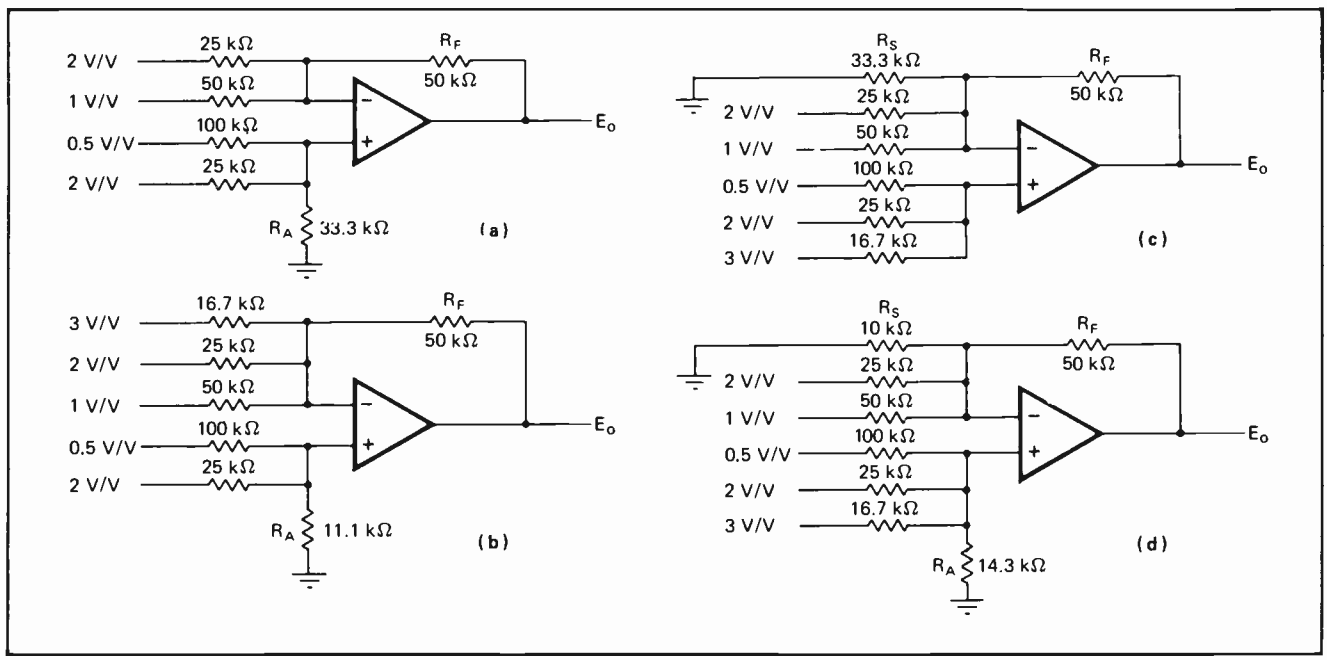
$K_{I1} = 50k/25k = 2$
$K_{I2} = 50k/50k = 1$
$K_{N1} = 50k/10k = 5$

Next, find K' for $\Sigma K_{IN} = 3$. From Eq. 8:

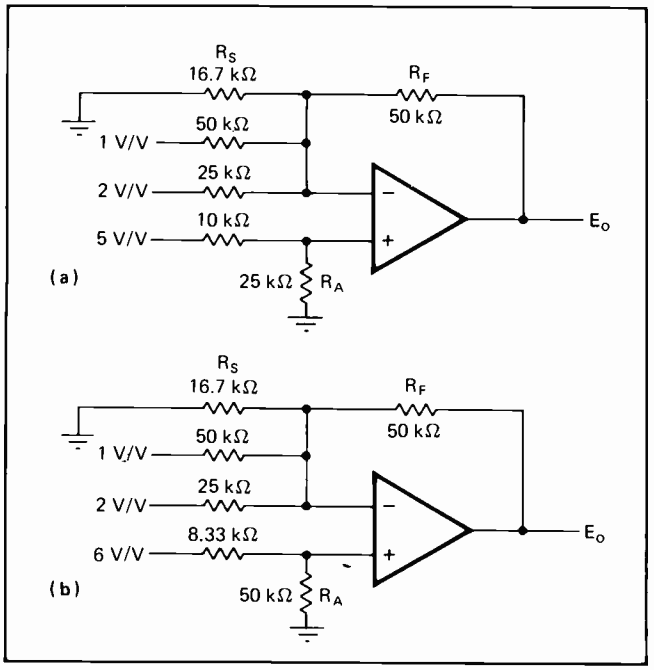
$K' = 50k/16.7k + 3 = 6$

For the modified circuit, K_{N1} must be 20% higher, or:

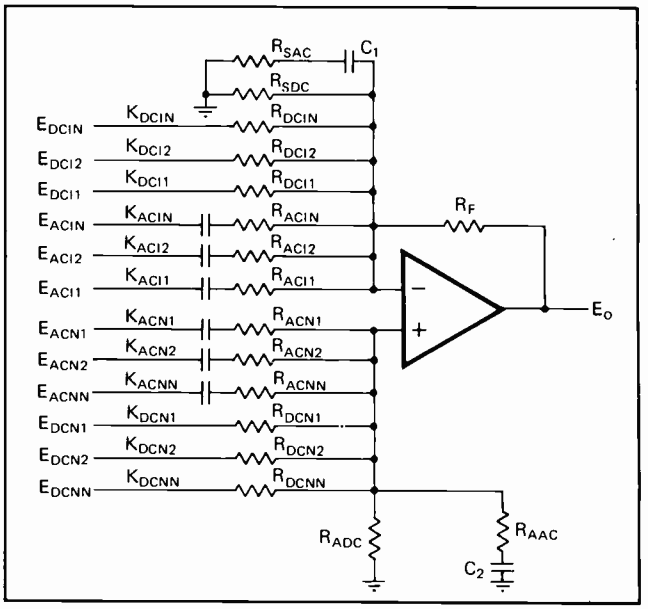
$K_{N1} = 5(1.2) = 6$



2. Amplifier examples. When another inverting input is added to amplifier (a), as in (b), values of existing input resistors are not affected, but R_A changes value. If non-inverting input is added instead, as in (c), R_S becomes necessary and R_A is eliminated. Amplifier (d) is final design for modified version of (c) that can handle increased non-inverting gains or decreased inverting gains.



3. Making changes. New design equations are also useful for modifying existing circuits. When non-inverting gain of amplifier (a) is increased by 20%, from 5 to 6, resistors to inverting input are unaffected. As shown in (b), only R_{N1} and R_A must be changed.



4. Generalized amplifier. For complete design analysis, both ac (AC) and dc (DC) elements and signals must be taken into account. Dc relationships are simply those developed for amplifier of Fig. 1. And ac solutions for signal gain and input resistors are identical, but involve ac quantities. Since computing R_{SAC} and R_{AAC} requires both ac and dc parameters, dc solution should always be found first.

Checking the minimum value for K′ with Eq. 9:

K′ = 6 is greater than or equal to 6 - 1

Since the inequality holds, K′ = 6 is satisfactory.

The value of R_S does not change because K′ and the inverting signal gains remain the same, but:

R_{N1} = 50k/6 = 8.33 kilohms

and from Eq. 7:

R_A = 50k/(1+6 - 6) = 50 kilohms

The modified amplifier circuit is drawn in Fig. 3(b). Instead of just a 20% increase, suppose K_{N1} is doubled in value to 10. Since the minimum K′ now changes:

K′ is greater than or equal to 10 - 1 = 9

Select K′ = 10, then:

R_{N1} = 50k/10 = 5 kilohms

R_S = 50k/(10 - 3) = 7.13 kilohms

R_A = 50k/(11 - 10) = 50 kilohms

All the design equations developed assume that the impedance of a source resistance is low and can effectively be neglected. However, this is not always true. If source resistances are some constant known values, the equations are easily modified. Simply subtract a given source resistance from the appropriate calculated input resistor. For example, if R_F is 50 kilohms, K_{I1} is 2, and the source resistance driving E_{I1} is 2 kilohms, then:

R_{I1} = 25k - 2k = 23 kilohms

Ac considerations

Amplifier inputs can also be capacitively coupled. The generalized amplifier configuration of Fig. 4 shows both ac and dc circuit elements and parameters. (Of course, subscript AC denotes an ac element or signal, while subscript DC is for a dc element or signal.)

Although the equations used thus far involve only dc quantities, ac signal analysis parallels the dc. Ac output/input relationships, for instance, are the same as those for a dc signal:

$E_o/E_{ACIN} = K_{ACIN}$ and $E_o/E_{ACNN} = K_{ACNN}$

And input resistor computations are also equivalent:

$R_{ACIN} = R_F/K_{ACIN}$ and $R_{ACNN} = R_F/K_{ACNN}$

The values for resistors R_{SAC} and R_{AAC}, however, depend on both ac and dc signal conditions.

If: $1 + \Sigma K_{DCIN} + \Sigma K_{ACIN}$ is greater than or equal to $\Sigma K_{DCNN} + \Sigma K_{ACNN}$

then: $R_{SAC} = \infty$

and: $(R_{ADC}R_{AAC})/(R_{ADC}+R_{AAC}) = R_F/(1+\Sigma K_{DCIN}+\Sigma K_{ACIN} - \Sigma K_{DCNN} - \Sigma K_{ACNN})$

If: $1 + \Sigma K_{DCIN} + \Sigma K_{ACIN}$ is less than $\Sigma K_{DCNN} + \Sigma K_{ACNN}$

then: $(R_{SAC}R_{SDC})/(R_{SAC}+R_{SDC}) = R_F/(K'_{AC} - \Sigma K_{DCIN} - \Sigma K_{ACIN})$

and: $(R_{AAC}R_{ADC})/(R_{AAC}+R_{ADC}) = R_F/[1 + K'_{AC} - (\Sigma K_{DCNN}+\Sigma K_{ACNN})]$

where: $K'_{AC} = R_F/R_{SDC} + \Sigma K_{DCIN} + R_F/R_{SAC} + \Sigma K_{ACIN}$

And the minimum value for K'_{AC} becomes:

K'_{AC} is greater than or equal to $\Sigma K_{DCNN}+\Sigma K_{ACNN} - 1$

When using these equations to analyze a circuit, the dc properties must be calculated before tackling any ac problems. Of course, the dc input resistors and R_{SDC} and R_{ADC} are computed with Eqs. 1 through 9.

A few practical circuit considerations should also be remembered. Signal frequencies applied to capacitive inputs should be at least 100 times greater than the maximum frequency on the direct inputs so that capacitors C_1 and C_2 can properly isolate frequency bands. And time constants C_1R_{SAC} and C_2R_{AAC}, as well as the time constant formed by each input capacitor with its input resistor, should be about $0.1/6.28f_{ac}$ seconds, where f_{ac} is the lowest frequency on any of the capacitive inputs. □

One-shot timing performance: don't take it for granted

Study of industry standard monostable multivibrator—the 9601-type of one-shot—reveals that vendor-to-vendor variations in timing accuracy are wide enough to prevent device interchangeability

by David E. Green, *Honeywell Information Systems Inc., Billerica, Mass*

☐ All too often, designers presume that a component's data sheet is precise. Inaccurate performance specifications are not intentional misrepresentations on the part of the manufacturer. Instead, they result from problems inherent in processing techniques, device geometries, or packaging effects. But, no matter what its cause, excessive performance variations—particularly those of so-called building blocks that can be used in a number of applications and that are readily available off-the-shelf from several manufacturers—must be brought to the designer's attention.

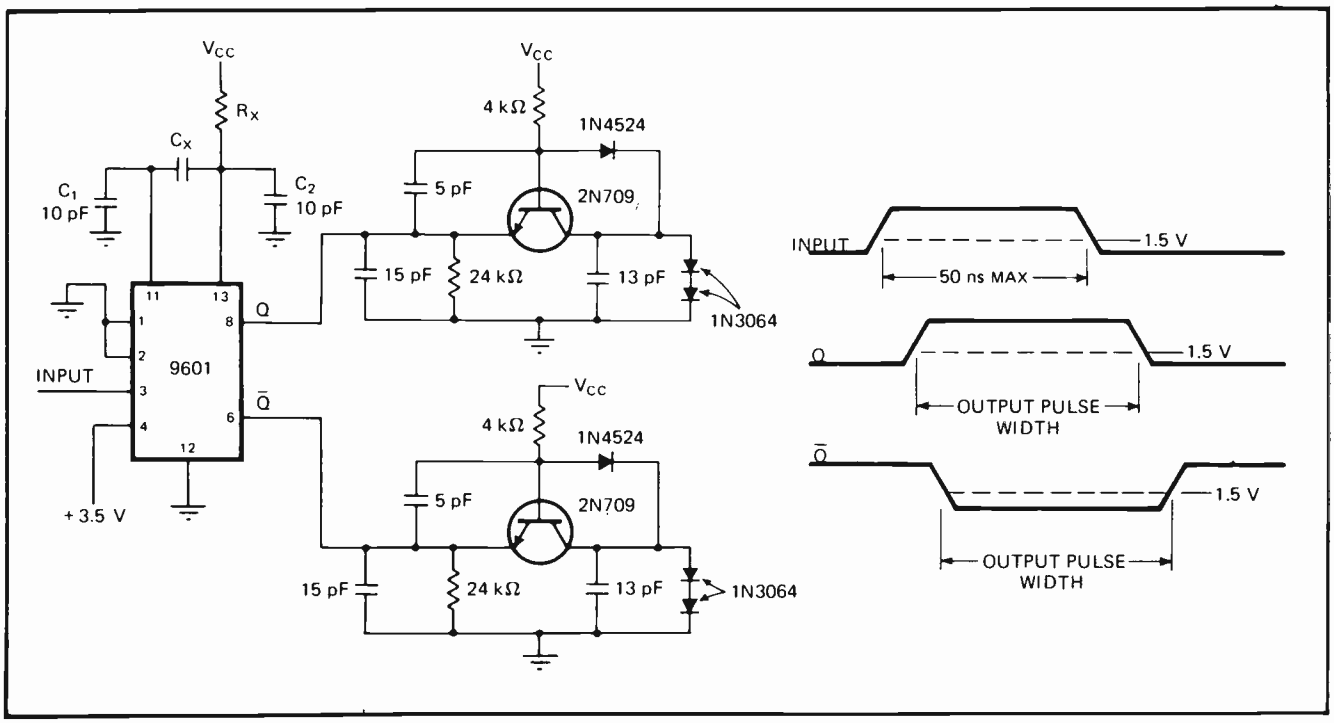
Consider, for example, the industry standard retriggerable monostable multivibrator, typified by the 9601. A recent study of a dozen sample lots of these one-shots from several different companies shows that the variations in output pulse width are so severe—sometimes approaching 60%—that some manufacturers are re-evaluating their current designs, whereas others are already in the process of redesign.

Timing errors become especially significant for small values of timing capacitance. For instance, the one-shot's minimum true output pulse is specified to have a maximum value of 65 nanoseconds, but approximate extremes of 30 and 92 ns were observed.

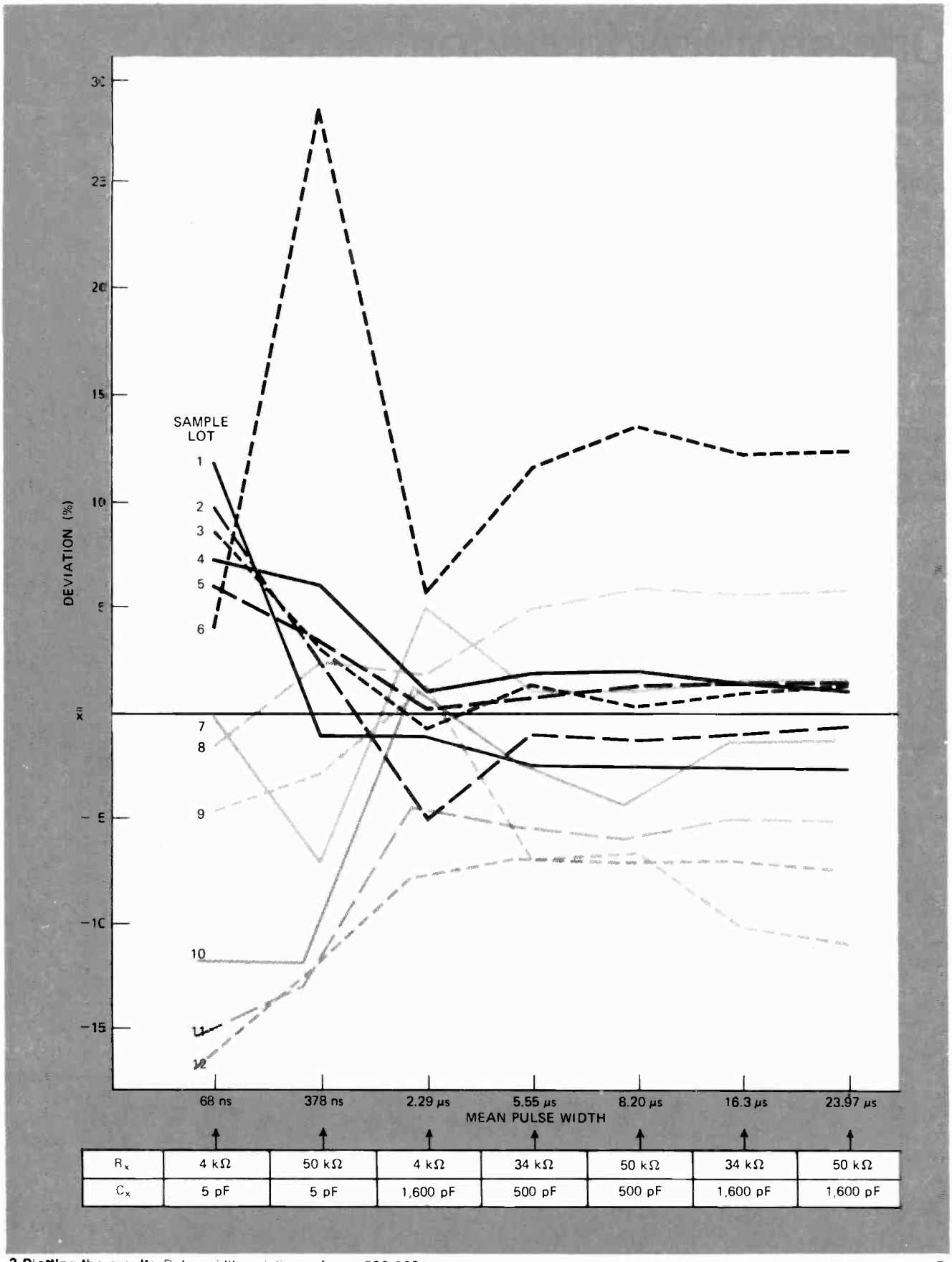
Examining the problem

Pulse width variation for the monostable is specified at a minimum of 3.08 microseconds and a maximum of 3.76 μs about a nominal output of 3.42 μs. Or, in-specification variations of timing accuracy can be thought of as ±10%. Therefore, after accounting for timing resistor and timing capacitor tolerances, as well as supply voltage variations, the designer must deal with an overall timing limit tolerance of ±15% to ±20%, making any additional one-shot timing inaccuracies difficult to handle.

Adding a trimmer potentiometer is the simplest way to compensate for this wide tolerance spread, or even poor one-shot timing—but an acceptable trimmer is



1. Testing the one-shot. Test circuit for retriggerable monostable multivibrator employs unit TTL load on each output. Timing network formed by R_X and C_X determines output pulse width at Q and $\bar{Q}$. Capacitors C_1 and C_2 are fixed at 10 picofarads (including stray capacitance and fixture capacitance), and minimum C_X is held to 5 pF. Output pulse width is measured at device's low-level logic threshold.



R_x	4 kΩ	50 kΩ	4 kΩ	34 kΩ	50 kΩ	34 kΩ	50 kΩ
C_x	5 pF	5 pF	1,600 pF	500 pF	500 pF	1,600 pF	1,600 pF

2. Plotting the results. Pulse width variations of over 500 9601-type one-shots are shown as percentage deviation from mean pulse width ($\bar{x}$) for entire group. Test points for 12 sample lots are plotted individually. Values noted for R_X and C_X are those used to obtain indicated mean pulse widths from 68 ns to 24 µs. Scattered distribution of results indicates significant discrepancy between actual and specified timing performance. Also, output pulse variations from one vendor to next are so great that parts cannot be used interchangably.

generally more expensive than the multivibrator itself. And for most printed circuit boards, no provision is made for adding a trimmer at some later date if a problem arises.

Specified one-shot timing accuracy implies that the part holds pulse-width variations to ±10% for outputs above and below the nominal 3.4-μs value. However, extensive testing of over 500 of these multivibrators shows that this is not true. The study notes the variation in output pulse width for 12 sample lots of 9601-type one-shots from a number of different vendors.

The test circuit used is illustrated in Fig. 1. Stray capacitance and capacitance from the test fixture are represented by capacitors C_1 and C_2. The total value for Sach of these capacitors is fixed at 10 picofarads to permit the use of a variety of test fixtures. Timing capacitance C_X is held to a minimum value of 5 pF since the minimum data sheet value of 0 pF is not really achievable in practice.

Both Q and $\bar{Q}$ outputs are terminated with a unit transistor-transistor logic load and a 15-pF load capacitor that includes probe capacitance. (In this case, a unit load is the equivalent of a standard TTL gate that requires the one-shot to supply 60 microamperes for its high output and to sink 1.4 milliamperes for its low output.)

All pulse widths for the study were measured at the low-level logic threshold of the Q output.

The graph of Fig. 2 summarizes test results by comparing the mean pulse width for each sample lot ($\bar{x}$) to the mean pulse width for all the units tested ($\bar{\bar{x}}$). Final values of $\bar{\bar{x}}$ are indicated along the horizontal axis, showing the mean pulse width obtained for the timing components used. For every combination of timing component values, there is a set of 12 data points, each point representing the percentage deviation of mean pulse width $\bar{x}$ for a given vendor from the group mean width of $\bar{\bar{x}}$, which ranges from 68 ns to 24 μs.

Analyzing test results

Several observations can be made from the graph. For instance, the data point at 2.29 μs, near the standard test point of 3.4 μs, suggests that the number of units meeting specification is not very high since deviations from $\bar{\bar{x}}$ are significant. Also the ±10% tolerance band is drastically exceeded for several pulse widths, indicating a serious discrepancy from predicted performance.

For some sample lots, output pulse width diverges from its specified value as pulse width increases, even though published timing data states that the output width should be linearly related to timing component values when C_X is greater than 1,000 pF.

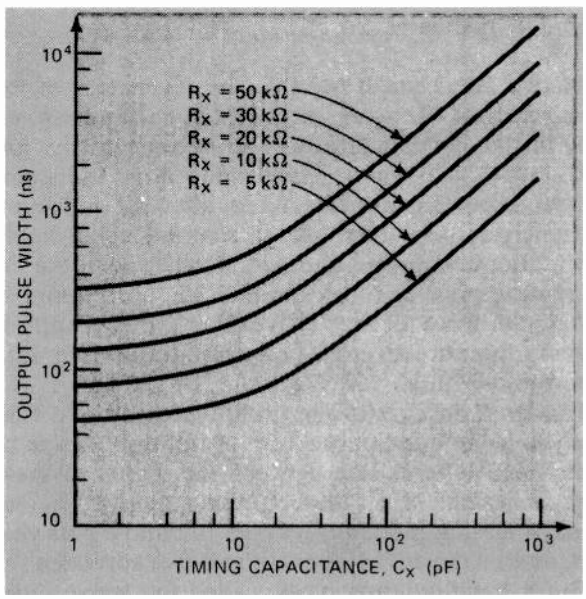
In addition, for narrow output pulses, performance tracking from vendor to vendor is particularly poor, with a highly undesirable broad distribution of data points. A user changing vendors would encounter significant timing performance differences, especially since the plot deals only with deviation from a mean, and does not show worst-case errors. For example, when R_X = 50 kilohms and C_X = 5 pF, supposedly identical devices from vendor 6 and vendor 12 can generate pulses ranging from 237 to 732 ns in width.

Published timing data

The expected output pulse width of the widely used 9601 type of monostable multivibrator is easily determined from its data sheet. Generally, how the unit's timing is computed depends on the value of timing capacitance C_X. When C_X is greater than 1,000 picofarads, output pulse width can be computed:

$$T = 0.32R_XC_X(1 + 0.7/R_X)$$

where T is in nanoseconds, timing resistance R_X in kilohms, and C_X in picofarads. For C_X values of less than 1,000 pF, manufacturer's timing curves, like those shown, must be used.



A singular advantage to testing pulse width is the ability to select those vendors whose products fall within the desired tolerance of ±10% over the full timing range. One-shot timing should be monitored for all pulse widths of interest by using permissible combinations of R_X, between 5 and 50 kilohms, and C_X, up to 1,000 pF.

As this study decidedly points out, in-spec performance at one pulse width does not imply across-the-board in-spec performance. One vendor's products, for instance, exhibited unorthodox characteristics even though the one-shots passed the standard 3.4-μs ±10% pulse width test for R_X = 10 kilohms and C_X = 1,000 pF. Some devices displayed a variation of ±40% around a 68-ns mean pulse width, while others could not generate pulses wider than 3.5 μs under any conditions.

Once the vendors whose products track together are selected, additional testing should still be done for absolute certainty of timing performance. To virtually eliminate any excessively inaccurate one-shots, the tests should fix the allowable ±10% timing tolerance as the 3s limit of a Gaussian distribution of test results. Based on the graph of Fig. 2, the recommended pulse widths and timing networks are: 85 ns ±10%, 5 kilohms and 5 pF; 380 ns ±10%, 50 kilohms and 5 pF; 3.4 μs ±10%, 10 kilohms and 1,000 pF; and 17 μs ±10%, 50 kilohms and 1,000 pF. □

Active resonators save steps in designing active filters

Resonator model allows active filter sections to be treated as common components, side-stepping design details that bog down analysis; the model employs a simulated inductance that remains inherently lossless

by Randy Brandt, *Integrated Electronics Inc., Los Gatos, Calif.*

☐ Active filters make possible the realization of inexpensive high-Q networks at low frequencies. Passive filters, on the other hand, tend to become costly, lossy, and unwieldy in physical size when large inductances are required. Since active filters simulate inductance, extremely large values can be realized while holding down filter cost, losses, and size. Furthermore, the ever-decreasing price of today's monolithic operational amplifier, the heart of any active filter, is constantly improving the attractiveness of building an active, rather than passive, filter.

However, because of the proliferation of active filter analysis techniques, only a core of full-time design specialists can differentiate between the merits of various approaches and select the optimum solution. The occasional filter designer finds it easier to build a passive circuit, despite the advantages of the active approach.

But a basic building block, called the active resonator, allows even the occasional filter designer to handle an active filter as an ordinary circuit component. This active resonator model is common to all active filter sections. It consists of a tuned RLC circuit for resonance and an op amp for the necessary gain and isolation.

Modeling the active resonator

An active filter section, regardless of how many amplifiers it contains, is the fundamental repetitive portion of a complete active filter. Generally, the active filter section can perform as a filter itself or be cascaded to realize higher-order filter functions. The term "active resonator" is simply another label for active filter section. With varying degrees of difficulty, any active filter can be reduced to active resonator form.

Because of its utility and simplicity, a sound choice for demonstrating how to form an active resonator model is the popular biquad active filter. This filter is particularly noted for its insensitivity to variations in component values. When it has three amplifiers, as shown in Fig. 1(a), the biquad filter provides both low-pass and bandpass outputs. By adding a fourth summing amplifier, the circuit can supply a high-pass, all-pass, or notch output.[1]

The network's transfer function between its bandpass output, $(V_o)_{BP}$, and its low-pass output, $(V_o)_{LP}$, is that of a non-inverting integrator:

$$(V_o)_{LP}/(V_o)_{BP} = 1/sR'C'$$

where s is the Laplace variable. Feedback current is:

$$i_f = (V_o)_{LP}/R_f = (V_o)_{BP}/sR'R_fC'$$

Solving for the equivalent impedance of the loop with these two equations gives:

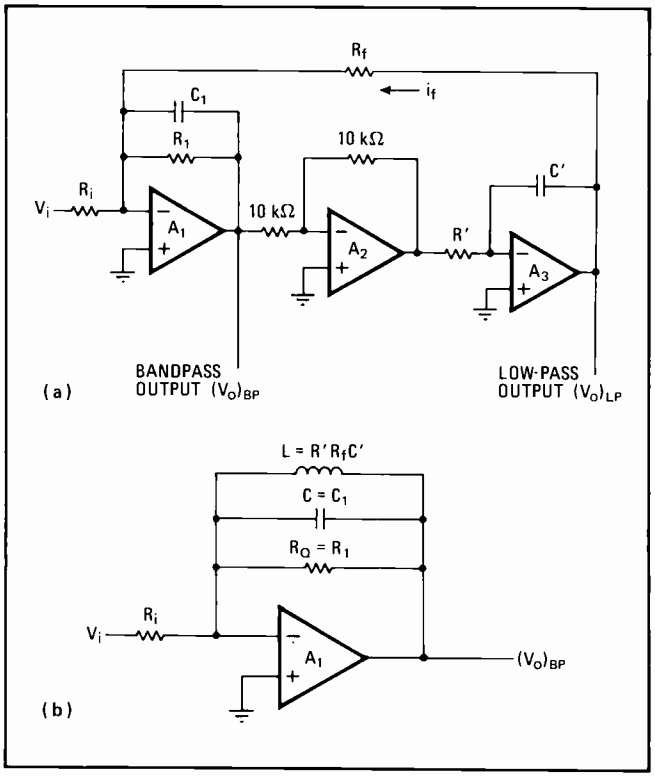
$$Z_L = (V_o)_{BP}/i_f = sR'R_fC'$$

showing Z_L to be inductive in nature. Therefore, amplifiers A_2 and A_3, and feedback resistor R_f can be replAced with the equivalent inductance:

$$L = R'R_fC' \qquad (1)$$

connected in a negative feedback loop around amplifer A_1. Now the general form of the active resonator can be drawn as depicted in Fig. 1(b).

Identifying equivalent inductance L is the key to deriving the active resonator model. Once L is defined in terms of existing components in an active filter section,



1. Resonator model. Biquad filter section (a) can be reduced to active resonator model (b) by replacing amplifiers A_2 and A_3 with equivalent inductance L. This simulates L with non-inverting integrator in negative feedback loop, but other techniques can be used. Very high but lossless inductances can be realized. Single-amplifier resonator can be treated as complete filter section.

the active resonator model can be used to represent that particular active filter section.

Since L is known for the three-amplifier biquad network, it can be handled as a single-amplifier circuit. This reduces analysis complexity and allows the designer to concentrate on his over-all filter requirements without being unduly concerned with the details of each filter section.

For the biquad filter, inductance L may be simulated in several ways by using different non-inverting integrators in a negative feedback loop around an operational amplifier.[2] Of course, any other technique for simulating a stable inductance is also suitable for the biquad network or whatever filter section is being modeled as an active resonator.

Because L is simulated, its inductance can be very large and yet remain absolutely lossless if ideal amplifiers are used. Although ideal operational amplifiers are fictitious, practical op amps can approach the ideal so that inductance L stays virtually pure (lossless). This is true whenever resistance into the summing junction is an order of magnitude less than the amplifier open-loop input impedance, and when the gain of the feedback loop is high enough to prevent open-loop rolloff from affecting desired Q.

Therefore, assuming that loop gain and amplifier input impedance are sufficiently large, the only lossy element in the network is the parallel resistor, R_Q. It can be regarded as the Q-setting resistor, even though the product of R_QC really determines the 3-decibel bandwidth, and both the R_QC and the LC products establish the Q of the active resonator.

Matching the transfer function

The transfer function of the resonator's tuned circuit must be identical to that of its passive counterpart. For the entire resonator of Fig. 1(b):

$$V_o/V_i = s/R_iC(s^2 + s/R_QC + 1/LC)$$

Analyzing this function in the complex s-plane yields the graph of Fig. 2(a). The location of the complex-conjugate pair of poles is determined by the roots of the denominator, while the positions of two transmission zeros (roots of the numerator) are fixed at frequencies of zero and infinity.

This means that the logarithmic magnitude response has a bandpass characteristic with a shape as illustrated in Fig. 2(b). The slope of each curve in the vicinity of resonant frequency f_o is a function of Q. The slope away from resonance is eventually 6 dB per octave because of the zeros that are located at zero and infinity.

The transfer function of a passive parallel RLC network can be written as:

$$G(s) = hs/(s^2 + \Delta\omega s + \omega_o^2)$$

where h is the attenuation factor of the network, and $\Delta\omega = \omega_o/Q$. Comparing the coefficients of G(s) to the coefficients of V_o/V_i for the active resonator yields:

$$\omega_o = 1/(LC)^{1/2} \quad (2)$$

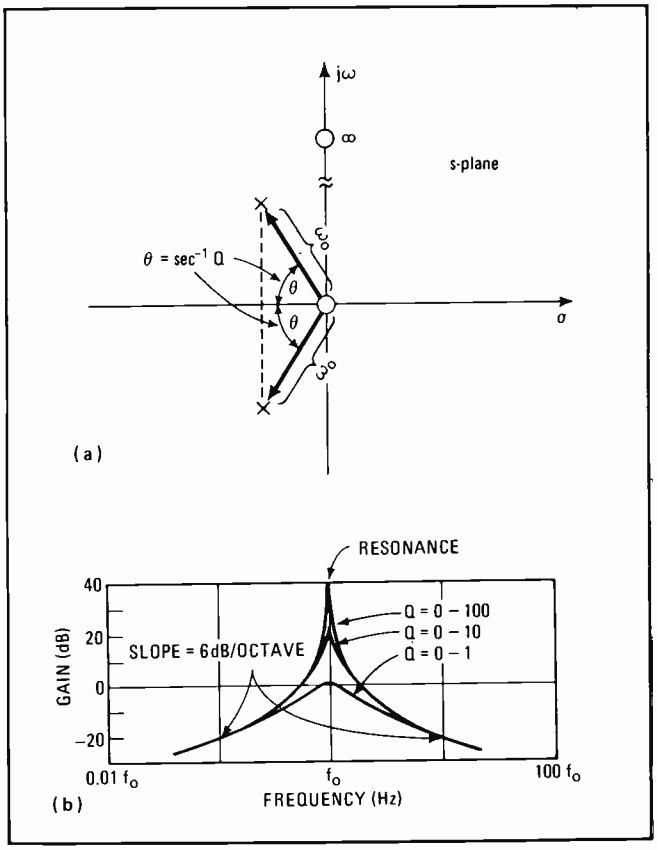
and:

$$\Delta\omega = 1/R_QC \text{ or } Q = \omega_o R_Q C \quad (3)$$

and:

$$h = 1/R_iC$$

The magnitude response of G(s) reaches a maximum at $\omega = \omega_o$, and the 3-dB bandwidth is determined by the



2. Resonator response. Characteristic behavior of active resonator is identical to that of tuned RLC circuit. Pole-zero plot (a) illustrates bandpass nature of resonator transfer function—there are two complex-conjugate poles and two zeros. Magnitude of pole vector is fixed by radian center frequency ω_o, while vector direction is function of Q. Slope of resonator magnitude response (b) depends on Q near resonance and then becomes a constant value.

$\Delta\omega$ coefficient of s in the denominator. At $\omega = \omega_o$, response magnitude becomes:

$$A(\omega_o) = h/\Delta\omega$$

For the active resonator, the response magnitude at ω_o is found by substituting $h = 1/R_iC$ and $\Delta\omega = 1/R_QC$ in this last equation. Then:

$$A(\omega_o) = R_Q/R_i \quad (4)$$

Since the impedance, at resonance, of a parallel tuned LC network with lossless inductors is infinite, the closed-loop gain of the active resonator at resonance is simply equal to a resistance ratio. The active resonator, then, has all the properties of a parallel RLC network and can be described in familiar terms once inductance L is identified.

Designing with the resonator

The placement of poles and zeros in the complex-frequency plane fully defines the shape of a filter's response. Furthermore, the locations of these poles and zeros are determined strictly by the Q and ω_o of the transfer function. And since Q and ω_o are known for the active resonator, complete active filter networks can now be designed.

In general, filter design with either active or passive sections is a matter of obtaining the best curve fit over a band of frequencies for a given set of specifications. The designer usually begins by searching through tables or

Bandpass transformations

The appropriate low-pass approximation function for transforming to a second-order bandpass function has a single pair of complex-conjugate poles in the left-hand s-plane. To transform fourth-order functions, the transformation equations for the second-order functions are used twice.

Transforming each low-pass complex-conjugate pole (a) into its bandpass equivalent requires six parameters: the over-all Q of the bandpass filter at its center frequency (Q_c), the bandpass center frequency (f_o), and the real and imaginary parts of the two low-pass poles.

Since the vectors drawn from the origin to the poles in (a) are defined in terms of Q and f_o, it is convenient to write the transforms with Q and f_o as dependent variables. As shown in (b), the low-pass complex-conjugate pole pair transforms into the bandpass plane as two pairs of complex-conjugate poles and two pairs of zeros.

The bandpass pole Qs are identical, and the center frequencies are geometrically symmetrical about the center frequency of the over-all filter. The zero pairs are located at $\omega = 0$ and $\omega = \infty$, thereby establishing the bandpass character. Further, for each pair of complex-conjugate poles and each pair of zeros, there is a filter section with Q and f_o given by the Q and f_o of the transformed pole pair.

The bandpass Q transformation for a low-pass complex-conjugate pole pair can be written as:

$$Q_p = \left[\frac{4 + ry + (r^2y^2 + 8ry - 16y + 16)^{1/2}}{8y}\right]^{1/2}$$

Here, y is defined as:

$y = (Re/Q_c)^2$

where Re is the real part of the low-pass pole pair, and Q_c is the cutoff-frequency Q. And r is defined as:

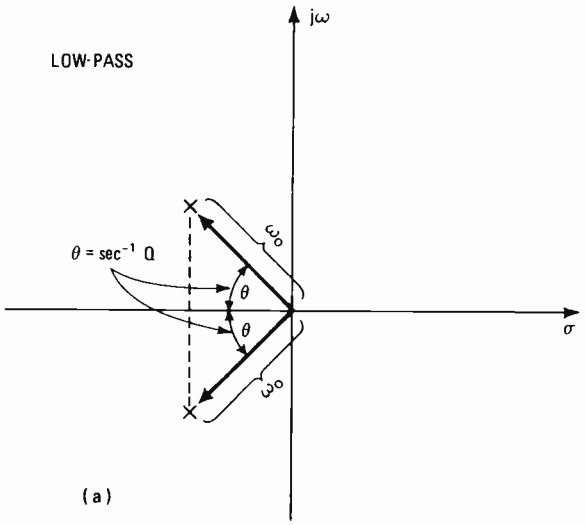
$r = 1 + (Im/Re)^2$

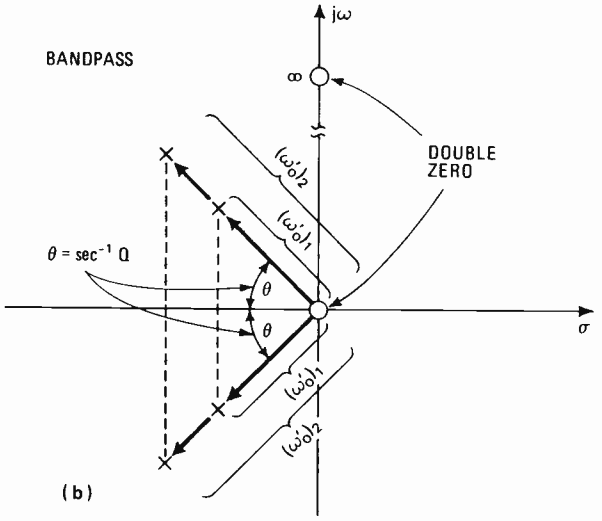
where Im is the imaginary part of the low-pass pole pair. The f_o transformation is:

$(f_o')_1 = [Q_p y^{1/2} + (Q_p^2 y - 1)^{1/2}]f_o$

$(f_o')_2 = f_o/[Q_p y^{1/2} + (Q_p^2 y - 1)^{1/2}]$

where $(f_o')_1$ and $(f_o')_2$ are the resonant frequencies of the bandpass filter sections, and f_o is the resonant frequency of the low-pass filter.





by using a computer program to find the mathematical function that most closely approximates his requirements. In doing so, he may select any one or a combination of such well-known functions as Butterworth, Chebyshev, or Bessel.

Once the function or functions are chosen, the designer decides on the order of the filter, based on characteristics such as shape, minimum stopband attenuation, maximum passband ripple, group delay, and phase response. The order of a filter function fixes the number of sections needed for a given response. And the coefficients of the filter's characteristic equation determine how each section is to be tuned for Q and f_o.

As an example, a typical fourth-order bandpass filter—the type frequently used in low-speed telephone data communications systems—illustrates designing with the active resonator. Suppose the specifications are: a center frequency (f_o) of 2,125 hertz, an over-all passband gain [$A(\omega_o)$] of 200 (46 dB), a 3-dB bandwidth (Δf_3) of 400 Hz, a minimum stopband attenuation (A_{min}) of 60 dB at a lower cutoff frequency (f_L) of 1,270 Hz, a maximum passband ripple (A_{max}) of 0.1 dB, and geometrical symmetry.

First, the filter type and function order that best fit the specifications must be found. To do this, the bandwidth at -60 dB (Δf_{60}) is computed from the upper (f_U) and lower (f_L) frequencies about geometric mean f_o:

$f_U = f_o^2/f_L = (2{,}125)^2/1{,}270 = 3{,}560$ Hz

Then, for this case:

$\Delta f_{60} = f_U - f_L = 3{,}560 - 1{,}270 = 2{,}290$ Hz

And the center-frequency Q (Q_c) of the entire filter is:

$Q_c = f_o/\Delta f_3 = 2{,}125/400 = 5.32$

Shape factor Ω_s is determined next:

$\Omega_s = \Delta f_{60}/\Delta f_3 = 2{,}290/400 = 5.13$

The design step that follows often involves the transformation of a normalized filter function into the proper filtering plane. After transforming and denormalizing this function, the designer can tune each resonator to a particular Q and cutoff frequency. Tables of transfer functions are usually written for low-pass functions so that realizing other filter types requires transforming the low-pass function into the desired function.

Using the computed value of Ω_s, and specified values of A_{min} and A_{max}, and published filter data[3] shows that a fourth-order Chebyshev filter will satisfy the example's skirt, bandwidth, and ripple requirements. The normalized coefficients of the low-pass Chebyshev function are found in a table of low-pass Chebyshev polynominals.[4] For a ripple of 0.1 dB and an order of four, the filter's characteristic equation is given as:

$D(s) = (s^2+0.458s+1.153)(s^2+1.616s+0.789)$

Solving for the roots of D(s) yields:

$s_{A1,A2} = -0.229 \pm 1.05j$, $s_{B1,B2} = -0.808 \pm 0.369j$

These low-pass roots contain two complex-conjugate pole pairs, which transform (see panel, "Bandpass transformations") into bandpass equivalents of four complex-conjugate pole pairs and eight zeros. Since there are four pairs of poles, four active resonators are needed to attain the requirements.

Finding resonator components

From the low-pass-to-bandpass transform equations in the panel, the values of Q and f_o can be computed for each resonator in the bandpass filter. Low-pass roots s_{A1} and s_{A2} characterize the first two resonators:

$Q_1 = 23.3, (f_o)_1 = 2{,}350$ Hz

$Q_2 = 23.3, (f_o)_2 = 1{,}925$ Hz

while s_{B1} and s_{B2} characterize the last two resonators:

$Q_3 = 6.6, (f_o)_3 = 2{,}135$ Hz

$Q_4 = 6.6, (f_o)_4 = 2{,}120$ Hz

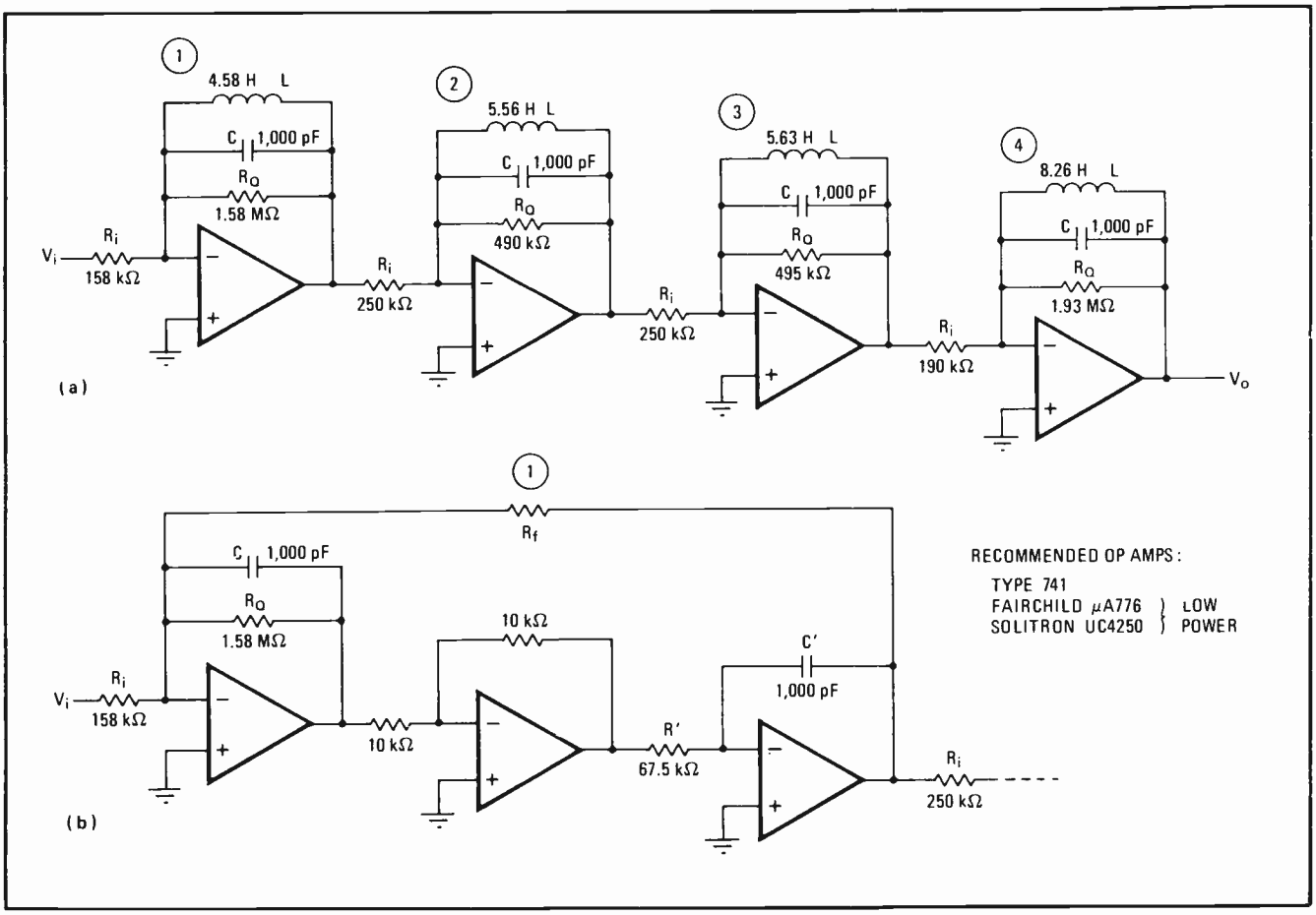
Off-the-shelf resonators

Packaged active resonators, available as standard product lines from more than a dozen companies, can almost reduce active filter design to a matter of resistor selection. Some manufacturers refer to their lines of active resonators as universal active filters, but the circuit function is the same.

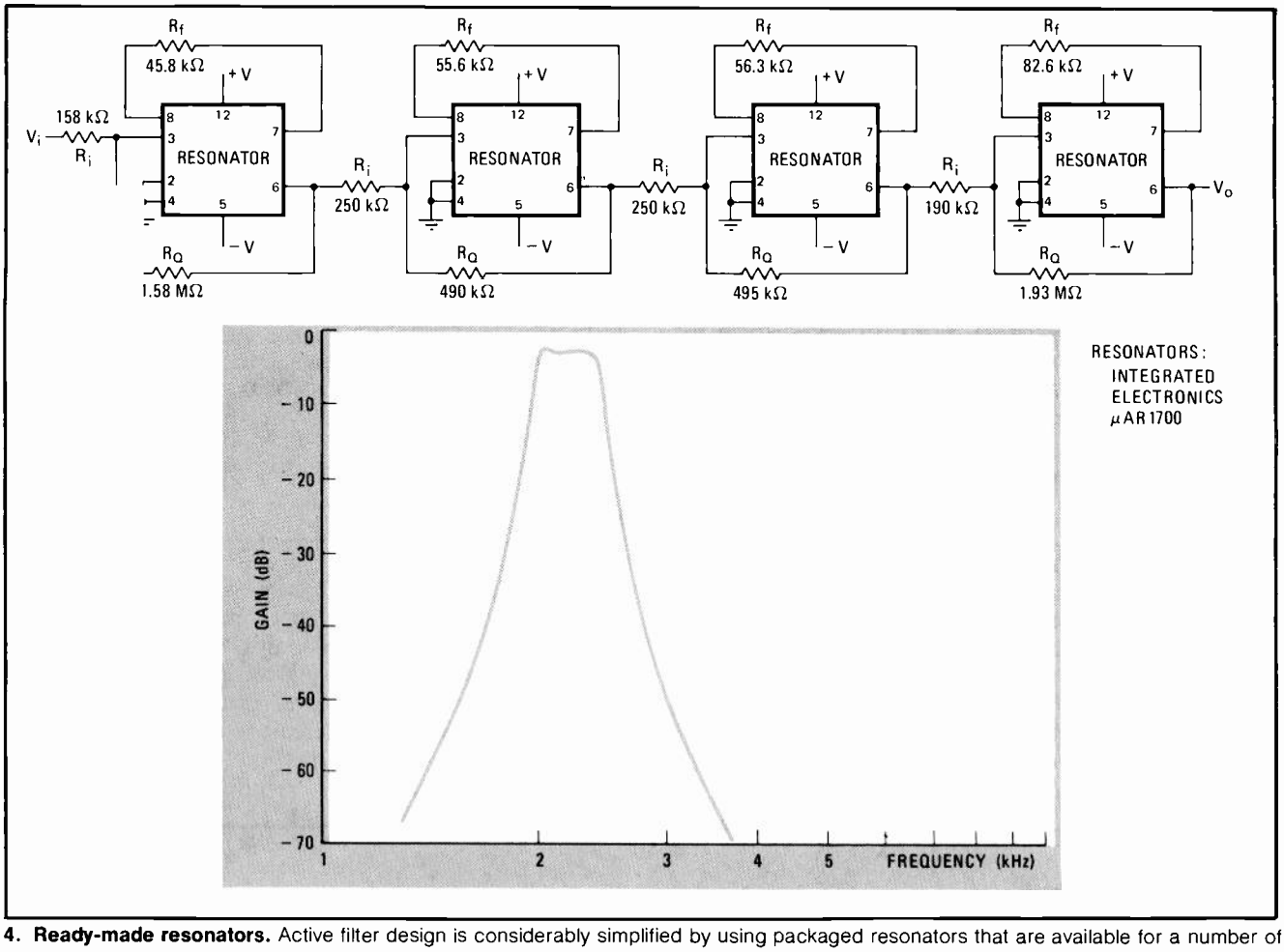
The larger suppliers include Beckman Instruments Inc., Fullerton, Calif.; Datel Systems Inc., Canton, Mass.; Kinetic Technology Inc., Santa Clara, Calif.; Optical Electronics Inc., Tucson, Ariz.; and TRW Semiconductor division, Lawndale, Calif.

A standard family of hybrid microcircuit active resonators also is offered by Integrated Electronics Inc., principally for use in audio and subaudio applications. In large quantities, they range in price from about $5 to $8.

Figure 3(a) shows the bandpass filter configuration using the active resonator representation. It should be remembered that the resonator model employs an equivalent inductance requiring practical simulation and that each resonator section actually consists of three amplifiers and associated circuitry, as noted in Fig. 3(b) for the input resonator. Once the components for the resonators are known, those required to complete each



3. From model to design. Fourth-order bandpass filter (a) is represented by four cascaded resonators. Each resonator, with its simulated inductance, actually requires three amplifiers (b), making 12 op amps necessary for entire filter. Component values can be found, once Q and f_o are known for each resonator. Capacitor values are assigned for computation convenience. R_Q principally determines Q of resonator.



4. Ready-made resonators. Active filter design is considerably simplified by using packaged resonators that are available for a number of filtering functions. Those in this diagram are biquad networks connected to realize bandpass filter of Fig. 3. Only three components must be added to each package—R_i for gain adjustment, R_Q to fix resonator Q, and R_f to set resonant frequency.

filter section can be found.

To keep the analysis simple (neglecting the input impedance of practical operational amplifiers), a convenient value is chosen for capacitor C. Generally, C should vary between 800 and 1,000 picofarads for resistor values to remain reasonable. By letting C = 1,000 pF and computing the radian center frequency ($\omega_o = 2\pi f_o$) for each resonator, L can be found from Eq. 2:

$$L = 1/\omega_o^2 C$$

The value of resistor R_Q is determined with Eq. 3:

$$R_Q = Q/\omega_o C$$

Since there are four resonators and the over-all required gain is 200, then each resonator must provide a gain of 50. Eq. 4 becomes:

$$A(\omega_o) = R_Q/R_i = 50$$

which can be solved for input resistor R_i:

$$R_i = R_Q/50$$

After the component values for the four resonators are computed, the other components needed to simulate inductance L can be found. Again, the value of 1,000 pF is chosen for capacitor C′ to simplify the calculations. Feedback resistor R_f is set equal to resistor R′:

$$R_f = R' = R$$

so that Eq. 1 can be used to find R:

$$R = (L/C')^{1/2}$$

Active resonators, however, are available as standard products from several manufacturers, as noted in the panel, "Off-the-shelf resonators." These packaged circuits often reduce the final design step to choosing resistor values, once Q and f_o are known.

For instance, the μAR 1700 resonator from Integrated Electronics is a biquad network that can be used for the resonator sections in the fourth-order bandpass filter design example. Components C, L, R_Q, and R_i are computed as before; of these, only R_Q are R_i are required for the actual filter implementation, as indicated in Fig. 4. None of these component values differ from those already calculated.

Next, the "internal" resonator parts are found. In addition to setting C′ = 1,000 pF, R′ is assigned a value of 100 kilohms for convenience, and then R_f is computed from Eq. 1:

$$R_f = L/R'C'$$

The resulting values of R_f are noted in the figure. When the μAR 1700 resonator is used to build an active filter, R_Q effectively sets resonator Q, and R_f effectively sets resonator f_o. The magnitude response of the fourth-order bandpass filter is also illustrated. □

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Active filters get more of the action

Built around the new, better, cheaper IC op amps, active filters are beginning to move in on passive filters; their advantages include flat passbands with sharp corners, inherent isolation, and easy tuning

by Lucinda Mattera, *Circuit Design Editor*

☐ For all practical purposes, an active filter is just an RC network tacked on to an operational amplifier—or amplifiers—and its price and performance depend essentially on those of the op amp. Recently IC op amps have improved so much on both counts that active filters have started challenging passive filters at the lower end of the frequency spectrum. In fact, the very lowest end is by now all theirs.

A great many are being built in-house. They are relatively straightforward to design, because they can be easily handled in mathematical terms and lend themselves to computer-aided design. But with the manufacturers of active filters busily cutting prices and introducing standard products that can be customized by the buyer, the make-or-buy decision is becoming more difficult than it was a year ago.

Presently, communications applications in telephone equipment and various military programs are making heaviest use of active filters. They are also being exploited in some areas of data acquisition, notably telemetry, medical research, oceanography and the monitoring of geophysical phenomena. But much larger and practically untapped markets exist in process control, data acquisition, computer terminals, and modems. Other potential markets include pager systems, petrochemistry, and instrumentation.

From this listing, it's clear that active filters perform the same functions as passive filters, providing either low-pass, high-pass, bandpass or band-reject (notch) outputs. Their response characteristics are also identical, since they can realize a Butterworth, Chebyshev, Bessel, Gaussian or Cauer (elliptic) response. As a result, deciding which type of filter will do the better job boils down to the traditional design tradeoff between cost and performance.

Two frequency breakpoints—100 hertz and 20 kilohertz—can be used as soft guidelines for the decision. Active filters should be considered only if they are to operate at very low frequencies or in the audio region—say, from 0.001 Hz to 20 kHz. Above 20 kHz, the passive filter costs less than the active and provides comparable or better performance. Below 100 Hz, passive performance is quite sloppy, so that the active filter is the more practical choice almost regardless of cost. From 100 Hz to 20 kHz, however, the active filter's cost does not really change, while the passive filter's steadily drops, making the performance the deciding factor in this region.

Over the audio range and below, the active filter has a flat constant-amplitude passband and sharp corner frequencies. Moreover, even when operating at frequencies below 10 Hz, it provides reasonably high values of Q, allowing good selectivity to be obtained. In contrast, the vlf passive filter requires very high inductance values so that the inductors are physically large and cannot provide the Q needed for good selectivity.

Above 20 kHz, the op amp is the limiting factor. Its gain-bandwidth product determines the highest frequencies at which the filter can work. The output power level of most low-cost general-purpose IC op amps begins to roll off at about 20 kHz, attenuating the filter output voltage. But op amps with gain-bandwidth products large enough to sustain filter operation above 20 kHz are expensive, costing $5–$10 instead of $1.

Comparing active and passive

In general, it's the component parts of the active filter that contribute most to its cost—the IC op amps cost nearly a dollar each, whereas resistors and capacitors get only a few cents apiece. With the passive filter, on the other hand, the design time needed to produce desired performance is the expensive element.

This can be inferred from a comparison of active versus passive performance:

- The behavior of practical inductors is very nonlinear at low frequencies, especially with respect to temperature coefficient. But because even low-cost general-purpose op amps offer dependable temperature performance, the active filter can achieve a corner frequency as tight as 100 parts per million per °C without too much difficulty.
- Obtaining a frequency accuracy within only 5% can be troublesome with the passive filter, but is easy with the active.
- Getting sharp corner frequencies, which are inherent in the active filter, requires many inductors and capacitors in the passive-filter. This makes the passive bigger than the active for the same skirt selectivity.
- The active filter can supply a controlled gain over its entire operating frequency range. The passive filter always attenuates a signal.

■ Additionally, the active filter is easily tuned to the desired operating frequency with a resistor, while the passive must be tuned with an inductor and/or capacitor.
■ Impedance matching at either the active filter's input or its output is unnecessary because its op amp provides it with inherent isolation in the form of a high input impedance and a low output impedance. For the passive filter, impedance matching can prolong design time inordinately, and proper termination may even involve active devices (an emitter-follower or an op amp) at each end.
■ Realizing higher-order filter functions is a simple matter of cascading active-filter sections, each of which provides at least a second-order filter function. This is a marked improvement on implementing higher-order functions with the passive filter, which requires the addition of inductors and capacitors that make the design more complex and interaction problems more acute.

Mathematically, in fact, the active-filter section can be treated as a second-order transfer function that is synthesized as a pole pair rather than a low-pass or high-pass filter section. This makes the active filter easy to manipulate on paper or to design with the aid of a computer without special complicated programs.

Other cost considerations

Admittedly, the passive filter operates without being tied to a power supply, while the active cannot. Op-amp power supplies are common to so many applications, however, that the addition they make to the price is usually very reasonable.

And even so, there are situations in which active filters are more cost-effective than are passive. Several active filters, for instance, can fit on one printed-circuit board, while at least one board is usually needed for each passive filter. The cost of associated hardware like pc boards, connectors, and cables could be substantial enough to tip the balance toward active filters.

Moreover, active filters often help lower production costs. When housed in small IC-compatible packages they can save assembly time, and are adaptable to existing automatic production machinery, like insertion and wire-wrapping equipment.

Today's practical active filter is one that uses an active device to synthesize inductance. There are four basic types.

Data acquisition: promising

Although computer-controlled data acquisition systems are popular, only a few contain analog-to-digital converters that use filters to precondition incoming analog signals for improved data analysis accuracy. The filters that are used, however, are generally active, since much of the data being collected occurs at frequencies of 20 hertz or below.

Only rather specialized data gathering systems—for example, systems for special automobile testing, offshore drilling operations, and checking bridge construction—presently employ filters. For the most part, process control, where a good deal of data acquisition is done in the noisy environment of industrial machinery, remains a holdout against filtering.

Manufacturers selling data acquisition systems with prefiltering include: Digital Equipment Corp., Maynard, Mass.; Data General Corp., Southboro, Mass.; and Analogic Corp., Wakefield, Mass. Another company, Datel Systems Inc., Canton, Mass., will be introducing a prefiltered multiplexing system at the Wescon show.

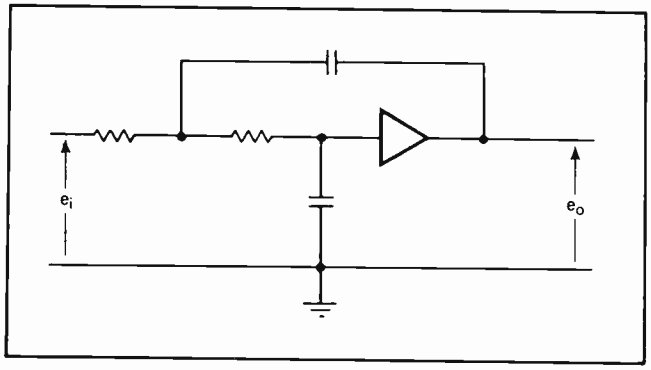
The least used—the positive-feedback filter (Fig. 1)—is also the only one to employ a noninverting op amp. This filter, which is also known as the voltage-controlled voltage source, usually requires the fewest resistors and capacitors and is easily tunable over a wide frequency range. It is the only practical active filter circuit that offers zero phase shift without needing a second amplifier for signal inversion.

The other three circuits incorporate negative feedback, using the op amp in its inverting mode. For these, the output signal is out of phase with the input by 180°. Common names for the three are multiple-feedback, state-variable, and biquad active filters.

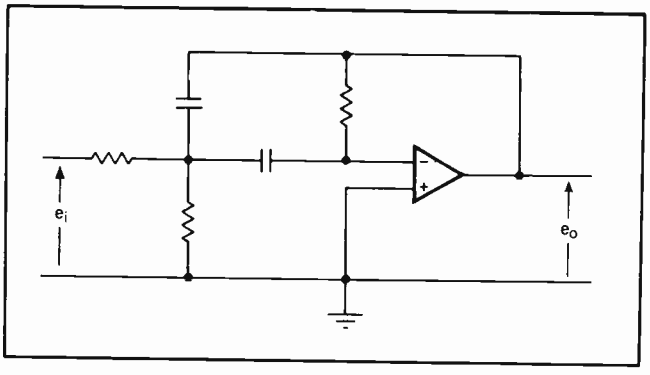
Negative-feedback filters

The multiple-feedback active filter (Fig. 2), which is the most widely used, consists of a single op amp and an associated RC network. As a bandpass filter, it offers constant-gain-and-bandwidth performance that does not change as the filter's center frequency is shifted. Two variations of this filter—the bridged-T and the twin-T active filters— have only one feedback path. But they are less popular than the multiple-feedback ver-

1. Non-inverting. Positive-feedback active filter (low-pass, in this case) maintains zero phase shift between input and output. This least-used filter circuit minimizes component count.



2. Most popular. Multiple-feedback filter has two or more negative-feedback paths. Here a bandpass function is realized. The shifting of center frequency does not affect filter's gain and bandwidth.



sion, because they need more passive components and have higher output impedances.

Both the state-variable (Fig. 3) and biquad (Fig. 4) active filters realize a transfer function through the analog computing technique of integrating and summing. The former is based on general state-variable theory, while the latter is a modified state-variable filter that involves quadratic equations.

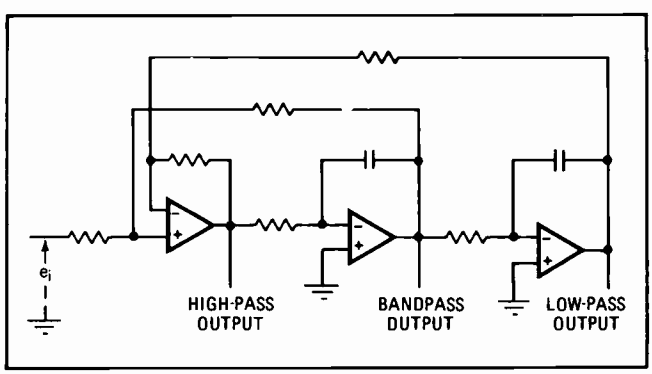
Simultaneous low-pass, high-pass, and bandpass outputs are available from the state-variable filter. The biquad filter provides simultaneous low-pass and bandpass functions, but requires an additional amplifier to realize a high-pass output. This choice of output function is why these circuits are often referred to as universal active filters or active resonators [*Electronics*, "Active resonators save steps in designing active filters," April 24, p.106].

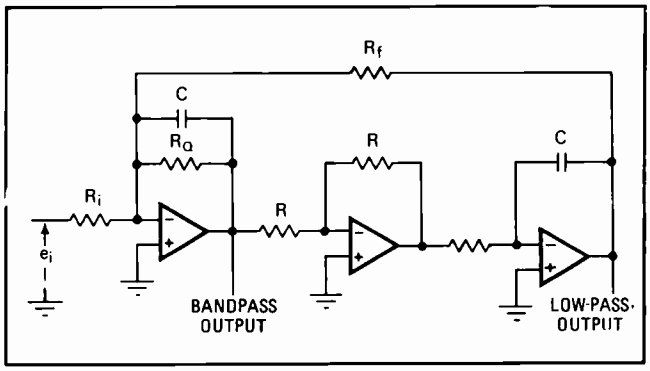
Both these types of filter require two or three op amps each, in addition to the necessary resistors and capacitors, making them rather more expensive than the multiple-feedback filter. In exchange for this higher cost, however, they do offer a choice of output functions and simpler design procedures. Also, they are relatively insensitive to passive-component tolerances. The Q, gain, and operating frequency of the two can be independently adjusted with resistors.

Better temperature stability can be obtained from the state-variable and biquad filters than from the multiple-feedback filter, but op-amp quality must be better; the multiple-feedback filter is not as sensitive to amplifier performance. On the other hand, since the gain-bandwidth product of cascaded amplifiers is smaller than the gain-bandwidth product of a single amplifier, the upper frequency limit of the state-variable and biquad filters tends to be lower than that of the multiple-feedback filter circuit.

As for the relative merits of the biquad and the state-variable filters, the former is usually the better for a low-pass or bandpass function, and the latter better for

3. Versatile. State-variable filter requires three op amps to supply high-pass, low-pass, and bandpass outputs at same time. Operating frequency, gain, and Q are independently adjustable. Also, circuit is not sensitive to passive-component tolerances.





4. Modification. Biquad active filter offers most advantages of state-variable circuit, but cannot produce a high-pass function without additional amplifier. R_i sets gain, R_Q sets Q, and R_f sets frequency.

a high-pass function. But the values of the resistors and capacitors in a biquad may be so high that their temperature coefficients become inadequate. In that case, the state-variable filter is to be preferred, since its performance parameters are set by component ratios and it can make use of low resistor and capacitor values, with their better temperature coefficients. For example, the Q of the state-variable is determined by a resistance ratio, not a single resistor value as with the biquad.

Deciding to make or buy

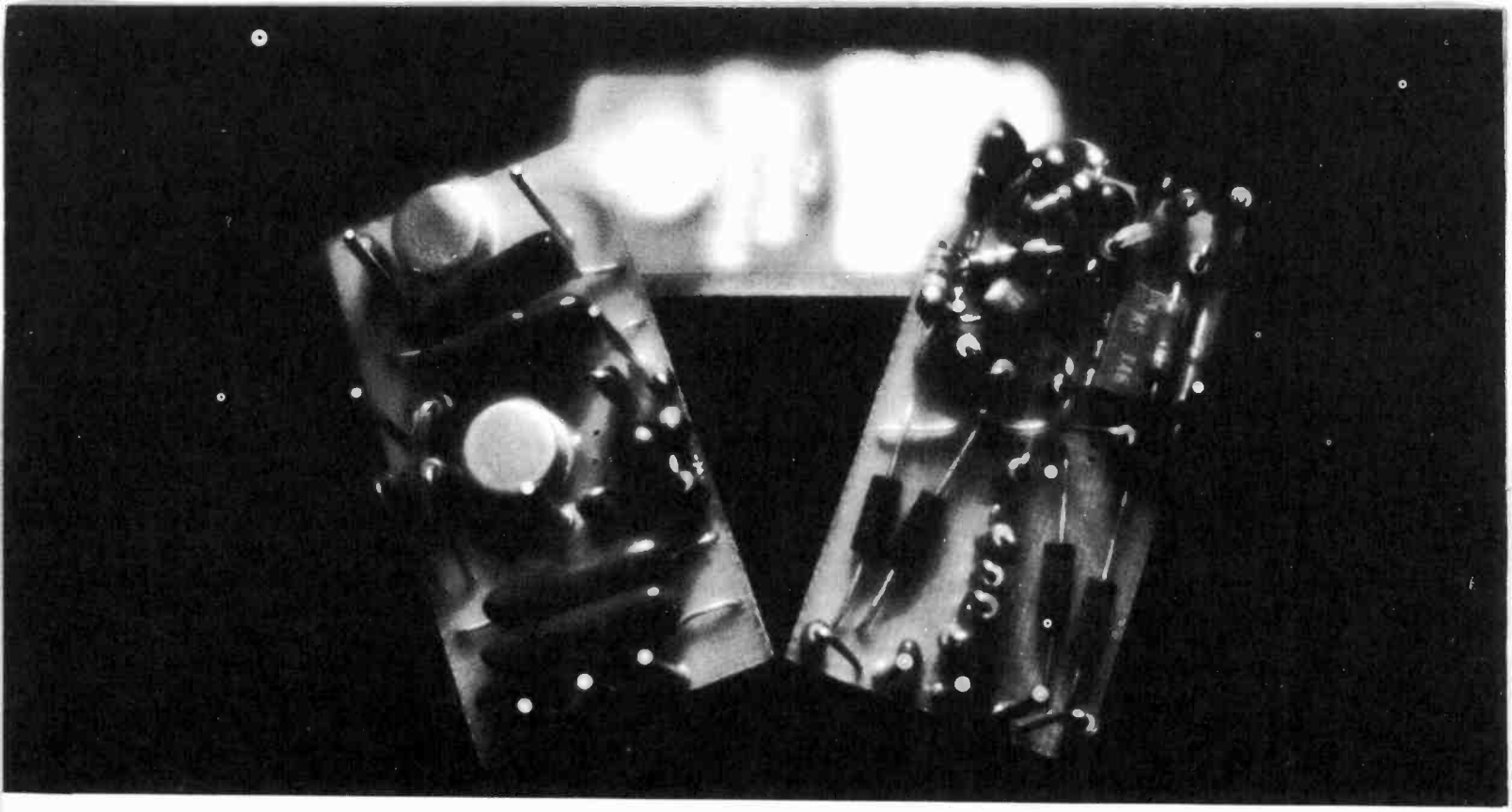
As a rule, active-filter users build their own circuits if they have the necessary design experience, and if they use filters in large quantities. Active filter suppliers find their main customers are among those users who lack design know-how, or who have particularly stringent performance requirements.

In contrast to the ones built in-house on pc boards, purchased active filters are always plug-in modules that are housed in IC-compatible packages. These ready-made units are either modular encapsulated assemblies (Fig. 5) of packaged discrete-type components or precision hybrid circuits (Fig. 6) that contain chip amplifiers, chip and/or discrete capacitors, and thick-film and/or thin-film resistors. They are usually negative-feedback filter circuits of the three types discussed above, and can range in price from about $26 for a single standard unit to a few hundred dollars for a single special unit.

Only about four years ago, the market for active filters seemed to have a bright future. But many potentially large markets have remained relatively unpenetrated because of widespread in-house design, the firm establishment of passive filters, and the lack of filtering in many data gathering applications. Nevertheless, active filter sales are expected to be close to $10 million for 1972, climbing to $19 million by 1975.

While the current market is growing at the rate of 10% to 15% per year, usage of active filters is probably growing much faster since many more filters seem to be being built in-house than are being sold by filter manufacturers. To attract more sales, some filter suppliers are hoping to launch the same kind of customer-education campaign that was extremely successful for the op amp. That goal should be helped along by the declining prices of recent and upcoming new filter products.

Because most filters are custom items, their manufacturer is primarily in the business of selling engineering



5. Off-the-shelf. Modular-type filters manufactured by Frequency Devices are assembled from discrete amplifiers, resistors, and capacitors. Several vendors supply similar filters in both standard and custom models, as either factory-tuned or customer-tuned circuits.

services. Filter makers who do supply standard filters attribute only about 30% of their sales to them.

Several companies are offering the universal active filter as a standard product, but its reception has been mixed. Some users say that its principal feature, its variability, is useless since filter needs are usually specialized. The filter's data sheet is said to be difficult to understand, and tuning it to desired specifications may not be easy. Tuning can be further complicated when several of the devices are cascaded, because their tuned component values generally differ from resonator to resonator. Finally, the universal filter is expensive because it contains more than one op amp.

However, as one supplier points out, this filter can be used as a basic building block by the manufacturer to realize a whole line of filters, without harming the filter's tuning versatility. The manufacturer can choose the filter function he wants and then encapsulate. Eventually, therefore, the universal filter will cost the manufacturer less to make—and his customer less to buy.

Filter makers stress lower pricing

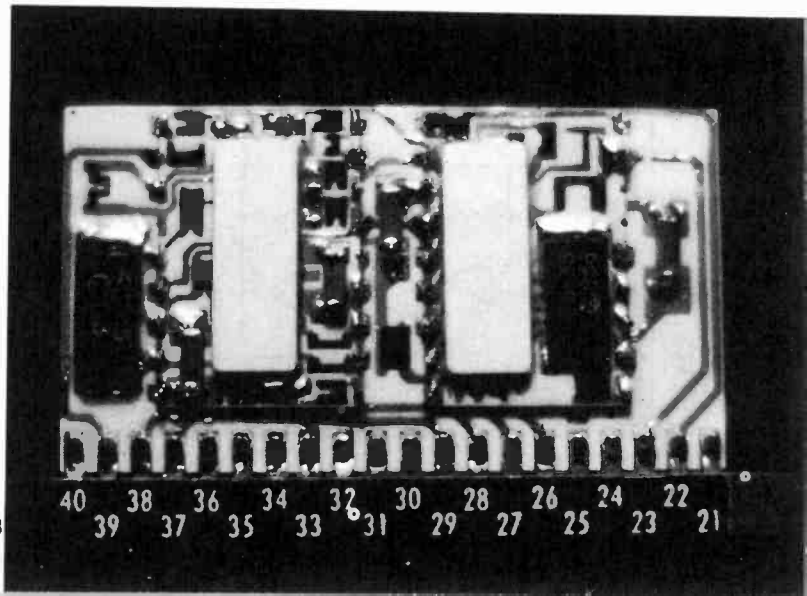
One of the oldest suppliers of modular-type active filters, Burr-Brown Research Corp., Tucson, Ariz., is keenly aware of the need for a low-cost ready-made unit. This month, the company is introducing its series ATF76 filters that are about half as expensive as its earlier units and are intended to be priced about 10% below competing lines. The new filters are fixed-tuned units that employ IC op amps instead of discrete transistors. Single-unit prices begin at $29 for a two-pole lowpass Butterworth filter.

Ron Gadway, product marketing engineer, data conversion products, sums up the filter maker's biggest problem, "Our competition is really the customer himself. If we can't give him what he wants for his price, he'll build it himself." Burr-Brown expects to expand its standard line with a state-variable filter before the end of this year, and to add a voltage-tunable filter shortly afterwards.

Another manufacturer of modular-type filters is Frequency Devices Inc. of Haverhill, Mass. This small company has an interesting way of keeping parts cost low. Alan Schutz, director of engineering, explains, "We buy capacitors with tolerances of ±20%, but know their actual values to within ±0.5%. Resistor values are then easy to determine with a simple computer program."

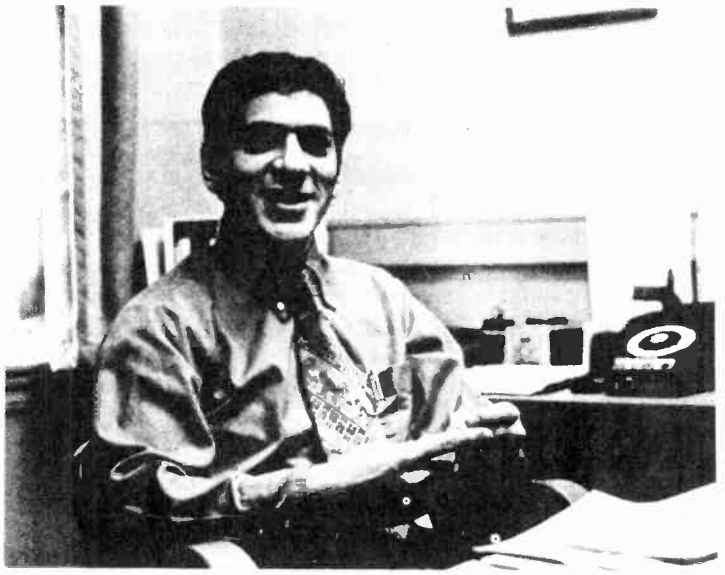
A recently introduced family of tunable active filters

6. Chips and films. Hybrid active filters tend to be customized circuits of thick- and thin-film resistors, chip capacitors, and chip amplifiers. Pictured is digitally tunable bandpass filter made by Sprague Electric for the military. Molded tantalum capacitors (on left and right sides) are sometimes used to furnish required capacitance.



7. Module maker. Alan Schutz of Frequency Devices thinks that suppliers must teach customers how to select and use active filters.

8. Hybrid maker. Active filter suppliers must also service other markets to survive, asserts Eugene Donovan, Sprague Electric.



9. Instrument maker. Variable active filters can be used as design aid to find filter needed, observes Ernest Lutfy, Krohn-Hite Corp.

from Frequency Devices frees the customer from the difficult and time-consuming job of capacitor trimming. The capacitors are inside the package, and tuning is accomplished with outboarded resistors. Frequency Devices is one of the few companies with a standard series of voltage-tunable active filters. Tuning ranges for these extend down to 0.01 Hz and up to 50 kHz. Single-unit pricing starts at $2.10.

Manufacturers that make hybrid active filters do so, for the most part, as a byproduct of their other hybrid business. A well-known supplier of hybrid circuits for several years is the Semiconductor division of Sprague Electric Co., in Worcester, Mass. Eugene Donovan, operations manager, hybrid circuits, points out, "Anybody who depends on filters totally is going to have a difficult time. At Sprague, we build hybrids and can serve several markets with the same technology, because the components used in our converter products can also be used in our filters."

In an attempt to break hybrid filters out of the predominantly custom market, Sprague intends to introduce a second line of standard filters in the next month or so. The filters will be tunable, using external resistors to control Q, frequency and gain. Both bandpass and notch functions will be available for frequencies of 30 Hz to 10 kHz. Pricing is not yet firm.

Motorola Semiconductor, Phoenix, Ariz., is aiming particularly for penetration of the modem area with active hybrid filters. But, observes Don Kessner, manager of systems, industrial applications, "because of cost, the hybrid active filter will probably never replace the pc-board active filter used in those modems where space is not critical." Only when the "so-called all-MOS data modem" becomes practical does he feel that a high-volume special market may develop for the inexpensive hybrid filter. Intended for low-speed operation, this modem would comprise two packaged circuits—a digital MOS chip and an analog front-end conditioner for the chip. The analog portion could be a hybrid filter.

Kinetic Technology of Santa Clara, Calif., which re-

covered from bankruptcy officially this last December, is selling both modular and thick-film hybrid active filters. The company's standard hybrid filters are state-variable circuits that provide a variety of response characteristics, from Butterworth to elliptic. The least expensive filter in this family sells for $26 singly, dropping to less than $5 in quantities over 10,000. It includes an extra op amp.

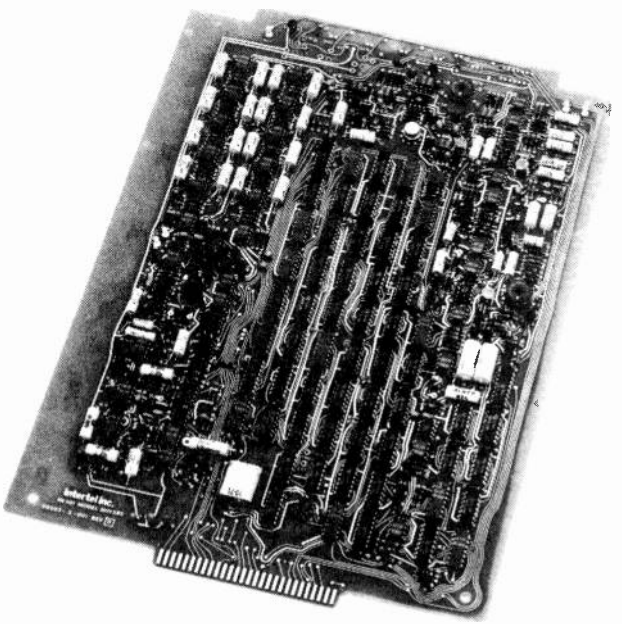
Fred Glynn, Western regional sales manager, offers a bit of customer advice. "If frequency accuracy within 1% is acceptable," he says, "the customer can use inexpensive 1% resistors to tune our filters without difficult trimming. If his accuracy requirement is tighter, we suggest that he use a less expensive filter [of ours] and tune it with a fixed resistor and a trimmer potentiometer."

For completeness' sake, the instrument type of active filter (Fig. 10) should also be mentioned. It can provide a number of filtering functions over a wide frequency range. The user selects the functions he wants (low-pass, high-pass, or a combination of these) and then dials the frequency he wants.

Krohn-Hite Corp., Cambridge, Mass., manufactures a series of these variable active filters. The company's instruments can perform low-pass, high-pass, band-pass and band-reject filtering from 0.001 Hz to 3 MHz. Prices range from $450 to $2,075 for frequency accuracies of ±2% to ±10%.

"Because our instruments are tunable and can be operated over a wide frequency range, they are sometimes used as a design aid to help pinpoint the fixed-frequency filter that will be needed," notes Ernest Lutfy, sales manager. Medical researchers are also using the variable filter, for example, to test the frequency response of the ear, or to listen to the heartbeat of a fetus while filtering out unwanted signals from its expectant mother.

10. Variable active filter. When filter frequency must be continuously varied, an instrument-type filter can be used. Corner frequencies and filter function can be selected from front panel.



11. Tight fit. Intertel Inc. employs narrow-band active filters to eliminate noisy sidebands in receiver portion of pc-board 201-type modem. Complete modem measures only 9.5 by 12.9 inches.

Users justify building in-house

In-house active filter design is done by companies who can spread engineering costs over a number of products. "We seldom buy outside because it's just too expensive," says Farouk Al-Nasser, a principal scientist at the test instrument division of Honeywell Inc., in Denver, Colo., who is involved in designing data storage systems. But he cautions that learning how to design active filters may take as long as two to three years, because existing literature does not cover practical considerations for the op amp. Most filter theory still treats the op amp as an ideal element having infinite gain and perfect isolation.

Many modem manufacturers have a staff of active filter design specialists. One of these is Paradyne Corp. of Clearwater, Fla. "The cost of active filters depends on who designs them," says Tom Saliga, senior engineer. "Using only one op amp, we can build a [multiple-feedback] filter with four to five poles for around $1 to $1.50."

Paradyne even standardizes its active filter designs to some extent to realize additional cost savings. Most of the filters the company incorporates in its modems use the same two values of capacitance, enabling Paradyne to buy capacitors in very large volume.

Specializing in pc-board modems (Fig. 11), Intertel Inc. in Burlington, Mass., uses active filters exclusively to keep its modems as small as possible. "We need very special filters and prefer designing our own," says George Harlem, marketing coordinator. "Nobody else can build them as cheaply as we can, and nothing that we could buy is equivalent in terms of performance."

Many designers actively prefer active filtering to passive. Jerry Holsinger, Intertel president, explains why: "In a sense, passive filter design is a black art. Active filter design is really a totally new concept in which the general-purpose building block is not a physical component, but simply a second-order transfer function." He's referring to the fact that an active filter can be completely described by its pole-zero plot, which always contains a pole pair, permitting the filter to be easily manipulated mathematically.

One designer, John DeFalco, who is a lead engineer at Honeywell Information Systems in Billerica, Mass., personalizes his preference for active filters. "Passive filter design is just a matter of looking up data in tables and charts—it's a lot more fun designing an active filter," he says. □

The integrated Schmitt trigger: a versatile design component

Availability of the Schmitt trigger in an IC version is expanding its use in common circuits, such as multivibrators and pulse stretchers; here are a few design tips on how best to apply it

by John A. DeFalco, *Honeywell Information Systems, Billerica, Mass.*

☐ As basic digital circuits go, the Schmitt trigger requires careful and sometimes time-consuming design. That fact has deterred many circuit and systems designers from working with it, despite its versatility. Recently, however, several manufacturers have introduced an integrated dual Schmitt trigger, the type 7413, which is completely compatible with the popular type 7400 TTL circuits.

To use the type 7413 to its best advantage, the designer should first take an inside look at the chip and see how it operates. That means understanding how to derive the values of the major parameters from the circuit diagram.

The circuit's most important parameters are its positive- and negative-going threshold voltages, V_{T+} and V_{T-}. V_{T+} must be exceeded to switch the output from a high to a low state, while at V_{T-} the output switches from low to high.

These voltages, together with the effects of temperature and power supply variations, can be easily calculated for the chip from the circuit diagram of Fig 1. Each half of the type 7413 Schmitt trigger is actually a combination of 7400-type logic and the basic Schmitt trigger. Logically, the integrated Schmitt functions as a four-input NAND gate; tying all four of the inputs together allows the circuit to be driven by signals with larger amplitudes.

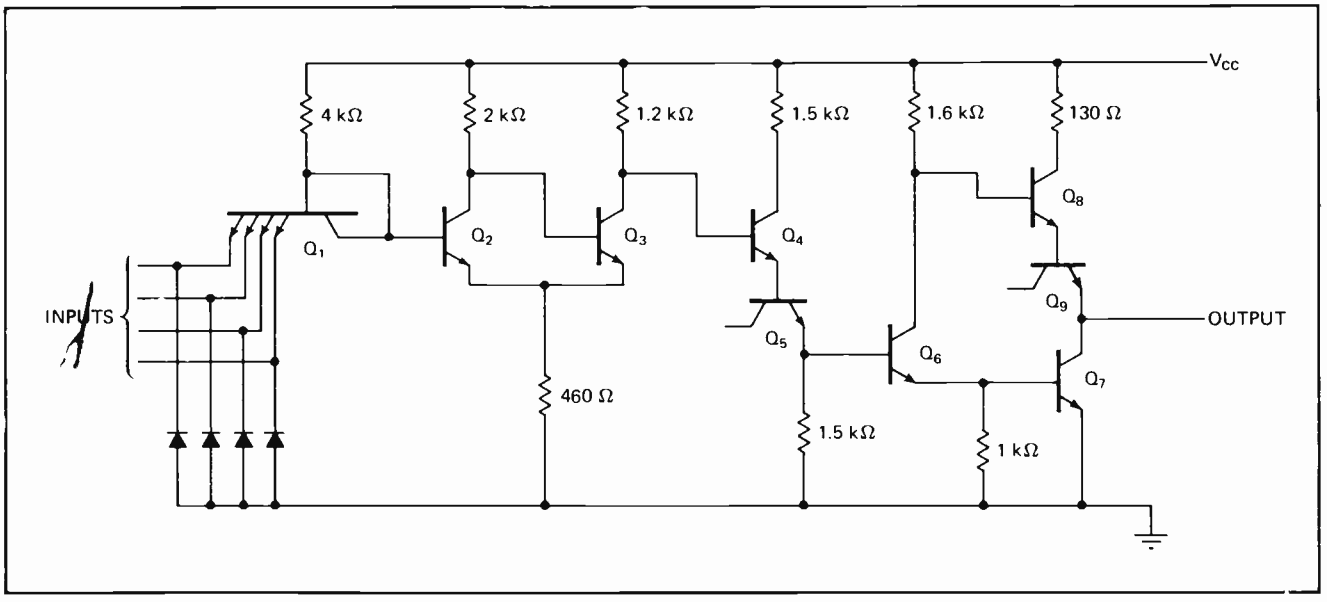
Analyzing the IC Schmitt

Multiple-emitter transistor Q_1 operates as a diode (its collector-base junction is shorted). Transistors Q_2 and Q_3 are the actual Schmitt trigger, while transistors Q_4 through Q_9 make up a NAND gate with conventional TTL-type output characteristics. Two of these transistors, Q_5 and Q_9, function as emitter-base diodes (collector open).

When the input (assuming all four inputs are tied together) is low, Q_2 is off and Q_3 is saturated. To calculate the positive-going threshold voltage, the circuit of Fig. 2a (left) can be used to obtain the Thévenin equivalent (right) with transistor Q_3 in saturation. Summing voltage drops around the input loop,

$$V_{T+} = -V_{BE1} + V_{\gamma 2} + V_E$$

where V_{BE1} is the base-emitter voltage of transistor Q_1 and $V_{\gamma 2}$ is the emitter-base voltage required to turn on transistor Q_2. Voltage V_E from the emitters of Q_2 and



1. Integrated Schmitt circuit. Each Schmitt trigger contained in the type 7413 package functions logically as a four-input NAND gate. Tying all four inputs together maximizes the size of signal that can be accepted. Transistors Q_2 and Q_3 are basic Schmitt; remaining transistors form TTL-type NAND gate. Multiple-emitter transistor Q_1 and transistors Q_5 and Q_9 operate as diodes. Output of Schmitt is TTL-compatible.

Q_3 to ground can be found from the Thévenin equivalent circuit:

$V_E = (460\,\Omega)(4.6\text{ v})/(750\,\Omega + 450\,\Omega) = 1.74$ v

Assuming values of $V_{BE1} = 0.7$ v and $V_{\gamma 2} = 0.55$ v:

$V_{T+} = -0.7\text{ v} + 0.55\text{ v} + 1.74\text{ v} = 1.59$ v

Negative-going threshold V_{T-} can be determined by assuming transistor Q_2 is on and saturated. As the input to the Schmitt trigger drops, transistor Q_3 begins to turn on and the circuit conditions of Fig. 2b apply. When Q_3 turns on, transistor Q_2 is in the active state and its collector voltage is:

$$V_{C2} = V_{CC} - I_{C2}R_{C2} \quad (1)$$

Computing Q_2's collector current:

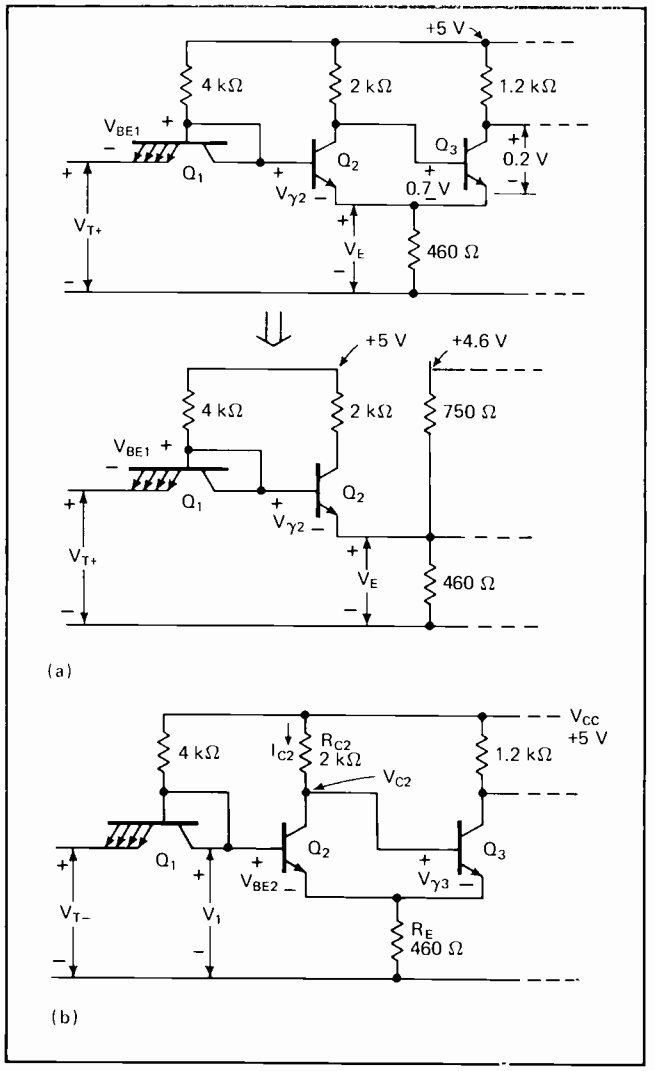
$$I_{C2} = [\alpha_2(V_1 - V_{BE2})]/R_E \quad (2)$$

where α_2 is the common-base current gain of transistor Q_2. Substituting Eq. 2 into Eq. 1 and solving for V_1 with $\alpha_2 = 1$ yields:

$V_1 = V_{BE2} - V_{\gamma 3} + V_{CC} - R_{C2}(V_1 - V_{BE2})/R_E$

or:

$$V_1 = V_{BE2} + (V_{CC} - V_{\gamma 3})/(1 + R_{C2}/R_E) \quad (3)$$



2. Calculating threshold voltages. Positive and negative switching thresholds are the most important Schmitt parameters. Simple way of finding positive-going voltage (V_{T+}) needed to switch from high to low state is to use Thévinin equivalent (right) of circuit (left) in (a), with Q_2 in cutoff and Q_3 in saturation. To compute negative-going threshold (V_{T-}), Q_2 is saturated while Q_3 is cut off, as in (b).

The equation for V_{T-} becomes:

$V_{T-} = -V_{BE1} + V_{BE2} - V_{\gamma 3} + V_{C2} = -V_{BE1} + V_1$

Replacing V_1 with Eq. 3:

$V_{T-} = -V_{BE1} + V_{BE2} + (V_{CC} - V_{\gamma 3})/(1 + R_{C2}/R_E)$

Since V_{BE1} approximately equals V_{BE2}, this equation reduces to:

$V_{T-} = (V_{CC} - V_{\gamma 3})/(1 + R_{C2}/R_E)$

With the circuit component values shown and with $V_{\gamma 3} = 0.55$ v, the negative-going threshold voltage can be easily evaluated:

$V_{T-} = (5\text{ v} - 0.55\text{ v})/[1 + (2\text{ k}\Omega)/(460\,\Omega)] = 0.83$ v

Both threshold voltages vary considerably with supply voltage V_{CC}. For example, a 1-v change in V_{CC} will cause a variation of 380 millivolts in positive-going threshold voltage V_{T+}:

$dV_{T+}/dV_{CC} = 0.38$

Similarly, for V_{T-}:

$dV_{T-}/dV_{CC} = 1/(1 + R_{C2}/R_E) = 0.185$

The type 7413 Schmitt trigger can operate over a wide temperature range. Positive-going threshold V_{T+} is almost insensitive to temperature changes because its thermal variations either cancel or are negligible. And negative-going threshold V_{T-} is only slightly temperature-dependent:

$V_{T-} = V_{CC} - V_\gamma/(1 + R_{C2}/R_E)$

Differentiating this equation with respect to temperature (T) yields the negative-going threshold temperature dependence:

$dV_{T-}/dT = dV_\gamma/(1 + R_{C2}/R_E)dT$

Since $dV_\gamma/dT = -2$ mv/°C, then:

$dV_{T-}/dT = 0.37$ mv/°C.

Widely used Schmitt circuits

The integrated Schmitt trigger is useful in a variety of applications. For instance, Fig. 3a shows a simple RC multivibrator that can be implemented with only one-half a type 7413 Schmitt trigger, plus a single resistor and a single capacitor.

Circuit operation is simple. Capacitor C is initially uncharged and has a voltage across it that is less than V_{T+}; the circuit's output level is high. The capacitor charges through resistor R and through multiple-emitter transistor Q_1. When the voltage across C reaches V_{T+} (about 1.6 v), the Schmitt changes state so that its output goes low, discharging C through R and saturated output transistor Q_7. When capacitor voltage drops to V_{T-} (about 0.8 v), the Schmitt switches to its high state and C begins to charge again.

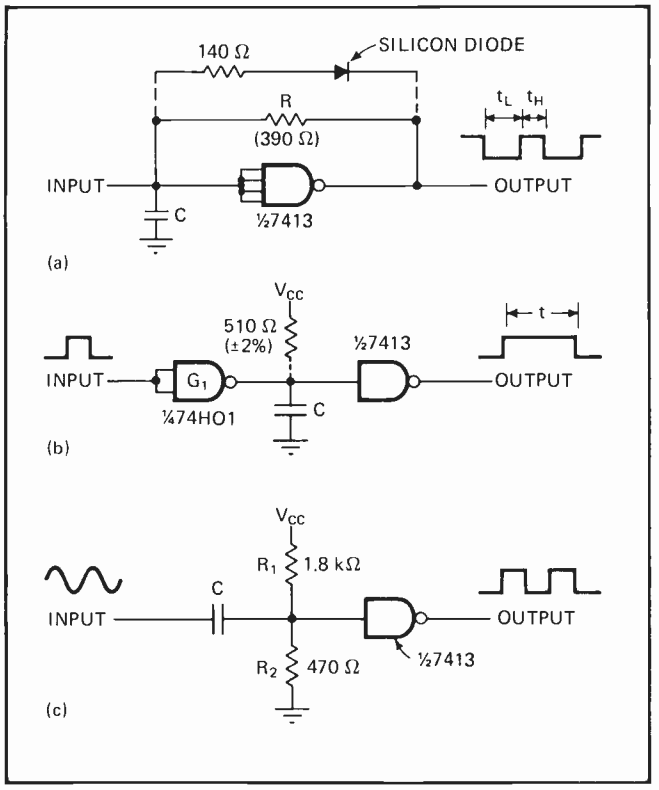
Several dc considerations influence the selection of resistor R. It must not draw excessive current from the output, but its value must be high enough to prevent the loading of subsequent stages. Its maximum value is restricted by the current-sinking capability of output transistor Q_7. A resistance of 390 ohms is recommended by one manufacturer of the type 7413 Schmitt for a fanout of 2.

With R = 390 ohms, the equations for output pulse width are:

$t_H = 0.15C$

$t_L = 0.34C$

where t_H is the period of time (in nanoseconds) during which the multivibrator is high, and t_L the duration (in nanoseconds) of the low output period. (The units of ca-



3. Using the Schmitt. Simple multivibrator (a) requires only external resistor and capacitor; adding diode and second resistor achieves 50% duty cycle. For pulse stretcher (b), extra resistor compensates for unit-to-unit processing variations so that output pulse width is more predictable. Biasing Schmitt at its mid-threshold point enables it to convert sine waves to square waves (c).

pacitance are picofarads.) Multivibrator frequency in hertz, therefore, will be:

$f = (2.02 \times 10^{-3})/C$

where C is in farads.

As the timing equations indicate, the multivibrator output is low approximately 70% of the time. Adding a resistor and a diode, as shown by the dashed lines, reduces the discharge cycle time, yielding a multivibrator with a duty cycle of 50%. With the values shown, output frequency becomes:

$f = (3.3 \times 10^{-3})/C$

Again, C is expressed in farads and f in hertz.

A relatively simple one-shot (or pulse stretcher) can be built with the circuit configuration of Fig. 3b. When an input pulse is applied to NAND gate G_1, its output goes low, but the Schmitt trigger's output remains high. Before the Schmitt can switch to its low output state, capacitor C must charge to V_{T+}. The charging resistor is the base resistor of transistor Q_1. Output pulse width for this circuit is nominally:

$t = 1.95C$

where t is in nanoseconds and C in picofarads.

Variations in the charging resistor cause output pulse width to vary from unit to unit. Performance can be improved by inserting a resistor between the supply and the capacitor. Pulse width then becomes:

$t = 0.26C$

for t in nanoseconds and C in picofarads. Pulse width is reduced with the additional resistor.

Another useful circuit converts a sine wave to a square wave, as shown in Fig. 3c. Resistors R_1 and R_2 bias the Schmitt trigger at the mean value of its threshold voltages to obtain the necessary 50% output duty cycle. To avoid differentiating the input signal, the impedance of capacitor C at the operating frequency of interest should be much less than the parallel resistance of R_1 and R_2:

C approximately equals $(4.3 \times 10^{-3})/f$

where C is in farads and f in hertz.

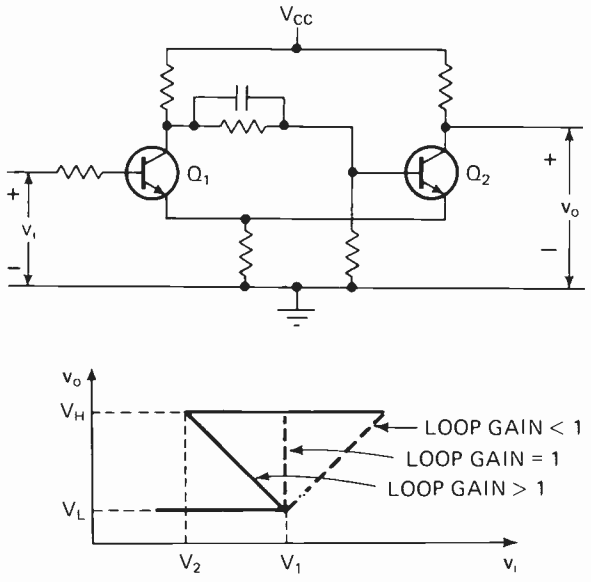
The converter can be operated at frequencies up to about 8 megahertz. If all four inputs of the Schmitt trigger are tied together, peak input voltage can be as high as 6.5 V. If only one input is used, maximum input voltage becomes 5.5 V peak. The minimum input voltage should be about 1 V peak. □

The Schmitt trigger reviewed

A variation of the basic Eccles-Jordan bistable multivibrator, the Schmitt trigger is also called an emitter-coupled binary. Unlike the conventional binary, it exhibits hysteresis, switching from one state to another at different threshold voltages, depending on the direction of the triggering input. Additionally, the Schmitt's input terminal is not involved in regenerative switching and so keeps the same potential during and after transition, creating an excellent triggering circuit.

Normally, the Schmitt operates with a loop gain of greater than unity. Circuit hysteresis can be eliminated by making the loop gain equal to unity through resistance adjustment. The positive- and negative-going threshold voltages can also be shifted.

For a more-than-unity loop gain, input voltage v_i must reach positive-going threshold V_1 before the Schmitt can switch to its high output state ($v_o = V_H$). When v_i decreases, it must pass the V_1 threshold level before the transition to the low output state occurs ($v_o = V_L$). The circuit is unstable in the region between V_L and V_H. For the low output state, Q_1 is off and Q_2 on; for the high state, Q_1 is on and Q_2 off.



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Electronic fuel injection reduces automotive pollution

An MOS read-only memory is at the heart of a British system that minimizes pollutants by measuring exact quantities of fuel and timing their insertion into combustion chambers

by Malcolm Williams, *Joseph Lucas (Electrical) Ltd., Shirley near Solihull, England*

☐ In a massive effort to limit automotive exhaust pollution, one of the devices being evaluated carefully is an electronically controlled fuel-injection system.

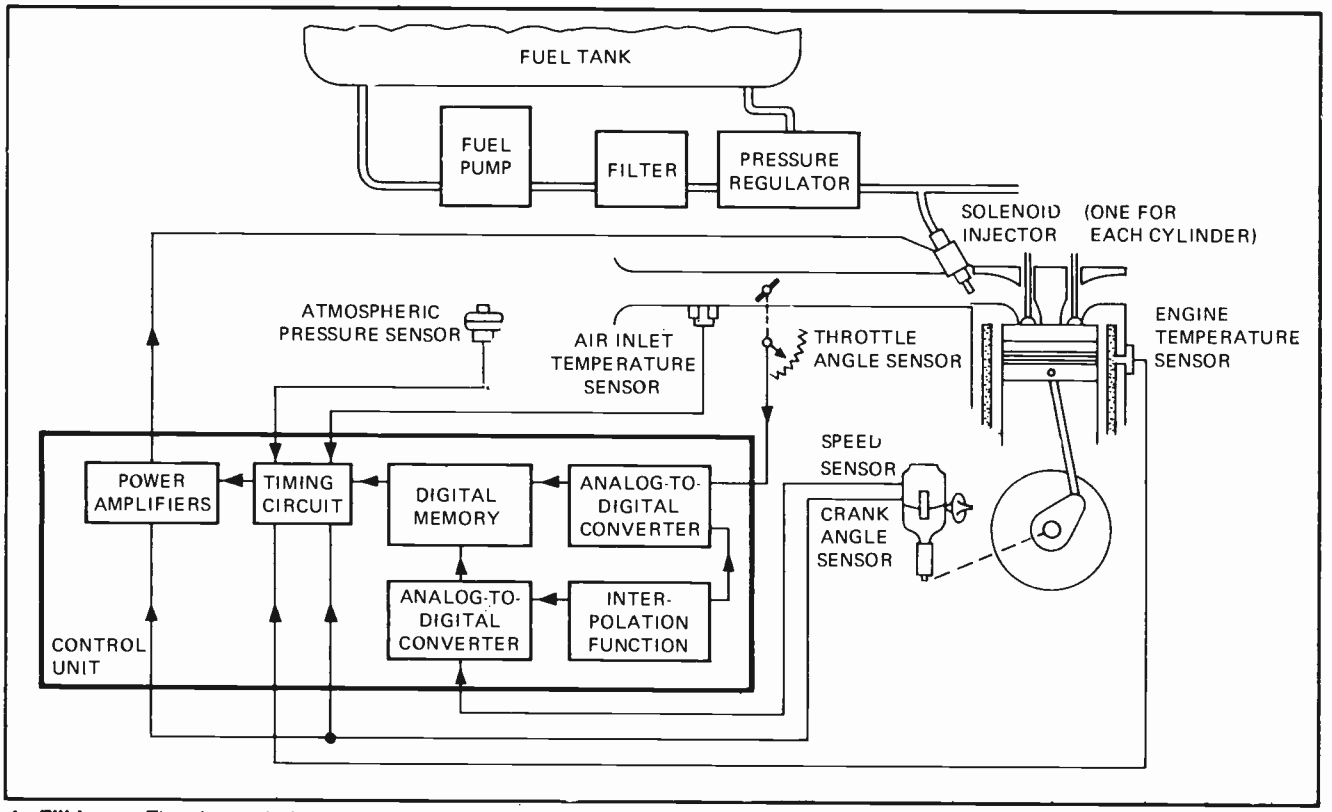
Besides the advantage over standard carburetion of increased power offered by fuel injection, the accurate cylinder-to-cylinder fuel distribution and optimum fuel control under turbulent manifold air conditions enable fuel injection to minimize exhaust pollution.

It is unlikely, however, that a fuel-injection system alone will meet the latest legal emission requirements, and some form of exhaust treatment also will be necessary. Nonetheless, the cost of exhaust treatment in a vehicle fitted with fuel injection would be lower than it would be without fuel injection.

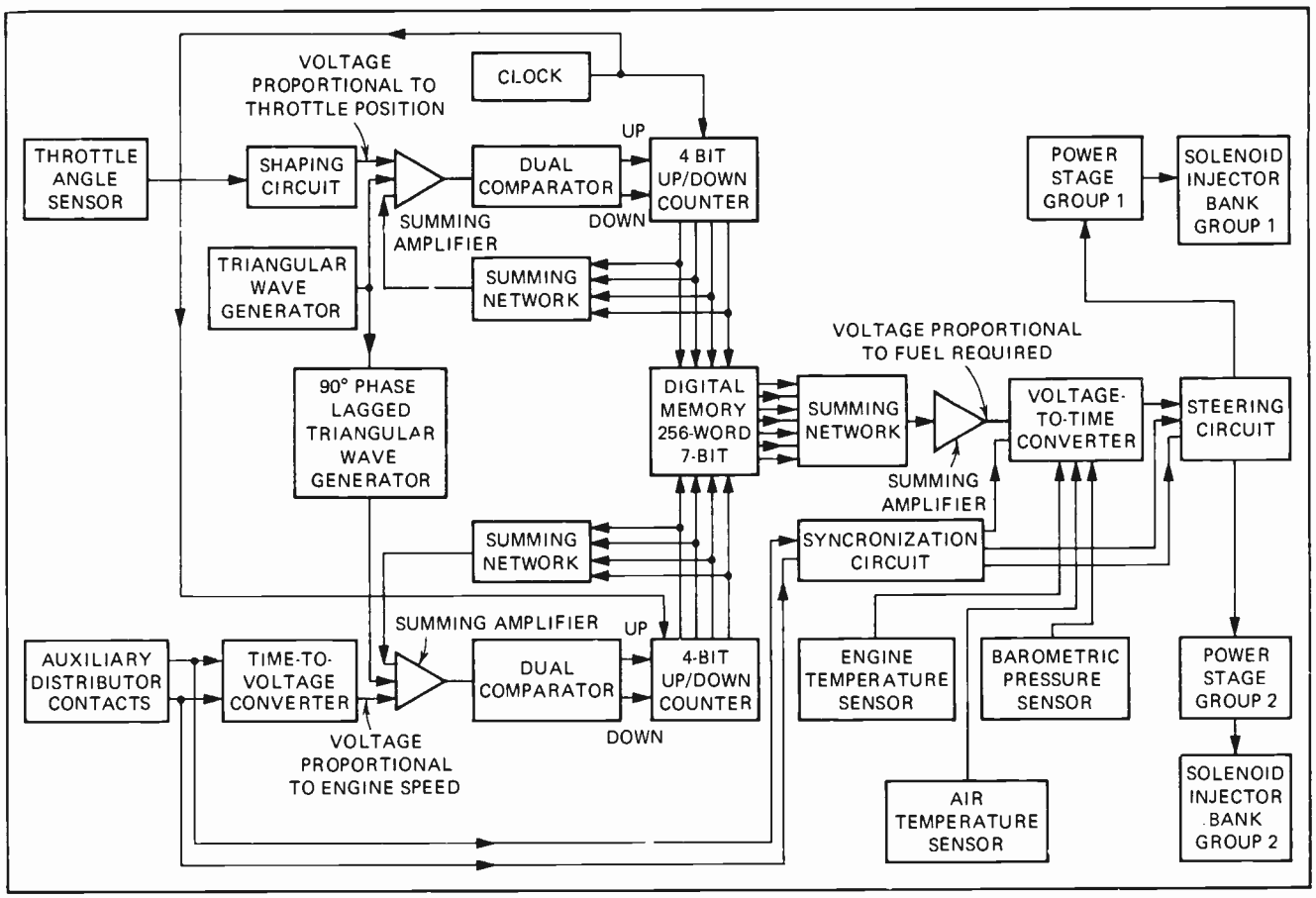
To achieve low-pollution exhaust emissions, a high air-to-fuel ratio is required over the engine's complete working range. This minimizes wasted fuel, and, as a consequence, gives rise to fewer partially burnt pollutants. It is also important to obtain an accurate measurement of engine conditions and fast, accurate measurement of air-mass flow. The system must be able to supply the optimum amount of fuel when the air in the inlet and exhaust manifolds is resonating.

The engine parameters that best meet these requirements are throttle angle and engine speed. But the cost of a complex control function is prohibitive if standard analog electronic techniques are applied. However, by using a digital memory to store the fuel-demand characteristics, a system becomes economically attractive.

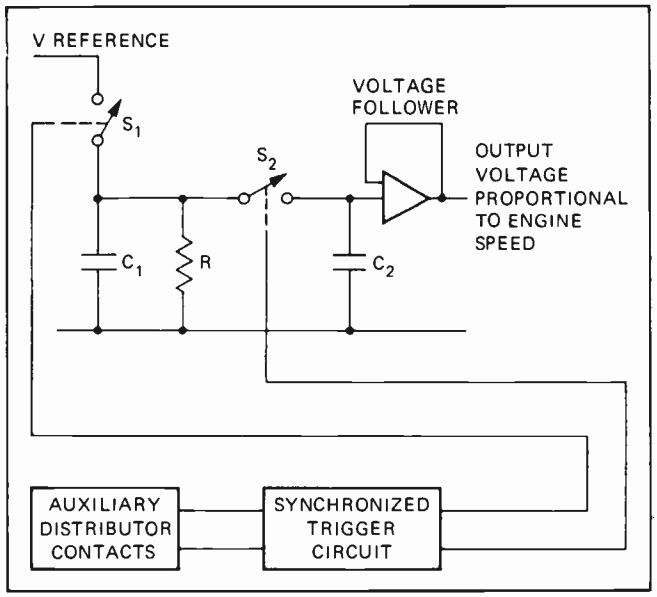
A prototype fuel injection system has been developed for a standard 150-cubic-inch, six-cylinder Triumph sedan. Engine speed and throttle angle information are stored in a digital memory containing 256 seven-bit words. Each word in the MOS read-only memory repre-



1. Fill 'er up. The electronic fuel-injection system shown as part of the auto power plant is designed to provide accurate amounts of fuel to the engine cylinders. based on demand (throttle angle), engine speed, engine temperature, and ambient conditions.



2. Electronic controller. The complete fuel-injection system comprises TTL, MOS, and linear devices to process analog information from engine and throttle to produce signals that help determine the exact fuel quantity to be fed into each cylinder.



3. Speeding ticket. To get engine-speed information, auxiliary contacts are mounted on the distributor. The circuit shown above converts the time measured between contact pulses into analog voltage. This voltage is converted to digital signals.

sents a different quantity of fuel. By reading out the right word at the right time, the correct quantity of fuel is injected into the induction port of the engine. The selection of the word is controlled with the information supplied by strategically placed sensors that monitor the engine's condition and driver's demand (Fig. 1).

Both digital and linear ICs were used. Their functions include counting, comparison, and amplification to convert analog data into a form that will address a digital read-only memory and for interpolation between the exact digital steps. Interpolation is necessary because the memory covers the range of possible engine fuel requirements and must progress smoothly from one state to another.

When the driver switches on the ignition, the electric fuel pump mounted in the trunk sends fuel to the solenoid injectors in the engine. Injection pressure is constant, and the controller determines the quantity of fuel injected by controlling the time the injector is open. Hence, each word stored in the memory corresponds to a time interval.

On turning over the engine, auxiliary contacts in the distributor cause the solenoid injectors to commence fueling at the correct point in the engine cycle and also provide engine-speed information to the control circuit, selecting the appropriate memory word (Fig. 2). With a cold engine, the fuel supply is increased over the amount a hot engine would need by multiplying the quantity stored in the digital memory by a factor dependent on the engine's temperature sensor. This sensor, which is fitted on the engine block, is tailored to provide easy starting with minimum emissions and thereby function as an automatic choke.

The driver controls the power delivered by the engine by depressing the accelerator pedal, which controls the

throttle aperture in the air intake. The angle of the restricting butterfly valve, in conjunction with the engine speed, measures air flow. Both the driver's demand and the engine's air intake can be measured by coupling a potentiometer to the throttle shaft. As the throttle is depressed, extra air flows into the engine, and simultaneously a new word is addressed in the memory, thus optimizing the amount of fuel injected into the cylinders.

To account for changes in air density due to climatic conditions and radiant heating by the engine of the intake air, an atmospheric pressure sensor and air-inlet temperature sensor are also installed.

Data converted

The throttle angle and engine-speed information both have to be converted into digital form to address the memory. Whenever the combination of throttle angle and engine speed hit a precise point in the memory, the engine's fuel demand is obtained by direct reference. However, when the values of throttle angle and engine speed are between these exact memory sites, the engine fuel demand is calculated by interpolation from the adjacent stored data.

For the throttle signal, a potentiometer output proportional to throttle angle is first shaped to define more closely the changes at the initial low throttle opening. The signal is then converted into digital form by a simple analog-to-digital converter, which uses a feedback resistor network. For signals of equal amplitude, the output from the amplifier is zero, and the digital word-signal feedback from the counter is equal to the input analog signal. When this analog signal increases, the output from the amplifier decreases from zero until the comparator threshold level is reached.

The counter is then allowed to count up the clock pulses, thus changing the digital word until equality of both signals again is achieved. The digital signal remains constant until an error greater than half the least-significant bit occurs, at which point the digital value changes to reduce the error. This particular a-d converter tracks the throttle signal rapidly.

The auxiliary contacts mounted in the distributor provide engine-speed information, which is turned into an analog voltage from the time between contact pulses

EXHAUST POLLUTION EMISSIONS IN EXPERIMENTAL CAR
(grams/mile)

Pollutant	U. S. Federal	California	Achieved on Test Engine*
1971 LEGISLATION[1, 2]			
Carbon Monoxide	23	23	3.5
Hydrocarbons	2.2	2.2	0.8
Nitrogen Oxides	–	4.0	0.8
1975 LEGISLATION[3, 4]			
Carbon Monoxide	3.4	12	3.5
Hydrocarbons	0.41	0.5	0.8
Nitrogen Oxides	3.0	1.0	0.8

*7–mode California cycle

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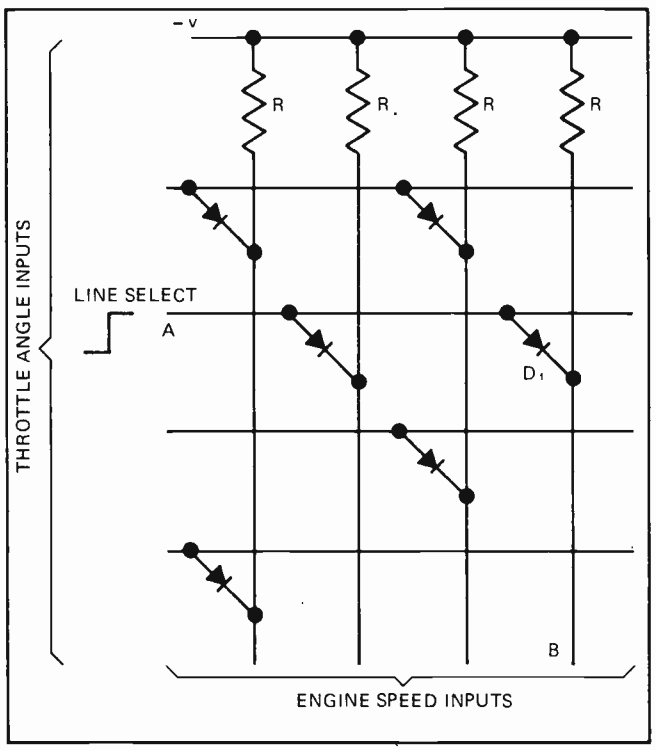
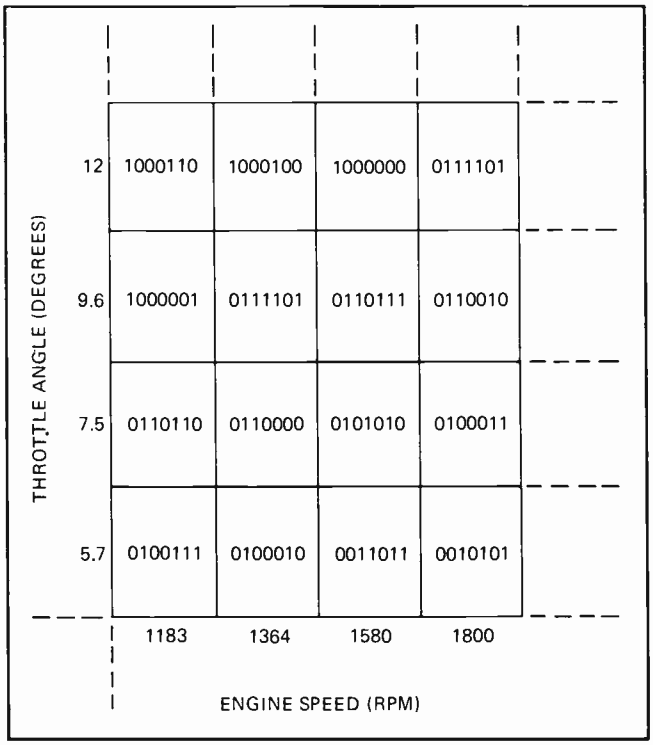


4. Memory lane. Digital words representing throttle angle and engine speed are fed into a decoder circuit, which then selects a programed line in the memory matrix to calculate fuel quantity.



5. Fuel program. Each box in the memory program has a digital code number representing location and proper amount of fuel required for that particular operating condition.

(Fig. 3). On closure of the first contacts, capacitor C1 rapidly charges toward a reference voltage. After about 5 microseconds, S1 opens, and the capacitor decays through a fixed resistor R for the remainder of the engine revolution. When the second distributor contact closes, this voltage is sampled for about 10 μs through switch S2 and is stored on capacitor C2. The voltage follower acts as a buffer to prevent discharge of capacitor C2. This cycle is repeated for every engine revolution.

Another a-d converter changes the analog voltage representing the engine speed to a digital word. The two four-bit digital words—one representing throttle angle, the other representing engine speed—are fed to decoding circuits; each decoder circuit then selects a particular line in the memory matrix (Fig. 4).

Engine-speed conversion

For example, if line A on the throttle input is selected and a positive voltage is impressed on the line, then diode D will conduct. If line B is sensed by the engine-speed decoder, the positive voltage through diode D will be sensed on line B if the particular line sensed has no diode on line . If the particular line sensed has no diode, then a negative voltage would be sensed. So by the presence or absence of a diode, a binary 1 or 0 can be programed for any particular input line.

This example shows a simple memory matrix of 16 one-bit words. To increase the number of bits, separate matrixes should be addressed simultaneously. The digital memory used in the controller consists of 256 words, each of seven bits. MOS transistors are used to form the matrix instead of diodes.

The digital information (Fig. 5) stored in the square corresponding to the intersection of throttle angle 9.6° and engine speed 1,580 rpm is 0110111. The data in the adjacent sites in the memory bear no relation to each other, and whatever the optimum fuel required by the engine at the appropriate site, it can be provided by the control system.

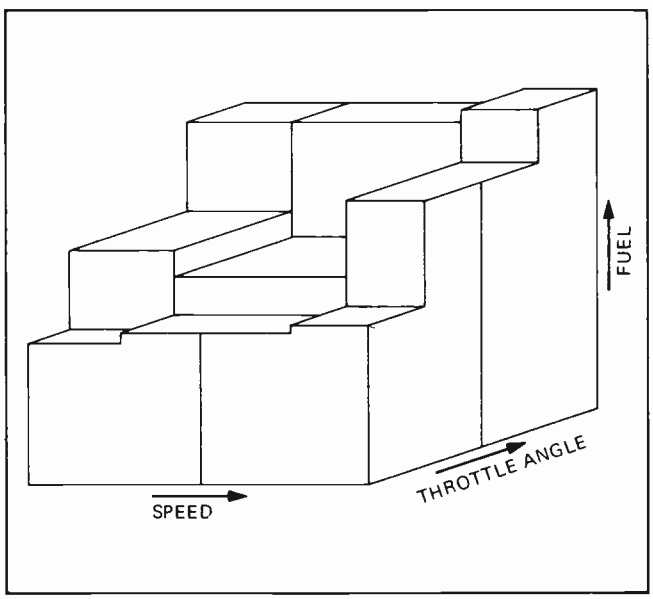
The fuel surface represented by the stored information in the memory would consist of a number of flat planes (Fig. 6), the height being proportional to the fuel quantity to be delivered per engine stroke. However, the required surface cannot have these discrete steps. The control unit achieves a smoothly varying surface by linearly interpolating stored data whenever the combination of the throttle angle and engine speed do not hit an exact memory site (Fig. 7).

Circuits interpolate

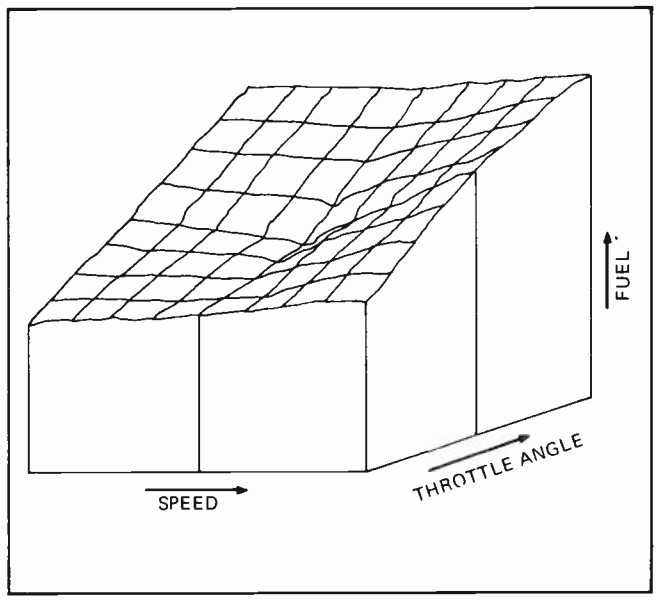
There are two interpolation circuits—one for engine speed and one for throttle angle. Each generates a positive and negative triangular wave of fixed amplitude and frequency. The effect, for each parameter, is to make the memory sites each side of an intermediate point read out alternately for periods proportionate to the distance of the sites from the intermediate point. To do this, the triangulations superimpose on the sensor voltage from the summing amplifier. To distinguish between the two parameters, one wave generator is placed 90° out of phase behind the other.

When a sensor output voltage corresponds exactly to one of the 16 matrix input levels tied to that sensor, the positive and negative triangular oscillators are equal in amplitude, and the running voltage level in the comparator is within the threshold levels identifying that particular matrix line. When the sensor voltage moves slightly, one triangle peak pushes the comparator voltage within the levels identifying the next matrix line for a fraction of the triangle cycle time.

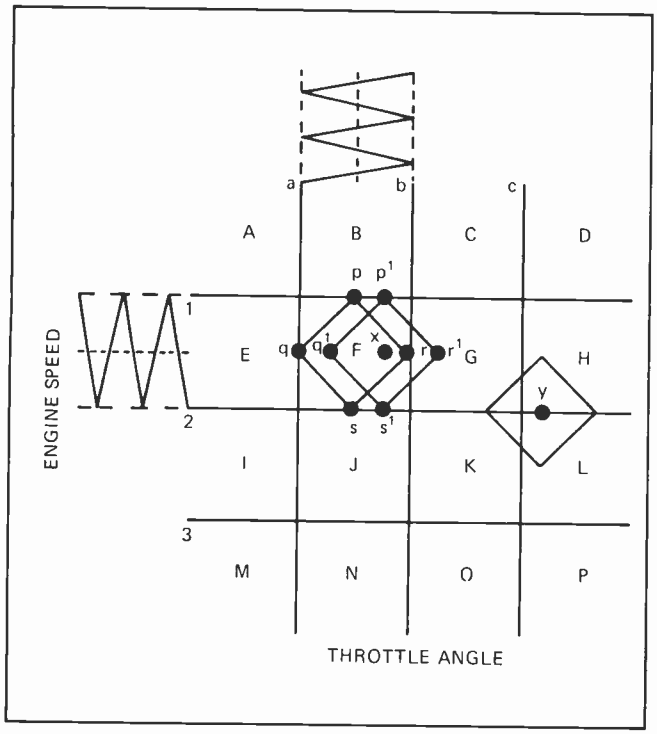
Half-way between the lines, half the triangle extends into the next line level, and so on. To connect voltage levels and matrix lines, each line in each parameter is identified by a four-bit digital word, and an a-d converter translates voltage into word. Hence, two four-bit words act on each of the seven memory planes, identifying in each plane a particular memory site. All seven sites are read out simultaneously, making a seven-bit



6. Injection plot. Without interpolation, a three-dimensional plot of speed, throttle angle, and fuel amount would look like this series of discrete and flat planes produced by an X-Y plotter.



7. Bumpy road. With interpolation to facilitate continuous engine operation, the surface of an X-Y plot becomes a series of undulations, assuring smoother engineer operation.



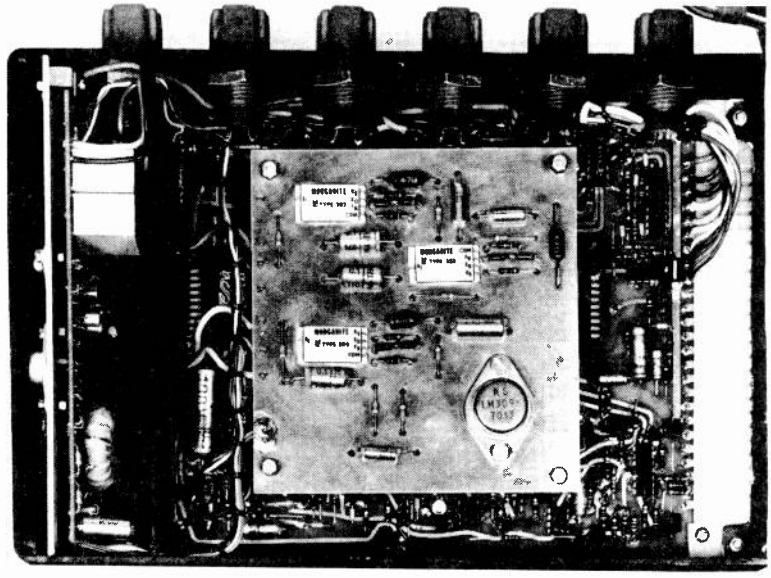
8. Gas station. When fuel demand coincides with an exact memory site, the interpolation signal causes only that site to be addressed (point F); but when fuel needs don't correspond to an exact site—which is normally the case—an interpolation of as many as four adjacent word sites may be necessary (point Y).

word identifying an exact injector opening time. Because most throttle and engine-speed selections will be somewhere between exact sites, most of the time the memory output, under the influence of the interpolation circuits, is cycling around four adjacent sites.

Fig. 8 shows the effect of the triangular waves on the memory where the memory sites, alphabetically labelled, represent the engine conditions when the fuel data have been measured. The solid lines represent the decision points where the a–d converter changes from one word to the next, thus selecting a different memory site. When the driver's demand, i.e., throttle angle and the resulting engine speed, are both sent to the same memory site, the interpolation signal causes only that memory site to be addressed. For example, if F is the selected point, the resultant path traveled through the matrix is the square bounded by p, q, r, and s. When the driver demands more power, point x would be selected, and the output from the memory would be alternatively the words stored at memory sites F and G.

As the matrix is swept at a constant velocity, the time for which each word appears at the output of the memory is proportional to the throttle-angle position between F and G. A lag in the summing circuit averages the memory output to give linear interpolation between F and G. With the throttle angle and engine speed set to select the point Y—the typical operating situation—the output from the memory consists of the four adjacent word sites G, H, K, and L in cyclical sequence. These words are averaged to produce a two-dimensional interpolated surface (Fig. 7).

To control the fuel delivered to the engine, auxiliary distributor contacts activate the synchronization circuit, which, by means of the steering circuit, turns on an appropriate group of injectors. At the same time, the voltage-to-time converter commences its timing period.



9. It's a gas. Prototype unit contains both ICs and discrete semiconductors, but follow-on versions will replace analog with digital devices. Protrusions on the top of the unit are power resistors used to set the time-constant of the solenoid fuel injectors.

This period is a direct function of the voltage supplied from the memory, but it's modified, depending on engine temperature, air temperature, and barometric pressure. At the end of the timing period, the steering circuit is reset, and the appropriate group is turned off, cutting the fuel supply to those particular cylinders.

Prototype has standard parts

The prototype unit specifically developed to control the fuel system for the test vehicle (Fig. 9) is 2.25 inches by 6.75 in. by 10.25 in. All the components, as well as some discretes, are readily available ICs; for instance, a standard MOS ROM has been programed with the information pertaining to the Triumph that had been obtained from engine tests. However, in production units, custom-designed integrated circuits would be used exclusively.

Although the system is in the early development phase, it has already shown considerable improvement over currently available fuel-control devices. Development is being continued to assess the full potential of this type of control system. The pollution figures from this unit have fallen short of meeting the new Federal and California requirements for 1975 (see Table 1), although it did perform within the limits of previous legislation. This unit has shown that accurate fueling under both steady-state and transient conditions can reduce pollutants and work in conjection with a total antipollution system.

Current work is aimed at digitizing the analog speed-measurement stage and the analog fuel-measurement stage after the memory. A digital interpolation technique is being devised so that the only analog stage in the system will be throttle-angle sensing. This should mean that all the electronics can be packed on one bipolar IC and one MOS IC. □

Take a bit of advice: use 16-bit converters carefully

Their wide dynamic range and extremely fine resolution allow design simplification, while improving performance and cutting costs. But take care in applying them, or their performance will be wasted.

by Wayne Marshall and Cyril Brown, *Analog Devices Inc., Norwood, Mass.*

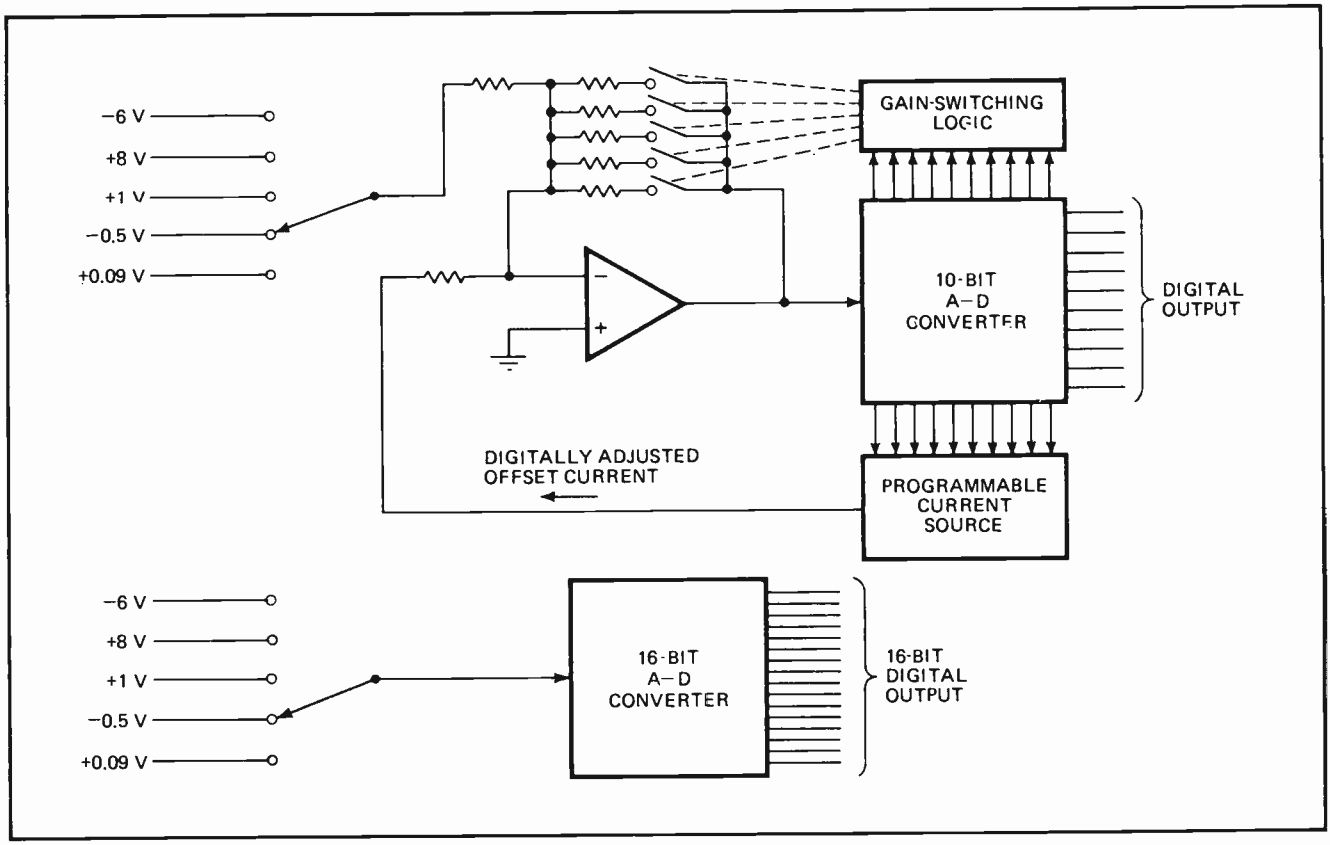
☐ A 16-bit analog-to-digital or digital-to-analog converter that actually works is something of a modern technological marvel (See Part I of this two-part article in the last issue of *Electronics*). True 16-bit devices are now available off-the-shelf, but at prices on the order of $1,000. The extremely fine resolution, monotonicity, high accuracy, linearity, and broad dynamic range that characterize these converters make them ideal for a wide variety of applications—from nuclear research to precision function generation.

However, the unsophisticated user may waste the advantages of the converter's tight performance specifications unless he exercises extreme care in circuit design. Potential perils that must be considered include thermocouple effects, voltage drops in short lengths of wire, low-level noise, radio-frequency interference, and even millivolt common-mode signals. In short, factors of only secondary concern in the design and use of a 12-bit converter can have an overwhelmingly adverse impact on the operation of a 16-bit unit.

To understand how and where these precision converters can be most effectively applied, it is helpful to begin by studying their key characteristics, then examining applications that these characteristics suggest, and finally discussing methods to ensure that the devices will operate properly in a real-world environment.

Would you believe 65,536:1?

The most outstanding characteristic of a 16-bit converter is its extremely wide dynamic range—that is, the ratio of full-scale value to the value of the least-significant bit (LSB) it can handle. For a 16-bit converter, the



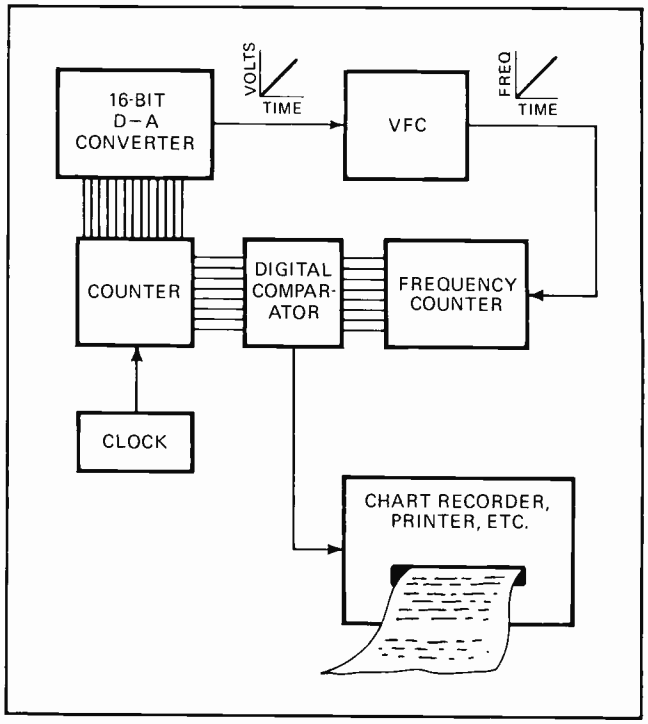
1. Simplicity. Complexity of conventional gain-changing data-acquisition circuitry (top) is reduced by exploiting wide dynamic range of 16-bit converter (bottom). Bottom circuit is not only simpler, it's also more accurate, faster, and less expensive.

dynamic range is 2^{16}:1, or 65,536:1, or slightly more than 96 dB. Thus a d-a converter with a full-scale output voltage of 10 V can change its output in steps as small as 150 μV, approximately.

This wide dynamic range means that many naturally occurring variables—like light and sound levels—can be handled by these converters without range-switching or variable-gain amplifiers. The high resolution implied by a wide dynamic range means that accurate ratio measurements can be made between two large-amplitude signals that differ by only a small amount.

A true 16-bit converter must have a linearity specification commensurate with its resolution. For 16 bits, this means that the maximum deviation from perfect linearity should never exceed 0.0015% of full scale. Some applications that only need, say, 12 bits of resolution are better served by a 16-bit converter because of its superior linearity.

Scintillation counters, ion chambers, and other nuclear instruments, for example, are frequently used to separate energy levels, charge levels, or particle momenta into well defined categories. The number of categories that can be obtained is determined by the resolution of the converter, but the uniformity of the category "widths" is determined by its linearity.



2. Function generator. D-a converter is used as ramp generator in setup for testing linearity of voltage-to-frequency converter.

Monotonicity is the tough one

Monotonicity is the toughest single specification that a converter must meet, because it imposes a maximum limit of ±½ LSB on the converter's step-to-step nonlinearity. What is most difficult is preserving the converter's monotonicity over a useful temperature range. Monotonicity is particularly important in digital servo systems. If such a system is trying to find a null, and the converter is non-monotonic around the balance point, the null balance will never be attained.

Speed is a converter parameter that can be all-important in one application and insignificant in another. Automatic testing systems and CRT displays obviously demand fast converters. However, many slower systems can benefit from using high-speed a-d converters to fight noise. The trick: take several readings of the same input signal in quick succession and average them. Noise will be reduced proportionally to the square root of the number of readings.

Accuracy's true meaning

The definition of accuracy is a semantic problem that tends to separate the purists—who think in terms of National Bureau of Standards certification—from the engineers and scientists with data to acquire or distribute. Since the best zener reference sources drift at some 5 ppm/°C, it is difficult to see how a converter can claim any reference to NBS certified standards. The reality is that 16-bit converters don't claim absolute accuracy to 0.0015%, but offer 15 ppm resolution, linearity to 15 ppm, and excellent stability, which can be exploited for valuable results.

Absolute accuracy is certainly the critical specification for a digital voltmeter, which must make error-free readings from a variety of unrelated sources. By contrast, an a-d converter usually takes readings within a given system, where *relative* voltage magnitudes, *not absolute ones*, are required. Nonetheless, of course, the relative magnitudes must be measured with considerably certainty, but this requires high linearity if the converter uses a reference common to all sources, rather than absolute accuracy.

Closely related to a converter's accuracy is its stability over both time and temperature. This stability must be commensurate with the need for repeating measurements day after day without introducing discrepancies between one day's results and the next. This is often a relative accuracy factor, since the absolute values of readings may be unimportant so long as they can be repeated with precision. An example occurs in computer-output microfilming, where it may be necessary to update data on a piece of film that was originally recorded days, or even months, earlier.

Eliminating range switching

What applications do the preceding characteristics suggest? One obvious one is the elimination of range-switching and variable-gain amplifiers. An example of such an application is in a multichannel data acquisition system that must digitize analog signals developed by thermocouples, strain gauges, and other transducers (Fig. 1). The upper diagram of Fig. 1 shows the rather elaborate arrangement required to switch amplifier gain automatically from channel to channel to bring the low-level signals up to the converter's full-scale input range. The bottom illustration shows the dramatic reduction in complexity provided by a 16-bit converter.

But the 16-bit machine does more than simply eliminate a few extra components. It can improve performance and cut costs at the same time. To understand how, suppose that the system of Fig. 1 requires the nominally 8-V input to be resolved within 1 millivolt over the range of 8 to 9 V. Since a 10-bit converter with

a 10-v reference provides only slightly more than 100 increments between 8 v and 9 v, preamplification by 10 is needed to obtain the desired resolution.

How can a voltage between 8 v and 9 v be multiplied by 10 and still fit into the converter's 10-v amplitude range? The answer is to use an op amp and apply to its summing junction a stable bias current having a magnitude that is exactly sufficient to make the amplifier output zero when the 8-v input is applied. This will allow the 1-v difference signal between 8 v and 9 v to be expanded to fill the converter's full 10-v span. In this way, the 10-bit converter can resolve the amplified signal variation to 1 part in 1,024, or slightly better than 1 mv. However, in addition to a programable-gain amplifier, the auxiliary equipment now requires a bias source output to be fed into the amplifier's summing junction.

If the system involves many suppressed-zero readings like the foregoing, the circuitry for generating the precise biasing currents adds significantly to the complexity of the over-all conversion equipment; it also adds error sources at the 10-bit level, even though 1-mv resolution of the expanded 1-v signal swing requires performance at roughly the 13-bit level.

Although a 16-bit a-d converter costs appreciably more than any 10-bit counterpart, over-all cost of equipment is considerably reduced, and performance is improved: the 1-v interval between 8 v and 9 v is resolved into more than 6,000 150-μv steps, with 16-bit, rather than 10-bit, operation. Further, because it takes an automatically switched amplifier roughly 500 microseconds for each range change, the digitizing rate is greatly enhanced by use of the 16-bit converter, since range switching is eliminated.

A 16-bit converter can be surprisingly useful in precision function generation. Because the LSB is such a tiny fraction of the full-scale output of a 16-bit d-a converter, the converter can be programed to produce a wide variety of output functions with a quantizing noise level approximately 96 dB below full scale.

The usefulness of such a function generator is illustrated in Fig. 2. A setup is shown for testing the linearity of precision voltage-to-frequency converters (VFCs). The automatic testing setup makes use of the d-a converter's excellent linearity as a ramp generator. Clock pulses accumulated in the up-down counter continually update the d-a converter, feeding an analog voltage ramp to the VFC undergoing the linearity test. By holding the quantizing noise of the converter's ramp waveform down to the -96-dB level, while simultaneously ensuring linearity at least tenfold better than the voltage-to-frequency converter's own performance specification, highly accurate calibration curves can be plotted.

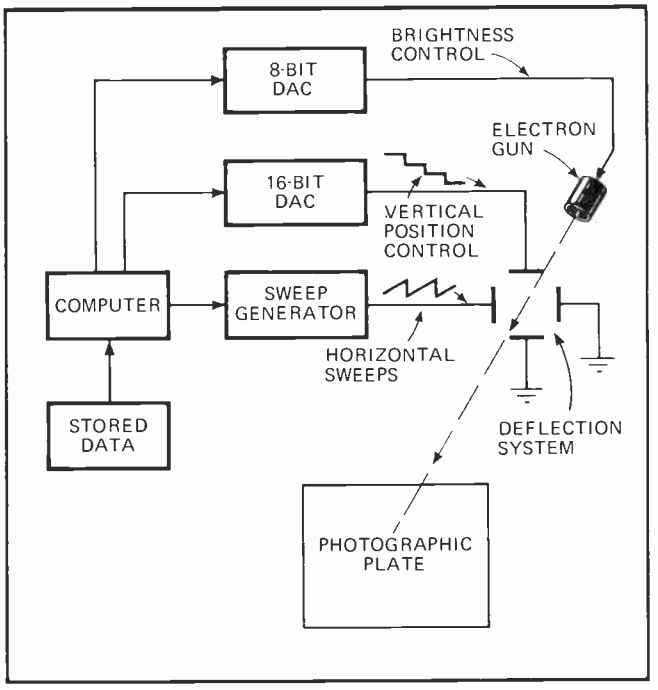
The technique can also be applied to digital frequency synthesizers to produce output waveforms in which harmonically related noise is some 96 dB below the full-scale signal level. In such an application the converter's output would be arranged for bipolar signal swings.

An undistorted view

Although CRT displays are widely used for presenting data to human operators-in aircraft flight controls, interactive computer terminals, newsprint preparation, and so on-there are many additional applications for the basic idea of using a deflected electron beam as a tool for generating and displaying data that have not yet been fully developed.

For example, "photographs" of Mars and other planets could be transmitted to earth by satellite-borne cameras, but they would have to undergo a considerable amount of digital massaging before emerging in conventional photographic format. Similarly, in geological and mineral explorations, where sonar and explosive reverberations are echoed from inner-earth strata and recorded for later transformation into pictures of the

3. Precise positioning. To approach the quality of a real photograph while using a TV-type raster-scanning approach, this CBS Laboratories electron-beam recording system uses a 16-bit d-a converter to set the beam's vertical position. Computer-enhanced photo of earth was taken from an orbiting satellite.



earth's geological cross-section, the raw data is processed by a computer before being converted into an image.

In both these instances, the final picture is produced by exposing a piece of photographic film inside a vacuum system to a digitally positioned electron beam. And it is often wise to use a 16-bit d-a converter to position the beam, even if 16 bits of positioning are not needed. The reason is a need for the 16-bit converter's linearity.

To see why this is so, consider the electron-beam recording system marketed by CBS Laboratories (Fig. 3). This system uses a raster-scanning process not unlike that of conventional television, but with eight bits of bright-to-dark-gray shading, and digital control of the vertical position. To avoid visible distortion in the pictures it produces, the CBS system imposes tight tolerances on the spacing between its horizontal scan lines.

Because a d-a converter's specifications allow an error of up to ±½ LSB on its output amplitude, it would be possible for successive horizontal scan lines to vary by as much as half a line width in their vertical positioning if the d-a converter's resolution were the same as the vertical resolution of the system. By using a 16-bit converter in a system that requires only 12 bits of vertical resolution, CBS has cut the sloppiness with which its 4,096 scan lines are positioned from ±½ line width to ±1/32 line width. The quality of the picture that results is evident in Fig. 3.

Preserving the performance

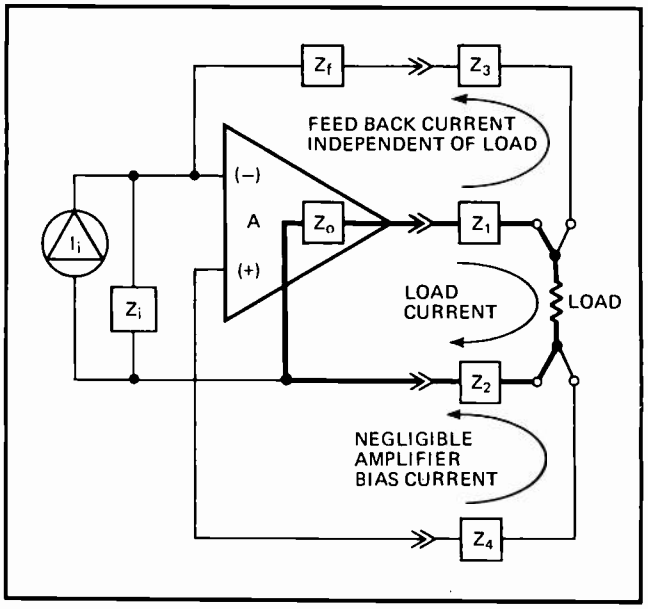
For the user to get all of the performance of which a 16-bit converter is capable, he must avoid the inadvertent introduction of errors on the order of 1 LSB. This is not as easy as it sounds. For example, just 15 mA—the full-scale output of some d-a converters—flowing through 2 feet of 18-gauge wire will drop approximately 165 μV, the equivalent of slightly more than 1 LSB.

To combat this problem, converter manufacturers have introduced four-terminal output-connection techniques (Fig. 4) that allow the user to include the impedance of the connecting circuit inside the amplifier's feedback loop. In short, feedback signals are derived from the load, ensuring that the converter's output amplifier places the desired voltage at the actual load terminals, and not merely at the converter's output pins.

In some applications—CRT displays and certain automatic test systems, for example—the output-voltage transients produced by the d-a converter cannot be tolerated. Deflection amplifiers tend to integrate these glitch spikes, creating dc offsets that may persist for many microseconds, creating a noticeable distortion in any smooth CRT trace.

Similarly, semiconductor testers that use d-a converters to control applied voltages and currents cannot tolerate glitches either. When these converters try to creep up slowly on critical threshold voltages, large glitch spikes can burst through the critical region, trigger erroneous responses, and even damage sensitive devices. In such applications, the use of a sample-and-hold deglitch module becomes mandatory.

The problem of getting data into a 16-bit a-d converter is analogous to the difficulties in transmitting



4. Error reduction. Four-wire output connection eliminates errors caused by voltage drop between converter output and load.

data from a 16-bit d-a converter to a remote load. Because the dc power for the a-d converter must travel a finite distance from the power supply, and perhaps pass through printed-circuit board interconnections with relatively high resistances, there is likely to be a voltage drop across the power cable and connectors that will raise the entire converter to some finite common-mode voltage. This voltage may easily exceed a few 150μV least-significant bits. In the absence of some subtle precautions in feeding analog data into the measuring circuitry, the digital conversion is therefore likely to be in error by many least-significant bits, because of this common-mode effect alone. The solution is to use a high-performance differential input circuit, or buffer, at the a-d converter's front end. The common-mode rejection of such a circuit then scales the common-mode voltage down to negligible proportions.

Shot noise, 1/f noise, and thermal noise can only be held to an irreducible minimum by careful circuit design and component selection. To keep the noise down, extreme care must be taken with the wiring associated with the converter. In particular, analog and digital grounds should be kept separate to prevent the leakage of large digital pulses onto the analog lines.

Because of high source impedances and other constraints imposed by various signal sources, it is much more difficult to minimize noise effects when measuring, instead of generating, precise analog values. In fact, the 16-bit a-d converter is vulnerable to radio-frequency interference, 60-Hz pickup, feedthrough from digital power-supply transients, and even magnetic coupling from nearby motors and transformers. Therefore, even if all possible care has been taken to minimize circuit noise, it still may be necessary to use the data-averaging technique mentioned earlier. This technique exploits the converter's high speed by taking several readings of the same input data. In this way, averaging techniques will yield a reading that approximates more closely the true analog input. (Noise is reduced in proportion to the square root of the number of readings.) □

Tables shorten design time for active filters

Both low-pass and high-pass Butterworth-Thomson filters, which use either unity-gain or infinite-gain amplifiers, can be designed from tables of normalized component values; filter orders as high as 10 are covered

by Farouk Al-Nasser, *Honeywell Test Instruments division, Denver, Colo.*

☐ As the IC operational amplifier grows steadily better and cheaper, active filters are becoming more popular than passive. Their performance is superior and more predictable, they have no need for impedance matching, nor are nonlinear inductor properties a problem, since the active filter uses an op amp and an associated RC network to simulate inductance.

But perhaps the greatest attraction that active filters hold for the designer is that they lend themselves to a building-block approach. Being inherently isolated, they can be cascaded to realize higher-order filter functions, and the passive-component values needed to implement each filter block or section can be computed in a normalized form and tabulated. This also means that active-filter design can be reduced to a matter of looking up tables, once the engineer has determined the type of filter required and chosen a filter circuit.

Selecting the right type of active filter depends on the signal being processed, as well as the time- and frequency-domain properties that the filtered signal must have. The Butterworth type of filter, for instance, exhibits flat passband amplitude characteristics up to the cutoff frequency, a rolloff of $-6n$ decibels per octave beyond cutoff (where n is the order of the filter), and nonlinear phase characteristics that lead to a nonlinear group delay. On the other hand, the Thomson filter (also referred to as the normalized Bessel filter) has a linear phase response in the passband, and an amplitude response that is not as flat as that of the Butterworth filter in the passband and stopbands. Group delay for the Thomson filter is constant up to cutoff.

In some cases, a compromise characteristic that trades off the best properties of the Butterworth and the Thomson filter is needed. The result is the class of Butterworth-Thomson filter. Its characteristics vary smoothly between the maximally flat amplitude of the Butterworth filter and the maximally flat envelope delay of the Thomson filter.

Butterworth-Thomson filter properties

In the complex frequency plane, the poles of the Butterworth-Thomson filter lie between those of the Butterworth and Thomson types, as shown in Fig. 1. The actual pole location is denoted by P, the length of the vector to the pole by R, and the angle of this pole vector by θ. Letting subscript BT represent the Butterworth-Thomson filter, subscript B the Butterworth filter, and subscript T the Thomson filter, the equation that defines the location of a Butterworth-Thomson pole can be written as:

$$P_{BT} = R_T^m \exp[-j(\theta_B - m(\theta_B - \theta_T))]$$

where m is a parameter that varies between 0 and 1. When m = 0, the Butterworth-Thomson poles are the same as those of the Butterworth filter:

$$P_{BT} = \exp(-j\theta_B) = P_B$$

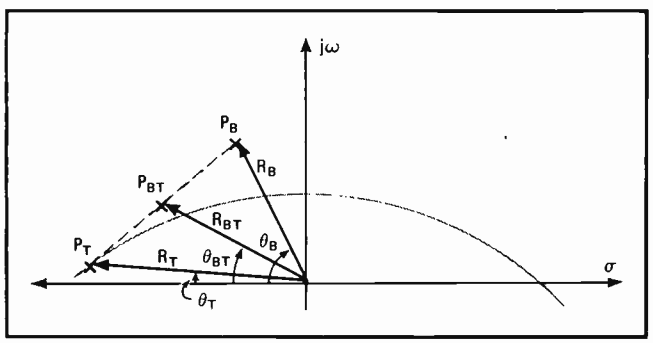
When m = 1, the Butterworth-Thomson and the Thomson poles are the same:

$$P_{BT} = R_T \exp(-j\theta_T) = P_T$$

From these equations, the pole locations, the magnitude and angle of the pole vectors, and the filter Q factor can be computed for various values of parameter m. Tables 1 through 6 list this data for m = 0, 0.2, 0.4, 0.6, 0.8, and 1 for both even and odd filter orders from 2 to 10. Data for intermediate values of parameter m can be obtained by interpolation.

From the general transfer function of the Butterworth-Thomson filter, which can be found in reference literature, both the frequency- and time-domain characteristics can be obtained. Graphs 1 and 2 relate filter gain to normalized frequency for m = 0.4 and m = 0.8, respectively. The group delay characteristics, again for m = 0.4 and m = 0.8, are drawn in Graphs 3 and 4. For any order filter, in either the frequency or time domain, the Butterworth-Thomson filter changes smoothly from the Butterworth to the Thomson characteristics, as parameter m varies from 0 to 1.

Active-filter circuits synthesize a second-order transfer function with one or more op amps and an RC net-



1. Pole locations. Butterworth-Thomson filter compromises the flat amplitude of the Butterworth filter with the flat envelope delay of the Thomson filter. Its poles (P_{BT}) are located between those (P_B) of the Butterworth filter and those (P_T) of the Thomson filter.

TABLE 1

POLE LOCATIONS FOR m = 0

Order	Real	Imaginary	Magnitude	Angle from neg. real axis (deg.)	Q factor
2	−0.70711	0.70711	1.00000	45.00000	0.70711
3	−1.00000	0.00000	1.00000	0.00000	
	−0.50000	0.86603	1.00000	60.00000	1.00000
4	−0.92388	0.38268	1.00000	22.50000	0.54120
	−0.38268	0.92388	1.00000	67.50000	1.30656
5	−1.00000	0.00000	1.00000	0.00000	
	−0.80902	0.58779	1.00000	36.00000	0.61803
	−0.30902	0.95106	1.00000	72.00000	1.61803
6	−0.96593	0.25882	1.00000	15.00000	0.51764
	−0.70711	0.70711	1.00000	45.00000	0.70711
	−0.25882	0.96593	1.00000	75.00000	1.93185
7	−1.00000	0.00000	1.00000	0.00000	
	−0.90097	0.43388	1.00000	25.71430	0.55496
	−0.62271	0.78245	1.00000	51.48570	0.80294
	−0.22252	0.97493	1.00000	77.14290	2.24698
8	−0.98079	0.19509	1.00000	11.25000	0.50980
	−0.83147	0.55557	1.00000	33.75000	0.60134
	−0.55557	0.83147	1.00000	56.25000	0.89998
	−0.19509	0.98079	1.00000	78.75000	2.56292
9	−1.00000	0.00000	1.00000	0.00000	
	−0.93969	0.34202	1.00000	20.00000	0.53209
	−0.76604	0.64279	1.00000	40.00000	0.65270
	−0.50000	0.86603	1.00000	60.00000	1.00000
	−0.17365	0.98481	1.00000	80.00000	2.87939
10	−0.98769	0.15643	1.00000	9.00000	0.50623
	−0.89101	0.45399	1.00000	27.00000	0.56116
	−0.70711	0.70711	1.00000	45.00000	0.70711
	−0.45399	0.89101	1.00000	63.00000	1.10135
	−0.15643	0.98769	1.00000	81.00000	3.19623

TABLE 2

POLE LOCATIONS FOR m = 0.2

Order	Real	Imaginary	Magnitude	Angle from neg. real axis (deg.)	Q factor
2	−0.74314	0.66913	1.00000	42.00000	0.67282
3	−0.98804	0.00000	0.98804	0.00000	
	−0.55189	0.84115	1.00604	56.73050	0.91145
4	−0.92089	0.35967	0.98863	21.33390	0.53678
	−0.43822	0.91164	1.01150	64.32650	1.15409
5	−0.98484	0.00000	0.98484	0.00000	
	−0.81940	0.55883	0.99182	34.29390	0.60521
	−0.36431	0.94842	1.01598	68.98710	1.39440
6	−0.95464	0.24348	0.98520	14.30820	0.51601
	−0.72778	0.67917	0.99546	43.02160	0.68390
	−0.31255	0.97057	1.01966	72.15020	1.63120
7	−0.98335	0.00000	0.98335	0.00000	
	−0.89756	0.41069	0.98706	24.58720	0.54986
	−0.65070	0.75798	0.99897	49.35490	0.76761
	−0.27429	0.98524	1.02271	74.44310	1.86431
8	−0.96628	0.18372	0.98359	10.76510	0.50896
	−0.83600	0.52926	0.98945	32.33720	0.59178
	−0.58822	0.81141	1.00220	54.06020	0.85188
	−0.24483	0.99562	1.02528	76.18490	2.09390
9	−0.98250	0.00000	0.98250	0.00000	
	−0.93021	0.32331	0.98480	19.16590	0.52934
	−0.77746	0.61608	0.99197	38.39430	0.63795
	−0.53590	0.85034	1.00512	57.78010	0.93779
	−0.22142	1.00334	1.02748	77.55510	2.32017
10	−0.97154	0.14743	0.98266	8.62893	0.50572
	−0.88731	0.43102	0.98646	25.90860	0.55587
	−0.72420	0.68154	0.99446	43.26170	0.68660
	−0.49204	0.87947	1.00775	60.77410	1.02406
	−0.20237	1.00930	1.02938	78.66240	2.54337

TABLE 3

POLE LOCATIONS FOR m = 0.4

Order	Real	Imaginary	Magnitude	Angle from neg. real axis (deg.)	Q factor
2	−0.77715	0.62932	1.00000	39.00000	0.64338
3	−0.97622	0.00000	0.97622	0.00000	
	−0.60258	0.81318	1.01211	53.46100	0.83981
4	−0.91747	0.33698	0.97740	20.16790	0.53266
	−0.49363	0.89617	1.02312	61.15300	1.03633
5	−0.96990	0.00000	0.96990	0.00000	
	−0.82884	0.52982	0.98371	32.58790	0.59342
	−0.42026	0.94279	1.03222	65.97430	1.22806
6	−0.94334	0.22850	0.97062	13.61640	0.51446
	−0.74738	0.65067	0.99093	41.04320	0.66294
	−0.36750	0.97258	1.03970	69.30030	1.41455
7	−0.96698	0.00000	0.96698	0.00000	
	−0.89375	0.38787	0.97429	23.46010	0.54506
	−0.67773	0.73250	0.99794	47.22410	0.73623
	−0.32766	0.99328	1.04593	71.74330	1.59604
8	−0.95191	0.17265	0.96744	10.28030	0.50816
	−0.83984	0.50312	0.97901	30.92440	0.58286
	−0.62016	0.79008	1.00440	51.87040	0.80979
	−0.29645	1.00853	1.05120	73.61980	1.77299
9	−0.96530	0.00000	0.96530	0.00000	
	−0.92061	0.30503	0.96982	18.33180	0.52673
	−0.78804	0.58929	0.98401	36.78860	0.62434
	−0.57134	0.83319	1.01026	55.56030	0.88411
	−0.27128	1.02026	1.05571	75.11010	1.94581
10	−0.95561	0.13869	0.96562	8.25786	0.50524
	−0.88324	0.40843	0.97310	24.81720	0.55087
	−0.74041	0.65560	0.98895	41.52340	0.66784
	−0.52990	0.86636	1.01557	58.54810	0.95826
	−0.25052	1.02959	1.05963	76.32480	2.11490

TABLE 4

POLE LOCATIONS FOR m = 0.6

Order	Real	Imaginary	Magnitude	Angle from neg. real axis (deg.)	Q factor
2	−0.80902	0.58779	1.00000	36.00000	0.61803
3	−0.96454	0.00000	0.96454	0.00000	
	−0.65189	0.78218	1.01822	50.19150	0.78098
4	−0.91363	0.31462	0.96629	19.00180	0.52882
	−0.54872	0.87744	1.03489	57.97950	0.94300
5	−0.95519	0.00000	0.95519	0.00000	
	−0.83734	0.50078	0.97566	30.88180	0.58260
	−0.47673	0.93409	1.04871	62.96140	1.09989
6	−0.93203	0.21388	0.95625	12.92460	0.51300
	−0.76590	0.62165	0.98643	39.06480	0.64397
	−0.42357	0.97184	1.06013	66.45050	1.25144
7	−0.95088	0.00000	0.95088	0.00000	
	−0.88954	0.36543	0.96168	22.33300	0.54055
	−0.70377	0.70606	0.99690	45.09330	0.70826
	−0.38258	0.99892	1.06968	69.04350	1.39798
8	−0.93769	0.16189	0.95156	9.79540	0.50740
	−0.84300	0.47717	0.96868	29.51160	0.57454
	−0.65132	0.76748	1.00660	49.68070	0.77274
	−0.34991	1.01938	1.07777	71.05470	1.54005
9	−0.94841	0.00000	0.94841	0.00000	
	−0.91089	0.28716	0.95508	17.49770	0.52426
	−0.79779	0.56242	0.97611	35.18290	0.61176
	−0.60627	0.81458	1.01543	53.34040	0.83744
	−0.32320	1.03545	1.08472	72.66520	1.67811
10	−0.93990	0.13020	0.94887	7.88679	0.50477
	−0.87879	0.38623	0.95992	23.72580	0.54616
	−0.75575	0.62934	0.98348	39.78510	0.65066
	−0.56752	0.85167	1.02344	56.32220	0.90168
	−0.30089	1.04844	1.09076	73.98720	1.81256

work. First-order transfer functions, on the other hand, are realized with a simple passive resistor-capacitor combination, so that an active third-order filter is actually an active second-order circuit cascaded with a passive first-order RC network.

To realize high-order filters, second-order and/or third-order filter sections are cascaded. If the filter order is even, only second-order sections are used. For example, a sixth-order filter is obtained when three second-order sections are cascaded. Odd-order filters are implemented by cascading a third-order section with one or more second-order sections. For a seventh-order filter, therefore, one third-order section is cascaded with two second-order sections.

Different circuits can be used to realize the basic second-order or third-order active filter section. Two popular configurations, which require only one op amp per section, are the positive-feedback and the multiple-

TABLE 5

POLE LOCATIONS FOR m = 0.8

Order	Real	Imaginary	Magnitude	Angle from neg. real axis (deg.)	Q factor
2	−0.83867	0.54464	1.00000	33.00000	0.59618
3	−0.95300	0.00000	0.95300	0.00000	
	−0.69963	0.74822	1.02436	46.92200	0.73207
4	−0.90939	0.29260	0.95531	17.83570	0.52524
	−0.60331	0.85544	1.04678	54.80600	0.86753
5	−0.94071	0.00000	0.94071	0.00000	
	−0.84491	0.47173	0.96768	29.17570	0.57265
	−0.53356	0.92225	1.06547	59.94860	0.99845
6	−0.92071	0.19962	0.94210	12.23290	0.51162
	−0.78333	0.59213	0.98195	37.08630	0.62678
	−0.48063	0.96824	1.08097	63.60070	1.12454
7	−0.93505	0.00000	0.93505	0.00000	
	−0.88496	0.34336	0.94923	21.20590	0.53632
	−0.72878	0.67871	0.99588	42.96240	0.68325
	−0.43895	1.00204	1.09397	66.34370	1.24611
8	−0.92361	0.15142	0.93595	9.31054	0.50668
	−0.84549	0.45143	0.95846	28.09880	0.56681
	−0.68166	0.74367	1.00881	47.49090	0.73997
	−0.40517	1.02805	1.10501	68.48960	1.36362
9	−0.93181	0.00000	0.93181	0.00000	
	−0.90106	0.26971	0.94056	16.66360	0.52192
	−0.80671	0.53551	0.96827	33.57720	0.60014
	−0.64063	0.79453	1.02063	51.12050	0.79658
	−0.37716	1.04877	1.11453	70.22020	1.47752
10	−0.92441	0.12196	0.93242	7.51572	0.50433
	−0.87399	0.36442	0.94692	22.63440	0.54172
	−0.77020	0.60276	0.97803	38.04680	0.63491
	−0.60482	0.83542	1.03137	54.09630	0.85262
	−0.35349	1.06572	1.12281	71.64960	1.58817

TABLE 6

POLE LOCATIONS FOR m = 1

Order	Real	Imaginary	Magnitude	Angle from neg. real axis (deg.)	Q factor
2	−0.86603	0.50000	1.00000	30.00000	0.57735
3	−0.94160	0.00000	0.94160	0.00000	
	−0.74564	0.71137	1.03054	43.65250	0.69105
4	−0.90476	0.27092	0.94445	16.66970	0.52193
	−0.65721	0.83016	1.05882	51.63250	0.80554
5	−0.92644	0.00000	0.92644	0.00000	
	−0.85155	0.44272	0.95976	27.46960	0.56354
	−0.59059	0.90720	1.08250	56.93570	0.91646
6	−0.90939	0.18570	0.92816	11.54110	0.51032
	−0.79965	0.56217	0.97749	35.10790	0.61119
	−0.53855	0.96169	1.10222	60.75080	1.02331
7	−0.91949	0.00000	0.91949	0.00000	
	−0.88000	0.32167	0.93695	20.07870	0.53236
	−0.75274	0.65047	0.99485	40.83160	0.66082
	−0.49669	1.00251	1.11881	63.64390	1.12626
8	−0.90968	0.14124	0.92058	8.82567	0.50599
	−0.84733	0.42590	0.94834	26.68610	0.55961
	−0.71114	0.71865	1.01103	45.30110	0.71085
	−0.46217	1.03439	1.13294	65.92450	1.22567
9	−0.91550	0.00000	0.91550	0.00000	
	−0.89113	0.25266	0.92626	15.82950	0.51971
	−0.81480	0.50858	0.96050	31.97150	0.58941
	−0.67436	0.77305	1.02586	48.90070	0.76061
	−0.43314	1.06007	1.14515	67.77530	1.32191
10	−0.90913	0.11396	0.91625	7.14465	0.50391
	−0.86885	0.34300	0.93410	21.54300	0.53755
	−0.78377	0.57591	0.97261	36.30850	0.62047
	−0.64175	0.81758	1.03937	51.87030	0.80979
	−0.40832	1.08127	1.15580	69.31190	1.41531

feedback active filters. The first uses the op amp in its noninverting unity-gain mode, while the second uses it as an infinite-gain device.

The cutoff frequency and the Q factor of the positive-feedback filter are more sensitive to passive component tolerances and amplifier gain variations than the multiple-feedback filter. However, for the same cutoff frequency, the positive-feedback version does not demand as much bandwidth from the amplifier. Additionally, both the second- and third-order positive-feedback filters require one fewer resistor than the same-order multiple-feedback filters.

Low-pass Butterworth-Thomson filters

A second-order low-pass filter section using a unity-gain amplifier and another using an infinite-gain amplifier are shown in Fig. 2a and 2b, respectively. The circuits in Fig. 2c and 2d are the comparable third-order low-pass filter sections.

The transfer function of the second-order low-pass positive-feedback filter of Fig. 2a can be written as:

$$G(s) = 1/[s^2C_1C_2R_1R_2 + sC_2(R_1+R_2) + 1]$$

where s is the Laplace transform variable. For the second-order low-pass multiple-feedback filter of Fig. 2b:

$$G(s) = (-R_3/R_1)/[s^2R_2R_3C_1C_2 + sC_2(R_2+R_3+R_2R_3/R_1) + 1]$$

For the third-order positive-feedback filter of Fig. 2c:

$$G(s) = 1/[s^3C_1C_2C_3R_1R_2R_3 + s^2(C_2C_3R_3(R_1+R_2)+C_1C_3R_1(R_2+R_3)) + s(C_3(R_1+R_2+R_3)+C_1R_1) + 1]$$

For the third-order multiple-feedback filter of Fig. 2d:

$$G(s) = 1/[s^3R_1R_2R_3C_1C_2C_3 + s^2((R_2R_3+R_3R_4+R_2R_4)(R_1C_1C_3/R_4)+(R_1+R_2)R_3C_1C_3) + s((R_3R_4+R_2R_3+R_2R_4+R_1R_3+R_1R_4)(C_3/R_4)+(R_1R_2C_1/R_4)) + (R_1\ \vartheta\ R\ 2)/R_4]$$

Tables 7 and 8 give the normalized capacitor values that satisfy these transfer functions when all the resistors have the same value. Table 7 lists the capacitances for the positive-feedback Butterworth-Thomson filter for m = 0.2, 0.4, 0.6, and 0.8 for both even and odd filter orders from 2 to 10. Table 8 duplicates this data, but for the multiple-feedback Butterworth-Thomson filter. Interpolation yields the normalized capacitor values for intermediate values of parameter m.

How to use the tables and graphs

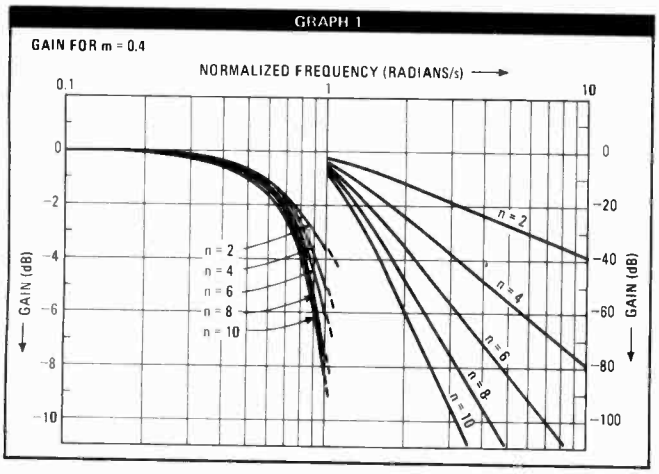
Now that all the data needed to put an active Butterworth-Thomson filter together is at hand, a general design procedure can be outlined. Of course, the filter characteristics that will satisfy the specifications must first be selected. This is done by choosing the best value of parameter m, as well as the necessary filter order, from Tables 1 through 6 and Graphs 1 through 4. (The desired filter operating frequency is set equal to the normalized frequency of 1 radian/second.)

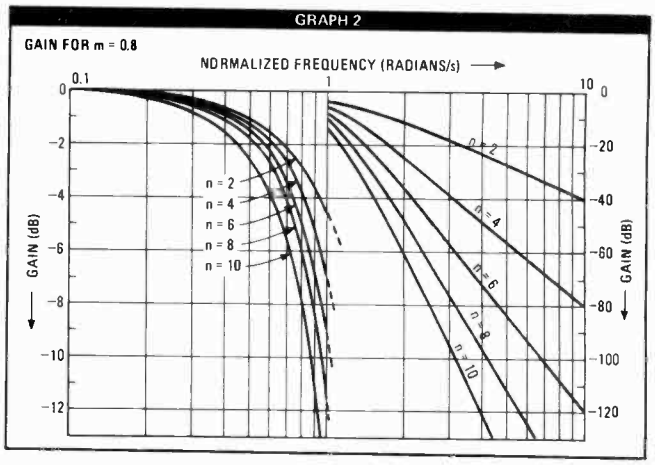
If a low-pass function is required, the first steps are to find the proper normalized capacitor values for each filter section from Table 7 or 8, depending on the circuit preferred, and then choose a convenient value of resistance. (A different resistance value may be assigned for each section.) Actual capacitor values (C_a) are found by a simple division:

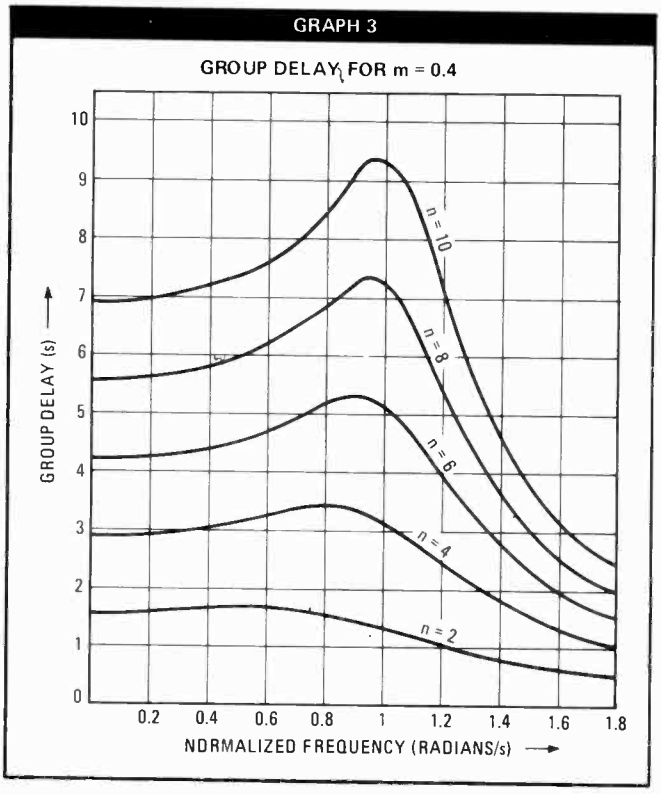
$$C_a = C_n/\omega_o R$$

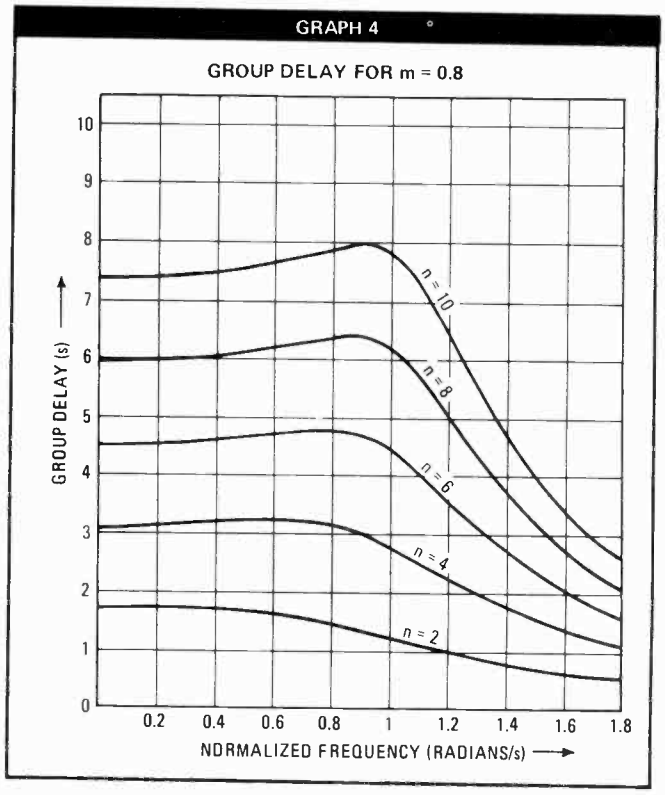
where C_n is the normalized capacitor value, ω_o is the actual filter operating frequency, and R is the resistance value chosen for a given section.

High-pass filter functions synthesized with the positive-feedback circuit can also be designed from the normalized capacitor values given for low-pass filters in Table 7. Since the positions of resistors and capacitors cannot be interchanged for the multiple-feedback cir-









cuit, Table 8 cannot be used for this high-pass filter. Fig. 3 shows the two active filter circuits that correspond to the low-pass filters of Fig. 2a and 2c. The second-order high-pass positive-feedback filter is illustrated in Fig. 3a, and the third-order version of this filter is drawn in Fig. 3b.

Designing the filter

The design procedure for an active high-pass Butterworth-Thomson filter is similar to the one for a low-pass filter. After the correct value for parameter m and the desired filter order have been selected, the normalized capacitor values are picked from Table 7. Normalized resistor values are then computed:

$R_n = 1/C_n$

A convenient value is next chosen for capacitor C; a different value of C may be chosen for each filter section. The actual resistor values (R_a) can then be found from the normalized resistor values:

$R_a = R_n/\omega_o C$

where ω_o is the actual filter operating frequency.

A few specific examples will clarify the general procedures just outlined.

A fourth-order multiple-feedback low-pass Butterworth-Thomson filter is needed with m = 0.4 and ω_o = 10,000 radians/second. From table 8, the normalized capacitor values can be obtained. For the first filter section:

$C_{1n} = 2.8812$ and $C_{2n} = 0.3633$

For the second section:

$C_{1n} = 1.4147$ and $C_{2n} = 0.6753$

Setting the resistors for both sections equal to 1,000 ohms, the denormalizing conversion factor becomes:

$\omega_o R = 10^4(10^3) = 10^7$

The actual capacitor values can then be computed. For the first section:

$C_1 = 2.8812/10^7 = 0.28812$ microfarad

$C_2 = 0.3633/10^7 = 0.3633\mu F$

And for the second section:

$C_1 = 1.4147/10^7 = 0.14147\ \mu F$

$C_2 = 0.6753/10^7 = 0.06753\ \mu F$

The component values needed to build the filter are now known.

A fifth-order positive-feedback high-pass Butterworth-Thomson filter must be designed for m = 0.2 and ω_o = 1,000 radians/second. The normalized capacitor values are found in Table 7. For section 1:

$C_{1n} = 1.3369$, $C_{2n} = 1.7467$, and $C_{3n} = 0.4276$

For section 2:

$C_{1n} = 2.7449$ and $C_{2n} = 0.3529$

The normalized resistor values for section 1 become:

$R_{1n} = 1/1.3669 = 0.732$

$R_{2n} = 1/1.7467 = 0.573$

$R_{3n} = 1/0.4276 = 2.34$

And for section 2:

$R_{1n} = 1/2.7449 = 0.365$

$R_{2n} = 1/0.3529 = 2.84$

Choosing a convenient value for capacitor C—let C = 0.1 μF = 10^{-7} farads—allows the denormalizing conversion factor for the resistances to be calculated:

$\omega_o C = 10^3(10^{-7}) = 10^{-4}$

The actual resistor values for section 1 can then be readily determined:

$R_1 = 0.732/10^{-4} = 7.32$ kilohms

$R_2 = 0.573/10^{-4} = 5.73$ kilohms

$R_3 = 2.34/10^{-4} = 23.4$ kilohms

And for section 2:

$R_1 = 0.365/10^{-4} = 3.65$ kilohms

$R_2 = 2.84/10^{-4} = 28.4$ kilohms

The filter can now be assembled from the computed component values.

Practical considerations

For the most part, literature on active filter design supposes the op amp to be ideal—that is, it is assumed to have infinite gain, infinite input impedance, and zero output impedance. But when operating frequency becomes high and filter Q large, the finite gain-bandwidth product of an op amp, as well as its sensitivity parameters, can no longer be neglected.

A common assumption is to consider the actual op amp gain-bandwidth product, f_a, to be at least an order of magnitude larger than the desired filter cutoff frequency, f_o. However, for a second-order positive-feedback filter:

$$f_a/f_o = Q/(1 - f_{oa}/f_o) \quad (1)$$

where Q is the desired filter Q, and f_{oa} is the actual filter cutoff frequency. This frequency ratio can also be expressed solely in terms of filter Q:

$$f_a/f_o = Q/(Q_a/Q - 1) \quad (2)$$

where Q_a is the actual Q. The same relationships can be developed for the second-order multiple feedback filter, which uses an infinite-gain as opposed to a unity-gain amplifier:

$$f_a/f_o = 1.5Q/(1 - f_{oa}/f_o) = 1.5Q/(Q_a/Q - 1)$$

Suppose that the actual cutoff frequency, f_{oa}, must deviate less than 5% from the desired cutoff frequency, f_o, and that actual filter Q, Q_a, must be within 2% of the desired filter Q. Using Eq. 1 yields:

f_a/f_o must be greater than $Q/0.05 = 20Q$

or, from Eq. 2:

f_a/f_o must be greater than $Q/0.02 = 50Q$

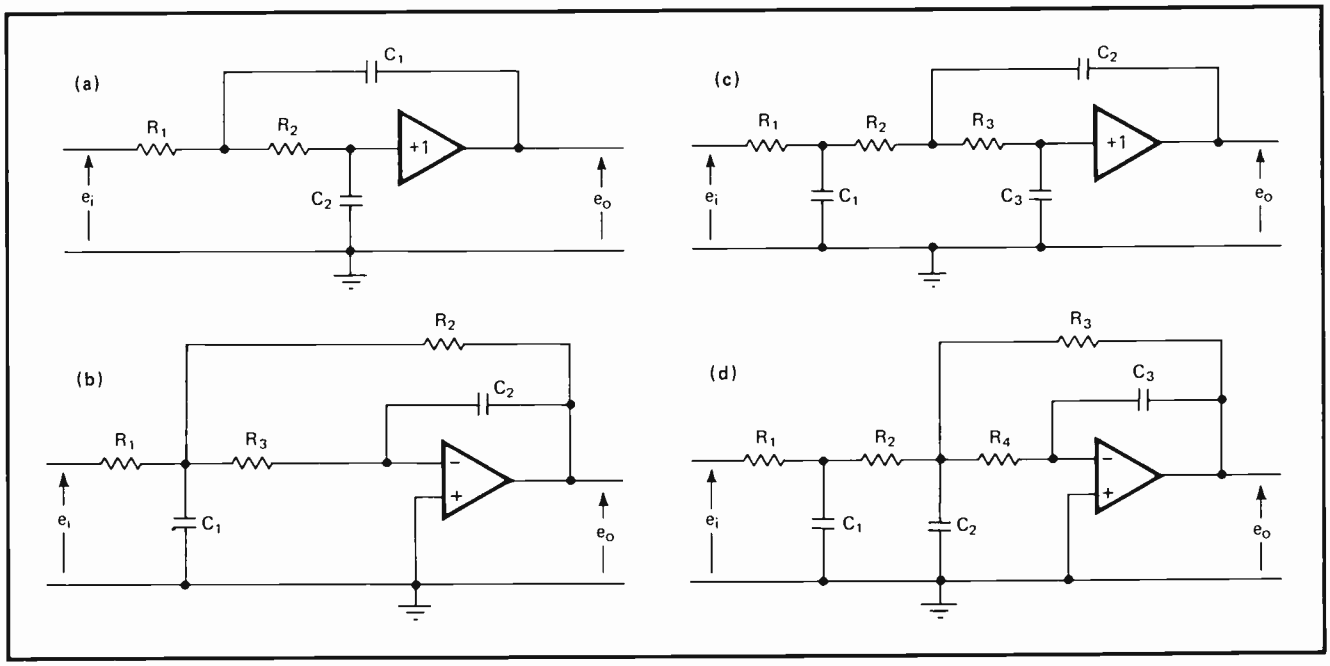
Since the latter condition is the more stringent, it is the one that must be obeyed.

If a fourth-order filter, with m = 0.2 and f_o = 1,000 hertz, is being designed, Table 2 indicates that Q = 0.53678 for section 1 and Q = 1.15409 for section 2. The gain-bandwidth product of the amplifier for the second section must satisfy the condition:

f_a must be greater than $50Qf_o = 5(1.15409)(10^3)$

f_a must be greater than 57.7045 kilohertz

to achieve less than 2% accuracy in the Q of the filter. A multiple-feedback filter would require even more amplifier bandwidth, because:



2. Low-pass filters. Second-order low-pass filter can be implemented with unity-gain amplifier in positive-feedback circuit (a), or with infinite-gain amplifier in multiple-feedback circuit (b). Third-order filters (c) and (d) are second-order filters that have been cascaded with first-order RC network at input end. Tables 7 and 8 give normalized capacitor values for these low-pass filters having orders up to 10.

TABLE 7

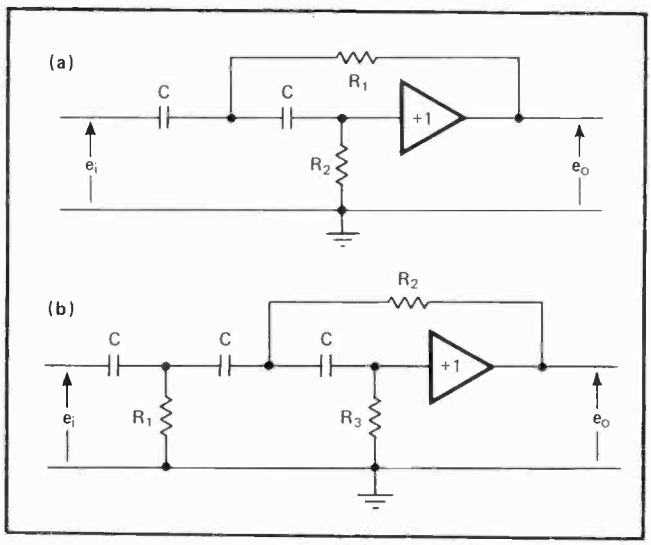
NORMALIZED CAPACITOR VALUES USING UNITY-GAIN AMPLIFIERS

Order	Section	m = 0.2			m = 0.4			m = 0.6			m = 0.8		
		C(1)	C(2)	C(3)	C(1)	C(2)	C(3)	C(1)	C(2)	C(3)	C(1)	C(2)	C(3)
2	1	1.3456	0.7431		1.2868	0.7771		1.2361	0.8090		1.1924	0.8387	
3	1	1.3950	3.2775	0.2190	1.3963	3.2851	0.2185	1.3963	3.2853	0.2185	1.3951	3.2779	0.2189
4	1	1.0859	0.9422		1.0900	0.9604		1.0945	0.9785		1.0996	0.9965	
	2	2.2819	0.4283		2.0258	0.4716		1.8224	0.5123		1.6575	0.5506	
5	1	1.3669	1.7467	0.4276	1.3796	1.7651	0.4234	1.3922	1.7841	0.4192	1.4048	1.8036	0.4150
	2	2.7449	0.3529		2.3795	0.3944		2.0976	0.4335		1.8742	0.4700	
6	1	1.0475	0.9835		1.0601	1.0013		1.0729	1.0193		1.0861	1.0374	
	2	1.3741	0.7344		1.3380	0.7611		1.3057	0.7871		1.2766	0.8124	
	3	3.1995	0.3006		2.7211	0.3400		2.3609	0.3769		2.0806	0.4113	
7	1	1.3546	1.5423	0.4920	1.3726	1.5601	0.4860	1.3909	1.5791	0.4799	1.4094	1.5992	0.4738
	2	1.5368	0.6520		1.4755	0.6805		1.4209	0.7081		1.3722	0.7348	
	3	3.6458	0.2622		3.0519	0.2995		2.6138	0.3344		2.2782	0.3668	
8	1	1.0349	0.9988		1.0505	1.0171		1.0664	1.0356		1.0827	1.0544	
	2	1.1962	0.8539		1.1907	0.8762		1.1862	0.8984		1.1827	0.9204	
	3	1.7000	0.5856		1.6125	0.6147		1.5353	0.6428		1.4670	0.6698	
	4	4.0845	0.2329		3.3733	0.2683		2.8578	0.3012		2.4681	0.3318	
9	1	1.3487	1.4715	0.5197	1.3696	1.4889	0.5127	1.3908	1.5077	0.5056	1.4124	1.5279	0.4984
	2	1.2862	0.7901		1.2690	0.8139		1.2535	0.8373		1.2396	0.8604	
	3	1.8660	0.5305		1.7503	0.5598		1.6494	0.5880		1.5610	0.6150	
	4	4.5162	0.2097		3.6863	0.2434		3.0941	0.2747		2.6514	0.3036	
10	1	1.0293	1.0061		1.0465	1.0249		1.0639	1.0439		1.0818	1.0633	
	2	1.1270	0.9118		1.1322	0.9327		1.1379	0.9537		1.1442	0.9747	
	3	1.3808	0.7323		1.3506	0.7570		1.3232	0.7814		1.2984	0.8052	
	4	2.0324	0.4845		1.8871	0.5138		1.7621	0.5418		1.6534	0.5686	
	5	4.9415	0.1910		3.9918	0.2231		3.3235	0.2529		2.8289	0.2804	

TABLE 8

NORMALIZED CAPACITOR VALUES USING INFINITE-GAIN AMPLIFIERS

Order	Section	m = 0.2			m = 0.4			m = 0.6			m = 0.8		
		C(1)	C(2)	C(3)	C(1)	C(2)	C(3)	C(1)	C(2)	C(3)	C(1)	C(2)	C(3)
2	1	2.2294	0.4485		2.3314	0.4289		2.4271	0.4120		2.5160	0.3975	
3	1	1.3495	5.2591	0.1405	1.3423	5.1960	0.1419	1.3337	5.1220	0.1436	1.3236	5.0383	0.1457
4	1	2.8266	0.3620		2.8812	0.3633		2.9355	0.3648		2.9894	0.3665	
	2	1.2850	0.7606		1.4147	0.6753		1.5370	0.6075		1.6518	0.5525	
5	1	1.2640	2.9081	0.2771	1.2713	2.9226	0.2757	1.2785	2.9372	0.2742	1.2857	2.9520	0.2728
	2	1.0588	0.9150		1.1833	0.7932		1.3004	0.6992		1.4100	0.6247	
6	1	2.9506	0.3492		3.0039	0.3534		3.0578	0.3576		3.1121	0.3620	
	2	2.2033	0.4580		2.2833	0.4460		2.3613	0.4352		2.4372	0.4255	
	3	0.9018	1.0665		1.0199	0.9070		1.1306	0.7870		1.2340	0.6935	
7	1	1.2297	2.7070	0.3202	1.2436	2.6252	0.3174	1.2578	2.6444	0.3146	1.2722	2.6647	0.3117
	2	1.9561	0.5123		2.0416	0.4918		2.1244	0.4736		2.2045	0.4574	
	3	0.7867	1.2153		0.8986	1.0173		1.0031	0.8713		1.1004	0.7594	
8	1	2.9964	0.3450		3.0512	0.3502		3.1067	0.3555		3.1631	0.3609	
	2	2.5618	0.3987		2.6287	0.3969		2.6952	0.3954		2.7611	0.3942	
	3	1.7569	0.5667		1.8442	0.5375		1.9284	0.5118		2.0094	0.4890	
	4	0.6987	1.3615		0.8048	1.1244		0.9037	0.9526		0.9955	0.8227	
9	1	1.2138	2.5053	0.3388	1.2311	2.5240	0.3353	1.2487	2.5440	0.3318	1.2667	2.5654	0.3282
	2	2.3703	0.4287		2.4416	0.4230		2.5120	0.4178		2.5813	0.4132	
	3	1.5914	0.6220		1.6794	0.5834		1.7640	0.5498		1.8450	0.5203	
	4	0.6292	1.5054		0.7302	1.2288		0.8241	1.0314		0.9109	0.8838	
10	1	3.0184	0.3431		3.0746	0.3488		3.1317	0.3546		3.1898	0.3606	
	2	2.7355	0.3757		2.7982	0.3774		2.8611	0.3793		2.9241	0.3814	
	3	2.1969	0.4603		2.2711	0.4502		2.3441	0.4411		2.4156	0.4328	
	4	1.4535	0.6775		1.5414	0.6290		1.6255	0.5874		1.7058	0.5511	
	5	0.5729	1.6472		0.6693	1.3306		0.7587	1.1078		0.8412	0.9430	



f_a must be greater than $1.5(50)Qf_o$
f_a must be greater than $1.5(50)(1.15409)(10^3)$
f_a must be greater than 86.5568 kHz

The infinite-gain amplifier, however, has lower sensitivity parameters than the unity-gain amplifier. □

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3. High-pass filters. Circuits (a) and (b) correspond to low-pass configurations on Fig. 2a and 2c, but provide high-pass function. Reciprocals of normalized capacitor values in Table 7 are used to determine resistor values for these high-pass filters.

Instrumentation amplifier conditions computer inputs

Two-stage amplifier detects more than 100 multiplexed signals at computer-speed scanning rates with minimum noise over wide frequency range; signal levels can range from microvolts to volts

by Thomas C. Lyerly, *IBM General Systems Division, Boca Raton, Fla.*

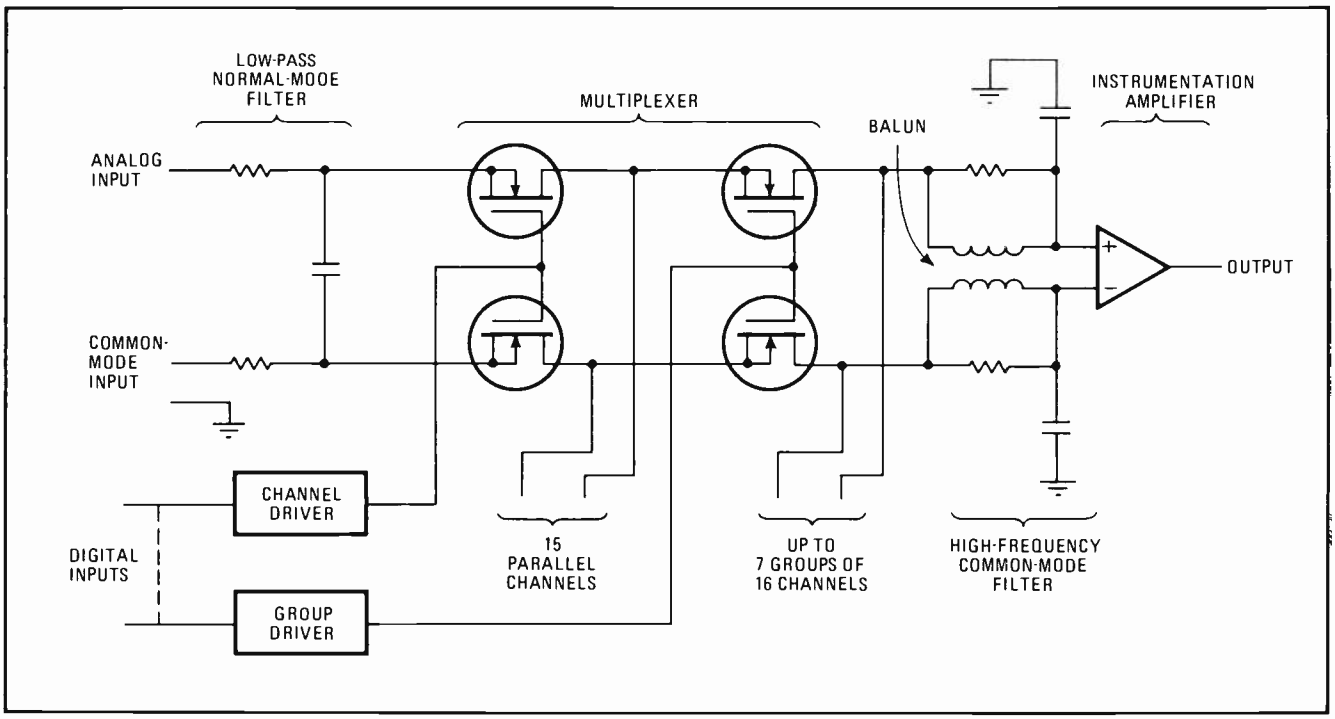
☐ Since the job of data gathering has become so complex that computers are needed to process measurement information, increasingly stringent performance requirements are being placed on the instrumentation amplifier. A single instrumentation amplifier must frequently accept more than 100 multiplexed signals with levels ranging from a few microvolts to several volts. The amplifier must also reject unwanted noise signals from dc to hundreds of megahertz, as well as provide a noise-free, properly scaled, single-ended output signal that can be sampled quickly for processing.

Precision low-level signal conditioning can be achieved with a two-stage amplifier that employs cascode transistor pairs, degenerative feedback, and balanced frequency compensation to provide exceptional gain-bandwidth performance without gain-adjustment potentiometers. Even in noisy environments, this amplifier can detect microvolt signals at high scanning rates. It can also be adapted for programable gain selection.

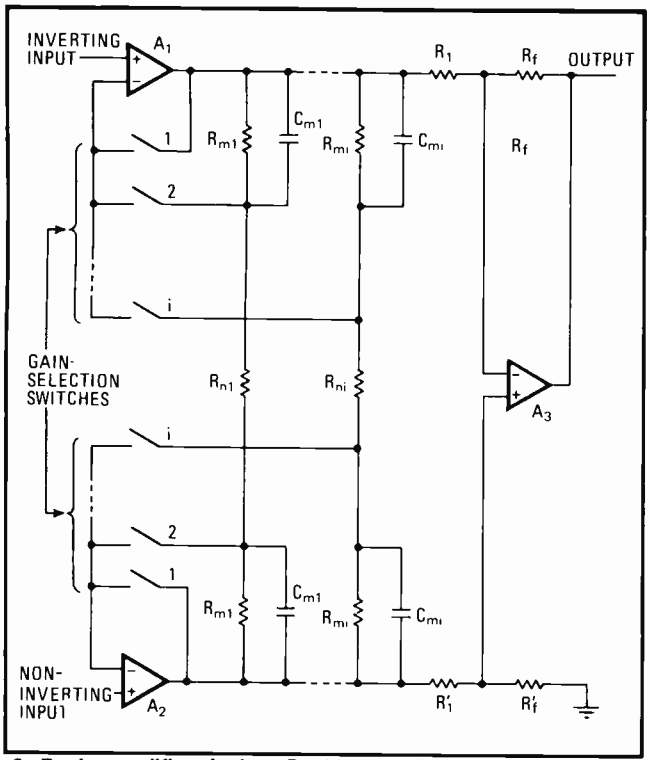
The environment for the precision amplifier is the computer analog input subsystem, such as the typical one shown in Fig. 1 for the IBM System/7 computer. As many as 128 analog input signals may be connected through single-pole low-pass filters to the multiplexer, which is made up of p-channel MOSFET switches. The multiplexer can handle up to eight parallel groups of signals, with each group consisting of up to 16 parallel channels.

The differential output of the multiplexer is connected to an instrumentation amplifier through a balun transformer that serves as a high-frequency noise filter for the amplifier. Multiplexed analog input signals must be accurately processed by the amplifer at scanning rates as fast as 20 kilohertz without any adverse effects from noise sources that are both external and internal to the analog input subsystem.

External noise may be separated into two types—common-mode, and normal- or differential-mode signals. Differential-mode noise is the easier to reject. It can be filtered by passive low-pass networks located at



1. The environment. Analog input computer subsystem challenges the instrumentation amplifier. Data is filtered before being multiplexed to eliminate normal- or differential-mode noise. Balun transformer acts as high-frequency common-mode noise filter for the amplifier.



2. Basic amplifier design. Double-amplifier input eases demands on individual amplifiers A_1 and A_2. Amplifier A_3 rejects unwanted common-mode noise signals by subtracting balanced common-mode signals from A_1 and A_2.

the multiplexer inputs, as shown in Fig. 1, since a given channel is generally sampled at a rate that is much slower than the speed at which the amplifier scans the channels.

Common-mode noise is more difficult to reject because low-frequency common-mode filtering reduces the multiplexer's ac common-mode rejection ratio, while increasing its common-mode settling time. For the analog input subsystem to operate at fast multiplexer-scanning rates, the instrumentation amplifier must be able to reject common-mode noise over a large bandwidth. Therefore, a balun transformer is placed at the amplifier input as a high-frequency common-mode filter to reject the common-mode noise beyond the bandwidth of a practical amplifier.

(This noise is filtered to prevent the amplifier from rectifying rf noise on the input lines and effectively producing dc offset errors. The balun transformer of Fig. 1 is a low-pass common-mode filter with a bandwidth of approximately 5 megahertz.)

Noise within the analog input subsystem, which takes the form of capacitively coupled noise signals and switching transients, is primarily caused by the multiplexer because of the device capacitance of the MOSFET switches. This internal noise source appears to the amplifier to be primarily common-mode noise as a result of the balanced design of the multiplexer and the low-pass input filter.

Configuration outline

An instrumentation amplifier that provides excellent rejection of unwanted common-mode noise is sketched in Fig. 2. The circuit also offers good gain-bandwidth characteristics and can be adapted for programable gain selection.

Amplifiers A_1 and A_2 provide the desired input characteristics and signal ranging. A third amplifier, A_3, acts as an inverting unity-gain device for differential inputs and operates as a precision broad-bandwidth subtractor for unwanted common-mode signals. To reject common-mode signals over a large bandwidth. A_1 and A_2 must perform as broadband unity-gain amplifiers, generating balanced common-mode signals for subtractor amplifier A_3.

The common-mode rejection ratio of the over-all amplifier can be expressed as:

$$\text{CMRR} = (R_f/R_1)(1+2R_m/R_n)/[(1/\text{CMRR}_1 \pm 1/\text{CMRR}_2)(1+2R_m/R_n)(R_f/R_1) + (R_f/\text{CMRR}_3(R_1+R_f) + R_f/(R_1+R_f) - R_f'/(R_1'+R_f'))/R_1'(R_1'+R_f')]$$

where CMRR_1, CMRR_2, and CMRR_3 are the individual common-mode rejection ratios of amplifiers A_1, A_2, and A_3, respectively.

Other common-mode input errors, not included in this equation, are caused by the voltage-divider effect between the source impedance of each analog input line and the common-mode input impedance of its amplifier. To prevent common-mode signals from being converted into differential signals from source imbalance at the input of the over-all amplifier, amplifiers A_1 and A_2 must maintain a high common-mode input impedance over a large bandwidth.

The high impedance of these two amplifiers also helps the over-all amplifier to reject the transients generated when the multiplexer channels are switched. These transients are caused by common-mode voltages, sometimes as high as 10 volts, that are switched into the instrumentation amplifier inputs at rates that can approach several hundred volts per microsecond.

The first stage

A first-stage design that satisfies the tough input performance requirements is illustrated in Fig. 3. Basically, the circuit attempts to eliminate amplifier input errors caused by offset voltage, bias current, offset-voltage drift, offset-current drift, and input impedance.

Input offset voltage can be reduced to less than 2 microvolts with the nonlinear potentiometer network of resistors R_1, R_2, and R_3 and the voltage divider set up by resistors R_4 and R_5. The input-offset voltage drift with temperature is also low because the difference between the base-emitter voltage drops of matched input transistors Q_1 and Q_2 is nearly zero.

Additionally, input bias current can be adjusted to less than 1 nanoampere by parallel potentiometers R_6 and R_7, which are driven by the high-impedance constant-current source, consisting of cascode transistors Q_3 and Q_4 and resistor R_8. The potentiometers are also driven by the common-mode input voltage through a feedback network in the emitter circuit of the Q_1-Q_2 input transistor pair. The network, made up of transistors Q_5, Q_6, and Q_7 and resistor R_9, supplies a constant voltage for biasing resistors R_{10} and R_{11} that is independent of the common-mode input voltage.

The input-impedance component of the amplifier from the feedback bias network is several thousand

megohms. Therefore, this feedback circuit provides a stable bias current without reducing the input impedance of the amplifier. A heated-substrate matched-input transistor pair can further improve the bias current, the offset-current drift, and the offset-voltage drift of the amplifier.

To increase the amplifier's common-mode input impedance, FETs Q_8 and Q_9 are connected in a cascode configuration to feed the common-mode emitter voltage of transistors Q_1 and Q_2 back to their collectors. The feedback reduces the effective input capacitance, but increases the effective input resistance between the base and collector of both input transistors. The impedance in the emitter loop of the Q_1-Q_2 input pair is also increased by a cascode pair, Q_{10} and Q_{11}, along with resistor R_{12}, in the emitter-current source.

The first-stage design can provide a common-mode input resistance of more than 2,000 megohms and an input capacitance of no more than a few tenths of a picofarad. It also offers a good common-mode rejection ratio, as well as power-supply rejection ratio because of the high drain output impedance of the FET cascode circuits. (Voltages V_1 and V_2 are zener-stabilized levels.)

The second stage

Performance requirements for the second stage are determined primarily by the programable signal ranging and gain-bandwidth requirements of the over-all instrumentation amplifier. An ideal amplifier has an infinite open-loop gain so that its closed-loop voltage gain is determined only by external resistive networks. However, a practical amplifier's gain accuracy decreases for increasing values of closed-loop gain because it has a finite open-loop gain. The closed-loop gain for the practical amplifier of Fig. 2 can be written as:

$$CLG = (1+2R_m/R_n)(R_f/R_1)[1/(1+1/A)(1+2R_m/R_n))][1/(1+(R_1+R_f)/AR_1)]$$

where A represents open-loop gain:

$$A = A_1 = A_2 = A_3$$

Instrumentation amplifiers with large closed-loop gains usually require gain-adjustment potentiometers if a high degree of gain accuracy must be maintained. However, a second-stage design with sufficient gain can eliminate the need for potentiometers without degrading gain accuracy. A schematic of a high-gain second stage is shown in Fig. 4.

The dc gain of the stage is directly proportional to the impedance at the drain terminal of FET Q_1. A high-impedance node is developed at point A because the Q_1-Q_2 cascode pair drives the Q_3-Q_4 cascode pair and FET Q_5 is connected as a source-follower. The dc resistance from node A to ground may be as high as 500 megohms, depending on the quiescent current of the cascode pairs and the resistance in the emitter circuits of transistors Q_2 and Q_4.

Cascading the stages

The circuit permits voltage gains in excess of several million to be achieved with a single stage. To make the gain of the stage less sensitive to changes in transistor parameters, emitter degeneration is provided by the resistors labeled R_E so that the voltage gain is approximately equal to the ratio of the resistance of high-impedance node A and the value of resistor R_E.

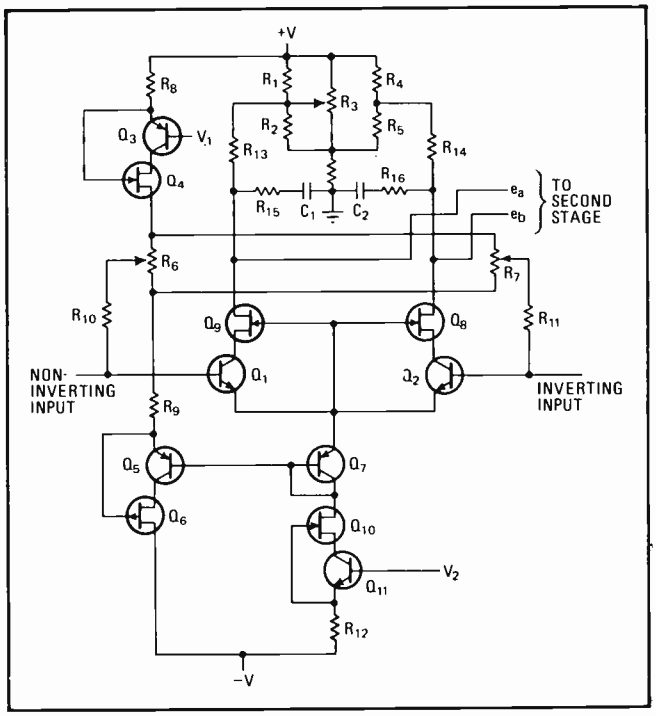
When the first- and second-stage designs are cascaded, they form a differential amplifier with a stable and well-defined open-loop dc voltage gain that can exceed 140 decibels. Since the open-loop gain is very large, the errors in the closed-loop gain caused by a finite open-loop gain are reduced to a negligible level. Therefore, gain-adjustment potentiometers are not required, and the closed-loop gain of the instrumentation amplifier can be established by resistive networks alone.

To satisfy the fast sampling-rate requirements of the analog-input subsystem, the settling time of the amplifier must be minimized. Settling time is determined by both bandwidth and slew rate, which is a measure of the rate at which the amplifier output can change.

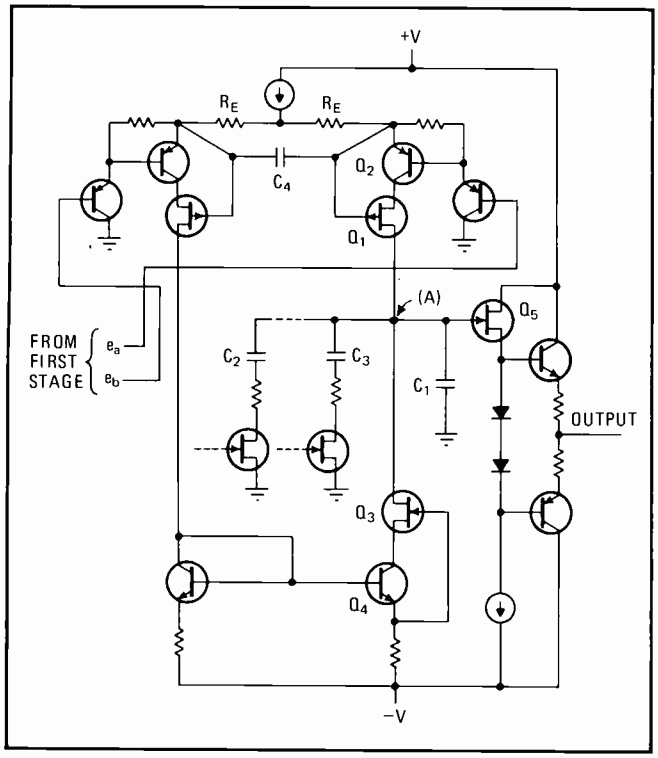
Slew-rate limiting

Slew rate is limited in feedback amplifiers when the maximum output rate of change that is fed back to the inverting input is less than the rate of change at the noninverting input. Under these conditions, a large differential error is produced across the amplifier inputs. The differential input impedance drops while the amplifier is slew-rate limiting and may be further reduced if the input step voltage exceeds the amplifier differential breakdown voltage.

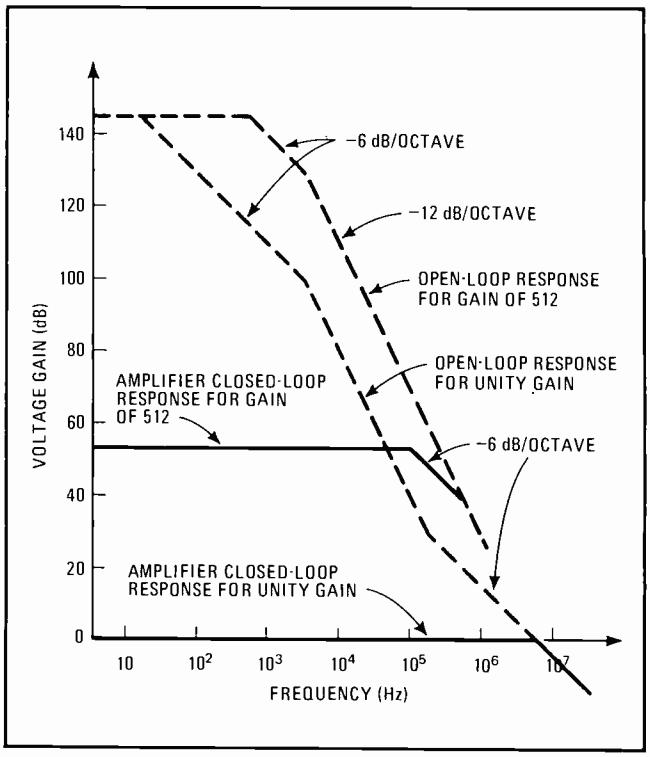
The low input impedance that occurs during slew rate limiting can produce large errors if low-pass filters with long recovery time constants are associated with the multiplexer, because charge is transferred from the filter capacitors to the amplifier inputs. To minimize this error, the amplifier must have a fast slew rate, as well as



3. First stage. Differential input amplifier stage almost zeroes out errors caused by offset voltage, offset-voltage drift, bias current, offset-current drift, and input impedance. The circuit, which has matched input transistors, Q_1 and Q_2, offers a high common-mode input resistance, but it holds input capacitance to a fraction of a picofarad. Cascode transistor pairs act as constant-current sources.



4. Second stage. Since this stage can attain voltage gains of several million without losing gain accuracy, gain-adjustment potentiometers are not needed. Circuit gain approximately equals the resistance ratio of high-impedance node A and resistor R_E.



5. Response curves. Cascaded first and second stages result in amplifier that maintains its unity-gain bandwidth of almost 10 megahertz over wide range of closed-loop gains. For instance, the upper frequency breakpoint is 125 kilohertz for a closed-loop gain of 512.

a relatively high open-loop input impedance.

In a practical amplifier, one that must operate over a wide range of closed-loop gains, the fastest possible response time is achieved for large closed-loop gains by extending the natural break frequencies of the open-loop amplifier to obtain the largest possible gain-bandwidth product. Amplifier capacitance, which determines bandwidth, can then be kept small, and the slew rate, which is also fixed by amplifier capacitance, can be held at a large value.

A high open-loop gain presents a difficult frequency-compensation problem when a fast unity-gain closed-loop response is needed. For example, suppose the same bandwidth must be available from a single-pole 6-dB/octave amplifier for unity-gain operation and for a closed-loop gain of 512. To do this, the amplifier's open-loop gain must be reduced by a factor of 512 at the desired bandwidth by increasing the internal compensation capacitance by a factor of 512. The increase in capacitance decreases the slew rate by a factor of 512 and degrades the unity-gain time response. One solution to the problem is to select the appropriate frequency-compensation components digitally so that the settling time for each gain setting is optimized.

The simplified Bode plots of Fig. 5 show the individual frequency responses of the over-all amplifier, along with the closed-loop responses for unity gain and a gain of 512. The bandwidth for a closed-loop gain of 512 is determined primarily for first-stage capacitors C_1 and C_2 and second-stage capacitor C_1, all of which assume small values. The 125-kilohertz upper frequency limit is determined by the RC networks of Fig. 2.

The capacitive component and the resistive component of high-impedance node A of the second stage establish the first break point of the amplifier. Since the resistive component is very large, the first break point occurs at a relatively low frequency with only a small value of capacitance, thereby permitting slew rates of several hundred volts per microsecond to be realized.

The second break frequency, at around 4 kHz, is determined by time constants $R_{13}C_1$ and $R_{14}C_2$ in the first stage. The resulting two-pole response reduces the open-loop gain at a rate of 12 dB/octave, which increases slew rate and the high-frequency loop gain more than the 6-dB/octave rate.

The unity-gain bandwidth can be determined by a lag-lead network that is digitally selected at the high impedance node of the second stage, as shown in Fig. 4. This type of unity-gain compensation has the advantage of a 12-dB/octave rolloff. Unlike the compensation for a gain of 512, the unity-gain compensation increases bandwidth while decreasing slew rate so that the settling times for the two gain settings are approximately the same. Similarly, opposing compensation networks can be traded off for gain values between unity and 512.

Two additional lead-compensation networks in the first stage (time constants $R_{15}C_1$ and $R_{16}C_2$) and one in the second stage (time constant $2R_EC_4$) complete the over-all amplifier's internal frequency compensation. These three lead networks cancel poles in those cascode transistor pairs that have two natural poles.

The gain degeneration employed throughout the amplifier design stabilizes the lag and lead compensation networks, and provides an over-all gain-bandwidth performance that is determined by passive components, instead of sensitive semiconductor parameters. □

Dynamic zero-correction method suppresses offset error in op amps

In data-acquisition systems, the offset voltage and offset voltage temperature drift of a FET-input op amp can be held to only a few microvolts by a sample-and-hold correction technique

by Richard C. Jaeger and George A. Hellwarth, *IBM General Systems Division, Boca Raton, Fla.*

☐ Although today's monolithic FET-input operational amplifier offers the advantages of high input impedance, large open-loop gain, fast slew rate, and low input-bias current, it often has a high initial offset voltage that drifts with time and with changing temperature.

However, certain dynamic zero-correction techniques can drive the initial offset voltage to zero and reduce the effect of initial offset current when the amplifier is used for signal conditioning in a multiplexed or sampled data-acquisition system. One such scheme keeps the amplifier's input voltage to only a few microvolts and its offset voltage temperature drift to merely a few hundredths of a microvolt per degree Celsius.

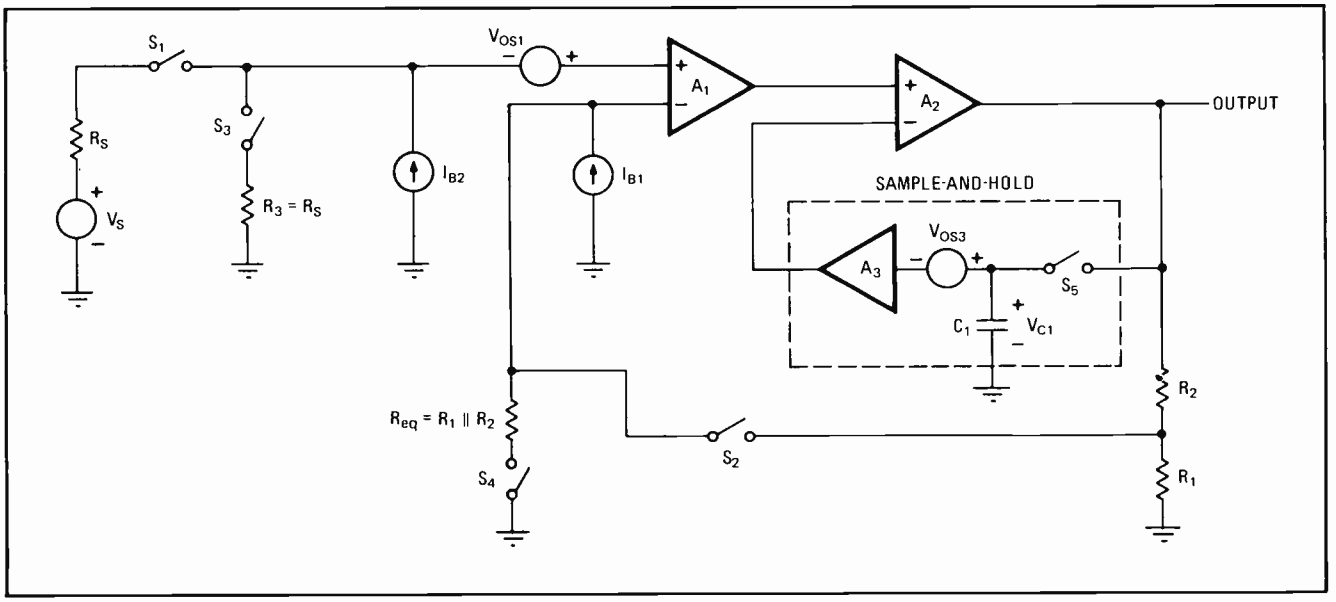
This method overcomes the shortcomings of previous dynamic zero-correction techniques. One method, for example, controls drift by inserting a dc correction signal into the amplifier's input with a periodically operated switch or modulator, an auxiliary ac-coupled amplifier, and a demodulator switch and filter. This scheme is not only expensive, but it produces carrier-frequency noise from the switches and recovers slowly from an overload condition.

Recent methods require switches operating synchronously between the cycles of a multiplexer or an analog-to-digital converter so that the switches and demodulation filter become a measure-and-hold circuit. After measuring the magnitude of the input offset voltage (with the amplifier input shorted by a switch), the circuit holds the correction voltage inserted at the amplifier input. This technique is sometimes hampered by errors in the sample-and-hold circuit and by feedback instability during the correction cycle.

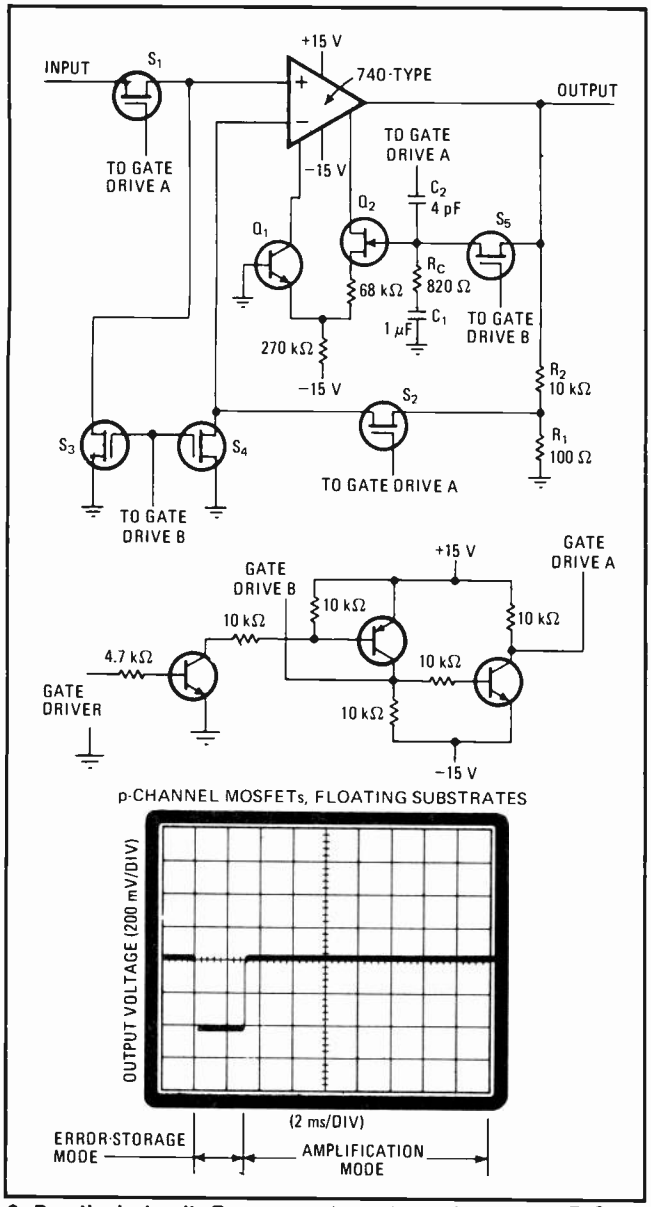
Zeroing out offset error

In the improved zero-correction scheme (Fig. 1), the amplifier is also driven by a multiplexer, and the offset voltage is dynamically eliminated between multiplexer cycles. A set of switches, which are synchronously linked to the multiplexer timing control, change the amplifier's operating mode to eliminate offset error. MOSFETs are usually used as the switches because of their operating speed and predictable switching action.

Zero correction is implemented by disconnecting and grounding both inputs of amplifier A_1, allowing the forward gain of the over-all amplifier to generate a large output voltage that is fed back to the input of interstage



1. Dynamic zero-correction. Offset voltage of over-all amplifier is held to a few microvolts by inserting correction voltage at input of amplifier A_2. By applying correction voltage at interstage between A_1 and A_2, errors due to sample-and-hold inaccuracies can be minimized. Sample-and-hold circuit stores correction voltage while over-all amplifier has its feedback loop open and is disconnected from source



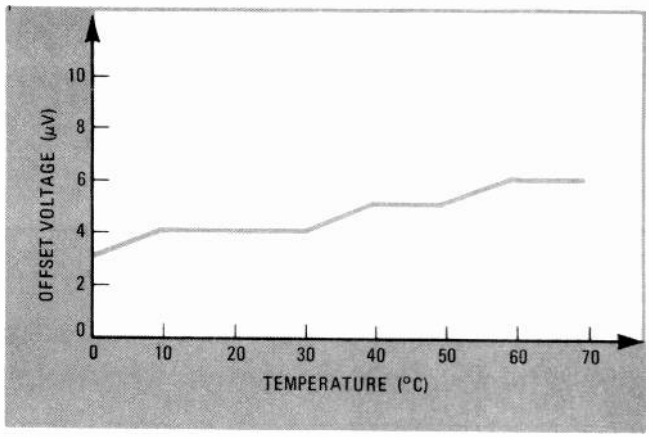
2. Practical circuit. Zero-correction scheme for popular 740-type op amp employs MOSFET switches to cycle op amp between error storage and amplification modes. Sample-and-hold circuit, which is composed of switch S_5, transistors Q_1 and Q_2, and capacitor C_1, inserts correction current, rather than correction voltage, into an intermediate stage of op amp. Scope trace shows op-amp output.

amplifier A_2. The feedback voltage is sampled and held while amplifier A_1 is returned to normal operation by reconnecting its input to the signal source.

The over-all amplifier is cycled between two modes of operation—amplification and error storage. The error storage cycle begins when switches S_1 and S_2 are opened and switches S_3, S_4, and S_5 are closed. This causes A_1 to amplify its own offset voltage and the sampling circuit to derive the correction voltage.

Opening switches S_3, S_4, and S_5 and closing switches S_1 and S_2 start the amplification cycle by driving A_1 with the input-signal source and closing the over-all amplifier's normal feedback loop. The correction voltage remains applied to amplifier A_2 so that A_1's offset is reduced by an amount determined by A_2's gain.

The zero-corrected amplifier offset, therefore, can be



3. Almost-zero drift. Offset voltage of zero-corrected 740-type op amp is initially 3 μV and has temperature drift of under 0.05 μV/°C.

expressed in terms of A_1's offset and A_2's gain:

$$V_{OS} = V_{OS1}/(1+G_{A2})$$

where V_{OS1} is the equivalent amplifier input offset voltage without correction, and G_{A2} is the open-loop gain of A_2. The correction voltage stored on capacitor C_1 is:

$$V_{C1} = G_{A1}G_{A2}V_{OS1}/(1+G_{A2}) + V_{OS3}$$

where V_{OS3} is the offset voltage of unity-gain amplifier A_3, and G_{A1} is the open-loop gain of amplifier A_1.

Because the correction voltage is applied after the first stage of the over-all amplifier, the effect of errors caused by sample-and-hold inaccuracies is significantly reduced. Resistor R_{eq} is made equal to the parallel combination of resistors R_1 and R_2 to correct for the error caused by bias current I_{B1}, which flows through these resistors during normal amplifier operation. Similarly, the error due to bias current I_{B2} is compensated for by resistor R_3, which has the same value as resistor R_S.

Getting practical

Figure 2 shows a practical zero-correction scheme for the popular FET-input 740-type op amp. The components are numbered to correspond with the labels of Fig. 1. Amplifiers A_1 and A_2 of Fig. 1 become the op-amp's input and output stages, respectively.

The sample-and-hold circuit, which is formed by switch S_5, transistors Q_1 and Q_2, and capacitor C_1, injects a correction-signal current, instead of a correction-signal voltage as shown in Fig. 1, into the interstage offset adjustment port of the op amp. Resistor R_C is included to stabilize the negative feedback of the correction loop during error storage.

When switch S_3 opens, the correction voltage on capacitor C_1 is disturbed because the circuit's gate-drive signal is coupled through the gate-source capacitance of the MOSFET that is being used as the switch. Capacitor C_2, which is returned to the gate-drive signal having opposite polarity, neutralizes this error. The scope trace depicts the circuit's output as the op amp cycles between the error-storage mode and the amplification mode, where the source voltage is zero.

A plot (Fig. 3) of offset voltage (referred to the op amp's input) as a function of temperature illustrates the remarkably low drift this zero-correction scheme can attain. The circuit brings the initial offset voltage down to only a few microvolts and holds offset voltage temperature drift to less than 0.05 μV/°C. □

Programs in Getel speak test engineer's language

English-based language and translator can be applied to automatic test equipment, making it easy for engineers and technicians to write in new routines and check out program parameters

by Gene Kierce, *General Electric Co., Schenectady, N.Y.*

☐ Because each computer-controlled test system must be addressed in its own language, only the operators have had the opportunity to become fluent in those languages. As a result, many engineers with product quality responsibilities have not been able to easily check what parameters actually were being measured. Such difficulties have even spread to the equipment troubleshooters, who had to figure out what the test equipment was testing before they could even begin the task of finding out what was wrong with the equipment under test.

To solve such problems, test equipment engineers from 15 different departments at General Electric Co. joined forces to develop a single language and a translator that applies it to any piece of automatic test gear. An added bonus is that the language, Getel (for general test engineer language, pronounced jee-tell), is based on English, so that an operator needs little formal training and almost anyone else can understand what's actually being tested.

Experience with the language has shown that technicians and engineers can learn to read and understand a Getel program in anywhere from a few minutes to a couple of hours and can be programing proficiently in less than a week. The use of English also allows even a typist to correct many spelling and programing errors, and troubleshooters can use the source listing as a checkout routine.

Getel is now in wide use in many General Electric plants, furnishing inputs to a wide range of systems such as the GE-MAC tester controlled by a GE-PAC 30 controller, the Hewlett-Packard rf tester, the tape-driven Systomation Fixit tester for checking wiring, and the tape-driven Texas Instruments TI553 integrated-circuit tester.

Mini-translator. Although English is the most convenient language for an operator, it is difficult to translate into a useful format for controlling machines. Originally, the plan was to develop a large central software translator to process Getel. The translator was to produce an intermediate language that could be processed by a smaller machine, which in turn would control a specific instrument. However, the language and the translator became larger and larger as the development went on, so that only the largest computers could be used to process the translation program. Although this software translator has actually been designed (and named Mark III), it is not actually in use. Rather, a smaller translator, the Mark I, is in regular use, since it can fit into a minicomputer with an 8,192-word memory.

The Mark I can translate from Getel into any langauge that the user desires. In the case of the GE-PAC 30-GE-MAC test system, the Getel compiler translates test statements directly into GE-PAC 30 assembly code.

A medium-size translator, the Mark II, has also been developed. It can fit into a 16,384-word machine, and is mounted in a computer, but has not yet been used at GE because the Mark I has been able to serve all the users' needs to this time.

Filling the blanks. The Mark I's translation from Getel into a tester's language is performed with a template-type approach. The Getel statement is considered to have a fixed portion that corresponds directly with a statement in the translated language, and a variable portion, which contains the specific numbers relating to the test at hand. For example in the statement

100 SET 'L1' TO 50 OHMS

the value for the load, 50, is a variable. The remainder of the statement is fixed and thus, if the variable part is deleted, the statement appears with a hole in this place (denoted by an asterisk) and thus can be considered to be a template.

100 SET 'L1' TO * OHMS

Such templates are part of the automatic test equipment (ATE) conversion table, which is composed by a test engineer for each particular automatic test system. The ATE table thus relates Getel to a particular test system, requiring only the specific numbers to fill the holes and thus complete an instruction to the automatic test system in its own language. For example, the corresponding statement in GE-PAC 30 assembly code for the above term, as might be required for the GE-MAC test systems would be

```
        LHI RE,2
        BAL RF, MONITR
        B* +8
        DC A(Z99999)
        *
        *     *
Z99999 DC 50
```

The statement in Getel is called a source statement and the translated form is called the object statement. Once the templates have been created for the ATE con-

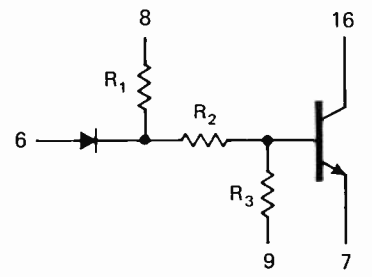
version table, any engineer can write programs in Getel without concerning himself with the details of the particular automatic test equipment that will perform the tests. However, note that not all Getel statements will have holes—many will be control-type statements that have direct counterparts in the object language that controls the tester.

Getel is based on a logical assignment of tasks to man and the computer, taking advantage of the capabilities of each. The early steps of carrying out a test program either are creative or require decision-making ability that is best performed by a man, while the later steps are best assigned to the computer, since it can store and retrieve data without error. To demonstrate the assignment of tasks, here are the typical steps in the process of performing a test.

After getting together all the necessary prints, schematics, and specifications the test operator must establish parametric requirements for the unit to be tested. This is best done by a man at present, since he can evaluate the circuit performance and thus set limits on the various parameters to be tested. However, some design automation programs are closing the gap since they can be designed with a capability to analyze the circuit and relate certain internal parameters to input-output requirements.

Next, the operator must determine the best test sequence, taking into account the likelihood of failure for each test and the relative importance of each test in meeting the specifications. The next step is to determine what actions must be taken based on the results of the test.

1. Easy reading. Test routine for simple inverter circuit is written as instructions for manual test (left column), and also in programing languages for four different testers. Getel program for same test is at right. Note close correspondence between Getel terminology and instructions for manual test that would be performed by a technician at the test bench.

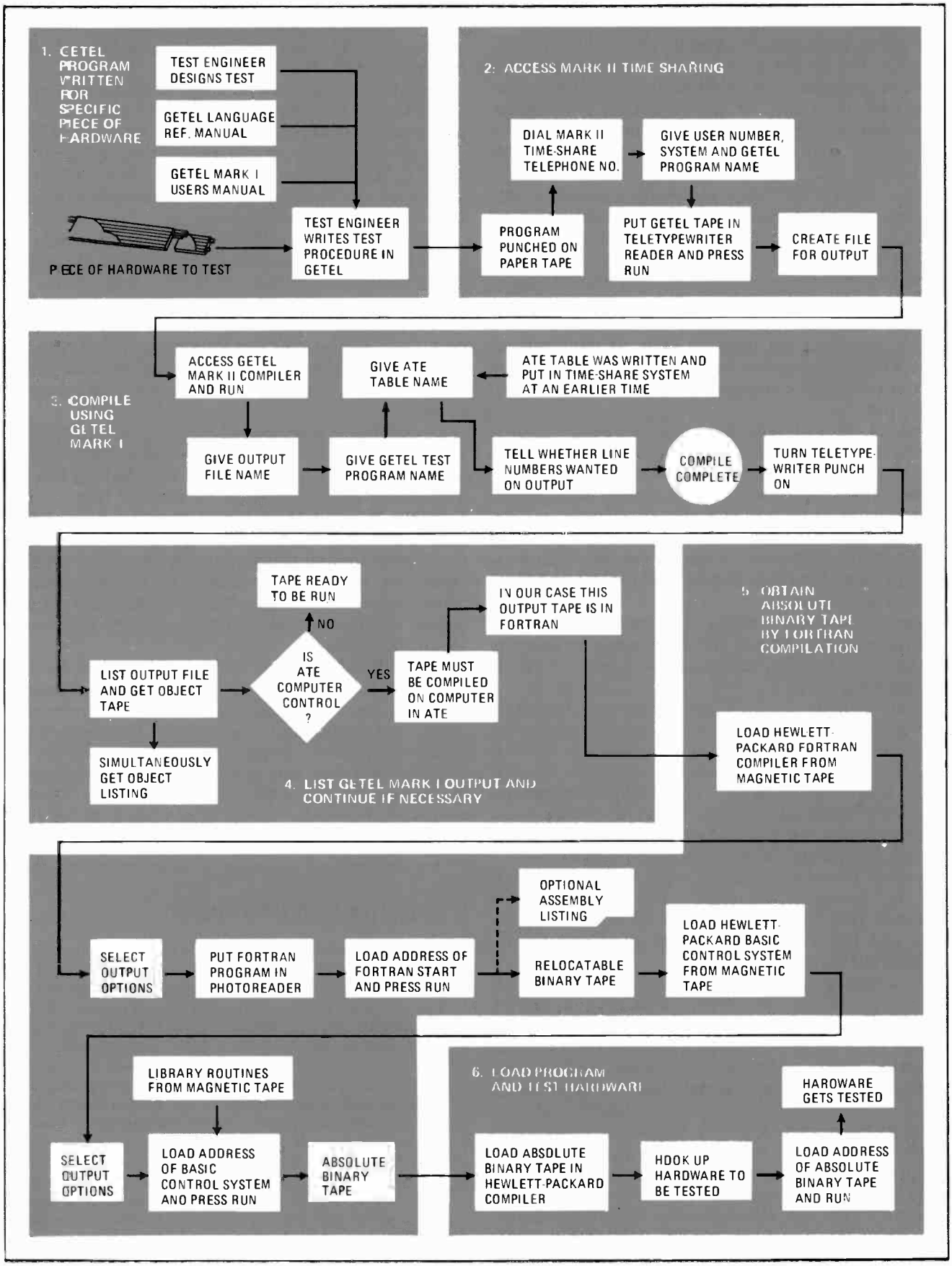


CIRCUIT INPUT REQUIREMENTS :	CIRCUIT OUTPUT REQUIREMENTS :
+12 volts dc on pin 8 −12 volts dc on pin 9 Ground on pin 7 Logical 1: +6.1 volts dc Logical 0: +0.0 volts dc } pin 6	Unloaded output, pin 16 Logical 0, or 'down level' High limit: +0.5 volts dc Low limit: +0.0 volts dc } 12 ma. Logical 1, or 'up level' High limit: +12.0 volts dc Low limit: +11.3 volts dc } 0 ma.

MANUAL TEST INSTRUCTION	A	B	C	D	GETEL
1.0 Test 1	01 @TEST NO. 01@	TID001	980000040001	04	100 Test 1
Apply 12 volts dc to pin 8 reference to pin 7.	02 FB +12.00, TB08	BV11200	010120850800	10 20	110 Apply 12.0 VDC to 'pin 8'
Apply −12 volts dc to pin 9 reference to pin 7.	03 FC −12.00, TB09	BC1PL2	021120850800	31	
Apply 12 ma dc to pin 16 reference to pin 7.	04 TG07	W1001	034120807800	08	120 Apply −12.0 VDC to 'pin 9'
Apply 6.1 volts dc to pin 6 reference to pin 7.	05 FE +012.0, TE16	BV21200	040610704800	20 88	
Measure output dc voltage on pin 16 reference to pin 7.	06 FD +06.10, TD06	BC2NL2	100000047120	39	130 Apply 12.0 MADC to 'pin 16'
Compare output dc voltage against high limit −0.5 volts dc —and low limit—0 volts dc.	07 MV16/H +0.5v/L +0.0v	W1102	110000030000	20	
Record the value if it fails.	08 PFC	W0911	221600000000	89 39	140 Measure 'DC voltage',10±.1%
		BIX03M1200	214000070000	20	
		BVX03M1200	202050000000	87 39	150 VDC at 'pin 16'
		BV30610	----------	24	160 Record 'result'
		BC3PL2 W0703		81 34	170 Compare 'result' to '0.5,'0.0' goto 'HIGHM', 'LOWM'
		W201403		21 96	
		MTRSVPOR		31	180 Perform Test 2
		MAXP0050P0		24 85	190 HIGH; MESSAGE TEST1 FAILED HI
		MINP0000P0		33 20	
		RIU4		96 33	200 LOWM; MESSAGE TEST1 FAILED LO

A: AAI Model 1000 IC tester; B: TI 553 IC tester; C: Fairchild Model 5000; D: GE-PAC 200 controller

2. Test run. At GE, test engineers use the Mark II time-sharing system to prepare Getel programs. After accessing the system, Getel is compiled with the Mark I translator program (Getel MI). In this example, Getel is translated to Fortran for use on the Hewlett-Packard rf tester. The output of the system is a tape to be inserted in the tester to control the actual test.



Likewise, the operator is best able to decide how much data is enough and how best to control the operator displays. He also can explore other possible ways of performing the test, if he decides that the test station cannot do it.

However, after this, the computer can take over. The computer can be instructed about what equipment is available and what its capabilities are. From this instrument pool, the computer can choose the instruments, since it can even keep track of which instruments are in use on other tests and which instruments are available for this test.

The computer can then translate the instructions into machine code to operate the instruments, using look-up tables. This is one step that a man performs poorly—it is an unthinking task and errors often creep in. Also, the translation of these machine codes back into English to see if any errors have been introduced is unnecessary with the computer. The machine can also optimize test time by checking the machine code for duplications. Thus, with Getel, the user can describe the parameter to be tested and the computer will select the instrument for the job.

Test instrumentation falls into three categories: sources (power supplies, signal generators); sensors (digital voltmeters, electronic counters); and loads (resistors, capacitors, inductors). To control such instruments, the operator uses as statements simple imperative sentences containing verbs that are commonly used by test engineers. Prefixes, suffixes, and units abbreviations for Getel are taken from IEEE standards and Government documents.

The user also can define synonyms and insert standard routines into the body of the program to compose new complex test functions based on groups of simple test functions.

As an example of how Getel differs from languages used in the automatic testers, consider a typical inverter circuit that is common enough to be tested practically on any of several types of automatic testers. The test will be programed in each of several languages and also in Getel. (The actual meaning of each command in the languages is not really important for this discussion—the example is presented only to illustrate complexities.)

Testing. To test the inverter, appropriate supply voltages must be applied along with a certain signal level to the input. Then the output must be measured and compared with the design value, and the output must be recorded if the inverter fails the test.

The circuit is shown in Fig. 1, along with a set of test instructions written for interpretation by a technician actually doing manual testing. The instructions in the column for tester A—AAI Corp.'s model 1000, a popular integrated circuit tester—are almost self-evident. This tester uses a pseudo-variable-field technical programing language, in which the alphabetic terms are used; FB means fix bias supply B, and TB means tie (connect) bias supply B, but still an engineer might find it difficult to interpret the instructions with certainty unless he actually knew the language.

Tester B, TI's 553, also uses some alphabetic characters, but Tester C, Fairchild's model 5000, uses numeric code only, as does Tester D, the GE-PAC 200 controller. In many cases, single instructions for the manual test must be expanded into several subinstructions for the automatic tester.

In Getel, there is little difference between the instructions for manual test and the instructions for automatic testing. Only line numbers have been added and all labels have been apostrophized.

Most users at General Electric access Getel through GE's Mark II time-sharing system (the Mark II in this case bears no relationship to the presently unused Mark II translator for Getel; the redundancy occurred because of the assignment of the name Mark III to the large translator, and this term propagated through later versions of Getel translators).

Step by step. Before the test engineer signs onto the Mark II system, he familiarizes himself with the unit to be tested and designs the test. He then converts the test instructions to a Getel program. The Getel program then is punched on paper tape in ASCII (American Standard Code for Information Interchange), and then the engineer dials the GE Mark II system on a telephone hooked up to a teletypewriter, as shown in the diagram in Fig. 2.

Upon request from the time-sharing system, he gives his user number to identify himself as a qualified user, and the system then queries him on which of the two available languages—Basic or Fortran—he wants to use. Since the Mark I translator is written in Fortran, he responds with that selection. He then gives a name to his Getel program and enters the paper tape into the teletypewriter reader for insertion in the time-sharing memory. He then creates a file in the time-sharing system in which the translated program (the object program) will be stored.

After telling the system that he wishes to use the Getel Mark I program, he goes through some bookkeeping steps with the teletypewriter, loads in the proper ATE conversion table, and the system then delivers a punched tape of the object program for use on the automatic test system that he intends to use. This tape can then either be processed further on the test system's computer or the test can be run directly from the tape, depending on the tester in use. □

Anyone can use Getel

Getel is available to users outside General Electric. It has been put on GE's Network Service, a time-sharing service centered in Cleveland. Remote concentrators in Los Angeles, Kansas City, Atlanta, Teaneck, N.J., Schenectady, N.Y., and Washington, D.C., link the central computer complex—which comprises a GE-635 central processor, a GE-4020 communications processor, and a disk file complex—to remote buffer units in major metropolitan cities. Customers can gain access to the system with a local phone call. Overseas, the network can be used in such cities as Amersfoort, Brussels, London, Manchester, Birmingham, and Paris. In the western hemisphere, outside the continental United States, the network can be dialed from remote units in such cities as Mexico City, San Juan, Montreal, Toronto, Vancouver, and Anchorage.

GETEL VOCABULARY

OPERATIONS

APPLY
CALCULATE
CLEAR
COMPARE
COMPLETED
CONNECT
CONTINUE
DEFINE
DELAY
DISCONNECT
END
EXECUTE
EXTERNAL
GOTO
IF-GOTO
IF-PERFORM
INSERT
LET
MEASURE
NOTE
PAUSE
PERFORM
PROCEDURE
READ
RECORD
RESERVE
RESET
ROUTINE
ROUTINE END
SELECT
SENSE
SHARE
TEST
TITLE
TURNOFF
TURNON
USE

LOGIC SIGNAL

ZERO MAG
ONE MAG
RT
FT
NOISE
FREQ
SKEW TIME

SQUARE WAVE

BW
IMP
PHASE-JITTER
RT
FT
TIME ASYM
OVERSHOOT
UNDERSHOOT
PRESHOOT
DROOP
RINGING
ROUNDING
DC-OFFSET

MULTIPLIERS

P	(10^{-12})
N	(10^{-9})
U	(10^{-6})
M	(10^{-3})
K	(10^{3})
MEG	(10^{6})
G	(10^{9})

TIME INTERVAL

TIME
SEC
MIN
HR
START
STOP
TRIG
FIRST POS SLOPE
FIRST NEG SLOPE
CHANNEL A

TRIANGULAR WAVE

FREQ
BW
IMP
PHASE-JITTER
NONLIM
TIME ASYM
PEAK-DEGEN
DC-OFFSET

UNITS

AAC
AMP AC
AMPS AC
ADC
AMP DC
AMPS DC
VAC
VOLT AC
VOLTS AC
VDC
VOLT DC
VOLTS DC
WATT
WATTS
A/SEC
AMP/SEC
AMPS/SEC
DB
DEG
DEG-C
DEG-F
DEG-K
DEG-R
FD
HY
HZ
HERTZ
HR
OHM
PCT
PPS
RAD
REV
SEC
S-PARAMETERS
V/HZ

AM SIGNAL

MODUL-AMPTD
CARR-AMPTD
CARR-FREQ
HARMONICS
NONHARMONICS
NOISE
PHASE-JITTER

DC SIGNAL

POWER
CUR-LIM
VOLT-LIM
IMP
RIPPLE
RIPPLE-FREQ
NOISE
DISTORTION
CUR MONITOR
VOLT MONITOR

FM SIGNAL

FM-INDEX
CARR-FREQ
MODUL-FREQ
HARMONIC DIST
NONHARMONIC DIST
AMPTD-MODUL
MODUL-DIST
NOISE

SUFFIXES

-TRMS (true rms)
-AU (average)
-PP (peak-to-peak)
-P (peak)

Sceptre rules benevolently over computer-aided design

Some practical tips on solving nonlinear problems with Sceptre reduce the complexity and cost of this computer program; tradeoffs must be made between circuit models, solution accuracy, and running time

by George C. Kenney, *North American Philips Corp . Briarcliff Manor, N Y*

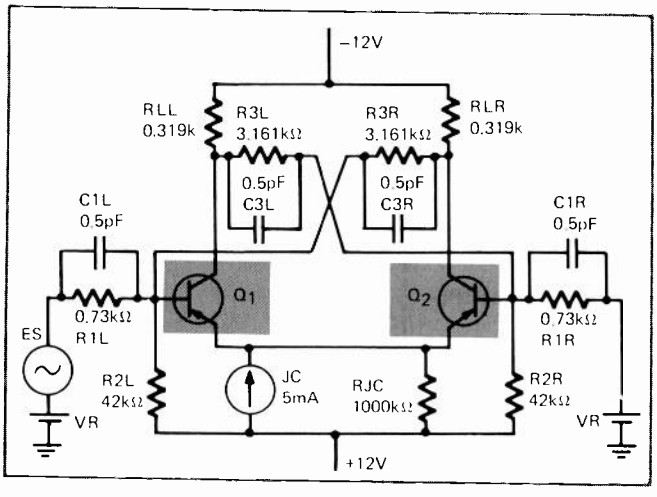
☐ Solving linear and nonlinear circuit problems is the province of a powerful computer program called Sceptre. Unfortunately, its reign has been limited by its complexity, high cost, and lengthy computer time. Sceptre, however, can be a practical and very valuable engineering instrument if used properly.

Sceptre, which stands for system for circuit evaluation and prediction of transient radiation effects, can determine initial dc conditions and transient responses to general forcing functions for linear and nonlinear systems. Although it is primarily intended for circuits, it can find solutions for systems in any discipline.

Until recently, Sceptre was available only by batch run at a computer facility, making it costly, time-consuming, and difficult to use. As a result, many nonlinear problems were solved by hand calculations, circuit experiments, or by piecewise linearization with ECAP (electronic circuit analysis program).

But now, input/output data for a Sceptre program can be handled by a remote teletypewriter terminal (through software provided by Computer Sciences Corp., Infonet div., El Segundo, Calif.). This allows the user to solve nonlinear problems with an ease approaching that of time-shared ECAP, and with reasonable expenditure of time and cost.

1. Circuit problem. Hysteresis of this flip-flop can be computed and plotted with Sceptre. Circuit elements are labeled for easy computer callout, with letters L and R differentiating between left and right side of flip-flop. Current sources are denoted by J.



Sceptre accepts input system data in two forms: as nonlinear, first-order, differential equations or as engineering descriptions of a circuit (similar to ECAP). Initial dc conditions are computed or supplied by the user if known, then a transient analysis of the system's response to forcing functions—such as time-varying voltages or currents—is carried out. It is also possible to run initial conditions only and then, after inspection, run transient conditions, or compute only the transient mode by supplying the initial conditions.

Sceptre recognizes standard passive elements such as resistors, capacitors, inductors, transformers, and the ideal diode. Linear dependent sources—like voltage-controlled current or voltage sources or current-controlled voltage or current sources—can also be used. These circuit elements enable the user to synthesize Ebers-Moll models for transistors as well as diodes that are operational in the large- or small-signal region.

Models stored on tape can be retrieved for use at any point in a circuit. The models can be interconnected groups of passive or active, linear and nonlinear elements. Nonlinear "black boxes" are implemented by tables or a Fortran expression. A special section allows special parameters to be defined that may be unrelated to the primary problem. Moreover, the user may write his own Fortran program and insert it into a normal Sceptre run as a subroutine.

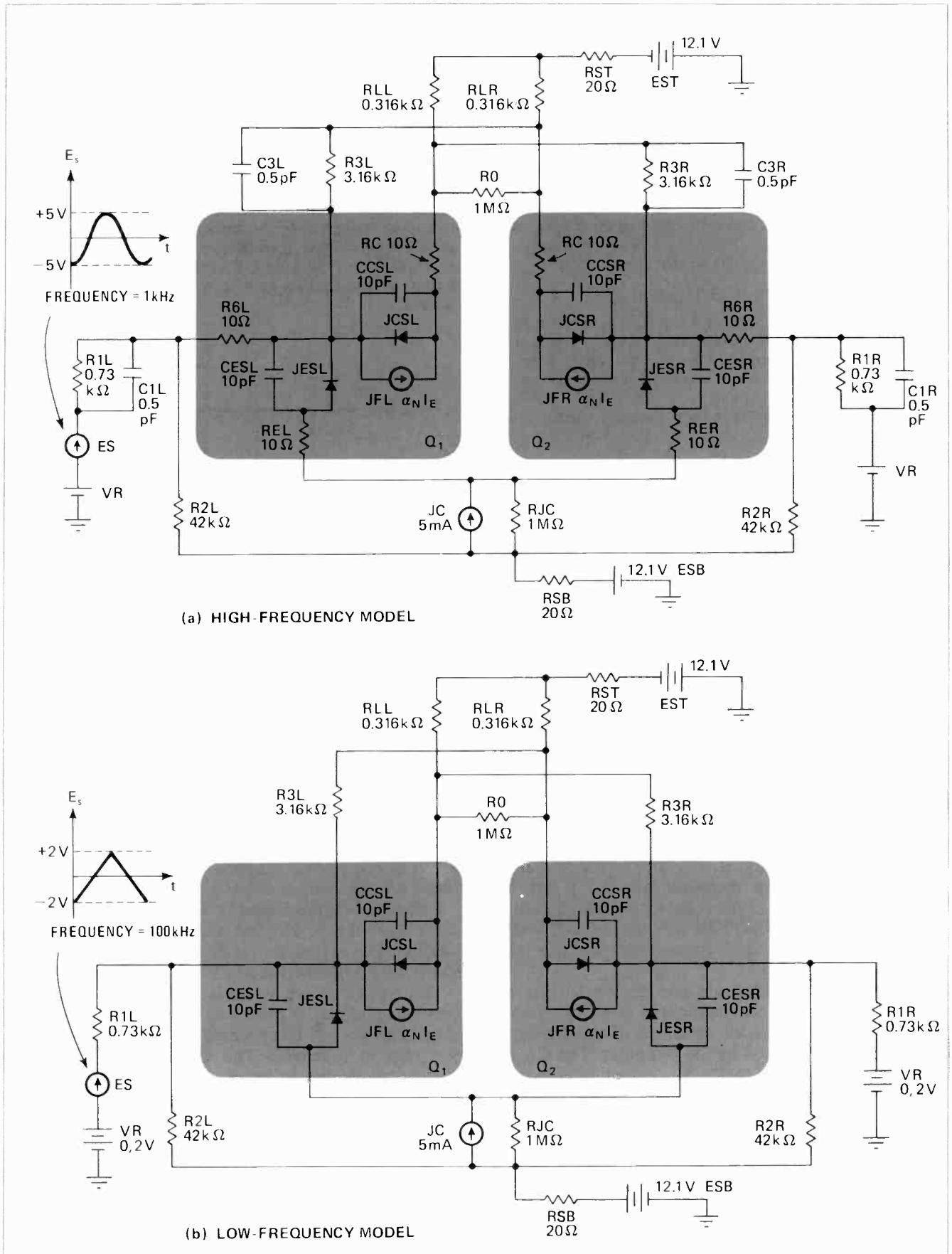
Using Sceptre. Printout is in tabular and/or selected graphical form. Sceptre will print any or all sources, in addition to circuit element currents or voltages, which are defined as a function of time or of any other parameter. The plots are easily requested, automatically scaled, and labeled.

An automatic termination feature stops the program upon satisfaction of any Fortran expression involving any of the circuit elements. For example, the statement

TERMINATE IF(-IR7 GT.10.1.AND.R9 LT.12.2)

will terminate the run when the reverse current through R_7 is greater than 10.1 milliamperes, and the voltage across R_9 is less than 12.1 volts.

Sceptre uses the state-variable principle as its mathematical basis. Capacitor branch voltages and inductor link currents are the state variables chosen to form a network of first-order, nonlinear, differential equations. This method is very efficient since computation time relates only to the number of state variables and not the number of elements.



2. Sceptre models. High-frequency model (a) on flip-flop includes transistor speed-up capacitors and lead resistance. These circuit elements, however, severely slow up solutions at low frequencies because Sceptre must take thousands of steps to arrive at answer. Changing to model shown in (b) speeds solution. Increasing frequency of forcing function and decreasing its amplitude also helps.

Ebers-Moll pnp transistor model

There are usually two circuit equations associated with the Ebers-Moll transistor model: one for the collector current, I_C, and the other for the emitter current, I_E.

The collector current is:

$$I_C = I_{CS}(e^{\theta_I V_{B'C'}} - 1)$$

where I_{CS} is the base-collector saturation current with the base-emitter shorted, and θ_I the slope of the natural log of I_C versus $V_{B'C'}$.

This equation can also be written as:

$$I_C = I_{CO}(e^{\theta_I V_{B'C'}} - 1)/(1 - \alpha_I\alpha_N)$$

where I_{CO} is the base-collector saturation current with the base-emitter open, α_I the inverted common-base current gain, and α_N the normal common-base current gain. For computer program listing, the collector current becomes:

I_C Γ DIODE EQUATION (θ_I, $V_{B'C'}$)

Similarly, the expression for the emitter current can be written as:

$$I_E = I_{ES}(e^{\theta_N V_{B'E}} - 1)$$

where I_{ES} is the base-emitter saturation current with the base-collector shorted, and θ_N the slope of the natural log of I_E versus $V_{B'E}$.

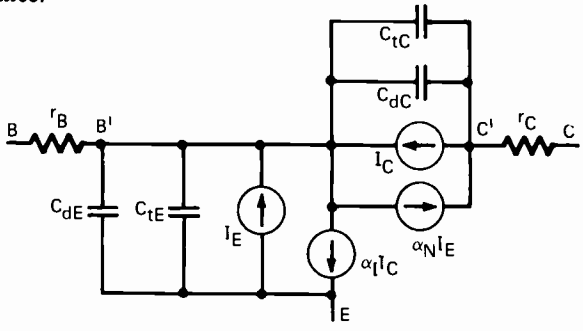
Another version of the equation is:

$$I_E = I_{EO}(e^{\theta_N V_{B'E}} - 1)/(1 - \alpha_I\alpha_N)$$

where I_{EO} is the base-emitter saturation current with the base-collector open. The program listing for I_E becomes:

I_E = DIODE EQUATION (θ_N, $V_{B'E}$)

The model's circuit elements are defined as: r_B, the base-spreading resistance; r_C, the series collector resistance; C_{dC}, the collector diffusion capacitance; C_{tC}, the collector junction transition capacitance; C_{dE}, the emitter diffusion capacitance; and C_{tE}, the emitter junction transition capacitance.



The first step in preparing a problem for analysis with Sceptre is to draw an equivalent circuit using resistors, inductors, capacitors, transformers, sources, and any necessary stored models. Circuit elements may be linear or nonlinear, and defined by a numerical constant, tabular list, or Fortran expression.

Next, name or number all nodes and name each circuit element. Then choose current flow direction in each passive element and source. Assign circuit values in a constant set of parameter units. (For high speed, a good set is kilohms, picofarads, microhenries, milliamperes, volts, and nanoseconds.)

Circuit elements can now be easily combined to form an Ebers-Moll large-signal transistor equivalent circuit (see "Ebers-Moll pnp transistor model," p. 74). The emitter current, I_E, and the collector current, I_C, are entered as DIODE EQUATION (θ,V) or DIODE TABLE XY to achieve numerical convergence for the initial condition solution.

An example will illustrate how to use Sceptre and how to implement model changes in order to achieve a successful run. The circuit hysteresis of the flip-flop in Fig 1 is to be predicted by the computer. The diagram uses a labeling scheme that is convenient for calling out circuit elements in a program. Besides the usual numerical differentiation between components, the letters L and R distinguish between elements on the left side and right side of the circuit.

The Sceptre model of the flip-flop in Fig. 2(a) uses a slightly modified version of the Ebers-Moll transistor equivalent shown on p. 74. Since the flip-flop's transistors never saturate, current source $\alpha_I I_C$ can be omitted. Diode JCSL (or JCSR) replaces current source I_C, and diode JESL (or JESR) replaces source I_E. Both the diffusion and transition emitter capacitances are combined in capacitor CESL (or CESR), while the diffusion and transition collector capacitances become CCSL (or CCSR). Also, small speed-up capacitors (5 pF) and lead resistances (10 ohms) are included for better accuracy.

Because the flip-flop's hysteresis is reflected in the difference between the collector voltage of Q_1 and Q_2, resistor RO is added. Circuit hysteresis, which is a function of R1L (and R1R) and R3L (and R3R), can be predicted by computing the voltage across RO.

Operating frequency range for the flip-flop is 1 kilohertz to 10 megahertz. Therefore, a forcing function with a frequency of 1 kHz is a reasonable choice for the excitation voltage. To guarantee that the flip-flop will trigger, the amplitude of the forcing function will be 5 V. Let the forcing function, then, be $E_s = -5\cos 2\pi 1000t$, where t is time.

Fail-safe. For the model of Fig. 2a, Sceptre will correctly solve the dc case but will fail to give a transient solution. The reason for the failure will be indicated as SMALLER MINIMUM STEP SIZE REQUIRED.

This type of failure, which is sometimes called the Eigenvalue problem, is caused by a conflict in circuit time constants that will incapacitate any nonlinear analysis, computer or otherwise. The flip-flop has natural frequency modes caused by short time constants that require very small time steps for accurate analysis. Because of the long running time to complete the solution, Sceptre will decline to solve the problem.

There are several elements aggravating the flip-flop's time-constant problem. Speed-up capacitors, header capacitances, and transistor lead resistance do not affect a low-frequency solution, but they do complicate solution processes and increase program time.

Step size is determined by the specified problem duration (stop time) and by the smallest time constant of the circuit. The initial step size chosen by Sceptre is 10^{-3} times the stop time. This step size is tested by the inte-

gration routine for accuracy, and if that size is found to be erroneous, a new step size that is half the previous value is attempted.

The test process is repeated until a small enough step size is found or until the step size is smaller than 10^{-5} times the stop time. If the step size required is less than this value, the run is terminated because a smaller minimum step size is required.

A successful run can be achieved without changing the low-frequency hysteresis by removing all speed-up capacitors and all lead resistances as shown in Fig. 2(b). It is also helpful to decrease the magnitude and period of the forcing voltage, E_s, to speed up the integration.

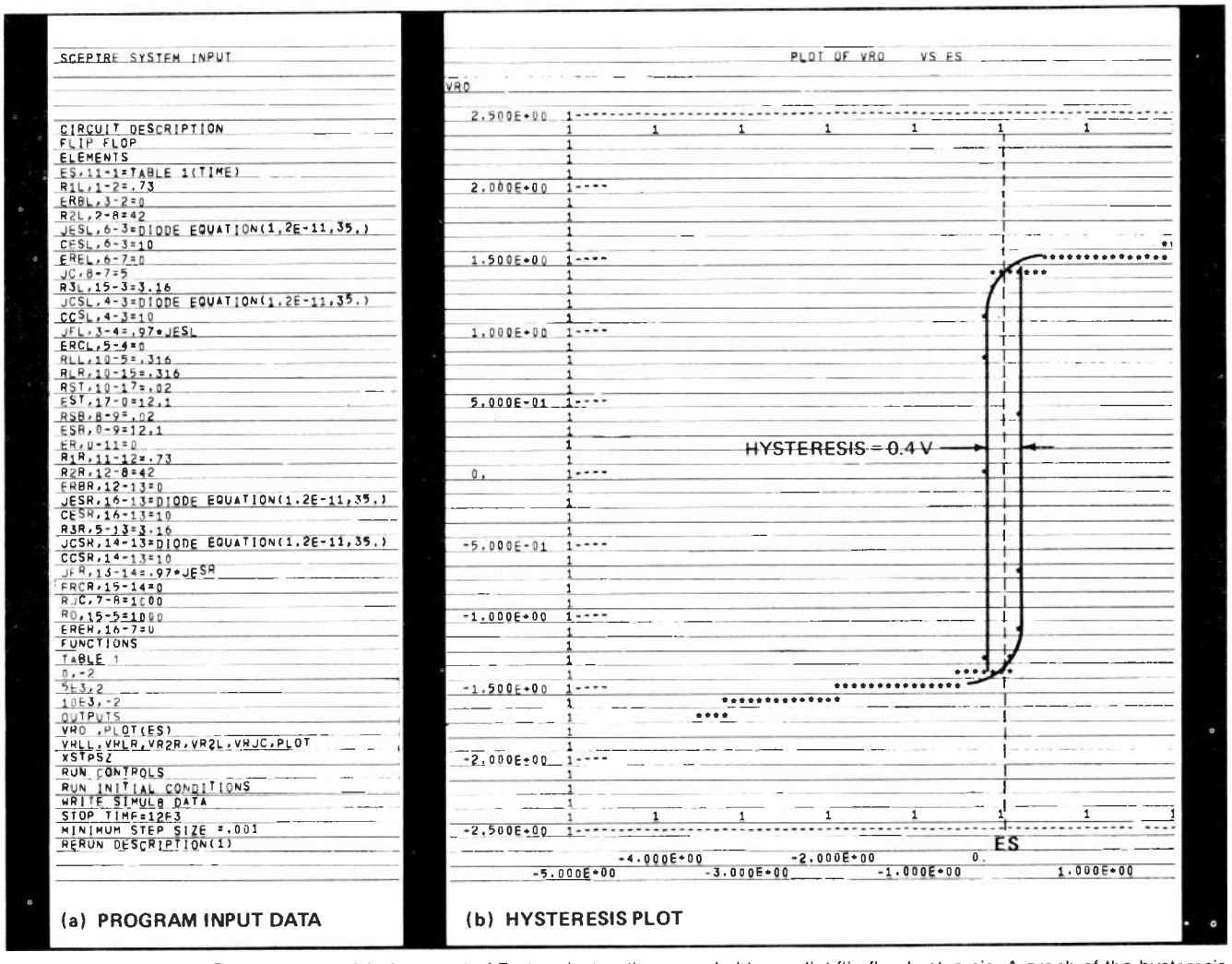
Actually measuring circuit hysteresis helps to determine how to modify E_s. A measurement will show that the hysteresis is about 0.5 V at 1 kHz as well as at 100 kHz; therefore, changing the frequency of E_s from 1 kHz to 100 kHz will speed the solution without affecting accuracy. Reducing the amplitude of E_s from 5 to 2 V also aids the solution without impairing the triggering of the flip-flop. Switching from a cosine wave to a triangle wave is another simplification. To see the change in hysteresis at high frequencies, another run could be made at 10 megahertz with the original model and original E_s.

Figure 3 reproduces the successful run of the program input data and the hysteresis plot. The forcing function, E_s, is entered as a table; all diodes are represented by the exponential diode equation. The program requests a plotted output of VRO, the voltage across resistor RO, versus E_s. The plot correlates fact with theory—computed hysteresis is 0.4 V; the measured is 0.5 V.

A brief look at cost considerations is also essential. Because Sceptre is a large program that requires expensive Fortran compilation, a good deal of its cost tends to be a fixed overhead. The flip-flop problem, for example, can be run with identical numerical results on an IBM 360-65 or a Univac 1108, using a conversational, remote, job entry teletypewriter. The price of the IBM run will be approximately $90, 80% of which is overhead, while the Univac solution costs $30 with 20% overhead.

Defined parameters. Another example will serve to illustrate the flexibility of Sceptre through the use of its special defined parameters section. Suppose the problem is to solve a set of first-order, simultaneous, differential equations that may be entirely independent of any electrical network:

$$X'(t) = -6X(t) + 5Y(t) + 10$$



3. Computer printout. Program listing (a) shows set of Fortran instructions needed to predict flip-flop hysteresis. A graph of the hysteresis (b) is obtained by requesting a plot of the collector difference voltage (between Q_1 and Q_2), represented by VRO, versus the forcing function, E_s. Distance between colored lines is predicted hysteresis voltage, which is 0.4 volt compared with measured value of 0.5 V.

Modified pnp Ebers-Moll model

A few minor modifications of the conventional Ebers-Moll transistor model improves its speed without adversely affecting its accuracy. Eliminating extraneous resistances and carefully combining diffusion and transition capacitances implements the change.

The equation for transistor collector current, I_C, can be written as:

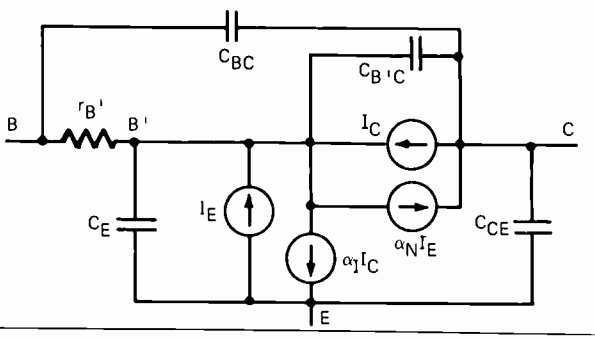
$$I_C = I_{CO}(e^{\theta_I V_{B'C}} - 1)$$

while the expression for transistor emitter current, I_E, becomes:

$$I_E = I_{EO}(e^{\theta_N V_{B'E}} - 1)$$

All modified circuit elements are defined in terms of the original model:

$C_{BC} = 3C_{tC}/4$
$C_{B'C} = C_{tC}/4 + C_{dC}$
$C_E = C_{dE} + C_{tE}$
$C_C = C_{dC} + C_{tC} = C_{BC} + C_{B'C}$
C_{CE} = collector-emitter header capacitance
$r_{B'}$ = base-spreading resistance
$C_{dC} = \theta_I \tau_S I_C$
where τ_S is storage time
$C_{dE} = \theta_N \tau_E I_E$
where τ_E is the minority carrier transit time
$\tau_E = 1/\omega_{alpha} = 1/1.2\omega_T$
where ω_{alpha} is the alpha cutoff frequency, and ω_T is the beta cutoff frequency
$C_{tC} = C_{obo} - C_{CE}$
where C_{obo} is the output capacitance with the emitter open
$C_{tE} = C_{ibo} - C_{CE}$
where C_{ibo} is the input capacitance with the collector open.



$Y'(t) = 5X(t) - 7Y(t)$

The initial conditions are $X(0) = 6$ and $Y(0) = 5$.

Each of the derivatives may be entered under the program listing DEFINED PARAMETERS in explicit form. A proper sequence would be:

```
CIRCUIT DESCRIPTION
DIFFERENTIAL EQUATION EXAMPLE
(Enter data, for instance, as in Fig. 3(a).)
DEFINE PARAMETERS
DPX = EQUATION 1 (PX,PY)
DPY = EQUATION 2 (PX,PY)
PX = 6
PY = 5
OUTPUTS
PX(X), PY(Y), XSTPSZ, PLOT
FUNCTIONS
(Define equations X'(t) = -6X(t) + 5Y(t) + 10 and
Y'(t) = 5X(t) - 7Y(t) by using dummy variables A
and B for X and Y, respectively.)
EQUATION 1 (A,B,) = (-6.*A+5.*B+10.)
EQUATION 2 (A,B) = (5.*A-7.*B+2.)
RUN CONTROLS
INTEGRATION ROUTINE = TRAP
STOP TIME = 100
END
```

Since the derivatives of PX and PY (DPX and DPY, respectively) are entered in the program, the functions of PX and PY must be updated at each integration step.

It should be noted that the initial values of the variables X and Y are entered as PX = 6 and PY = 5; the differential equations themselves are entered under DEFINED PARAMETERS. Since the quantities X and Y are treated like the state variables of a general transient problem, they are subject to the same step-size limitations in whatever Sceptre integration routine is used.

When the defined parameters feature is used, it should be remembered that Sceptre can only solve nonlinear, first-order, differential equations. Higher-order equations must be reduced to a set of first-order ones.

Limitations. There are several important factors to keep in mind when using Sceptre. The first one is to know the application. Sceptre can solve very complicated nonlinear problems; if the problem is linear, use ECAP. It is often worthwhile to simplify the problem by using different models at different frequencies.

Another consideration is computer models. For most nonlinear applications, transistors can satisfactorily be handled by Sceptre with the Ebers-Moll model shown in "Modified pnp Ebers-Moll model," above. It offers a good compromise between speed and accuracy. Always remember that the simplest satisfactory circuit model has the best chance of running.

Sceptre is limited to two types of active dependent circuit elements for accurate dc (initial condition) analysis. These are a current source that depends on a current and a nonlinear element, like the diode. The diode must be entered as a diode equation or a diode table. Any other active dependent circuit elements (such as voltage-dependent current sources, passive elements that depend on either voltages or currents, and tables for zener diodes, tunnel diodes, or any device whose characteristic curve does not monotonically increase) may cause convergence difficulties in the dc solution.

However, these elements present no difficulty for the transient solution portion of Sceptre. They even offer an alternate method of obtaining a circuit's initial condition when the dc method fails.

To approximate a dc steady-state solution, some initial conditions can be assumed and a transient solution run (with the forcing function set to zero and all capacitors given equal values) for a duration of five constants. Using the steady-state values obtained in this way as initial conditions, a transient run with a proper forcing function can be made. This technique should only be used after unsuccessful attempts to solve the dc case. Finding initial conditions by transient response will al-

ways require two runs to achieve a final solution.

Another difficulty often encountered is the Eigenvalue or small-time-constant problem. First, it should be determined whether the elements causing the trouble are necessary to get the desired solution. About 90% of the time, they are superfluous and only serve to bog down the program.

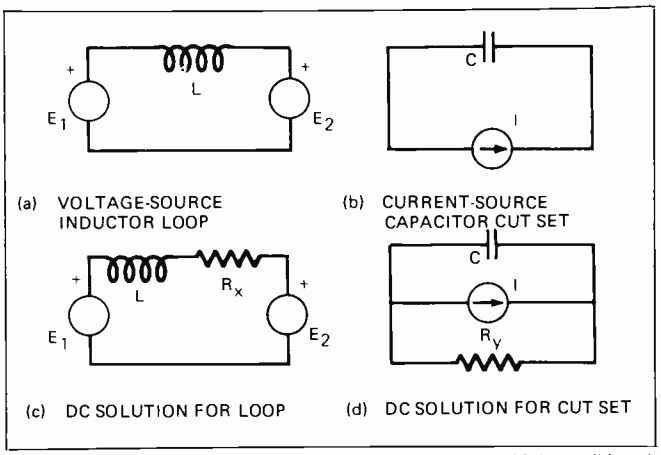
One method of solution is to use a simple model at low frequencies and a complex one at high frequencies, where the forcing-function frequency and the Eigenvalues are compatible. A good low-frequency model is one that has no capacitances except large diode shunt capacitors and that uses E_s at the highest possible frequency without appreciably changing the dc solution.

An appropriate, but not overly complex, model should be used for a second run at higher frequencies. This two-model technique will probably be more satisfying and less expensive than using the same model for high and low frequencies, as can be done with ECAP.

Even if the problem involves conflicting Eigenvalues and all attempts at separate solution are unsatisfactory, there is yet another approach. The user can allow Sceptre to take a smaller step size than the normal 10^{-5} times the stop time. A specific minimum step size (for example, MINIMUM STEP SIZE = 0.00001) is called out as a RUN CONTROLS instruction. Sceptre follows the same process to determine step size—starting with 10^{-3} times the stop time and dividing by two each integration pass until the specified limit is reached.

It is also useful to call out a maximum step size (like MAXIMUM STEP SIZE = 100) that is about 1% of the stop time. The program can then take large steps in time toward the solution when the derivative of the state variables are changing slowly. For example, a circuit problem may require very small step sizes in the beginning, but it could correctly take large steps later, near the steady-state condition.

Excessive computer time is not a concern when a very small step size is specified. A built-in counter logs integration passes and automatically terminates the run when the number of passes exceeds 20,000. When step size is varied, it is a good idea to call for XSTPSZ, PLOT under the OUTPUTS instruction so that step size is plotted as a function of time.



4. Topological restrictions. To solve the dc case (initial conditions) for a voltage-source inductor loop (a) or a current-source capacitor cut set (b), Sceptre requires the addition of a resistance—in series for the loop (c) and shunting for the cut set (d).

Nonlinear computer programs

At present, there are four computer-aided design programs for solving nonlinear circuit problems: Sceptre, NET-1, Circus and TRAC. Each one has its own special application and, when properly matched to a problem, will minimize both time and cost. Generally, Sceptre is considered the most powerful, flexible, and expensive of the four; it can solve many problems beyond the reach of the others.

NET-1 (network analysis program) employs predetermined stored Ebers-Moll models of junction diodes and bipolar transistors for a good compromise between speed and accuracy. But the program's flexibility is limited. NET-1 does not allow the user to account for such things as junction breakdown, base narrowing or conductive modulation.

Circus (circuit simulator) employs a somewhat awkward charge-control model that is mathematically equivalent to the Ebers-Moll model. Program restrictions include acceptance of only pulse or sine inputs, limited element library, and no tables or analytical expressions.

TRAC (transient radiation analysis by computer) cannot handle stored elements, tables, or analytical expressions. However, a problem that can be solved with TRAC will be done more economically and faster than with Sceptre.

Sceptre has three integration routines: TRAP, XPO, and RUK, which (in this order) are increasingly accurate, time consuming, and costly. For most applications, XPO, which gives a 2.5-term approximation of the Taylor series, offers optimum speed and accuracy.

Although Sceptre can handle up to 300 circuit branches, it is advisable to limit the number of branches to 70. The Fortran compiler cannot handle more than 70 branches at once, and large programs become difficult to run.

There are several reasonable topological restrictions imposed by Sceptre for dc solutions. Two are shown in Fig. 4—a voltage-source inductor loop and a current-source capacitor cut set (dual of a loop, connecting one node to another node). The dc case for these problems is solved by adding a small resistor, R_x, to the loop and a large resistor, R_y, to the cut set. The resistors should be eliminated for the transient run since cut sets and loops are acceptable for the integration routine. It should be noted that a diode, instead of a resistor, can be used to prevent the formation of a cut set, as it does in the Ebers-Moll model.

Very small and very large passive element values should be avoided in Sceptre because of the time constant problem. Also, zero values of resistance, inductance, or capacitance will cause a run to terminate in Fortran. Because Sceptre can plot the current through voltage sources and the voltage across current sources, a zero-impedance element can be represented by a zero-value voltage source, and a zero-value current generator makes an ideal infinite-impedance element. Moreover, the diode capacitances in the Ebers-Moll model should not be neglected since their exclusion would cause solution errors. □

Optinet guides electronic products from design through marketing

Software system goes beyond usual optimization and analysis functions of CAD programs—helping users develop a prototype, control production, and dramatically expedite marketing procedures

by Robert Hall, *Dean Hall Associates Inc., Los Altos, Calif.*

☐ The various people involved in designing, building, and selling electronic equipment have various requirements—the engineers want to optimize design, the production staff aims for maximum efficiency, and the marketing men seek to reach the right customer. Now they have a software package that can satisfy all of their goals. Called Optinet, the program can be used to optimize circuit designs, keep track of production controls, and expedite marketing procedures.

Optinet includes a full set of computational facilities and uses them to perform modeling with variable parameters. Also provided is storage for models, solutions, and intermediate results, as well as commercial product data. Another feature is a dial-up access capability that brings the system to manufacturers and customers.

The software package is available through National CSS Inc., Stamford, Conn., and Sunnyvale, Calif. By next March, other time-sharing services are expected to offer the program.

Optinet generally requires a large computer facility on the order of the IBM 360/67. The program is written in Fortran 4. Though Optinet is one of the fastest and least-expensive analysis programs available, design analysis itself is not always the highest-priority consideration when introducing a new product. With its sensitivity analysis, worst-case diagnosis, production modeling, and market data capabilities, Optinet can cut costs and time involved in the critical process of transferring the product to the production and marketing stages.

Optinet is designed for devices, components, and subsystems that can be described in terms of piecewise-linear ac models. Additional modeling capability is added regularly so that the system will be able to handle dc, nonlinear and transient calculations sometime next year.

A closer look. Modeling with Optinet is straightforward. Networks are broken down into subnetworks, sections, and elements. A catalog of more than 75 elementary sections provides easy access to lumped, distributed, active, passive, analytical, numerical, and hypothetical models. Up to 15 networks can be defined simultaneously, each with its own frequency range and performance requirements, permitting modeling of piecewise-linear and multistate networks. A total of 15 elements in these networks may be identified as the variable parameters of the model.

Basically, Optinet requires three types of files—network, frequency, and performance—to solve an analysis problem. They are numbered to correspond to each other; for example, files N1, F1, and P1 form a set, as do files N2, F2, and P2. Up to 15 complete file sets are available. The network file gives the circuit description, the frequency file lists the frequencies of interest within a design band, and the performance file defines circuit requirements.

Data files (30 in all) are independent of the other files and contain values of frequency-dependent circuit elements or circuit specifications, which are defined in either a network or performance file. These data files can be used anywhere in the analysis.

A variable file is required for design, because the user must specify the circuit elements he is willing to vary to meet desired performance specifications. This file allows either a circuit element as called out in a network file or a circuit parameter as specified by a performance file to become a variable. Limits and nominal values for the variables are established by the file, which can contain up to 15 lines.

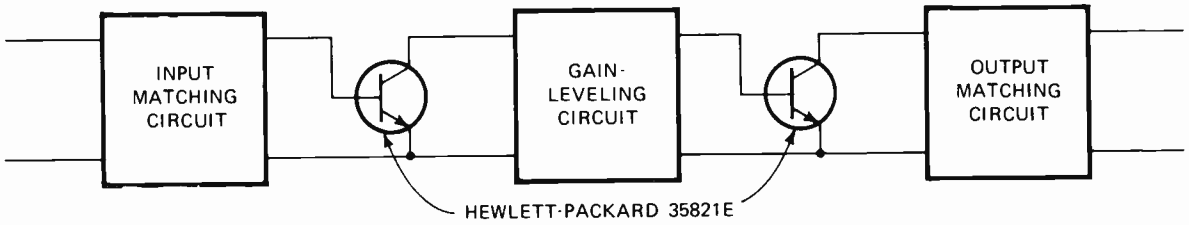
A criterion file is also required for Optinet's design capability and can have up to 15 lines. The criterion file defines a function that represents best circuit performance. The function usually has one form for performance optimization and another for worst-case analysis. For example, an optimization criterion could be a function whose minimum value represents best performance, while a worst-case criterion could be a function that goes to zero if desired specifications are not met.

Optinet provides a sensitivity analysis capability, too. It can vary individual parameters by any desired percentage and print the resulting variations of the performance requirements. A trace capability lets the user plot frequency-dependent performance as a function of a variable parameter over its entire range.

Ample storage facilities are another feature: up to 15 complete problem groups can be saved in a private disk area. When a problem group is retrieved, the contents of all files are reset exactly as they were when the problem group was saved. The problem then may be continued from the last result.

Information for use by multiple subscribers may be stored in read-only files for general access. The contents are retrieved by code names supplied along with the information at the time it is stored. These names also can

(a) AMPLIFIER BLOCK DIAGRAM



(b) TRANSISTOR CHARACTERIZATION

```
FORWARD NETWORK  2
AVERAGE VALUES

     GM      DB   = 6.49855
     R       OHM  = 19.0001
     X       OHM  = 10.2284
     RHM          = .470666

MAXIMUM VALUES

     GM      DB   = 9.39645 AT F = 1.6   GHZ
     R       OHM  = 20.2859 AT F = 3     GHZ
     X       OHM  = 16.3528 AT F = 3     GHZ
     RHM          = .48 AT F = 2.39999    GHZ

MINIMUM VALUES

     GM      DB   = 4.02796 AT F = 3     GHZ
     R       OHM  = 18.17 AT F = 1.6     GHZ
     X       OHM  = 4.14764 AT F = 1.6   GHZ
     RHM          = .469999 AT F = 2.1    GHZ
```

```
REVERSE NETWORK  5
AVERAGE VALUES

     GM      DB   = -19.0961
     R       OHM  = 39.0471
     X       OHM  = -46.3705
     RHM          = .482

MAXIMUM VALUES

     GM      DB   = -17.4579 AT F = 3    GHZ
     R       OHM  = 52.4157 AT F = 1.6   GHZ
     X       OHM  = -40.3198 AT F = 3    GHZ
     RHM          = .520001 AT F = 3     GHZ

MINIMUM VALUES

     GM      DB   = -21.2096 AT F = 1.6  GHZ
     R       OHM  = 28.2906 AT F = 3     GHZ
     X       OHM  = -52.9882 AT F = 1.6  GHZ
     RHM          = .46 AT F = 1.7       GHZ
```

1. Desired amplifier. Transistorized microwave amplifier (a) must supply gain of 12 decibels ± 1 dB and have 50-ohm input and output impedances from 1.6 to 3 GHz. Due to transistor transmission characteristics, gain-leveling and matching circuits can be separated. Important transistor properties are tabulated in (b) for forward and reverse performance.

be stored in a directory that can be printed out during any Optinet session.

The program uses a time-shared computer system primarily because it is the best choice of communications. Through time-sharing, Optinet can rapidly service scattered users by providing mutual access to models and performance criteria.

Furthermore, Optinet offers a number of convenience facilities. For example, it controls the cost of computation. Total dollar expenditure is reported on demand, and estimates of the cost of computation are available before the computation is run.

Information and diagnostics keyed to the current state of the problem may be obtained by typing "?". Successively deeper explanations are given when "?" is typed again. Also included is an adaptive editor to speed the flow of information, manage files, and adjust to the user's style.

Design example. How Optinet works is best illustrated by following a hypothetical project from design through marketing, and restricting the example to four basic areas: design, interpretation of measured data, production control, and marketing.

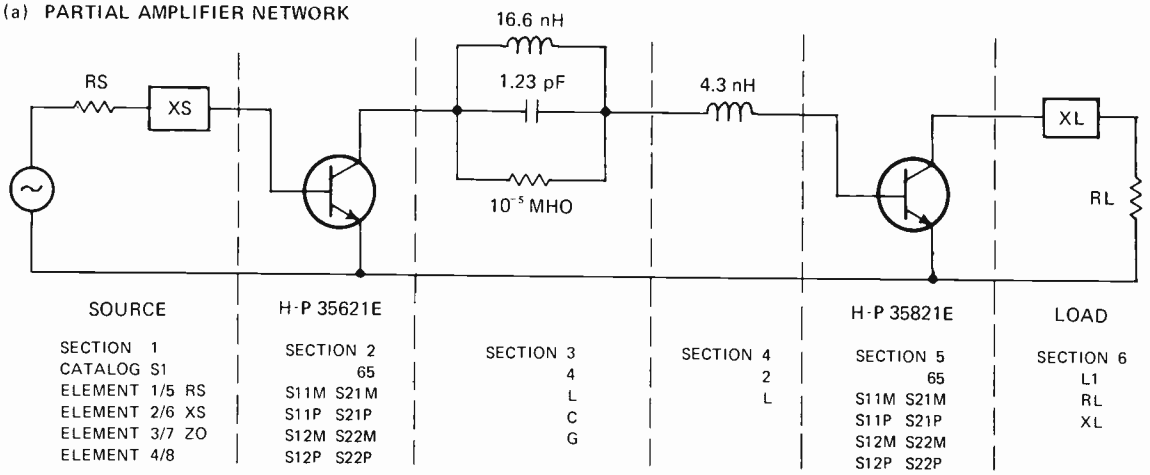
Suppose the desired product is a broadband amplifier that uses microwave transistors. Its specifications are: a minimum gain of 12 decibels with a flatness of ± 1 dB; a center frequency band of 2 to 2.5 gigahertz; a total bandwidth of 1.6 to 3 GHz; a minimal number of stages; and 50-ohm input and output impedances, with maximum reflection coefficients of 0.2.

Data on a suitable transistor is prestored in the Optinet public data file by the device's manufacturer. Using Hewlett-Packard's type 35821E transistor for this example, it is characterized in the file by S parameters at 15 volts and 15 milliamperes over a frequency range of 100 to 4,500 megahertz.

The major transistor design problems are gain variation and mismatched input and output impedances. Since this particular transistor has low reverse transmission, gain-leveling and matching circuits can be separated as shown in Fig. 1(a). Transistor properties relevant to the problem are computed from S parameters stored in the public file, as shown in Fig. 1(b).

Optinet describes the transistor for both forward (input) and reverse (output) characteristics. Average, maximum, and minimum values are tabulated for gain magnitude (GM), resistance (R), reactance (X), and reflection coefficient (RHM). Also noted is the frequency at which the value occurs as well as its units callout. For example, maximum input resistance is 20.2859 ohms at 3 GHz, while minimum output resistance is 28.2906 ohms at 3 GHz.

(a) PARTIAL AMPLIFIER NETWORK



SECTION 1
CATALOG S1
ELEMENT 1/5 RS
ELEMENT 2/6 XS
ELEMENT 3/7 ZO
ELEMENT 4/8

SECTION 2
65
S11M S21M
S11P S21P
S12M S22M
S12P S22P

SECTION 3
4
L
C
G

SECTION 4
2
L

SECTION 5
65
S11M S21M
S11P S21P
S12M S22M
S12P S22P

SECTION 6
L1
RL
XL

(b) NETWORK FILE

N2

SECTION	CATALOG	ELEMENT1/5	ELEMENT2/6	ELEMENT3/7	ELEMENT4/8
1	S1	50	0	50	
2	65	1C1D9	1C2D10	1C3D11	1C4D12
		1C5D13	1C6D14	1C7D15	1C8D16
3	4	16.6C12	1.23C9	1E-5	
4	2	4.3C10			
5	65	1D9	1D10	1D11	1D12
		1D13	1D14	1D15	1D16
6	L1	50	0		

(c) FREQUENCY FILE

F2

LINE	FREQUENCY
1	1.6
2	1.7
3	1.8
4	1.9
5	2
6	2.1
7	2.2
8	2.3
9	2.39999
10	2.49999
11	2.59999
12	2.69999
13	2.79999
14	2.89999
15	3

DATA FILE

D13

LINE	DATA
1	2.95
2	2.8
3	2.62
4	2.54
5	2.37
6	2.3
7	2.15
8	2.08
9	1.98
10	1.91
11	1.86
12	1.77
13	1.73
14	1.63
15	1.59

(d) VARIABLE FILE

V

LINE	COMMON	NEG-BOUND	POS-BOUND	VALUE
1	9	1	2	1.23
2	10	2	6	4.3
3	11	11	13	12
4	12	10	20	16.0

(e) PERFORMANCE FILE

P2

LINE	MEASURE	FORM	WEIGHT	REFERENCE	COMPARE
1	GM	PLOT	10	12C11	SQ
2	R	D1			
3	X	D2			

(f) CRITERION FILE

C

LINE	OPERATOR	SOURCES
1	SUM	P2

2. Gain-shaper. Partial amplifier (a) is described by its network file (b). Frequency file (c) sets test frequencies in operating band, while data file shows corresponding values of transistor gain. Variable file (d) establishes specification limits, performance file (e) defines amplifier gain requirements, and criterion file (f) optimizes gain flatness.

Of the several procedures that could be used to design the amplifier with Optinet, a very direct one is to first ignore input and output matching (since about the same amount of gain is lost across the entire band due to mismatching), and find approximate element values for an interstage circuit that provides adequate control over gain slope. Next, amplifier input and output impedances are computed and approximate element values for 50-ohm matching networks are found. Finally, the complete circuit is assembled, overall performance criteria are defined, and optimization is used to adjust the various element values for best performance.

The data in Fig. 1(b) indicates that the transistor's maximum input resistance and minimum output resistance nearly match at the high end of the operating frequency band if a series inductance is used to balance out reactance. It can also be seen that the gain rolloff, from a maximum of 9.4 dB at 1.6 GHz to a minimum of 4 dB at 3 GHz, is about 6 dB per octave.

Since there are two transistors, approximately 12 dB of gain rolloff must be introduced at the low end to flatten amplifier gain response. Thus, at least three reactive elements are needed to increase the gain control circuit's reactance slope. Values will be chosen to provide the flattest and highest gain within the operating band.

Figure (2a) illustrates a partial amplifier design and

Fig. 2(b) is its description. The network is partitioned into sections that correspond to lines in the network file and elementary sections in Optinet's catalog of subcircuits. Elementary sections are represented by mnemonics (like S1 and L1) or numbers in the catalog.

The mnemonics are listed in the CATALOG column of network file N2 to indicate which sections are needed. Certain element values are required to complete the section description. For example, Fig. 2(a) shows that section 1 contains a voltage source (S1), described by a source resistance (RS), a reactance (XS), and a characteristic impedance (ZO). These elements are assigned appropriate numerical values each time they are used, as done on the first line of the network file.

Eight S parameters are required to completely describe each transistor's performance at any frequency. The S parameters are complex numbers forming a 2-by-2 matrix, and are represented by mnemonics S11M through S22P (M is for magnitude, P for phase). The double-number designation fixes the S parameter's row and column location in the matrix. For instance, S11M is the magnitude of the S parameter in the first row and first column of the matrix; S21P is the phase of the S parameter in the second row and first column of the matrix. Because each transistor is described by identical S parameters, only one set of eight must be stored; these values go into data files D9 through D16.

Also included is a master numbering system for the circuit elements. Every network file has four ELEMENT columns, differentiated by numbers 1/5, 2/6, 3/7, and 4/8. A number is assigned to each element in a network section. For any single section, Optinet can accept up to eight elements, the maximum required to completely describe any network section. From the network file of Fig. 2(b), it can be seen that section 2 comprises elements 1 and 5 (1C1D9 and 1C5D13) through elements 4 and 8 (1C4D12 and 1C8D16).

Section 3 of the partial amplifier calls for catalog subcircuit number 4, which is a parallel inductance (L), capacitance (C), and conductance (G). Because the conductance merely accounts for minor parasitic losses, it is specified as $10\nu^5$ (noted as 1E-5 in Fortran) mho.

Program files. Network elements may be made variable and/or frequency-dependent. Figure 2(c) shows a frequency file; it gives the frequency points to be evaluated and the data file for S21M. The latter represents the variation of element S21M over the frequency range called for in frequency file F2. Whenever network performance is computed, the appropriate gain for S21M is chosen from data file D13. If the frequency of interest is 2 GHz on line 5 of the frequency file, corresponding gain is 2.37 on line 5 of the data file.

If an element value is stored in one of 25 special locations, called common storage locations, it can be used for several elements in a network and/or it can be made a variable parameter. To be stored in one of these locations, a flag designated by a mnemonic C1 through C25 must immediately follow the element's numerical value. Element values stored in this way act as multipliers.

Data files can be treated similarly. If data files are called out as shown for the eight S parameters (1C1 through 1C8) in line 2 of network file N2, the element value is the number stored in the selected common location multiplied by the appropriate data file entry.

The variable file of Fig. 2(d) specifies a set of variable parameters whose values are to be adjusted for best performance: up to 15 numbers of a maximum of 25 stored in common locations C1 to C25 can become variables. These are listed (by number) in the COMMON column. A range for each variable must be defined by listing its lower limit (NEG-BOUND) and upper limit (POSBOUND). Nominal variable values are called out in the VALUE column.

Variable file V presents the data for amplifier gain and the passive gain-leveling circuit elements shown in Fig. 2(a). Line 1 calls for the 1.23-picofarad capacitor stored in common location C9, line 2 the 4.3-nanohenry inductor in C10, and line 4 the 16.6-nH inductor in C12. Line 3 stores amplifier gain in common location C11 and confines its value to 12 ± 1 dB. Storage locations for gain-control elements are also noted in the network file.

Values of variables may be assigned or changed by making an appropriate entry in the variable file, as well as in any file where the common location is referenced. Variables are required for all of Optinet's higher computing functions, such as sensitivity analysis and optimization. During optimization, any changes in variable parameter values are readily examined by printing the variable file.

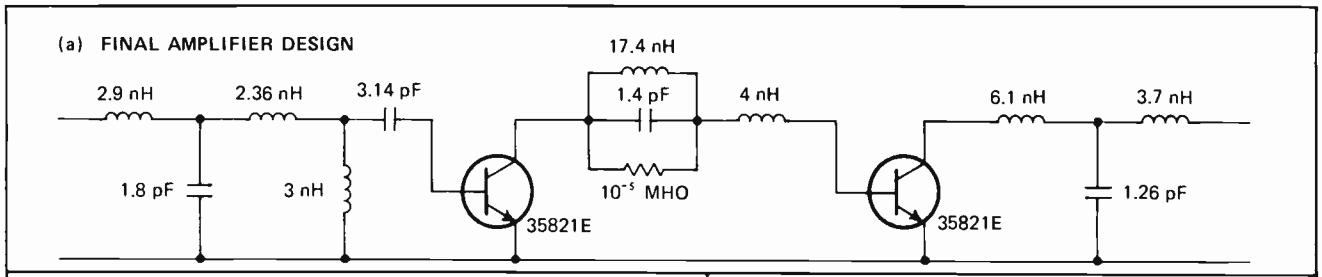
The performance file of Fig. 2(e) defines the proposed network's performance requirements. Line 1, for instance, requests the gain magnitude (GM) to be presented in the form of a plot versus frequency whenever the network is analyzed. The REFERENCE column cites the nominal value of the variable of interest (gain magnitude in this case) and its storage location. A callout of 12C11, for example, refers to the variable listed on line 3 of the variable file; its nominal value is 12 and it's stored in common location C11.

The gain affects the criterion function because its weight is positive (not zero). Weight value is assigned by the user and reflects the relative importance of the quantity being computed.

Two other factors influence the weight value. One is the magnitude of the quantity, and the other is how often it is computed during a run. Gain, for example, is computed 15 times (because of the 15 frequencies in the band) and has a high value of 10 to 15 dB. Reflection coefficient, however, is found only once in the band and has a low value of 0.1 to 0.2. To make these two quantities approximately equal in importance, the user could assign a weight of 1 to the gain and a weight of 1,500 to the reflection coefficient.

Since gain is specified as a point-by-point measure (PLOT) in performance file P2, it contributes a value to the criterion function at each point in the operating frequency band. This value is the WEIGHT (10) multiplied by the square (SQ) of the difference between the gain magnitude and the reference. The COMPARE column in the performance file indicates what mathematical operation should be carried out.

Minimizing the criterion value, WEIGHT $(GM\text{-}REF)^2$, will bring the gain closer to the reference at each point in the band. Since the reference is a variable parameter, an optimization search can adjust it to a value that gives the flattest gain curve.



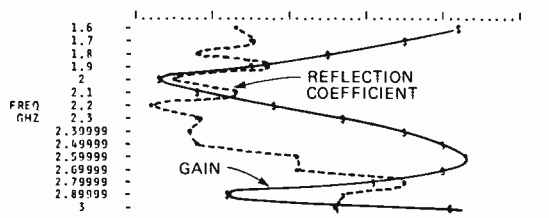
(b) NETWORK FILE

N2

SECTION	CATALOG	ELEMENT1/5	ELEMENT2/6	ELEMENT3/7	ELEMENT4/8
2	2	2.89173C16			
3	11	1.80025C17			
4	2	2.36116C18			
5	12	3.02681C19			
6	1	3.13776C20			
7	65	1C1D9	1C2D10	1C3D11	1C4D12
		1C5D13	1C6D14	1C7D15	1C8D16
8	4	17.412C12	1.39919C9	1E-5	
9	2	3.99244C10			
10	65	1D9	1D10	1D11	1D12
		1D13	1D14	1D15	1D16
11	2	6.0872C13			
12	11	1.25798C14			
13	2	3.71329C15			

(c) PERFORMANCE CHECK

```
FORWARD NETWORK  2
AVERAGE VALUES

     GM      DB  = 14.4017
     RHM         = .137713

MAXIMUM VALUES

     GM      DB  = 14.0977 AT F = 2.79999   GHZ
     RHM         = .216116 AT F = 2.59999   GHZ

MINIMUM VALUES

     GM      DB  = 13.997 AT F = 2.2   GHZ
     RHM         = .015975 AT F = 2   GHZ

PROCEED WITH PLOTS? (Y OR N): y

* GM    DB    13.95      14.25      14.55      14.85      15.15      15.45
$ RHM              0   .0500001         .1         .15         .2         .25
```



3. Optimum amplifier. Final optimization results in amplifier shown in (a) and described by network file (b). Optinet can also predict performance of finished amplifier. Performance check (c) notes that minimum gain is 14 dB at 2.2 GHz, and maximum input reflection coefficient is 0.22 at 2.6 GHz. Gain and reflection coefficients are plotted.

For optimization, only the first line of performance file P2 is used, because the other lines have no weights. When an analysis is run, the network gain magnitude is plotted, and network input resistance (R) and reactance (X) are automatically computed and stored in files D1 and D2 for use in solving the input matching problem.

The criterion file of Fig. 2(f) gives the final requirements for a function whose minimum represents best performance. Contributions from one or more performance files can be combined to create the criterion function in the way specified by the OPERATOR column. Possible operators are sum (SUM), maximum (MAX), and product (PRO). Sum and maximum are generally used for design purposes, while product is usually listed for worst-case analysis. Performance files to be combined to form the criterion function are listed in the SOURCES column.

First-order design. Now that the Optinet files needed for a solution are established, the amplifier design problem can be run. Figure 2 contains all the files needed to establish an interstage gain control circuit.

Next, an output matching network can be found by computing input and output impedances across the operating band. The complete first-order design is then optimized to produce the best performance.

The final amplifier design, its network file, and a final performance check are shown in Fig. 3. As indicated in Fig. 3(c), the amplifier's maximum reflection coefficient does not quite meet desired specifications; its value is 0.216 at 2.6 GHz. Minimum gain, however, exceeds the original design objective with a value of about 14 dB at 2.2 GHz. To improve the reflection coefficient, another computer run would be necessary and some degradation permitted in gain performance.

With the initial part of the product design finished, the time and expense incurred thus far can be examined. Slightly more than 24 engineering hours in addition to seven hours on a time-shared terminal are required. A reasonable time-and-cost estimate for the entire design task is about a week of engineering time and around $300 to $700 for computer time, including the investigation of alternative circuits.

The design is not complete until sensitivity and worst-case performance are checked. Optinet's sensitivity analysis indicates the change in network performance as each variable circuit element is individually increased by some small amount. Worst-case analysis predicts circuit performance if all the variables are changed simultaneously. For this amplifier, the key performance specifications are minimum gain and maximum input reflection coefficient.

For sensitivity analysis, these two performance measures are called for by altering performance file P2 as shown in Fig. 4(a). The variables to be changed are the gain and circuit elements whose optimized values are indicated for the amplifier of Fig. 3(a). Nominal value of each variable will be increased by 1%.

Figure 4(b) illustrates the results of the analysis (potentially troublesome areas are surrounded by boxes). Nominal values of gain and reflection coefficient are printed, along with the incremental change that occurs in these quantities when a given variable is increased.

Numbers 1 through 11 correspond to the variables listed on the same-number lines in the variable file.

A 1% increase in variable 1, the 1.4-pF capacitor in Fig. 3(a), causes a 0.003 increase in the reflection coefficient and a 0.07-dB increase in the gain. For this design example, an increase in any variable causing more than a 1% change in a performance measure is considered potentially troublesome. Therefore, any increment greater than 0.002 in the reflection coefficient and greater than 0.14 in gain is surrounded by a box in Fig. 4(b). (Note that gain performance never goes out of specification; taken as a whole, the amplifier design is satisfactory.)

The cost of sensitivity analysis is usually nominal (under $10 in this case). The analysis not only pinpoints the elements that may need to be adjusted in the final design but also helps to define acceptable tolerances on other elements. And it could be useful to overdesign a circuit by using more than the minimum number of circuit elements, thereby reducing all of their sensitivities.

Worst-case analysis is the next step. Optinet can determine what specifications will not be met, at what frequencies in the band, as well as for what combinations of component values and value tolerances. The necessary files are given in Fig. 5(a); these must be used along with the network file of Fig. 3(b).

Worst-case analysis. For the amplifier example, the worst-case criterion function must go to zero if the desired specifications are not met at any point in the band. The variables in the variable file are normalized values of the eight S parameters that characterize each transistor. The boundary values shown reflect a ±10% tolerance as specified by the manufacturer.

Performance file P2 places an upper bound (UB) on minimum gain to assure that the first term in the criterion function will be 0 if the gain falls below 13 dB. Line 2 of the file sets a lower bound (LB) for the maximum reflection coefficient to make certain that the second term of the criterion function is 0 if the maximum reflection coefficient in the band exceeds 0.33. The product operator (PRO) in the criterion file sets the criterion function equal to the product of the terms in file P2.

When the worst-case performance objectives defined by the performance file are exceeded, Optinet terminates the search and prints the results as shown in Fig. 5(b). The normalized S parameters that cause worst-case performance are listed in the VALUE column of a new variable file. (Note that none of the worst-case S parameter values exceed their specified tolerance.)

According to the analysis, the reflection coefficient will be 0.346 at 3 GHz and, therefore, not within specification. Minimum gain, however, stays within design objectives—its value is 13.9 dB at 1.8 GHz. Worst-case analysis always identifies the frequency with the poorest performance.

When the limit for the maximum reflection coefficient is changed to 0.5, gain variation is emphasized. Running through worst-case analysis again yields the results shown in Fig. 7(c) and a different set of S-parameter values. Gain will be just over 13 dB at 2.2 GHz and still within specification. Reflection coefficient also meets the desired limit with a value of 0.346 at 3 GHz. Cost for this worst-case analysis is about $55.

(a) PERFORMANCE FILE FOR SENSITIVITY ANALYSIS

```
P2
 LINE  MEASURE  FORM   WEIGHT     REFERENCE   COMPARE
   1     GM     MIN
   2     RHM    MAX
```

(b) SENSITIVITY ANALYSIS RESULTS

```
FORWARD NETWORK  2
     PERFORMANCE                INCREMENT DUE TO 1% CHANGE IN VARIABLE
PARAMETER    VALUE                  1          2          3          4
MAX  RHM    .216116    [.003296138]  [.00365709]      0      5.02765E-4
MIN  GM     13.997      .0704467      .0468922        0      .0151348

     PERFORMANCE                INCREMENT DUE TO 1% CHANGE IN VARIABLE
PARAMETER    VALUE                  5          6          7          8
MAX  RHM    .216116    .00141782  1.80125E-4  -7.512E-4  [.00443208]
MIN  GM     13.997     .00505447   .00344276  -.00498772  -.00266947

     PERFORMANCE                INCREMENT DUE TO 1% CHANGE IN VARIABLE
PARAMETER    VALUE                  9          10         11
MAX  RHM    .216116    .00186241  8.47638E-4  .00172377
MIN  GM     13.997    -.00534058   .00244141  -.00295639
```

4. Sensitivity analysis. Performance of final amplifier is checked for sensitivity to changes in individual variables. A 1% increase in each variable is introduced separately. Performance file (a) indicates that gain and reflection coefficient should be tested. Results in (b) have possible trouble spots noted with a box.

The worst-case performance study indicates the S parameters that should be avoided at specific frequencies for acceptable amplifier performance. Variations in transistor parameters generally are compensated for by adjusting circuit elements, and Optinet can determine appropriate ranges and parameters.

Another application for the Optinet system is interpretation of measured data. The program can determine the values of the variable model parameters that provide the best fit between computer and measured data. Using this feature requires that a bench model of the Optinet-designed amplifier be built and tested.

Because of tolerance ranges in purchased components, it's highly unlikely that the test data for the prototype will accurately match predicted performance. But Optinet accepts the measured performance data and finds the new variable values needed to make measured performance match the computed. The program indicates those parts of the circuit responsible for any discrepancy and notes corrective action required.

Implementing this Optinet feature involves using the same files that are employed for design. However, the measured data is stored in data files to establish amplifier performance for each frequency in the band. These data files are then listed in the REFERENCE column of a performance file. Optinet will automatically adjust circuit element values to achieve the best match for the reference (measured) data. The user then can determine those elements that require adjustment and by what amount.

Production modeling. Transferring a product from development to production usually causes many problems. Some can be reduced or even eliminated if both an Optinet model and prototype are available to production personnel.

A study of the prototype quickly shows what tolerance must be held and what performance changes occur, with certain circuit element variations. As pilot

(a) FILES DEFINING WORST-CASE ANALYSIS

```
V
 LINE   COMMON   NEG-BOUND   POS-BOUND    VALUE
   1        1          .9         1.1        1
   2        2          .9         1.1        1
   3        3          .9         1.1        1
   4        4          .9         1.1        1
   5        5          .9         1.1        1
   6        6          .9         1.1        1
   7        7          .9         1.1        1
   8        8          .9         1.1        1

P2
 LINE  MEASURE  FORM  WEIGHT  REFERENCE  COMPARE
   1      GM     MIN      1         13       UB
   2     RHM     MAX    100        .33       LB

C
 LINE  OPERATOR  SOURCES
   1      PRO      P2
```

(b) WORST-CASE ANALYSIS RESULTS

```
V
 LINE   COMMON   NEG-BOUND   POS-BOUND    VALUE
   1        1          .9         1.1     .999343
   2        2          .9         1.1     .945808
   3        3          .9         1.1     1.0627
   4        4          .9         1.1     .949303
   5        5          .9         1.1     .990328
   6        6          .9         1.1     .980838
   7        7          .9         1.1     1.02744
   8        8          .9         1.1     1.04963

FORWARD NETWORK  2
MAXIMUM VALUES

     RHM          = .346239 AT F = 3    GHZ

MINIMUM VALUES

     GM      DB   = 13.9353 AT F = 1.8   GHZ
```

(c) MODIFIED WORST-CASE ANALYSIS

```
V
 LINE   COMMON   NEG-BOUND   POS-BOUND    VALUE
   1        1          .9         1.1     1.04319
   2        2          .9         1.1     .915946
   3        3          .9         1.1     1.07918
   4        4          .9         1.1     1.03349
   5        5          .9         1.1     .912463
   6        6          .9         1.1     .904025
   7        7          .9         1.1     1.00344
   8        8          .9         1.1     .921671

FORWARD NETWORK  2
MAXIMUM VALUES

     RHM          = .324711 AT F = 3    GHZ

MINIMUM VALUES

     GM      DB   = 13.0834 AT F = 2.2   GHZ
```

5. Worst-case analysis. If all circuit variables are changed at the same time, amplifier performance can be checked for worst-case conditions. Files (a) define worst-case gain (GM) and reflection coefficient (RHM) when transistor S parameters are varied by ± 10%. Printouts (b) and (c) show results.

models are built and checked. Optinet can interpret test data for the adjustment of the production process to provide target performance. Optinet also can even continuously monitor production so that drifts can be corrected before the product goes out of specification.

Optinet also can compensate for variations in state-of-the-art components that may be the only devices available for a given production run. With an Optinet production model of the whole product, data on the doubtful parts can be entered into the program. Optinet then will investigate the corrective action possible through controlled changes in other circuit parameters.

Another consideration in production modeling is answering requests for quotations that involve some deviation from standard performance. It may be difficult to determine quickly whether these special specifications can be met on the production line. With Optinet, the special specifications can be used in the optimization routine. Knowing the best values for the elements and the best performance obtainable can greatly improve bidding accuracy and production planning.

Marketing. The final step in developing a new product is marketing. Through its public data file, Optinet can make this task easier, as well as reduce time and expense for both seller and buyer. Since the program is available through a time-shared network, any subscriber has easy dial-up access to the public file and, therefore, to the Optinet product model. A potential customer can explore the properties of the product or even run through a complete design, as was done here with the Hewlett-Packard transistor.

Instead of spending months exchanging samples, building prototypes, and trying to agree on mutually acceptable product performance, the manufacturer and his customer can trim this exploratory period to a matter of weeks. Costs, too, are dramatically reduced because less engineering time is needed.

Suppose a conventional sample-and-build period is about three months. Engineering costs, including support and overhead expenses, normally would be about $10,500. Optinet could reduce the time factor to two weeks, dropping engineering costs down to $1,750. Adding about $700 for computer time brings the total expenditure to $2,450, a significant saving.

Since Optinet's public data file has the same capacity as its working file, there is ample space to store product data, frequency ranges, performance properties, and component tolerances. The amplifier example could be represented explicitly by its network file description. Or the circuit's two-port performance may be given in terms of S parameters or any other equivalent numerical description.

If an Optinet subscriber already has a model in his private files, it can be transferred to the public disk without charge and stored for $10 to $20 per month. The public file can be updated from subscribers' private files at any time.

As the Optinet system grows in scope, the catalog of products in its public data file also will grow. It should be remembered, however, that the program's most up-to-date source of product information is its directory, which can be listed simply by giving a command during an Optinet terminal session. □

Program calculates load effects of high-speed digital circuits

Digital interconnections are analyzed by program called Line as if they were transmission lines; from a minimum of input data it accurately computes line voltage, plots ringing characteristics

by Laurence P. Flora, *Burroughs Corp., Pasadena, Calif.**

☐ High-speed digital circuitry often lands its designer with the job of analyzing the loading effects, like circuit ringing and delay, that result from line discontinuities. This analysis is highly complex, and requires a computer's speed and accuracy.

However, it has to be performed in terms of transmission line equations, and ECAP (electronic circuit analysis program) and its equivalents are really only satisfactory for standard lumped-constant circuitry. A lumped-element model doesn't fit transmission lines too accurately. Besides, the programs take an extremely long time to solve even moderately complex problems of this nature.

To help the engineer plot an accurate analysis of a high-speed transmission line, a program called Line was recently developed. It's based on a general load configuration that represents all circuits to be used in the systems under study. It also is based on what the general load effects are when a unit step or unit ramp function is transmitted down the line, and closely approximates any reflection without reference to the line's history from time zero. The program, which is written in Fortran, is conversational, and can be run on a time-shared terminal. In contrast to existing computer programs, Line can precisely analyze a transmission line problem, but it cannot handle a general circuit consisting of various lumped components.

Line makes use of the accurate, yet general, load configuration of Fig. 1. Besides being an adequate representation of the circuits used in most systems, this RC network may also model a purely resistive discontinuity (i.e., when $R_2 = \infty$) or purely capacitive discontinuity ($R_1 = \infty$, $R_2 = 0$, and $R_3 = \infty$).

Computing the reflection

To understand how Line solves for general load effects, consider the response of a line to a unit step or a unit ramp function. These two forcing functions are chosen since either provides a good approximation for most input waveforms.

For the load of Fig. 1, the reflection voltage due to a unit step function is:

$$[V_r(t)]_{step} = K_2 + (K_1 - K_2)e^{-t/r} \quad (1)$$

while a reflection voltage due to a unit ramp function can be expressed as:

$$[V_r(t)]_{ramp} = K_2 t + r(K_1) - K_2)(1 - e^{-t/r}) \quad (2)$$

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where:

$$K_1 = (R_2R_3 - Z_oR_2 - Z_oR_3)/(R_2R_3 + Z_oR_2 + Z_oR_3)$$

and:

$$K_2 = (R_1R_3 + R_2R_3 - Z_oR_1 - Z_oR_2 - Z_oR_3)/(R_1R_3 + R_2R_3 + Z_oR_1 + Z_oR_2 + Z_oR_3)$$

and:

$$r = C_1(R_1R_2R_3 + Z_oR_1R_2 + Z_oR_1R_3)/(R_1R_3 + R_2R_3 + Z_oR_1 + Z_oR_2 + Z_oR_3)$$

and Z_o is the line output impedance.

Now the solution can be generalized, and computation time minimized. Since the reflection voltage may assume an infinite number of waveforms, the final solution must be some approximation that produces accurate results from a minimum of information. With such an approximation, comparatively little need be known about the line's immediate past history, and the complexity due to multiple reflections is minimized.

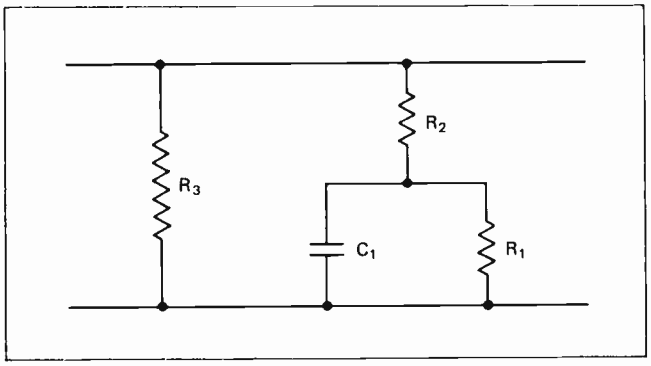
Of course, any waveform can be approximated as a series of small steps. But a better approach in this context is to use a series of small ramps, since this is nearly an exact approximation of a pulse with a finite risetime and falltime — the usual shape of waveforms transmitted over lines in high-speed digital systems.

Assume that the input waveform is a ramp with a slope of A volts per second up to time T_1. Then, at T_1, the slope increases by an amount B, which gives a new slope of A + B. By superposition, reflection voltage is:

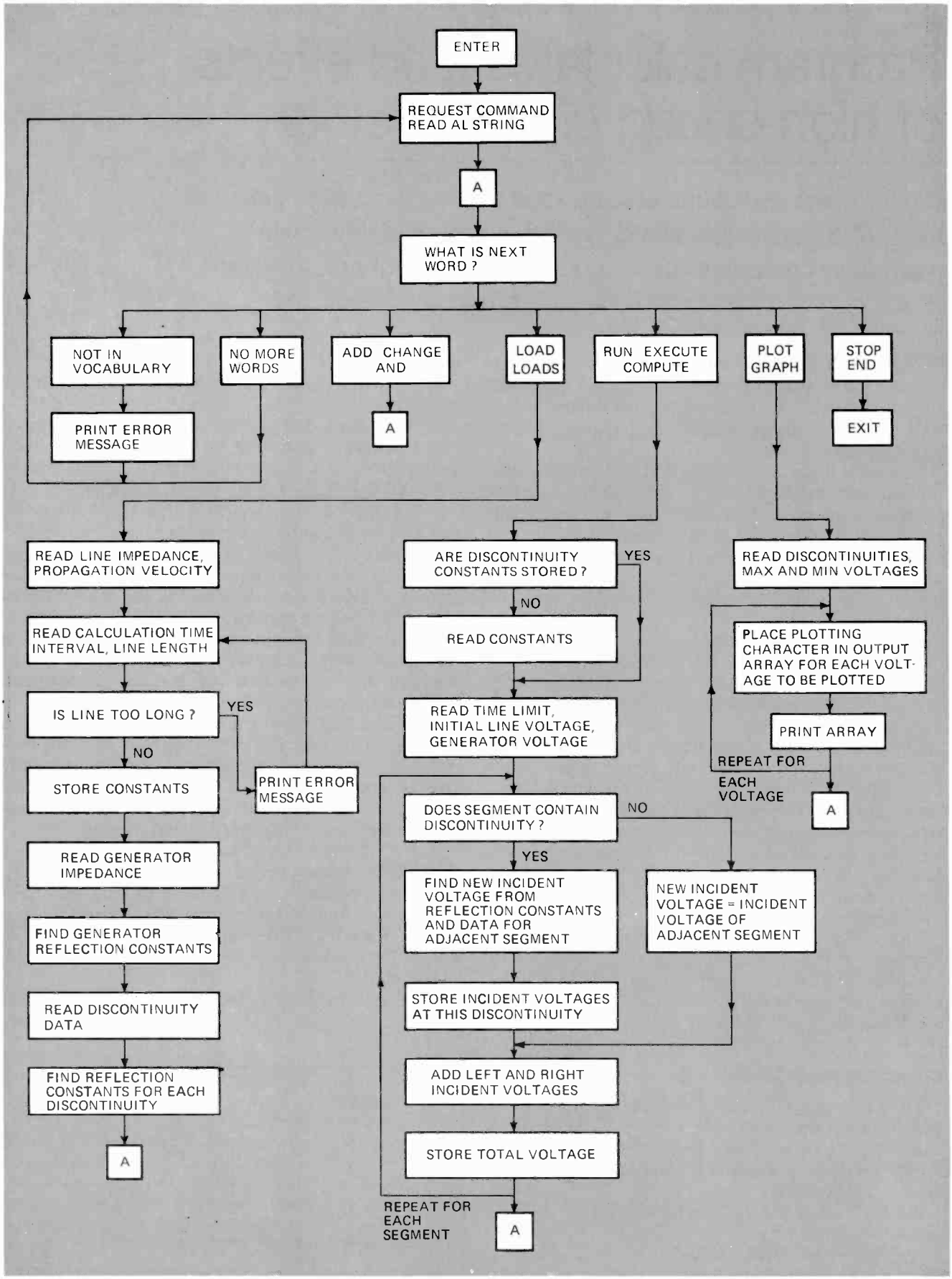
$$V_r = A[V_r(t)]_{ramp}U(t) + B[V_r(t - T_1]_{ramp}U(t - T_1)$$

where U(t) is a unit step function, and $U(t - T_1)$ a delayed unit step.

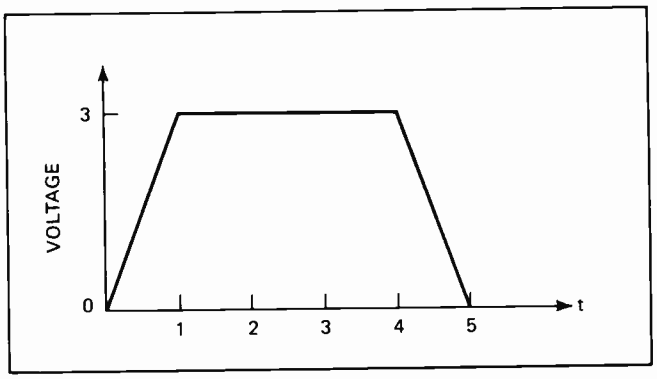
The forward voltage at time T_1, which is represented



1. General load. RC network accurately represents most loaded transmission lines in high-speed digital systems. When $R_2 = \infty$, it is resistive; when $R_1 = \infty$, $R_2 = 0$ and $R_3 = \infty$, it is capacitive.



2. Flow chart. Once initial data is entered, Line computes incident voltage and reflection constants for each line segment, storing only incident and transmitted voltages from previous adjacent segment. There are three basic instructions: LOAD (describing physical line properties), RUN (establishing initial electrical conditions), and PLOT (graphing reflection voltage at several load points).



3. Input voltage. Line accepts input waveforms as piecewise linear functions with up to 20 breakpoints. For example, the voltage waveform shown is described by an initial value (0,0) and four breakpoints with coordinate locations of (1,3), (4,3), (5,0), and (10,0).

by $V_f(T_1)$, can be expressed as:

$$V_f(T_1) = A\left[K_2T_1 + r\left(K_1 - K_2\right)\left(1 - e^{-T_1/r}\right)\right]$$

And the final equation for the reflected voltage is:

$$V_r = V_f(T_1)e^{-dt/r} + (A + B)[V_r(dt)]_{ramp} + (AT_1)[V_r(dt)]_{step} - (AT_1)(K_1 + 1)e^{-dt/r} \quad (3)$$

where:

$V_f(T_1)$ = forward voltage at the end of the last time interval

$V_r(dt)_{ramp}$ = the unit ramp reflection of Eq. 2

$A + B$ = the new ramp slope

$V_r(dt)_{step}$ = the unit step reflection of Eq. 1

AT_1 = the incident voltage at the end of the last time interval

dt = the time interval.

Note that only two pieces of information about the line's history need be saved for the next calculation—the incident voltage, AT_1, and the transmitted voltage, $V_f(T_1)$, at the end of the last time interval.

Using the results

To program Eq. 3 into a computer, the values of circuit variables R_1, R_2, R_3, and C_1, or mathematical variables K_1, K_2, and r must be stored. Also, the input waveform must be represented in memory, for example, by a table of voltages or by an equation.

The reflected and transmitted voltages are calculated at each discontinuity, but need to be stored for only one time interval. However, it is convenient to save the transmitted voltage for each interval since the instantaneous line voltage is the sum of two transmitted voltages (one for each direction). Some provision should also be made for the distance between loads so that the transmitted voltage (plus the reflected voltage due to the voltage incident in the opposite direction) reaches the next load after a suitable time delay.

The program Line reads the values of R_1, R_2, R_3, and C_1, and calculates and stores K_1, K_2, and r. The input waveform is described by a piecewise linear function that has up to 20 breakpoints. Total line voltage at each discontinuity is also stored and can be plotted. The computation interval is determined from the resolution requested by the user; it is the output time interval divided by 10. This allows a very close approximation of any waveform, including a step with a fast risetime.

The instruction sequence for Line is shown in the flow diagram of Fig. 2. To start the program, the command RUN LINE (or equivalent instruction, depending on the time-sharing system used) is used. After this, there are three operating instructions that can be repeated as many times as desired.

Operating instructions

The first of these is LOAD or LOADS, which allows the user to describe the line's physical properties. For proper operation, Line requires the line impedance, the propagation velocity on the line, how often (at what time intervals) the voltages should be computed, the total length of the line, the impedance of the driving generator, and the positions and values of loads on the line.

To describe a load for Line, load position (distance from the generator), and the values of R_1, R_2, R_3 and C_1 must be entered. Up to 19 loads can be accommodated. Constants representing the loads are saved in a disk file.

Any consistent set of units may be used. For instance, the system of ohms, feet, seconds, and farads is acceptable, and velocity would then be entered in feet per second. But this system may be cumbersome, and a more convenient set of units is kilohms, inches, nanoseconds, and picofarads. Velocity is then expressed in inches per nanosecond. (It should be noted that the unit of capacitance multiplied by the unit of resistance must be consistent with the unit of time.)

The second operating instruction describes the incident voltage waveform, and uses the command RUN, EXECUTE, R, E, or COMPUTE. For this computation, Line requests the maximum time for which the voltages are to be computed, the initial line voltage, and the breakpoints of the input voltage waveform. For instance, an input voltage like the one illustrated in Fig. 3 would be described by initial voltage (0, 0) and breakpoints (1,3), (4,3), (5,0), and (10,0).

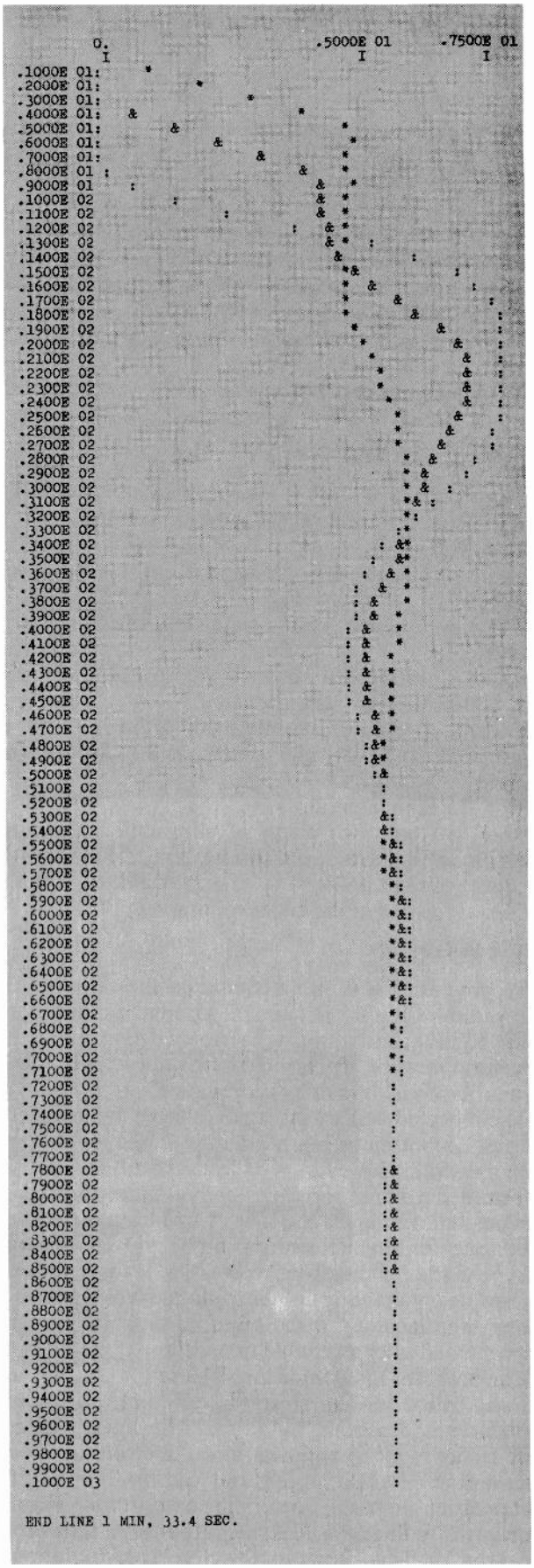
The time at which the last breakpoint occurs must be equal to or greater than the maximum time for which the voltages are computed. When this last breakpoint is entered, Line calculates the voltage waveforms at every load and writes them in a disk file.

If one of the commands describing the incident voltage is given before the physical properties of the line have been established (through a LOAD command), an error message is typed. When this occurs, the command RUN LINE must be entered again.

The third and last operating instruction, PLOT or GRAPH, causes Line to graph the voltage at one or more of the load points. If several separate plots are desired, the command must be given several times. Line prints each load's number and position, and asks for the number of waveforms the user wants plotted, plus the numbers of those loads for which plots are desired.

Along with the load numbers, Line lists load positions, and the typewriter character with which each load will be plotted. Finally, the program asks for the desired minimum and maximum voltage scale for each plot. All plots are superimposed. If either the PLOT or GRAPH command is given before the voltage waveforms have been computed, an error message is printed, and the command RUN LINE must be given again.

```
RUN LINE
 RUNNING

WHAT IS YOUR COMMAND?ADD LOADS

WHAT IS THE LINE IMPEDANCE?.100

WHAT IS THE PROPAGATION VELOCITY?8

AT WHAT TIME INTERVALS DO YOU WANT THE VOLTAGES?1

HOW LONG IS THE LINE?60

THE LINE WILL BE BROKEN INTO SEGMENTS  .800E 00 LONG.
WHAT IS THE IMPEDANCE OF THE GENERATOR?.020

DISCONTINUITIES ARE OF THE FORM R1 IN PARALLEL WITH
C, ALL IN SERIES WITH R2, ALL IN PARALLEL WITH R3.
INPUT LOAD POSITION, C, R1, R2, AND R3.
INPUT 5 ZEROS IF NO MORE DISCONTINUITIES.
?1,0,1000,1000,1000
?12,10,1000,.100,1.0
?24,5,1000,.200,2.0
?36,15,1000,.067,.667
?48,5,1000,.2,2
?60,10,1000,.1,1
?0,0,0,0,0

WHAT IS YOUR COMMAND?RUN

VOLTAGES WILL BE COMPUTED FOR EVERY
 .100E 01 INCREMENT IN TIME.
WHAT IS THE MAXIMUM TIME?100

WHAT IS THE INITIAL LINE VOLTAGE?0

INPUT WAVEFORM BREAKPOINTS BY ENTERING
TIME,VOLTAGE
?5,5
?100,5

THE VOLTAGES AT THE DISCONTINUITIES HAVE
BEEN WRITTEN IN THE OUTPUT FILE LINEV.

WHAT IS YOUR COMMAND?PLOT AND STOP.

NUMBER       1     2     3     4     5     6
POSITION  0.80 12.00 24.00 36.00 48.00 60.00
HOW MANY VOLTAGES DO YOU WANT PLOTTED?3

INPUT THE NUMBERS OF THE DISCONTINUITIES
AT WHICH THE VOLTAGES ARE TO BE PLOTTED.
?1,3,6

  DISCONTINUITY     PLOTTING
NUMBER   POSITION   CHARACTER
   1     .800E 00       *
   3     .240E 02       &
   6     .600E 02       :
WHAT ARE THE MINIMUM AND MAXIMUM VOLTAGES?0,10
```



4. Line example. Sample program and plot shows total line voltage versus time for three points of discontinuity along a line. Different typewriter characters represent the three ringing waveforms, which are plotted at 1-nanosecond intervals.

A RUN command may be given several times, as can the PLOT command. RUN causes Line to find the response of the loaded line to different input waveforms. Either STOP or END terminates the program.

It is also possible to obtain the voltage response at some point on the Line where there is no load, without affecting voltage at that point. The user simply inserts a load where desired by letting R_2 and R_3 be several orders of magnitude larger than the line impedance.

To make Line's commands more readable, punctuation and the words ADD, CHANGE and AND may be used. Then a simple command to completely describe a problem, compute the waveforms, obtain a plot, and stop would be: ADD LOADS, RUN, PLOT AND STOP.

Figure 4 is a sample run of the program to find the ringing characteristics of a line at three points of discontinuity for 100 nanoseconds. Total line voltage is plotted at 1-ns intervals along the line. The program restricts minimum and maximum voltage excursions to 0 and 10 volts, respectively, if the line voltage exceeds these limits. □

Printed copies of Line are available at $0.75 each from the author, Laurence P. Flora, 40 Highland Ave., Cambridge, Mass. 02139.

Computer helps design of complementary MOS logic

Accurate characterization of MOSFET current-voltage curve permits computer modeling of silicon-gate C/MOS logic circuits; switching performance of both combinational and sequential logic circuitry can be predicted or analyzed

by James Foltz and Fuad Musa, *Motorola Semiconductor Products Inc., Phoenix, Ariz.*

☐ Complementary metal-oxide-semiconductor logic circuitry is being more widely used as the demand increases for digital systems that operate at low power levels and from low supply voltages. C/MOS satisfies these requirements with its extremely low dynamic power dissipation and its essentially zero quiescent power consumption. Moreover, silicon-gate C/MOS can operate from very low supply voltages—as little as 1 volt, thereby further reducing power requirements.

Complementary logic structures, however, can become quite complex, making the use of computer-aided analysis essential, since the basic C/MOS logic element, the inverter, requires two devices—an n-channel and a p-channel MOS field-effect transistor. To use the computer, a practical model of the silicon-gate MOSFET is needed that satisfies C/MOS requirements.

The model must be suitable for both transient analysis and determining the effect of MOS device parameters, especially threshold voltage, on circuit performance. As threshold voltage becomes smaller, operating speed can be increased, but possibly at the price of higher power consumption.

The MOSFET model

Because of its simplicity and accuracy, the low-frequency large-signal equivalent circuit of the MOSFET (Fig. 1) provides a good basis for developing the appropriate equations for C/MOS computer analysis. Through Sceptre, a general-purpose computer program, and MOSFET current and voltage relationships, this equivalent circuit can be used to predict C/MOS switching speed, power dissipation, and the effect of threshold voltage on transient response and power-speed product.

The MOSFET model is a four-terminal device consisting of drain-source current generator I_{DS} and five capacitors that represent the device's gate-source C_{GS}, gate-drain C_{GD}, gate-substrate C_{GB}, drain-substrate C_{DB}, and source-substrate C_{SB} capacitances. For an n-channel MOSFET, current flows from the drain terminal to the source terminal; for a p-channel transistor, current flows from source to drain.

Model capacitors C_{DB} and C_{SB} represent junction capacitances and can be evaluated readily by conventional methods. However, since C_{GS}, C_{GD}, and C_{GB} are MOS gate-oxide capacitances, they are functions of processing parameters and device geometry, as well as MOSFET terminal voltages. Although the sum of these latter capacitances is constant, their individual values vary with biasing conditions and also depend on the direction of current flow between drain and source terminals. Detailed descriptions of how to evaluate MOS capacitances are available.[1,2,3,4]

This model does not account for any source or drain series resistances because the effect of these resistances can be neglected, due to the extremely low current developed by the MOSFET at silicon-gate C/MOS operating voltage levels. (Peak current is about 100 microamperes, while drain-source voltage approximately equals the 1.5-v gate-source voltage).

Characterizing the model

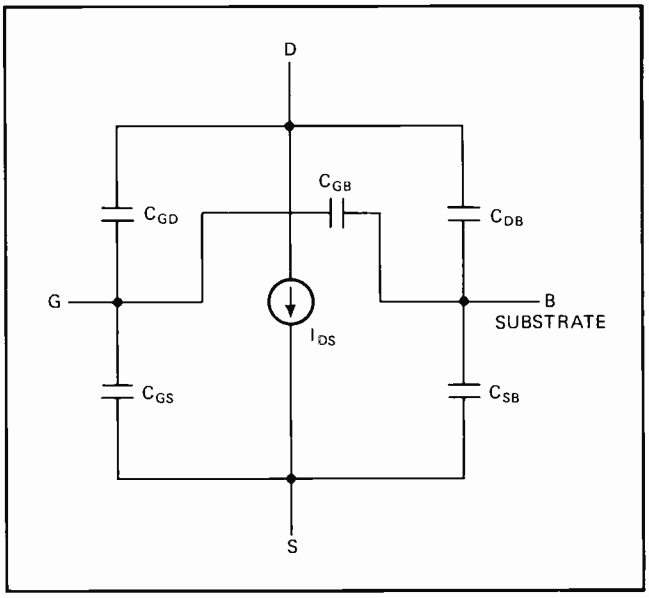
In the linear region, the current generator, I_{DS}, can be written as:[5,6,7]

$$I_{DS} = B_o[(V_G - V_o - V_D/2)V_D - (V_G - V_o - V_S/2)V_S - (2/3)K_o(|V_D + 2\phi_F|^{3/2} - |V_S + 2\phi_F|^{3/2})] \quad (1)$$

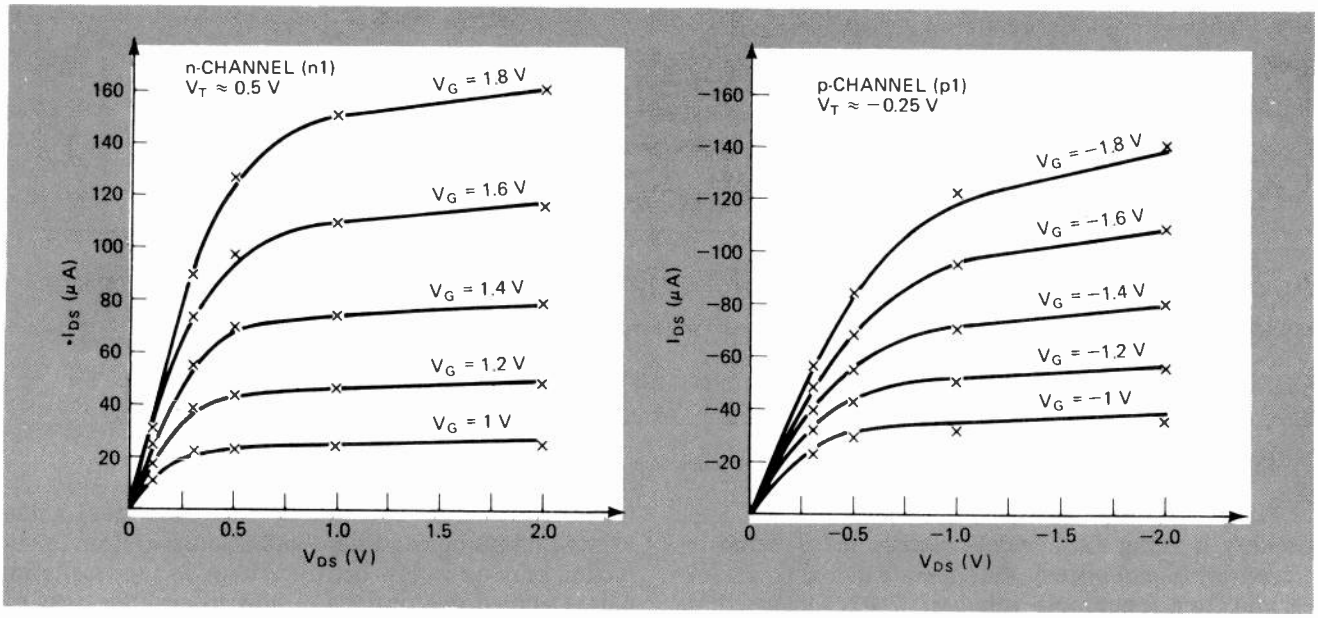
where all voltages are referenced to substrate potential:

$$B_o = Z\mu C_o/L$$

$$V_o = \phi_{MS} - Q_{SS}/C_o + 2\phi_F$$

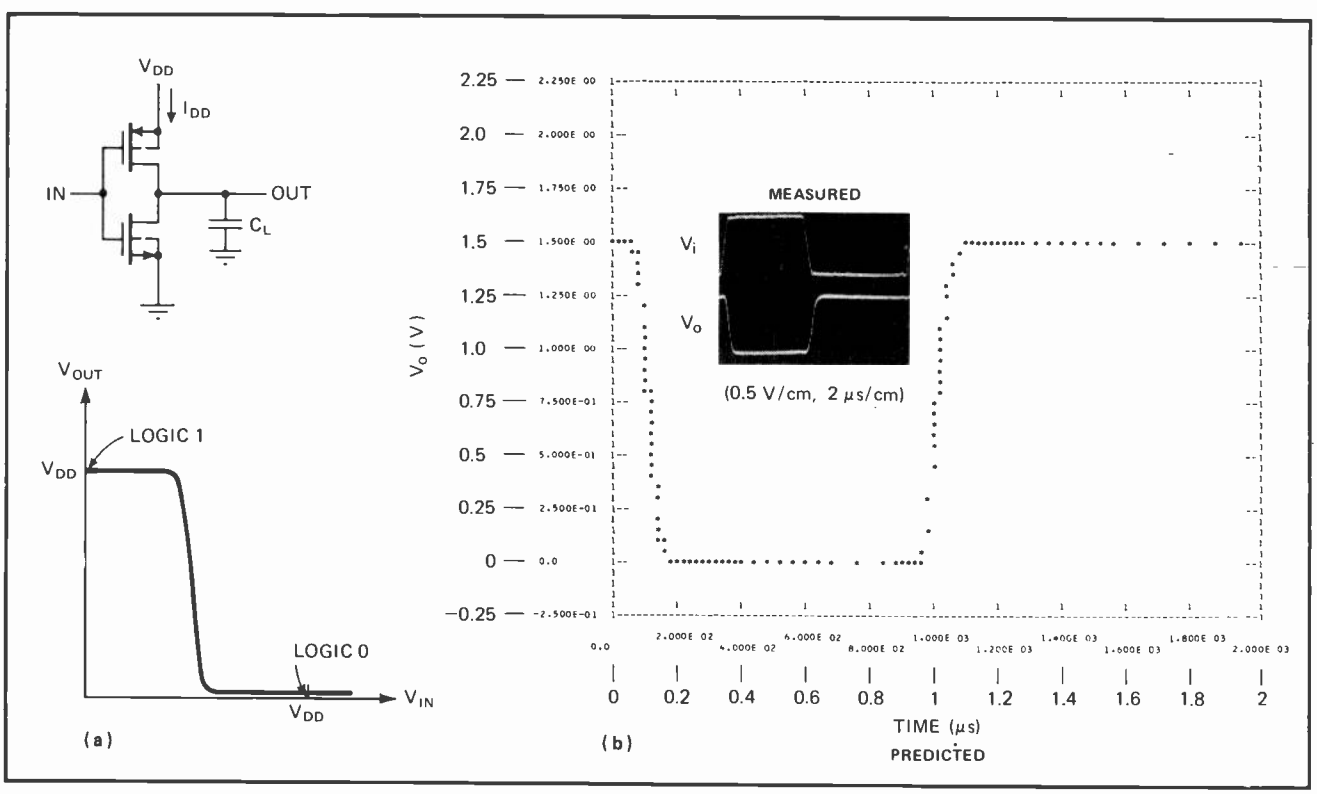


1. MOSFET model. Low-frequency large-signal equivalent circuit of MOSFET serves as model for complementary MOS logic. Equation for current generator, I_{DS}, represents model's current-voltage characteristic, which can be applied to C/MOS design or analysis. Current flows from drain to source for n-channel device.



OPTIMIZED PARAMETERS							
Device type	B_o (A/V^2)	V_o (V)	N_D (cm^{-3})	X_o (microns)	Q_{SS}/C_o (V)	L (microns)	V_T (V)
n1	2.85×10^{-4}	−0.57	4.3×10^{15}	0.117	0.27	3.9	0.48
p1	-1.4×10^{-4}	0.24	1.1×10^{15}	0 115	0.30	5.2	−0.25
n2	8.9×10^{-4}	−0.68	1.12×10^{16}	0.122	0.24	20.0	1.20
p2	-3.49×10^{-4}	0.14	4.72×10^{15}	0.122	0.33	25.0	−1.0

2. Mathematical versus practical. Device parameters needed to compute model current, I_{DS}, are noted in table for small (nl and pl) and large (n2 and p2) transistors. Parameters are mathematically optimized to approximate the current-voltage characteristics of real devices. I-V curves for nl and pl MOSFETs embody the comparison of predicted results (solid lines) with measured data (test points).



$K_o = (2\varepsilon_o\varepsilon_S qN_D)^{1/2}/C_o$

V_G is the gate voltage, V_D the drain voltage, V_S the source voltage, Z the channel width, L the channel length, μ the inversion layer mobility, C_o the gate-oxide capacitance per unit area, ε_o the permittivity of free space, ε_S the relative dielectric constant of silicon, N_D the substrate impurity concentration, ϕ_{MS} = he meta semiconductor work function difference, Q_{SS} the fixed positive charge at the silicon/silicon-oxide interface, ϕ_F the Fermi substrate potential, and e the electron charge.

In the saturation region, V_{DSAT} replaces V_D in Eq. 1 and is defined by:[5]

$$V_{DSAT} = V_G - V_o \pm (K_o^2/2[1 - (1 \pm 4(V_G - V_o + 2\phi_F)/K_o^2)^{1/2}]^{1/2} \quad (2)$$

(In Eq. 2, where a choice is indicated, the sign is + for n-channel and - for p-channel.) To simplify computations, the channel conductance in the linear region, g_{ds}, can be regarded as a linear function of V_G, provided that $V_S = 0$ and V_D) is much less than $2\phi_F$:

$$g_{ds} = \left.\frac{dI_{DS}}{dV_D}\right|_{V_D = \text{constant}} = B_o(V_G - V_T)$$

where threshold voltage V_T is:

$$V_T = V_o + K_o(2\phi_F)^{1/2}$$

When channel conductance g_{ds} is plotted against gate voltage V_G for an actual MOS device, the value of variable B_o (slope) becomes smaller with increasing gate voltages. This is due to reduced surface mobility and to the series source resistance, which lowers the gate-source voltage below the applied gate voltage. For all silicon-gate MOSFETs, variable B_o can be approximated by a constant when V_G is less than or equal to 2 V.

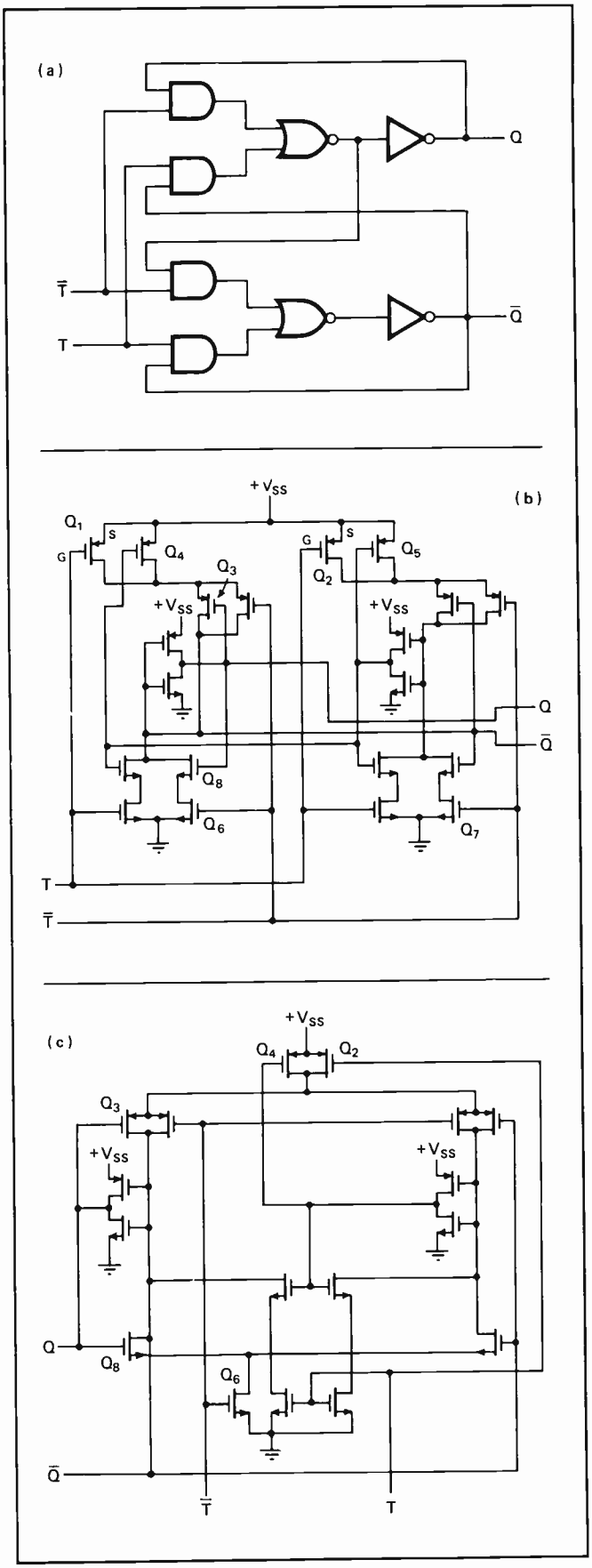
Modeling C/MOS logic

A computer-aided technique can be developed to optimize the values of Qss, V_o, oxide thickness X_o, channel length L, and impurity concentration N_D so that the current-voltage relationships calculated with Eqs. 1 and 2 closely approximate those measured for practical silicon-gate C/MOS devices.

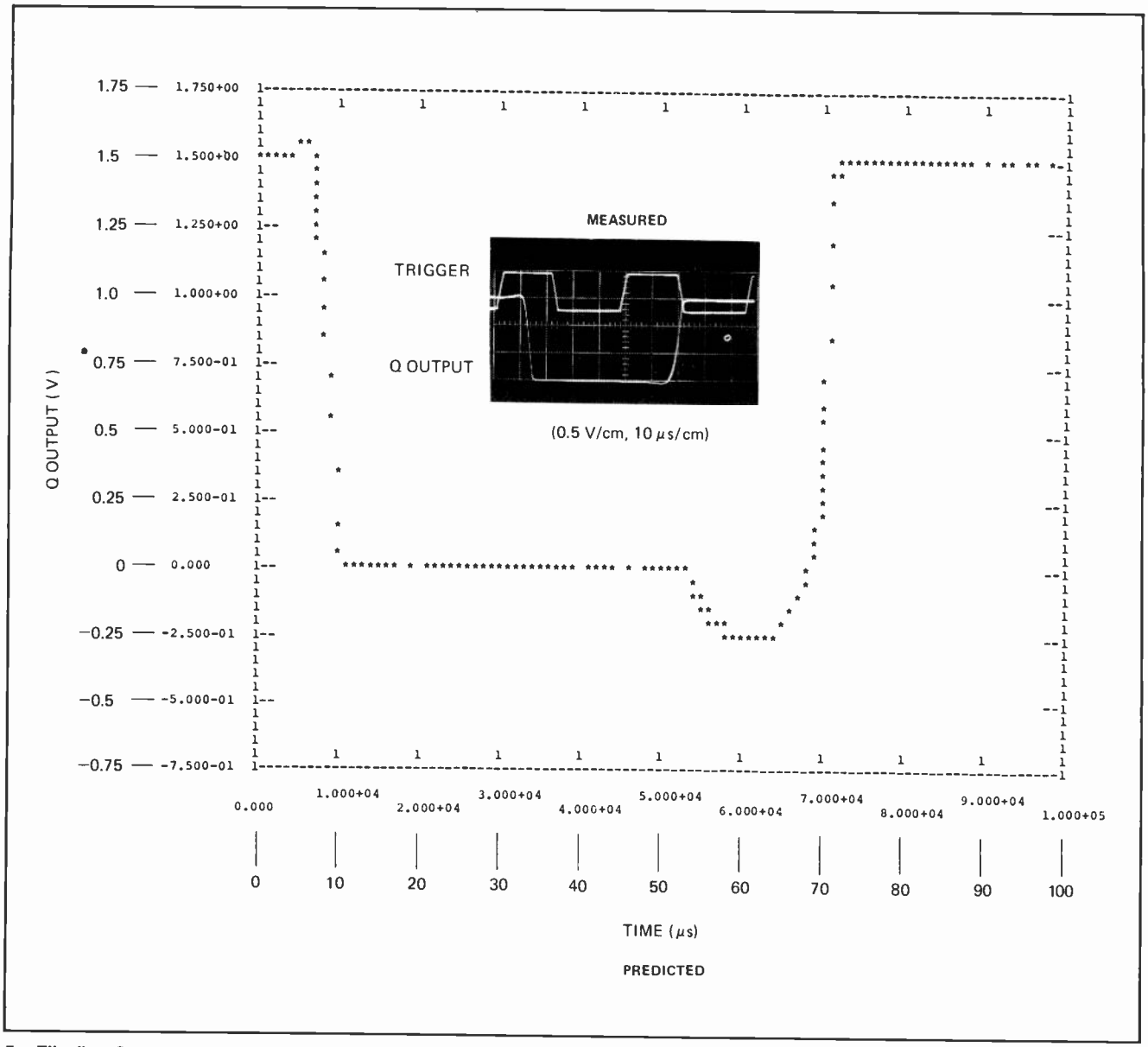
The table in Fig. 2 lists the most important optimized parameters for two pairs of n-channel and p-channel MOSFETs. The upper two sets of values, n1 and p1, are for small transistors, while the lower two, n2 and p2, are for large transistors. Both the predicted (with the model's equations) and the actual (from existing transistors) current-voltage characteristics of devices n1 and p1 also appear in Fig. 2. The differences between the predicted and the measured curves are small.

The basic element of the C/MOS logic family is the inverter, which is shown in Fig. 3a along with its transfer characteristic. Figure 3b shows the inverter's predicted and measured switching performance. The printout reflects the computed switching speed, based on the optimized parameters of transistors n1 and p1. And the oscilloscope trace displays the switching action of a circuit

3. C/MOS logic inverter. Basic C/MOS logic element is inverter (a) comprising p-enhancement MOSFET (top) and n-enhancement MOSFET (bottom). Voltage transfer function shows transition from logic 1 to logic 0. Computer plot (b) of output voltage versus time projects inverter switching performance using n1 and p1 parameters. Scope display is for inverter built with nl and pl MOSFETs.



4. Minimizing device count. Flip-flop (a) requires 20 MOSFETs, as shown in (b). But three transistors are redundant and can be removed—one between either Q_1 or Q_2, another between Q_4 or Q_5, and the third between Q_6 or Q_7. Final flip-flop (c) uses 17 MOSFETs.



5a. Flip-flop Q output. Predicted switching performance is plotted by computer for Q output of toggle flip-flop that is simulated with n2 and p2 parameters of Fig. 2. Oscilloscope trace displays same Q output for actual flip-flop built with practical n2 and p2 MOSFETs.

built with actual nl and pl transistors. Each switching waveform is the voltage across load capacitor C_L (2 picofarads) when the inverter is operated from a 1.5-v dc supply and is driven by a 1.5-v input having 100-nanosecond rise and fall times.

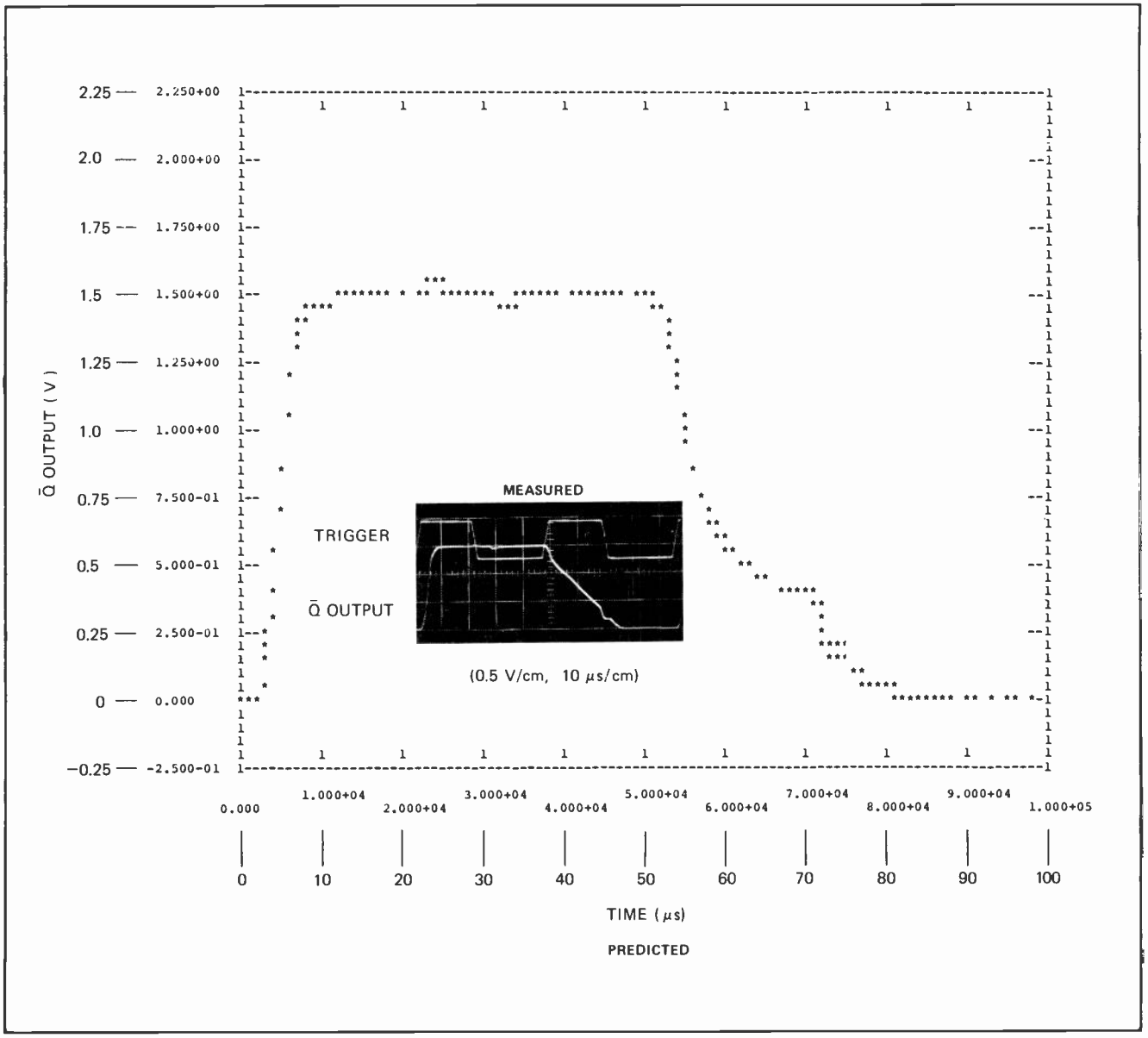
Power-speed product

One of the most important performance parameters of any switching circuit is its power-speed product; power consumption and operating speed are directly proportional to each other. Here, the C/MOS inverter has the advantage of dissipating power only during its transition, when charging or discharging its load and internal capacitances. However, I^2R power may be dissipated if both MOSFETs conduct simultaneously during transition, when the supply voltage and the input signal amplitude exceed the sum of the n- and p-channel threshold voltages. Dissipated power then becomes a function of input rise and fall times and increases with slower signals. Therefore, the C/MOS inverter's power-speed product, which is defined as $V_{DD}I_{DD}$/frequency, may not necessarily be constant with frequency if the input signal is sinusoidal or has varying rise and fall times. The MOSFET model can be used to predict the power-speed product by employing a function subroutine in conjunction with Sceptre[8] to calculate the average inverter current drain, I_{DD}.

For example, if an inverter's sum of threshold voltages is about half a 1.5-v supply, its power-speed product goes up by a factor of four when input rise and fall times are increased from about 0.1 microsecond to around 5 μs. The power-speed product for an inverter having a sum of threshold voltages that is greater than the supply does not change with slower inputs.

Sequential logic circuits

In addition to combinational logic, sequential C/MOS logic circuit performance can also be predicted with the MOSFET equivalent circuit. Sequential circuits can be considered as interconnected combinational logic



5b. Flip-flop Q̄ output. Computer predicts switching action of flip-flop Q̄ output by plotting output voltage versus time. Again, device parameters of n2 and p2 MOSFETs are used to simulate flip-flop. Switching performance of practical flip-flop is shown by scope trace.

blocks, like gates and inverters, with appropriate feedback. A toggle (type T) flip-flop, for example, can be implemented with the blocks noted in Fig. 4a.

In this form, the flip-flop requires 20 transistors, as indicated in Fig. 4b. A closer inspection, however, reveals that a few transistors serve the same functional purpose.

P-enhancement transistors Q_1 and Q_2, for instance, have identical bias conditions; their gates and sources are common. One of these transistors can be eliminated when the drains of the two have been tied together. This is possible, since their common drains will be buffered from the logic output node by transistor Q_3.

The same reasoning applies to transistors Q_4 and Q_5, since their drains are also common, once Q_1 and Q_2 are tied together. Moreover, transistors Q_6 and Q_7 have an identical biasing arrangement, allowing one of them to be eliminated after connection of their drains, which will be buffered from the output by transistor Q_8. In all, three devices are redundant and may be removed. The final flip-flop, Fig. 4c, requires 17 transistors.

The MOSFET model can be employed to predict the switching performance of the toggle flip-flop, as was done for the inverter. The parameters of MOSFETs n2 and p2 can be used for computation, and actual n2 and p2 transistors can be used to breadboard the flip-flop.

Both the predicted and measured Q and Q̄ output forms are noted in Fig. 5, when each output drives a 7-pF load. The longest part of the switching cycle, about 20 μs, is the fall time of the Q̄ output, Fig. 5b. □

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Aedcap: the circuit designer's computer-assisted slide rule

This powerful conversational software system solves circuit problems easily; designs can be analyzed quickly for dc, ac, and transient analysis, and their sensitivity to component tolerances can also be determined

by Ronald A. Rohrer and Jorge E. Rodriguez, *SofTech Inc., Waltham, Mass.*

☐ Although the virtues of computer-aided circuit design are well known by now, most engineers still avoid using the computer because they don't know how to interface with the machine. A year-old fully conversational computer program called Aedcap, however, allows the designer to communicate with the computer in an instruction-reply format that is written in engineering terms.

Available on a time-shared basis, Aedcap (Automated Engineering Design Circuit Analysis Program) provides as much analytical power as batch-processed software packages while making efficient use of computer time to hold down design costs. Circuits can be treated as prototypes being probed with an instrument.

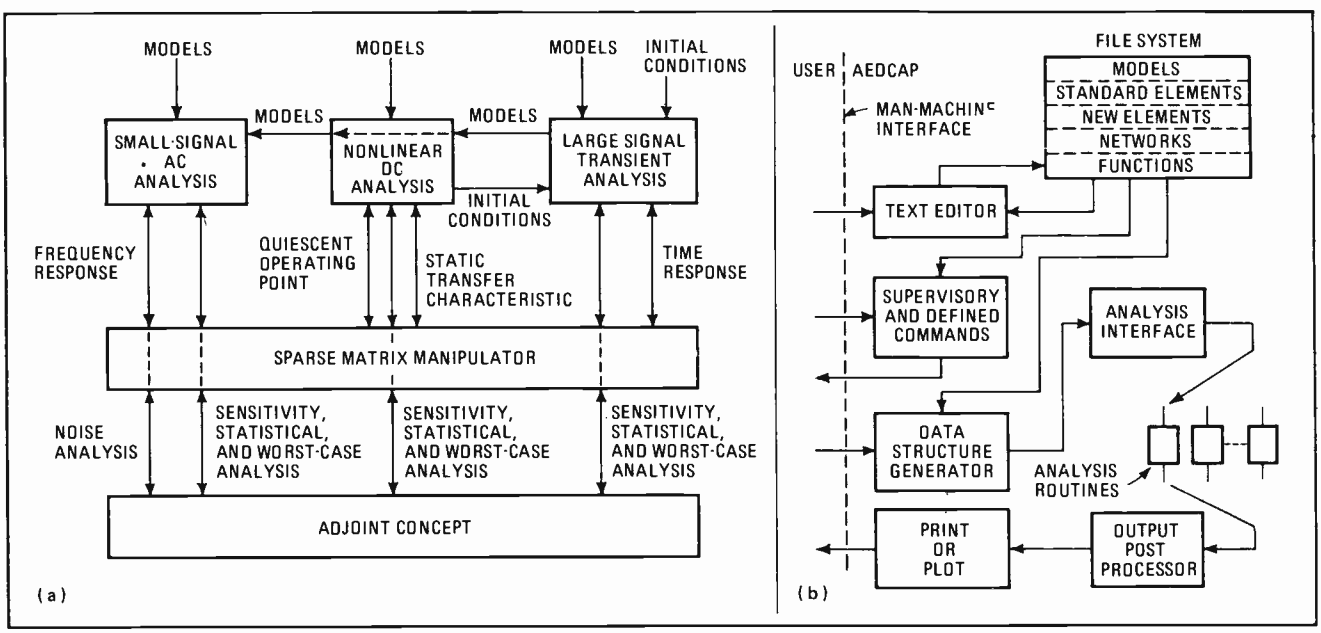
Aedcap can perform linear and nonlinear dc analysis, small-signal ac analysis, and large-signal transient analysis. All three analysis modes can be easily intercoupled. Moreover, the roles of signals and parameters can be interchanged so that a single computation can assess accurately the effects of every circuit parameter perturbation on a selected signal.

The program can simulate circuits composed of linear resistors, capacitors, and inductors; independent voltage and current sources; voltage-controlled current sources; junction diodes; bipolar junction transistors; and MOS and junction field-effect transistors. Theoretically, there is no limit to the size of the circuit Aedcap can accommodate, but, from a practical point of view, circuit size is restricted by the amount of computer memory available. Presently, hundreds of circuit nodes can be analyzed in a single computer run.

Models are built-in

Diode and transistor models are predefined; the user merely specifies the electrical parameters that characterize the active device. If the user chooses to leave a parameter value unspecified, the program inserts a default value, which usually simplifies the model.

Once characterized, a model can be stored so that it can be called out by name when needed to describe a circuit. Models for physical devices are used to reduce the circuit being described to N nodes (not including



1. Framework. Flowcharts map Aedcap's analysis (a) and control (b) structures The program can perform dc, ac, or transient analysis, as well as sensitivity, statistical, or worst-case analysis. Sparse matrix (one having many zero-valued entries) conserves computer time; adjoint network technique permits reversing roles of signals and parameters. Aedcap's interactive framework eases interface between user and computer. Conversational language and built-in active device models keep program instructions simple.

the datum or ground node) and B branches. Each branch is defined by a relationship between the branch current and the branch voltage. The unknown circuit variables are the N node voltages.

Aedcap employs nodal analysis to solve circuit problems. The program applies Kirchoff's current law at each node to produce a set of N independent equations in matrix form. A large circuit often has a nodal admittance matrix that is typically 75% to 95% sparse. (Sparsity denotes the percentage of zero-value entries in the matrix). The sparse matrix approach saves computer time. Flow charts for Aedcap's analysis and control structures are presented in Fig. 1.

To perform dc analysis, Aedcap replaces capacitors and inductors by open and short circuits, respectively, and then solves the circuit for fixed source values. A set of static transfer characteristics can be obtained by solving for sequential values of a given source.

Of course, dc analysis is used to determine a circuit's quiescent operating point so that linearized model parameters can be computed for small-signal ac analysis. Nonlinear elements are then replaced by linearized equivalents, and the resulting linear circuit is solved at sequential frequency points.

Large-signal transient analysis is used to determine the time-domain response of a circuit to various input waveforms, starting with the initial conditions found with a dc analysis.

Full sensitivity analysis capability

Aedcap allows the user to perform dc or ac sensitivity analysis, finding the change in a circuit output parameter caused by variations in one or more circuit elements. Since dc or ac sensitivity analysis is an inherent part of any dc or ac solution, its presentation does not require a new solution of the circuit. Worst-case analysis and statistical analysis are also available as part of a dc or ac solution.

Worst-case analysis computes the output degradation that will occur if all the element parameter tolerances vary collectively in the most pessimistic possible manner. A design that passes this test may be used with the utmost assurance that it will function properly.

Statistical analysis with Aedcap predicts the percen-

Bipolar transistor model

Aedcap offers a built-in bipolar junction transistor model that is an extension of the Ebers-Moll charge-control model used by most programs. The model includes an emission coefficient in each exponential term that characterizes a junction. Additionally, three series parasitic resistances and an output resistance augment the dc transistor characterization, while nonlinear capacitors model the base and depletion layer charge storage. A linear collector-substrate capacitance is also added to complete the modeling of transistor charge-storage effects.

The circuit shown is an npn transistor model. It is characterized by six equations—two defining junction currents I_{BE} and I_{BC}, and the other four defining capacitances Q_{BE1}, Q_{BE2}, Q_{BC1}, and Q_{BC2}:

$$I_{BE} = I_{ES}[\exp(qV_{BE}/n_{BE}kT) - 1]$$

$$I_{BC} = I_{CS}[\exp(qV_{BC}/n_{BC}kT) - 1]$$

$$Q_{BE1} = C_{jE0}\int_0^{V_{BE}} dV/(1 - V/\phi_{BE})^{1/2}$$

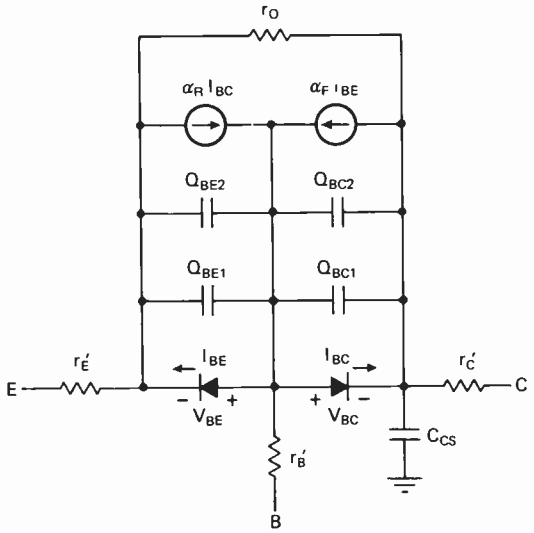
$$Q_{BE2} = \alpha_F \tau_F I_{BE}$$

$$Q_{BC1} = C_{jC0}\int_0^{V_{BC}} dV/(1 - V/\phi_{BC})^{1/2}$$

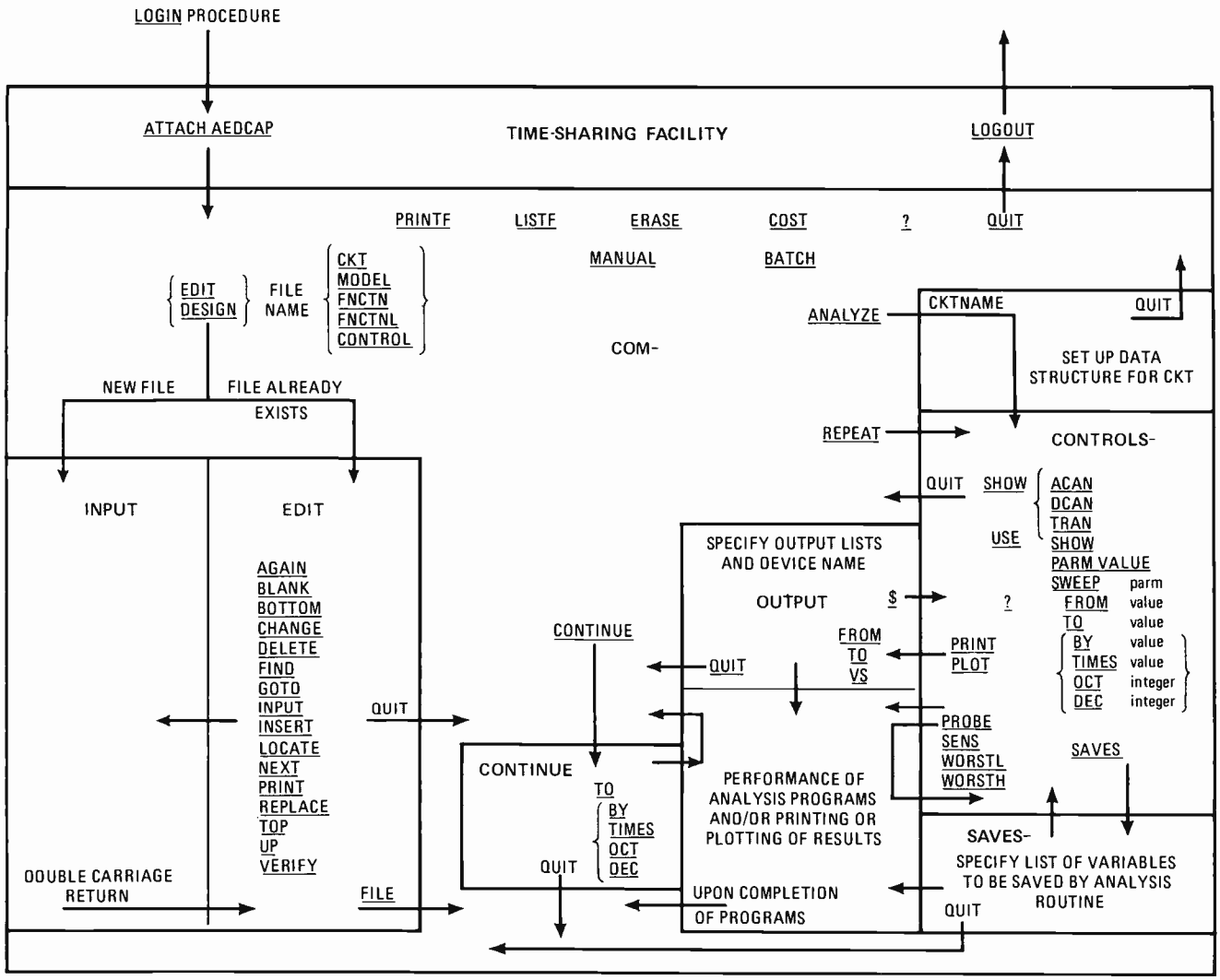
$$Q_{BC2} = \alpha_R \tau_R I_{BC}$$

In all, 18 parameter values are needed. Default values are put in by Aedcap when parameters are not specified.

For a pnp transistor, polarity is reversed for voltages V_{BE} and V_{BC}, currents I_{BE} and I_{BC}, and dependent generators $\alpha_R I_{BC}$ and $\alpha_F I_{BE}$. Voltages V_{BE} and V_{BC} coincide with terminal potential differences only when the voltages across resistors r_B', r_C', and r_E' are negligible.



TRANSISTOR PARAMETERS			
Parameter Symbol	Aedcap Name	Parameter Name	Default Value
Type		Transistor type, npn or pnp	
β_F	BF	Forward common-emitter current gain	100
β_R	BR	Reverse common-emitter current gain	1
r_B'	RB	Base ohmic resistance	0
r_C'	RC	Collector ohmic resistance	0
r_E'	RE	Emitter ohmic resistance	0
C_{CS}	CCS	Collector-substrate capacitance	0
τ_F	TF	Forward transit time	0
τ_R	TR	Reverse transit time	0
C_{jE0}	CJE0	Zero-bias base-emitter capacitance	0
C_{jC0}	CJC0	Zero-bias base-collector capacitance	0
I_{ES}	IES	Base-emitter saturation current	1×10^{-14}
I_{CS}	ICS	Base-collector saturation current	2×10^{-14}
n_{BE}	NBE	Base-emitter emission coefficient	1
n_{BC}	NBC	Base-collector emission coefficient	1
ϕ_{BE}	PHIBE	Base-emitter junction potential	1
ϕ_{BC}	PHIBC	Base-collector junction potential	1
r_O	RO	Output resistance	∞



2. Road map. Using Aedcap does not require special skills. Road map charts basic chain of command and shows how they are related to each other. The three primary command areas are COM-, controls, and input/edit. Instructions typed on terminal by user are underlined.

tage of circuits that will be out of tolerance in a production run. This analysis is a variation of sensitivity analysis that yields a simulated standard deviation of the desired circuit output parameter. The standard deviation figure gives a tolerance or voltage deviation within which roughly two-thirds of the circuits in a production run will fall. Before his design is firm and the production line set up, the designer can learn what his yield is likely to be.

In practice, Aedcap's statistical analysis has only limited accuracy. But, taken in conjunction with other design uncertainties, the predictions Aedcap makes can be useful to engineers engaging in statistical design.

Instructions are conversational

Three types of commands are available to the Aedcap user. The road map of Fig. 2 outlines the instructions included in each major command area. Control commands, for instance, are the various analyses that may be performed, while input/edit commands are the instructions needed to describe or modify circuits. The central command area, designated as COM-, provides access to the controls and input/edit sections, and also contains several auxiliary commands.

Sitting at his computer terminal, the user logs into the time-sharing network and then gains access to Aedcap by typing ATTACH AEDCAP. The system responds with the word COM-, signifying that it is ready to accept any command listed in the COM- area on the road map. (User-supplied commands are underlined).

The designer then calls for a circuit already filed in the system, or he describes a new circuit. He may do this by typing DESIGN AMPLIFIER CKT, if "amplifier" is the formal name by which he wishes to file his circuit. The system then searches for any circuit with this name. If it does not find one, the system notifies the user, who may then proceed to describe his circuit.

After executing any edit commands given by the user, the system returns to the COM- area, from which the user can exit with the command ANALYZE. ANALYZE precedes requests for the various analysis routines listed under controls. When the analysis is complete, the system returns to COM-. If he wishes, the user may now terminate the session and log out to study his results. The circuit he has just analyzed may be filed in the Aedcap system for future reference or for subsequent additional analysis.

Pointing out some limitations

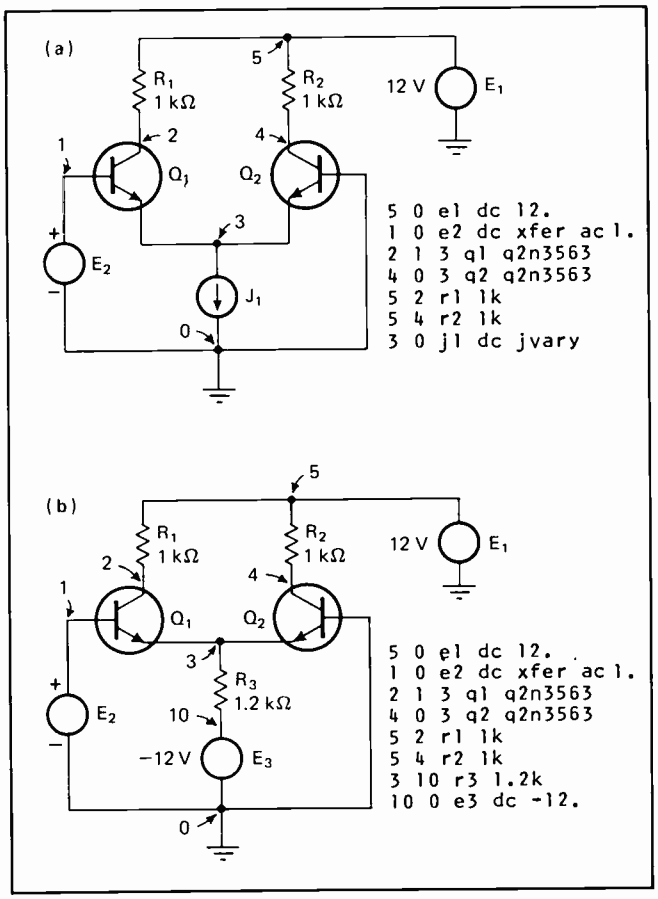
Parameter determination and modeling are still two of the most significant limitations to the effective application of circuit-simulation systems. Aedcap attempts to

minimize these problems with a large model library. Device models can be stored permanently and made available for future designs and other engineering users.

Although Aedcap's built-in bipolar junction transistor model (see panel) is adequate for most circuit applications, it does neglect a number of higher-order effects that may occasionally be important. For example, the common-emitter forward current gain, is not a constant, as assumed in the Ebers-Moll and Aedcap models. However, a reasonable representation of the beta variation can be obtained by augmenting Aedcap's built-in model with other standard elements.

Other shortcomings of the modeling equations can often be handled in a similar manner. Aedcap's modeling equations do not currently extend to microwave frequencies, but microwave devices can be simulated through suitable manipulations.

Another common problem is getting the series expansions for the solutions to converge. Aedcap minimizes this problem, with the help of the designer. For example, a bistable circuit can be particularly troublesome, since the computer does not know which of the two stable modes represents the desired solution. The designer's knowledge of the circuit he is analyzing should suggest to him that this may occur. He can avoid the problem by biasing the simulated circuit so as to eliminate the superfluous solution.



3. Designing with Aedcap. Differential transistor pair (a) must supply voltage gain of 50 ±10%. After approximating value of ideal current source that provides desired gain, real supply (E_3) and series resistors (R_3) can be substituted, as in (b). Tables are Aedcap circuit descriptions. Once all circuit nodes are numbered, elements are described on a line by listing the higher-potential node first. Transistor terminal nodes must be ordered—collector, base, then emitter. Also, a transistor must be identified as one of Aedcap's built-in models.

The bistable example illustrates a general property of simulation circuits. Practical circuits will always present more possibilities than could be envisioned by any set of program equations. The designer, therefore, must have some idea of what he wants his circuit to do, and how it is likely to perform before he can make intelligent use of a simulation system. He cannot expect the computer to describe all the possibilities inherent in a particular design.

Using Aedcap is easy

A typical design session will illustrate how to work with Aedcap. Figure 3a shows an every-day circuit—a differential transistor pair containing transistors Q_1 and Q_2, resistors R_1 and R_2, voltage sources E_1 and E_2, and ideal current source J_1. The circuit has five nodes, which are numbered. (The ground node is always made 0 by Aedcap convention; otherwise, any node numbering scheme will do.)

The Aedcap description for the differential pair also appears in Fig. 3a. It is a listing, by node connection, of the circuit elements. Only a few simple rules must be followed to describe a circuit. Each line in the table describes an element; the node that lies at the higher potential is listed first. Therefore, supply E_1 has its node connections written as 5 and then 0, since node 5 is at 12 volts and node 0 is ground.

For transistors, the collector node is listed first, followed by the base and emitter nodes, respectively. Transistors, it should be noted, must be separately described as models so that the computer can refer to them when they are used in a circuit. Failure to specify all 18 parameter values of Aedcap's built-in transistor model will cause default values to be used.

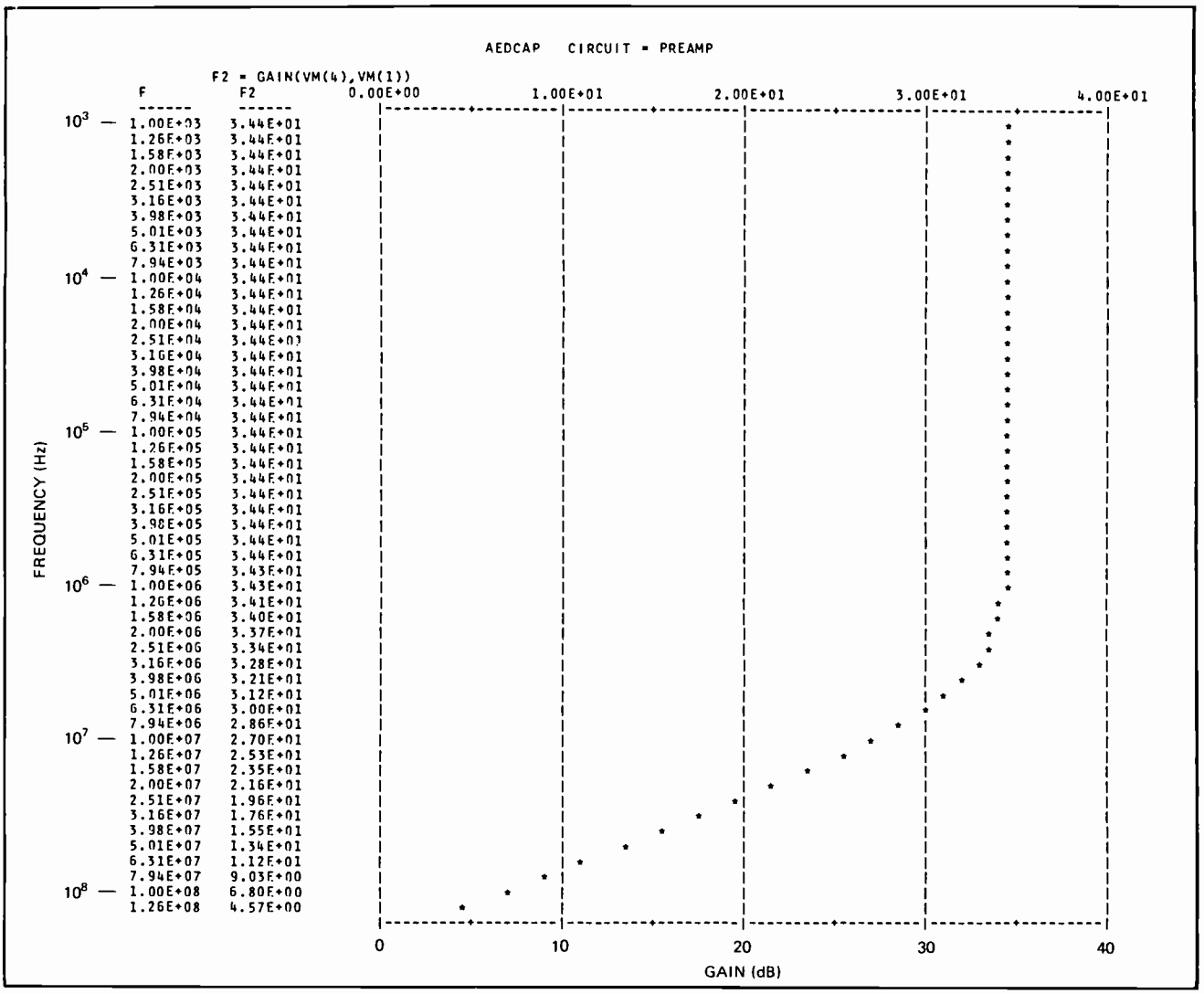
The differential pair of Fig. 3a is to be a preamplifer in a larger circuit configuration. Its load resistance will be 1 kilohm, and a single-ended voltage gain of 50 ±10% is desired. The power supplies are +12 V and −12 V. (The negative supply is to be added later in place of the ideal current source.) Transistor model parameters are known and stored in the Aedcap file.

From circuit design experience, it is known that the gain of this circuit depends on the value of transistor emitter current, I_E. The design procedure, then, consists of establishing an ideal current source (J_1) to determine the correct value of I_E. After this value is found, the ideal current source can be replaced by an emitter resistance and a negative supply.

A computer run

Once the circuit is described, the current for J_1 can be estimated and tested. Since the frequency response of this preamp should be essentially flat, ac voltage gain can be quickly checked by computing the voltages at nodes 2 and 4 for a signal frequency of 1 hertz (for simpler calculations). Knowing the voltage at either node 2 or node 4 would be sufficient, but finding the potential at both nodes will help confirm expected performance.

To test a 2-milliampere value of J_1, the user simply types a request for an ac analysis, specifying the 2-mA



4. Performance check. Computer plot of frequency response for differential pair in Fig. 3b shows that gain is about 35 dB out to 1 MHz.

estimate in place of JVARY in the table of Fig. 3a. At the same time, he requests a printout of the voltages at nodes 2 and 4. The computer will find that both voltages are approximately 7.3 V.

Since the estimate of 2 mA yields a voltage gain of only 7.3, the analysis is repeated for a current source of 10 mA. This gives a satisfactory gain of about 55.3.

Ideal current source J_1 can now be replaced by a real resistor and a real supply. By calling in the Aedcap editor, source J_1 can be removed, and a 1.2-kilohm resistor (R_3) and a -12-V supply (E_3) can be inserted. The practical differential pair is illustrated in Fig. 3b, along with its Aedcap description.

Again, circuit gain is checked by computing the voltages at nodes 2 and 4 for a 1-Hz input. If the gain is not within the desired specification of 50 ±10%, the value of resistor R_3 must be changed. A computer run shows that the gain is within tolerance, indicating that the circuit is essentially designed.

At this point, there are a number of possible analyses that can be performed. For example, the circuit's dc transfer characteristics can be determined by plotting the output voltages at nodes 2 and 4 as functions of dc input E_2. Or the common-mode gain can be computed by first calling in the Aedcap editor to connect Q_1's base to Q_2's base and then looking at the output voltage transfer curve at node 4.

The circuit's pulse transient response can also be checked out by using standard Aedcap pulse functions or any user-desired pulse function. And the sensitivity of the circuit can be tested to see how well the design is likely to fare under production conditions.

Since the circuit's frequency response was initially assumed to be flat, a sensible computation is checking the gain of the differential pair over a broad range of frequencies, taking advantage of Aedcap's ability to do full frequency sweeps. The computer printout of Fig. 4 shows the results of sweeping the circuit from 1 kilohertz to 100 megahertz and obtaining a plot of gain (in decibels) versus frequency. The graph verifies that the frequency response will be essentially flat to 1 MHz.

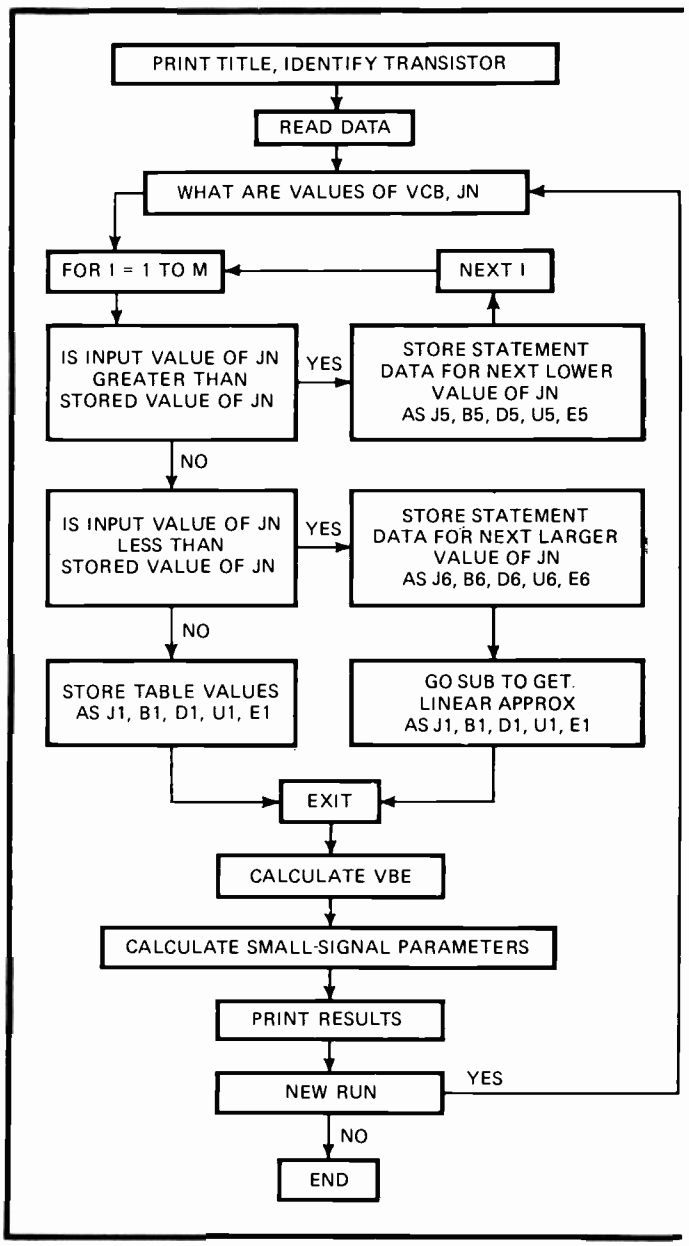
Program availability

Aedcap requires a large in-house computer, or it can be used interactively through the time-sharing facility of National CSS in Stamford, Conn. The computer terminals that the program can now accommodate include the IBM model 2741, Teletype models 33 and 35, and the Tektronix types T4002, T4002A, and T4010 graphic computer terminals. □

Easy-to-use Hypi program makes possible transition from nonlinear to linear transistor model

Acting as an interface between linear and nonlinear analysis programs, a new computer program called Hypi converts parameters of nonlinear charge-control transistor model to those of linear hybrid-pi model

by John R. Greenbaum, *General Electric Co., Syracuse, N.Y.*



☐ Most nonlinear computer programs can analyze circuits only in the time domain, while linear computer programs perform analysis in the frequency domain. However, practically all available transistor performance data is in nonlinear form, making it inappropriate for the linear programs. Consequently, an intermediate program is needed to convert nonlinear transistor models to linear models, so that the linear programs can be used for frequency analysis.

A new short program, which is called Hypi (pronounced high-pie), enables the user to describe his circuit with a nonlinear transistor model, but perform his analysis with a linear computer program, like Cornap (Cornell network analysis program), ECAP (electronic circuit analysis program), ACnet (ac network analysis

1. Hypi computer program. Flowchart outlines how Hypi converts nonlinear charge-control transistor model to linear hybrid-pi transistor model. The user simply supplies data for transistor collector current and base-collector voltage. Previously stored table contains data for charge-control model parameter values. (Linear interpolation is used to bridge table values.) After reading user input data, Hypi solves equations relating charge-control parameters to hybrid-pi parameters. Sample program develops model for type 2N1711 transistor.

```
HYPII*

100 PRINT"PROGRAM TO DERIVE SMALL SIGNAL HYBRID PI FROM LARGE SIGNAL"
110 PRINT "DATA"
120 PRINT "*************************************************************"
130 REM N1=B,N2=BC,N3=BE,A1=A1,A2=A2,I1=IC,I2=IES,I3=ICS
140 REM P1=PHI1,P2=PHI2,T1=THETA R,T2=THETA I,N1=N1,N2=N2
150 REM V1=VCE, V2=VAC, V3=TIBE, J1=JN, J2=JI, J3=JC, J4=JE
160 REM C1=CDE,C2=CDC,C3=CTC-C4=CTE,C5=CE,C6=CC,G1=GME,R4=RBE
170 REM R5=RCC
180 REM C(]=JN, B(I)=BA, D(I)=J1, U(I)=TCN, V(I)=TCI
190 PRINT "MODEL 2N1711"
200 PRINT"............"
210 DATA 23.,.7,.001,27.E-12,21.E-12,1.62E-13,.42E-13
220 READ N1,N2,R5,A1,A2,I2,I3
230 DATA 1.0,.9,39.7,37.8,.45,.37
240 READ P1,P2,T1,T2,N1,N2
250 LET R5=1.E7
260 DIM C(50),B(50),D(50),U(50),V(50)
270 LET M=22
280 PRINT
290 REM DATA TABLE IN MONOTONIC INCREASING CURRENTS
300 DATA .00J5E-3,.2,.56,5.E-10,3.E-6
310 DATA .005E-3,.2,.56,5.E-10,3.E-6
320 DATA .0095E-3,.13,.56,5.E-10,3.E-6
330 DATA .61E-3,.20,.56,5.E-10,3.E-6
340 DATA .82E-3,.25,.56,5E-10,3E-6
350 DATA .83E-3,.28,.58,5E-10,3E-6
360 DATA .95E-3,.32,.65,5.E-10,3.E-6
370 DATA .97E-3,.36,.67,5E-10,3E-6
380 DATA .1E-3,.42,.74,5.E-10,3.E-6
390 DATA .2E-3,.55,.72,5E-10,3E-6
400 DATA .3E-3,.65,.70,5E-10,3E-6
410 DATA .7E-3,.82,.64,5E-10,3E-6
420 DATA .5E-3,.70,.67,5.E-10,3.E-6
430 DATA 1.E-3,.96,.62,5.E-10,3.E-6
440 DATA 2E-3,.105,.57,5E-10,3E-6
450 DATA 3E-3,.117,.53,5E-10,3E-6
460 DATA 5.E-3,.130,.,5,5.E-10,3.E-6
470 DATA 7E-3,.140,.47,5E-10,3E-6
480 DATA 10E-3,.145,.42,5E-10,3E-6
490 DATA 20E-3,.158,.38,5E-10,3E-6
500 DATA 30E-3,.160,.36,5E-10,3E-6
510 DATA 50E-3,.160,.33,5E-10,3E-6
520 FOR I=1 TO M
530 READ C(I),B(I),D(I),U(I),V(I)
540 NEXT I
550 PRINT"YOUR VALUES FOR VCB,JN ARE";
560 REM VCB=V2 IN VOLTS   JN=J1 IN AMPS
570 INPUT V2,J1
580 PRINT
590FOR I=1 TO M
600 IF J1<C(I) THEN 670
610 IF J1<C(I) THEN 730
620 LET B1=B(I)
630 LET D1=D(I)
640 LET U1=U(I)
650 LET E1=V(I)
660 GO TO 1000
670 LET J5=C(I)
680 LET B5=B(I)
690 LET D5=D(I)
700 LET U5=U(I)
710 LET E5=V(I)
720 GO TO 960
730 LET J6=C(I)
740 LET B6=B(I)
750 LET D6=D(I)
760 LET U6=U(I)
770 LET E6=V(I)
780 LET Y1=B5
790 LET Y2=B6

HYPII* CONTINUED

800 GO SUB 1270
810 LET B1=Y3
820 LET Y1=D5
830 LET Y2=D6
840 GO SUB 1270
850 LET D1=Y3
860 LET Y1=U5
870 LET Y2=U6
880 GO SUB 1270
900 LET U1=Y3
910 LET X1=E5
922 LET Y2=E6
930 GO SUB 1270
940 LET E1=Y3
950 GO TO 1000
960 NEXT I
1000 LET V3=LOG(J1/I2)/T1
1010 LET J2=I3*(EXP(T2*V2)-1.)
1020 LET J3=J2/B1-J1
1030 LET J4=J1/B1-J2
1040 LET C1=T1*U1*(J1+I2)
1050 LET C2=T2*E1*(J2+I3)
1060 LET C3=A2/(P2-V2)^N2
1070 LET C4=A1/(P1-V3)^N1
1080 LET C5=C1+C4
1090 LET C6=C2+C3
1100 LET G1=T1*J1
1110 LET R4=B1/G1
1120 PRINT
1130 PRINT
1140 PRINT"FOR VCB=";V2;",JN=";J1
1150 PRINT"-------------------------------------------------------"
1160 PRINT"RB=";R1,"RC=";R2,"RE=";R3,"RBE=";R4
1170 PRINT "RCC=";R5,"CC=";C6,"CE=";C5,"GME=";G1
1180 PRINT"VBE=";V3
1190 PRINT
1200 PRINT" IF YOU WANT A NEW RUN TYPE 1, FOR NO NEW RUN TYPE 0"
1230 LET X=2
1240 INPUT X
1250 IF X=1 THEN550
1255 STOP
1260 REM SUROUTINE FOR LINEAR APPROXIMATION
1270 LET A = (Y2-Y1)/(J6-J5)
1280 LET B=Y1-A*J5
1290 LET Y3 =A*J1+B
1300 RETURN
1310 END
```

program), or any one of several other programs.

Developed at General Electric, Hypi can be run on a time-shared basis and is written in Basic language. It converts the parameters of the nonlinear large-signal Beaufoy-Sparkes charge-control transistor model to the parameters of the familiar linear small-signal hybrid-pi transistor model. The panel, "From charge-control to hybrid-pi," shows the two models and the conversion equations.

There are several ways to solve these equations. For instance, they can be solved directly, if not very conveniently, with the nonlinear program, Sceptre (system for circuit evaluation and prediction of transient radiation effects) [*Electronics*, Aug. 16, 1971, p. 72]. Alternatively, Hypi can be used alone, after the values for two of the parameters for the charge-control model, current density J_N and base-collector voltage V_{BC}, have been computed manually. Or, again, the nonlinear program, Circus (circuit simulator), can be used to find the J_N and V_{BC} values, and then Hypi used to finish the conversion.

Examining Hypi

Hypi's flowchart (Fig. 1) is a generalized description of how the hybrid-pi model data is obtained. The program identifies the transistor type being examined, reads the data describing the charge-control transistor characteristics, and then asks the user for the operating conditions specific to his circuit's performance.

Hypi represents the charge-control model parameters of forward gain β_N, inverse gain β_I, normal time con-

stant τ_N, and inverse time constant τ_I, as points on the curves normally used to describe these functions. (This data can be obtained from published transistor literature.) The Hypi program automatically provides linear interpolation between adjacent parameter values when necessary. Therefore, a proper result is obtained when an evaluation is requested for a value of current density J_N that does not exactly correspond with one of the listed entries.

User input data is examined to determine whether it agrees with the charge-control model data previously stored or whether an interpolation is required. The charge-control model equations are then solved, and the results inserted in the conversion equations for the hybrid-pi model. The outcomes of these computations are labelled with the hybrid-pi parameter descriptions.

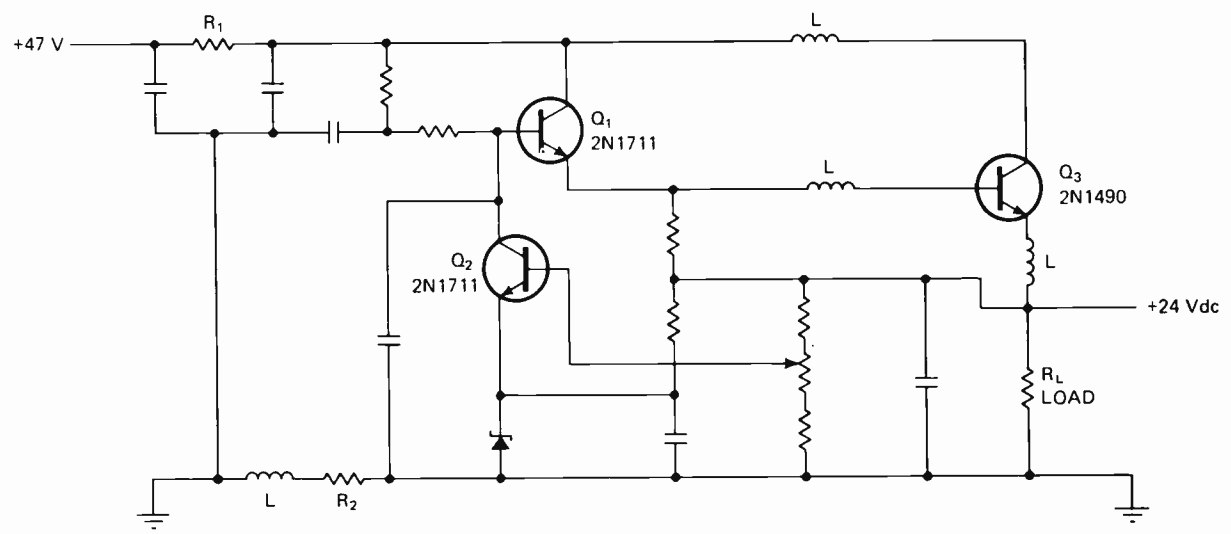
A sample Hypi program is also included in Fig. 1. Statements 100 through 200 identify the program, the transistor that is being evaluated (in this case, type 2N1711), and the variables in the program. Statements 210 through 540 cause the data describing the transistor to be read into the program. By changing this data, different transistors can be modeled.

The charge-control model parameters are called out in statements 210 and 230. Statement 210 provides data for base bulk resistance R_{BB}, collector bulk resistance R_{CC}, emitter bulk resistance R_{EE}, base-emitter capacitance A_1, base-collector capacitance A_2, saturation emitter current I_{ES}, and saturation collector current I_{CS}. Statement 230 enters data for intrinsic base-emitter potential ϕ_1, intrinsic base-collector potential ϕ_2, and constants θ_1, θ_2, N1, and N2.

Statement 270 indicates the number (m) of different collector current values to be stored in the program. Statements 300 through 510 list these various values of current J_{Nm}, in addition to the values for forward gain β_{Nm}, inverse gain β_{Im}, normal time constant τ_{Nm}, and inverse time constant τ_{Im}. This creates a data table, with the current values given in increasing order.

User input data for current J_N and voltage V_{CB} is requested by program statements 550, 560, and 570. With this input information, Hypi searches its data table to determine if the input current value agrees with a stored current value. If no agreement is found, a linear interpolation is performed between the two stored current values between which the input current value falls.

This procedure is described in statements 590 through 960. The lower data point values for β_N, β_I, τ_N,



ALL INDUCTORS (L) AND RESISTORS R_1 AND R_2 ARE DUE TO LEAD LENGTHS

NONLINEAR TRANSISTOR OPERATING CONDITIONS

R_L (Ω)	Q_1		Q_2		Q_3	
	V_{BC} (V)	J_N (A)	V_{BC} (V)	J_N (A)	V_{BC} (V)	J_N (A)
25	−5.54	0.0132	−13.90	0.0027	−6.16	0.996
50	−12.40	0.00536	−14.00	0.00626	−13.00	0.519
125	−16.70	0.00228	−14.10	0.00848	−17.30	0.220
250	−18.20	0.00151	−14.10	0.00924	−18.80	0.119

2. Sample analysis. Voltage regulator can be examined for potential instabilities. Nonlinear Circus program is used first to determine collector currents and base-collector voltages of all three transistors for four different load conditions. Table shows results of Circus analysis of the transistors for load resistances of 25 to 250 ohms, which cause load current for the 24-volt regulator to vary from 1 to 10 amperes.

From charge-control to hybrid-pi

When a transistor operates under varying conditions, a nonlinear model is needed to describe device behavior properly. One such model, a simplified version of the Beaufoy-Sparkes charge-control transistor model, is shown along with a tabulation of its parameters and some typical values.

The equations to determine the current generators for the model are:

$$I_1 = (1/\beta_N + 1)J_N - J_I$$
$$I_2 = -J_N + (1/\beta_I + 1)J_I$$

where:

$$J_N = I_{ES}[\exp(\theta_N V_{BE}) - 1]$$
$$J_I = I_{CS}[\exp(\theta_I V_{BC}) - 1]$$

The depletion and diffusion capacitances for the model can be expressed as:

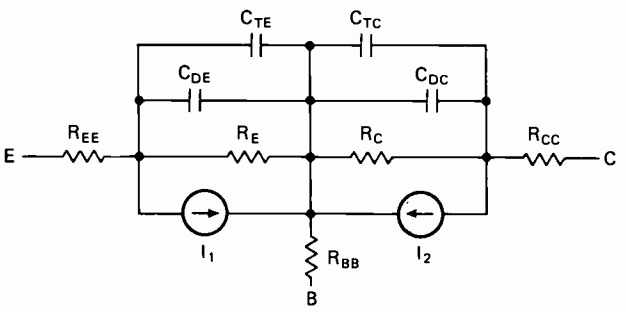
$$C_{TE} = A_1/(\phi_1 - V_{BE})^{N1}$$
$$C_{TC} = A_2/(\phi_2 - V_{BC})^{N2}$$
$$C_{DE} = \theta_N \tau_N(J_N + I_{ES})$$
$$C_{DC} = \theta_I \tau_I(J_I + I_{CS})$$

The accuracy of nonlinear transistor modeling and the convenience of linear problem-solving can be combined by converting the nonlinear charge-control model parameters to the parameters of the linear hybrid-pi model shown. Four equations must be solved:

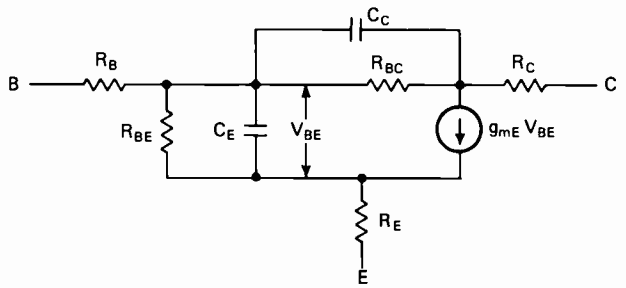
$$g_{mE} = \theta_N J_N$$
$$R_{BE} = \beta_N/\theta_N J_N = \beta_N/g_{mE}$$
$$C_C = A_2/(\phi_2 - V_{CC})^{N2} + \theta_I \tau_I(J_I + I_{CS})$$
$$C_E = A_1/(\phi_1 - V_{CE})^{N1} + \theta_N \tau_N(J_N + I_{ES})$$

Generally, base-collector resistance R_{BC} is assumed to be so large that it can be neglected.

NONLINEAR CHARGE-CONTROL MODEL



LINEAR HYBRID-PI MODEL



CHARGE-CONTROL TRANSISTOR PARAMETERS

Parameter	Definition	Sample value
R_{BB}	Base bulk resistance	55 Ω
R_{CC}	Collector bulk resistance	5 Ω
R_{EE}	Emitter bulk resistance	1 mΩ
R_C	Collector reverse-bias leakage resistance	10 MΩ
R_E	Emitter reverse-bias leakage resistance	30 MΩ
C_{TC}	Collector depletion capacitance	–
C_{TE}	Emitter depletion capacitance	–
C_{DC}	Collector diffusion capacitance	–
C_{DE}	Emitter diffusion capacitance	–
I_{CS}	Saturation collector current when $V_{BE} = 0$	0.485 pA
I_{ES}	Saturation emitter current when $V_{BC} = 0$	3.5 fA
J_N	Forward current generator	–
J_I	Inverted current generator	–
β_N	Normal beta with $V_{BC} = 0$, $V_{BE} = 0$	72
β_I	Inverse beta	0.62
A_1	Base-emitter capacitance	3.7 pF
A_2	Base-collector capacitance	3.3 pF
ϕ_1	Intrinsic base-emitter junction potential	1.1 V
ϕ_2	Intrinsic base-collector junction potential	1.1 V
θ_N	q/mkT, 1 < m < 2, T = 25°C	40.1 V^{-1}
θ_I	q/mkT, 1 < m < 2, T = 25°C	29.4 V^{-1}
N1	Constant, 0.33 (graded junction) to 0.5 (step junction)	0.34
N2	Same as N1, usually N2 ≤ N1	0.10
τ_N	Normal storage time constant	120 ps
τ_I	Inverted storage time constant	35 ns

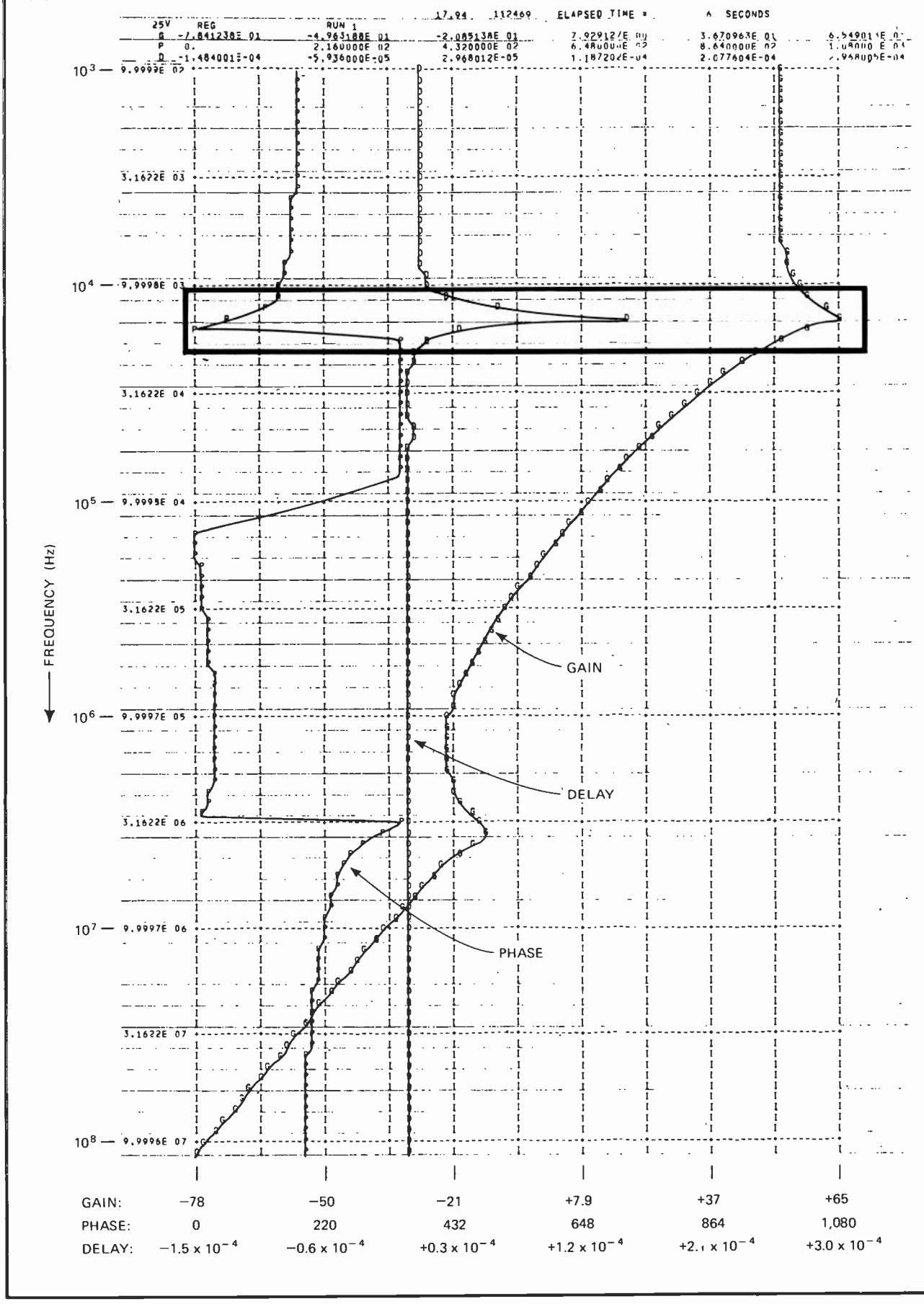
and τ_I are stored as J5, B5, D5, U5, and E5, respectively. Upper data point values for these same parameters are stored respectively as J6, B6, D6, U6, and E6.

The values for the hybrid-pi model parameters are calculated with the equations listed in statements 1000 through 1100. Printout instructions for these computed values are given in statements 1140 through 1180. Statements 1220 through 1250 allow additional circuit operating conditions to be examined and, therefore, other parameter values to be generated at the user's option. If no further modeling is required, the program stops.

Using Hypi

A design example will illustrate how the Hypi program can simplify circuit analysis. The voltage regulator of Fig. 2 is to be examined to identify any potential cir-

(a)


FREQUENCY (Hz)
10^3
10^4
10^5
10^6
10^7
10^8
GAIN
DELAY
PHASE
GAIN: −78 −50 −21 +7.9 +37 +65
PHASE: 0 220 432 648 864 1,080
DELAY: -1.5×10^{-4} -0.6×10^{-4} $+0.3 \times 10^{-4}$ $+1.2 \times 10^{-4}$ $+2.1 \times 10^{-4}$ $+3.0 \times 10^{-4}$

(b)

17.94 112469 ELAPSED TIME = 4 SECONDS

25V REG RUN 1

TRANSFER FUNCTION CRITICAL FREQUENCIES - HZ

OUTPUT VARIABLE - I RL1
SOURCE VARIABLE - I4

GAIN CONSTANT IS 5.9664833D-03

POLE POSITIONS			ZERO POSITIONS		
REAL PART	IMAGINARY PART	ORDER	REAL PART	IMAGINARY PART	ORDER
-2.7480649D 08	0.	1	-2.7480622D 08	0.	1
-5.3880355D 06	0.	1	1.3145697D 06	0.	1
-5.6950299D 06	-2.3229797D 07	1	-5.6977901D 06	-2.3199971D 07	1
-7.4132548D 05	4.0710722D 06	1	-6.6625225D 05	-4.2086433D 06	1
-7.0530964D 05	3.5812489D 06	1	-1.8070639D 06	4.5857293D 05	1
-2.2069888D 06	0.	1	-6.0152818D 05	0.	1
-1.2590207D 04	0.	1	-3.5091589D 04	0.	1
-1.0208272D 03	1.3869207D 04	1			

TRANSFER FUNCTION POLYNOMIALS - RADIANS
SCALED BY 1.000D 08 IN FREQUENCY AND 1.000D 03 IN IMPEDANCE

DENOMINATOR COEFFECIENTS	DEGREE IN S	NUMERATOR COEFFECIENTS	DEGREE IN S
1.0000000000000D 00	12	1.0000000000000D 00	10
1.864217802923 70D 01	11	1.825079863676 18D 01	9
2.674495982819 17D 01	10	1.952706452240 86D 01	8
5.344559084114 75D 01	9	4.441617336461 98D 01	7
3.104441593153 80D 01	8	1.193467832064 69D 01	6
1.169884435379 86D 01	7	3.594712320496 98D 00	5
3.414506494686 25D 00	6	4.624796708579 83D-01	4
6.148752089695 85D-01	5	-5.280801379067 99D-03	3
8.910538394723 56D-02	4	-3.889261945336 46D-03	2
6.590655930135 16D-03	3	-1.279931354482 66D-04	1
6.060732181377 69D-06	2	-2.633680676423 26D-07	0
5.683390326587 98D-09	1		
3.931137143311 77D-12	0		

3. Frequency response. Nonlinear transistor model data computed by Circus is entered into Hypi so that hybrid-pi model and, therefore, linear program can be used to analyze regulator. Subsequent frequency analysis by linear Cornap program provides plot (a) of regulator characteristics for 1-ampere load, as well as tabulation (b) of pole-zero locations. Potential instability is outlined in color.

cuit instabilities that could cause unwanted oscillation.

First, the collector currents and base-collector voltage drops of all the transistors are found with the nonlinear Circus program for four different load conditions. In this case, load current ranges from approximately 1 ampere to 10 milliamperes, as load resistance is varied from 25 to 250 ohms. The table in Fig. 2 gives the results of this analysis.

The current and voltage values are then entered into the Hypi program; a separate run is needed for each transistor. The hybrid-pi model data supplied by Hypi can then be entered into any one of several linear analysis programs. For this example, the widely used linear program, Cornap, is chosen for convenience. With a command of only a single instruction, Cornap can provide transfer functions, pole-zero locations, and plots.

Figure 3a is a Cornap frequency-domain plot of the regulator's gain, phase and delay characteristics when load current is about 1 A. Amplitude values and peak amplitude locations vary with transistor collector current. The peak (outlined in color) in the vicinity of 14 kilohertz for all characteristics indicates the presence of a potentially critical pole.

Cornap's tabulated output format (Fig. 3b) for the regulator's frequency-domain transfer function and pole-zero locations lists the potentially troublesome pole (outlined in color) as having its real part located at 1,021 hertz and its imaginary part at 13,869 Hz. An analysis of this pole location reveals that the pole's phase angle is approximately 86°, which implies extreme sensitivity to ringing and probable oscillation if parameter values change even slightly. □

The author wishes to acknowledge J.E. Hooper's help in developing the Hypi program.

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