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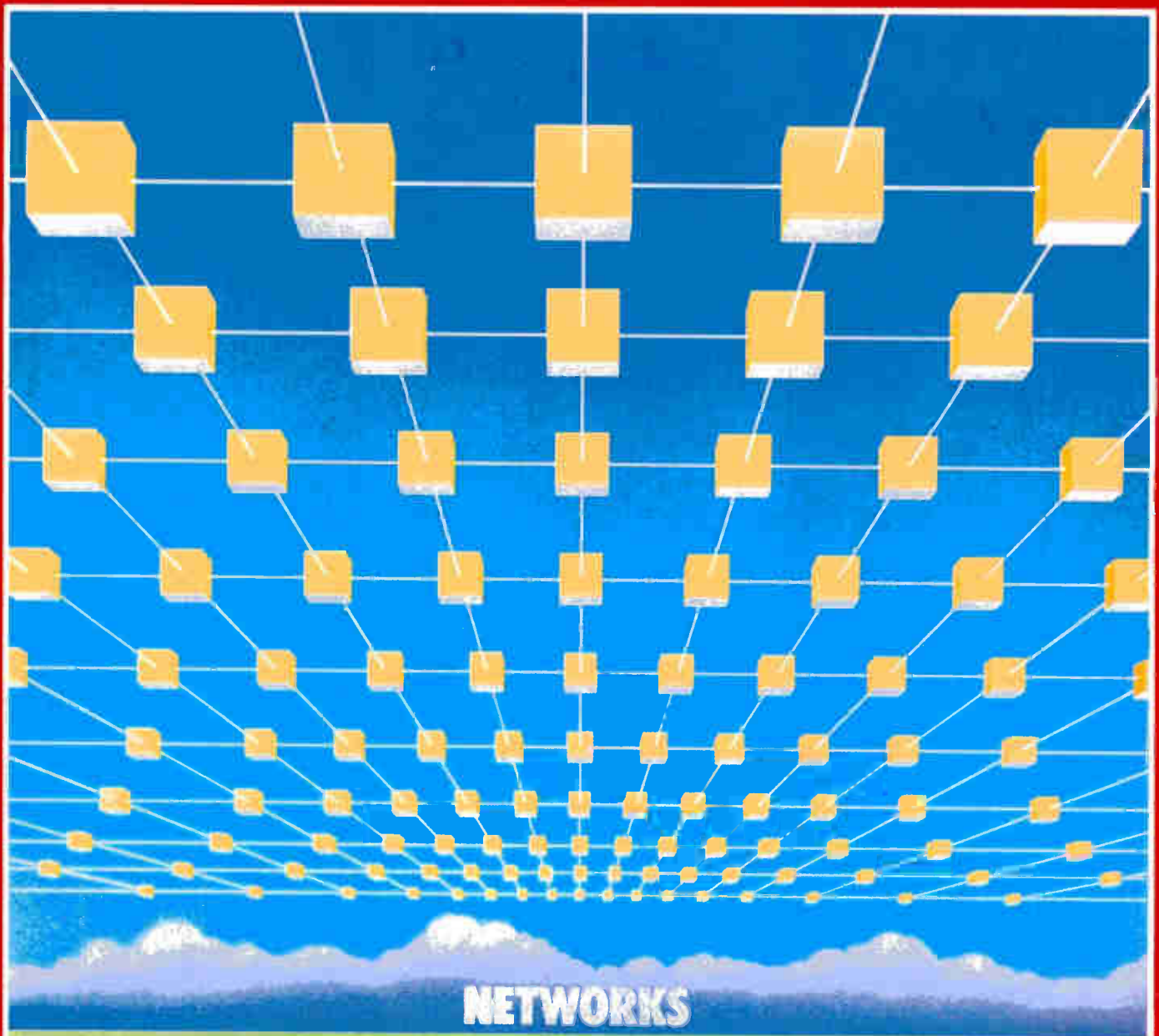
A VNU PUBLICATION

# Electronics

APRIL 14, 1988




## FROM SYSTEMS TO STANDARDS, THE PACE QUICKENS

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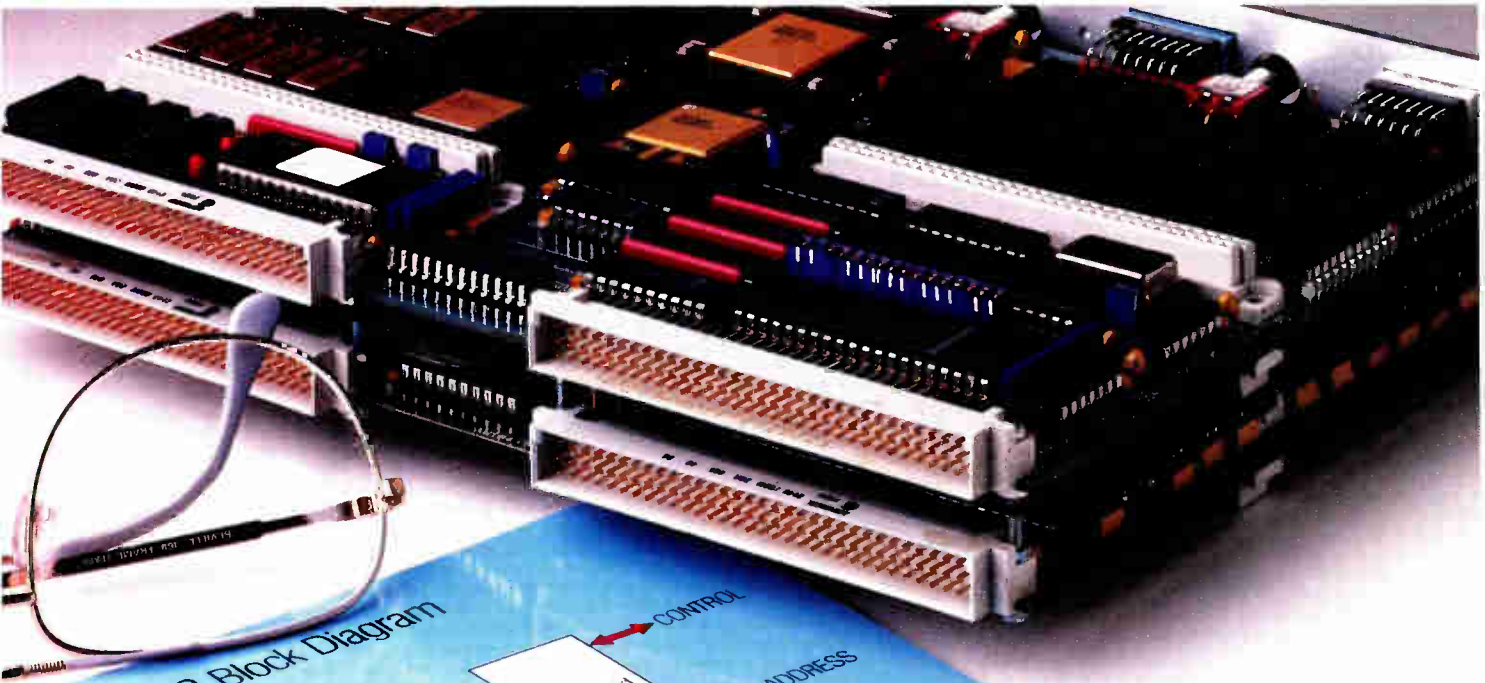
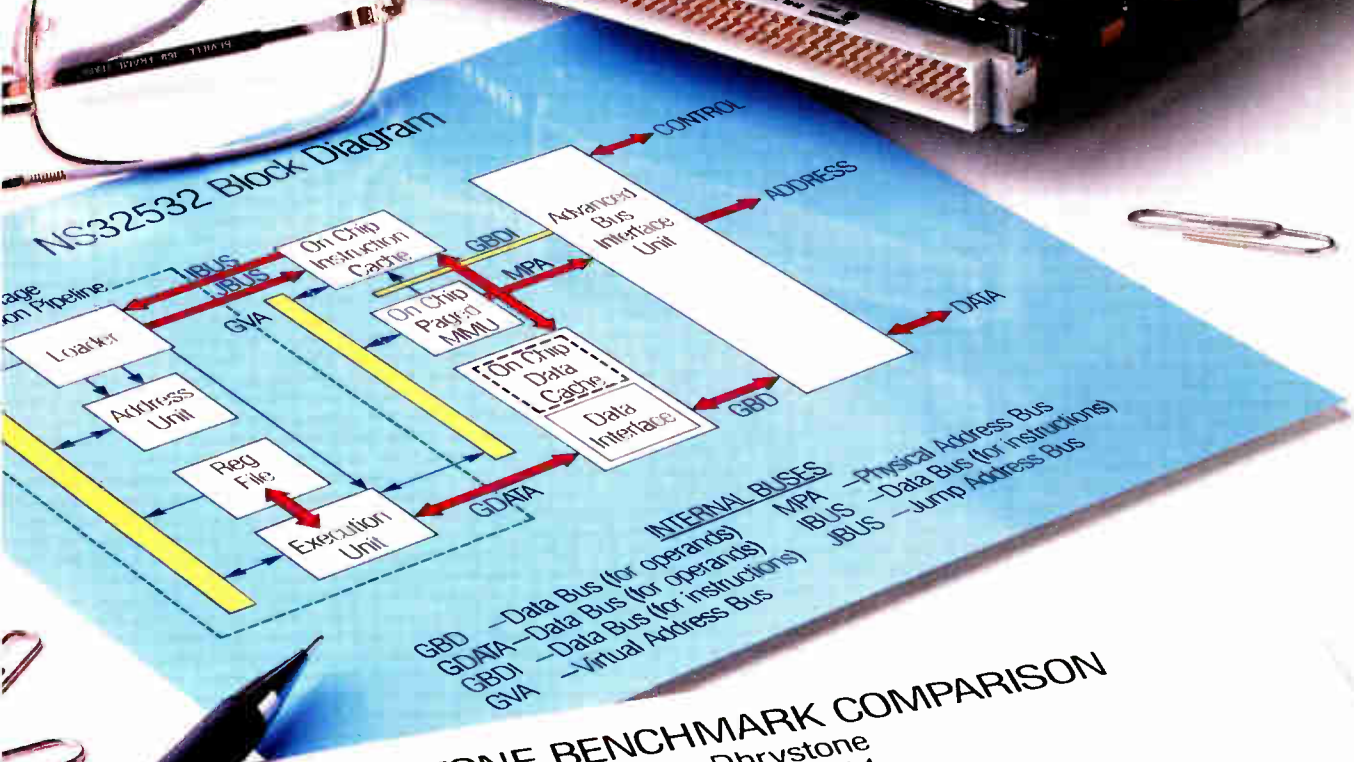
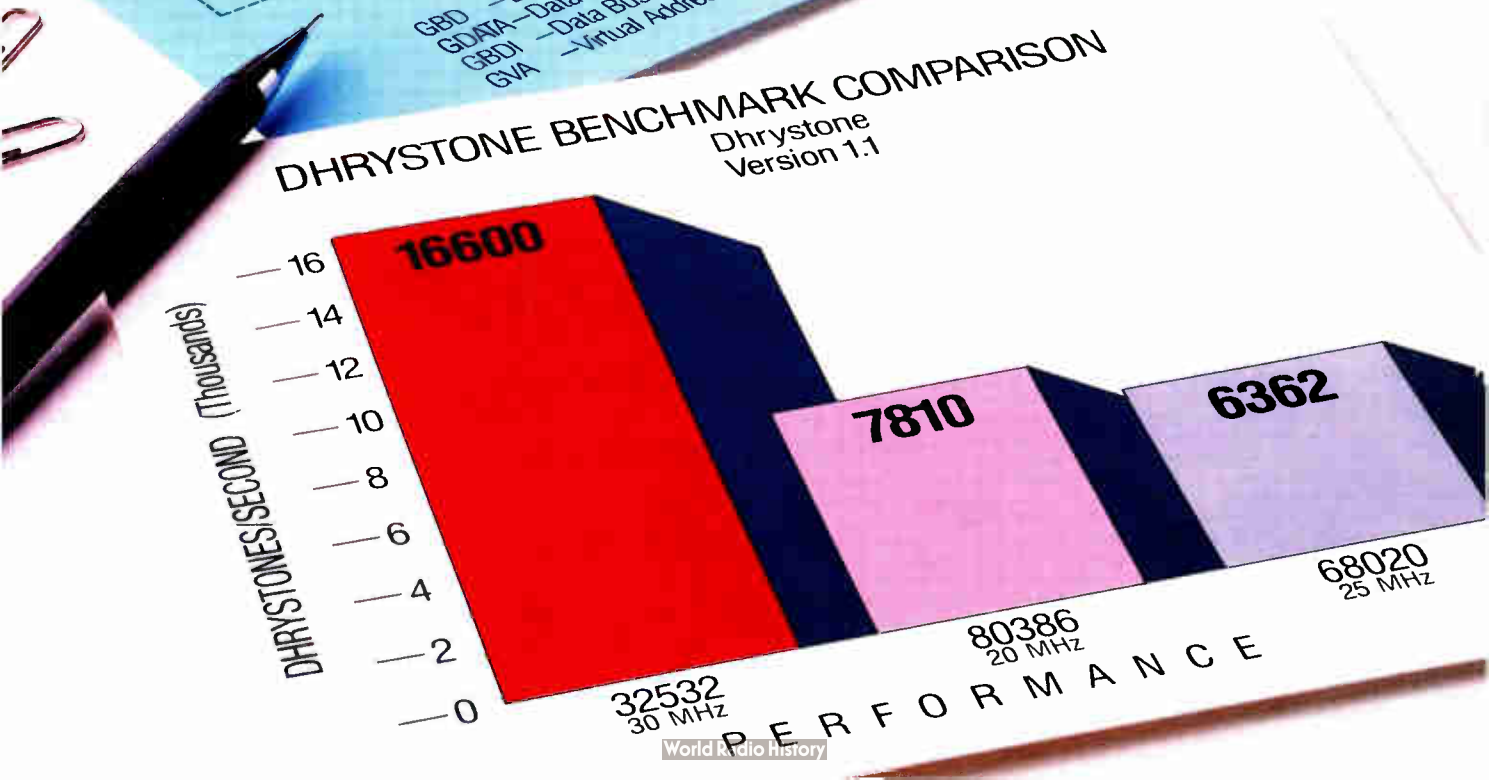
National Semiconductor





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# The NS32532: Real-world performance for real-world applications.

At National, we believe that a high-performance 32-bit microprocessor should be worked with, not around.

That's why the NS32532 offers you some of the highest performance specs in the industry.

Yet it's performance you can *use*. Because the NS32532 was created for real-world designers working on real-world systems to meet real-world needs.

## PERFORMANCE YOU CAN COUNT ON

The NS32532 is capable of delivering 15 MIPS peak performance, 8-10 MIPS sustained, at 30 MHz.

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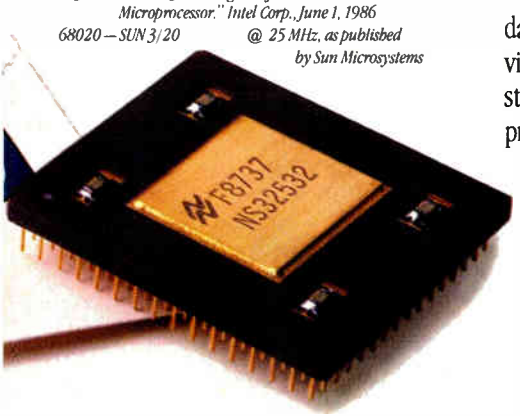
Not to mention high integer performance *and* high floating-point performance. With a range of FPU solutions that deliver up to 8 million double-precision Whetstones per second.

*Below: NS32532 chip*
*Left: VME532 evaluation board; NS32532 block diagram; competitive performance comparison**

* *Sources:*
*NS32532 — August 1987 Performance Evaluation Tests*
*80386 — "The 80386: A High-Performance Workstation Microprocessor." Intel Corp., June 1, 1986*
*68020 — SUN 3/20 @ 25 MHz, as published by Sun Microsystems*




### The NS32532

- 8-10 MIPS sustained, 15 MIPS peak
- 20-, 25-, and 30-MHz devices
- On-chip 1,024-byte 2-way set associative physical data cache
- On-chip 512-byte direct mapped physical instruction cache
- Hardware cache invalidate for high-performance cache coherency
- On-chip demand-paged memory management including 64-entry fully associative Translation Lookaside Buffer
- 4-stage instruction pipeline including instruction prefetch and branch prediction
- 2-clock basic READ/WRITE cycle
- 1-clock burst-mode transfers
- Unique bit-manipulation and string-handling instructions
- Highly symmetrical and orthogonal instruction set producing compact code
- Extremely fast context switch (3.6 $\mu$s) and interrupt service (1.3 $\mu$s)
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- 370,000 transistor sites
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## SUPER-MINI PERFORMANCE ON A CHIP

The NS32532 achieves its superior performance because it integrates key systems functions on a single piece of silicon.

Only the NS32532 incorporates on-chip data and instruction caches, demand-paged virtual memory management, and a 4-stage instruction pipeline. With instruction prefetches and branch prediction. Plus a hardware cache invalidate mechanism that ensures cache coherency.

## SCALABLE PERFORMANCE

The NS32532 is one of seven CPUs based on the same 32-bit architecture. With the same orthogonal, highly symmetrical instruction set.

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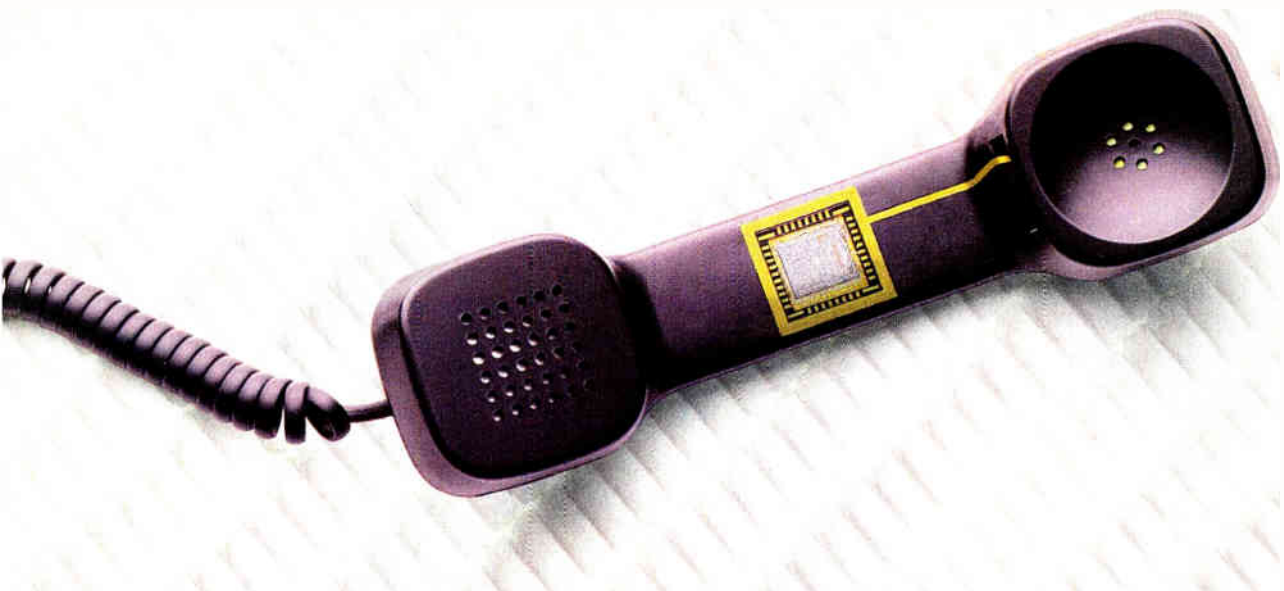
National Semiconductor



Circle 1 on reader service card

# THE $17* DIGITAL TELEPHONE



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# IT TAKES TIME, BUT JUSTICE DOES TRIUMPH

## Belatedly, a key man behind the microprocessor is getting the attention he deserves: this month, Federico Faggin receives a Marconi Fellowship

It often takes a heckuva long time, but justice usually triumphs. Latest example is my friend Federico Faggin. Several companies and people in recent years have been quick to grab credit for developing the microprocessor. And usually Federico's name doesn't come up. But in Rome on April 28, he will be awarded the prestigious Marconi International Fellowship for—you guessed it—"his contributions to the implementation of the microprocessor." The fellowship singles out individuals who have made highly original contributions to communications technology. Some observers have felt that Federico's role in moving the microprocessor to market has been ignored and his technical contributions played down. No more.

Federico notes that pioneering work had already been done at Fairchild and Rockwell when Intel's Ted Hoff, aided by Stan Mazor, proposed an architecture and an instruction set for a group of standard components that could be programmed to handle the calculator needs of Japan's Busicom. Federico was hired in April 1970 to design this chip set and was told the architecture and logic design had already been done, that only some circuit design and chip layout work remained. "But that is not what I found," recalls Federico.

He resolved the remaining architectural issues and did the logic and circuit design and layout. One of those chips was a 4-bit CPU, the 4004. "I felt that something very important had happened, but that perception was not shared by Intel management, who thought it was good only for calculators." In November 1971, thanks to Federico's prodding, Intel announced the 4004. More processors rolled out, including the 8080, which really got the microprocessor ball rolling. But Federico had grown restless, so he decided to start a company that would be dedicated to the MPU market. Zilog was founded, and soon Federico had designed another winner, the Z80.

And he's still at it. He believes that semiconductor technology is about to bear another child: building structures using the same principles of information processing as the animal nervous system. The best way to go about this is to build massively parallel structures of analog computation elements, he says. Within 5 to 10 years, he predicts, "we will be able to build a neural system chip the size of a whole wafer and containing over 1 billion components. It is at once a marvelous and disquieting possibility." **ROBERT W. HENKEL**

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APRIL 14, 1988

# Electronics

## NEWS

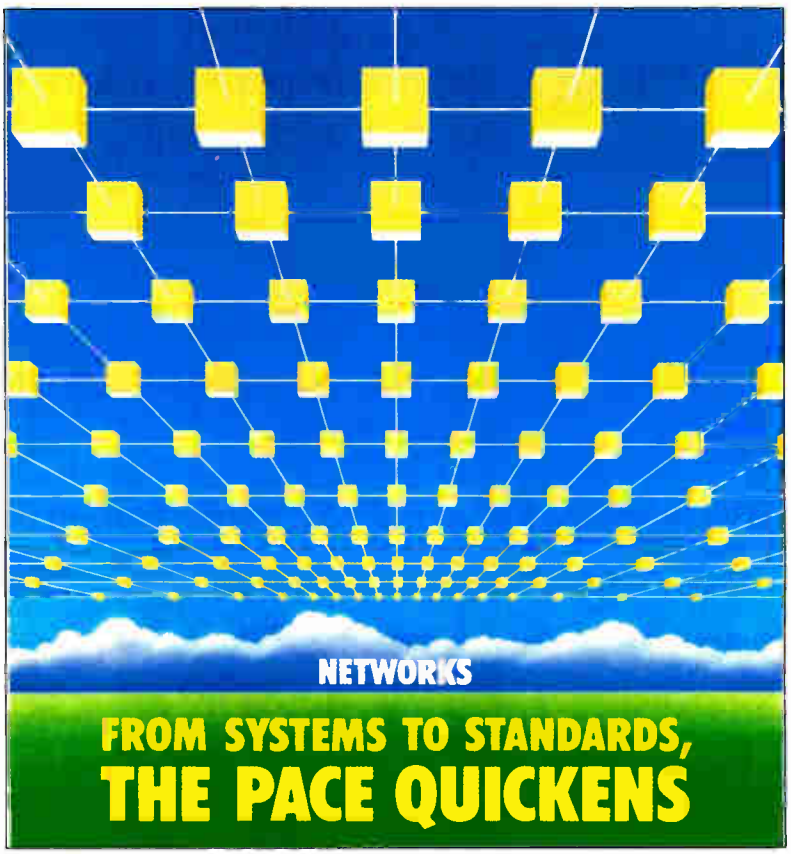


## INSIDE TECHNOLOGY



## PROBING THE NEWS

COVER: DAVID MYERS

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## NEW PRODUCTS

**Newsletter, 25**
- NEC delivers a 500-fold speed boost in a graphics IC . . .
- . . .And its 16-bit V33 is four times faster than its predecessor
- Microchip links three tool suites to cut weeks off DSP design
- Crystal Semiconductor goes for two new markets with 16-bit analog-to-digital chips

**Semiconductors, 103**
- Intel makes reprogramming its 64- and 256-Kbit flash EEPROMs easy and endows the chips with access times as fast as 150 ns
- A disk-controller chip from Cirrus Logic doubles system performance for high-end IBM Corp. PC ATs and compatibles
- Teledyne Philbrick's trio of power hybrids saves $70,000 to $90,000 in engineering and design costs for customized power supplies
- A cache controller from Austek Microsystems runs at a 25% faster clock speed than its predecessor chip

**Military/Aerospace Newsletter, 101**
- Should the U. S. limit foreign ownership of defense contractors?
- Plessey gets a big incentive to save money
- Magnetek's ship-board power system won't quit when it overloads
- The Pentagon sets up the Defense Manufacturing Board in order to sharpen U. S. competitiveness
- Now there's a fast way to produce inexpensive cockpit prototypes

## DEPARTMENTS

# M68000 Family

## Growing to meet your changing needs.

Your high-performance systems require a wide range of microprocessor and peripheral support. The versatile M68000 Family serves those needs with product that's well documented, easy to use, cost effective, easy to get and as varied as your applications.


## Versatile solutions for your data *communication* needs.

Motorola has developed a family of high-performance communications controllers called Serial Processing Units (SPUs) based on a modular design concept.

The MC68605 X.25 Protocol Controller (XPC) independently generates link-level commands for X.25 and X.75 networks. It expertly terminates the Link Access Procedure Balanced (LAPB) at the full 1.544 or 2.048 data rates provided by T1 facilities. It has passed rigorous Defense Data Network certification tests, and its global acceptance is suggested by use on packet networks all over Europe.

The MC68824 Token Bus Controller (TBC) is the only single-chip VLSI implementation of the IEEE 802.4 Media Access Control (MAC) sublayer defined in the Manufacturing Auto-

mation Protocol (MAP) specification.

This high-performance microcoded communications engine also supports the real-time extensions required in MAP version 3.0, on-chip diagnostics, MAC-level bridging, and implements the recommended standard MAC-to-physical serial interface.

The MC68184 Broadband Interface Controller is, with RF circuitry, the broadband modem required for each node of a broadband MAP network.

In addition to the SPUs, M68000 communications peripherals include the MC68661 Universal Synchronous Communications Controller, the MC68652 Multi-Protocol Communications Controller, several DMA circuits and a variety of miscellaneous single- and multifunction devices.

## The highest-performance 8/16/32-bit *MPUs* smooth the migration path for your products.

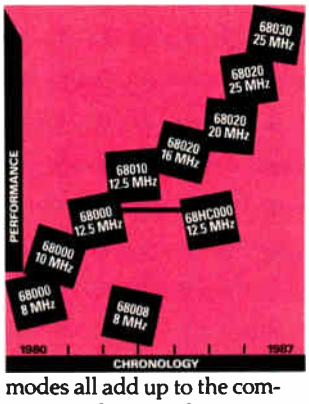
Common internal 32-bit architecture. Object-code software compatibility. Just two of the reasons M68000 Family microprocessors from the 8-bit MC68008 to the latest 32-bit entry, the MC68030, give your products both the highest performance and the smoothest migration path.

Operating speeds range from 8 MHz for low-cost applications to the industry's fastest general purpose MPUs at 25 MHz.

And, products based on M68000 Family MPUs are the standard for UNIX® operating systems, CAD/CAM workstations, next-generation office automation, multi-user/multitasking departmental computers, color graphics as well as for real-time factory automation.

M68000 MPUs are also preferred engines for high-performance artificial intelligence with large linear addressing requirements.

Large, flexible 32-bit register set, large linear address space, powerful yet simple instruction set and flexible addressing




modes all add up to the competitive advantage for your M68000 MPU-based product.

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## Emulate in real time, debug in record time, with M68000 Family *development system.*

Motorola's HDS-300™ hardware/software development station can give you an important edge in slashing development time and moving your product to market when you design in one of the industry's leading M68000 family MPUs.

It simplifies and speeds up debugging and testing of your MPU hardware and software, and in the appropriate configuration can also provide source-level debug for even greater development-time reduction.

Labor-saving features include real-time no wait-state emulation to 25 MHz, system performance analysis and "C" language source-level debugging. Cost efficiency is achieved with a modular approach that permits operation with any of the available emulator modules, including MC68030, MC68020, MC68010, MC68000 and MC68008.

There are so many more reasons why the HDS-300 development station is the ultimate emulation and analysis tool for systems based on M68000 Family processors. Discover them.

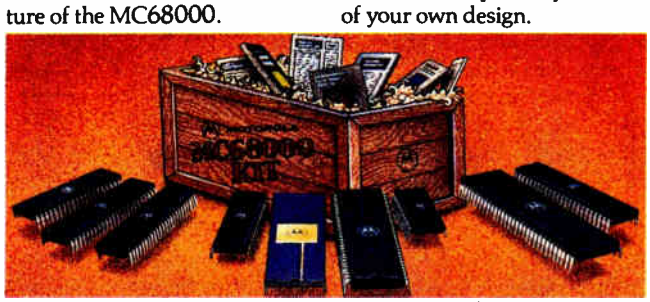
HDS-300 is a trademark of Motorola Inc.

## Create three different high-performance systems with our *$98 design kit.*

It's worth a lot more, of course, but we put the irresistibly low $98 price on our MC68000KIT so you'll never forgive yourself if you don't experience the flexibility, versatility and performance of the M68000 Family.

The design kit has just what you need to create three M68000-based systems.

Three MPUs include the MC68000 16-bit general-purpose standard, the high-performance 16-bit virtual memory MC68010 and the cost-effective 8-bit MC68008 with the 32-bit internal architecture of the MC68000.



Six flexible family peripherals are included so you can design for your specific applications.

The MC68440 with dual independent DMA channels provides DMA control. System timing and parallel I/O requirements are handled by the MC68230. The MC68901 is a multifunction circuit with a single-channel UART for data communications, in addition to an 8-source interrupt controller, four 8-bit timers and eight parallel I/O lines.

Three different serial communications devices, MC68681, MC68661 and MC68652, complete the parts complement, and the kit also contains the documentation you'll want for converting these high-performance M68000 Family devices into superior systems of your own design.

The MC68000KIT is available only through authorized Motorola distributors. Contact your Motorola distributor to take advantage of this great $98 value.

## M68000 Family now offers *surface-mount* packaging.

As customers develop the ability to utilize surface-mount packages, Motorola is putting the M68000 Family in "J" leaded, Plastic Leaded Chip Carriers. Several MPUs and over a half-dozen varied peripherals are already available now or later this year. The MC68000, MC68HC000 (HCMOS) and MC68010 are available now in the 68-lead package. The MC68008 is available now in the 52-lead version.

PLCC-packaged family peripherals include the MC68824 and MC68605 SPUs (84-lead), MC68440 and MC68442 DMA devices (68-lead), MC68681/2681 DUART (44-lead), MC68230 Programmable Interface/Timer (52-lead) and the MC68901 Multifunction circuit (52-lead). And this is only the beginning.

## Heralded Motorola M68000 Family *training courses* now available on audio cassettes.

Three Motorola-developed training courses for the MC68000, MC68020 and MC68030 are now available on audio cassettes. Both of these low-cost courses include course notes and appropriate technical literature as well as the tapes.

Course MTTA1 is an overview of the MC68000 microprocessor, teaching the MPU itself: pins and bus operation, addressing modes, instruction set and exception processing including interrupts. Successful course completion brings you to basic familiarity with the MC68000.

Course MTTA2 is an introduction to the MC68020, exploring the internal architecture, programming model, pins and bus operation, addressing modes, instruction set and exception processing. The student should have completed Course MTTA1 or have equivalent knowledge of the MC68000 for best results.

MTTA1 is $60, MTTA2 is $95, and the special price for both courses together is $140.

A new course on the MC68030, MTTA3, is now available at $95.

## *Literature* packs supply M68000 Family device and application information.

M68000 Family product literature has been assembled into three special, distinct assortments for differing interests. They include brochures, technical summaries and data sheets, benchmark reports, application notes, technical article reprints and other useful pieces.

The M68KPAK is the M68000 Family overview, from chips and software to board- and system-level products.

The M32BITPAK focuses on our top-o'-the-industry 32-bit products, featuring the MC68030, of course.

The M68KCOMPAK is oriented to the extensive M68000 Family communications capabilities.

## One-on-one design-in help.

Get engineer-to-engineer insight on designing-in the M68000 Family

**1-800-521-6274**

Call toll-free any weekday, 8:00 a.m. to 4:30 p.m., MST. If the call can't cover your needs, we'll have our local applications engineer contact you.

We're on your design-in team.

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**Please send me the following information on the M68000 Family.**

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- ☐ HDS-300™ Hardware/Software Development Station
- ☐ M68000KIT
- ☐ M68000 Family Communications Capability
- ☐ M68000 Family PLCC Packaging
- ☐ M68000 Family Audio Cassette Training Courses
- ☐ Literature Packs:
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  - 2 ☐ M32BITPAK (Family 32-bit)
  - 3 ☐ M68KCOMPAK (Communications)

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**PEOPLE**

# GENRAD'S ANDERSON MOVES FOCUS TO CUSTOMER SUPPORT

**CONCORD, MASS.**

Now that things are looking better for GenRad Inc., Robert E. Anderson, the company's new president and chief executive officer, says it's time to refocus the company's attention on customer satisfaction instead of stanching the flow of red ink. The 46-year-old Anderson was named to head the automatic-test-equipment company at the start of the year [*Electronics*, Jan. 21, 1988, p. 94] in a move that surprised analysts who track the business. The betting had been that Richard Rogers, the front man in all the cost-cutting moves that brought GenRad under control over the past 18 months, would succeed William Thurston, now chairman. Rogers was executive vice president and chief operating officer until his recent resignation from the company.

Insiders say GenRad's board chose Anderson because Rogers was considered to be better as an inside man than as a CEO. Anderson points out that the harsh cost controls stemmed from a team effort, and that he was a prominent player. The major move was cutting 1,100 employees and closing down the Semiconductor Test Divsion. "I recommended that the division be closed, and that was tough to do," he says. The move took GenRad out of the VLSI test business—a decision that was made because the operation would have been a drain on profits until a new test system could begin to produce revenues.

GenRad has been through some tough times lately. The company lost money for nine quarters in a row before it reported a profit from continuing operations in last year's third quarter. And though it isn't out of the woods yet, Anderson says he's encouraged by the latest results. Revenues of $194 million for the year ended Jan. 2 were up from last year's $177 million. There was a net loss of $37 million, but it is all attributable to writeoffs associated with closing the Semiconductor Test Division in Milpitas, Calif. In addition, there was income of $2 million from continuing operations.

Anderson interprets that as a sign that the company can put "the hardest times" behind it and move customer service to the top of the priorities list. "GenRad has a long history of being strong in that area," he says, "but over the past few years—through rapid growth and decline—other priorities came along. You can get into cost-cutting modes that overlook customer satisfaction, which I think will become the differentiating factor in U.S. business."

To prevent it from becoming a hollow wall-poster theme, Anderson met with almost all GenRad employees within a week of his appointment to alert them that customer support is the company's primary goal. Further, he intends to "greatly step up our investment in employee training to teach them more about quality needs."

Now that GenRad is out of VLSI device testing, Anderson says the product focus will be on better board testers, with a strong emphasis on quality-management software and design-to-test links. In fact, Anderson will reemphasize a 10-year-old GenRad slogan: "The difference in testers is the difference in software." Evidence of that came in January with the introduction of GR-EXCEL, a series of hardware and software packages that extends the combinational testing and fault-diagnostic abilities of the GR 2276 board test systems.

The GR-EXCEL software is intended to ease the time-consuming problems of preparing functional test programs and fault diagnostics for printed-circuit boards containing application-specific ICs, surface-mount devices, and high-density VLSI devices.

"There's a lot more work to be done in linkages for design verification," Anderson points out. To make sure that GenRad does that work, "I intend to be close to the customers, to our products, and to our operations," Anderson says. "That level of closeness is vital, and that will be my style," adds the new president. *–Lawrence Curran*

**Robert Anderson** says that after nine losing quarters in row, the worst is over for ATE manufacturer GenRad.

# THE SOFTWARE PROBLEM SOLVERS

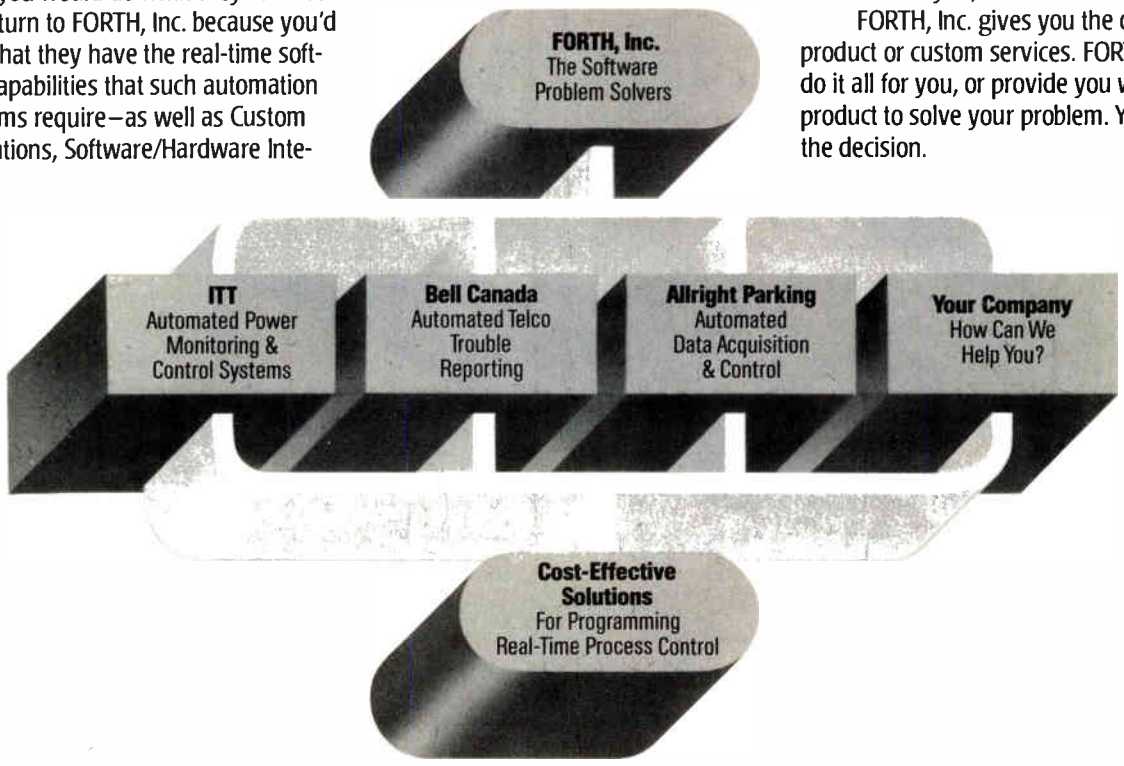
If you were ITT and had to automate power monitoring and control systems for telephone power plants, who would you turn to? And what if you were Bell Canada and your purpose was to automate the company's trouble reporting, analysis, and control procedures? Or suppose you were the Allright Parking Company and had to automate the data acquisition and distributed control of a large number of parking facilities?

If you knew what those companies know, you would do what they did. You would turn to FORTH, Inc. because you'd know that they have the real-time software capabilities that such automation programs require—as well as Custom Applications, Software/Hardware Integration, Installation and Training, Ongoing Maintenance, and Hot Line Support.

And if yours is not a custom application, FORTH, Inc. also offers its powerful family of polyFORTH software and related hardware products. These interactive development tools are compatible with the most popular computers from microprocessors to super-minis.

So, for applications-oriented products or expert help with your automation project, do what the major corporations are doing. Turn to FORTH, Inc., the "software problem solvers" who understand such real-time applications as process control, robotics, digital signal processing, machine vision, data acquisition and analysis, and networking.

FORTH, Inc. gives you the option—product or custom services. FORTH will do it all for you, or provide you with a product to solve your problem. You make the decision.

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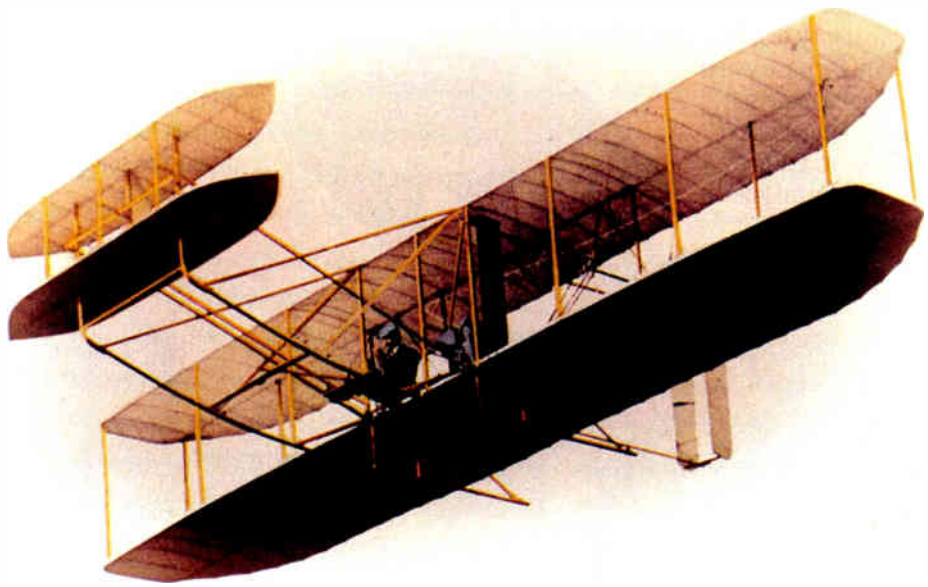
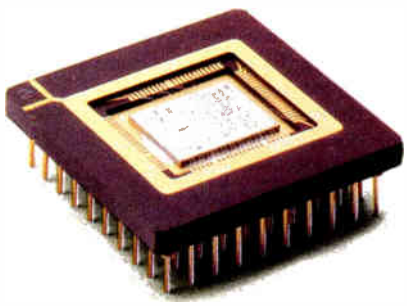
# "WITH THE EXCEPTION OF OBSERVATION, I SEE NO MILITARY USE FOR IT."

## AMERICAN GENERAL, 1908



# "IT'S GOT POSSIBILITIES, BUT IT'S JUST TOO POWERFUL FOR MY APPLICATION NEEDS."

## DESIGN ENGINEER, 1988



Over the centuries, people have looked at the latest in technology with a bit of skepticism. The Transputer from INMOS is no exception.

When we first introduced the Transputer, designers were indeed intrigued. They were impressed with our T800—a 32-bit floating point microprocessor with an average speed of 10 MIPS and the ability to sustain 1.5 MFLOPS or 4.0 million single precision whetstones. "Incredible," designers said. "But it's more than we can use."

Not true. The fact is as a stand-alone processor, the T800 gives you benefits you can use every day. It runs programs even faster than Intel's combined 80386 and 80387 or Motorola's combined 68020 and 68881. Plus, it requires significantly less memory to hold compiled code.

And, by increasing the number of Transputers, you can increase system performance proportionally with no limit to the number of Transputers that can operate concurrently. Like linking seven T800's together to give you the processing power of a mighty Cray 1S supercomputer.

Or you could use ten IBM add-in cards from INMOS carrying ten T800's each, to enable your desktop PC to deliver 150 MFLOPS. That's like having the power of 150 11/780 VAX machines right at your fingertips.

So take another look at the Transputer. It's not just a dream for the future, it's a high-performance product for today. And it's a technology that is already taking off.

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## LETTERS

### Intel's still the EPROM leader

**To the editor:** Your special report on ISSCC 1988 [*Electronics*, Feb. 18, 1988, p. 67] was extremely well-written and fair—with the exception of one statement: "The *one-time* leader in ultraviolet-erasable programmable read-only memories is striking back."

According to Dataquest, in 1987 Intel represented nearly 19% of the total worldwide EPROM market (units shipped). The next highest share belongs to Hitachi at 11.5%. Further, Intel shipped more 128-Kbit, 256-Kbit, 512-Kbit, and 1-Mbit EPROMs than any other supplier in 1987.

Beyond densities from 16 Kbit to 1 Mbit, Intel's EPROM line includes n-MOS, CHMOS, plastic OTP, and surface-mount plastic leaded chip-carrier packages, and a variety of architectures, speeds, and temperature ranges to accommodate the varying needs of EPROM users. As a result, we have to disagree with your assessment of Intel being a "one-time" leader. I think the facts paint a different picture.

*Janet L. Woodworth*
*Senior Product PR Specialist*
*Memory Components Division*
*Intel Corp., Folsom, Calif.*

### MMIC amps from another source

**To the editor:** In an *Electronics* newsletter [*Electronics*, March 3, 1988, p. 22], you describe Harris Microwave Semiconductor's HMM-10620 2- to 6-GHz MMIC amplifier as worthy of note largely for its low power, with a typical chip power consumption of 65 mA.

Pacific Monolithics has been building and marketing GaAs MMIC amplifiers for over three years. For about one year, we have been producing the PM-AM0609 2- to 6-GHz GaAs monolithic amplifier, which draws only 40 mA typically for 12 dB of gain, resulting in a figure of merit value of 3.3 mA/dB compared with the HMM-10620's value of 3.5 mA/dB. The PM-AM0609's output power is 14 dBm, whereas the Harris part delivers only 13 dBm.

Pacific Monolithics also has an earlier 2- to 6-GHz amplifier, the PM-AM0607, which has 10 dB of gain and draws only 20 mA, for a figure of merit of 2.0, which we believe to be the best available for this kind of part. (The power-out level of the PM-AM0607 is 5 dBm, making it a truly useful low-current microwave gain block.)

*Cedric R. Braun, Comm. Manager*
*Pacific Monolithics Inc.*
*Sunnyvale, Calif.*

**Correction:** The story about Vitesse Semiconductor Corp.'s gallium arsenide static random-access memory chips [*Electronics*, March 31, 1988, p. 95] incorrectly identified the chips as 16-Kbit parts. The chips are 1-Kbit, organized 256 by 4.

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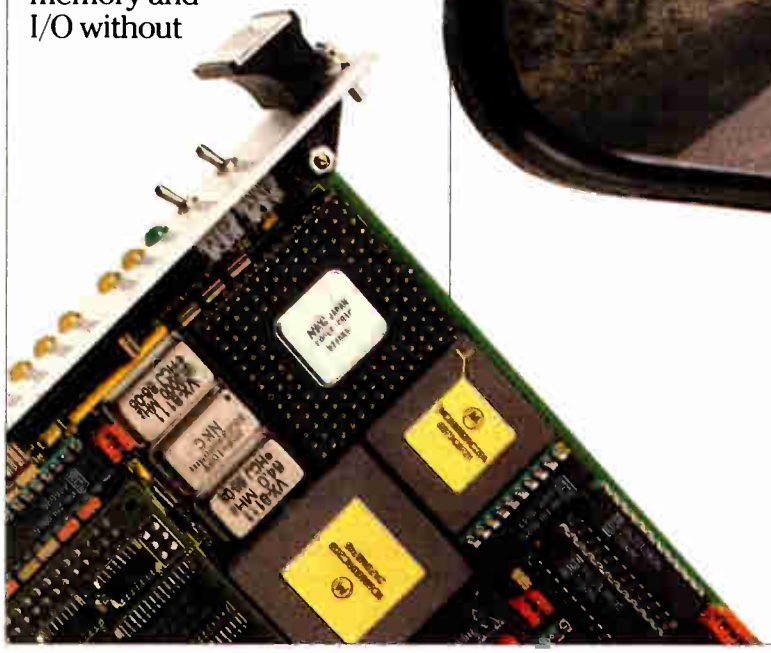

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# ELECTRONICS NEWSLETTER

## SUN FIRES A SALVO AT OS/2 WITH ITS UNIX-BASED 386i BUSINESS COMPUTER

Sun Microsystems Inc. is arming itself to invade the business computing market—and to help the Unix operating system gain an edge over Microsoft Corp.'s OS/2. With the introduction April 6 of the Sun 386i, the Mountain View, Calif., company has its first entry into the business market. The new machine is "Sun's armor-piercing bullet to get into business computing," says Brad Smith, director of research in the technical computer group at Dataquest Inc. of San Jose, Calif. He says the 386i could bring Sun $100 million to $200 million in revenues this year alone. But Sun isn't just trying to squeeze its way into the office market—it's fighting to make Unix the standard operating system for business users, instead of OS/2, the successor to MS-DOS designed for IBM Corp.'s Personal System/2 line. Computer analyst Jonathan Seybold says that with the 386i, Sun and Unix-developer AT&T Co. have the opportunity to move the computer industry more firmly toward Unix and away from OS/2, in part because the machine is the first work station based on Intel Corp.'s 80386 microprocessor to merge Unix with MS-DOS applications. □

## WHY IS IBM LETTING COMPETITORS PEEK AT ITS CHIP TECHNOLOGY?

IBM Corp. startled the industry early in April by admitting that it has supplied a limited number of semiconductor chips to Digital Equipment Corp. and other computer makers. The disclosure left many in the computer industry wondering about IBM's motives: Why is IBM, notoriously closemouthed about its chip technology, willing to offer it to arch competitors like DEC? "I doubt that it's out of the goodness of IBM's heart," says Harvey Cohen, president of BIS-Mackintosh, a consulting and market analysis firm in Boston. "It could be that IBM is trying to get a sense of where it stands in terms of price, performance, and technology, compared to other suppliers. We see a trend toward firms with captive semiconductor divisions becoming more aware of the market. They have to be competitive with the world outside, or they have no edge." Kenneth Bosomworth, president of International Resource Development Inc., a Norwalk, Conn., market analysis firm, says IBM may be worried that its traditional strategy of always doing things its own way could backfire. "IBM may be quite disturbed by the possibility that it's going off on a limb by itself while most of the industry is going to more standard chips and architectures," he says. "The position of the nonconformist has become precarious." As to who else might have been the recipient of IBM chips, no one is saying. Control Data Corp. and NCR Corp. both deny being on the receiving end, and Unisys Corp. refuses to comment. □

## DIGITAL GOES OPTICAL WITH 12-INCH WORM DRIVE

Optical memory is getting a powerful endorsement from Digital Equipment Corp. The Maynard, Mass., company is easing into the optical-memory market with its first offering, a write-once-read-many-times (or WORM) disk drive. The RV20 uses removable 12-in. platters and is being sold as a storage subsystem for DEC's VAX computers. The $30,000 unit can store up to 2 gigabytes of data and is driven by new media-management software DEC calls the Storage Library System. DEC isn't making the drives itself, but it also isn't saying who is. CAP International, however, a Marshfield, Mass., market research and consulting firm, says the drives are probably supplied by Laser Magnetic Storage Inc., Colorado Springs, Colo., a joint venture between Philips of the Netherlands and Control Data Corp. of Minneapolis. What's up next for DEC? Scott McCready, CAP International's associate director for image-communication systems, says he expects this introduction of a WORM drive will be closely followed by a VAX-supported optical jukebox. □

# ELECTRONICS NEWSLETTER

## TI WILL HAVE AN ADA COMPILER FOR ITS NEXT-GENERATION DSP

Texas Instruments Inc. and an unnamed software firm are planning to break new ground for military users of digital signal processors with the first military-certified Ada language compiler for a DSP chip. They are on the verge of signing a joint-development pact aimed at providing by mid-1989 a verified Ada compiler for a military version of TI's next-generation 32-bit DSP, called the SMJ320C30. The 32-bit 320C30 has integrated floating-point capabilities and can achieve 33 million floating-point operations/s [*Electronics*, March 19, 1987, p. 21]. For TI, the move represents a further effort to strengthen its grip on the DSP chip market. The Dallas-based chip maker boasts about 68% of U. S. DSP chip sales, says analysts Will Strauss of Forward Concepts of Tempe, Ariz. He says the deal is important to TI because of the military portion of the DSP market, which he estimates will be about one-third of a total $813 million market in 1988. □

## EVANS & SUTHERLAND TO OFFER A 1-GIGAFLOPS SUPERCOMPUTER FOR GRAPHICS

Evans & Sutherland Computer Corp. is leaping into the graphics supercomputer fray. The Salt Lake City pioneer in high-performance graphics says its computer division in Mountain View, Calif., is completing development on a high-end general-purpose supercomputer optimized for simulation and modelling applications. The new machine will cost between $3 million and $8 million when it hits the market late this year. E&S is boasting very fast scalar performance for the top-of-the-line model—over 1 billion instructions/s and 1 billion floating-point operations/s. The moderately parallel architecture offers one to eight processors, each with 16 computational units. E&S says each computational unit is a high-speed computer in its own right, with performance equal to about half that of an IBM Corp. 3090 mainframe. □

## NOW THERE'S AN ELECTRONIC MAIL SYSTEM THAT GOES SOMEWHERE

The problem with electronic mail systems is that they have always been limited to single networks. Users that needed to communicate with people on other networks were locked out. But 3Com Corp. of Santa Clara, Calif., has come up with a solution: a product that gives users of the company's 3+ network operating system a gateway to MCI Communications Corp. electronic mail service. The $595 software package, called 3+Reach/MCI, enables users with 3+Mail to exchange messages with telex addresses, MCI Mail's more than 100,000 users, and any postal address with MCI Postal Delivery capabilities. The software also allows the user to connect to other electronic mail systems such as IBM Corp.'s PROFS, Digital Equipment Corp.'s All-in-1, and Wang Laboratories's WangOffice, among others. □

## SHOULD FEDERAL RESEARCH CENTERS COMPETE FOR WORK?

The special relationship the government has with its 36 federally funded research and development centers—such as Los Alamos National Laboratory in Albuquerque, N. M., or the Jet Propulsion Laboratory in Pasadena, Calif.—doesn't always benefit the government, according to a report released by the U. S. General Accounting Office. The GAO says that while the centers offer certain flexibility and conveniences, they also exist in a noncompetitive environment that doesn't always net the government the best price or the finest work. So the GAO is recommending that the government issue broad agency announcements based loosely on proposals put forth by the centers in order to compare them with competing offers. If the GAO gets its way, the Pentagon—the biggest user of these centers—will soon begin using the announcements on a trial basis. □

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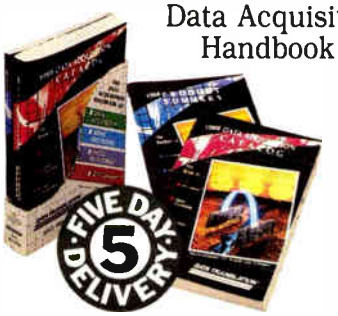


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Circle 24 on reader service card

# PRODUCTS NEWSLETTER

## NEC DELIVERS A 500-FOLD SPEED BOOST IN A GRAPHICS IC...

Work stations geared for high-speed graphics can get a speed boost thanks to flash-write circuitry in NEC Corp.'s 1-Mbit graphics buffer that also has a random-access-memory port and a serial port. The μPD42274's new flash-write facility transfers the contents of 512 by 4 bits in a color register into 2,048 data bits in one clock cycle—compared with 512 clock cycles in standard dual-port RAMs. The device's RAM-port configuration is 256-K words by 4 bits, and versions with 100- and 120-ns access times are available. Serial-port configuration is 512 words by 4 bits. Chip size is 6.24 by 13.52 mm. Tokyo-based NEC says that it will provide sample quantities of the μPD42274 for 8,000 yen each in May, with production scheduled in October. The chips come in three types of 400-mil packages—zig-zag in-line, J-leaded small-outline, and dual in-line. □

## ...AND MAKES ITS 16-BIT V33 RUN FOUR TIMES FASTER THAN ITS PREDECESSOR

The speed race in 16-bit microprocessors is heating up again with NEC Corp.'s 16-MHz V33—an enhanced version of the Tokyo-based company's 10-MHz V30. Fabricated in 1.2-μm CMOS, the V33 runs at 2.8 million instructions/s, four times the V30's speed. NEC engineers did it by separating the address bus from the data bus and using hard-wired logic. The V33 is software-compatible with the V30. But, unlike the V30, it is not compatible with Intel Corp.'s 80286, because its does not incorporate a memory-management unit and has a different address space structure. The V33 features an extended address mode for 16 Mbytes of memory address space, and a dynamic bus sizing that lets it match up with 8-bit data buses. Samples will cost 20,000 yen starting in May in both the domestic and overseas markets. A low-cost, 12.5-MHz version will cost 15,000 yen. □

## MICROCHIP CUTS WEEKS OFF DSP DESIGN BY LINKING THREE TOOL SUITES

Designers of digital signal processors can cut weeks off the time needed to get functional assembly code for Texas Instruments Inc.'s 32-MHz 320C10 processor with Microchip Technology Inc.'s MicroWorkshop Development System. Instead of the conventional method of using separate editing, assembly, and testing tools, the Newport Beach, Calif., company combined all three in a single software package that runs on IBM Corp. Personal Computers XT, AT, and compatibles, including those based on 80386 processors. By incorporating Microsoft Corp.'s Windows software, the MicroWorkshop lets designers display code, text, and captured waveform graphics on the screen simultaneously—the first DSP development system to do so, the company says. The system consists of the editor/assembler/testing software plus custom enhancement boards. Available in May, it costs $9,995. □

## CRYSTAL SEMICONDUCTOR GOES FOR BROAD NEW MARKETS WITH 16-BIT ADC CHIPS

Two low-cost monolithic 16-bit analog-to-digital converters from Crystal Semiconductor Corp. promise to open large new markets: one targets measurement and control applications and the other digital-audio-tape machines and related markets. The Austin company's CS5501 is an inexpensive alternative to the hybrid circuits now used. The low-speed, delta-sigma ADC combines advanced digital filtering, calibration circuitry, and control features that allow it to be mounted right next to a sensor; a serial link returns data to the system. The CSZ5126 for high-fidelity digital audio is a derivation of the earlier CSZ5116; it offers a 92-dB dynamic range and harmonic distortion of better than 0.002%; its 240-mW power needs suit it to portable decks. The 1,000-piece prices are $13.60 for the CS5501 and $27.20 for the CSZ5126. □

# PRODUCTS NEWSLETTER

## IMAGRAPH FRAME GRABBER IS PROGRAMMABLE TO ANY VIDEO-IMAGE FORMAT

System integrators of equipment for medical imaging, computer-aided design and computer-aided engineering, and seismic analysis can sidestep the problem of customizing a solution for every common video format with the Digital Frame Grabber board from Imagraph Corp. Compatible with IBM Corp.'s Personal Computer AT and clones, it can be programmed to handle almost any video-image format, including NTSC, PAL, the IEEE RS-330 and High-Definition TV, say executives at the Woburn, Mass., company. In addition to its programmability, the Digital Frame Grabber boasts 1.25 Mbytes of video memory—more than double the memory of its closest competitor, which also lacks video format progammability. The Digital Frame Grabber is available now, priced at $4,500. □

## HP's NEWEST RISC-BASED COMPUTER RUNS UP TO 75% FASTER THAN SUN 4/260

Hewlett-Packard Co. is adding three new products to its HP 9000 model 800 series computer line. The trio, based on the company's HP-PA reduced-instruction-set architecture, will deliver significantly better price/performance than the competition, HP claims. The computing-intensive 835S, for example, runs the Unix operating system and boasts performance of 2.02 million double-precision floating-point instructions/s. That's 75% faster than a Sun Microsystems Corp. 4/260 but at a comparable price, says the Palo Alto, Calif., company. The HP9000 model 855S will be the company's new performance leader when it becomes available in 1989, offering 50% better performance than the 835S. The 30-user 835S costs $45,000 and will be available in the third quarter of this year. The 855S will cost $320,000; the midrange 835SE, which handles up to 70 users, costs $99,000. □

## TI'S BIPOLAR FIFOS RUN 70% FASTER THAN THE COMPETITION

Texas Instruments Inc. is using its 2-μm Impact-X bipolar technology in three first-in, first-out buffer memories to achieve 30-ns maximum fallthrough time—the delay between clocking data in and clocking it out. That performance makes the 64-by-8 bit SN74ALS2232 and the 64-by-9-bit SN74AL2233 and 2234 70% faster than competing FIFOs with similar architectures, say product managers in Dallas. The delay takes zero clock cycles, running at 40 MHz, to complete the fallthrough time. All three devices can be cascaded to serve 16- and 32-bit buses, and the the 2234 can be cascaded in depth as well. All three feature full and empty status flags, and the 2233 also has half-full, almost-full, and almost-empty flags. In 1,000-piece quantities, the 2232 and 2233 are now available for $18.77 in 28-pin plastic packages. Samples of the 2234 are ready, with volume production set for late in the second quarter. □

## PHOTONICS DOUBLES DISPLAY AREA IN ITS HIGH-RESOLUTION PLASMA SCREEN

Integrators of medical imaging, military command, and computer-aided design/manufacturing systems that demand the largest possible display can now get more than double the competition's active area in Photonics Technology's 2,048-by-2,048-pixel display. The PTT-2048-2048-48.8 terminal is based on black-on-white plasma-discharge technology. The terminal's screen measures 42 by 42 in. and boasts 50-line/in. resolution. Its matrix more than quadruples the 1,000-by-1,000-pixel resolution attained by competing products that project images on a screen. The terminal features a 32-bit Motorola Inc. 68020 display processor/controller and terminal emulations for Digital Equipment Corp. and Tektronix Inc. products as well as the North American Presentation Level Protocol Syntax (ANSI X3.110-1983). The terminal is available now; prices start at $100,000 but vary with configuration. □

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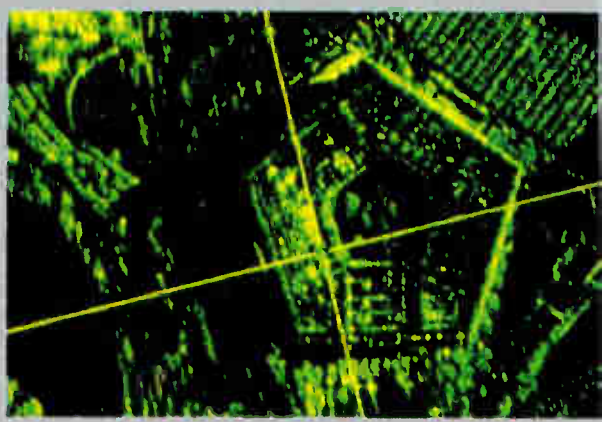

While developing software for the B1-B Bomber radar system, Westinghouse Defense landed on a tough problem – integrating its computer resources. "We needed a complete network that would allow hundreds of software engineers across the country to interact, create, enhance and modify the software," says Ron Clanton, Manager of Software and Information Systems.

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Remarks Clanton, "The network is so comprehensive, it extends even to the air in our Flying Software Lab. Giving us real-time, in-flight software testing and development capabilities. The Software Lab alone provides a cost savings of up to 98% versus traditional in-flight testing in the B1-B Bomber."

# "A networked software engineering environment that helped Westinghouse Defense zero in on ways to cut in-flight test costs by 98%."

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Clanton sums it up this way, "Our Digital network and The Flying Software Lab allow us to cut software development time and costs across the board. And that's increasing our productivity and ability to compete for similar projects."

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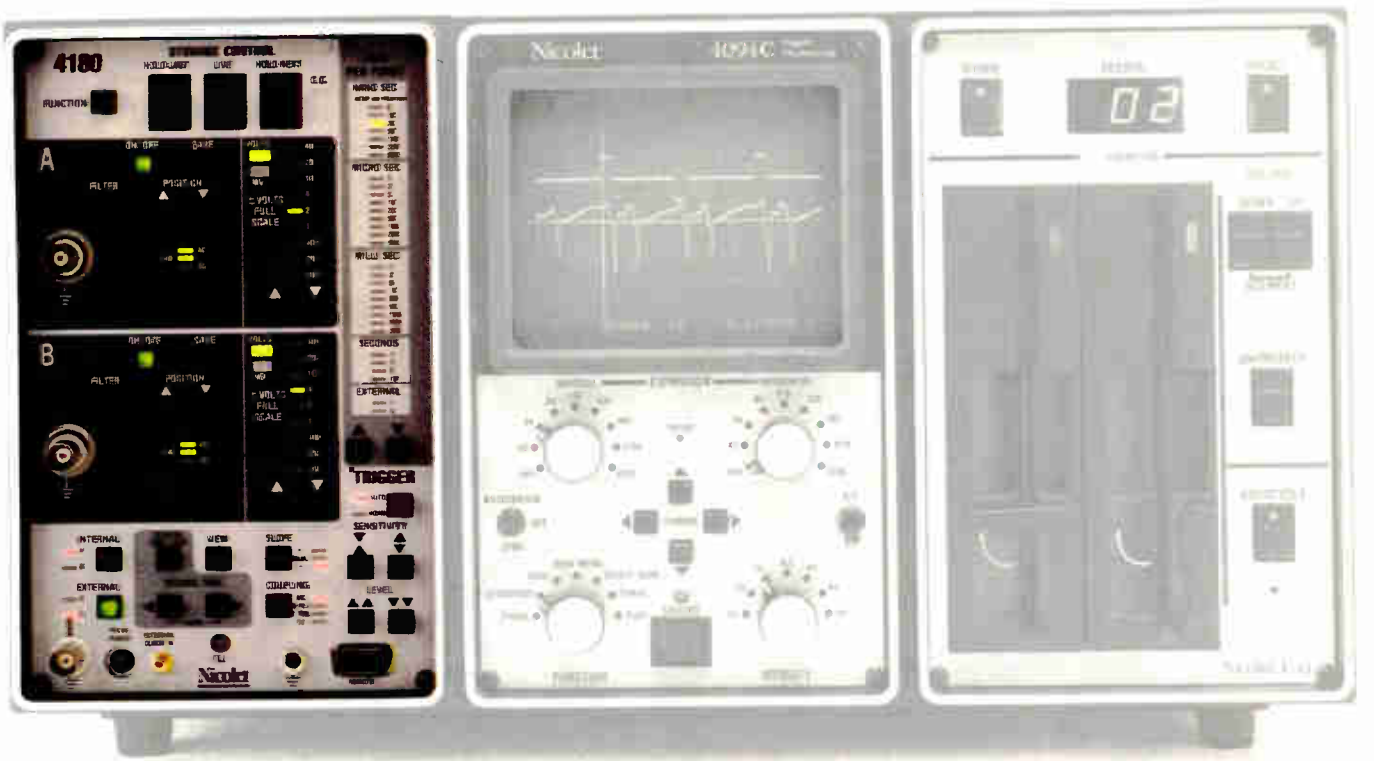


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# USERS BACKING MOTOROLA'S 88000 CHIP BAND TOGETHER AND JOIN THE RISC BATTLE

## New rival of Sun and MIPS camps pushes to make the processor a standard

**NEW YORK**

A powerful contingent of users is lining up behind the newest reduced-instruction-set-computer architecture. Started by early users of Motorola Inc.'s new 88000 RISC microprocessor chip, the organization was quickly backed by the chip maker as a way to build support for its processor—and to throw down the gauntlet to the two other major RISC camps pushing devices from Sun Microsystems Inc. and MIPS Computer Systems Inc.

The goal of the 88open group is open standards for all hardware and software system vendors using the Motorola RISC-chip family. It's moving fast. The 88000 is not even out of the starting gate—official introduction is scheduled for April 18. But the user group is set to formally announce on April 11 the formation of a consortium to work together on such issues as binary compatibility, hardware compatibility, and a common version of the Unix operating system for the RISC chip set.

Tektronix Inc., one of the first companies to reveal that it was designing with the 88000, was instrumental in setting up 88open. "We saw a rare opportunity in the industry to create a step function—to get a group together to develop standards for a significant new technology before the product is available," says Bob Anundson, work station group manager at Tektronix. Anundson and his collegues at the Beaverton, Ore., company decided there was a chance to create a standard environment in way that has not been done before. Anundson was one of the driving forces behind 88open.

The Motorola entry was previewed in February [*Electronics*, Feb. 18, 1988, p. 83]. The 88000 chip set will go head-on in the market against the Sparc chip designed by Sun and made by several foundries; the R3000 chip set offered by MIPS and its foundries; and a few others such as Intergraph's Clipper, AMD's AM29000, and Apollo's Prism. But it's the big three—Sun, MIPS, and now Motorola—that are fighting to line up enough system vendors behind their designs to make them industry standards.

There is no doubt that the 88000 consortium will help get Motorola's entry off to a fast start. Offiically called the 88open Consortium Ltd., the group signed up 17 members at its second charter meeting in Chicago on April 5.

**GROWING LIST.** Such computer industry stalwarts as Convergent Technologies, Stratus, and Tektronix top the list. For competitive reasons, Motorola says, the remaining members do not want to be identified until after they have announced their 88000-based products, which many plan to do at the April 18 coming-out party. However, Motorola expects that as many as 50 may join the group over the next few months.

"By creating a set of standards prior to building products, we are doing something hitherto unheard of and hope to maximize the leverage each member has in the marketplace," says Roger Cady, acting executive officer of 88open. "We plan to have a small paid staff for administration and coordination, but the major [standards] work will be done by technical subcommittees [of member participants]," says Cady, a former vice president of Digital Equipment Corp. The headquarters site has not been determined, but in the meantime, 88open is using as a contact point Cady's phone number: 603-778-3001. The organization also plans to open regional offices in Europe and the Pacific Rim.

Competing vendors adopting the 88open standards will be able to concentrate their development efforts on features and services that differentiate their products rather than on retrofitting products to multiple standards and carrying out endless porting activities. This will be particularly helpful to applications software vendors.

"Vendors have traditionally spent too much time porting and retrofitting software and hardware to individual, competing standards that quickly become obsolete," says Cady. "With the 88open [standards], multiple companies are combining around one single architecture and set of standards to provide greater, more cost-effective hardware and shrink-wrapped software," he adds.

Although Motorola obviously is a strong supporter of the 88open Consortium and is working hard to launch the organization, it is not yet clear exactly what official role the company will have in the organization. As formed, 88open is an independent organization open to companies and individuals that manufacture, develop, sell, or use products based on the 88000 architecture. The consortium is run by a nine-member board of directors that consists of representatives from hardware vendors, software vendors, the academic community, the membership at large—and only one board member from Motorola.


Convergent Technologies Inc. is another charter member. "Though not one of the instigators, we joined as soon as we heard about 88open," says Tom Mace, who represents the San Jose, Calif., company. "We thought it was a great idea; we want to see 88000 standards develop in a more coherent fashion than other systems have developed," he adds.

*–Tom Manuel, with reporting by Jonah McLeod*

# WHAT'S HOLDING UP THE PS/2 CLONES?

**NEW YORK**

A year has passed since IBM Corp. introduced its Personal System/2, and the biggest guessing game going in the computer industry now is "Where are the clones?" There's been much conjecture about when the first plug-compatible copies of the PS/2 Micro Channel models 50, 60, and 80 will hit the market, but there has been no product introduced.

Is every vendor with a product in the wings waiting for the first entry to see how strictly IBM protects its patents? Are they waiting for licenses from Big Blue? Or are technical problems holding things up?

A flurry of recent events indicates that the answers could be imminent. For one thing, IBM has just announced that it will ship its 2 millionth PS/2 later this month. Industry observers expect the company to introduce, perhaps as early as mid-April, a second generation of PS/2 machines. Some observers think that perhaps that big a lead on its would-be rivals—a second generation plus 2 million machines humming away—will induce IBM to start licensing its first-generation PS/2 technology.

But some market watchers believe that clone builders may also need a license from Computer Automation of Irvine, Calif., for its technology to automatically identify boards when they are added to the Micro Channel. IBM already holds one such license, and now Computer Automation has granted the first to anyone other than IBM—to Canon Inc. of Tokyo and to a computer company in Taiwan that Computer Automation won't identify. Muddying that picture is the school of thought that maintains that a license from Computer Automation is not required.

**WORKING MODEL.** Another happening along the road to a commercial PS/2 clone is the recent demonstration by Chips & Technologies Inc. and Adaptec Inc. of a working model of a personal computer compatible with the PS/2 model 50. To demonstrate that it is possible to clone a PS/2, the two companies used the CHIPS/250 chip set with VGA graphics, a complete seven-chip set of system logic circuits that Chips & Technologies introduced in January; Adaptec's ACB-2610 Micro Channel controller, also introduced in January; and Phoenix Technologies Ltd.'s Advanced ROM BIOS software.

The reduced chip count possible with the Chips & Technologies and Adaptec set will allow clone makers to top IBM's performance. "Makers of PS/2 compatibles now must raise the price/performance curve even more dramatically than IBM to be successful," says Gordon A. Campbell, Chips & Technologies' chairman.

Meanwhile, rumblings about just when the first Micro Channel-compatible product will emerge are circulating in the industry. A spokesman at Chips &Technologies in San Jose, Calif., says that the company believes that will happen this month, though he doesn't name the manufacturer. He adds that the company, in fact, expects several product announcements by the end of April and several more in May. And it is possible that a number of PS/2 clones will be shown at Comdex Spring in Atlanta May 9 to 12.

But some industry observers think that several issues may hold back the announcements for a while yet. For example, it's believed that a small crowd of potential vendors is still waiting for utility licenses from IBM that the big company is holding back because it really wants a two-year lead. Some others may be building up an inventory before announcing.

And still others may be busy doing some technical tweaking. Indeed, perhaps the most difficult barrier to breach on the road to the market is that PS/2 work-alikes will not be as easy to build as were the PC, XT, and AT copies [*Electronics*, Feb., 4, 1988, p. 34].

IBM may try to control the number of PS/2-compatible products through limited selective licensing. "I think IBM will license one compatible vendor by the end of this year; there won't be more than 10 [PS/2] compatible products on the market next year," says Robert Madge, managing director of Madge Networks Ltd. in Giles, England, Europe's leading supplier of IBM-compatible Token Ring network products. *–Tom Manuel*



# AIRCRAFT POWER CONTROL FINALLY GOES SOLID STATE

**BUENA PARK, CALIF.**

Believe it or not, the computer-driven avionics gear in military aircraft still depends on electromechanical power management. But that won't be the case for long: airplane builders are moving to upgrade that control task, the most visible one not yet handled by solid-state technology.

In April, the Leach Corp. will deliver an automated power-management system to Boeing and McDonnell Douglas. And it is more than just the first standard modules that assure an uninterruptible power flow to the growing number of airborne processors.

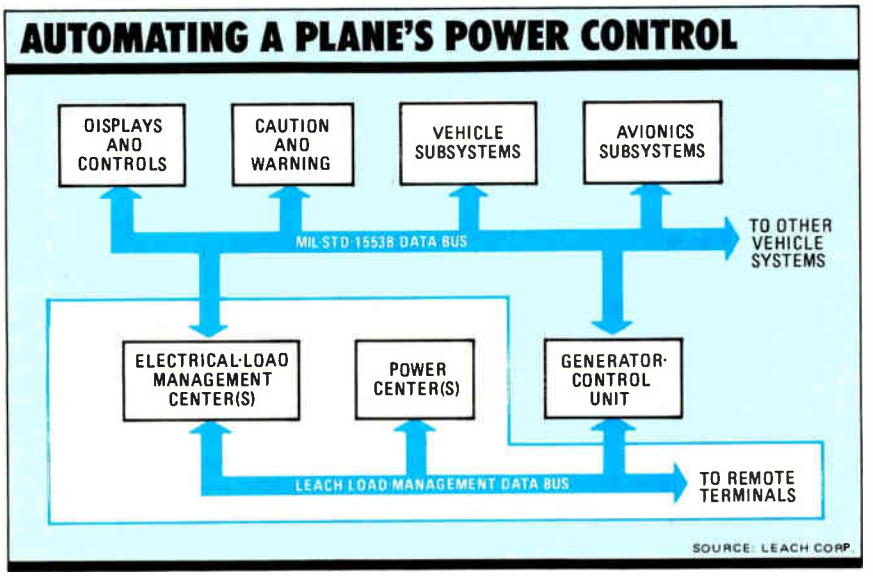
By applying fault-tolerant computer-control technology, the Leach equipment reduces the clutter of electromechanical gear, considerably simplifing pilot routines. Moreover, automated storage and analysis of data can provide better diagnostics for easier maintenance and better reliability, and lower costs over the life of the equipment.

The Leach power-management system arrives not a moment too soon. "The workload [electrical-power management] is at the point where the pilot can't spend the necessary time on it," says Ishaque Mehdi, manager of electrical system research at Boeing Co.'s Advanced Systems Division in Seattle. "This technology is the wave of the future, and crucial to keep aircraft flying." Adds Evan E. Clements, corporate director of research and development at Leach, "It has long been apparent to Air Force officials and plane designers that even a few seconds without backup power could be disastrous in an aircraft." The customary practice of visually monitoring and manually switching between power sources cannot be relied on any longer, says Clements, who directed the development.

**CATCHING UP.** The problem is that "electrical power systems have to catch up to digital avionics and control," says Michael Cronin, who manages secondary power work for Lockheed Aircraft Corp.'s Advanced Systems Engineering Division in Burbank, Calif.

For that reason, the Air Force earlier this decade put Boeing to work studying how to design future fault-tolerant computing and power systems for advanced aircraft. Based on conclusions presented in a 1984 report by Boeing, Leach immediately started on its version, financing the work with company funds. The privately held firm, with about $65 million annual sales, specializes in power and control products for the aerospace industry.

Leach set out to design a simplified fault-tolerant system that would make use of available components, such as




**Leach's** solid-state power-management system uses off-the-shelf parts, such as MIL-1750A microprocessors, to replace electromechanical circuit-breakers, relays, and switches.

MIL-1750A airborne microprocessors for computing, and entirely replace electromechanical circuit-breakers, relays, and switches with integrated circuits. The goal was to provide a fully automated operation with continuous electrical monitoring that senses problems in real time and reconfigures itself as required. In addition, the power system had to be modular so that it could be adapted to requirements of different craft, which can vary considerably.

At the heart of the Leach system is the electrical load management center, which distributes and controls power to all parts of the aircraft. It interfaces with the main avionics computer through a dual-redundant MIL-STD-1553B Data Bus (see figure); the pilot accesses it through cockput avionics displays. The 1750A processors are contained on cards in the management center, two of which are needed in the simplest system, along with at least one power center unit for bus switching and two remote terminal assemblies that can hold up to six power modules. These modules have controller devices and custom hybrid multiplex chips that decode and route commands from the load-management processor to the power units. The entire system can be configured by software to different mission tasks.

Leach will deliver a prototype system to Boeing to be integrated into a fault-tolerant electrical-power simulator being built for the Air Force's Wright Aeronautical Laboratory. The purpose is to write requirements for the Advanced Tactical Fighter for the next decade. Leach has also built an automated unit for McDonnell Douglas Helicopter Co. in Tempe, Ariz., for its advanced Apache craft, also to be shipped this month. And Lockheed is evaluating the Leach development for possible use on its P-3 aircraft.

Beyond that, Leach plans to market the gear in both system and component form to aircraft manufacturers worldwide, and for retrofitting existing planes. Commercial aircraft could present opportunities also, but not until the product has proven itself on military craft, Clements says. *–Larry Waller*

**VHSIC**

# AFTER THREE YEARS, A VHSIC CHIP STANDARD

**WASHINGTON, D.C.**

A milestone has been reached in the Very High Speed Integrated Circuits program's drive to promote interoperability among VHSIC chips. After more than three years of effort, a set of common electrical and bus specifications for use with 0.5-μm Phase 2 chips was agreed upon and delivered by the three Phase 2 contractors in February, says J. P. Letellier, an official at the Naval Research Laboratory in Washington, who spearheaded the interoperability effort.

By simplifying VHSIC chip testing, the standards will pay big dividends in maintaining future military systems, Letellier says. And by assuring that VHSIC chips from different manufacturers will work together on a common backplane—as well as with standard TTL devices—the specifications will simplify the design task for VHSIC-based systems. Finally, by establishing a larger common market for the devices, they should also encourage more investment by chip vendors in VHSIC-class technology, Letellier says. The effect will be multiplied later, as the standards also will be required eventually for new and redesigned circuits built in 1.25-μm Phase 1 VHSIC technology.

The benefits are likely to spill into the commercial chip world as well. Thanks to close cooperation by military officials with groups working on commercial testability standards, at least partial compatibility between the commercial and military chip worlds seems assured.

**FOUR SPECS.** The new VHSIC standards call out four separate specifications. An Electrical Interface Specification defines power supply, input/output voltage levels and drive currents, and clocks to be used with VHSIC Phase 2 chips. The other three specifications provide for standard buses covering interfaces at both the board and chip levels.

At the board level is the PI-Bus (for Parallel Interface Bus), a backplane bus that allows up to 32 boards to be connected. It can be implemented as 16 or 32 bits wide, each with two optional levels of error protection. Depending on loading, the bus will run at 12.5 MHz to 25 MHz.

A second backplane bus is aimed at test and maintenance functions. The TM-Bus (for Test and Maintenance Bus) is a 32-bit serial bus that handles the same 32-node set and uses the same addressing scheme as the PI-bus. It will typically run at a 6.25-MHz clock, and allows for the downloading of test routines and instructions from a single maintenance node.

Third is the ETM-Bus, to handle the same function at the chip level. Up to 32 chips can be connected in a variety of configurations. The ETM-Bus operates at 1/16th the speed of the VHSIC system clock, which can be up to 100 MHz.

Already, a committee of the Joint Integrated Avionics Working Group has recommended the PI-Bus and TM-Bus for use on the Air Force's Advanced Tactical Fighter, the Navy's Advanced Tactical Aircraft, and the Army's Advanced Tactical Helicopter.

The ETM-Bus will apparently have a counterpart on the commercial side. VHSIC backers have been working with a group known as the Joint Test Action Group, led by Philips of the Netherlands, which is also developing standard test methods for VLSI circuits. JTAG recently agreed to have the standards that it has developed incorporated as part of

corporated as part of another proposed standard. That standard is being readied by the P1149 testability bus standardization committee of the Institute of Electrical and Electronic Engineers, says committee chairman Jon L. Turino, president of Logical Solutions Technology Inc., Campbell, Calif.

Although some minor differences remain to be worked out, "it looks like the JTAG bus and the ETM-Bus will become essentially the same bus," says Letellier. The JTAG bus requires the use of four pins per chip, while the ETM-Bus in its current form requires six. But VHSIC backers are willing to multiplex two of the six pins in future versions of the ETM-Bus specification, thereby providing JTAG bus compatibility on four of the pins, Letellier says. A fifth pin, which is required by the military, will be made optional in the proposed IEEE standard. *–Wesley R. Iversen*

**DESIGN AUTOMATION**

# TEK-MENTOR DEAL MAY SOLVE A SLEW OF PROBLEMS

**BEAVERTON, ORE.**

It has all the earmarks of a match made in heaven—at least to the principals. When Mentor Graphics Corp. bought Tektronix Inc.'s computer-aided engineering and computer-aided software engineering businesses in early April, it solved a slew of problems for the two Beaverton, Ore., neighbors. Mentor did away with a formidable competitor and now will have access to Tektronix's installed base of equipment. The deal also relieved Tektronix of a struggling operation.

But the deal goes beyond that. The two companies squeezed competitor Hewlett-Packard Co. of Palo Alto, Calif., by signing a nonexclusive strategic alliance integrating their electronic design and test-and-measurement products. To handle that task, Tektronix has already formed a new Design and Test Integration Division. More ties could follow—Mentor executives hint that a computer-integrated-manufacturing product line could be next.

The deal could spell trouble for HP because until now, it has been the only company offering a full design-to-test solution. But HP is still not a major force in design automation or application-specific integrated-circuit design verification, areas where the Mentor-Tektronix tandem excels.

Other companies, notably Valid Logic Systems Inc. of San Jose, Calif., have also targeted an integrated design-to-test solution. But these smaller companies lack



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# MEMORY MANAGEMENT

IN THE ERA OF

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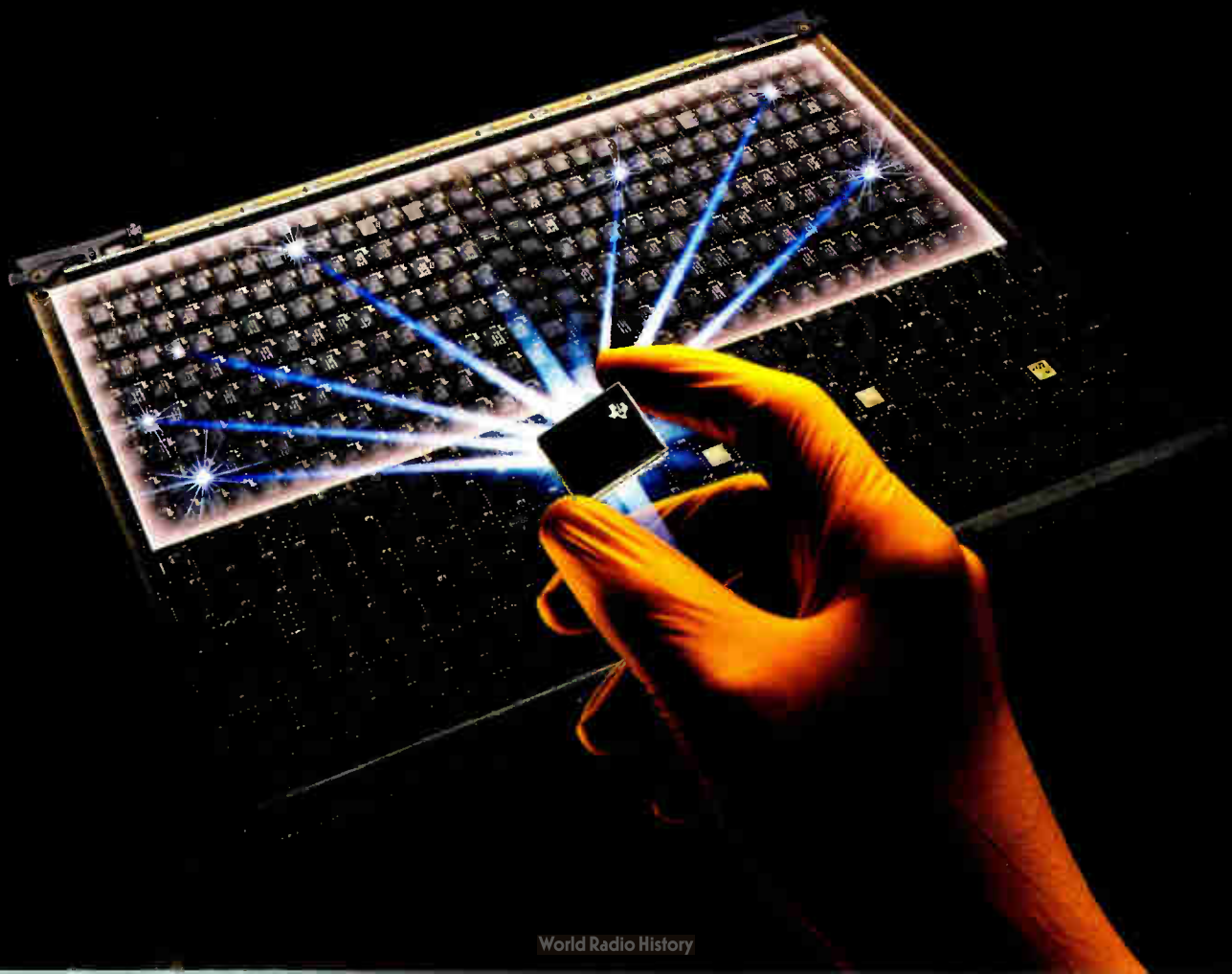

Memory management in the Era of MegaChip Technologies:

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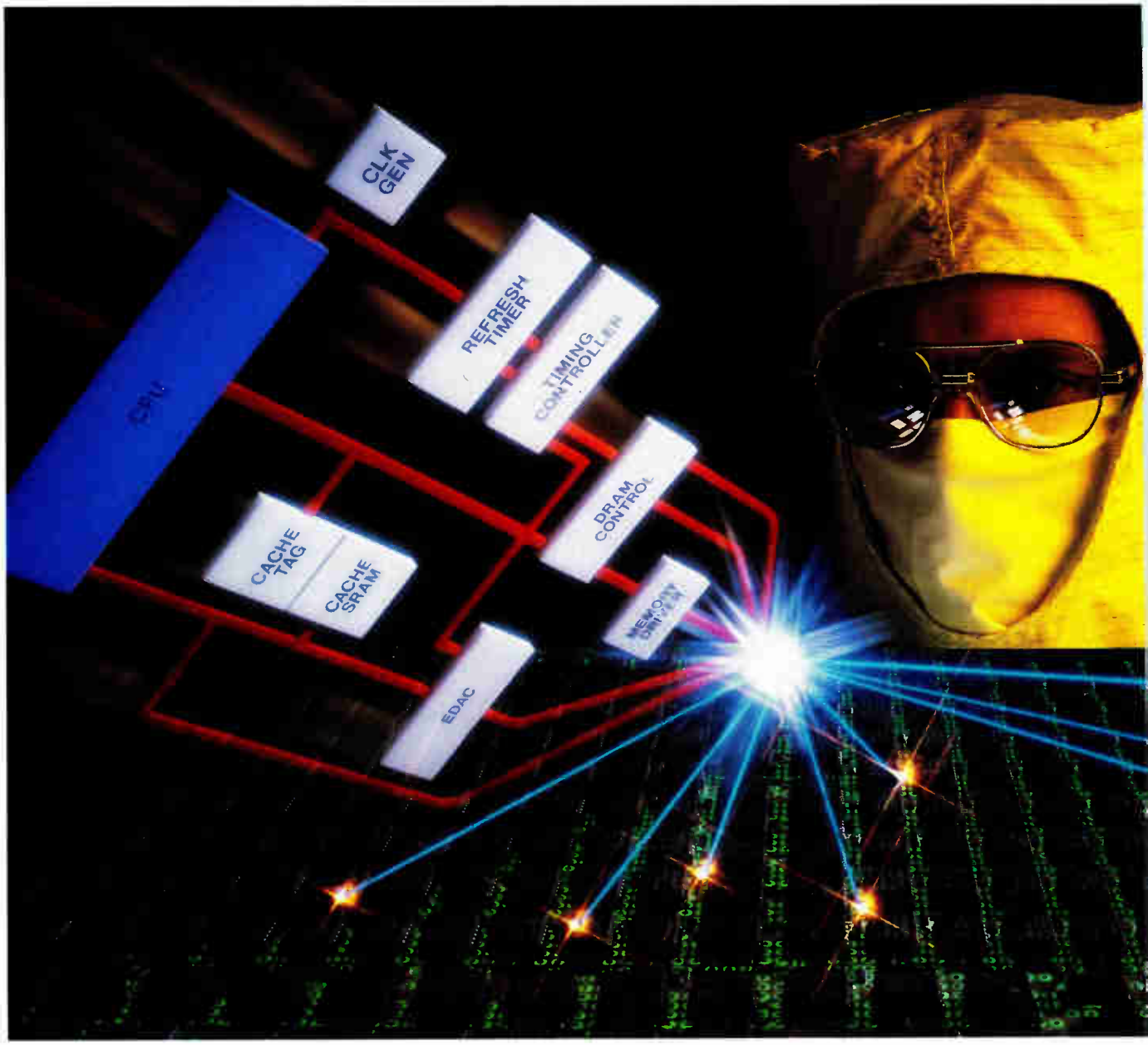


**Memory systems are a prime area for significant improvements in overall system throughput. Read how TI's memory-management ICs can get you in and out of memory faster no matter which processor you choose.**

You can now solve a problem whose solution has eluded design engineers for years: How to catch memory speeds up to CPU speeds. The solution lies with TI's advanced memory-management circuits, and you can use them with whichever processor best suits your application.

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A universal architecture enables these TI devices to work with — and enhance — virtually any high-speed microprocessor or bus structure, even custom engines.

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## TI addresses your major memory-design concerns

*To immediately improve memory-access time,* use both main and cache memories, as shown in the block diagram. This approach can produce up to a 3X increase in system performance.

Frequently accessed data and instructions are stored in a few high-speed static random-access memories and "tagged" by a TI industry-standard cache controller (SN74ACT2151/4). These 2K×8 CMOS controllers are the fastest available and can support deep cache architectures of 16K or even 32K.

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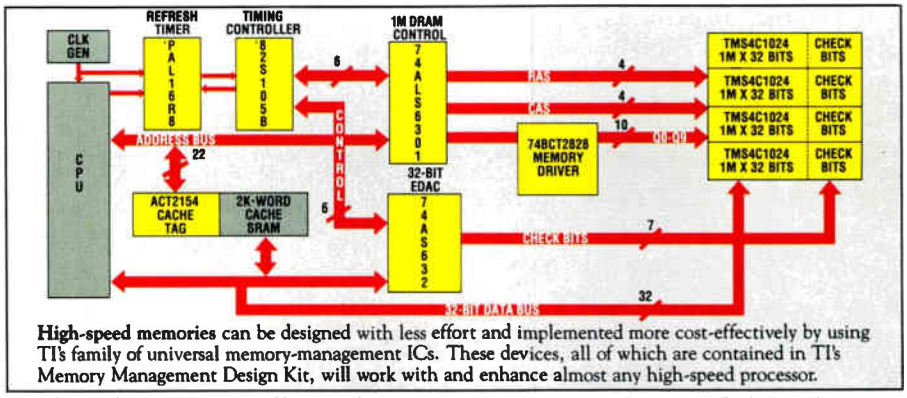
Our emphasis on volume manufacturing of high-density circuits is the catalyst for ongoing advances in how we design, process, and manufacture semiconductors and in how we serve our customers. These are our MegaChip™ Technologies. They are the means by which we can help you and your company get to market faster with better, more competitive products.

tions on chip to improve flexibility and speed and to allow for custom timing routines. This controller supports nibble- and page-mode access and scrubbing-mode refresh to increase memory output.




**High-speed memories can be designed** with less effort and implemented more cost-effectively by using TI's family of universal memory-management ICs. These devices, all of which are contained in TI's Memory Management Design Kit, will work with and enhance almost any high-speed processor.

This scheme is cost-effective because slower, less expensive dynamic random-access memories (DRAMs) can be used for main memory.

*When you must assure system integrity,* use of an error-detection-and-correction (EDAC) circuit can improve system reliability 500-fold. Since this approach is necessary with memory arrays larger than half a million bits, TI offers its leadership 32-bit EDAC.

The SN74AS632 detects dual-bit errors and detects and corrects single-bit errors while avoiding processor wait states. And at 25 ns for error detection, it meets your high-performance needs.

*Interfacing between processor and main memory* gets tougher as speeds increase. But TI has the SN74ALS6301 DRAM timing controller. It can handle any DRAM up to 1 Mbit and incorporates only the essential func-

Soon to come: An ASIC (application-specific integrated circuit) solution.

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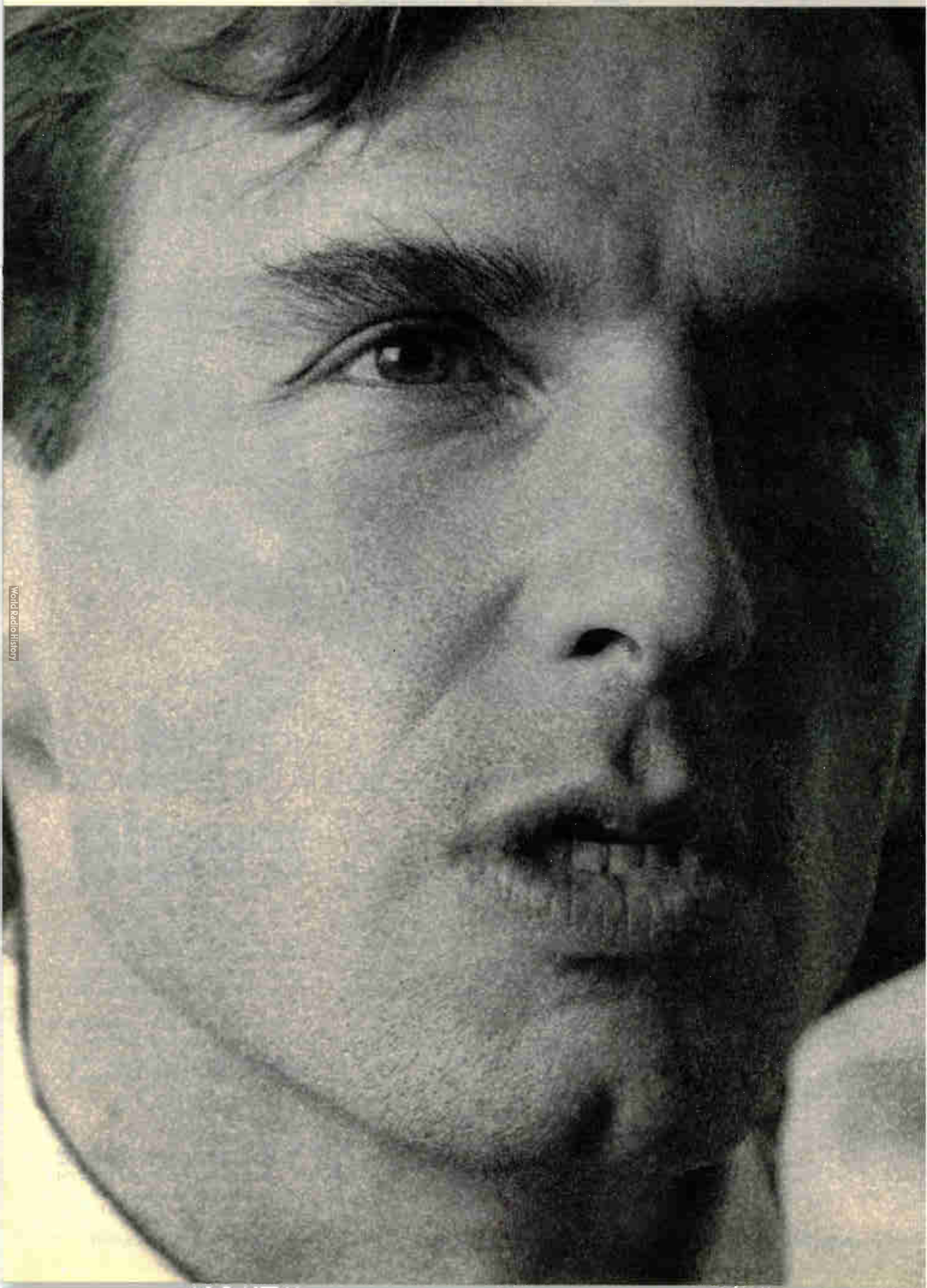
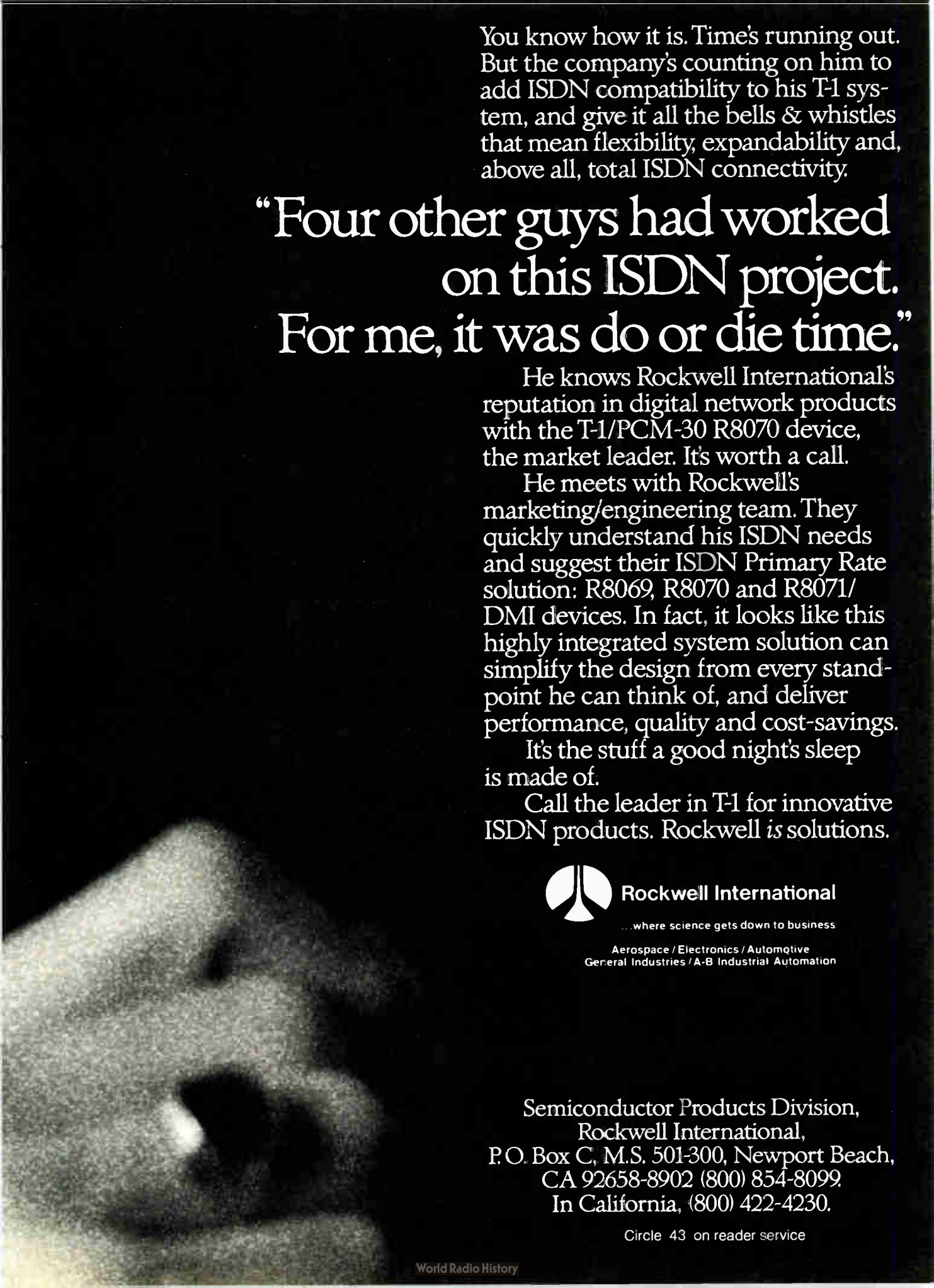
TEXAS INSTRUMENTS





You know how it is. Time's running out. But the company's counting on him to add ISDN compatibility to his T-1 system, and give it all the bells & whistles that mean flexibility, expandability and, above all, total ISDN connectivity.

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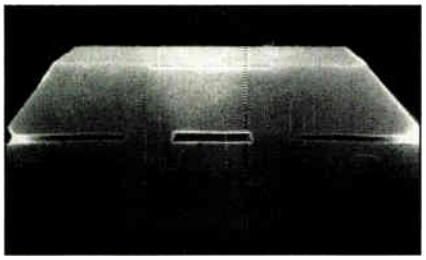

**Cross-section** of GTE's laser: light-emitting area is the black rectangle in the center.

ing the new devices, GTE scientists expect to be able to send 200 to 400 video channels over a single fiber, transmitting digital signals in computer networks at 16 gigabits/s or 4 to 8 gigabits/s in optical interconnections between circuit boards in supercomputers. The light-emitting layer of the lasers is composed of indium, gallium, arsenic, and phosphorous.

Using earlier versions of these devices and traditional satellite communication techniques, the Waltham team has already demonstrated an experimental system that carries 60 video channels over a single fiber. Robert Olshansky, senior staff scientist at the labs and principal investigator for the laser project, says that field trials are planned for this year of a system for military communications with a bandwidth of 17 to 18 GHz. Such a system would deliver data rates of at least 17 to 18 gigabits/s. In contrast, the promised Fiber-optic Distributed Data Interface standard will handle 100 Mbits/s when it is available.

To produce the lasers, GTE Labs employed conventional liquid-vapor-phase epitaxy to deposit the indium, gallium, arsenic, and phosphorous layers between two layers of an InP wafer substrate. Chemical etching follows to produce the four-layer structure, Olshansky says, which is a crystal about 1 $cm^2$ that yields 500 diode lasers.

The 22-GHz frequency was achieved by decreasing the width of the light-emitting layer of the lasers from 1.5 to 0.8 $\mu$m. "The theory of these devices is well understood," Olshansky says. "We can increase the photon density in the cavity by making the cavity as narrow as possible. This creates a strong interaction in the cavity between photons and electrons. There is a strong resonance in that interaction that determines the maximum modulation bandwidth that can be achieved."

In fact, the frequency of the diode emitters may be as great as 24 to 25 GHz, but can't be precisely measured yet because of the InGaAs photodetectors used in the test setup. Says Olshansky, "The frequency response we get with these new lasers is actually faster than 22 GHz, but we have to account for the rolloff of the photodetectors."

Olshansky says it will probably be three to four years before the first 10-GHz commercial fiber-optic systems appear. Meantime, GTE Labs is also working on a 120-channel video system that Olshansky hopes will be running by June at about 12 GHz, using 15-GHz laser emitters. *–Lawrence Curran*

**INDUSTRIAL**

## PHILIPS MOVES TO GRAB AUTOMATIC-TOLL MARKET

**KISTA, SWEDEN**

Big as it is, Philips can move with alacrity when it spots a new market opportunity. In the latest demonstration of its nimbleness, the Dutch electronics giant and its subsidiaries in Scandinavia are using their expertise in a number of technologies to roll into a relatively new hardware market that executives

are convinced is about to open wide: electronically controlled toll stations at bridges, tunnels, and highways.

In a pilot installation in Norway that Philips says is the first of its kind, cars pass through the toll point without stopping—in fact, they can go as fast as 35 mph and still be identified. Microwave equipment picks up the vehicle's code from an identification plate attached to the window. After appropriate data is fed to a computer, the car owner's bank account is debited automatically.

Philips described the system at the inauguration last month of a Philips technology center in Kista, a suburb of Stockholm. Managers at Philips Kistaindustrier AB, which developed the system, pointed up the potentials of electronic toll stations.

For one thing, stations with attendants on hand are labor- and hence cost-intensive. And at unattended exact-change setups or those with credit-card machines, drivers must either slow down or come to a stop. Where lanes are restricted to subscribers, freeloading is simple.

The electronic toll station eliminates all that. And there's a bonus, says Staffan Gunnarsson, development manager for identification systems at Philips Kistaindustrier: drivers need not renew their subscription or remember to pay on time.

The system would pay for itself in less than a year, says Gunnarsson. And the market potential is huge. In Europe, there are hundreds of manually run toll stations that the Philips system could replace. Elsewhere, there are big road, bridge, and tunnel projects underway that authorities want to help finance with tolls.

Several technologies converge in the new system: smart cards, integrated circuits, microwaves, and data processing.

**Cars can go as fast as 35 mph and still be identified**

It borrows heavily from Philips's Premid (programmable remote identification) equipment, which the company has installed at a number of European automakers to monitor and identify cars coming down the assembly line.

In toll collection, the local bank, for example, issues the driver an identification plate. A code is programmed in the plate's memory circuit to identify the car. Philips engineers won't reveal details, saying only that programming is done by microwave pulses that unlock the memory and put the identifying binary-coded words into it. The ID plate, about the size of a credit card, attaches to the car's side window.

When a car enters the toll station, an inductive sensor in the road bed registers its presence. At the same time, antennas at the toll point emit unmodulated microwaves at around 1 mW, low enough so as not to affect humans. The ID plate modulates the microwaves with the code it contains and reflects them to the antennas. The antenna-to-ID distance is up to 5 m.

The setup analyzes the reflections and the result is passed to the station's computer, a VMEbus machine based on a Motorola Inc. 68000 microprocessor and a Unix operating system. The computer compares the information it receives with stored data and sends its results to the bank, where the fee is charged to the driver's account.

If the system sees no ID plate at the time a car passes over the inductive sensor, the car is videotaped so that legal action may be initiated.

In the few weeks that it has been in operation, Philips says, the system in Norway has been 99.6% reliable, a figure that company managers think can still be improved. *–John Gosch*

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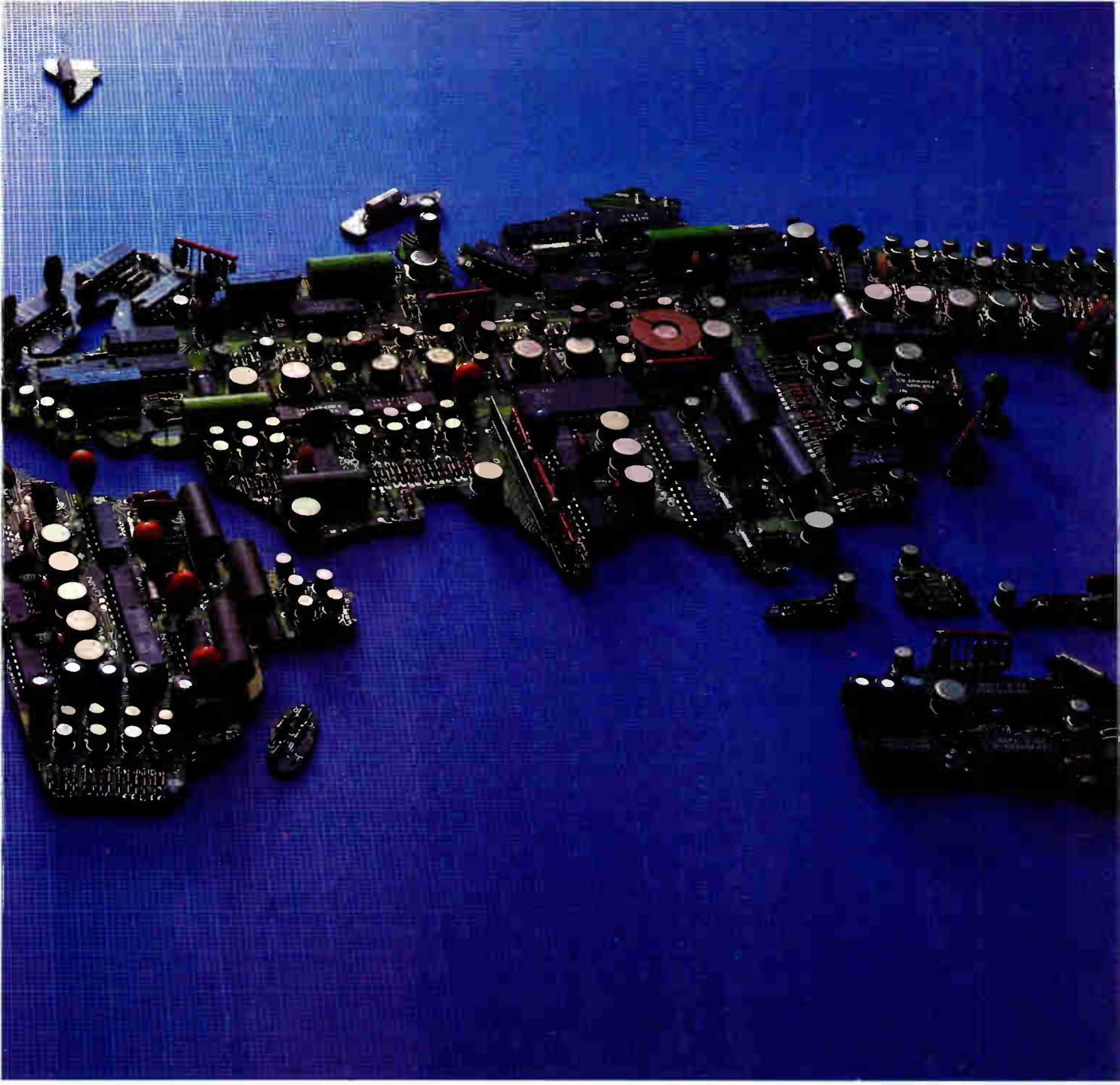

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# CIBA-GEIGY

The sun never sets on CIBA-GEIGY'S world of electronic chemicals

Circle 47 on reader service card

president to president and chief executive officer with the aim of refocusing the drifting electronics giant.

The reshuffling seems to have worked. "In the last three years, Jerry and Mark have been a model working pair," says one TI vice president. "The pairing has changed Mark."

There is also another side to Shepherd: the emotional man who is not afraid to display those emotions. Not only can he display anger in public, but he has shed tears at annual meetings. He also says his favorite job over the years was as general manager of the Semiconductor Components Division from 1954 to 1961. "I had a rule. I would get in at 8 o'clock every morning and I would not schedule anything until 10," he remembers. "I would just drop my briefcase and go around the labs and shops. I found out more about what was going on that way than all of the reporting mechanisms." And one thing Shepherd's friends and foes agree on is that he has remained accessible, never aloof.

Shepherd concedes that heart surgery in 1974 and a bout with a rare strain of pneumonia in 1985 drained away much of the stamina required for his post. But 1983 was the most difficult year of all. That was when TI's home-computer fiasco threatened to unravel the company.

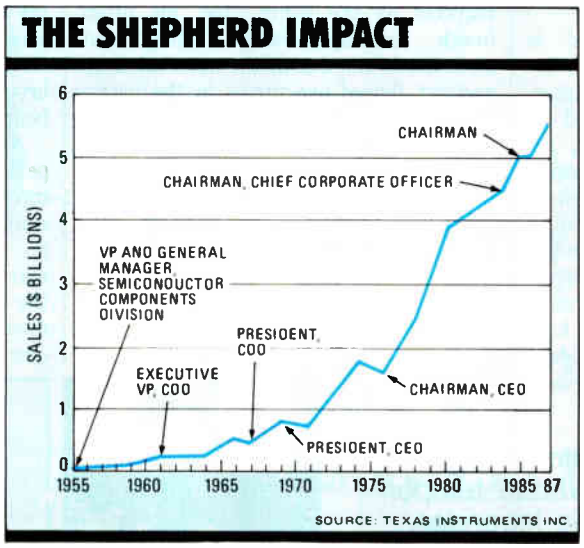
"I think I would be lying if I did not say 1983 took a lot out of me. It was the hardest year I have ever put in during my life," says Shepherd. He had originally planned to retire at about that time, he says, but "could not walk away from that." TI's home-computer line drained hundreds of millions of dollars from the company, and Shepherd remembers that workers were so frightened that he had to "tromp all over the world, talking to employees, telling them why we were not going to go bankrupt. That turned the tide."

Aside from that, Shepherd most regrets TI's slipping behind in CMOS technology in the 1970s. He says that's why TI has no host microprocessor. The CMOS lag also undermined the company's digital-watch thrust. And he says moving TI's MOS operation to Houston in the late 1960s was also a critical mistake, because it caused several key engineers to leave and start Mostek Corp.

But overall, the decades could not have been choreographed any better for Shepherd. The drive to the top actually began in 1948—fittingly, the year that the transistor was unveiled at Bell Laboratories. Shepherd took a job that year as project engineer in the Laboratory and Manufacturing Division of Geophysical Service Inc. in Dallas. The company created TI in 1951 as its new parent. In April 1952, TI sent a team that included Shepherd to a symposium Bell Labs had convened in Murray Hill, N. J., with an eye to licensing the transistor patents.

Also a member of the team was Patrick Haggerty, executive vice president. "Haggerty badgered them into giving us a ticket. They did not know what in the hell we wanted to do with it," recalls Shepherd. "We were there completely without portfolio. We did not know thing one about semiconductors. I did not even know if it was 'germanium' or 'geranium.' "

After 10 days of note-taking and sketching, the TI team returned to Dallas and quickly set about making germanium-grown junction devices. Diodes followed. While silicon vendors ignored the small company, TI started producing its own material and hit the market with the first silicon transistors. In 1958, TI announced the invention of the IC.




**Mark Shepherd** rose and so did TI's revenues as the small Dallas company became a $5 billion electronics giant.

During the late 1950s and early 1960s, Shepherd and TI rode the semiconductor wave. After heading the surging semiconductor operation, he was promoted to corporate executive vice president and chief operating officer. In 1963 he was elected to the board, and in 1967, he was named president (see figure).

"My promotions tended to coincide with the bad periods in the history of the company," Shepherd jokes, referring to economic slumps that had little impact on a maturing TI until the late 1960s. When TI threatened to become unwieldy, the company's managers moved to create a structure to keep innovation alive. "Institutionalizing that hunger is what you have to do, and that's a very difficult thing. By definition, when you institutionalize something you generate bureaucracy and it goes full circle. Bureaucracy is the enemy of innovation," he says.

Perhaps the biggest change during the Shepherd-Junkins era has been refocusing on profitability. In 1980, TI aimed to grow from $4 billion to $15 billion by the early 1990s. Some say that goal led TI to overcommit in the home computer market. While TI remains about $9 billion off the mark, Shepherd says he and Junkins have focused more on the bottom line. "But we still want to maintain growth. An organization dries up if you don't challenge it with growth," he adds.

All in all, Shepherd says he wouldn't change a thing: "I prefer exactly what happened. If I had to go write a scenario of a fun path, I've been through it." He particularly delights in knowing he has played a key role in building a $5 billion company, a major technology industry, and Dallas itself, where he grew up the son of a city policeman. "There are very few people in the world that have the privilege of having those three things happen," he says with a large grin.

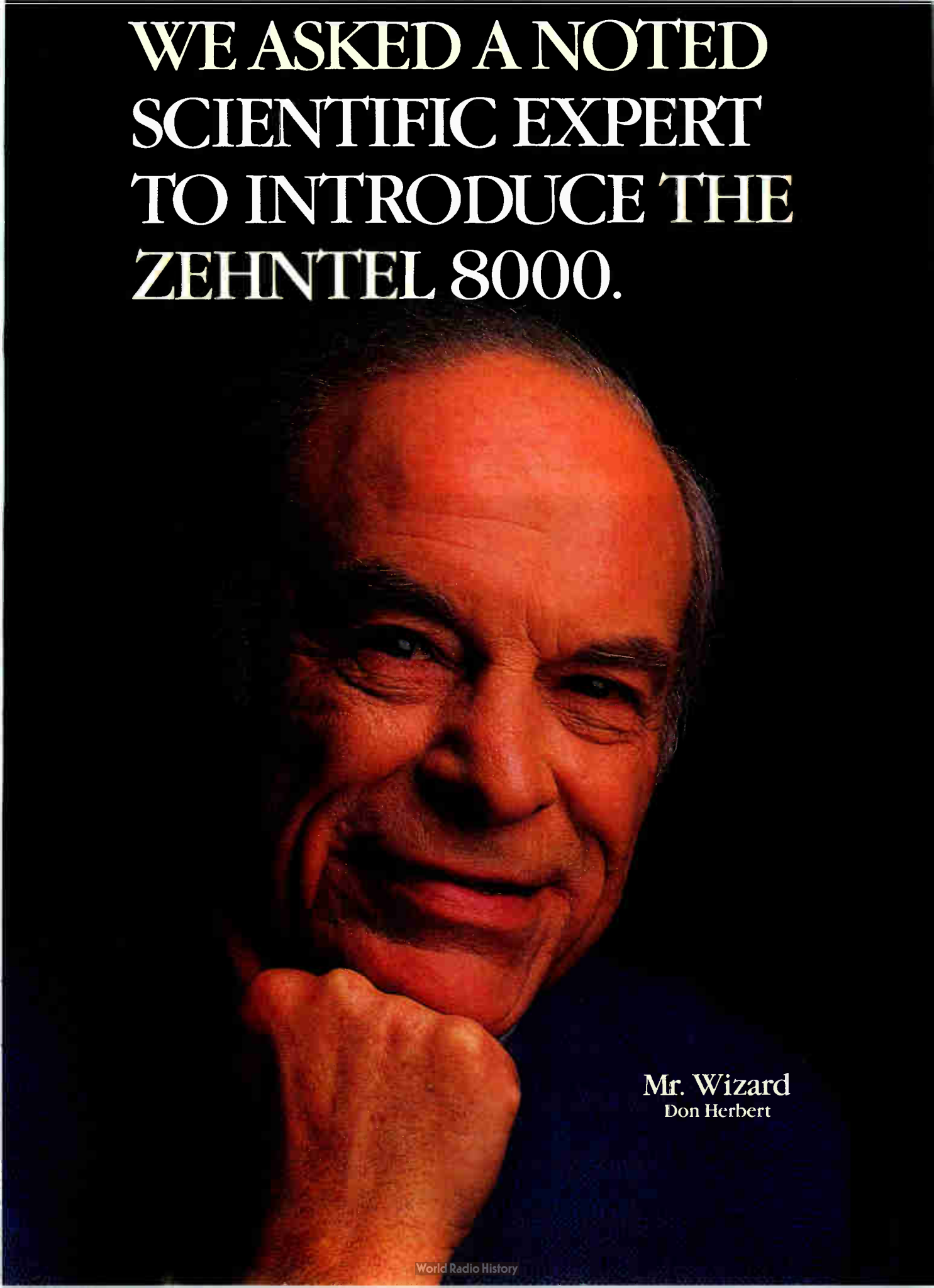
Shepherd will remain a board member. What he would like to see is TI establishing "a more meaningful stake in the end-equipment business," adding to its growing military-systems business, its fledgling industrial-automation efforts, and its modest commercial-computer group.

Looking ahead, Shepherd expects to see the global electronics market fragment into a handful of multination trading blocs as import barriers grow and become an increasing fact of business during the coming decade. "A lot of people howl in horror when I say that, but I really think it may happen," he says. He envisions a trade environment in which Europe and North America each form a bloc and Asia divides into two separate blocs, one centering on Japan and another on the Soviet Union and India. But "politics could change all of that tomorrow," he concedes.

He also believes that a silicon house must be in the commodity chip business to be successful, even though application-specific ICs are all the rage. "Today's special device is tomorrow's commodity," he says. "It has always been that way, and I don't think that will change. I think the imminent demise of the commodity business is overstated."

Shepherd's retirement is widely expected to have little bearing on the long-term direction of TI. Junkins had already taken over most of the day-to-day control during the past three years. But analysts and electronics executives agree that Shepherd's departure marks the end of an eventful era for both TI and the industry. *–J. Robert Lineback*

# WE ASKED A NOTED SCIENTIFIC EXPERT TO INTRODUCE THE ZEHNTEL 8000.



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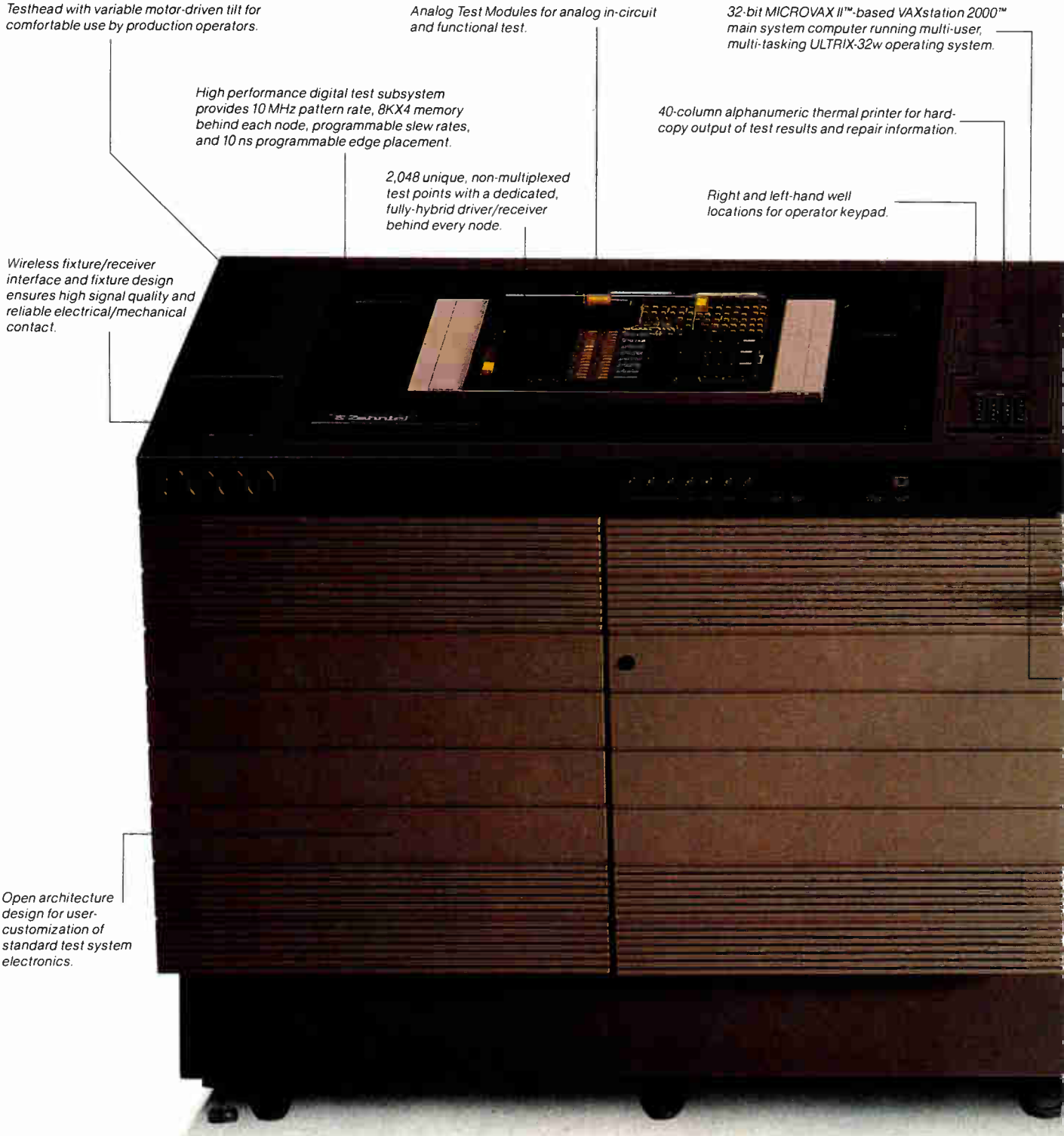


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# INTERNATIONAL NEWSLETTER

## SIEMENS WANTS TO LIMIT SGS-THOMSON'S ACCESS TO JESSI TECHNOLOGY . . .

Despite official pronouncements to the contrary, there does appear to be reluctance inside Siemens AG to share semiconductor technology with SGS-Thomson Microelectronics via the Joint European Submicron Silicon Initiative, or Jessi—a counterpart to the U. S. Sematech effort. Jessi's principal participants have been Siemens of Munich and Philips of the Netherlands [*Electronics,* Feb. 4, 1988, p. 51]; STM has had very little involvement in Jessi's planning phase, a Siemens executive points out. Now, however, the Italian-French chip combine is showing interest in joining the four-part Jessi project. The four areas are basic research, chip technology, equipment and materials, and circuit applications, and Siemens has no problem with bringing STM into three of them. But Siemens insiders have reservations about the technology part. They say that the German and Dutch companies have an edge on STM in many aspects of fine-line, high-density memory technology, an edge they have acquired through their cooperation in the Megaproject. They don't like the idea of sharing this know-how with STM. □

## . . . AND SGS-THOMSON WANTS JESSI'S EUREKA FUNDING CUT IF THAT HAPPENS

Philippe Geyres, corporate vice president for strategic planning at SGS-Thomson Microelectronics, is threatening to file a complaint with the European Communities, with the full backing of the French government, if Siemens and Philips don't allow STM to participate as a full partner in the Jessi project. "I don't think it will get to that point," says Geyres. Siemens and Philips cannot exclude STM and receive funding from Eureka, Europe's government-funded research program, Geyres feels. The Jessi participants hope that, through Eureka, European governments will pay 50% of the project's estimated $2 billion cost. He denies that his company is behind Siemens and Philips in technology for building high-density memories. □

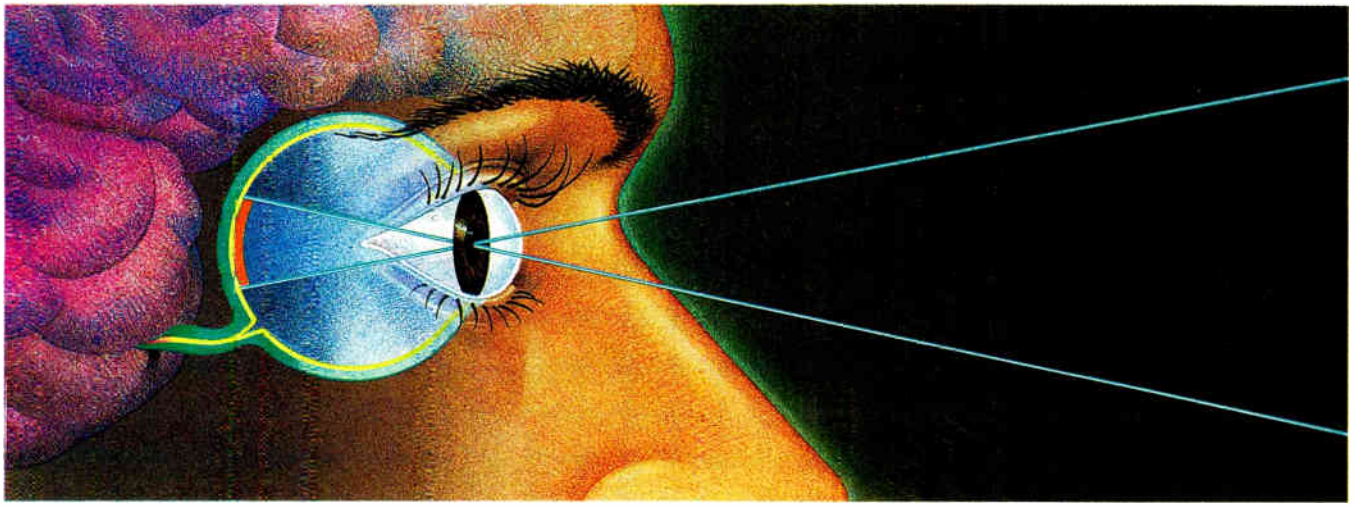
## JAPAN OPENS SUPERCONDUCTIVITY PROJECT TO FOREIGN PARTICIPATION

Japan's Ministry of International Trade and Industry has decided to open a key research consortium to foreign participation—smarting, perhaps, from criticism over keeping such projects closed to non-Japanese companies. MITI's superconductivity research consortium was set up in January with members limited to Japanese electrical-equipment, electronics, and wire manufacturers, as well as power-generating companies. Now the International Superconductivity Technology Center, Tokyo, has welcomed IBM Japan Ltd., Tokyo, as its first foreign-owned member. IBM Japan joined 46 Japanese firms as one of ISTEC's "general members"—giving it the right to attend ISTEC symposiums. IBM Japan is not a "special member"—the designation given the 44 companies that can do basic research at ISTEC's lab. □

## SIEMENS AND WESTINGHOUSE MAKE A FORMIDABLE TEAM

New products for industrial automation developed through the combined expertise of two world-class heavyweights in the field will hit the market in coming years if Siemens AG and Westinghouse Electric Corp. succeed in setting up joint ventures in the field. The two giants of electronics and electrical equipment have signed a letter of intent to cooperate in the areas of process and production automation and industrial energy distribution and control. One venture, aimed at automation-equipment production, is to be in the U. S. Others will build industrial-control components in the U. S. and make power switches based on Westinghouse technology in Europe. The moves will let Pittsburgh-based Westinghouse expand its equipment offerings in Europe and improve access to U. S. markets for Munich-based Siemens. □

# THE ANATOMY OF A FRAME TRANSFER SENSOR



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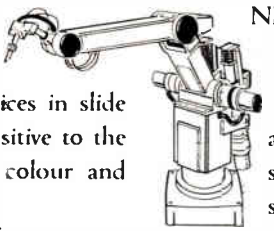

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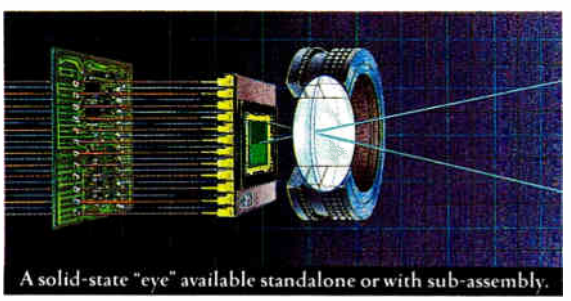

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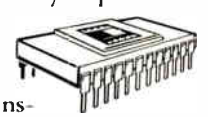

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# INTERNATIONAL WEEK

## JAPAN MOVES VCR CAPACITY OFFSHORE

Escalating trade friction between Japan and the European Community [*Electronics*, March 31, 1988, p. 52A] has prompted Matsushita Electric Industrial Co., Osaka, to move some of its manufacturing technology of VCR read/write heads to Grundig GmbH, Fürth, West Germany. Grundig has been manufacturing drums and supplying them to Matsushita Video Manufacturing GmbH, in Peine—which now assembles VCR mechanisms with Grundig drums and heads from Japan—since 1986. Matsushita also expects Grundig to buy stock in Matsushita Video Manufacturing.

## BOSCH AND MITSUBISHI TEAM ON HYUNDAI ICs

Robert Bosch GmbH, the West German automotive accessories producer, has entered a joint venture with Japan's Mitsubishi Electric Corp. and South Korean auto maker Hyundai to fabricate electronic fuel-injection systems for use in internal combustion engines. The three companies will start a production facility near Seoul in which Stuttgart-based Bosch and Tokyo-based Mitsubishi will each have a 25.5% share, with Hyundai taking the remaining 49%. Bosch and Mitsubishi will supply the technology for the injection systems.

## CELLULAR PHONES ARRIVE IN MANILA

Cellular telephone technology has established a beachhead in the Philippines with the inauguration of the Philippine Long Distance Telephone Co. service. Direct-dial service from mobile stations is available in 32 metropolitan areas as well as to 117 points around the world. The new system uses seven repeater stations located at strategic places to pick up and send signals to and from a mobile telephone unit via radio or mobile switching mode. Each base station has a varying transmission radius of about 20 km to ensure continuity of signals within a cell.

## ALCATEL CHOOSES A LAN PARTNER

French telecom giant Alcatel NV has chosen David Systems Inc. to be its local-area-networking partner. The Sunnyvale, Calif., company specializes in LAN products for banks, hospitals, and utilities. Alcatel will distribute the David Information Manager, an integrated voice and data LAN network that provides connectivity for Ethernet work stations, RS-232-C devices, and IBM Corp. 3270 display stations over ordinary telephone wiring. Alcatel will also incorporate David's technology into its current generation of PBXs.

## BRITAIN TO PROBE ITS MISSILE NEEDS

The British Ministry of Defence is looking into the need for a new medium-range surface-to-air missile and has contracted British Aerospace Ltd. to carry out a feasibility study on the best and most cost-effective way of meeting its requirements. The study will examine the potential for upgrading existing British systems as well as using foreign equipment alone or in combination with British developments.

## HITACHI WILL BUY U. S. ICs AND ASICs

Hitachi Ltd., Tokyo, has announced its intention to buy semiconductors from two major U. S. chip makers for its VCRs and air conditioners. Among the American chips destined for integration in Japanese consumer products are Intel Corp.'s 80C51 8-bit single-chip microcomputer and its 8096 16-bit microcomputer. Hitachi will also buy Texas Instruments Inc.'s standard-cell application-specific ICs manufactured by Texas Instruments Japan Ltd. The U. S. chips will be used in about 20% of Hitachi's air conditioners and 5% of its VCRs starting this summer—that's about 2% of all Hitachi semiconductor purchases in the fiscal year beginning April 1.

## HERE COMES A PC WITH DESIGN FLAIR

A personal computer for homes and small businesses that features a radical packaging concept is on the way from European computer giant Ing C. Olivetti SpA. Inside, the Olivetti PC1 will be compatible with IBM Corp. PCs, but its avant-garde look will be the work of Italian industrial artist Mario Bellini. Olivetti has already signed on Dixons Ltd., one of Britain's largest electronic retail chains, to market the product. Entry-level prices will start at £399, among the lowest in Britain, and will be aimed at toppling Amstrad Ltd. from its pole position in the market.

## ALPS PICKS IRELAND FOR PARTS PLANT

Cork, Ireland, will be the site of Tokyo-based Alps Electric Co.'s seventh overseas plant. It will be owned by Alps Electric (Ireland) Ltd., and will manufacture computer peripherals such as keyboard switches, graphics input equipment, and disk drives—including floppy and hard types. The new plant will use a manufacturing facility purchased from Apple Computer Inc.

## GERMANS AIM R&D AT SUPERCONDUCTORS

Superconductor research in West Germany will get a shot in the arm from a new team of three West German industrial giants: auto maker Daimler-Benz AG; chemicals producer Hoechst AG; and the electrical and electronics manufacturer Siemens AG. The trio will concentrate on ceramic high-temperature superconductors in a search for new materials with better superconducting properties than the well known yttrium-barium-copper combinations. They will also study the methods needed to ready such materials for practical applications.

## GERMAN LASER FIRM BUYS U. S. RIVAL

West Germany's Rofin Sinar Laser GmbH, a subsidiary of Siemens AG, has acquired the Industrial Laser Division of Spectra-Physics Inc., San Jose, Calif. The deal, still subject to approval by West Germany's Cartel Office, brings together two leading firms in the field of carbon-dioxide lasers for metal-finishing applications.

## COMMERCIAL PLANES TO GET LCD METERS

The first application of active-matrix liquid-crystal diodes in commercial cockpits is at hand. Thomson CSF and Boeing Corp. will jointly develop the flat-panel LCD instruments for Mach air-speed indicators, altimeters, radio distance magnetic indicators, and vertical speed indicators. The new equipment will be interchangeable with existing gear—it will have the same form, fit, and functions—but will be cheaper and more flexible.

## UK GETS FORECAST OF 9% GROWTH IN ICs

Semiconductor orders in the UK automotive, consumer, and data processing markets continue to improve, says the British Electronics Components Industry Federation. Despite weakness in the defense market—largely due to currency fluctuations—1988's overall growth is expected to be about 9%.

# NEW PLCC LEAD DIMENSIONAL INSPECTION SYSTEM

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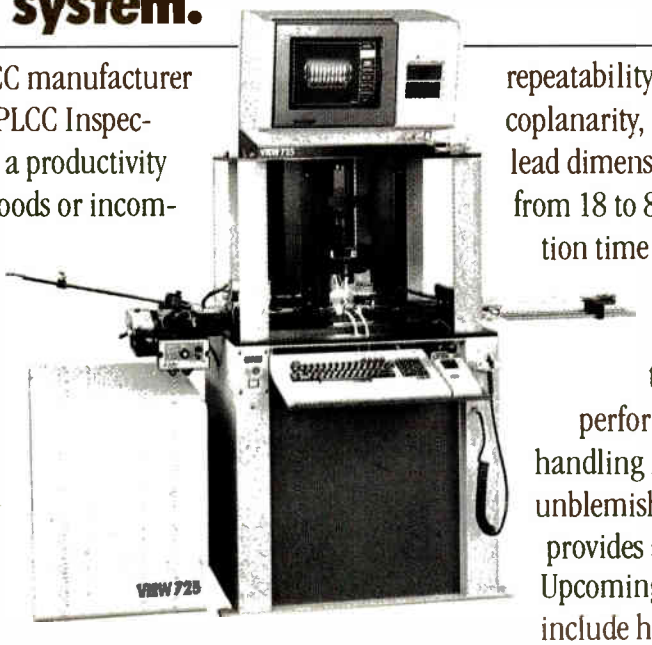


Whether you're a PLCC manufacturer or user, our new 725 PLCC Inspection System gives you a productivity bonus. For finished goods or incoming-inspection, or in-process inspection, the VIEW 725 is the only fully-automated, non-contact PLCC inspection system that gives you higher accuracies, faster inspection times, quicker change-overs and less problems than any method you're using today. We know since we have more than 25 systems delivering these same benefits in major semiconductor facilities around the world. Handling up to 2,000 PLCCs an hour—hour-after-hour with 100% repeatability. Inspecting seating plane coplanarity, tweezing coplanarity, and lead dimensions on PLCC devices with from 18 to 84 leads. Reducing inspection time and improving inspection accuracy.

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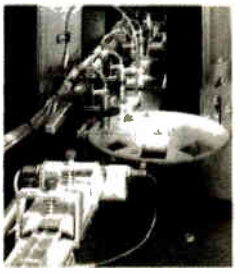

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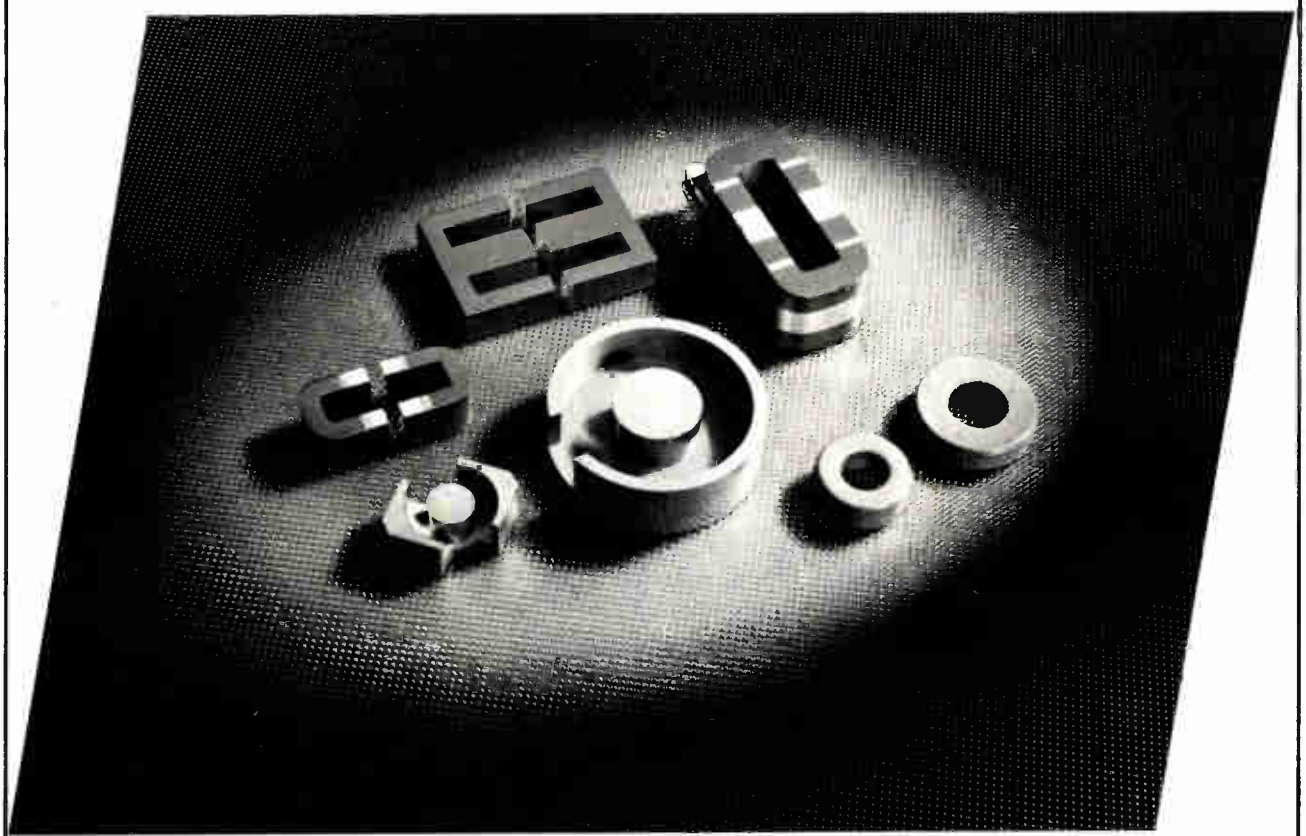

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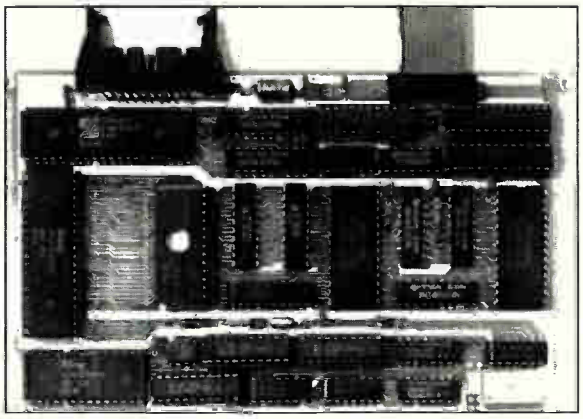
# INTERNATIONAL PRODUCTS

# PERDIX'S VERSATILE CONTROLLER HANDLES ANY FLAT-PANEL DISPLAY

## Proprietary code achieves compatibility with 15 terminals with minor software changes

By painstakingly developing 32 Kbytes of machine code for a proprietary operating system and then tightly coupling that software with its hardware, Perdix Components Ltd. is delivering a display controller board that offers designers of high-resolution flat-panel displays virtually complete programmability. Without redesign, the UK company's SPX-20 board can handle three distinct flat-panel technologies and emulate 15 commonly used terminal standards.



**The SPX-20** controller board includes ports for RS-232-C serial communications, plus printer and keyboard connections.

The board can drive ac- or dc-powered plasma panels, liquid-crystal displays, or electroluminescent panels, as well as conventional cathode-ray tubes. Minor software changes configure the board to emulate Digital Equipment Corp.'s VT220 and VT320 terminals. Also supported are protocols for computers manufactured by Data General, Hewlett-Packard, Honeywell, IBM, ICL, Systime, Tandberg, and Wyse Technology.

**ADAPTABLE.** Perdix, in Biggin Hill, Kent, set out to produce a single controller board that could be adapted by software to meet almost every foreseeable variation. As a result, each new project need not be designed from scratch.

"While virtually every project has unique features," says Nicholas Jarmany, manager of the board's design team, "they are, in general, permutations of a relatively limited number of parameters such as protocol requirements of industry-standard host computers, keyboard or control panel layouts, and character or graphic symbol sets.

"We use programmable logic arrays, electrically programmable read-only memory, and nonvolatile random-access memory coupled with Zilog Corp.'s Z-80 microprocessor to produce a design where the hardware and software are tightly coupled," Jarmany explains. "The variations we need then require only minimal additional coding—allowing us to turn around a new design in a few days."

Jarmany estimates that around 100 man-years of software design time were ground into the 32 Kbytes of machine code that form the proprietary operating system for the SPX-20, which Perdix calls Basic Code.

Hardware performance has been carefully specified to be able to accommodate future technologies. Depending on the type of panel used and the nature of the application, for example, the interface can handle a data bus with anywhere from one to eight bits—with four bits being the most common specification. The Z-80—although regarded by many designers as outmoded—provides more than adequate performance, Jarmany says.

Further flexibility stems from the proprietary keyboard interface, which Jarmany says can be adapted to present the user with any keyboard or control pad standard, irrespective of the terminal emulation in use. "We have supplied systems where the user has to work with a DEC host computer, but who wanted IBM layout keyboards," he says.

The SPX-20 comes complete with a 12-in. flat panel and power supplies for both board and panel. The standard display panel is a flicker-free 640-by-400-pixel ac plasma panel, manufactured by Perdix Components' sister company, Densitron International Ltd.

Display format is a standard 80 column by 25 lines, with characters formed from a matrix of 7 dots by 12 dots, each in an 8-by-16-dot cell. Display size can be controlled from software or from a keyboard or control pad to be dynamically variable between 16 and 40 lines deep. Other features of the panel include a 100° viewing angle, jump or smooth scrolling, and a split-screen capability. The controller board supports a 60-Hz, noninterlaced refresh rate.

The board and communications interface are attached to the back of the display panel to make a compact unit measuring 293-by-187-by-25-mm thick.

Managing director Rodney Tietjen says that liquid-crystal display or electroluminescent panels are available as options, and the unit can be also be supplied packaged or as a complete terminal with keyboard.

The controller board includes ports for RS-232-C serial communications, printer and keyboard connections. On-board memory includes 32 Kbytes dedicated to the display and 8 Kbytes of character-generator read-write RAM that allows character fonts to be loaded from the host computer.

Jarmany describes the board as a universal controller. "The design evolved from our experience as flat-panel suppliers," he says. "Apart from the Japanese manufacturers of portable computers, very few designers are using flat panels in sufficient volumes to justify their developing complex drive circuits tailored to their specific requirements. So we offered a design service for them."

**USES.** Applications range from displays for air traffic controllers' desks through machine-tool control panels to travel agency and financial terminals and automated teller machines.

Serial port performance is specified at up to 3.84 Kbits/s for communications with host computers and peripherals and the controller's video bandwidth is the equivalent of 35 MHz.

A significant by-product of the design is that since all data is sent to the display panel in parallel form, terminals using the SPX-20 are not susceptible to bugging. Tietjen says that nearly all

cathode-ray-tube terminals radiate signals that can be intercepted and re-constituted on a remote monitor.

Future development will concentrate on reducing the chip count on the board with the dual aim of reducing unit cost and incorporating more functionality. "We will shrink the design to six chips," says Jarmany. He indicates that the next step may be to add circuits with more data-processing capability—perhaps to build a complete personal computer system onto the back of a display panel.

The price of the SPX-20 varies according to the type of panel supplied. Electroluminescent panels are the most expensive, says Tietjen, and LCDs the least. A controller board programmed to customer's specifications for a plasma panel—plus the panel and power supplies—costs around £600 in volume quantities. The unit is available now. Quantities supplied range from 30 to 1,000 units. – *Peter Fletcher*

Perdix Components Ltd., Unit 4, Airport Trading Estate, Biggin Hill, Westerham, Kent, TN16 38W, UK.
Phone 44 0959 71011 [Circle 500]

Densitron Corp., Kyowa Nanabankan 5F, 1-11-5, Omori-Kita Ota-ku, Tokyo, Japan 143.
Phone 81-3-767-9701 [Circle 501]

## IMAGE SCANNER OFFERS 40% WIDER FIELD

The UDH07 image-scanning device from Alps Electric Co. can handle paper in sizes ranging from that of a postcard up to 105-mm wide—40% greater maximum width than its standard scanner.

The scanning system is driven by charge-coupled-device technology that

delivers an output pixel density of 8 dots/mm. The scanner can output data in black, white, and three half-tones.

An automatic density adjustment mechanism integrated into the UDH07 lets it read papers of different densities. A read-through window is provided to calibrate the device for paper density.

Unlike many scanners, the UDH07 can read red lettering and graphics because it uses a yellow-green light-emitting diode as its light source. A feeder is available as an optional attachment.

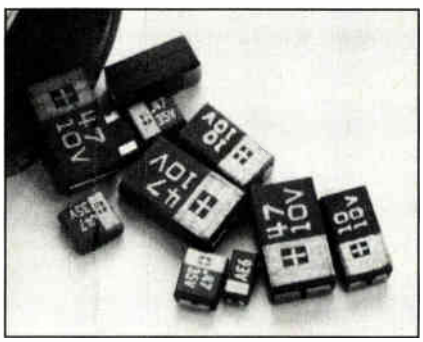
The UDH07 is available now. Price depends on importing country.

Alps Electric Co. Ltd., 1-7 Yukigaya-Otsukacho, Ota-ku, Tokyo 145, Japan.
Phone 81-3-726-1211 [Circle 701]

## CAPACITORS WITHSTAND 260°C SOLDERING

A new series of tantalum chip capacitors from Siemens AG can handle temperatures up to 260°C for 10 seconds during printed-circuit-board assembly, which suits them for flow, reflow, and vapor-phase surface-mounting technologies.

Encased in ceramic, the capacitors in



the Type B 45196 series range for 1 to 1,000 pf and are specified for power supplies of from 6.3 to 35 V. Depending on capacitance and voltage specifications, the tantalum chips come in various sizes.

The devices come mounted on tape for easy automated handling. They are available on 12-mm-wide tapes that have 2,000 capacitors per roll and on 8-mm-wide tapes that have 750 capacitors per roll.

Shock resistance of the devices is 981 m/s². The operating temperature range is −55° to +125° C.

The devices are available now. Price depends on importing country.

Siemens AG, P. O. Box 103, D-8000, Munich 2, West Germany.
Phone 49-89-2341 [Circle 704]

## NINE-CHIP SET CLONES IBM'S PS/2 MODEL 30

Acer Ltd.'s PC86 nine-chip set provides all the system control, input/output support, peripheral interface, floppy-disk-drive control, and graphics functions required to build a personal computer fully compatible with IBM Corp.'s Personal System/2 model 30.

Based on application-specific integrated circuit designs and fabricated in 1.5-μm CMOS, the chip set also includes a high-performance 256-by-18-color palette chip that provides compatibility with IBM's MCGA and VGA graphics standards. MCGA graphics offer 256 colors from 256,000 combinations.

The M1201 system controller can handle 10-MHz clock speeds for Intel Corp.'s 8085 and NEC Corp.'s V30 microprocessors.

The complete set, including the M2105 Mouse controller IC, carries an export price of $77 when purchased in 1,000-unit quantites. Samples and a demonstration board will be available in May, with production quantities ready in July.

Acer Ltd., Grove House, 628 London Rd., Slough, Berkshire SL3 8QH, UK.
Phone 44-753-686-008 [Circle 702]

## LIGHT SENSOR BOASTS HIGH RESOLUTION

The TH X31150 charge-coupled-device image sensor from Thomson-CFS Electron Tube Division offers a full-frame, 512-by-512-pixel active surface and is sensitive to light in the 400- to 1,100-nm spectrum.

Pixel size is 19 μm by 19 μm, which yields an image area of 9.7 mm². The TH X31150 has two readout registers, one at the top and one at the bottom of the image zone, each with bidirectional readout capability. Each of the four outputs can read out either half the image field or the full field.

The readout registers have two selectable stages so that they can accommodate on-chip amplifiers for either low-frequency or high-frequency bandwidths.

The TH X31150 is available now. Price depends on importing country.

Thomson-CFS Electron Tube Div., 29, rue Vauthier, B. P. 305, 92102 Boulogne-Billancourt Cedex, France.
Phone 33-1-4604-8175 [Circle 703]

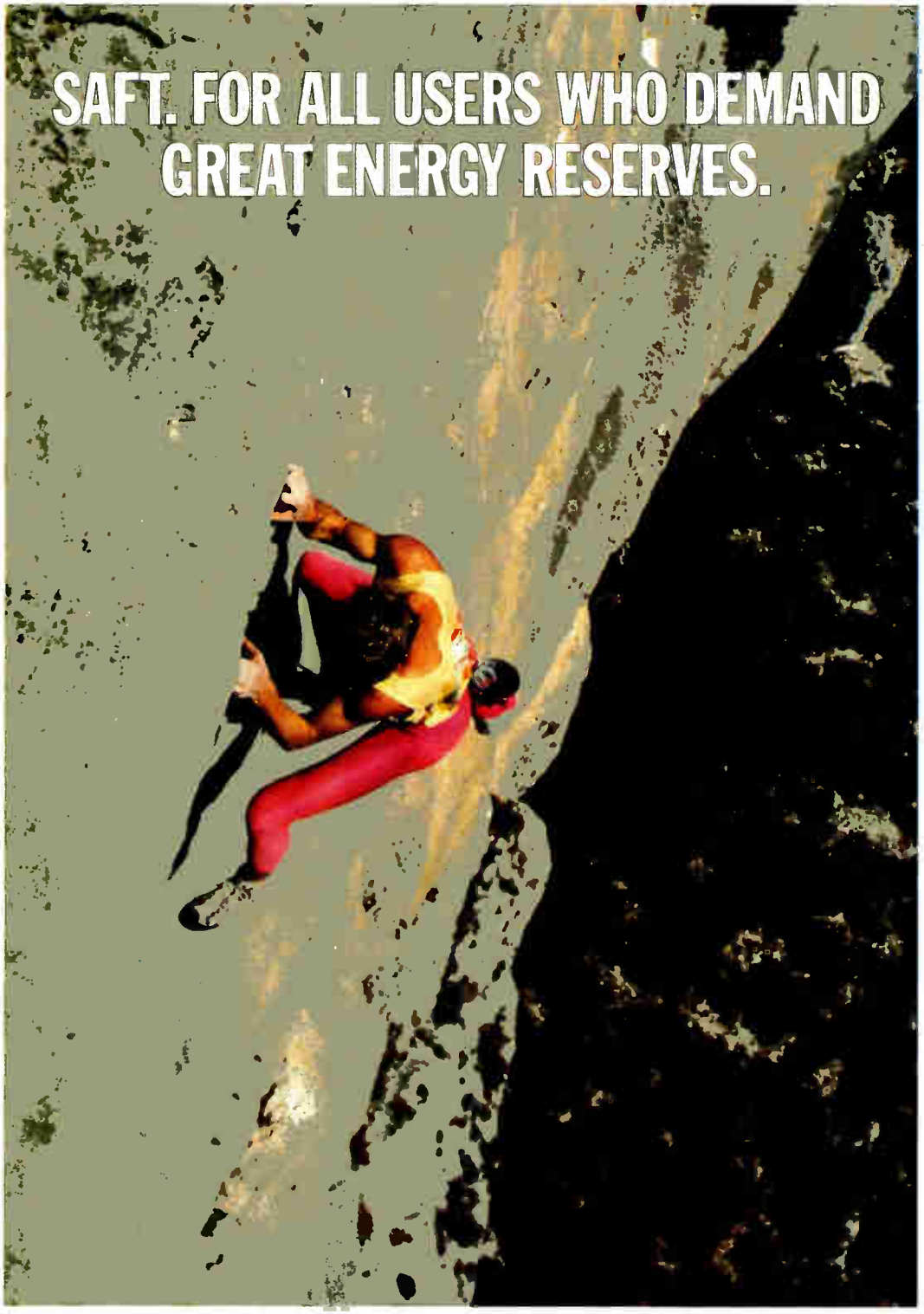
## IMAGING CARDS OFFER 6-BIT RESOLUTION

The IAS20 and IAS25 plug-in image analysis boards from Loughborough Sound Images Ltd. capture TV signals with 6-bit/pixel resolution to deliver 64-shade gray-scale images. An additional two bits handle the displayed binary and text overlay planes.

Image resolution is 256 by 256 pixels for the IAS20 and 512 by 512 pixels for the IAS25. The boards are based on Texas Instruments Inc.'s TMS 32010 digital signal processing chip; they plug into IBM Corp. Personal Computers and compatibles. They come with software packages for image processing.

The Genias package is for users without programming experience. It includes functions for image enhancement, complex gray-shade operations such as convolutions, and edge detection.

A comprehensive imaging system library called Genial is available for Pascal programmers. It allows the functions in Genias to be built into applica-

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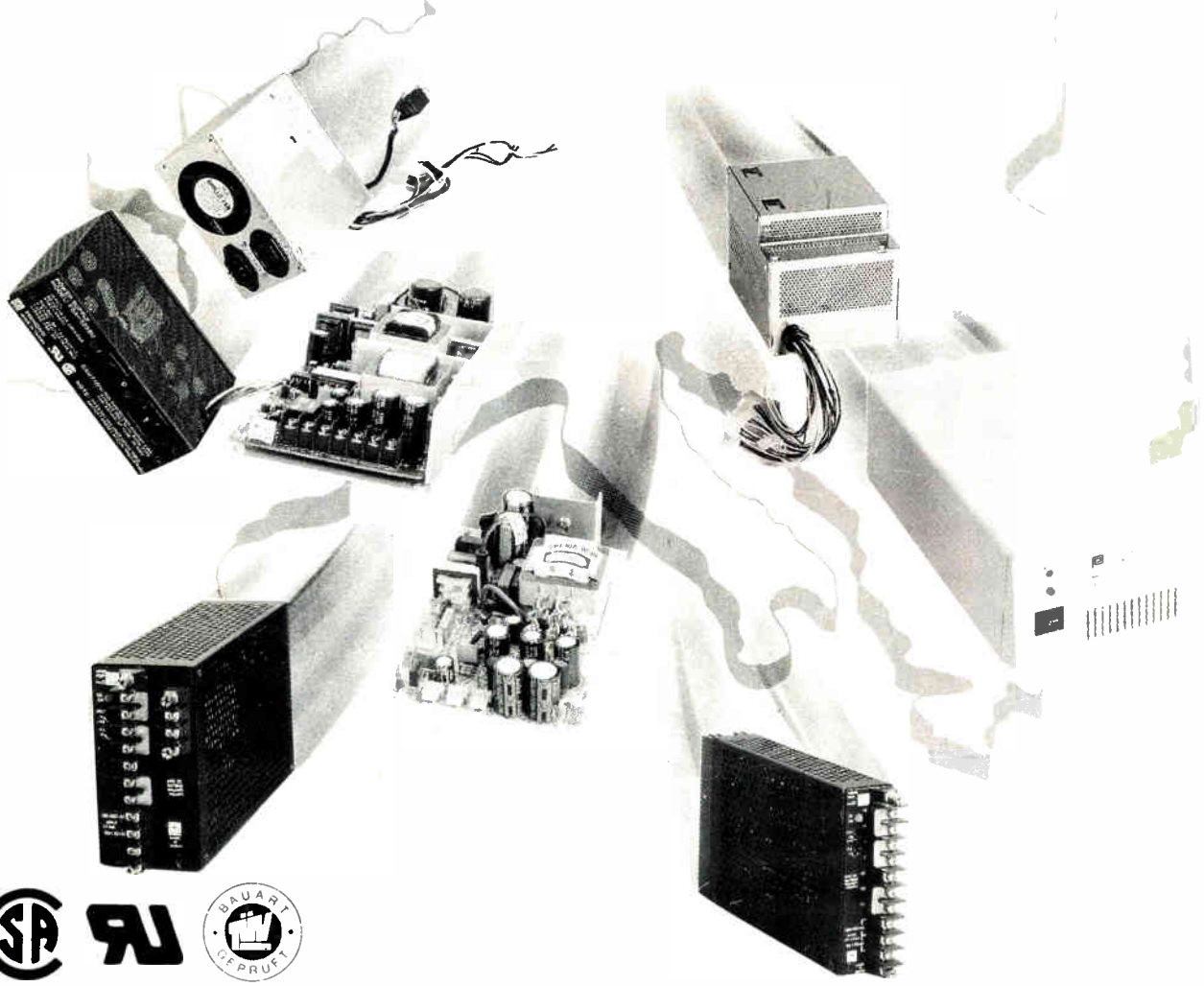

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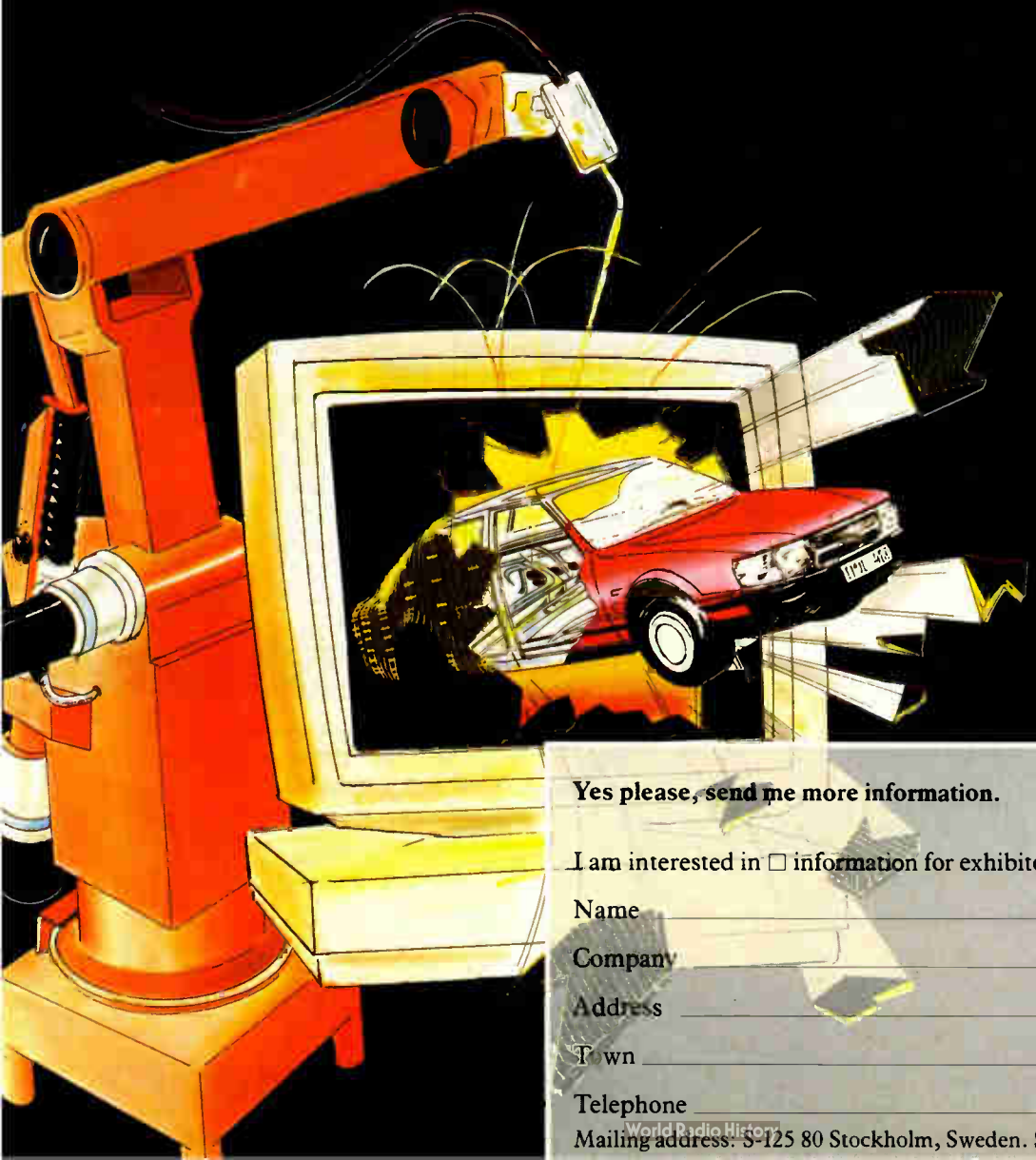
# Welcome to CIM-88

The Nordic CAD/CAM days have expanded into CIM 88. A new fair! Scandinavia is one of the leading markets in the world for developments in CIM – Computer Integrated Manufacturing. For a few days in April, 1988, CIM 88 will form Scandinavia's first and most concentrated focal point for all that's new in CIM. Naturally you will want to take part – send for more information.

## April, 25-28 1988



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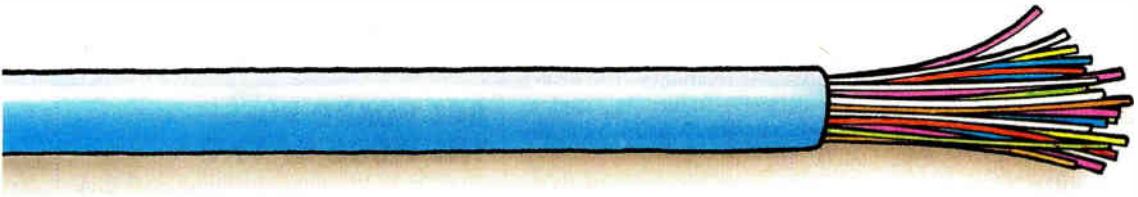
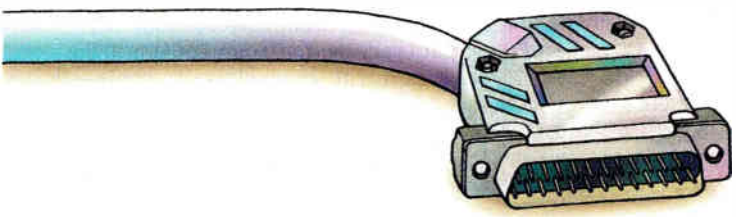
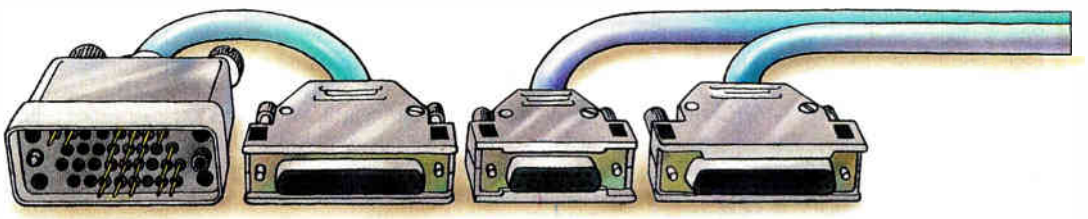


# digital data or analog information

# down the wire, whether you use just one



# type of interface or lots of different ones:



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tion-specific programs written by the user.

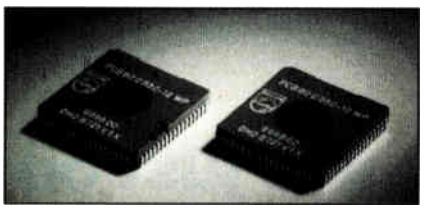
Both systems target value-added reseller applications such as systems for medical screening, remote sensing, and industrial inspection. Available now, the IAS20 costs £2,495 and the IAS25 £5,995. Price includes either Genias or Genial.

Loughborough Sound Images Ltd., The Technology Center, Epinal Way, Loughborough, Leistershire LE11 0QE, UK.
Phone 44-509-231-843 [Circle 705]

## MICROCONTROLLER IS EASY TO PROGRAM

The PCB83C552 microcontroller from Philips Components Division targets automotive applications with a modular design that allows for easy programming to control different car functions, including injection systems, gear-box operation, and instrumentation.

An on-chip timer is used to control the operation of valves, stabilize engine idle, or recirculate exhaust gases. An on-chip 10-bit analog-to-digital converter helps



track variables such as engine coolant flow, gasoline flow, and battery voltage.

The 68-pin PCB83C552 boasts power dissipation of 125 mW, due largely to software-selectable idle and power-down modes that cut current to 10 mA and 50 μA. Its standard temperature range is 0° to 70°C.

The chips are available now in plastic leaded chip carrier packages. Pricing varies depending on importing country, but ranges from DM 24 to DM 25 for 100-piece purchases.

Philips Components Division, P. O. Box 523, 5600 AM, Eindhoven, the Netherlands.
Phone 31-40-757005 [Circle 706]

## SOLID-STATE MEMORY EMULATES HARD DISK

Vermont Research Ltd.'s model 4256 solid-state memory system packs from 2 to 129 Mbytes of storage into a 7-in.-high chassis. Unlike many competing solid-state memory systems, it offers full emulation of traditional disk storage devices.

Controllers are available emulating disk-drive interfaces for computers from Digital Equipment Corp., Data General Corp., and General Automation Ltd. Other interfaces supported include the Small Computer Systems Interface,

Storage Module Drive, and Diablo.

In addition to the order-of-magnitude advantage in access speed afforded by solid-state storage, the absence of moving parts increases reliability. The 4256's mean time between failure is rated at 30,000 hours. On-site repairs typically take just 30 minutes.

Data backup security is available through an optional ¼-in. tape cartridge and battery power pack, so that data is automatically copied if the main power source fails.

Available now, the basic 4256 with 2 Mbytes of memory costs £5,000 in volume purchases.

Vermont Research Ltd., Cleeve Rd., Leatherhead, Surrey KT22 7NB, UK.
Phone 44-372-376-221 [Circle 708]

## UNIT MEASURES 6-MICRON COATINGS ON PC BOARDS

The Fischerscope X-Ray 1010-PCB from Helmut Fischer GmbH uses x-ray fluorescence methods to measure the thickness of coatings on printed-circuit boards. It determines thicknesses down to 6 μm for coatings made of gold and down to 40 μm for coatings made of silver or tin.

At the heart of the system is an open-top table that allows boards to be positioned manually with the aid of a color monitor. A printer logs all readings and provides a test certificate.

The instrument's working-surface area is 600 by 630 mm, and is accessible from all sides. Boards up to 90-cm wide can slide along embedded Teflon ball bearings for positioning in the cross-hairs projected on the monitor.

The Fischerscope X-Ray 1010-PCB can be delivered four to eight weeks after ordering. Its price is around 60,000 DM, depending on configuration.

Helmut Fischer GmbH, P. O. Box 4, D-7032 Sindelfingen 6, West Germany.
Phone 49-7031-3030 [Circle 707]

## CONNECTORS COMBINE SIGNAL, POWER PINS

The Han K series of connectors from Harting Elektronik GmbH have their signal and power contacts built into a single unit.

Eight power contracts handle voltages up to 380 V ac or 450 V dc, and 24 signal contacts handle up to 250 V ac or 300 V dc.

All 32 contacts may be of the snap-in removable type and can be terminated with standard hand-crimping tools or by automatic crimping machines.

The signal contacts may be used for fiber-optic cables. Aimed at applications in industrial electronics, machine tools, robotics, and process control, the Han K connectors are available from stock. Price will be given on request.

Harting Elektronik GmbH, P. O. Box 1140, D-4992 Espelkamp, West Germany.
Phone 49-5772-47244 [Circle 709]

## ADC BOARD DOES THE WORK OF TWO

The Trian 12 analog-to-digital and digital-to-analog conversion boards from the Essex Electronic Centre can replace two or more conventional conversion boards in many applications, thanks to their modular design.

Ten versions are available. Each offers a different combination of functions, including up to 16 multiplexed, single-ended ADC channels or up to 8 differential channnels. Also, an instrumentation amplifier based on Analog Devices Inc.'s 10-μs AD574A is available, as is a sample-and-hold function with 7-μs acquisition time.

Four DAC channels can be provided—they are implemented by Analog Devices' AD5737, which features a 1.5 μs settling time.

The boards are available now with prices ranging from £200 for four DAC output channels (the Trian 12-04) to £395 for a card with 16 single ADC inputs—each with the sample-and-hold feature—plus four ADC channels (the Trian 12-16SH-4).

Essex Electronics Centre, University of Essex, Colchester CO4 3SQ, UK.
Phone 44-206-872-922 [Circle 710]

## 2-CHANNEL SCOPE ADDS, INVERTS SIGNALS

Philips has enhanced its popular 15-MHz, two-channel PM3206 oscilloscope so that signals on channels A and B can be added and those on channnel B inverted. Both channels can be grounded.

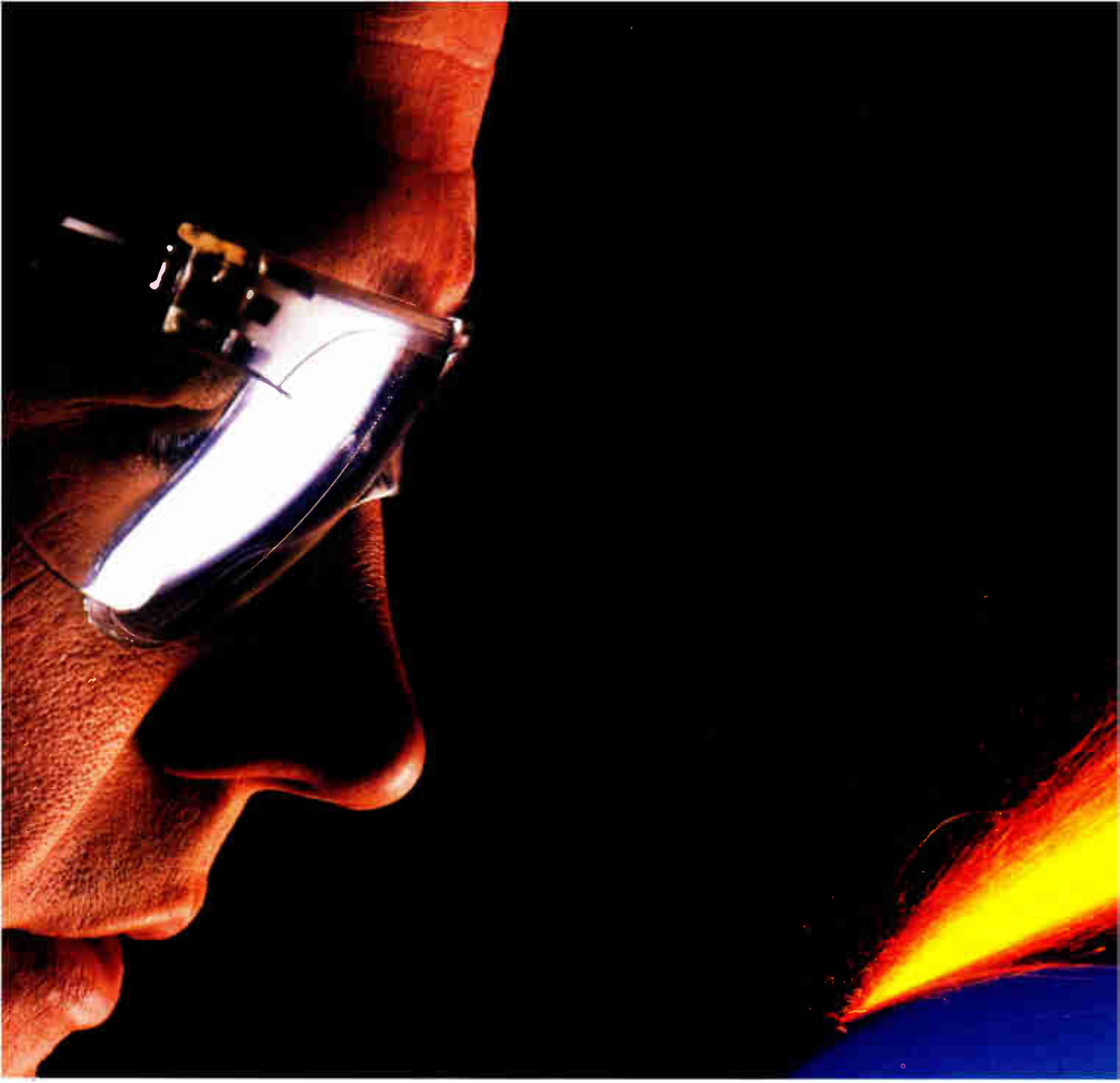
The instrument boasts a sensitivity of 5 mV/cm peak-peak triggering, TV triggering, and a bright display that make the PM3206 suitable as an all-purpose instrument for use in the field and in the laboratory.

Despite its low price—about 1,000 DM—the oscilloscope fulfills all professional specifications and international standards regarding safety, shock, and nonflammability.

The PM3206 is available now.

Philips GmbH, P. O. Box 310320, D-3500 Kassel, West Germany.
Phone 49-561-5010 [Circle 711]

# Gould has features you won't find at the ordinary ASIC house.



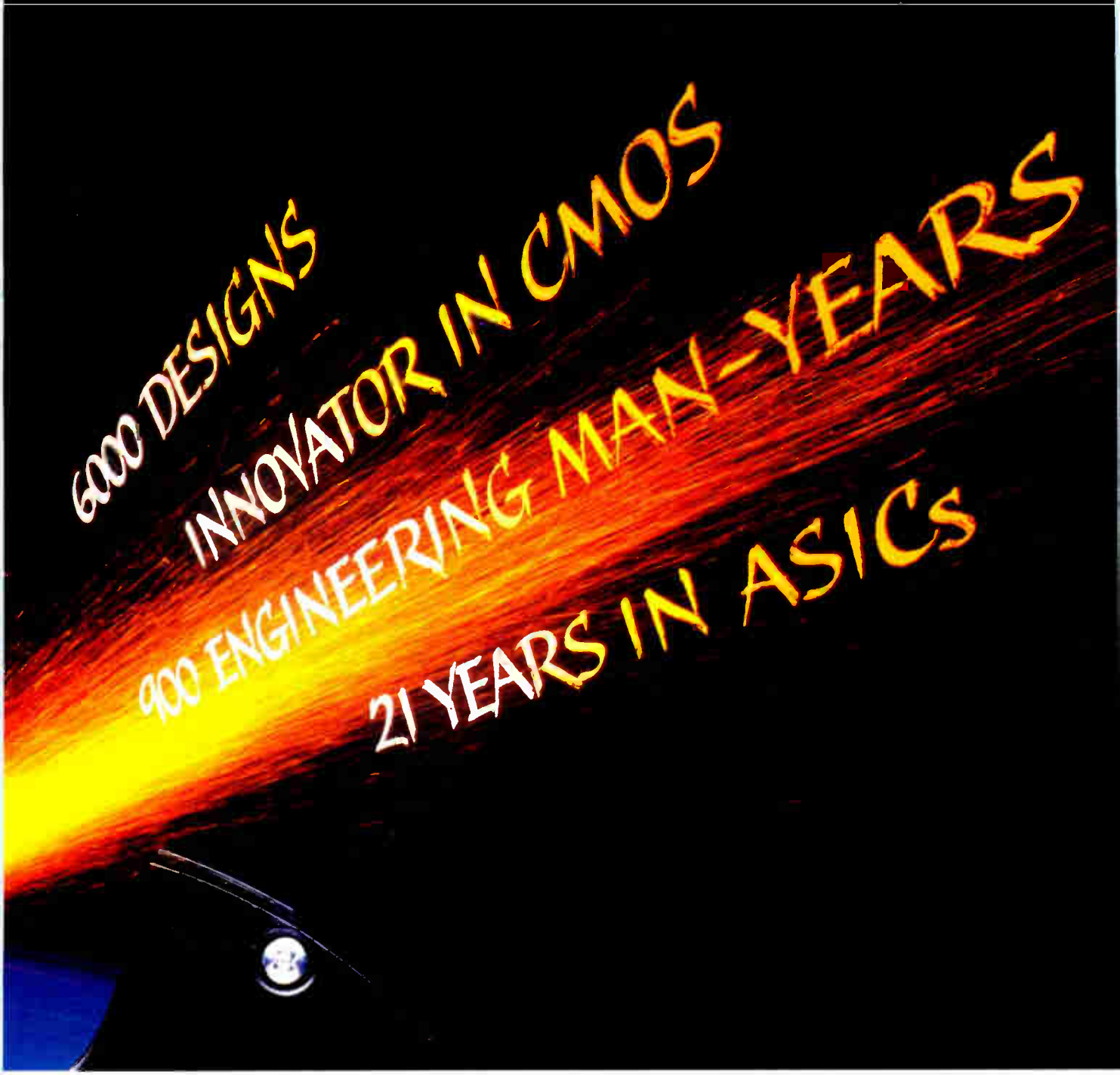
# A nose to the grindstone.

What do twenty-one years as an ASIC vendor do for your customers? A lot.

Two decades give you the time you need to develop and manufacture over 6000 successful designs. The time you need to accumulate 900 man-years of engineering experience. The time you need to learn things not found in the textbooks.

That's the kind of experience Gould Semiconductors can put to work for you on every circuit you do.

Gould recognized early how valuable the combination of CMOS processes and CAD/CAE technology would be for our customers. We have been an innovator in both of these areas.




We've also had time to fully develop application-specific IC techniques that still frustrate other vendors. For instance, Gould is an acknowledged industry leader in analog/digital circuit combinations. Many ASIC producers can't even offer them.

The most important advantage to you, though, is that Gould has probably produced a design similar to yours already. We know the problems to look for and how to avoid them. In many cases, we can recommend easily incorporated features that add value to your system.

That's what twenty-one years of hard work can do for you.

**Manufacturer of Gould AMI Semiconductors.**

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# An ear for your problems.

All ASIC customers want essentially the same things: better system performance, lower system cost, quick development and production cycles. But every ASIC project has a different set of priorities.

Your only guarantee of success is the vendor's sensitivity to your individual needs. For two decades, Gould has listened and responded with strategies to provide the best system solution. The ASIC Continuum is one such strategy.

The ASIC Continuum provides a design solution effective for any application. There are low-cost $E^2$PLDs for instant prototypes and small volume production applications. Also gate arrays for fast prototyping


and cost-effectiveness over a broad range of volumes.

More advanced implementations get standard cell or cell-based custom circuits. These are ideal for analog/digital combinations, high-density systems and other circuits requiring special performance characteristics.

We are also meeting your needs with expert-based design aids. Extensive cell and macro families for PCs and workstations. A full-service design group. And more comprehensive programs to give you the best ASIC solution.

**Manufacturer of Gould AMI Semiconductors.**

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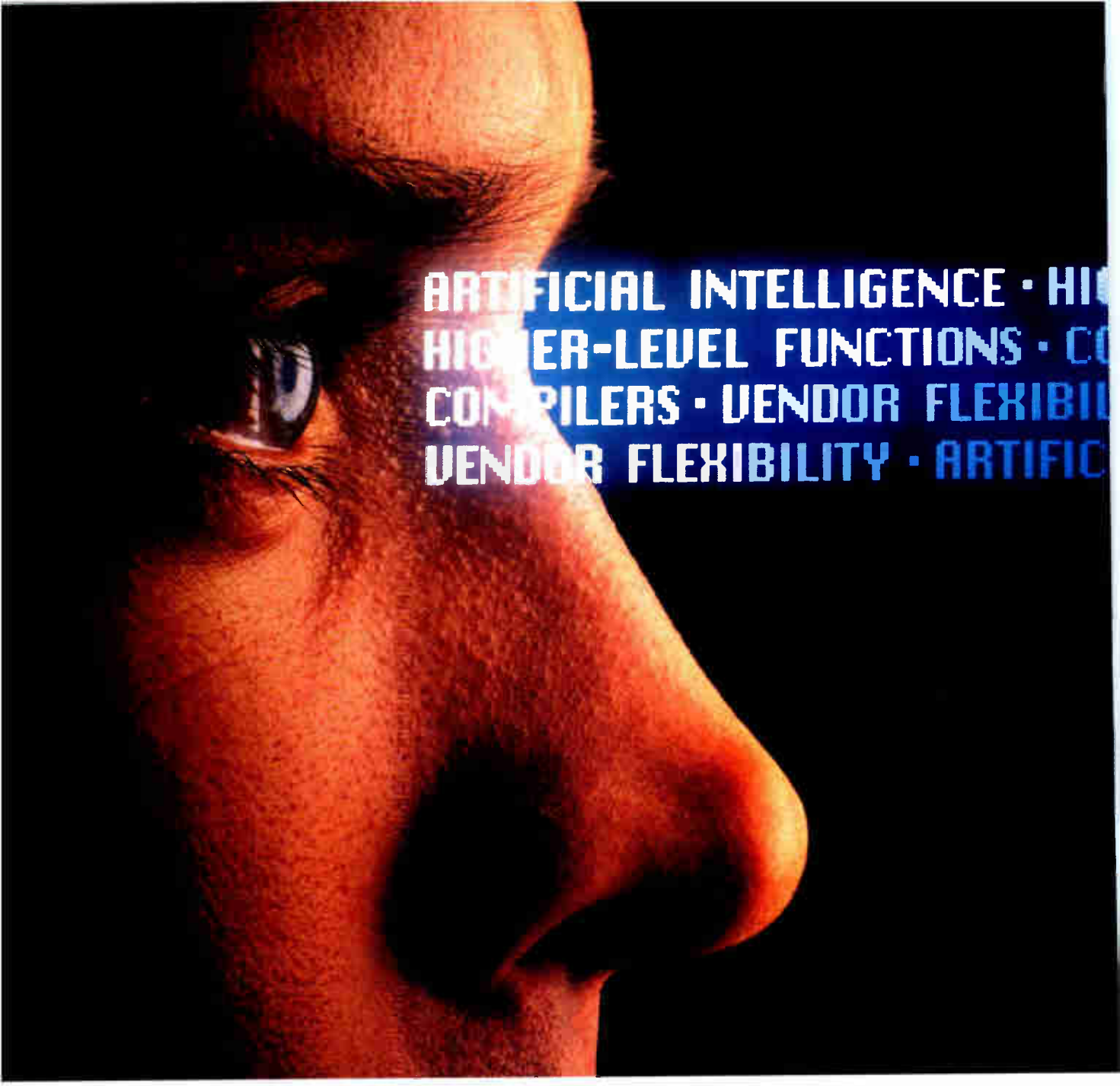
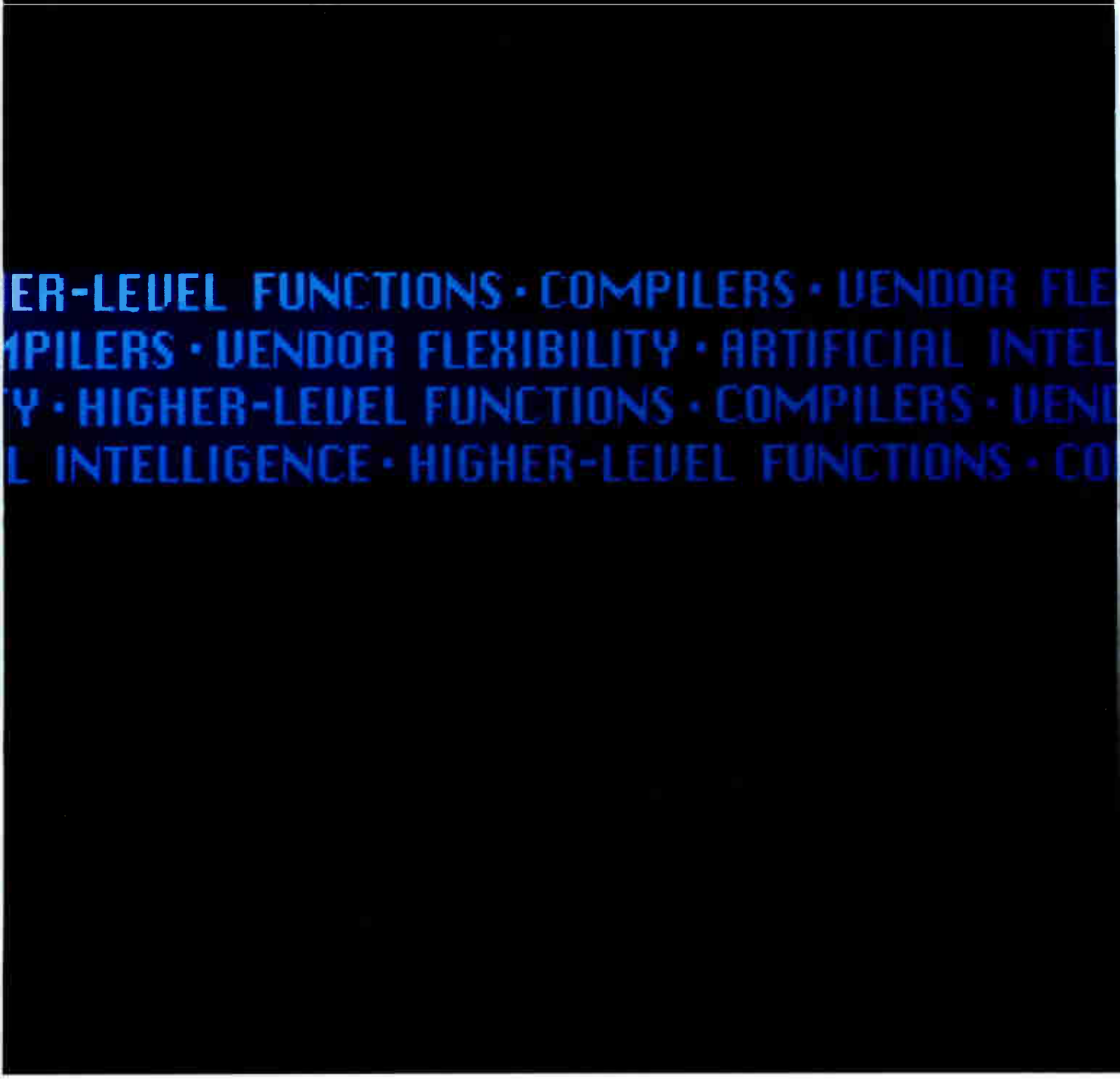



# An eye on the future.

The pressure on system designers will continue to be intense. Gould has responded by cutting development spans, increasing functions and performance. And now we're using artificial intelligence (AI) to go even further.

Already Gould Expert Systems™ tools are adding value for system designers. AI-based generators and compilers create cells in days instead of weeks. Standard cells. ROMs. RAMs. Even analog cells, like op amps and filters. And these tools are process independent, making our libraries some of the easiest to tailor to your needs.

Going a step further, megacell compilers create large custom functions (bit-slice

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# STRANGE BEDFELLOWS.

*The primary aim of the LFAST project was to develop a linear bipolar process that could match the density of linear CMOS but not sacrifice bipolar's performance advantages.*

## Fairchild Gets Linear Circuits Without Sacrificing Densities.

"A new process from Fairchild Semiconductor Corp. seems to resolve what has always appeared to be an irreconcilable problem for chip-designers: how to get high-performance analog and high-density digital functions to reside on the same chip. The new process, called LFAST, is a 5-$\mu$m linear bipolar process from Fairchild's Linear Division in Mountain View, Calif.

Before LFAST, any process capable of producing linear circuits with enough dynamic range to be useful in practical analog applications had to sacrifice the density required for large-scale integration. The process achieves a tenfold increase in density over existing linear bipolar approaches without sacrificing speed..."

*Excerpted from an exclusive article in the April 16, 1987 issue.*

**Electronics**

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INSIDE TECHNOLOGY

# FROM SYSTEMS TO STANDARDS, THE PACE QUICKENS IN NETWORKING

**When the networking ideal—any computer working with any other computer—is reached, it will revolutionize the way people work: employees split among offices on two continents will be able to collaborate as if they were all in the same room**

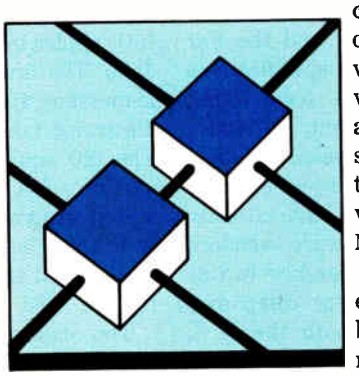
by Stan Runyon

The ultimate dream in data communication is to make any computer work seamlessly with any other computer anywhere in the world. Networking, however, is still light-years away from that goal. A hodgepodge of incompatible machines, operating systems, applications, and utility software are haphazardly connected by a maze of different physical links and protocols.

But things are getting better fast. On every front, from systems to standards and software, the development pace is quickening. The driving force is world competition. Progress is being made on several fronts: mixing voice, data, and other services; speeding up the flow of data; making the information more secure; hooking any computer to any computer, and any network to any network.

When those ambitious goals are reached, perhaps within the next decade, it will revolutionize the way people will work: A project leader and his 20-person design team, split between offices in, for example, Sunnyvale, Calif., and London, will be able to sit down at individual work stations and together design a million-transistor central processing unit, each viewing the other person's moves. While at their stations, the designers can call on a supercomputer in New York to simulate the chip's performance. Simultaneously, the staff in the documentation department, sitting at personal computers, will pull information from the chip's design data base to produce the voluminous paperwork needed for such a project. The marketing and sales departments, armed with their assortment of computer equipment, will tap the same data base to plan their strategies for the upcoming new part.

Networking in this sense is more than physically connecting computers. It is a global system of standards and protocols that allows applications programs to run across diverse networks made up of computers and other equipment from a variety of vendors. In the ideal case, each work station or computer does what it does best, and the total of human and machine interact like one giant computing system—with each component working seamlessly and flawlessly, and with all the interaction occurring transparently. Nor is such networking confined to the technical arena. It is applicable to publishing, manufacturing, the sciences, financial services—almost any application.



Foremost among the forces driving toward this heterogeneous networking is the worldwide competitive market. To stay competitive, a company's engineers, designers, marketers, and support staff can no longer work as islands. They must turn out more complex products faster than ever.

To do that, they must talk to each other—that is, work as a design team on a network. On the corporate side, especially within the *Fortune* 1000 group of leading companies, competition demands the coordination of geographically dispersed centers—and that means worldwide networking. Also, the hodgepodge of incompatible local-area networks within many operations is begging for control. That means executives are looking for internetworking products to make more efficient use of the installed nets.

Marketing pressure for global electronic services is growing. At a world conference earlier this month of the International Videotex Industry Association, representatives of 21 countries cited the lack of easily accessible networks as a major stumbling block for videotex development.

On top of those forces, rapid developments in standards and communications technology are about to overcome many of the limitations of existing networks. Those limitations are not inconsiderable. According to Gordon Bell, vice president of Ardent Computer Corp. in Sunnyvale, Calif., if national research-and-development computing environments are to be connected, LANs need to be speeded up by an order of magnitude, to 100 Mbits/s, and wide-area networks—which are just reaching 1 Mbit/s—must go beyond 100 Mbits/s.

A global system of networked heterogeneous equipment will be reached by a number of parallel steps over the next decade. First, standardization will

begin to accelerate as more people adopt fewer standards. Those proposed by the International Standards Organization will begin to prevail (see p. 68). Many more operations with geographically dispersed LANs or wide-area nets will begin interconnecting—LAN to LAN and LAN to WAN (see p. 70). Installations of both private and public WANs will accelerate, linking far-flung computer and telecommunications operations through an assortment of copper cabling, fiber optics, satellites, and other media (see p. 75).

At the same time, all work groups of any significant size, whether using work stations or personal computers, will be connected over some kind of LAN. This is already well under way, with three LANs prevailing: Ethernet, which is backed by a number of vendors, principally Digital Equipment Corp. and Xerox Corp.; token ring, also backed by numerous vendors, chief among them IBM Corp.; and Appletalk, the solution from Apple Computer Inc. A fourth LAN, based on FDDI, the forthcoming fiber distributed data interface standard, will begin to ramp up starting next year (see p. 80). High-end work stations, at least, will become synonymous with networking and with distributed computing (see p. 83). At the component end, semiconductors will be pivotal in networking, providing facile, inexpensive chips specifically for FDDI, integrated services digital network, and other networking applications (see p. 87).

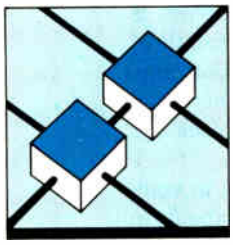
Models for intercontinental networks already exist, thanks to pioneers like Apollo, Hewlett-Packard, and others. Apollo's corporate network topology, for instance, incorporates thousands of nodes and users, with small and large computers from Apollo itself, AT&T, Apple, DEC, HP, IBM, Texas Instruments, Wang, and others. Data zoom over a variety of media and protocols, including Ethernet, fiber optics, coaxial cable, IBM's System Network Architecture, TCP/IP (transport control protocol/internet protocol), and others. And X.25 links to public networks take the data across the U. S. and overseas.

The networking momentum will produce staggering markets. According to Volpe & Covington, an investment banking firm in San Francisco, the market for LANWANs—which are integrated, optimized communications facilities, resources, and services that are both locally and globally distributed—should spurt to nearly $2 billion by 1990, growing at an average of 56% a year. In that year, Dataquest Inc. sees worldwide LANs hitting $6.9 billion, then $8.2 billion a year later. With numbers like those, it is no wonder that the market has attracted hundreds of new vendors touting thousands of software and hardware networking goods. No wonder untangling the net of vendors, products, protocols, and standards has become a full-time job. To many, sorting out the standards imbroglio is the place to start—and the key to networking vitality.



# COMPUTERS ARE ON THE VERGE OF THE OPEN-SYSTEMS ERA

## The OSI model is almost complete, and products that meet its standards are starting to appear



The concept of open systems in computers and communications is finally becoming a reality. What's making it materialize is the International Standards Organization, which is in the process of finishing up work on standards through all seven layers of its Open Systems Interconnection reference model.

A surge of activity is rocking the OSI world. A multivendor demonstration of products using OSI standards is scheduled for June in the U. S. Organizations in the U. S., Western Europe, and the Far East are working on the real functional specifications for base standards and conformance tests. That means increasing numbers of equipment, software, and service vendors can more easily develop products conforming to the OSI standards. The largest computer companies are supporting OSI and have already fielded OSI-compatible hardware. Software vendors are starting to offer OSI products. Adherence to OSI standards soon will be a prerequisite for companies bidding for government contracts in both the U. S. and Western Europe.

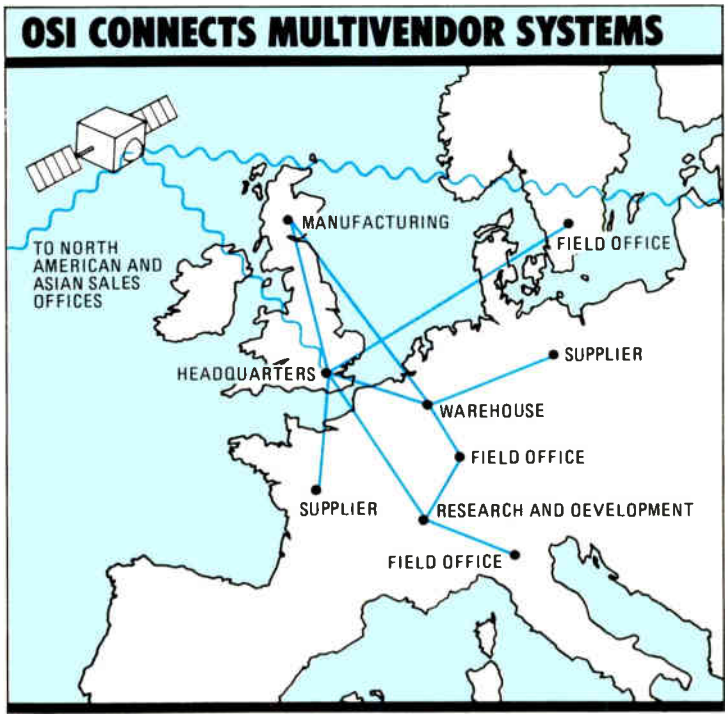
Several OSI standards already exist and are beginning to be used in products—enough to make networking of computer equipment from multiple vendors ready to blossom (see fig. 1). Several other, high-level OSI standards will be finished this year, especially in the crucial seventh, or application, layer. This layer deals with correctly formatting data between one application and another—it is the layer that makes the OSI network useful and accessible to the users. A number of vendors are getting ready with products that use the emerging standards.

"Activity has been quite intense and interesting in the application layer in the last two years," says Robin John, senior manager of communication software development at Concurrent Computer Corp. in Slough, UK. Seven such standards are either ready or moving rapidly toward completion (see fig. 2), says John, who is also the convenor of Working Group 5 of ISO's OSI Subcommittee 21.

"This year is a landmark for WG5 because the first ISO application standards will be published," says John. The first standard is FTAM. The X.400 electronic-message standard, an application-layer standard for electronic mail, was first published in 1984 by CCITT. The ISO equivalent, Motis, extends X.400, and a new version of X.400 to be published by CCITT this year will incorporate the Motis extensions. Following rapidly behind FTAM will be the standards for job transfer and virtual terminals, says John. Both will be ready by late 1988 or early 1989.

The main standard currently under development by WG5 is the transaction processing standard, OSI-TP.

**1. With OSI standards** in use, an organization can communicate among computers at various offices, suppliers, and customers.



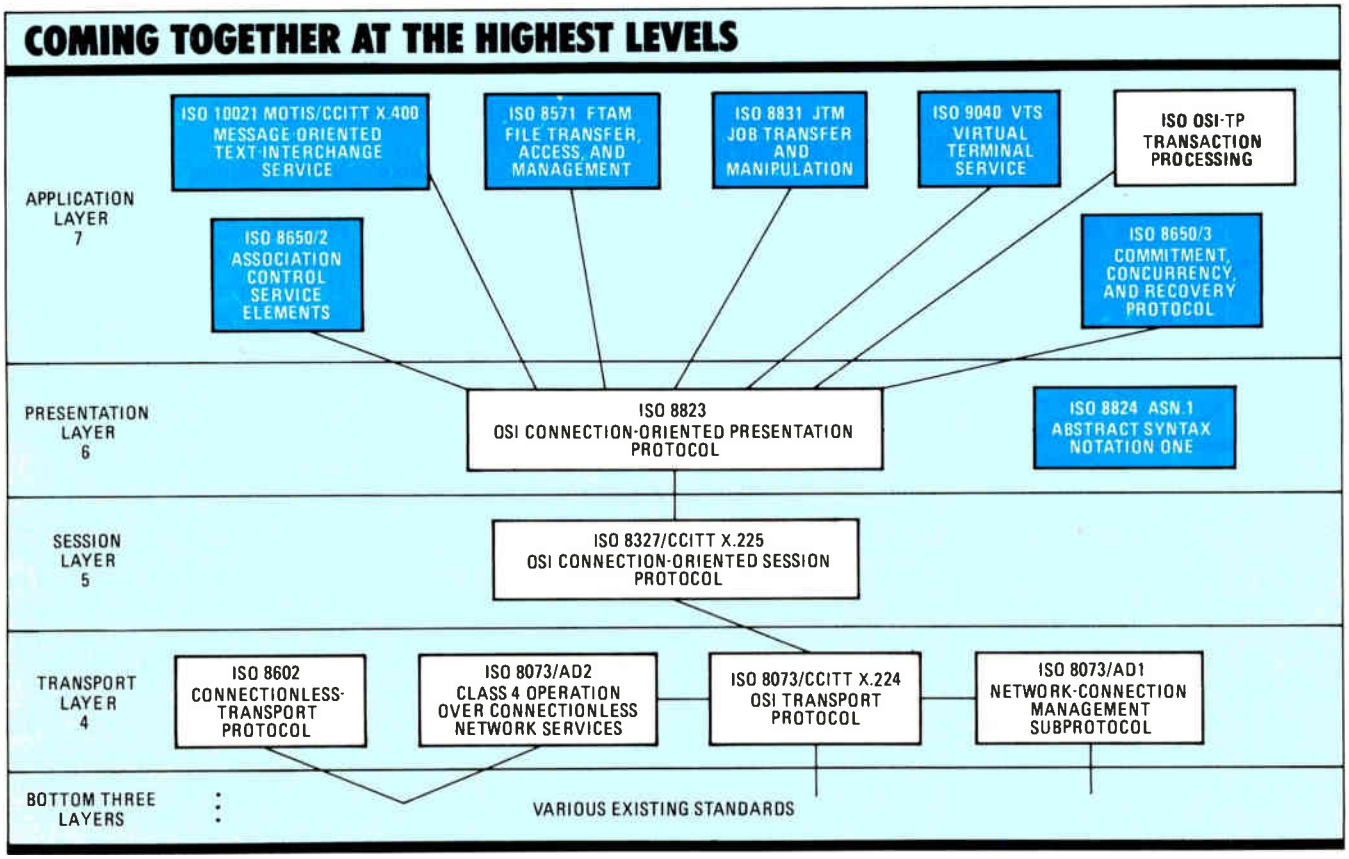

"We are making extremely rapid progress on this one—we reached the draft proposed standard stage in 18 months," says John. "We expect to push it to the draft initial standard stage during 1989."

An important aspect of OSI-TP is that it won't be the same as IBM Corp.'s Logical Unit 6.2 Advanced Program to Program Communications. "Some of the services provided will be similar, the way they will be implemented at the protocol level will be quite different," John says.

An important demonstration of OSI networking is scheduled for early June in Baltimore. Sponsored by the Corporation for Open Systems and the MAP/TOP Users' Group, the Enterprise Networking Event 1988 International will be a demonstration of OSI solutions to enterprise-wide communications. Taking part in this showcase will be over 50 vendors from the U. S. and Western Europe. It will be held in the Baltimore Convention Center, June 6 through 9. An OSI technical conference is being held concurrently.

Elsewhere, the European Workshop for Open Systems was formed in Brussels last December to develop actual implementation specifications or working standards drawn from the base OSI standards. EWOS brings together nine organizations representing different industries, user groups, research institutes, standards committees, and a few telephone operating companies from across Europe. The formation of EWOS "was a decisive step not only for the industry but also for computer and communication systems users," says Herbert Donner, chairman of the EWOS Steering Committee and a Siemens AG executive.

EWOS aims to define, analyze, and develop OSI implementation specifications—called profiles—and the related specifications for conformity testing. Its work




**2. Standards for** the upper OSI layers are coming together as several application-layer standards march rapidly to completion.

is similar to the work being done by the National Bureau of Standards' OSI Workshop and the conformance test systems being generated by the Corporation for Open Systems in the U. S. In Asia, Japan and several other countries are putting together an Asian-Pacific Workshop to do the same.

As important as the work being done on the standards is the support they are gathering. All the major U. S. and Western European computer companies are behind OSI. IBM, for example, has made several strong, clear statements and actions regarding its support. "The primary thing I learned about OSI at IBM is that our customers, even those that are all-IBM, recognize that their business demands require that their computers be networked—not just among themselves but to those of their suppliers and customers worldwide," says Vann E. Hettinger, director of communications programming at IBM's Communications Products Division in Research Triangle Park, N. C. IBM sees OSI as a complement to its proprietary networking architecture, System Network Architecture, which will remain the core for communications among IBM equipment. "OSI is a very strong extension to SNA," says Hettinger. "We are now working in the standards groups and with COS to encourage them to concentrate on the fact that OSI has no network management," says Hettinger. IBM supports network management in SNA; the company would like to see OSI address this gap in the reference model.

IBM already offers several OSI software products, including X.400 message-handling links in its VM and VSE operating systems. It also is offering OSI-SNA interoperation verification and test services. More products are coming, probably this year, says Hettinger.

Another major computer maker, Digital Equipment Corp., seems even more committed to OSI. The Maynard, Mass., company is currently adapting its entire Digital Network Architecture to the OSI model. DEC also has five OSI products available now. They are VAX DEC/MAP, a multivendor LAN for manufacturing, which conforms to the MAP Version 2.1 standard; Message Router X.400 Gateway V1.0; VAX OSI Applications Kernel V1.0; VAX OSI Transport Service; and VAX Packetnet System Interface.

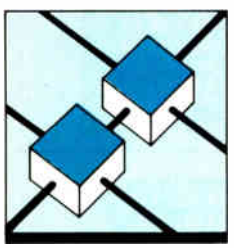
Like DEC, Data General Corp. is adapting its Xodiac network architecture to the OSI model. "We intend to have a full, totally compliant OSI network architecture over the next couple of years," says Joe Forgione, director of marketing for communications products. The Westboro, Mass., company is about halfway there, with coverage of the first four layers already in place. It also has an X.400 product and is working on other application-layer products, with an FTAM product almost ready to go.

*-Tom Manuel with additional reporting by John Gosch*



# THE RACE TO INTERCONNECT COMPUTER NETWORKS IS ON

## Vendors of bridges, routers, and gateways are fighting for position in the OSI-product market



The proliferation of multivendor computer networks incorporating dissimilar topologies, architectures, and communication protocols carries with it both challenge and opportunity for the companies building links. The market for these glue products—bridges, routers, and gateways—is in an upsurge that will translate into an order-of-magnitude growth by 1991.

The challenge lies in deciding which computer and network vendor approaches—and especially which communication standards—offer the best chances to grow. Right now, it looks as if system, network, and link product suppliers are all lining up behind the International Standards Organization's Open Systems Interconnection reference model as they jockey to gain market share—which is where the opportunity lies (see chart, p. 74). The companies that grab the lead in OSI products will be getting a slice of a market that's projected to grow to more than half a billion dollars in the next four years.

ISO has just about finished defining the seven layers of the OSI standards (see p. 69). After the standards get their final touches, OSI-related products should start appearing in large numbers; they should begin arriving next year. Further OSI-related market stimulation will come from the U. S. government, which has set a timetable of two years to specify compatibility with OSI standards in its network-related procurements.

Meanwhile, there's gold awaiting the vendors of internetwork products even before the steep OSI market climb takes place. Forrester Research Inc., a Cambridge, Mass., market research firm, estimates that while the value of U. S. shipments in repeaters, bridges, routers, and gateways in 1987 was $58 million, it will grow to some $549 million by 1991 (see chart, next page). Gateways, the most technically sophisticated internetwork links, will account for a big chunk ($242 million) of the 1991 shipments because they have higher prices than bridges and routers.

Repeaters amplify and regenerate local-area-network signals to extend the distance over which the signals can travel. They sell for up to about $6,000. Bridges are protocol-independent, sell for as much as $40,000, and are used to connect both homogeneous and heterogeneous LANs, either locally or remotely. For example, a bridge might link an Ethernet with a token-ring network.

Routers encompass higher-level protocols to route traffic to the proper device locations across complex topologies and wide areas. A router could link an OSI/Ethernet to an IBM Corp. System Network Architecture Token Ring, for example. Router prices can be as much as $50,000. Gateways accommodate applica-

tions such as electronic mail and file transfers in linking networks with dissimilar protocols. They may translate X.25 to Ethernet, for example. Prices can reach $50,000 or more.

As with many emerging markets, this one is populated primarily by young companies, often startups that are quick to recognize and react to new opportunities. There are giants as well, notably Digital Equipment Corp., Maynard, Mass. At DEC, the corporate dedication to providing a range of interconnected compatible systems from desktop units to supercomputers has fostered a rich parallel business in bridges, routers, and gateways to link DECnet Ethernets and to tie those into IBM's SNA.

**THE MARKET FOR SPANS WILL SOAR**

| Span type | 1987 | 1988 | 1989 | 1990 | 1991 |
|---|---|---|---|---|---|
| | $ thousands | | | | |
| Repeaters | 5,000 | 8,750 | 13,130 | 22,150 | 20,500 |
| Bridges | 15,000 | 34,300 | 70,700 | 88,600 | 164,050 |
| Routers | 15,000 | 23,100 | 46,000 | 73,800 | 118,260 |
| Gateways | 23,000 | 26,250 | 67,800 | 150,390 | 241,990 |
| Total | 58,000 | 92,400 | 197,630 | 334,940 | 544,800 |

SOURCE: FORRESTER RESEARCH INC.

That business will continue to flourish, in the opinion of George Colony, Forrester Research's president, as DEC broadens its penetration of the IBM world. "I expect the installation of gateways and bridges between the IBM and DEC network environments to boom," Colony says. He also looks for DEC to step up its efforts to comply with OSI standards, a direction DEC clearly indicated in recent announcements.

One of those in January encompassed the VAX Message Router/P gateway, which enables users of IBM's Profs electronic mail to exchange mail or documents with DEC's MAILbus electronic-mail users in a global messaging network. Michael Gayowski, marketing manager for DEC's IBM interconnect products, says those products fall into two categories: a single-VAX system-to-network solution, called VMS/SNA; and a network-to-network solution, named DECnet SNA gateway, which connects multiple VAXes to the SNA world.

Gayowski says users can transfer files between DEC and IBM systems without having to learn a new language or system architecture "by using our data-transfer facility, with a VAX accessing a file from an IBM computer or vice-versa." And at DECWorld last fall, DEC went on record as saying that DECnet phase 5 will comply with the OSI standards. "We're committed to standards," Gayowski says. "That's fundamental to our strategy for the future."

Colony, of Forrester Research, observes that OSI is later than hoped for in becoming widely deployed. That fact has benefitted IBM—large companies are continuing to standardize on IBM communications. But even IBM supports OSI in Europe with a gateway running under the VM operating system.

OSI standards (see fig. 2) are fundamental to the strategy of Retix, Santa Monica, Calif., which has built a solid business supplying software protocols (and recently systems) based on OSI standards since its founding in early 1985. Retix has more than 80 licensees using its software, including Hewlett-Packard, IBM, and Prime Computer.

For his part, Charles Chriss, vice president for North American marketing and sales for Retix, isn't perturbed by OSI's slow evolution. "OSI has been slow to emerge because the standards are very complex," he says. "This is the successor to all existing communication technologies, and it shouldn't be surprising that it takes a long time to get things done technically and politically" when dealing with standards organizations.

Chriss sees 1988 as a transition year for OSI developments. "The standards have been defined and things will start moving," he says. "Where last year we saw almost no OSI products, we'll see them everywhere we look next year."

Back at DEC, Karl Pieper is marketing manager for extended LANs in Merrimack, N. H. He's closely monitoring OSI standards evolution, although DEC's LAN Bridge 100 "could run OSI tomorrow" because bridges are protocol-independent. The company's router products would need an OSI routing capability that they'll acquire with DECnet phase 5 OSI.

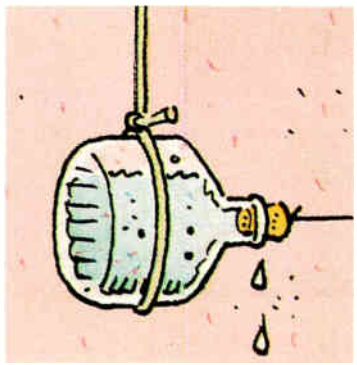
Pieper explains that DEC's bridges are truly extenders between LANs that are close to each other—on the same campus, for example. For a remote-LAN interconnect, for example to link a LAN in New York with one in Chicago, DEC turns to Vitalink Communications Corp., Fremont, Calif.

Vitalink grew out of the satellite communications business, but the company's core business is now in providing LAN bridges, according to Randy Fardal, director of marketing. Vitalink has a joint marketing agreement with DEC under which Vitalink provides DEC a bridge to tie remote Ethernets into an IEEE 802 wide-area network.

Fardal says that more than 3,000 TransLan bridges have been installed in more than 500 WANs to date. One of the largest of these Ethernets, using 35 bridges, is centered at General Motors Hughes Electronics in El Segundo, Calif. (see fig. 3). Fardal points out that because of customer feedback from these numerous installations, Vitalink has developed a "brouter," a product that combines bridging transparency with router path control.

Last year, Vitalink and DEC together took another step to facilitate bridging sophistication that still offers the simplicity of bridging to users. The two companies refined and implemented the Spanning Tree Protocol, which identifies loops or paths in a network, calculates all possible path capacities, and deterministically places the lowest-capacity links in a backup mode. Then by adding distributed load sharing on top of the STP, Vitalink came up with a protocol superset

# MAKE THE RIGHT CONNECTIONS.



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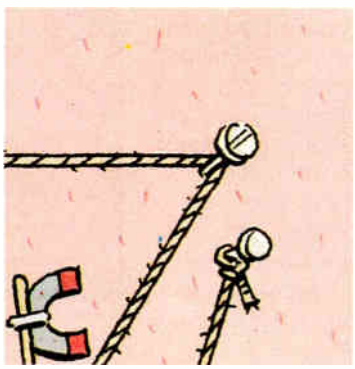

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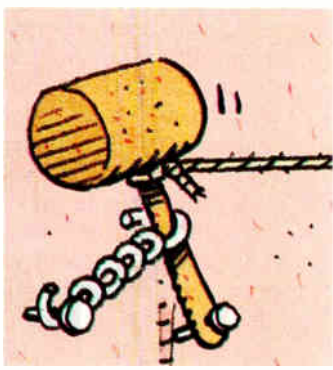

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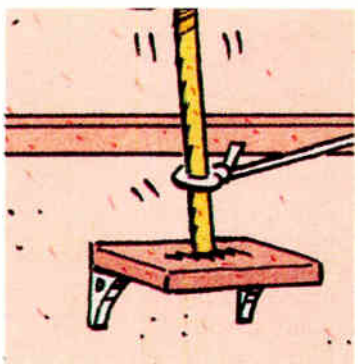

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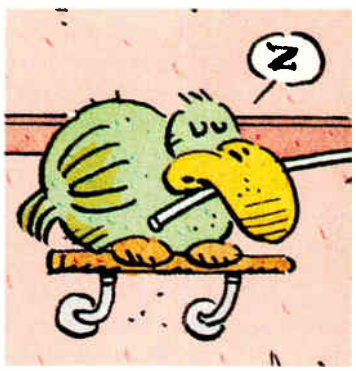


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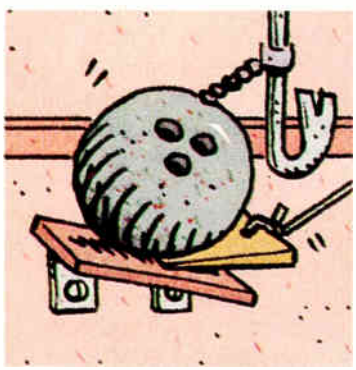

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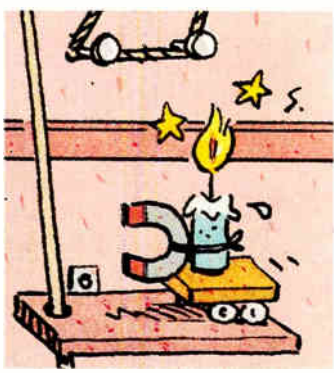

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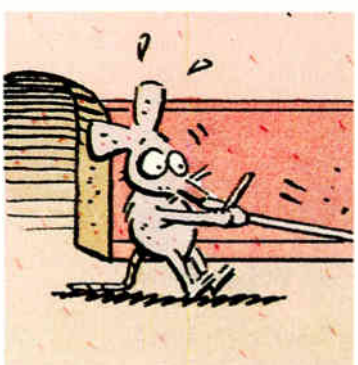

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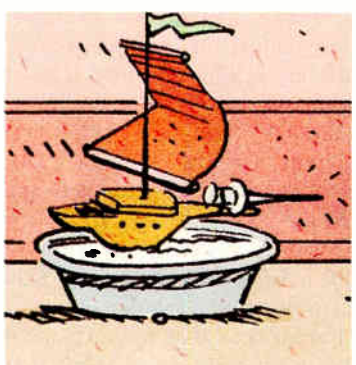

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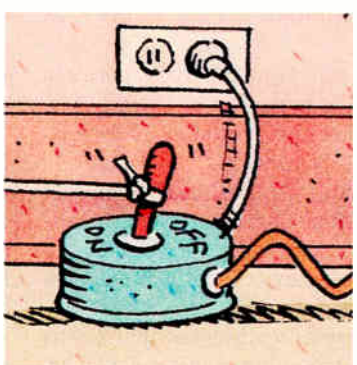


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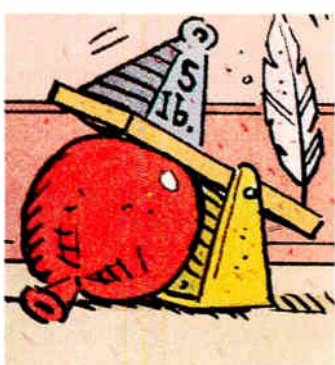


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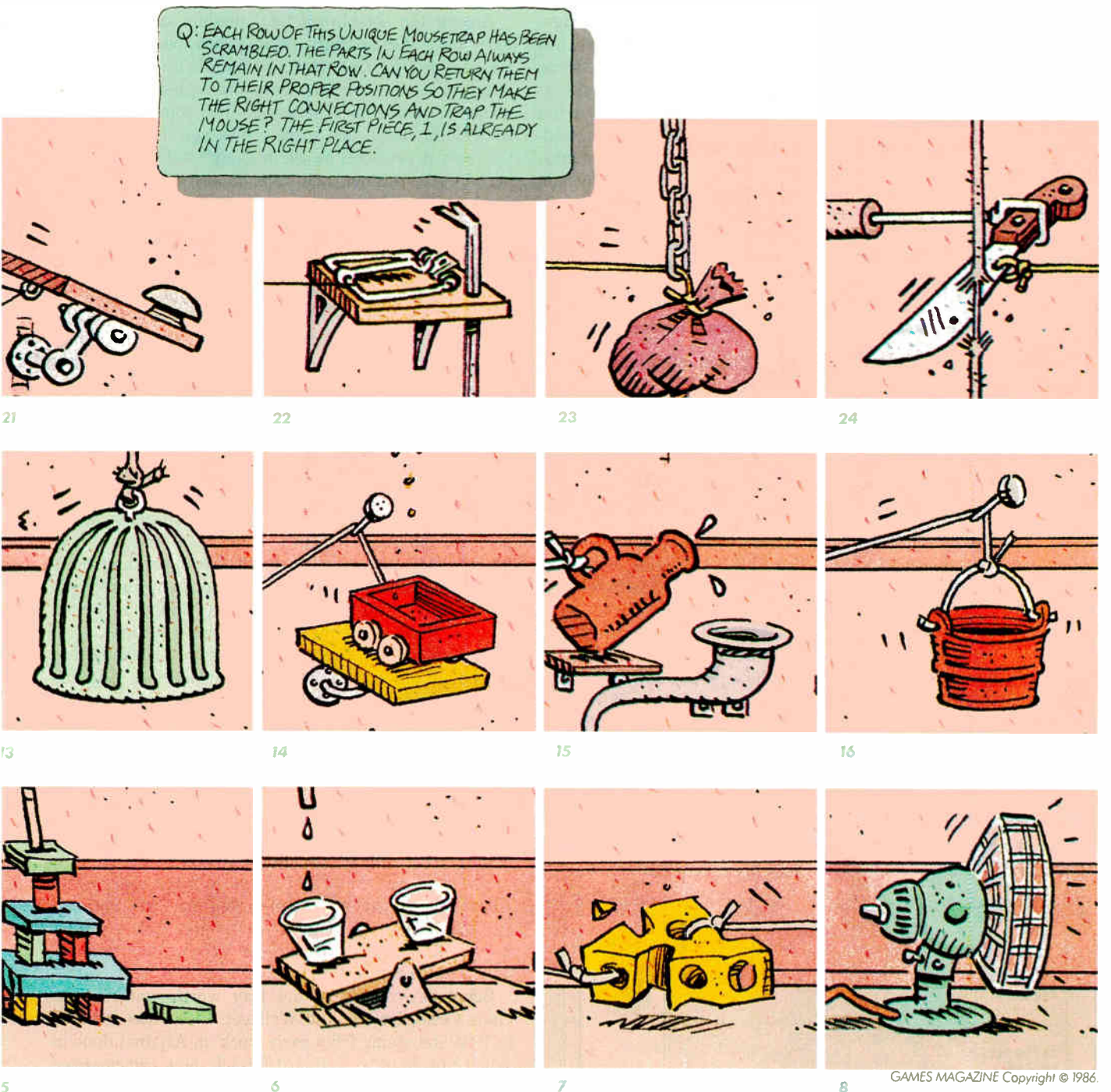


that differentiates a brouter from an ordinary bridge.

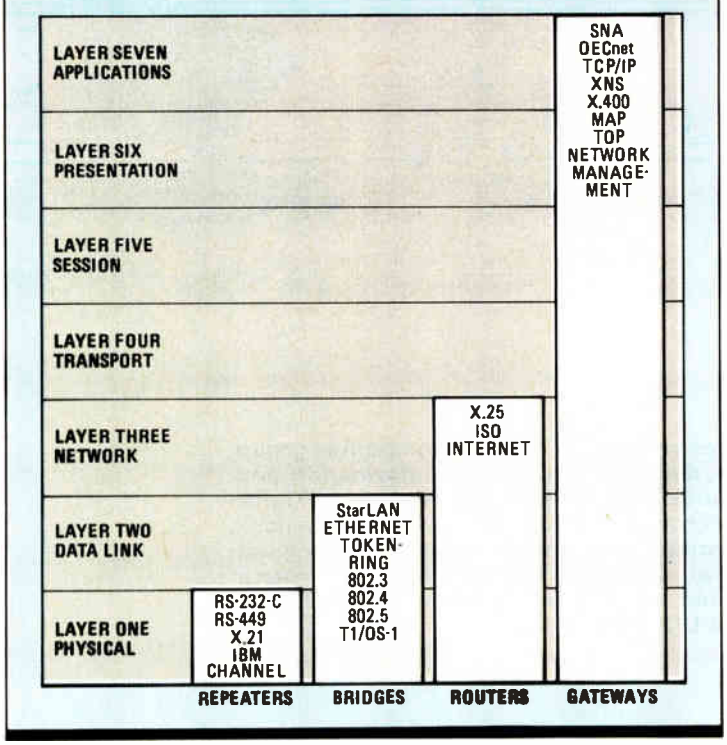
Vitalink has been the dominant bridge supplier, but that situation could change as other companies, some of them startups, hop onto the internetwork bandwagon. The roster includes familiar names such as the Bridge Communications division of 3Com Corp.; Advanced Computer Communications, Mitek Systems, and Proteon. Relative newcomers to the fray include

'Fiber-optic Distributed Data Interface will be a major market phenomenon; network hierarchies now evolving need the 100-Mbit/s speed of FDDI'

Cisco Systems, CrossComm, Halley Systems, and Wellfleet Communications.

Tad Witkowitz, president of CrossComm, Marlborough, Mass., agrees with Forrester's Colony in scoping the growth of the interconnect product market. "We came up with a similar range of figures," Witkowitz says. His company's latest product is the ILAN-1, a sophisticated bridge that links any combination of Ethernet or StarLAN networks into a single communications net. The ILAN-1 chassis will later accommodate token-ring and optical-fiber networks, as well as AT&T Co.'s T1 and 56-Kbit/s leased lines. Witkowitz looks for twisted-pair Ethernet, rather than today's coaxial cable, to come on strong in the near future, as does DEC. But he expects both the Fiber Distributed Data Interface and the Integrated Services Data Network standards to take substantially longer to penetrate the market because of their relatively higher costs.

**WHERE SPANS FIT IN THE OSI MODEL**




Among the established LAN product suppliers, Proteon Inc., Westborough, Mass., has been supplying LANs since 1981. Gateways and routers are more recent offerings as the company eyes the high-speed requirements of optical-fiber networks. The company's p4200 router, introduced just three weeks ago, handles all of the popular protocols in use in today's networks, including TCP/IP, DECnet, and XNS. It also allows users to create large, high-speed fiber-optic backbone networks and can migrate easily to the FDDI standard when FDDI becomes a commercial reality.

Patrick Courtin, Proteon's president, says that if he were a computer central processing unit designer today, he'd go to the FDDI's 100-Mbit/s data rate in the CPU backplane in order to handle a hierarchy of networks that range from that level down to below Ethernet's 10-Mbit/s rate. "We believe that FDDI will be a major market phenomenon, and the network hierarchies that are now evolving need the speed of FDDI."

Another veteran company, Advanced Computer Communications , Santa Barbara, Calif., has jumped into the remote Ethernet bridge market with an offering that challenges Vitalink's bridges, accommodating modems ranging in speed from 1,200 bits/s to 64 Kbits/s. ACC got its start in 1975 by providing host-computer attachments to the Arpanet (now Darpanet).

The ACS 4030 remote Ethernet bridge sells for about a third of the price of Vitalink's bridges, says Gary Krall, ACC's director of marketing. He says that Vitalink "has had a hold on that market, but the market is now opening."

An oldtimer by today's standards, The Bridge Communications division of 3Com Corp., Santa Clara, Calif., provides a broad range of bridges, routers, and gateways. The company has deep roots in the past but is also looking ahead at both FDDI and OSI opportunities, according to Bobbi Murphy, Bridge's product line manager for internetworking products.

She estimates that FDDI is two to three years away from implementation. "We're looking at FDDI and will participate in that market. We've also got a strong commitment to OSI, and already have an OSI terminal server, the CS-1, on the market."

Some newcomers to the fray worth watching include Cicso, Halley, and Wellfleet. Cisco was founded in 1984 and stems from early work on Arpanet done in TCP/IP by founder Leonard Bosack, now principal scientist and a board member. William Graves, chief executive officer, maintains that Cisco's internetwork products, which include gateways and terminal servers, allow the interconnection of larger and more complex networks than heretofore possible.

He says Cisco's gateway technology can handle networks as large as 100,000 subnets in an integrated WAN comprised of multimedia, multiprotocol, and multivendor subsystems. One of the company's claims to fame is its Interior Gateway Routing Protocol, which provides for automatic packet routing and optimal packet flow. Cisco has landed an impressive customer in Hewlett-Packard Co.'s HP Internet, a corporate network that links 10,000 computers over five continents and more than 110 Ethernet segments.

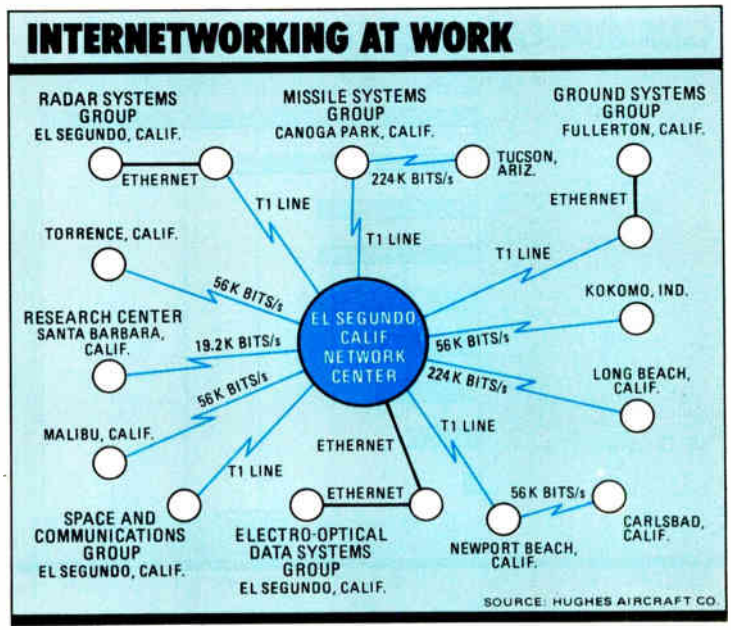
Wellfleet, located in Bedford, Mass., is even newer

than Cisco and isn't talking about customers yet. The company was founded in mid-1986 by Paul Severino, president and chief executive officer, who earlier founded a network-products company, Interlan, before selling it to Micom Inc. Severino started Wellfleet after he recognized the need to provide standards-based internetworking products. The company's 68000-based chassis [*Electronics*, Nov. 26, 1987, p. 168], accommodates bridges and routers that interconnect any combination of most LANs and WANs.

"Our focus is in WAN and T1 connections especially," Severino says, "and on sophisticated users who have to deal with multiple protocols and more than two sites." Wellfleet also provides network management, while another distinction, according to Severino, is the ability of Wellfleet's server to allocate the 1.544-Mbit/s bandwidth of a T1 line among routing, bridging, and voice services to make more cost-effective use of expensive T1 lines.

Halley Systems Inc., San Jose, Calif., founded last May, has just introduced a LAN/WAN internetworking system called ConnectLAN. Ed Moura, marketing manager, describes it as a brouter, another combination of bridge and router. Moura adds that ConnectLAN can do all that Vitalink's brouters do, and then some, because of the comprehensive network-management tools the product incorporates.

The management function is provided by a graphics-based work station, which offers network mapping; device installation, configuration and control; real-time monitoring; troubleshooting and traffic analysis.




**Hughes Computer Network** is one of the largest Ethernets to date, linking more than 10,000 users in 20 sites.

These newcomers reflect a trend that Forrester's Colony says will become even more widespread. The black-box protocol/conversion of the past will give way to sophisticated servers—computers that combine the bridge, router, and gateway functions as they creep upward in the OSI model. *–Lawrence Curran*

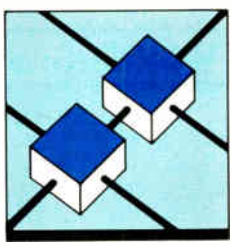
**INSIDE TECHNOLOGY** **NETWORKS**

# WIDE-AREA NETS EXPLODE AS STANDARDS EMERGE

## The market for communications gear is about to soar, with ISDN equipment setting the pace

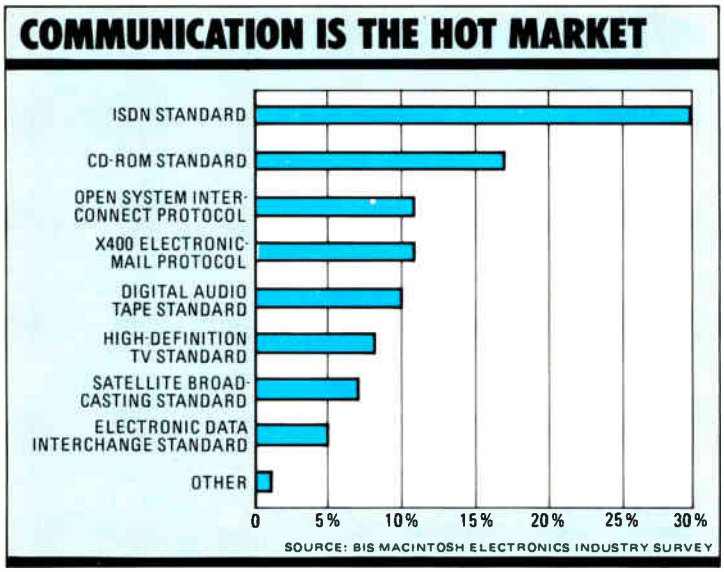
Equipment markets tied to wide-area networking are expected to snowball as the impact of a projected 34% growth in the data and telecommunications sector this year ripples past the private branch exchange and into the customer's premises. Growth will be driven not just by the availability of high-speed, error-free communications technologies, but by the adoption of standards that rationalize a proprietary-systems jungle. Communications-product manufacturers will find markets in chips, high-speed switching systems for voice and data, and, perhaps most important, the hardware and software to manage the networks (see panel, p. 77).

In a 1987 survey, London-based BIS Mackintosh Ltd. asked a worldwide sample of electronics industry managers to pinpoint the hottest product groupings for 1988. Communications products finished first with a projected 34% sales growth. The managers were also asked to specify which of nine developing standards would have the greatest impact on market development. Three of the top four standards—Integrated Services Digital Network, Open Systems Interconnect Communications Protocol, and the latter's subset, X.400 Protocol—accounted for 52% of the responses (see graph, p. 76). The only evolving noncommunications standard to break the top four was the compact-disk read-only-memory standard, with the digital-audio-tape standard ranked fifth. Not mentioned in the survey but potentially a major market force was Sonet, a product of the Bell Communications Research Corp.



ISDN—a global standard that integrates voice and data on the same service—was a particularly strong finisher in the survey, with 30% of the respondents saying it will be a major force in shaping the market. "Agreement on standards is notoriously difficult to achieve," says Gerry Clarke, project manager for ISDN research at BIS Mackintosh. "In these circumstances, to have more than 10% of the responses saying that a particular standards development will make the most significant contribution to market development in 1988 is a substantial result. A 30% agreement on the importance of ISDN is a clear pointer to what will dominate in 1988 and subsequent years."

Sales of chips that implement both ISDN's 192-Kbit/s, two-channel basic service and its 23-channel, 1.54-Mbit/s primary service have spurted. Of the approximately 5 million ISDN chips sold over the past




**When BIS Mackintosh** asked industry leaders which new standard would most affect market growth, 30% said ISDN.

five years, half were sold in 1987 alone, says Alan Clark, telecommunications marketing manager for Siemens Components Inc., Santa Clara, Calif. The market for integrated circuits is expected to grow at a rate of 25% per year from a 1988 base of $50 million. A major reason is that the vast body of ISDN standards, although not final in most cases, has been closely enough identified that any last-minute changes can be easily accommodated in either silicon or software. The trend toward introducing development tools [*Electronics*, Oct. 1, 1987, p. 65] has continued, and is exemplifed by the ExpressCard introduced last year by Mitel Corp. AT&T, Intel, Rockwell, and more recently Siemens have introduced similar products. "Our development tools help you generate source-code software," says Clark. "This way, you can handle changing standards or quickly change switches." Software written for Northern Telecom's DMS100 digital central-office switch can now almost automatically be amended to work with AT&T's 5ESS switch or Siemens' EWSD switch.

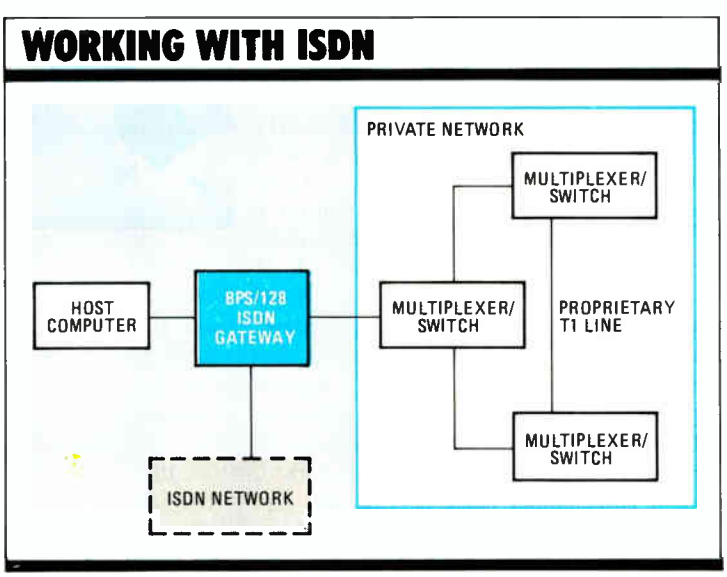
The chore of making ISDN compatible with existing telecom hardware has become the market focus of several startups. Telestream Inc.'s Bitstream Processing System, for example, reflects a trend toward use of programmable platforms to create customized network products—and to make market entry easier. When used as an ISDN gateway, the BPS/128 packs the processing power to perform the complex conversions between proprietary signaling systems and the protocols of ISDN's Primary Rate Interface (see figure, below). The BPS/128 can also provide compression and compatibility conversions for ISDN's voice and data channels. Powered by Motorola Corp. 68020 microprocessors, the BPS/128 can support up to 20 T1 lines and boasts an internal bus capable of handling 1.28 gigabits/s. Using it as a platform reduces research and development costs for WAN products and shortens time to market.

Bob Emerson, marketing vice president at the Mountain View, Calif., company, agrees that ISDN "is certainly starting to happen. But companies interested in benefiting from it should be focusing on the incompatibilities between the major implementations. The standard bodies still are not finished, and the network layer is incomplete enough that it gives the major vendors a large degree of freedom. AT&T, Siemens, and Northern Telecom all have different implementations of the primary rate."

While the services will be there, says Emerson, users of ISDN-compatible equipment still have a substantial investment in T1 equipment—PBXs and multiplexers, for example—and a technological catalyst is needed. "One application we see for our BPS/128 is to do real-time conversions, expecially since there is often a proprietary multiplexer at each end of the T1 line," says Emerson.

Beyond telecom applications, ISDN will eventually make a big impact in the home. With 80 million households in the U. S., says Emerson, the most likely area for growth is the professional who works on a personal computer in the office and wants the same power at home. "No modem would be required, and you would need a basic-rate terminal-adapter box on the desk," says Emerson. "If the Macintosh SE had a jack for connecting to the phone, that would be an interesting enhancement. Mac software original-equipment manufacturers could do things like tap ISDN's signaling channel for the calling party's phone number and match it in a data base to identify the caller by name. I think there is more opportunity in the basic rate for the PC manufacturer than for the phone people."

Joining ISDN in the Mackintosh BIS list of the top four standards developments expected to drive the market in 1988 and beyond are the CCITT's OSI protocols and the X.400 protocols for electronics messaging. X.400, a subset of the OSI protocol, is one of the first to reach the marketplace. It provides a standard for exchanging electronic mail between incompatible com-




**Configured as** an ISDN gateway, Telestream's BPS/128 performs the conversion to link old and new network protocols.

puter systems. Although formal adoption may be a year or more away, "X.400 is now a standard to the extent that it is no longer a moving target," says Joseph Forgione, director of communications products marketing for Data General Inc., Westboro, Mass.

Data General introduced its X.400 software product last year as a complement to its Comprehensive Electronic Office electronic mail and office automation system. Digital Equipment Corp. is expected to announce similar X.400 enhancements to its All-In-1 electronic office system this year. So is IBM Corp. for its Profs and DISOSS systems. The standardization of electronic messaging will almost certainly drive demand higher for office-automation equipment, says Forgione, but the market is so new—and potentially vast—that "it would be very difficult to put a dollar figure on it."

Meanwhile, OSI's already mature X.25 packet-switching standard expects new growth. Because it uses packet-switched multiplexing—and is not dependent on keeping an open channel—X.25 lets users buy the bandwidth they need and then assemble and dissassemble data according to the protocols. X.25 technology has achieved critical mass, says Doug Avery, manager of U.S. network marketing programs for Hewlett-Packard Co. in Cupertino, Calif. Secondary-market vendors are already providing devices that achieve connectivity by changing various protocols, with X.25 as a common denominator between proprietary systems.

Expansion of WANs using X.25 will mean opportunities for small-to-medium OEMs to develop products in secondary markets. "A lot of small companies with specific networking needs will provide markets for niche products or value-added products," says Avery. "On the local-area-network side, people will be looking for new services, such as facsimile machines that support X.25."

While protocol standards are on the move, standards are also advancing in the crucial area of transmitting data as fast as possible. Although most of the

## IN NETWORK MANAGEMENT, A LESS PROPRIETARY APPROACH EMERGES

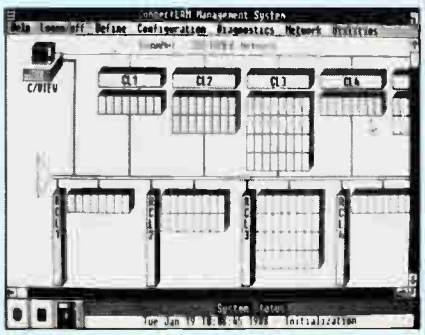
Network-management systems are no longer stand-alone, one-vendor products. Now when a vendor tackles the problem, it must bow to IBM Corp.'s approach while genuflecting toward evolving net-management standards from the International Standards Organization. The issue grows more vital and complex as large numbers of physically scattered local-area networks running on different hardware under different protocols are tied together into a cohesive whole.

While industry observers agree that IBM's contribution to network management is crucial, most feel that IBM is unlikely to dominate the market for net-management systems. In fact, the networking world is beginning to break loose from the proprietary approach to internetworking and network management that has been the norm.

Recent introductions from Hewlett-Packard Co., Palo Alto, Calif., and Halley Systems Inc., San Jose, Calif., fit the pattern. HP's OpenView and Halley's ConnectLAN/View are both designed for managing multi-LAN networks tying hardware from multiple vendors. Both are designed to operate where no IBM systems are present and where the Open Systems Interconnect standards from ISO are not yet implemented. But both companies say they either can or will shortly provide links to the NetView product IBM unveiled in 1986, and that they will fit in with the OSI standards as they develop.

A network-management system is a software package running on a mainframe (in the NetView case) or on a work station. Data from such network hardware as bridges, gateways, multiplexers, switches, and intelligent modems is sent to the net-management system, which stores it and performs a number of functions that aid the network's human managers.

The system monitors the network's operation, notifying operators when troubles—such as malfunctioning equipment or an undue rise in error rates at some location—occur. Tools for network configuration, performance measurement, troubleshooting, equipment control, data-base querying, report generation, and inventory management are among the offerings from various companies. The "view" in product names refers to the move to graphic representations of a network's topology: the network manager is not just handed a list of printed data on network functions, but can look at a visual map of the whole network showing exactly what is linked how, and where the problems lie (see photo).



**A graphic view** of a net from Halley System's ConnectLAN/View aids management.

Most existing net-management systems take a proprietary approach. They may tie together LANs and equipment from multiple vendors, but the hardware used for the internetwork linkage—modems, gateways, and so on—must all be from the one company providing the network management solution. The reason for this is that there have been no standards as to the exact type and format of data that the net hardware passes back to the net-management system.

But the new systems will be able to pass alarms and collected statistics to NetView, if the customer has chosen IBM's approach to central net management—a likely choice, if his network includes mainframes communicating via IBM's Systems Network Architecture protocols. Thus Halley System's modems and bridge/routers can be used in conjunction with NetView, because the data they generate can be passed on to NetView by the ConnectLAN/View system.

Internetworking-equipment makers, meanwhile, are keeping an eye on the OSI standards called Management Framework and the Common Management Information Service and Protocol. These and related network-management draft standards are expected to mature next year. IBM's NetView is a factor that must be dealt with now. But another set of links—to the OSI world—will grow in importance as that standard takes shape. *–Jeremy Young*

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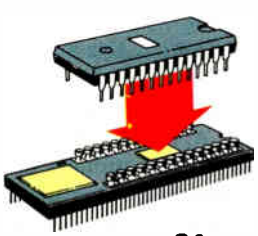

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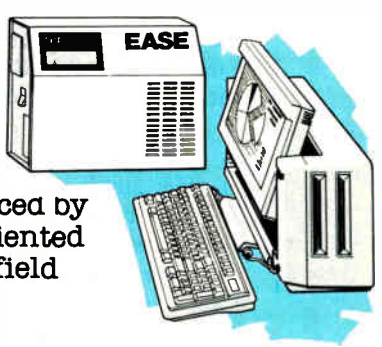


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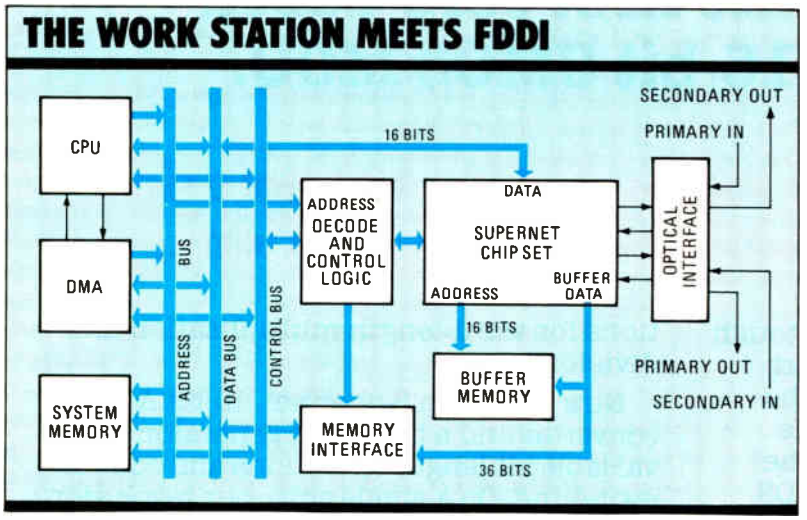



**2. Advanced Micro Devices'** upcoming FDDI Supernet chip set will allow work stations to share data over 100 Mbit/s fiber-optic networks.

Apollo last year, the forum's charter is to exchange ideas and agree on common technical approaches for computing on networks of multivendor systems. Its members include HP, Cray, Olivetti Research, Vanderbilt University, U. C. Lawrence Berkeley Laboratory, Apple, Mentor Graphics, and the Ford Motor Co.

The International Standards Organization is also getting into the act. A new working group, WG7, will submit a draft proposal by the end of next year for a Reference Model of Open Distributed Processing. RM-ODP will define the technical basis for ODP standards and relate the standards to other ISO reference models and standards. Intended to cover all matters pertaining to distributed processing, ODP will coordinate with the Open Systems Interconnection for its communications interconnection.

Standards and protocols have been both a boon and bane of communications, and networking is no different. Without the proliferation of Unix and TCP/IP, it is unlikely that Ethernet would have been popularized as quickly. Work-station vendors have no choice but to offer anything a customer wants in the way of connectivity or protocols, says Dave Dorfmueller, senior systems manager at Intergraph Corp. in Huntsville, Ala. That may involve DEC or IBM or whoever; XNS, TCP/IP, ISO, and anything else under the sun. "All those standards make it expensive but we can't ignore them," says Dorfmueller.

Whether any protocol will prevail is doubtful, therefore, even though TCP/IP has the lead in high-end work stations. But Daisy Systems Corp.—which recently announced an open-systems policy with respect to operating systems, graphics interfaces, and communications—does see TCP/IP as the winner. "The TCP/IP camp ultimately will prevail because everybody considers TCP interoperability as the ultimate goal—not just the Unix crowd, but IBM," says Bob Miller, manager of data-communications software for the Mountain View, Calif., company. "And it looks like VMS will take a serious stance in the TCP and NFS arena." Intergraph may prove him right. The company has in the works a product that will allow PC ATs, XTs, and compatibles to attach to Ethernets and communicate using TCP/IP.

Daisy is also a proponent of X Windows, a windowing standard developed at the Massachusetts Institute of Technology and supported by a sizable group of work station, software, and computer suppliers. The widespread acceptance of X-Windows, Unix, and Sun's Distributed File System will give impetus to distributed computing, as applications programs then could easily port between unlike machines and operate identically on any work station over any network.

Apple Computer Inc. is also counting on X Windows as a big factor in Mac connectivity. But the Cupertino, Calif., firm also recently introduced A/UX—its version of Unix for the Macintosh II—and plans a bag full of other communications products. One prime example is Mac-APPC (advanced program-to-program communication), a product that directly challenges IBM in the networking work-station arena. Analogous to IBM's LU 6.2 (Logical Unit) peer-to-peer environment, APPC not only allows Macs to infiltrate IBM's Systems Network Architecture networks, but also to do so as intelligent distributed members, rather than dumb terminals.

Just as interesting is the snuggling up of Apple and DEC [*Electronics*, Feb. 4, 1988, p. 47]. Within a few months, they will announce specifications to integrate AppleTalk and DECnet/OSI networks. DEC has also stated it will offer VAX connectivity to machines running MS-DOS, OS/2, and Ultrix, its own version of Unix. The deal with DEC gives Apple obvious benefits. Some say, though, that DEC's motivation is not in promulgating open systems but in warding off competition—Sun Microsystems, for example. Others are busy connecting Macs. Kinetics Inc. in Walnut Creek, Calif., has been attaching AppleTalk to Ethernet for the last two years, and TOPS, a Sun Microsystems company in Berkeley, Calif., links Macs to IBM, Sun, and other Unix computers.

With seemingly everything connected to everything else, there is little doubt that users will seek more connections and that bandwidth will become a premium. The way out seems to be fiber-optic LANs such as FDDI (see fig. 2) and backbones, and new protocols. Already, fiber networks are available from several quarters. Du Pont offers one for Appletalk that connects three times the usual number of stations and stretches the distance between stations by five times. More than 100 stations can be linked, with each almost a mile apart.

There's more: Proteon Inc. in Westboro, Mass., offers its ProNet-80, an 80-Mbit/s token ring. Artel Communications, Hudson, Mass., recently connected 90 vendors' work stations over fiber at a Sun User Group annual meeting. At Network Systems Corp. in Minneapolis, a project called DATApipe has yielded a 275-Mbit/s fiber network with many innovative developments.

But some say FDDI itself will have to wait for its blossoming. Daisy's Miller claims, "FDDI is a ways off because there's no demand for increased performance at the physical media level." – *Stan Runyon*

# LAN CHIP MAKERS GRAPPLE IN A TURBULENT MARKET

## Many back Ethernet and Starlan; others get behind Token Ring, MAP, Arcnet; a few eye FDDI

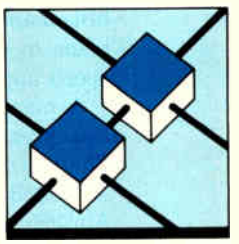
Activity at the chip level in local-area networking resembles one of those tag team wrestling matches on television. Battling it out in center ring for the largest share of the LAN market are companies backing Ethernet and Starlan. Set to jump into the ring are various firms pushing IBM Corp.'s Token-Ring network, Arcnet, or the Manufacturing Automation Protocol. Waiting in the wings for a victor to emerge are other chip makers, who could team up with any side or for that matter go their own way.

Making the situation chaotic are new variations of Ethernet, new support for the Starlan environment, as well as many companies that are hedging their bets by supporting more than one system. Throwing their weight behind Ethernet and Starlan are companies such as Advanced Micro Devices, Intel, National Semiconductor, and Seeq Technology. At the same time, Texas Instruments Inc. is supporting IBM's Token-Ring; Motorola Inc. has developed a chip set for the Manufacturing Automation Protocol; and Standard Microsystems Corp. is backing Arcnet.

Companies hedging their bets include Western Digital Corp., which plans to support the Token-Ring protocol, the token bus-based MAP, and Ethernet. Fujitsu Ltd. has a new Etherstar chip that supports both Ethernet and Starlan. Intel Corp. has a MAP board built around a custom chip design, as well as a new Ethernet chip incorporating logic that allows it to support Starlan as well. National Semiconductor Corp. has developed an interface chip that can be used to reconfigure its Ethernet controller to work in the Starlan environment. Even Motorola is hedging its bets with an Ethernet-based protocol it calls TOP, for technical and office protocol.

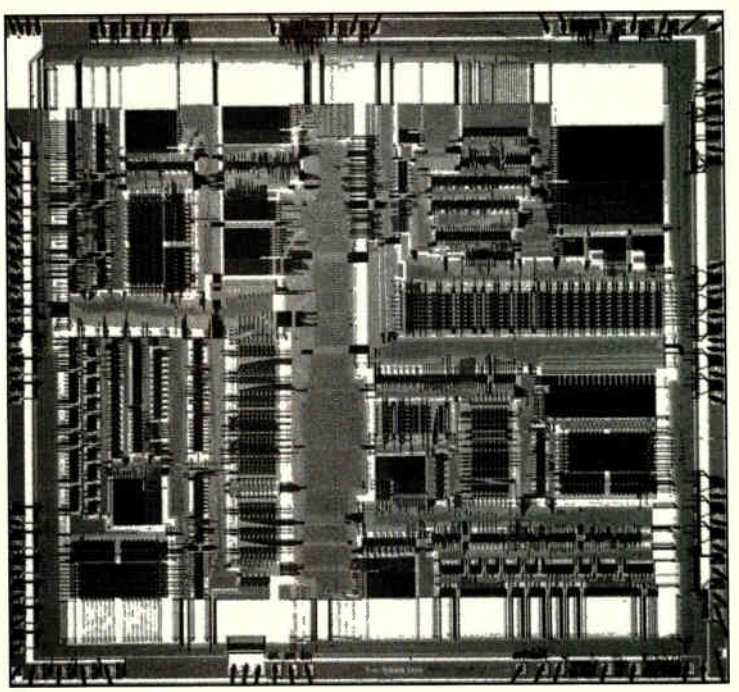
What may add to the confusion as well are chips developed for the 100-Mbit/s Fiber-optic Distributed Data Interface standard. Advanced Micro Devices Inc. was first with an FDDI-based chip set. Also considering getting into this still-developing market are National, Plessey Semiconductor Ltd. of the UK, and Signetics Corp. of Santa Clara, Calif. Muddying the waters too is the emergence of new Ethernet variations such as 10-Mbit/s, hub-based, twisted-wire systems that are an alternative to Starlan, says Tom Slykhouse, strategic marketing manager for high-speed networking products at AMD, Sunnyvale, Calif. "With twisted wire, we now have an Ethernet alternative to Starlan that is ten times faster and cheaper to boot," he says. The effect on other LAN alternatives is just as devastating, in particular the 6-Mbit/s token ring, which uses IBM's version of the standard twisted-wire specification, Slykhouse says.

In addition, the emergence of optical-fiber-based Ethernet systems does not bode well for protocols such as MAP, which is being championed by Motorola and General Motors Corp., says Gary Nelson, chief scientist, networks and communications at National, Santa Clara, Calif. "Except for the fact that MAP is designed to be implemented using the coax cabling already existing in many manufacturing facilities," he says, "an optical-fiber Ethernet configuration offers not only comparable speed, but equivalent or better hardiness in the electrically noisy industrial environment."



Claiming a dominant position in the LAN market, National offers a three-chip set that allows a designer to develop a product that supports any of the three options available within the IEEE 802.3 specification—Ethernet, Thin Ethernet, and Starlan. Under development is an interface chip that will allow it to work with the newly emerging twisted-wire Ethernet. Currently, the chip set offered by National includes the CMOS DP8390 network-interface controller, the DP8391 low-power Schottky bipolar serial network interface, and the bipolar advanced-Schottky-logic-based DP9392 coaxial transceiver interface.

The transceiver interface is designed to receive signals from the coaxial cable and send them to the network interface, which decodes the signal from Manchester code to the nonreturn-to-the-zero format that it understands. The network interface then converts that signal from serial to parallel so that it can transfer data through the system bus. There are plans to move to an all-CMOS implementation of the chip set within a year or so, as well as to incorporate the 8390 as a core cell in the company's standard-cell library, Nelson says.



**1. With its own on-board EPROM,** Seeq's CMOS 8005 Ethernet Datalink controller can support up to six unique Ethernet addresses.

For two years, the main competition to National's chip set has been Intel's 82588, a CMOS-based LAN controller designed to work in conjunction with the system central processing unit. Based on a sophisticated linked-list direct-memory-access architecture, it is designed to work with the 82C501, a CMOS-based Ethernet serial interface chip, and the 82502 Ethernet transceiver chip. Earlier this year, the 82588 was followed by a second-generation 8-bit-wide LAN controller, the 82590. The 82590 supports both Ethernet and Thin Ethernet (Cheapernet), the IBM PC baseband and broadband networks, and Starlan. In addition, Intel plans to offer a 16-bit version, the 82592, for higher-speed applications.

A more recent player is AMD, with its Am7990, a local-area network controller for Ethernet (Lance). The CMOS device is designed to work with the CMOS Am7992B serial interface adapter and the bipolar Am7996 transceiver. A key feature of the AMD offering is the ability to interface both multiplexed and demultiplexed data buses with a minimum of external logic and the ability to support four different node addressing schemes allowing considerable flexibility in the way the network is configured.

Going head to head with the larger companies is Seeq Technology Inc. of San Jose, Calif. In an attempt to broaden its product offerings beyond nonvolatile memory, Seeq has introduced the 8001 and 8002, n-MOS-based LAN controllers. They were followed more recently by the 8005, a CMOS-based Advanced Ethernet Datalink controller, which can be configured to support up to six Ethernet addresses stored in its own on-board erasable programmable read-only memory (see fig. 1).

The fast-growing Ethernet market has attracted more competition and the gang of four—National, Intel, AMD, and Seeq—must now fend off Motorola and Western Digital, among others. Western Digital is aiming to be a broad-based supplier of networking products, says Steve Ford, manager of protocol products. The Irvine, Calif., company has just introduced an Ethernet chip set for both coaxial and thin coaxial media. A three-chip solution, the Western Digital offering includes the WD83C690, a CMOS-based network interface controller; the WD83C691, an Ethernet data separator; and the WD83B692, an Ethernet coax transceiver. The chip set is fabricated using a two-level metal bipolar process.

In addition to continuing to support the MAP architecture, Motorola is also developing a board-level implementation of its own version of Ethernet. The technical and office protocol will be followed by a chip-level implementation should the market justify it, says Motorola.

Alternatives to Ethernet are still lurking about, however, including systems based on Starlan, IBM's Token Ring, and Arcnet. The 1-Mbit/s Starlan protocol remains a competitor, despite the emergence of the 10-Mbit/s hub-based, twisted-pair Ethernet standard. At least three chip makers plan to continue to support the standard with chip sets: AMD, Exar, and Western Digital. What's more, rather than develop a separate chip offering, three other companies—Fujitsu Ltd., Intel, and National—have designed their LAN offerings to incorporate the Starlan protocols as well.

AMD's offering is the Am7961 [*Electronics*, June 25, 1987, p. 89], a single-chip Starlan transceiver. Exar, of San Jose, Calif., supports Starlan with its XR-T82515 and XR-T82C516 transceiver chip set, which is designed to work with Intel's 825886 and 82588 LAN controllers. Western Digital offers a two-chip set: the CMOS WD83C603 Starlan codec and mini-hub controller and the WD83B604 dual Starlan transceiver, fabricated using its two-level metal bipolar process.

But don't give up on the IBM Token Ring, says Leon Adams, LAN market manager at TI in Houston. TI is actively supporting the architecture with a five-chip, 4-Mbit/s solution. The chips include the TMS38010 communications processor, the TMS38020 protocol handler, and the TMS38030 system interface. They also incorporate ring interface chips: the TMS38051/52, which handle transmission and reception of data, monitor cable integrity, and control network insertion for twisted-pair, shielded twisted-pair, and fiber-optic cabling.

In addition, Adams says the company has just announced the availability of preconfigured application-specific integrated circuits for TMS380-based Token-Ring adapter cards. This will eliminate much of the glue logic previously required, make it easier to adapt the chip set to specific system applications, and reduce chip count by as much as 50%. Two preconfigured ASICs are being offered: a dynamic-read-access-memory expansion unit and a PC-family-bus-interface unit, both built using the company's ASICLAN tool kit. The DRAM memory expansion unit re-

## COMPETITION HEATS UP AS ISDN SORTS ITSELF OUT

**With all of the frenzied activity** in local-area networking, chip makers are not ignoring the integrated services digital network. There are at least seven vendors, including Advanced Micro Devices, Intel, National Semiconductor, Northern Telecom in cooperation with Mitel, Motorola, and Rockwell vying for a piece of the ISDN market.

Despite the competition ISDN is churning up, though, the market is not moving as fast as many expected. The problem is that there are too many offerings, says Ron Ruebusch, director of marketing for communications products at AMD in Austin, Texas. Many original-equipment manufacturers are holding off until they can evaluate all the alternatives, or until the market sorts itself out into a few basic architectures, he says.

As a result, most of the effort during 1988 is in fielding evaluation boards and development software to attract designers. The most recent such effort is from Intel Corp. The Santa Clara, Calif., company this month introduced the ISP88, an ISDN software package for the 80188. Also introduced was a PC-based coprocessor board that allows a user to establish a voice call and simultaneous circuit switched data or PC-to-PC file transfer through ISDN switched access.

Demonstration subroutines are included to show examples of the same capabilities in a back-to-back PC environment with no switching involved, says Mammohan S. Passi, Intel's telecom marketing manager. A debug port is provided on the board and supported by software so that diagnostic messages can be sent over a standard RS-232-C connections. *–B.C.C.*

places the glue logic required to interface the chip set to DRAM expansion memory, providing a 14-to-1 parts saving, Adams says. The PC-family-bus-interface unit replaces the glue logic required to link the chip set to an IBM PC or clone input/output bus, providing about a 22-to-1 parts savings.

TI is also aware of the perceived advantage of the 10-Mbit/s Ethernet data-transmission rate over the current 4-Mbit/s Token Ring, Adams says. TI is developing a 16-Mbit/s version, scheduled for introduction in the fourth quarter, that will more than quadruple the current Token-Ring transmission rate and outperform the Ethernet specification by 60%. In addition, the new Token-Ring offering will reduce total component count, excluding glue logic, from five to two chips, he says.

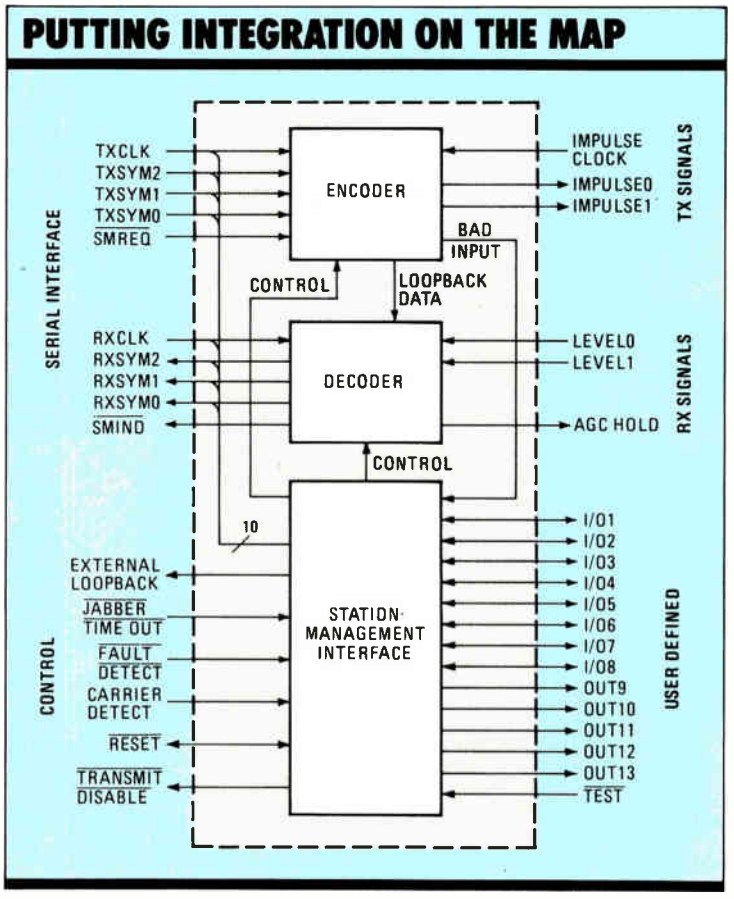
Nor will TI have to go it alone as the only other source of Token-Ring chips, other than IBM itself. As part of its overall networking strategy, Western Digital also plans to introduce a two-chip Token-Ring implementation late in the year. Ford says it will be capable of implementing a Token-Ring scheme at either 4 or 16 Mbits.

Meanwhile, Motorola remains the only supplier for MAP, once heralded as the wave of the future in U.S. factories because of its high 10-Mbit data rate and the use of a token bus architecture to insure reliability in the noisy environment. Undaunted, the Schaumberg, Ill., company has moved beyond its initial offering—the CMOS-based MC68824 media access controller—to include the MC68184, a broadband controller chip.

Introduced early this year, the BIC chip (see fig. 2) reduces the cost of a MAP broadband modem by combining the functions of 50 small-scale and medium-scale integrated circuits into a single chip, says Bob Franklin, protocol products marketing manager. It is designed to handle both data manipulation and management control for an external r-f transmitter and receiver. The MAP market has not expanded as fast as expected because it was an evolving standard until recently, Franklin says. "With the formalization of MAP 3.0 and a commitment by General Motors to keep the standard relatively stable for the next five years," he adds, "I expect to see MAP establish a position in the industrial market."

Going it alone with Arcnet is Standard Microsystems Corp., with a 2.5-Mbit/s baseband deterministic token-passing protocol developed by Datapoint Corp. in 1977. Since developing its first Arcnet controller chip in 1981, the company has introduced a wide array of board-level products for coaxial, twisted pair, and fiber-optic media. Standard Microsystems claims to have installed more than 500,000 Arcnet nodes all over the world.

In the PC LAN market in particular, SMC's Arcnet products now constitute 15% of the installed base and 25% of new installations, says Geof Karlin, director of marketing. He says he expects market penetration to continue unabated, especially with the introduction in December of the company's newest Arcnet chip set. The chip set includes the COM9026, a CMOS-based local-area network controller; the COM90C32, a CMOS-based LAN coax transceiver; the HYC9068 LAN driver; and the HYC9058 high-impedance transceiver, which allows system designers to use virtually any wiring, including twisted pair. With the development of the new chip family, the company expects to make significant inroads in the industrial and manufacturing environment, especially in combination with MAP. Also in development is a 5- to 6-Mbit next-generation version of its Arcnet chip set, scheduled for introduction next year.




**2. Integrating** 50 SSI and MSI circuits onto a single chip, Motorola's MC68184 chip greatly cuts the cost of a MAP modem.

Waiting in the wings for the next round—when customers begin looking beyond the current 10 to 16 Mbits of present LAN technology—is the 100-Mbit/s FDDI protocol. Currently only one company, AMD, has made a significant commitment. Its Supernet chip set includes three CMOS devices: the Am79C81 RAM buffer controller, the Am79C82 data path controller and Am79C83 fiber-optic-ring media-access controller; and two bipolar circuits, the Am7984 receiver and Am7985 transmitter.

Most other companies—such as National, TI, and Intel—have put FDDI on the back burner, especially as the market for copper-based coax and twisted wire LANs continues to grow. National's Nelson says the growth of FDDI depends on the media. National is hedging its bets too, though, by having two FDDI chip sets in development. "Optical fiber is just now being considered as a LAN media alternative, but only in applications where the higher cost of the media is not a factor," Nelson says. "When the cost of the media comes down and becomes more widespread, we expect FDDI to take off very quickly." *–Bernard C. Cole*

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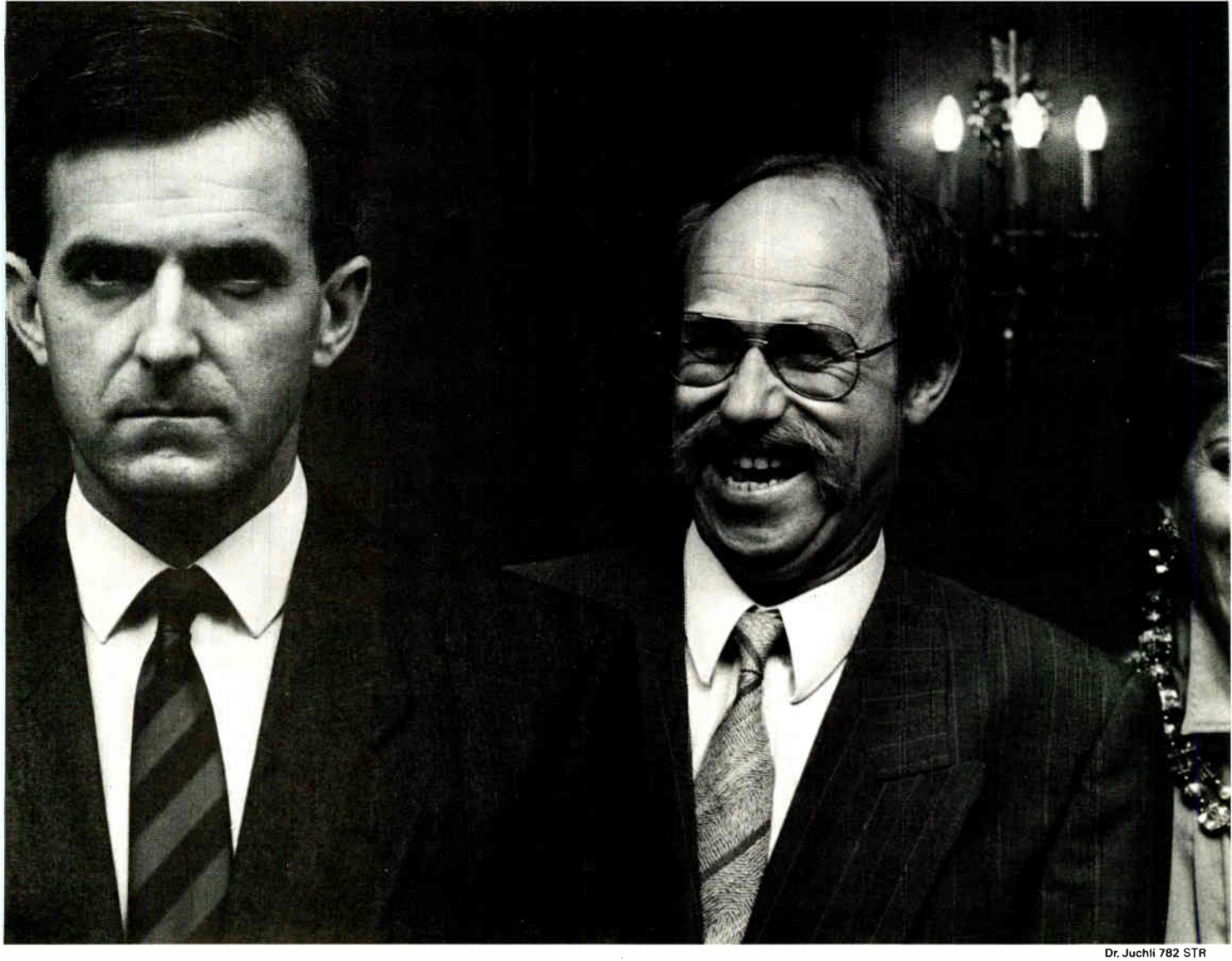

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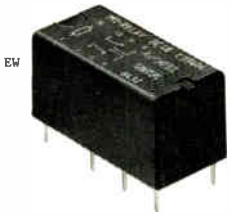


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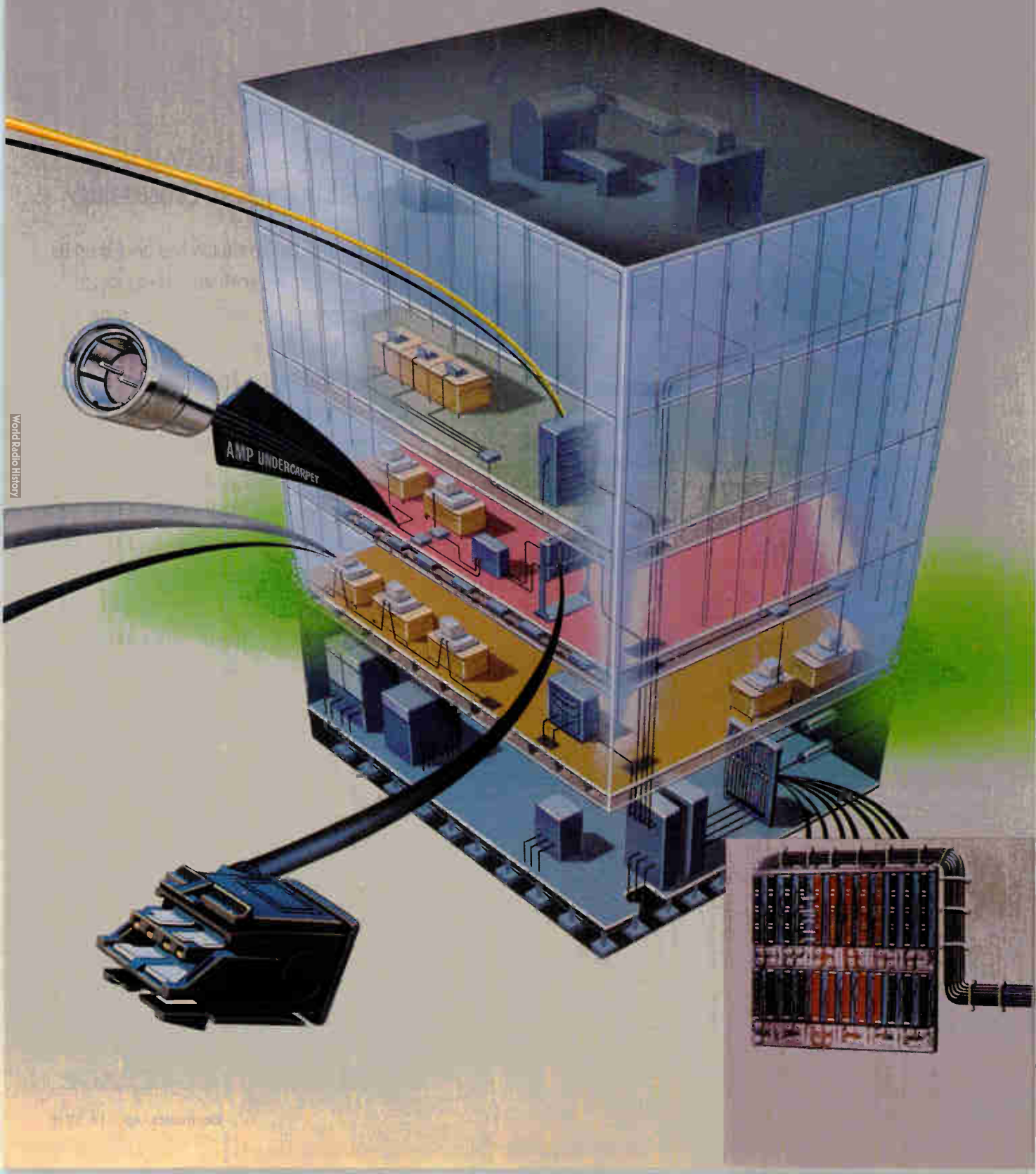
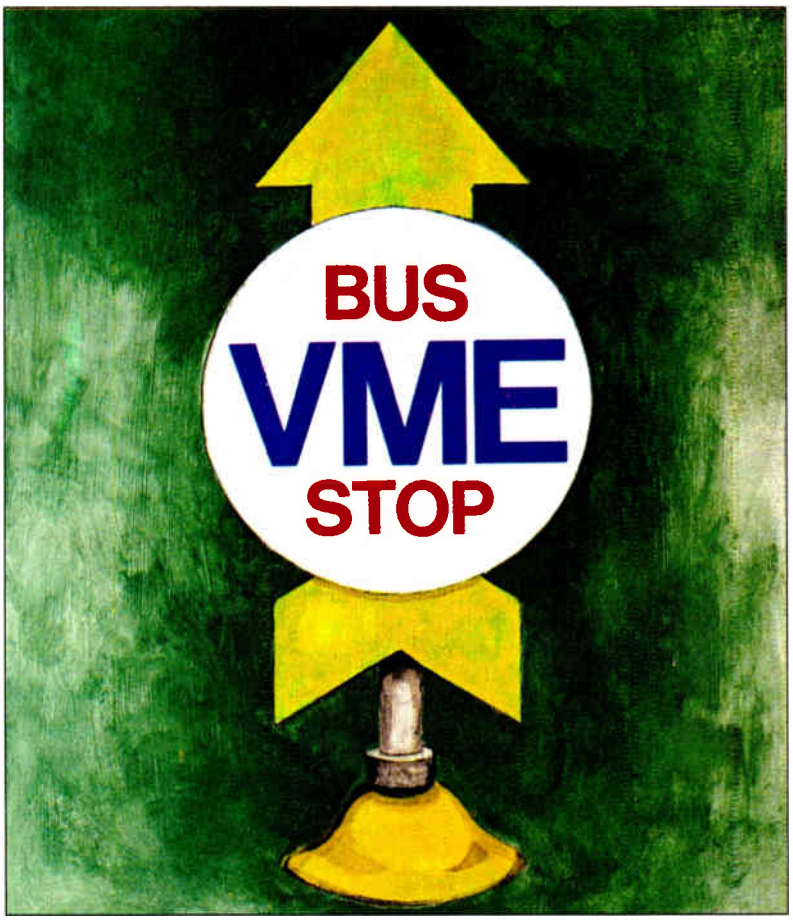


# BUS DRIVER.




*By combining basic functions in different arrangements, the board set provides a wide variety of real-time image-processing functions.*

## Matrox Offers Low-Cost Way To VMEbus Image Processing.

"A Canadian company has beefed up its graphics board set without adding much fat to its price, by combining real-time image processing with hardware-generated graphics. The MVP-VME from Matrox Electronic Systems Ltd. provides an easy way for VMEbus systems designers to include both image processing and high-end graphics capabilities in their designs. The two-board set, however, costs $6,000, just one half to one quarter of the price of competing systems.

The MVP-VME is the Dorval, Quebec, firm's second image-processing and graphics-combination board product. The first brought real-time image processing and graphics to the IBM PC AT..."

*Excerpted from an exclusive article in the May 14, 1987 issue.*

**Electronics**

**THE LEADER IN NEW TECHNOLOGY COVERAGE**

# MAPCON TAKES ON FACTORY NETWORK CONFIGURATION

## Industrial Technology Institute's tool uses AI to lay out networks that meet MAP 3.0 standards

If the Manufacturing Automation Protocol is ever to catch on as a mainline factory-networking scheme, users will not only need MAP products—they will also need tools that can help them with the complex task of MAP-network system integration and operation. That's the rationale behind MAPcon, an expert-system network configurator from the Industrial Technology Institute in Ann Arbor, Mich., for use with the forthcoming version 3.0 of the MAP specification. The final version of MAP 3.0 is expected to be released this summer.

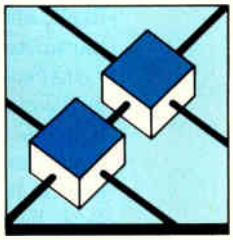
A tool like MAPcon will be a virtual necessity for MAP-network designers. Products that are built to the full seven-layer MAP 3.0 specification will typically require users to specify 62 separate parameters for each station on the network in order to link that station to a MAP network. "Some of these parameters are hard to set. Some of them are pretty trivial," says Andrew H. McMillan, director of the Institute's Communications and Distributed Systems Laboratory. "But nonetheless, the sheer magnitude of the task is not trivial. And when you multiply [62] by a few hundred nodes, you've got quite a task."

That's where MAPcon comes in. It queries the user on about a half-dozen key parameter settings for each network station. Then it graphically constructs the remaining parameter settings. Alternatively, if a particular set of devices cannot be configured together, MAPcon alerts the user and suggests alternatives [*Electronics*, March 31, 1988, p. 22].

The MAPcon package features an icon-based user interface and is implemented in Knowledge-Craft, an integrated set of software tools from Carnegie Group Inc., Pittsburgh, for rapid construction of knowledge-based systems. It currently runs on a Texas Instruments Inc. Explorer Lisp Machine. By next month, the package will be adapted for use on Sun work stations. Eventually, it will be joined by an entire suite of MAP network-management tools that are now in the works at the Institute. All of the tools will ultimately be spun out as commercial products. Although the Institute is a not-for-profit corporation, it plans to enter partnerships with vendors who will develop the tools into products. But the Institute also plans to provide early availability of prototype versions of MAPcon and other tools through a low-cost industrial-partnership program that begins in June.

In operation, MAPcon will run as a plug-in module to a network-manager platform, a software package that is now being developed at the Institute. It will address the first of three categories of network management covered under MAP 3.0—configuration management, fault management, and performance management. Knowledge-based modules handling the latter two categories will come later. Like MAPcon, they will also run on the network-manager platform, eventually providing a totally integrated, intelligent, control environment for MAP 3.0 networks. (The tools will also work for version 3.0 of MAP's sister protocol for the office, the Technical Office Protocol.)

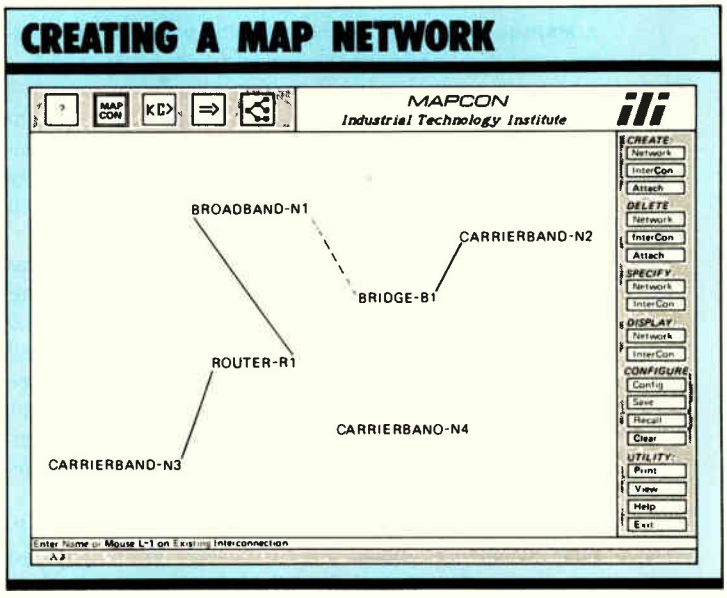
Featuring integrated use of screen graphics, pop-up windows, menus, and a mouse, in addition to help keys on a standard keyboard, the MAPcon interface is flexible enough for use by either novices or seasoned network engineers. Users can switch back and forth among applications by clicking the mouse over the appropriate icon.



The MAPcon user starts by creating stations and organizing them into a proposed network topology using the system's graphics capability (see fig. 1). MAPcon supports both broadband and carrier-band systems, and can also handle multiple topologies incorporating subnetworks connected by bridges, routers, and gateways.

Once a topology is created or, with an existing network, modified, the user supplies key parameters for each functional component and other connections to the proposed network. He then invokes MAPcon's configuration function, causing the system to generate the remaining parameters. If problems within the proposed configuration exist, MAPcon alerts the user to them. Or, if some key parameters are still needed to complete the configuration, MAPcon will ask for what it needs (see fig. 2). The user then enters the additional necessary parameters or makes configuration modifications as needed, and again invokes the configuration function. This process is repeated until MAPcon signals a successful network configuration.

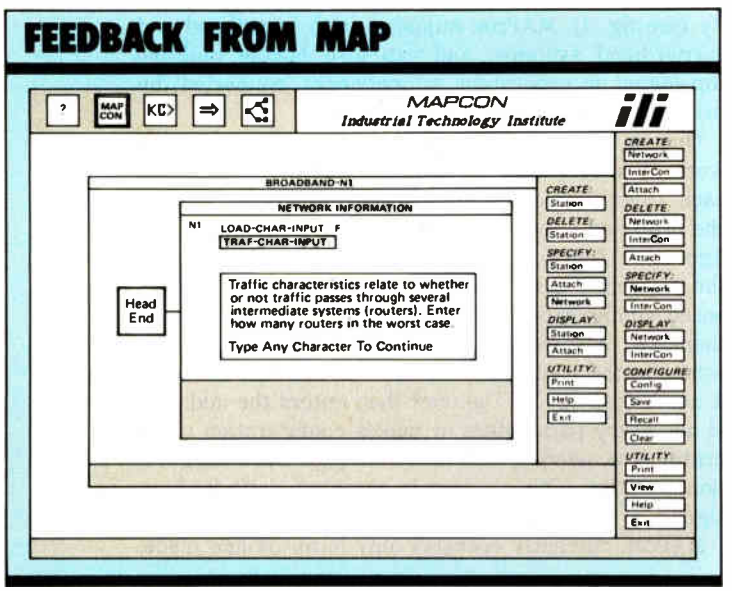
MAPcon currently operates only in an off-line mode,




**1. MAPcon allows users** to create stations and organize them into proposed topologies, using a graphics-oriented interface.

providing the user with a listing of parameter values that then must be physically set on the factory floor. Since MAP networks will typically link equipment supplied by a variety of vendors, this means that users will be required to deal with a number of different interfaces during physical parameter loading. But within six months, the Institute plans to convert MAPcon to an on-line system attaching directly to a MAP 3.0 network. For MAP networks that are already running, this will allow configuration parameters to be directly downloaded to new nodes over the network itself, eliminating the chore of physically entering the parameters.

MAPcon will not only speed up and simplify the MAPcon 3.0 network-configuration task; it will also help users head off incompatibility problems among equipment supplied by multiple vendors. As MAP 3.0 enters the real world, such problems will crop up, MAP backers concede, despite the fact that such incompatibilities among varying vendors' equipment is the very thing that MAP aims to eliminate. One potential trouble spot comes in layers 1 and 2 of the seven-layer Open Systems Interconnect model developed by the International Standards Organization, upon which MAP is based.




**2. MAPcon alerts users** to problems within proposed configurations and, if key information is missing, asks for what it needs.

Those layers include what is known as the media-access-control slot timer, a key parameter affecting overall network timing. For layer 1, "the [MAP] 3.0 specification calls out the IEEE-802.4 standard, and the standard says the slot time can be set anywhere within a certain range," says McMillan. Equipment from some MAP equipment vendors allows for a variable slot timer, McMillan says, but other manufacturers fix the slot-timer value in their hardware.

That opens the potential for incompatibility. MAPcon, however, "allows you to specify an anticipated network in theoretical form before you actually buy any equipment or put anything in place," says H. Van Dyke Parunak, manager of the Institute's Communications and Distributed Systems Laboratory. "It allows you to enter the kind of constraints that individual manufacturers' boxes would have, and saves you the embarrassment of buying a box, only to discover after the fact that there's no way you can make it run with something else you bought."

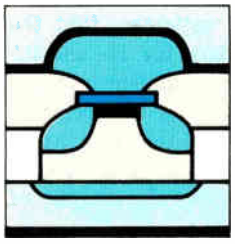
MAPcon, under development for about two years, is the first of several knowledge-based modules for use with MAP 3.0 networks. All are planned to attach to the Institute's network-manager platform. Unlike the modules, the network manager will not employ artificial intelligence. But it will provide users with analysis tools for performing configuration, fault, and performance management based on human direction. The MAPcon module will automate the configuration portion of the network management task and subsequent AI-based modules will automate other portions.

A prototype version of the network manager—with an attached MAPcon module—will go into beta tests at an unnamed industrial site in November, McMillan says. The Institute is currently talking with several potential industrial partners about converting the prototype network manager into product form, and is also looking for partners to commercialize MAPcon.

The network manager will be available as a commercial product from at least one vendor by this year's fourth quarter, or next year's first quarter, McMillan predicts. MAPcon itself will come later, he says, followed by a second knowledge-based module, called MAPfam, which will automate the fault-management portion of the task. The Institute's plan calls for a working MAPfam prototype by March 1989, McMillan says. Formal work has not yet begun on a third AI module to automate performance management, he says.

McMillan declines to make a prediction as to when MAPcon will become commercially available. "Because it's an expert system, the more expertise you build into it, the better it gets, and it's hard to say when it will be good enough to put out there and say, 'Use this tool and make your networks depend on it'," he says. The beta site testing that begins in November will provide information on how well MAPcon meets real industrial requirements, he says.

Industrial users who want early access to the prototype version of MAPcon can get it, though. Development of MAPcon was sponsored under an Industrial Technology Institute partnership program known as GAINS, for Group for Advanced Implementation of Networked Systems. The members of GAINS now are General Motors, Eastman Kodak, and Siemens, who already have access to MAPcon. In June, the Institute plans to announce a new GAINS structure by which new members can join for less than $1,000, says Stephen W. Schweer, the Institute's GAINS program manager. These memberships will include the right to purchase MAPcon and other prototype tools developed under GAINS. That prototype MAPcon purchase price for new members has not yet been set, but is expected to be between $4,000 and $5,000. The network-manager platform, though it was not developed under GAINS, will also be made available to new members, Schweer says. *–Wesley R. Iversen*



# INTEL'S AMBITIOUS GAME PLAN IN EMBEDDED CHIPS

The chip maker is embracing both RISC and flash EEPROM technologies as part of its strategy to grab a bigger market share in the high-end embedded-controller arena; it's also scaling down the 80386 for general-purpose-system designers

by Bernard C. Cole

After months of industry speculation and rumor, Intel Corp. has dropped the shoe—three shoes in fact. The chip maker is revealing its strategic response to the burgeoning market for embedded controllers, the rapidly increasing popularity of reduced-instruction-set computer processors, and the growth of flash nonvolatile reprogrammable memory technology. Now Intel plans to expand its role in the embedded-control marketplace by introducing three product families that offer designers processors geared to application niches.

Several challenges faced the Santa Clara, Calif., chip maker. A wide range of new processor chips based on RISC architectures have hit the market. In high-end embedded control, the emergence of several processor alternatives are challenging Intel's technology lead. And in nonvolatile memory, competitors such as Seeq Technology Inc. and Toshiba Corp. have been working on a new technology called flash electrically erasable programmable read-only memory [*Electronics*, March 17, 1988, p. 149].

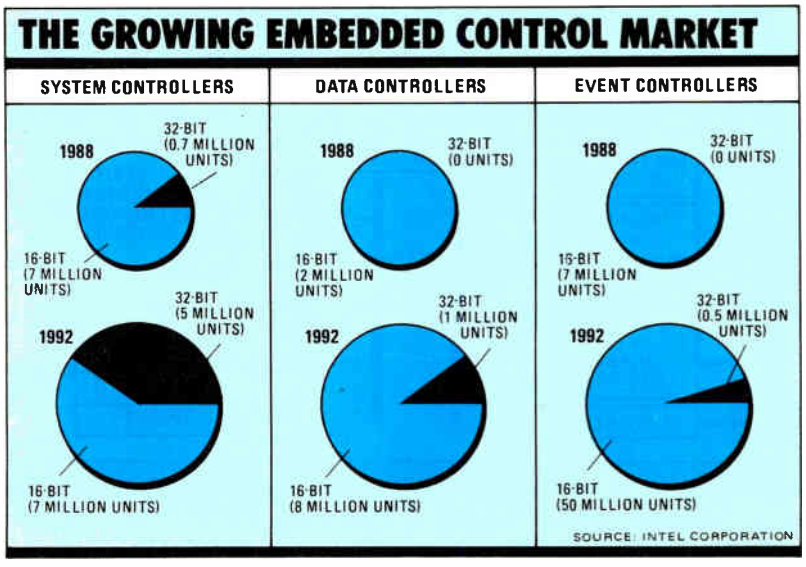
In response, Intel is introducing the 80376 family (see fig. 1a) to expand its position in a still-growing market for embedded controllers based upon general-purpose processors such as its 16-bit 80186 and 80286, as well as the 32-bit 80386. A scaled-down version of the 80386 central processing unit, the 80376 is paired with a new multifunction peripheral circuit, the 82370 (see fig. 1b), which itself is a derivative of a similar device, the 82380, used with the 80386.

The two devices in the 80376/82370 family are designed to serve an existing market that accounts for practically all of Intel's more than 2,000 design wins with the 80186, says Bill Rash, product marketing manager for Intel's microprocessor division in Santa Clara, Calif. About 20% to 30% of the general-purpose 80286 and 80386 have reached the same users. In the 80376, the user gets the same instruction set and internal architecture as he does with the 32-bit 80386. In addition, the user obtains the same 2.5- to 3-million-instruction/s performance. What has been eliminated internally are the programming modes not needed in embedded applications, Rash says.

The second product offering, the 80960 family of RISC-like 32-bit embedded processors, includes three devices that perform up to 7.5 mips and feature a burst rate of 20 mips at a 20-MHz clock rate. The 80960 family is designed to be the high-end follow-up to the company's 8- and 16-bit embedded microcontrollers.

In the 80960 series, Intel is attempting to meld elements of RISC architecture, application-specific designs, and its know-how as a major supplier of single-chip microcontrollers. The family's first devices include the 20-MHz 80960KA and 80960KB (see fig. 2) and the 80960MC. In addition to RISC design features, 80960KA and 80960KB use an instruction mix that also reflects the requirements of embedded-processing applications, says Vinod Mahendroo, director of marketing at Intel's microcomputer division in Chandler, Ariz..

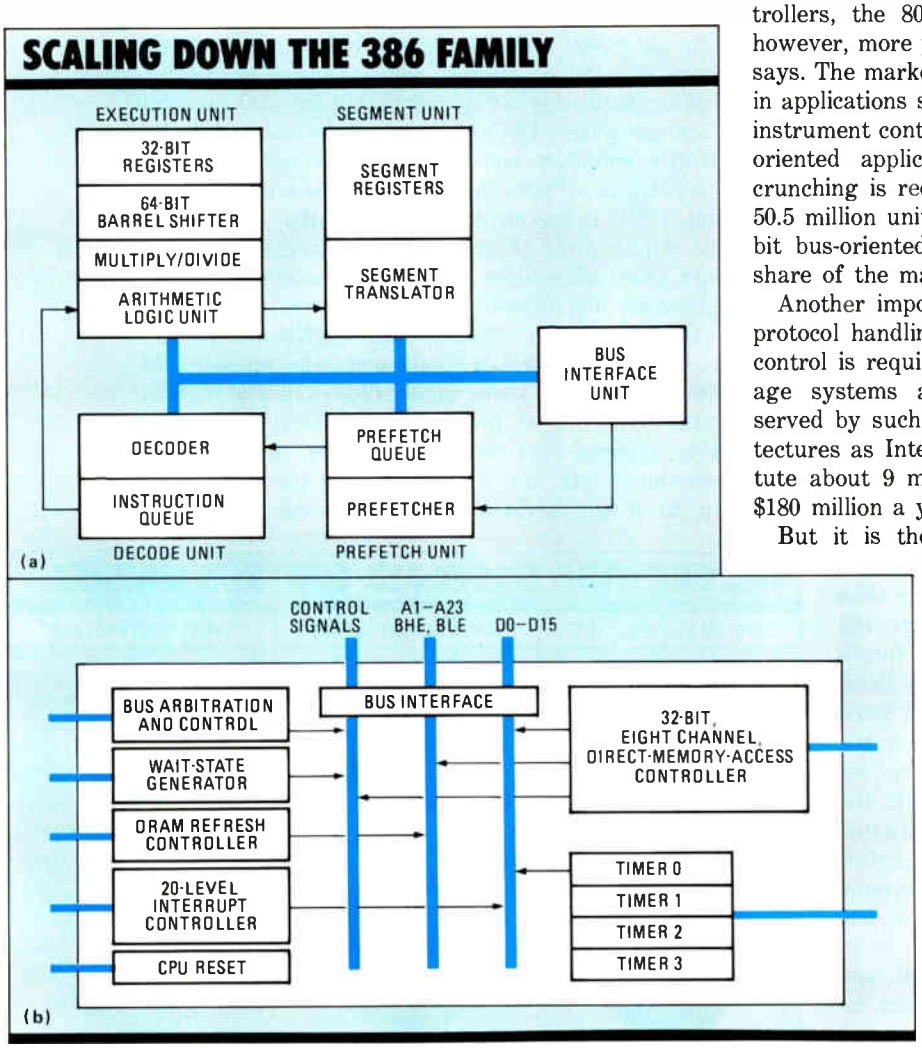
Unusual for a RISC chip, the 80960KB incorporates an on-chip 32-bit floating-point unit. Also on-board the 80960KB is a 512-byte instruction cache, a register cache consisting of four sets of 16 local registers, a 32-bit internal data bus, a proprietary 32-bit external local burst bus, and a 32-bit address bus that allows up to 4 gigabytes of linear address space. The



80960MC also has an on-chip 32-bit floating-point unit. In addition, the 8096MC incorporates features such as virtual-memory management and support for multiprocessor systems that Intel says will be useful in many military embedded-control applications.

Devices to follow the 80960KB will extend both upward to higher speeds and possibly wide word sizes as well as downward into applications areas now served by Intel's existing microcontroller families, Mahendroo says. In addition, the follow-ups will diversify with a proliferation of application- and user-specific processors.

The third part of the plan is Intel's new flash EEPROM family, which includes a 28-pin 8-K-by-8-bit device, the 57F64, as well as two 32-K-by-8-bit devices: the 32-pin 27F256 and the 28-pin 28F256. They are the glue to Intel's embedded strategy. The new family of flash EEPROMs was designed to offer low-cost, in-system, alterable-code capability for storing the large programs required by many advanced embedded applications. In embedded applications such as graphics, robotics, and real-time processing, the devices will aid rapid prototyping and updates in the field, says Bruce McCormick, flash EEPROM marketing manager at Intel's memory operation in Folsom, Calif. Like the other two product groups, the flash EEPROMs are fabricated using the company's 1.5 μm CHMOS IIe process.




**1. Intel's new 80376** processor (a) and its associated 82370 multifunction peripheral device (b) combine an internal 32-bit architecture with an external 16-bit address bus.

Intel's thrust into the embedded-controller arena is not happenstance—the company thinks the market is set to take off. Based on market numbers from Dataquest Inc., San Jose, Calif., Intel estimates that the overall embedded-control marketplace for 16- and 32-bit processors will grow to almost 72 million units by 1992. In dollars, sales of 32-bit embedded processors, which constitute about one-fourth of the total 32-bit market, which will grow to $740 million by 1992, says Dave House, vice president and general manager of the microcomputer components group.

The embedded-processor marketplace is more diverse and niche-oriented than the relatively monolithic general-purpose programmable-CPU marketplace, which requires commonality of architecture, instruction set, and software compatibility, House says. The embedded-control market breaks out into three specific segments, each of which has its own subsets of performance, architectural, and instruction-set requirements. House says the three segments are event control, data control, and systems control (see chart, p. 97).

In event control, House says, most of the market needs are now served by Intel's 8- and 16-bit microcontrollers, the 8051 and 8096 architectures. By 1992, however, more powerful solutions will be required, he says. The market for such high-end processors will be in applications such as motor, engine and machine, or instrument control. Intel estimates that in such event-oriented applications, where considerable number-crunching is required, the total market will be about 50.5 million units a year, about $200 million, with 16-bit bus-oriented architectures constituting the lion's share of the market.

Another important segment is data control, where protocol handling, data formatting, and input/output control is required in applications such as mass storage systems and graphics-oriented systems. Now served by such general-purpose programmable architectures as Intel's 80186, this subsegment will constitute about 9 million units a year by 1992, or about $180 million a year.

But it is the third category—system controllers, aimed at applications like image processing, robotics, process control, and telecommunications—that will have the largest dollar volume, Intel says. Although unit shipments of 7 million a year is less than the other two categories, annual sales of almost $370 million are projected, approaching that of the other two categories combined.

Anticipating that the embedded-control market will grow significantly, Intel has developed a three-pronged attack. The 80376/370 processor combination has particular advantages for designers of embedded systems who are cost/performance-conscious. Cost reduction comes from two sources, Rash says.

At prices of $99 and $57 each in 100-piece quantities, he says, the 80376/370 combination is considerably cheaper than other embedded alternatives of equivalent performance, because it takes advantage of the economies of scale already achieved with the current 386/380 combination. With sample quantities expected in June, the 80376/370 combination will be in production by the end of the year. Both 100-lead fine-pitch gull-wing packages for surface mounting as well as 88-pin grid arrays, where hermeticity is required, will be available.

In addition, because it is essentially a subset of the full 32-bit configuration, the 80376 has access to virtually all of the software-development tools and compilers used in the 386. Most industry standard real-time operating systems will also be available for it to run on. Even now, existing 386 real-time operating systems can be run with minor changes.

## A NARROWED APPROACH

As a scaled-down version of the 32-bit 80386 CPU unit, the 80376 also offers a narrowed approach. "The 386 in essence was given a split personality, with a protected mode designed for Unix-oriented full 32-bit applications, and three modes—the real mode, the 80286 mode, and the virtual 8086 mode—for PC-oriented systems," Rash says. In the 80376, only the 386 protected mode has been retained, considerably simplifying programming. Taking into account the requirements of many embedded applications, the external data bus also has been scaled down to 16 bits rather than 32 bits, and the address bus also is pared, from 32 to 24 bits. The reduction results in a total address space of only 16 Mbytes rather than four gigabytes.

To match it to the architecture of the 376, the 80370 multipurpose peripheral retains all of the 80386's features, except for a 16-bit data bus and a 24-bit address bus. The number of direct-memory-access channels and interrupts available to the designer now using the 80186 is increased by four times. This is accomplished by incorporating the functions of eight DMA channels, three interrupt controllers, four 16-bit programmable interval timers, a wait-state generator, and bus-control logic.

In the 80960 series, which includes the 20-MHz 80960KA and 80960KB and the military-oriented 80960MC, Intel is offering system designers a mix of RISC architecture and application-specific designs geared to the embedded control marketplace (see fig. 3).

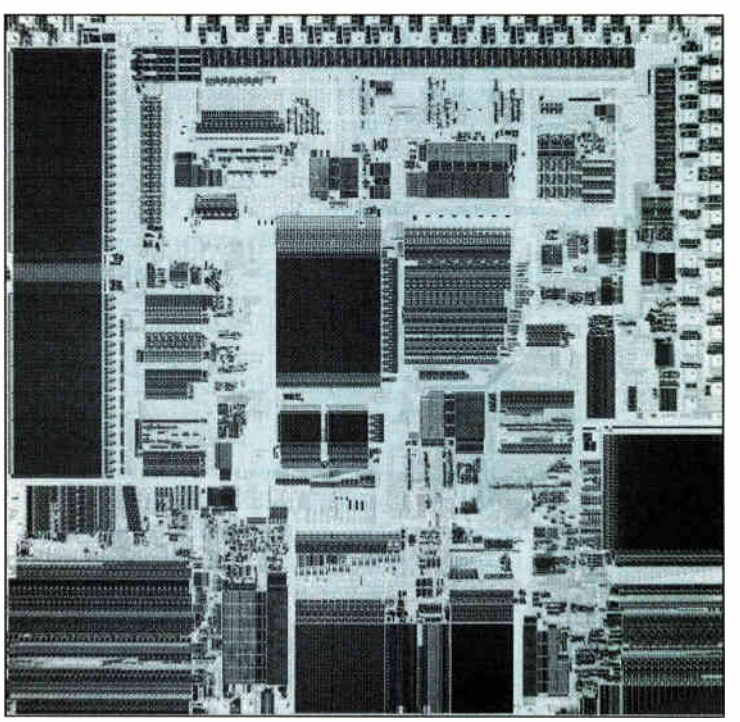
In adapting RISC, Intel has followed its own ideas about how the technology should be used. "RISC is not a set of architectural edicts that must be followed blindly," says Mahendroo, of the microcomputer division. "Rather, it is a set of techniques and principles to be applied where appropriate, when designing a processor, to achieve higher speed." What must also be factored into the equation, he says, are factors such as cost, application specificity, and ease of use and programming.

Using the 80960 family as the starting point, Mahendroo says, Intel expects to generate a variety of standard product offerings with the same basic instruction set but with features that optimize them for particular market segments. Also in the works are a series of application-specific standard processors. Whereas the standard processors are market-segment-driven, the ASSPs are application-driven, with instruction sets and features targeted to specific applications. "The advantage of this second approach is that for the same process and architecture you can get a higher performance than a comparable RISC design," Mahendroo says. Ultimately, the 80960 will be incorporated as a core-processor macrocell into Intel's standard-cell library, allowing customers to develop their own user specific processors, he adds.

The 80960 series is available now in sample quantities. The 80960KB in a 132-pin leadless pin grid array is $390 each in 100-lot quantities. The 80960A, which will be available in the fourth quarter of 1988, will be $230 each. Twenty-five MHz versions will be available in the first quarter of 1989. Military-temperature versions of the 80960MC will be available in the third quarter for $2400 each in 100-unit quantities. Fully qualified STD 88C versions will follow in the fourth quarter.

The 80960 architecture has many RISC-like characteristics as well as many advantages over complex-instruction-set computers: it operates at higher clock rates, has a reduced number of cycles per instruction, uses deeper pipelines and parallel instruction-execution techniques, and contains more registers and on-chip register and instruction caches. Where it differs, Mahendroo says, is in the use of an instruction mix that reflects as much the requirements of embedded-processing applications as it does traditional RISC machines.

An example of Intel's reluctance to follow RISC dictates is its decision to use a floating-point unit on board the 80960KB and 80960MC, Mahendroo says. "When you look at the broad range of applications for embedded processors, you will find a significant percentage require some sort of advanced floating-point capability."



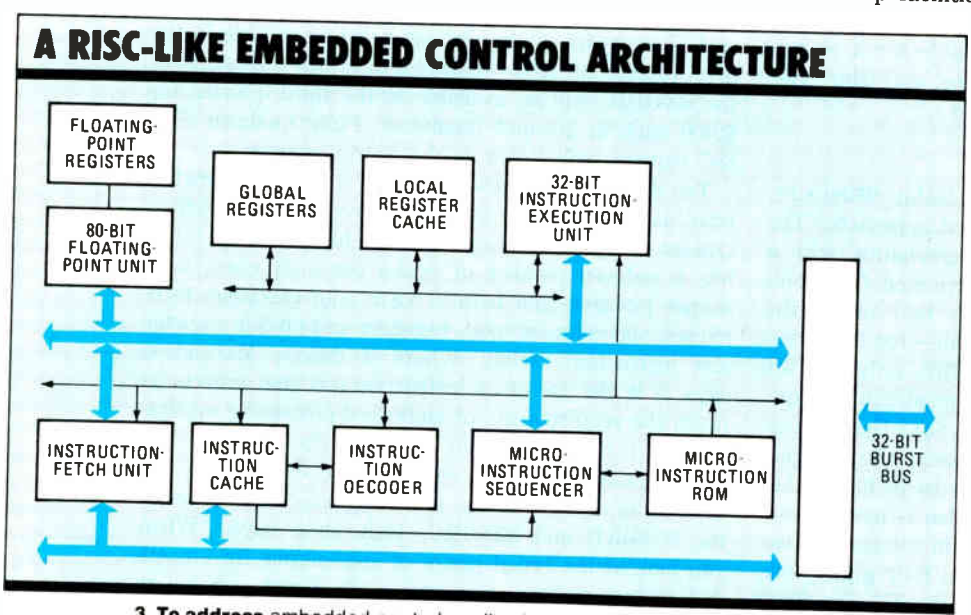
**2. Intel's new 80960** RISC-like 32-bit embedded processor packs 350,000 transistors into a 390×390-mil die using its new 1.5-$\mu$m CHMOS-IIe process.

The processor provides support for both mandatory and recommended portions of the IEEE 754 standard for floating-point arithmetic, exponential, logarithmic, and other transcendental functions.

The 8096MC's on-chip virtual-memory management facilities include support for demand-paged memory with a two-level protection scheme as well as page swapping and on-chip translation look-aside buffer circuitry. To support multiprocessor systems, the 9060MC also incorporates such features as external message passing, to allow preemption of activities running on other processors, and high-level process management, to handle scheduling and dispatching.

Even in its RISC-like features, the 80960 improvises to net performance gains. As with most RISC machines, the 80960 architecture uses load and store instructions to access memory. In addition, however, the architecture uses a simplified instruction format to ease hardwired decoding of instructions. Specifically, the instructions are word aligned, so that all instructions are one word long, except for one class that uses the subsequent word as a 32-bit displacement.

The 80960 has a core of 51 instructions out of 184 that are designed to be executed in a single clock cycle, Mahendroo says. But unlike other RISC machines, the 80960KB also supports a number of important multicycle instructions, such as 32-bit multiply and divide instructions. Integration of such operations on-chip eliminates much software overhead and the negative effects of code density. To further optimize performance, the 80960 overlaps instruction execution, making use of special on-board logic for write buffering and register scoreboarding. Write buffering allows a write instruction to proceed as soon as it is placed in the buffer, rather than waiting for the actual write operation to occur on the bus. Similarly, register scoreboarding allows the processor to continue execution of instructions when it encounters a load instruction, reducing the effect of slow memory speed.




**3. To address** embedded-control applications requiring 32-bit functionality, Intel's 80960 combines RISC-like features with an on-chip floating-point unit.

To support operation in a 20-mips burst mode at 20 MHz, the 80960 incorporates a proprietary wideband local bus (L-BUS) which consists of a 32-bit multiplexed address/data path and control signals for data transactions. Because of the large amount of on-board caching, the L-bus supports up to four successive data words, with one word transferred every clock cycle. Transactions on the L-bus can use 8-, 16-, or 32-bit data types and address up to four gigabytes of physical memory.

Also unusual in a RISC machine is the 80960's sophisticated interrupt controller, similar in concept to techniques used in Intel's low-end 8- and 16-bit microcontrollers. The technique allows the 960 to use either the on-chip facilities, an external interrupt controller, or both, with the type of structure specified by an internal interrupt vector register. And for systems with multiple processors, the 80960KB provides a fourth method, called interagent communication, where the processor can interrupt another one by sending an IAC signal.

Not to be underestimated in Intel's overall strategy is the third product group—the new flash EEPROM family (see p. 103)—which links these diverse processor efforts into an integrated whole. This integration is obtained by giving the user a nonvolatile memory of sufficient density to incorporate the large amounts of code necessary for many complex embedded applications and by allowing in-system programming without removing the circuitry.

By combining the hot-electron write feature of EPROMs with the cold-electron erasability of full-featured EEPROMs [*Electronics*, March 3, 1988, p. 47], the 64-Kbit 57F64 and 256-Kbit 27F256 and 28F256 flash EEPROMs will revolutionize embedded-control system design, says Bruce McCormick, flash EEPROM marketing manager at Intel's memory operation in Folsom, Calif. "What is needed is a low-cost, in-system, alterable-code capability for rapid prototyping, and updates in the field," he says. In most embedded applications using ultraviolet-erasable PROM, this can be done only by removing the board and replacing the memory, a difficult task in many applications. EEPROM is an alternative only in less price-sensitive designs and where a large amount of program memory is involved, McCormick says. Because it incorporates a single transistor cell, similar to an EPROM, the flash EEPROM will track EPROM densities very closely.

McCormick says the flash EEPROMs will allow new programming approaches that were either too cumbersome for EPROM or too expensive for EEPROM. Applications would include telephone line transfers of new code, the use of local-area networks to provide code updates and the use of floppy disks to download new code to embedded peripheral controllers. □

# MILITARY/AEROSPACE NEWSLETTER

## SHOULD THE U. S. LIMIT FOREIGN OWNERSHIP OF DEFENSE CONTRACTORS?

The U. S. may be leaving itself vulnerable to dependence on foreign companies for key defense technology, posing the threat of a major breach in national security, defense analysts worry. Alan Benasuli, a managing director and defense-industry specialist at Drexel Burnham Lambert, New York, says Congress should protect U. S. defense companies from foreign takeover by limiting the extent of foreign ownership. "We should slap a limit on foreign acquisitions of defense companies, like the 20% limit the British have," he says. "In defense electronics alone, we have seen six acquisitions by foreign firms, primarily British companies." Benasuli says that without government intervention, such as the pressure used a year ago to get Fujitsu Ltd. to drop its bid for Fairchild Semiconductor Corp., foreigners will continue to buy into the U. S. industry. Electronics firms are particularly vulnerable, he says, because of the high cost of research and development. "They need parents with deep pockets," he says. Moreover, big defense contractors will "need a defense electronics capability in order to compete in the future." □

## PLESSEY GETS A BIG INCENTIVE TO SAVE MONEY

The British Army is trying to save money with a new contracting scheme as it aims to upgrade its Ptarmigan battlefield communications system. The prime Ptarmigan contractor, Plessey Defence Systems Ltd. of Hampshire, UK, has won the UK's first incentive-driven contract—a deal that offers Plessey financial rewards for bringing the job in under budget. If Plessey completes the contract below the $160 million price ceiling, the company and the Army will split the savings evenly. The deal calls for Plessey to add high-integrity data communications to the battlefield system, develop an interface to allow it to tie into the communications networks of other North Atlantic Treaty Organization armies, and produce a version for armored vehicles. □

## MAGNETEK'S SHIP-BOARD POWER SYSTEM WON'T QUIT WHEN IT OVERLOADS

Today's Naval ships are much smaller and lighter than the battleships of World War II, and because they are not heavily armored, they depend far more on active electronic navigation and defense systems than ever. But when the power systems shut down, even momentarily, the ship becomes vulnerable, says Lawrence Schaffer, director of business development at Magnetek ALS Corp., Anaheim, Calif. The company's Fault Isolation Unit and a family of frequency converters called PACE, for Pulse-synthesized Advanced Conversion Equipment, together are 20% to 33% lighter than traditional ship-board power equipment and provide for 300% overload capacity. The systems can recover from 50% load changes in just 1.25 ms—twice as fast as traditional ship-board power systems. They are also reliable. The mean time between critical failures—those that actually take the system off-line—is 15,000 hours, or twice that in a dual power-train setup. □

## PENTAGON SETS DEFENSE MANUFACTURING BOARD TO SHARPEN U. S. COMPETITIVENESS

With an eye toward sharpening U. S. industrial competitiveness, the Defense Department is creating a Defense Manufacturing Board to help identify problems and offer solutions to build a more effective defense industry. "We must find new ways to help industry help itself," Robert B. Costello, undersecretary of defense for acquisition, told the House Subcommittee on Economic Stability at the end of March. The board will be made up of members from both defense and nondefense industries, Costello says, as well as from labor and academia. The new board is modeled on the Defense Science Board, which advises the Pentagon on current scientific issues. □

# MILITARY/AEROSPACE NEWSLETTER

## NOW THERE'S A FAST WAY TO PRODUCE CHEAP COCKPIT PROTOTYPES

Northrop Corp.'s Aircraft Division in Hawthorne, Calif., has developed a rapid prototyping tool for designing advanced airplane cockpits that it says allows it to produce cockpit prototypes for pilot testing 100 times faster and for 10% of the cost of current methods. The Reconfigurable Cockpit is based on custom software running on a pair of Silicon Graphics Inc. 3120 work stations and a custom-built close-focus high-resolution projector that displays an image of the cockpit for pilot testing. "We can reconfigure this thing in as little as 10 minutes and design from the ground up in less than a week," says Paul Pencikowski, manager of Crew Systems Integration and the designer and technical manager of the Reconfigurable Cockpit. "This tool allows you to get meaningful man-in-the-loop design data prior to baseline," he says, referring to the point, early in the development cycle of any aircraft or upgrade, when contractors must submit a final design proposal. "If you've got to build these things out of hardware, you can do two design iterations," Pencikowski says. "In that same 90- to 180-day period, I can do 200 designs easy." □

## MARINE CORPS PROCUREMENT IS IN A SHARP DECLINE

U.S. Marine Corps procurement spending, which tripled in the first year of the Reagan military buildup, has fallen hard ever since, and at the present rate of decline will reach the 1981 spending level by 1991, says Maj. Gen. Ray Franklin, commander of the Marines' Research, Development, and Acquisition Command in Washington. Franklin's 1989 budget proposal calls for about $1.15 billion in Marine Corps procurement, of which roughly one-third will be for stand-alone communications and electronics equipment. That's about $80 million less than the Marines will spend this year, and almost $300 million less than the $1.44 billion the Corps spent in 1987. Adjusting for inflation, the Marines have taken a 48% cut since 1983, when spending peaked at $2.4 billion in 1989 dollars, Franklin argues. He warned the House Subcommittee on Defense in March that "If future procurement budgets continue to decline, new starts will be almost nonexistent, and we will be faced with the block obsolescence and technological shortfalls that we encountered in the 1970s." It could happen. Joseph Campbell, a defense-industry analyst at PaineWebber Inc. in New York, says, "History shows the numbers [for defense spending] can get lower—a lot lower." The decline, he adds, could continue beyond 1991. □

## BOEING PUTS ITS TOUCH ON THE NAVY'S P-3 ANTISUBMARINE AIRCRAFT

Boeing Aerospace Co. is using touch-screen technology and a heavy complement of custom software to make the five terminals in Update IV of the Navy's P-3 Anti-Submarine Warfare system generic. P-3 is an airborne system that monitors submarine traffic with remote sonobuoys and other sensing equipment. In its present form, the system's five crew stations are each unique. That's caused problems in the past when one terminal went down, and vital data such as the P-3's imaging radar, infrared detection system, or acoustic input from sonobuoys was lost for the rest of the mission. But Boeing designed a high-bandwidth data bus so that each terminal can now access any data available on the aircraft. The touch panels—the first prototypes use IR touch panels, and later versions will also include a pressure-sensitive touch technology—replace the keyboards that earlier P-3s used, and can be used to quickly change any terminal to perform any function, says H. W. "Pete" Peterson, international product development manager for Air ASW Programs at the Seattle company. "With this system you don't have a whole lot of different display terminals," he says. "You've got one type of display, and it really cuts down on spare parts costs." □

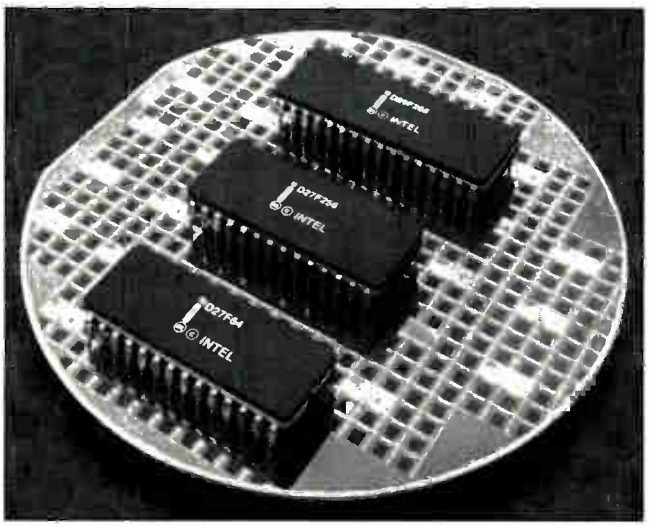
# NEW PRODUCTS

## INTEL'S FIRST FLASH EEPROMs MAKE IN-CIRCUIT REPROGRAMMING EASY

Targeting embedded-control applications, the 64- and 256-Kbit chips boast 150-ns access times

Intel Corp.'s first flash electrically erasable, programmable read-only memories boast access times as low as 150 ns and incorporate special circuitry to make reprogramming easier in embedded applications where physical access is difficult.

In addition to the conventional programming mode with an external PROM programmer, the 64-Kbit 57F64 provides an on-board mode that maintains supply voltage at 5 V. The chip-enable and output-enable signals are maintained at standard logic levels. As a result, devices socketed or soldered to circuit boards can be erased and programmed via an edge connector to a PROM programmer or board tester.




**Intel's 256-Kbit** flash EEPROMs have access times of 170 and 250 ns; the 64-Kbit device comes in 150- and 250-ns versions.

In the 256-Kbit devices—the 27F256 and the 28F256—new command-register circuits have been implemented that are directly compatible with the write interface of most microcontrollers. In this approach, a 12-V signal applied to the programming pin can access all functions associated with altering memory contents via the command register. Commands are written using standard microprocessor write timings.

**CONTROL.** As a group, flash devices target embedded control applications where the system central processing unit provides occasional code updates over the lifetime of the product. Intel's devices offer 100-cycle program-and-erase endurance rates. Reprogramming failure is less than 0.01%, says Richard Pashley, general manager of Intel's flash memory operation in Folsom, Calif. A device capable of 10,000 reprogramming cycles is under development.

By combining the hot-electron writability of ultraviolet erasable EPROMs and the tunnelled cold-electron erasability of traditional EEPROMs, flash devices deliver both high density and in-circuit electrical erasure and reprogramming [*Electronics*, March 3, 1988, p. 47]. Intel's method for providing these basic features is primarily its use of proprietary EPROM tunnel-oxide technology.

Intel's new chips are part of the Santa Clara, Calif., company's broad strategy to capture the embedded control marketplace (see p. 97).

To further enhance their use in embedded applications, the flash devices incorporate proprietary high-speed programming and erase algorithms. Using a new Quick-erase algorithm, the contents of the flash devices can typically be erased in less than 1 s, compared with the 10 to 20 min. required for UV erasability. Using the Quick-pulse programming algorithm, the devices reprogram in less than 4 s.

The fast erase/programming capability provides considerable time and cost savings to embedded control system manufacturers whose EPROM-based applications require the added flexibility, says Pashley. For example, some applications require a device that can update code or parameters, or accumulate data in-system.

Fabricated in the company's 1.5-μm CHMOS-IIE process, the 256-Kbit devices have access times of 170 and 250 ns; the 64-Kbit device has speeds of 150 and 250 ns. Those speeds eliminate wait states for most 8- and 16-bit microcontrollers, says Pashley.

The 256-Kbit devices cost $29.90 for the 170-ns version and $22.00 for the 250-ns version in 1,000-unit purchases. The 64-Kbit device costs $12.00 for 150-ns access and $10.00 for 250-ns speed. The 28F256 and 27F64 are available now in volume, while the 27F256 is available only in sample quantities. – *Bernard C. Cole*

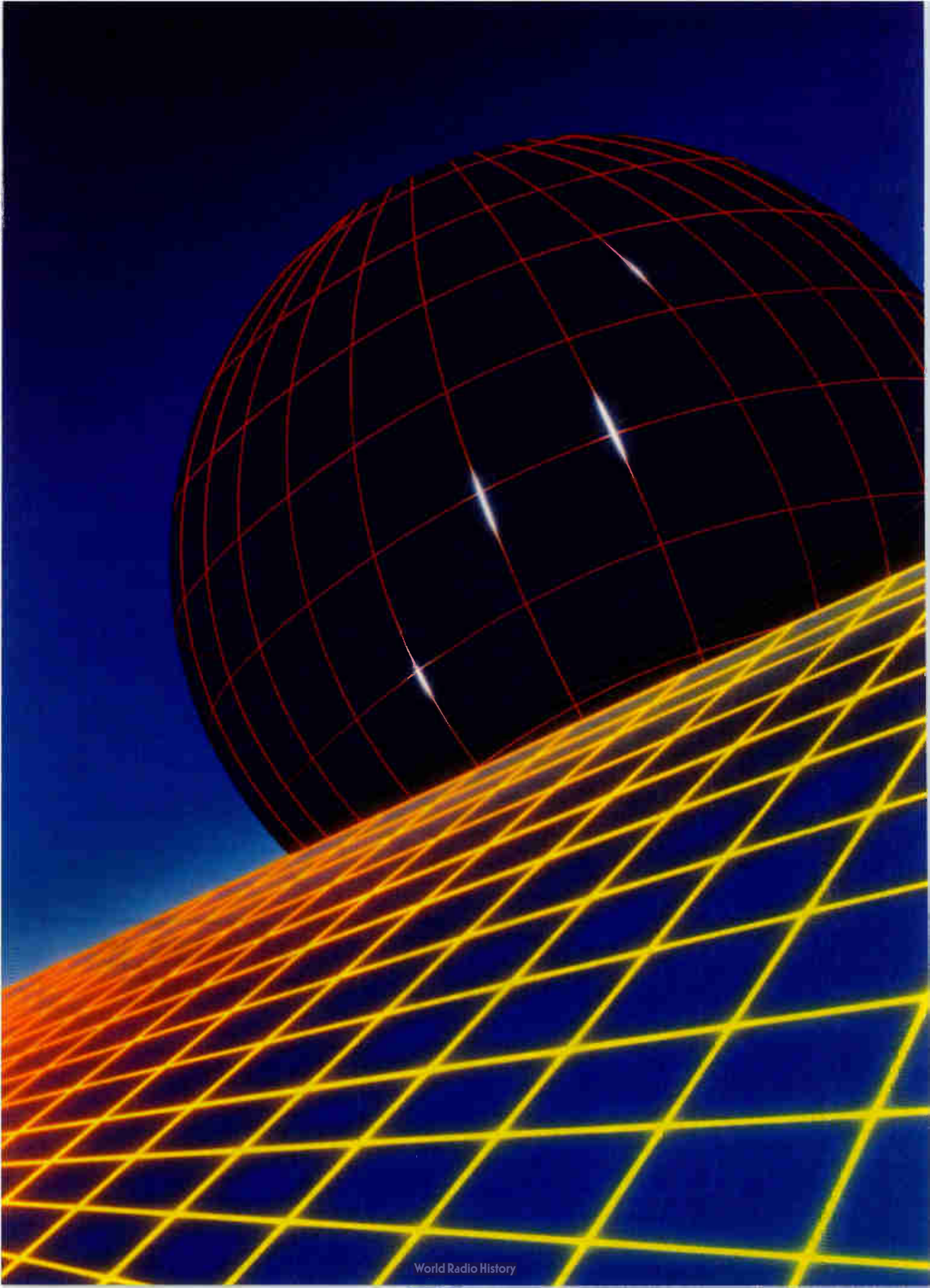
Intel Corp., Literature Department, W-424, 3065 Bowers Ave. Santa Clara, Calif., 95051.
Phone 800-548-4725 [Circle 360]

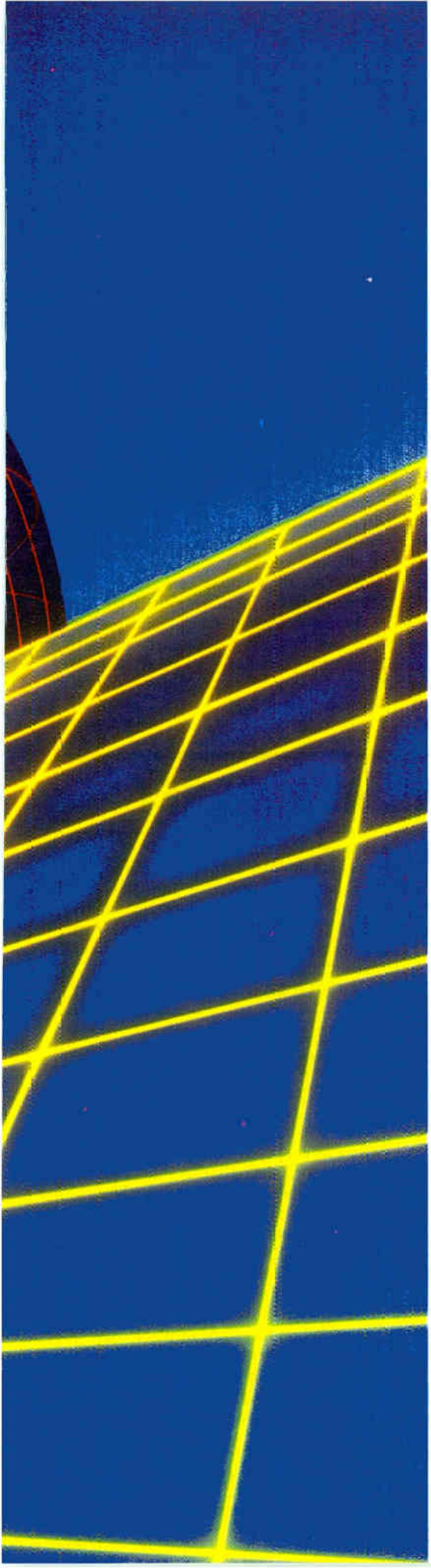
## CIRRUS DISK-CONTROLLER IC DOUBLES PC PERFORMANCE

Disk-memory subsystems for IBM Corp. Personal Computer ATs and compatibles can achieve a sustained 2-Mbyte/s data-transfer rate using Cirrus Logic Inc.'s CL-SH260 controller chip—that translates into a twofold boost in overall system performance compared with present solutions that need up to eight integrated circuits.

Fabricated in 2-μm CMOS, the new controller supercharges overall performance by integrating three major disk-controller functions—the PC, PC/XT, and PC AT interface, buffer manager, and formatter—onto a single chip. The chip can handle peak data rates up to 20 Mbits/s—fast enough to operate the system's read-and-write functions in a 1:1 interleaved mode instead of the more conventional 3:1 interleave mode.

Disk controllers with bit-transfer rates less than 20 Mbits/s cannot process information fast enough to read consecutive sectors on the disk because the disk is





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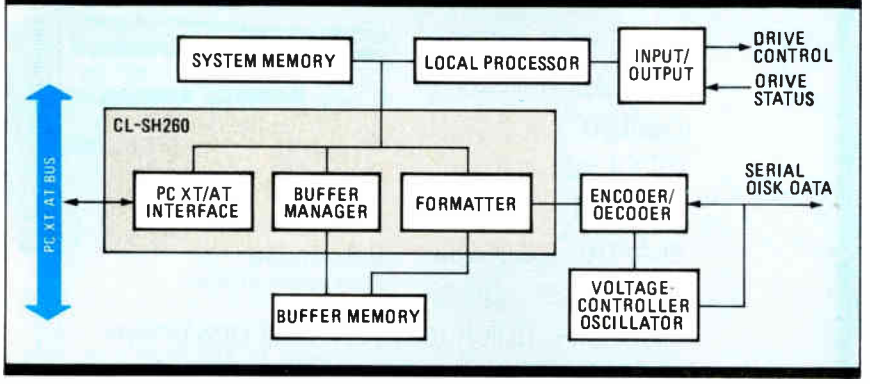
## FOLDING THREE ICs INTO ONE




**The CL-SH260** combines three major controller functions, attains speeds of 4 Mbytes/s on its host bus, and features automatic wait-state generation for compatibility with host processors.

rotating too fast for them to react, says Cirrus President Michael Hackworth. Consequently, they must read every third sector and wait for subsequent revolutions to access the other consecutive sectors. Until the arrival of the SH260, only high-end, expensive board-level systems could offer its level of performance, says Hackworth, but this custom solution had the additional disadvantage of occupying a slot on the PC's backplane.

The SH260 operates with enough speed to handle the new generation of hard-disk drives that must interface the fastest desktop and portable personal computers. Its host bus, which can attain sustained data rates of 4 Mbytes/s, features automatic wait-state generation for compatibility with all speed grades of host processors from 6-MHz 80286 systems to 20-MHz 80386 systems.

In addition to its performance advantage, the SH260 saves manufacturers of disk controller boards, motherboards, and embedded drives fabrication costs by replacing up to eight medium-scale integration and VLSI devices. Since it is fabricated in CMOS technology, the device is a power miser, consuming 250 mW in typical operating mode. Maximum power consumption is 500 mW. The Milpitas, Calif., company used its proprietary silicon-compiler technology based on 35 "microtile" building blocks to custom design the SH260.

Cirrus expects the chip to have its biggest impact in the market for 3½-in. drives, a market that is expected to grow from 4.2 million units in 1987 to 21 million in 1990, says Hackworth. "We looked beyond the traditional market for disk-controller boards into a market that is rapidly moving toward systems with disk control on the motherboard, or disk drives with embedded control intelligence," he says.

Another advantage the SH260 offers manufacturers of embedded intelligence drives is a master/slave control capability that allows them to install multiple intelligent drives on the same PC bus. Moreover, the chip is compatible with standard Basic Input/Output Systems.

Available now in sample and production quanties, the SH260 costs $30 each in volume purchases. – *Jack Shandle*

Cirrus Logic Inc., 1463 Centre Point Dr., Milpitas, Calif., 95035.
Phone (408) 945-8300 [Circle 363]

# POWER HYBRIDS SAVE DESIGN TIME AND MONEY

A trio of packaged power-hybrid circuit functions from Teledyne Philbrick needs only a few additional components to become a complete power supply instead of spending a year or more on a custom design. The Dedham, Mass., company is targeting designers of power supplies for high-reliability military and aerospace applications with the package, and it's willing to make custom modifications for application-specific critical specifications. The company says it can deliver a custom power supply much faster and at a fraction of the cost of in-house design.

The three hybrids are the 2491 regulating pulse-width modulator, the 2473 power driver/switcher, and the 2478 full-bridge/half-bridge power Schottky rectifier. A complete power supply can be configured by combining these functions and adding a transformer, input and output filters, and two capacitors.

Along with Omnirel Corp., Leominister, Mass., Teledyne Philbrick is one of the first companies into this market [*Electronics*, March 31, 1988, p. 91]. "Building custom power supplies involves a lot of nonrecurring engineering cost and delay in getting to market," says Paul Burgarella, project engineer. "We estimate customers can save a minumum of a year in design and breadboarding time, and between $70,000 and $90,000 in NRE costs with these predesigned functions," he says.

The 2491 pulse-width modulator incorporates all the control functions for a dc-to-dc converter. Included are a frequency-compensated error amplifer, a voltage reference, pulse-width modulator, oscillator, output drivers, and special current-limiting circuitry. The chip is designed to operate at 167 KHz. Compensation can be modified for frequencies up to 500 KHz.

Integrated into the 2473 power driver/switcher are two high-current FET switches and snubber circuitry supplying a minimum of 30 A of continuous current (120 A maximum, pulsed) over a frequency range of 50 to 500 KHz.

Thermal resistance is a low 1°C/W maximum. Burgarella says the 2473 is designed for a 100-W converter and can easily deliver 85% efficiency. It can also be used in motor-drive applications.

Rounding out the trio, the 2478 full-bridge/half-bridge power Schottky rectifier offers 40-A continuous output current, 900-V forward voltage drop, and thermal resistance of 1.0° C/W.

Each of the power hybrid functions comes housed in a 1-in.$^2$, 30-pin metal (Kovar) flatpack that can be surface mounted. Pricing in quantities of 100 is $443 each for the 2473, $502 each for the 2478, and $292 each for the 2491. The devices are available now in limited quantities. – *Lawrence Curran*

Teledyne Philbrick, 40 Allied Dr., Dedham, Mass. 02026.
Phone (617) 329-1600 Circle 361]

## CACHE CONTROLLER BOOSTS SPEED BY 25%

Austek Microsystems Proprietary Inc.'s A38152-25 memory-cache controller for Intel 80386-based systems delivers a 25-MHz clock speed—25% faster than its predecessor, the A38152—but remains pin-compatible with the earlier chip.

Aimed at applications in high-performance personal computers and work stations, the A38152-25 supports 32 Kbytes of zero-wait-state cache static-random access memory using only four 64-Kbit SRAMs, which saves board space.

Sample quantites are available now in 84-pin plastic-leaded chip carriers for $145 each, with production volumes scheduled for July availability.

Austek Microsystems Proprietary Inc., 444 Castro St., Suite 1020, Mountain View, Calif., 94041.
Phone (415) 960-1315 [Circle 345]

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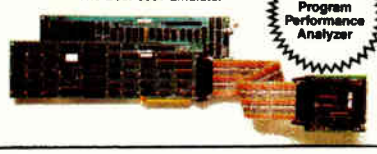

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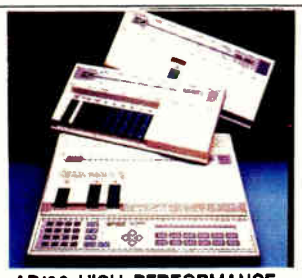

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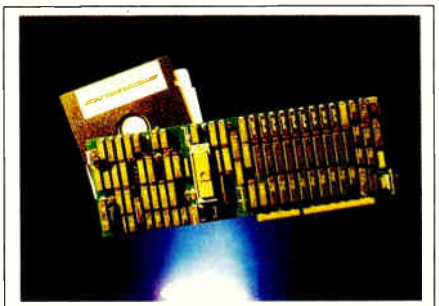

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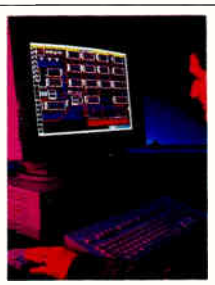

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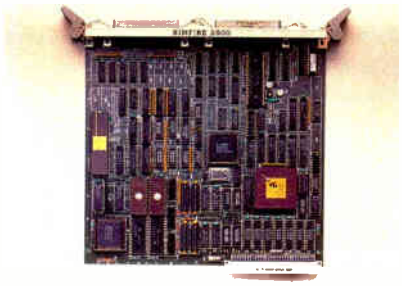

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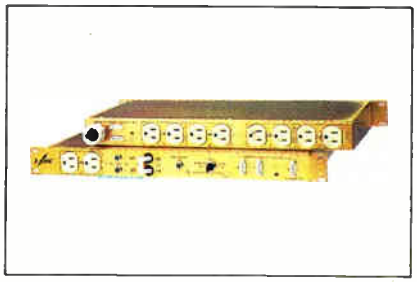

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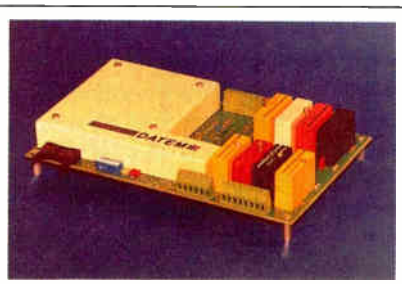


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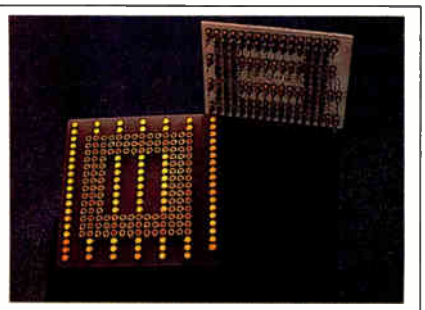

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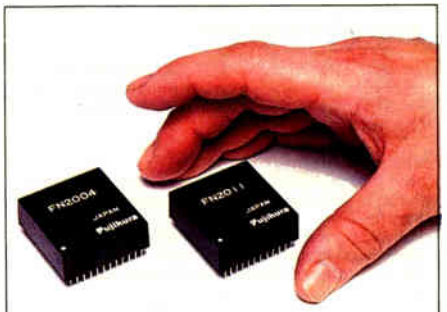


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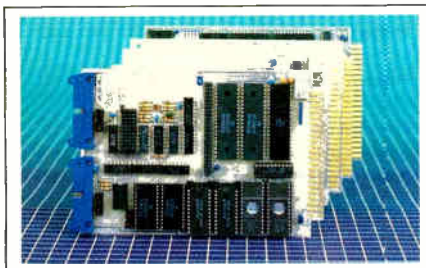

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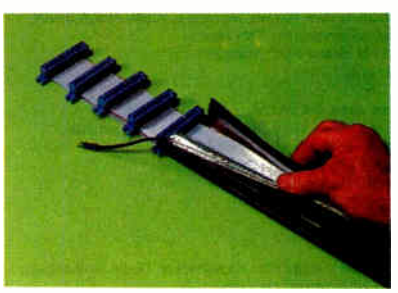

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# ELECTRONICS WEEK

## IBM BUILDS FASTEST SILICON CHIP EVER . . .

IBM Corp. scientists claim they've built the world's fastest silicon circuits using n-MOS transistors designed with 0.1-μm geometries. The chips, which are still in the experimental stage, operate only when cooled in a bath of liquid nitrogen. They can switch on or off in 13 ps—75 billion times/s. IBM says its next challenge will be to build more complex CMOS chips using the same electron-beam lithography developed for these first chips.

## . . . AS CORNELL MAKES FASTEST GaAs DEVICE

A team of researchers at Cornell University in Ithaca, N. Y., and the Siemens Research and Technology Laboratories in Princeton, N. J., say they've built the world's fastest gallium arsenide transitor, a device capable of running at 113 GHz. The transistor uses a variation of a modulation-doped FET technology called ModFET, which consists of several layers of silicon-doped GaAs and aluminum GaAs deposited with molecular-beam epitaxy. The highest previously recorded switching speed for a GaAs circuit was 80 GHz.

## MOTOROLA ADMITS TO OVERCHARGING

Motorola Inc.'s Government Electronics Group pleaded guilty in U. S. District Court in Phoenix to three counts of making false statements to the federal government in connection with "improper labor charges" on Navy contracts in 1983. Motorola will pay $10 million to settle the case, and in return the U. S. Justice Department will not prosecute Motorola on other programs also under investigation. The settlement won't hurt the Schaumberg, Ill., company's government business, though. It says the Pentagon has determined that as a currently "responsible government contractor," Motorola should not be barred or suspended from government business.

## JAPAN'S EXPORT LEAD IS SLIPPING

Japan still has a firm grip on its lead as the top exporter of electronics products to the U. S., but other Pacific Rim nations are eating away at its share. The U. S. imported $24.5 billion worth of chips and assembled electronic gear from Japan in 1987, the American Electronics Association says, and Taiwan held on to second place with $5.6 billion. But Japan's dominance is eroding. The AEA says Japan accounted for 63.5% of U. S. electronics imports from the Pacific Rim in 1985, but only 57.1% in 1987.

## AT LAST: ROM BIOS FOR PS/2 CLONES

The first read-only memory, basic input/output system products for manufacturing hardware equivalent to IBM Corp.'s Personal System/2 models 50 and 60 are appearing. They were jointly developed by Faraday Electronics Inc. of Sunnyvale, Calif. and Phoenix Technologies Ltd. of Norwood, Mass. The ROM BIOS serves as the interface between operating systems, applications software programs, and hardware components for PS/2 machines. The BIOS will be marketed by both Western Digital Corp., Faraday's parent, and Phoenix Technologies. An evaluation kit will be available this spring for $2,500.

## CONTROL DATA BUYS INTO GRAPHICS FIRM

Control Data Corp. plans to pay $68.9 million for a 20% stake in Silicon Graphics Inc., in a drive to become a major player in high-end graphics work stations. The Minneapolis company already markets work stations built by Silicon Graphics, of Mountain View, Calif., and expects to purchase an additional $150 million worth of Silicon Graphics work stations over the next three years. The firms are expected to launch a joint development effort aimed at future-generation work stations. But Control Data has no plans to acquire control of Silicon Graphics; it is prohibited for 10 years from raising its stake over 21%.

## UNISYS ROLLS OUT 386-BASED SYSTEMS

Unisys Corp., which sold $500 million worth of Unix hardware and software last year, has added another family of Unix systems to its line: the U 6000 series, based on Intel Corp.'s 80386 processor. The first system from the Detroit company is the U 6000/50, which starts at $24,500 and supports up to 32 users. The new family fits into the Unisys line between offerings based on Motorola 68000-family processors and superminicomputers built by Computer Consoles Inc.

## THERE'S RISC IN STRATUS' FUTURE

Stratus Computer Inc. will use Motorola Inc.'s 88000 reduced-instruction-set computer microprocessor as the foundation for the new generation of fault-tolerant computers it plans to ship in the early 1990s. The Marlboro, Mass., supplier's RISC-based online transaction-processing systems will be source-code-compatible with today's 68000-based family. Such systems are used in real-time applications such as automated bank tellers, brokerage trading systems, and factory floor control.

## PRINT ENGINE RUNS AT 180 PAGES/MINUTE

A new printer aimed at minicomputer and mainframe original-equipment-manufacturer printer distributors uses a pair of ion-deposition nonimpact print engines to deliver 180 pages/minute on two sides of paper. The S9000-2C from Delphax Systems uses two engines in series to print two-sided copies but only one engine to print single-sided pages at a slower 90-page/minute rate. The system will sell for between $180,000 and $225,000, depending on quantity. The Randolph, Mass., company claims that comparably fast printers for data processing and on-demand publishing applications typically sell for more than $400,000.

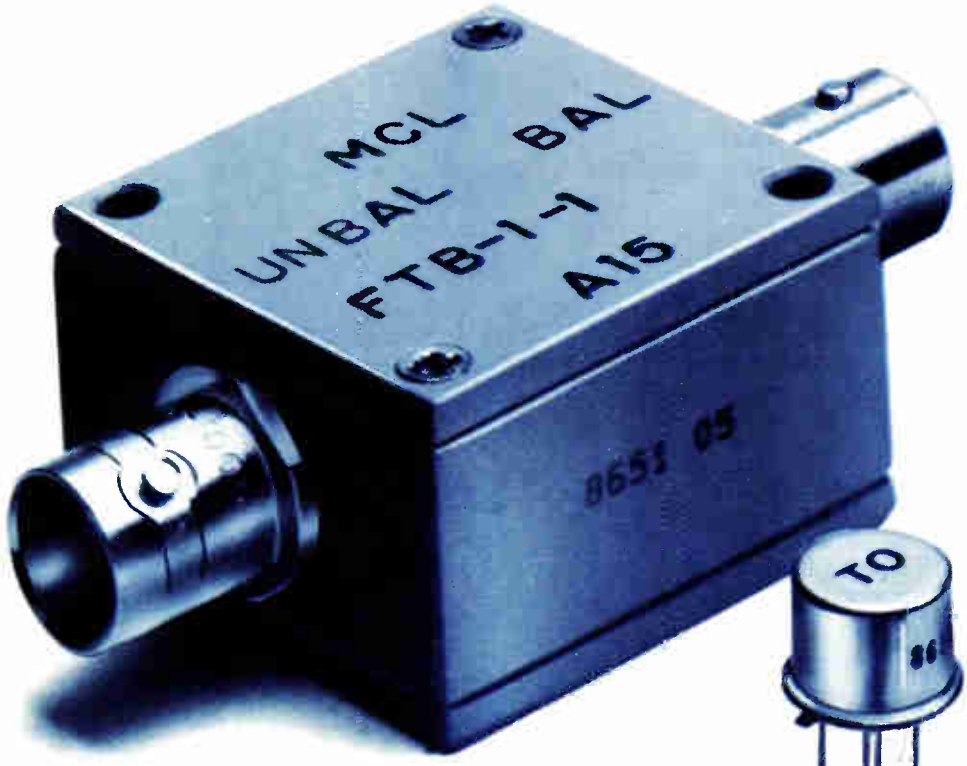
## MOTOROLA SLASHES VME BOARD PRICES

Motorola Inc.'s Microcomputer Division in Tempe, Ariz., is tightening pressure on competitors with across-the-board price cuts on VMEbus computer boards of up to 38%—on an interface module—on 24 products. Pricing for two boards based on Motorola's MC68010 microprocessor were reduced 23%, to $995, and the price for several boards using the MC68020 processor were cut 14%. Motorola, which owns a 30% share of the VMEbus board market, says the price cuts were made possible by higher levels of integration that led to more economical production.

## ALLIANT BUYS RASTER TECHNOLOGIES

In a move to broaden its marketing base, minisupercomputer maker Alliant Computer Systems Corp. will acquire Raster Technologies Inc., a leading supplier of high-performance two-dimensional and three-dimensional color graphics systems. The two released a letter of intent for the sale in late March calling for Alliant, of Littleton, Mass., to issue about 2.2 million shares of its common stock in exchange for outstanding shares of the common stock of Westford, Mass.-based Raster.

# RF transformers

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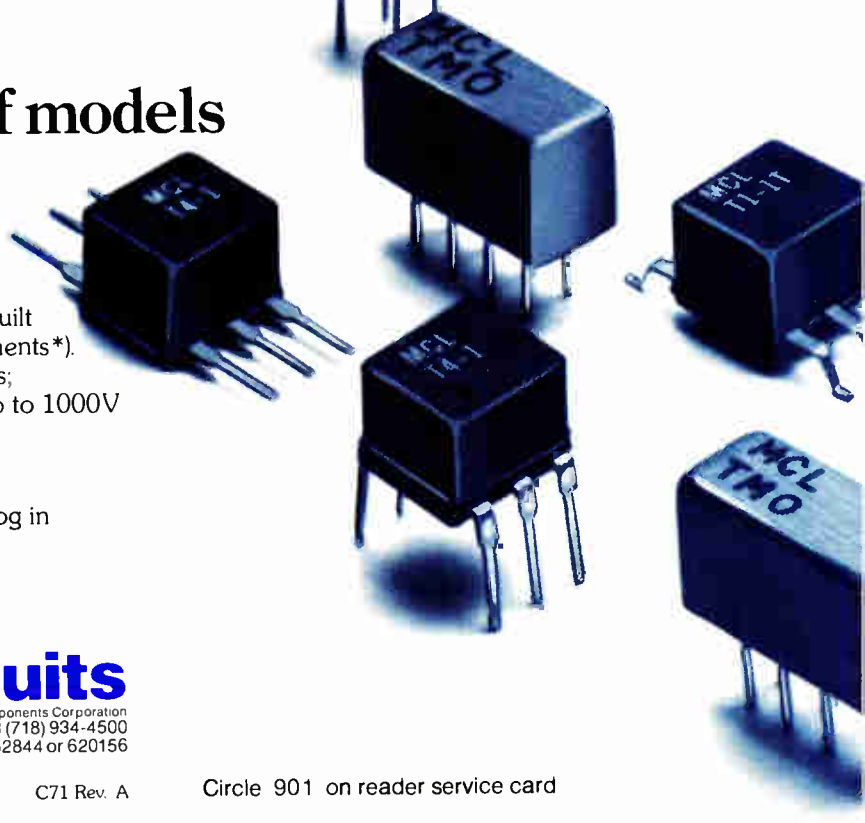


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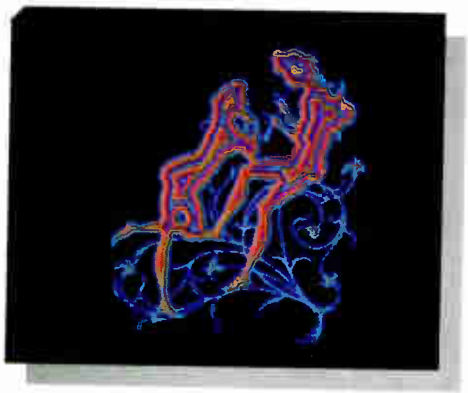

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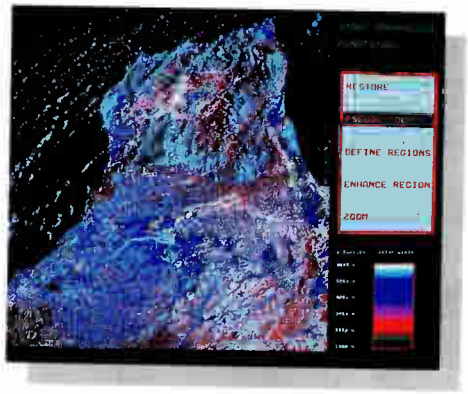


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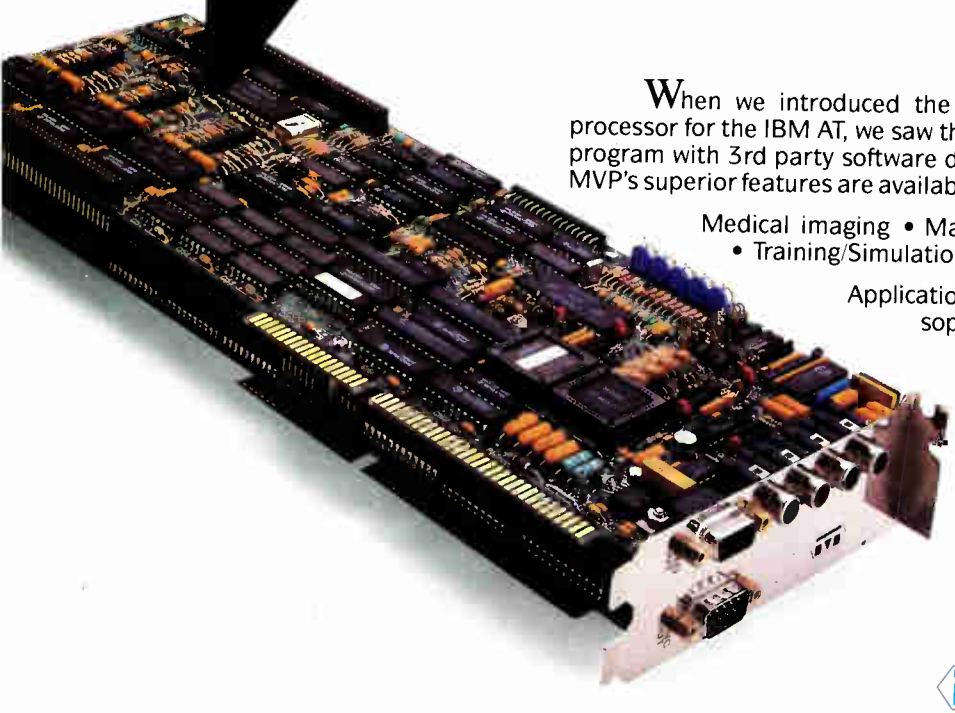

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