FLOATING POINT MILESTONE: AMD, TI, AND WEITEK LAUNCH FIRST SINGLE-CHIP, IEEE-STANDARD PROCESSORS/77

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Electronics®

THE EMBEDDED PROCESSOR BREAKS OUT OF ITS NICHE

PAGE 61

MOTOROLA'S NEW DSP ENGINE COMES WITH FLOATING POINT/64

NATIONAL ALTERS ITS CISC CHIP TO DO EMBEDDED CONTROL/66

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Below: NS32532 chip
*Left: VME532 evaluation board; NS32532 block diagram; competitive performance comparison**

* *Sources:*
NS32532 — August 1987 Performance Evaluation Tests
80386 — "The 80386: A High-Performance Workstation Microprocessor." Intel Corp., June 1, 1986
68020 — SUN 3/20 @ 25 MHz, as published by Sun Microsystems

The NS32532

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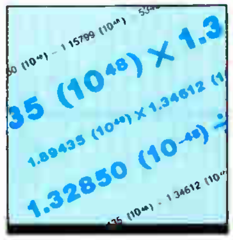
Of all the editorial skills needed to spot and write about the significant news in the electronics industry, the most important are being able to find the trend amid the mass of information that is constantly bombarding us and the talent and energy necessary to move quickly to develop a story. One of the cover packages made its way into this issue because two of our veteran editors possess those skills and talents to a remarkable degree.



It all started at last month's International Solid State Circuits Conference in San Francisco. Executive Editor Sam Weber and Special Projects Editor Stan Runyon were busily meeting with sources, talking to designers, listening to the latest industry gossip—all the things that editors do at what has become the premier technical meeting of the semiconductor business.

As Stan tells it, "Among all the tidbits that we were picking up was the news that three major chip houses, unbeknownst to each other, were planning the world's first single-chip IEEE floating-point processor." In other words, the standards for the 64-bit floating-point arithmetic set by the Institute of Electrical and Electronics Engineers would finally be implemented on one chip.

"But we had to move on the story fast," Stan continues, "because the chips were about to hit the market. We had to get started right away."

Stan and Sam quickly got on the phone to headquarters in New York. The March 17 issue was only two weeks away and its feature pages were already filled. It would take an important story to get the editor-in-chief to add the floating-point package at this late date. But the San Francisco team turned the trick, convincing the people back home that the story was worth the effort.

After Stan convinced one of the companies, which was reluctant to discuss its product, to become part of the coverage, the staff swung into action. Art Director Fred Sklenar revamped the cover. Rob Lineback in Dallas was already writing an article about the Weitek chip, and the Texas Instruments piece was added to his assignment. Stan turned to the Advanced Micro Devices story. Rob also contributed the overview that leads off the package on p. 77. In addition, interviews had to be scheduled and conducted for the biographical sketches, and photos had to be taken.

"It was quite an impressive display of teamwork," says Stan. With Stan serving as manager of the project, "the time elapsed between our arrival back in New York from the ISSCC until the pages closed was about two weeks—and that includes the time it took for the display material to arrive."

As for the companies involved, says Rob, "they couldn't have picked a better time to get their chips to market. The soaring popularity of reduced-instruction-set computer architectures and the proliferation of the new, powerful work stations are pushing the growth of numerically intensive jobs. The result is that floating-point units are being rushed into the game to substitute for data-processing software. Technical work stations are on the shopping lists of bankers, economists, and stock brokers."

And you're going to read about it first in *Electronics*—all because our team of veteran editors and production people both know a story when they see one and know how to turn that story around fast.

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Electronics

NEWS

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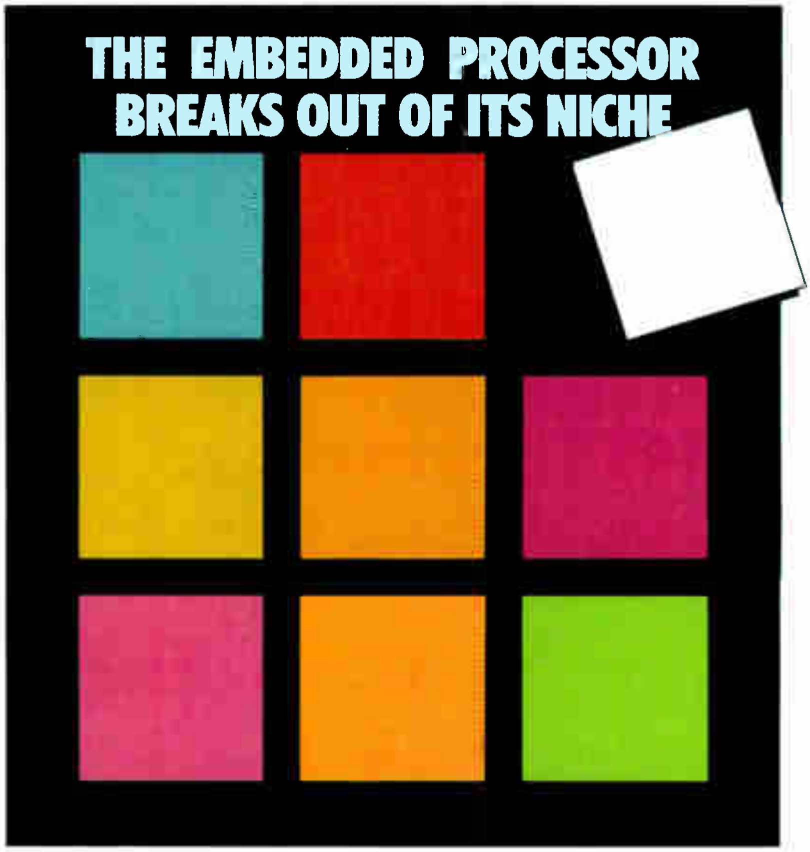
TECHNOLOGY SERIES

COVER: ART DIRECTOR FRED SKLENAR



PAGE 61

NEW PRODUCTS

DEPARTMENTS

Great advances have always displaced lesser theories.

Introducing a revolution that will change forever the way you view the world of *cell-based ASIC design.*

For centuries the earth was flat; it remained that way until someone brought us a new, and better, view of the world. Great advances have always given us new ways to see our world as well as new worlds to see. Now Motorola introduces its next revolution, destined to change forever the way you view the world of cell-based ASIC designs—the Silicon Compiler Modules. Until now all cell-based libraries have stifled creativity by limiting you to *something pretty close,* until now...

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• D-Register	• Barrel Shifter	• PLA
• Comparator	• Incrementer/ Decrementer	• Prescaler
• 3-State Buffer	• Parity Gen/ Checker	• RAM
• Counter	• Inverter	• ROM
• Adder	• Serial Interface (SPI function)	• Status/ Control Register
• Multiplexer		• Timer
• Register File 1R/W		• UART (SCI function)
• Register File 2R/1W		

How it works.

The menu-driven system makes it easy for anyone to use, simply select the function you need and go. Through schematic entry, input the parameters for the cell function you've chosen and the compilers build the correct implementation. On command the compiler executes according to your instructions, supplying all the proper symbols and the function and performance parameters. Afterwards, the silicon compiler provides all pertinent information about the cell you've just designed.

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FYI

IT BEGINS TO SOUND LIKE THE GOOD OLD DAYS

A 'superheated' chip market strains production capacities, vendor-customer relationships, and just-in-time manufacturing; double-ordering rises

By now, I shouldn't be the least bit shocked by anything that comes along in the boom-or-bust semiconductor business. As far back as 1959, I was writing about a coming shakeout with no more than five producers surviving. So much for that. By 1973, I described it as a "wild and woolly" industry, where technology-driven companies were being run by inexperienced, immature managers and frantic customers were double-ordering at the slightest hint of a parts shortage. Well, welcome to 1988!

An early March trip to eight Southern California chip makers—yes, Virginia, there are exciting chip makers based outside Silicon Valley—proved to me some things just don't change in this crazy business. Yep, some executives are gaining maturity, and, yep, some companies are becoming market driven. But both examples are still in the minority. And despite closer working relationships between vendors and buyers, many customers are just as apt to over-order as they ever were.

Business is certainly good for most chip makers in and out of Southern California. But it's most exciting for those outfits that are increasingly market driven. I ran into this at Western Digital in Irvine and Brooktree in San Diego. But nowhere was it more obvious than at Silicon Systems in Tustin, where CEO Carm Santoro has been busy showing us how a niche strategy can be wonderful. He has also been busy revising upwards his 1988 sales forecast. Originally budgeted for $95 million, sales are now expected to hit as high as $125 million, most of this growth added by getting more output from foundries. "My big problem," Carm adds, "is I'm out of capacity." So he's now looking for a big wafer fab to buy.

"It's a superheated market," Carm acknowledges: "a lack of dynamic RAM and 386 microprocessors." He doesn't see anyone holding much inventory in his markets, "which tells you some growth is being missed." But there's still double-ordering aplenty in some markets. Despite what chip makers believe, some system houses have been raising their inventories to protect themselves, as well as expanding their vendor base for short-supply parts—evidence that tight customer relationships and just-in-time shipment programs are under growing strain. Convex Computer in Richardson, Texas, has increased its DRAM inventories to help cover any potential shortfalls. And Unisys is expanding its chip-supplier base from less than five. Even so, the No. 2 computer maker has been forced into the spot market for 256-Kbit chips. Clearly this is the worst memory chip shortage in history—due as much as anything to so much memory being designed into products during the "free memory" days of the past three years.

ROBERT W. HENKEL

THE SOFTWARE PROBLEM SOLVERS

If you were ITT and had to automate power monitoring and control systems for telephone power plants, who would you turn to? And what if you were Bell Canada and your purpose was to automate the company's trouble reporting, analysis, and control procedures? Or suppose you were the Allright Parking Company and had to automate the data acquisition and distributed control of a large number of parking facilities?

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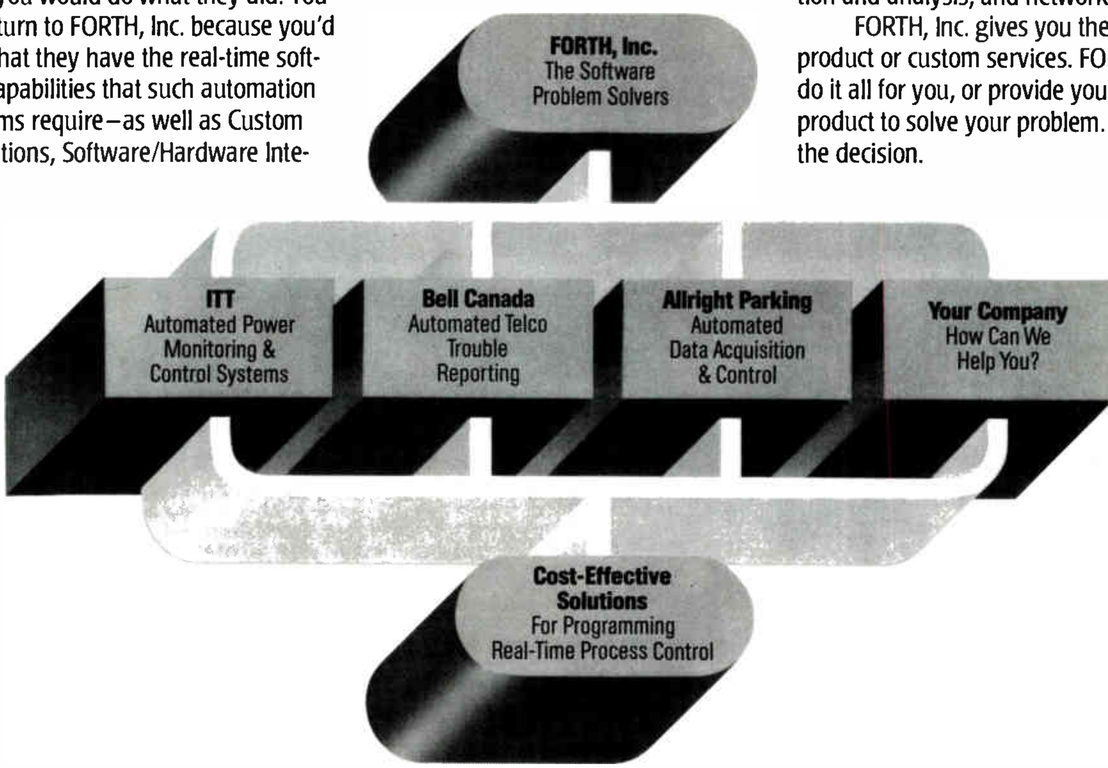

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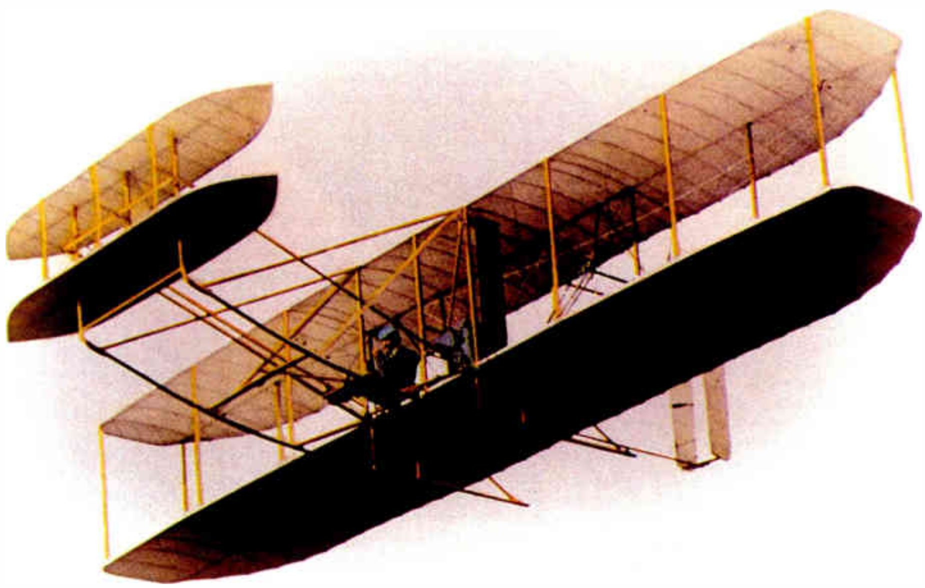
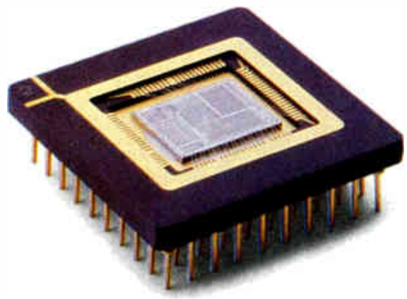
"WITH THE EXCEPTION OF OBSERVATION, I SEE NO MILITARY USE FOR IT."

AMERICAN GENERAL, 1908



"IT'S GOT POSSIBILITIES, BUT IT'S JUST TOO POWERFUL FOR MY APPLICATION NEEDS."

DESIGN ENGINEER, 1988



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LETTERS

RISC-Y BUSINESS

To the editor: In his letter [*Electronics*, Nov. 12, 1987, p. 12], D. H. Methvin tries to compare the HP Precision Architecture with the HP 3000 stack architecture to cast doubt on the relative advantages of reduced-complexity architectures. His comparison, however, is not between the architectures themselves, but between implementations of those architectures.

The implementations that he compares are apparently the 4.5-mips HP 3000/930 and the 1.3-mips (not 1.1) HP 3000/68, although this is only implied in his letter. The native mips ratio of these processors is approximately 3.5 to 1.

The HP 3000/68 is a microprogrammed implementation of a complex architecture consisting of ten logic boards, two microstore boards, and one cache board. Each logic board contains 120 ECL chips. The HP 3000/930 is a directly implemented reduced-complexity architecture consisting of three processor boards, one cache board, and one virtual-address translation cache board, plus a one-board floating-point coprocessor. The three processor boards are populated with a total of about 450 advanced Schottky TTL packs—no custom logic.

This TTL machine is a simpler, smaller, slower hardware implementation, yet it can run programs in less than a third of the time of the ECL processor. I invite readers to consider what level of native performance would result from implementing the Precision Architecture in equivalent ECL logic.

Many applications for the stack HP 3000s have been carefully "folded" to fit within the constraints of 16-bit segment addressing. Users are finding that the simplifications permitted by larger virtual addresses reduce instruction counts significantly, leading to more than 20 to 1 speedups in some cases.

Michael J. Mahon, Lab Manager
Information Technology Group
Hewlett-Packard, Cupertino, Calif.

□ D. H. Methvin, president of Davin Computer Corp., replies: *"Mr. Mahon makes my case for me. The 930 is much cheaper to build than the 68, a slow architecture implemented on a 16-bit frame. The 930 has a higher mips rating than the 68. Its performance, however, appears to fall significantly below what I would expect of a machine that is twice as wide, 3.5 times as fast (in mips), and uses a register-intensive architecture instead of the much slower memory stack architecture. For a small compute task that is repetitive and can fit into its cache, the 930 should whip the 68 by a factor of 6 or 8 or more. Where's the mips? I'm afraid I'm still confused."*

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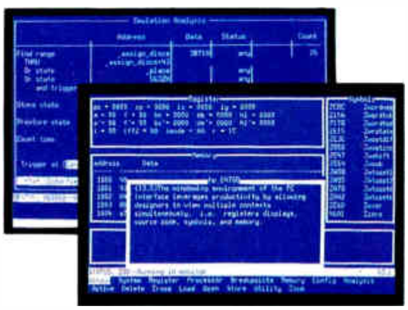
In addition to the features shown above, there are lots of others that put the HP 64700s in a class by themselves. To name a few: function with IBM-PC, HP Vectra and compatibles, RS-422 high-speed serial we never stop asking "What if..."

You could spend a lot more and get a lot less.



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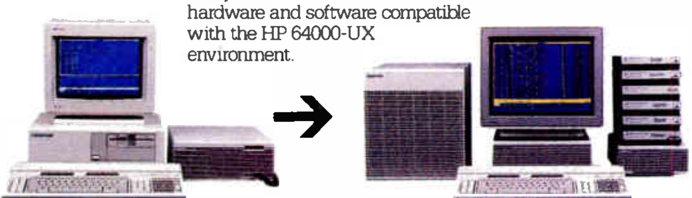
Up to 32 emulators can be interconnected, synchronously started, cross armed, cross triggered, and halted.



Entry level HP 64700 emulators are hardware and software compatible with the HP 64000-UX environment.

interface for superior download and upload speed, code coverage analysis for efficient software testing and design, host-independent portability, and compatibility with popular absolute file formats such as Tektronix and Intel hexadecimal and Motorola S record.

Once you get your hands on an HP 64700 emulator, you'll agree that this is the new standard in the field. Especially at a starting price of $8,900.

Free demo disc.

For a free demo disc that gives you the "hands-on" feel for HP 64700 Series capabilities, call HP at 1-800-752-0900 ext. 501A, or mail the attached business reply card.

HEWLETT PACKARD

Circle 19 on reader service card

WHY VTC? ASK THE VME CONSORTIUM.

"For a bunch of companies that don't always agree on everything, we sure were unanimous on VTC."

Joseph Ramunni, chairman (left), and Jack Regula, technical director, VME Technology Consortium.

The VME Consortium needed an economical, yet highly functional VME bus interface chip, to minimize design time . . . and to help raise the VME standard to higher levels.

"We looked at the leading suppliers," said Joe Ramunni, consortium chairman (and president of Mizar), "and VTC came out on top. Their CMOS standard-cell ASIC approach gave us the high drive capability we needed, optimized for bus interfacing. And, it proved much more cost-effective, with higher performance, than gate array technology."

The VME Consortium is made up of such firms as Plessey Microsystems, Omnibyte Corporation, Mizar Inc., Ironics Inc., Heurikon Corporation, Matrix Corporation, and Clearpoint Inc., among others. What did they look for in a supplier?

"We needed a credible business partner," said Ramunni, "with a proven track record, who could provide a turnkey package . . . both design and fab. A supplier that could produce in quantity, and provide technical support to the market at large.

"We also needed a firm with an international marketing structure, because we expect this chip to be the de facto standard worldwide.

"But, we needed *people* we could work with, too. VTC had the right 'comfort factor'."

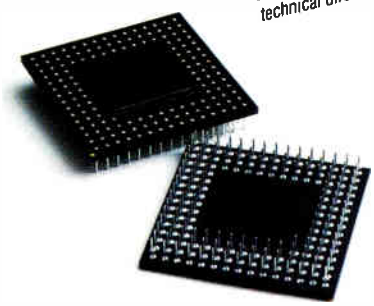
Jack Regula, consortium technical director (and VP-R&D, Ironics) added: "Our requirements for high speed, high gate-count, low power consumption, and VME bus drive capability were all met well with VTC's 1-micron CMOS standard cell library. And we were extremely impressed with VTC's facilities, its people, and its customer list."

In the future, the VME bus chip (VIC) will become a standard cell within VTC's CMOS library, to allow customers to further customize the chip.

Shouldn't you be getting to know VTC, too? You'll be in good company when you do. Call or write us today, and we'll send you our short-form product catalog, which describes our product offerings in linear signal processing, high-speed CMOS logic, mass storage ICs, bipolar ASIC, and CMOS ASIC.

VTC Incorporated, 2401 East 86th Street, Bloomington, MN 55420. (In Minnesota, 612/851-5200.) Telex 857113.

CALL 1-800-VTC-VLSI



VTC Incorporated
Performance, Pure & Simple™

ELECTRONICS NEWSLETTER

EUROPEAN COMPLAINT COULD UPSET THE U. S.-JAPAN CHIP TRADE ACCORD

The U. S.-Japan semiconductor trade agreement could be endangered next week when representatives of the 95 signatories to the General Agreement on Tariffs and Trade meet in Geneva on March 22. A GATT panel, formed in response to European Communities' charges that the chip pact allows the U. S. and Japan to fix chip prices, has at last produced a report. The confidential study is now being reviewed by the EC, the U. S., and Japan. The U. S. Trade Representative's Office in Washington believes that the EC's problem can be ironed out between the GATT panel and Japan's Ministry of International Trade and Industry, without abrogating the current agreement. If so, the solution may involve little more than changing Japan's procedures for preventing the dumping of Japanese chips. If not, a new round of negotiations involving the EC, the U. S., and Japan may be needed. Solving the EC's complaint could be tough: the EC is not just concerned with the fixing of prices in world markets, but also with the pact's mandate for U. S. access to Japan's chip market (see p. 31), which is not shared by EC members. □

IBM GETS CLOSER TO MAKING BALLISTIC TRANSISTORS PRACTICAL . . .

IBM Corp. has taken a big step toward making ballistic transistors a practical technology, but researchers at its Thomas J. Watson Research Center say there's still a long way to go. By demonstrating ballistic-hole transistors for the first time, IBM scientists recently did what many in the physics community thought impossible. The holes are the spaces left after electrons have jumped to a new location. The problem had been that 95% of them are considered too heavy and slow to charge from one gallium arsenide layer to another through a thin layer of insulation—in this case aluminum gallium arsenide—says IBM physicist Mordehai Heiblum. But by getting the right level of doping in the base material and a thin-enough insulating layer, Heiblum was able to filter out heavier holes and still get a significant number of lighter holes to cross the insulating barrier at ballistic speed. The ballistic-hole transistor is a p-type positive transistor, and is a complement to the ballistic-electron transistor, which is n-type, or negative. "Potentially this is the fastest semiconductor device type there is," he says, adding that 1-ps switching speeds are already within reach. But useful circuits are still at least five years away. □

. . . AS AT&T USES ALL-METAL TECHNIQUE TO MAKE SINGLE-ELECTRON TRANSISTORS

Scientists at AT&T Co.'s Bell Laboratories have developed a single-electron transistor that is so sensitive that a single electron can change the current flowing through the device. The metal-oxide-metal structure, which has an intrinsic speed of less than 1 ps, is constructed of two submicron aluminum layers that sandwich a tiny oxide layer just tens of angstroms thick, says Greg Blonder, who heads the Photonics and Electronics Research Department at the Murray Hill, N. J., facility. The device "is very much like a FET structure," he says, but it requires an ultra-cold environment to work—less than 1.2 K. That, combined with the need for drawn features of just 0.05 μm, means such devices won't be practical for at least a decade, Blonder says. □

UNISYS USES CMOS VLSI CHIPS TO BOOST MAINFRAME PERFORMANCE

Unisys Corp. is using densely packaged CMOS VLSI circuits to gain up to a fourfold price/performance boost in its newest family of mainframe computers. The 2200/400 family of multiprocessing mainframes from the Blue Bell, Pa., company will be priced to compete with IBM Corp.'s 4300, 9300, and 3090 systems. The family, part of Unisys' OS-1100 line, will cost from $178,000 for a one-processor unit to $952,000 for a six-processor model.□

Quality champ captures low price title with $745 data acquisition board.

By: Joe Zimmerman, Sports Staff
Marlboro, MA

Faster than you could say "what hit me?" the fight was over.

With speed (20 kHz), multiple I/O combinations (16 A/D, 2 D/A, 16 DIO), and a below-the-belt price, Data Translation brawled its way to the low price data acquisition championship.

Asked after the fight about the loser's slow speed and high price, Fred Molinari said, "Was he fightin' in slow motion, or what? I can't believe anyone would pay him more."

Indeed, this reporter can't believe it either. The DT2811 is a great value—even without the FREE DT/Gallery Software that Data Translation ships with it. And optional industry standard software packages are available at incredibly low prices.

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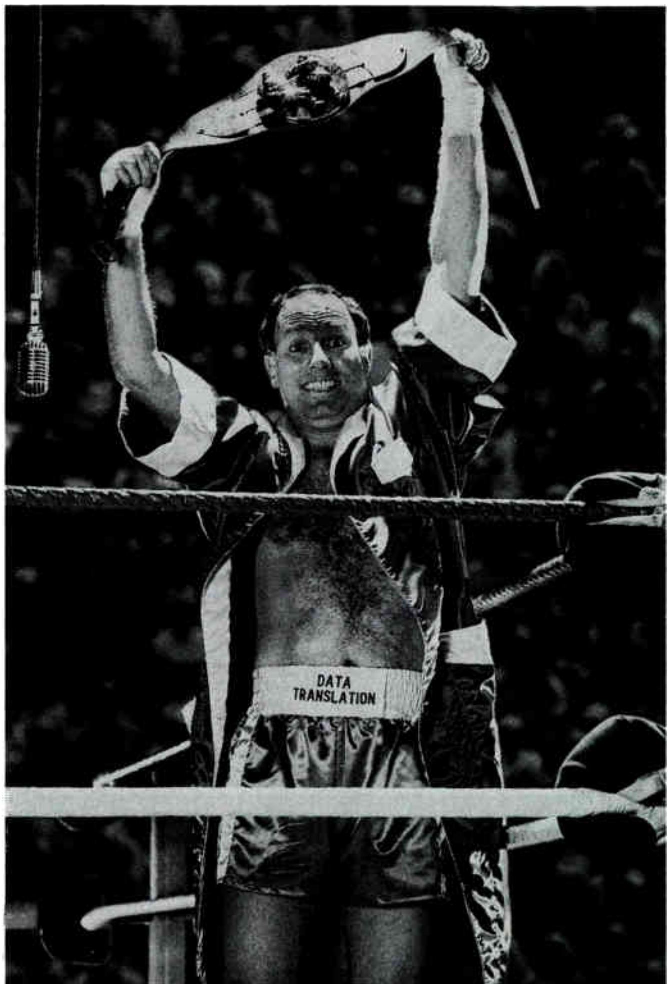
Call (617) 481-3700.

To learn more, see us in Gold Book 1987, or call to receive our first-ever 1987 3-Book Set, including 1987 Catalog, Product Summary Price List, and Applications Handbook.



Fred Molinari, President

	Analog Inputs			Analog Outputs			Digital Functions				
Model	Input Channels	Resolution (bits)	Throughput	Output Channels	Resolution (bits)	Throughput	I/O lines	Programmable Clock	Screw Terminal Panels	Software	Price
DT2811	16SE/8DI	12	20 kHz	2	12	50 kHz	8 In, 8 Out	Yes	Yes	DT/Gallery (free) LPCLAB LABTECH ACQUIRE DT/Notebook	$795

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Circle 24 on reader service card

PRODUCTS NEWSLETTER

HP WORK STATIONS OUTDO COMPETITORS' FLOATING-POINT PERFORMANCE...

Hewlett-Packard Co.'s latest crack at the lucrative computer-aided-graphics market is a pair of work stations delivering double the floating-point performance and 40% better integer performance than the competition. The two-dimensional 835CHX and the three-dimensional 835SRX both offer 2-million-floating-point-instructions/s and 14-million-integer-instructions/s performance, filling the gap between older machines and the TurboSRX series (see p. 95). The Palo Alto, Calif., company boosted floating-point speed by teaming high-end multiplier/divider and arithmetic logic with a proprietary floating-point controller chip that overlaps operations between reduced-instruction-set-computer and math chips. Integer performance gains come from speeding up the clock on HP's proprietary n-MOS III RISC chip and by enlarging the central-processing-unit cache from 16 to 128 Kbytes. The 2-d 835CHX sells for $59,500 and the 3-d 835SRX for $69,000. Orders begin in April. □

...AS SILICON GRAPHICS PLANS EXTENSIONS AT BOTH ENDS OF ITS LINE

Look for Silicon Graphics Inc. to extend its line of three-dimensional graphics work stations in both directions by year's end. At the high end, it plans to add a multiprocessor system with up to eight MIPS Computer Systems Inc. processors and increased graphics-processing capability. The machine will fall in the range of 5 to 15 Linpack megaflops and a price range of $75,000 to $150,000, and will compete with the powerful new work stations from Ardent, Hewlett-Packard, and Stellar. Also on the way is a low-end system, which the Mountain View, Calif., firm says will create a new category—personal 3-d work stations. Such systems will combine powerful graphics with computation capability of 8 to 10 mips and 1 Linpack megaflops for $15,000 to $30,000. By 1990, these machines will be 70% of its business, the company says. □

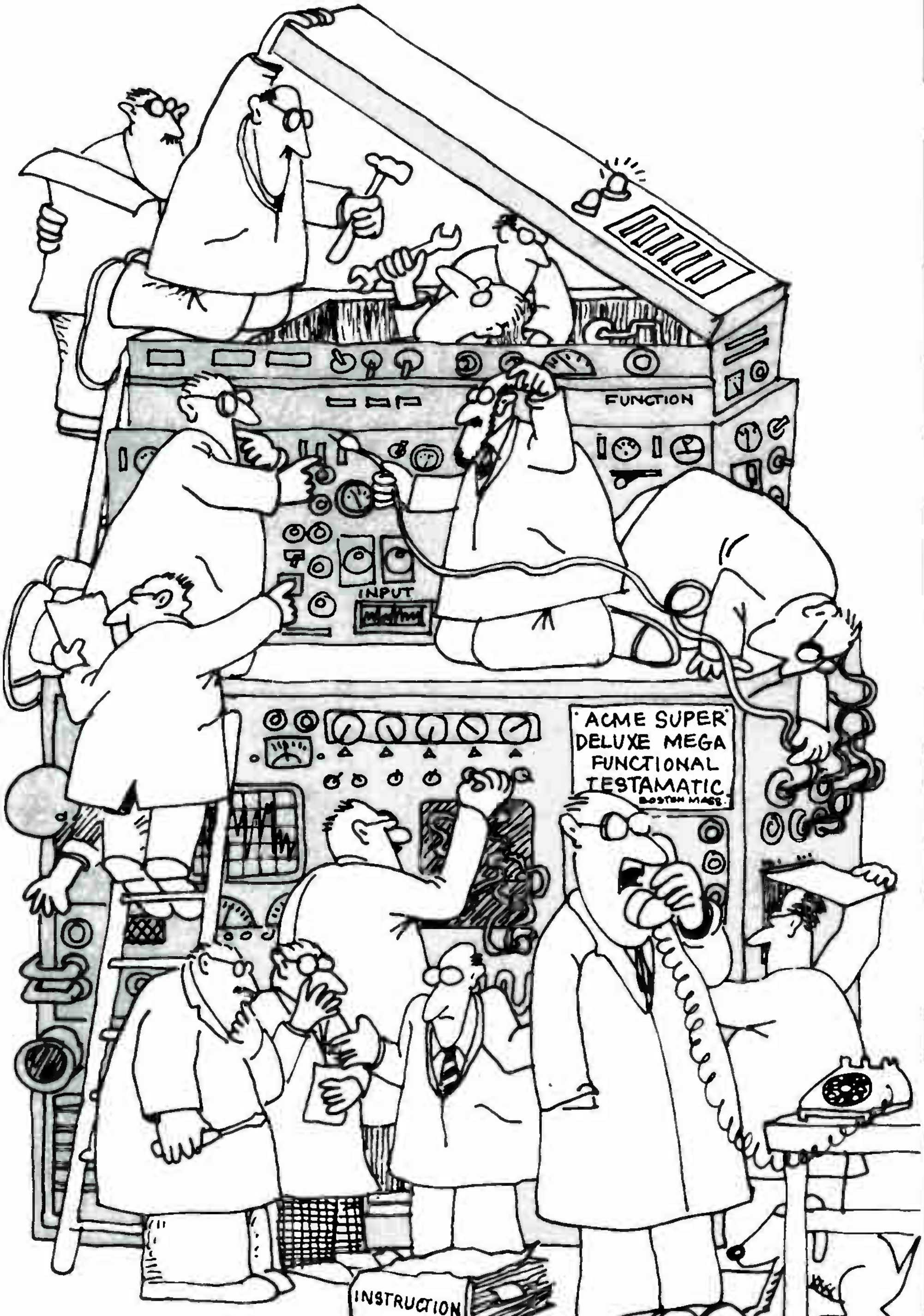
ANALOG DEVICES GIVES ITS POPULAR DSP CHIP A 66% BOOST IN SPEED

Finer geometries in Analog Devices Inc.'s CMOS process are making its industry-standard ADSP-2100 digital-signal-processing chip about 66% faster. The Norwood, Mass., company's new ADSP-2100A comes in two speeds—a 10-MHz version upgrading the previous-generation 6-MHz chip, and a 12.5-MHz version that takes over the speed-leader spot of the 8-MHz ADSP-2100. Aimed at high-performance telecom applications, the ADSP-2100A is fabricated in a 1.0-μm process instead of the 1.5-μm process used for the original, but the upgraded units retain compatibility with the originals in both instruction code and pinouts. Both speed versions are available in 100-pin ceramic or plastic leaded chip carrier packages. Samples are available now. Production pricing in purchases of 100 to 500 will be $175 each for the 10-MHz part and $225 each for the 12.5-Mhz part. □

TELEDYNE'S OPTICALLY COUPLED RELAY DELIVERS SEVEN TIMES FASTER SWITCHING

Designers of automated-test equipment and other equipment that demand super fast relays can get seven times better performance with Teledyne Solid State's new optically coupled C66 series. The top-of-the-line C66-2 boasts a 150 μs turn-on time—previous optically coupled devices ranged between 1.0 and 10 ms. The entire C66 line turns off in 300 μs at a 255 mA input current, say officials at the company's relay division in Hawthorne, Calif. Another key feature is a low, 50-nA leakage current that helps enhance ATE measurement accuracy. Typical output leakage current of the competition ranges from 10 μA to 1.0 mA, says the company. The C66-2 also boasts a continuous output load voltage rating of ± 350 V and continuous load output current of 300 mA. Available now, the relays cost $65.90 each. □

There ought to be a better way to test bus-structured boards.



"Sure, sure... no problem, we'll have this baby up and running any day now... yep, just a few more days now... coming right along... heck of a tester... just a few more days more or less... yep, sure... no problem..."

Installing and programming some new testers can be almost comical.

Unless of course, it's *your* tester.

Fortunately, the Zehntel 3200 shrinks installation and programming time from months to *weeks*.

What's more, the Zehntel 3200 can test the full range of bus-structured boards. Even with multiple microprocessors.

The Zehntel 3200 has diagnostics that track faults right to the root cause of failure—normally, in less than 3 minutes. And you get reliable, 99% yield.

Now consider this.

The Zehntel 3200 delivers all this capability for about one-third the cost of some other functional testers.

Just write or call for complete information today.

Otherwise, you're just wasting your time.

The Zehntel 3200 performance tester. Up and running in weeks.

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Circle 27 on reader service card

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There's no simpler, faster, easier, or more accurate way to test active devices than through use of the Wiltron 360. In addition to bias tees, Wiltron Active Device Test Sets feature step attenuators in each port line to set signal levels. A third step attenuator allows direct measurement of all four S parameters, including output match, on devices with up to one watt output power. Only Wiltron gives you step attenuators to 40 GHz and a 140 dB confidence-building dynamic range.

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Phase-locked accuracy. Compared to anything else available, the 360 improves twentyfold, from 40 to 2 ms, the time needed to phase lock at each test frequency. Only the 360 gives you phase-lock accuracy at "real-time" measurement speeds. No high-priced synthesizer is required.

Unmatched color display. Choose any single, dual, or four channel combination: magnitude (real or imaginary), phase, rectangular, Smith chart, time or frequency domain, or group delay. With the color display, markers and limit lines are easily and quickly distinguished from test data and the graticule grid.

Passive or active devices. Test Sets for passive and active devices cover the 40 MHz to 20 GHz *and* 40 MHz to 40 GHz ranges from a single coaxial test port.

For more information, please address Wiltron Co., 490 Jarvis Drive, Morgan Hill, CA 95037-2809. Phone (408) 778-2000.

WILTRON

Circle 29 on reader service card

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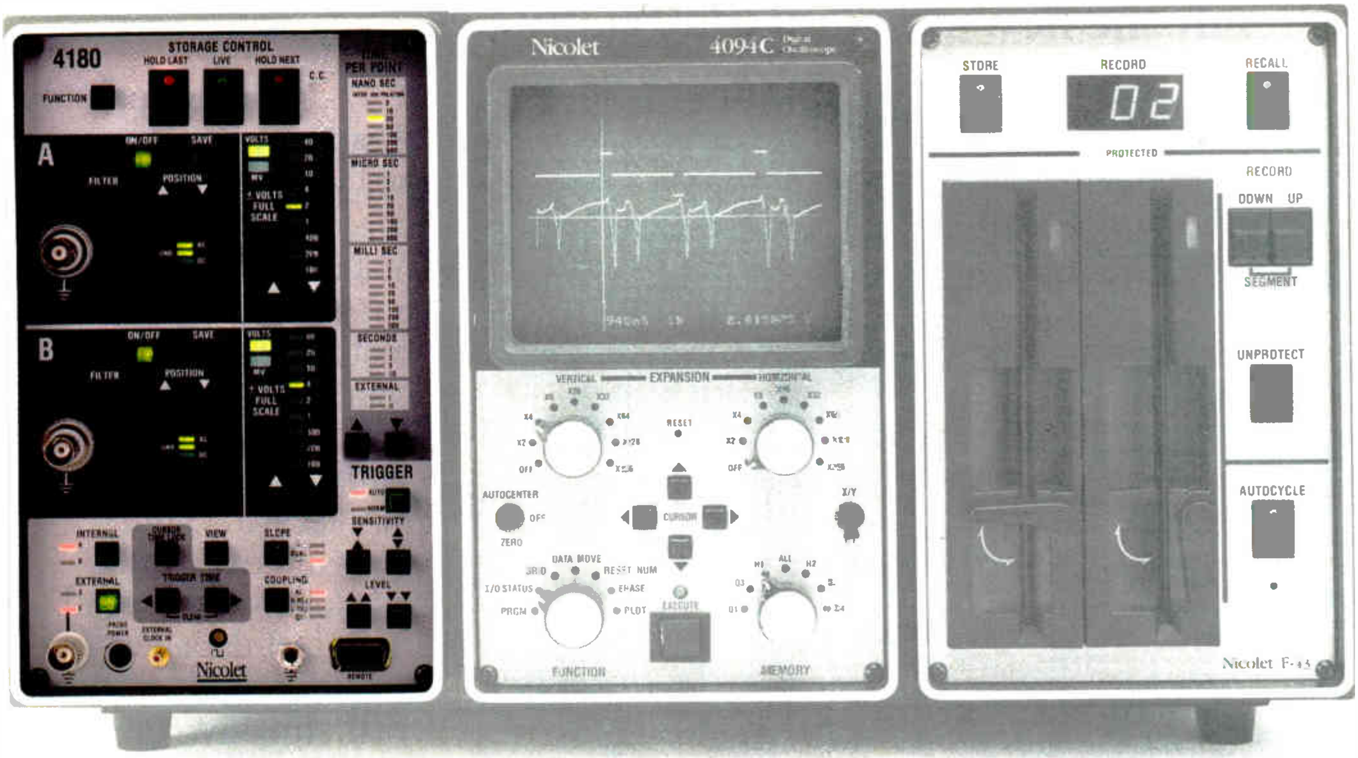
SPEED TRIALS.



• Multi-channel: two or four channel configurations.
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Speed. Using the latest designs in ADC technology, your input signal can be digitized at speeds up to 200 MHz (5ns per data point) and saved for analysis. The wide band input amplifiers allow signals up to the 100 MHz Nyquist limit to be input without distortion. Sophisticated trigger setup displays allow you to accurately set the level, sensitivity, and slope to make one-shot transients easy to catch; eliminating the usual hit or miss guesswork. For multi-channel applications two 4180's can operate together in one mainframe producing a four channel scope with no degradation in speed or performance.

Real-Time Math. In addition to the extensive post-processing capabilities in the mainframe, the 4180 has several useful routines which present computed results as live, real-time displays: *FFT, MAX/MIN, A+B, A−B, A×B, A/B,* and *AVERAGING.*

Nicolet
INSTRUMENTS OF DISCOVERY

Circle 30 on reader service card

systems side are Richard Alberding, executive vice president of marketing at Hewlett-Packard; Scott McNealy, chairman and president of Sun Microsystems; and James Treybig, president of Tandem Computers. The chairman is William Krause, president of 3Com Corp., presumably a disinterested party, because his company is not a major DRAM user.

The panel is the child of an industry summit meeting among 14 chief executives that was convened quietly in Santa Clara early this year by the American Electronics Association. The AEA had decided something had to be done to end the "unseemly scraps between interdependent parts of the U.S. industry," says Ralph Thomson, senior vice president of public affairs for the AEA. "We just felt we had to take the bull by the horns."

The panel's first task was to lay out its position. To do that, it started work on what became the nine points. That paper was taken to both the AEA and the Semiconductor Industry Association—generally speaking, the former represents both chip and systems houses; the latter, chip makers—and got both of them to endorse it. For its part, the SIA is backing changes in the way the trade pact sets fair-market values for chips, which help determine prices.

So far, the idea of a united front seems to be working. "You'll find a different tone and different substance [in the talks] than you would have six months ago or even three months ago," says the AEA's Thomson.

The test will come when the panel starts fleshing out its ideas. In addition to the plan to set up chip-buying consortia—for which antitrust exemptions would probably have to be sought from Congress—the joint task force will consider these pioneering proposals:

- Modify the trade agreement's procedure for setting fair market values by excluding products that have no current or potential U.S. production base.
- Postpone price floors on semiconductors whenever prices climb and shortages occur because demand outstrips supply. When prices reach a certain percentage of the fair market value, the pricing system would kick in again.
- Support long-term semiconductor purchase arrangements.
- Encourage individual Japanese companies to comply with the intent of the trade agreement by lifting sanctions on those buying more components from U.S. manufacturers.

"These are proposals on the table, and we are going to take them up at a meeting by the end of March or early April," says Thomson. *– J. Robert Lineback*

SOFTWARE

RELAX, UNIX USERS; AT&T IS KEEPING IT OPEN

NEW YORK

Unix licensees nervous about the new AT&T-Sun Microsystems Inc. alliance can breathe easier: a formal program is evolving at AT&T Co. that backs up the company's promise to keep the operating system from becoming "privatized." AT&T is offering to work with microprocessor vendors to get the next Unix version—System V Release 4.0—ready to go at about the same time and with the same binary-compatibility advantages as the chips, like Sun's Sparc and Intel's 386, used in AT&T product lines. And Motorola Inc. is the first to say that it intends to sign up.

In January, many Unix-system vendors reacted angrily when the telecommunications giant announced closer ties with Sun, including the adoption of its Sparc architecture for use in AT&T products and the purchase of 20% of the work-station company [*Electronics*, Jan. 21, 1988, p. 33]. Companies basing their systems on other processors feared they might be handicapped in the race to offer 4.0 quickly, or faced with a Unix tuned to the Sparc architecture. But now Motorola and AT&T have let it be known that they are working together on Release 4.0 for Motorola's 68000-family microprocessors, as well as for Motorola's recently announced 88000 reduced-instruction-set-computer chips [*Electronics*, Feb. 18, 1988, p. 83].

Also jockeying for a share of the Unix work-station market are Advanced Micro Devices, Intergraph, MIPS Computer Systems, and National. "We are having discussions with a number of microprocessor vendors," says AT&T's Dale Hazel, district manager for Unix system business planning, in Summit, N.J.

One way that AT&T already works with microprocessor makers—as well as with software houses—is to provide them with early releases of a new Unix version so that they can get to work on porting it to non-AT&T architectures. The new twist this time around is the development of binary standards called Applications Binary Interfaces. These attempt to ensure that application programs running on one system based on a particular processor architecture have binary compatibility, enabling them to run without recompilation on other systems using that same processor.

All microprocessor vendors can get new Unix releases at the same time

Binary standards for several processors are already on the way. The ones for the Intel 386 and Sun Sparc are leading the pack, but Motorola has been working with Unisoft Corp., Emeryville, Calif., on one for the 68000 family since last year. Last month, the two unveiled a specification, which they are calling a binary compatibility standard. Three weeks later, Motorola and Unisoft announced that Motorola is acquiring a piece of Unisoft, which is speeding its work on Release 4.0 for Motorola's microprocessors.

"There will be an early-release program for vendors who are working with us on ABIs for their architectures," says Hazel. "The primary goal is to get Release 4.0 on as many microprocessor architectures as we can as fast as we can—and to do so in a way that ensures binary compatibility of applications for an architecture."

There already are "well-defined programs for the ABI on the 386 as well as the ABI on the Sparc architecture," he says. The current target is to have 4.0 ready on the AT&T 3B2 architecture—the processor it is being developed on—during the third quarter of 1989. The plan calls for having 4.0 available on the 386 and Sparc by the end of 1989.

For those with binary-standard agreements with AT&T, "we think we're providing [pre-releases] early enough in 1989 so that they have an excellent shot at getting [4.0] out there in roughly the same time frame" as the Sparc and 386 versions, says Hazel. *–Jeremy Young*

AUTOMOTIVE

FIRST HEAD-UP DISPLAYS SLATED FOR GM CARS

INDIANAPOLIS

Aerospace-style head-up-display technology will hit the roads for the first time in U.S. production automobiles this spring, thanks to the efforts of General Motors Corp. engineers steeped in both military optics and automotive electronic displays.

GM will show off its new technology at the Indianapolis Speedway here May 29 in a special version of the 1988 Oldsmobile Cutlass Supreme, this year's official Indianapolis 500 pace car. The dis-

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GPIB Power Supply Series $4500

Lambda's new LT-870 Series is a stand alone IEEE-488 GPIB power supply. It is designed with three internal PC cards allowing for voltage and current limit programming over the bus.

The Interface Card handles the communication over the bus. The Programming Card provides the appropriate D/A conversion necessary for voltage and current limit programming over the entire voltage range. The third card, the Interconnect Card, is designed with these rear panel features:

- 5-bit DIP switch for primary address selection.
- Pushbutton reset switch—to reset the voltage and current limit to zero.
- Auto/manual select switch sets the power supply for either local or computer control.
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The stand alone LT-870 IEEE-488 Power Supply is backed by Lambda's 5 year guarantee and is available for one day delivery from stock.

	MAX CURRENT AT AMBIENT OF (AMPS) 40°C	50°C	60°C	71°C	DIMENSIONS (INCHES)	PRICE	MODEL
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	300.0	266.0	218.0	160.0	$5\,^{3}/_{16} \times 19 \times 16\,^{1}/_{2}$	2750.00	**LT-821**
	500.0	450.0	400.0	325.0	$5\,^{3}/_{16} \times 19 \times 17\,^{1}/_{2}$	3200.00/4500.00	**LT-861/LT-871**
0-18 Volts	70.0	61.0	52.0	40.0	$5\,^{3}/_{16} \times 19\,^{3}/_{16} \times 8\,^{3}/_{8}$	1733.00	**LT-802**
	150.0	133.0	109.0	80.0	$5\,^{3}/_{16} \times 19 \times 16\,^{1}/_{2}$	2750.00	**LT-822**
	225.0	205.0	180.0	145.0	$5\,^{3}/_{16} \times 19 \times 17\,^{1}/_{2}$	3200.00/4500.00	**LT-862/LT-872**
0-36 Volts	34.5	30.5	26.0	20.0	$5\,^{3}/_{16} \times 19\,^{3}/_{16} \times 8\,^{3}/_{8}$	1733.00	**LT-803**
	80.0	71.0	58.0	42.0	$5\,^{3}/_{16} \times 19 \times 16\,^{1}/_{2}$	2750.00	**LT-823**
	115.0	104.0	92.0	75.0	$5\,^{3}/_{16} \times 19 \times 17\,^{1}/_{2}$	3200.00/4500.00	**LT-863/LT-873**
0-60 Volts	21.5	19.0	16.0	12.5	$5\,^{3}/_{16} \times 19\,^{3}/_{16} \times 8\,^{3}/_{8}$	1733.00	**LT-804**
	50.0	43.0	35.0	25.0	$5\,^{3}/_{16} \times 19 \times 16\,^{1}/_{2}$	2750.00	**LT-824**
	70.0	63.0	56.0	45.0	$5\,^{3}/_{16} \times 19 \times 17\,^{1}/_{2}$	3200.00/4500.00	**LT-864/LT-874**

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LT SERIES — Specifications

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Voltage range shown in table.

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CONSTANT

regulation, line	0.02% + 2mV for line variations from 187 to 242VAC (205 to 265VAC on "V1" option) for LT-800 series. 187 to 229VAC (207 to 253VAC on "V1" option) for LT-820 series. 0.05% for line variations from 187 to 265VAC for LT-860 and LT-870 series.
regulation, load	0.02% + 2mV on LT-801, 802, 821, 822; 0.02% + 4mV on LT-803, 804, 823, 824; 0.05% on LT-860 and LT-870 series for load variations from 0 to full load.
remote programming resistance	200Ω/volt nominal.
remote programming voltage	volt per volt.
ripple and noise	10mV RMS, 50mV pk-pk for LT-801, 821. 15mV RMS, 100mV pk-pk for LT-802, 803, 804, 822, 823, 824. 20mV RMS, for LT-860 and LT-870 series.
temperature coefficient	(0.02% + 50μV)/°C.

CONSTANT CURRENT
(Current regulated line and load) Automatic Crossover.

voltage range	as shown in Table.
current range	5% to full load current.
regulation, line	0.3% of Io(max) for line variations from 187 to 242VAC (205 to 265VAC on "V1" option) for LT-800 series. 0.3% of Io(max) for line variations from 187 to 229VAC (207 to 253VAC on "V1" option) for LT-820 series. 0.3% of Io(max) for line variations from 187 to 265VAC on LT-860 and LT-870 series.
regulation, load	0.3% of Io (max) for load variations from 5% to rated DC voltage.

AC INPUT

line	LT-800 series: 187 to 242VAC (205 to 265VAC on "V1" option), 47-63Hz. (Derate all ratings by 10% at 47-53Hz) LT-820 series: 187 to 229VAC, 3 phase ± 10% max phase imbalance, 4 wire, 47-63Hz (207 to 253VAC on "V1" option). (Derate 40°C ratings by 10% at 47-53Hz.) LT-860 and LT-870 series: 187 to 265VAC, 3 phase ± 10% max phase imbalance, 4 wire, 47-63Hz.
power	LT-800 Series: 1985 watts maximum. LT-820 Series: 4000 watts maximum. LT-860, LT-870 Series: 5000 watts maximum.

EFFICIENCY
Minimum 65% at maximum output voltage for LT-800 series, 70% for LT-820 series, 78% for LT-860 and LT-870 series.

INPUT CURRENT
18A RMS max on LT-800 series, 17A RMS max per phase on LT-820 series, LT-860 and LT-870 series.

OPERATING TEMPERATURE RANGE
Continuous duty from 0°C to 71°C with appropriate deratings from 40°C to 71°C.

STORAGE TEMPERATURE RANGE
−55°C to +85°C.

OVERLOAD PROTECTION
THERMAL
Thermostat protects unit from excessive ambient temperature as well as inadequate air velocity. AC power must be momentarily removed from unit after thermal shutdown in order to restore operation.

ELECTRICAL
External overload protection — adjustable, automatic electronic current-limiting circuit limits output current to preset value. Current-limiting setability to 105% of rated current via front panel adjust.

OVERVOLTAGE PROTECTION
Built-in, adjustable overvoltage protection is standard on all sets. When preset voltage is exceeded, the overvoltage protector crowbars the output and removes the inverter drive. AC power must be momentarily removed from unit after overvoltage shutdown in order to restore operation.

OVERVOLTAGE PROTECTION ADJUSTABLE RANGES

Model	Vov(Min)	Vov(Max)
LT-801/821/861/871	3.5V	10V
LT-802/822/862/872	6V	24V
LT-803/823/863/873	9V	47V
LT-804/824/864/874	12V	70V

IN-RUSH LIMITING CIRCUIT
Limits in-rush current at turn-on to 200% of full load peak current.

COOLING
Fan cooled. Forced air cooling utilizing all metal, shaded pole, ball bearing, long life fan. (No lubrication needed). Leave adequate clearance at all air intakes and exhausts. Exhaust is at rear of unit.

CONTROLS
DC OUTPUT CONTROLS
Coarse and fine voltage adjust and single current adjust on front panel.

OVERVOLTAGE PROTECTION
Overvoltage trip point set by screwdriver adjust on front panel.

POWER
On-off switch on front panel of LT-800 series. On-off circuit breaker on front panel of LT-820, LT-860 and LT-870 series.

INPUT AND OUTPUT CONNECTIONS
Heavy duty barrier strips for AC input, ground and sensing. DC output via bus bar at rear of chassis.

METERS
Digital panel meter standard on LT-800, 820 series. Monitors output voltage/current by means of a volt/amp selector switch on LT-800 series. Separate digital panel meters on LT-820 series allow simultaneous monitoring of output voltage and current. Separate analog meters on LT-860 and LT-870 series provide for simultaneous monitoring of output voltage and current. Additional LED on front panel of LT-870 indicates auto/manual operation.

LED STATUS INDICATORS
An overvoltage/overtemperature indicator lamp will light to notify the user of the occurrence of either an overvoltage or overtemperature shutdown condition. AC power must be removed from the unit to reset the power supply and the light. A line fault indicator with automatic reset indicates power loss or loss of a phase on LT-860 and LT-870 series.

REMOTE SENSING
Provision is made for remote sensing to eliminate effect of power output lead resistance on DC regulation.

REMOTE ON/OFF
Isolated terminals on LT-860 and LT-870 series allows for these remote functions: Turn-on — Logic zero, short circuit or open circuit; Turn-off — provide 5mA into ± R terminals.

EMI
Conducted EMI conforms to FCC 20780 class A on LT-800 and LT-820 series.

PHYSICAL DATA

Package Model	Weight Lbs. Net	Weight Lbs. Ship	Size Inches
LT-800 series	30	37	5 3/16 × 8 3/8 × 19 3/16
LT-820 series	70	82	5 3/16 × 19 × 16 1/2
LT-860, LT-870 series	60	72	5 3/16 × 19 × 17 1/2

OPTIONS
AC INPUT

Series Model	Add Suffix	For Operation at:	Price
LT-800	−V1	205 to 265VAC 47-63Hz	12%
LT-820	−V1	207 to 253VAC 47-63Hz	12%

ACCESSORIES
Pot Covers available on LT-800, LT-860 and LT-870 series. LRA-17 Rack Adapter available for LT-800 series. Chassis slides available for LT-820, LT-860 and LT-870 series.

GUARANTEED FOR 5 YEARS
5 year guarantee includes labor as well as parts. Guarantee applies to operation at full published specifications at end of 5 years.

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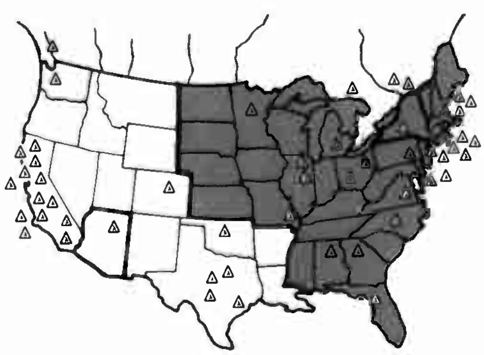

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2/88

capture or modify chip conditions on the fly during system operation.

By shifting in test commands along with diagnostic data, critical states of ICs are precisely tracked and controlled. Doing so could potentially reduce by an order of magnitude the number of clock cycles needed to set up exact conditions inside the circuit, says Michael J. Miller, who developed the concepts.

IBM's original concept of Level Sensitive Scan Design, which gives each register a dual purpose (test and normal operation), is widely used in semicustom chips. But IDT thinks the IBM approach is too heavily oriented toward component-level testing. "We have oriented it for chip- and system-level test. The ability to shift in commands has turned the function into an active element instead of a passive element of previous methods," says Jordan.

IDT is going public with the full-purpose Serial Protocol Channel block in March, announcing a new register-packing 4-Kbit-by-16-bit static random-access memory, the IDT71502. The 35-ns 64-Kbit SRAM is believed to be the first monolithic writable-control storage SRAM, replacing 10 chips in most applications. It sells for $44 each in 100-piece lots. IDT will also announce a fast CMOS octal register part with the channel, the IDT49FCT818, which sells for $3.35. It is to become a key building block for equipment using IDT's scan-path technique in board- and system-level tests. Last fall, IDT announced a 16-Kbit electrically erasable PROM, but the firm promoted the feature then mostly as an additional programming channel, keeping a low profile on the testing aspect. *–J. Robert Lineback*

COMPUTERS

IBM TO MAKE FIRST OEM MOVE, AND IT'S WITH FERRANTI

MANCHESTER, UK

After quietly pursuing original-equipment-manufacturer agreements for its PS/2 computer line, IBM Corp. is about to sign the first one—with Ferranti International plc of England. The OEM strategy is a keystone of IBM's battle to fend off competition from Digital Equipment Corp. and Apple Computer Corp., as well as to stymie the erosion of its market base by low-cost clones of its earlier PC AT and XT personal computers.

IBM will not confirm that negotiations with Ferranti have been going on. But industry watchers believe that there may already be a second deal in the works, with speculation centering on

Silicon talks.

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Our MC68000 Family offers three different protocol controllers to handle all your data communication needs; whether it's across the building or around the world there's a Motorola device that will make your job easier. With our '68000 Family you can choose the protocol and system designs that get you on line quickly and economically.

X.25 Protocol Controller 1984 CCITT X.25 LAPB.

The MC68605 Protocol Controller (XPC) implements the 1984 CCITT Recommendation X.25 Link Access Procedure Balanced (LAPB) for U.S. and European T1 applications. By generating link-level commands and responses, the XPC relieves the host processor of communication link managerial tasks. It's also fully DDN and Telenet certifiable.

Our XPC features an optional transparent mode which allows the implementation of other HDLC-based protocols, with user generation of all frames. The XPC handles full-duplex synchronous serial data rates up to a maximum 10 Megabits Per Second (Mbps) for high-speed computer links.

Multi-link LAPD Controller CCITT Q.920/Q.921 LAPD.

The MC68606 Multi-link LAPD (MLAPD) Protocol Controller fully implements CCITT Recommendation Q.920/Q.921 Link Layer Access Procedure (LAPD) protocol for ISDN networks. The MLAPD is designed to handle both signalling and data links in high-performance ISDN primary rate applications.

This VLSI device provides a cost-effective solution to ISDN link-level processing with simultaneous support for up to 8K logical links. The MC68606 is an intelligent communications protocol controller compatible with AT&T specifications for ISDN devices and features low power consumption and high performance, with an aggregate data rate in excess of 2.048 Mbps.

Token Bus Controller IEEE 802.4 MAC.

The MC68824 Token Bus Controller (TBC) is the only single-chip solution to implement the IEEE 802.4 Media Access Control (MAC), specified by Manufacturing Automation Protocol (MAP). The TBC implements four levels of message priority and the Request With Response (RWR) frame type to meet the real-time needs of factory floor communications and MAP 3.0.

The TBC conforms to the IEEE 802.4G standard MAC to Physical layer serial interface to support broadband, carrier-band, and fiber optic networks. The TBC's low power consumption coupled with its extended temperature range versions make it ideally suited for factory automation applications.

Token Bus Frame Analyzer Software speeds development of token bus networks.

The MC68KTBFA Token Bus Frame Analyzer Software (TBFA) is a real-time software tool that speeds development of token bus networks. The TBFA keeps track of statistics while monitoring network performance. By using the simple menu-driven interface, the user can define triggers to selectively store and display frames, creating a powerful tool for network analysis.

The TBFA is a set of four EPROMs which runs on a VMEbus MVME372 Token Bus Controller board and requires a modem, a VT100 terminal, and a power source. The cost-effective TBFA sells for about one-tenth the cost of existing token bus protocol analyzers.

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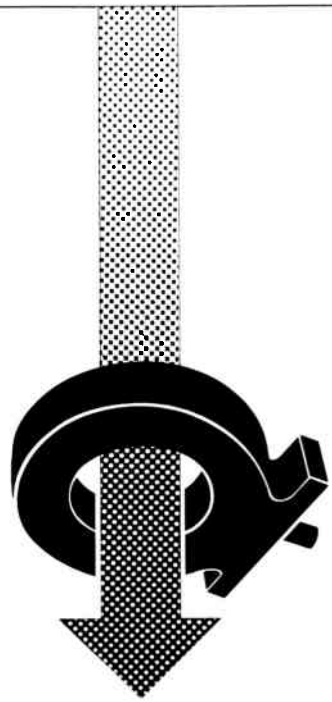


the audio information without contact. With DAT, by contrast, there's tape-to-magnetic head contact and tape abrasion. And not only can the MOD disks record, but they also have information on both sides. Uhde's team is now working to increase the information content from the present 54 minutes per side, possibly to two hours.

Also, Thomson's researchers are looking into the possibility of using MOD for data storage. It could provide advantages over floppy disks and magnetic tape because of its larger storage capacity, its freedom from wear and tear, and its relatively fast random access. Work in that direction is also going on in Japan and the U. S.—for example, at Nippon Kogaku K. K. (Nikon) in Japan and IBM Corp. and Carnegie Mellon University in the U. S. [*Electronics*, April 16, 1987, p. 33]. *–John Gosch*

GE DIGITAL VIDEO STANDARD GETS STRONG BACKING

NEW YORK

In the emerging market for interactive video systems based on compact-disk technology, General Electric Co. has gotten its nose out in front by signing up a microprocessor maker and two software houses to work with its standard. At least one expert believes that if GE's pricing matches its timing, the rival Philips-Sony Corp. technology could be in trouble.

Joining GE to back its Digital Video Interactive, or DVI, standard are Intel, Lotus, and Microsoft. A GE spokeswoman says that Intel Corp. will work to make DVI compatible with its microprocessor architectures and that Lotus Development Corp. and Microsoft Corp. will be involved with application software packages. GE also says it will deliver this month DVI prototypes to 10 of the 50 software companies that are exploring application products. All of the potential products will be for commercial use. One, for example, is a design operation for furniture makers and dealers, and another is a retail point-of-purchase system. Products should start appearing in the early 1990s, GE says.

The Philips/Sony duo, which calls its technology Compact Disk-Interactive, or CD-I, said last fall that it would have products this year [*Electronics*, Nov. 26, 1987, p. 92], but the two companies say now that their target is 1989.

"GE's move does not affect our short-term plans at all," says Joop Witvoet, director of communications in Philips's New Media Systems Division in Eindhoven, the Netherlands. "Our system is oriented more toward the consumer and institutional sector, not so much toward the professional market, as is GE's."

But they should check with GE. The spokeswoman says that the company views DVI as a consumer product, unlike Philips/Sony. What's more, DVI has a built-in advantage: it can deliver 72 minutes of full-motion video, computer graphics, or audio and graphics on standard read-only CD. On the other hand, CD-I offers only partial animation. "If you can get partial animation or full motion for the same price," asks industry watcher David Lachenbruch, editor of *TV Digest*, "why go for the Philips/Sony version?" *–Howard Wolff*

WITH ANTI-COPY CHIPS DEAD, A NEW DAT BATTLE IS BREWING

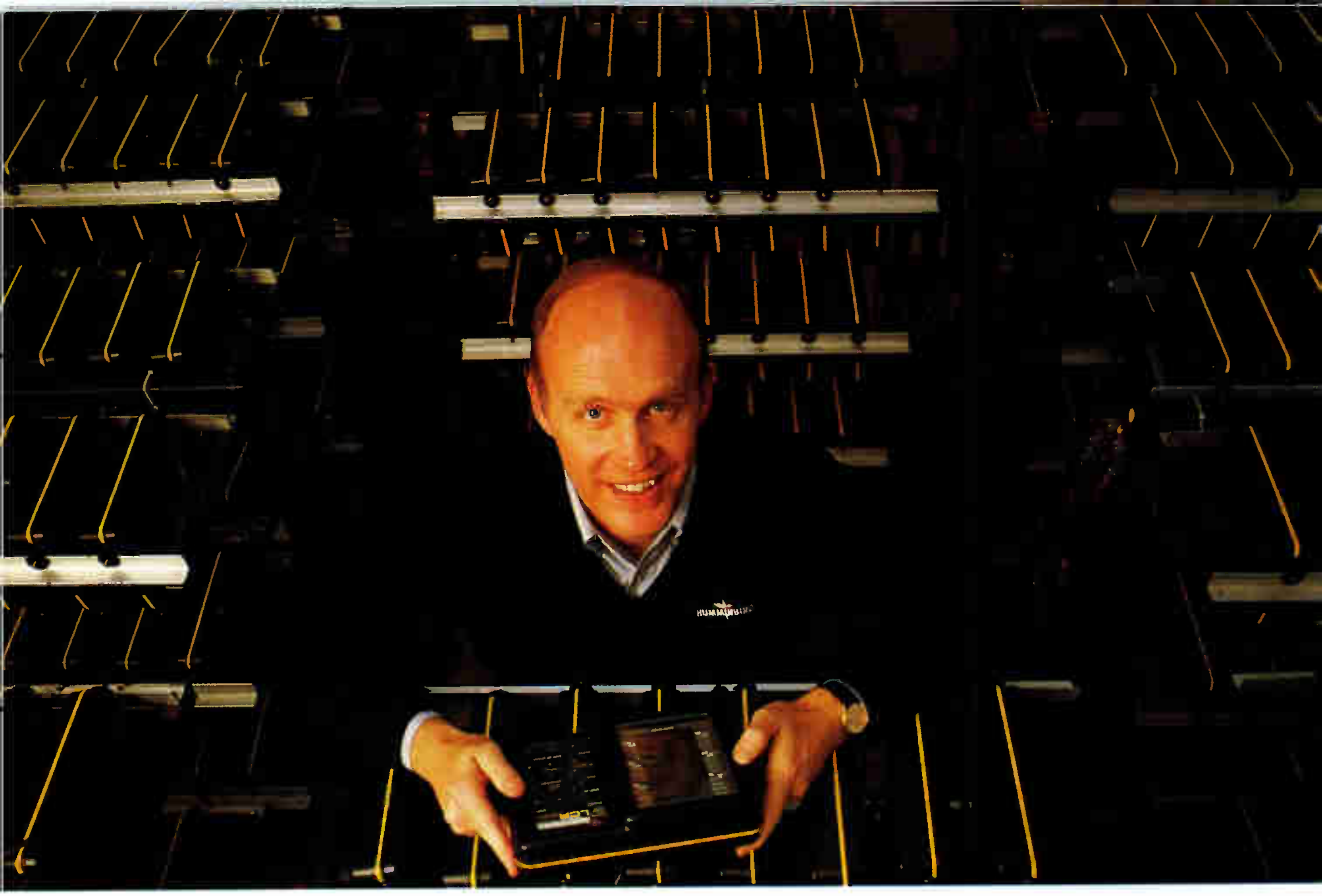
CHICAGO

The recording industry is digging in for a renewed battle over digital audio tape, following the release of a five-month-long government study showing that proposed DAT copy protection chips don't always work, degrade music quality, and are easily circumvented.

The findings reported this month by the National Bureau of Standards effectively kill the idea of federal legislation mandating use of the chips in U. S.-sold DAT recorders. But the NBS didn't settle the record industry's objections to DAT. And in the wake of the March 1 report, the response from big-name consumer hardware vendors is uncertain. Major manufacturers led by Sony and Philips are said to be meeting this month to work out a consensus position on how they should respond.

The recording industry had backed the legislation, which would have required the vendors to use the CBS-designed chip that was shot down by the NBS. But the music industry is not backing down.

"We're as committed as ever to finding a solution to the home taping threat posed by DAT, and resolving that, and then having DAT introduced," says Jason S. Berman, president of the Recording Industry Association of America, Washington D. C. "But in the interim, [before a solution is reached] it's clearly our intention to sue if the machines are introduced here," Berman says. The RIAA views DAT as a copyright threat, since a DAT machine that does not have



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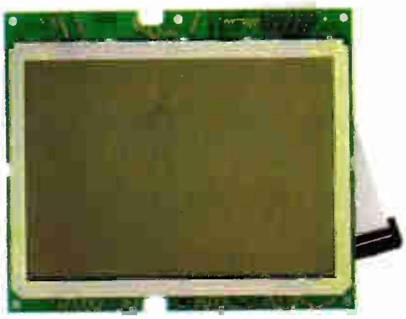

And the best part is, we never have to ask for it."

"Hitachi makes it clear that their most important product is our product."
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To learn about how partnering with Hitachi can benefit your company, call Tom Klopcic or David Ross at (312) 843-1144. Or write to Hitachi America, Ltd., Electron Tube Division, 300 N. Martingale Road, Suite 600, Schaumburg, IL 60173.

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some means of copy protection can be used to produce near-master-quality reproductions of prerecorded material.

A threatened RIAA lawsuit aside, some smaller consumer-audio vendors are pushing ahead with U.S. DAT marketing plans. Harmon America, of Woodbury, N.Y., says its $2,199 Citation 26 DAT machine will be on store shelves here by June. And Casio Inc., of Fairfield, N.J., is planning to test market its $1,399 portable DA-1 machine in the U.S. in April.

At Marantz Co. in Chatsworth, Calif., president James Twerdahl is hopeful the NBS decision will send a signal to Japanese component and system suppliers that the coast is now clear for U.S. DAT sales. Marantz has been promising to market DAT hardware here for nine months. But the firm has been unable to produce because of broken commitments by Japanese suppliers, Twerdahl says. "We're now saying that we will import DAT from any OEM suppliers willing to supply us, if our original suppliers have cold feet," he declares.

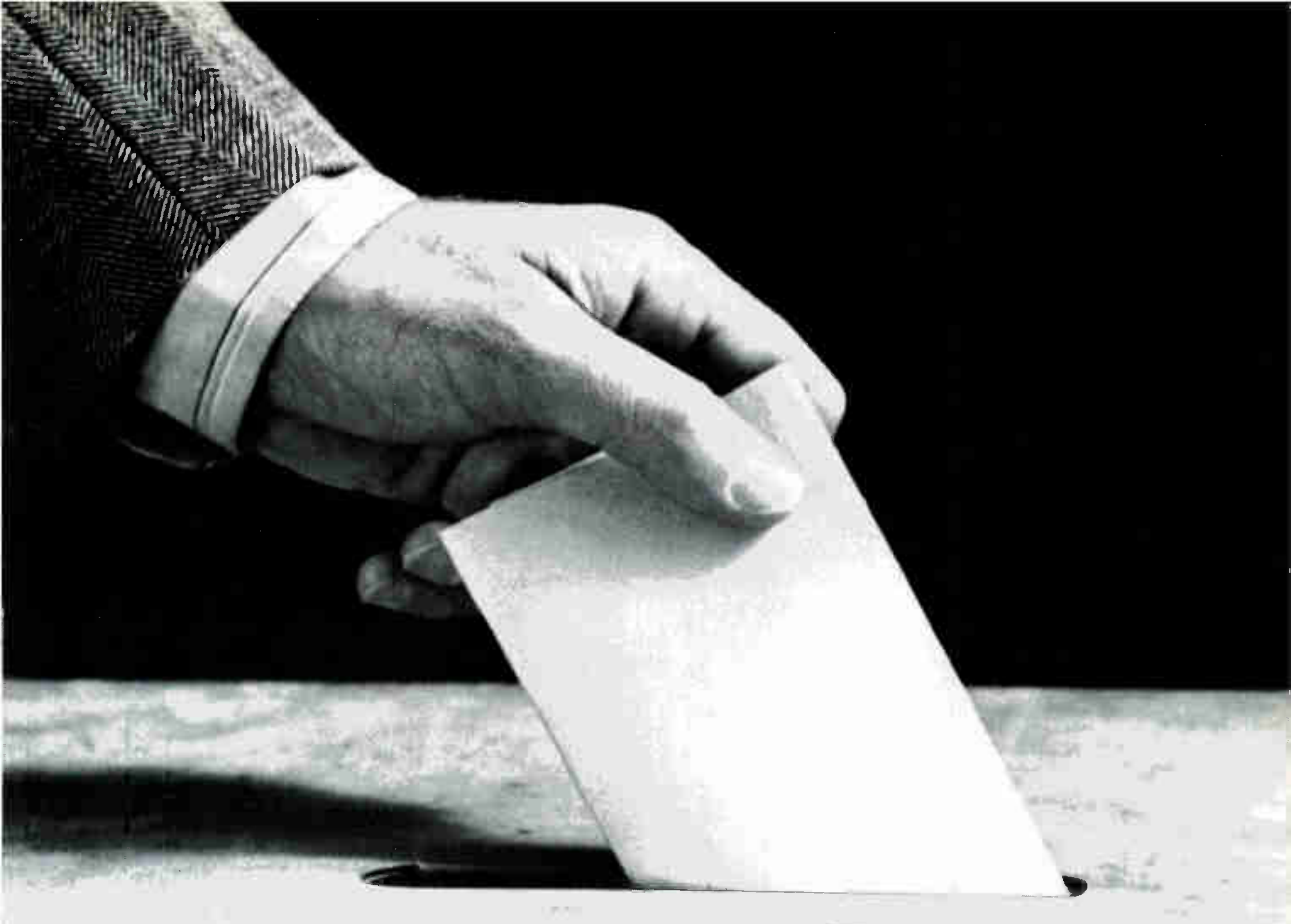
> 'DAT suppliers know where to get ahold of me,' says the record makers' point man

However, makers of major brands have been slower to react. "The NBS decision certainly didn't tell us anything we already didn't know," says a Sony Corp. of America spokesman in Park Ridge, N.J. Sony is "still looking at the U.S. market and what kind of products we want to bring here." The firm has nothing yet to say about introduction dates.

Indeed, some U.S. observers believe that much could hinge upon the outcome of meetings overseas among the major Japanese and European DAT suppliers, led by Sony and Philips. And the RIAA's Berman, for one, says he hopes that the vendors are developing a consensus on how to negotiate a solution to the problems the record industry sees with DAT. "I said before the NBS report that I would be prepared to negotiate with them on a solution without being bound to the copy-code chip," Berman says.

Berman is noncommittal on what such "solutions" might be. But in the past, the RIAA has supported a royalty on U.S. sale of blank DAT software. And the organization has also proposed an alternative technology known as Unicopy that would limit a DAT recorder to making a single copy of a prerecorded source.

"We're encouraged by the fact that the hardware manufacturers are meeting," Berman says. "I'm here. They know where to get ahold of me, that's for sure. And we'd welcome the opportunity to sit down with them." *–Wesley R. Iversen*



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Reliability is critical in 32-bit systems. The V70 is ideal for designing fault-tolerant systems with its unique on-chip Functional Redundancy Monitor. Use two V70's, one master and one checker. During each bus cycle the checker monitors the master and issues mismatch warnings.

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NEW AUTOMATED INTELSAT EARTH STATION

The 3rd INTELSAT standard-A earth station by Singapore Telecom heralds a new generation of satellite communications systems with advanced automatic operation and maintenance capabilities.

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Our Computerized Supervisory and Control System (CSCS) allows the operator to centrally control, monitor, and report on the operating status of equipment and circuits with utmost efficiency.

The System Testing Facility (STF) automatically executes line-up tests with other earth stations and also performs in-station loop tests and on-line monitoring of essential carrier parameters. The STF handles virtually all in-station testing, from the selection of a measuring route to the preparation of test reports.

Moreover, the Bukit Timah earth station is equipped with our Time Division Multiple Access/Digital Speech Interpolation (TDMA/DSI) equipment for maximum utilization of satellite circuits.

For coverage of the Pacific Ocean region, the Bukit Timah No. 2 earth station is also under construction by Singapore Telecom and NEC is supplying similar advanced systems.

FIRST CCD CAMERA DESIGNED FOR FIELD PRODUCTION

Following up the success of the SP-3A for news gathering, NEC introduces the EP-3, the first CCD color camera (NTSC system) expressly designed for field production.

Incorporating exclusive high density CCD sensors, the 2nd-generation solid-state camera goes head-to-head with any tube-based portable in picture quality. It offers 700-line horizontal resolution, 62dB S/N ratio and F5.6/2,000 lux sensitivity.

The threshold illumination level is 15 lux (+18dB gain).

The new field production camera features virtually no smear and a 7-speed electronic shutter (1/60 – 1/1,500 sec) thanks to NEC's anti-smear, interline frame transfer CCD technology.

The EP-3 camera has a host of sophisticated control functions to support the creativity of videographers. Its automatic functions include White Balance with two memories, Auto Black Balance and Auto Iris/Auto Black Level.

The EP-3 also provides complete flexibility in operation. It is remotely controlled via multicore, triax or wireless systems. For recording, either Beta or MII-format VTR is attached.

NEW OEICs TRANSMIT 52KM AT 1.2 GBPS

Optoelectronic ICs developed at the NEC Optoelectronics Research Laboratory were successfully tested in a recent experiment using a 1.3μm optical single-mode fiber. The new OEICs set a world record for high-speed, long-distance transmission without repeaters – 52.5km at data rates of 1.2Gbps.

The transmitter OEIC delivers over 10mW in output power with a low 13mA threshold current. Modulation up to 2.4Gbps is possible in the NRZ mode. The 350 x 900μm chip integrates a buried type InGaAsP laser diode and high-speed driver (3 GaAs MES FETs) on the same InP substrate.

The receiver OEIC features –26dBm sensitivity. It packs an InGaAs PIN photo-diode and low-noise amp (4 GaAs MES FETs, 5 GaAs Schottky diodes and one resistor) on a 1 x 1mm InP chip.

The new high-performance OEICs are expected to play key roles in terminal equipment for the emerging optical broadband ISDN and optical networks between cities or within intelligent buildings.

Connected where it counts

The TRW MIMIC team has more than just expertise in producing low-cost MIMIC chips.

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INTERNATIONAL NEWSLETTER

CHIPS FOR CLONING IBM PS/2 PCs WILL SOON GO ON SALE IN JAPAN

Japanese computer makers who want chip sets for building personal computers compatible with IBM Corp.'s PS/2 products will be able to get them from Kanematsu Semiconductor Corp., a leading semiconductor trading firm. By the end of March, the Tokyo company will start marketing chips for clones of the PS/2 model 30, to be followed by others for copies of the model 80. The chips were designed by Oak Technology Inc. of Santa Clara, Calif., which has sold Kanematsu the rights to market them in Japan only. The set will include a chip for graphics compatible with IBM's VGA, EGA, and CGA adapters. Samples of chips for building a low-cost version of the 386-based PS/2 model 80 will be available in September. This low-end system design has reduced addressable memory and a 16- or 20-MHz clock—and no cache memory. Chips for Oak's high-end 386-based design will support cache, more memory, and a 25-MHz clock, but the schedule for these chips is not yet set. Volume production of the model-30 chips will start in May or in June at a Japanese manufacturer that Kanematsu won't disclose. □

X-RAY RESIST MATERIAL ALLOWS RAPID EXPOSURE OF FINE STRUCTURES

An important milestone in West Germany's national X-ray lithography project [*Electronics,* Feb. 5, 1987, p. 78] has been reached: Frankfurt-based chemicals-producer Hoechst AG has developed an X-ray resist material that allows chips to be made with structures down to 0.3 μm. The new resist—Hoechst declines to reveal its composition—boasts a sensitivity so high that it cuts X-ray exposure times down to about one minute, from the one hour or so common for conventional resists. The fine structures should enable chip makers to produce 64-Mbit memories and other high-density devices, the goal of Europe's Jessi venture [*Electronics,* Feb. 4, 1988, p. 51]. □

TWO TROUBLED ISRAELI ELECTRONICS COMPANIES MOVE BACK IN THE BLACK

Two of Israel's leading high-tech companies, Elscint Ltd. and Scitex Corp., have returned to profitability for the first time in years. The most dramatic turnaround was that of Elscint, the Haifa-based producer of medical-diagnostic imaging equipment. After the largest loss in Israeli corporate history—$116 million for the 1985-86 fiscal year—it appeared that Elscint would have to shut down. A new managing director, former Israeli Air Force commander Benny Peled, was brought in, and now Elscint is reporting a $300,000 profit on sales of $42 million in the quarter ending last December. Company officials attribute Peled's success to a massive reorganization and his decision to drop X-ray systems to concentrate on more sophisticated products. For its part, Herzeliya-based Scitex, a maker of imaging equipment for the printing industry, reported a $1.8 million net profit for the quarter ending in December. Its 1987 losses were $4.6 million, compared with $34 million for the previous year. Scitex sales are up 20%, a comeback due in part to good market conditions, including favorable changes in currency exchange rates. □

PHILIPS AND EUROPEAN SILICON STRUCTURES STRIKE A WORLDWIDE ASIC DEAL

Fast-turnaround prototypes of CMOS application-specific integrated circuits are now available to customers of Philips, following an agreement between the Dutch company and European Silicon Structures. ES2, a specialist in ASICs [*Electronics,* Sept. 16, 1985, p. 30], will apply its proprietary electron-beam direct-write processes for fast prototyping to Philips's standard 1.5-μm dual-layer-metal CMOS technology. When a customer is satisfied with the prototypes produced at ES2's factory in France, Philips can then produce the devices in volume at five plants in Europe, the U. S., and the Far East. □

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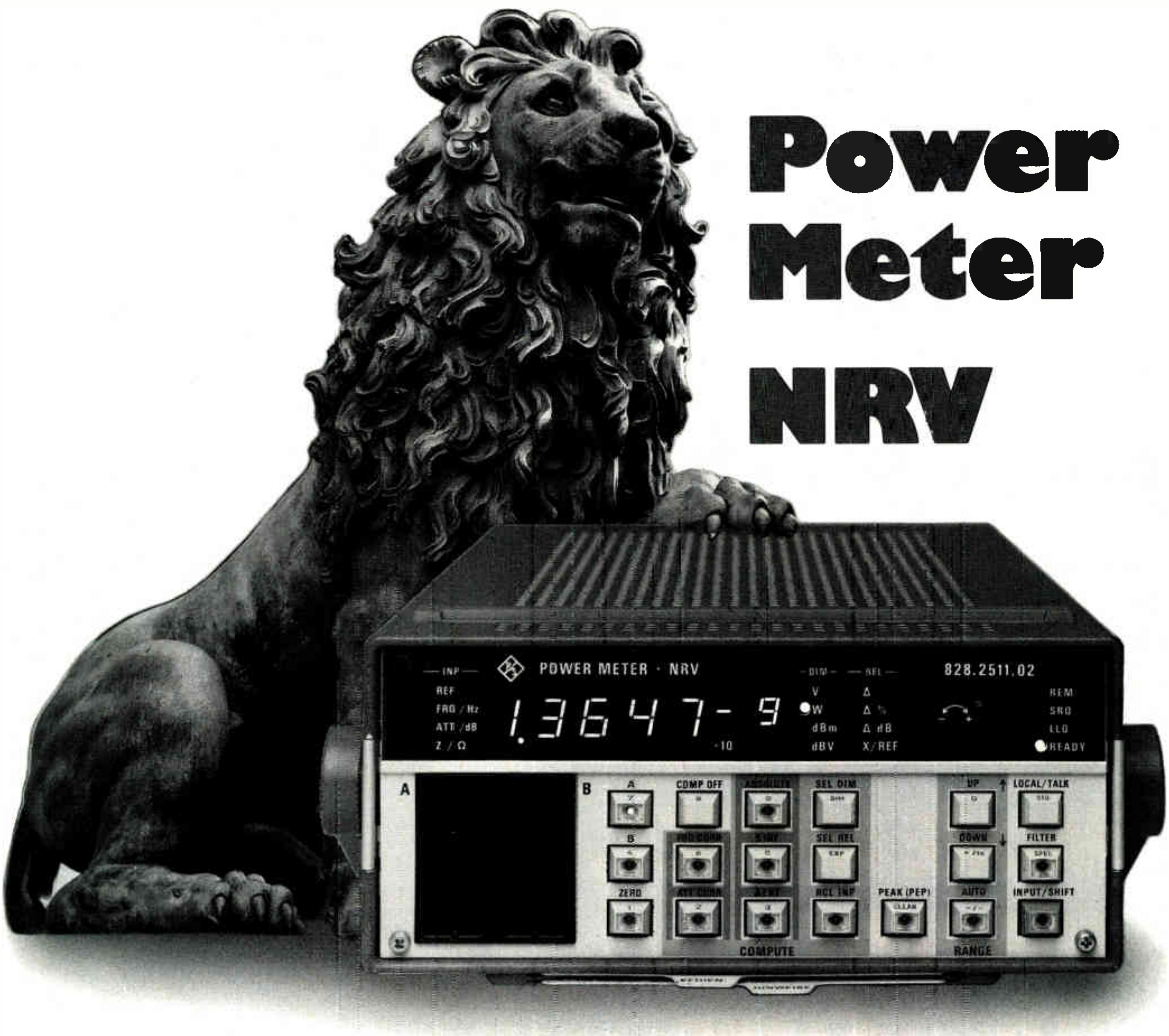

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INTERNATIONAL WEEK

EUROPE DRAWS UP TELECOM TIMETABLE

A tight timetable for unifying European telecommunications markets to open up competition has been drawn up by the Commission of the European Communities (CEC). The market for receive-only satellite antennas will be open for transborder competition by Dec. 31, 1989, and the terminal-equipment market will be opened a year later. Other moves will ensure a common formula for setting telecommunications tariffs and policies to ease protectionist policies.

SANYO'S TI PACT EASES TRADE TENSION

A technology agreement between Sanyo Electric Ltd., Osaka, and Texas Instruments Inc. to develop image-processing LSI chips seems likely to help mitigate trade tension between Japan and the U. S. The project is in line with the Ministry of International Trade and Industry's instructions to Japanese manufacturers to increase imports of U. S.-made semiconductors. When device development ends later this year, TI divisions in either Dallas or Tokyo will manufacture the LSI chips. Sanyo will buy them for use in its video cassette recorders and other products.

GROUPE BULL UNVEILS THREE MAINFRAMES . . .

France's Groupe Bull is aiming to increase its share of the transaction-processing market with the addition of three new mainframes. The new DPS 7000/72 biprocessor and the 82 and 92 quad-processors fill in a gap in power between the Bull DPS 7000/50 and the large Bull DPS 7/1007. Their transactional power is between 17 and 34 debit-credit-TPI-type transactions/s. The three new models will provide small-mainframe users with the same benefits of fault transparency as the large redundant mainframes on the market, the company says. Prices range from 2 million to 5 million French francs.

. . . AND BEEFS UP ITS PC LINE

Groupe Bull is also targeting a bigger share of the personal computer market with major upgrades. The Bull Micral 75 is twice as powerful as any PCs currently offered by Bull. Built around an Intel 80386 microprocessor, it can handle Windows 386 and run under OS/2 or as a multiple station system under Prolog. The new Bull Micral 45 is a midrange, compact, single station system, built around an Intel 80286 microprocessor. It operates under OS/2 with 3½-in. disks and new application programs. Prices start at 51,800 French francs.

TRAINS AND PLANES TO GET TV SERVICES

Philips of the Netherlands and the U. S.'s Warner Brothers Inc. have formed a 50-50 joint venture, Airvision, that will sell and service video entertainment and data information systems for public transportation companies. The Dutch firm will supply liquid-crystal screens for installation between or on the back of seats on airplanes, trains, buses, and taxis. For its part, Warner will provide Los Angeles-based Airvision with programs from its own libraries, including films, sports, and news programs.

FOUR FIRMS AGREE ON ISDN INTERFACE

Four European communication equipment makers—France's Alcatel NV, Italy's Italtel, the UK's Plessey Ltd., and West Germany's Siemens AG—have agreed to use a standard interface between components for integrated services digital network systems. The standard, called General Circuit Interface, makes the present ISDN Oriented Modular Interface upwardly compatible.

IBM FRANCE FINDS A NETWORK PARTNER

To bolster its position in the the growing networking market, IBM France is marrying its networking skills to the French Société d'Etudes des Systèmes d'Automation SA's systems-integration expertise. The as-yet-unnamed joint venture company will be 51% owned by SESA, a subsidiary of Cap Gemini Sogeti, and 49% by IBM France.

NEC WORK STATIONS GET CAD CAPABILITY

NEC Corp., Tokyo, is marketing a computer-aided engineering system based on Visula, the popular CAE software package for printed-circuit-board design, developed by Racal-Redac Ltd., Tewkesbury, UK. Modified to run on NEC's EWS 4800 series engineering work station, Visula automatically designs wiring for high-density printed-circuit boards with surface-mounted devices on one or both sides, and has sufficient precision for designs with minimum line spacing of 0.01 μm. It costs 7.52 million yen for circuit design and 25.88 million yen for both design and layout.

NIXDORF AUTOMATES CHINESE POST OFFICES

Nixdorf Computer AG is gaining a beachhead in China's market for banking terminals and related equipment by supplying a distributed-transaction-processing system to the Chinese Ministry of Posts and Telecommunications. The Paderborn, West Germany, company will computerize five post offices in each of three cities—Beijing, Shanghai, and Canton—with a total of 33 Nixdorf 8810-based intelligent banking terminals and 15 Chinese-language printers plus other peripheral devices.

BBC'S VIDEOTEX GETS HIGH-RES GRAPHICS

The British Broadcasting Co. is leasing part of the bandwidth of its Datacast teletext service to Bishopsgate Terminals Ltd. of Guildford, Surrey. Bishopgate's complete turnkey service will provide high-resolution graphics encoded to the North American Presentation Level Protocol Standard. A Matra-Harris graphics-decoder chip handles the decoding chore. Capable of burst data rates up to 8 Mbits/s, Datacast is an extension of broadcast teletext and uses spare television raster scan lines to broadcast data during the TV picture's vertical blanking interval.

UK FIRMS TARGET COMPUTER SECURITY

A joint venture between British Telecom and Systems Designers plc is aiming at the computer-security market. The partnership will be known as Secure Information Systems Ltd. (SISL), and it is a finalist for the the UK Ministry of Defence's Corporate Headquarters Office Technology System—destined to be one of the largest secure systems in Europe.

TOYOTA TO MARKET ROBOT LINES

Toyota Motor Corp., Toyota, Japan, is pushing into the market for factory-automation equipment with welding and coating systems. The systems will use robots supplied by Toyota's affiliated firm, Toyoda Machine Works Ltd., Kariya, and other manufacturers. The car maker moved into electronics last year when it invested in Sanritz Automation Co., Tokyo, a microcomputer engineering venture, which will also take part in the project, providing microprocessor system and equipment design assistance.

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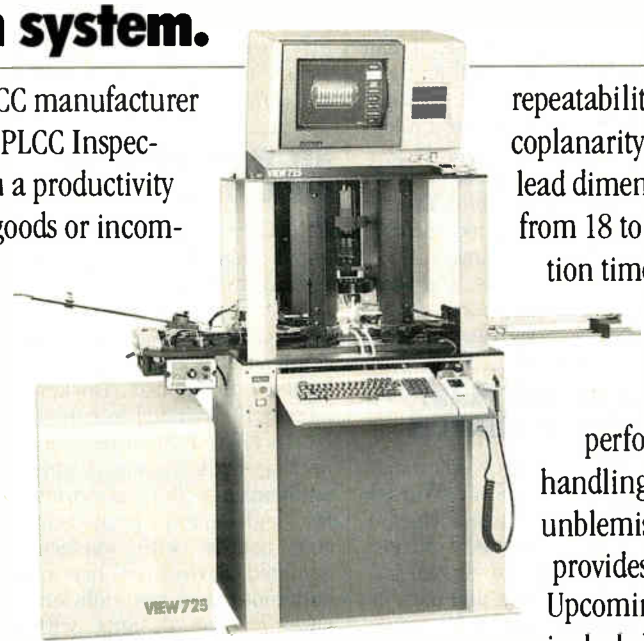

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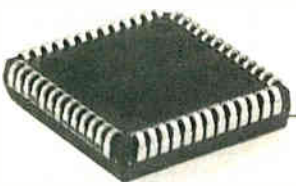

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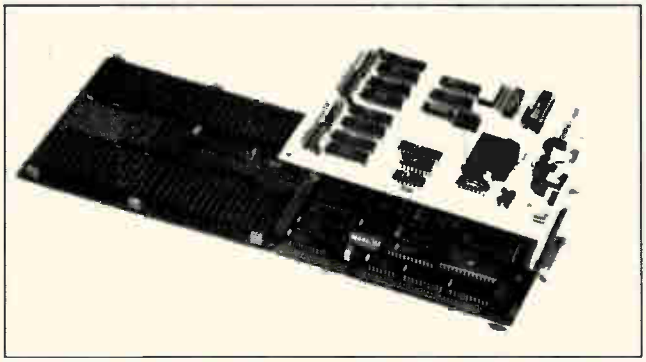
INTERNATIONAL PRODUCTS

PLUG-IN CONTROLLER TURNS PC AT INTO HIGH-END GRAPHICS WORK STATION

W. German module draws 12.5 million pixels/s at 2,048-by-2,048-resolution

A modular graphics controller from Projekt-Team Electronic GmbH turns an IBM Personal Computer AT or compatible into a high-end graphics work station capable of resolution up to 2,048-by-2,048 pixels and drawing speeds of 12.5 million pixels/s. But what should impress potential customers as well is the price of CAD-Genius—20% to 30% less than the competition.



The graphics controller attains a computing speed as high as six million instructions/s and a drawing speed of 12.5 million pixels/s.

Aimed at original-equipment manufacturers, the basic controller consists of a processor board and a video board. The processor gives a 2,048-by-2,048 pixel resolution with a pixel depth of four bits, producing up to 16 colors; or 2,048-by-1,024 pixel resolution with pixel depth of eight bits for 256 colors.

That performance for a single processor board puts PTE's system among the frontrunners in the graphics controller field, says Harald Buchberger, the company's managing director. Most competing graphics controllers require two or more processor boards for the same resolution. Eliminating extra board space puts PTE's prices in front of the competition's.

50-MHz CLOCK. By using a fast 32-bit 34010 microprocessor from Texas Instruments Inc. as its central processing unit and operating at a 50-MHz clock frequency, the controller attains a computing speed as high as 6 million instructions/s and a drawing speed of 12.5 million pixels/s, says Buchberger. A fast interface allows controller-to-host PC data transmissions at 40 Mbits/s. For complex mathematical operations, PTE offers as an option a mathematical coprocessor for the controller.

The controller's modularity makes it easy to upgrade and configure according to an OEM's requirements. At present, it is possible to connect in parallel up to four processor boards. A four-board configuration offers 2,048-by-1,024 resolution with a 32-bit pixel depth—which delivers more than 16 million colors or gray shades—and an overlay with an eight-bit pixel depth. That configuration allows pictures to be shown with all details and near-absolute faithfulness.

Since PTE's system has its own CPU, the controller itself is a computer. When it's integrated into an AT-class PC, the latter offers users the advantages of a high-resolution graphics computer and, at the same time, the proven PC/AT technology.

PTE is targeting CAD-Genius for OEM applications in high-performance personal computers that handle computer-aided design and desktop publishing. The advantage it has in such applications stems from the CPU. Using the built-in processing power, the CAD-Genius builds up an image while the PC goes about its regular tasks. For example, it can pick out certain picture segments or it can reposition the cursor to the desired spot. Because it offloads graphics chores from the PC AT and lets the PC handle other computations, the CAD-Genius should help accelerate the use of personal computers for complex CAD applications and desktop publishing tasks, says Buchberger.

Other PCs, even fast types of the AT class, are too slow to be standalone systems for many CAD jobs. And while a picture is created on the monitor, the PC cannot process other tasks. That lengthens time required to do a design job.

The controller supports more than 30 graphics output functions—from drawing pixel-thick lines, arcs, and polygons to initiating graphics environments, video timing, and screen refresh. It also handles various color palettes, pixel array, and cursor control functions, and performs viewport management. Further, it takes care of three-dimensional transformation, text output, text-attribute inquiry and control, and graphics system initialization.

It is this wide-ranging capability that makes Buchberger see a big market ahead for high-resolution graphics controllers. That market, he says, should grow at a rate of 300 to 400% a year in the near future, reaching at least 25,000 to 30,000 units sold worldwide next year alone.

Buchberger forecasts 500 CAD-Genius controllers to be sold this year and around 1,500 units in 1989. The company plans to enter the U.S. market via a sales representative this year. PTE is a $3 million, 25-man engineering firm in Ober-Ramstadt, near Frankfurt.

Operationally, CAD-Genius requires only that the PC transfer the necessary commands to the graphics controller. Command transfer goes from an interface to a first-in first-out buffer and then to the controller's CPU. A V.24 interface connects the controller to a mouse or digitizer.

TWO MEMORIES. The controller's processor board contains two memories: a picture memory and a program memory, each with a capacity of 2 Mbytes. The program memory is implemented with 1-Mbit dynamic random-access memory chips and the picture memory with 256-Kbit video dynamic RAMs.

The picture memory stores the pixels either in an x-y format or in a linear format. The PC AT's monitor presents to the user a section of the picture memory's contents, the size of the section depending on the resolution available from the monitor. As for the program memory, the user can read into it his own C-language graphics program. Pictures, segments of pictures, and menus can also be written into the program memory.

The controller's video module processes the various pixel depths and delivers the red-green-blue signals to the moni-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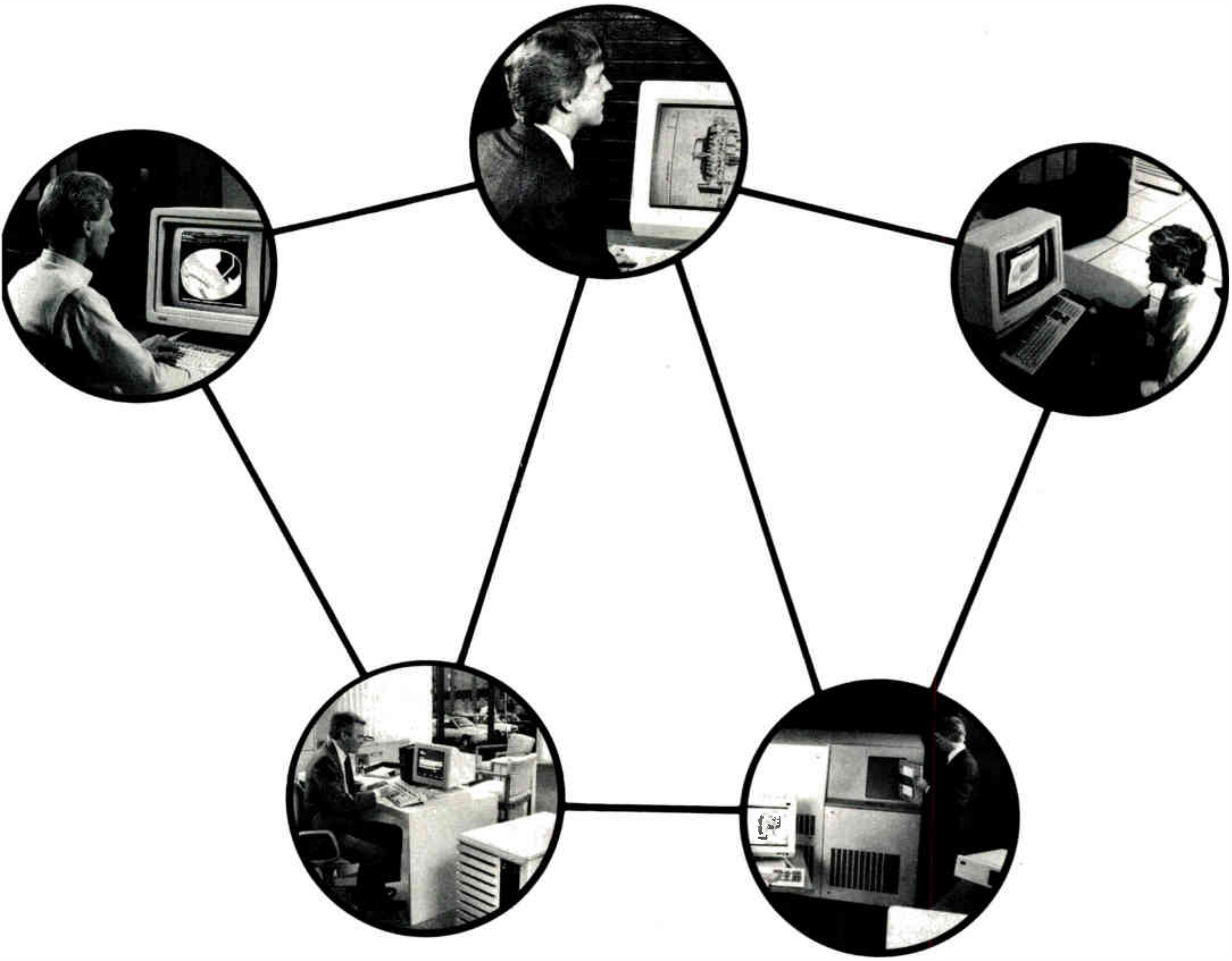

The promise of networking is fast becoming a reality. New VLSI circuits are now making low-cost networks feasible. Advances in fiber-optics are bringing fiber nets beyond telecommunications and into the local-area network arena. And new software programs are providing the tools necessary to manage and control these networks.

On April 14, the editors of *Electronics* will devote an entire special issue to the latest developments and technology trends in networking. We'll examine all the practical aspects encompassing local-area nets. The strategies that companies are embracing for connecting workstations with mainframes. Explore the status of Ethernet, X-open, OSI, and FDDI. And have an exclusive look at the latest entries in network chips, fiber optics, and network software.

If you manufacture products with network applications, it's an important opportunity to have your features and capabilities share the spotlight as we devote an entire issue to what's happening in networks. Be there!

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Thinking of getting into bed with RISC?

If you're looking for a cost-effective way to add a commercial high-end multiuser computer to your product line, you're probably looking at RISC. Should you be?

After all, how can you leverage your present investment in 680X0 family software with a non-compatible RISC product? You can't.

Better take a real close look before you leap into bed with RISC technology. Those powerful teeth you think RISC can put into your product line just might eat you alive.

RISC could devour your software investment, your company's profits, maybe even your company. RISC will force you to spend an enormous amount of time, energy and money porting new software. All the while, you'll be supporting and maintaining two separate product lines. Not to mention the fact that you'll be losing market share for every extra year it takes you to bring out your RISC product.

What about the inevitable RISC shake-out? Today, more and more RISC processors are appearing on the market. Tomorrow many of them will be history. Which processors will survive the shake-out? And what happens to those computer manufacturers who pick the wrong ones?

The consequences are obvious. A lot of companies who get into bed with RISC now will someday find themselves sleeping out in the cold. Alone.

I'm convinced, RISC is risky business. So what's the alternative? If you have a 680X0-based product line, there is only one viable alternative: Edge Computer.

In fact, three multibillion dollar computer companies are already powering their way into the high-end commercial, multiuser market with Edge technology. Here's why:

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Edge integrates at whatever level is most efficient and profitable for the OEM, from board set on up.

Edge allows OEMs to develop a full product spectrum with a single architecture. In other words, their customers won't be burdened with the added, substantial cost of supporting RISC.

Edge gives OEMs a clear path. We're at the forefront of 68030 technology. We'll be at the forefront of 68040.

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PIC 7000I-4	TMS 7000 NA-4	PIC 7040I-4	TMS 7040 NA-4
PIC 7001-2	TMS 7001 NL-2	PIC 7041-2	TMS 7041 NL-2
PIC 7001I-2	TMS 7001 NA-2	PIC 7041I-2	TMS 7041 NA-2
PIC 7001-4	TMS 7001 NL-4	PIC 7041-4	TMS 7041 NL-4
PIC 7001I-4	TMS 7001 NA-4	PIC 7041I-4	TMS 7041 NA-4
PIC 7020-2	TMS 7020 NL-2		
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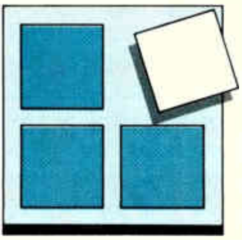
INSIDE TECHNOLOGY

THE EMBEDDED PROCESSOR BREAKS OUT OF ITS NICHE



Not long ago, embedded controllers were used only to run event-control applications, but not the new 16- and 32-bit versions; they are designed to do sophisticated real-time jobs that also include math and digital-signal-processing functions

by Bernard C. Cole

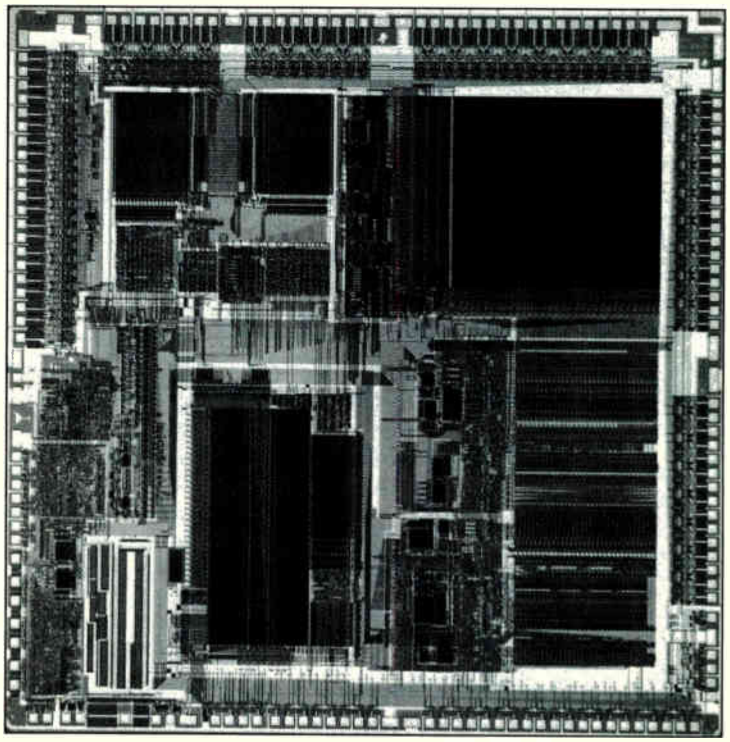
Now emerging from the pack of general-purpose 16- and 32-bit microprocessors is a new class of central processing unit—the embedded processor. These powerful new chips are transcending event control, the traditional embedded-microcontroller niche. They are aimed at such sophisticated functions as graphics and printer control, robotics, image processing, hard-disk control, process control, input/output control, and local-area-network node control.

These embedded processing and control operations require that the processor perform mathematical and digital-signal-processing functions on the information it receives before a specific control operation can be executed. They are not like event-control applications, where the microcontroller directs a mechanical system to perform a preprogrammed set of events in a predetermined order. Instead, the applications that these high-end 16- and 32-bit embedded processors are designed to run require that a complicated set of arithmetic calculations or transformations be performed before the system completes a particular control function. Also, sophisticated embedded processing functions must be performed in real time, necessitating a computing engine that can operate in the millions-of-instructions-per-second range.

Traditional embedded controllers are single-chip 4-, 8-, and 16-bit microcontrollers with on-board random-access and read-only memories that can perform functions requiring no more than a few kilobytes of program and data storage and with cycle times in the milliseconds. These low-end microcontrollers are aimed at event-control applications in games, television tuners, appliances, motor control, vending machines, machinery control, scales, and others which can be performed adequately in a single CPU with a small amount of on-chip RAM and ROM. In contrast, the new high-end embedded processors are aimed at applications requiring megabytes of external RAM and ROM, cycle times of microseconds or nanoseconds, and the ability to perform complex floating-point operations—capabilities that are far beyond those of most single-chip microcontrollers.

Most of these embedded-control processing functions have been performed by general-purpose microprocessors such as Intel's 80186 and 80286 or Motorola's 68000. As many as 2,000 design wins for the 80186 were for such embedded-controller applications, Intel claims. And many advanced laser printers use a 68000 to perform specialized DSP and graphics functions. But now, specialized high-end microcontrollers that can do the job more efficiently and faster are coming into the marketplace. These new chips include high-performance reduced-instruction-set computers, dedicated complex-instruction-set computers, and DSPs. There are also custom and semicustom solutions designed to fill out the mix of general computing and signal-processing functions required in such embedded-control applications.

With these new chips, the traditional distinction be-



1. Advanced Micro Devices' Am29000 is a 32-bit RISC machine with a sustained speed of 17 mips, optimized for embedded applications.

MOTOROLA'S NEW DSP ENGINE COMES WITH FLOATING POINT

The company hangs on to the record for fastest single-chip DSPs—its latest chip runs at 13.3 mips

In the drive to push embedded processors beyond their traditional applications, Motorola Inc. is launching two versions of a powerful new chip. The DSP96001 and DSP96002 promise to smash the speed records set by the Schaumberg, Ill., company's own DSP56000 single-chip digital signal processor two years ago. With that kind of performance, the new device can compete for the same high-end embedded control and processing applications that makers of specialized reduced-instruction-set computers and complex-instruction-set chips are targeting.

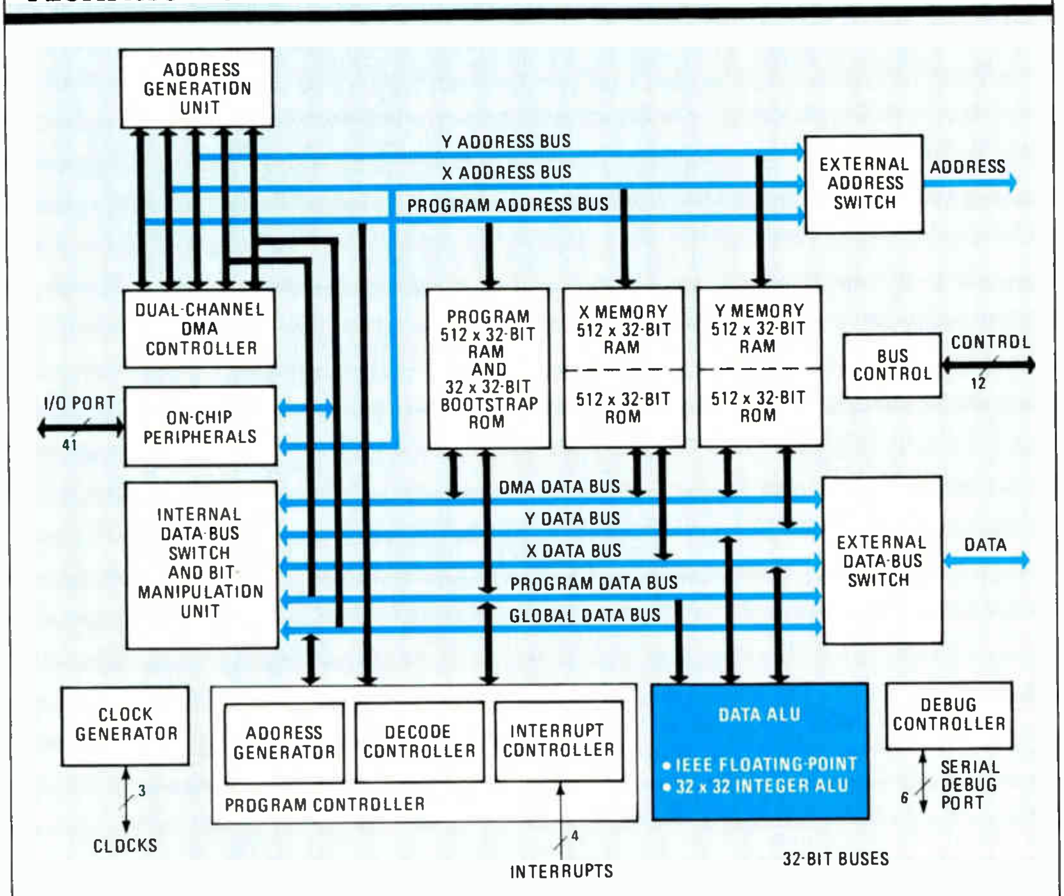
The DSP96001/2 keeps the speed record for single-chip DSPs set by its predecessor, Motorola claims, running at 13.3 million instructions/s compared with 10.25 mips for the DSP56000 [*Electronics*, March 10, 1986, p. 30]. Sample quantities of the DSP96001/2 are due by the fourth quarter.

If initial performance specifications are any indication, the new DSP chip, which Motorola is calling an "attached processor," will give competitors more than a run for their money. At 13.3 mips, the 161-pin device can execute a 1,034-point complex fast Fourier transform in less than two milliseconds, a full 30% to 35% faster than its predecessor. Featuring a peak performance of 40 million floating-point operations/s with an instruction execution cycle time of only 75 ns, the DSP96001 can execute 66.66 million addresses/s external, with an internal peak performance of 256.66 Mbytes/s. On-chip functions include a host central processing unit and serial and synchronous-serial interfaces. On the DSP96002, the on-chip peripherals are removed and a bus controller and a second extended address switch added.

The performance improvement comes from revamping the architecture (see fig. 1)—up to a full 32-bit implementation—expanding the data arithmetic logic unit's register set from a 56- to a 96-bit-wide word configuration. On-chip random-access and read-only memories have also been expanded. An improved host interface and a dual-channel, direct-memory-access controller to support the higher bandwidth have been added. In addition, an on-chip barrel shifter and a 32-by-32 multiplier/adder are now incorporated on-chip. And the basic 56000 instruction set has been enhanced to implement fully the IEEE 754-1985 standard for binary single-precision and extended single-precision floating-point arithmetic.

The DSP96001 outdoes the DSP56000 when performing many DSP benchmarks, says Bryant Wilder, manager of digital signal processing operations in Austin, Texas. For example, he says, a finite impulse response filter with data shift is per-

FLOATING POINT ON AN EMBEDDED PROCESSOR



1. The DSP96001/2 hits a performance rate of 40 megaflops by increasing the number of data buses, adding a dual-channel DMA controller, and incorporating a multiplier and barrel shifter into its data ALU.

formed in 0.075 μs per tap, 25% faster than the DSP56000 and 4 to 10 times faster than competitive single-chip DSP circuits.

The most significant modification to the architecture has been in the register structure of the data ALU portion, says Kevin Kloker, principal staff engineer at the systems research laboratory in Schaumberg. In the earlier unit, the data ALU contained four 24-bit general purpose input registers which could be treated as four independent 24-bit registers or as two 48-bit registers, and six accumulator registers, four of which were 24 bits wide and two that were 8 bits wide.

To implement the IEEE 754-1985 standard for single-precision and extended single-precision binary floating-point arithmetic, the data ALU in the 96001/2 is organized as one file of ten 96-bit general-purpose registers that can also be addressed as thirty 32-bit registers. Also added into the ALU for the same purpose is a 32-bit barrel shifter, 32-bit adder, and 32-bit parallel multiplier. The width of the register file means the data ALU can do any mix of multiplication, addition, subtraction, format conversion, shifting, and logical operations in one instruction cycle. Multiplication with positive or negative accumulation takes no more than two cycles.

To boost overall performance over the DSP56000—by up to 35%—to 13 to 14 mips, Motorola designers completely revamped the internal architecture on the DSP96001/2. All of the buses, internal and external, have been expanded to 32 bits—the DSP56000 had only three internal and one external address buses, which were 16 bits wide, and internal and external data buses, which were 24 bits wide. The total number of internal buses has been upped as well, from four on the DSP56000 to five on the DSP96001/2. In addition to the bidirectional x and y data buses—the program and global data buses—the chip also has an additional bidirectional bus to accommodate the on-chip dual channel DMA controller. To give system designers even more flexibility, the DSP96001/2 bus structure is designed so that under certain conditions and with certain instructions, the two 32-bit x and y data buses can function as a single 64-bit-wide bidirectional bus.

Also, says Wilder, the highly parallel architecture of the DSP56000 has been enhanced in the DSP96001/2. The data ALU, address arithmetic units, and program controller operate in parallel within the CPU so that an instruction prefetch, up to three floating-point operations, two data moves, and two address pointer updates can be executed in a single instruction cycle. These functions may use any of three types of arithmetic—linear, modular, or reverse carry. "I think you will find it hard to dig up any RISC controller, much less any CISC machine, that can do anything comparable," says Kloker.

A dual-channel DMA controller on the chip operates in parallel with the CPU. The DMA controller performs all the address storage and effective address calculations that are necessary to address the DMA source and destination-memory locations on two channels.

To support its use in embedded control applications, the DSP96001/2 also incorporates on-chip RAM and ROM. Both the x- and y-data RAMs contain 32 by 512 bits each, versus 24 by 256 bits on the DSP56000. On-chip program RAM space has also been expanded, from 512 by 24 bits to 512 by 32 bits. In addition, the on-board x and y data bootstrap ROM space has been expanded, from 32 by 24 bits to 32 by 32 bits each.

Just as Motorola offered the 56-bit-word-wide DSP56000 as a single-chip alternative to traditional 8- and 16-bit microcontrollers such as Intel Corp.'s 8051 and 8096 in real-time event-control applications requiring digital signal processing, a similar strategy is being taken with the DSP96001/2 in the high-end embedded processor market. It is aimed at applications such as graphics and image processing and robotics as well as the more traditional DSP applications—array processing, digital audio, instrumentation, medical equipment, and speech processing. Indeed, says Wilder, the DSP96001/2 should be a real contender on two counts. "Unlike most of the other offerings, we have not given up on the single-chip solution [but instead offer] a single device which incorporates not only the CPU and some RAM and ROM, but program control and floating-point processing as well."

A second benefit is architectural flexibility. If, for example, the system designer wants to embed the additional processing functions within the host system itself, the DSP96001 would be used, configured as a host interface slave (see fig. 2a) using its own internal RAM resources or additional RAM and input/output resources via an optional local bus. It could also be used as a bus interface master where it accesses the data and programs in the system RAM (see fig. 2b). Where the system designer wants to embed the additional processing in a peripheral, such as a printer, rather than the host, the DSP96002 would be used with additional RAM and ROM linking to the host CPU via some external bus or network connection. *–Bernard C. Cole*

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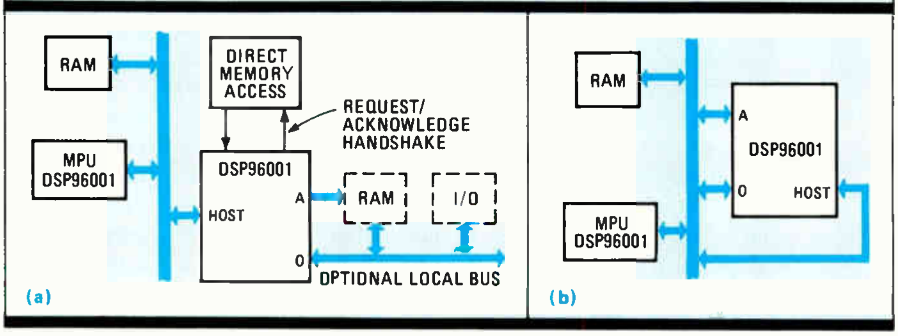
SLAVE AND MASTER



2. The DSP96001 acts as an attached processor in either a host interface slave (a) or a bus interface master (b) configuration, sharing the system memory.

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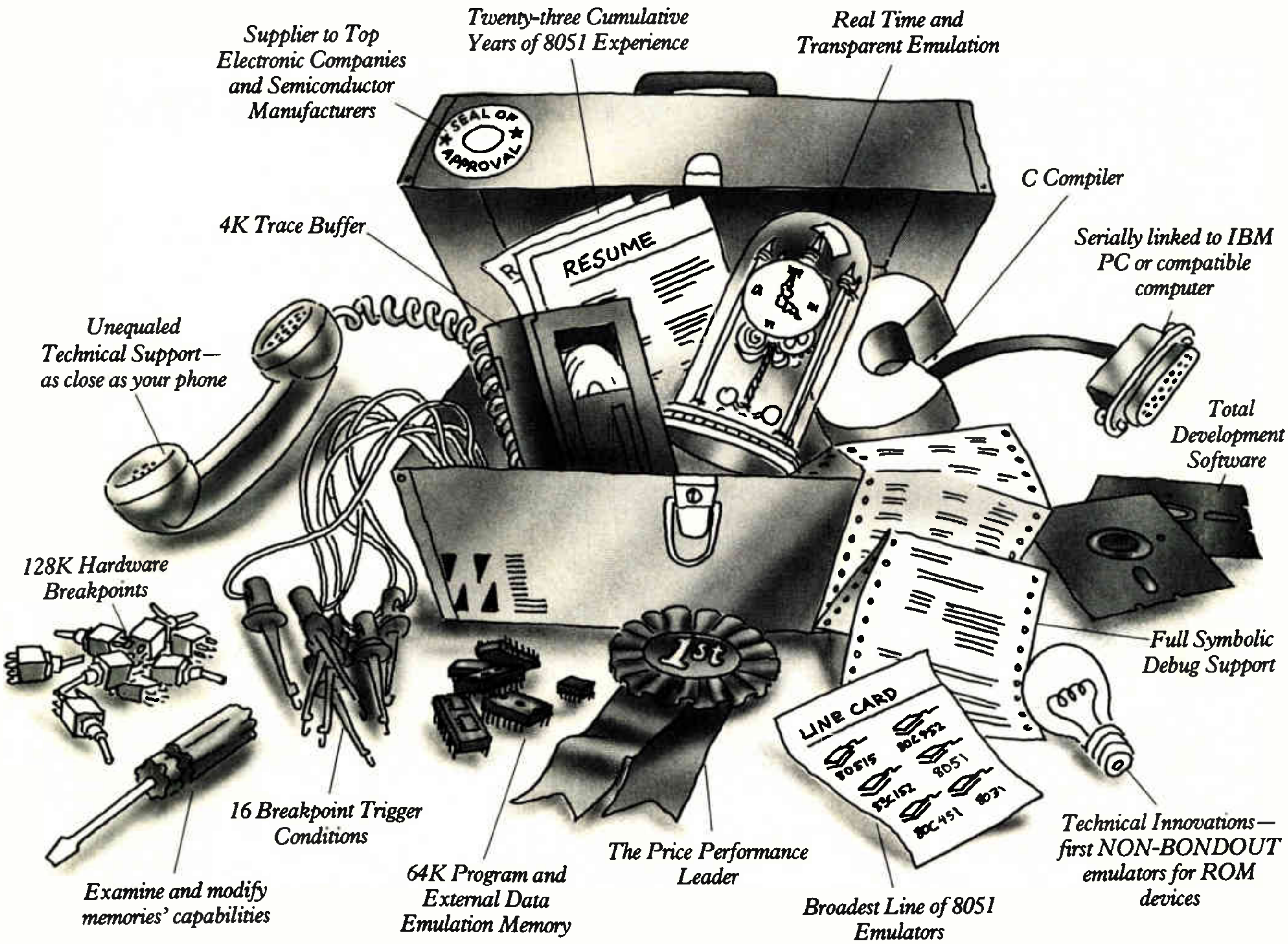

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addressing range, as well as the lower costs associated with manufacturing a standard CPU architecture. To perform the complex graphics-oriented functions needed in many laser-printer applications without sacrificing performance, National has added about 15 graphics-oriented commands, unique to the National chip, to its instruction set. This feature has been combined with the addition of special circuitry to simplify systems design, including an on-chip clock generator, DMA control signals, interfacing circuitry for an external graphics accelerator such as a BitBlt processing unit, and flexible bus timing. The 32CG16 also incorporates additional circuitry to simplify interfacing to a microcontroller and DRAM controller.

Among the most important instructions are those required for BitBlts to move characters around quickly and create patterns, windows, and other block-oriented effects. One very powerful instruction is EXBLT, which executes an entire BitBlt routine rather than implementing specific logic operations—AND, OR, and NOR—as other BitBlt instructions do. EXBLT is useful in applications where overlapping windows demand vertical and/or horizontal movement.

Other instructions relate to line drawing, filling of objects, floating-point computations (needed for scaling and rotation of objects), and data compression/expansion (for networking and facsimile applications). For example, the MOVMP command (move multiple pattern) is a very fast instruction for clearing a DRAM and drawing patterns and lines; SBITS (set bit string) can quickly fill objects, outline characters and draw horizontal lines; and SBITPS (set bit perpendicular string) is used for vertical-line drawing.

The same instructions necessary for magnifying or compressing data can be used to create a larger pattern by simply multiplying the "length" value by the expansion instruction. "As the pattern of data is expanded, it can be magnified by up to 10 times or more," says Wilson. "This creates several sizes of the same style of character or changes the size of a logo." On the other hand, by combining one of these instructions with another specialized command—move string—along with the BitBlt instruction, a line can be lengthened, shortened, or duplicated while maintaining the same aspect ratio.

National designers made a special effort to include instructions in the 32CG16 to deal with specific bottlenecks in the Postscript page-description language used in many personal-computer-based desktop publishing systems.

"Although no standard has yet to emerge, Postscript is one of the better page-description languages for printer text graphics," Wilson says. In fact, it is a more compact and flexible language than the well-known GKS [Graphics Kernel Standard] when used with laser printers." Another major advantage of Postscript in desktop publishing applications, he says, is that it uses character fonts well established in typesetting and GKS does not.

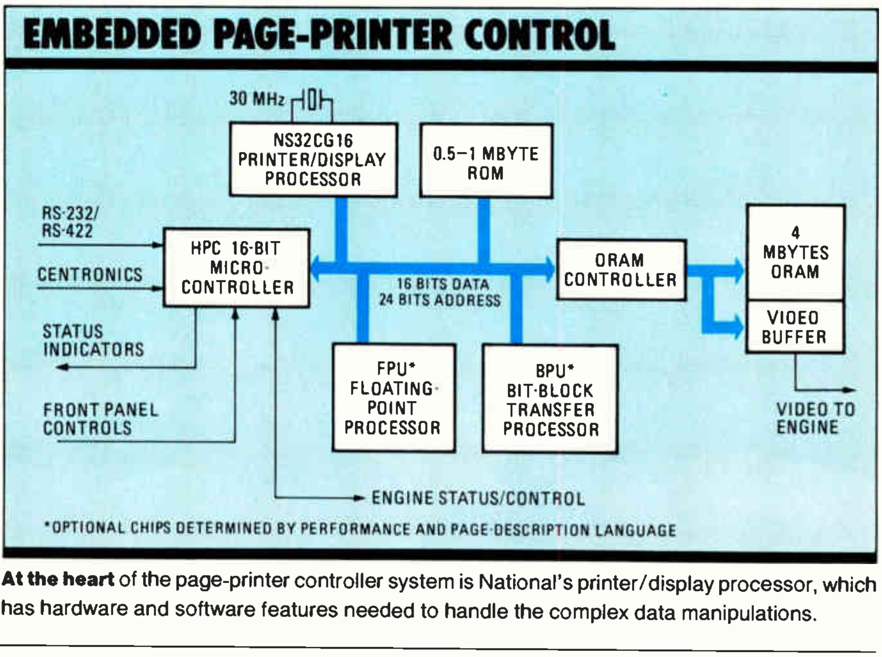
Because fill operations tend to be slow in Postscript, the 32CG16 provides a high-speed fill operation that will push the processor to its maximum bus bandwidth of 60 million pixels/s. To accelerate the process of generating outline fonts, the printer/display processor on the chip will work with floating-point units such as the NS32081 and NS32381, which speed the computations.

Also in the set are binary data compression/expansion instructions for font storage, using RLL (run-length-limited) encoding. Using these instructions, says Wilson, a compressed character set can be stored in 30% to 50% less memory space, allowing the use of fewer read-only memories or allocating the space for additional functions. "Depending on the algorithm used and the type of data being processed, the compression ratio can be 50 : 1 or higher." Aside from their compression and expansion duties, these instructions can be used for graphics operations, such as finding the boundaries of an object, or for line drawing.

Although the company is still in the early stages of defining a variety of special-purpose embedded processors, Wilson believes the approach can be used in such applications as copying, facsimile, and optical-character reading. "All boil down to the use of bit-mapped graphics to store the digital representation of an image in a memory [frame buffer]," he says. "The image may be compressed, expanded, stored on a disk, or manipulated in other ways before being printed." Indeed, says Wilson, with a few changes to the instruction set and interface logic, a chip such as the 32CG16 could be modified to serve in the copying, facsimile, or optical character-reading applications.

Eventually, says Wilson, as processors such as the 32CG16 increase in power and integrate more functions on-chip, systems designers will be able to build a single machine to incorporate at least three functions—copying, printing, and fascimile. *–Bernard C. Cole.*

For more information, circle 481 on the reader service card.



At the heart of the page-printer controller system is National's printer/display processor, which has hardware and software features needed to handle the complex data manipulations.

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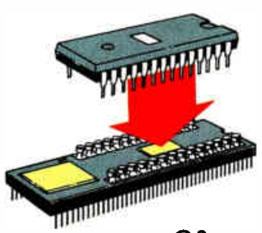

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A BIT-SLICE MICROPROCESSOR FOR EMBEDDED APPLICATIONS

Integrated Device Technology says its chip can do anything RISC chips can—and in more architectures

Despite the emergence of reduced-instruction-set computers and algorithmic-specific processors aimed at particular embedded control applications, Integrated Device Technology Inc. is forging ahead with a highly parallel, high-performance second-generation version of its 32-bit microprogrammed microprocessor.

The Santa Clara, Calif., company cites the adaptability of the microprogrammed bit- and word-slice processor to a wide variety of bus architectures, its flexibility in algorithm modification, and its ease of memory management—not to mention its speed. The IDT49C404A is fabricated in the company's new third-generation 1-μm enhanced CMOS process, CEMOS 3B, says Michael Miller, manager of processor product definition and applications engineering. The 32-bit slice has an instruction-cycle time of 70 to 80 ns and is 20% to 30% faster than its first-generation predecessor, twice that of competitive CMOS devices, and equivalent in speed to some bipolar parts, he says.

To ensure high-performance embedded control and processing applications—graphics, mass-storage control, data-base accelerators, image processing, and robotics—the IDT49C404A boasts a specially optimized architecture to perform shift, rotate, mask, and merge operations in parallel rather than in sequence. It also has a 64-by-32-bit expandable seven-port random-access memory that allows three write and four read operations to be performed in a single clock cycle and three bidirectional 32-bit data ports for virtually unlimited bus accessibility and easy external-memory expansion. Add the proprietary on-board serial protocol channel, which considerably simplifies the writing and debugging of microcode, system testing, and maintenance, and Miller claims the processor can more than hold its own against the many RISC designs aimed at embedded-control applications.

The attraction of advanced RISC designs for performing embedded control functions is that they incorporate features such as deeper pipelines to allow faster cycle times, as well as separate instruction and data caches to allow the processor to fetch and process data and instructions simultaneously. RISC's large register files eliminate the need to go off-chip to access data.

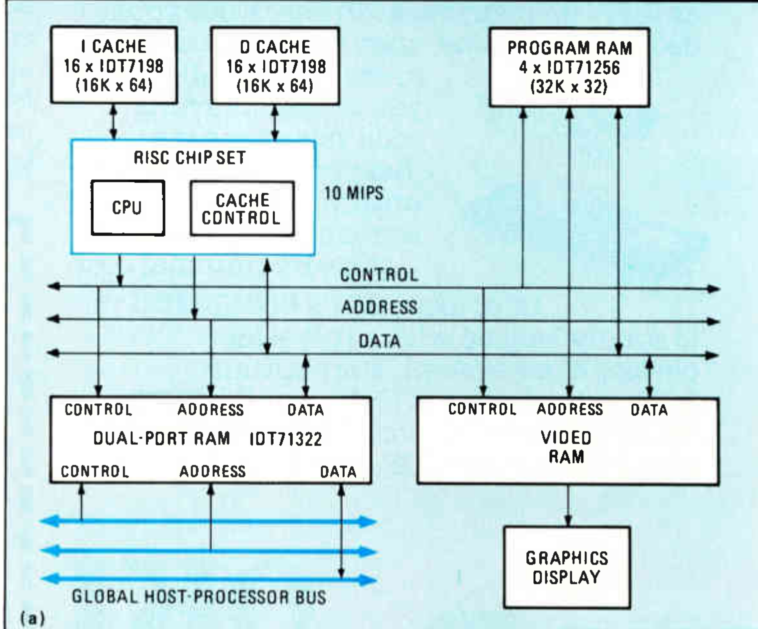
But Miller claims that the microprogrammable building-block approach, based on bit- and word-slice architectures, allows the design of systems with all the features of a RISC design. Indeed, he says, it is in bit-slice-based systems that many of the basic features of today's single-chip RISC chips were first implemented. But where the single-chip RISC approach is limited to a small on-board instruction set, the microprogrammable approach can be used in different classes of bus architectures.

Its ability to modify the control algorithm is important in high-end applications where standards are not defined. Microprogrammable processors, unlike RISC machines, do not use sophisticated memory-management units or cache memory. "Practically, in many embedded-control applications, such features only confuse the issue, especially where precise cycle timing is important, such as in real-time control," he says.

The chip's designers combined flexibility, low component count, and compact design with high performance, says Miller, by using the company's CEMOS 3B process to implement a design that combines a highly parallel architecture, high-throughput three-bus structure, and proprietary multiport register file.

A common bottleneck in present bit-slice designs, says Miller, is the sequence of operations for performing various arithmetic, shift, and merge operations. Often, these functions are implemented to be performed in successive clock cycles, with up to 20 cycles sometimes required to extract a field of data, operate on it, return it to the register file, and shift it

DISPLAY CONTROL: RISC vs. MICROPROGRAMMED



Performance of an embedded graphics controller using a RISC implementation (a) is exceeded by a factor of eight or more with a bit-slice version (b) using IDT's 49C404A.

to an output. In the IDT49C404A, the onboard seven-port register file feeds data in parallel—rather than sequentially—to an onboard funnel shifter, arithmetic logic unit, mask generator, and merge logic block. Thus, for simple sequences, Miller says, the user can select data from the registers, operate on it with the ALU, and merge it in one 70-to-80-ns cycle.

Enhancing the parallelism of the design is a seven-port register file RAM designed for writing three locations while reading four locations—all in one cycle—as well as three bidirectional data buses. Unlike competing designs in which the ports are dedicated to either input or output operations, data can be read out of the register file on either of two buses, or both, or brought in independently on either bus. A third bidirectional bus links the output of the merge-logic block to the input of the register file, allowing ALU operations to be performed in parallel with extraction of data out of the register file.

These features allow the implementation of the tight inner loops of computation-intensive and repetitive code in fewer writable-control-store memory devices, relying on the host processor to provide all of the glue code. The result is a significant decrease in component count—22 parts for the RISC-based system and 16 for the 404A-based implementation—but without any compromises in performance, says Miller. "In many embedded control applications, a 49C404A-based system can achieve throughput rates at least 10 times that of a comparable RISC implementation."

For example, in a typical embedded graphics control application, where icons must be moved in bit form out of a dual-port memory-based host system interface and into video memory at arbitrary bit offsets, a 32-bit design built around the 49C404A requires fewer parts and is ten times faster, Miller says. Using a typical RISC machine made by MIPS Computer Systems Inc., but second-sourced by IDT, with instruction and data caches and program RAM for storing algorithms, a typical instruction execution loop might be performed in 10 instructions. At a sustained rate of 10 million instructions per second, this would yield 1 million loop iterations per second (see fig. 1a) A more realistic approximation, he says, requires more instructions with the rate being one-half to one-third of the ideal, thus yielding a rate of 500,000 iterations per second.

The same application, built around the 49C404A (see fig. 1b) would take advantage of its parallel architecture: operands are computed, fetched, merged, and stored in parallel, requiring two microprogram clock cycles of 60 ns each. This translates into a loop iteration rate of 8 million loops per second, Miller says. "Depending on whether you use the ideal or the realistic rates for the implementation, the performance improvement in the 49C404A system is anywhere from eight to 16 times."

As a bonus for designers of embedded control systems, says Miller, the company's engineers have incorporated a proprietary serial protocol channel to simplify the tasks of writing and debugging microcode, field maintenance, debugging, and testing as well as system testing during manufacturing. Adding only four additional pins and requiring only 5% more logic, the serial protocol channels allow designers to examine and alter the internal state of a system without having to remove the device. Because the processor is buried inside the system—and of because double-sided surface-mount packaging—in embedded applications, this is a major improvement, he says.

Among the primary blocks needed to implement the serial protocol channel onchip are a command decode logic block, serial command and address/data registers, and I/O pad scan circuitry. The command-decode logic block controls the data paths and generates the signals to exercise the hardware. The serial-command register decodes the 16 special diagnostic instructions and coordinates the transfer of data between the RAM and serial-data register, which is connected to the internal bus to gain access to the RAM register file and on-chip data breakpoint circuitry. Address/data registers hold the RAM address/data and the data obtained after the diagnostic commands are executed and the I/O scan circuitry scans specially located flip-flops to monitor the state of the device's pins, as well as simulating external conditions. *–Bernard C. Cole*

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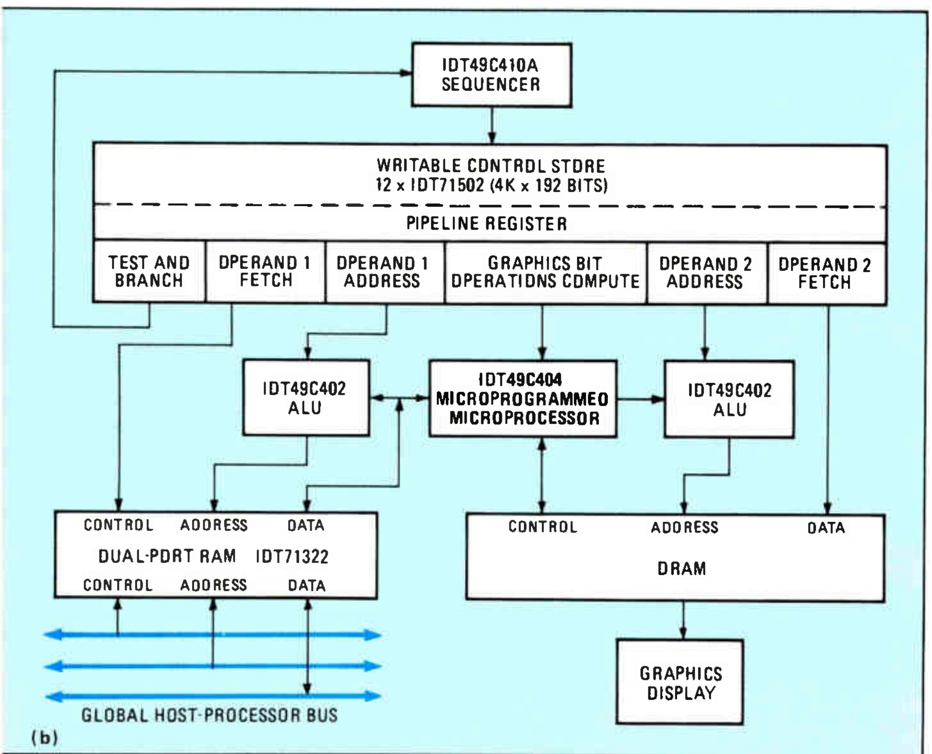

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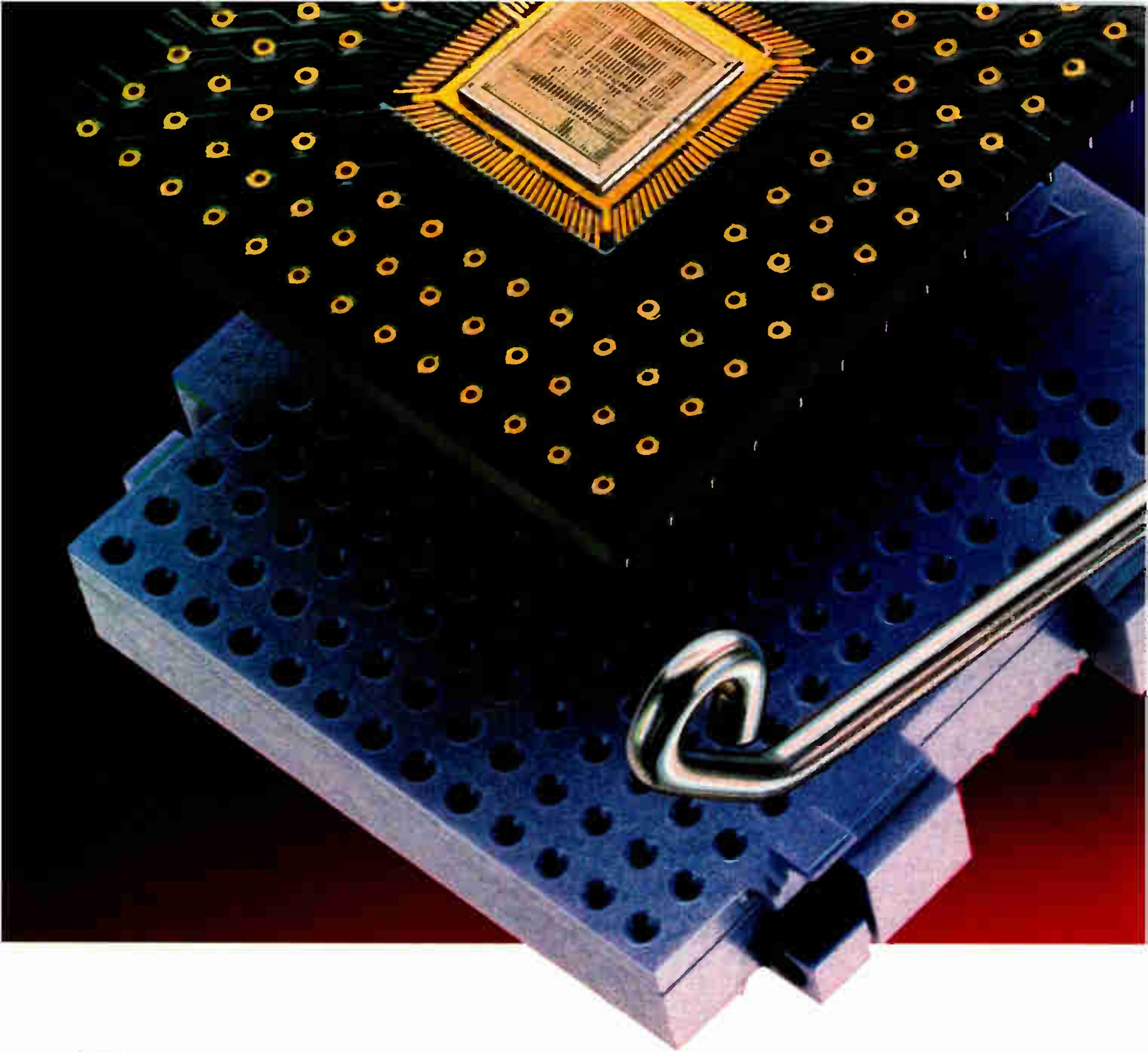

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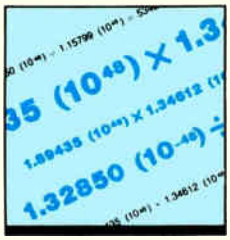


FLOATING-POINT MILESTONE: SINGLE-CHIP PROCESSORS

With floating-point applications exploding, at least three U. S. chip makers have just completed the difficult task of designing and building a single-chip processor that will meet the IEEE standard for 64-bit binary floating-point arithmetic

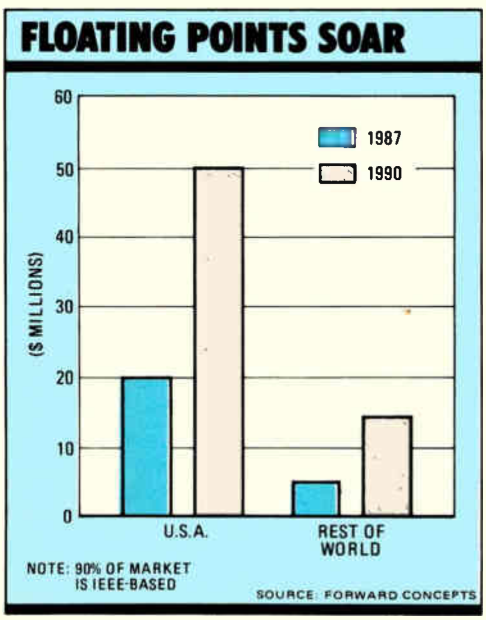
by J. Robert Lineback

Single-chip technology has caught up with standards for the 64-bit floating-point arithmetic set by the Institute of Electrical and Electronics Engineers, and the timing could not be better. Floating-point markets are about to be propelled beyond the traditional technical markets by the explosion in reduced-instruction-set computer architectures and powerful work stations and the accompanying growth of numerically intensive applications.

Floating-point units are suddenly finding work where once only data-processing software had been employed. Bankers, economists, and stock brokers are buying technical work stations to automate business forecasting and model global financial markets.

"Floating-point has turned out to be a lot broader market than people thought it would ever be," says industry analyst Will Strauss of Forward Concepts in Tempe, Ariz. He estimates market growth at a healthy 36% annual rate. The merchant market for floating-point processor chips and chip sets stood at $25 million worldwide in 1987, Strauss says, and will grow to $64 million in three years (see chart). About 90% of the floating-point market is expected to comply with the IEEE standards set in 1985.

What's more, the floating-point niche is an area where U. S. chip makers appear to have a decisive edge over arch rivals in Japan. This advantage exists because of the software-intensive nature of the business and its current small size.



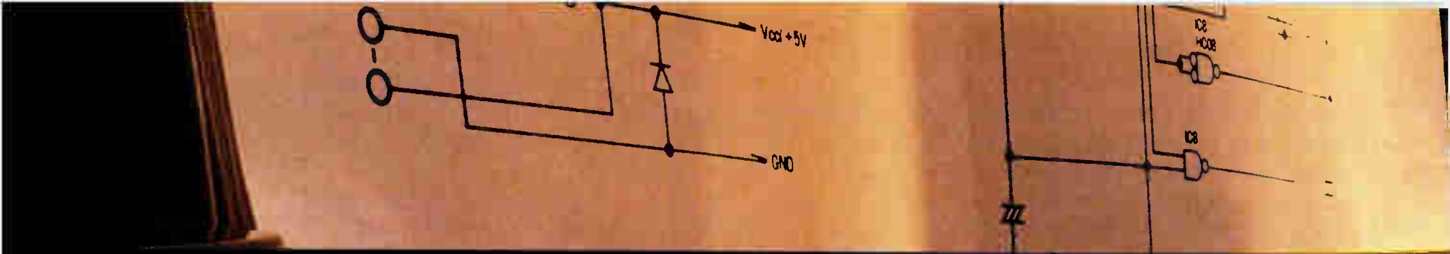
Until now, the IEEE's standard for binary floating-point arithmetic was supported only by multiple chip sets that work together to support most, but not all, of the spec's operating modes or required accuracy. New 1-μm CMOS technology has given chip makers enough integration power to pack double- and single-precision math units onto one chip.

With that breakthrough in hand, the battle is turning to the development of innovative architectures for parallel operations, new embedded algorithms for higher accuracy in rounding off results, and hooks to make the IEEE-standard parts easier to use in a growing number of systems.

At least three U. S. competitors are aggressively launching single-chip floating-point units. Advanced Micro Devices Inc., Texas Instruments Inc., and Weitek Corp. are aiming at driving down costs and raising performance of systems conforming to the IEEE standard. AMD, of Sunnyvale, Calif., plans to take that goal two steps further (see p. 78), by also conforming to other formats created by IBM Corp. and Digital Equipment Corp. The AMD chip also is a top performer in both scalar and vector operations.

TI in Dallas is launching a new powerful 209-pin CMOS processor (see p. 80), which has features that will support several RISC architectures, including one backed by Sun Microsystems Inc. And traditional floating-point powerhouse Weitek in Sunnyvale, Calif., is introducing its highly parallel chip, which integrates three separate 64-bit processors on a single die (see p. 84).

All three of the chips do more than implement the tough IEEE-754 floating-point specifications, because just meeting the IEEE specs alone will not be enough for chip integrators, says John F. Rizzo, marketing manager at Weitek, which pioneered the floating-point processor market in the early 1980s. "Three years ago when you would go in to sell a chip, floating-point customers were only concerned about speed. Now, they worry about software compatibility, standards, and interfacing to specific processors as well as matching performance and price to an application," Rizzo says. □



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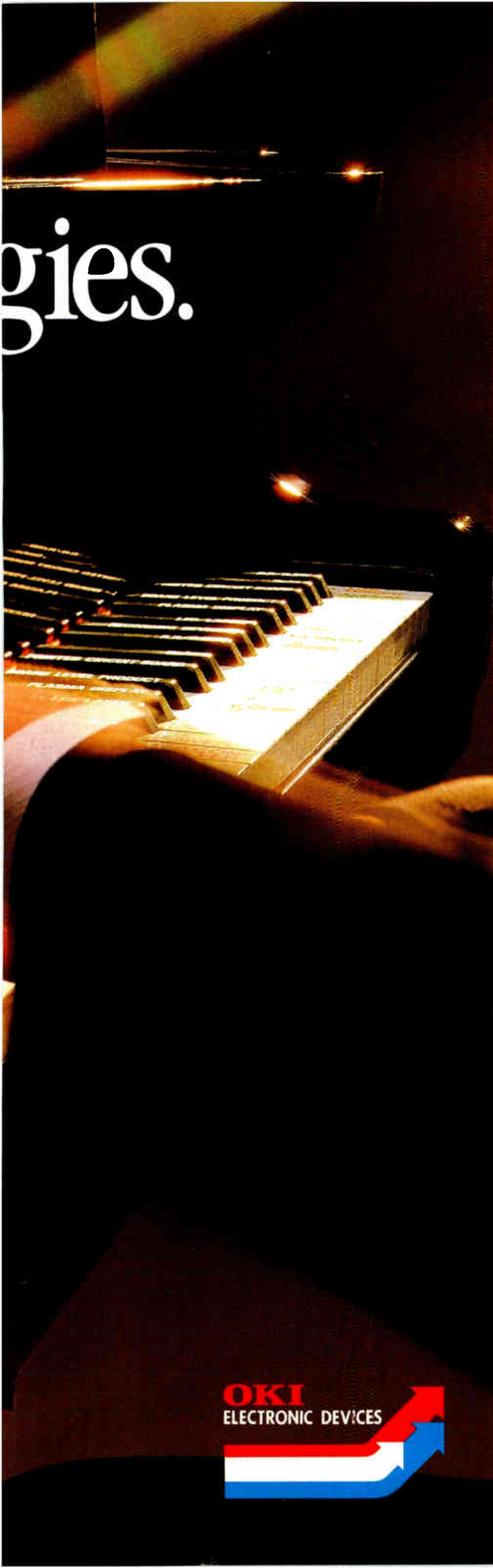

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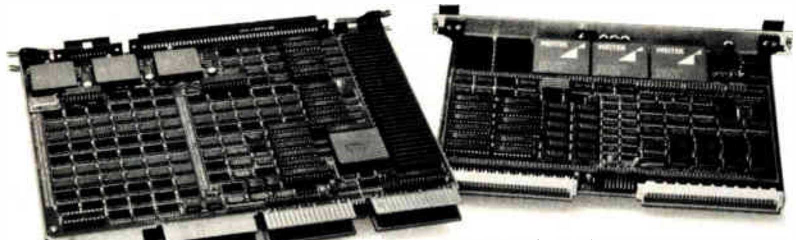

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GRAPHICS VISUALIZATION IS A REAL EYE OPENER

High-end graphics work stations, image computers, and desktop graphics supercomputers meld high-performance computing with realistic 3-d image rendering; network sharing of new visualization techniques is just under way

by Tom Manuel

New ways of seeing are opening up to engineers, scientists, and designers who can now create realistic-appearing models, manipulate them, and visualize the results in real time. Creating images to represent the intensive computations and data inherent in many computer applications areas is a dream coming true. So, too, is working interactively with computer graphics images that look as real as photographs or involve fast surface rendering of full-color three-dimensional objects. The machines of the new visualization age are high-performance graphics work stations, image computers, and a brand new class of computers, called graphics supercomputers.

The capabilities of these machines are improving rapidly, even as their prices hold steady or drop. Graphics work stations typically have computational processors ranging from 2.5 million to 15 million instructions/s, floating-point units, and a graphics subsystem. High-end graphics work stations sport powerful 3-d graphics engines with built-in algorithms for fast surface rendering of images of 3-d solid objects.

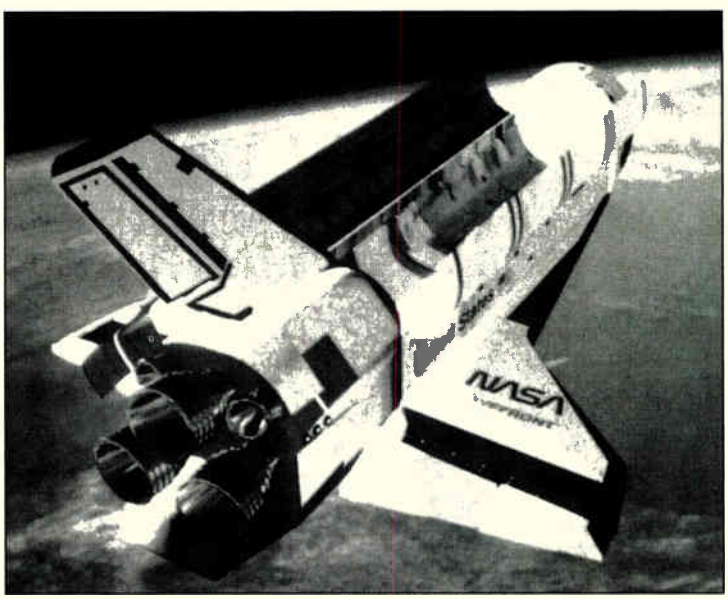
Image computers are more powerful and handle more data than graphics work stations. "An image computer is two orders of magnitude more powerful than a graphics work station in computational speed and in memory size," says Alvy Ray Smith, executive vice president of Pixar in San Rafael, Calif. For applications in which the data fills up 3-d space, such as many scientific simulations, seismic and weather data, and medical scanning, image computers with graphics work-station front ends are the preferred tools.

Graphics supercomputers combine graphics performance beyond the top end of today's graphics work stations with processors that provide minisupercomputer power. They are well suited for applications where lots of calculations must be done and the results must be immediately rendered on the screen for interaction by the user, such as in mechanical design.

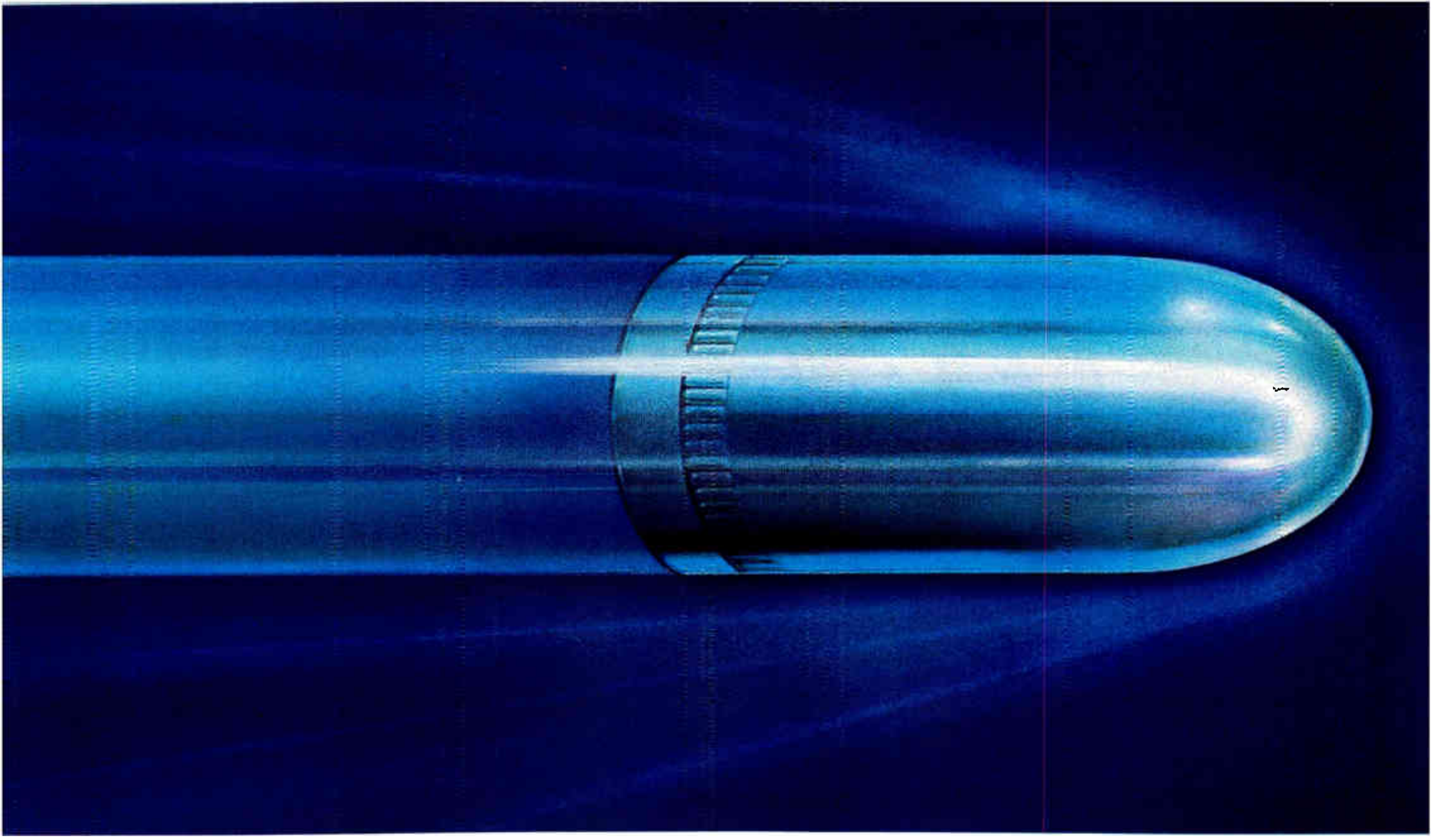
There is a big product push now to provide advanced scientific visualization techniques to scientists to help them understand computer-assisted scientific research. And, in engineering, more realistic rendering of images is emerging as a necessary competitive tool for interactive analysis and design (see fig. 1). Encompassing these applications and many other computer graphics applications is the role beginning to be played by graphics in computer networks. Standards such as the Computer Graphics Metafile are paving the way for users of different systems to exchange images over networks.

Scientific visualization, high-performance engineering graphics, and the integration of graphics into network systems will all be highlighted in the program and exhibits of the forthcoming National Computer Graphics Association conference to be held in Anaheim, Calif., March 20-24. This year's NCGA show features a special demonstration of graphics systems integration involving systems from more than 30 vendors in one network.

A leap-frogging race for top performer in high-end graphics work stations is evident at the NCGA show. The latest vendor to jump over competitors is Hewlett-Packard Co. (see p. 95). The Palo Alto, Calif., company will introduce its HP 9000 model 835 TurboSRX, a new 14-mips work station that the company claims will render photorealistic images up to 10 times faster than its previous top-end graphics work stations,



1. Software from Wavefront Technologies Inc. created this realistic image of the space shuttle, an example of high-quality surface rendering.



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RAPID
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HP DELIVERS PHOTO REALISM ON AN INTERACTIVE SYSTEM

Realistic 3-d images can be viewed from any angle without recomputing the TurboSRX's algorithms

Leapfrogging the competition in graphics and computational performance is the aim of every graphics-work-station company, and the latest to jump ahead in the race is Hewlett-Packard Co. It made the leap by implementing its precision architecture processor on a fast new chip and introducing new graphics architecture and hardware. The Palo Alto, Calif., company has produced a work station performing 14 million instructions/s, with three-dimensional graphics that look as real as photographs. The system, which offers interactive capabilities as well, draws images up to 10 times faster than previous top-of-the-line HP work stations.

HP's technical computer group in Ft. Collins, Colo., is introducing the model 835 TurboSRX as the new high end of its HP 9000 work-station line. The 835 refers to the new 14-mips precision-architecture processor; the new high-performance graphics component is called TurboSRX. A second model, the HP 9000 350 TurboSRX, mates the new graphics subsystem with HP's MC68020-based work station. Prices start at $91,500 and $70,000, respectively—comparable to other high-end graphics work stations.

The TurboSRX systems are the first to offer a new hardware-assisted rendering technique called radiosity, which models the way light reflects between all surfaces of a displayed image. The result is a rendered object, with the photorealism of ray tracing, which can be viewed from any angle. Ray tracing, which the TurboSRX offers as a software utility, requires a complete rerendering of the object for each new view—radiosity does not.

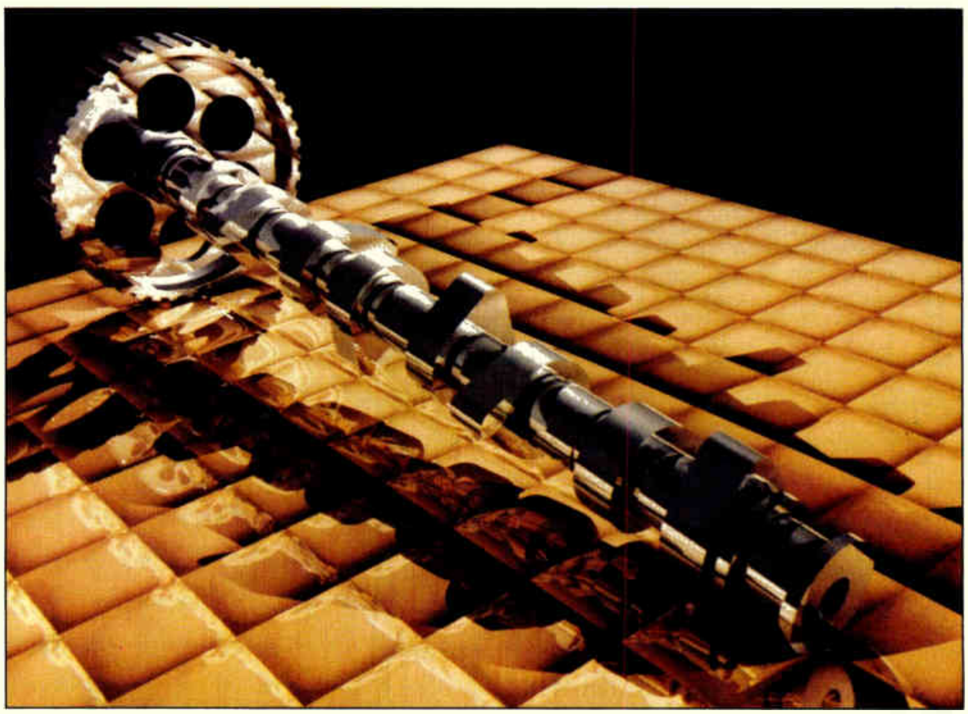
These work stations are also the first to offer sixth-order nonuniform rational B-splines. Affectionately called Nurbs in the graphics world, these B-splines deliver faster graphics interactivity on the HP work stations than any competitive system can provide, the HP designers say.

A B-spline is the mathematical equivalent of a set of draftsman's French curves, which allow a designer to create complex curves—the wing of an airplane, for example—by fitting simpler curves together. The sixth-order Nurbs that HP is offering on the TurboSRX systems produce greater continuity in joining simpler curves together and therefore more realistic-looking surfaces than the fourth-order Nurbs offered on previous HP graphics work stations.

The model 350 TurboSRX and model 835 TurboSRX are especially good for such scientific and design applications as molecular modeling, solids modelling, animation, and imaging. The model 835 system, which is scheduled to ship in October, will compete directly with high-end graphics work stations and desk-top supercomputers offered by Apollo, Ardent, Raster Technologies, Silicon Graphics, and Stellar (see p. 97). In the midrange of performance, the model 350 TurboSRX, with the same graphics performance but lower computational performance than the 835, will compete with products from Apollo, Silicon Graphics, Sun Microsystems, and Tektronix. The 350 TurboSRX will ship in late June.

One distinction of the TurboSRX systems from competitive offerings is their ability to implement and accelerate radiosity algorithms in hardware. Radiosity is a new alternative to ray tracing. Although it requires a lot of computing power, ray tracing has been used since the late 1970s to provide photorealistic images of solid-object models. Equally realistic images produced by the radiosity technique can be manipulated interactively, something impossible with ray-tracing.

The radiosity algorithms were developed by students at Cornell University under the guidance of Donald Greenberg, director of the computer graphics program and made available to HP as part of a cooperative



1. This image of a camshaft from an HP 835 TurboSRX shows off the system's photograph-like realism and provides an example of its ability to render curved surfaces with complex lighting and shading.

technology exchange agreement. The algorithms are based on fundamental energy equilibrium methods used in thermal engineering. Light leaving a surface—the radiosity of the surface—consists of light emitted, reflected, or transmitted through the surface. The radiosity method models the interaction of light travelling between these reflecting surfaces. The radiosity algorithms are accelerated with proprietary hardware in the TurboSRX graphics subsystem. To calculate the light relationships between all polygonal surfaces, the graphics accelerator "creates a set of simultaneous equations describing all possible combinations of light between all the polygons in a given scene," says Harry Baeverstad, R&D section manager at HP.

Ray tracing and radiosity, though producing excellent rendered images, are both very computational-intensive operations, especially if the scene contains large numbers of reflective surfaces. An automobile surrounded on three sides by mirrors, for example, could take over a week to render on a graphics work station. However, the great advantage of an image rendered with the radiosity technique is that once the radiosity of a scene is computed, the viewer can rotate, zoom, or view the object from any angle, in other words, interact with it in real time. That is impossible with ray tracing because each movement of the object requires a complete recalculation of the ray trace.

By comparison, in the radiosity technique, light reflections will not change based on the viewing angle. "While you can view a scene from different angles in a radiosity environment, you cannot change the geometric relationship of objects in the scene because that changes how the light interacts between the objects," Baeverstad says.

"The main advantages of our implementation [which includes hardware-assisted radiosity and software-implemeted ray-tracing] is that it is totally compatible with Starbase, our graphics library interface," he explains. "Any display list used to render an object on the TurboSRX can also use either the ray tracer or the radiosity functions without having to change its data base at all."

Instead of having to perform ray tracing in software or write a special applications program to provide radiosity, an applications software package such as Geomod from Structural Dynamics Research Corp., a General Electric Co. subsidiary in Cincinnati, Ohio, a user only needs to make a call to the Starbase library for either of the two rendering functions, ray tracing or radiosity. The system automatically does the rest.

Just as radiosity permits the user to interact with a fully rendered image in real time, HP's B-spline capability allows the user to interact in real time while creating an image. A B-spline is the mathematical equivalent of a draftsman's French curve. To create a complex curve such as the profile of an airplane wing using French curves, a draftsman selects different curves from a template and traces the curves together to form the desired shape. To create the complex curve mathematically in a computer graphics system, applications software uses different polynomials, each of which defines a unique curve, or B-spline.

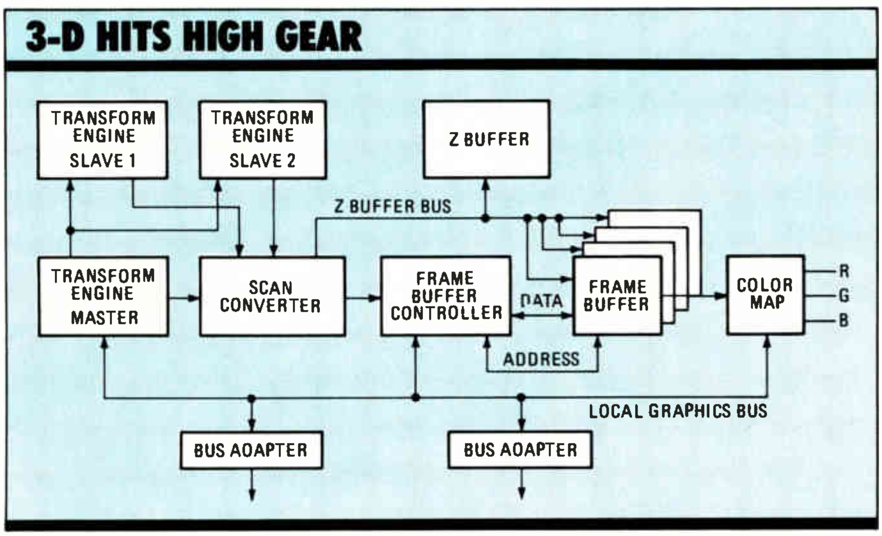
The software places these B-splines together to form a final curve and displays the result on a CRT screen just as the draftsman selects French curves from his template and places them together. This process is termed a piecewise approximation of a curve. To create a surface—such as that of an airplane wing—the B-spline is replicated along the z axis. The higher the order of the polynomial used in each B-spline, the higher is the degree of continuity between the joints of different B-splines.

A nonuniform rational B-spline enables an application program to specify the joints, where one curve meets another, to be nonlinearly spaced. The capability allows the application program to break a B-spline into even smaller pieces. For example, in the design of an automobile trunk, one B-spline defines the curve sloping downward toward the bumper. To add a wind spoiler to the trunk, a nonuniform B-spline jutting upward where the trunk would normally curve downward to the bumper is inserted in the bumper's B-spline curve.

Finally, a rational B-spline surface is one expressed as a ratio of two polynomials. "Without this capability, the system cannot produce true conic sections—cylinders, spheres, cones, etc.," says Baeverstad. Using the HP system, a designer could not create a model of an automobile cam shaft, for example, without using a rational B-spline (see fig. 1).

HP's original SRX was the first system with B-spline functionality in its graphics engine. It represents surfaces as polynomial equations rather than as a collection of polygons which approximate the surface. Before the SRX, an applications program, such as a solids-modeling package like Geomod from SRDC, had to translate the B-spline representation in its data base into a representation which can be displayed with polygons on the CRT screen.

Not only did this require much computing power and a large memory to contain the polygon representation, but it also meant that the user could not



2. HP's new TurboSRX graphics processor contains the graphics transform engine, scan converter, Z buffer, frame buffer controller, frame buffer, and color map for fast solids modeling.

interact with the system in real time. Now applications programs using B-spline representation can command the TurboSRX to draw B-splines.

For example, a program to create a sphere with a polygon every 30 seconds of arc requires 9.3 Mbytes of memory and 35.5 seconds of computing time on a work station without B-splines. By contrast, the TurboSRX with B-splines takes 792 bytes of memory and 4.62 seconds of computing time.

A graphics processor containing the graphics transform engine, scan converter, frame buffer, Z buffer, frame-buffer controller, and color map is the main element of a Turbo SRX (see fig. 2). The processor is a separate assembly that fits into the desk-high cabinet of a HP9000 model 350 or model 835 work station.

During operation, the central processor of the associated HP9000 work station sends segments of a graphics image display list—a polygon, a line, or other primitive—through the bus adapter, over the local graphics bus, into the master transform engine of the graphics processor. If the master is busy with a previous segment, it passes the incoming segment to one of the two slave transform engines, both of which operate in parallel with the master.

After the CPU processes the image using world coordinates, the transform engines convert the image to the 1,280-by-1,024-pixel display-coordinate system. These engines also perform all the computation for B-spline, light source, and color. Each of the three transform engines is a new HP-designed 177,000-transistor custom chip called Treis (transform engine in silicon). The Treis chips are implemented in HP's own n-MOS III process.

As a graphic element comes into the transform engine, it is processed and sent to the scan converter, which performs six-axis interpolation of the graphic primitive or polygon. Where the transform engine specifies a graphic primitive in screen coordinate space, the scan converter specifies the pixel needed to represent the primitive on screen in x, y, and z coordinates—three of the six axes of interpolation. The other three are red, green, and blue colors, which the scan converter also interpolates; for example, the different colors on intermediate pixels resulting from a red pixel on one edge of a polygon and a blue pixel on another.

The frame buffer controller routes the pixels out of the scan converter into the correct frame buffer bank. At the same time, the scan converter routes z-axis data to the Z buffer. As the frame buffer controller draws pixel data into the frame buffer, it uses the Z-buffer data to determine the relative position of one surface with another to remove automatically one surface hidden by another. The frame buffer also controls data transfer's timing from the color map to the CRT display. The system comes with a new color-map chip developed by HP and implemented in its own 108-MHz, 1-μm CMOS gate array. Four of these color-map chips are used in the system. Each chip accepts 8 bits in and provides a 24-bit digital-to-analog conversion, which emits an analog red, green, or blue signal. *–Jonah McLeod*

For more information, circle 486 on the reader service card.

TECHNOLOGY TO WATCH — **COMPUTER GRAPHICS**

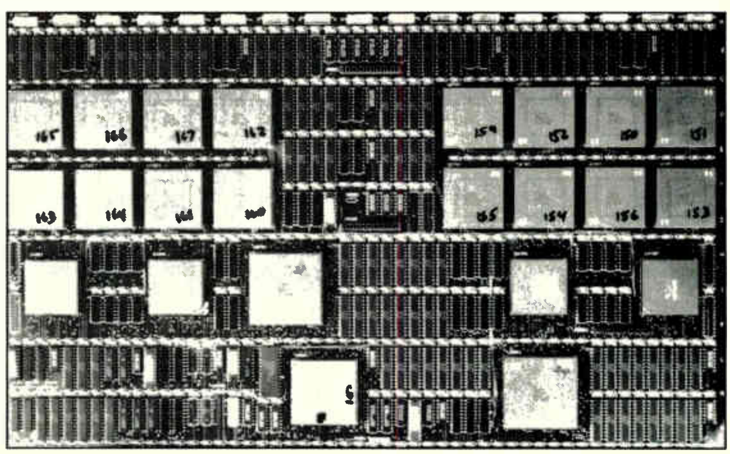
STELLAR'S GRAPHICS MACHINE STRESSES INTERACTIVITY

The single-user supercomputer generates real-time dynamic graphics at 500,000 3-d vectors/s

One of the worst-kept secrets in recent years, the GS1000 graphics supercomputer from Stellar Computer, Inc., made its official debut this week. The long-rumored system [*Electronics*, Feb. 18, 1988, p. 22] combines on a desktop the power of a minisupercomputer with high-performance real-time 3-d graphics—and all for a price of about $100,000.

The system executes more than 20 million instructions/s and can perform as many as 40 million double-precision floating-point operations/s. In the graphics realm, the important numbers are its ability to draw 500,000 3-d vectors/s and display 150,000 Gouraud-shaded triangles/s. That parlay gives the GS1000 computational performance equal to or better than that of early minisupercomputers combined with graphics performance that tops today's best work stations.

The GS1000's multiple-processor architecture hinges on a superwide 512-bit data path. More than half of 61 high-density CMOS application-specific integrated circuits implemented in the system are found in the extrawide data paths. Another key feature is the multistream processor (see fig. 1), which has four full internal streams or instruction paths and consists of a three-chip set. On top of its graphics performance, the system executes more than 20 million instructions/s



1. This multistream processor board from the Stellar GS1000 graphics supercomputer uses many of the big ASICs developed for this system.

and performs up to 40 million double-precision floating-point operations/s—computational performance that is equal to or better than that of early minisupercomputers.

In founding Stellar, chairman and chief executive officer John William Poduska is aiming to bring interactive visualization—dynamic photorealistic images that can be manipulated interactively—to single users in a desktop system (see panel, p. 99). The GS1000 is targeted at applications in mechanical design and engineering, molecular modeling, computational fluid dynamics, and computer animation.

Poduska says the ASICs, architecture, and vectorizing compiler combine to give the GS1000 its heady performance numbers. The GS1000's high-density ASIC devices, which add up to 2 million gates, were developed and fabricated for Stellar by LSI Logic Corp., Milpitas, Calif. "That is at least as many gates as there are in a top-of-the-line IBM mainframe," Poduska adds. The ASIC density ranges from about 15,000 to 55,000 gates, but Poduska declines to elaborate on the internal chip architectures until patents are granted. Each chip is housed in a 300-pin ceramic package.

The system delivers 18 to 20 megaflops in a 300-by-300 double-precision floating-point Linpack array benchmark. That compares favorably with two first-generation midrange supercomputers from Alliant Computer Systems Corp. and Convex Computer Corp. Alliant's FX/8, with four processors, performs 12 megaflops and the single-processor Convex C-120 does 15 megaflops. The Stellar system's 100-by-100 all-Fortran Linpack benchmark is 8.6 megaflops, compared with 6 megaflops for both the just-introduced Apollo Computer Co. series 10000 and the Ardent Computer Corp.'s Titan [*Electronics*, March 3, 1988, p. 65 and p. 69]

Stellar's innovative design approach is embodied in the GS1000 hardware; especially in the 512-bit-wide data path, the overall architecture, and the multistream multiprocessor. Most high-performance computers have data-path widths no greater than 64 bits. The 512-bit width is like a superhighway between the elements in the GS1000, says Craig Mathias, director of marketing. He says the data path functions as an interconnect to perform switching, multiplexing, and demultiplexing.

The data-path chips also manage the transfer of data between system segments with disparate-width data paths. The pathways to main and cache memories are 512 bits, while the link between the data path and instruction processor in the multistream processor, for example, is 96 bits. In all, 32 of the CMOS ASICs—all of the same design—are devoted to the data path.

The GS1000 architecture employs five kinds of processors (see fig. 2). The four primary ones are a multistream processor (main integer processor); a vector/floating-point processor; a rendering processor for graphics; and as many as four input/output processors. The fifth processor is the SPC/386, a 386-based PC AT-compatible processor. The AT processor and bus allow the system to run a variety of administrative and support software and popular plug-in personal computer boards. The system's 512-bit-wide data path interconnects all of the processors, plus the main memory of 16 to 128 Mbytes, and a large cache memory of 1 Mbyte.

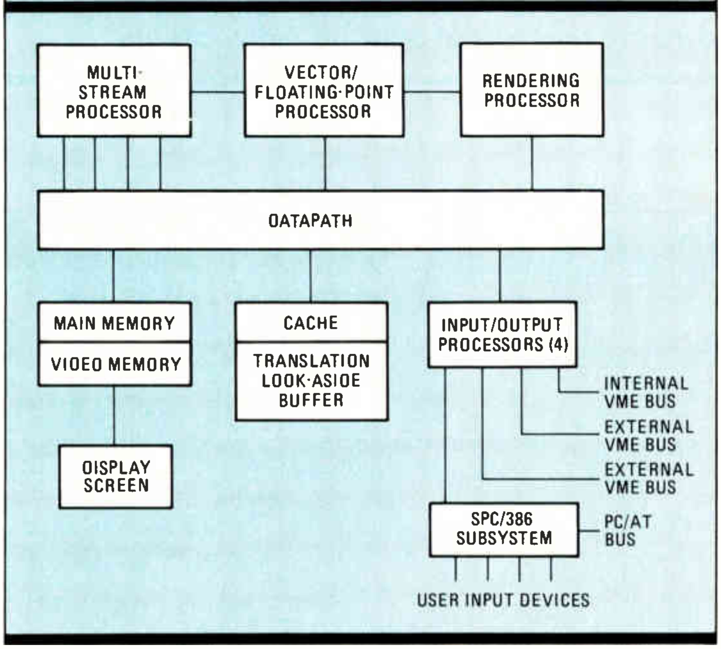
Each of the multistream processor's four full internal streams or instruction paths has 32 dynamically assignable concurrency registers. The four streams share a pipeline, and can work simultaneously on one program or be assigned by the compiler to independent tasks. The compiler dynamically decides which code to run and in how many streams, says Mathias, so that the architecture adapts dynamically to the system load.

The multistream processor's three-chip set consists of an instruction-parsing chip, an effective address chip, and an execute chip. The instruction parser in the front end of the MSP determines what disposition to make of a given instruction; the effective address chip parcels instructions off to the vector/floating-point processor or to the execute chip. Integer and general-purpose instruction execution is the realm of the execute chip. However, it also assists the effective address chip—under direction of the compiler—in grouping those instructions that can be executed in one cycle.

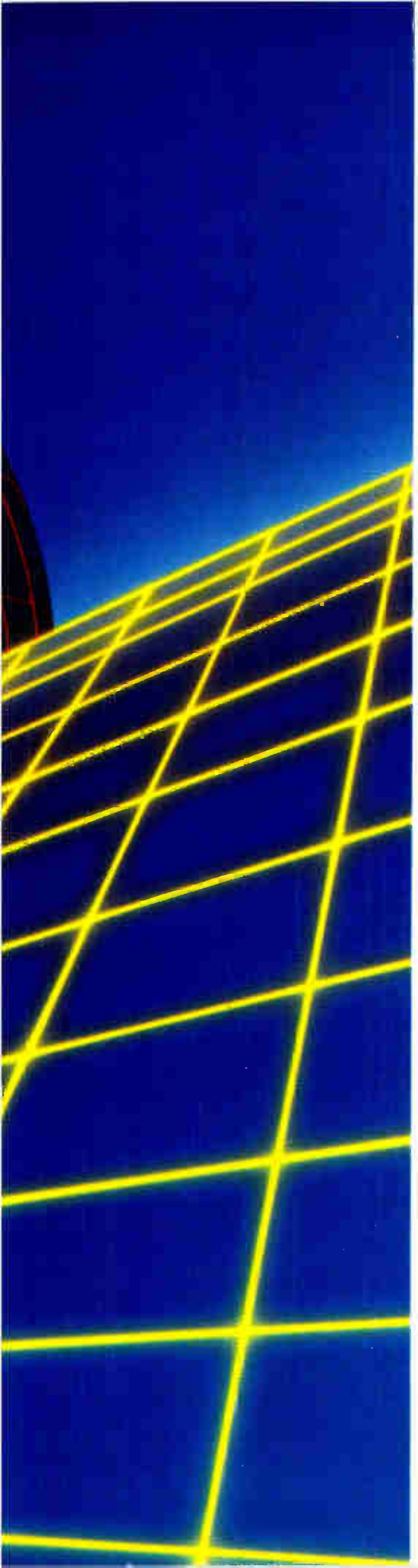
Only one of the vector/floating-point processor's three chips is a Stellar-designed CMOS ASIC: a vector control chip that routes appropriate instructions to the floating-point chips in that processor and sends graphic instructions to the rendering processor for execution. The floating-point devices are the Weitek 2264 and 2265—high-performance CMOS units that give the GS1000 much of its 40-megaflop floating-point speed.

Poduska is especially enthusiastic about the Stellar machine's interactive graphics. The high-bandwidth concurrent architecture embodied in the four-steam multistream processor and the innovation of the footprint processor/rendering engine contribute greatly to real-time dynamic 3-d graphics. The GS1000's ability to generate 500,000 3-d vectors/s is far ahead of general-

THE PATH TO GRAPHICS



2. A 512-bit data path links multiple processors, including a multistream scalar processor, a vector stream processor, and a graphics engine.



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Circle 101 on reader service card

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30-2	7	LP	Elliptical	0.1Hz — 9.9kHz
30-3	7	LP	Elliptical	0.01Hz — 990Hz
31-1	7	HP	Elliptical	1Hz — 99kHz
31-2	7	HP	Elliptical	0.1Hz — 9.9kHz
31-3	7	HP	Elliptical	0.01Hz — 990Hz

IEEE-488

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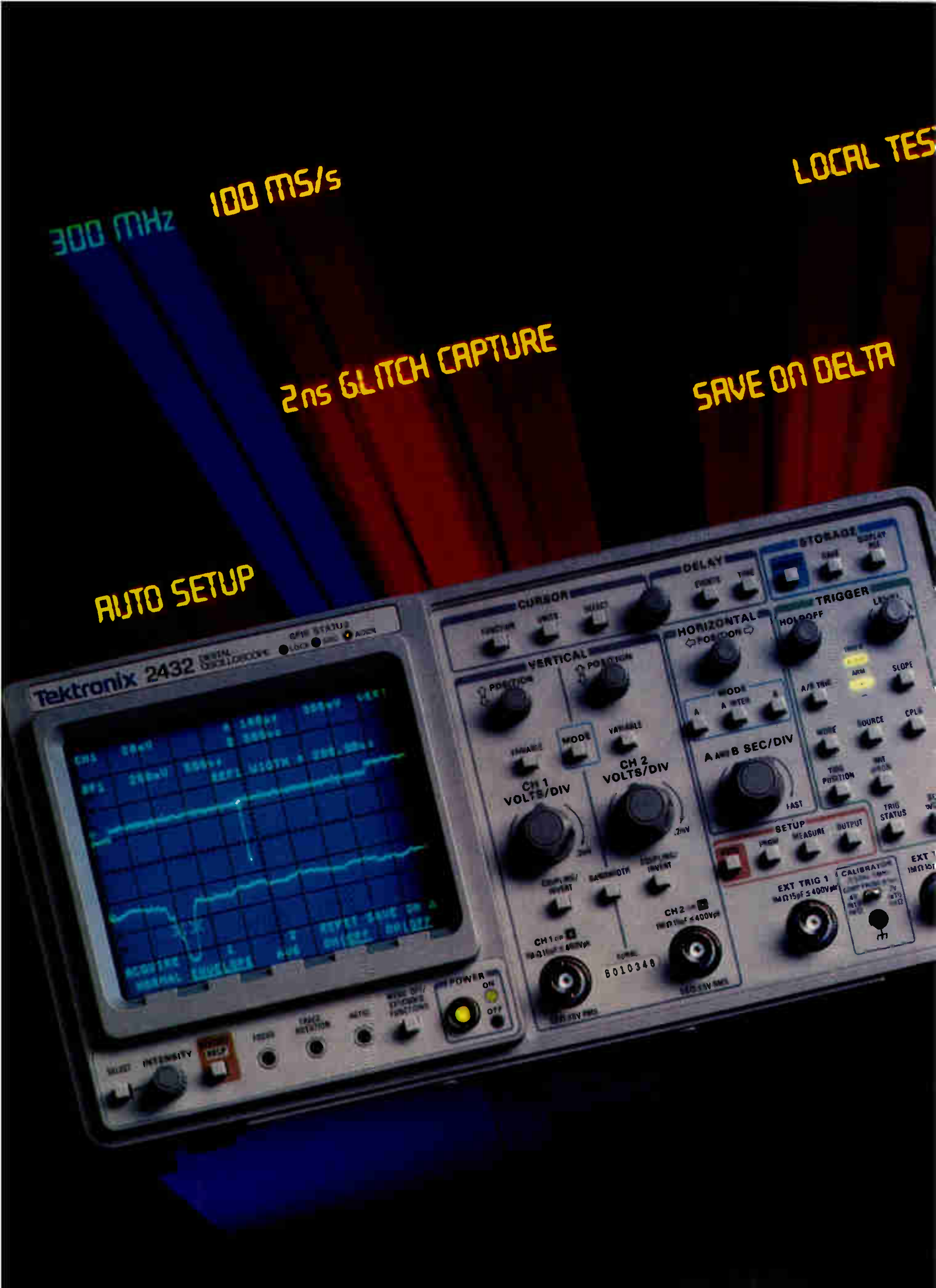
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100 MS/s
LOCAL TES
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SAVE ON DELTA
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Tektronix 2432

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The 2432 and its 150 MHz version—the 2430A—operate like the analog scopes you're used to. They offer a familiar front panel and simple, one level menus. And powerful new features put less time between you and results.

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TODAY'S STANDARD Tektronix 2400 Series Digital Oscilloscopes

Features	2432	Now lower-priced! 2430A
Dual-Channel Bandwidth	300 MHz	150 MHz
Digitizing (Sampling) Rate	100 MS/s	100 MS/s
Max. Sweep Speed	2 ns/div	5 ns/div
Record Length	1K	1K
Vertical Resolution	8 bits	8 bits
Time-Base Accuracy	0.001%	0.001%
Glitch Capture	Yes (2 ns)	Yes (2 ns)
Printer/Plotter Out	Yes	Yes
GPIB	Standard (full programmability)	
Warranty	3-year on labor and parts, including CRT	
Price	$9500	$7950

Tektronix
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Circle 105 on reader service card

quickly enough. Generally speaking, the instrument of choice today for studying nonrepetitive pulses with rise times of less than 5 or 10 ns is still the analog storage scope.

Studying a pulse means being able to look at its features in detail, examining it for preshoot, overshoot, ringing, and the like. Since those phenomena tend to have durations on the same order as rise time, a sampling instrument suitable for studying such pulses will need to acquire many samples during the 5- or 10-ns period of interest. Whether any digital sampling scope now on the market is adequate for the task depends upon how many samples are needed. Ten samples doesn't seem like much, yet to get that number would require a sampling rate of 2 gigasamples/s for a 5-ns rise time—a rate beyond the capabilities of all but the most exotic and expensive of today's digital scopes (see table, p. 117).

THAT'S NOT WHAT NYQUIST SAYS

Many users fail to appreciate the limitations of sampling because of a popular misinterpretation of the Nyquist sampling theorem. They often think that satisfying the theorem requires only slightly more than two samples per period of the signal of interest in order to capture it completely. What the theorem actually says is that slightly more than two samples per period of the highest frequency present in the signal are what's needed to capture it completely. The two statements are equivalent only for sine waves.

For square waves, which have significant overtones beyond the 10th harmonic, the sampling theorem suggests acquiring more than 20 samples per period of the fundamental. It's only because the input amplifiers of most oscilloscopes act as low-pass filters that users can get away with sampling at rates lower than Nyquist really demands. This also means that they do not know what their signals really look like, a drawback that holds true with analog scopes as well.

Be it analog or digital, a 100-MHz scope—that is, one in which the input amplifiers have a bandwidth of 100 MHz—has a rise time of 3.5 ns. If a signal displayed on such a scope appears to have a rise time of about 3.5 ns, then its rise time is a lot less than that figure. Also, its amplitude is greater than whatever is being displayed. If the displayed rise time is somewhat greater than but close to 3.5 ns, then the well-known formula relating the rise time of the displayed signal to the rise time of the scope and the rise time of the actual signal can be used to calculate the real rise time ($t_{DISP}^2 = t_{SCOPE}^2 + t_{SIGNAL}^2$).

According to this formula, a signal with an apparent rise time of 4 ns as displayed on a 100-MHz scope actually has a rise time of slightly less than 2 ns. This is a significant error of a type that users probably make every day with analog scopes. While it is true that analog scopes generally do not lead the unwary as spectacularly astray as digital scopes can, neither is it true that they can always be relied upon to tell the whole truth. As the formula reflects, the effects of scope rise time become insignificant for signals having rise times that are several times longer than that of the instrument.

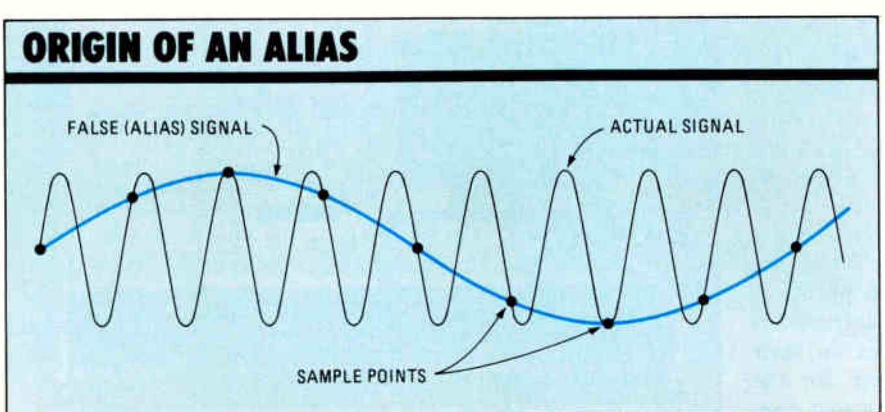
For low-frequency single-shot events, the picture is very different. In such applications, the digital scope can really strut its stuff. For example, a switch closure or a power-supply startup transient with no energy above, say, 20 MHz can be very advantageously studied by a digital scope having a sampling rate of 50 megasamples/s. Memory permitting, the digital scope can store a long record, which can then be exploited with various zoom and expansion features to allow for detailed study in ways that analog scopes simply cannot approach. Moreover, the signal will not fade over time, as it will with analog storage.

Of even greater importance in some applications, digital scopes can present pretrigger information—that is, they let the user study what the signals were doing before the trigger event occurred. This feature can justify the purchase of a digital scope all by itself, because it means that the scope can trigger on a malfunction and then display what the signal was doing just before things went sour.

Key to this capability is the fact that a digital scope can be set to acquire data constantly in the absence of a trigger. When its memory fills up, it simply writes over the contents, so the scope always has the most recent data stored. Then, when the trigger event occurs, the scope stops acquiring data and displays the events leading up to the trigger, to the limit of its memory. More commonly, users set the trigger position to some intermediate point so that some pretrigger data is displayed along with some posttrigger data.

When the ability to look back in time from the trigger point is a major reason for using a digital scope, the size of the acquisition memory takes on great importance. Many digital scopes have only 1 or 2 Kbits of such memory behind each channel, but some have much more. The Data Precision Data 6100, for example, has 128 Kbits, and the LeCroy 9400 has 32 Kbits.

Besides making it possible to look at pretrigger events and to manipulate stored signals for as long as the operator wishes, most digital scopes have at least some ability to average signals



1. Sampling the 1-KHz actual signal at 900 samples/s—instead of at the required rate of more than 2 kilosamples/s—results in an alias at the difference frequency of 100 Hz.

and to extract pulse parameters automatically. Some of these scopes, such as the members of the Tektronix 11000 series and the Hewlett-Packard 54100 family, reduce the task of measuring, say, rise time to pushing a single button. Others—the Philips 3320, for example—give the operator more control over complex waveforms, by requiring that, before the button can be pushed, one cursor be positioned near the bottom of the pulse edge and a second cursor near the top. The scope then moves the cursors to the 10% and 90% points, measures the time between them, and displays the result. In both cases, the measurement is made without any reliance on human judgment, so the results are repeatable from day to day and from operator to operator. Of course, it is also possible to position the cursors manually and to have the scope merely read out the time interval between them.

Another advantage of some digital scopes is computational capabilities that can put a computer to shame. The Data Precision Data 6100, for example, can perform fast Fourier transforms, calculate correlation functions, and even perform complex test sequences in which conditional branching modifies the test sequence depending upon intermediate results.

For all their advantages, however, digital scopes can still cause trouble for users—even in studying moderate-speed, single-shot events, to which digitals are extremely well-suited. Just because the instrument is capable of making the measurement doesn't mean that it can't also be misapplied. For example, problems can even arise if the scope is used to view switch-closure or power-supply transients, both of which are characterized by rather long durations coupled with fairly high frequency content, which all but invite the user to set the sweep speed too low. Here, the trap into which the unwary may fall is related to the depth of the acquisition memory.

If a signal has a duration of 2 ms and yet has frequency components as high as 20 MHz, the scope will need to sample it at, say, 50 megasamples/s for 2 ms, during which time a total of 100,000 samples will be acquired. But very few scopes have that much acquisition memory. Nevertheless, the user will probably set the sweep speed to 200 μs per division, which will spread the 2-ms signal across the full width of the screen. In most digital scopes, the sweep speed sets the sampling rate so as to just fill the available memory with one screenful of data. In the case of a 200-μs/division sweep speed and, say, a 4-Kbit memory, the sampling rate will be 2 megasamples/s, not the required 50 megasamples/s.

This is the kind of situation in which aliasing typically occurs. Aliasing is the result of undersampling a signal—that is, sampling it more slowly than the Nyquist sampling theorem mandates. The result can be very misleading: the display will show a signal that simply does not exist. For instance, if a 1-KHz sinusoid, which should be sampled at more than 2 kilosamples/s, is sampled at a rate of 900 samples/s, an alias will be generated at 100 Hz (see fig. 1).

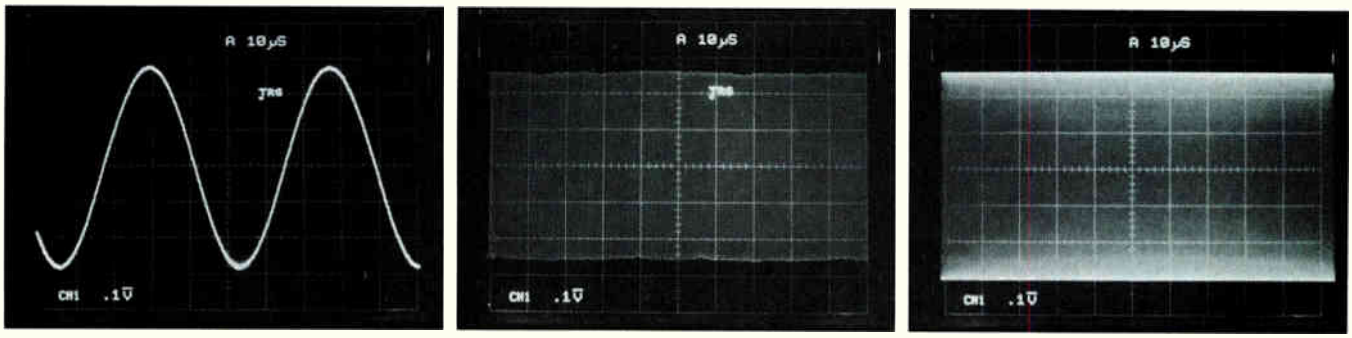
Nothing is foolproof—just because the instrument is able to make a measurement doesn't mean that it can't be misapplied

Fortunately, there are a variety of means available for detecting aliasing. Probably the simplest and most commonly used technique is to speed up the sampling clock by speeding up the sweep rate. If the only effect is the expected time-scale expansion, then there is no aliasing problem. If the very nature of the signal changes, then the first signal probably was an alias.

Another means provided by most scope makers is the min-max mode, which actually plots two amplitude values at each horizontal point instead of the usual one. In this mode, the sampling clock runs at full speed, capturing as many intermediate points as it can between the points that will be plotted.

For the example of a sweep speed of 200 μs/division and a 4-Kbit acquisition memory, the clock will run at its top speed of, say, 100 megasamples/s, grabbing a sample every 10 ns. However, since the memory doesn't have room for all of those samples, the scope stores and displays the largest and the smallest values that it sees between its 4-megasample/s sample points. That is, every 250 ns, it stores the minimum and maximum values that it saw during the interval just ended. When the scope creates a display from the stored data, it shows both the minimum and maximum values (see fig. 2). If there is no aliasing, there will be very little difference between the normal display and that of the min-max mode. However, if there is aliasing—that is, if there are significant signal excursions between sample points—then the min and max points will be widely separated and the display will clearly indicate that.

Yet another digital-scope feature that can be used



2. A sweep speed of 10 μs/div is much too slow to display a 10-MHz sinusoid, as shown on this Kikusui COM 7101A combined analog/digital scope, and results in aliasing (left). Turning on the digital envelope mode (center) or the analog mode (right) clearly shows that something is awry.

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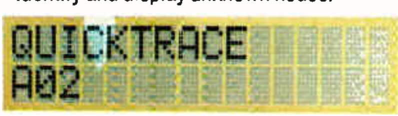

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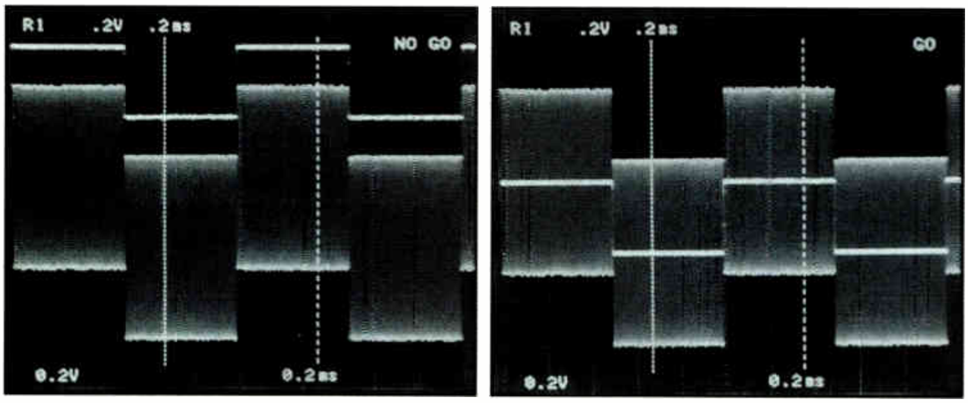
Manufacturer	Model No.	Analog bandwidth (MHz)	Digital bandwidth (MHz)	Sampling rate (Msamples/s)	Number of channels	Per-channel acquisition memory depth (kilobits)	Vertical resolution (bits)	Comments	Circle No.
Data Precision Div. Analogic Corp. Danvers, Mass. (617) 246-1600	DATA 6100	Has no analog mode	0.1 to 1,000 (Note 1)	0.1 to 250 (Note 1)	2 to 4 (Note 1)	16 to 64 (Notes 1, 4)	8 to 16 (Note 1)	Extensive computational capability, including extremely high-resolution FFT processing; up to 10-ps timing resolution on repetitive waveforms.	380
Gould Inc. Test & Measurement Cleveland, Ohio (216) 361-3315	4072	Has no analog mode	100	400	2	1	8	5-ns glitch capture; includes integral 4-color plotter; optional key pad on a pod does limit testing and signal processing, and stores setups.	381
	4074				4				
Hewlett-Packard Co. Palo Alto, Calif. (contact local sales office)	54110D	Has no analog mode	1,000	40	2	1	7	Color display; 4-bit pattern trigger; waveform algebra and automatic measurement of pulse parameters.	382
	54111D		500	1,000	2	8	6 to 8, depends on speed		
	54120T	Has no analog mode	20,000	Note 2	4	1	12	Color display; includes time-domain reflectometer; up to 0.25-ps timing resolution on repetitive waveforms; automatic measurements.	383
Hitachi Denshi Ltd. Woodbury, N.Y. (516) 921-7200	VC-6165	100	100	100	2	4	8	Has traditional front-panel layout; X–Y display in storage mode; analog outputs.	384
Iwatsu Instruments Inc. Carlstadt, N.J. (201) 935-5220	DS-6121	100	100	40	2	2	8	Extensive computational capability; go no-go comparisons against stored waveforms; analog and digital plotter outputs; choice of pulse, curve, and vector (linear) interpolation.	385
	SAS-8130	Has no analog mode	12,400	Note 2	2	1	10	Less than 20 ps of jitter; useful for time-domain reflectometry; automatic measurement of pulse parameters.	386
Kikusui International Corp. Torrance, Calif (213) 371-4662	COM 7101A	100	100	50	4	1	8	Envelope modes uses analog peak detector; 20-ns glitch capture.	387
	COM 7201A	200							
LeCroy Corp. Chestnut Ridge, N.Y. (914) 425-2000	9400	Has no analog mode	125	100	4	32	8	Up to 200-ps timing resolution; dual zoom for two expanded traces; extensive computational capability, including FFT processing.	388
Nicolet Test Instruments Div. Madison, Wis. (608) 273-5008	4094	Has no analog mode	0.05 to 100 (Note 1)	0.1 to 200 (Note 1)	4 (Note 3)	8 (Note 4)	8 to 15 (Note 1)	Extensive computational capability, including FFT processing; Autocenter feature allows single-cursor selection of any waveform feature, or shifts horizontal cursor to analog zero voltage.	389
Philips/Fluke Everett, Wash. (206) 347-6100	3320	Has no analog mode	200	250	2, plus trigger view	2 (Note 4)	10	Can display up to 8 waveforms at once; cold switching for enhanced reliability; soft keys ease user interface.	390
Tektronix, Inc. Beaverton, Ore. 800-426-2200	2432	Has no analog mode	300	100	2	1	8	2-ns glitch capture; go/no-go comparisons against stored waveforms; fast update rate for 'live' feel.	391
	11402	Has no analog mode	1,000	20	8	2 (Note 4)	10	Very fast update rate for 'live' feel; extensive computational capability, including waveform calculus; automatic de-skew assures accurate channel-to-channel measurements.	392
	7250	Has no analog mode	6,000	1,000,000	1	0.5	11	Based on scan-converter technology; trigger jitter below 100 ps; automatic waveform parameter measurements.	393
	7854	400	14,000	0.5	2	1	10	Time-domain-reflectometry capability; plug-in system with several heads; extensive computational capability.	394

Notes: 1. Depends on plug-in.
2. Slow. Scope is for repetitive signals only.
3. With two plug-ins, each having two channels.
4. More memory is available if all channels are not active.



The go/no-go feature shown here on the Iwatsu VC-6165 sets upper and lower bounds for the input signal. The scope can be set to trigger when the signal falls out of bounds.

that do use sequential sampling need more front-end gain than do their lower-frequency counterparts, and so their signals tend to be much noisier.

Regardless of the type of sampling used, the ratio of effective sampling rate to signal frequency for repetitive signals tends to be so high that the aliasing problem all but disappears. Nevertheless, some users still refuse to believe that a digital scope is telling the truth until its accuracy is confirmed by an independent witness, namely an analog scope. Realizing that, some scope makers include an analog scope in each of their digital units. With those scopes, simply pushing a button switches operation between stored and real-time operation.

The Iwatsu Model DS-6121, the Hitachi VC-6165, and the Kikusui COM 7101A and COM 7201A all combine an analog scope and a digital unit under the same roof, which their makers feel is the best way to deal with users' reluctance to trust straight digital scopes. Manufacturers who do not include analog capability tend to stress the superior display quality, higher reliability, and cost savings that accrue when the high-frequency CRT and associated circuitry required for real-time capability can be eliminated from an instrument. These makers feel that the best way to deal with aliasing is through user education and higher sampling rates.

Automatic signal finding—an extremely convenient feature provided by most manufacturers in both groups—offers antialiasing insurance almost as a side effect. What Tektronix and Philips call Autoset, Hewlett-Packard calls Autoscale, and Gould calls Auto/set-up, automatically sets the horizontal and vertical scales, and sets up the triggering so that a stable signal is displayed on the CRT. Since these automatic features start at the highest sweep rate and step down until they get to the optimum rate for the signal being viewed, they greatly reduce the possibility of aliasing.

Users often can get emotional about their oscilloscopes in a way that they don't about other instruments. They tend to feel that scopes should have certain controls in certain positions and should respond to them in traditional ways. This puts digital-scope makers in a peculiar position. Their latest products have so many features that providing access to them through traditional controls, with switches and knobs dedicated to each function, would require an enormous front panel. In consequence, some manufacturers have adopted a menu-driven user interface.

By giving the user a set of appropriate choices at each step in the setup process, a menu makes the instrument easier for the infrequent operator to use. At the same time, it penalizes the expert by forcing him to walk through that same series of steps, when he knows exactly where he wants to go.

In general, digital scopes that offer a great deal in the way of preprogrammed computational capability tend to use menus, while the others have a more traditional user interface. In what may well be the wave of the future, Tektronix, in its 11000 series, shoots for the best of both worlds. Scopes in the 11000 series use menus, but the menus are so designed that the most frequently used functions—the vertical and horizontal scale controls—are always accessible.

One of the biggest criticisms leveled against digital scopes has been their low update rates, in comparison with analog units. Where the time between sweeps in an analog scope is so fast that it appears instantaneous, some digital scopes acquire only two or three traces per second. The result is that users are always aware of the fact that the signal they are watching is slightly stale.

Although not of great significance in most applications, this shortcoming can be very annoying when the operator is making an adjustment and observing its effect on the scope. An instrument with a slow update rate will lag behind as a potentiometer is turned, forcing the user to slow down or even backtrack. Scope makers are all well aware of this problem. Their latest introductions tend to be much improved in this respect over their predecessors. Tektronix, in particular, has paid a lot of attention to this problem, developing proprietary display-control ICs that boost update rate enough to give its scopes a 'live' feel. Under some conditions of trigger rate and sweep speed, Tek's 2432 updates its display at better than 100 Hz. The 11400 series is even faster. Although Tek has the lead in this area right now, other makers have improved on their earlier products. Before this year is out, several new introductions are expected, almost all of which will have fairly high screen update rates.

Another selling point for these new scopes will be well-designed front panels that will make them more attractive to users of conventional scopes. Most important, this new breed of digital scopes will cost appreciably less than earlier versions. While still more expensive than their analog counterparts, they will drastically narrow the price gap between analog and digital scopes, bringing the day much closer when cost difference is no longer a major issue. And that, when all is said and done, is what everyone is waiting for.□

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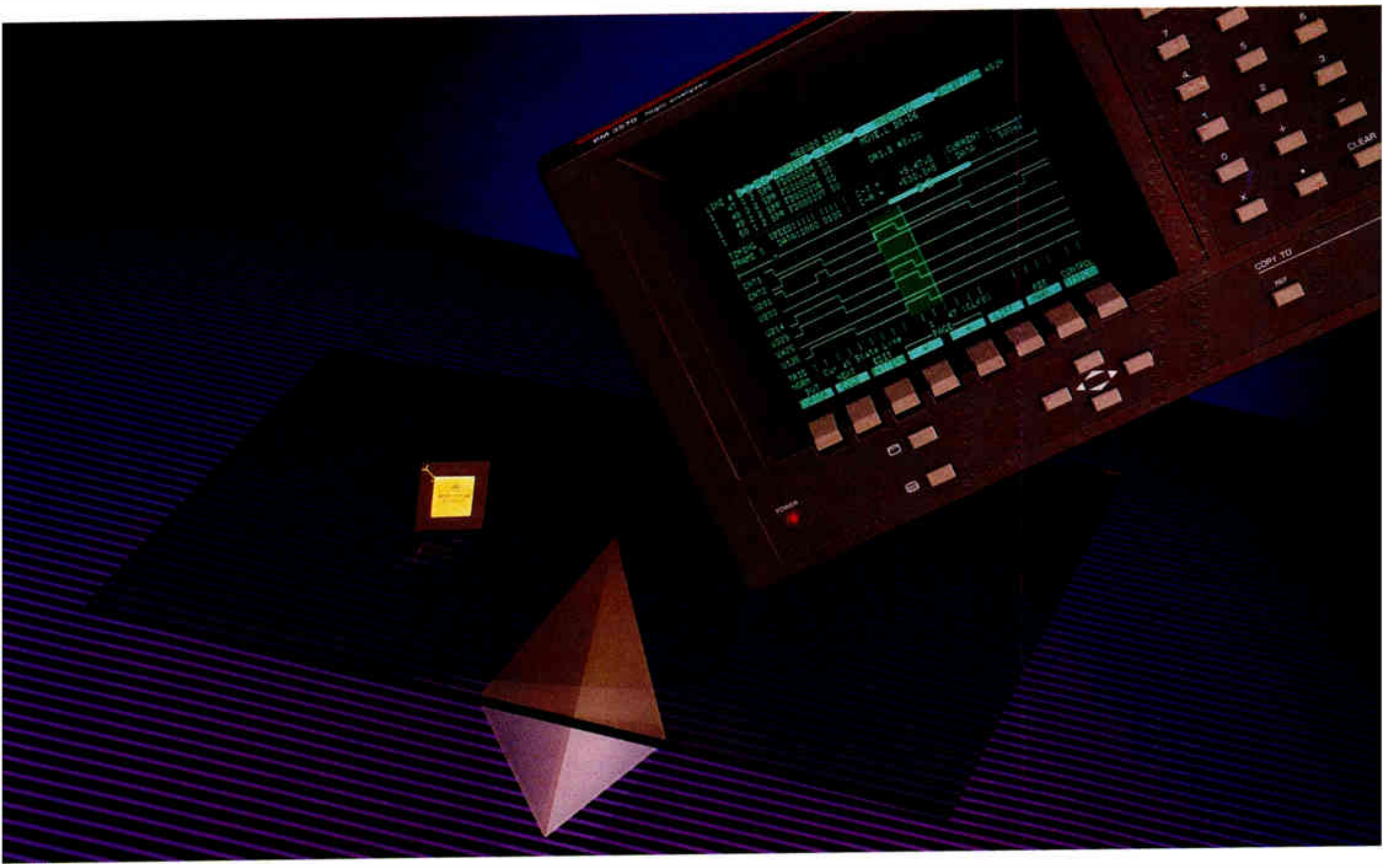

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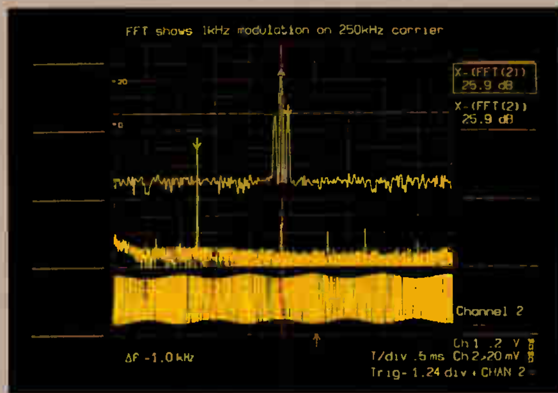
The 9400's familiar "analog" front panel and its unique instantaneously-updating display make it an easy to use yet complete test and measurement instrument.



An amplitude modulated signal is analyzed using the 9400's FFT capability. Expansion reveals a 250 kHz carrier with 1 kHz sideband.

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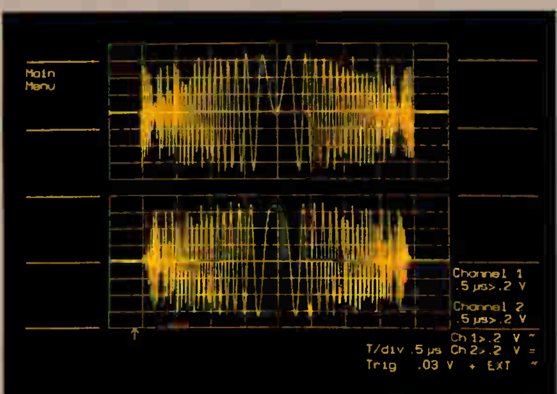

9100 outputs duplicating radar "chirp" pulses in phase quadrature measured with Model 9400 DSO above.

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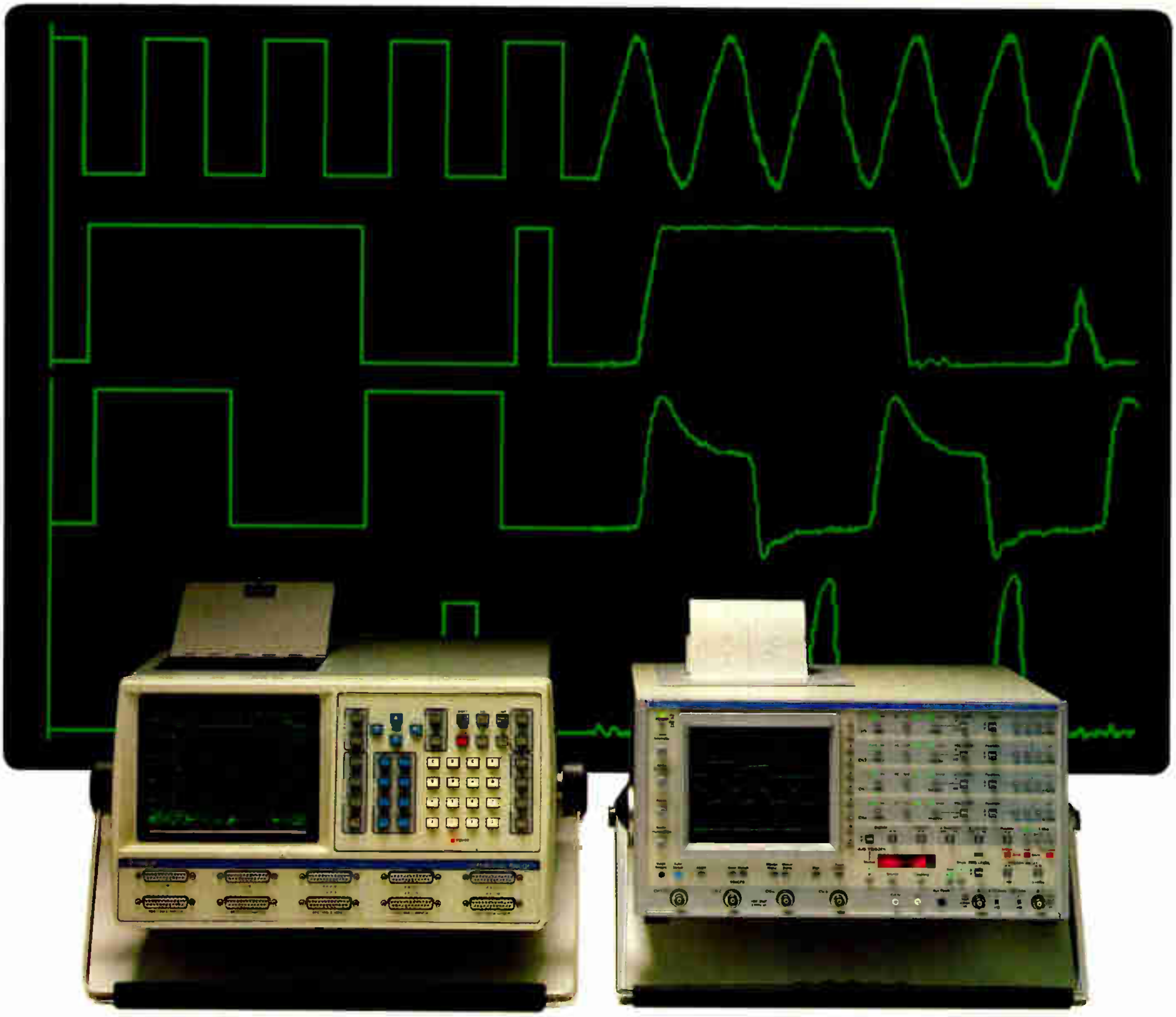

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THE SYSTEM DMM BECOMES A FAR MORE POWERFUL TOOL

The new DMMs are as accurate at the end of a year as their predecessors were at the end of a day, and accuracy isn't the only achievement—they're smarter, faster, and more versatile, making them indispensable for more tasks than ever before

by Rex A. Berg, *Hewlett-Packard Co.*

The ubiquitous system digital multimeter is quietly turning into a far more powerful instrument. First off, it's a lot more accurate—ten years ago, an absolute dc-voltage accuracy of 80 parts per million per year was a respectable long-term accuracy for a DMM having a calibration cycle of 90 days; today, the best DMMs offer 5 or 10 parts ppm per year. In fact, many of the new DMMs are as accurate at the end of a year as their predecessors were at the end of a day. Moreover, their mean time between failure has been extended from hours to years. What was accepted as the price of high performance in years past—low reliability—is not tolerated nowadays. Even the most complex DMM on the market now boasts a mean-time-between-failure rate of at least 20 years.

But it's not just in accuracy that DMMs have gained. Advancing technology is making today's DMM smarter, faster, and more versatile than its predecessors. These changes are making it indispensable for more tasks than ever before.

The DMM is part and parcel of virtually every computer-aided test system, and is often embedded in systems dedicated to specific tasks such as linear-circuit testing, in-circuit board testing, assembly functional testing, and process control. Besides offering full programmability through the GPIB (the IEEE-488 general-purpose instrument bus), it has become a full-fledged talker/listener on the GPIB, automatically controllable for all measurement functions. And although accuracy and speed have improved by orders of magnitude over the last 10 years, the DMM's price has remained low: a unit with fairly high resolution of 5½ digits costs only $1,000.

Together with greater intelligence, the enhanced performance of the system DMM is increasing test throughput, improving production yields, and offloading the GPIB control computer. Moreover, the system DMM can now measure much more than traditional steady-state dc voltages. Nowadays, it can often double as a counter/timer or serve as a digitizer for measuring dynamic signals. In addition, electronic calibration and higher reliability have led to significantly longer DMM uptime.

And with the wide choice of DMMs now available, users can find the right instrument to fit any job or budget. As a rule, system DMMs fall into three classes: low-cost, midrange, or high-performance, which have prices ranging from about $1,000 up to $8,000 or so (see table, below). For modest measurement needs, there is a large selection of lower-cost models from which to choose. It is easy to find moderate accuracy of 50 ppm, moderate speed of 5 readings/s, and mod-

FOR SYSTEM DMMs, A THUMBNAIL SKETCH OF PERFORMANCE

Parameter	Low-cost	Midrange	High-performance
Price	$1,000 to $2,000	$2,000 to $4,000	$4,000 and up
Resolution *(digits)*	5½	5½ to 7½	6½ to 8½
Measurement speed *(readings/s)*	10 to 1,000	10 to 1,500	10 to 100,000
Dc voltage accuracy *(ppm over 24 h to NBS)*	30 to 50	10 to 30	2.5 to 10
Relative accuracy *(ppm over 24 h to calibration standard)*	greater than 30	5 to 30	0.5 to 5
Transfer accuracy *(ppm)*	Not specified	2 to 10	0.1 to 2
Linearity *(ppm)*	greater than 5	0.5 to 5	0.1 to less than 0.5
Long-term stability *(ppm over 1 yr)*	greater than 80	30 to 80	5 to 30
Short-term stability *(ppm over 1 h)*	Not specified	2 to 4	greater than 0.1 to 2
Repeatability *(ppm)*	Not specified	2 to 10	0.05 to 2

multiplier of 100 would measure to within 5 V ± 0.002 V, and the loss in yield would be a nominal 0.02%. In the extreme, if the margin were the same as that of the DMM, only those devices that tested perfectly would be able to pass.

In many applications, another important consideration is DMM versatility, or how many measurement functions the instrument offers in addition to dc voltage. Most DMMs measure both ac and dc voltage, as well as resistance; and many offer current measurement. Several of the new system DMMs add frequency measurement along with period counting, functions that allow the DMM to double as a counter. The frequency range corresponds with the frequency range of ac voltage measurement. For example, the frequency range of the new high-performance HP 3458A spans 1 Hz to 10 MHz; for the midrange 3457A, it covers 10 Hz to 1.5 MHz. The period-counting capability is simply the reciprocal of the frequency range.

A DMM's frequency capability is particularly useful for making low-frequency measurements, and that capability brings a twofold benefit. The user gets an extra measurement function, and therefore may not need to buy a frequency counter. Moreover, since the DMM is isolated from ground, he can preserve the ground isolation in his system by making a floating frequency measurement, a feature that most frequency counters don't offer.

Now that the system DMM is inherently intelligent because of its resident microprocessor, the ability to execute mathematical operations has become rather commonplace and in the process has contributed to DMM versatility. The DMM now performs many of the measurement computations, such as ratios, that formerly required separate circuitry. A good many DMMs can now compute their own statistics (mean, standard deviation, maximums and minimums); make decisions on pass/ fail limits for reporting out-of-limit measurements; provide alarm outputs (audio, visual, or a TTL-compatible signal) to flag failures; store measurement readings in memory for complete data retrieval later; and remember instrument setups (states) and measurement sequences for faster communication between the GPIB control computer and the DMM during testing.

In fact, because of its versatility, the system DMM has even begun to enter, albeit quietly, into instrument realms that have been the exclusive domain of oscilloscopes and spectrum analyzers. Provided it has adequate measurement speed, timing accuracy, and input bandwidth, the DMM can digitize dynamic signals, typically, with more resolution than most digital scopes offer. Those dynamic signals can have frequency components of up to half the reciprocal of the DMM sampling period.

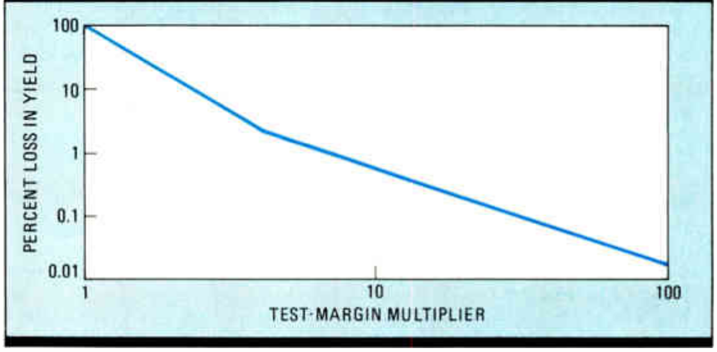
As a result of this digitizing capability, the performance of the system DMM is being characterized by some nontraditional DMM parameters, including aperture, dynamic linearity, timing jitter, and trigger latency (see table, next page). Usually, the DMM is called upon to measure an event that is in a steady state, but it is not restricted to them—the new breed is measuring dynamic signals, too.

By measuring dynamic signals, the digitizing DMM can team up with the GPIB control computer to form a low-frequency oscilloscope or a low-frequency spectrum analyzer. With the aid of the fast Fourier transform, waveform-analysis software can easily turn the DMM's high-speed measurements into frequency spectrum graphs of the test signal with more than 96-dB dynamic range. Or, the DMM can generate time-domain plots directly from the data it captured for other parametric information like pulse width, rise time, and overshoot. Of course, the system DMM is not intended for real digitizing in the normal sense of the word. However, if the test signal is within the DMM's frequency capability, the combination of the DMM and the automatic test equipment's computer display makes an inexpensive way to see the waveform of interest in any system.

Because of its fast reading rate, the digitizing DMM can be the central measuring device for the dynamic testing of analog-to-digital and digital-to-analog converters as well as telecommunications devices such as codecs and universal asynchronous receiver/transmitters. In this case, the high-speed DMM not only measures static data to full resolution and accuracy but also tests dynamic characteristics to their limits. Even when the converter's performance exceeds that of the DMM for direct measurements (the converter may be faster), the resolution of the DMM and its timing capability allow the indirect measurement of dynamic performance. For example, in the case of a high-speed (say, 1 MHz), high-resolution (say, 16 bits) DAC, the measurement of dynamic linearity can be inferred from the FFT of the digital pattern given to the DAC to convert at its rated speed. If that digital pattern were a sine wave, any deviation from the desired pattern would show up in the FFT as a spurious response that would be attributed to some failure mode in the DAC. Clearly, it is essential that the DMM not be the cause of the spurious response.

The technological advances that have vastly expanded the system DMM's usefulness have also affected the cost of ownership. That cost includes not only the price of the DMM itself, but also the expense of maintenance and any downtime associated with that maintenance, including keeping the instrument in calibra-

INCREASING PRODUCTION YIELDS



When the test margin of the system DMM is significantly higher than the limits for the device under test, production yields go up.

THE DIGITIZING DMM: WHAT THE SPECIFICATIONS MEAN

Aperture:
The width of the sample window the DMM uses to acquire samples of the signal to be measured.

Jitter:

Aperture jitter:
The short-term variation of the width of the sample aperture window.

Timing jitter:
The short-term variation of the timing between sample points.

Trigger jitter:
The short-term variation between the trigger event and the first sample point. Trigger jitter can be caused by amplitude variations on the trigger event as well as timing fluctuations in the trigger circuits.

Dynamic linearity:
A measure of the flatness of the input voltage response of the DMM's internal ADC when it operates at its rated maximum reading rate. Dynamic linearity is specified as either differential nonlinearity (a measure of the maximum deviation between adjacent points) or integral nonlinearity (a measure of the maximum deviation of any point from a least-mean-square fit of the actual response of the ADC).

Since most digitizing DMMs are characterized by the number of bits of resolution they provide, instead of the number of digits, linearity specifications are sometimes presented in terms of the least significant bit (LSB) of the conversion—for example, a differential nonlinearity of plus and minus 2 LSBs in the 16-bit mode of operation.

Timing Accuracy:
A measure of how closely the DMM's internal timebase tracks a known time standard.

Trigger:
The event that starts the sampling of the input signal. The trigger can be the input signal itself, another signal, or the GPIB controller.

Trigger latency:
The fixed time offset between the trigger event and the first sample point.

tion. The calibration cycle varies with the requirements of the application and the DMM.

Features like self-testing add very little to the cost of the DMM, but they can be a great way to gain confidence in how the instrument is working and can eliminate unnecessary repairs. Self-testing, however, does not assure calibration; it only adds confidence that the DMM is functioning. Somewhere a comparison with a standard is necessary to make sure that the instrument is calibrated. In the past, the DMM would go to the calibration lab, where a variety of test standards and adjustments was used to make the DMM meet its specifications. Nowadays, internal electronic calibration makes the job simpler, more foolproof, and more reliable. Electronic calibration has eliminated both the human drudgery and the human error, a significant source of uncertainty. At the push of a button, for example, the new HP 3458A's automatic-calibration function maintains the unit's accuracy by recalibrating all of the measurement functions to the internal references. Even the ac-voltage-frequency response is internally recalibrated to 10 MHz without the need of an external reference. And with just two external references (10 V dc and 10 Kohms) and a short, the HP 3458A can be completely calibrated to its 24-hour specifications for every function and range.

Which DMM a user chooses to buy will depend, of course, on his application. For the production test floor—assuming that the DMM meets the most demanding measurement requirement—then the order of priority for ranking DMM features should be measurement speed, setup speed, system uptime, and accuracy. In research and design areas and calibration labs, test margin holds the highest rank, followed by uptime and speed. In either production or R&D, when the DMM serves as a high-resolution digitizer, the priority ranking becomes the maximum reading rate, measurement resolution, bandwidth, triggering, and timing accuracy.

As for the future, one trend already affecting the system DMM is the emergence of instruments on a card. The industry standard here is VXI (VMEbus Extensions for Instrumentation), which is the instrument version of the VMEbus card cage. Overall, the market for system DMMs has been growing about 15% a year since 1975, but most of this growth has been in these so-called card-cage DMMs, which have been growing at twice that rate.

The stand-alone DMM will probably always offer an edge in measurement performance over the card-cage unit. However, for some high-throughput applications requiring low system-lifetime cost, the card-cage DMM offers several distinct advantages. It utilizes a common display in the instrument-card cage, an integral digital bus for rapid communication between the card-cage controller and the DMM controller, and a shared power supply. For example, the card-cage version of the HP 3457A DMM does not offer quite the accuracy of its stand-alone equivalent, but its speed of up to 80 measurement setups/s is nearly three times faster and it costs a few hundred dollars less.

On the whole, the natural trend in DMMs is to extend today's superlative performance to the commonplace and reduce the cost while doing so. Resolution and accuracy may further improve, but the emphasis is bound to be on higher-speed measurements and faster test setups. Right now, the system DMM is the fastest instrument in the test system over the GPIB, and there is need for a much faster scanner that can truly support switching test signals to the DMM at a speed of 100,000 channels/s and with 16-bit integrity. In the future, the line between the system DMM and the digitizer—whether it is a digital scope, a waveform recorder, or a waveform analyzer—will get even fuzzier. Some DMMs of tomorrow may even offer CRTs for their displays. □

Rex A. Berg, a product marketing engineer at Hewlett-Packard's Loveland Instrument Division in Loveland, Colo., has been involved with the introduction of three major system DMMs in less than 10 years. He works with a design team to help define, introduce, and support a new DMM—and, when the time comes, to phase out that product in an orderly way. He has written numerous articles since joining the company in 1973, when he graduated from Purdue University with a bachelor of science degree in physics.

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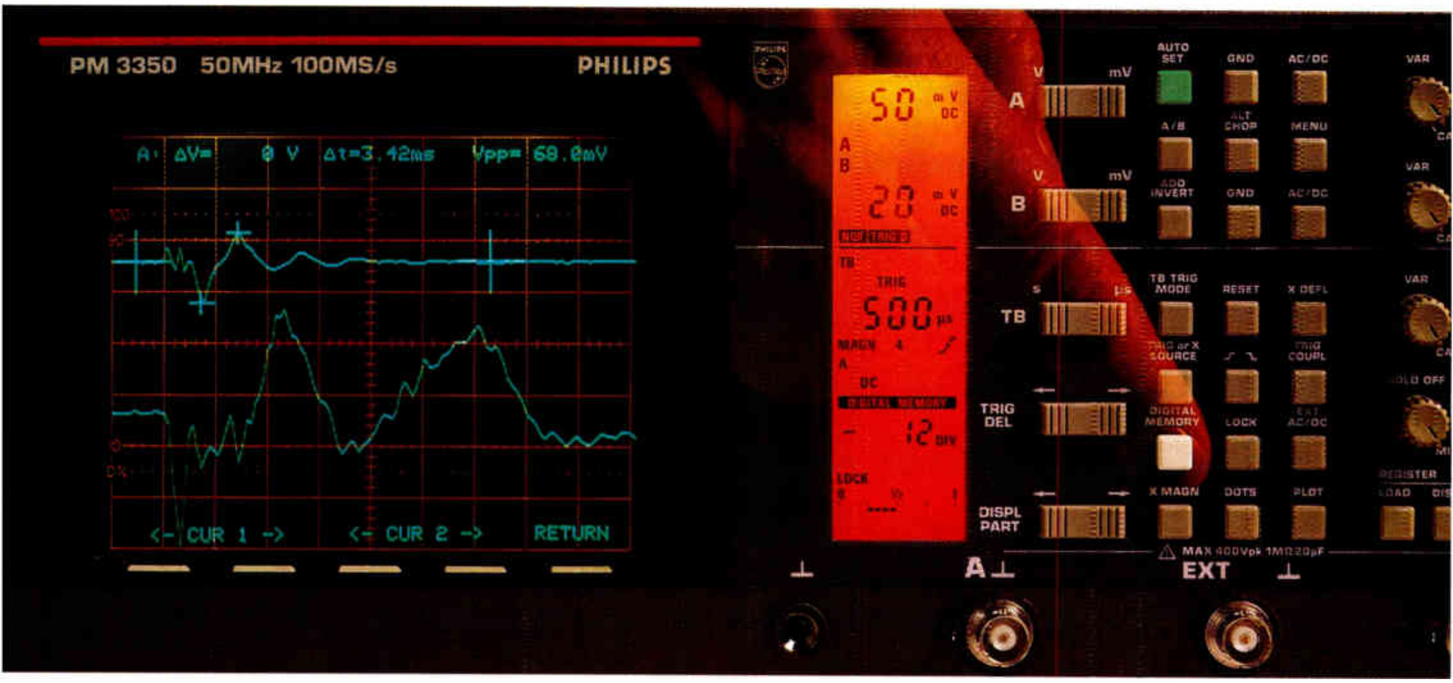

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BUILDING BIG SYSTEMS TAKES HARDWARE LOGIC ANALYZERS

Simulators and layout tools can be a great way to build the wrong design faster—and that's where logic analyzers come into play, because they can take on the signal, protocol, and state analysis needed to debug complex digital hardware designs

by Doug Boyce, *Tektronix Inc.*

All too often these days, automation can be a powerful tool for building the wrong design faster. Although simulation verifies that the blocks lesigned satisfy the designer's test cases, it does not ;uarantee that the design is indeed what is required. 'urthermore, layout tools can put a lot of circuitry on . board in a fashion that precludes correct circuit peration when those tools are not given the proper nstructions regarding optimal placement, signal ternination, and power-supply decoupling.

In translating a design from schematic to circuit oard, computer-aided-engineering tools for simulation nd layout help eliminate possible bookkeeping errors. Iowever, these tools do not address the integration roblems. In particular, they ignore the subtle errors reated by incorrect or incomplete specification of ciruit functions, interface protocols, and fabrication reuirements for system modules.

The right tool—in fact, the only tool—for debug;ing complex hardware designs and their integration roblems is the hardware logic analyzer (see panel, . 132). As a design debugging tool, the hardware nalyzer must offer performance features usually asociated with timing analysis, which reflects the relaionships in time among a large number of signals vithin the digital system. As an integration tool, it lso must be able to trigger competently on a seuence of system signal values having associated urations.

Sophisticated new processors and affordable highensity digital ASICs, such as gate arrays with the quivalent of 100,000 gates, are placing new demands n the logic analyzer. As the instrument of choice for esigning, debugging, and testing digital systems, the nalyzer derives its power from its ability to track ifferent signal levels on numerous nodes and to deect combinations of signal values that occur in a articular sequence.

Before the emergence of ASICs, a board-level deign might contain one fairly complex logic module. s a result, the possible problems with the design vere fairly simple, usually involving signal integrity nd logic implementation. But today, hardware inteeration—the process of fusing together designs of odules to create a system—has become a critical ssue as well. In fact, hardware integration has now eached a level of difficulty comparable with the softvare bottleneck encountered when software engineers vere first working with the microprocessor.

The task of hardware integration hits snags when one of the modules in the digital system under development fails to function as it should. The hardware analyzer says which module is faulty by showing that module's interfaces (inputs and outputs) in terms that relate directly to system performance. Integration testing usually begins at the interfaces, because inputs and outputs provide the best clues to the behavior of the block being integrated.

A hardware analyzer is a basic tool for both design and integration because it can examine the system interfaces without unduly loading any of them. Three areas of concern are associated with the interfaces between the blocks of any digital system: signal, protocol, and state (see table, below). Signal analysis determines the quality, or integrity, of the digital signals within the system; protocol analysis pinpoints the sequence of signal transitions within the required timing intervals at control and data nodes; and state analysis monitors the actual data values and the sequence in which they are passed between modules. In broad terms, the analyzer helps to solve signal prob-

THREE-LEVEL HARDWARE ANALYSIS

SIGNAL ANALYSIS—Applies to any signal node
- Waveform abberations
- Noise margin
- Rise and fall times
- Overshoot and undershoot
- Connection errors

PROTOCOL ANALYSIS—Applies to a single internal data bus
- Timing margins on control signals
- Sequence of control signals
- Handshake operations on data transfers

STATE ANALYSIS—Applies to all data buses to a block
- Correlation of multiple data streams
- Long history of data transfers
- Block functional response to input data

function of connecting an additional probe channel to the system under test. For flexibility, most hardware analyzers include 8 to 10 channels per probe, with special emphasis on low capacitance and inductance so that the probe connection does not load the system under test.

The trend towards high-density surface-mount packages, like pin grid arrays, has made debugging a far more formidable task by significantly increasing the number of pins, or terminals, for a single device. Besides dramatically multiplying the number of signal nodes per device, those high pin counts are exacerbating the difficulty of probing and increasing the likelihood of poor physical connections.

All too often, device pins are so close together that it is really not possible to attach a probe to them. Attempting to do so simply causes the probe to short one pin to its adjacent neighbors. And frequently nowadays, tracing back a fault through the signal-generating logic reveals a simple failure caused by the lack of integrity of a physical connection, with signal nodes shorted to each other, shorted to power-supply lines, or not connected at all (an open circuit). The tight physical tolerances and complex mounting techniques of surface-mounted devices are particularly problematic with prototype boards (ones built for engineering purposes), because their tooling errors are showing up on boards that have untested logic designs.

Signal errors that are not the result of direct integrity problems are usually caused by incorrect logic—that is, an incorrect implementation of a functional block so that the correct input fails to produce the correct output. Signal errors can also be caused by the actual physical implementation of the system when that implementation fails to correctly control the analog nature of digital signals. That analog nature encompasses signal problems such as crosstalk, ringing, incorrect termination, and improper power-supply decoupling (see table, below).

Digital circuits built with different logic families exhibit different analog performance characteristics, which can interact with the hardware analyzer to impact the difficulty of debugging. For example, emitter-coupled-logic families and several of the new advanced CMOS standard-logic families have logic transitions and gate bandwidths capable of responding to pulses as narrow as 1.5 ns. In order to characterize problems in systems employing these logic families, the hardware analyzer must be able to respond to such narrow signal pulses and inform the user of their occurrence.

Specifically, the analyzer's probe and that probe's leadset interact with the system being tested because the system signal nodes are also driving the analyzer's input. As long as the analyzer is probing a node, the additional load on the system by the probe and leadset can sufficiently reduce the amplitude of narrow pulses so

COMMON ANALOG PROBLEMS

Crosstalk:
- Cause: Too close placement of multiple signals and their return paths next to a sensitive wire run, or the inductive coupling of a signal into a signal return path.
- Effect: Generates unwanted pulses on the affected signal. Those pulses are usually narrow, on the order of 1 to 25 ns. Clock lines are especially vulnerable.

Ringing:
- Cause: Without a defined or controlled impedance, the wire run for a signal is longer than the edge transition time of that signal will permit for faithful transmission of the signal.
- Effect: Violations of setup and hold times, extended instability of the signal, or undesired multiple clocking of sequential logic.

Termination:
- Cause: Incorrect termination, missing termination, or no pullup resistor.
- Effect: Slow transition times, logic levels out of specification, ringing, or clock pulses that are too narrow to correctly clock sequential logic.

Power supply:
- Cause: Failure to decouple high-current switching supplies properly, poor system grounding, or unwanted current loops
- Effect: Loss of noise margin due to differences in the reference levels between driving and receiving logic.

that the analyzer's input cannot detect them.

However, there are a couple of ways to detect very narrow low-amplitude pulses. One attractive approach is to use a high-performance digitizing oscilloscope to capture the pulse and display its full analog nature. The hardware analyzer, then, should be able to trigger that scope based on the occurrence of a group of digital signals. This is a powerful combination—the scope provides information on the narrow pulse and the hardware analyzer on the conditions causing it. Another method is to use a high-speed timing analyzer, one of the high-bandwidth, low-capacitance instruments capable of sampling pulses as narrow as 800 ps on up to eight channels. This choice has the added advantage of pinpointing the exact location of the rising and falling edges of these narrow pulses—and on multiple channels.

When it comes to debugging complex digital systems, protocol analysis has much broader ramifications than the usual definitions of communication protocols, like the ubiquitous RS-232 standard for serial communication or the IEEE-488 standard for instrument buses. In this case, protocol refers to the control information used to pass data between functional blocks in a system. Designing separate modules within a large digital system necessitates the development of local protocols within that system.

Developing a robust protocol that can account for potential error sources is not particularly easy and, therefore, not always done within a system design. Such an incomplete specification allows some system modules to use protocol in an unanticipated manner. As a result, because the information required is not always available, debugging sessions can uncover bizarre operations within the interface under test.

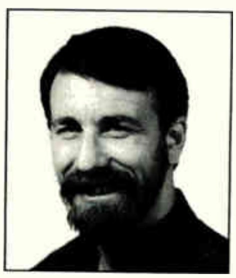
Debugging protocol problems begins with a review of the states of the control lines at the interface and the exact transition times associated with them. Frequently, design implementations contain signals in different gate paths that may combine into a single signal. The consequence is unwanted variation in the times when signal transitions occur. If the variation in a control line violates a protocol specification, signal transfers on control lines go awry.

Key features within its triggering capability allow the hardware analyzer to deal with protocol debugging. The analyzer's trigger creates a specific point of reference in time to flag exactly when the system under test stores data, and it presents information in a window around that time. The trigger may be programmed to monitor the control signals associated with the protocol and then trap an error condition within them. Trapping protocol errors requires a trigger machine capable of identifying initial conditions on the control signals, timing the period required until the next control signal condition, and following through the entire transfer.

Because it is easy to use, a hardware analyzer that does not offer many trigger features might be regarded as a blessing by some users. However, when attempting to do protocol debugging, those users will quickly discover that they do not have the resources they need to get the job done. Protocol bugs tend to be time-consuming to find and difficult to solve, so a feature-rich trigger system is essential.

State analysis provides an even higher level of information than protocol analysis about how a system is performing. State analysis does a good job of debugging both the flow of information within a system and the processing of data by the system. It suppresses control signals and timing information but emphasizes the data within the transfer block.

When the system under test employs



Doug Boyce is the business unit engineering manager for digital instruments in the Logic Analyzer Division of Tektronix Inc., Beaverton, Ore., where he oversees the development, design, and support of midrange logic analyzers. Boyce has 11 years of experience working with logic analyzers and has been with Tektronix for 14 years, ever since earning his BSEE from Washington State University in 1974. He holds one patent, as a coinventor for multiple timebase correlation in logic analysis.

standard buses, state analysis can readily monitor the flow of information processed by a system module. A microprocessor, for example, is a module usually debugged by state analysis, because operations within it are developed from standard buses, which use well-documented signal and protocol requirements. With custom buses, a system's signals and protocols are unique, making state analysis more difficult and causing the user to become very involved with the proper setup of the hardware analyzer to probe that custom system bus.

In state analysis, the hardware analyzer must be able to store the data streams that are based on the signal protocols used in the system. Such internal data streams between interfaces involve a mixture of serial and parallel buses. Consequently, a hardware state analyzer must be able to handle data rates of at least 50 MHz to deal with the broad range of hardware implementations now available to the digital system designer.

State problems are either fairly simple or complex and intermittent. For instance, some processing blocks always perform the same operation on data streams—a digital-multiplier block, for example, always multiplies two data streams together. With state analysis, the hardware analyzer can observe the multiplier's two input data streams and its output stream to verify correct operation.

Other system blocks, such as control modules for virtual memory, are more complex. A programming stream that may have occurred some significant time earlier can alter their operation. Verification of proper operation, then, must be based on the historical programming information, and that means it is vital for the hardware analyzer to maintain a history of that programming information. As ASICs incorporating larger random-access memory and more state variables become common, the hardware analyzer's ability to track and display instructions and multiple operand streams will become far more important for state analysis.

Yet another useful feature in state debugging is the analyzer's ability to compare large data blocks with known-good reference files. This feature allows the analyzer to trap block-size errors even if just a single data value at a single location in the block is different from the expected value.

Ultimately, the hardware analyzer must build a stronger link to simulation tools. It must relate actual information about system blocks—information regarding the timing of probed control signals and the state data sent to various internal blocks—to simulations of those blocks. The hardware analyzer cannot probe inside devices, but it can link physical measurements to the simulator, which does probe the internal information.

The development of such links will help the designer deal with the present disparity between the time required to simulate a complex system and the number of errors now found in the system when integration begins. There are still far too many errors. To do the job properly, the hardware analyzer must provide especially good timing resolution on exactly when pulse transitions occur. The simulator requires very accurate information about the edge placement of the signals, to help isolate potential timing-related design problems.

In the future, the hardware analyzer will also take on some of the higher-level data operations now common for the software analyzer. Those higher-level presentations of information include tracking data by symbolic mnemonic references, charting information by state maps that show the flow of signal control, and statistically analyzing data content (such as generating a graph of a data value over time). Symbol reference translates acquired data by means of a table of data values and reference names. More complex symbol translation can take into account the sequence of historical data values to develop a set of rules for the translation. To generate state maps, sequential data patterns that occur frequently within data blocks are assigned a higher-level name, much as symbol translation does with single occurrences of data values.

Even custom presentations of data will be possible when the hardware analyzer of tomorrow provides a standard interchange format for acquired data and passes that data to the user's computer. The user can then employ applications software to process the data in any manner. As both computer capability and design complexity grow, the user of the hardware analyzer can truly have the information he wants, the way he wants it.☐

MILITARY/AEROSPACE NEWSLETTER

ONLY 18 SUPPLIERS QUALIFY AS 'QUALITY VENDORS' FOR DESC

Only 18 of the 144 companies that applied made the grade in the first phase of the Defense Electronics Supply Center's Quality Vendor Program. The Dayton, Ohio, clearinghouse for military electronics is beginning the program in five product categories, including integrated circuits, communications equipment, and passive components. DESC plans to add five more categories to the list this spring. Among the 18 certified vendors are the Ground Systems Group of Hughes Aircraft Co., Control Data Corp., the Collins Defense Communications Division of Rockwell International Corp., and a number of distributors, including Schweber Electronics and Avnet Inc. Last August, DESC invited 5,000 suppliers to apply for certification in the program, which is designed to encourage contract officers to consider delivery and quality history as well as price when awarding contracts. ☐

MIMIC PROGRAM MANAGERS GIRD FOR A 22% CUT IN 1989 FUNDING . . .

One of the programs hit hardest by proposed cuts in President Reagan's fiscal 1989 defense budget is the Microwave and Millimeter Wave Integrated Circuits project, or Mimic. The program is due for a 22% reduction in funding, to $67 million, from its requested $86 million level. The program will cost $45.5 million in fiscal 1988, which ends Sept. 30. The cut's effect is not yet clear, says an official in the Pentagon's Office of Computer and Electronic Technology. "We're considering scaling back the Phase 1 awards," he says. But the biggest cutbacks will probably come in the program's ancillary third phase, which was to run concurrent to Phase 1 (Phase 2 won't start until 1991) and was to include development work in computer-aided-design, lithography, and automatic-test equipment. First-phase bidders are now negotiating final pricing for their bids, but it will be late April before contracts are let and costs are disclosed. That, in turn, will determine what's left for Phase 3. ☐

. . . AS THE IR FOCAL PLANE ARRAY PROGRAM IS PUT OFF UNTIL 1989

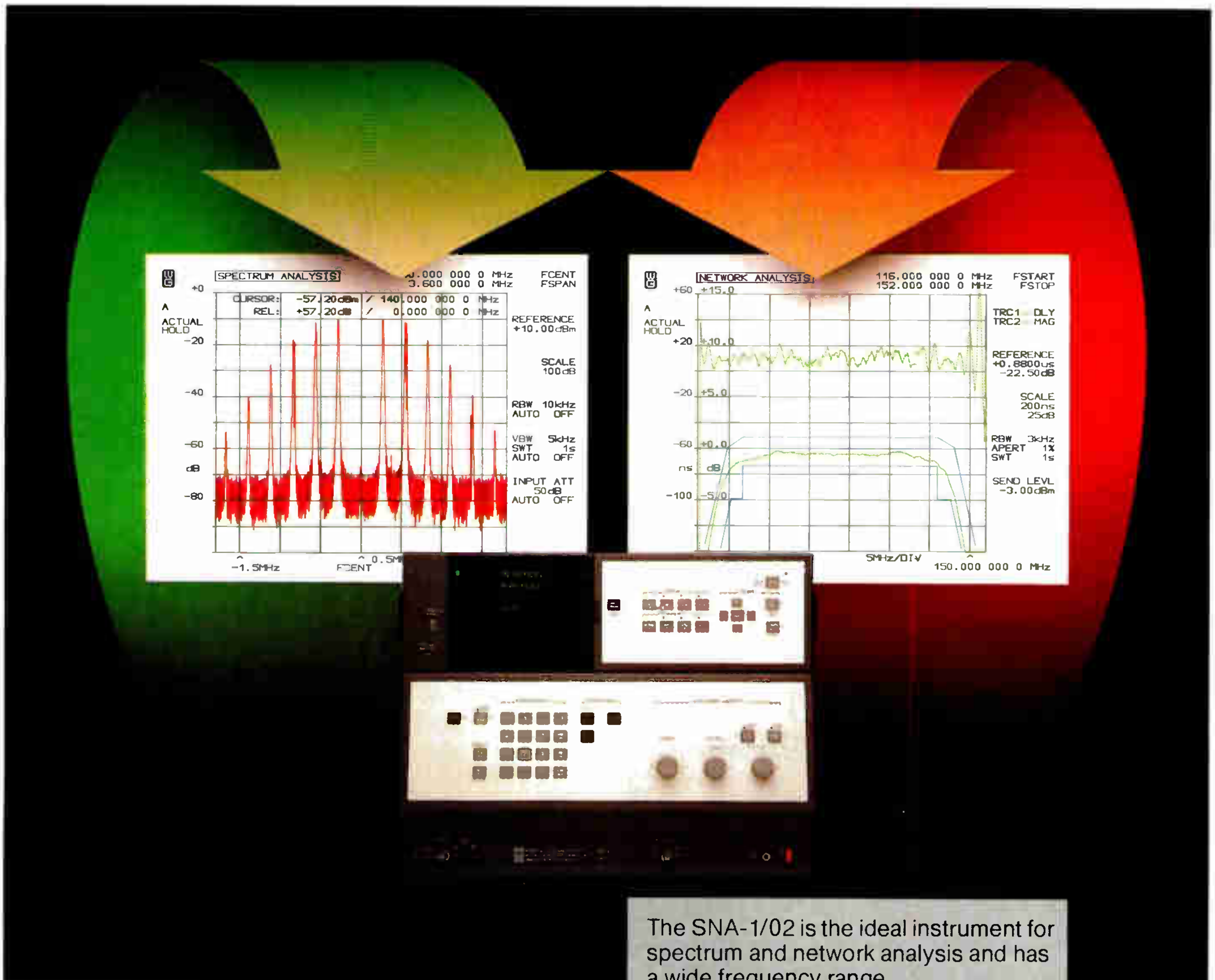
The Defense Department has decided to put off its Infrared Focal Plane Array Initiative until fiscal 1989 because of funding problems. The program got slightly less than $2 million for the current fiscal year, a far cry from the $45 million it had been seeking [*Electronics*, Sept. 3, 1987, p. 103], so program managers in the Pentagon's Office of Computer and Electronic Technology had to rethink the effort. Now the program is facing further cuts. President Reagan's proposed budget for fiscal 1989 asks for just $23.5 million, less than a third of what the program had been seeking. The Pentagon now hopes to get the program started in the fall. ☐

LOCKHEED DUSTS OFF ITS RADAM RADAR PROCESSOR

Defense electronics spending in fiscal 1989 will go heavily for upgrades and retrofits, analysts say, and Lockheed Electronics Co. plans to take advantage of that by pushing a radar processor that can see through camouflage and foliage. First conceived in the early 1970s, when there was a need for radars that could penetrate the dense Vietnamese jungles, the idea for Radam—Radar Detection of Agitated Metals—was shelved as the war ended. Now Lockheed is trying to bring it back. The Plainfield, N. J., company is offering Radam to the Army and another unnamed service as an enhancement for airborne radars that don't already have such capabilities. William Guyton, director of advanced programs in Lockheed's Radar and Fire Control Division, says Radam is "simpler than synthetic-aperture radar," a technique that creates a video image from the radar feedback and requires much more signal-processing power. ☐

Wandel & Goltermann

Electronic Measurement Technology



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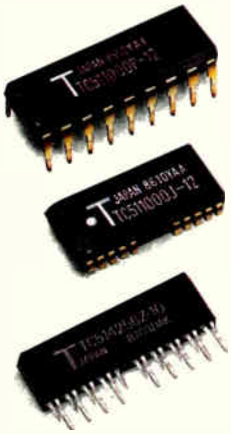
1 MB CMOS DRAMS



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Part Number	Org.	Process	Samples	Prod.	Speed Sorts Available	Pkg Options & Comments
TC511000P/J/Z	1MbX1	CMOS	YES	YES	85 100 120	P/J/Z
TC511000AP/AJ/AZ	1MbX1	CMOS	4/88	5/88	70 80 100	P/J/Z
TC511001P/J/Z	1MbX1	CMOS	YES	YES	85 100 120	P/J/Z
TC511001AP/AJ/AZ	1MbX1	CMOS	4/88	5/88	70 80 100	P/J/Z
TC511002P/J/Z	1MbX1	CMOS	YES	YES	85 100 120	P/J/Z
TC511002AP/AJ/AZ	1MbX1	CMOS	4/88	5/88	70 80 100	P/J/Z
TC514256P/J/Z	256KX4	CMOS	YES	YES	85 100 120	P/J/Z
TC514256AP/AJ/AZ	256KX4	CMOS	4/88	5/88	70 80 100	P/J/Z
TC514266AP/AJ/AZ	256KX4	CMOS	4/88	5/88	70 80 100	P/J/Z
TC514258P/J/Z	256KX4	CMOS	YES	YES	85 100 120	P/J/Z
TC514258AP/AJ/AZ	256KX4	CMOS	4/88	5/88	70 80 100	P/J/Z
TC514268AP/AT/AZ	256KX4	CMOS	4/88	5/88	70 80 100	P/J/Z
TC524256P/J/Z	256KX4	CMOS	YES	2Q'88	100 120	P/J/Z
TC524257P/J/Z	256KX4	CMOS	YES	2Q'88	100 120	P/J/Z
TC521000P	256KX4	CMOS	YES	YES	N/A	P
TC41000L	1MbX4	CMOS	6/88	7/88	70 80 100	L
THM81000S/L	1MbX8	CMOS	YES	YES	85 100 120	S/L
THM91000S/L	1MbX9	CMOS	YES	YES	85 100 120	S/L
THM91020L	1MbX9	CMOS	2/88	4/88	70 80 100	L
THM8512L	512KX8	CMOS	YES	YES	85 100 120	L

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Part Number	Org.	Process	Speed	Standby Power	Package
TC55257APL-85	32KX8	CMOS	85ns	100μAMAX	28PIN
TC55257APL-10	32KX8	CMOS	100ns	100μAMAX	28PIN
TC55257APL-12	32KX8	CMOS	120ns	100μAMAX	28PIN
TC55257APL-85	32KX8	CMOS	85ns	30μAMAX	28PIN
TC55257ALP-10L	32KX8	CMOS	100ns	30μAMAX	28PIN
TC55257APL-12L	32KX8	CMOS	120ns	30μAMAX	28PIN

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Circle 147 on reader service card

NEW PRODUCTS

SEEQ'S 512-KBIT FLASH EEPROMs SUPPORT IN-SYSTEM PROGRAMMING ON 12-V SUPPLY

One-transistor cells, 1.5-micron process, deliver high density and fast erasing

New host-interface features, 12-V programming, and a 1.5-μm CMOS process are being combined by Seeq Technology Inc. to launch a new line of flash electrically erasable programmable read-only memories. They offer easy in-system programming and high bit-packing densities. The single-transistor cell-based flash memories also erase 30 times faster than conventional EEPROMs.

The 32-pin, 512-Kbit 48F512 becomes the first CMOS flash memory tailored for in-circuit programming with 12-V power supplies. It is also now the densest EEPROM chip being sold in a 64-K-by-8-bit organization, claims the San Jose, Calif., company.

Designers added latches on address, data, and control input ports to keep the parts compatible with the erase and programming cycles of host microprocessors (see figure). Seeq also added extra control logic to implement a 512-byte block-erase mode, so the chip can selectively reprogram chunks of the array. Flash EEPROMs generally must be erased entirely during reprogramming because the one-transistor cell design typically trades off byte erasures for small size.

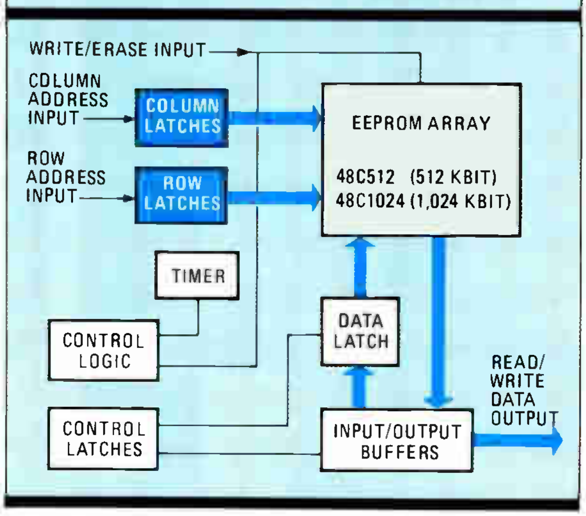
The lower, 12-V programming supply, for example, can also be applied to the part while it is read. Seeq managers say the reduction of voltage requirement will make the part more suitable for in-circuit programming applications.

ONE TRANSISTOR. On an architectural level, the 48F512 flash memories marry the advantages of one-transistor cells in ultraviolet EPROM and the erasure mechanism of conventional EEPROMs. Flash cells program like an EPROM, using hot-electron injection, but are erased like an EEPROM, using cold-electron tunneling.

The 48F512 flash memories use this one-transistor storage-cell design to achieve high bit-packing densities. The technology helps deliver the high densities and low costs that have eluded conventional EEPROMs, which usually have two-transistors per cell. Seeq's 48F512 is fabricated with a 1.5-μm process that reduces cell sizes to nearly 20 μm^2, compared with 35 μm^2 with the company's previous n-MOS flash memory, says Mike Villott, vice president of marketing.

Compared with ultraviolet-EPROMs, flash-memory programming-erasure times are fast. The part will entirely erase its array in one minute—20 to 30 times faster than EPROMs. The maximum time for writing to the chip is 1 ms per byte. The maximum block-erase time is 7.5 seconds. The 48F512 has a minimum erase-write endurance level of 100 times. Parts will be also be sold with 1,000-cycle endurance. Data retention is guaranteed for 10 years.

LATCHES EASE PROGRAMMING



Latches on address, data and control ports keep the EEPROM in step with programming cycles of host microprocessors.

Seeq uses a stacked polysilicon gate layout in a folded-cell configuration that merges the bit-select transistor of a conventional EEPROM with a floating gate. The split-gate layout is identical to the technology in Seeq's first flash memory, the 128-Kbit 48128, which is made of n-MOS and requires 21-V programming [*Electronics*, Aug. 21, 1986, p. 53].

In the summer, Seeq will offer samples of a pin-compatible 1-Mbit flash EEPROM, the 48F1024, based on the same cell design and CMOS process. "Customers will be able to design a socket for the 512-K or the 1-Mbit part," says Villott. Seeq's development of a family of compatible 256-Kbit-to-1-Mbit flash memories is part of a joint-development pact with National Semiconductor Corp.

The part dissipates 100 mA in standby mode and 60 μA active. Available now with 250-ns access times, the part costs $18.75 each in 100-piece quantities. *– J. Robert Lineback*

Seeq Technology Inc., 1849 Fortune Dr., San Jose, Calif. 95131.
Phone (408) 432-1550 [Circle 360]

IDT'S ECL-COMPATIBLE SRAM DELIVERS 50% POWER SAVING

An ECL-compatible, 64-Kbit biCMOS static random-access memory from Integrated Device Technology Inc. delivers a 50% power saving over the power-hungry emitter-coupled-logic devices that currently dominate the high-speed memory market. What's more, its 15-ns access times rival the ECL competition.

Organized as 64-K-by-1 bit and compatible with ECL 100-K logic, the IDT100490 dissipates 320 mW typical. It gets its speed/power performance from the Santa Clara, Calif., company's proprietary BiCEMOS process, says Larry Jordan, vice president of marketing. The 22-pin device features separate data input and outputs; static operation without clocks or refresh; and open-emitter outputs.

The BiCEMOS process is built on the company's 1.5-μm CEMOS 3B technology, but incorporates bipolar transistors that operate at cutoff frequencies above 6 GHz. This combination provides better

CLEAR DIGITIZING PAD CUTS COMPETITION'S PRICE IN HALF

Ovonic Imaging Systems' E-Z Image Pad uses proprietary resistive film to make entering handwriting or tracing drawings and photographs easy

A thin film of proprietary resistive material deposited on a transparent glass substrate is the key technology in Ovonic Imaging Systems Inc.'s digitizing pad for direct entry of handwritten information into a computer. And at $110, the versatile pad costs about half the price of competing systems.

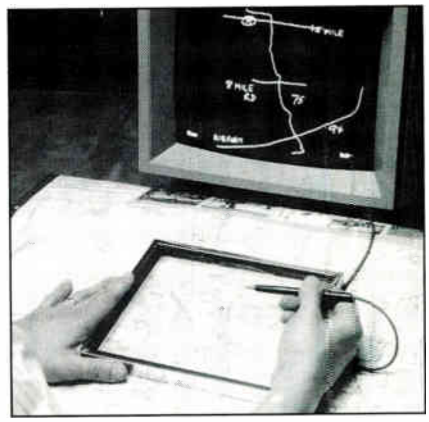
When the user writes or draws with a conductive stylus on the Troy, Mich., company's E-Z Image pad, an image of the inscription appears on a computer display in bit-mapped form. Simple circuitry around the edges of the pad senses the location of the stylus.

The pad is compatible with IBM Corp.'s Personal Computer family. Since it is transparent, E-Z Image can be used as an overlay for tracing drawings, maps, and photographs. It can be placed over a light box, CRT screen, or flat-panel display. Another use is as a direct-entry notepad in applications such as filling out forms electronically, or in signature-verification systems for security purposes, banking, and credit-card transactions.

The system offers a versatile, simple-to-use approach to computer entry that requires no special training, says Lionel Robbins, Ovonic Imaging's vice president for sales and marketing. "This is more user-friendly than, say, a mouse device," he says.

The $110 price tag, for 1,000-unit quantities, compares with approximately $250 for competitive products, Robbins says. "The real basis for this technology is our ability to deposit and work with thin films on large glass substrates, resulting in the low cost," he explains.

The E-Z Image pad with a 7-by-8½-in. active area is available now complete with stylus and interface card.



E-Z Image is compatible with IBM's Personal Computer family.

Ovonic Imaging also offers the pad, interface, and stylus separately, priced at $60, $40, and $10 respectively, in 1,000-unit quantities. The company will customize pads for size and interface cards or RS-232C ports based on customer demand. – *Wesley R. Iversen*

Ovonic Imaging Systems Inc., 1896 Barrett St., Troy, Mich. 48084.
Phone (313) 362-2738 [Circle 340]

KIT IMPLEMENTS MICRO CHANNEL INTERFACE

Manufacturers of expansion memory boards for the IBM Corp. Personal System/2 models 50 and 60 can cut both the time and engineering costs required to implement a design—and do it using up to 30 fewer chips—with a two-chip set and design package from Edsun Laboratories Inc.

The EL2010 is one of the first VLSI chip sets implementing the PS/2 Micro Channel interface and memory-control functions, claims the Waltham, Mass., company. It provides a complete Micro Channel interface, expansion memory controller—indeed, "everything needed to manufacture and introduce PS/2 add-on memory boards," says Richard Simon, director of marketing.

QUICK UPGRADE. Its use offers suppliers of expansion boards a way to upgrade their products quickly, says Simon. He estimates it can also save newcomers to the PS/2 add-on business six to 12 months in design time and $50,000 or more in engineering resources.

The kit includes a sample board, printed-circuit-board artwork, drill tape, schematics, manufacturing diagnostics, a user manual, and software drivers for the Lotus-Intel-Microsoft Expanded Memory Specification 4.0 and OS/2 extended memory.

The chip set/design package combination is intended to meet a PS/2 memory-board market that will grow when the OS/2 extended-edition operating system arrives later this year, says Simon. OS/2 requires a minimum of 1.5 Mbytes for the operating system alone and the extended edition will consume 3 Mbytes. But the 80286-based PS/2 models 50 and 60 are shipped with just 1 Mbyte of system memory.

The chip set embodies a full set of power-on-setup registers, selectable board ID codes, parity and channel-check logic, translation random-access memory control, and decoding for one parallel and two serial ports. It supports up to 14.25 Mbytes of memory in up to eight banks, includes an optional on-board relocatable BIOS read-only memory, and will accommodate 256-Kbit or 1-Mbit dynamic RAM chips. The EL2010 devices will run in systems operating at up to 16 MHz.

The chips come in a standard 84-pin plastic leaded chip carrier. They can be surface-mounted or socketed.

Two versions of the DesignWare package—for 2- and 8-Mbyte expansion boards—are available. The kit's board uses three IBM-authorized ID numbers, which prevent the problems some early PS/2 add-on-board suppliers encountered without them. Those problems ranged from an inability of the operating system to recognize all of the expansion memory available, to total failure of the memory board.

The DesignWare package is priced at $2,500. The chip set sells for $35 in quantities of 1,000. Samples will be available at the end of March, and Simon projects that production quantities will be available "in time to meet manufacturers' needs." – *Lawrence Curran*

Edsun Laboratories Inc., 9 Spring St., Waltham, Mass. 02154.
Phone (617) 647-9300 [Circle 342]

$8,000 VMEBUS BOARD DELIVERS 16 MILLION COLORS

A series of single-board bit-map display controllers from Univision Technologies Inc. delivers true color performance for VME-based Sun Microsystems work stations. Yet at $8,000, the controllers cost about a quarter of the price of the high-end systems that offer true color, but also incorporate much higher vector performance than many users need, says the Burlington, Mass., company.

The UDC-3400 series supports 60-Hz noninterlaced monitors and can handle

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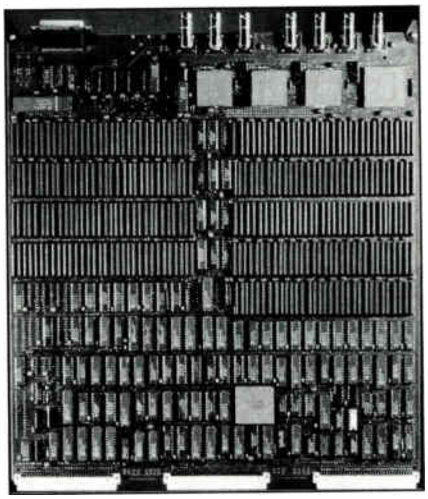
16.8 million colors with 34-bit/pixel graphics resolution. Eight bits each are used for red, green, and blue signals, eight for indexing/tagging, and two for overlay. The controllers target applications such as computer-aided design and image analysis. The series has not been fully benchmarked, but Warren Mootrey, director of sales and marketing, says that 20-pixel horizontal-vector line drawings are done at a rate of 50,000/s.

One version of the series, selling for $7,995, offers 1,280-by-1,024-pixel resolution with 24-bit depth and two bits of overlay. Another version of the controller boasts resolution of 34 bits/pixel and costs $8,995.

Mootrey says he knows of no other



The UDC-3400 series offers 16 million colors with 34-bits/pixel graphics resolution.

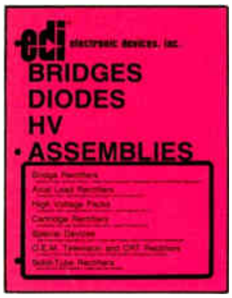
single-board display controller for Sun systems in this price/performance range. The UDC-3400 series has been positioned to fill a market need below that met by the high-end solutions: three- or four-board sets that plug into Sun systems for 3-d real-time applications and cost as much as $34,000.

The UDC-3400 series gets its performance by combining a 20-MHz Intel Corp. 82786 display controller with up to 9 Mbytes of dual-ported video memory. That combination allows high-speed operations, such as polygon and line drawing, bit-block transfers, and multifont text generation.

The dual-ported memory also gives fast access to the host bus, while an optional external VSB-standard bus interface provides access to very-high-speed processing by means of an outboard array processor or coprocessor at a transfer rate of 10 Mbytes/s. A 512-Kbyte display-list memory allows users to store primitives, such as circle arcs, commands, and text.

The series is available now.

Univision Technologies Inc., 12 Cambridge St., Burlington, Mass. 01803.
Phone (617) 273-5388 [Circle 341]



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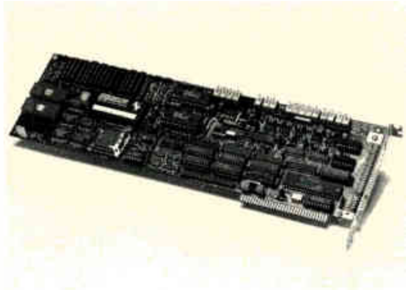

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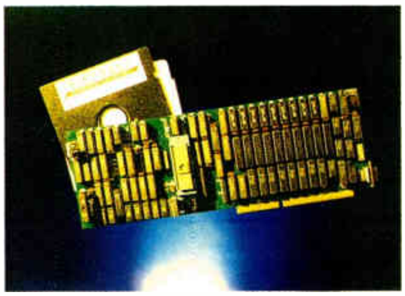

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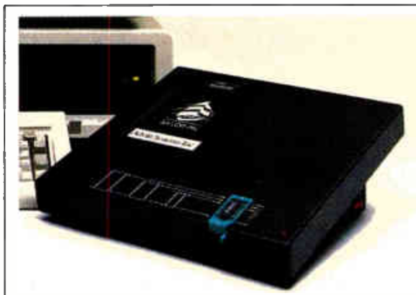

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ELECTRONICS WEEK

DAVIDOW TAKES CHARGE AT ACTEL

William Davidow, a former Intel Corp. executive turned venture capitalist, is stepping back into management in the chip business as chairman of Actel Inc., a Sunnyvale, Calif., startup. Davidow, a general partner in Davidow Ventures, of Menlo Park, Calif., succeeds founder Amr Mohsen, who will stay on as president and chief executive officer. Two-year-old Actel is developing a user-configurable CMOS gate array technology to compete in the application-specific chip market [*Electronics*, Feb. 18, 1988, p. 75].

TEKTRONIX CUTS 1,000 JOBS . . .

Less than five months after starting an ambitious reorganization, Tektronix Inc. is streamlining its operations—and cutting 1,000 jobs between now and May 28, when its fiscal year ends. The Beaverton, Ore., maker of instruments, work stations, and displays, struggled through four years of flat growth before David Friedley took over as president and chief executive officer and shook things up last fall [*Electronics*, Feb. 4, 1988, p. 45]. "Most of the reductions affect managerial and professional jobs," Friedley says. Friedley is hoping that cutting the work force by 6% to about 16,000 employees will help Tektronix return to high growth and profitability.

. . . BUT 88000-BASED RISC SYSTEM IS CLOSE

While Tektronix Inc.'s management struggles over cutting back its staff, the company's engineers are pushing ahead with a planned high-performance work-station product, based on Motorola Inc.'s 88000 chip, a new 32-bit reduced-instruction-set-computer processor [*Electronics*, Feb. 18, 1988, p. 83]. The 88000-based RISC work station will be one of several key projects Tektronix will emphasize this spring after its streamlining job is complete, says president David Friedley. "We have a number of growing, profitable businesses which are performing well, including portable oscilloscopes, television-related units, and the graphics printer and terminal divisions," he says. "We are also aggressively pursuing other growth opportunities, such as telecommunications equipment, work stations, and measurement systems."

COMING SOON: FIBER-OPTIC NET FOR CARS

Codenoll Technology Corp. and Hoechst AG are joining in a 10-year deal to make polymer optic-fiber components and networks, primarily for the automotive market. Codenoll, of Yonkers, N. Y., and Hoechst, the West German chemical giant, will unveil a prototype system in April at the Hanover Fair. They say that the first system will be the first fiber-optic network to completely control an automobile.

EMCORE BREAKS INTO JAPANESE MARKET

Emcore Corp., a Somerset, N. J., maker of specialized gallium arsenide chip-making equipment, has scored its first overseas sale. The three-year-old company broke into the Japanese market by selling a metal-organic chemical-vapor-deposition system to Mitsui Toatsu Chemicals Inc. The system, a research model, is designed for use with 2-in. gallium-arsenide wafers, and costs more than $300,000.

MULTIPROCESSOR VAX FINALLY DEBUTS . . .

Digital Equipment Corp.'s long awaited high-end VAX, the 8800 series, finally hit the street in March. The primary foundation for the new family, which will compete with IBM Corp.'s low-end mainframes, is VMS SMP, a symmetrical multiprocessing version of DEC's VMS operating system. Five models, offering from one to four processors and up to 512 Mbytes of main memory, are available immediately for prices ranging from about $544,000 to $1.6 million.

. . . AS DEC JOINS SIEMENS IN TELECOM

Digital Equipment Corp. intends to bolster its excursion into the U. S. telecommunications markets by working with Siemens AG, the world's third largest producer of telecommunications equipment. The Maynard, Mass., computer maker and Siemens Communications Systems Inc., a U. S. subsidiary of the Munich firm, have signed a nonexclusive pact to develop a wide range of products for openings—resulting from deregulation—that they spot in the market.

EXPORT GROWTH OUTPACES IMPORTS

Exports of U. S. electronics grew 20% last year, outpacing the growth of imports for the first time since 1980, the Electronics Industries Association reports. Exports leaped almost 20% in 1987 to $40 billion, up from $33.4 billion in 1986. Electronics imports, meanwhile, reached $57.9 billion, up 15% over the 1986 figure of $50.3 billion. The EIA attributes the turnaround in export growth mainly to a lower dollar, but also credits higher quality and aggressive marketing.

APPLE ACQUIRES NETWORKING FIRM

Apple Computer Inc. acquired a small networking firm in its home town of Cupertino, Calif., as part of its principal 1988 technology objective: expanded networking and communications systems. Apple paid an undisclosed sum for four-year-old Network Innovations Corp., which sells systems for easy data communications between Macintosh desktop computers and minicomputers from Digital Equipment Corp. The duo intends to promote CL/1, Innovation's universal language for transparent desktop-computer/mainframe links, as an industry standard across all major computing environments. The first CL/1 connection ties Apple Macintosh desktops to Digital Equipment Corp.'s VAX mainframes. Links for IBM hosts will follow.

GOULD MOVES FORMER AMI UNIT TO IDAHO

Gould Inc. is consolidating the last remnants of what was once American Microsystems Inc. of Santa Clara, Calif., into its growing Pocatello, Idaho, semiconductor plant. About 100 marketing and adminstrative employees of what's now called the Gould Semiconductor Division are being asked to move to Idaho within 90 days. Gould, which purchased AMI in the early 1980s, has been shifting the bulk of its chip-making activities to Idaho for the past three years. About 850 employees are at the Pocatello site today.

IBM SETS NEW MARK IN SUPERCONDUCTORS

Researchers at IBM Corp.'s Almaden Research Center in San Jose, Calif., have upped the ante in high-temperature superconductivity to 125 K using a ceramic oxide of thallium, barium, calcium, and copper. Earlier, scientists at the University of Arkansas in Fayetteville had reported superconductivity—the loss of all electrical resistance—at 106 K for a different material containing the same elements. The two back-to-back U. S. announcements came two months after the first 1988 record was claimed in Japan. IBM is filing a patent on its newest bulk superconductive material.

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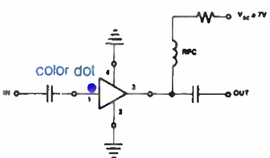

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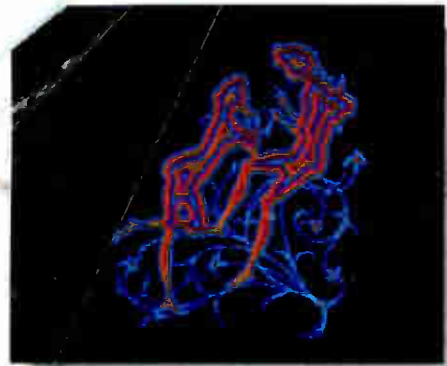

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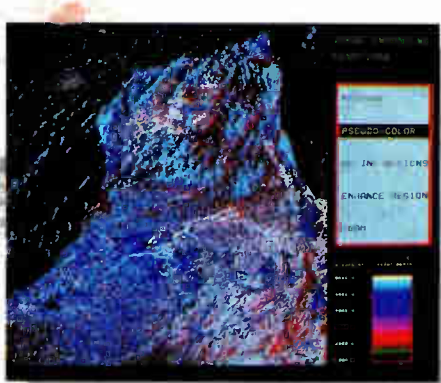

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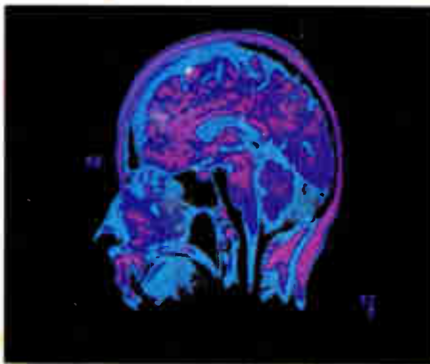

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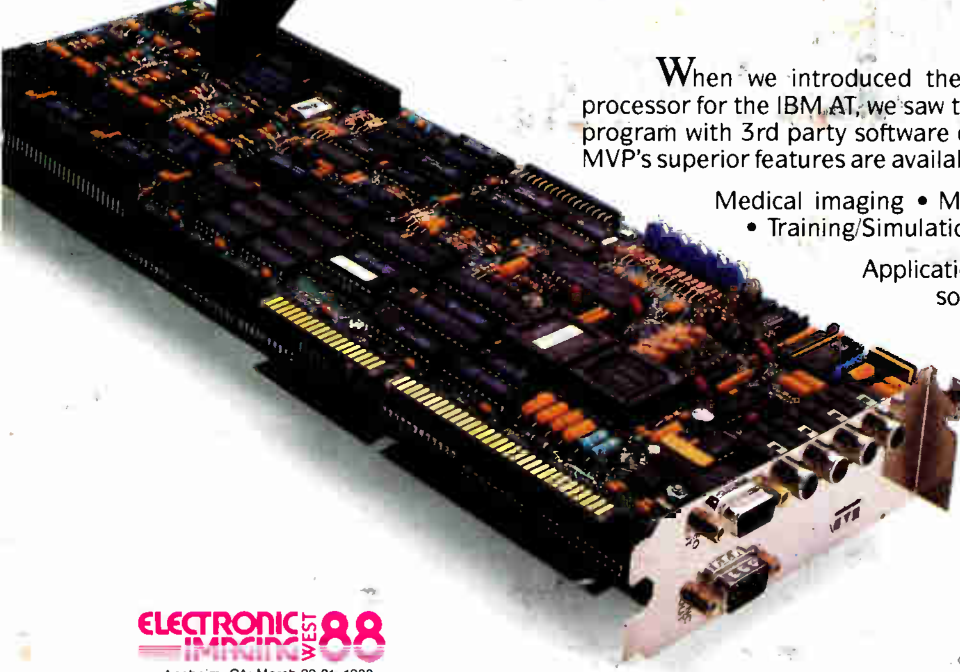

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