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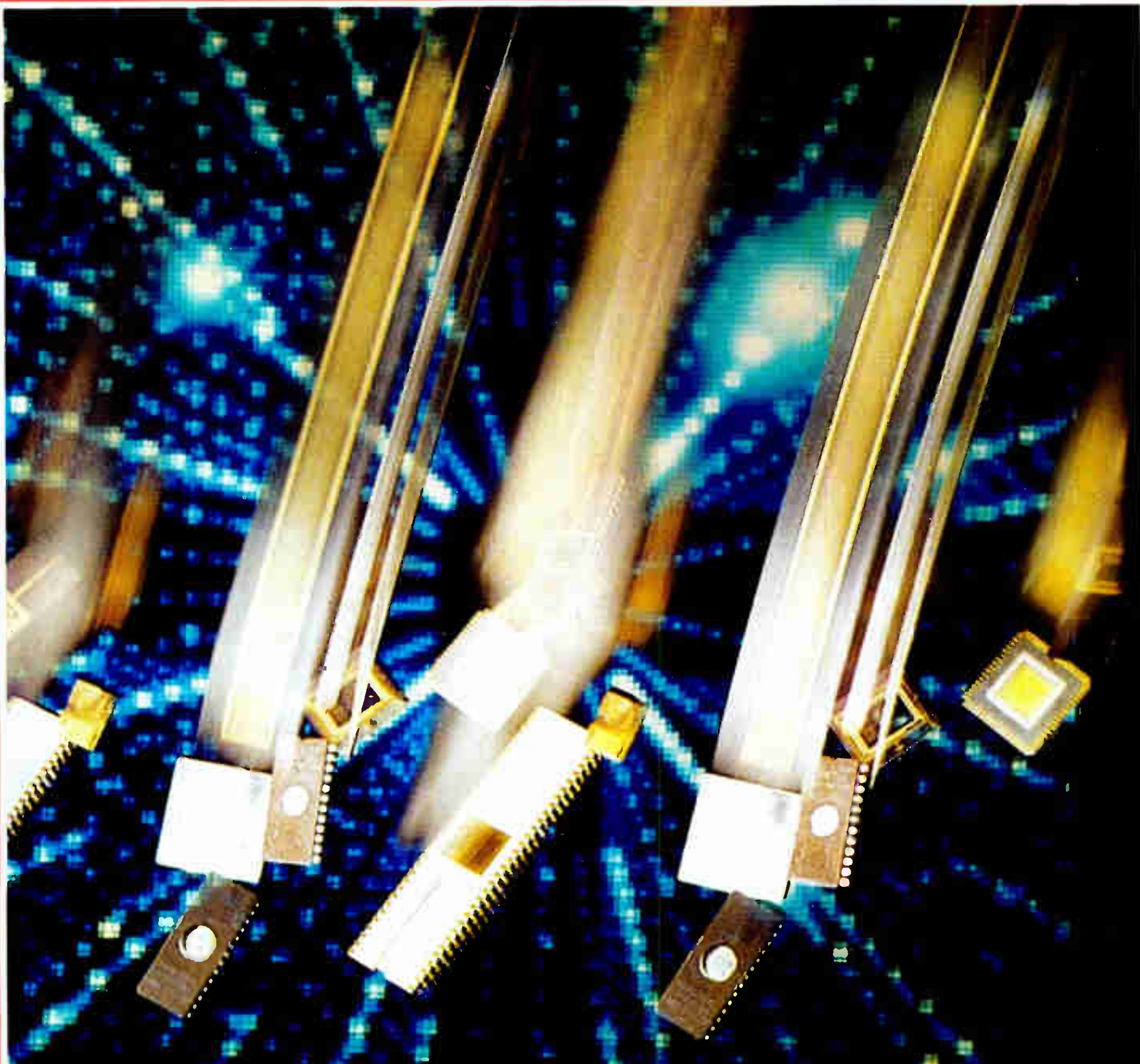

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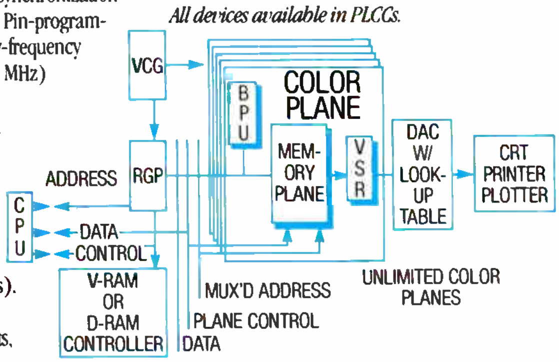

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Electronics

Anyone who has been in the news business for any period of time knows that the story doesn't end just because it has seen print. There always are continuing new developments to be reported, new angles to be covered.

No one knows that better than *Electronics*. For example, last year we published two special issues on the semiconductor industry—two issues that, by the way, have won two major editorial excellence awards. The first, "The Chip Makers: Where They're Heading," appeared on April 2. Then, four months later, on Aug. 6, we dug into "The ASIC Takeover." But we're not about to stop there. There have, of course, been further developments, and in this issue, *Electronics* mounts a three-pronged investigation that may be considered an extension of those two special reports from last year.

The first, starting on p. 67, is a special nine-part series on the International Solid State Circuits Conference, going on this week in San Francisco. With semiconductors editor Bernie Cole spearheading the operation from his base in San Mateo, and executive editor Sam Weber running the show in New York, the package parallels the ISSCC's technology tracks. Moreover, it once again shows how *Electronics* is able to deploy its team of seasoned editors to blanket a breaking story.

Included are contributions from Cole, Larry Waller in Los Angeles, and Tobias Naegele and Stan Runyon in New York. The articles run the semiconductor gamut, from memories to converters, logic to processors. As a matter of fact, Bernie describes the 1988 edition of the ISSCC as "a show that will be remembered as one that spotlighted a raft of watershed developments." For example, he says, "There are the new 16-Mbit random-access memories—that's more memory space than some hard disks, more memory space than two floppy drives on an IBM PC.

"Equally exciting are the 1-Mbit static RAMs with 15-to-40-ns speeds. They're as large as the dynamic RAMs coming into production and five to six times faster. That means they can be used instead of the slow DRAM and cache static, and the designer winds up with both high speed and more density." In addition, notes Bernie, there are the algorithm-specific processors that do in hardware what now has to be done in software, thereby saving memory space.

Technology doesn't exist in a vacuum, so even as we describe in great detail the excitement generated by all these advances in chip technology, we are not neglecting the business side of the industry. So the second major part of the semiconductor coverage in this issue—and of our pledge to provide complete and continuing examination of both sides of the equation—is Rob Lineback's Inside Technology on p. 81 dissecting the rarely explored question of profitability. Rob points out that a big question looms over the industry today: is the current disappointingly low return on equity a serious harbinger of bad times on the horizon—or is simply a hangover from the bad times that the chip makers went through in the early part of the decade? This is the takeoff point for his article.

Rounding things out is the exclusive Inside Technology article on p. 83 describing Motorola's hot new reduced-instruction-set-computer chip. Earlier this month, Stan Runyon flew from New York to Texas to join Dallas bureau manager Lineback for a first look at the long-awaited chip. Runyon was impressed. He says, "Motorola's chip could do for the world of RISC what its 68000 family did for the world of CISC."

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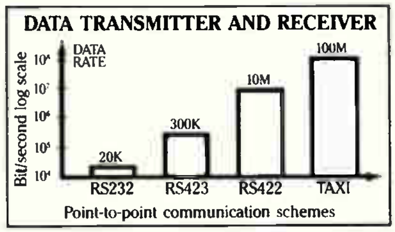

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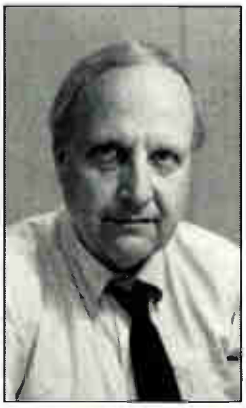
'THREAT OF THE WEEK': COMPUTER VIRUSES

How the "Times" riles us with its doomsday scenario of virulent outbreaks of viruses that can put worldwide computer networks out of commission



I couldn't believe my eyes. In the Sunday *New York Times*, bold headlines proclaimed: "Virus programs that can elude most barriers have begun to infect computers around the world." In what a long, rambling article described as a "science-fiction nightmare come to life," viruses that "subvert, alter, or destroy programs" were reported to have infected personal computers at several places. These viruses were said to be highly contagious, capable of instantaneously cloning copies of themselves and burying them inside other programs. These programs then become contagious and the viruses pass to other computers that come in contact with the infected software. Thus a PC-based electronic bulletin board could rapidly infect thousands of small computers.

As far as I was concerned, the *Times* story itself was a piece of science fiction. At best, it didn't muster nearly enough evidence to back up its scare headlines. Even so, we checked it out. After talking to the experts, we found most believed the *Times* story was "alarmist," but they also agreed such viruses were indeed possible.

A Washington-based expert for one leading consultant who knows about such things says these viruses are "extremely rare." No system he or his people had ever worked on that had a reasonable level of security has ever been attacked by a virus, he maintains. But he did point out that many systems are set up with insufficient security, and that some of the possible forms of attack on these computers are "scary." The main way to avoid such problems, he notes, is to carefully restrict access to a system.

Once such press reports appear, you can look for one of two possible scenarios, says SRI International's Donn Parker, a leading expert on computer crime. "The whole thing can just blow over, just as it did after the publicizing of other computer threats such as rf emanations, hackers, and phone freaks," he says. "Viruses will be just another computer system vulnerability to be wary of." But his worst-case scenario is worrisome: virus attacks will increase dramatically and end up destroying all public domain software, causing what Donn calls the "Tylenol Syndrome." Software will be suspected of contamination and will be avoided, possibly causing the demise of some software companies. While Donn leans strongly toward his first scenario, we are sufficiently motivated to dig into this. Stay tuned. **ROBERT W. HENKEL**

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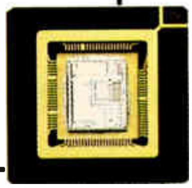

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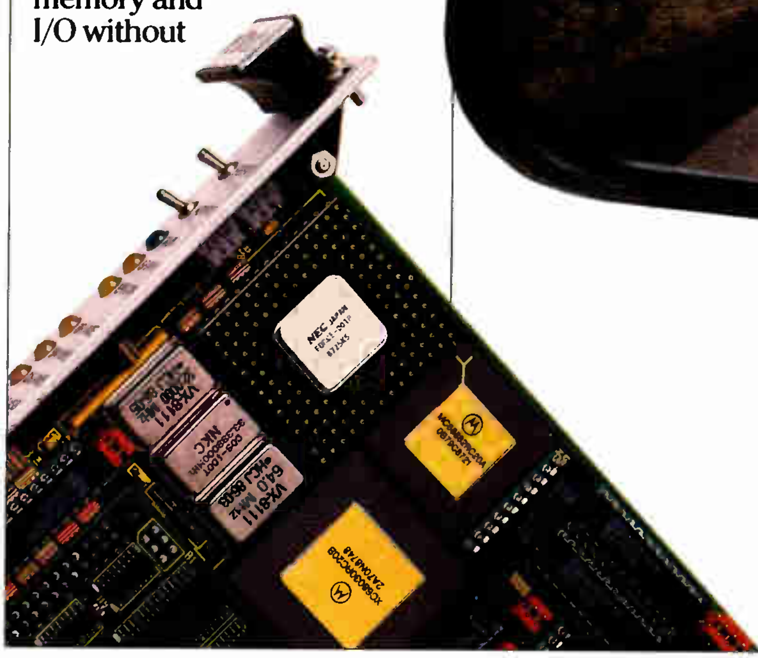

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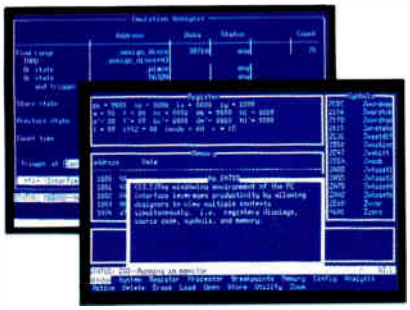

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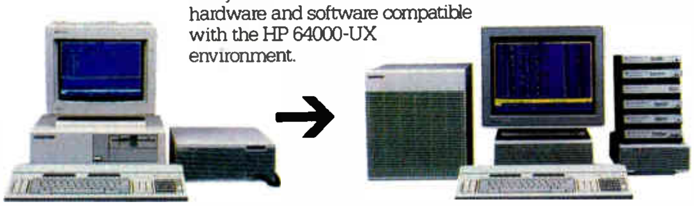

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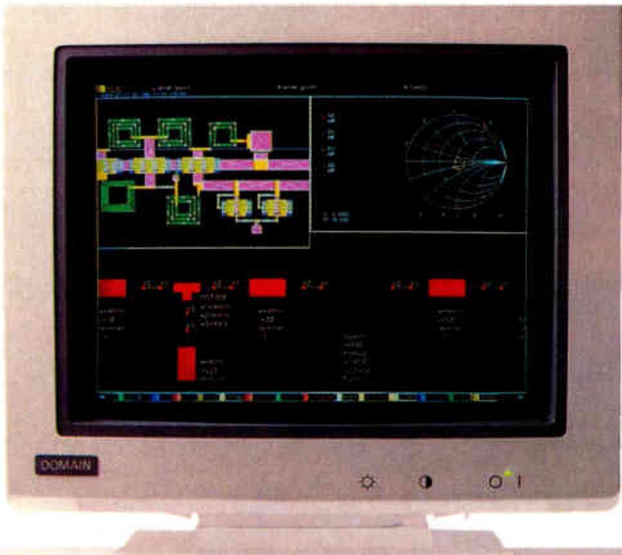

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ELECTRONICS NEWSLETTER

INTEL GETS ON THE SCOREBOARD WITH 10-MIPS CONTROLLER...

Look for plenty of action from Intel Corp. in the embedded processor/controller market in the months ahead. The Santa Clara, Calif., company tipped its hand in a late paper on "scoreboarding" at this week's International Solid State Circuits Conference in San Francisco. In the proprietary technique, registers keep track of outstanding read accesses as the processor continues to execute other instructions. This overlapping scheme, Intel designers say, significantly improves performance and reduces the effects of slower external memory. The scheme will be one of the reduced-instruction-set features incorporated in a new 32-bit controller family, which will push performance to between 2 and 10 million instructions/s. Intel also has in mind a slimmed-down version of its 80386, a follow-on to its 80186 embedded processor [*Electronics,* Oct. 29, 1987, p. 22]. □

...AND FLASHES NEW EEPROM AT ISSCC

In still another late ISSCC paper, Intel Corp. signalled its entry in the market for flash electrically erasable programmable read-only memories, which until now has been the sole preserve of Seeq Technology Inc., San Jose, Calif. Intel will enter the market with a 256-Kbit double-polysilicon CMOS part that is based on a single-transistor cell. Fabricated with a 1.5-μm CMOS process, the 150-mW Intel device features a 110-ns access time, a 200-ms erase time, and a 100-μs-per-byte programming time. Seeq and Intel won't have the market all to themselves for long, however. A number of other companies have announced that they intend to enter the fray—among them, Exel Microelectronics, Hitachi Ltd., National Semiconductor Corp., and Toshiba Corp. □

AT&T WILL START BRIEFING CUSTOMERS ON VERSION 4.0 OF UNIX V THIS SUMMER

A new version of AT&T Co.'s Unix System V is in the offing for late 1989 and yet another version is taking shape. At last week's Uniforum show in Dallas, AT&T announced it would start briefing computer companies and software developers about Unix System V Version 4.0 this summer. The company also used the show to give licensees a peek at what's in store: Sun Microsystems Inc.'s Remote Procedure Call and Network File System software will be added, along with some features of Microsoft Corp.'s Xenix System V and others that are derived from Berkeley Unix. Meanwhile, Bill Joy, Sun's vice president of research and development, is setting up a group to rewrite the Unix kernel in C++, an object-oriented extension to the C programming language. This kernel will be used in Version 5 of Unix System V, and Joy says it should make the operating system easier for licensees to enhance. □

HONEYWELL-NEC CONTEMPLATES A SUPERCOMPUTER WITH TWICE THE CRAY Y-MP'S SPEED

Cray Research Inc. barely had time to bask in the glow of the Y-MP introduction (see story, p. 31) when rumors surfaced that Honeywell-NEC Supercomputers Inc. (HNSX) is working on a four-processor supercomputer that will double the Y-MP's 6-ns clock speed. At the moment, the HNSX machine is just a cloud on the horizon—a senior HNSX official says the company doesn't have a multiprocessor machine at the moment. "We've been visited in Tokyo by people from some significant laboratories who have been exposed to ideas and concepts, not a machine. No announcement is imminent, but we're in the market to stay if NEC's history of getting into any market is a precedent." A source at NEC admits that the Tokyo company is doing research on a multiprocessor supercomputer but still extolls the virtues of the fastest possible single processor with a large number of parallel pipelines. □

PRODUCTS NEWSLETTER

HITACHI LIKELY TO BE FIRST TO MARKET WITH 1-MBIT STATIC RAM

Looks like Hitachi Ltd. will be the first to market a 1-Mbit static random-access memory. Although Hitachi's chip seems likely to be outperformed by a slew of 1-Mbit introductions later this year (see story p. 69), its 70-ns access time is fast enough to replace dynamic RAMs in high-end computer systems. Configured as 128 K by 8 bits, the HM628128 will be available in sample form in April with 70-, 85-, 100-, and 120-ns access times. The part is built using 0.8-μm design rules—compared with 1.3 μm rules for the Tokyo-based company's 256-Kbit SRAMs—and a triple-layer-polysilicon process. The 7-by-14.4-mm chip operates at 70 mA, has a standby current of 2 mA, and is TTL-compatible. Devices come in 32-pin dual in-line and small-outline packages. Prices in Japan range from 52,000 yen for the 70-ns DIP to 70,000 yen for the fastest SO units. Export pricing has not been set. □

ANALOG DEVICES TEAMS WITH BROOKTREE TO ENTER GRAPHICS-DISPLAY CHIP MARKET

Analog Devices Inc. will team up with Brooktree Corp. to enter the exploding graphics display market; the duo hopes to establish a video standard. The two companies will independently develop, manufacture, and market RGB (red, green, blue) video digital-to-analog converters for generating analog signals for color displays, says James Bixby, president and chief executive officer of Brooktree in San Diego. Under phase one of the agreement, Analog Devices, Norwood, Mass., will second-source Brooktree's Bt471 and Bt478 RAMDACs, which are, respectively, a triple 6-bit and a triple 8-bit DAC with onboard RAM, aimed at the PS/2 personal computer market. Later, Analog Devices will adapt Brooktree architecture and pinouts to develop its own proprietary products. □

ELXSI'S "SUPERFRAME" BLAZES IN REAL-TIME PROCESSING

Control lines hardwired directly into the central processing unit of Elxsi Corp.'s upcoming 6460 processor will enable the new vector-scalar system to stop on a dime and service external interrupts in less than 10 μs. That beats by 10 times the speed of competing machines, says Peter Appleton Jones, Elxsi's president. Jones, in fact, is touting the 6460 as a new class of hardware—the "Superframe"—that merges the best of supercomputers and mainframe power. The San Jose, Calif., company plans to patent the architecture, which has eight interrupt lines wired into the CPU as opposed to more conventional message systems using firmware and software. Up to ten 6460 vector-scalar units can be loaded into an Elxsi chassis. A fully loaded system will run at 250 million instructions/s or 100 million floating-point operations/s and cost just under $4 million. □

NEC'S IMAGE-COMPRESSION CHIP IS TWICE AS FAST AS THE COMPETITION

NEC Corp.'s image compression/expansion chip for black-and-white applications such as facsimile machines and image work stations doubles the best performance of the competition—and delivers the kind of power needed for storing and retrieving images from optical or hard disks. The μPD72185 gets its speed by using pipeline processing in a four-stage dedicated circuit and a high-speed on-chip CPU. The chip compresses or expands a standard, letter-size CCITT test chart in less than 0.75 s. Facsimile machines using it can talk to almost any other fax because the μPD72185 handles the three most popular compression/expansion algorithms. Image size can also be doubled or halved. The 180,000-transistor device is fabricated in 1.5 μm CMOS technology on a 9.5-by-9.9-mm. chip. Sample shipments will begin in April at a price of 20,000 yen. Production will begin in June. □

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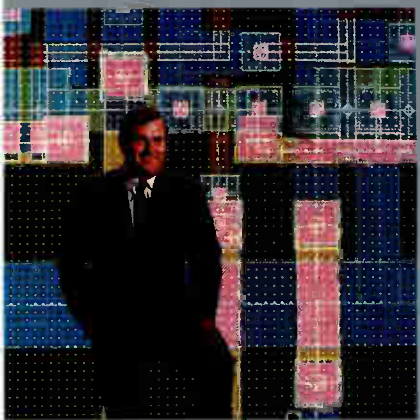

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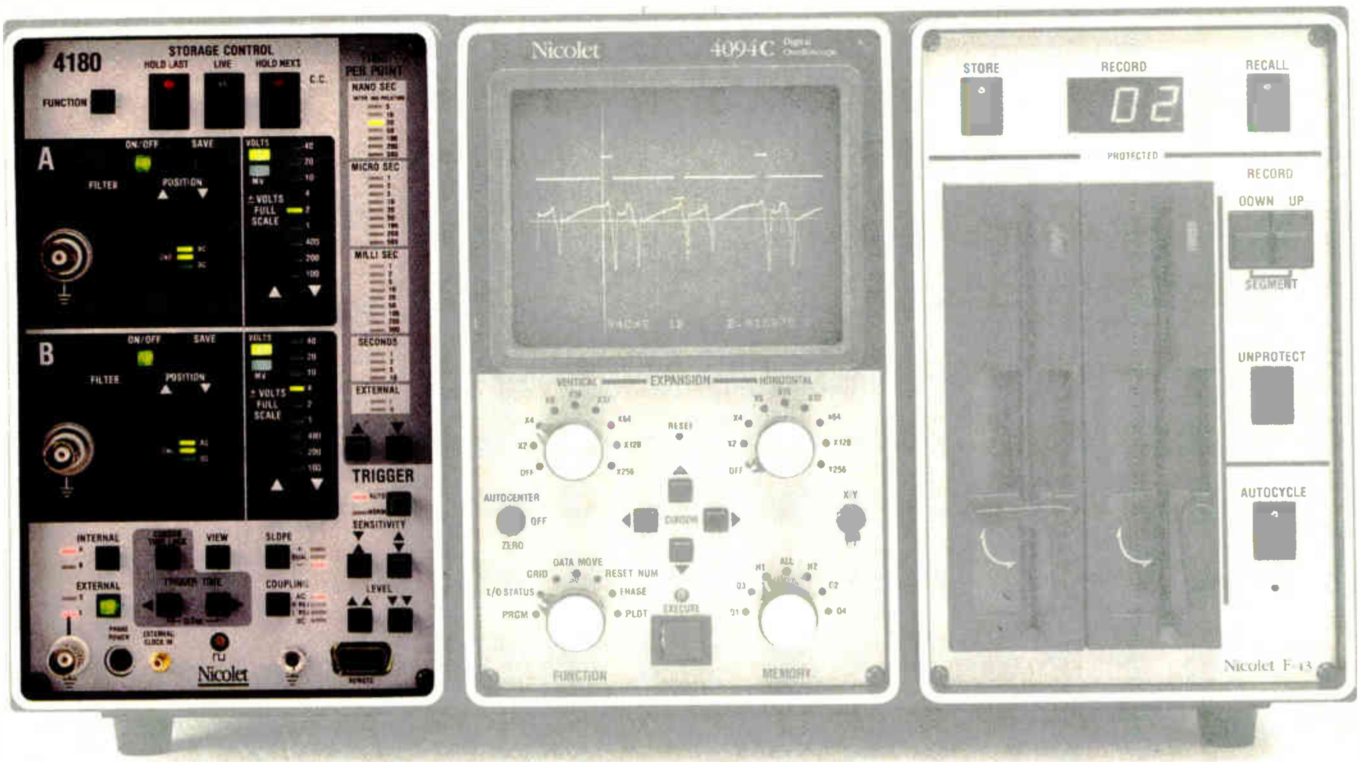

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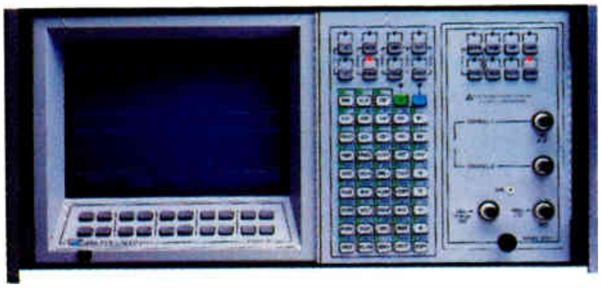

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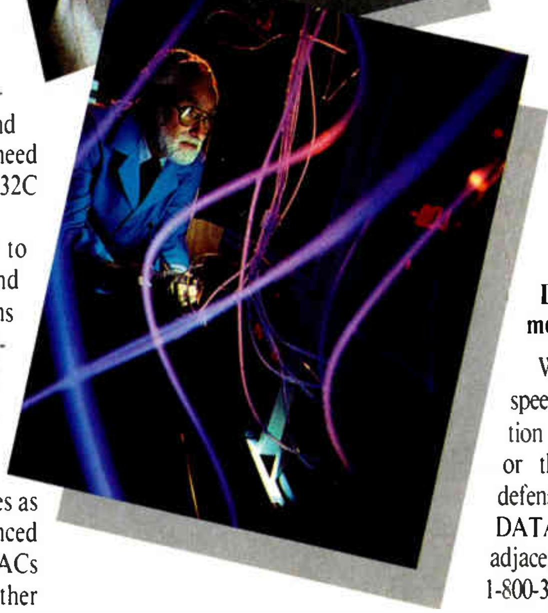

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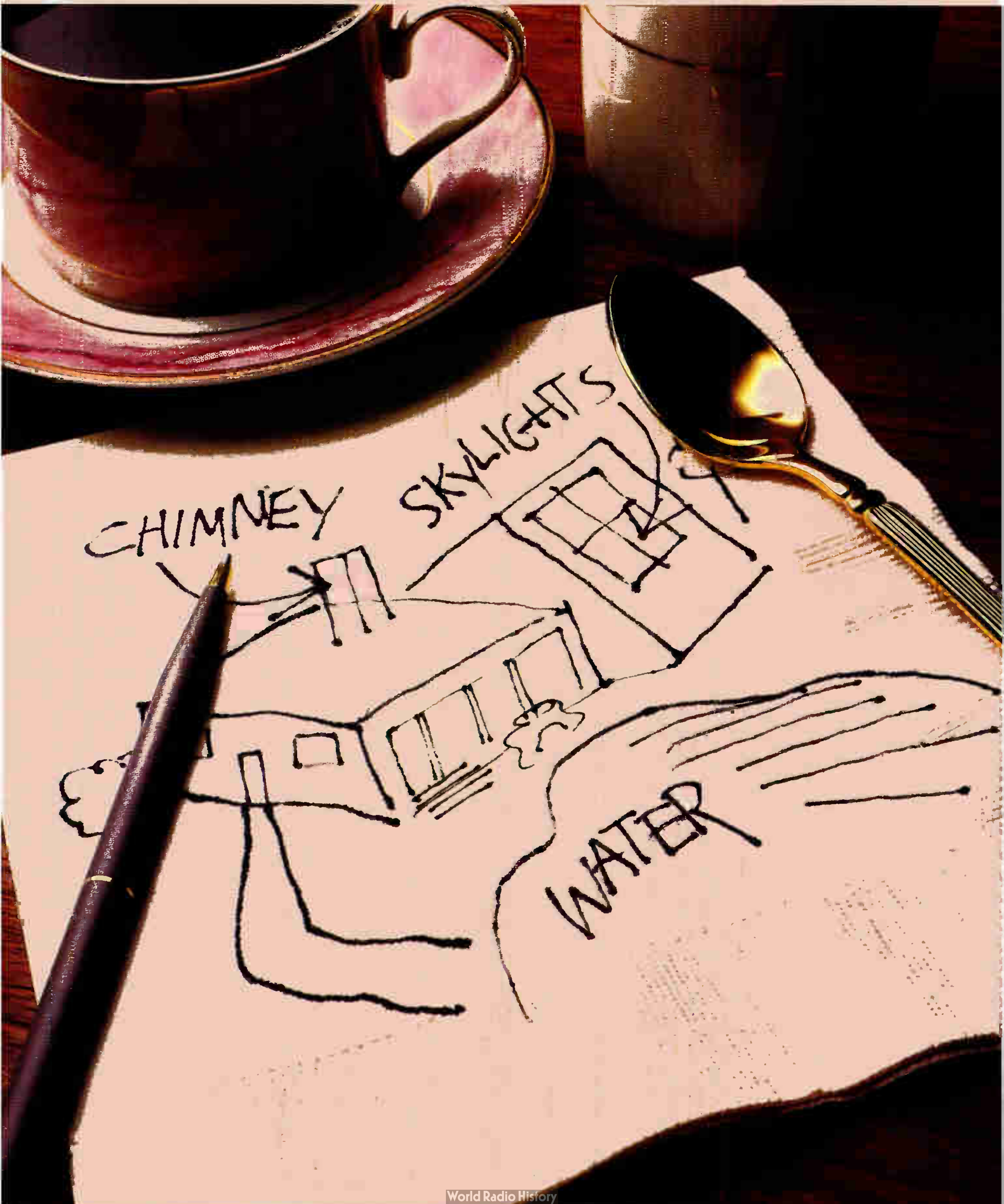

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D. Test and measurement equipment
E. Consumer products (TV, radio, hi-fi, recorders, home computers, appliances)
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R. Industrial control systems and equipment
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I. Other manufacturers using electronic equipment as part of their manufacturing process (machine tools, chemicals, metals, plastics, pharmaceuticals, etc.)
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K. Independent research and development laboratories or consultants
L. Research and development organizations which are part of an educational institution
M. Independent software developers
N. Operators of communications equipment (utilities, railroads, police, airlines, broadcasters, etc.)
O. Educational: 2-4 year colleges, universities
P. Other (please describe) ______

2. ☐ **Your principal job function: (Insert one code only)**

A. Corporate management (owner, partner, president, VP, etc.)
B. Operating management (general manager, group manager, division head, etc.)
C. Engineering management (project manager, chief engineer, section head, VP of engineering, VP of research and development, VP of quality control, etc.)
D. Software engineering
E. Systems engineering/integration
F. Quality control engineering (reliability and standards)
G. Design engineering
H. Engineering support (lab assistant, etc.)
I. Test engineering (materials, test, evaluation)
J. Field service engineering
K. Research and development (scientist, chemist, physicist, etc.)
L. Manufacturing and production
M. Purchasing and procurement
N. Marketing and sales
O. Professor/instructor at ______
P. Senior student at ______
Q. Graduate student at ______
Z. Other (please describe) ______

3. ☐ **Your principal responsibility: (Insert one code only)**

1. General management
2. Engineering management
3. Engineering
4. Other ______

4. Estimated number of employees at your location: (Check one box only)

☐ 1 to 49 ☐ 50 to 249 ☐ 250 to 999 ☐ 1,000 or more

5. Your engineering function: (Check all that apply)

A. ☐ I design or develop electronic products and systems (hardware and/or software)
B. ☐ I supervise electronic design or development engineering work
C. ☐ I set standards for, evaluate, test and/or support the manufacture of design components, systems and materials
D. ☐ Other function (please describe) ______

6. In your company or organization, do you participate in: (Check all that apply)

A. ☐ Business planning and forecasting
B. ☐ Product planning
C. ☐ Technology planning
D. ☐ No involvement in planning

7. Your involvement in the following stages of product development: (Check all that apply)

A. ☐ Evaluate the need for new products
B. ☐ Develop device specifications
C. ☐ Evaluate suppliers
D. ☐ Review prices and availability
E. ☐ Select Vendors
F. ☐ Approve purchases
G. ☐ Place orders
H. ☐ No involvement

8. ☐ **What is your title? (Insert one code only)**

Operations Management

01. President/Chairman/Owner/Partner
02. Vice President
03. Vice President of Engineering
04. Product Marketing Manager

Engineering Management

11. Technical Director
12. Chief Engineer
13. Principal Engineer
14. Research Director
15. Section Head
16. Project Engineer
17. Senior Engineer
18. Software Manager
19. Senior Test Engineer
20. Senior Field Test Engineer
21. Manufacturing/Production Manager
22. Group Leader
23. Department Head
24. Other Management (please explain) ______

Design or Standards Personnel

31. Systems Engineer
32. Software Engineer
33. Test Engineer
34. Field Test Engineer
35. Manufacturing Engineer
36. Production Engineer
37. Engineer
38. MTS
39. Consultant
40. Scientist
41. Physicist
42. Other Staff (please explain) ______

9. Products that you specify or authorize purchase of: (Check all that apply)

ICs and Semiconductors
01. ☐ Digital ICs
02. ☐ Linear ICs
03. ☐ Microprocessors
04. ☐ Semiconductor memories
05. ☐ Custom/semicustom ICs

Components
11. ☐ Resistors and capacitors
12. ☐ Interconnections
13. ☐ Switches and relays
14. ☐ Optoelectronic components
15. ☐ Readout and display devices
16. ☐ Fiber-optic components
17. ☐ Printed circuits

Equipment
21. ☐ Power supplies
22. ☐ Test and measurement equipment
23. ☐ Automatic test equipment
24. ☐ Field service test equipment
25. ☐ Analog/digital panel meters
26. ☐ Cabinets and enclosures
27. ☐ Semiconductor production equipment
28. ☐ Robotics components/equipment
29. ☐ Microprocessor development systems

Computer-based Systems and equipment
31. ☐ CAE hardware/software
32. ☐ CAD/CAM hardware/software
33. ☐ Minicomputers
34. ☐ Microcomputers
35. ☐ Computer terminals
36. ☐ Computer boards
37. ☐ Disk/tape memories
38. ☐ Graphic displays
39. ☐ Software packages/services
40. ☐ Printers/plotters
41. ☐ Computer peripherals
42. ☐ Modems
43. ☐ Communications equipment
44. ☐ None of the above

10. Your degree of profit accountability: (Check one box only)

A. ☐ I have direct profit responsibility
B. ☐ I share profit responsibility with others
C. ☐ I have no profit responsibility

11. Your level of sign-off or purchase approval authority for your company o[r] organization: (Check one box only)

A. ☐ None
B. ☐ Less than $1,000
C. ☐ $1,001 to $ 5,000
D. ☐ $5,001 to $10,000
E. ☐ $10,001 to $25,000
F. ☐ More than $25,000

12. Other publications that you read regularly (3 out of 4 issues): (Check all that apply)

A. ☐ Electronic Design
B. ☐ Electronic Engineering Times
C. ☐ EDN
D. ☐ Electronic News
E. ☐ Electronic Business
F. ☐ Computer Design
G. ☐ Electronic Products
H. ☐ None of the above

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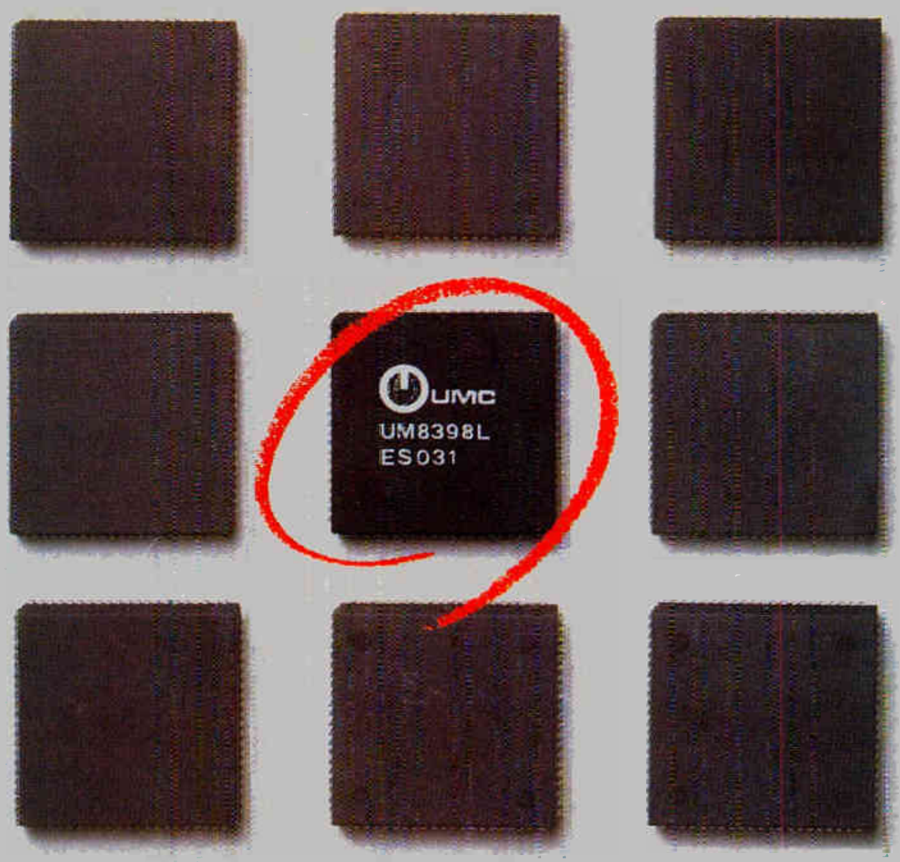

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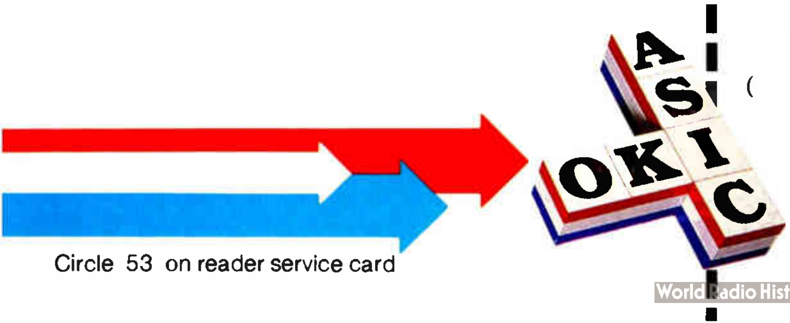

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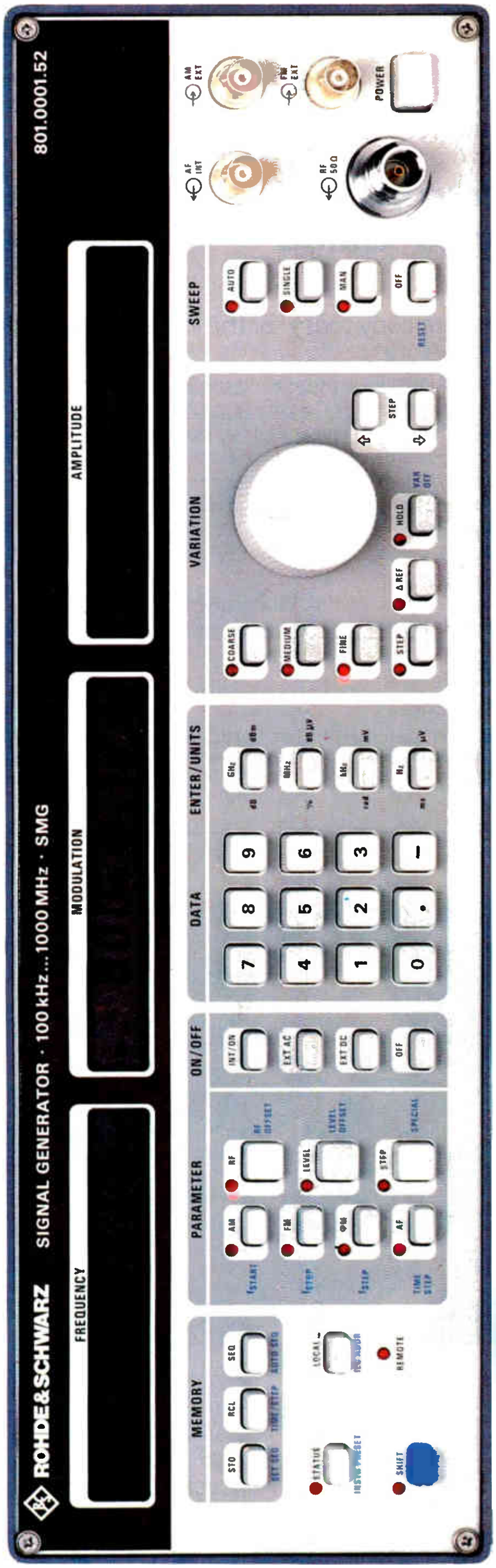

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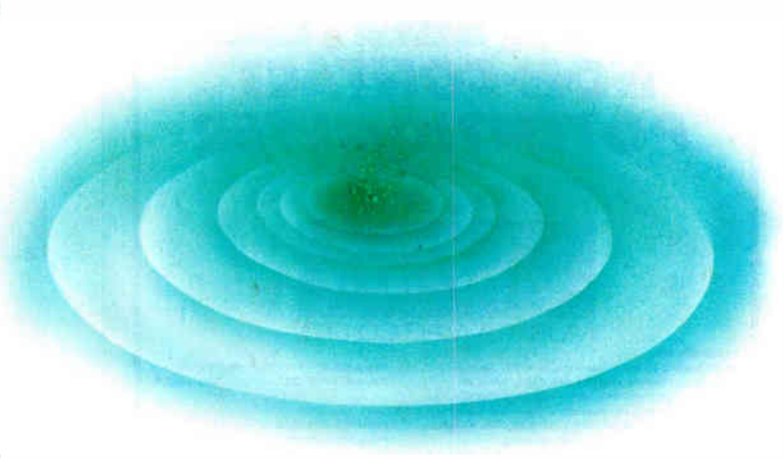

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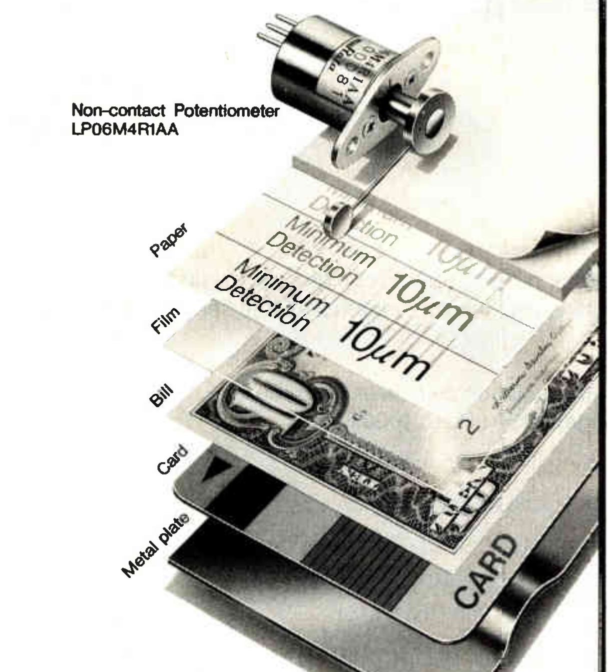

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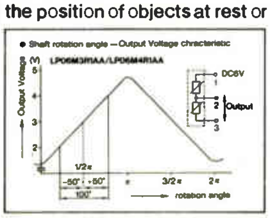

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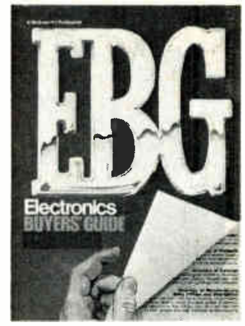

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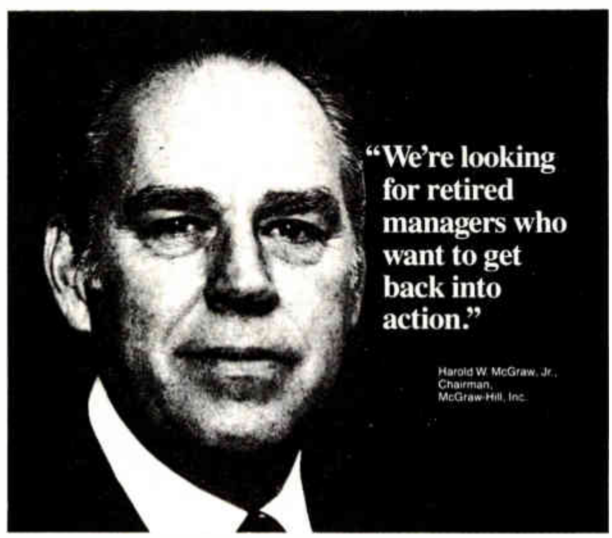

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Single Output.

	MAX CURRENT AT AMBIENT OF (A) 40°C	50°C	60°C	DIMENSIONS (inches)	PRICE QTY. 1	QTY. 100	QTY. 250	QTY. 1000	MODEL
5V ±5% ADJ.	2.0	2.0	1.00	1.22 × 2.91 × 2.83	$ 43.00	$ 34.50	$ 25.75	$ 22.75	LSS-34-5
	3.0	3.0	1.50	1.42 × 2.91 × 3.35	51.00	44.25	30.50	28.00	LSS-35-5
	5.0	5.0	2.50	1.54 × 2.91 × 4.13	79.00	60.00	47.50	37.50	LSS-36-5
	10.0	10.0	5.00	1.54 × 3.74 × 4.72	106.00	88.00	63.50	58.25	LSS-37-5
	20.0	20.0	10.00	2.17 × 3.74 × 6.30	150.00	135.00	104.00	94.50	LSS-38-5
	30.0	30.0	15.00	2.56 × 3.74 × 7.09	215.00	165.00	141.00	129.00	LSS-39-5
6V ±5% ADJ.	1.7	1.7	0.85	1.22 × 2.91 × 2.83	43.00	34.50	25.75	22.75	LSS-34-6
	2.5	2.5	1.25	1.42 × 2.91 × 3.35	51.00	44.25	30.50	28.00	LSS-35-6
	4.2	4.2	2.10	1.54 × 2.91 × 4.13	79.00	60.00	47.50	37.50	LSS-36-6
	8.4	8.4	4.20	1.54 × 3.74 × 4.72	106.00	88.00	63.50	58.25	LSS-37-6
	17.0	17.0	8.50	2.17 × 3.74 × 6.30	150.00	135.00	104.00	94.50	LSS-38-6
	25.5	25.5	12.50	2.56 × 3.74 × 7.09	215.00	165.00	141.00	129.00	LSS-39-6
12V ±5% ADJ.	0.9	0.9	0.45	1.22 × 2.91 × 2.83	43.00	34.50	25.75	22.75	LSS-34-12
	1.3	1.3	0.65	1.42 × 2.91 × 3.35	51.00	44.25	30.50	28.00	LSS-35-12
	2.1	2.1	1.05	1.54 × 2.91 × 4.13	79.00	60.00	47.50	37.50	LSS-36-12
	4.2	4.2	2.10	1.54 × 3.74 × 4.72	106.00	88.00	63.50	58.25	LSS-37-12
	8.5	8.5	4.25	2.17 × 3.74 × 6.30	150.00	135.00	104.00	94.50	LSS-38-12
	12.5	12.5	6.25	2.56 × 3.74 × 7.09	215.00	165.00	141.00	129.00	LSS-39-12
15V ±5% ADJ.	0.7	0.7	0.35	1.22 × 2.91 × 2.83	43.00	34.50	25.75	22.75	LSS-34-15
	1.0	1.0	0.50	1.42 × 2.91 × 3.35	51.00	44.25	30.50	28.00	LSS-35-15
	1.7	1.7	0.85	1.54 × 2.91 × 4.13	79.00	60.00	47.50	37.50	LSS-36-15
	3.4	3.4	1.70	1.54 × 3.74 × 4.72	106.00	88.00	63.50	58.25	LSS-37-15
	7.0	7.0	3.50	2.17 × 3.74 × 6.30	150.00	135.00	104.00	94.50	LSS-38-15
	10.0	10.0	5.00	2.56 × 3.74 × 7.09	215.00	165.00	141.00	129.00	LSS-39-15
24V ±5% ADJ.	0.5	0.5	0.25	1.22 × 2.91 × 2.83	43.00	34.50	25.75	22.75	LSS-34-24
	0.7	0.7	0.35	1.42 × 2.91 × 3.35	51.00	44.25	30.50	28.00	LSS-35-24
	1.1	1.1	0.55	1.54 × 2.91 × 4.13	79.00	60.00	47.50	37.50	LSS-36-24
	2.1	2.1	1.05	1.54 × 3.74 × 4.72	106.00	88.00	63.50	58.25	LSS-37-24
	4.5	4.5	2.25	2.17 × 3.74 × 6.30	150.00	135.00	104.00	94.50	LSS-38-24
	6.5	6.5	3.25	2.56 × 3.74 × 7.09	215.00	165.00	141.00	129.00	LSS-39-24
28V ±5% ADJ.	0.4	0.4	0.20	1.22 × 2.91 × 2.83	43.00	34.50	25.75	22.75	LSS-34-28
	0.6	0.6	0.30	1.42 × 2.91 × 3.35	51.00	44.25	30.50	28.00	LSS-35-28
	0.9	0.9	0.45	1.54 × 2.91 × 4.13	79.00	60.00	47.50	37.50	LSS-36-28
	1.8	1.8	0.90	1.54 × 3.74 × 4.72	106.00	88.00	63.50	58.25	LSS-37-28
	3.8	3.8	1.90	2.17 × 3.74 × 6.30	150.00	135.00	104.00	94.50	LSS-38-28
	5.5	5.5	2.75	2.56 × 3.74 × 7.09	215.00	165.00	141.00	129.00	LSS-39-28
48V ±5% ADJ.	0.2	0.2	0.10	1.22 × 2.91 × 2.83	43.00	34.50	25.75	22.75	LSS-34-48
	0.3	0.3	0.15	1.42 × 2.91 × 3.35	51.00	44.25	30.50	28.00	LSS-35-48
	0.5	0.5	0.25	1.54 × 2.91 × 4.13	79.00	60.00	47.50	37.50	LSS-36-48

Triple Output.

	VOLT Vo	MAX OUTPUT CURRENT (AMPS) 40°C	50°C	60°C	MAX OUTPUT POWER (WATTS) 40°C	50°C	60°C	DIMENSIONS (inches)	PRICE QTY. 1	QTY. 100	QTY. 250	QTY. 1000	MODEL
5V $^{+0.3}_{-0}$ V ADJ., ±12V FIXED	5	7.00	7.00	4.55	50	50	32.5	1.42 × 3.74 × 6.10	$118.00	$ 84.00	$ 71.00	$ 66.00	LST-37-133
	+12	1.50	1.50	0.97									
	−12	0.50	0.50	0.32									
	5	8.00	8.00	5.20	76	76	49.4	1.61 × 3.74 × 6.89	146.00	108.00	95.00	86.00	LST-38-133
	+12	3.20	3.20	2.00									
	−12	0.50	0.50	0.32									
	5	13.00	13.00	8.45	101	101	65.6	1.93 × 3.74 × 7.48	169.00	129.00	117.00	106.00	LST-39-133
	+12	4.00	4.00	2.60									
	−12	1.00	1.00	0.65									
5V $^{+0.3}_{-0}$ V ADJ., ±15V FIXED	5	7.00	7.00	4.55	50	50	32.5	1.42 × 3.74 × 6.10	118.00	84.00	71.00	66.00	LST-37-144
	+15	1.20	1.20	0.78									
	−15	0.50	0.50	0.32									
	5	8.00	8.00	5.20	75	75	49.0	1.61 × 3.74 × 6.89	146.00	108.00	95.00	86.00	LST-38-144
	+15	2.50	2.50	1.60									
	−15	0.50	0.50	0.32									
	5	13.00	13.00	8.45	103	103	67.0	1.93 × 3.74 × 7.48	169.00	129.00	117.00	106.00	LST-39-144
	+15	3.20	3.20	2.00									
	−15	1.00	1.00	0.65									
5V $^{+0.3}_{-0}$ V ADJ., +12V −5V FIXED	5	7.00	7.00	4.55	50	50	32.5	1.42 × 3.74 × 6.10	118.00	84.00	71.00	66.00	LST-37-131
	+12	1.50	1.50	0.97									
	5	0.50	0.50	0.32									
	5	8.00	8.00	5.20	725	725	46.5	1.61 × 3.74 × 6.89	146.00	108.00	95.00	86.00	LST-38-131
	+12	3.20	3.20	2.00									
	5	0.50	0.50	0.32									
	5	13.00	13.00	8.45	94	94	61.0	1.93 × 3.74 × 6.89	169.00	129.00	117.00	106.00	LST-39-131
	+12	4.00	4.00	2.60									
	5	1.00	1.00	0.65									

LS SERIES

Specifications

DC OUTPUT
Voltage range shown in tables.

REGULATED VOLTAGE
regulation, line .... 0.4% for input variations from 85 to 132VAC or 132 to 85VAC.

regulation, load ...... 0.8% for load changes from zero to full load and from full load to zero on LSS models. 0.8% for load changes from .75A to full load on main output of LST-37; from 1.5A to full load on main output of LST-38, LST-39. 150mV max from zero to full load and full load to zero on auxiliary outputs of LST-37, 38, 39 with main output preloaded.

ripple and noise. ...... 15mV RMS for all models; 120mV pk-pk for 5V and 6V models; 150mV pk-pk for 12V and 15V models; 200mV pk-pk for 24V and 28V models.

temperature coefficient .... 0.02%/°C.

AC INPUT
line .... 85 to 132VAC, 47-440Hz.

DC INPUT
110 to 175VDC.

EFFICIENCY
72% typical for 5V LSS models. 70% typical for LST models, and 12V and 15V LSS models. 82% typical on 24V through 48V LSS models.

OVERSHOOT
No overshoot at turn-on, turn-off or power failure.

OPERATING TEMPERATURE RANGE
0-60°C with suitable derating above 50°C.

STORAGE TEMPERATURE RANGE
−30°C to +85°C.

OVERLOAD PROTECTION
External overload protection, automatic electronic current limiting circuit, limits output current to a safe, preset value, thereby protecting the load as well as the power supply.

OVERVOLTAGE PROTECTION
Overvoltage protection is standard on all LSS models and on main output of LST Models. If output voltage increases above a preset level, inverter drive is removed.

HOLD UP TIME
5V and 6V LSS models, and all LST models will remain within regulation limits for at least 16.7 msec. after loss of AC power when operating at full load, nominal output voltage and 100VAC input voltage.

IN-RUSH CURRENT LIMITING
The turn-on in-rush current will not exceed 15A typical on LSS-38, LSS-39; 24A typical for LSS-34; 30A typical for LSS-35, LSS-36, LSS-37; 15A typical for LST-38, LST-39; 35A typical on LST-37.

COOLING
Convection cooled, no fans or blowers needed.

DC OUTPUT CONTROLS
Simple screwdriver adjustment.

REMOTE SENSING
Provision is made for remote sensing to eliminate the effects of power output lead resistance on DC regulation for LSS-38 and LSS-39.

INPUT AND OUTPUT CONNECTIONS
All input and output connections are made via barrier strip terminals.

OUTPUT STATUS INDICATOR
LED indicates presence of output voltage on LSS models and 5V output of LST models.

MOUNTING
Two mounting surfaces, two mounting positions. One mounting surface and one mounting position for LSS-39. Some derating may be required in horizontal mounting position.

ISOLATION RATING
2000V RMS input to output.

PHYSICAL DATA

Package Model	Weight Lbs. Net	Weight Lbs. Ship	Size Inches
LSS-34	0.46	0.55	1.22 × 2.91 × 2.83
LSS-35	0.64	0.75	1.42 × 2.91 × 3.35
LSS-36	0.66	0.75	1.54 × 2.91 × 4.13
LSS-37	0.88	1.00	1.54 × 3.74 × 4.72
LST-37	0.93	1.10	1.42 × 3.74 × 6.10
LST-38	1.21	1.41	1.61 × 3.74 × 6.89
LST-39	1.54	1.79	1.93 × 3.74 × 7.48
LSS-38	1.54	1.85	2.17 × 3.74 × 6.30
LSS-39	2.31	2.50	2.56 × 3.74 × 7.09

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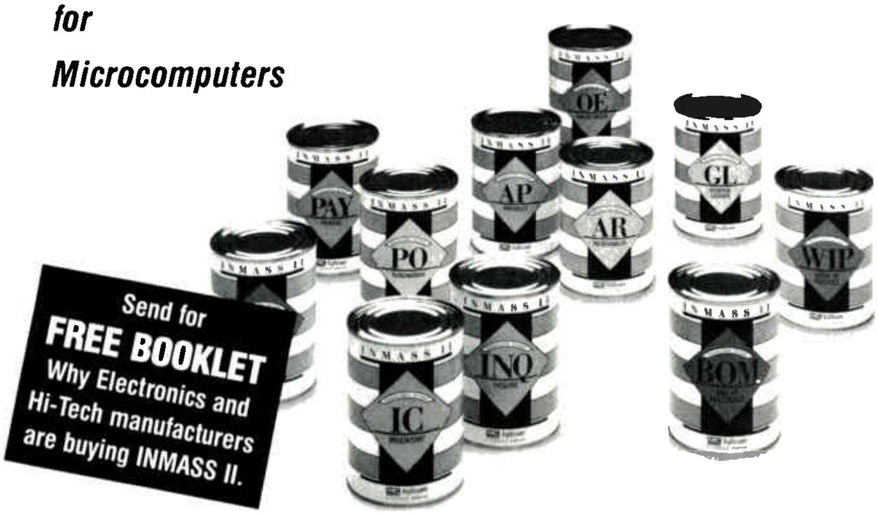

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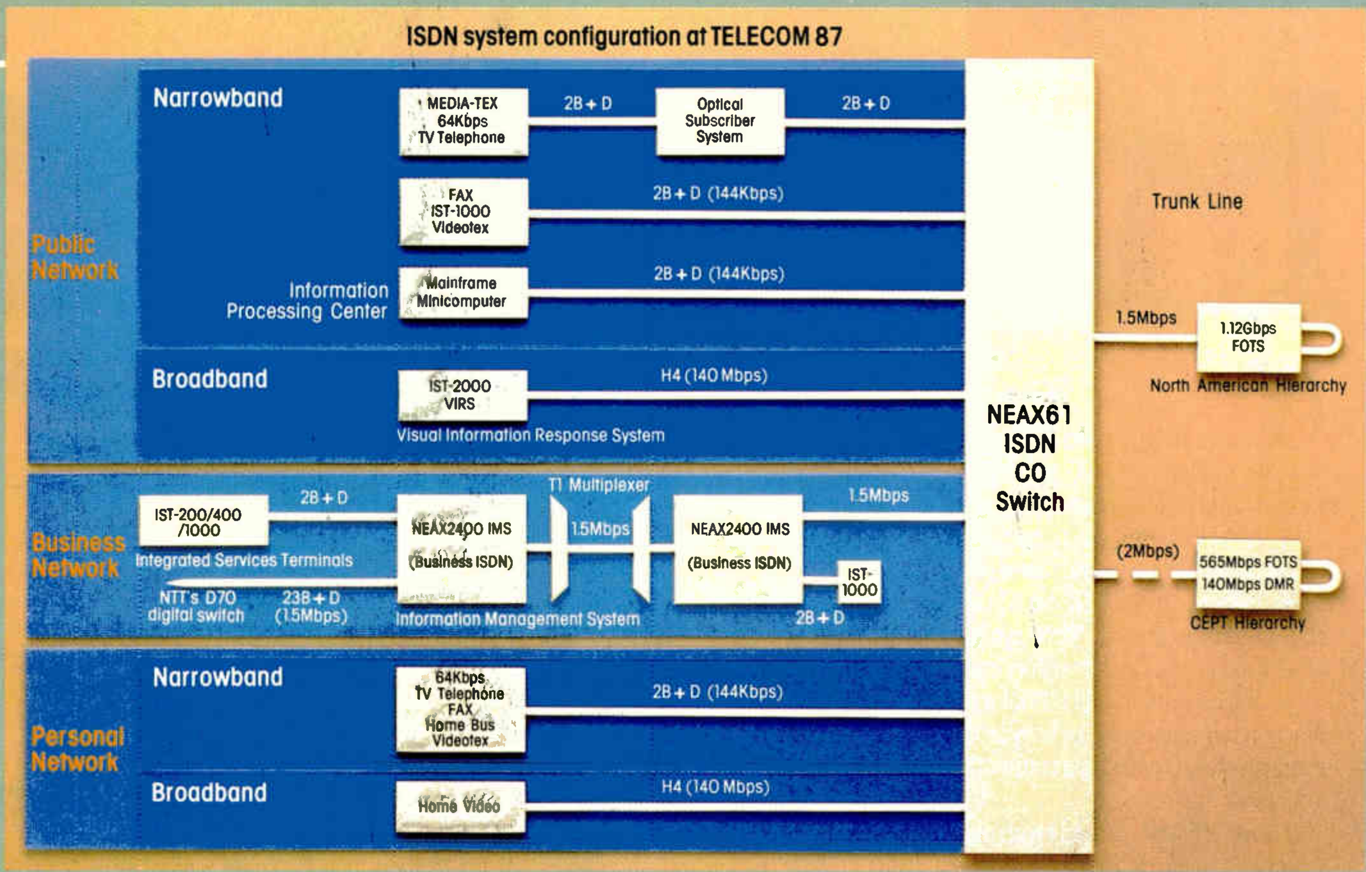
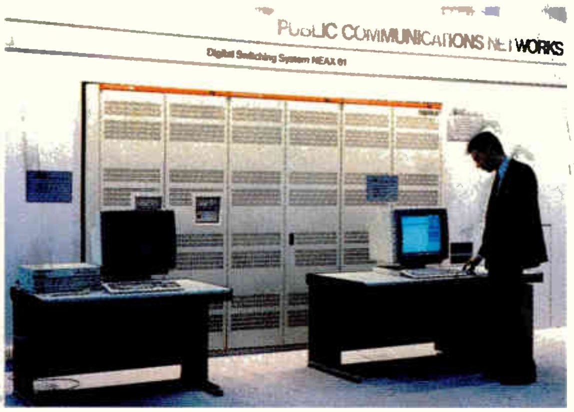




Digital switching system: NEAX61

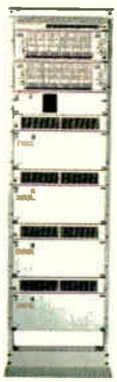
The core of the demonstration was the NEAX61. It displayed integrated broad- and narrowband switching capability, as well as 1.5Mbps high-speed packet switching.

Network management system (NMS)

The NMS efficiently monitors/controls switching and transmission networks. For easy trouble-shooting, it offers expert system technology which guides users to the source of system problems.

1.12Gbps FOTS

The 1.12Gbps Fiber Optic Transmission System (FOTS) demonstrated its ability to combine 16,128 voice channels into a single-mode fiber.



AT THE R&D ZONE

NEC's intensive R&D efforts, ranging from components to total systems, gave visitors a glimpse of many futuristic visions come true.

4Gbps FOTS

This ultra high-speed system utilizes 1.55μm DFB LDs and InGaAs APDs and transmits over 30km without repeaters.

Photonic switching

NEC's display included a photonic switching system with 8×8 matrix optical switches. The system demonstrated 140Mbps broadband switching capability using IST-2000 video communication terminals.

High resolution CCD color camera

A compact HDTV camera, featuring 1.24-million pixel CCD chips, showed the latest advance in CCD technology.

NEC

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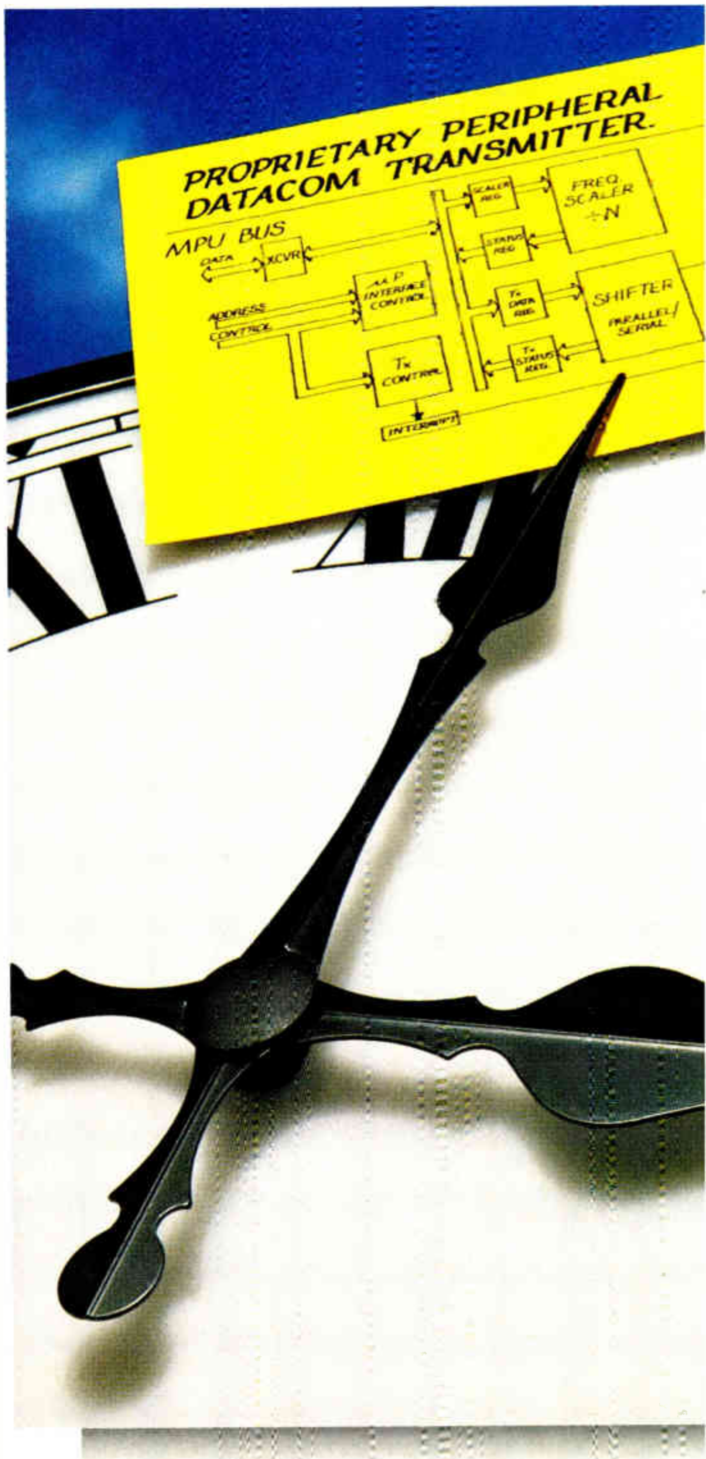

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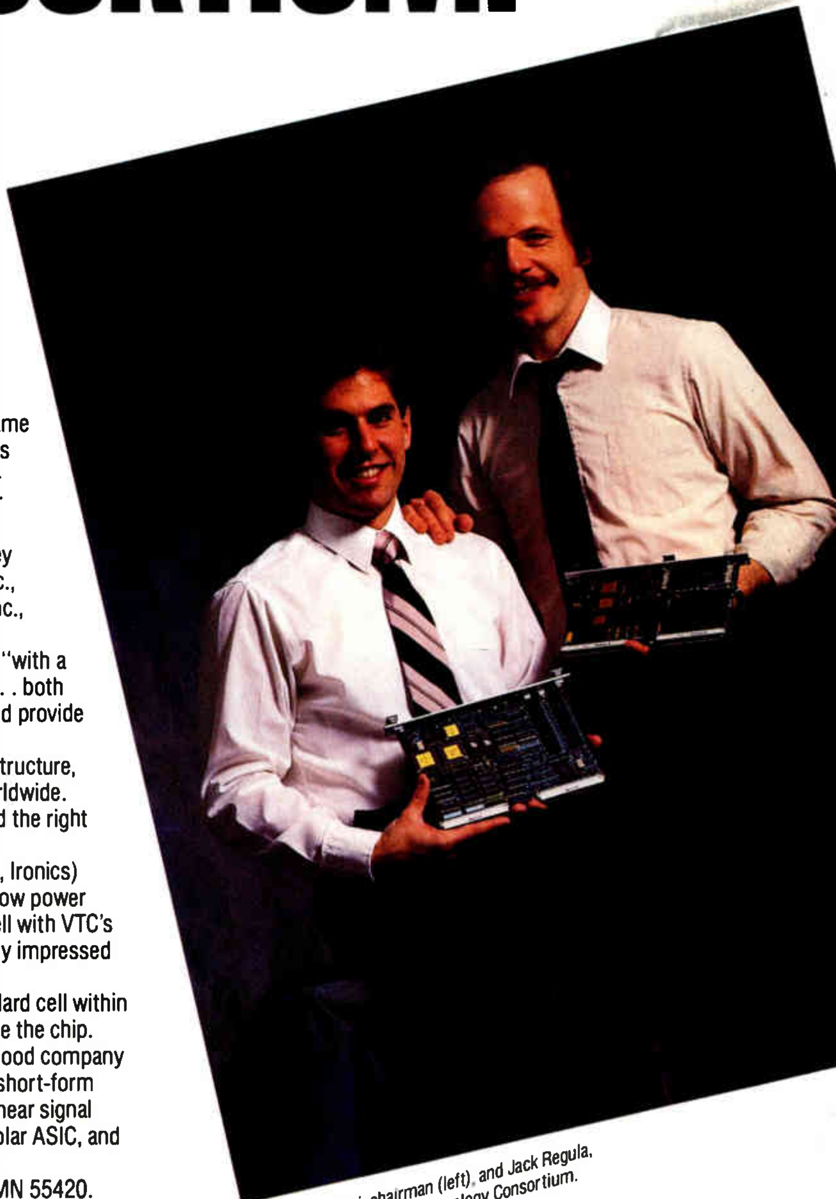
WHY VTC? ASK THE VME CONSORTIUM.

"For a bunch of companies that don't always agree on everything, we sure were unanimous on VTC."



Joseph Ramunni, chairman (left), and Jack Regula, technical director, VME Technology Consortium.

The VME Consortium needed an economical, yet highly functional VME bus interface chip, to minimize design time . . . and to help raise the VME standard to higher levels.

"We looked at the leading suppliers," said Joe Ramunni, consortium chairman (and president of Mizar), "and VTC came out on top. Their CMOS standard-cell ASIC approach gave us the high drive capability we needed, optimized for bus interfacing. And, it proved much more cost-effective, with higher performance, than gate array technology."

The VME Consortium is made up of such firms as Plessey Microsystems, Omnibyte Corporation, Mizar Inc., Ironics Inc., Heurikon Corporation, Matrix Corporation, and Clearpoint Inc., among others. What did they look for in a supplier?

"We needed a credible business partner," said Ramunni, "with a proven track record, who could provide a turnkey package . . . both design and fab. A supplier that could produce in quantity, and provide technical support to the market at large.

"We also needed a firm with an international marketing structure, because we expect this chip to be the de facto standard worldwide.

"But, we needed *people* we could work with, too. VTC had the right 'comfort factor'."

Jack Regula, consortium technical director (and VP-R&D, Ironics) added: "Our requirements for high speed, high gate-count, low power consumption, and VME bus drive capability were all met well with VTC's 1-micron CMOS standard cell library. And we were extremely impressed with VTC's facilities, its people, and its customer list."

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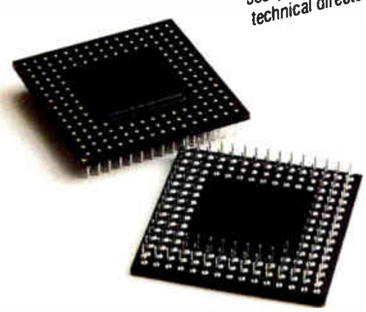

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INSIDE TECHNOLOGY

A TORRENT OF FUTURE PRODUCTS AT THE SOLID STATE CONFERENCE

Now more than ever, the ISSCC is the leading barometer for divining the future direction of the semiconductor industry and its customers; the annual event is clearly the center stage for previewing significant upcoming products

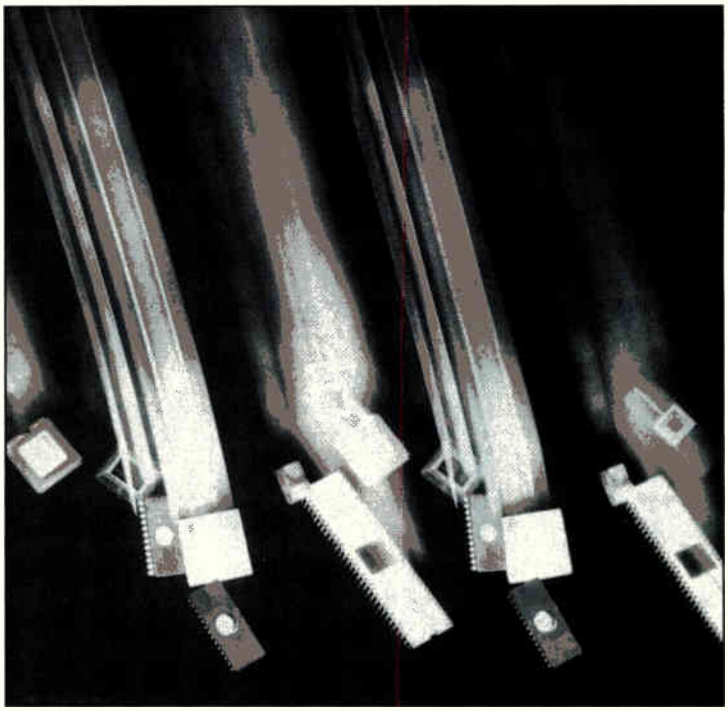
by Bernard C. Cole

The annual International Solid State Circuits Conference, convening in San Francisco this week, looks like the best one yet. More than ever, the 31-year-old conference is turning into the leading barometer for reading the future direction of the semiconductor industry and its systems customers. Not only does the ISSCC continue to be the premier forum for reporting on new technology, but it is now the stage on which chip makers preview major new products slated for introduction anytime from the next few months to the next two years. This year's incredibly rich harvest of papers points to the following new products:

- A flood of various memories that push the frontier of density and speed. This year, papers from Hitachi, Matsushita, and Toshiba report on 16-Mbit dynamic random-access-memory designs (see p. 68). Equally impressive are the high-density, high-speed static RAMs, including sub-35-ns 1-Mbit circuits from Fujitsu, Hitachi, IBM, Mitsubishi, and Philips (see p. 69), as well as sub-15-ns ECL-compatible biCMOS SRAMs from Hitachi, Fujitsu, National Semiconductor, and Texas Instruments (see p. 71). These devices make it possible for system designers to rethink the hierarchy of memory storage. For example, 16-Mbit dynamic RAMs mean replacing several megabytes of disk drive with a single circuit. And sub-50-ns static RAMs in the 1-Mbit range can be substituted for dynamic RAMs in the main memory of many 32-bit microprocessor-based applications.
- A slew of specialized application- and algorithm-specific processors performing functions previously handled in software. One particular focus this year is graphics, with specialized processors from General Electric, Matsushita, Nippon Telegraph & Telephone Corp., Toshiba, and Visual Information Technologies (see p.73).
- A host of analog-to-digital-converter chips (see p. 77) that show there is more than one way to get high speed, accuracy, and resolution.

Along with the general trends are the individual achievements. These include:

- Intel Corp.'s introduction of a 4-Mbit ultraviolet-erasable programmable read-only memory. It opens numerous new application areas (see p. 72). A single nonvolatile memory chip will be able to store as much data as several floppy disks.
- Rockwell International's 8-bit-slice, 1-μm depletion MES FET gallium arsenide processor. As well as reaching an impressive level of complexity for GaAs, it runs at 150 million operations per second (see p. 74).
- Actel Corp.'s antifuse-based configurable gate arrays. They could combine the density of traditional gate arrays with the flexibility of EPROM and EEPROM-based programmable logic devices (see p. 75).
- The source of many future chips will be IBM's computer-aided-design system, which is capable of designing chips with a mixture of analog and digital devices and standard cells that have 75% routability. It uses a maze-runner algorithm to generate wiring automatically (see p.76).



THE NEXT WAVE: 16-MBIT DRAMS FROM JAPAN

An announcement concerning dynamic random-access memories at the ISSCC in recent years has almost always had the ability to astound, often leaving attendees shaking their heads in amazement and, in the case of U. S. engineers, not a little regret and perplexity. This year's meeting in San Francisco is no exception.

Scarcely has production begun on 1-Mbit DRAMs and approached the sampling stage on a few 4-Mbit circuits than the 16-Mbit DRAM is on the scene—not from one source, but from three. And all of them are Japanese. Hitachi Ltd. is showing a 16-Mbit design employing a transposed data-line structure; Matsushita Electric Industrial Co.'s device has an open-bit-line architecture; and Toshiba Corp. is demonstrating a unique design that incorporates a serial 1-Mbit high-speed read/write mode.

When these devices are finally brought to the marketplace, advanced 16- and 32-bit microprocessors will finally have a memory device to match their megabytes of address space. In terms of system performance, a typical personal computer with such high-density DRAMs could achieve as much as a tenfold improvement in performance, due to the fact that half a dozen of the most memory-hungry application programs for word processing, spreadsheets, and desktop publishing could be located in DRAM. This means they would not need to be constantly seeking to access the disk drives.

But if the efforts described so far by these three companies are any indication, there are considerable technical hurdles left to overcome. It will be at least 1990 before such devices begin appearing in sample quantities.

At Hitachi, engineers have come up with a single 5-V design with an internal 3.3-V operating voltage for the memory array. This design allows access times in the 60-ns range and cycle times of about 180 ns, with a typical power dissipation of 420 mW. To get such performance, Hitachi designers have gone to a 0.6-μm twin-well CMOS process using double-level metal.

One of the major problems the Hitachi designers have run into is interference noise due to an increase in interdata-line capacitance. Although similar problems have occurred at lower densities, at the 16-Mbit level they take on new importance. The engineers report encountering a new form of data-line interference noise generated during the sense-amplifier operation. It was to address this problem that they devised their transposed data-line structure, which should reduce such noise by a factor of about three—from roughly 25% of the signal to less than 10%.

BRINGING DOWN THE SIZE

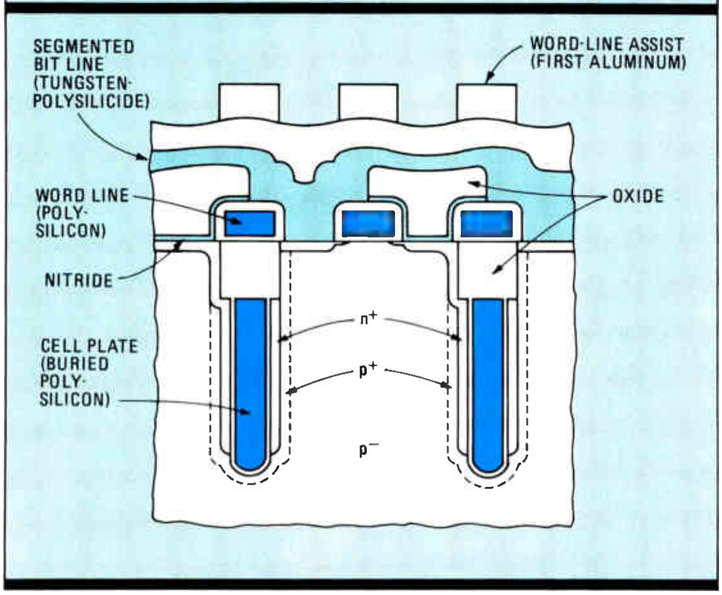
The designers at Matsushita have posed themselves an even more difficult problem, a 16-Mbit design with roughly the same access and cycle times as the Hitachi device, but tucked into a diminutive chip area. The Matsushita designers have been able to build a cell with an area of 4 μm^2, which allows the DRAM to be incorporated into a low-cost, 300-mil, dual in-line package. To shrink the cell, Matsushita uses a 0.5-μm n-well CMOS process with double polysilicon, double metal, and a single level of polysilicide (see figure).

The traditional open-bit-line architecture and trench isolation that Matsushita uses make possible the small-geometry cell. But the total packing density is constrained, since scaling of the cell is limited by the layout pitch of the array's sense amplifiers. To reduce the size of the total array, the designers devised a relaxed sense-amplifier pitch scheme.

The only problem with this modified open-bit-line architecture, in common with earlier designs, is that it still has a noise immunity far inferior to the less dense folded-bit-line approach. So, the designers have adopted a reverse dummy word-line technique for use in a memory array segmented into thirty-three 512-Kbit blocks of 2,048 segmented bit lines and 256 word lines.

In this design, one reverse dummy word line is assigned to each 256 word-line segment. Only a dummy word line belonging to the segment having an accessed word line turns to a low level;

MATSUSHITA'S TINY 16-MBIT DRAM CELL



Matsushita achieves minimum cell size in its open-bit-line architecture using a trench construction for the storage capacitor.

the other dummy word lines of nonselected segments are kept high. Consequently, the researchers say, the noise that occurs by coupling between the word line and the bit line is canceled.

The Toshiba 70-ns DRAM achieves 16-Mbit density through a combination of advanced CMOS processing, a new stacked trenched-capacitor cell, and a pseudo-open-bit-line layout. Using 0.7-μm design rules, the device incorporates a cell measuring 6.12 μm^2 and fabricated using a p-well CMOS process with three levels of polysilicon, two levels of aluminum, and a single level of molybdenum silicide. Intended for applications in high-definition image processing, the RAM has been developed to have a 100-MHz serial read/write mode for up to 2 Kbits of continuous data.

The peripheral circuits are formed with a twin-tub CMOS process. As in the other 16-Mbit designs, the device employs a trenched capacitor cell. But to reduce intercell leakage, the memory cell is constructed with a polysilicon-to-polysilicon capacitor in a trench and a side-wall diffusion layer from the first layer of polysilicon.

To increase packing density, designers at the company's VLSI Research Division in Kawasaki use a pseudo-open-bit-line architecture. In this architecture, blocks of 32-bit columns are laid out alternately as open-bit and folded-bit-line arrays. Since the polysilicon cell plate is located below, rather than beside, the switching transistor, self-aligning contacts are not needed to connect the bit line to the cell. In order to save space in the area devoted to decode logic, the second aluminum is used for column-select lines from a common column decoder.

–Bernard C. Cole

TECHNOLOGY TO WATCH is a regular feature of *Electronics* that provides readers with exclusive, in-depth reports on important technical innovations from companies around the world. It covers significant technology, processes, and developments

TECHNOLOGY TO WATCH **ISSCC**

FIVE BLAZING FAST CMOS SRAMS ARE COMING

As eye-catching as the 16-Mbit dynamic random-access memories may be, the development that will have a more immediate effect on the way memory is implemented is the new breed of static RAMs combining 1-Mbit density with blazing speed. Five such CMOS devices—three from Japan and one each from the U. S. and the Netherlands—emerged at this year's ISSCC boasting access times ranging from 14 to 30 ns. The entries come from Japan's Fujitsu Ltd., Hitachi Ltd., and Mitsubishi Electric Corp., as well as from IBM Corp.'s General Technology Division in Essex Junction, Vt., and Philips's Research Laboratories in Eindhoven, the Netherlands.

Other than using CMOS as the base process, the five SRAMs have little in common. Four designs—from IBM, Hitachi, Mitsubishi, and Philips—are built around a six-transistor cell for high speed. Fujitsu Ltd. has instead opted for a four-transistor design with polysilicon resistor loads to achieve high density. The Philips chip is organized as 128 K by 8 bits, while those from Fujitsu and Hitachi feature a 256-K-by-4-bit architecture. The IBM SRAM can be configured by laser personalization into 128 K by 8 bit, 256 K by 4 bit, or 1 M by 1 bit. The Mitsubishi chip boasts a 1-M-by-1-bit organization, dynamically reconfigurable for testing to 256 K by 4 bits.

Once such high-speed 1-Mbit SRAMs become commercially available in the next year or so, designers of personal computers and low-end work stations using 32-bit complex- or reduced-instruction-set central processing units will have to rethink the way they use memory, says the chairman of the SRAM session at the ISSCC. "Currently available 32-bit CPUs running at 10 to 20 MHz are far outdistancing the performance of the 70- to 120-ns 256-Kbit and 1-Mbit CMOS DRAMs," says Roger Kung, who is director of MOS memory design at Motorola Inc. in Austin, Texas.

As a result, system designers currently must either employ wait states to compensate for the lower-speed main memory, or incorporate lower-density 15- to 35-ns data-cache and tag-cache SRAMs between the CPU and the higher-density main memory. "With the availablity of 15- to 35-ns 1-Mbit SRAMs, designers who can afford it can build 32-bit-based systems with just one kind of memory device," Kung says. "This will considerably simplify their designs and significantly lower overall system cost."

The most flexible 1-Mbit SRAM design is IBM's. In addition to the three organizations, it can also be configured to run asynchronously, with static-column and chip-enable speed-up modes; or synchronously, with a fast-page or static-column mode. As an asynchronous device, access time is 34 ns. In the static-column mode, access time is 33 ns, and in the chip-select speed-up mode, 29 ns. As a synchronous SRAM, access time is 29 ns, with a fast-page-mode speed of 24 ns.

To achieve a size of about 58 μm^2 for the six-transistor cell, the IBM device uses a 0.9-μm retrograde n-well polysilicon CMOS process with two metal layers, one of tungsten and one of aluminum. Active power dissipation is 225 mW in the synchronous mode and 230 mW in the asynchronous. Consisting of four quadrants of 256 Kbits partitioned into eight blocks of 32 Kbits each, the device has a chip area of 10.8 by 8.5 mm^2. It can operate off either 3.3- or 5-V supplies.

Departing from the six-transistor approach is

ONE-CHIP ADCs REACH 2 GHz; OTHERS HIT 18-BIT ACCURACY

This year's ISSCC clearly demonstrates why the analog-to-digital converter remains the quintessential analog circuit and why no other function better represents its class. The ADC continues to dazzle with architectural virtuosity that vaults it to unprecedented heights of resolution, speed, and accuracy.

Driven by the needs of video and digital signal processing, among other things, single-chip ADCs are rising to the occasion, reaching sampling rates of 2 GHz and resolutions of 18 bits, albeit not simultaneously. To stretch that far in performance, however, architectural design alone may not be enough, says Robert Blauschild, chairman of the session on ADCs. Indeed, advances in mortar and brick—in the form of advanced processing—are just as essential in some cases.

So, while some designers at the ISSCC are busy describing monoliths wrought with such techniques as pipelining, error correction, sampling-and-holding, recursion, and folding, others are revealing the biCMOS and leading-edge bipolar processes making possible the techniques or contributing to the speed of operation. One unusual converter, to be described by engineers from Analog Devices Inc., Wilmington, Mass., is highly representative of the new breed. Intended for audio-digital-signal processing and designed by both analog and digital experts, the 10-μs device converts its 14 bits in five successive (recursive) passes through a 4-bit flash subconverter, each time narrowing down its range. It accepts its ac input signal through an on-board sample-and-hold amplifier. To do all that, the chip's circuits are carved from biCMOS—CMOS for its complex logic and output registers, bipolar for its sample-and-hold and other amplifiers.

Another high riser, from Philips Research Laboratories in Sunnyvale, Calif., is an 8-bit, 100-MHz flash ADC with a twist—it folds its input signal eight times, interpolates some of the more significant bits, and uses the same comparators a number of times (see figure). The idea is to cut the number of comparators—to 66 from the 255 conventionally needed—and reduce die size so as to realize the stringent signal and clock timing distribution needed to achieve the high speed.

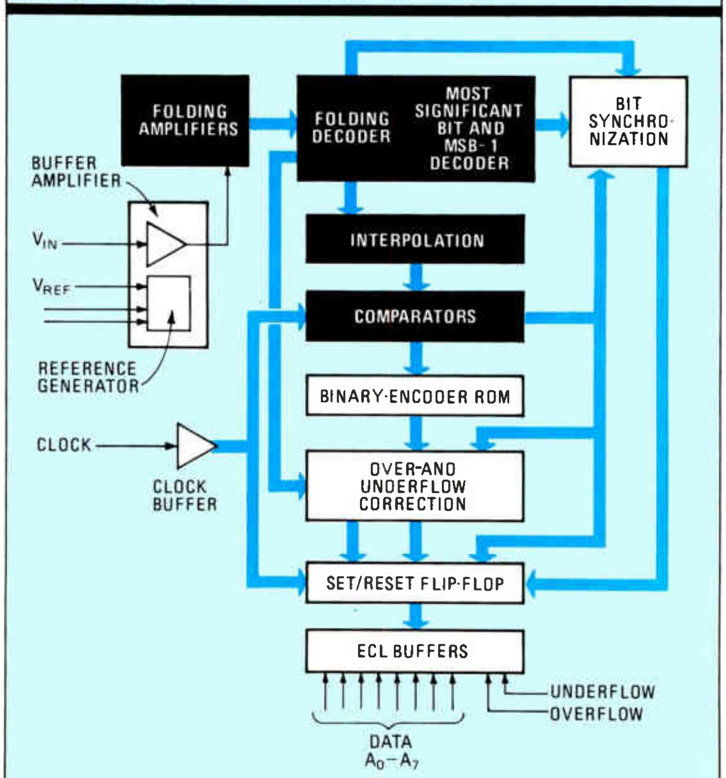
Still another way to get high resolution (above 8 bits) at the speed of flash ADCs—without the attendant hardware—is with pipelining. One chip that does just that comes from the Electronics Research Laboratory at the University of California, Berkeley. According to designers Sehat Ray and Paul Gray, to maintain 13 bits of differential linearity, three stages of pipelining alone were not enough; they had to add a segmented DAC to correct errors. The resulting design could run at 1.5 million samples/s when fabricated in 3-μm CMOS. Instead, the designers chose to optimize for least area. The result: speeds of 250,000 samples/s and dimensions of 1.4 by 1.6 mm.

Pipelining appears again in two other CMOS ADCs. One exhibits high throughput (1 MHz) and linearity (12 bits) with relatively little circuitry. This is achieved by cascading 1-bit ADCs and using a capacitor averaging technique to correct crucial errors. The other strides at 20 MHz and resolves 8 bits by digitally correcting errors and autozeroing its differential comparator/sample-and-hold circuit. The first is a joint effort of the Department of Electrical and Computer Engineering at the University of Illinois in Champaign-Urbana and AT&T Bell Laboratories, Murray Hill, N. J.; the second hails from various groups at Hitachi Ltd. in Tokyo.

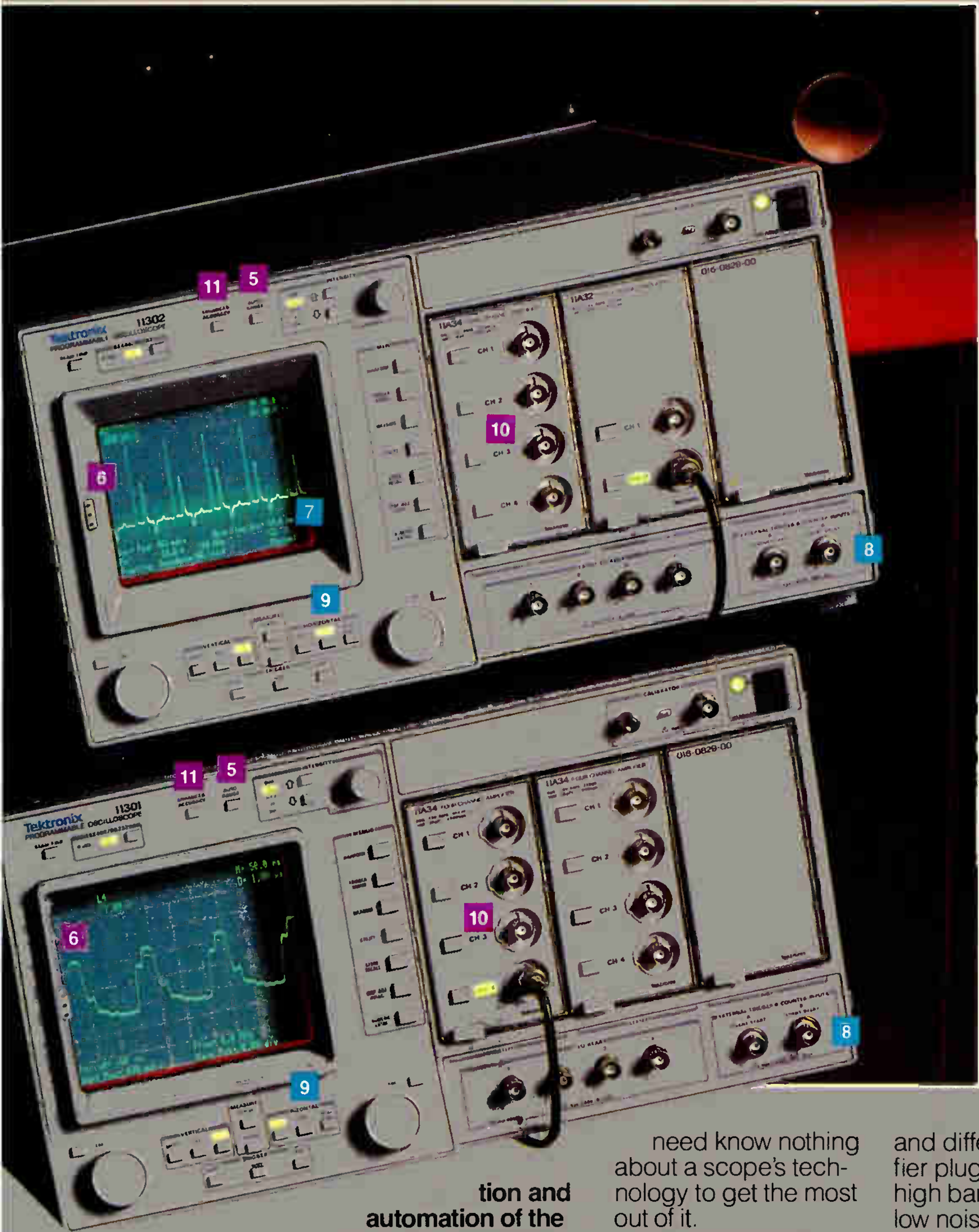
Top honors for speed go to Nippon Telegraph and Telephone LSI Laboratories' bipolar flash 6-bit ADC. It samples at a blazing 2 gigasamples/s. Another medal winner, this time for resolution, is an 18-bit performer from NEC Corp. with 105-dB signal-to-noise ratio and 0.003% total harmonic distortion.

–Stan Runyon

HOW PHILIPS BOOSTS SPEED



Philips cuts the number of comparators in its 8-bit analog-to-digital converter from 255 to 66 in order to reduce die size. The result: 100-MHz flash speed.



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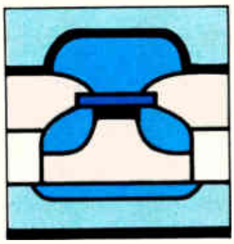


CAN U. S. CHIP PROFITS PAY FOR A NEW GENERATION OF FABS?

The current surge in earnings might make it easier to say yes, but some experts continue to worry that profits over the long term still won't be able to support the high cost of building plants employing the fine-line technology of the 1990s

by J. Robert Lineback

Happy days are here again for the U. S. semiconductor industry, with record profits reported at almost every chip maker, from giants like Intel Corp. down to recent startups. But behind the celebrations, a wide-ranging controversy still rages over the long-term viability of the semiconductor business.

On the one hand, many industry observers are alarmed by the poor long-term return on equity they see among chip makers. Some analysts offer bleak assessments of recent balance-sheet trends and maintain that the low profit margins have set fundamental changes in motion while the industry rode the roller-coaster cycles of the turbulent 1980s. They don't see how industry profits can support the capital-intensive push to the next generation of fine-line chip-fabrication technology.

On the other hand, chip merchants refute the gloom-and-doom scenarios, saying low returns on equity in the 1980s are false profit indicators, warped by the unusually hard times early this decade, notably the punishing market-share wars with Japan. While they worry about the cost of new fab lines, they also see encouraging signs in the market. They feel that careful management, the use of shared foundries, and focused market strategies will pull the industry through.

Such steps are crucial, say most analysts, who put chip-industry returns on equity near a poor 6% average for the decade—about half of what it was in the 1970s and far from the profit margins of most other electronic segments. With that rate of return, they argue, chip makers are not self-supporting.

"They seem to be at a critical crossroad," says Peter Bearse, president of Development Strategies Corp., Gloucester, Mass., which recently conducted an industrywide survey on profit margins for the American Electronics Association. The survey shows chip making second to last in the ratio of net income to equity, when stacked up against other 1987 electronics businesses (see chart, right). And the ratio was lower in the 1987 recovery year than in the weaker 1982 period.

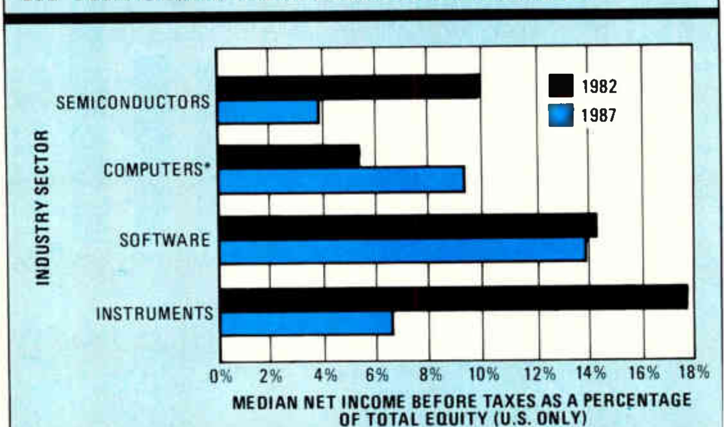
The survey also showed that semiconductor capital expenditure rates were lower than all other major segments except for production equipment (see chart, p. 82). The fast pace of chip technology is quickly making production equipment obsolete, setting up what is expected to be a capital-investment crunch at a time when profit margins are unattractive to investors.

"This is a profitable business, but the long-term problem is that the profits are not enough to pay for the next round of fab," warns analyst Andrew J. Kessler with PaineWebber Inc. in New York.

Michael J. Krasko, managing director at L. F. Rothschild & Co. Inc. in New York agrees. "I think over time it will become increasingly difficult for the semiconductor industry to generate returns that support continued equity investments. The long-term impact is the consolidation of the industry first, and then a greater focus by all semiconductor manufacturers on what areas to pursue."

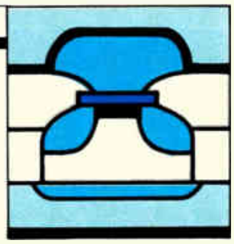
Chip-company executives respond that the profit declines have been an aberration caused by too

THE FINANCIAL PICTURE IS WORSENING IN THE SEMICONDUCTOR BUSINESS



*NOTE: COMPUTER FIGURES FOR 1982 DO NOT INCLUDE THE THEN-SMALL MICROPROCESSOR-BASED SEGMENT

SOURCES: AMERICAN ELECTRONICS ASSOCIATION AND DEVELOPMENT STRATEGIES CORP.



MOTOROLA'S BOMBSHELL— A RISC CHIP THIS SPRING

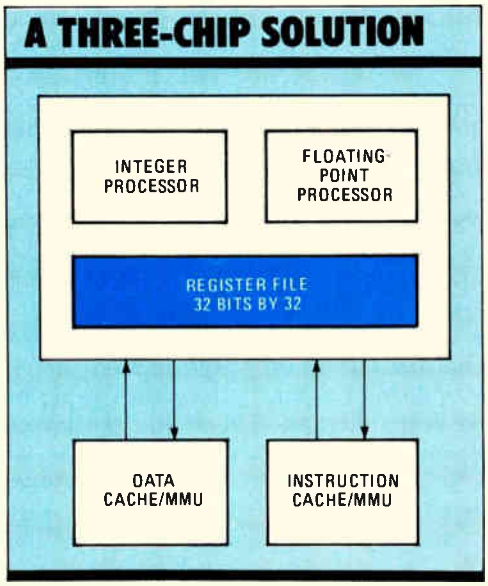
The chip maker saw silicon last year, and now it's almost ready to release a three-chip set, optimized for Unix, that will start out at 17 mips and could make systems that hit 50 mips

by Stan Runyon

Motorola Semiconductor Inc. is about to spring one big surprise on the electronics industry. While it's no secret that the U. S. chip leader has been working for a couple of years on a reduced-instruction-set-computer chip, only a few of its customers know that the chip maker saw silicon last year and expects to unwrap its product—a three-chip set—sometime during the second quarter of 1988.

Perhaps more surprising than the lightning-like speed of Motorola's moves is the comprehensive nature of the results. Not only will Motorola unveil a three-chip RISC set based on the Harvard architecture, but it will also offer a complete systems solution, including crucial development software. "We're going to provide everything from soup to nuts this year for the customer," says Jack W. Browne, Jr., marketing director of the company's High End MPU Division in Austin, Texas. Ready to go, for example, is a software simulator and a system to run Unix.

"People will be surprised at how complete our product offering is and how fast we're moving," Browne says. And here's an even bigger bombshell: Motorola already has two dozen customers committed to its new 32-bit RISC family; another 200 potential customers are evaluating it. The set—composed of a central processing unit chip and two cache/memory-management chips, one each for the instruction and data paths—will burst out of the gate fortified with architectural horsepower meant to leave the competition eating dust (see figure). "Working silicon is here, and we have measured its speed at 34,000 Dhrystones," Browne says. "We are projecting a rough rate of 17 working VAX mips to start, but we will show our customers how they can hit 50 mips this year." Sun Microsystems RISC chip—the scalable processor architecture, or Sparc—carries a 7- to 10-million-instructions-per-second rating [*Electronics*, Sept. 3, 1987, p. 72].



Motorola's 17-mips RISC chip set hinges on the classic Harvard architecture.

There appears to be plenty of performance headroom in the Motorola RISC—which will not be dubbed the 78000, its rumored designation. Carved out of 1.5-μm double-metal double-polysilicon CMOS, the set is scalable. It can go down to 0.8 μm, independently of the architecture, which has been optimized to run the Unix operating system, Browne says.

Despite all the heat and noise generated in the past year about RISC chips, "Motorola is not playing catchup," Browne maintains. Some observers have wondered just how the chip giant would enter the RISC market in a way that wouldn't hurt its lead in the 32-bit microprocessor market. But Browne sees no competition between Motorola's wildly successful complex-instruction-set 68000 family and its RISC chips, which are source-code—but not binary—compatible. "The issue is time to market, both for us and our customer. RISC's simplicity lets us quickly satisfy the speed craving and lets our customers streak into their markets with raw performance. The 68000, on the other hand, is in more of a price-sensitive market.

"There'll be no cannibalization of the 68000 market," Browne says. "We'll take the RISC business out of other people's hides." He is counting on Motorola's resources, reputation, and huge customer base. And he is quick to mention the more than $20 million that Motorola will spend this year alone in RISC development, not counting process

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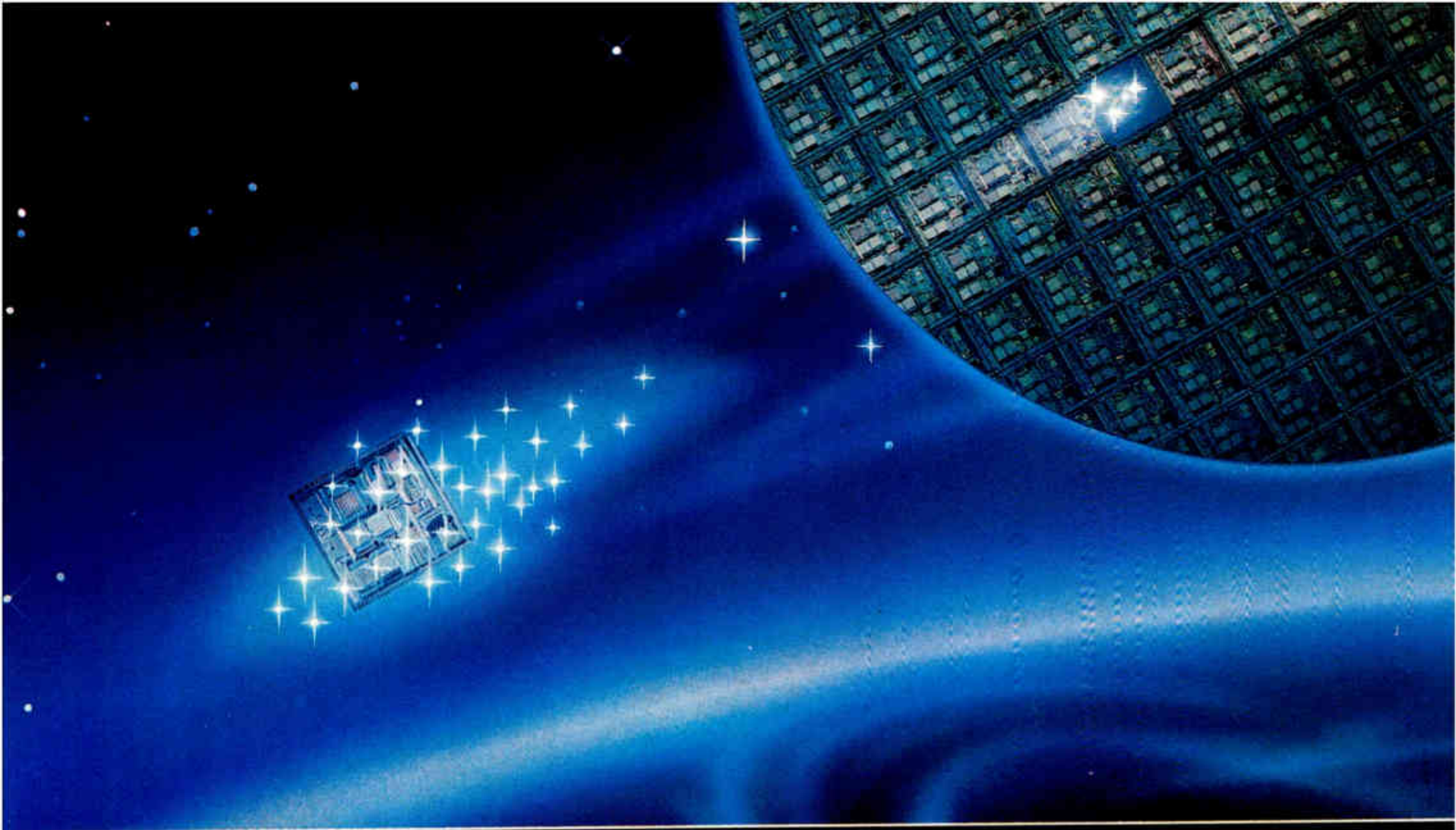

say about a little bit.

Little bits of silicon are also used in the Philips Smart Card - although the processing power required is, of course, much less than that of the superchip.

The Smart Card contains a microchip within its plastic cover to provide both security and intelligence. In fact, the Smart Card is a tiny personal computer which can be programmed for a variety of cardholder services.

For example, as a personalized passkey, it can provide privileged access to a residence, a business complex, a computer system or an electronic network. As a storage medium for the cardholder's medical history it can even become a lifesaver.

In France, where Philips helped to pioneer the Smart Card, the national banking association has adopted it for electronic financial transactions.

The 1-Mbit chip and the Smart Card are only two examples of Philips' extensive R&D programme on which the company spends over U.S.$2 billion each year, translating high technology into tangible user benefits.

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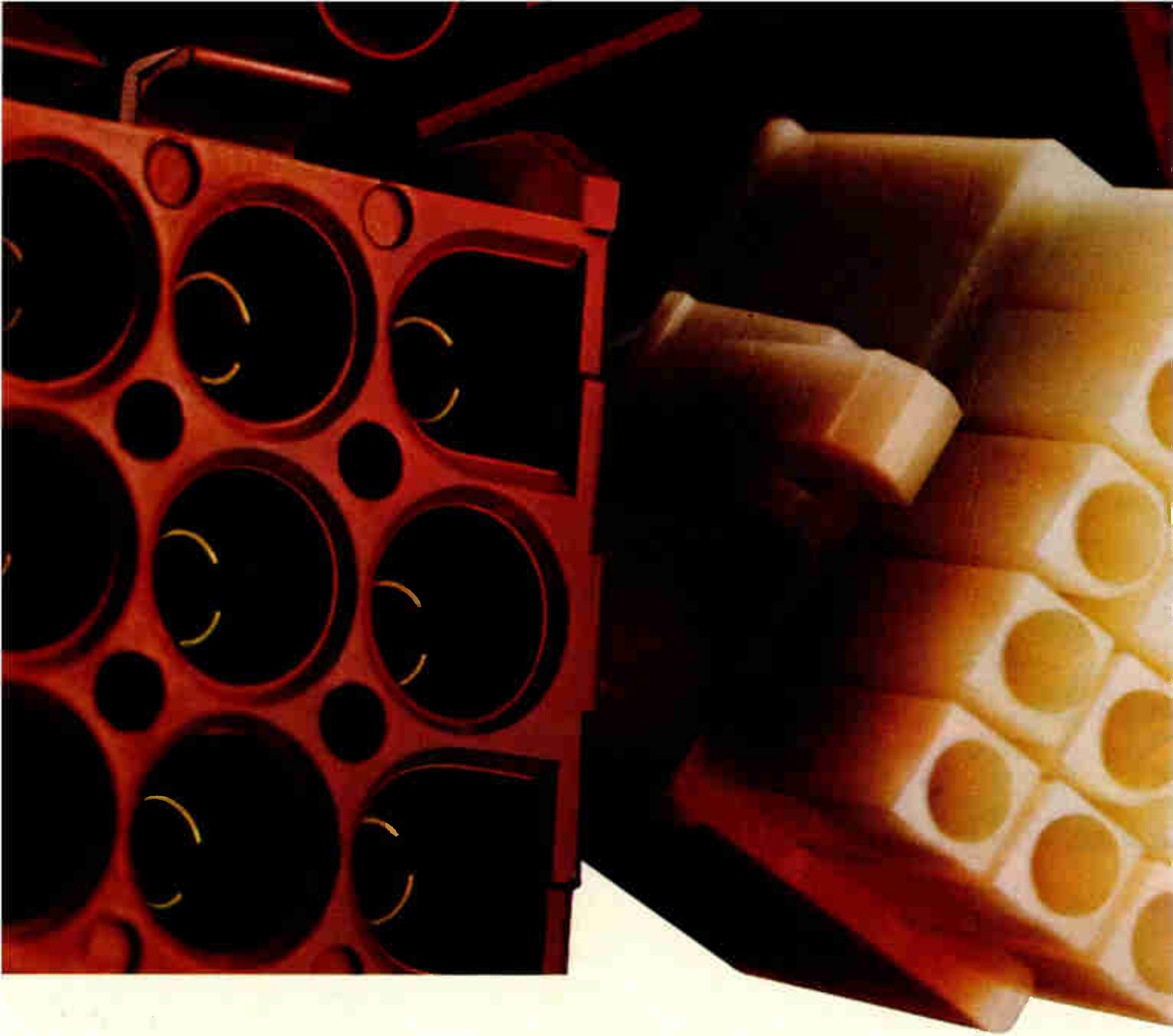
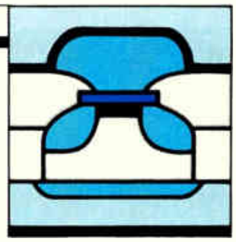


One good idea in safe-to-handle connectors deserves another. And another.



A NEW MEMORY TECHNOLOGY IS ABOUT TO HIT THE MARKET

Two startups are about to offer a new type of RAM, based on the ferroelectric effect, that will challenge nonvolatile memories by delivering speed and density as well as nonvolatility

A new kind of memory technology, exploiting the well-known but little-used ferroelectric effect, may be the key to the ideal memory device: nonvolatile, fast, dense, and radiation-hard. The technology is about to emerge in the form of products turned out by two startups: Ramtron Corp. of Colorado Springs, Colo., and Krysalis Corp. of Albuquerque, N. M. [*Electronics*, Feb. 4, 1988, p. 32]. The following two Technology to Watch articles delve into the Ramtron and Krysalis approaches to ferroelectric random-access memories.

Nonvolatility is inherent in ferroelectric memories, and if these new RAMs deliver the promised read/write speeds and long life, they could largely supplant erasable programmable read-only memories and electrically erasable PROMs, says Howard Z. Bogert, vice president of Dataquest, the San Jose, Calif., market research firm. Furthermore, he says, they could be a threat to dynamic RAMs. They are relatively simple—a 4-Mbit ferroelectric RAM could be built without trench capacitors, for example—and it is possible that further development could bring their cost and their read/write times down into DRAM territory.

All this is being claimed for devices built around the ferroelectric effect. Although the ferroelectric effect was discovered in 1921, it was poorly understood until the 1960s. Iron has nothing to do with the effect. The prefix "ferro" originated with early attempts to describe the phenomenon, which assumed that the ferromagnetic properties of some iron-bearing compounds were involved.

The ferroelectric effect is the tendency for certain crystalline materials to spontaneously polarize under the influence of an externally applied field and remain polarized after the field is removed. Reversal of the field causes spontaneous polarization in the opposite direction. So ferroelectric materials can be modeled as bistable capacitors with two distinct polarization voltage thresholds.

No external electric field or current is required for the ferroelectric material to remain polarized in either state, so a truly nonvolatile ferroelectric "digital memory capacitor" can be built for storing 1s and 0s. Data stored in a ferroelectric memory element can be read by sensing the interaction of an applied field with the element's polarization.

In practice, ferroelectric materials do not polarize instantaneously, and polarization thresholds are not perfectly defined. Most early ferroelectric research concentrated on finding materials with better characteristics. Those efforts were unsuccessful, but now Ramtron and Krysalis, working separately, say they have made the breakthroughs in materials, processing, and circuit design that will turn ferroelectrics into commercial reality.

FERROELECTRIC CAPACITORS ARE RAMTRON'S BRIGHT IDEA

They act as backups for SRAM cells, storing logic states when the power is interrupted

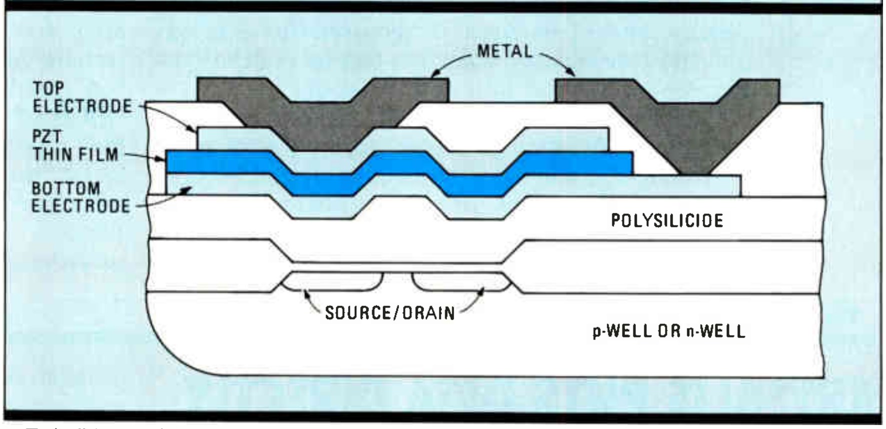
It took an all-out research-and-development effort in circuit design and semiconductor processing, as well as in materials, to make the breakthroughs required to manufacture practical ferroelectric devices, say researchers at Ramtron Corp. The Colorado Springs, Colo., startup has devised a static random-access memory that achieves nonvolatility by using backup ferroelectric capacitors to store logic states during power interruptions.

The result is what Ramtron calls a ferroelectronic RAM, or FRAM. Its first chip—a 256-bit nonvolatile static RAM—will be introduced at the Feb. 16-19 International Solid State Circuits Conference in San Francisco. It is the forerunner of a family of larger FRAM products, including 16- and 64-Kbit memories due out later this year and 256-Kbit devices slated for 1989.

"The FRAM is the world's first true nonvolatile read/write memory," says Richard Horton, Ramtron's director of business development. "The breakthrough technology is expected to have a ed, the transmission gates are turned on, connecting the ferroelectric capacitors to the cell inputs and polarizing them to the RAM cell state prior to power loss. Sufficient polarization for nonvolatile recovery occurs within 10 to 20 ns, well before the RAM loses its state or the power supply collapses. Once charged, the capacitors can retain their state almost indefinitely.

Recovery from power loss and return to active RAM mode are also direct. As power is applied, the capacitors strongly bias the inputs of the RAM cell to reflect the stored condition. Once fully powered, the transmission gates are opened, removing the ferroelectric capacitors from the circuit and leaving the RAM in the same data condition that it was in prior to power loss.

HOW RAMTRON BUILDS ITS FRAM



3. To build capacitors—the nonvolatile storage elements—on top of a silicon-gate MOS FET, Ramtron adds two electrodes with a PZT thin film in between.

The design eliminates the traditional problem of fatigue in ferroelectric memory, which until now has limited its use to about 10^{10} cycles. Most previous experimental designs relied on ferroelectronic polarization for every write cycle, making them impractical for the majority of main memory applications. In the FM801 and the first generation of commercial devices, an endurance cycle of 10^{10} is more than adequate, since ferroelectric polarization occurs only during power sequencing. This means that the FM801 has a life expectancy exceeding 27,000 years, even if a power loss occurs 10 times per day. And early test results suggest that lifetimes of 10^{15} cycles are possible. Longer endurance will allow ferroelectric storage to be built into the active memory circuit, replacing the dynamic capacitor storage used in DRAMs.

Virtually all of the FRAM's external characteristics are identical to those of standard SRAMs. Read and write cycles are symmetrical and as fast as a SRAM's: the FM801 has an access time of 70 ns, while the upcoming commercial parts will boast 20- to 40-ns speeds.

Like the FM801, these devices will also be based on the six-transistor SRAM topology, and will include 2-K-by-8-bit and and 8-K-by-8-bit configurations in standard Jedec packaging. They will be directly pin-compatible with current 5-V SRAMs and EEPROMs. For the next generation of 256-Kbit models, Ramtron is developing an optimized, merged technology eliminating redundant metallurgical steps. When the merged process is coupled with a one-transistor cell design, (see fig. 2b), FRAM manufacturing costs will approach those of DRAMs.

As with the circuit design, the FRAM fabrication process is simple and straightforward. The base circuitry of the FM801 is built using a conventional 3-μm silicon-gate CMOS ASIC process, with a single level of metal interconnection (see fig. 3). No process adjustments to the underlayers are reqired to add the ferrolectric process steps. Three process steps must be added to the base circuitry: two layers of metal for electrodes and a thin film of a ceramic lead zirconate titanate. The metal-PZT-metal sandwich produces what might be called a digital memory capacitor, which is the nonvolatile storage element. This is a new component for circuit design—Horton says it as fundamental as the field-effect transistor. Connection to the base circuitry is made using conventional metalization and vias to the underlayers.

The ferroelectronic layers can be added directly over active devices. The result is a true three-dimensional circuit, built vertically over standard semiconductor devices. Ramtron's ferroelectronic process is complementary to current semiconductor processes, including bipolar and CMOS silicon, as well as to gallium arsenide, silicon on insulator, and others. All of the physical and electrical features of the underlying circuitry are preserved, and no additional area is required. Further, logic compatibility can be programmed over a wide range by varying the PZT film thickness and metallurgy, making ferroelectronics largely independent of the substrate and underlying process.

The PZT material itself has highly desirable physical and electrical properties. Among them are high resistance, since its tight crystal lattice makes it an insulator; thermal and chemical stability, because it is almost unreactive chemically, and has a Curie—or phase-change temperature—exceeding 350°C; and because it has the hardness that is typical of ceramics. Ramtron's PZT remains nonvolatile from −180° to above +350°C, well beyond the operating temperature range of existing silicon circuits. And breakdown voltage of the PZT film is high; the film used for CMOS-logic compatibility easily withstands 40 V. In addition, it is highly resistant to radiation.

Another advantage of the PZT material is very high dielectric constant, which at 1,200 is roughly 300 times that of the dielectric used in exist-electric capacitors, which can be changed by an applied electric field to store digital data states.

Krysalis will not reveal details of its process or the ferroelectric material it uses. The firm will say only that the material is a perovskite crystallization structure that is a derivative of lead zirconate titanate, which is deposited using a method compatible with conventional semiconductor-processing techniques. The ferroelectric thin film will add about 5% to 10% to the cost per wafer of a standard 12-mask CMOS process, the company says. Currently, it takes three masks to form the ferroelectric cells, but later designs could need only one additional mask step to integrate the ferroelectric with the silicon, according to Krysalis.

The company's chips differ in some respects from Ramtron's initial parts. Whereas the Ramtron devices will rely on conventional six-transistor static-RAM silicon cells that are "shadowed" by nonvolatile ferroelectric memory, the Krysalis UniRAM line will use the ferroelectric as the primary storage element. "Our technology is a direct RAM, where every [write and access] cycle talks to the ferroelectric cell," says William Miller, vice president for process development. "Every time you write, you write to the ferroelectric memory, and therefore, it's always nonvolatile. You never have to worry about doing a store before a power down, or having to do a power-fail detect."

The approach also pays dividends in cost and density, Miller says. Instead of a six-transistor SRAM-type silicon cell plus the ferroelectric elements, the Krysalis cell contains only a single transistor and a single ferroelectric capacitor. The 16-Kbit products will employ a double-ended scheme requiring two cells, or four devices, per bit. But subsequent 64- and 256-Kbit UniRAM parts will use a different approach requiring only one cell per bit, further improving density, Miller says. Samples should be available in early 1989.

In the Krysalis 512-bit demonstration chip, the double-ended cell scheme creates a self-referencing signal differential across the sense amp (see fig. 2). The memory bit consists of a word line controlling two pass transistors, a bit line, a $\overline{\text{bit}}$ line to collect charge from the capacitors, and a common drive line to actively drive the capacitors. A sense amp resides between the bit line and the $\overline{\text{bit}}$ line.

For a write, the sense amp is set to the desired state, and the bit and $\overline{\text{bit}}$ lines are driven to the opposite voltage values of V_0 and ground. The drive line is pulsed in such a way that the high drive line against the grounded bit line writes the 0 state into its capacitor. When the drive line drops to ground after the pulse, the other capacitor has a 1 written in it by its high bit line voltage.

In the read operation, a voltage step is applied to the drive line with the bit lines floating and the sense amp off. Since the capacitors are in opposite states, the bit line and $\overline{\text{bit}}$ line will collect different amounts of charge and produce a voltage differential of a polarity determined by the stored data. The sense amp then turns on to capture the bit. With the sense amp on, the bit lines are driven to the opposite rails and the destructively read bit is automatically restored. The restore is invisible to the user and occurs in parallel with the output gating of the read data to the input/output ports.

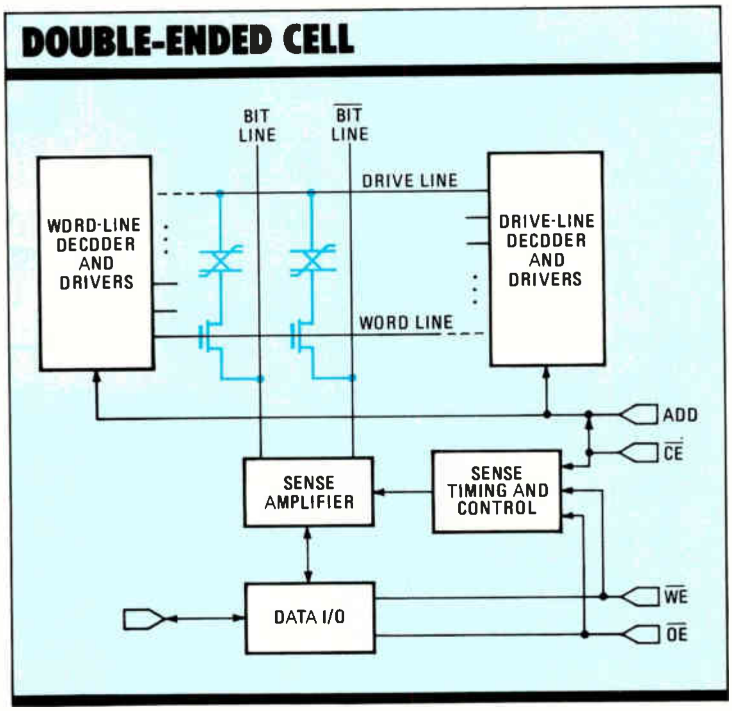
The memory array in the 512-bit part is arranged as 64 rows of 8 bits apiece with no column decode. One row consists of 16 capacitors sharing a common word line and drive line and arranged as eight double-ended memory bits. The part also includes on-board test circuitry.

Its capacitors measure approximately 5 µm by 9 µm, are less than 1 µm thick, and have nominal capacitance of 1 picofarad apiece. The drive-line and word-line drivers are located on either side of the memory array. Regenerative feedback amplifiers similar to those in DRAMs constitute the sense amps. The device has standard three-state I/O functions.

Buffered inputs control the word line, drive line, sense amp, and equalization functions. In combination with the I/O controls, the device requires seven timing inputs, a setup designed to allow experimentation with timing algorithms. However, the Krysalis 16-Kbit parts will be offered with standard SRAM three-line control.

Likewise, the 512-bit part requires both a 5-V power supply and a second 7.5-to-10-V supply. But the commercial 16-Kbit parts will operate on a single 5-V supply. *–Wesley R. Iversen*

For more information, circle 481 on the reader service card.



2. Early Krysalis chips will use a double-ended, two-cell scheme with four devices per bit; later versions will have one transistor and capacitor per cell.

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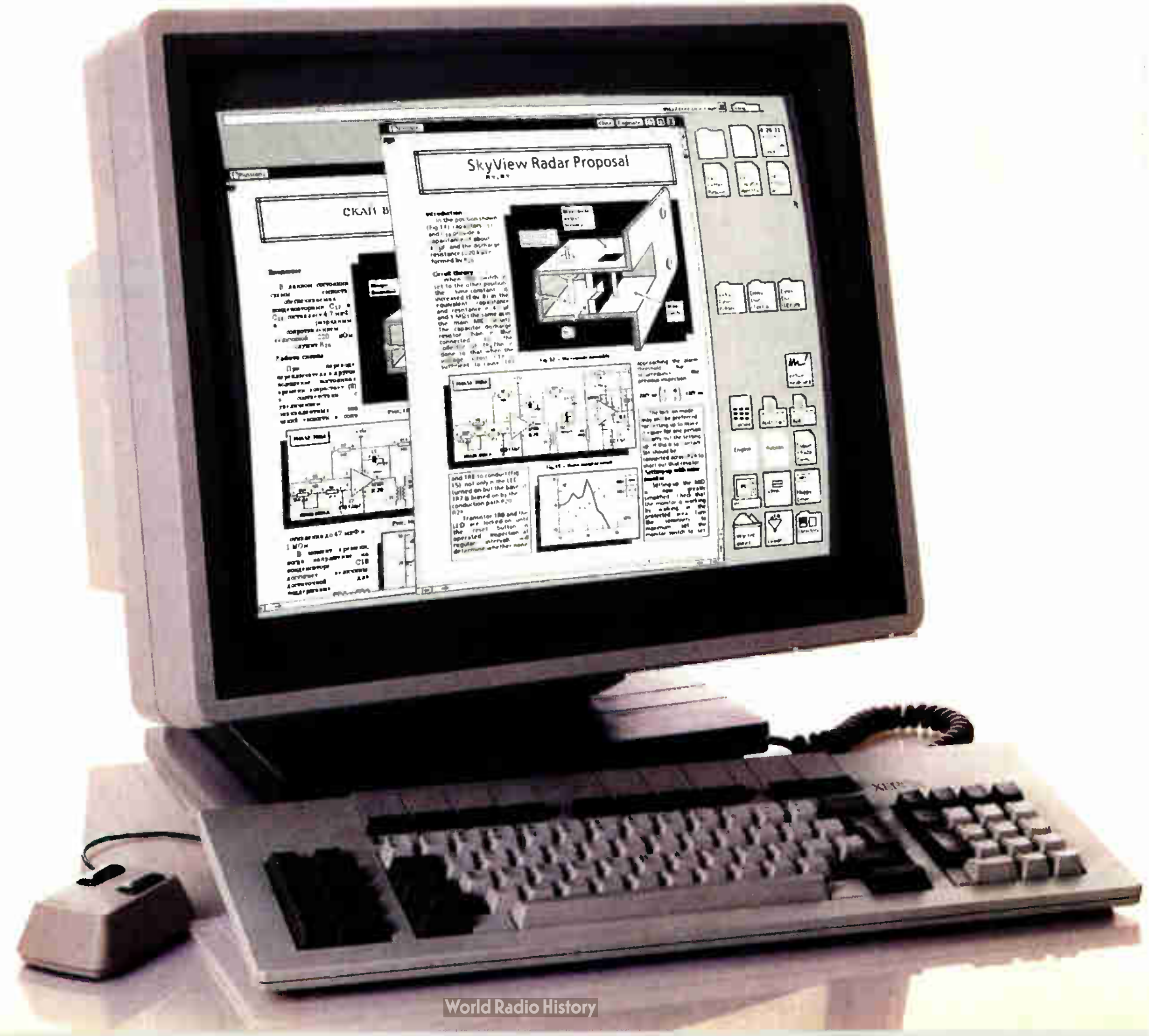

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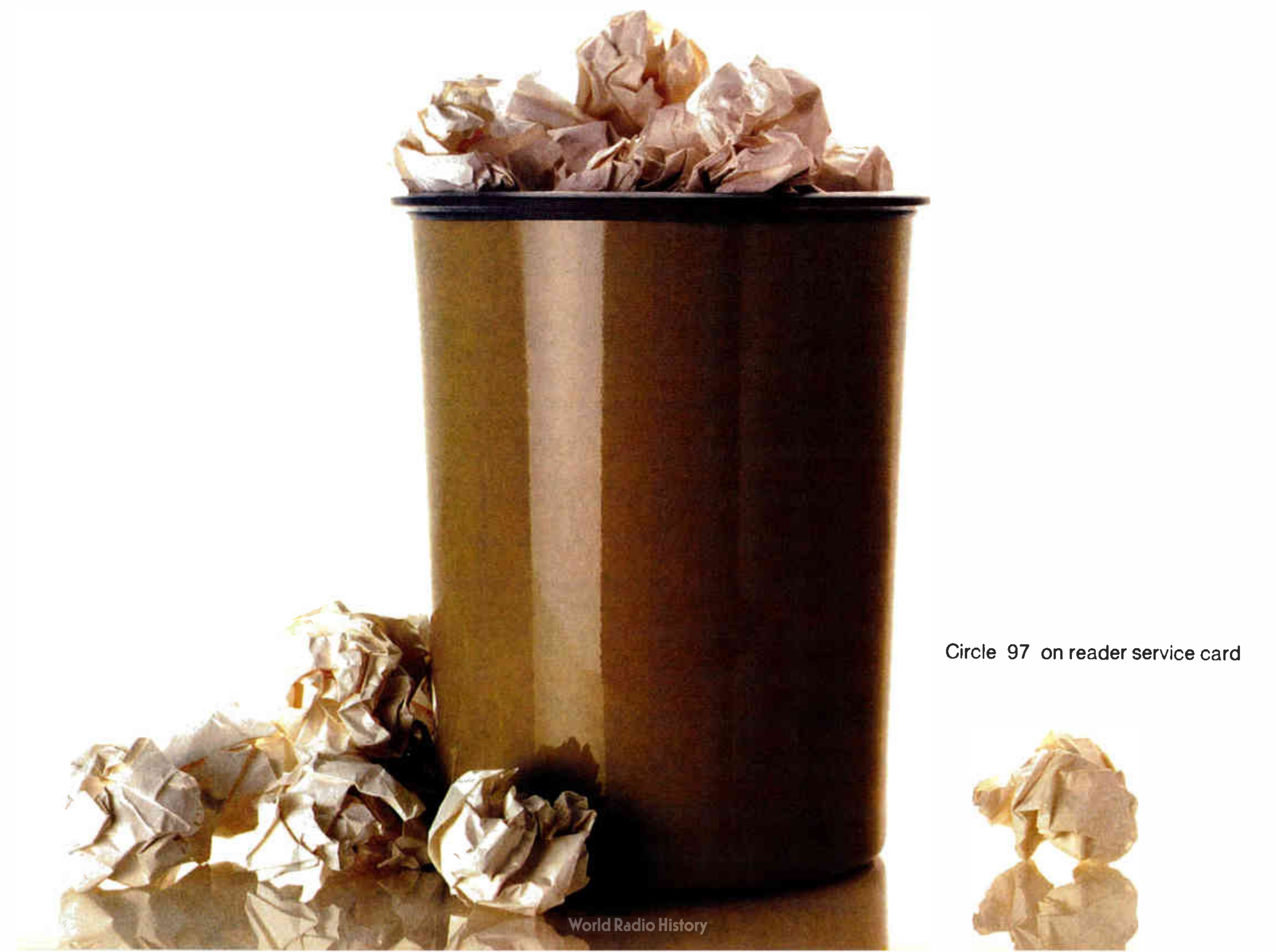


Circle 97 on reader service card

ALTERA'S SPEEDY WAY TO TAILOR ADD-ONS TO IBM'S PS/2

Its newest EPLD gives board makers a working interface to the PS/2's bus, cutting time to market and saving board space; when used with a companion DMA chip, it replaces 18 components

by J. Robert Lineback

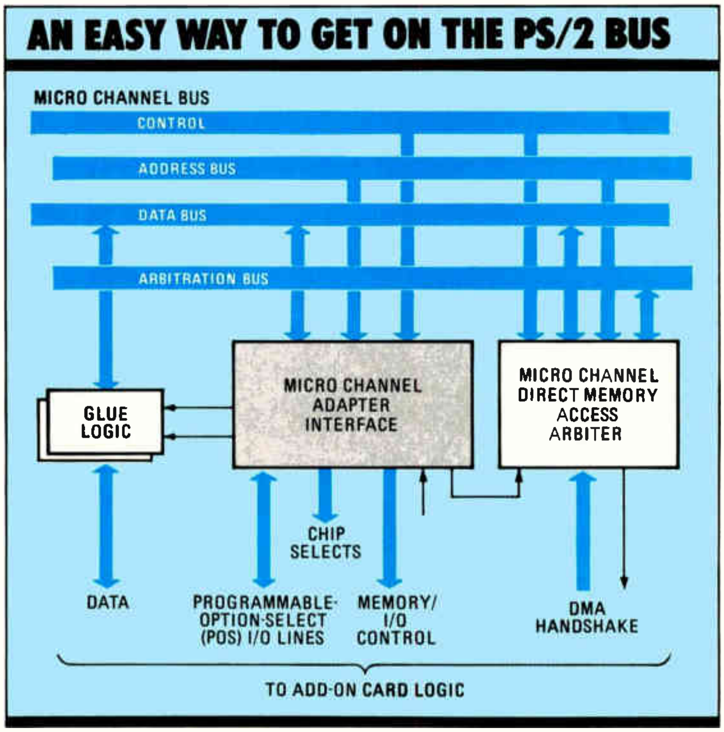
Add-on board suppliers will soon get an all-in-one programmable interface chip that will help them quickly enter the potentially huge market for plug-in peripheral cards serving IBM Corp.'s Personal System/2 and its widely expected clones. Altera Corp. is launching the industry's first erasable programmable logic device aimed at providing a complete interface to the IBM Micro Channel bus. Not only will the new CMOS EPLD save time in turning out the add-on boards, but it will save board space as well. Accompanying development software will cut the time to market even more, and vendors will be able to put their add-on PS/2 interface functions into four reserved programmable spaces on the EPLD.

The newest function-specific chip from the Santa Clara, Calif., company gives board vendors a working interface (see fig. 1) to the Micro Channel for any of a range of peripheral cards, including tape and disk controllers, communication links, special graphics capabilities, data acquisition, and multifunction plug-in cards. Compared with existing nonprogrammable Micro Channel chip sets and emerging mask-programmable semicustom interfaces, the EPB2001 should dramatically reduce the board space required to meet IBM's complex new logic and timing specifications.

Initial shipments of the software, the 2001 EPLD interface chip, and a companion 28-pin direct-memory-access arbiter are slated for the second quarter. The 2002 arbiter chip is Altera's first nonconfigurable integrated circuit; the firm opted to leave the DMA's functions off the 2001 because about half of the anticipated applications will not require such features. Volume production of both chips will start in the second half of 1988. In 10,000-piece quantities, the 2001 interface device will cost less than $12 each, says David A. Laws, vice president of marketing at Altera, and the 2002 will go for $5.

The Altera package is after a big market. About 400,000 PS/2s equipped with Micro Channel were shipped last year and another 800,000 should be sold by the end of 1988, Laws estimates. On average, each Micro Channel-based PS/2 will get three plug-in cards within 18 months, Altera estimates.

And because of the EPLD, the company thinks, many of these PS/2 users will have additional, cost-effective options available to them. "With our user-configurable interface, add-on board manufacturers can quickly prepare prototypes or launch small-to-medium-volume products without taking on the expense of custom circuits," says Laws, who notes that the PS/2 plug-in boards are about 40% smaller than the cards for IBM's Personal Computer AT and compatible PC models. "The cost of custom circuits [to reduce the Micro Channel interface logic or the peripheral function's own logic] could keep some startups from getting start-



1. Altera's new EPLD and some glue logic are all that are required to get on the Micro Channel bus. The DMA chip is optional.

brary. This contrasts sharply with other systems, which restrict block placement. Some will only place large blocks in the corners of the layout. Others will not allow the use of oddly configured blocks, such as L-shapes, U-shapes, and C-shapes, but will accept only rectangular blocks. In addition, some other systems place blocks only roughly, so that the designer must correct the placement before a router connects the blocks.

Chip Crafter not only provides complete freedom in placing large blocks of cells, but also provides greater latitude in what goes into the blocks

Besides more flexibility in placing blocks, ChipCrafter provides greater latitude in what goes into the block. When a design calls for using standard and megacells in the same layout, ChipCrafter need not simply gather standard cells into one or more large blocks, as other systems do. It can leave the standard cells as a single block or divide them into multiple blocks as needed to create the most efficient floorplan. The system therefore can sprinkle them in whatever open spaces exist between blocks, on the basis of connectivity and the most efficient placement.

ChipCrafter lays out in two passes. During the first, it determines optimum placement for blocks and standard cells, given the interconnection list and the size and shape of the blocks. It then routes the blocks and cells. The system also calculates the number of outputs any one gate will drive (fanout) and the load the fanout places on the gate's output driver stage. To get the best performance, ARAR+ matches the outputs of individual blocks to the length of line at each output and the load at the end of each line.

During its second pass, ChipCrafter takes information attained in the first pass and makes the transistors inside all of the nonrectangular blocks and standard cells larger or smaller, to match the loading and fanout conditions derived in the first pass (see photos, p. 101). Of course, when the size of the transistors inside a block is changed, the blocks change in size and shape, too. So the system performs a second place and route, readjusting the layout to accommodate the changes. "No other layout tool available can dynamically resize transistors inside a large block," Morrell says. *–Jonah McLeod*

For more information, circle 483 on the reader service card.

TECHNOLOGY TO WATCH **CAD/CAE**

CATCHING GLITCHES AND DELAYS IN DENSE ASIC DESIGNS

SMOS Systems uses expert-system technology to find and display bugs, cutting a week off design cycles

A new generation of design tools from SMOS Systems Inc. will make it much easier to get rid of harmful glitches and cut down timing delays in application-specific integrated circuits. Both glitches and timing delays have become far more serious problems as ASICs move toward 1.2-μm or finer geometries and clock rates grow faster. Glitches, or noise pulses, can upset complex logic designs and cause system failure. Timing delays can disrupt the chip's operation, and trying to avoid them on a dense chip makes component placement in a design a nightmare for designers.

The LADDS 5.00 series E—an upgrade of the San Jose, Calif., company's LADDS 5.00 series D set of design tools—automatically finds glitches and delays in signal paths that can prevent a gate from functioning. It also contains a place-and-route-tool that, operating automatically after a single pushbutton command, produces a layout that is completely routed with its timing corrected.

The software runs on IBM Corp. PCs and compatibles, Digital Equipment Corp. MicroVAXes, and Intergraph work stations. Available now, it is provided at no charge to a designer with an SMOS foundry service contract. The tools work with SMOS's CMOS processes only—the company is a high-volume foundry which typically contracts for a minimum order of 10,000 devices per month using gate arrays and standard cells.

To guard against glitches, the series E simulator uses expert system technology. It finds those glitches that might produce an error—all others are ignored—and presents them to the designer on a display. The designer then determines which errors need to be removed and which can be ignored.

With the glitches eliminated, the designer can evaluate the functioning of his logic design without having to debug it. After debugging, the designer performs another simulation, and the simulator shows the designer what his circuit does with noise pulses propagating through the design.

Working with densities of 2-μm or more in CMOS, the designer could usually catch all these glitches unaided. "The larger-geometry CMOS processes were very forgiving, so the number of glitches that had to be debugged during simulation was relatively small," says John Conover, director of engineering. "With the advent of 1.5-μm and smaller-geometry CMOS, the problem has become too complex to be done effectively without the simulator."

And the simulator needs expert-system technology to work effectively. When it's simulating a circuit implemented in fast process technologies, the simulator produces a file containing a huge number of detected glitches. "A glitch file can have several megabytes of data," Conover says. Without a smart simulator, the designer must wade through the file line by line, examining each glitch to determine its effect on circuit operation.

By contrast, the expert system in the SMOS simulator compares the debugged model of the circuit with the model containing the detected glitches. It then performs the line-by-line analysis and presents to the designer those glitches which are most likely to affect circuit operation. The expert-system software will err in favor of catching too many errors, rather than leaving a catastrophic error in the design. But the designer makes the determination of which glitches are significant. "This software aid will cut from one to two weeks out of a design cycle," says Conover.

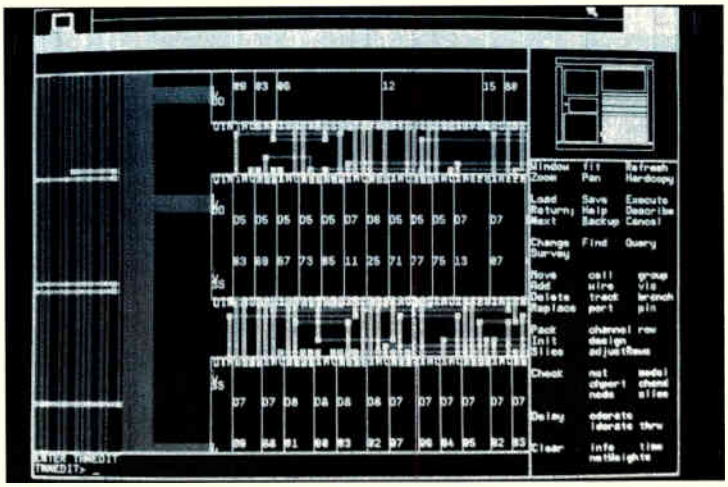
There are two ways for the designer to work with the simulator. One is interactively: the designer gets a display on the design system's cathode-ray tube. On encountering a glitch, the system highlights the error on the display (see photo) and asks the designer whether to ignore or to propagate it. In interactive mode, to aid in evaluating the glitches it has culled, the simulator allows the designer to examine a single glitch at a time (or any other number desired) and propagate it backward or forward through the system. The process repeats for all the glitches culled by the expert system. If the glitch is propagated, each error produced by the propagated glitch is highlighted for the designer to evaluate. He can evaluate each glitch individually without confusing one with another.

The simulator also operates in batch mode. "Most designers prefer to run the entire simulation at once, with no interaction," Conover explains. "At the end of the run, the simulator creates a file containing the significant glitches. The designer then refers back to his schematic to evaluate the impact of each of these glitches."

With the glitches detected and, where necessary, eliminated, the designer can start to work cutting down timing delays, by evaluating set-up-and-hold violations. In 2-μm process technologies, the difference in arrival time for two pulses at the input of a gate due to timing delays in the lines leading up to the gate was insignificant. Now, with faster 1.2-μm CMOS, the difference in delays can produce meaningful errors. The gate delay—amount of time required for a pulse to pass through a gate—is 1.29 ns for 2-μm CMOS; the gate delay for 1.2-μm CMOS is 0.53 ns.

If he has to do the job by hand, the designer must trace a signal through the circuit and add and subtract delays in the data path of one or both signals to ensure the D input reaches the flip-flop at the right time relative to the clock input. The process is repeated for all the flip-flops which have a set-up-and-hold violation.

"With the expert system capability added to the tool, this function occurs automatically," Conover says. "The tool alerts the designer if the time relationship between the D-input and clock of a flip-flop is inadequate. It specifies the faulty flip-flop and when the set-up-and-hold violation occurs." The designer corrects all the set and hold violations as well as all the glitches, performs a logic simulation, and then passes the file to the place-and-route tool for automatic layout.



PLACEMENT. SMOS's system places cells relative to one another to conform to design timing specs and to eliminate glitches.

In the faster CMOS process technology, wire length becomes a contributing factor to violations of set-and-hold-times as well as other timing anomalies. A typical place-and-route tool in an ASIC design tool kit lays out a debugged schematic it receives from the front-end design system. Then it sends the design simulator a netlist containing the circuit timing resulting from the layout. If the timing simulation shows that the layout altered the circuit, the designer must adjust the layout to eliminate the problem. The LADDS place-and-route tool differs from this approach in that it is a timing-driven layout system. Before any layout is undertaken, it looks at the simulation from the front end system to determine the timing constraints. It then makes a layout that meets these constraints.

In creating a layout, the system assigns 2 mm of aluminum for each interconnection on the chip. "On a chip with 30,000 gates, the 2-mm figure is a good, conservative number," Conover says. "There are not likely to be many wires that long in a chip layout. If the circuit works with this conservative wire length, it will work in any condition in the circuit." The layout system knows, in effect, that in some instances it must create a wire length longer than 2 mm. If it must make placements which exceed the simulated 2-mm length, the system determines if the longer wire violates the timing specification of the device. If it does, then the tool alters the placement to shorten this wirelength to an acceptable length. *–Jonah McLeod*

For more information, circle 484 on the reader service card.

deliver a paper on achieving accurate placement of fine-pitch surface-mount devices through measurement and feedback at the time of placement. The paper describes a new system in which four video cameras measure the placement error at each of the four corners of a fine-pitch package. The four views are displayed simultaneously on a monitor to the operator, who can then adjust the position of the machine's placement table to reduce the alignment error. Drislane notes that SR Technologies is currently developing a next-generation system using machine vision to close the adjustment loop—in other words, it will correct alignment errors automatically. This system is applicable to gull-wing and flat-pack package types, as well as leadless ceramic carriers.

A real-world application of a modified SR Technologies semi-automatic system is dicussed in the session's closing paper. Donald R. Mullen of the Evans & Sutherland Computer Division, Mountain View, Calif., tells how the system is used for surface-mount placement and soldering of a square gull-wing package measuring 2 ½ in. on a side. The package has 340 leads on 25-mil centers.

Thus, surface-mount packages with very high lead counts are clearly headed for practical commercial use. So too is a whole new family of oddly shaped molded thermoplastic pc boards. A raft of real-world applications of this technology are described in a standout Nepcon session on the commercial applications of production facilities for 3-d molded pc boards.

A paper from Xetec Corp., Salinas, Kan., for example, describes the use of 3-d molded board technology (furnished by DuPont) in solid-state ballasts for fluorescent lighting. Another paper, from Smith-Corona Corp., Cortland, N. Y., discusses the use of technology from Pathtek Inc., Rochester, N. Y., for constructing molded boards for a light-emitting-diode assembly used in an electronic typewriter. The approach is said to result in substantial savings in parts, labor, and tooling.

Two papers from the ICI Electronics Group an operating company of ICI America, Wilmington, Del., cover 3-d molded boards for brushless motors and a connector for a telecommunications application. In one of the papers, John Williams and John Haffey of ICI discuss the review process of the requirements for two brushless-motor circuit boards for two different customers. One of the resulting molded-plastic boards is a circular one for a disk-drive motor; the second is a shaped board that replaces a more expensive flexible circuit.

A second paper by Sean McKinley of ICI and Gary Nault of ADC Telecommunications Inc., Minneapolis, talks about the requirements and the fabrication of a four-wire patch plug for testing the main boards of telephone exchanges. ADC formerly used a version of this plug made of FR-4 glass-epoxy material. This unit had poor reliability, a short life, and problems with frequent breakage. The 3-d board, thanks to the ruggedness of ICI's polyethersulfone (Victrex) plastic, increased reliability and board life by at least a factor of three, according to the paper's authors. Furthermore, it cut costs by eliminating the need for a separate connector—a connector is an integral part of the molded pc-board assembly.

As board-manufacturing and packaging technologies advance, new problems must be solved by test and inspection engineers. One Nepcon session on inspection and another on test show how some of these challenges are being tackled.

Nepcon will also hear about a raft of new test and inspection solutions

The inspection session features papers by Nicolet Test Instrument Division, Madison, Wisc., and IRT Corp., San Diego, on X-ray techniques for inspecting assembled pc boards. "Electrical testing often gives only half the story for boards loaded with certain types of packages," says the chairman of the inspection session, Edward Soron of IRT. Pin-grid-array packages and leadless chip carriers have many solder joints that are can't be inspected, for example, and plastic leaded chip carriers with J-leads bent under the body of the carrier are extremely difficult to inspect.

The only way to find out whether the barrel of a hollow PGA socket pin on a pc board is full of solder is by using transmissive X-ray techniques, says Soron. The same radiography technique is needed to check the solder fillets of leadless ceramic chip carriers.

Trace Instruments, a division of Methode Electronics Inc., Canoga Park, Calif., covers a problem testing area peculiar to today's high density, fine-line pc boards—board damage caused by testing.

The effects of various stimulus voltage and current levels on fine-line bare boards, hybrids, and substrates are examined in a paper given by George Hroundas of Trace Instruments. Strict control of these parameters is vital if testing is not to degrade or destroy board interconnections. The way test stimulus voltage affects both conductor integrity and isolation resistance is explored along with the cost consequences of less-than-optimum testing strategies and parameters. □

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MILITARY/AEROSPACE NEWSLETTER

SURPRISE! GE BEATS OUT IBM TO DEVELOP SUBMARINE COMBAT SYSTEM

In a surprising development, General Electric Co. beat out IBM Corp. for a much-coveted contract to develop the combat system for the Sea Wolf, the Navy's next-generation attack-class submarine. The decision was a major disappointment for IBM, which is the prime contractor for the AN/BSY-1 combat system on the current generation of attack-class subs [*Electronics*, Nov. 26, 1987, p. 148]. The BSY-2 contract is particularly valuable because of the long design cycle involved—the first Sea Wolf won't be launched before the year 2000. Moreover, BSY-2 had been a major focus of IBM's work in its Very High Speed Integrated Circuit program. Development of a set of four chips designed for an advanced sonar system was a key part of the company's effort in VHSIC's second phase [see story, pg. 37]. The award to GE of an initial $13.6 million contract to guide BSY-2 from the design definition phase into full-scale engineering and development won't leave IBM out in the cold, however. An IBM spokesman says the company expects to join GE and its teammates, Computer Sciences Corp., Martin Marietta Corp., and Singer Co., in a follow-up role later this year. □

THE ARMY WANTS TO MOVE TECHNOLOGY FASTER INTO MILITARY SYSTEMS . . .

The Army Science Board is worried that new technologies aren't finding their way into Army systems fast enough, so it is sponsoring a six-month study on how to speed up the process. The board has charged an 18-member panel with producing a set of recommendations by July and a final report for public release by October. The group, which will be chaired by Paul W. Kruse Jr., chief research fellow at Honeywell Inc., Bloomington, Minn., will meet for the first time late this month to try to focus its attention on a few vital technologies. It is expected to zero in on the Defense Department's Very High Speed Integrated Circuit program. Developed to advance military electronics, VHSIC chips have yet to find wide application in military systems. □

. . . AND CUT THE SPIRALING COSTS OF TESTING

Testing procedures for military components and systems have been criticized for years for everything from being too easy to too expensive. The problems have sparked the Army Science Board to order a study on testing strategy. A science board panel will report this summer on "how we go about testing components and systems," says Col. Richard E. Entlich, the board's executive secretary. The panel will analyze testing procedures and make recommendations on more cost-effective testing. "Sometimes we actually overtest," he says, adding that the Army can't afford that luxury. □

VARIAN IMPROVING TEST GEAR TO BOOST YIELDS ON GaAs DIODES

Varian Associates Inc., Palo Alto, Calif., is developing manufacturing techniques for Gunn and varactor diodes that it says will boost yield by a factor of three. The diode chips are key components in the Army's Sense and Destroy Armor munitions program, and Varian is supplying them to both Honeywell Inc. and Aerojet Electro Systems Co. The challenge is that the parts are so small—8 to 10 $mils^2$—and the specifications so tight that imprecise positioning during such manufacturing steps as wire-bonding and radio-frequency testing can cause perfectly good parts to fail, says Michael Kopec, sales manager for Varian's III-V Device Center. In addition, GaAs chips are brittle and break easily during testing. The company is taking basic equipment and "optimizing the positioning systems so they don't smash the chips into oblivion," Kopec says. He expects the new equipment will help Varian push overall yield of qualified wafers into the 50% to 70% range. □

NEW PRODUCTS

HP HALVES THE COST OF INSTRUMENTS THAT TEST FREQUENCY-HOPPING RADIOS

THE 8645A IS A ONE-BOX ANSWER TO WHAT HAS BEEN A CUSTOMIZED SETUP

Makers of frequency-hopping radios for military and other security-oriented applications now have a single instrument that simultaneously evaluates both the radio's hopping and its transmission performance—and does so at less than half the cost of a customized solution.

Since frequency-hopping-radio technology is a relatively recent development, the appearance of Hewlett-Packard Co.'s HP8645A saves users from custom-designing a test setup that would—for starters—include a frequency-hopping local oscillator costing between $15,000 and $80,000, plus an FM modulator, which can run between $15,000 and $30,000. By contrast, the HP8645A costs $32,000.

PERFORMER. HP's 8645A operates from 250 kHz to 2.06 GHz and can change frequency every 15 μs with an accuracy of 1 Hz per MHz.

RF SIMULATOR. The 8645A can also simulate a complex rf environment for users who want to test receivers for susceptibility to interference. The instrument is equipped to test the fastest receivers. It operates over a frequency range of 250 kHz to 2.06 GHz and can change frequency every 15 μs with an accuracy of 1 Hz per MHz.

Extending the range down to 8 MHz increases switching speed to 85 μs. Below 8 MHz, the switching speed is 500 μs. Users can enter up to 2,400 unique frequencies and sequence through 4,000 frequency settings.

Frequency-hopping radios are becoming increasingly important aspects of communications technology across all branches of the military. Analysts peg the market for secure communications at $2.6 billion in 1986 and see it soaring to $7.5 billion by 1992, HP says.

Part of the reason for this anticipated boom is that advanced frequency-hopping radios have been developed in programs such as the U.S. Sincgars (for single-channel, group-to-air radio system) program, which created a backpack-portable radio for the infantry. It is expected to account for the production of several hundred thousand units. In addition, the Department of Defense's Jtids (for joint tactical information system) program has produced a larger transportable unit for mobile command posts and ships.

HP's 8645A offers a wide, versatile set of test functions while producing high-fidelity signals at precise frequencies. When measuring in-channel distortion, sensitivity, and hum and noise, for example, it delivers simultaneous fm, am, and pulse modulation with less than 2 Hz of residual fm. Signals with less noise and lower residual fm offer less interference in the measurement, reducing measurement uncertainty on radios being tested. FM distortion is 1% and output level accuracy is ±1 dB for measurements down to –120 dBm.

The instrument can be modulated with an internal audio source that produces 10 Hz to 400 kHz signals. When wider bandwidths for modulating are required, it can use external sources ranging as high as 10 MHz. In fast-hopping mode, the maximum deviation is ±4 MHz. For measuring adjacent channel specifications such as selectivity and spurious response, the HP8645A has specified phase noise to –129 dBc at offsets of 20 kHz or greater. Spurious noise is 100 dB or more below the level of the carrier.

To test frequency-hopping and surveillance receivers, the signal generator can be synchronized either with a transmitter or directly to the receiver under test. Key receiver parameters such as hop rate, dwell time, amplitude, and frequency can be controlled precisely. Each amplitude setting can be set with ±1 dB accuracy.

The receiver's susceptibility to jamming can be tested by adjusting the amplitude of the signal generator's output. This feature allows the 8645A to effectively emulate a "follower jammer," which is a jamming device that locks onto and follows the frequency of the transmitted signal with a jamming signal.

Available now, the 8645A is delivered 10 weeks after order. – *Jonah McLeod*

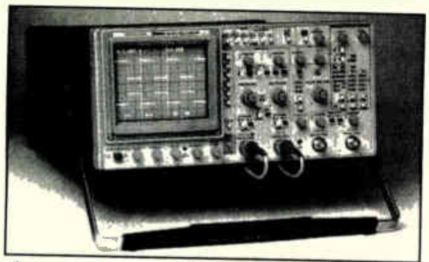
Hewlett-Packard Co. Customer Information Center, 19310 Pruneridge Ave., Cupertino, Calif., 95014 [Circle 380]

PC-BASED EPLD TOOLS TARGET CMOS ONLY AND COST $1,000

By using personal computers as a platform and aiming solely at CMOS devices, Pistohl Electronics Tool Co. has come up with a development system for programmable, erasable logic devices that costs just $1,000. The system includes a logic assembler with an embedded 50-rule expert system, and its hardware can switch each of its 38 input/output lines on the fly without creating glitches in programming.

Tailoring the PET100 family family for CMOS chips avoided the costs involved in building systems that are to be used developing bipolar chips. Such systems generally require three voltage levels and special features to sense outputs signals, says Howard W. Johnson, the two-year-old-company's founder.

The Cupertino, Calif., company also took advantage of the personal-computer explosion by making the tools run on



changes in voltage, trigger, and ground level for the wave form. It also stores up to 20 test setups and recalls them to the screen at the press of a button. Both scopes provide four channels, two of which are optimized for logic.

The 2245A costs $1,795 and the 2264A costs $2,395. Both of the models are available now.

Tektronix Inc., Portable Instruments Div., P.O. Box 1700, Beaverton, Ore., 97007.
Phone (800) TEK-WIDE [Circle 385]

PS/2 EXTENDER BOARD SPEEDS DEVELOPMENT

Tiara Computer Systems Inc.'s extender board lets hardware designers shorten development time for add-ons to IBM Corp.'s Personal System/2 computers, by allowing the prototype board to be removed from the computer housing for easy probe access.

The board features Micro Channel compatibility, four-layer pc-board noise immunity, shunts on +5-, +12-, and –12-V power lines, and over 21 sq. in. of prototyping area. All Micro Channel signals are available on header posts, each labeled according to its pin number on the connector. A logic ground reference is provided through a bus bar along the connector.

Available now, the PS/2 Extender costs $225.

Tiara Computer Systems Inc., 2700 Garcia Ave., Mountain View, Calif., 94043.
Phone (415) 965-1700 [Circle 389]

MEMORY TESTER RUNS UP TO 200 MHz

The T5481 memory tester from Advantest handles speeds up to 200-MHz VLSI memories and comes with two test heads.

The Advanced General-Purpose head provides 100-MHz testing capability. The Advanced ELC head can be used in multiplexed mode to test up to 200 MHz. The general-purpose head offers 2-ns output transition time at 3 V and 4.5-ns minimum pulse width over the full test clock range.

The ECL head boasts 0.5-ns output time and comparable pulse-width specifications. A wafer prober and autohandler interface are available options.

Up to 16 devices can be tested simultaneously with two test heads, and the system can handle up to eight 4-Mbit-by 1-bit dynamic random-access memories and static RAMs with 4- to 8-bit width at one time.

The T5481 is available now.

Advantest Inc., 300 Knightsbridge Pkwy., Lincolnshire, Ill., 60069.
Phone (312) 634-2552 [Circle 386]

80C86/80C88 EMULATORS OPERATE IN REAL TIME

Real-time, zero-wait-state emulation for the 16-bit 80C86 and 80C88 microprocessors sold by Intel Corp. and Harris Semiconductor Inc. is available for clock speeds of 8 MHz in the ES 1800 emulator from Applied Microsystems Corp.

The new emulator also includes a proprietary event monitor that provides powerful state-machine capabilities for triggering, breakpoint, and emulation control.

Options offered include a high-level language debugger and a software debugger. Both of these packages run on an IBM Corp. Personal Computer XT and AT or compatible machines. With them, engineers can debug in several high-level languages, among them C, Pascal, PL/M, Fortran, or Jovial.

The emulator also includes a Small Computer Systems Interface that allows data-transfer rates of 300 Kbytes/s.

Available now, the ES 1800 80C86/80C88 emulator costs $11,495.

Applied Microsystems Corp., 5020 148th Ave., NE, Redmond, Wash., 98073.
Phone (206) 882-2000 [Circle 387]

CAD TOOLS TARGET MIMIC DESIGNS

A set of microwave-circuit design-automation tools jointly developed by Ecad Inc. and Compact Software Corp., Patterson, N. J., provide designers with a means of drastically reducing design times for the Department of Defense's Mimic (Microwave Millimeter Wave IC) program.

Present microwave designs require manually interfacing and checking each step of a design. MiSym automates these functions.

The MiSym package includes tools for every stage of Mimic circuit design from schematic capture through physical layout. It also offers a direct interface to other microwave-simulation packages and incorporates a common user interface across all its packages.

MiSym is available now for Digital Equipment Corp.'s MicroVAX computers as well as Apollo Computer Co. and Sun Microsystems Inc. work stations. Pricing depends on the platform chosen.

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ELECTRONICS WEEK

2ND $1 BILLION MONTH FOR U. S. CHIP ORDERS

The Semiconductor Industry Association says U. S. chip demand is holding steady and strong. The January book-to-bill ratio stayed even with December's at 1.13, and bookings crossed the $1 billion mark for the second straight month—the first time the SIA has recorded back-to-back billion-dollar months since 1984. But the news wasn't all good: bookings slipped 2.9% to $1.006 billion and billings suffered a 12.2% drop to $850.7 million. The slight downturn casts some doubt about the semiconductor industry's high hopes for 1988.

CDC SETTLES ON ONE UNIX VERSION . . .

Control Data Corp. says it will be the first computer vendor to offer one version of Unix for everything from desk-top work stations to supercomputers. The Minneapolis company will begin offering a version of Unix System V that is compatible with Posix, the forthcoming portable operating system interface standard [*Electronics*, Feb. 4, 1988, p. 31], on its Cyber Series work stations and mainframes by the second half of next year. It will be the same version scheduled for release in the third quarter of 1988 on the family of ETA[10] supercomputers, which are built by ETA Systems Inc., a subsidiary based in St. Paul, Minn.

. . . AND BEGINS WORK ON 100-Mbyte/s NET

Control Data Corp. will develop a high-speed fiber-optic communications link for its Cyber mainframe computers under an agreement with Fibronics International Inc. The agreement calls for Control Data to design an intelligent peripheral interface that will let its Cyber computers communicate over Fibronics's 100-Mbyte/s System Finex network. Finex is the Hyannis, Mass., company's implementation of the Fiber-optic Distributed Data Interface, or FDDI network standard.

FEDERMAN BECOMES VENTURE CAPITALIST

Irwin Federman is following a host of other Silicon Valley executives into the venture capital business. The former president of Monolithic Memories Inc. and current vice-chairman of Advanced Micro Devices Inc. is joining Dillon Read & Co. as managing director of the firm's Concord Partners office in Palo Alto, Calif.. But he's not quitting his post at AMD. W. J. Sanders III, AMD's chairman, says Federman will continue to chart AMD's "strategic and tactical directions."

JUDGE REFUSES TO DROP Z80 CASE

Zilog Inc. is claiming a key legal victory in a judge's refusal to dismiss its case against NEC Corp. In its action, Zilog seeks rescission of a 1983 pact that settled earlier infringement claims against the Tokyo company by swapping Z80 rights for NEC's V series of microprocessors. Zilog officials in Campbell, Calif., want to nullify the pact because NEC was later sued by Intel Corp., which claims the V series violates its microcode rights. While the Intel-NEC battle continues, Zilog has opted not to ship any V series parts. No date has been set for Zilog's case in the U. S. District Court for the Northern District of California.

APPLE SHIPS ITS UNIX FOR MAC II

A version of the Unix operating system that Apple Computer Inc., Cupertino, Calif., has developed for the Macintosh II personal computer is now shipping, with a handful of third-party application programs ready now and others promised. Software written for Unix System V.2.2 can be ported to A/UX fairly easily, Apple says. The company has married Unix to the friendly Macintosh user interface, which makes A/UX unique in the Unix world. But the 2.2 version it is based upon is not the current standard—version 3.0—so Apple still has more catching up to do.

HITACHI WILL MAKE DRAMS IN U. S.

Hitachi Ltd. plans to make dynamic random-access memories in the U. S., and has resumed construction on a front-end wafer line in Irving, Texas. The fab was put on hold in 1986 during the DRAM market collapse. But with demand and prices rising, Hitachi's interest has peaked again. Full-scale production of 256-Kbit chips is expected to start in May 1989, using a 1.3-μm CMOS process. Hitachi may eventually also use the new wafer fabrication line to build logic products, such as microprocessors and application-specific integrated circuits.

SPIRE'S SOLAR CELL IS 21.7% EFFICIENT

In the leapfrogging competition to improve space-based solar cell efficiency, Spire Corp. has taken the lead with a gallium arsenide-on-germanium cell that proved 21.7% efficient in simulated space conditions. The previous record for space-based solar cells was 19.4%. On Earth, the 2-by-2-cm cells do even better—24.3%. By using germanium as a substrate, the Bedford, Mass., firm was able to make thinner, lighter cells with two junctions, one in each layer.

SONY TAKES AIM AT U. S. CAD MARKET

Sony Corp. is gunning for a share of the U. S. work station market. The company has set up a new unit, Sony Microsystems Co., to market NEWS, for Net Work Station, a 32-bit Unix-based engineering work station [*Electronics*, March 19, 1987, p. 79]. The $4,000 work station is priced well below offerings from Sun Microsystems Inc., which is a leading player in the two markets that Sony is most interested in: design systems for software and technical publishing. Unit president Masahiro Morimoto says the company expects to recruit 200 independent U. S. software vendors to develop application programs for NEWS.

MCC SUPERCONDUCTOR STUDY HAS 13 BACKERS

Thirteen companies have joined the Microelectronics and Computer Technology Corp.'s research study into electronic applications of high-temperature superconductivity. MCC began studying the materials last summer, concentrating on using high-temperature supercomputers as interconnects in super-cooled computers. Future work will include thin-film deposition and superconducting micro-chips.

TANDEM WILL USE MIPS'S RISC CHIP

Future work stations from Tandem Computers Inc. will use a reduced-instruction-set computer architecture designed by MIPS Computer Systems Inc. Executives at Tandem's Micro Products Division in Austin, Texas, decline to say when the company will introduce the RISC-based systems, which use AT&T Co.'s Unix System V operating system. The new work stations are expected to replace Tandem's year-old LXN system. Tandem's choice of MIPS is a big win for the Sunnyvale, Calif., company, which is battling an emerging field of other RISC vendors in a race to line up customers.

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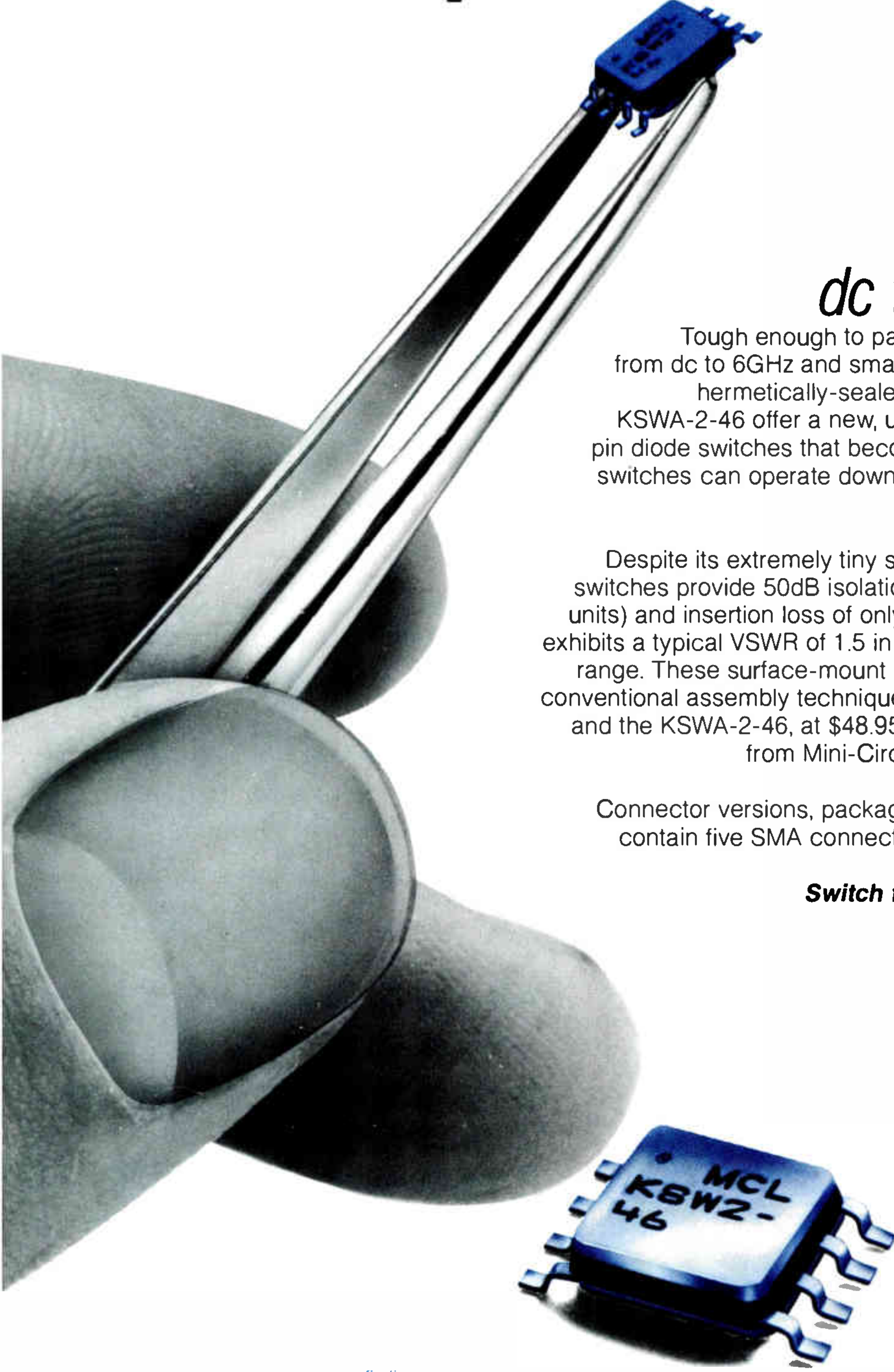

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		KSW-2-46 ZFSW-2-46		KSWA-2-46 ZFSWA-2-46	
FREQ. RANGE		dc-4.6 GHz		dc-4.6 GHz	
INSERT. LOSS (db)		typ	max	typ	max
dc-200MHz		0.9	1.1	0.8	1.1
200-1000MHz		1.0	1.3	0.9	1.3
1-4.6GHz		1.3	1.7	1.5	2.6
ISOLATION (dB)		typ	min	typ	min
dc-200MHz		60	50	60	50
200-1000MHz		45	40	50	40
1-4.6GHz		30	23	30	25
VSWR (typ)	ON	1.3:1		1.3	
	OFF	—		1.4	
SW. SPEED (nsec) rise or fall time		2(typ)		3(typ)	
MAX RF INPUT (bBm)					
up to 500MHz		+17		+17	
above 500MHz		+27		+27	
CONTROL VOLT.		-5V on, OV off		-5V on, OV off	
OPER/STOR TEMP.		-55° to +125°C		-55° to +125°C	
PRICE (1-24)		**$32.95** **$72.95**		**$48.95** **$88.95**	

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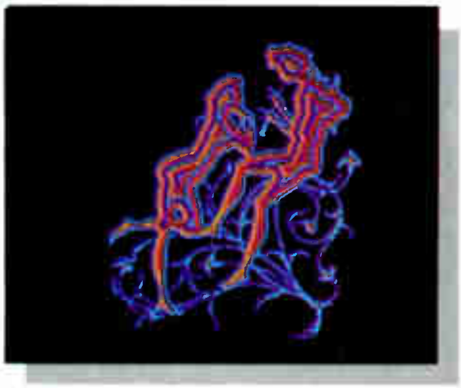

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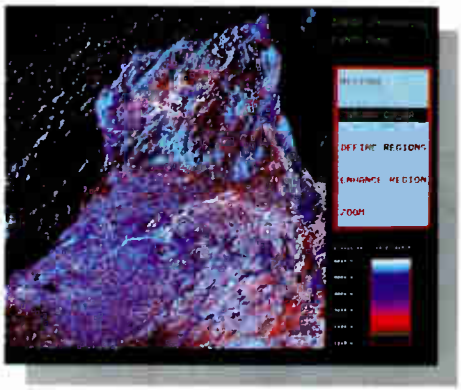

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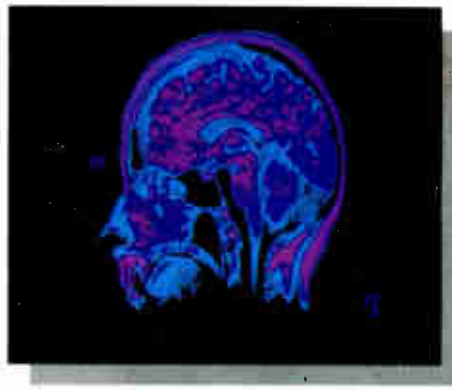

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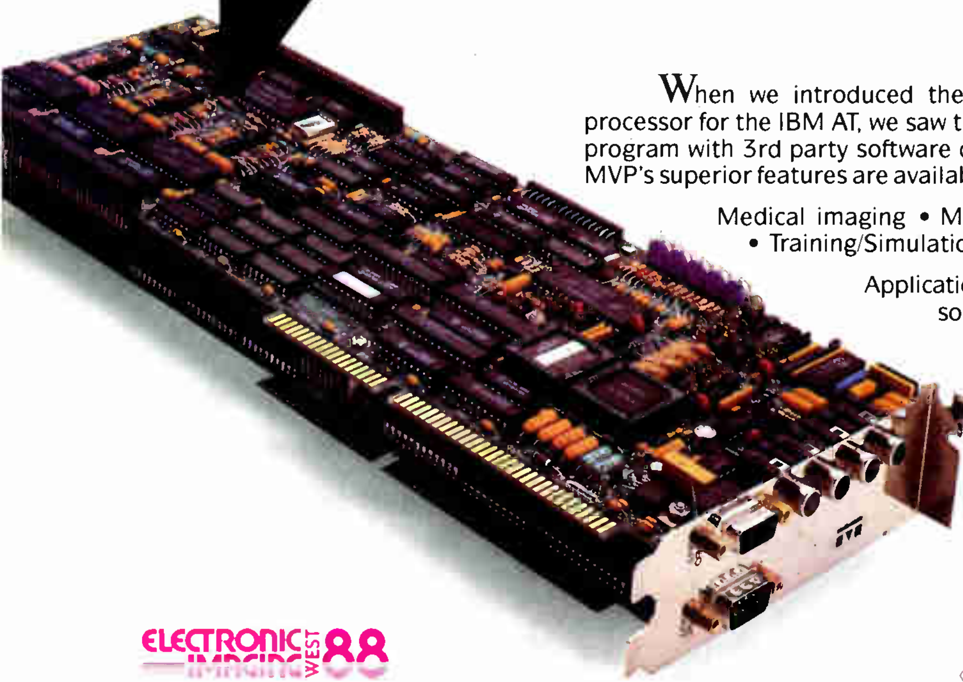

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