

**AT LAST: A TOOLKIT FOR CREATING REAL-TIME SOFTWARE/81
CALMA BRINGS AUTOMATION TO CUSTOM-IC DESIGN/92**

A MCGRAW-HILL PUBLICATION

SIX DOLLARS ■ SEPTEMBER 17, 1987

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PAGE 61

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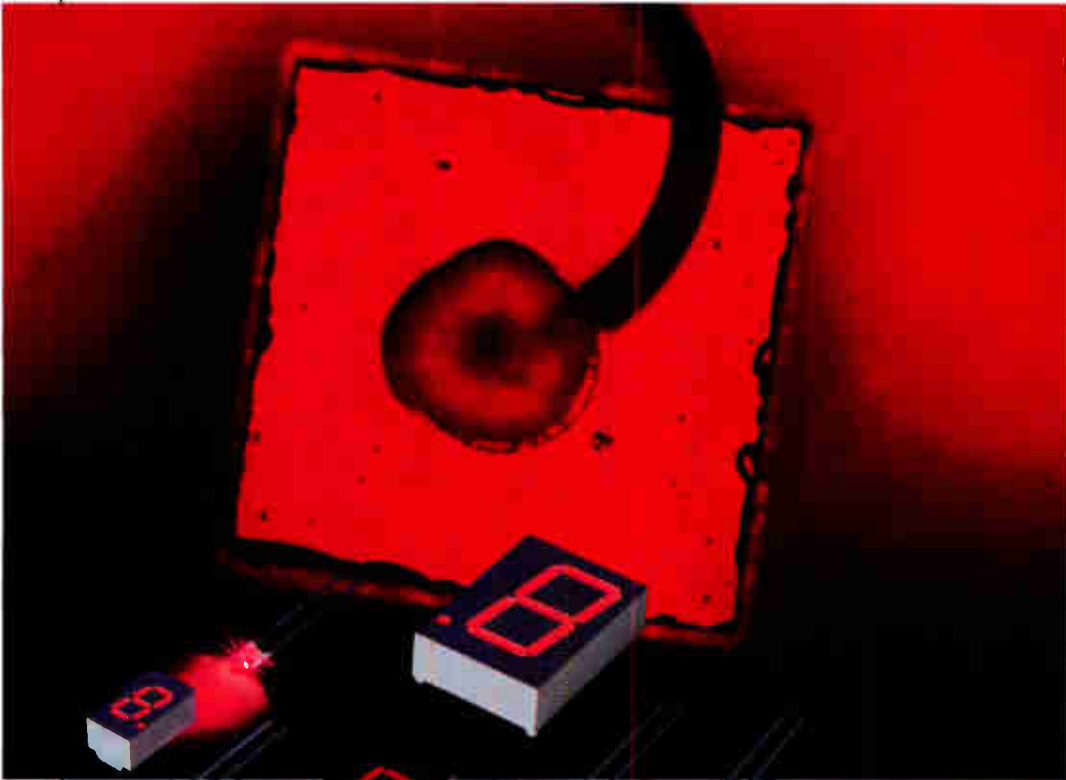
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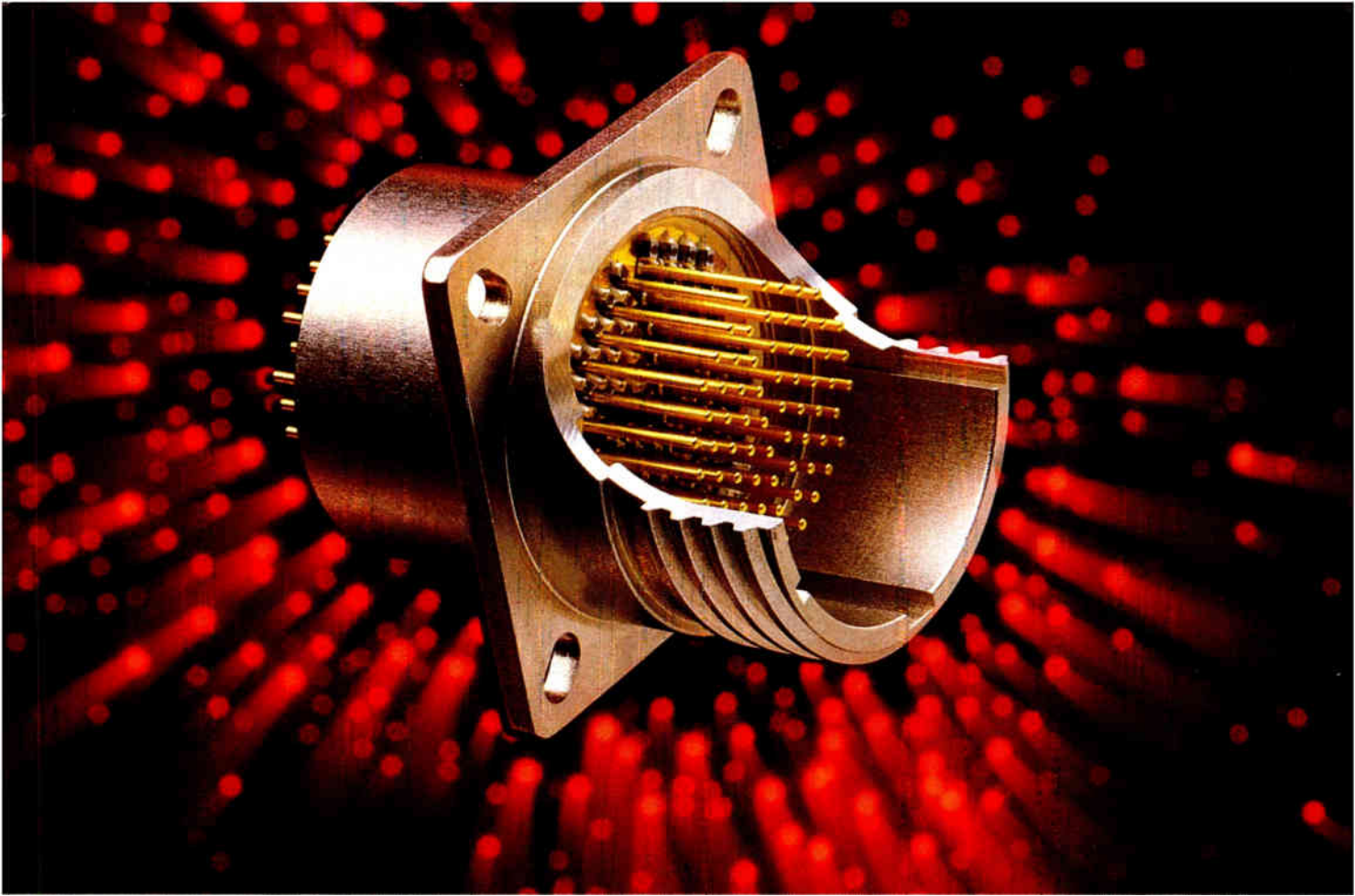
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There is no substitute for experience, and that applies to the people who design magazine articles as much as to those who design electronic devices and systems. That is why *Electronics*, with its veteran staff of journalists stationed around the world, can add so much more perspective in less time than our competitors.

Typical of our approach is the story in this issue on the sale of Fairchild Semiconductor to National

Semiconductor (see p. 43). The coverage was directed from New York headquarters by Features Editor Jeremy Young, who maintains that his job is relatively simple: "We just call on our experienced editors to scope out the meaning of major industry events. Then we lay out the possible approaches to handling the story and pick the one that we think will be of the greatest value to our readers."

But it only appears easy, because we do it so regularly that we have honed our response to the point where everyone knows his battle station and goes right to work. Not only that, but, as Jeremy puts it, "With our eyes and ears always focused around the world, we often can tell when something big is about to break. On top of that, over the years most of us have developed a kind of sixth sense about when one of these things is about to happen. It's almost cyclical."

After the editors have decided how best to approach the story, the journalist's most valuable tool comes into play: sources. "This is where they separate the men from the boys," notes Jeremy, "where the old pro leaves the young hotshot in his dust." It takes time to



YOUNG: Using experience to scope out the meaning.

develop high-level sources and to build up their trust in you. "The only real way to do that," says Jeremy, "is to be fair and honest. There are no shortcuts."

Our field editors go to their sources to develop the inside material on the significance, both short-term and long-term, of the event. "One of the best at this is Rob Lineback, who wrote the Fairchild-National piece," says Jeremy. Lineback, who has a well-deserved reputation

as a consummate craftsman, excels at writing on short deadlines—at least partly because his sources can trust his fairness and accuracy.

Staying focused not only helps us handle the story of the big event, but enables us to know when it is time to report on a significant change in the industry. That's the case with this issue's Probing the News, about the progress being made by gallium arsenide technology in its struggle to get into the mainstream (see p. 48).

"The companies leading the way are not making much noise about their progress, because so much has been said before without anything really happening," says Los Angeles editor Larry Waller. "But I have been hearing talk from my industry sources that GaAs has been coming on. Everyone has heard that before, so I was a bit skeptical. But I checked things out and decided that this time the picture looked more solid."

That's another example of how our unsurpassed experience keeps us on top of the latest trends and developments in the electronics industry.

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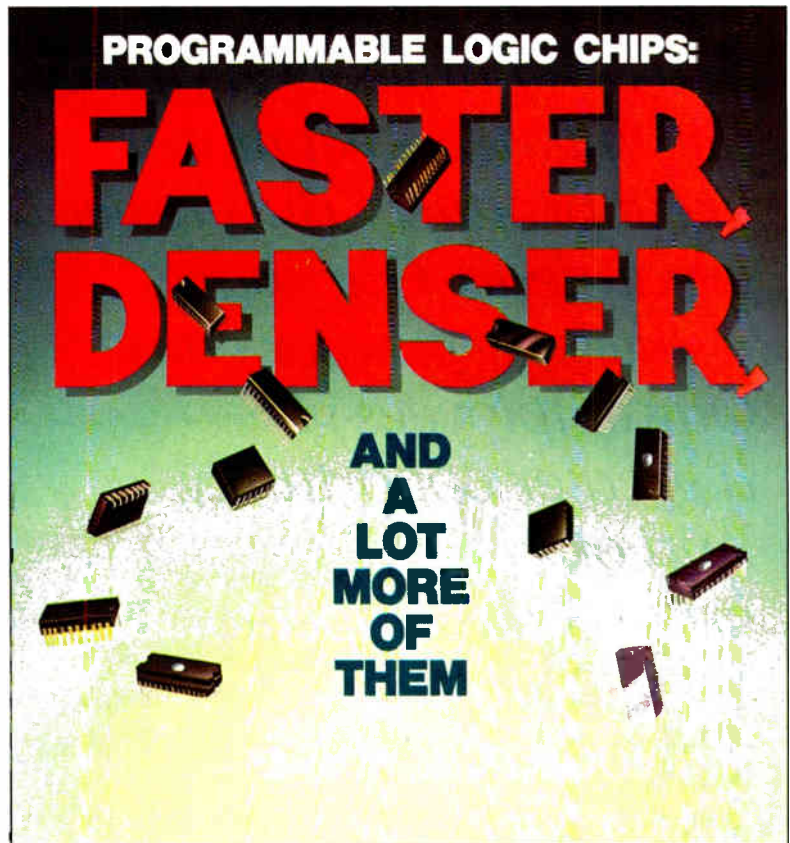
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- Zoran's 32-bit floating-point processor is loaded with new features
- A pair of TRW's image processing chips can replace 100 ICs
- TransImage's plug-in board enables IBM PC to read any text optically

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- Iomega hikes the capacity of its Bernoulli Box cartridge and puts two together in a 40-Mbyte double-drive configuration
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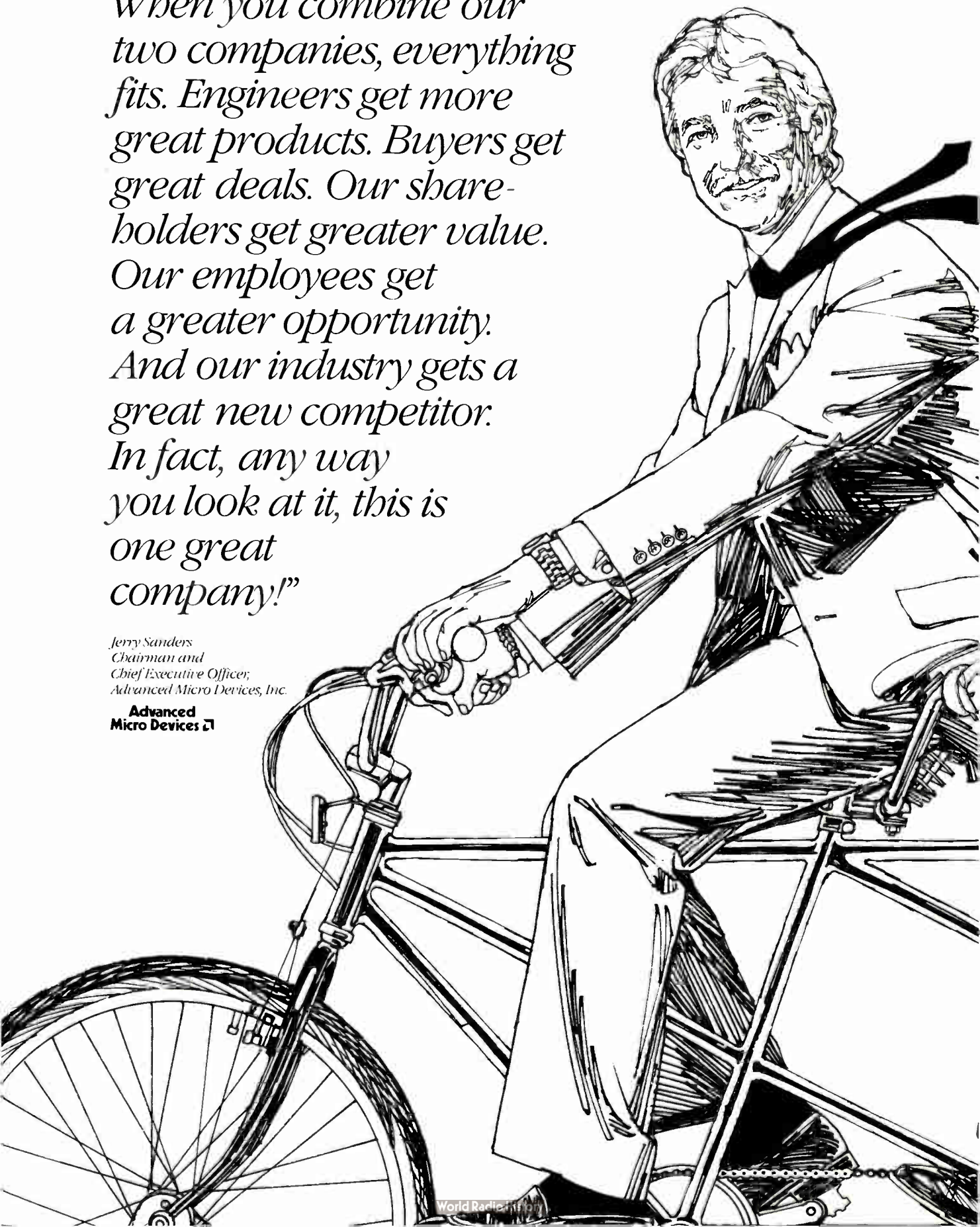
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- AT&T pumps up its computer line . . .
- . . . as Unisys adds to its minicomputer line
- U. S. electronics industry is up 4.5% in the first half
- Prime Computer enters the PC CAD market

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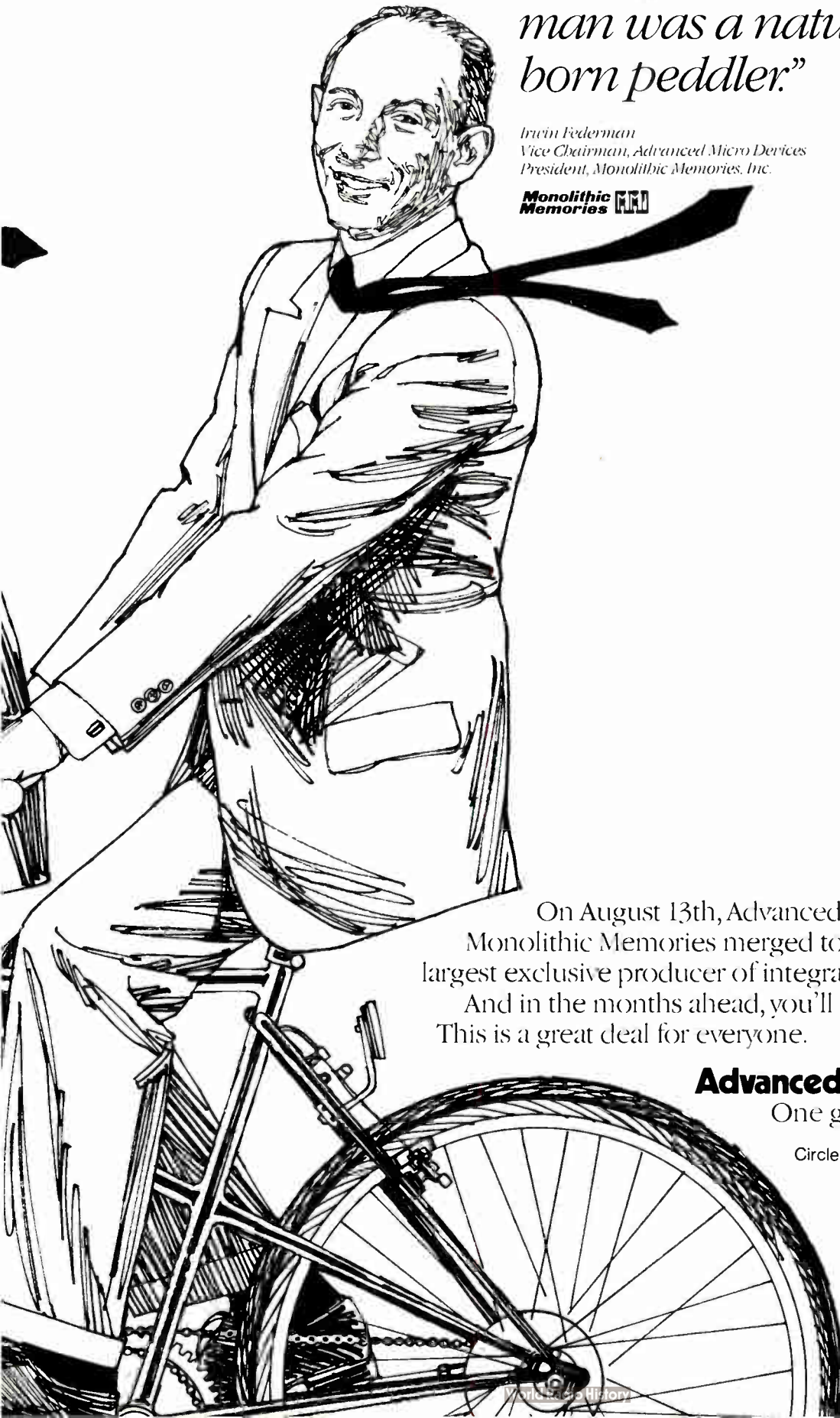
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SEPTEMBER 17, 1987

FYE

Melding two very different corporate cultures is always tough; we wish National's Charlie Sporeck and Fairchild's Don Brooks the best of luck



I have two significant "secrets" to reveal. To begin with, I have an alternate lifestyle; despite the many joys of living on the East Side, I get away from Manhattan as often as I can. Destination: Down East Maine, so far down east that my home looks out over the Bay of Fundy and the Canadian coast. My neighbors are fishermen, and there are no condos crowding the beaches (yet). Without going to the moon, I've always thought this was as far away from everything, including the electronics industry, that I could get.

So imagine my surprise when I picked up a copy of the *Portland Press-Herald* at my nearby Irving gas station only to spot a front-page story sporting a big headline that declared Fairchild Semiconductor was to be acquired by National Semiconductor! It was important news, of course, because Fairchild has 2,000 employees in South Portland. But the story quickly pulled me away from my rocky Maine coast and back to the "real" world (we sort it all out on p. 43).

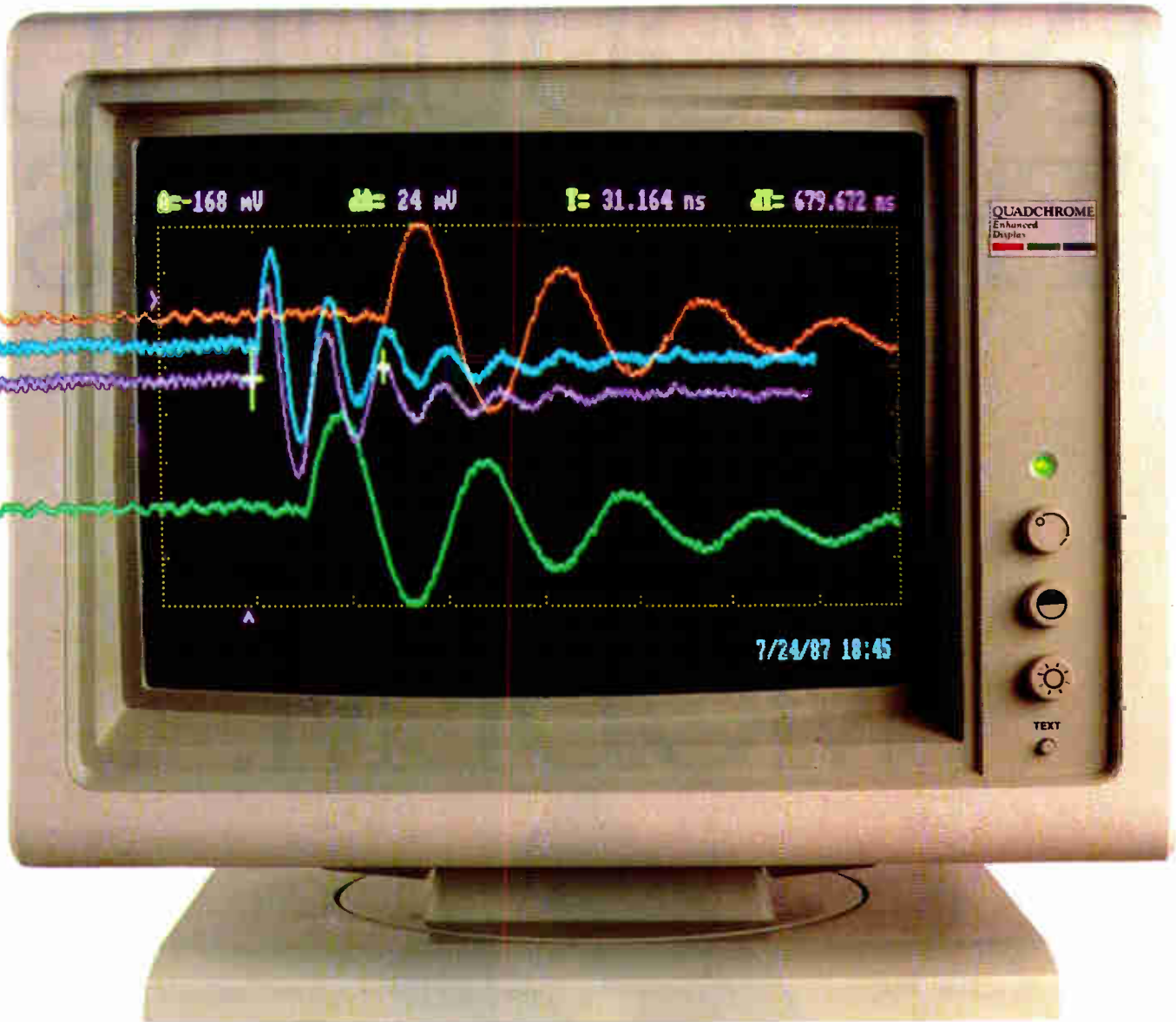
We had heard the rumors about National's interest, but frankly—and this is my second big secret—I was rooting for a management buyout by president Don Brooks and his band of Texas Instruments expatriates. I have much empathy for Don; he got his operation back on track with the right product only to be blasted by a major depression. But Don stuck to his guns and kept investing in people and product. When we put him on our Feb. 24, 1986 cover, the headline borrowed from our own promotion: "Fairchild is back!"

After Fujitsu bailed out under pressure, it seemed like a good idea when Brooks put together a package to buy the company and keep it headed in the same direction under the guidance of the same management team. Now it's not to be. I am delighted, of course, that at a time when chip makers need to be bigger and stronger to compete against foreign companies, the U.S. will gain a bigger, stronger producer. And I certainly don't have anything against National; I've covered and admired Charlie Sporeck and his company for almost as long as I have reported on Fairchild. But I'm surprised, as well as sorry, that Schlumberger didn't sell the chip maker to its management. Despite continuing losses, Brooks was getting his act together and had put together an exciting company with a talented, dedicated work force. Melding two very different corporate cultures is always tough—we wish Charlie and Don all the luck.

ROBERT W. HENKEL

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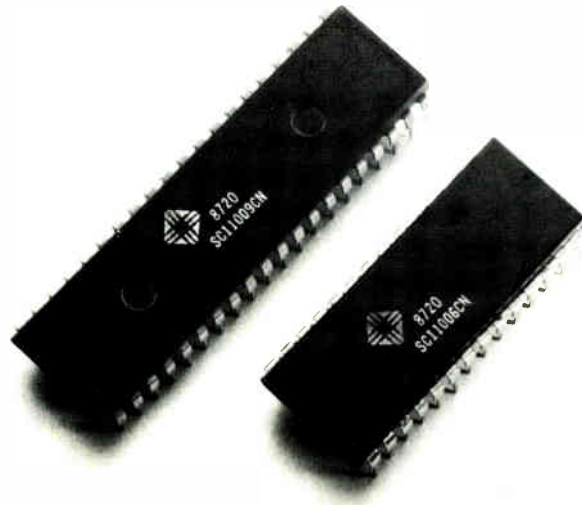
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HOW MEISE PLANS TO STEER BANYAN TO \$100 MILLION

WESTBORO, MASS.

You don't often take a \$10.5 million company to \$100 million overnight. So when David Mahoney, chairman and chief executive officer at Banyan Systems Inc., went looking for a president and chief operating officer for his company—a growing developer of personal-computer networking systems, file servers, and the Unix-based Vines network operating system—he looked “for a long time” for someone with this kind of growth experience. Despite the tough specs, he has found his man: Richard Meise, the 50-year-old former senior vice president and chief marketing officer at Convergent Technologies Inc.



MEISE: “You learn a lot when you go through a growth curve” like the one at Convergent.

Meise was with Convergent, the San Jose, Calif., manufacturer of display-based computer systems, through its meteoric rise from about \$12 million in revenue to almost \$400 million. “You learn a lot when you go through a growth curve like that” Meise says, rolling his eyes. And though Banyan probably won't make that steep a climb, Mahoney sees an excellent opportunity for the Westboro firm to become a \$100 million company.

Mahoney, a former Data General Corp. networking manager, founded Banyan in 1983. The company has gone from revenues of \$3.5 million in 1985 to \$10.5 million last year. He projects this year's revenues will top \$22 million; the company has been profitable over the past several quarters. Mahoney and his senior managers realized in mid-1986 that they “could build almost anything we wanted to, within reason, but we didn't have the marketing skills that we needed.”

Enter Meise. Not only did he win his marketing and sales spurs at Convergent, dealing with original-equipment manufacturers, but he also put in 18 years at Honeywell Inc., many of them devoted to end-user marketing and sales management. “Dick's experience in building early-stage companies into major corporate enterprises” completes a team that will lead Banyan through its next growth phase, Mahoney says.

For his part, Meise hasn't made any “startling changes or redirection. We're just doing some tuning and trying to minimize sales-channel conflicts,” he says. He points out that Banyan has always used end-user, OEM, and value-added-reseller channels, “but now we've

identified what some of the concerns are in each of these.” For example, not all of the value-added resellers were doing the job, he says, “so we fired 10 of the 23 we had, and we have replaced them with stronger organizations.”

His end-user emphasis will be on *Fortune* 1,300 companies “that are centrally located and controlled, because our products are mainly central network servers.” For example, he's looking for more opportunities like the one at Merrill Lynch in New York, where he says Banyan won the nod to network five floors of personal computers in competition with 3Com Corp. and Novell Inc.

A CONVERGENT LINE. It's no coincidence that Convergent Technologies is now one of Banyan's five major OEMs, offering a modified version of Banyan's Vines network operating system as PC Exchange/Vines. That relationship came about while Meise was at Convergent, just after a merger between Convergent and 3Com was aborted at the eleventh hour. “It was all but completed,” Meise says. “People actually had been transferred between the two companies. When it was called off, it was clear that Convergent had a need for networking.”

Meise chartered a three-month study to find a networking company and product that would make a good fit for an OEM transaction. “That study showed Vines to be the superior product among the seven we evaluated,” he says. And Banyan's strategy under Meise will be to leverage the considerable software skill he says Vines represents “and proliferate it across a broad range of platforms while still evolving our own proprietary hardware.” —Larry Curran



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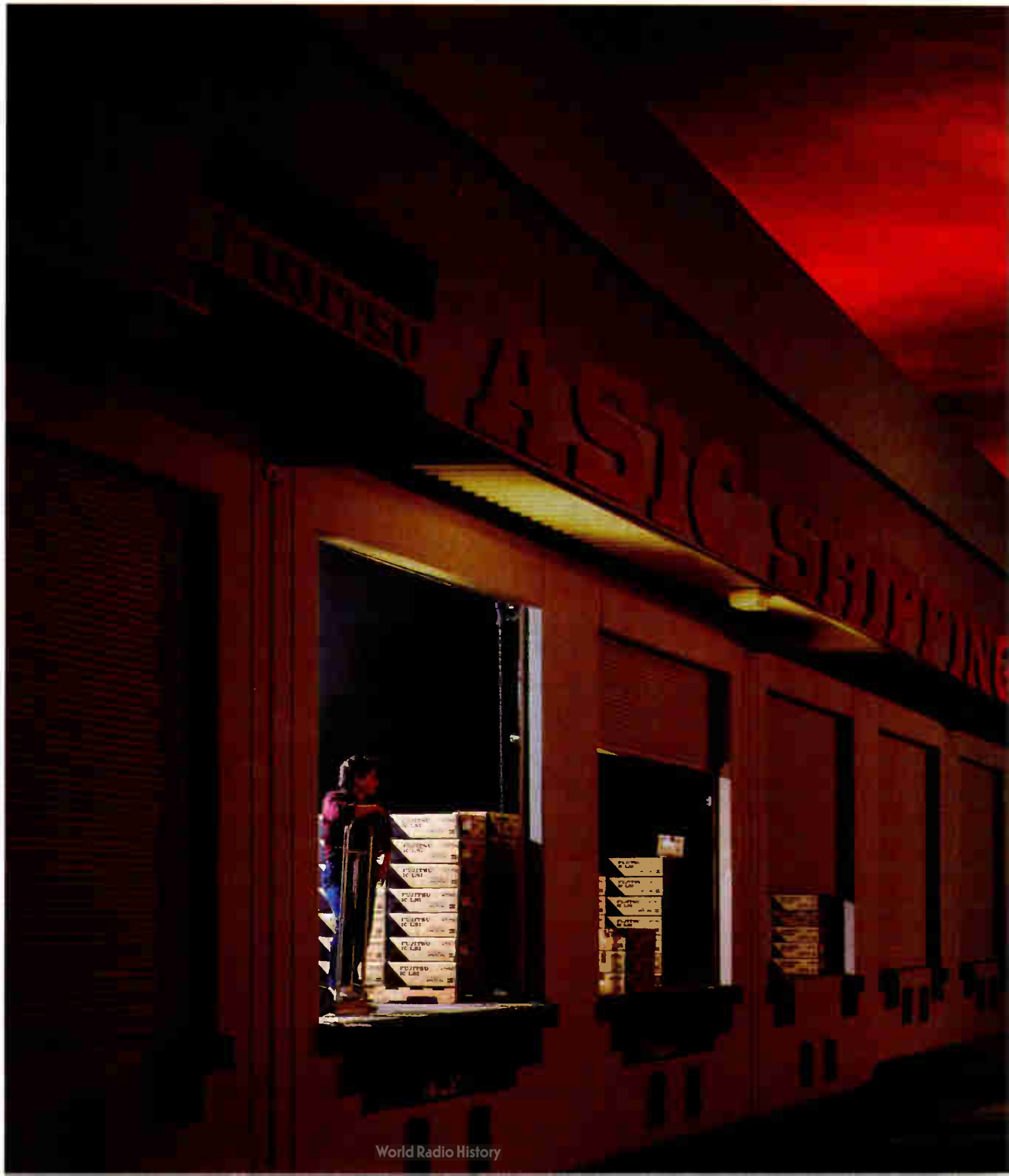
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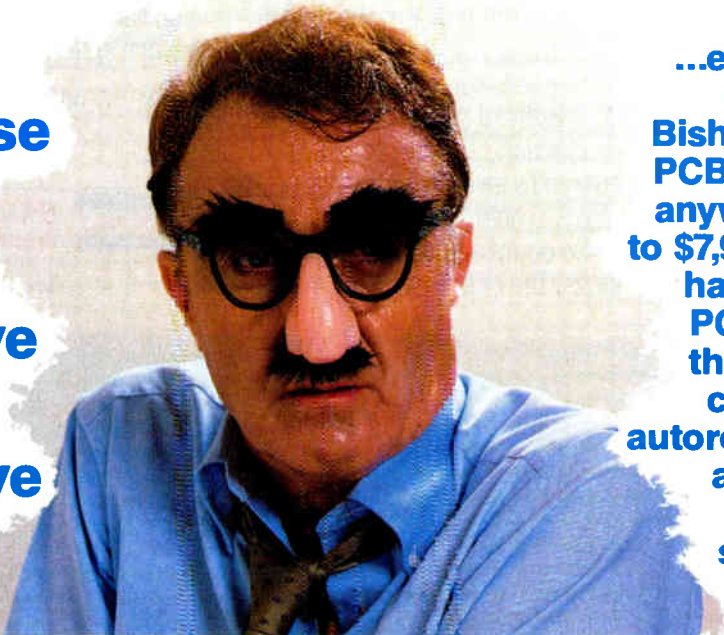
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If you've been designing printed circuit boards or doing hand tape-ups during the last 22 years, then you know Bishop Graphics as the world leader in printed circuit design and engineering products. An interesting thing happens when you are effectively the only company selling PCB design products in over 72 countries in the world. You see, there is absolutely no company anywhere in the world that has the existing customer base that Bishop has. As a result, just about every CAD company or author has approached Bishop to either privately label their CAD package or distribute it for them.

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We know that the majority of the serious designers would like a fully integrated CAD system with an autorouter that can lay down as many as three traces between a DIP if they want. The problem is not a heck of a lot of people can afford to spend \$80,000 to \$200,000 for a CAD package. It didn't take us long to realize that PATHFINDER's AutoRouter had the power and performance of the most expensive mainframe-based PCB CAD systems. Nothing that we had evaluated, or that was brought to us (including most of the brand names that you know), could compare with the overall ability of PATHFINDER.

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PATHFINDER works in conjunction with, and uses the industry standard for 2D drafting... AutoCAD™. You get a complete PCB and electro-mechanical 2D CAE workstation. You have full schematic drawing and capture, layout plus 32-bit autorouting. Not only can you create your own netlists, partslists, etc. but you can take an ASCII formatted list or document from another CAD system and format it so that PATHFINDER will read it. You've also got full IGES and Gerber I/O capability. PATHFINDER even allows you to "preview" your photoplot before sending it out to be plotted. You have generation of silkscreen and solder mask layers, drill drawings, assembly drawings, fabrication drawings, fast "on-the-fly" parts creation, 3D views, color or monochrome at any resolution, hardware pan and zoom, the use of a TTL, discrete and connector part library, stretching the layout, the latest concept of "what you see is what you get" (WYSIWYG), ratsnesting, drag and rubber-banding, semi-automatic heat sinks, keepout areas, top and bottom views for SMT with 3D views, and on and on.

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PATHFINDER also provides you with real time Display While Routing. What good does it do to come back after the autorouting has taken place only to discover that you wish you would have stopped it 5 minutes into the routing design to make a manual edit? Also, you'll be able to autoroute down to 6¼ mil trace widths...3 traces between a DIP pad.

Another thing we discovered is that even mediocre autorouters can achieve 100% completion rates if the parameters are sloppy enough. The real test of autorouting is not just speed, not just percent completion, but most importantly the quality of design. You'll achieve the same kind of performance and completion rates that you would achieve on mainframe-based autorouters with PATHFINDER. You can autoroute up to 16 layers. You have total access to the strategy parameters given you in the AutoRouter including rip-up and re-route when needed.

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World Radio History

ELECTRONICS NEWSLETTER

TI TO USE NEW BICMOS PROCESS TO BUILD ADVANCED LINEAR CHIPS

Texas Instruments Inc. isn't going to let the pending merger of arch-rivals National Semiconductor Corp. and Fairchild Semiconductor Corp. get in the way of its year-old drive to take the lead in the advanced linear integrated-circuits business. A major push for the Dallas company will come from custom and semicustom circuits based on a new bipolar-CMOS process that can mix up to 30 analog functions with a selection from TI's library of 300 3- μ m CMOS digital standard cells. A new analog-digital IC-design system is being created to shorten the time it takes to complete full-custom linear ICs from months to weeks, TI managers claim. They plan to allow customers to design their own LinASIC chips by mid-1988. The challenge is stiff: TI is trying to grab linear market share from the National-Fairchild combine, which should become the analog-IC market leader once the deal is completed (see p. 43). □

CRAY'S DECISION TO DROP THE MP COULD HAUNT IT IN THE FUTURE...

Cray Research Inc.'s abrupt decision early this month to ax development efforts on its most advanced supercomputer, the MP (see p. 49), is likely to produce a new competitor at the high end of the supercomputer market, industry watchers say. It could also make things tougher for Japanese firms intent on cracking the U. S. supercomputer market. MP designer Steve Chen has vowed to form his own company and go head-to-head with Cray's founder, Seymour Cray. "There could now be two superstar American supercomputer designers targeting the high end of that market," says Gary Smaby, a technology analyst at Piper, Jaffray & Hopwood Inc. in Minneapolis. Cray Research was faced with choosing between Chen's MP and Seymour Cray's Cray 4, Smaby says; "they probably couldn't have afforded both." Cray Research canceled the MP because development costs were projected to reach \$100 million, double the original estimate. □

... WHILE CHEN SHOULD FIND FINANCIAL BACKING WITH EASE

It shouldn't take Steve Chen long to establish a company to compete with Cray Research Inc. Observers say the supercomputer wizard, who left Cray earlier this month, probably will find it easy to round up the backing he needs to develop his MP supercomputer, which would tie up to 64 processors together with a high-speed optical-interconnect scheme. "There are a lot of people out there who would be willing to write a \$100 million check today if you can convince them you've got a machine fast enough to solve their problems," says J. Richard Sherman, cofounder and director of the Consortium for Supercomputer Research, an Edina, Minn., market researcher. The consortium projects that 15 to 25 high-end machines carrying price tags of \$25 million to \$100 million will be installed between 1990 and 1992. □

NOW HYPRES'S TIME-DOMAIN REFLECTOMETER HAS A 120-GHz BANDWIDTH

Tiny Hypres Inc., the Elmsford, N. Y., company that produced the first commercial Josephson-junction-based instrument, a 70-GHz sampling oscilloscope and time-domain reflectometer [*Electronics*, Feb. 19, 1987, p. 49], has halved the rise time of its chips to 3 ps in a working prototype. That corresponds to an effective bandwidth of 120 GHz. The company also has produced versions of the superconducting chips that could potentially have 0.5-ps rise times using niobium nitride technology, marking the first time that useful circuits have been fabricated in niobium nitride outside Japan, says Hypres's president and founder, Sadeg Faris. Niobium nitride becomes superconductive at 10 K; the niobium alloys Hypres previously used became superconductive at 4.2 K. □

ELECTRONICS NEWSLETTER

AMP AND DALLAS SEMICONDUCTOR TO DEVELOP A NEW KIND OF CONNECTOR

Dallas Semiconductor and Amp Inc., the Harrisburg, Pa., connector manufacturer, have teamed up in a research-and-development partnership to develop devices in the field of "micromechanics aimed at innovative chip-to-chip interconnects and alternative printed-circuit-board techniques," according to the prospectus for an upcoming Dallas Semiconductor stock offering. Amp has an equity interest in the Texas company but would not disclose its value. Michael Bolan, Dallas Semiconductor's marketing vice president, says the agreement will "marry [his] company's expertise in putting intelligence into sockets and the mechanical engineering know-how of Amp, with the aim of embedding large functional blocks in connectors." Such reconfigurable connectors, says New York analyst James Magid, could allow users to configure systems for a variety of specific applications. □

EUROPE'S CHIP MAKERS TELL U. S. AND JAPAN: 'NO MORE MR. NICE GUY'

US. and Japanese semiconductor suppliers will face harder times in Europe if the European Electronic Component Manufacturers' Association has its way. In a just-released report, the association demands greater protection against unfair trading practices and dumping, pushes for rapid technical standardization across the 12-nation European Community, and calls for a shift in government support from pure research to product development and manufacturing. The group says its members can compete "anywhere in the world" when it comes to circuit research and innovation, but fears that America's marketing muscle and Japan's heavy government support of industry will undermine Europe in world markets. Brutal competition seems inevitable: the group estimates that world integrated-circuit production capacity will reach \$70 billion by 1990—but demand will trail at only \$55 billion. □

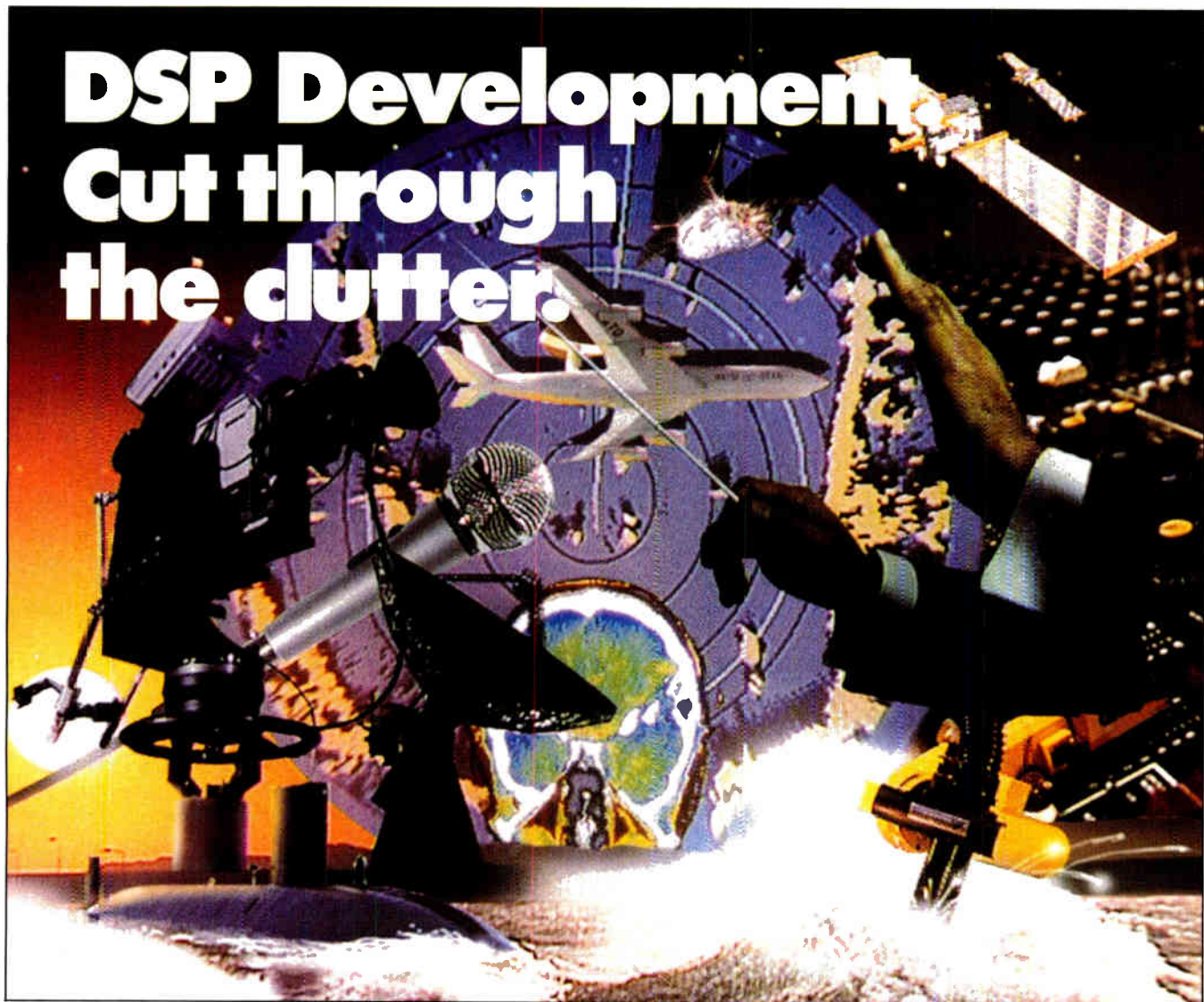
SONY'S BIG WORK-STATION PUSH WILL STAY IN JAPAN FOR NOW

Sony is ramping up its presence in the Japanese work-station market by expanding its line of Unix-based, 68020-microprocessor work stations. Sony would like to break into the U. S. market, but it blames high U. S. tariffs for holding it back. The company can't predict when the work stations will reach the U. S., but that's good news for U. S. competitors. With the latest introductions, Sony's line now spans the range from low-end diskless smart terminals to high-speed expandable systems with over 1 gigabyte of disk capacity. Sony is also one of just two Japanese firms—the other is Sanyo—to offer Berkeley Unix with its work stations. It also supports the proposed standard user interface, X Windows. Sony's newest models are the NWS-711, which has a single processor, no hard disk, and a \$4,000 price; and the top-of-the line NWS-921, which has a 20-MHz 68882 floating-point coprocessor, greatly increased expandability, and a \$55,000 price tag. □

NORTH, LATE OF TRW, SIGNS ON WITH NEURAL-NETWORKS STARTUP

Robert North, who was fired by TRW Inc. from his group vice president's post last December, has been named president and chief executive of Hecht-Nielsen Neurocomputer Corp., a San Diego, Calif., startup. North, who ran TRW's \$700 million Electronic Systems Group, was dismissed after TRW acknowledged that its San Diego Military Electronics and Avionics Division had been overcharging on defense contracts (see p. 122). He has since described himself as a scapegoat, claiming he knew nothing of the overcharging, and has filed a lawsuit for wrongful termination. Hecht-Nielsen was founded last year by two former TRW military-electronics veterans to develop computers and software tools based on neural-network technology. □

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PRODUCTS NEWSLETTER

TI PLANS TO HAVE 4-MBIT DRAM SAMPLES EARLY NEXT YEAR

Look for samples of 4-Mbit dynamic random-access memories from Texas Instruments Inc. in the first quarter of 1988. Fabricated at TI's Miho, Japan, plant, the 4-M-by-1-bit TMS4C4096 will have a 200-by-625-mil die size and targets a power dissipation of 50 mW active. It will follow an introduction schedule similar to the Dallas-based company's 1-Mbit DRAMs, which are in volume shipment now to key customers but not yet available through distributors. The 1-Mbit DRAMs cost \$14 to \$25 each, and the company will be producing them at a rate of a million units per month by December. TI plans to make the 1-Mbit DRAM generally available next year in both 1 M-by-1-bit and 250-K-by-4-bit configurations. □

ZORAN'S 32-BIT FLOATING-POINT PROCESSOR IS LOADED WITH NEW FEATURES

Zoran Corp.'s 32-bit VSP-325 floating-point processor boasts faster execution of a 1,024-point fast-Fourier transform than the company's 16-bit VSP-161—1.7 ms, compared with 2.4 ms. But that's just the beginning. The new vector signal processor also offers loopback and control features analogous to those of microprocessors, including 52 digital-signal-processing instructions, general control functions, and the ability to address 16 million floating-point words in external memory. Fabricated in the Santa Clara, Calif., company's 2- μ m double-metal CMOS process, the VSP-325 operates as a stand-alone processor in applications such as laboratory instrumentation, image processing, sonar, and radar. Whereas the VSP-161 is optimized for operations such as finite-impulse-response filtering [*Electronics*, July 24, 1986, p. 59], the VSP-325 targets infinite-impulse-response filtering. Execution time for a typical infinite-impulse-response filter is 0.4 μ s. Samples will be available in the second quarter of 1988 for \$490 each in 100-lot quantities. □

A PAIR OF TRW'S IMAGE-PROCESSING CHIPS CAN REPLACE 100 ICs

Designing image-processing boards can be a lot simpler—and cheaper—thanks to a new chip from TRW Inc.'s LSI Products division. Two TMC2301 Image Resampling Sequencers replace as many as 100 devices now needed for tasks such as image rotation, rescaling, and filtering, claims the La Jolla, Calif., division. Used in pairs for horizontal and vertical control, two microprogrammed TMC2301s can manipulate images up to 4,096 by 4,096 pixels while dissipating less than 0.5 W. The 18-MHz device processes a complete 512-by-512-pixel field in 15 ms. Now in production, the TMC2301 comes in two commercial versions and one military version—all packaged in 68-pin grid arrays. In quantities of 1,000, the standard 0°-70°C commercial chip costs \$69, and a burned-in version costs \$77. The military-qualified device, which is fully screened to MIL-STD-883C specifications, costs \$145 in 1,000-unit quantities. □

PLUG-IN BOARD ENABLES IBM PC TO READ ANY TEXT OPTICALLY

System integrators can build nearly limitless document-scanning flexibility into desktop publishing products with TransImage Corp.'s OCR Co-Processor board. Unlike competing products that can read a limited number of programmed fonts, the OCR Co-Processor handles fixed-pitch, proportionately-spaced typeset documents as well as text from typewriters and near-letter-quality printers. It turns the trick with proprietary algorithms in system memory that filter out stray marks, isolate each character, and classify it through a shape-recognition system. The Sunnyvale, Calif., company's board plugs into IBM Corp. Personal Computers and compatibles and sends ASCII text to the computer. Available now, prices start at \$1,200 each in volume purchases. □

PRODUCTS NEWSLETTER

TAPE DRIVES CHANGE INTERFACES IN A SNAP

System integrators can now meet customer demands for interchangeable interfaces in backup tape drives by integrating California Peripherals Inc.'s E-series ¼-in. drives into their products. The 125-Mbyte CP-125E and the 150-Mbyte CP-150E can be configured with the Small Computer Systems Interface, the basic QIC-36 interface set down by the industry's Quarter-Inch Compatibility committee, or the QIC-02 interface simply by replacing formatting boards inside the units. Both subsystems fit into a half-height, 5¼-in. form factor commonly used for floppy disks. Evaluation units of the Torrance, Calif., company's E-series drives are scheduled for delivery in November, with volume production set for March 1988. Pricing is \$475 to \$525 in volume purchases, depending on the interface selected. □

TOSHIBA'S GaAs CHIP SET MULTIPLEXES UP TO FIVE TIMES FASTER

High-capacity fiber-optic communications networks and other high-speed applications can run their multiplexing/demultiplexing operations up to five times faster with Toshiba Corp.'s gallium-arsenide chip set, compared with present silicon implementations. The 4:1 TG3000G multiplexer and the 1:4 TG3001G demultiplexer achieve 3-GHz operation by using tungsten nitride for their gate electrodes—a manufacturing breakthrough, claims the Tokyo company. The chips' operating voltages mean they can be used as direct replacements for emitter-coupled logic circuits that now dominate high-speed multiplexing applications, including high-speed measuring instruments and ultra-high-speed LSI testers. The chips have source-coupled FET logic circuits with a lightly doped drain structure and 0.8- μ m gate lengths. The 2-by-2-mm chips are available now in Japan in a 28-pin ceramic package at a sample price of 60,000 yen each. So far, export prices have not been set. □

ROBOT CONTROLLER DELIVERS FASTER CYCLES, BETTER ACCURACY

By using closed-loop digital control of robot servomotors instead of conventional analog servo-control techniques, GMFanuc Robotics Corp.'s RH Karel Robot Controller offers significant improvements in robot cycle times and arm-path accuracy. Characterization is not complete, says the Rochester Hills, Mich., company, but performance improvements could range up to 40%. The controller also adapts easily to change. Robots controlled by analog techniques require tuning of precision potentiometers when robot parameters are changed, for example, but digital technology allows an arm to be programmed for optimum performance under a variety of load, extension, velocity, and overshoot parameters. The RH controller has a 34% smaller footprint and an optional 27% reduction in cabinet height compared with the RF. It is not sold separately but is available in about 80% of GMF's robot line. Pricing varies according to configuration. A GMF A-200 robot suitable for electronic assembly applications, for example, is priced from about \$35,000 to \$45,000, including the RH controller. □

HARRIS'S CMOS 80286 DELIVERS UP TO 60% POWER SAVING

Harris Corp.'s CMOS version of Intel Corp.'s 80286 microprocessor consumes only 100 mW per MHz—that's 60% less than the standard n-MOS part and 40% less than the low-power version. The 80C286 comes in 10- and 12.5-MHz speeds and is part of a second-source agreement between Intel and the Melbourne, Fla., company's semiconductor division. Samples are available now. The 10-MHz device costs \$125 each in 100-lot quantities and the 12.5-MHz version is \$170. A 16-MHz version is due in sample quantities during the fourth quarter. □

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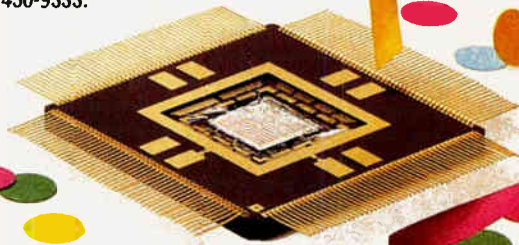
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Electronics

DIGITAL EQUIPMENT STRIKES BACK AT IBM'S 'VAX KILLERS'

BUT SOME OBSERVERS CALL THE PRICING DISAPPOINTING

BOSTON

Digital Equipment Corp. has accelerated its assault on IBM Corp. with an unprecedented MicroVAX product blitz. The impressive display of technology actually managed to outshine the splash and flash of a dazzling 11-day DECworld show that is believed to have cost the company more than \$20 million and included the use of two ocean liners as hotels and meeting sites for customers.

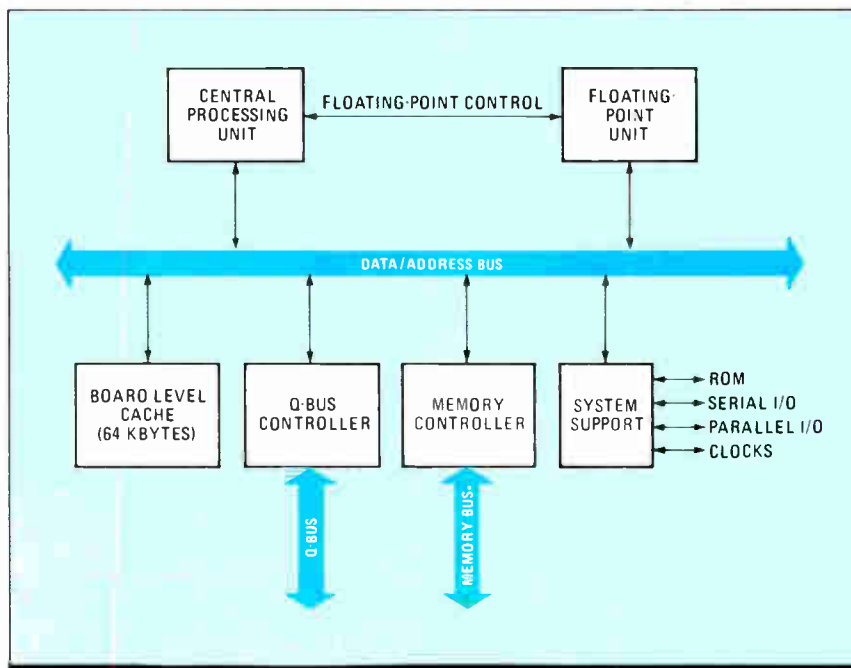
The extravaganza at Boston's waterfront World Trade Center featured 11 new MicroVAX products, including two systems, two work stations, three server products, and several disk drives. But the technology star was a new MicroVAX custom CMOS chip set. The set elevates performance of the systems to levels 2.6 to 4.2 times those of comparable members of the two-year-old MicroVAX II.

Developed over three years at DEC's huge Hudson, Mass., semiconductor facility and at its engineering design center in Tokyo, the set underlies the performance of the new systems. Importantly, the chips allow the new MicroVAX 3500/3600 family to run more than 3,500 existing VAX application programs without modification.

The company is shooting squarely at IBM's 9370 family—the so-called VAX killers. Jesse Lipcon, senior consulting engineer and MicroVAX program manager in Maynard, Mass., says the 3500's performance "exceeds that of the IBM 9370 Model 60 at less than the price of the 9370 Model 20. We'd like to benchmark it against the Model 90, but we can't get one."

MIXED REACTION. Industry observers generally applauded the products, but some found the pricing disappointing. "The MicroVAXes look like terrific products, but we were expecting lower prices," says John Freeman, senior analyst at The Yankee Group in Boston. John W. Adams, chairman of Adams, Harkness & Hill Inc., Boston, agrees: "These are not aggressively priced. It may be that they're getting plenty of business without aggressive pricing, or wanted to wait and see how it goes in manufacturing before dropping prices."

Mark D. Stahlman, a research analyst



NEW PARTS. The chips in DEC's new 3500/3600 chip set are made in a two-metal-layer CMOS process and consume 1.2 W per chip, about half the power of the set in the MicroVAX II.

who follows the computer-system and work-station markets for Sanford C. Bernstein & Co. in New York, says the 3500/3600 fills a gap in the DEC product line between earlier members of the MicroVAX II family and the midrange VAX 8000 line. "They've placed these new MicroVAXes just right and will be very successful with them," he says. "The story is much less important on the workstation side, however. There's still a big gap between these VAX stations and Sun and Apollo," with DEC lagging.

The chip set is made up of five VLSI and two LSI chips; all of them are used in the central processor of the MicroVAX 3500 and 3600 and in the new VAX-station work stations. The chips are made with two-metal-layer CMOS. Bob Supnik, corporate consultant in DEC's semiconductor engineering group in Hudson, says CMOS was chosen because it consumes less power than the n-MOS used in the two-chip MicroVAX II chip set—1.2 W per chip vs. 2.5 W.

That power differential shows up in

the effective clock speed of the new central-processing-unit chip, which is designated the 78034: 22 MHz vs. 10 MHz in the earlier design. The device is a 32-bit pipelined microprocessor built with 180,000 transistors.

It has on-board cache implemented in single-transistor dynamic cells, which Supnik believes makes it the first complex microprocessor to use single-transistor dynamic random-access-memory design. The result is three times as much cache on the die as would be possible using static-RAM technology. Lipcon points out that the on-chip cache feature contributes to system performance in DEC's two-tier cache scheme for the MicroVAX 3500/3600 by speeding instruction execution time by at least 2-to-1. Besides the CPU chip, there are a VLSI floating-point unit, memory controller, Q-bus interface device, and system-support chip. A smaller clock generator and memory transceiver complete the set.

With 16 Mbytes, the MicroVAX 3500

has twice the main memory of the MicroVAX II, and it houses a new 280-Mbyte 5.25-in. Winchester disk drive in its 27-in.-high pedestal. The MicroVAX 3600 has 32 Mbytes of main memory, offers a new 622-Mbyte 14-in. Winchester in a single 41-in.-high cabinet, or two such drives in an expanded-cabinet ver-

sion. Prices for the systems range from \$74,800 to \$180,000.

Lipcon says the MicroVAX 3500 has a 90-ns microcycle, compared with 200 ns in the MicroVAX II, or 400 ns for each microcycle involving a memory reference. "In effect," he says, "we're getting a 4:1 speedup if we hit in the chip-

level cache." And the CPU chip also incorporates six more instructions in microcode than does the MicroVAX II CPU chip, "which makes for more robust processing than leaving them to software emulation, which is the case in the MicroVAX II," Supnik maintains.

-Lawrence Curran

OPTOELECTRONICS

LASER MILESTONE: GaAs ON SILICON

CHAMPAIGN, ILL.

Gallium arsenide-on-silicon is taking on a new glow at the University of Illinois, where researchers have managed for the first time to fabricate semiconductor lasers on the material that can operate continuously at room temperature.

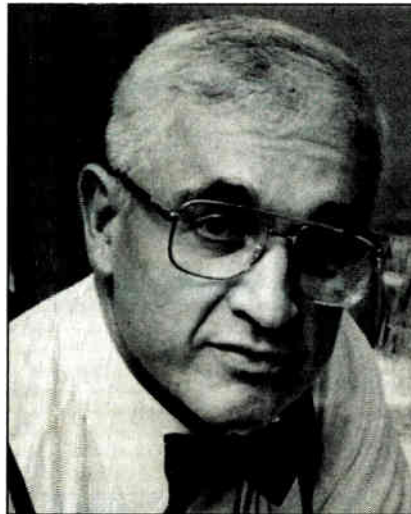
Researchers have been striving hard at about a dozen U. S. and Japanese university and industrial labs to build such a device, since it could one day lead to monolithic integrated optoelectronic devices that combine dense silicon circuitry on chip with high-speed III-V lasers for lightwave communications.

GaAs-on-silicon has already been proven for electronic circuitry [*Electronics*, Sept. 18, 1986, p. 31]. But by demonstrating continuous-wave room-temperature operation of lasers built in GaAs-on-silicon, Illinois researchers have accomplished what many in the field consider to be the acid test for the material.

"It's a milestone that everyone has been looking for as sort of an indication that there is some practical reality to this idea," notes Russell D. Dupuis, a technical staff member at AT&T Co.'s Bell Laboratories, Murray Hill, N.J. "This has been sort of like the Holy Grail," adds Andrew J. Purdes, manager of III-V materials at Texas Instruments Inc.'s Central Research Laboratory in Dallas.

MISMATCH. The main obstacle stems from a lattice mismatch between the silicon substrate and the atoms-thick layers of GaAs grown on it. This causes dislocations that thread their way from the silicon through the GaAs film. Majority-carrier devices, such as FETs, are less susceptible to these defects than are minority-carrier devices, such as lasers. The defects raise laser operating thresholds and erode device performance because of carrier recombination.

"With a laser diode, you're generating photons and heat, and both of them contribute to the multiplication of the dislocations," explains Nick Holonyak Jr., Illinois researcher and professor of electrical and computer engineering. "This creates dark line defects that just grow and grow until the device becomes opaque. It just stops working."



HOLONYAK: "More things are going to happen over the next year or two."

Labs including Lincoln Laboratory in Lexington, Mass., and the Nagoya Institute of Technology in Japan have reported on lasers built in GaAs-on-silicon that can operate in a pulsed mode at room temperature [*Electronics*, Feb. 10, 1986, p. 16]. But before Illinois, no team had succeeded in making any cw versions that could operate at 300°K.

Illinois researchers teamed with counterparts at TI and Xerox Corp. to pull off the feat. The starting GaAs-on-silicon was provided by TI and grown by molecular-beam epitaxy. After initial ex-

periments at Illinois, this material was shipped to the Xerox Palo Alto (Calif.) Research Center, where workers used metal-organic chemical vapor deposition to grow an AlGaAs/GaAs heterostructure atop the GaAs-on-silicon.

This process formed a quantum-well active region for the laser. Single quantum-well laser diodes 10 to 20 μm wide and 250 μm long were then fabricated in the AlGaAs/GaAs layer back at Illinois.

The researchers do not claim to have licked the defect problem entirely. Most of the dislocation lines are "absorbed" at the silicon/GaAs interface in the epitaxial material, and are further strained out in the first deposition layers, Holonyak says. But dislocation lines still exist in the deposited epitaxial layers all the way up to the quantum-well active region, he notes, though in the upper layers they are about 1 μm apart. This means that while the material is good enough to support cw lasers that work "for hours," Holonyak says, the devices are still unstable and can degrade. Threshold currents on one device started at 110 mA and rose to 178 mA after 90 minutes.

Some researchers believe commercialization is a decade away, but others are more optimistic. "More things are going to happen over the next year or two," Holonyak predicts. "It wouldn't surprise me if in two years somebody has some circuitry on silicon that's driving a laser that's sitting on top of that silicon."

-Wesley R. Iversen

STANDARDS

IS SIMPLER QUALIFICATION COMING FOR MIL-SPEC ICs?

ROME, N. Y.

A landmark military specification for gate arrays is shaking things up in the market for military application-specific integrated circuits, and it may end up having far wider impact. The new spec is the first in what is likely to be a series of generic specifications that will allow manufacturers to qualify entire product lines simply by meeting requirements with their most complex part.

The specification—Mil-M-38510/600, for bipolar gate arrays, and /605, for CMOS parts—sets the first definitive quality and performance standards for military gate arrays and puts them on the Qualified Parts List. Previously, they were individually qualified by the chip and systems makers.

Gate arrays are just a starting point, though. "What we see is more and more custom circuits in low-volume produc-

tions," says Charles Windish, a project engineer who helped write the spec at the Rome Air Development Center, Griffiss Air Force Base, Rome, N. Y. Qualifying a product line from design methodology and tools through wafer fabrication, testing, packaging, and final assembly should save time and money, Windish says. If that holds true, standard-cell ASICs and very high-speed ICs (VHSIC parts), both usually low-volume production parts, will also get generic specification.

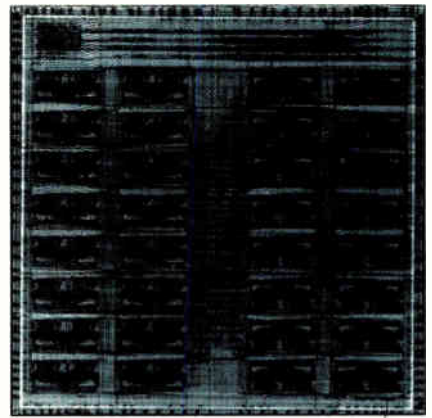
BIG IMPACT. Such fallout from the new generic spec to other kinds of chips, particularly commodity parts, "could have explosive impact," says Scott Hudson, who tracks the military chip business for Integrated Circuit Engineering Co., a Scottsdale, Ariz., consultant. But the new spec's biggest impact could be in shaking up the gate-array market.

Hudson says it could force a realignment of vendors, since players such as General Electric Co. and United Technologies Corp. have taken the lead in getting certified. Although neither one is considered a gate-array force, both now have an edge on such competitors as bipolar leaders Motorola, Fairchild, and Applied MicroCircuits. Motorola and Fairchild won't comment, and Ap-

plied Microcircuits says it is evaluating the new standard. Joseph Gemperline, Microelectronics Branch chief at the Defense Electronics Supply Center in Dayton, Ohio, which is handling the certification process, counts GE, UTC, Honeywell, and LSI Logic as furthest along in the race to be qualified.

The qualification procedure is complex. Manufacturers must provide DESC with specifications for the product family, a list of quality-control procedures, a list of design and manufacturing equipment, and other data. Nothing is taken for granted. Joseph Fero, technical-programs manager at LSI Logic Corp., Milpitas, Calif., says that not only is it the first spec to consider a company's quality-assurance work for commercial customers, but "it's the first that considers design procedures, along with wafer fab, assembly, and testing."

Design methodology is also vital. Gemperline says that when DESC schedules a site inspection and audit, it will investigate the computer-aided-design equipment as well as the wafer fab and test stations. The thinking is that by controlling these design phases, it is not necessary to qualify separately the different gate arrays produced by changing final mask levels. In effect, the mili-



ONE FOR ALL. The DOD's generic spec affects gate arrays, like this one from LSI Logic.

tary has accepted the way that semiconductor makers have dealt with large customers for years in ship-to-stock programs where the basic device is qualified only once.

The final step is the manufacture of a standard evaluation circuit on the maker's largest gate-count device. Windish says, "We're looking for at least 75% utilization" of the chip. And once that is done, says DESC's Gemperline, a chip line can be qualified within a matter of days. —Tobias Naegele, Larry Waller

MEMORIES

NOW, NEC STORES FILES ON A CHIP

TOKYO

Taking aim at a chunk of the memory market now served by disk drives, NEC Corp. engineers have developed a 128-Kbyte "silicon file memory" whose capacity and ruggedness would suit it for computers from portables to mainframes.

File memories—battery-backed non-volatile random-access-memories or bubble memories that run upwards of 20 Mbytes—bridge the speed and size gap between slow magnetic-disk mass storage and rapid main memory. Unlike RAM disks, however, the file memories do not cut down the available space in the main memory. The new NEC memory chips are dense and rugged, so they should find a home in minicomputers and high-performance work stations as well as in personal computers and portables. And with the cost-per-megabyte of chip memory edging down toward that of disk memory, a 5% share of the fast-growing \$7.5 billion file-memory market is a realistic target, says Shigeki Matsue, general manager of NEC's Memory Products Division.

One disadvantage of chip memory is volatility, but NEC has minimized this problem. By trading off lower power for somewhat less speed, they have made

battery backup practical: standby power consumption is reduced 30 times and the operating power about fivefold, compared with standard dynamic random-access memories. That makes it feasible to cram 20 Mbytes of silicon file devices and a battery good for several months' backup into the same size package as a 5¼-in. half-height hard-disk drive.

*Its target: 5% of
the \$7.5 billion
file-memory market*

The new memory would be a boon for personal computers, where a portion of main memory is often preempted for use as a RAM disk—and with no battery backup, it is practical only as a temporary file. Moreover, the main-memory size is reduced, maximum storage size is limited, and cost and power are excessive. Silicon file chips are also superior to standard RAM chips for use as electronic disks in mainframe computers. In present mainframes, the cabinet for the backup battery is usually larger than the case for the disk itself, even though the backup is only two days at most.

The new devices resemble page-mode

CMOS DRAM memories, but there are important differences because of the speed-power tradeoff. For each page of 512 successive bits, the devices have a maximum access time of 1 μ s for the first bit and 200 ns for successive bits, providing a 5-Mbit/s transfer rate.

Cells are similar to those in standard DRAMs, including a trench capacitor, but are redesigned for the power advantage. CMOS peripheral circuits are designed so that both n-MOS and p-MOS transistors of each pair are never on at the same time.

The new device, designated the μ PD42601, is fabricated on a 4.5-by-10- μ m chip in a 1- μ m CMOS process with one layer of polysilicon and one layer of aluminum. It will be available in three types of packages—an 18-pin dual in-line package, a 20-pin zig-zag in-line package, and a 26-pin small-outline J-lead chip carrier. Pinouts are the same as in standard DRAMs, with the addition of a refresh connection to one of the no-connection pins.

The sample price will be about \$35 when shipments begin in November. Full production at a rate of about 200,000 units a month will begin in January. The production price is not yet available. —Charles L. Cohen

A DSP INTERFACE GOES ECONOMY CLASS

AUSTIN, TEXAS

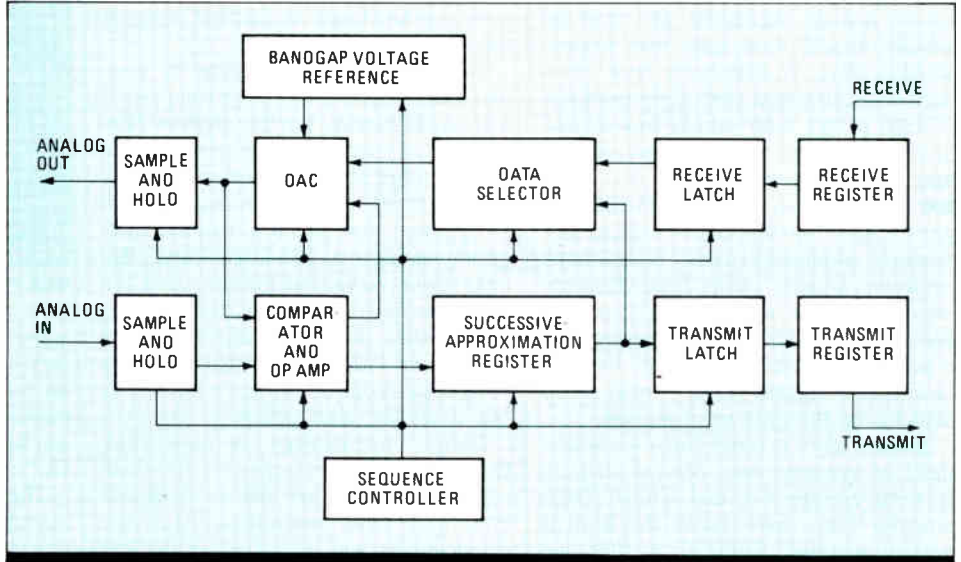
One fairly new niche business is jumping off the charts these days. As might be expected, new products propelling this market for digital-signal-processing interface chips have emphasized improved accuracy even when it means an increase in price. Now Motorola Inc. is entering this market but it is taking a different tack.

The big chip maker is targeting the market segment for medium-performance DSP applications with a low-cost, less accurate data-conversion circuit that marries the analog signals of the real world to the processing precision of digital computing. For the entire DSP interface market, sales are expected to grow from just over \$218 million in 1986 to \$1 billion in 1991, according to analyst Will I. Strauss of Forward Concepts Inc., Tempe, Ariz. "There are a whole bunch of startups gearing up, and the major competitors are pouring into this field," he adds. "Application-targeted ICs are coming into play very early."

FLOATING RESOLUTION. Motorola is holding down the cost of its new 13-bit linear codec, the MC145402, by using a digital-to-analog converter architecture that adjusts 9 bits of resolution as amplitude changes. The floating-resolution approach enables Motorola to boost the accuracy of a chip made with a six-year-old CMOS technology. At the same time, it avoids costly self-calibration logic that some other manufacturers have integrated onto early DSP analog-interface chips for still higher accuracy.

Motorola's codec delivers enough accuracy over 13 bits of dynamic range to satisfy a large number of cost-sensitive DSP applications, such as high-speed modems, echo cancelers, sonar, or voice and music synthesizers. The chip's architecture also yields a smaller die compared with DSP interfaces that have on-board calibration logic, says Al Mouton, marketing manager for the product in Austin. Self-calibration logic can take up more than twice the real estate of the converter circuitry that it is controlling.

Motorola is not going to leave the high end of the interface market to its competitors. It plans to add high-performance 16-bit analog-to-digital and digital-to-analog conversion using a totally different architecture and a new 1.5- μ m CMOS technology. And rival Texas Instruments Inc. isn't idle either. TI is also



ECONOMY MODEL. Motorola is holding down the price of its DSP interface chip by adopting a floating-resolution architecture that adjusts 9 bits as amplitude changes to increase accuracy.

focusing its CMOS attention on a broad line of analog interface circuits as a companion-product strategy for its TMS320 DSP family. This month TI introduced its first DSP interface chip, the 32040, and high-end self-calibrating interfaces are also due.

And Crystal Semiconductor Corp. is already marketing 16-bit ADCs with self-calibrating logic on-chip. The parts use new testing software that specifies performance in a DSP-oriented frequency domain, rather than the traditional linear method. *-J. Robert Lineback*

PARALLEL PROCESSING

CONCURRENT TO MARKET NAVIER-STOKES COMPUTER



NEW YORK

Parallel computing is quick, but application-specific parallel computing is spectacularly fast. That's the approach researchers at Princeton University in New Jersey followed to build a super-fast supercomputer—a system that's now going commercial.

The Princeton machine designs and models fluid-dynamics systems. It should outperform even the future Cray 3 supercomputer, reaching speeds beyond 50 to 60 billion floating-point operations per second. Now Concurrent Computer Corp., a Tinton Falls, N.J., parallel-computer maker, will license the Princeton technology to build a commercial version of the computer.

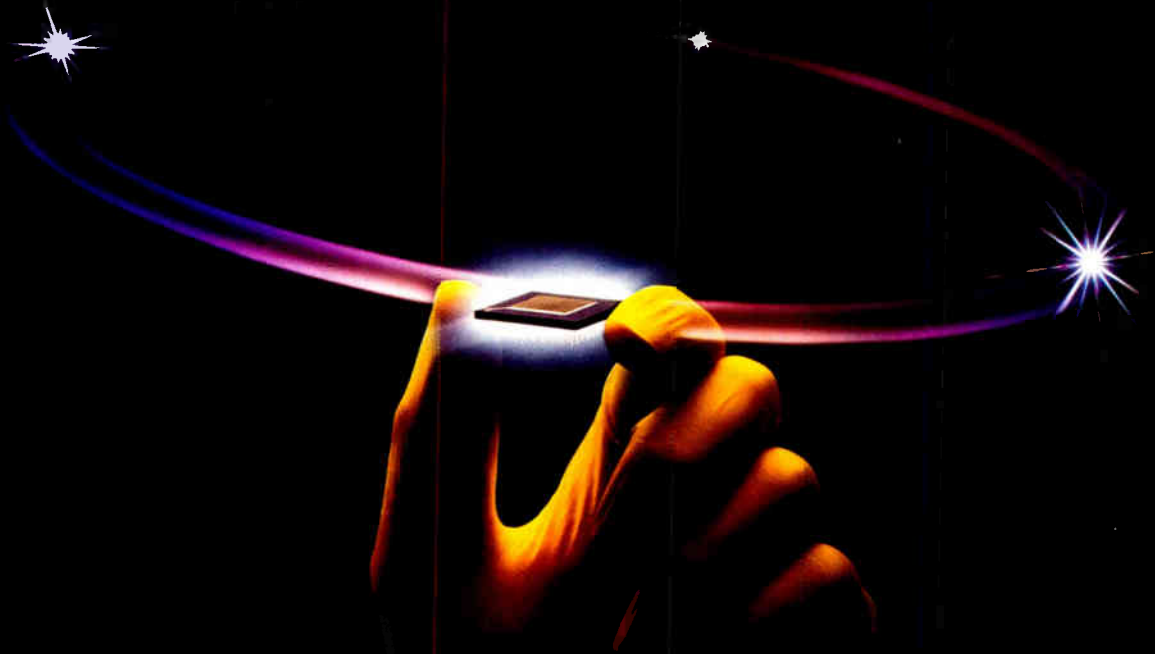
The machine, a dynamically reconfigurable parallel architecture,

NOSENCHUCK: "I didn't have the tools to solve my problem, so I invented one."

TEXAS INSTRUMENTS REPORTS ON
NETWORKING

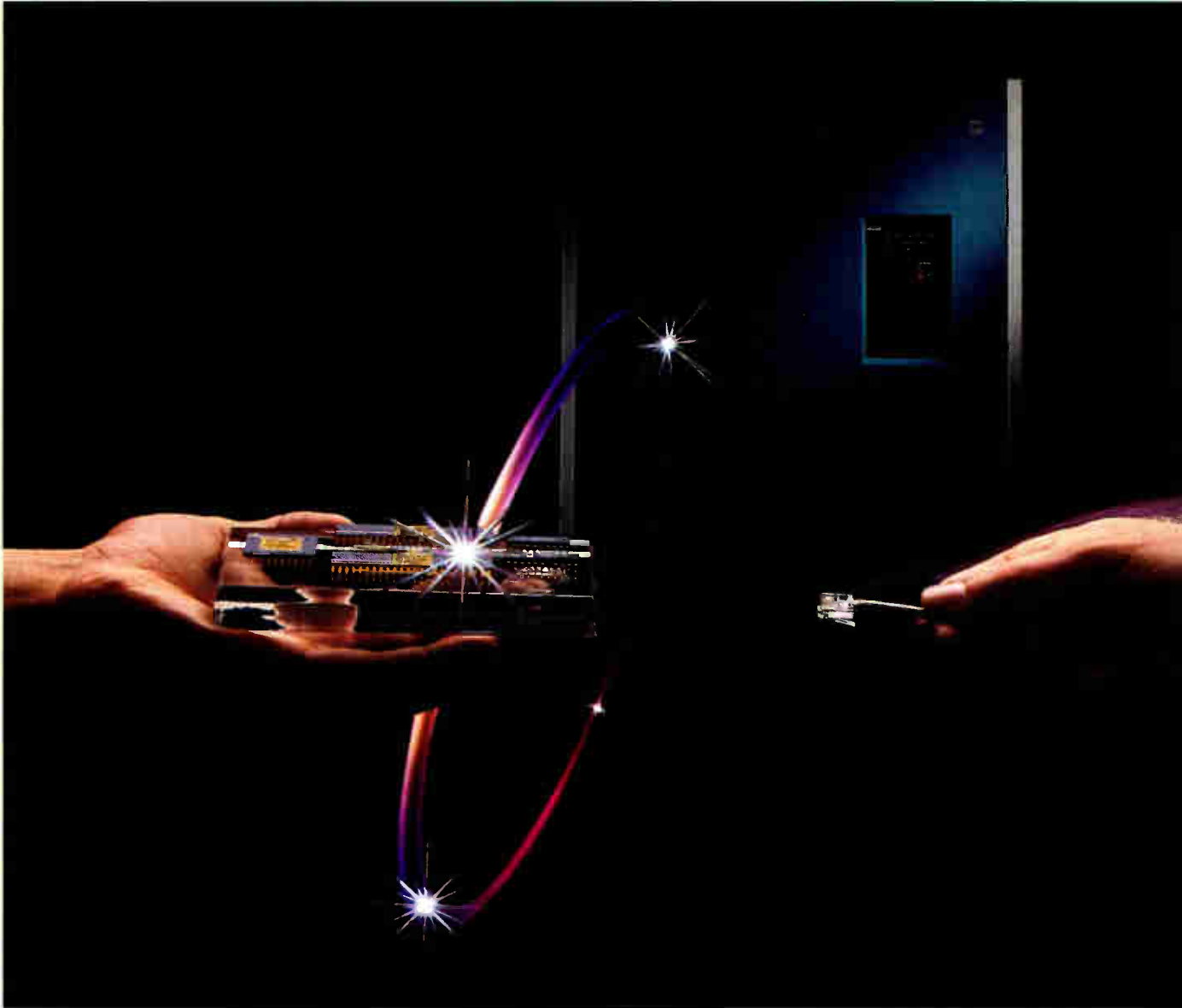
IN THE ERA OF

MegaChip [□]
TECHNOLOGIES



Networking in the Era of MegaChip Technologies:

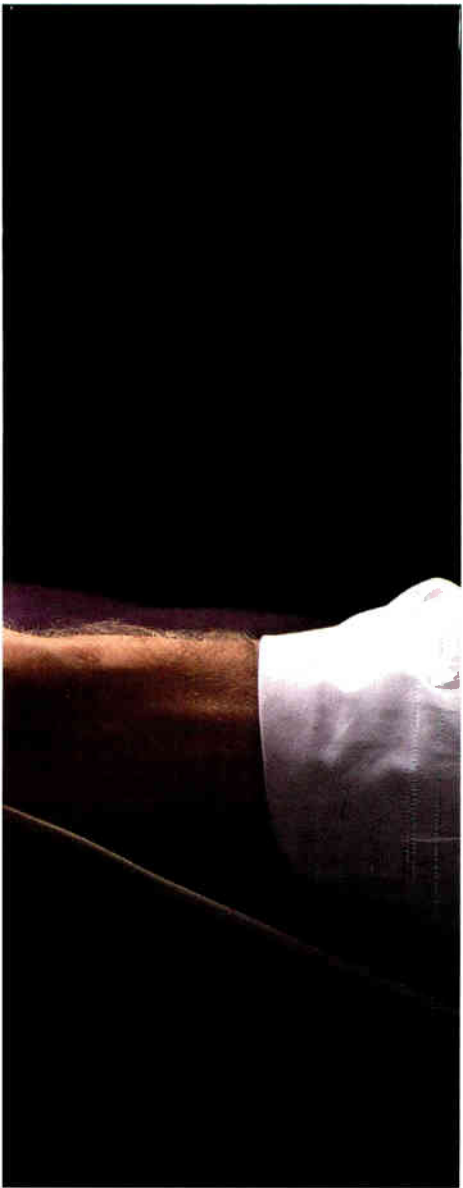
When connecting to the you need to connect with



Only the TMS380 Chip Set from Texas Instruments is tested and verified with IBM. That frees you to concentrate on the important business of making your products market winners.

Industry observers agree: The IBM® Token-Ring Network is capturing a lion's share of the LAN (local-area network) market. As stated by IBM in their October 15, 1985, product announcement, the IBM Token-Ring Network is "an 'open' network architecture for accommodation of non-IBM and IBM attaching devices . . . with semiconductor components available

IBM Token-Ring, Texas Instruments first.



the chief reason for turning to TI first when designing-in token ring connectivity. You know your TMS380-based product will be 100% compatible with IBM and industry standards.

As a result, you avoid any problems of validation, verification, or long development time. You gain time to add product enhancements that can mean a competitive edge in the marketplace.

Martin Sinnott, director, Dayton Development Center of the NCR Corporation, sums up the advantage this way: "We offer the very highest level of interoperability with the IBM Token-Ring Network via TI's TMS380 Chip Set and our own software."

An integrated solution for "open" systems

TI's TMS380 Chip Set begins with a 40-million-bits-per-second DMA interface. This provides efficient connection to high-speed microprocessors such as Intel's 80X86 and Motorola's 680X0 families and open-system buses like IBM's Micro Channel™ and Apple's NuBus™

Having built-in software jointly copyrighted by IBM and TI, the TMS380 provides all IEEE 802.5 media-access control processing, including on-board network-management services (see box). In addition, the TMS380 provides capability for message-buffer expansion and higher layer protocols, such as IBM-compatible IEEE 802.2 Logical Link Control (LLC), available from TI.

The TMS380 completes your connection to the IBM Token-Ring with physical-layer interface circuits that provide clocking, data reception and transmission, and ring-insertion control.

Opening the way to internetworking the TMS380 facilitates the design of token ring bridge and gateway products.

Good news about cost

Another reason to choose the TMS380 is that the cost of connectivity is com-

Reliable network management

"We have designed our ProNET®-4 product using the industry-standard TI TMS380 Chip Set. In addition to normal data-communications functions, the chip set provides power-up self-test as well as network-management frames for automatic error detection, parameter services, and reconfigurations. The net effect is reliable, manageable network operation."

Howard Salwen,
Chairman and Founder, Proteon, Inc.

ing down. The chip set is available now at a suggested resale price under \$100.00 (quantity 100).

The TMS380 reflects the influence of TI's MegaChip™ Technologies. These are the skills and disciplines acquired through ongoing development of high-density circuits which generate advances in semiconductor design, processing, manufacturing, and service.

These technologies are having an effect on other LAN standards. For example, TI has developed the SN75061/62 single-channel drivers/receivers that can easily be configured for use with StarLAN IEEE 802.3 1BASE5 networks. These new devices perform data transmission/reception and minimize transmission-line noise. The SN75061 is ideally suited to 1BASE5 stations; the lower-power, lower-cost SN75062, to hubs.

For more information on the broad TMS380 support, turn the page.



from Texas Instruments." All you need to capitalize on the growing demand for products that will operate on the ring is to design with TI's TMS380 Chip Set.

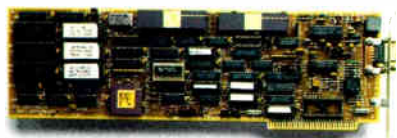
"We use TI's TMS380 Chip Set and TI's implementation of IEEE 802.2 LLC protocols to ensure IBM compatibility at media-access and software levels."

That is Howard S. Charney, senior vice president of 3Com Corporation, stating

Comprehensive support from TI speeds TMS380 design-in.

To help you with everything from token ring adapter-card prototyping through communications-protocol development and systems integration, TI makes available the comprehensive TMS380 Development Products Family.

Design-in Accelerator Kit includes hardware and debug software for completing a prototype token ring adapter: Three sample TMS380 chip sets, engi-



neering debug software with User's Guide, and an interconnect schematic.

PC Adapter Card helps you develop software and analyze traffic on the IBM Token-Ring Network. It works in both the PC Family and PC AT compatibles and incorporates TI's new IEEE 802.2 LLC. The card comes with demonstration software as well as protocol-analysis software to help develop your communications protocol.

Test Wiring Concentrator (TWC) provides the mechanism for any station to be inserted on the ring and adds LEDs that indicate ring insertion.

TMS380 LLC Evaluation Kit provides the hardware, software, and documentation required to evaluate the IBM-compatible IEEE 802.2 LLC software on your designs.

ASIC-LAN Tool Kit enables the fast development of highly integrated, differentiated, and compact adapters. The kit contains ASIC software macro building blocks and completed design examples. These support Adapter Memory Expansion and PC Bus Interface. The kit not only helps save board space, but also several months of system and hardware design.



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Token Ring Seminars are conducted on request at TI Regional Technology Centers or at your site. A two-day

workshop includes an introduction to the TMS380 Chip Set and hands-on experience in the lab. A one-day TMS380 Advanced Topics Workshop provides an understanding of the extended LLC interface on the TMS380 and provides insight into bridge applications.

For more information on TI's TMS380 Chip Set, call TI's hot-line number, (713) 274-2380. Or complete and return the coupon today to Texas Instruments Incorporated, P.O. Box 809066, Dallas, Texas 75380-9066.



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has been under development at Princeton for the past three years [*Electronics*, Nov. 25, 1985, p. 19]. It is called a Navier-Stokes computer, because its job is to solve the partial differential equations representing turbulence in fluid flow, which were developed by the 19th-century mathematicians Claude-Louis Navier and Sir George Stokes. The Princeton project is directed by Daniel M. Nosenchuck, assistant professor of mechanical and aerospace engineering. Primary funding has been by research grants from the National Aeronautics and Space Administration, which wants the machine to help it design the ultra-fast National Aerospace Plane.

Concurrent Computer will attempt to turn the design into a commercial product because "the computational fluid-dynamics market is not a small one," says James K. Sims, president. The company expects the market to reach \$1 billion by 1990, with the Navier-Stokes computer competing for 25% of that. The design can also be adapted for other applications, such as computational chemistry and the design of automobiles, ships, and submarines.

Concurrent is eyeing 25% of a \$1 billion fluid-dynamics market

The designers of the Navier-Stokes computer set out to develop a system to model the effects of air flow over airplanes and spacecraft at the transition to turbulence. "I didn't have the tools to solve my problems, so I invented one," says Nosenchuck, who is an engineer, not a computer scientist.

In studying fluid-flow control over all kinds of vehicles, it is desirable to mix and control these flows in real time over the entire vehicle. No computers exist today that can do the complete job, and wind and water tunnels also fall short. "Parallel computers with small nodes couldn't do the job either, so we decided to build a parallel machine made up of the highest-performance nodes we could build," says Nosenchuck.

First came the micronode, a prototype built in 1985, which ran at 6 megaflops. The second prototype, built last year, is called the mininode, capable of 200 megaflops. NASA will get a system made up of four mininodes; Concurrent Computer's commercial version will have yet a higher-performance node with performance equivalent to a high-end supercomputer, says Sims. A big system may have up to 128 of these nodes, with performance peaking at 50 to 60 gigaflops.

Although the machine looks like a very specialized computer, its dynamic reconfigurability makes it adaptable to

many different tasks. The topology of the interconnections among the nodes and memory modules can be quickly changed. "The machine can be reconfigured into a custom computer in less than 50 billionths of a second, to customize the machine on the fly for specific problems," says Nosenchuck.

Concurrent and Princeton both foresee that this technology will deliver a new level of computational capability in a modular and affordable system for designing advanced aircraft, spacecraft, ships, and submarines. That means it could help maintain U.S. competitiveness in the military and commercial vehicle industries. "We are targeting a

price-performance level of \$2,000 per megaflop" for the commercial system, says Sims.

Other unorthodox computers designed with government funds have gone commercial. A recent example is the fast Warp systolic-array-based processor now being offered by General Electric Co. of Fairfield, Conn. The Warp machine is based on research sponsored by the Defense Advanced Research Projects Agency at Carnegie Mellon University [*Electronics*, June 25, 1987, p. 21]. Project director H. T. Kung says Intel Corp. of Santa Clara, Calif., intends to reduce the Warp processor boards to single chips. —Tom Manuel

IEEE ELECTION

SHOULD THE IEEE HAVE TO OFFER A BALLOT CHOICE?

NEW YORK

Labor Day means the end of summer, the start of school—and election time for the Institute of Electrical and Electronics Engineers. And where there is an IEEE election these days, there is also Irwin Feerst and a controversy.

The IEEE's board has selected Emerson W. Pugh to run for president-elect. He will become president in 1988 because he is running unopposed. That's where the controversy comes in.

Feerst, the gadfly who came within 242 votes of becoming president-elect last year, asks, "What kind of election can it be with one person on the ballot?" He has mounted a successful petition campaign to place before the voters a proposed constitutional amendment that would force the board to pick at least two candidates for both president-elect and executive vice president.



PUGH. His unopposed run for IEEE president-elect is causing a controversy.

The board is opposed, maintaining that current procedures for circulating petitions to put candidates on the ballot are adequate. It points out that "a petition candidate has been elected president over a single board nominee; another individual has run as a petition candidate five times, losing twice in three-person contests and three times against single board nominees."

NOT EASY. That individual, of course, is the acerbic Feerst, who with his Committee of Concerned EEs is determined to remake the institute. He says it's dominated by executives and academics, and that it needs to change to an organization that protects the interests of working EEs. He rejects the ease-of-entry argument, saying that to run by petition requires signatures of 1% of IEEE's voting members—"more than 2,000"—and that means time, money, and organization. To pass, his proposed amendment must get two thirds of the votes cast on the issue, provided at least 20% of the voters indicate yes or no.

Meanwhile, the voting goes on. On the directors' selected ticket with Pugh—a physicist and a member of the IBM Corp. research staff—is the unopposed candidate for executive vice president, Dennis Bodson, a government engineer who is assistant manager of the National Communications System in Washington, D. C. Not surprisingly, both agree with the board that enough opportunity for opposition is provided by the petition procedure, though Pugh adds, "I personally prefer a two-candidate election."

There is also a full slate of candidates for regional and division directorships, some of which are contested. Ballots, mailed by Aug. 31 to voting members, are due by Nov. 2. The results will be announced soon after. —Howard Wolff

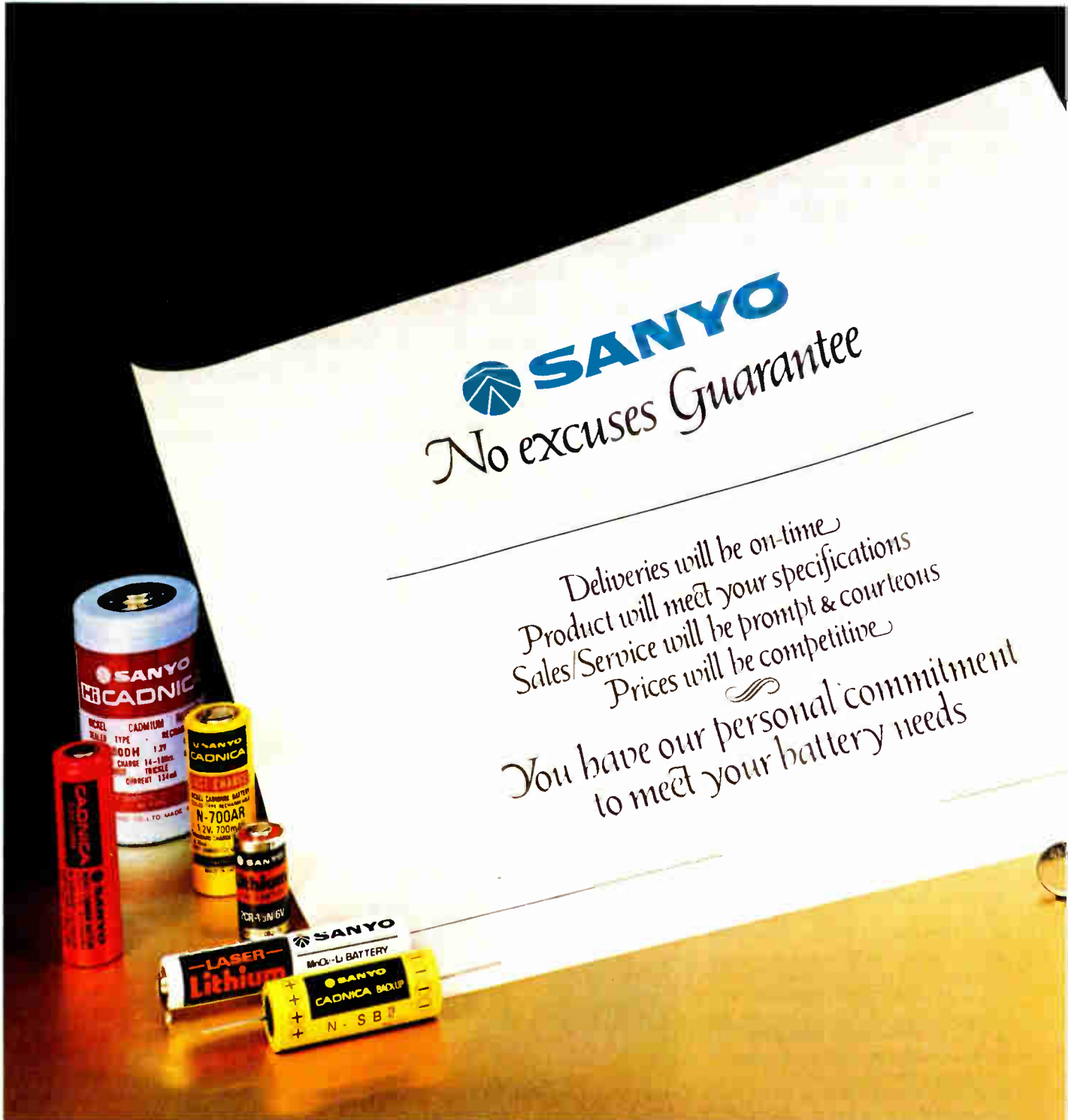
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PROBING THE NEWS

SWALLOWING FAIRCHILD MAKES A GIANT OF NATIONAL

THE MOVE VAULTS NATIONAL TO NO. 1 IN MILITARY AND ANALOG CHIPS

by J. Robert Lineback

CUPERTINO, CALIF.

Some people think the pending \$122 million purchase of Fairchild Semiconductor Corp. by National Semiconductor Corp. is a marriage made in silicon heaven. Others say it's more like a shotgun wedding in Silicon Valley. Actually, it's both.

America is losing a chip-making pioneer that played a key role in shaping the industry. But it's gaining a semiconductor giant with all the makings for world-class stature, potentially commanding chip sales of \$1.7 billion in 1987.

Taking over Fairchild's technologies, product lines, and businesses would instantly cause National to:

- Climb from 11th in total worldwide chip sales to the No. 6 spot.
- Jump from No. 6 in military chip shipments to undisputed market leader, giving the combined company at least a \$100 million lead over its closest competitor.
- Leapfrog Texas Instruments Inc. and Hitachi Ltd. to become the No. 1 supplier of analog circuits.
- Shoot up three places to second in total bipolar sales with the addition of Fairchild's strength in high-speed bipolar logic.
- Rise to No. 3 in emitter-coupled logic shipments behind Motorola Inc. and Fujitsu Ltd. with a boost of \$75 million in Fairchild products added to its own \$20 million annual volume.
- And move up from 13th to No. 7 in gate-array shipments with a combined total of \$90 million.

At National's headquarters in Santa Clara, Calif., officials are still attempting to sort through exactly what the proposed merger will give birth to, if it clears antitrust hurdles at the U.S. Department of Justice this month. At first, National was reportedly bidding only on selected pieces of Fairchild's business, with hopes of grabbing profitable products in military, high-speed CMOS and bi-

polar logic, ECL technologies, and semi-custom linear arrays. Instead, it wound up with the whole thing, excluding nonoperating facilities in Japan and West Germany and the related debt.

But if the purchase is an undisputed National coup, it's a major disappointment to Fairchild's top management. Several of the company's executives had put together a proposal for a leveraged buyout, backed by Citicorp Venture Capital in New York. Instead of owning the company, they've ended up with orders by its parent, Schlumberger Ltd., to go along with the deal quietly—or lose their jobs and stock incentives. They are refusing to talk, but the rest of Silicon Valley is abuzz, wondering why the French oilfield-service giant decided to accept National's offer of \$122 million in common stock and warrants instead of the buyout package, reportedly valued at \$225 million.

Most believe Schlumberger, which had high expectations when it bought Fairchild for \$425 million in 1979, has had enough of the massive losses it has racked up during its tenure in the chip business. That total amounts to as much as \$2 billion. The National deal was a clean break with its obligations. A management buyout engineered by Fairchild's president Donald W. Brooks might have been too risky in the eyes of Schlumberger management. Others suggest that Schlumberger executives, stung by the political storm whipped up when the company tried to sell 80% of Fairchild to Fujitsu for \$200 million, were angry at Brooks for not recognizing the embarrassment such an attempt would heap on the parent. Still others believe Schlumberger did not want Brooks to have a chance to turn Fairchild profitable next year, which would leave egg on the faces of Schlumberger

HOW NATIONAL CLIMBS THE RANKINGS BY BUYING FAIRCHILD

Total semiconductor sales			Military IC sales			
Ranking	Company	1987 Sales (\$ millions)	Ranking	Company	1987 Sales (\$ millions)	
1	NEC	3,090		National/Fairchild	273	
2	Toshiba	2,825		AMD (with MMI)	170	
3	Hitachi	2,450		TI	160	
4	Motorola	2,270		Harris	160	
5	Texas Instruments	2,200		Fairchild	155	
6	National/Fairchild	1,700		General Electric	125	
7	Philips	1,550	6	National	118	
8	Fujitsu	1,390	Bipolar semiconductor sales			
9	Matsushita	1,370		TI	1,300	
10	Intel	1,230		National/Fairchild	945	
11	Mitsubishi	1,125		Philips/Signetics	780	
—	National	1,120		Motorola	758	
—	Fairchild	580		Hitachi	725	
Analog semiconductor sales (1986)				5	National	610
1	National/Fairchild	400		6	NEC	600
2	TI	325	7	Fairchild	335	
3	Hitachi	320	SOURCE: INTEGRATED CIRCUIT ENGINEERING CORP.			
—	National	300				
—	Fairchild	100				

brass intent on unloading Fairchild. Brooks had hopes of reaching profitability as early as the first quarter next year, says one source.

"By any measure, National got a \$200 million bargain" for just \$120 million, says analyst Michael A. Gumpert of Drexel Burnham Lambert Inc. in New York. "The outlook over the next year looks bright. National did not take on any debt, and it seems to be well capitalized."

Still, most analysts say National has its work cut out: trimming redundancies in the combined work force, phasing out products that don't fit well with its own, and merging Fairchild's high-performance, niche-oriented technologies with its own common-process. It also needs to hang on to enough key Fairchild people to keep newly developed products rolling in the market, which won't be easy. One side effect of the merger is expected to be a final generation of Fairchild-spawned startups, as managers decide to follow in the entrepreneurial footsteps of numerous past Fairchild employees. As many as 200 companies—including the likes of Intel and Advanced Micro Devices—can trace their lineage to Fairchild.

Meanwhile, the industry is trying to get used to the idea of a chip business without Fairchild. National says it plans to drop the Fairchild name from the acquired business units, and it is studying



REASSURANCES. National's Sporek says Fairchild customers will get what they need.

whether or not to retain the current product designations. All of Fairchild's second-source pacts will be continued, but National is expected to look at each agreement to determine which will be kept over the long term, says a corporate spokeswoman. National's president Charles E. Sporek promises all customers depending upon any Fairchild product will continue to receive shipments.

Regardless of any promises, the merger apparently has struck sensitive nerves in the military chip-procuring

segment. Several defense contractors are said to be worried about their close working relationships with Fairchild's South Portland, Maine, operation. Some reportedly have filed complaints over the merger with the procurement officials in the Navy and the Defense Electronics Supply Center.

Initially, Fairchild will inject needed advanced bipolar technology—such as advanced ECL—into National's portfolio. Sporek, who left Fairchild in 1967 to join the fledgling National Semiconductor, believes the merger will complement his company's CMOS emphasis of this decade. He hopes the combination will be able to blanket the customer base, with National's emphasis on ICs for computer peripherals working with Fairchild's focus on technologies aimed at high-speed work stations, mainframes, and supercomputers.

About \$1 billion of National's total \$1.9 billion revenues in its 1987 fiscal year came from chip sales. Fairchild's sales are now about \$500 million a year. "It is a very strong combination. Fairchild's military business alone was worth the \$122 million price National is paying," says analyst Bill McClean of Integrated Circuit Engineering Corp. in Scottsdale, Ariz. "TI and Motorola both should have been bidding for Fairchild at that kind of price," he adds.

Actually, TI along with some other in-

MORE AND MORE CHIP MAKERS ARE EXPECTED TO MERGE

Industry observers expect to see more merger action among semiconductor manufacturers soon. They think companies around the world are very likely thinking hard now about making key acquisitions to avoid losing market-share standing.

The purchase of Fairchild Semiconductor Corp. by National Semiconductor Corp. provides a sterling example of why this is happening: National was No. 6 in military chip sales and Fairchild was No. 4, but by combining forces a company that is No. 1 in military markets—by far—is created. The recent merger of Advanced Micro Devices Inc. with Monolithic Memories Inc. builds a company that is No. 2 in military sales, but still slightly ahead of the two former leaders in this segment of the marketplace, Texas Instruments and Harris.

Making the merger mood more urgent is the limited number of viable combinations. "Semiconductor companies will start wondering—if they don't make a purchase, then someone else will," suggests Richard Skinner of Integrated Circuit Engineering Corp., a Scottsdale, Ariz., market analysis company. "Look at TI. This National-Fairchild combination puts National in roughly the same ballpark. If everyone

else is out buying, you'd better be out there buying too. Just like that, you could drop from No. 5 to No. 10 because of mergers."

ICE estimates that former military-chip leaders TI and Harris will achieve \$160 million each in 1987 military sales. The AMD-MMI combo is expected to rack up \$170 million in this market segment in 1987, with \$135 million coming from AMD, while the National-Fairchild total is expected to hit \$273 million.

"We might see more acquisitions as opportunities present themselves, but I don't think Motorola or TI should panic just yet," says ICE's Bill McClean. Strategic alliances with smaller chip makers are an alternative to the cost of a merger, he says. "TI is approaching it that way—with alliances to gain access to the technology without having to take on a business."

The track record for chip-company acquisitions has been dismal in the 1980s, but financial analyst Michael Gumpert of Drexel Burnham Lambert Inc., New York, thinks the failures can be blamed on the purchasers. "All the purchases by non-semiconductor companies—Schlumberger's deal for Fairchild, United Technologies Corp.'s for Mostek, Exxon's for Zilog, and so on—have ended up terribly.

I think these more recent ones [by chip companies] will work out much better."

By nearly all accounts, there are likely to be fewer semiconductor companies by the end of the century. Jack Beedle of In-Stat Inc. in Scottsdale, Ariz., predicts there will be only 10 to 12 giants shipping semiconductors, with 75 other smaller chip houses serving niches. "The big are going to get a lot bigger," he says. "The giants will have to be \$3 billion to \$4 billion in size. There will probably be four of those in Japan, four in the U.S., and a couple in Europe." Beedle thinks it's possible that the industry will see several attempts by corporate raiders to buy up chip houses and turn them into candidates for a surviving giant. "It's happened in the retailing and oil industries—why not here?"

Acquisitions also present one way of heading off legal tangles when strategic alliances turn sour. "Every U.S. manufacturer is having to decide whether it can afford to go solo or find a way of sharing the cost of business by alliances or mergers. It seems a safer course to buy up some company when you look at the recent legal tangles of intellectual property or ownership, like the AMD-Intel scrap," notes Michael Boss of Dataquest Inc. in San Jose, Calif. —J. R. L.



SILENCED. Don Brooks, Fairchild president, isn't talking.

tional, a supplier of high-speed silicon-gate CMOS and 4000-series metal-gate logic, had been considering an entry into the emerging arena of advanced-CMOS logic. The acquisition of Fairchild's Fact line takes care of that handily.

Overlaps exist in linear ICs, but many Fairchild products have the advantage of broad use in military markets. National executives are especially excited about getting Fairchild's linear arrays. And immediate paybacks are expected in ECL, where National has only \$20 million in annual sales, says ICE's McClean; the deal puts the firm on the same level as Motorola and Fujitsu. The big technology prize, according to most, is Fairchild's Aspect process—a contactless-transistor concept that reduces the size of devices, resulting in 2- μ m VLSI products rivaling the density of CMOS [Electronics, Sept. 4, 1986, p. 55].

ASIC BOOST. In ASICs, National is expected to retain its own CMOS gate arrays; in field-programmable logic it will pick up 10-ns ECL programmable array logic from the Fairchild portfolio that is more advanced than National's own. National is also expected to put to use Fairchild's biCMOS mixed technology, which is used to make 10- to 15-ns 256-K static random-access memories.

In the microprocessor arena, National is studying whether to market Fairchild's 32-bit Clipper chip aggressively. Some officials think it might overlap too much with National's own 32-bit 32000 family.

Some believe National should pick up the Clipper to complement its general-purpose 32-bit microprocessor. "I think they will discover it is a positive add-on to the 32000 offering," says Beedle at In-Stat. Others disagree. "It seems they would do best by pushing one or the other [Clipper or the 32000 line]. They probably won't kill one, but won't push it because of the cost of supporting a processor," says ICE's Skinner.

"From a market base, National-Fairchild has a major asset. They have a fairly broad base of loyal customers and it will be difficult for others to break business away despite the merger," Skinner adds. However, some distributors caution that if National completely drops the Fairchild name, it could end up losing customers loyal to Fairchild—enough to account for as much as 25% of Fairchild's sales.

Layoffs are expected, however. Initial estimates are about 10% of Fairchild's 9,000 workers could get laid off. Some analysts believe the number may be much smaller, if the chip business continues to recover this fall. □

interested chip makers did respond to a prospectus issued earlier this year by Schlumberger's investment agent, Lazard Frères in New York, sources indicate. But Brooks—a former TI vice president—suspected that the Dallas company was only seeking competitive information when it asked to review unannounced technology and products, according to a source within Fairchild. The information was denied, and TI made no offers.

The merger will give National a shot in the arm in both specific market segments and across its technologies. In application-specific ICs, the National-Fairchild merger would place the combined company "on the map, so to speak, as the seventh largest worldwide supplier," according to Michael Boss of Dataquest Inc. in San Jose, Calif.

"I don't think anyone really perceived National by itself as a broad-line supplier, although they like to say they are," says Jack Beedle of In-Stat Inc., Scottsdale, Ariz. "This will make them walk along the same footpath as Motorola and TI."

Perhaps most important to National, the merger is a viable defense against being acquired itself, notes Richard Skinner of ICE. "It is positive on both sides. With Fairchild under Schlumberger, there was always the chance that the second shoe would drop and there would be no more Fairchild," Skinner says. "National had been rumored to be an acquisition candidate for the last two or three years, because it is becoming more apparent that it is difficult to stay in the business when a large part of total revenues come from semiconductors."

Analysts predict that the deal, following on the heels of Advanced Micro Devices Inc.'s purchase of Monolithic Memories Inc., could touch off merger mania, with chip companies gobbling up other manufacturers in an attempt to grab market share (see "More and more chip makers are expected to merge," p. 44).

Right off, National fills some obvious holes in its own IC product line with Fairchild products. Both firms have Schottky and low-power Schottky bipolar lines, but National's Schottky lines serve different system designs than the higher-performing Fast bipolar logic from Fairchild. Na-

**COMING IN THE
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**THE INDUSTRY'S FIRST
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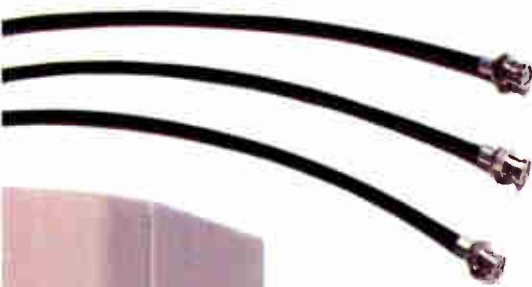
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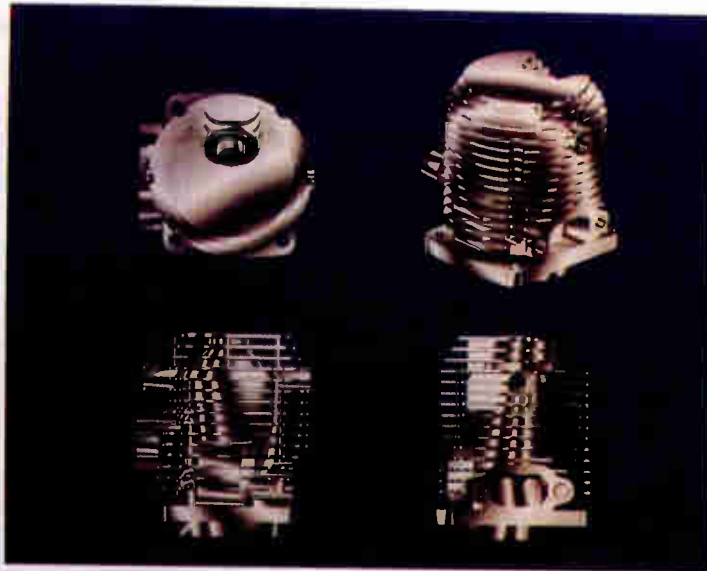
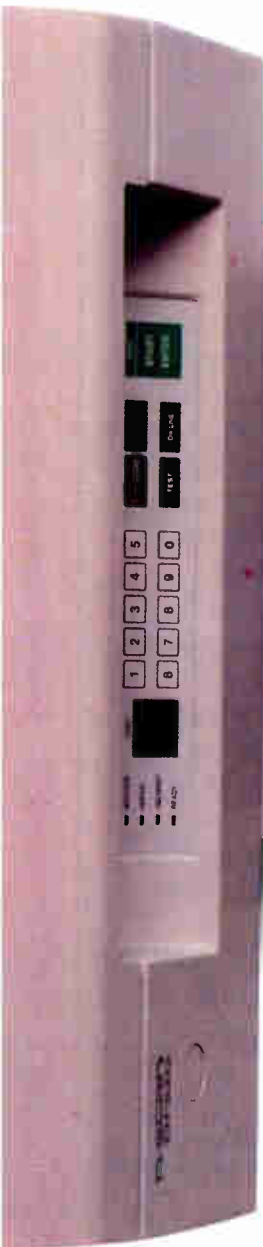
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COMMERCIAL QUANTITIES OF LSI GaAs ARE FINALLY HERE

VITESSE AND TRIQUINT GATE ARRAYS ARE SETTING THE PACE

by Larry Waller

Gallium arsenide LSI is moving into production at several companies and the chips should soon be rolling off lines in commercial quantities. Eliminating that long-term bottleneck comes none too soon, since even the biggest GaAs fans were beginning to have their doubts. One producer, in fact, Ford Microelectronics Inc., has even been predicting a growing production shortfall of GaAs devices of all types as demand climbs faster than the ability of GaAs houses to turn out these products (see graph, right).

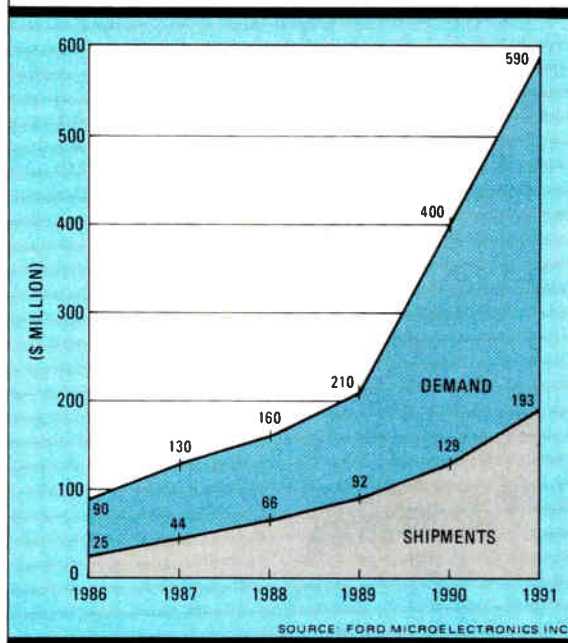
As GaAs fab lines get ready to turn out thousands of gate arrays on the heels of last year's first LSI product announcements [*Electronics*, Sept. 19, 1986, p. 61], one industry analyst, William I. Strauss, president of Forward Concepts Inc. of Tempe, Ariz., says that 1988 shipments, projected by Ford at \$66 million, "could easily double now that the production bottleneck appears to be broken." And the industry could at last dispel the notion that GaAs is more talk than action.

A pair of small companies seem to have taken the early lead in the production race—Vitesse Semiconductor Corp. of Camarillo, Calif., and TriQuint Semiconductor Inc. of Beaverton, Ore. Vitesse is in production with new 1,500- and 4,500-gate arrays and a 1-K static random-access memory (see p. 100); TriQuint has been delivering large quantities of a 3,000-gate array.

Vitesse and TriQuint are not running away from the field, however. Several other GaAs companies say they are at nearly the same stage. Among them are Gigabit Logic Corp. of Newbury Park, Calif., with 1,500-to-2,000-gate arrays, and Gain Electronics Corp. of Somerville, N.J., with offerings at the 1,700, 3,500, and 6,000-gate equivalent level.

Also, Ford Microelectronics, of Colorado Springs, Colo., is looking toward production of a 1-K SRAM with 2.5-ns cycle times, as is Texas Instruments Inc., whose Defense Systems and Electronics Group in Dallas is shipping samples of its 1-K chip. And Cray Research Inc., the supercomputer maker that has designed GaAs into its future Cray 3 system, is now farming out the fabrication to Gigabit Logic (see "Cray is still using GaAs—

GaAs SHIPMENTS DON'T SATISFY DEMAND



but not its own," opposite).

Vitesse got its edge, paradoxically, because it didn't get started until 1985, says president Lou Tomasetta. "We made a clean break with the past, starting with a clean blackboard," he says. Tomasetta himself goes back a ways with GaAs, to Rockwell International Corp., a GaAs pioneers, and then with startup Gigabit Logic in the early 1980s.

Vitesse's clean slate enabled it to make fast headway with the enhancement/depletion-mode process that experts say holds the key to building complex components. By combining enable/data-mode FETs in the same circuit, not only can densities be more than doubled over depletion FETs, but power needs can be cut to about one tenth, or about 0.1 to 0.25 mW/gate.

GOLD GONE. But Tomasetta credits a process innovation developed by Vitesse that gives much better control of the threshold voltage of GaAs, whose wide swings can spoil many chips on the wafers. "We got rid of gold as a material in the self-aligned gates," he explains, after gold was identified as the culprit causing temperature instability that changed threshold voltages, particularly at the 200°C to 300°C range. Junctions have to

withstand up to 900°C. Instead, Vitesse now uses what Tomasetta will describe only as "metalization similar to standard silicon processes."

That change has worked wonders in yields, but Vitesse also has made improvements in other areas, such as compensating for the piezoelectric effects exhibited by GaAs (which silicon does not have). In this technique, Vitesse damps the stress that builds into an electrical field in the rigid GaAs layers. Yields are "10 to 20 times better," says Tomasetta, which works out to nearly 50% for the first parts in quantity production, the processor family. The new gate arrays are expected to ramp up to

these levels, too, he says.

Vitesse's premier product is the new VSC1500, which it terms "an application-specific configurable gate array." It targets a generic data-processing function for fiber-optic and computer-to-computer data links, where speed is everything and the three-to-one advantage of GaAs over emitter-coupled logic offers a big advantage. With two functional sets of gates on a chip, the 1500 is more like a system than a simple gate array. The array, with 1,500 equivalent gates and 8,000 transistors, is a single-chip solution for multiplexing a number of parallel lines onto a single line with speeds of nearly 1.5 gigabits/s, and demultiplexing the signal back to parallel form.

The VSC1500, which is being designed into new equipment by a number of customers, has two major sections. The interface part is compatible with 100-K ECL signals and draws only 0.4 mW per gate, while the high-speed register cells have a 2-GHz toggle rate and interface at 1.5 GHz. The device can handle up to 22 inputs and 10 outputs for multiplexing, slightly less for demultiplexing, and it dissipates about 2.5 W. The VSC4500 gate array, with 20,000-transistor density, provides 800-MHz performance, in-

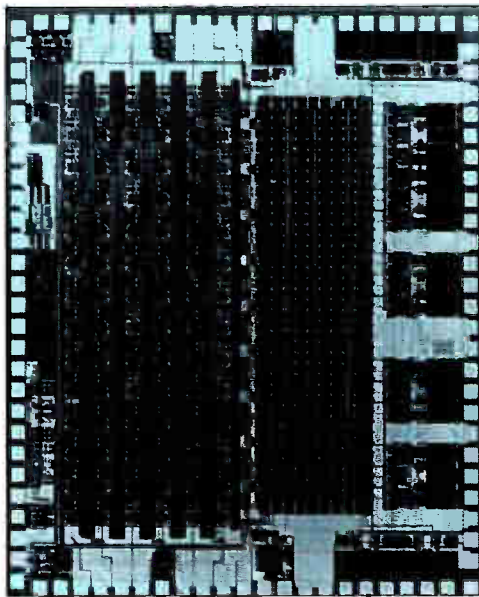
terfaces with TTL and ECL signals, and coexists with other types of chips and CMOS-oriented systems.

Vitesse had not said much about its new GaAs parts and manufacturing improvements until now, after the first customers had given the devices their stamp of approval. At TriQuint, management is still keeping quiet about details of its 3,000-gate product, preparing for a high-decibel announcement late this month before the GaAs Integrated Circuit Symposium, the major industry event that will take place Oct. 13 to 16 in Portland, Ore. At the same forum last year, TriQuint unveiled an early version of the enhancement/depletion GaAs array, which then could handle data rates up to 700 MHz [*Electronics*, Sept. 18, 1986, p. 59]. Performance subsequently has improved, industry sources say, and TriQuint is now shipping thousands of parts.

Both companies are wary because of damage done to the credibility of GaAs by the earlier failures of companies to make good on promises. That stigma is only now starting to fade, says Vitesse's Tomasetta. "There's extreme skepticism about gallium arsenide among customers that can only be beaten down with parts [put into their hands]," he says. Customers have to be convinced "that both Vitesse and GaAs are for real."

With thousands of gate arrays emerging from the fab lines on the heels of last year's first LSI products—GaAs versions of Advanced Micro Devices Inc.'s Am2900 4-bit bit-slice family [*Electronics*, Sept. 19, 1986, p. 61]—that perception can only strengthen. The processors have gone into volume manufacturing, along with the new parts.

CAUGHT UNAWARES. The reticence of Vitesse and TriQuint left analysts who closely follow developments in GaAs unaware that production quantities of LSI devices are at last available. "One of the limitations of gallium arsenide certainly has been the inability to manufacture it



at LSI levels," says Robert N. Castellano of The Information Network, a San Francisco market consulting firm. Castellano was one of the first GaAs watchers to note, in 1985, that until LSI-level parts came onstream in quantity, "those billion-dollar market projections [being made by other analysts] are totally unrealistic. GaAs must make it at the LSI level to be cost-effective." But his latest report on GaAs ICs speculates that the GaAs LSI era could be close at hand.

Not everyone, though, thinks digital GaAs is that close. Michael Gagnon, director of marketing at Anadigics Inc., a Warren, N.J., producer of analog versions, is skeptical about digital LSI GaAs. "I'm not sure that it really is here yet," he says. "I'd say it's 24 to 30 months off."

Vitesse's LSI work has at least one fan in William I. Strauss, the Tempe, Ariz., process and market consultant who is president of Forward Concepts Inc. "If Vitesse can truly ship in volume, they are head and shoulders ahead

NEW ENTRY. Vitesse calls this an application-specific configurable gate array.

of the pack," he says. Dropping gold from the enhancement/depletion-mode process is a bold move no others have seriously tried, Strauss says. "But I'll bet they will soon," he adds.

Production success also means that pricing is critical if GaAs is to break into the merchant market. Vitesse is intent on making its lines competitive with the ECL parts it intends to displace, says Tomasetta. Ultimately, the arrays will sell at "very little premium over ECL." A part three times as fast, for example, could initially cost triple its silicon competitor—"but not ten times," as is the case in many military and custom programs. Tomasetta is reluctant to give prices for Vitesse arrays, because each customer configures them differently. But a typical bit-slice 2900 processor sells for about \$50, or double the silicon version.

There is also the matter of second-sourcing, particularly since with any emerging semiconductor technology, commercial buyers like the security of having alternate suppliers available. Vitesse and Ford are moving slowly toward a partnership even though in the GaAs business that is a difficult proposition with enhancement/depletion-mode processing since each supplier does things differently. Also, older players are still shifting from depletion mode into the newer process. But alliances can strengthen both parties, help spur growth, and cut the costs of duplicated research in this still-fragmented business.

So Vitesse and Ford announced early this year an alternate-sourcing agreement for foundry services. The operation is not yet in place because details still have not been completed for compatible layout rules and processing. Tomasetta says he does not at present contemplate expanding the accord to cover the new Vitesse LSI family, because far tighter device densities are needed for them than for foundry work.

One major puzzle now remaining concerns the Japanese thrust in digital GaAs, where semiconductor giants NEC, Fujitsu, and Hitachi are leading the charge. Tomasetta says they have demonstrated mastery of E/D-mode processing and already can produce RAMs in quantity, "but we don't see any sign of them," he adds. The best guess by consultant Castellano is that those Japanese firms, which are computer manufacturers also, "are absorbing them internally and not selling them until low prices and high quality guarantee them a sizable portion of the world market, as with silicon." □

CRAY IS STILL USING GaAs—BUT NOT ITS OWN

One of the pioneers in designing with gallium arsenide, Cray Research Inc., is still committed to GaAs despite its decision earlier this month to cancel its next-generation MP supercomputer and the January shutdown of its internal GaAs fab line. The Minneapolis company's other design effort, the Cray 3, is due in 1989 or 1990, and it will rely on full-custom GaAs in the 300-to-500-gate range.

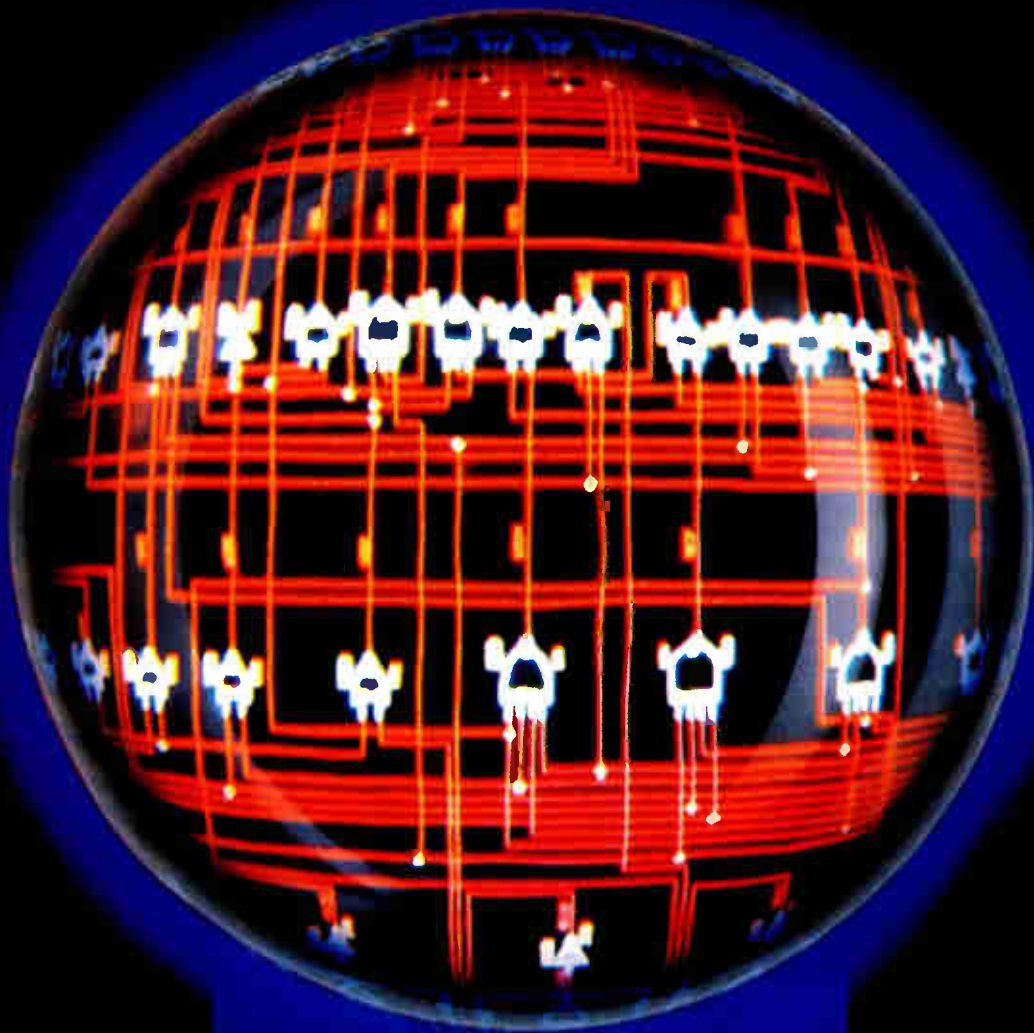
Cray has decided to farm all GaAs fab work out to Gigabit Logic Inc. of Newbury Park, Calif., in which it owns a part interest. As one source puts it, "It was Seymour [Cray]'s decision to go totally external rather than support two efforts. GaAs has been slow to develop,

and a lot of these [GaAs IC] companies have got to hang on, and they need support." Besides that, the small number of wafers needed during prototyping was deemed not enough to justify the internal effort—Cray is getting 5 to 10 wafers a week.

About 150 to 200 different types of logic devices will be used. The technology will be depletion mode, not enhancement/depletion mode, because "the commitment for the Cray 3 technology was made several years ago," explains a spokesperson. Cray is also planning to use some small GaAs memory devices in the Cray 3, on the order of about 1-Kbit size.

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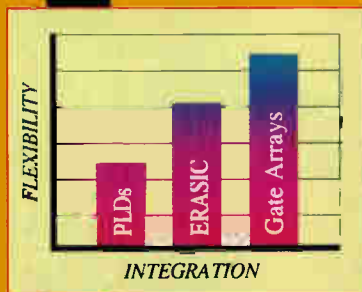


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INTERNATIONAL NEWSLETTER

JAPANESE TO PUT TWO-WAY DATACOM ON CABLE-TV NETWORKS

The Japanese Ministry of Posts and Telecommunications plans to use existing cable-TV networks for two-way data communications similar to the service available over leased telephone lines. Cable-TV systems can broadcast data now but are not capable of two-way communication. The ministry plans to set up a laboratory later this year with three manufacturers of CATV-related products—NEC, Toshiba, and Furukawa Electric—to work on two-way cable-based communications. The lab will develop technology for exchange hardware, for communications among users of different types of systems, and for maintaining communications privacy. □

FREQUENCY-DIVIDER CHIP R&D PROMISES RECORD SPEEDS

Astatic 8-to-1 frequency divider operating at up to 8 GHz—the highest ever for such a device made with relatively crude 2- μ m features—raises the prospect of much higher frequencies in chips made with finer lines. The chip was developed by researchers at Siemens AG in cooperation with Hans-Martin Rein, a professor at the Ruhr University in Bochum, West Germany. Siemens contributed self-aligned polysilicon bipolar techniques, while Rein optimized the circuit for voltage swings and transistor dimensions and parameters. The team is now developing 2- μ m dividers that work beyond 8 GHz and are intended mainly for optical communications. It hopes to do this by reducing the emitter-junction depth and the base width. □

PERSONAL-COMPUTER COMPATIBILITY PLANS PERCOLATE IN JAPAN

Astandard that's being proposed in Japan would establish guidelines for personal computers that are compatible with both IBM Corp.'s PC AT and NEC Corp.'s PC-9801, the best-selling Japanese PC. The proposed standard was formulated by a software-development organization with the goal of helping expand the Japanese PC market and boost software sales as well. The organization, called the Japan Personal Computer Software Technical Laboratory Inc., Tokyo, made the proposal because Japanese PC manufacturers are starting to build AT-compatible machines, separate lines of 9801-compatible systems, and, most recently, PCs that are compatible with both standards at once. Software developers foresee a market populated by dual-standard machines that achieve their dual compatibility in different ways, leaving program developers with major hardware-compatibility headaches. There are 47 software houses among the 54 sponsors of the PC Software Technical Lab. □

ISRAELI COMPANIES ARE OUT HUNTING FOR PARTNERS

The recovery of many of Israel's high-tech firms continues to be elusive—notably for two of its better-known electronics firms, which have set about looking for foreign partners to shore up their financial positions. Both Elscint Ltd., a producer of medical imaging equipment, and Scitex Corp., which makes computerized systems for printing and publishing, are continuing to lose money. Elscint, based in Haifa, reported a \$51 million loss on sales of \$132 million in the fiscal year ended March 31; the previous year it lost \$115.8 million on sales of \$124 million. Industry sources say that several of Israel's leading banks, which hold stock options, are looking for an international company to invest in Elscint. Similarly, the principal shareholders of Scitex are negotiating with leading foreign electronics firms in hopes of bringing in a partner. Scitex has had eight consecutive losing quarters: in the first half of 1987 it reported \$70.6 million in sales and a loss of \$7.4 million—but that's only a third of the loss for the same period in 1986. □

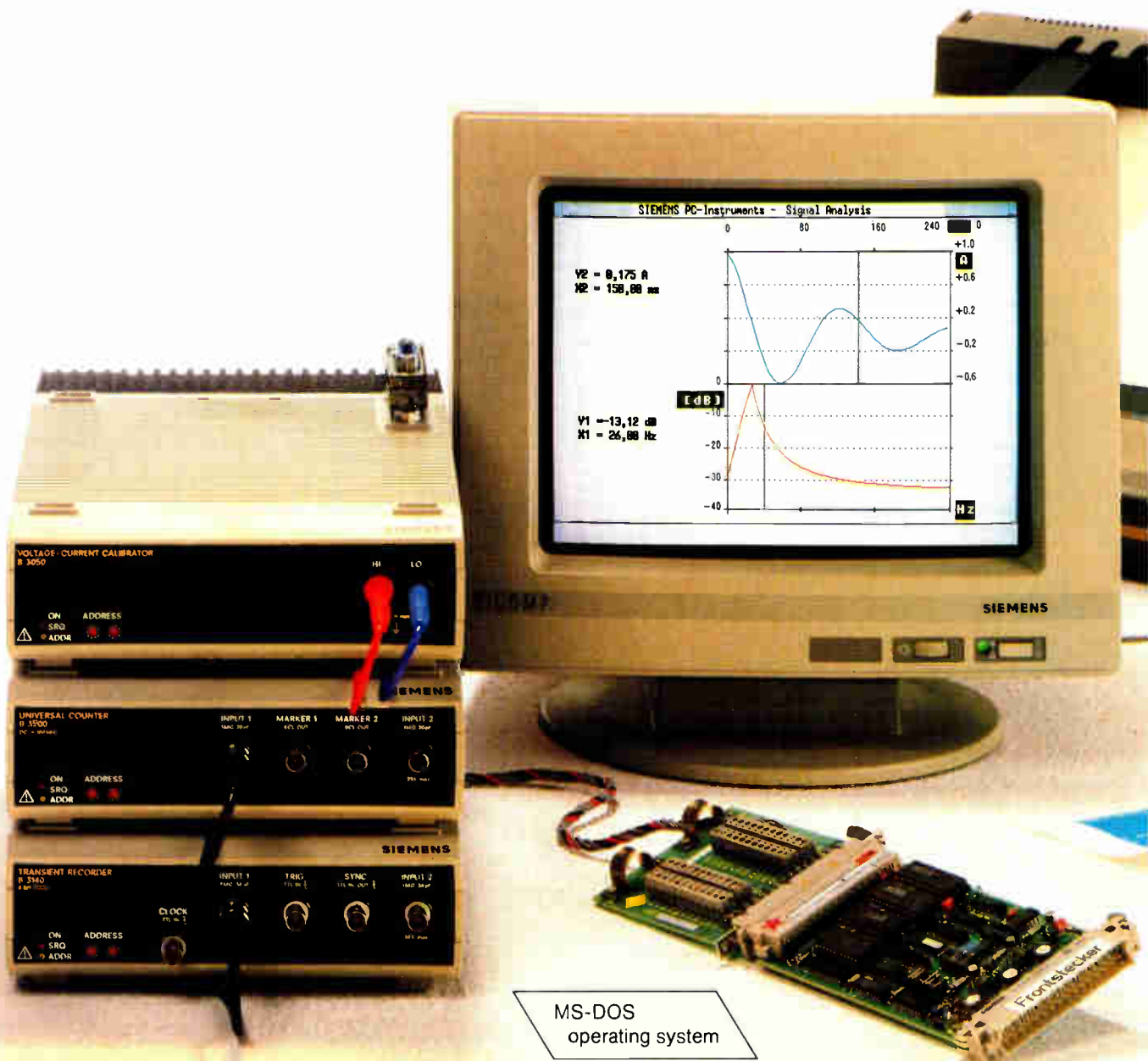
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INTERNATIONAL WEEK

SONY GOES TO 2-IN. FLOPPY IN PORTABLE

Sony Corp.'s new 2-in. floppy-disk drive has just been put on the market—incorporated into the Tokyo firm's portable Japanese-language word processor. The drive and its companion floppy disk, both announced in May, boast a 14.3-Mbit/s data-transfer rate and pack 0.819 Mbytes of formatted information on a single side [*Electronics*, May 28, 1987, p. 100]. The new word processor weighs only 3.97 kg; the weight drops to 2.32 kg when the thermal transfer printer, with a resolution of 32 by 32 dots per character, is detached. Sony hopes to sell 10,000 units a month at 115,000 yen each.

BRITISH PUSH FOR OPTICAL STORAGE

A drive has been mounted by PA Technology to put together a European consortium that will develop and market an erasable optical data-storage system. The Cambridge, UK, technology consulting firm has talks under way with a dozen leading computer firms and advanced technology houses—among them GEC, ICL, Germany's Nixdorf, Italy's Olivetti, Switzerland's Balzers, and France's LETI. For starters, PA wants the consortium to do a market study and then draw up a detailed proposal for a project to be carried out within the framework of the European Communities' Esprit advanced-technology program.

MICROWAVE OVENS ARE HOT IN JAPAN

Japan's housewives are fast warming up to microwave ovens. The Japan Electrical Manufacturers' Association reports sales of some 854,000 units in its domestic market during the first four months of the current fiscal year. JEMA now estimates growth

for 1987 will top 50%, a solid gain over 1986 growth of 37%. JEMA attributes the rapid growth to lower prices and a steady increase of single-person households. Microwave ovens have now found their way into around 52% of all households in Japan, an increase of 5% over 1986.

UK PICKS 4 BIDDERS FOR OA PROJECT

The UK Ministry of Defence has selected four consortiums to bid for two pilot schemes for a 10-year, multi-million pound contract for office automation. After an 18-month trial period with 200 terminals, the Ministry will select one consortium to build the Corporate Headquarters Office Technology System. The Unix-based system will serve some 24,000 users in more than 40 Ministry buildings throughout the UK after it is installed in the 1990s. Those selected to bid are consortiums headed by British Telecom, GEC, International Computers Ltd., and Software Sciences Ltd.

BUNDESPOST ADDS BERLIN TO FIBER NET

The Bundespost, West Germany's communications authority, has completed a vital link in its country-wide fiber-optic network—the one that connects West Berlin to West Germany proper, traversing 211 km of East Germany's territory. The Bundespost paid 35 million deutschmarks to the East Germans for cable laying and repeater installation. It will pay an additional 6.2 million DM a year to the East Germans for servicing the link. The cable can simultaneously handle some 58,000 voice channels.

BASF TO MARKET 5-HOUR VHS TAPE

West Germany's BASF AG will soon come out with what the firm says is the world's first VHS video cassette with

a five-hour playing time at standard speeds. It can thus record, for example, three feature-length movies in one pass. Designated VHS E300, the cassette uses chromium-dioxide-covered tape and boasts the same sound and picture quality as the company's 3- and 4-hour cassettes. BASF managed to pack the longer 5-hour tape into a standard-size cassette by reducing tape thickness to a mere 9 µm. The VHS E300 goes on sale in November.

ICL CONSORTIUM WINS RAF JOB

A British consortium headed by International Computers Ltd. has won the contract to supply a £37 million UKAIR high-security air command and control system to the Royal Air Force. The consortium, which has agreed to a 1991 delivery date, had to best bidders from other NATO countries to land the business. The system will tie work stations throughout the UK with central processing facilities at the RAF Strike Command at High Wycombe, and will form one of the first links in an air command and control system that eventually will cover the NATO countries in Europe.

SONY TO LAUNCH PORTABLE DAT UNIT

Sony will introduce a portable digital audio tape recorder in the domestic market in early December. The portable DAT unit has most of the functions of the DAT deck that Sony began to market in March, but in addition has a remote stereo microphone, battery, and programming clock. The new machine can run on line current with an external AC adapter. Initially, Sony expects to sell 3,000 units of the portable recorder, which weighs 1.85 kg, at 250,000 yen. The price is 25% higher than the DAT deck, of which Sony has sold 6,000 units.

IBM PC AT TO GET KANJI SOFTWARE

IBM's PC AT and its compatibles have caught on so strongly in Japan that a Tokyo software house will soon start selling a Japanese-language word-processing program for them. Information Technology Software Laboratory Co. licensed a package originally developed for NEC Corp. and Fujitsu Ltd. personal computers and adapted it for Japanese Kanji text on IBM and compatibles fitted with an EGA or Hercules display adapter. The price of the word-processing package will be 95,000 yen. ITL hopes to sell 1,000 packages initially. It also plans to develop a communications package for PC ATs.

MITSUBISHI TO MAKE DRIVES IN THAILAND

Mitsubishi Electric Corp. will begin to manufacture 5¼-in. floppy-disk drives in Bangkok, Thailand, in October, for sale primarily to the U.S. and other overseas markets. Through Melco Manufacturing (Thailand) Co., a joint venture with Kang Yong Electric Mfg. Co. of Thailand, Mitsubishi initially will produce 20,000 units monthly and eventually attain 100,000 units per month. This will bring Mitsubishi's overall production of floppy-disk drives, including 3½- and 8-in. versions, to over 3 million units per year.

RICOH TO SELL IBM COMPUTERS

Japan IBM Ltd., Tokyo, will supply to Ricoh Co. for resale its new personal computer series, Personal System/55, and the older departmental computer, System/36, starting in April 1988. The PS/55, which went on sale in May, is being made compatible with IBM's Personal System/2 and will be able to use both American and Japanese PC software products.

gin in April priced at 2,700 yen in lots of 10,000.

-Charles L. Cohen

Hitachi Ltd., International Sales Div. III, 1-5-1 Marunouchi, Chiyod-ku, Tokyo 100, Japan.

Phone 81-3-212-1111

[Circle 500]

MULTIPLEXER HANDLES 32 OUTPUT PORTS

Adacom 3270 Communications Ltd.'s CM-2132 32-port multiplexer for IBM Corp.'s 3174 controller handles all 32 output channels through a single coaxial, fiber-optic, or twisted-pair cable.

The comparable IBM multiplexer delivers 8 channels and cannot run on fiber-optic or twisted-pair cabling.

The multiplexer can be used alone as the source for a local distribution network or connected to another CM-2132 to send data to remote locations.



Using custom ICs has reduced the overall installation cost to about £100 per port. The CM-2132 comes with a modular rack and power supply. It uses interchangeable cards for channel configurations. Available now, the multiplexer costs £2,400.

Adacom 3270 Communications Ltd., Laser House, 4-8 Peartree St., London EC1V 3SB, UK.

Phone 44-1-251-5191

[Circle 701]

TESTER EMULATES ISDN TERMINALS

Idacom Electronics Ltd.'s IPT468 tester for Integrated Services Digital Network systems handles D-channel protocol testing by harnessing a dedicated Motorola Corp. 68000 microprocessor to 2 Mbytes of random-access memory.

The IPT468 can function as an ISDN terminal or network terminator during the monitoring of S or T bus interfaces. It includes a LAP-D (for Link Access Protocol-Version D) emulation program and two modular jacks for 192-Kbit/s S-bus interfaces.

An option lets users access ISDN B channels as well as the D channel. With it, the D-channel processor runs LAP-D while the B channel simultaneously runs another protocol such as X.25.

Available now, the basic unit costs U. S. \$22,500. With the B-channel option, it costs \$26,600.

Idacom Electronics Ltd., Edmonton R&D Park, 9411 20th Ave., Edmonton, Alberta, Canada T6N 1E5.

Phone (403) 450-2468

[Circle 702]

RACKS PROTECT FACTORY COMPUTERS

The Tecnorack series of 19-in. equipment racks from Schroff GmbH feature computer compartments with dust- and water-resistant glass doors to improve computers' survivability in harsh industrial environments.

The racks also have a compartment for the computer's keyboard, and one for power supply and peripherals. The equipment racks are available from stock. Prices depend on importing country.

Schroff GmbH, D-7541 Straubenhardt 1, West Germany.

Phone 49-7082-7940

[Circle 703]

POWER UNIT PROTECTS PCs FROM OUTAGES

An uninterruptible power supply from NPS Inc. protects personal computers and their data during power outages with a dc battery backup that delivers full-load power for 5 min.

Under 50% load conditions, such as when a modem or disk drive is not drawing power from the battery, the UP-0500 provides a reliable backup for up to 15 min.



Users are signaled by a buzzer and by a warning light when the battery is approaching the limit of its capacity. The UP-0500 also offers a small footprint. It measures 400 mm wide by 65 mm high and 400 mm deep.

The power supply is available now. Price depends on importing country.

NPS Inc., Mani Building, Shibuya 37-10 Udagawa-cho, Tokyo 150, Japan.

Phone 81-3-466-5400

[Circle 704]

PROJECTOR PUTS CAD ON 14-FT. SCREENS

The ECP Graphics video projection unit from Electrohome Ltd. operates with horizontal scan rates as high as 80 KHz to deliver high-resolution images on large screens.

The projector displays graphics created on computer-aided design and engineering software on projection screens 5 to 14 ft. across.

Images are projected through a single lens via three CRTs converged within a dichroic mirror cube. Up to 28 parameters such as brightness, contrast, convergence, and size can be stored in the system's memory for specific projector



applications. Focusing is manually controlled by three knobs, but the other parameters are under microprocessor control.

Available now, the ECP Graphics projector costs U. S. \$21,995.

Electrohome Ltd., 809 Wellington St., N. Kitchener, Ontario, Canada N2G 4J6.

Phone 519-744-7111

[Circle 706]

8-MBYTE RAM BOARD UPS PC PERFORMANCE

The SuperRAM memory board from ICCT Ltd. offers up to 8 Mbytes of random-access memory for IBM Corp. Personal Computers and compatibles, and a battery backup to preserve data even when the PC is switched off.

By using memory implemented in 1-Mbit CMOS chips instead of a conventional disk drive, the SuperRAM boosts performance of PCs to the level of PC-ATs and comparable microcomputers in applications that require extensive data retrieval.

Available now, the SuperRAM costs £595.

ICCT Ltd., Worcester House, Vintners Place, Upper Thames St., London EC4V 3AU, UK.

Phone 44-1-248-8895

[Circle 705]

GaAs CHIP INTEGRATES RING-MIXER DIODES

By implementing its gallium-arsenide diodes in a ring-mixer configuration on a single chip, Telefunken electronic GmbH ensures that each diode in the ring will have the same electrical characteristics.

The diodes feature a minimum voltage of 620 mV at 1 mA and a series resistance of 15 Ω at a maximum current of 5 mA. Type S450D comes in a TO50 package that contains the GaAs chip with four integrated Schottky diodes connected as a full ring. Type S455D connect two diodes into a half ring. Both devices are available now, and prices depend on the importing country.

Telefunken electronic GmbH, P. O. Box 1109, D-7100 Heilbronn, West Germany.

Phone: 49-7131-672230

[Circle 707]

SIEMENS

Short circuit eliminated

Card relay E

Siemens offers a highly extensive range of tried and tested electro-mechanical components, plus all the experience of a manufacturer who has consistently invested a great deal of know-how in developing and perfecting electromechanical requirements geared to market requirements.

The card relay E is a typical example. Fitted with one changeover, make or break contact, it provides reliable electrical isolation between light-current control circuits and heavy-current switching circuits – thus making a short circuit or “break-down” virtually impossible.

Other notable features include:

- High switching capacities (max. 4000 V/A)
- High dielectric strength (4 KV coil/contact)
- Immunity to external interference
- High overload capability

This makes the card relay E the ideal interface device in instrumentation, control and process engineering.

All the other features of the card relay E are detailed in a special publication. If you would like one, please use this journal's reader service or send us the coupon.

**Contacts you can rely on.
Electromechanical components from Siemens.**



Circle 131 on reader service card

World Radio History

Coupon: To Siemens AG, Infoservice 149/Z481, Postfach 2348, D-8510 Fürth 2
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We have developed these powerful options for the new 7610/C logic analyser. It is, of course, possible to update existing models to these new standards. This is one of the benefits of ENERTEC INSTRUMENTS' policy of continuous improvement, a real guarantee to protect your investment in our products.

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Enertec Instruments 5 rue Daguerre - 42030 St-Etienne cedex 2 France
Tél. 77.25.22.64 - Telex 300796

ENERTEC
Schlumberger

Circle 132 on reader service card

TRANSPUTER BOARD GIVES IBM PC 40 MIPS

Quintek Ltd.'s Fast4 add-on board for the IBM Corp. Personal Computer and compatibles uses four Inmos Ltd. transputer microprocessors to boost performance from 1 million instructions per second up to 40 mips.

Fast4 can also be used as a single-board computer and can be linked to other Fast4 boards to create transputer arrays of rings, grids, and hypercubes.

It runs all Inmos software without modification and supports both the 32-bit T414 transputer and the new T800-20.

Each of the four transputers has its own 1 Mbyte of random-access memory. This configuration allows one transputer to control the other three as a subordinate network.

Fast4 supports Fortran, Pascal, and C. It is available now. Price depends on importing country.

Quintek Ltd., Southfield House, 2 Southfield Rd., Westbury-on-Trym, Bristol BS9 3BH, UK.

Phone 44-272-628196

[Circle 708]

POWER UNITS BOAST PRECISE OUTPUTS

The 800 Series of switch-mode power supplies from Dewar Electronics Pty. Ltd. feature load regulation as low as 0.3% and line regulation as low as 0.2%.

Four models in the series range in output voltage from 5 V dc to 28 V dc and from 1 W to 70 W output power. Input power can be either 235 V ac or 117 V ac.

Both input and output circuits are fuse-protected high-efficiency switching regulators that are used to reduce heat-sink requirements. The power supplies are available now. Price depends on importing country.

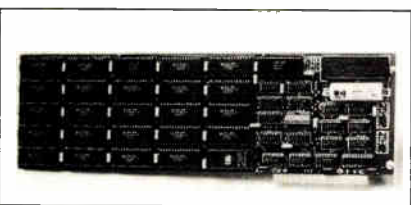
Dewar Electronics Pty. Ltd., P.O. Box 49, East Ringwood, Victoria 3135, Australia. Phone 61-3-725-3333

[Circle 709]

RUGGEDIZED RAM HOLDS DATA 10 YEARS

Two on-board batteries maintain data integrity on Innotech AS's CMOS random-access memory cards for up to 10 years. The Silicon Disk is available in 128- and 736-Kbyte versions.

Targeting industrial applications and other environments where magnetic-disk



storage is impractical, the product's integral I/O drivers are compatible with all versions of Microsoft Corp.'s MS/PC-DOS operating systems. Applications include process control, data acquisition, communications, and as a replacement for expensive bubble-memory systems.

In 100-unit lots, the Silicon Disk costs U.S. \$319 for the 128-Kbyte version and \$489 for the 512-Kbyte version. Large quantities can be delivered 30 days after receipt of order.

Innotec AS, P.O. Box 2080, N-Oslo 5, Norway.

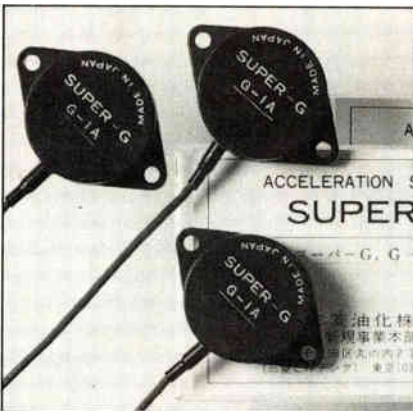
Phone 47-2-384120

[Circle 710]

ACCELERATOR SENSOR OPERATES ABOVE 100°C

The Super-G series of accelerometers from Hakuto Ltd. use piezo-plastic technology for both sensor and packaging to raise their operating temperature to above 100°C.

By constructing the transducer of a piezoelectric sensor, transistor, and amplifier, Hakuto eliminated the charge-am-



plifier stage required in conventional devices.

Used as sensors in adaptive or "active" automobile suspensions, condition monitoring of machinery, and other applications, the accelerometers can sense vibrations as low as 0.5 Hz.

The devices are available now. Price depends on importing country.

Hakuto Ltd., 1-1-3 Khinjukuku, Tokyo 160, Japan.

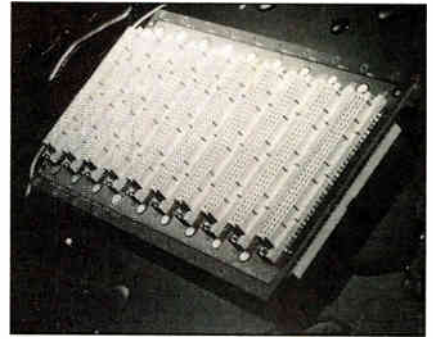
Phone 81-3-341-2611

[Circle 712]

BACKPLANES LIMIT CHANNEL CROSSTALK

Dage Ltd.'s 96 Bus series of backplanes for multilayer Eurocard boards ensure low crosstalk between channels by using plated through-holes connected at each signal plane to inner ground planes.

The backplanes come assembled and include DIN 41612 connectors. A patented tracking systems allows all 96 pins to be bused on both sides of the board, making double tracking unnecessary.



In addition to offering a wide choice of off-the-shelf configurations, Dage will also alter the backplanes to suit customer requirements. Two pitch options are available: 0.6 in. and 0.8 in. The number of board slots ranges from five to 28.

The 96 Bus series is available now. Prices vary, depending on the importing country.

Dage Ltd., Eurosem Div., Rabans La., Aylesbury, Bucks HP19 3RG, UK.

Phone 44-296-393-200

[Circle 713]

PULSE DIALER HAS LOW DRAIN CURRENT

The S2571 pulse-dialer IC from Austria Microsystems International GmbH features a 1-mA memory-retention current at 1.5 V. It operates from power supplies of 1.5 to 5 V.

The CMOS device converts information received from a phone's push-button handset to a format familiar to private branch exchanges.

The S2571 also offers an operating current drain of 50 μ A, on-chip memory for up to 32 digits, and a feature that allows additional digits to be dialed during a redialing operation.

The device is available now in an 18-pin dual in-line package. Pricing depends on the importing country.

Austria Microsystems International GmbH, Schloss Premstätten, 8141 Unterpremstätten, Austria.

Phone 43-3136-366-0

[Circle 711]

MICROSCOPE SPOTS WAFER DEFECTS

The Axiotron FL fluorescence microscope from Carl Zeiss GmbH helps users spot fluorescing particles, such as resist residues, on semiconductor wafers.

A high-pressure mercury lamp ensures a bright image, and an extensive selection of filter combinations makes the microscope capable of isolating a wide range of fluorescing particles.

The instrument will be available at the end of this year. Price has not yet been determined.

Carl Zeiss, P.O. Box 1369/1380, D-7082 Oberkochen, West Germany.

Phone 49-7346-203242

[Circle 714]

68000™

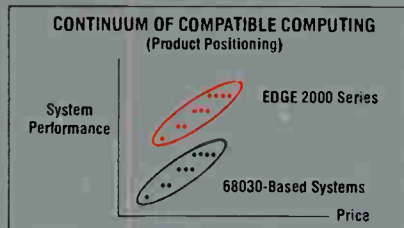
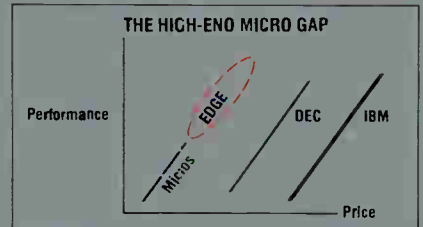
FAMILY UPDATE NO. 2

SEPTEMBER, 1987

OEMs CAN NOW OFFER HIGH-END, LOW-COST 68000 FAMILY COMPATIBLE PRODUCTS WITH 16 MIPS UNIPROCESSOR PERFORMANCE

By any measure, the 2000 Series VME™ board set recently unveiled by Edge Computer represents a quantum leap in 68000-compatible computing. Designed to fill the microprocessor high-end performance gap, the EDGE 2000 has driven performance costs down to about \$1K per MIPS (OEM quantities). The 2000 Series is available in a VME 3 high eurocard, 4 board set for easy product integration.

The EDGE 2000 is actually a CISC machine that operates with RISC-like efficiency. The specs are impressive. The uniprocessor version of the EDGE 2000 delivers 16 MIPS sustained performance and 60 MB/sec I/O bandwidth. At 1.4 cycles per instruction, the EDGE 2000's AIT (average instruction time) is lower than any other computer on the market today. Quad configurations of the powerful 2000, which supports scalable, transparent multiprocessing with one to four CPUs, are rated in excess of 56 MIPS sustained performance. The modular 2000 Series is based on a proprietary high-speed EDGEbus structure that offers 64 bit, 128 MB/sec parity protected transfers. Global memory can range from 8 MBytes to 1 GByte. Up to four standard or proprietary secondary I/O busses can be supported through dual I/O controllers. In spite of its incredible price/performance characteristics, the EDGE 2000 features a very small footprint (17"W x 29"H) to fit in a normal office environment.



EDGE SOLVES COSTLY SOFTWARE PORTING AND ARCHITECTURAL COMPATIBILITY PROBLEMS

Those OEMs and System Integrators with 68000-based products looking to develop high-end products outside of the 68000 family must overcome a number of costly, lengthy software compatibility obstacles. Porting the operating system, utilities and application software for target hardware, designing I/O interfaces and compilers are among the most formidable. The ongoing costs for support and maintenance of two architectures are equally important considerations. 68000-compatible products developed by Edge Computer let OEMs and System Integrators move ahead with a high-end compatible 68000 architecture to eliminate substantial software porting expenditures while still maintaining architectural compatibility.

EDGE COMPUTER FORMS SWISS SUBSIDIARY

Edge Computer Corporation has formed a European subsidiary in Lausanne, Switzerland. The new company was established to capitalize on the rapidly growing European demand by OEMs, System Integrators and Value-Added Resellers for compatible high-end Motorola 68000-based products. The subsidiary will be headed by Heiner Krapp, vice president of international operations.

EDGE
COMPUTER

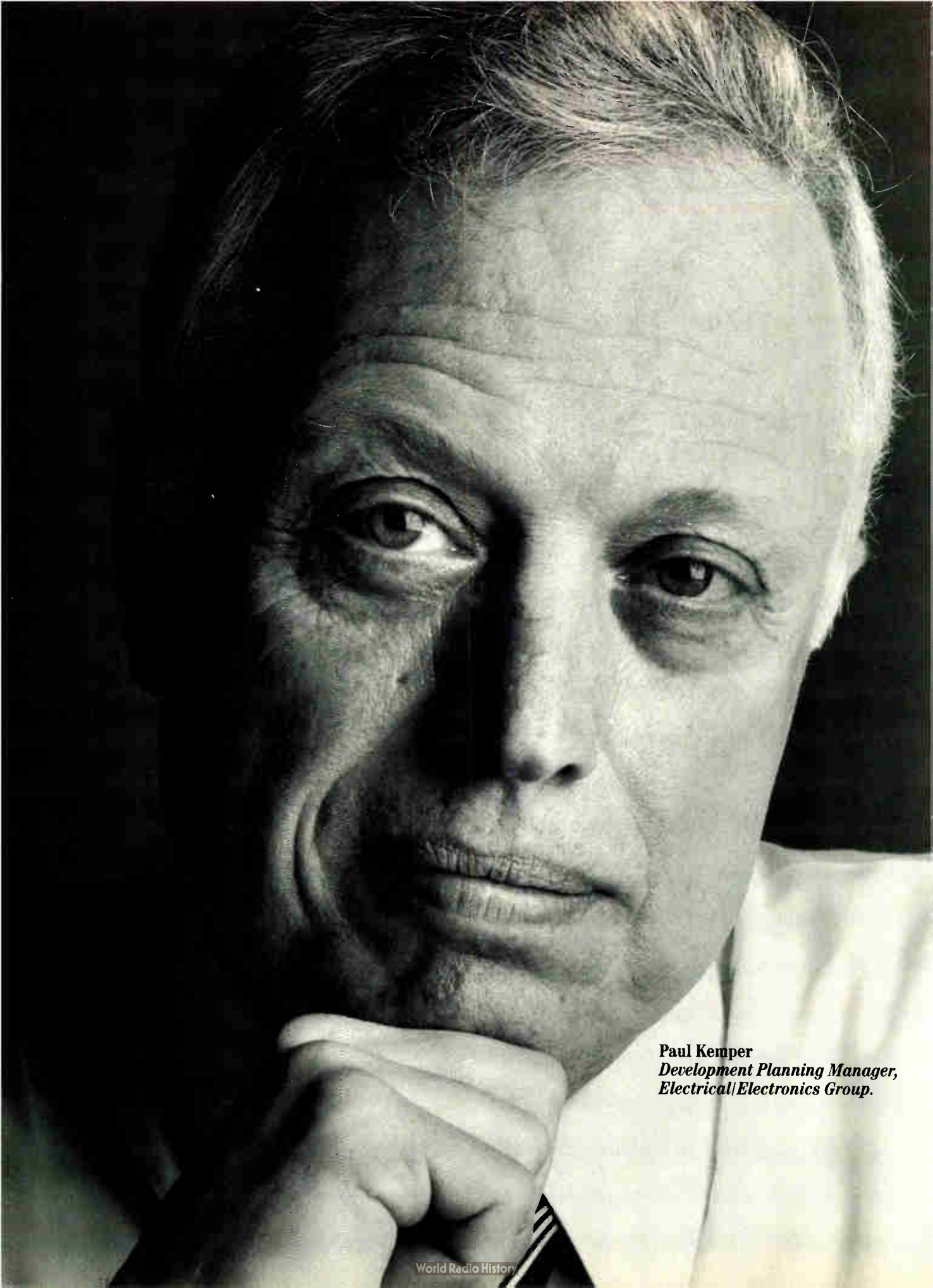


Compatible With Your Future

For more information, contact Pamela Mayer, Edge Computer Corporation, 7273 E. Butherus Drive, Scottsdale, AZ 85260, 602/951-2020. European Sales Office contact Heiner Krapp, 5, Avenue des Jordils CH 1000 Lausanne 6 Switzerland, 41-21-275315.

68000 and VME are trademarks of Motorola Corporation.

Circle 55 on reader service card



Paul Kemper
*Development Planning Manager,
Electrical/Electronics Group.*

“I never know where I’ll be next week...

When the phone rings, I go...

I was checking out of my hotel...

a Mr. Thompson calls...now I don’t know any Thompson, but I figure I have time to talk before my plane takes off...

Turns out the guy’s connectors are breaking...he wants to replace the plastic he’s using.

One or two of our plastics would’ve worked...but he really had some fundamental design flaws...so I suggested changes...knowing full well they’d help the competitor’s plastic perform properly.

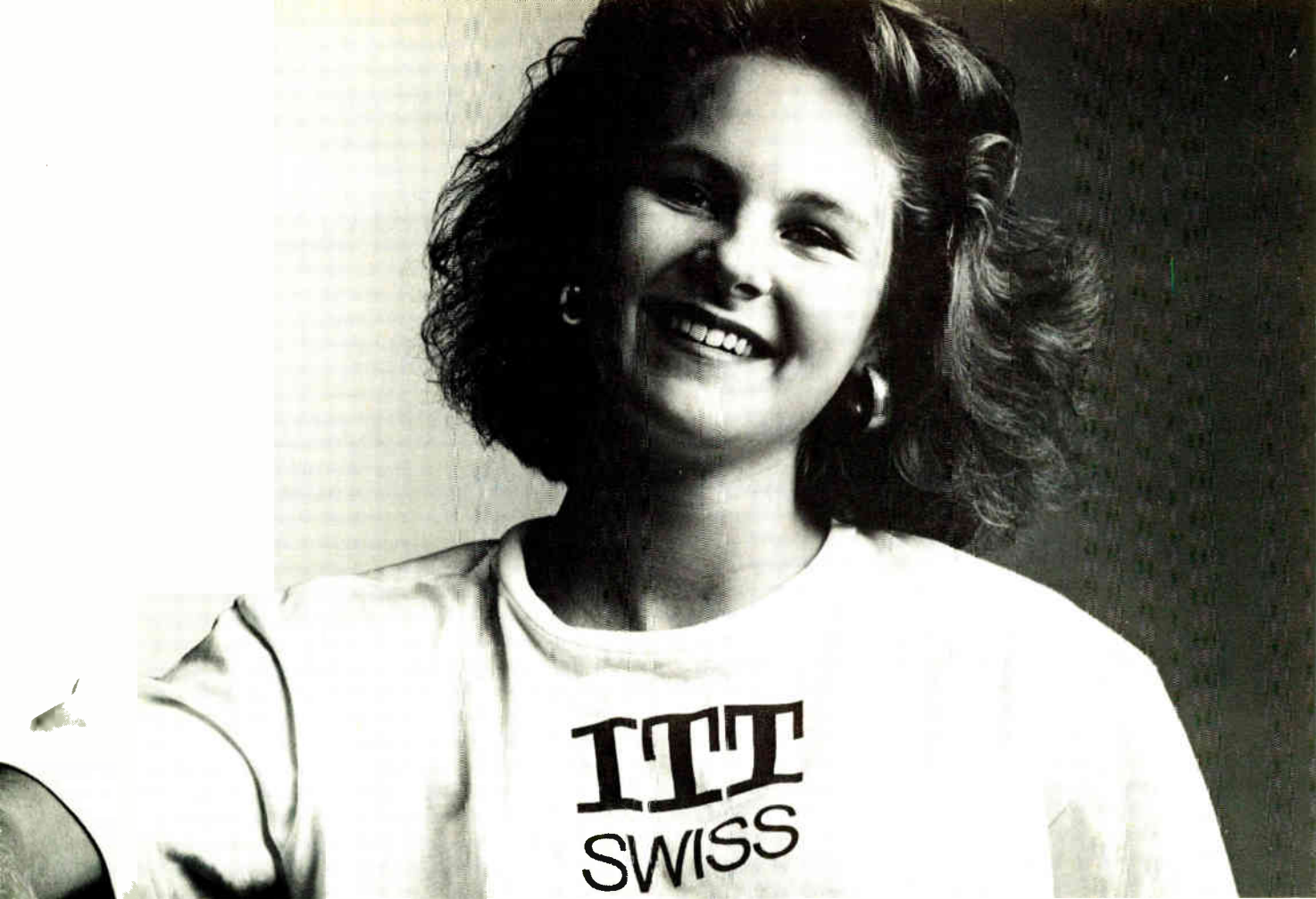
No. I didn’t make a sale...didn’t make my plane either...but I guess I made some kind of impression...got a call from one of our sales reps last week...Thompson’s using our plastic now...in a design that looks real familiar.”

DuPont Engineering Plastics

It all starts with a phone call...(302) 999-4592



Circle 57 on reader service card



**THE ONLY DIFFERENCE
BETWEEN AN
ITT SWISS RELAY AND AN
ALCATEL SWISS RELAY
IS THE NAME.**

But you probably already knew that. ITT Swiss relays now have another name on the front. You can't miss it. The name Alcatel Swiss is in the same place where ITT Swiss was.

So, what's different? Not much. And definitely less than our competition would have liked.

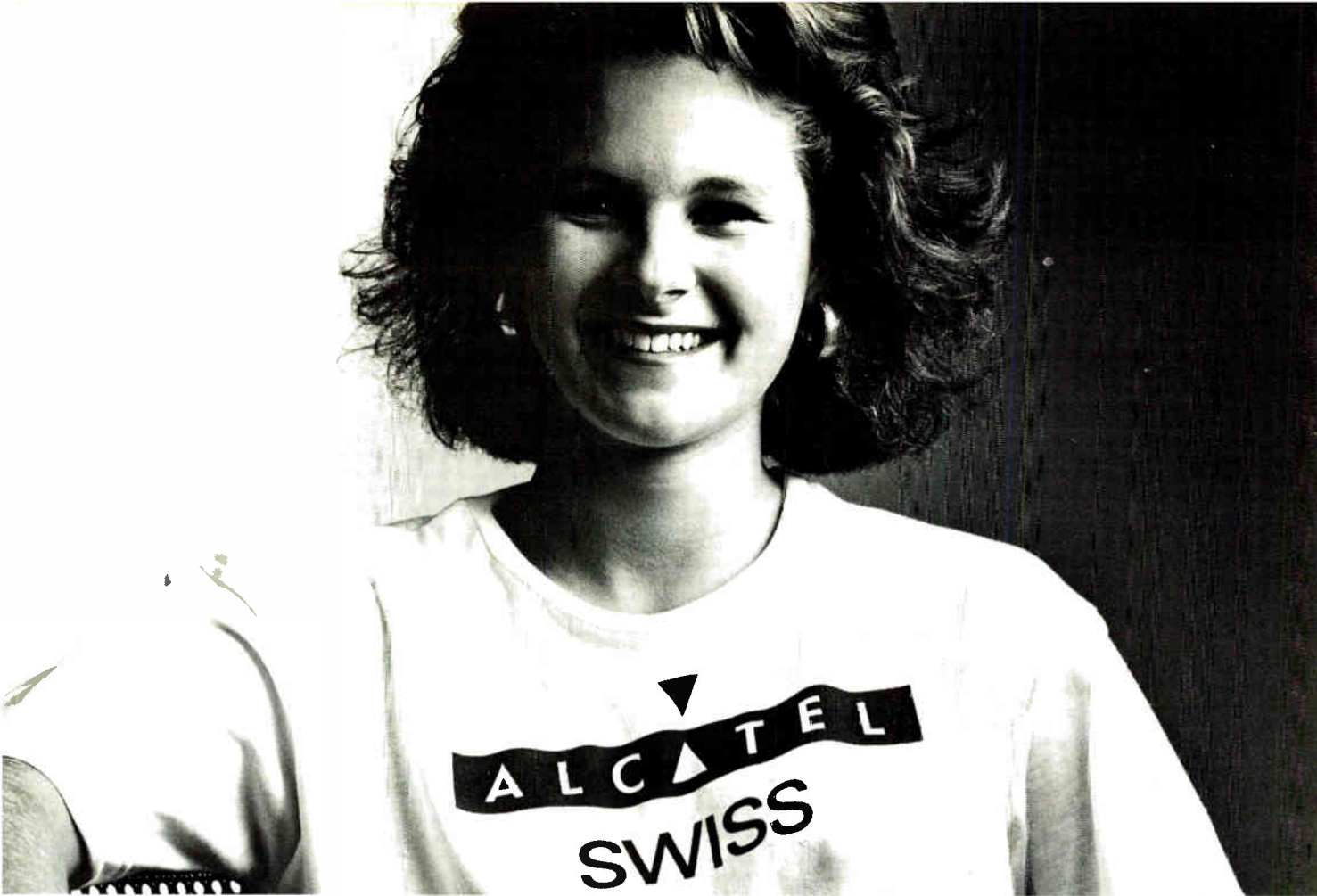
Some details: Alcatel: Despite its youthfulness, this European association of enterprises has become quite well known.

Alcatel's goals have always been set quite high, a fact which is not really surprising when we consider the competition from America and Japan—not to mention that from the Far East.

So it must be clear that our competence in the manufacture of relays is a matter of great importance in this situation. We can offer a list of plus points which will continue to be available in the future, of course.

Indeed, these plus points are precisely those points necessary to meet the competition of today and tomorrow. Therefore they will be changed very little.

Our relay customers know what we mean. If you are not one of them, then this information will be even more important for you. Allow us to make a few points:



Dr. J. Chli 780 STR

PZ Relay: a wonderful example of our pioneering in this field. This was the first relay which could be soldered directly into P.C. boards. This is the only series in the world with a choice of 2, 4 or 6 changeover contacts.

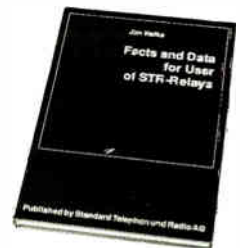
SM Relay: Another typical pioneering effort of our relay laboratories featuring extremely flat profile and an extremely quiet operation. Completely plastic coated, this unit exhibits (in contrast to the competition) exceptionally good anti-shock and anti-vibration characteristics as well as resistance to tropical and wet conditions.

MT Relay: a monostable relay that has no peers. Non-polarized. Suitable for very high packing density. Compatible. Never needs re-adjustment. A guaranteed 10 million changeovers under dry conditions. Functionally guaranteed within a temperature range of -55 to +70 degrees centigrade. Failure ratio guaranteed to be under 0,5% over the lifetime of the relay. Can be supplied for coil voltages up to 48V and 150 mW capacity!

We are sure you will agree that is an impressive list of relay plus points.

Now it should be clear just why, except for the name, it is the same old range of products. After all, they are still the latest state of the art.

Everything you have always wanted to know about relays but didn't know where to find the information, has been compiled in the new STR Relay Handbook. A competently written indispensable practical aid for everyone who wants to be on top of everything in the world of relays. We would be happy to send you one - free of charge, of course.



Company

Address

Responsible Party

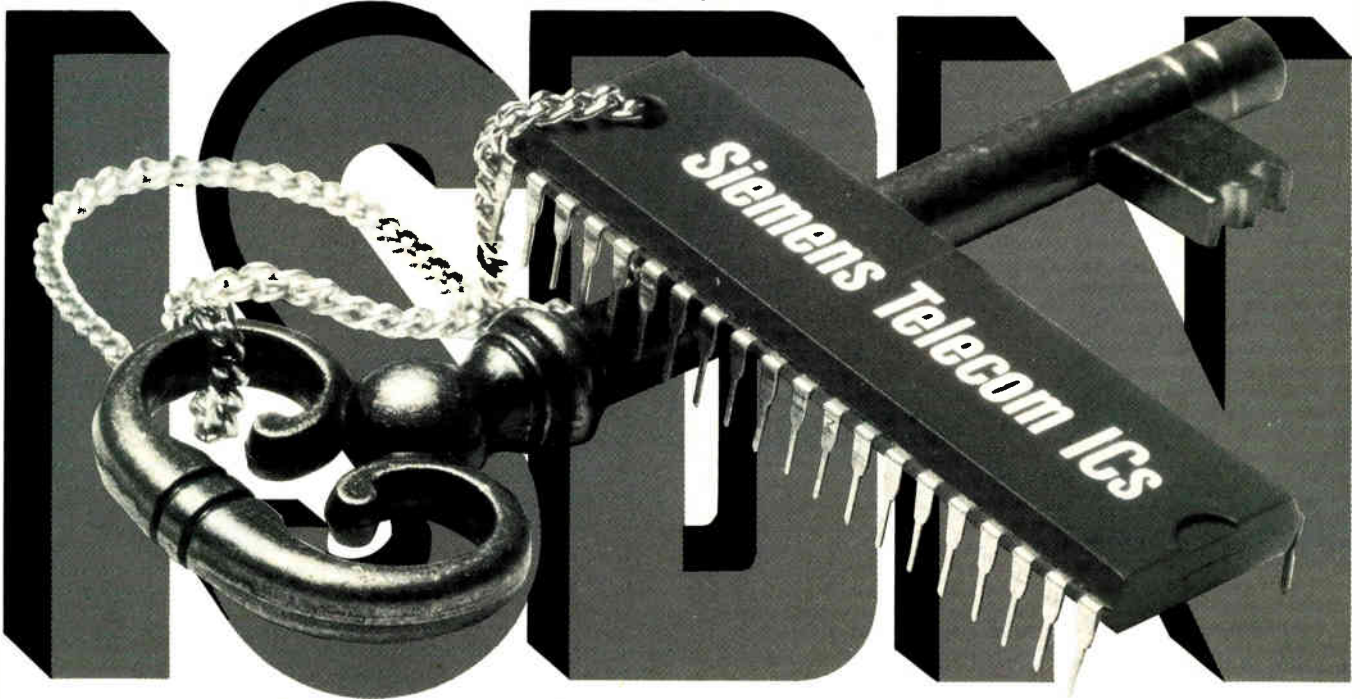
EW 9, 17

Standard Telephon und Radio AG, CH-8055 Zurich
Friesenbergstrasse 75, Switzerland


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SIEMENS

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ISDN SOLUTIONS TO THE DESIGN CHALLENGE

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Each seminar will feature different speakers, and cover a range of topics including:

- Field Trials
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- Future ISDN ICs
- Design specific presentations
- Applications presentation and demonstrations on new ISDN evaluation boards
- Software-Level 1 front end drivers, Level 2 LAPD, and Level 3 Call Control (both generic and switch specific)
- ISDN testers

Siemens Seminars... Where and When for ISDN

Boston, MA	-	October 26 & 27
Los Angeles, CA	-	November 3 & 4
Chicago, IL	-	November 10 & 11

For additional information on the seminar of your choice and for hotel details call the number below.

Registration Fee of \$125 per person also includes comprehensive literature packet (copies of presentation, technical product information, and more): continental breakfasts, luncheons, and dinner with keynote speaker. Seating is limited, so don't delay!

**Register today for the
Siemens ISDN seminar nearest you:
CALL 1-800-227-1817 Ext.96**

INSIDE TECHNOLOGY

PROGRAMMABLE LOGIC DEVICES: FASTER, DENSER, AND A LOT MORE OF THEM

After spending nearly 20 years as a low-end commodity part, the programmable logic device is going high-tech. CMOS ultraviolet-erasable and electrically erasable PLDs are moving in on the bipolar fusible-link parts that have long dominated the high-performance market—and new architectures, such as static RAM-based parts, are appearing. EPLDs and EEPLDs now boast speeds that only bipolar parts had been offering, and bipolar devices are responding by getting even faster. The CMOS parts also are leading the race toward greater densities: the PLD is beginning to encroach on gate-array turf as densities push into the 10,000-gate range. Equally important, the PLD is moving from a commodity part into the application-specific and function-specific realm. The upshot is that users are finding PLDs now offer them a whole new range of options from which to choose.

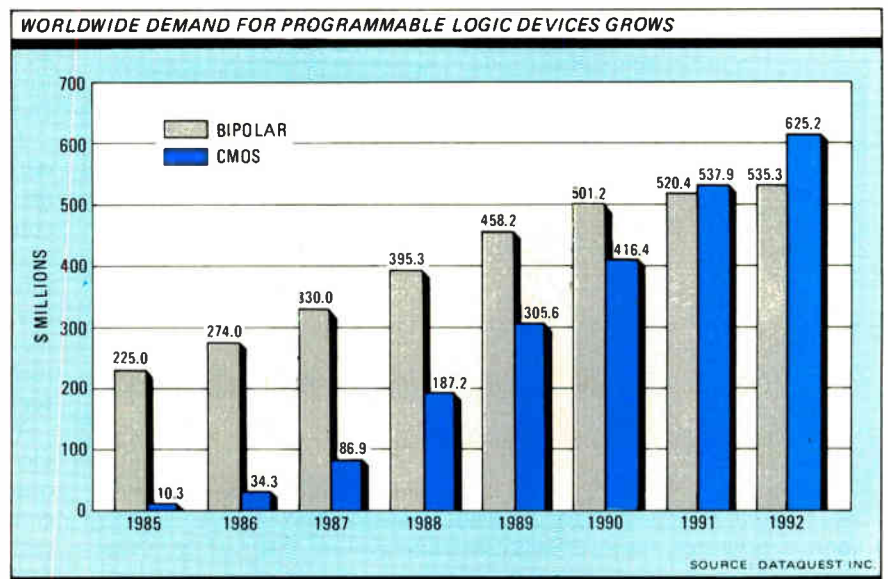
As CMOS makers hone their processes, EPLDs and EEPLDs are speeding up fast—delays are dropping from 40 to 50 ns down to 20 to 25 ns. In response, bipolar manufacturers are applying advanced processes to push TTL-compatible PLDs down to 10 to 15 ns and emitter-coupled-logic PLDs below 10 ns.

Long the province of Monolithic Memories and Signetics, the PLD is suddenly moving into the limelight as the number of makers and options explodes. Numerous contenders are leaping into the fray—from traditional semiconductor manufacturers, such as Advanced Micro Devices, Fairchild, Intel, National Semiconductor, and Texas Instruments, to relative newcomers: Altera, Cypress, Exel, Lattice, PLX Technology, and Xilinx. According to Dataquest Inc., of San Jose, Calif., the market will swell from \$235 million in 1985 to \$417 million this year, and to over \$1 billion by 1992 (see chart, right).

As the market expands, it is

A host of new choices for users: EPLDs and EEPLDs with speeds that rival bipolar PLDs and densities that rival gate arrays; application- and function-specific parts

by Bernard C. Cole



branching into niches: low-power medium- and high-speed CMOS; TTL and blazingly fast ECL; three flavors of density: low (300 to 800 gates), medium (1,000 to 2,000 gates), and high (3,000 to 9,000 gates); and more-complex 28- and 40-pin devices with flexible macrocells and hidden registers. Interest is growing in more complex structures, such as the programmable-AND, pro-

CMOS is pushing PLD densities into the 5,000-to-10,000-gate range, encroaching on the territory that's dominated by gate arrays

grammable-OR logic array and the programmable logic sequencer. And there are movements away from simple single-level designs based on AND-OR logic and toward more complex multilevel schemes based on NAND-NAND and NOR-NOR logic.

As traditional AND-OR-based programmable logic devices reach their density limits, several companies are looking for ways to push PLD gate counts into the 5,000-to-10,000 range, the territory of as much as 80% of all gate arrays, says Wes Patterson, executive vice president at Xilinx Inc. in San Jose, Calif. Xilinx is first off the mark. This week it introduced a new family of its SRAM-based Logic Cell Arrays incorporating an enhanced architecture that promises to push programmable logic to densities as high as 9,000 gates later this year (see p. 69). And betting that this approach is the way to higher PLD densities, Monolithic Memories Inc. is going into production with the first in a series of devices using technology acquired from Xilinx.

Not to be outdone, Altera Corp. and Cypress Semiconductor Corp. have entered into a five-year technology-exchange agreement aimed at developing high-density PLDs. The first devices resulting from this agreement are coming later

this year, says Rodney Smith, president of Altera. Designated MAX, for multiple array matrix, the family of products from the Santa Clara, Calif., company will extend traditional AND-OR-based EPLD densities to at least 5,000 equivalent gates. And scheduled for mid-1988 are UV-erasable CMOS versions of Signetics' programmable macro logic, which are expected to reach densities of at least 7,500 gates.

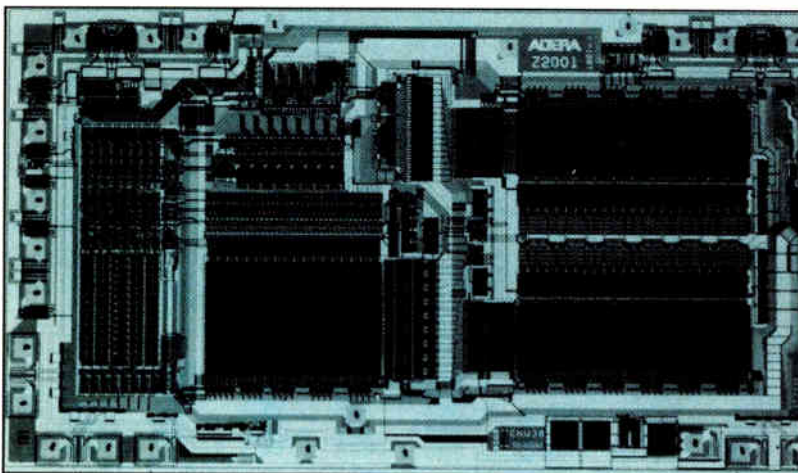
Aside from density, one of the more surprising developments has been the speed with which CMOS PLDs have penetrated the market, following the introduction of the first such device in 1985 by Altera. During that first year, total sales of CMOS PLDs amounted to only \$10 million—less than 5% of the total market, says Dave Laws, vice president of marketing at Altera. But by 1992 Dataquest expects CMOS PLDs to hit total yearly sales of \$625 million, versus \$535.3 million for bipolar PLDs. And with the exploding market for CMOS PLDs, the competition has blossomed. Joining Altera in UV erasables are Cypress, Harris Semiconductor, Intel, National, Panatech Semiconductor, Sprague Solid State, and VLSI Technology Inc.

One measure of the impact of CMOS EPLDs is seen in the CMOS programmable logic entries introduced in recent months by the industry leader in bipolar PLDs—Monolithic Memories Inc. of Santa Clara, Calif.—and its crosstown rival, Signetics Corp. Monolithic Memories has introduced CMOS versions of its original 20- and 24-pin family of programmable-array-logic devices as well as a CMOS version of the Advanced Micro Devices bipolar 24-pin AmPAL22V10. The latter is an advanced PAL device that extends beyond the simple programmable-AND, fixed-OR array of Monolithic Memories' original PALS. It incorporates 10 I/O macrocells, allowing implementation of very complex glue logic and state-machine designs.

Signetics' new CMOS entry is a 24-pin UV-erasable version of its programmable logic array, a two-level device with both a programmable-AND and a programmable-OR array. With 24 AND and 22 OR gates, the PLC473 allows the user to implement extremely wide OR-gate functions, up to 24 inputs per OR term.

In addition, in the past six months application- and function-specific PLDs have appeared. These devices combine the user-configurable flexibility of general-purpose PLDs with function and performance optimized for a specific target application. Under development by a number of companies are PLDs aimed at such applications niches as sequencers, transceivers, bus interfaces, and the like.

What's surprising is not that such devices evolved, but that it's happening so quickly. "Traditional PLDs are basically commodity-type devices, standard configurations of logic produced in jellybean-like fashion," says Altera's Laws. "But just as



1. LOGIC SEQUENCER. Altera's EPS448 uses a programmable-AND, fixed-OR architecture and can be configured with microcode, a truth table, or logic equations.

standard ICs moved with increasing levels of integration from commodity-logic functions to application-specific devices for telecommunications and disk drives and bus-interface circuits, so is a similar evolution occurring in programmable logic. In standard ICs, this evolution took place over decades, whereas in programmable logic it is taking place over a period of a few years or months, mostly in response to the mounting needs—indeed, demands—of users.”

One of the first application-specific areas that Altera, AMD, Monolithic Memories, Intel, and others have focused on is programmable logic sequencers, a traditional PLD niche long dominated by Signetics [*Electronics*, Jan. 27, 1986, p. 25]. In the original devices introduced by Signetics, PLA architectures were combined with logic to perform such dedicated functions as interface protocol control, sequence detection, peripheral control, timing generation, and a variety of sequential circuit designs. In the past few months the newcomers have entered the market with their own variations, but they’re using the much simpler and faster programmable-AND, fixed-OR PAL-type architecture.

For example, from Altera comes the EPS448, a stand-alone microsequencer [*Electronics*, March 19, 1987, p. 76], which combines in a single 28-pin PLD a branch-control-logic front end with an EPROM-based 2910 bit-slice microsequencer and pipeline register (see fig. 1). According to Laws, the branch-control logic provides the equivalent of 768 product terms, while the 448-word-by-36-bit EPROM-based microcode sequencer provides the functional equivalent of a 2910 sequencer, four octal registers, eight MSI/SSI TTL components, and five high-speed 512-by-8-bit PROMs or EPROMs. Fabricated with 1.5- μ m CMOS split-gate EPROM technology, it can operate at clock rates up to 30 MHz. The advantage of the Altera approach, says Laws, is that it can be configured with either the microcode techniques of bit-slice devices or with the truth table or logic equations of programmable logic devices.

Another approach, from Monolithic Memories, combines a PAL-based array and a programmable ROM array in the same device. The 24-pin PMS14R21/A is the first in a family of dedicated 20- and 25-MHz bipolar programmable sequencers. This combination offers designers an efficient yet powerful structure for implementing very large state machines, says Andy Robin, the company’s director of programmable logic device marketing.

In this design, a PAL array with 14 inputs, two active-high outputs, and eight product terms per output acts as the control element, providing conditional input decoding. Eight external inputs determine the next state, and two

connections to the PROM array allow up to four branches from any state. The PROM array serves as the execution element, storing both state information and outputs. It holds up to 128 possible states—twice as many as the programmable sequencers available from Signetics, Robin says.

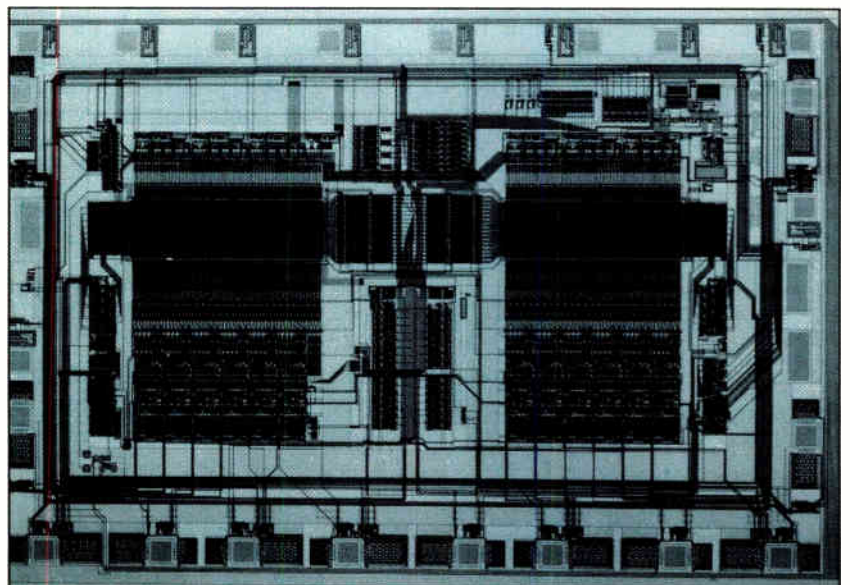
Still a third variation is the AmPAL23S8, a 20-pin bipolar PAL-based sequencer from Advanced

Standard ICs took decades to move from commodity logic to application-specific functions, but for programmable logic devices this evolution is happening far more quickly

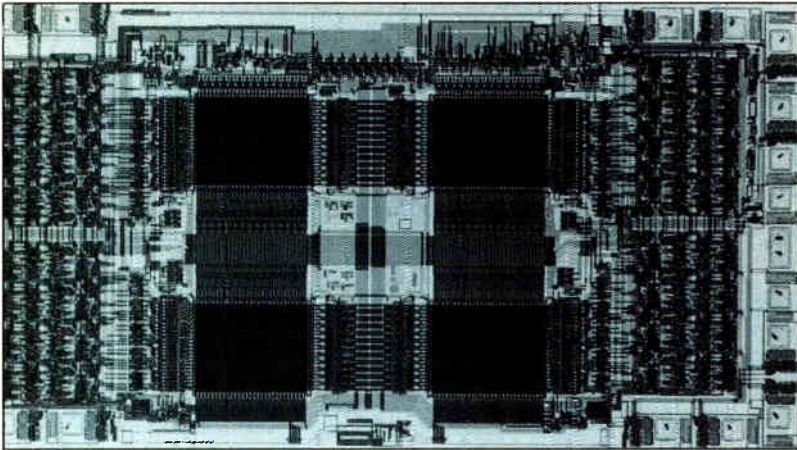
Micro Devices Inc. that combines in a single device the logic required to do a variety of sequencing functions and many of the features of its bigger brother, the 24-pin 22V10—including four output logic macrocells, four output registers, and six buried state registers. Although eight registers are the common maximum for devices with this pin count, the addition of six buried registers allows such internal functions as control sequencing, timing, and arbitration for up to 64 states, freeing up valuable I/O pins for other logic tasks.

The 23S8 has nine dedicated inputs, four bidirectional I/O pins, and 10 internal feedback paths, for a total of 23 array inputs and 135 product terms. The device will be offered in two speed ranges: one has a 20-ns propagation delay, with a 33-MHz clock rate and a 40-MHz internal rate; the other features a 25-ns propagation delay, with a 28.5-MHz external rate and a 33-MHz internal rate.

Other vendors entering the application-specific market have focused their attention on the glue logic necessary in many advanced 16- and 32-bit



2. HIGH PERFORMANCE. Intel's 5AC312 is aimed at such logic functions as decoding, bus arbitration, and memory addressing in 16- and 32-bit microprocessor applications.



3. FLEXIBLE. AMD's PAL-based AmPAL29M16 features 188 product terms and 16 I/O macrocells.

microprocessor designs, particularly in regard to bus interfacing. One of the first to enter this area is Intel Corp., which recently introduced the 5CBIC, a bus-interface control EPLD fabricated with the company's CHMOS II-E process. The part is aimed at replacing as many as four SSI/MSI TTL components or two 20-pin bipolar PALs at the interface between the CPU and its peripherals. The 5CBIC contains a bus-management unit and a programmable logic unit, says Larry Palley, product marketing manager for Intel's programmable logic device operation in Folsom, Calif.

The bus-management unit incorporates all of the logic necessary for synchronous or asynchronous data transfer on as many as three byte-wide buses. It holds user-programmable options for real time or latched data transfer. The programmable logic unit, on the other hand, contains eight programmable macrocells to allow users to implement their own interface requirements.

Following on Intel's heels was Altera, with the EP1400, a 40-pin, 1.5- μm CMOS EPLD aimed at replacing the glue logic sitting between the peripherals surrounding the CPU and the external system environment. It has a 25-MHz clock rate and incorporates the equivalent of 1,400 EPROM-based two-input NAND gates. The EP1400 is a programmable bus-peripheral interface PLD containing a dedicated byte-wide bidirectional bus-interface port, an I/O buffer, and 20 general-purpose macrocells that can be programmed to be any of four types of flip-flops. It also boasts either synchronous or asynchronous clocking, individual output enables for each macrocell, independent pin- or macrocell-feedback lines, and up to eight product terms per macrocell.

This month, Intel introduced the 5AC312 (see fig. 2), a more generic PAL-type device optimized for use in high-performance 16- and 32-bit microprocessor applications. The 24-pin 1.0- μm CMOS device is aimed at replacing the TTL-logic standard PAL-type devices that are now used to implement such logic functions as decoding, bus arbitration, and memory addressing (see p. 65), says product line manager Karlheinz Weigl.

Also due out this month is the PLX448 from

outputs to act as true transceivers, says company president and founder Michael Salameh. Two independent clock inputs are also provided. The 448 has a propagation delay of 25 to 35 ns when operating at a 28.5-MHz clock rate.

Walking the thin line between such system-specific EPLD solutions and more general-purpose PAL circuits, Cypress Semiconductor Corp. is entering the market with a family of application-specific devices optimized for synchronous, asynchronous, and combinatorial applications (see p. 67). This approach allows the complexity and flexibility of advanced PLDs such as AMD's 22V10, but without sacrificing the speed of simpler 20- and 24-pin PALs, says Dane Elliot, manager of applications engineering.

On another PLD front, an increasing number of companies are gambling that designers will want a higher degree of reprogrammability than is possible with present UV-erasable PLDs. These companies are moving into electrically erasable devices, a market that Dataquest projects will grow sixty-fold, from only \$2.5 million in sales this year to more than \$150 million by 1992. Previously alone in this electrically erasable PLD niche, Lattice Semiconductor Corp. of Beaverton, Ore., with its PAL-like Generic Array Logic devices, has been joined by Exel Microelectronics, Gould Semiconductor, and International CMOS Technology.

Another recent entry is Advanced Micro Devices Inc. of Santa Clara, Calif., with a 24-pin PAL-based device, the AmPAL29M16 (see fig. 3), a synchronous device with 188 product terms and 16 I/O macrocells. And through technology and marketing agreements with Lattice Semiconductor, both National Semiconductor and SGS Semiconductor expect to enter the market with similar devices, as does Monolithic Memories, which recently signed an agreement with EEPROM manufacturer Seeq Technology Inc. of San Jose, Calif. Looking to maintain its technology lead, Lattice just introduced the first PLA with electrically reprogrammable AND and OR arrays (see p. 71), which have speeds approaching those of bipolar TTL-compatible PLDs. □

INTEL'S PLD PACKS BOTH SPEED AND COMPLEXITY

When it comes to the glue logic surrounding 80286- and 80386-based systems, the name of the game is speed and complexity. Taking dead aim at that logic, Intel Corp. has developed a programmable logic device with both assets. Other PLDs may be fast, but they don't contain enough circuitry to envelop all or most of the logic of high-performance 16- and 32-bit systems. Those that do have enough circuitry just aren't fast enough.

Intel's 5AC312, an ultraviolet-erasable, 1- μ m 131-by-189-mil single-metal CMOS circuit, incorporates 12 macrocells, each with a programmable input/output structure. The architecture hurdles four basic problems now limiting PLDs in high-performance applications:

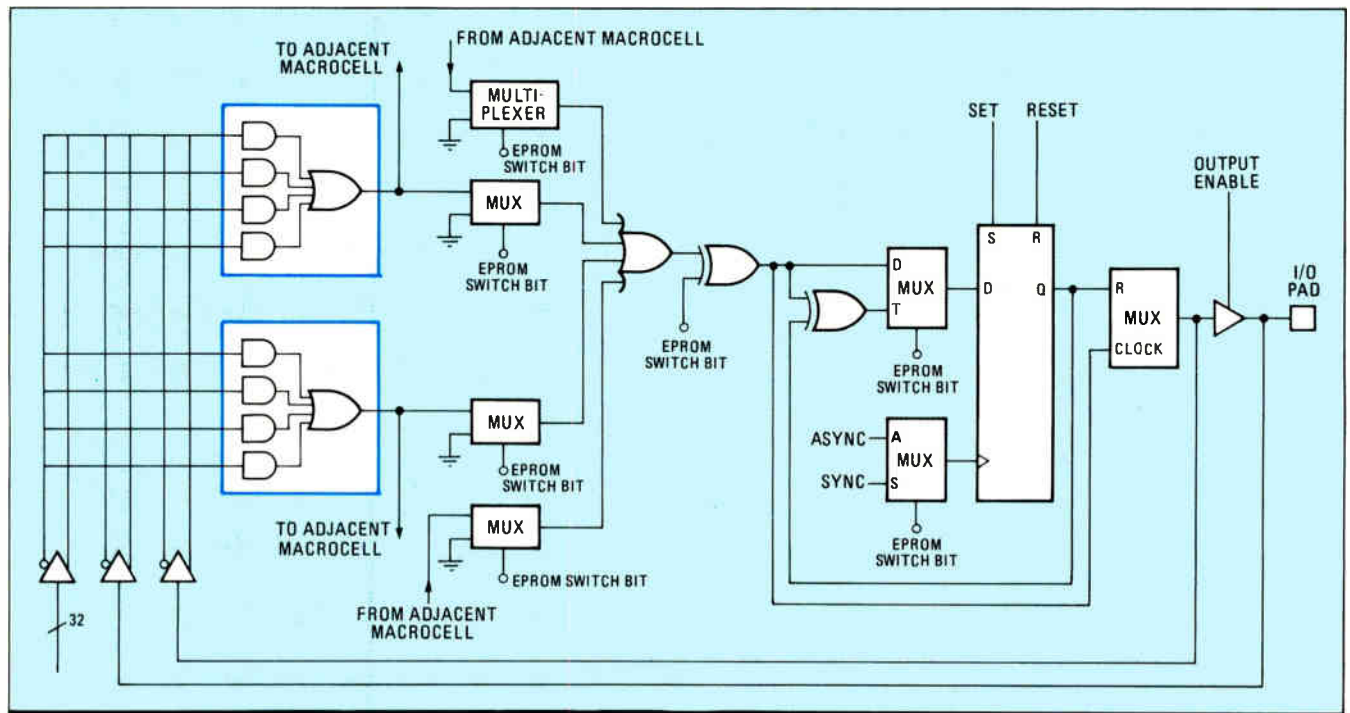
- Eight programmable inputs on the chip can implement either latched D-type registers or flow-through configurations, giving it the ability to latch and hold incoming data or signals.
- The latched registers on the inputs allow the 5AC312 to implement a state machine.
- Software-controlled product-term allocation between adjacent macrocells lets the Intel part satisfy more than eight product terms per macrocell while maintaining a user-definable pinout.
- Two product terms on all control signals meet the need for multiple product terms on secondary control signals.

Despite such complexity, speed has not been compromised, says Karlheinz Weigl, Intel's product line manager for erasable PLDs in Folsom, Calif. The 5AC312's propagation-delay time through the array is only 25 ns when operating at a clock rate of 35.7 MHz. This is equivalent to

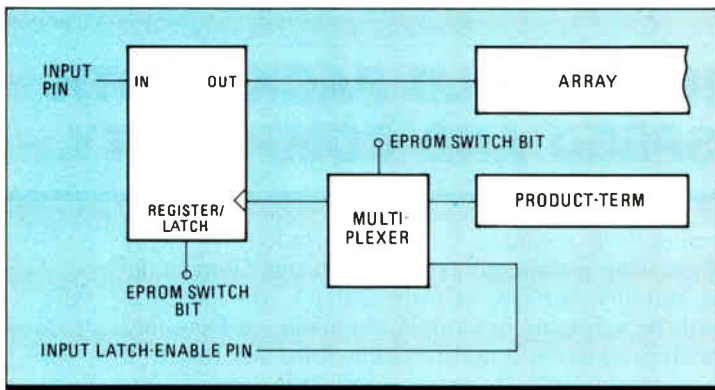
many less complex PAL-type circuits, he says. Featuring a nominal active current of 50 mA and a standby current of only 150 μ A, the 5AC312 will be available in sample quantities in October, with production quantities scheduled for the first quarter of 1988. Its price is \$22.50 in lots of 100.

According to Weigl, a major limitation of available traditional 20- and 24-pin PLDs—the only ones that match the speed requirements of 80286 or 80386 systems—is the inability to latch and hold incoming data. However, these microprocessors, with their pipelined bus-cycle structure, require data to be latched or stored for further decoding or other purposes at various points in the system. Latches for demultiplexing are also imperative for system operation with members of the older iAPX86 family, which uses a multiplexed address-data bus.

The standard approach to overcoming the lack of input latches or registers on PLDs is to use fast external TTL latches or TTL registers to perform the storage function, and a fast PLD in a second stage to perform the decoding function or other application-specific tasks. A significant problem with this approach, says Weigl, is that no matter how fast the TTL device is, it still adds a delay to a critical timing path, accounting for 30% to 50% of the actual propagation-delay time of the PLD. To compensate for this additional



1. FIVE WAYS. The 5AC312 can be programmed for flow-through, synchronous or asynchronous D-latch, or asynchronous or synchronous D-register.



2. ALLOCATION. In the 5AC312, EPROM-controlled multiplexers allow macrocells to share P-terms with each other.

delay, the designer has to call on a faster, costlier PLD to meet the requirements dictated by the microprocessor or by peripheral-chip timing.

Another problem with this approach, he says, is that the two devices have to be placed close together to avoid unwanted impedances introduced by printed-circuit-board traces. "This can be an unresolvable problem on very dense boards, possibly affecting operating frequencies," Weigl says.

To reduce the workload of the CPU in many microprocessor designs while maintaining a high level of performance, it is often necessary for dedicated tasks—such as interrupt servicing, bus arbitration, and time-out routines—to run on small state machines outside the CPU, notes Weigl. But, he says, none of the PLDs available today will accommodate a true register-logic-output state-machine architecture without a designer using the PLD's internal feedback capabilities or adding an external TTL latch or register at the input. And both of these solutions increase prop-

A user can create his own complex functions for the Intel PLD by shifting the logic resources—the P-terms—among the macrocells; it's all done with software

agation delay. "Either way, the designer will need very fast TTL components and very fast PLDs just to compensate for these architectural insufficiencies," Weigl says.

To solve both the inability to latch and hold incoming signals and the inability to implement a state machine, the 5AC312's input structure (see fig. 1) accommodates latch or register functions in most signal paths. Any of the PLD's input pins can be programmed to one of five different operations: flow-through; synchronous D-latch; synchronous D-register; asynchronous D-latch; or asynchronous D-register. Synchronous operation indicates that the latch/register combination is controlled by an external signal through a dedicated pin; in asyn-

chronous operation, the clock or latch enable is derived from a product term that can represent any possible combination of input signals.

The flow-through mode indicates that the latch/register combination is bypassed internally, and that any signal transitions on pins working in this mode are fed into the chip without timing considerations. With eight of these inputs, the part eliminates the need for external TTL functions, reducing chip count in a system and avoiding additional delays in critical timing paths.

Another major limitation of PAL-type programmable logic devices is that with few, if any, exceptions, currently available devices offer only eight product terms in one macrocell. "Although this many P-terms will cover many applications, it restricts the design engineer in complexity," says Weigl. The problem is that he cannot borrow unused P-terms from other macrocells in the PLD.

This dilemma is resolved in the 5AC312 with a proprietary architecture tailored to support P-term allocation, allowing the logic resources of the chip to be shifted around internally. At first glance, the 5AC312's internal structure (see fig. 2) looks like any other PLD macrocell, with eight user-programmable P-terms feeding into a logic OR function, followed by a programmable inversion option and the I/O control circuitry. But in the Intel chip, the eight P-terms of any macrocell are subdivided into two groups of four each. Instead of the P-terms going directly into the OR function, a layer of multiplexing functions sits between these nibbles, or groups of four, and the OR gate.

Controlled by external EPROM bits, the multiplexer implements the allocation of P-terms by passing through either the sum-of-products generated by the four P-terms in a macrocell or a combination of this sum-of-products and that generated by a nibble in an adjacent macrocell. In the latter case, the nibble borrowed from the adjacent macrocell can no longer contribute to the logic of the macrocell; its functionality has been allocated to support the demand for more P-terms in another macrocell.

This means that any macrocell inside the 5AC312 can handle logic functions demanding either 4, 8, 12, or 16 P-terms. This P-term allocation scheme allows for flexible fitting between logic resources and logic demand, rather than locating functions with high P-term demand at a predefined spot inside the chip. Consequently, a user can create his own application-specific pinout.

To enhance functionality and flexibility even further, the 5AC312 features two separate P-terms per secondary control signal—handy where several intelligent devices share common resources (buses, memory, and I/O lines) dealing with complex bus-transfer protocols or arbitration algorithms. Weigl says that because present PLDs provide only one P-term, designers have to call on primary logic resources, such as macrocells, which could serve better elsewhere. □

For more information, circle 480 on the reader service card.

EPLD LINE FROM CYPRESS IS APPLICATION-SPECIFIC

In its first four years in business, Cypress Semiconductor Corp. has successfully mined the niches in the markets for static random-access memories, nonvolatile memories, and logic. Now the San Jose, Calif., company is out to strike gold again—this time in programmable logic. Cypress has developed a family of what it calls application-specific erasable programmable logic devices, chips that attempt to combine two sets of sometimes contradictory features: speed on the one hand, and complexity on the other. Speed is a virtue often found in early 20- and 24-pin programmable array logic. Complexity and flexibility usually characterize later 28-, 40-, and 68-pin arrays—for example, the Advanced Micro Devices AmPAL22V10 or Altera's latest EPLDs (see p. 61).

The application-specific nature of Cypress's new chips enables them to bring a high level of complexity to their tasks and to achieve high speed as well, because they are not burdened with overhead from capabilities that are superfluous to their jobs. Fabricated using the company's 0.8- μ m double-level-metal, double-polysilicon CMOS EPROM process, the first parts in this family of 28-pin ultraviolet-erasable devices are the CY7C330 (see fig. 1), which is optimized for synchronous state-machine applications; the CY7C331, an asynchronous registered EPLD; and the CY7C332, built for registered combinatorial applications. All three parts are scheduled for volume production by the beginning of 1988.

Although first-generation PAL-type devices are extremely fast and efficient in terms of gate usage when the programmed functions fit into one device, they become inefficient when the functions must reside in small portions of several devices, says Dane Elliot, manager of applications engineering. Ensuing PLDs, he says, have sought to overcome this difficulty by providing in a single device all the functional capability of the most popular first-generation parts put together.

Although this approach does achieve high functional density, because one device can be tailored to the architecture required for a specific application, it has brought with it two main disadvantages, says Elliot. One is diminished gate efficiency—that is, in any given application some part of the chip will not be put into service. The second is eroded performance, not only because of the increased complexity, but because the unused functions still load the device, thereby slowing it down.

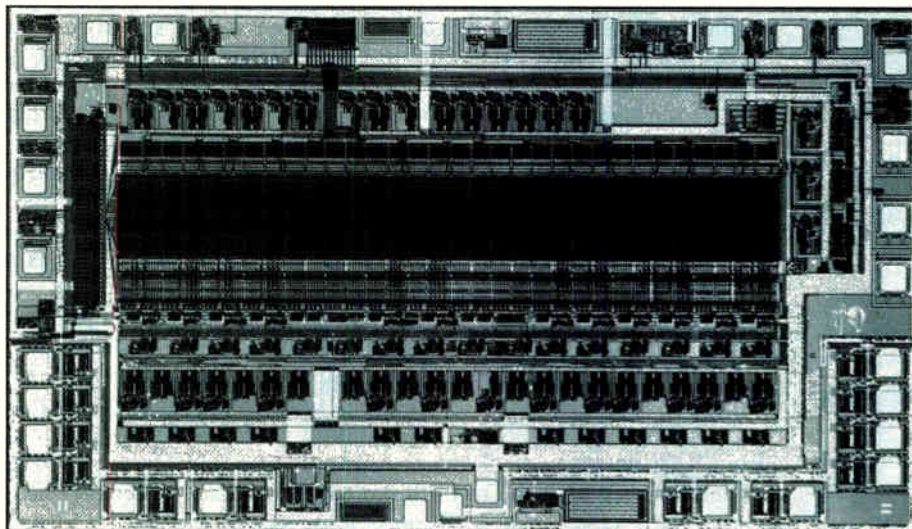
The solution is to develop programmable logic devices that are

application-specific yet flexible enough to solve a large and varied number of problems without the inefficiency of unused gates and without a performance penalty, Elliot says. "The main idea is that devices intended for synchronous applications need not be burdened with features that are not intended for synchronous use. In the same way, asynchronous and combinatorial devices should not be burdened with features that do not enhance their use in these types of applications."

Illustrative of Cypress's application-specific approach is the CY7C330, a 50-MHz, 256-product-term synchronous state machine built using about 17,000 EPROM cells. The 330 weighs in with 20-ns delays from the setup-and-clock input to the output and from the input register to the output register—equivalent to many less complex bipolar PLDs, Elliot says.

"Every feature on this device is optimized for synchronous operation," he continues. For one thing, the CY7C330 has an input/output macrocell structure of unusual design, incorporating two input-clock multiplexers, two feedback multiplexers, and two output-enable multiplexers (see fig. 2). The circuit contains six such macrocells, each of which is shared by two registered tri-state I/O pins.

"One way to look at these structures is as two macrocells, each of which contains its own state register and feedback term, and shares a third feedback term. What this allows the designer to do is hide one or the other of the state registers," Elliot says. "A big problem with present implementations is that if you use an I/O pin as



1. SPECIALIZED EPLD. The Cypress CY7C330 tackles synchronous state-machine applications.

an input, you lose the use of the state registers, because the only available feedback path is the input line of the state register. The advantage of the Cypress configuration is that you can feed back without giving up the state registers.”

For example, unlike the usual single-clock input on most PLDs, the CY7C330 contains three separate clocks; so it can synchronize independent synchronous state machines. And unlike most PLDs, which incorporate a single clock for

signal feeds back to an output register,” he says. The 330 avoids this problem because of its input registers.

And in a manner similar to Intel’s new EPLD (see p. 65), Cypress engineers have optimized the 330 for true state-machine operations by incorporating registers on the inputs—23 versus 11 for the Intel device, and none for any other PLD. With both input and output registers, a complete state machine can be implemented in a

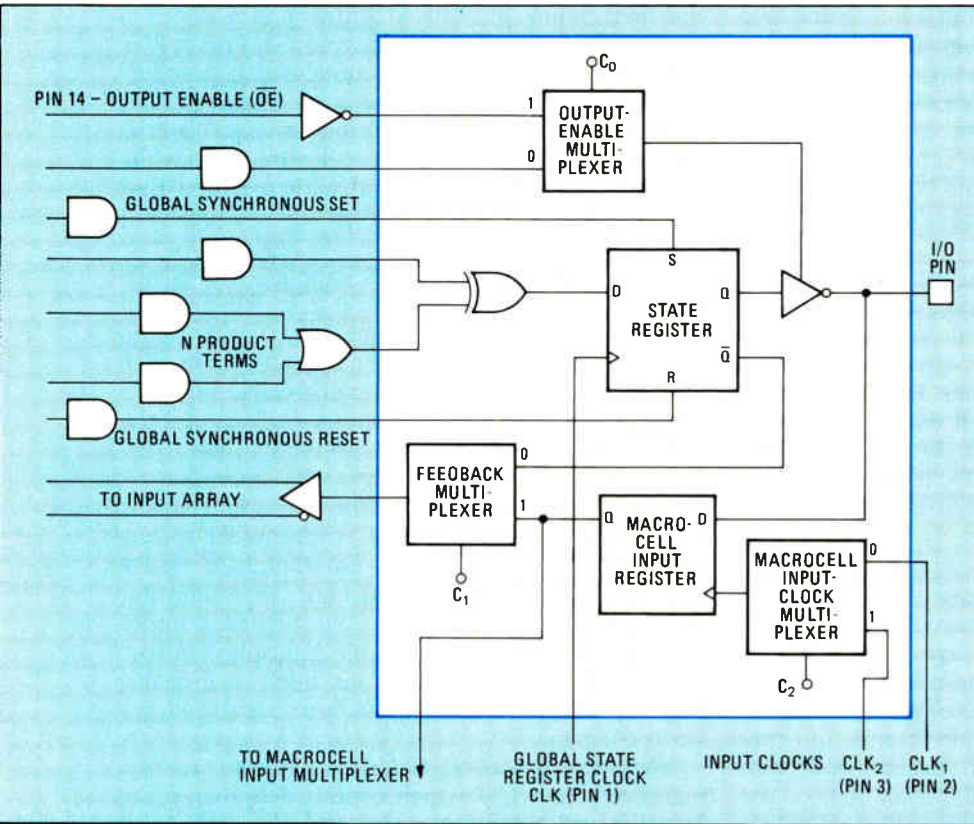
single device—without an external latch or register, and without feeding back through the device to make use of the output register, says Elliot. “Consequently, device performance is the sum of the time it takes to set it up and the clock-to-output delay,” he says. “Totally eliminated is the typical delay across the internal AND-OR array of most PLDs.”

The other members of the new Cypress family will also be application-specific. The CY7C331, for example, is a 192-product-term EPLD with 24 multi-function registers that’s optimized for asynchronous operation through the incorporation of a bi-directional I/O capability, separate synchronous D-type flip-flop set and reset features, and separate clock generation in the EPROM array. Of the device’s 13 dedicated input

pins, 12 drive the array; one asynchronously loads the data applied to the I/O pins into the six macrocell flip-flops for testing and for initialization. Also, the registers may be clocked from any logical clock that can be created from the array, preloaded, or bypassed. The 331 contains 8,000 EPROM cells and uses a 25-MHz clock; it has a 25-ns propagation delay, a 15-ns setup time, and a 25-ns clock-to-output delay.

Also incorporating 192 product terms, the CY7C332 is aimed at registered combinatorial applications. Containing about 8,000 EPROM cells and operating at a clock rate of 33 MHz, the 332 also contains 13 dedicated input pins; however, 12 of the pins can be programmed to be either registered or combinatorial. The 13th pin is reserved for synchronous, rather than asynchronous, loading of data applied to the I/O pins. Clock-to-output delay and propagation delay are both 15 ns. □

For more information, circle 481 on the reader service card.



2. MIGHTY MACRO. Each of the six I/O macrocells in the CY7C330 incorporates two input-clock multiplexers, two feedback multiplexers, and two output-enable multiplexers.

use by the state registers, the CY7C330 contains two input clocks, enabling a state machine to sample input signals generated by another system but which may be available on a bus only for a short period. “What this allows the designer is a high degree of flexibility,” Elliot says. “Using the state-register clock and one of the input clocks allows two state machines to be implemented. And using both input clocks allows four state-machine modes to be operated simultaneously, a feat that is impossible on other PLDs without adding external components.”

Also unusual among PLDs is the 330’s pipelined architecture, which in effect doubles the performance of a given function compared with its implementation on present nonpipelined architectures, says Elliot. “Usually pipelining is avoided on PLDs with fixed-AND, programmable-OR architectures, because the data on an I/O pin would require two clock cycles to get to a register whenever an external device is attached or a

Building on its static-RAM-based Logic Cell Array technology introduced last year, Xilinx Inc. has extended its proprietary family of programmable logic devices by using an architecture that will soon lead to fast arrays with as many as 9,000 equivalent NAND gates. This density level will, for the first time, allow programmable logic to compete for designs in 80% of the applications now targeted for gate arrays, says Wes Patterson, executive vice president of the San Jose, Calif., company.

The first device in Xilinx's new family of enhanced Logic Cell Arrays is the XC3020, which will allow densities of up to 2,400 equivalent gates. Available now in sample quantities, the third-generation 3020 [*Electronics*, Sept. 3, 1987, p. 25] will be followed later this year with a 9,000-gate device. The 3020 will be in full production in the first quarter of 1988.

ENHANCED ARCHITECTURE

The keys to the higher potential gate density of this new series of programmable logic devices are a 1.2- μm double-layer-metal CMOS process and an array of architectural enhancements that give the Logic Cell Arrays a flexibility and density heretofore associated only with traditional gate arrays, says Dave Galli, director of marketing communications at Xilinx. These enhancements include a more flexible logic-block architecture that permits easier routing and higher gate utilization. Also, wider logic-block functions facilitate both routing and higher gate utilization and allow faster performance for counters and decoders. Galli says that gate utilization is further enhanced by increased and improved interconnection resources.

During 1988, the company will fill out the family, bridging the gap between the low and high ends with Logic Cell Arrays of 2,700-, 4,000-, and 6,000-gate densities, Patterson says. By comparison, programmable logic devices based on the traditional AND-OR structures are available now with up to only 2,000 gates.

The XC3020, like the earlier members of the Logic Cell Array family, has an architecture with an interior array of uncommitted logic elements called CLBs, a surrounding ring of uncommitted I/O elements called IOBs, and programmable interconnections. As with gate arrays, says Galli, users can connect the CLBs in any fashion to build higher-level logic functions. The CLBs, in turn, can be connected to any of the IOBs, which can be

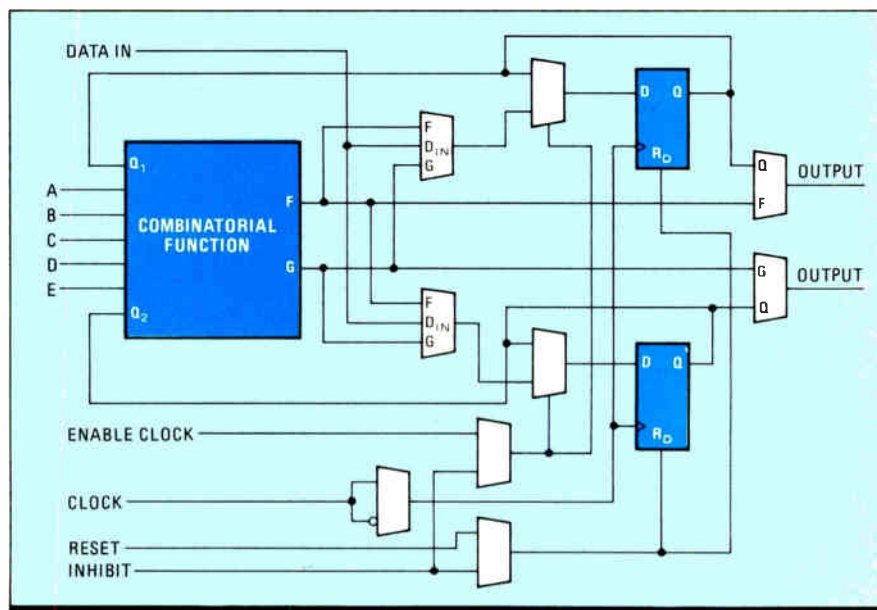
XILINX DESIGN TO LEAD TO 9,000-GATE PLDs

defined on a pin-for-pin basis as input, output, or three-state.

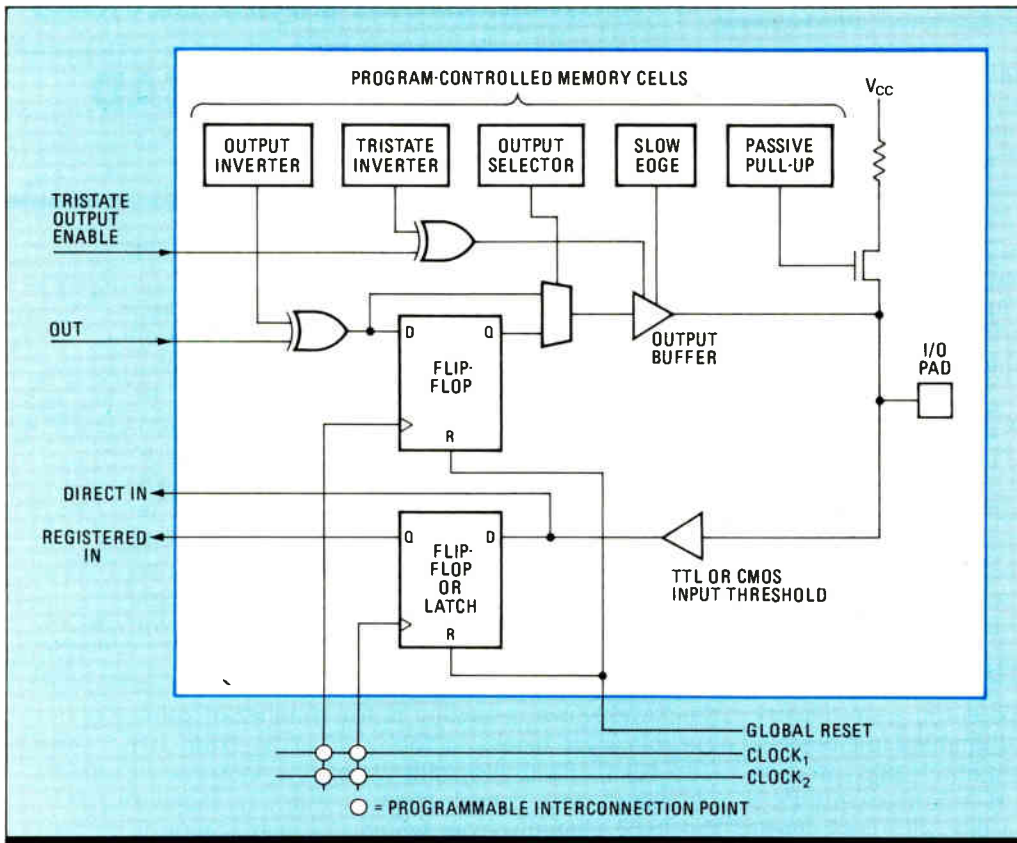
The definition of the XC3020's functions—routing of internal signals and the configuration of the logic and I/O blocks—is controlled by a configuration program stored in an internal 16-bit static RAM, eliminating the need for fuses, reprogrammable EPROM, or EEPROM elements to customize the part. An advantage of the SRAM-based design is that Logic Cell Arrays can be programmed much like microprocessors and their peripherals, via software loaded from an external ROM or PROM—one for each three Logic Cell Arrays—or under microprocessor control, says Patterson.

One important architectural enhancement in the XC3020 is a reduction in the number of configurable logic blocks in the basic array from 100 (10 \times 10) to 64 (8 \times 8), and a parallel increase in the complexity of each block (see fig. 1). Besides the logic element from which the user's logic is constructed, each CLB contains a block of combinatorial logic: dedicated logic for implementing clock, reset, and output selection functions, plus two edge-triggered flip-flops, compared with one for earlier devices.

Also increased in each CLB are the number of general-purpose combinatorial logic inputs, from four to five (A through E in fig. 1). Shared between the two flip-flops are two clock logic inputs, a reset input, and a direct flip-flop data input. The flip-flop outputs are also available as



1. LOGIC. The XC3020's configurable logic block has two storage elements and combinatorial logic.



2. CONNECTION. The I/O block connects its logic array and routing network with external pins.

direct inputs to the combinatorial logic block, further increasing the flexibility of this new architecture over earlier implementations. Also, the outputs of the CLB, X and Y, can be selected from either a combinatorial logic output (F or G) or a flip-flop output (Q1 or Q2).

The combinatorial logic block within a CLB uses a table look-up memory to implement Boolean functions. As a result, the 10-ns propagation delay through the combinatorial network is independent of the function generated. It can be configured as any two functions of up to four variables, a single function of five variables, or some functions of six or seven variables when Q1 and Q2 are used as inputs to the combinatorial logic block. When the combinatorial block implements two functions of four variables, two independent outputs—F and G—are available. F and G are equal when five-, six-, or seven-variable functions are implemented.

According to Galli, these different base configurations permit the designer to implement denser designs. For example, when a four-input function is required, the designer can split the CLB, rather than use all of the five-input block.

The two storage elements in the CLB share common reset, clock, and clock-enable lines. The edge-triggered flip-flops can be toggled at rates up to 70 MHz. Only one phase of the clock signal needs to be distributed.

As with earlier Xilinx implementations, one advantage of the architecture used in the XC3020

is that the I/O logic blocks (see fig. 2), which provide the interface between external package pins and the internal CLB logic blocks, are independent of the internal logic structure. Their routing, both into and out of the logic blocks, is determined by the designer. Thus the user can utilize the I/O flip-flops for logic functions such as counters or shift registers.

The particular improvement in this block of the new architecture is the addition of a second flip-flop to each of the I/O blocks. For one thing, in the improved version, two paths—one direct and one registered—are available for both the input signal and the output signal. The registered inputs can be latched by

the edge- or level-sensitive flip-flop, and the outputs can be simultaneously clocked out of the chip by the output flip-flop.

In addition, through programming, the output signal can be inverted, three-stated, or have its transient response controlled. It can be connected to a pull-up resistor if the pin is unused, to prevent unnecessary power dissipation. The input buffer level is selectable as either CMOS or TTL for the entire device.

Another key to the more flexible architecture is an improved interconnection scheme, in which metal segments with programmable switching points implement the variable routing. In this advanced version of the Logic Cell Array architecture, says Galli, there are three types of interconnection: general-purpose interconnection, direct interconnection, and long lines.

General-purpose interconnection is a grid of five metal segments that run horizontally and vertically between the rows and columns of logic and I/O blocks. It is usually used to conduct less-critical signals within a localized area. Where these segments overlay at an intersection of a row and column, a switching matrix composed of n-channel pass transistors is provided to make the interconnection.

Direct interconnection is used to build localized, high-speed structures, such as counters and shift registers. It feeds CLB output signal Y to the inputs of the two CLBs that are directly above and below. Similarly, the X output is fed

to inputs of two CLBs that are to the left and right. The propagation time of this interconnection is near zero, because it bypasses the normal output-buffer and input-selection circuits.

But the key enhancement to the XC3020's interconnection scheme lies in how the long lines running vertically and horizontally across the device are implemented, says Galli. They bypass the switch matrices and are intended for signals that must travel a long distance or that must

have little or no skew between multiple destinations. For each row of CLBs there are four vertical lines—two general-purpose and two intended for clock signals—and two horizontal lines. Unlike the earlier Logic Cell Array architectures, the two horizontal long lines are connected to additional three-state logic that can implement an on-chip bidirectional bus, similar to that of traditional gate arrays. □

For more information, circle 482 on the reader service card.

TECHNOLOGY TO WATCH

PROGRAMMABLE LOGIC DEVICES

LATTICE ADDS FLEXIBILITY TO EEPROM-BASED PLD

Lattice Semiconductor Corp. is aiming to scale new heights of flexibility and functionality in programmable logic devices. The Beaverton, Ore., company's CMOS GAL39V18 programmable logic array for the first time puts electrically erasable AND and OR arrays on the same chip. This dual-programmable-logic-array approach provides more flexibility than the traditional single-programmable-array logic, in which only the AND array is programmable and the OR array is hard-wired. And the 39V18 provides more functionality than the typical dual-programmable PLA because it incorporates such PAL-style features as macrocells and buried registers.

The 39V18 (see fig. 1) could steal a march on all other PLDs. Besides gaining additional functionality, users of the traditional fuse-programmable bipolar PLAs who switch to the 39V18 get the benefits of erasability and PAL-style speed. Users of the traditional fuse-programmable PAL who switch gain the flexibility of dual programmability without giving up the added functionality with which PAL makers have enhanced their parts. And users of the newer PAL-style CMOS ultraviolet-erasable PLDs and of Lattice's first EEPROM family now have a dual-programmable alternative.

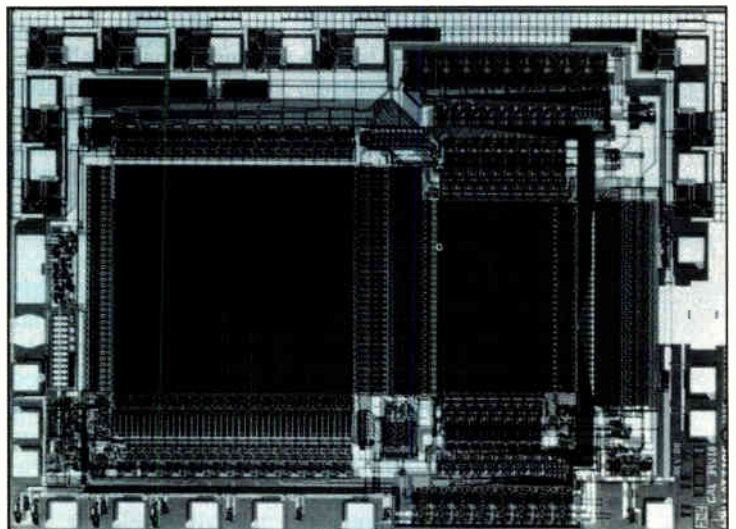
Until now, the problem with dual-programmable arrays, both the fuse-programmable PLAs and the UV-erasable EPLDs, has been a lack of speed, says Dean Suhr, product marketing manager at Lattice. In the 39V18, Lattice attained more speed by using an aggressive CMOS process that also gave the density that accommodated increased functionality such as macrocells. The design flexibility of the company's dual-programmable-array architecture is further enhanced by the use of a complex D-E type register macrocell. What's more, the 39V18 gains added flexibility by using buried states, or registers, for the first time on a PLA-type device.

The UltramOS-III process, a slightly relaxed version of the company's CMOS EEPROM technology, was chosen for the new array. The process is characterized by 0.7- μm effective gate lengths, double polysilicon, and double-level metalization. It uses Lattice's electrically erasable core cell, which is approximately 16 by 15 μm . TTL-compatible input structures are featured, along with high-drive bipolar-compatible output buffers that

offer a full 16 mA of output drive. There are 5,700 cells in the AND array driving 2,300 cells in the OR array.

Asynchronous propagation delay is typically 20 ns total through both arrays. The 39V18 is also capable of high-performance synchronous operation. A clock-to-output delay of 12 ns (15 ns maximum) allows the device to run at more than 40 MHz in pipelined applications and at 25 MHz as a state machine. That's as fast as any bipolar PLD currently available. Collector current is low, typically 80 mA. And at 400 mW, the 39V18 consumes half the power of less-functional bipolar PLDs. Samples of the part are available now, and full production is slated to begin by year's end.

The 39V18's programmable AND and OR arrays are served by four types of macrocells (see fig. 2) Driving the AND array are 38 inputs, each of which has a macrocell associated with it; 10 are input logic cells, 10 are I/O logic cells, 10 are output logic cells, and 8 are buried state-logic cells. The OR array is driven by 64 product terms,



1. **DUAL ARRAY.** Both AND and OR arrays on Lattice's GAL39V18 electrically erasable PLD are programmable.

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Designing complex state machines and high performance controllers can really drive you crazy.

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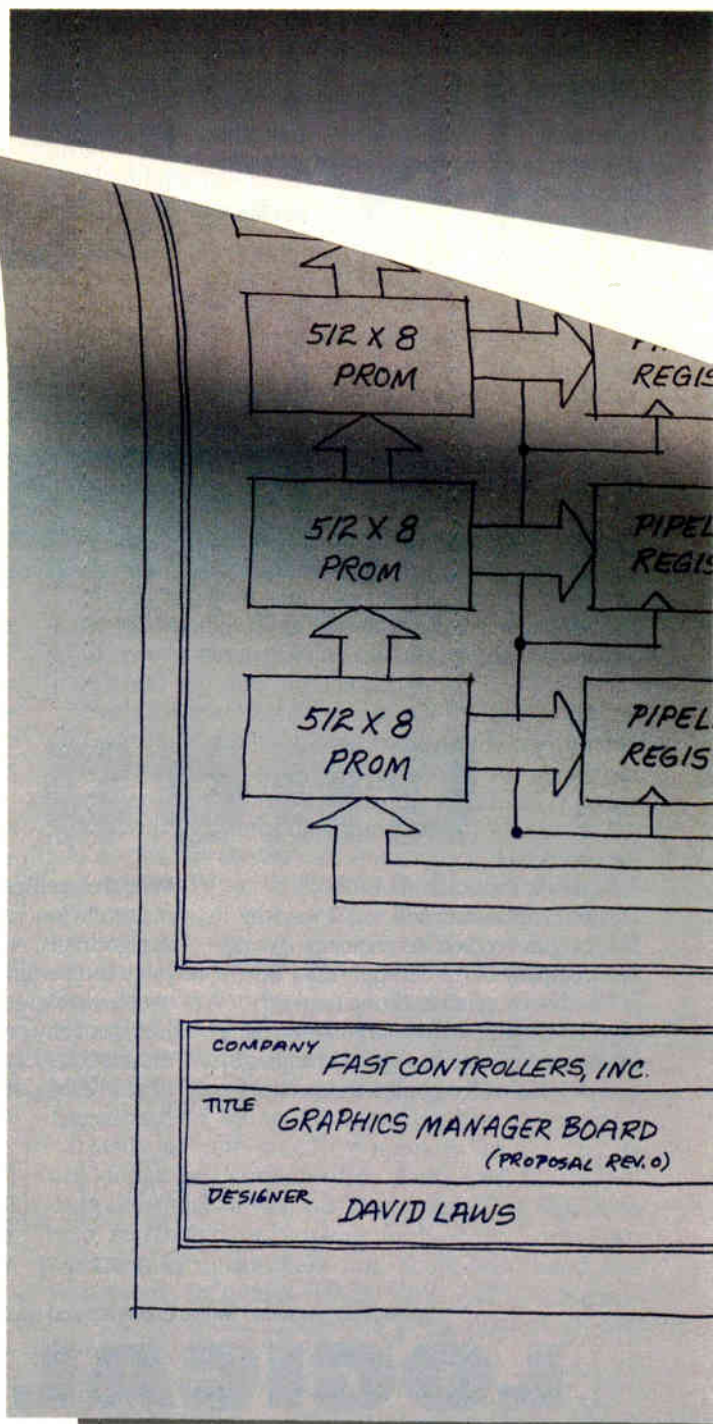
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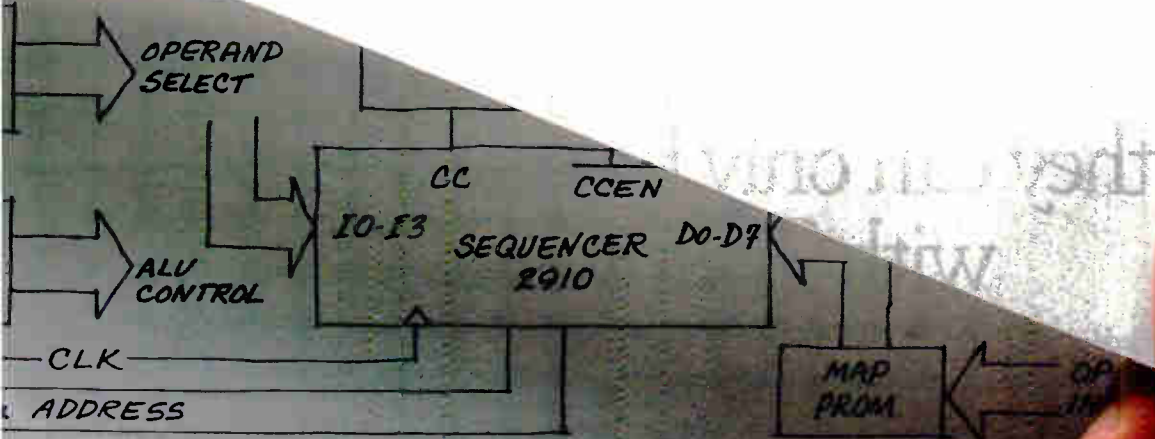
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- PROMS - 27S29 (5)
- PIPE - 74F-374 (4)
- MUX - 74F-153 (2)
- SEQUENCER - 2910 (1)

CONTRACT NO.

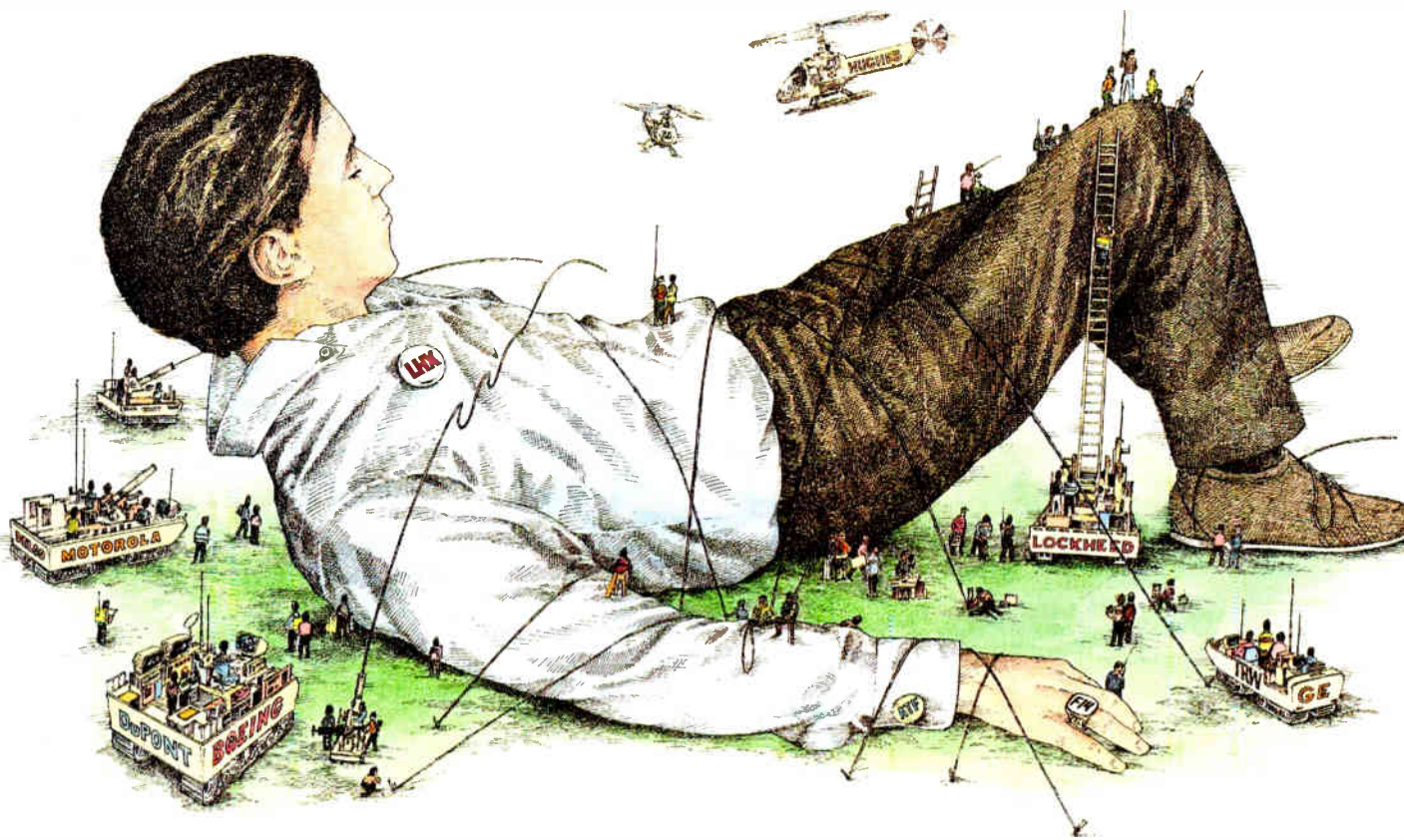
87

APPROVALS

Don Nelson

Bob Golen

Baron...



Some development projects are so big they can only be managed with Teamwork.

Creating embedded software systems can be a gigantic challenge. But now there's a way to manage the process, lower costs, improve productivity, and keep your team competitive.

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Teamwork is a registered trademark of Cadre Technologies Inc.

Teamwork is being used by many leading companies like Grumman, Rockwell, DuPont, Litton, HP, Delco, Motorola, General Dynamics, and Westinghouse for their most sophisticated projects. And it's helping many of these users meet stringent DoD-2167 requirements.

No wonder Teamwork is the number one workstation-based CASE tool on the market. It was the first to support real-time modeling. First to support all workstation environments. First with data base sharing for workstation users. And it has the most advanced user interface of any CASE tool on the market, making it extremely easy to learn and use.

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If computers are so smart, why don't they write their own software? The simple answer, of course, is that they aren't that smart yet. But computers finally are beginning to help with this

excruciating job. Just as computer hardware became so complex that computers had to be enlisted to help design it, so the growing complexity of software is spurring the emergence of computer-aided software engineering.

Despite a good deal of overselling, CASE products are gaining attention because they're beginning to offer some real benefits. CASE is starting to deliver on some of its promises—making finished software match the requirements originally specified for it, delivering more reliable software, making it easier to maintain software over its entire useful life, and producing more software in much less time and at lower costs.

But CASE still has a long way to go. Although nearly 100 products from over 30 companies are available (see tables, pp. 77-78), overall the offerings are considered barely sufficient. These products do a fair job in specific areas, but there are plenty of holes to be plugged. Even more important, these products and those that eventually fill the gaps must be able to work together. "The number-one need is an integrated tool set," says Rick Potter, general manager of the CASE division of Tektronix Inc. Software developers want products that share common data bases and standard interfaces, in a system that takes care of all the phases in the software life cycle—from requirements to detailed specifications, from design, coding, and testing, and through the maintenance that goes on until the day the software is scrapped.

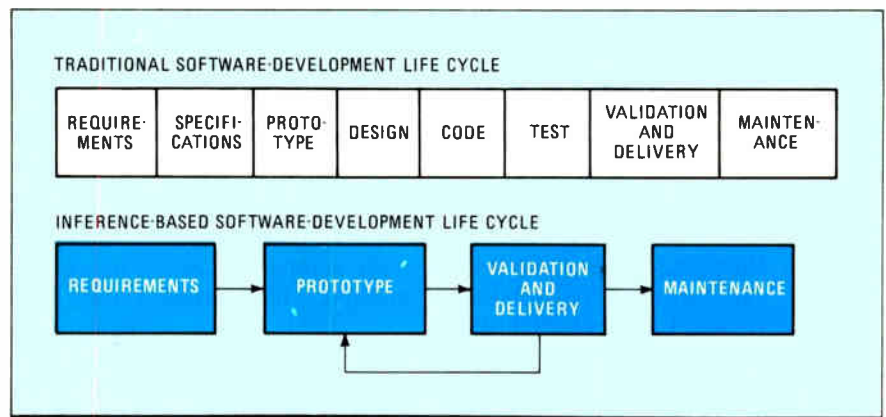
CASE developers are finally listening to their customers and are starting to work hard on the integration problem. At least one company, Cadre Technologies Inc., proposes the adoption of a standard that not only would help CASE packages work together but would also serve to link them with CAE systems—paving the way for integrated hardware and software design systems. Another standard is being pushed by a group of countries in Western Europe.

Integration on that level will not come easily. There are too many CASE packages that have little in common—they automate only specif-

SPECIAL REPORT: INTEGRATION IS CRUCIAL TO CASE'S FUTURE

Computer-aided software engineering is finally beginning to deliver on some of its promises, but the No. 1 demand now from CASE users is an integrated tool set

by Tom Manuel



1. SQUEEZE PLAY. Aion's application-development system allows rapid prototyping by using AI technology to compress the software-development life cycle down to four phases.

ic phases in a software-development project. Some prepare the way for writing code, defining requirements, preparing specifications, and verifying designs. Others smooth the path for implementation, after coding, by helping to test, reverify, deploy, and maintain the software. A growing number automate documentation, an important aspect of software projects that often gets little attention, and in several cases documentation is being expanded to become a tool that manages software-development projects.

The wide variety of CASE tools leads some vendors to believe that integration at a stroke is unlikely to happen. They feel it makes more sense to gradually tie together the tools for each phase, working step by step. Others put their faith in what they think could be much faster approaches based on artificial intelligence. AI already can drastically compress software development, squeezing the many stages of the software life cycle down to just four—requirements, prototyping, validation, and maintenance (see fig. 1).

Regardless of the way they want to get there, though, all CASE companies see integration as crucial. This view led Cadre Technologies to favor a broad-based approach. The Providence, R. I., company wants to establish a standard for data-interchange formats that all CASE tools would use, and at the Design Automation Conference in Miami Beach in June, it proposed that all CASE companies adopt the Electronic Design Interchange Format. EDIF is the same standard that the CASE companies' hardware counterparts, the computer-aided-engineering companies, are almost sure to embrace [*Electronics*, July 9, 1987, p. 31].

If Cadre wins widespread support for EDIF, the implications for system design will extend beyond software engineering alone. Use of the standard would be a logical first step toward integrating CASE and CAE systems, meaning the design of complete systems, hardware and software, could be automated.

Cadre has already demonstrated the feasibility of using EDIF as a CASE integration tool. Working with an extended version of the standard, Cadre integrated its own Teamwork CASE environment, a set of CASE tools for work stations, with the personal-computer version of Exceleator, a CASE product from Index Technology Corp., another of the leading CASE companies. So far, however, no other CASE company has come forward to support EDIF.

Another move to promote a CASE standard—a different one—is under way in Western Europe. A number of companies in France, the United Kingdom, West Germany, Belgium, and Italy have started joint development of an internation-

CASE PRODUCTS ARE AVAILABLE . . .

Company	Leading Product or Family
Aion Corp. Palo Alto, Calif.	Application Development System
American Management Systems Inc. New York, N. Y.	Life-cycle Productivity System
Atherton Technology Sunnyvale, Calif.	Software Backplane
Cadre Technologies Inc. Providence, Rhode Island	Teamwork/SA /RT /SD
Case Ware Inc. Costa Mesa, Calif.	Amplify Control
Context Corp. Beaverton, Ore.	Documentation Management Systems
Cortex Corp. Waltham, Mass.	CorVision
Hewlett-Packard Co. Palo Alto	HP Teamwork/SA /RT /SD
Iconix Software Engineering Inc. Santa Monica, Calif.	Prism
Index Technology Corp. Cambridge, Mass.	Exceleator
Information Research Associates Austin, Texas	PAWS/GPSM
Interactive Development Environments Inc. San Francisco, Calif.	Software Through Pictures
Nastec Corp. Southfield, Michigan	DesignAid
Netron Inc. Toronto, Ontario	Netron/CAP

al standard interface for CASE tools. This effort, which is being promoted by a NATO unit called the Independent European Program Group, aims at one interface standard for military and civilian use.

But most CASE companies are taking a somewhat less ambitious route. Some are concentrating on specialized markets. Ready Systems, for example, has developed a highly integrated, computer-aided development package, but it is aiming that package at the market for real-time software (see p. 81). "Real-time is not a little market—it's worth about \$40 billion a year in military real-time systems alone," says Aryeh Finegold, president and CEO of the Palo Alto, Calif., company. It is also a market with special needs in software tools. These needs have largely been ignored, Finegold says, making real-time ripe for development tools.

A more general approach is being taken by Atherton Technology. The Sunnyvale, Calif., startup has developed a smart idea into a prod-

FROM MANY COMPANIES	
Company	Leading Product or Family
Parameter Driven Software Inc. Birmingham, Michigan	PDS-Adept
Promod Inc. Lake Forest, Calif.	ProMod CASE Tools
Productivity Products International Inc. Sandy Hook, Conn.	Objective-C, Vici
Ready Systems Palo Alto	CARDTools
Reasoning Systems Inc. Palo Alto	Refine
SoftLab Inc. San Francisco	Maestro Environment
Software Products Services Inc. New York	EPOS
Solutions Systems Norwell, Mass.	Brief Programming Editor
Step Engineering Inc. Sunnyvale, Calif.	Meta Step Microprogramming Development Language
Team Engineering Inc. Santa Cruz, Calif.	Tiger User Interface Toolkit
Tektronix Inc. Beaverton, Ore.	Integral CASE Software Factory
Texas Instruments Inc. Plane, Texas	Information Engineering Facility
Unisys Corp. Bluebell, Penn.	Ally Software Development Environment
ViaSoft Corp. Phoenix, Ariz.	Via/Insight
Visual Software Inc. Santa Clara, Calif.	vsDesigner

uct that will integrate tools from any source into a CASE system. Its Software BackPlane puts the tools under common management control, makes a common user-interface environment available, and provides portability to different operating systems and hardware platforms (see p. 83).

However, Atherton's bright idea will only work if the Software BackPlane has many CASE tools in it. Atherton plans to put in tools of its own, but it acknowledges that no company can develop all the necessary tools for a complete CASE environment and do them well. So it is inviting other CASE companies to join in. So far, one other CASE company, Interactive Development Environments Inc. of San Francisco, has taken up the challenge.

Interactive is adapting its Software Through Pictures tools to the Software BackPlane. Designed to provide graphical tools for structured analysis and structured design of both standard and real-time systems, and for prototyping those systems, the Software Through Pictures tool kit

is a good start toward an integrated CASE system using the Software BackPlane. How quickly other tools are made available will determine whether the BackPlane can become the base standard for integrated CASE. If it does, it has the potential to revolutionize large-scale software-development projects.

But these are only separate and isolated attempts to integrate CASE. Whether any of them will become a rallying point for the industry remains to be seen. In the meantime, CASE companies are concentrating on solving specific problems that arise at the different stages of a software-development project.

Some companies are concentrating on finding and fixing errors in the earliest possible stages of development, since it costs a lot more to correct errors in software after coding and delivery (see chart, p. 80). Others have pinpointed different needs to address all through the cycle.

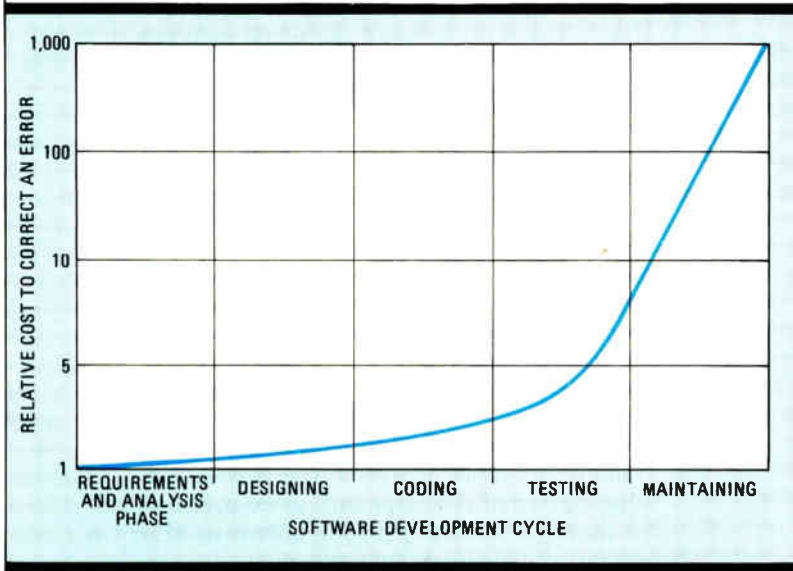
Tektronix's Potter singles out two areas he thinks are vital: "tools for verifying that software meets requirements prior to and again after coding, and the ability to trace from the requirements all the way down to the implementation and make sure that each step correctly relates to the previous step." The Beaverton, Ore., company's software developers will soon be working on the needs outlined by Potter. Over the next year, they will add to the CASE family of products a package for step-by-step verification. Another package will validate, at the end of the project, that the original requirements have been met.

This step-by-step approach may, in fact, turn out to be another approach to integration as well, says Brad Yackle. He is project manager for HP Teamwork, a CASE product

line from the technical-systems business unit of Hewlett-Packard Co. in Fort Collins, Colo. HP Teamwork is a version of the Cadre Teamwork family of products that runs under HP UX, HP's version of the Unix operating system, on the company's 9000 work stations. "Integration will come as a natural evolution," Yackle says. "First, we will get some CASE tools like HP Teamwork out there into users' hands. Then we need to make the various tools share as much information as possible. Finally, we need tracking and consistency checking between phases of the software-development cycle. All this adds up to what people are calling an integrated programming software environment."

Lending credence to Yackle's view, Texas Instruments Inc. is introducing an integrated CASE system—but it's doing it step by step. The company's Information Systems and Service Group in Plano, Texas, announced the product, the Information Engineering Facility, at the beginning of

FIXING ERRORS EARLY SAVES MONEY



July. Two components are already available. They are an Analysis Toolset, a set of graphics-oriented tools for specification and analysis that runs on personal computers, and a Mainframe Encyclopedia, a central repository running on IBM Corp. mainframes. A Design Toolset will be ready this month, says Eldin Patterson, director of development for IEF. "We also have code-generation and data-base-design modules working in the lab, which we will soon introduce," he says.

All components of IEF run off a central model and are tightly integrated. "If an engineer makes a change in one place, the change is automatically made in all other affected parts. We plan to generate 100% of the code," Patterson says.

Among other companies taking a step-by-step approach, several are addressing one particular phase: documentation. Long the stepchild of software development, documentation is finally

getting some attention from major CASE vendors. The next project for HP, for example, is to take output from HP Teamwork for input to a documentation package. And Tektronix has just announced the addition of a documentation package to its product line.

Another company, Context Corp. in Beaverton, Ore., sees documentation packages as more than just another tool to add to CASE systems. Context's Documentation Management system will take on a key role in integrated programming software environments, the company claims.

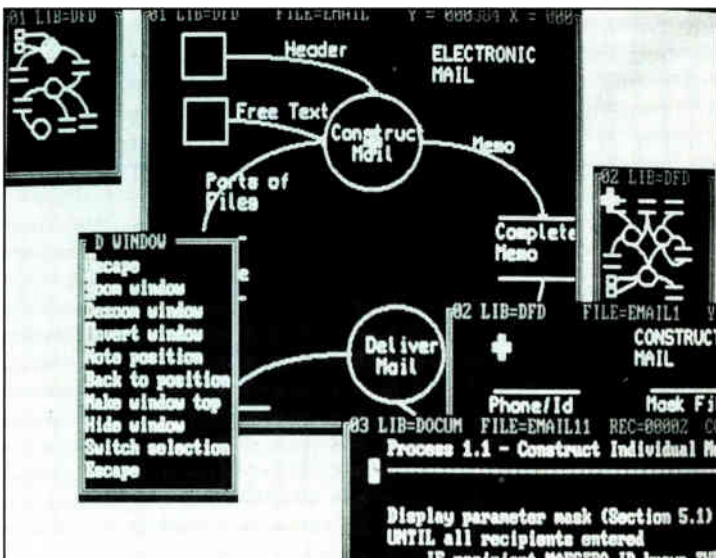
Besides producing documents, Context's system manages and controls all hardware and software changes to all system-design documentation. In playing such a central role, this change-control feature in the Context documentation system could become the central project-management tool in future integrated systems.

Documentation is also seen as the key to another software-development environment for project control and project management, the Maestro system offered by Softlab Inc. (see fig. 2). The San Francisco company and its parent, West Germany's Softlab AG, are among the oldest and largest CASE companies. The Maestro system, which grew out of the German firm's need for a development environment for its big software projects, had its beginnings in 1971. It is used now on over 17,000 work stations in 15 countries.

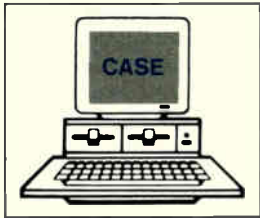
Maestro is primarily a software project-management and document-control system. It runs on networked work stations and a central department minicomputer. The mini handles the centralized management, information, and communications functions of the system. Maestro does project logging, enforces standards, maintains a project library, tracks documentation, and maintains special libraries for each programming language to help keep coding formats correct.

The drawback to doing things step by step, of course, is that it takes time. Some CASE companies think artificial intelligence promises to help automate software production more quickly. One of those companies is Aion Corp., a Palo Alto, Calif., company that's applying AI inference technology to CASE. The Aion Development System "is a fundamental step forward in how we view and do programming," says Harry C. Reinstein, company president. "The breakthrough in ADS is the processing of specifications using inference technology rather than processing procedures."

Using ADS, programming starts with a logical specification. Then a prototype program is developed and tested. Next, enhancements are made to the prototype until the program is ready for delivery. Changes to the program during development and after deployment during the maintenance phase are done by modifying the specifications. □



2. PC TARGETED. The Maestro analyst's workbench uses graphics and multiple windows on a personal computer to show hierarchical software structures.



The developers of real-time software now have a set of computer-aided software-engineering tools that are designed to meet their special needs. CARDtools from

Ready Systems can help overcome the challenges that are unique to the design of real-time applications.

For the designers working on such software, these challenges can be monumental. Not only must their applications generate correct responses, but they must do so within critically tight time deadlines, with extremely high reliability, on hardware with myriad different input/output devices. The deadlines are imposed by real-world events; not meeting them is a potentially catastrophic failure of the system.

Until now, CASE tools have been targeted primarily at data-processing applications and have not addressed the special requirements of real-time processing. Since the timing and behavior of hardware don't have much effect on the correct operation of such applications, most CASE tools do not support modeling and analysis of timing and detailed hardware interfaces. But CARDtools does.

Ready Systems, a Palo Alto, Calif., real-time software company, designed CARDtools (the name stands for computer-aided real-time design tools) as an integrated set of interactive tools, all operating on a common data base. They currently run on the complete range of VAX VMS systems from Digital Equipment Corp. (see fig. 1) and on IBM Corp. personal computers and compatibles.

There are four major parts to CARDtools:

- Tools with which to specify the software-hardware interface.
- TaskBuilder, a tool package to completely model and analyze real-time multitasking.
- RTPV, a package of real-time performance verification tools with which to check performance against time deadlines, before detailed design or code implementation.
- A package-definition tool set to model the design in terms of its components and also to provide support for writing code in Ada and other object-oriented languages.

The specification tools are crucial to CARDtools. Real-time software must be aware of the real-world equipment it is controlling, so it must know how the hardware behaves and what constraints it imposes. The hardware-to-software interface must be completely specified. To be complete enough for a real-time system to be able to take all possible cases into consideration, this interface specification must include five critical components.

First, the designer must describe all the hard-

AT LAST: A TOOLKIT FOR REAL-TIME SOFTWARE

ware devices that will be sending data to the software. Then he must spell out the characteristics of data-item values being sent, such as range, units, and accuracy. Next, he needs to set down the representation of data, given in number of bits and location of bits. Fourth, the designer must fully describe the instruction set for accessing data. And, finally, the critical time deadlines imposed by real-time events, within which data has to be read and processed, must be included in this specification of the interface of the system to the real world. Later on in the design, when performance has been modeled or measured, this is the record against which performance should be checked.

The CARDtools package which supports the capture of this hardware-to-software interface data with data typing and I/O questionnaires (see fig. 2). The data types used are the same as those in the Ada programming language. A CARDtools data-item specification includes full data-typing information. Should a data type be declared to be in the category of hardware numeric or logical, the user is prompted for a full description of the hardware-software interface.

The second set of tools is the TaskBuilder package. Virtually all real-time systems are mul-

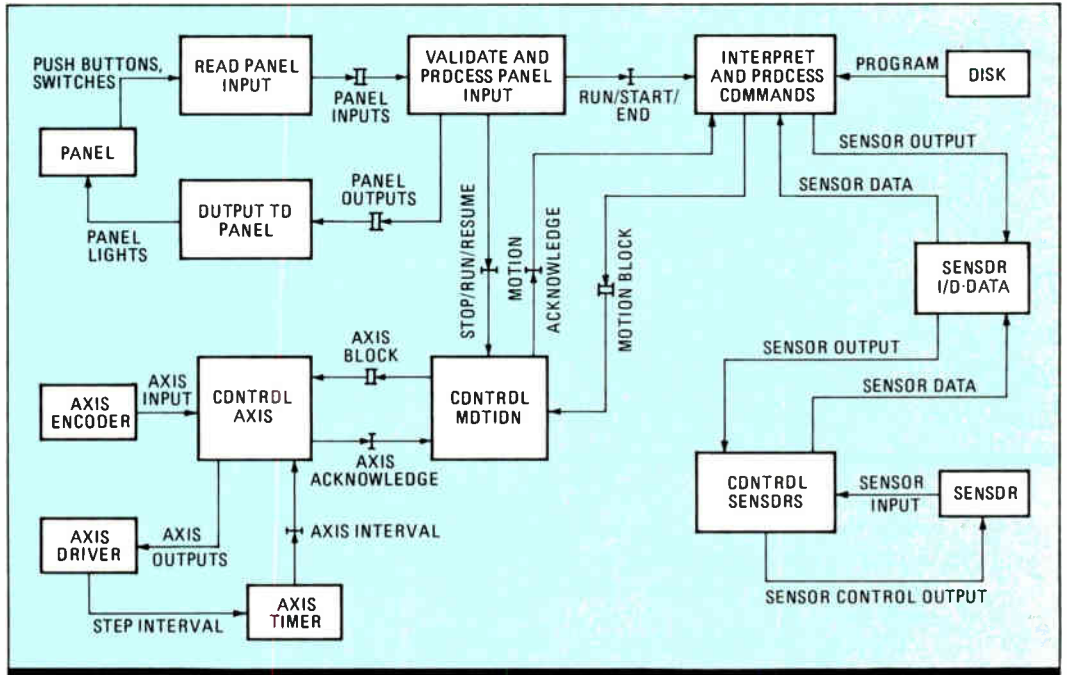


1. MODERN TOOLS. CARDtools runs on a variety of systems such as this VAXstation 2000, all other VAXes, and standard personal computers.

3. MODEL. CARDtools can draw and verify a complex task model, such as this one of a robot control system.

modules into the overall software-system design. This is a practical necessity for developing large, complex systems, which are almost always built by first designing modules of small, well-understood components, then fitting the components together. In many real-time systems, this procedure is being mandated by the use of Ada, a highly modular language. The CARDtools package-definition facility integrates the design of such components with the design of the overall system.

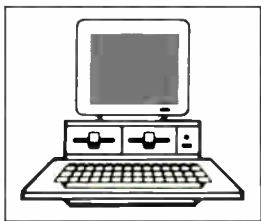
Packages are defined as libraries of functions that all operate on the same object. An object could be a data type or a hardware device. The package-definition facility supports specification of the object and functions, including complete



functional decomposition and Ada data types. Package functions may then be used to build up an overall functional decomposition of the system. Strong type-checking is then automatically performed between the overall system model and the package model. □

For more information, circle 484 on the reader service card.

TECHNOLOGY TO WATCH



Software development is a mess. Virtually all large, complex software projects run over budget, miss delivery schedules, and end up producing programs that are only marginally reliable. Typically, the finished software fails to meet specifications and is difficult and expensive to maintain.

Now an all-purpose software-engineering system from Atherton Technology promises to help clean up the software mess. The Software Backplane is based on computer-aided software-engineering tools, the kind offered by several companies to aid in the management of software projects. But where individual CASE tools are directed only at a handful of software-development problems, the Software BackPlane integrates CASE tools into a single system that can be installed on a variety of hardware platforms.

Atherton, a Sunnyvale, Calif., startup, is the first company to offer a commercial, off-the-shelf version of such a system, known as an integrated project-support environment, or IPSE. The system integrates tools from a variety of

ATHERTON FINDS A WAY TO INTEGRATE CASE TOOLS

different vendors into a system with a common user interface. Management facilities collect all the data gathered and used by the tools and store it in a master data base. This master data base may manage all project data or comprise the different data bases of the individual tools.

Building an IPSE is difficult and time-consuming, but a few companies have developed them for in-house use. Generally, such internal systems don't provide a very high level of tool integration, version control, equivalence relationships among related objects in the software life cycle, history tracking, or automated system modeling and building (see fig. 1). The Software BackPlane, by contrast, takes over command and control of the system with a scheme for coordinating and controlling the tools and the information generated by them.

First, the Software Backplane integrates off-the-shelf CASE tools from different vendors, although such tools usually are not designed to

work together. It also provides a common data structure through which all of the tools can exchange data. It isolates the tools from particular operating systems and from different hardware platforms, allowing tools from different vendors to run on most popular platforms and under most popular operating systems. The same integrated package will be able run on future plat-

The Software Backplane aims at linking tools from many vendors in a system with a common user interface and a master data base for all the data the tools collect

forms and operating systems. Finally, the Software Backplane provides a common, easy-to-use interface for all the tools, eliminating the annoyance of having to learn a different interface for each tool.

The Software BackPlane is able to link a diverse collection of CASE tools and networked hardware platforms together because of its layered architecture (see fig. 2). Over the entire architecture is the consistent user-interface environment that gives all CASE tools under it the same look, feel, and command structure.

Two of the three kinds of CASE tools that can be incorporated into the system run under the user environment. They are fully integrated tools—which use all the other capabilities of the system as well, including its generic operating system—and tightly coupled tools, which run under both the user environment and one of the facilities provided by the Software Backplane, the management-control services. The third type, loosely coupled tools, only take advantage of the management-control services.

A monitor function handles all requests for service, responding to the requests by initiating the software in the system that can fulfill a given request. It also invokes the IPSE functions, such as the management-control services, an entity-relation browser tool, and data-base access. In addition, it initiates the CASE applications that are integrated into the environment. Once initiated, the application is still allowed to address the operating system directly, when necessary. Applications can also make requests for operating-system functions via the monitor.

The foremost components in the Software BackPlane are the management-control services that track project development. The management-control facility tracks successive versions of related objects—specifications, designs, program code, test procedures, and documentation—throughout the software life cycle.

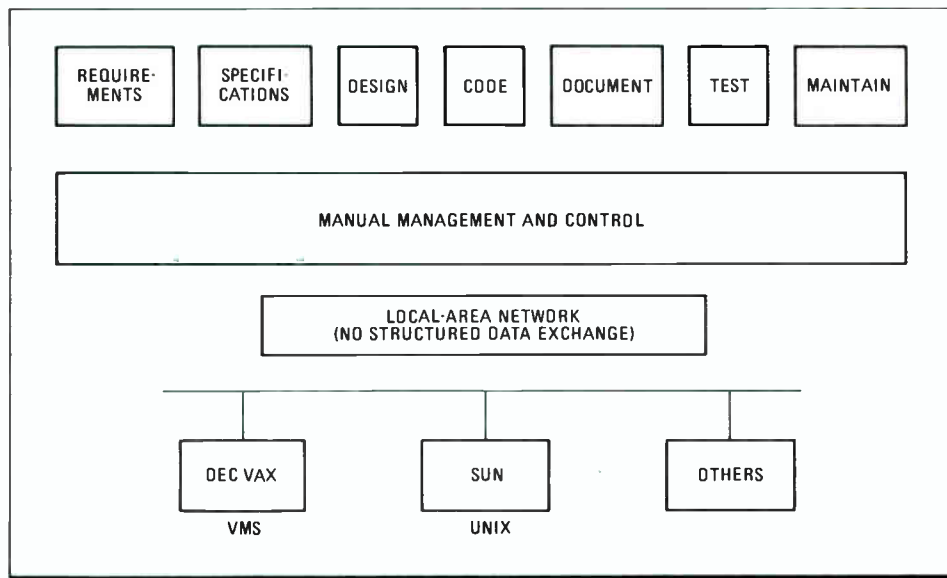
It assures compliance with contract requirements and saves reworking the software, by providing version-level control for software components and establishing dependency relationships—one program in a suite is related to one or more others in the suite. It also provides mechanisms for release control, the logical grouping of objects or sub-releases; for implementing access control; and for integrating user- and third-party-developed software tools.

Among the major management-control services is the history executive, which maintains and controls versions of objects contained in the environment. It uses the host operating-system facilities for carrying out version control. Management-control services provide uniform check-in/check-out of objects, and record the history of changes performed on objects in the system—when they were created, checked out, and so on.

There is also an equivalence executive, which helps users establish relationships among a set of objects produced by tools in the system. When any member of the set of related objects changes, the executive automatically notifies other objects in the set.

A configuration executive provides efficient data exchange between the data base and the host file system. It tracks all source versions of objects, tool versions, and the exact options used to construct each release of a complete software system.

The tool-integration executive maintains an integrated-tool catalog for all registered tools. It supports a uniform method for opening, closing, creating, and deleting tools. "The value Atherton brings



1. OLD WAY. To put together packages of CASE tools, users have had to collect packages that were not built to work together or share the same data base.

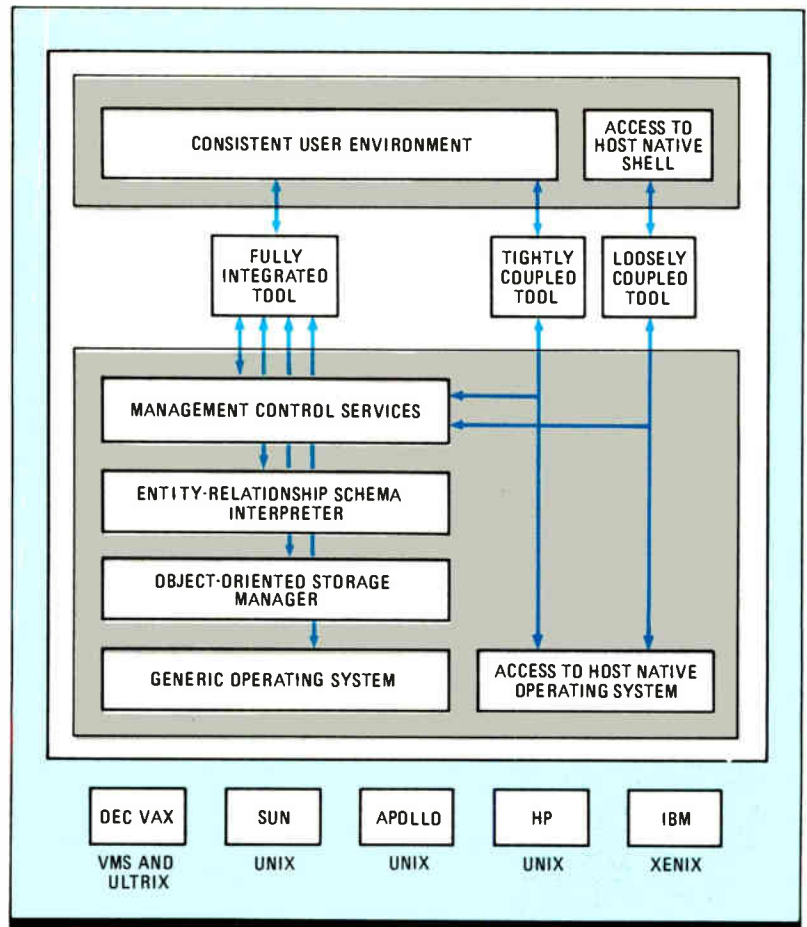
is to allow the user high-level query capability, so he can ask questions of the system about his programs," says Ram Banin, Atherton Technology's president. "This analysis is provided on-line to the user. He does not have to leave his existing application—the editor, for example. All of this capability is immersed in the configuration-management environment. So whatever the user does, the system is creating an audit trail of his activity for later use."

The common data base is the glue that binds all the pieces together in the Software BackPlane. A virtual object-oriented storage manager controls and manages the data base of objects. It provides quick access to large sets of diverse objects in the data base. Each object has a permanent, unique identification number. Software programs needing service from the object manager can provide this identifier to access objects. The object storage manager works in combination with an entity-relation schema, which is like an outline or directory of the contents of the data base, to provide efficient storage and manipulation of the large sets of objects required throughout the life cycle of a software project.

An entity-relation browser allows the user to examine a data model's schema and the specific relationships of components in a data base. It can display all the relationships of a given object, its current revision level, and each of its previous revision levels.

The entity-relation schema interpreter is layered above the object-manager layer and provides a data model of the object-oriented data base. It provides a conceptual representation of the data base only for Atherton Technology applications. This representation indicates logical relationships among objects. Users can, however, instruct the entity-relation schema interpreter to define a schema for any application that runs in the Atherton Technology environment.

The Software BackPlane includes its own generic operating system, which enables it to run on a variety of hardware platforms and under various software operating-system environments. The generic operating system isolates the user and his applications from the different host operating systems and languages. "For example, it would allow users working on work stations that are operating with the Unix operating system and others that are working on MicroVAX II systems to develop software as if all of them were working with the same hardware and software environment," says Banin. An application not only can run on any operating system in the environment, but also can be made to run on whatever new operating systems may someday emerge.

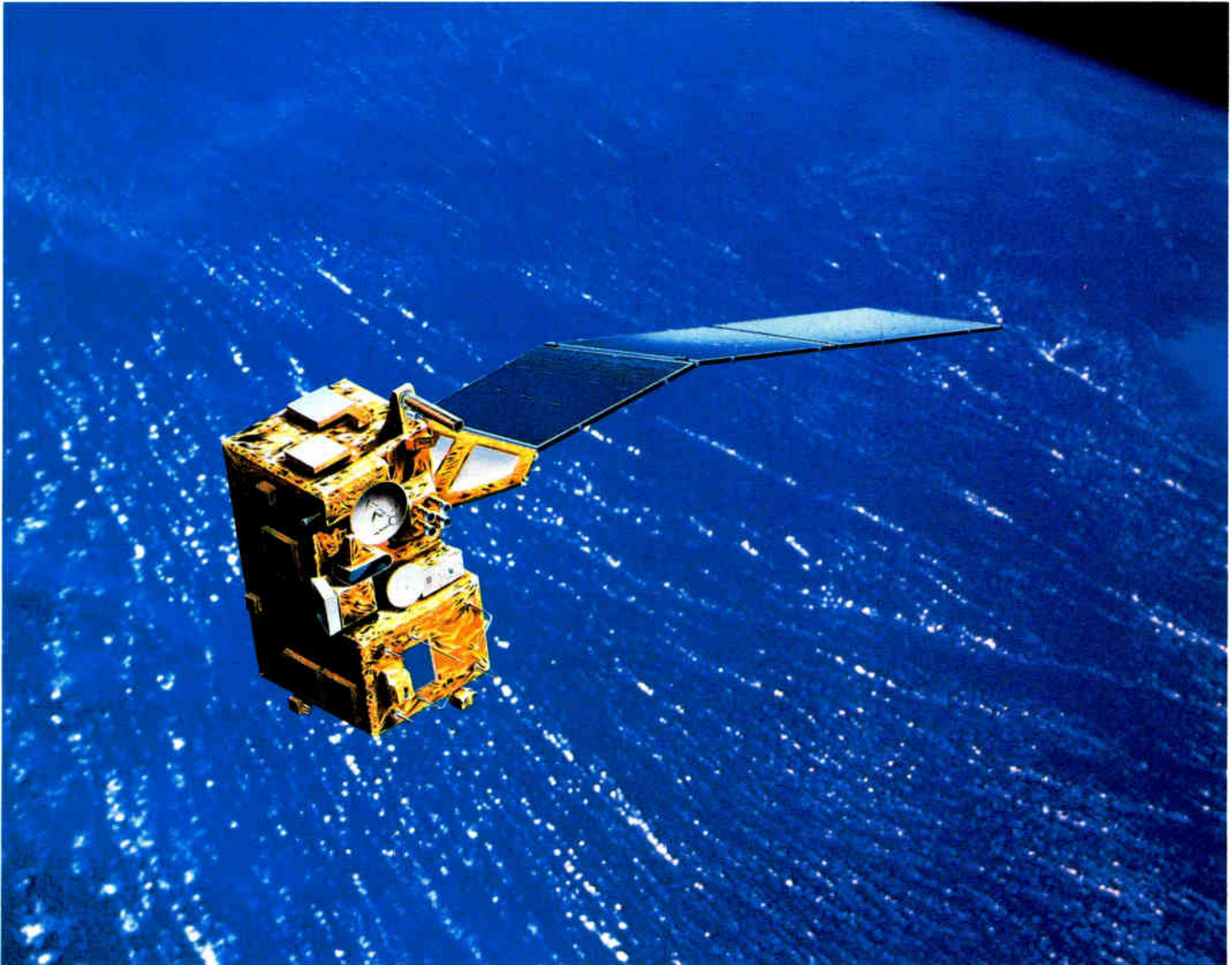


2. NEW WAY. The Software BackPlane links diverse collections of CASE tools to run on different hardware platforms using various operating systems.

Inside each layer, the designers of the Software BackPlane put hooks to allow system integrators or end users to integrate CASE tools into the environment. "For example, in the programming environment we did not write the compilers we use for analysis: Ada, C, and so on," says Banin. "We did not write the editors, either. Rather, we implemented the editor that comes with the software and hardware platform. We supply added value to systems without taking away tools the user is already familiar with."

While allowing the user to choose tools he is most comfortable working with, the Software BackPlane also provides a common user interface to each of these tools. The user-interface layer is based on the industry-standard X-Windows. It provides a set of functions for displaying and manipulating user input, multiple windows, bit maps, cursors, icons, text, and graphics. "The benefit of having a common interface is that the user sees the same user interface on a variety of different hardware platforms—Sun, DEC, Apollo," says Banin. "Software BackPlane unifies today's fragmented system environments, which consist of collections of disjointed CASE tools running on heterogeneous platforms with limited communications." □

For more information, circle 485 on the reader service card.



JAPAN LAUNCHES INTO A NEW ERA IN REMOTE SENSING.

Japan's first Marine Observation Satellite-1 (MOS-1) is now circling around the globe, covering its entire surface in 17 days from 909km up in space.

With three sensors aboard, the new remote sensing satellite beams back an enormous volume of data on diverse aspects of the sea, land and atmosphere. One of the sensors,

MESSR (Multispectral Electronic Self-Scanning Radiometer) senses colors of the sea and land, and recognizes surface features 50m by 50m, utilizing CCD (Charge-Coupled Device) image sensing devices. The MOS-1 is expected to contribute greatly to fishery, agriculture, forestry, resources finding and environment preservation worldwide.

As the prime contractor to the National Space Development Agency of Japan (NASDA), NEC was engaged in system design, system integration and manufacture of key subsystems including major bus subsystems, the MESSR sensor, the DCS (Data Collection System) repeater, ground receiving system and image data processing system.

With more than 30 years of experience in space development, NEC has been involved, as a prime contractor or system integrator, in 23 of the 37 satellites placed in space by Japan.



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NUMBER 138

DIGITALIZATION EXPANDS IN LATIN AMERICA.

In keeping with the ultimate goal of a global ISDN, telecom authorities in Latin America are stepping up their digital network programs.

Telecomunicações Brasileiras S.A. recently awarded NEC do Brasil S.A. a giant order for state-of-the-art digital equipment. It includes NEAX61 digital switching systems (360,000 lines), 5GHz 140M-bit digital microwave communication equipment (1,800 sets), fiber optic communication equipment (200 sets) and PCM transmission equipment (1,300 sets). Most of the systems are to be produced locally with delivery starting this year.

Meanwhile, Empresa Nacional de Telecomunicaciones, Argentina has awarded PECOM-NEC S.A. a contract for NEAX61 digital switches (300,000 lines) and PCM transmission equipment to be installed in the metropolitan and northern areas of Argentina. Local production is scheduled to begin soon. In 1982 NEC constructed a 320-km fiber optic digital telephone system, interconnecting 6 tandem exchanges and 60 telephone offices in the metropolitan area.

NEC is also contributing to the 5-year telecom digitalization project by Compañía Anónima Nacional Teléfonos de Venezuela by supplying NEAX61 digital switches to 97 exchanges in Maracaibo, Puerto La Cruz, and other important areas. For interconnection of these exchanges NEC will supply a 200-km fiber optic communication system.

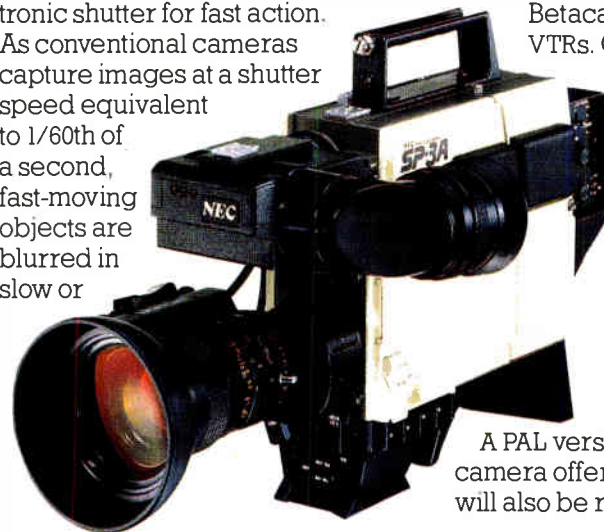
As one of the world's leading suppliers of digital exchanges, microwave and fiber optic systems, NEC is helping to further the digital revolution throughout the world.

NEW CCD CAMERA STOPS ACTION ELECTRONICALLY.

The trend in color cameras for broadcast use is irrevocably "solid-state". CCD cameras are more compact, dependable and durable than tube types and have no comet tails and burn-in when shooting extremely bright objects.

On top of these inherent benefits, NEC's new SP-3A CCD Color Camera has an exclusive feature—the electronic shutter for fast action.

As conventional cameras capture images at a shutter speed equivalent to 1/60th of a second, fast-moving objects are blurred in slow or



still playback on VTR. To remedy this problem, our SP-3A stops the action electronically at 1/60th to 1/2000th of a second, offering precise, clear-cut images.

The SP-3A uses 3 new CCD chips—two for the green channel and one for the combined red/blue channel. This dual green system provides much higher resolution and sensitivity than the conventionally-structured RGB system.

The new CCD camera displays widespread versatility. Besides standalone use it forms an efficient shoot/record system with integral Betacam, MII or 8mm-format VTRs. Options are available for multi-core or triax remote control.

Users' acceptance of this versatile new camera has been remarkable. NBC, a major U.S. TV network, recently sealed a five-year contract to purchase the SP-3A for electronic news gathering.

A PAL version of NEC's CCD color camera offering broadcast quality will also be released.

WORLD'S FASTEST ECL GATE ARRAYS.

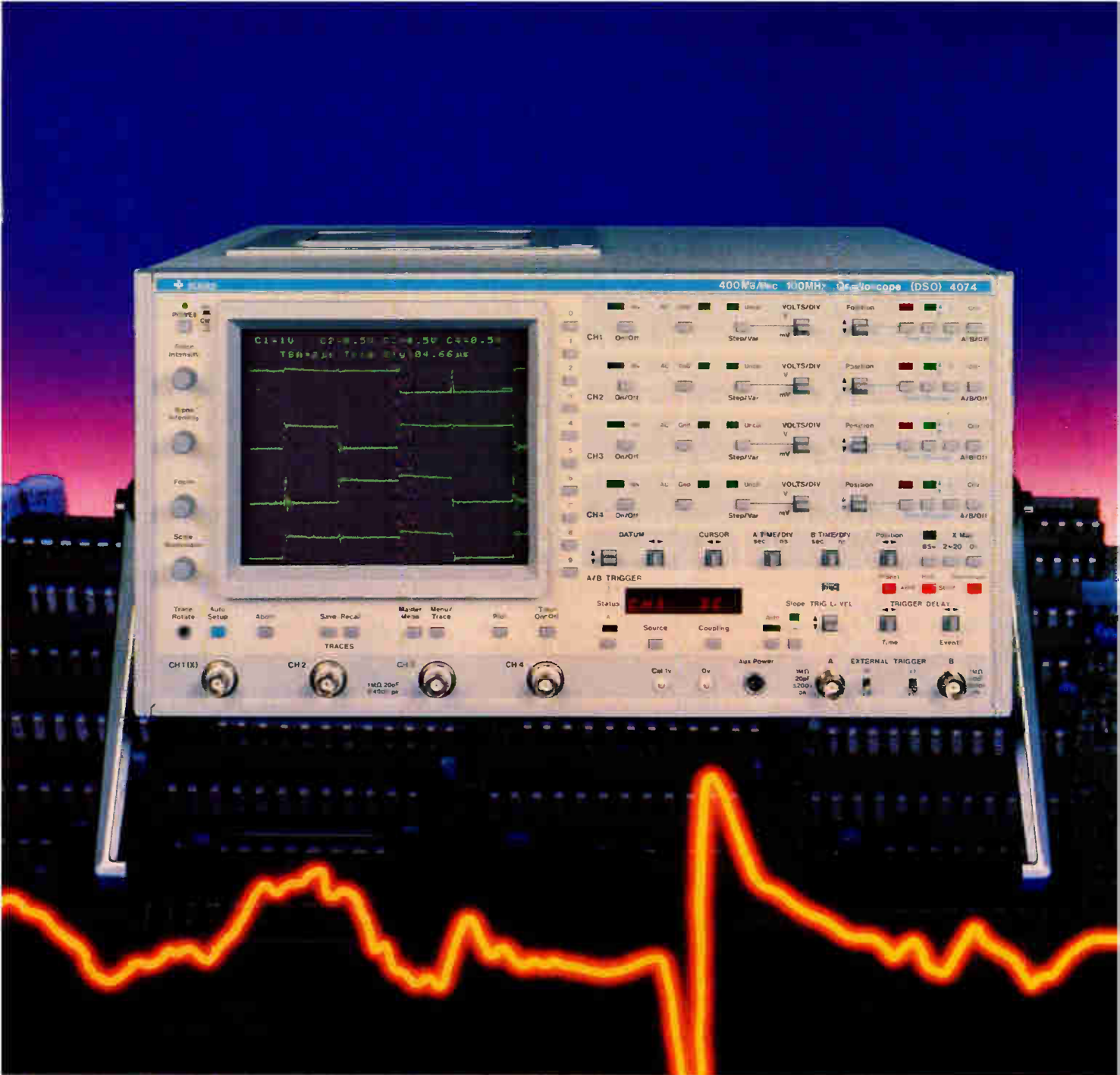
The performance of high-speed silicon logic LSIs is rapidly accelerating. NEC's new ECL-4 gate arrays are the swiftest in the world with a 100ps basic gate delay or 220ps fully loaded.

Combining unprecedented speed and flexibility, the ECL-4 family includes the μ PB6312 with 1,200 gates (400 Full-adders) and the μ PB6303 with 600 gates (200 Full-adders). Both offer 100K or 10KH interface options and ample I/O up to 108 pins.

NEC's ECL-4 gate arrays are available in a choice of 72- or 132-pin PGA packages, and operate in ordinary forced-air-cooling environments since sophisticated heat sinks are standard.

NEC offers 61 internal macros and 33 I/O blocks plus complete CAD tools. The ECL-4 family should hasten the development of speed-oriented computers, graphic terminals, LSI testers and telecom equipment.

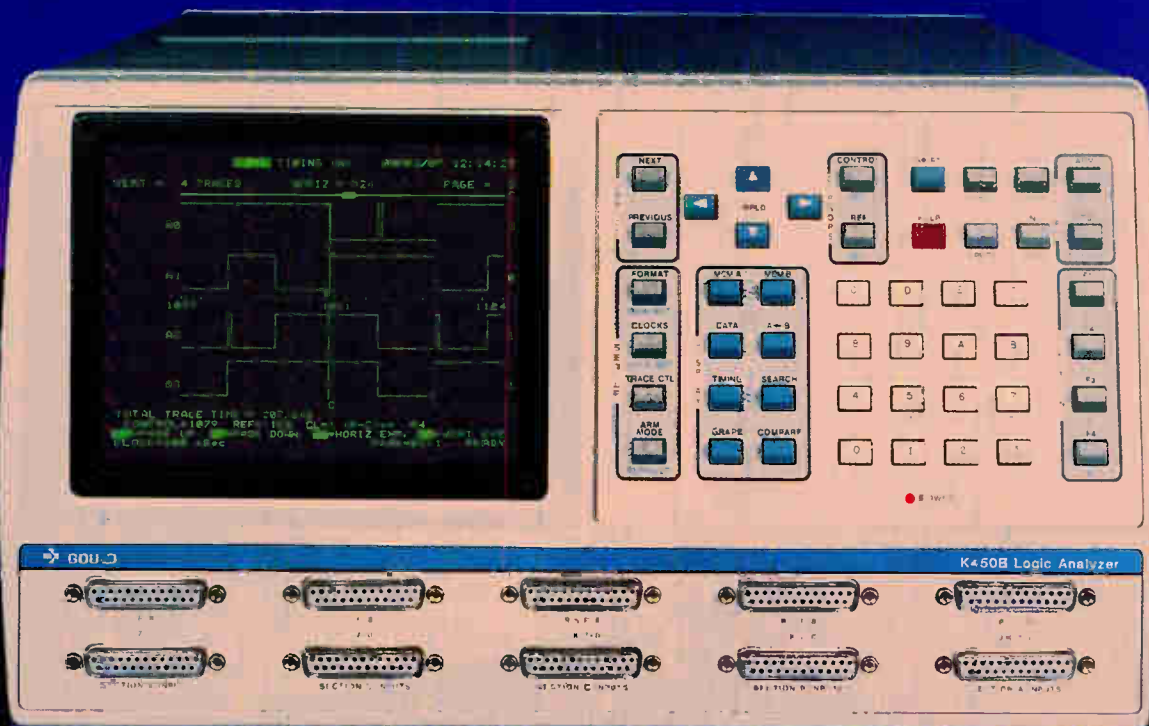
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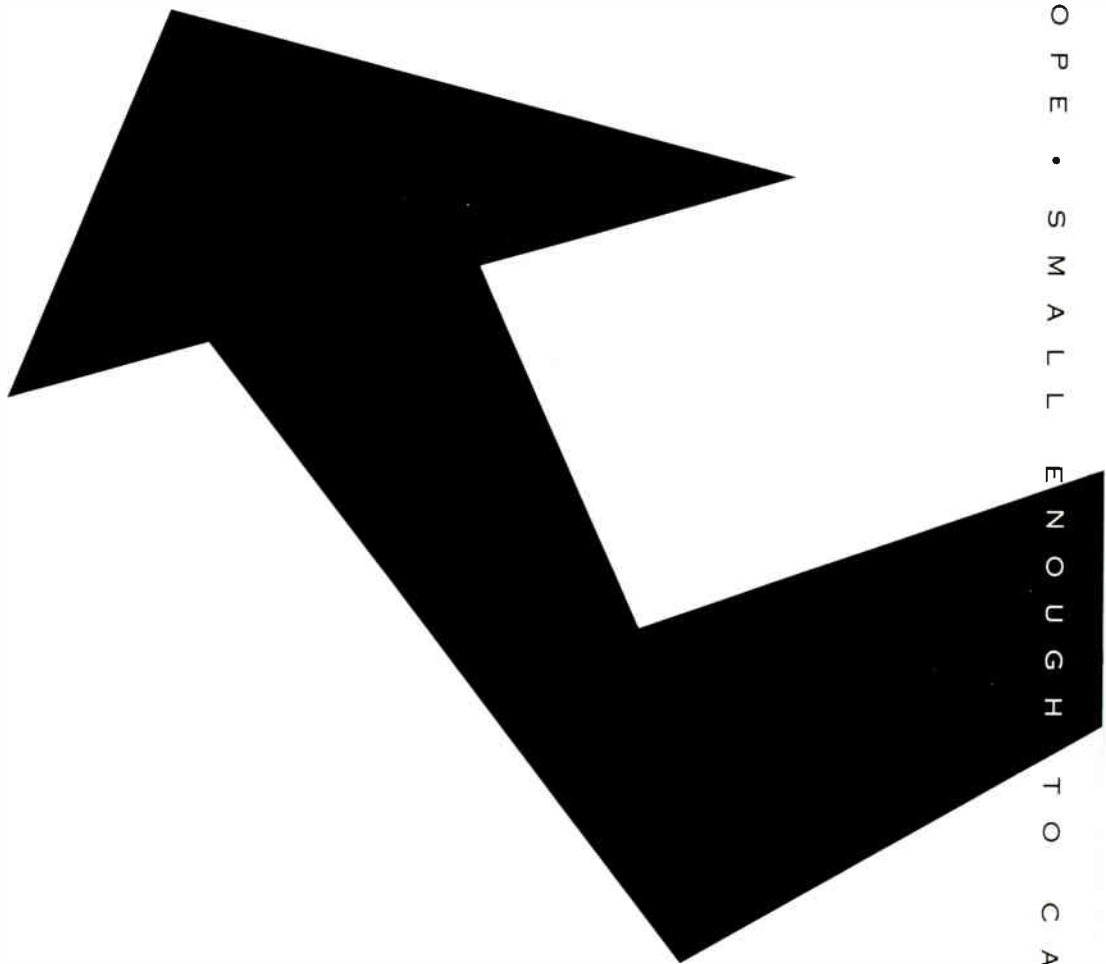
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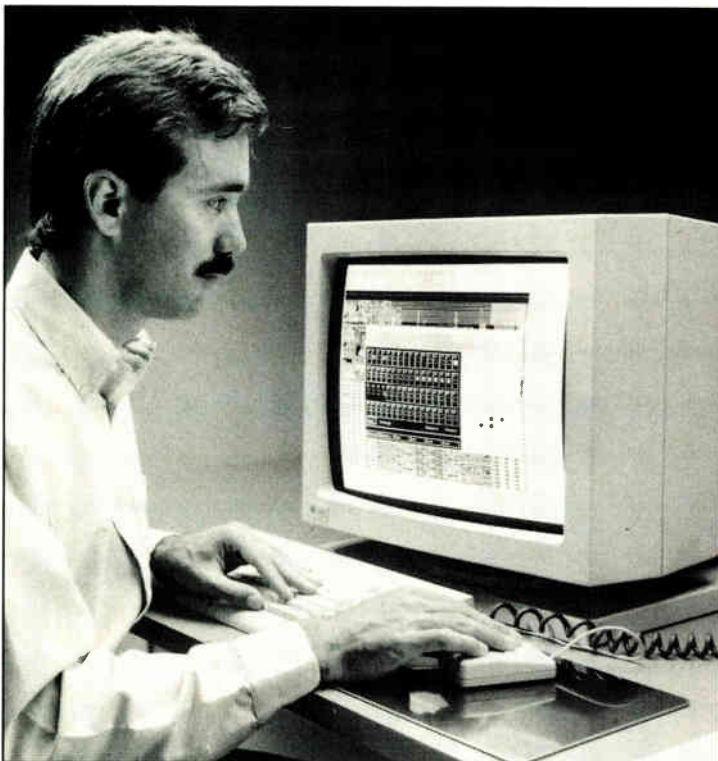
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CALMA BRINGS AUTOMATION TO CUSTOM-IC DESIGN

Custom-chip designers finally are getting an automatic place-and-route tool, plus silicon efficiency that rivals the handcrafted work of expert designers

by Jonah McLeod

The Calma Co. is rolling out a new set of tools that for the first time gives custom-chip designers automatic place-and-route capability—and the tools attain the same silicon efficiency as the handcrafted approach. Called the EDS III Layout System, the tool kit will route standard cells, macrocells, and—thanks to an expert-system approach—the custom circuitry that a designer creates himself (see fig. 1). It comes with a user-friendly graphics interface and can be networked with the popular GDS II layout system also produced by Calma, a subsidiary of



1. USER-FRIENDLY. Calma's EDS III Layout System runs on a Sun Microsystems Inc. work station and provides a user interface with pull-down menus.

the General Electric Co. in Milpitas, Calif.

The superior circuit densities achievable with the expert-system-based EDS III mark a significant step forward. Suppliers of automatic design gear for standard-cell and macrocell layout often claim that their tools produce integrated-circuit layouts that are "almost as good" as those laid out by hand. But for many manufacturers of custom ICs, "almost" just isn't good enough. They demand the most efficient layouts possible, and until now, that could only be achieved by an IC layout designer working meticulously by hand.

The first version of EDS III, for standard cells, will begin shipping in November for \$86,000, including the Sun Microsystems Inc. 3/60 work station on which it runs. In the second quarter of 1988, the company will introduce a version that will handle macrocells as well. It will run on Sun and Apollo Computer work stations and on Digital Equipment Corp. MicroVAX II computers.

Until now, designers performing full-custom IC layout had no access to the automated place-and-route tools and other aids widely used in semicustom design. Instead they had to place each individual device feature separately, in the form of polygons, and then route the interconnections among them, relying on experience.

But the productivity gains achieved by automation in semicustom work had custom-IC designers clamoring for the same kinds of features—especially as they increasingly turned to mixing standard cells and macrocells in with their full-custom designs. The EDS III was created to meet their needs.

The EDS III system is based on a simple place-and-route algorithm guided by a powerful rules-based expert system that mimics the way an IC designer creates a layout. David Hightower, manager of advanced IC systems at Calma, asserts that it can create layouts as efficient in the use of silicon as hand design. In addition, the designer can enter new rules to continually improve the tool.

The system also provides flexibility for the designer. It can route any blocks shaped with right angles—E- and F-shapes, for example—as well as the rectangles and L-shaped boxes handled by most systems. And it allows the designer to route either in channels or between blocks, outside of channels. The first, standard-cell, version of EDS III will accommodate two routing layers. Designers using it will be able to place and route larger macrocells in the layout man-

ually. Hightower says the second version, supporting both standard and macrocell placement, will also accommodate floor planning and will handle unlimited routing layers.

The tool kit represents Calma's attempt to expand on the success it has achieved in the custom-chip layout market with its widely used GDS II Layout System (see p. 95). That tool, which runs on a minicomputer from Data General Corp., can be networked via Ethernet to the new EDS III. But the company wanted to create a new system that was easier to use and that would run on the new generation of less expensive work stations. As a result, EDS III was written in C, runs under the Unix operating system, and comes with a Macintosh-like graphics interface featuring pull-down menus and other user-friendly features. In addition, the company adapted a significant subset of the GDS II functionality to the new EDS III system.

"One of three goals that the new EDS III system seeks to achieve is to offer design-automation tools to IC designers currently performing full-custom design," says Hightower. "A second is to provide the tools in a modern networked work-station environment."

The final aim, he says, was "to make a system that the logic [systems] designer could use." The EDS III does not quite meet that goal, but it approaches it. Because of the user-friendly elements, the system is a great deal simpler to use than GDS II, which is accessible only to the experienced chip-layout expert; but it falls short of many ASIC layout systems, which are intended for novices. A systems designer, says Hightower, might be able "to sit down in front of the new [EDS III] system without knowing the commands or having a user's guide, and figure out what to do."

EDS III differs from most commercially available tools in a number of ways. One of them is in the placing of standard cells and blocks of cells. In a hierarchical design, standard cells are collected into larger blocks, which are then placed and routed. Most systems typically collect all standard cells into one block, then place and route it with other larger macrocells.

However, in a layout comprising, say, five large blocks and a large number of standard cells, EDS III partitions the standard cells into more discrete elements—namely, a number of large blocks of cells that operate together on the basis of their connective wiring. As a result, the elements can be routed more finely, and the designer need not become involved with the partitioning, with how the standard cells are laid out, or with where they are placed.

With most systems, the tool makes an initial layout and the designer modifies it. But he is restricted in where he can locate large blocks. By contrast, a designer using EDS III is given complete control over the placement and routing of his design. He can place one or more blocks himself before the tool makes its layout, and he can change

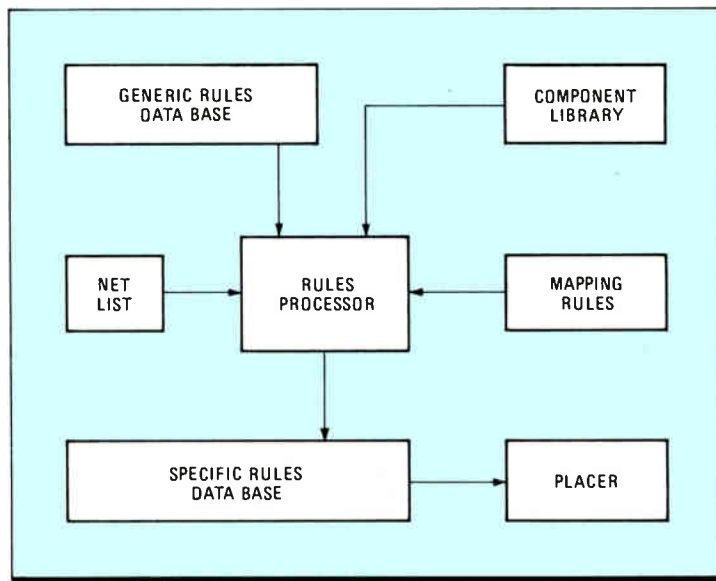
the automatic layout once it is made.

With other tools, the designer is restricted in the shape of the blocks that can be automatically laid out—typically, he's limited to rectangles and L-shaped blocks. But the EDS III block manager uses a switch-box router, which means that any shapes based on right angles are permissible: E- and F-shapes, for example, as well as L-shapes.

In conjunction with the switch-box router, the block manager uses an automatic feed-through router to find routing resources (undedicated feed-throughs) left unused. This function means that no extra wires will be put into the routing channel if the designer wants to conserve routing resources. And while the current-generation router can handle two layers at a time, "we are doing a completely new router to be available in the second version of the EDS III. It will be able to route 'n' layers, to serve designers who are starting designs with three-layer CMOS," Hightower says.

At the heart of the tool set is the block manager (see fig. 2), which performs four functions: automatic placement, delay analysis, spacing, and automatic routing. The key to its silicon efficiency is the combination of a new algorithm with the expert-system approach. "We believe we have a way to get more efficient standard-cell placement than is currently possible today," says Hightower. "Calma has a simple placement algorithm that gets its power from a rules data base."

By contrast, most commercially available tools are based on the simulated-annealing placement algorithm, which is a mathematical description of the way molecules position themselves in a cooling crystal [*Electronics*, May 5, 1986, p. 37]. Hightower says the layouts produced by such tools do not utilize silicon area as efficiently as manual layout. These systems usually place restrictions on the shape of the blocks that can be moved around; they constrain the way standard



2. EXPERT HELP. The block-manager expert system has a generic-rules data base, specific-rules data base, mapping rules, and component library.

and macrocells can be laid out; and they limit the number of interconnection layers.

"Standard-cell placement tools based on [these] algorithms are good for laying out sequential logic and logic that follows a pattern," Hightower says. "Pure random logic is difficult to place no matter which algorithm is chosen. Simulated annealing also begins to bog down with more-complex macro blocks." For example, he says, he once used a simulated-annealing-

in fact, an expert system. It has a generic rules data base, a specific rules data base, mapping rules, and a component library (see fig. 2).

The generic rules data base feeds a rules processor, an inference engine that produces a set of specific rules that it applies to the netlist. For standard cells, the generic rules data base contains such directives as "if pin Z of a NAND gate connects to pin CTL or FF, then place [NAND gate and flip-flop] horizontally adjacent and align pins." The specific rules data base makes a more detailed description of how the flip-flop and NAND gate should be laid out—for example, "place NAND-2D and DFF-2B37 horizontally and align pins 3 and 7."

The rules processor finds instances of different circuit types in the netlist and creates specific rules for laying them out. For instance, it might discover in the netlist a combination of NAND gate and flip-flop repeated several times, and conclude that the structure is a register. It would then create a rule to lay out such combinations in a row or a column.

Calma is developing an interactive editor that will allow the designer to enter rules in the specific rules data base himself. It will be part of the second EDS III release due next year. "With the editor, the designer can add specific rules that would order the placement of large blocks," says Hightower. "Any rule the designer can conceive of for laying out a chip can be inserted into the rules data base."

All the flexibility offered by the EDS III can itself make work for the designer, but Hightower holds that most IC experts won't mind as long as the result is silicon efficiency and better performance. For example, the designer may specify some preliminary wiring that makes it impossible for automatic routing to take place without creating a short circuit in the process. "In an ASIC design environment, that would be unacceptable," he explains. "But in the EDS III full-custom design environment, the designer doesn't care: the system tells him where the shorts occur so he can remove them manually after completing the automatic layout." □

For more information, circle 486 on the reader service card.

TECHNOLOGY TO WATCH is a regular feature of Electronics that provides readers with exclusive, in-depth reports on important technical innovations from companies around the world. It covers significant technology, processes, and developments incorporated in major new products.

Rather than applying brute-force math, Calma made its placement system intelligent; the block manager is an expert system with data bases for rules and a component library

based tool to lay out an IC design containing a couple of thousand standard cells. "We were using upward of 20 hours of CPU time... on a VAX 11/780," he recalls. By contrast, a good IC designer working largely by hand with the aid of a GDS II system could do the job in just about the same amount of time, he says.

Rather than applying brute-force mathematics and consequently more computer time to the problem, Calma chose to make the placement system more intelligent. The block manager is,

WHY CALMA STARTED OVER IN DESIGNING EDS III

Calma Co.'s new EDS III Layout System had its genesis in an effort to update the firm's popular GDS II tool. "There is a tremendous loyalty in the customer base for the GDS II system," says David Hightower, Calma's manager of advanced integrated-circuit systems. "It provides the functionality the IC designer needs to do his job."

But there's a drawback to GDS II: it runs on a Data General Corp. minicomputer, "which costs twice as much and offers half the performance of the current-generation Sun or Apollo work stations," Hightower says. "And the designer's boss cannot justify buying" such expensive hardware.

"Inside of Calma this realization had been around for some time," he continues, and the company was considering two solutions. The first was a project to adapt the GDS II software from Data General's Algol-like DGL language over to the C language and the Unix operating system, to allow it to run on work stations. One part of this thrust was a DGL-to-C translator.

In parallel with this effort was a separate project to write a new IC layout editor with a more modern data base and user interface. In December 1986, the company analyzed the two approaches and decided to abandon the first, in part because the company's software developers preferred starting over to modifying the existing software. So Calma turned its full attention to accelerating development of the new editor. But in the process it decided to retain some aspects of the GDS II—namely, its more powerful, nongraphic functions so beloved of veteran IC designers.

"We used the DGL-to-C translator to move the nongraphical functions over to the new editor," Hightower says. The result is that "a significant subset of the GDS II functionality" in chip layout is available to users of EDS III, so designers can now have the best of both worlds: their favorite parts of GDS II plus a host of new functions and a fresh, sophisticated graphics interface—all available on Sun, Apollo, and Digital Equipment machines.



HIGHTOWER

HOW CALMA PLANS TO FIGHT BACK IN CAD

The Calma Co. is waging a long-term campaign to reassert its leadership in computer-aided design. The Milpitas, Calif., company dominates the market for full-custom integrated-circuit layout tools, but new competition from makers of application-specific-IC layout tools threatens its kingpin status. Calma intends to fight off the threat by introducing a new design system (see p. 92). And with a new, better-focused company strategy, it plans an assault on two new key markets.

Calma's plans mark a turn-about from the strategy it devised two years ago. The General Electric Co. subsidiary decided then to expand its CAD business into architectural and mechanical as well as electronics design. Later, it made even more ambitious plans to break into computer-aided engineering.

However, it soon became clear that the company was biting off more than it could chew. Management started rethinking its plans, and early this year announced a new direction—one that meant "we were no longer going to pursue the goal of being everything to everybody in design automation," says Caroline Mullery, vice president of marketing for design-automation operations. Calma targeted three segments in the CAD market: IC layout, printed-circuit-board layout, and hybrid-chip layout.

Calma is solidly entrenched in full-custom IC layout: the San Jose, Calif., market research firm, Dataquest Inc., says it has 70% of the market, and that market will be worth \$200 million by the end of 1987. Calma itself claims an installed base of 3,000 systems out of a total available market of 4,000.

But Calma isn't invulnerable. Until recently, its main product was the GDS II/32 custom-IC layout software, which runs on relatively expensive Data General Corp. minicomputers. Suppliers of

ASIC tools, offering simple-to-use layout software boasting a graphics interface and running on industry-standard work stations, have started encroaching on Calma's turf.

Now, "Calma is moving to reassert its dominant position in the IC layout market with the introduc-



NEW DIRECTIONS. Carolyn Mullery and David Eggleston are helping Calma focus on three key CAD market segments.

tion of the EDS III," says Isodore Katz, senior market analyst at Dataquest. The EDS III Layout System, introduced this month, runs on work stations, comes with a new user-friendly graphics interface, and is compatible with GDS II.

Besides its usual customers, the veteran IC-layout designers, Calma hopes the user-friendly aspects of EDS III will attract some systems designers as well. They will get "the automatic tools needed to create an efficient mix of full-custom and semicustom layout," says David Eggleston, vice president of electronic design automation sales and support.

In the second market it is targeting, pc-board layout tools, Calma sees wide opportunity. "There is currently no dominant supplier," Mullery says. Equally

enticing, it is the largest of the design-automation markets, worth \$1.4 billion this year, according to Dataquest, and the growth rate will increase to 35% annually by the end of the decade.

To get in on that growth, Calma introduced in February the Calma Board Series Design System. The company says it can do what most layout tools can't.

The system can place and route the high-pin-count ASICs or the high-speed emitter-coupled-logic circuits increasingly found on newer pc boards. It can also handle surface-mounted devices and the fine line traces required to accommodate them, something else other tools have problems with. Finally, it can route up to 32-layer boards, more than enough to route the growing number of 8- to 20-layer boards. Competing tools can't meet any of these requirements, Calma says.

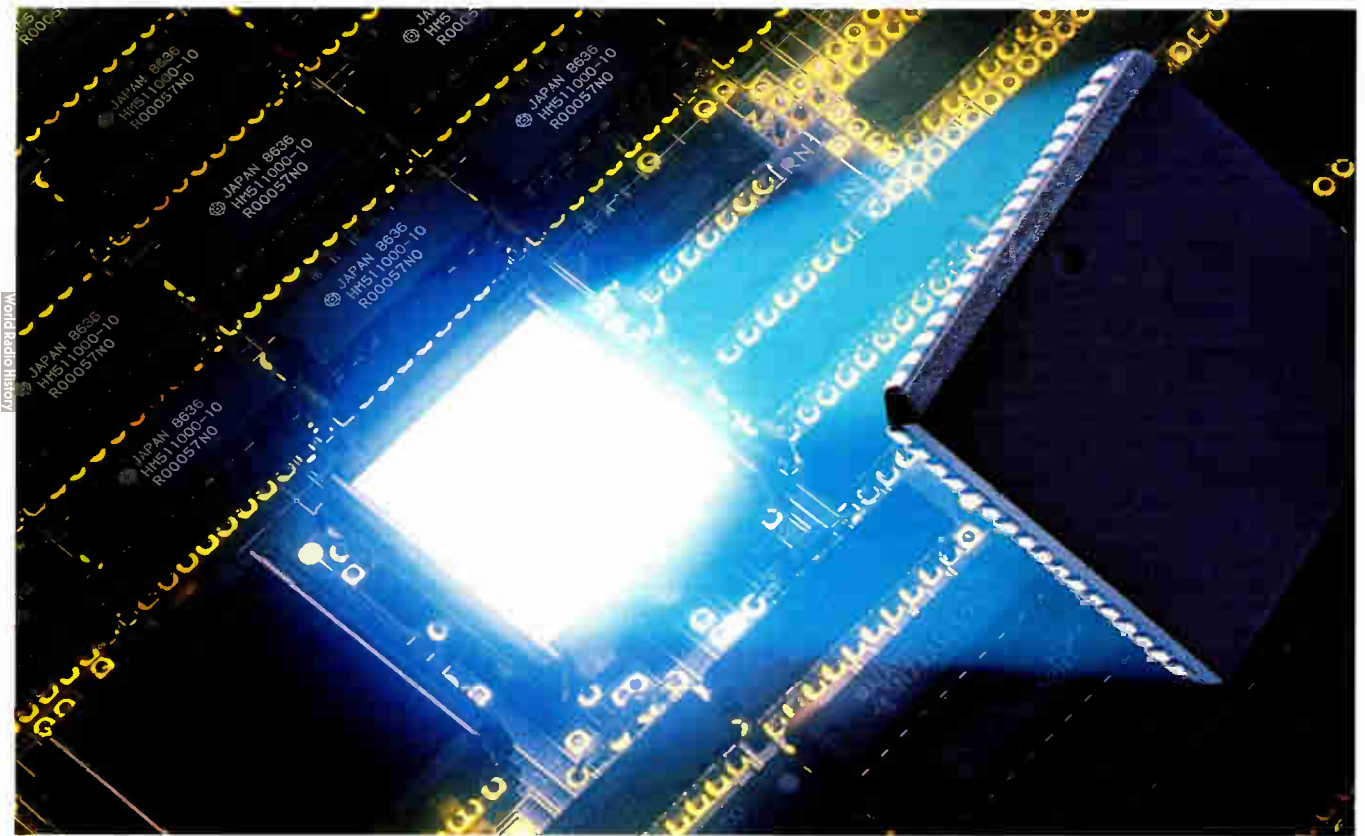
In the third targeted market, hybrid circuits, Calma says it also has something nobody else has: a product specifically for hybrid-circuit layout, the Tech Plus. Competing systems come mostly from

makers of pc-board layout tools who have modified them to perform hybrid layout. "The problem with this approach is that the hybrid designers tend to manipulate the layout more as an IC designer would than as a pc-board designer would," Eggleston says. "Calma's strength in hybrids is leveraged off of our IC design capability."

There are sound economic reasons for aiming at this market, too. "Companies in the military, aerospace, telecommunications, and medical industries all have special packaging needs that only hybrids can solve," Eggleston says. In fact, Calma projects the hybrid market will be worth \$36 million by 1990, and that it will grow at about 15% a year for the next few years.

—Jonah McLeod

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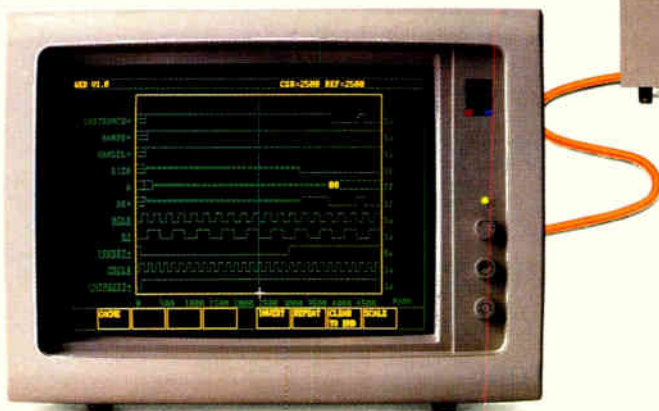
estimated delays prior to layout for accurate results. Cadnetix' powerful CAE tools verify an ASIC design quickly. Our Configurable Analysis Engine, a powerful network resource, provides accelerated logic simulation, worst-case simulation, and fault simulation.

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Circle 97 on reader service card

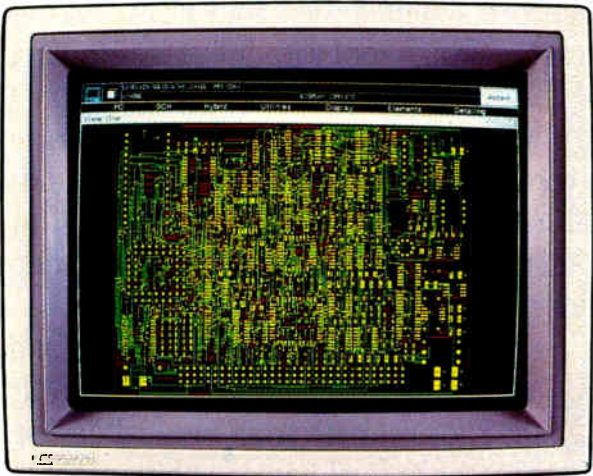
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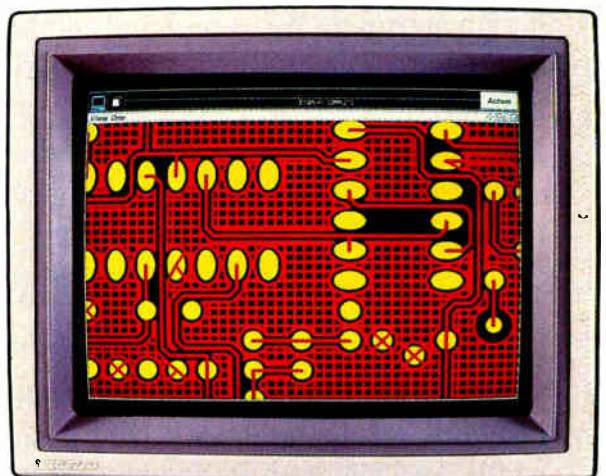
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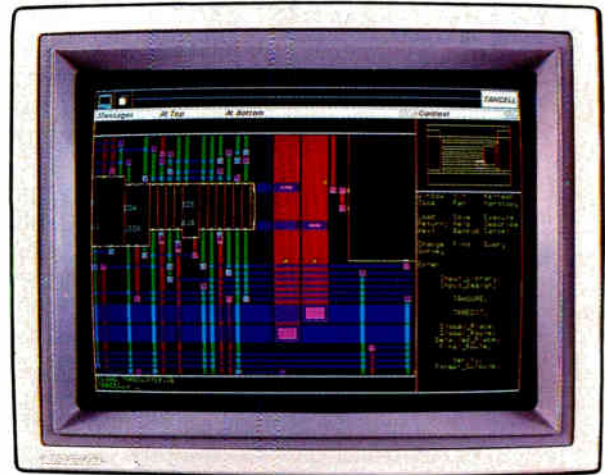
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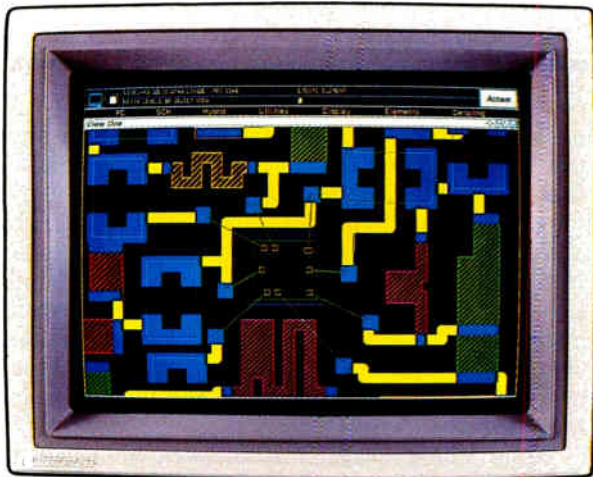
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64-bit mechanical design packages and electronic publishing software round out a system for total product development

INTERGRAPH

UPDATE: VMS EMULATION IS A WINNER FOR ELXSI



THIS SUPERCOMPUTER ALSO RUNS VAX/VMS PROGRAMS

With its new software, the Elxsi 6400 mini-supercomputer runs applications from the most popular computer environments for engineering and scientific institutions.

Elksi Corp. looks to be winning its bet that VAX/VMS shops want a way to expand into minisupercomputer territory. Last year, the San Jose, Calif., company introduced EMS [*Electronics*, Sept. 4, 1986, p. 74], an emulation of the popular VMS operating system offered on Digital Equipment Corp. VAX superminicomputers. EMS runs on Elxsi's System 6400 64-bit mini-super, and so VAX/VMS users now have a way to easily in-

crease the capacity of their computing installations. The System 6400's top speed of 80 million instructions/s is roughly six times that of the VAX 8800, according to Elxsi.

"My wild guess is that 20% of our customer sites have EMS and about half of those are using it intensely," says Robert Olson, director of software development. For example, a couple of cus-

tomers sites where EMS is the primary operating system and the principal development environment are Grumman Corp., Bethpage, Long Island and McDonnell-Douglas Corp. in Long Beach, Calif. "Both bought the machine for its performance, but EMS was the clincher to the sale," says Olson.

The Elxsi software engineers had also planned to extend the company's data-base management system, EDMS, to run under EMS, but have since changed their minds. "We threw in the towel on a proprietary product," says Olson. The company concluded it made more sense to offer industry-standard data-base management systems that would be supported by the data-base vendors than to offer a proprietary version that Elxsi would have to maintain. EDMS was the company's version of Ingres from Relational Technology Inc., and so Elxsi is replacing it with the real Ingres, which will run under all four Elxsi operating systems: EMS, its own Embos operating system, and both major versions of Unix, AT&T System V and Berkeley 4.2.

And Elxsi has an agreement with Oracle Corp., Belmont, Calif., to adapt its Oracle data-base management system to Elxsi's operating systems. "We are taking the same standards approach with data bases as with operating systems," says Olson. —Tom Manuel

UPDATE: GaAs LSI FROM VITESSE IS ON TRACK



BIT-SLICE ICs KICK OFF ERA OF COMMERCIAL GaAs LSI

Vitesse's 29240 bit-slice LSI members are functionally compatible with their AMD equivalents, but operate 100ns faster and are two to three times faster.

A year ago, Vitesse Semiconductor Corp. set out to usher in the era of large-scale-integrated gallium arsenide chips with GaAs versions of Advanced Micro Devices Inc.'s 2900 series bit-slice parts [*Electronics*, Sept. 18, 1986, p. 61]. It has succeeded admirably. The three VE29G00 parts and Vitesse's 1-K-by-4-bit static random-access memory all came out on schedule.

And now the Camarillo, Calif., company is introducing a second generation of GaAs LSI parts, 1,500- and 4,500-gate arrays and a new 3ns 1-K static random-access memory (see p. 48). It has also reduced the prices of the VE29G00 family. The 29G00 bit-slice family members are functionally compatible with their AMD equivalents, but the Vitesse parts are two to four times faster than the AMD ECL parts.

Now that Vitesse is able to make the only

commercial enhancement/depletion-mode GaAs parts—a mode with much lower power dissipation than the depletion mode—and can produce them in volume, it has moved the bit-slice parts into distribution. The first distributor chosen by Vitesse is Zeus Components of Port Chester, N. Y., a distributor that specializes in the military market. Vitesse soon will be expanding its distribution to other U. S. distributors with more commercial focus and to distributors in Japan and Western Europe, says Pat Hoffpauir, executive vice president.

While Vitesse says it is fully capable now of cranking out the LSI parts in volume, it is just ramping up production because its bit-slice customers are still finishing their product development. But the company is ready to run up to 5,000 wafers a month and expects volume deliveries to begin very soon. In addition, Vitesse anticipates receiving some high-volume orders for the SRAM chip.

Vitesse has had more than six months to refine the manufacturing process and increase yields on the new series. The expected yields of more than 30% on the bit-slice parts and well above 40% on the RAM have materialized, and volume prices have plunged substantially below the \$100 barrier the company hoped to reach by the end of 1987. —Tom Manuel

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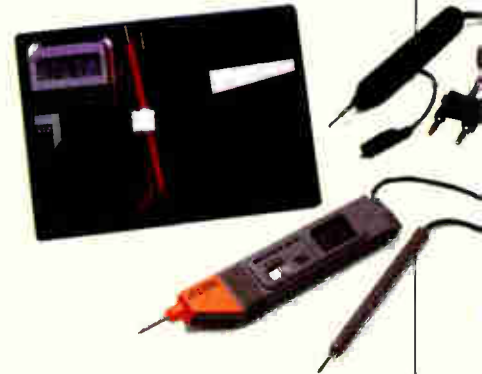
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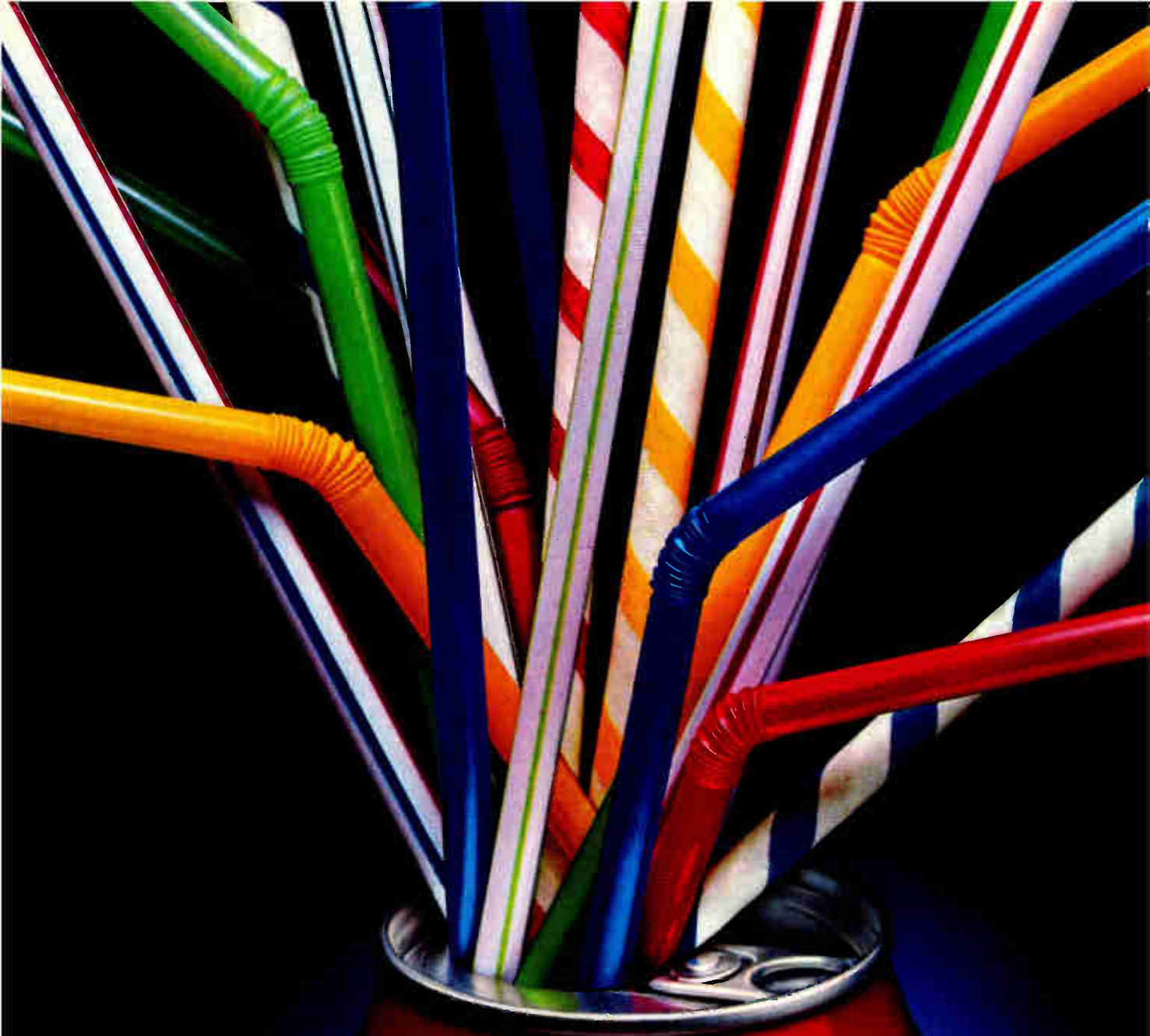
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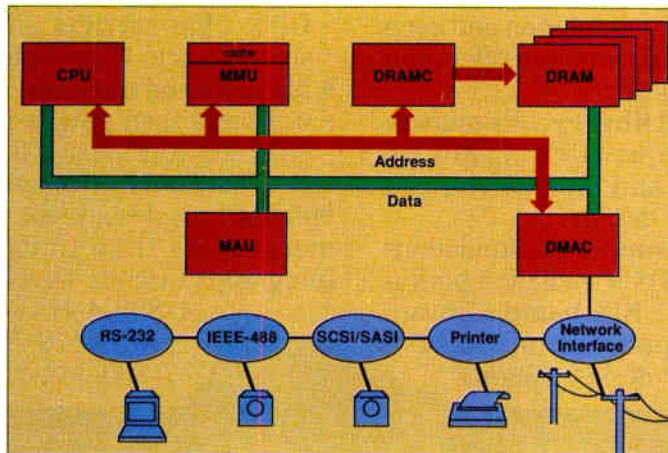
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AT&T's newest system design offers a cache memory that runs at 20 to 30 MHz.

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MILITARY/AEROSPACE NEWSLETTER

BY FALL, THE LOW BIDDER MAY NOT ALWAYS WIN THE CONTRACT AT DESC

Low prices alone won't get you a supply contract anymore with the Defense Electronics Supply Center in Dayton, Ohio. Seeking to reward reliability—and to assure quality deliveries—DESC has notified suppliers that it will begin certifying "quality vendors" this fall. Suppliers who have steered clear of "major quality problems" in 99.5% of their deliveries will now be eligible to win competitive contracts even if their bids come in as much as 20% higher than the lowest competitive bid, says Eleanor Holland, a DESC procurement analyst. Among such quality problems, DESC listed recurring field failure, improper packaging of electrostatic- or electromagnetic-sensitive components, and unauthorized substitutions. More than 40 companies have already applied for favored-vendor status, and Holland expects several of those to gain approval by 1988. □

DEC FIGHTS AIR FORCE OVER 'ILLEGAL SPECS' IN COMPUTER INTERFACE RFP

The General Services Board of Contract Appeals will hear testimony this week from the Air Force and Digital Equipment Corp., which charged in August that the Air Force included "illegal specifications" in its request for proposals for the Standard Multiuser Small Computer Requirements contract. In August, an administrative law judge within the GSA suspended action on the program pending a hearing before the Board of Contract Appeals in August, setting the stage for the mid-September showdown. DEC says the Air Force solicitation unduly restricts competition by requiring that the chosen system conform to AT&T Co.'s proprietary System V Interface Definition. Ultimately, the RFP requires that the chosen system be adapted to conform to the Institute of Electrical and Electronics Engineers' portable operating-system interface, a pending standard. DEC says it supports the future IEEE standard, and that the imposition of an interim specification is an undue hardship. □

NASA SEEMS LIKELY TO WIN FUNDING FOR SPACE STATION ...

The National Aeronautics & Space Administration should win its battle to fund the space station project in the 1988 budget, even though Sen. William Proxmire (D-Wis.) is still trying to rally support for his plan to kill the program. The senator has opposed the space shuttle and other high-profile space programs in the past without result, and an aide to the HUD-Independent Agencies Subcommittee of the Senate Appropriations Committee, which Proxmire chairs, concedes this fight is likely to be another losing effort because the space station enjoys bipartisan support. Proxmire maintains that the \$767 million earmarked for the space station in the 1988 budget would go a long way toward cutting the federal deficit while leaving money for other space-science projects. He calls the space station "ill-conceived" and says it "has no mission." NASA calls the space station "essential." □

... BUT PROXMIRE PUSHES FOR A PRIVATELY FUNDED ALTERNATIVE

Sen. William Proxmire is pushing for a privately funded alternative to the space station—the Industrial Space Facility—as a replacement for the long-term expense of NASA's project. A team made up of Boeing, Lockheed, Westinghouse, and Houston's Space Industries is developing the "man-tended" research platform, and could deploy it with a single space shuttle mission as early as 1990—five to seven years before NASA's space station is operable. The consortium will pay for construction and launch, and it plans to lease the facility for research—but like NASA, it sees its program as an adjunct to the space station. Comparing the two, says a NASA spokesman, "is like comparing a rowboat to the Queen Mary." □

MILITARY/AEROSPACE NEWSLETTER

WINNERS OUTNUMBER LOSERS AFTER ISRAEL CANCELS THE LAVI

The Israeli government's decision to scrap the Lavi fighter plane project was welcomed by the U. S. government, but not by the several U. S. firms involved in the project. These include Lear Siegler, which developed the flight-control system; Pratt & Whitney, which would have supplied the engine; and Grumman, which would have built the Lavi's wings and tail. Another U. S. firm, General Dynamics, did score on the deal: it will sell Israel 75 F-16s in place of the Lavi jets. While Israel Aircraft Industries will have to lay off several thousand workers as a result, other Israeli firms will benefit: Tadiran, Elbit Computers, Elisra, and the Rafael Arms Development Authority should end up with increased orders or new contracts for alternative projects. □

GAO SLAMS AIR FORCE PLAN FOR INTERIM AMRAAM MISSILE

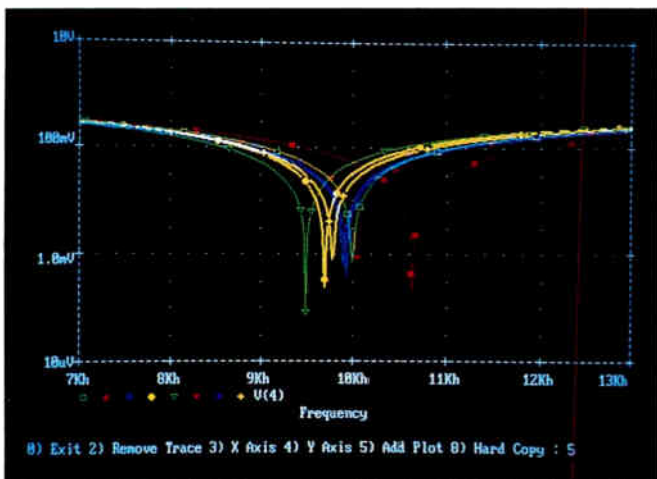
The Air Force's plan to deploy an interim design of its troubled Advanced Medium-Range Air-to-Air Missile takes unnecessary risks, charges the U. S. General Accounting Office. The interim design does not include software to protect the AMRAAM from electronic countermeasures that could steer the missile off course. Deploying the interim software program, called Tape 3A, in place of the full-production system, Tape 4, will allow the Air Force to maintain its scheduled 1989 initial deployment. But the GAO warns that using an "unstable design increases production risk." That instability is reflected in changes that continue to be made or planned in the Tape 3A version—the extent of which "will not be known until additional tests are completed," the report says. "Beginning production before the design has stabilized increased the risk that production schedules will be disrupted, the system will not perform satisfactorily, and retrofit programs will be required." Tape 4 is getting closer—the first prototype is due in October—but it will be May 1989 before the government has fully tested that system. □

NINE FIRMS FORM UK CONSORTIUM TO PARTICIPATE IN NATO FRIGATE PROGRAM

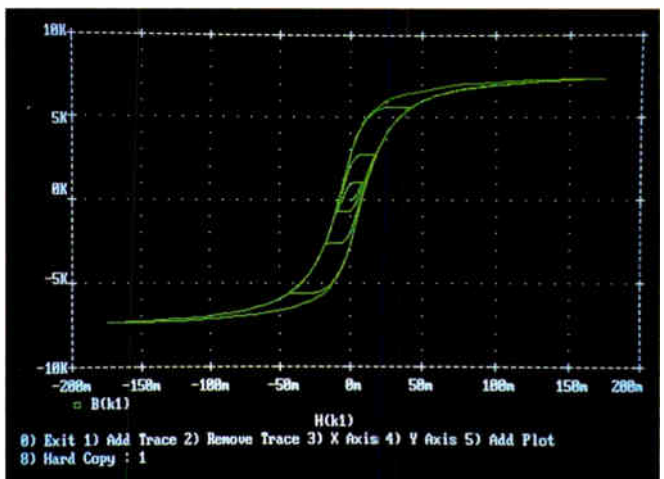
Nine British electronics, aerospace, and shipbuilding companies are forming the Supermarine Consortium Ltd. to represent British interests in the eight-nation NFR-90 project to design a new frigate for NATO. The program is unique in that the work is being split up among nine NATO nations, with each country putting together its own contracting team to handle its share of the project. SCL will become the UK shareholder in the International Joint Venture Company, which will handle the project-definition phase of the frigate program. The U. S. shareholder is Westinghouse. The ship is not scheduled to go into service until the turn of the century, but the three-year first phase of the program will begin after the Oct. 21 signing of a memorandum of understanding between the nations involved: Canada, France, Italy, the Netherlands, Spain, the UK, West Germany, and the U. S. The nine equal partners in the British consortium are British Aerospace, Ferranti, Plessey, Racal Electronics, Rolls-Royce, Thorn EMI Electronics, VSEL, Vosper Thornycroft, and Yarrow Shipbuilders. □

ROCKWELL, GEC AVIONICS JOIN IN BID FOR NATO NAVIGATION SYSTEM

The Guidance Systems Division of GEC Avionics Ltd. of the UK is teaming with Rockwell International Inc.'s Autonetics Systems Division to develop a navigation system based on ring laser gyro technology for NATO. The two hope to win a contract for NATO's Ships Inertial Navigation System with their design, which is based on Rockwell's G16B precision laser gyro and a single 3-axis electromagnetic accelerometer. A control and display unit from GEC completes the system. □



Monte Carlo analysis of a notch filter



B-H curve from a core in the PSpice transformer library

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- The Probe "software oscilloscope", allowing interactive viewing of simulation results. The photographs above are Probe displays.
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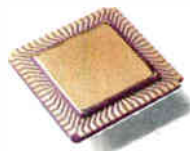
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World Radio History

Circle 109 on reader service card



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NEW PRODUCTS

MITEL'S SIMULATOR BOARD SAVES TIME IN DESIGNING-IN ISDN

THE \$1,500 PRODUCT WILL HELP DESIGNERS ANALYZE ITS ISDN CHIP SET

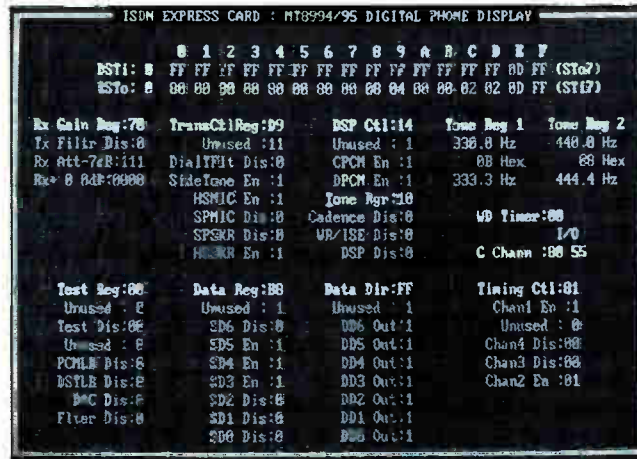
If a computer hardware designer is unfamiliar with the complexities of the emerging Integrated Services Digital Network, it can take him up to a year to learn enough to design ISDN into his new products. Now Mitel Corp. has come up with its Express Card evaluation board and associated software to get around this problem.

The promise of ISDN—to deliver high-speed integrated voice, data, and video services to the user's desktop—also means that equipment designers must expand their expertise beyond data communications and into telecommunications technology. The Express Card eases the pain of coping with complex protocols, multiple channels, and new bus architectures by providing pre-configured interfaces, evaluation software, and drivers for each component.

NEW DIRECTION. "After we pounded out our ISDN family of integrated circuits over the past year, we realized that our customers were having trouble assimilating them," says Al Hawtin, assistant vice president for component marketing at Mitel's Semiconductor Division in Kanata, Ontario, Canada. "Our aim with the Express Card is to provide a development environment that includes all the components on a single board so the designer could access each component and analyze it."

The Express Card comes with 12 Mitel ICs that can be configured in a variety of ways to simulate an ISDN system. The chips include the MH89760 for implementing the T1 interface for 1.544-Mbit/s primary-rate service in the U.S. and the MH89780 for implementing the interface for the 2.048-Mbit/s primary-rate service that is the European standard.

For 192-Kbit/s basic-rate service, the card has an MT8972 chip for the U interface—the point where the 192-Kbit/s channel is divided into two 64-Kbit/s data channels and a 16-Kbit/s signaling channel. It also has the MT8930 S-inter-



EASY READ. A typical screen displays the bit stream on each channel in the top two lines; register contents are listed underneath.

face chip linking the subscriber's on-premises distribution lines to specific devices such as digital telephones, work stations, and telemetry devices. Also on the board are eight special-purpose chips, among them the MT8952 High-Level Data Link Controller, which formats data consistent with the CCITT's X.25 packet-switching protocol; the MT8980 Digital Crosspoint Switch; and digital-phone chips conforming to both U.S. (MT8994) and European (MT8995) specifications.

"It would typically take four months for a customer to pull together the entire process of wire-wrapping the board, debugging, and getting the interface to work," says Hawtin. With the Express Card plugged into an IBM Corp. Personal Computer or compatible, designers bypass that stage and begin familiarizing themselves with the chips the first day.

Mitel saved additional months by writing the software drivers for each component. "A customer can save six months of his time-to-market for a relatively simple device like a digital phone, and sometimes as much as a year for more complex equipment," says Hawtin.

With telecommunications technology already well entrenched, conversion to ISDN will result in billion-dollar markets for digital products. Market research

consultant Ovum Inc., Princeton, N.J., predicts the combined U.S. and European market for ISDN products will grow to \$11.3 billion by 1991. Expenditures for private branch exchanges alone will total some \$6.7 million. Digital feature phones will grow to a \$1.6 billion market by 1991, and integrated voice and data work stations will be a \$700 million market.

Although other IC vendors have evaluation and development boards for their products, none packs so many chips for evaluation—because few chip makers offer as extensive a family as Mitel. Mitel manufactures telecommunications

equipment as well as ICs, and its market strategy is to "put our chips in every one of the interfaces," says Hawtin.

The development software accompanying the Express Card gives users direct access to register-level activity in every board component. By calling up a separate menu screen for each IC, users can select the device of interest and change the control, status, and activity registers. By pressing the cursor keys, they can step through the valid states of each device. A simple ISDN system can be configured by using a channel-selection menu at the top of the screen to connect the digital phone chip, for example, to the S interface, or to construct a U interface at the termination of a T1 line. A help screen can be called up to explain the options available if the designer hits an impasse.

BOARD LAYOUT. By exercising the chips, users familiarize themselves with the interface and with the architecture of Mitel's ST-bus link between chips. Another major advantage, says Hawtin, is that the ISDN interfaces have already been physically configured on the Express Card. "Interface chips tend to be very layout-sensitive because of the high bit rates, and high voltage in the case of a T1 line," he says. Mitel has already solved problems arising from clock noise. "We expect people to lift the

board layouts right off the Express Card because they know it works to their satisfaction," says Hawtin.

Similarly, transformers—particularly in T1 applications—are surprisingly challenging to specify. Ordering them requires an 8-to-12-week lead time. "So we provide the customer with the transformer specifications through the Express Card," says Hawtin.

Express Card software runs on an IBM PC or compatible running under Microsoft Corp.'s MS-DOS 2.0 or higher operating system. Software written in C is available now supporting the T1 and S interfaces and digital phone chips. Software for the remaining chips will be released over the next four months. Customers who purchase the Express Card package will automatically receive software upgrades as they become available.

PROTOTYPES. Designers prototyping equipment can use software drivers written by Mitel for the devices on the board and write applications software using the PC. As the prototyping advances, the PC's narrow data bandwidth becomes a limiting factor. To solve that problem, Mitel has provided two 2,048-Mbit/s connectors on the board that allow the application to be moved to a faster processor. This technology transfer involves rewriting the software developed in the MS-DOS Intel 8088 environment to support the prototype environment, but that was not considered a serious problem by Mitel's alpha-site customers, says Hawtin, because it is the sort of thing they have done before.

The Express Card with software and a designer's manual is available now for \$1,500 each in U.S. dollars.

—Jack Shandle

Mitel Corp., 360 Legget Dr., P.O. Box 13320, Kanata, Ontario, Canada K2K 1X5. Phone (613) 592-2122 [Circle 440]

LAN PUTS ETHERNET ON TWISTED PAIRS

SynOptics Communications Corp.'s LattisNet local-area network eliminates the costs of installing shielded cable to implement a 10-Mbit/s Ethernet system by operating over the unshielded twisted-pair wiring for normal on-premises telephone service.

Capable of supplying reliable service for distances up to 330 ft. over two pairs of wire compatible with AT&T's Premises Distribution System standards, LattisNet consists of a Model 405 host module that handles compatibility with the Ethernet specifications and the Model 505 transceiver.

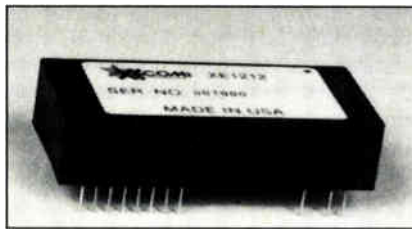
The LAN's transmission distance can be extended 2 km by using fiber-optic cabling and the Model 1010 concentrator as a link to twisted-pair distribution points within the building.

Pricing varies with system configuration but averages about \$500 per node. The products are available now.

SynOptics Communications Inc., 329 Bernardo Ave., Mountain View, Calif. 94043. Phone (415) 960-1100 [Circle 445]

FCC REGISTRATION COMES WITH MODEM

The XE1212 modem from Xecom Inc. simplifies the implementation of data communications by offering a user-transferable Data Access Arrangement



that has already been registered with the Federal Communications Commission.

Capable of 1,200- and 300-baud operation according to both Bell 212A/103 and CCITT V.22/V.21 specifications, the XE1212 interfaces directly with microprocessor-based systems by emulating the transceiver implemented in IBM Corp. Personal Computers.

The compact unit, measuring 2¼ by 1 by ½ in., is available now and costs \$96 each in 1,000-unit purchases.

Xecom Inc., 374 Turquoise St., Milpitas, Calif. 95035.

Phone (408) 945-6640 [Circle 446]

14.4-KBAUD MODEM BOOSTS SPEED 50%

A board-level, 14.4-Kbit/s synchronous half-duplex modem from Rockwell International Corp. offers original-equipment manufacturers of facsimile equipment 50% greater data-transmission speed than the industry standard 9.6 Kbits/s.

The R144HD conforms to the CCITT V.29 facsimile standard and can operate on public telephones. Specifically designed for compact Group 2 and Group 3 fax machines, it is also well suited to personal-computer-based facsimile systems. It operates at 12, 9.6, 7.2, and 4.8 Kbits/s.

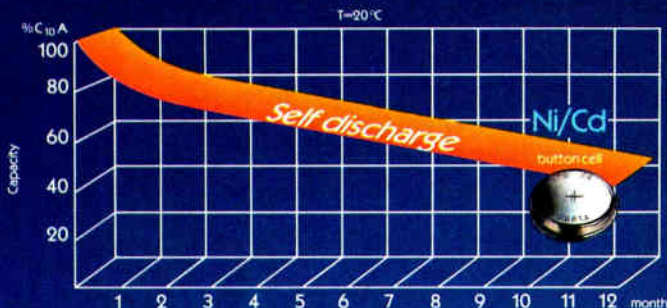
Features include an on-board tone generator for dial-up applications, an adaptive equalizer to compensate for phone-line distortions, and a parallel microprocessor-bus interface to allow the host CPU to monitor and control modem operation.

Available now, the R144HD costs \$140 each in 1,000-unit quantities.

Rockwell International Corp., 4311 Jamboree Rd., Newport Beach, Calif. 92658.

Phone 714-833-4700 [Circle 448]

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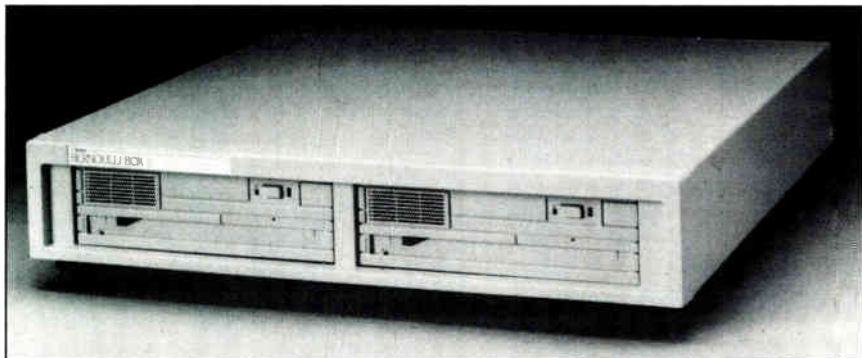
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IOMEGA HIKES STORAGE IN ITS BERNOULLI BOXES

A SMALLER CARTRIDGE SIZE DOUBLES CAPACITY AND PAVES THE WAY FOR A 40-MBYTE DOUBLE-DRIVE CONFIGURATION



PERFORMANCE. Bernoulli Box II systems boast a continuous 6.5-Mbit/s data-transfer rate and a voice-coil actuator that pushes average disk-access time down to 40 ms.

Personal-computer designers can build up to 40 Mbytes of high-performance, removable-cartridge storage into their next generation of products with Iomega Corp.'s latest family of Bernoulli Box drives. The smaller cartridge size in the Bernoulli Box II doubles capacity, to 20 Mbytes, over the first-generation product from the Roy, Utah, company. And the new cartridge lets Iomega employ a 5¼-in. half-height form factor for its drives, instead of the 8-in. form factor used before. The company can fit two of the new drives into a box not much bigger than its original single-drive product.

The Bernoulli Box II systems have a Small Computer System Interface to handle a continuous 6.5-Mbit/s data-

transfer rate—60% higher than most high-end Winchester drives. Engineering features such as buffered data transfer, a closed-loop servo mechanism, and a voice-coil actuator push average access time down to 40 ms. As in the previous Bernoulli Box systems, the removability of the data cartridges makes off-line storage capacity virtually unlimited.

Four variations are offered on the theme. Two products are designed to be installed inside computers. One of the internal drives is the master Bernoulli drive, and the other is a slave drive to upgrade the internal subsystem.

External-drive products come as single-drive and dual-drive subsystems. The single-drive, 20-Mbyte subsystem targets primary mass-storage devices,

auxiliary mass storage where large volumes of off-line storage are required, and backup for large hard-disk drives.

The dual-drive configurations offer the flexibility of using the second drive to double on-line storage or for backing up the main storage.

In its most fundamental form, Bernoulli Box technology depends on the system's ability to control a stream of air that is directed over a flexible disk rotating over a fixed plate. The name comes about because the Bernoulli principle of fluid flow as it passes over the plate. When properly controlled, the air stream makes the flexible magnetic disk behave like a rigid disk at the drive's operating speed, allowing the read/write heads to float very close to the surface without touching it, thereby yielding high bit density along with fast and reliable performance.

The new 5¼-in. half-height drives are available now for all IBM Corp. Personal Computers and compatible machines, such as the product lines from Compaq Corp., Tandy Corp., Unisys Corp., and Leading Edge Hardware Products Inc. Iomega says that drives for additional PCs will be available in the future.

The Model B220x Bernoulli Box II external dual-drive system carries a retail list price of \$2,499. The single-drive Model B120x costs \$1,599. The internal single drive, the Model B120i Master Bernoulli Drive 2, is \$1,299.

Iomega also offers upgrade kits for both single-drive models. The Model B120iu internal drive upgrade kit sells for \$900, and the B120xu Slave Bernoulli Drive 2 external-drive upgrade subsystem is priced at \$1,200. —Tom Manuel
Iomega Corp., 1821 West 4000 South, Roy, Utah 84067.

Phone (801) 778-3170

[Circle 340]

MEMORY UNIT TRANSFERS 140 MBYTES/S

System integrators with applications that demand data-transfer rates unattainable by high-end hard-disk drives can plug into 140-Mbyte/s performance with Zitel Corp.'s solid-state memory. The System 93 Plus transfers data 70 times faster than the IBM Corp. 3380 hard-disk drive.

The solid-state memory can be added in 64-Mbyte increments to a maximum of 512 Mbytes in a 14-by-9-in. chassis, and up to 60 chassis can be daisy-chained to provide 30 gigabytes of mass storage.

Fast average access time, combined with the parallel data transfer from the memory, account for the system's high data-transfer rate.

Data is read from memory as 64-bit-

wide words. The solid-state memory system, made up of 1-Mbit dynamic random-access memories, uses a four-way, on-board interleaving scheme to achieve a 55-ns average access time. This compares with the DRAMs' average access time of 190 ns.

Typical high-end solid-state-memory applications include high-speed radar processing, satellite data downlink, and geological surveys, in which large amounts of data are collected in a brief time period.

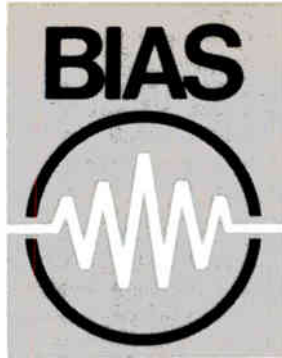
Solid-state memory can also encroach on the Winchester-drive market in conventional applications, says James McBurney, senior marketing manager at the Milpitas, Calif., company. Utilization studies show that 50% to 75% of all

large mainframe disk accesses are made to 2% of the disk drives, and using solid-state memory instead of disk caches in those 2% can deliver a threefold performance improvement, he says. This is because the average access time of a disk cache is degraded by requests that cannot be fulfilled by data from the cache.

Packaged in an 8-ft.-high rack along with battery back-up power supplies, the solid-state memory system has a higher storage capacity per square foot of floor space—500 Mbytes/ft²—than disk memory, which averages about 250 Mbytes/ft².

The memory can be connected into a computer as a disk-drive emulator tied into the input/output port, which would normally contain a Winchester. It can

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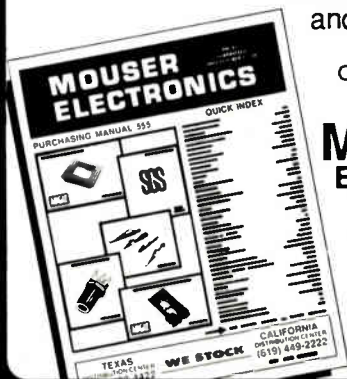
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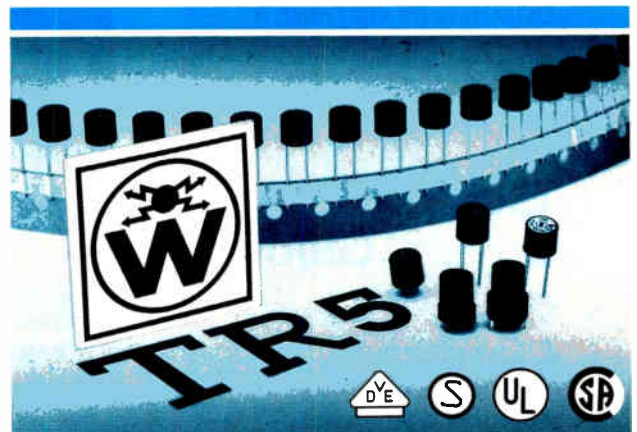
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2. TR 5, 125V to UL 198 G with UL and CSA approval available with radial leads, plug-in pins, or on tape for automatic insertion. Further technical information available on request.

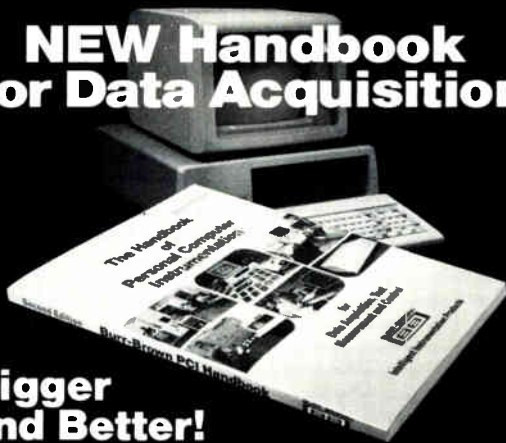


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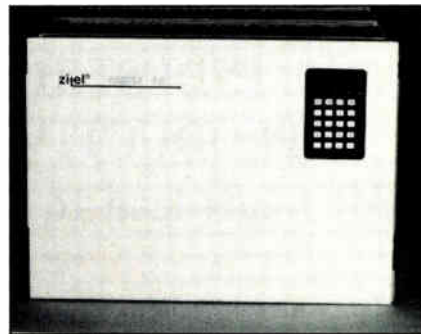
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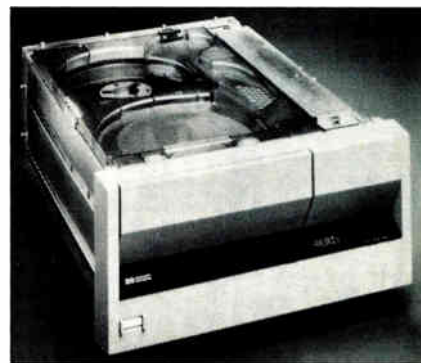
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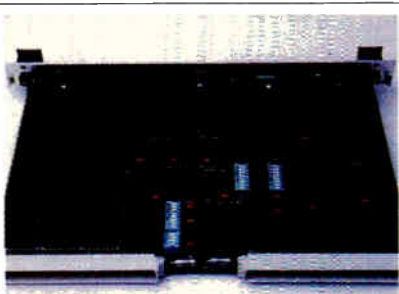
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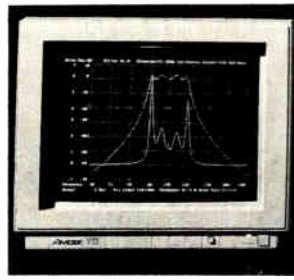
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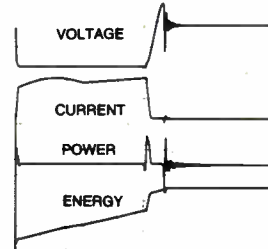


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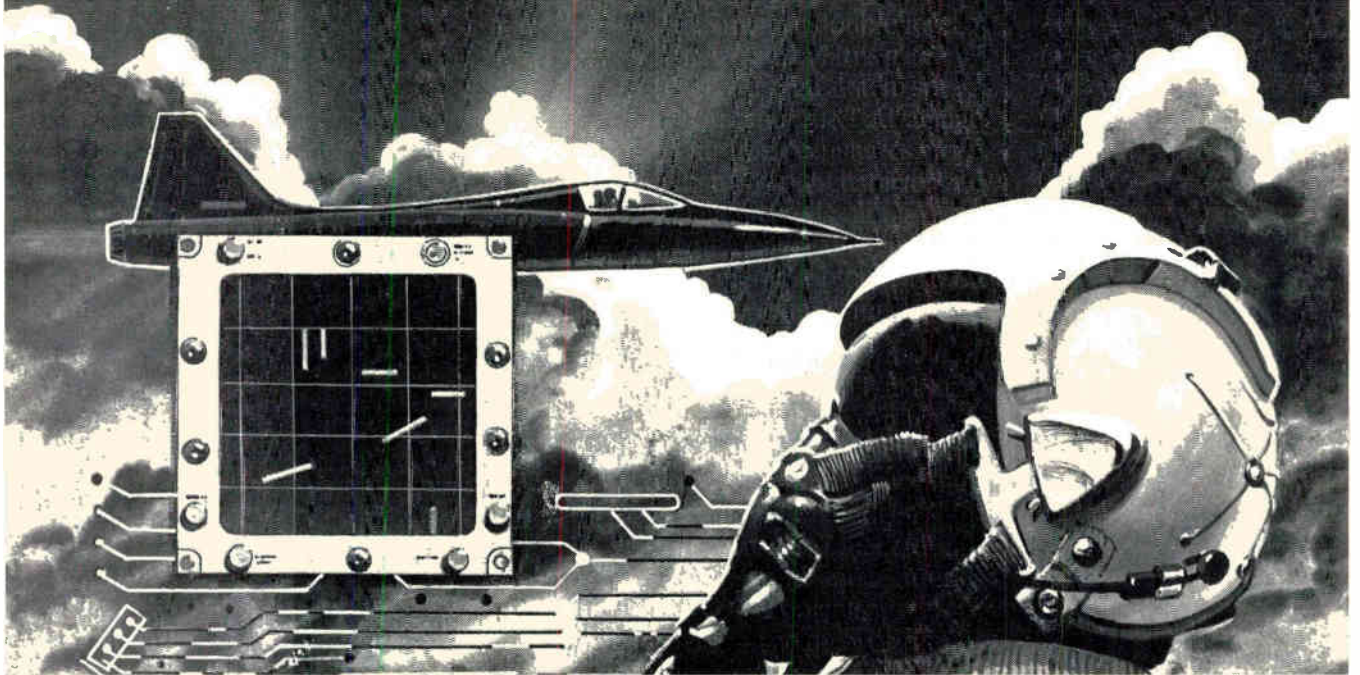
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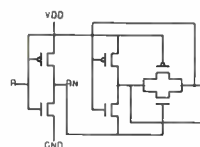
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ELECTRONICS WEEK

EUROPE AGREES ON MOBILE-PHONE NET

The heads of 12 European PTTs, meeting in Copenhagen, have agreed in principle to establish standard specifications for the upcoming pan-European mobile telephone network. Signees are the Common Market big four—West Germany, Italy, France, and the UK—plus Denmark, Belgium, the Netherlands, Sweden, Norway, Finland, Spain, and Portugal. The capitals and largest airports of the countries involved will be equipped first, in 1993, followed two years later with all traffic links between capital cities.

AT&T PUMPS UP COMPUTER LINE...

AT&T Co.'s Data Systems division has strengthened its computer line with the introduction of high-end models for its personal-computer and minicomputer product lines. The 6386 Work Group System, a multiuser PC based on the Intel 80386 microprocessor, supports both Unix System V and MS-DOS applications. The cornerstone of AT&T's strategy to be Unix-compatible across its entire line, the 6386WGS can support up to 32 users and will cost between \$5,000 and \$11,000. And at the top end of its computer family, AT&T introduced the 3B/4000, its most powerful computer to date. Capable of processing up to 40 million instructions per second, the 3B/4000 will cost around \$120,000 in a basic configuration.

... AS UNISYS ADDS TO 'A SERIES' LINE

Unisys Corp. is moving to compete more strongly for low-end customers against IBM Corp. and Digital Equipment Corp. by adding three new Smallframe models to its A-series minicomputer line. Entry prices for the 48-bit deskside machines start at \$25,000 for the A1 processor

and run up to \$145,000 for the A6. The intermediate A4 carries a \$55,000 price tag. Performance ranges from 0.5 million instructions per second for the A1 to 1.6 mips for the A6. All Smallframe models use the same cabinet, allowing easy upgrades. Fully configured systems range from \$59,000 to \$300,000.

U.S. INDUSTRY IS UP 4.5% IN 1st HALF

First-half sales figures for 1987 indicate that the electronics industry may have bounced back from its prolonged slump, but the American Electronics Association is withholding judgment until the year is out. U.S. sales of electronics products and services rose 4.5% in the first six months of 1987, from \$111.2 billion to \$116.1 billion, the Santa Clara, Calif., industry group says. June was the seventh consecutive month in which sales figures bettered the comparable 1986 period—an indication that the rebound from the hard times of 1985 and 1986 has been both strong and steady.

MINI-MAKER ENTERS PC CAD MARKET

Prime Computer Inc., Natick, Mass., has bought privately owned Versacad Corp., a \$6 million company that makes computer-aided-design software for personal computers and work stations. Versacad, of Huntington Beach, Calif., will be an independent subsidiary, selling CAD software for most major stand-alone machines, including those of IBM, Apple, Hewlett-Packard, Olivetti, Sun, and Apollo. Prime already offers CAD software for its own general-purpose multiuser systems.

TRW MAKES AMENDS: \$17 MILLION WORTH

TRW Inc. pleaded guilty to overcharging in U.S. government contracts and will pay \$17 million in restitution, in-

cluding \$2.5 million already paid back for unbillable items by TRW's Military Electronics and Avionics division in San Diego, Calif. Robert L. North (see p. 22), a senior corporate officer of TRW, and Hugo Poza, head of the division, were fired; they have since filed wrongful termination suits and have testified that TRW's contract system was flawed. The company will not be barred from receiving future government contracts.

APOLLO AND RIDGE GO NETWORKING

Work stations and superminicomputers can be tied more closely together as a result of a joint agreement between Apollo Computer Inc. of Chelmsford, Mass., and Ridge Computers of Santa Clara, Calif. Ridge's reduced-instruction-set superminis will be linked to Apollo's work stations via Apollo's Network Computing System. This integrated computing environment is aimed toward engineering and scientific users who want high-performance graphics, networking, and computationally intensive applications such as electrical and mechanical design.

CORNING GETS OUT OF COMPONENTS

Corning Glass Works is bailing out of the electronic components business. The Corning, N. Y., company is selling its capacitor operations to AVX Corp. of Great Neck, N. Y., for \$67 million, and its resistor business, which has plants in the U.S. and Europe, to Vishay Intertechnology Inc. of Malvern, Pa., for \$39 million. AVX and Vishay say they will continue to operate all the Corning plants and retain virtually all of the Corning employees.

13 SIMULATORS USE TERADYNE TESTER

Design simulators from 13 vendors that are used for test-

ing VLSI boards will now run smoothly on Teradyne Inc.'s L200 family of VLSI testers. Test Systems Strategies Inc. of Beaverton, Ore., is supporting the Boston company's L200 series in its Test Development Series software, which creates standard test programs from different simulation waveforms. Multivendor compatibility will allow Teradyne's users to take advantage of test vectors already created for in-circuit testing of application-specific ICs while maintaining the L200 family's timing flexibility.

IBM AND ERICSSON TEAM ON PHONE NET

IBM Europe SA will combine its expertise in data-base and data-network management with the AXE switching technology from Sweden's Ericsson Corp. under a long-term, nonexclusive agreement to build advanced telephone networks. A corporate Virtual Private Network service will recognize a user's call as private and automatically connect it over a normal switched line to another business location. Solutions will be based on standard IBM and Ericsson systems, plus specialized software that is compatible with regional Bell operating companies in the U.S.

SYSTEM PREDICTS DISK-DRIVE FAILURES

An expert system from National Advanced Systems, a Santa Clara, Calif., subsidiary of National Semiconductor Corp., will predict failures in the company's installed NAS 7380 disk-storage subsystems before they happen. Nastrack combines a printed-circuit board and software to monitor seven critical parameters. Data is fed daily to National's central support center in San Diego, and if the system detects a faulty drive, it stores the disk's information and alerts the support center to send a customer representative to the site.

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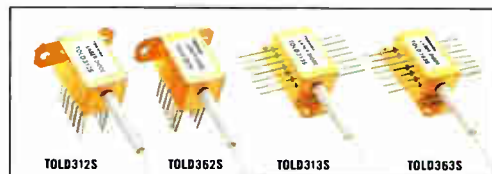


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